Earthing Schemes Enabling Effective Protection and Fault Location Techniques for Low Voltage Direct Current Microgrids

PhD Thesis

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

Growing public awareness and concern about the pollution caused by traditional power generation has sparked a clean energy revolution that is challenging the current century-old power system networks. Existing LV distribution networks are being overstretched to accommodate an increasing number of low-carbon technologies such as electric vehicles (EVs), heat pumps, energy storage, and solar PV generation. This radical shift necessitates significant work to support the systems in order to alleviate the pressure and growth in power demand that are fundamentally challenging the capacity of the existing LV distribution networks. Alternatively, Low Voltage Direct Current (LVDC) microgrids have been identified by a number of industrial and research organisations as one of the most beneficial approaches for alleviating congestion and expanding capacity on existing LV distribution networks in order to meet the anticipated increases in transportation and heat demand. Along with advancements in power electronics and converters, a rising number of applications that operate predominantly with DC is a significant indication of the adoption of the LVDC microgrid infrastructure, with a number of applications, both industrial and consumer-based, that operate largely with DC as a primary power source. However, the lack of existing standards, accurate islanding detection, effective and reliable earthing systems, and DC location and protection solutions have contributed to a challenge to the transition to a fully operated DC distribution architecture.

This thesis is devoted to the development of a reliable and accurate fault location technique, as well as a selective protection scheme that will ensure secure and reliable LVDC microgrid operations, thereby facilitating the transition to widespread implementation of LVDC microgrids.

Typically, the LVDC microgrid's network is interfaced to the AC grid through a two-level voltage source converter (VSC) that regulates the bus voltage. When the VSC converter is disconnected from the utility, the system goes into islanded mode. Rapid and accurate islanding detection (ID) is critical to ensuring that the system disconnects or switches to islanding operation mode. This is particularly challenging in DC systems because some of the variables that are typically used in AC systems to

differentiate islanding events (such as phase and frequency) are absent in DC. Thus, the ROCOV and ROCOC methods are developed in this thesis for the detection of LOM (islanding) events, which in turn allows for the discrimination between islanding and non-islanding events (i.e. Faults). The detection performance of these schemes is evaluated in a variety of simulation scenarios. Besides that, system earthing is a technical challenge in LVDC microgrids, and therefore should be carefully designed to ensure device and user safety while also increasing the microgrid's effectiveness. In this thesis, numerous earthing schemes, including multiple earthing points, have been scrutinised in order to determine the most reliable and effective earthing scheme capable of enabling safe and secure operation in LVDC microgrids. The corresponding understanding of the system's behaviour when the LVDC microgrids are earthed with multiple earthing points during grid-connected and islanded modes, allowing the design of effective DC fault location and protection solutions.

Leveraging these understandings facilitated the development of a method for locating DC faults through the use of multiple capacitive earthing schemes. This proposed technique is capable of estimating the fault location with high accuracy regardless of whether the remote end is connected to DC sources or a load. The enhanced performance of the proposed fault location technique has been validated through simulation studies and laboratory experiments. This enhanced accuracy and reliability facilitates DC faults to be accurately located and enables rapid network reconfiguration and post-fault cable maintenance to take place. In addition, a novel current-based fault detection and isolation technique for LVDC microgrids has been developed and validated through simulation studies and laboratory experiments. The proposed technique is communication-less and relies only on local measurements. The proposed protection scheme has the ability to effectively protect against both solid and highly resistive faults and is capable of discriminating between internal and external faults under both grid-connected and islanded modes. Thus, it eliminates the need for selection of different protection settings for different LVDC topologies.

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List of Abbreviations

AC	Alternate Current
ACCB	Alternate Current Circuit Breaker
AMR	Anisotropic Magneto-Resistance
BESS	Battery Energy Storge System
CMV	Common Mode Voltage
DC	Direct Current
DG	Distributed Generator
DOD	Depth of Discharge
EVs	Electric Vehicles
FCL	Fault Current Limiter
ID	Islanding Detection
IGBT	Insulated Gate Bipolar Transistor
IT	Isolated-Terre
LV	Low Voltage
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
MAF	Moving Average Filter
MCCB	Molded-Case Circuit Breaker
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MMC	Modular Multilevel Converter
MPPT	Maximum Power Point Tracking
MVDC	Medium Voltage Direct Current

NDZ	Non-Detection Zone
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PEN	Protective Earth Neutral
PET	Power Electronics Transformer
PI	Proportional Integral (Controller)
PLL	Phase Lock Loop
PoE	Power over Ethernet
PPU	Power Probe Unit
PV	Photovoltaics
PWM	Pulse Width Modulation
P&O	Perturb and Observe (MPPT method)
RCD	Residual Current Device
RES	Renewable Energy Source
RLC	Resistance-Inductance-Capacitance
ROCOC	Rate of Change of Current
ROCOF	Rate of Change of Frequency
ROCOV	Rate of Change of Voltage
SOC	State of Charge
SSCB	Solid State Circuit Breaker
SST	Solid State Transformer
TN	Terre-Neutral
TT	Terre-Terre
TVS	Transient Voltage Suppression
UIE	Unintentional Islanding Event
USB	Universal Serial Bus
VSC	Voltage Source Converter

Chapter 1

Introduction

1.1 Research Context

The depletion of fossil fuels and their environmental impact have stimulated extensive research into more inclusive, secure, cost-effective, and low-carbon distribution power systems. Renewable energy resources, particularly wind and solar photovoltaic (PV), have grown at an unprecedented rate in recent years, increasing the demand for advanced power electronics technology. According to the Energy Information Administration (EIA), world net electricity generation from energy sources will increase from 24TWh to 44TWh between 2018 and 2050, as shown in Figure 1.1. Renewable energy sources are the fastest growing sources of electricity generation, with average annual increases of 2.8% beginning in 2018 and projected to continue until 2050 [1].

The substantial growth in sales of electric vehicles (EVs) globally is placing additional pressure on existing low-voltage (LV) distribution networks. Over 2 million electric cars, 345 thousand electric buses, and 200 million electric motorcycles (mostly from China) were deployed globally in 2016 [2]. Besides that, many governments around the world have decided to phase out the sale of fossil-fuel-powered automobiles in the near future. This is already a reality in Norway (by 2025), the Netherlands (by 2030), and Scotland (by 2032), to name a few [2]. Additionally, the ability of power systems to cope effectively with the variability and uncertainty associated with renewable energy generation, the integration of vehicle electrification into existing systems, and the attempt to avoid renewable energy sources being curtailed in order to meet consumer demand for reliable energy, all place an increasing demand on system flexibility.

In light of recent advancements in power electronic converters and the growing number of applications that are inherently powered by DC systems, as well as recent power grid failures in some countries as a result of natural disasters or severe weather, a number of industrial and research organisations have identified Low Voltage Direct

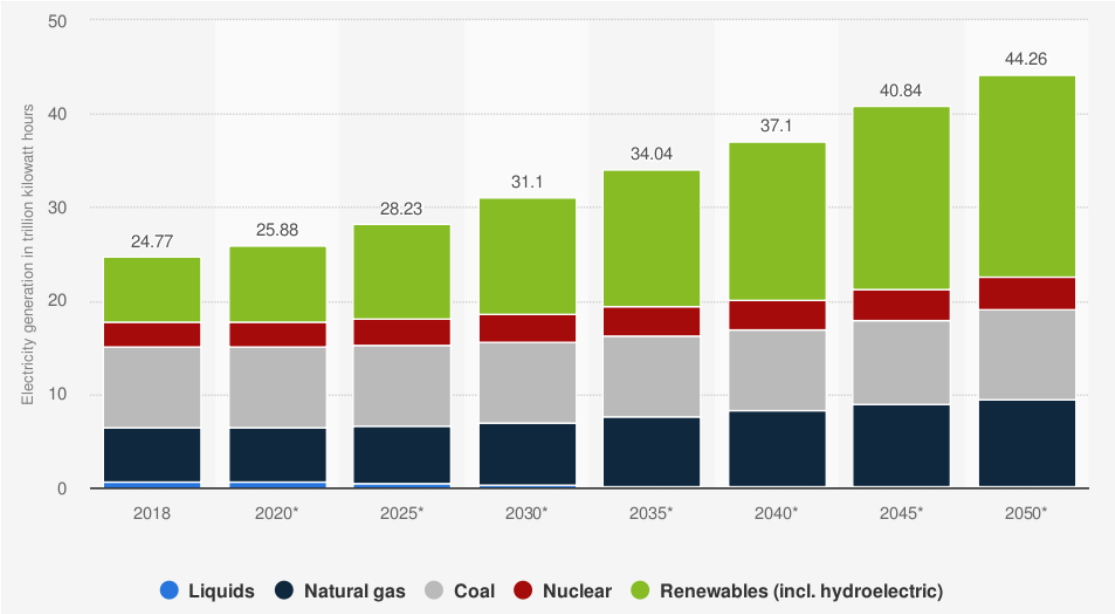

Figure 1.1: World net electricity generation by energy source in trillion kilowatt-hours [1].

Current (LVDC) microgrids as a preferred solution [3]. The primary motivation for LVDC microgrids is that the vast majority of distributed renewable energy sources (RES, e.g. photovoltaics), fuel cells and batteries (e.g. those used in electric vehicles), are inherently DC [4, 5]. Through transitioning the distribution grid from AC to DC, the need for DC/AC and AC/DC conversions is significantly reduced, thereby eliminating conversion losses (refer to Figure 1.2). Additionally, DC systems have the advantages of being easily integrated into the grid, allowing for better control and coordination of RES, and allowing for easy management of RES generation and load fluctuations through the use of a battery energy source [4].

The International Electrotechnical Commission (IEC) published technical guidance and standards to facilitate the transition toward increased LVDC adoption [7]. Numerous researchers and the IEC have identified several challenging areas that should be addressed in order to ensure the safe and stable operation of LVDC microgids, including the implementation of effective earthing systems, enhanced DC fault location techniques, and enhanced DC protection solutions [8]. Generally, the way the main grid and the LVDC microgrid are interfaced has a significant impact on the design and performance of LVDC protection schemes. Usually, an LVDC microgrid will have multiple converters connected to the DC bus, including two-level Voltage Source Converters (VSCs), which are frequently used to connect LVDC microgrids to the AC grid due to their simplicity and low cost, and buck-boost converters. However, one of the challenges associated with protecting a VSC-based LVDC microgrid is detecting and

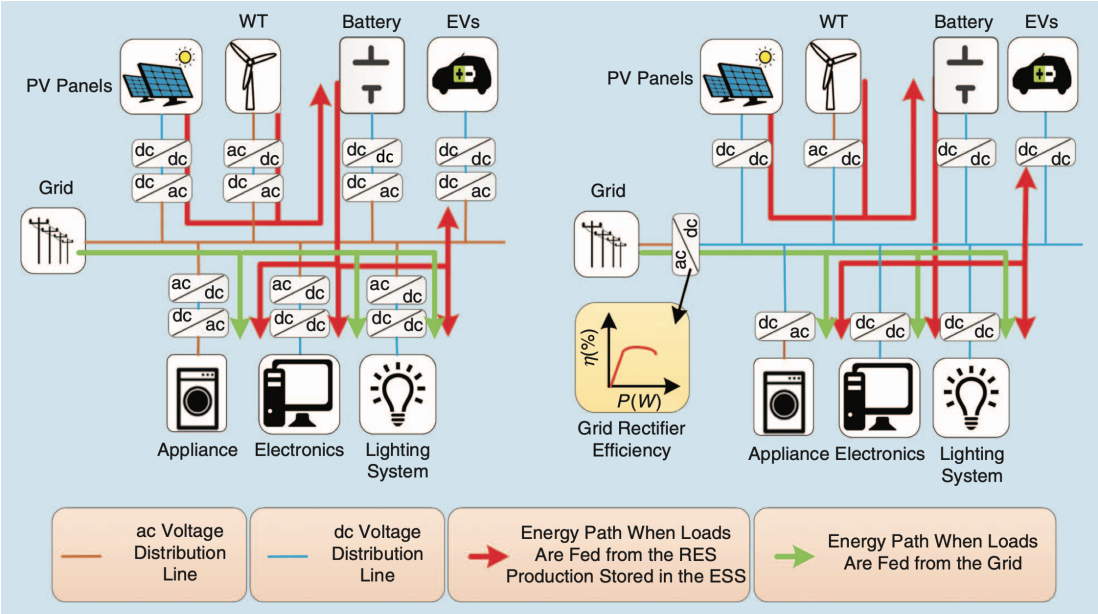

Figure 1.2: Comparison between a LVAC distribution line (left) with a LVDC distribution line (right). LVDC distribution line allows the elimination of many dc/ac conversion stages taken from [6] with minor modification.

extinguishing DC fault current quickly. This is because the typical two-level VSC's DC fault current withstand rating is only twice the converter full-load current. Therefore, implementing existing AC protection strategies for the LVDC microgrid will be insufficient to ensure safe and secure operation in the future. Some of the world's leading DC protection schemes are developing DC circuit breakers, but these technologies are not yet cost effective for distribution level deployment.

Overall, LVDC microgrids have begun to be adopted in standalone and transport applications. However, the absence of international standards for DC operating voltages, earthing systems, and advanced DC protection methodologies, all contribute to the technology's slow adoption at the distribution level.

The following are the primary challenges that this thesis will address and briefly describe in light of these implications.

- There have been more contributions to research on islanding detection methods in recent years, particularly for LVAC microgrids [9, 10], but the same techniques cannot be applied to LVDC microgrids. This is because, the only magnitude variables that can be affected in LVDC microgrids during an islanding event are the voltage and current; thus, methods based on frequency, such as the Rate of Change of Frequency (ROCOF) [11, 12], and those based on phase variation [13], cannot be implemented on LVDC microgrids. Therefore, it is necessary to comprehend and investigate islanding detection methods for LVDC microgrids,

as well as to define their capability to distinguish between non-islanding and islanding events. This will facilitate the understanding of how islanding events in DC systems can be detected and, ultimately, in the design of an effective protection solution.

- LVAC microgrids frequently incorporate a central earthing point based on a TN-S earthing scheme. In LVDC microgrids, it is preferable to use a TN-S earthing scheme. However, a single earth point is insufficient if the system is composed of multiple decentralised sources. This will have consequences for the protection and earthing of the systems. Additionally, when an islanding event results in the loss of a DC microgrid's earthing system, a local earthing system is required to act as a path for earth fault current to flow through the earthing system. Therefore, it is necessary to understand the fault characteristics of the LVDC microgrid in grid-connected and islanded modes using a single earthing point and multiple earthing points in order to determine how DC systems should be earthed and how corrosion issues can be avoided using a capacitive earthing scheme.

- There is a need to improve the accuracy and reliability of LVDC fault location estimation within LVDC microgrids in order to facilitate effective post-fault network maintenance. Existing LVDC fault distance estimation methods rely on additional hardware to locate a fault, increasing the network's cost and requiring a repair crew to relocate external equipment, while others rely on communication between the converters, implying a reliability issue if the communication channel is lost. Meanwhile, existing fault location techniques are ineffective at determining the fault current contributions of remote end converters (i.e., DC loads or DC sources), negatively impacting the accuracy of their local measurement-based methods.

- LVDC protection presents a challenge due to the absence of a zero crossing point. As a result, faults are more difficult to interrupt with fuses and circuit breakers than they are with AC protection. Additionally, converter-based DG sources operating in islanded mode contribute a small amount of fault current, necessitating the development of a protection scheme capable of detecting very small DC fault currents. Likewise, a high-impedance fault can be difficult to detect because the fault current is unlikely to trip the overcurrent protection and is more likely to be confused with a load step-up change, making the comparison between the two difficult. Furthermore, existing protection methods have been developed for LVDC microgrids operating in grid connected or standalone mode; a few of them can protect the network in both modes of operation. Thus, it is vital for devel-

oping a protection solution that is capable of providing effective fault detection and discrimination between upstream and downstream faults, is less sensitive to resistive faults, does not rely on current magnitude, and can protect the network in both operation modes.

In light of this, there are new opportunities to expand existing knowledge and develop novel fault location and protection solutions for LVDC microgrids, thereby addressing the identified gap. To this end, the thesis's primary work focuses on the development of effective fault location and protection techniques for LVDC microgrids that can accelerate restoration, reduce system downtime, and guarantee system reliability and availability at all times for the consumer, as well as to operate in both grid-connected and islanded modes, ensuring a seamless transition between system configurations. This is based on an examination, analysis, and identification of the limitations of existing DC fault location and protection solutions. Following that, a novel fault location estimation technique based on multiple capacitive earthing schemes, as well as fault detection and isolation for LVDC microgrids using the sign of the current of the second derivatives technique, are proposed to ensure the safe and reliable operation of future LVDC microgrids.

1.2 Research Contributions

This thesis provides the following contributions to knowledge:

- A demonstration and analysis of new passive islanding detection techniques for use in LVDC microgrids with a zero or near-zero power mismatch has been conducted. The proposed methods are based on calculating the rate of change of voltage (ROCOV) and current (ROCOC) in order to detect LVDC microgrid islanding events. A simulation analysis was performed to determine these methods' ability to distinguish between non-islanding (e.g. load step changes and transient fault currents) and islanding events.

- An investigation of various earthing schemes to determine their suitability for LVDC microgrids has been performed. This includes a comparison of the contribution of fault current that flows from the VSC converter during fault conditions. Additionally, a detailed fault characterisation using multiple earthing points (capacitive earthing scheme) for LVDC microgrids operating in grid-connected and islanded modes was performed. This enables a better understanding of the system's behaviour when the LVDC microgrids are earthed with multiple earthing points during grid-connected and islanded modes, allowing for the design of ef-

fective protection solutions. The results of the study have been published in a journal paper.

- Two novel techniques for estimating the fault distance, based on single and multiple capacitive earthing schemes, have been developed and tested. The first proposed method employs the Moore-Penrose Pseudo Invers technique in combination with Moving Average and Savitzky Golay filters to accurately estimate the inductance value between the capacitor earthing and the fault, thereby defining the fault location in a LVDC microgrid network and received the best paper at an international conference on DC microgirds. The second proposed method is capable of estimating the fault location with high accuracy regardless of whether the DC source or load is connected to the remote end. The proposed fault location method's accuracy and reliability are evaluated using LVDC microgrid detail modelling and further validated using a scaled-down laboratory prototype. This work is described in a journal publication.

- A novel current-based fault detection and isolation technique for LVDC microgrids has been developed and tested using a scaled-down laboratory prototype. The proposed protection scheme has the ability to effectively protect against both solid and highly resistive faults and is capable of discriminating between internal and external faults under both grid-connected and islanded modes. Thus, it eliminates the need for selection of different protection settings for different LVDC topologies. The proposed technique is communication-less and relies only on local measurements. This novel technique is currently being evaluated by a peer-reviewed journal.

1.3 Thesis Overview

Outline of the work contained within this thesis is presented below:

Chapter 2: This chapter outlines the key factors promoting the adoption of LVDC microgrids, highlighting increased pressure on existing LV networks, advancements in power electronics, an increase in the number of DC-operated applications, and the demonstrated benefits of LVDC, all of which contribute to the transition to LVDC microgrid. The chapter then discusses the evolution of LVDC microgrids, including the concept of LVDC microgrids, the development of an international and regional LVDC standard, and descriptions of LVDC pilot projects. Additionally, this chapter discusses the challenges associated with islanding detection methods for LVDC microgrids. In

light of this, two passive islanding detection methods are presented in detail. Furthermore, LVDC technologies such as LVDC interfaces and earthing requirements are discussed, as well as the corrosion effects on LVDC networks, DC protection devices, and measurements. The chapter concludes by identifying the technical and economic challenges associated with expanding the use of LVDC microgrids. The discussion established the primary research themes for this work.

Chapter 3: This chapter investigates various earthing schemes to determine their suitability for LVDC microgrids and compares them under faulted conditions in order to determine the most reliable and effective earthing scheme capable of enabling safe and secure operation in LVDC microgrids. Following that, a detailed fault characterisation using multiple earthing points (capacitive earthing scheme) for LVDC microgrids operating in grid-connected and islanded modes is performed. This enables a better understanding of the system's behaviour when the LVDC microgrids are earthed with multiple earthing points during grid-connected and islanded modes, allowing for the design of effective protection solutions.

Chapter 4: This chapter describes the development of two novel fault location algorithms for LVDC microgrids that facilitate faster system restoration following a fault and reduce power outage time. The chapter begins by highlighting the limitations of the existing fault location techniques when LVDC feeders are connected to renewable energy sources through remote end converters. On the basis of these discussions, two novel techniques for estimating the fault distance that make use of a capacitive earthing scheme are discussed in detail. The accuracy and reliability of the proposed fault location methods are evaluated using detailed modelling of an LVDC microgrid and further validated using a scaled-down laboratory prototype.

Chapter 5: This chapter discusses the development of novel current-based fault detection and isolation technique. The chapter begins by highlighting the limitations of conventional LV current-based protection schemes, before introducing a novel current-based protection scheme that utilises DC current concavity (sign of d^2I/dt^2) to discriminate between internal and external faults. Finally, the feasibility of the proposed method is verified by an experimental model that provides laboratory characterisation of LVDC microgrid fault behaviours.

Chapter 6: This chapter summarises the research's contributions and identifies the remaining opportunities for future work. By addressing issues such as earthing systems, fault location estimation, and fault detection and isolation, the findings of this research

will significantly facilitate the transition to LVDC microgrids, which will be beneficial to all stakeholders.

Figure 1.3 provides an overview of this thesis and the core focus of the work in each chapter.

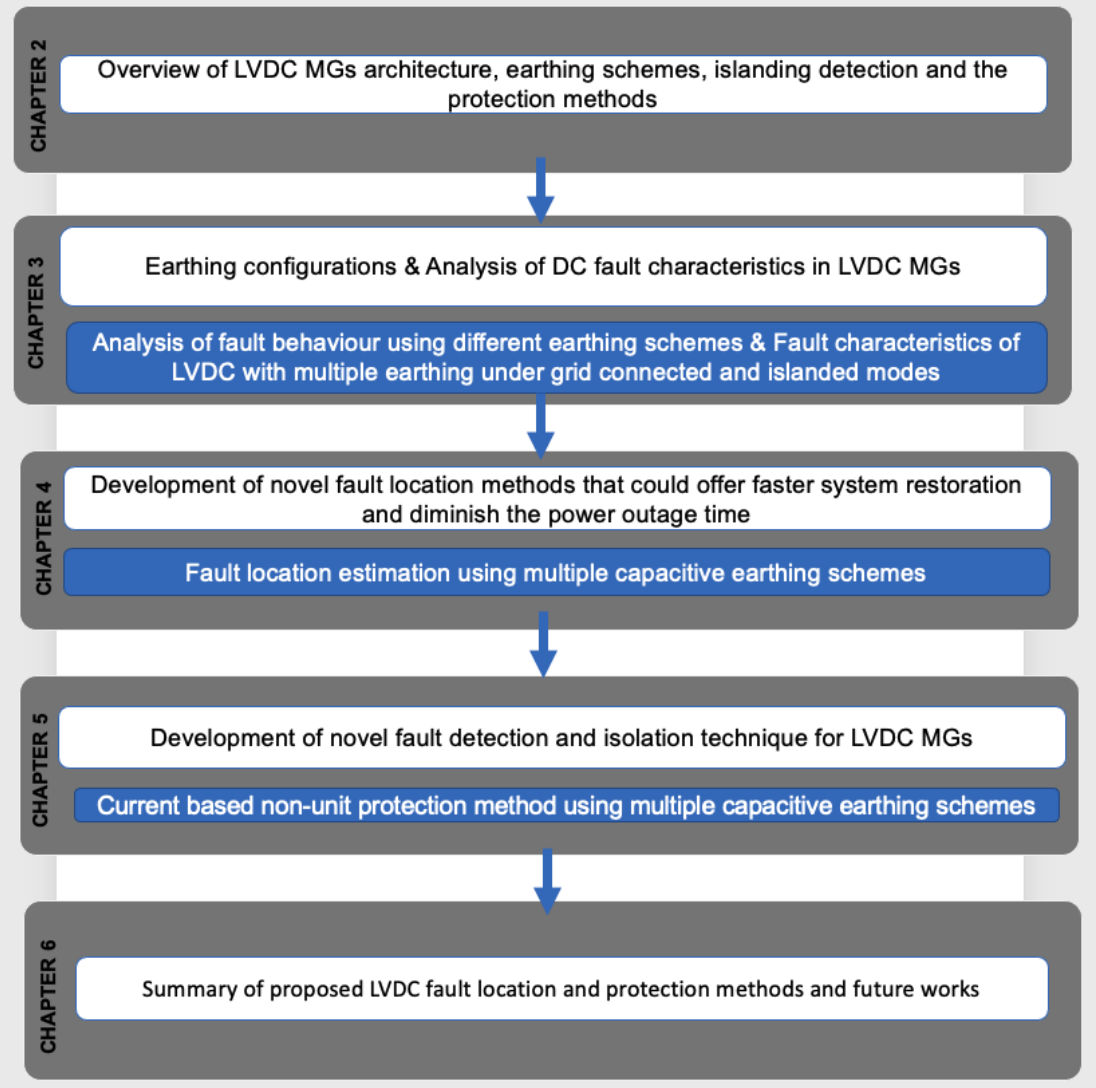

Figure 1.3: Overview of thesis chapters and outputs.

1.4 Publications

The work undertaken through the course of this PhD has contributed to the following publications:

1.4.1 Journal Articles

Published

- **A. Makkieh**, V. Psaras, R. Peña-Alzola, D. Tzelepis, A. Emhemed and G. Burt, "Fault Location in DC Microgrids based on a Multiple Capacitive Earthing Scheme," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2020.2995946.
- **A. Makkieh**, A. Emhemed, D. Wang, A. Junyent-Ferre and G. Burt, "Investigation of different system earthing schemes for protection of low-voltage DC microgrids," in The Journal of Engineering, vol. 2019, no. 18, pp. 5129-5133, 7 2019, doi: 10.1049/joe.2018.9365.

Under Review

- **A. Makkieh**, R. Peña-Alzola, L. Mackay and G. Burt, "Current Based Non-Unit Protection for DC Microgrids Using A Capacitive Earthing Scheme," in IEEE Transactions on Smart Grid.

1.4.2 Conference Papers

Published

- **A. Makkieh**, A. Emhemed, D. Wang, G. Burt, S. Strachan and A. Junyent-Ferre, "Fault Characterisation of a DC Microgrid with Multiple Earthing under Grid Connected and Islanded Operations," 2018 53rd International Universities Power Engineering Conference (UPEC), Glasgow, 2018, pp. 1-6, doi: 10.1109/UPEC.2018.8541892.
- **A. Makkieh**, A. Florida-James, D. Tzelepis, A. Emhemed, G. Burt, S. Strachau and A. Junyent-Ferre, "Assessment of Passive Islanding Detection Methods for DC Microgrids," 15th IET International Conference on AC and DC Power Transmission (ACDC 2019), Coventry, UK, 2019, pp. 1-6, doi: 10.1049/cp.2019.0016.

- **A. Makkieh**, A. Emhemed, R. Peña-Alzola, G. Burt, and A. Junyent-Ferre, "Capacitive Earthing Charge-Based Method for Locating Faults within a DC Microgrid,"In 3rd IEEE International Conference on DC Microgrids (ICDCM 2019), Matsue, Japan, 2019, pp. 1-6. (Best Paper Award)

1.4.3 Contributing to Report

Having led a survey of academic/research institutions engaged in LV/MV DC system research and was a co-author of the CIRED working group's first DC distribution network report.

G. Jambrich and et al. DC Networks on the Distribution Level – New Trend or Vision? Liège, Belgium, 2021. 113 p. (DC Distribution Networks).

Chapter 2

LVDC Microgrids: Architecture, Technologies and Protection

2.1 Introduction

This chapter will briefly discuss the key drivers for the adoption of LVDC microgrids, emphasising the increase pressure on existing LV networks, advancements in power electronics, an increase in the number of DC-operated applications, and the demonstrated benefits of LVDC, all of which are facilitating the transition to LVDC microgrids. Following that, the evolution of LVDC microgrids will be discussed, including the concept, development of an international and regional standard for LVDC, and descriptions of LVDC pilot projects. Additionally, LVDC technologies will be described, including LVDC interfaces and earthing requirements, as well as the effects of corrosion on LVDC networks, DC protection devices, and measurements. In this chapter, the existing technical and economic barriers to expanding the use of LVDC microgrids will be identified.

2.2 Drivers for the development of an LVDC microgrids

There are four key drivers for facilitating the transition from existing LV networks to LVDC microgrids, including increased pressure on existing LV networks, advancements in power electronics, an increase in the number of DC-operated applications, and the demonstrated benefits of LVDC.

2.2.1 The pressure placed on the existing LV network

Growing public awareness and concern about the pollution caused by traditional power generation has sparked a clean energy revolution that is challenging the current century-old power system networks. Existing LV networks are being overstretched to accommo-

date an increasing number of low-carbon technologies such as electric vehicles (EVs), heat pumps, energy storage, and solar PV generation. This trend is expected to continue, as legislation establishes ambitious targets. Many countries, like Norway, Germany, and the UK, will ban the sale of gasoline and diesel vehicles and replace them with EVs by 2025, 2030, and 2040 respectively [14]. This radical shift in the transportation sector will significantly increase pressure on existing LV networks. In the UK a high deployment of electric vehicles is expected to result in an annual demand of up to 90TWh by 2050 under a future low carbon scenario [15]. This is a 30% increase in demand over 2017. Another low-carbon technology, heat pumps, are expected to become prominent in the UK by 2050, resulting in a 70% reduction in the usage of gas boilers [15]. These will be required significant investment, estimated at £30-45 billion for the UK grid. Therefore, radical changes to LV networks will be required to meet anticipated demand increases [16]. This will necessitate significant work to support the systems in order to alleviate the pressure and growth in power demand that fundamentally challenges the capacity of the existing LV networks. A number of industrial and research organisations have recently identified LVDC microgrid distribution as one of the beneficial approaches for alleviating congestion and expanding capacity on existing LV networks in order to meet the anticipated increases in transport and heat demand [17].

2.2.2 Utilization of power electronics is increasing

The advancement of power electronic technologies is a vital element in facilitating the transition to a LVDC microgrid distribution network. The Insulated Gate Bipolar Transistor (IGBT), for example, has been utilized in the majority of power electronic applications in recent years, particularly with medium and high power equipment (e.g. wind and solar generation) [18]. Years later, as demand for high-power density devices increases, Gallium nitride (GaN) and silicon carbide (SiC) devices have altered the landscape of the energy sectors. These devices provide significant advantages over MOSFETs and IGBTs, including the ability to operate at significantly higher temperatures, have a greater current density, have lower switching losses, and enable higher switching frequencies [19]. The advancement of power electronics has increased the likelihood that LVDC microgrids will include converters that are more compact and smaller in size than typical AC transformers in LVAC networks. In addition, power electronics improvements have revolutionised the state of the art in AC/DC and DC/DC conversion topologies, resulting in more efficient and advanced AC/DC and DC/DC conversions. One notable development is the use of solid-state transformers (SSTs) that utilise high-frequency galvanic isolation. Typically, an SST is substantially smaller in size than a

normal 50Hz AC transformer, and it can provide more efficient and flexible voltage and power management capabilities for MVDC, LVDC, and LVAC supplies [20]. Through the development of power converters, the transition from almost LVAC systems to hybrid AC/DC or entirely LVDC microgrids can be made much more efficiently.

2.2.3 Growing number of applications operate with LVDC

Along with advancements in power electronics and converters, a rising number of applications that operate predominantly with DC is a significant indication of the adoption of the LVDC microgrid infrastructure, with a number of applications, both industrial and consumer-based, that operate largely with DC as a primary power source. The market has been represented by DC ready applications for a long time, including telecommunications [21], data centres [22], marine applications [23], and rail transportation [24]. Renewable energy generation technologies such as solar photovoltaic have also been increasingly utilized as a cost-competitive renewable energy source, with the generated DC power being directly stored in a supplementary battery energy storage system (BESS) or supplied to AC feeders [25].

On the customer end, there are a variety of DC-ready technologies, including cooling and heating (for example, radiant heating [26] and air conditioners [27]), refrigeration [28], and lighting systems [29]. Additionally, there has been a rapid uptake of Light-Emitting Diode (LED) lights due to their great energy efficiency and short payback period [30], with the majority of LED bulbs operating on AC with an inbuilt converter. DC LEDs, on the other hand, can operate on a dedicated DC network and have been shown to be more efficient, delivering higher lighting quality while also being more resilient to voltage fluctuations [31], among other advantages. In addition, an increasing number of companies are now developing Power over Ethernet (PoE) lighting solutions for commercial and residential buildings, which are becoming increasingly popular. In terms of transportation, electric vehicles are developing rapidly as they become a vital factor in society's decarburization [32]. Numerous automobile manufacturers, including Mercedes, Audi, BMW, Toyota , and Nissan, have produced electric vehicles that can be charged directly from DC power [33]. Besides that, the advancement of sophisticated DC rapid chargers alleviates concerns about mileage range, charging accessibility, and charging time [34]. Furthermore, the number of end-user appliances requiring DC continues to grow, including mobile phones and computers. The Universal Serial Bus (USB) is an example of a commonly used DC system that is available in almost all personal computers and desktop computers and requires a rectifier to convert AC power to DC. To this end, transitioning to an LVDC microgrid distribution network is a more efficient method of interconnecting these DC-ready applications as it avoids multiple

conversions and thus losses. The following section will discuss the energy and cost reductions associated with implementing an LVDC network.

2.2.4 Energy savings and cost reductions are conceivable with LVDC applications

In certain developing nations, the medium of DC offers electricity access to 1.2 billion people, allowing them to significantly improve their quality of life [7, 35]. This is primarily due to the fact that solar PV panels have become more affordable and lithium ion batteries have become more efficient. At the same time, the development of LED lighting enables the rapid expansion of locally installed and operated systems that do not require a connection to the main grid, which is frequently more difficult to do in the case of many developing nations. In addition, there is no necessity for synchronisation when connecting DC power generation to LVDC microgrids network, and, unlike with AC transmission, there is no need to consider skin effect in the cables. In terms of cabling, DC is more efficient and transmits more power than AC since the current density is dispersed uniformly throughout the whole cable cross-section. Along with these numerous exceptional benefits of DC, various additional benefits related to LVDC applications have been reported through modelling, experimental verifications, and pilot projects. There are numerous devices that operate entirely on DC and are more efficient than their AC counterparts [36]. In the case of LED lighting systems, a study reported in [37] indicated that LED lighting systems powered by DC solar energy can save up to 5% on annual costs when compared to LED lighting systems powered by AC solar energy.

The implementation of LVDC microgrids has been demonstrated to be a more effective solution in a variety of applications, including rural and urban distribution networks, as well as marine systems. In rural areas, LVDC microgrids have been demonstrated to be an effective approach for replacing ageing MV lines supplying light loads, saving up to 10% to 25% in life cycle costs and 5% in operational costs when compared to conventional reinforcing methods [38]. The cost savings are associated with the reduction of rural network maintenance costs as a result of the enhanced automation provided by LVDC microgrid systems and converter control functionalities. In urban populations, improved energy management is required to manage increased loads and avoid additional costs associated with LV network reinforcement. Thereby, LVDC solutions have been reported to be attractive due to their ability to increase the capacity of the local grid without requiring large capital expenditures. For example, Philips has installed a grid-connected DC system in an office on the Eindhoven (Netherlands) High Tech Campus, using a 2kW LED lighting system as load and a hybrid supply

from a 2kW solar power system and a 2kW central rectifier, and compared its energy performance to that of an equivalent AC system. According to their study, the system saves 2% of energy and the efficiency advantage can reach 5% when the power level is doubled. These savings can be attributed to lower losses in an AC/DC rectifier and power-factor-correction circuits as a result of the use of natural DC electricity sources such as PV solar power systems, as well as lower losses in power cables when operating at 380 V DC instead of 230 V AC [22]. ABB has developed an Onboard DC Grid system for marine use, which is capable of distributing electricity on board ships. It is suitable for any electrical ship application up to a maximum of 20MW and operates at a nominal voltage of 1000V DC. The primary benefit of this approach is a reduction in fuel consumption up to a 27% reduction in the consumption of specific fuel oil. Additionally, the system enables significant weight and space savings, resulting in increased cargo capacity [23].

The identified key drivers indicate a wider awareness of the advantages that a transition to LVDC microgrids can provide by easing the pressures associated with hosting an increasing number of renewable energy installations and electrified heat and transportation loads. Power electronics advancements and the growing number of DC-based applications are accelerating the transition to an LVDC power grid. Additionally, the economic advantages of existing DC-powered applications and DC pilot projects demonstrate that LVDC microgrids have the potential to be the more efficient method of distributing power at low voltage. The following sections will provide an overview of the LVDC standards, pilot projects, and technologies that have been developed.

2.3 The evolution of the LVDC microgrids

This section introduces the concept of LVDC microgrids and their topologies. The operation of LVDC microgrids and the introduction of islanding detection methods are also covered in this section. Finally, a brief description of LVDC solutions and pilot projects is provided, along with an overview of the development of the international standard and guidelines for LVDC.

2.3.1 LVDC microgrid concept

Traditional Alternating Current (AC) power systems have been designed to transfer central station AC power to AC powered businesses and households, via high-voltage transmission lines and lower-voltage distribution lines. It is well known that for more than a century, the AC current has established itself as the worldwide standard in electrical power distribution. With the depletion of fossil fuels, the struggle to reduce

the emission of greenhouse gases and the increasing demand for greener energy, there has been a growing need to build innovative energy control and management architectures that allow for smart grid techniques to be implemented at the power distribution level [39, 40]. During the last 10 years, several research works propose the study of DC current applications, especially for buildings (refer to Table 2.1). DC distribution architectures facilitate the integration of distributed renewable energy sources, increase system efficiency, and improve grid resilience and management in the event of grid failure (e.g. islanding mode) [41]. Additionally, DC distribution architectures distinguish themselves from their AC counterparts due to the nonexistence of reactive power flows, frequency regulation and power quality issues, allowing simpler control and robust stability. Furthermore, today's consumer equipment/household appliances (e.g. computers, mobiles, LED lighting, variable speed drivers) and renewable energy plants are operating on DC current [40]. However, the lack of existing standards and protection methodologies has contributed to a challenging transition to a fully operated DC distribution architecture [40]. In traditional AC bus distribution, the local microgrid produces DC power that is converted to AC power to supply a building's electric system; this power then has to be reconverted to DC for many end users. This AC-DC conversion will result in substantial losses and costs.

Moreover, distributed renewable generation (i.e. solar photovoltaic panels and storage energy systems) produces a DC power, and must be converted to AC to tie into the buildings electric system. Therefore, a new concept of LVDC microgrid has been proposed to make a DC grid incorporated within a building or several buildings, which can eliminate these conversion losses entirely. In addition, the DC output power of solar photovoltaic panel and other distributed DC generation can be used directly without conversion into low voltage direct current (LVDC) distribution system (elimination of one or two energy conversion stages, absence of reactive power and harmonics) [40]. When LVDC microgrids are decoupled from the AC grid (even when not completely islanded), it makes the end-user equipment on the LVDC microgrid less susceptible to frequency and voltage disturbances from the AC grid [39]. The ability of a DC system to seamlessly act as an islanded microgrid can increase system reliability, resiliency and addresses the government's strategic plan for disaster mitigation [39]. In addition, DC bus distribution is highly compatible with electricity storage, which may increase the efficiency of plug-in hybrid electric vehicles and electric vehicles, for which the number is supposed to increase in a few years.

Table 2.1: Demonstration sites for LVDC microgrids in residential and commercial buildings

Description	**Voltage**	**Rating**	**Power sources**	**Benefit Achieved**	**Country**
Experimental system, combined energy and heat system	380 V	N/A	PV, BESS, EV, biomass	Utilization of RES	Japan
Use of active comprehensive protection (ACP)	600-220 V	128 kW	PV, BESS	Utilization of RES	China
Use of EMS, 48,24 and 12 V for DC loads, use of high-speed DCCBs	380 V	N/A	PV, BESS	Utilization of RES	Japan
Energy and heating system (Mitsubishi)	380 V	N/A	PV, BESS,EVs	Utilization of RES	Japan
Distributes DC and AC power to various DC an AC end-use loads (Hawaii Natural Energy Institute)	380 V	500 kW	PV, WT, fuel cells	Utilization of RES	USA
Distributes DC and AC power to various DC an AC end-use loads (Hawaii Natural Energy Institute)	380 V	500 kW	PV, WT, Fuel cells	Utilization of RES	USA
Centralized EMS, No grounding, ±190 V at customer side	± 750 V	500 kW	PV, WT, BESS, EV	Controllability	Korea
DC office building test bed	380V	30kW	PV	Efficiency (energy saving) and cost	Germany
Grid-connected, PV-powered DC test bed installation for an office LED lighting system in Eindhoven High Tech Campus (Philips)	380V	2 kW	PV	Efficiency (energy saving) and cost	Netherlands
Smart home devices, ZigBee, EMS	380V	N/A	PV, WT, BESS, CHP, EVs	Utilization of RES	Denmark

2.3.2 Topology/Architecture and Classification

There are a number of LVDC microgrid configurations that have been reported in the literature, for example, radial and ring (i.e. loop) configurations. For the purpose of

this thesis, radial configuration is going to be the focus of this study as it is the most commonly used due to being frequently employed in practical industrial applications [42]. The radial LVDC microgrid is interfaced with an AC grid on one side through an AC/DC converter (e.g. two-level voltage source converter, 2L-VSC) and the loads on the other side (AC or DC). Therefore, only a single DC bus is connected between the distributed generations and the loads. This DC bus can be unipolar or bipolar depending on the requirements and type of the applications. In a unipolar DC system, the sources and loads are connected between two conductors, the positive and negative poles of the DC bus, as depicted in Figure 2.1.

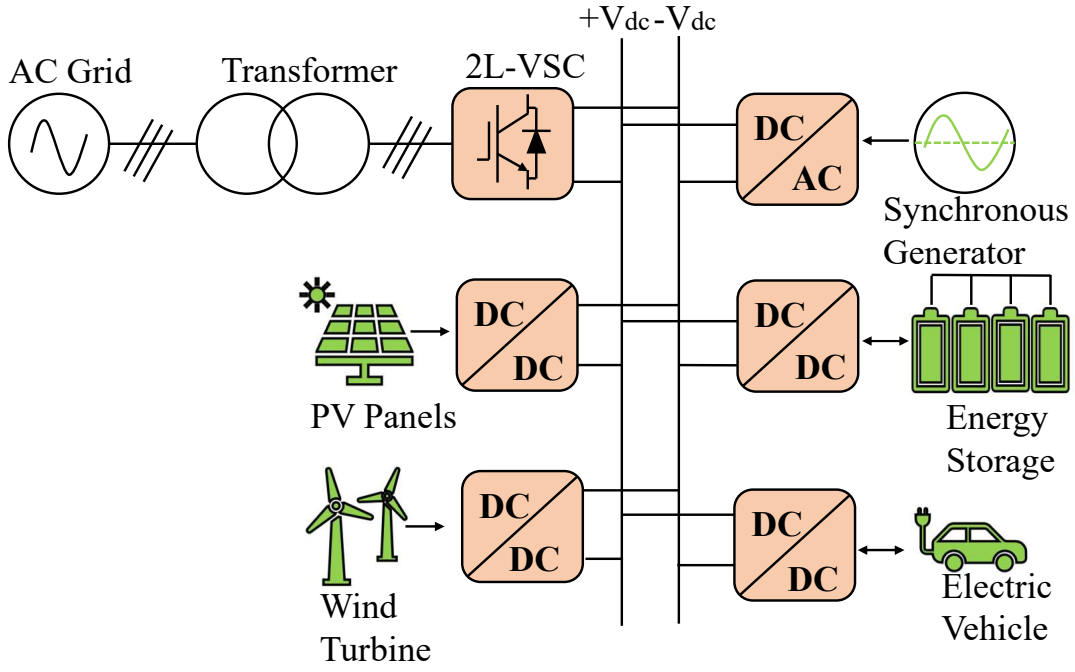

Figure 2.1: Unipolar LVDC microgrid bus architecture

The unipolar DC system has one DC voltage level for power transmission. Therefore, the selection of the DC voltage level is a key element in this type of system. This is because a higher voltage level will increase the power transmission capacity, but it can possibly increase safety risks on the customer side. With a low voltage level, the power transmission capacity is limited to a short distance. However, it can prevent the installation of a large number of DC/DC converters. Overall, the unipolar DC system is simple to implement in the rural areas. However, it does not provide any redundancy, in practice, during fault conditions. In a bipolar DC system, the sources and loads are connected to a three-wire DC bus system, the positive, negative, and earth poles of the DC bus as illustrated in Figure 2.2.

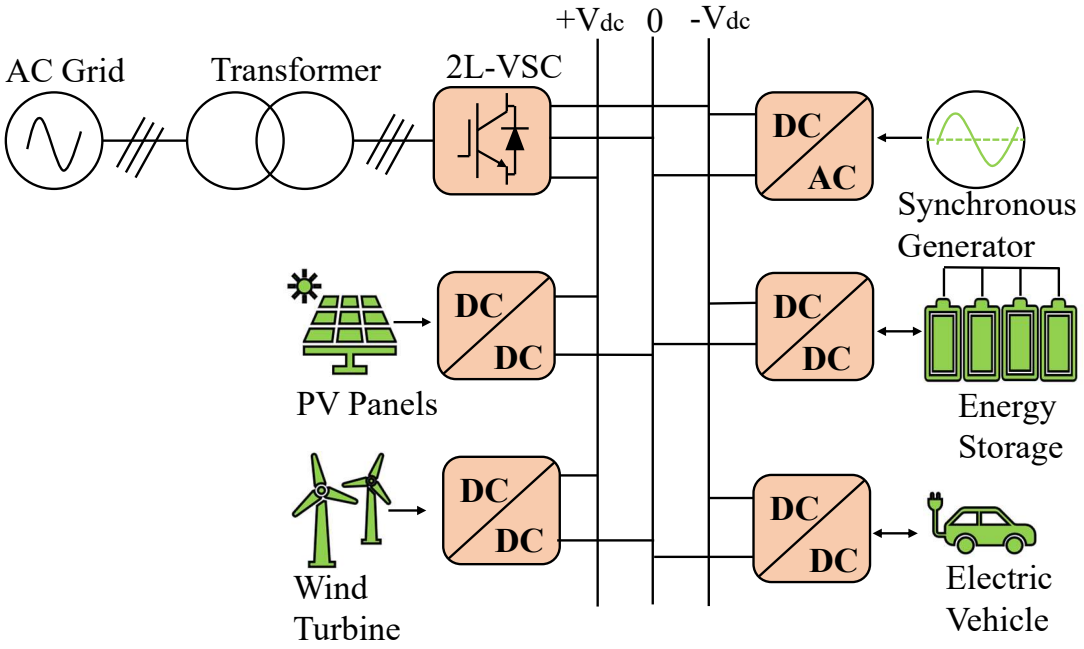

Figure 2.2: Bipolar LVDC microgrid bus architecture

In this configuration, the customers have the option to connect to three different voltage levels: positive pole to earth or negative pole to earth or between the positive and negative poles. This results in increased reliability and flexibility during faulted conditions. As an example, if a DC fault occurs on one of the DC poles, the power can still be supplied by a two-wire (unipolar) network. Furthermore, the bipolar DC system has a wider range of DC voltage levels compared to the unipolar DC system, but it requires more components in order to connect different loads. This may result in an unbalanced system when the loads are not identically connected. Therefore, a voltage balancer circuit is recommended for this type of system [43].

2.3.3 Operation of a LVDC microgrids

LVDC microgrids usually consist of a combination of PV arrays, wind turbines, DC converters, and loads. The control of the LVDC microgrid can be operated either connected or islanded from the grid (refer to Figure 2.3). The islanded mode in a microgrid happens due to unplanned events such as faults (Unintentional Islanded Events, UIE) or planned events such as maintenance or repair. It is worth mentioning that the voltage should be controlled through power electronic converters (i.e. battery converters or PV converters) under islanded conditions [44, 45]. When the microgrid is connected to the grid through the two level VSC, the DC bus voltage is regulated. However, when the microgrid operates in an islanded mode (i.e. off-grid operation),

the loads should be met via smart DGs and battery systems in order to supply the power requirements to the loads and maintain system stability [44, 45]. Depending on the generations and load requirements, PV models deliver the power generation to the microgrid based on the Maximum Power Point Tracking (MPPT) algorithm. Otherwise, it stores the excess energy in the battery in the situation when the load demand is less than the total generation power. However, the storage energy sources supply the load requirements when the total power load is greater than the total power generation of the DGs. This is completely based on the State of Charge (SOC) and the current of the battery system [44, 45].

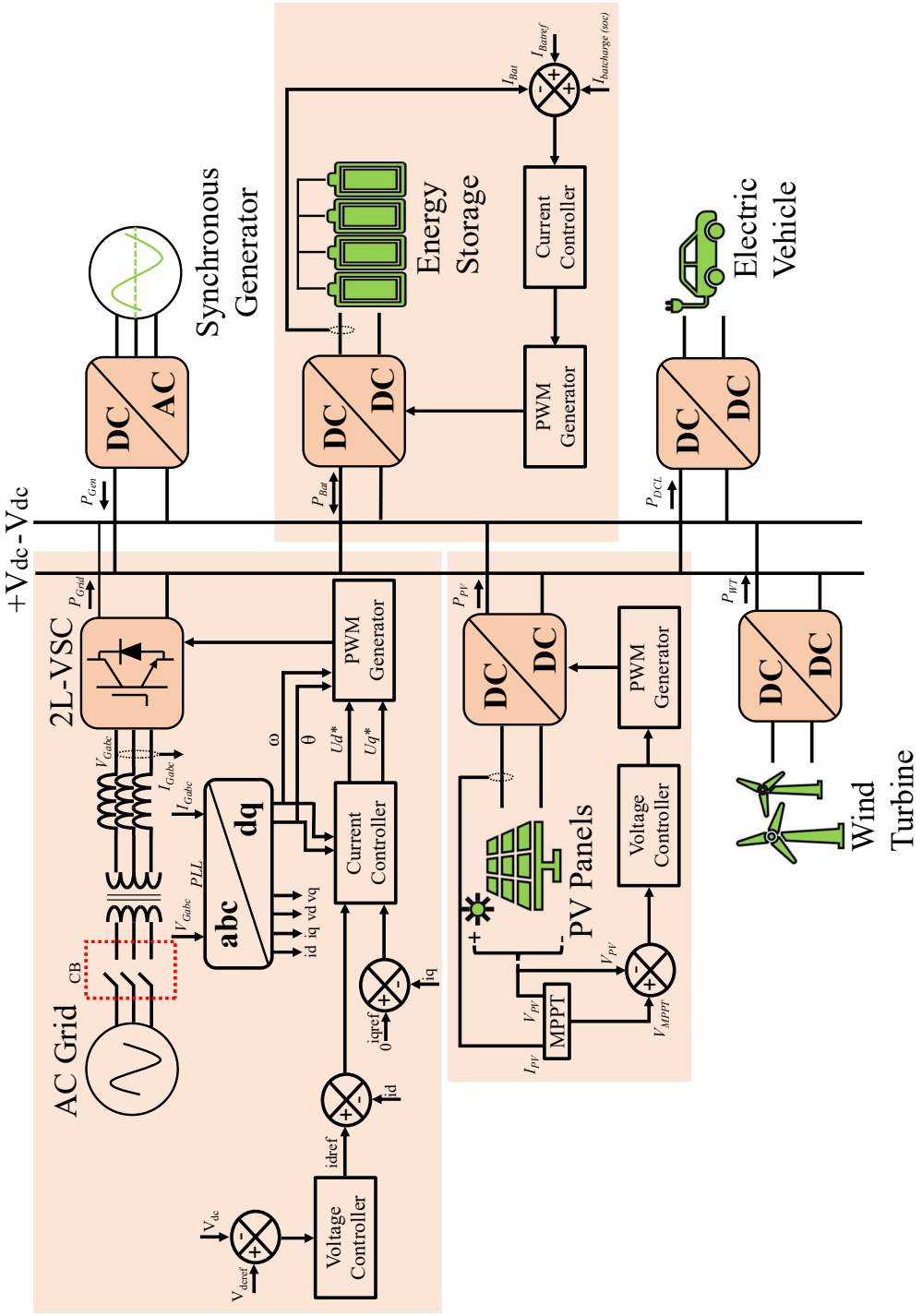

Figure 2.3: System architecture with a control mechanism for LVDC Microgrid

2.3.4 Development of an international standard and guidelines for LVDC

For LVDC technology to be widely available and safe, standardisation efforts are necessary. There are regional and international standardisation bodies established with the aim of developing guidelines and requirements for the implementation and safe operation of LVDC applications (e.g. data centres, marine systems, traction systems, and PV generations). This includes the International Electrotechnical Committee (IEC), Emerge Alliance,

Table 2.2: A summary of applicable standards for LVDC applications

Application	**Design**	**Protection criteria**	**Safety**	**Power quality**	**Earthing-Bonding**	**Switchgear-circuit breaker**
Microgrids	IEEE P2030.10	-	-	-	-	-
Ship power	IEC 60092-201	IEC 60092-202,IEC 60092-507	-	-	-	-
Public Networks	IEEE P2030.10.1,IEEE P2030.10.2	BS EN 60947-3	IEEE P2984, IEC 61439-2, IEC 61557	IEC TR 63282,IEC 61000-2-2	ESQCR	IEC 61439-1
Power Converter	IEC TS 62578, IEC 60146-1-1, IEC 60146-2	-	IEC 62477-1	IEC 61204-3	-	-
Residential	IEEE P2030.10.2	-	-	IEC 61000-4-17	-	IEC 61008-1
Telecom-ICT	ITU T Rec. L.12011	-	-	ITU T Rec. L.1200	-	-
Data Centre	-	-	IEC 62040-1	-	-	-
LED Lighting	-	-	IEC 60598-1, IEC 61347-1	-	-	-
Solar PV	-	IEC 60269-6	-	-	-	-

and Institute of Electrical and Electronic Engineering (IEEE). Table 2.2 summarises several relevant international standards and recommendations for existing LVDC applications. The purpose of the IEC SyC LVDC is established to provide system-level standardisation, coordination, and guidance in the areas of LVDC and LVDC for Electricity Access, whereas the Emerge Alliance facilitates the development of LVDC standards and promotes the use of DC systems. The IET has published a code of practise for low and extra-low voltage DC power distribution in buildings. This code of practice is intended to promote the safe, effective, and competent installation of cabling and wiring for LVDC power distribution in buildings. ETSI develops standards for data centres and telecommunications systems that operate at 48V DC and up to 400V DC. Additionally, the IEEE's Distribution Resources Integrated Working Group/remote LVDC Microgrids is currently developing standards for LVDC microgrids for rural and remote electricity access applications.

Although there are currently no international standards guiding the development of large-scale DC distribution systems such as islanded LVDC microgrids or hybrid AC/DC microgrids, there are opportunities to use knowledge gained from previous DC traction systems to aid in the establishment of future LVDC standards. While it is undeniable that stand-alone LVDC applications have well-developed standards, however public LVDC distribution networks are still found to be lacking in standards particularly those relating to voltage harmonics, earthing configurations, safety, and protection requirements [8].

The following subsection will present a number of LVDC solutions and pilot projects, emphasising the cost advantages and challenges associated with LVDC distribution.

2.3.5 Descriptions of LVDC solutions and pilot projects

There are a number of LVDC pilot projects being implemented in various countries, including United Kingdom, Finland, the Netherlands, South Korea, and China. This section presents a collection of pilot installations, technical solutions and commercial installations from around the world and briefly describes the characteristics and primary objectives of these LVDC pilot projects [46].

China

The AC/DC hybrid project is based in Tongli Suzhou Jiangsu, China, and is funded by one of China's 2017 national key research and development projects. The primary motivation behind the development of this system is as follows:

- To expand the capacity of the public power grid to capture additional renewable energy.

- To provide energy at a high efficiency level. This can be achieved through the integration of DC systems, resulting in a more efficient power grid.
- To conduct research in the area of advanced energy conversion technologies.

Tongli's AC/DC hybrid system is comprised of a power electronic transformer (PET), a fault current limiter (FCL), a DC solid state switch, a DC EV charging station, rooftop solar panels, a super capacitor, and energy storage system as illustrated in Figure 2.4. By the end of 2019, the project's total capacity had reached 4.38 MW, with all units operating normally. The system's generators and loads are supplied at four distinct voltage levels via a 750V LVDC microgrid, a 375V LVDC microgrid, a 220V DC nano grid (including a 48V DC bus), and two 380V AC microgrids. Meanwhile, two 3 MVA PETs, two 2.5 MVA VSCs, and one bidirectional DC/DC converter have been installed to ensure reliable electrical transition between these micro/nano grids. Each microgrid is connected to the public grid via at least one PET or VSC, allowing it to exchange electricity in both directions with the public grid. The Figure 2.4 illustrates the structure of the Suzhou Tongli AC/DC hybrid system.

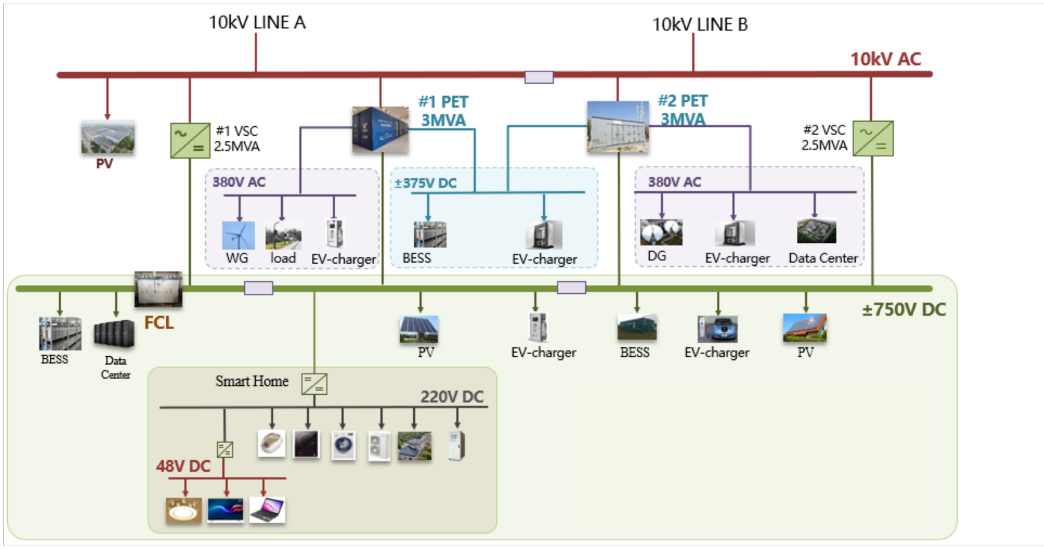

Figure 2.4: Suzhou Tongli LVDC site configuration in China [47]

The project incorporates several key operating technologies that demonstrate the advantages of LVDC microgrids as commercially feasible solutions, including technologies for multiple-port high-efficiency power electronic transformers. These transformers employ a combination of centralised high-capacity and distributed low-capacity technology to accommodate a variety of energy dispatch scenarios. The system's efficiency and reliability are enhanced by the coordination of these transformers. Additionally, a multi-boundary protection scheme based on the DC grid topology is developed to elimi-

nate the complex fault mechanism, short fault feature duration, and difficult fault location in DC distribution networks. Furthermore, this project established an impedance-based method for analysing and optimising low frequency oscillations. The output equivalent impedance is found to have noticeable peaks in the low frequency band, which can easily interfere with the load side's equivalent input impedance. Through parameter optimization, the stability margin of the multi-cascade system is increased, and oscillation on the 750V DC bus is successfully restrained. Finally, Tongli's system utilises single point direct earthing to address the issue of current corrosion. To effectively reduce the current flowing through the earth wire during unbalanced operation, the negative poles are connected to the earth via anti-parallel diodes, while the earth wire is earthed directly via a single point.

Germany

"DC-Industrie" is a German initiative comprised of a consortium of twenty-one industrial firms and four research institutes. It is based on two phases funded by the German Federal Government's Energy Research Program and focused on improving energy efficiency and flexibility in industrial production by establishing a DC-based smart grid for industry. The project's first phase concentrated on the demonstration, evaluation, and gaining operational experience with a basic configuration for several production cells, including robot cells for the automotive industry. Meanwhile, the second phase of the project focused on ensuring a secure and robust energy supply for manufacturing plants, simplifying project planning, and maximising the use of decentralised and regenerative energy production. The project's objective is to lay the foundation for the development of a manufacturer-independent LVDC system concept. The system consists of modules connected to the LVAC main grid via AC/DC rectifiers, variable speed motor drives, DC-supplied machines and robots, and passive DC loads aggregated into distinct load zones as illustrated in Figure 2.5. These modules are connected using connection boxes that contain equipment for load zone and cable protection through rapid hybrid and solid-state LVDC circuit breakers, pre-charging and disconnection, as well as photovoltaic plants and energy storage systems connected via a DC-bus (DC-backbone). The DC network is buffered with sufficient intermediate-circuit capacity to keep switching frequency-based clearing procedures away from devices operating in a semi-industrial environment. The industrial DC power supply incorporates an energy management system that balances the nominal DC voltage of 540 V DC for uncontrolled supply on a 400 V AC grid and 650 V DC for controlled and uncontrolled supply on a 480V grid within pre-defined bands such as nominal, steady-state, over/under voltage, and transient over/under voltage. According to the project's researchers, switching to

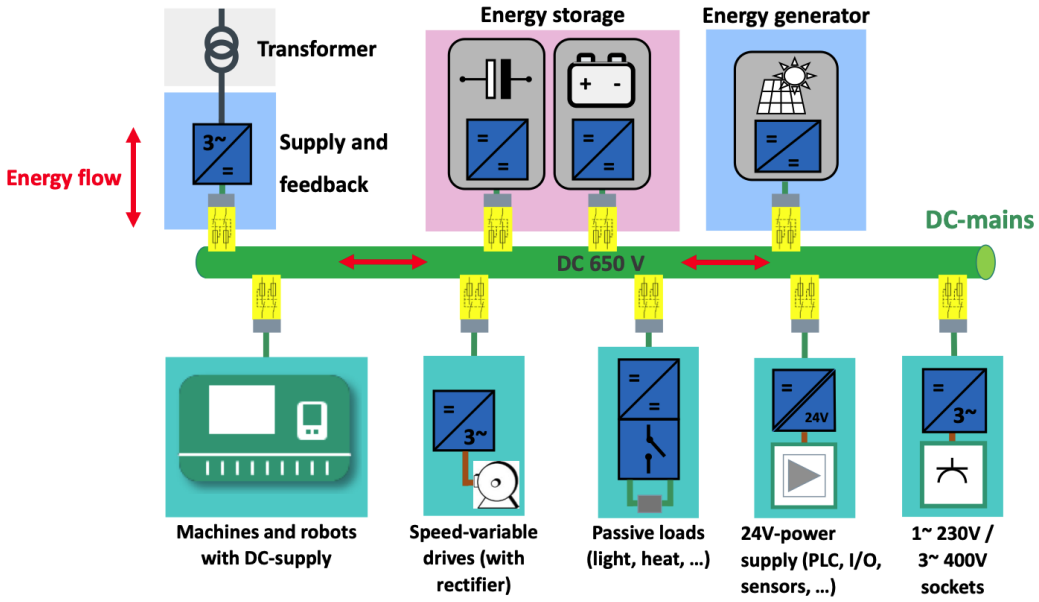

Figure 2.5: An industrial DC's topology-grid for the factory [48]

DC voltage for power supply results in enormous efficiency improvements and energy savings. The fundamental benefits of this project are the elimination of transformation and transportation losses (improved efficiency) and the reduction of equipment costs and space requirements associated with the elimination of power electronics. In terms of system stability, additional investments in power supply filtering and compensation can be avoided, while existing grids are maintained. Additionally, cost savings on energy purchases are feasible by implementing a smart DC grid infrastructure with intelligent energy flow control [49].

Netherlands

The provincial roadway N470 was a one-of-a-kind regional initiative, involving a large number of industry partners. South Holland aims to manage and maintain its highways, rivers, bridges, and locks in a carbon-neutral manner. These remarkable aims were met in the N470 project by constructing the most environmentally friendly road in the Netherlands. They demonstrated that this type of innovation is a viable business approach within the existing ecosystem. It is the region's first road to have been completely reconstructed carbon-neutral and to generate its own energy for lights and traffic signals. Additionally, the employment of DC technologies has resulted in increased traffic flow and road safety. The network is connected to the AC grid via two 100kW active front ends with the DC system is electrically isolated from the AC system. DC/DC converters are used to connect solar panels to the grid, as depicted in Figure

2.6. A 1MWh LiFePo4 battery system is comprised of 12 strings of LiFePo4 batteries coupled via DC/DC converters and protected by solid state circuit breakers. The 4.7-kilometer-long power distribution cable has a four-core cable rated at ±700 V DC with a +/-60V DC droop control. The network is earthed via a TN-S with multiple earthing configuration, with additional stray-current safety supplied by diodes that separate the metallic and electric earthing. A streetlight DC load is connected to a network of 23 x 350V strings with a +/-30V DC droop control coupled with DC/DC led drivers and power line control. The network is protected using hybrid and solid-state circuit breakers and is designed to protect against over-voltage and arc faults. The technological

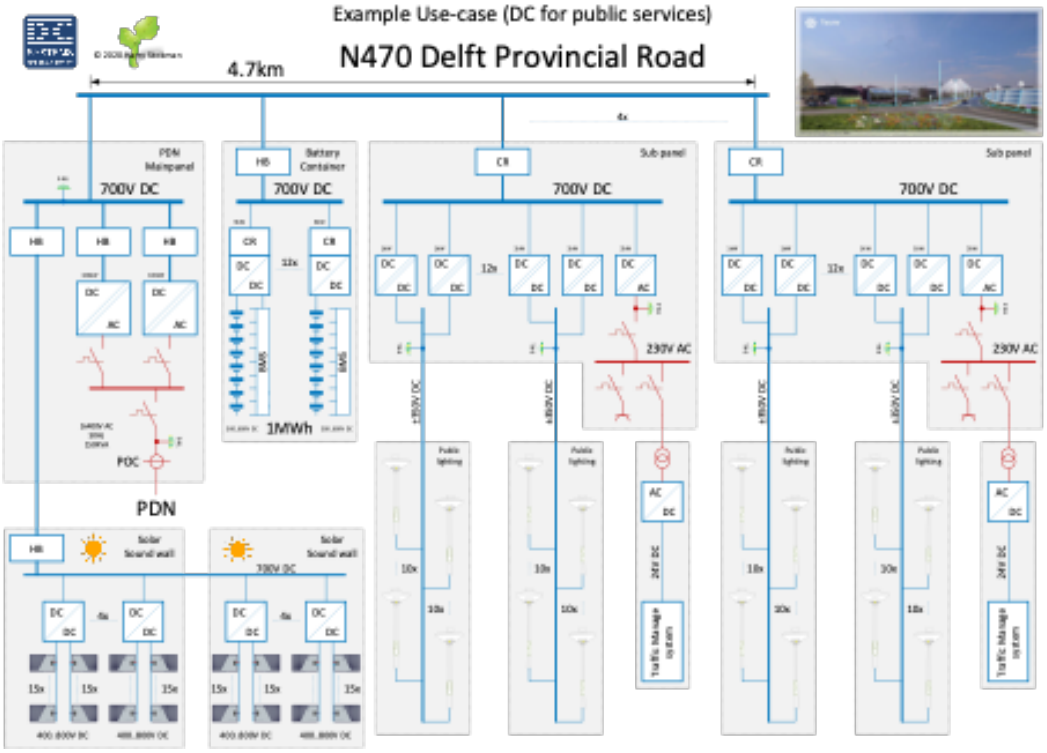

Figure 2.6: N470 site network [50]

advantages of implementing this commercial project include the following:

- The system is powered by a single 4.7-kilometer-long cable. The cable is powered by DC to overcome the challenges inherent in passing AC across a water channel.
- When the main grid is disrupted by an unanticipated occurrence, the system has the capability of running in islanded mode.
- The system is an autonomous LVDC microgrid that operates in conjunction with renewable energy sources (photovoltaic (PV) and energy storage) and regulated power flow, and it does not require digital communication.

- The system has energy management capabilities but does not require data or an internet connection, hence avoiding security hacking occurrences.

UK

SP Energy Networks, one of the UK's Distribution System Operators (DSOs), is conducting a trial of solid state transformers (SSTs) at 11 kV/0.4 kV substations to deliver hybrid AC/DC networks as depicted in Figure 2.7. The LVDC demonstration is one of the most innovative parts of the project, as it has never been trialled previously in the UK by any DSO. The project's objective is to validate the technology, but also to develop a standard solution for network operators' future deployment of LVDC networks. This application is being developed to enable the establishment of an LVDC network capable of powering ultra-rapid electric vehicle chargers. In this instance, a customer-owned 150 kW EV charger is supplied by SP Energy Networks through a 950 VDC (±475 V bipolar) supply. Consumers can anticipate immediate benefits from this project in the form of a significant reduction in the cost of the EV charging unit, a more efficient device (by 2%), and a smaller environmental footprint.

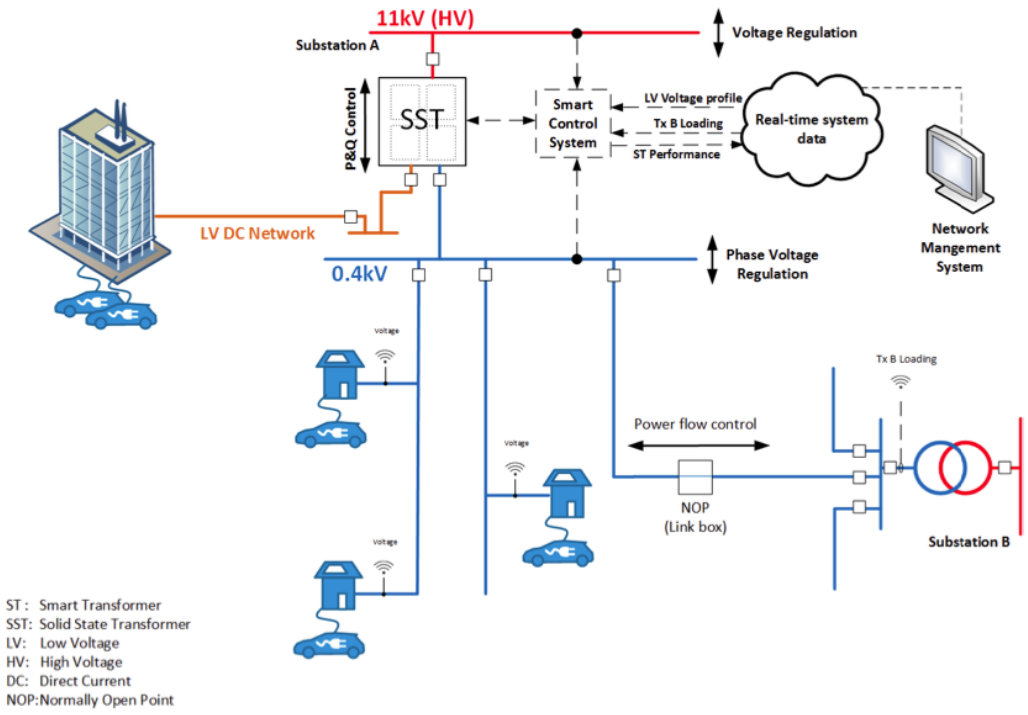

Figure 2.7: The fundamental concept underlying the LV Engine solution [51]

This LV Engine project has demonstrated a variety of functionalities, including the following:

- Voltage regulation on LV networks;

- Capacity sharing with other substations;
- Elimination of LV imbalance load detected by the 11 kV network;
- Compensation for reactive power and power factor correction in secondary substations;
- Deployment of LVDC for rapid and ultra-rapid charging of electric vehicles.

To this end, the following developments have been carried out in the project:

- Two cutting-edge SST topologies have been developed to implement the LV Engine's functionality. The SST is a three-stage conversion that utilises a high frequency transformer in the middle stage.
- The TN-S earthing system was considered to be the most appropriate earthing solution for this project. DNOs are obliged to provide solid earth on their low voltage network under the UK's Electricity, Supply, Quality, and Continuity Regulations (2002) (ESQCR). Additionally, TN-S earthing was chosen over TN-C or TT earthing to minimise the chance of stray DC currents in the protective earth;
- Rather of depending just on overcurrent protection, this project developed a protection technique that incorporates undervoltage shunt release in order to avoid the need for oversizing the DSO's source converter.

The aforementioned world-wide LVDC demonstrations are just a few examples of published pilot projects. There are still a number of other projects ongoing around the world, but with little publicly available information. These pilot projects are all focused on quantifying the advantages of the LVDC microgrid over the LVAC microgrid for both short and long term operations. However, as described in Section 2.3.4, public LVDC microgrids continue to lack standards in several areas, most notably when it comes to power quality regulation, earthing configurations and protection solutions. Various research initiatives and the IEC LVDC technology report emphasise the importance of defining a suitable earthing scheme and establishing reliable DC protection technologies capable of providing adequate protection while retaining a high level of safety, selectivity, and resilience. In general, the LVDC interface between the main grid and the LVDC microgrid distribution network has a significant impact on the design and performance of LVDC protection solutions. As a result, the following section will discuss the evolution of LVDC interfaces.

2.4 LVDC interface architectures, modelling, and operation

This section describes the architecture, modelling and operation of AC/DC and DC/DC converters commonly used in DC microgrids. There are several converters available in the literature. However, for the purpose of this study, the following converters have been considered.

2.4.1 Two-Level voltage source converter (VSC) converter

A two-level VSC is a grid-interfaced AC/DC converter with a voltage sourced DC bus and the current (direction and magnitude) can be changed to control the power flow. In order to filter out the high frequency harmonics resulting from the PWM modulation, L or LCL filters will be used as an interface between the grid and the converter. The two significant advantages of VSC over thyristor-based CSC converters are that it can provide sinusoidal currents with unity power factor and can be programmed to control the amplitude as well as the phase. Such a converter has a DC-link capacitor installed across the DC bus in order to produce constant DC voltage with minimum ripple. Although, a large DC capacitor improves the dynamic performance at the expense of bulkier design. The nested loop dq current control is the most mature and common control methodology utilized in VSC [52]. This nested dq control scheme, normally has two control loops. These are known as outer control and inner control loop are employed in the two-level VSC as shown in Figure 2.8. The outer loop controls the active, reactive power, or AC and DC voltages while the inner loop controls and regulates the dq currents and generates appropriate switching pulses for converters. A frame of reference transformation is utilized to transform the AC voltages and currents into dq quantities via Park's transformation. The control loops generate the correspondent dq current references (id and iq). These signals are then processed within the decoupled current controller and the voltage reference signals are generated with the aid of phased-locked loop (PLL) to dq and vice versa and then transformed into the abc frame. The PLL generates the angle reference (θ) from the voltage $Vabc$ at the point of common coupling (PCC) [52].

2.4.2 DC/DC Boost converter connected to PV

A PV array consists of many solar cells where each one is represented by a current source. The output current capacity depends on the cell temperature and on the sunlight exposure. In general, a solar cell can be designed and modelled as a current source with an anti-parallel diode as shown in Figure 2.9.

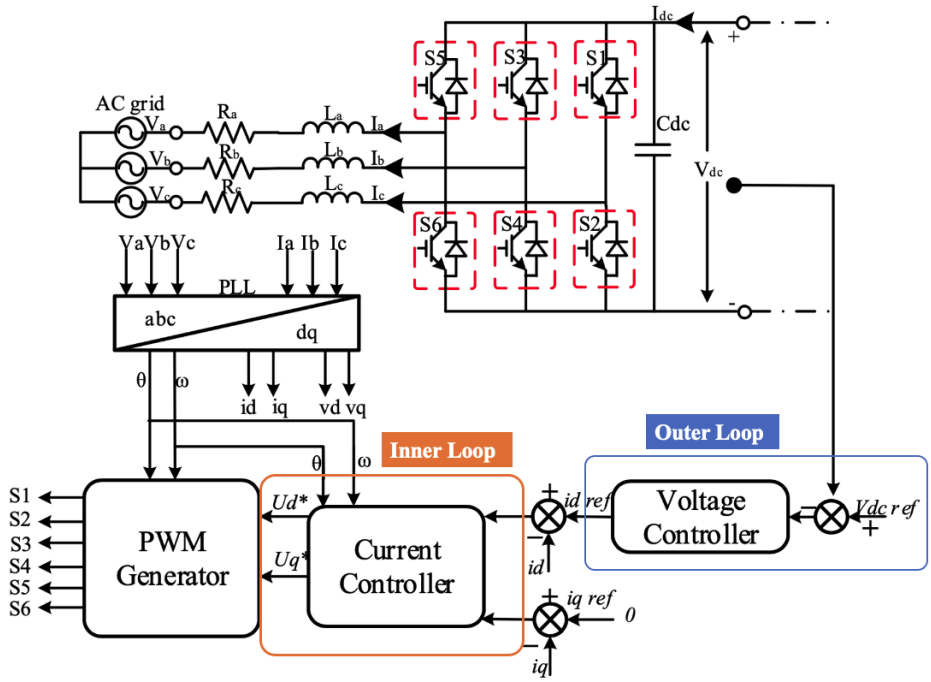

Figure 2.8: Diagram two-level voltage source converter with control loops.

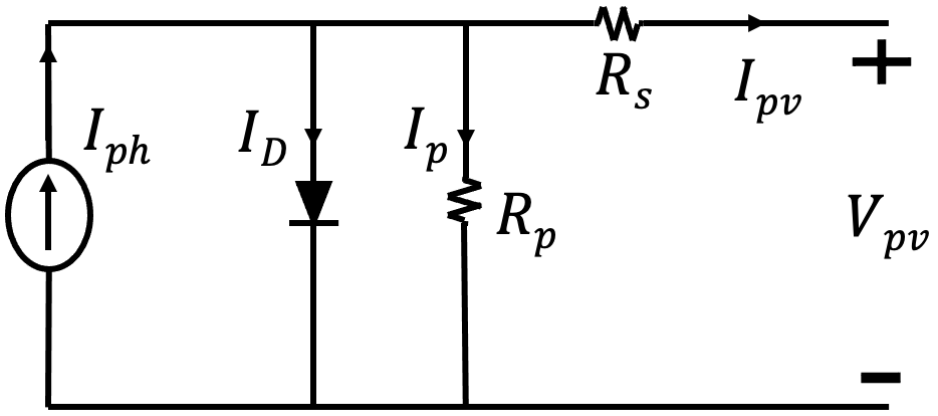

Figure 2.9: The circuit model of a PV panel.

A parallel resistor R_p represents the leakage current inside the cell, and a series resistor R_s represents the conducting losses.

$$I_{pv} = n_p I_{ph} - n_p I_{sat} \times \left[\exp\left(\frac{q}{AKT} \left(\frac{V_{pv}}{n_S} + I_{pv} R_s \right) \right) - 1 \right] \tag{2.1}$$

where I_{ph} is the photocurrent, V_{PV} is the terminal voltage of PV panel, I_{sat} is the saturation current, q is the electron charge, A is the ideality factor, k is the Boltzman constant, n_p is the number of parallel solar cells, n_s is the number of series solar

cells, and T is the junction temperature. The output power of a photovoltaic panel is determined by the I-V curve, as illustrated in Figure 2.10, where I_{sc} and V_{oc} represent the short circuit current and open-circuit voltage, respectively. The output power P_{PV} varies with the output current due to the nonlinear relationship between the output current and the terminal voltage described in Equation 2.1. At the terminal voltage V_{mp} and the output current I_{mp}, a Maximum Power Point (MPP) exists. As a result, a photovoltaic panel should be programmed to operate at the MPP.

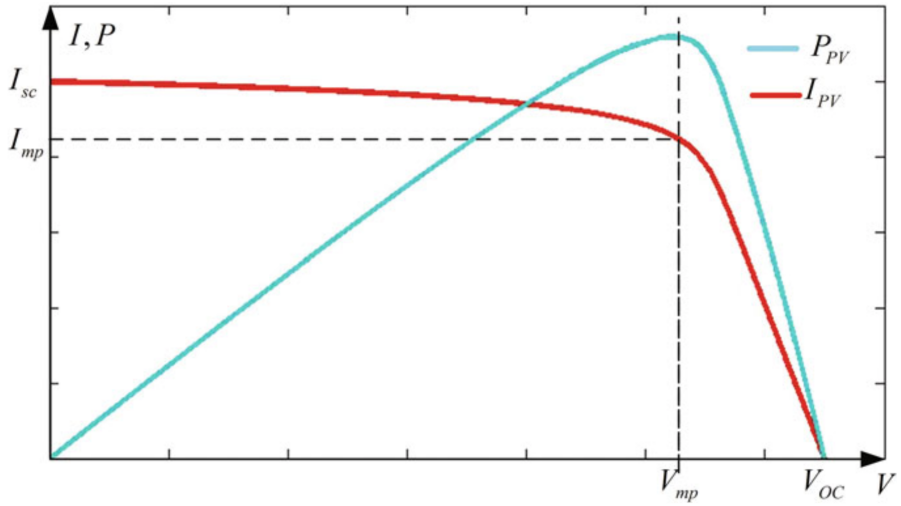

Figure 2.10: The I-V and P-V curves of a PV panel [53].

A PV array of 10 kW is modelled according to the equations in [54], and connected to a boost converter as shown in Figure 2.11, which uses a maximum power point tracking (MPPT) algorithm to extract maximum power from the PV. There are several MPPT algorithms available in the literature, including Perturbation & Observe (P&O), Incremental Conductance (IC), and fractional open-circuit voltage [55, 56, 57].

The actual terminal voltage V_{PV} is compared to the reference voltage V_{ref} in the outer voltage loop, and the error is processed by the proportional-integral (PI) controller to generate the reference current and then the duty cycle command for the DC/DC boost converter. These values are then passed to the PWM generator, which generates the necessary switching signal to generate the voltage that results in the maximum amount of power as dictated by the mppt [56].

2.4.3 DC/DC Buck-Boost converter connected to a Battery Energy Storage System (BESS)

Depending on the needs of the microgrid, the battery may operate under either charging or discharging conditions. These conditions depend on the state of charge (SOC) of the

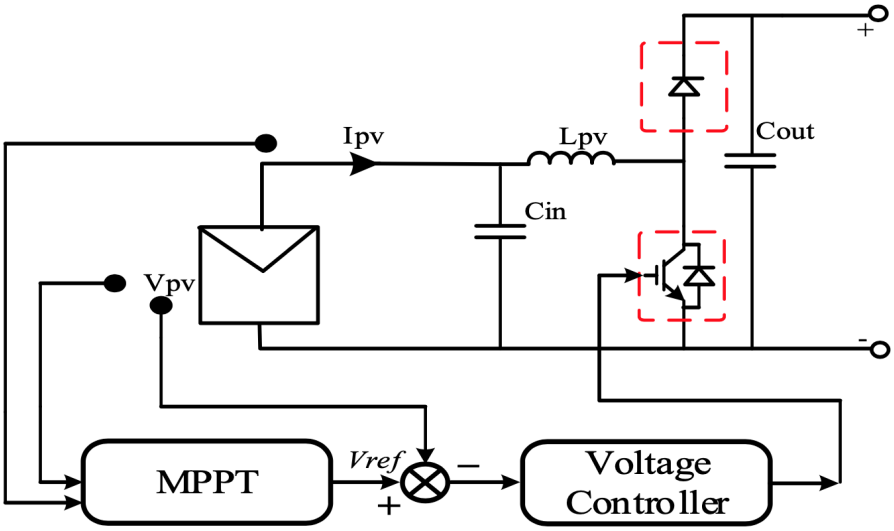

Figure 2.11: Diagram of PV with MPPT based DC/DC Boost converter.

battery and the active power requirement of the microgrid. The battery system does not participate in the system frequency control. Although being the best source of DC voltage, a battery cannot work when the SOC is lower than a threshold and the depth of discharge (DOD) may affect its life-time [58, 59]. Therefore, an adequate battery model with control strategies should be developed.

A battery energy storage system is connected to the bidirectional DC/DC buck-boost converter as shown in Figure 2.12. When discharging, it functions as a boost converter; when charging, it functions as a buck converter. Voltage regulation and power control modes are selectable on the battery converter [60]. This control structure enables operation in both grid-connected and islanded configurations. In particular, when connected to the grid, the DC/DC bidirectional converter regulates the output power based on predefined setpoints or acts as a current limiter. In contrast, when the battery is in islanding mode, it acts as a DC voltage forming unit, regulating the output voltage to its nominal value. Alternatively, the voltage-active power droop curve can be used to determine the battery's output voltage [61]

2.5 DC fault characteristics

Generally, regardless of the LVDC microgrid architecture, a DC fault can occur in either the DC bus or in the DC cables. Due to its intended simplicity, a LVDC microgrid acts as a single point of energy interface between the distributed generators (DGs) and the load. The drawback is that a fault on either the DC bus or cable will have an effect on both the DGs and the battery. Therefore, a single fault anywhere within this system can have consequences.

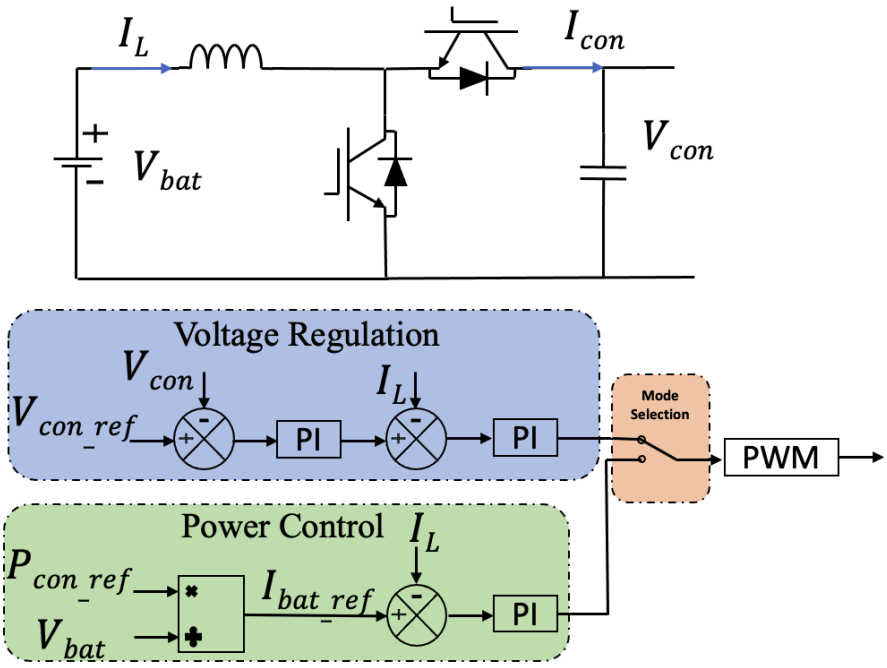

Figure 2.12: A bidirectional battery converter's circuit and control block diagram [53].

2.5.1 Two-Level VSC DC fault characteristics

An AC-DC converter is an essential device for interfacing AC and DC sections of the modern microgrid. It is widely used to integrate various types of energy resources and can be implemented with a variety of topologies. Typically, LVDC applications employ a two-level VSC structure. On the DC side, the VSC converter is equipped with a short-term energy storage component (C) whose primary function is to maintain a constant DC-side voltage. Additionally, an inductance (L_{ac}) is connected in series with the AC terminals to ensure that the AC-side currents remain sufficiently constant during the short time interval between switching. A fault here causes the capacitor to discharge at such a high current amplitude that it can lead to damage of the VSC components. Therefore, the protection strategy should have a fault current ride-through capability in order to manage the excessive peak fault current to prevent damage to both the system and its components. With the aim of analysing the DC fault characteristics of the VSC, a non-linear system is utilised and can be characterised by three stages, as depicted in Figure 2.13.

Stage 1- Capacitor Discharge (Natural response)

In this stage, the capacitor starts discharging through the cable impedance as a result of a fault, as illustrated by the example of the traces of three stages of a two-level VSC

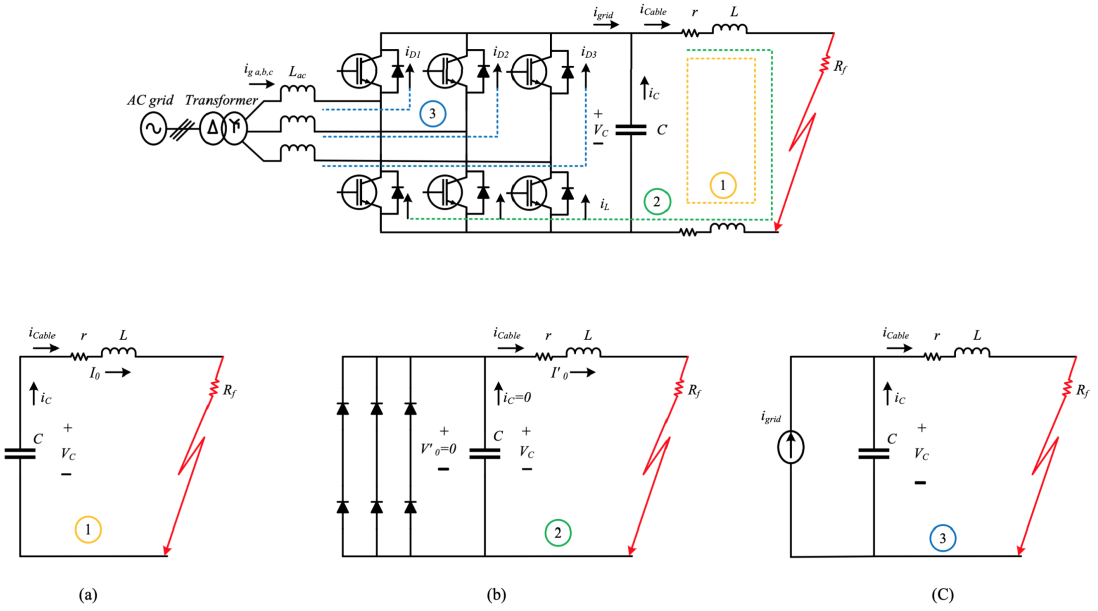

Figure 2.13: Equivalent circuit for two-level VSC under a short-circuit fault, (a) Stage1-Capacitor discharge, (b) Stage2-Diodes freewheeling, (c) Stage3-Grid-side current feeding [62]

during a pole-to-pole fault in Figure 2.14. The resulting peak value of fault current could go up to 100 times the VSC rated current as it depends on the internal resistance of the DC filter capacitor, capacitor value and cable inductance. An equivalent of the RLC circuit is formed and its response in the Laplace domain can be written as [63, 64, 65]:

$$I(s) = \frac{v_{c_0}/L + sI_0}{s^2 + R/Ls + 1/LC} \quad R = (r + R_f) \tag{2.2}$$

where I_0 and v_{c_0} are initial the current through inductor and voltage across the capacitor, respectively. r and L are the resistance and inductance of the cable from the converter to the fault point, R_f is fault resistance and R is the sum of r and R_f. The fault current I_t can be expressed in the time domain as:

$$I_t = \frac{v_{c_0}}{L(s_1 - s_2)}\left[e^{-s_1 t} - e^{-s_2 t}\right] + \frac{I_0}{s_1 - s_2}\left[-s_1 e^{-s_1 t} - s_2 e^{-s_2 t}\right] \tag{2.3}$$

where s_1 and s_2 are the roots of the characteristic equation of 2.3, and are equal to,

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega^2} \tag{2.4}$$

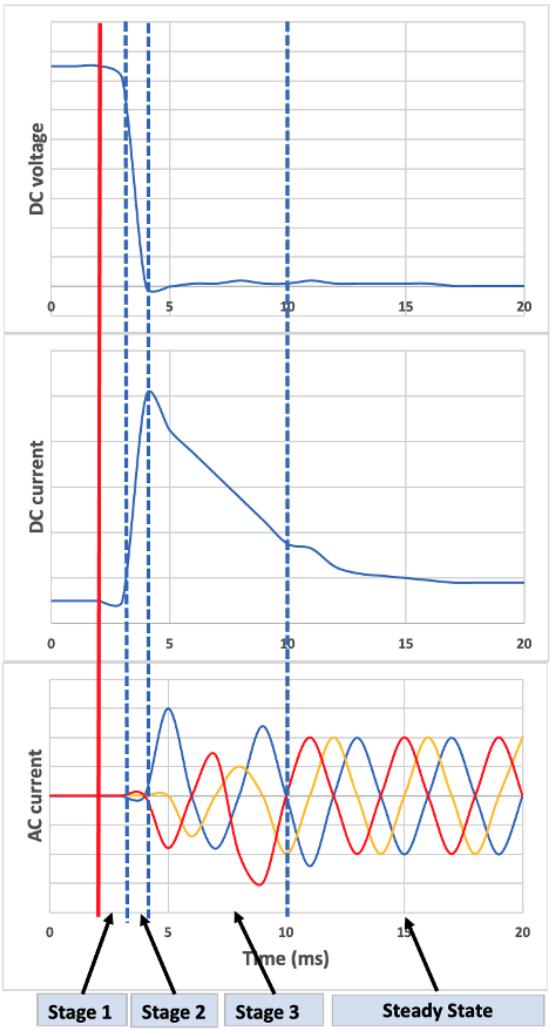

Figure 2.14: Two-Level VSC DC fault characteristics during pole-to-pole fault

where α and ω are respectively the damping factor and the resonance frequency and are defined as:

$$\alpha = \frac{R}{2L} \tag{2.5}$$

$$\omega = \frac{1}{\sqrt{LC}} \tag{2.6}$$

The current response is determined based on the magnitudes of α^2 and ω^2, where $\alpha^2 > \omega^2$ (over-damped), $\alpha^2 = \omega^2$ (critically) and $\alpha^2 < \omega^2$ (under-damped). For example, the current response is obtained as follows for an under-damped system:

$$I_t = \frac{v_{c_0}}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) + I_0 e^{-\alpha t} \left[\cos(\omega_d t) - \frac{\alpha}{\omega_d} \sin(\omega_d t) \right] \tag{2.7}$$

where $\omega_d = \sqrt{\omega^2 - \alpha^2}$

Stage 2- Diode Freewheeling

In this stage, the capacitor will be discharging through the cable until its voltage reaches near zero. In this case, the cable current commutates to the VSC freewheeling diodes (refer to Figure 2.13 (b)). The cable current and current of each leg of the freewheeling diode can be expressed as:

$$i_{cable} = I_0' e^{-(R/L)t}, i_{D_1} = i_{cable}/3 \tag{2.8}$$

This stage can be very damaging to the diodes of the converter because when the capacitor voltage reaches near zero, the initial cable current I_0' may be almost ten times the nominal current value. Thus, it is highly desirable to detect and isolate the fault during the first stage (capacitor discharge) before entering the second stage.

Stage 3- Grid-side Current Feeding Stage (Forced response)

At this stage, the IGBTs are turned off for self-protection purposes, and the VSC converter acts as an uncontrolled full-bridge rectifier and contributes to the fault current through the freewheeling diodes [62]. The fault current in this stage is calculated as:

$$i_{grid} = i_{D_1} + i_{D_2} + i_{D_3} = i_{g_a} + i_{g_b} + i_{g_c} \tag{2.9}$$

where i_{g_a}, i_{g_b} and i_{g_c} are respectively positive value of the phase a, b, and c currents passing through the freewheeling diodes.

For phase a, the $i_{g_a} > 0$ is calculated as [62]:

$$i_{g_a} = I_g \sin(\omega_s t + \alpha - \theta) + [I_{g_{|0|}} \sin(\alpha - \theta_0) - I_g \sin(\alpha - \theta)] e^{-t/\tau} \tag{2.10}$$

where $\theta = \arctan\left[\frac{\omega_s(L_{ac}+L)}{R}\right]$, $\tau = \frac{L_{ac}+L}{R}$, I_{g_0}, and θ_0 are the initial grid current amplitude and phase angle respectively, L_{ac} is the grid-side inductance.

In most cases, a DC microgrid is connected to a large number of distributed energy sources and AC/DC loads. As illustrated in Figure 2.14, the DC voltage drops precipitously in two milliseconds during the fault, necessitating a fast protection approach to detect the fault. As a result, the DC protection approach should exploit the transient

characteristics of the capacitor to identify faults as quickly as possible, which means that the protection should act between stages 1 and 2 when the capacitor discharges.

2.5.2 DC/DC Converter fault characteristics

Like the VSC, the DC/DC converter can be subjected to failures as a consequence of faults happening in the DC system. When a fault occurs, the resulting current can increase the nominal steady-state current (up to 15 times) due to the capacitor discharge through un-controlled paths (diode). When the fault current flows through the diode, it forces its commutation to on-state. At this point, in order to protect the semiconductor components of the DC converter (IGBT) due to the low short circuit withstand of these components , an external protective system (i.e. DC circuit breaker or fast acting fuse) has to be placed in the conducting ports of the inter-connected converters [65]. The most traditional non-isolated topologies of a DC/DC converter in an LVDC microgrid are the Buck and Boost converters.

DC/DC Boost converter

Similar to VSC, this converter presents three stages during short-circuit fault conditions which are the capacitor discharge stage, diode freewheeling stage, and input source feeding stage as depicted in Figure 2.15. When a fault occurs, the short-circuit current will increase gradually until system failure occurs. Therefore, it is important to implement a protective scheme that has the ability to drive down the fault current from the input source within several microseconds [65].

DC/DC Buck converter

The non-linear performance of the fault current in the Buck DC/DC converter is defined by two stages (refer to Figure 2.16). Under faulty conditions, the transient fault current behaviour is different in the Buck DC/DC converter compared with the Boost DC/DC converter because the freewheeling current is restricted to the inductor current. This is due to the inductor current (iL) in the Buck converter not being able to change instantaneously under faulty conditions. If the inductance is relatively large, the fault current will be limited and the pulse voltage will be attenuated. Therefore, current limiting methods in Buck converters must either be able to deal with long fault recovery times or be able to include a dissipative element in the freewheeling path in order to drive down the fault current quickly when a fault occurs [66].

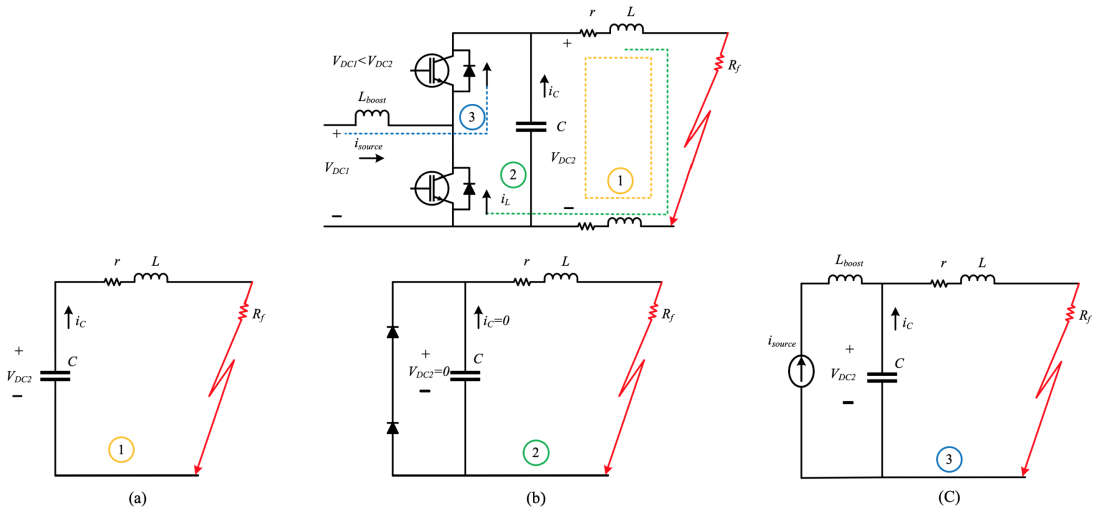

Figure 2.15: The three stages of the DC/DC boost converter under short-circuit fault conditions. (a) Capacitor discharge stage , (b) Diode freewheeling stage and (c) Input source feeding stage [65].

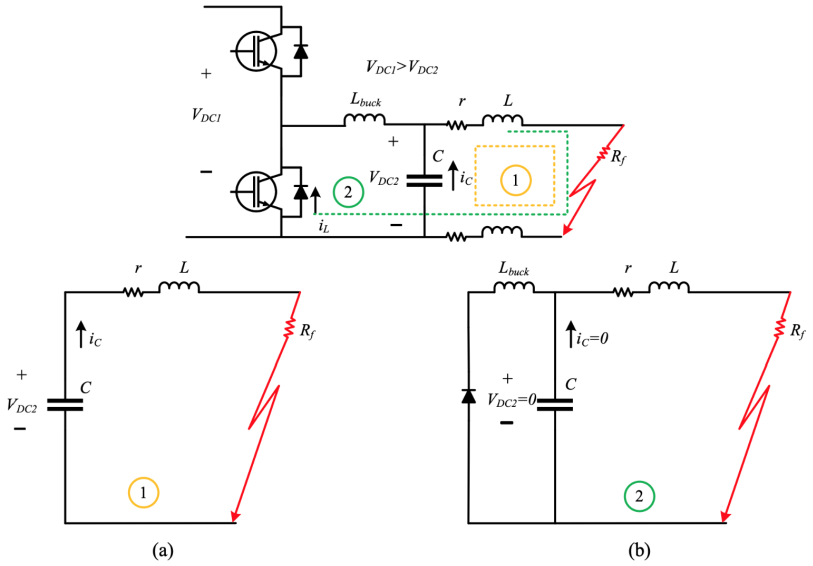

Figure 2.16: The two stages of the DC/DC Buck converter under short-circuit faulty conditions: (a) Capacitor discharge and (b) Diode freewheeling [65].

2.5.3 Fault location in LVDC microgrids

Apart from detecting the fault, it is essential to ascertain the location of the fault in the system in order to facilitate rapid post-fault maintenance such as cable replacement and network reconfigurations to be performed [65]. The natural zero-crossing events

produced by the AC voltage/current allow solid earth faults in AC systems to be cleared relatively easily. However, this is not the case in DC systems [65]. Considering that in DC systems do not have zero-crossing points for voltage and current, there has been a considerable interest in DC protective devices and strategies that are capable of interrupting a non-zero current [67, 68]. Most topologies connected to the AC grid install circuit breakers on the AC side that rapidly extinguish a current while placing slower switches on the DC side to properly segment the system [69] and ensure the safety of individuals in buildings. The power router, a form of the triple active bridge (TAB) is proposed in [70, 71] as an alternative method of segmenting a grid based on a topology that can limit current on its own. These novel techniques for interrupting and rerouting current have enabled the development of architectures with multiple paths that provide higher reliability, mostly through redundancy [42, 72]. Radial architectures present the lowest redundancy in the system, which means if any one line in the system downtimes, that entire section of the system loses power. Ring architectures create a secondary path for current, ensuring that the load will not lose power even if a single point of failure occurs [73, 74]. The addition of redundancy can be seen when architecture is interconnected [75]. However, by adding multiple current paths, it becomes more difficult to identify the faulty line [69] and its location within that segment, which makes it more difficult to repair the line in a timely manner.

In particular, fault location techniques can be classified into two categories: online methods and off-line methods. The majority of existing techniques for fault location are primarily based on off-line methods [76, 77]. These methods typically involve injecting current or voltage signals into the main circuit and detecting the electrical response to the injected signals to determine the location of the fault. Undeniably, the off-line method requires additional operating time and manual intervention. Online methods are proposed to reduce the level of human invention and to accelerate postfault maintenance. This subsection compares and contrasts various off-line and online methods, as well as the accuracy of the various developed techniques.

Off-line Fault Location Methods

Active Distance Estimation Technique: The distance protection scheme operates on the basis of estimating the distance between the protective device and the fault by measuring the short circuit reactance at determined frequencies. This method is widely used to protect AC systems; however, the extremely small series cable inductance in DC systems poses a small barrier to their use in DC systems. Additionally, the fundamental frequency term is no longer a predetermined default value for identifying the transient impedances of a DC system [78]. Active distance estimation methods for

DC microgrid protection have been proposed in [76, 79], based on the similar concept of distance protection in AC systems. A power injecting unit (also known as a probe power unit) is used in these methods to inject low-power current or voltage signals with a predetermined frequency spectrum into the faulty loop. The signals' voltage/current responses are sampled and analysed in order to determine the fault distance and thus locate the fault. Active distance relays are typically implemented with a low-power electronics converter serving as the probe unit that generates the desired signals. Additionally, the injection unit can be composed of a large capacitor connected to a source via a controllable switch, resulting in a second-order RLC circuit between the probe unit and the fault path [76]. Signal Processing Techniques: such as the Fast Fourier Transform (FFT) and least square curve fitting are used to extract information about the fault impedance from post-fault data acquisition over a predetermined time period. The distance between the relay and the fault point is estimated using the mathematical relationship between the fault location and the fault impedance [80, 81]. The sensitivity in estimating the location of faults is highly dependent on the mathematical relationship established. As a result, it is vital to consider carefully all of the system's variables and dynamics during a fault transient. While this is sufficient for a simple DC system, when a more complicated circuit is on the far end, a single probe unit cannot clearly indicate the remote fault location. To locate the fault in a reasonably complex system topology, it is recommended that the DC system be divided into distinct zones, each with its own probe. Despite the fact that active distance protection provides adequate data about the system's state. The requirement for each node to have a probing arrangement with signal injection and a high bandwidth measuring unit increases the cost of the protection system. The phenomenon of multiple probes with a more sophisticated DC system topology can significantly increase the complexity of such a scheme.

Online Fault Location Methods

Derivative Based Technique: To facilitate fault location, online methods are proposed that utilise voltage, current, and di/dt values measured locally during a transient stage in a radial DC distribution system [82, 83]. These techniques are based on the development of a linear relationship between di/dt and the impedance of the fault loop. The fault inductance between the protective device and the fault point is estimated using these measured values. The time required for fault detection and location estimation is theoretically assumed to be less than 0.65 ms with an error of less than 20% in order to accurately build up the linearized relationship between di/dt and the fault location. It is essential to establish an appropriate transient model in order to min-

imise the error associated with fault location. This inaccuracy is exacerbated by the converters' non-linearity in fault conditions, which complicates the system's evaluation. The time required to locate a fault, the error associated with distance estimation, and the inaccuracies inherent in DC microgrid modelling make this technique difficult to implement in multi-terminal DC microgrids with a variety of converter topologies [84]. Noise Pattern Analysis-Based Technique: Identifying an earth fault in an unearthed system is a significant challenge in DC microgrids. This is because fault current is minimal in such faulty conditions. The majority of fault locators are incapable of locating pole-to-earth faults in an unearthed system. To tackle this issue, a technique for locating pole-to-earth faults based on Multi-Resolution Analysis (MRA) and wavelet analysis has been proposed in [85, 86]. MRA is a technique for extracting significant features from higher-resolution signals [87]. The wavelet analysis technique is being used to recognise inherent high frequency noise patterns by analysing electrical noises over time. Assuming that these distinct patterns are initiated by parasitic inductances and capacitances interacting with the switching patterns of power electronic devices, the information about earth faults can be obtained from the noise signals' analysed feature. This method is completely self-contained and does not require any additional signal generation equipment, voltage or current measurement equipment, or inter-device communication. Nonetheless, the technique is suggested to be effective in the following circumstances:

- The system is unearthed or has an extremely high impedance.
- Forms a circuit loop through earth using parasitic circuit elements.
- The characteristics of the fault signal should be highly related to the location of the fault, and the noise signal should be easily measurable [86].

For a DC microgrid with a relatively sophisticated configuration, such as one with multiple terminals, a variety of converter types, and variable switching frequencies, the previous conditions may become rather demanding to actually fulfil. Voltage Resonance-Based Technique: After a short-circuit fault, the discharge of terminal capacitors causes voltage and current resonance in a VSC-based DC system [85, 88]. In fault transient conditions, these resonances can form an RLC resonance circuit by passing through the VSC-link capacitor, the cable resistance, the cable inductance, and the fault resistance. A voltage resonance-based fault location scheme can be formed by defining a relationship between the cable parameters (i.e. cable inductance and resistance) during the circuit's resonance behaviour [88]. When this method is used, two distinct relationships are formed under solid and resistance fault conditions. Then, using Prony's technique, the transient circuit based on the RLC circuit is solved. The results of the impedance

measurements are then used to calculate the estimated location of the fault. Although the method does not rely on communication links to estimate fault locations, its accuracy is still dependent on the linearized RLC modelling and its consistency with the data acquisition. Transient Peak Current Based Technique: Considering the fact that peak current and steady-state fault current are closely related to the fault impedance, they are recognised for online fault location as well. The total inductance in the loop can be determined by developing linear relationships between the dc side resistance, inductance, and transient peak current over a continuous period of post-fault oscillations [89]. As a disadvantage, using a steady-state current profile necessitates semiconductor devices to withstand a higher amount of let-through energy (i^2t) for a longer period of time, which requires the semiconductor and/or fault current limiting devices to have sufficiently large ratings to survive those most severe faults.

In summary accurately locating a fault while minimising network downtime continues to be a challenge. As numerous researchers have developed offline techniques for fault location, each of them necessitates the use of a distinct signal injection unit (probe unit). These signal injection units add additional costs and delays to the network's restoration. In contrast, online methods for locating faults rely on accurate circuit modelling of the system, which takes into account the system's dynamic behaviour in the event of a fault. As a result, current online techniques are not mature enough for practical application. As a summary, Table 2.3 compares all developed fault locating methods on the basis of their operation metrics, approximate estimated time for fault location, fault type that can be located, and maximum distance estimation error.

2.5.4 Fault detection and protection methods in LVDC microgrids

As described in Section 2.4, the LVDC microgrid network employs a variety of converter technologies, which results in a variety of fault characteristics. The majority of the LVDC microgrid projects are interfaced with the main grid through two-level voltage source converters, which poses challenges for LVDC protection solutions. This is because the dc fault current can penetrate the circuit very rapidly as a result of the dc-link capacitor being discharged. One of the most important functions of an LVDC protection method is to detect and isolate faults in a timely and accurate manner. There are two types of faults that can occur in a DC network: pole-to-pole and pole-to-earth faults. Pole-to-pole faults exhibit low impedance fault characteristics, whereas pole-to-earth faults exhibit both low and high impedance fault characteristics [90]. Detecting a pole-to-earth fault with high impedance is challenging, due to the fact that the fault current is unlikely to trip the overcurrent protection, and is therefore more likely to be

Table 2.3: Comparative Analysis of Various Fault Location Techniques for LVDC Applications

Fault location scheme	**Operation metrics**	**Approximate estimated time**	**Fault type**	**Maximum estimation error**
Active distance estimation technique	Offline	20 ms	Pole-to-pole fault	7-8%
Derivative technique	Online	0.65-0.75 ms	Pole-to-pole/pole-to earth faults	2-20%
Noise pattern technique	Online	-	Pole-to earth fault in unearthed systems	-
Voltage resonance technique	Online	1.5 ms	Pole-to-pole fault	2%
Transient peak current technique	Online	1.7 ms	Pole-to-pole fault	15%

confused with load step-up events [91, 92]. Additionally, because converter-based DG sources operating in islanded mode contribute only a small amount of fault current, the development of a fault current detection and protection scheme that is capable of detecting DC fault currents of small magnitudes is required [93].

Existing fault detection and protection methods can be classified into two categories as described in the literature (unit and non-unit protections), each with its own set of benefits and drawbacks that will be discussed in detail in Chapter 6. Given the challenges associated with detecting high impedance faults and small fault current magnitudes in islanded mode, this thesis developed a protection scheme based on the sign of the current of the second derivative that prevents HIF faults from going unnoticed and putting equipment and infrastructure at risk of damage, while also protecting the network during islanded mode and no need of communication link. Chapter 6 discusses the technique in detail.

2.5.5 Systems earthing for LVDC microgrids

Earthing is a complicated subject that entails a number of design considerations and trade-offs [45–47]. An effective earthing scheme should be able to [26,45], maximise personal safety (i.e. reduce the touch voltage), minimise stray current (i.e. reduce the leakage current to the soil), facilitate the detection of earth faults, and minimise

common-mode noise between AC and DC [94, 95]. IEC 60364-1 standard classifies earthing configurations for LVDC microgrids as TT, TN-S, TN-C, TN-C-S, and IT as shown in Figures 2.17, 2.18 and 2.19 respectively. In Chapter 4 will discuss in extensive detail the earthing configurations and methods used in the LVDC microgrid.

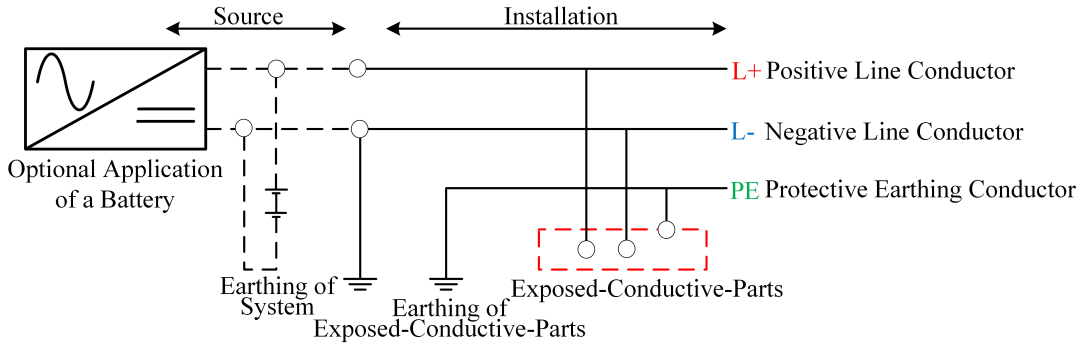

Figure 2.17: TT earthing scheme [96].

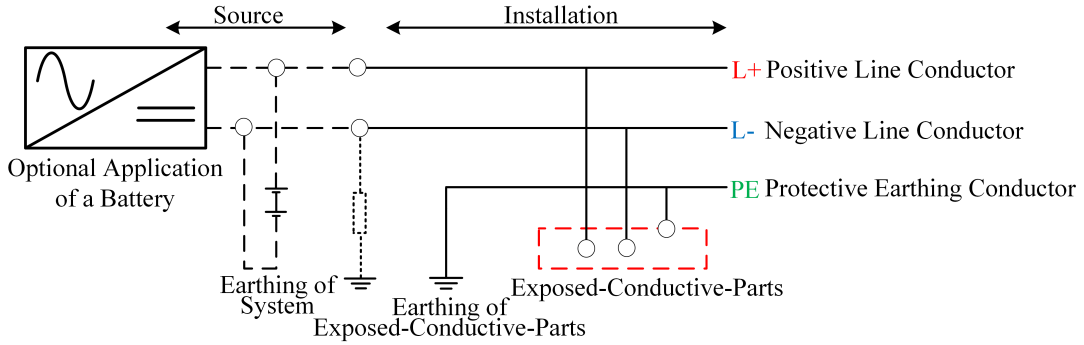

Figure 2.18: IT earthing scheme [96].

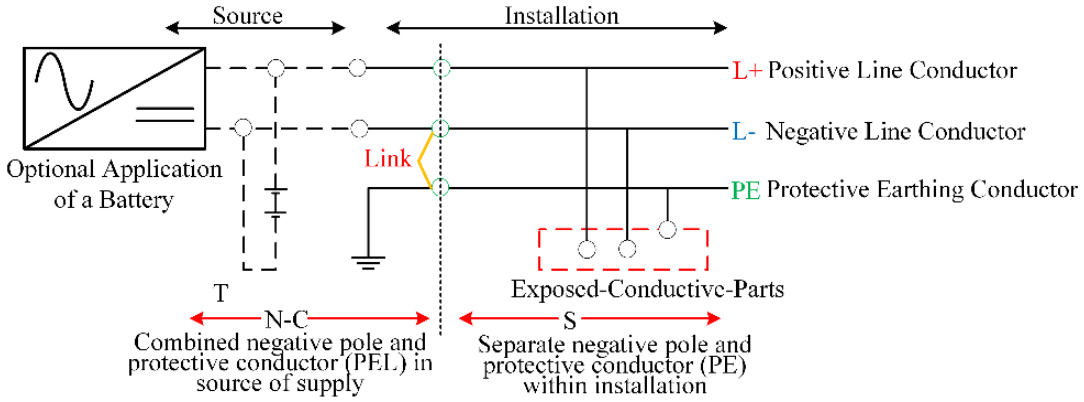

Figure 2.19: TN earthing scheme [96].

2.6 Islanding detection methods for LVDC microgrids

As previously explained in section 2.3.3, LVDC microgrids can be operated either connected or islanded from the main grid. Islanding detection (ID), which is the process of determining when the converter has been disconnected, is a critical feature of any converter designed to operate in a LVDC microgrid and continues to be a challenging task [97]. The islanding detection method enables the DC system to disconnect immediately upon the occurrence of an islanding event or to switch to a controller configured for this operating mode. By selecting an appropriate controller for both grid-connected and islanded operation, the DC system can be made to operate safely and efficiently. An unintentional islanded event (UIE) in a LVDC microgrid can impose a serious risk to both human life and equipment [98]. An UIE event occurs when a section of the distribution system becomes electrically isolated from the main grid and continues to be energised by its own generators [99]. According to the standards BS EN 62116 [100], IEEE 929-2000 [101], IEEE 1547.1-2005 [102] and IEC 62116-2008 [103] an islanded event should be detected within 2 seconds in order to avoid system damage [99]. An islanded event can be easily detected when there is a big variation between the power generated and consumed. However, and according to IEEE Standards 929-2000 [101], the most challenging islanded event condition to detect is when this variation is near zero, therefore, an anti-islanded algorithm is necessary to detect such events.

Once an islanding event is detected, several actions are possible. In many applications, it is mandatory for converters to disconnect from the grid immediately upon detection of an islanding event, typically within a short time period (100-300 ms) [104]. Other applications require the system to continue operating during an islanding event to ensure service to the load is maintained [105, 106, 107]. It is essential when designing the converter controller that it has the capability of switching smoothly between different operation modes. This can be accomplished using advanced techniques or simple PI techniques [97], depending on the application. Conventionally, bidirectional AC-DC converters regulate the DC distribution voltage. When the converter is disconnected from the utility, the system goes into islanded mode [98]. In this case, the system is either shut down or regulated by another component (i.e. storage interface). In a conventional AC system, current, voltage and frequency are the variables that can be measured and used to detect an islanding scenario. Conversely, in a DC system, current and voltage are the only variables under such a situation, and thus, they are the focus of anti-islanding algorithm development [108, 109].

The islanding detection methods in AC systems are generally classified into remote, passive and active. In LVDC microgrid, only active and passive methods have been reported in the literature [98, 109, 110] and will be explored in the next section. Ac-

tive methods attempt to detect islanding events by injecting small perturbations (e.g. current perturbations of a known frequency) into the system [98]. These lead to signal changes (e.g. current imbalance) which can be detected and compared against a pre-set threshold value and, consequently used to extrapolate an islanding event [108]. Passive methods attempt to monitor transient changes in voltage and current at the Point of Common Coupling (PCC) and compared with a pre-set threshold value. As with active methods, if this threshold is crossed, an islanding event can be detected.

Several methods for detecting islanding events in DC systems have been reported in the literature, using both active and passive methods, and these will be discussed in greater detail in the following subsections.

Active detection methods

Active methods are based on detecting disturbances in the voltage and current signals when deliberate perturbances are injected. This is based on the fact that when a microgrid is grid-connected, any injected disturbance will be absorbed by the system and it will not impose any instability. However, if the system is islanded, this disturbance will cause system instability, allowing the recognition of an islanding event [109]. The most commonly used methods for LVDC microgrids are positive feedback [111], insertion of a controllable load methods [112]. Active methods can potentially provide a cheaper approach compared to the passive methods for islanding detection and can significantly reduce the NDZ [113]. This is due to feedback control techniques that detect changes in the parameters such as the voltage or current at the DG [108, 109]. However, the continuous perturbations in the system can potentially lead to degradation of power quality. Additionally, the need for, in some cases, system controllers can increase system complexity and perhaps cost [114, 115].

Passive detection methods

In DC systems, these methods rely on continuously monitoring the local measurement parameters, such as voltage and current, without injecting any disturbance into the system [116]. Therefore, not impacting negatively on the power quality of the electrical power system. When an UIE occurs, these parameters will fluctuate (e.g. over/under voltage) and the protection devices will initiate a control command (e.g. disconnect or change to islanding mode). In the literature, only two passive methods have been reported and tested in LVDC: frequency and voltage deviation at PCC [117] and DC voltage control [116]. The first method monitors the deviation of frequency at PCC on the AC side and the voltage fluctuation at the DC-link point [117]. The second method bases itself on the variation of the magnitude of the DC-link voltage when the

voltage at PCC changes as a result of an UIE [116]. The performance of these methods deteriorates if such mismatches are zero or nearly zero, as a large Non-Detection Zone (NDZ) is created [116, 118]. However, passive methods are quite simple and can be very effective when there is a significant power mismatch between generation and demand, prior to islanding [119]. Also, the power quality is not affected and it does not require an additional controller system, rendering this system inexpensive in comparison to active methods [113]. Although several techniques are capable of detecting islanding events, few islanding detection methods are capable of discriminating between islanding and non-islanding events (faults and changes in the load). Two passive anti-islanding detection methods in LVDC microgrids have been assessed. These were the Rate of Change of Voltage (ROCOV) and the Rate of Change of Current (ROCOC).

2.6.1 Implementation of a passive anti-islanding method in a LVDC microgrid (ROCOV and ROCOC)

In this subsection, two passive anti-islanding methods are proposed. These methods have been previously implemented in LVAC microgrids, but their feasibility is assessed in LVDC microgrids in this thesis. The two methods monitor the DC voltage and current magnitude, and their Rate of Change of Voltage (ROCOV) and the Rate of Change of Current (ROCOC) are calculated and analysed. The ROCOV and ROCOC equation can be written as follows.

$$ROCOV = \frac{v(t_k) - v(t_k - \Delta t)}{\Delta t} \tag{2.11}$$

$$ROCOC = \frac{i(t_k) - i(t_k - \Delta t)}{\Delta t} \tag{2.12}$$

where, $v(t_k)$ and $i(t_k)$ is the measured value of voltage and current at the time of k^{th} sample and Δt is the simulation time step.

The ROCOV and ROCOC detection methods monitor the real power mismatch between the local load and generation. The real power during islanding results in a large deviation and the magnitude of the ROCOV and ROCOC has a significant value. When the magnitude of the ROCOV and ROCOC exceed the threshold, islanding is detected. Due to a continuous power mismatch between the PCC and the load, there is a dynamic change in the voltage and the current. This dynamic behaviour of ROCOV and ROCOC can be expressed in [120]:

$$ROCOV = \frac{V}{2P_L} * \frac{\Delta P}{\Delta t} \tag{2.13}$$

$$ROCOC = \frac{I}{2P_L} * \frac{\Delta P}{\Delta t} \tag{2.14}$$

where ΔP is the active power imbalance, V and I is the terminal voltage and current respectively and P_L is the active power of the DC load. From the above equation (2.13) and (2.14) respectively, it can be shown that during islanded mode the ROCOV and ROCOC are directly proportional to ΔP.

2.6.2 Islanding detection methods challenges

The proposed passive methods discussed in this chapter were developed with the aim of detecting an islanded event and distinguishing between DC fault (non-islanding) and Loss of Main (LOM) islanding scenarios in a network comprising of a battery and a photovoltaic module connected to a common DC bus through the use of local measurements at the PCC(refer to Figure 2.3). Following that, the obtained measurements were processed and expressed as ROCOV and ROCOC values. In the case where voltage and current measurements are captured at the DC-DC converter side of the battery, after t=0.075s, the ROCOV values at the battery buck-boost converter begin to gradually diverge in the presence of LOM and DC fault. This, however, does not distinguish sufficiently between the two scenarios (refer to Figures 2.20(a) and 2.20(b)). While the ROCOC value is expected to be high in the LOM scenario, this is because the battery is discharging current to enable DC-link voltage regulation, as described in [98]. As can be seen from the simulation results (refer to Figure 2.20), there is a significant difference in the ROCOC values for the two different load step changes scenarios. This is due to the battery's current flow being in a different direction(discharging and charging current). The ROCOC value, however, was similar between t=0.05 and 0.075s in both the LOM and DC fault scenarios (refer to Figure 2.20(d)). This may impair the method's ability to distinguish between LOM and other disturbances (e.g., a DC fault) in the presence of a small power mismatch.

In the case where the voltage and current signals are captured at the DC-DC converter side of the PV. The ROCOV value was comparable to that of the battery-connected DC-DC converter. This is because the battery and PV are both connected via a common DC bus, in this case at 750V (refer to Figure 2.21(b)). The highest ROCOC value is obtained in the DC pole-to-pole with a high resistive fault scenario, which reaches close to +15 A/s, as illustrated in Figure 2.21 (d). This is because the PV's DC-DC boost converter is incapable of limiting the fault current. To this end, the simulation results clearly indicate that both proposed passive methods are capable of detecting an islanding event; however, discriminating between DC fault with high fault resistance and LOM scenarios using only the ROCOV and ROCOC methods is challenging.

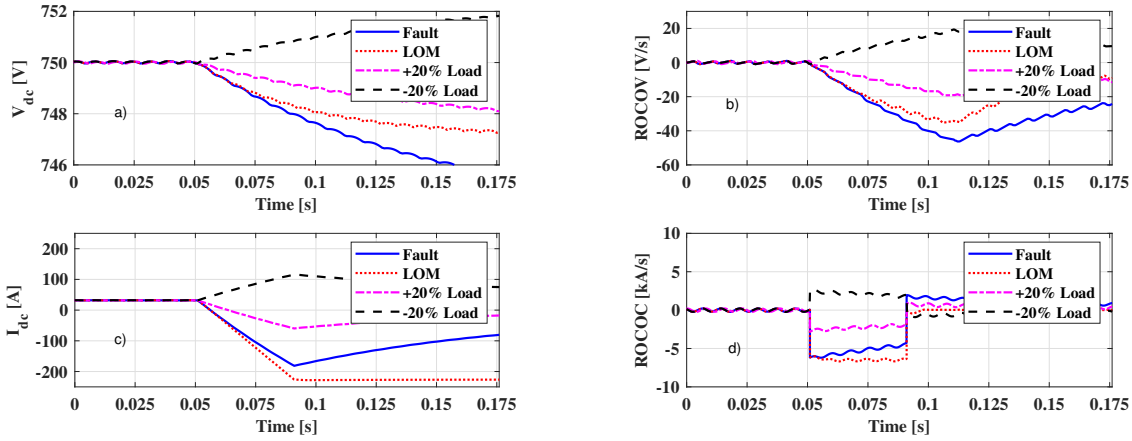

Figure 2.20: The system response to four scenarios (measurements taken at the battery terminal) a) V_{dc}, b) $ROCOV$, c) I_{dc}, d) $ROCOC$.

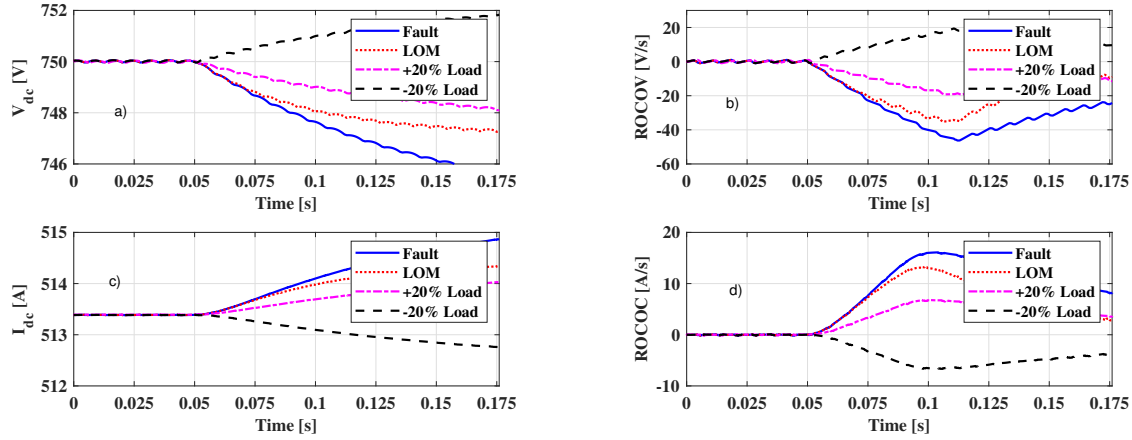

Figure 2.21: The system response to four scenarios (measurements taken at the PV terminal) : a) V_{dc}, b) $ROCOV$, c) I_{dc}, d) $ROCOC$.

In summary, The ROCOV and ROCOC were calculated using voltage and current signals captured at the battery and photovoltaic terminals, respectively. The proposed techniques are limited to situations in which a single designated converter is used to maintain voltage stability during an islanding condition. When multiple converters perform this function, interference from other source converters within the same grid can be a challenge; additional research is needed to address this challenge. The proposed methods are evaluated under a variety of conditions, including load step changes, DC pole-to-pole faults, and LOM events. The ROCOV and ROCOC-based islanding detection methods are capable of detecting islanding event, however, discriminating between DC faults with high fault resistance and LOM scenarios is challenging using these proposed methods.

2.7 DC measurement transducers implementation

The following section discusses briefly the DC measurement transducers available for measuring current and voltage accurately.

Hall Effect Sensor

The Hall effect sensor is a very common type of DC measurement transducer. Loop Hall effect sensors are classified into two topologies : open loops and closed loops. The open loop sensor is the most straightforward use of the hall effect sensor, as illustrated in Figure 2.22. An open-loop Hall-effect sensor makes use of a magnetic transducer to generate a voltage that is proportionate to the current being measured by the sensor. Amplification of this signal is then performed in order to provide an analogue output signal that is proportionate to the amount of current flowing through the conductor. For field concentration, the conductor is routed through the centre of a ferromagnetic core, with the magnetic transducer being mounted in the gap of the core. The disadvantage of an open-loop sensor is that any nonlinearity or drift in the Hall-effect current sensor IC's sensitivity in relation to temperature can result in inaccuracy [121].

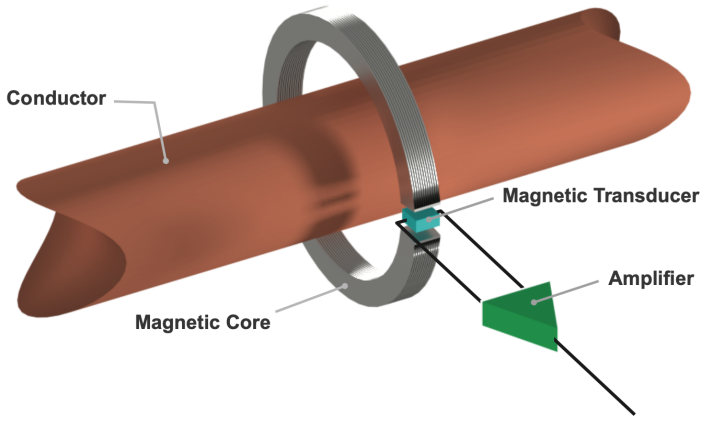

Figure 2.22: Open-Loop Topology[121]

A closed-loop sensor employs a coil that is actively controlled by the current sensor IC to generate an opposing magnetic field to that produced by the conductor's current. Following that, the Hall sensor detects a magnetic field of zero strength at the transducer. The output is formed by a resistor with a voltage proportional to the current driven into the coil and also proportional to the current flowing in the primary conductor multiplied by the number of turns of the coil wound around the magnetic core as

illustrated in Figure 2.23. Closed-loop current sensors require not only ferromagnetic cores, but also a coil and extra high-power amplifiers to drive the coil in order to function properly. While closed-loop current sensors are more complicated to implement than open-loop current sensors, they eliminate the sensitivity error associated with the Hall sensor IC since the system is operated at a single point at zero field, as opposed to open-loop current sensors[121].

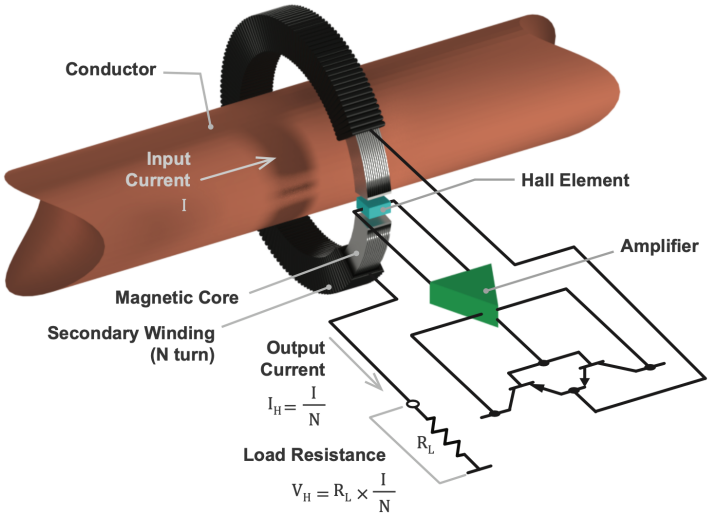

Figure 2.23: Closed-Loop Topology[121]

Fluxgate current sensor

Fluxgate current sensors are magnetic field sensors that detect both AC and DC currents at low frequencies. Fluxgate operates on a non-linear relationship between the permeability of ferromagnetic materials and the ambient magnetic field. A fluxgate sensor in its simplest form is composed of a ferromagnetic rod-shaped core, an excitation coil, and a pick-up coil as depicted in Figure 2.24. The excitation winding is used to push the core to saturation in both directions with the high-frequency excitation signal. At the point of saturation, the magnetic permeability of the core decreases significantly, resulting in the collapse of the ambient magnetic flux. The shift in magnetic flux causes a voltage in the pick-up coil that is proportional to the ambient magnetic field. Although fluxgates are one of the most precise magnetic sensors available (up to 0.0002 %), their applicability is limited due to their complexity and the high cost of commercially available products [122, 123, 124].

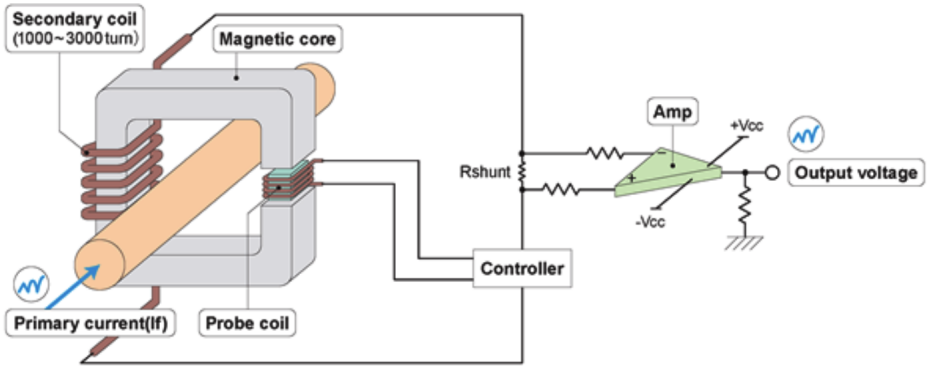

Figure 2.24: Open-Loop Topology[125]

Magnetoresistive sensor

The use of magnetoresistive (MR) sensors is widespread, with a variety of applications being supported. In general, the MR-effect describes the change in electrical resistance caused by the presence of an external magnetic field using one of three physical phenomena: the anisotropic magnetoresistance effect (AMR), the giant magnetoresistance effect (GMR), or the tunnel magnetoresistance effect (TMR) as depicted in Figure 2.25 [126]. MR sensors are not only utilised for measuring magnetic fields and linear motion, but they are also utilised for non-contact switching applications and, more importantly, for highly dynamic current measurement.

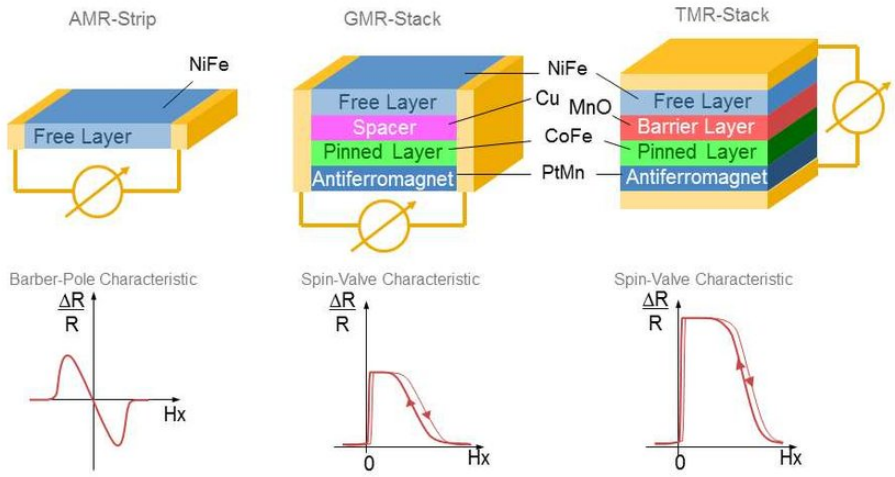

Figure 2.25: A comparison of Magnetoresistive (MR) technologies[126]

The anisotropic magnetoresistance effect in metals characterises how the resistance of the material varies according to the orientation of the current and magnetic field, with the resistance being lowest when the current and magnetic field are perpendicular to one

another. In the presence of a non-magnetic conductor between two ferromagnetic layers, the giant magnetoresistance effect causes a significant increase in resistance between the layers. When the magnetic fields in the two layers are parallel, the resistance decreases, whereas when the magnetic fields are anti-parallel, the resistance increases. The disadvantage of these two approaches is that the resistance changes are relatively small, necessitating the use of a Wheatstone bridge and signal amplifier for detection. The resistors are arranged in such a way that they resemble a differential field sensor. This method minimises temperature drift and eliminates interference fields. To this end, magnetoresistance sensors have very low hysteresis and highly accurate linear measurement accuracy. They have an extremely wide bandwidth and are capable of detecting magnetic fields at frequencies of up to MHz [124].

2.8 Protection devices

This section briefly describes the operating principles along with their advantages and disadvantages. Overall, there are three protection devices (PDs) commonly used in DC systems. These are fuses, mechanical DC circuit breakers (MCBs), and solid-state DC circuit breakers (SSCBs).

Fuses

The fuse is composed of a metallic conductor with two contacts and a box or cartridge to house the element. Depending on the voltage level, the cartridge is typically equipped with an arc extinction device made of quartz sand [127, 128]. Fuses are typically made of copper or silver and are used to protect the system by being connected in series with the power line. The fuse operates on the principle of the electric current's heating effect. When current flows through a conductor with a specified resistance, the resistance loss dissipates as heat. Under normal operating conditions, the fuse element's heat is smoothly dissipated into the surrounding environment by the current flowing through it. When a fault occurs, such as a short circuit, the fusible element's current flow exceeds the specified limits. This generates excessive heat, which melts the fuse and effectively breaks the circuit [129]. Fuses are classified as either fast-acting or time-delay fuses [130]. While time-delay fuses are preferred for applications involving higher inrush and surge currents, fast-acting fuses are suitable for use in series with converters to protect them. Although fuses are the simplest and most cost-effective method of protection in DC systems [131] and are recommended for protecting batteries, photovoltaic systems, and load-feeders that work in conjunction with mechanical switches and relays [132], they have several disadvantages: they must be replaced after operation and selecting

a suitable fuse rating and coordinating with other protection devices can be difficult [133]. Additionally, if a fault occurs in a single line, fuses isolate only the faulted pole, leaving the remaining pole operational.

Mechanical Circuit Breaker

MCBs are similar to normal mechanical switches. The operating mechanisms of MCBs are classified into pneumatic, hydraulic, spring, and magnetic. Generally, spring and magnetic operating mechanisms are commonly used in vacuum CBs, however the magnetic one is more attractive as it has fewer moving parts and has higher reliability [65]. The mechanical switch contacts are separated and an electric arc is created between the contacts when the fault occurs. These mechanical switches are applicable in the AC microgrid due to the existence of a natural zero-crossing current. However, in the LVDC microgrid, with the absence of the zero-crossing current, employing the mechanical switches will be limited to numerous DC applications. Therefore, passive and active resonance circuits have been proposed to overcome this issue [134] as illustrated in Figures 2.26 and 2.27. The mechanical circuit breakers consist mainly of three parts, the mechanical switch, the commutation circuit and the energy absorber circuit (i.e. Metal Oxide Varistors, MOV). Figure 2.26 shows the passive resonance circuit which has a capacitor and an inductor connected in series, and the capacitor has not been pre-charged. During normal operation, the mechanical switch will conduct the

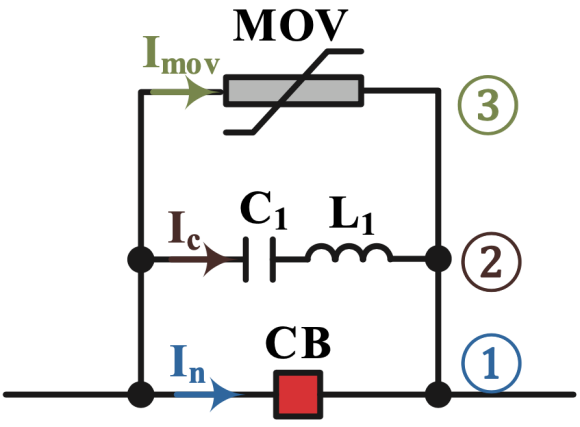

Figure 2.26: MCB with a passive commutation circuit[65]

load current with a low amount of loss as the resistance of the mechanical switch is around ten $\mu\Omega$ [135]. Once the fault occurs, the mechanical switch opens and an arc is generated between the contacts. The arcing voltage is established and the current is commuted from the load current path to the commutation circuit path. Then the commutation circuit (capacitor and inductor in series) generates a current oscillation.

Conversely, Figure 2.27 shows the active commutation circuit that consists of a capacitor, an inductor, and a thyristor switch. The difference between the passive and the

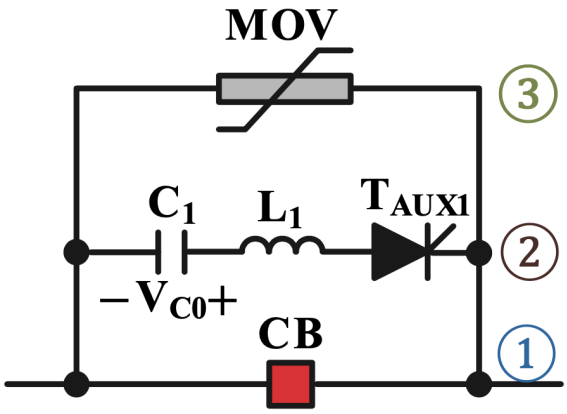

Figure 2.27: MCB with a active commutation circuit[65]

active commutation circuit is that the active circuit, the charged capacitor injects a negative current equal to the fault current to generate an instant zero-crossing current. This interrupts the current by a mechanical switch. The main advantages of the MCB are having low power losses and being cost-effective. However, their limited current interruption capability and slow response time are the main drawbacks.

Solid-state Circuit Breaker

SSCBs act as a current interruption by turning off power electronics devices. Solid state circuit breakers replace the conventional electro-mechanical switch with a semiconductor based switch to address the problem of slow time response. The usage of solid state devices allows current interruption within microseconds. A generic SSCB, as shown in Figure 2.28 [136], has key components such as a power semiconductor device, a gate driver, a cooling system (to ensure high efficiency of the SSCB during the conducting condition), a voltage clamping circuit, a fault sensing system, a sense and trip electronics, and an auxiliary power supply. Many Silicon (Si)-based semiconductor switching devices including Gate-off Thyristor (GTO), Integrated Gate-Commutated Thyristor (IGCT), Silicon Insulated-gate Bipolar Transistor (IGBT), and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), have been used for power electronics application [60]. GTO, IGCT, ETO, IGBT and MOSFET switches, are fully controllable. This means that they can be turned ON/OFF easily by control signal. The thyristor switches have the lowest conduction losses, hence this allows for a reduction in overall life-cycle costs and decreases the investment on the cooling system. However, not being able to actively turn OFF the current and having a long switching response,

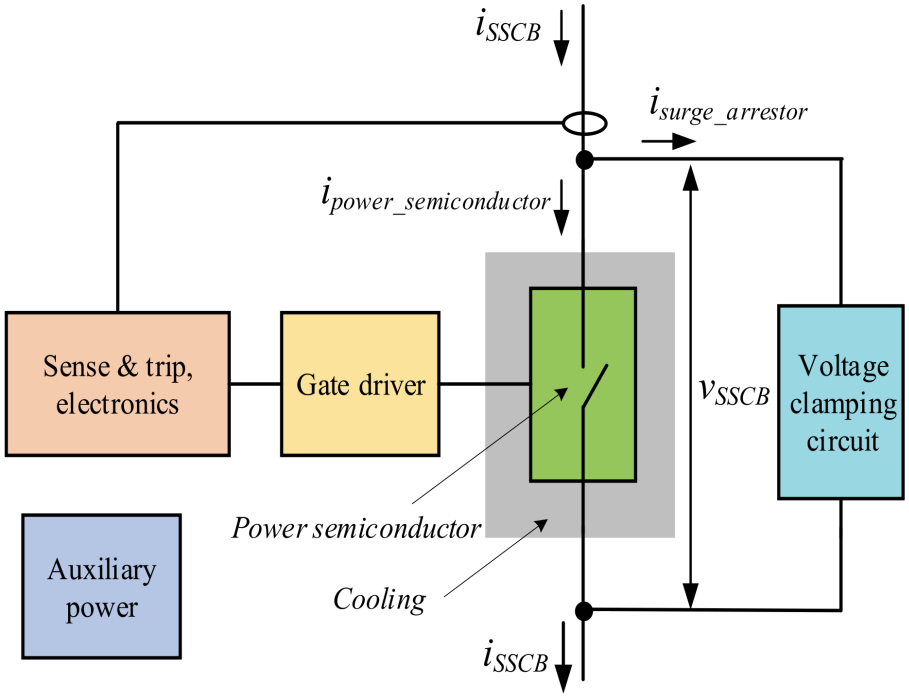

Figure 2.28: Key components of SSCB[136]

leads to high fault currents [65]. When a fault occurs, the sense and trip electronics switch OFF the power semiconductor through a gate driver. When the semiconductor is switched OFF, the residual energy in the system inductance develops a voltage across the power semiconductor. When this voltage reaches a pre-set value, the voltage clamping circuit is activated and the voltage is clamped. Once the voltage clamping circuit absorbs all the residual energy, the current is steered to zero. Both the power semiconductor and the voltage clamping circuit are in a high impedance state, and the voltage across the CB settles on the system voltage [136]. Although the solid state circuit breaker offers faster operation, this system has the disadvantage of having higher conduction losses and a large sized cooling system due to the presence of heatsinks or coldplates [65, 137, 138]. Additionally, the advantages and disadvantages of the different DC protection devices are summarised in Table 2.4.

2.9 Remaining technical and economic challenges for LVDC microgrids deployment

Many LVDC microgrids are still in the conceptual or prototype stages, and only a small number of practical examples have been implemented to date. There are still some technical and economic hurdles to overcome before LVDC microgrids can be

Table 2.4: Comparison of different DC protection devices for LVDC microgrid

Type of protective devices	**Advantages**	**Disadvantages**
Fuses	• Low cost • Low power losses • Low contact resistance	• Difficulty in selecting a suitable fuse rating and coordinating with other protection devices. • A fuse must be replaced for proper operation.
Mechanical Circuit Breakers	• Very low power losses • Very Low contact resistance • Low cost PDs	• Limited current interruption capability • Slow time response 10-30 ms
Solid State Circuit Breakers	• Fast response in ranges of tens of microseconds	• High conduction losses capability • Big size due to heatsink • High cost PDs

widely deployed nationwide. In terms of technical obstacles, although there are numerous DC application standards available, LVDC microgrids currently lack standards for regulating and guiding technical aspects such as power quality, earthing arrangements, voltage levels, and protection solutions. At the moment, there is no definite agreement on the voltage levels for DC distribution networks, with Finland ((750V/±750V) the Netherlands (700V/±350V), China (±750V/220V) and the UK (950V/±475V) all taking distinct approaches. LVDC protection is the foremost focus among the technical difficulties associated with the limited installation of DC distribution networks. As pointed out previously, existing trial projects rely mostly on traditional overcurrent protection combined with an overrated converter to endure fault circumstances. The nature of the short-circuit fault current is highly dependent on the interfaced converter topology, as discussed in Section 2.4, with different converter topologies contributing to varied amounts of fault current. Therefore, the fault current contributions and protective capabilities of converters should then be regulated to assure the reliability, selectivity, and speed of LVDC protection systems. Meanwhile, protection strategies must be evaluated in conjunction with a variety of converter topologies and network architectures.

The two distinct operation modes of a LVDC microgrid present a challenge in terms of developing an appropriate protection solution, since the short circuit levels in the islanded and grid connected modes are quite different. During grid connected operation, the LVDC microgrid connects to the MV grid, so that grid and DG fault current levels increase gradually. The contribution of DG sources to fault current causes short circuit levels to exceed the rated values of systems, and therefore high capacity circuit breakers or reclosers must be installed. However, when operating in islanded mode, the LVDC microgrid is disconnected from the main grid and the fault current of DG sources equals the maximum capacity of the LVDC microgrid. This is because the fault currents generated in this operation mode are limited, and the fault current of the LVDC microgrid will be extremely low when compared to the fault current generated in the grid connected mode. This low current level is insufficient to trigger the protection devices, which are designed for higher current levels. Thus, to protect the LVDC microgrid, an enhanced protection solution that detects fault currents in both modes of operation is required [139].

One of two principal approaches to designing a system to regulate a bus voltage in a LVDC microgrid is to have all converters in the system regulate the voltage collaboratively, or to have only a converter (i.e. master-slave control) regulates the voltage while the rest of the system follows their lead. Islanding detection (ID), which is the process of determining when a main converter has been disconnected, is a vital element of any converter designed to operate in a LVDC microgrid and continues to be a complex and challenging task. If the ID method (IDM) is operating effectively, the system can immediately disconnect or switch to a controller optimised for this mode of operation. Thus, it is essential to select a suitable controller and IDM for islanded and grid-connected mode, in order to ensure that the DC system operates safely (by maintaining that the bus voltage is always regulated) and efficiently (ensuring that distributed sources operate in accordance with the rules of local optimization).

System earthing is another technical challenge. The earthing of a system is dependent on the application for which it is intended. For instance, the shipboard power system is expected to withstand a single earth fault, which is why high-impedance earthing is commonly used in such applications [47]. However, earthing is a complex issue in land-based systems, as there are numerous topologies and design approaches. It is required to ensure device and user safety in addition to enhancing the effectiveness of the microgrid system. A LVDC microgrid can be unearthed or earthed with high or low resistance, as discussed in Section 2.5.5. It is essential to have a code of practise and regulations in place that address the issue of LVDC microgrid earthing configurations and the impact of stary current corrosion. Along with addressing the implication of converters on protection solutions and the requirement for coordination between

converters and protection solutions, guidance and recommendations for designing protection devices are required. On the market, there are several DC protection devices (such as fuses and MCCBs) that are designed specifically for individual DC applications. To protect complex DC public distribution networks, however, it is essential that standards and regulations specify how these protection devices should operate within the networks. Additionally, developing technologies such as fault current limiters and SSCBs continue to lack industry standards and procedures that would enable their integration into future LVDC microgrids. These types of faults and challenges should be carefully addressed during the design of the protection solutions. The development of islanding detection methods, earthing systems, fault detection and location methods and the improvement of protective devices are vital for LVDC microgrids to be as reliable and secure as possible.

Aside from technical challenges, there are still significant economic challenges to overcome, such as a lack of market maturity for appliances that can be operated with relative ease on DC networks. This is also because a limited number of products are directly powered by DC, and that the vast majority of existing DC devices are connected through rectifier stages. Additionally, only a few manufacturers concentrate their efforts on the development and design of DC products, which hinders the market's growth. Hence, manufacturers are vital in establishing a new DC market that can serve as a source of competition for the expansion of DC distribution networks. Currently, the DC market is constrained by the comparatively high capital investment costs associated with the technology, which are higher than those associated with the AC technologies. For example, a high cost investment in developing protective devices [140]. Even though certain LVDC pilot projects are developing high-cost protection methodologies that may be viable for industrial applications, they are inappropriate for domestic applications that should be developed at a low cost and widely adopted in the market.

2.10 Key research themes identified in this thesis

It is possible to conclude from the preceding literature review that economic challenges are partially driven by technical challenges that impede the widespread implementation of LVDC microgrids, the most significant of which is the lack of effective and reliable earthing systems and DC protection solutions. Four distinct opportunities for research contributions have been identified in order to gain clarification on how these protection dilemmas should be addressed.

Firstly, there is an opportunity to evaluate the islanding detection approach in LVDC microgrids, as this is a particularly challenging task in DC systems due to the absence of certain parameters (such as phase and frequency) required to distinguish

the islanding event. Islanding is a major element of an electrical grid, which is why detection of islanding is critical. Islanding detection should be fast and accurate to ensure that the system transitions from non-islanding to islanding mode or vice versa. Two passive islanding detection approaches have been selected in this thesis because they are simple, easy to implement, and have no detrimental impact on the system's power quality. This investigation is primarily focused on the ability of these passive islanding detection methods to distinguish between fault (no-islanding event) and loss of main power (islanding event) and ensuring that the system maintains regulated power to the loads in a decentralised manner (without communications).

Secondly, in LVDC microgrids, there is an opportunity to scrutinise the functionality and fault characteristics of various earthing systems in order to determine how the DC systems should be earthed and how corrosion issues can be avoided. Frequently, a central earthing point based on a TN-S earthing scheme is incorporated into AC systems. Additionally, for DC systems, it is preferable to use a TN-S earthing scheme. However, if the system is composed of multiple decentralised sources, a single earth point is inappropriate. This will have consequences for the protection and the cost of the earthing of the systems. Also, when an islanding event causes a LVDC microgrid to lose its earthing system, a local earthing system is required to act as a path for earth fault current to flow through the earthing system. Consequently, whenever an islanding situation is recognised, the local earthing system should be triggered. The limited knowledge of the functionality of earthing a DC network with multiple earthing points has created an opportunity for research contribution.

Thirdly, there is an opportunity to improve the reliability and accuracy of the fault location method in order to facilitate and expedite LVDC post-fault maintenance. A number of different fault-location methods for DC systems have been reported in the literature, some of which require additional hardware to locate a fault, increasing the network's cost and requiring a repair crew to relocate external equipment around, while others rely on communication between the converters, which implies a reliability issue in the event that the communication channel is lost. Meanwhile, the implications of remote end converters have been inadequately investigated. These factors have a significant impact on the accuracy of fault distance estimation, providing an opportunity for new research contributions to this field.

Finally, an opportunity to enhance protection solutions and fault detection for high impedance faults has emerged. The absence of a zero crossing point is a fundamental challenge of DC protection; as a result, faults are more difficult to interrupt with fuses and circuit breakers than they are with AC protection. Additionally, converter-based DG sources operating in islanded mode contribute only a small amount of fault current, necessitating the development of a protection scheme capable of detecting DC fault

currents of very small magnitude. Also, a fault with a high impedance can be difficult to detect because the fault current is unlikely to trip the over current protection, and is instead more likely to be confused with a load step-up change, making it difficult to distinguish between the two.

2.11 Chapter 2 summary

This chapter discusses briefly the key factors promoting the adoption of LVDC microgrids, emphasising the increased pressure on existing LV networks, advancements in power electronics, an increase in the number of DC-operated applications, and the demonstrated benefits of LVDC, all of which play an important role in the transition to LVDC microgrids. Following that, the evolution of LVDC microgrids is discussed, including the concept of LVDC microgrids, development of an international and regional standard for LVDC, and descriptions of LVDC pilot projects. Additionally, LVDC technologies such as LVDC interfaces and earthing requirements are discussed, as well as the effects of corrosion on LVDC networks, DC protection devices, and measurements. Based on this literature review, technical and economic barriers to expanding the utilisation of LVDC microgrids have been identified. This justifies the choice of DC protection as the primary research topic for this thesis.

Several key findings were drawn from a review of relevant literature. To begin with, islanding detection in LVDC microgrids is a particularly difficult task due to the absence of certain parameters (such as phase and frequency) necessary to differentiate between islanding events. It was concluded that an investigation of islanding detection methods is required to define their capability to distinguish between non-islanding and islanding events. This will enhance a conceptual understanding of how islanding events can be detected and, ultimately, in designing an effective protection solution.

Secondly, it was concluded that fault characterisation and evaluation of various earthing systems are required in order to determine the proper earthing method for LVDC systems and how to avoid corrosion issues. Additionally, earthing an LVDC network with multiple earthing points is considered necessary, particularly in the event that an islanding event results in the loss of a LVDC microgrid's earthing system point. This will facilitate the understanding of how various earthing systems for LVDC microgrids affect the performance of protection systems.

Thirdly, to facilitate and expedite LVDC post-fault maintenance, it was concluded that a more accurate and reliable fault location technique is required that does not require additional hardware to locate a fault, and does not rely on communication between converters, but instead accurately considers the impact of remote converter fault current contributions when determining the fault distance.

Finally, it was determined that in order to detect a fault with high impedance and detect DC fault currents of very small magnitude, particularly during islanded mode, a method capable of providing effective fault detection and discrimination without relying on current thresholds is needed.

Chapter 3

Earthing Configurations in LVDC Microgrids

3.1 Introduction

LVDC microgrids will become more prevalent in the area of civil buildings as power electronics technology advances and distributed energy sources become more accessible. Although the voltage levels in civil buildings are not excessive, there are still significant electrical safety risks to equipment and users. Fast and selective fault protection remains a significant challenge in LVDC microgrids. The advancement of DC protection is hampered by the absence of reliable and effective earthing schemes capable of ensuring the safe and secure operation of LVDC microgrids in both grid connected and islanded modes.

LVDC microgrids can accommodate renewable energy resources such as photovoltaic, battery energy storage systems, and DC loads (electric vehicles) connected through power electronic converters. For those interfaced by converters such as DC renewable resources and in many cases, no galvanic isolation is used in between. This is driven by the need for cost and size reduction of the installation. However, such technologies can pose safety and common-mode noise challenges if the earthing of the microgrid is not properly designed. Additionally, the majority of work in the literature and on existing DC distribution trials has not demonstrated different DC earthing systems utilising different methods on a similar LVDC microgrid in order to determine the best protection strategy. Therefore, this chapter discusses various LVDC microgrid earthing methods and comprehensively evaluates the effect of various earthing methods on the fault behaviour of an LVDC microgrid via simulation studies.

3.2 System earthing requirements

The main objective of designing an earthing scheme is to ensure the safety of both humans and equipment. System earthing is vital for a power distribution network to operate safely and reliably [141]. The earthing aspects of LVDC microgrid networks have not been thoroughly investigated, and there are still safety concerns [142, 143]. As a result, it is essential to address earthing issues and identify earthing configurations that facilitate the network to operate more safely and reliably. This section discusses the requirements for DC safety specified in the IEC60479 and IEC60364 standards. This includes the risk of electric shock and the corrosion effects. Additionally, the available safety standards for mitigating the risk of electric shock and corrosion are discussed.

3.2.1 Risk of electric shock

The risk of electric shock can arise in faulted electrical systems when exposed conductive segments become 'live'. To mitigate this risk, these segments require an effective earthing and fault detection system capable of quickly resolving a fault before it affects the public or livestock [144]. As illustrated in Figure 3.1, the IEC60479 standard defined four time-current regions in the two-dimensional plane of the ventricular fibrillation current I and duration of the current flow t. The regions depict the various effects on the human body of a short-circuit electric shock. These include DC-1, where minor sensations are felt, DC-2 where muscles may involuntary contract, DC-3 strong muscle contractions and adverse heart effects are experienced, and DC-4 critical effects can occur that may result in death depending on exposure to the current [144]. It is therefore essential to select DC voltage levels and protection devices such as RCDs, that have a sufficiently short interrupting time and thus limit exposure to body currents. It is suggested in [145] that voltages less than 50 V DC pose no danger to humans, this is based on a body impedance of 1 kΩ and a threshold current of 50 mA. Additionally, according to IEC 60479-1 standard, it is recommended to earth the negative pole rather than the positive pole in two-wire DC systems. This is because earthing the positive pole causes the fault current to flow 'upwards' through the heart, increasing the likelihood of ventricular fibrillation. The threshold of ventricular fibrillation for a DC downward current is approximately twice as high for a DC downward current as it is for an upward current. Thus, two-wire DC systems should have an earthed negative conductor, so that contact with a live part at a positive potential exposes people to a downward flow of current with a reduced risk of ventricular fibrillation.

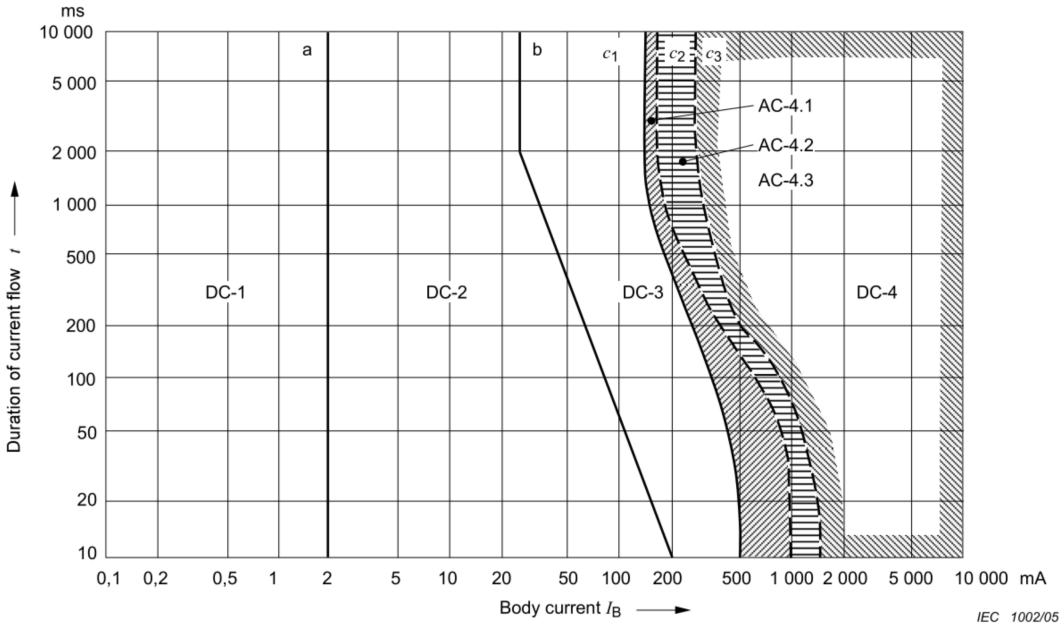

Figure 3.1: Characteristic curve of body current-duration of current flow [141].

3.2.2 Corrosion Effects

Corrosion is a result of chemical and/or physical reactions between a material and its environment, usually resulting in its damage. The corrosion reaction is an electromechanical procedure that transforms the metal into oxide and hydroxide. The effect of the reaction with the environment can result in a change of the material properties (in many cases its strength). This form of corrosion is not typical in day-to-day experience, but it is of great importance to the corrosion engineer. This is because understanding the cause of the corrosion will minimize the destructive procedure, save time and money and particularly maintain the safe operation of the facilities [146, 147]. Stray current (a type of metallic corrosion) is an electric current flowing along other elements that are not components of the custom-built electric circuit. In this case, the DC power circulates in a metallic structure and can be derived from the electrified traction system, the offshore structure, or from marine platforms, and then conducted through several parts of infrastructure in particular locations (such as reinforcement in concrete and buried pipelines). Upon a stray direct current interference, a cathodic reaction intervenes where the stray current penetrates the metallic structure, whilst an anodic reaction takes place where the current leaves the structure as shown in Figure 3.2. Often, this type of corrosion is localised and can have major consequences for a metallic structure [148]. The most well-known and accepted method of mitigating this issue is to install an appropriate earthing scheme (diode, thyristor and capacitor

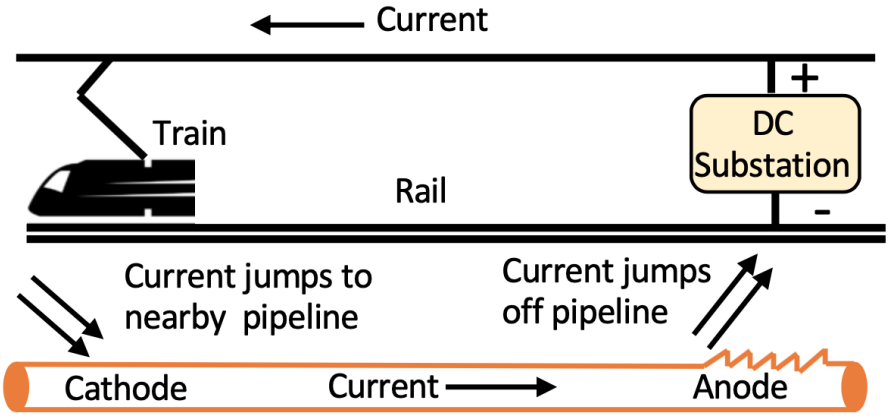

Figure 3.2: Railway stray current schematic diagram[149]

earthing schemes) between the pipe and the negative rail [148, 150]. By doing that it can prevent the current from flowing in the reverse direction. In this way, current is passed back to the rail electronically and there is no electrolytic current discharge from the pipe, as a result no corrosion occurs as shown in Figure 3.3. It is necessary during the planning, installation and commissioning stages that all other organisations having buried cables or pipes in near neighbourhood of the installation are completely aware of the circumstance [149, 151].

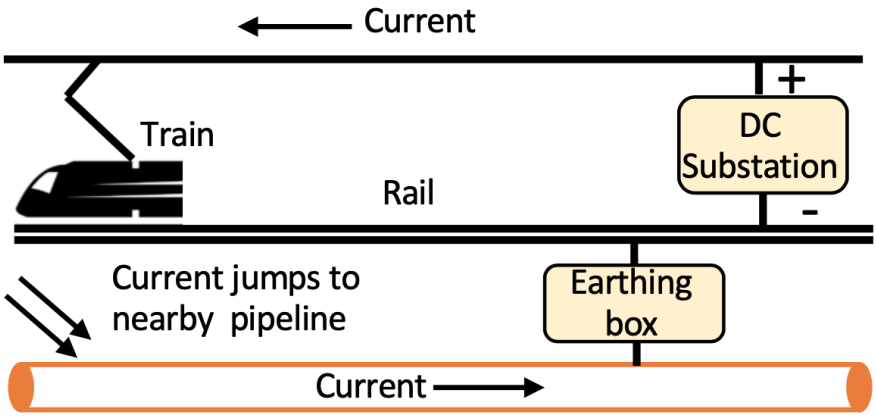

Figure 3.3: Railway drainage bond [149]

There are currently no specific standards that address or recommend ways to mitigate the effects of electrolytic corrosion. However, the IET's (Practical Considerations for DC Distribution) proposes that the IT earthing arrangement naturally reduces the earth current during faults, providing a high level of protection to the adjacent metalwork than the TT earthing arrangement [152]. However, IT earthing system is not common in public networks, unless galvanic isolation is used between the supply and the

end users. The British standard BS EN 50162 specifies in detail how to protect against corrosion caused by stray currents from direct current systems. Nonetheless, because this standard applies to traditional DC power applications, it requires an update to incorporate recent advances in LVDC distribution applications such as microgrids and building level distribution [153]. The -48 V telecom standard employs an earthed positive pole to mitigate against electrolytic corrosion; however, it is not recommended at high voltage levels and is considered to be more dangerous from the safety perspective [154]. As previously discussed, stray current corrosion has been extensively studied in direct current traction systems, and a reasonable analogy can be drawn when evaluating the impact of large photovoltaic (PV) plants on an LVDC network (refer to Figure 3.4). Stray current interference from DC traction systems is characterised by periodic fluctuations of relatively short duration and fast corrosion potential variations. Solar farm interference is more likely to be related to the basic properties of photovoltaic current generation, with longer-term effects. To this end, consider the situation in which a faulted dc buried cable (which may act as the source of stray leakage current into the soil) shares a parallel corridor with buried metallic infrastructure (such as gas pipelines) located within or near the PV plant. It is highly likely that a portion of the stray leakage current from the faulted dc cable is picked up by nearby metallic infrastructure, travels a distance before discharging back into the soil, and then returns to the energy source. The latter rationally assumes that the stray current will attempt to return to its source via any low-resistance paths in the soil. As a matter of fact the metallic structures can provide these low resistance paths by nature, particularly when these structures are bare or not perfectly insulated. Consequently, severe damage can occur to metallic structures at the point where the current discharges back into the soil to return to its source of energy. DC leakage currents can create potentially hazardous situations. It is essential to carefully regulate the amount of current flowing, and to reduce or even prevent its flow. The calculation of metal loss due to stray current corrosion is based on Faraday's laws: [156]

$$M_{metal} = K.I.t \tag{3.1}$$

where M_{metal} the mass of metal that reacts (in grams), K the electrochemical equivalent, constant which value depends on the metal considered (in gram per coulomb), I the current (in amperes), and t the duration of the current flow (in seconds). For steel, indicate that 1 A of constant current flowing for one year will corrode approximately 9.1 kg. The value of 20 mA revealed as the blind spot by the authors of [155] indicates that when the corresponding leakage currents are below the detection values of the monitoring devices (i.e., if the system is floating the threshold is approximately

30 mA), then these can be left unattended for an extended period of time, resulting in the constant flow of leakage currents through unintended return paths through the soil or other conductive materials. Thus, it is essential to remember that the insulation condition of underground dc cables, the size and age of the PV plant, and the soil characteristics (e.g., moisture content) of the area it occupies greatly influence the stray current in large solar systems.

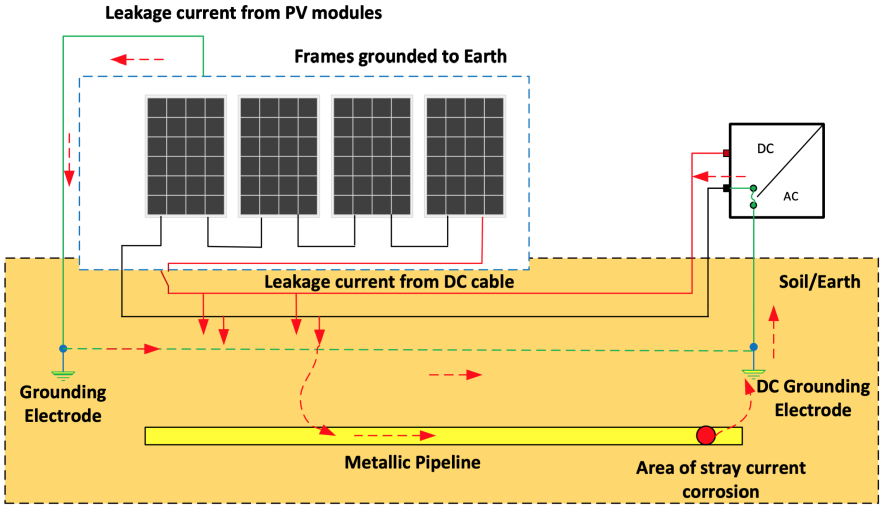

Figure 3.4: DC leakage currents paths of earthed PV systems [155]

3.3 Different earthing Configurations

Earthing is a fundamental topic for electrical systems and a necessary brief summary is presented in this section. The well-known earthing schemes used in terrestrial systems are classified using two letters [157]. The first letter refers to the source connection and the second letter refers to the load connection. The letters can be T (for Terre, earth in French), I for isolation and N for neutral (refer to Table 3.1). According to IEC 60364-1 there are three earthing configurations available Terre-Terre (TT), Terre-Neutral (TN, with three subclasses TN-C, TN-S and TN-C-S) and Isolated-Terre (IT) [94, 158].

In TT networks, the source and the loads are connected directly to earth through separate electrodes as shown in Figure 3.5.

Figure 3.6 illustrates this earthing scheme under a faulted situation. The circuit is closed through the ground impedance R_G and the fault current I_f is:

$$I_f = \frac{V_s}{R_G} \tag{3.2}$$

Table 3.1: Nomenclature of earthing configuration

Earthing Nomenclature	**T**	**I**	**N**
1^{st} letter (earthing of source bus)	Direct connection of the earth	No connection of the earth	-
2^{nd} letter (earthing of conductive parts)	Direct earthing of the exposed conductive parts	-	Connection of the exposed parts to the earth neutral

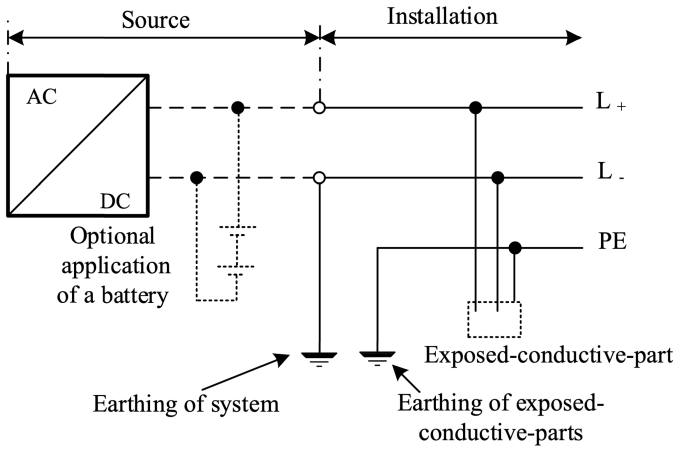

Figure 3.5: Earthing scheme for TT [159]

The ground impedance is not known exactly and the clearance of the fault is not guaranteed as the current may be not sufficient to trigger the circuit breaker. This is why it is mandatory to use a residual current device (RCD) in TT networks mainly for personnel safety reasons [161]. Additionally, this earthing configuration produces circulating currents, which means there is a possibility of causing high voltage stress and it is unable to prevent corrosion [94, 162]. The current circulating through the human body is determined by the touch DC voltage and the human body resistance (which varies with moisture).

There are three sub-categories of TN networks, namely, TN-C, TN-S, and TN-C-S. Figure 3.7 shows the TN-C scheme, where the earthed line conductor for example $L-$ is the same as the protective conductor (PEL, the functions of earthed line conductor $L-$ and the protective conductor are combined in one single conductor throughout the installation). This is, in theory, the most cost effective and lightest procedure [94, 158]. However, it is the worst option from the point of view of EMC (electromagnetic compatibility) as the earthed line conductor $L-$ can also conduct electricity when load unbalance is present [94, 158]. This consideration is especially important as high frequency currents coming from any PWM power electronic converters may contaminate

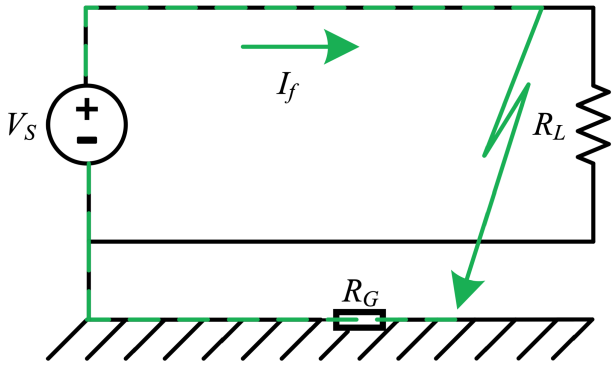

Figure 3.6: Earthing scheme for TT under pole-to earth fault [160]

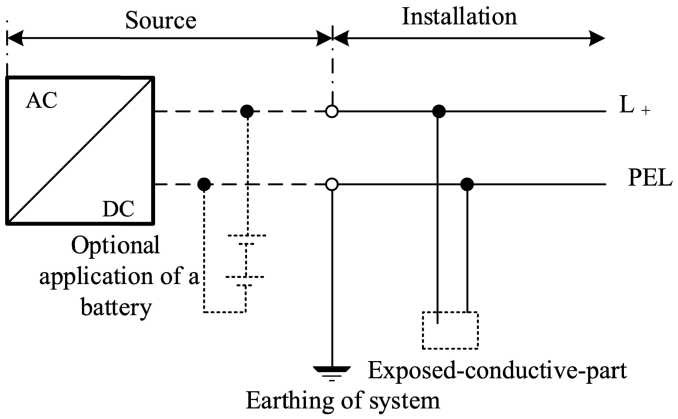

Figure 3.7: Earthing scheme for TN-C [159]

the earthed line conductor. In the TN-S configuration, shown in Figure 3.8, the earthed

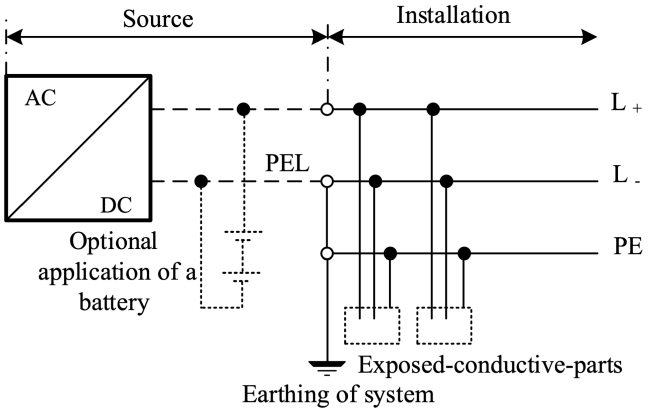

Figure 3.8: Earthing scheme for TN-S [159]

line condcutor $L-$ is separated from the protective conductor throughout the instal-

lation [94, 163]. This option is expensive as it requires an extra cable to be deployed [94]. In the TN-C-S configuration, shown in Figure 3.9, the functions of earthed line

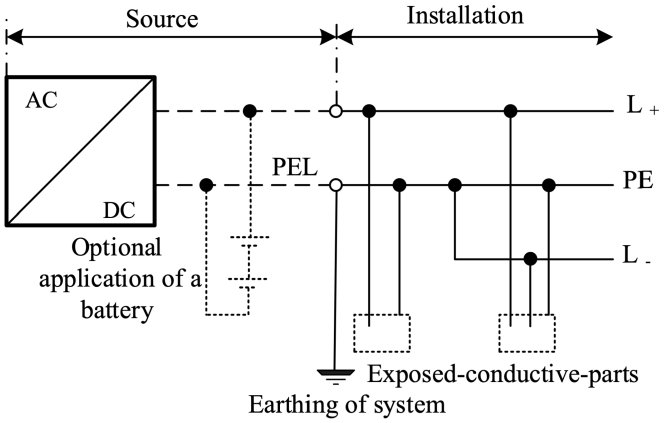

Figure 3.9: Earthing scheme for TN-C-S [159]

conductor $L-$ and the protective conductor are combined in one single conductor in a part of the installation, but they are separated upstream. It is not recommended to combine the earthed line conductor $L-$ and the protective conductor downstream of a TN-S network as there is a risk of losing the earth if the protective conductor is broken upstream. TN networks result in very high fault currents that can easily trip a short-circuit relay. In some cases, those elevated currents can be dangerous as they may result in fire (especially TN-C) or large electromagnetic forces/interference [94, 162].

In the IT configuration shown in Figure 3.10, the source is isolated from the earth or connected to it through a very large resistance R_I [94, 158, 161]. The IT earthing

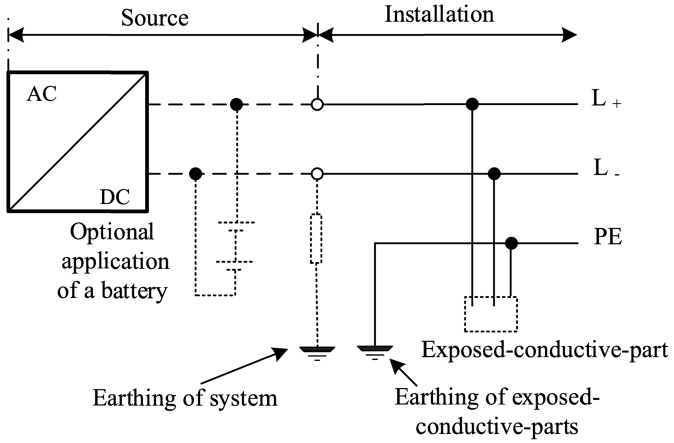

Figure 3.10: Earthing scheme for IT [159]

configuration is widely used in applications where earthing is difficult, but above all

where continuity of supply is required following an initial earth fault. However, if none of the conductors are earthed, there is a risk that dangerous over-voltages could take place between an exposed conductive part and the earth due to static electricity. In order to mitigate this risk, overload discharges can be used [160].

Figures 3.11 and 3.12 show an IT network under a first fault and a second fault respectively. In the event of a first fault between the positive conductor and the earth (refer to Figure 3.11), the plant operation is unaffected due to the current has no reclosing paths and therefore it cannot circulate. Whereas in the event of double fault (refer to Figure 3.12), the current may circulate and eventually find a reclosing path. Therefore, it is preferred that a device capable of sending signals indicating an earth fault to be installed in the plant. In this manner, the fault is eliminated in a timely manner to prevent the occurrence of a second earth fault on the other conductor. In addition, it should be noted that full earth isolation is not guaranteed as the capacitive coupling is always present [94, 161]. This will make the fault location more difficult to be determined.

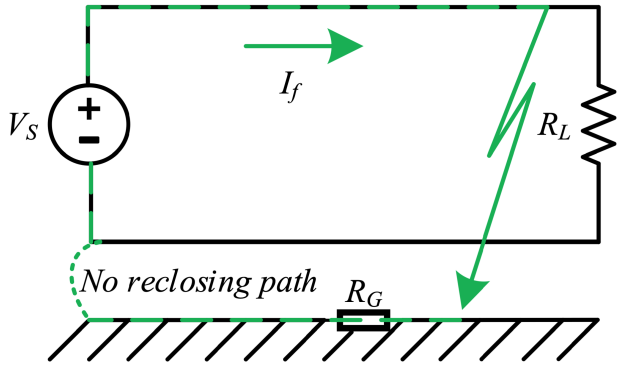

Figure 3.11: Earthing scheme for IT under the first fault [160]

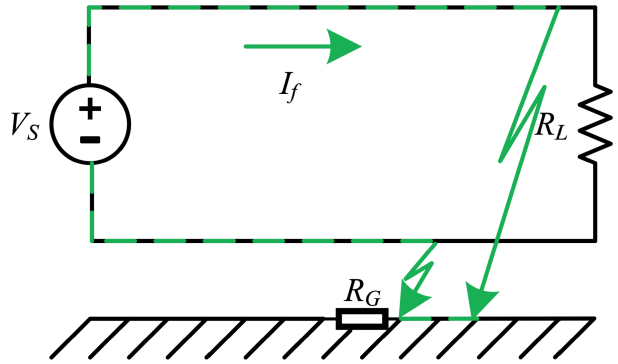

Figure 3.12: Earthing scheme for IT under the second fault [160]

3.3.1 Earthing connection through impedance and semiconductor devices

The earthing method utilised on the DC side is dependent on the earthing method utilised on the AC side. When the AC side has an earthing point, it is preferable to unearth the DC side. When the AC side is not earthed, the DC side's earthing method selection becomes more flexible. From a DC source-side earthing perspective, LVDC microgrid earthing modes are typically classified as unearthed (floating), earthed by solid earth, resistance, and reconfigurable earthing selections.

Unearthed DC networks

The primary advantage of an unearthed system is that it allows for continuous operation of the LVDC microgrid in the event of a single pole-to-earth fault and produces very little stray current [164]. Additionally, because no devices are connected to the negative pole (refer to Figure 3.13), this earthing system is simple and economical. However,

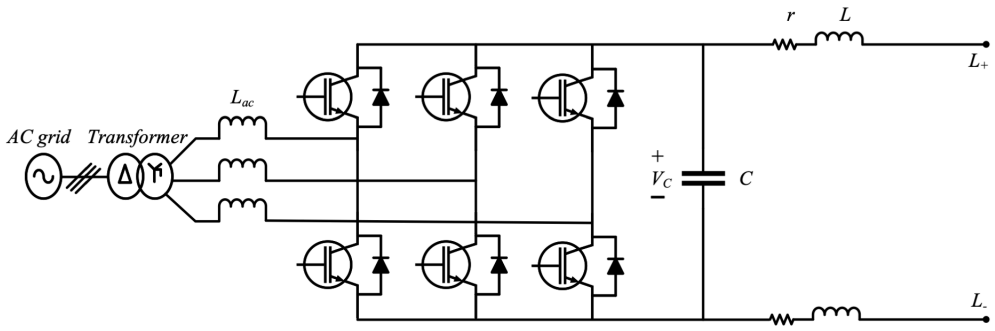

Figure 3.13: DC bus unearthed

the level of CMV in the unearthed system may be high, posing a risk to personal safety. Additionally, due to the low earth current, fault detection is difficult, and a second pole-to-earth fault in another pole results in a pole-to-pole fault, which has the potential to cause significant damage [165]. As a result, fault detection in the unearthed system is critical for improving these systems' performance [142],[166]. It is necessary to implement more sensitive insulation monitoring schemes, in which AC or DC signal injection is used to monitor the system response, in order to detect the loss of insulation caused by an earth fault [167, 168]. Nonetheless, the unearthed system is used in some applications. For example, on navy ships, the earthing system of their network is floating to ensure the uninterrupted supply of energy to critical loads [169].

High resistance earthing

Similar to unearthed DC networks, high resistance earthed systems (refer to Figure 3.14) enable fault ride-through capability due to the absence of a low resistance path for the circulation of earth current [143, 170, 171]. Earth current magnitude can be

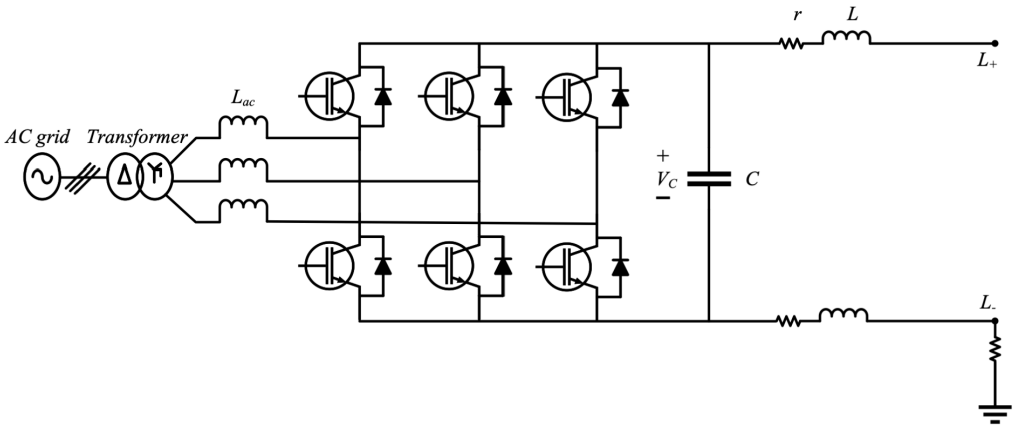

Figure 3.14: High resistance earthed

kept to a safe level during a pole-to-earth fault by carefully selecting earthing resistance [143, 163]. Generally, earthing resistance is chosen so that a pole-to-earth fault produces a small current flow that enables fault detection but is not so large that it poses a threat to human safety [143]. In these networks, earth current monitoring and insulation monitoring relays can be used to detect pole-to-earth faults. In [172] the authors proposed a directional element for locating earth faults in high-resistance earthed networks. Additionally, the authors in [173, 174] proposed a method based on digital signal processing for locating faults in high-resistance earthed networks. As with unearthed DC networks, high-resistance earthed networks minimise stray current flow but are susceptible to transient overvoltages during disturbances [167, 175].

DC network solidly earthed

When the DC negative pole is solidly earthed (refer to Figure 3.15), it generates a measurable amount of earth current, effectively creating a pole-to-pole fault during an earth fault. As a result, the network reacts as if it were experiencing a pole-to-pole fault, necessitating immediate protective actions[163, 167, 176]. Earth current monitoring relays can be used in these networks to detect earth faults [167]. Earth currents as low as a few milliamps are easily detected by today's high-sensitivity relays [177, 178]. Another advantage of this configuration is its ability to absorb network disturbances and mitigate voltage spikes caused by such disturbances. A solidly earthed DC network, however, is degraded by stray current flow [42, 163, 179].

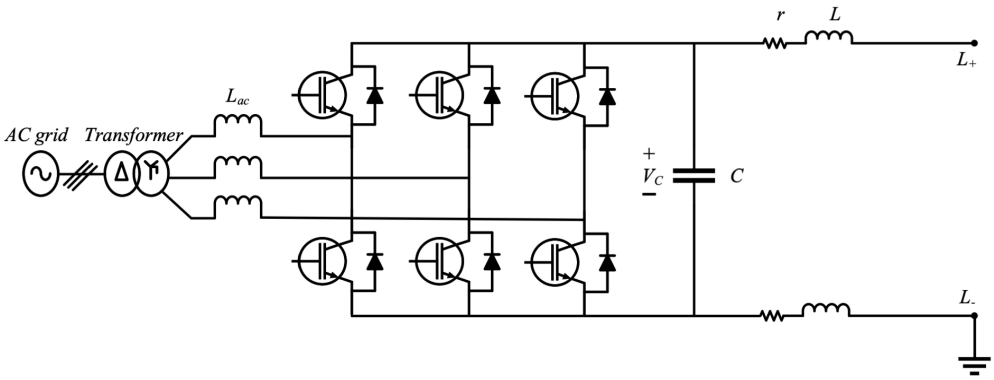

Figure 3.15: DC bus solid earthing

Reconfigurable earthing options in LVDC microgrids

As previously discussed, when selecting an earthing configuration for an LVDC microgrid, minimising stray current, avoiding dangerous transient overvoltages, and facilitating earth faults are essential requirements. In contrast to the DC network earthing methods discussed previously, the authors in[164] present reconfigurable earthing methods for DC traction networks, where the network is operated in an unearthed configuration to minimise corrosion intensity and is earthed when a high voltage is detected. Reconfigurable earthing is primarily recommended for DC traction networks to reduce stray current [180, 181].

In DC traction, a 12-pulse thyristor bridge at the station supplies DC power to the catenary. The return path is formed by the railways so that no extra copper is required. Ideally, all the current should circulate through the railways. In practice, the currents find a low impedance path through the resistance between the railways and the earth. The currents circulate through the metallic structures (pipes) that are connected to the earth, as shown in Figure 3.16, and it results in corrosion.

Figure 3.16 illustrates the earthing schemes for DC traction where R_c is the catenary resistance, R_R is the railway resistance, and R_s is the stray resistance between the railway and the earth. The stray resistance is distributed, but it is shown lumped for the sake of simplicity. Finally, R_G is the resistance for the earth connection. The station is modelled as a simple voltage source and the train motor drive as a simple current source. In order to prevent the corrosion in DC traction, current collect mats are used and solid earthing is not admitted [180]. For the case with the earth connection through a resistor, the current circulating through the earth (and not through the rail) is:

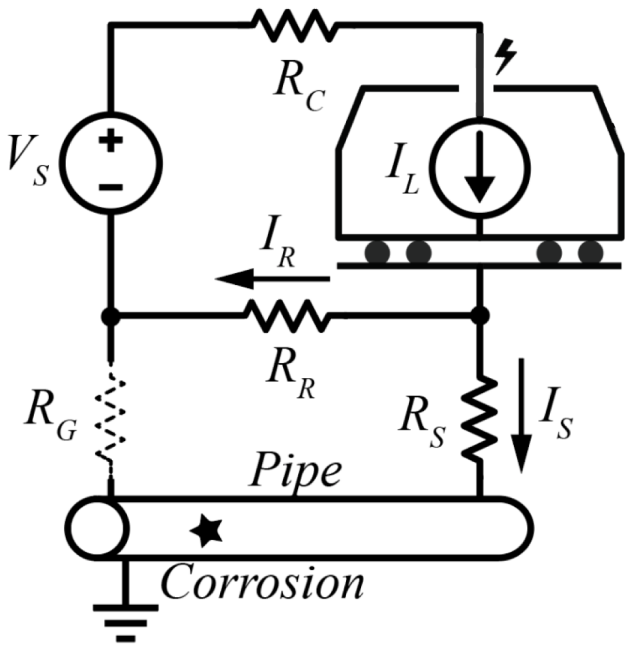

Figure 3.16: Earthing in DC traction

$$I_s = I_L \frac{R_c}{R_s + R_G + R_c} \tag{3.3}$$

It can be seen that the return current to earth is maximum (and so the corrosion) when R_G=0 (solidly earthed) and minimum when $R_G \to \infty$ (isolated earth). Therefore, it would be advisable to use an isolated earth. However, insulation monitoring relays must be used to detect ground faults in these networks, which increase the network's cost. Instead of a passive element for earth connection, DC traction can use semiconductor devices. The most common procedure (refer to Figure 3.17), consists in using a diode to connect the station's negative terminal to the earth [182]. Assuming an ideal diode with a voltage drop V_t (approx. 0.7 volts) and no resistive drop, the stray current results:

$$I_s = \frac{I_L - V_t/R_c}{1 + R_s/R_c} \tag{3.4}$$

This value is only valid for $I_L > V_t/R_c$ If this condition is not met, then the stray current is ideally zero. In practice, there is a permanent leakage current circulating through the diode because it is not ideal [94]. During faults, the diode allows circulating fault currents as it is inversely polarised.

More control can be established when using a thyristor (semi-controllable device),

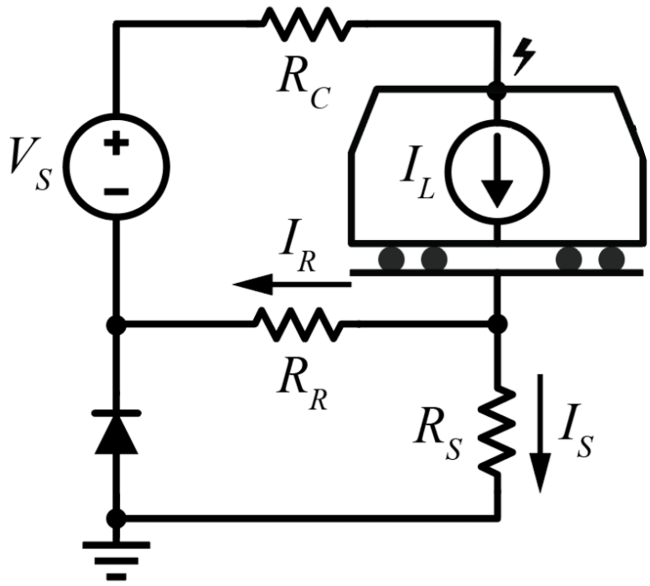

Figure 3.17: Diode connection in DC traction

as shown in Figure 3.18, instead of a diode [183]. When the thyristor is not conducting, the stray current is theoretically null and the voltage across the negative terminal and earth is:

$$V_{-GND} = -I_L R_c \tag{3.5}$$

After a pole-to-earth fault occurs on the positive terminal (catenary) the voltage across the negative terminal at the substation and the earth is:

$$V_{-GND} = -\frac{R_s}{R_s + R_R + R_c}\left[(1 + \frac{R_R}{R_s})V_s - I_L R_c\right] \tag{3.6}$$

The thyristor gate is triggered when the negative-to-earth voltage exceeds a threshold value. When the current decays to values close to the regular stray current, the thyristor is turned-off. If the current does not decay, then a positive pole-to-earth fault is the most likely to have happened and the DC feeder breakers are tripped. The advantage of using a thyristor is that it keeps the system permanently unearthed except during faults, so the stray current is minimised [94]. As the problem with corrosion becomes more serious, most of the DC traction systems leave the rails floating and use a stray current monitoring system for safety [164].

In the case of LVDC microgrids, the use of reconfigurable earthing configurations has not yet been investigated. In this chapter, a capacitive earthing scheme (capacitor connected in parallel with the diode) is considered as a reconfigurable earthing method, in which the network is unearthed during normal operation to minimise stray

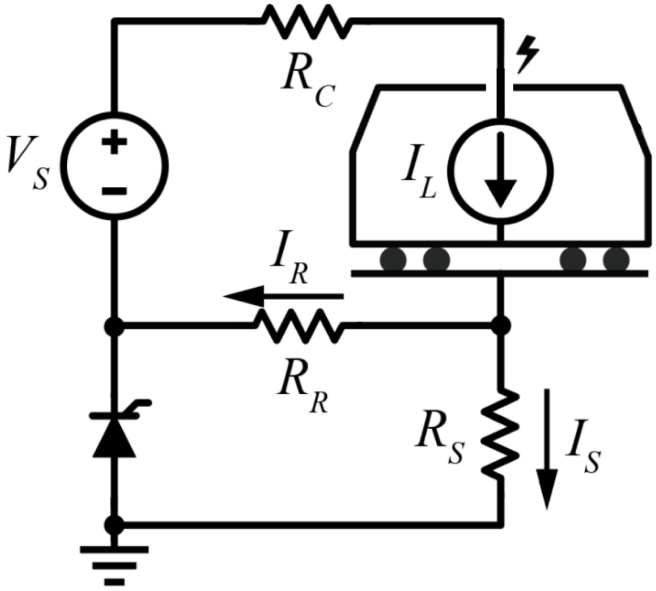

Figure 3.18: Thyristor connection in DC traction

current corrosion, and switches to earthed mode to detect the earth fault current. Additional details regarding the capacitive earthing implementation will be discussed in the following section.

3.3.2 Implementation of capacitive earthing scheme

For LVDC microgrids, a capacitive earthing scheme has been developed to prevent DC current leakage in the protective earthing conductor (under normal operating conditions) and to also form a conducting fault path during DC pole-to-earth faults [184, 185]. The advantage of this earthing scheme is discovered in this thesis to be useful for detecting and locating a faulty feeder. Capacitor within such an earthing scheme is charged during fault conditions by transient currents that are proportional to the fault distance and resistance. As a result, the distance to the fault can be estimated by examining the scheme's response during the fault.

Steady state condition

During steady state operation, the use of a capacitive earthing scheme means the impedance to earth is infinite. As a direct consequence of this, the flow of DC earth current can be restricted, preventing corrosion. Alternatively, for high frequencies, the capacitor impedance decreases and hence, acts as a low resistance earthing scheme for fast transients.

Under earth fault condition

In the event of a pole-to-earth fault, the fault current will circulate through the capacitive earthing. Figure 5.1 illustrates a simplified representation of the capacitive earthing scheme and the corresponding voltage and current signatures across the capacitor when a pole-to-earth fault occurs . At $t = 1\ ms$ the switch, S, closes (i.e. fault is triggered) and current flows into the capacitor (the capacitor, Ce, is considered to be initially discharged). The resistor, R_f, is being used to represent the fault resistance, and the the capacitor's charging behaviour is described in (3.7) and (3.8):

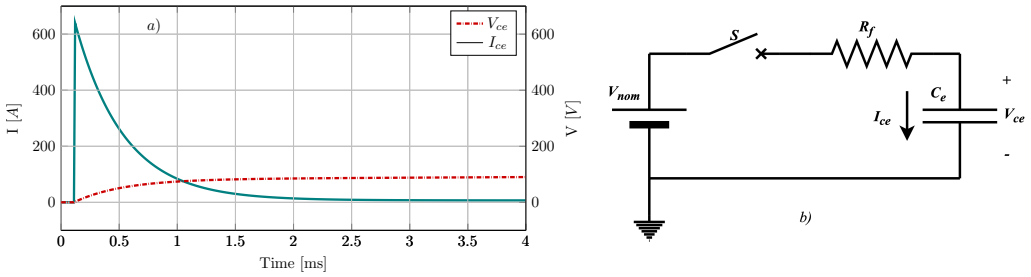

Figure 3.19: Capacitive earthing scheme under pole-to-earth fault: a) Voltage and current signatures, b) Simplified circuit representation.

$$V_{ce}\left(t\right) = V_{nom}\left(1 - e^{-\frac{t}{\tau}}\right),\ \tau = R_f C_e \tag{3.7}$$

$$i_{ce}\left(t\right) = C_e \frac{\mathrm{d}}{\mathrm{d}t} V_{ce} = \frac{V_{nom}}{R_f} e^{-\frac{t}{\tau}} \tag{3.8}$$

where, V_{ce}, is the voltage across the earthing capacitor, V_{nom}, is the nominal voltage of the supply network, i_{ce}, is the current flowing through the earthing capacitor and τ is the time constant.

Voltage clamping

The earthing capacitors will charge following the occurrence of a fault and prior to its isolation. If nothing is done, their voltage may approach that of the voltage across the fault. Thus, it is necessary to clamp the voltage to prevent the DC capacitor from fully charging. With the addition of a voltage clamp, the voltage across the capacitors can be limited to avoid dangerous overvoltage. A voltage-clamping diode is connected in parallel with the capacitor earthing as shown in Figure 3.20. An equivalent voltage clamping scheme can be made of a string of series-connected diodes, connected in

parallel with the earthing capacitors. By doing so, when a fault occurs in the network, the earthing capacitors continue to charge for the duration of the time window during which the fault remains undetected.

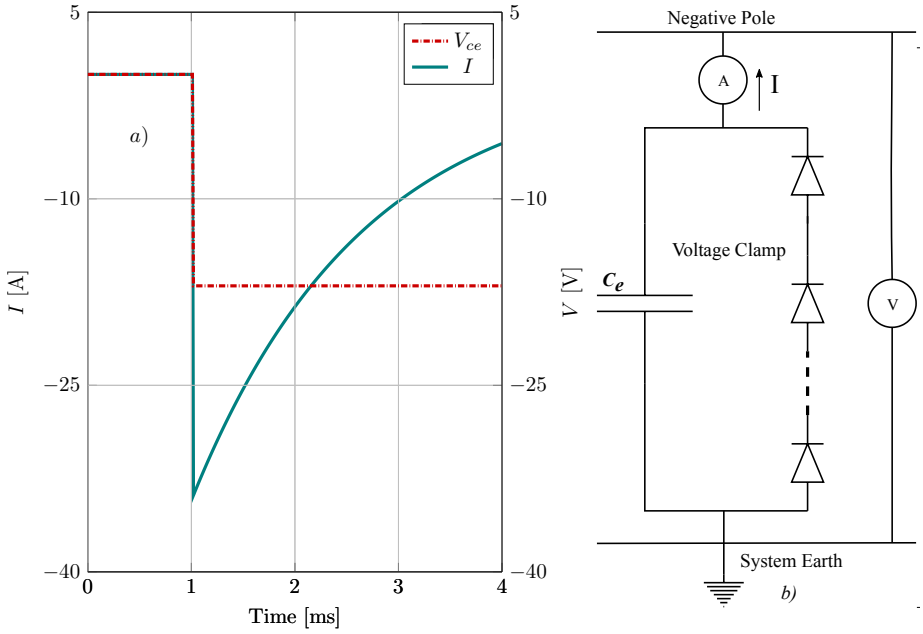

Figure 3.20: Voltage clamping scheme: a) Voltage and current signatures, b) Equivalent circuit.

The voltage across the capacitor earthing can be regulated by including a voltage clamping diode. When the voltage across the capacitor reaches the clamp voltage, the diode begins to conduct, preventing the voltage from rising any further. While the diode is conducting, the system is earthed by an equivalent low-resistance earthing scheme (i.e. zener diodes provide a low-resistive conduction path).

3.3.3 Capacitor sizing

It is essential to correctly size the earthing capacitor in order to allow enough time for the protection device to isolate the fault before the capacitor reaches clamp voltage. This prevents the voltage-clamping diode from conducting during the fault condition. To achieve this, it is desirable to keep the earthing capacitor charged in the network. The earthing capacitor size is calculated using the IEC 60479-1 standard, which specifies the maximum trigger time for protection operation [186]. Here, the following assumptions have been made:

- The maximum resistance of the fault path is chosen to be 1050 Ω, the value at which the body impedance is at its maximum. Note that this maximum fault path resistance value is only used to determine the size of the earthing capacitor.

- The total inductance value of a fault loop varies according to its location. A higher inductance value will lead to a lower di/dt of the fault current. As such, it is not considered in the calculation because it may have an effect on the earthing capacitor sizing.
- The voltage across the fault is determined by the load connected to the faulty pole and is referred to as the nominal pole voltage.
- Calculations are performed using the maximum fault current.

The following equation describes the capacitor voltage:

$$V_{ce}(t) = V_{nom}\left(1 - e^{-\frac{t}{\tau}}\right),\ \tau = R_f C_e \tag{3.9}$$

By considering that V_{ce}=V_{clamp}, and that during the fault V_{nom}=V_f, the size of the earthing capacitors can be calculated using equation (3.12) [187], where V_{clamp} is the clamp voltage, V_f is the voltage across the fault, R_f is the fault resistance, and t_{max} is the maximum time for the protection to operate.

$$V_{clamp} = V_f\left(1 - e^{-\frac{t_{max}}{R_f C_e}}\right) \tag{3.10}$$

$$\Leftrightarrow \frac{1}{C_e} = -\frac{R_f}{t_{max}}\ln\left(1 - \frac{V_{clamp}}{V_f}\right) \tag{3.11}$$

$$\Leftrightarrow C_e = -\frac{t_{max}}{R_f}\left(\ln\left(1 - \frac{V_{clamp}}{V_f}\right)\right)^{-1} \tag{3.12}$$

3.4 System response with different earthing methods under pole-to-earth fault

This section examines the response of an LVDC microgrid to a pole-to-earth fault using various earthing methods (refer to Figure.3.21). These earthing methods are connected to the negative pole of the DC network (as previously explained, in order to protect people from upward current circulation), and simulation studies are conducted to determine the effect of various earthing methods on the pole-to-earth fault current.

3.4.1 Modelling

A model of an LVDC microgrid test network with negative pole earthed using various earthing methods is developed and used for simulation validation studies as illustrated in Figure 3.22. The DC network is coupled to a secondary substation with a transformer

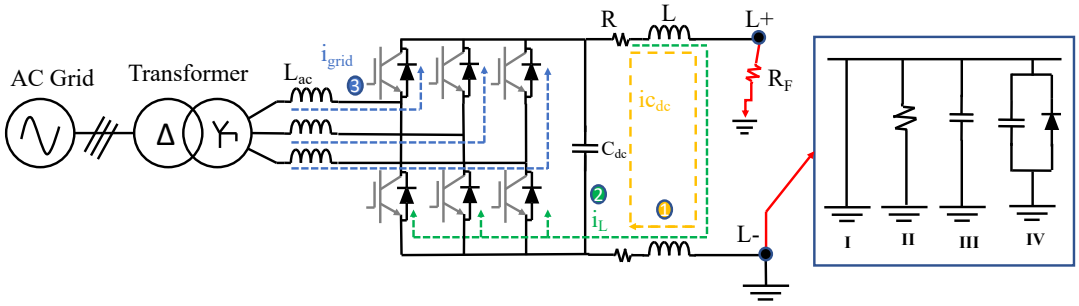

Figure 3.21: Current path of the fault current following the occurrence of a positive pole-to-earth fault using various earthing methods.

rating of 11/0.4 kV via a two-level voltage source converter (VSC) and is modelled in PSCAD/EMTDC. For modelling purposes, the secondary side of the transformer is earthed with a high-resistance 1MΩ (i.e. IT earthing scheme). The parameters of the LVDC microgrid test system are illustrated in Table 3.2. At the point of common

Table 3.2: AC and DC Network Parameters

Parameter	Value
AC grid Voltage [kV]	11
Transformer voltage ratio [kV]	11/0.4
Choke inductance [LChoke][H]	0.003
DC-link capacitance [Cdc][uf]	3300
LVDC main voltage	750 V (pole to pole)
R, L, CSA of LV cable	0.164 Ω/km, 0.24 mH/km-185mm^2 [188]
cable length [km]	1
PV rating[kW]	10
DC resistive load[kW]	10

coupling, the VSC converter provides a 750 V DC voltage at the Bus A (Upstream). A one-kilometer feeder is modelled using a resistor in series with an inductor. A photovoltaic array and battery storage are coupled to the DC Bus B (Downstream).

3.4.2 Simulation results

This research investigates four distinct earthing methods: solidly earthed DC bus, high resistance earthing, capacitor earthing, and capacitor in parallel with diode earthing. At the LVDC microgrid's main feeder, a DC positive pole-to-earth fault is applied (refer to Figure 3.22). For these studies a temporary fault has been applied, the fault is initiated at time t = 0.5 s and lasts 100 ms to capture the transient fault and steady state current, and then the fault is cleared at time 0.6 s.

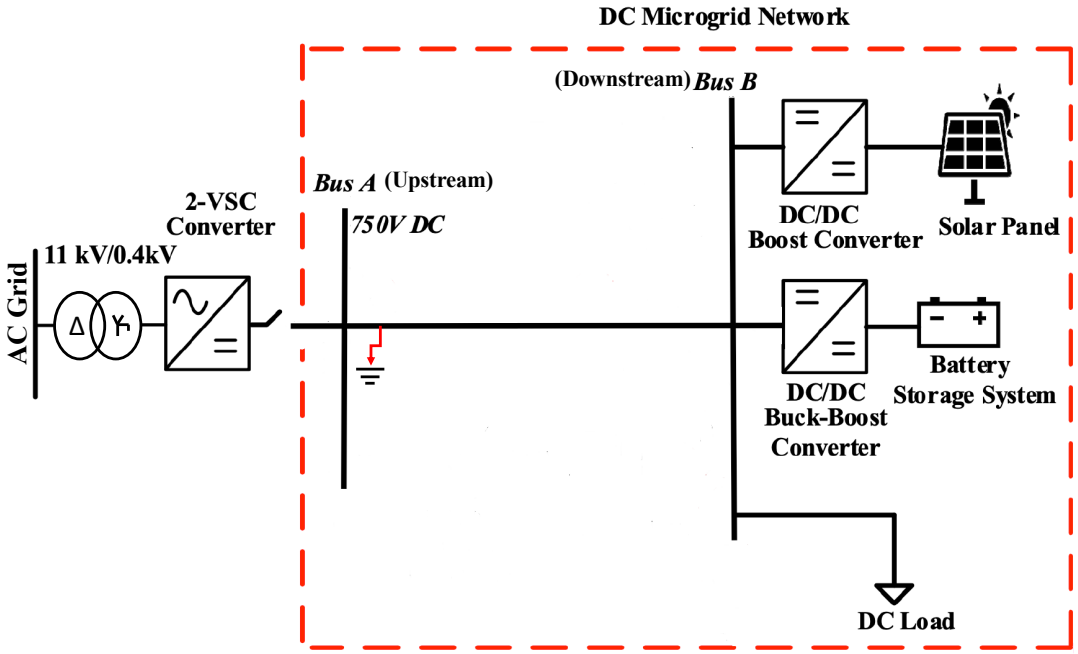

Figure 3.22: DC microgrid test network.

Case I: negative pole is solidly earthed

When the negative pole is solidly earthed, a DC positive pole-to-earth fault is initiated at time t=0.5 s, effectively resulting in the formation of a pole-to-pole fault during an earth fault. As a result, the network behaves as if it were experiencing a pole-to-pole fault. The DC link voltage V_{dc} is completely collapsed as shown in Figure 3.23(a). The capacitor of the VSC converter is completely discharged in this configuration, resulting in a transient fault current $I_{upstream}$ of 1.7 kA peak. This is followed by forward biassing the antiparallel diodes, which results in an uncontrolled steady-state fault current flowing from the AC grid to the fault point, as illustrated in Figure 3.23(b). Additionally, the PV and BESS contributed to the fault current from the downstream side, as their DC/DC converter interfacing is modelled without limiting the fault current functionality. Under this faulted condition, the total transient fault current from upstream and downstream is approximately 2.6 kA, as shown in Figure 3.23(b). Thus, in order to protect an LVDC microgrid interfaced by two-level VSC solidly earthed from overcurrent, fast-acting protection schemes are required to isolate the faulted component in a timely manner. Otherwise, over-dimensioning would be required for equipment with higher ratings.

Case II: negative pole is earthed through high-resistance

Earthed systems with a high resistance are analogous to unearthed DC networks. If the resistance value is extremely large, it can be considered infinite, and if no connection

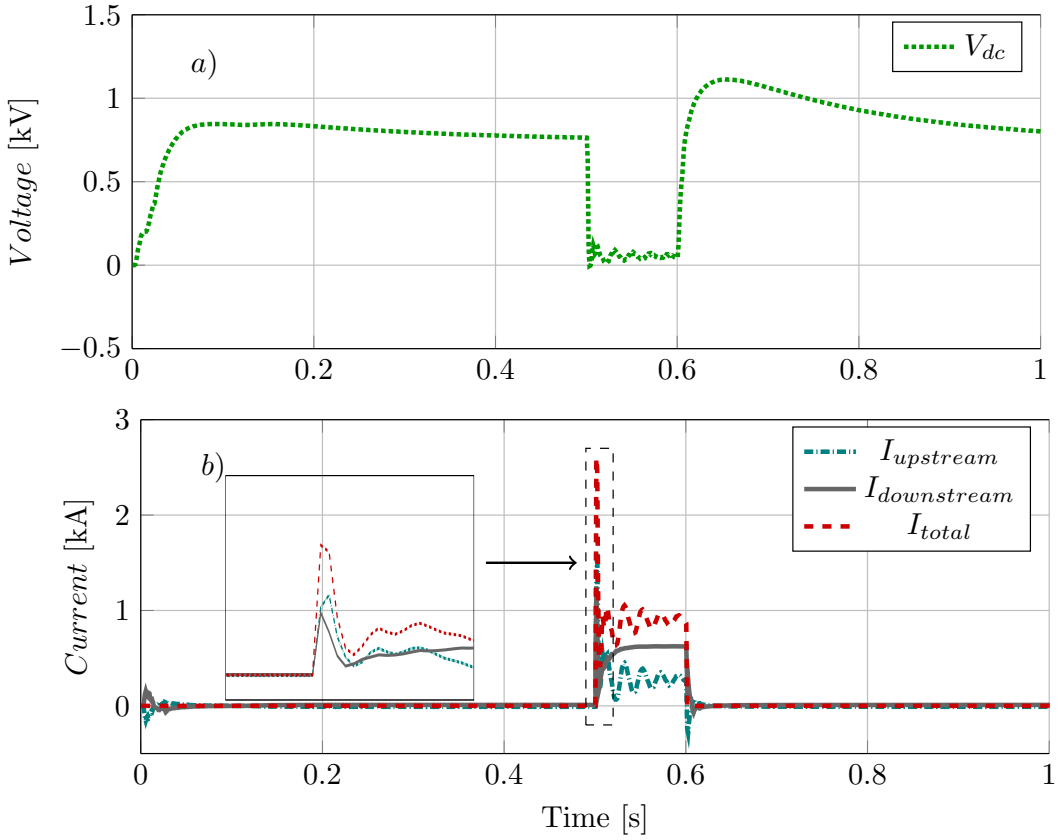

Figure 3.23: Pole-to-earth fault system responds with solid earthing (a) DC voltage response (b) Upstream DC current, downstream DC current and total fault current transient.

exists at all, the system is unearthed (IT network). In this case, a 50 k Ω earthing resistor is assumed to be used in the simulation study, and two faults are initiated with different times of 0.45 s and 0.5 s to simulate the first and second faults at the LVDC microgrid's main feeder (refer to Figure 3.22). The system operates continuously and without interruption during the first pole-to-erath fault at t= 0.45 s. Thus, only a parasitic capacitance is discharged because there is little energy stored, making the fault current difficult to detect as shown in Figure 3.24. After the first fault occurs on a network, power can be continued and a warning alarm set. However, the fault should be cleared as quickly as possible because the IT network becomes a TN or TT system and a second fault results in a failed operation, as illustrated in Figure 3.24 when the second pole-to-earth fault (i.e. pole-to-pole fault) is initiated at t= 0.5 s the transient fault current $I_{upstream}$ reaches 1.7 kA. It is concluded that during the first fault with the large resistor, the system will promote safe operation of the DC network, as the fault current can be significantly limited by the earthing resistance. However, the risk

increases during the second fault, which can create a path for the fault current, posing a safety hazard in the LVDC microgrid network.

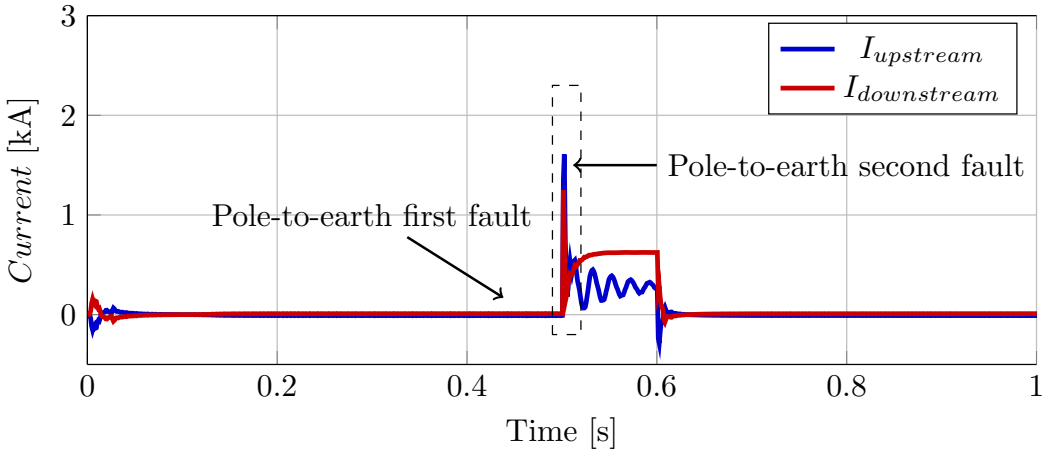

Figure 3.24: Pole-to-earth fault system responds with HR earthing

Case III: negative pole is earthed through capacitor and resistor

As previously stated, reconfigurable earthing methods are vital for LVDC microgrids in order to minimise corrosion intensity, as both solid earthing and earthing with a high resistance method cannot provide the level necessary to reduce stray current. A

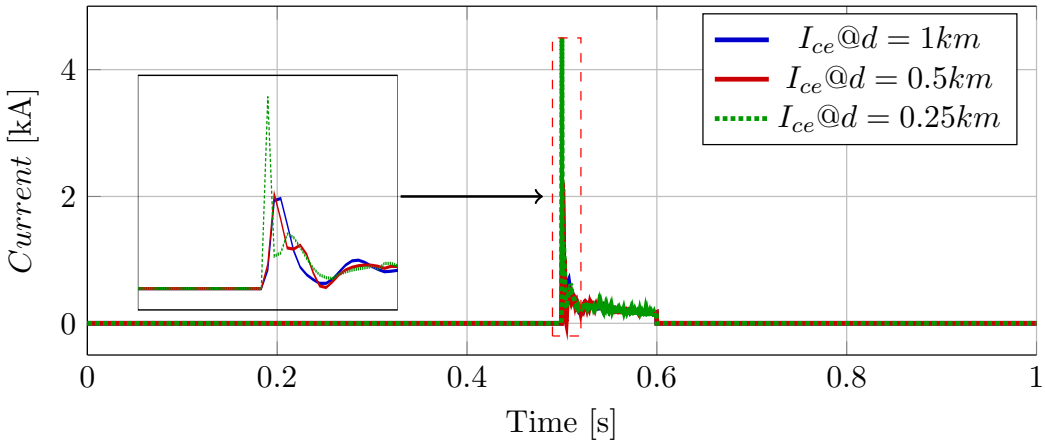

Figure 3.25: Pole-to-earth fault system responds with capacitor earthing

capacitor can be used as a passive element to earth the LVDC microgrid network. The capacitor will generate a large initial short circuit current during a pole-to-earth fault but will produce no short circuit current in the steady state (i.e. DC earth current is minimised and no corrosion will develop). In comparison to high resistance earthing method, the advantage of capacitor earthing method is that the earth fault can be detected and located by measuring the fault current flow through the capcitor earthing

when the faut occurs. Three distinct pole-to-earth faults are initiated at t= 0.5 s with different locations at the beginning, middle, and end of the LVDC microgrid network's main feeder in order to analyse the system's response to this earthing method at various fault locations. As illustrated in Figure 3.25, when the fault is initiated, the capacitor within the earth path immediately generates a large transient current. Additionally, the location of the fault in relation to the capacitor earthing has a direct effect on the magnitudes of transient fault currents. However, this method does not maintain the fault current for an extended period of time because it is instantaneous, making it difficult for protection devices to operate fast. The advantage of using capacitor earthing is that an earth fault can be detected and located by measuring the fault current flowing through the capacitor earthing when the fault occurs. However, because it is instantaneous, this method does not allow the fault current to be maintained for an extended period of time, making it difficult for protection devices to respond quickly.

Case IV: negative pole is earthed through capacitor in parallel with diode
In comparison to the previous case (Case III), the advantage of using a capacitor in parallel with a diode for DC earthing is that the flow of DC earth current can be restricted during steady state conditions, thereby preventing corrosion and providing a persistent signal for fault detection and location. When a pole-to-earth fault is initiated

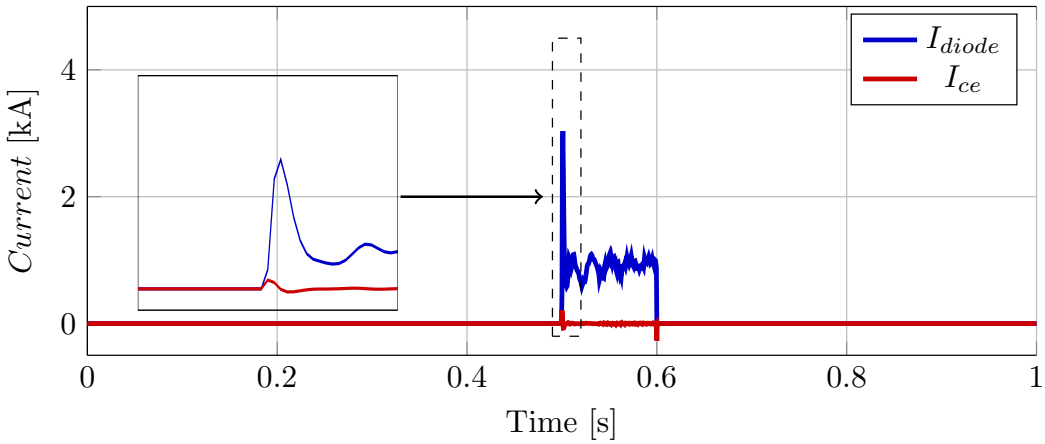

Figure 3.26: Pole-to-earth fault system responds with capacitor connected in parallel with diode earthing

at the LVDC microgrid's main feeder at t= 0.5 s, the earthing capacitor provides the initial fault current path until the voltage across its terminal reaches a level sufficient to cause the parallel diode to conduct, as illustrated in Figure 3.26. It can be concluded that this method is capable of reducing stray current(corrosion) and facilitating the detection of pole-to-earth faults.

3.5 Discussion of simulation results

The simulation results indicate that when a DC pole-to-earth fault occurs in a solidly earthed network, the voltage drops to zero, resulting in service interruption. Additionally, the solid earthing configuration provides a path for a large discharge current of the DC link capacitor, which is approximately 1.7 kA in this case. Thereby, fast acting circuit breakers are recommended with a time scale of 1.5 millisecond to disconnect the faulted cable as soon as the fault is detected to protect the system from overcurrent. On the other hand, the advantage of a high resistance earthing scheme is that no fault current circulates in the network during a single pole-to-earth fault, allowing the system to continue operating. However, fault-clearing action is required because a second fault will result in the formation of a double pole-to-earth connection, which can result in extremely high current. An insulation monitoring device is required for this type of earthing in order to detect the first fault. This results in an increase in the system's cost. Both configurations are incapable of providing a sufficient level to prevent corrosion, and thus a reconfigurablel earthing method is required, such as capacitor earthing or capacitor connection in parallel with the diode earthing. Using these methods, the earthing connection can be changed from high to low impedance depending on the state of the system. The advantage of using capacitor earthing is that the earth fault can be detected and located by monitoring the fault current flowing through the capacitor earthing when the fault occurs. However, because this method is instantaneous, it prevents the fault current from being maintained for an extended period of time, making it difficult for protection devices to respond fast. Whereas the benefit of using a capacitor in parallel with a diode for DC earthing is that the flow of DC earth current can be limited during steady state conditions, preventing corrosion and providing a persistent signal for fault detection and location. Table 3.3 illustrates a comparison between the different earthing schemes scrutinized in this chapter.

Table 3.3: Comparison between different earthing methods.

System earthing method	**Fault current level**	**Stray current level**	**Fault detection and location**
Solidly earthed	High	High	Easy/Difficult
High resistance earthed	Low	Moderate	Difficult/not-feasible
Capacitor earthed	High	Moderate Low	Moderate/feasible
Capacitor and diode earthed	High	Low	Easy/feasible

3.6 Fault characteristics analysis in an LVDC microgrid with a variety of converter topologies

When a fault occurs in a DC network where power converters are used to interface sources to the LVDC microgrid, it results in large currents flowing through the network. This is caused by the converter's dc-link capacitors being discharged. Those converters that have the ability to control the output current can limit the current level caused by a fault condition. These converters participate in the protection design process and work in conjunction with protective devices such as relays, fuses, and circuit breakers. Those converter topologies, on the other hand, that are unable to limit the output current are at risk of failing quickly. As a result, it is necessary to analyse the DC system during a fault in order to calculate critical parameters such as peak current and critical clearing time. The LVDC microgrid's control system should be operated either connected to or islanded from the main grid [189]. Much research has concentrated on the design of existing controllers and operational strategies that enable converters to switch between grid-connected and islanded modes [190, 191], with little understanding of the effects of this transition under faulted conditions. Besides that, earthing the network with a single earthing point is ineffective because when an islanded event occurs, this earthing point will be lost, and the network becomes unearthed (IT system), posing a risk to people and equipment. Having the network floating under the islanded mode, the fault current may be undetectable by conventional protection devices, posing a serious risk of protection failure. Therefore, to ensure that the entire DC system is always earthed, islanded network should have all DC sources earthed. Multiple earthing points (capacitors connected in parallel with diodes) are proposed in this chapter for earthing the LVDC microgrid in order to facilitate the detection of pole-to-earth faults, particularly in the islanded mode, and to reduce DC leakage current during normal operation. Finally, with the aim of developing protection and fault location schemes (one of the primary objectives of this thesis), the following section investigated the fault characterisation in relation to converter topology, fault type, and operating conditions by utilising multiple earthing points.

3.6.1 Fault analysis through the use of multiple earthing points

The fault characteristics of an LVDC microgrid are analysed in this subsection to determine the current trends within the network and to gain insight into the protection requirements of an LVDC microgrid with multiple earthing points. To analyse the fault characteristics of an LVDC microgrid system, consider the previous network depicted in Figure 3.22, but adding an energy storage connected to the DC bus to enable opera-

tion in an islanded mode. Pole-to-pole and pole-to-earth faults are two types of faults that can occur in an LVDC microgrid. These faults can occur in a variety of locations, including the DC bus, converters, DG sources, and load branches [176, 192]. The most frequent fault type in a distribution network is a pole-to-earth fault [193]. Typically, pole-to-pole faults have a low impedance, whereas pole-to-earth faults can have a low or high impedance. These faults have a detrimental effect on the entire network, particularly on power electronic converters and DG sources units [192]. Additionally, fault resistance Rf, earthing configurations, DG interface converters, type of DG source, and microgrid operation modes all have an effect on fault characteristics [75, 176, 194]. This section analyses the transient and steady-state fault characteristics of an LVDC microgrid during the most common faults, pole-to-earth faults, in various operation modes utilising multiple earthing points. These fault characteristics are essential when developing schemes for fault detection, localization, and protection [62, 75, 192].

3.6.2 Modelling

To analyse the fault characteristics of LVDC microgrids under various fault conditions with multiple earthing points, the previous model of LVDC microgrid was modified by adding a battery energy storage system (BESS) and connecting it to the DC point of common coupling (PCC) (refer to Figure 3.27), in order to maintain a 750Vdc voltage at the PCC and to enable stable operation of the DC microgrid in both grid-connected and islanded modes [152]. Multiple earthing points (a capacitor conncted in parallel with a diode) are used to facilitate the detection of an earth fault and to ensure personal safety while in islanded mode. However, one must keep in mind that the larger the network, the more earthing capacitor schemes are required to be connected. This will increase the cost of the solutions, but it will ensure that selectivity (discrimination) between protection devices is achieved in both connected and islanded modes. The equivalent circuit of a LVDC microgrid with multiple earthing points is illustrated in Figure 3.28 when a DC pole-to-earth fault occurs.

3.6.3 Simulation results

This section investigates the fault characteristics of the test LVDC microgrid network using multiple earthing points through simulation studies. The simulation studies consider both connected and islanded operation modes for the LVDC microgrid. At $t =$ 1.5 s, DC pole-to-earth faults are initiated with a fault resistance of 0.01 Ω at various locations (shown as location 1-2 in Figure 3.27) and no protection actions are implemented. The first DC pole-to-earth fault is initiated at the beginning of DC bus A in location 1, whereas the second fault is initiated at the end of the LVDC microgrid

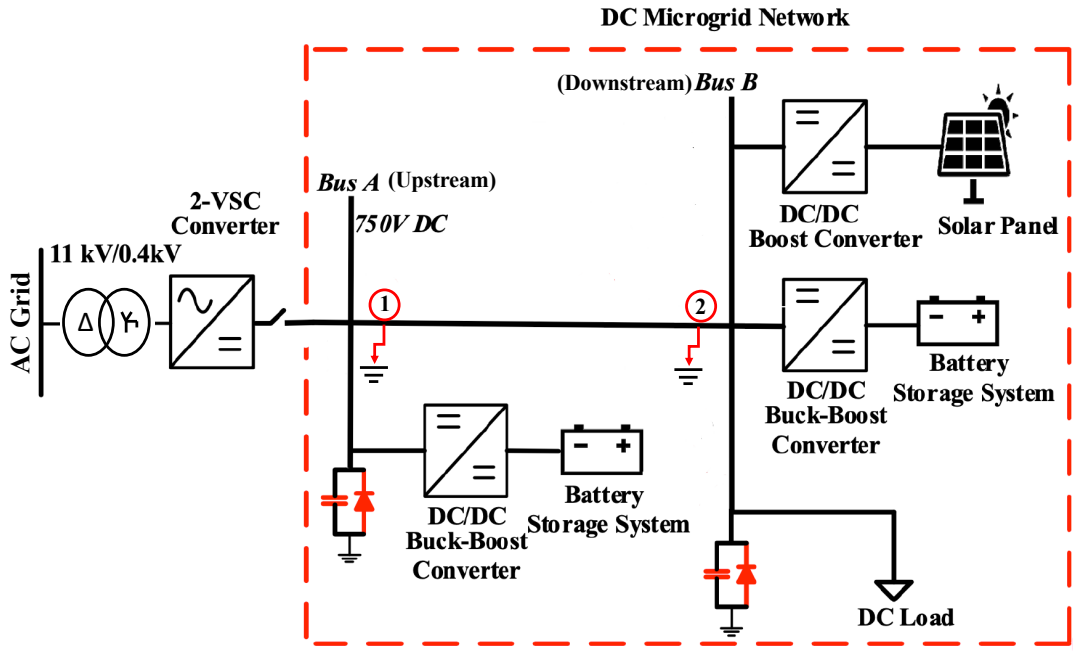

Figure 3.27: DC microgrid test network with multiple earthing capacitors.

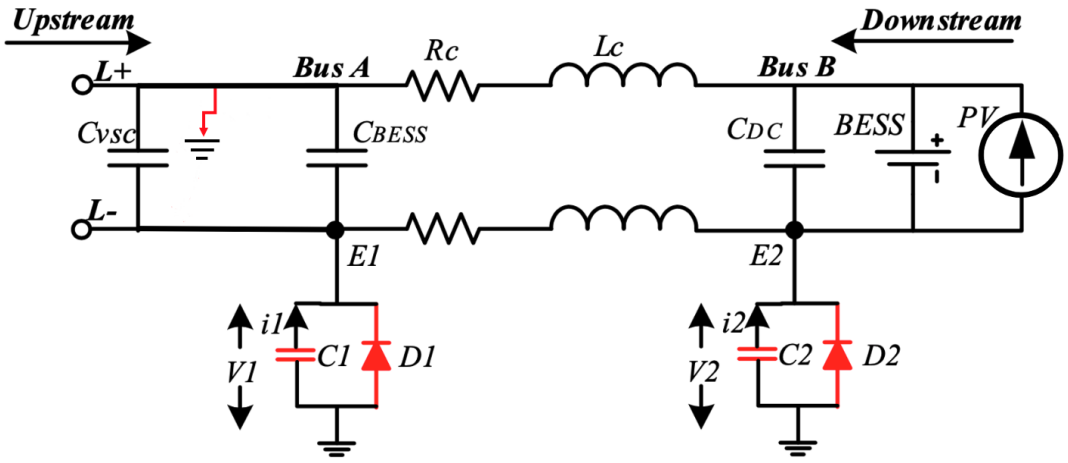

Figure 3.28: Equivalent circuit of DC microgrid network under pole-to-earth fault.

network's main feeder in location 2. The current signals are measured at the upstream and downstream, as well as at the earthing points of both capacitors.

LVDC microgrid is connected to the main grid

Fault applied at location 1: In this case, a positive DC pole-to-earth fault occurs at the start of DC bus A, resulting in transient discharge currents provided by the associated capacitors ($CVSC$, $CBESS$, and CDC). This transient current discharge

behaves similarly in the presence of a pole-to-pole fault, as an earth fault effectively creates a pole-to-pole fault. The fault current transient measured upstream is approximately 2kA, while the fault current transient measured downstream is approximately 0.5kA as illustrated in Figure 3.29(a). The earthing diodes $D1$ and $D2$ of the earth points $E1$ and $E2$ are forward biassed, resulting in the charge of the earthing capacitors $C1$ with a transient current peak of 0.35kA and $C2$ with a transient current peak of 0.14kA, as illustrated in Figure 3.29(b). While both earthing capacitors are triggered when a fault occurs, their transient circulation currents are quite different. This is due to the fact that their pre-fault voltages differ due to their location within the LVDC microgrid network.

Fault applied at location 2: In this case, a positive DC pole-to-earth fault is initiated at the end of the LVDC microgrid network's main feeder, resulting in transient discharge currents supplied by the associated capacitors ($CVSC$, $CBESS$, and CDC). The difference between this case and the previous one is that the charging current of the earthing capacitors $C2$ is much higher, with a transient current peak of 0.35kA, while $C1$ has a transient current peak of 0.14kA, because the fault is located near the second earthing point and the feeder's inductance is shorter than the value of the feeder's inductance for the first earthing point, as illustrated in Figure 3.29(b).

LVDC microgrid in an Islanded mode

Fault applied at location 1: During islanded mode, the primary VSC converter is disconnected from the LVDC microgrid and the network is supplied by the energy storage system.When a DC positive pole-to-earth fault is initiated, the transient current discharged is primarily from the $BESS$ filter capacitor ($CBESS$), with an upstream contribution of approximately 1.3 kA and a downstream contribution of approximately 0.6 kA as illustrated in Figure 3.30(a). The simulation results clearly demonstrate that the fault current level is lower in islanded mode than in grid connected mode, implying that it may be difficult to select a single threshold setting for protection devices operating in different operation modes. The earthing diodes $D1$ and $D2$ at the earth points $E1$ and $E2$ are forward biassed, resulting in a charge of the earthing capacitors $C1$ with a transient current peak of 0.35kA and $C2$ with a transient current peak of 0.14kA, as illustrated in Figure 3.30(b).

Fault applied at location 2:

A positive DC pole-to-earth fault is initiated at the end of the LVDC microgrid network's main feeder in this case, resulting in transient discharge currents supplied by the associated BESS capacitor $CBESS$ and downstream fault current contributions from the PV and storage unit as described previously. The diode $D2$ connected to the

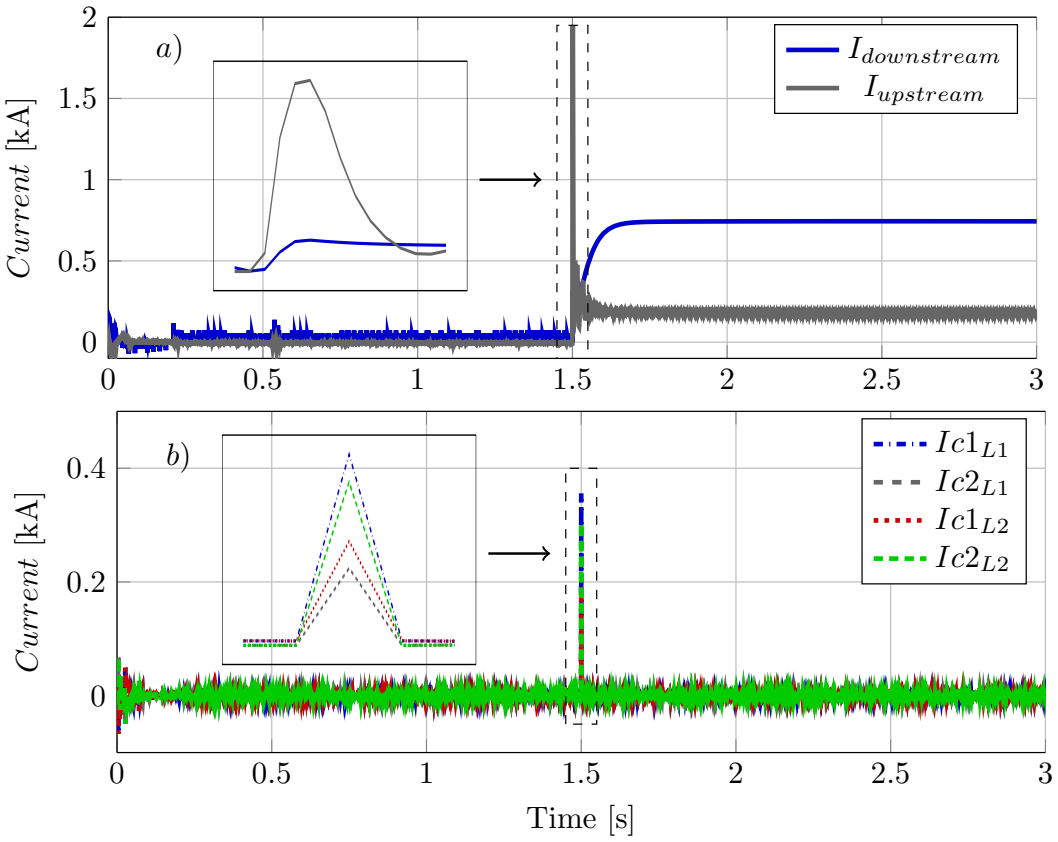

Figure 3.29: Pole-to-earth fault response at locations 1 and 2, (a) Upstream and downstream DC currents at location 1 (b) Current profiles of the earthing capacitors C1 and C2.

earthing point $E2$ establishes an earth path between the earthing points $E1$ and $E2$, allowing the capacitor earthing $C2$ to circulate a transient current with a peak value of 0.4kA, as indicated by the transient current $IC2_{L2}$ in Figure 3.30(b). Whereas the diode $D1$ connected to the earthing point $E1$ causes $C1$ to charge at a lower fault current (0.2kA), as illustrated in Figure 3.30(b). This is due to the equivalent fault impedance within the earth path.

3.7 Discussion of simulation results

The simulation results indicate that when a DC pole-to-earth fault occurs at locations 1 and 2 when the LVDC microgrid is connected to the main grid, a significant transient current rise results from discharging the VSC converter's DC link capacitor as well as the fault current contribution feeding to the fault point from the converters on the downstream side. This is because these converters interface with the DG units lack the

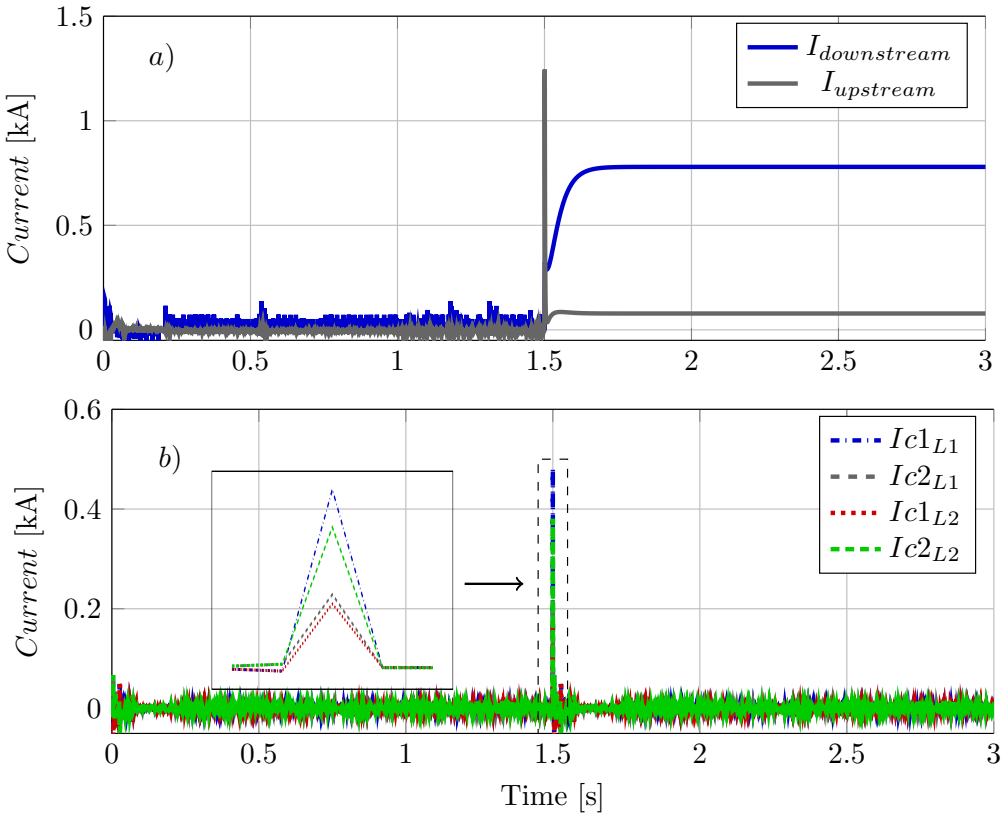

Figure 3.30: Pole-to-earth fault system response at locations 1 and 2, (a) Upstream and downstream DC currents at location 1 (b) Current profiles of the earthing capacitors C1 and C2.

capability to limit the output fault current. On the other hand, when a DC pole-to-earth fault occurs at locations 1 and 2 when the LVDC microgrid is disconnected from the main grid, the transient fault current is reduced compared to the grid connected case, implying that it is difficult to select a single overcurrent protection threshold that will operate in both operation modes. As a result, it is vital to develop a protection scheme that is capable of effectively protecting both people and equipment during various LVDC microgrid operation modes. The advantages of utilising multiple earthing points are that the network remains earthed through the earthing points during islanding mode, posing no risk to people if a fault occurs during islanding mode. Additionally, by utilising multiple earthing points, the need for galvanic isolation is eliminated, as there is no DC current flowing between the earthing points under normal operating conditions. Finally by measuring the initial current signal from each capacitor earthing, it is possible to detect the pole-to-earth fault as well as localise it by determining whether the fault is close to the DC bus or far from the protection devices. The benefit of performing these measurements locally is that it can eliminate the need for communication between protection devices.

3.8 Chapter 3 summary

This chapter provides an overview of the various earthing methods (i.e., earthing configurations and earthing devices) that are applicable to LVDC microgrids. Additionally investigate the effects of earthing methods on pole-to-earth fault currents, leakage currents, and personal and equipment safety, as well as evaluate and provide a comprehensive review of the benefits and drawbacks of LVDC microgrid earthing configurations. The system response of an LVDC microgrid network connected with a variety of earthing devices to a pole to earth fault is investigated using detailed simulations of an LVDC network modelled in the PSCAD software. The findings of the study indicate that, unipolar solid earthed systems generate a significant amount of fault current, necessitating rapid fault detection and isolation. Additionally, an earthed unipolar high-resistance system generates a small fault current from the first pole-to-earth fault. The system can continue to operate in this case. However, fault clearing action is required to prevent the formation of a second fault, which will result in a pole-to-pole fault with a significantly large fault current. As a result, this type of earthing scheme requires insulation monitoring devices. Finally, earthing LVDC microgrids via a capacitor connected in parallel with the diodes is the optimal configuration. This is because the capacitor prevents DC earth current from circulating during normal operation (thus reducing corrosion) and has a low impedance when a transient fault occurs (i.e. the voltage across the diodes exceeds some threshold value). These findings are recognized as a necessary first step toward developing protection methods that incorporate appropriate earthing schemes to ensure the safe and secure operation of LVDC microgrids. To address the difficulties associated with the system being un-earthed during islanded modes, this chapter has discussed the use of multiple earthing points to detect DC faults and ensure public safety. On this basis, a detailed fault characterisation was performed for LVDC microgrids operating in grid-connected and islanded modes using multiple earthing points (capacitor connceted in parallel with diode). From the study concluded that when the LVDC microgrid is disconnected from the main grid, the fault current level decreases, resulting in an insufficient fault current to trigger the protection device. As a result, protecting an LVDC microgrid in islanded mode from faulted conditions using a single protection relay setting is inadequate. Additionally, by measuring the initial current signal from each capacitor earthing, it is possible to detect and localise pole-to-earth faults by determining whether they are close to the DC bus or far away from the protection devices, which is a significant advantage when developing fault location and protection schemes.

Chapter 4

A Novel Fault Location Method based on Capacitive Earthing with Enhanced Accuracy

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4.1 Introduction

The network of LVDC microgrids is typically comprised of a number of converters and energy storage units. However, once a DC fault occurs on a DC line, each unit injects energy into the fault point, resulting in a large fault inrush current and a severe impact on the DC grid's safe operation. Thus, accurate knowledge of the faulted line is one of the key elements in facilitating quick maintenance, rapid restoration, and reduction of the outage duration, all of which contribute to enhancing the availability and reliability of the system as a whole [60, 195]. The most of existing offline fault location methods rely on additional hardware that is connected to the network to locate a fault (i.e. after protection operates [196]). These methods, however, require isolating the faulty section first to avoid interference between the external device and the grid power supply, which is time consuming and necessitates relocation of external equipment by a repair crew [197]. Apart from offline fault location methods, a few online fault location methods (i.e. the method operates during the fault period) have been proposed in [198, 199]. These methods, however, implicitly assume that the remote end converter is uniform to the main converter. This is less likely to happen in LVDC microgrids due to the presence of varying amounts of renewable energy and end-user devices. Whereas others rely on communication between the converters, implying a reliability issue if the communication channel is lost.

Therefore, this chapter develops a mathematical model to describe the fault response with capacitive earthing during the transient period of DC faults and analyses the influence of remote converters on the accuracy of fault location. On the basis of this analysis, two novel methods for locating faults along feeders in an LVDC microgrid that employs a capacitive earthing scheme are proposed. Capacitors within the earthing scheme are charged during fault conditions by transient currents proportional to the fault distance and resistance. Thus, the distance to the fault is estimated by observing the capacitive earthing scheme's response during the fault. The proposed methods make use of instantaneous current and voltage measurements (taken at the feeder terminals and earthing capacitors) in conjunction with an analytical mathematical model of the faulted feeder. These proposed methods have been evaluated for their accuracy in locating the fault position along the faulted feeder, as well as for their performance under a variety of loading scenarios and highly resistive faults. Additionally, the proposed method with optimization technique's performance and practical feasibility have been experimentally validated through the development of a low-voltage laboratory prototype.

4.2 Review and limitations of existing fault location methods

As previously outlined in section 2.5.3, existing fault location methods can be classified into two board categories active and passive. Active methods are based on the injection of signals into the faulted feeder (typically through the use of auxiliary equipment), followed by the analysis of the reflected signatures. Unlike active fault location methods, passive fault location methods rely solely on the collection and analysis of measurements (which can be local or remote). Additionally, fault location methods can be classified as offline methods, which calculate the distance to the fault after it has been cleared, or online methods, which calculate the distance to the fault as it develops.

In the [200] the authors propose an active fault location method in which the fault is located by injecting a DC voltage into the faulty feeder. The method employs a probe unit and an RLC circuit model to extract both the oscillation frequency and attenuation coefficient, allowing for the estimation of the distance to the fault. This method has been enhanced by the work described in [201, 202] by taking into account the effect of the attenuation coefficient on the accuracy of the fault location calculations. In the [203, 204], methods for passive fault location based on single-ended travelling waves are proposed. Despite the fact that travelling waves have been widely used for fault location on transmission-level applications (i.e. on high voltage DC grids with

long transmission lines [205]), their application in LVDC microgrids can be challenging due to the small surge reflection time, which can degrade the reliability and accuracy of the estimation [206].

In the [207], the authors have proposed a differential, current-based fast detection and fault location method. The method is non-iterative and employs a cumulative sum average approach. It is based on current measurements taken from both ends of the faulted feeder. Communication-based methods are associated with increased costs for the communication infrastructure as well as concerns about reliability in the event of a communication link failure. An approach is proposed in [208] that makes use of the least square method and boundary inductance as a way to eliminate the need for communication requirements. This method, on the other hand, takes a long time to detect and locate a fault. Other methods for locating faults are described in [209, 210], which make use of local voltage and current measurements. These methods, however, have not taken into account the influence of remote fault current contributions, which are dependent on the fault resistance and distance between the faults and are relatively difficult to predict [182]. To address the aforementioned issues, this chapter proposes passive and communication-less fault location methods that are applicable to any type of feeder termination and support both passive connections and converter-interfaced loads and sources equipped with DC-link capacitors.

The following section will discuss the two proposed methods, the first of which involves estimating the inductance value between the capacitor earthing and the fault utilising moving average and Savitzky-Golay filters. The second proposed method utilised multiple capacitive earthing schemes to determine the fault location along the feeder.

4.3 Single capacitive earthing scheme based fault locator for LVDC microgrids

The proposed fault location method is based on two key aspects: calculating the inductance value (the distance between the capacitor earthing and the fault) and smoothing and differentiating the noisy signal obtained from the measurement devices using moving average and Savitzky-Golay filters. When a DC fault occurs, the capacitor earthing within the earth path begins charging a transient current. This charge current does not increase instantly; rather, it increases at a rate determined by the voltage across the capacitor earthing and the fault path inductance. With knowledge of the cable's inductance per unit length (mH/km), the distance between the capacitor earthing and the fault location can be calculated using the equation in (4.7). Once the value of

di/dt is determined, the inductance L can be calculated as well. The Moore-Penrose pseudo inverse technique [211] is used to estimate the inductance between the capacitor earthing and the fault, which allows for more accurate estimation of the inductance between the capacitor earthing and the fault. This technique is derived from the least squares solution of a system of linear equations that does not have a unique solution. It produces more accurate results for estimating the fault location than conventional iterative fault location estimators, which require a number of samples (i.e. local voltage and current measurements) prior to calculation. Usually current and voltage measurements extracted from events recorded by relays or monitoring devices; the accuracy of these devices is critical because it can affect the fault location estimation. Therefore, filters and smoothers such as moving average and Savitzky-Golay filters are proposed during the estimation process to not only reduce noise, but also to sustain the shape and height of the waveform peaks. The following subsections discusse how moving average and Savitzky-Golay filters are implemented for fault distance estimation.

Moving average smoothing filter

The most frequently used filter for analysing a random noise signal is an online moving average filter. A moving average filter performs by averaging a set of data points from the input signal to produce each point in the output signal, as outlined in (4.1) [212]. This operation is repeated with a window length of M points (the average's number of points) to calculate the data set's average.

$$y[n] = \frac{1}{M} \sum_{j=0}^{M-1} x[n-j] \tag{4.1}$$

To obtain di/dt, a numerical differential operator is used in conjunction with a moving average filter. The current derivative is obtained using a first-order approximation method similar to that described in (4.2).

$$\frac{di_k}{dt} = \frac{i(k) - i(k-1)}{T} \tag{4.2}$$

Where $\frac{di_k}{dt}$ is the current derivative at interval k , $i(k)$ is the measured current at interval k and T is the sampling period.

Savitzky-Golay smoothing filter

The Savitzky-Golay filter is a technique for smoothing and differentiating noisy data obtained from measurement devices. It is based on a local least squares polynomial approximation[213]. To sample the area around the centre of the data point, a window

with a length of $N = 2M + 1$ samples is employed. As in (4.3) and (4.4), the samples within the window are fitted with a polynomial of order p in order to minimise the mean squared error.

$$\epsilon_n = \sum_{i=-M}^{M} (q(i) - x(i))^2 \tag{4.3}$$

$$q(i) = \sum_{k=0}^{p} a_k.i^k \tag{4.4}$$

Where p = polynomial order, k = (0,....,n) and a_k is k^{th} coefficient of polynomial.

A polynomial coefficient vector $a = [a_0, a_1, a_2, ...a_n]^T$, input samples vector $x = [x_{-M}, ...x_{-1}, x_0, x_1....., x_M]^T$, and for $p < 2M+1$, the coefficient a can be obtained:

$$a = (A^T.A)^{-1}.A^T.x = H.x \tag{4.5}$$

$$\text{where } A^T = \begin{bmatrix} (-M)^0 & \cdots & (-1)^0 & 1 & 1^0 & \cdots & M^0 \\ (-M)^1 & \cdots & (-1)^1 & 0 & 1^1 & \cdots & M^1 \\ (-M)^2 & \cdots & (-1)^2 & 0 & 1^2 & \cdots & M^2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ (-M)^N & \cdots & (-1)^N & 0 & 1^N & \cdots & M^N \end{bmatrix} \tag{4.6}$$

The coefficient a denotes the smooth value of x at $M = 0$. The Savitzky-Golay filter has an interesting property in that it can be used to obtain a smoothed version of the derivative of $x(i)$. This can be attained by multiplying the first row of the matrix H by the vector of samples x in order to obtain the coefficient a_1 and thus the value of di/dt.

4.4 The Proposed Fault Location Estimation Concept

4.4.1 A mathematical model for estimating the equivalent inductance of a faulted feeder

Figure 4.1 depicts a simplified DC circuit consisting of a DC feeder connected to a DC source and a DC load, with the circuit's negative pole connected to the earth through a diode in parallel with a capacitor. The state space equation for this circuit is written as:

$$V_{dc} + V_{ce} = L_H \frac{\mathrm{d}i_{ce}}{\mathrm{d}t} + (R_H + R_f) i_{ce} \tag{4.7}$$

Where V_{dc} is the DC current input voltage, V_{ce} is the voltage across the capacitor earthing, and I_{Ce} is the current flowing through the capacitor earthing instantaneously. The resistance and inductance of the positive pole are denoted by R_H and L_H, respectively, while the resistance and inductance of the negative pole are denoted by R_L and L_L. The capacitor earthing point and the fault resistance are denoted by C_e and R_f, respectively.

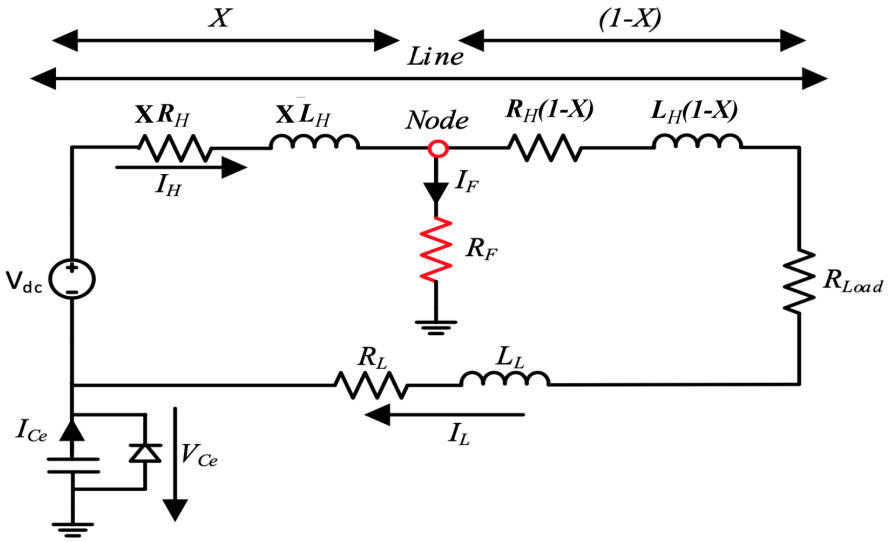

Figure 4.1: A faulted DC feeder with positive earth fault condition

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During a pole-to-earth fault the capacitor earthing acts as a low resistance path, and thus the capacitor earthing charging current flows through the diode and R_f. The charge current in a capacitor is proportional to its capacitive impedance. This means that as the cable length increases, the peak charging current decreases and the charging period increases. The capacitor's earthing voltage, current, and current derivative are sampled at different time steps, whereas $(R + R_f)$ and L can be estimated using the least squares method from data sampled at multiple time instants. The differential equation in (4.7) can be rewritten in matrix form as follows in terms of the number of measurement samples, N:

$$B = A \begin{bmatrix} L \\ \\ R + Rf \end{bmatrix} \tag{4.8}$$

$$A = \begin{bmatrix} \frac{\mathrm{d}i_{ce}}{\mathrm{d}t}(0) & \frac{\mathrm{d}i_{ce}}{\mathrm{d}t}(0) \\ \vdots & \vdots \\ \vdots & \vdots \\ \frac{\mathrm{d}i_{ce}}{\mathrm{d}t}(N) & \frac{\mathrm{d}i_{ce}}{\mathrm{d}t}(N) \end{bmatrix} B = \begin{bmatrix} V_{dc} + V_{ce}(0) \\ \vdots \\ \vdots \\ V_{dc} + V_{ce}(N) \end{bmatrix} \tag{4.9}$$

The unknown resistance, R, and inductance, L, are calculated by the pseudo inverse technique as in (4.10)

$$\begin{bmatrix} L \\ R + Rf \end{bmatrix} = (A^T.A)^{-1}.A^T.B \tag{4.10}$$

4.4.2 The proposed approach for estimating the equivalent inductance of a faulted feeder

Based on the previous analysis, a novel fault location technique is proposed that utilises the least squares method to estimate the inductance value between the earthing capacitor and the fault in combination with moving average and Savitzky-Golay filters. In radial DC systems, the inductance value is estimated by measuring the voltage, current, and di/dt values during the transient stage. This proposed method is based on the establishment of a linear relationship between di/dt and the fault loop impedance. As a result, the fault inductance between the protective device and the fault point is estimated using these measured values. When a fault occurs, the earthing capacitor begins charging; the transient voltage, current, and di/dt signals are determined locally based on the charging time prior to the fault current being limited. Then, based on the measured signals, the equivalent fault inductance between the local protective device and the fault is estimated. To increase the accuracy of the estimation, moving average and Savitzky-Golay filters are used to determine the equivalent inductance. The following stages comprise the proposed method for locating faults using a single capacitive earthing scheme:

Stage I- Once an overcurrent protection device detects a fault, the voltage and current of the earthing capacitor are captured and sampled at each time step.

Stage II- Once the earthing capacitor current signal measurement is available, the current derivative is then calculated and filtered using moving average and Savitzky-Golay filters.

Stage III- Following that, the corresponding inductance value between the capacitor earthing and the fault point is estimated using the least squares method.

4.5 Validation of the fault location estimation using the least squares method

The proposed method is validated using an LVDC microgrid test network. Numerous fault scenarios are considered to demonstrate the effectiveness of the proposed fault location technique. The accuracy of the fault location estimation is determined by applying faults with varying fault resistance values (0.1Ω, 0.5Ω, 1Ω, 1.5Ω, and 2Ω) along a 1000m feeder. Typically in LVDC microgrids fault resistance would vary from solid to 10 Ω [214, 215, 216, 217], while 2 Ω has been conceived as high-resistance fault and 10 Ω is classed as a very high-resistance fault [218]. For this purpose, a pole-to-earth fault with fault resistance of 2 Ω is simulated in this study along with an ideal ground. The faults are applied along the feeder at intervals of 100m between each fault. Then, a comparison of estimating the inductance-based fault location method using the moving average, Savitzky-Golay filters, and initial di/dt calculation method is performed. The proposed fault location method is evaluated using relative errors calculated from MATLAB/Simulink simulations under various fault conditions. The following equation is being used to describe the error in determining the location of the fault:

$$\varepsilon(\%) = \frac{L_{cal} - L_{act}}{L_{act}}.100\% \tag{4.11}$$

where ε is the relative error in percentage, L_{act} is the actual inductance, L_{cal} is the calculated inductance.

4.5.1 LVDC microgrid test network

An LVDC microgrid network is developed as depicted in Figure 4.2. The DC network is connected to the AC grid through a two-level voltage source converter and transformer. The VSC provides 0.35kV DC pole-to-pole voltage at the point of common coupling (PCC). The LVDC feeder is modelled as an equivalent R-L circuit with 1000m long. A DC bus is connected to a lumped DC load. A capacitor's earthing point in parallel with a diode is used to detect earth faults and ensure personal safety. Using the equation (3.12) in Section 3.3.3 the size of the capacitor earthing is 3.7mF, the clamp voltage is defined based on the assumption that the biggest allowable deviation on the poles is 5% of the nominal voltage (i.e. 350 V), in this case, ± 17.5 V. The parameters of the LVDC microgrid test system are shown in Table 4.1

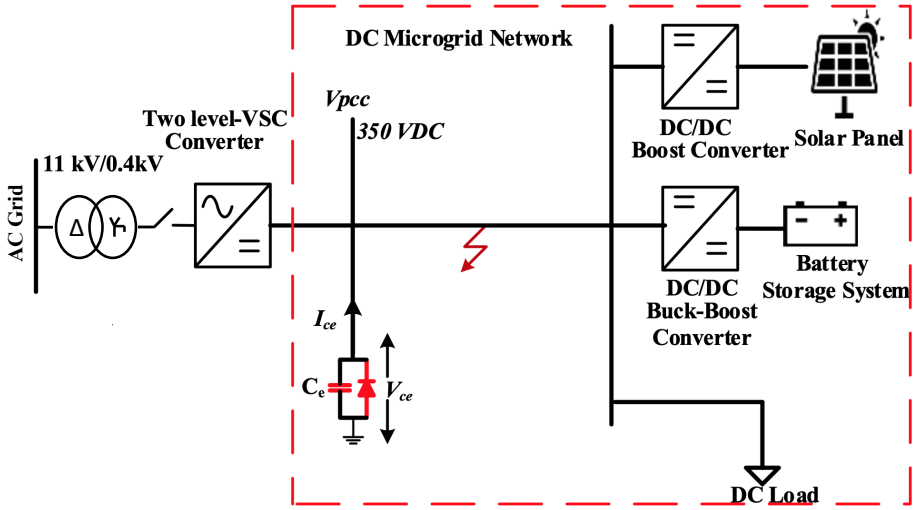


Figure 4.2: LVDC microgrid test network.

Table 4.1: AC and DC Network Parameters

Parameter	Value
AC grid Voltage [kV]	11
Transformer voltage ratio [kV]	11/0.4
DC voltage [V]	350
R, L of LVDC cable	0.0164 [Ω/km],0.14 [mH/km]
Earthing capacitor[mF]	3.7
Battery rating [kWh]	7.8
PV rating[kW]	10
DC load[kW]	5

4.5.2 Simulation results

In the simulation studies, DC pole-to-earth faults are applied along the 1km cable with 0.5Ω fault resistance intervals in the range from 0.1Ω to 2Ω. The proposed method is then implemented using a moving average filter and then a Savitzky-Golay filter, and the performance is compared to the initial di/dt measurement method proposed in [219].

Fault locations estimation with moving average filter

The Table 4.2 illustrates the relative errors associated with estimating fault distance using a moving average filter for a range of fault distances and resistances. Within 500 m for 0.1 Ω fault resistance, the estimation of the fault location has a relatively small error (1.4 m, 0.28 %, the fault applied at the middle of the feeder). When the fault is

moved beyond 500 metres, the error in locating the fault increases (up to 3m, 0.3 %, the fault applied at the end of the feeder). On the other hand, the fault location estimation has a relatively high error for the 2 Ω fault resistance 32 m, 6.52 %, for the fault applied in the middle of the feeder. This is because, when the earth fault resistance dominates the fault loop, the calculation errors for inductance increase dramatically.

Table 4.2: Percentage error in estimating the fault distance using a moving average filter.

Distance [km]	R_f=**0.1** Ω	R_f=**0.5** Ω	R_f=**1.0** Ω	R_f=**1.5** Ω	R_f=**2.0** Ω
0.5	0.28 %	1.5 %	3.18 %	4.8 %	6.52 %
0.6	0.26 %	1.53 %	3.13 %	4.78 %	6.46 %
0.7	0.25 %	1.51 %	3.12 %	4.77 %	6.42 %
0.8	0.25 %	1.42 %	3.13 %	4.7 %	6.35 %
0.9	0.25 %	1.53 %	3.15 %	4.77 %	6.4 %
1	0.3 %	1.6 %	3.2 %	4.8 %	6.4 %

Fault locations estimation with Savitzky-Golay filter

The Table 4.3 illustrates the relative errors associated with estimating fault distance using a Savitzky-Golay filter for a range of fault distances and resistances. Within 500 m for 0.1 Ω fault resistance, the estimation of the fault location has a relatively small error (1.5 m, 0.3 %, the fault applied at the middle of the feeder). When the fault is moved beyond 500 metres, the error in locating the fault increases (up to 3m, 0.3 %, the fault applied at the end of the feeder). On the other hand, the fault location estimation has a relatively high error for the 2 Ω fault resistance 36 m, 7.28 %, for the fault applied in the middle of the feeder.

Table 4.3: Percentage error in estimating the fault distance using Savitzky-Golay filter.

Distance [km]	R_f=**0.1** Ω	R_f=**0.5** Ω	R_f=**1.0** Ω	R_f=**1.5** Ω	R_f=**2.0** Ω
0.5	0.3 %	1.62 %	3.34 %	5.1 %	7.28 %
0.6	0.3 %	1.63 %	3.33 %	5.05 %	6.81 %
0.7	0.31 %	1.62 %	3.31 %	5.01 %	6.74 %
0.8	0.31 %	1.56 %	3.31 %	4.95 %	6.65 %
0.9	0.32 %	1.65 %	3.32 %	5 %	6.67 %
1	0.3 %	1.7 %	3.3 %	5 %	6.7 %

Fault locations estimation with initial di/dt measurement method

In this case, the actual inductance value is calculated using equation 4.7. The authors in [219] assumed that $i_{ce}(0)$ is negligible due to the low line resistance and initial current, and that L could be determined by measuring di_{ce}/dt and $V_{dc}(0) + V_{ce}(0)$. The Table 4.4 illustrates the relative errors associated with estimating fault distance using the initial di/dt measurement method proposed in [219] for a range of fault distances and resistances. Within 500 metres of 0.1 Ω fault resistance, the location of the fault is estimated with a significant error (43 m, 8.6 %, the fault applied at the middle of the feeder). When the fault is relocated beyond 500 metres, the error associated with fault location increases (up to 67m, 6.7 %, the fault applied at the end of the feeder). On the other hand, the estimation of the fault location has an extremely high error for the 2 Ω fault resistance (700 m, 140.8%, for the fault applied in the middle of the feeder), and the relative error increases significantly as the fault is moved away (315 m, 31.5%, for the fault applied at the end of the feeder).

Table 4.4: Percentage error in estimating the fault distance using initial di/dt measurment method.

Distance [km]	R_f=**0.1** Ω	R_f=**0.5** Ω	R_f=**1.0** Ω	R_f=**1.5** Ω	R_f=**2.0** Ω
0.5	8.6%	27.4 %	57.96 %	94.8 %	140.8 %
0.6	12.6 %	27.93 %	53.76 %	84 %	120.66 %
0.7	12.48 %	21.45 %	37.47 %	56.28 %	76.42 %
0.8	8.91 %	16.1 %	28.25 %	37.25 %	49 %
0.9	7.07 %	13.22 %	21.33 %	30.33 %	39.33 %
1	6.7 %	10 %	17.5 %	24.6 %	31.5 %

From the above analysis, it can be concluded that the proposed method, which employs the least squares method in conjunction with moving average and Savitzky-Golay filters, provides more accurate fault location estimation when compared to the initial di/dt measurement method. For example, when the fault resistance is 0.1 Ω, the estimation of the fault location has a relatively small error (1.5 m, 0.3 %, the fault applied at the middle of the feeder) when compared to the initial di/dt measurement method, which results in a significant error in estimating the fault location (43 m, 8.6 %, the fault applied at the middle of the feeder). In comparison to the results in Tables 4.2 and 4.3, the reduced fault estimation errors are primarily enhanced by combining the least squares method with a moving average and Savitzky-Golay filters. The comparison of the two methods demonstrates that the proposed method is significantly more reliable and accurate at varying fault distances and resistances. Additionally, because the

proposed technique is based on local measurements taken from the capacitor earthing, it enables accurate location of DC faults and enables rapid post-fault cable maintenance.

LVDC microgrids typically have multiple source-end power converters with cables feeding the DC loads. A single earthing point will not be enough if there are multiple decentralised sources in the system. Additionally, in the event of an islanding mode, if the system loses its main earthing point, the system becomes floating, posing a safety risk. As a result, multiple earthing are required in this case. In the following subsection, the concept of locating a fault in an LVDC microgrid using multiple capactive earthing schemes will be described.

4.6 Multiple capacitive earthing schemes based fault locator for LVDC systems

The proposed method determines the location and resistance of the fault along the feeder by capturing the current and voltage signals from the earthing capacitor connected at both ends of the feeder. The following section will discuss the mathematical analysis of a faulted feeder and describe the proposed algorithm for estimating the location of a fault on a feeder that is connected to DC loads and DC sources at the remote ends.

4.6.1 Description of a mathematical faulted feeder model

This section will present a mathematical analysis of the faulted feeder model when it is connected to DC loads and DC sources at both ends. The circuit's negative pole is earthed through a multiple capacitive earthing scheme. To begin developing the algorithm for fault location, an equivalent network of DC feeders with a DC source and a DC load is derived when the fault occurs at 50% of the feeder's length. The DC load is connected at the network's remote end. Following that, the same analysis is performed on an equivalent network of DC feeders with multiple DC sources connected at both terminals.

Faulted feeder model

The state space equations, which reflect the feeder terminal voltages under the influence of a pole-to-earth fault (as depicted in Fig.4.3), are written as:

$$V_{ce1} + V_{dc1} = L_1 \frac{\mathrm{d}}{\mathrm{d}t} i_1(t) + i_1 R_1 + (i_1 + i_{ce2}) R_f \tag{4.12}$$

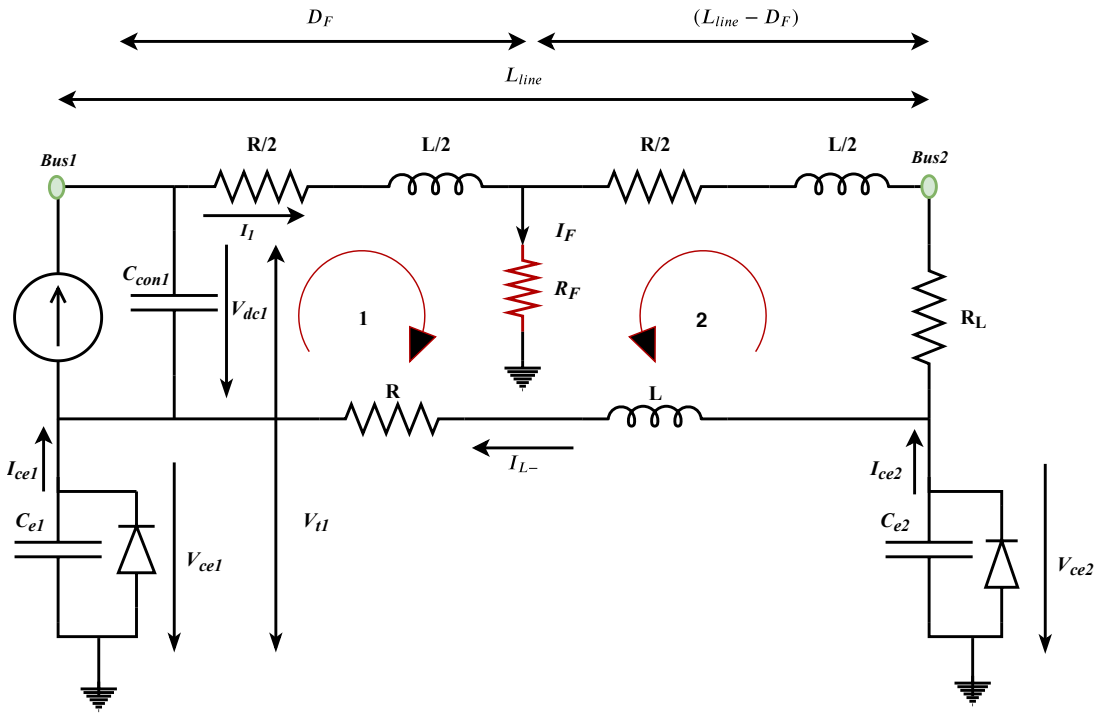


Figure 4.3: Equivalent network of DC feeder with DC source, load and multiple capacitive earthing scheme. Fault occurs at D_F=50% of the feeder's length in the shown case.

$$V_{ce2} = i_{ce2}\, R_L + (i_1 + i_{ce2})\, R_f + i_{ce2}\, (R_T - R_1) + \frac{\mathrm{d}}{\mathrm{dt}} i_{ce2}(t)(L_T - L_1) \tag{4.13}$$

where L_1, R_1 are the equivalent cable inductance and resistance up to the fault point (taking as reference Bus1), R_f is the fault resistance, L_T and R_T are the total inductance and resistance of the feeder, V_{dc1} is the voltage across the filtering capacitor at Bus1, V_{ce2} is the voltage across the earthing capacitor at Bus 2, i_1 is the line current from Bus1 and i_{ce2} is the earthing capacitor current at Bus2 during the fault. In the case of the pole-to-earth fault, the feeder parameters can be written in terms of the relative fault distance, m:

$$R_1 = mR_T, L_1 = mL_T \tag{4.14}$$

where m=D_F/L_{line} is the ratio between the actual fault distance and the total length of the feeder. Subtracting (4.13) from (4.12) and substituting L_1, R_1 and m from (4.14) gives:

$$\begin{aligned} V_{ce1} + V_{dc1} - V_{ce2} = mL_T \frac{\mathrm{d}}{\mathrm{d}t} i_1(t) + i_1\, mR_T - i_{ce2}\, R_L \\ -i_{ce2}\,(R_T - mR_T) - \frac{\mathrm{d}}{\mathrm{d}t} i_{ce2}(t)(L_T - mL_T) \end{aligned} \tag{4.15}$$

During the course of a fault, the earthing capacitors C_{e1} and C_{e2} are being charged by the fault current, which continues until voltage clamping is initiated. Meanwhile, filtering capacitors C_{con1} and C_{con2} are being discharged, contributing to the fault current. The current, i_{ce2}, flowing through the earthing capacitor, C_{e2}, during the fault transient is proportional to the voltage, V_{ce2}, as follows:

$$V_{ce2} = \frac{\int_0^t i_{ce2}\,\mathrm{d}t}{C_{e2}} \tag{4.16}$$

Substituting V_{ce2} from (4.16) in (4.15) gives:

$$\begin{aligned} V_{ce1} + V_{dc1} - \frac{\int_0^t i_{ce2}\,\mathrm{d}t}{C_{e2}} = mL_T \frac{\mathrm{d}}{\mathrm{d}t} i_1(t) + i_1\, mR_T - i_{ce2}\, R_L \\ -i_{ce2}\,(R_T - mR_T) - \frac{\mathrm{d}}{\mathrm{d}t} i_{ce2}(t)(L_T - mL_T) \end{aligned} \tag{4.17}$$

Rearranging equation (4.12) in terms of i_{ce2} and substituting the resulting relationship in (4.17) yields :

$$G_1\, m^2 + G_2\, m + G_3\, R_f + J = Y^* \tag{4.18}$$

where J is an integration constant and $G1$, $G2$, $G3$ and Y^* are coefficients, given by:

$$G_1 = {R_T}^2 i_1 + 2\, L_T R_T \frac{\mathrm{d}}{\mathrm{d}t} i_1 + {L_T}^2 \frac{\mathrm{d}^2 i_1}{\mathrm{d}t^2} \tag{4.19}$$

$$\begin{aligned} G_2 = & -{L_T}^2 \frac{\mathrm{d}^2 i_1}{\mathrm{d}t^2} - R_L\, L_T \frac{\mathrm{d}}{\mathrm{d}t} i_1 - 2\, L_T R_T \frac{\mathrm{d}}{\mathrm{d}t} i_1 \\ & - R_L\, R_T\, i_1 - {R_T}^2 i_1 - L_T \frac{\mathrm{d}}{\mathrm{d}t} V_{t1} \\ & - R_T\, V_{t1} + \frac{L_T \int_0^t i_1\,\mathrm{d}t}{C_{e2}} + \frac{R_T \int_0^t i_1\,\mathrm{d}t}{C_{e2}} \end{aligned} \tag{4.20}$$

$$G_3 = -L_T \frac{\mathrm{d}}{\mathrm{d}t} i_1 - R_L\, i_1 - R_T\, i_1 + \frac{\int_0^t i_1\,\mathrm{d}t}{C_{e2}} + V_{t1} \tag{4.21}$$

$$Y^* = -R_L\, V_{t1} - R_T\, V_{t1} \; - L_T \frac{\mathrm{d}}{\mathrm{d}t} V_{t1} - \frac{\int_0^t V_{t1}\,\mathrm{d}t}{C_{e_2}} \tag{4.22}$$

The proposed method employs equation (4.18) to determine the cable fault distance m

and the cable fault resistance R_f. At each time interval, the coefficients $G1$ to $G3$ and Y^* are calculated assuming a sampling time of Δt. Equation (4.18) in matrix form for various time instances is written as :

$$\begin{bmatrix} Y^*(t) \\ Y^*(t+\Delta(t)) \\ \vdots \\ Y^*(t+N\Delta(t)) \end{bmatrix} = \begin{bmatrix} m^2 & m & R_f \end{bmatrix} \begin{bmatrix} G1(t) & G2(t) & G3(t) \\ G1(t+\Delta(t)) & G2(t+\Delta(t)) & G3(t+\Delta(t)) \\ \vdots & \vdots & \vdots \\ G1(t+N\Delta(t)) & G2(t+N\Delta(t)) & G3(t+N\Delta(t)) \end{bmatrix} \tag{4.23}$$

where N is the number of samples available for analysis.

The estimated state is then expressed as a least squares optimisation problem by minimising the sum of the square errors (or residuals) between the prediction function Y and the calculated function, $Y*$, within the selected dataset.

Y which is obtained by multiplying the matrix $G1$-$G3$ by the initial estimation values X_0 of the fault distance m and the fault resistance R_f.

$$Obj = \sum \left(\frac{Y - Y^*}{Y^*} \right)^2 \tag{4.24}$$

In this case, the variables m and R_f are estimated using the non-linear programming function-fmincon. The fmincon function in MATLAB is a nonlinear interior point optimisation technique that starts at X_0 and attempts to find a minimiser X of the function described in Obj [220].

$$X_{(m,Rf)} = fmincon\,(Obj, X_0) \tag{4.25}$$

where X is a two-dimensional scalar containing estimates of both fault location and its fault resistance, Obj is the objective function, and X_0 is an initial guess value. The $fmincon$ function has been deployed from the MATLAB optimisation toolbox [221].

In the case of multiple DC power converters connected at both ends of the DC feeder as illustrated in Figure 4.4, a simplified model is developed to derive the approach. The fault current is supplied from both ends of the feeder due to the fact that these power electronic converters have capacitors on both sides, which contribute to the fault

currents at both ends of the cable. The following amendments apply to the equations (4.12) and (4.13):

- Replace $(V_{ce1} + V_{dc1})$ with V_{t2}
- i_{L1} becomes the total fault current flowing from Bus1
- i_{L2} becomes the total fault current flowing from Bus2

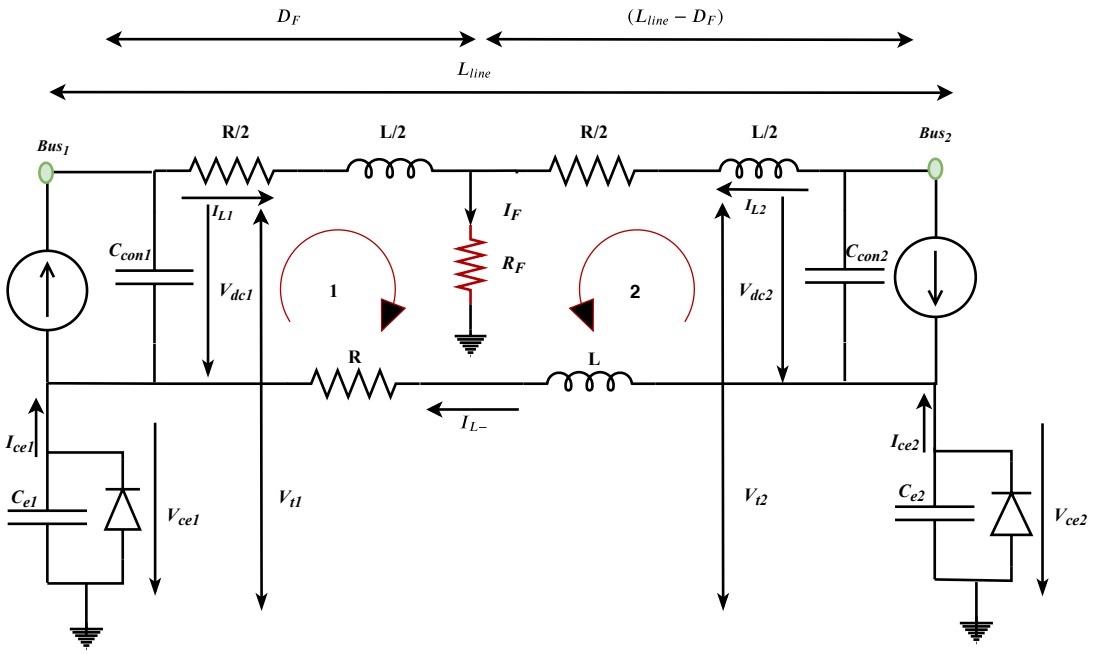


Figure 4.4: Equivalent network of DC feeder with DC sources at both terminals and multiple capacitive earthing scheme. Fault occurs at D_F=50% of the feeder's length.

4.6.2 Description of the fault location algorithm

The proposed fault location method consists of three main stages as depicted in Fig. 4.5 and is explained in detail as follows:

Stage I: Signal acquisition and coefficient calculation

At this stage, all necessary voltage and current signals are captured (voltage across the filtering and earthing capacitors, as well as the earthing capacitor current), and the corresponding coefficients (i.e. $G1$, $G2$, and $G3$) are calculated. When there is a fault on the feeder, the current flowing from the earthing capacitor to the fault point exceeds its normal zero current(th). Following that, the proposed fault location algorithm records the post-fault voltage and current traces associated with the earthing capacitor and

converter. At each time interval, Δt, the coefficients $G1$ to $G3$ and Y^* are calculated. For accurate calculation, the equation (4.23) is constructed using selected sets of ten sampling points ($N = 10$). The proposed method considers a signal sampling rate of 100 kHz. This is because, the algorithm needs an elevated number of samples for the minimum square estimation gathered in the short time allowed by the capacitor charging.

Stage II: Fault location and resistance estimation

At this stage, the process of determining the location of the fault and its associated resistance begins. The objective function is defined first, followed by the prediction function. The objective function, in particular (referring to equations (4.24) and (4.25)), is a minimisation problem in which the sum of the square errors (or residuals) between the prediction function, Y, and the calculated function, Y^*, within the selected dataset should be minimised. Then, using non-linear programming (Fmincon function), the problem is formulated and solved as an optimization problem in order to determine the unknown values of m and R_f.

Stage III: Fault location evaluation

This is the final stage of the proposed method, in which the location of the fault is reported using a reliability criterion. Before reporting the fault location on the feeder, the proposed algorithm checks the sign of the calculated function Y^*; if the sign of the calculated function is positive, the fault location is reported. If the calculated function's sign is negative, the term $1 - m$ is replaced for m in the algorithm to restore proper operation. From the mathematical point of view, the sign of function Y^* has an impact on the operation of the solver for obtaining the feasible solutions. More specifically, when the function Y^* becomes negative, the reliability of the solver is compromised. For clarification, additional analysis will be provided in the subsection 4.7.2.

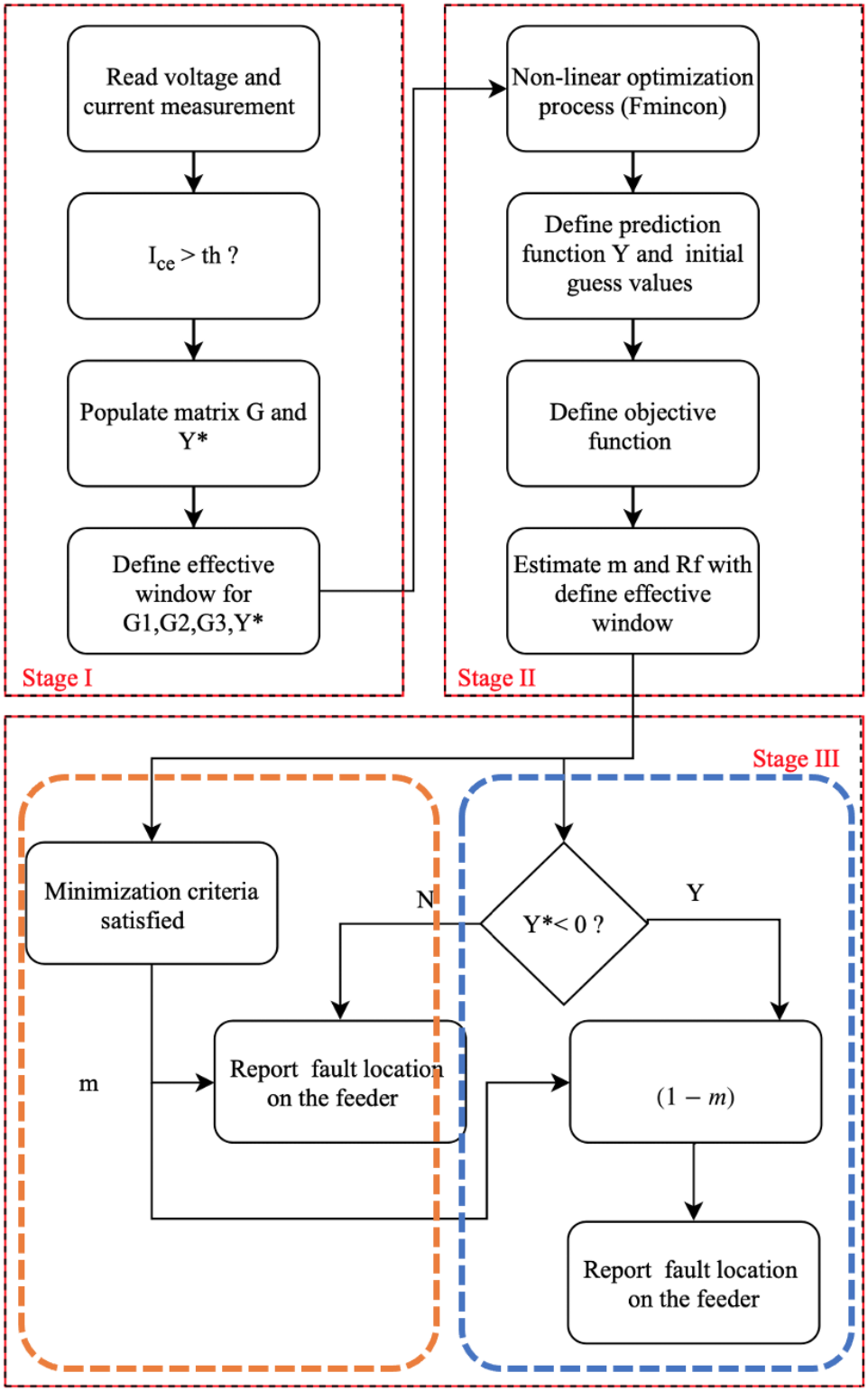


Figure 4.5: Flow chart of the proposed fault location algorithm.

4.7 Simulation Validation

In this section, the proposed method for locating faults is evaluated using the LVDC test network presented in Chapter 4. The LVDC test network incorporates the proposed fault location algorithm. To demonstrate the effectiveness of the proposed fault location technique, various fault scenarios are considered. To begin, validate the accuracy of the fault location estimation. Applying faults with varying fault resistances (e.g., 0.1 Ω, 0.5 Ω, 1 Ω, 1.5 Ω, and 2 Ω) along a 1000m feeder connected between DC sources and passive DC loads with the faults applied at 100m intervals as examples. Then, validate the proposed technique for locating faults on a 1000m feeder connected between local and remote converters (i.e. multiple DC sources). These two cases evaluate the effect of varying cable lengths and different interfaces connected to the remote end (i.e. remote converter or remote DC load) on the proposed fault location technique's accuracy. Finally, the proposed fault location method's performance is compared to that of existing fault location solutions. The following sub-sections will describe the developed model that will be used for validation, followed by detailed simulation studies and a discussion of the simulation results.

4.7.1 Development of the LVDC microgrid test network model

The developed LVDC microgrid test network with a multiple earthing capacitors (depicted in Figure 4.6) is developed and used for the simulation validation studies. The DC network is connected to an AC grid supply point through a two-level VSC and a transformer at Bus 1. DC-DC converters are connected at Bus 2 to integrate the Battery Energy Storage System (BESS) and solar PV system [222]. A lumped DC load is connected at DC Bus 3. A capacitive earthing scheme is connected to Bus 1, Bus 2 and Bus 3 [223]. Using the equation (3.12) in Section 3.3.3 the total capacitance is 10 mF for the entire network. Therefore, the individual earthing capacitor can be calculated as follows:

$$C_{e_{Individaul}} = \frac{C}{N} \tag{4.26}$$

where C is the total capacitance and N is the number of earthing points. In this study, three earthing points are considered and therefore the size of the each earthing capacitor is 3.3 mF. The clamp voltage is defined based on the assumption that the biggest allowable deviation on the poles is 2.5% of the nominal voltage (i.e. 750 V), in this case, ±18.75 V. The LVDC cables are modelled as an equivalent resistance in series with an inductance with each cable assumed to be 1km long. A summary

of the corresponding system parameters of the developed test network are illustrated in Table 4.5. Fault Location Estimators (FLE), where measurements are collected

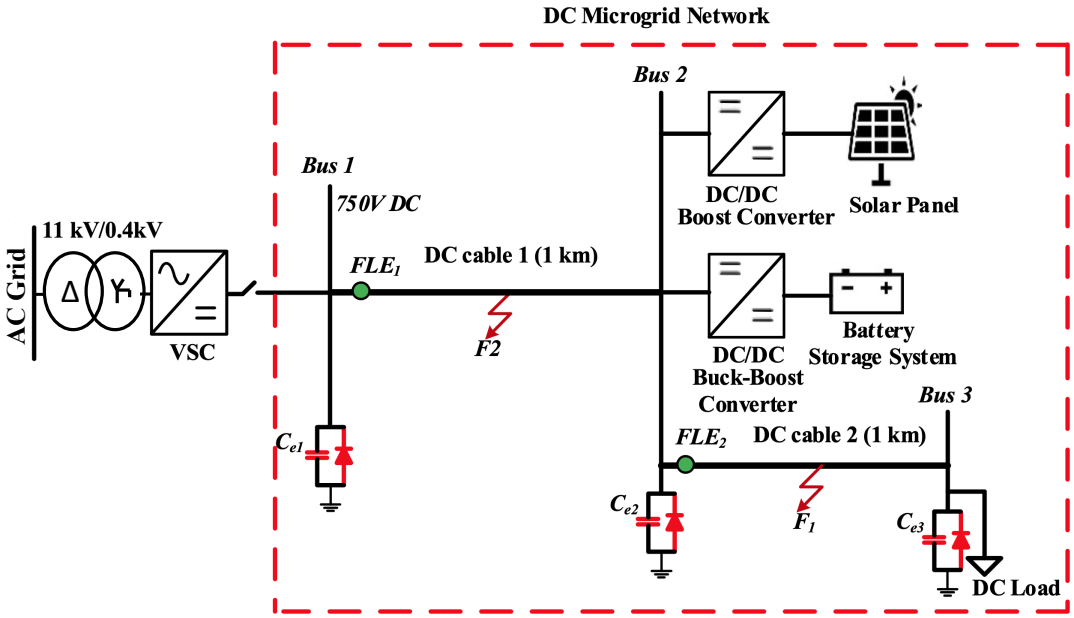


Figure 4.6: Representation of DC microgrid.

Table 4.5: AC and DC Network Parameters

Parameter	Value
AC grid Voltage [kV]	11
Transformer voltage ratio [kV]	11/0.4
DC voltage [V]	750
R, L of LVDC cable	0.017204 [Ω/km],3.3 [mH/km] [224]
Earthing capacitor[mF]	3.3
Battery rating [kWh]	7.8
PV rating[kW]	10
DC load[kW]	19

and algorithm executed, are positioned at Bus 1 and Bus 2 respectively. The fault location results presented in this chapter consider FLE_1 and FLE_2 respectively. The values of fault location estimation error reported in the following subsections have been calculated according to (4.27):

$$error_m(\%) = \frac{mL_{line} - D_F}{L_{line}}.100\% \tag{4.27}$$

where mL_{line} is the calculated fault distance, D_F is the actual fault distance and L_{line} is the total length of the faulted cable. Similarly for fault resistance, R_f, the error reported in the following subsections have been calculated according to (4.28):

$$error_{R_f}(\%) = \frac{R_f - R_{f_{(a)}}}{R_{f_{(a)}}}.100\% \tag{4.28}$$

where R_f is the calculated fault resistance and $R_{f_{(a)}}$ is the actual fault resistance.

4.7.2 Simulation studies

In the simulation studies, DC pole-to-earth faults are applied along the 1km cables with 0.5 fault resistance intervals between 0.1Ω to 2Ω. Faults are applied to DC cable '1' to simulate a feeder with converters connected to its ends, and to DC cable '2' to simulate a feeder with DC passive load connected to its end.

Test case 1: Fault distance estimation for cable between DC sources and passive DC Loads

In this case,the proposed fault location method is evaluated when a feeder is connected between a DC source and a passive DC load. A fault, F_1, is triggered at the DC cable connecting Bus 2 and Bus 3 at various fault locations and resistances, as illustrated in Figure 4.6. The relative error in the fault distance estimated by the FLE_2 is given in Table 4.6. By observing the values in Table 4.6 , it can be demonstrated that the proposed method has a satisfactory level of accuracy (i.e. when the resistance of the fault is 2Ω at a distance of 50m, the maximum error is -0.402%). However, there is a general

Table 4.6: Distance estimation errors for faults at DC cable 2.

Distance [km]	R_f=**0.1** Ω	R_f=**0.5** Ω	R_f=**1.0** Ω	R_f=**1.5** Ω	R_f=**2.0** Ω
0.05	-0.0197 %	-0.0792 %	-0.1391 %	0.2209 %	-0.4022 %
0.1	-0.0273 %	-0.0835 %	-0.1445 %	-0.1878 %	-0.1956 %
0.2	-0.034 %	-0.084 %	-0.139 %	-0.185 %	-0.219 %
0.3	-0.032 %	-0.077 %	-0.127 %	-0.166 %	-0.195 %
0.4	-0.016 %	-0.054 %	-0.099 %	-0.142 %	-0.18 %
0.5	-0.005 %	-0.046 %	-0.094 %	-0.137 %	-0.175 %
0.6	-0.003 %	-0.045 %	-0.094 %	-0.138 %	-0.179 %
0.7	-0.003 %	-0.047 %	-0.1 %	-0.15 %	-0.196 %
0.8	-0.003 %	-0.053 %	-0.114 %	-0.172 %	-0.227 %
0.9	-0.003 %	-0.06 %	-0.128 %	-0.194 %	-0.258 %
0.95	-0.003 %	-0.06 %	-0.13 %	-0.197 %	-0.262 %

trend that as fault resistance increases, the current waveforms become smoother and the persistent excitation signals for the minimum square algorithm decrease, reducing the estimation accuracy. Additionally, the feeder's total inductance is small in comparison to the high fault resistance. As a result, when fault resistance dominates system response, the calculation errors for fault distance increase.

In the same case, it can be deduced from the Figure 4.7 that the relative error in estimating the fault resistance is greater with a long cable distance and less with a short cable distance. Hence, the corresponding error for a fault at 0.95 km is -0.28 %.

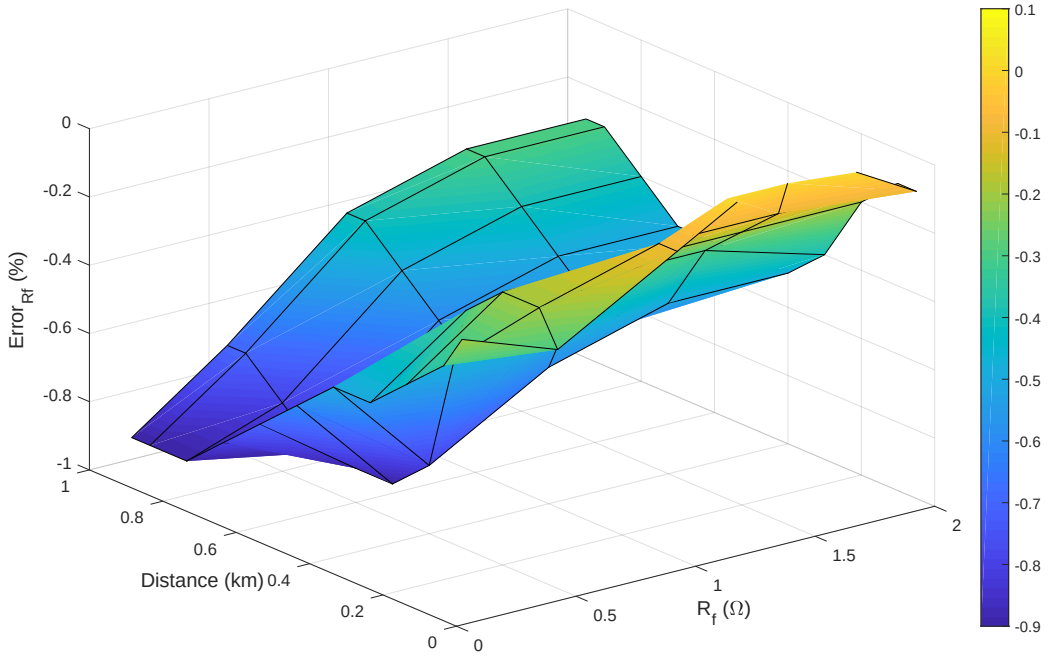


Figure 4.7: Relative errors for fault resistance estimation for faults at DC cable 2.

Test case 2: Fault distance estimation with multiple DC sources

In order to test the proposed fault location method in cases where DC sources are connected at both cable terminals (i.e. to consider the effect of the in-feed transient current generated from both DC converters during a fault), a fault (i.e. F_2) has been triggered along the DC cable connecting Bus 1 and Bus 2 (refer to Fig.4.6) for varying fault location and resistance values. It can be seen in Table 4.7 that when a fault occurs after a certain point along the total cable length, a significant error in distance estimation is induced. This is because the influence of the calculated output coefficient, Y^*, on the optimisation function, X. Therefore, in order to investigate the influence of the calculated output coefficient, Y^*, on the estimation results, the current flow through

Table 4.7: Distance estimation errors for faults at DC cable 1.

Distance [km]	R_f=**0.1** Ω	R_f=**0.5** Ω	R_f=**1.0** Ω	R_f=**1.5** Ω	R_f=**2.0** Ω
0.05	-0.015 %	-0.071 %	-0.136 %	-0.199 %	-0.254 %
0.1	-0.014 %	-0.056 %	-0.101 %	-0.135 %	-0.156 %
0.2	-0.002 %	0.029 %	0.099 %	0.203 %	0.352 %
0.3	0.035 %	0.281 %	0.693 %	1.241 %	1.969 %
0.4	0.18 %	1.284 %	1.362 %	1.741 %	1.932 %
0.5	-0.042 %	-0.258 %	-0.539 %	-0.88 %	-1.308 %
0.6	-19.765 %	-18.119 %	-10.993 %	-11.748 %	-13.984 %
0.7	-40.148 %	-39.447 %	-39.211 %	-26.39 %	-38.017 %
0.8	-60.048 %	-60.841 %	-69.857 %	-64.077 %	-62.466 %
0.9	-80.898 %	-73.686 %	-77.339 %	-78.172 %	-78.706 %
0.95	-93.8359 %	-88.0894 %	-88.5491 %	-88.8488 %	-89.1084 %

the inductor, the voltage derivative and the calculated output coefficient values are compared for four different fault locations on the cable, (i.e. fault at 10%, 30%, 50%, and 90% of the total cable length) as shown in Fig. 4.8. The fault current magnitude is reduced as the fault moves away from the measurement point as shown in Fig. 4.8(a). Also, it is observed that the magnitude of the rate of change of voltage varies with the fault location, as shown in Fig.4.8(b). This is because the closest capacitors supply the majority of the fault current. Consequently, the magnitude of the output coefficient, Y^*, varies with respect to the magnitude of the voltage derivative dv/dt (i.e. the rate of change of the sum of the voltage across the DC link V_{dc1} and the voltage across the earthing capacitor V_{ce1}) in accordance with (4.22) as shown in Fig. 4.8(c). The depicted Fig. 4.8(b) is the result of a detailed simulation. Obviously, the detailed simulation captures many behaviours that were not computed in the simplified model as for example the saturation of the current control . The discontinuity shown in the Fig. 4.8(b) is a result of the nonlinearity of the detailed model (the second discontinuity corresponds to the voltage clamping of the capacitor). Additionally, because the objective function's squared magnitude (refer to 4.24) has an effect on the estimation results after 50% of the total cable length, another criterion (i.e. the sign of the output coefficient Y^*) is incorporated into the algorithm to determine the valid function. As a result, after 50% of the total cable length, an adjustment is made to the fault distance estimation such that when $Y*$ is negative, the term $(1-m)$ replaces m in the algorithm to restore proper operation. The relative errors in the estimations performed by FLE_1 have therefore been reduced after 50% of the total cable length, as shown in Table 4.8.

Similarly, for the purpose of estimating the fault resistance. As shown in the Figure

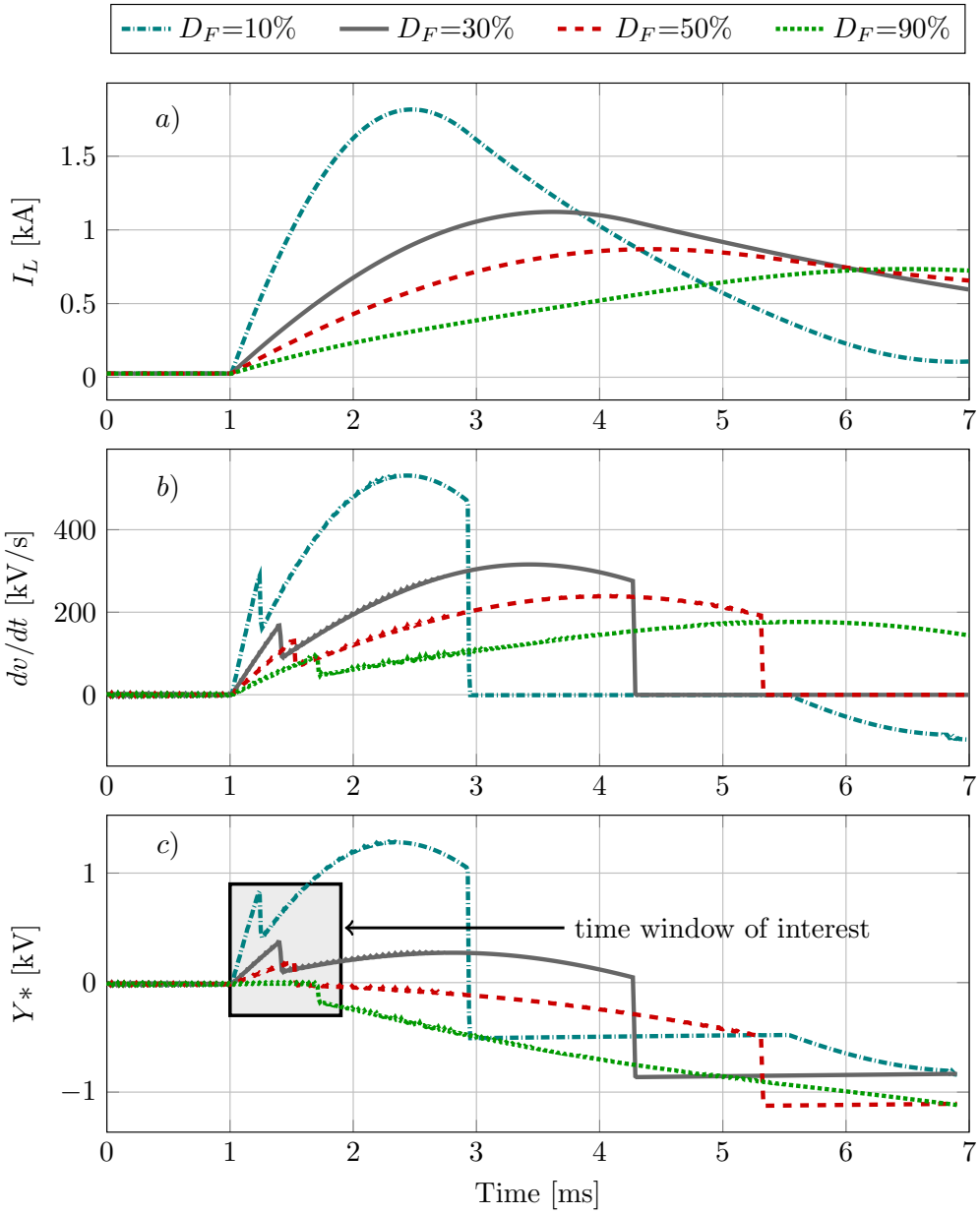


Figure 4.8: System response for faults along various point on the cable: a) Current I_L, b) Voltage derivative $\frac{\mathrm{dV}}{\mathrm{dt}}$, c) Output calculated coefficient Y^*.

4.9, FLE_1 accurately estimates the fault resistance, R_f, for faults located near the fault location estimator point. This is because, when the fault occurs close to the estimator point, the effect of the in-feed transient fault current from the remote end is less than that of a fault that occurs close to the remote side (i.e. fault at 60%, 70%, and 90%). Hence, the maximum error obtained for the fault resistance estimation, as expected at 0.95 km, is 6.5% for an expected fault resistance of R_f=2Ω. In summary, the simulation results (Table 4.6, Table 4.8) demonstrate the difference in estimation errors between

Table 4.8: Improve distance estimation errors for faults at DC cable 1.

Distance [km]	R_f=**0.1** Ω	R_f=**0.5** Ω	R_f=**1.0** Ω	R_f=**1.5** Ω	R_f=**2.0** Ω
0.05	-0.015 %	-0.071 %	-0.136 %	-0.199 %	-0.254 %
0.1	-0.014 %	-0.056 %	-0.101 %	-0.135 %	-0.156 %
0.2	-0.002 %	0.029 %	0.099 %	0.203 %	0.352 %
0.3	0.035 %	0.281 %	0.693 %	1.241 %	1.969 %
0.4	0.18 %	1.284 %	1.362 %	1.741 %	1.932 %
0.5	-0.042 %	-0.258 %	-0.539 %	-0.88 %	-1.308 %
0.6	-0.235 %	-1.881 %	-1.007 %	-1.252 %	-1.016 %
0.7	0.148 %	-0.553 %	-0.789 %	-0.61 %	-1.983 %
0.8	0.048 %	0.841 %	0.857 %	0.177 %	0.466 %
0.9	0.898 %	0.686 %	0.339 %	0.127 %	0.706 %
0.95	-1.164 %	-1.910 %	-1.450 %	-1.151 %	-0.891 %

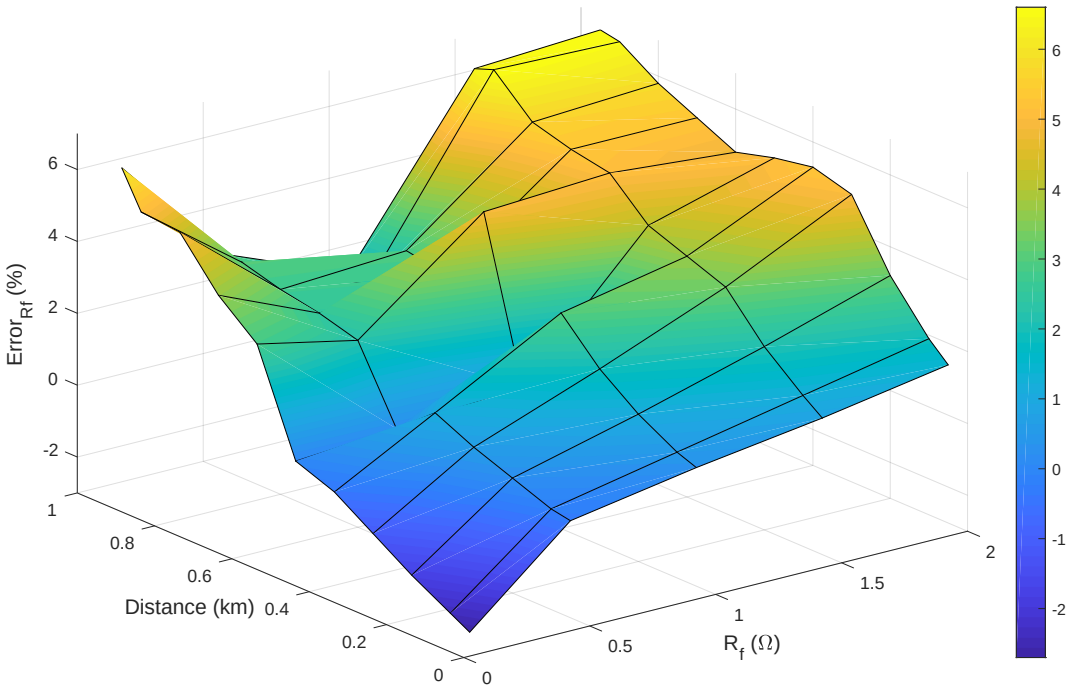


Figure 4.9: Relative errors for fault resistance estimation for faults at DC cable 1.

locator units FLE_1 and FLE_2. The locator unit FLE_1 calculates the fault distance and associated fault resistance when a DC cable is connected to multiple DC sources. In this case, the cable is connected at both ends to various power electronic sources. These power electronic devices are equipped with DC capacitors on both sides of the

network, which contribute to the fault currents developed at both ends of the cable. The results indicate that when the fault occurs beyond 50% of the cable's total length, the relative error can reach 93% for estimating the fault distance. It is noticeable that when the LVDC feeder is connected to different converters on both ends, the fault location estimation is significantly different. The proposed fault location algorithm is improved, allowing for more accurate estimation of the fault distance. This results in a lower relative error of -1.1% and more accurate fault location estimation, particularly for faults located between 500m and 1000m from locator unit FLE_1. Conversely, when a DC cable is connected to a DC source and a DC passive load, the locator unit FLE_2 calculates the fault distance and associated fault resistance. In this case, the DC network is connected upstream with the power source and downstream with the DC passive load. The upstream bus supplies the fault current in this system. As can be seen from the results, increasing the faut resistance results in an inaccurate estimation of the fault distance. This is because as the fault resistance increases, the current waveforms become smoother and the minimum square algorithm's persistent excitation signals decrease, lowering the estimation accuracy.

4.8 Discussion of simulation results

This chapter proposes a novel method for locating faults in an LVDC microgrid by utilising a multiple capacitive earthing scheme. The proposed algorithm is capable of successfully estimating the fault distance regardless of whether the remote end is connected to a DC source or a DC load. The simulation results demonstrated that the proposed algorithm was capable of estimating fault distance for both low- and high-resistance faults (ranging from $R_F = 0.1\ \Omega$ to $2\ \Omega$). Even with high resistance, the proposed algorithm's fault localization accuracy is nearly constant. For instance, when the fault resistance is $2\ \Omega$, the maximum error in fault estimation is 2 %(calculated using the locator unit FLE_1).

On the basis of accuracy, cost, and communication required to locate the fault, the proposed method's performance is compared to that of existing methods [202],[200],[207, 208], and [209] suggested in the literatures. The maximum fault resistance specified in [202], is less than $2\ \Omega$ for DC systems. Additionally, the methods described in [200],[207],[208] and [209] have been conducted with fault resistance values less than $2\ \Omega$. As a result, Table 4.9 includes a qualitative comparison of the proposed method and existing methods for fault resistance value of $2\ \Omega$. Adding hardware components and communication infrastructure increases the cost of the fault location method naturally. In comparison to [202],[200], and [207] the proposed method is relatively inexpensive because it does not require a current injection device and instead estimates the fault

location using local measurements. Additionally, in contrast to the methods described in the literature, the proposed method estimates the fault distance and associated fault resistance for a network that include numerous converter-connected DC loads and DC sources connected at both ends of the feeders. In terms of accuracy, existing methods consider only the case where the DC network is connected upstream to the power source and downstream to the DC passive load; thus, the proposed method's estimation fault distance error is compared to the existing methods' estimation fault distance error in this case. As illustrated in Table 4.9, the fault location algorithm in method [202] has been improved on the basis of method [200], and the fault location accuracy has been increased to greater than 96.4 %. In the case of online fault location, the method described in [207] required two-terminal data synchronisation, with a maximum error of 6 % without taking communication delay into account. The iteration method proposed in [209] has a maximum error of 5 % in fault estimation. The least square method proposed in [208], which is appropriate for single-ended DC network, has a maximum error of 20 %. Whereas the chapter's proposed method has a maximum error of -0.4 % when the fault resistance is within 2 Ω. The simulation results for this case demonstrate the effectiveness of the proposed method, which is based on non-linear optimization for fault location.

4.9 Practical validation of the proposed fault location method

In this section, the experimental validation of the proposed fault location method was conducted with the aim of verifying the proposed method's effectiveness in accurately estimating the fault location and resistance without the need for a communication channel, which was selected based on the worst-case fault distance estimation (i.e. the fault applied at the end of the feeder). This is done to demonstrate the robustness of the proposed method. Additionally, the performance of the proposed method is evaluated in estimating the fault location by taking into account the error and noise in the measurement signal captured by the DC current transducer in the laboratory environment.

4.9.1 Experimental setup

The LVDC microgrid depicted in Figure 4.6 is simplified and scaled down using the low-power test demonstrator and is shown in Figure 4.10 (a photograph of the actual experimental layout is presented in Figure 4.11). The primary VSC and its associated filtering capacitor are represented by a DC source connected in parallel with a capacitor (as shown in Figure 4.10), with the latter providing transient fault current. The

Table 4.9: Qualitative assessment of the existing fault location methods

Study	Technique	Measurement Type	Cost	R_F Estimation	Error (Multiple DC sources)	Error (DC Source-Load)
[202]	Probe Power Unit (PPU)	Local	High	Not Considered	Not Considered	3.6 %
[200]	Noniterative fault-location using PPU	Local	High	Not Considered	Not Considered	7.6 %
[207]	Noniterative Moore-Penrose Pseudo Inverse Technique	Communication	High	Not Considered	Not Considered	6 %
[208]	Least Square method and boundary inductance	Local	Low	Not Considered	Not Considered	20 %
[209]	Iteration method	Local	Low	Not Considered	Not Considered	5 %
Proposed Method	Non-Linear Opti-misa-tion method	Local	Low	Considered	2 %	-0.4 %

capacitor earthing is connected in parallel with a Transient Voltage Suppression (TVS) diode at the negative pole. When the TVS device reaches its clamping voltage (VCL), which is chosen in this experiment to be 6.8 Vdc, it will conduct at its maximum rated current. The clamping voltage requirements are determined by the reverse working and reverse breakdown voltages. When the voltage on the protected line reaches the TVS breakdown voltage, it begins conducting current to earth, effectively clamping the voltage to VCL. Hall-effect sensors are used to measure the DC currents and voltages [225]. To clear the fault-currents, four antiparallel MOSFETs are used as solid-state DC breakers. Artificial fast earth faults are created by controlling the gate driver [226] of a MOSFET in order to create a path to earth (i.e short circuit).

All measuring sensors are connected to the Intelligent Electronic Devices (IEDs), which are emulated on a National Instruments (NI) CRIO-based FPGA instrument [227] that is used to log data and generate gate signals to turn-on or turn-off the MOSFETs. The hardware parameters for the experimental setup are listed in Table 4.10.

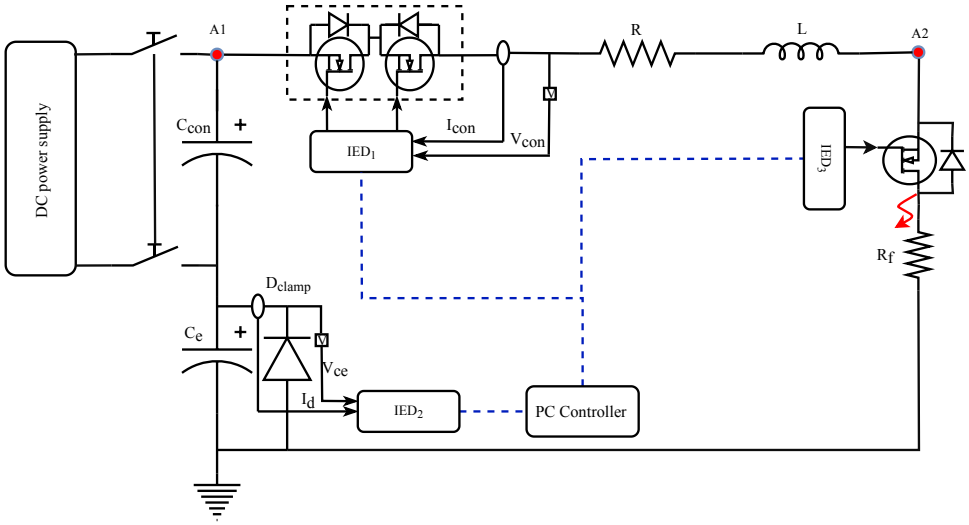


Figure 4.10: Schematic diagram of the experimental arrangement.

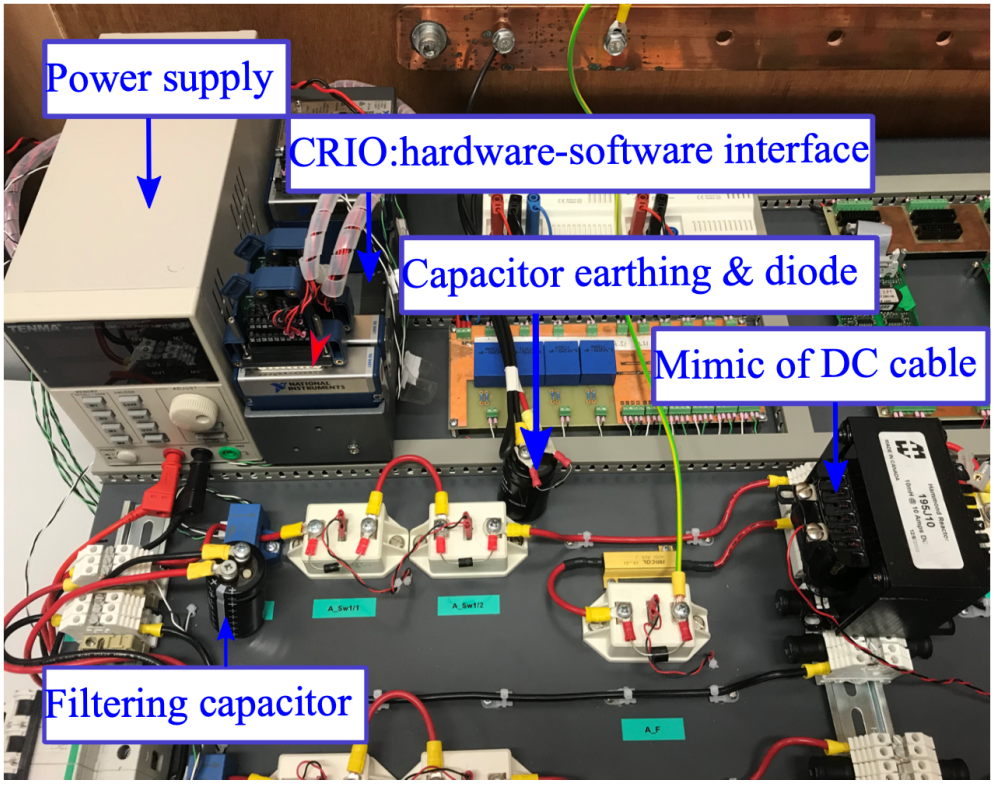


Figure 4.11: Laboratory experimental setup.

4.9.2 Experimental testing and results

The test circuit shown in in Figure 4.10 is energised at 15 V, to remain with the safe operating range of the DC rig (±7.5). A 10 mH inductance is selected to represent the

Table 4.10: Circuit parameters of the experimental arrangement.

V_{dc} [V]	C_{con} [mF]	C_e [mF]	$MOSFET$	$Diode$	R_{line} [Ω]	L_{line} [mH]
15	2.2	2.2	Rated 100 V/200 A	6.8 V	0.07	10

fault distance associated with a typical 3 kilometer section of a DC cable. To evaluate the proposed fault location method's effectiveness in estimating the fault location and resistance, a pole-to-earth fault with a fault resistance of 0.5 Ω is artificially created at the end of the DC cable, as shown in Figure 4.10. The experimental results obtained during this fault are shown in Figure 4.12. When the fault occurs at t=0.1 ms, the voltage across the filtering capacitor, V_{dc}, drops and the filtering capacitor's current, I_{conv}, increases, as illustrated in Figure 4.12(a). Consequently, the voltage across the capacitive earthing scheme increases, V_{ce}, (refer to Figure 4.12(b)) until the diode conducts (at approximately 5 ms) resulting in voltage clamping, at the moment the TVS diode fully conducts. The voltage and current traces associated with the earthing capacitor and filtering capacitor are initially stored in memory and are later transferred to the data management streaming file. These measurements have been used to calculate the coefficients ($G1$, $G2$, $G3$, and $Y*$) for each time interval Δt. Consequently, these coefficients are assigned offline to the non-linear programming function $fmincon$ in order to determine the fault distance and fault resistance. Alternatively, because the algorithm does not have significant real-time limitations, it could be integrated into the processor of a general-purpose protection system or run on a dedicated microcontroller. The fault location algorithm estimates the fault distance and resistance for the period following fault detection and before the diode begins conducting, as illustrated in Figure 4.13. The calculated error for a fault located at 3 kilometres and R_f=0.5 Ω is identified to be 3.1 %. As expected, the accuracy of the experimentally calculated fault location is slightly less than that of the simulation-derived fault location. This could be due to component parameter inaccuracies such as system noise and sensor measurement errors, which have a significant effect on the calculation of di/dt and dv/dt. The accuracy of the proposed algorithm could be increased by reducing sensor noise and signal conditioning (e.g. incorporating a low-pass filter to eliminate noise from the source), which would incur additional costs. To demonstrate the method's feasibility, a moving average filter is used to filter out the noise from the source, ensuring that the location estimated error is kept to a minimum. The estimated location and resistance of the fault are shown in Figure 4.13 after the filter is applied. It can be seen that the estimation process becomes stable at t=3.5 ms with the corresponding

error calculated for the experimental-based signatures being 1.1 % for estimating the fault location (refer to Figure 4.13), demonstrating that the addition of filtering improves the proposed method's accuracy when compared to estimation without filtering. This experiment demonstrates that even with additional filtering, the proposed algorithm performed correctly. As a result, the proposed algorithm is considered to offer a reasonable trade-off between accuracy and implementation cost.

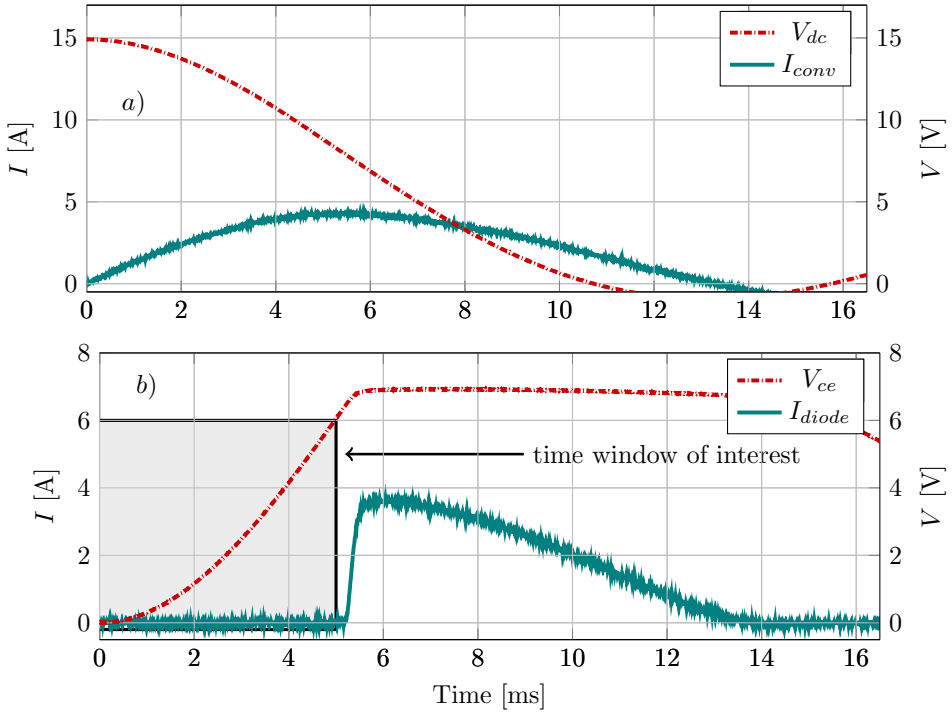


Figure 4.12: Experimental results: a) DC Voltage and current of VSC filtering capacitor, b) Voltage across capacitive earthing scheme and diode current

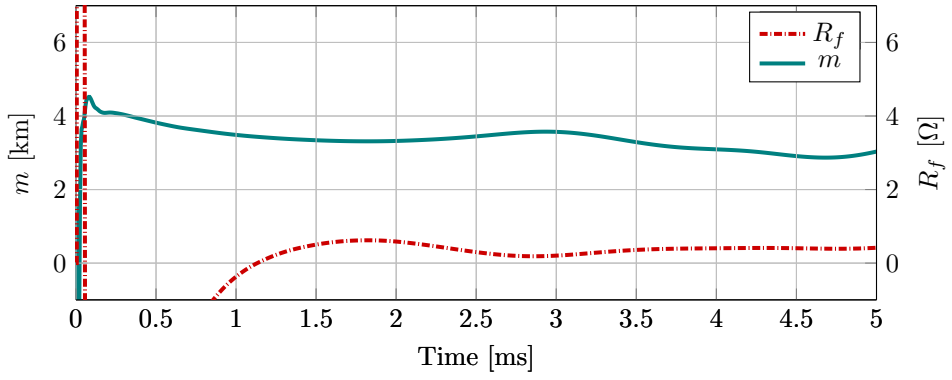


Figure 4.13: Fault distance and fault resistance estimation during experimental testing.

4.10 Chapter 4 summary

This chapter has developed two novel fault location estimation techniques through the use of a capacitive earthing scheme that can be applied successfully for LVDC microgrid. The mathematical analysis of the faulted feeder model with single earthing and multiple earthing schemes is performed. It can be concluded that the proposed method, which combines the least squares method with a moving average and Savitzky-Golay filters, provides a more accurate estimation of fault location than the initial di/dt measurement method. For example, when the fault resistance is 0.1 Ω, the estimation of the fault location is relatively accurate (1.5 m, 0.3 %, with the fault applied in the middle of the feeder) in comparison to the initial di/dt measurement method, which results in a significant error in estimating the fault location (43 m, 8.6 % , the fault applied at the middle of the feeder). The simulation results indicate that combining the least squares method with a moving average and Savitzky-Golay filters significantly reduces the fault estimation errors. While, the second method proposed, the proposed algorithm is capable of successfully estimating the fault distance regardless of whether the remote end is connected to a DC source or a DC load. The simulation results indicated that the proposed algorithm was capable of estimating fault distance for both low- and high-resistance faults (ranging from $R_F = 0.1$ Ω to 2 Ω). Even with high resistance, the proposed algorithm's fault localization accuracy is nearly constant. For instance, when the fault resistance is 2 Ω, the maximum error in fault estimation is 2 %(calculated using the locator unit FLE_1). The increased accuracy enables accurate location of DC faults and expeditious post-fault cable maintenance, even when different converters are deployed at each end of a feeder. Finally, the improved accuracy of the proposed fault location techniques enables the use of LVDC microgrids in a broader range of applications.

Chapter 5

Fault Detection and Isolation in LVDC Microgrid Networks with a Capacitive Earthing Scheme

5.1 Introduction

From chapter 4, it has been established that a DC fault current, originated from the discharge of the DC-link capacitor, could increase to more than a hundred times the nominal current during a sudden fault inception. In order to prevent these high currents from damaging the internal components of the VSC converter, it is crucial to have an effective protection scheme in place. The ideal protection scheme must be able to detect and interrupt the DC fault current fast and efficiently before any damage can be done to these components (e.g. IGBT). One of the main impediments to the transition from a primarily AC-based power system to one that takes advantage of the benefits of DC integration, is the provision of adequate protection equipment and personal safety. This very much depends on having a reliable protection scheme that provides a quick and reliable fault identification, discrimination, and isolation.

A fundamental challenge in DC protection is the lack of zero crossing point, therefore faults are more difficult to interrupt with fuses and circuit breakers as seen in AC circuits. Additionally, converter-based DG sources in islanded mode have limited fault current contribution, thus requiring a protection scheme able to detect low DC fault currents magnitude [228]. Finally, the lack of published standards and limited field experience have made it challenging for the DC industry to design effective protection strategies [229]. Therefore, this chapter will focus on addressing these challenges with the development of a novel DC current-based protection scheme that uses a multiple capacitive earthing scheme to rapidly detect, discriminate and effectively isolate DC

faults in a LVDC microgrid. The proposed protection method relies on local measurements (e.g. the current of the earthing capacitors) to detect the fault and therefore does not require the assistance of communication links. This arrangement allows for a faster fault detection since it does not rely on the communication between local and remote-end relays, which commonly results in a delay in the response time. In order to be able to discriminate the location of the fault, the proposed method uses the capacitor currents concavity (sign of d^2I/dt^2, extracted from the increasing and decreasing trends in the rate of change of fault current dI/dt) to extrapolate if the fault is internal or external. The proposed method is independent of current magnitude and allows the detection of high resistance faults, which would not be otherwise detected if threshold-dependent methods were employed. Furthermore, the proposed protection method was validated under both grid connected and islanded modes, in order to test the effectiveness of the proposed protection scheme under these conditions.

5.2 Limitations of the existing fault detection and discrimination methods

DC protection schemes can be classified into two main groups non-unit and unit protection techniques. Non-unit protection schemes do not protect precise zone boundaries of the power system and instead operate whenever a threshold criterion is breached. Unit protection schemes on the other hand protect against faults occurrences within the specified boundary zones of the power system while remaining inoperative for external faults. The main disadvantages associated with unit protection schemes is that they do not provide backup protection capability to adjacent elements in the system [230]. Additionally, there can be a considerable cost associated with the use of the communication links, which is concerning in terms of the reliability and complexity of such schemes. Thus, non-unit protection is often deployed alongside unit protection to provide valuable backup protection functionality. The main unit protection schemes proposed in literature are differential protection and directional protection schemes. Differential protection schemes rely on a continuous comparison of measurements taken from both ends of the protected zone (normally current is used) to determine whether a fault has occurred or not [200, 231]. A differential current-based fast detection and fault location method is reported in [207]. The method relies on current measurements captured from both ends of the faulted feeder and utilizes a non-iterative and cumulative sum average approach. Nevertheless, the main area of concern associated with differential protection is the need for a communication system of potentially high cost as well as the susceptibility to current transducer errors. Directional protection is an-

other technique for unit protection that makes use of the current direction but does not require a threshold selection. DC directional protection compares the direction information of relays directly via communication. A directional protection scheme for a DC ring microgrid where communications are in place is reported in [232, 233]. The method proposed by these authors relies on capturing voltage and current data during a fault using a local Intelligent Electronics Device (IED). A least squares technique is used to estimate the inductance of the fault path to discriminate between internal and external faults with respect to the IED. This method was improved by the work introduced in [233], by specifically considering the use of the oscillation frequency and transient power information at both ends.

In contrast, the main non-unit protection schemes reported in the literature are overcurrent protection and current derivative protection. Overcurrent DC protection is similar to the conventional AC overcurrent protection in the respect that a threshold criterion is considered to determine the incidence of the fault. A method involving the combination of overcurrent and under voltage embedded into a converter is reported in [234]. The authors illustrated that such a method can quickly detect and locate a fault within a few milliseconds, however this method does not take into consideration the impact of high fault resistance. As a consequence, a lack of sensitivity in detecting high resistive faults results in either longer fault clearance times or the disconnection of more parts of a network than necessary in the event of a fault. The operating principle of current derivative protection is based on calculating the current derivative once the fault has occurred. Using the peak value of the current derivative allows the identification of a fault in a very short time. A protection scheme based on the natural characteristics of DC current in relation to its first and second derivatives under fault transients is reported in [235]. This scheme relies on analytically calculating the threshold of the first and second derivatives, in order to improve the selectivity of the protection scheme. However, the threshold calculation of the fault current derivative requires a high sampling frequency to classify the faults as internal or external. This, in turn, amplifies the noise in the measurement components and may result in maloperation of the protection scheme. Also, calculating the threshold for all operating conditions of a LVDC microgrid is considered the main drawback of this method. A singularity detection approach using stationary wavelet transform (SWT) is reported in [236] considering the current signal of the DC link capacitor of the DAB converter. However, this procedure is faster than the FFT and sliding DFT but it still requires several computations which result in a penalty in the performance which though acceptable for fault location is not suitable for the protection application considered here. Therefore, the following section will present a novel DC current-based (i.e. non-unit protection scheme) communication-less protection scheme that uses the current concav-

ity to improve the selectivity (i.e. discrimination between internal and external faults) compared with existing current-based protection methods in LVDC microgrid network, and that can operate under both grid connected and islanded modes.

5.3 Concept of the proposed protection scheme

5.3.1 Description of a mathematical faulted feeder model

This section will present a mathematical analysis to describe the response of a simplified DC network connected to a multiple capacitive earthing scheme, under faulted conditions (i.e. internal and external pole-to-earth faults).

Simplified model

The simplified model is depicted in Figure 5.1. In this model, the initial current during steady state is primarily determined by the R_1 and R_2, and these are assumed to be very small. The network is of fourth-order, with four nodes and three mats when the fault branch is combined with the fault resistance (R_F).

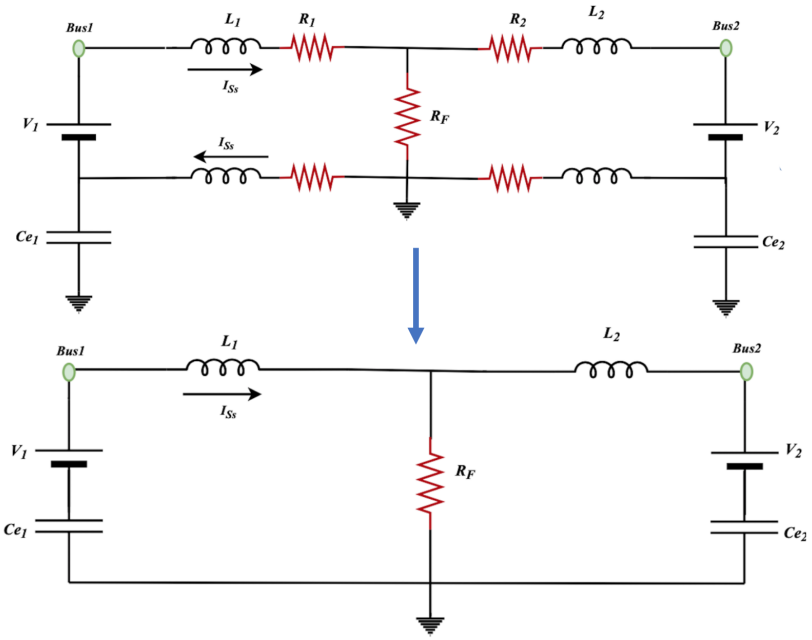


Figure 5.1: Simplified model.

To simplify the equations, resistances are omitted from the circuit, as inductors have a greater effect on the DC current than resistors do during the transient state. Additionally, return current is omitted from the circuit because it does not close the path to the earth and has a negligible effect. Finally, in this model, it is assumed the capacitor's initial current be the same as the return current. Therefore, the capacitor in

the earth fault circuit is unaffected. It is worth noting that the earth capacitor current is zero during steady state operation, regardless of the line currents.

Internal faulted feeder model

The state space equations, representing the faulted feeder under the influence of a pole-to-earth fault occurring internally (as depicted in Figure.5.2), are written in the Laplace domain form as:

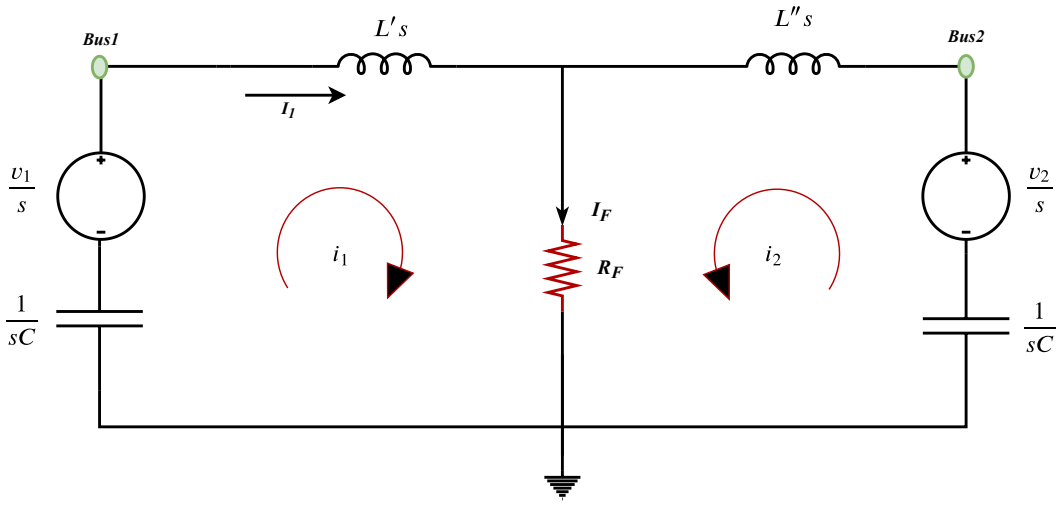


Figure 5.2: Equivalent network of DC feeder with DC sources at both terminals and a multiple capacitive earthing scheme. Fault occurs in the middle of the feeder as shown.

where L' is the equivalent cable inductance up to the fault point (taking as reference Bus1), L'' is the equivalent cable inductance up to the fault point (taking as reference Bus2). R_F is the fault resistance, v_1 is the initial voltage across the filtering capacitor at Bus1, v_2 is the initial voltage across the filtering capacitor at Bus2, i_1 is DC current flowing through an earthing capacitor in connection to Bus1 and i_2 is DC current flowing through an earthing capacitor in connection to Bus2 during the fault. The earthing capacitance is denoted C at both ends.

In the case of a pole-to-earth fault, when the fault occurs at the middle of the line, the DC currents flowing through an earthing capacitors i_1 and i_2 in connection to Bus1 and Bus2 can be expressed in the Laplace domain as follows:

$$\frac{v_1}{s} - \frac{1}{sC}i_1 - sL'i_1 - R_f(i_1 + i_2) = 0 \tag{5.1}$$

$$\frac{v_2}{s} - \frac{1}{sC}i_2 - sL''i_2 - R_f(i_1 + i_2) = 0 \tag{5.2}$$

solving the equations 5.1 and 5.2 to obtain I_1

$$I_1(s) = \frac{C(v_1 + CL''v_1s^2 + CR_fv_1s - CR_fv_2s)}{C^2L'L''s^4 + (C^2L'R_f + C^2L''R_f)s^3 + (CL' + CL'')s^2 + 2CR_fs + 1} \tag{5.3}$$

Since the function $I_1(s)$ is defined in the Laplace domain, the first derivative of the current can be determined using the initial value theorem at $\lim_{t\to 0^+} \frac{di_1}{dt}(t)$:

$$\lim_{t\to 0^+} \frac{di_1}{dt}(t) = \lim_{s\to\infty} s^2 I_1 = \frac{v_1}{L'} \tag{5.4}$$

Consequently, using (5.3), the second derivative of the current can be determined using the initial value theorem at $\lim_{t\to 0^+} \frac{d^2i_1}{dt^2}(t)$:

$$\lim_{t\to 0^+} \frac{d^2i_1}{dt^2}(t) = \lim_{s\to\infty} s^3 I_1 = -R_f\left(\frac{v_1}{L'^2} + \frac{v_2}{L'L''}\right) \tag{5.5}$$

The negative sign of the initial value for the second derivative of the earthing capacitor's DC current is considered in identifying the fault section within the network as an internal fault.

External faulted feeder model

The state space equations representing the faulted feeder under the influence of a pole-to-earth fault occurring externally (as depicted in Figure.5.3), are written in the Laplace domain form as:

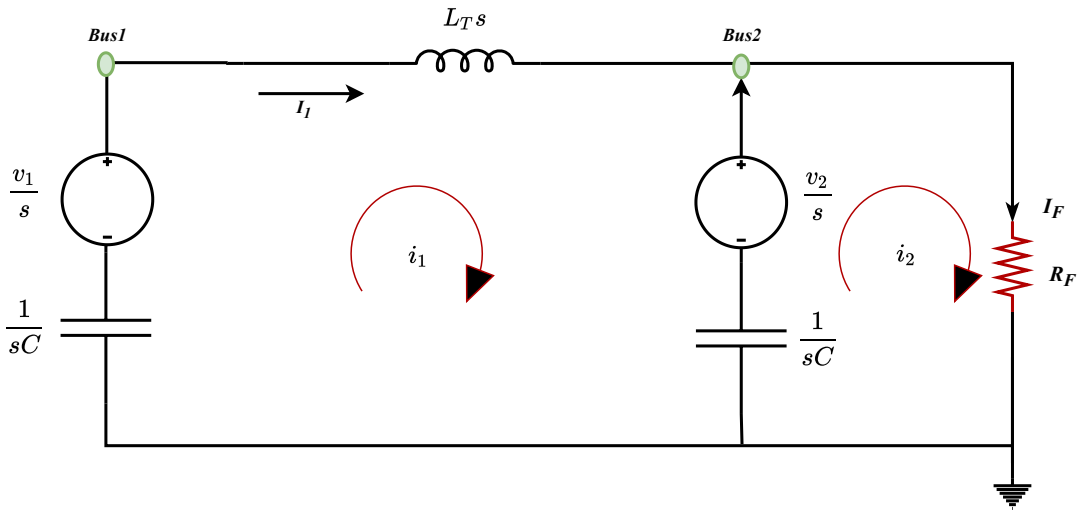


Figure 5.3: Equivalent network of DC feeder with DC sources at both terminals and a multiple capacitive earthing scheme. Fault occurs at the end of the feeder as shown.

where L_T is the total equivalent cable inductance, R_F is the fault resistance, v_1 is the initial voltage across the filtering capacitor at Bus1, v_2 is the initial voltage across the filtering capacitor at Bus2, i_1 is DC current flowing through an earthing capacitor in connection to Bus1 and i_2 is DC current flowing through an earthing capacitor in connection to Bus2 during the fault. The earthing capacitance is denoted C at both ends. In the case of the pole-to-earth fault, when the fault occurs at the end of the line, the DC current flowing through an earthing capacitor I_1 in connection to Bus1 can be expressed as follows:

$$I_1(s) = \frac{C(v_1 + CR_f v_1 s - CR_f v_2 s)}{L_T R_f C^2 s^3 + L_T C s^2 + 2R_f C s + 1} \tag{5.6}$$

Since the function $I_1(s)$ is defined in the Laplace domain, the first derivative of the current can be determined using the initial value theorem at $\lim_{t\to 0^+} \frac{di_1}{dt}(t)$:

$$\lim_{t\to 0^+} \frac{di_1}{dt}(t) = \lim_{s\to\infty} s^2 I_1 = \frac{v_1 - v_2}{L_T} \tag{5.7}$$

Consequently, using (5.6), the second derivative of the current can be determined using the initial value theorem at $\lim_{t\to 0^+} \frac{d^2 i_1}{dt^2}(t)$:

$$\lim_{t\to 0^+} \frac{d^2 i_1}{dt^2}(t) = \lim_{s\to\infty} s^3 I_1 = -\frac{(v_1 - v_2)}{CL_T}) + \frac{v_1}{CL_T R_f} \tag{5.8}$$

For this expression (5.8) to be positive :

$$\begin{aligned} \frac{v_1}{CL_T R_f}[1 - \frac{(v_1 - v_2)}{CL_T}\frac{CL_T R_f}{v_1}] &> 0 \\ \frac{v_1}{CL_T R_f}[1 - (1 - \frac{v_2}{v_1})R_f] &> 0 \\ (1 - \frac{v_2}{v_1})R_f &< 1 \end{aligned} \tag{5.9}$$

Assuming that the voltage drop across the line is less than 10% ($\frac{v_2}{v_1} > 0.9$), the initial value of the second derivative of the DC current (5.8) will be positive for values of R_f<10 Ω. This range R_f<10 Ω covers faults with reasonably high resistance in DC microgrids [217].

Discontinuities in the second derivative

In the ideal case, when a network encounters a fault, the DC fault current changes abruptly, resulting in a step change in the first derivative and a Dirac delta function (discontinuity function) in the second derivative as illustrated in Figure 5.4.

Following this transient after the fault, current and its derivatives become continu-

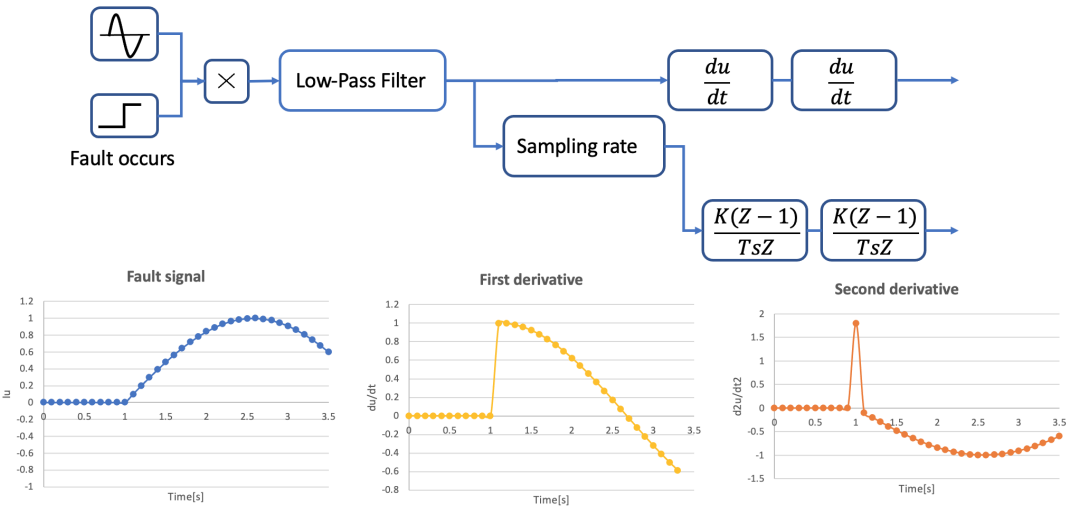


Figure 5.4: The optimal sampling model of the DC current and its derivatives

ous signals. The passive elements (inductance, capacitance, and resistance) will act as a low-pass filter for the response. As a result, the sampling period is always assumed to be greater than the circuit's fast time constant τ (where τ denotes the passive elements' time constant). This indicates that the peak will disappear prior to the next sampling time. This results in a dirac delta function for the second derivative of the discretized version of the continuous signal. These transients must be taken into account when computing the current first and second derivatives in a discrete format. The proposed method's discrete implementation with non-synchronised sampling (i.e. the fault (assumed instantaneous) will not occur at the same time as the sampling instant) utilizes two samples (i.e. current sample and previous sample) to estimate the first derivative and three samples to estimate the second derivative (i.e. current sample and two previous samples) as illustrated in Figure 5.5. As a result, the explained transient should have no effect on the three current samples being used to estimate the derivate. In order to implement the procedure described above, at least three samples must be delayed after the fault detection. It is worth noting that computation delay is not considered (calculations are carried out instantaneously after the sampling). The effect of sampling discontinuous signals is thoroughly explained in [26].

From the above analysis, the developed protection algorithm will use the sign of the current of the second derivative (d^2I/dt^2) to extrapolate if the fault is internal or external, and this can be described as follows:

- If $d^2I/dt^2 < 0$, the fault is classified as internal
- If $d^2I/dt^2 > 0$, the fault is classified as external

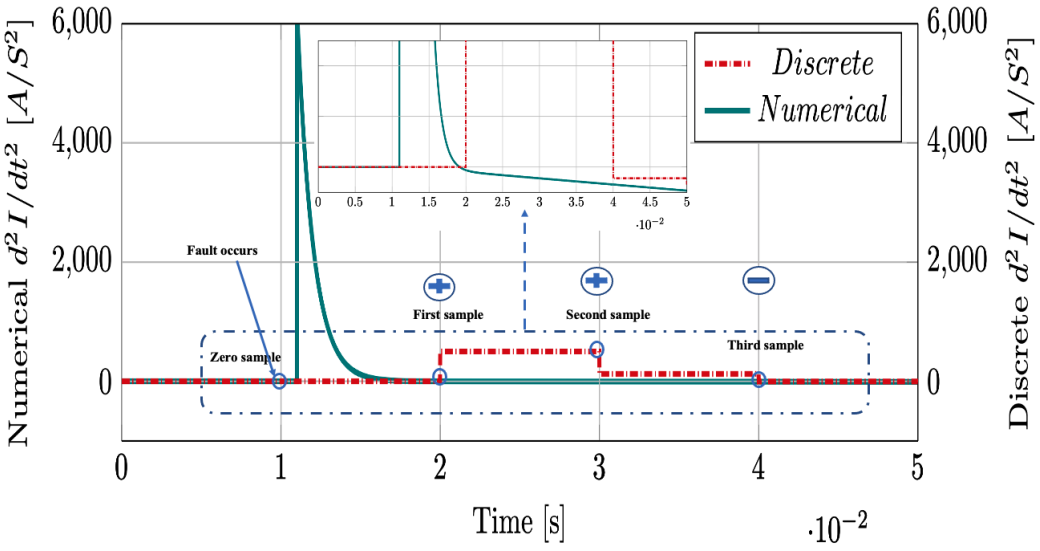


Figure 5.5: Computing the second order derivative with non-synchronised sampling.

5.3.2 Description of the current based-protection algorithm

The flow chart of the proposed protection scheme can be divided into three main stages (depicted in Figure 5.6) explained in detail as follows:

Stage I-Signal acquisition

On stage one, the capacitive earthing current signals required for the implementation of the DC protection method are captured and used to calculate the first derivatives of the DC earth current.

Stage II-DC fault detection

At this stage, when a fault occurs on the feeder, the current flowing from the earthing capacitor I_{ce} becomes substantially higher than the zero current. For the purposes of this study, it is assumed that the threshold is 1% of the rated current. As a result, the algorithm will generate a flag signal, rendering the transient as a fault. This earth fault initiates a closed loop circuit to earth thus charging the earthing capacitor. In contrast, a sudden load change will not cause a jump in the voltage across the earthing capacitor, and so does not affect the detection procedure of the proposed method. Following to that, the sign of the first derivative has to be positive in order to avoid an unwanted trip. If the criterion for Stage II is established that a earth fault has been detected, then the fault discrimination algorithm can be initiated.

Stage III-DC fault discrimination

This is the final stage of the proposed method. The main purpose of discrimination (selectivity) is to identify the faulted section within a network. This process is achieved by measuring at least three sample points of the capacitor current of the second derivative (notice that, in the previous subsection, considers computing the second derivative as the right side limit for t as it approaches $0+$), then check the sign of the following one sample of the current of the second derivative. If it is positive, then the discriminatory algorithm classifies the fault as external and no trip command is generated. On the contrary, if it is negative, then the algorithm will check if the previous three sample points are monotonic or non-monotonic (i.e. to distinguish between transient and other effects upon which it falls). If the previous three sample points are monotonic, the discriminatory algorithm classifies the fault as external and no trip command is generated. If the previous three sample points are non-monotonic and the following one sample is negative, then the discriminatory algorithm classifies the fault as internal. Therefore, a trip command is sent to the associated circuit breakers to isolate the faulted section.

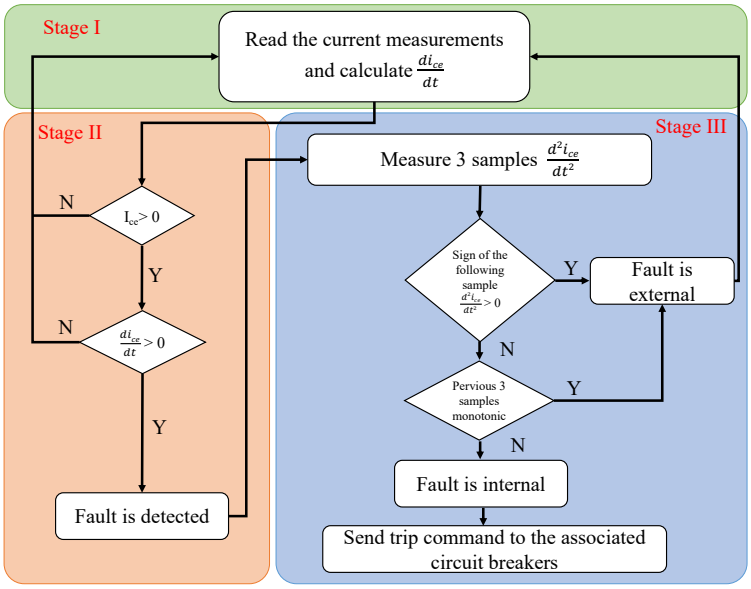


Figure 5.6: Flow chart of the algorithm for the protection scheme.

5.4 Simulation Validation

In this section, the proposed protection scheme is tested in the LVDC test network built based on the LVDC model presented in Chapter 4. The proposed current-based

protection algorithm is incorporated in the LVDC test network. The proposed protection scheme is tested under solid and high-resistance faults during grid-connected and islanded modes in order to verify the feasibility of the proposed protection scheme. For each mode, the ability of the proposed protection scheme to discriminate between internal or external fault is also assessed. The impact of measurement noise on the performance of the proposed method is included in the simulation to evaluate the resilience of the developed scheme. Finally, the performance of the proposed protection scheme is compared with existing current-based protection solutions. The following sub-section will introduce the developed model that is going to be used in the validation followed by detailed simulation studies, and the discussion of the simulation results.

5.4.1 Development of the LVDC microgrid test network model

The developed LVDC microgrid test network with a multiple earthing capacitors (depicted in Figure 5.7) is developed and used for the simulation validation studies. The DC network is connected to an AC grid supply point through a two-level VSC and a transformer at Bus 1. DC-DC converters are connected at Bus 2 to integrate the Battery Energy Storage System (BESS) and solar PV system [222]. A lumped DC load is connected at DC Bus 3. A capacitive earthing scheme is connected to Bus 1, Bus 2 and Bus 3 [223]. However, the capacitive earthing scheme only works if it is connected to every buses. This will increase the cost of the solutions, but it will ensure that selectivity (discrimination) between protection devices is achieved in both connected and islanded modes. The LVDC cables are modelled as an equivalent resistance in series with an inductance with each cable assumed to be 1km long. A summary of the corresponding system parameters of the developed test network are illustrated in Table 5.1.

Table 5.1: AC and DC Network Parameters

Parameter	**Value**
AC grid Voltage [kV]	11
Transformer voltage ratio [kV]	11/0.4
DC voltage [V]	750
R, L of LVDC cable	0.017204 Ω/km, 3.3 mH/km [224]
Earthing capacitor [mF]	3.3
Battery rating [kWh]	7.8
PV rating [kW]	10
DC load [kW]	19

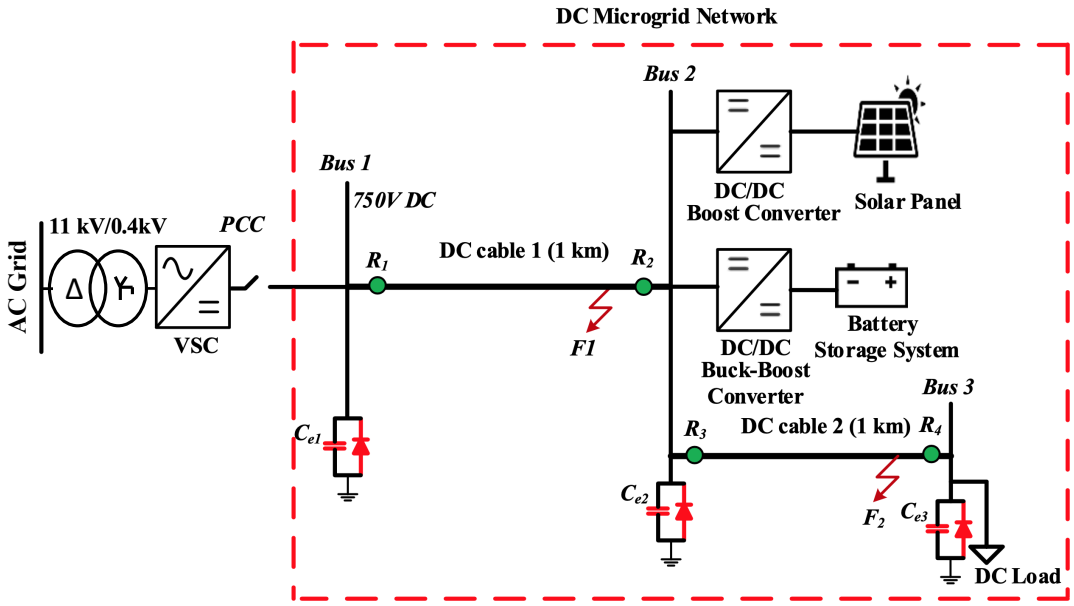


Figure 5.7: Representation of LVDC microgrid.

5.4.2 Simulation studies

In the following section, several fault scenarios under both grid-connected and islanded modes are simulated to demonstrate the effectiveness of the proposed method. In all the study cases, it is assumed that a fault is initiated at $t = 0.1$ ms. Also, it is assumed that the operating time of the solid state DCCBs to be less than 1 ms [237]. Fault discrimination is initiated after the detection criterion is met. The sign of the second current derivative discrimination algorithm is executed to classify a relay as internal or external to the faulted cable. Then, a trip command to clear and isolate the DC fault is sent to the DC circuit breakers classified as internal to the faulted cable. To ensure that the proposed protection scheme can extrapolate the derivative signals within high resolution window, a signal sampling rate of 100 kHz was utilized [238]. Simulation studies are carried out using MATLAB/Simulink software package.

Test case 1: Performance of the proposed protection methods under grid-connected

A) Protection against solid earth faults

A solid pole-to-earth fault, F_1, with respect to relays R_1 and R_2 is triggered at the end of cable 1 (refer to Figure 5.8). In this case, the relays 1 and 2 (R_1 and R_2, respectively) should be identified this fault as internal (within their cable) and the relays 3 and 4 (R_3 and R_4, respectively) should be identified this fault as external to them (outwith

their cable).

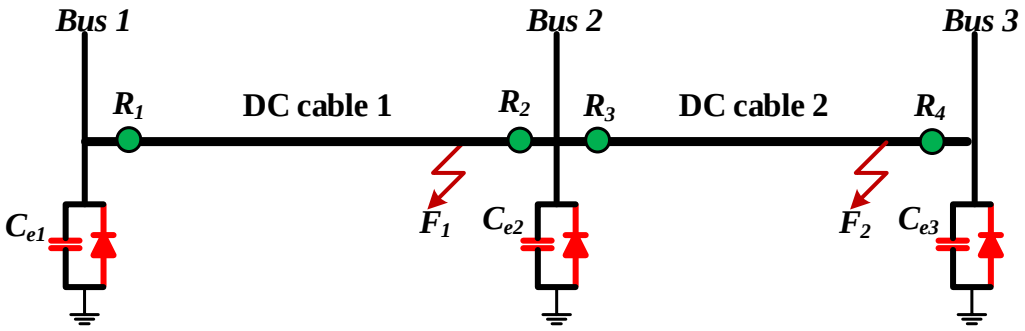


Figure 5.8: Simplified diagram of an LVDC cable under solid faults being applied on cable 1 (Fault 1, F_1) and cable 2 (Fault 2, F_2).

A-I) Internal fault location

The response of the protection system for solid earth fault is represented in Figure 5.9. After the fault is trigged at $t = 0.1$ ms, there is a rapid increase in the current from the earthing capacitor connected to the faulted feeder (refer to Figure 5.9(a)). As a consequence, the rate of change of current(di_{Ce1}/dt) experiences an increase following the DC fault occurrence. Due to the initial discrete form of the mathematical model, a sudden change at the beginning of the second derivative of the current occurs. Therefore, for calculation of (d^2i_{Ce1}/dt^2) at least three sample points after the fault incident should be elapsed (t>0+). The elapsed time for (d^2i_{Ce1}/dt^2) is sufficient time to cancel the effect of discrete implementation of the derivative as previously demonstrated [239]. It should be noted that the values of di_{Ce1}/dt are always positive, which is well-aligned with the theoretical analysis introduced in (5.4). The last stage of the algorithm verifies that the previous three sample points of the current of the second derivative (d^2i_{Ce1}/dt^2) are non-monotonic and the sign of the following one sample point is negative (refer to Figure 5.9(c)), and is verified by the theoretical analysis introduced in (5.5). This satisfies the criterion for an internal fault and therefore, the algorithm will initiate a tripping command to the relays R_1 and R_2 connected to the faulted feeder (refer to Figure 5.9(e)), to clear and isolate the DC fault.

The discriminatory algorithm will not initiate a tripping command to relays R_3 and R_4 (refer to Figure 5.9(e)) for isolation of the faulted section, since the previous three sample points of the current of the second derivative (d^2i_{Ce3}/dt^2) are monotonic, and therefore it is considered as an external fault with respect to them (refer to Figure 5.9(d)).

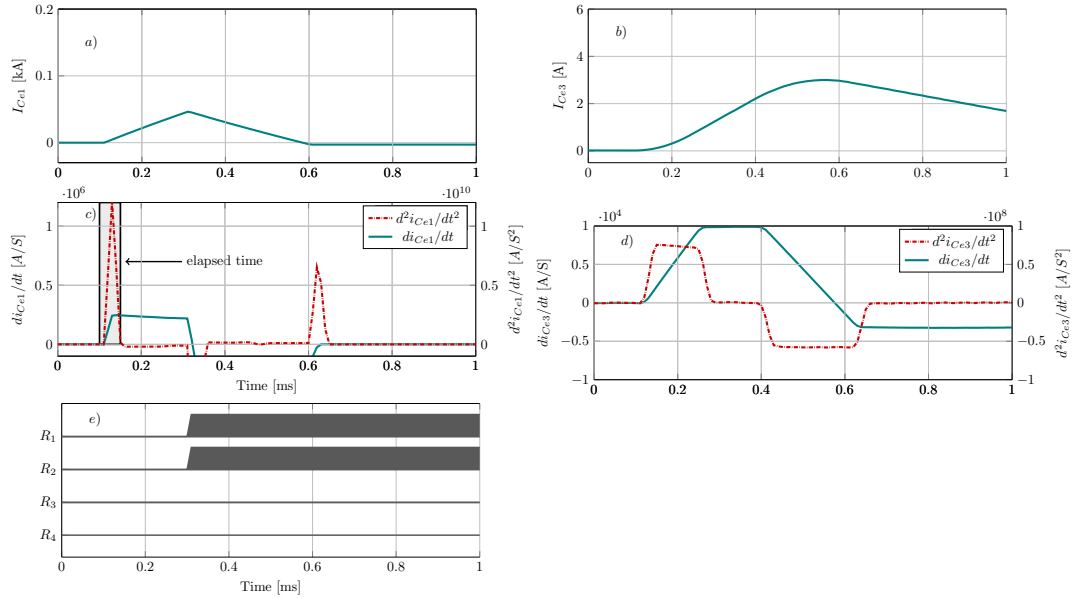


Figure 5.9: Response of protection system to internal fault (solid-earth fault F_1): a) DC current I_{Ce1}, b) DC current I_{Ce3} c) The rate of change of current di_{Ce1}/dt and d^2i_{Ce1}/dt^2, d)The rate of change of current di_{Ce3}/dt and d^2i_{Ce3}/dt^2 e) Tripping signals.

A-II) External fault location

A solid pole-to-earth fault, F_2, with respect to relays R_3 and R_4 is triggered at the end of cable 2 (refer to Figure 5.8). In this case, the relays 1 and 2 (R1 and R2, respectively) should be identified this fault as external (outwith their cable). The response of the protection system for this fault is depicted in Figure 5.10. After the fault is triggered at $t = 0.1$ ms, the DC fault current is analysed with respect to the relay R_1, which is external to the faulted feeder. The DC fault current is increased slowly with a small amplitude value (refer to Figure 5.10(a)), this is due to the effect of the impedance of the line. The first current derivative produces a positively increasing trend over a period of time that aligns with the theoretical analysis introduced in(5.7). Accordingly, the second derivative of current also increases towards a positive value (refer to Figure 5.10(b)), and is corroborated with the theoretical analysis introduced in (5.8). In this case the voltage drop across the line is lower than 1%. It is worth noting that when the corresponding CBs connected to the faulty feeder are operated, the second derivative of the current decreases immediately, but the discriminatory algorithm will not initiate a tripping command to relays R_1 and R_2 for isolation of the faulted section, since the previous three sample points of the current of the second derivative (d^2i_{Ce1}/dt^2) are monotonic, and therefore it is considered as an external fault with respect to them. On the contrary, the algorithm will initiate a tripping command to the relays R_3 and R_4 connected to the faulted feeder (refer to Figure 5.10(c)) to clear and isolate the DC

fault.

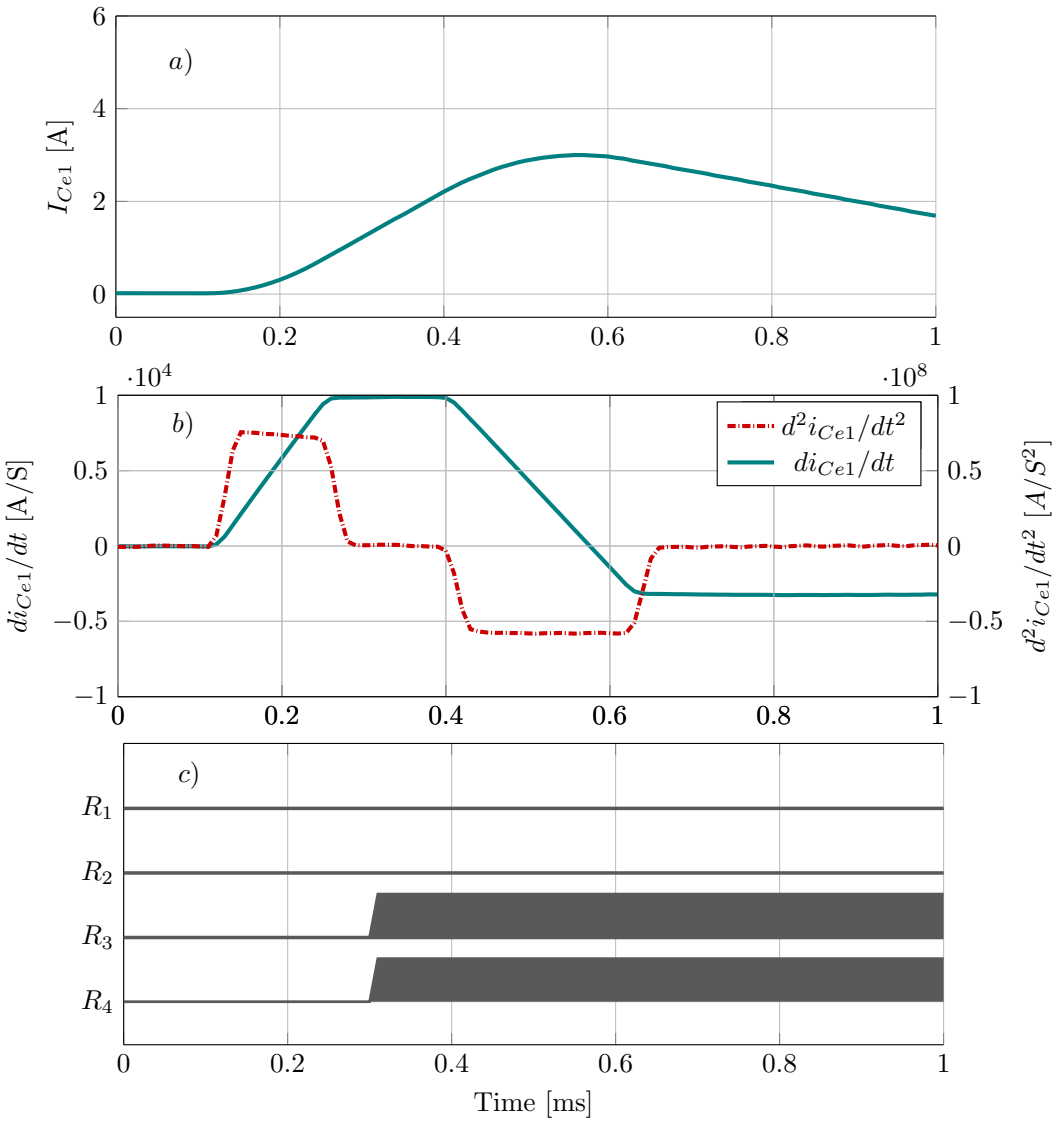


Figure 5.10: Response of protection system to external fault (solid-earth fault F_2): a) DC current, b) The rate of change of current di/dt and d^2i/dt^2, c) Tripping signals.

B) Protection against high-resistance earth faults

In this section, the developed DC protection algorithm is assessed in the case of high resistance faults. Typically in LVDC microgrid fault resistance is from solid to 10 Ω [214, 215, 216, 217] where a 2 Ω has been conceived as high-resistance fault and 10 Ω is classed as a very high-resistance fault [218]. For this purpose, a pole-to-earth fault with fault resistance of 2 Ω [217] is simulated for both internal and external faults as following:

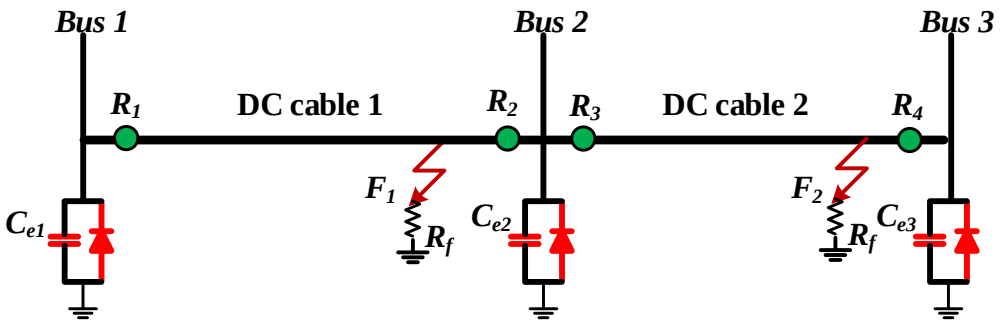


Figure 5.11: Simplified diagram of an LVDC cable under high-resistance faults being applied on cable 1 (Fault 1, F_1) and cable 2 (Fault 2, F_2).

B-I) Internal fault location

An internal fault, F_1, is triggered at the end of the cable 1, as illustrated in Figure 5.11, and the response of the protection system for this fault is depicted in Figure5.12. The DC current amplitude in this case is reduced due to the effect of the high resistance fault (refer to Figure 5.12(a)), however, the detection algorithm is initiated even with this reduced fault current. It should be noted that the value of the first derivative of the current changes instantly and reaches a high value at the occurrence of the fault (refer to Figure 5.12(b)). Since the discriminatory algorithm does not depend on the magnitude but rather the sign of the second derivative of the current, the algorithm classifies the fault as internal (the sign of the $d^2 i_{Ce1}/dt^2$ is negative). Therefore, a tripping command will initiate to the relays R_1 and R_2 connected to the faulted feeder (refer to Figure 5.12(c)) to clear and isolate the DC fault. This confirms that the proposed method is robust against fault current levels, extremely important in such cases of highly resistive faults.

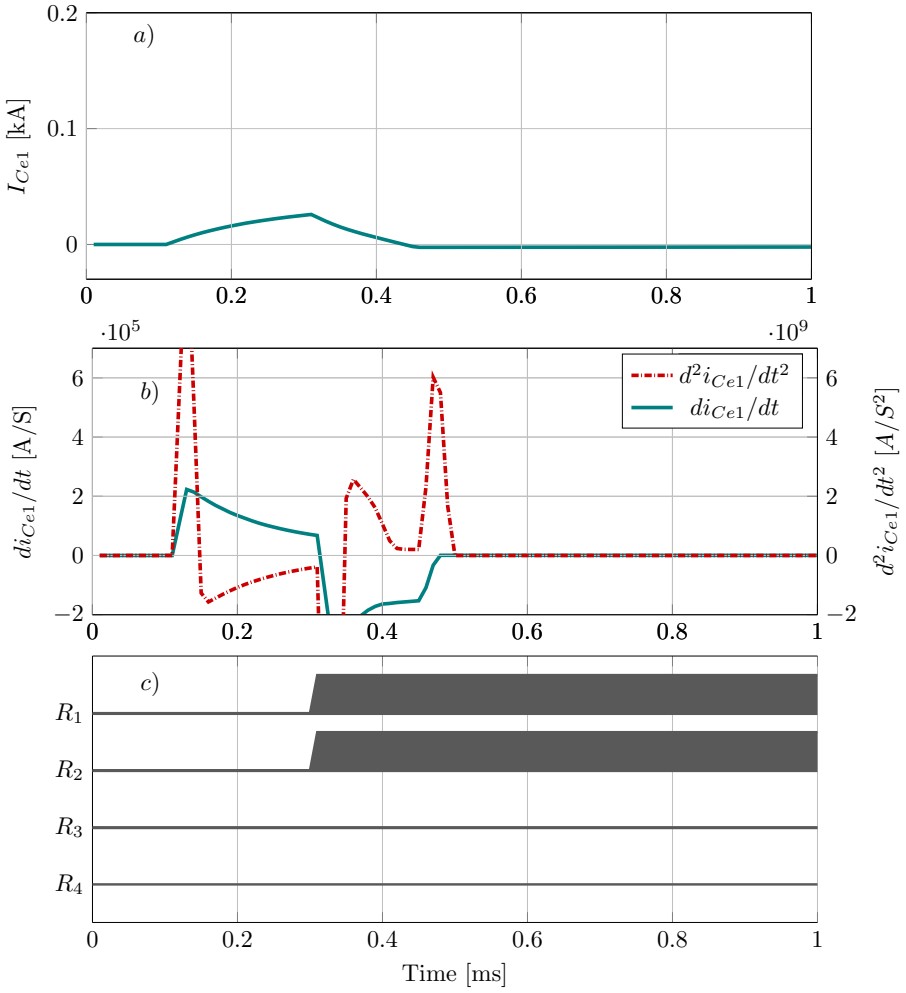


Figure 5.12: Response of protection system to internal fault (high resistance-earth fault F_1): a) DC current, b) The rate of change of current di/dt and d^2i/dt^2, c) Tripping signals.

B-II) External fault location

A high-resistance pole-to-earth fault, F_2, with respect to relays R_3 and R_4 is triggered at the end of cable 2 (refer to Figure 5.11). The response of the protection system for this fault is depicted Figure 5.13. After the fault is triggered at $t = 0.1$ ms, DC fault current is analysed with respect to the relay, R_1, which is external to the faulted feeder (refer to Figure 5.13(a)). The positive sign of the second derivative of the current, d^2i_{Ce1}/dt^2, indicates that the fault is external, (refer to Figure 5.13(b)) which is consistent with the theoretical analysis introduced in (5.8). In this case the voltage drop across the line is less than 2%. It is also interesting to observe that the value of the di_{Ce1}/dt continues to increases no matter the effect of the fault resistance on the DC current. The response of the protection system is controlled when the second derviative reverts to a negative

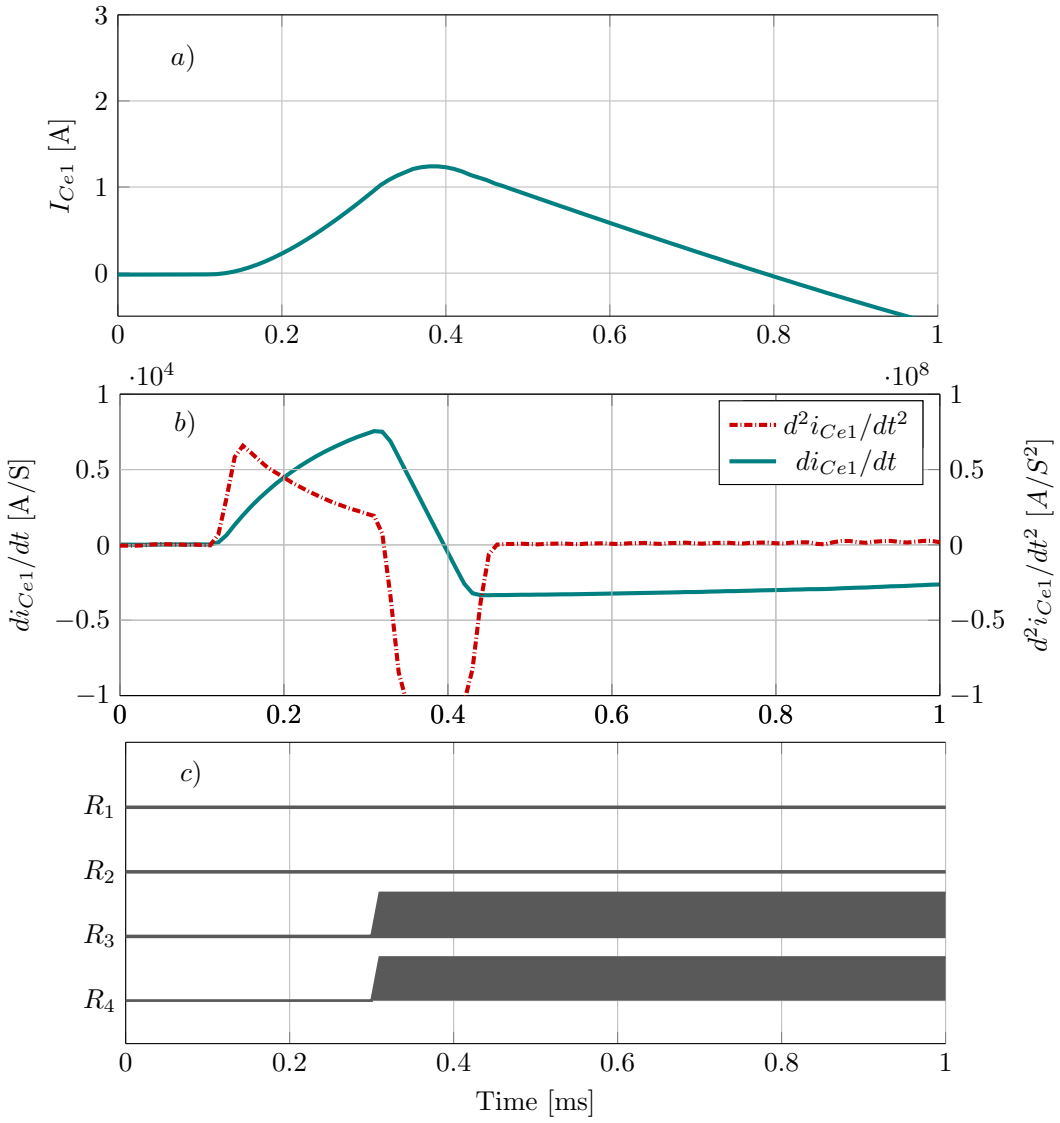


Figure 5.13: Response of protection system to external fault (high resistance-earth fault F_2): a) DC current, b) The rate of change of current di/dt and d^2i/dt^2, c) Tripping signals.

value and the discriminatory algorithm will not initiate a tripping command to relays R_1 and R_2 for isolation as depicted in Figure 5.13(c), since the previous three sample points of the current of the second derivative (d^2i_{Ce1}/dt^2) are monotonic. It is clear that the sensitivity of this algorithm is not affected by the fault resistance (R_f=2Ω) but instead is largely dependent on the resulting sign of the second derivative of the current following the detection of the current transient.

Test case 2: Performance during Islanded mode

The performance of the proposed protection scheme in an islanded LVDC microgrid is also scrutinised in this chapter, in order to appraise the robustness of the proposed scheme in the islanded mode of operation.

A) Protection against solid earth faults

An internal solid pole-to-earth fault with respect to relays R_3 and R_4, F_2, is applied at the end of the cable 2 after the point of common coupling (PCC) switch is disconnected from the main grid (refer to Figure5.7). Once the LVDC microgrid is disconnected from the grid, the LVDC microgrid is controlled through a droop control-based strategy to facilitate the transition from grid-connected mode to islanded mode. The response of the protection system for this fault scenario is illustrated in Fig.5.14. The DC currents

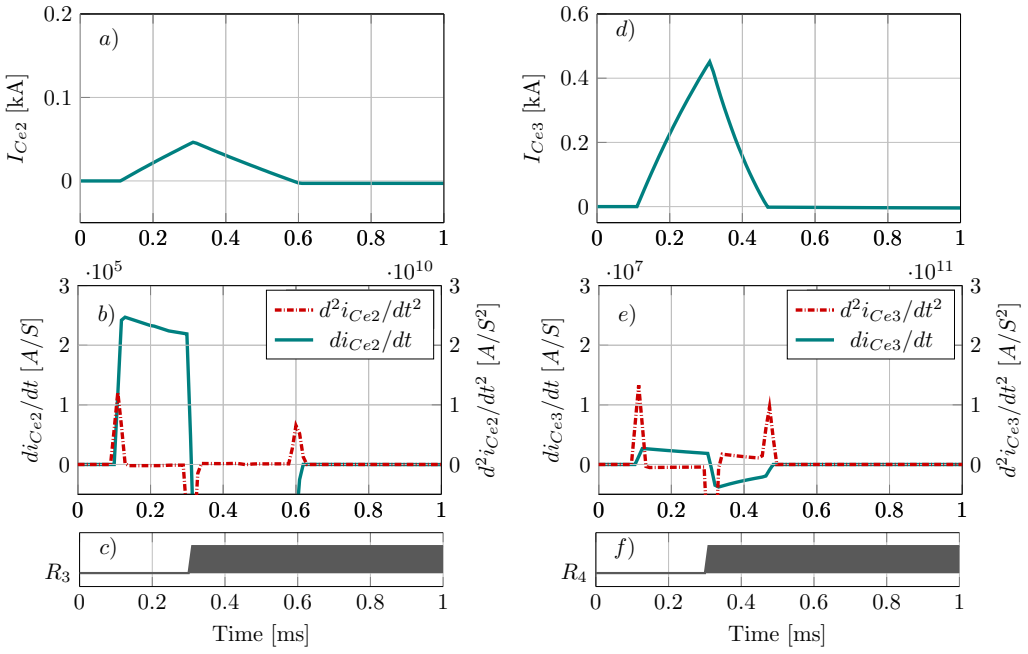


Figure 5.14: Response of protection system during islanded mode to an internal fault (solid earth fault F_2): (a,d) DC currents of I_{Ce2} and I_{Ce3} respectively, (b,e) The rate of change of currents di/dt and d^2i/dt^2, (c,f) Tripping signals of R_3 and R_4 respectively.

from both relay nodes (e.g. relays R_3 and R_4) are seen to rise during fault occurrences (refer to Fig.5.14 (a,d)). The fault current flowing from the R_4 is of higher magnitude. This is because the fault is positioned close to R_4. Following the incidence of DC faults the rate of change of current experience an increase. These values are fed into the protection algorithm and the sign of the second derivative of the current is verified. Due to the sign of the d^2i_{Ce2}/dt^2 and d^2i_{Ce3}/dt^2 for both relays being negative (refer to

Fig.5.14(b,e)), the fault can be rendered as internal. Consequently, a tripping command initiates to relays R_3 and R_4 connected to the faulted feeder (refer to Fig.5.14(c,f)) to clear and isolate the DC fault.

B) Protection against high-resistance earth faults

An internal fault with respect to relays R_3 and R_4, F_2, with fault resistance of 2 Ω is applied at the end of the cable 2 after the point of common coupling (PCC) switch is disconnected from the main grid (refer to Figure 5.7). As observed in Fig 5.15, DC currents from both relays are seen to increase (refer to Fig.5.15(a,d)), indicating that the fault current flowing from R_4 has higher magnitude as the fault occurs located close to R_4 with a short distance. The distinctions between this case and the pervious case where the magnitude of the current is decreased due to the influence of the fault resistance. However, the discriminatory algorithm does not rely on the magnitude, but rather on the sign of the second derivative of the current. Since the sign of the d^2i_{Ce2}/dt^2 and d^2i_{Ce3}/dt^2 for both relays are negative (refer to Fig.5.15(b,e)), the algorithm classifies the fault as internal. Accordingly, a tripping command initiates to relays R_3 and R_4 connected to the faulted feeder (refer to Fig.5.15(c,f)) to clear and isolate the DC fault.

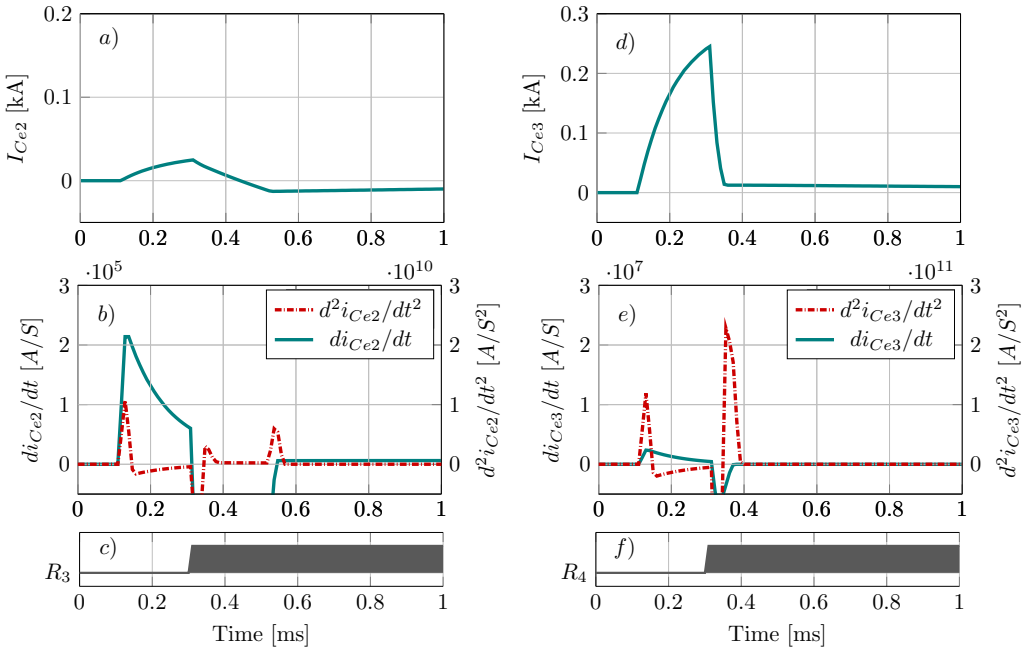


Figure 5.15: Response of protection system during islanded mode to an internal fault (high resistance-earth fault F_2): (a,d) DC currents of I_{Ce2} and I_{Ce3} respectively, (b,e) The rate of change of currents di/dt and d^2i/dt^2, (c,f) Tripping signals of R_3 and R_4 respectively.

Test case 3: The impact of measurement noise on the performance of the proposed method

The proposed protection method is assessed with signal noise added to demonstrate the practical applicability of the method.

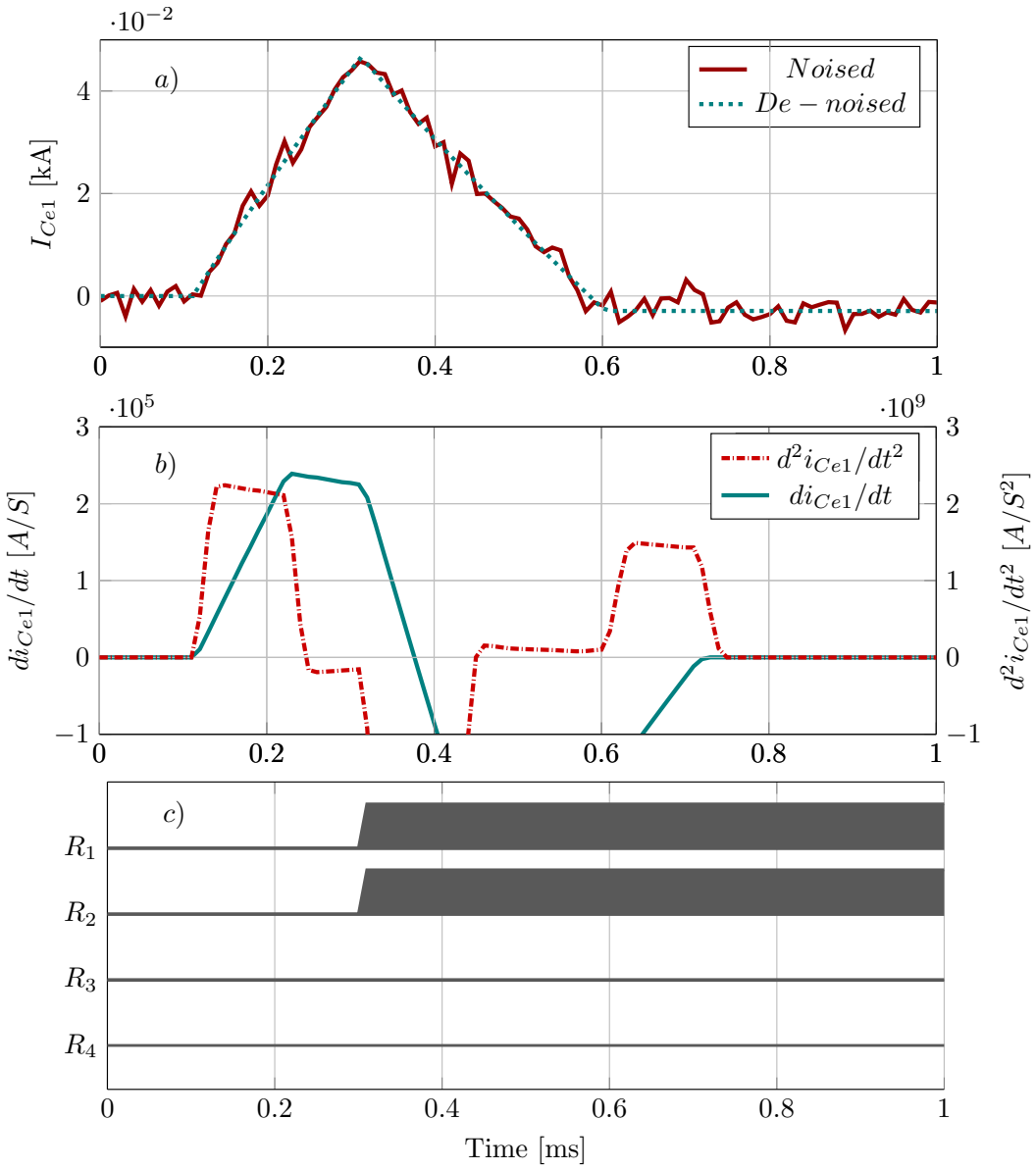


Figure 5.16: Response of protection system with noise to internal fault (solid-earth fault F_1): a) DC current, b) The rate of change of current di/dt and d^2i/dt^2, c) Tripping signals.

Frequently, noise can interfere with the protection function due to several factors such as measurement devices. For this purpose, the current signals at the two ends of

the respective feeder are contaminated by white Gaussian noise with SNR of 20 dB, generated using MATLAB. Generally, signals contaminated with noise are mitigated by utilizing de-noising methods. As such, a moving average low pass filter with three-sample time window has been integrated to filter the noisy DC fault current signal before evaluating the first and second derivatives of the current in order to avoid a false triggering. The response of the protection scheme for this level of noise is depicted in Figure 5.16(a)). The negative sign of the second derivative d^2i_{Ce1}/dt^2 indicates that the fault is internal,(refer to Figure 5.16(b)), and thus, a tripping command initiates to the relays R_1 and R_2 connected to the faulted feeder (refer to Figure 5.16(c)) to clear and isolate the DC fault. In this scenario, the protection method is capable of determining the faulted section despite the noisy environment. In practice, the protection technique can be further improved by analysing the sampling frequency and using advance filtering design to increase the quality of this technique against the impact of noise [240].

5.4.3 Discussion of simulation results

The proposed protection method has been established in this chapter using a multiple capacitive earthing scheme. The sign of the second derivative of the current has been used to classify the fault as internal or external, and the relay has been triggered in response to the fault. The proposed protection scheme efficiently protects both grid connected and islanded LVDC microgrid without the need to change the protection relay current settings. In addition, in the presence of noise in the measurement signal, the proposed protection method successfully detected the fault and effectively disconnected the faulty cable. To ensure an effective protection scheme, performance requirements must take into account the speed of operation, and protection functional requirements such as sensitivity, security, selectivity, and robustness. In terms of sensitivity, the proposed protection scheme is capable of detecting faults within the protected zone, including those with a high resistance. In terms of speed, the proposed protection scheme is capable of interrupting faults quickly enough to prevent equipment damage. In terms of security (i.e stability) the proposed method utilizes the initial natural response of the earthing capacitor current signatures during ground faults. Therefore, the influence of sudden load changes or non-fault conditions will not affect the performance of the proposed method. This is because the voltage across the earthing capacitor will not jump immediately and will change very little during load steps (they will however affect the DC-link capacitors of the converters). The earthing capacitor will be charged by current when a closed loop circuit to ground is initiated during ground faults. Thus, load steps or non-fault conditions will not significantly affect the detection procedure of the proposed method. In spite of this technique's effectiveness, the high sampling

rate of sensors used to measure the current derivative amplify noise and could result in false tripping. Table 5.2 shows the comparison of the proposed method with existing techniques that can detect and isolate a fault on the cable. As observed from Table 5.2, the proposed protection method has the shortest operating detection time among well-known existing current based protection studies on LVDC microgrid. The proposed method and [235], [207],[234] are communication-less which means they prevent the issues associated with data loss and latency in the communication link. Furthermore, unlike any of the other methods in the literature, the proposed method was evaluated in both grid-connected and islanded modes and does not require threshold calculation for different microgrid topologies. Simultaneously, as compared to other observed methods, the proposed method provides fast fault detection and isolation when the noise measurement signal of 20 dB is taken into consideration. Finally, the cost evaluation is based on the extra hardware circuitry needed to detect the fault, such as interfacing diode, and inductor which increases the total cost of the protection scheme. As a results, the proposed method is regarded as comparatively inexpensive when compared to other methods described in the literature. The above points clearly highlight the various benefits and overall effectiveness of the proposed method over other existing current based techniques.

Table 5.2: Qualitative assessment of the existing fault protection methods

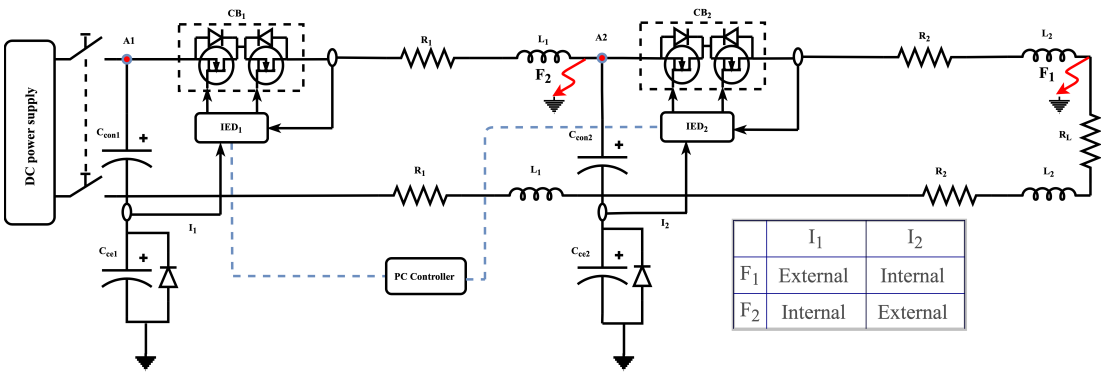
Study	[235]	[207]	[229]	[234]	Proposed method
Fault detection time [ms]	<1	<5	<2	<2	<0.2
Communication required	No	No	Yes	No	No
Threshold calculation required	Yes	Yes	Yes	Yes	No
Both grid and islanded modes consideration	No	No	No	No	Yes
Noise sensitivity	High	High	High	High	Moderate
Cost	Medium	High	Medium	High	Low

5.5 Practical validation of the proposed DC protection strategy

In this section, the experimental validation of the proposed protection method was conducted with the intention of verifying the effectiveness of the proposed protection method (fault detection and discrimination capabilities) in order to distinguish both internal and external faults within the actual noise signal captured by the DC current transducer in the laboratory environment. A scaled DC laboratory demonstrator has been utilized for replicating transients fault.

5.5.1 Experimental setup

The LVDC microgrid depicted in Figure 5.7 is simplified and scaled down using the low-power test demonstrator and is shown in Figure 5.17 (a photograph of the actual experimental layout is presented in Figure 5.18). The main VSC and associated filtering capacitor are represented by a DC source connected in parallel with a capacitor (shown in Figure 5.17), where the latter is used to supply transient fault current. Multiple capacitive earthing schemes are connected at the negative pole. The DC currents are measured using Hall-effect sensors [225]. Four antiparallel MOSFETs are used as solid-state DC breakers to clear the fault-currents. The fast earth-faults are created artificially by controlling the gate driver [226] of a MOSFET connecting the DC cable directly to earth. All measuring sensors are interfaced to the Intelligent Electronic Devices (IEDs) which are emulated on a National Instrument (NI) CRIO-based FPGA [227] used for data logging as well as generating the gate signals to turn-on or off the MOSFETs. The parameters of the hardware used for the experimental setup are provided in Table 5.3



	I_1	I_2
F_1	External	Internal
F_2	Internal	External

Figure 5.17: Schematic diagram of the experimental arrangement.

Table 5.3: Circuit parameters of the experimental arrangement.

V_{dc} [V]	C_{con} [mF]	C_e [mF]	*MOSFET*	*Diode*	$R_{1,2_{line}}$ [Ω]	$L_{1,2_{line}}$ [mH]	$Cable_{1,2_{length}}$ [km]	R_L [Ω]
15	3.3	3.3	Rated 100 V/200 A	5.8 V	0.04	2.5	1	5

5.5.2 Experimental testing and results

The test circuit shown in in Figure 5.17 is energised at 15 V, to remain with the safe operating range of the DC rig (±15). Two 2.5 mH inductances are selected to represent the DC cables, corresponds to a 1 km length for each cable. In order to evaluate the effectiveness of the proposed protection method in addressing the effects of high fault

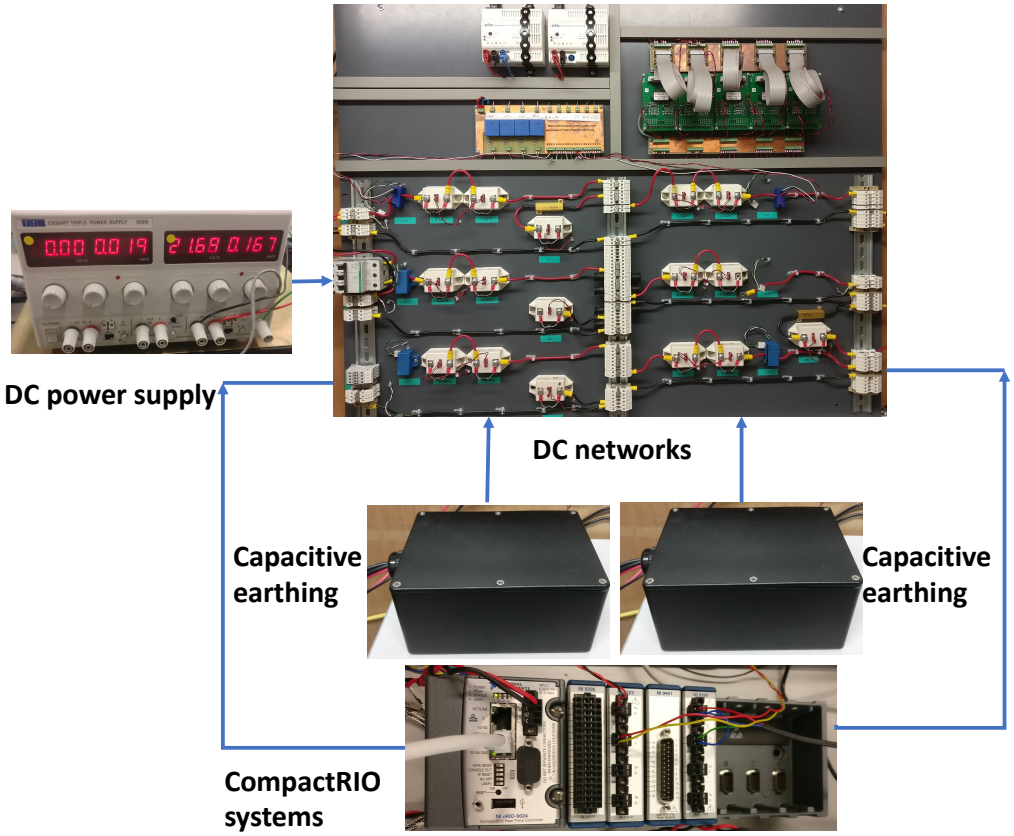


Figure 5.18: Laboratory experimental setup.

resistance, a pole-to-earth fault with a high fault resistance of 1 Ω is created artificially at the end of the second DC cable as shown in Figure 5.17. The experimental results corresponding to this fault are presented in Figure 5.19. The current measurement data is acquired from the experimental setup with a sampling rate of 5 kHz in order to test the effective of the proposed protection method under low sampling frequency. These measurements have been utilized and the corresponding first and second current derivatives are calculated at each time interval. Consequently, the calculated first and second current derivatives are assigned to the proposed algorithm to discriminate between the internal and external fault currents by analysing the sign of the second current derivative. When the fault occurs at $t = 1$ ms at the end of the second DC cable, the earthing capacitor current measurements I_1 and I_2 are analysed (refer to Figure 5.19(a),(d)). The last stage of the algorithm verifies that the previous three sample points of the current of the second derivative (d^2I_1/dt^2) are monotonic and the sign of the following one sample point is positive (refer to Figure 5.19(b)) which is consistent with simulation results explained previously. As a result, the discriminatory algorithm subsequently classifies the fault as external and no tripping signal is initiated for the

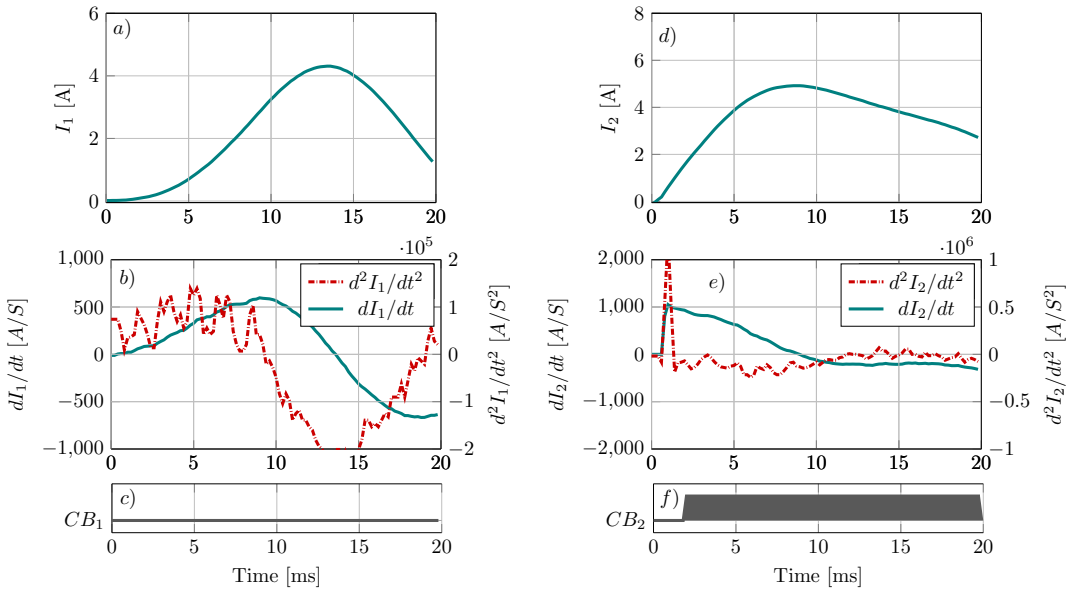


Figure 5.19: Experimental results: (a,d) External DC current I_1 and internal DC current I_2 respectively, (b,e) The rate of change of currents di/dt and d^2i/dt^2, (c,f) Tripping signals of CB_1 and CB_2 respectively.

circuit breaker (CB_1) (refer to Figure 5.19(c)). At the same time, the DC current I_2 experiences a rapid increase in current from the earthing capacitor connected to the faulted feeder (refer to Figure 5.19(d)). The discriminatory algorithm subsequently classifies the fault as internal since the previous three sample points of the current of the second derivative (d^2I_2/dt^2) are non-monotonic and the sign of the following one sample point of the second derivative of the current is negative (refer to Figure 5.19(e)). Therefore, the algorithm in this instance will initiate a tripping command for the circuit breaker (CB_2) connected to the faulted feeder (refer to Figure 5.19(f)) to clear and isolate the DC fault.

5.6 Chapter 5 Summary

This chapter has identified the specific protection challenges of LVDC microgrid especially the limited fault current during the islanded operating mode and detecting a high fault resistance earth fault, all of which can pose a safety issue for LVDC microgrid. The appropriateness and limitations of existing current-based methods for discriminating between LVDC internal and external faults and ensuring a high degree of protection in grid-connected and islanded modes have been underlined.

On this basis, this chapter has proposed a novel communication-less protection scheme capable of detecting and locating DC faults even at limited fault levels. To accurately locate and isolate DC faults, the proposed approach relies entirely on local measurements (i.e. current measurements) during the fault. A mathematical model of a generic faulted feeder for a LVDC microgrid is developed and used by a DC protection algorithm based on DC current concavity (sign of d^2I/dt^2) that can discriminate between internal and external faults. The proposed scheme has been shown to provide discriminative, sensitive, and fast protection under pole-to-earth faults (solid and high resistance faults), while remaining stable during external faults. It is also demonstrated that the proposed protection scheme is not dependent on the magnitudes of fault current signatures, but rather on the sign of the current's second derivative. The proposed scheme effectively protects both grid-connected and islanded DC microgrid operations without requiring protection settings to be changed. Furthermore, the scheme's performance is validated for high resistance faults (R_f=2 Ω) and for DC current signals contaminated with noise, indicating the method's versatility and robustness. Finally, the feasibility of the proposed method is verified by an experimental model that provides laboratory characterisation of LVDC microgrid fault behaviours.

Chapter 6

Conclusions and Future Work

6.1 Summary

At the moment, LV distribution networks are under pressure to accommodate an increasing number of low-and-zero carbon technologies. In light of recent advancements in power electronic converters and the growing number of applications that are inherently powered by DC systems, as well as recent power grid failures in some countries as a result of natural disasters or severe weather, a number of industrial and research organisations have identified LVDC microgrids as a preferred solution for alleviating this pressure on hosting an increasing number of low-and-zero carbon technologies. However, according to a number of research studies and industrial groups, the primary outstanding LVDC microgrid technical challenges are the implementation of effective earthing systems, reliable and accurate fault location, and enhanced DC protection solutions. This thesis addresses a number of predominant issues regarding the fault location and protection of LVDC microgrids.

In particular, the work addresses the earthing systems, fault location estimation, and DC protection of an LVDC microgrid that is interfaced to the AC grid through a two-level VSC converter, this architecture being chosen due to its simplicity and low cost. However, one of the complexities involved in protecting a VSC-based LVDC microgrid is rapidly detecting and extinguishing DC fault current. This is because the typical two-level VSC's DC fault current withstand rating is only twice the converter full-load current. Therefore, implementing existing AC protection strategies (i.e., overcurrent protection schemes) for the LVDC microgrids will be insufficient to ensure safe and secure operation in the future. Additionally, the integration of renewable energy sources into LVDC microgrids will have a significant impact on the accuracy and reliability of fault distance estimation as existing fault location techniques rely on additional hardware to locate a fault. Thus, increasing the network's cost and requiring a repair

crew to relocate external equipment, while others rely on the communication between the converters, implying a reliability issue if the communication channel is lost. These issues have a significant impact on post-fault recovery efforts, such as cable section replacement and network reconfiguration.

To this end, this thesis presents a novel fault location technique and a novel protection scheme that facilitate the use of LVDC microgrids in a broader range of applications:

(I) Novel fault distance estimation utilising multiple capacitive earthing schemes that improves accuracy regardless of whether a DC source or load is connected to the remote end,

(II) Novel current-based fault detection and isolation technique that enhances protection selectivity to effectively discriminate between internal and external faults, under both grid-connected and islanded modes.

The performance of the proposed fault location and protection techniques have been verified by MATLAB/Simulink simulations and laboratory experiments.

The following sections expand on the important contributions to new knowledge achieved by this research and identify the areas worth taking forward as future work to enhance the collective understanding of the LVDC microgrids and the development of earthing and protection schemes.

6.2 Conclusions

The contributions from the work undertaken throughout this thesis can be attributed to three distinct knowledge streams. The following sub-sections present the contributions to each stream in detail.

6.2.1 Earthing configurations in LVDC microgrids

This thesis addressed a knowledge gap in the development of a robust and effective earthing scheme capable of ensuring the safe and secure operation of LVDC microgrids. This includes:

- A new in-depth review of earthing configurations and earthing devices compatible with LVDC microgrids.
- Identification and analysis of the effect of various earthing strategies on pole-to-earth fault currents, and leakage currents, that reveals new insight into human and equipment safety.

- Evaluating and providing a comprehensive review of the advantages and disadvantages of LVDC microgrid earthing strategies.

The system response of an LVDC microgrid with different earthing devices to a pole to earth fault is investigated through detailed simulation of an LVDC network modelled in the PSCAD software. The study's findings indicate that, firstly, unipolar solid earthed systems generate a significant amount of fault current, necessitating rapid detection and isolation of faults. Secondly, unipolar high-resistance earthed systems generate a small fault current from the first pole to the earth fault. In this case, the system can continue to operate. However, fault clearing action is required because a second fault may form, resulting in a pole to pole fault with a significantly large fault current. Therefore, insulation monitoring devices are required for this type of earthing scheme. Thirdly, earthing LVDC microgrids with a capacitor in parallel with the diodes is the most appropriate configuration. This is because the capacitor prevents circulating DC earth current during normal operation (i.e. minimising corrosion) and has a low impedance when a transient fault occurs (i.e. the voltage across the diodes exceeds some threshold value). These findings are considered as a necessary first step toward the development of protection methods that incorporate appropriate earthing schemes to enable safe and secure LVDC microgrid operation.

Additionally, to address the difficulties associated with the system being un-earthed during islanded modes, this thesis considers the use of multiple earthing points to detect DC faults and ensure public safety. On that basis, a detailed fault characterisation using multiple earthing points (i.e. capacitive earthing scheme) for LVDC microgrids operating in grid-connected and islanded modes was performed. This enables a better understanding of the system's behaviour when the LVDC microgrids are earthed with multiple earthing points during grid-connected and islanded modes, allowing for the design of effective protection solutions. The analysis was conducted while considering the DC fault characteristics from the converter's perspective while implementing a capacitive earthing scheme in an LVDC microgrid, and the following were the main conclusions:

- When the LVDC microgrid is disconnected from the main grid, the fault current level decreases by a third, resulting in a fault current that is insufficient to trigger the protection device. As a result, protecting an LVDC microgrid under faulted conditions in islanded mode with a single protection relay setting is insufficient.
- Multiple earthing schemes (using capacitors connected in parallel with diodes) provide distinct responses to different faults and locations, which is a significant advantage when developing fault location and protection schemes.

Crucially, the comprehensive fault characterisation presented in Chapter 3 was utilised to develop a novel protection scheme capable of protecting the LVDC microgrids in both operational modes (grid-connected and islanded modes).

6.2.2 Fault location methods based on capacitive earthing with enhanced accuracy

The accuracy of fault location is of major importance in the LVDC microgrids as it will enable faster system restoration, diminish power outage time, and thereby enhance the overall reliability of the system. Therefore, two novel fault location estimation techniques have been developed that successfully apply to LVDC microgrids through the use of the capacitive earthing scheme. The proposed methods are capable of accurately estimating the faulted segment of a cable over a wide range of fault resistance and cable length. The first proposed method, which combines the least squares method with a moving average and Savitzky-Golay filters, provides a more accurate estimation of fault location than the initial di/dt measurement method. For example, when the fault resistance is 0.1 Ω, the estimated location of the fault is relatively accurate (0.3 %, with the fault applied in the middle of the feeder), in comparison to the initial di/dt measurement method, which results in a significant error in estimating the fault location (8.6 % , the fault applied at the middle of the feeder). Combining the least squares method with a moving average and Savitzky-Golay filters significantly reduces fault estimation errors, as demonstrated by the simulation results. The second proposed method is capable of successfully estimating the fault distance and associated fault resistance regardless of whether the remote end is connected to a DC source or a DC load. The simulation results demonstrated that the proposed algorithm was capable of estimating fault distances for both low- and high-resistance faults (with R_F values ranging from 0.1 to 2 Ω). Even when the fault resistance is high, the proposed algorithm's accuracy in fault localization is nearly constant. When the fault resistance is 2 Ω, for example, the maximum error in fault estimation is 2% (calculated using the locator unit FLE_1). When compared to existing fault location methods, this proposed method has the following advantages:

- This proposed technique has been shown to be capable of accurately estimating the faulted segment of a feeder connected between multiple DC sources, such as those found in an LVDC microgrid, even in the presence of highly resistive faults.
- In LVDC microgrids with multiple sources and DC loads, this proposed method considered the impact of fault resistance on the estimation of fault location.
- The proposed method has been experimentally validated by utilising a capacitive

earthing scheme and relying entirely on local measurements (i.e. voltages and currents) during a DC fault to determine the fault location and associated fault resistance.

To the end, the proposed methods require no additional hardware (i.e. signal injection) and are communication-less, rendering them a relatively inexpensive methods. The enhanced accuracy enables accurate estimation of the fault distance and expeditious post-fault cable maintenance, even when various converters are installed at each end of a cable.

6.2.3 Fault detection and isolation in LVDC microgrid networks with capacitive earthing

This thesis proposes a novel current-based non-unit protection scheme for VSC-connected LVDC microgrids based on multiple capacitive earthing schemes in order to address the limitations of existing current-based protection schemes. Chapter 5 revealed that existing current-based protection schemes lack effective fault discrimination between internal and external faults in grid connected and islanded modes, are more susceptible to resistive faults, and are based on current magnitude. Rendering the network protection incredibly challenging whilst in islanded mode. Therefore, to overcome these issues, the proposed scheme has the following advantages when compared with existing current-based protection methods:

- The proposed protection scheme enhances selectivity by effectively discriminating between internal and external faults in both grid-connected and islanded modes, as it incorporates the sign of the current's second derivative (sign of d^2I/dt^2).
- The proposed protection scheme is communication-less, fast acting under pole-to-earth faults (solid and highly resistive) and discriminatory.
- The proposed protection scheme does not depend on the magnitude of fault current signatures, but rather on the sign of the current's second derivative. Thus, it eliminates the need for selection of different protection settings for different LVDC microgrid operation modes.

Additionally, the proposed scheme's performance is validated for high resistance faults (R_f=2 Ω) and for DC current signals contaminated with noise, indicating the method's versatility and robustness. The simulation results demonstrate that the developed protection scheme is capable of reliably detecting and locating DC faults within a faulted LVDC microgrid network interfaced by VSC. This proposed protection scheme is capable of detecting DC faults in less than 100 μs. Given the rapid response time

of the DC protection scheme, DC faults have the potential to be interrupted at an early stage, resulting in less short circuit stress on the system. Finally, the feasibility of the proposed method is demonstrated using an experimental model that provides laboratory characterisation of DC microgrid fault behaviours.

6.3 Future Work

This thesis has tackled four complementary themes that work together to deliver appropriate, cost-effective, robust and versatile fault location and protection methods in LVDC microgrid distribution systems. Based on the findings and conclusions of the work undertaken, areas of future work have been identified in order to further the collective understanding of fault location and protection methods in LVDC microgrids:

6.3.1 Development of islanding detection method for LVDC microgrids

Passive, active and communication-based approaches have been widely used in the development of unintentional islanded events in AC distribution networks. However, there is a lack of their utilization for solving the islanding detection problem in LVDC microgrids. It is suggested that the potential merits can arise from the utilization of hybrid islanding detection methods for LVDC applications. Hybrid islanding detection methods can be used mainly for detection of unintentional islanded events where the time is not critical and the discriminatory capability is essential.

6.3.2 Development of back-up protection scheme

The proposed protection method presented in Chapter 5 is considered as primary protection. The literature review has shown that the majority of research is only addressing the primary protection. Consequently, there is a need to shift attention toward a backup protection system for a LVDC microgrids.

6.3.3 Further investigation of implementing capacitive earthing scheme on different network topologies

The proposed protection and fault detection scheme presented in this thesis used a LVDC microgrid unipolar topology. However, further investigation should be carried out considering LVDC microgrid bipolar topologies. Furthermore, the capacitive earthing scheme (outlined in Chapter 3) should be implemented in a bipolar topology in order to understand fault characteristics. This will, in turn, establish the foundation for the design and assessment of fault protection methods in LVDC bipolar topologies.

6.3.4 Further investigation of faults in the AC side

In this thesis, a capacitive earthing scheme has been successfully designed and utilized in locating and protecting a fault on the DC side of the system. However, this capacitive earthing scheme should be investigated further to assess its influence on protection and control when the fault occurs on the AC side.

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