Protection, Fault Location & Control in High Voltage Multi Terminal Direct Current (HV-MTDC) Grids

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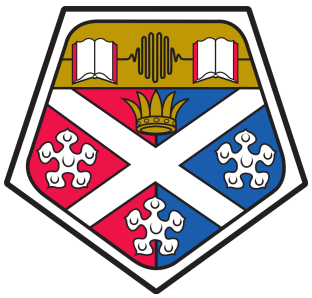

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Abstract

With an increased penetration of renewable energy sources, balancing the supply and demand is likely to be one of the major challenges in future power systems. Consequently, there is a growing need for meshed interconnections between countries in order to effectively share the available power capacity and thereby increase operational flexibility and security of supply. This has been raised as a major issue in Europe but also in Asia and United States of America.

The concept of supergrid has been identified as a possible solution towards a new backbone transmission system, permitting massive integration of renewable energy sources. High voltage direct current (HVDC) links, utilising voltage-source converters (VSCs), are expected to become the preferred technology for the realisation of such a supergrid. This is due to the fact that such systems offer improvements in terms of system stability, lower cost and operational losses. A natural extension of the existing point-to-point HVDC transmission technology is a multi-terminal direct-current (MTDC) system which utilises more than two VSC stations, effectively forming a DC grid. Such a configuration can provide further technological and economical advantages and hence accelerate the realisation of a supergrid. However, technical limitations still exist, and it is not yet a straightforward task to construct and operate an MTDC grid, as several outstanding issues need to be solved. Consequently, it is essential to study, analyse and address potential challenges imposed by MTDC systems in order to enable widespread adoption.

Even though numerous challenges are introduced for the practical implementation of MTDC networks, this thesis deals with the challenges related to the DC-side faults, which is the main issue when considering HVDC technology. DC-side faults in HVDC systems are characterised by large inrush currents caused by the discharge of trapped energy in the system capacitances, escalating over a very short period of time. These include lumped capacitors installed on the DC side of converters, transmission line capacitances, and also the sub-module capacitors contained within modular multi-level converters.

When faults occur in multi-terminal HVDC grids, the DC protection system is expected to minimise the detrimental effects by disconnecting only the faulted section while permitting the remaining healthy part of the grid to continue normal operation. Such requirements introduce the need for transient DC fault characterisation and subsequent development of a discriminative, fast, sensitive and reliable DC protection method. Therefore, one of the main objectives of this thesis is to provide demonstrable solutions to the key challenges involved in protecting MTDC grids, and hence enabling the realisation of HVDC-based supergrids. Two alternative, novel protection schemes are proposed, designed and assessed with the aid of transient simulation. The key advantages of the proposed schemes consist in enhanced reliability, fast fault detection, superior stability, and high level of selectivity. To further validate the practical feasibility of the schemes, small-scale laboratory prototypes have been developed to test the performance of the schemes under real-time fault conditions.

It should be also highlighted that when a permanent fault occurs in an HVDC transmission system, accurate estimation of its location is of major importance in order to accelerate restoration, reduce the system down-time, minimise repair cost, and hence, increase the overall availability and reliability of HVDC grids. As such, another contribution of this thesis is related to the challenges involved in accurate fault location in HVDC networks, including non-homogeneous transmission media (i.e. the lines which include multiple segments of both underground cables and overhead lines). Two novel fault location methods have been developed and systematically assessed. It is demonstrated that the schemes can reliably identify the faulted segment of the line while consistently maintaining high accuracy of fault location across a wide range of fault scenarios. Further sensitivity analysis demonstrates that the proposed schemes are robust against noisy inputs.

In its concluding section, the thesis also outlines a few possible avenues of further research in this area.

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Glossary of Abbreviations

Λ : Grating Period

λ_B : Bragg Wavelength

Ψ : Mother Wavelet

$\Psi^*_{a,b}$: Daughter Wavelet

$A - RCB$: Active Resonance Circuit Breaker

C_ϵ : Strain Sensitivity

C_T : Strain Temperature

CB : Circuit Breaker

$CCSC$: Circulating Current Supression Controller

CFT : Continuous Fourier Transform

CWT : Continuous Wavelet Transform

D_F : Fault Distance

D^*_F : Actual Fault Distance

d_{33} : Longitudinal Piezoelectric Charge Constant

DFT : Discrete Fourier Transform

DWT : Discrete Wavelet Transform

E : Electric Field

FBG : Fibre Bragg Grating

FMS : Fast Mechanical Disconnector

FSM : Frequency Sensitive Mode

$HbCB$: Hybrid Circuit Breaker

HIL : Hardware In the Loop

HTM : Hybrid Transmission Media

$HVAC$: High Voltage Alternating Current

$HVDC$: High Voltage Direct Current

$IGBT$: Insulated gate Bipolar Transistor

L_{seg} : Segment Length

LCC : Line Commutated Converter

LCS : Load Commutation Switch

$LFSM$: Limited Frequency Sensitive Mode

MMC : Modular Multi-level Converter

MOV : Metal Oxide Varistor

$MTDC$: Multi Terminal Direct Current

n_{eff} : Effective Refractive Index

NLC : Nearest Level Control

NPC : Neutral Point Clamped

OHL : Overhead Line

$P-RCB$: Passive Resonance Circuit Breaker

$PD-PWM$: Phase Disposition Pulse Width Modulation

PLL : Phase Locked Loop

$PS-PWM$: Phase Shift Pulse Width Modulation

PWM : Pulse Width Modulation

RCD : Residual Current Disconnector

RES : Renewable Energy Sources

SAr : Surge Arrester

$SCFCL$: Super Conducting Fault Current Limiter

SHE : Selective Harmonic Elimination

SNR : Signal to Noise Ratio

$SSCB$: Solid State Circuit Breaker

$STFT$: Short Time Fourier Transform

$SV - PWM$: Space Vector Pulse Width Modulation

UGC : Underground Cable

v_{prop} : Propagation Speed

VCO : Voltage Controlled Oscillator

VSC : Voltage Source Converter

WT : Wavelet Transform

ZnO : Zinc Oxide

Chapter 1

Introduction

1.1 Introduction to the Research

High Voltage Direct Current (HVDC) power transmission is becoming increasingly competitive compared to high-voltage alternate-current (HVAC) power transmission, especially for bulk power transmission over long distances. This is because of many commercial and technical advantages introduced by HVDC trasmission systems, utilising the most recently developed voltage source converters. Those advantages include bulk power transfer (notably from offshore wind) over long distances [5], upgrading existing AC networks [6], interconnection of asynchronous grids and black start capability [7].

HVDC technology can be formed by two distinctive technologies, namely Line Commutated Converters (LCCs) and Voltage Source Converters (VSCs) [8]. The LCC-based technology has been a key player in bulk power transmission around the world over the last sixty years [9]. However, it is accompanied by some well-known issues (e.g. commutation failure and relatively large reactive power consumption [10, 11]), that have historically limited the applications of HVDC technology. Such limitations have been overcome by the introduction of VCSs which are capable of providing independent control of active and reactive power, immunity to commutation failures, faster dynamic response and connectivity to weak grids [8]. Over the last decade, such technology has become a universally-accepted solution for HVDC transmission due to all the aforementioned dynamic features and operational flexibilities [12]. Those have been achieved by the utilisation of two-level and neutral-point clamped converter topologies [13]. Further improvements with regards to fault blocking capability, semiconductor losses, scalability, improved AC-side waveform quality and elimination of DC-link capacitor, have acceler-

ated the adoption of the so called Modular Multi-level Converters (MMCs) in many of the recent HVDC transmission system projects [14–16].

The majority of presently operational and planned HVDC links are point-to-point with two points of connection with AC networks. These connections are utilised for long distance power transmission within a country or for interconnection between different countries. At present, there is only one MTDC grid in operation located in Zhoushan, China which was commissioned in 2013 [17]. However, with an increased penetration of renewable energy sources (RES), balancing the supply and demand is likely to be one of the major challenges in future power systems [18]. Consequently, there is a growing need for meshed interconnections between countries in order to effectively share the available power capacity and thereby increase operational flexibility and security of supply. This has been raised as a major issue in Europe but also in Asia and United States of America.

Due to several limitations of AC-based transmission (e.g. higher power losses for long transmission lines, skin effect, high charging currents and prohibited interconnection of asynchronous grids [19]), the utilisation of meshed DC grids is considered one of the viable options for the aforementioned interconnections. Specifically, Figure 1.1 illustrates the cost and losses distribution for AC and DC-based power transmission. Even though DC systems require higher initial cost and impose larger terminal losses, after a 'critical distance' the transmission of power is more beneficial both in terms of cost and losses.

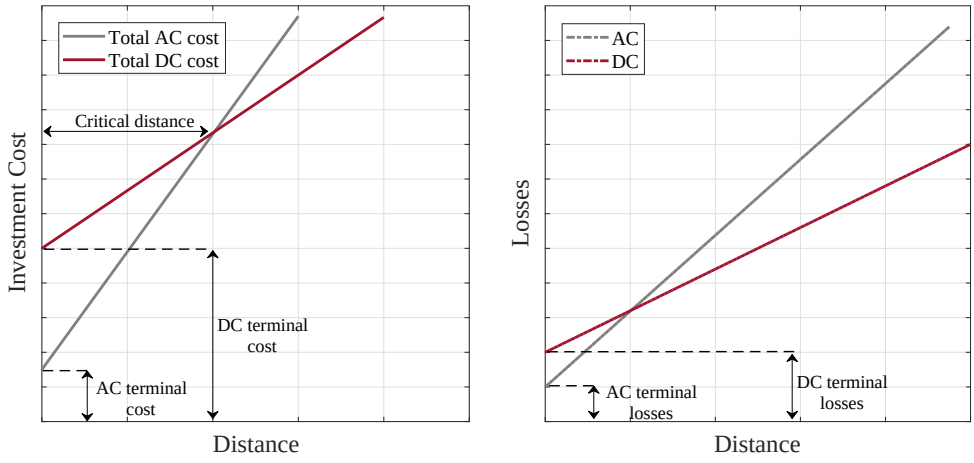
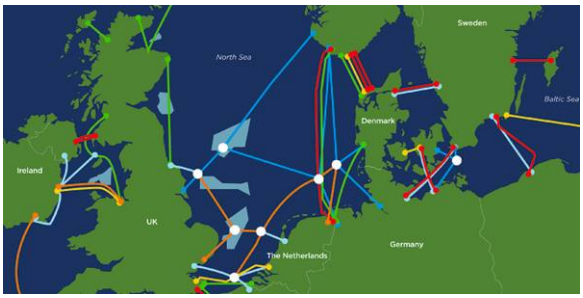


Figure 1.1: Cost and losses curves for AC and DC transmission systems.

To enable more efficient interchange of power and also to harness RES, there is a business case for setting up a European Supergrid. A supergrid can be defined as a transmission backbone which allows massive integration of RES [19, 20]. It has the ability to connect different remote energy sources to an existing grid, offer improved

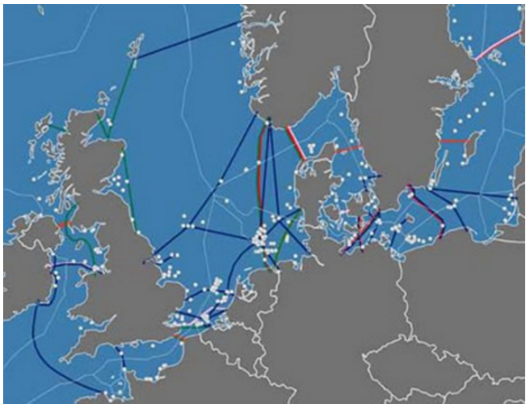
controllability, bring efficient energy balance over a wide geographic spread, and most significantly, allow a more diversified energy portfolio. There are several concepts for the topological setup of such a supergrid, proposed by several organisations which are depicted in Figure 1.2.



(a) Wind Energy Europe [21]

(b) Friends of Supergrid [22]

(c) Airtricity [23]

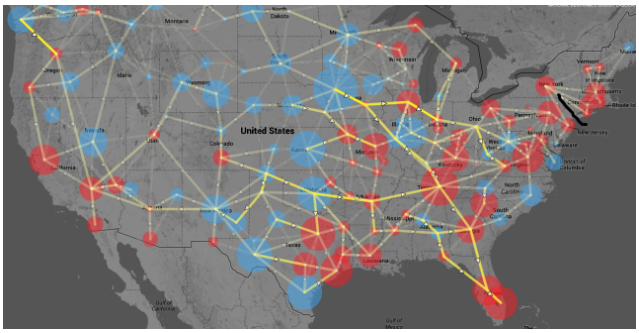


(d) European Commision [24]

Figure 1.2: European Supergrid concepts.

In addition to the Eurpoean Supergrid, there are proposed concepts for setting up supergrids in Asia and United States of America [25], which are shown in Figure 1.3(a) and Figure 1.3(b) respectively.

(a) North-East Asia [26]



(b) United States of America [27]

Figure 1.3: Non-European Supergrid concepts.

It is therefore evident that in many respects the development of a wide HVDC supergrid is an inevitable outcome, especially in Europe due to its leading role in renewables integration. Even though HVDC technology introduces many major advantages (Table 1.1) upon which planned future supergrids are based, it is also accompanied by several technical barriers and challenges. Therefore, the work presented in this thesis is associated with the challenges imposed by DC-side faults.

Table 1.1: VSC HVDC trade-offs.

Advantages	**Challenges**
Interconnection of asynchronous AC grids	DC-side fault management
Flexible integration of RES	Grid code establishment
Fast power flow control	Complex control systems
Connection to weak AC grids	Development of pricing mechanisms
Enhancement of AC system stability	Generation of harmonics
Reduced pylon and cable profile	Compound grounding systems
Long-distances bulk power transfer	Low availability-reliability

1.2 Research Motivation

For the practical implementation and operation of MTDC grids there are several outstanding issues to be solved. Major categories of these include power flow control [28–30], dynamic behaviour and stability [7,31,32], grid and system integration [33–35] and finally fault detection and protection [1,36–38]. Consequently, it is essential to study, analyse and address potential challenges imposed by MTDC systems in order to accelerate their widespread adoption.

DC-side faults is the main issue when considering HVDC technology. This is due to the fact that DC-side faults in HVDC systems are characterised by large inrush currents caused by the discharge of trapped energy in the system capacitances. These include lumped DC capacitors installed on the DC side of the VSCs, transmission line capacitances, and also the sub-module capacitors contained within MMCs. When faults occur in multi-terminal HVDC grids, the DC protection system is expected to minimise the detrimental effects by disconnecting only the faulted section while permitting the remaining healthy part of the grid to continue normal operation. However, DC-side faults escalate over a very short period of time and hence the permissible fault clearance time (detection and isolation) is very short (in the range of 5 ms). This amount of time is

essential to prevent DC voltage collapse and is also subjected to thermal boundaries of power electronic components and limited interruption capability of DC breakers. Such a short fault clearance time is extremely challenging when a meshed DC system is considered and line discrimination (i.e. disconnection of the fault line only) is required. Furthermore, interruption of DC current requires dedicated breakers due to the lack of zero crossing point. As such, longer time delays are introduced which should be taken into account.

Regarding fault-related issues in HVDC grids, according to 'ENTSO-E Code on HVDC Connections and DC-connected Park Modules' [39], HVDC systems (including DC overhead lines), shall be capable of fast recovery from transient faults within HVDC system. In addition to this, it is highlighted that with regard to priority ranking in the area of protection and control, the HVDC system owner shall organise its protections and control devices in compliance with the following priorities, listed in decreasing order of importance:

- Network system and HVDC system protection.
- Active power control for emergency assistance.
- Synthetic inertia, if applicable.
- Automatic remedial actions.
- Limited Frequency Sensitive Mode (LFSM).
- Frequency Sensitive Mode (FSM) and frequency control.
- Power gradient constraint.

It is therefore evident that fault protection is of the highest importance for the healthy operation of HVDC grids. As such, the above-mentioned requirements and challenges introduce the need for transient DC fault characterisation and subsequent development of a discriminative, fast, sensitive and reliable DC protection method. Therefore, one of the main objectives of this thesis is to provide demonstrable solutions to the key challenges involved in protecting MTDC grids and hence enabling the realisation of HVDC-based supergrids.

Additionally, as reported in 'IEEE Guide for Establishing Basic Requirements for High-Voltage Direct-Current Transmission Protection and Control Equipment' [40], along with the HVDC protection equipment, the following important subsystems should interact closely and effectively to implement the required functions:

- DC line fault locator.
- Electrode line monitoring equipment.
- Transient fault recorder.
- Station clock synchronisation equipment.
- Harmonics monitoring equipment.
- Converter valve cooling control and protection equipment.
- DC measuring equipment.

Consequently, fault location is another important function required to run alongside protection. This is due to the fact that after the successful detection and isolation of a fault, and assuming the fault is permanent, accurate estimation of its location is of major importance in order to accelerate restoration, reduce the system down-time, minimise repair cost and hence improve the overall reliability and availability of the transmission system. This is particularly important in the case of a supergrid, where a single disconnection can tremendously affect power exchange between different countries. As such, another major objective of this thesis is to provide solutions towards estimating accurately the location of a DC-side fault.

1.3 Research Methodology

The research presented in this thesis has been undertaken in stages. The overall methodology including the dependencies between different elements of the work are depicted in Figure 1.4.

Initially, a review of HVDC-based transmission was carried out which included the principles of operation and the technology of various components such as converters, network architectures and DC breakers. This was followed by a comprehensive literature survey of the existing and proposed protection and fault location methods, with the aim of identifying possible research gaps (the requirements of protection and fault location in HVDC systems have been identified at this stage).

Specifically, a review of existing and proposed MTDC protection and fault location techniques revealed that much of the reported research focuses on the conceptual aspects but neglects important practical facets (e.g. sampling frequency, time window, breaking capacity and time response of DC interruption devices, processing of digitised signals).

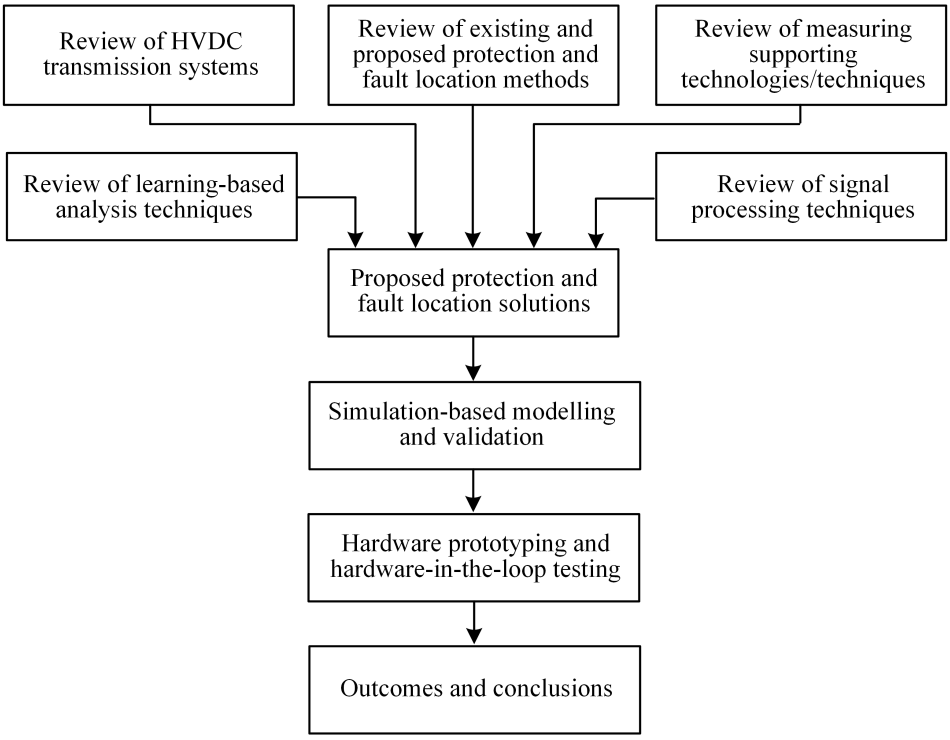


Figure 1.4: Research methodology outline.

Additionally, it has been found that there is no discussion or studies on the practical feasibility of the schemes, and the way measurements and signals exchange can be realised locally (either on a line or busbar) or within a DC substation and different converter terminals.

Further research has been conducted on the available measuring technologies to support real-time monitoring and recording of the system phenomena. Additionally, signal processing techniques suitable for analysis of fast transient phenomena as well as learning-based methods have been evaluated.

Based on the identified research gaps and potential merits arising from the utilisation of certain measuring technologies/techniques, signal processing methods and learning-based analysis approaches, novel protection and fault location solutions have been proposed. Specifically, optical hybrid sensors have been selected to enable distributed current monitoring of transmission lines. Moreover, signal analysis belonging to Wavelet transform group and pattern recognition techniques have been put forward.

The performance of the proposed solutions have been initially validated by simulation-based analysis. It has been found that the utilisation of optical hybrid current sensors and Wavelet-based signal processing can accelerate the performance of protection schemes by enhancing the speed of operation, sensitivity, selectivity and stability. Moreover, it

has been demonstrated that they can enhance the fault location accuracy and assist towards the faulted segment identification when overhead lines and underground cables are combined in one feeder. Further application of machine learning techniques have been found to be useful for reducing the fault location error and hence increasing the accuracy of calculations.

The proposed schemes have been also validated by developing small-scale hardware prototypes and testing them under real-time conditions using hardware-in-the-loop (HIL) testing.

1.4 Principal Contributions

The key contributions of this thesis can be summarised as follows:

- Novel 'Single-ended Differential Protection' scheme based on distributed optical sensing. The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using a scaled-down laboratory prototype. The key advantages have been outlined which result in enhanced reliability, superior stability, and high speed of operation.

- Enhanced 'Travelling Wave-based Fault Locator for Hybrid Transmission Systems' based on distributed optical sensing, suitable for hybrid networks with segments of overhead lines and underground cables. The performance of the scheme has been validated both in detailed transient simulation and laboratory testing. The proposed algorithm has been found to successfully identify the faulted segment of the line while consistently maintaining high accuracy of the fault location estimation.

- Novel 'Centralised Busbar Differential and Wavelet-based Line Protection' scheme which utilises the principles of busbar differential protection and travelling waves. The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using real time, hardware-in-the-loop testing. It has been found that the proposed scheme can provide fast and discriminative protection for busbar and line faults, including both solid and highly resistive.

- Novel 'Single-ended Pattern Recognition-based Fault Locator' which utilises current measurements of hybrid circuit breakers during the interruption process. The fault location method was found to be capable of classifying pole-to-pole and pole-to-

ground faults, while consistently achieving high accuracy of the calculation of fault location.

- Utilisation and practical demonstration of optically-based sensing methods and techniques, suitable for DC voltage and current measurement. Such measuring techniques have been employed to achieve fast line differential protection, fault location based on travelling waves and voltage distribution across the lines.

- A methodology for sizing DC current limiting inductors with respect to the required protection performance, voltage level and highest permissible fault current levels.

- Investigation of IEC-61689 with regards to its suitability for capturing DC-side fast transient phenomena and its applicability for DC protection applications. No such studies have been found in technical literature.

- Characterisation of DC-side faults through systematic evaluation of their dependencies on the converter topology, fault location, ground resistance, fault type and operating condition. No such detailed study had been found in technical literature.

- Investigation and transient performance evaluation of the state-of-the-art DC breakers and VCSs, suitable for DC-side fault studies in MTDC networks.

- Analysis and investigation of signal processing methods explicitly suitable for accurate and fast detection of DC-side fault transients in HV-MTDC networks. The impact of network components, such as current limiting inductors, is also considered in the analysis.

1.5 Thesis Overview

An outline of the work contained within this thesis is presented below:

Chapter 2 reviews the background literature relevant to HVDC grids. The review includes network architectures, converter designs and configurations, transmission lines and alternative grounding options. Additionally, the chapter includes important material related to DC protection such as DC circuit breakers and various techniques for DC voltage and current measurement. The techniques and approaches which enable fast, effective and efficient full-scale modelling of HVDC grids are also described and analysed.

Chapter 3 describes the outcome of a systematic, theoretical as well as simulation-based transient analysis of DC-side faults. The characterisation is carried out considering converter operating stages during DC-side faults, and their dependencies on converter topology, fault type, fault resistance and operating conditions.

Chapter 4 analyses faults in MTDC networks focusing on the fault transient phenomena known as travelling waves. It has been established that the transient-based studies do not depend on the converter topology (or generally on the power source), but rather on the DC network components such as current limiting inductors, cables/lines and DC breakers. For these studies, cables and lines are modelled with a detailed approach, in order to represent all transient phenomena. Additionally emphasis is given to signal processing methods for obtaining a deeper insight into the nature of the faults.

Chapter 5 presents two novel protective solutions for MTDC networks enabling fast, sensitive, reliable and discriminative protection. Simulation and experimental results are presented to verify and support the feasibility of the proposed protection strategies. This chapter also includes an explanation of the optical sensing technology, which is a key enabler for one of the proposed protection methods. Moreover, the practical challenges and requirements with regards to protection in HVDC grids are also discussed.

Chapter 6 describes the principle of operation and assesses two novel fault location algorithms, also developed as part of this research work. The proposed methods aim to accurately estimate the distance to fault in HVDC transmission lines. Transient simulation based studies and experiments are presented, which verify the practical feasibility of the proposed schemes. A few technical challenges related to the distance estimation accuracy requirements are also discussed in this chapter.

Chapter 7 concludes the thesis by summarising and highlighting the key outcomes and contributions resulting from this work. A few potential avenues for future research in this area are also suggested.

1.6 Publications

Journal Papers - Leading author:

- 'Single-Ended Differential Protection in MTDC Networks using Optical Sensors',
  D. Tzelepis, A. Dyśko, G. Fusiek, J. Nelson, P. Niewczas, D. Vozikis, P. Orr, N. Gordon, C. Booth
  IEEE Transactions on Power Delivery
  DOI: 10.1109/TPWRD.2016.2645231

- 'Novel Fault Location in MTDC Grids with Non-Homogeneous Transmission Lines Utilizing Distributed Current Sensing Technology'
  D. Tzelepis, G. Fusiek, A. Dyśko, P. Niewczas, C. Booth, X. Dong
  IEEE Transactions on Smart Grid
  DOI: 10.1109/TSG.2017.2764025

- 'Centralised Busbar Differential and Wavelet-based Line Protection System for MTDC grids, with practical IEC-61869-compliant Measurements'
  D. Tzelepis, A. Dyśko, S. M. Blair, A. O. Rousis, S. Mirsaeidi, C. Booth, X. Dong
  IET Generation Transmission & Distribution
  Accepted, DOI pending

- 'Advanced Fault Location in MTDC Networks utilising Optically-Multiplexed Current Measurements and Machine Learning Approach'
  D. Tzelepis, A. Dyśko, G. Fusiek, P. Niewczas, C. Booth, S. Mirsaeidi, X. Dong
  International Journal of Electrical Power & Energy Systems
  DOI: 10.1016/J.IJEPES.2017.10.040

- 'A New Fault-Ride-Through Strategy for MTDC networks incorporating Wind Farms and Modular Multi-Level Converters',
  D. Tzelepis, A.O. Rousis, A. Dyśko, C. Booth, G. Strbac
  International Journal of Electrical Power & Energy Systems
  DOI: 10.1016/J.IJEPES.2017.04.015

- 'Intelligent Fault Location in MTDC Networks by Recognising Patterns in DC Circuit Breaker Currents During Fault Clearance Process'
  D. Tzelepis, A. Dyśko, C. Booth, Q. Hong
  IEEE Transactions on Industrial Informatics, (Under Review)

JOURNAL PAPERS - CO-AUTHOR:

- 'Challenges, Advances and Future Directions in Protection of Hybrid AC-DC Mircorgrids'
  S. Mirsaeidi, X. Dong, S. Shi, D. Tzelepis
  IET - Renewable Power Generation
  DOI: 10.1049/IET-RPG.2017.0079

- 'A Predictive Control Strategy for Mitigation of Commutation Failure in LCC-HVDC Systems'
  S. Mirsaeidi, X. Dong, D. Tzelepis, S. Shi, M. Said, C. Booth
  IEEE Transactions on Power Electronics, (Under Review)

- 'A Novel Traveling-wave- based Protection Scheme for LCC-HVDC Systems Using Teager Energy Operator'
  W. Hao, S. Mirsaeidi, X. Kang, X. Dong, and D. Tzelepis
  International Journal of Electrical Power & Energy Systems
  Accepted, DOI pending

- 'Fault blocking converters for HVDC transmission: A steady state comparison'
  D. Vozikis, G. Adams, P. Rault, D. Tzelepis, S. Finney
  International Journal of Electrical Power & Energy Systems
  Accepted, DOI pending

- 'Optimal design of a hybrid AC/DC microgrid: Case study on an islanded residential application in Greece'
  A. O. Rousis, D. Tzelepis, G. Strbac
  International Journal of Electrical Power & Energy Systems, (Under Review)

CONFERENCE PAPERS - LEADING AUTHOR:

- 'Distributed Current Sensing Technology for protection and Fault Location Applications in HVDC networks'
  D. Tzelepis, A. Dyśko, C. Booth, G. Fusiek, P. Niewczas, T. C. Peng
  IET - Developments in Power System Protection (DPSP), March 2018
  Accepted, DOI pending

- 'Design of DC-line terminating inductors for enhancement of protective functions in MTDC grids'
  D. Tzelepis, A. Dyśko, C. Booth, S. Mirsaeidi, X. Dong
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  Accepted, DOI pending

- 'Enhanced DC Voltage Control Strategy for Fault Management of a VSC-HVDC Connected Offshore Wind-farm'
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  D. Tzelepis, S. Ademi, D. Vozikis, A. Dyśko, S. Subramanian, H. Ha
  IET - Power Electronics Machines and Drives (PEMD), April 2016
  DOI: 10.1049/CP.2016.0263

- 'Performance of Loss-Of-Mains Detection in Multi-Generator Power Islands'
  D. Tzelepis, A. Dyśko, C. Booth
  IET - Developments in Power System Protection (DPSP), March 2016
  DOI: 10.1049/CP.2016.0066

- 'Impact of Distributed Generation Mix on the Effectiveness of Islanded Operation Detection'
  D. Tzelepis, A. Dyśko
  PACWolrd Conference, Jun. 2015.

CONFERENCE PAPERS - CO-AUTHOR:

- 'A Novel Approach for Protection of Radial and Meshed Microgrids'
  S. Mirsaeidi, X. Dong, D. Tzelepis, C. Booth
  IET - Developments in Power System Protection (DPSP), March 2018
  Accepted, DOI pending

- 'Practical risk assessment of the relaxation of LOM protection settings in NIE Networks' distribution system'
  A. Dyśko, D. Tzelepis, C. Booth, J. Pollock, D. Hill
  IET - Developments in Power System Protection (DPSP), March 2018
  Accepted, DOI pending

- 'Power Management, Control and Protection of DC Microgrids'
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- 'Assessment of Fault Location Techniques in Voltage Source Converter based HVDC systems'
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- 'Fault current characterisation in VSC-based HVDC systems'
  S. Ademi, D. Tzelepis, A. Dyśko, S. Subramanian, H. Ha
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Chapter 2

Layout, Control and Modelling of HVDC Grids

2.1 Basics of HVDC

HVDC power transmission is becoming increasingly competitive compared to HVAC, due to numerous commercial and technical advantages such as those listed below [5,6,8,41–43]:

- Efficient bulk power transfer over long distances (notably from offshore wind).
- Interconnection of asynchronous grids.
- Black start capability.
- Reduced cable and tower profile.
- AC system frequency support.
- No technical limit to the length of a submarine cable connection.
- Increase of power infeed without increasing the short circuit level.
- AC decoupling (immunity from impedance, phase angle, frequency or voltage variations).
- Independent management of frequency and generator control.
- AC system stability improvement.
- Independent and fast control and provision of active and reactive power.

HVDC technology can be formed by two distinctive technologies, namely LCCs and VSCs [8]. The LCC-based technology has been a key player in bulk power transmission

around the world over the last sixty years [9]. However, it is accompanied with some well-known issues, which to a certain extent limit further applications of this technology. One of the limitations is the significant amount of reactive power required at both ends of the HVDC link. Such requirement originates from the thyristor firing after commutation voltage becomes positive. This results to a delay in the current rise (with respect to voltage) and hence both rectifier and inverter consumes reactive power [10]. An additional major drawback of LCC-based technology (especially in the context of supergrids) is the difficulty to be connected to weak grids such as wind farms. In such grids the effective short circuit ratio and the inertia constant are both significantly lower [44] and therefore LCC-based technology cannot be utilised easily. Moreover, large harmonic filters are required, which in the case of offshore wind farms, calls for bigger platforms located at rectifier stations [45, 46]. One of the most important challenges in the employment of LCC-based technology is the commutation failure under fault conditions [11], which leads to the interruption of transmitted power [47] and impose further electrical stresses on the converter equipment [48].

The aforementioned limitations have been overcome by the introduction of VCSs, which are capable of providing independent control of active and reactive power, immunity to commutation failures, faster dynamic response and connectivity to weak grids [8]. Over the last decade, due to all the aforementioned dynamic features and operational flexibilities [12], such technology has become the universally-accepted solution for HVDC transmission. This has been achieved by the utilisation of two-level and neutral-point clamped converter topologies [13]. Further improvements with regards to fault blocking capability, lower semiconductor losses, scalability, improved AC-side waveforms quality and elimination of DC-link capacitor, has led to the increased adoption of MMCs in many of the recent HVDC transmission system projects [14–16].

It should be highlighted that the main reason VSC-based technology is superior than the LCC-based (especially in the context of supergrids) relies on the power reversal mechanism. In VSC-based systems, power flow can be reversed without altering the DC voltage polarity. On the other hand, LCC requires voltage reversal in order to change the power flow direction. This is not a challenge for point-to-point links, but LCC does not support a meshed grid operation without physical isolation. Consequently, VSC-based technology is the natural choice for the implementation of meshed DC grids.

A simple representation of an VSC-HVDC system is shown in Figure 2.1. Active

and reactive power is fed to or from a converter, operating as a rectifier or inverter respectively. DC power is transferred through a transmission media (cable or overhead line), and is independent of the AC frequency, phase and voltage level. Power converters are connected with AC grid using power transformers. This arrangement provides a galvanic isolation which is essential especially in the cause of faults both on the AC and DC side of the system. AC-side filters are also utilised in order to eliminate all the unnecessary harmonics, present both on voltage and current components. The formation of harmonics is mainly determined by the switching frequency of semiconductor devices, the selected control approach and the converter architecture. A reactor is usually utilised on the AC side to act as a low-pass filter for the line currents. Due to its inductive nature, it limits the rate of change of current and prevent abrupt changes in voltage polarity, caused mainly by the switching of the valve devices and faults either on AC or DC side.

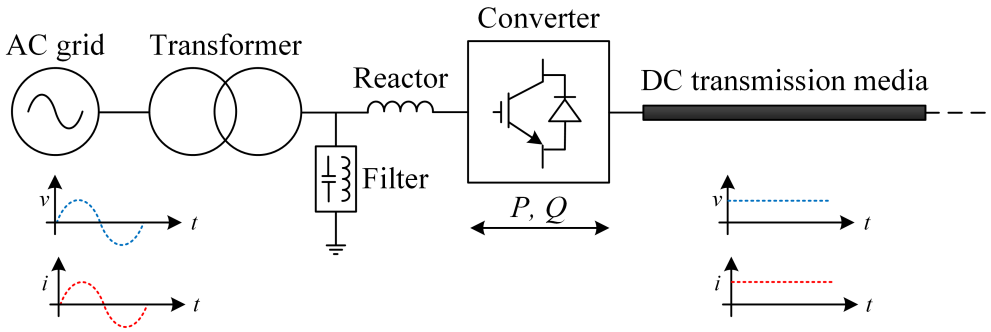


Figure 2.1: Typical structure of an VSC-HVDC system.

2.2 Network Architectures

An HVDC transmission system can be formed by adopting numerous operating design architectures. The most commonly accepted are presented in this section indicating their characteristics, advantages and disadvantages. The reviewed HVDC network architectures are summarised in Table 2.1 and depicted accordingly in Figures 2.2 to 2.6.

Table 2.1: HVDC Network Topologies.

Monopole	**Bipole**
Symmetric	Metallic return
Asymmetric - Metallic return	Ground return
Asymmetric - Ground return	–

Monopole configurations, as the name indicates, employ only one set of conductors.

Such systems are the simplest and least expensive for moderate power transfers, since only one high voltage insulated cable (or line conductor) and two converters (one per each terminal) are required.

Bipole configurations introduce at least two converter stations located at each DC terminal which gives an advantage of a doubled power rating, compared to monopole configuration. Moreover, the advantages of a bipole solution over a solution with two monopoles are reduced cost, due to one common or no return path, and lower losses. The main disadvantage is that unavailability of the return path with adjacent components will affect both poles.

According to the return path option, both monopole and bipole configurations can be further classified. For return path, such systems can be equipped with ground electrodes (both sea or land electrodes) or with dedicated insulated conductors of medium-voltage, normally know as 'metallic return' [49]. The main difference is that for the ground return configuration, each station is individually grounded whereas the metallic return needs only one grounding point. What is also worth mentioning is that the metallic return path is utilised under situations where the earth resistivity is too high, or when other underground metallic installations can interfere with the system [18]. Additionally, the metallic return path has a very low insulation requirement.

2.2.1 Symmetric monopole

Symmetric monopole configuration (refer to Figure 2.2) assumes the DC voltage on each pole to be half of the nominal. In such a configuration, DC-side grounding can be totally absent, or alternatively located at the mid point of the DC-link capacitors [43]. Such a configuration has a unique characteristic that eliminates the AC feed during pole to ground faults and at the same time the AC-side transformer is not exposed to DC stresses [50]. However, due to the insulation requirement of both conductors, it has a higher cost than other monopole configurations.

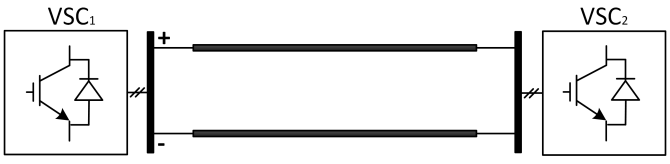


Figure 2.2: Symmetric monopole.

2.2.2 Asymmetric monopole with metallic return

Asymmetric monopole with metallic return operates with full nominal DC voltage on one of the poles. Due to the utilisation of a metallic conductor as a return path (refer to Figure 2.3), such a configuration does not introduce any ground currents. Since the full voltage is present on one of the poles, the metallic conductor has low requirements for high voltage insulation. Additionally, such network architecture can be expanded to a bipole network [18]. However, such a system requires that the AC transformers be designed for DC stresses and there is a limited redundancy compared to a bipole configuration [2].

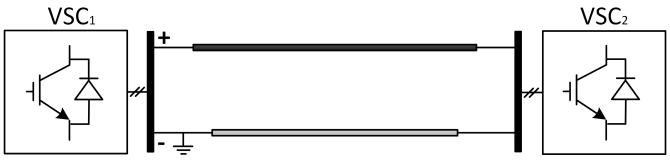


Figure 2.3: Asymmetric monopole - metallic return.

2.2.3 Asymmetric monopole with ground return

Asymmetric monopole with ground return configuration employs ground electrodes, located at both converter stations, as the return path. In such a case the positive pole voltage is equal to the full nominal DC voltage. This topology offers the great advantage of significantly reduced cost due to requirement of a single DC conductor. Additionally, by a quick observation of its equivalent circuit, depicted in Figure 2.4, it can be seen that there is an option for expansion to a bipole network. However, during DC pole to ground faults there is an in-feed from the AC side which in turn imposes the need for the DC stress resilience of the AC side transformer [1]. Moreover, permission is required both for continuous operation with DC ground current and the installation of electrodes.

Figure 2.4: Asymmetric monopole - ground return.

2.2.4 Bipole with metallic return

Bipole with metallic return systems utilise a single metallic return path to be shared by both poles as shown in Figure 2.5. Since the two poles operate with an equal voltage, the current will flow to the return path only in the case of voltage imbalance between the two poles. If a fully insulated cable were to be installed as the metallic return, it could be used as a spare cable during a faulted condition and thus provide a more flexible solution [50]. Moreover, in such network architecture there is a 50 % redundancy of the total rating. On the other hand (and compared with monopole configuration) the cost for the same voltage and power rating is higher. Additionally, there is a requirement for low-voltage insulated neutral conductor and the AC transformers should be designed to withstand DC stress [2].

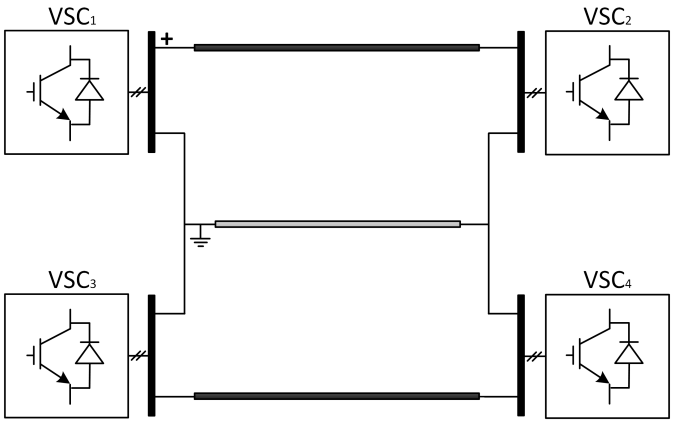


Figure 2.5: Bipole - metallic return.

2.2.5 Bipole with ground return

Bipole with ground return configuration introduces the placement of ground electrodes at each side as shown in Figure 2.6. Compared to bipole with metallic return, this topology is costly effective as it does not require an extra conductor. However, compared with monopole configuration the cost for the same voltage and power rating is higher. Moreover, during DC pole-to-ground faults, there is an infeed of fault current from the AC side and hence the AC transformers should be designed to withstand DC stress. Additionally, permission is required both for temporary operation with DC ground current and the installation of electrodes (including environmental effects) [2].

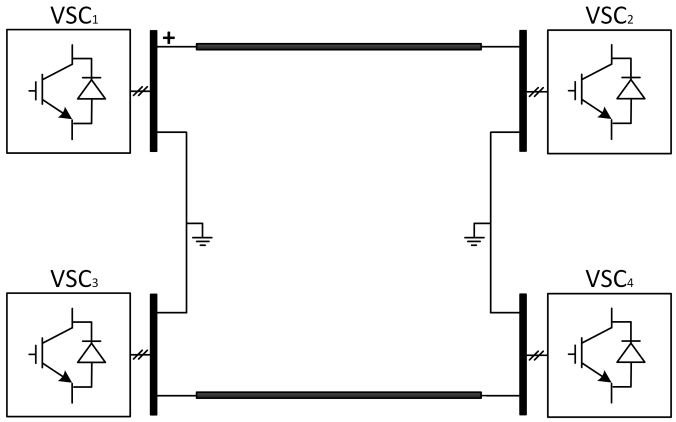


Figure 2.6: Bipole - ground return.

2.2.6 Multi-terminal

Multi-terminal systems can be designed based on all the configuration mentioned above with their advantages and disadvantages. For the sake of a robust DC voltage and power control, especially for large wind farm integration [51], multi-terminal HVDC networks are constructed using the symmetric monopole. An example of a MTDC network based on symmetric monopole architecure is depicted in Figure 2.7.

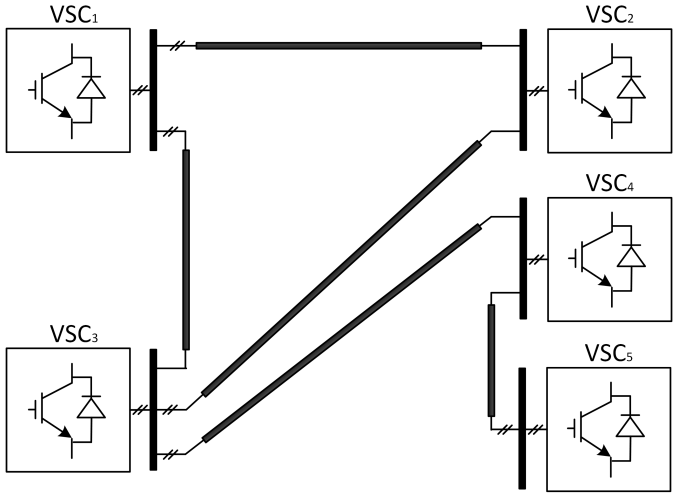


Figure 2.7: Multi-terminal.

As it can be observed, only the symmetric monopole operates with negative and positive DC voltage. In the case of asymmetric monopole, only one pole operates at full DC voltage. Nevertheless, a negative polarity is preferred (mainly for overhead lines) due to reduced corona losses and radio interference [18].

2.3 Converter Designs

2.3.1 Two-level converters

The two-level converter is by far the most common VSC for a wide variety of applications such as industrial drives, automotive drive systems and integration of renewable energy sources. Figure 2.8 illustrates the basic structure of a two-level VSC. Such converter is equipped with a short-term energy storage (i.e. DC capacitor) whose main purpose is to cater for a low-impedance route during the converter turn-off phase (fraction of a fundamental cycle) and hence maintain a constant DC-side voltage (V_{dc}). An inductance is also connected in series with the AC terminals which should maintain the AC-side currents sufficiently constant in the short time-frame between switching.

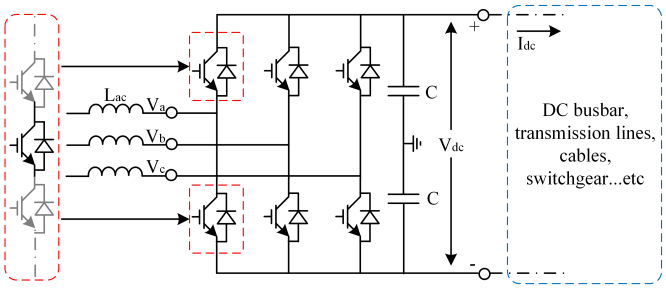


Figure 2.8: Two-level VSC.

A two-level VSC synthesises an AC voltage at its terminals from the DC voltage supplied to it and vice versa. This is typically implemented using a fast switching technique (e.g. PWM, SPWM) between the voltages at the upper and lower DC supply [3] as illustrated in Figure 2.10(a). High order switching harmonics are removed by appropriately sized AC-side filters.

2.3.2 Neutral point clamped converters

Further improvement of two-level converter has been achieved with a three-level topology, using the Neutral Point Clamped (NPC) converter as illustrated in Figure 2.9. The use of optimal PWM (detailed switching selection to reduce harmonics [52] and third harmonic injection [53] to boost DC voltage utilisation) allow a further reduction in switching frequency, harmonic generation and losses.

Due to the voltage withstand of each IGBT, both in two-level and three level designs, each switch in reality consists of hundreds of series-connected IGBTs. Consequently this creates some additional challenges related to control of the simultaneous switching of the

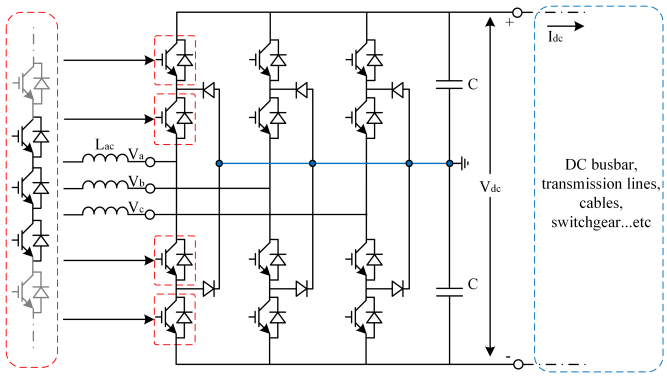


Figure 2.9: Three-level Neutral Point Clamped VSC.

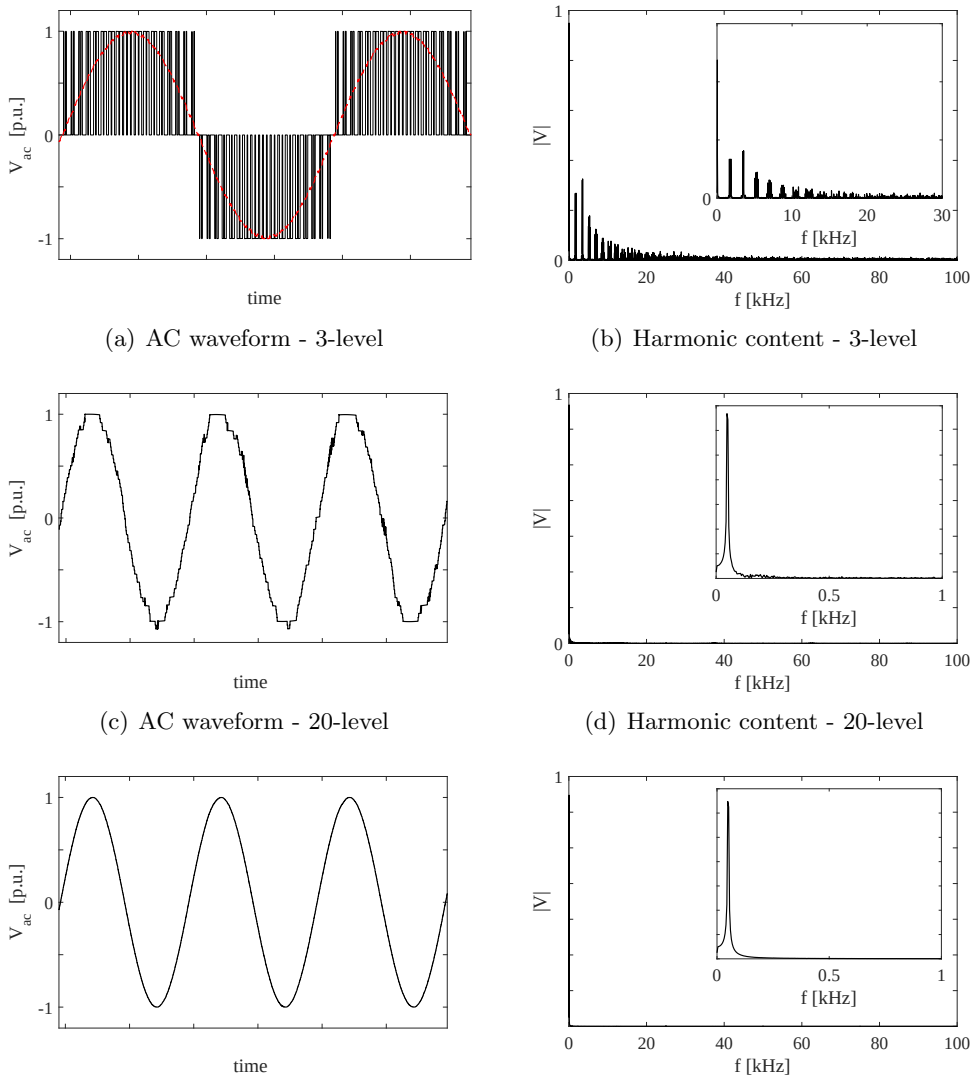
IGBTs. Another major drawback of such converter design is the generation of harmonics (see Figure 2.10(b)), which in turn increase losses, size of filtering equipment and hence the footprint (very important in offshore platforms) [54].

2.3.3 Modular multi-level converters

In an attempt to overcome the aforementioned challenges, manufactures have proposed a new converter design concept known as MMC, as illustrated in Figure 2.11. Both the working principle and the design of the MMC are completely different from two-level and three-level converters. From the design point of view, it is observed that the DC-link capacitance is completely absent. In fact, the total capacitance is now divided and installed on each sub-module (SM) which each arm is built upon. Each sub-module can be constructed by adopting half bridge [55], full bridge [56] or mixed cell topology [57]. In order to balance any transient voltages and limit possible fault currents, arm inductors (L_{arm}) are also inserted [58, 59].

In MMC-based VSCs, AC and DC voltage is formed by connecting and disconnecting the capacitors in the series-connected SMs of each arm. The resulting voltage is now formed in discrete levels as shown in Figures 2.10(c) and 2.10(e) (example AC waveforms for 20-level and 400-level respectively), and it is evident that the resulting voltage is smoother. As a result, the harmonic content in now significantly reduced (Figures 2.10(d) and 2.10(f)), which means that AC-side filters can now be significantly reduced in size or completely eliminated.

Due to its design and operating principle, MMC is characterised by some very advantageous features such as lower switching frequency [60, 61], DC fault blocking capability [15,62], reduced semiconductor losses [63,64], enhanced reliability [65], reactive



(a) AC waveform - 3-level

(b) Harmonic content - 3-level

(c) AC waveform - 20-level

(d) Harmonic content - 20-level

(e) AC waveform - 400-level

(f) Harmonic content - 400-level

Figure 2.10: AC waveform and harmonic content for different converter topologies.

power support [66], improved AC and DC power quality [67] and scalability [68].

Even though the MMC offers a wide variety of advantages and operation features, it comes accompanied with some challenges related to the control. Specifically, there is a voltage balance issue of series-connected capacitors [69], which is very important as AC and DC voltage is formed by the sum of these capacitor voltages [70]. Moreover, during the operation there will always be some degree of voltage imbalance between the arms of the converter. This will lead to the formation of circulating currents among the three phase units, which will distort the sinusoidal arm current, and introduce further losses.

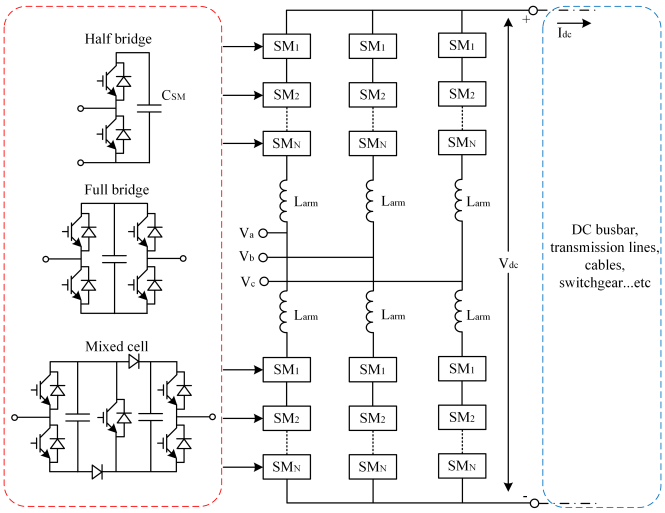


Figure 2.11: Modular multi-level VSC.

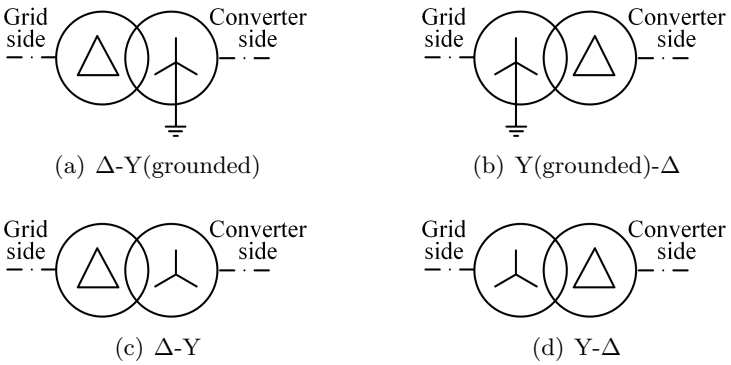
2.4 Grounding Options

The aspect of system grounding is essential to power systems, as it affects the behaviour of the system to transients, determines the load types which the system can accommodate and influences the system protection requirements and grading. The grounding configuration refers to the way that any neutral point of a power component is connected to the ground, which can be referred to any of the following devices:

- Generators
- Transformers
- Power Converters
- STATCOMs/Filters
- Loads

Within the scope of VSC-HVDC fault analysis (especially for pole-to-ground faults), grounding configuration plays a significant role. This is because different conducting paths and current loops are formed within the system components during such faults. The possible grounding configurations can be numerous depending on the point of grounding, both at AC transformers (Figure 2.12), and DC-link capacitors (Figure 2.13).

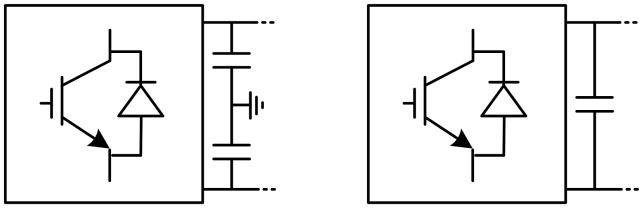
System grounding forms a medium in order to keep the voltage-to-ground of each pole to predictable and safe limits. In addition, it allows the isolation of faulted components within the system during fault conditions. Determining the system grounding is strongly



(a) Δ-Y(grounded) (b) Y(grounded)-Δ

(c) Δ-Y (d) Y-Δ

Figure 2.12: AC transformer grounding configurations.



(a) Capacitor midpoint grounded (b) Ungrounded

Figure 2.13: DC-link capacitor configurations.

related to the selection of system layout. Choosing the grounding scheme includes a trade-off between cost of insulation, protection design and desired measuring points and techniques.

The different options to connect the neutral connection point with the ground are shown in Figure 2.14 [6]. The neutral point of the system can be left intentionally ungrounded (no grounding) or solidly grounded. Additionally, by utilising and combining R, L, C components, there is a option for an impedance grounding.

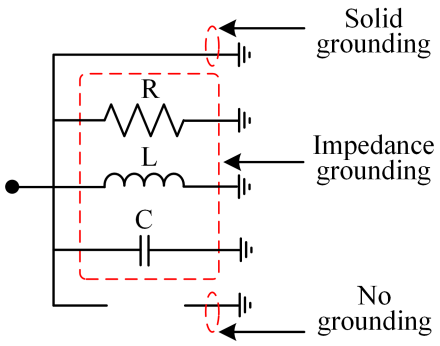


Figure 2.14: Grounding options.

Ungrounded systems refer to the system operation with no intentional ground connection. In fact, such systems are connected to the ground through the capacitance

of live conductors and the ground [71]. As there is no voltage reference, in most cases such configuration forms an extremely high impedance. In fault conditions involving ground, the resulting currents can be low, which is advantageous, as the system can keep operating with ground fault present. Moreover, ungrounded systems are costly more beneficial, as the capital investment for grounding equipment is eliminated. On the other hand, an ungrounded system can produce high transient pole-to-ground over-voltages, which can lead to breakdown of any involved insulation medium, or any other equipment. In particular, in the case of a pole-to-ground fault, the faulted pole voltage would drop to zero, while the voltage on the healthy pole would jump to a high value (nominal or double nominal for assymetric monopole and bipole schemes respectively) [72].

Impedance grounded systems establish a connection with the ground via a resistance, inductance, capacitance or any combination of them. This type of grounding can be classified into high impedance and low impedance. Even though in practice there is a clear difference between them, there are no standards for the level of current that could potentially define them [73]. However, two general shortcomings can be deduced [74]:

- High Impedance ⇒ Limits the fault current. In particular a high value of impendence can make the system as if ungrounded.
- Low Impedance ⇒ Such configuration can be characterised as solid. During faulty conditions, such option will double the pole-to-ground voltage on the non-faulty (healthy) pole.

In resistive grounding, the neutral is connected to the ground through one or more resistors. In case of pole-to-ground fault, a resistive grounding can be used to reduce the steady-state fault current. A low resistive grounding configuration can limit the voltage while premiting a greater level of fault current. On the other hand a high resistive grounding can limit the fault current, but the system voltage can be higher. When a reactor is used to establish a grounding connection the rate of change of fault current can be significantly reduced. However, during fault transients, an inductive component will introduce a voltage between the ground and the neutral point. This imposes a voltage rise in the healthy pole and introduces further electrical stresses. When a capacitive grounding configuration is used, any voltage excursion is eliminated during pole-to-ground faults. However, a capacitor would absorb a huge current after the fault, which could cause problems to the performance of a protection scheme.

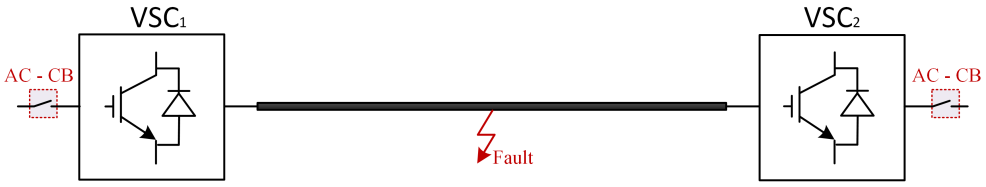
Solidly grounded systems refer to the direct connection of a neutral point to ground. Such configuration does not provide any restriction to the fault current levels. However such behaviour can be advantageous, as it causes a faster fault detection. The largest element of impedance in this configuration is formed by the soil surrounding the grounding and the conductor itself. Consequently, during pole-to-ground faults, the steady state fault current is only limited by the aforementioned elements.

Another concern regarding the system grounding configuration, refers to the DC current distribution [75]. Great ground potential differences will be present due to the flow of great DC currents. Such currents will flow through the transformer (taking into consideration that their neutral is grounded) which in turn will introduce a DC bias stress. Consequently such stress may cause noise, vibrations, rise of temperature and even make protection systems mal-operate. Additionally, according to [76] the selection of the grounding element can affect the distribution of DC currents in the neighbouring AC system components. In particular, the error on AC measurements can be increased, but also the current flowing to other substations' transformers may experience a great rise.

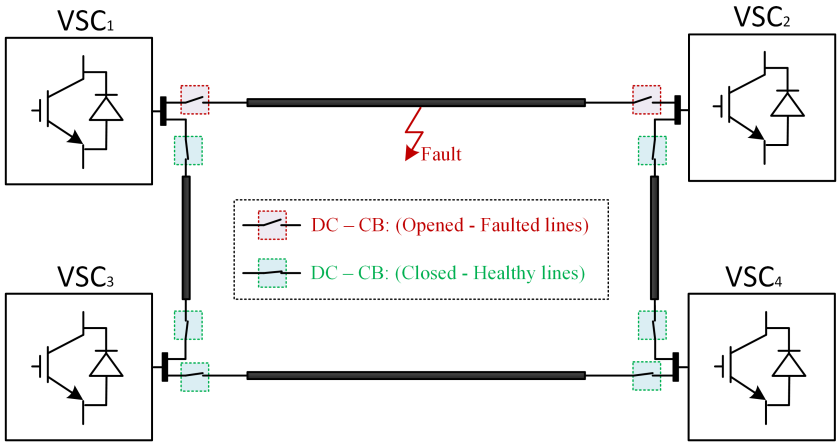
2.5 HVDC Circuit Breakers

The majority of the presently operational and planned HVDC links are point-to-point with two points of connection. Traditionally, in these networks DC-side faults are disconnected through AC-side breakers (see Figure 2.15(a)) or by fault blocking converters [60,62,77,78]. However, within the context of MTDC grids these two options are not practical, as the whole grid would be de-energised. Consequently, the feasibility of operating secure MTDC networks relies largely on the ability to quickly interrupt DC-side fault currents, so that the operation of the healthy parts of the network is not compromised when one element of the network is faulted (see Figure 2.15(b)).

DC-side fault currents in VSC-based networks are characterised by large magnitudes with small rising time [79]. The absence of a natural current zero crossing (as is the case with AC systems) requires a dedicated mechanism to drive the current to zero while dissipating the energy stored in the short circuit (mainly trapped within the system inductances [80]) before the switching element can successfully interrupt the flow of current. Up to now there is not a globally accepted solution for HVDC current interruption devices. This is due to the fact that designing and selecting a breaking



(a) Point-to-point network: Disconnection from AC side



(b) MTDC network: Disconnection from DC side

Figure 2.15: Fault current interruption strategies.

device is a matter of operational losses, operating time, energy absorption withstand, size, cost and expected maximum fault current level. Breaking time and energy dissipation are two controversial aspects, since the smaller the breaking time the greater the energy required to dissipate.

There are many HVDC circuit breaker (CB) concepts proposed in the literature; however, all have a similar structure, consisting of a commutation branch to drive the current to zero, a switching component for voltage withstand, and an absorption path for dissipating energy. Usually the voltage-withstand switch component, consists of multiple switches in series connection, since a single component cannot withstand hundreds of kilovolts. It is a common practice that the voltage withstand component to remain turned-off during healthy operation, in order to reduce operational losses. Regarding the component for energy dissipation a surge arrester (SAr) is used. This can be a Metal Oxide Varistor (MOV) or Zin Oxide (ZnO). According to the latest literature the following devices can be applied to interrupt or limit the fault current in VSC HVDC transmission systems:

- Hybrid Circuit Breakers (HbCBs).
- Solid State Circuit Breakers (SSCBs).

- Active and Passive Resonance Circuit Breakers (A-RCBs, P-RCBs).
- Super-Conducting Fault Current Limiters (SCFCLs).

2.5.1 Hybrid circuit breaker

A schematic of a HbCB can be seen in Figure 2.16, consisting of three distinctive paths, namely load path, commutation path and absorption path. During healthy operation the current flows through the fast mechanical disconnector (FMS) and the load commutation switch (LCS). When a tripping signal is initiated, LCS opens driving the current through the commutation branch. This allows the FMS to open, as no current is flowing through its contacts. In the next stage the commutation branch turns off, resulting in over-voltage which causes the SAr to operate. From this point the current flows through the SAr, where energy is dissipated and the current gradually falls to zero. Usually there is an inductor in a series connection with the breraker, in order to increase the rise time of a fault current [81].

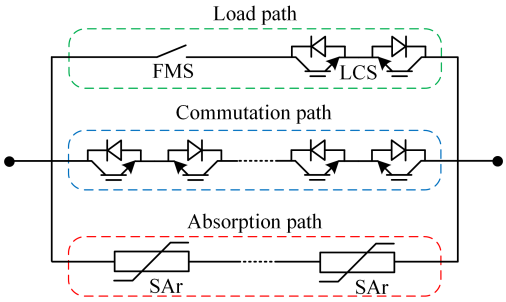


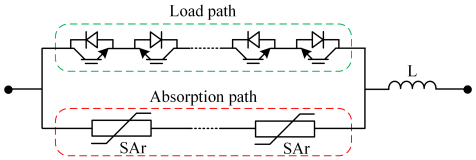
Figure 2.16: Hybrid HVDC breaker.

Since there is no current flowing through the commutation branch during healthy operation, the power losses are fairly low. Regarding the voltage requirements of LCS is typically in the kilovolt range hence the number of IGBTs is significantly reduced [55]. Due to voltage withstand requirements of the commutation branch, there is a large number of series-connected IGBTs required which raises the entire device cost.

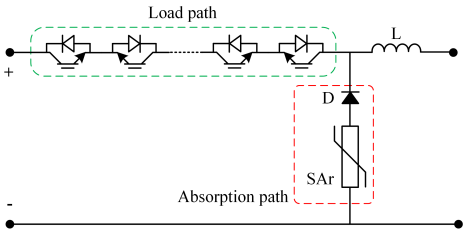
The HbCB concept was firstly introduced by ABB [82] and according to the manufacturer a breaking time of 2 ms (opening time of FMS) is achievable while the maximum rating of the breaking current is 9 kA. There are a few alternatives of HbCB in the literature [83] depending on the addition of extra components (e.g. switches, capacitors and inductor) and circuit design.

2.5.2 Solid state circuit breaker

SSCBs are build upon the fact that mechanical contacts are completely absent in the CB circuit [84]. This feature makes SSCBs significantly faster than the aforementioned HbCBs. A simple representation of a SSCBs can be seen in Figure 2.17(a). During healthy operation the current flows through the load path, which consists of series-connected semiconductor devices (e.g. IGBTs). When a fault is present and relays have sent tripping signals to the breaker, the semiconductors devices will turn-off. This will force the current to flow through the SAr, the voltage across the breaker will be suppressed to the clamping voltage of the SAr. Then, reverse voltage is applied to inductance L, and the fault current decreases. An alternative of SSCB can be seen in Figure 2.17(b).



(a) Design 1



(b) Design 2

Figure 2.17: Solid state HVDC breakers.

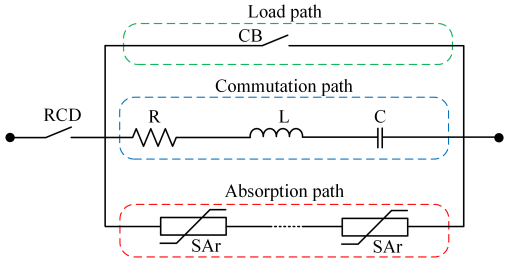
At this arrangement, the abortion path consists of a SAr in series connection with a diode, which is installed vertically between positive and negative pole. During normal operation current flows through the load path. After the successful detection of a fault, the entire load path will turn-off. At this case the fault current will commutate through commutation path which will immediately fade to zero and the inductance L will be de-energised again by SAr. This circuit arrangement can reduce the energy required to be absorbed by the breaker [85] by suppressing the surge voltage on the load path.

In all SSCB arrangements there is always a path (with multiple semiconductor devices) which is turned-on during normal operation. This introduces increased operational losses and hence such arrangements are not always favourable (even though they can achieve very small interruption times) [86].

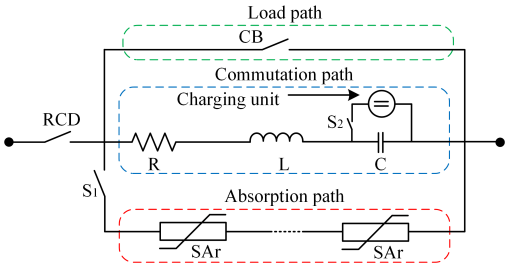
2.5.3 Resonance circuit breaker

Resonance circuit breakers can be divided into passive and active, as illustrated in Figures 2.18(a) and 2.18(b) respectively [38]. The main concept of the RCBs is to oscillate the current in order to create a zero crossing point for arc extinction.

For example, in P-RCB (Figure 2.18(a)) during normal operation the current flows through load bath. Once a tripping signal is sent to the breaker, the CB will start opening and current will commutate through the commutation path, consisting of a resonance R, L, C circuit. After a few ms, current will start oscillating, until a zero crossing point is present which will drastically lead to arc extinction. At this point, the total current is still high due to the stored energy in the entire circuit inductance. After the arc extinction, capacitor C is charged and there is an over-voltage formed across the CB. This will force the SAr to operate and hence the current will flow through the abortion path, where it will gradually fade close to zero. The interruption process is finalised by opening the residual current disconnector (RCD). The total operation time of the P-RCB is considered relatively slow as it takes around 50 ms for full current interruption.



(a) Passive



(b) Active

Figure 2.18: Resonance HVDC breakers.

In A-RCB (Figure 2.18(b)) the principle is the same as in P-RCB. The difference lies across the commutation path and the current oscillation mechanism. After opening the main contact in load path, pre-charged capacitor C will inject a negative current into the

load path (by closing S_1). This will significantly reduce the time to reach the initial zero crossing in current (compared to P-RCB). The rest of the interruption process remains the same. This CB is significantly faster than P-RCB; it takes approximately 20 ms for the full interruption process. However, it requires an additional DC charging unit for the capacitor.

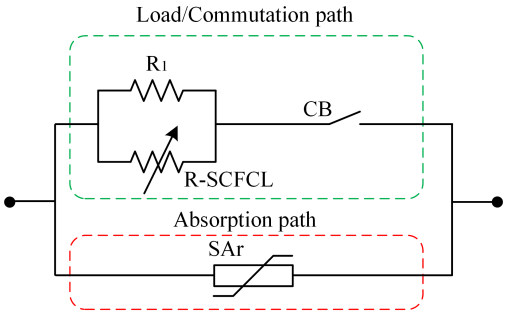
The reason that RCBs (both active and passive) are relatively slow is due to the fact that the CBs are quite slow to operate (usually in P-RCB the CBs are AC-air blast or SF6 puffer [87], while for the A-RCB vacuum CBs are used [88]) and consequently there is a latency for the arc extinction.

2.5.4 Super conducting fault current limiters

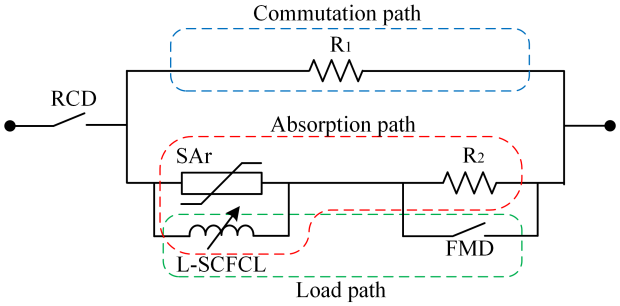
The main concept of SCFCL-based CBs is to provide a high impedance path to the fault, which will reduce the instantaneous fault current level and minimise the requirements for the breaker circuit (components' rated power/voltage and size) [89, 90]. Since SCFCLs are actually limiters, they do not offer a full breaking solution; hence, they are always accompanied with CBs and other extra components [91]. Some typical SCFCL-based CB design concepts proposed in the literature are shown in Figure 2.19 [92, 93].

In the design depicted in Figure 2.19(a), during normal operation the current flows through the load path and the resistance value of R-SCFLC is low. After a fault is present, the value of the resistance value of R-SCFLC will increase, providing a high impedance path to the fault. This will limit the fault current to low level and then the CB can interrupt a low DC current easily. Due to current limitation, the CB has low requirements in terms of current breaking capability, voltage withstand and arc extinction time. Due to the opening of the CB and the formation of an arc, the SAr in the absorption path will be enabled, forcing the total current to reach near-zero values.

An alternative desing of SCFCL is depicted in Figure 2.19(b). This CB circuit is mainly composed of a current-limiting resistance R_1, an FMD, a protective resistance R_2, a SAr, and a current-limiting SCFCL-based inductor L. During normal operation, FMD is closed and current flows through the inductance L-SCFCL (which is maintained in the zero-resistance/superconducting mode). When a fault is present, due to the current limitation of L-SCFCL, current will mainly flow through R_1. Since low current flows through FMD, it can now open (R_2 will be inserted in the fault path). The fault interruption will be completed by opening the RCD (current has now reached low values



(a) Design 1



(b) Design 2

Figure 2.19: SCFCL-based HVDC breakers.

and interrupting low DC current is not so crucial). Any over-voltages and residual currents within the breaker will be cleared by the SAr.

Even though SCFCL-based CBs can effectively limit the fault currents and hence reduce the requirements of CBs, they require high energy during healthy operation. This indicates high cost both for maintaining low temperatures but also for equipment.

Even though all the schemes have their own advantages and disadvantages, the HbCB breaker has been found to posses the best total efficiency regarding the cost, losses and applicability [84, 94]. Such a circuit breaker has been considered as the possible candidate for interrupting DC-side faults in future MTDC grids for this reason. In fact, the HbCB concept has been utilised in many power system studies for MTDC networks, including protection [36], fault analysis [50], modelling [14] and stability [95].

2.6 Voltage and Current Measuring Techniques

In order to capture DC-side fault transients for protection, control and fault location applications, measuring equipment is required to be placed on HVDC installations [40]. Since DC-side fault signatures are characterised by a high-frequency content, high analogue bandwidth and sampling frequency are required. High-voltage measurement

equipment typically consists of a converting device, transmission device, and recording device [20].

2.6.1 Resistive-capacitive voltage transformer

In VSC-based HVDC systems, measurement of voltage is usually obtained using resistive-capacitive voltage transformer [20], as shown in Figure 2.20. Pure capacitive or inductive voltage divider are not well-suited for the measurement of fast transients on account of their limited transfer behaviour leading to narrow frequency bands [96, 97].

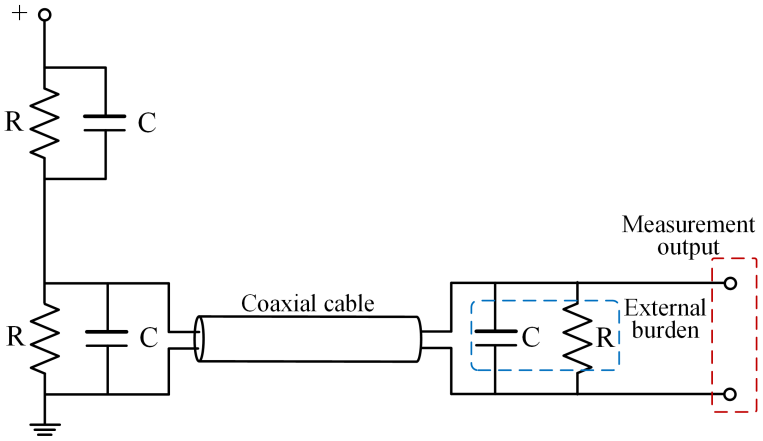


Figure 2.20: Resistive-capacitive voltage transformer.

The resistors connected in parallel to the capacitors are designed to guarantee an extremely low resistance variation through time, electrical stress and temperature [97]. Single- or double-shielded coaxial cables are used to transmit pulses from one end to another, preserving the information in the signal. To prevent any possible reflection phenomena (occuring mainly during fast transients), the coaxial cable is usually terminated with an external burden impedance. Resistive-capacitive voltage transformers output an accurate voltage representation over a wide frequency band (typically from DC up to 500 kHz) [97, 98].

2.6.2 Zero-flux transformer

For the measurement of DC current in HVDC applications, closed loop transducers, also called Hall Effect compensated, or zero flux transformers are commonly used [20, 98]. A typical structure of the transformer can be seen in Figure 2.21 [99] which consists of two windings (W_1 primary and W_2 secondary), a magnetic core, a Hall sensor and an operational amplifier (OP).

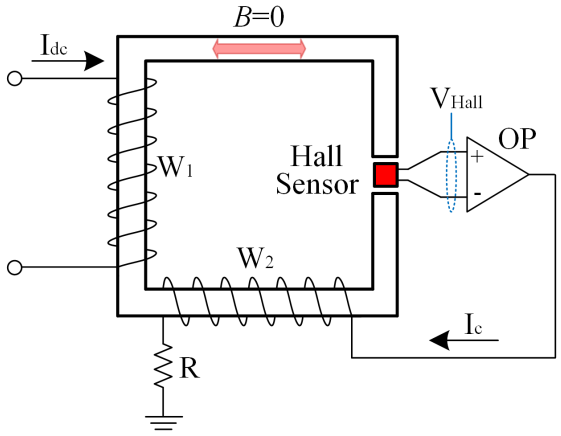


Figure 2.21: Zero-flux DC current transformer.

When primary current I_{dc} flows through winding W_1 it generates a magnetic field B in the core which induces a voltage V_{Hall} at the sensor output. The sensor output voltage V_{Hall} is almost proportional to the magnetic field, which, in turn, is proportional to the current to be measured. The primary current I_{dc} is compensated with current I_c fed to W_2 which results in zero flux ($B = 0$) in the magnetic core. If now the primary current contains a DC component, the current proportional to this is fed to the positive input of the OP. The resulting compensation current I_c is a true-to-scale, galvanically-separated copy of the primary current [100]. Depending on the type of construction of the DC transformers, bandwidths of up to 500 kHz at currents of maximum 5 kA and up to 10 kHz at currents of maximum 25 kA can be attained [96].

2.6.3 Fibre optic current sensors

Current sensors based on optical sensing commonly rely on the Faraday effect. The Faraday effect describes that when light passes through a transparent medium under the effect of a magnetic field, its travelling speed changes slightly. Consequently, light waves accumulate an optical phase difference in proportion to the field's strength.

A typical scheme based on Faraday effect is depicted in Figure 2.22. A laser with a polariser generates a linearly polarised light wave. The magnetic field H, is the result of current I_{dc} flowing in parallel with the fibre sensor. As per the Faraday effect, field H causes a rotation of the polarisation plane by an angle β. The combination of the analyser and the photo-detector convert and modulate the polarised light into an electrical signal, which in turns corresponds to the current to be measured.

In Figure 2.23 [101] a reflective fibre optic current sensor scheme is depicted which is

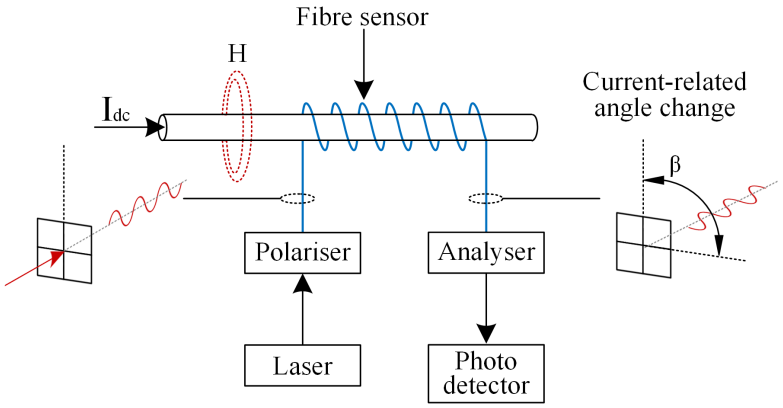


Figure 2.22: Optical fibre current sensor as per the Faraday effect.

an enhanced version of the Sagnac interferometer [102].

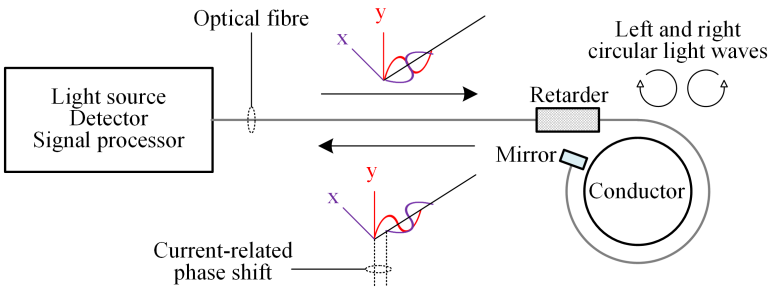


Figure 2.23: Fibre-optic current sensor.

The presented scheme consists of an electronic device (light source, detector and signal processor), a retarder and a mirror. A simple loop of optical fibre is wounded around the conductor which carries the current to be measured.

The light source generates a light wave which is decomposed in right and left circularly polarised light waves which travel along the coil of the sensing fibre. The waves are then reflected by the mirror and their polarisation direction is swapped. When a DC current is flowing though the conductor, a current-related phase shift is present to the reflected wave. This difference (detected and analysed by the detector and signal processor) is therefore a direct and highly precise measurement of the current.

The aforementioned fibre-optic current sensor is commercially available by ABB [103], and can measure uni- or bidirectional DC currents of up to 500 kA with an accuracy of $\pm 0.1\%$ of the measured value.

2.7 Control Structures

It is recognised that MMC-VSCs have some hierarchical-base structure as shown in Figure 2.24. Such structure can provide flexibility on simulation models approaches [104], type of study [54] and therefore on actual MMC-based applications.

As shown in Figure 2.24 the entire control structure of a VSC can be divided in the following three layers:

- Dispatch/Station control
- Upper-level control
- Lower-level control

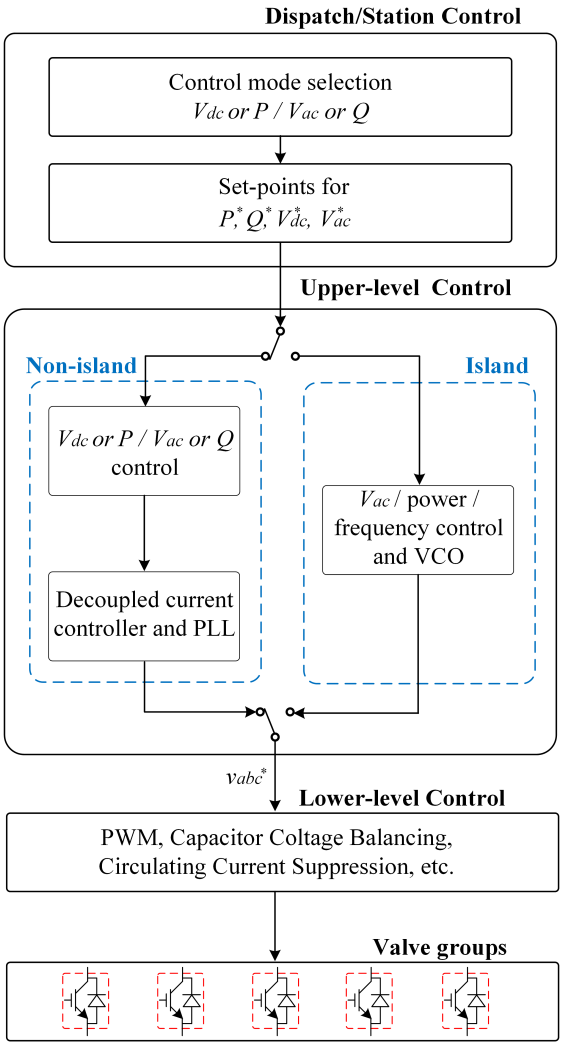


Figure 2.24: VSC control modes hierarchy.

2.7.1 Dispatch/station control

Dispatch/Station control is responsible for the operating set points (V_{dc}, V_{ac}, etc) and the operating modes to meet the requirement of DC and AC systems. By definition, the control mode refers to the functionality control sets and structures which a converter operates (DC voltage control, power control or frequency, and AC voltage control versus reactive power or power factor control). The dispatch commands have to be controlled by a system operator, similar to the AC systems [105].

2.7.2 Upper-level control

The upper-level control accepts reference signals (V_{dc}^*, V_{ac}^*, P^*, Q^*) from the dispatch and station control and outputs a voltage reference signal v_{abc}^*. The main influencing factor is the selection between 'non-island' and 'island' modes.

In non-island mode, VSCs are connected to a strong AC system with active synchronous generation. The entire control structure of non-island mode is depicted in Figure 2.25 where $d-q$ quadrature components af the AC currents are utilised. A phase-locked loop (PLL) is used to generate the angle reference θ from voltage V_{abc} at the point of common coupling (PCC). The reference currents i_d^* and i_q^* are generated by the active and reactive power loops, located at axes d and q respectively. The active power exchange (defined in d axis) is adjusted by DC voltage control or direct active power control. Similarly, reactive power exchange (defined in q axis) is adjusted by AC voltage control or direct reactive power control at the PCC. Reference signals i_d^* and i_q^* are then processed within the decoupled current controller. At this stage, voltage reference signals v_d^* and v_q^* are generated which, with the aid of the PLL, are transformed into abc frame and then sent to lower-level control.

For the sake of stable and safe operation of DC-side and AC-side networks, external control loops may be added to the upper-level control [106–108]. Such control loops enable advanced active and reactive power sharing between VSCs connected to the same system, but also between VSCs and AC networks (including wind farms) [109–111]. Those assist on maintaining a safe range for AC/DC voltage [112], frequency [35, 113] but also enhance the system stability considering AC and DC dynamics [31]. Typical droop controllers can be seen in Figure 2.26 which can be characterised according to the following three categories:

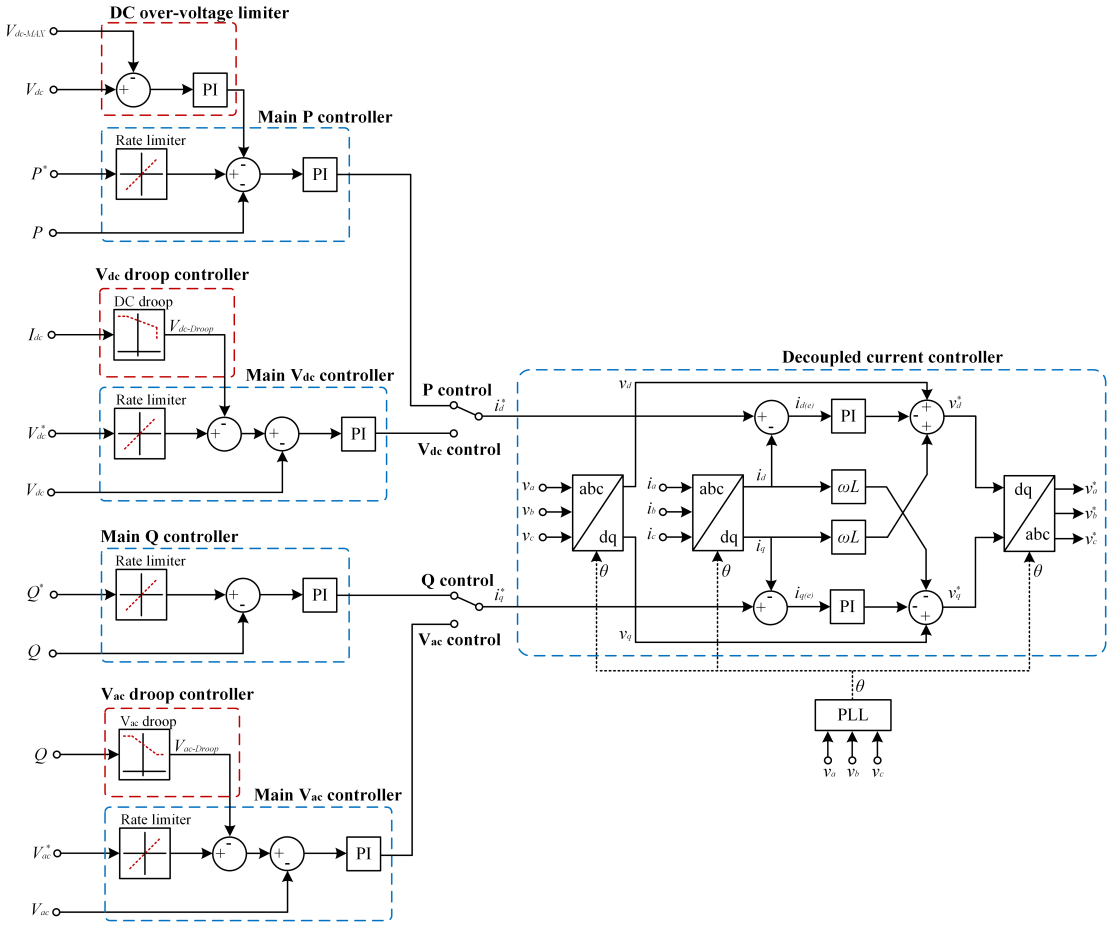
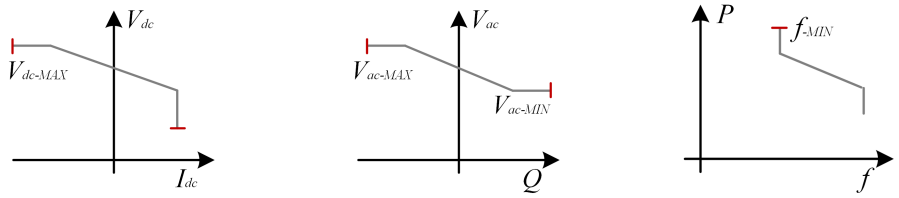


Figure 2.25: Upper-level control structure (non-island control mode).

- **DC voltage droop:** is used when multiple converters operate in DC voltage control mode.
- **AC voltage droop:** is used when multiple converters operate in AC voltage control mode, in conjuction with other AC voltage regulating devices in the AC side (e.g. STATCOMS, SVCs, etc).
- **Frequency droop:** is used when a converter is operating in direct active power control mode and is required (usually by dispatch control and system operator) to have primary functions for the AC-side stability.

Island control mode is adopted when VSCs are connected to an AC system with asynchronous generation (e.g. wind farms), weak grids or passive loads. As can be seen from the structure of island mode in Figure 2.27, the underlying control procedure is carried out using the voltages on d axis. Since there is no strong synchronous generation on the AC side, the need for grid synchronisation is eliminated; hence, there is no



(a) DC voltage - DC current

(b) AC Voltage - Reactive power

(c) Active power - frequency

Figure 2.26: Droop functions. DC current flows from the converter into DC system and Positive Q and P flows from the converter into AC system.

decoupled current control requirement. Specifically, the angle reference θ^* is directly generated from a voltage oscillator [114]. Another benefit of this approach is that a PLL can be eliminated as the frequency and phase of the AC voltage are directly set by the controller itself [115].

Additional frequency droops may by added when the rated power of the AC system is comparable to the VSC's, and hence the power exchange can lead to significant frequency deviations. AC voltage droops are usually required when more than one AC voltage controlling units are connected to the same bus.

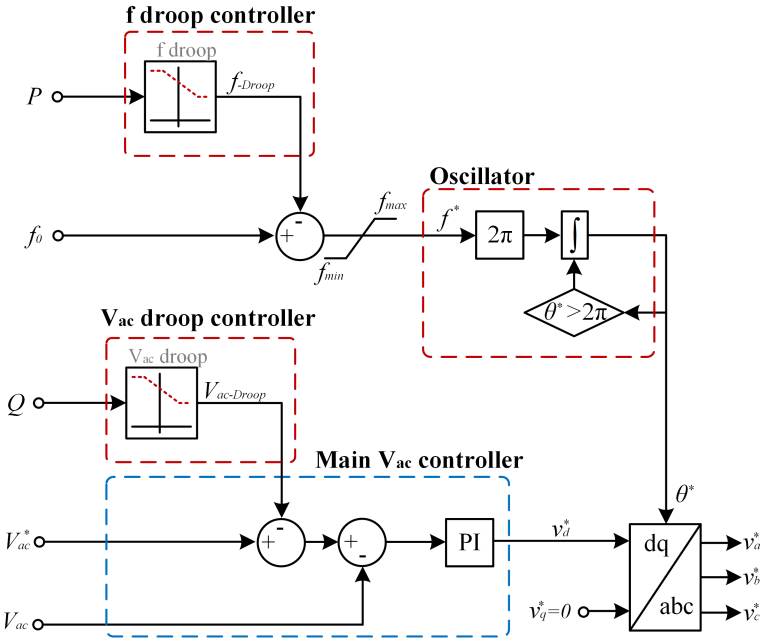


Figure 2.27: Upper-level control structure (island control mode).

2.7.3 Lower-level control

The lower level controls are responsible for the development of firing pulses, necessary to generate the AC waveforms v^*_{abc} that were requested by the upper-level controls. The structure of such control can change significantly according to the utilised valves, converter architecture (i.e. two-level, three-level, MMC, etc.) or the MMC sub-module configuration (e.g. half-bridge, full-bridge, mixed-cell, etc). In the case of MMC (which is main converter technology in the studies presented in this thesis), the following three major operations are included within the lower level control.

- **Modulation:** The purpose of a modulator is to generate the required switching signals for the semiconductor devices on the basis of user defined inputs. Modulation techniques include Phase Disposition PWM (PD-PWM) [116, 117], Phase Shift PWM (PS-PWM) [118–120], Space Vector PWM (SV-PWM) [121], Selective Harmonic Elimination (SHE) [122–124] and Nearest Level Control (NLC) [61, 125]. Due to the increase of number of levels in MMCs, the NLC has been found to be the simplest and yet most effective [126].

- **Circulating Current Suppression:** During unbalanced grid voltage conditions, the converter legs are under different voltage levels. This voltage variation results in the generation of currents inside the converter, known as circulating currents [127]. Such current have negative sequence and double the fundamental frequency [59], and introduce higher power losses, voltage fluctuation and hence thus reduce the power transmission efficiency and increase the investment of MMC-HVDC in steady-state [128, 129]. For this reason additional control loops are included within the lower-level control layer in order to remove the their existence. Typical concepts include the Proportional-Resonant Circulating Current Suppression Controller (PR-SCCC) or q-d Circulating Current Suppression Controller (d-q-CCSC).

- **Capacitor voltage balancing:** Since in MMCs there is a lack of common DC-link capacitance, the total capacitance in now distributed within series-connected submodules on each arm. One of the most important challenges is to balance the voltage across the series-connected capacitors at their nominal values and hence achieve power equilibrium among the submodules [64]. To meet this requirement, a few methods are reported in [69, 70, 130–135], however, the least computational and sophisticated voltage balancing algorithm is always favoured.

2.8 Converter Models

Full scale modelling of MMC in electromagnetic transient simulation software is a computationally intensive task, both in term of memory and simulation time. Such an excessive computational burden is introduced by the need to include thousands of IGBTs and other passive and active components (e.g. capacitors, inductors, etc.), which in turn increase the number of nodes and matrices to be solved.

In an attempt to overcome these challenges, different modelling approaches have been proposed by working groups and researchers [13, 29, 104, 105, 136–145]. The main idea is to reduce the number of electrical nodes in converter model while maintaining simulation accuracy, depending on the type of study and the required depth of analysis. Based on the simplification and assumptions, seven major types of models have been recognised.

2.8.1 Type 1: Physics model

This type of model is illustrated in Figure 2.28, and each IGBT valve device is represented by the full physics model. This type of model is not suitable for grid studies as the complexity and number of nodes would require significant computational power. However, this type of model is used mainly for thermal analysis, switching characteristics of valve devices [137, 138]; hence, it is useful for submodule design.

2.8.2 Type 2: Fully-detailed model

In this approach, the valve devices of each submodule are modelled as ideal switches while the diodes are modelled as non-ideal, non-linear resistances [139] (utilising classical characteristics of commercially available diodes). This model is used to study issues related to switching characteristics and losses of valved devices and also for validation of other simplified models. Further studies could be carried out such as capacitor voltage balancing, circulating currents, controller tuning, power flows and faults, but the simulation time would be excessive (especially for increased number of submodules).

2.8.3 Type 3: Simplified switchable resistances model

In this model type, semiconductor devices (both IGBT and diodes) are simulated as resistors (see Figure 2.30) [13, 139, 140] with two values: one small value for the ON state and one large value for the OFF state. The resistance value depends on the gate signal

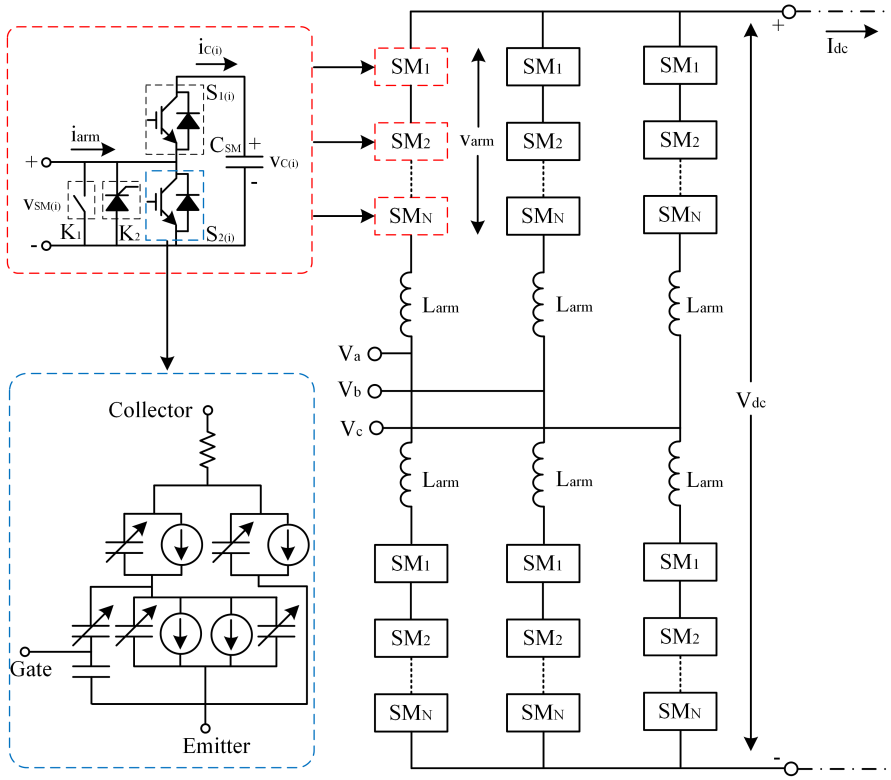


Figure 2.28: MMC Type 1.

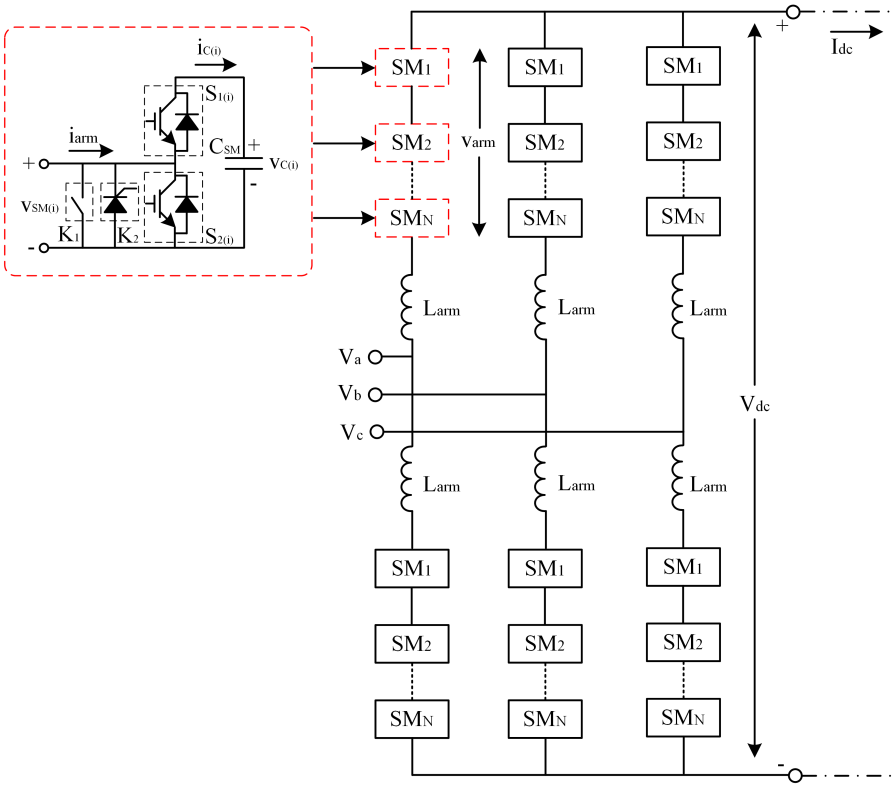


Figure 2.29: MMC Type 2.

and the current/voltage. The same studies for which Type 2 is used may also be carried out with this model, but with added speed. As in Type 2, further studies could be carried out such as capacitor voltage balancing, circulating currents, controller tuning, power flows and faults, but the simulation time would be excessive (especially for increased number of submodules).

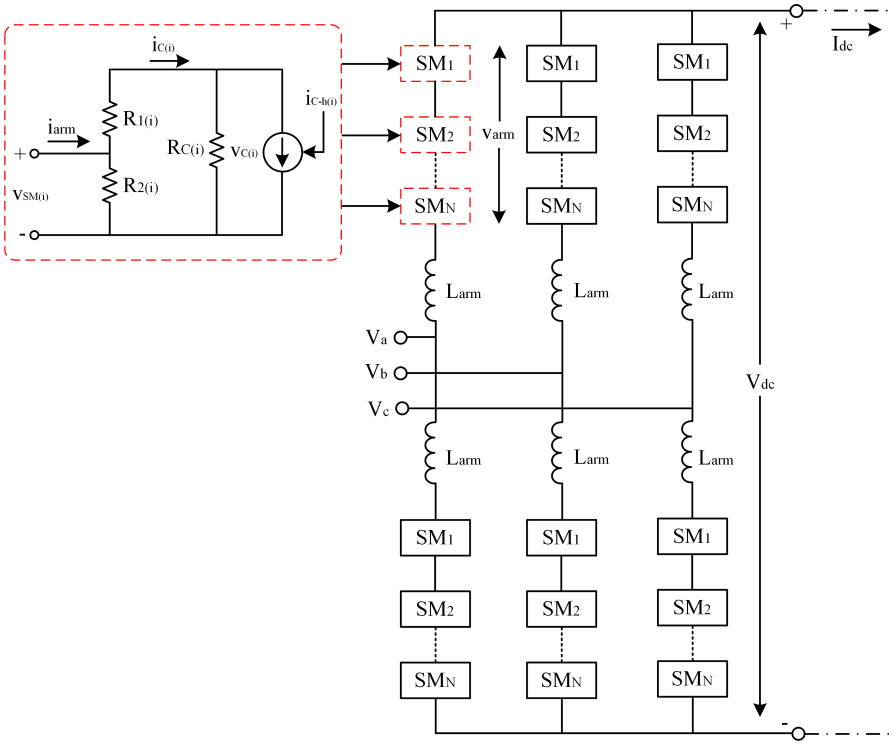


Figure 2.30: MMC Type 3.

2.8.4 Type 4: Detailed equivalent model

The converter response of this modelling approach is achieved through controlled voltage and current sources both for AC and DC side (see Figure 2.31), which replace the submodules in each converter arm [104, 139, 141, 142]. The signals driving the controlled sources may include harmonic contents from modulation control or fault-blocking behaviour (OFF state). The main advantage of this approach is that the number of nodes is significantly reduced, and thus enabling ultra fast simulation. Such models are suitable for studies related to circulating currents, controller tuning, power flows and faults without compromising the accuracy of the response.

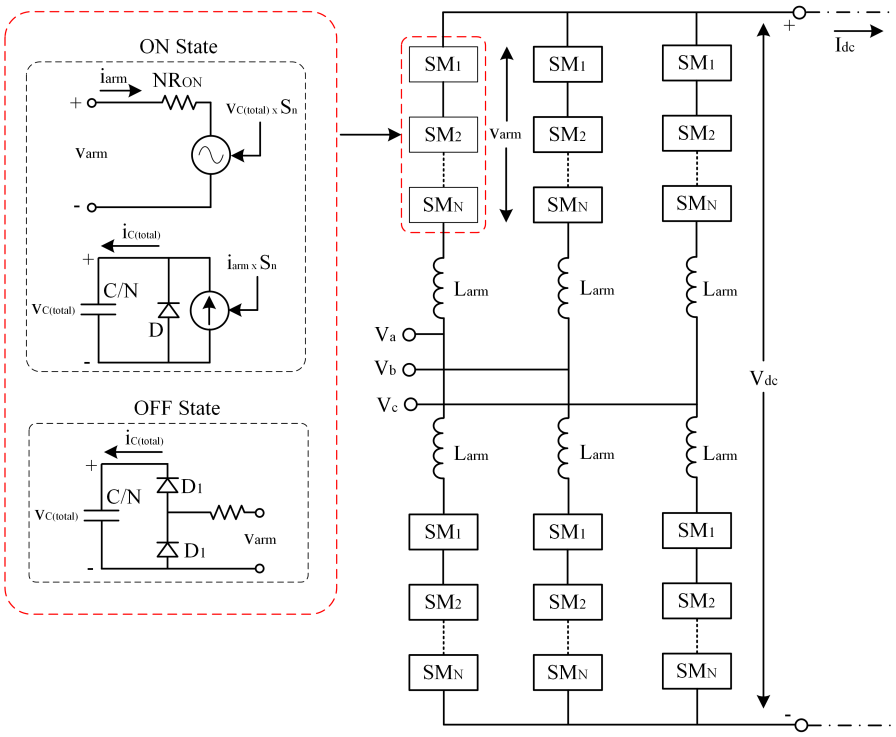


Figure 2.31: MMC Type 4.

2.8.5 Type 5: Average value model

In the average value models, the submodules are not explicitly modelled; the entire MMC behaviour is represented using controlled voltage and current sources [139, 143, 144] as illustrated in Figure 2.32. The controlled sources include the harmonic content from the modulation control (or switching functions) in the AC voltage waveforms. With this model type studies related to wider power systems may be carried out. These include load flows, transients involving disturbances on AC systems or design and tune of high level control systems (droop, upper-level, etc.)

2.8.6 Type 6: Simplified average model

Simplified average models (also called phasor models, RMS models or fundamental frequency models) are based on the assumption that all harmonics are neglected while a perfectly sinusoidal signal is present. As seen in Figure 2.33, the AC side representation of the entire MMC is a voltage source behind an impedance (equvalent for transformer and filters) while for the DC side, a current source with the equivalent MMC capacitor is present [29, 145]. Since the total MMC is over simplified, such model type enables large time frame studies from seconds to tens of hours.

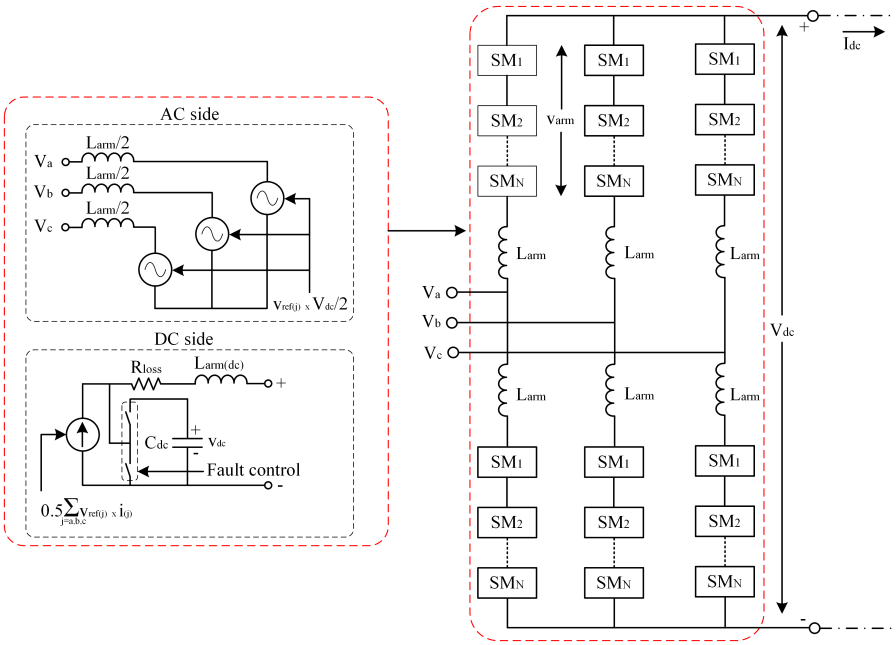


Figure 2.32: MMC Type 5.

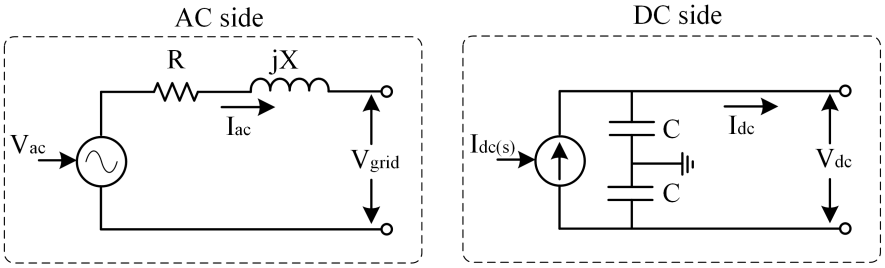


Figure 2.33: MMC Type 6.

2.8.7 Type 7: RMS load flow mModel

Similar to Type 6, this model follows the same description and any converter transformer shall be represented by an explicit transformer model in the power flow data. This model can be used in power flow analysis for large AC and DC grids also for power system planning studies. The main areas for the application of power flow calculations can be divided in normal and contingency system conditions.

2.9 Transmission Line Models

Power system networks have profound dynamic characteristics containing behaviour in the very wide frequency zone from DC to surge phenomena. As such, it is of major importance to understand and represent the behaviour of power systems all over the spectrum of interest. Different line models for steady-state and transient representation

are presented in this section and can be allocated into three main categories as illustrated in Figure 2.34.

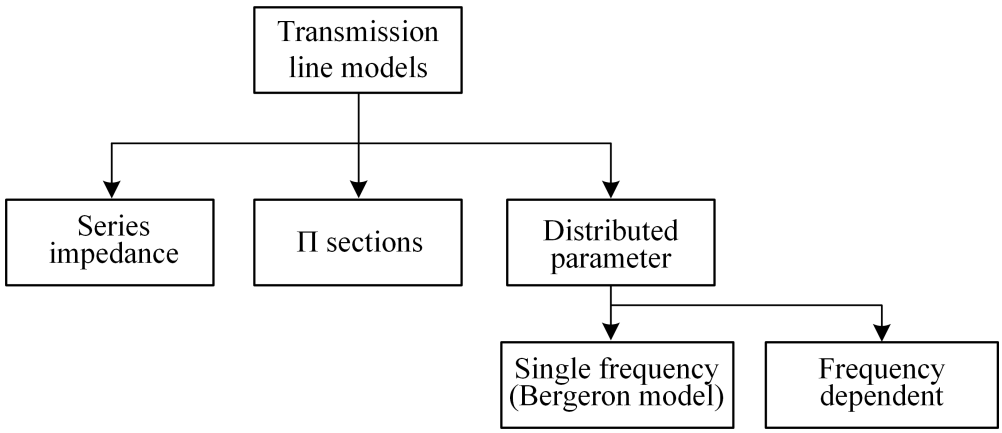


Figure 2.34: Overview of transmission line models.

2.9.1 Series impedance RL

The simplest transmission line model consists of a single impedance (with series $R-L$ components), as illustrated in Figure 2.35. In such representation any capacitance is neglected. With regards to HVDC studies, this model is only accurate for load flow calculations. As such it cannot be adopted for representation of transient phenomena especially when long transmission lines are involved.

Figure 2.35: Transmission line model based on $R-L$ series impedance.

Such representation has been utilised for fault studies in medium voltage DC cables in [146, 147] and also for calculation of short-circuit currents in DC auxiliary installations in power plants and substations in the IEC-61660 standard [148].

2.9.2 Lumped Π sections

For this transmission line model, resistance R, inductance L, capacitance C and conductance G are considered and uniformly distributed along the line. An approximate model of the distributed parameter line is obtained by cascading several identical Π sections, as shown in Figure 2.36.

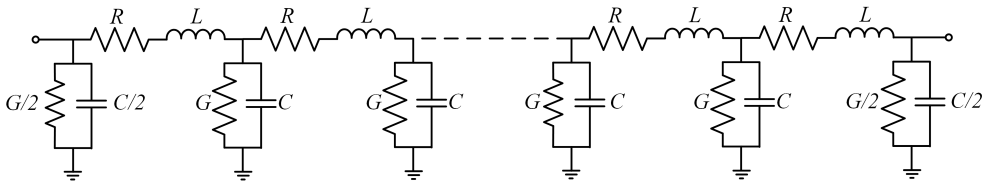


Figure 2.36: Transmission line model based on cascaded lumped Π sections.

An approximation of the maximum frequency range represented by the Π line model is given by

$$f_{max} = \frac{Nc}{\pi l} \tag{2.1}$$

where N the number of cascaded Π section, c the travelling wave velocity and l the total length of the line.

For studying interactions between a power system and control systems, this simple model could be sufficient. However, for studies related high-frequency transients (in the kHz-MHz range) and long transmission lines, multiple Π sections with small length should be used. The models generally utilising cascaded Π sections result in a poor representation of the cable modes in the state-space plane. This can lead to false conclusions on the dynamic response and stability margin of HVDC systems [149]. Moreover, due to the additional reflections at the junctions between two neighbouring Π sections, the resulting waveforms can be artificially distorted [150]. Cascaded Π sections have been utilised to simulate the HVDC cables for transient studies and converter control in [151, 152].

2.9.3 Distributed parameters

When transmission lines are modelled considering distributed parameter, representation of travelling wave theory is actually considered.

Figure 2.37: Transmission line model based on Bergeron approach.

The Bergeron model represents the total system inductance L and capacitance C in a distributed manner (as opposed to lumped Π sections). Specifically, it is equivalent to an infinite number of series-connected Π sections except that the total system losses are approximated by adding series lumped resistance elements into the loss-less, distributed parameter branch as shown in Figure 2.37.

Taking into account the total resistance R, the loss-less line is divided into two segments, with length equal to $l/2$ [153]. Each segment has an $R/4$ resistance at each end, and hence when such segments are combined, a lumped resistance of $R/2$ in the middle and $R/4$ at each end is formed.

The frequency dependent models aims to represent the full frequency dependence of a transmission system and considers multimodal wave propagation. These models represent not only the total system inductance L and capacitance C in a distributed manner but also the resistance R (as opposed to Bergeron model). The representation over a wide frequency range is achieved by solving the line parameters at many frequency points and hence such models are not very computationally efficient.

Distributed parameter models have been used for many transient-based applications including fault location and protection [154–158].

2.10 Summary

In this chapter a comprehensive literature review of the background material regarding HVDC grids has been presented. The review included network architectures, converter designs and configurations, transmission lines and the available grounding options. Additionally, the review included important material related to DC protection such as state-of-the-art circuit breakers and the available measuring techniques for DC voltage and current measurements.

The review of the background material contributed towards choosing the most suitable network components for realistic modelling of HVDC grids. Specifically, regarding to the network architecture, a symmetric monopole has been adopted due to its unique characteristic that eliminates the AC feed during pole to ground faults and at the same time the AC-side transformer is not exposed to DC stresses. Moreover, with regards to DC breaker, the HbCB concept has been put forward. This was based on the fact that such breaker has been found to posses the best total efficiency regarding cost, losses and applicability. As such, it is considered as the possible candidate for interrupting DC-side faults in future MTDC grids. For the selection of converters two major architectures have been considered, namely two-level and half-bridge MMC. This was based on the fact that the two-level converter is already installed in numerous HVDC-based transmission systems and also in back-to-back configurations. Additionally, the MMC is adopted in a few installations so far, while it is considered to be the key player to future and

already-planned HVDC projects.

This chapter assisted also towards selecting the most suitable modelling approach for MMC. In particular, the models of power converters utilised in this thesis are based on 401-level Type 4 half bridge MMCs. Such a representation has been validated against fully detailed models, and has been demonstrated to accurately represent the converter behaviour during steady-state, transient and fault conditions while remaining numerically stable and computationally efficient.

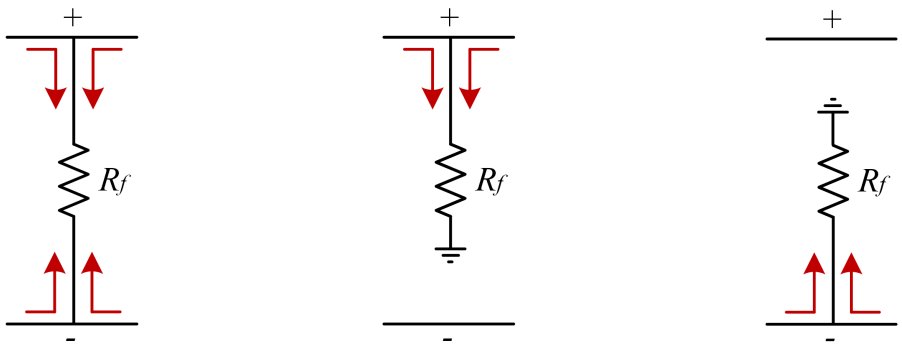
Last but not least, the background material regarding the modelling representation of transmission lines was also of major importance. Specifically, the modelling of HVDC grids and the subsequent development of the proposed protection and fault location schemes, was based on models belonging to distributed parameter family. This was based on the need to capture all the transient phenomena on the high frequency range (kHz to MHz).

Chapter 3

Converter Fault Analysis

VSCs are highly vulnerable to DC-side faults, such as DC-link short circuits, DC cable short circuits and DC cable ground faults. Among them, cable ground faults usually occur more often than in other parts of the system, and are mainly caused by insulation deterioration or breakdown, electrical stresses, environmental conditions, ageing and physical damage.

Within the scope of developing protection and fault location schemes (which is one of the primary objective of this thesis), it is essential to characterise DC-side faults and their dependencies on converter topology, fault type, fault resistance and operating conditions. Different types of DC-side faults (i.e. DC cable ground faults (pole-to-ground faults) and DC cable short circuits (pole-to-pole faults)) are analysed, simulated and discussed in the following subsections. The fault model utilised for the studies presented in this thesis is depicted in Figure 3.1.



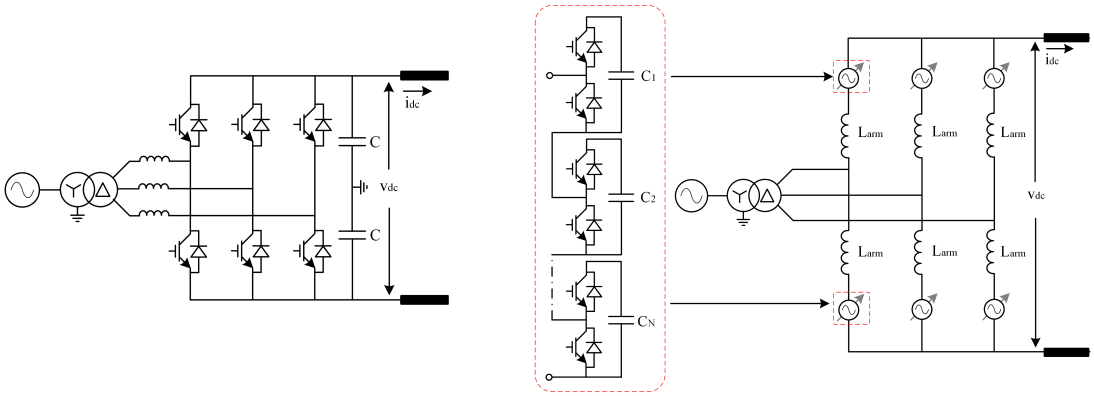
(a) Pole-to-pole fault

(b) Positive pole-to-ground fault

(c) Negative pole-to-ground fault

Figure 3.1: Fault model representation.

In this chapter, the fault analysis is carried out only from the converter point of view, analysing the stages and the corresponding equivalent circuits on which faults can be decomposed. Such studies have been implemented considering two major converter architectures, namely two-level and half-bridge MMC. The configuration of such converters are shown in Figure 3.2; the associated parameters are listed in Table 3.1. The converters operate at a symmetric monopole configuration at $\pm 400\ kV$, connected to a 300 km DC line and the AC transformer is grounded on the AC side. Since the purpose of these studies is the behaviour of the converters (and not transients occurring from the lines or cables), transmission lines are represented with lumped R,L,C elements.



(a) Two-level (b) MMC

Figure 3.2: Converter models for simulation-based analysis.

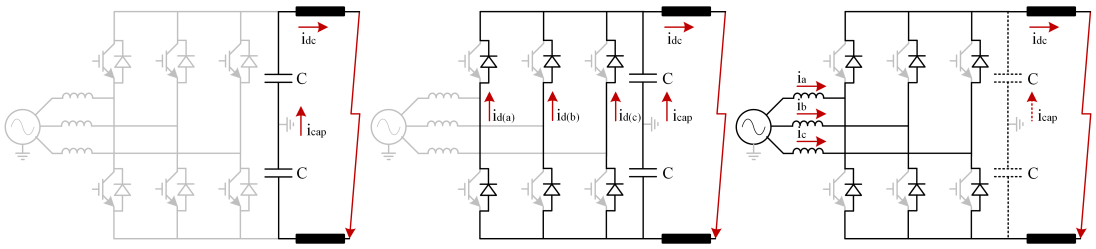
Table 3.1: System parameters for converter models.

Parameter	**Two-Level**	**MMC**
Number of levels	2	400
DC voltage [kV]	±400	±400
Rated power [MVA]	200	200
DC line length [km]	300	300
DC-link capacitance [μF]	100	N/A
Equivalent arm capacitance [nF]	N/A	20.84
Choke inductance [mH]	60	N/A
Arm inductance [p.u.]	N/A	0.1
AC voltage [kV]	400	400
AC frequency [Hz]	50	50
AC short circuit level [GVA]	40	40

3.1 DC-side Faults with Two-level Converters

3.1.1 Pole to pole faults

The DC cable fault response for two-level converters in general case can be characterised by three stages as illustrated in Figure 3.3.



(a) Capacitor discharge (b) Diode freewheeling (c) Grid feed

Figure 3.3: Fault stage analysis of two-level VSC during pole-to-pole faults.

Capacitor discharge: This stage is the immediate effect after the fault occurrence. Assuming that such stage is taking place within $t_0 \leq t \leq t_1$ the cable current and DC voltage can be calculated by

$$I_{dc} = I_{cap} = C_{eq}\frac{\partial v_{dc}}{\partial t} = -\frac{I_{dc}\omega_0}{\omega}e^{-\gamma t}sin(\omega t - \xi) + \frac{V_{dc}}{\omega L_{eq}}e^{-\gamma t}sin(\omega t) \tag{3.1}$$

$$v_{dc} = \frac{V_{dc}\omega_0}{\omega}e^{-\gamma t}sin(\omega t - \xi) - \frac{I_{dc}}{\omega C_{eq}}e^{-\gamma t}sin(\omega t) \tag{3.2}$$

where

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2},\ \omega_0 = \sqrt{\gamma^2 + \omega^2},\ \gamma = \frac{R_{eq}}{2L_{eq}},\quad \xi = tan^{-1}\left(\frac{\omega}{\gamma}\right)$$

$R_{eq},\ L_{eq},\ C_{eq}$ are respectively the equivalent resistance, inductance and capacitance (converter, cables/lines and any other lumped component).

Diode freewheeling: This is a conduction stage taking place after the capacitor discharge, when V_{dc} drops to zero. The line current at this stage [18, 146] is given by

$$i_{dc} = I_{dc}e^{(\frac{R}{L})t} \tag{3.3}$$

This stage can be very damaging for the anti-parallel diodes of the converter. In

particular, the diode carries one third of the line current as given by

$$i_{d(a)} = i_{d(b)} = i_{d(c)} = \frac{i_{dc}}{3} \tag{3.4}$$

Grid feed: This is the last and steady state stage of the fault. In this stage, the IGBTs are turned off for self-protection purposes. For this stage, the DC line current and voltage can be calculated by

$$I_{dc} = C_1 sin(\omega_g t + \lambda) + C_2 e^{-t/\tau} + \frac{C_3 \omega_0 e^{-\gamma t}}{\omega_n} sin(\omega t + \theta_{g0}) + \frac{C_4 e^{-\gamma t}}{\omega} sin(\omega t) \tag{3.5}$$

$$V_{dc} = R_{eq} I_{dc} + L_{eq} \frac{\partial I_{dc}}{\partial t} \tag{3.6}$$

where

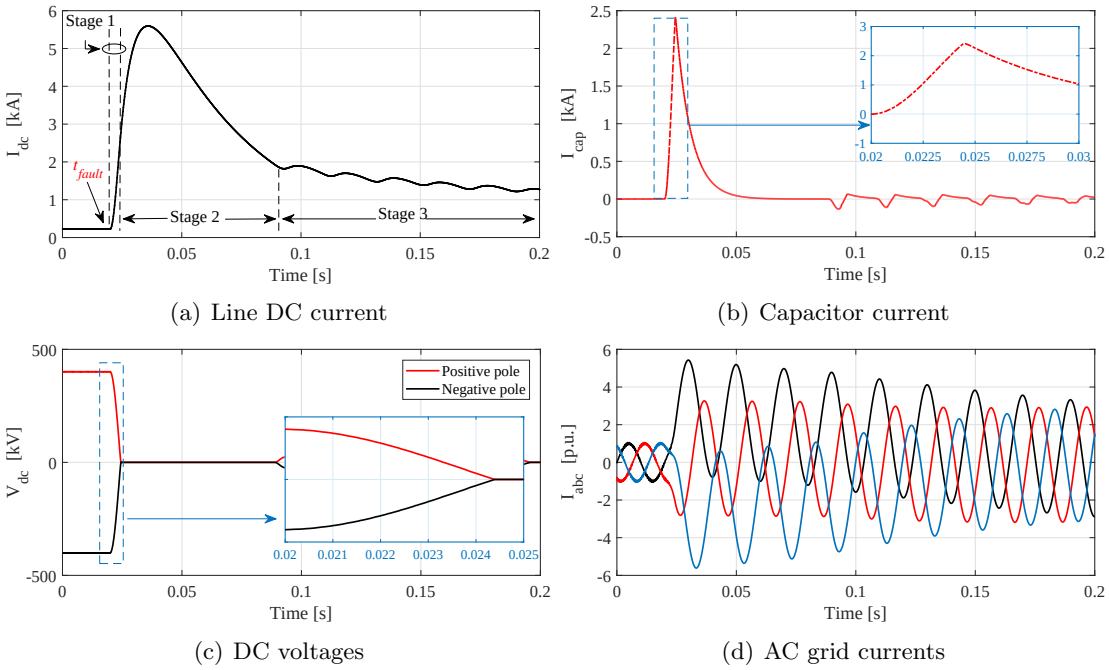
$$C_1 = I_m \sqrt{\left(1 - \omega_g^2 L_{eq} C_{eq}\right)^2 + \left(R_{eq} C_{eq} \omega_g\right)^2},\ C_2 = I_m \left(\frac{\tau^2}{\tau^2 - R_{eq} C_{eq} \tau + L_{eq} C_{eq}} \right)$$

$$C_3 = -C_1 sin\lambda - C_2,\ C_4 = \frac{C_2}{\tau} + \omega_g C_1 cos\lambda,\ I_m = I_{a1} - I_g sin(\theta_{g0} - \delta),\ \lambda = \theta_{g0} - \delta - \sigma$$

$$\sigma = tan^{-1} \left(\frac{R_{eq} C_{eq} \omega_g}{1 - \omega_g^2 L_{eq} C_{eq}} \right)$$

In Figure 3.4 simulation results are shown for a pole-to-pole fault. The fault is triggered at $t = 0.02$ s, and as can be seen in Figure 3.4(a) there is high DC current flowing into the line, where the fault stages are very distinct. It is observed that the capacitor is fully discharged within less 5 ms (Figure 3.4(b)), leading to DC voltage collapse (Figure 3.4(c)). It is worth noting that both positive and negative pole voltages collapse towards zero value. From the AC-side point of view, AC currents will reach an initial value of 5.0 p.u. and then fall around 2.0 p.u. during steady state, as shown in Figure 3.4(d). During AC grid freed stage, the capacitor will try to recharge (negative currents can be observed in Figure 3.4(b)) causing some further fluctuation in line DC current (Figure 3.4(a)).

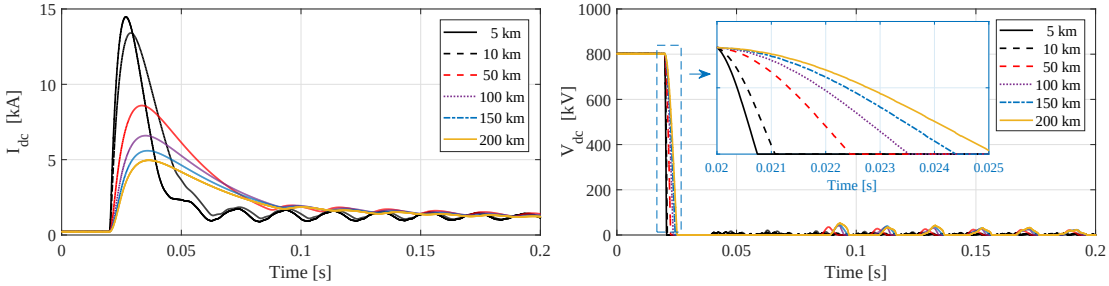
To further investigate the influence of distance-to-fault and fault resistance, simulation results are shown in Figures 3.5 and 3.6 for different distance-to-fault and fault resistance values respectively.



(a) Line DC current (b) Capacitor current

(c) DC voltages (d) AC grid currents

Figure 3.4: Simulated two-level VSC response during pole-to-pole fault.

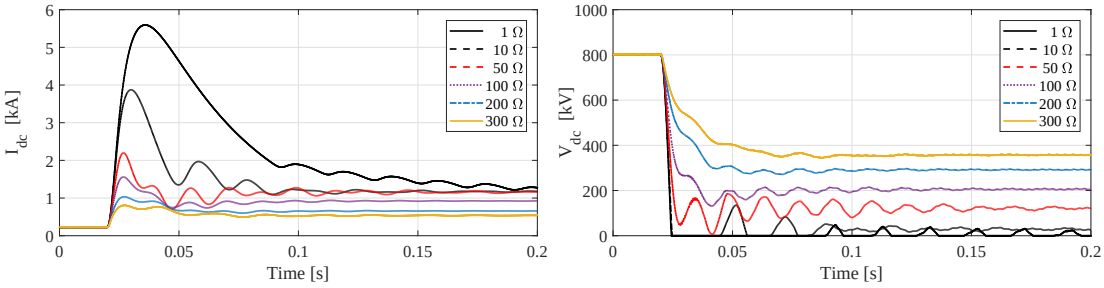


(a) Line DC current (b) DC-link voltage

Figure 3.5: Simulated two-level VSC response during pole-to-pole fault at different distances.

By observing Figure 3.5, it is evident that the location of the fault is of great influence on the system performance during pole-to-pole faults. It seems that as the fault location increases, the system response gets slower both for DC currents and voltages. This can be better noted in Figure 3.5(b), where a zoomed version of DC voltages are depicted. It is evident that DC currents have reduced maximum values, but also the rise time is increased. Accordingly, this has a great influence on DC voltage, as it takes more time to collapse towards zero. Such a response is actually expected; the higher the distance to the fault, the higher the values or R and L included in the fault current loop. Consequently, higher values of L would increase the rise time, while higher values of R would decrease the maximum level of current reached. The natural response of pole-to-pole fault can be

only limited by the 'portion' of the cable/line included and fault resistance in the fault current loop.



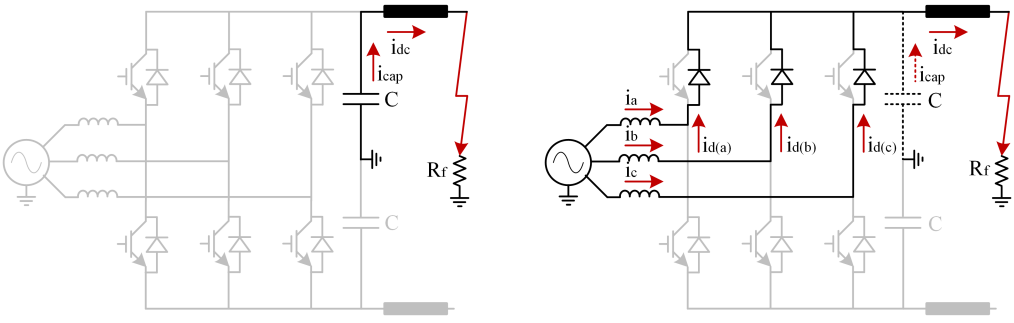
(a) Line DC current (b) DC-link voltage

Figure 3.6: Simulated two-level VSC response during pole-to-pole fault for different resistance values.

Fault resistance is also of great influence to the fault. Specifically, it is evident from Figure 3.6 that high resistance values limits the level of fault current and consequently the maximum voltage drop during the fault. Highly-resistive faults seem to be more challenging to detect; however, they are less harmful for the system.

3.1.2 Pole to ground faults

This type of fault is more likely to occur; however, relative to the aforementioned pole-to-pole faults, they are less harmful to the system. In practice, such faults are triggered when the insulation of the cable breaks and the live conductor touches the ground directly or through other conducting path. In this type of fault, the earthing arrangement of the system components plays a significant role, as different current loops can be formed. In Figure 3.7 the fault stage analysis of two-level VSC during pole-to-ground fault is depicted.



(a) Capacitor discharge (b) Grid feed

Figure 3.7: Fault stage analysis of two-level VSC during pole-to-ground fault.

Unlike pole-to-pole faults, the stage of diode freewheeling effect is completely eliminated in pole-to-ground faults due to the fact that there is no conducting return path between ground and diodes. Additionally, the resistance of the ground is added into the circuit analysis, which plays a significant role to the system response. The two-stage analysis of pole-to-ground faults is taking place as follows:

Capacitor discharge: In this stage DC-link capacitor discharges (only when middle-point is grounded), and is a long-time transient which can be expressed by [74, 146]

$$\begin{bmatrix} v_{cap} \\ i_{dc} \\ i_{ac} \end{bmatrix} = \begin{bmatrix} 0 & -2C_{eq} & 1/2C_{eq} \\ 1/L_{eq} & -R_f + R_{eq}/L & 0 \\ -1/L_{ac} & 0 & 1 \end{bmatrix} \times \begin{bmatrix} V_C \\ I_{dc} \\ I_{ac} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1/L_{ac} \end{bmatrix} V_{abc_g} \quad (3.7)$$

Under the condition of $R_f + R_{eq}/2 < 2\sqrt{L_{eq}/4C_{eq}}$, the solution of the second-order circuit natural response gives a non-oscillating discharge process.

Grid feed: This stage is taking place after the capacitor discharge (when actually its voltage drops close to zero). The steady-state fault DC current i_{dc} can be calculated taking into consideration the diode currents $i_{d(a)}$ by

$$i_{dc} = i_{d(a)} + i_{d(b)} + i_{d(c)} \quad (3.8)$$

$$i_{d(a)} = i_{d(b)} = i_{d(c)} = \frac{V_{ag}}{|Z|} \angle \alpha - \phi \quad (3.9)$$

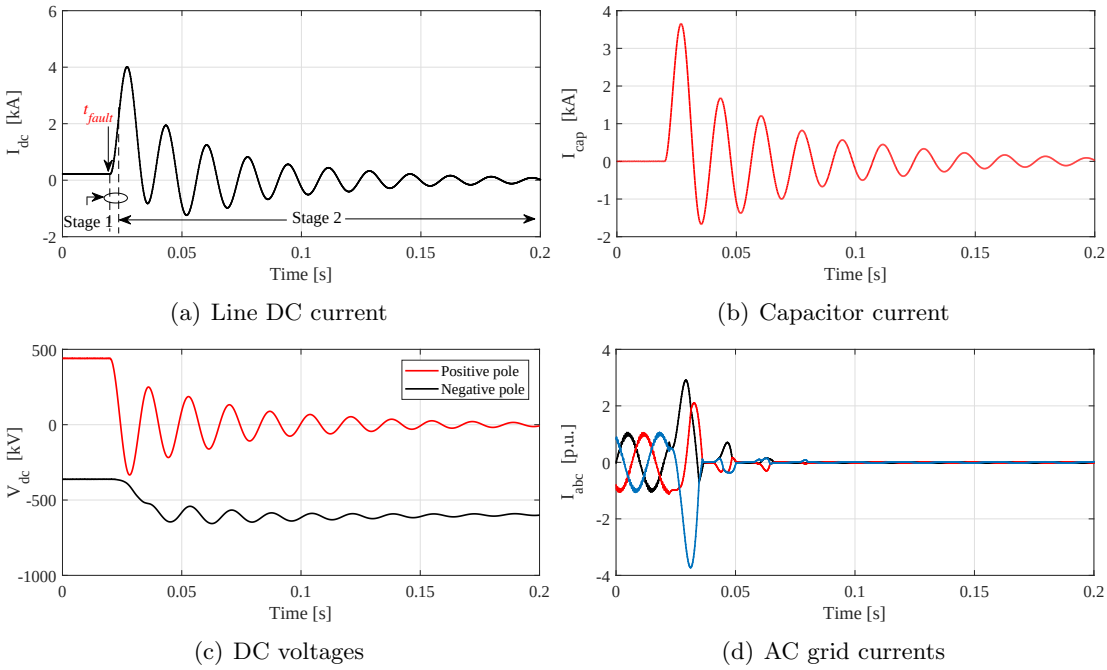
where $|Z|$ is the magnitude of the equivalent impedance Z:

$$Z = (R_f + R_{eq} + j\omega_s L_{eq}) \| (1/j\omega_s C_{eq}) + j\omega_s L_{ac} = |Z| \angle \phi \quad (3.10)$$

It should be noted that if the AC transformer is not grounded on the converter side, AC and DC sides are isolated and hence this stage is not occurring at all.

In Figure 3.8 simulation results are shown for a pole-to-ground fault. Such faults have a different impact on the system behaviour than pole-to-pole.

Initially, it can be observed from Figure 3.8(c) that DC voltage switches from symmetrical to asymmetrical, where the faulted (positive) pole voltage collapses towards



(a) Line DC current

(b) Capacitor current

(c) DC voltages

(d) AC grid currents

Figure 3.8: Simulated two-level VSC response during pole-to-ground fault.

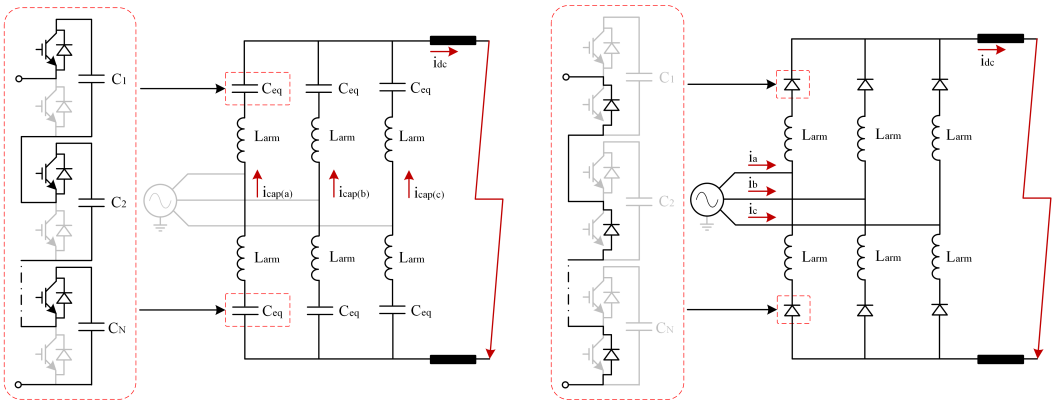
zero, and the healthy (negative) pole voltage jumps towards 2.0 p.u. When the faulted pole voltage reaches zero (Figure 3.8(c)) first stage (capacitor discharge) has finished and there is a transient taking place. In particular, DC-link capacitor is trying to recharge leading to an oscillation in line and capacitor current (Figures 3.8(a) and 3.8(b) respectively). As a result, this leads to an oscillation of DC voltage (Figure 3.8(c)) mainly observed at the faulted pole. It is worth telling at this point, that there is no diode freewheel conduction stage, as there is no return path among diodes and ground and hence the total DC-link voltage does not reach zero.

Moreover, it can be observed that after IGBTs are turned off there is no current feed from the AC system (Figure 3.8(d)), which is conflicting with the theoretical analysis shown in Figure 3.7(b). This is due to the fact that in the presented simulation-based studies presented in Figure 3.8, the converter is grounded on the grid side (converter side is ungrounded). Regarding the influence of fault resistance values and distance-to-fault, same behaviour is expected as shown for pole-to-pole faults.

3.2 DC-side Faults with MMCs

3.2.1 Pole to pole faults

Pole-to-pole faults in MMC-based systems are quite different from those in two-level converters. This is due to the fact that the total DC-link capacitance is distributed on each converter arm, and is no longer uncontrollable and free to discharge during the fault. Pole-to-pole faults can be analysed in two major stages as depicted in Figure 3.9.



(a) SM capacitor discharge (IGBTs ON) (b) Grid feeds (IGBT OFF)

Figure 3.9: Fault stage analysis of MMC during pole-to-pole fault.

SM capacitor discharge: After a DC-side fault occurs, the converter remain initially operational before the converter detects the fault and shuts down for self-protection. At this stage, IGBTs are held on, and the submodule capacitors discharge.

During operation of the MMC, half of the submodules on each converter phase are always turned on. Consequently, the equivalent capacitance on each converter phase during the fault is defined by

$$C_{phase} = C_{eq} = \frac{C_{SM}}{N_{SM}} \tag{3.11}$$

where C_{eq} is the equivalent capacitance of upper and lower part of each arm, C_{SM} is the capacitance of each sumbmodule and N_{SM} is the total number of submodules per arm.

The total converter capacitance is then defined as

$$C_{MMC} = 3C_{eq} = 3\frac{C_{SM}}{N_{SM}} \tag{3.12}$$

Taking into account that $\sum(v_u + v_l)$ the sum of upper and lower arm voltages on each phase of the MMC, natural response of DC fault current can be calculated by

$$i_{dc} = 3\frac{C_{SM}}{N_{SM}}\frac{\partial V_{dc}}{dt} = 3\frac{C_{SM}}{N_{SM}}\frac{\partial \sum(v_u + v_l)}{dt} \tag{3.13}$$

or alternatively

$$i_{dc} = e^{-t/\tau}\left(-\frac{I_{dc}\omega_0}{\omega}sin(\omega t - \xi) + \frac{V_{dc}}{\omega L_{eq}}sin(\omega t)\right) \tag{3.14}$$

where

$$L_{eq} = \frac{2L_{arm}}{3} + L_{line},\ R_{eq} = \frac{2R_{conv}}{3} + R_{line}$$

$$\tau = 2L_{eq}/R_{eq},\ \omega = \sqrt{\frac{1}{L_{eq}C_{MMC}} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2},\ \omega_0 = \sqrt{\frac{1}{L_{eq}C_{MMC}}},\ \xi = arctan(\omega\tau)$$

Alternately, DC fault current i_{dc} can be calculated by the sum of the capacitive currents flowing through each converter phase. Specifically, the capacitive current on each phase can be calculated as

$$i_{cap(a)} = i_{cap(b)} = i_{cap(c)} = \frac{1}{L_{arm}}\int_{t_0}^{t} v_{L_{arm}}dt \tag{3.15}$$

where t_0 is the time instant of fault occurrence and $v_{L_{arm}}$ is the voltage across arm inductor L_{arm}.

Consequently, by using equation (3.15) total DC line current is the sum of arm currents and initial current I_{dc}

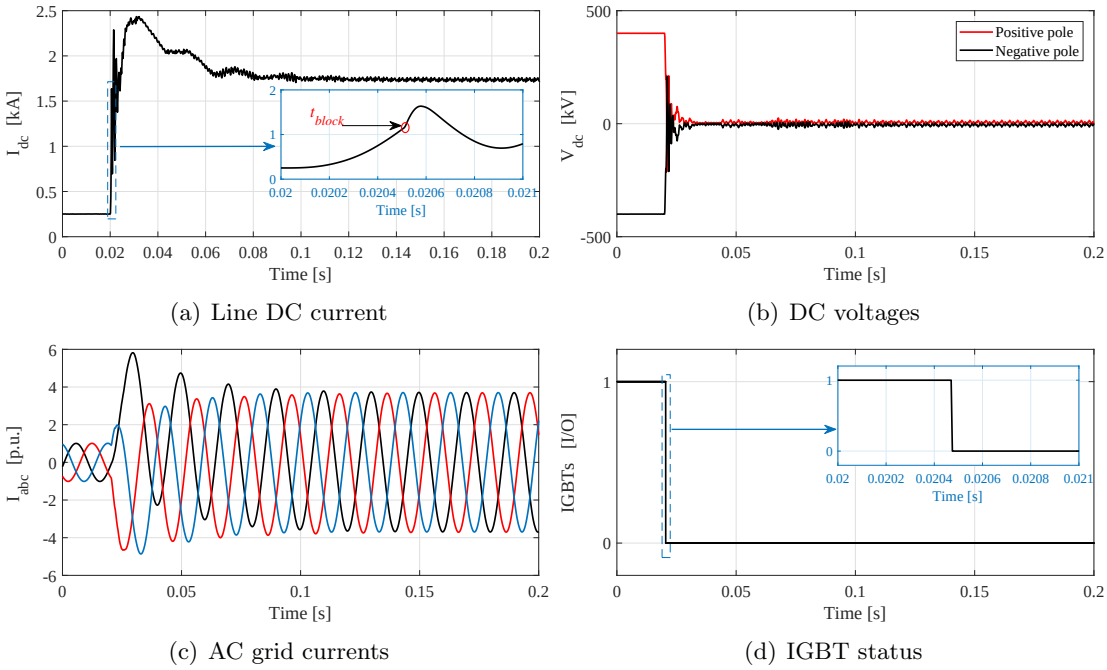
$$i_{dc} = I_{dc} + i_{cap(a)} + i_{cap(b)} + i_{cap(c)} = I_{dc} + \frac{3}{2L_{arm}}\int_{t_0}^{t} V_{L_{arm}} \tag{3.16}$$

Accordingly, the DC voltage response can be deduced taking into account i_{dc} [159]:

$$u_{dc} = R_{eq}i_{dc} + L_{eq}\frac{\partial i_{dc}}{dt} \tag{3.17}$$

Grid feed: This is the last stage of the fault when the IGBTs are turned off and current is flowing through anti-parallel diodes (Figure 3.9(b)) and MMC is actually operating as an uncontrolled rectifier. The response is similar with the two-level converter as described in Section 3.1.

In Figure 3.10 simulation results are shown for MMC response during a pole-to-pole fault. After fault occurrence at $t = 0.2$ s, the equivalent capacitance of the converter is discharging rapidly. After a few ms, IGBTs will turn off (Figure 3.10(d)), which denotes

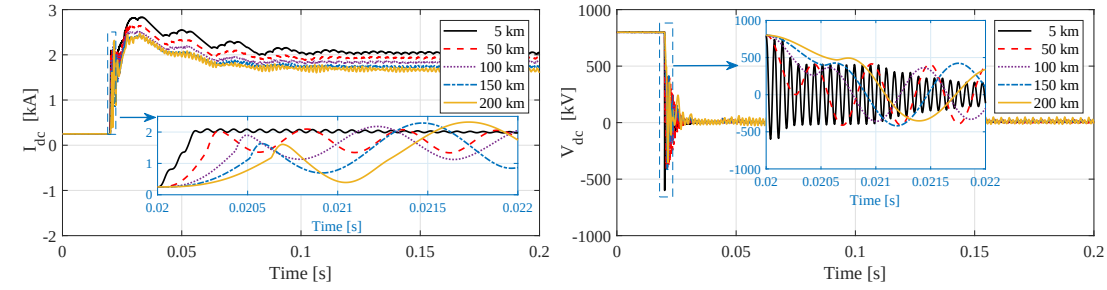


(a) Line DC current (b) DC voltages

(c) AC grid currents (d) IGBT status

Figure 3.10: Simulated MMC response during pole-to-pole fault.

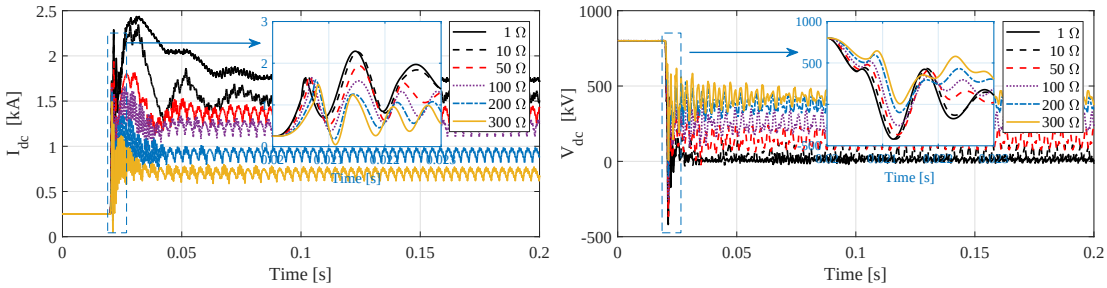
the end of first stage (SM capacitor discharge). During this stage DC voltage collapses towards zero both for negative and positive pole (Figure 3.10(b)). It worth noting here that in the case of MMC, DC voltage collapses faster, compared with the two-level. This is due to the fact that DC-link capacitor in two-level converter provides a DC voltage support, while in the case of the MMC, the equivalent capacitance stays connected only for a few ms, before it is bypassed. After IGBTs are turned off at $t = t_{block}$, fault will proceed to second stage when the MMC behaves as an uncontrolled rectifier, feeding current to the fault point. As depicted in Figure 3.10(c), the steady state current reaches values up to 4.0 p.u.



(a) Line DC current (b) DC-link voltage

Figure 3.11: Simulated MMC response during pole-to-pole fault at different distances.

The influence of fault resistance and distance to fault have been studied and results are shown in Figures 3.11 and 3.12 respectively. The same behaviour is observed with



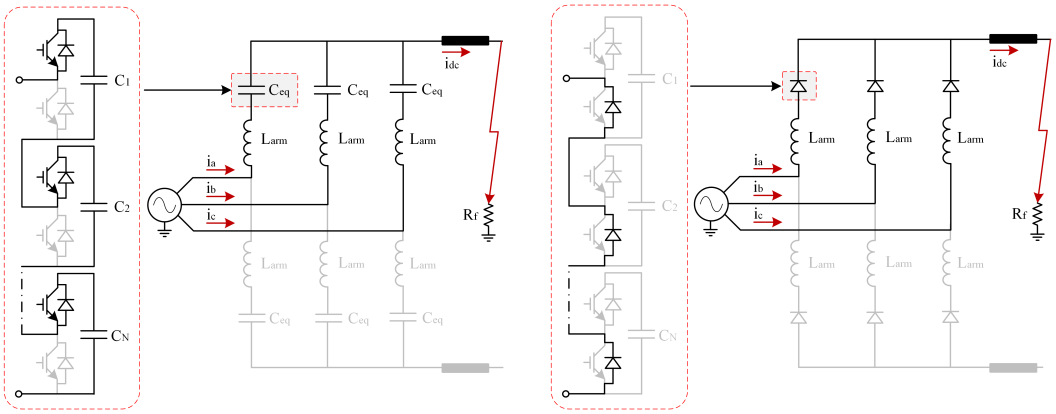
(a) Line DC current (b) DC-link voltage

Figure 3.12: Simulated MMC response during pole-to-pole fault for different resistance values.

the analysis described in Section 3.1 (fault analysis for two-level converters). As also expected, while distance and fault resistance increases, IGBTs take more time to turn-off, as the maximum permissible operating current (and hence equivalent thermal stress) takes more time to be reached.

3.2.2 Pole to ground faults

Pole-to-ground faults in MMC-based systems can be analysed in two major stages as depicted in Figure 3.13.



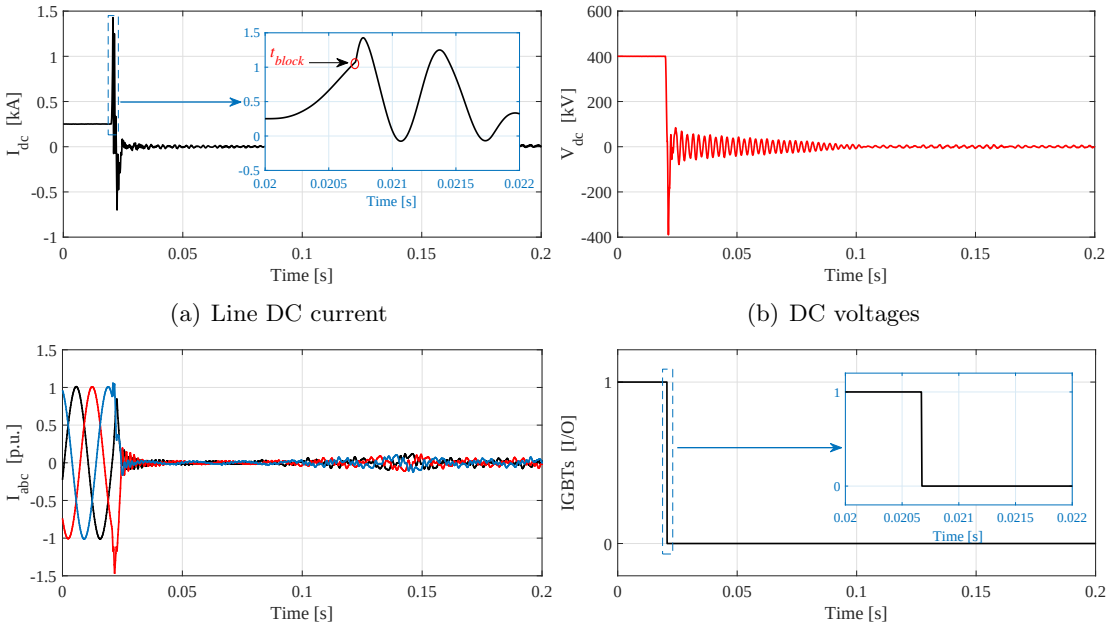
(a) SM capacitor discharge (IGBTs ON) (b) Grid feed (IGBTs OFF)

Figure 3.13: Fault stage analysis of MMC during pole-to-ground faults.

SM capacitor discharge: After a DC-side fault occurs, the transient begins with the submodule capacitors discharge. DC current and voltage can be again described using equations (3.11) to (3.17). The only difference can be found in the equivalent inductance L_{eq} and resistance R_{eq}. Specifically, at this case half of converter arm inductances (L_{arm}) and half of the cable impedance (only from faulted pole) is inserted in the fault current loop.

Grid feed : This stage is initiated after IGBTs are turned off. The steady-state fault DC current is the sum of the currents flowing from the AC on each converter's arm, taking into account that the AC transformer is grounded on the converter side. As in the case of two-level converter it can be calculated by utilising equations (3.8) to (3.10).

In Figure 3.14 simulation-based results are shown for a pole-to-ground fault for an MMC. After the fault occurrence at $t = 0.2$ s, DC current increases rapidly (Figure 3.14(a)) due to the discharge of the equivalent capacitance, and positive pole voltage collapses towards zero (Figure 3.14(b)). After around 5 ms, IGBts turn-off (Figure 3.14(d)) and DC current drops to zero due to zero AC current infeed. What is worth noting here is the fact that there is no oscillatory response of DC current and voltage as in the case of pole-to-ground faults for two-level converters. This is due to the fact that there is no significant capacitance in the circuit (after IGBTs are turned off) charging and re-charging.



(a) Line DC current

(b) DC voltages

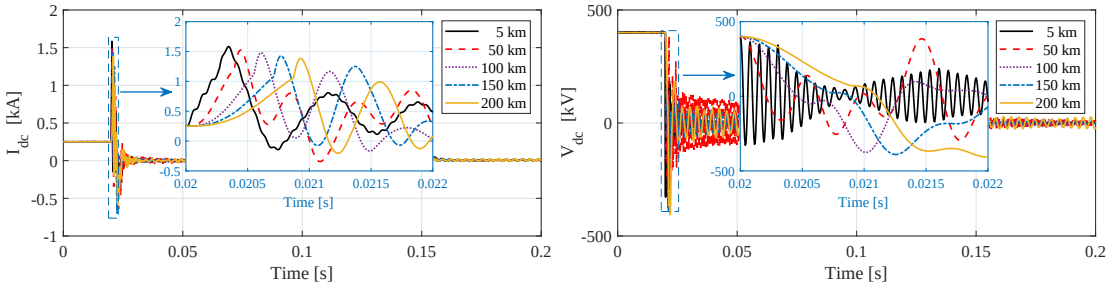
(c) AC grid currents

(d) IGBT status

Figure 3.14: Simulated MMC response during pole-to-ground fault.

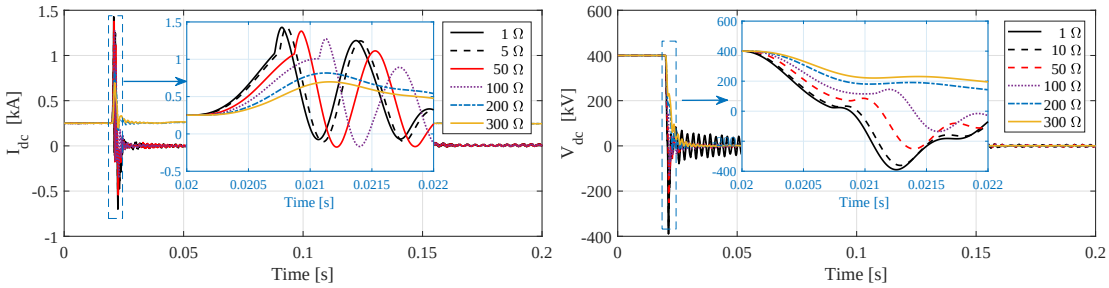
The effect of distance to fault and fault resistance is depicted in Figures 3.15 and 3.16 respectively, and has the same impact as shown in previous studies. What is interesting is that in the case of highly resistive faults (i.e $R_f = 200, 300\ \Omega$), the IGBTs are not turned off due to limited fault current amplitude (i.e. the maximum current threshold is not reached). This results in continuous operation of the converter and verifies that highly-resistive faults are in general more challenging to be detected (especially by simple

over-current schemes).



(a) Line DC current (b) DC-link voltage

Figure 3.15: Simulated MMC response during pole-to-ground fault at different distances.



(a) Line DC current (b) DC-link voltage

Figure 3.16: Simulated MMC response during pole-to-ground fault for different resistance values.

3.3 Summary

This chapter described the outcomes of a detailed, theoretical but also simulation-based transient analysis of DC-side faults. The characterisation has been carried out considering various states of the converters during DC-side faults, their dependencies on converter topology, fault type, fault resistance and operating conditions. The analysis took place considering mainly DC-side faults from the converter point of view, analysing the stages and the corresponding equivalent circuits on which faults (pole-to-pole and pole-to-ground) can be decomposed. From the analysis the following observations can be reflected:

- Pole-to-pole faults are considered more severe due to the fact that they force the system to collapse, but they are less likely to occur. On the other hand, pole-to-ground faults are less harmful but more likely to happen.
- It is necessary to isolate the DC-side faults to prevent voltage collapse and before excessive current flow through system components (e.g. power electronic vales).

This means that the DC-side faults have to be cleared within a few milliseconds, including fault detection, localisation and isolation.

- DC fault signatures are predominately defined by the energy contained on the DC side at the moment of fault inception. Therefore, the AC side does not significantly contribute to the DC fault current during the first few milliseconds after the fault.
- The fault position appears to have the same effect on both types of faults, i.e. fault peak and rate of change of current are both reduced with distance to fault. In particular, for pole-to-pole faults this is clearly evident as the line impedance is the main current limiting factor. However, for pole-to-ground faults the fault resistance is considered as one of the main influencing elements so the impact of fault position cannot be pre-determined.
- System behaviour is highly dependent on earthing arrangements implemented and needs to be taken into account when developing operational procedures including fault detection and protection strategies.
- Different converter architectures introduce different fault signatures the first few milliseconds of DC-side faults. This is due to the different arrangement and allocation of power components (e.g. capacitors, inductors, etc.) which make the equivalent DC energy to vary at the moment of fault inception.

The comprehensive fault characterisation presented in this chapter acted as preliminary knowledge for the design of DC side fault-related systems for HVDC networks. It has been identified that there is a need for fast DC protection solutions. Specifically, a protection system should be able to identify and isolate a DC-side fault in less than 5 ms. This is due to the fact that after such time DC-side collapses and controllability and restoration capability of the DC grid is lost.

Chapter 4

DC Fault Transient Phenomena

In this chapter, a number of systematic studies are presented considering short-circuit DC-side faults in MTDC networks and resulting in fast transient phenomena known as travelling waves. These are associated with some unique features such as magnitude, polarity and time intervals. As such, the utilisation of travelling wave-based techniques for fault-related studies, is based upon their successive identification on voltage and/or current traces. Since travelling waves is the natural mechanism for the generation of fault currents and voltages, it can be considered one of the best techniques for studying faults in power systems. This is the reason that travelling wave-based techniques is well established in AC systems for protection and fault location applications.

It should be highlighted that travelling waves do not depend so much on the converter topology (and generally on the power source), but rather depend on components external to the converter such as lines/cables, DC breakers and line termination components. For such studies, cables and lines are modelled with a detailed approach, including travelling wave representation of the transmission line. Additionally in this chapter, advanced signal processing techniques (belonging to the Wavelet Transform group) are introduced and applied to accurately analyse transient signals. Emphasis is given to their applicability in HVDC protection and fault location schemes.

4.1 Introduction to Travelling Waves

4.1.1 The travelling wave equation

During abrupt changes (e.g. faults, sudden load changes, breaker switching, etc) on a network, electromagnetic waves (also known as surges) are generated which travel along transmission lines and/or cables. The speed of propagation can be close to the speed of light.

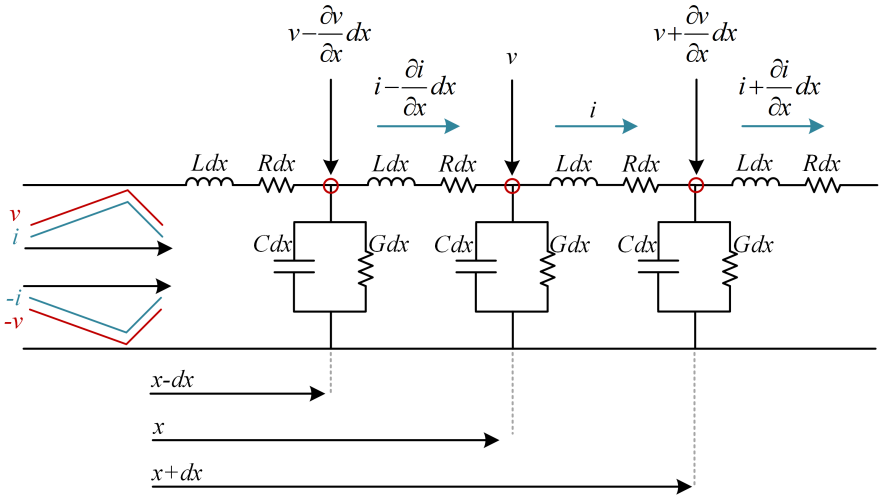


Figure 4.1: Distribution circuit of transmission line.

In Figure 4.1 the distribution circuit of a transmission line is shown, where $v(x,t,)$ and $i(x,t,)$ express the voltage and current at point x and time instant t. Consequently, applying the 1^{st} and 2^{nd} Kirchoff's law to a line section between two points (i.e. points x and $x+dx$), the voltage and current distributions are given by

$$v(x,t) - \left(v(x,t) + \frac{\partial v(x,t)}{\partial x}dx\right) = Ldx\frac{\partial i(x,t)}{\partial t} + Rdx\ i(x,t) \tag{4.1}$$

$$-i(x,t) + \left(i(x,t) - \frac{\partial i(x,t)}{\partial x}dx\right) = Cdx\frac{\partial v(x,t)}{\partial t} + Gdx\ v(x,t) \tag{4.2}$$

which can be simplified to

$$-\frac{\partial v(x,t)}{\partial x} = L\frac{\partial i(x,t)}{\partial t} + Ri(x,t) \tag{4.3}$$

$$-\frac{\partial i(x,t)}{\partial x} = C\frac{\partial v(v,t)}{\partial t} + Gv(x,t) \tag{4.4}$$

where L, R, C, G is the inductance, resistance, capacitance and admittance per unit length of the line respectively and dx a small distance of line section.

Equations (4.3) and (4.4) can be rewritten into

$$\frac{\partial^2 v(x,t)}{\partial x^2} = LC\frac{\partial^2 v(x,t)}{\partial t^2} + (LG + CR)\frac{\partial v(x,t)}{\partial t} + RGv(x,t) \tag{4.5}$$

$$\frac{\partial^2 i(x,t)}{\partial x^2} = LC\frac{\partial^2 i(x,t)}{\partial t^2} + (LG + CR)\frac{\partial i(x,t)}{\partial t} + RGi(x,t) \tag{4.6}$$

where there is only one variable, namely voltage $v(x,t)$ or current $i(x,t)$. Each of these differential equations is called a *'travelling wave equation'* and is required as a starting point for the analysis of transient phenomena on transmission lines.

If the losses on a transmission circuit are negligible ($R = 0$, $G = 0$), equations (4.3) to (4.6) can be rewritten as

$$-\frac{\partial v(x,t)}{\partial x} = L\frac{\partial i(x,t)}{\partial t} \tag{4.7}$$

$$-\frac{\partial i(x,t)}{\partial x} = C\frac{\partial v(x,t)}{\partial t} \tag{4.8}$$

$$\frac{\partial^2 v(x,t)}{\partial x^2} = LC\frac{\partial^2 v(x,t)}{\partial t^2} \tag{4.9}$$

$$\frac{\partial^2 i(x,t)}{\partial x^2} = LC\frac{\partial^2 i(x,t)}{\partial t^2} \tag{4.10}$$

The solution of equations (4.9) and (4.10) leads to

$$v(x,t) = \underbrace{v_1(x-ut)}_{forward\ wave} + \underbrace{v_2(x+ut)}_{backward\ wave} \tag{4.11}$$

$$i(x,t) = \frac{1}{Z_0}\left[\underbrace{v_1(x-ut)}_{forward\ wave} - \underbrace{v_2(x+ut)}_{backward\ wave}\right] \tag{4.12}$$

where

$$Z_0 = \sqrt{\frac{L}{C}},\ \text{surge impedance,} \tag{4.13}$$

$$u = \frac{1}{\sqrt{LC}}, \text{ travelling wave velocity} \tag{4.14}$$

By observing these equations, the term $v_1(x - ut)$ moves along the line for distance x with velocity u and term $v_2(x + ut)$ also moves along the line but in the opposite direction. Thus, $v_1(x - ut)$ is the *'forward wave'* and $v_2(x + ut)$ is the *'backward wave'*.

Therefore, the voltage and current at point x and time t can be expressed as the summation (or composite) of forward and backward waves. A visual representation of voltages and current travelling waves through time is depicted in Figures 4.2 and 4.3 respectively. Note that forward and backward waves are conceptual quantities (both for voltage and current) and hence cannot be measured independently. This should not be confused with the actual measurable total voltage and current quantities.

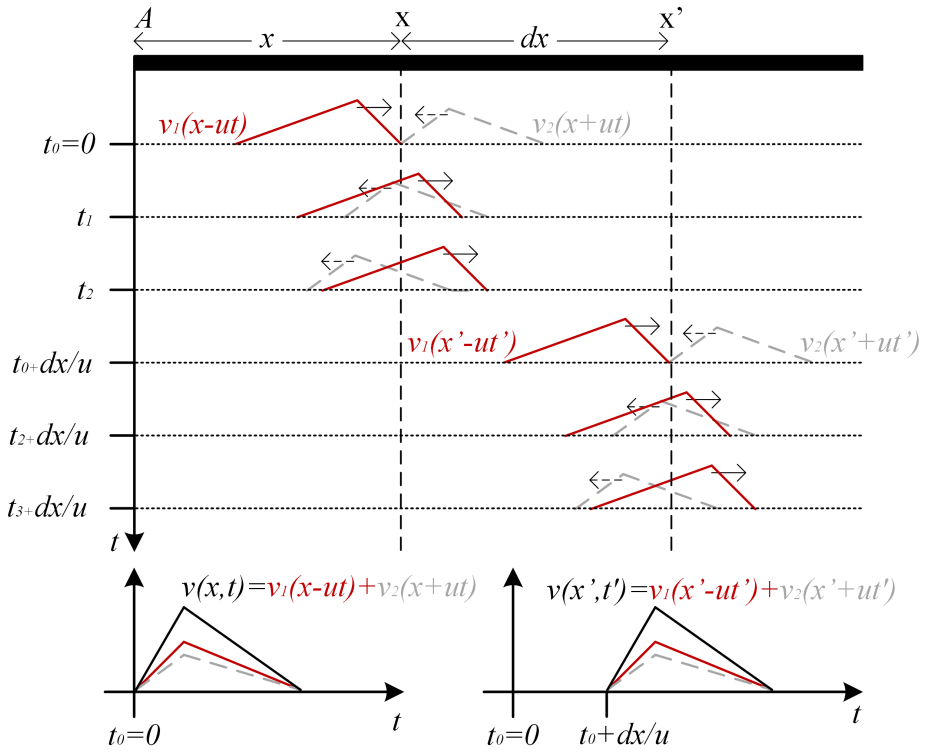


Figure 4.2: Voltage travelling waves representation on a transmission line.

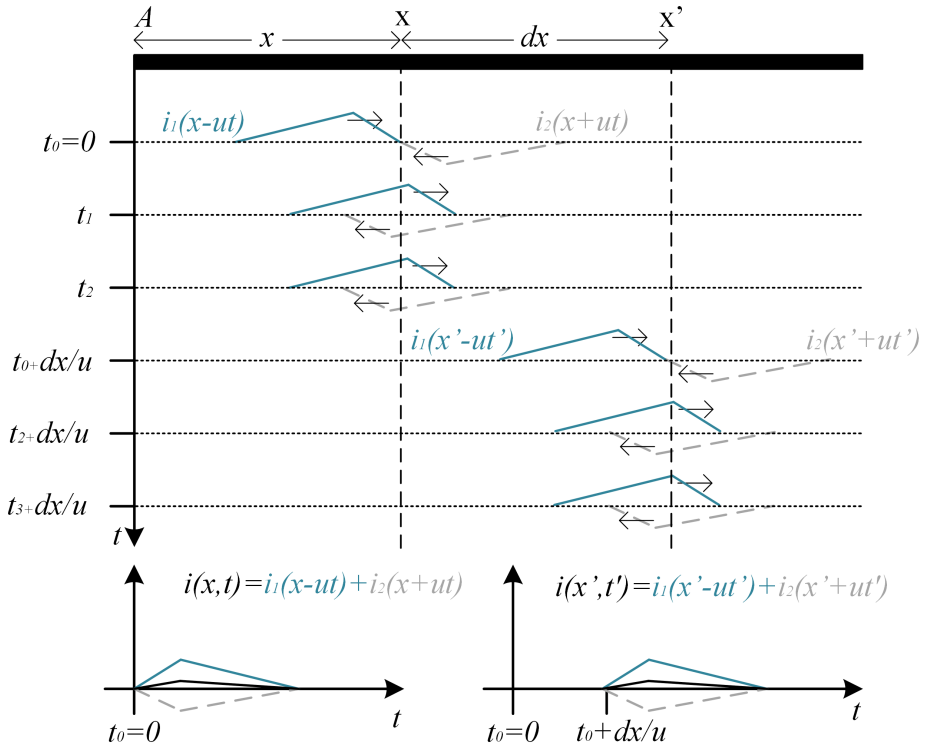


Figure 4.3: Current travelling waves representation on a transmission line.

4.1.2 Transition points

A transition point is a point on a line where the circuit constants change significantly, and hence there is a change in surge impedance and travelling wave velocity.

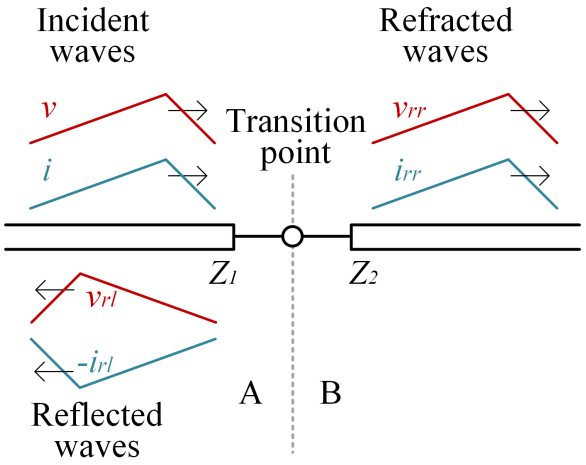


Figure 4.4: Behaviour of voltage and current travelling waves at a transition point.

When a travelling wave approaches a transition point, a part of it is reflected back and a part travels towards the rest of the network [155, 160]. As shown in Figure 4.4, the

initial wave is called *'incident wave'* and the remaining two at the transition point are called *'reflected wave'* and *'refracted wave'*. The behaviour of the aforementioned waves (both for current and voltage) at a transition point can be expressed by

$$\text{Incident waves: } v, i \rightarrow \frac{v}{i} = Z_1 \tag{4.15}$$

$$\text{Reflected waves: } v_{rl}, i_{rl} \rightarrow \frac{v_{rl}}{i_{rl}} = Z_1 \tag{4.16}$$

$$\text{Refracted waves: } v_{rr}, i_{rr} \rightarrow \frac{v_{rr}}{i_{rr}} = Z_2 \tag{4.17}$$

$$\text{Continuity of voltage waves: } v + v_{rl} = v_{rr} \tag{4.18}$$

$$\text{Continuity of current waves: } i - i_{rl} = i_{rr} \tag{4.19}$$

where:

$$Z_1 = \sqrt{\frac{L_1}{C_1}},\ Z_2 = \sqrt{\frac{L_2}{C_2}}$$

Therefore, by using equations (4.15) to (4.19), reflected waves ($v_{rl},\ i_{rl}$) and refracted waves ($v_{rr},\ i_{rr}$) can be expressed by equations (4.20) to (4.23), as a function of incident waves ($v,\ i$) and surge impedance Z_1 and Z_2:

$$v_{rl} = \frac{Z_2 - Z_1}{Z_2 + Z_1} v \tag{4.20}$$

$$v_{rr} = \frac{2Z_2}{Z_2 + Z_1} v \tag{4.21}$$

$$i_{rl} = \frac{Z_2 - Z_1}{Z_2 + Z_1} i \tag{4.22}$$

$$i_{rr} = \frac{2Z_1}{Z_2 + Z_1} i \tag{4.23}$$

Moreover, reflection and refraction factors (ρ and μ respectively) can be given by

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{4.24}$$

$$\mu = \frac{2Z_2}{Z_2 + Z_1} \tag{4.25}$$

Such factors are useful for analysing the behaviour of sequential travelling waves as it will demonstrated later.

For the validity of the above analysis for transitions points, it is mandatory to prove the continuity of power between sides A and B (Figure 4.4), to be established that $P_A = P_B$, where power of sides A and B are calculated by

$$P_A = (v + v_{rl})(i + i_{rl}) = \left(\frac{2Z_2}{Z_2 + Z_1}v\right)\left(\frac{2Z_1}{Z_2 + Z_1}i\right) \tag{4.26}$$

$$P_B = (v_{rr})(i_{rr}) = \left(\frac{2Z_2}{Z_2 + Z_1}v\right)\left(\frac{2Z_1}{Z_2 + Z_1}i\right) \tag{4.27}$$

$$\therefore P_A = P_B$$

Therefore, power equality is secured and the analysis carried out for a transition point can be considered as valid.

In Figure 4.5, a Bewley Lattice diagram [161] is shown integrating a network with four transition points. The reflection ($\rho,\ \rho'$) and refraction ($\mu,\ \mu'$) operators for each point are defined by

$$\rho_1 = (Z1 - Z_0)/(Z1 + Z_0),\ \mu_1 = 2Z1/(Z1 + Z_0) \tag{4.28}$$

$$\rho_1' = (Z0 - Z_1)/(Z0 + Z_1),\ \mu_1' = 2Z0/(Z0 + Z_1) \tag{4.29}$$

$$\rho_2 = (Z2 - Z_1)/(Z2 + Z_1),\ \mu_2 = 2Z2/(Z2 + Z_1) \tag{4.30}$$

$$\rho_2' = (Z1 - Z_2)/(Z1 + Z_2),\ \mu_2' = 2Z1/(Z1 + Z_2) \tag{4.31}$$

$$\rho_3 = (Z3 - Z_2)/(Z3 + Z_2),\ \mu_3 = 2Z3/(Z3 + Z_2) \tag{4.32}$$

$$\rho_3' = (Z2 - Z_2)/(Z2 + Z_3),\ \mu_3 = 2Z2/(Z2 + Z_3) \tag{4.33}$$

In this representation, the incident voltage travelling wave v arrives at transition point P_1 at $t = 0$. The refracted wave $v_{rr} = 1$ (waveform of step value 1), starts to propagate from left to right along line 1. Then the wave arrives at transition point P_2 with a valus of a ($a = 0 - 1\ \rightarrow$ attenuation ratio of line 1). Then, the wave a is decomposed into a

reflected wave, which travels back to line 1 with value $a\rho_2$, and refracted wave, which propagates towards line 2 with a value of $a\mu_2$. This routine (reflections and refractions) is repeated continuously, until the waves are diminished due to attenuation.

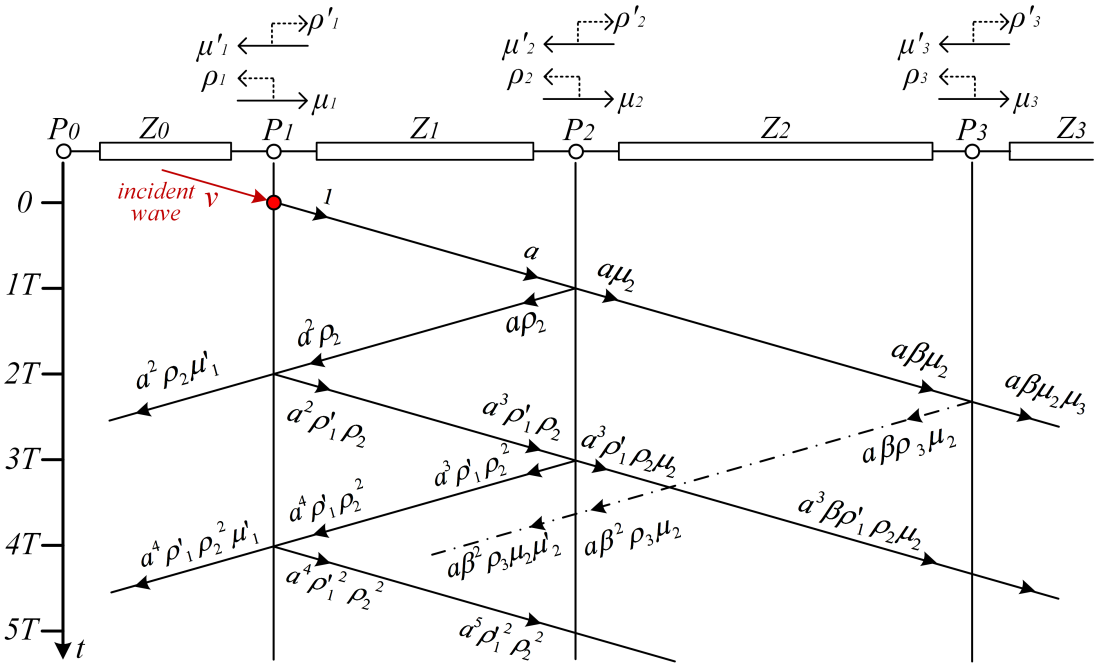


Figure 4.5: Lattice diagram integrating multiple transition points.

Consequently, the voltage at any point of the network can be written as the summation of reflected and refracted waves within time. Taking as example the voltage at points 1 and 2, the voltage expressions can be written as

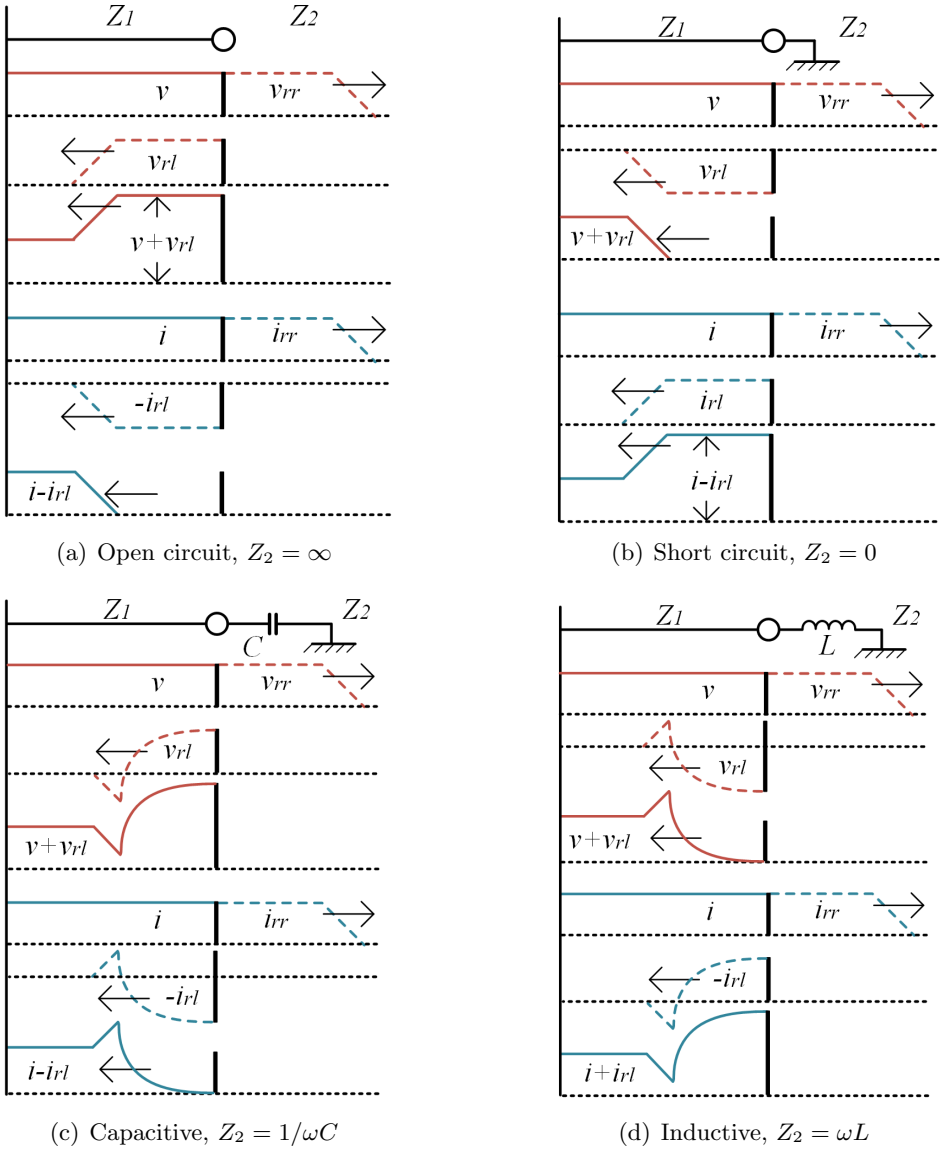
$$v_1(t) = \underbrace{1}_{(0-2)T} + \underbrace{(a^2\rho_2 + a^2\rho_1'\rho_2)}_{(2-4)T} + \underbrace{(a^4\rho_1'\rho_2^2 + a^4\rho_1'^2\rho_2^2)}_{(4-6)T} + \underbrace{(a^6\rho_1'^2\rho_2^3 + a^6\rho_1'^3\rho_1^3)}_{(6-8)T} + \ldots$$
$$\therefore\ v_1(t) \rightarrow \text{converging to: } \tfrac{1+a^2\rho_2}{1-a^2\rho_1'\rho_2} \tag{4.34}$$

$$v_2(t) = \underbrace{0}_{(0-1)T} + \underbrace{(a + a\rho_2)}_{(1-3)T} + \underbrace{(a^3\rho_1'\rho_2 + a^3\rho_1'\rho_2^2)}_{(3-5)T} + \underbrace{(a^5\rho_1'^2\rho_2^2 + a^5\rho_1'^2\rho_2^3)}_{(5-7)T} + \ldots$$
$$\therefore\ v_2(t) \rightarrow \text{converging to: } \tfrac{a(1+\rho_2)}{1-a^2\rho_1'\rho_2} = \tfrac{a\mu_2}{1-a^2\rho_1'\rho_2} \tag{4.35}$$

Note that at the above analysis, the converged values denote the final (i.e. steady state) values when $t \rightarrow \infty$.

4.1.3 Line termination

As discussed in the previous subsection, the point at which there is a change in the surge impedance is known as a transition point, and changes in the magnitude, polarity and shape of travelling waves (both voltage and current) can occur at these points. Usually in power systems, lines are terminated under specific conditions and with specific components (e.g. resistors, inductors). This is achieved either intentionally, or unintentionally due to system transients (e.g. line disconnection, faults, CB switching, etc.). Consequently, it is essential to identify a few typical and representative cases of line termination and its impact on travelling waves (both voltage and current).



(a) Open circuit, $Z_2 = \infty$

(b) Short circuit, $Z_2 = 0$

(c) Capacitive, $Z_2 = 1/\omega C$

(d) Inductive, $Z_2 = \omega L$

Figure 4.6: Travelling waves behaviour for different line terminations.

Typical configurations can be seen in Figure 4.6, namely open circuit, short circuit, capacitive and inductive [162]. The incident wave is propagating from Z_1 towards Z_2.

- **Open circuit** ($Z_2 = \infty$): When there is an open circuit at the end of a line (Figure 4.6(a)), both the refracted and reflected voltage waves are each equal to the incident wave ($v = v_{rr} = v_{rl}$). The resulting voltage is equal then to $v + v_{rl} = 2v$. Current waves behave differently; this is because the reflected wave changes polarity at the transition point. Consequently, total current becomes zero ($i - i_{rl} = 0$).

- **Short circuit** ($Z_2 = 0$): In the case of a short circuit at a line terminal (Figure 4.6(b)), voltage reflected wave changes polarity and the total voltage becomes zero ($v + v_{rl} = 0$). On the other hand, the reflected current wave is $i_{rl} = -i$ and hence the total current is doubled ($i + i_{rl} = 2i$).

- **Capacitive termination** ($Z_2 = 1/\omega C$): This configuration (Figure 4.6(c)) makes the system behave like a short circuit for voltage wave-front ($\because\ Cdv/dt \ggg 0$) and like an open circuit for wave-tail ($\because\ Cdv/dt = 0$). The resulting voltage and current waveforms can be deduced according to Figures 4.6(a) and 4.6(b).

- **Inductive termination** ($Z_2 = \omega L$): In this case(Figure 4.6(d)), the system behaves like an open circuit for current wave-front ($\because\ Ldi/dt \ggg 0$) and like a short circuit for wave-tail ($\because\ Ldi/dt = 0$). The resulting voltage and current waveforms can be deduced according to Figures 4.6(a) and 4.6(b).

4.2 Simulation Analysis of Transient Phenomena

In this section DC-side faults and their associated generated transient phenomena are analysed. For such an analysis, a five terminal HVDC grid (illustrated in Figure 4.7) has been developed from scratch. The system architecture has been adopted from the Twenties Project case study on DC grids [163]. There are five MMCs operating at $\pm 400\ kV$ (in symmetric monopole configuration), HbCBs and current limiting inductors at each transmission line end. Transmission lines have been modelled by adopting distributed parameter model. The parameters of the AC and DC network components are described in detail in Table 4.1.

The models of power converters utilised in these studies are based on 401-level Type 4 half bridge (HB) MMCs, which have been developed according to guidelines and

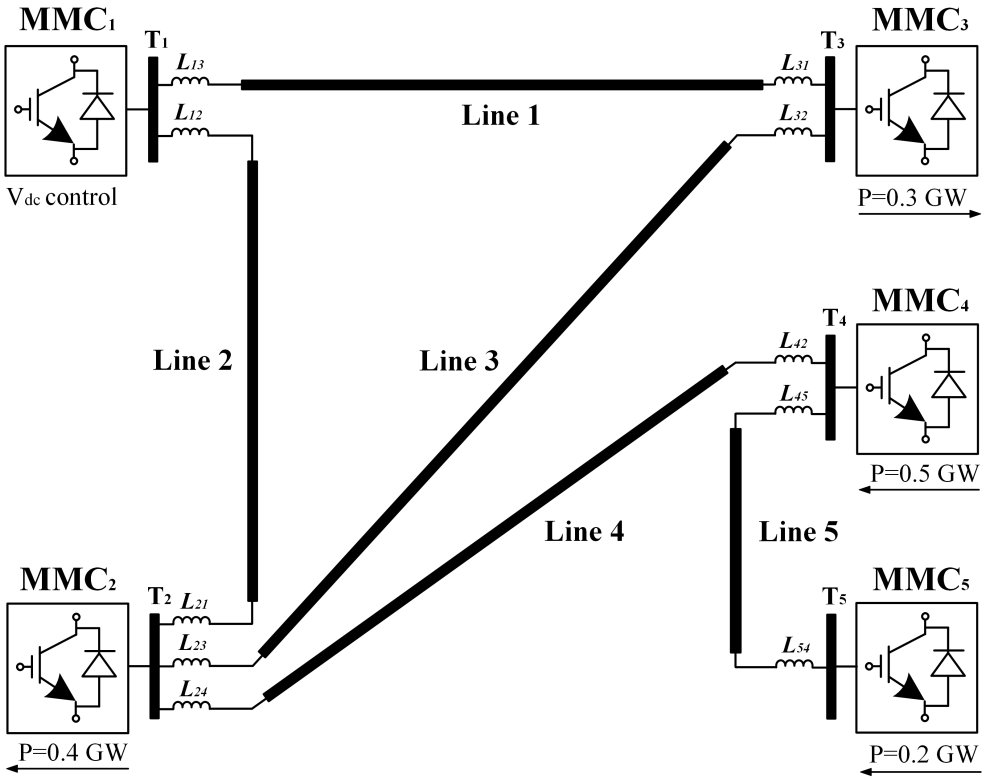


Figure 4.7: MTDC network model for simulation-based analysis of fault transients.

Table 4.1: MTDC network parameters.

Parameter	Value
DC voltage [kV]	± 400
DC inductor [mH]	150
Line resistance [Ω/km]	0.015
Line inductance [mH/km]	0.96
Line capacitance [μF/km]	0.012
Line lengths (1 to 5) [km]	180, 120, 500, 150, 100
AC frequency [Hz]	50
AC short circuit level [GVA]	40
AC voltage [kV]	400
MMC levels	401
MMC arm inductance [p.u.]	0.1
MMC equivalent arm capacitance [μF]	20.84

approaches described in Chapter 2.8. Such a representation has been validated against fully detailed models, and has been demonstrated to accurately represent the converter behaviour during steady-state, transient and fault conditions while remaining numerically stable and computationally efficient. Figure 4.8 illustrates the Type 4 equivalent for one phase. The converter response is achieved through controlled voltage and current sources. A fault controller is also included which bypasses the sub-modules when the maximum

current of the IGBTs is exceeded. In this case, the converter behaves like an uncontrolled rectifier. Due to unbalanced voltage conditions, circulating currents are generated inside each MMC which increase current stress, introduce current distortion (arm currents), and produce additional conduction losses. To eliminate such currents, a proportional resonant, circulating current suppression controller (PR-CCSC), as described in [164], has been integrated into the control system.

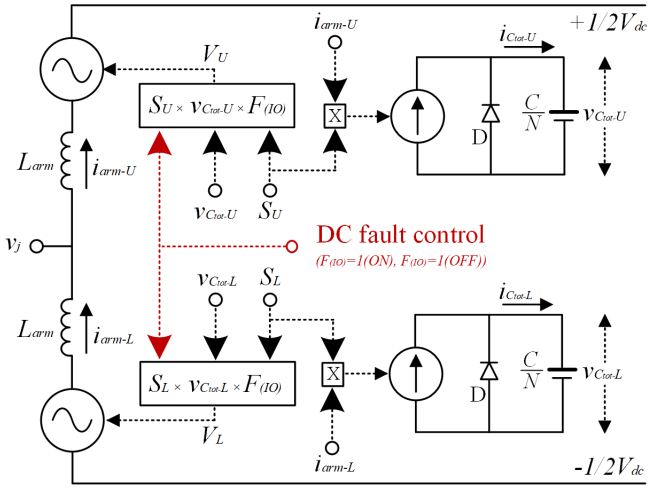


Figure 4.8: Equivalent of the MMC Type 4 Model.

4.2.1 Sequence of events of DC-side faults

The time course of DC currents and voltages after the occurrence of a DC-side fault can be characterised by a series of fast phenomena. These are analysed, taking as an example the fault case illustrated in Figure 4.9 where a fault occurring at Line 1 (70 km from T_1).

In Figure 4.10, DC current and voltages are shown for the prospective (i.e. no tripping of CBs) and interrupted case. The DC current corresponds to the current measurement at Line 1 (at T_1 side) while the voltage is also measured at terminal T_1.

When there is no tripping initiated, it can be shown that the prospective fault current reaches high values (Figure 4.10(a)) due to the infeed from the converters directly-connected to the faulted line (i.e. MMC_1 and MMC_3), but also from the neighbouring lines and converters. In this case the corresponding voltage (Figure 4.10(b)) will collapse towards zero without any restoration. In the case of the interruption, the CBs corresponding to the faulted line (i.e. CB_{13} and CB_{31}) are tripped. After a few milliseconds the current will fall gradually to zero. The voltage response at this case is much better. In fact, within the time that fault current starts decreasing, there is a voltage restoration

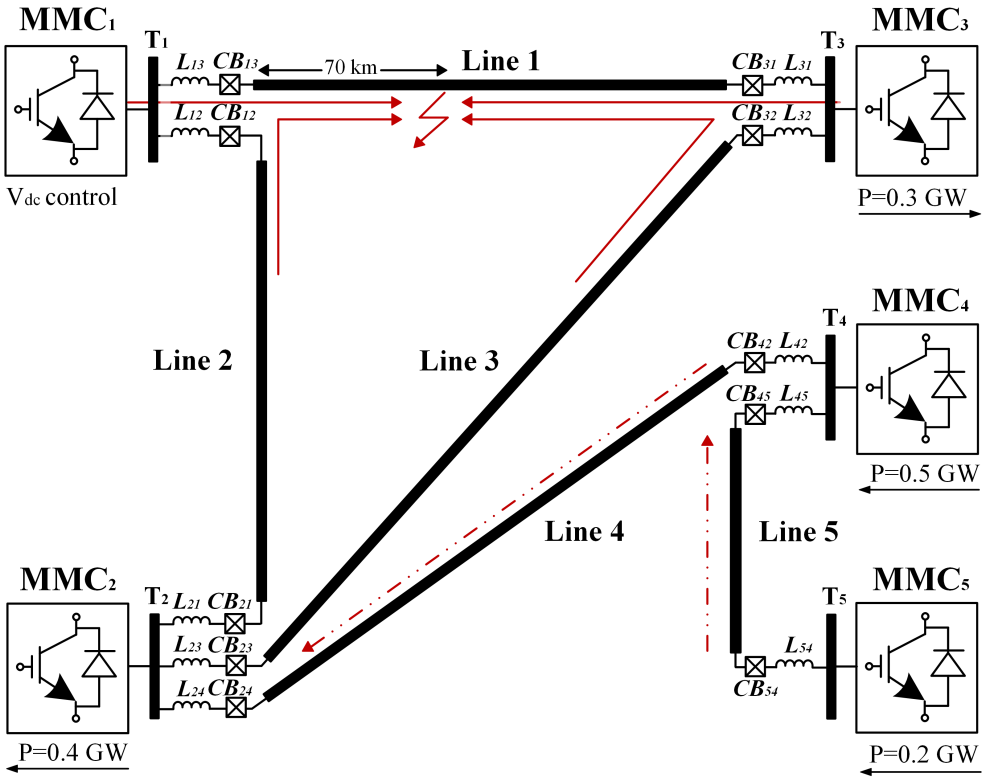
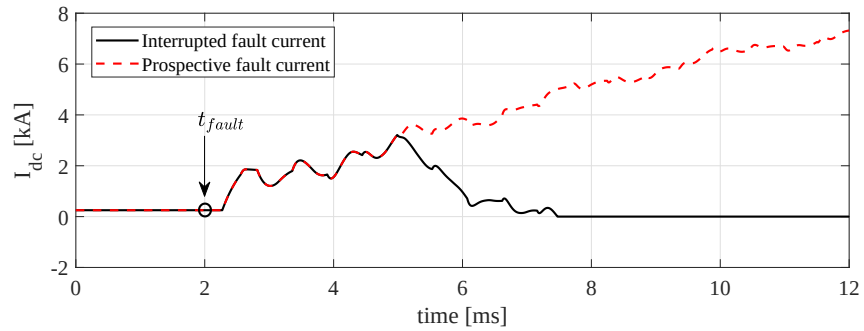
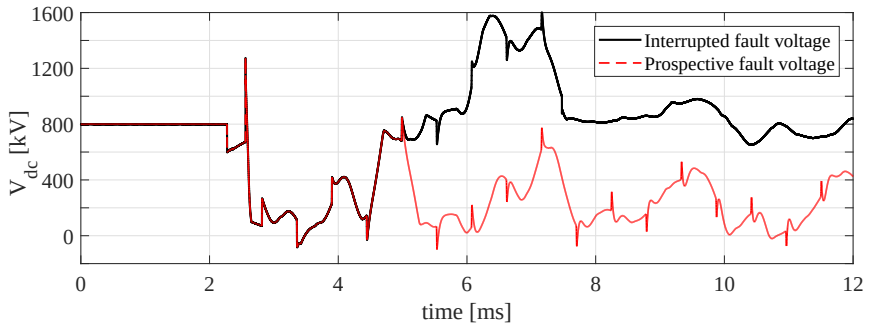


Figure 4.9: Five terminal MTDC network with fault occurring at Line 1.



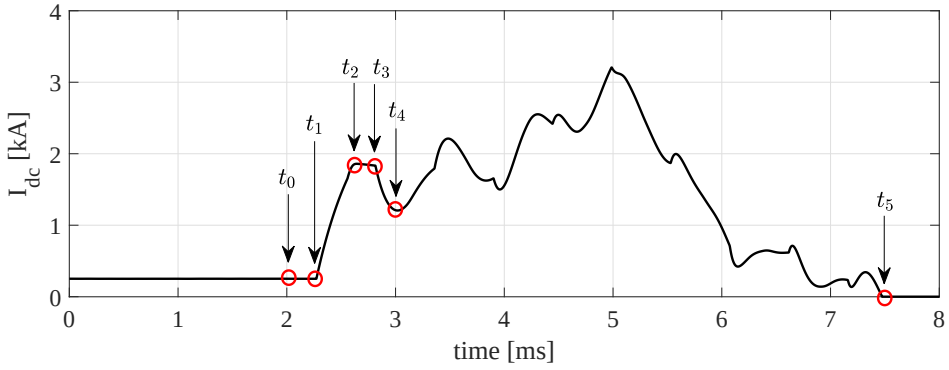
(a) DC current



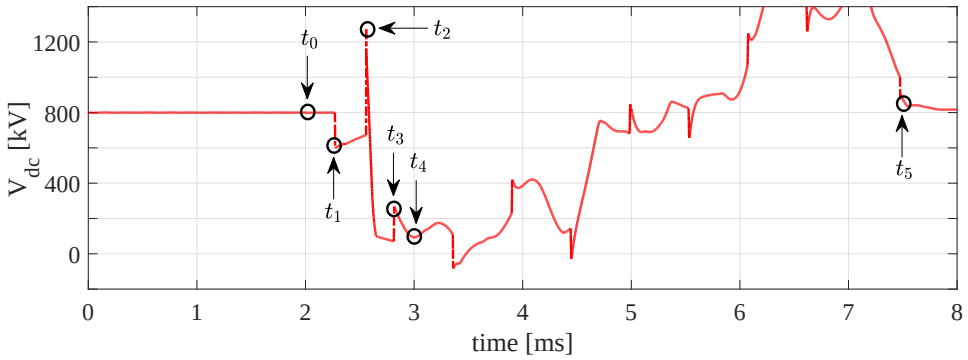
(b) Current interrutpion in HbCB

Figure 4.10: Prospective and interrupted time course of DC current and voltage after DC-side fault.

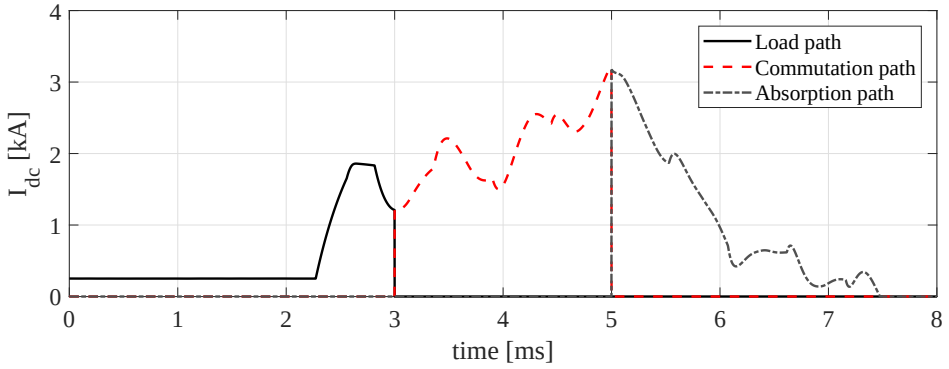
taking place. However, there is an over-voltage observed due to the opening of CB (as discussed in Chapter 2.5) which is then vanished after the fault current is completely cleared (i.e. $I_{dc} = 0$). Further and faster voltage stability could be achieved with enhanced control loops of the converters (or other voltage support equipments). The operation of CBs indicate not only their significance as protective equipment and their contribution so voltage stability, but also the fact that their operation takes significant time (considering the fast nature of DC-side faults) and shall be included in the time course analysis of DC-side faults.



(a) DC current



(b) DC voltage)



(c) Current interrutpion in HbCB

Figure 4.11: Time course of DC-side faults.

In Figure 4.11 the time course of DC-side faults is shown for DC voltage and current. The analysis is taking place from fault inception until fault clearance. The stages are analysed as below:

- t_0 : Fault is triggered at the line. Voltage and current waves are generated, which start propagating towards the transmission line terminals.
- t_1 : Voltage and current travelling waves reach terminal T_1. Part of the waves is reflected back to the fault point and part is refracted to the rest of the network. The total equivalent capacitance of the converter will start discharging and there is a current rise starting.
- t_2 : The valves of the converter are blocked for self-protection. At this stage, the fault current is fed from the AC side and partially from other neighbouring elements.
- t_3 : Another set of voltage and current travelling wave reach terminal T_1.
- t_4 : CB receives a tripping signal and the tripping sequence of the breaker is initiated.
- t_5 : Fault is cleared.

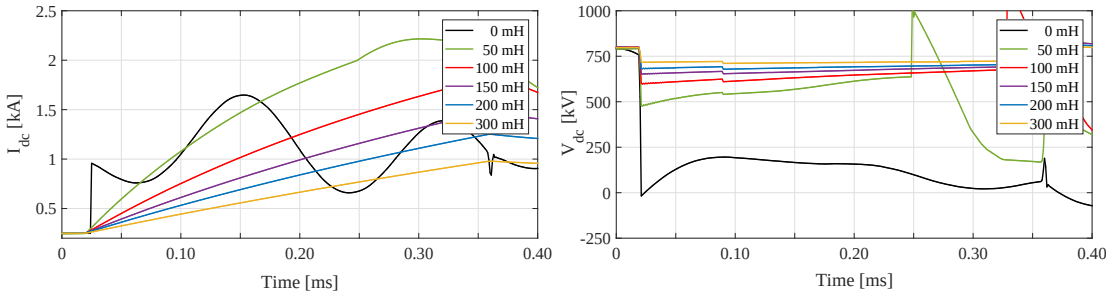
It should be noted that the sequence or time duration of the aforementioned events could be changed according to the breaker technology, protection algorithm of the relays, fault distance and converter blocking operational point. However, all of the involved phenomena will be present both in voltages and currents.

4.2.2 Impact of inductive line termination

In this section the impact of current limiting inductors on the fault signatures is investigated. The analysis has been extended to include the impact of such inductors on fast transient phenomena known as travelling waves. Specifically, DC-side inductors can form a significant reflection boundary for the generated travelling waves.

The deliberate inclusion of additional inductance not only limits the rate of change of DC current, but also the resulting DC voltage signatures (and the fact that they may be different depending on fault location and known values of inserted inductance at line terminals) can help to achieve a deeper insight to the fault nature.

The fault scenario depicted previously in Figure 4.9 has been repeated for different values of L at line terminals. The resulting DC current and voltage signatures are



(a) DC current (b) DC voltage

Figure 4.12: Impact of inductive termination to DC current and voltage during DC-side faults.

illustrated in Figure 4.12. It should be noted that those measurements are captured at the beginning of Line 1 (at the converter-side of the inductor).

By observing 4.12(a) it can be seen that higher values of inductance L will increase the rise time of DC fault current. This will have an impact on the time response of the converter blocking point, as the maximum operating current of valves will be delayed. Higher values of inductance will also result in lower voltage drop while they will filter the magnitude of the incoming travelling waves.

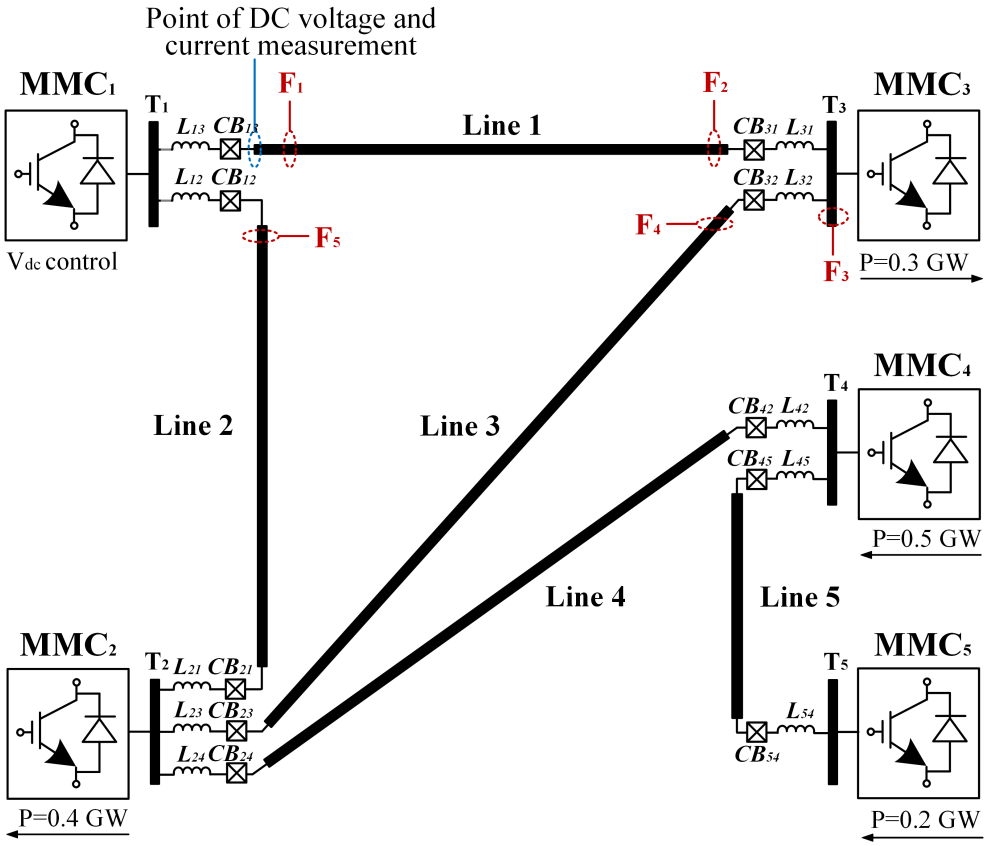


Figure 4.13: Fault scenario points on five-terminal MTDC network.

In order to further investigate the impact of inductive line termination on transient phenomena, studies on five different fault scenarios have been carried out. Those are depicted in Figure 4.13 and explained in Table 4.2. It should be noted that for those cases, the voltage and current measurements have been captured at the line side of L_{13}. In this convention, fault F_1 is considered close-up internal, F_2 is considered remote internal, F_3 is a busbar fault (external), F_4 is a forward external fault and F_5 is a reverse external fault. For those scenarios the inductance L has been set to $L = 100\ mH$ while CB operation have been suspended in order to capture the natural response of the faults. Further discussion on the inductor sizing will be reported in the next chapter.

Table 4.2: Descritpiton of fault scenarios.

Scenario	**Description**
F_1	Close-up internal fault at Line 1 (15 km from T_1)
F_2	Remote internal fault at Line 1 (179 km from T_1)
F_3	Busbar external fault at Busbar 3
F_4	Forward external fault at Line 3 (5 km from T_3)
F_5	Reverse external fault at Line 2 (5 km from T_1)

For the analysis of the fault scenarios presented in Table 4.2, it is of major importance to define the equivalent inductance L from point of measurement (i.e. line side of L_{13}) to the actual fault. Those have been calculated and included in Table 4.3.

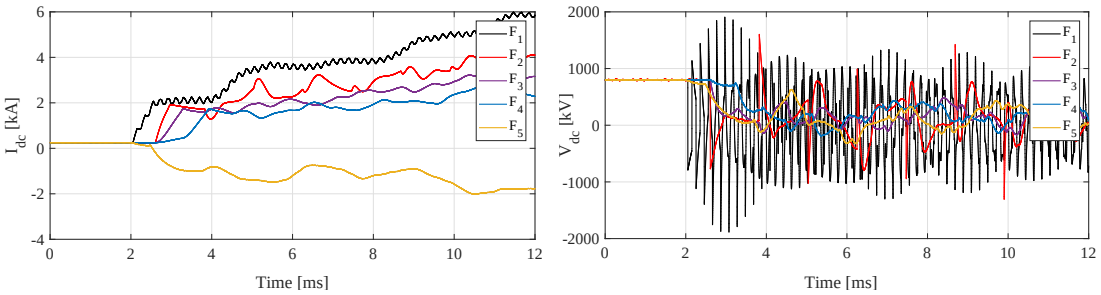
Table 4.3: Equivalent L from point of measurement to the fault (corresponding to scenarios F_1 to F_5 - Table 4.2).

Fault scenario	**Fault path impedance**	
	L	**Value [mH]**
F_1	$L_{L1} \cdot d_{L1}$	14.4
F_2	$L_{L1} \cdot d_{L1}$	171.84
F_3	$(L_{L1} \cdot l_{L1}) + L_{31}$	272.8
F_4	$(L_{L1} \cdot l_{L1}) + L_{31} + L_{32} + (L_{L3} \cdot d_{L3})$	377.6
F_5	$L_{13} + L_{12} + (L_{L2} \cdot d_{L2})$	204.8

where $L_{L1},\ L_{L2},\ L_{L3}$ is the inductance per kilometre of lines 1 to 3 respectively, $l_{L1},\ l_{L2},\ l_{L3}$ is the total length of lines 1 to 3 respectively and $d_{L1},\ d_{L2},\ d_{L3}$ is the distance to fault for faulted lines 1 to 3 respectively

Figure 4.14(a) illustrates the current feed into Line 1 for faults scenarios F_1 to F_5. As expected, after the fault trigger at $t_{fault} = 2.0\ ms$ high currents flow through Line 1. Even though travelling waves (and their associated propagation delays corresponding to fault location) are present in current measurements, there are not so much distinctive

features for fault discrimination. The only apparent feature is concerned with fault F_5 where power and hence current reversal is observed.



(a) DC current (b) DC Voltage

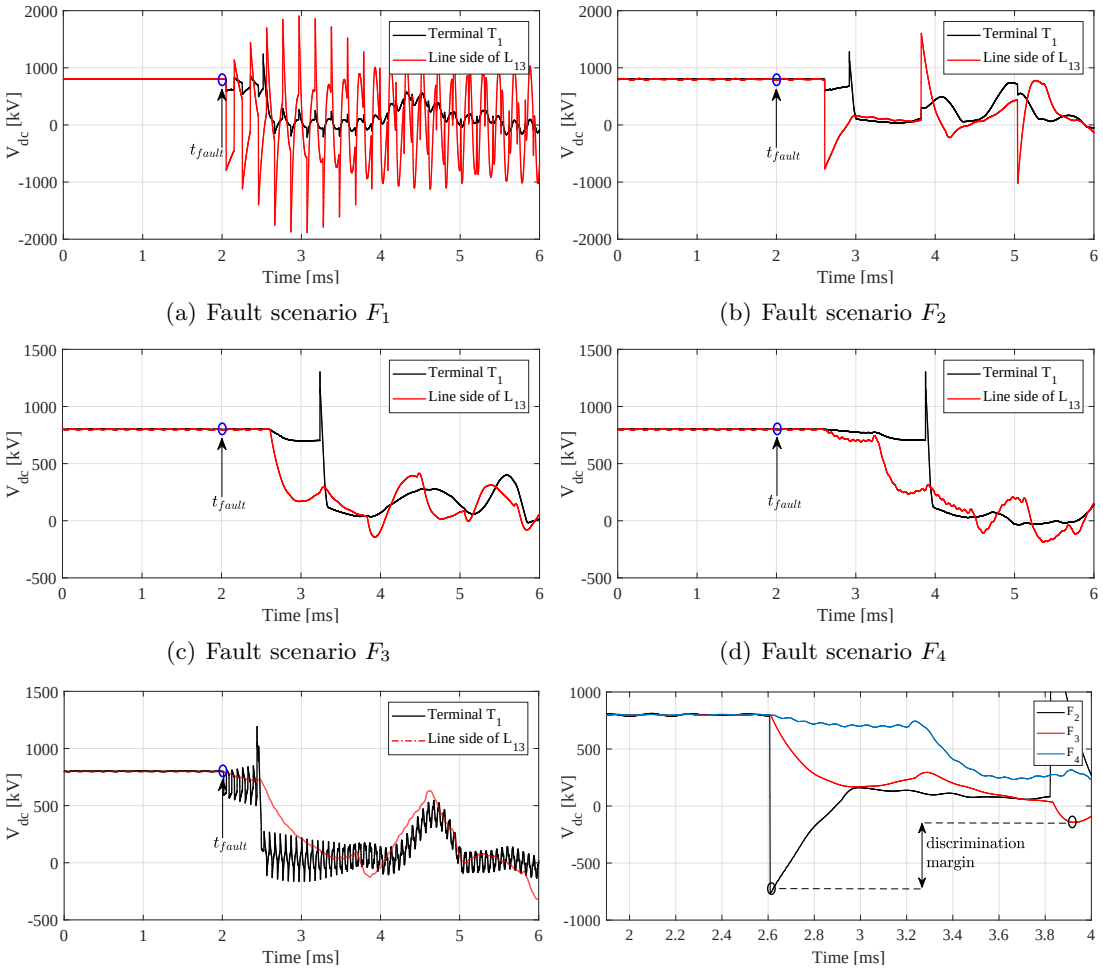
Figure 4.14: DC voltage and current response corresponding to fault scenarios described in Table 4.2.

For this reason, the nature of the faults is better investigated with the utilisation of voltage measurements. For each case fault scenario, the voltage response is depicted in Figure 4.15. Additionally, the voltage of measurement at terminal T_1 is also included to better demonstrate the significance of current limiting inductors.

In all cases there is a significant difference between the two captured voltage waveforms for internal faults F_1 and F_2 (Figure 4.15(a) and Figure 4.15(b) respectively). These which appear to have distinctive sharp edges which are more pronounced on the line side of inductor L_{13} (as the measuring point is closer to the fault and does not have any lumped reactor in-between). As for external faults F_3, F_4 and F_5, the voltage response is more gradual and there are no sharp edges on the voltage waveforms. This is expected since for any external fault, the equivalent inductance included in the fault current path is always significantly larger than for the internal fault due to the installed lumped reactors (see Table 4.3).

A challenge for those five fault scenarios would be the discrimination between F_2, F_3 and F_4 as they are practically in the same location separated by different values of lumped inductors. Such discrimination would be very useful in the context of protection.

By observing the expanded view area depicted in Figure 4.15(f) for faults F_2, F_3 and F_4, it can be seen that for the remote internal fault (i.e. F_2) the magnitude of the first voltage travelling wave reaches the lower values approximately $-700\ kV$. However, for any external fault (i.e. F_3 and F_4) the lowest are higher than $-170\ kV$. This gives a relatively wide margin to achieve reliable discrimination based on under-voltage criteria. The same logic could be applied by adopting rate of change of DC voltage, but challenges



(a) Fault scenario F_1

(b) Fault scenario F_2

(c) Fault scenario F_3

(d) Fault scenario F_4

(e) Fault scenario F_5

(f) Fault scenario F_5

Figure 4.15: Voltage response (measured both at Terminal T_1 and line side of L_{13}) to fault scenarios described in Table 4.2.

related to noise are expected. Even though the level of DC voltage can assist towards the discrimination of faulted feeders, there is a significant challenge related to fault resistance R_f. Specifically, highly-resistive fault can impose smaller voltage drop and hence it would be difficult to set voltage thresholds. As such, Wavelet Transform is a possible solution to mitigate these challenges.

4.3 Signal Processing Techniques

The generated voltages and currents after the fault contain abundant information such as time of fault occurrence, fault location, fault direction, faulted feeder and so on. Such information may vary significantly with regards to different operating and fault conditions. Consequently, it is of major importance to analyse the fault transients signals in order

to extract the desired features for the corresponding application (e.g. protection, fault location, etc.).

4.3.1 Fourier transform

The analysis of a signal in the time and frequency domains is one of the basic characteristics for describing a signal. The observation of a signal in the time domain is easily carried out as it is in its natural form. However, analysis in the frequency domain requires the signal to be transformed. The most common transform of a signal $v(t)$ from time domain to frequency domain is the Fourier transform. The Fourier transform of a signal, $v(t)$ is given by

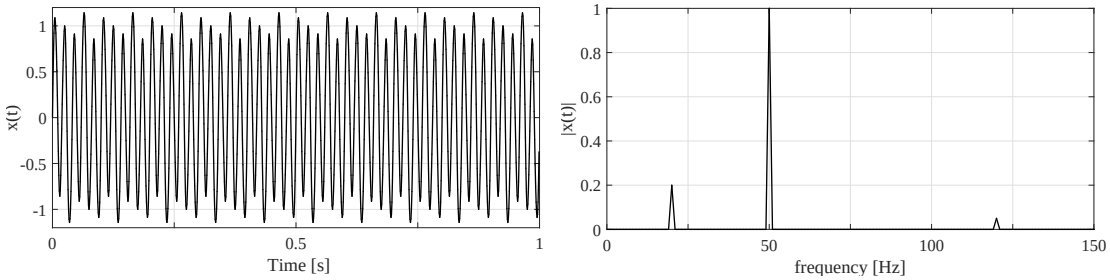
$$V(j\omega) = \int_{\Re} v(t)e^{-j\omega t}dt \tag{4.36}$$

For the application of Continuous Fourier Transform (CFT) to real engineering applications, equation (4.36) should be discretised, yielding the Discrete Fourier Transform (DFT). The DFT is the equivalent of the continuous transform (equation (4.36)) for signals with N points (i.e. finite points of data) separated by sampling time T, thus

$$V(j\omega) = \int_0^T v(t)e^{-j\omega t}dt \simeq \sum_{t=0}^{N} e^{-j\omega t}v(t)\Delta dt \tag{4.37}$$

where $\Delta t = \frac{T}{N}$

Even though both CFT and DFT have been applied to signal processing, especially time–frequency analysis, the Fourier integral cannot be localised simultaneously in the time and frequency plane. In fact, Fourier transform has the ability of local analysis in the frequency domain rather than time domain. The waveform in Figure 4.16(a) represents the signal $v(t) = \frac{1}{5}sin(2\pi 20t) + sin(2\pi 50t) + \frac{1}{20}sin(2\pi 120t)$.



(a) Time domain (b) Freqeuncy domain

Figure 4.16: Diagram of short Fourier transform.

The Fourier transform of signal $v(t)$ is depicted in Figure 4.16(b); as it can be seen, the amplitudes of the signal at specific frequency components are shown accurately. However, it is evident that the time indices which those signals have occurred are unknown. In an attempt to overcome this barrier, Short-time Fourier transform (STFT) is introduced. The main idea of STFT is the division of the signal of interest into many time intervals and each one is then analysed for frequency extraction. STFT has partially solved the problem of standard Fourier transform. However, STFT depends in a fixed time window whose characteristics (i.e. function, form and shape which determine the resolution cannot change within time). Consequently, for the analysis of non-stationary signals STFT cannot still meet the requirements of simultaneous time-frequency analysis.

4.3.2 Wavelet transform

Transient signals in power system are typical stationary signals. In previous subsection it has been demonstrated that in traditional signal processing, Fourier transform builds up the connection between the frequency domain and time domain of a signal. However, for nonstationary signals, Fourier transform has numerous deficiencies, such as lack of time orientation function, fixed resolution, and so on, which limits its application for analysis of transient signals in power systems. For this reason, there is a need for algorithms to improve traditional Fourier transform, which will provide a higher time resolution.

Wavelet Transform theory has been developed in the later 1950s and early 1990s as a tool for signal analysis simultaneously in time-frequency domain [165] . Even though other methods have been proposed (e.g. Gabor [166, 167], Wigner [168], Cohen [169, 170], etc.), Wavelet Transform has been recognised as the most powerful.

The localisation in both time–frequency domain is a unique feature of Wavelet transform. By utilising Wavelet Transform in power systems (especially for analysis of transients), several technical foundations may be established which can assist for the enhancement of several applications as those listed below:

- Power systems protection [171, 172].
- Fault location [173–176].
- Signal denoising [177–179].
- Power quality analysis [180–182].
- Data compression [183–185].

4.3.2.1 Definition of mother wavelet

The wavelet transform of a function $v(t)$ can be expressed as the integral of the product of $v(t)$ and the daughter wavelet $\Psi^*_{a,b}(t)$ as

$$WT_{\psi(\alpha,b)}v(t) = \int_{-\infty}^{+\infty} v(t) \quad \underbrace{\frac{1}{\sqrt{\alpha}}\Psi\left(\frac{t-b}{a}\right)}_{\text{daughter wavelet } \Psi^*_{a,b}(t)} \quad dt \tag{4.38}$$

The daughter wavelet $\Psi^*_{a,b}(t)$ is a scaled and shifted version of the mother wavelet $\Psi_{a,b}(t)$. Scaling is implemented by α which is the binary dilation (also known as scaling factor) and shifted by b, which is the binary position (also known as shifting or translation). If the function $v(t)$ and mother wavelet $\Psi_{a,b}(t)$ are real functions then the resulting $WT_{\psi(\alpha,b)}v(t)$ is also a real function. In any other case, the mother wavelet $\Psi_{a,b}(t)$ and the resulting $WT_{\psi(\alpha,b)}v(t)$ are complex functions.

4.3.2.2 Frequency and time spectrum of Wavelet transform

In Wavelet transform, the scale parameter, α, plays the role of compressing or stretching the mother wavelet. Specifically, higher values of α correspond to the low-frequency spectrum of a signal, whereas a fairly small α corresponds to the high-frequency analysis of a signal. This is also illustrated graphically in Figure 4.18 where the time frequency plane of wavelet transform is illustrated with respect to scaling factor α. The shifting parameter, b, determines the central position of time, or the time domain centre of the analysis of $v(t)$. Therefore, the entire time-frequency scope of a mother wavelet is adjusted by the manipulation of α and b.

Taking into account that $V(\omega)$ and $\Psi(\omega)$ are the Fourier transforms of $v(t)$ and $\psi(t)$ respectively, the Fourier transform of $\Psi_{a,b}(t)$ can be expressed by

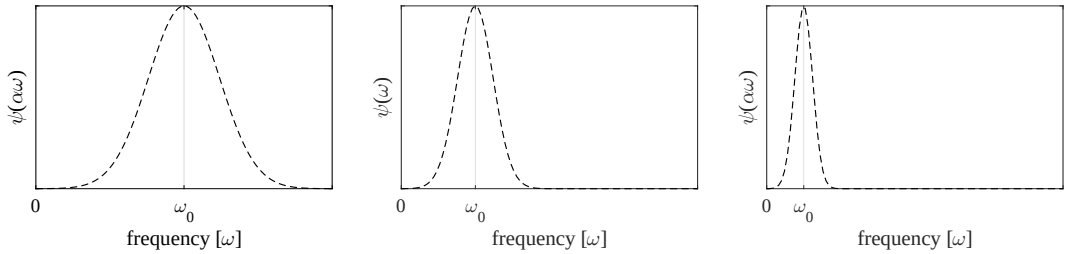
$$\Psi_{a,b}(\omega) = \sqrt{\alpha}\Psi(\alpha\omega)e^{-j\omega b} \tag{4.39}$$

Combining equations (4.38) and (4.39) and applying Parseval's theorem [186–188] for uniformly placed values of a signal, the wavelet transform in the frequency domain can be expressed as

$$WT_{\psi(\alpha,b)}v(t) = \frac{1}{2\pi}\left[V(\omega), \Psi_{(\alpha b)}(\alpha\omega)\right] = \frac{\sqrt{\alpha}}{2\pi}\int_{-\infty}^{+\infty} V(\omega)\Psi^*(\alpha\omega)e^{j\omega b}d\omega \tag{4.40}$$

Considering that a function $\psi(t)$ has time width and central point set to Δt and t_0 respectively, the corresponding frequency width and central point will be $\Delta\omega$ and ω_0 respectively. By scaling the signal $\psi(t)$ by α (i.e. $\psi(\frac{t}{\alpha})$), the time domain central point will still be t_0, while the width will change to $\alpha\Delta t$. Consequently, the corresponding frequency width and central point will be $\Delta\omega/\alpha$ and ω_0/α respectively.

Figure 4.17, illustrates the impact of scaling factor α to $\psi(\omega)$. When α decreases (Figure 4.17(a)), the time domain decreases as well; however, the frequency band $\Delta\omega$ widens, and the central frequency shifts to higher value. On the contrary, when α increases (Figure 4.17(c)), the time domain increases as well; however, the frequency band $\Delta\omega$ narrows, and the central frequency shifts to smaller value. Considering these observations, the relation between the bandwidth, time domain width, time centre and the central frequency of Wavelet transform can be presented graphically in the time-frequency (see Figure 4.18).



(a) $\alpha = 0.5$ (b) $\alpha = 1.0$ (c) $\alpha = 2.0$

Figure 4.17: Demonstration of $\psi(\omega)$ with respect to changes in scaling factor α.

It is interesting to point out here that the product of $\Delta\omega$ and Δt is constant (i.e. cannot change for changes in scaling factor, α); hence, Wavelet transform is still subjected to the uncertainty principle. Moreover, by this observation the quality factor (Q_F) can be introduced as

$$Q_F = \frac{\Delta\omega}{\omega_0} = \frac{bandwidth}{centrefrequency} \tag{4.41}$$

Quality factor Q_F remains constant for changes in scaling factor α. This is the reason that the domains shown in Figure 4.18 are characterised by equal surfaces and proves the adjustable time window capability of wavelet transform.

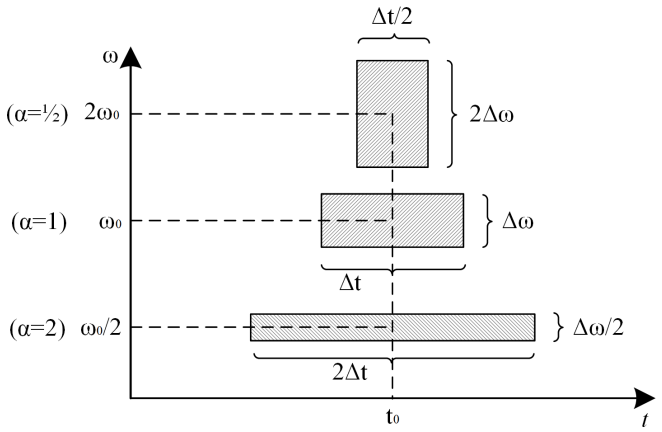


Figure 4.18: Impact of scaling factor α on time-frequency domains of Wavelet transform.

4.3.2.3 Continuous and discrete analysis

Wavelet transform can be distinguished in two categories: Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT). The difference lies upon the resolution of binary dilation α and binary position b. In DWT they move discretely in dyadic blocks. Specifically, α and b can only take values of the power of two, as expressed by

$$\alpha_j = 2^j, \ (\alpha_0 = 2^0 = 1, \alpha_1 = 2^1 = 2, ...) \tag{4.42}$$

$$b_j = 2^j N, \ (b_0 = 2^j 0 = 0, b_1 = 2^j 1 = 2^j, ...) \tag{4.43}$$

where j is the level of decomposition and N is the sample index.

Consequently, the CWT described in equation (4.38) results in the following discrete form

$$WT_{\psi(2^j,b)}v(t) = \int_{-\infty}^{+\infty} v(t)\frac{1}{\sqrt{2^j}}\Psi\left(\frac{t-2^jN}{2^j}\right)dt \tag{4.44}$$

The selection between CWT and DWT is a trade-off between time accuracy of the wave detection, and processing resources and their associated time delays [189]. In the case of CWT, the daughter wavelet can be positioned smoothly over the signal; hence, the accuracy of the wave time detection is better than for DWT techniques. This is the reason that CWT is preferred for fault location applications [190], where the computational time is not crucial. However, DWT is computationally more efficient [189], which enables faster wave detection. As a result, DWT is considered more suitable for power system protection applications [191].

4.3.2.4 Multi-resolution analysis

When DWT is applied to a discrete signal $v(n)$, the signal can be decomposed into high-frequency detailed coefficients and low-frequency approximation coefficients, which are given by

$$W_{2^j} v(n) = \sum_k g_k A_{2^{j-1}} v(n - 2^{j-1}k) \tag{4.45}$$

$$A_{2^j} v(n) = \sum_k h_k A_{2^{j-1}} v(n - 2^{j-1}k) \tag{4.46}$$

where g_k is the high-pass filter coefficients, h_k is the low-pass filter coefficients and A_{2^0} is the initial signal.

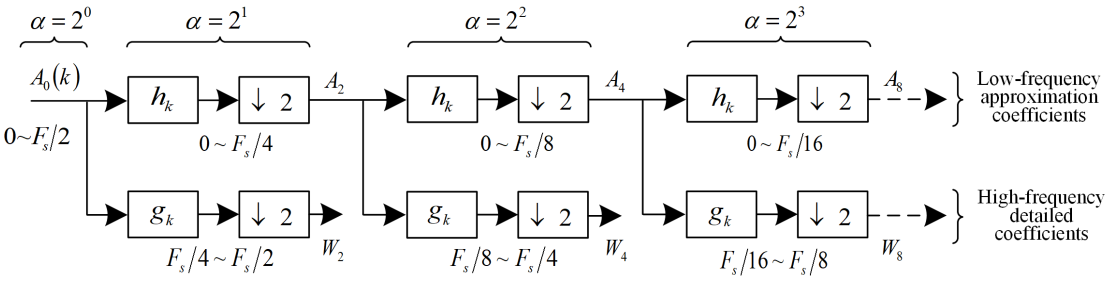


Figure 4.19: Decomposition structure for multi-resolution analysis based on filter banks.

Taking into account that signal $v(n)$ has a sampling frequency F_s, it contains components in the frequency spectrum $0 \sim F_s/2$ as per Nyquist theorem. As show in Figure 4.19, DWT decomposes the signal into different frequency bands and *'multi-resolution'* analysis [165] is achieved. The frequency bandwidths of high-frequency detailed and low-frequency approximation coefficients for each decomposition level are given by

$$f_{band-high} = \frac{F_s}{2 \cdot 2^j} \sim \frac{F_s}{2 \cdot 2^{j-1}} \tag{4.47}$$

$$f_{band-low} = 0 \sim \frac{F_s}{2 \cdot 2^j} \tag{4.48}$$

It is therefore evident that according to the frequency band of interest, the corresponding scaling factor may be selected. The multi-resolution decomposition analysis depicted in Figure 4.19 can be implemented in a bi-directional manner. This means that a signal can be decomposed to a desired number of levels and then re-constructed using only the coefficients of interest.

4.4 Application of Wavelet Transform to HVDC Fault Analysis and Detection of Travelling Waves

In this subsection, the presented analysis aims to provide an insight to the nature of DC-side faults and illustrate the basic benefits of Wavelet transform. For this purpose, the network depicted in Figure 4.20 (corresponding details are presented in Table 4.4) has been utilised. A pole-to-pole fault occurring at 150 km on a 300 km transmission line has been selected as test case to perform Wavelet transform on DC voltage and current measurements captured on the line-side of inductor L_{12} at terminal T_1. In order to capture all the transient phenomena and better illustrate the performance of Wavelet transform, the simulation and the measurement recordings have been implemented by utilising a sampling frequency of 2 MHz. The presented Wavelet-based analysis takes into account the impact of mother wavelet, scaling factor and the presence of noise in captured signals.

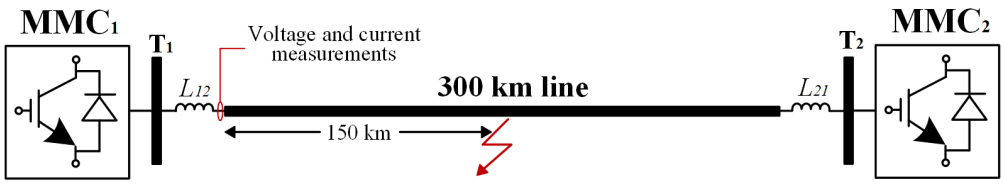


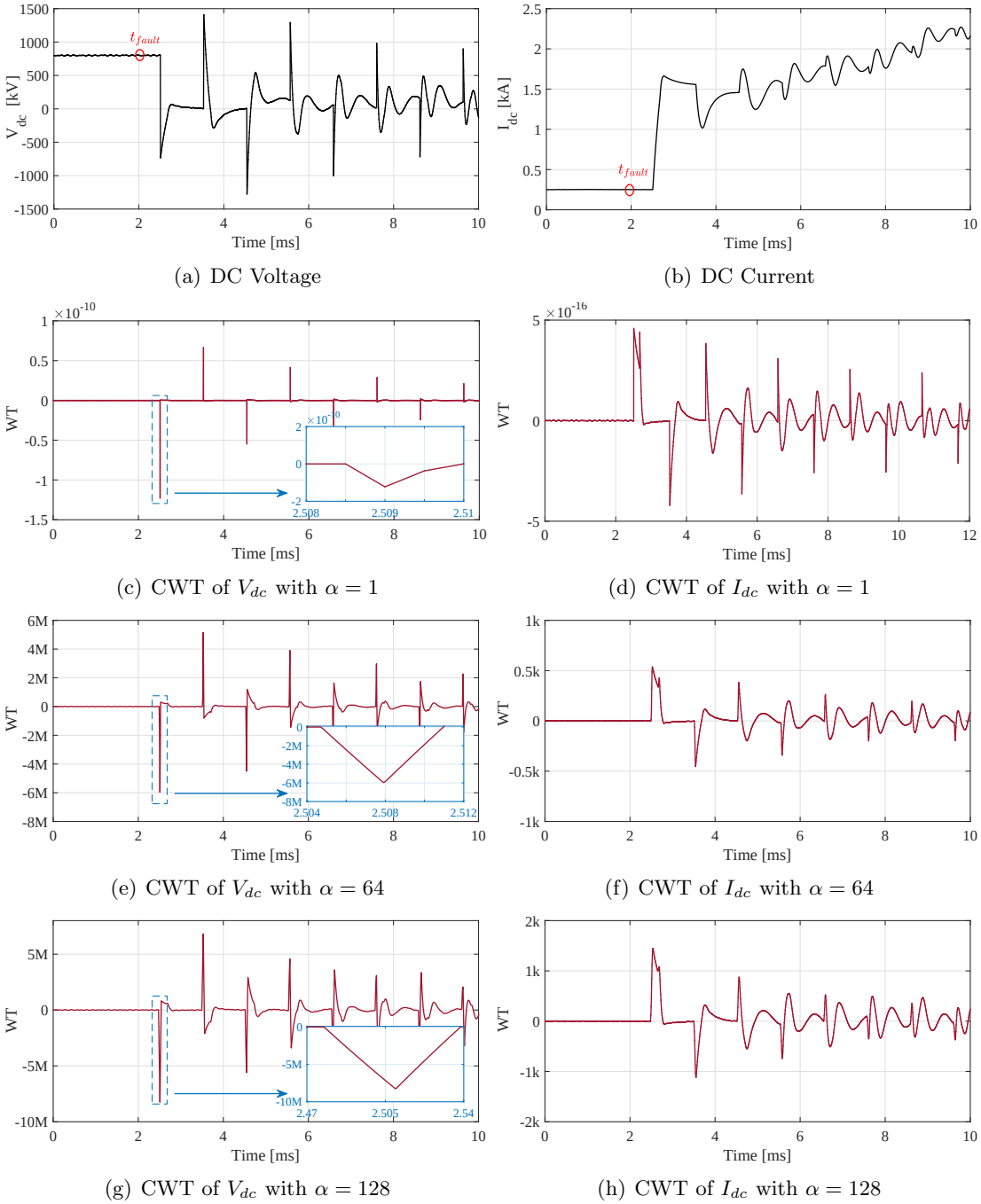
Figure 4.20: Point-to-point HVDC network with fault occurring at 150 on a 300 km line.

Table 4.4: MTDC network parameters.

Parameter	Value
DC voltage [kV]	± 400
Rated power [MVA]	200
DC inductor [mH]	100
Line resistance [Ω/km]	0.015
Line inductance [mH/km]	0.96
Line capacitance [μF/km]	0.012
Line length [km]	300
AC frequency [Hz]	50
AC short circuit level [GVA]	40
AC voltage [kV]	400
MMC levels	401
MMC arm inductance [p.u.]	0.1
MMC equivalent arm capacitance [μF]	20.84

4.4.1 Impact of scaling factor α

In Figure 4.21 the DC voltage and current signatures during DC-side fault and the corresponding Wavelet transforms at different scales (calculated using equation (4.44)) are depicted.



(a) DC Voltage

(b) DC Current

(c) CWT of V_{dc} with $\alpha = 1$

(d) CWT of I_{dc} with $\alpha = 1$

(e) CWT of V_{dc} with $\alpha = 64$

(f) CWT of I_{dc} with $\alpha = 64$

(g) CWT of V_{dc} with $\alpha = 128$

(h) CWT of I_{dc} with $\alpha = 128$

Figure 4.21: DC voltage and current signatures of DC-side fault and the corresponding CWT at different scales.

The fault is triggered at $t = 2$ ms and the resulting DC voltage and current signatures are depicted in Figures 4.21(a) and 4.21(b) respectively. For these two measurements, Wavelet transform has been applied by using three different scales (i.e. $\alpha = 1,\ 64,\ 128$). The Wavelet transform results in 'unique' peaks which correspond to the arrival of travelling waves, present both in voltage and current. Consequently, the detection and realisation of travelling waves becomes more discrete and this is the so called 'signal singularity' [165].

By observing Figures 4.21(c) to 4.21(h), it is evident that the scale of Wavelet transform has an impact on the magnitude but also in the shape of the resulting waveforms. Specifically, the higher the scaling factor α the lower the magnitude and 'narrower' the shape of peaks. The resulting waveforms in conjunction with changes in scaling factor α are well-aligned with the theoretical analysis described in Section 4.3.2.

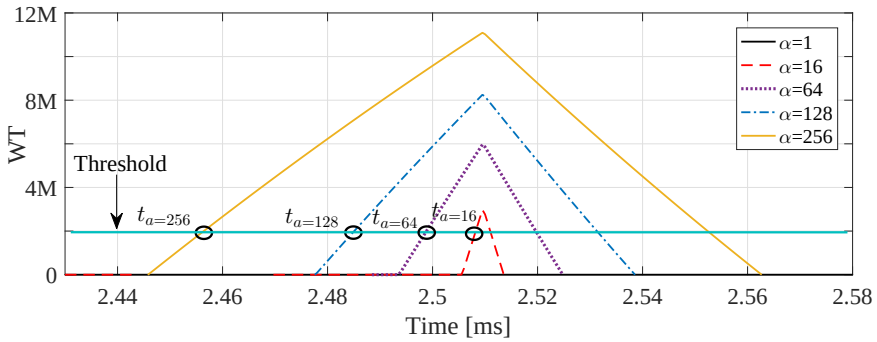
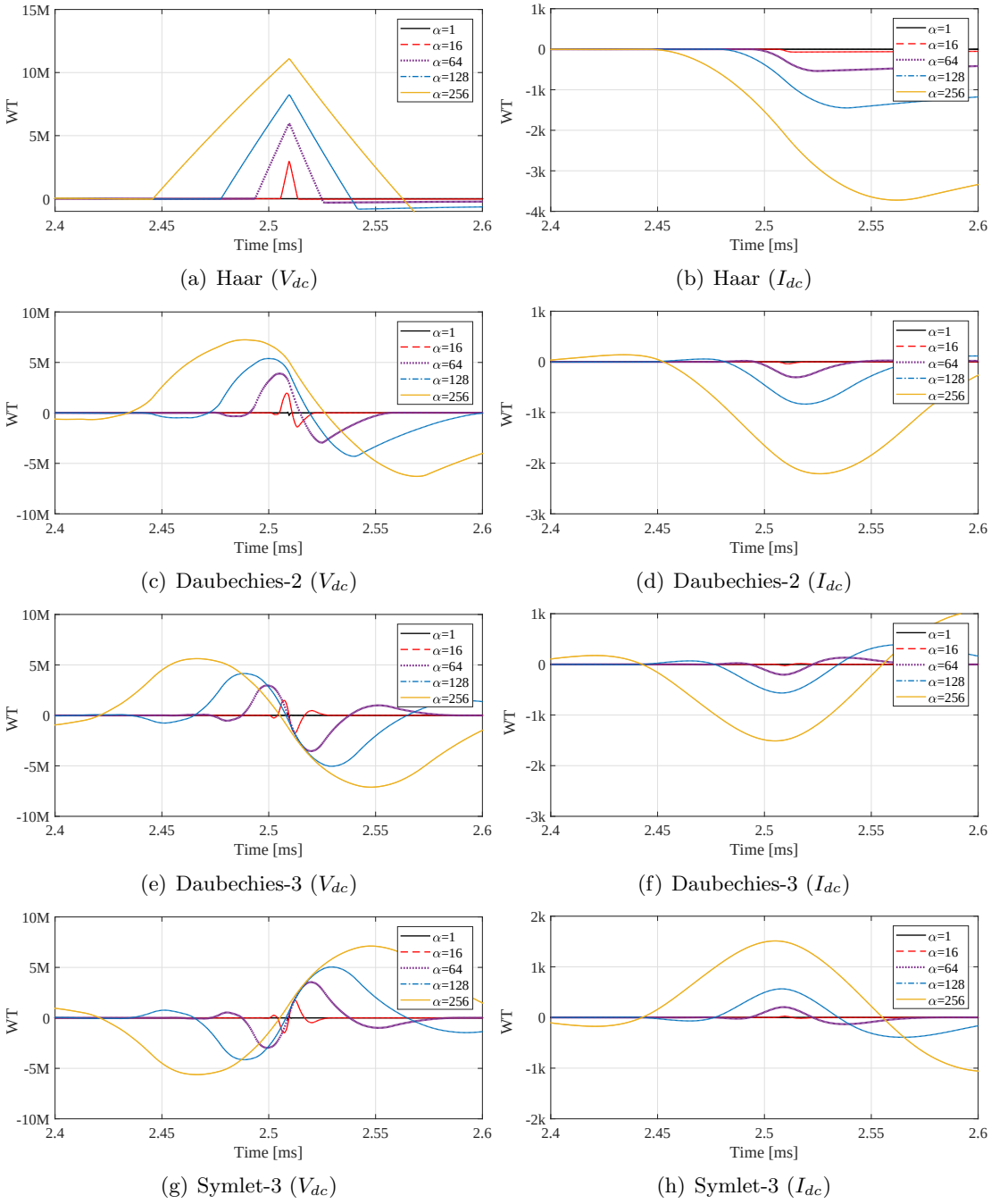


Figure 4.22: Detection of travelling waves by threshold comparison of CWT magnitudes.

Changes in scaling factor α have an impact on the detection of travelling waves. Usually, the detection of travelling waves is achieved by comparing the resulting magnitude of Wavelet transform with a predefined threshold. In Figure 4.22 the absolute values of Wavelet transform of DC voltage alongside a threshold are illustrated. It can be seen that Wavelet transform with different scaling factors α will results in different time indices for travelling wave detection. This is due to the fact that different scales correspond to different magnitudes, but also they cover a different range in the time domain. This raises concerns regarding the selection of the most suitable scale depending on the application. For example, for HVDC protection scheme design this time difference might not have a serious impact. However, in fault location applications, the exact estimation of the arrival time of travelling waves will play a significant role to the calculated distance. Consequently, large deviations from the actual arrival time will lead to large distance errors.

4.4.2 Impact of mother wavelet Ψ

As discussed earlier there is a number of mother wavelets available for the implementation of Wavelet transform. A few of them have been selected and applied in DC voltage and current measurements of the previous fault case illustrated in Figure 4.20.



(a) Haar (V_{dc}) (b) Haar (I_{dc})

(c) Daubechies-2 (V_{dc}) (d) Daubechies-2 (I_{dc})

(e) Daubechies-3 (V_{dc}) (f) Daubechies-3 (I_{dc})

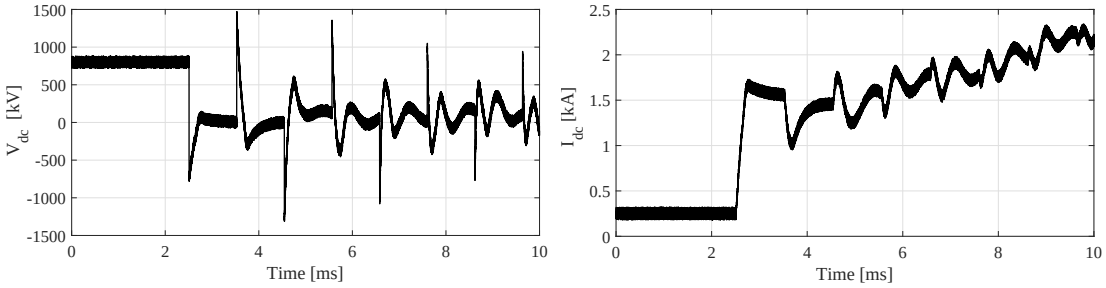
(g) Symlet-3 (V_{dc}) (h) Symlet-3 (I_{dc})

Figure 4.23: Wavelet transform of DC voltage and current signatures using different mother wavelets Ψ and scaling factors α.

The resulting Wavelet Transform signatures are depicted in Figure 4.23 for different mother wavelets at different scales. It can be seen that different mother wavelets affect the magnitude, polarity and symmetry of the resulting waveforms, which all affect the sensitivity and time detection of travelling waves.

4.4.3 Impact of noisy inputs

It has been demonstrated before in Figure 4.21, that in lower scales the time resolution of Wavelet transform (and therefore the time accuracy in detection of travelling waves) is higher. This is due to the fact that lower scales correspond to higher frequency content and the time representation of fast transients phenomena are better illustrated. However, direct usage of a signal in lower scales can be problematic in the case of noisy signals. To better illustrate the impact of noise, the measurements of DC voltage and current used in Figure 4.21 have been contaminated with artificial noise. Afterwards, Wavelet transform in three different scales has been performed. The contaminated measurements together and resulting Wavelet transform are illustrated in Figures 4.24 and 4.25 respectively.

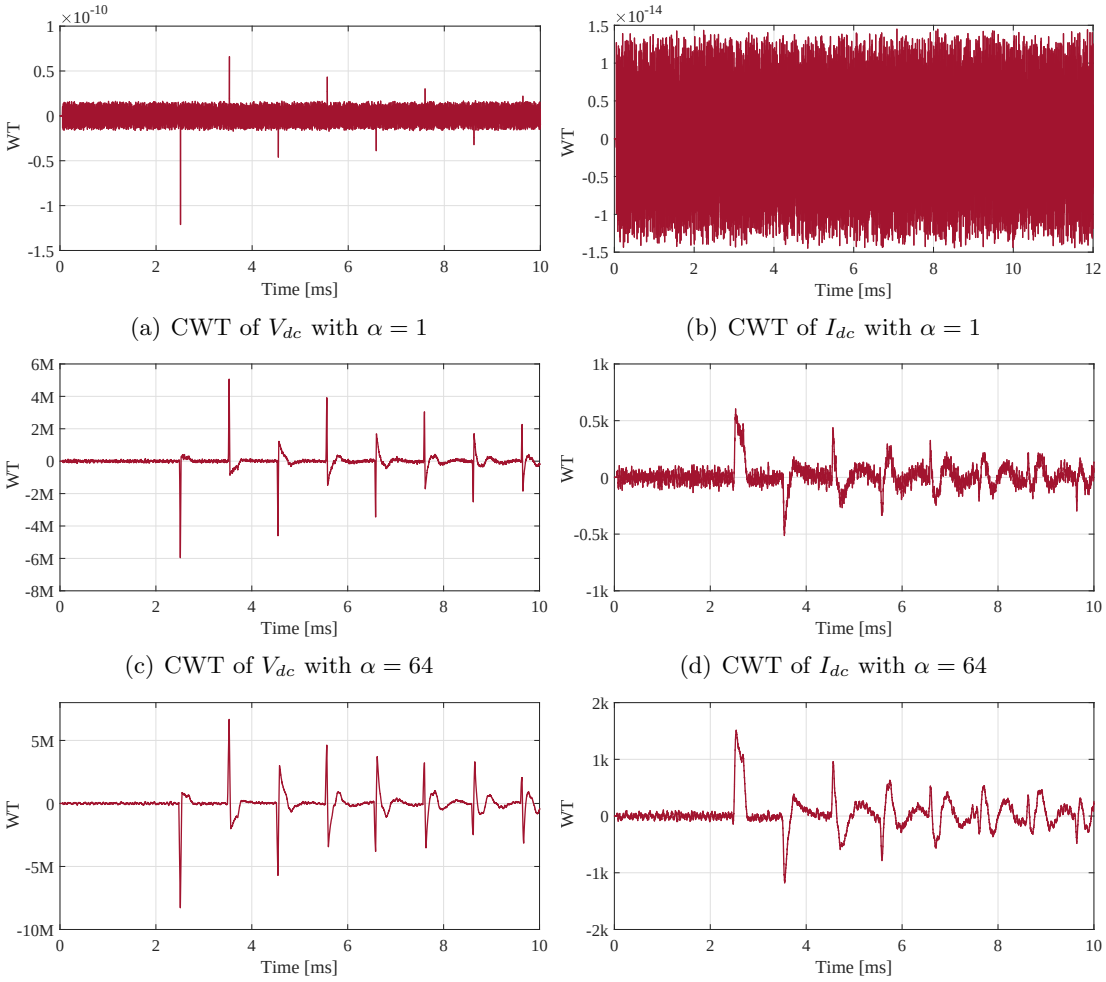


(a) Voltage (b) Current

Figure 4.24: DC voltage and current signatures of DC-side fault considering the presence of noise.

It is evident from Figures 4.25(a) and 4.25(b) that the resulting Wavelet transform in low scales, deduced from noisy signals, has high content of noise. This makes it practically challenging to distinguish the actual fast transient phenomena (i.e. travelling waves) from noise. This is very important in the case of a Wavelet-based protection scheme, in terms of stability to noise and other disturbances and sensitivity to actual faults. This issue can be resolved by increasing the scaling factor (which will lead to a loss of time information) as illustrated in Figures 4.25(c) to 4.25(f). In this case, when higher scale is utilised high frequency content are significantly filtered out.

It is worth mentioning here that a solution to deal with noisy inputs is to utilise



(a) CWT of V_{dc} with $\alpha = 1$

(b) CWT of I_{dc} with $\alpha = 1$

(c) CWT of V_{dc} with $\alpha = 64$

(d) CWT of I_{dc} with $\alpha = 64$

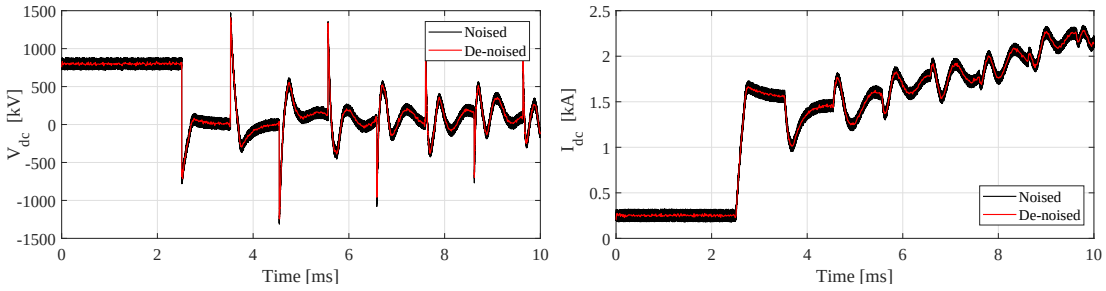
(e) CWT of V_{dc} with $\alpha = 128$

(f) CWT of I_{dc} with $\alpha = 128$

Figure 4.25: Resulting CWT at different scales considering the presence of noise.

Wavelet-based multi-resolution analysis as described in Section 4.3.2.4 to decompose and reconstruct the signal of interest. The aforementioned noise-contaminated measurements have been de-noised by using Wavelet-based multi-resolution analysis. The measurements have been decomposed up to five levels, filtered using fixed-form thresholds and reconstructed. The Wavelet-based de-noising together with the original signal is illustrated in Figure 4.26.

It can be seen that a significant portion of noise has been filtered out. Further filtering can be achieved by decomposing the signal to higher number of scales and/or increasing the cut-off thresholds.

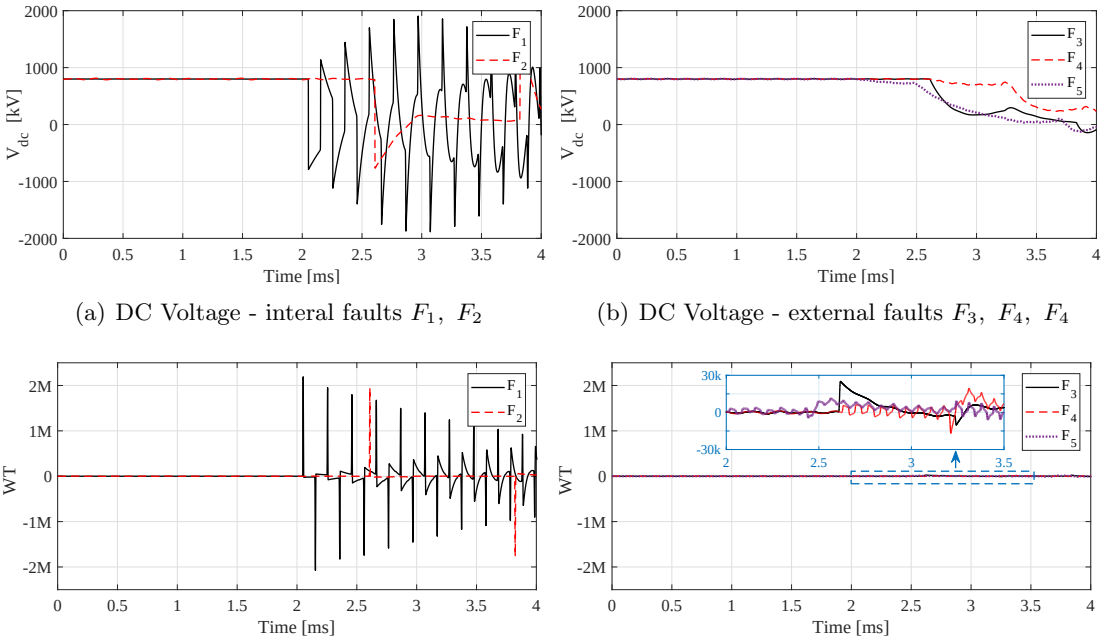


(a) DC Voltage (b) DC Current

Figure 4.26: Signal de-noise using Wavelet-based multi-resolution analysis.

4.4.4 Impact of inductive line termination to Wavelet transform and detection of travelling waves

It has been demonstrated in Section 4.2.2 that the inductive termination of transmission lines forms a significant boundary for DC voltage and current signatures; this was demonstrated both for internal and external faults. The difference is more significant for DC voltage traces than current.



(a) DC Voltage - interal faults F_1, F_2 (b) DC Voltage - external faults F_3, F_4, F_4

(c) WT - interal faults F_1, F_2 (d) WT - external faults F_3, F_4, F_4

Figure 4.27: Post fault DC voltage and the resulting WT.

To further investigate the impact of inductive termination on Wavelet transform and the detection of travelling waves, the DC voltage measurements captured for fault scenarios F_1 to F_5 presented in Section 4.2.2, have been analysed through Wavelet-transform.

Figures 4.27(a) and 4.27(b) illustrate the DC voltage signatures (captured at the

line side of inductor) for internal and external faults respectively. The corresponding Wavelet-transform is depicted in Figures 4.27(c) and respectively 4.27(d).

In the case of internal faults F_1 and F_2, the resulting Wavelet transforms reach high values up to $2 \cdot 10^6$(Figure 4.27(c)). This is due to the fact that the measuring point is closer to the fault and does not have any lumped reactor in-between. As for external faults F_3, F_4 and F_5, the resulting magnitude of Wavelet transforms are highly attenuated (Figure 4.27(d)). This is expected since for any external fault, the equivalent inductance included in the fault current path is always significantly larger than for the internal fault due to the installed lumped reactors (see Table 4.3).

The difference in magnitude of Wavelet transform between and external faults, provides a significant safety margin for fault discrimination and hence to the design of a reliable protection system. This feature is utilised for a protection scheme design which will be demonstrated in the next chapter.

4.5 Summary

In this chapter, a theoretical and simulation-based analysis of fast fault-related transient phenomena in MTDC networks has been presented. It has been found that such studies do not depend on the converter topologies (or generally on the power source), but instead they are more dependent on components taking place within a DC network (after the converter DC terminals) such as current limiting inductors, cables/lines and DC breakers. Additionally emphasis has been given to signal processing methods for obtaining a deeper insight of nature of the faults. The investigation revealed the following remarks:

- Travelling waves can be detected both in DC voltage and current traces.
- The fault resistance can decrease the amplitude of travelling waves. Extremely high values of fault resistance can minimise the sharpness of travelling waves, which in some cases it can be difficult to discriminate them from noise or other disturbances.
- Line termination (e.g. resistive, inductive, capacitive) plays a significant role to the shape of travelling waves.
- The point of measurement affects on a significant degree the captured fault signatures. As a result, depending on the point of measurement different fault-related functions (e.g. protection) can be realised accordingly.

- The deliberate inclusion of additional inductance not only limits the rate of change of DC current but also the resulting DC voltage signatures (and the fact that they may be different depending on fault location and known values of inserted inductance at line terminals) can help to achieve a discriminative non-unit type protection.

- A series of DC-side faults within an MTDC network has been applied. Considering a single point of observation, the resulting signatures and their corresponding analysis has been found to be capable of distinguishing the nature and location of the faults.

- Signal processing methods have been introduced. It has been demonstrated that conventional signal processing techniques such as Fourier Transform are not suitable for fast and simultaneous time-frequency analysis. On the contrary, it has been shown that Wavelet Transform is a powerful tool for analysis of fast transient phenomena such as DC-side faults.

- Two categories of wavelet transform can be distinguished: Continuous Wavelet Transform and Discrete Wavelet Transform (DWT). The selection between CWT and DWT is a trade-off between time accuracy of the wave detection, and processing resources and their associated time delays. In the case of CWT, the accuracy of the wave time detection is better than for DWT techniques but the power requirements are higher. This is the reason that CWT is preferred for fault location applications, where the computational time is not crucial. However, DWT is computationally more efficient, which enables faster wave detection. As a result, DWT is considered more suitable for power system protection applications.

- The selection of mother wavelet and scaling factor α is of major influence to the resulting signatures both in time and amplitude. Attention should be paid to lower scales where noise in the measurements can be amplified and cannot be distinguished from other power system transients.

The work conducted and presented in this chapter formed a basis for developing novel travelling wave-based protection and fault location schemes. These will be analysed in detail later in Chapter 5 and Chapter 6.

Chapter 5

Protection Solutions for MTDC Grids

When a fault occurs in multi-terminal HVDC grids, protection systems are expected to minimise the effects of the fault by disconnecting only the faulted section while permitting the remaining healthy part of the grid to continue normal operation. Therefore, the performance of HVDC protection is very important and necessary to ensure the secure and reliable operation of HVDC grids. Such requirements introduce the need for transient DC fault characterisation, establishment of requirements and structure of HVDC protection schemes and subsequent development of a discriminative, fast, sensitive and reliable DC protection method.

This chapter presents two novel protective solutions for MTDC networks enabling fast, sensitive, reliable and discriminative protection. Simulation and experimental results are presented to verify and support the feasibility of the proposed protection strategies. Part of this chapter includes explanation of optical sensing technology, which one of the proposed protection are based upon. Moreover, the challenges and requirements with regards to protection in HVDC grids are also discussed.

5.1 Requirements and Structure of HVDC Protection

DC grid protection philosophy is well-aligned with the objectives of AC grid protection which include reliability, selectivity, stability, speed and sensitivity [192]. However, there are a few essential differences mainly determining the time window of events. In AC

networks, the fault-clearing time is defined by the ability of synchronous generator to retain synchronism during the disturbances. The critical clearing time is within the region of hundreds of milliseconds. On the contrary, in a DC grid there are other factors affecting the critical time such as the limits imposed by DC breakers and power electronic devices installed inside the converter. Moreover, when a fault is present, the converter is blocked for self-protection purposes. In this case, the controllability of the converter (and partially of DC grid) is temporarily lost. Therefore, more complex control systems are present in the HVDC grid; furthermore attention should pe paid regarding interference of the protection on control systems. Due to the fast nature of DC-side faults, its propagation to other nodes of the grid is highly affected by the clearing time. Consequently, the more nodes lost in the DC grid, the slower the system can be restored to normal operation. Finally, a protection system should be integrated in the HVDC grid without affecting normal operation.

The disconnection of the faulted section will protect the equipment of the HVDC grid from any severe damage. In an HVDC transmission system, different zones might be introduced as shown in Figure 5.1. Different protection principles and philosophies can be used to achieve selective isolation and zone discrimination.

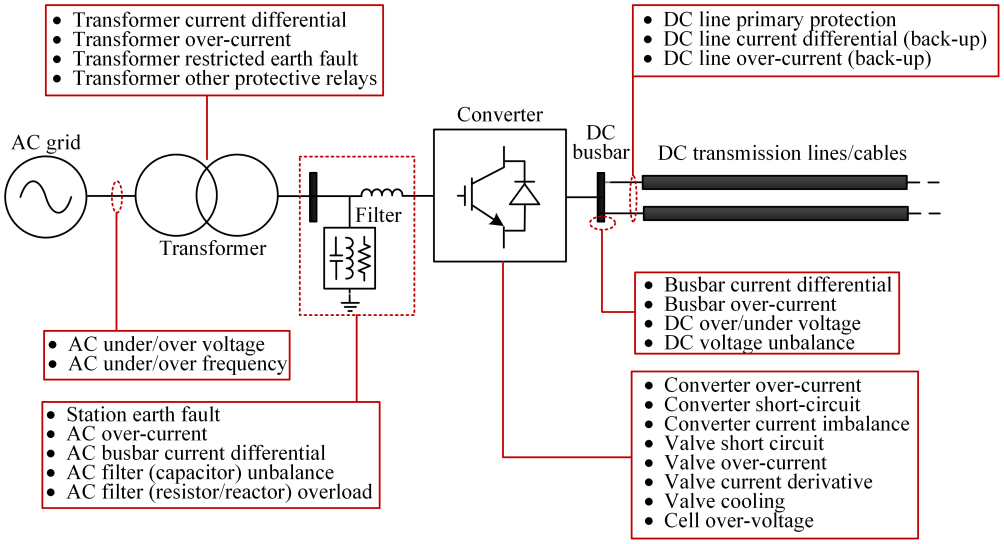


Figure 5.1: Protection functions for a typical VSC HVDC terminal [1–4].

The protection equipment should have a high degree of security and reliability. It should operate quickly and accurately without any malfunctions (failure to operate or maloperation) at all operation modes, and should be able to minimise unnecessary system shutdown resulting from protection equipment failure. Each protection system must be

structured to operate reliably and independently; therefore, the protection systems will include self-supervision and monitoring. Any failures detected in the protection system (hardware or software) shall lead to mitigating actions being taken, such as switch-over to another protection system (either back-up or another primary) and shut-down of the faulty one. It is preferable that each protection system be equipped with dedicated measurement transducers, auxiliary and tripping circuits.

The design of an HVDC protection system should acknowledge the following facets in detail [1, 2, 4, 40]:

- HVDC grid structure.
- Earthing configuration.
- Availability and point of measurements.
- Behaviour of converters for pole-to-pole and pole-to-ground faults.
- Operational conditions prior to a fault.
- Fault types (converter faults, AC-side system faults, DC-side faults).
- Line termination.
- Utilisation of HVDC breaker technology.
- Assistance from communication links.

In addition to the above, the design and coordination of an HVDC protection within a DC substation system should fulfil the following requirements:

- Detection of both pole-to-pole and pole-to-ground faults.
- All equipment shall be encompassed by at least one protection zone.
- Zones of protection shall overlap when possible (to avoid dead zones).
- All faults should be detected by two different protections (main protection equipment and back-up protection with separate transducers as far as practicable).
- The HVDC protection system should be properly coordinated with the HVDC control system.

- The backup protection (usually slower and/or less sensitive) should isolate the faulty units when the main protection fails, while providing backup protection for adjacent zones.
- Inter-station communication interfaces should be provided for protection equipment to allow coordination between converter stations. Transmission delays should meet the functional requirements of the control and protection system.

When a fault is detected, and depending on its location, the following protective actions shall be initiated:

- Selective tripping of HVDC breakers.
- Change of converter control mode.
- Temporary block of the converters.
- Permanent block of converter followed by trip of AC-side breakers (in the case of point-point links or failure of DC-side protection).

5.2 Review of HVDC Protection Philosophies

The existing and proposed HVDC protection schemes can be allocated in three main categories, namely 'non-unit', 'unit' and 'back-up' and shall be analysed in the following subsections. Non-unit protection schemes refer to those methods where the protection algorithm is executed using only local measurements. Unit protection usually involves comparison of quantities at the boundaries of the protected zone as defined by the locations of the measurements. This comparison may be achieved by direct hard-wired connections or via communications links. Back-up protection can be implemented either with local and/or remote measurements. It should be noted that several methods have been proposed in the past for point-to-point HVDC links [156, 193–197]; however, those cannot be applied to MTDC networks since the requirements are fundamentally different both for detection and isolation.

5.2.1 Non-unit

For the implementation of non-communication-based schemes, there is a noteworthy trend towards the placement of DC reactors at both ends of transmission lines. The

intentional placement of such inductive components reduces the rate of rise of DC current, while it changes the resulting DC voltage signatures. Based on the fact that the voltage is different, depending on the faulted line, can assist towards the implementation of a discriminative protection system. [198–201]. In [198], a two-stage protection scheme is proposed by utilising under-voltage and voltage derivative criteria. Nevertheless, the scheme requires validation for highly resistive faults, as it has been only tested for faults with resistance of up to 10 Ω. In [199], the DC voltage derivative (calculated from the line side of the reactor) is used for fast detection and localisation of DC-side faults. However, the post-fault DC voltage response of the converter seems to remain uninfluenced (which is not always the case). Additionally, faults with high resistance, which are likely to affect the performance operation of the protection scheme, are not investigated. Both methods reported in [198, 199] do not take into account transients such as power reversal or the differences between cables and overhead lines. These studies have been carried out in [200] where an alternative approach is introduced by utilising the derivative of DC voltage across the inductor. In [201], a method based on ratio of transient voltages, (calculated by voltage measurements at both sides of current-limiting inductors) is proposed. The method is able to achieve fault sensitivity and selectivity for solid and highly resistive faults with resistances of up to 200 Ω.

A handshaking method is proposed in [202] for detection of DC-side faults. However, due to the fact that the fault clearance is achieved through AC-side breakers (which will take several cycles of AC current and therefore tenths of ms to operate), the scheme can be considered relatively low, while shut-down of the entire converter station is inevitable. In [147], the proposed detection method is based upon the capacitor discharge during the fault. However, the method seems to have poor performance for faults with high resistance. In [146], DC voltage and current signatures are utilised to obtain a fault-distance relationship. All of the methods presented in [146, 147, 202] only approximately estimate the location of the faulted network branch, but the process or the structure of the fault detection scheme is not considered.

The method proposed in [203] utilises travelling waves and derivatives of both current and voltage signals, to establish a discriminative protection system. However, the scheme could be very sensitive to induced noise, and hence cause false tripping. Another method is proposed in [204] based on bus and line current measurements. The scheme requires communication on bus-level for fault discrimination and selective tripping of circuit

breakers (CBs). However, the proposed reliability criterion could be jeopardised by CB failure or by an increasing oscillatory current after the fault clearance of neighbouring line. The detection method in [205] utilises a three-stage approach and a voting scheme to identify and discriminate the existence and location of faults. The stages include wavelet analysis of DC voltages and currents, as well as voltage derivative and amplitude. However, pole-to-ground faults have not been investigated while the protection algorithm appears to be relatively complex and dependent on many parameters, and may therefore be impractical to implement. The method proposed in [206] is based on voltage and current measurements and uses a two stage approach to detect faults in MTDC networks. The first stage is the fault inception which is based on travelling waves detected by wavelet transform. The second stage is the fault location element which is based on the characteristic harmonic of the current. The proposed method utilises very complex mathematical operations while current interruption devices and high resistive faults (more than 100 Ω) are not investigated.

5.2.2 Unit protection schemes

A number of differential-type schemes are proposed in the literature [36,207,208]. In [207], measurements of current from both line ends are utilised to perform Discrete Wavelet Transform (DWT). Internal and external faults are distinguished by calculating and comparing the energy of DWT components. Another current-based differential scheme is reported in [208]. The scheme utilises mechanical DC breakers and comparison of current at each line terminal. However, the scheme is dependent on fault-tolerant converters in order to allow low-speed fault clearance. Moreover, the scheme is based only on a constant predefined threshold, which could make the whole protection system vulnerable to induced noise, instability during non-fault transients and measurement inaccuracies [209]. In [36], a high-speed differential scheme is proposed based on a network of distributed current sensors along the transmission line. The proposed approach has been found to be fast, sensitive and reliable for solid and highly resistive internal faults while maintaining stability during external faults. Some of the main challenges and drawbacks associated with unit protection schemes include the inherent communication time delays, delays associated with encoding and decoding messages and correcting for latency of communications paths, and the reliability of the method if one of the measurements fails or the communications link is compromised.

5.2.3 Backup

Even though numerous unit and non-unit primary relaying algorithms have been proposed, the need for backup relaying is always inevitable. Such schemes can ensure system reliability should the main protection fail to operate. Main protection systems might fail to operate due to several reasons such as failure of transducers, communication system or the relaying algorithm itself [210].

A method in [211] is proposed based on classifications. The approach is based on fault classification in the V/I locus for cleared but also for uncleared faults across the network. The system requires training data and takes into account both CB and relay failure. The proposed scheme provides efficient backup protection but further studies have to be implemented considering acceptable levels of noise, sampling frequency and high resistive faults.

A similar method based on V/I locus can also be found in [212]. However, the sampling frequency requirements have not been specified, while primary protection system failure in case of pole-to-ground faults have not been considered at all.

Another backup protection scheme is proposed in [208]. In this scheme, the DC current is compared against a small threshold, after a specific time of the initial fault inception. However such a scheme is considered to be slow; furthermore, the whole protection concept relies on fault tolerant converters, which would potentially increase cost, losses and complexity.

5.2.4 Summary of review

A review of existing and proposed MTDC protection techniques leaves the impression that much of the reported research focuses on the conceptual aspects but neglects important practical facets such as sampling frequency, time window and breaking capacity and time response of DC interruption devices. This is also evident from Table 5.1 where the aspects of each protection scheme are reported. Additionally, there is no discussion or studies on the practical feasibility of the schemes, and the way measurements and signals exchange can be realised locally (either on a line or busbar) or within a DC substation. Taking into account the requirements of fast DC protection, all of the above play a significant role in the physical implementation of any protection scheme.

Accordingly, this thesis presents two novel protection systems suitable for rapid and discriminative fault detection and isolation in MTDC grids while addressing all the above-mentioned significant facets.

Table 5.1: Summarised review of protection schemes.

Method	Measurements		Breakers	Communication requirement	Sampling frequency	Fault type	
	Voltage	Current					
[198]	Y	Y	DC-HB	N	100 kHz	PGF	Non-unit
[199]	Y	N	DC-HB	N	–	PPF, PGF	
[200]	Y	N	DC-HB	N	–	PPF	
[201]	Y	N	DC-HB	N	50 kHz	PPF, PGF	
[202]	N	Y	AC	N	–	PGF	
[147]	Y	Y	–	N	–	PPF, PGF	
[146]	Y	Y	–	N	–	PPF, PGF	
[203]	Y	Y	DC-HB	N	–	PPF, PGF	
[204]	Y	N	DC-HB	N	50 kHz	PPF, PGF	
[205]	Y	Y	DC	N	–	PPF	
[206]	Y	Y	–	N	20 kHz	PGF	
[36]	N	Y	DC-HB	N	5 kHz	PPF, PGF	Unit
[207]	N	Y	DC	Y	100 kHz	PPF, PGF	
[208]	N	Y	DC-Mec	Y	–	PPF	
[213]	N	Y	DC	Y	–	PPF, PGF	
[214]	N	Y	DC-SS	Y	1 MHz	PPF, PGF	
[211]	Y	Y	DC-HB	N	50 kHz	PPF, PGF	Back-up
[212]	Y	Y	DC-HB	N	–	PPF	

5.3 Scheme 1: Single-ended Differential Protection

This proposed strategy includes a method for rapid detection of faults on VSC multi-terminal HVDC transmission networks using multi-point optical current sensing. The proposed method uses differential protection as a guiding principle, and is implemented using current measurements obtained from optical current sensors distributed along the transmission line. Performance is assessed through detailed transient simulation using verified MTDC models, integrating inductive DC-line terminations, detailed DC circuit breaker models and a network of fibre-optic current sensors. Moreover, the feasibility and required performance of optical-based measurements is validated through laboratory testing. The proposed scheme is termed here as 'single-ended differential protection'.

5.3.1 Protection strategy

The proposed protection strategy is explained using Figure 5.2 where internal and external faults are illustrated. An internal fault is considered to be a fault within the protected element (i.e. DC Line 1 in this case) and an external fault is any fault outside the protected element. A series of current measuring sensors $S_1, S_2, ..., S_n$ are distributed along the line. These measurements can be accessed directly at either end of the line

(the sensing locations are completely passive and require no power supply), where the optical interrogation, protective equipment and CBs are located.

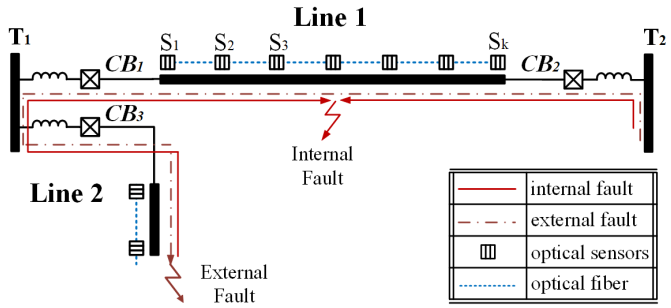


Figure 5.2: Part of an MTDC network illustrating differential protection principle for external and internal DC-side faults.

A series of the differential currents are calculated using the measurements of two consecutive sensors according to

$$\Delta i_{(k)}(t) = i_{s(k)}(t) - i_{s(k+1)}(t) \tag{5.1}$$

where $\Delta i_{(k)}(t)$ is the k-th differential current derived using the currents $i_{s(k)}$ and $i_{s(k+1)}$ measured at two adjacent sensors k and $k+1$ respectively ($k = 1, 2, ..., n-1$).

During external faults the differential current $\Delta i_{(k)}(t)$ will be very close to zero, while for internal faults a high differential value is expected. In order to ensure high sub-millisecond accuracy of the instantaneous differential current, the propagation time delay compensation is applied before the differential current is calculated, given by

$$\Delta i_{(k)}(t) = i_{s(k)}(t - \Delta t) - i_{s(k+1)}(t) \tag{5.2}$$

The amount of compensation, Δt, is constant; additionally, it is directly proportional to the distance between adjacent sensors S_k and S_{k+1} and speed of electromagnetic field propagation. The proposed algorithm is illustrated using a flowchart in Figure 5.3. The protection logic can be analysed in the following three stages:

Stage I: This stage includes a differential current $\Delta i_{(k)}(t)$ threshold comparison with a predefined value I_{TH}. To minimise the chances of protection instability caused by measurement errors, induced noise and/or transients during external faults, the value of the threshold needs to be carefully considered. Therefore, systematic iterative simulations have been performed with pole-to-pole and pole-to-ground faults at multiple locations on the transmission network model (including busbar faults), in order to establish the

optimum current thresholds to be applied in Stage I and Stage II. Additionally, artificial noise was superimposed on the current measurements to verify the threshold selection and reduce the chance of spurious tripping.

Stage II: This stage is based on the rate of change of current. When the threshold I_{TH} is reached (Stage I) for a differential current $\Delta i_{(k)}$, the protection algorithm will look at the historical data of $di_{s(k)}/dt$ and $di_{s(k+1)}/dt$ using a short time window Δt_w. If any of the historical values of the derivatives $di_{s(k)}/dt(t - \Delta t_w)$ or $di_{s(k+1)}/dt(t - \Delta t_w)$ exceed a predefined threshold di/dt_{TH}, the criterion for Stage II is fulfilled. This stage ensures that the relay operating decision is reached purely as a result of a fault and not due to any short signal disturbance (e.g. a short spike should not be visible in the historical data). It was assumed that the window Δt_w=0.2 ms was adequate for this purpose.

Stage III: This stage is included in the protection algorithm to ensure that protection operation does not result from any sensor failure. If no sensor failure is detected, Stage III initiates a tripping signal to the CB. The performance and analysis behind this stage is explained better in Section 5.3.4.8.

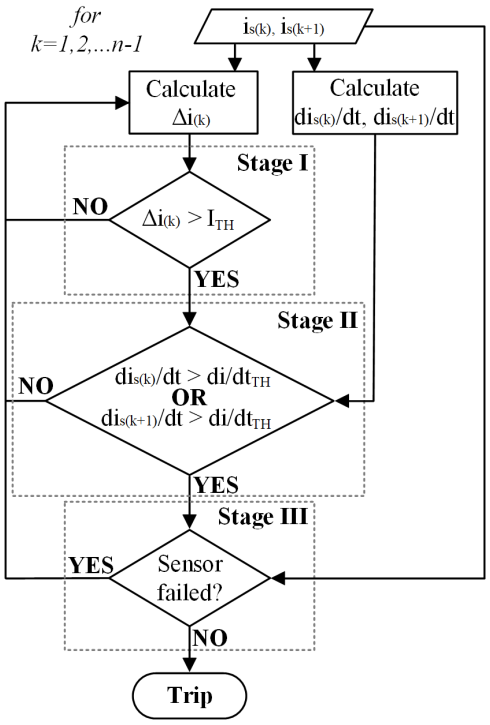
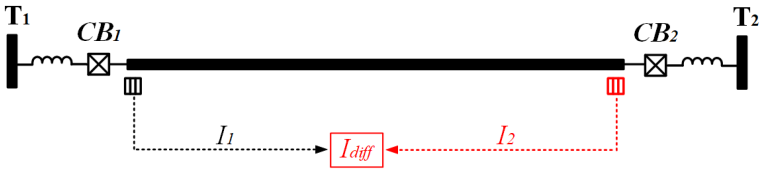


Figure 5.3: Single-ended differential protection process.

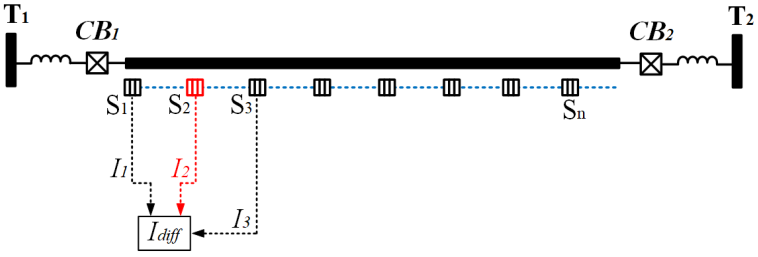
5.3.2 Key advantages

The proposed differential protection scheme offers a number of significant advantages compared to conventional differential protection schemes, which typically require the use of time-consuming encoding and decoding at each line terminal in conjunction with dedicated communications schemes. These advantages are inherently achieved through the single-ended, multi-point sensing design of the proposed scheme and can be analysed in the following three categories:

Enhanced reliability: In conventional differential protection schemes, if one measurement points fails, the entire protection system would be unable to operate (see Figure 5.4(a)). In this case, the entire protection system would lead to spurious tripping, or a back-up protection would take action, which would reduce the speed of operation and potentially subject the system to higher and more sustained fault currents [208, 211], However, considering a case of a sensor failure, the proposed scheme can still operate with a reduced number of sensors. Taking as example the scheme shown in Figure 5.4(b), if sensor S_2 fails, this will be detected and the differential current will be calculated using measurements from sensors S_1 and S_3.



(a) Convenetional differential scheme

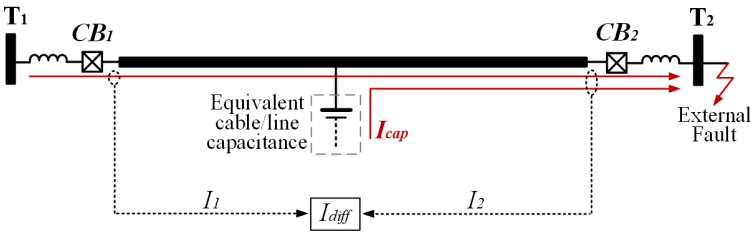


(b) Proposed scheme

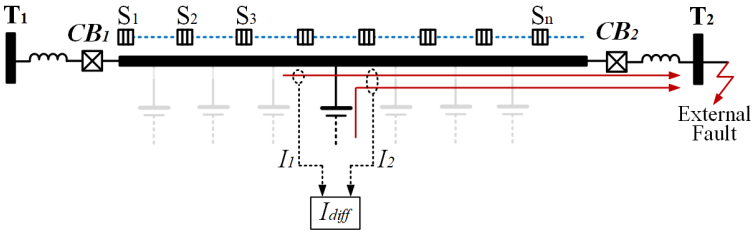
Figure 5.4: Illustration of measurement point fault.

Superior stability: During external faults, the energy in cable capacitance discharges producing a short burst of differential current. With conventional DC differential protection (one measurement point for each cable termination), such a discharging can

compromise protection stability especially with long transmission lines [215]. This is due to the fact that the remote measurement (see I_2 in Figure 5.5(a)) 'sees' the current produced by the discharged of the entire line/cable capacitance. To address this issue, the differential current threshold would have to be increased, or additional delay introduced (as a 'wait and see' strategy) which would reduce protection sensitivity and/or speed. Alternatively, such current would have to be compensated which requires extra computation, voltage measurements while the compensation is not always successful [215]. The proposed protection scheme effectively eliminates the impact of cable capacitance by limiting the length of each protected element to the distance between two adjacent sensors as illustrated in Figure 5.5(b).



(a) Convenetional differential scheme

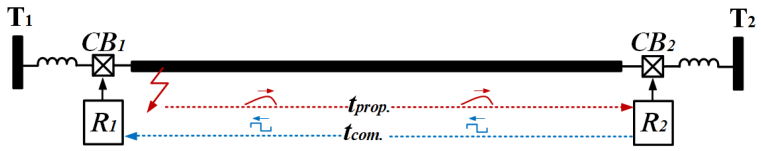


(b) Proposed scheme

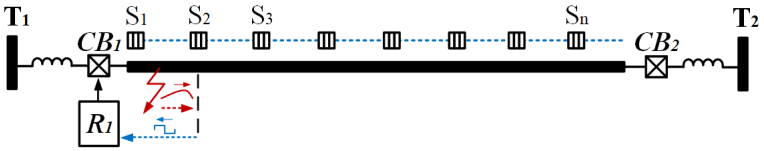
Figure 5.5: Illustration of differential current burst during external faults.

High speed of operation: When an internal fault occurs (see Figure 5.6(a)), in conventional differential protection, there is latency because of the travelling wave (t_{prop}), but also due to the time required for communicating the measured current to the remote end of the line (t_{com}) [208]. This time comprises encoding, time-tagging, latency and decoding. This time can amount to several milliseconds, which, in HVDC systems, is long enough to allow currents to increase enough to exceed the breaking capability of the existing DC breakers. Additionally, such overcurrents can seriously harm the diodes within the IGBTs of the converter during the freewheeling state [79, 146].

The worst case scenario is a close-up fault (also illustrated in Figure 5.6(a)) where the rate of change of current is the highest and the signal delay the longest (as it



(a) Convenetional differential scheme



(b) Proposed scheme

Figure 5.6: Illustration of time delays during close-up faults.

includes additional travelling wave delay to the remote end). Again, with the single-ended distributed sensing system, there is no additional communication time delay, and the delays resulting from travelling waves are limited to the distance between two adjacent sensors (see Figure 5.6(b)), thus enabling ultra-high speed of protection operation.

5.3.3 Modelling

5.3.3.1 MTDC network

A five-terminal HVDC grid has been developed and utilised in all case studies as illustrated in Figure 5.7. The system architecture has been adopted from the Twenties Project case study on DC grids [163]. There are five MMCs operating at ±400 kV (symmetric monopole), HbCBs and current limiting inductors at each transmission line end. The parameters of the AC and DC network components are described in detail in Table 5.2.

On each transmission line, optical sensors are installed to accurately measure DC current every 30 km including the terminals. Therefore, the numbers of DC current sensors are seven, five, eleven, six and four on lines one to five respectively. The arrows indicate the direction of power flow from sending to receiving end of each line. It is emphasised that the proposed method is not direction-dependent. Sending/receiving ends are used as a reference to better demonstrate the protection performance.

5.3.3.2 Converters and DC breakers

The models of power converters utilised in this studies are based on 401-level Type 4 half bridge (HB) MMCs which have been developed according to guidelines and approaches described in Chapter 2.8. Such a representation has been validated against fully detailed

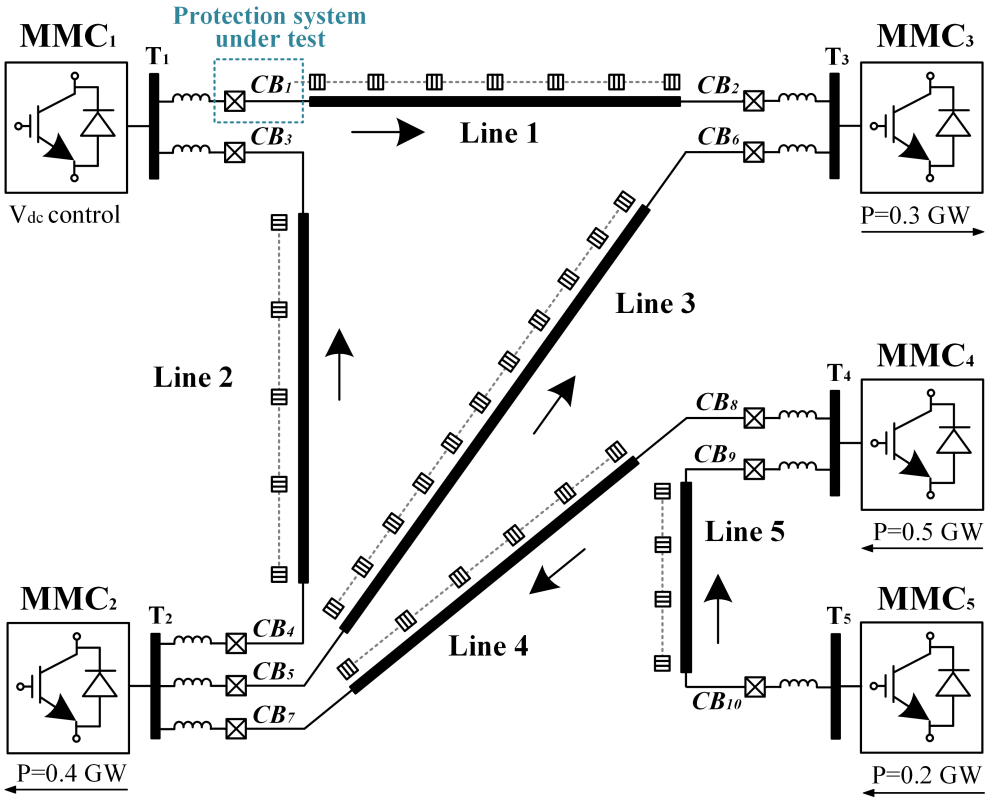


Figure 5.7: Case study five-terminal DC network integrating distributed sensing networks.

Table 5.2: DC and AC Network Parameters.

Parameter	Value
DC voltage [kV]	± 400
DC inductor [mH]	150
Line resistance [Ω/km]	0.015
Line inductance [mH/km]	0.96
Line capacitance [μF/km]	0.012
Line lengths (1 to 5) [km]	180, 120, 300, 150, 90
AC frequency [Hz]	50
AC short circuit level [GVA]	40
AC voltage [kV]	400
MMC levels	401
MMC arm inductance [p.u.]	0.1
MMC equivalent arm capacitance [μF]	20.84

models and has been demonstrated to accurately represent the converter behaviour during steady-state, transient and fault conditions while remaining numerically stable and computationally efficient. The HVDC CB model represents a hybrid design as analysed in Section 2.5.1. The modelling has been implemented following guidelines by ABB's HbCB [82]. According to the manufacturer a breaking time of 2 ms is achievable while the maximum rating of the breaking current is 9 kA.

5.3.3.3 DC inductors

DC transmission lines are terminated with external inductances L_{dc} which limit the rate of rise of DC fault current di_{dc}/dt, and thus, provide additional fault detection time required by the protection system (before the CB maximum breaking current is reached). The inductor size was established taking into account the maximum current of 9 kA, and the sum of all time delays (before the current breaking begins), calculated using

$$t_{op} = t_{CB} + t_{meas} + t_{process} \tag{5.3}$$

where t_{CB} is the operating time of the HbCB (2 ms), t_{meas} is the delay associated with the remote measurement wave propagation and $t_{process}$ is the time allocated to signal processing and decision making by the protective device.

For the calculation of time delays related to the remote measurements, equation (5.4) has been used. The worst case (longest delay) is a solid close-up fault (practically at 0 km) which results in 60 km, a distance the remote measurement has to cover before it arrives at the local end (i.e. 30 km for the current wave to travel to the remote sensor, and 30 km for the measurement to travel back along the fibre optic cable). A refractive index of 1.4682 was assumed for SMF-28 fibre according to [216], thus

$$t_{meas} = \frac{2\ d_{2s}}{c/n} = \frac{60\ [km]}{\frac{299{,}792.5\ [km/s]}{1.4682}} \simeq 0.3\ [ms] \tag{5.4}$$

where d_{2s} is the distance between two sensors, c is the speed of light in vacuum and n is the refraction index of optical fibre.

Taking into account 1 ms for signal processing and decision making, the total estimated time delay is 3.3 ms. With 9 kA as the maximum breaking current and 3.3 ms as the total operation time t_{op}, the current rise rate di_{dc}/dt should be less than 2.73 kA/ms (i.e. $9\ kA/3.3\ ms \approx 2.73\ kA/ms$). The worst case scenario would be a solid fault at any busbar, as illustrated in Figure 5.8(a) and the equivalent circuit in Figure 5.8(b).

Taking into account that CBs are not activated during the initial phase of the fault, their resistance R_{CB} can be taken as zero. Since the worst case is a solid fault, the corresponding fault resistance R_f can also be treated as zero. Consequently, based on the proposed ±400 kV network and for a solid fault at any busbar, the theoretical value of the inductor is calculated according to

(a) Busbar fault at DC terminal (b) Equivalent circuit

Figure 5.8: Illustration of DC busbar fault for L_{dc} sizing.

$$L_{DC} \geq \frac{\Delta V}{di_{DC}/dt} \geq \frac{400\ kV}{2.73\ kA/ms} \rightarrow L_{DC} \geq 146.5\ mH \tag{5.5}$$

where L_{dc} is the inductor value, ΔV is the inductor voltage and di_{dc}/dt the DC current rise rate.

For clarity, Figure 5.9 illustrates simulation results for a pole-to-pole solid fault at terminal T_1 (see Figure 5.7), trigerred at $t = 0$ ms with 2 ms post fault data for different inductance values.

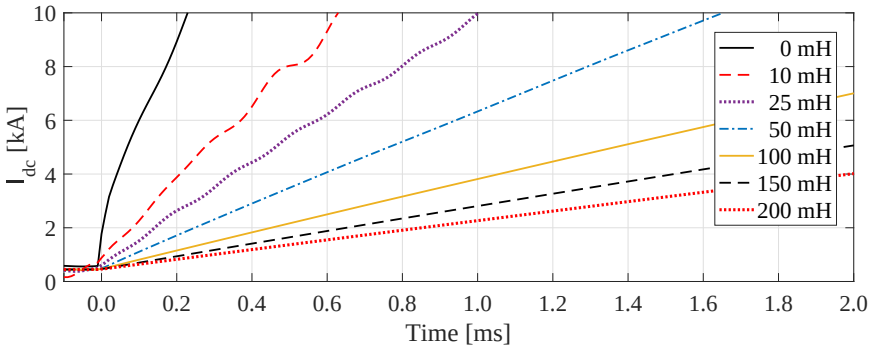


Figure 5.9: Rate of rise of DC current with different inductance values, for solid pole-to-pole fault at terminal T_1.

Table 5.3 presents the time required to reach 9 kA for the inductances illustrated in Figure 5.9. As calculated by equation (5.5), it is therefore verified that the inductance value of 150 mH is the most appropriate option.

Table 5.3: Time indices at 9 kA.

Inductance [mH]	0	10	25	50	100	150	200
Time [ms]	0.22	0.60	0.93	1.49	2.70	3.97	5.31

5.3.4 Simulation results

5.3.4.1 Fault scenarios

This section presents simulation results which quantify the overall performance of the proposed protection scheme under different fault scenarios, including pole-to-pole faults, pole-to-ground faults(incorporating highly resistive faults) and busbar faults (all faults are permanent). In all cases the measurements have been contaminated with white noise to account for possible effects due to measurement-related noise on the protection response. A selection of representative test cases have been considered and summarised in Table 5.4; which demonstrate the worst case scenarios in terms of stability and sensitivity of the scheme.

Table 5.4: Description of fault scenarios.

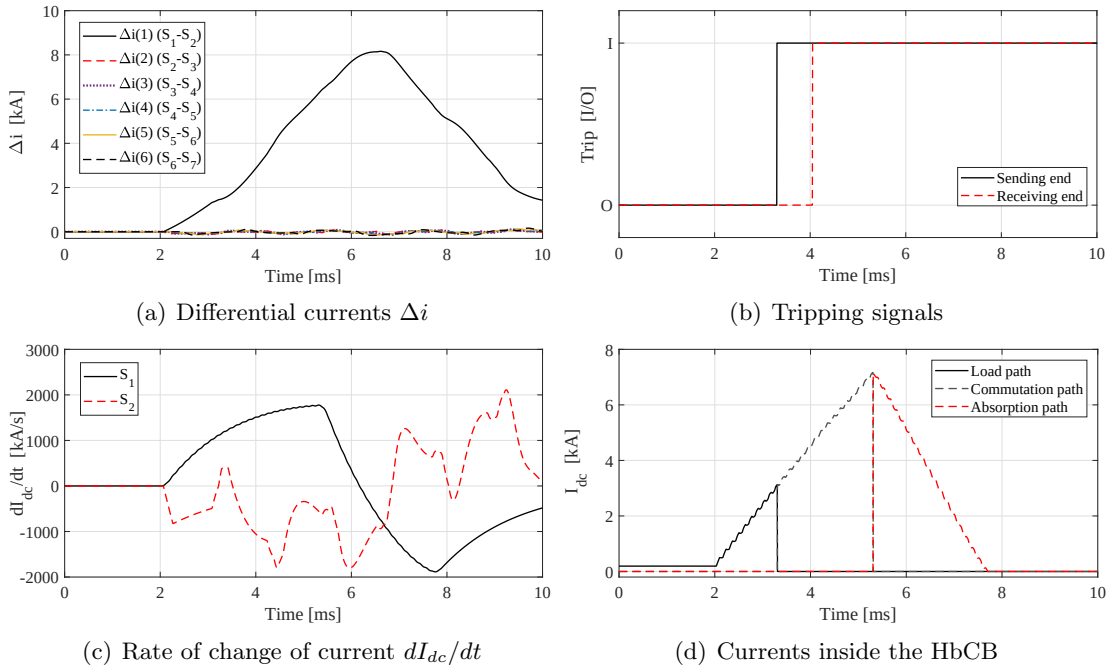
Scenario	Description	Classification
I	Pole-to-pole fault 10 km at Line 1 ($R_f \approx 0\ \Omega$)	Solid, close-up, internal
II	Pole-to-ground fault 10 km at Line 1 ($R_f = 500\ \Omega$)	Highly resistive, close-up, internal
III	Pole-to-pole fault 179.5 km at Line 1 ($R_f \approx 0\ \Omega$)	Solid, remote, internal
IV	Pole-to-ground fault 179.5 km at Line 1 ($R_f = 500\ \Omega$)	Highly resistive, remote, internal
V	Pole-to-pole fault at terminal T_3 ($R_f \approx 0\ \Omega$)	Solid, forward, external
VI	Pole-to-pole fault at terminal T_1 ($R_f \approx 0\ \Omega$)	Solid, reverse, external
VII	Sensor failure at Line 1 (4^{th} sensor)	N/A

For the fault scenarios presented in Table 5.4 the performance is assessed considering that protection scheme is installed at Line 1.

5.3.4.2 Fault scenario I

In Figure 5.10 the protection response to a fault occurring at 10 km from terminal T_1 on DC Line 1 (internal fault) is illustrated. The fault is triggered at $t = 2$ ms. During this fault, which is physically located between sensors S_1 and S_2, it can be seen that the differential current derived from the measurements of these two sensors is increasing rapidly (Figure 5.10(a)), exceeding the protection threshold; thus, fulfilling the first operation criterion is fulfilled.

Since the fault is internal, it can be seen that prior to the fault detection the rate of change di_{dc}/dt for both currents (sensors S_1 and S_2,) are non-zero (Figure 5.10(c)) which indicates the satisfaction of the second criterion. Finally, as shown in Figure 5.10(b), a tripping signal is initiated by the third criterion (Stage III). The tripping signal sending end is initiated with a time delay which correspond to the propagations time of fault (i.e. time required for the fault to be 'seen' at receiving end of DC Line 1). The fault



(a) Differential currents Δi

(b) Tripping signals

(c) Rate of change of current dI_{dc}/dt

(d) Currents inside the HbCB

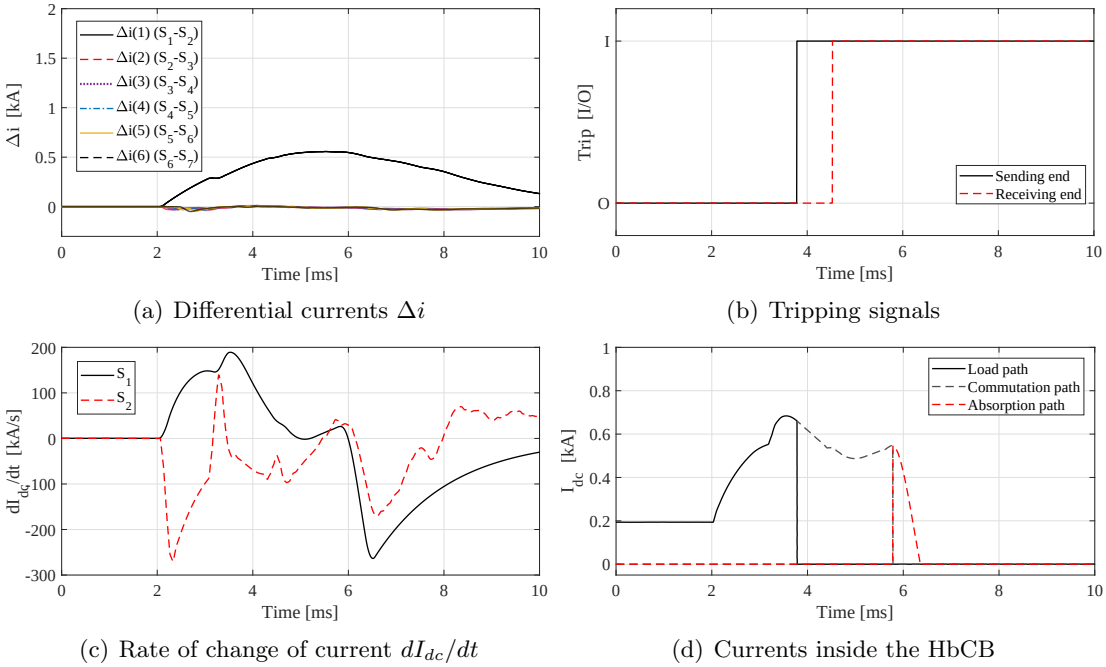
Figure 5.10: Protection system response for fault scenario I.

current interruption process is illustrated in Figure 5.10(d) for sending of DC Line 1. Before the breaker operates the current flows through the commutation path. After the fast mechanical disconnector opens (2 ms) the current flows through the surge arrester where it gradually reduces to zero and the interruption process is finally complete. It can be seen that after the initiation of the tripping signal, it takes 2 ms for the breaker to operate.

5.3.4.3 Fault scenario II

Figure 5.11 illustrates the protection response to a highly resistive ($R_f = 500\Omega$), close-up fault occurring at 10 km from terminal T_1 on DC Line 1. Like previously in fault scenario I, the fault is physically located between sensors S_1 and S_2.

The response is quite similar to fault scenario I, but some differences can be seen. Initially, the magnitudes of differential currents Δi (FIgure 5.11(a)) and current derivative dI_{dc}/dt (Figure 5.11(c)) reach lower values due to the high resistance. This results in slower initiation of tripping signals (i.e. it takes more time to reach the threshold values). Finally, the fault current is driven to zero and fault is cleared (Figure 5.11(d)).



(a) Differential currents Δi

(b) Tripping signals

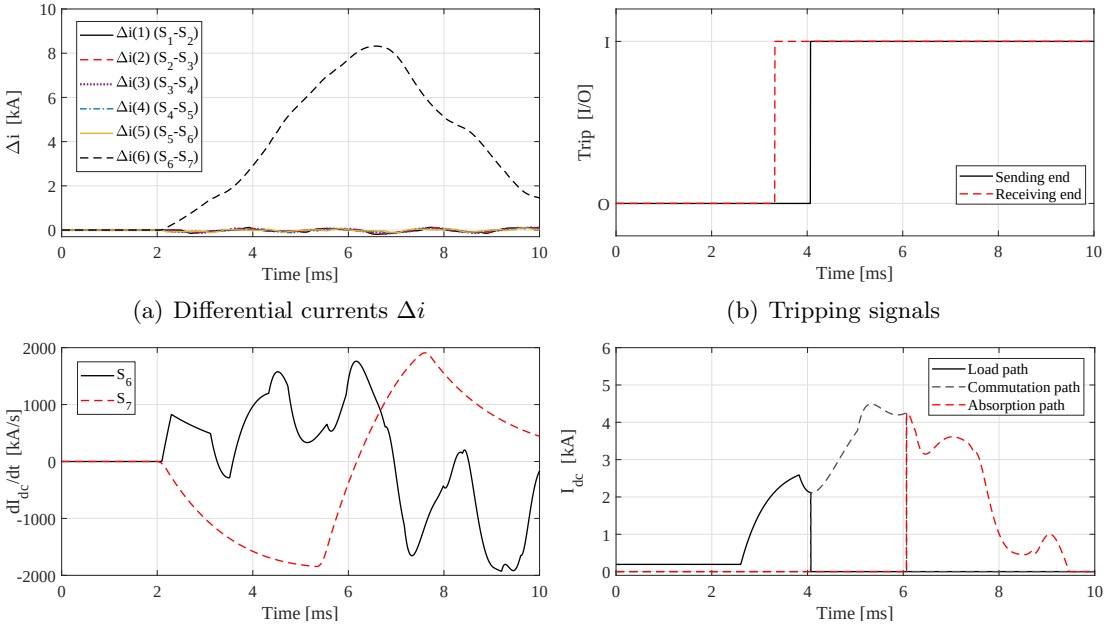
(c) Rate of change of current dI_{dc}/dt

(d) Currents inside the HbCB

Figure 5.11: Protection system response for fault scenario II.

5.3.4.4 Fault scenario III

The response of the protection system for a remote, pole-to-pole fault, occurring at 179.5 km from T_1 on DC Line 1, is depicted in Figure 5.12.



(a) Differential currents Δi

(b) Tripping signals

(c) Rate of change of current dI_{dc}/dt

(d) Currents inside the HbCB

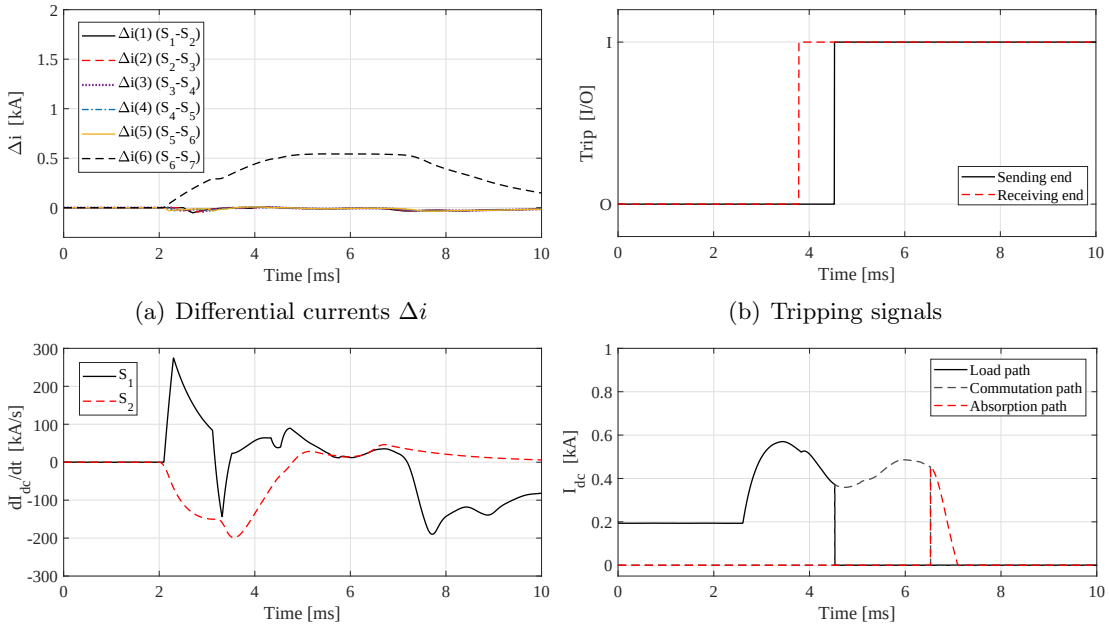
Figure 5.12: Protection system response for fault scenario IV.

At this case, the fault is physically located between sensors S_6 and S_7. This is the reason that differential current Δi from the measurements of these two sensors is increasing rapidly (Figure 5.12(a)). Accordingly, the corresponding rate of change di_{dc}/dt (Figure 5.12(c)) is non-zero, which satisfies the second criterion (Stage II).

Finally, tripping signals are generated both for sending and receiving ends as shown in Figure 5.12(b). It is worth pointing out that at this case the tripping signal on receiving end is initiated faster that the one on sending. This is exactly the opposite response from the one observed in fault scenario I (i.e. close-up fault).

5.3.4.5 Fault scenario IV

In Figure 5.13, the protection response to a fault occurring at 179.5 km from terminal T_1 on DC Line 1 (internal fault) is illustrated. The response is quite similar with the pole-to-pole fault described previously in fault scenario III. However, at this case the fault is highly resistive with $R_f = 500\ \Omega$. Consequently, the magnitudes observed in differential currents Δi (Figure 5.13(a)), rate of change di_{dc}/dt (Figure 5.13(c)), and currents inside HbCB (Figure 5.13(d)), are quite lower.



(a) Differential currents Δi

(b) Tripping signals

(c) Rate of change of current dI_{dc}/dt

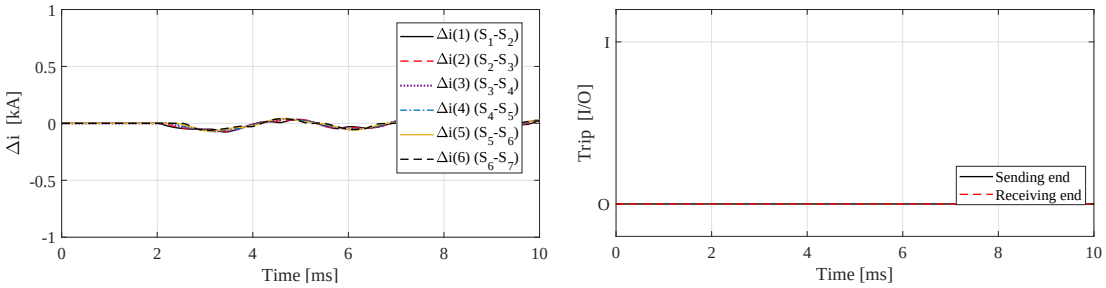
(d) Currents inside the HbCB

Figure 5.13: Protection system response for fault scenario IV.

The tripping signals illustrated in Figure 5.13(b) are initiated much slower (compared to the tripping signals generated for previous scenario shown in Figure 5.12(b)).

5.3.4.6 Fault scenario V

In order to demonstrate the superior stability of the scheme, an external pole-to-pole busbar fault (as seen by the protection system of DC Line 1) has been applied at terminal T_3. Figure 5.14 illustrated the response of the system. Figure 5.14(a) illustrates the differential currents as calculated by the proposed protection scheme and it is evident that they remain at relatively low values and hence there no tripping signal initiated (Figure 5.14(b)).



(a) Differential currents Δi (b) Tripping signals

Figure 5.14: Protection system response for fault scenario V.

During an external fault, the cable capacitance between two measurement points discharges to the fault, producing a short temporary burst of differential current. The longer the distance between the measurement points, the higher the cable capacitance, hence the higher the magnitude of this temporary differential current. For the proposed protection scheme, such differential current is limited by the capacitance between two sensing points (i.e. 30 km). The differential current as calculated by a conventional differential protection scheme is much higher due to the inclusion of the entire line capacitance.

Figure 5.15 illustrates the differential currents as calculated by the proposed protection scheme (i.e. obtained from two adjacent sensors S_1 and S_2) and a conventional differential protection (i.e. two measuring points at opposite ends of the line). In order for the protection system to remain stable during such external faults, a threshold (and probably a time delay) is required to be included in the algorithm, which in the case of a conventional scheme would be much higher, leading to a 'sensitivity loss'.

5.3.4.7 Fault scenario VI

An additional external fault has also been considered to test the stability of the proposed scheme. This time, however, the fault is placed at terminal T_1 and hence is considered a

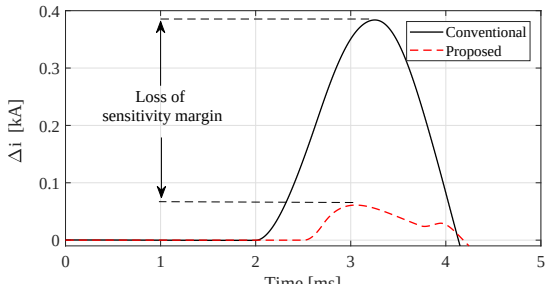
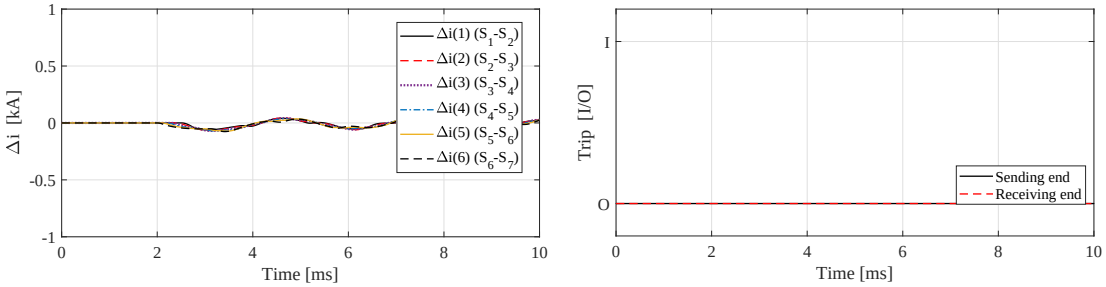


Figure 5.15: Differential currents for external pole-to-pole busbar fault at T3 as seen by a conventional and the proposed differential scheme of DC line 1.

reverse one. The response of the protection system is depicted in Figure 5.16



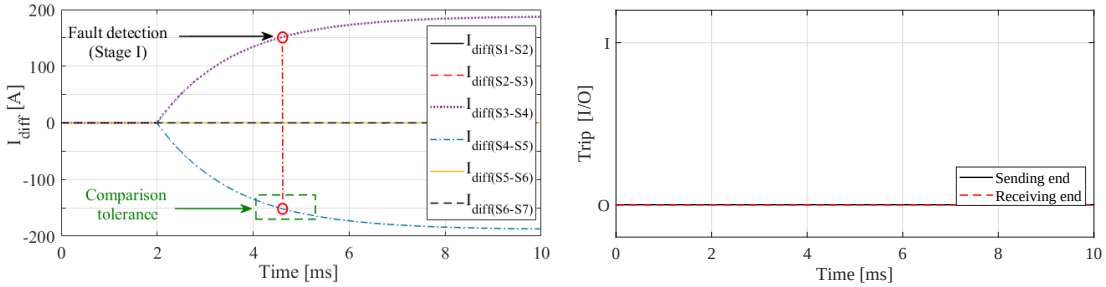
(a) Differential currents Δi (b) Tripping signals

Figure 5.16: Protection system response for fault scenario VI.

Since the differential currents (Figure 5.16(a)) remain at relatively low values, there is no tripping signal initiated (Figure 5.14(b)).

5.3.4.8 Fault scenario VII

Figure 5.17 depicts a case where the 4^{th} sensor on DC Line 1 fails. This is emulated by artificially driving the current measurement to zero (worst case scenario) at $t = 2$ ms. Such a change is expected to make an impact on all of the differential currents calculated measurements from the fourth sensor (i.e. $I_{diff(S3-S4)}$, $I_{diff(S4-S5)}$).



(a) Differential currents Δi (b) Tripping signals

Figure 5.17: Protection system response considering a failure of the 4^{th} sensor.

The key to detection of a sensor failure is the comparison of the differential current (e.g. $I_{diff(S3-S4)}$) at the time instant when Stage I operates with an adjacent differential current ($I_{diff(S4-S5)}$). As Figure 5.17(a) illustrates (and considering a threshold set at 150 A), such currents are expected to have similar amplitudes but opposite polarity. A comparison tolerance of ±10% is included to improve reliability of sensor failure detection. Consequently, as seen in Figure 5.17(b) no tripping has been observed in this case.

5.3.4.9 Additional fault scenarios

Tables 5.5 and 5.6 illustrate simulation results for pole-to-pole and pole-to-ground faults respectively, for different distances along all transmission lines. It can be seen that in all cases only the required breakers operate, proving high selectivity of the scheme. It is also important to report that the CB current never exceeds 9 kA as required. This verifies the importance of the inductive terminations of the transmission lines. For pole-to-ground faults the protection system has been tested with ground fault resistances of up to 500 Ω and the protection scheme has been found to successfully and correctly operate in all cases.

Table 5.5: Protection system performance results for pole-to-pole faults.

Line	**Distance [km]**	**Breakers operated**	**Sending end**		**Receiving end**	
			CB trip time [ms]	**CB max. current [kA]**	**CB trip time [ms]**	**CB max. current [kA]**
1	1	CB_1, CB_2	1.329	7.45	2.075	4.07
	90	CB_1, CB_2	1.525	5.12	1.675	5.28
	120	CB_1, CB_2	1.677	5.41	1.525	5.82
	179	CB_1, CB_2	2.074	4.44	1.331	7.07
2	1	CB_3, CB_4	1.327	7.49	1.775	5.17
	25	CB_3, CB_4	1.280	6.47	1.730	5.00
	60	CB_3, CB_4	1.373	5.97	1.524	5.81
	119	CB_3, CB_4	1.774	5.56	1.326	7.06
3	1	CB_5, CB_6	1.328	7.44	2.076	4.10
	150	CB_5, CB_6	1.523	5.11	1.676	5.30
	250	CB_5, CB_6	1.674	5.38	1.526	5.83
	299	CB_5, CB_6	2.073	4.43	1.327	7.04
4	1	CB_7, CB_8	1.332	8.03	1.925	3.80
	75	CB_7, CB_8	1.521	6.46	1.520	4.75
	100	CB_7, CB_8	1.670	5.84	1.375	5.06
	149	CB_7, CB_8	1.928	5.46	1.323	6.44
5	1	CB_9, CB_{10}	1.325	7.33	1.630	5.20
	45	CB_9, CB_{10}	1.376	6.18	1.374	5.73
	89	CB_9, CB_{10}	1.631	5.64	1.330	6.98

Table 5.6: Protection system performance results for pole-to-ground faults.

Line	Distance [km]	Breakers operated	Sending end		Receiving end	
			CB trip time [ms]	CB max. current [kA]	CB trip time [ms]	CB max. current [kA]
1	1	CB_1, CB_2	1.382	1.65	2.125	1.05
	90	CB_1, CB_2	1.565	1.40	1.715	1.12
	120	CB_1, CB_2	1.714	1.42	1.567	1.19
	179	CB_1, CB_2	2.128	1.38	1.380	1.43
2	1	CB_3, CB_4	1.377	2.12	1.820	0.98
	25	CB_3, CB_4	1.330	2.03	1.780	1.03
	60	CB_3, CB_4	1.420	1.84	1.566	1.04
	119	CB_3, CB_4	1.830	1.75	1.381	1.22
3	1	CB_5, CB_6	1.376	2.27	2.715	0.96
	150	CB_5, CB_6	1.865	1.67	2.015	1.09
	250	CB_5, CB_6	2.460	1.60	1.418	1.37
	299	CB_5, CB_6	2.725	1.50	1.388	1.47
4	1	CB_7, CB_8	1.385	2.35	1.975	0.82
	75	CB_7, CB_8	1.568	1.91	1.565	0.84
	100	CB_7, CB_8	1.717	2.02	1.416	0.94
	149	CB_7, CB_8	1.970	2.01	1.375	1.07
5	1	CB_9, CB_{10}	1.400	0.81	1.700	1.08
	45	CB_9, CB_{10}	1.415	0.74	1.414	1.13
	89	CB_9, CB_{10}	1.680	0.86	1.383	1.25

5.3.5 Optical sensing

Hybrid optical voltage and current sensors have previously been developed by the authors [217–219] to enable remote AC and DC voltage and current measurements in various metering and protection applications including distance and differential protection [220–223]. It will be shown in the following sections that the optical sensors technology is suitable for rapid detection of faults in HVDC circuits.

5.3.5.1 Working principle

Fibre Bragg Grating (FBG) sensors are formed by periodic modulation of the refractive index along an optical fibre core over a length of 5-20 mm.

As illustrated in Figure 5.18, when such a structure is illuminated by a broadband light, it reflects a relatively narrow part of the incident light spectrum with a distinctive peak in the light intensity around the so called Bragg wavelength, λ_B. The spectral position of the peak is determined during the sensor fabrication process and described by the following relation:

$$\lambda_B = 2\ n_{eff}\ \Lambda \tag{5.6}$$

where n_{eff} is the effective refractive index of the FBG section and Λ is the grating period.

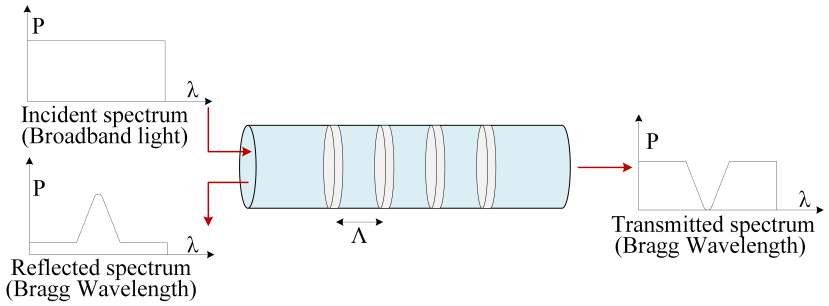


Figure 5.18: FBG structure.

Any relative change in the grating period due to longitudinal elongation or contraction of the fibre causes spectral shift of the FBG peak. Since the refractive index of the fibre is a function of temperature, the FBG peak spectral position is also temperature dependent. A relative change in the FBG peak wavelength, $\Delta\lambda_B/\lambda_B$, due to a change in strain, $\Delta\epsilon$, and temperature, ΔT, can be expressed by

$$\Delta\lambda_B = C_\epsilon \Delta\epsilon + C_T \Delta T \tag{5.7}$$

where C_ϵ and C_T are the strain and temperature sensitivities [224].

5.3.5.2 Sensor design

For the purposes of demonstrating the practical feasibility of DC current measurements, four FBGs inscribed in polyimide coated fibres, having a length of 7 mm, a bandwidth of 0.3 nm and peak wavelengths at 1539.60, 1551.56, 1554.72 and 1557.38 nm (as shown in Figure 5.19) were utilised to build four hybrid low voltage sensors in order to prove the principle of the new protection scheme.

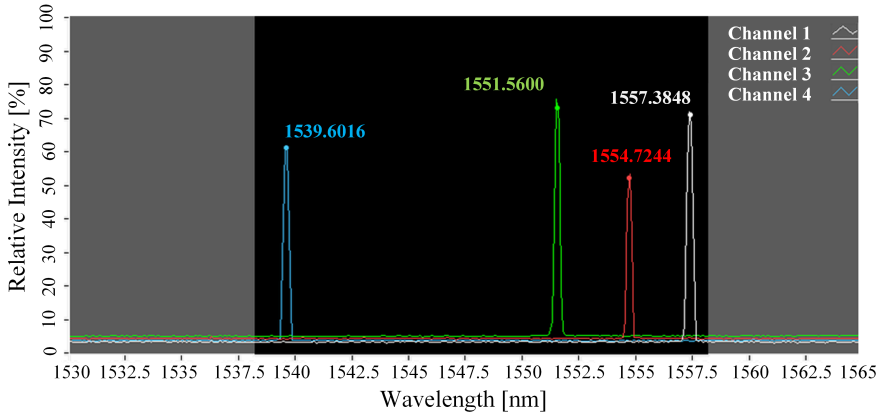


Figure 5.19: FBG spectra.

To construct a hybrid low voltage sensor, a 9 mm low voltage stack, P-883.11 PICMA® from Physik Instrumente Ltd [225] having a maximum AC operating voltage of 30 V_{peak} (21.21 V_{rms}) was fixed between two alumina end blocks and an FBG sensor was pre-tensioned and epoxied to the ceramic blocks using EPO-TEK® 353ND. The sensor construction is shown in Figure 5.20. Providing there is no mechanical stress in the piezoelectric material, the strain (i.e. relative elongation $\Delta l/l$) induced by an external electric field is given by

$$\epsilon = d_{33}E = d_{33}\frac{V}{l} \tag{5.8}$$

where d_{33} is the longitudinal piezoelectric charge constant, E is the electric field, V is the voltage applied across the piezoelectric material and l is the length of the material [217].

A voltage applied across the stack generates strain which is exerted on the FBG producing a corresponding shift in its peak wavelength. Thus, the peak wavelength shift can be calibrated in terms of voltage [217].

By monitoring voltage across a burden resistor connected to the output of a conventional current transformer (CT), an AC optical current sensor can be realised whereby the FBG wavelength shift may be related to current [218]. Ultimately, by replacing a piezoelectric component with a magnetostrictive transducer, a DC current sensor can be realised [219], which would be a device of choice for the final deployment of this system. Light, composite insulators can be used to provide the means of guiding optical fibre between the sensors (installed directly on the conductor) and the pole which is at ground potential. Optical fibre would be provided in a trench alongside the HVDC transmission line, or in some cases may be integrated within the conductors or wrapped around conductors (very common in AC systems).

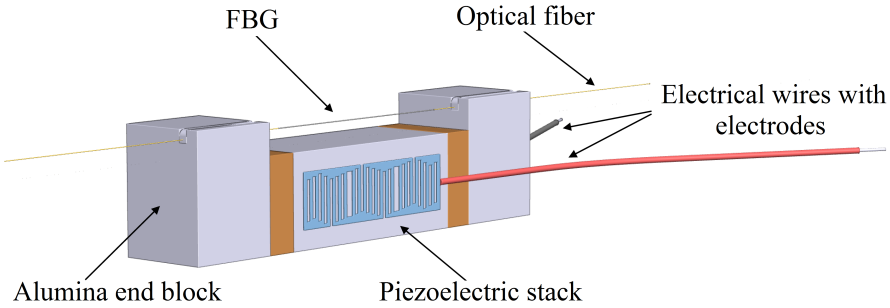


Figure 5.20: Hybrid FBG-based voltage sensor.

5.3.5.3 Experimental arrangement

A diagram of the experimental set-up utilised for practical validation of the proposed scheme is shown in Figure 5.21. Pre-simulated fault currents at corresponding four locations along the transmission line were used to produce replica voltage waveforms (generated directly from a multi-function data acquisition card). These voltage traces (which represent the DC line currents) were physically input to the optical sensors and the sampled data obtained from the optical interrogation system was stored on a PC for processing by the protection system algorithm developed in Simulink.

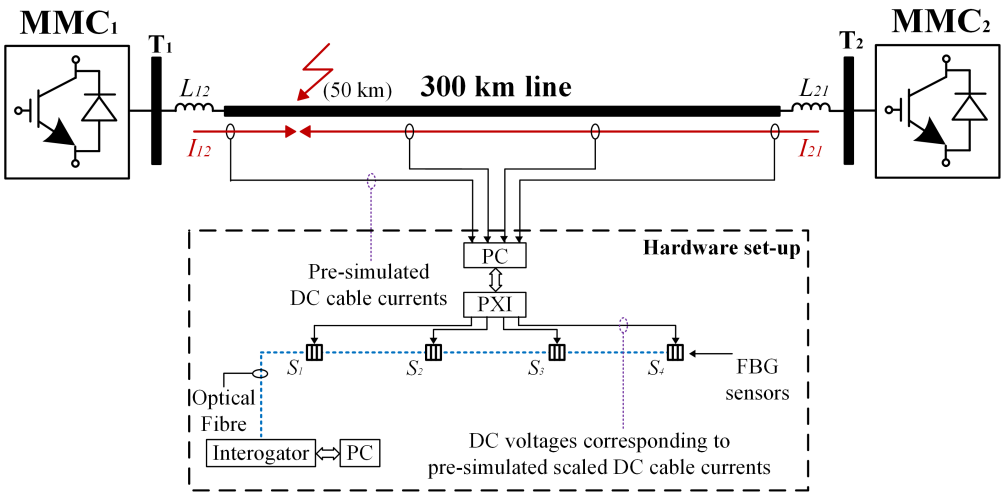


Figure 5.21: FBG model setup.

To simplify the experimental circuitry, FBG optical voltage sensors were used instead of current sensors. The FBGs were optically connected to a commercial SmartScan interrogator (Smart Fibres) offering a scanning speed of 2.5 kHz over a spectral range of 1528-1568 nm. To increase the scanning speed, the device's maximum wavelength range was narrowed to 1538-1558 nm and the optical signals reflected from the sensors were acquired at a frequency of 5 kHz. A PXIe-8106 controller and a 16-bit PXIe-6259 data acquisition card (both from National Instruments) were used for generating signals utilised for driving the voltage sensors. The card offers 16 analogue inputs that can be scanned at a maximum sampling rate of 1.25 MS/s and 4 analogue outputs with a maximum update rate of 2.8 MS/s. The maximum DC voltage range for the input and output channels is $\pm 10\ V$

To protect the piezoelectric component from depolarization and degradation due to over-voltage conditions, a transient voltage suppression (TVS) diode was connected between the component terminals (not shown in Figure 5.20) [224].

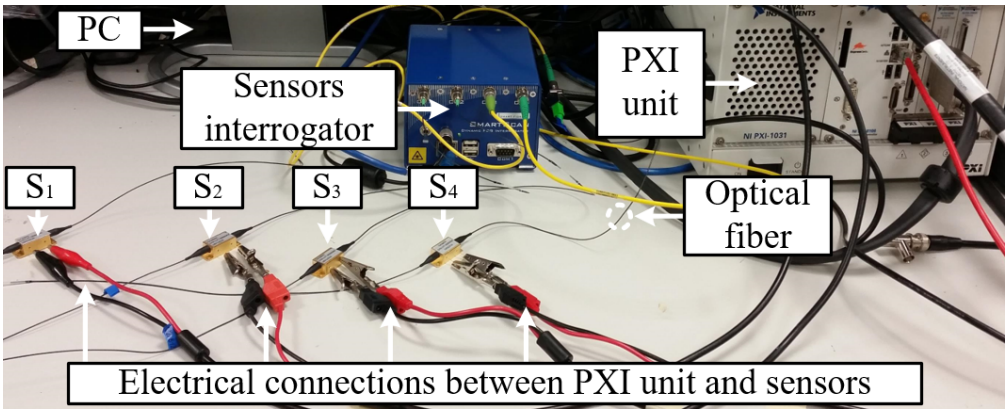


Figure 5.22: Actual experimental arrangement.

Prior to testing, the low-voltage sensors were characterised and calibrated. A DC voltage was applied across the piezoelectric transducers in 1 V steps within a range of ± 10 V. The FBG peak wavelengths were then recorded for all corresponding voltages. The inverted function was then used to calibrate wavelength shifts in terms of voltage. The actual experimental setup is depicted in Figure 5.22.

5.3.5.4 Experimental results

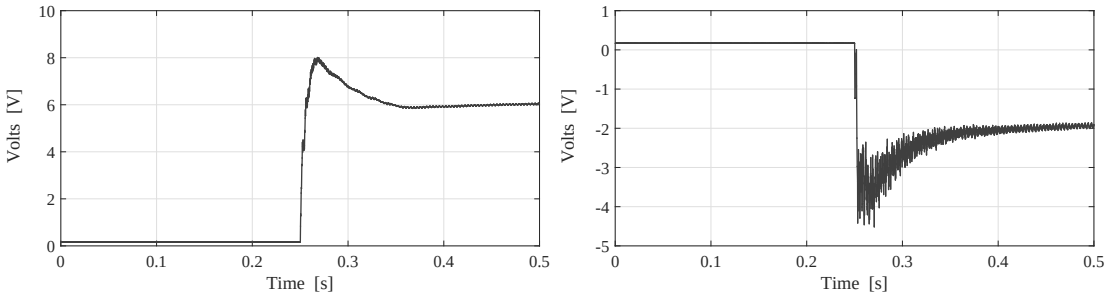
The measured response of the optical sensors and the protection system to an internal fault on a 300 km line occurring at 50 km (see Figure 5.21) is shown in Figure 5.23.

The recorded DC voltages are scaled down replicas of the DC Line currents which were pre-simulated and physically generated in real-time using a data acquisition card.

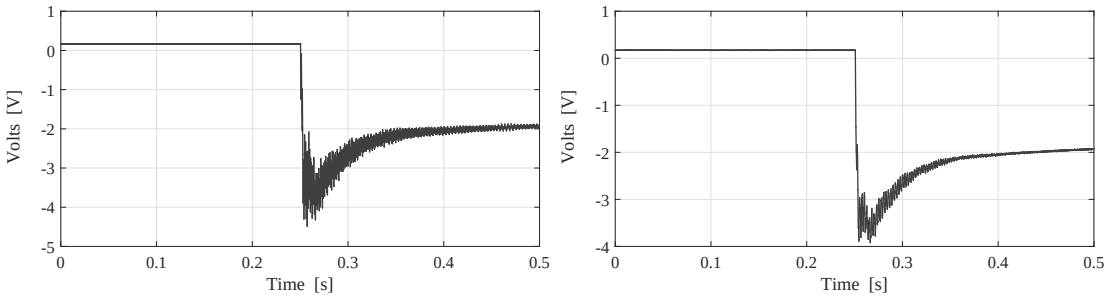
These voltage traces were physically input to the FBG optical sensors. The sampled data obtained from the optical interrogation system was stored on a PC for processing. The depicted traces represent the reflected Bragg Wavelength $\Delta\lambda_B$, individually for each sensor. Due to mechanical inertia of the sensors and other environmental conditions (e.g. temperature), the raw measured response (black solid line) of the sensor contains a significant level of noise.

For this reason, the measurements have been filtered by using Discrete Wavelet multi-resolution analysis. In particular, the measurements have been decomposed and reconstructed using a six-level tree analysis and fixed threshold de-noising. The de-noised signals are also illustrated in Figure 5.24 alongside the raw measurements. It is evident that the de-noised signals contain less high frequency components and can be used with much more confidence for high-speed protection applications.

The inverted function was used again to normalise the DC voltage in terms of shifted

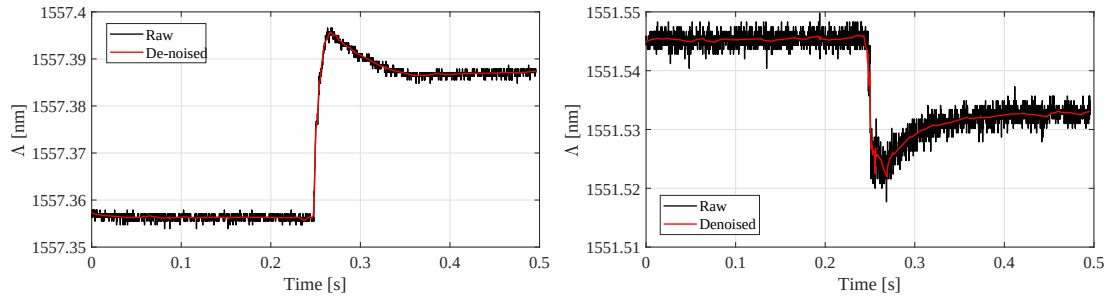


(a) Sensor S_1 (b) Sensor S_2

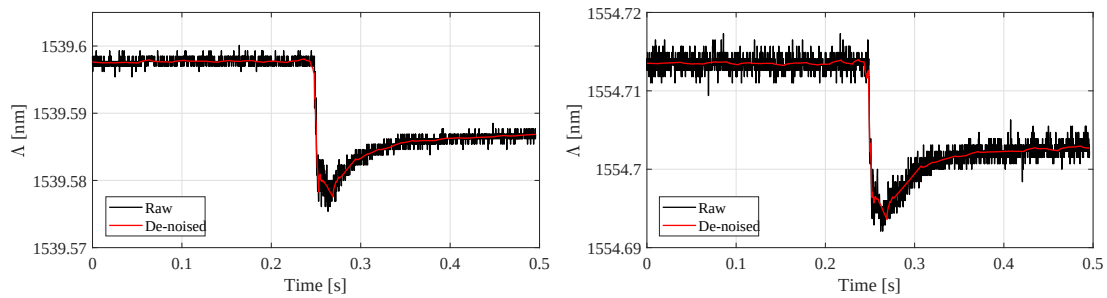


(c) Sensor S_3 (d) Sensor S_4

Figure 5.23: Voltage traces representing DC line currents at four sensing location (as per Figure 5.21).



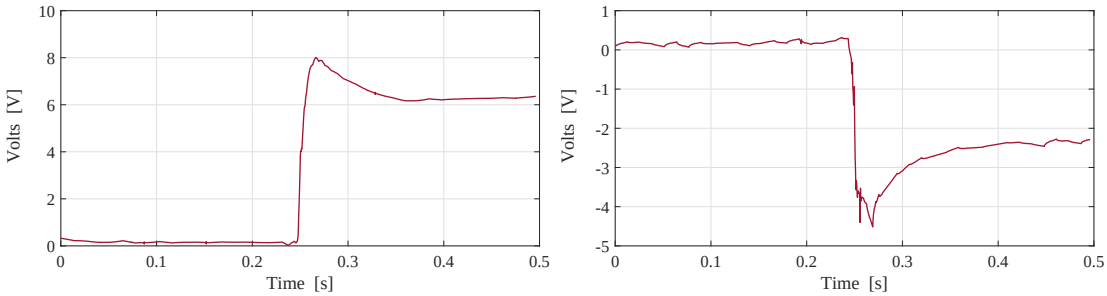
(a) Sensor S_1 (b) Sensor S_2



(c) Sensor S_3 (d) Sensor S_4

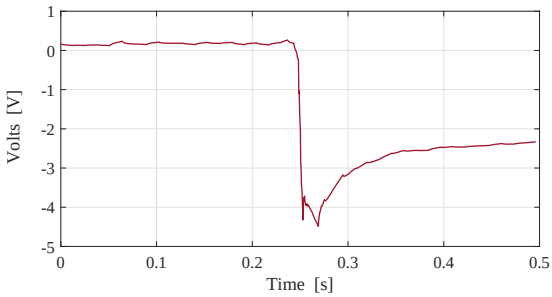
Figure 5.24: Sensors response to DC voltage traces depicted in Figure 5.23.

Bragg Wavelength $\Delta\lambda_B$. The resulting waveforms of wavelength-to-voltage conversion is illustrated in Figure 5.25 individually for each sensor. It is evident that these traces are of great resemblance with the originally-simulated (see Figure 5.23).

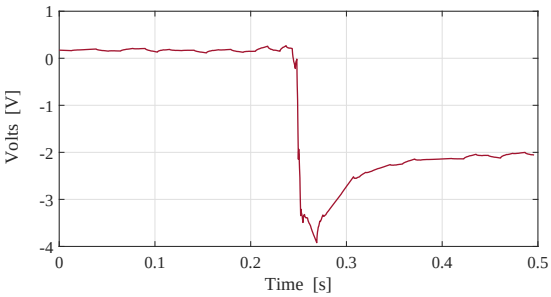


(a) Sensor S_1

(b) Sensor S_2



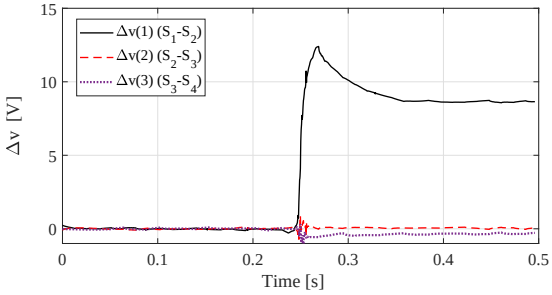
(c) Sensor S_3



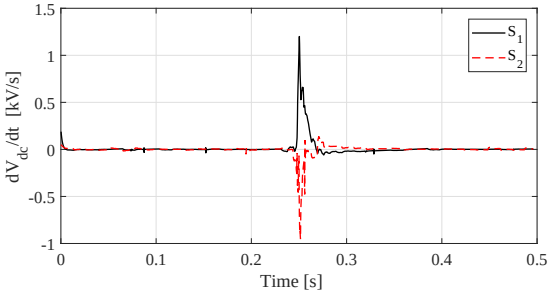
(d) Sensor S_4

Figure 5.25: Normalised DC voltages corresponding to shifted Bragg Wavelengths $\Delta\lambda_B$.

The normalised DC voltages were input on a PC for processing by the protection system algorithm developed in Simulink. As such, they have been used to calculate the differential voltage Δv, and rate of change of voltage dV_{dc}/dt, corresponding to the differential currents Δi and rate of change of current dI_{dc}/dt in the primary power system respectively. These are depicted in Figures 5.26(a) and 5.26(b) respectively.



(a) Differential voltage Δvdc



(b) Rate of change of current $dvdcdt$

Figure 5.26: Protection system recorded response.

Since the fault is physically located between sensors S_1 and S_2, it can be seen that the differential voltage derived from the measurements of these sensors S_1 and S_2 is increasing rapidly (Figure 5.26(a)). The protection threshold is exceeded; thus, the first operation criterion is fulfilled. It can also be seen in Figure 5.26(b) that prior to the fault detection the rate of change dV_{dc}/dt for both voltages (sensors S_1 and S_2) are non-zero

(Figure 5.26(b)), which indicates the satisfaction of the second criterion. Since there is no indication of a faulted sensor (i.e. differential voltage rises only for one pair of sensors), a tripping signal would be initiated.

5.3.6 Discussion

A new single-ended differential protection scheme has been described above which utilises the principle of distributed optical sensing. After the successful evaluation of the proposed scheme the following conclusions can be pointed out:

- The proposed scheme is highly sensitive, discriminative and fast both for pole-to-pole and pole-to-ground faults.
- The proposed scheme has been found to be stable during external fault occurring on adjacent lines or busbars.
- The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using a scaled-down laboratory prototype.
- The key advantages of single-ended instantaneous current measurement have been outlined which result in enhanced reliability, superior stability, and high speed of operation.
- The optical signals reflected from the sensors were acquired at a frequency of 5 kHz.
- The design, construction and operating principles of the hybrid optical sensors have been discussed with specific emphasis on the practical aspects of implementing such sensors in distributed monitoring of transmission lines.
- Excessive noise of optically-based measurements requires de-noising, which has been implemented using Wavelet multi-resolution analysis and reconstruction of the signal. Other methods could be also used (e.g. low-pass filter).

5.4 Scheme 2: Centralised Busbar Differential and Wavelet-based Line Protection

This section presents a method for discriminative detection of DC faults on VSC-powered multi-terminal HVDC transmission systems using two fundamental guiding principles: instantaneous current-differential and travelling waves. The proposed algorithm utilises local voltage and current measurements from all transmission lines connected to a DC busbar, and current measurement from the DC-side of the converter. The scheme operates at a sampling frequency of 96 kHz, which conforms with IEC 61869-9 [226]. No long distance communication is involved, while measurements and signal exchange within DC substations are enabled by the utilisation of IEC 61850 [227].

The review of existing and proposed MTDC protection techniques carried out in Section 5.2 leaves the impression that much of the reported research focuses on the conceptual aspects but neglects important practical facets such as sampling frequency, time window and breaking capacity and time response of DC interruption devices. Most importantly, there is no discussion or studies on the practical feasibility of the schemes, and the way measurements and signals exchange can be implemented locally (either on a line or busbar), within a DC substation or remotely. Taking into account the requirement of fast DC protection, all the above play a significant role in the physical implementation of any protection scheme. Accordingly, the proposed scheme is designed to detect both busbar and line faults within an MTDC grid as a centralised protection solution [228], which is compliant with IEC 61869-9 and IEC 61850. The design, practical feasibility of the scheme and case studies, have also been validated using hardware prototyping and comprehensive laboratory testing. It should also be highlighted that even though IEC 61869-9 has promoted the sampling frequency of 96 kHz for DC applications, its performance and suitability for DC protection has not been studied and reported in open literature (neither practically nor simulation-based). Consequently, another significant contribution of the present work is the utilisation and examination of IEC 61869-9 with regards to DC protection applications.

5.4.1 Protection strategy

The centralised protection scheme presented in this thesis requires voltage and current measurements from all transmission lines and the converter attached to a DC busbar as depicted in Figure 5.27.

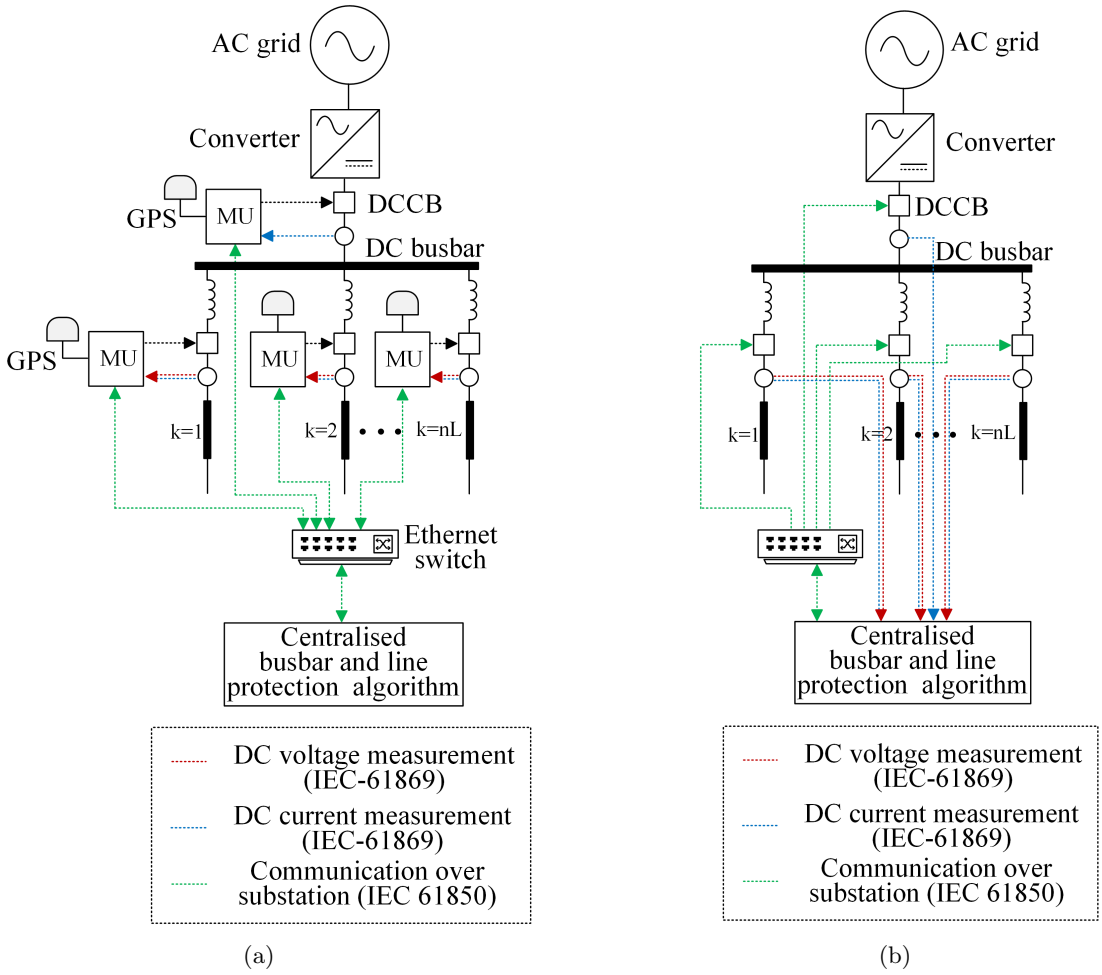


Figure 5.27: Overview of protection scheme.

There are two major options for the practical implementation of the proposed scheme. The first option (see Figure 5.27(a)) utilises Merging Units (MUs) to digitise local DC voltage and current measurements and transmit them, including a timestamp, to the centralised protection system using the IEC 61850-9-2 Sampled Value (SV) protocol. Time synchronisation is shown as being achieved using Global Positioning System (GPS) receivers, but other methods, such as using IEEE 1588 to synchronise devices over the Ethernet network, could be used instead. IEC 61850-8-1 GOOSE messaging [229] would be used to transfer tripping signals to CBs. In the second option (see Figure 5.27(b)), direct wiring of DC measurements to the centralised protection system is adopted. In

this case, GOOSE messaging and the corresponding communication infrastructure is used only for tripping signals. The first option is particularly appropriate for larger substations, where the distance between the measurement locations and the central controller prohibits the use of analogue signalling. In the work presented in this section the first option has been put forward. It should be noted that measurements are not required to be transferred between substations. Although blocking signals for internal busbar faults and trip signals for line faults could be transmitted to remote substations to improve system-wide protection coordination.

The algorithm consists of three stages as illustrated in Figure 5.28 which are explained in detail below.

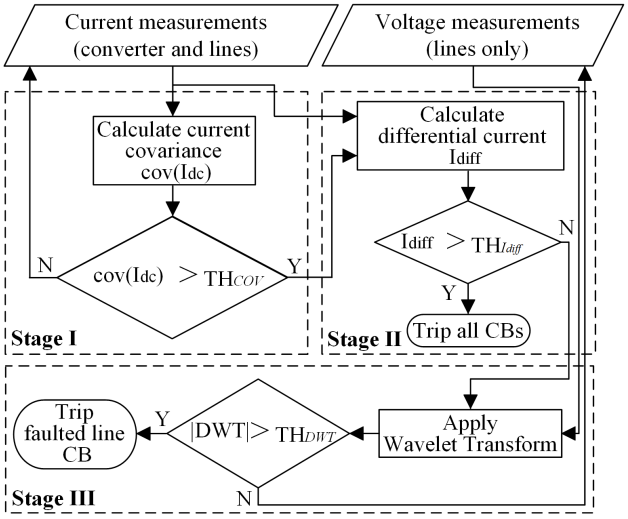


Figure 5.28: Protection algorithm.

Stage I - Fault Detection: This initial stage of operation is where the fault presence is detected using all the currents from the converter and the lines attached to the same busbar. Using a ten-sample time window as illustrated in Figure 5.29, the covariance $cov(I_{dc})$ of each current is calculated.

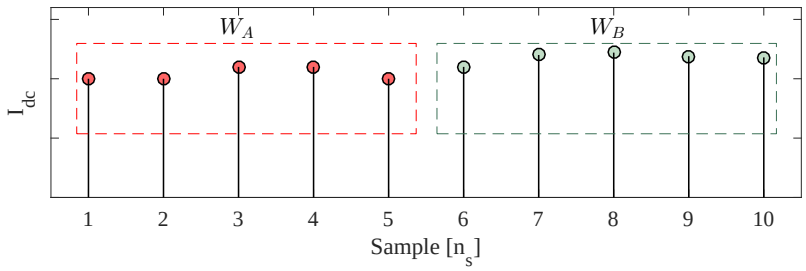


Figure 5.29: Ten-sample time window illustrating sub-windows W_A and W_B for covariance calculation.

Considering the sub-windows W_A and W_B as independent variables within the ten-sample moving window, the covariance is calculated by

$$cov(I_{dc}) = \frac{1}{n_s/2 - 1} \sum_{k=1}^{n_s/2} (W_{A,k} - \mu_{W_A}) \cdot (W_{B,k} - \mu_{W_B}) \tag{5.9}$$

where n_s is the number of samples, $W_{A,k}$ and $W_{B,k}$ are the covariance variables (i.e. samples included in sub-windows W_A and W_B), μ_{W_A} and μ_{W_B} are the mean values of sub-windows W_A and W_B respectively.

Covariance is a measure of change in one variable ($W_{A,k}$) with respect to a second variable ($W_{B,k}$). Consequently, a significant change in current (I_{dc}) (which can be a potential fault case) can be detected.

The fault detection is achieved by comparing $cov(I_{dc})$ of every current (i.e. converter and line currents) with a predefined threshold TH_{COV}. If any of these covariance values exceed this threshold, a fault is assumed to be present and the algorithm proceeds to Stage II. It should be noted that covariance is calculated using a fixed length ten-sample window, moving in one-sample intervals. Due to its averaging effect, any short spike (i.e. in one or two current samples) would not indicate a fault. This provides additional level of security when it comes to Stage II (differential protection) as the covariance-based indicator provides an enabling signal for the differential element.

Stage II - Busbar Fault Detection: In this stage the protection algorithm determines whether the fault is on the busbar or on one of the lines. This is achieved by calculating the differential current I_{diff} by utilising converter and line current measurements, giving

$$I_{diff} = \sum_{k=1}^{n_L} (I_{dc-Line,k} + I_{dc-Conv}) \tag{5.10}$$

where n_L is the number of the lines connected to the busbar (as also shown in Figure 5.27), $I_{dc-Line,k}$ is the current in line k and $I_{dc-Conv}$ is the converter output current. During line faults, the locally-calculated busbar differential current is expected to be theoretically close to zero, while for busbar faults it should obviously reach high values. The presence of a busbar fault is perceived by comparing the differential current with a threshold $TH_{I_{diff}}$. If such threshold is exceeded, then a busbar fault is deemed to exist and all CBs connected to the busbar will be tripped and the algorithm will terminate at

this point. As also shown in Figure 5.28 if a such threshold is not exceeded, the algorithm proceeds to Stage III, considering that the fault is present on one of the connected lines.

Stage III - Faulted Line Selection: This is the final stage of the protection algorithm where the faulted line(s) are detected by observing travelling waves on the voltage measurements. This is achieved by applying DWT to voltage waveforms captured on the line side of the current-limiting inductor (for each line separately).

The wavelet transform of a function $v(t)$ can be expressed as the integral of the product of $v(t)$ and the daughter wavelet $\Psi^*_{a,b}(t)$ as

$$W_\psi v(t) = \int_{-\infty}^{\infty} v(t) \quad \underbrace{\frac{1}{\sqrt{\alpha}}\Psi\left(\frac{t-b}{a}\right)}_{\text{daughter wavelet } \Psi^*_{a,b}(t)} \quad dt \tag{5.11}$$

The daughter wavelet $\Psi^*_{a,b}(t)$ is a scaled and shifted version of the mother wavelet $\Psi_{a,b}(t)$. Scaling is implemented by α which is the binary dilation (also known as scaling factor) and shifted by b which is the binary position (also known as shifting or translation).

Two categories of wavelet transform can be distinguished: Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT). The difference lies upon the resolution of binary dilation α and binary position b. In DWT they move discretely in dyadic blocks. Specifically, α and b, can only take values of the power of two as expressed by

$$\alpha_L = 2^L, \ (\alpha_0 = 2^0 = 1, \alpha_1 = 2^1 = 2, ...) \tag{5.12}$$

$$b_L = 2^L N, \ (b_0 = 2^L 0 = 0, b_1 = 2^L 1 = 2^L, ...) \tag{5.13}$$

where L is the level of decomposition and N is the sample index.

The selection between CWT and DWT is a trade-off between time accuracy of the wave detection, and processing resources and their associated time delays [189]. In the case of CWT, the daughter wavelet can be positioned smoothly over the signal; hence, the accuracy of the wave time detection is better than for DWT techniques. This is the reason that CWT is preferred for fault location applications [190], where the computational time is not crucial. However, DWT is computationally more efficient [189], which enables faster wave detection. As a result, DWT is considered more suitable for power system protection applications [191], and therefore, DWT is the chosen technique.

The key to discrimination of the faulted line lies in the inductive termination of each line. The placement of inductors not only results in the reduction of the rate of rise of fault current, but also mean that voltage waveforms and their DWT contain very distinctive features (also demonstrated in Sections 4.2.2 and 4.4.4). When a fault occurs on one of the busbar-connected lines, the voltage measured at the line side of the inductor will be subjected to a severe depression and hence the DWT is expected to reveal sharp edges and possess high magnitude. For the same fault, the voltage change measured on the healthy lines is expected to be more gradual due to the inductances included in the fault current path from one healthy line, through the busbar, to the faulted line. As a result, travelling waves calculated using DWT will be attenuated both in sharpness and magnitude compared to those on the faulted line. Such differences allow for a reliable discrimination of the faulted lines. In particular, a faulted line is identified by comparing the calculated DWT magnitude with a predefined threshold TH_{DWT}. Once such threshold is exceeded, a tripping signal is sent to the corresponding CB.

5.4.2 Selecting thresholds and Wavelet

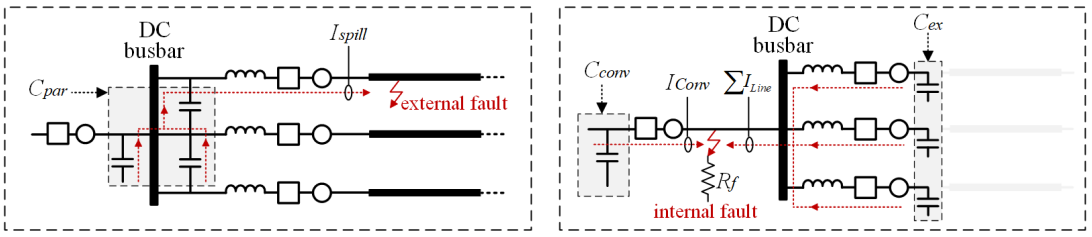
As described in the previous subsections, the sensitivity and stability of the proposed scheme depends on the three thresholds TH_{COV}, $TH_{I_{diff}}$ and TH_{DWT}, for covariance, differential current and DWT respectively. This section elaborates on the procedure of selecting appropriate values for these thresholds.

Firstly, regarding the covariance threshold TH_{COV}, the following formula has been used:

$$TH_{COV} \leq \frac{C_{min} \cdot dV_{cap}^{min}}{t_s \cdot n_s^2} \tag{5.14}$$

where C_{min} is the minimum capacitance expected to discharge during the fault, dV_{cap}^{min} is the expected minimum voltage drop across the capacitance C_{min}, t_s is the sampling frequency, and n_s is the number of samples used in covariance calculation.

Equation (5.14) has been derived based on the fact that a capacitive current (generated by the discharge of the minimum capacitance C_{min}) should be captured within the time window used for covariance calculation (i.e. $n_s = 10$ samples). The average value of such discharging current over the time window sets the maximum value of TH_{COV} and ensures that in case of any fault, the resulting covariance $cov(I_{dc})$ will exceed TH_{COV}.



(a) Spill current during external line fault (b) Fault currents during internal busbar fault

Figure 5.30: Illustration of faults currents for threshold selection.

For explaining the procedure of selecting the threshold $TH_{I_{diff}}$, the circuits depicted in Figure 5.30 are utilised. For the differential protection to operate correctly, two main criteria should be fulfilled. Firstly, for protection security purposes the threshold $TH_{I_{diff}}$ needs to be higher than the spill current I_{spill} generated during external faults. As illustrated in Figure 5.30(a), a spill current I_{spill} is produced by the discharge of combined shunt parasitic capacitance C_{par} during external line faults. This capacitance is formed between the live conductors, includes additional lumped circuits (e.g. resistive-capacitive DC voltage transformers), and any other capacitance formed between the substation components and earth. The spill current I_{spill} can be approximated as

$$I_{spill} = C_{par}\frac{dV_{C_{par}}}{dt} \tag{5.15}$$

where $dV_{C_{par}}/dt$ is the expected (or estimated) maximum value of the rate-of-change of voltage across the shunt capacitance C_{par}.

Secondly, to ensure differential protection dependability, the directed sum of all busbar currents (i.e. the differential current) should be higher than $TH_{I_{diff}}$, even for the worst case highly-resistive faults. For the first ms of the fault, a high burst differential current is formed by the discharge of capacitance C_{conv} and C_{ext} as illustrated in Figure 5.30(b). The term C_{conv} represents the equivalent capacitance of the converter and C_{ext} is the total external capacitance of the neighbouring feeders. The algebraic sum of all busbar currents can be estimated as

$$\sum I_{Line} + I_{Conv} = C_{par}\frac{dV_{C_{conv}}}{dt} + C_{ext}\frac{dV_{C_{ext}}}{dt} \tag{5.16}$$

where $dV_{C_{conv}}/dt$ and $dV_{C_{ext}}/dt$ are the expected (or estimated) minimum rate-of-change of voltage across the converter and external capacitance C_{conv} and C_{ext} respectively.

Taking into account the above analysis for internal and external faults together with

the associated equations (5.15) and (5.16), the following formula (5.17) sets the range of acceptable values for $TH_{I_{diff}}$:

$$k_{sf} \cdot I_{spill} < TH_{I_{diff}} < \left(\sum I_{Line} + I_{Conv} \right) \tag{5.17}$$

It can seen that spill current is multiplied by a safety factor k_{sf} to reduce the possibility of spurious tripping. The selection of thresholds for covariance and differential current depends on the approximation of capacitive currents during the first ms of the fault. This is due to the fact that the proposed scheme is designed as a primary protection system and hence high speed of operation is required. The analysis requires the expected or estimated rate-of-change of voltage on capacitive elements which should take into consideration highly resistive pole-to-ground faults as explained in [230].

Regarding the selection of thresholds related to DWT, the following impedances need to be estimated: i) impedance seen from the point of measurement to the remote end of the protected line, and ii) impedance seen from the point of measurement to the nearest point outside the protected line. The analysis should include the highest considered fault resistance R_f, as it will affect the resulting amplitude of travelling waves. The estimated impedance can be used to calculate the corresponding transfer function with regards to voltage. The frequency response of each transfer function should provide sufficient margin for successful internal/external fault discrimination. As the lines are terminated by lumped inductors (with inductance being much higher than that of the lines) there is a significant attenuation boundary for high frequency travelling waves resulting from external faults. For further insight on the selection of DWT related thresholds the literature in [191, 231] provides a useful guidance.

5.4.3 Measurement and communications delays within DC substation

It is important to ensure that the proposed method will operate correctly, despite delays from a realistic implementation. Assuming the use of MUs as illustrated in Figure 5.27, the maximum delay, t_d, to be expected from the measurement and communications can be calculated as

$$t_d = t_s + t_{MU} + t_n + t_{cc} \tag{5.18}$$

where t_s is the maximum delay due to analogue sampling (i.e. $t_s = 1/96$ kHz$= 10.42\mu s$),

t_{MU} is the processing time in the MU (i.e. the time to encode the SV frame), t_n is the total maximum Ethernet network latency, and t_{cc} is the processing time for the central controller (i.e. the time to decode the SV frame).

The size of the SV Ethernet frame would be 64 bytes (the minimum frame size) because a maximum of two DC values are digitised within the dataset which would require only 58 bytes, including overhead and quality values [232]. As suggested by IEC 61869-9, a dedicated 1 Gbps Ethernet network is assumed, and therefore t_n is composed of the data transmission time for two Ethernet links (i.e. $2 \times 0.7\mu s$), the switch processing delay (assumed to be 1 μs), and jitter associated with queuing due to other traffic. These could include IEEE 1588 frames and data from other measurement locations; assuming a maximum of four simultaneous competing frames and a transmission delay of 0.58 μs per frame [233], the maximum queuing delay is $4 \times 0.58\mu s$. t_{MU} and t_{CC} can be estimated as 12 μs and 9.5 μs, respectively, based on the measurements in [234] for approximately double the frame size, but this depends on the performance of the platform. Combining all of these factors, the worst case delay can be calculated as

$$t_d = 10.42 + 12 + (1.4 + 1 + 4 \times 0.58) + 9.5 = 36.64 \ \mu s \tag{5.19}$$

Further delays are introduced by the protection system and they arise from the window-based processing required by the covariance calculation and DWT. Time delay t_{df} associated with the window-based processing is given by

$$t_{df} = (N_W - N_{WO}) \cdot t_{si} \tag{5.20}$$

where N_W is the length of the processing window in samples, N_{WO} is the amount of window overlap between two consecutive calculations frames, and t_{si} the sampling period of the input signal. Since a ten-sample time window has been used with a nine-sample overlap, and considering 96 kHz as the sampling frequency, the total time delay t_{df} is 10.42 μs. It should be highlighted that since the DWT and covariance use different processing windows which run in parallel, there is no additional queuing of the voltage and currents measurements. As such, the value 10.42 μs is not subjected to any additional delays.

5.4.4 Modelling

For the purposes of validating the proposed protection scheme, a model of a five-terminal HVDC grid illustrated in Figure 5.31 has been developed. The network architecture is an enhanced version of a network from the Twenties Project case study on DC grids [163]. There are five modular multi-level converters (MMCs) in the network operating at ±400 kV (in symmetric monopole configuration), current-limiting inductors and HbCBs.

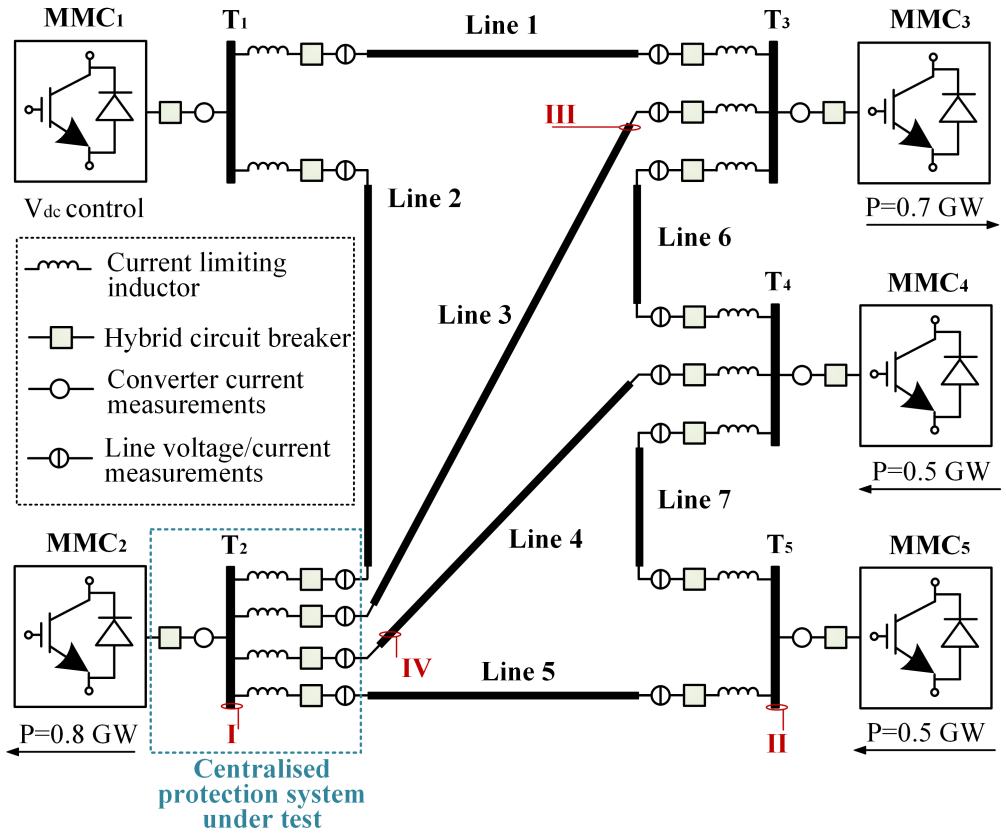


Figure 5.31: MTDC case study grid.

The MMC models are identical to those used in [36] and the AC-DC network parameters are presented in Table 5.7. The lines have been modelled using a distributed parameter model. The HbCB is modelled by adopting a hybrid concept by ABB as reported in [82] (2 ms operation time with a maximum breaking current of 9 kA).

5.4.5 Simulations results

5.4.5.1 Fault scenarios

This section presents simulation results which quantify the overall performance of the proposed protection scheme under different fault scenarios, including pole-to-pole faults,

Table 5.7: DC and AC Network Parameters.

Parameter	**Value**
DC voltage [kV]	± 400
DC inductor [mH]	150
Line resistance [Ω/km]	0.015
Line inductance [mH/km]	0.96
Line capacitance [μF/km]	0.012
Line lengths (1 to 7) [km]	300, 200, 600, 180, 150, 120, 100
AC frequency [Hz]	50
AC short circuit level [GVA]	40
AC voltage [kV]	400
MMC levels	401
MMC arm inductance [p.u.]	0.1
MMC equivalent arm capacitance [μF]	20.84

pole-to-ground faults (incorporating highly resistive faults) and busbar faults. In all scenarios the faults are permanent and are triggered at $t = 0.5$ ms. In all cases, the measurements have been contaminated with white noise to account for possible effects due to measurement-related noise on the protection response.

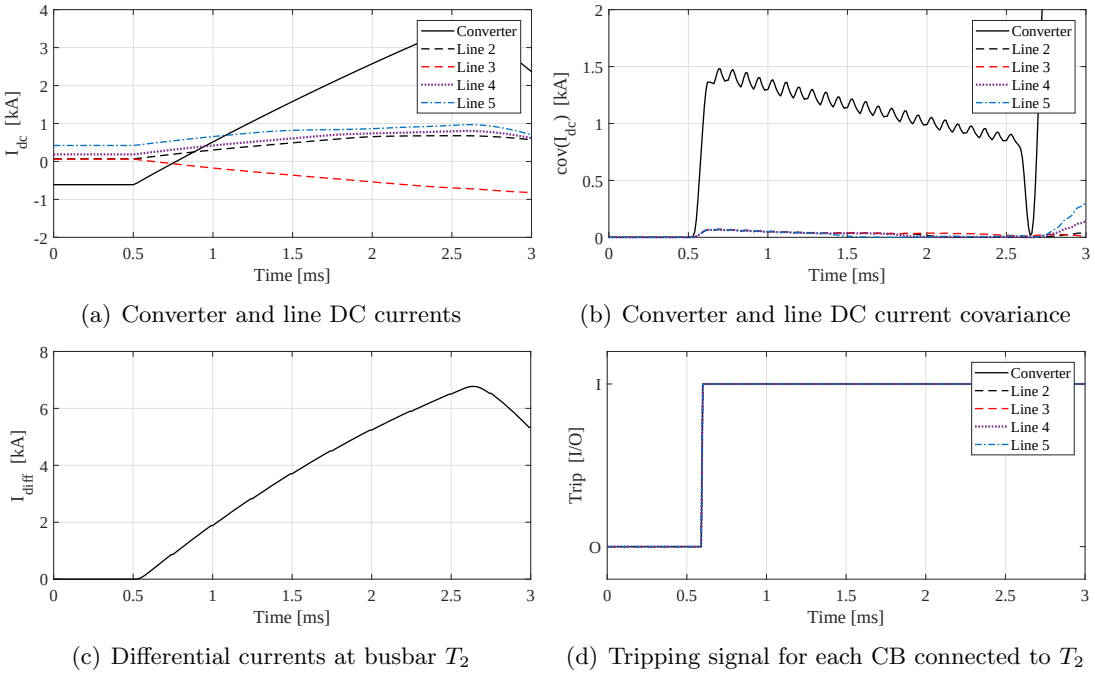
Table 5.8: Description of fault scenarios.

Scenario	Description	Classification
I	Pole-to-pole fault at busbar T_2 ($R_f \approx 0\ \Omega$)	Solid, busbar, internal
II	Pole-to-pole fault at busbar T_5 ($R_f \approx 0\ \Omega$)	Solid, busbar, external
III	Pole-to-ground fault at Line 3 (590 km from T_2, $R_f = 500\ \Omega$)	Highly-resistive, remote internal
IV	Pole-to-pole fault at Line 4 (5 km from T_2, $R_f \approx 0\ \Omega$)	Solid, close-up, internal

It is assumed that the assessed protection scheme is placed at terminal T_2. A selection of representative test cases have been included here (summarised in Table 5.8 and also depicted on Figure 5.31) which demonstrate the worst case scenarios in terms of stability and sensitivity of the scheme. Scenario I is included to illustrate the ability to detect and isolate internal busbar faults. The most challenging for line protection are the fault scenarios which include a solid external fault at the end of the shortest line (Scenario II - stability test), and an internal far-end high impedance fault on the longest line (Scenario III - sensitivity test). An additional close-up fault (scenario IV) has been added to test the performance and speed of the proposed scheme. Moreover this scenario has been repeated under different sampling frequencies to investigate its impact on the protection performance.

5.4.5.2 Fault scenario I

This fault scenario illustrates the protection performance under a busbar fault triggered at $t_{fault} = 0.5$ ms.



(a) Converter and line DC currents

(b) Converter and line DC current covariance

(c) Differential currents at busbar T_2

(d) Tripping signal for each CB connected to T_2

Figure 5.32: Response of T_2 protection system to fault scenario I.

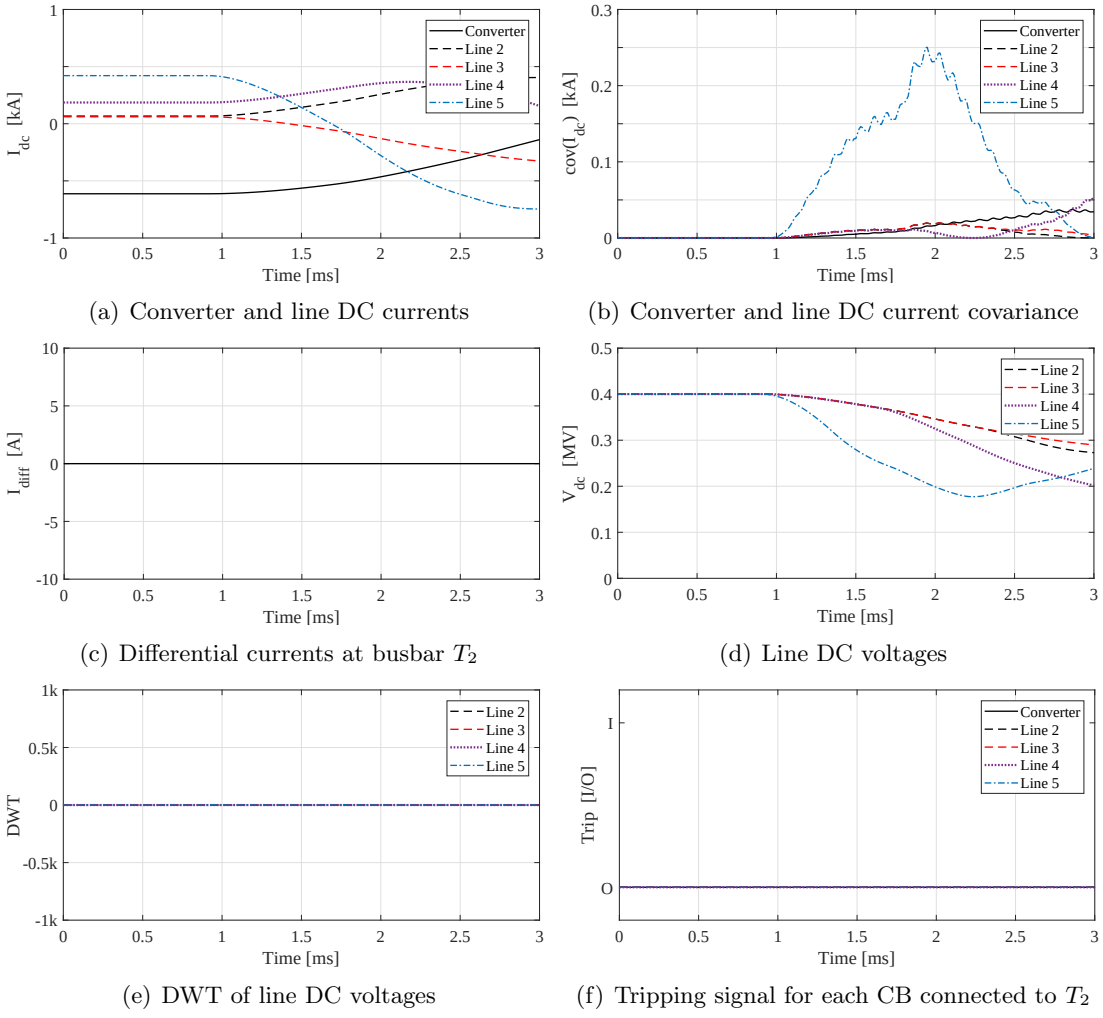
Figure 5.32(a) shows that immediately after the fault there is a rapid increase in the current from the converter. This is due to the discharge of the capacitance in the converter's sub-modules (prior to IGBT blocking). There is also a current infeed from the connected lines (Lines 2, 3, 4 and 5), but their rate of rise is limited due to the inductive terminations. As a result, there is a rapid increase in current covariance $cov(I_{dc})$ (Figure 5.32(b)), which satisfies Stage I (fault detection) of the protection algorithm.

The rapid increase in current infeed from both the converter and from the lines, results in the rapid rise of differential current I_{diff} as shown in Figure 5.32(c). This satisfies Stage II (busbar fault detection) of the protection algorithm and is followed by the tripping of all the HbCBs (Figure 5.32(d)), after which the algorithm terminates.

5.4.5.3 Fault scenario II

This fault scenario is designed to demonstrate the stability of the protection system during external faults (i.e. faults on remote lines or busbars). A solid external fault at the remote end of the shortest line (i.e. Line 5: 150 km) is applied on terminal T_5. The

performance of the protection system located at terminal T_2 is depicted in Figure 5.33.



(a) Converter and line DC currents

(b) Converter and line DC current covariance

(c) Differential currents at busbar T_2

(d) Line DC voltages

(e) DWT of line DC voltages

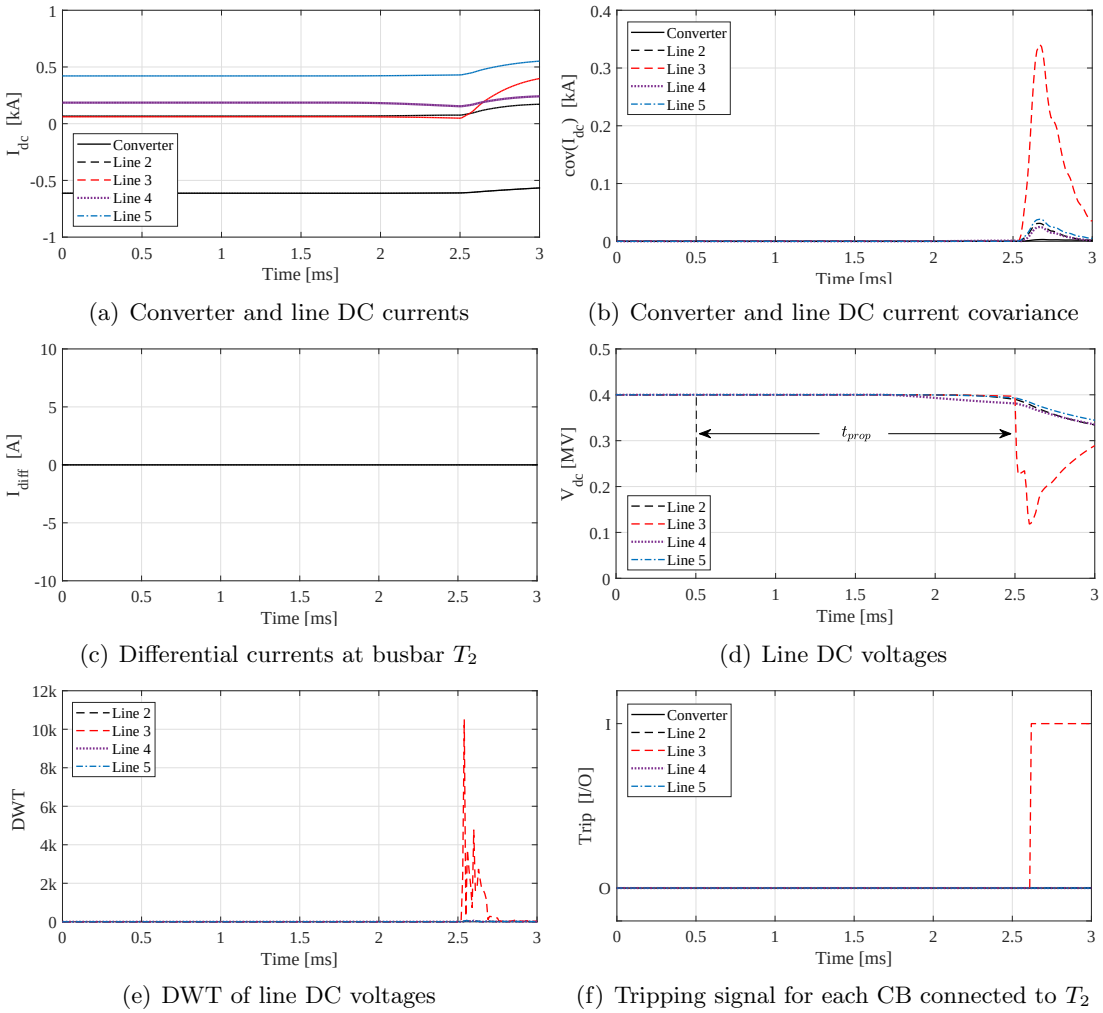
(f) Tripping signal for each CB connected to T_2

Figure 5.33: Response of T_2 protection system to fault scenario II.

Approximately 0.7 ms after the fault occurrence at $t_{fault} = 0.5$ ms (which corresponds to the propagation delay along Line 5), a change in the DC currents can be observed both in the converter output and the lines (Figure 5.33(a)). This results in an increase in covariance (Figure 5.33(b)), especially for Line 5. This satisfies the Stage I criterion and the algorithm will proceed to Stage II (busbar fault detection). As expected, the differential current I_{diff} (Figure 5.33(c)) remains at an extremely low level; consequently the algorithm will proceed to Stage III (line fault detection). As illustrated in Figure 5.33(e), there is no visible transient observed in DWT magnitude. As the voltage change is measured on the healthy lines the DWT is extremely attenuated both in sharpness and magnitude. Therefore, there is no tripping signal initiated for any of the CBs at terminal T_2 (Figure 5.33(f)), i.e. the scheme is stable during this worst case external fault.

5.4.5.4 Fault scenario III

In this scenario, the sensitivity and discrimination of the protection scheme is demonstrated. As shown in Figure 5.34 after the fault occurrence at $t_{fault} = 0.5$ ms, there is a current increase from the converter but also from the lines (Figure 5.34(a)).



(a) Converter and line DC currents

(b) Converter and line DC current covariance

(c) Differential currents at busbar T_2

(d) Line DC voltages

(e) DWT of line DC voltages

(f) Tripping signal for each CB connected to T_2

Figure 5.34: Response of T_2 protection system to fault scenario III.

Similarly, due to the inductive terminations, the rate of rise of current in the healthy lines is limited. Moreover, it can be noted that there is a time delay t_{prop} corresponding to the electromagnetic propagation speed and distance to the fault on Line 3. After approximately 2 ms, the covariance value $cov(I_{dc})$ of the currents (especially from Line 3) increase to high values and the criterion of Stage I is satisfied.

The algorithm proceeds to Stage II where the differential current I_{diff} is calculated. It is evident from Figure 5.34(c) that there is no busbar fault detected, since the values of differential current I_{diff} remain close to zero. Consequently, the algorithm proceeds to

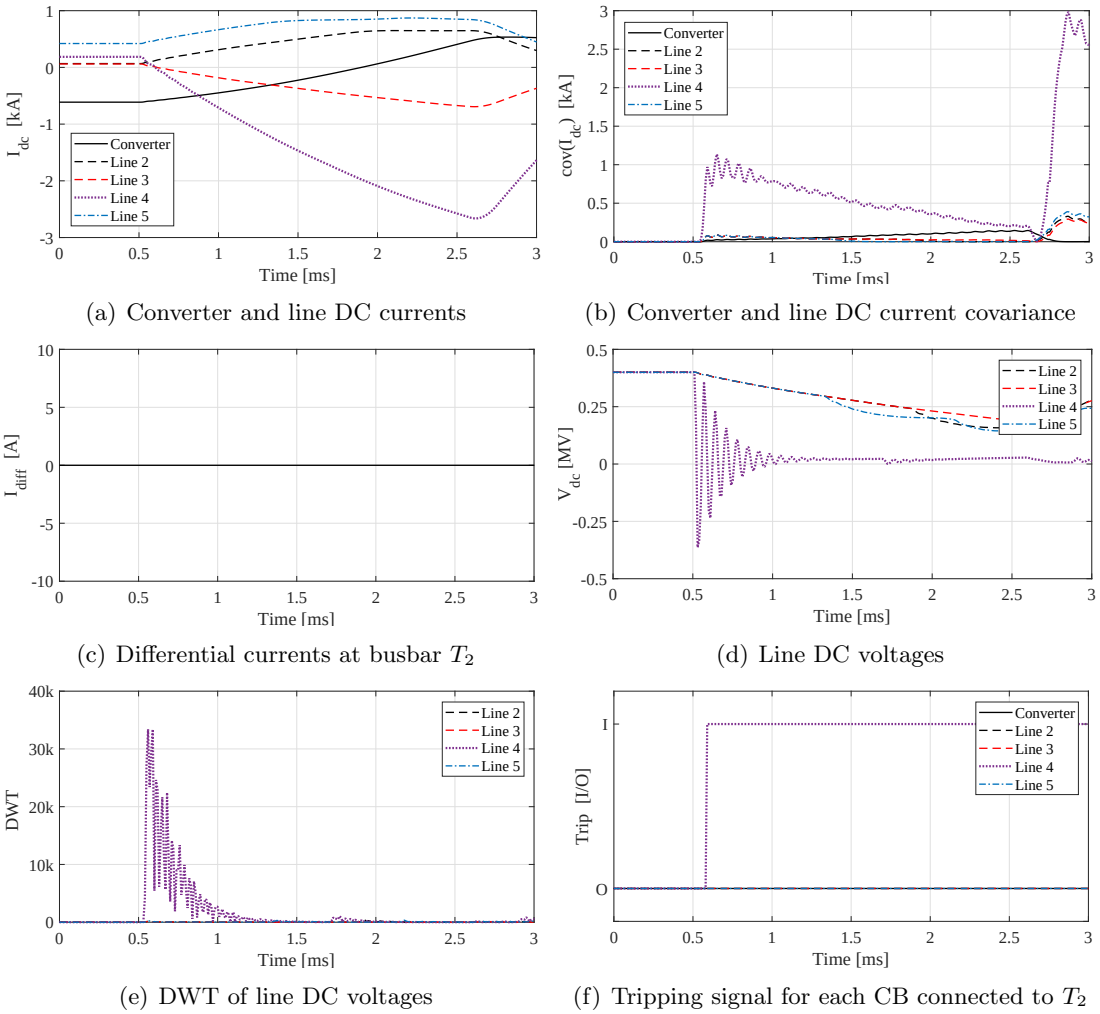
Stage III considering the presence of a line fault. As can be seen in Figure 5.34(d), the voltage of the faulted line (i.e. Line 3) shows a relatively steeper transient phenomena (i.e. travelling wave). Such transients cannot be seen in the healthy lines for two reasons: first, transients are attenuated by inductive terminations; second, voltages are captured on the line-side of the current-limiting inductors. The difference becomes more pronounced when the DWT is executed as shown in Figure 5.34(e). It is evident that the faulted line can be discriminated using the magnitude of DWT, as its value is three orders of magnitude greater than those obtained from the healthy lines. This results in selective tripping of the HbCB corresponding to the faulted line as can be seen in Figure 5.34(f).

5.4.5.5 Fault scenario IV

This scenario aims to test the ability of the protection scheme to simultaneously detect quickly close-up faults while maintaining its discrimination. As illustrated in Figure 5.35 immediately after the fault occurrence at $t_{fault} = 0.5$ ms, there is a current increase from the converter but also from the lines (Figure 5.35(a)), especially from Line 4. After approximately 0.07 ms, the covariance value $cov(I_{dc})$ of the currents (especially from Line 4) increase to high values and the criterion of Stage I is satisfied. Again, due to the inductive terminations, both the rate of rise of current and covariance in the healthy lines is limited.

The algorithm proceeds to Stage II where the differential current I_{diff} is calculated. It is evident from Figure 5.35(c) that there is no busbar fault detected, since the values of differential current I_{diff} remain close to zero. Consequently, the algorithm proceeds to Stage III considering the presence of a line fault.

As can be seen in Figure 5.35(d), the voltage of the faulted line (i.e. Line 3) experiences high depression followed by steep and high frequency transients. Such transients are not present in the healthy lines, since they are attenuated by the inductive terminations, and due to the fact that the voltages are captured on the line-side of the current-limiting inductors. The difference becomes more distinct when the DWT is applied as shown in Figure 5.35(e). This results in satisfaction of Stage III and selective tripping of the HbCB corresponding to Line 4 as can be seen in Figure 5.35(f).



(a) Converter and line DC currents

(b) Converter and line DC current covariance

(c) Differential currents at busbar T_2

(d) Line DC voltages

(e) DWT of line DC voltages

(f) Tripping signal for each CB connected to T_2

Figure 5.35: Response of T_2 protection system to fault scenario IV.

5.4.5.6 Impact of sampling frequency

In order to investigate the impact of sampling frequency on the protection performance, fault scenario IV has been repeated for different sampling frequencies. The summary of the protection response is presented in Table 5.9.

It is evident that below 60 kHz protection has failed to operate correctly due to the failure of Stage III (faulted line discrimination). Even though smaller sampling frequencies can successfully pass Stage I (fault detection) and Stage II (busbar fault detection), there is a difficulty on travelling wave-based analysis for fault discrimination. The correct discriminative operation of the proposed scheme relies on the correct, accurate and fast detection of travelling waves which evidently requires an adequate sampling frequency. Consequently, the recommendation of 96 kHz in IEC-61869 provides enough confidence for the correct and fast detection of transient phenomena in DC systems.

Table 5.9: Impact of sampling frequency on protection performance.

f_s [kHz]	1	5	10	20	50	60	70	80	96	100	200
Correct operation	N	N	N	N	N	Y	Y	Y	Y	Y	Y
Stage I	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Stage II	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Stage III	Fail	Fail	Pass	Fail	Fail	Pass	Pass	Pass	Pass	Pass	Pass

5.4.6 Hardware validation

5.4.6.1 Experimental arrangement

A real-time hardware prototype has been developed in order to validate the practical implementation of the proposed scheme. For such development the Opal-RT OP5600 HILBOX has been utilised, integrating digital-analogue I/O and GPS cards.

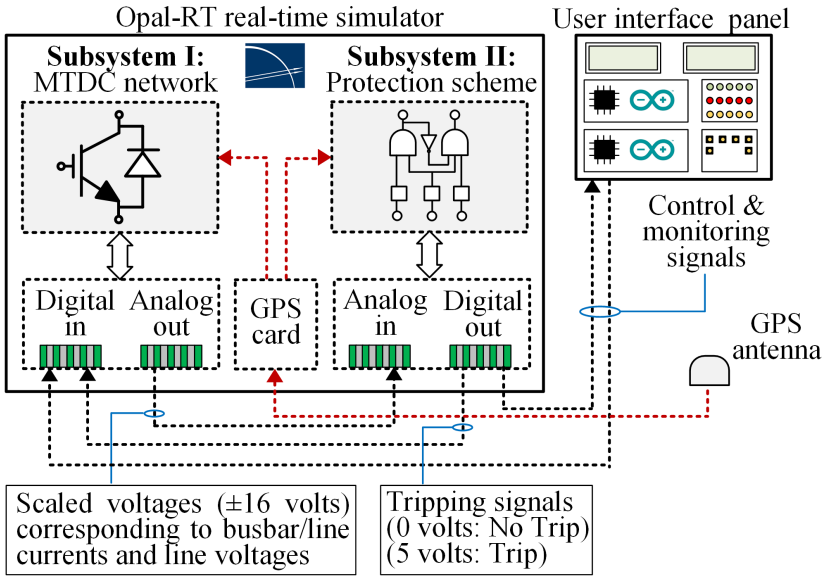


Figure 5.36: Experimental arrangement.

As illustrated in Figure 5.36, the entire system is divided into two subsystems, one for the MTDC test network and one for the protection scheme algorithm. The input signals to the protection scheme are current and voltage signals (both converted to proportional voltages) recorded from the MTDC network simulation. Time synchronisation of the measurements is implemented through a GPS TSync-PCIe card. All inputs have been scaled-down to remain within the safe operating range of the I/O cards (±16 volts). Consequently, all the protection thresholds have been scaled-down accordingly. The analogue inputs are sampled at 96 kHz as per IEC 61869-9.

Communication and measurement delays within DC substation have been emulated

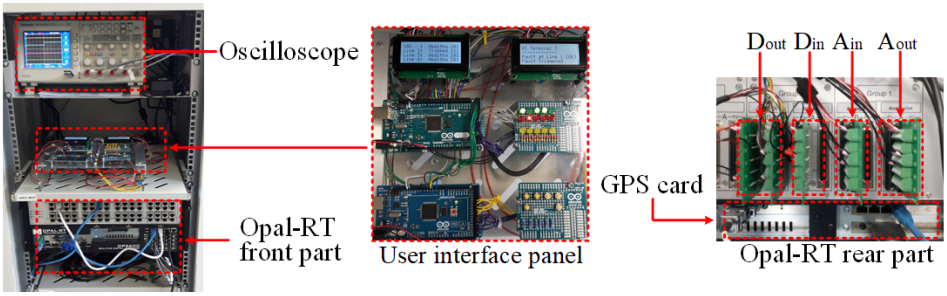


Figure 5.37: Photo of experimental setup.

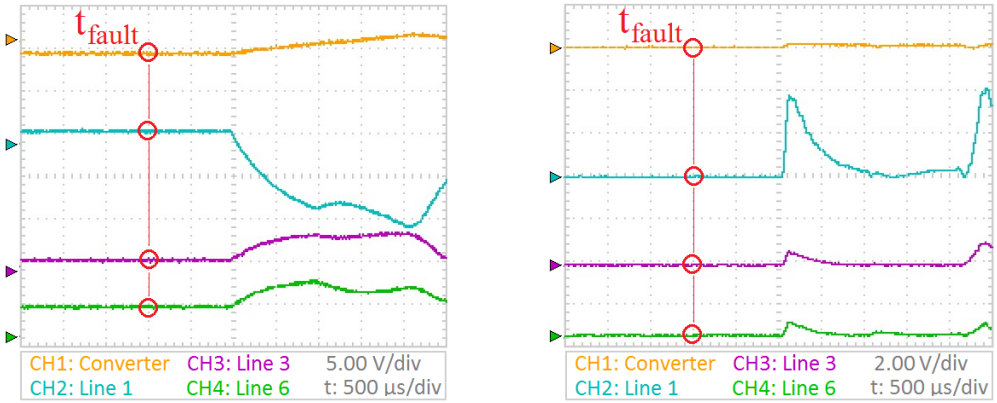
taking into account equation (5.18) and hence a physical Ethernet switch and merging units has not been used. There is also a user interface panel, from which the user can monitor and control the simulation. Specifically the user can trigger or reset the fault scenarios or monitor the tripping status of the protection system and CBs. As illustrated in Figure 5.37, the user interface panel consists of micro-controllers (2 x Arduino Mega 2560), LED and button panels, and alphanumeric LCD screens.

5.4.6.2 Experimental results

For the experimental validation of the proposed scheme a pole-to-pole in the middle of Line 1 is utilised. Due to the limited number of channels of the available oscilloscope, the results are presented considering the operation of the protection system placed at terminal T_3.

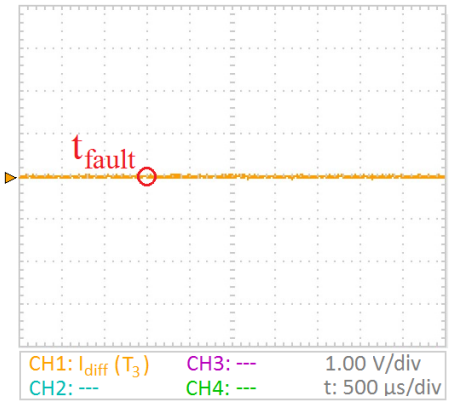
In Figure 5.38, the results are presented as captured during real-time simulation of the aforementioned fault, triggered at $t_{fault} = 1.5$ ms. Following the fault, there is a DC current infeed from the converter and the Lines 1, 3 and 6 (Figure 5.38(b)), which in turn results in the increased covariance values (Figure 5.38(b)) enabling protection Stage I. Since there is no change in the differential current (Figure 5.38(c)) the algorithm proceeds to Stage III. As shown in Figure 5.38(d), the DC voltage of the faulted line (i.e Line 1) reveals steep changes, while for the healthy lines there is a much smoother transition. As a result, the DWT magnitude (Figure 5.38(e)) for Line 1 increases significantly. It should be noted here that even in such small scale, the discrimination of the faulted line is very distinct as the DWT magnitude of the healthy lines is practically zero. After approximately 1.1 ms, the algorithm proceeds to the selective tripping of Line 1 (Figure 5.38(f)), which is also depicted in the alphanumeric LCD screen of the user interface panel in Figure 5.39.

It is evident that the proposed scheme is practically feasible using commercially

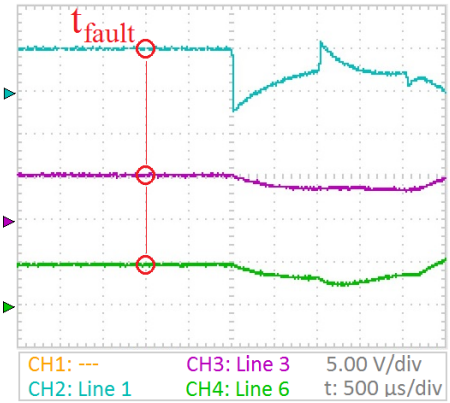


(a) DC currents

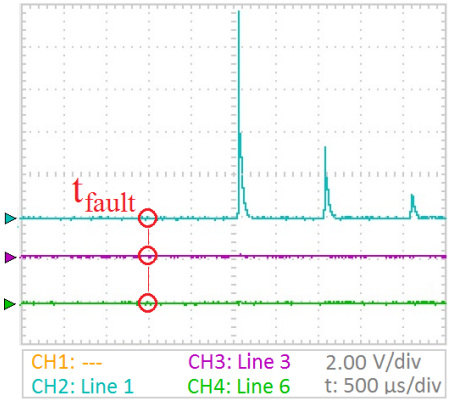
(b) DC current convariance



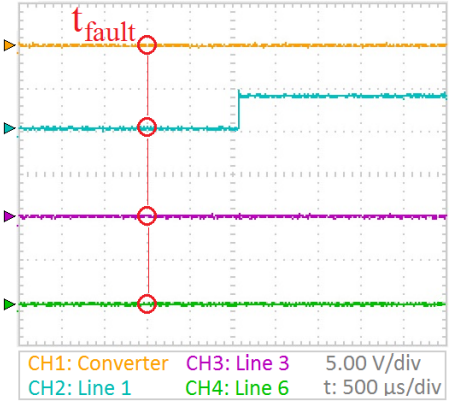
(c) Differential current



(d) Line DC voltages



(e) DWT of line DC voltages



(f) Tripping signals

Figure 5.38: Hardware prototype response to pole-to-pole fault at Line 1.

available hardware (which, in this case, has modest processing power), while the sensitivity to fault inception and the selectivity of the scheme has been clearly demonstrated.

5.4.7 Discussion

A new centralised protection scheme for MTDC grids has been proposed which utilises the principles of busbar differential protection and travelling waves. A thorough investigation

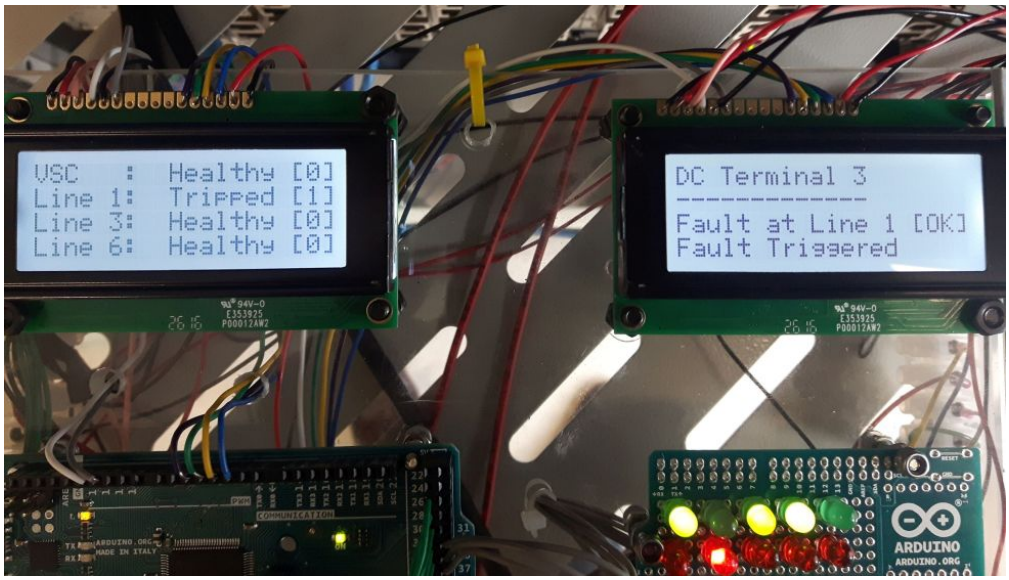


Figure 5.39: User interface panel output.

of the proposed scheme revealed the following remarks:

- The scheme requires communication within DC substation which has been enabled with IEC 61850.
- It has been found that the recommended frequency of 96 kHz reported in IEC 61869-9 is suitable for the detection of fast transient phenomena in HVDC grids; hence can be utilised for the implementation of fast and reliable DC busbar and line protection incorporating travelling waves.
- It has been found that the proposed scheme can provide fast and discriminative protection for busbar and line faults (both solid and highly resistive), including multiple faults occurring simultaneously on different transmission lines.
- The use of line terminating inductors leads to the limitation of the current rise in case of a fault, assists in the discrimination of the faulted line and also prevents the currents from exceeding the breaking capability of the CB.
- The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using a scaled-down laboratory prototype. This prototype provides a high level of confidence that the proposed method is practical, considering realistic measurements, communications and computation.
- Further sensitivity analysis revealed that a minimum sampling rate of 60 kHz would be adequate for this application.

5.5 Summary

This chapter has presented the structure and the requirements of MTDC protection. It has been pointed out that the performance of MTDC protection is very important and necessary to ensure the secure and reliable operation of HVDC grids. Such requirements introduce the need for transient DC fault characterisation, establishment of requirements and structure of HVDC protection schemes and subsequent development of a discriminative, fast, sensitive and reliable DC protection method.

A literature review of existing and proposed MTDC protection techniques has been carried out. It has been observed that much of the reported reserach on MTDC protection is still in very early stages; hence the focus has been on the conceptual aspects; however, important practical facets such as sampling frequency, time window, breaking capacity and time response of DC interruption devices have been neglected. Most importantly, there is neither discussion nor studies on the practical feasibility of the schemes, and the way measurements and signals exchange can be implemented locally (either on a line or busbar), within a DC substation or remotely. Taking into account the requirement of fast DC protection, all of the above play a significant role in the physical implementation of any protection scheme. Consequently, there are still unresolved issues and more research to be carried out.

Two protection solutions have been proposed in this chapter. The first one, termed as 'single-ended differential protection', utilises the principle of distributed optical sensing. It has been found that the proposed scheme can correctly operate for all types of faults, providing fast and discriminative protection for HVDC transmission systems. This has been demonstrated in detailed transient simulations, and further validated using a scaled down laboratory prototype of the proposed differential scheme. The key advantages of single-ended instantaneous current measurement have been outlined, which result in enhanced reliability, superior stability, and high speed of operation. The design, construction and operating principles of the hybrid optical sensors have been discussed in the chapter with emphasis given on the practical aspects of implementing such sensors in distributed monitoring of transmission lines.

The second solution is a new centralised scheme which utilises the principles of busbar differential protection and travelling waves and conforms with IEC 61869-9 and IEC 61850. It has been found that the proposed scheme can provide fast and discriminative protection for busbar and line faults (both solid and highly resistive). This has been validated in

detailed transient simulations, and further demonstrated using a real-time hardware-based laboratory prototype. This prototype provides a high level of confidence that the proposed method is practical, considering realistic measurements, communications and computation. The use of line terminating inductors leads to the limitation of the current rise in case of a fault, assists in the discrimination of the faulted line and also prevents the currents from exceeding the breaking capability of the HbCB (9 kA). Additionally, it has been found that the recommended frequency of 96 kHz reported in IEC 61869-9 is suitable for the detection of fast transient phenomena in HVDC grids, and hence can be utilised for the implementation of fast and reliable DC busbar and line protection incorporating travelling waves. Further sensitivity analysis revealed that a minimum sampling rate of 60 kHz would be adequate for this application.

Chapter 6

Enhanced DC Fault Location in HVDC Transmission

After the occurrence of a feeder fault on a transmission system, protection systems are expected to minimise its detrimental effects by initiating clearing actions such as selective tripping of circuit breakers. Following the successful fault clearance (and assuming the fault was permanent), the following action should be the accurate estimation of its location along the feeder. This is of major importance as it will enable faster system restoration, diminish power outage time, and therefore enhance overall reliability of the system.

This chapter demonstrates the outcome of several novel fault location algorithms, enabling accurate distance estimation in HVDC transmission lines. Transient analysis based on simulation and experiments are presented which verify the practical feasibility of the proposed schemes. A few technical challenges related the necessity for distance estimation accuracy are also discussed in this chapter.

6.1 Review of Fault Location Techniques

6.1.1 Travelling waves

During transmission line faults, due to the abrupt change in voltage, a series of transients are generated; these propagate along the lines in all directions. These transients are known as travelling waves (TWs). Associated with TWs are some unique features: magnitude, polarity and time intervals [235, 236]. It has been demonstrated in many

publications that TWs can be used to accurately estimate fault position on a transmission line. This estimation can be achieved using measurements either from a single end or from both ends of the faulted circuit. Single-ended methods require identification of two consecutive TW reflections measured at one terminal, while the two-ended methods use the first reflection only (captured and time-stamped at both line terminals). As the first reflection always provides the clearest signature, two-ended methods are considered more reliable [190]. Nevertheless, the selection between single-ended and two-ended methods is a trade-off between the cost, complexity and required reliability of the estimation [237].

A Wavelet transform approach is utilised in [238] to locate the faults in star-connected MTDC systems. The method uses continuous Wavelet transform applied to the DC line current waveforms. It is shown to be capable of completely eliminating the requirement for repeater stations at the network junctions. However, a high sampling frequency (2 MHz) and time-synchronised measurements are required. Additionally, highly resistive faults have not been investigated thoroughly.

Based on unsynchronised voltage and current measurements from the two terminals of the line, a mix of Bergeron time domain and TW-based fault location method is proposed in [239]. The method has been found to be accurate with both metallic and highly resistive faults (with impedances of up to 500 Ω).

In [236] two graph theory-based lemmas together with the basic principle of single-ended TW-based fault location is proposed to locate the faults in MTDC networks. However, both publications [236, 239], indicate a need for high sampling frequency of 1 MHz. The method presented in [240] eliminates the requirement to detect the arrival time of the initial waves by utilising the dominant natural frequency in the spectrum analysis of TWs. The proposed scheme requires voltages and currents only from one terminal, sampled at 100 kHz. However, this method has been tested only for highly resistive faults up to 50 Ω.

A special category of fault location applies to networks which include hybrid non-homogeneous feeders with segments of both underground cables and overhead lines. For such applications, TWs have also been found to be a powerful method for fault location. However, in such networks, additional challenges for TW-based methods arise from the fact that the speed of electromagnetic wave propagation is not uniform, additional reflections are generated at the junction points, and there is an increased difficulty in identifying the faulted segment. For such networks in HVDC systems, a number of

fault location approaches are presented in [190, 241]. The authors of [190] propose the application of two-ended TW-based fault location based on time-stamped measurements (voltages and capacitor currents) sampled at 2 MHz. Prior to the TW-based fault location, the faulted segment is found by solving a set of equations estimating distance to fault for each segment. The method is very accurate even with noisy inputs; however, fault resistances up to 100 Ω were taken into account. Additionally, the requirement of high sampling rate and synchronised measurements could be considered a barrier in practical applications.

A fault location method featuring a combination of TWs, Hilbert-Huan Transformations (HHT) and Ensemble Mode Decomposition (EEMD) was proposed in [242]. The HHT and EEMD are used to obtain the time-frequency graph from which the arrival time of the waves and the corresponding instantaneous frequency are derived. The propagation velocity in then calculated (by using the instantaneous frequency) and together with the arrival time two-ended technique is used to calculated the fault distance. The sampling requirement of this method is 1 MHz; furthermore, highly resistive faults have not been investigated.

A single-ended hybrid method based on WT and correlation coefficients is proposed in [243] for accurately locating faults in submarine HVDC cables. However, in the proposed method extremely high rates have been used (i.e. 500 MHz & 250 MHz).

A flexible TW-based fault location technique is proposed in [244] which can be either adopt single or two-ended fault location approaches to accurately locate the position of the fault. However, the proposed idea requires TW data acquisition centres, repeater stations and communication links which obviously increase the cost and complexity while the reliability could be low.

6.1.2 Learning-based techniques

A special category of fault location identification techniques includes the application of learning-based approaches. Even though the application of such advanced techniques is widely used for fault classification and localisation in AC networks [245–249], there is a limited number in the literature for their applicability in HVDC networks [237, 241, 250].

A method based on post-fault voltage signatures (sampled at 80 kHz) is proposed in [237]. The proposed scheme calculates the fault location by estimating the Pearson coefficients between pre-simulated post-fault voltage patterns and existing cases, where

the location is unknown. The method was tested for long transmission lines and for different fault types and has been found to be achieve satisfactory accuracy. However, the method has been validated only for highly-resistive faults with values of up to 80 Ω.

A different approach is introduced in [241] where a support vector machine (SVM) is initially employed for faulted segment identification. Further investigation on TWs provides assistance to the calculation of fault location. For the implementation of this method, both voltage and current measurements of one end are required. Nevertheless, the requirement for sampling frequency is not specified, while the scheme has been validated for fault resistance values of up to 70 Ω.

6.1.3 Reflectometry

Reflectometry is a meausurement technique used to determine the characteristics of electrical lines by observing reflected waveforms. Such methods can be based on measurements in frequency or time domain [251]. These methods use external equipment to inject low-voltage, high frequency signal to the line and detect and process the resulting waveforms for anomalies (e.g. faults) along the length of the line [252].

In [253] an improved fault localisation technique is proposed which is based on time-frequency domain reflectometry and tangent distance pattern recognition. The method requires a signal generator to inject a reference signals into submarine cables. The reflected signal is then captured and together with the reference signal are used for post-fault by adopting time-frequency distribution, Euclidean and Tangent distance. The method has been validated practically on a section of a HVDC cable and has been found to be accurate. However, the sampling rate for reference and reflected signal is 8 GHz and 312.5 MHz respectively, which require special and possibly expensive equipment. In addition, the analysis requires a series of multiple and complex mathematical operations and the influence of fault resistance has not been investigated at all.

The article in [254] reviews the methods for diagnosing and locating faults in submarine power cables with case studies relevant to long AC cables and very long HVDC cables. Emphasis is given on the differences in the conditions and methods between locating a fault on a submarine cable from land cables, and the best practices for diagnosing and locating these types of faults are discussed. Even though the actual methodologies and test results are not presented thoroughly, it can be deduced the need for external equipment and high sampling rates can be taken as drawback of these methods.

6.1.4 Other methods

In [255] the location of the fault is calculated by estimating the voltage distribution across a Bergeron line model. For this method, voltages and currents sampled at 6.4 kHz are required and the method has been found to be accurate for long transmission lines and for resistive faults up to 500 Ω. The only drawback of the method is the requirement for synchronised measurements.

With regards to impedance-based methods, even though they are well established in AC systems [256] it is quite impractical to implement them in HVDC lines due to the lack of a fundamental frequency component.

6.1.5 Challenges and barriers in fault location

A literature review on the existing and proposed fault location techniques revealed that there is a wide selection of options which can accurately calculate the location of a fault. However they are all accompanied by some technical challenges and barriers which are presented below for each category:

Travelling waves: Most of methods based on TWs usually require high sampling frequency in order to achieve high accuracy on the estimation of the fault location [238]. Such a requirement is frequently considered as an important drawback of TW-based methods. Additional challenges include the first wave detection [237], the need for synchronised measurements (for two-ended methods) [190], the impact of fault resistance [235,257], and the fact that the propagation speed of the transmission medium should be known (can be either deduced by the conductor geometry or estimated by a known fault location) [190].

Learning-based: The major challenge in learning-based methods is the requirement of training samples. Since fault records are not always sufficient (or sometimes not available at all) the training is usually implemented by simulation-based iterative studies. This could raise concerns with regards to the reliability of the system training.

Reflectometry: One of the main disadvantages of these methods is the need of external equipment which is usually a signal generator and a fault recorder/processor. Moreover, most of the existing methods based on reflectometry require sampling rates in the range of MHz to GHz. Last but not least, the application of reflectometry-based methods require a

site visit to the feed terminal and assembly and disassembly of testing equipment. Apart from the fact that a site visit cannot be always permitted, the assembly and disassembly procedure could take days for HVDC substations.

Last but not least, most of the above-reviewed methods consider mainly point-to-point HVDC links in the study cases. As such, the post-fault measurements (voltage and current) are sufficient enough to allow post-fault analysis (faults are usually cleared from the AC side which take several cycles to operate). This raises concerns regarding their applicability in VSC-MTDC grids as dedicated breaker mechanisms (DC circuit breakers) are expected to clear the faulted line. The requirements of fast operation of HVDC protection (detection and interruption) could potentially make fault localisation more challenging as limited measurement data during the fault can be extracted (excluding reflectometry-based methods).

6.2 Method 1: Travelling Wave-based Fault Locator for Hybrid Transmission Systems

This part of the thesis presents a new method for locating faults in MTDC networks incorporating hybrid transmission media (HTMs), including segments of underground cables (UGCs) and overhead lines (OHLs). In such networks, challenges for TW-based methods arise from the fact that the speed of electromagnetic wave propagation is not uniform, additional reflections are generated at the junction points, and there is an increased difficulty in identifying the faulted segment.

The proposed TW-type method uses Continuous Wavelet Transform (CWT) applied to a series of line current measurements obtained from a network of distributed optical sensors. The technical feasibility of optically-based DC current measurement is evaluated through laboratory experiments using Fibre-Bragg Grating (FBG) sensors and other commercially available equipment (has also been demonstrated and used in Chapter 5.3). Simulation-based analysis has been used to assess the proposed technique under a variety of fault types and locations within an MTDC network. The proposed fault location scheme has been found to successfully identify the faulted segment of the transmission media as well as accurately estimating the fault position within the faulted segment. Systematic evaluation of the method is presented considering a wide range of fault

resistances, mother wavelets, scaling factors and noisy inputs. Additionally, the principle of the proposed fault location scheme has been practically validated by applying a series of laboratory test sets.

6.2.1 Fault location strategy

The proposed fault location scheme utilises the TW principle applied to a series of measured waveforms obtained from current sensors distributed along the transmission line. The distributed optical measuring arrangement has been previously shown by the authors as being capable of enabling highly discriminative DC line protection. The details and rationale for utilising distributed optical sensing can be found in [36] and are also explained in detail in Chapter 5.3. It should be noted here that the key advantage of the measuring arrangement is that all sensing points are completely passive (i.e. require no power supply) and can be interrogated directly from a single piece of equipment at either end of the line, where the protective equipment is placed. In fault location applications, the immediate benefit of multiple distributed sensing is that the fault location can be successfully performed in transmission lines containing multiple segments, and is not limited to two segments as described in [241]. Additionally, when compared to [190] and several other methods, the proposed fault location approach requires neither high sampling frequency nor external time-stamping equipment (i.e. GPS).

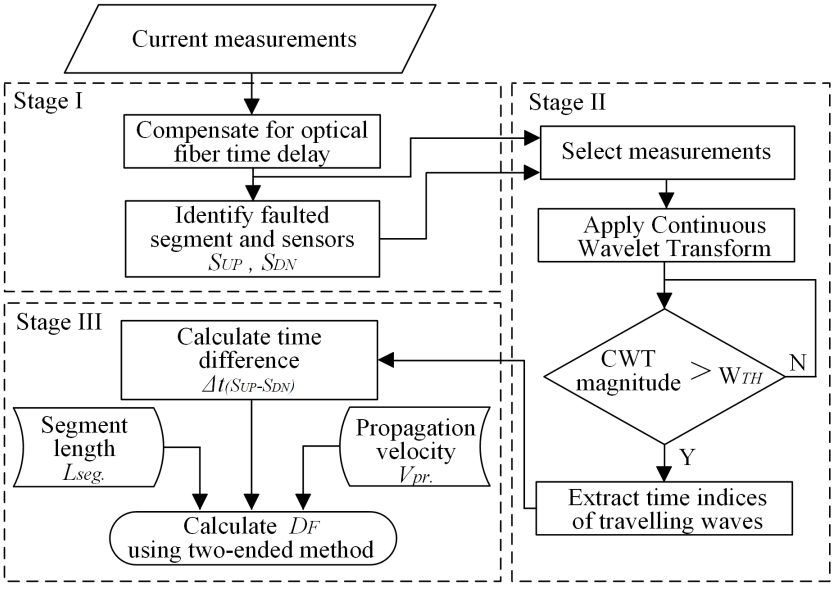


Figure 6.1: Fault location algorithm flow chart.

As the scheme depends primarily on the utilisation of TWs which can be observed in

both voltage and current waveforms, the choice of specific signal is usually guided by the ease of measurement and cost. In this case, the current was considered more appropriate due to the availability of the distributed optical sensing arrangement used previously in the current-based protection described in [36]. However, in a different practical situation, the use of voltage measurement could also provide similar fault location functionality.

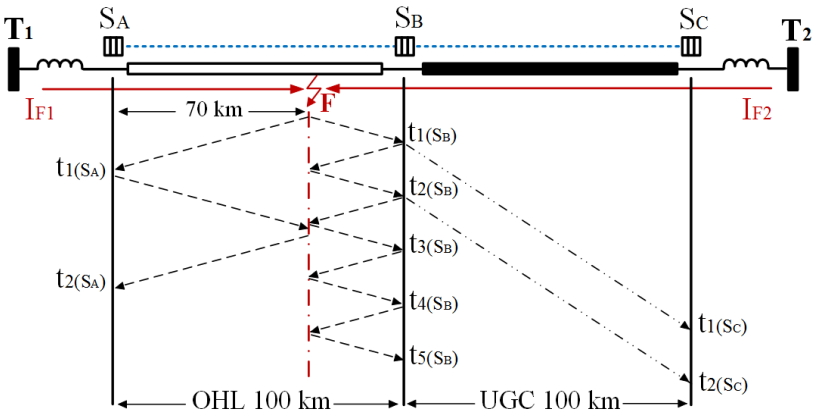


Figure 6.2: Bewley Lattice diagram incorporating OHL, UGC and distributed optical current sensors.

The proposed fault location scheme consists of three main stages as depicted in Figure 6.1. To enhance clarity of the description an example illustration is presented in Figure 6.2 which includes a hybrid circuit with 100 km OHL and 100 km UGC. A fault is shown to occur on the OHL at a distance of 70 km from T_1 (where the measurements are collected). The three stages of the proposed fault location alogrithm are explained in detail as follows:

Stage I - Faulted Segment Identification: In this stage the faulted segment (e.g. UGC or OHL) is identified. As seen in Figure 6.1, prior to any processing the measurements are compensated for the time delay imposed by the optical fibre. Such time delay corresponds to the speed of light and the refractive index of SMF-28 fibre which can be found in [216]. The fault segment identification approach is illustrated in more detail in Figure 6.4.

The faulted segment identification is implemented by calculating the differential current I_{diff} for every pair of adjacent sensors. When a fault occurs between two sensors, the differential current derived from those sensors reaches much higher level than the current derived from any other adjacent pair. For the fault case shown in Figure 6.2 differential current I_{diff} is calculated for the two adjacent sensor pairs $S_A - S_B$ and $S_B - S_C$, and is illustrated in Figure 6.3. The difference is almost one order of magnitude

which allows for a reliable selection of the faulted section of the line using a simple instantaneous value comparison.

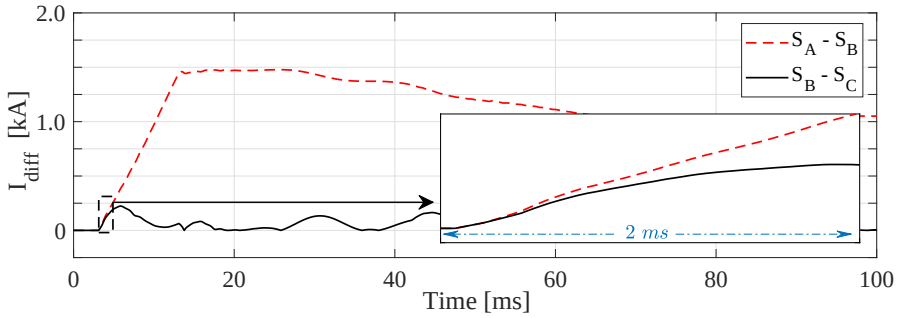


Figure 6.3: Differential currents for the fault case corresponding to Figure 6.2.

The identification stage produces two outputs S_{UP} and S_{DN} which correspond to the two adjacent sensors, one upstream and one downstream with respect to the fault (S_A and S_B in the depicted case). To achieve this, the algorithm incrementally searches for the first sensor (index r) corresponding to the highest differential current (in this case $r = A$). This sensor becomes $S_{UP} = r$, and the adjacent sensor becomes $S_{DN} = r + 1$ (considering that highest differential current has been reached by measurements of sensors r and $r + 1$).

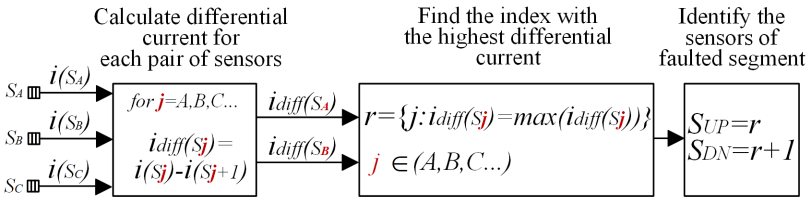


Figure 6.4: Faulted segment identification algorithm.

Since high frequency components are not used at this stage (and also to eliminate any interference from noise), a moving average with a time window of 5 ms is applied. It is also shown in the zoomed area of Figure 6.3 that only a small amount of post-fault data (less than 1 ms) is needed to successfully perform the faulted segment identification. This is evident from the zoomed area of the initial 2.0 ms following the fault where the current corresponding to the faulted segment can be clearly distinguished from a very early stage. Consequently, the performance of the proposed faulted segment identification cannot be jeopardised, even with ultra fast DC protection schemes (considering combined detection and isolation time).

Stage II - Wave Detection: In this stage the precise time of wave arrival is established. The algorithm initiates with the selection of the two measurements adjacent to the fault S_{UP} and S_{DN} as reported by Stage I. Those measurements are then processed by the CWT to detect the precise arrival times of the individual TWs.

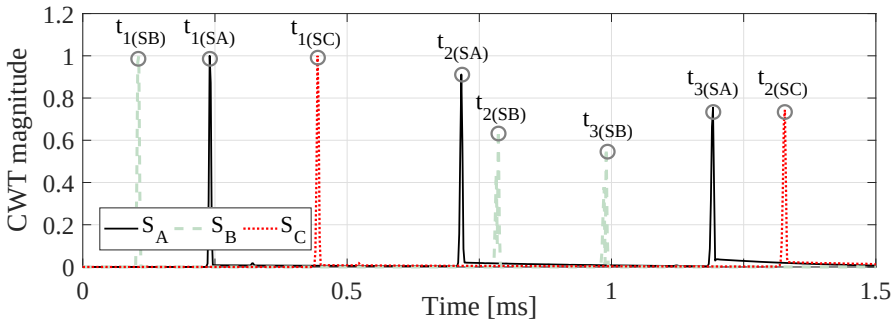


Figure 6.5: Normalised absolute values of wavelet coefficient magnitudes for the fault case corresponding to Figure 6.2.

The wavelet transform of a function $\zeta(t)$ can be expressed as the integral of the product of $\zeta(t)$ and the daughter wavelet $\Psi^*_{a,b}(t)$ as

$$W_\psi \zeta(t) = \int_{-\infty}^{\infty} \zeta(t) \underbrace{\frac{1}{\sqrt{\alpha}} \Psi\left(\frac{t-b}{a}\right)}_{\text{daughter wavelet } \Psi^*_{a,b}(t)} dt \tag{6.1}$$

The daughter wavelet $\Psi^*_{a,b}(t)$ is a scaled and shifted version of the mother wavelet $\Psi_{a,b}(t)$. Scaling is implemented by α which is the binary dilation (also known as scaling factor) and shifted by b which is the binary position (also known as shifting or translation). For further analysis of Wavelet transform Chapter 4.3 may be consulted.

In Figure 6.5 the normalised absolute values of wavelet coefficient magnitudes for the fault case corresponding to Figure 6.2 are depicted. It should be noted that the magnitudes have been normalised individually according to the maximum value of the TWs in each measurement (which is usually the initial TW).

In this case the selected measurements would be from sensors S_A (black solid line) and S_B (green dashed line). The exact times of the waves are established by comparing the waveforms with a predefined threshold W_{TH} (i.e. the time instant is recorded when the threshold is exceeded). For sensor S_A those time instances correspond to $t_{1(SA)}$ and $t_{2(SA)}$ (as shown in Figure 6.5), while for the sensor S_B those times are depicted as $t_{1(SB)}$, $t_{2(SB)}$, $t_{3(SB)}$, $t_{4(SB)}$ and $t_{5(SB)}$.

Stage III - Fault location calculation: In the final stage of the algorithm, the actual fault location is calculated. Since the measurements from both ends of the faulted segment are available locally, two-ended fault location approach can be conveniently applied. It is worth reiterating that the utilised optical sensing scheme can interrogate all sensors from a single acquisition point, and thus synchronised measurements can be ensured without the need of GPS (i.e. the difference in measurement time arrival from individual sensors is known and can be easily calculated). Taking as a reference the left-hand side (i.e. where S_{UP} is located) of the HTM the fault location can be estimated by

$$D_F = \frac{L_{seg} - \Delta t_{(S_{UP}-S_{DN})} \cdot v_{prop}}{2} \tag{6.2}$$

where D_F is the distance between S_{UP} sensor and the fault (calculated using the measurements of both sensors S_{UP} and S_{DN}), L_{seg} is the total length of the faulted segment, $\Delta t_{(S_{UP}-S_{DN})}$ is the time difference of the initial TWs at sensing locations S_{UP} and S_{DN}, and v_{prop} is the propagation velocity of the faulted segment.

For the studies presented in this section the propagation velocity has been calculated according to the conductor geometry of each segment.

6.2.2 Modelling

A model of a five-terminal HVDC grid illustrated in Figure 6.6 has been developed in for the purposes of evaluating the proposed fault location method. The network architecture has been adopted from the Twenties Project case study on DC grids [163]. There are five modular multi-level converters (MMCs) in the network operating at ±400 kV (in symmetric monopole configuration), current limiting inductors, and HTMs with OHLs and UGCs (both are represented by the distributed parameter line model). The line lengths of each HTM segment can be seen in Table 6.2. The parameters used in modelling of the OHLs and UGCs can be found in Table 6.3 [258].

A network of distributed current optical sensors is installed on all HTMs. The sensors are installed at each line end, and one at each junction. The main purpose of the junction sensor is to facilitate the faulted segment identification. Therefore, there is no need for the installation of two sensors at both sides of the junction (unless there were more than two lines connected to the node) as the same current would be measured by both sensors. Each sensing network is terminated at one end of the HTM where the measuring

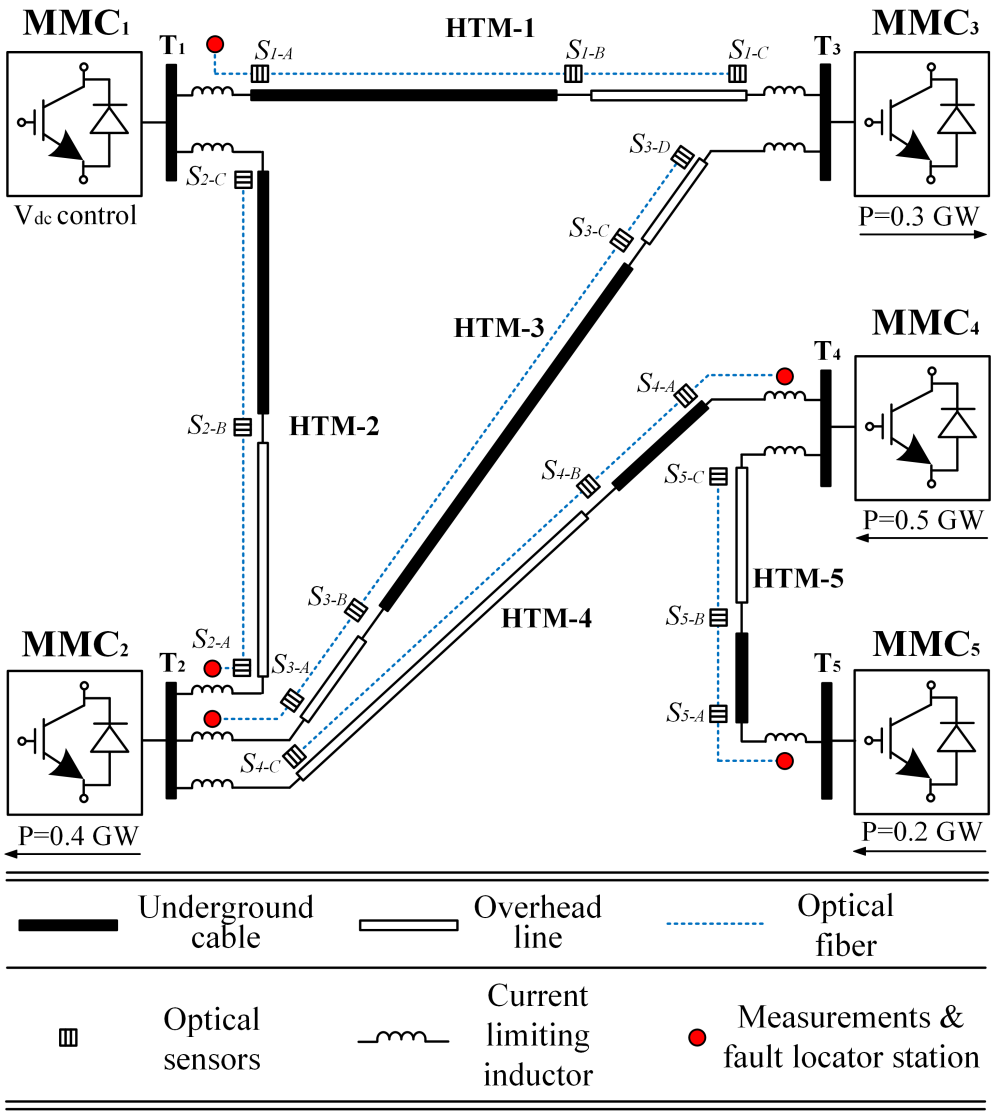


Figure 6.6: Case study five terminal HVDC network.

and fault location equipment (i.e. fault locator station) is placed. As the method is single-ended by its nature, there is only one optical measurement interrogator, and one fault locator station required for each HTM. Therefore, in some converter stations (e.g. MMC_3) there is no measuring equipment, only the sensors attached to the end of the optical fibre. The fault location results presented in the following sections are reported taking the fault locator station as a reference point. The parameters of the AC and DC network components are included in Table 6.1.

Table 6.1: DC and AC network parameters.

Parameter	Value
DC voltage [kV]	± 400
DC inductor [mH]	150
AC frequency [Hz]	50
AC short circuit level [GVA]	40
AC voltage [kV]	400
MMC levels	401
MMC arm inductance [p.u.]	0.1
MMC equivalent arm capacitance [μF]	20.84

Table 6.2: Lengths of OHLs and UGCs included in MTDC case study grid.

HTM-1	UGC: 150 km, OHL: 70 km
HTM-2	OHL: 100 km, UGC: 100 km
HTM-3	OHL-a: 65 km, UGC: 180 km, OHL-b: 35 km
HTM-4	UGC: 50 km, OHL: 130 km
HTM-5	UGC: 30 km, OHL: 70 km

Table 6.3: Parameters of UGC and OHL.

Parameter	OHL	UGC
Resistance [Ω/km]	0.015	0.0146
Inductance [mH/km]	0.96	0.158
Capacitance [$\mu F/km$]	0.012	0.275
Speed of propagation [km/s]	294,627.8	151,706.8

6.2.3 Simulation results

6.2.3.1 Case studies and methodology

Pole-to-pole faults (PPFs) and pole-to-ground faults (PGFs) have been simulated in all segments of the MTDC network, at varying distances and with various fault resistances (R_f) of up to 500 Ω. Additionally, test cases have been expanded to include a wide range of mother wavelets Ψ, scaling factors α and the impact of noisy measurements.

First, the signals have been sampled at 135 kHz (which corresponds to the resonant frequency of optical sensors, imposed by their mechanical properties) and the CWT magnitudes have been normalised (as also shown in Figure 6.5). The threshold W_{TH} used for establishing the wave arrival time has been set to 0.25. As also discussed in [238] the value of the threshold is subject to the assumed safety margins, anticipated levels of noise in the measured signal and scale of CWT.

The most suitable mother wavelet is usually selected by trial-and-error studies. The

two major criteria are the provision of sharp edge for wave detection and the requirement for processing resources. However the latter is not so crucial in fault location applications as they are more focused on accuracy. For HVDC fault location applications it has been found in the literature that mother wavelets with relatively good performance include the *'Haar'* and *'db1'* [190, 238, 241] wavelets. This will be also verified later with the aid of simulations.

The values of fault location estimation error have been calculated according to

$$error\ [\%] = \frac{D_F - D_F^*}{L_{seg}} \cdot 100\% \tag{6.3}$$

where D_F is the calculated fault distance, D_F^* is the actual fault distance and L_{seg} the total length of the faulted segment.

6.2.3.2 Fault location results

The results of faulted segment identification and fault location are included in Table 6.4 for PPFs and Tables 6.5 and 6.6 for resistive PGFs with $R_f = 100\ \Omega$ and $R_f = 500\ \Omega$ respectively. The presented results were obtained by utilising *'Haar'* mother wavelet with a scaling factor $\alpha = 2$, since (theoretically) results with increased accuracy are expected in lower scales.

The minimum, maximum and average errors observed for PPFs are 0%, 1.4817% and 0.3768% respectively while for PGFs ($R_f = 100\ \Omega$) those errors were 0.0262%, 1.3389% and 0.3714% respectively. The aforementioned errors for PGFs with $R_f = 500\ \Omega$ correspond to 0.000%, 1.4770% and 0.4170%, which verify that the proposed scheme is accurate even for highly-resistive faults. The faulted segment has been identified correctly in 100% of the cases for both types of faults. What is also interesting to note is that the proposed fault location scheme achieves high accuracy even in the case of close-up faults (i.e. faults occurring close to the head or end of each line segment).

Table 6.4: Segment identification and fault location results for PPFs.

HTM	Segment	Fault distance [km]	Reported sensors S_{UP}	Reported sensors S_{DN}	Reported fault location [km]	Error [%]
1	UGC	25.0	S_{1-A}	S_{1-B}	24.9929	-0.0047
1	UGC	55.0	S_{1-A}	S_{1-B}	55.3343	0.2229
1	UGC	78.5	S_{1-A}	S_{1-B}	78.3713	-0.0858
1	UGC	103.5	S_{1-A}	S_{1-B}	103.6557	0.1038
1	UGC	141.0	S_{1-A}	S_{1-B}	141.3015	0.2010
1	OHL	23.2	S_{1-B}	S_{1-C}	22.9966	-0.2905
1	OHL	48.0	S_{1-B}	S_{1-C}	48.2108	0.3012
1	OHL	57.7	S_{1-B}	S_{1-C}	57.9155	0.3079
1	OHL	65.5	S_{1-B}	S_{1-C}	64.4628	-1.4817
2	OHL	18.5	S_{2-A}	S_{2-B}	18.3548	-0.1452
2	OHL	50.0	S_{2-A}	S_{2-B}	51.0912	1.0912
2	OHL	63.6	S_{2-A}	S_{2-B}	64.1858	0.5858
2	OHL	77.0	S_{2-A}	S_{2-B}	77.2804	0.2804
2	UGC	9.0	S_{2-B}	S_{2-C}	8.4211	-0.5789
2	UGC	43.8	S_{2-B}	S_{2-C}	43.2575	-0.5425
2	UGC	69.4	S_{2-B}	S_{2-C}	69.1038	-0.2962
2	UGC	88.0	S_{2-B}	S_{2-C}	88.2076	0.2076
2	UGC	90.0	S_{2-B}	S_{2-C}	89.8933	-0.1067
3	OHL-a	12.4	S_{3-A}	S_{3-B}	11.7669	-0.9740
3	OHL-a	35.0	S_{3-A}	S_{3-B}	35.7736	1.1902
3	OHL-a	42.0	S_{3-A}	S_{3-B}	42.3209	0.4937
3	OHL-a	50.1	S_{3-B}	S_{3-C}	51.0506	1.4625
3	OHL-a	57.3	S_{3-B}	S_{3-C}	57.5979	0.4583
3	UGC	10.0	S_{3-B}	S_{3-C}	9.6516	-0.1936
3	UGC	39.7	S_{3-B}	S_{3-C}	39.9929	0.1627
3	UGC	56.7	S_{3-B}	S_{3-C}	56.8493	0.0829
3	UGC	95.0	S_{3-B}	S_{3-C}	95.0569	0.0316
3	UGC	100.0	S_{3-B}	S_{3-C}	99.5519	-0.2489
3	UGC	103.0	S_{3-B}	S_{3-C}	102.9232	-0.0427
3	UGC	161.2	S_{3-B}	S_{3-C}	161.3584	0.0880
3	UGC	173.0	S_{3-C}	S_{3-D}	172.5959	-0.2245
3	OHL-b	26.7	S_{3-C}	S_{3-D}	26.6210	-0.2256
3	OHL-b	30.0	S_{3-C}	S_{3-D}	29.9337	-0.1893
3	OHL-b	33.7	S_{3-C}	S_{3-D}	33.8682	0.4806
4	UGC	3.8	S_{4-A}	S_{4-B}	3.6487	-0.3027
4	UGC	13.2	S_{4-A}	S_{4-B}	13.2006	0.0012
4	UGC	29.10	S_{4-A}	S_{4-B}	29.4950	0.7900
4	UGC	46.6	S_{4-A}	S_{4-B}	46.3513	-0.4973
4	OHL	29.0	S_{4-B}	S_{4-C}	28.9899	-0.0077
4	OHL	53.5	S_{4-B}	S_{4-C}	52.9966	-0.3872
4	OHL	74.0	S_{4-B}	S_{4-C}	73.7297	-0.2079
4	OHL	110.2	S_{4-B}	S_{4-C}	109.7398	-0.3540
4	OHL	125.0	S_{4-B}	S_{4-C}	125.0168	0.0129
5	UGC	2.6	S_{5-A}	S_{4-B}	2.6387	0.1290
5	UGC	7.9	S_{5-A}	S_{4-B}	8.2575	1.1916
5	UGC	10.7	S_{5-A}	S_{4-B}	10.5050	-0.6501
5	UGC	15.0	S_{5-A}	S_{4-B}	15.0000	0.0000
5	UGC	29.5	S_{5-A}	S_{4-B}	29.6088	0.3627
5	OHL	7.9	S_{5-B}	S_{4-C}	7.7196	-0.2576
5	OHL	33.8	S_{5-B}	S_{4-C}	33.9088	0.1554
5	OHL	45.5	S_{5-B}	S_{4-C}	44.8209	-0.9701
5	OHL	66.6	S_{5-B}	S_{4-C}	66.6452	0.0646
5	OHL	69.0	S_{5-B}	S_{4-C}	68.8276	-0.2462

Table 6.5: Segment identification and fault location results for PGFs ($R_f = 100\ \Omega$).

HTM	Segment	Fault distance [km]	Reported sensors S_{UP}	Reported sensors S_{DN}	Reported fault location [km]	Error [%]
1	UGC	39.5	S_{1-A}	S_{1-B}	39.6017	0.0678
1	UGC	56.0	S_{1-A}	S_{1-B}	55.8962	-0.0692
1	UGC	100	S_{1-A}	S_{1-B}	100.2845	0.1896
1	UGC	135.6	S_{1-A}	S_{1-B}	135.6827	0.0552
1	UGC	148.0	S_{1-A}	S_{1-B}	148.0440	0.0294
1	OHL	12.2	S_{1-B}	S_{1-C}	12.0845	-0.1650
1	OHL	38.7	S_{1-B}	S_{1-C}	38.2736	-0.6091
1	OHL	43.2	S_{1-B}	S_{1-C}	42.6385	-0.8021
1	OHL	68.0	S_{1-B}	S_{1-C}	67.7364	-0.3765
2	OHL	19.8	S_{2-A}	S_{2-B}	20.5372	0.7372
2	OHL	48.8	S_{2-A}	S_{2-B}	48.9088	0.1088
2	OHL	88.8	S_{2-A}	S_{2-B}	88.1925	-0.6075
2	OHL	90.0	S_{2-A}	S_{2-B}	90.3749	0.3749
2	UGC	13.3	S_{2-B}	S_{2-C}	12.9161	-0.3839
2	UGC	33.3	S_{2-B}	S_{2-C}	33.1437	-0.1563
2	UGC	56.0	S_{2-B}	S_{2-C}	55.6188	-0.3812
2	UGC	71.6	S_{2-B}	S_{2-C}	71.3513	-0.2487
2	UGC	86.7	S_{2-B}	S_{2-C}	87.0839	0.3839
3	OHL-a	7.9	S_{3-A}	S_{3-B}	8.4933	0.9128
3	OHL-a	15.5	S_{3-A}	S_{3-B}	16.1318	0.9720
3	OHL-a	38.9	S_{3-A}	S_{3-B}	39.0473	0.2266
3	OHL-a	46.8	S_{3-A}	S_{3-B}	46.6858	-0.1757
3	OHL-a	62.1	S_{3-A}	S_{3-B}	61.9628	-0.2111
3	UGC	9.9	S_{3-B}	S_{3-C}	9.6516	-0.1380
3	UGC	10.5	S_{3-B}	S_{3-C}	10.7753	0.1530
3	UGC	59.0	S_{3-B}	S_{3-C}	59.0968	0.0538
3	UGC	87.1	S_{3-B}	S_{3-C}	87.1906	0.0503
3	UGC	100.0	S_{3-B}	S_{3-C}	99.5519	-0.2489
3	UGC	144.0	S_{3-B}	S_{3-C}	144.5021	0.2789
3	UGC	153.4	S_{3-B}	S_{3-C}	153.4921	0.0512
3	UGC	166.0	S_{3-B}	S_{3-C}	165.8534	-0.0814
3	UGC	177.7	S_{3-B}	S_{3-C}	177.6528	-0.0262
3	OHL-b	20.5	S_{3-C}	S_{3-D}	20.7736	0.7818
3	OHL-b	30.7	S_{3-C}	S_{3-D}	30.5946	-0.3012
4	UGC	6.5	S_{4-A}	S_{4-B}	6.4581	-0.0839
4	UGC	15.2	S_{4-A}	S_{4-B}	15.4481	0.4962
4	UGC	25.5	S_{4-A}	S_{4-B}	25.5619	0.1238
4	UGC	41.7	S_{4-A}	S_{4-B}	41.8563	0.3126
4	OHL	10.8	S_{4-B}	S_{4-C}	10.4393	-0.2775
4	OHL	55.3	S_{4-B}	S_{4-C}	55.1791	-0.0930
4	OHL	65.4	S_{4-B}	S_{4-C}	65.0000	-0.3077
4	OHL	99.1	S_{4-B}	S_{4-C}	98.8276	-0.2095
4	OHL	115.4	S_{4-B}	S_{4-C}	115.1959	-0.1570
5	UGC	5.2	S_{5-A}	S_{4-B}	4.8862	-1.0460
5	UGC	6.6	S_{5-A}	S_{4-B}	6.3344	-0.8854
5	UGC	14.7	S_{5-A}	S_{4-B}	15.0000	1.0000
5	UGC	26.6	S_{5-A}	S_{4-B}	26.2375	-1.2082
5	OHL	11.3	S_{5-B}	S_{4-C}	10.9933	-0.4382
5	OHL	21.0	S_{5-B}	S_{4-C}	20.8142	-0.2654
5	OHL	27.5	S_{5-B}	S_{4-C}	27.3615	-0.1979
5	OHL	44.0	S_{5-B}	S_{4-C}	44.4975	0.7107
5	OHL	58.0	S_{5-B}	S_{4-C}	57.9155	-0.1207
5	OHL	65.4	S_{5-B}	S_{4-C}	64.4628	-1.3389

Table 6.6: Segment identification and fault location results for PGFs ($R_f = 500\ \Omega$).

HTM	Segment	Fault distance [km]	Reported sensors S_{UP}	Reported sensors S_{DN}	Reported fault location [km]	Error [%]
1	UGC	1.2	S_{1-A}	S_{1-B}	1.3941	0.1294
1	UGC	5.7	S_{1-A}	S_{1-B}	5.8891	0.1261
1	UGC	34	S_{1-A}	S_{1-B}	33.983	-0.0114
1	UGC	100	S_{1-A}	S_{1-B}	100.2845	0.1896
1	UGC	129	S_{1-A}	S_{1-B}	129.5021	0.3347
1	UGC	149	S_{1-A}	S_{1-B}	149.7297	0.4864
1	OHL	35	S_{1-B}	S_{1-C}	35.0000	0.0000
1	OHL	55	S_{1-B}	S_{1-C}	54.6419	-0.5116
1	OHL	67	S_{1-B}	S_{1-C}	66.6452	-0.5068
2	OHL	1.5	S_{2-A}	S_{2-B}	1.9866	0.4866
2	OHL	50.7	S_{2-A}	S_{2-B}	51.0912	0.3912
2	OHL	90.2	S_{2-A}	S_{2-B}	90.3749	0.1749
2	OHL	95	S_{2-A}	S_{2-B}	94.7398	-0.2602
2	UGC	12.7	S_{2-B}	S_{2-C}	12.3542	-0.3458
2	UGC	29.9	S_{2-B}	S_{2-C}	29.2105	-0.6895
2	UGC	45.8	S_{2-B}	S_{2-C}	44.9431	-0.8569
2	UGC	66.6	S_{2-B}	S_{2-C}	66.2944	-0.3056
2	UGC	87.7	S_{2-B}	S_{2-C}	87.6458	-0.0542
3	OHL-a	8.1	S_{3-A}	S_{3-B}	8.4933	0.6051
3	OHL-a	23.8	S_{3-A}	S_{3-B}	24.5979	1.2276
3	OHL-a	35.6	S_{3-A}	S_{3-B}	35.7736	0.2671
3	OHL-a	46.5	S_{3-A}	S_{3-B}	46.6858	0.2858
3	OHL-a	55.5	S_{3-A}	S_{3-B}	55.4155	-0.1300
3	UGC	8.8	S_{3-B}	S_{3-C}	8.5278	-0.1512
3	UGC	12	S_{3-B}	S_{3-C}	11.8991	-0.0561
3	UGC	33	S_{3-B}	S_{3-C}	33.2504	0.1391
3	UGC	56.4	S_{3-B}	S_{3-C}	56.2874	-0.0626
3	UGC	100	S_{3-B}	S_{3-C}	100.1138	0.0632
3	UGC	144.3	S_{3-B}	S_{3-C}	144.5021	0.1123
3	UGC	156	S_{3-B}	S_{3-C}	155.7396	-0.1447
3	UGC	165.7	S_{3-B}	S_{3-C}	165.8534	0.0852
3	UGC	177.5	S_{3-B}	S_{3-C}	177.6528	0.0849
3	OHL-b	15.2	S_{3-C}	S_{3-D}	15.3176	0.3359
3	OHL-b	34	S_{3-C}	S_{3-D}	33.8682	-0.3765
4	UGC	5.1	S_{4-A}	S_{4-B}	5.3343	0.4686
4	UGC	28	S_{4-A}	S_{4-B}	28.3713	0.7425
4	UGC	42	S_{4-A}	S_{4-B}	42.4182	0.8364
4	UGC	48.5	S_{4-A}	S_{4-B}	49.1607	1.3214
4	OHL	4	S_{4-B}	S_{4-C}	2.8008	-0.9225
4	OHL	66	S_{4-B}	S_{4-C}	66.0912	0.0702
4	OHL	83.5	S_{4-B}	S_{4-C}	83.5506	0.0390
4	OHL	99	S_{4-B}	S_{4-C}	98.8276	-0.1326
4	OHL	115.7	S_{4-B}	S_{4-C}	116.2871	0.4516
5	UGC	2.7	S_{5-A}	S_{4-B}	2.7056	0.0186
5	UGC	9.5	S_{5-A}	S_{4-B}	9.9431	1.4770
5	UGC	11	S_{5-A}	S_{4-B}	11.3287	1.0958
5	UGC	18.4	S_{5-A}	S_{4-B}	18.6331	0.7771
5	UGC	28.5	S_{5-A}	S_{4-B}	28.7469	0.8231
5	OHL	11.5	S_{5-B}	S_{4-C}	10.9933	-0.7239
5	OHL	23	S_{5-B}	S_{4-C}	22.9966	-0.0048
5	OHL	39.8	S_{5-B}	S_{4-C}	39.3649	-0.6216
5	OHL	55.1	S_{5-B}	S_{4-C}	54.6419	-0.6545
5	OHL	67.3	S_{5-B}	S_{4-C}	66.6452	-0.9354

6.2.3.3 Effect of mother Wavelet Ψ and scaling factor α

In order to investigate the effect of mother wavelet Ψ and scaling factor α, a section of UGC at HTM-3 has been tested. In particular, PPFs from 90 km to 120 km with steps of 250 meters have been generated. For this range of faults the minimum (Min.), maximum (Max.) and average (Avg.) values have been calculated for different mother wavelets Ψ and scaling factors α, as shown in Table 6.7. The scaling factor values α have been selected using a power-of-two series $\alpha = 2^N$ (with $N = 1, 2, ..$). This is a common practice adopted in WT [190, 238, 259], and it provides a common base for comparison between different methods but also for comparison between CWT and DWT (scaling factors in DWT can only assume values of the power of two).

Satisfactory results have been achieved for the majority of mother wavelets and scaling factors. However, an increase in fault location error can be observed when the majority of mother wavelets have higher values of the scaling factor (e.g. $\alpha = 128$). The output of such study is that for the proposed fault location technique, the best performance (considering minimum, maximum and average values of error and for all the scaling factors) shall be provided by mother wavelets *'Haar', 'db1', 'db2', 'sym1' and 'sym2'*. The best overall accuracy in terms of average error has been achieved for mother wavelet *'coif2'* and scaling factor $\alpha = 4$. Predominantly, high performance is achieved to lower scales as they correspond to higher frequency components and the accuracy is expected to be theoretically greater [190, 191].

Table 6.7: Fault location errors of PPFs at UGC (HTM-3) for different values of scaling Factor α and Mother Wavelets Ψ.

α / Ψ	2			4			8			16			32			64			128		
	Min.	Max.	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.	Min.	Max.	Avg.
Haar	0.0000	0.2282	0.0860	0.0000	0.2667	0.0905	0.0000	0.2063	0.0833	0.0000	0.2448	0.0998	0.0000	0.5253	0.1505	0.0028	0.7055	0.3616	2.9111	4.4581	3.7014
db1	0.0000	0.2282	0.0860	0.0000	0.2667	0.0905	0.0000	0.2063	0.0833	0.0000	0.2448	0.0998	0.0000	0.5253	0.1505	0.0028	0.7055	0.3616	2.9111	4.4581	3.7014
db2	0.0000	0.2586	0.1102	0.0000	0.2517	0.0950	0.0000	0.1719	0.0788	0.0000	0.3906	0.1411	0.0014	0.6326	0.2840	0.7577	2.0462	1.1061	2.9303	3.5368	3.1106
db3	0.0000	0.7466	0.1285	0.0000	0.2229	0.0894	0.0000	0.4097	0.0958	0.0000	0.4097	0.0958	0.1472	0.9049	0.4186	1.0244	14.6712	1.8594	5.9309	17.3664	15.7722
db4	0.0000	0.4580	0.1357	0.0000	0.1719	0.0792	0.0000	0.2586	0.1081	0.0000	0.2420	0.0965	0.8073	7.0462	2.5598	2.1382	13.8035	6.9622	5.7920	19.4827	14.6758
sym1	0.0000	0.2282	0.0860	0.0000	0.2667	0.0905	0.0000	0.2063	0.0833	0.0000	0.2448	0.0998	0.0000	0.5253	0.1505	0.0028	0.7055	0.3616	2.9111	4.4581	3.7014
sym2	0.0000	0.2586	0.1102	0.0000	0.2517	0.0950	0.0000	0.1719	0.0788	0.0000	0.3906	0.1411	0.0014	0.6326	0.2840	0.7577	2.0462	1.1061	2.9303	3.5368	3.1106
sym3	0.0000	0.7466	0.1285	0.0000	0.2229	0.0894	0.0000	0.4097	0.0958	0.0000	0.4097	0.0958	0.1472	0.9049	0.4186	1.0244	14.6712	1.8594	5.9309	17.3664	15.7722
sym4	0.0000	0.4483	0.0994	0.0000	0.2420	0.0914	0.0000	0.4097	0.1078	0.0000	0.4455	0.1204	0.0000	0.5486	0.1450	0.0028	1.3711	0.7267	5.3066	7.9647	7.1351
coif1	0.0000	0.2420	0.0926	0.0000	0.1913	0.0837	0.0000	0.2586	0.1077	0.0000	0.4167	0.1258	0.0042	0.6601	0.2502	0.0055	0.6931	0.2957	7.8230	8.9823	8.5436
coif2	0.0000	0.1746	0.0801	0.0000	0.1677	0.0784	0.0000	0.1913	0.0847	0.0000	0.4441	0.1382	0.0028	0.4882	0.2257	0.0083	1.5608	0.3624	18.9369	22.2275	20.7976
coif3	0.0000	0.4580	0.1615	0.0000	0.1924	0.0791	0.0000	0.1913	0.0834	0.0000	0.4441	0.1536	0.0000	0.3507	0.1184	0.1896	2.2195	0.8455	25.5966	28.4678	27.4921
coif4	0.0000	0.7618	0.2123	0.0000	0.1993	0.0798	0.0000	0.1913	0.0824	0.0000	0.3163	0.1270	0.0000	0.3657	0.1190	0.4330	2.5660	1.1809	25.9088	28.4651	27.7475
meyr	0.0000	0.4497	0.1521	0.0000	0.7701	0.1619	0.0000	1.3806	0.1534	2.3295	3.2757	2.9622	0.5170	8.2713	2.9133	0.8140	3.4681	1.7820	8.8956	77.0236	51.3887
dmey	0.0000	0.8306	0.1812	0.0000	0.8306	0.2240	0.0000	1.5195	0.1499	2.0875	3.2399	2.8410	0.4813	8.3056	2.8923	0.7810	3.4337	1.7588	8.2713	30.7533	22.8975

6.2.3.4 Impact of noisy measurements

In order to assess and further scrutinise the performance of the proposed fault location scheme, the studies presented previously have been repeated considering noisy inputs. In particular, the current measurements have been subjected to artificial noise with

increasing amplitude up to 28 dB Signal to Noise Ratio (SNR). Excessive noise may result at the transimpedance amplifier stage, particularly when spectral signals from Fibre Bragg Grating (FBG) sensors need to travel relatively long sections of optical fibre and require significant amplification. Results for mother wavelet *'Haar'* are presented in Table 6.8.

Compared to the noise-less signal (infinite SNR), the increase in noise level (lower dB values correspond to higher levels of noise) has inevitably a degrading effect on the fault location accuracy. It can be concluded that the proposed fault location scheme is relatively robust to the additive noise, symptomatic of the fibre section lengths and sampling rates (hence photodetector bandwidth) considered in this simulation. In terms of average error it has been found that the error rises by 0.0369% for the SNR dropping to 28 dB.

Table 6.8: Fault location errors of PPFs at UGC (HTM-3) for Haar Mother Wavelet and for different levels of SNR and scaling factors α.

α / SNR [dB]	**2**			**4**			**8**			**16**			**32**			**64**			**128**		
	min	max	avg	min	max	avg	min	max	avg	min	max	avg	min	max	avg	min	max	avg	min	max	avg
∞	0.0000	0.2282	0.0860	0.0000	0.2667	0.0905	0.0000	0.2063	0.0833	0.0000	0.2448	0.0998	0.0000	0.5253	0.1505	0.0028	0.7055	0.3616	2.9111	4.4581	3.7014
80	0.0000	0.2282	0.0860	0.0000	0.2667	0.0905	0.0000	0.2063	0.0833	0.0000	0.2448	0.0998	0.0000	0.5253	0.1505	0.0028	0.7055	0.3616	2.9111	4.4581	3.7014
55	0.0000	0.2282	0.0860	0.0000	0.2667	0.0905	0.0000	0.2063	0.0824	0.0000	0.2517	0.1016	0.0000	0.5253	0.1523	0.0028	0.7055	0.3616	2.9111	4.4581	3.7039
45	0.0000	0.2254	0.0848	0.0000	0.2736	0.0906	0.0000	0.2063	0.0826	0.0000	0.2586	0.1044	0.0000	0.5253	0.1565	0.0028	0.7976	0.3745	2.9097	4.4581	3.6988
40	0.0000	0.2282	0.0860	0.0000	0.2667	0.0916	0.0000	0.2063	0.0829	0.0000	0.2517	0.1028	0.0000	0.5253	0.1637	0.0028	0.7976	0.3733	2.7035	4.4581	3.6807
38	0.0000	0.2282	0.0862	0.0000	0.2667	0.0913	0.0000	0.2063	0.0825	0.0000	0.2448	0.0999	0.0000	0.5253	0.1610	0.0028	0.7687	0.3684	2.7709	4.4581	3.6962
35	0.0000	0.2351	0.0862	0.0000	0.2764	0.0954	0.0000	0.2365	0.0875	0.0000	0.3288	0.1039	0.0000	0.5253	0.1758	0.0028	0.7687	0.3733	2.6334	4.4594	3.6652
30	0.0000	0.2351	0.0882	0.0000	0.2764	0.0920	0.0000	0.2035	0.0838	0.0000	0.4001	0.1208	0.0028	0.4910	0.1907	0.0028	0.9545	0.3857	2.4243	4.5956	3.6343
28	0.0000	0.2420	0.0849	0.0000	0.3590	0.1046	0.0000	0.2750	0.0888	0.0028	0.3975	0.1367	0.0042	0.4702	0.1780	0.0028	0.9420	0.3889	2.5976	4.5969	3.6652

6.2.3.5 Impact of fault current limiters

To accelerate practical feasibility of MTDC grids various types of fault current limiters are often utilised, installed either on the DC or AC side of the system [91, 93, 260]. It should be highlighted that the proposed fault location scheme should be immune against any practical fault current limiter, installed either on the AC or DC side. This will be better explained with the aid of Figure 6.7.

A transition point is a point on a line where there is a change in surge impedance. When an electromagnetic wave passes through a transition point, a part of it is reflected, and a part continues to travel in the same direction [155, 160]. As indicated in Figure 6.7, the initial wave is termed *'incident wave'*, and the resulting two at the transition point are called the *'reflected wave'* and the *'refracted wave'* (for in-depth analysis of travelling waves and transition points refer to Chapter 4.1). Any fault current limiting or interruption device, installed either on AC or DC side, is expected to increase the impedance (i.e. Z_{grid}) and consequently affect the amplitude of reflected and refracted

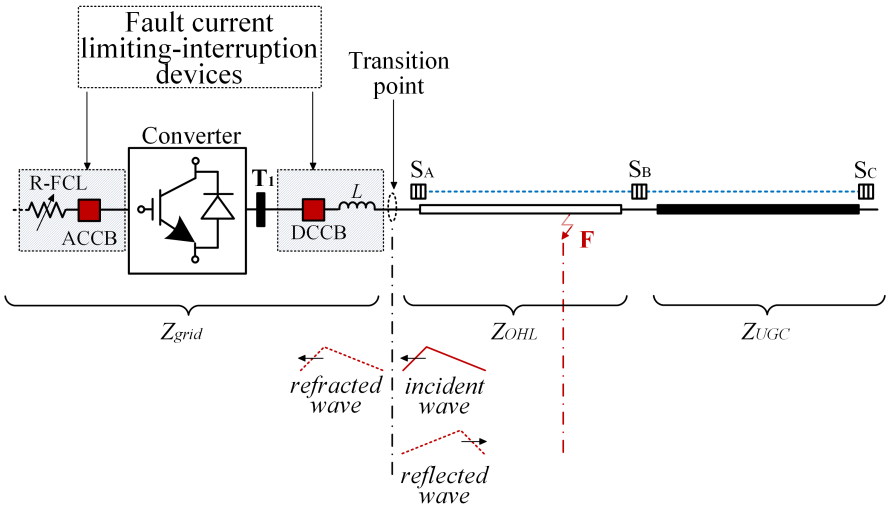


Figure 6.7: Explanation of travelling waves at a transition point.

waves. However, no impact is expected on the time of arrival of the TW which is determined by the line impedance Z_{OHL} and distance to fault. Considering this and the fact that the sensors of the proposed scheme are installed on the line side of any potential fault limiting element (see Figure 6.7) the performance of the scheme should not be compromised.

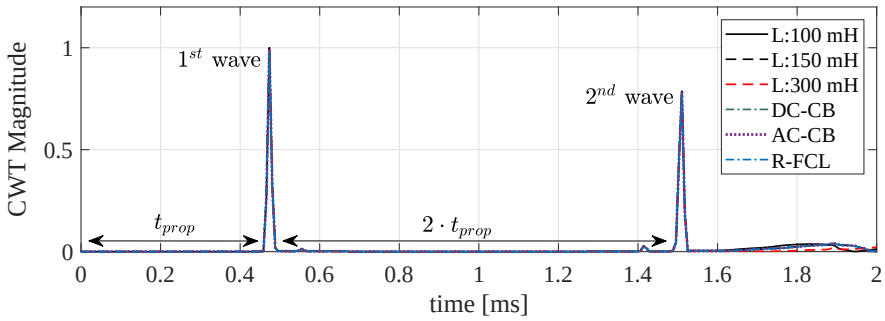


Figure 6.8: Normalised CWT magnitude for different fault current limiting technologies.

It should be noted that typical terminating inductors of 150 mH are already included in all the simulation results presented in previous sections. In order to further validate the above reasoning, a fault occurring at 78.5 km on the UGC section of HTM-1 has been simulated with different fault current limiting and interruption technologies. In particular inductive current limiters (with different inductance values), DC-CBs, AC-CBs, and AC resistive fault current limiters (R-FCLs) have been considered in the studies. DC-CBs represent a hybrid design as introduced in [36, 82], R-FCL have been modelled according to [261], while the AC-CBs are represented by mechanical disconnectors. The normalised

CWT magnitudes (for wave detection) of these cases are depicted in Figure 6.8, and the corresponding fault location errors have been reported as -0.0858% for all cases. The results in Figure 6.8 have been generated by utilising current measurements from sensors S_A and S_B as shown in Figure 6.7. The results demonstrate that fault current limiters and breakers (either on DC or AC side) do not distort the time response of TWs at the specific point of measurement and hence the fault location accuracy is not affected.

6.2.3.6 Effect of sampling time and small increments of fault distance

In order to investigate the effect of sampling time, a small incremental change in fault distance has been applied to the UGC section of HTM-3. The results for PPFs at positions of 99 km to 101 km with steps of 100 meters have been generated. For this range of faults the error is shown in Figure 6.9. The presented results were obtained by utilising *'Haar'* mother wavelet with a scaling factor $\alpha = 2$.

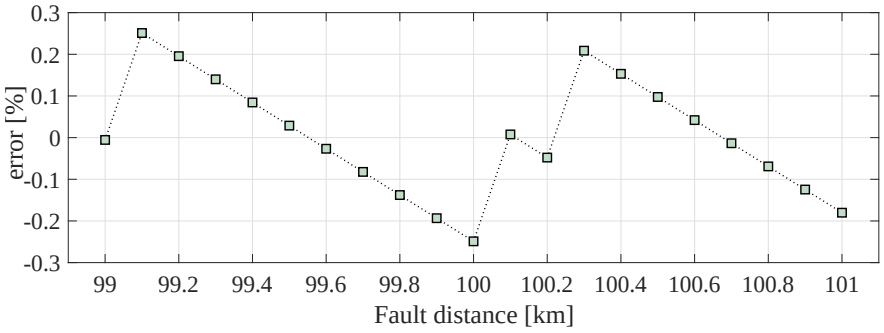


Figure 6.9: Fault location error with respect to small distance increment.

By moving fault position in short increments of 100 meters, an effect of randomly changing sampling instant is emulated. It has been established that the error can fluctuate between -0.2489 % and 0.2489 %. This result has been achieved at a very moderate sampling rate of 135kHz (used in all simulations presented in the thesis). To reduce the sampling-time-related error, the sampling rate would have to be increased. A similar effect can be expected from all TW-based methods.

6.2.4 Optical sensing technology

6.2.4.1 Transition joint pits

Optical sensing technology for HVDC applications is a growing area of research and development. However, there are only a handful of field trials reported in open literature

[101, 262, 263]. The purpose of such sensing schemes is to assist the implementation of protection, control, power quality and other power-system-related functions.

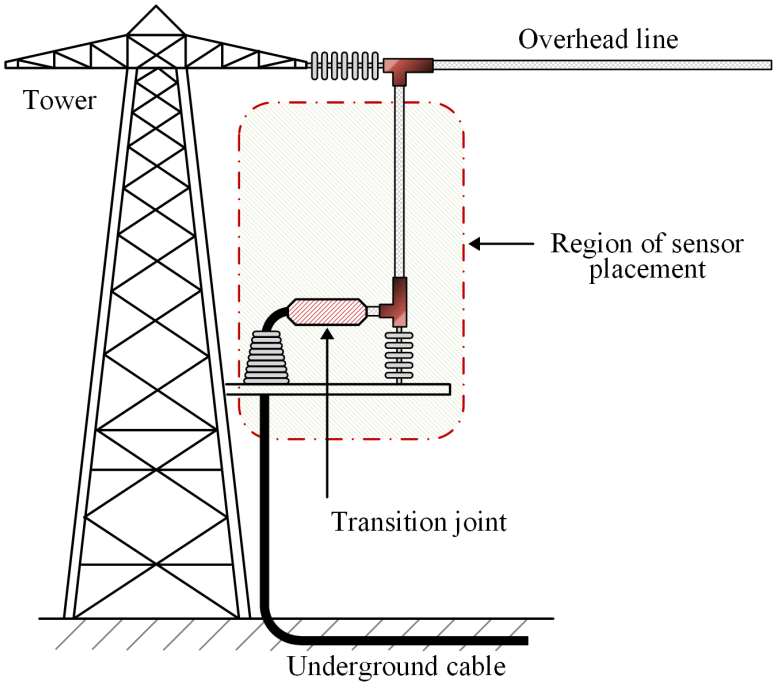


Figure 6.10: Typical representation of a transition joint pit.

Optical sensing schemes (i.e. examples of optical current transformers) for HVDC applications are also reported in IEC-61689 [226] (Part 9: Standards for Digital Interface for Instrument Transformers). From the technical point of view, the connection between overhead lines and cables is taking place at 'transition joint pits' (see Figure 6.10), and the actual conductor connection is established with 'transition joints' [49, 264]. Such pits are actual onshore installations with other protective, measuring and control components. Considering this, current optical sensors can be attached and installed around the transition joint and hence current measurements can be realised at transmission junctions.

6.2.4.2 Testing methodology

In order to prove the principle of the proposed fault location scheme, the optical sensor system previously developed and demonstrated in Chapter 5.3 to enable distributed DC line monitoring was utilised in this study.

The optical voltage sensor is formed by attaching an FBG to a piezoelectric transducer and measure strain generated as a result of a voltage applied across the transducer. The

strain exerted on the FBG produces a corresponding shift in its peak wavelength which can be calibrated in terms of voltage. An analogous function can be achieved by utilising a magnetostrictive transducer that responds to magnetic field generated around a conductor experiencing a fault current.

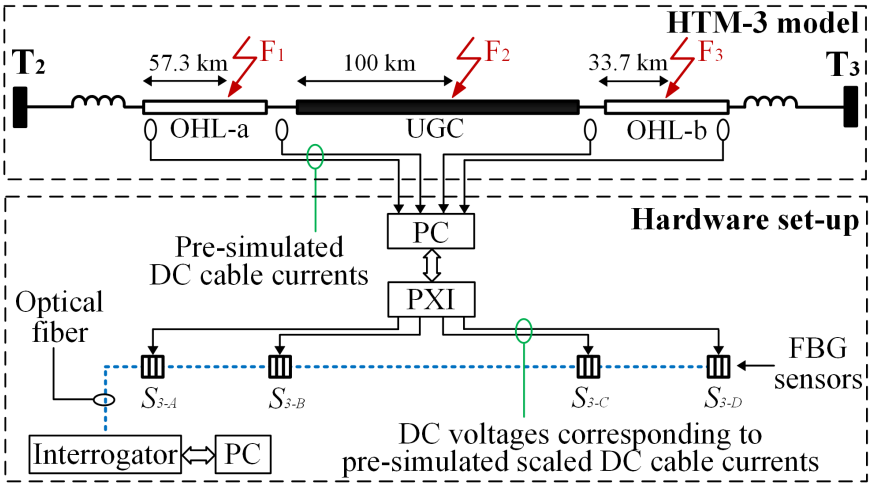


Figure 6.11: Experimental setup schematic diagram. Fault is shown between sensors S_B and S_C, at UGC segment.

Due to the working range of the utilised data acquisition card, the generated voltages were scaled to remain within a range of ±10 V. The voltage traces representing the DC line currents were then applied to the optical sensors while the corresponding measurement data obtained from the optical interrogation system was recorded on a PC for further processing by the fault location system algorithm.

6.2.4.3 Hardware setup

A schematic diagram of the experimental setup employed for the practical validation of the proposed fault location scheme and its physical arrangement are shown in Figure 6.11 and Figure 6.12, respectively. The experimental setup depicted in Figure 6.12 is applicable to any HTM regardless of the number of segments and shall be installed independently for each HTM. As a result, each fault location scheme operates independently and is not affected by the operation of any other distributed sensing networks. This facilitates high flexibility under various operating modes. For example, when an HTM is out of service, only the scheme corresponding to the specific HTM needs to be deactivated, permitting the remaining fault location schemes to continue operating. It should be noted that the HTM-3 was selected for demonstration as the most challenging case considering the

number of segments and the length of lines.

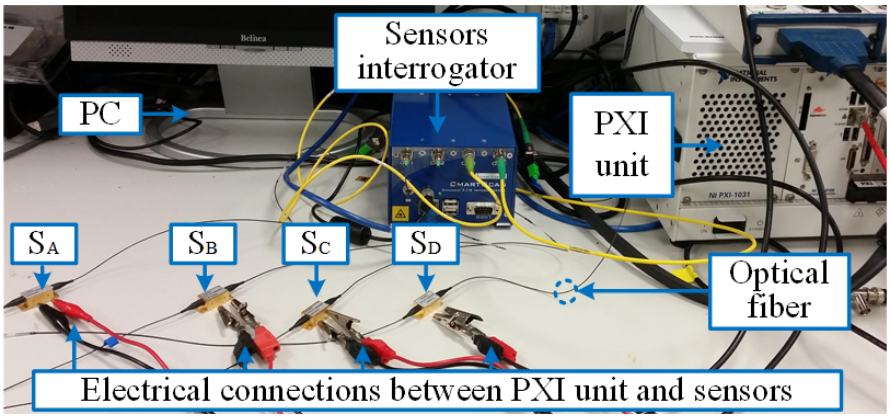


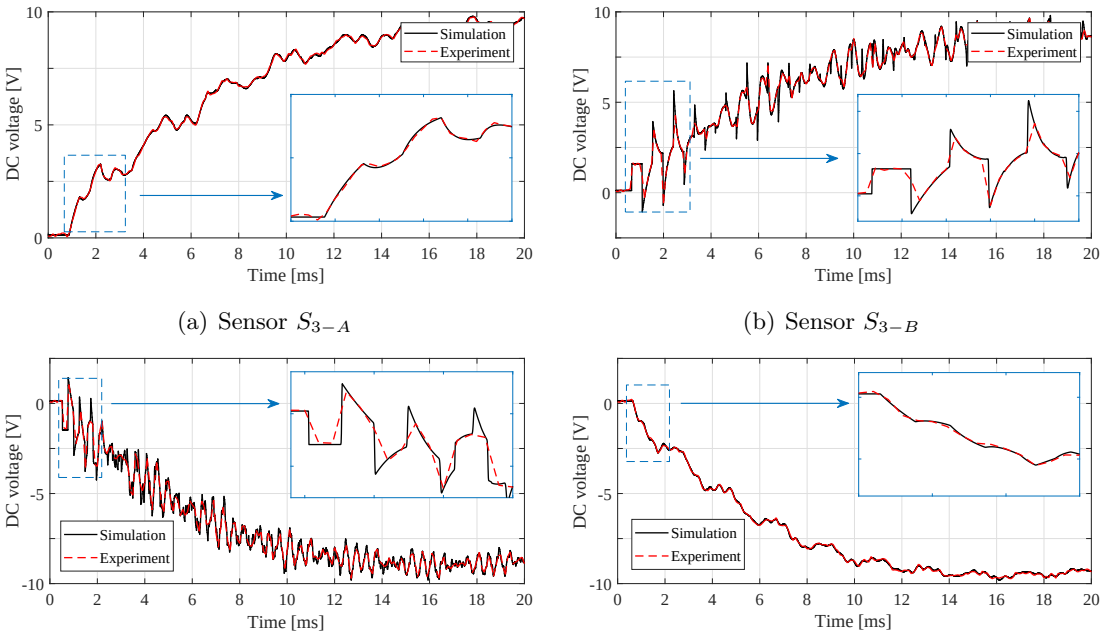
Figure 6.12: Laboratory experimental setup.

In the presented case, the HTM-3 section of the MTDC network (see Figure 6.6) consisting of three segments and four optical sensors was considered. Pre-simulated fault currents at the corresponding four sensing locations along HTM-3 were used to provide replica voltage waveforms generated directly from a multi-function data acquisition card. Prior to testing, the sensors were characterised and calibrated by applying a DC voltage across the piezoelectric transducers (in 1 V steps within the range of ± 10 V). For all the corresponding voltages, the FBG peak wavelengths were recorded and the inverted function was used to calibrate wavelength shifts.

The FBG peak wavelength shifts were monitored by a dedicated commercial FBG interrogation system capable of acquiring the sensors spectra at 5 kHz. As such, the proposed fault detection algorithms could only be demonstrated in practice at this relatively low sampling frequency, resulting in reduced accuracy of fault location. It should be noted, however, that the acquisition frequency limit of 5 kHz is strictly due to the FBG interrogator that was available for the experiments. Higher sampling rates can be achieved when alternative interrogators are employed, such as a solid state interrogator based on an Arrayed Waveguide Grating (AWG) previously developed by the authors [265, 266]. In such a case, the limiting factor for high speed operation would be the performance of the employed data acquisition and signal processing electronics, but scanning frequencies greater than 100 kHz can readily be achieved and the accuracy of the proposed fault location technique could be improved significantly.

6.2.4.4 Experimental results

The measured response from the sensors corresponding to fault scenario F_2 depicted in Figure 6.11 is illustrated in Figure 6.13 (summarised response to all the fault scenarios is presented in Table 6.9). For the ease of comparison both simulation and experimental results are combined in the same figure.



(a) Sensor S_{3-A} (b) Sensor S_{3-B}

(c) Sensor S_{3-C} (d) Sensor S_{3-D}

Figure 6.13: Simulated and experimental DC voltages corresponding to DC scaled fault currents for the fault case corresponding to Figure 6.11.

The DC voltage traces shown in Figure 6.13 correspond to scaled-down replicas of the fault currents. It can be seen that all the dynamic features of the simulated currents are captured with some inevitable level of noise. It should be noted that due to the fault occurrence on the UGC there is a current reversal taking place between sensors S_{3-B} and S_{3-C}. The shape of TWs in terms of frequency of reflections and waveform damping effect is a function of distance to fault and properties of the transmission media. The measurements S_{3-B} and S_{3-C} are the closest to the fault which occurs at UGC (cable segment), and therefore, the TWs appear less damped and with higher frequency of reflection, while the sensors S_{3-A} and S_{3-D} are at the far ends of the OHL lines which results in longer travelling times and higher damping (i.e. travelling wave fronts appear much less 'sharp'). As it is difficult by visual inspection to assess the difference between the simulated and measured response recorded from the sensors, the values

and their impact on the performance of the proposed scheme are better appreciated by investigating the results of Stage I, II and III of the algorithm.

For the experimental voltage traces illustrated in Figure 6.13 the differential voltage V_{diff} has been derived (corresponding to I_{diff} as explained in Section 6.2.1) individually for every pair of adjacent sensors and is depicted in Figure 6.14. The differential voltage calculated for the pair of sensors (i.e. S_{3-B} and S_{3-C}) adjacent to the faulted segment reaches much higher values compared to those related to healthy segments (i.e. S_{3-A}-S_{3-B} and S_{3-C}-S_{3-D}). Therefore Stage I (faulted segment identification) of the proposed fault location algorithm is also verified experimentally.

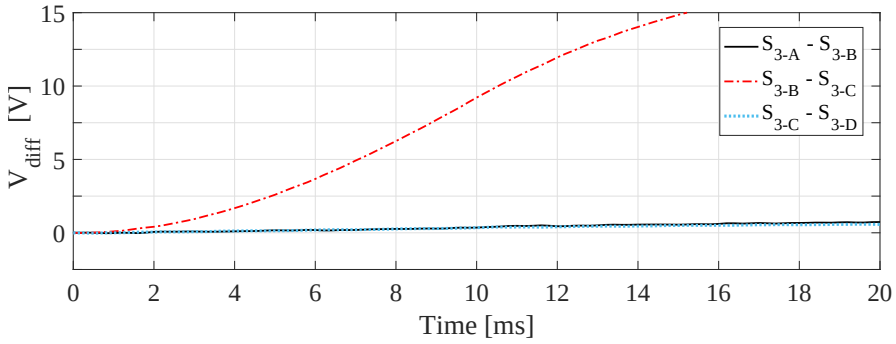


Figure 6.14: Differential voltages calculated from experimental voltage traces.

The measurements from the sensors S_{3-B} and S_{3-C} have been utilised to perform CWT and calculate the arrival time of the TWs. The CWT for such measurements is depicted in Figure 6.15. The time indices for fault location calculation correspond to $t_{1(S_{3-B})} = 0.760$ ms and $t_{1(S_{3-C})} = 0.660$ ms for the sensors S_{3-B} and S_{3-C} respectively.

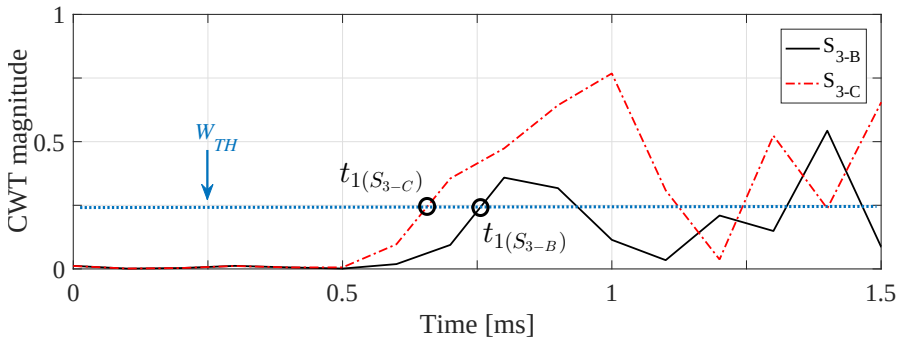


Figure 6.15: CWT calculated from experimental voltage traces from sensors S_{3-B} and S_{3-C}.

The summarised response of the three fault cases is presented in Table 6.9, where they are also compared with the simulation-based performance. As expected, the resulting

accuracy of the experimentally-calculated fault location is slightly lower due to the reduced sampling rate (i.e. 5 kHz), determined by the available interrogation system. The sampling rate has an impact on the Wavelet Transform and the subsequent extraction of time difference $\Delta t_{(S_{UP}-S_{DN})}$ which is used in equation (6.2) for fault distance calculation. This is also verified by observing the extracted time difference $\Delta t_{(S_{UP}-S_{DN})}$ for each fault scenario. For fault scenarios F_1, F_2 and F_3 the simulation based time difference is 0.16834 ms, 0.13183 ms and 0.10996 ms respectively. However, the time-difference values extracted from experiment have larger deviation compared to those obtained from simulation, and hence larger errors. As demonstrated by the simulation results included in Section 6.2.3 much better accuracy can be expected at higher sampling rates. The assumed rate of 135 kHz at which the simulations were performed is technically achievable with commercially available upgraded equipment (this is currently unavailable in our laboratory facilities).

Regarding the faulted segment identification, it is evident from the reported sensors $S_{up} - S_{dn}$ that it has been correctly identified in all three cases, both for simulation and experimental-based analysis. Consequently, it can be concluded that the robustness of the proposed scheme is empirically demonstrated.

Table 6.9: Comparison of experimental and simulations results.

Faults		F1	F2	F3
Error	Sim.	0.4583	-0.2489	0.4806
[%]	Exp.	-1.3254	-1.3415	1.0652
$\lvert\Delta t_{(S_{UP}-S_{DN})}\rvert$	Sim.	0.17037	0.12592	0.11110
$[\mu s]$	Exp.	0.16249	0.10000	0.11250
Reported sensors	Sim.	S_{3-A}, S_{3-B}	S_{3-B}, S_{3-C}	S_{3-C}, S_{3-D}
$S_{UP} - S_{DN}$	Exp.	S_{3-A}, S_{3-B}	S_{3-B}, S_{3-C}	S_{3-C}, S_{3-D}

6.2.5 Discussion

A new fault location scheme suitable for hybrid networks with segments of overhead lines and underground cables has been proposed. The systematic and successful evaluation of the proposed fault location scheme revealed the following merits and features:

- The scheme relies on the measurements obtained from a network of distributed current optical sensors, and it uses travelling wave principle to estimate the fault position.

- The proposed algorithm has been found to successfully identify the faulted segment of the line in all cases while consistently maintaining high accuracy of the fault location estimation across a wide range of fault scenarios including both pole-to-pole and pole-to-ground faults with resistances up to 500 Ω.

- Assuming a sampling rate of 135 kHz, and using the mother wavelet *'coif2'* with scaling factor $\alpha = 4$, the maximum fault location error has been found to be 0.1677% while the average error is 0.0784%.

- The proposed scheme has been found to be robust against noisy inputs for a wide range of mother wavelets and scaling factors.

- The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using a scaled-down laboratory prototype.

- Studies have included the impact of fault current limiting and interruption devices installed both on AC and DC side and the accuracy of the proposed scheme was found to be immune when such devices are utilised.

- A hardware prototype based on FBG optical sensors has been employed to conduct a series of laboratory tests which confirm the practical feasibility of the proposed scheme. A few considerations regarding the installation of the sensors at the transition points of transmission lines and underground cables have also been reported.

6.3 Method 2: Single-ended Pattern Recognition-based Fault Locator

In this part of the thesis, a novel single-ended method for locating faults in MTDC grids is proposed. Different from most of other methods (where the fault current interruption is not considered), the proposed fault location method takes into account that a fault in MTDC systems should be cleared by fault current interruption devices (e.g. hybrid circuit breakers). By utilising currents inside HbCB during the interruption stages, a pattern recognition approach is utilised from which the fault location is estimated. For the proposed algorithm, only a small time window around 5 ms at 96 kHz is required. Training patterns have been obtained by applying a series of different faults within an MTDC grid. The proposed method overcomes the challenges related to travelling waves while the need of line parameters estimation is completely eliminated. Results showed that the proposed idea can accurately estimate the location and type of fault; furthermore, the proposed method is shown to be very effective for highly resistive faults.

6.3.1 Fault current interruption using HbCBs

Following the successful and discriminative fault detection in HVDC grids, the CBs corresponding to the faulted line(s) should be opened to isolate and clear the fault. DC CBs require a special mechanism to drive the fault current to zero and dissipate the energy as there is an absence of a zero crossing point in current.

As also presented in Section 2.5, several CB concepts have been proposed so far in the literature: solid state [85], hybrid [81], super conducting (SC) [90] and resonant [38]. However, all seem to have a similar structure consisting of a commutation path, a switching component for voltage withstand, and an absorption path for dissipating energy [38]. Even though all the schemes have their own advantages and disadvantages, the HbCB has been found to posses the best total efficiency regarding cost, losses and applicability [84]. This is the reason that such a breaker has been considered as the possible candidate for interrupting DC-side faults in future MTDC grids. In fact, HbCB concept has been utilised in many power system studies for MTDC networks, including protection [36, 211], fault analysis [50], modelling [14] and stability [95].

The schematic of HbCB can bee seen in Figure 6.16 and the corresponding fault current interruption process in Figure 6.17. During normal operation, the current flows

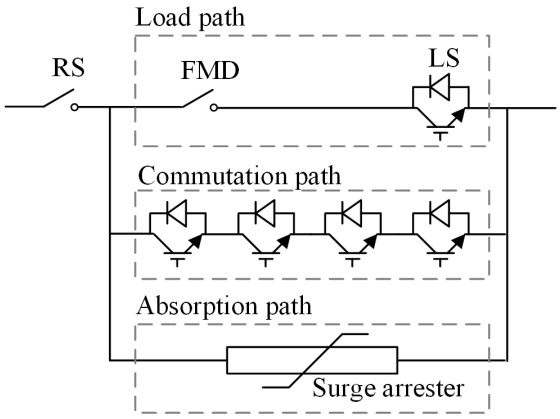


Figure 6.16: Equivalent of hybrid circuit breaker.

through the load path which includes the fast mechanical disconnector (FMD) and the load switch (LS). After a fault occurrence the current inside load path start rising at $t = t_{Rise}$. After a few milliseconds (time to detect the fault) a tripping command is sent to the breaker, the LS opens at $t = t_{LS}$, forcing the current to flow through the commutation path. As no current flows thought the FMD, it can now open at $t = t_{FMD}$. In the next stage, the power electronic valve device in commutation path turns off, which results in over-voltage. From this point, the surge arrester in the absorption path operates, and the current gradually falls to zero while the energy is dissipated. When the current is in a near-zero region, the residual switch (RS) opens at $t = t_{RS}$ and the fault is finally cleared.

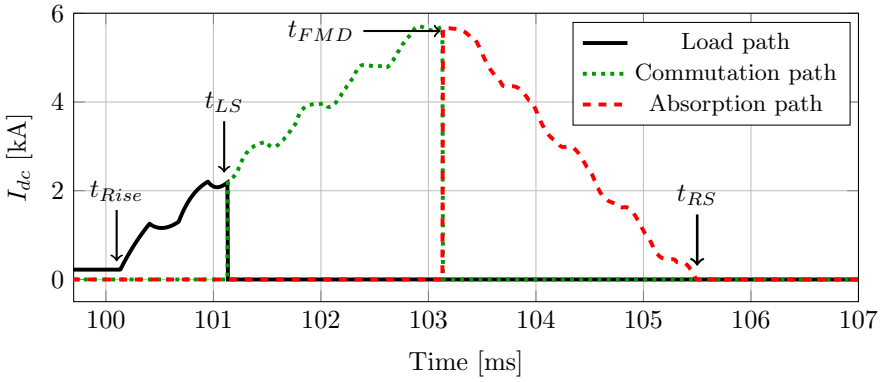


Figure 6.17: Illustration of fault currents inside HbCB during interruption process.

6.3.2 Fault location strategy

The proposed fault location technique utilises the performance of the HbCB during the fault clearance, and takes into account that current measurements (individually for each

path of the HbCBs) can be assessed. This is due to the fact that current measuring devices are installed inside the CB for self protection and control purposes [267].

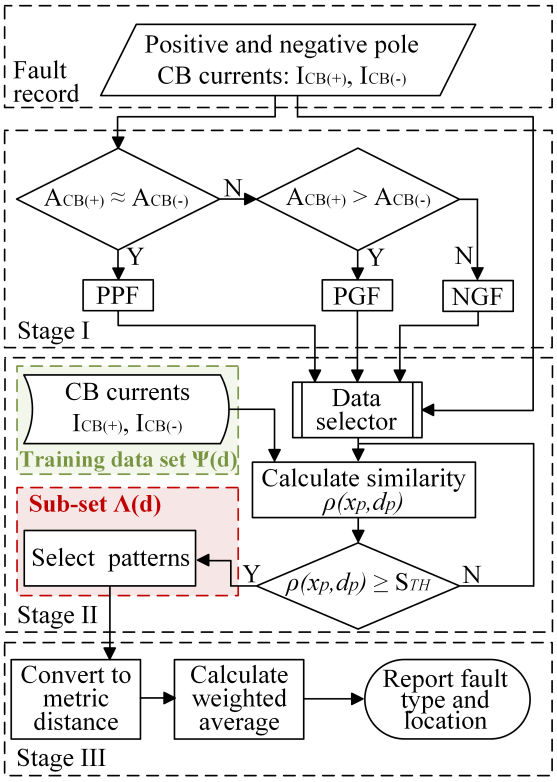


Figure 6.18: Fault location algorithm flow chart.

Such measurements, together with a pattern recognition approach, are used for fault distance estimation. Specifically, by matching the HbCB currents (from a case with unknown fault location) individually for each conduction path, with existing patterns obtained by training data sets, the fault location is calculated. For the implementation of the algorithm, HbCB currents from one end of the line are utilised, both from the positive and negative poles. For enhanced clarity of the algorithm description, a test case of a fault occurring at 100.5 km on a 300 km line is utilised. The sampling frequency for the proposed fault location algorithm is set to 96 kHz which is consistent with the industry standard IEC 61869-9 [226]. The algorithm consists of three stages as illustrated in Figure 6.18 which are explained in detail below.

Stage I - Fault Detection: In the first stage the algorithm determines the type of fault, considering three possibilities: pole-to-pole fault (PPF), positive-pole-to-ground fault (PGF) and negative-pole-to-ground fault (NGF). In Figure 6.19 the currents of positive and negative pole HbCBs ($I_{CB(+)}$ & $I_{CB(-)}$ respectively) are illustrated for the

three considered types of faults.

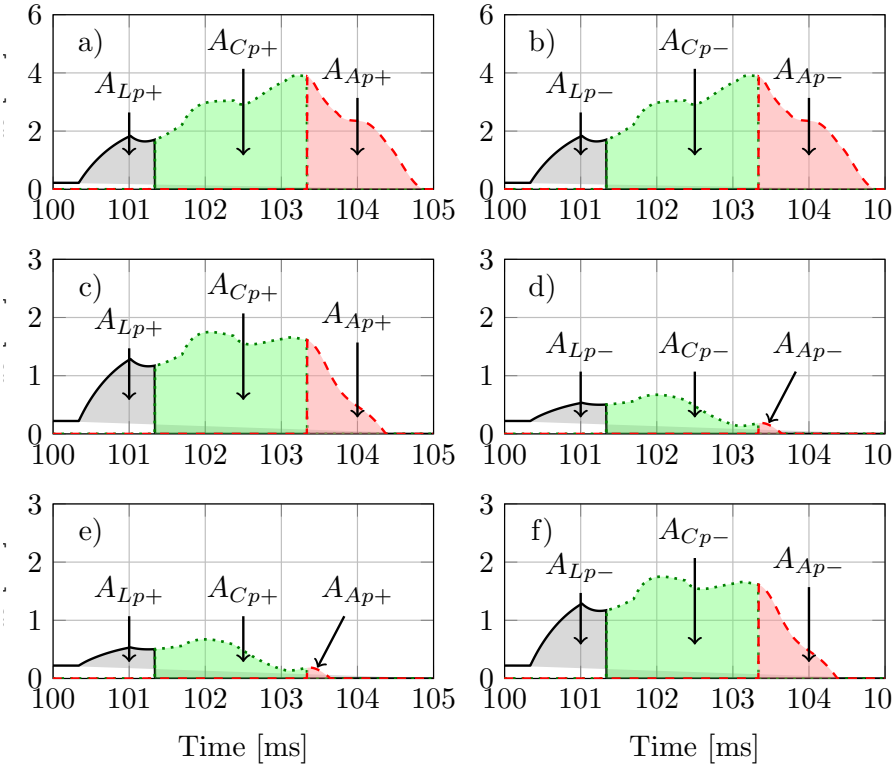


Figure 6.19: Fault classification pattern based on CB currents: a) PPF: positive pole CB, b) PPF: negative pole CB, c) PGF: positive pole CB, d) PGF: negative pole CB, e) NGF: positive pole CB, f) NGF: negative pole CB.

The characteristics of currents corresponding to those faults are very distinctive: in the case of PPF, both positive and negative pole currents are equal (or nearly equal), while for PGFs the faulted pole current is significantly higher than the healthy one. Therefore, a simple comparison of the two currents is generally sufficient to reliably determine the fault type. In order to obtain a single value which can be used in direct comparison between rapidly changing currents, the current time integral (i.e. area under the current waveform) is calculated over the whole duration of the fault. The total area of currents for positive ($A_{I_{CB(+)}}$) and negative ($A_{I_{CB(-)}}$) pole is calculated by

$$A_{I_{CB(+)}} = \underbrace{\int_{t_{Rise}}^{t_{LS}} I_{Lp^+}\,dt}_{A_{Lp^+}} + \underbrace{\int_{t_{LS}}^{t_{FMD}} I_{Cp^+}\,dt}_{A_{Cp^+}} + \underbrace{\int_{t_{FMD}}^{t_{RS}} I_{Ap^+}\,dt}_{A_{Ap^+}} \tag{6.4}$$

$$A_{I_{CB(-)}} = \underbrace{\int_{t_{Rise}}^{t_{LS}} I_{Lp^-}\,dt}_{A_{Lp^-}} + \underbrace{\int_{t_{LS}}^{t_{FMD}} I_{Cp^-}\,dt}_{A_{Cp^-}} + \underbrace{\int_{t_{FMD}}^{t_{RS}} I_{Ap^-}\,dt}_{A_{Ap^-}} \tag{6.5}$$

where I_{Lp}, I_{Cp}, I_{Ap} and A_{Lp}, A_{Cp}, A_{Ap} is the current and its area for load path, commutation path and absorption path respectively. Signs + and − denote the positive and negative pole respectively.

Consequently, as illustrated on the algorithm flowchart in Figure 6.18 (Stage I), a direct comparison of the current areas $A_{I_{CB}(+)}$ and $A_{I_{CB}(-)}$ is used to establish the fault type. If the two areas are almost equal (i.e within a margin of tolerance of ± 10% to account for measurement uncertainties, induced noise and other possible distortion factors) a decision is made that a PPF occurred. Otherwise, it is either PGF or NGF and the decision is made on the basis of the greater of the two current areas.

Stage II -Pattern Recognition: In this stage, a pattern recognition-based method is implemented which uses the fault classification output from Stage I and the training data set $\Psi(d)$ which contains pre-simulated fault current cases (denoted by d) on all MTDC lines and at various locations (the data set creation process is described in detail in section 6.3.4). Initially, the required data sub-set is selected corresponding to the known faulted line and the type of fault identified in Stage I. For PPF and PGF, positive pole HbCB currents ($I_{CB(+)}$) are selected from the set, while for NGF negative pole HbCB currents ($I_{CB(-)}$) are used.

The pattern recognition is achieved by utilising the Pearson's correlation coefficients. Specifically, the Pearson's correlation coefficients of two variables d and x is given by

$$\rho(d_p, x_p) = \frac{1}{N-1} \sum_{k=1}^{N} \left(\frac{d_{k_p} - \mu_{d_p}}{\sigma_{d_p}} \right) \left(\frac{x_{k_p} - \mu_{x_p}}{\sigma_{x_p}} \right) \tag{6.6}$$

where d and x are the variables being compared using N scalar observations. The values μ_d, σ_d, μ_x and σ_x are the mean and standard deviation of d and x respectively. In this application variable d corresponds to N samples of pre-simulated fault current (with known fault location), and x contains N samples of the observed fault current (with unknown fault location). The calculation of the correlation coefficient is performed separately for each of the three conduction paths, i.e. load, commutation and absorption.

The correlation coefficients $\rho(d_p, x_p)$ (with $p = 1, 2, 3$ representing the three conduction paths) are used as a measure of similarity and provide the ability to quantify the correlation of the observed behaviour x (with unknown fault location) with the individual training samples d (with $d \in \Psi(d)$). Correlation values approaching -1 and +1 imply high level of linear correlation (negative and positive respectively), while the values approaching

zero indicate poor correlation. If two cases are similar, values of $\rho(d, x)$ close to 1 are expected. In this application a fixed similarity threshold S_{TH} has been introduced to select closely matching patterns. The patterns with a correlation coefficient of 0.985 and above are included in the sub-set $\Lambda(d)$ which is subsequently used in Stage III to calculate distance to fault according to equation (6.7).

It is also worth clarifying here that the similarity is calculated separately for each of the conduction paths, and if any of the three correlation coefficients $\rho(d_p, x_p)$ $(p = 1, 2, 3)$ exceeds the threshold S_{TH}, the whole case is still selected and included in the matching sub-set $\Lambda(d)$.

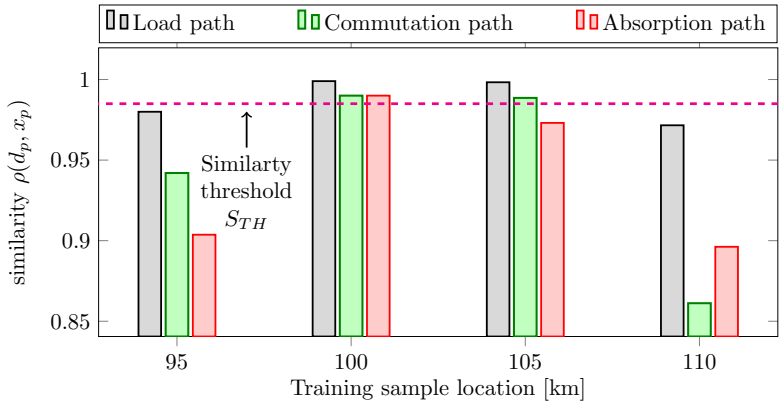


Figure 6.20: Calculated similarity representation of a PPF (at 100.5 km on a 300 km line) and different training samples.

Table 6.10: Similarity values of a PPF (at 100.5 km on a 300 km line) and different training samples.

Distance [km] $\rightarrow$		**95**	**100**	**105**	**110**
Load path	$\rho(d_1, x_1)$	0.9800	0.99900	0.9983	0.9716
Commutation path	$\rho(d_2, x_2)$	0.9420	0.9900	0.9886	0.8612
Absorption path	$\rho(d_3, x_3)$	0.9037	0.9900	0.9731	0.8962

In table 6.10 and Figure 6.20 correlation coefficients of a PPF (located at 100.5 km on a 300 km long Line 1) calculated using four training cases at different fault locations are presented. In this small example the pattern set $\Psi(d)$ contains four HbCB currents resulting from faults at 95, 100, 105 and 110 km from terminal T_3 (see Figure 6.21). The similarity is calculated between these four samples (patterns) and the HbCB currents of the fault occurring at 100.5 km. As can be seen from Figure 6.20, only two cases (i.e. 100 km and 105 km) exceed the similarity threshold S_{TH}. These two samples form the sub-set $\Lambda(d)$ which is used in the fault location calculation. Even though the similarity of the

pattern at 105 km does not exceed the threshold S_{TH} for all the three paths (correlation coefficient for the absorption path is below S_{TH}), the whole case is still selected.

Stage III - Fault Location Calculation: This is the final stage of the algorithm where the fault type (output of Stage I) and its location is reported. The fault location calculation utilises a weighted averaging function based on exponential kernels [268, 269]. After the sub-set of closely matching samples (i.e. sub-set $\Lambda(d)$) has been identified in Stage II, the fault location is calculated by

$$D_f(x) = \frac{\overbrace{\sum_{d\in\Lambda(d,x)} D_f(d)\; e^{-(1-\rho(d_1,x_1))^2}}^{Load\ path} + \overbrace{\sum_{d\in\Lambda(d,x)} D_f(d)\; e^{-(1-\rho(d_2,x_2))^2}}^{Commutation\ path} + \overbrace{\sum_{d\in\Lambda(d,x)} D_f(d)\; e^{-(1-\rho(d_3,x_3))^2}}^{Absorption\ path}}{\underbrace{\sum_{d\in\Lambda(d,x)} e^{-(1-\rho(d_1,x_1))^2}}_{Load\ path} + \underbrace{\sum_{d\in\Lambda(d,x)} e^{-(1-\rho(d_2,x_2))^2}}_{Commutation\ path} + \underbrace{\sum_{d\in\Lambda(d,x)} e^{-(1-\rho(d_3,x_3))^2}}_{Absorption\ path}} \tag{6.7}$$

where $D_f(x)$ is the calculated distance to fault corresponding fault current x, $\Lambda(d)$ is a sub-set of $\Psi(d)$ with selected test patterns similar to case x, $D_f(d)$ is the known fault location of pre-simulated patterns d, and $\rho(d_p, x_p)$ $(p = 1, 2, 3)$ is the Pearson correlation coefficient of the case x and pre-simulated patterns d (calculated separately for each conduction path).

The purpose of the weighted function in (6.7) is to apply more 'weight' (and thus have more influence on the result) to most closely matching patterns in the sub-set $\Lambda(d)$. For this reason the correlation coefficients $\rho(d_p, x_p)$ are converted to form a positive measure of distance between the ideal match (i.e. 1) and the value of $\rho(d_p, x_p)$. This can be seen in the exponent of e in (6.7), i.e. $(1 - \rho(d_p, x_p))^2$. Maximum values in the weighted function are achieved by the elements with the highest values of $\rho(d_p, x_p)$ (i.e. zero distance between actual and test case fault position), and the function should decay exponentially as the distance increases (according to the selected kernel).

6.3.3 Modelling

A five-terminal HVDC grid has been developed and utilised in all case studies as illustrated in Figure 6.21. The network topology has been adopted from the Twenties Project case study on DC grids [163]. There are five MMCs operating at ±400 kV (symmetric monopole), HVCBs and current limiting inductors at each transmission line end. Overhead

lines have been included in the network adopting the distributed parameter model.

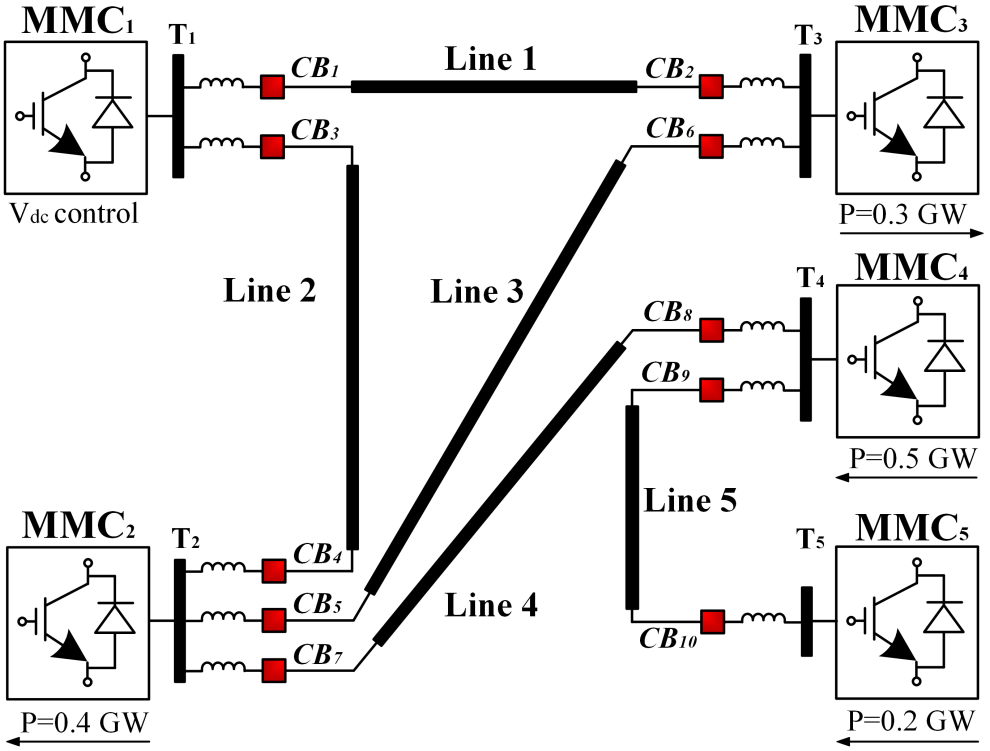


Figure 6.21: Case study five terminal HVDC network.

The HbCB model represents a hybrid design by ABB [82] which, according to the manufacturer, has a potential breaking time of 2 ms while the maximum rating of the breaking current is 9 kA. For the purposes of modelling, all power electronic devices have been modelled as ideal switches with practically zero resistance during their on-state. Additionally, a time delay of 2 ms has been added to represent the operation time of the FMD. The AC and DC network component values are provided in Table 6.11.

6.3.4 Training data

The training patterns (data set $\Psi(d)$) have been generated by simulating PPFs, PGFs and NGFs on all lines at varying distances and fault resistance values. The fault positions have been applied in 5 km increments, and fault resistances covered the range between 0 to 500 Ω (in steps of 25 Ω).

Since the fault detection and protection strategies are out of scope of this work, for each simulated case the HbCB sets have been tripped with the typical time associated with DC protection operation. To represent real-life variations in the tripping time, randomisation of operating time using normal probability distribution has been applied.

Table 6.11: DC and AC network parameters.

Parameter	Value
DC voltage [kV]	± 400
DC inductor [mH]	150
Line resistance [Ω/km]	0.015
Line inductance [mH/km]	0.96
Line capacitance [μF/km]	0.012
Line lengths (1 to 5) [km]	300, 200, 600, 180, 150
AC frequency [Hz]	50
AC short circuit level [GVA]	40
AC voltage [kV]	400
MMC levels	401
MMC arm inductance [p.u.]	0.1
MMC equivalent arm capacitance [μF]	20.84

It has also been assumed that the HbCB current never exceeds 9 kA (maximum breaking capacity).

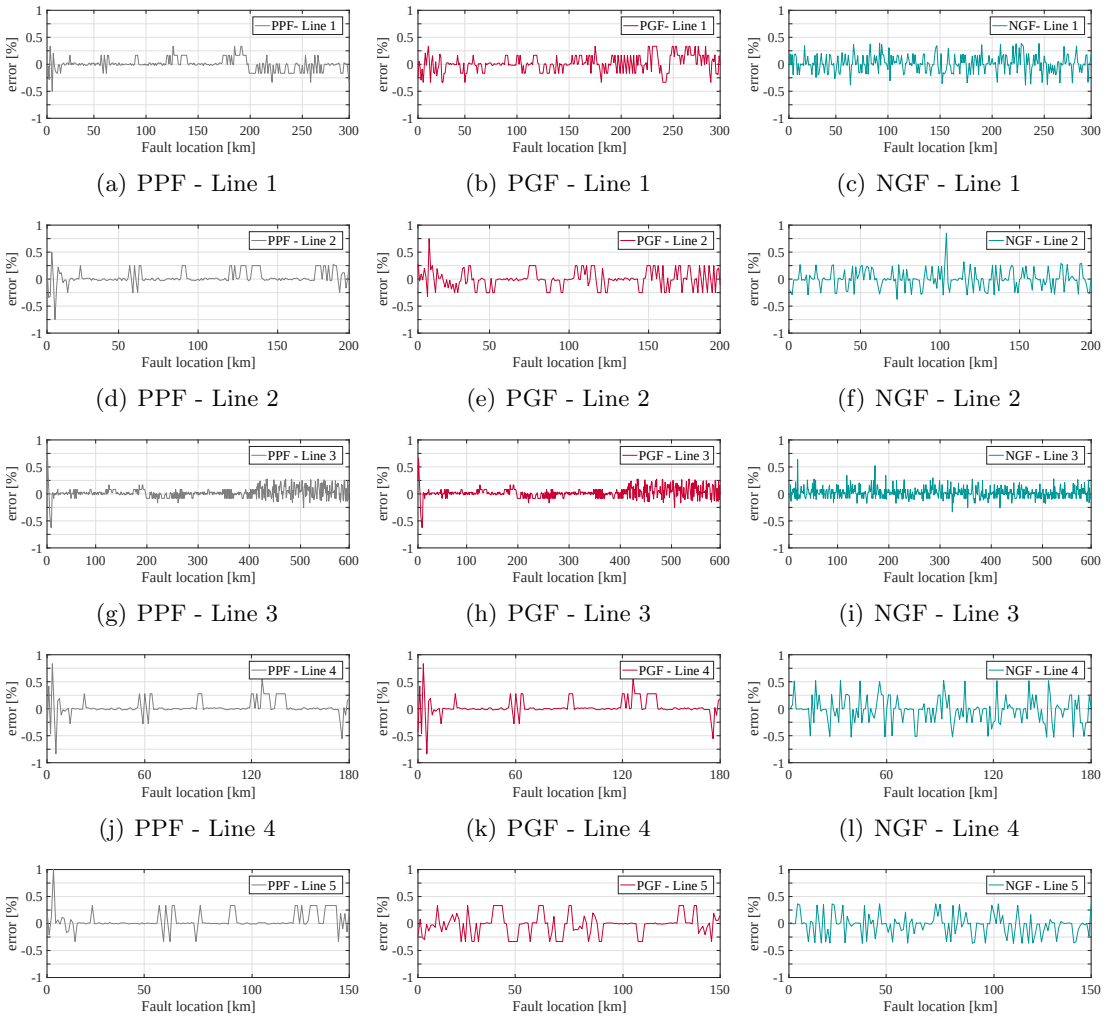
6.3.5 Simulation results

Fault cases have been simulated along all the transmission lines within the HVDC grid, considering a wide range of fault distances and resistances for all type of faults. Specifically, for lines one to five, 290, 190, 590, 170 and 140 cases representing different fault distances have been considered. For each case HbCB currents from the faulted line have been fed into the fault location algorithm. In order to better examine the robustness of the proposed fault location algorithm, artificial white noise has been included to HbCB currents. For every case, the fault location is estimated and the reported errors have been calculated by

$$error\ \% = \frac{D_F - D_F^*}{L_F}\ 100\% \tag{6.8}$$

where D_F is the calculated distance to fault, D_F^* is the actual distance to fault and L_F is the length of the faulted line.

In Figure 6.22 the distribution of errors is illustrated for all the lines and type of faults. The depicted values consider PPFs, PGFs and NGFs with fault resistance of 1 Ω. The statistical report of the fault location results (illustrated in Figure 6.22) are presented in Table 6.12. The table includes minimum, maximum and average values of the errors.



(a) PPF - Line 1 (b) PGF - Line 1 (c) NGF - Line 1

(d) PPF - Line 2 (e) PGF - Line 2 (f) NGF - Line 2

(g) PPF - Line 3 (h) PGF - Line 3 (i) NGF - Line 3

(j) PPF - Line 4 (k) PGF - Line 4 (l) NGF - Line 4

(m) PPF - Line 5 (n) PGF - Line 5 (o) NGF - Line 5

Figure 6.22: Distribution of errors for faults at different lines and fault types.

Table 6.12: Fault location results for different lines and fault types.

Line	Fault type	Error [%]		
		Minimum	Maximum	Average
1	**PPF**	0.00025	0.50000	0.07249
	PGF	0.00038	0.33334	0.11303
	NGF	0.00044	0.39190	0.11830
2	**PPF**	0.00036	0.75000	0.07580
	PGF	0.00028	0.74998	0.11640
	NGF	0.00027	0.85160	0.11870
3	**PPF**	0.00001	0.66566	0.06762
	PGF	0.00001	0.66665	0.07340
	NGF	0.00013	0.63520	0.07344
4	**PPF**	0.00024	0.83334	0.07864
	PGF	0.00028	0.55557	0.18235
	NGF	0.00026	0.52750	0.16890
5	**PPF**	0.00041	0.99998	0.09100
	PGF	0.00026	0.33333	0.12979
	NGF	0.00028	0.36670	0.13680

As can be seen by both Figure 6.22 and Table 6.12, the accuracy of the proposed fault location method achieves values within an acceptable range for a wide range of fault distances for all the lines. Specifically, the minimum value of error recorded is 0.00001 %, while the maximum corresponds to 0.99998 %. Considering average values of errors, the minimum and maximum value have been found to be 0.0676 % and 0.1824 % respectively. Even though it is not included in the tables, the fault type (e.g. PPF, PGF, NGF), as explained in Stage I of the algorithm, has been identified correctly in all cases.

6.3.5.1 Performance with highly resistive faults

The fault location algorithm has been tested under the occurrence of highly-resistive faults. The fault distance scenarios presented previously have been repeated for a wide range of fault resistance values. In particular values of 50, 75, 100, 150, 200, 300, 400 and 500 Ω have been utilised. The resulting average errors corresponding to such cases are presented in Tables 6.13, 6.14 and 6.15, for PPFs, PGFs and NGFs respectively.

Table 6.13: Average error values for PPFs under different fault resistance values.

R_f [Ω]	Line				
	1	**2**	**3**	**4**	**5**
1	0.07249	0.07580	0.06762	0.07864	0.09100
50	0.07487	0.08618	0.07121	0.07953	0.10317
75	0.08311	0.07993	0.06754	0.080517	0.09550
100	0.10640	0.0905	0.09969	0.12292	0.10572
150	0.07801	0.09272	0.12394	0.10441	0.08707
200	0.07612	0.09059	0.14068	0.07895	0.11849
300	0.11445	0.10465	0.09834	0.09236	0.12341
400	0.12828	0.10827	0.09516	0.09200	0.12566
500	0.10813	0.11649	0.08819	0.10076	0.09290

Table 6.14: Average error values for PGFs under different fault resistance values.

R_f [Ω]	Line				
	1	**2**	**3**	**4**	**5**
1	0.11303	0.11640	0.07340	0.18235	0.12979
50	0.12642	0.13199	0.073516	0.20701	0.14114
75	0.11264	0.11958	0.07875	0.13385	0.14848
100	0.12537	0.25127	0.12954	0.20677	0.21236
150	0.12392	0.15432	0.29715	0.12715	0.22931
200	0.17154	0.11748	0.31836	0.21836	0.19943
300	0.18100	0.18500	0.09553	0.27671	0.14541
400	0.17620	0.11711	0.08859	0.17138	0.13753
500	0.18709	0.18039	0.09101	0.16078	0.13086

By observing Tables 6.13, 6.14 and 6.15, the minimum and maximum errors for PPFs are 0.06754 % and 0.14068 % respectively. For PGFs, those errors correspond to 0.0734 % and 0.31836 % and for NGF to 0.07344 % and 0.27524 %. It can be concluded that the

Table 6.15: Average error values for NGFs under different fault resistance values.

R_f [Ω]	Line				
	1	**2**	**3**	**4**	**5**
1	0.11830	0.11870	0.07344	0.16890	0.13680
50	0.13231	0.13460	0.07355	0.19174	0.14877
75	0.11789	0.12194	0.17879	0.093014	0.15650
100	0.13122	0.21079	0.12961	0.20274	0.22383
150	0.12969	0.15737	0.12711	0.27524	0.24169
200	0.17954	0.11980	0.12310	0.19487	0.21020
300	0.18943	0.18865	0.09559	0.25630	0.15326
400	0.18442	0.11942	0.08864	0.17191	0.14495
500	0.19581	0.18395	0.09106	0.17712	0.13792

proposed alogrithm can maintain a relatively low error even with highly resistive faults up to 500 Ω and the accuracy is not compromised.

6.3.5.2 Impact of Sampling Frequency

In order to investigate the impact of sampling frequency on the proposed fault location technique, studies on PPFs (with $R_f = 1$ Ω) have been repeated for different sampling frequencies. The resulting average errors are presented in Table 6.16.

Table 6.16: Average error values for PPFs for different sampling frequencies.

f_s [kHz]	Line				
	1	**2**	**3**	**4**	**5**
5	0.7669	0.7351	0.6188	0.6912	0.9901
10	0.5042	0.4773	0.4686	0.4884	0.8891
20	0.3085	0.4008	0.4233	0.3688	0.5069
30	0.1678	0.2085	0.2488	0.2619	0.3141
40	0.1316	0.1479	0.1704	0.2304	0.2595
50	0.0953	0.0918	0.0784	0.1030	0.1131
96	0.0725	0.0758	0.0676	0.0786	0.091
100	0.0724	0.0758	0.0676	0.0786	0.0909
200	0.0723	0.0756	0.0675	0.0785	0.0908
500	0.0708	0.0756	0.0654	0.0768	0.0888

By observing the table it can bee seen that the dependency of the accuracy on the sampling frequency is considerable for frequencies below 30 kHz. This is due to the fact that the entire current interruption process lasts about 5 ms; therefore with low sampling frequency only a few points can be extracted. The sampling frequency can be set to a minimum around 50 kHz without the accuracy being compromised. Additionally, it evident that exceeding sampling rate above 96 kHz results in insignificant improvement of fault location accuracy.

6.3.6 Discussion

A new learning-based fault location method for locating fault in MTDC networks, based on the current measurements of HbCBs during the interruption process and a pattern recognition approach, has been proposed. The following remarks can be pointed out:

- The proposed scheme requires training data. These have been generated taking into account a wide range of fault distances and resistance values. Additional artificial noise has been added to represent uncertainties and any other possible source of noise.
- The sampling frequency was set to 96 kHz according to IEC 61869-9.
- The fault location method was found to be capable of classifying PPFs, PGFs and NGFs while the accuracy achieves values within an acceptable range even for highly resistive faults up tp 500 Ω.
- The proposed method overcomes the challenges related to travelling waves and reflectometry while the need of line parameters estimation is completely eliminated.
- Further sensitivity analysis revealed that a minimum sampling frequency of 50 kHz would be sufficient for this application. This is due to the fact that the current interruption process lasts about 5 ms. Consequently, when adopting lower sampling frequencies the number of extracted data is not sufficient to execute the algorithm efficiently.
- As in any learning-based scheme, there is always a challenge for obtaining training data.
- The minimum and maximum errors for PPFs are 0.06754 % and 0.14068 % respectively. For PGFs those errors correspond to 0.0734 % and 0.31836 % and for NGF to 0.07344 % and 0.27524 %.

6.4 Summary

In this chapter the challenges and requirements with regards to fault location in HVDC networks have been analysed. It has been pointed out that fault location is mostly related to accuracy rather than speed of calculation. The accuracy of fault location is of major

importance as it will enable faster system restoration, diminish the power outage time, and therefore enhance the overall reliability of the system.

A literature review on the existing and proposed fault location techniques revealed that there is a wide selection of options which can accurately calculate the location of a fault. All have their own advantages and disadvantages, which have been pointed out.

From the research point of view, this thesis has contributed to the fault location problem by introducing two major ideas. The first one is related to a special fault location challenge where non-homogeneous transmission feeders are involved (i.e. segments of underground cables and overhead lines are combined in one feeder). In such networks, challenges for TW-based methods arise from the fact that the speed of electromagnetic wave propagation is not uniform, additional reflections are generated at the junction points, and there is an increased difficulty in identifying the faulted segment. The proposed TW-type method uses Continuous Wavelet Transform (CWT) applied to a series of line current measurements obtained from a network of distributed optical sensors. The technical feasibility of optically-based DC current measurement is evaluated through laboratory experiments using Fibre-Bragg Grating (FBG) sensors and other commercially available equipment), The proposed algorithm has been found to successfully identify the faulted segment of the line in all cases while consistently maintaining high accuracy of the fault location estimation across a wide range of fault scenarios including both pole-to-pole and pole-to-ground faults with resistances up to 500 Ω. Additionally, the proposed scheme has been found to be robust against noisy inputs for a wide range of mother wavelets and scaling factors. Studies have included the impact of fault current limiting and interruption devices installed both on AC and DC side and the accuracy of the proposed scheme was found to be immune when such devices are utilised.

The second solution for fault location utilises a learning-based approach. Specifically, by utilising currents inside HbCB during the interruption stages, a pattern recognition approach is utilised from which the fault location is estimated. For the proposed algorithm, only a small time window around 5 ms is required. Training patterns have been obtained by applying a series of different faults within an MTDC grid. Results showed that the proposed idea can accurately estimate the location and type of fault, while it is also very effective for highly resistive faults. The required training data have been generated taking into account a wide range of fault distances and resistance values. Further sensitivity analysis revealed that a minimum sampling frequency of 50 kHz would be sufficient for

this application. This is due to the fact that the current interruption process lasts about 5 ms. Consequently, when adopting lower sampling frequencies the number of extracted data is not sufficient to execute the algorithm efficiently. It has been found that the proposed method overcomes the challenges related to travelling waves while the need of line parameters estimation is completely eliminated.

Chapter 7

Conclusions and Future Work

This chapter concludes the entire thesis by summarising and highlighting the findings and contributions of the research. Additionally, based on this thesis, future work is also suggested.

7.1 Summary and Key Outcomes

Chapter 1 presented evidence for the growing need for HVDC interconnections both as individual links (i.e. point-to-point) and multi-terminal configurations. It is expected that the HVDC-based power transmission will be one of the key players for the realisation of Supergrids. It has been pointed out that the challenges of fault-related issues is of major importance. Emphasis has been given to protection and fault location applications of DC-side faults. These are of major importance as they can reassure the safe and secure operation of MTDC grids, accelerate restoration, minimise repair cost, reduce the system down-time and increase the overall availability and reliability of the HVDC-based transmission.

Chapter 2 presented a comprehensive literature review of the background material reagrding HVDC grids. The review included network architectures, converter designs and configurations, transmission lines and the available grounding options. Additionally, the review included important material related to DC protection such as state-of-the-art circuit breakers and the available measuring techniques for DC voltage and current measurements.

Chapter 3 described the outcomes of a detailed, theoretical but also simulation-based transient analysis of DC-side faults. The characterisation has been carried out considering various states of the converters during DC-side faults, their dependencies on converter topology, fault type, fault resistance and operating conditions. The analysis took place considering mainly DC-side faults from the converter point of view, analysing the stages and the corresponding equivalent circuits on which faults (pole-to-pole and pole-to-ground) can be decomposed. From the analysis the following observations can be reflected:

- Pole-to-pole faults are considered more severe due to the fact that they force the system to collapse, but they are less likely to occur. On the other hand, pole-to-ground faults are less harmful but more likely to happen.

- It is necessary to isolate the DC-side faults to prevent voltage collapse and before excessive current flow through system components (e.g. power electronic vales). This means that the DC-side faults have to be cleared within a few milliseconds, including fault detection, localisation and isolation.

- DC fault signatures are predominately defined by the energy contained on the DC side at the moment of fault inception. Therefore, the AC side does not significantly contribute to the DC fault current during the first few milliseconds after the fault.

- The fault position appears to have the same effect on both types of faults, i.e. fault peak and rate of change of current are both reduced with distance to fault. In particular, for pole-to-pole faults this is clearly evident as the line impedance is the main current limiting factor. However, for pole-to-ground faults the fault resistance is considered as one of the main influencing elements so the impact of fault position cannot be pre-determined.

- System behaviour is highly dependent on earthing arrangements implemented and needs to be taken into account when developing operational procedures including fault detection and protection strategies.

- Different converter architectures introduce different fault signatures the first few milliseconds of DC-side faults. This is due to the different arrangement and allocation of power components (e.g. capacitors, inductors, etc.) which make the equivalent DC energy to vary at the moment of fault inception.

The comprehensive fault characterisation presented in this chapter acted as preliminary knowledge for the design of DC side fault-related systems for HVDC networks.

Chapter 4 presented a theoretical and simulation-based analysis of fast fault-related transient phenomena in MTDC networks. It has been found that such studies do not depend on the converter topologies (or generally on the power source), but instead they are more dependent on components taking place within a DC network (after the converter DC terminals) such as current limiting inductors, cables/lines and DC breakers. Additionally emphasis has been given to signal processing methods for obtaining a deeper insight of nature of the faults. The investigation revealed the following remarks:

- Travelling waves can be detected both in DC voltage and current signatures.
- The fault resistance can decrease the amplitude of travelling waves. Extremely high values of fault resistance can minimise the sharpness of travelling waves, which in some cases it can be difficult to discriminate them from noise or other disturbances.
- Line termination (e.g. resistive, inductive, capacitive) plays a significant role to the shape of travelling waves.
- The point of measurement affects on a significant degree the captured fault signatures. As a result, depending on the point of measurement different fault-related functions (e.g. protection) can be realised accordingly.
- The deliberate inclusion of additional inductance not only limits the rate of change of DC current but also the resulting DC voltage signatures (and the fact that they may be different depending on fault location and known values of inserted inductance at line terminals) can help to achieve a discriminative non-unit type protection.
- A series of DC-side faults within an MTDC network has been applied. Considering a single point of observation, the resulting signatures and their corresponding analysis has been found to be capable of distinguishing the nature and location of the faults.
- Signal processing methods have been introduced. It has been demonstrated that conventional signal processing techniques such as Fourier Transform are not suitable for fast and simultaneous time-frequency analysis. On the contrary, it has been

shown that Wavelet Transform is a powerful tool for analysis of fast transient phenomena such as DC-side faults.

- Two categories of wavelet transform can be distinguished: Continuous Wavelet Transform and Discrete Wavelet Transform (DWT). The selection between CWT and DWT is a trade-off between time accuracy of the wave detection, and processing resources and their associated time delays. In the case of CWT, the accuracy of the wave time detection is better than for DWT techniques but the power requirements are higher. This is the reason that CWT is preferred for fault location applications, where the computational time is not crucial. However, DWT is computationally more efficient, which enables faster wave detection. As a result, DWT is considered more suitable for power system protection applications.

- The selection of mother wavelet and scaling factor α is of major influence to the resulting signatures both in time and amplitude. Attention should be paid to lower scales where noise in the measurements can be amplified and cannot be distinguished from other power system transients.

Chapter 5 presented the challenges and requirements with regards to protection in HVDC grids. DC grid protection philosophy is well-aligned with the objectives of AC grid protection which include reliability, selectivity, stability, speed and sensitivity. However, a few essential differences have been pointed out which mainly determine the time window of events. As such, it has been demonstrated that DC-side protection should be fast enough to isolate DC-side faults in around 5 milliseconds (including detection and interruption).

Based on such requirements, two different methods have been introduced. The first one, termed as 'Single-ended Differential Protection' utilises the principle of distributed optical sensing. After the thorough evaluation of the proposed scheme, the following remarks can be pointed out:

- The proposed scheme is highly sensitive, discriminative and fast both for pole-to-pole and pole-to-ground faults.

- The proposed scheme has been found to be stable during external faults occurring on adjacent lines or busbars.

- The performance of the scheme has been demonstrated in detailed transient simulations, and further validated using a scaled-down laboratory prototype.
- The key advantages of single-ended instantaneous current measurement have been outlined which result in enhanced reliability, superior stability, and high speed of operation.
- The design, construction and operating principles of the hybrid optical sensors have been discussed with specific emphasis on the practical aspects of implementing such sensors in distributed monitoring of transmission lines.
- Excessive noise of optically-based measurements requires denoising which has been implemented using Wavelet multi-resolution analysis and reconstruction of the signal. Other methods could be also used (e.g. low-pass filter).

The second solution is a new centralised scheme which utilises the principles of busbar differential protection and travelling waves. The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using a scaled-down laboratory prototype. This prototype provides a high level of confidence that the proposed method is practical, considering realistic measurements, communications and computation. After the successful evaluation of the proposed scheme the following conclusions can be pointed out:

- The scheme requires communication within DC substation which has been enabled with IEC 61850.
- It has been found that the recommended frequency of 96 kHz reported in IEC 61869-9 is suitable for the detection of fast transient phenomena in HVDC grids, and hence can be utilised for the implementation of fast and reliable DC busbar and line protection incorporating travelling waves.
- It has been found that the proposed scheme can provide fast and discriminative protection for busbar and line faults (both solid and highly resistive), including multiple faults occurring simultaneously on different transmission lines.
- The use of line terminating inductors leads to the limitation of the current rise in case of a fault, assists in the discrimination of the faulted line and also prevents the currents from exceeding the breaking capability of the CB.

- Further sensitivity analysis revealed that a minimum sampling rate of 60 kHz would be adequate for this application.

In Chapter 6 the challenges and requirements with regards to fault location in HVDC networks have been analysed. It has been pointed out that fault location is mostly related to accuracy rather than speed of operation. The accuracy of fault location is of major importance as it will enable faster system restoration, diminish the power outage time, and therefore enhance the overall reliability of the system.

A literature review on the existing and proposed fault location techniques revealed that there is a wide selection of options which can accurately calculate the location of a fault. All have their own advantages and disadvantages, which have been pointed out. Some of the main challenges include the need of time-synchronised measurements, requirements of high sampling rates and the utilisation of external equipment.

From the research point of view, this thesis has contributed to the fault location problem by introducing two major ideas. The first one is related to a special fault location challenge where non-homogeneous transmission feeders are involved (i.e. segments of underground cables and overhead lines are combined in one feeder). In such networks, challenges for TW-based methods arise from the fact that the speed of electromagnetic wave propagation is not uniform, additional reflections are generated at the junction points, and there is an increased difficulty in identifying the faulted segment. The scheme relies on the measurements obtained from a network of distributed current optical sensors, and it uses travelling wave principle to estimate the fault position. The performance of the scheme has been demonstrated in detailed transient simulation, and further validated using a scaled-down laboratory prototype. A hardware prototype based on FBG optical sensors has been employed to conduct a series of laboratory tests which confirm the practical feasibility of the proposed scheme. A few considerations regarding the installation of the sensors at the transition points of transmission lines and underground cables have also been reported. The successful evaluation revealed the following merits:

- The proposed algorithm has been found to successfully identify the faulted segment of the line in all cases while consistently maintaining high accuracy of the fault location estimation across a wide range of fault scenarios including both pole-to-pole and pole-to-ground faults with resistances up to 500 Ω.
- Assuming a sampling rate of 135 kHz the maximum fault location error has been found to be 0.1677% while the average error is 0.0784%.

- The proposed scheme has been found to be robust against noisy inputs for a wide range of mother wavelets and scaling factors.
- Studies have included the impact of fault current limiting and interruption devices installed both on AC and DC side and the accuracy of the proposed scheme was found to be immune when such devices are utilised.

The second solution for fault location utilises a learning-based approach. Specifically, by utilising currents inside a hybrid DC circuit breaker during the interruption stages, a pattern recognition approach is utilised from which the fault location is estimated. For the proposed algorithm, only a small time window around 5 ms is required. Training patterns have been generated assuming a wide range of fault distances and resistance values. Additional artificial noise has been added to represent uncertainties and any other possible source of noise. Simulation-based analysis demonstrated the following features:

- The fault location method was found to be capable of classifying pole-to-pole, positive pole-to-ground and negative pole-to-ground faults. The accuracy achieved values within an acceptable range even for highly resistive faults up tp 500 Ω.
- The proposed method overcomes the challenges related to travelling waves and reflectometry while the need of line parameters estimation is completely eliminated.
- Further sensitivity analysis revealed that a minimum sampling frequency of 50 kHz would be sufficient for this application. This is due to the fact that the current interruption process lasts about 5 ms. Consequently, when adopting lower sampling frequencies the number of extracted data is not sufficient to execute the algorithm efficiently.
- As in any learning-based scheme, there is always a challenge for obtaining training data.
- The minimum and maximum errors for pole-to-pole faults are 0.06754 % and 0.14068 % respectively. For positive pole-to-ground faults, those errors correspond to 0.0734 % and 0.31836 % and for negative pole-to-ground faults to 0.07344 % and 0.27524 %.

7.2 Future Work

After the successful development and evaluation of the proposed protection and fault location schemes, it has been identified that there are still several research directions to be explored. For further work with regards to DC-side faults in MTDC networks the following remarks may be consulted:

7.2.1 Development of back-up protection schemes

The proposed protection schemes presented in Chapter 5 are considered to be primary. It is also concluded by the literature review that most of the research is focused on the primary protection systems. Consequently, more research should be steered towards the development of back-up protection systems for MTDC networks.

7.2.2 Assistance from communication Llinks

It has been pointed out that most of the research is focused on non-unit protections schemes. However, the assistance from communication links should be investigated thoroughly to identify the potential merits for protection and fault location applications. The investigation should include the identification of optimal network infrastructure but also the analysis of the potential challenges with regards to decoding and encoding, time latencies and compliance with IEC 61850 and other standards.

7.2.3 Further investigation of IEC 61689

It has been demonstrated in Chapter 5.4 the the recommended sampling frequency of 96 kHz for HVDC applications reported in IEC 61689 is sufficient enough for analysing fast transient phenomena in HVDC systems. The recommended sampling frequency should be further investigated to identify the limitations with regards to time and amplitude accuracy in conjunction with increasing levels of signal-to-noise ratio. This should be tested for various application such as protection, fault location and control.

7.2.4 Improvement of optical sensing technology

Optical sensing technology (notably distributed sensing) is a powerful tool for power system monitoring. Such technology has been used for development of both protection and fault location schemes presented in this thesis. The basic principles and technical

guidelines for realising such technology have been described in Chapters 5.3 and 6.2. It is recommended that future research should focus on the design and implementation of dedicated sensors for DC voltage and current measurements along HVDC feeders. Emphasis should be given to the achievement of high sampling rates with low signal-to-noise ratio. Some major technical challenges are expected to involve the impact of the properties of magnetic materials, optical interrogators, requirements of voltage insulation properties and signal amplification.

7.2.5 Further investigation of additional fault types

The proposed protection and fault location schemes presented in this thesis were focused on non-arc faults. However, further investigation should be carried out considering arc faults. Moreover, faults on the AC side of the system should be studied and their impact on protection and control should be investigated.

7.2.6 Effect of non-optimal conditions

Further research should be carried out considering the effect of non-optimal conditions, such as the degradation of equipment (e.g. DC breakers) and non-uniform behaviour of measurements.

7.2.7 Interoperability with flexible power transmission

Voltage source converters have significantly evolved to perform advanced power system operations. These include fault ride through of DC-side faults, rapid change of operating modes and other flexible operations. During such operations the physical quantities in the system will be disturbed and therefore protection and control devices can be spuriously tripped. It is therefore proposed that protection and control devices shall be equipped with advanced functions to correctly identify those disturbances and adopt their behaviours. A research approach could be the internal communication between converters and protective relays within a DC substation. This could be an elevation of the proposed scheme presented in Chapter 5.4.

7.2.8 Utilisation of learning-based methods

Learning-based approaches for protection and fault location applications has been widely used in AC power systems. However, there is a significant lack of their utilisation for

problem solving in HVDC systems. It is suggested that potential merits can arise from the utilisation of learning based methods for HVDC applications. Learning based methods shall be used mainly for fault location applications where the time is not critical and the margin for error is greater.

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