Research and Development of Diagnostic Algorithms to Support Fault Accommodating Control for Emerging Shipboard Power System Architectures

Ruturaj R. Soman

A thesis submitted for the degree of Doctor of Philosophy to

Institute for Energy and Environment

University of Strathclyde

June 2013

II

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed:

Date:

Abstract

The U.S. Navy has proposed development of next generation warships utilising an increased amount of power electronics devices to improve flexibility and controllability. The high power density finite inertia network is envisioned to employ automated fault detection and diagnosis to aid timely remedial action. Integration of condition monitoring and fault diagnosis to form an intelligent power distribution system is anticipated to assist decision support for crew while enhancing security and mission availability.

This broad research being in the conceptual stage has lack of benchmark systems to learn from. Thorough studies are required to successfully enable realising benefits offered by using increased power electronics and automation. Application of fundamental analysis techniques is necessary to meticulously understand dynamics of a novel system and familiarisation with associated risks and their effects. Additionally, it is vital to find ways of mitigating effects of identified risks.

This thesis details the developing of a generalised methodology to help focus research into artificial intelligence (AI) based diagnostic techniques. Failure Mode and Effects Analysis (FMEA) is used in identifying critical parts of the architecture. Sneak Circuit Analysis (SCA) is modified to provide signals that differentiate faults at a component level of a dc-dc step down converter. These reliability analysis techniques combined with an appropriate AI-algorithm offer a potentially robust approach that can potentially be utilised for diagnosing faults within power electronic equipment anticipated to be used onboard the novel SPS.

The proposed systematic methodology could be extended to other types of power electronic converters, as well as distinguishing subsystem level faults. The combination of FMEA, SCA with AI could also be used for providing enhanced decision support. This forms part of future research in this specific arena demonstrating the positives brought about by combining reliability analyses techniques with AI for next generation naval SPS.

Acknowledgments

Foremost, I would like to thank Prof. Stephen McArthur for giving me an opportunity to undertake a PhD programme at the University of Strathclyde and for his constant support, supervision and encouragement. I would also like to thank Mr. Euan Davidson for his valuable inputs and guidance during the entire research work. Thanks are due to Dr. John Fletcher for his unwavering help with technical issues and especially hardware tests. I would also like to thank Mr. Alex Mair for expert advice on Weka.

Further, I would like to thank researchers at Center for Advanced Power Systems (CAPS) – Florida State University (FSU), USA, Dr. Dave Cartes, Dr. Sanjeev Srivastava and Dr. Karl Schoder for their periodic assistance during the entire PhD research.

I am grateful to my family, for their untiring, unconditional love and support, without which I would have accomplished nothing.

Contents

List of Figures

List of Tables

List of Equations

Glossary of Abbreviations

AC	Alternating Current
ACZED	AC zonal electrical distribution system
AI	Artificial Intelligence
CAPS	Centre for Advanced Power Systems
CBM	Condition Based Maintenance
CDG	Component Dependency Graphs
DC	Direct Current
DCZED	DC zonal electrical distribution system
DF	Dissipation Factor
EMTDC	Electromagnetic Transient and DC
ESR	Effective Series Resistance
FA	Fault Accommodation
FACS	Fault Accommodating Control System
FMEA	Failure Mode and Effects Analysis
FFT	Fast Fourier Transform
F-FMEA	Functional FMEA
FMECA	Failure Mode Effect and Criticality Analysis
FPGA	Field Programmable Gate Array
FSU	Florida State University
GA	Genetic Algorithm
GCM	Generalized Connection Matrix
GIS	Geographical Information System
GTO	Gate Turn Off thyristor
H-FMEA	Hardware FMEA
HIL	Hardware In Loop
IFTP	Integrated Fight Through Power
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
IPS	Integrated Power System
JADE	Java Agent Development Environment
LC	Inductor-Capacitor
LSA	Latent Semantic Analysis
MAS	Multi Agent System
MM	Multiple Model
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MVAC	Medium Voltage AC
MVDC	Medium Voltage DC
NLP	Natural Language Processing
NN	Neural Network
ONR	Office of Naval Research
PART	Projective Adaptive Resonance Theory
PCA	Principal Component Analysis
PEBB	Power Electronics Building Blocks
PEC	Power Electronic Converter
PMS	Platform Management System
PSCAD	Power System Computer Aided Design
RMS	Root Mean Square

RPN	Risk Priority Number
RTDS	Real Time Digital Simulator
SCA	Sneak Circuit Analysis
SPS	Shipboard Power System
SVM	Space Vector Machines
US	United States
UML	Unified Modelling Language
VTB	Virtual Test Bed

Chapter 1 Research Background

1.1 Introduction to research arena

The preference for integrated electric propulsion architectures aboard naval vessels has been proposed since approximately 1995 onwards through a series of papers titled "The Electric Warship" mainly by C.G. Hodge [1-7]. This research forms one of the primary works that provide the impetus to move from conventional mechanical propulsion to fully integrated electrical propulsion [1]. The authors make the case for DC power distribution aboard modern warships providing meticulous calculations to compare the benefits of DC over AC [2], [6]. The papers elaborate on advances in motors (especially permanent magnet technology) to help increase propulsion efficiency as well as energy storage issues to support advanced high power weaponry. The recurring emphasis however, is on the extensive use of power electronics devices as the major enabling technology [1], [3-5], [7] and [8]. The work by Hodge et al. forms the base of this research field and the recommendations can be summarised into three parts.

1. Move from standard mechanical propulsion to electric propulsion for naval vessels.
2. Preference for DC power distribution along the ship.
3. Extensive use of power electronics devices onboard, especially converters.

Progressing on from this preliminary research, concepts such as integrated propulsion system and medium voltage AC and/or DC zonal distribution have come into prominence. The U.S. navy has proposed designs of future warships that heavily rely on power electronics devices and novel distribution architectures [9]. Next generation naval vessels have been envisioned with a reduction in crew (by 75% - 90% [10]) thereby implying increased computational intelligence and automation to achieve mission goals with high efficiency. This puts an emphasis on the system being able to provide decision support and aid remedial action in contingency scenarios.

The overall research efforts are along the lines of the U.S. Office of Naval Research's (ONR) control challenge problem statement, wherein the essential goal is [11];

"To provide continuous mobility, power, and thermal management for shipboard combat systems despite major disruptions involving cascading failures."

As such, the control architecture is expected to accurately diagnose faults and mitigate the risks posed thereby effectively accommodating disturbances within the shipboard power system (SPS). This requirement gives rise to a term, fault accommodating control system (FACS), which could be defined as a system capable of the following automated tasks:

1. Accurate fault diagnosis which includes fault detection and identification.
2. Timely fault isolation which is a task of the onboard protection system.
3. Remedial action which aims at reconfiguring the system in order to best utilise available resources to achieve the present mission's goal(s).

Keeping in mind the need for decision support alongside increased automation, leads this research into the realm of artificial intelligence (AI) based capabilities. The search for suitable AI technique(s) to diagnose faults aboard a novel shipboard power distribution system requires meticulous understanding of AI used on general power system applications such as terrestrial networks. From this stage, the study continues into checking feasibility of known AI methods to diagnose faults for a relatively unknown system or the need to develop new diagnostic techniques. Devising fault diagnosis techniques to differentiate and identify various types of disturbances in the novel shipboard architecture forms the driving requirement for this research and delivers the underlying novelty in the work.

1.2 Justification and rationale for research

The development of DC power distribution SPS architectures is still in a conceptual phase with a lack of actual benchmark systems. Research is ongoing in this field with work centred on:

- Analysing the fundamental aspects of such a paradigm shift.
- Issues related to supervisory control and decision support capabilities.
- Protection coordination and automation.
- Power system reconfiguration and restoration.

Detailed studies need to be conducted to understand fundamental differences between terrestrial power networks, conventional SPS and the proposed SPS. The overall aim of this research is the development of the FACS, for which a detailed study needs to be conducted across inter-related domains.

The emphasis on increased use of power electronics devices and automation for the proposed architecture makes it imperative to understand and mitigate risks. As a result, this requires studies within reliability analyses and power electronics domains. FMEA and SCA are used in this research which falls under the reliability analyses domain.

Another vital requirement is the establishment of a meticulous research methodology which could be ideally generalised to study similar envisioned SPS of next generation warships. An ideal approach would be one that takes into account risks at all levels i.e. component, device, sub-system and system as a whole, then helps highlight pertinent disturbances on which AI based diagnostics could be focussed. Additional issues such as decision support for onboard crew also need to be addressed for which AI techniques could be employed as well. This forms part of future planned research in this particular field.

1.3 Research novelty and contribution

This research follows a methodology informed through a detailed FMEA for the novel shipboard power system architecture. FMEA is conducted initially at the system or sub-system level, gradually moving down to component levels. FMEA is one of two established reliability analysis techniques used in this research, the other being sneak circuit analysis (SCA).

The initial functional FMEA helped narrow down critical devices of the network, which identified the dc-dc buck converters as vital devices to realise benefits of the proposed zonal distribution architecture. Hardware FMEA done on the buck converter was used to increase understanding about its component level faults and their effects, further narrowing down pertinent issues. This overall information is then used for simulating fault scenarios to generate data for further research and analysis into diagnostics. This approach of using FMEA to guide and inform further research into diagnostics attempts to lay the groundwork for further research in the field of SPS risk management.

The other aspect of novelty lies in the modification of SCA to output usable data that were effectively employed to differentiate between different fault scenarios. The modification differs from the convention of using component symbols to form the SCA generalised connection matrix (GCM) as actual current and voltage values are

used to form the GCM instead. The determinant of the GCM outputs numeric values that are shown to differentiate between various operating scenarios of the buck converter circuit. The data produced with this modification is from a SIMULINK circuit and a corresponding hardware test setup. Standard sensor output is used to calculate circuit currents and voltages applying circuit laws and component models [12] by using local measurements (input/output currents and voltages) and values of component parameters. The advantage lies in the fact that additional sensors are not needed to obtain measurements of quantities required to be used for the modified SCA process.

Employing the projective adaptive resonance theory (PART) algorithm [13], heuristics were generated utilising the software tool Weka [14]. Thereafter, these rules were encoded using conditional statements (if-else) and tested on the data offline to check the diagnostic efficiency. The results were promising in showing an ability to distinguish different component level faults which have been elaborated in later sections. Thus, FMEA helped narrow down critical sections to focus research, thereafter SCA was used to produce data that help differentiate component level faults in a buck converter when run through an AI based algorithm such as PART. This systematic research approach within this field of study is illustrated in fig.1.1.

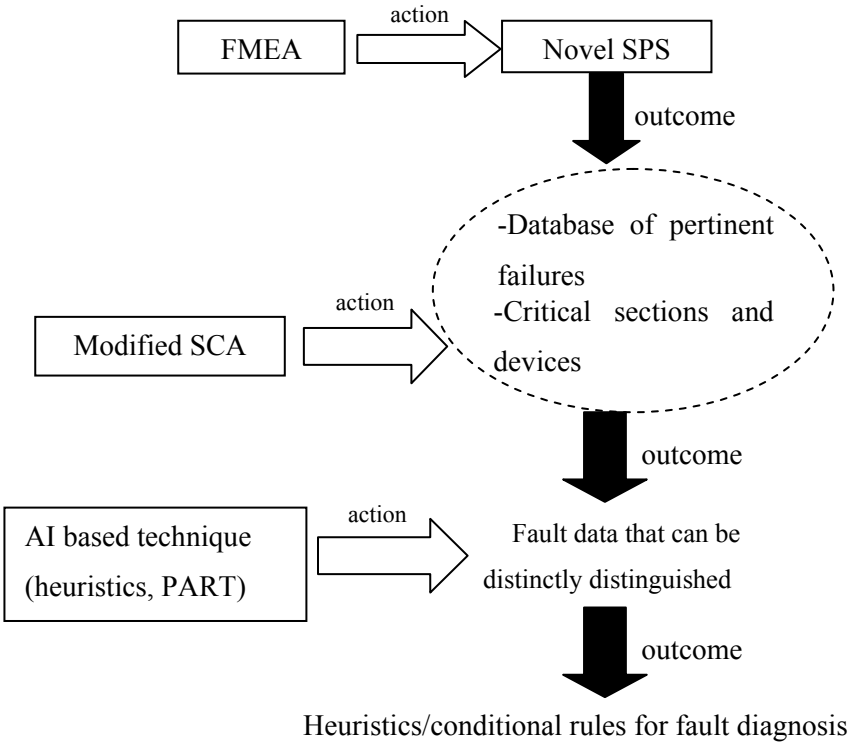


Figure 1.1: Approach proposed in this thesis for developing a potentially robust methodology to help diagnose faults

1.4 Thesis structure

There are 7 chapters in this thesis. This chapter offered a concise introduction to the specific research arena along with the thesis outline. Chapter 2 provides a detailed coverage of efforts of researchers in this field that adhere to root concepts such as:

- Fundamental analysis, modelling and stability issues with risk assessment.
- Automation, reconfiguration of network, power restoration and load shedding.
- Fault diagnosis and prognosis

Chapter 3 gives relevant information on research conducted in the field that actively supports the novel SPS research, namely power electronics. In this chapter the emphasis is laid on power electronics fault diagnosis at a device as well as component level. Further, the concept of fault accommodation as outlined in the power electronics domain is described by referencing relevant publications.

Chapter 4 highlights research in reliability analysis, which forms the basis for studying envisioned SPS from a risk management point of view. The two major reliability analyses methods outlined here are failure mode and effects analysis (FMEA) and sneak circuit analysis (SCA).

Chapter 5 demonstrates utilisation of FMEA on the proposed zonal SPS studied in this research. A meticulous methodology is followed which helps understand possible failures and faults. This aids to further focus research into diagnosing pertinent failures and issues. This methodology is a systematic approach applied in this particular research arena.

Chapter 6 explains the modification of conventional SCA to aid in producing diagnostic indicators that helps differentiate types of faults at a component level within a dc-dc buck converter. This forms a novel aspect of this research added to the methodology stemming from FMEA. This chapter also discusses results of the proposed approach applied to both a computerised model (MATLAB-SIMULINK) as well as a representative hardware system. The results are compared after applying Weka (open source data mining software) to generate diagnostic rules with the help of modified SCA elaborated in the previous chapter.

Chapter 7 concludes the Ph.D. research and the thesis by summarising the justifications and novelties of this work. Discussions are presented on the possible future paths that could be derived and undertaken from this research work.

1.5 Associated publications

The following publications have arisen as a result of studies conducted and elaborated in this thesis.

Conference papers:

1. Soman, R.R.; Davidson, E.M.; McArthur, S.D.J.; , "Using functional failure mode and effects analysis to design the monitoring and diagnostics architecture for the zonal MVDC shipboard power system," *Electric Ship Technologies Symposium, 2009. ESTS 2009. IEEE*, vol., no., pp.123-128, 20-22 April 2009

2. Mair, A.J., Soman, R.R., Davidson, E.M., Srivastava, S.K., Schoder, K., McArthur, S.D.J. and Cartes D.A.; "Intelligent distributed control for shipboard

power systems based on fault diagnosis and condition monitoring," *Engine as a weapon III, Portsmouth*, UK, 23-24 June, 2009.

3. Mair, A.J., Soman, R.R., Davidson, E.M., Srivastava, S.K., Schoder, K., McArthur, S.D.J., Cartes D.A. and Edrington, C.S.; "Fault Classification and Accommodation in Shipboard Power Systems," *Proceedings of the International Simulation Conference*, Turkey, 13-16 July, 2009.

4. Mair, A.J., Soman, R.R., Baker, P.C., Davidson, E.M., Srivastava, S.K., Schoder, K., McArthur, S.D.J., Cartes D.A. and Andrus, M.; "Progress in the development of adaptive control for shipboard power systems through modelling and simulations," *Proceedings of the Grand Challenges in Modelling and Simulation Conference*, 2010.

Journal paper:

1. Soman, R.R.; Davidson, E.M.; McArthur, S.D.J., Fletcher, J.E. and Ericsen, T.; "Model-based methodology using modified sneak circuit analysis for power electronic converter fault diagnosis", *Power Electronics, IET*, vol.5, no.6, pp.813-826, July 2012.

A detailed description of each publication and their relevance is presented in section 3.4.

Chapter 2 Literature Review

2.1 Introduction

The overall aim of this research is the development of a fault accommodating control system (FACS). The difference between this FACS and a classical fault tolerant control system is that the FACS will try to explicitly identify faults and incorporate this additional information to achieve system-wide robustness. Therefore, after a fault is diagnosed and located, it is believed that appropriate control actions can automatically be taken to mitigate the effects of that fault. It is envisaged that this will be achieved through the changing of controller parameters or by system reconfiguration such that the consequences of the fault can be avoided or minimised. It is also expected that the time by which remedial action can be taken in response to a fault will be greatly reduced.

Thus such a proposed system must have accurate fault diagnosis followed by an additional system that can reconfigure the network once the diagnosis is made. Another aspect of the research is to provide adequate decision support to the onboard crew by potentially using information gathered from the diagnosis and monitoring system. Apart from an accurate diagnostic capability, an open area of research is in prognostics. While a diagnostic system would concentrate on the timely detection and identification of the fault, a prognostic system would aim to predict the time remaining for failure by detecting potential precursors. This added capability of predicting behaviour to estimate the most likely outcome is highly advantageous in this research arena of the notional zonal SPS with a FACS.

To achieve the mentioned aim of building a FACS, detailed studies in a number of sub-domains have to be conducted. As expected, research is ongoing within these domains and has been elaborated upon in this and the next two chapters.

2.2 Envisioned SPS analyses, modelling, stability and risk assessment

An informative and detailed discussion about the challenges at design stages of the envisioned DC architecture for warships is presented in [15] by Amy explaining the analytical aspects of developing the US Navy's integrated power system (IPS).

Here, a clear distinction between terrestrial power systems and shipboard power systems (SPS) is made highlighting the practical issues to be considered while analyzing each type. This paper is important to understand the fundamentals of shipboard power systems and to gain insight into the top-level requirement of the research field.

Hegner and Desai in [16] further elaborate on IPS development and introduce a new term namely integrated fight through power (IFTP). The IFTP idea explains the envisioned zonal SPS distribution concept wherein power electronic converters play a major role. The paper explains differences between the traditional radial power distribution system with the proposed method which uses starboard and port busses that supply power to zones. The diagrammatic comparison shown by the authors between proposed AC and DC zonal electrical distribution systems (ACZEDS and DCZEDS respectively) is shown in fig.2.1. A performance evaluation between ACZEDS and DCZEDS is made along with highlighting other practical aspects such as corresponding weights of the two setups. Furthermore, the advantage of choosing DCZEDS is clarified reporting on factors like isolation of the faulted zone during system level disturbances (e.g. grounding issues) to prevent fault propagation. These factors make the use of power electronic converters as power delivery devices vital for the envisioned SPS. A detailed description of the envisioned zonal SPS is provided in chapter 4.

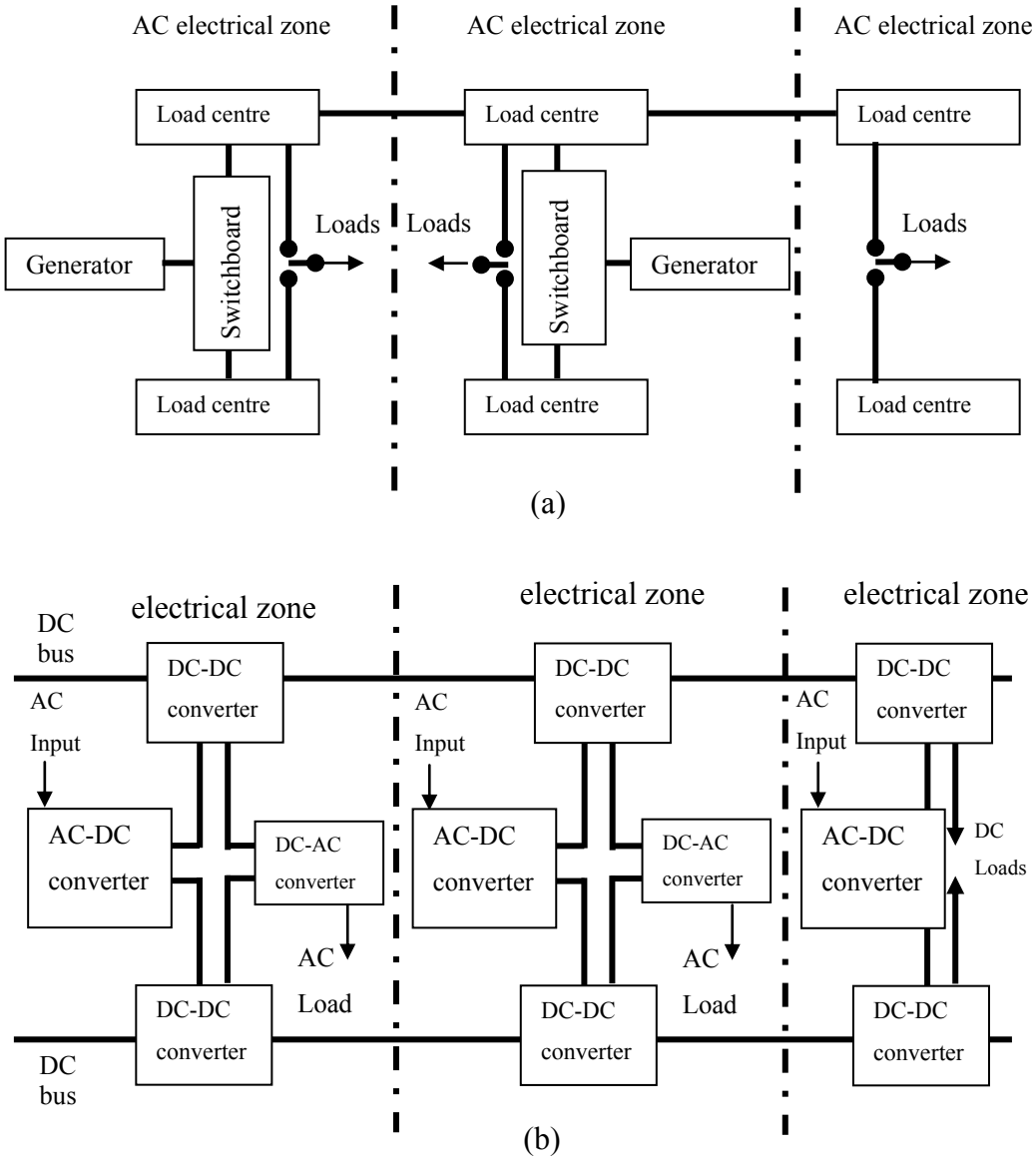


Figure 2.1: (a) ACZEDS representation [16] , (b) DCZEDS representation [16]

An important concept emphasizing the use of advanced power electronics for the notional warship was proposed by Ericsen et al. in [9] abbreviated as power electronic building blocks (PEBB). Owing to the extensive use of power electronic converters to facilitate various power needs of loads, the ship's mission goals are aimed to be achieved using the minimum number of PEBB 'boxes' instead of using a separate set of equipment for each separate mission type. The PEBB devices can be used during the design phase to produce different products by varying hardware configurations. This research in [9] outlines a detailed study of the PEBB concept shedding light on the modular and hierarchical design principles of each such device.

The emphasis is on producing advanced devices with interactive elements that fit in with the objectives of the envisioned SPS, vital among which are reduced manning and increased automation. A physics-based design model development approach is adopted where new designs will be built incrementally over time incorporating hardware-in-the-loop testing. This paper marks the crucial need for research into advanced power electronics devices (especially converters) with preferably built-in fault diagnostics at not only the system level but also at the sub-system and component level. The concept of PEBB devices and its modularity allow for building open and novel shipboard power distribution architectures that could include intelligent methods for protection, reconfiguration, restoration, fault diagnostics, condition monitoring and perhaps prognostics.

Ciezki and Ashton in [17] describe the move of the US navy from the traditional radial AC system to the notional DCZEDS. They also detail the various pros and cons in support of the DCZEDS. This argument forms a good base to understand the interest to adopt the DC zonal power architecture from an ideal viewpoint. However, the authors aim to touch upon the stability issues concerned with such a zonal system which is a crucial aspect owing to the lack of thorough understanding of the novel system's behaviour. One aspect outlined is the differences between the slow dynamics of the power source and the much faster dynamics of power electronic devices. This is a crucial point that needs emphasis while dealing with fault isolation as well as diagnostics. The authors admit that this research is still in its infancy and more work is needed to understand how to deal with these constraints imposed, when a large number of power electronics are utilized in an already lesser known DC architecture. Not much detail is provided on various stability issues, most probably due to the lack of benchmark systems and understanding of the notional power architecture.

Momoh et al. in [18] propose probabilistic security indices for the notional power system. The research is conducted to develop a more accurate load flow study method to take into account contingency situations. The method adopted for the power load flow analysis is called expected contingency margin which is able to handle the contingency probabilities and the priorities of the path causing the fault. Ten different contingency situations are studied namely, 5 cable losses, 3 generator outages and 2 converter failures. The IPS is modelled using MATLAB wherein a

portion of an entire network is simulated that includes the cables, generators and two converters. This paper reports a useful metric which provides a method to compute probabilities of occurrence of certain faults. However, there is no detailed explanation as to why only certain type of contingencies have been considered, further, there is no detail about the kind of converter faults (2 failures), a device which forms the crux of the zonal power distribution system. Perhaps this approach needs to be applied in much more detail to all possible faults that can happen in a given shipboard system employing ACZEDS or DCZEDS, thereafter an informed decision could be made as to which are the pertinent faults based on their probabilities computed. An initial rigorous methodology is needed to assess various possible faults that may occur in the novel SPS at all levels of the distribution architecture in order to thoroughly understand associated risks.

A different risk management aspect to [17] and [18] is presented in [19] by Schulz et al. from the monitoring and measurements point of view. Apart from faults occurring in the power equipment, loads, cables etc. and developing methods to diagnose and accommodate those faults, it is important to ensure that sensors and measurement devices are monitored too. This includes studies into sensor positioning and redundancy. In [19] a genetic algorithm approach is used to determine the minimum number of measurement meters required to estimate the state of the system. A contingency analysis is also done where meters are removed one by one and a check is done to ensure sufficient data to achieve the mission goal is being obtained. This research is aimed at providing means to enable efficient response to reconfiguration during a fault scenario where physical damage may occur to parts of the vessel resulting in loss of equipment. The approach simulated in MATLAB is useful to verify whether adequate data is available given the current topology of the power architecture during different operational scenarios. This paper however does not deal exclusively with restoration and reconfiguration aspects of the system, but the research presented may have potential uses for these activities.

MATLAB is again used to model AC and DC power systems by Schulz et al. in [20]. Here a more detailed attempt is made including models for protection system as well as hardware-in-the-loop (HIL) testing. This is a good example of combining the best of simulation as well as real hardware tests wherein an enhanced understanding of the interaction between real and virtual systems in a non-destructive and cost

effective way could be obtained. This paper reports overall research being conducted in the sub-domains that comprise the notional SPS namely:

1. Protection system
2. Reconfiguration system
3. Stability analysis
4. Power electronics

The emphasis on power electronic converters and interfaces is made for developing the IPS as per the proposed guidelines. A reference to the PEBB technology is made showing its use within research concentrating on protection, reconfiguration and stability issues.

The zonal power distribution architecture still being in the conceptual phase means that there is a lack of actual existing systems for reference. This means, meticulous research is needed to simulate the behaviour of such a system in various operational scenarios using purely virtual means or HIL inclusive techniques. In [21], Feliachi et al. aim to build a hardware prototype to conduct experimentation related to the US Navy AC/DC distribution, to help validate work done on automatic reconfiguration and to aid in studying embedded controls for these applications. Such an initiative is an important step towards getting more real-world data as opposed to only software simulation data. This paper describes the various tests that could be conducted on a hardware test-bed including control system experimentation. A higher level system employing intelligent software agents is also proposed that could potentially form a useful human-machine interface. Several researchers including Feliachi discuss variants of multi agent system (MAS) applications going hand in hand with the increased power electronics onboard the notional SPS. More on the application of MAS for managing tasks aboard the SPS [22-24] are discussed in section 1.3. The positives that arise by using software agents which by definition have *reactivity, proactivity* and *social ability* seem to fit in with the anticipated advanced capabilities the future's naval SPS is supposed to possess. Much work needs to be done though to make the agents intelligent enough to form an effective human-machine interface especially in the case of handling automated power reconfiguration, restoration and fault diagnosis.

2.2.1 Discussion

The US ONR proposed IPS is still in its conceptual phase. Being a relatively unknown system without previous benchmarks, the start to the research thus must begin at a fundamental level beginning with assessing the differences between the envisioned system with its traditional and conventional counterparts. Researchers have conducted comparison studies between terrestrial power systems plus traditional SPS with the envisioned IPS to highlight analytical and practical differences that could impact applications such as condition monitoring and fault diagnostics. To advance research, it is absolutely vital to gain a strong understanding of the operational dynamics of the envisioned distribution system, after which studies into monitoring, diagnostics, decision support and prognostics could be successfully launched. The works of researchers highlighted in this section mainly deal with analysing the novel SPS idea from a scientific and mathematical viewpoint. Once the underlying theoretical understanding is gained, the next step is to develop computer aided tools for simulation studies and corresponding hardware test rigs to validate proposed analysis approaches and improve understanding.

The research described in this section is the important preliminary work in this field. After dealing with aspects of understanding fundamental theories, associated risks and their mitigation and stability issues, section 1.3 deals with the logical next step of system level power reconfiguration, restoration and load shedding schemes.

2.3 SPS automated reconfiguration, restoration and load shedding

This section outlines major research towards functional tasks such as power reconfiguration, restoration and load-shedding. The system reconfiguration problem is formulated as a variation of a fixed charge network flow problem by Butler-Purry et al. in [25] using load and path priorities along with various system constraints mentioned in the paper. In the paper, an illustration of the method is shown using a three-dimensional layout of the shipboard system generated with computer aided design and drafting aids. This layout integrates information from a relational database which contains the electrical parameters of the SPS. This integrated virtual system forms what is referred to by the authors as the geographical information system (GIS). By using well established and known design parameters, such a GIS

forms a feasible method to get close to mimicking an actual SPS. An automated self healing reconfiguration strategy for power system restoration aboard naval vessels is presented in [26] by the same researchers. The paper aims to address the goal of providing continuous mobility, power and thermal management for shipboard combat systems in the presence of major interruptions. Here, the authors discuss power system restoration in the event of a missile strike. On current shipboard systems when critical loads fail to obtain power due to faults, the restoration is done manually. In this paper automated restoration is proposed such that when subjected to a contingency, the system is able to assess its impact in order to contain it to restore the power system to the best possible state in that situation. What remains an open issue is the system behaviour in the presence of faults because there is no past knowledge existing in this case. The research in [25] and [26] however is based on the radial power distribution system and not the notional ACZEDS or DCZEDS. But nonetheless, the approach holds merit owing to the iterative nature of good quality research, thereby enabling enhancements to simulations. With appropriate advancements to the GIS from the information database modifications, a healthy understanding of system behaviour under various situations can potentially be studied.

An alternative method to reconfigure power to vital loads in the presence of a fault is presented in [27] utilising an expert systems approach. Here a rule based expert system does fault detection by comparing threshold values of voltages and currents measured. The research simulates a test case representing a missile strike by de-energising loads and demonstrates the method's capability of restoring power to them using load shedding operations. The paper however does not elaborate on fault diagnosis of more common faults such as ground faults or device level faults in equipment.

These papers show a technique that automatically suggests alternate paths to restore power to vital loads as per priority. The nature of contingency discussed is in the rare event of a missile hit. The power system architecture discussed is the radial system and not the envisioned DC zonal distribution system with increased use of power electronics. Further, the method is for a system-wide contingency and does not address fault diagnosis for sub-system or device level issues which are important owing to the fact that the DCZEDS is expected to isolate faults and prevent their

propagation, making zonal (sub-system) and device/component level diagnostic research a must.

An automated agent based reconfiguration method is proposed in [28]. The paper reports research done on the envisioned DCZEDS. Here five major faults are discussed, namely:

1. Primary DC bus zone fault
2. Secondary DC bus zone fault
3. Buck converter source side DC rail fault
4. Intra zonal fault
5. Generator fault

The agent based reconfiguration method is demonstrated for the most commonly occurring problems, namely the primary and secondary DC bus faults. The proposed method is run on a DC zonal system simulated on PSCAD. The paper effectively deals with power routing in the event of a fault using agents but does not report on diagnostics, decision support or prognostics. Neither is anything discussed about using the proposed methods on an actual hardware test setup (scaled down version for example) that produces more realistic signals than simulations.

A proposal for a decentralized multi-agent system (MAS) for reconfiguring the shipboard power architecture is reported in [29]. The agents are developed in MATLAB while the system is simulated on the virtual test bed (VTB). MATLAB-SIMULINK is extensively used to simulate power systems in part or whole using the various toolboxes available within the software. The use of MATLAB to build agents as presented in this paper makes this software in general promising to be utilized for analyzing and experimenting within this research field. This paper though attributes the adoption of decentralized MAS to counter battle damage scenarios where physical damage may render a centralized control system ineffective. This reasoning seems impractical owing to the fact that it is practically impossible to determine where a missile would strike. Also, there is no emphasis given to how the reconfiguration would take place which normally takes into account load priorities.

Feliachi et al. propose a distributed scheme with MAS based control agents in [22]. This is to aid the notion of automated reconfiguration and self-healing in the event of battle damage and other fault scenarios. With a system utilising agents, the crucial aspect is the information fed into individual software agents and its accuracy.

Here, the authors aim to implement a graph theoretic self-stabilising maximum flow algorithm as the agents' strategy to ensure efficient power management which would include considering constraints and load priorities. A layered agent architecture is proposed to form a logical hierarchy classified by functionalities. The topmost layer in this architecture forms the human-machine interface wherein aspects like interactivity and decision support may be explored and included.

An MAS with two layers (shown in fig.2.2) for power system reconfiguration is proposed by Cartes et al. in [23]. One layer is the power system layer with a network of devices and the other layer is the one with software agents. Every device has its agent with whom information can be exchanged. The communication constraints on every agent are placed such that information exchange is possible only with a neighbouring agent. This paper is one of the first to introduce a layered MAS where the electrical devices in the hardware layer are mapped onto its respective agent in the MAS software layer. Simulations are carried out by the authors using a real time digital simulator (RTDS). The RTDS offers high fidelity simulation and is a high speed, real time testing framework on which control system simulations and general power network simulations can be carried out. The authors make use of iPAQs to implement the agents. A field programmable gate array (FPGA) is used as an interface between the device layer (on the RTDS) and the agent layer (MAS). Further, to test this proposed MAS, various operational scenarios are simulated on the RTDS to carry out automatic reconfiguration applying the proposed scheme. These detailed efforts are important in the overall research for the development of automated reconfiguration techniques. Cartes et al. systematically propose a structured methodology making use of state-of-the-art technology to provide a potentially promising intelligent system that may be adopted for the SPS not only for reconfiguration (as suggested in [23]) but for other tasks such as condition monitoring, fault diagnosis and perhaps prognosis as well. Using MAS could also aid in providing a decision support interface to the onboard crew. However, the type of information exchanged between agents is mentioned, but the methodology and data used to build an agent is not clearly explained. More detail regarding power system information needs to be incorporated into the agents such as topology information, power capacity information etc. as reconfiguration depends on the consideration of

data like available power and load priorities. It may be interesting from the research point of view to extend this approach to conduct fault studies.

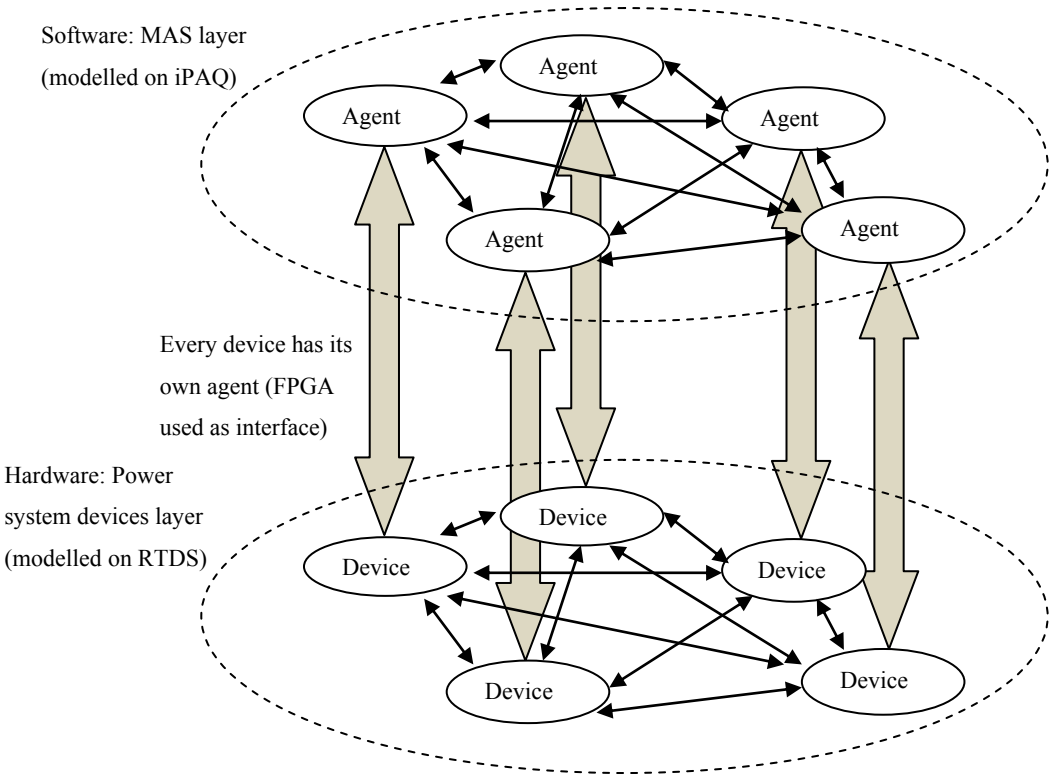


Figure 2.2: Two layered MAS for SPS with devices having their own software agents [23]

Due to a lack of real existing systems with the proposed zonal distribution, almost all of the reconfiguration and restoration studies conducted thus far have been on simulated systems that adhere to the set guidelines given by the US office of naval research (ONR). A positive from the research described in this section is the viability of software products such as MATLAB-SIMULINK to be used in this field of study for better understanding of operating scenarios in a safe non-destructive environment.

A SPS power system restoration scheme using an MAS is proposed by Momoh in [24]. The rationale given by the author to use an MAS is its decentralised network and local data processing capability which greatly reduce the computation time and network bandwidth. Another advantage is the ease of scalability in case newer loads/devices are added to the network and the subsequent ease of extensibility to carry out required tasks. The ONR control challenge reference system is used to test

the proposed MAS for power restoration. The MAS differs from [23] because here Momoh proposes a single negotiating agent, several load agents and several bus agents divided into two layers, the communication sub-system and operational sub-system. The three different agents communicate among one another and solve tasks using local information without a control centre. Simulated tests on the reference system are shown to be able to successfully restore power during a complete outage as well as partial outage. Though this methodology is elegant, it is tested on a highly simplified simulated system. The MAS's feasibility for a more complex network remains to be seen.

A detailed survey of reconfiguration methods is given by Nagaraj et al. in [30]. This work also highlights the important issue described by Amy in [15], i.e. of finite inertia in the case of SPS. The authors in this research adopt a theoretical stability based graphical approach as opposed to more hybridised approaches used by other researchers mentioned earlier. This work though in its initial stages offers a potentially important contribution by making high level comparisons between terrestrial system reconfiguration and that proposed by previously mentioned authors for SPS applications.

An expert system based load shedding scheme is presented by Cartes et al. in [31]. The dynamic prioritization of loads is obtained by combining both the significance level and critical natures of loads using analytical hierarchy. The authors present a detailed explanation of the various factors affecting the process of load prioritisation. The load priority list is based on the mission goal and nature of loads and is an advantage over traditionally used schemes which are less flexible. Once the loads that are to be shed have been determined, system knowledge and expert reasoning are required to find an optimal solution for switching actions to shed the loads. Thus, an expert system that emulates the search behaviour of human experts in solving a problem is a preferred choice for this scheme. Simulations are carried out on the validated SPS model on the RTDS and show promising results. To apply an expert system approach, the expert knowledge elicitation process needs to be detailed, rigorous and accurate. This research is demonstrated for one zone of the DCZEDS and needs to be applied to different types of zones with different load profiles to test feasibility. Also, a detailed expert knowledge elicitation methodology needs to be put

in place if the approach is to be applied for a variety of zones and eventually the system as a whole.

2.3.1 Discussion

Power management which is inclusive of reconfiguring the system, restoring power and load shedding are the logical system related applications underpinned by the fundamental understanding of SPS architectures and behaviours. Publications associated with power managing aboard the notional SPS are described in this section. Numerous researchers propose using MAS architectures to fulfil the envisioned goals of the IPS. The structuring of the MAS varies and a layered architecture where every device has its individual mapped software agent to interface with the onboard crew is one of the most promising proposals. System modelling on platforms such as RTDS has made it possible to study high fidelity simulations of the notional SPS in a non-destructive and safe environment to test real time controls. It also paves the way for experimenting with new ideas which would otherwise be difficult to study using actual hardware setups. Formulating techniques to handle power delivery and ensure continuity of power to vital loads in the network is followed by going into further detail dealing with system and device level faults. An important positive from the research presented in this section is the viability of using software such as MATLAB-SIMULINK, PSCAD etc. for conducting SPS related experiments. Research related to fault studies specific to the notional SPS is described in the next section.

2.4 SPS related automated fault detection, diagnosis and prognosis

Moving on, the next crucial study area on a system-wide basis is fault studies and particularly identification, location and diagnosis. Researchers such as Amy, Momoh, and Schulz have highlighted fundamental differences between terrestrial and shipboard power systems. Keeping these in mind, the need for understanding fault manifestations within the novel architecture becomes vital. Known methods to diagnose system wide faults, accommodate them and mitigate associated risks could be borrowed from terrestrial power system applications or from traditional shipboard systems. However, a careful analysis of faults and the system's associated behaviour is necessary owing to the fundamental differences between the envisioned

architecture and the traditional shipboard power system as well as terrestrial networks. It is possible that well known fault diagnostic methods could need modifications to be applied to the studied system or completely new diagnostic methods may be needed to deliver efficient performance.

In [10], Logan outlines the various crucial needs to fulfil the proposed functions of the envisioned IPS architecture. Extensive use of PEBB technology is proposed to facilitate a plug-and-play hardware concept thereby reducing the cost and time for research related experimentation as well as benefitting application aboard the notional warship. An important figure mentioned by Logan is the reduction in manning by up to 90% compared to current vessels. As a result, the importance of decision support and automation in activities such as diagnostics, reconfiguration and restoration becomes very clear. In this paper, the extensive use of power electronic devices (e.g. converters) for the proposed SPS is highlighted. The use of artificial intelligence (AI) based algorithms for reconfiguration, survivability and fault diagnostics is emphasized which points towards importance of having detailed understanding of the network dynamics, fault cases and methods to mitigate or eliminate the associated risks. In the light of having a far reduced number of human personnel onboard, the paper reports on the major areas for the all electric ship where automated intelligent diagnostics related knowledge will be needed such as,

1. Sensors
2. Thermal management system
3. Power sources
4. Power transmission network
5. Control system
6. Power electronic devices
7. High power and vital loads (e.g. electric rail gun)

The high percentage of reduced manning proposed makes enhanced automation a necessity especially in activities such as system reconfiguration, power restoration and fault diagnostics in the event of a risk. The novelty of the proposed distribution architecture makes studies into network topologies and its modification during various operational scenarios followed by reconfiguration of the system an important research topic. Several researchers have proposed intelligent methods to analyse as well as reconfigure simulated versions of the proposed shipboard power system architecture.

Cartes et al. in [32] provide a more detailed overview of state-of-the-art developments in the IPS research arena emphasising fault diagnostics, prognostics and the informed transition of US navy ships towards condition based maintenance (CBM) systems that are able to intelligently identify when maintenance is needed. The use of intelligent systems such as MAS for various applications on the SPS is highlighted. The idea to match every major device or vital load in the SPS to its respective agent is proposed in this research. A clear list of tasks is highlighted for both diagnostic and prognostic agents. Application of agents is extended to various sub-systems of the SPS shown in fig.2.3. Numerous examples are given to explain functions of various agents constituting the MAS. This paper is important for emphasising the need for intelligent systems utilising schemes such as CBM onboard the warship. Further, the authors provide adequate detail with literature reviews about similar systems from which lessons could be learnt to develop the notional SPS. The encouragement for using agents adheres to one of the envisioned goals of reduced manning aboard the notional warship which can be replaced by the agents. Obviously, this means that a lot of work is needed to make agents intelligent and resourceful enough to take the place of human personnel. For this purpose more detailed and rigorous research is needed into understanding SPS behaviour in the presence of faults.

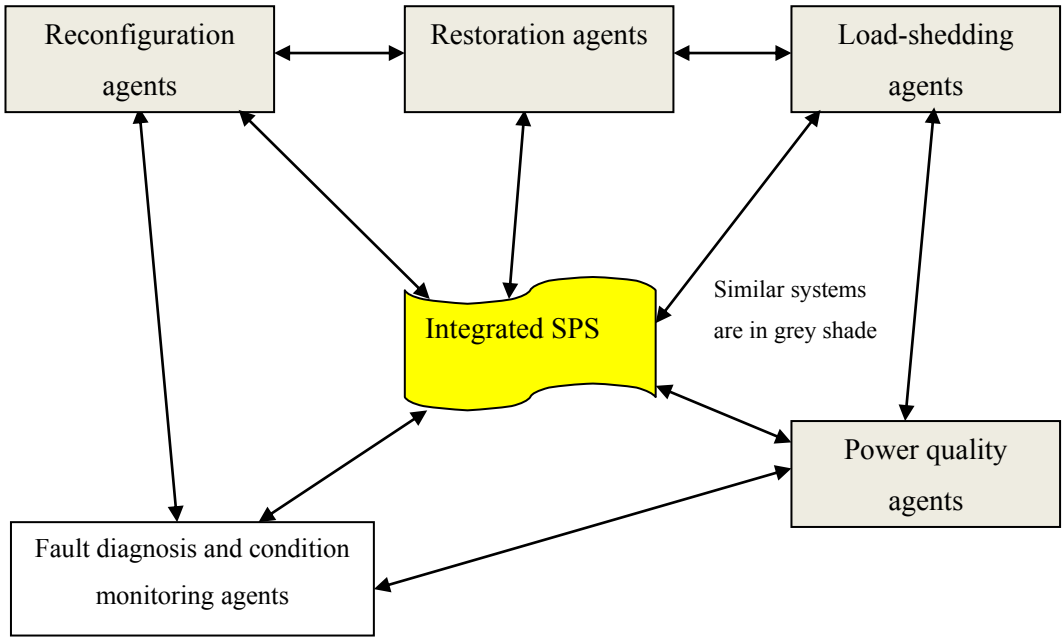


Figure 2.3: Various MAS applications for SPS sub-systems [32]

Baran and Mahajan in [33] discuss the issues of grounding and associated risks occurring in a prototype of the envisioned DC distribution system proposed by the US Navy. Power electronic converters are used for converting power to the desired level as well as to distribute power through DC lines. After the initial AC to DC conversion, loads within a zone are supplied through a DC-DC converter. It is reported here that using a DC bus not only simplifies the cabling for power distribution, but also transfers more power than its AC counterpart. The extensive use of solid state power converters overcomes the challenges of DC distribution associated with reliable power conversion and DC current interruption during fault scenarios. These mentioned aspects make the power converters the most vital equipment aboard the new architecture. As a result, an important system related challenge associated with the use of power converters for DC distribution is the issue of grounding necessary to minimise the neutral voltage shift. Simulation studies carried out using PSCAD/EMTDC (as in [22]) were done under three perturbations namely:

1. At least one generator failure
2. Ground fault
3. DC bus short circuit

To counter the effects of the above system wide faults, the authors propose a high impedance grounding scheme which through simulations is demonstrated to accommodate the effects of the three faults. This paper proposes this idea which is essentially to be applied during the design phase in order to mitigate risks associated with the mentioned faults. This research gives valuable insight on the importance of the use of power converters in the envisioned shipboard system as well as certain issues exclusively occurring in such a power distribution architecture. Further, the paper highlights advantages of using power converters extensively in turn emphasising their importance.

A hierarchical and layered method named platform management system (PMS) to handle contingencies is suggested in [34]. A fault diagnosis model is proposed which could use information such as knowledge and frequency of possible fault scenarios to make a decision. The notional SPS's variants have been discussed in [35] by the same pair of researchers in an attempt to apply supervisory control to each kind using PMS. The PMS aims to work alongside the increased automation aboard future

warships in order to enhance fault diagnosis and reconfiguration. This idea of PMS though is yet to solve integration issues with the constantly evolving designs of the zonal IPS. Also, although the idea to form a detailed approach in obtaining crucial information about operational scenarios holds merit considering the relatively unknown system behaviour, a rigorous methodology to obtain such detail is absent from the research reported. Additionally, the researchers fail to provide any experimental data to support their work through at least simulations using any preferred software utilised by other researchers, e.g. MATLAB.

As proposed in [22] by Feliachi et al. of utilising an agent based control distributed control system, the same researcher(s) propose an MAS framework for fault diagnostics aboard the notional warship. The continuity of research carried out by Feliachi et al. from the prototype system building in [21] and graph theory informed agents in [22] is combined in work reported in [36]. The research in [36] includes fault location as an added application. The fault is located using a model of directional power flows from one node in the network to another node using connectivity information. This fault location information is transmitted to the reconfiguration algorithm having information on switches in the network as well as graph theory. A combination of MATLAB and Java agent development framework (JADE) is used for simulations involving the proposed fault location and system reconfiguration agents. The intelligent agents described in this paper are mapped onto each equipment type i.e. load-agents, switch-agents and so on which in turn have the appropriate data model to be followed. Owing to the nature of the MAS architecture proposed which is at a higher level (system level), the fault studies conducted to validate the model deals with single or multiple line faults. The performance of the system in these types of system wide faults seems satisfactory from the view of time needed which is in the order of ms for fault location. But owing to the very fact that the system is a simulated environment, a HIL simulation may potentially provide more concrete validations. Also, this simulated experiment does not offer much detail on power electronic component behaviour where owing to the multiple use of these devices, a human-MAS-machine mapping may offer positives if sufficient system behaviour details under different scenarios is incorporated.

The idea of using a MAS with individual agents representing the respective equipment (presented by Cartes et al. in [32]) for the human-machine interface is utilised in greater detail by McArthur et al. in [37]. The authors present a three layered MAS with each layer having a set of separate definitions and responsibilities. The three layers of the MAS (depicted in fig.2.4) communicate with the layer immediately above it in hierarchy. These MAS layers and their constituting agents are defined as follows,

1. Control layer – These agents deal with system reconfiguration where the agents interface directly with the power equipment.
2. Reactive layer – Here the agents are responsible for condition monitoring and fault diagnosis. To enable accurate diagnosis, here methods that are able to detect, locate and diagnose faults are included within agents. The methods could potentially be AI based techniques either well established ones or novel ones.
3. Proactive layer – These agents form the interface with the human crew member. Here the agents oversee and monitor the state and health of agents in the other layers. Also, this layer could hold customisable decision support agents for benefit of the crew.

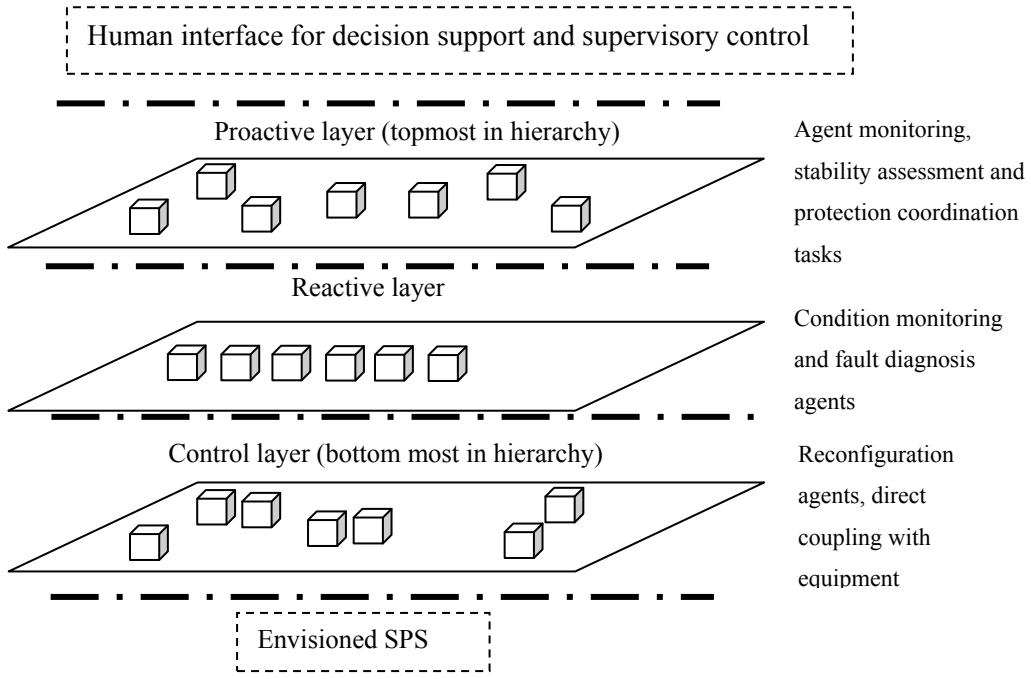


Figure 2.4: Three layered MAS architecture for SPS [37]

In [38] Momoh et al. describe work done in simulating an arcing fault which is a different type of system-wide fault than the grounding issues mentioned earlier. A high impedance fault is an unwanted connection between a bare energised conductor

and a non-conducting body such that the fault current magnitude is restricted below levels that can be reliably measured by conventional means. An arcing fault is a special case of high impedance fault resulting from an air gap due to poor contact with the ground or a grounded object. These air gaps may occur in the ground (soil) or grounded object (concrete, tree, etc.). With a high impedance grounding scheme, seemingly a preferred option for the DCZEDS, this system fault is a justified study area through rigorous simulations and validations. An important aspect of the research reported here is the use of well established theories to simulate the arcing fault. The two well known arc models applied are,

1. Arc model for utility power grid
2. Arc model for circuit breaker interruption

Another systematic aspect is the need for incorporating prior knowledge as the fault detection process would need data on distinguishing normal and abnormal system states. This approach to develop system level fault detection schemes in a system whose behaviour is relatively unknown, from well established theories in related applications (utilities, radial systems etc.) is a promising methodology. Here, Momoh et al. train an artificial neural network using prior knowledge to distinguish between normal and faulty operation. Fast Fourier transforms (FFT) based signatures are used for fault detection. The simulations are carried out on the state-of-the-art DCZEDS IPS network. The method explained though, does not provide information on fault location. But, the overall methodology (depicted in fig.2.5) applied in bringing the research to the point of enabling differentiation among operational states is an advantage for further research that can be extended to other types of faults as well.

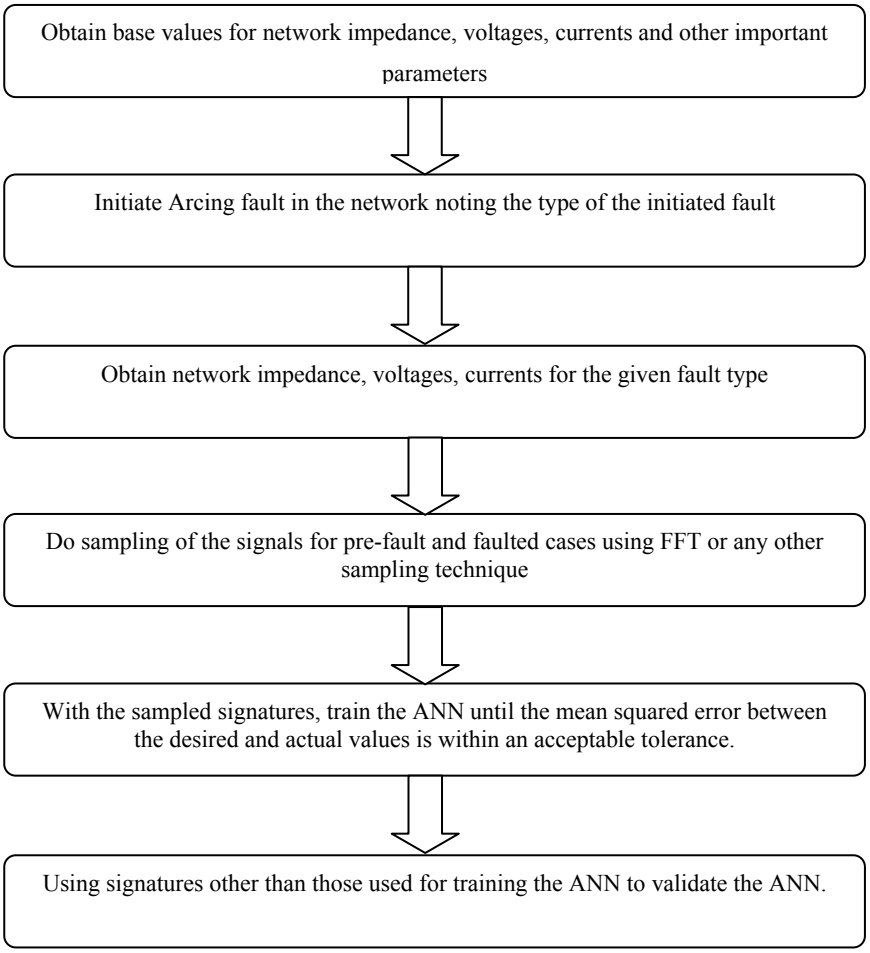


Figure 2.5: Methodology using well established methods applied to SPS along with known AI based techniques [38]

In [39, 40] Steurer et al. focus research on the state-of-the-art ungrounded or high-impedance grounded DCZEDS. The system simulated is the most recent DCZEDS design utilising a large number of power electronic conversion devices connected in the proposed zonal architecture. As in [38], here too a frequency domain based analysis technique is used to differentiate fault and no-fault patterns. Multi-resolution wavelet analysis is used here for analysing the differences in power converter switching noise, which shows changes as per operating scenario. The justification for adopting this method is satisfactorily made by Steurer et al. based on the following characteristics of the DCZEDS,

1. The DCZEDS is implemented as either an ungrounded system or one having high impedance grounding to improve reliability and power quality. This renders single phase to ground fault currents unusable for traditional fault tracing methods.

2. The zonal system has interconnecting cables which act as parasitic elements to form ringing circuits that contain a path through the ground.
3. Excitation of such ringing circuits often occurs in such an IPS owing to switching of power converters, speed changes in propulsion motors and other non-linear loads. Thus there is ample scope to produce noise in the measurements.

A major positive in this research apart from the fault differentiation technique used is the validation with a hardware test setup. The researchers aim to make the simulated system on PSCAD/EMTDC to produce signals as close to the hardware signals as possible. Also, this research aims to address fault studies at a sub-system level (zonal) as opposed to system wide studies (grounding, arcing, reconfiguration etc.) discussed by several other researchers. Further, the power converters themselves are made use of to produce fault signatures, a promising approach for a system that uses a large number of such devices.

The research methodology (depicted in fig.2.6) used by Steurer et al. is promising owing to the utilisation of hardware tests. Also, from the software simulations point of view, the practice of trying to mirror hardware behaviour is an excellent learning activity for further research. One negative aspect though is the lack of details about automated real time diagnosis of faults. The method elaborated is capable of differentiating between no fault and one fault case. The idea of using power converter noise in theory seems promising, but it needs to be tested for various other fault types as well. In addition, more research is needed to apply a wavelets based analysis in a real-time situation keeping in mind the need to produce diagnostics quick enough to match the small timescales in power electronics operation.

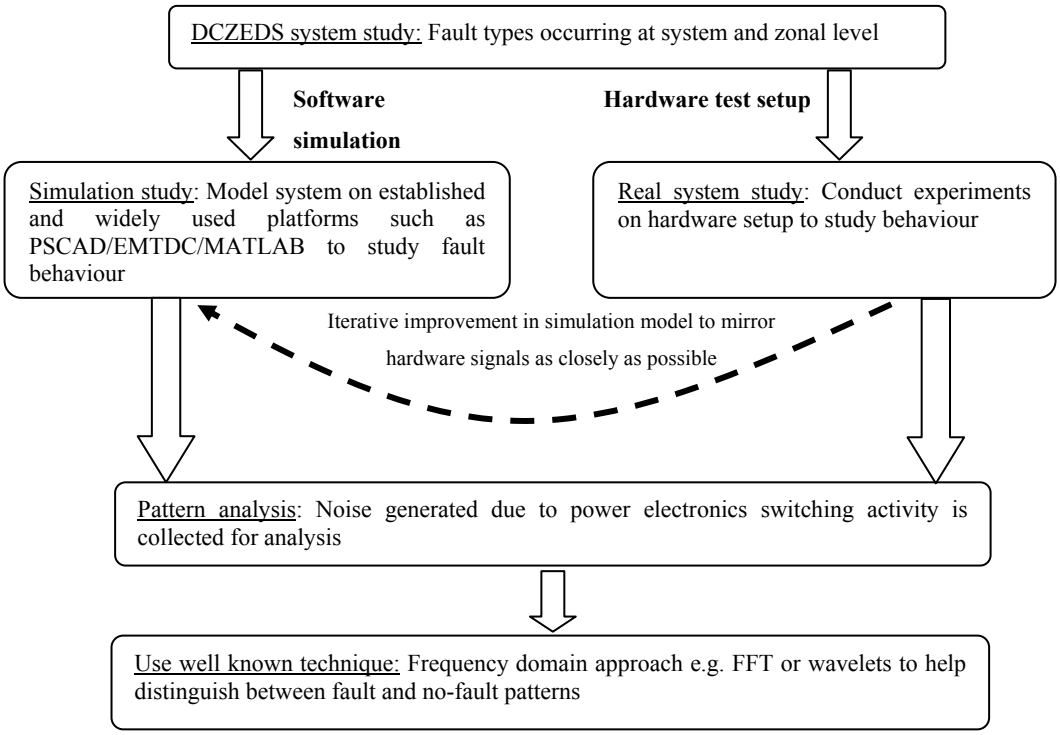


Figure 2.6: Methodology involving both computer models and matching hardware setups

Baran and Mahajan [41] discuss the use of PEBB based devices for the DC zonal protection system requirements. A crucial issue addressed here is the DC circuit breaker to limit fault current. This is an important paper because it reports state-of-the-art research employing PEBB technology and addresses a fault occurring in the power electronic converters which are a crucial device in the zonal architecture. The work deals with a risk associated with a DC bus fault that adversely affects the filter capacitor in the power electronic converters. The authors consider this a design phase issue and propose a snubber DC circuit breaker as a solution. This paper indirectly explains the need to monitor component level faults for the power converters, in this case focussed on the shunt capacitor. A detailed fault study for component level faults is needed to study more such associated risks and which may either be solved at the design phase or by accurate fault diagnosis. An alternative method for DC bus fault current limiting is presented by the same authors in [42]. Here, a voltage source converter is used as a crowbar and the AC side circuit breaker limits the current. This conventional approach is simulated on the DCZEDS modelled on PSCAD/EMTDC. This work represents a feasibility study to combine a conventional approach and a proposed approach (snubber DC circuit breaker [41]) to limit DC bus fault currents.

This methodology adopted by Baran et al. (shown in fig.2.7) is robust in the sense that a comparison between a conventional technique and a new one is made to address the same issue.

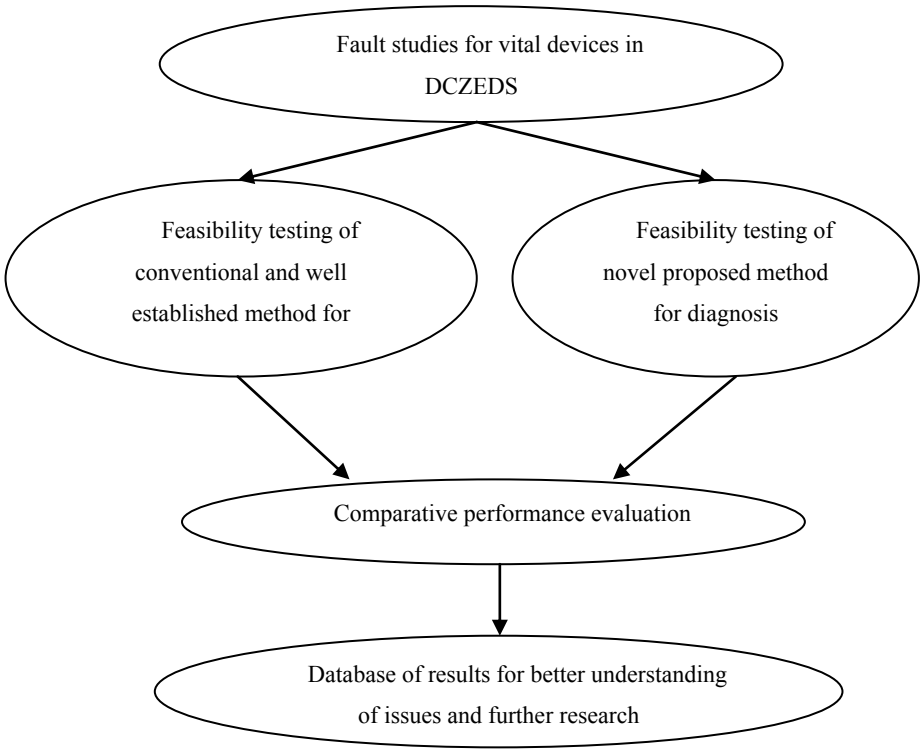


Figure 2.7: Performance evaluation and comparison between conventional and new methods for DCZEDS fault analysis [42]

Very few researchers have discussed fault studies or their diagnosis in SPS power electronic converter in the zonal topology. Owing to this, cascaded converter arrangements will be common where intra-zonal conversions are needed. In [43], fault detection and location for a cascaded arrangement of power converters is discussed. Statistical moments theory is used to detect and identify faults. The system employing a simulated set of results is reported to detect faults in 200μs. This paper is one of the initial attempts at addressing fault detection associated with cascaded converters. The IGBT short circuit fault and its effects are discussed here with associated fault current magnitudes computed. The research presented does not elaborate on the simulation tools used by the researchers. Further, there does not seem to be rigorous validation of the research approach. If the method used indeed is useful to detect faults, performance testing of the method under various loading conditions and operational scenarios is needed.

2.4.1 Discussion

This section describes research into mainly system level faults and their diagnosis. The main fault type discussed by researchers is the ground fault. Solutions to accommodate the ground fault range from design stage proposals as well as employing power converter devices for limiting fault current. Cartes, Logan and McArthur among others advocate the application of MAS to build an overall monitoring and diagnostics architecture owing to various mentioned advantages using agents. Research methodologies are followed which offer promise for advancements in this field for the SPS development. Research reported in this section identifies power electronic converters as vital and crucial for realising the benefits of the notional zonal architecture. Even so, very little research exists towards diagnosing faults and incipient failures in power converters within the SPS environment. Almost no research methodology is present to understand pertinent component level failures and their impacts on a zone and the system as a whole. With the advent of PEBB technology and its imminent widespread application for SPS testing and development, a structured fault diagnosis capability is vital to enable success of the plug-and-play concept. Intelligent methods such as the use of artificial neural networks and expert systems have been employed by researchers as well as pattern recognition approaches such as wavelet analysis. This paves the way for rigorous research into device and component level diagnostics for power electronic converters beginning at using known methods. It also means that possibly new diagnostic methods may need to be developed. The issue of prognosis is seldom discussed and as such remains an open issue in this field. The next section describes in detail well established power converter diagnostics techniques employed in non-SPS applications.

2.5 Chapter summary and conclusion

This chapter described the various research domains related with this Ph.D. The first section dealt with fundamental theories of the envisioned SPS. Here it was adequately shown that the differences between terrestrial power systems and shipboard power systems were well understood.

Once fundamental theories were understood, the succeeding section described the next level of research, to analyse the system as a whole from the view of power

management. In this section, research centred on strategies to automatically reconfigure the power network and restore power was described. Several researchers proposed the use of MAS architectures to facilitate integration of reconfiguration and condition monitoring for the notional SPS.

The third section discussed research focussed on fault diagnosis for the SPS. The major research concentrated on detection and location of ground faults in the power network. Techniques to counter the risks included design phase suggestions. MAS architectures were proposed here to integrate condition monitoring, fault diagnosis and decision support. Other methods proposed to diagnose system level faults were neural networks and wavelet analysis. The major research still remaining in the SPS domain is a thorough understanding of faults at every level of the network. There is little to no work to diagnose component level faults in power electronic converters, whose effects may cause power disruptions to vital loads. Power electronic converters being a vital device to facilitate the DCZEDS, finds little attention towards study of fault scenarios. A research validation approach using representative hardware setups also is relatively untouched in this domain. Further, a detailed methodology to enable understanding of faults and associated risks is absent considering the zonal integrated SPS with increased automation and power electronics is still in its conceptual stage.

Chapter 3 Literature Review: Power electronics

3.1 Introduction

The previous chapter outlined research on fundamental areas important for the novel SPS development. The envisioned zonal SPS is anticipated to rely on increased power electronics systems and devices to enable achievement of the aim of building the FACS. This chapter focuses on the power electronics related research which forms an integral part of SPS studies overall.

3.2 Power electronics development and device/component level diagnostic research

Research conducted by Amy, Hegner, Ericsen et al. marks the use of advanced power electronics as vital to the development of the notional SPS and the realisation of its benefits. Logan, Cartes, McArthur, Butler-Purry et al. suggest the use of artificial intelligence methods and MAS for supporting activities of the SPS such as reconfiguration, monitoring and load shedding as well as fault diagnosis for system-level disturbances (mainly grounding issues).

Research by Baran, Schulz, Momoh, Jayabalan, Steurer and others highlight power electronic converters as very important devices in the zonal topology. Research methodologies in which established diagnostic and monitoring methods used previously either for terrestrial power systems or traditional AC SPS were attempted for the zonal SPS to check their feasibility. This was done for capacitor fault issues and associated fault current limiting. Well known techniques such as expert systems and neural networks from the AI domain have been proposed typically for reconfiguration of the SPS. Even though promising research methodologies have been followed in the various sub-domains of the integrated SPS development, adequate research for the power converter component fault diagnosis and study of associated effects is lacking. This section highlights prevalent diagnostic techniques for power electronic converters used for terrestrial power systems in general.

A comprehensive and detailed review of AI-based techniques for automated fault diagnosis is provided in [44]. The paper reviews research from over two decades in the field of diagnostics and monitoring reasoning their pros and cons. The emphasis

is laid on the most widely used AI techniques thus far which are model based methods, rule based methods and case based approaches with their respective applications. A detailed literature review provides further references to the development of the AI based diagnostics field over the years. Although this paper is over a decade old, it is a useful base to understand the major early contributions in this field.

Fuchs in [45] presents a survey of diagnosis methods prevalent for electric drives fed by three phase power electronic converters. Here a detailed mention of the various types of faults that can occur in the parts of a power electronics based drive system is given. The author discusses the classification of faults into three types:

- Faults resulting in total breakdown
- Faults where emergency operation is possible
- Incipient faults

The aspect of diagnosing incipient faults is important and more detailed study is required in this regard because different internal components of a converter may have any combination of the three classified fault types. This paper forms an important base to introduce researchers to the field of power converter diagnosis as the author discusses a variety of techniques. Also, established theoretical methods in electricity such as Kirchhoff's laws are mentioned in the analysis portion, which shows that a detailed study of the field from fundamental principles has its applications even in advanced needs such as fault diagnosis. Such a fundamental knowledge base could be implemented to create rules for an expert system application for fault diagnosis.

Another important aspect of [45] is the mention for diagnosing incipient faults in filter capacitors on the DC side. Mostly researchers focus on open circuit faults of power switches. Here, an equation (eq.3.1) for computing the effective series resistance (ESR) of the capacitor is discussed which can be used to determine aging of the capacitor. The equation is given below,

$$\frac{1}{ESR(t)} = \frac{1}{ESR(0)} . \left(1 - k.t^{\frac{-4700K}{T-273K}}\right)$$

Equation 3.1

where; T = aging temperature, t = aging time, ESR(0) = ESR at time = 0, k = constant depending on the construction and design of the capacitor.

Such an equation can potentially be used in a predictive model that could detect aging signs for a capacitor. For this, accurate data acquisition is mandatory and an advantage of detecting slowly growing incipient failures is that due to their large time frames, intensive computation effort is not necessary. A statistical or equation employing model based system needs detailed and deep fundamental analysis, but shows potential promise for detecting incipient failures in critical systems.

Rothenhagen and Fuchs in [46] present an overview of semiconductor switch open circuit fault diagnosis techniques. The authors mention three crucial failure modes for initial open circuit failures in IGBT namely:

1. Physical lifting of bond wires due to thermic cycling
2. Driver circuit failure
3. Short circuit fault induced rupture of IGBT

This paper compares the performances of three commonly used methods to detect and locate the failed open transistor in an IGBT based three phase converters. The authors validate results by comparing simulation data with hardware data. This approach of mirroring simulations and hardware in evaluating diagnostic techniques is a robust research methodology which can be adopted with appropriate modifications for SPS research. The three fault detection methods compared are:

1. Slope method
2. Simple direct current method
3. Modified normalised direct current method

This paper indicates that the slope method out of the three shows the poorest performance. Also, the paper reports on closed loop systems thereby implying the real time application of diagnostics inherently within the processor of the drive. The modelling and simulation work in this research uses MATLAB-SIMULINK to generate signals and a bench setup with similar parameters is used to generate hardware data.

This research however, analyses only three fault detection methods and does not discuss detection methods for short circuit faults of switches or faults occurring in other components. Also, the diagnosis methods discussed are traditional ones, thus

perhaps more analysis and evaluation of AI based techniques such as model-based, rule-based, expert systems etc. is needed.

Another important survey paper is [47] which meticulously details the merits and demerits of several fault diagnosis techniques in use for IGBT-inverters. The fault diagnosis related to power converters is chosen by authors owing to the statistic that 38% of faults in power electronic based electric-drive applications is due to switch failure. Most commonly used switch is IGBT and a semiconductor switch in general has three failure modes:

1. Open-circuit fault
2. Short-circuit fault
3. Gate-misfiring fault

From the above fault modes, the gate-misfiring fault is usually of less significance compared to the other two because of advancements in digital controls. The authors present a comparison between various fault detection and protection techniques which may form a useful reference for other researchers to choose suitable techniques as fits their work. The authors mention more than 20 open-circuit fault detection methods and 10 short-circuit fault detection methods for comparison. The conclusion made is that for open-circuit faults, the modified normalised DC current method is most effective while a controlled turn-off during a short-circuit fault is the most effective protection technique.

However, a vital comparison is made among AI based techniques such as fuzzy logic, wavelets and neural network (NN) based methods. The main advantage of these methods is the intelligence they add to the diagnosis process by means of incorporation of failure mode information, interactivity and expert knowledge. Here the only disadvantage highlighted is the computational effort required to apply AI based diagnosis techniques.

In high power applications multi-level converters have emerged as important power delivery devices owing to their fault tolerant operation capability. Aguilera and Rodriguez in [48] propose diagnosing internal component level faults for such a cascaded arrangement made up of numerous single cells of converters. Such converters can be reconfigured to continue operation in case a fault occurs in an internal component in a cell. The authors propose fault detection for a problematic cell using output voltage pattern recognition. Frequency analysis using discrete

Fourier transform of the switching component of the output voltage forms the basis of the fault detection scheme. Comparison with a threshold value indicates the presence of a fault while the phasor analysis indicates the location (fault cell). This research mainly deals with faults in the semiconductor switch of the power converter such as IGBT, GTO etc. This research shows a simple and promising technique to detect a power switch fault; however there is no validation of the result using hardware testing in a real time manner.

Research in [49-51] addresses fault diagnosis issues for the electric motor and power electronics based inverter drives which form the major pair of components in industrial and automotive electric drives. The research reports a model based fault diagnosis system using machine learning for detecting and locating multiple classes of faults in the electric drive. Since from the hardware failure point of view, the power electronics inverter in the electric drive assembly is considered the weakest link, the fault diagnosis is concentrated on the inverter components. Fault diagnostics in an electric drive can be performed by developing an intelligent system that can learn to detect fault signatures under various operating conditions. The main challenges in developing such a robust diagnostic system lies in the fact that it is relatively easier to identify signatures of a fault condition versus the normal condition, whereas signatures of one fault versus another one often differ in a more subtle manner. The authors use the input parameters such as the three voltages and three currents along with the electromagnetic torque (7 parameters) as input to the signal segmentation and feature extraction system. Following this step a neural network (NN) is trained on the features to learn to differentiate signals.

This research mainly deals with the switch-open circuit type of converter fault; though the method proposed is shown to be able to distinguish signatures from open-circuit type of converter faults as well. The research also includes what is called the post-short-circuit fault condition which occurs after complete burn out of a switch. Thus the total number of fault cases dealt with is 6 single switch failures plus 3 post short circuit failures in papers [49, 50]. In [51], the 6 switch short-circuit fault cases are also included, making the total fault diagnosis scheme extendible to 15 fault types.

An important and vital research conducted here is the validation of the diagnostics scheme by verifying with real data generated by means of a hardware setup.

MATLAB-SIMULINK is utilised to model the system and test the diagnostic scheme. A hardware test that is identical is carried out to check the performance of the NN and machine learning based diagnosis on real world data.

This model based fault diagnosis scheme shows a lot of promise to detect component level faults within a power electronic converter (in this case a three phase inverter). Further, the robust research approach is important from the feasibility and performance validation point of view. The researchers claim that the method can be generalised for other faults such as those related to internal diodes, capacitors etc. which though remains to be tested.

Fault diagnosis using NN based classification is presented by Khomfoi and Tolbert in [52] for multi level inverter drives supplying high power motors. This research follows a similar methodology to [49-51]. The research here is centred mainly on assessing the feasibility of using an AI technique (in this case a NN) for diagnostic purposes for a power converter. The same pair of researchers go one step further in their next paper where an integrated fault diagnosis and reconfiguration architecture is proposed in [53]. The condition monitoring and fault diagnosis is carried out using AI techniques owing to advantages outlined by the authors such as:

- No pressing need for mathematical models resulting in time saving
- Utilisation of data from the system itself to form diagnosis (in case of data-driven techniques)

The fault diagnosis system proposed by the authors is composed of different modules integrated together which are:

1. Feature extraction – This is done using principal component analysis (PCA). The principal components are selected using genetic algorithms (GA) whose multivariate optimisation capability can be used to search the best combination of principal components to train the NN.
2. NN classification – This is done using multilayer feed-forward networks.
3. Fault diagnosis – The module responsible to detect and identify faults within the converter cells based on the output of the trained NN.
4. Reconfiguration module – Once a fault cell is identified and an alternative path is provided to enable continuity in operation

The authors use MATLAB-SIMULINK to extract features using PCA and train the NN. The same SIMULINK model is used for simulation and experiments. An experimental laboratory setup is done to further validate the results using hardware

signals. The two fundamental switching fault cases are studied by the authors here, which are:

1. Open circuit fault case – Semiconductor switch e.g. IGBT fails to close.
2. Short circuit fault case – Semiconductor switch fails to open.

The authors here aim to validate simulation results using corresponding hardware signals as done by Steurer et al. in references [39, 40]. This robust and detailed research methodology shows a lot of promise to enable better understanding of fault related behaviour of the circuit studied.

The research presented in [53] is a combination of several individual sub-domains such as dimensionality reduction, data classification and pattern recognition. The researchers apply a novel concept of combining different techniques to produce fault diagnosis for known fault types and reconfiguration capability for a vital device such as a three phase power electronics converter. The fault types considered here are at the component level, in this case for the power semiconductor switch. This research could be extended to other component level faults within this converter topology such as the filter capacitor, which is a vital element from the converter's output power quality and performance point of view. Although this research produces satisfactory results following a meticulous methodology, aspects about its practical application have not been addressed with the view of the computational power required to incorporate modules requiring PCA, NN, GA together.

Zidani et al. [54] investigate the use of fuzzy logic for fault detection in a three phase inverter. This research is different from previously mentioned works utilising NN. The rationale for choosing a fuzzy approach according to the authors lies in the fact that differences between two levels of a certain fault or between two faults are not sharply defined. Thus, using classic true or false logic may be inappropriate, justifying the use of a fuzzy logic instead.

The diagnostic procedure here is based on analytical and heuristic knowledge symptoms where the heuristic knowledge in the form of qualitative process models is represented as conditional if-then-else rules. Fig.3.1 shows the schematic of the proposed method,

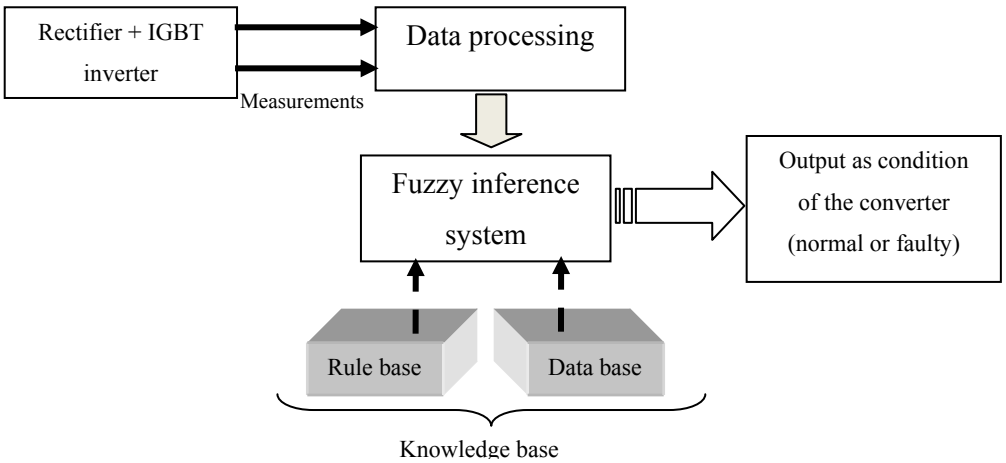


Figure 3.1: Fuzzy based diagnostic approach for power electronic converter using heuristic knowledge base [54]

Similar to numerous other researchers in the power electronics diagnosis domain, Zidani et al. also utilise data from a hardware experimental setup to validate simulation results. This research uses fuzzy logic according with the Concordia stator current pattern analysis to diagnose faults. The scheme is employed for gate misfiring faults and the authors claim that owing to the relative ease of forming the heuristics, an online real-time monitoring and diagnostic system may be feasible. However, the authors do not address other common IGBT faults such as the open and short circuits and including those in the research would enable a generalised evaluation of the proposed technique.

Wang et al. in [55, 56]discuss grounding issues associated with switch short circuit failures within a three level power electronic converter. The neutral point clamped converters discussed here are preferred choices for high power medium voltage applications such as in the envisioned SPS. As is mentioned in references [39-41] in the previous chapter, there is considerable research to detect ground faults aboard the SPS and in [43], the authors discuss faults associated with multi-level cascaded converters. Here in [56], the research is more detailed regarding fault modes manifested in multi-level converters that may cause a fault with the ground.

The underlying system on which this research is based bears resemblances with the proposed SPS with regards to the voltage levels and DC busses. Owing to the novelty of the SPS field, it may be imperative to look at other domains of research to borrow known fault detection and diagnosis techniques (depicted in fig.3.2). As a result, work by Wang et al. forms an unintended but important contribution owing to

the fact that the research they present considers component level fault studies of the power converter used in the study. The focus is on detecting a ground fault by detecting and monitoring the dc-link neutral point voltage along with the overvoltage effects of device short circuit followed by studies into protection approaches. This approach is far more detailed than the prevalent style for SPS diagnosis, where as mentioned previously, the concentration is on system level faults like the line-to-line fault and their protection instead of component level faults occurring in converters that may eventually lead to system level faults. As is the case with numerous previously mentioned works, here too the authors conduct experimental verification of their results using a hardware setup.

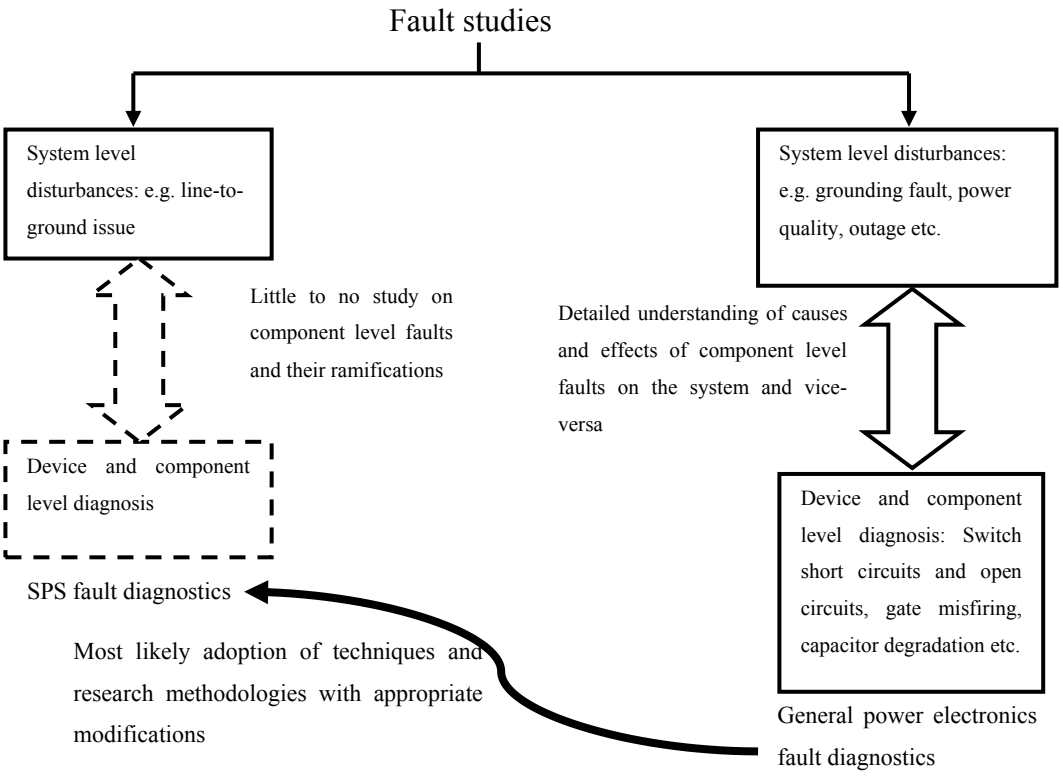


Figure 3.2: Learning from well established power electronics diagnosis research for application to SPS studies

Fault diagnosis of a MOSFET DC-DC converter is presented in [57]. This research offers fault analysis for a step down DC-DC converter or buck converter, as opposed to the largely researched three phase converters. The buck type converter is largely employed as zonal power delivery converters in the integrated SPS design. This research offers a technique to detect MOSFET short circuit and gate misfiring faults. The authors do not discuss open circuit failures because of the tendency of

semiconductor switches short circuiting due to over-current or over-voltage making the open circuit fault a rarity. However, it is observed that even an initial switch short-circuit failure progresses to an open circuit [125] owing to breaking of physical contact at the switch junction due to heat generated by the short circuit fault or by the induced rupture of IGBT [46].

The research presented in [57] applies to a hybrid vehicle system which can be compared to a ship owing to similarities such as high power density and isolated power system (though the voltage levels and loads differ a lot). The proposed signal processing circuit consists of an integrator and a peak detector and the input to this circuit is the dc-link current. A simple technique using the ratio of the peak to integral values is employed to differentiate between the faults considered. The method is tried on a hardware setup of a full bridge zero voltage switching DC-DC converter with the proposed MOSFET fault diagnosis scheme. This research forms an important reference for buck converter diagnosis methods where a component level fault is exclusively discussed although it could be argued that the failure mode of the components considered are practically similar in all converter types. The technique could be used to check its performance against other component level faults such as incipient capacitor degradation, switch open circuit faults (for buck converters using other types of switch e.g. IGBT, IGCT).

The previous paper dealt with the step down DC-DC converter faults, while [58] deals with step-up DC-DC converter also known as boost converter faults. In [58], the fault studies are centred on the output side filter capacitor. Numerous researchers concentrated on switch failures proposing varied techniques, Amaral et al. provide methods to detect capacitor failures which are also highly critical components in the converter. The factor used for the fault detection is the ESR value that can be computed using eq.3.1. An increasing ESR leads to reduced efficiency of the converter and increases the output voltage ripple. ESR also indicates the degree of deterioration of the electrolytic capacitor. The value of ESR could be obtained by two methods used in this research which are:

1. Invasive method – Based on the relation between the average values of output voltage ripple and capacitor current ripple considered during the conduction time of the transistor

2. Non-invasive method – Based on the relation between the values of output voltage ripple for half the transistor conduction time and the average value of output current.

The same author presents an offline technique for evaluating the health of a capacitor in [59]. Since the aging of an electrolytic capacitor can be represented in terms of its ESR and capacitance values, both these quantities are estimated in this proposed approach. Another factor considered here is the dissipation factor (DF) which is specified by the manufacturer along with the capacitance. The DF is the ratio of the ESR and reactance and represents the quality of the capacitor. The capacitance, ESR and DF values change over time due to temperature, frequency, current ripple and aging.

A discrete Fourier transform is employed to process the data acquired through MATLAB. In this research, the proposed approach is to feed the capacitor by a sinusoidal voltage with the required power. From the resultant impedance vector defined by the capacitor voltage and current ESR, DF, and capacitance can be computed. The aging of electrolytic capacitors can be expressed by the increase of their ESR, the reduction of capacitance, and an increase of the DF. Thus, their estimation enables evaluating the condition of the capacitor. The research approach presented here shows a detailed attempt at using fundamental knowledge to arrive at condition evaluation capability. This research touches upon component level diagnostics, in this case the capacitor, for the power converter. The method proposed shows potential in real-time applications and since the authors have verified its accuracy by comparing the results with actual measurements on hardware, it makes the approach all the more promising.

In [60], a technique to compute aging of an electrolytic capacitor is presented such that the failure prediction circuitry can potentially be integrated within the package of the component to improve reliability. Here, the output voltage ripple, expressed in terms of the capacitor ESR is used to detect different degrees of aging. Since this research applies to a switching mode power converter which has a smoothing LC circuit, load variations that in turn affect output ripple are minimal. This ensures that false alarms will be minimal making the use of this strategy feasible for switching mode converters. As is the norm with power electronics research, a hardware setup is used to validate the proposed approach.

The authors present a simple technique to detect aging signs in a capacitor in [60], but the approach seems best suited only to switching mode power converters. This research like [58, 59] discusses capacitor fault detection which is vital, though there may be questions regarding its extendibility for general application to other power electronic converter circuits. Also, there is little explanation on providing information to the user about the fault diagnosis activity.

Imam et al. present yet another method to compute ESR in [61] to help estimate deterioration for electrolytic capacitors. The method employed here utilises Bode plots and frequency domain analysis of measured signals. The authors propose an indirect way of estimating ESR from the RMS values of the capacitor ripple voltage and current ratio. This research although deals with an important component (capacitor) within the DC-DC converter (in this research a boost converter is used for hardware validation), there is little discussion on the computation effort needed to employ this approach on a real-time basis.

3.2.1 Discussion

The research regarding fault studies at the device level for the integrated SPS is as of now in its early stages. This section concentrated on research conducted in the core domain of power electronics in general which has rich resources dedicated to device and component level fault diagnosis. This field is well developed especially in the sub-domain of fault diagnosis in three phase converters which are part of electric drives. Robust research methodologies are followed by researchers in the major works mentioned. A common theme in power electronics research is the ready validation of simulation results by comparing them with corresponding hardware experiments. This approach is feasible in the power electronics domain owing to the fact that well established circuits and systems exist and are easily available, as opposed to the integrated SPS architecture designs which are still in the conceptual phase.

Another important aspect highlighted in this section is the emphasis laid on utilising fundamental theories and principles to aid in diagnostic efforts. Researchers spend considerable effort in building a strong knowledge base about the system at hand, which makes the diagnostic task well informed. This detailed study enables a thorough understanding of effects of faults from a system wide disturbance affecting

a particular device (and in turn an internal component), or a fault in a device (in turn because of an internal component failure) causing system-wide disturbances. This detailed approach of going to the component level to study fault modes is required to be applied to the SPS to enable thorough understanding of fault effects and in turn development of methods to mitigate associated risks.

3.3 Concept of fault accommodation

As mentioned in the introduction, the overall aim of this particular research is the development of a fault accommodating control system (FACS) for the notional DCZEDS. Such a system that integrates condition monitoring, fault diagnosis and reconfiguration is a novel concept in the SPS research domain. It could be viewed as a type of fault tolerance wherein the system is reconfigured to operate at the best possible efficiency even with the presence of one or more fault. This section describes research outside of the SPS domain which caters to accommodating faults in other systems.

In one of the earlier works in the concept of fault accommodation (FA), Polycarpou defines the need of intelligent systems to facilitate high performance through higher reliability, availability and automation of maintenance procedures [62, 63]. The process of system failure characterisation is divided into three distinct steps:

1. Detection – deals with determining the presence of a malfunction
2. Diagnosis – deals with isolating or identifying the malfunction
3. Accommodation – attempts to correct the malfunction through reconfiguration of the system

This paper proposed a learning methodology to construct an automated diagnosis and accommodation system using non-linear modelling techniques. The author conducts research into adding stability analysis in the event of unknown linear disturbances and modelling errors. Here a neural network is used that learns the characteristics of the fault manifestation online and provides corrective actions, thereby successfully accommodating the effects of the fault.

This work forms one of the earliest research efforts to form an automated system that integrates condition monitoring, fault diagnosis and fault accommodation through reconfiguration. These ideas find application in the various MAS based

architectures proposed by SPS domain researchers for combining monitoring and diagnostics.

The notion of automatically accommodating failures within a system is applied through a fault tolerant approach by Zhang and Jiang in [64]. Here, an integration of the fault detection, diagnosis and reconfiguration is done based on an interacting multiple model (MM) approach. The authors propose using a hidden Markov chain model for systems with failures. The various failure modes of the system can be represented and their corresponding transition probabilities. As a result, a set of *N* models can be used to represent *N-1* failure scenarios. This research emphasises the need to study failure modes of a system, to effectively represent them to enable automated fault detection, diagnosis and subsequent accommodation (through reconfiguration).

The use of an MM scheme is employed by researchers in [65] to achieve fault diagnosis and accommodation. The authors concentrate on providing fault accommodation in the case of unknown system faults. Known faults can be diagnosed effectively by incorporating fault signature information either in terms of a model or a rule based system. Since here, a multiple model approach is utilised, the fault modes that are known can be potentially represented as models and their signatures matched with online measurements to form a diagnosis.

In the case of online real-time fault accommodation for unknown failures, a different strategy needs to be used. As a result of this need, the authors propose a method using the discrete-time Lyapunov stability theory. The research results show satisfactory fault accommodation achieved through simulation experiments. The price paid is the lack of understanding of the failure dynamics of unknown and unanticipated faults as well as increased computational complexity. However, this paper is an important read to understand background of the FA research field. Also, the authors list major contributors in the field as well as the prevalent techniques in use to achieve FA (fig. 3.3). An important aspect of successful FA emphasised by researchers is its dependence on accurate fault diagnosis.

3.3.1 Discussion

This section highlighted some important research that aims to explain the concept of FA and its association with fault tolerance and diagnosis. FA is a related area of

research which takes the role of automated fault diagnosis a step further. While fault tolerance could be achieved in its simplest by redundancy, fault accommodation in theory is expected to adapt controller parameters or reconfiguring the system to avoid and/or minimise the consequences of a fault although performance may degrade. A simple well established way of fault accommodation is based on pre-designed controllers, which are trained offline in known and expected failure modes. Thereafter, appropriate online failure accommodation techniques are suggested by a fault diagnosis system which analyses fault patterns online. Diagnosis of known faults in an FA enabled system is presented using the MM approach by researchers in this domain, whereas unknown faults are accommodated using neural networks. Similar to fault diagnosis research activities, most of the FA schemes are primarily developed based upon the powerful and well-understood linear control methodology.

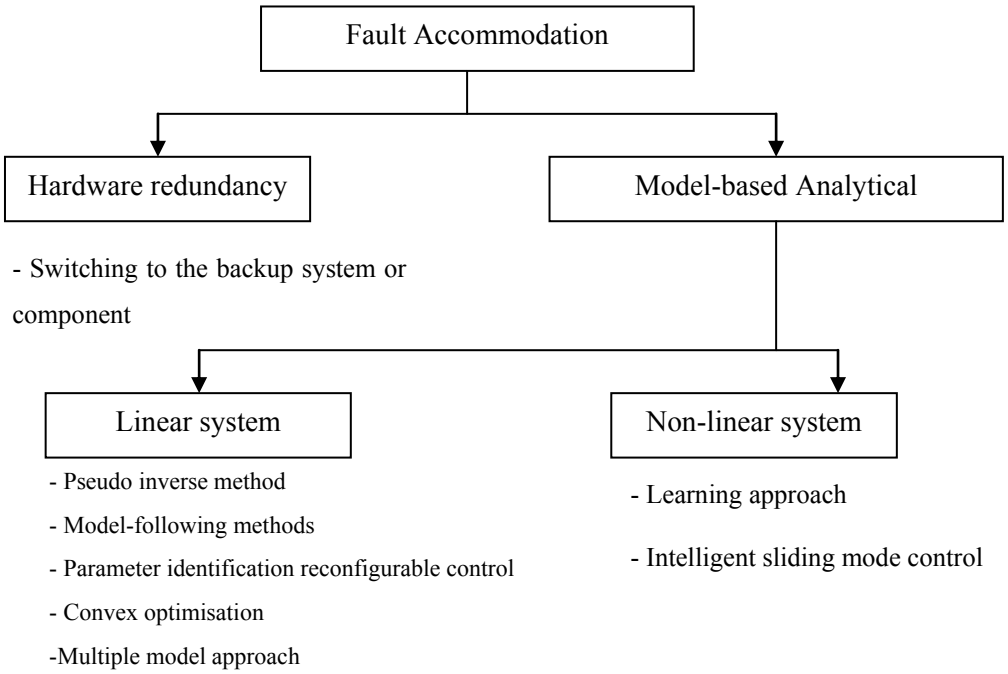


Figure 3.3: Known fault accommodation techniques [65]

For the envisioned SPS aim, the primary objective of FACS is to take necessary actions to prevent the system from becoming unstable and maintain the successful control mission after the action of detecting and isolating the emerging failures has been performed. This definition fits with the mentioned theories of FA in the research outlined in this section.

This scheme makes FA critically dependant on an accurate fault diagnostic system as well as prior understanding about known and expected faults, especially for the

integrated zonal distribution network for the envisioned SPS. This directly identifies the need to thoroughly understand faults at all system levels i.e. zonal, device and internal component level for the vital devices aboard the SPS architecture. In other words, besides the obvious need to develop an accurate fault diagnostic technique with reconfiguration (to achieve the FACS), the more fundamental need is to conduct a thorough study of failure modes, effects of faults and related system behaviour. In addition to this, a systematic research methodology needs to be formed which can help conduct generic research in the SPS domain.

3.4 Related research publications

This section highlights publications related to the research contained in this Ph.D. thesis. The previous sections in this chapter discussed the major contributions by researchers in the integrated SPS development domain. Also, research pertaining to vital devices aboard the notional warship was discussed regarding power electronic converters. The notable outcomes point towards a need to understand fundamental concepts of the SPS research domains that would aid in developing a FACS capable of accurately diagnosing faults and provide reconfiguration. In this regard, the need to conduct a detailed fault study for the given SPS network is discussed in [66]. This paper focuses on following well known methods under the umbrella of reliability analyses to enable understanding of fault modes. Here, a functional failure mode and effects analysis (FMEA) process is explained and applied to the SPS architecture, which helps outline critical sections and devices in the network. This research identifies the lack of a systematic methodology to understand pertinent failures within the notional SPS. The research is proposed to begin at a system level FMEA and progressing to the more detailed device/component level known as hardware-FMEA. With the help of an established and well known reliability analysis like FMEA, further research in this field gets a set direction, in this case by indicating that work needs to be concentrated on power converters. This methodology forms the crux of this Ph.D. thesis as well.

Research reported in [67] re-emphasises the need to conduct an FMEA on the envisioned SPS and lists its merits in enabling researchers to gain better understanding of fault causes and their effects. Results of machine learning techniques applied to simulation data obtained from the RTDS model of the SPS are presented in this paper. These models provide data in case of a line-to-line fault. Data

collected at the input and output of the power converters at every zone was used to classify and distinguish the fault from normal operational state as well as locate the fault. This paper deals with the system level disturbance and emphasises the need to continue research into studying device and component level faults and their associated risks.

[68] discusses the aim of developing the FACS and various anticipated capabilities of such a system. Also discussed are the modelling and simulation strategies to model the medium voltage envisioned SPS on the RTDS to conduct fault studies. This paper describes the necessary steps needed to be taken from the control system side to enable accommodation of faults. Also discussed are the algorithms employed to differentiate a line-to-line fault from normal operation and locate it within the distribution architecture.

The first step in this Ph.D. research towards studying component level faults through MATLAB-SIMULINK models is described in [69]. Here the SIMULINK models for the buck converter are developed such that switch open and short circuit faults can be simulated. The converter modelled on SIMULINK is the same in specifications as the one on the RTDS model which is used to simulate the zonal distribution system. This approach ensures consistency in producing data for system level disturbances such as line-to-ground faults as well as device level failures.

Research in [70] deals with component level fault diagnostics for the buck converter in detail using a novel model based method. Here, the SIMULINK model is built to closely match and mimic the signals generated by a hardware converter circuit. This methodology of validating simulation results with hardware data, which is prevalent in power electronics research is used here, where the authors demonstrate that the new technique is able to distinguish between switch open/short circuit faults as well as faults in other components like the capacitor and inductor.

3.4.1 Discussion

The papers described in this section progressively show the Ph.D. research from its initial phase to current phase. This study identifies the research gaps in the general SPS field, the major one being the lack of a meticulous and systematic methodology to enable a thorough understanding of faults, their causes and effects at all levels of the system. Further, to cater to the overall aim of developing an FACS, research into

AI based methods was carried out. Data driven classification techniques reported in [67-69] were used to help differentiate between normal and ground-fault scenarios modelled on the RTDS. Model based diagnosis methods were studied to deal with component level faults within a power electronic converter (in this case a buck converter) [70].

3.5 Chapter summary and conclusion

In the first section, this chapter highlighted research that dealt with fault diagnosis at the component level within power electronic converters, owing to the fact that little research in the SPS domain focussed on these devices. An important lesson learnt besides getting a grasp of prevalent diagnostic strategies for pertinent faults was the robust methodology followed by almost all the researchers in this domain. A common research validation theme adopted here is conducting accurate simulations on preferred software (e.g. MATLAB-SIMULINK) and comparing the results with a hardware test bench. These methodologies could be adopted with appropriate modifications to be applied in the relatively new field of the integrated SPS development.

The section following power electronics research discussed the concept of fault accommodation. The overall aim for the SPS development being the building of a FACS, it is important to understand what is meant by accommodating a fault. This application being related to fault tolerance, the papers listed belonged mainly to the control systems engineering domain. The fundamentals of developing a system capable of accommodating faults as mentioned in control theory were mirrored in the attempts of researchers desiring to integrate condition monitoring, fault diagnosis and reconfiguration. This review ensured that the SPS research adhered to well established definitions and theories regarding fault accommodation.

The final section described papers arising out of the Ph.D. research conducted. This thesis is focussed on attempting to bridge the gaps in existing SPS research with well established domains such as power electronics and fault tolerance based accommodation. An aspect emphasised here is the lack of detailed and generic methodologies that help understand faults and risks associated in the novel SPS.

Owing to this, the work in this Ph.D. proposes to begin research employing reliability analysis techniques such as FMEA. FMEA is a valid starting point to

understand expected malfunctions in a system whose behaviour is largely unknown. Another reliability analysis employed in this research is sneak circuit analysis (SCA). The next chapter is dedicated to the merits of using FMEA as a chosen reliability analysis for research in the integrated SPS arena.

Chapter 4 Application of reliability analysis techniques

4.1 Introduction

The previous chapter enumerated the various research domains that need to be examined in order to build understanding towards fulfilling the aim of developing the fault accommodating control system (FACS). The research in the envisioned integrated shipboard power system (SPS) community concentrated on understanding fundamental issues. Also, the focus was on analysing system level power management activities such as topology changes, reconfiguration and load shedding. Limited fault studies were conducted overall, the researchers who discussed risk assessment for the envisioned SPS, did so for system level issues such as line-to-line or line-to-ground faults.

The previous chapter also discussed prevalent fault diagnosis methods in power electronic equipment, especially converters. This is an important discussion owing to the fact that power electronic converters form a critical device in the envisioned zonal power distribution topology for the notional warship. From core power electronics community research, lessons are learnt which could be highly useful for application in the relatively new SPS research field such as:

- Emphasis on a meticulous and iterative methodology that considers fundamental principle studies to guide research.
- Consideration of artificial intelligence (AI) techniques to assess risk mitigation methods.
- Importance of validating simulation results by conducting hardware experiments with similar or identical specifications.

The research for the SPS development is still largely in its conceptual phase. There is also a lack of a strong research methodology which can be followed and one that includes meticulous studies of fundamental principles, fault studies and risk mitigation approaches. This fact is highlighted as a major research gap in this field. As a result, the logical first step to begin detailed analysis into possible risks associated with a novel architecture is proposed to begin with failure mode and effects analysis (FMEA).

FMEA can be used to support reliability, maintainability, testability, safety and logistics analyses. When performed in an accurate and timely fashion, FMEA information can be used for the following:

- To aid the design of test systems,
- Development of trouble shooting procedures,
- Planning of scheduled maintenance, and
- Development of integrated diagnostics capabilities.

An effective FMEA presents an examination of a system's strengths and weaknesses. This chapter describes the basics of FMEA and its applications as described through reliability analyses literature. Along with FMEA, another well established reliability analysis method namely sneak circuit analysis (SCA) and its related research is discussed here. Much like FMEA, SCA is also used for risk assessment, though specifically for electrical circuitry. This fact and the fact that SPS research deals with electrical power systems makes SCA a favourable risk assessment method to pay attention to.

4.2 FMEA applications and research

A guide to the history, development, method and application of FMEA can be found in [71]. This book provides the following description for an FMEA;

"An FMEA is a systematic method of identifying and preventing product and process problems before they occur. FMEAs are focused on preventing defects, enhancing safety, and increasing customer satisfaction. Ideally, FMEAs are conducted in the product design or process development stages, although conducting an FMEA on existing products and processes can also yield substantial benefits."

A comprehensive set of definitions, descriptions and case studies are presented in the book to familiarise oneself with the process of FMEA and its purpose. [71] is an important reference to learn the fundamental steps involved in carrying out a detailed and exhaustive FMEA of a given system.

One of the earliest publications listing the detailed use of FMEA is by Tashjian in [72]. Here the application of FMEA at the design phase is explained for the nuclear industry. The author clearly emphasises that FMEA is necessary to evaluate designs to understand effects of single faults. The paper presents an illustration of using FMEA in the design of the nuclear reactor protective system. The process is shown as a worksheet (table 4.1), which provides a systematic layout for tabulating information and keeps track of the analysis steps. The analysis is conducted by identifying components in the subsystem, listing their failure modes, and studying

their failure mode effects on system performance. These effects are observed for various operating modes of the system.

Functional level *System :* Reactor protective system *Sub-system :* Sensor channel *Equipment :* Pressure sensor				Diagram of system *(not shown here)*			Other details such as project number, date, report number etc.	
No.	Name	Failure mode	Cause	Symptoms and local effects including dependent failures	Method of detection	Inherent compensation provision	Effect on reactor protective system	Remarks and other effects
1.	Pressure sensor	Fail low	Corrosion wear, mechanical damage, heat	Low outpour and bistable in channel A. Bistable relays remain energised.	Periodic test.	Redundant channels B, C and D	Adversely affects reactor protective system trip logic	Channel A of parameter will not be in trip state other parameter not affected

Table 4.1: Example of FMEA for design evaluation [71]

The author further makes a distinction between annunciating failures and non-annunciating ones. A suggestion is made to develop means to detect non-annunciating failures or render them incapable of causing single faults. Table 4.2 shows the non-annunciating failures related to the nuclear reactor protective system discussed in this paper.

Component	Failure mode
DC power	*Fail high*
Trip relay	*Fail on*
Matrix relay	*Fail closed*

Table 4.2: Example of non-annunciating failure that need means to detect them [71]

The sample analysis outlined by Tashjian in [72] shows the meticulous nature of FMEA enabling better understanding of system operation. The steps listed for a basic FMEA are as follows:

- System under analysis is described
- System is represented in functional block diagrams
- System boundaries are defined
- Level of analysis is established (sub-system depth at which FMEA is conducted)

This early research reporting on the use of FMEA for a critical application such as the nuclear plant shows the faith of researchers in applying this analysis. Also, the author emphasises that apart from identifying components that could cause problems, FMEA also provides detailed documentation in the form of worksheets. To

understand the merits of FMEA and its appropriate application as well as method, this paper is important.

The process of FMEA has been extensively used and documented in the aerospace and aeronautics industries since about 1960 [71]. In the late 1970s, with the advent of computers, automating FMEA became an active research topic. A matrix based automated FMEA method is presented in [73]. This method consists of a pictorial representation of the relationship between components of the system, their failure modes and the resultant failure effects. The approach needs inputs in a set code that defines elements of the system, their failure modes and effects. From this information, the computer develops the matrix and generates formal effect statements. This process thus far initiates at human input and goes towards producing a computerised output which shows promise from the view of speed of output and reduction of errors. Although, it still means that a significant chunk of the process depends on human intervention at the initial end of the process.

Herrin added to the ability of computerising FMEA by introducing a reverse matrix method [74]. Here after the basic step of creating a list of components, their failures and effects, it is possible to trace backwards from every stage to highlight contributing factors that lead to the final failure. In many cases it is possible that a fault in one device, could lead to failure of another, which could be termed in simple functional terms as the inability to operate as desired. Instead of such a simple message, the reverse matrix method for FMEA is able to show the path (if any) of one fault causing or leading to another failure. This approach is an important step in tying FMEA to fault detection. Some advantages of this technique to conduct FMEA as described in [74] are:

- Fault isolation for any defined failure effect can be traced through lower levels to contributing components.
- Failure candidates can be ranked according to probability of failure.
- Identification of mission critical parts can be ascertained upon criticality ranking of the failure effects.
- The information in reverse format of FMEA can be utilised for maintainability, logistics, training and preparing documents like a maintenance manual.

Dussault in [75] reports prevalent FMEA techniques and automation tools. This is an important survey paper, wherein the author chronologically describes

- Traditional FMEA methods,
- Automation of traditional FMEA methods,
- Fault tree analysis techniques
- Sneak circuit analysis
- Combination of techniques

Here, a comparative analysis is made between various failure/fault study methods, with their automation and resultant evolution. This paper provides a wholesome overview of various methods under the umbrella of reliability analyses that are widely used to understand faults and failures occurring in a given system.

A tool to aid engineers to perform automated FMEA named 'The Flame System' is reported by Price et al. in [76]. The research presented is one of the early approaches to view automated FMEA as a knowledge based system related process. The application developed is for electrical circuits, to address design issues, faults and failures. The Flame system divides automated FMEA into three distinct parts:

1. Model building – Here the system technical information is used to build a software model. This contains a functional level description with intended system behaviour.
2. FMEA generation – The model developed is run to obtain fault effects information, which is followed by analysing the significance of the risk associated.
3. Interactive interface – This part allows the user to review the FMEA output and intervene in case certain modifications are necessary.

The research in [76] builds on the prior efforts to automate FMEA. The authors apply a detailed and structured approach to incorporate system knowledge to aid fault studies. The research forms an important basis to launch further research into combining traditional manual FMEA with emerging software capabilities.

FMEA mainly discussed in [71] - [75] dealt with applications to hardware. An important research contribution pertaining to FMEA for software is presented in [77]. Here the author presents system level software FMEA which is for the top level system design and carried out in the early stage of the design. A more detailed software FMEA is done during the later stages to verify that the protection intended in the top level design and assessed using system level software FMEA has been achieved. Such a software FMEA is reported to be in use for military and automotive products to assess the embedded safety critical real-time control systems. Some

crucial software failure modes for each software element, identified by the author are as follows:

- Failure of the software element to execute
- Incomplete execution
- Incorrect functional result produced
- Incorrect execution timing

Apart from the failure modes, it is important to also account aging of data as well as the ability of the software-element's design to protect against system failures in both hardware and software. However, an important precursor to software FMEA is a hazard analysis, wherein, the preliminary identifications where software issues could be a potential cause of the hazard exist. This paper presents an effective addition to traditional FMEA (done for physical hardware), especially viable for modern systems which use extensive amounts of software.

Another example of FMEA for software is presented in [78]. As in the previous paper, here too the author discusses early stage FMEA at the higher-level of the system. This is with an attempt to avoid design related issues that emerge during early stages of the development cycle. This paper describes a risk assessment approach using heuristics at the architectural level. The authors define a scenario as;

"A set of component interactions triggered by specific input stimulus"

Such scenarios form the basis of simulations using UML sequence diagrams. Component dependency graphs (CDG) are utilised in this research as probability models. CDGs are directed graphs developed from scenarios that consist of the following:

- Component reliabilities
- Link and interface reliabilities
- Transitions and their probabilities

The methodology to perform risk assessment proposed here is shown in fig. 4.1.

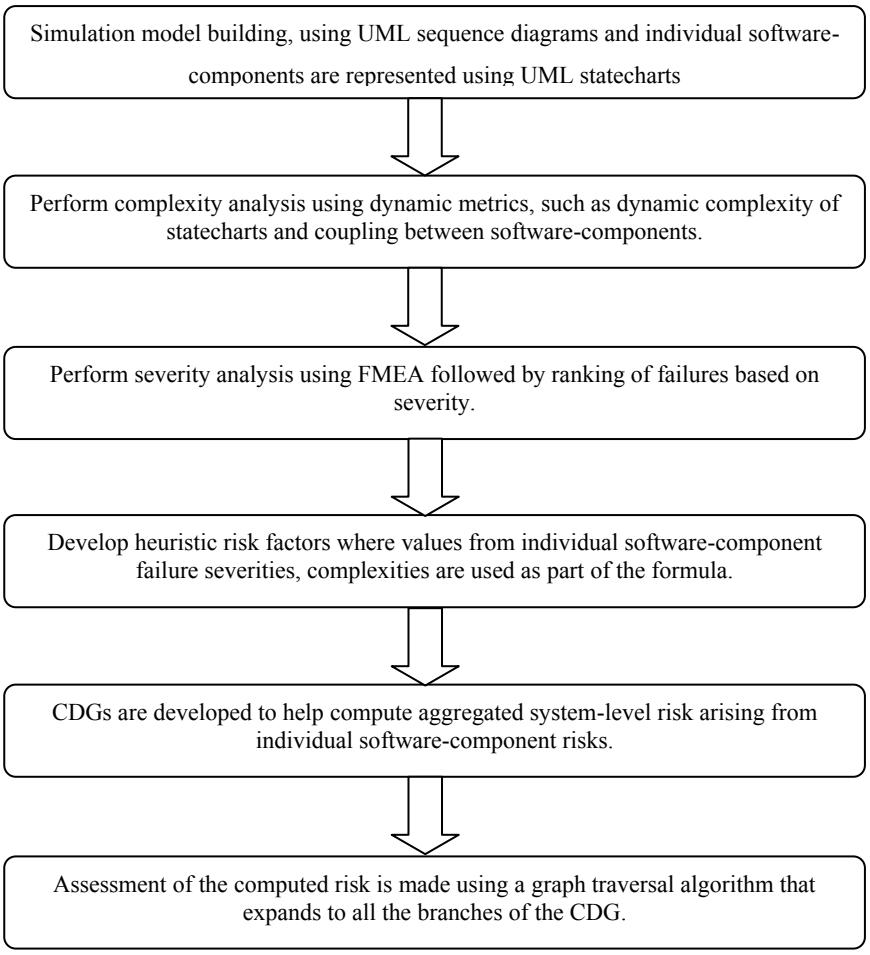


Figure 4.1: Methodology for risk assessment proposed in [78]

This paper meticulously demonstrates an approach to perform risk assessment for a software system where FMEA principles form a crucial part. As verification of their approach, the authors present an example of a pacemaker, where the proposed methodology is applied to perform risk assessment including a higher-level FMEA for the instrument detailing faulty components and the associated effects as well as severity measure.

Even though, the research presented does not go into hardware level details of faults and their effects, the higher-level of FMEA when properly executed provides ample information at the design stage to aid in improving the development of the product. The other important aspect of this research is the detailed methodology followed, which begins at modelling the system and progresses to studying dependencies, performing FMEA, ranking failures and guiding further course of action. The example and approach proposed here, is an important guide that could be adopted to conduct risk mitigation related research for the SPS development.

A generic approach to automating FMEA is presented in [79]. Here the authors aim to quicken traditional FMEA approaches using engineering information such as component specifications, diagrams and failure knowledge. This forms a generic approach to perform automated FMEA, with applications in systems for which models can be developed. The authors argue that in case models of the system do not exist, then a structured model could be made consisting of more elemental and individual parts for which models are more likely to exist. In this regard, the paper essentially emphasises the importance of paying attention to component level fault analysis which is an automatic progression from the higher system-level fault analysis presented in previously mentioned papers. In this research, FMEA is generated from fault tree analysis. The advantage of using fault trees is that failures due to more than one component can be recorded whereas classical FMEA considers typically single component failure causes. This combined information positively adds to the benefits of FMEA along with the time saved by automating the process. The authors use MATLAB-SIMULINK to build models from which the fault trees and FMEAs are generated. Although, this work does not possess adequate verification, the approach shows promise especially in cases where a large number of individual devices (whose models exist) are integrated to form one working system, such as a naval vessel and thus could find potential applications for SPS research.

An application of FMEA and fault tree analysis for power distribution systems is presented in [80]. This paper underpins the need of FMEA to address understanding of problems using a structured methodology. Further, the issue of dormant failures in distribution network is shown to be effectively addressed by performing a detailed FMEA. Such failures could exist in the system unrecognised and may show undesirable effects upon the occurrence of an associated failure such as a short circuit. Such a relation of one failure with another leading to system wide power outage (which is a major fault) can be studied using FMEA. The authors provide sufficiently detailed tabular examples of performing FMEA for an electrical network. An analysis repeated here is the forming of a severity ranking document for the failures. This work is a relatively recent publication that uses well established FMEA methods and applies it to a distribution network. In turn, it shows that a rigorous FMEA would have numerous benefits from the risk mitigation point of view in SPS zonal power distribution studies as well.

Fig.4.2. outlines the use of FMEA demonstrated by various researchers in the papers mentioned. The need to resort to FMEA is shown in the figure, its relative degrees of detail as well as the benefits and meaning of the FMEA results from the further research point of view.

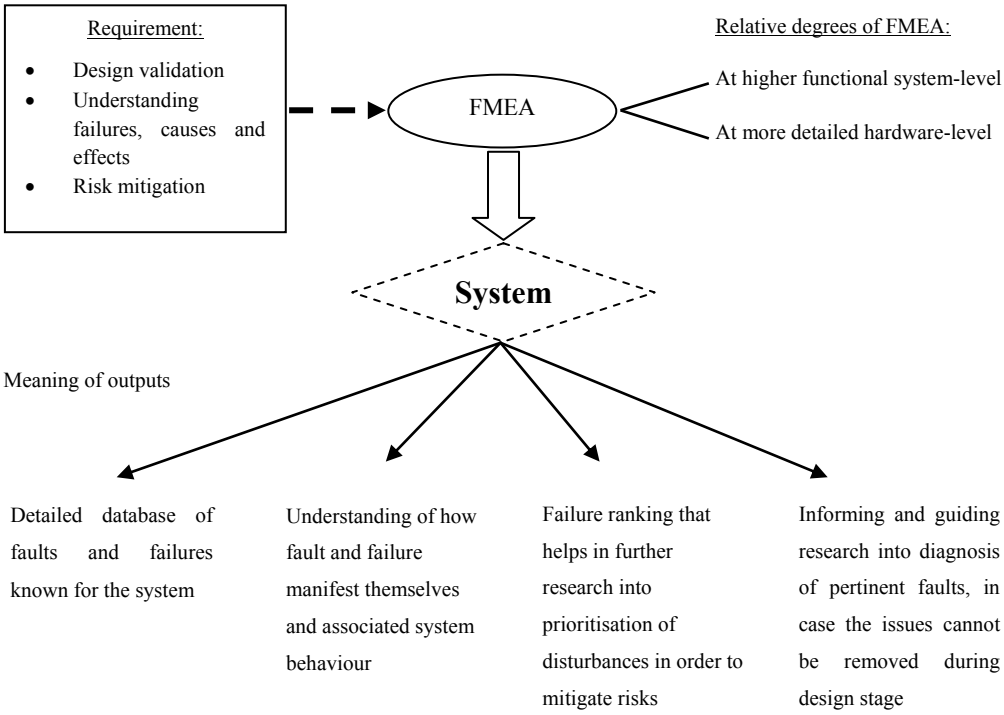


Figure 4.2: Need for FMEA, its varying degrees and meaning of FMEA outputs for research

A consistent feature in FMEA results is the ranking of failures according to their severity. This simultaneous process has been integrated into FMEA giving rise to a new term failure modes effects and criticality analysis (FMECA). Research to improve FMECA outputs is reported in [81]. Although as shown in previously listed papers, the notion of performing a failure criticality ranking is a task that goes hand in hand with FMEA. By integrating this task with traditional FMEA, the authors attempt to make the reliability analysis more compact and thorough. Research reported in [81] sufficiently details the methodology proposed along with tabular examples. This is an important paper which aims to combine traditional FMEA with an essentially separate failure severity study to result in a computerised tool for users. This research is one of the early benchmarks in trying to make FMEA outputs quicker, more meaningful and easy to understand for users giving rise to follow up

research into FMECA. Fig. 4.3 shows an overview of FMECA and its roots as well as outputs which in turn form inputs for further analyses.

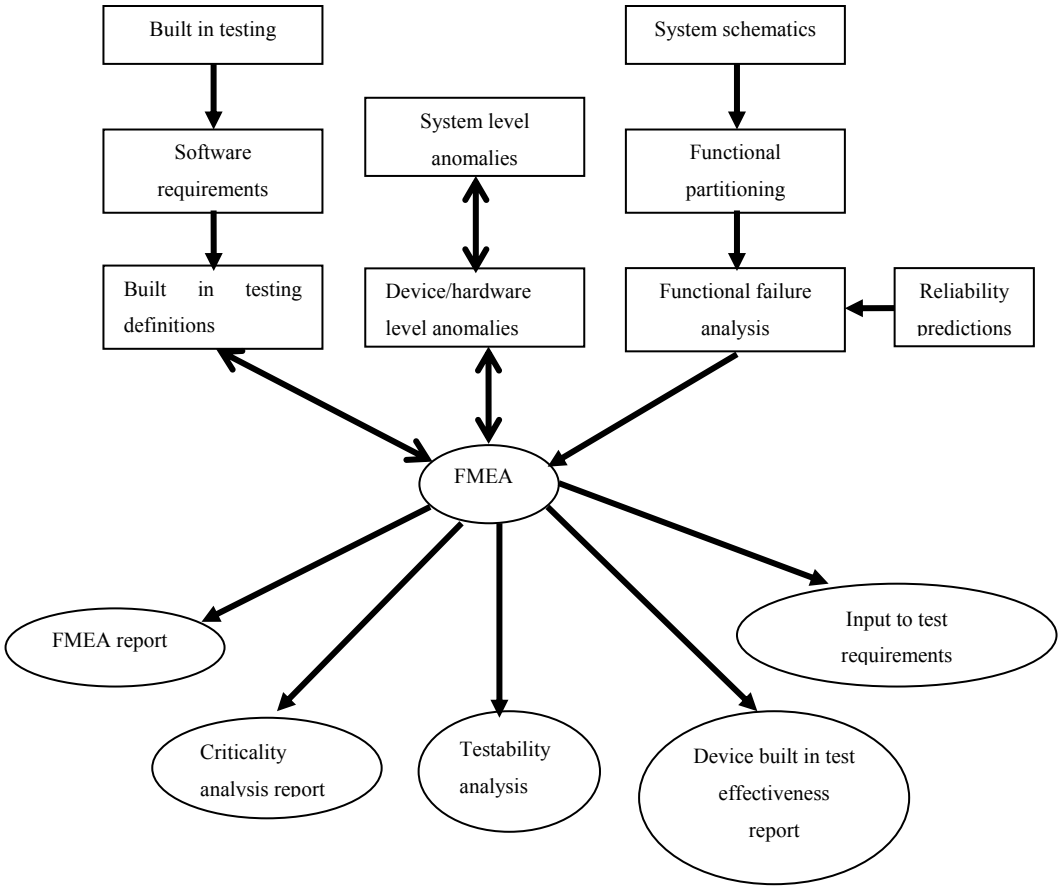


Figure 4.3: Overview of FMECA [81] with directional arrows that indicate flow of data

The papers described thus far deal with FMEA theory from its early introduction followed by its computerised automation and then its application to various real systems. The concept of FMECA also was mentioned in the previous paper. Researchers in [82] present research where artificial intelligence (AI) techniques like fuzzy logic and Bayesian networks are utilised in combination to improve the output of FMEA. Here domain knowledge about failures and their severities is taken from experts for an offshore system. This knowledge in combination with a Bayesian belief structure plus a fuzzy inference engine produce linguistic failure criticality estimates instead of numerical estimates. In this manner, understanding of pertinent failures can be obtained through prioritising. Such an approach is important from the viewpoint of providing decision support to humans with respect to failures in the

system, which is an important aspect of SPS research keeping in mind the reduced number of crew onboard future naval warships. An important drawback of this research however, is the lack of testing for more failures and faults in interconnected systems such as power networks and devices. Even then, the approach presented which makes use of AI methods in conjunction with well established reliability analysis such as FMEA is a robust approach to ensure progress in providing safety and risk mitigation. Further, this research may be viewed as an extension of FMECA performed using help of AI techniques.

Another example of utilising fuzzy logic to improve and enhance FMEA (or FMECA) outputs is presented in [83]. This research addresses the need for a consistent FMEA output that is able to perform decision support through linguistic failure criticality rankings similar to the research in [82]. The research in both [82] and [83] offers alternatives to the traditional risk priority number method of FMEA to rank failures, making use of intelligent techniques such as fuzzy logic. Although the validation in this case is not as robust compared to that in power electronics diagnosis research, the important contributions are the research approaches and methodologies applied in combination with traditional FMEA. Fig. 4.4 shows the overall progress of FMEA from its initial stages to current practice and the associated benefits.

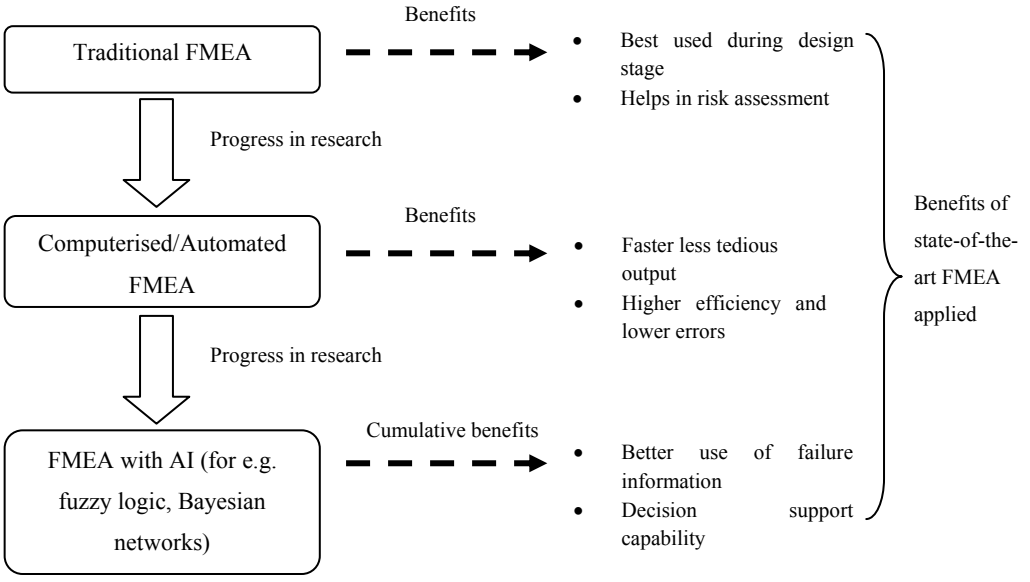


Figure 4.4: Progress of FMEA research and cumulative benefits of state-of-the-art FMEA

In [82] and [83], fuzzy theory was used to enhance FMEA. In [84] fuzzy theory is used to propose a FMECA methodology. The previous papers listed reported using system and domain knowledge to enhance FMEA. This partial notion here is applied in its complete form by creating a fully fledged expert system. Here a robust FMEA forms the crux of the research, which when combined with criticality assessment of failures results in a wholesome FMECA output. Validation of the proposed approach is done by analysing eight main components of a typical transformer substation which are:

1. Main transformer
2. Auto transformer
3. Potential transformer
4. Circuit breaker
5. Disconnecting switch
6. Current transformer
7. Surge arrester
8. Protective relay

A notable aspect is the utilisation of a fuzzy expert system which combines the severity and the criticality into the risk level which can help the decision maker to prioritise maintenance policies for each component. This in turn is shown to resolve ambiguity for determining priority order of maintenance task. Another important contribution of this research is the validation of the approach using a real system for reference. Previous research using fuzzy logic was inept at validating proposed methodologies. Here the researchers show the positives arising from combining FMEA with AI for a power system device (transformer) resulting in overall improvements for the user with regards to decision support. The proposed methodology seems promising for other power system related devices as well and could be utilised for power electronic converter related risk assessment for SPS research.

4.2.1 Discussion

This section outlined past and prevalent research in FMEA, which is one of the foremost reliability analyses techniques. FMEA although in use since the 1960s mainly in the aerospace and aviation industries, in more recent times, power distribution and software systems also utilised this analysis for risk assessments.

The previous chapter elaborated on power electronics research through showing detailed and robust research methodologies and the FMEA research presented in this section also presents equally detailed methodologies to tackle problems arising from risk assessment of systems. By default, the FMEA is an exhaustive process dealing with all system levels down to hardware devices and components. But research proposed lesser detailed levels of FMEA where the need to analyse top level system failures was considered sufficient as a preliminary measure for risk assessment. Such a top level FMEA was called a functional-FMEA while the detailed version is a hardware-FMEA.

FMEA applied to power domains dealt mainly with distribution systems where an integration of AI methods (fuzzy logic used commonly) and traditional FMEA was studied. A good FMEA produces a detailed understanding of the system components and operational states along with the expected know-how about possible failures. Using AI with such FMEA outputs was found to be particular advantageous for tapping this wealth of information in order to provide decision support for users. This positive result is specifically promising for SPS research wherein decision support in the wake of increased automation and use of newer technology, makes FMEA an automatic choice for risk assessment.

4.3 Sneak circuit analysis applications and research

This subsection outlines the applications and research relevance of another reliability analyses approach namely sneak circuit analysis (SCA). The previous subsection elaborated on the well established FMEA, its basics, state-of-the-art applications and proposed advancements. Research in [85] discusses the combining of FMEA and SCA to form a comprehensive reliability analysis technique. In this paper, a sneak circuit is defined as;

"An unexpected path or logic flow within a system that may under certain conditions lead to an unwanted or unintended action or inhibit a desired action"

This definition is standard for SCA which typically applies to electrical and electronic circuits. This paper explains the fundamentals of SCA and introduces the concept of using FMEA along with it for circuits. An important concept mentioned in this paper is functional FMEA. An FMEA conducted at a higher system level without tending to the device/component level details constitutes such a functional

FMEA, and although this notion has been used by researchers in papers outlined previously, in [85] a specific name is given to this kind of FMEA. The opposite of a functional FMEA is a hardware-FMEA where an exhaustive study for hardware devices and associated failures is conducted. Here, Savakoor et al. aim to integrate functional FMEA with functional SCA. Although this research is a conceptual proposal, the attempt is crucial to emphasise the importance of reliability analyses to study electrical circuits. This paper is a vital early contribution in order to understand intricacies of two widely used and prevalent reliability analysis methods and the results of their integration.

The trend of research shown in the previous section relating to FMEA dealt with automating the traditional method. The trend is similar in the case of SCA, wherein [86] researchers aim to build an automated tool. Price and Hughes aim to provide automated SCA tools for vehicle electronic systems. In this research SCA is again combined with FMEA though not as explicitly as in [85]. The software tool developed uses simulations to enable flexibility in conducting an SCA, in turn allowing the user to experiment. The ability of this approach is to provide useful information in addition to the standard SCA results. Therefore, the approach presented shows promise towards building diagnostic knowledge and potentially aiding in diagnosis research.

In [87], Hughes progresses the research reported in [86] by elaborating on functional level system modelling to aid SCA tasks. The research here focuses on modelling the system's component level behaviour combined with system functionality models. This approach involving functional modelling of both schematics and components forms a promising abstraction method that reflects the manner in which an engineer considers behaviour of systems and its constituents. Traditionally, SCA is based on connectivity information of individual components, and basic automation is present through heuristics that perform such an SCA. This research emphasises the advantages of modelling and simulation in combination with manual reliability analysis. Also, an important indication here is the lack of attention paid to detailed hardware level information usage for reliability analysis, in turn showing that basic top-level or functional data is sufficient to achieve acceptable performance. The relative ease in developing functional models therefore, may be a highly promising beginning to assess conceptual systems such as the envisioned SPS.

The literature on SCA mentioned until now, deals with in general an overall system's reliability. In most cases, this overall system typically consists of a single circuit or a network that can be treated as a single entity, thus applying SCA to determine unwanted current paths or FMEA to understand risks. A vital contribution towards device and in turn component level reliability assessment is presented by Qui et al. in research papers [88-92]. These five papers report application of SCA for power electronic converter types in turn providing methodologies to improve designs and understand fault behaviours. A detailed hardware FMEA is a promising method to understand power converter risks, but the added SCA process on these devices enhances the risk assessment output by providing information about current paths at the component level. Such detailed information is vital if one is to build up knowledge about fault causes, effects and associated risks, which in turn would benefit the overall aim to achieve an automated system capable of accommodating faults.

A detailed SCA based study for the step-down DC-DC converter is presented by Qui et al. in [89] and [88]. Well known theoretical equations for the converter's operation are used for explaining the current paths during normal working. This strong theoretical knowledge base is utilised to predict various combinations of sneak paths that could cause unwanted behaviour from the circuit. The robust validation methodology shown in power electronics research arena of verifying theory with hardware test setups is followed by Qui as well. This process provides more credibility to theoretical derivations and these papers form a vital reference to progress SCA at the device level for power electronic converters.

Qui et al. extend their research to include multi-cell converters keeping in mind their emergence as preferred power delivery devices in high power and power dense applications. In [90, 91], the n-stage converter is analysed using SCA. In these papers, an important methodology to compute sneak paths is introduced, called the generalised connection matrix using directed graphs. By using this method, the authors propose a step-wise process to manually compute sneak paths and take measures to eliminate the occurrences. The directed graphs are diagrammatic depictions of current paths from one component to another within the device (in this case a step-down power converter). These diagrams incorporate directional information of the current paths, thereby adding an element of background

information for the analysis. This aspect is important because, in case of utilising this technique for automated risk assessment, utilisation of device circuit knowledge could come handy in providing decision support. Further, the diagrammatic representation makes it easier for the user to visualise the current paths as well as remove analysis errors and backtrack when they occur. Qui et al. provide a continuous research attempt wherein the SCA applied begins at a basic converter and then progresses to the multi-cell type of converter. Also, the matrix method to formulate sneak paths shows promise in case of automating the process.

Extending the research further on from step-down converters, the same researchers form a generic SCA methodology for the step-up power converter in [92]. This is a logical extension of the research which eventually provides a topology independent SCA methodology for assessing power converters in general. In [92], the researchers provide illustrative examples of making a directed graph for a given converter circuit, followed by deriving the generalised connection matrix. The determinant of the matrix provides an equation in symbolic form which indicates current paths among components of the device. Thus a user can know which paths are undesirable and hence take measures to try and account for them (ideally eliminate them altogether). This methodology used by Qui et al. to determine design defects among power converters forms a crucial body of research to ensure safe operation of these devices. This in turn relates positively to SPS research in which the distribution architecture is set to have numerous converters making them a vital device for the zonal network as shown in SPS research community papers outlined in the previous chapter.

In the FMEA research presented, more recent advances aimed at utilising AI methods to enhance the traditional FMEA outputs. For SCA research, relatively fewer attempts exist to attempt a similar thing, though one notable contribution is [93]. Here, a neural network (NN) in MATLAB is used to perform SCA using back propagation algorithms. The information fed to train the NN is the circuit connectivity data. The NN then computes the various switch combinations to decipher the current paths, and thus the sneak circuits if any can be determined. This process is essentially similar to the generalised connection matrix yielding current paths, but provides an approach using AI based automation. The research in [93] highlights related publications that also make use of AI techniques to enhance SCA.

The authors, Liping and Tao in [93], aim to present a prognostic methodology to predict the sneak paths that may occur in circuit topologies. Effectively, given a circuit, the methodology presented is able to compute possible combinations of the constituting components from which certain resultant topologies could be undesirable leading to failure. One major issue with the technique is the premise of the undesirable circuit topology coming into existence. As there is no rationale explained with regards to probabilities and practical occurrences of the undesirable topologies, calling the approach's outputs as a prognosis is questionable. As mentioned earlier, the authors use MATLAB to model the NN and like researchers in power electronics, the software finds applications for reliability analysis as well.

4.3.1 Discussion

Like FMEA, SCA is also a well established reliability analysis technique specifically applied to electrical and electronic circuitry. The research community for SCA followed roughly in the footsteps of FMEA advancements with an eye on automation, enhancing outputs and combining with AI methods.

An important research proposal was to combine the FMEA and SCA. Such an approach seems particularly promising for novel electrical distribution systems (such as the zonal SPS) because;

1. For a power network without prior benchmarks, FMEA is a logical starting point to assess risks, their effects and inform further research into mitigation of such occurrences.
2. For the individual electronic devices within the novel network, SCA provides a well researched methodology to analyse risks from the current paths point of view.
3. Combining FMEA and SCA forms a generalised pair of risk assessment methodologies that can promise to provide a rich information database containing data on failures, fault manifestations, operational states, undesirable circuit behaviour, risk causes and risk effects.
4. Learning from using AI with FMEA and SCA, the rich information obtained from the reliability analyses outputs can be of potential use for decision support.

4.4 Chapter summary and conclusions

This chapter specifically dealt with a survey of prominent research into reliability analyses techniques. The two most prevalent techniques discussed were FMEA and SCA. The rationale for any reliability analysis to be conducted on a given system is

to gather information on risks that could be associated with various operational modes. This fundamental need in turn drives further research into studying associated effects of these identified risks; mitigate the effects and perform remedial actions. This overall study underpins the importance of understanding pertinent faults and efficiently diagnosing them.

The previous chapter elaborated research within the SPS community. A major gap in the research was seen in risk assessment of the novel zonal architecture at a functional level as well as hardware level. Hence, it is imperative that attention must be given to established risk assessment methods such as FMEA and SCA which either individually or as a combination offers a promising initial approach to understanding faults and associated risks for the notional system.

An important output of reliability analyses such as FMEA and SCA is a database of information regarding system operation related to a variety of fault scenarios. The added process of ranking failures as per severity provides further insight into faults and associated risks. Such information is vital to guide further research into diagnostics which deal with methods of identifying and managing the associated risks. Reiterating the fact that such detailed risk assessment for the notional zonal SPS is absent, it is a logical step to proceed to conduct a reliability analysis on the system at hand. Hence, the following chapter reports on FMEA conducted on the zonal SPS network at both functional and a hardware level which underpins the critical sections and devices to focus further research from the fault diagnosis point of view.

For detailed studies, researchers made use of MATLAB-SIMULINK as a simulation and modelling tool for both FMEA and SCA work. Also, MATLAB-SIMULINK was used while combining AI techniques such as fuzzy logic and NNs with reliability analysis. The faith shown by researchers in this software tool is promising for conducting simulations in SPS related research as well that could potentially stem from reliability analyses and AI combinations.

Chapter 5 Application of FMEA for the Shipboard Power System model studied

5.1 Introduction

Previous chapters highlighted research prevalent in the notional zonal shipboard power system (SPS) domain as well as the research into reliability analyses techniques especially failure mode and effects analysis (FMEA) and sneak circuit analysis (SCA). The rationale for emphasising on an FMEA as a starting point in the SPS research for understanding of risks and their mitigation was also explained. This chapter focuses on conducting FMEA for the SPS studied. The analysis largely follows procedures outlined in relevant literature, while modifications to conventions have been reasoned.

The notional SPS having a zonal topology is explained in this chapter. The zonal network and operational characteristics of constituents is also outlined to aid in conducting an effective FMEA.

5.1.1 Medium voltage zonal shipboard power system topologies

This research contains two types of topologies studied under the category of notional zonal SPS. These two types are described here. This thesis however focuses on one type of topology and the reasons for this have been outlined in this section.

5.1.1.1 Original zonal SPS topology with AC power generation ring

The notional next generation warships proposed by the U.S. Navy will operate on the medium voltage AC (MVAC) and medium voltage DC (MVDC) systems. These systems are anticipated to heavily rely on power electronics which are relatively new and unproven technology [94] for naval SPS applications. The zonal topology is expected to use increased power electronics with a view to enhance controllability and flexibility of the SPS. The U.S. Office of Naval Research (ONR) has defined the control challenge problem [11, 95] that can be summarised as;

"To provide continuous mobility, power and thermal management for shipboard combat system despite major disruptions involving cascading failures"

The proposed MVAC and MVDC zonal power distribution topologies are modelled based on the ONR reference system [11]. Recommendations and

information about contemporary practices with specifics about MVDC shipboard systems is contained in [96].

A Real time digital simulator (RTDS) model of a representative medium voltage zonal power distribution system has been developed at the Centre for Advanced Power Systems (CAPS) of the Florida State University (FSU). The system modelled on the RTDS is shown in fig. 5.1. The model consists of a 4.16kV AC ring bus that connects two main turbine generators each of 36MW capacity and two auxiliary generators of 4MW each. This AC ring bus consists of distribution modules that could include transformers, load centres and switchgears [97] to facilitate transfer of power. The AC ring through the distribution modules supplies two propulsion motors, a pulsed power load and 3MW radar which constitute vital loads.

The AC ring bus supplies a total of three power electronic converters (AC-DC three phase rectifiers) that convert the AC input to 1kV DC output. This 1kV DC output is fed into longitudinal port and starboard DC busses that supply the zones of the SPS architecture. Each zone is supplied by DC-DC step down power electronic converters (also called buck converters) at either side (port and starboard). These buck converters convert 1kV DC to 800V DC.

The zones of the modelled SPS could have either DC and AC loads or both. These loads are a lumped (non-segregated) mathematical model that draws power from both converters simultaneously which in other words means that the zonal loads are shared by both converters. The zonal buck converters supply the zones via a 4% droop control technique through auctioneering diodes [94] to ensure uni-directional current path. More detailed implementation specifics of the RTDS CAPS-FSU model can be found in [98] while general developmental reports are provided in [99].

5.1.1.2 Newer zonal SPS topology model without AC power generation ring

An alternative zonal topology incorporating majority MVDC distribution is being simultaneously researched and modelled on the RTDS at CAPS-FSU. This alternate topology is shown in fig. 5.2. Here, the AC ring of the original zonal approach is eliminated and the AC to DC conversion is done at the output of the main generators. By this method, the only AC sections are immediately at output of power source and in places where specific DC to AC conversion has taken place owing to particular load demands (such as in some zones with AC loads). The port and starboard DC

busses carry current at 5kV as opposed to 1kV in the original model while similar to it; the zones are supplied at 800V by buck converters.

In the alternate topology, the zonal loads are modelled separately and are shown in fig. 5.3. Here a DC-AC conversion is shown to supply AC loads and the other loads in the zone are predominantly DC. Power management research using this alternate approach has been reported in [100] by Srivastava et al. Further research is ongoing at CAPS-FSU related to variations in the zonal SPS and associated system-level power management issues

5.1.1.3 Zonal SPS topology used in this research

For the research presented in this thesis, the zonal SPS model having both MVAC and MVDC parts is used as reference (fig. 5.1.). The presence of distinct AC and DC sections in the chosen topology means that different types of power electronic converters are needed to execute specific power demands. As a result, the zonal segregation displayed in fig. 5.1 for this topology shows that AC-DC, DC-DC and DC-AC converters are abundantly used in various sub-sections. This extensive use of power electronics in power systems has been known to produce significantly higher levels of harmonic distortions [101]. These can cause problems to normal operation of electrical machines and power transformers as well as have negative impact on the protection system, power quality and intelligent devices using algorithmic calculations for fault diagnosis [102-104]. Adding to these aspects is the fact that in general, SPS are finite inertia isolated power systems. The proposed zonal SPS is expected to have large number of power electronics equipments that are tightly coupled [105] such that disturbances experienced in one section could potentially impact other places on the ship.

Also, owing to the fact that the zonal SPS field in itself is in a conceptual phase, the topology of fig.5.1 is relatively better established and well researched compared to newer variants. Keeping all these mentioned challenges and aspects in mind, the zonal topology based on the ONR reference system represented in fig.5.1 provides an ideal platform to commence research into studying faults in a novel architecture and finding methods to mitigate associated risks.

Later sections of this chapter focus on FMEA conducted on the SPS described in 4.1.1.1.

Figure 5.1: RTDS e-ship model subsystem partitioning (courtesy: CAPS-FSU).
Abbreviations explained in table 5.3.

Figure 5.2: Alternate majority DC zonal topology modelled on RTDS (courtesy: CAPS-FSU). Abbreviations similar to those in table 5.3.

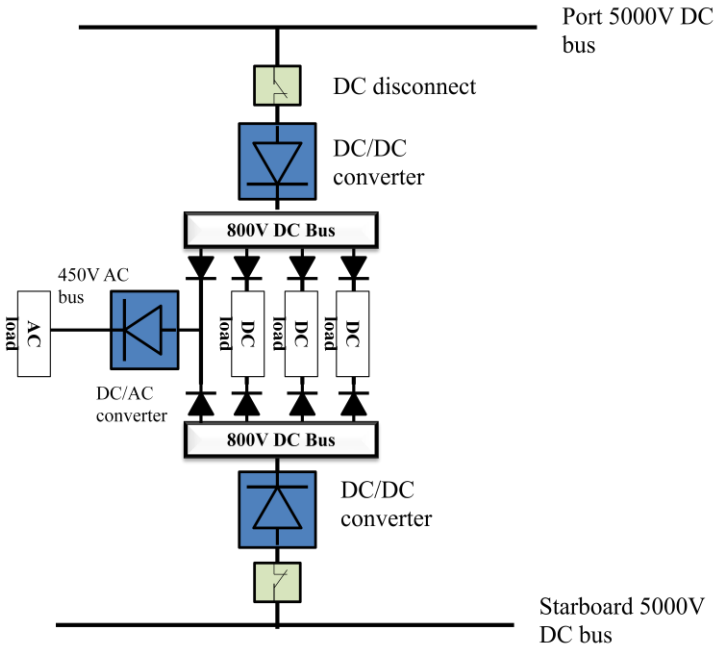


Figure 5.3: Load centres (courtesy: CAPS-FSU)

5.1.2 FMEA process

The goal of FMEA is to review a system or process to find and understand the ways in which failures can occur and indicate the resulting effects of these failures on the system. An inductive, bottom-up method is generally used to evaluate the potential for failures. A comprehensive analysis of a complex system such as naval warship may consist of separate hardware FMEAs for each subsystem or device. A thorough FMEA is expected to analyse dependent causes and effects of failures. These individual FMEA results could then be aggregated to form an overall FMEA for the system.

An alternate direction could be the top-down approach. This could be used typically when the dynamics of the constituent subsystems or devices are relatively unknown, but the overall system's operation as a whole is better defined. This approach could be adopted for systems whose operational aims and expected performance has been theorised, but the system uses a large number of individual subsystems that are highly dependent on each other creating the need to study these interactions from a risk management point of view. In such a scenario, a top-level analysis provides a good starting point to begin FMEA. This reasoning goes well for the notional SPS which is still in a conceptual phase and where extensive

documentation on fault related behaviour and associated risks of individual subsystems would help inform further research.

Once the level of detail is established for an FMEA, criticality analysis of failure modes could be performed and plans of actions can be defined for resulting risk categories. For example, high-risk failure modes might require the formulation and implementation of plans to eliminate the possibility of their occurrence; medium-risk failure modes might require the design and installation of various types of detection mechanisms; low-risk failure modes might require no immediate action. This distinction of remedial action is a useful output from FMEA that can aid finding best suiting fault diagnosis techniques. In this section, a description of the two sub-types of FMEA has been provided. In the studied SPS, three distinct system levels (or layers) which differ in complexity could be considered.

- Highest (system) level – Comprises of the entire SPS. This level would have a single mission goal during respective scenarios. The disturbances associated with this level affect the entire system and a common example for a system-wide disturbance for the proposed SPS is a line-to-ground fault.
- Middle (sub-system or zonal) level – This level comprises the zones of the notional SPS considered to be "smaller systems" operating within their respective parameters and mission goals. Typically, disturbances and faults at this level remain constrained within the originating zone.
- Lowest level (device and/or component level) – This is the lowest level comprising of individual devices and their components. Here the devices themselves are considered stand-alone systems whose faults may or may not affect the sub-system (zone) the device is in or the entire system. This level needs the most detailed work with regards to fault studies owing to numerous and varied types of equipments, their interactions, and fault associated effects with their risk assessment.

Detailed references to conducting an FMEA are provided in [71]. The ten fundamental steps for an FMEA are mentioned here as follows:

1. Review the process or product.
2. Brainstorm potential failure modes.
3. List potential effects of each failure mode.
4. Assign a severity ranking for each effect.
5. Assign an occurrence ranking for each failure mode.
6. Assign a detection ranking for each failure mode and/or effect.
7. Calculate the risk priority number (RPN) for each effect.

8. Prioritise the failure modes for action.
9. Take action to eliminate or reduce the high-risk failure modes.
10. Calculate the resulting RPN as the failure modes are reduced or eliminated.

The above steps to varying degrees of application are a necessity for the SPS studied and have been demonstrated in this chapter. To effectively conduct a meticulous FMEA, detailed tabular worksheets are also mentioned in [71] and an example is shown in table 5.1.

An example of FMEA conducted on an engineering system in a tabular format is seen in [72]. The corresponding format as used by Tashjian [72] is shown in table2. table2 even though less detailed than table1, encompasses necessary aspects for understanding possible failures and their root causes, information of which is useful to guide further research into diagnosing the perturbations (faults, failures etc.).

In this research, certain details mentioned in the above formats have been omitted while certain additions have been made. One such difference is the application of two sub-parts of FMEA. These types of FMEA namely, functional FMEA (F-FMEA) and hardware FMEA (H-FMEA) are explained by Savakoor et al. in [85] and are described in the next sub-section.

This chapter demonstrates these two FMEA approaches, F-FMEA and H-FMEA on the SPS model studied for this research. The emphasis is laid on F-FMEA which serves as the most appropriate method to start analysing failure cause and effects in a complex system without benchmarks such as the proposed zonal SPS. F-FMEA helps identify critical sections and devices of the studied SPS architecture, helping focus further research. The next step after F-FMEA is the more detailed H-FMEA on the identified critical devices from the risk assessment point of view.

Action results	RPN				
	Detection				
	Occurrence				
	Severity				
	Action taken				
General FMEA process	Responsibility and target completion date				
	Recommended action				
	RPN				
	Detection				
	Current controls, detection				
	Current controls, prevention				
	Occurrence				
	Potential cause(s) of failure				
	Severity				
	Potential effect(s) of failure				
	Potential failure mode				
	Component and function				
No.		1.	2.	3.	4.

Table 5.1: Example of a detailed and standard FMEA table as given in [71]

Functional level				Diagram			Project no., date etc.	
No.	Name	Failure mode	Cause	Symptoms and local effects including dependent failures	Method of detection	Inherent compensation provision	Effect on system	Remarks and other effects
1.								
2.								
3.								

Table 5.2: Relatively less detailed FMEA table as given in [72]

5.1.3 Two sub-parts of a detailed FMEA

FMEA as a detailed process can be divided into two parts of differing levels of technicality. These two parts are F-FMEA and H-FMEA and are elaborated by Savakoor et al. in [85]. The fundamental differences between F-FMEA and H-FMEA are described in this section.

(a) Functional FMEA (F-FMEA) – This type focuses on the functions that a system, process, or service is to perform rather than on the characteristics of the specific implementation. When developing a functional FMEA, a functional block diagram is used to identify the top-level failure modes for each functional block on the diagram. For example, a heater's two potential failure modes would be: "Heater fails to heat" and "Heater always heats". Another example of a functional FMEA would consider that a capacitor is intended to regulate voltage and then analyze the effects of the capacitor failing to regulate voltage. It would not analyze what would occur if the capacitor fails because of an open-circuit or shorted-circuit. As FMEAs are best begun during the conceptual design phase, long before specific hardware information is available, the functional approach is generally the most practical and feasible method by which to begin an FMEA, especially for large, complex systems that are more easily understood by function than by the details of their operation. When systems are very complex, the analysis for functional FMEAs generally begins at the highest system level and uses a top-down approach.

(b) Hardware FMEA (H-FMEA) – This type examines the characteristics of a specific implementation to ensure that the design complies with requirements for failures that can cause loss of end-item function, single-point failures, and fault detection and isolation. Once individual items of a system (piece-parts, software routines, or process steps) are identified in the later design and development phases, component FMEAs can assess the causes and effects of failure modes on the lowest-level system items. H-FMEA is also referred to as piece-part FMEAs, and are more common than F-FMEAs since usually in a system, the individual components are well known and altogether novel components as such are rare. H-FMEAs generally begin at the lowest piece-part level and use a bottom-up approach to check design verification, compliance, and validation.

For complex systems, a combination of (a) and (b) may be required which constitutes a "Detailed FMEA". In the case of the SPS, the combination of F-FMEA

and H-FMEA is necessary as it is a system still in the conceptual phase, without the presence of any hardware based benchmarks. Fig.5.4 illustrates the difference in scope between F-FMEA and H-FMEA showing that both together constitute a detailed FMEA. Also, FMEA is iterative in nature, needing regular exchange of and updating of data on failure causes and effects. This is shown by bi-directional arrows in both F-FMEA and H-FMEA in fig. 5.4.

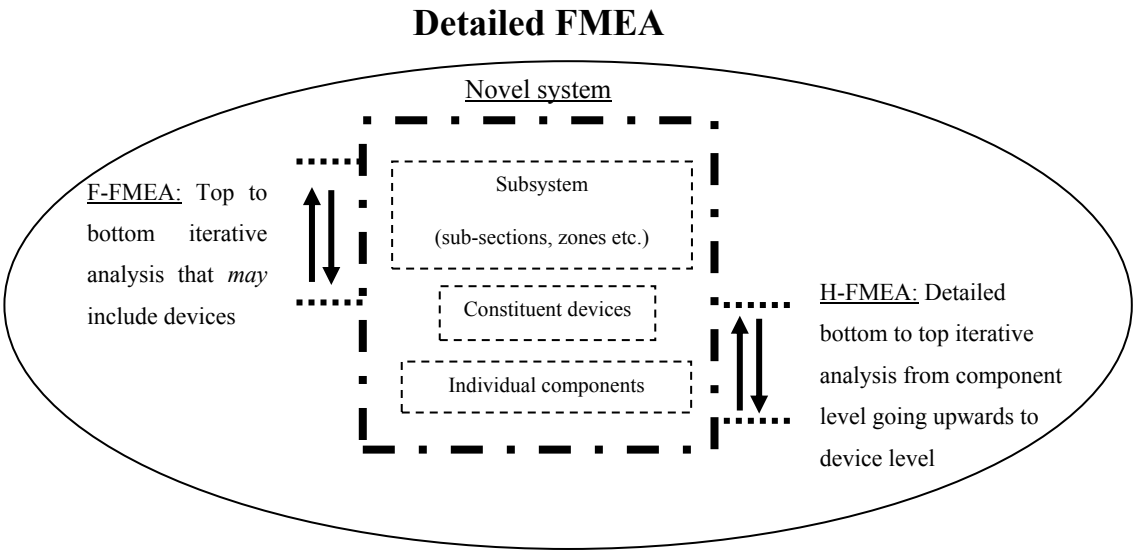


Figure 5.4: Subtle difference between F-FMEA and H-FMEA that add up to produce a detailed FMEA

F-FMEA applied on the notional zonal SPS provides information on critical sections and devices in the network. This output in turn guides the more intensive H-FMEA to focus on such critical devices for fault studies. Outputs of H-FMEA in turn narrow down vital components whose faults and failures may lead to disturbances in the sub-system or system that could be termed as catastrophic (or highly severe). This progressive filtering provides a list of pertinent faults on which further studies could be centred. The next logical progress would be into testing known diagnostic methods to differentiate faults or develop novel techniques. Another outcome could be the development of prognostics techniques to help predict failure times in order to prevent major faults if possible.

5.2 Functional FMEA (F-FMEA)

The block diagram of the zonal SPS modelled on the RTDS housed at CAPS-FSU is shown in fig. 5.1. The details of the constituents of the general SPS model on the RTDS are explained here.

5.2.1 Ranking of sub-sections and devices to create hierarchy

An important aspect that can be added here is ranking of a zone or device depending on its importance. This is similar to ranking of failures as per severity which is shown in table1. Ranking a sub-section helps prioritise attention for remedial action. Such ranking could be done based on the constituent devices in the zone (which in turn need to be ranked as per importance). In other words, even though the F-FMEA does not go into component level detail like the more intense H-FMEA, it incorporates sufficient technical details to provide a wholesome understanding of the system's hierarchy. But before a ranking scheme can be put in place for the specific case of the studied SPS, it is necessary to outline a set of general definitions and guidelines.

5.2.1.1 Defining types of devices and their importance

1. **Primary power source –** These are typically turbines (prime movers) that are the sources of the electrical power aboard the vessel. An example are gas turbine generators, steam turbine generators etc.
    - *Importance definition –* Such devices are deemed here of "Rank 1 importance" owing to the fact that their failure would cause no power output and as such is one of the most singular issues.
2. **Power delivery device –** These are devices that transfer power either without any change or with specific modifications. An example of such devices is switchboards while an example of specific power delivery devices are power electronic converters (PEC).
    - *Importance definition –* These types of devices are deemed of "Rank 2 importance" because they supply the power from the source to respective loads. Even though power sources may be operating normally, any issue with power delivery devices would cause operational problems at the receiving end.
3. **Load –** These are consumers of power and convert electrical energy at their input to some other form of energy at their output.
    - *Importance definition –* These types of devices are deemed of "Rank 3 importance" in general after the power source and delivery modules. However, ranking of loads is slightly more complex than other devices owing to the fact that some loads may be more vital to the

SPS's mission aim than others. To establish this internal hierarchy, the connection of the load to preceding device could be considered. For example, a load connected directly to a source (or with just one power delivery device between source and load) would be of higher importance than one that obtains power from a series of power delivery devices.

4. **Secondary power source –** This class of devices could be defined as energy storage modules such as batteries that initially consume power to charge and then can be used as power sources while they discharge.
    - *Importance definition* – These types of devices are deemed of "Rank 4 importance" and as such are of least importance in the established hierarchy of devices.

To simplify understanding of the zonal system represented in fig. 5.1, a line diagram could be used to interpret the network. The resulting line diagram in fig. 5.5 shows a general representation for zones that have similar constituents. The colour code for voltage in fig. 5.5 is the same as that in fig. 5.1. To represent starboard and port side PCM-1 PECs, the suffixes S and P have been used respectively in fig. 5.5.

Using line diagrams, one can begin breaking the overall zonal SPS into smaller sections on which an F-FMEA can be effectively commenced. But before that, more information needs to be clearly outlined preferably in a tabular format. Table 5.3 shows the various types of constituent devices and related useful information. The devices are labelled according to their type as defined above. Also, their relative importance is stated.

Table 5.4 lists functions of devices. Table 5.5 shows the devices as part of zones and other sub-sections along with the functions of the sub-sections. The listing of functions by sub-section or zone and also device is the fundamental step to begin F-FMEA and to get a clear view of various operations from a functional point of view.

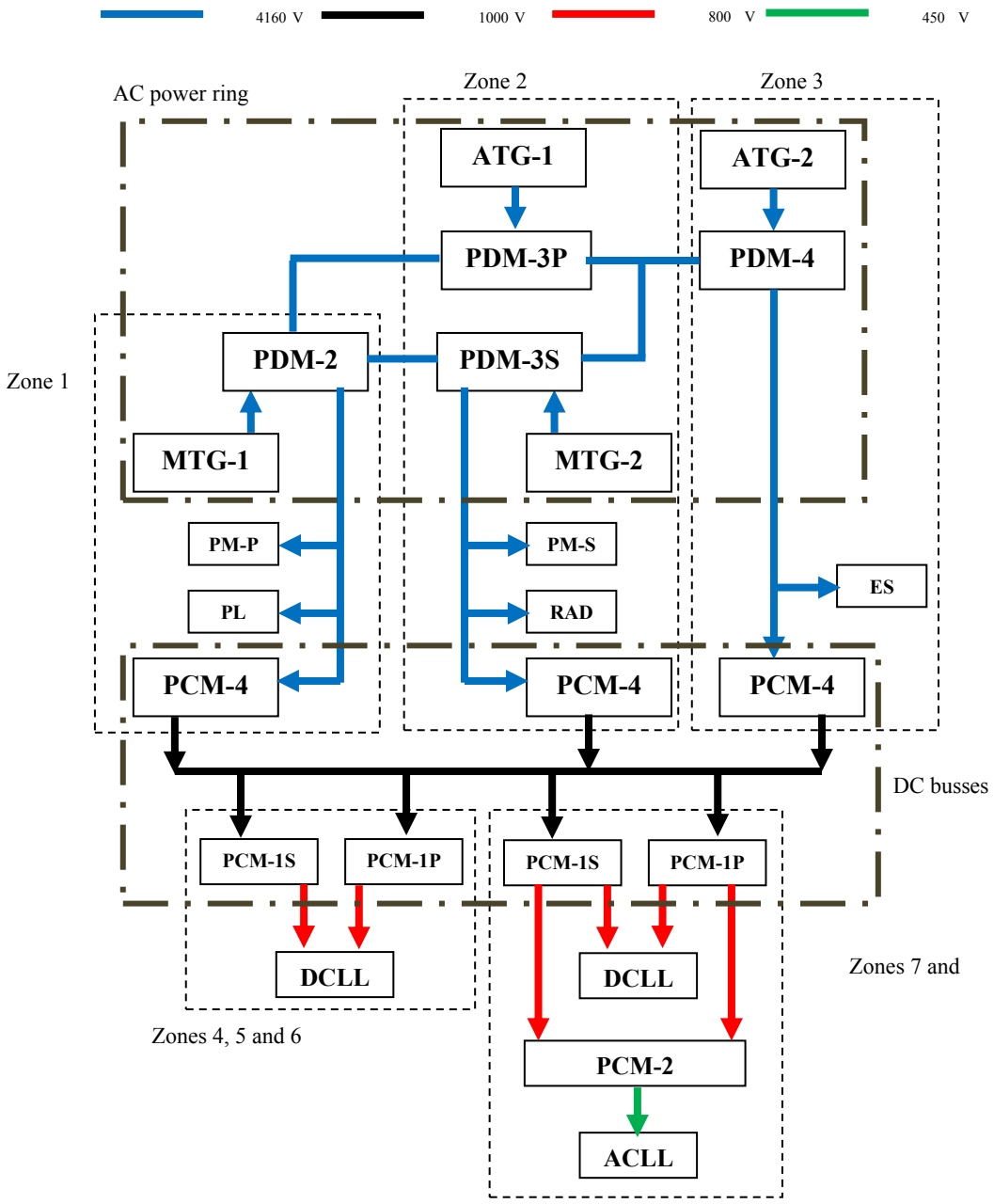


Figure 5.5: Line diagram to represent the modelled SPS

Device	Quantity	Type of device	Importance rank	Relevant information	Abbreviation used
Main turbine generator	2	Primary power source	1	Typically gas turbine generators of 36MW each.	MTG-1 and MTG-2
Auxiliary turbine generator	2	Primary power source (back-up)	1	Typically gas turbine generators with lower rating than main generators (4MW each).	ATG-1 and ATG-2
AC-DC rectifier	3	Power delivery device (specific PEC)	2	Consists of power semiconductor switches to convert AC to DC (4160V AC to 1000V DC).	PCM-4
DC-DC converter	10	Power delivery device (specific PEC)	2	In this SPS, these are DC-DC step-down converters (1000V DC to 800V DC) also known as buck converters.	PCM-1S for starboard side and PCM-1P for port side
DC-AC inverter	2	Power delivery device (specific PEC)	2	These change DC within the zone to AC for the respective load (800V DC to 450V AC).	PCM-2
Propulsion motor	2	Load	3	Could be AC or DC motor. One each on starboard and port side abbreviated with suffix S and P respectively.	PM-S for starboard side and PM-P for port side
Radar	1	Load	3	Standard radar	RAD
Pulsed power load	1	Load	3	Could be a rail-gun for example. These loads consume power in order of MW over very short time intervals causing “spikes” in their power consumption profile.	PL
Energy storage	1	Secondary power source	4	Could be flywheels, or a series of batteries.	ES
DC lumped loads	5	Load	3	These constitute the DC service loads and are simulated as a single entity which draws DC power.	DCLL
AC lumped loads	2	Load	3	These are the AC loads which like the DC counterparts are modelled as single entities.	ACLL
Power distribution modules	4	Power delivery device (general switchboard)	2	Transfer of power from source to load or PECs or busses. The modules are indicated with suffix P and S for port and starboard side respectively.	PDM-2, PDM-4, PDM-3P and PDM-3S where suffixes P and S stand for port and starboard respectively

Table 5.3: List of devices modelled on the RTDS as part of the notional zonal SPS, refer fig. 5.1 and fig. 5.5.

Device	Abbreviation used	Function(s)
Main turbine generator	MTG-1 and MTG-2	• Provide continuous power at the specified rating
Auxiliary turbine generator	ATG-1 and ATG-2	• In case main generators fail, then to provide continuous power at specified rating • Provide continuous power in case general power demand increases
AC-DC rectifier	PCM-4	• Convert AC power from generator side input to DC power at output fed into the DC bus at specified rating
DC-DC step-down converter	PCM-1S and PCM-1P	• Convert DC power from bus at input to lower DC power at specified values • Provide rated DC power in a continuous manner to zonal loads
DC-AC inverter	PCM-2	• Invert DC to AC at required rating • Supply continuous power to AC loads
Propulsion motor	PM-S and PM-P	• Propel the vessel at required speed and in the required direction as needed
Radar	RAD	• To perform tasks related to navigation and tracking
Pulsed power load	PL	• To provide high power weapons capability under special circumstances and mission-modes
Energy storage	ES	• To act as back-up for providing additional power.
DC lumped loads	DCLL	• General ship loads.
AC lumped loads	ACLL	• General ship loads.
Power distribution modules	PDM-2, PDM-4, PDM-3P and PDM-3S	• These modules comprise of switchboards to transfer power from sources to vital loads such as motors, radar etc.

Table 5.4: List of devices with abbreviations used and corresponding functions refer fig. 5.1 and fig. 5.5.

Sub-section	Function(s)	Relevant information	Constituent devices
Zone 1	To provide continuous power to PM-P	• One conversion (AC-DC) through PCM-4 • Major power source i.e. MTG-1 • Pulsed load draws high power and may cause power quality issues and possibility of fluctuations • One of the two propulsion motors (PM-P) present in this zone could add to power quality issues (harmonics) owing to their non-linear power requirement	• PCM-4 • PDM-2 • MTG-1 • PL • PM-P
Zone 2	To provide continuous power to RAD and PM-S	• Once AC-DC conversion in PCM4 • Two power sources with one major and one auxiliary • Two distribution switchboards provide redundant paths • High power radar operation means added power is needed in this zone maintaining acceptable power quality • Similar to zone 1, propulsion motor (PM-S) present in this zone could add to power quality issues (harmonics) owing to the non-linear power requirement	• ATG-1 • PDM-3P • PDM-3S • MTG-2 • RAD • PCM-4 • PM-S
Zone 3	To fulfil criteria of energy storage and deliver the stored energy as and when needed.	• Single (AC-DC) conversion through PCM-4 • Auxiliary generator provides back up through PDM-4 connections • Energy storage capability realised through systems such as a series of batteries or flywheels	• PDM-4 • PCM-4 • ATG-2 • ES
Zone 4,5 & 6	To provide continuous power to DCLL.	• One conversion (dc-dc) on either bus to feed DC load	• PCM-1S • PCM-1P • DCLL
Zone 7 & 8	To provide continuous power to DCLL and ACLL.	• Total two conversions, PCM-1 (dc-dc step down) conversion followed by PCM-2 (dc-ac) conversion • Multiple conversions could cause harmonics and power quality issues within zones in the power supplied to both DC and AC loads	• PCM-1S • PCM-1P • DCLL • PCM-2 • ACLL
AC power ring section	To provide continuous power to other zones.	• Interconnected power sources through distribution switchboards • Back-up power generators also connected through same ring	• All four PDM (PDM-2, PDM-3P, PDM-3S and PDM-4) • MTG-1 and MTG-2 • ATG-1 and ATG-2
DC busses section	To deliver continuous power to entire DC network.	• PCM-4 converts AC to DC from power sources and feeds it to port and starboard busses • Each bus is connected to every PCM-4 to ensure alternate paths • The 1000V DC bus (both starboard and port) supplies the PCM-1 which in turn supply power to each zone providing 2 paths for power delivery	• All three PCM-4 • All five PCM-1S • All five PCM-1P

Table 5.5: List of sub-sections of the modelled SPS with constituent devices, refer fig. 5.1 and fig. 5.5.

5.2.2 F-FMEA at subsystem (zone) level

Here, an F-FMEA is conducted for the SPS at the sub-system or zonal level. The reference diagram is shown in fig. 5.3 and the simplified line diagram is shown in fig. 5.5. The system is segregated into zones and its constituents. The format is tabular, and the contents of the tables are a combination of the standard FMEA tables shown in table 5.1 and 5.2.

5.2.2.1 Zone 1 F-FMEA

The line diagram for zone 1 is shown in fig. 5.6 with its F-FMEA in table 5.6.

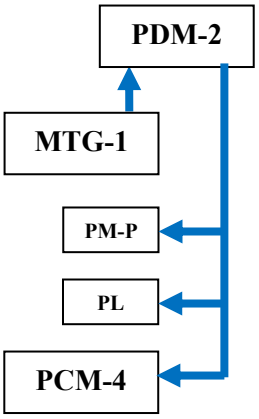


Figure 5.6: Zone 1-line diagram

Name of sub-section: Zone 1			**Diagram :** Shown in fig. 5.4	
Function: To provide required power to PM-S and PL and provide rated input to PCM-4				
No.	**Constituent devices (abbreviations)**		**Type**	
1	MTG-1		Primary power source	
2	PDM-2		Power delivery device (general switchboard)	
3	PM-P		Load	
4	PL		Load	
5	PCM-4		Power delivery device (specific PEC)	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Inability to provide input power to PM-P as desired.	-Inability of MTG-1 to produce desired output as result of a fault/failure. -Inability of PDM-2 to transfer power as a result of a fault/failure. -Internal component level fault/failure in motor.	Directly affects propulsion and potentially hampers achieving specific mission goal(s).	High – In general, an obstacle to achieve the mission goal is a very severe disturbance. Further, if a primary power source has a fault, the remedial action should be a priority irrespective of the presence of redundant sources or back-ups.
2	Inability to provide input power to PL as desired.	-Inability of MTG-1 to produce desired output as result of a fault/failure. -Inability of PDM-2 to transfer power as a result of a fault/failure. -Internal component level fault/failure in the pulsed power load.	Affects ability to use the high power pulsed load leading to potentially jeopardising mission goal(s).	High – Same reasoning as above.
3	Inability to provide required input current and voltage to PCM-4.	-Inability of MTG-1 to produce desired output as result of a fault/failure. -Inability of PDM-2 to transfer power as a result of a fault/failure. -Internal component level fault/failure in the PEC.	Affects output power supplied into the DC bus from PCM-4.	Medium – As there are other 2 PCM-4 devices that offer redundancy this failure mode is less severe than others for this zone.

Table 5.6: Zone 1 F-FMEA details

5.2.2.2 Zone 2 F-FMEA

The line diagram for zone 2 is shown in fig. 5.7. with its F-FMEA in table 5.7.

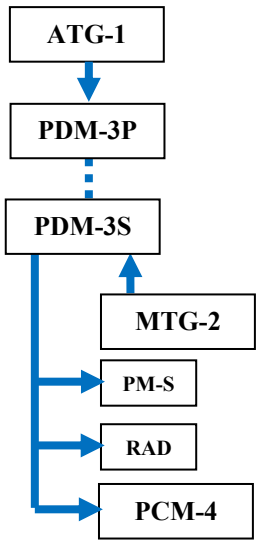


Figure 5.7: Zone 2-line diagram

Name of sub-section: Zone 2			**Diagram :** Shown in fig. 5.5	
Function: To provide required power to PM-S and RAD and provide rated input to PCM-4				
No.	**Constituent devices (abbreviations)**		**Type**	
1	MTG-2		Primary power source	
2	ATG-1		Primary power source	
3	PDM-3P		Power delivery device (general switchboard)	
4	PDM-3S		Power delivery device (general switchboard)	
5	PM-S		Load	
6	RAD		Load	
7	PCM-4		Power delivery device (specific PEC)	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Inability to provide input power to PM-S as desired.	-Inability of MTG-2 (or ATG-1 in case back-up generator is used) to produce desired output as result of a fault/failure. -Inability of PDM-3P or PDM-3S to transfer power as a result of a fault/failure. -Internal component level fault/failure in the motor	Directly affects propulsion and hampers achieving specific mission goal(s).	High – In general, an obstacle to achieve the mission goal is a very severe disturbance. Further, if a primary power source has a fault, the remedial action should be a priority irrespective of the presence of redundant sources or back-ups.
2	Inability to provide input power to RAD as desired.	-Inability of MTG-2 (or ATG-1 in case back-up generator is used) to produce desired output as result of a fault/failure. -Inability of PDM-3P or PDM-3S to transfer power as a result of a fault/failure. -Internal component level fault/failure in the radar	Affects ability to use the radar leading to potentially jeopardising mission goals in general.	High – Same reasoning as above.
3	Inability to provide required input current and voltage to PCM-4.	-Inability of MTG-2 (or ATG-1 in case back-up generator is used) to produce desired output as result of a fault/failure. -Inability of PDM-3P or PDM-3S to transfer power as a result of a fault/failure. -Internal component level fault/failure in the PEC.	Affects output power supplied into the DC bus from the PCM-4.	Medium – As there are other 2 PCM-4 devices that offer redundancy this failure mode is less severe than others for this zone.

Table 5.7 Zone 2 F-FMEA details

5.2.2.3 Zone 3 F-FMEA

The line diagram for zone 3 is shown in fig. 5.8. with its F-FMEA in table 5.8.

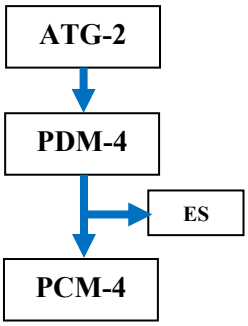


Figure 5.8 Zone 3-line diagram

Name of sub-section: Zone 2			**Diagram :** Shown in fig. 5.6	
Function: To provide required power to ES for desirable charging and rated input to PCM-4via PDM-4 and/or directly through ATG-2 if necessary				
No.	**Constituent devices (abbreviations)**		**Type**	
1	ATG-2		Primary power source	
2	PDM-4		Power delivery device (general switchboard)	
3	ES		Load and secondary power source	
4	PCM-4 (back up PEC device)		Power delivery device (specific PEC)	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Inability to provide required power to ES for charging.	-Inability ATG-2 (in case back-up generator is used) to produce desired output as result of a fault/failure. -Inability of PDM-4 to transfer power as a result of a fault/failure. -Internal component level fault/failure in the storage module.	Affects the energy storage module directly.	Low – It is anticipated that the ES is used relatively lesser than generator back-ups. Further, the only major problem area is a fault in the PDM-4, but alternate current paths exist as seen in fig.5.2 and 5.3 indicating that this disturbance is not very severe.
2	Inability to provide required input current and voltage to PCM-4.	-Inability of MTG-2 (or ATG-1 in case back-up generator is used) to produce desired output as result of a fault/failure. -Inability of PDM-3P or PDM-3S to transfer power as a result of a fault/failure. -Internal component level fault/failure in the PEC.	Affects output power supplied into the DC bus from the PCM-4 when in use as a back-up PEC.	Medium – As there are other 2 PCM-4 devices that offer redundancy this failure mode is less severe than others for this zone.

Table 5.8: Zone 3 F-FMEA details

5.2.2.4 Zone 4, 5 and 6 F-FMEA

Zones 4, 5 and 6 are identical in their arrangement and devices as shown by the line diagram in fig. 5.9. Table 5.9 is the corresponding F-FMEA.

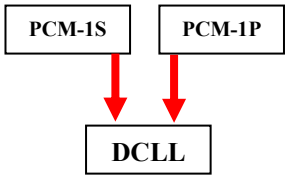


Figure 5.9: Zone 4, 5 and 6-line diagram

Name of sub-section: Zone 4,5 and 6			**Diagram :** Shown in fig. 5.7	
Function: To provide required power for desirable operation of DCLL				
No.	**Constituent devices (abbreviations)**		**Type**	
1	PCM-1S		Power delivery device (specific PEC)	
2	PCM-1P		Power delivery device (specific PEC)	
3	DCLL		Load	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Faulty/inadequate power input to DCLL.	-Faulty power output from at least one PCM-1. -Power quality issues in DC busses. -Internal fault with distribution switchboard(s). -Faulty power output from PCM-4 devices. -Faulty power output from primary power source(s). -Internal fault in DCLL.	Cannot operate DCLL as desired and may affect achieving mission objective.	High – Depending on every mission, the priority of loads may vary, making it vital to be able to operate the DCLLs which are needed at the time. Further, faults in the PEC (in this case PCM-1) of zones may cause disturbances in the DC bus leading to issues for other zones owing to factors such as switching harmonics.
2	No power input to DCLL	-No power output from at least one PCM-1. -No power flow in DC busses. -Internal fault with distribution switchboard(s). -No power output from PCM-4 devices. -No power output from primary power source(s). -Internal fault/failure in DCLL.	Possible system-wide power outage and inability to operate DCLL in turn hampering mission goal(s).	High – This failure mode may point towards system-wide disturbances apart from the obvious hindrance in achieving the mission goal in case a particular DCLL is off-line.

Table 5.9: Zone 4, 5 and 6 F-FMEA details

5.2.2.5 Zone 7 and 8 F-FMEA

Zones 7 and 8 are similar in their constituents and the line diagram is shown in fig. 5.10. Table 5.10 shows the F-FMEA for these zones.

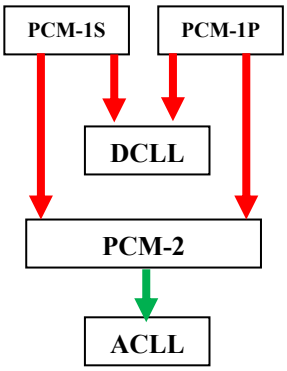


Figure 5.10: Zone 7 and 8-line diagram

Name of sub-section: Zone 7 and 8			**Diagram :** Shown in fig. 5.8	
Function: To provide required current and voltage for desirable operation of DCLL and at input to PCM-2 for providing rated power to ACLL to ensure desirable operation				
No.	**Constituent devices (abbreviations)**		**Type**	
1	PCM-1S		Power delivery device (specific PEC)	
2	PCM-1P		Power delivery device (specific PEC)	
3	DCLL		Load	
4	PCM-2		Power delivery device (specific PEC)	
5	ACLL		Load	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Faulty/inadequate power input to DCLL.	-Faulty power output from at least one PCM-1. -Power quality issues in DC busses. -Internal fault with distribution switchboard(s). -Faulty power output from PCM-4 devices. -Faulty power output from primary power source(s). -Internal fault in DCLL.	Cannot operate DCLL as desired and may affect achieving mission objective.	High – Depending on every mission, the priority of loads may vary, making it vital to be able to operate the DCLLs which are needed at the time. Further, faults in the PEC (in this case PCM-1) of zones may cause disturbances in the DC bus leading to issues for other zones owing to factors such as switching harmonics and current surges.
2	No power input to DCLL	-No power output from at least one PCM-1. -No power flow in DC busses. -Internal fault with distribution switchboard(s). -No power output from PCM-4 devices. -No power output from primary power source(s). -Internal fault/failure in DCLL.	Possible system-wide power outage and inability to operate DCLL in turn hampering mission goal(s).	High – This failure mode may point towards system-wide disturbances apart from the obvious hindrance in achieving the mission goal in case a particular DCLL is off-line.
3	Faulty/inadequate power input to ACLL.	-Faulty power output from at least one PCM-1. -Power quality issues in DC busses. -Internal fault with distribution switchboard(s). -Faulty power output from PCM-4 devices. -Faulty power output from primary power source(s). -Fault power output from PCM-2. -Internal fault in ACLL.	Cannot operate ACLL and may affect achieving mission objective.	High – Similar reasoning to case-1. Further, faults in the PEC (in this case PCM-2) of zones may cause disturbances within its zone (propagation of fault to busses and in turn other zones is evaded owing to isolation provided by the DC-DC PCM-1) owing to factors such as switching harmonics because of the added DC-AC inversion.
4	No power input to ACLL	-No power output from at least one PCM-1. -No power flow in DC busses. -Internal fault with distribution switchboard(s). -No power output from PCM-4 devices. -No power output from primary power source(s). -No power output from PCM-2. -Internal fault/failure in ACLL.	Cannot operate ACLL and very likely that entire zone is without power.	High – Similar reasoning to case-2 with respect to inability of being able to operate ACLL for a particular mission.

Table 5.10: Zone 7 and 8 F-FMEA details

5.2.2.6 AC ring F-FMEA

The AC power generation ring is shown in fig. 5.11. This sub-section is vital because it consists of all the primary power sources of the zonal SPS. Table 5.11 lists the various constituents of the AC power ring with functional failure modes.

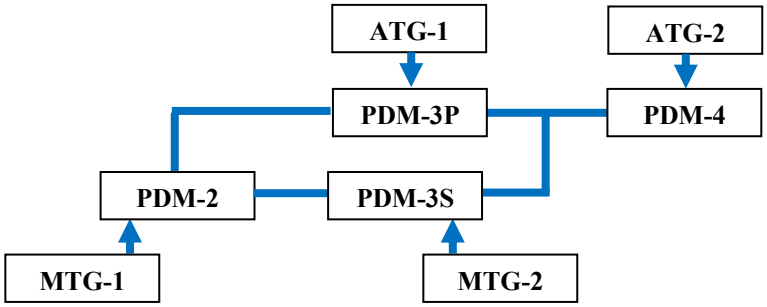


Figure 5.11: AC power generation ring line diagram

Name of sub-section: AC power generation ring			**Diagram :** Shown in fig. 5.9	
Function: To provide continuous power as per requirement during missions to aid in achieving the objective				
No.	**Constituent devices (abbreviations)**		**Type**	
1	MTG-1		Primary power source	
2	MTG-2		Primary power source	
3	ATG-1		Primary power source	
4	ATG-2		Primary power source	
5	PDM-2		Power delivery device (general switchboard)	
6	PDM-4		Power delivery device (general switchboard)	
7	PDM-3S		Power delivery device (general switchboard)	
8	PDM-3P		Power delivery device (general switchboard)	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No power output	-Fault/failure in at least one or more of primary power sources. - Fault/failure in at least one or more switchboard	Loss of power leading to system wide outage in the worst case.	High – Major issue in case of power outage which would need immediate remedial action.
2	Inadequate/faulty power output.	-Fault/failure in at least one or more of primary power sources. - Fault/failure in at least one or more switchboard	Poor quality power input to DC bus and subsequently in zones.	High – Major issue even though power input is non-zero, quality of input is needed to be acceptable.

Table 5.11: AC-power generation ring F-FMEA details

5.2.2.7 DC busses F-FMEA

There are mainly two DC busses, starboard and port. The concise and general representation of the DC busses is shown in fig. 5.12.

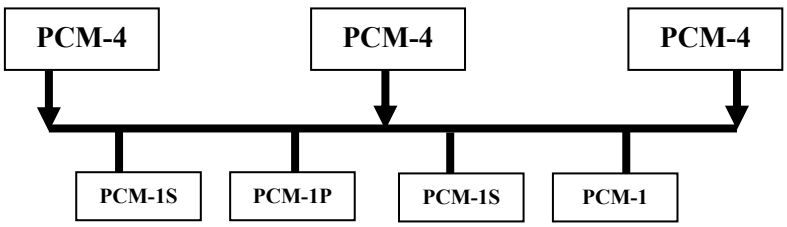


Figure 5.12: DC busses sub-section

Table 5.12 elaborates the F-FMEA for the DC busses sub-section. This sub-section is the novel part in the SPS architecture.

Name of sub-section: DC busses from output of PCM-4 to output of PCM-1		**Diagram :** Shown in fig.5.10		
Function: To provide DC power from AC input into DC-busses and further convert it to stepped down DC power to supply each zone				
No.	**Constituent devices (abbreviations)**		**Type**	
1	PCM-4 (3 in total)		Power delivery device (specific PEC)	
2	PCM-1 (10 in total)		Power delivery device (specific PEC)	
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No power input to port and/or starboard bus	- Failure in all PCM-4 devices. - Power outage due to failure in primary power sources. - No power transfer due to internal failure in switchboards.	No power conversion to required current and voltage and hence potentially may affect achieving mission goal(s)	High – DC busses being charged with required rated power is a vital necessity to realise benefits of the zonal SPS. Further, anything that could provide hindrance in achieving mission goal(s) is a serious problem requiring immediate attention.
2	Fault/inadequate power input to port and/or starboard bus	- Fault in at least one and/or more of the three PCM-4 devices. - Faulty/inadequate power input due to fault in primary power sources. - Fault in switchboards.	Inadequate power conversion that may affect achieving mission goal(s)	High – Similar reasoning to case 1.
3	No power input to zones.	- Failure in both PCM-1 due to internal component issues. - No power flow in DC busses due to failure. - No power output from any of PCM-4. - No power output from AC ring owing to failure in power source(s). - No power transfer from switchboards due to internal component failure.	No power conversion to required current and voltage as input to zones and subsequent loads and hence potentially may affect achieving mission goal(s)	High – No power to zones indicates a system-level fault and hence is obviously a matter of concern.
4	Faulty/undesirable power input to zones.	- Internal fault(s) in either or both PCM-1. - Faulty output from DC busses due to cabling issues. - Undesirable output from at least one PCM-4 because of internal fault. - Undesirable output from power generation ring due to internal fault (s) in primary power source(s). - Undesirable power transfer from switchboards due to internal fault(s).	-Momentary voltage and current fluctuation in case of PEC related issue until back-up device replaces it. - Inadequate power conversion as input to zones that may affect achieving mission goal(s)	High – Even though a faulty output from a PEC device could be accommodate owing to back-up converters, the issue needs attention from the point of view of fault propagation and harmonics potentially linked to faults.

Table 5.12: DC-busses F-FMEA details

5.2.3 F-FMEA at device level

5.2.3.1 Power delivery device (general switchboard) F-FMEA

Switchboards route power from the sources to other parts of the system. F-FMEA for these devices is shown in table 5.13 to table 5.16.

Name of device: PDM-2				
Direct connections: PDM-3P, PDM-3S, MTG-1, PM-P, PL and PCM-4				
Function: Distribute input power from main and/or auxiliary generators to other vital loads, switchboards and PCM-4 which then is distributed through the DC busses to PCM-1 devices into respective zones.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-No input due to MTG/ATG fault/damage. -Internal fault/damage.	- No power input to PL causing inability to use it. - No power input to PM-P. - No power input to PCM-4 and hence no output to DC bus from the particular PEC. - Possible momentary voltage dip until alternative power transfer path is connected via other PDM switchboards. - Possible current fluctuations. - MTG-1 power unavailable to AC ring.	High – The effects tend to hamper specific mission objectives in case special loads such as PL and PM-P need to be used. Also, a primary power source is disconnected from the network.
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s). -Internal fault/failure/damage.	- Insufficient power quality input to PM-P, PCM-4 and PL. - Possible voltage dip and current fluctuations. - MTG-1 power available to AC ring at degraded quality.	High – Similar reasoning to above even though power transfer is not totally zero.

Table 5.13: PDM-2 F-FMEA details

Name of device: PDM-4				
Direct connections: ATG-2, PDM-3S, PDM-3P, ES and PCM-4				
Function: Distribute input power from main and/or auxiliary generators to storage modules, switchboards and PCM-4 which then is distributed through the DC busses to PCM-1 devices into respective zones.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-No input due to primary power source fault/damage. -Internal fault/damage.	- No power input to ES and inability to charge the device. - No power input to PCM-4 and hence no output to DC bus from the particular PEC. - Possible momentary voltage dip until alternative power transfer path is connected via other PDM switchboards. - Possible current fluctuations - ATG-2 power unavailable to AC ring.	Medium – There is redundancy and alternative paths to provide power to DC bus in case PCM-4 receives no input.
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s) . -Internal fault/failure/damage.	- Insufficient power quality input to ES causing irregular charging. - Possible voltage dip and current fluctuations. - ATG-2 power available to AC ring at degraded quality.	Medium – Similar reasoning to above even though power transfer is not totally zero.

Table 5.14: PDM-4 F-FMEA details

Name of device: PDM-3P				
Direct connections: PDM-2, PDM-4, PDM-3S and ATG-1				
Function: Distribute input power from main and/or auxiliary generators to other vital loads and switchboards.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-No input due to MTG/ATG fault/damage. -Internal fault/damage.	- Possible momentary voltage dip and current fluctuations. - ATG-1 power unavailable to AC ring in case of internal fault in generator.	Low – No vital loads or PCM-4 directly connected, hence a relatively low priority disturbance.
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s) . -Internal fault/failure/damage.	-Possible voltage dip and current fluctuations. -ATG-1 power available to AC ring at degraded quality in case of internal fault in generator.	Low – Similar reasoning to above.

Table 5.15: PDM-3P F-FMEA details

Name of device: PDM-3S				
Direct connections: PDM-2, PDM-4, PDM-3P, MTG-2, PM-S, RAD and PCM-4				
Function: Distribute input power from main and/or auxiliary generators to other vital loads, switchboards and PCM-4 which then is distributed through the DC busses to PCM-1 devices into respective zones.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	- No input due to MTG/ATG fault/damage. - Internal fault/damage.	- No power input to RAD causing inability to operate it. - No power input to PCM-4 and hence no output to DC bus from the particular PEC. - No power input to PM-S. - Possible momentary voltage dip and current fluctuations. - MTG-2 power unavailable to AC ring in case of internal fault in generator	High – The effects tend to hamper specific mission objectives in case special loads such as RAD and PM-S need to be used. Also, a primary power source is disconnected from the network.
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s) -Internal fault/failure/damage	- Insufficient power quality input to PM-S, PCM-4 and RAD. - Possible voltage dip and current fluctuations. - MTG-2 power available to AC ring at degraded quality	High – Similar reasoning to above even though power transfer is not totally zero.

Table 5.16: PDM-3S F-FMEA details

5.2.3.2 Power delivery device (specific PEC) F-FMEA

The zonal topology has PEC devices that convert power at various levels. The corresponding F-FMEA is shown in table 5.17 to table 5.22.

Name of device: PCM-4 in zone 1				
Direct connections: PDM-2,PM-S, RAD and all PCM-1P, PCM-1S via DC busses				
Function: To convert AC power input from switchboard to required DC specifications to be supplied to port and starboard DC busses.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	- No input due to MTG/ATG fault/damage. - No input due to switchboard fault/damage. - Internal fault/damage.	- Momentary input power fluctuation for DC busses.	Medium – DC busses are supplied by three identical PCM-4 devices giving redundancy and alternative power inputs in case one of them fails. A matter of concern only would be when the cause of failure is traced to problems in the primary power source(s) or switchboard(s).
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Internal fault/failure/damage	- Power quality issues in DC bus. - Could cause added problems due to harmonics.	Medium – This failure mode indicates that the chances of the power source(s) or switchboard(s) having problems is lesser than the above case and as such alternate power paths and redundant devices would be anticipated to fulfil the power demand. However, the issue related to harmonics needs to be assessed.

Table 5.17: PCM-4 in zone 1 F-FMEA details

Name of device: PCM-4 in zone 2				
Direct connections: PDM-3S,PM-S, RAD and all PCM-1P, PCM-1S via DC busses				
Function: To convert AC power input from switchboard to required DC specifications to be supplied to port and starboard DC busses.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	- No input due to MTG/ATG fault/damage. - No input due to switchboard fault/damage. - Internal fault/damage.	- Momentary input power fluctuation for DC busses.	Medium – DC busses are supplied by three identical PCM-4 devices giving redundancy and alternative power inputs in case one of them fails. A matter of concern only would be when the cause of failure is traced to problems in the primary power source(s) or switchboard(s).
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Internal fault/failure/damage	- Power quality issues in DC bus. - Could cause added problems due to harmonics.	Medium – This failure mode indicates that the chances of the power source(s) or switchboard(s) having problems is lesser than the above case and as such alternate power paths and redundant devices would be anticipated to fulfil the power demand. However, the issue related to harmonics needs to be assessed.

Table 5.18: PCM-4 in zone 2 F-FMEA details

Name of device: PCM-4 in zone 3 (back-up)				
Direct connections: PDM-4,ES and all PCM-1P, PCM-1S via DC busses				
Function: To convert AC power input from switchboard to required DC specifications to be supplied to port and starboard DC busses when needed.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	- No input due to MTG/ATG fault/damage. - No input due to switchboard fault/damage. - Internal fault/damage.	-Momentary input power fluctuation for DC busses.	Low – The reasoning is identical to other PCM-4, but the failure is lower in severity because this PEC is generally for back-up.
2	Faulty output	-Insufficient power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Internal fault/failure/damage	- Power quality issues in DC bus. - Could cause added problems due to harmonics.	Low – Similar reasoning to above.

Table 5.19: PCM-4 in zone 3 F-FMEA details

Name of device: PCM-1S and PCM-1P in zones 4, 5 and 6				
Direct connections: all PCM-4 via DC busses and DCLL				
Function: To convert DC power input from DC busses to required specifications to be supplied to zonal loads.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output from at least one PCM-1	- No input in corresponding DC bus due to fault/damage in power source(s) and/or distribution switchboard(s). - No power flow in corresponding DC bus due to fault/damage to cabling. - No power input in due to fault/damage in all PCM-4. - Internal fault/damage.	- Momentary output power fluctuation to DCLL until opposite side converter supplies load completely. - Inability to operate DCLL as desired.	High – No output from either PCM-1 owing to no power flow in corresponding DC-bus (assuming bus is non-faulty) is a matter of concern given the adequate redundancy and alternate power flow paths. Thus, even though the failure is local (at device level), the supervising system must assess condition of power source(s), distribution switchboard(s), all PCM-4 and busses to ensure major equipment is working within parameters before considering a fault within the respective PCM-1.
2	Faulty output from at least one PCM-1	-Inadequate power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Issue with corresponding DC bus cabling. -Internal fault/failure/damage	-Power quality issues in DC bus. -Could cause added problems due to harmonic magnified by fluctuations. - Inability to operate DCLL as desired.	High – This failure mode indicates that the chances of the power source(s) or switchboard(s) having problems is lesser than the above case and as such alternate power paths and redundant devices would be anticipated to fulfil the power demand. However, the issue related to harmonics needs to be assessed. Further, as stated above, even though this disturbance is at the device level, it does not rule out problems with other major devices.
3	No output from both PCM-1	- No input in both DC busses due to MTG/ATG fault/damage. - No input in both DC busses due to switchboard fault/damage. - No power flow through DC busses due to fault/damage with the cabling. - No power input in due to fault/damage in all PCM-4 -Internal fault/damage.	- No power to zones and inability to operate DCLL which may cause hindrance in achieving mission objective(s).	High – This is a severe problem that could be traced to power source(s), switchboard(s), PCM-4 or the DC busses apart from the PCM-1 themselves having an internal failure. In any case, this failure mode affects the chances of achieving specific mission objectives owing to inability of using zonal loads.
4	Faulty output from both PCM-1	-Inadequate power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Issue with all of DC bus cabling. -Internal fault/failure/damage	-Inadequate power quality input to DCLL and potential inability to operate it affecting mission aim(s).	High – Similar reasoning as case 3 and 4.

Table 5.20: PCM-1P and PCM-1S in zones 4, 5 and 6 F-FMEA details

Name of device: PCM-1S and PCM-1P in zones 7 and 8				
Direct connections: all PCM-4 via DC busses, DCLL, PCM-2 and ACLL				
Function: To convert DC power input from DC busses to required specifications to be supplied to zonal loads.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output from at least one PCM-1	- No input in corresponding DC bus due to fault/damage in power source(s) and/or distribution switchboard(s). - No power flow in corresponding DC bus due to fault/damage to cabling. - No power input in due to fault/damage in all PCM-4. - Internal fault/damage.	- Momentary output power fluctuation to DCLL until opposite side converter supplies load completely. - Inability to operate DCLL as desired. - Momentary input fluctuation to PCM-2 and ACLL. -Possible problems to operate ACLL.	High – Similar reasoning to table 5.20 case-1. Further, owing to the added presence of PCM-2, any fluctuations could add to the effect of harmonics.
2	Faulty output from at least one PCM-1	-Inadequate power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Issue with corresponding DC bus cabling. -Internal fault/failure/damage	-Power quality issues in DC bus. -Could cause added problems due to harmonics magnified by fluctuations. - Inability to operate DCLL as desired. - Inadequate input to PCM-2 and in turn to ACLL. - Inability to operate ACLL as desired.	High – Similar reasoning to table 5.20 case-2 and issue of harmonics due to added conversion.
3	No output from both PCM-1	- No input in both DC busses due to MTG/ATG fault/damage. - No input in both DC busses due to switchboard fault/damage. - No power flow through DC busses due to fault/damage with the cabling. - No power input in due to fault/damage in all PCM-4 -Internal fault/damage.	- No power to zones and inability to operate DCLL which may cause hindrance in achieving mission objective(s). - No power input to PCM-2 and ACLL which may cause hindrance in achieving mission objective(s).	High – Similar reasoning to table 5.20 case-3.
4	Faulty output from both PCM-1	-Inadequate power quality input as a result of fault/failure/damage to primary power source(s) and/or switchboard(s). -Issue with all of DC bus cabling. -Internal fault/failure/damage	-Inadequate power quality input to DCLL and potential inability to operate it affecting mission aim(s). - Inadequate power quality input to PCM-2 and ACLL which may cause hindrance in achieving mission objective(s).	High – Similar reasoning as table 5.20 case-4.

Table 5.21: PCM-1P and PCM-1S in zones 7 and 8 F-FMEA details

Name of device: PCM-2 in zones 7 and 8				
Direct connections: PCM-1P and PCM-1S and ACLL				
Function: To convert DC power input from PCM-1 devices to required AC specifications to be supplied to zonal AC loads.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	- No input from PCM-1 devices due to internal fault/damage. - No power flow from DC busses due to cabling fault/damage. - No power transfer from distribution switchboards due to fault/damage. - No power output from primary source(s) due to fault/damage. - Internal fault/damage.	- Inability to operate ACLL causing potential hindrance in achieving mission aim(s).	High – Even though the fault is local, a check needs to be done on other devices.
2	Faulty output.	-Inadequate power quality input to ACLL and possible inability to operate it as desired. - Problems with PCM-1 and/or DC busses and/or switchboard(s) and/or power source(s). -Internal fault/failure/damage	- Inadequate input to PCM-2 and in turn to ACLL. - Inability to operate ACLL as desired causing potential hindrance to achieving mission aim(s).	Medium – Similar reasoning to above, though a non-zero power flow indicates that the problem is of slightly reduced severity.

Table 5.22: PCM-2 in zones 7 and 8 F-FMEA details

5.2.3.3 Primary power source F-FMEA

Turbine generators are the primary power sources of the zonal SPS. Their F-FMEA is presented in table 5.23 to table 5.26.

Name of device: MTG-1				
Direct connections: PDM-2				
Function: To produce rated power output and supply the connected distribution module in order to deliver the power to the SPS network.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-Internal fault/damage.	- MTG-1 power unavailable to AC ring. -Voltage and current fluctuation in SPS network until back-up generators are brought on-line.	High – Any fault to primary power source can be considered a top priority issue.
2	Faulty output	-Internal fault/failure/damage.	- Insufficient power quality input to SPS network. - Possible voltage dip and current fluctuations until issue resolved. - MTG-1 power available to AC ring at degraded quality.	High – Similar reasoning to above even though power transfer is not totally zero.

Table 5.23: MTG-1 F-FMEA details

Name of device: MTG-2				
Direct connections: PDM-3S				
Function: To produce rated power output and supply the connected distribution module in order to deliver the power to the SPS network.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-Internal fault/damage.	- MTG-2 power unavailable to AC ring. -Voltage and current fluctuation in SPS network until back-up generators are brought on-line.	High – Any fault to primary power source can be considered a top priority issue.
2	Faulty output	-Internal fault/failure/damage.	- Insufficient power quality input to SPS network. - Possible voltage dip and current fluctuations until issue resolved. - MTG-2 power available to AC ring at degraded quality.	High – Similar reasoning to above even though power transfer is not totally zero.

Table 5.24: MTG-2 F-FMEA details

Name of device: ATG-1				
Direct connections: PDM-3P				
Function: To produce rated power output when used as back-up and supply the connected distribution module in order to deliver the power to the SPS network.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-Internal fault/damage.	- ATG-1 power unavailable to AC ring. -Voltage and current fluctuation in SPS network until back-up generators are brought on-line.	High – Even though ATG-1 is used as a back-up, fault to primary power source can be considered a top priority issue.
2	Faulty output	-Internal fault/failure/damage.	- Insufficient power quality input to SPS network. - Possible voltage dip and current fluctuations until issue resolved. - ATG-1 power available to AC ring at degraded quality.	Medium – Since ATG-1 is for back-up purposes, a fault in it is relatively less severe as the generator can be taken off-line and the power demand fulfilled potentially by another power source.

Table 5.25: ATG-1 F-FMEA details

Name of device: ATG-2				
Direct connections: PDM-4				
Function: To produce rated power output when used as back-up and supply the connected distribution module in order to deliver the power to the SPS network.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	No output	-Internal fault/damage.	- ATG-2 power unavailable to AC ring. -Voltage and current fluctuation in SPS network until back-up generators are brought on-line.	High – Even though ATG-2 is used as a back-up, fault to primary power source can be considered a top priority issue.
2	Faulty output	-Internal fault/failure/damage.	- Insufficient power quality input to SPS network. - Possible voltage dip and current fluctuations until issue resolved. - ATG-2 power available to AC ring at degraded quality.	Medium – Similar reasoning to table 5.25 case 2.

Table 5.26: ATG-2 F-FMEA details

5.2.3.4 Loads F-FMEA

The various loads mentioned in the line diagram are considered here for F-FMEA shown in table 5.27 to table 5.32.

Name of device: PM-P				
Direct connections: PDM-2				
Function: To propel the vessel as desired for achieving specific mission objective(s).				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). -Internal fault/damage.	-Problem in moving the ship and direct impact on achieving mission objective(s). - Potential issue with operating PL.	High – No power input to a motor which has alternate power input paths and back-up sources is a major failure which needs to be assessed thoroughly. Also, in case the failure cause is due to internal component issues, this is a top priority issue as for any mission in general; the propulsion motor(s) must be available for use.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty output from any of the source(s). -Internal fault/damage.	-Same as above reason, even though motor is not fully stalled. - Possible trouble in operating PL as desired.	High – Similar reasoning to above even though motor is not fully stalled.

Table 5.27: PM-P F-FMEA details

Name of device: PM-S				
Direct connections: PDM-3S				
Function: To propel the vessel as desired for achieving specific mission objective(s).				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). -Internal fault/damage.	-Problem in moving the ship and direct impact on achieving mission objective(s). -Potential issue with operating RAD.	High – No power input to a motor which has alternate power input paths and back-up sources is a major failure which needs to be assessed thoroughly. Also, in case the failure cause is due to internal component issues, this is a top priority issue as for any mission in general; the propulsion motor(s) must be available for use.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty output from any of the source(s). -Internal fault/damage.	-Same as above reason, even though motor is not fully stalled. - Possible trouble in operating RAD as desired.	High – Similar reasoning to above even though motor is not fully stalled.

Table 5.28: PM-S F-FMEA details

Name of device: PL				
Direct connections: PDM-2				
Function: To fulfil operational need as desired for achieving specific mission objective(s).				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). -Internal fault/damage.	-This is a speciality load which is used during specific events and as such the inability to operate it has a direct impact on achieving mission objective(s). - Potential issue with operating PM-P	High – No power input to the PL which has alternate power input paths and back-up sources is a major failure which needs to be assessed thoroughly. Also, in case the failure cause is due to internal component issues, this is a top priority issue as for any mission in general; the propulsion motor(s) must be available for use.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty output from any of the source(s). -Internal fault/damage.	-Same as above reason as achieving the mission objective is top priority. - Possible trouble in operating PM-P as desired.	High – Similar reasoning to above even though the PL could be in partial-operation mode (not completely unusable).

Table 5.29: PL F-FMEA details

Name of device: RAD				
Direct connections: PDM-3S				
Function: To fulfil operational need as desired for achieving specific mission objective(s).				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). -Internal fault/damage.	-This is a speciality load which is used during specific events and as such the inability to operate it has a direct impact on achieving mission objective(s). - Potential issue with operating PM-S.	High – No power input to RAD which has alternate power input paths and back-up sources is a major failure which needs to be assessed thoroughly. Also, in case the failure cause is due to internal component issues, this is a top priority issue as for any mission in general; the propulsion motor(s) must be available for use.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty output from any of the source(s). -Internal fault/damage.	-Same as above reason as achieving the mission objective is top priority. - Possible trouble in operating PM-S as desired.	High – Similar reasoning to above even though the RAD could be in partial-operation mode (not completely unusable).

Table 5.30: RAD F-FMEA details

Name of device: DCLL				
Direct connections: PCM-1S and PCM-1P				
Function: To fulfil operational need as desired for achieving specific mission objective(s).				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). - No power output into DC-busses from any PCM-4. - No power output from either PCM-1. -Internal fault/damage.	-Impact on achieving mission objective(s). - Potentially no power input to connected PCM-4 of zone 4.	High – Based on load priority and the specific mission needs, each load must be available for use and any hindrance for this purpose is a major issue. Also, failure to operate a zonal load such as any DCLL may indicate system-wide issues and hence needs thorough assessment not just limited to corresponding zone.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty power output from any of the source(s). - Faulty power output into DC-busses from any PCM-4. - Faulty power output from either PCM-1. -Internal fault/damage.	-Same as above reason as achieving the mission objective is top priority. - Potential disturbance in normal operation of PCM-4 in zone 4.	High – Similar reasoning to above even though partial operation may be possible at lesser efficiency.

Table 5.31: DCLL F-FMEA details

Name of device: ACLL				
Direct connections: PCM-2				
Function: To fulfil operational need as desired for achieving specific mission objective(s).				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). - No power output into DC-busses from any PCM-4. - No power output from either PCM-1. - No power output from PCM-2. -Internal fault/damage.	-Impact on achieving mission objective(s).	High – Similar reasoning to case-1 in table 5.31.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty power output from any of the source(s). - Faulty power output into DC-busses from any PCM-4. - Faulty power output from either PCM-1. - Faulty power output from PCM-2. -Internal fault/damage.	-Same as above reason as achieving the mission objective is top priority.	High – Similar reasoning to case-2 in table 5.31.

Table 5.32: ACLL F-FMEA details

5.2.3.5 Secondary power source F-FMEA

F-FMEA for a secondary power source such as flywheel, battery, capacitor bank is shown in table 5.33.

Name of device: ES				
Direct connections: PDM-4				
Function: To fulfil operational need as desired as a secondary power source.				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Failure to operate	-No power transfer from distribution switchboard(s). -No power output from any of the source(s). -Internal fault/damage.	-Inability to operate device. - Potential issue with operating PM-P	Medium – More than the inability to use the device, the effort needed would be to monitor whether any PDM or generator has a problem.
2	Faulty operation	-Faulty power transfer from distribution switchboard(s). -Faulty output from any of the source(s). -Internal fault/damage.	-Inability to operate the device as desired, also device may not charge adequately due to bad quality input. - Possible trouble in operating PM-P as desired.	Medium – Similar reasoning to above.

Table 5.33: ES F-FMEA details

5.3 Interpretation of F-FMEA results

The F-FMEA demonstrated previously is spread across the middle and lowest levels of the system i.e. zonal and device levels. A similar analysis could be conducted at the overall system level by knowing beforehand the various typical mission types. In such an analysis, the function of the system is simply to enable fulfilling the mission goal(s) while a failure mode is the inability to do so. This analysis is not shown here because as mentioned before, the notional SPS is still in its conceptual phase without existence of actual benchmark systems. As such no concrete mission types and their constituent objectives have been finalised as yet. Also, a mission specific F-FMEA result could be integrated by combining individual F-FMEAs of the sub-systems and devices that would be used for achieving the desired goal(s).

Earlier, it had been emphasised that an important outcome of FMEA is the identification of pertinent faults and failures. Thinking along similar lines, the F-FMEA which is a relatively superficial analysis is expected to identify critical sub-sections and devices in the network without bothering about internal component issues. In this part of the chapter, an analysis is presented on the various failure

modes that were deemed “high” in the F-FMEA tables. These are the failure modes that further research is focussed upon.

5.3.1 Summary of high-severity functional failure modes

The most pertinent failure modes have been segregated as per sub-system and device type. Table 5.34 lists the number of functional failure modes in total as well as those that are classed under high-severity for sub-systems such as the various zones, AC power generation ring and DC busses. This table also lists the number and type of individual devices that these sub-systems consist of.

Sub-system	Functional failure modes [nf]	High-severity functional failures modes [sf]	sf/nf %	Primary power sources	Secondary power sources	Specific power delivery devices (PEC)	General Power delivery devices	Loads
Zone 1	3	2	66.66	1	0	1	1	2
Zone 2	3	2	66.66	2	0	1	2	2
Zone 3	2	0	0.00	1	1	1	1	0
Zone 4	2	2	100.00	0	0	2	0	1
Zone 5	2	2	100.00	0	0	2	0	1
Zone 6	2	2	100.00	0	0	2	0	1
Zone 7	4	4	100.00	0	0	3	0	2
Zone 8	4	4	100.00	0	0	3	0	2
AC power ring	2	2	100.00	4	0	0	4	0
DC busses	4	4	100.00	0	0	13	0	0
Sum totals	**28**	**24**	85.71					

Table 5.34: Summary of high severity functional failure modes at a sub-system level

Table 5.35 summarises the F-FMEA results at device level. Table 5.36 adds to the detail of table 5.35 by listing out the results for individual devices. This concise view of the F-FMEA at the sub-system and device levels which spanned 28 tables can be assessed using tables 5.34-5.36.

Type of device	Quantity	Functional failure modes [nf]	High-severity functional failures modes [sf]	sf/nf %
Load	11	12	12	100
Primary power source	4	8	6	75
Power delivery device (specific PEC)	15	16	9	56.25
Power delivery device (general switchboard)	4	8	4	50
Secondary power source	1	2	0	0
Sum totals	**35**	**46**	**31**	**67.39**

Table 5.35: Summary of high severity functional failure modes at a device level sorted as per percentage of high severity functional failures

Table 5.35 reveals that the loads need to be available at all times as functional failures in them could all potentially be high-severity ones. This fact is amply reflected in the F-FMEA tables, wherein the functional failure causes can in theory be traced back even to the source apart from devices such as distribution modules and converters in between. In other words, a load which fails to operate, not only could potentially jeopardise the mission, but could be a resultant of a more severe failure to vital devices such as power sources for example. The second most important device-type from the functional-failures point of view is the power sources with 75% of their functional failures classed as highly severe. This is to be expected as all the vessels power is provided by these devices during every mission type and any drop in efficiency could have an overall negative impact.

The power delivery devices (both specific PEC and general switchboards) have a comparable high-severity functional failure rate of around 50%. The energy storage module is probably the least important from a functional failure point of view. Even though there are 56.25% high-severity functional failures for power converter devices (specific PEC), table 5.36 shows a slightly different picture when each type of PEC is considered.

Name of device	Quantity	Functional failure modes [nf]	High-severity functional failures modes [sf]	sf/nf %
PDM-2	1	2	2	100.00
PDM-4	1	2	0	0.00
PDM-3S	1	2	0	0.00
PDM-3P	1	2	2	100.00
PCM-4 of zone 1	1	2	0	0.00
PCM-4 of zone 2	1	2	0	0.00
PCM-4 of zone 3	1	2	0	0.00
PCM-1P and PCM-1S of zones 4, 5 and 6	6	4	4	100.00
PCM-1P and PCM-1S of zones 7 and 8	4	4	4	100.00
PCM-2 of zones 7 and 8	2	2	1	50.00
MTG-1	1	2	2	100.00
MTG-2	1	2	2	100.00
ATG-1	1	2	1	50.00
ATG-2	1	2	1	50.00
PM-P	1	2	2	100.00
PM-S	1	2	2	100.00
PL	1	2	2	100.00
RAD	1	2	2	100.00
DCLL of zones 4-8	5	2	2	100.00
ACLL of zones 7 and 8	2	2	2	100.00
ES	1	2	0	0.00
Sum totals	**35**	**46**	**31**	**67.39**

Table 5.36: Summary of high severity functional failure modes for individual devices

A close look at table 5.36 shows that for a total number of 10 PCM-1 type devices, the 4 types of functional failures considered have a 100% high-severity rate. For the 3 types of PCM-4 devices, neither of the failures can be categorised as high-severity, mainly because these AC-DC rectifiers offer redundancy for the sole objective of supplying the DC-busses. The PCM-2 DC-AC inverters have a 50% high-severity functional failure rate.

This statistic shows that the functional issues with PCM-1 type devices which are DC-DC buck converters supplying each zone in the notional SPS are potentially top priority. Tables 5.9, 5.10, 5.20, 5.21 show the F-FMEA at both zonal and device level for these types of PECs. Fundamental inability of these converters to supply their respective zones could be a cause of a more severe disturbance (towards the power source side) unless the fault is within the converters themselves. Further, an inability of the PCM-1 to supply a zone means a power outage within it, making loads unavailable, and loads are a device established to be most sensitive from a functional failure (with respect to achieving mission goal) point of view (table 5.35). Keeping this logical reasoning in mind, and on the back of results from the F-FMEA, it could be interpreted that besides the power sources, PCM-1 type devices are critical for smooth operation of the zonal SPS and thus need to be monitored to ensure timely fault diagnosis and remedial action.

5.3.2 Discussion and conclusions

F-FMEA was conducted in this chapter, using similar tabular formats shown in [71] and [72]. The overall system was divided into progressively smaller parts for this analysis. This helped study the SPS network understanding the reference zonal topology and connections between devices. Adhering to the definition of functional analysis, the F-FMEA followed a fundamental approach wherein the emphasis was on the ability to fulfil one or more functions at both a zone-level as well as device-level. In such a fundamental analysis, an inability to fulfil the primary function(s) was deemed a functional failure mode.

Even though, F-FMEA does not cater to an in-depth analysis considering extensive underlying physics of processes, it still offers a detailed enough analysis as a first step to study a novel system. The language used to demonstrate the F-FMEA through tables 5.6 to 5.33 is largely similar and may seem repetitive. This is mainly

because of the non-complex nature of considering what defines a function and what could be a failure to hamper the ability to satisfy it in such a functionality based analysis.

Table 5.35 and 5.36 showed concise statistics on F-FMEA results. The reasoning derived from the overall F-FMEA analysis identified PCM-1 type DC-DC buck converters as critical devices. Adding to this interpretation from F-FMEA the issue relating to harmonics [101] and intelligent monitoring [102-105], puts PCM-1 devices into the spotlight for further analysis. Further fault studies need to be conducted in order to understand component level issues for buck converters.

F-FMEA results and logical reasoning has thus enabled to narrow down and focus further research into fault diagnosis, which in this case is selected for the buck converter. The next section shows a hardware-FMEA (H-FMEA) for the buck converter in an attempt to further guide research into diagnosis of pertinent faults.

5.4 H-FMEA for buck converter

This section outlines an H-FMEA for a typical buck converter circuit. It takes into account failure modes of individual components, causes and resultant effects. This section is aimed at indicating the level of details that an H-FMEA brings about as opposed to the more general and basic F-FMEA. The H-FMEA fundamentally is similar to F-FMEA because it considers failure modes to be those which disable the component from working normally (i.e. inability to perform normal function). The H-FMEA however, is far more exhaustive and as a result, a more generic F-FMEA is a handy tool in narrowing down a manageable number of devices on which to conduct a detailed H-FMEA.

Fig.13 shows a standard buck converter circuit diagram. Table 5.37 lists out the components of a typical buck converter with their functions.

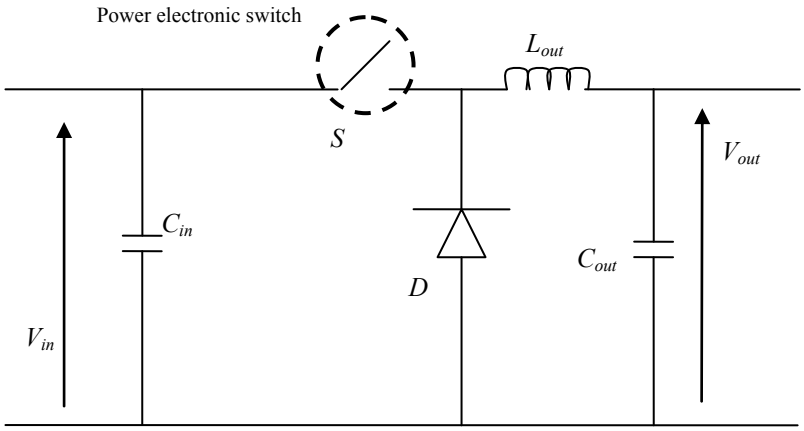


Figure 5.13: A standard dc-dc buck converter circuit

Component	Function(s)
Input side capacitor – C_{in}	• High frequency filtering. • Energy storage at input side.
Power electronic switch – could be • Thyristor • Insulated gate bipolar transistor (IGBT) • Integrated gate commutated thyristor (IGCT) • Gate turn off thyristor (GTO) • Metal oxide semi-conductor field effect transistor (MOSFET) etc.	• Switching action to step down voltage.
Diode – D	• Provide current path during switch's off state.
Inductor – L and Output side capacitor – C_{out}	• Inductor-capacitor (LC) filter to reduce output ripple. • Provide current during switch's off state.

Table 5.37: Standard dc-dc buck converter components and their functions

5.4.1 Existing research on component level fault studies

Throughout this chapter, analysis was conducted that helped progressively narrow down zonal SPS study areas to effectively focus research. At this stage, the dc-dc buck converter has been selected on which to perform further studies with faults and failures being the main theme. As a result, attention now sits firmly upon studying the types of faults and failures that may occur in a standard buck converter circuit owing to component issues.

Researchers in general approached fault studies for PECs to develop fault tolerant circuit topologies as well as protection schemes. Fault analysis of a power converter used to feed an induction motor system is provided by Kastha and Bose in [106].

Here the authors discuss a three phase converter actively operating in a common application of feeding a motor drive. The paper follows a focussed methodology of narrowing down on pertinent failures within the PEC only. A detailed study of a typical setup is conducted and commonly occurring faults are outlined, followed by their simulations. Even though [106] does not directly deal with a dc-dc buck converter, the research approach used is detailed and efficient in order to address pertinent issues and hence the paper is a useful guide.

Letor and Candeloro discuss short circuit behaviour of IGBT in [107]. Fault studies for static and dynamic short circuit stresses are presented and due recommendations made for an appropriate protection circuit. The paper highlights the mechanism of a short circuit failure mode and associated parasitic effects such as *dv/dt* (time rate of change of voltage) which need to be taken into account. Discussion for IGBT short circuit behaviour in event of fault current induced stress is presented in [108] similar to [107]. Here too the authors focus on protection during a short circuit fault. A detailed recommendation list is provided that forms a benchmark to develop fault tolerant systems that can handle short circuits. A detailed explanation of the failure mechanism is also outlined which enhances understanding for such failure modes.

IGBTs are widely used in switching applications and further research on their short-circuit failure modes can be found in [109]. Here like in [107, 108], a detailed explanation of mechanisms of failure are given. The papers [107-109] provide a sufficient understanding of short-circuit behaviour for the semiconductor switch (IGBT) and their dependent causes as well as effects. These papers reflect upon short circuits external to the power electronic converter which imposes stresses on the semiconductor switch owing to high fault currents. However, an important aspect common to the research is the emphasis on performing experiments on test circuits to generate real data.

Rothenhagen and Fuchs discuss the open-circuit failure mode in [46] for inverters connected to AC machines, in this case a permanent magnet synchronous machine. The authors acknowledge the fact that short-circuits are more common, but in rare cases initial open circuit failures can also occur owing to high heat build up. The mechanism for such an open-circuit failure mode for the semiconductor switch is discussed with an evaluation of several diagnosis techniques. A more detailed

evaluation of prevalent diagnosis methods and discussion of failure modes are presented in [47]. This research includes discussion of gate-misfiring faults, which effectively keep the switch in an open or closed state thereby mimicking short or open-circuit failures (but this failure could be intermittent or permanent unlike the open/short-circuit which is only permanent). However, it must be noted that in [46, 47], the PEC system considered is a three-phase converter and not dc-dc system. But nonetheless, this research provides an understanding of failure modes in a semiconductor switch that could fundamentally occur and is used in any type of PEC. Another aspect of note is the mention of IGBT based systems being more common than other types of semiconductor switches.

Similar to [106], an overall exhaustive view of semi-conductor switch faults in a three-phase PEC system is provided by Cardoso et al. in [110]. This research is relatively recent and as such the community has progressed on to multi-level converter topologies that incorporate fault tolerance aspects which were proposed earlier in earlier work [106-109]. In [110], the authors explain various faults that may occur, typically open and short-circuits and gate-misfiring in semiconductor switches. Methods to diagnose such faults are also discussed with simulations being conducted in MATLAB/SIMULINK. Test circuits are used to generate real fault data for verification of simulation studies. A similar analysis for switch open/short-circuit faults is provided in [111, 112], where IGBT is used for switching.

Research presented in [46, 47, 106-112] offer a detailed understanding of possible and known failure modes in semiconductor switches (mostly IGBTs as they are widely used). Authors explain failure mechanisms and associated causes and effects. Known methods to diagnose these types of faults are also evaluated. Further, a detailed methodology comprising simulations as well as the practise of real data generation using actual test-beds helps verify this research.

In [113], the authors analyse a three-level dc-dc converter system. These types of topologies are used in high voltage DC applications. The authors analyse every component (as opposed to previous examples discussing mainly the switch), such as the capacitors and diodes. The failure modes for the constituent components are discussed with their associated effects and possible causes. This paper mainly is aimed at the design of a protection circuit in the event of multiple faults. As seemingly is the norm within this research domain, the research is verified using a

test circuit. This paper offers more information about other components and their respective fault manifestations which would help in the effort to analyse faults in a dc-dc buck converter's components.

Failure modes and analysis for capacitors used in PECs is provided in [114, 115]. These papers provide information on internal and external causes for capacitor failures and make use of well established statistical data to explain rates of wear and ageing. In [60], information about capacitor degradation over time is provided and its link with the effective series resistance. A method is proposed to detect such a failure mode as it gradually happens over time. The same application to determine remaining life of the capacitor (electrolytic) is presented in [116] and is based on a dc-dc buck converter topology which makes it directly relevant to this research. Both the papers [60, 116] provide information on dependent factors that affect the operational life of a capacitor used in a PEC application. Amaral and Cardoso provide information on the mechanism of ageing within electrolytic capacitors and an online method to detect any changes in [117]. All of this information is useful to understand the causes and associated effects related to the various failure modes of capacitor types commonly used in PECs.

The freewheeling diode is relatively the weakest link within the PEC circuit and in [118] the authors explain various causes and associated effects of its failure modes. The paper provides comprehensive coverage of the problems that may arise in a diode while it performs the action of passing current during the semiconductor switch's off state. Further information about this failure mode for the freewheeling diode can be obtained from [119].

Failure modes of inductors, coils and chokes in general are presented in [120]. One can obtain fundamental information related to the function of an inductor in a circuit, its basic design and resulting faults that can occur such as loss of insulation, winding short-circuit and open-circuit leads due to mechanical damage. Further, an exhaustive repository of FMEA for circuit components such as semiconductor switches, diodes, capacitors, inductors etc. can be found in [121]. Denson in [121] provides a detailed analysis of failure mechanisms for types and sub-types of components used commonly in electronic circuits. The report also has information on mathematical failure models which could be used to run computer simulations.

The material researched [46, 47, 106-112] provides a detailed understanding of known failure modes of components used in a typical buck converter. Although most of the papers do not explicitly conduct FMEA for components, they still inform the reader about faults that can commonly occur at a component level and their causes as well as expected effects. Such information is vital if one is to conduct FMEA for a buck converter because component fault related understanding forms the crux of this approach. Based on the listed referenced material, the tables that follow in this section elaborate an H-FMEA for the typical dc-dc buck converter circuit.

5.4.2 H-FMEA in tabular format

Understanding of the dc-dc buck converter operation in general, its function within the zonal SPS and roles of individual components within it helps in its detailed H-FMEA. Research done to study faults and failure modes in other types of PECs give further insight into general causes and effects. The research in the power electronics domain is meticulous once the particular area of study is focused upon and more often than not involves verification using hardware setups. Such an approach is as yet not possible for the SPS arena due to lack of actually built benchmark systems.

As a result, the causes and effects of failure modes of buck converter individual components impacting the zonal SPS need to be theorised and estimations have to be made. These estimates are made using fundamental understanding of electrical/electronic concepts coupled with research presented in other papers demonstrating work in the general power domain. This section shows H-FMEA for individual components of the selected buck converter in a tabular format typically used for FMEAs [71, 72].

Table 5.38 shows H-FMEA for the semiconductor switch of a buck converter. As reported in previous research, the switch could be a GTO, IGBT, MOSFET etc. Typically IGBTs are preferred and relatively more widely used.

Name of component: Semiconductor switch (*S*)				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Short circuit	Overvoltage due to decreased power quality input.	Sudden high current and voltage breakdown causing shutdown of converter. A short circuit fault could induce rupturing of the switch resulting in an eventual open circuit.	High – Results in complete shutdown of converter operation.
2	Open circuit	Thermic cycling, lifting of bond wire causing break in contact, driver failure, rupture of component. [46]	No path for current during switch's turn-off state, causing malfunction.	High – Results in complete shutdown of converter operation.
3	Gate-misfiring	Problem with PWM circuit.	Either the switch is in on state or off state when it is not supposed to be in it leading to malfunction of switching operation.	High – Though converter may not completely shutdown (in case misfiring is intermittent), still this failure mode results in faulty and unwanted output.

Table 5.38: Semiconductor switch FMEA

The two capacitors used in the circuit have fairly similar functions and causes of failure and identical failure modes. However, the effects of failure modes are different. The corresponding analysis is shown in table 5.39 and table 5.40.

Name of component: Input capacitor (C_{in})				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Short circuit	Loss of dielectric medium causing plates to come in contact.	High current surge and voltage dip.	High – Results in complete shutdown of converter operation.
2	Open circuit	Physical damage to capacitor or loss of contact of leads to wires/cables.	Rise in input noise.	Low – Relatively minor fault though the noise increase may need monitoring. Although in high voltage applications the loss of the energy buffer provided by the capacitor may be more problematic.
3	Ageing	Wear and tear as part of usual operation.	Gradual decrease in capacitance due to electrolyte leakage (electrolytic capacitor).	Medium – Slowly progressing failure which needs timely remedial action.

Table 5.39: Input capacitor FMEA

Name of component: Output capacitor (C_{out})				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Short circuit	Loss of dielectric medium causing plates to come in contact.	High current and voltage breakdown.	High – Results in complete shutdown of converter operation.
2	Open circuit	Physical damage to capacitor or loss of contact of leads to wires/cables.	Increase in output voltage ripple causing undesirable operation.	High – Without filtering, the output would have undesirable noise and sub-standard quality.
3	Ageing	Wear and tear as part of usual operation.	Gradual decrease in capacitance and increase in output ripple.	Medium – Though this failure takes several thousand hours to cause a major disturbance, diagnosing it is vital to enable timely remedial action ensuring acceptable quality power output.

Table 5.40: Output capacitor FMEA

The output side inductor forms an important part of the filter circuit as well as helping to limit fault current. The H-FMEA for a general inductor is shown in table 5.41 with respective causes and effects impacting the network.

Name of component: Inductor (L)				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Short circuit	Windings coming into contact.	Reduced filtering at output side.	High – Shutdown of converter operation.
2	Open circuit	Physical damage to component or loss of contact of leads to wires/cables.	No current path causing no output.	High – Shutdown of converter operation.

Table 5.41: Inductor FMEA

The freewheeling diode plays a vital role for reverse recovery current. H-FMEA for it is in table 5.42 and a fault in it could cause converter shutdown.

Name of component: Diode (D)				
No.	**Failure mode**	**Cause**	**Effect**	**Severity and remarks**
1	Short circuit	Voltage transients and/or over-currents, overheat the component that may melt the silicon/germanium.	Sudden high current and voltage breakdown.	High – Results in high current surge and shutdown of converter operation.
2	Open circuit	Less frequent than the above failure mode and is typically caused when the stress from high current/voltage blows off the component resulting in an open section along the wire/cable.	No path for current during switch's off state, causing malfunction.	High – Malfunctions in converter operation.

Table 5.42: Freewheeling diode FMEA

5.4.3 Summary of high-severity failure modes

Table 5.43 shows a concise view of failure mode statistics for the buck converter components. In general, the high severity failures are considered those which cause either a complete shutdown of the normal operation or cause substantial problems at output (e.g. exaggerated ripple).

Name of component	**Quantity**	**Failure modes [nf]**	**High-severity failures modes [sf]**	**sf/nf %**
Semiconductor switch (S)	1	3	3	100.00
Input capacitor (C_{in})	1	3	1	33.33
Diode (D)	1	2	2	100.00
Output capacitor (C_{out})	1	3	2	66.67
Inductor (L)	1	2	2	100.00
Sum totals	**5**	**13**	**10**	**76.92**

Table 5.43: Summary of high severity failure modes for individual components of a buck converter

5.4.4 Discussion

In general, the switch failure modes cause most concern and need to be addressed. The diode is also a vital component whose failure can lead to shutdown. The typical failure mode for capacitors and inductors are gradual and occur over time due to wear and leakage. The next step in this research is to perform fault studies to gain a better understanding of circuit behaviour. These studies could be conducted using MATLAB/SIMULINK circuits wherein every possible failure mode can be studied. A hardware test setup that mimics the computer simulations would be an ideal way of enhancing understanding about component level faults and generating real data.

5.5 Chapter summary and conclusions

The previous chapters discussed the zonal SPS research arena and discussed the need to understand faults within the system. This fault study is essential to de-risk the novel architecture from effects of faults. Hence, the first step to commence research with this aim was identified as FMEA which could guide further research.

In this chapter, the zonal SPS under study was outlined with its constituents. Thereafter fundamentals of FMEA were elaborated, its sub-parts and its relevance for the system studied in this research. A detailed and meticulous analysis is conducted on the SPS network shown through numerous tables adhering to well established techniques. The outcome of a detailed FMEA in general is a list of pertinent issues that are ranked as per severity. As is expected, the F-FMEA enabled such a prioritisation to identify vital devices in the network. Logical reasoning further emphasised the results of the F-FMEA which led to the next step i.e. H-FMEA.

The H-FMEA study further helped focus attention on the device chosen, in this case the dc-dc buck converter designated as PCM-1. Research into component level failure modes, their causes and effects helped enhance understanding of underlying failure dynamics and mechanisms. The next step is to improve on this theoretical understanding by conducting computer simulations to study fault-related behaviour. Hardware studies are an ideal platform to verify simulation studies; however it should be taken into account that not all failures can be mimicked on test-setups due to safety considerations. Nevertheless, verification through hardware generated data forms an important step within research in the power electronics domain.

An important aspect to note is the language used to conduct FMEA. The tables filled are with concise information without resorting to lengthy elaborate explanations. The main idea is to inform the reader about failures by highlighting the message clearly. Once the precise relevant information is imparted, one can perform a detailed study using available resources if necessary.

Further research into using diagnostic techniques to aid developing an automated fault accommodation system is needed. The next chapter includes research conducted to develop a generalised technique to differentiate pertinent faults identified through FMEA in this chapter using another reliability analysis technique called sneak circuit analysis (SCA). The further study includes data generation by computer simulation using MATLAB/SIMULINK and an attempt to verify the results using hardware test-bed generated data.

Overall, the wider ranging benefits of using FMEA alongside the ones mentioned earlier in the chapter are to help generalising the effort to develop the FACS. After applying SCA (elaborated in the next chapter) for the most critical device chosen through FMEA (buck converter in this case), a similar approach combining FMEA and SCA could be applied to other devices and subsystems. Although this attempt to largely generalise the proposed methodology is out of the scope of this particular thesis, it is important to show the benefits of making FMEA (and its sub-parts) an essential effort to develop the FACS.

Chapter 6 Utilisation of Sneak Circuit Analysis for the Fault Accommodating Control System

6.1 Introduction

Chapter 4 explained the need to consider reliability analyses methods as an important aspect to develop the FACS for notional warships. For this purpose, FMEA and SCA were the two methods chosen. FMEA was established as the reasonable choice of reliability analysis to begin risk assessment studies for a novel system.

In section 5.2, an F-FMEA was conducted on the system level of the MVDC zonal SPS model, which helped identify critical sections and devices within the network that were vital to realise benefits of the novel power distribution architecture. Such an F-FMEA highlighted the importance of zonal buck converters and an added analysis in section 5.3 further emphasises this point. Consequently, a component level H-FMEA is shown in 5.4 which narrows pertinent faults occurring within vital devices identified previously, which in this case is the dc-dc buck converter that supplies power to individual zones.

This chapter explains SCA based analysis on the buck converter circuit, introducing a modification to the conventional approach. This novelty enables conventional SCA to output data that could be used to distinguish different operational states such as normal and fault scenarios. Data from a simulation in MATLAB-SIMULINK is used to perform the modified-SCA analysis on an experimental basis. A corresponding hardware circuit test setup is used to generate actual fault case and normal operation data, which too is processed in the same manner.

The simulation and actual data sets are used to generate heuristics by utilising the PART algorithm [13] in Weka [14]. One set of heuristics each for simulation and real circuits are compiled into conditional if-else statements. These conditional rules are first tested on their respective circuits and then the simulation circuit rules are tested offline on the hardware circuit data. This action helps assess two things,

1. Once we generate two sets of rules for software and hardware data, they are encoded and tested against their respective types of data. In other words, software rules are used to differentiate operational cases for a SIMULINK-

circuit data stream and hardware rules for the actual buck converter data stream. This helps ensure consistency of the rules, meaning that they are able to successfully distinguish different data types from the type of data source they were generated from.

2. Using rules derived from simulation data on the real hardware data, helps test feasibility of simulation studies to predict actual scenarios. A high success rate of simulation generated heuristics being able to diagnose faults for hardware data streams bodes well to follow a software-simulation based approach to visualise and study further fault cases. The approach could be extended to other circuits as well.

The major reason for employing PART through Weka is the ease of interpreting the output. The program provides a clear view of the conditional statements for every type of data presented to it, thereby making it easy to formulate if-else rules. A near identical alternate is provided by the J48 algorithm in Weka where the output is in the form of decision trees [122, 123].

6.2 Sneak circuit analysis (SCA)

SCA is a functional reliability analysis technique with the potential of detecting unintended and thereby undesirable system operation [85, 124]. A sneak circuit is defined as a latent path or condition that inhibits desired function or causes undesired function to occur. In contrast to failure effects, a sneak circuit does not require a component failure to occur. SCA is a unique method of evaluating the electrical circuit to detect specific patterns which are characteristic of sneak paths.

A sneak condition or path is present in a circuit, as designed, but may not always be active. SCA is typically performed during the design stage of an electrical circuit, in order to assess presence of any sneak paths and thus attempt to eliminate them. This research however does not involve designing new electrical circuits; hence SCA in its typical form is not used. Instead, a numerical modification to conventional SCA explained in this chapter shows its potential usefulness for this specific research work.

6.2.1 Obtaining sneak paths for an electrical circuit by constructing its directed graph

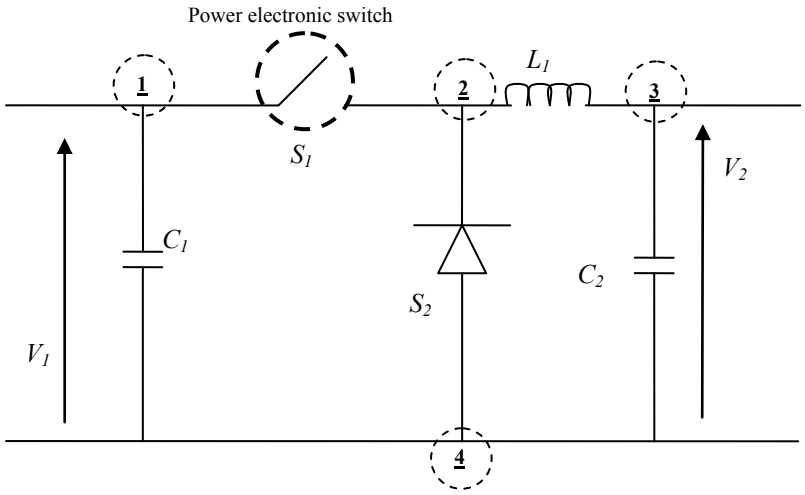
The sneak paths or sneak circuits are obtained through the determinant of the generalised connection matrix (GCM) [89, 92] which in turn is formulated by constructing the directed graph of the circuit studied. In general a directed graph of a

circuit depicts component connections with directions of associated currents and voltages. From this, an $N \times N$ (where N = no. of nodes) matrix can be constructed using component symbols. This matrix is the GCM and its determinant can provide sneak paths represented in terms of component symbols. The determinant could output numbers as well as terms with squared or higher order component symbols. These are ignored as they do not provide information regarding a logical electrical path, for example, a number is not a circuit path and a squared component symbol does not indicate its connection with other components in the circuit. Thus, what remains are possible and legitimate current paths within the given circuit. This information about sneak paths is useful in the design phase of a circuit in order to modify the design if a sneak path is identified or is to be avoided.

6.2.1.1 Example of conventional SCA

Fig.6.1 shows a standard dc-dc buck converter circuit with labelled components, voltages and nodes (junctions). This circuit will be used as reference in SCA shown hereafter for the buck converter.

Constructing the directed graph of the above circuit involves making a diagram depicting the probable current directions through each component based on its characteristics. Some components allow a unidirectional passage of current while others do so in either direction. These differences are shown by single or double arrow-heads from the corresponding node-point. A directed graph for the buck converter circuit of fig.6.1 is shown in fig. 6.2.



S_1 = Power electronic switch, could be IGBT, GTO etc., C_1 = Input side capacitor, S_2 = Freewheeling diode, L_1 = Inductor, C_2 = Output side filter capacitor, V_1 = Input voltage (dc), V_2 = Output voltage (stepped down dc)

Figure 6.1: Standard buck converter (dc-dc step down) circuit with numbered nodes

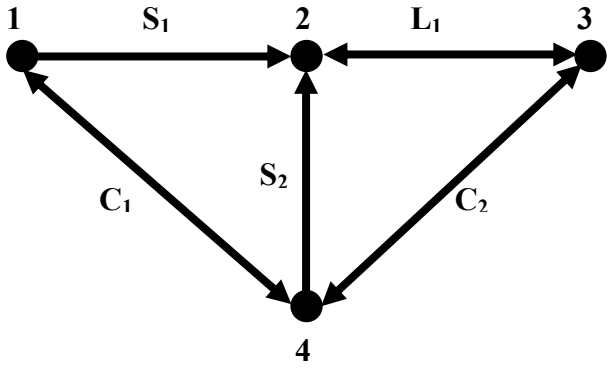


Figure 6.2: Directed graph of standard buck converter circuit

Next step is to construct the $N \times N$ generalised connection matrix (4×4 in this case). The matrix reflects the node to node connections of the individual components. The determinant of the matrix produces the various current paths possible within the circuit. Out of the total terms produced by the determinant, it is vital to cancel out unwanted paths and meaningless terms. These meaningless terms are typically numbers and terms having higher orders.

	1	2	3	4
1	1	S_1	0	C_1
2	0	1	L_1	0
3	0	L_1	1	C_2
4	C_1	S_2	C_2	1

Figure 6.3: GCM for buck converter directed graph

The determinant of the GCM in fig. 6.3 is shown below followed by the meaningful terms. The meaningful terms are those which do not contain numbers or higher power terms.

$$\text{Determinant, } |GCM| = 1 - C_2^2 - L_1^2 + S_2 \times L_1 \times C_2 - C_1 \times S_1 \times L_1 \times C_2 - C_1^2 + L_1^2 \times C_1^2$$

$$\text{Meaningful terms, } |GCM|' = S_2 \times L_1 \times C_2 - C_1 \times S_1 \times L_1 \times C_2$$

Equation 6.1

The paths highlighted by the determinant in eq.6.1 inform the circuit designer which paths are wanted and unwanted. Upon careful examination, the meaningful terms in eq. 6.1 reflect the various current loops that would exist in the given circuit. Fig. 6.4 illustrates the current paths as indicated by eq. 6.1. Owing to the advantage presented by understanding wanted and unwanted current paths, this analysis can be used typically in the design phase of a new circuit. However, any circuit in general can be subject to such an SCA to check existing current paths. Though this example showed an established buck converter topology, the redesigning is unnecessary as all the current paths are legitimate or wanted.

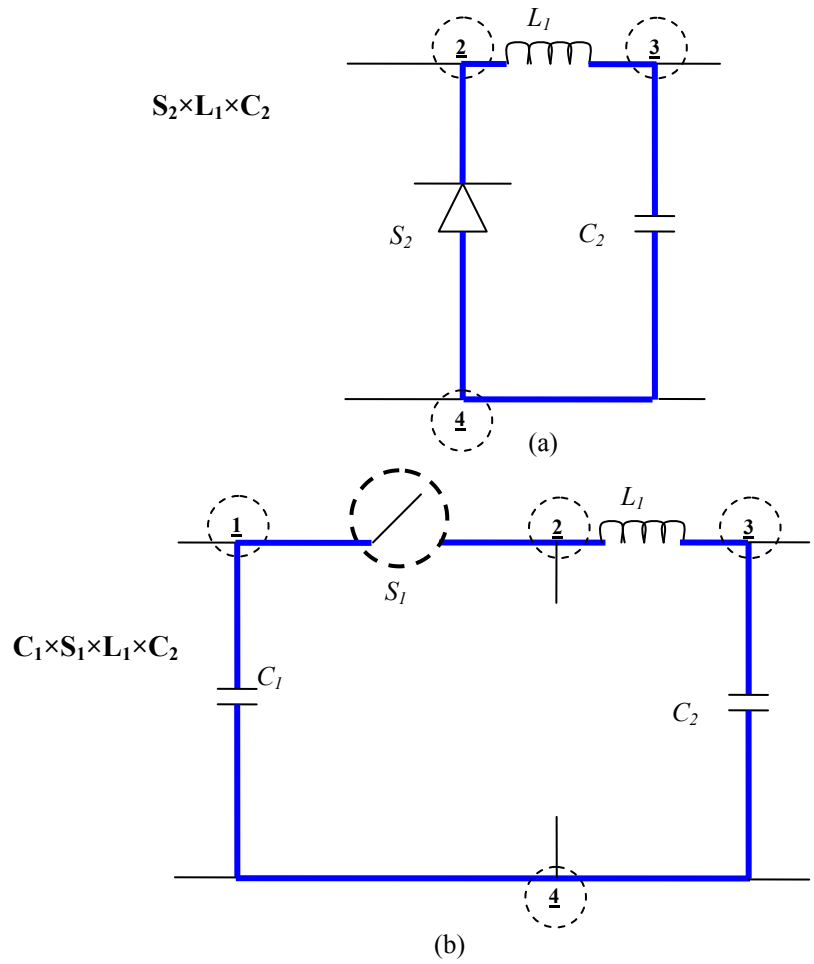


Figure 6.4: (a) The physical illustration of path represented by term $S_2 \times L_1 \times C_2$ (b) the path represented by term $C_1 \times S_1 \times L_1 \times C_2$

6.2.1.2 Modification to conventional SCA technique – The novelty of this research

The conventional SCA technique is a reliability analysis method used at the design phase of a circuit. Unwanted sneak paths can be eliminated by reviewing the design. This feature is not actually needed in this research as the converter circuits are well established and tested designs. The modification hence applied to this reliability analysis is in the idea that the directed graph for the circuit is made including the circuit current directions and end voltages. Thus, instead of the component symbols in the determinant, the output consists of currents and voltages. Following the SCA convention of ignoring numbers and higher order terms, the remainder of the terms produce numeric values from the determinant of the generalized connection matrix. These are used for generating signatures that could help differentiate between various fault patterns and normal operation of the circuit.

Also, a further modification applied is in considering the on and off states of the semiconductor switch at the beginning of the analysis. The equivalent on and off-state circuits are in turn used to construct the modified directed graph and then the corresponding GCM. This yields two separate numeric equations that reflect the basic circuit operations and might enhance the ability to differentiate between operating scenarios.

The measured and calculated currents are used to generate the connection matrix. This in turn produces numeric values from the matrix's determinant which can help differentiate between various operating scenarios.

The circuit for a standard buck converter of fig. 6.1 is shown below (fig. 6.5) with components and voltages depicted in text-boxes with the input and output currents. Nodes are also numbered and it can be noted that there are 6 as opposed to 4 shown in the conventional SCA of fig. 6.1, fig. 6.2 and fig. 6.4. It is important to note that extra nodes (which could be called pseudo-node or virtual-node) have been numbered at either ends of the circuit in fig.6.5. These virtual nodes no.1 and 5 in the circuit simplify the analysis by providing a numbered path for the input and output currents at either end.

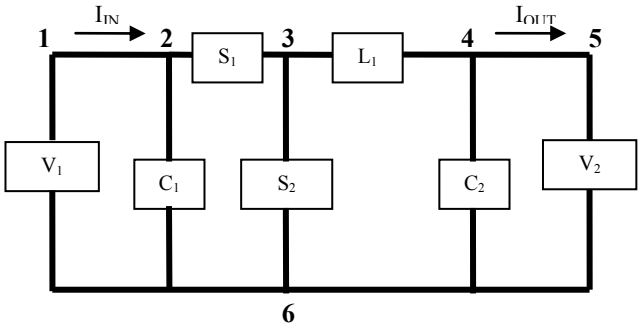
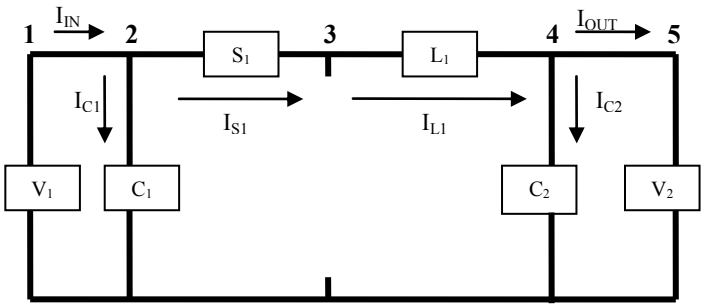


Figure 6.5: Standard buck converter circuit represented to use for SCA analysis

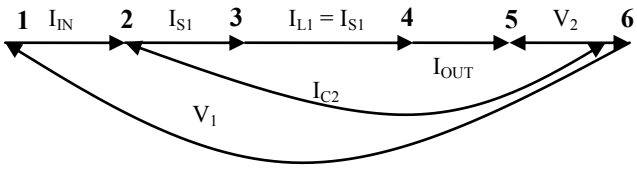
To draw the directed graph of this circuit, one needs to take into account the possible current paths through every component. Also, one needs to consider the two states of the circuit i.e. when the switch S_1 is ON (when current passes through it) and when it is OFF (when it blocks passage of the input current).

ON state equivalent circuit – Buck converter

Fig. 6.6 shows the equivalent circuit when the switch S_1 is turned on. The directed graph in terms of the current paths is shown below with the connection matrix.



(a)



(b)

	1	**2**	**3**	**4**	**5**	**6**
1	1	I_{IN}	0	0	0	V_1
2	0	1	I_{S1}	0	0	I_{C1}
3	0	0	1	I_{S1}	0	0
4	0	0	0	1	I_{OUT}	I_{C2}
5	0	0	0	0	1	V_2
6	V_1	I_{C1}	0	I_{C2}	V_2	1

(c)

Figure 6.6: (a) ON state equivalent circuit in which case $I_{S1} = I_{L1}$ (b) ON state modified directed graph (c) ON state modified GCM

The determinant of the GCM is,

$$ON\_state = 1 - V_1^2 - I_{C1}^2 + I_{C1} \times I_{IN} \times V_1 - I_{C2}^2 + I_{C2} \times I_{S1}^2 \times I_{C1} + I_{C2} \times I_{S1}^2 \times I_{IN} \times V_1 - V_2^2 + V_2 \times I_{OUT} \times I_{C2} + V_2 \times I_{OUT} \times I_{S1}^2 \times I_{C1} - V_2 \times I_{OUT} \times I_{S1}^2 \times I_{IN} \times V_1$$

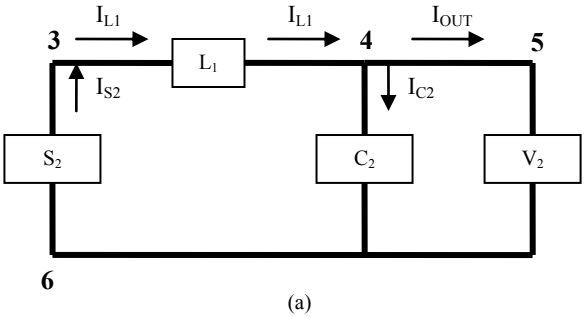
Ignoring the terms with higher order parts, the final usable equation is,

$$|S1on| = I_{C1} \times I_{IN} \times V_1 + V_2 \times I_{OUT} \times I_{C2}$$

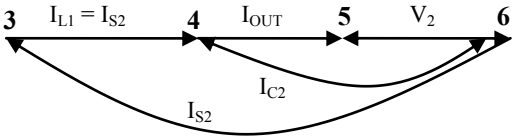
Equation 6.2

OFF state equivalent circuit – Buck converter

In S_1's off state, the diode S_2 completes the current path. The corresponding equivalent circuit, directed graph and connection matrix are shown below.



(a)



(b)

	3	**4**	**5**	**6**
3	1	I_{S2}	0	0
4	0	1	I_{OUT}	I_{C2}
5	0	0	1	V_2
6	I_{S2}	I_{S2}	V_2	1

(c)

Figure 6.7: (a) S1-OFF state equivalent circuit, in which $I_{S2} = I_{L1}$ (b) OFF state modified directed graph (c) OFF state modified generalised connection matrix

The determinant of the GCM is,

$$OFF\_state = 1 - V_2^2 + V_2 \times I_{OUT} \times I_{C2} - I_{C2}^2 + I_{OUT} \times I_{S2}^2 \times V_2 + I_{S2}^2 \times I_{C2}$$

Ignoring the terms with higher order parts, the final usable equation is,

$$|S_1 off| = V_2 \times I_{OUT} \times I_{C2}$$

Equation 6.3

Eq. 6.2 and 6.3 form the representations of the buck converter's fundamental operational states. Later in this chapter, these equations are shown to distinguish between normal and fault scenarios.

6.3 Simulation studies using proposed approach

The previous sections in this chapter explained basic SCA and the modification to convention that forms the novelty in this research. Two equations were derived that are shown in this section to be able to provide distinguishable signals for different operational states of the converter. The next subsection explains the simulations carried out using a buck converter circuit modelled in MATLAB-SIMULINK.

6.3.1 Buck converter modelled in SIMULINK to generate data and corresponding hardware setup

Section 5.4.2 of the previous chapter provided detailed information on failure modes for a buck converter through tables 6.38 to 6.42. The two common failure modes for every component are short and open circuits. Hence, the circuit used for simulations (software as well as hardware) are designed primarily to carry out short and open circuit fault studies to generate data. Another type of failure mode studied through simulations is gradual degradation of component mainly occurring in capacitors and inductors. No feedback controls have been employed on the SIMULINK converter circuits as the main focus of this research is reporting the use of the proposed technique for diagnostic purposes and not the control strategy for converters in case of faults.

In case of a semiconductor-switch failure, short-circuit is typically the first step of the semiconductor fault [125] which rapidly progresses eventually to an open-circuit failure in the switch. Open-circuit faults also need to be studied as permanent blocking could be caused by the gate-drive malfunction. Here, the open-circuit faults, whether device or gate-drive related, are simulated as a power switch open circuit fault. Short-circuits are simulated using a bypass switch in parallel while open circuits are simulated using an opening switch in series as shown in fig. 6.8(a) and (b).

The dc-dc buck converters in general contain 5 components namely, input side capacitor (C_1), output side capacitor (C_2), inductor (L_1), semiconductor switch (S_1) and free-wheeling diode (S_2) as shown in the reference diagram fig. 6.1. The short

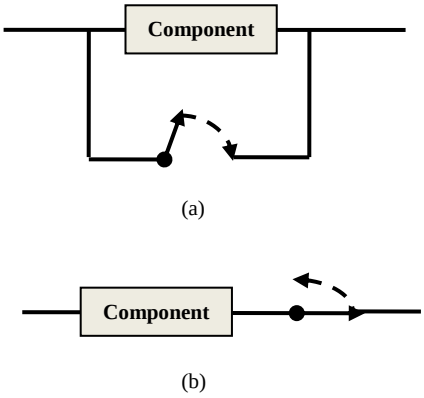


Figure 6.8: (a) When switch closes; the component is bypassed simulating a short circuit (b) When switch opens; the component is cut-off simulating an open circuit

circuit and open circuit failures happen over very small time durations without much prior notice. But, components like capacitors and inductors can degrade over time (several hundred hours) until they completely fail. These incipient failures if detected accurately can help with taking remedial action long before failure takes place. For this purpose, fault simulations involving reduction in capacitance and inductance were conducted. The converter circuits include two series connected inductors (making up L_1) and two parallel connected capacitors (making up C_2) as mentioned in table 6.1. One of the inductors is short-circuited thereby halving the inductance while one capacitor is open circuited to halve the net capacitance.

The modified SCA equations derived for the switch on and off-states for the buck converter contain either one of the input or output-side terms or an addition of both as understood from eq. 6.2 and 6.3 in subsection 6.2.1.2. In order to show the effectiveness of these equations, data is needed which can be processed to form these equations and used for distinguishing operational scenarios. A buck converter circuit was developed in SIMULINK (fig.9) to generate the required quantities with an IGBT as the semiconductor switch.

The quantities required to form the equations are either directly measured or calculated from known formulas. The required quantities are input capacitor current (I_{C1}), input current (I_{IN}), input voltage (V_1), output capacitor current (I_{C2}), output current (I_{OUT}) and output voltage (V_2). Typically, the input/output currents and voltages are directly measured using appropriate sensors.

Quantity	Symbol	Set value	Measurement
Input current	I_{IN}	*0.625 A or 625 mA*	*Direct via current meter*
Input voltage	V_1	*15 V*	*Direct via voltage meter*
Output current	I_{OUT}	*1.25 A or 1250 mA*	*Direct via current meter*
Output voltage	V_2	*7.5 V*	*Direct via voltage meter*
Input capacitor	C_1	*100μF*	*Known*
Filter capacitor at output	C_2	*13.6μF, made up of two parallel connected capacitors of 6.8μF each*	*Known*
Input capacitor current	I_{C1}	*Proportional to capacitance*	*Indirectly obtained using* $C_1 \times \frac{dV_1}{dt}$
Output capacitor current	I_{C2}	*Proportional to capacitance*	*Indirectly obtained using* $C_2 \times \frac{dV_2}{dt}$
Inductor	L_1	*1.2mH, made up of two series connected inductors of 0.6mH each*	*Known*
Duty cycle	δ	*50 % or 0.50*	*Known*
Switching frequency	f	*10kHz*	*Known*
Switching cycle time	t	*100μs*	*Known*
Output resistance	R	*6Ω*	*Known*

Table 6.1: Description of required quantities to form modified-SCA equations

Fig.6.9 shows the buck converter circuit modelled in SIMULINK. The input and output currents and voltages are measured in the simulation.

A hardware setup (fig.6.10) is with identical specifications as the SIMULINK version of the buck converter circuit. In a software simulation, every type of failure mode can be studied which is not the case for a hardware circuit. Keeping in mind safety issues, only some failure mode studies were conducted using the test setup. The failure modes studied and their results compared on both software and hardware tests are shown in table 6.2. Table 6.2 also outlines the expected observation which can be used as a basic benchmark to monitor the test manually. Although, some differences to the plots of operational cases may not be visible to the naked eye, the subtle differences are anticipated to be useful to form a computer aided diagnosis.

Tables 6.3-6.6 show comparative plots of the SIMULINK and hardware circuits for fault cases studied. The multiple fault case's plot is not shown here to avoid repetition as it closely resembles the individual inductor and capacitor faults. However, the multiple fault data is included for classification and generation of rules for forming a diagnosis. The idealised voltage source used in SIMULINK means that the input voltage is constant at the stated value. The output current follows the output

voltage. Hence only the input current and output voltage waveforms have been shown in figures in tables 6.3-6.6. Knowing that even for the hardware setup, the input voltage is practically constant; the corresponding waveforms show input current and output voltage to maintain consistency with SIMULINK circuit plots.

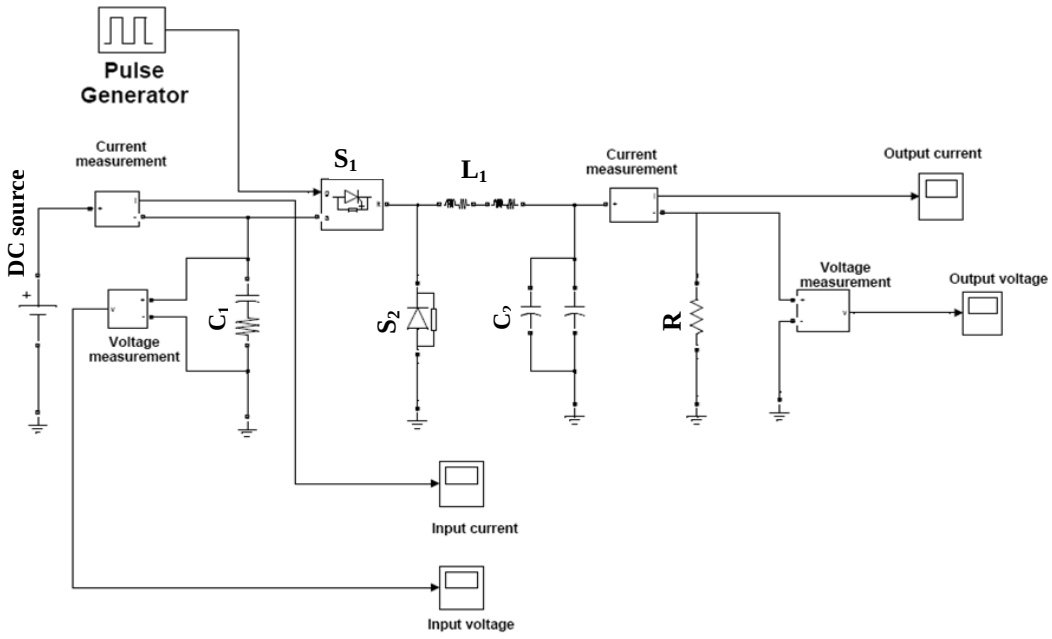


Figure 6.9: Buck converter circuit in SIMULINK

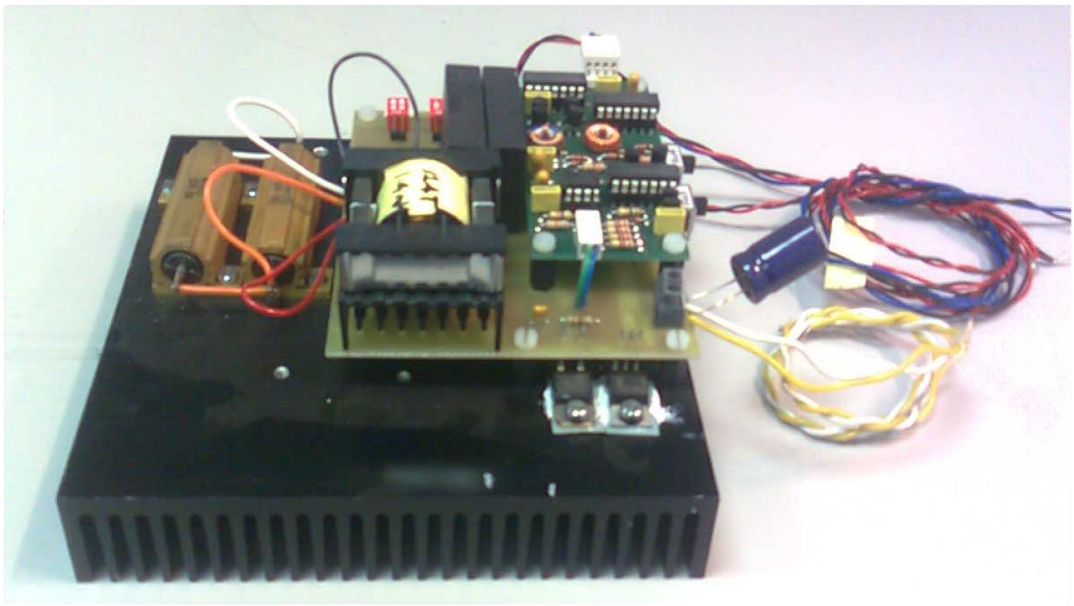


Figure 6.10: Buck converter hardware setup

Component	Failure mode induced	Expected observations at output
Capacitor (C_2) [single fault]	Degrading – Net filter capacitance is reduced to half the original value at start of simulation.	The ripple at output voltage gradually increases with time.
Semiconductor switch (S_1) [single fault]	Short circuit.	The output voltage rises above its required value immediately.
	Open circuit.	The output voltage suddenly drops to zero.
Inductor (L_1) [single fault]	Winding shorts – Net inductance reduced to half the original value at start of simulation.	Gradual increase in ripple which may be more or less than for the capacitor fault case.
Inductor (L_1) and capacitor (C_2) [multiple fault]	Both the filter capacitor and inductor values are altered using the same strategy as previous individual cases respectively.	Practically identical response to single fault in filter components (capacitor, inductor mentioned above).
Total number of fault cases	5	

Table 6.2: Faults studied for comparison between SIMULINK and hardware buck converter circuits [70]

The comparative plots show that although factors such as noise, wire resistance etc. are presents in the hardware data, the software model is acceptable as a study tool. A software model is obviously a vital part of the entire research process and hence it is necessary to validate how close it is to an actual hardware circuit. Once an acceptable level of accuracy is obtained from the SIMULINK model, various tests and experiments can be conducted to further enhance understanding about possible fault scenarios. However, as mentioned earlier, the hardware setup has limitations owing to safety issues for conducting fault experiments. Thus it is advantageous to perform a rigorous study of the modelling software used in order to arrange a circuit model whose behaviour is as close as possible to its hardware counterpart.

The next subsection describes the method to process the data set to be used. This is an important aspect which needs careful attention because for further tests the same process needs to be repeated to ensure consistency. One also needs to have a working knowledge of using Weka for training and testing the data sets used.

6.3.2 Data preparation for heuristic classification

This subsection explains the manner in which the data sets are processed for classification [70]. The method used for preparing data to be fed into the classifier is identical to both circuits. Data collection for both, fault and no-fault cases was done at a 10ns sampling rate over a 1ms time period amounting to 100,000 samples each. Using eq. 6.2 and 6.3, the values $|S1on|$ and$|S1off|$ respectively are computed for the switch's operating states. Table 6.1 shows the quantities measured directly and those that need to be estimated through well known formulae such as for the time rate of

flow of charge through a capacitor (or capacitor current) being equal to the product of the capacitance and time rate of change of voltage across it i.e. $I_{capacitor}$ = *Capacitance* × *d(Voltage)/dt.* Other quantities (mainly currents) can be computed if needed using Kirchoff's current laws. The individual quantities are used to obtain the final values of |*S1on*| and |*S1off*| for every data sample.

There are then 12 data sets, six for |*S1on*| (5 fault cases + no fault case) and six for |*S1off*|. Each set is separately processed by the classification algorithm. This data used in the classifier is first divided into ranges and windows. The range variable reflects the total number of samples considered by the classifier at one time and is set ideally in integral multiples of one switching cycle. Since one switching cycle is 100μs (refer table 6.1), there are 10 full cycles in a simulation time of 1ms. Thus each cycle produces 10,000 samples out of a total of 100,000.

These ranges are separated and labelled as per the data type. The window is the number of data points considered within each range. The idea is to use a small window size which then reflects the amount of samples needed per cycle to classify the data. Thus, a small window size produces a faster result. Further, the data is sorted in ascending order within each window. The final data set for the six cases consists of a number of rows (6 × range) and number of columns (6 × window). An extra column is added at the end of each row to assign its label. This file is saved in an Attribute Relation File Format (.arff) to be used in the Weka classification software[126] an example of which is shown in fig. 6.11.

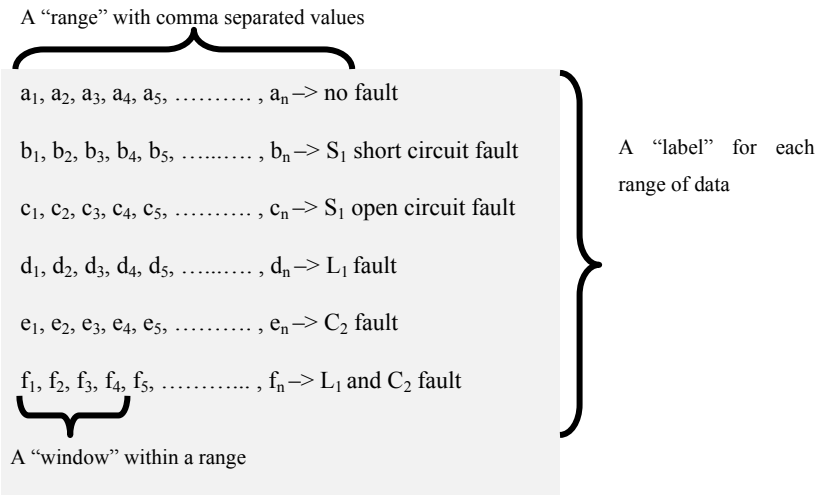
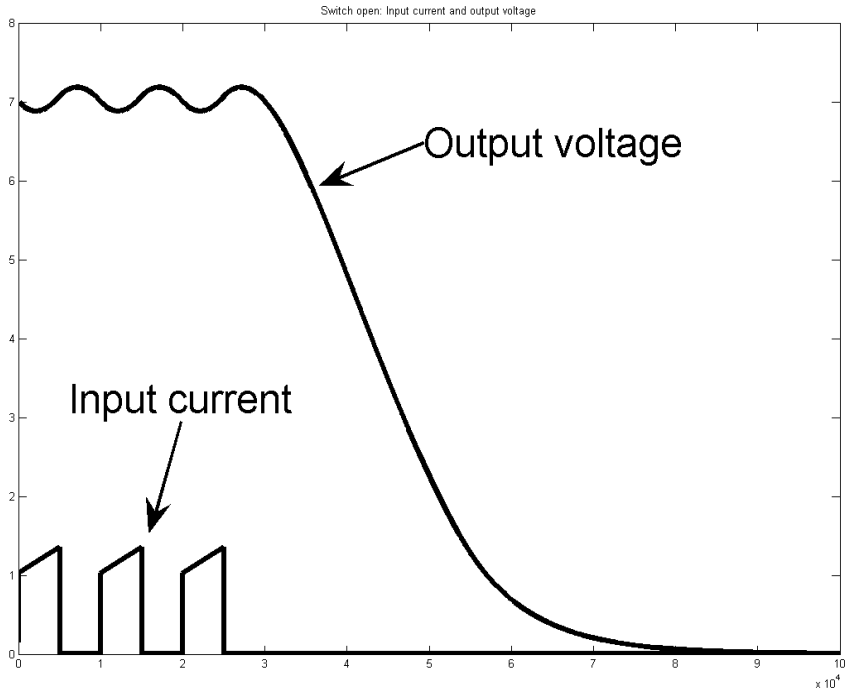


Figure 6.11: Example of building an arff. file for classification using PART algorithm in Weka

Operating scenario : Semiconductor switch (S_1) open circuit fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

SIMULINK circuit plot (input current and output voltage)



Hardware circuit plot (input current and output voltage)

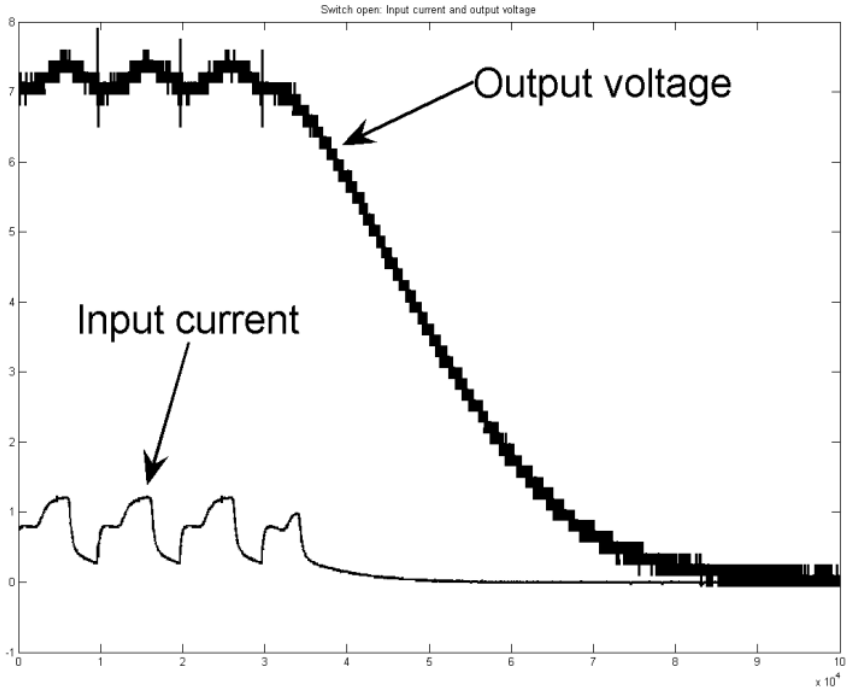
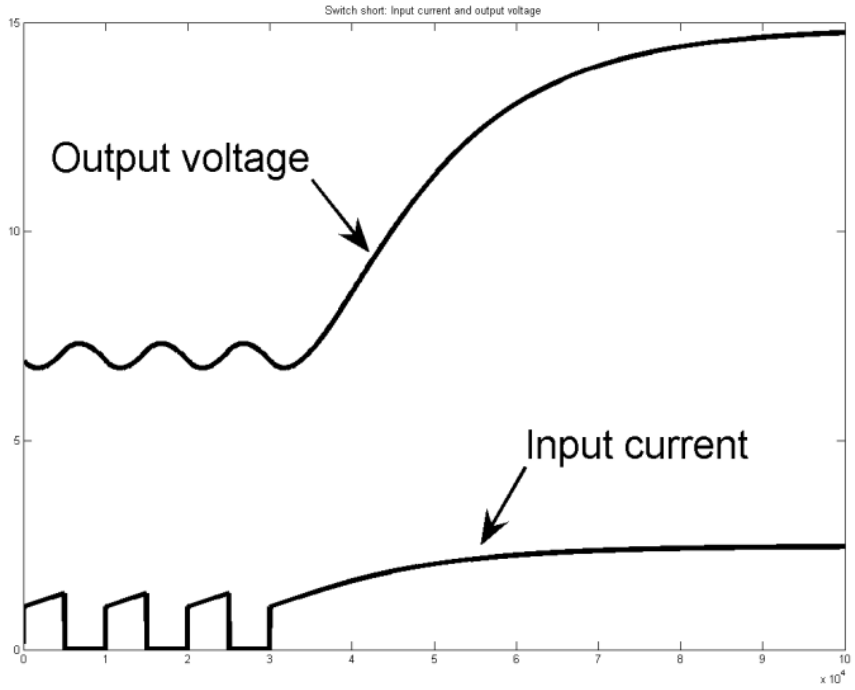


Table 6.3: Switch open circuit fault, data plots comparison

Operating scenario : Semiconductor switch (S_1) short circuit fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

SIMULINK circuit plot (input current and output voltage)



Hardware circuit plot (input current and output voltage)

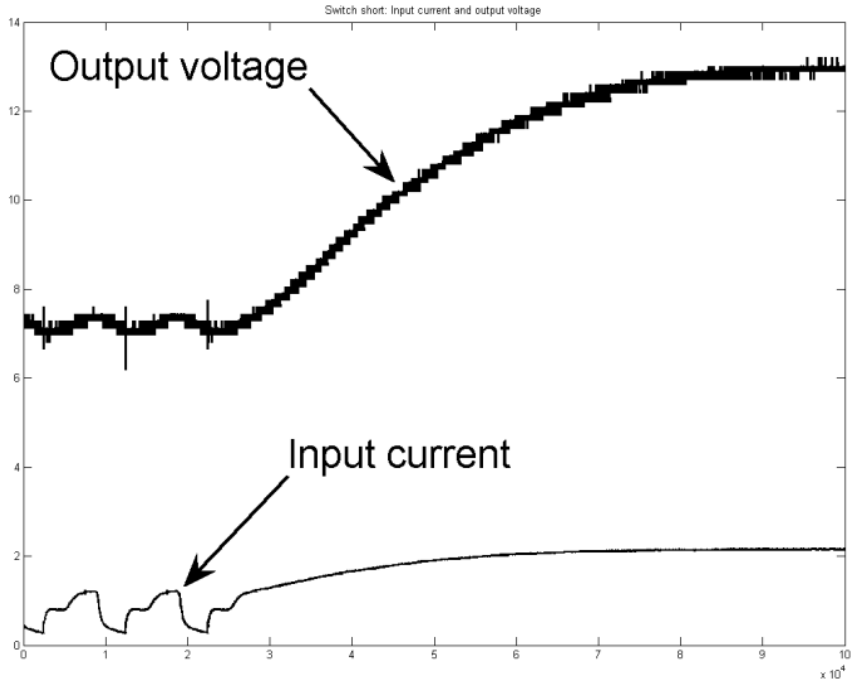
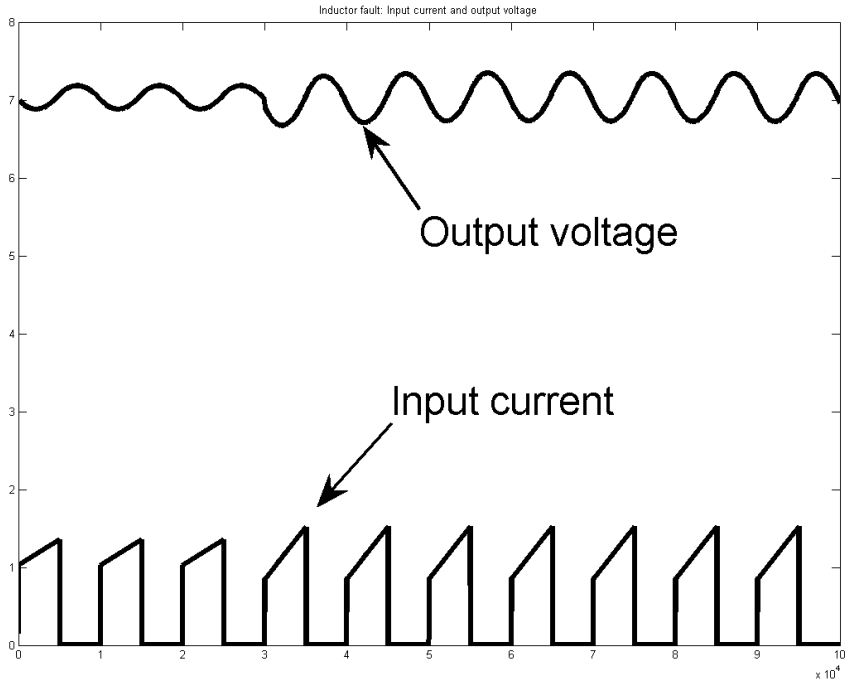


Table 6.4: Switch short circuit fault, data plots comparison

Operating scenario : Inductor (L_1) fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

SIMULINK circuit plot (input current and output voltage)



Hardware circuit plot (input current and output voltage)

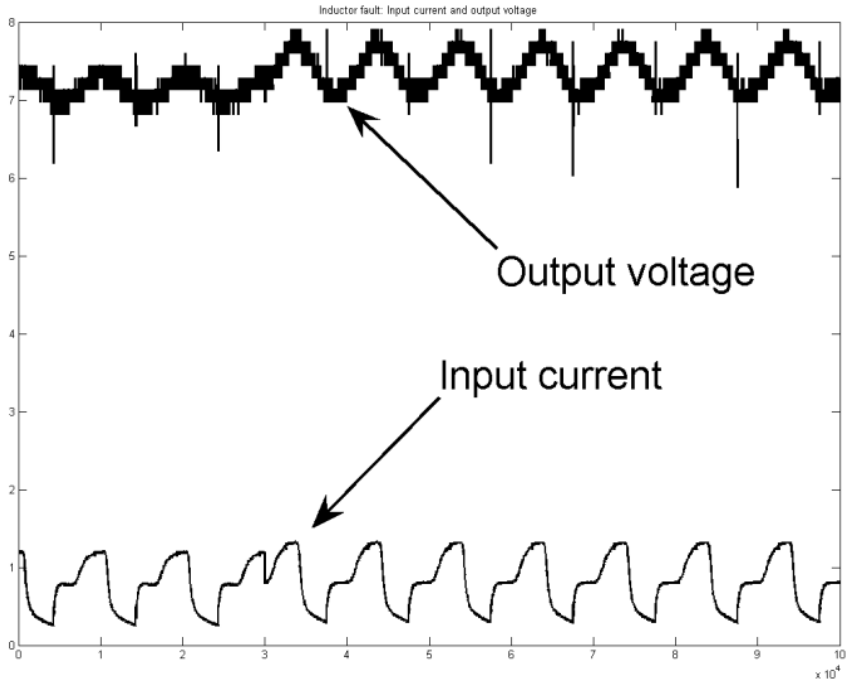
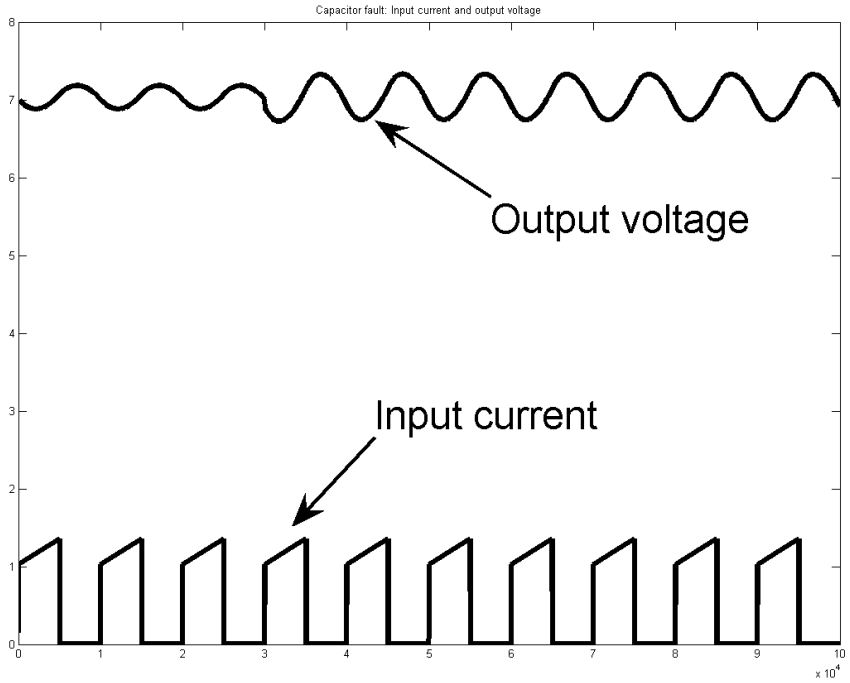


Table 6.5: Inductor fault, data plots comparison

Operating scenario : Capacitor (C_2) fault case
x axis: Time in ns (10×10^5ns), y axis: General unit to numerically show current in mA and voltage in V

SIMULINK circuit plot (input current and output voltage)



Hardware circuit plot (input current and output voltage)

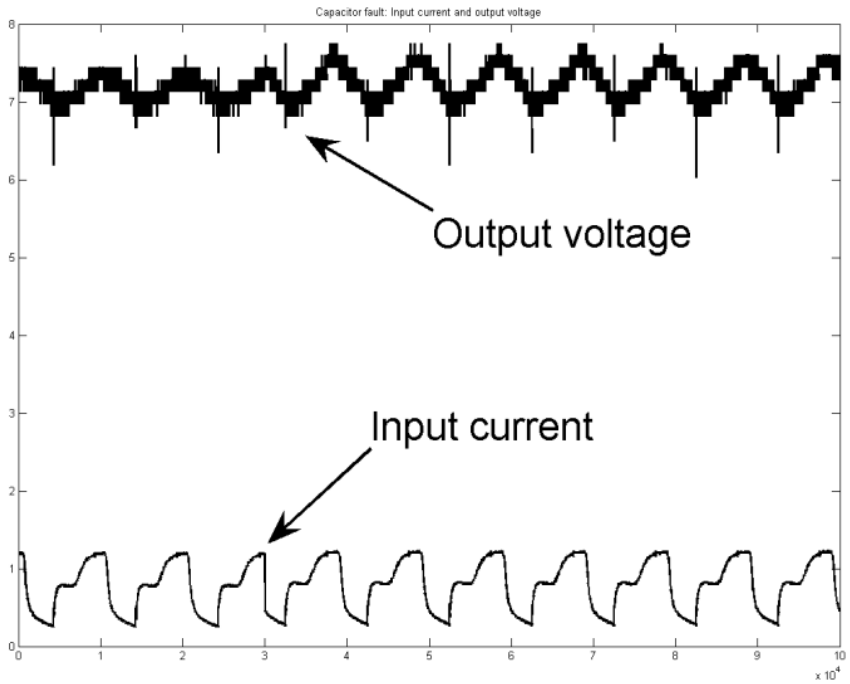


Table 6.6: Capacitor fault, data plots comparison

6.3.3 Comparison of classification results and their interpretation

In this subsection the data results from the hardware and software circuits are compared. Data produced for both cases was used with the classifier employing the PART algorithm in the software package Weka. The data was re-sampled at 100ns thus reducing the total captured data-samples by a factor of 10. Re-sampling eases the computational effort and memory requirements of the classifier. The algorithm uses a 10-fold cross validation testing scheme to calculate error rates. The output is a set of rules and a confusion matrix that shows the number of correctly and incorrectly classified instances. Below is a breakdown of results for the two states of the semiconductor switch for both hardware and software circuits.

1. Results for the |*S1off*| equation

   The processed data had the following attributes after re-sampling,

   total samples = 10,000 ; range = 2,000 ; window = 10

   total number of data sets = 6 (1 no fault case + 5 fault cases)

   With six data sets used, the total range becomes 6×2,000 = 12,000. The confusion matrix with the rule set is shown in fig. 6.12. The 23 classification rules for the hardware data are shown in table 6.3.

2. Results for the |*S1on*| equation

   The data attributes are identical to the |S1off| case used previously. The data is re-sampled in Weka in a similar manner. The confusion matrix with the rule set is shown in fig. 6.13. The 13 classification rules for the hardware data are shown in table 6.4. It is important to note that the SIMULINK circuit consists of an ideal voltage source which exhibits zero source impedance. This is unlike the case in the real hardware circuit. The implication is that in the simulation, $dV_I/dt = 0$ which means the input capacitor current $I_{CI} \approx 0$.

a	b	c	d	e	f
2000	0	0	0	0	0
0	2000	0	0	0	0
0	0	2000	0	0	0
0	0	2	1989	9	0
0	0	2	1	1997	0
0	0	0	0	0	2000

Number of Rules generated: 23
Classification rate: 99.883%

(a) Hardware data

a	b	c	d	e	f
1956	0	0	0	0	44
0	2000	0	0	0	0
0	0	2000	0	0	0
0	0	0	2000	0	0
47	0	0	0	1918	35
62	0	0	0	0	1938

Number of Rules generated: 10
Classification rate: 98.433%

(b) Software data

where; a = no fault data, b = switch short circuit fault data, c = switch open circuit fault data, d = inductor fault data, e = capacitor fault data, f = inductor & capacitor fault data.

Figure 6.12: (a) Confusion matrix for |S1off| equation for hardware circuit data (b) Confusion matrix for |S1off| equation for SIMULINK circuit data

a	b	c	d	e	f
1998	0	0	0	0	2
0	2000	0	0	0	0
0	0	2000	0	0	0
1	0	0	1999	0	0
0	0	0	0	2000	0
0	0	0	0	0	2000

Number of Rules generated: 13
Classification rate: 99.975%

(a) Hardware data

a	b	c	d	e	f
1950	0	0	0	16	34
0	2000	0	0	0	0
0	0	2000	0	0	0
0	0	0	2000	0	0
15	0	0	0	1954	31
14	0	0	0	0	1958

Number of Rules generated: 9
Classification rate: 98.85%

(b) Software data

where; a = no fault data, b = switch short circuit fault data, c = switch open circuit fault data, d = inductor fault data, e = capacitor fault data, f = inductor & capacitor fault data.

Figure 6.13: (a) Confusion matrix for |S1on| equation for hardware circuit data (b) Confusion matrix for |S1on| equation for SIMULINK circuit data

From fig. 6.12 and 6.13 it can be observed that the |*S1on*| equation produces marginally better results than the |S1off| for both software and hardware data. The difference in accurate classification in either case is less than 1%.

The rules produced by the PART algorithm can be understood using conditional execution statements as shown in tables 6.7 and 6.8. The algorithm uses the absolute values of the data fed to it (in this case the six data sets) to produce thresholds. The heuristics are derived for these absolute values. The data stream is input in windows of the specified length. The rules are output with reference to the position of every value within the window. Knowing that the data used was divided into a window size of 10, then the terms "Value1" or "Value9" refer to the 1st and 9th elements respectively in a given window.

Rules 1-5	Rules 6-10	Rules 11-15	Rules 16-20	Rules 21-23
IF Value8 > -500.26 AND Value5 <= -350.48 AND Value1 > -698.16 AND Value9 > -358.19 AND Value8 <= -212.37 AND Value4 > -500.26 THEN data is of type ‘a’	IF Value2 > -349.08 AND Value1 > -341.57 AND Value1 <= -224.59 THEN data is of type ‘c’	IF Value2 > -341.57 THEN data is of type ‘d’	IF Value1 > -349.08 AND Value8 <= 0 AND Value7 > -334.53 AND Value1 <= -224.59 AND Value3 <= -341.57 AND Value4 <= -218.48 AND Value6 <= -334.53 THEN data is of type ‘e’	IF Value8 <= -500.26 AND Value4 > -683.15 AND Value2 <= -806.82 THEN data is of type ‘f’
IF Value2 <= -665.33 AND Value2 > -727.5238 THEN data is of type ‘a’	IF Value3 > -332.666 AND Value3 <= -218.4866 THEN data is of type ‘c’	IF Value8 <= -212.37 AND Value2 <= -500.2624 THEN data is of type ‘e’	IF Value1 > -349.08 AND Value8 <= 0 AND Value7 > -218.48 AND Value6 > -218.48 AND Value1 <= -224.59 AND Value3 <= -341.57 THEN data is of type ‘e’	IF Value5 <= -500.26 AND Value2 > -619.93 THEN data is of type ‘f’
IF Value1 <= -349.08 AND Value1 > -500.26 THEN data is of type ‘a’	IF Value2 <= -698.16 AND Value9 <= -212.37 THEN data is of type ‘d’	IF Value2 > -349.08 AND Value2 <= -341.57 AND Value10 > -341.57 AND Value1 > -349.08 AND Value8 <= -334.53 THEN data is of type ‘e’	IF Value8 <= -365.89 AND Value4 <= -569.77 THEN data is of type ‘e’	IF Value1 <= -500.26 THEN data is of type ‘f’
IF Value8 <= -500.26 AND Value6 <= -727.5238 THEN data is of type ‘b’	IF Value8 <= -212.37 THEN data is of type ‘d’	IF Value1 > -727.52 AND Value2 > -349.08 AND Value2 <= -218.48 AND Value1 <= -500.26 THEN data is of type ‘e’	IF Value7 <= -218.48 THEN data is of type ‘e’	
IF Value2 <= -500.26 AND Value1 <= -619.93 THEN data is of type ‘b’	IF Value3 <= -218.48 THEN data is of type ‘d’	IF Value1 > -349.08 AND Value8 <= 0 AND Value3 <= -341.57 AND Value10 > 174.59 THEN data is of type ‘e’	IF Value8 <= 0 AND Value7 > -218.48 AND Value3 > -218.48 AND Value2 > -218.48 THEN data is of type ‘e’	

Table 6.7: Rules generated using |*S1off*| for hardware data

Rules 1-3	Rules 4-6	Rules 7-9	Rule 10-12	Rule 13
IF Value3 <= -3473 AND Value9 <= -2001.3696 AND Value1 <= -4130.2624 THEN data is of type ‘a’	IF Value1 > -942.24 THEN data is of type ‘c’	IF Value1 > -2605.36 AND Value7 <= -491.18 THEN data is of type ‘e’	IF Value6 > -3563.6 AND Value2 > -1800 AND Value2 <= -499.73 THEN data is of type ‘f’	IF Value5 > -3630 AND Value2 <= -350.48 THEN data is of type ‘a’
IF Value1 > -3580.4848 AND Value2 <= -3050.2 THEN data is of type ‘a’	IF Value1 <= -1766.7 AND Value2 <= -1848.24 AND Value9 > -3473 THEN data is of type ‘d’	IF Value1 > -1766.7 THEN data is of type ‘e’	IF Value1 > -4223.15 AND Value1 <= -3654.2 AND Value2 <= -3654.2 AND Value3 <= -3805.2 THEN data is of type ‘f’	
IF Value2 <= -4983 THEN data is of type ‘b’	IF Value3 <= -3998.16 AND Value9 > -3890.93 THEN data is of type ‘d’	IF Value1 <= -4677.37 THEN data is of type ‘e’	IF Value2 <= -1536 AND Value1 > -3998.16 AND Value8 > -3360 AND Value1 <= -3654.2 THEN data is of type ‘f’	

Table 6.8: Rules generated using |*S1on*| for hardware data

6.3.4 Application of results and avoiding false alarms

The rules listed in table 6.8 (|*S1on*| equation) were coded in MATLAB to test the ability to detect the fault types. The major reason for choosing |*S1on*| is its marginally higher classification rate. This fault detection was done offline. However, investigation is ongoing to use a similar approach for a real-time online application. The results of the offline application are plotted on the same graph as the output voltage waveforms (tables 6.9-6.12). This shows when the fault was introduced and gives an idea of the time taken by the proposed method to detect it. The plots show that the encoded heuristics are able to indicate the presence of a fault for each case. The data was collected for a total of 2ms at a 10ns sampling rate (total 200,000 samples). As before, this is re-sampled at 100ns (total 20,000 samples). The fault is introduced at 1ms for each case.

To avoid false alarms, the frequency of the fault indications was included over batches of data samples. This was performed using additional code which counts the number of fault indications every 5000 samples of the 100ns re-sampled data i.e. every 0.5ms, and indicates a fault only if more than 10 events are counted. A slight modification to this fault indicator counting scheme had to be used for the switch open circuit fault case. Since the switch being 'open' is a legitimate state of the circuit, the output would show a fault indicator continuously.

Hence, to detect the introduction of this type of fault, consecutive fault indications were counted per 0.5ms worth of data as opposed to the total number for other fault types mentioned. This was done based on the notion that since the switch open circuit would occur every cycle, only a large enough consecutive count will suggest a permanent switch open circuit failure. Therefore, the added code was modified to count 200 consecutive fault indications per 5000 data samples (i.e. worth 0.5ms). Tables 6.9-6.12 show the instant when a fault-signal is indicated while the classifier rules can be used to diagnose the type of fault.

This frequency check was found to reduce the number of false alarms while preserving the speed and reliability of fault detection. A similar procedure could be used over a larger or smaller batch size of data samples. Too large a batch (over 8000) might not reduce false alarms significantly, while too small a batch (below

4000) may impose additional computational burden. It was preferred to use a batch size of 5000 samples as it conveniently divides the pre-fault and post-fault parts of the data into two sub-parts each.

Fig. 6.14 illustrates the step by step process of using the proposed approach of how one can encode the classifier-rules to help differentiate a data stream thereby enabling distinguishing various operating scenarios. The systematic procedure is explained in brief as follows:

Step 1 *– Use measured data and known parameters to compute |S1on| for each sample*

Step 2 *– Divide and process the data into the correct range and window lengths*

Step 3 *– Use IF-THEN-ELSE statements mirroring the rules generated to form a primary diagnosis indication*

Step 4 *– Count the fault indicator as per the prescribed counting-scheme to avoid false alarms and improve reliability of the fault indication and declare the diagnosis result*

6.3.5 Training hardware data on software data generated rules

This subsection performs an important test within Weka to test software-data generated rules on hardware data. The same approach is applied here as before with regards to data preparation and using the sample-counting scheme to avoid false alarms. The $|S1on|$ equation is used as basis like in the previous subsection. Confusion matrices are shown in fig. 6.15.

The confusion matrix in fig. 6.15(c) shows an accuracy of approximately 62% for differentiating types of operational cases from one another. The rules generated shown in table 6.13 are used to see their fault indicating capability on a real-time data stream.

When compared to the classification rates of software or hardware only confusion matrices which are very close to 100%, this testing seems at a rate much lower than desired. However, it still may be prudent to continue with real time testing of rules as done previously.

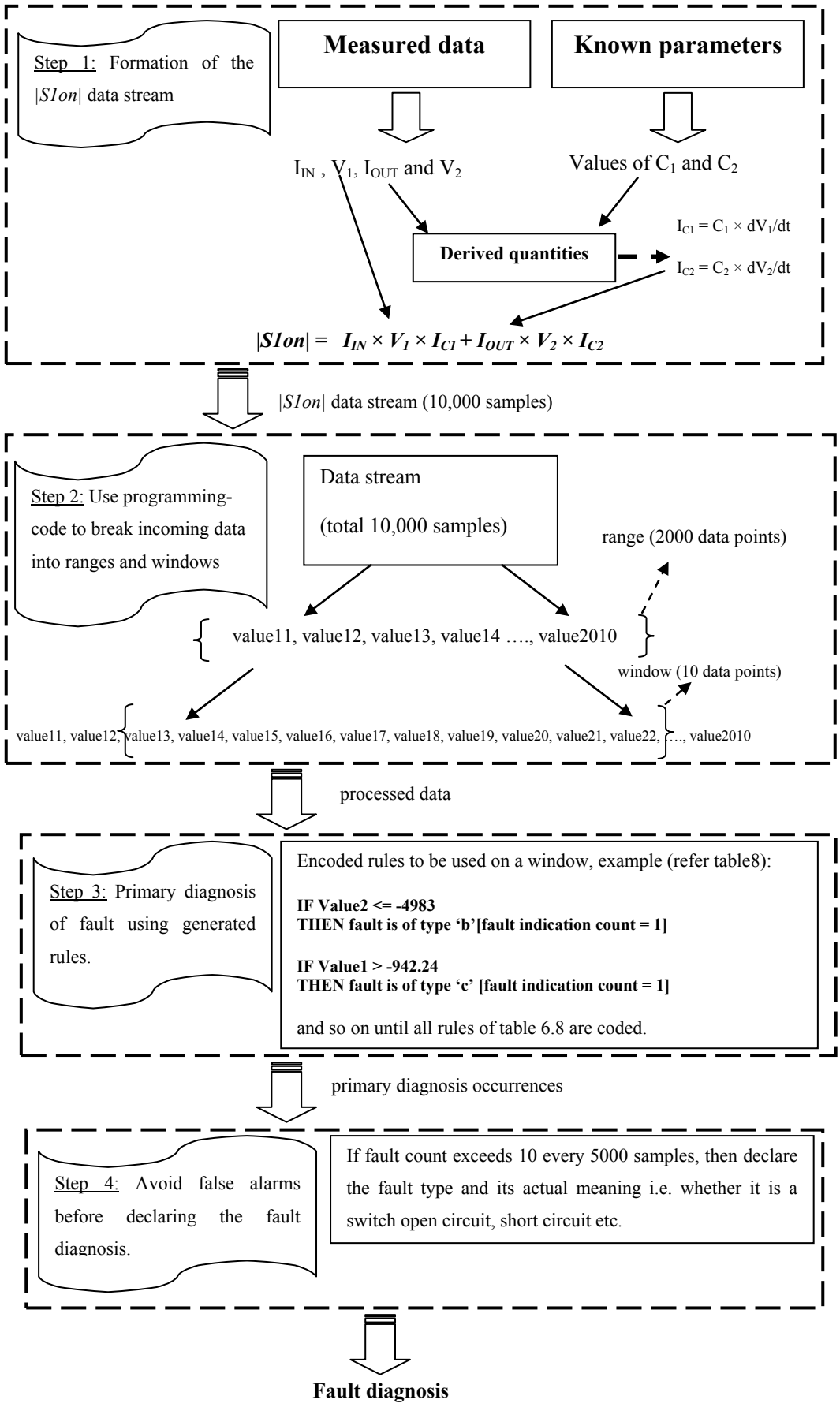


Figure 6.14: Example of encoding classifier results to test on a data stream

Operating scenario : Semiconductor switch (S_1) open circuit fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.3ms after fault introduction

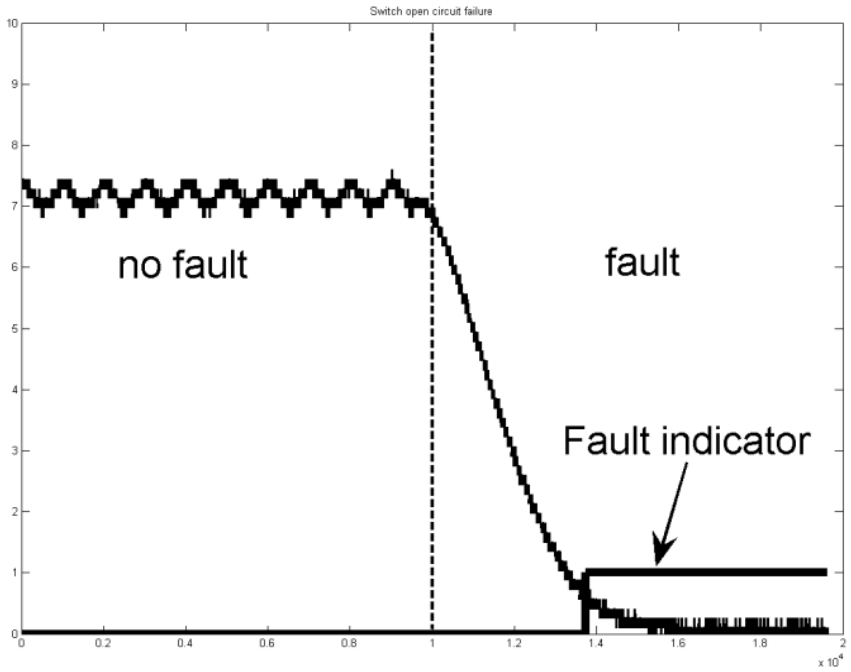


Table 6.9: Fault indication for switch open circuit fault case

Operating scenario : Semiconductor switch (S_1) short circuit fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.4ms after fault introduction

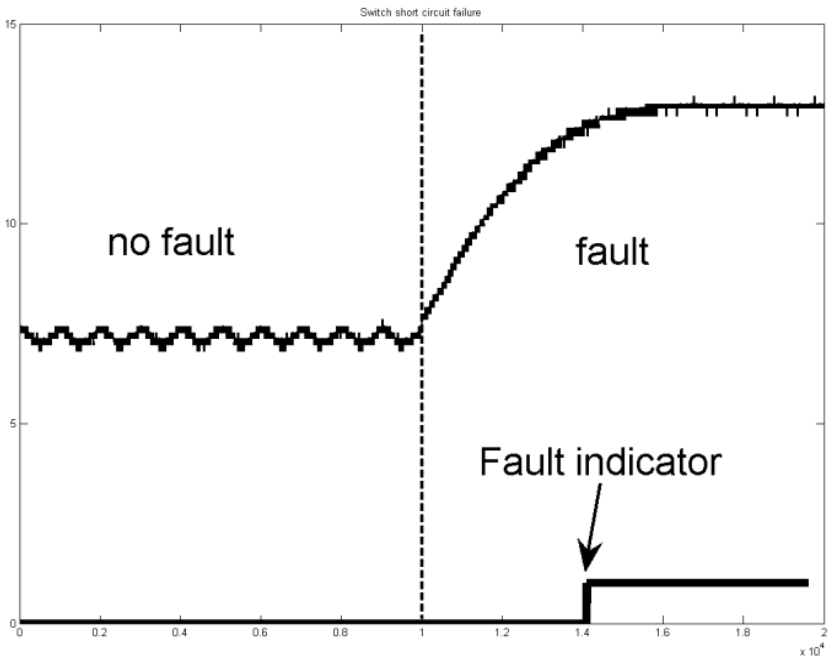


Table 6.10: Fault indication for switch short circuit fault case

Operating scenario : Inductor (L_1) fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.2ms after fault introduction

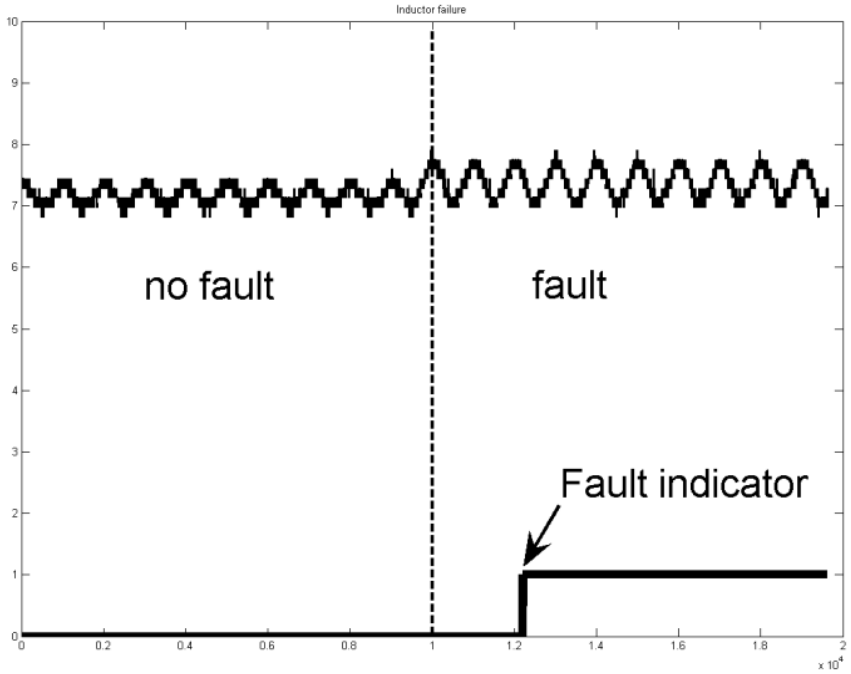


Table 6.11: Fault indication for inductor fault case

Operating scenario : Capacitor (C_2) fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.17ms after fault introduction

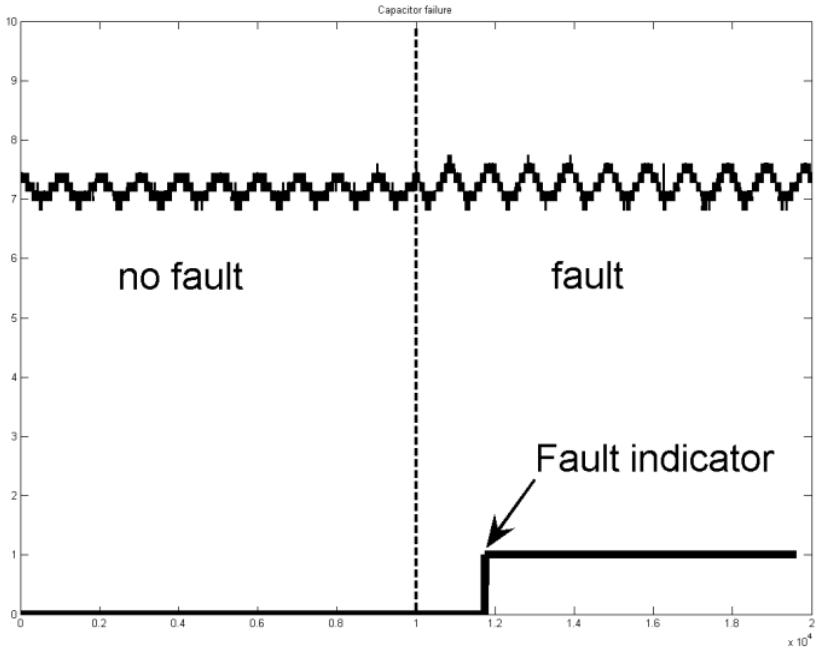


Table 6.12: Fault indication for capacitor fault case

a	b	c	d	e	f
1999	1	0	0	0	0
0	2000	0	0	0	0
0	0	2000	0	0	0
0	0	0	2000	0	0
0	0	0	0	2000	0
0	0	0	0	0	2000

Number of Rules generated: 20
Classification rate: 99.991%

(a) Hardware data

a	b	c	d	e	f
1999	0	0	0	1	0
0	2000	0	0	0	0
0	0	2000	0	0	0
0	0	0	1999	1	0
0	0	0	0	2000	0
0	0	0	0	0	2000

Number of Rules generated: 15
Classification rate: 99.983%

(b) Software data

a	b	c	d	e	f
1311	0	7	166	0	156
0	1801	0	89	32	78
0	0	2000	0	0	0
0	0	254	1215	165	366
0	0	57	1888	0	55
0	0	189	589	0	1222

Number of Rules generated: 15
Classification rate: 62.908%

(c) Hardware data trained on software rules

where; a = no fault data, b = switch short circuit fault data, c = switch open circuit fault data, d = inductor fault data, e = capacitor fault data, f = inductor & capacitor fault data.

Figure 6.15: (a) Confusion matrix for |*S1on*| equation for hardware circuit data (b) Confusion matrix for |*S1on*| equation for SIMULINK circuit data (c) Confusion matrix for |*S1on*| equation to check performance of software rules on hardware data

Table 6.13 lists the rule for each type of data per operational scenario. The rules generated are clubbed together according to the type of data differentiated. Table 6.13 also lists the total number of rules generated. Since the hardware data is tested on the rules derived from software data, the number of rules for these two cases is identical with appropriate adjustments based on the training operation. Other factors mentioned before for this Weka train-test process such as the 10-fold cross validation, algorithm used (PART) remain identical as mentioned before.

The real time testing of rules on hardware data in the previous section is achieved by comparing output voltage with the fault indicator (tables 6.9-6.12). In this case, input current is used for comparison to offer a different view (tables 6.14-6.18) than previously. Tables 6.14-6.18 show when the fault is introduced and the time it is indicated using the diagnostic scheme. Furthermore, in this case, the inductor and capacitor multiple fault case is also shown in table 6.18. Here as before, the data is 2ms long with an identical sampling rate as mentioned before.

Operational case	Software data (15rules)	Hardware data (20 rules)	Hardware data trained on rules from software data (15 rules)
No fault	Rule 1: Value1 <= -0.57784 AND Value1 <= -0.57979 AND Value1 > -0.6798 AND Value2 <= -0.57784 Rule 2: Value1 <= -0.57784 AND Value 1 > -0.61409	Rule 1: Value 1 <= -0.55753 AND Value 7 > -0.32158 AND Value 1 <= -0.64765 AND Value 1 > -0.68966 Rule 2: Value 1 <= -0.55753 AND Value 1 <= -0.72994 Rule 3: Value 2 <= -0.27426 AND Value 1 > -0.49804 AND Value 2 > -0.29346 Rule 4: Value 5 <= -0.1102 AND Value 2 > -0.19999 Rule 5: Value 2 <= -0.12784 AND Value 2 > -0.23824	Rule 1: Value1 <= -0.57784 AND Value1 <= -0.57979 AND Value1 > -0.6798 AND Value2 <= -0.57784 Rule 2: Value1 <= -0.57784 AND Value1 > -0.61409
Switch short circuit fault	Rule 1: Value4 <= -0.10681 AND Value 2 <= -0.72113	Rule 1: Value 6 <= -0.44085 Rule 2: Value 3 <= -0.23824	Rule 1: Value 4 <= -0.10681 AND Value 2 <= -0.72113
Switch open circuit fault	Rule 1: Value 1 > -0.25096	Rule 1: Value 3 > -0.011964	Rule 1: Value 1 > -0.25096
Inductor fault	Rule 1: Value 1 > -0.54284 AND Value 1 <= -0.52412 Rule 2: Value 1 <= -0.40546 AND Value 1 > -0.41725 Rule 3: Value 1 > -0.26333 Rule 4: Value 1 <= -0.4663	Rule 1: Value 1 <= -0.55753 AND Value 1 > -0.8654 AND Value 1 <= -0.64765 Rule 2: Value 1 <= -0.39083 AND Value 1 > -0.52735 Rule 3: Value 1 <= -0.23865 AND Value 1 > -0.25097 Rule 4: Value 2 > -0.12397 AND Value 1 > -0.12397	Rule 1: Value 1 > -0.54284 AND Value 1 <= -0.52412 Rule 2: Value 1 <= -0.40546 AND Value 1 > -0.41725 Rule 3: Value 1 > -0.26333 Rule 4: Value 1 <= -0.4663
Capacitor fault	Rule 1: Value 2 <= -0.213 AND Value 3 <= -0.19705 AND Value 8 > -0.12969 Rule 2: Value 1 <= -0.52735 AND Value 1 > -0.55753 Rule 3: Value 2 <= -0.12784 AND Value 2 > -0.24881 AND Value 1 > -0.31602 AND Value 1 > -0.25097 AND Value 1 <= -0.20344 Rule 4: Value 2 <= -0.23824 AND Value 1 <= -0.31602	Rule 1: Value 1 <= -0.3504	Rule 1: Value 4 <= -0.44672 AND Value 1 > -0.56454 Rule 2: Value 1 <= -0.40546
Inductor and capacitor fault	Rule 1: Value 1 > -0.2275	Rule 1: Value 1 > -0.49804 AND Value 8 <= -0.16211 Rule 2: Value 1 > -0.23865 AND Value 6 <= -0.10247 AND Value 1 <= -0.20344 Rule 3: Value 7 <= -0.26123 AND Value 8 <= -0.26123	Rule 1: Value 3 <= -0.54331 Rule 2: Value 1 <= -0.26333 AND Value 4 > -0.53028 AND Value 5 <= -0.37269 AND Value 9 <= -0.32954 Rule 3: Value 1 > -0.4663 AND Value 1 > -0.3715 AND Value 7 > -0.22899 Rule 4: Value 1 <= -0.37269

Table 6.13: Comparison of rules after training on software data and testing on hardware data

Operating scenario : Semiconductor switch (S_1) open circuit fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.35ms after fault introduction

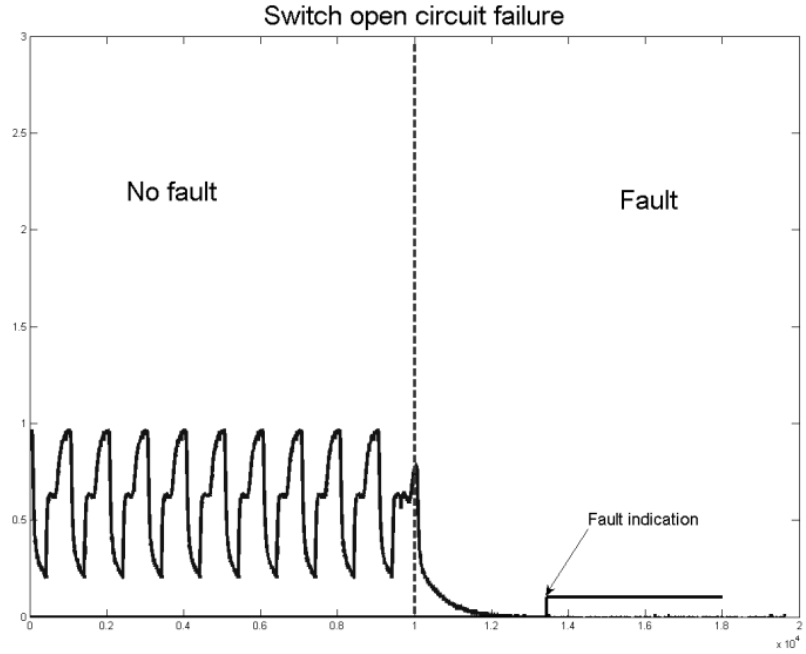


Table 6.14: Fault indication for switch open circuit fault case

Operating scenario : Semiconductor switch (S_1) short circuit fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.04ms after fault introduction

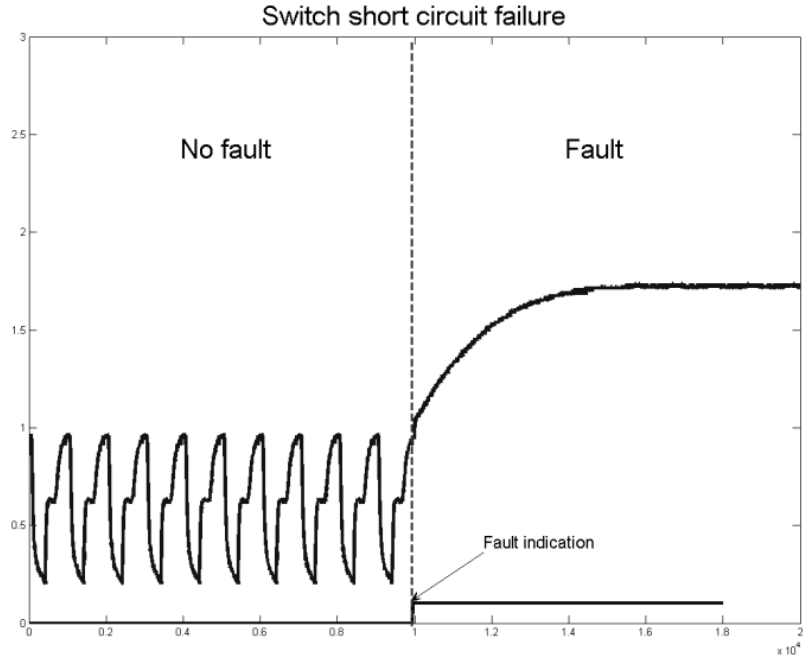


Table 6.15: Fault indication for switch short circuit fault case

Operating scenario : Inductor (L_1) fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.65ms after fault introduction

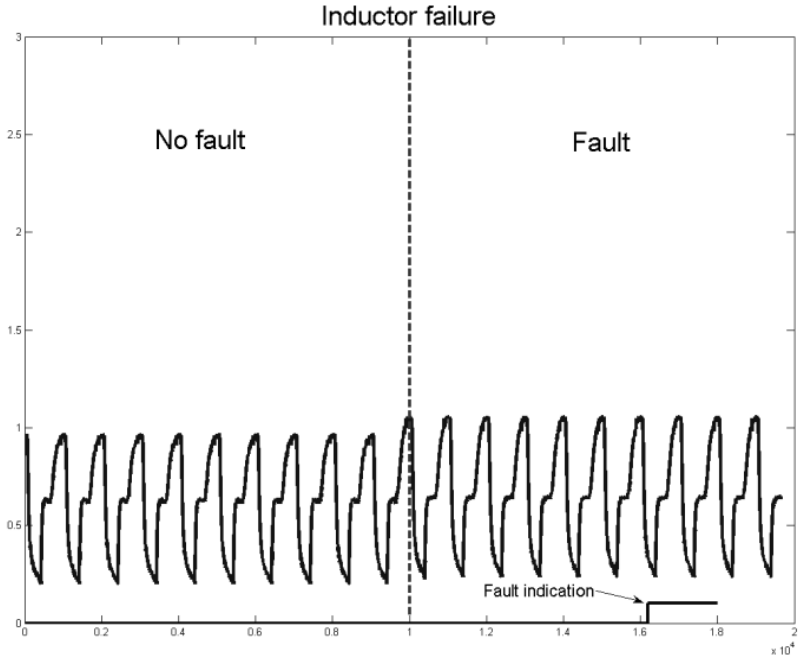


Table 6.16: Fault indication for inductor fault case

Operating scenario : Capacitor (C_2) fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.27ms after fault introduction

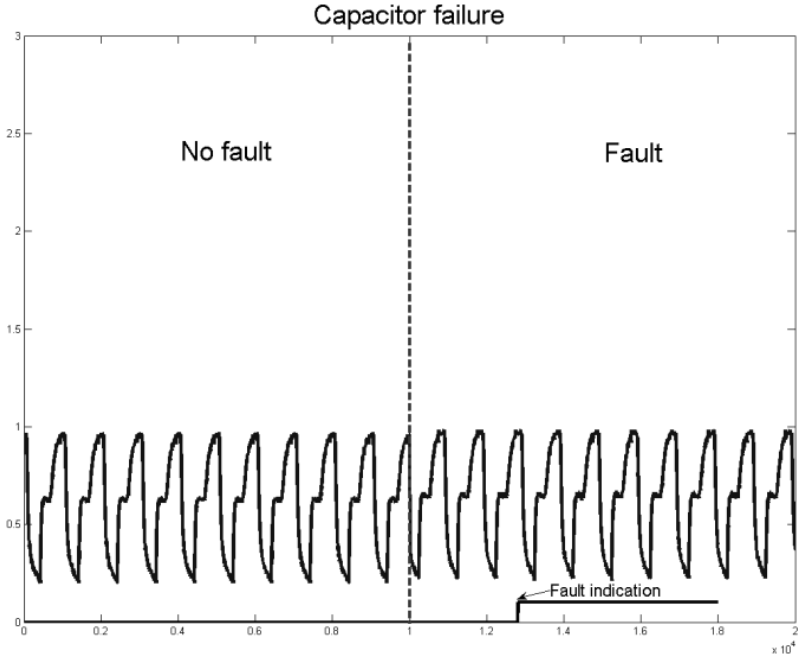


Table 6.17: Fault indication for capacitor fault case

Operating scenario : Inductor (L_1) and capacitor (C_2) fault case
x axis: Time in ns (10×10^5ns)
y axis: General unit to numerically show current in mA and voltage in V

Continuous fault indication approximately 0.22ms after fault introduction

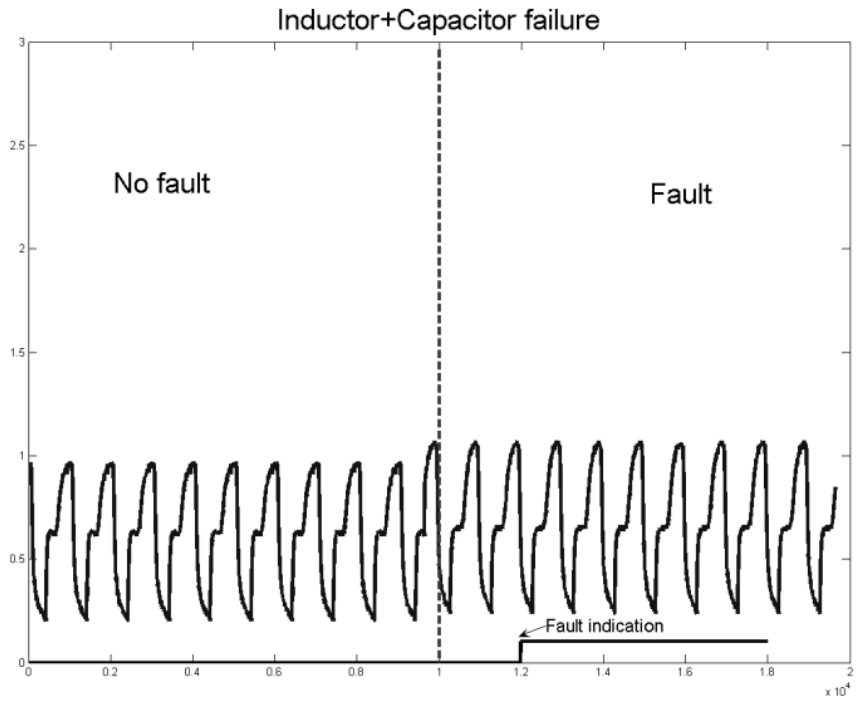


Table 6.18: Fault indication for capacitor fault case

The testing of software rules trained on hardware data as mentioned achieves the important goal of testing simulations to predict actual scenarios. The encapsulation of generated rules into conditional statements (IF-THEN-ELSE) and employing the aforementioned sample-counting method to avoid false alarms is identical to the procedure mentioned in sub-section 6.3.4 and illustrated in fig. 6.14. Ideally, the classification rate should be nearer 100%, but even with a rate of 62%, when the rules are tested, they are able to indicate a fault while differentiating the operational scenarios from each other, which is a promising outcome.

Another important observation about the results in table 6.15(c) is that there are no false negatives. In other words, the heuristics do not indicate there is a fault when the system is operating without a fault. There are crossovers and mis-classifications among fault-cases (which could be termed false positives), but there is no false negative which may be desirable outcome.

This feasibility check was carried out for the 50% duty cycle operation for the buck converter which is a special case. The same work could be carried out for a

range of duty cycles wherein matching software and hardware circuits are used to generate heuristics which in turn are compared by training and testing within Weka as shown. In the next section, a range of duty cycles are used to generate no-fault and fault data using the same SIMULINK circuit used before. This data is used to generate individual set of rules for the respective duty cycle which is then compared with other rule-sets to assess the ability of the classifier to generalise over variations in thresholds.

6.4 Generation of rules for different duty cycles of buck converter

This section looks at results of studies over a wider range of duty cycles. The attempt is to assess if heuristics arising from a specific duty cycle's data set could be generalised over data for various other duty cycle values.

6.4.1 Heuristics for duty cycles ranging from 10% to 95%

The sample analysis mainly elaborated in this chapter is the special case of 50% duty cycle for the standard buck converter circuit. More data could be produced using the same SIMULINK circuit by changing the duty cycle to values other than 50%. Since the voltage source in the circuit is ideal, the |*S1on*| and |*S1off*| equations would produce the same result because the additional term (I_{C1},= $C_1 \times dV_{IN}/dt = 0$) in the |*S1on*| equation would be zero. An identical study was carried out with duty cycle values mentioned in table 6.19 to generate sets of rules to distinguish the 5 type of faults discussed earlier. The total data thus generated was for 6 operational states for 5 duty cycles producing 30 individual streams of the |*S1off*| equation.

Test no.	Duty cycle (δ)	Equation used
1.	10%	$\|S1off\| = V_2 \times I_{OUT} \times I_{C2}$
2.	25%	$\|S1off\| = V_2 \times I_{OUT} \times I_{C2}$
3.	40%	$\|S1off\| = V_2 \times I_{OUT} \times I_{C2}$
4.	75%	$\|S1off\| = V_2 \times I_{OUT} \times I_{C2}$
5.	95%	$\|S1off\| = V_2 \times I_{OUT} \times I_{C2}$

Table 6.19: Different duty cycles for further tests

Like before, Weka was used to classify the data employing the PART algorithm. There are two logical practical applications that arise,

1. Rule scheduler – Depending on the particular duty cycle, the respective set of rules could be used to distinguish operational states.
2. Generalised rule set – A set of rules encompassing the entire range of duty cycles. Although in theory this would need to be done across smaller steps (for example every 1-5% steps of δ), it may provide a more compact way for automated diagnosis if a global set of heuristics could be derived.

In this subsection, tables listing rules for the five other duty cycles are displayed where symbols 'a' to 'f' are to indicate different operational states like in earlier cases. The tables display rules generated for different values of duty cycle and 6 operational states including the no fault case. Fig.6.16 shows the confusion matrix for the six operational cases.

a	b	c	d	e	f
1998	0	2	0	0	0
0	2000	0	0	0	0
0	0	2000	0	0	0
4	0	0	1974	0	22
0	1	0	2	1994	3
7	0	2	36	0	1955

Number of Rules generated: 39
Classification rate: 99.3417%

where; a = no fault data (nf_d10), b = switch short circuit fault data (S1sh_d10), c = switch open circuit fault data (S1op_d10), d = inductor fault data (L1f_d10), e = capacitor fault data (C2f_d10), f = inductor & capacitor fault data (L1C2f_d10).

Figure 6.16: Confusion matrix for duty cycle 10% using |S1off| equation for SIMULINK

Table 6.20 shows the various rules generated for the 10% duty cycle case. The abbreviations used here are indicative of the type of data and the duty cycle for example, no fault 10% duty cycle case is abbreviated as nf_d10. Other abbreviations used can be seen in fig.6.16.

Rules 1-8	Rules 9-16	Rules 17-24	Rules 25-32	Rules 33-39
IF Value9 > 0.024119 AND Value8 > 1.272801 THEN data is of type S1sh_d10 (2000.0)	IF Value8 <= -0.000057 AND Value7 > -0.004096 AND Value1 <= 0.000257 AND Value8 <= -0.004119 AND Value1 > -0.002498 THEN data is of type L1f_d10 (78.0)	IF Value7 > 0.003226 AND Value9 > 0.005343 AND Value1 <= 0.00316 THEN data is of type L1C2f_d10 (170.0)	IF Value9 > 0.001296 AND Value1 > 0.000417 AND Value2 > 0.000981 AND Value7 > 0.000918 AND Value8 > 0.002092 AND Value1 <= 0.004508 AND Value7 <= 0.003568 THEN data is of type L1f_d10 (41.0)	IF Value7 <= -0.004634 AND Value1 <= -0.0016 THEN data is of type L1C2f_d10 (23.0)
IF Value7 > 0.039569 THEN data is of type C2f_d10 (1196.0)	IF Value10 <= -0.000017 AND Value7 > -0.004096 AND Value1 <= 0.000231 AND Value2 <= -0.001154 AND Value9 > -0.004162 AND Value7 <= -0.001163 AND Value8 <= -0.001246 THEN data is of type nf_d10 (879.0/5.0)	IF Value7 <= -0.001265 AND Value2 > 0.000295 AND Value2 <= 0.012152 THEN data is of type L1C2f_d10 (77.0)	IF Value8 > -0.001246 AND Value9 <= 0.001296 AND Value7 <= 0.001357 AND Value9 <= 0.000722 AND Value1 <= 0.000732 AND Value7 > -0.001356 AND Value3 <= 0.000688 AND Value1 <= -0.000008 AND Value9 <= -0.000027 THEN data is of type nf_d10 (204.0)	IF Value8 <= -0.003544 AND Value1 <= -0.001187 THEN data is of type L1f_d10 (13.0)
IF Value9 <= -0.008635 AND Value8 > -0.014928 THEN data is of type L1C2f_d10 (870.0)	IF Value10 <= 0.000003 AND Value10 > -0.000017 THEN data is of type S1op_d10 (2002.0/2.0)	IF Value9 <= -0.001246 AND Value7 <= -0.004522 AND Value2 <= 0.012152 AND Value1 > -0.001977 THEN data is of type L1C2f_d10 (74.0)	IF Value7 <= -0.000031 AND Value2 <= 0.012152 AND Value2 <= 0.000673 AND Value2 > -0.000931 AND Value2 > -0.000443 THEN data is of type L1f_d10 (27.0)	IF Value9 <= 0.001296 AND Value8 > 0.00081 THEN data is of type nf_d10 (66.0)
IF Value1 <= -0.006853 THEN data is of type C2f_d10 (796.0)	IF Value7 <= -0.001265 AND Value7 <= -0.009712 AND Value1 <= -0.000024 THEN data is of type L1C2f_d10 (96.0/1.0)	IF Value7 > 0.003226 AND Value1 > 0.001578 AND Value1 <= 0.002612 THEN data is of type L1f_d10 (64.0)	IF Value1 <= -0.000046 AND Value10 > -0.001354 THEN data is of type L1C2f_d10 (34.0)	IF Value2 <= 0.004504 AND Value1 <= 0.001443 AND Value7 > 0.001184 THEN data is of type L1C2f_d10 (39.0/1.0)
IF Value7 > 0.00582 AND Value9 > 0.012345 THEN data is of type L1C2f_d10 (516.0)	IF Value2 > 0.003217 AND Value2 <= 0.005793 THEN data is of type nf_d10 (436.0)	IF Value7 <= -0.001265 AND Value1 > -0.000888 AND Value9 > -0.00221 THEN data is of type L1f_d10 (71.0)	IF Value7 <= -0.000031 AND Value2 <= 0.012152 AND Value2 > -0.000054 THEN data is of type L1C2f_d10 (19.0)	IF Value2 > 0.004504 AND Value2 > 0.014278 THEN data is of type C2f_d10 (7.0)
IF Value7 <= -0.004168 AND Value2 <= -0.000692 AND Value7 > -0.012279 AND Value7 <= -0.009628 AND Value10 <= -0.006432 THEN data is of type L1f_d10 (533.0)	IF Value7 <= -0.001265 AND Value1 <= -0.000226 AND Value10 > -0.008079 AND Value8 <= -0.001009 AND Value1 > -0.003217 AND Value10 <= -0.005453 THEN data is of type L1f_d10 (172.0)	IF Value7 > 0.003226 AND Value8 <= 0.003045 AND Value1 > 0.000177 AND Value7 > 0.005169 THEN data is of type L1f_d10 (78.0)	IF Value8 > -0.00003 AND Value9 <= 0.001296 AND Value7 <= 0.001357 AND Value2 <= 0.000857 AND Value10 <= 0.000862 THEN data is of type nf_d10 (135.0/1.0)	IF Value1 <= 0.004508 AND Value10 > 0.001594 AND Value10 <= 0.010322 THEN data is of type L1f_d10 (11.0)
IF Value7 > -0.000017 AND Value7 > 0.00582 AND Value1 > 0.002644	IF Value7 > 0.003226 AND Value8 <= 0.007834 AND Value1 > 0.002022 AND	IF Value8 > -0.001246 AND Value9 <= 0.003233 AND Value2 > 0.001294	IF Value2 <= 0.000857 AND Value10 > -0.007541 AND Value10 <= 0.002632	IF Value1 <= 0.004508 THEN data is of type L1C2f_d10 (5.0)

AND Value1 > 0.003213 THEN data is of type L1f_d10 (439.0/1.0)	Value3 <= 0.003202 THEN data is of type L1f_d10 (172.0)	THEN data is of type nf_d10 (283.0/1.0)	AND Value1 > -0.001588 AND Value2 <= 0.000814 THEN data is of type L1f_d10 (40.0)	
IF Value8 <= -0.000057 AND Value7 > -0.004096 AND Value7 > -0.000031 AND Value1 > -0.000993 AND Value1 <= 0.000665 THEN data is of type L1f_d10 (105.0)	IF Value7 <= -0.001265 AND Value1 <= -0.000226 AND Value1 > -0.002005 AND Value8 <= -0.002035 THEN data is of type L1f_d10 (134.0)	IF Value9 > 0.001296 AND Value8 > 0.003743 AND Value1 <= 0.002437 THEN data is of type L1C2f_d10 (43.0/1.0)	IF Value7 <= 0.000856 AND Value2 <= 0.012152 AND Value1 > -0.004039 AND Value8 > -0.008576 AND Value1 > -0.003324 AND Value8 > -0.006457 THEN data is of type L1C2f_d10 (50.0/17.0)	

Table 6.20: Rule set for duty cycle = 10%

Fig.6.17 shows the confusion matrix for the six operational cases for the 25% duty cycle operation and table 6.21 shows the corresponding rules.

a	b	c	d	e	f
1992	**0**	**0**	**2**	**5**	**1**
0	**2000**	**0**	**0**	**0**	**0**
2	**0**	**1998**	**0**	**0**	**0**
0	**0**	**0**	**1947**	**24**	**29**
33	**0**	**0**	**13**	**1938**	**16**
0	**2**	**0**	**41**	**32**	**1925**

Number of Rules generated: 92
Classification rate: 98.33%

where; a = no fault data (nf_d25), b = switch short circuit fault data (S1sh_d25), c = switch open circuit fault data (S1op_d25), d = inductor fault data (L1f_d25), e = capacitor fault data (C2f_d25), f = inductor & capacitor fault data (L1C2f_d25).

Figure 6.17: Confusion matrix for duty cycle 25% using |S1off| equation for SIMULINK

Rules 1-20	Rules 21-40	Rules 41-60	Rules 61-80	Rules 81-92
IF Value8 > 0.825866 THEN data is of type S1sh_d25 (2000.0)	IF Value7 > 0.117754 AND IF Value5 > 0.079534 AND IF Value7 <= 0.157055 THEN data is of type C2f_d25 (52.0)	IF Value7 > 0.081135 AND IF Value6 > 0.016561 AND IF Value1 > 0.041051 AND IF Value8 <= 0.12377 AND IF Value6 > 0.052374 THEN data is of type L1f_d25 (52.0/1.0)	IF Value5 <= -0.035628 AND Value8 > -0.091079 AND Value8 <= -0.034924 AND Value7 > -0.089327 AND Value5 <= -0.050784 AND Value8 <= -0.049741 AND Value5 > -0.074234 AND Value7 > -0.073842 THEN data is of type nf_d25 (134.0/6.0)	IF Value6 > 0.028992 AND IF Value5 > 0.045551 AND IF Value7 <= 0.07974 THEN data is of type C2f_d25 (7.0)
IF Value7 <= -0.263217 AND IF Value7 <= -0.425104 THEN data is of type L1C2f_d25 (728.0)	IF Value7 > 0.117754 AND IF Value5 > 0.079534 AND IF Value8 <= 0.218314 AND IF Value7 <= 0.212321 AND IF Value8 > 0.186365 THEN	IF Value8 <= -0.115291 AND IF Value6 <= -0.1081 AND Value8 > -0.277314 THEN data is of type C2f_d25 (34.0)	IF Value5 > 0.044893 AND IF Value7 > 0.044692 AND IF Value9 <= 0.079911 AND Value5 > 0.063003 THEN data is of type nf_d25 (78.0)	IF Value1 > 0.028828 AND IF Value9 > 0.014962 AND IF Value5 <= 0.046169 THEN data is of type L1C2f_d25 (39.0/1.0)

	data is of type C2f_d25 (48.0)			
IF Value7 > 0.206196 AND IF Value10 > 0.420141 THEN data is of type L1C2f_d25 (450.0)	IF Value7 > 0.117754 AND IF Value8 <= 0.123047 AND IF Value5 > 0.013213 AND IF Value8 <= 0.070628 THEN data is of type L1f_d25 (100.0)	IF Value7 <= -0.176737 AND IF Value8 <= -0.136783 AND IF Value7 > -0.337469 AND IF Value1 > -0.073825 THEN data is of type L1f_d25 (33.0)	IF Value9 > 0.062958 AND IF Value8 <= 0.063035 AND Value5 <= 0.040439 THEN data is of type L1f_d25 (24.0/1.0)	IF Value9 <= 0.014803 AND IF Value5 > 0.004502 AND IF Value7 > -0.050664 AND IF Value5 <= 0.023684 THEN data is of type C2f_d25 (54.0)
IF Value8 <= -0.008941 AND IF Value7 <= -0.164248 AND IF Value5 > -0.044485 AND IF Value7 <= -0.183843 THEN data is of type L1C2f_d25 (174.0)	IF Value7 > 0.117754 AND IF Value5 > 0.07885 AND IF Value8 <= 0.218314 AND IF Value7 > 0.182113 THEN data is of type L1f_d25 (64.0)	IF Value8 <= -0.167639 AND IF Value9 > -0.21728 AND Value6 <= -0.099896 THEN data is of type L1f_d25 (26.0)	IF Value9 > 0.063113 AND IF Value5 > 0.053616 THEN data is of type C2f_d25 (30.0)	IF Value1 <= -0.012698 AND IF Value8 > -0.052347 AND IF Value9 <= 0.034535 AND IF Value5 <= -0.035586 THEN data is of type C2f_d25 (30.0)
IF Value8 <= -0.008941 AND IF Value8 <= -0.164588 AND IF Value8 <= -0.256187 AND IF Value9 > -0.307922 AND IF Value7 <= -0.202151 THEN data is of type L1f_d25 (415.0/2.0)	IF Value8 <= -0.114595 AND IF Value9 > -0.115469 AND IF Value5 <= -0.011003 AND IF Value1 > -0.059376 THEN data is of type L1f_d25 (94.0)	IF Value7 > 0.081135 AND Value8 <= 0.087259 AND IF Value7 > 0.106373 THEN data is of type L1C2f_d25 (44.0)	IF Value7 > 0.063064 AND IF Value8 <= 0.069844 AND Value5 > -0.026785 AND Value5 <= 0.020384 THEN data is of type L1f_d25 (10.0)	IF Value9 <= -0.067859 AND IF Value1 > -0.087842 AND IF Value7 > -0.16572 THEN data is of type C2f_d25 (28.0/2.0)
IF Value7 > -0.008899 AND IF Value7 > 0.206196 AND IF Value6 > 0.109872 AND IF Value7 > 0.414901 THEN data is of type L1f_d25 (262.0)	IF Value7 > 0.117754 AND IF Value5 <= 0.091082 AND IF Value10 <= 0.192971 AND IF Value5 > 0.065499 AND IF Value8 <= 0.166756 THEN data is of type L1f_d25 (80.0)	IF Value8 > 0.079803 AND Value1 <= 0.043736 AND IF Value5 > 0.013622 THEN data is of type C2f_d25 (40.0/1.0)	IF Value7 <= -0.089132 AND Value7 <= -0.165213 AND Value1 <= -0.060431 THEN data is of type L1f_d25 (12.0)	IF Value7 <= -0.05041 AND IF Value1 <= 0.009343 AND IF Value1 > -0.048109 AND IF Value8 <= -0.006911 AND IF Value1 > -0.033677 THEN data is of type L1f_d25 (38.0)
IF Value7 > -0.008899 AND IF Value7 > 0.206196 AND IF Value6 > 0.109918 AND IF Value8 > 0.330035 THEN data is of type C2f_d25 (189.0)	IF Value8 > 0.117764 AND IF Value5 <= 0.07981 AND IF Value7 > 0.187943 THEN data is of type L1C2f_d25 (80.0)	IF Value10 > 0.081489 AND IF Value8 > 0.091393 AND Value7 <= 0.102774 THEN data is of type L1C2f_d25 (36.0)	IF Value5 <= -0.074234 AND Value5 > -0.094079 THEN data is of type nf_d25 (84.0)	IF Value7 <= -0.050785 AND IF Value8 > -0.089562 AND IF Value1 > -0.059376 THEN data is of type L1C2f_d25 (21.0)
IF Value10 <= -0.00005 AND IF Value7 <= -0.164248 AND IF Value7 > -0.263217 AND IF Value9 <= -0.18854 AND IF Value9 > -0.274141 THEN data is of type C2f_d25 (540.0)	IF Value7 <= -0.1148 AND IF Value6 > -0.007056 THEN data is of type L1C2f_d25 (40.0)	IF Value7 <= -0.114893 AND IF Value7 <= -0.178051 AND IF Value8 > -0.183107 THEN data is of type L1C2f_d25 (19.0)	IF Value7 <= -0.050664 AND Value6 <= 0.012996 AND Value9 <= -0.011533 AND Value6 > -0.014598 THEN data is of type C2f_d25 (63.0)	IF Value6 <= 0.018333 AND IF Value8 > 0.01232 AND IF Value5 > -0.005364 THEN data is of type C2f_d25 (11.0)
IF Value7 > -0.008899 AND IF Value7 > 0.206196 AND IF Value6 > 0.109872 AND IF Value7 <= 0.325068 AND IF Value8 > 0.267066	IF Value7 <= -0.1148 AND IF Value8 <= -0.253128 AND IF Value7 <= -0.162604 THEN data is of type L1C2f_d25 (27.0/1.0)	IF Value7 <= -0.114893 AND IF Value10 > -0.169945 AND IF Value10 <= -0.077418 AND IF Value7 > -0.158996 THEN data is of type C2f_d25	IF Value7 > -0.050664 AND Value8 <= -0.050668 AND Value1 > -0.032742 THEN data is of type L1f_d25 (18.0)	IF Value6 <= 0.018333 AND IF Value8 > 0.01232 AND IF Value9 <= 0.044331 AND IF Value5 > -0.018683 THEN data is of type C2f_d25

THEN data is of type C2f_d25 (130.0)		(53.0)		(10.0)
IF Value7 > -0.008899 AND IF Value7 > 0.206196 AND IF Value5 > 0.109862 AND IF Value7 > 0.263256 THEN data is of type L1f_d25 (159.0)	IF Value7 <= -0.1148 AND IF Value9 > -0.092023 AND IF Value1 > -0.047326 AND IF Value8 <= -0.052445 THEN data is of type L1f_d25 (58.0)	IF Value6 <= -0.034127 AND IF Value8 > -0.115296 AND IF Value8 <= -0.034143 AND IF Value7 > -0.115135 AND IF Value7 <= -0.034531 AND IF Value6 <= -0.088592 THEN data is of type nf_d25 (166.0)	IF Value7 > -0.050664 AND Value7 > 0.065755 AND Value8 <= 0.062547 THEN data is of type L1C2f_d25 (16.0/1.0)	IF Value8 <= 0.01232 AND IF Value1 <= 0.018125 AND IF Value7 > -0.044413 THEN data is of type L1f_d25 (26.0)
IF Value7 > -0.008899 AND IF Value8 > 0.20622 AND Value5 > 0.109862 AND IF Value3 > 0.118392 THEN data is of type C2f_d25 (81.0)	IF Value8 <= -0.114595 AND IF Value6 > -0.057862 THEN data is of type C2f_d25 (84.0)	IF Value7 <= -0.088358 AND IF Value9 <= -0.164848 AND IF Value9 <= -0.201918 THEN data is of type L1C2f_d25 (19.0)	IF Value7 > -0.050664 AND Value9 <= -0.015408 AND Value5 <= -0.007052 AND Value5 > -0.040087 THEN data is of type nf_d25 (126.0)	IF Value7 > -0.044368 THEN data is of type L1C2f_d25 (22.0)
IF Value7 > -0.008899 AND IF Value6 > 0.118376 THEN data is of type nf_d25 (402.0)	IF Value8 <= -0.115291 AND IF Value7 > -0.121356 AND IF Value8 <= -0.17988 AND IF Value10 > -0.140584 THEN data is of type L1f_d25 (19.0)	IF Value9 > 0.080093 AND Value10 > 0.114518 AND IF Value8 > 0.133853 AND Value1 <= 0.057709 THEN data is of type C2f_d25 (6.0)	IF Value7 > -0.050664 AND Value7 > -0.014882 AND Value8 <= 0.063666 AND Value5 <= 0.028993 AND Value9 <= 0.029088 AND Value5 > -0.015943 AND Value1 <= 0.019426 AND Value9 <= 0.020974 AND Value8 > -0.01605 THEN data is of type nf_d25 (174.0/2.0)	IF Value1 > -0.047636 THEN data is of type L1f_d25 (3.0)
IF Value10 <= -0.00005 AND IF Value8 <= -0.165006 AND IF Value10 > -0.303353 AND IF Value8 <= -0.187576 AND IF Value6 > -0.135968 AND IF Value9 > -0.250515 AND IF Value7 > -0.370908 AND IF Value7 <= -0.119811 AND IF Value7 > -0.316057 THEN data is of type L1f_d25 (129.0)	IF Value8 > 0.117764 AND IF Value5 > 0.076953 THEN data is of type C2f_d25 (78.0)	IF Value9 > 0.08305 AND Value10 <= 0.114518 AND IF Value5 > 0.020384 AND Value7 > 0.019331 AND Value7 <= 0.096937 THEN data is of type L1f_d25 (31.0)	IF Value7 > 0.019519 AND IF Value5 <= 0.014611 AND Value9 <= 0.070633 THEN data is of type C2f_d25 (23.0)	
IF Value10 <= -0.00005 AND IF Value8 <= -0.164588 AND IF Value8 > -0.187576 AND IF Value9 > -0.165077 AND IF Value7 <= -0.038668 THEN data is of type L1f_d25 (53.0/1.0)	IF Value8 <= -0.115291 AND IF Value7 > -0.119811 AND IF Value8 > -0.227067 THEN data is of type L1C2f_d25 (20.0)	IF Value7 <= -0.088358 AND IF Value5 <= 0.003001 AND IF Value9 > -0.042724 AND IF Value1 > -0.027606 THEN data is of type L1f_d25 (17.0)	IF Value7 > 0.019519 AND IF Value8 <= 0.019288 AND Value1 <= 0.02796 THEN data is of type L1f_d25 (6.0)	
IF Value10 <= -0.00005 AND IF Value7 <= -0.164248 AND IF Value8 > -0.304111 AND IF Value7 > -0.20391 AND IF Value9 <= -0.122619 THEN data is of type	IF Value8 <= -0.115291 AND IF Value8 <= -0.253128 AND IF Value1 <= -0.12201 THEN data is of type L1f_d25 (25.0)	IF Value7 <= -0.088358 AND IF Value5 <= 0.003001 AND IF Value6 > -0.031071 THEN data is of type C2f_d25 (51.0)	IF Value7 > 0.019519 AND IF Value8 > 0.019288 AND IF Value8 <= 0.06444 AND IF Value5 <= 0.036352 AND Value7 <= 0.039092 THEN data is of type nf_d25 (78.0)	

C2f_d25 (116.0)				
IF Value10 <= -0.00005 AND IF Value8 <= -0.166764 AND IF Value10 > -0.303353 AND IF Value1 > -0.122719 AND IF Value9 > -0.244254 AND IF Value6 <= -0.1081 THEN data is of type L1f_d25 (49.0)	IF Value7 > 0.117754 AND IF Value8 > 0.120024 AND IF Value10 <= 0.188533 AND IF Value3 > 0.033983 THEN data is of type C2f_d25 (43.0)	IF Value8 <= -0.088632 AND IF Value10 <= -0.180728 AND IF Value6 > -0.098548 THEN data is of type L1C2f_d25 (10.0)	IF Value7 > 0.036402 AND IF Value8 > 0.034421 AND IF Value7 <= 0.065473 AND Value5 <= 0.055475 AND Value8 <= 0.055267 AND Value5 > 0.044695 AND IF Value7 > 0.044325 THEN data is of type nf_d25 (54.0/6.0)	
IF Value10 <= -0.00005 AND IF Value6 <= -0.071102 AND IF Value8 > -0.165625 AND IF Value7 > -0.164702 AND IF Value6 <= -0.114766 THEN data is of type nf_d25 (416.0)	IF Value7 > 0.117754 AND IF Value8 > 0.096946 THEN data is of type L1C2f_d25 (42.0)	IF Value8 <= -0.088632 AND IF Value7 > -0.091443 AND IF Value7 <= 0.053625 AND IF Value1 > -0.100315 THEN data is of type L1f_d25 (34.0)	IF Value6 <= 0.055479 AND Value6 <= -0.040185 AND Value7 > -0.050664 AND Value8 <= -0.040204 THEN data is of type nf_d25 (57.0/1.0)	
IF Value7 <= -0.008899 AND IF Value10 > -0.000267 AND IF Value9 <= 0.000305 THEN data is of type S1op_d25 (2000.0)	IF Value6 > 0.080162 THEN data is of type nf_d25 (172.0)	IF Value7 <= -0.088452 AND IF Value8 > -0.082742 AND IF Value1 > -0.054635 THEN data is of type L1C2f_d25 (25.0)	IF Value7 > 0.036402 AND Value8 > 0.034421 AND Value8 <= 0.064928 AND Value5 <= 0.044695 THEN data is of type nf_d25 (38.0)	
IF Value7 > 0.117754 AND IF Value9 > 0.26076 THEN data is of type L1C2f_d25 (165.0)	IF Value6 <= 0.065835 AND IF Value8 <= 0.083041 AND IF Value3 > -0.02882 AND IF Value8 <= -0.020809 THEN data is of type L1f_d25 (50.0)	IF Value9 > 0.080093 AND Value8 > 0.073521 AND Value9 > 0.08305 THEN data is of type L1C2f_d25 (17.0)	IF Value6 <= 0.055479 AND Value6 > 0.026171 AND Value7 > -0.021198 AND Value8 > 0.000877 AND Value10 <= 0.06611 AND Value7 <= 0.043194 AND Value8 > 0.015679 THEN data is of type C2f_d25 (59.0)	
IF Value7 > 0.117754 AND IF Value5 > 0.07885 AND Value7 > 0.256151 THEN data is of type L1f_d25 (76.0)	IF Value9 > 0.079911 AND IF Value3 > 0.065555 THEN data is of type C2f_d25 (47.0)	IF Value7 <= -0.088452 AND IF Value7 > -0.226927 AND IF Value1 <= -0.067408 THEN data is of type C2f_d25 (18.0)	IF Value6 > 0.055479 THEN data is of type nf_d25 (36.0)	

Table 6.21: Rule set for duty cycle = 25%

Fig.6.18 shows the confusion matrix for the six operational cases for the 40% duty cycle operation and table 6.22 shows the corresponding rules.

a	b	c	d	e	f
1983	0	0	2	14	1
0	2000	0	0	0	0
2	0	1998	0	0	0
3	0	0	1931	32	34
39	0	0	15	1927	19
3	2	0	54	25	1916

Number of Rules generated: 98
Classification rate: 97.95%

where; a = no fault data (nf_d40), b = switch short circuit fault data (S1sh_d40), c = switch open circuit fault data (S1op_d40), d = inductor fault data (L1f_d40), e = capacitor fault data (C2f_d40), f = inductor & capacitor fault data (L1C2f_d40).

Figure 6.18: Confusion matrix for duty cycle 40% using |S1off| equation for SIMULINK

Rules 1-20	Rules 21-40	Rules 41-60	Rules 61-80	Rules 81-98
IF Value8 > 3.164686 THEN data is of type S1sh_d40 (2000.0)	IF Value7 > 0.580399 AND Value8 <= 0.591553 AND Value5 > 0.085629 AND Value8 <= 0.410465 THEN data is of type L1f_d40 (113.0)	IF Value8 > 0.41385 AND Value7 > 0.698135 AND Value1 <= 0.311544 THEN data is of type L1C2f_d40 (14.0)	IF Value7 <= -0.309833 AND Value9 <= -0.185258 AND Value7 > -0.526874 AND Value9 <= -0.245643 THEN data is of type C2f_d40 (74.0/1.0)	IF Value9 <= -0.042289 AND Value6 <= -0.009315 AND Value6 > -0.18131 AND Value6 > -0.138256 THEN data is of type nf_d40 (124.0)
IF Value8 <= -0.708187 AND Value9 <= -1.384841 THEN data is of type L1C2f_d40 (606.0)	IF Value7 > 0.580399 AND Value1 <= 0.215133 AND Value8 > -0.024249 THEN data is of type L1C2f_d40 (115.0)	IF Value8 > 0.41385 AND Value9 > 0.517918 AND Value8 > 0.505115 AND Value7 > 0.421278 AND Value7 <= 0.702912 AND Value9 <= 0.687434 THEN data is of type C2f_d40 (98.0)	IF Value7 <= -0.309833 AND Value8 > -0.329429 AND Value1 > -0.215508 THEN data is of type L1C2f_d40 (32.0)	IF Value7 > -0.040882 AND Value6 <= -0.042241 AND Value8 <= 0.164687 THEN data is of type C2f_d40 (32.0)
IF Value7 > -0.087032 AND Value9 > 1.582953 THEN data is of type L1C2f_d40 (479.0)	IF Value10 > 0.580621 AND Value8 <= 0.578847 AND Value5 > 0.264606 THEN data is of type L1f_d40 (70.0)	IF Value8 <= -0.537396 AND Value4 <= -0.382248 THEN data is of type L1f_d40 (27.0)	IF Value5 > 0.303918 AND Value7 <= 0.489687 THEN data is of type nf_d40 (138.0)	IF Value7 > -0.040882 AND Value9 <= 0.184738 AND Value8 > -0.039942 AND Value1 <= 0.095418 AND Value8 <= 0.118105 AND Value9 <= 0.099805 AND Value9 <= 0.08942 THEN data is of type nf_d40 (166.0)
IF Value7 > -0.087032 AND Value7 > 0.78382 AND Value4 > 0.439667 AND Value7 > 1.526026 THEN data is of type L1f_d40 (249.0)	IF Value6 <= -0.501421 AND Value7 > -0.747521 THEN data is of type nf_d40 (346.0)	IF Value8 <= -0.537396 AND Value7 <= 0.067359 AND Value9 > -0.731877 AND Value8 <= -0.618109 AND Value9 > -0.598465 THEN data is of type L1f_d40 (27.0)	IF Value9 > 0.301954 AND Value8 <= 0.299786 AND Value2 <= 0.178493 AND Value1 > 0.050981 THEN data is of type L1f_d40 (26.0)	IF Value7 > 0.089628 AND Value5 <= 0.089224 AND Value8 > 0.103759 THEN data is of type C2f_d40 (43.0)
IF Value10 <= -0.000946 AND Value8 <= -0.708187 AND Value2 <= -0.224068 AND Value8 <= -1.209416 AND	IF Value8 <= -0.500546 AND Value7 > -0.49972 AND Value1 > -0.227101 THEN data is of type L1f_d40 (57.0)	IF Value6 <= -0.391435 THEN data is of type nf_d40 (158.0)	IF Value9 > 0.301954 AND Value7 > 0.199616 AND Value9 <= 0.414476 AND Value8 > 0.30656 THEN data is of type C2f_d40 (66.0)	IF Value7 > 0.089628 AND Value5 > 0.184873 AND Value7 > 0.231328 AND Value8 <= 0.301919 AND Value5 > 0.252485 THEN data

Value3 <= -0.500257 THEN data is of type L1f_d40 (288.0)				is of type nf_d40 (64.0)
IF Value7 > -0.087032 AND Value7 > 0.78382 AND Value4 > 0.439886 AND Value8 > 1.329325 THEN data is of type C2f_d40 (132.0)	IF Value7 <= -0.500076 AND Value6 <= -0.04763 AND Value8 <= -0.874698 AND Value7 <= -0.692804 THEN data is of type L1f_d40 (83.0)	IF Value7 <= -0.392387 AND Value6 > -0.025991 THEN data is of type L1C2f_d40 (61.0)	IF Value9 > 0.302242 AND Value5 > 0.264402 AND Value8 <= 0.64441 THEN data is of type L1f_d40 (18.0)	IF Value7 > 0.089628 AND Value5 <= 0.184873 AND Value9 <= 0.184738 AND Value8 > 0.073815 THEN data is of type nf_d40 (120.0)
IF Value7 > -0.087032 AND Value7 > 0.78382 AND Value4 > 0.439667 AND Value7 <= 1.321558 AND Value8 > 1.17506 THEN data is of type C2f_d40 (98.0)	IF Value7 <= -0.500076 AND Value6 <= -0.04763 AND Value9 <= -0.456748 AND Value7 > -0.899471 AND Value8 > -1.179159 AND Value9 <= -0.540415 THEN data is of type C2f_d40 (235.0)	IF Value9 <= -0.391355 AND Value8 <= -0.537396 AND Value7 > -0.10781 THEN data is of type L1C2f_d40 (30.0)	IF Value9 > 0.302242 AND Value5 <= 0.271208 AND Value7 <= 0.214006 THEN data is of type L1C2f_d40 (18.0)	IF Value9 <= -0.136955 AND Value5 > -0.185048 AND Value5 <= -0.057876 THEN data is of type nf_d40 (56.0)
IF Value7 > -0.087032 AND Value7 > 0.78382 AND Value5 > 0.439662 AND Value7 > 1.16444 THEN data is of type L1f_d40 (113.0)	IF Value10 > 0.580621 AND Value1 > 0.3483 AND Value8 > 0.95229 THEN data is of type C2f_d40 (62.0)	IF Value7 <= -0.392387 AND Value7 <= -0.685717 AND Value1 > -0.21851 THEN data is of type L1f_d40 (18.0)	IF Value8 <= -0.309795 AND Value1 > -0.213554 THEN data is of type L1f_d40 (29.0)	IF Value5 > 0.183961 AND Value7 > 0.231328 AND Value8 <= 0.25299 AND Value5 > 0.231503 THEN data is of type nf_d40 (26.0)
IF Value10 <= -0.000946 AND Value7 <= -0.70758 AND Value6 > -0.250984 AND Value9 <= -0.501647 THEN data is of type L1C2f_d40 (172.0)	IF Value10 > 0.580621 AND Value1 > 0.3483 AND Value7 <= 0.943973 AND Value3 > 0.462599 THEN data is of type C2f_d40 (50.0)	IF Value9 <= -0.391355 AND Value7 > -0.73587 AND Value8 > -0.779058 THEN data is of type C2f_d40 (100.0)	IF Value7 > 0.305278 AND Value5 <= 0.271208 AND Value7 <= 0.52398 AND Value8 <= 0.545258 THEN data is of type L1f_d40 (42.0/10.0)	IF Value5 <= 0.183961 AND Value9 <= 0.08077 AND Value6 > 0.027539 AND Value6 <= 0.105489 THEN data is of type C2f_d40 (49.0)
IF Value7 > -0.087032 AND Value7 > 0.78382 AND Value5 > 0.43988 AND Value8 > 1.051291 THEN data is of type C2f_d40 (78.0)	IF Value8 <= -0.534982 AND Value4 <= -0.4918 AND Value7 <= -0.768338 THEN data is of type C2f_d40 (13.0)	IF Value8 <= -0.391416 AND Value1 > -0.199713 THEN data is of type L1f_d40 (54.0)	IF Value6 <= -0.12298 AND Value7 > -0.311006 AND Value8 <= -0.121115 AND Value4 <= -0.181022 AND Value10 <= -0.180625 AND Value2 > -0.269063 AND Value7 > -0.26903 THEN data is of type nf_d40 (125.0/9.0)	IF Value5 <= 0.183961 AND Value9 <= 0.08077 AND Value8 > -0.04766 AND Value8 > -0.025006 THEN data is of type C2f_d40 (46.0)
IF Value10 <= -0.000946 AND Value7 <= -0.70758 AND Value1 <= -0.585772 THEN data is of type C2f_d40 (217.0)	IF Value8 <= -0.535847 AND Value10 > -0.94076 AND Value7 <= 0.158731 AND Value4 > -0.382248 AND Value9 > -0.626372 AND Value4 <= -0.107126 AND Value3 > -0.269054 THEN data is of type L1f_d40 (46.0)	IF Value8 <= -0.39409 AND Value8 <= -0.499802 AND Value1 <= -0.227101 AND Value8 <= -0.675359 AND Value9 > -0.733399 AND Value7 > -1.138192 THEN data is of type L1f_d40 (17.0/2.0)	IF Value1 > 0.144072 AND Value7 <= 0.145066 AND Value7 > -0.008091 AND Value8 > 0.085474 THEN data is of type C2f_d40 (30.0)	IF Value5 <= 0.183961 AND Value1 > -0.01535 AND Value3 <= 0.108499 THEN data is of type L1f_d40 (67.0/1.0)
IF Value7 > -0.087032 AND Value7 > 0.78382 AND Value8 > 1.05206 THEN data is of type L1C2f_d40 (146.0)	IF Value9 > 0.580553 AND Value1 > 0.3483 AND Value9 > 0.693863 AND Value7 <= 0.938403 AND Value8 > 0.821397 AND Value3 <= 0.432861 THEN data is of type C2f_d40 (46.0)	IF Value7 > 0.412811 AND Value5 > -0.087553 AND Value8 <= 0.418217 AND Value1 <= 0.154669 THEN data is of type L1f_d40 (67.0)	IF Value1 > 0.144072 AND Value7 <= 0.145066 AND Value9 > 0.105637 THEN data is of type L1C2f_d40 (17.0)	IF Value5 > 0.183961 THEN data is of type C2f_d40 (41.0)

IF Value7 > -0.087032 AND Value5 > 0.581669 THEN data is of type nf_d40 (254.0)	IF Value8 <= -0.537396 AND Value10 <= -0.94076 THEN data is of type L1C2f_d40 (27.0)	IF Value7 <= -0.392566 AND Value6 > -0.146032 AND Value9 > -0.315455 THEN data is of type L1f_d40 (34.0)	IF Value6 > 0.14881 AND Value9 <= 0.302242 AND Value5 <= 0.255492 AND Value8 <= 0.254061 AND Value8 > 0.143497 AND Value10 <= 0.254115 AND Value5 > 0.184873 AND Value7 > 0.187025 AND Value5 <= 0.231503 AND Value8 <= 0.230374 THEN data is of type nf_d40 (61.0/5.0)	IF Value4 <= -0.111173 AND Value1 > -0.211791 THEN data is of type C2f_d40 (24.0)
IF Value10 <= -0.000946 AND Value8 <= -0.708187 AND Value7 <= -1.132733 AND Value7 > -1.613243 AND Value3 <= -0.417443 THEN data is of type L1f_d40 (115.0)	IF Value7 > 0.580399 AND Value1 > 0.3483 AND Value9 > 0.766841 THEN data is of type L1f_d40 (80.0/1.0)	IF Value8 <= -0.39409 AND Value1 <= -0.227101 THEN data is of type L1C2f_d40 (36.0)	IF Value10 > 0.408117 AND Value5 <= 0.271208 THEN data is of type L1C2f_d40 (16.0)	IF Value9 > 0.232438 AND Value1 > 0.03642 AND Value1 <= 0.153323 THEN data is of type L1f_d40 (18.0)
IF Value10 <= -0.000946 AND Value8 <= -0.708187 AND Value9 > -0.711076 AND Value7 <= 0.010659 AND Value7 > -1.12534 THEN data is of type L1f_d40 (106.0)	IF Value10 > 0.580621 AND Value10 <= 0.820889 AND Value5 > 0.285776 AND Value8 > 0.661579 THEN data is of type C2f_d40 (69.0)	IF Value9 > 0.412917 AND Value8 <= 0.41385 AND Value1 <= 0.220841 AND Value7 <= 0.434799 AND Value7 > 0.224958 THEN data is of type L1f_d40 (18.0)	IF Value6 <= -0.269856 THEN data is of type nf_d40 (57.0/1.0)	IF Value8 > -0.137122 AND Value7 <= 0.024031 THEN data is of type L1C2f_d40 (24.0)
IF Value7 > -0.087032 AND Value7 > 0.580399 AND Value1 > 0.348135 AND Value7 > 1.0405 THEN data is of type L1f_d40 (86.0)	IF Value6 > 0.414889 THEN data is of type nf_d40 (208.0)	IF Value7 > 0.412857 AND Value8 <= 0.329041 THEN data is of type L1C2f_d40 (34.0)	IF Value7 <= -0.18062 AND Value6 <= 0.06558 AND Value9 > -0.045378 AND Value1 > -0.061957 THEN data is of type L1f_d40 (18.0)	IF Value7 > -0.039382 AND Value4 > 0.064118 THEN data is of type L1C2f_d40 (12.0/1.0)
IF Value10 <= -0.000946 AND Value7 <= -0.70758 AND Value7 <= -1.133314 AND Value7 <= -1.259716 THEN data is of type L1C2f_d40 (36.0)	IF Value8 > 0.41385 AND Value8 > 0.704947 THEN data is of type L1C2f_d40 (47.0)	IF Value9 > 0.412917 AND Value8 <= 0.41385 AND Value1 > 0.220841 THEN data is of type L1f_d40 (17.0)	IF Value7 <= -0.18062 AND Value9 <= -0.060614 AND Value6 <= 0.06558 AND Value8 > -0.3056 AND Value9 <= -0.165171 THEN data is of type C2f_d40 (61.0)	IF Value7 <= -0.039382 THEN data is of type L1f_d40 (10.0/1.0)
IF Value10 <= -0.000946 AND Value7 <= -0.70758 AND Value9 <= -0.630601 AND Value7 <= -1.133314 AND Value1 <= -0.353097 THEN data is of type L1f_d40 (26.0)	IF Value8 > 0.41385 AND Value5 <= 0.107028 THEN data is of type L1C2f_d40 (24.0)	IF Value9 > 0.412917 AND Value9 <= 0.516876 AND Value8 > 0.410465 THEN data is of type C2f_d40 (66.0)	IF Value8 <= -0.181196 AND Value1 <= 0.044691 AND Value7 > -0.619869 THEN data is of type L1f_d40 (41.0)	IF Value8 <= 0.219542 THEN data is of type C2f_d40 (9.0)
IF Value10 <= -0.000946 AND Value7 <= -0.70758 AND Value9 <= -0.630601 AND Value8 > -1.107308 AND Value9 <= -0.863652 THEN data is of type C2f_d40 (225.0)	IF Value8 > 0.41385 AND Value9 > 0.704908 AND Value1 > 0.300031 THEN data is of type L1f_d40 (19.0)	IF Value6 <= -0.225307 AND Value7 > -0.39304 AND Value2 <= -0.310277 THEN data is of type nf_d40 (112.0)	IF Value7 <= -0.182694 AND Value9 <= -0.060614 AND Value8 > -0.168796 THEN data is of type C2f_d40 (20.0)	
IF Value7 <= -0.087032 AND	IF Value8 > 0.41385 AND Value7 <=	IF Value7 <= -0.309833 AND	IF Value7 <= -0.183227 AND Value7 > -0.764161	

Value10 > -0.001408 AND Value9 <= 0.001634 THEN data is of type S1op_d40 (2000.0)	0.317816 THEN data is of type L1C2f_d40 (14.0)	Value9 > -0.185258 AND Value1 > -0.121065 AND Value1 <= 0.022394 THEN data is of type L1f_d40 (14.0)	THEN data is of type L1C2f_d40 (25.0)	

Table 6.22: Rule set for duty cycle = 40%

Fig.6.19 shows the confusion matrix for the six operational cases for the 75% duty cycle operation and table 6.23 shows the corresponding rules.

a	b	c	d	e	f
1980	**0**	**0**	**2**	**18**	**0**
0	**1998**	**0**	**0**	**0**	**2**
2	**0**	**1996**	**1**	**0**	**1**
2	**0**	**0**	**1942**	**38**	**18**
43	**0**	**1**	**35**	**1913**	**8**
4	**2**	**0**	**39**	**24**	**1933**

Number of Rules generated: 97
Classification rate: 98.01%

where; a = no fault data (nf_d75), b = switch short circuit fault data (S1sh_d75), c = switch open circuit fault data (S1op_d75), d = inductor fault data (L1f_d75), e = capacitor fault data (C2f_d75), f = inductor & capacitor fault data (L1C2f_d75).

Figure 6.19: Confusion matrix for duty cycle 75% using |S1off| equation for SIMULINK

Rules 1-20	Rules 21-40	Rules 41-60	Rules 61-80	Rules 81-97
IF Value8 > 2.553644 AND Value9 <= 2.55462 THEN data is of type S1sh_d75 (2000.0)	IF Value8 <= -2.620603 AND Value8 > -4.7483 AND Value10 > -2.630715 AND Value7 <= 0.411348 THEN data is of type L1f_d75 (102.0)	IF Value7 > -1.376443 AND Value8 > 1.156874 AND Value7 <= 1.096917 AND Value1 <= 0.411747 THEN data is of type L1C2f_d75 (28.0)	IF Value8 > -0.016386 AND Value7 <= -1.138248 THEN data is of type S1op_d75 (224.0)	IF Value7 <= -0.651082 AND Value8 <= -1.166986 AND Value7 > -2.079428 AND Value1 <= -0.388129 AND Value1 > -1.084447 THEN data is of type L1f_d75 (22.0)
IF Value7 > -1.376443 AND Value8 > 4.148224 THEN data is of type L1C2f_d75 (588.0)	IF Value9 > 2.13812 AND Value8 <= 2.404311 AND Value5 <= 1.429479 AND Value1 > 1.000016 THEN data is of type L1f_d75 (101.0)	IF Value7 > -1.376443 AND Value8 > 1.161905 AND Value9 <= 1.929692 AND Value7 > 1.23675 AND Value9 <= 1.771776 THEN data is of type C2f_d75 (141.0/1.0)	IF Value7 <= -1.807441 AND Value6 <= -1.024149 AND Value9 > -3.650037 AND Value7 <= -2.864132 THEN data is of type L1f_d75 (50.0)	IF Value7 <= -0.651082 AND Value3 > -0.632892 AND Value3 <= -0.251389 THEN data is of type L1C2f_d75 (24.0)
IF Value7 > -1.376443 AND Value7 > 2.137183 AND Value1 <= 0.892374 AND Value8 > 1.329678 THEN data is of type L1C2f_d75 (207.0)	IF Value7 > -1.376443 AND Value8 <= -1.390885 AND Value10 > -1.791659 AND Value7 <= 1.188505 AND Value1 > -1.011613 THEN data is of type L1f_d75 (108.0)	IF Value7 > -1.376443 AND Value7 > 1.228321 AND Value1 > -0.429446 AND Value1 <= 0.729976 THEN data is of type L1f_d75 (41.0)	IF Value7 <= -1.807441 AND Value1 <= -1.417698 THEN data is of type C2f_d75 (55.0/1.0)	IF Value1 > 0.298862 AND Value8 <= 0.567239 AND Value7 > -0.228605 AND Value9 <= 0.563304 THEN data is of type C2f_d75 (41.0/4.0)
IF Value7 <= -2.610798 AND Value10 > -0.798913 THEN data is of type S1op_d75 (1642.0)	IF Value7 > -1.376443 AND Value7 > 2.139588 AND Value10 > 1.917559 AND Value10 <= 3.257809	IF Value8 <= -1.808386 AND Value1 <= -0.356512 AND Value9 > -1.814578 AND Value7 > -2.723199	IF Value7 <= -1.807441 AND Value7 <= -2.924095 THEN data is of type L1C2f_d75 (40.0)	IF Value2 <= -0.151483 AND Value8 > -0.068552 AND Value7 > -0.280492 THEN data is of type C2f_d75

	AND Value5 > 1.159806 AND Value7 > 2.849209 THEN data is of type C2f_d75 (138.0)	THEN data is of type L1f_d75 (44.0)		(34.0)
IF Value8 <= -2.612551 AND Value10 <= -5.394028 THEN data is of type L1C2f_d75 (432.0)	IF Value1 > 1.54813 AND Value9 > 0.780048 AND Value7 <= 2.293956 THEN data is of type nf_d75 (316.0)	IF Value7 > -1.376443 AND Value9 > 1.160625 AND Value5 > 0.463856 AND Value5 <= 0.702324 THEN data is of type L1f_d75 (38.0)	IF Value6 <= -1.381343 THEN data is of type nf_d75 (142.0)	IF Value9 > -0.258154 AND Value6 > 0.691295 AND Value9 <= 1.173424 THEN data is of type C2f_d75 (15.0)
IF Value7 > 2.137183 AND Value5 > 0.213152 AND Value7 > 3.688686 AND Value2 > 1.076435 AND Value2 > 1.409766 THEN data is of type L1f_d75 (249.0)	IF Value7 > -1.376443 AND Value7 > 1.58762 AND Value8 <= 1.42073 AND Value7 > 2.145102 THEN data is of type L1C2f_d75 (96.0)	IF Value7 > -1.376443 AND Value6 <= -0.622666 AND Value5 <= -1.015684 THEN data is of type nf_d75 (132.0)	IF Value7 <= -0.704267 AND Value9 > -0.717288 AND Value8 <= -0.790503 AND Value1 <= 0.001888 THEN data is of type L1f_d75 (25.0/1.0)	IF Value10 > -0.258211 AND Value10 > 0.705802 AND Value1 <= 0.833388 THEN data is of type L1C2f_d75 (9.0)
IF Value8 <= -2.611919 AND Value6 <= -1.548025 AND Value7 > -2.56664 THEN data is of type L1f_d75 (115.0)	IF Value9 > 1.588458 AND Value7 <= 1.586152 AND Value1 > 0.497572 AND Value8 <= 1.860737 AND Value7 > 0.945515 THEN data is of type L1f_d75 (48.0/2.0)	IF Value7 > -1.014214 AND Value8 <= -1.014073 AND Value1 > -0.470911 THEN data is of type L1f_d75 (27.0)	IF Value7 <= -0.704267 AND Value10 > -0.710662 AND Value1 <= -0.299686 THEN data is of type L1C2f_d75 (31.0)	IF Value10 > -0.258211 AND Value7 <= -0.259481 AND Value1 > -0.199432 AND Value1 <= 0.274769 THEN data is of type L1f_d75 (31.0)
IF Value7 > 2.137183 AND Value5 > 0.213152 AND Value8 <= 2.091226 THEN data is of type L1f_d75 (219.0/1.0)	IF Value7 > -1.376443 AND Value7 > 1.58762 AND Value10 <= 1.508461 AND Value1 > -0.317937 THEN data is of type L1f_d75 (64.0)	IF Value7 > -1.014214 AND Value7 > 1.232021 AND Value1 <= 0.87106 THEN data is of type L1C2f_d75 (26.0)	IF Value7 <= -0.704267 AND Value6 <= 0.044809 AND Value7 > -1.739734 AND Value1 <= -0.727825 AND Value8 > -1.788677 THEN data is of type C2f_d75 (120.0)	IF Value7 > -0.264582 AND Value9 <= 0.107101 AND Value3 <= 0.192126 AND Value8 > -0.290265 THEN data is of type nf_d75 (151.0)
IF Value8 <= -2.611919 AND Value6 <= -1.548249 AND Value8 > -5.386935 AND Value7 > -5.402661 AND Value9 <= -4.748239 THEN data is of type C2f_d75 (100.0)	IF Value7 > -1.376443 AND Value7 > 1.58762 AND Value9 <= 2.848114 AND Value5 > 0.051472 AND Value7 > 2.478596 AND Value5 > 1.121104 THEN data is of type C2f_d75 (127.0)	IF Value7 > -1.014214 AND Value1 <= -0.340761 AND Value7 <= -0.286399 AND Value3 <= -0.836499 THEN data is of type nf_d75 (66.0)	IF Value7 > -0.709763 AND Value9 <= -0.375935 AND Value1 <= -0.203499 AND Value3 > -0.511925 THEN data is of type nf_d75 (36.0)	IF Value10 > -0.167215 AND Value8 <= 0.110918 AND Value1 <= 0.32447 THEN data is of type L1f_d75 (52.0)
IF Value8 <= -2.611919 AND Value6 <= -1.548249 AND Value8 <= -4.735661 THEN data is of type L1f_d75 (115.0)	IF Value1 > 1.569388 THEN data is of type S1op_d75 (133.0)	IF Value7 > -0.838426 AND Value1 <= -0.300077 AND Value7 <= -0.246344 AND Value3 > -0.421365 THEN data is of type nf_d75 (62.0)	IF Value7 > -0.709763 AND Value9 <= -0.375935 AND Value7 <= -0.516368 AND Value1 <= -0.252664 AND Value8 > -0.705279 AND Value6 <= -0.64423 THEN data is of type nf_d75 (24.0)	IF Value7 > -0.144933 AND Value10 <= 0.388686 THEN data is of type nf_d75 (88.0)
IF Value8 > 2.137676 AND Value3 > 0.972779 AND Value9 > 3.663166 AND Value1 > 1.557675 THEN data is of type L1f_d75 (59.0)	IF Value8 <= -2.768012 AND Value6 <= -1.68477 AND Value1 <= -1.813848 THEN data is of type L1f_d75 (73.0)	IF Value7 > -0.838441 AND Value1 <= -0.300467 AND Value7 > -0.423505 THEN data is of type C2f_d75 (78.0)	IF Value7 > -0.63783 AND Value8 > 0.264712 AND Value7 <= 0.245009 AND Value7 <= -0.182119 THEN data is of type L1C2f_d75 (20.0)	IF Value6 > 0.580735 AND Value5 <= 0.838774 THEN data is of type nf_d75 (47.0)
IF Value8 > 2.14177 AND Value5 > 0.971059 AND Value3 > 1.766509 THEN data is of type	IF Value1 <= -1.817567 AND Value9 <= -0.886344 THEN data is of type nf_d75 (278.0)	IF Value7 > -0.838426 AND Value10 > 1.244972 AND Value7 > 1.141529 THEN data is of type L1f_d75	IF Value7 > -0.63783 AND Value2 > 0.319257 AND Value8 > 0.312285 AND Value2 <= 0.682984 AND Value6 <= 0.578827 THEN data is of type	IF Value10 > -0.167215 AND Value7 > -0.242494 AND Value1 <= 0.406167 THEN data is of type L1f_d75

C2f_d75 (213.0)		(26.0/1.0)	nf_d75 (116.0)	(19.0)
IF Value8 <= -2.611919 AND Value2 <= -1.54844 AND Value7 > -4.742886 AND Value9 <= -4.12823 THEN data is of type C2f_d75 (94.0)	IF Value8 <= -1.808386 AND Value7 > -1.347346 THEN data is of type L1C2f_d75 (105.0/1.0)	IF Value7 > -0.838426 AND Value6 > 0.540145 AND Value7 > 0.538574 AND Value9 <= 1.157283 AND Value4 <= 0.951287 AND Value9 <= 0.968063 AND Value2 > 0.682984 AND Value7 > 0.682096 THEN data is of type nf_d75 (137.0/13.0)	IF Value7 <= -0.63783 AND Value6 <= 0.082637 AND Value9 <= -2.158605 AND Value1 > -1.210867 THEN data is of type C2f_d75 (39.0)	IF Value6 > -0.26144 AND Value9 <= -0.157515 AND Value7 > -1.705202 THEN data is of type C2f_d75 (32.0/1.0)
IF Value8 <= -2.611919 AND Value6 <= -1.548249 AND Value8 > -4.139943 AND Value7 > -4.147857 AND Value1 <= -1.822641 THEN data is of type C2f_d75 (82.0)	IF Value8 <= -1.808386 AND Value7 <= -4.112838 AND Value1 > -1.627764 THEN data is of type L1C2f_d75 (65.0)	IF Value7 > -0.838426 AND Value6 <= -0.288346 AND Value3 <= -0.511925 AND Value7 <= -0.516368 AND Value8 > -0.838734 AND Value6 <= -0.709385 THEN data is of type nf_d75 (50.0)	IF Value7 <= -0.63783 AND Value6 > 0.082637 THEN data is of type L1C2f_d75 (35.0)	IF Value1 > -0.27297 AND Value1 <= 0.751854 THEN data is of type L1C2f_d75 (14.0)
IF Value8 <= -2.612551 AND Value1 > -0.975495 THEN data is of type L1C2f_d75 (97.0/1.0)	IF Value8 <= -1.808386 AND Value2 <= -1.019994 AND Value7 > -2.332599 THEN data is of type C2f_d75 (65.0)	IF Value7 > -0.704267 AND Value4 > 0.951287 AND Value9 <= 1.157283 THEN data is of type nf_d75 (101.0)	IF Value7 <= -0.63783 AND Value7 <= -2.142154 AND Value3 <= -0.763983 THEN data is of type L1f_d75 (32.0)	IF Value7 > -1.944345 AND Value7 > -0.516368 AND Value1 <= -0.416754 THEN data is of type C2f_d75 (13.0)
IF Value8 <= -2.620603 AND Value8 > -4.7483 AND Value1 <= -1.409933 AND Value8 > -3.249563 AND Value1 <= -1.525649 THEN data is of type C2f_d75 (58.0)	IF Value7 > -1.376443 AND Value9 > 1.588458 AND Value10 > 2.504733 AND Value1 > 1.294133 AND Value10 <= 3.560006 THEN data is of type L1f_d75 (62.0)	IF Value7 > -0.704267 AND Value8 > 0.685578 AND Value7 <= 0.670243 AND Value7 <= 0.269446 THEN data is of type L1C2f_d75 (21.0)	IF Value7 <= -0.63783 AND Value7 <= -2.154492 AND Value7 <= -2.351356 THEN data is of type L1C2f_d75 (30.0)	IF Value8 > -1.060112 THEN data is of type nf_d75 (66.0/13.0)
IF Value8 <= -2.620603 AND Value8 > -4.7483 AND Value1 <= -1.409933 AND Value9 > -3.38483 THEN data is of type L1f_d75 (96.0/1.0)	IF Value9 > 1.588458 AND Value7 > 1.548903 AND Value9 <= 2.509523 AND Value7 > 1.773531 THEN data is of type C2f_d75 (140.0/3.0)	IF Value7 > -0.704267 AND Value8 > 0.685578 AND Value6 <= 0.410999 AND Value6 > 0.05089 THEN data is of type C2f_d75 (98.0)	IF Value7 <= -0.63783 AND Value10 > -0.635362 AND Value8 <= -0.049716 THEN data is of type L1f_d75 (22.0)	IF Value8 > -1.737193 THEN data is of type L1f_d75 (7.0)
IF Value9 > 2.13812 AND Value1 <= 0.948539 AND Value9 > 2.177219 THEN data is of type L1C2f_d75 (51.0)	IF Value8 <= -1.808386 AND Value2 <= -1.019994 AND Value9 <= -2.351927 AND Value9 > -3.650037 AND Value1 > -1.636118 AND Value9 <= -2.836832 THEN data is of type C2f_d75 (52.0)	IF Value7 > -0.705397 AND Value9 > 0.688517 AND Value5 <= 0.855138 AND Value1 > 0.539318 AND Value7 <= 0.853369 THEN data is of type L1C2f_d75 (12.0)	IF Value8 <= -0.63949 AND Value10 <= -0.514989 AND Value7 <= -1.067085 AND Value9 <= -1.334454 AND Value3 > -0.6889 AND Value1 <= -0.140181 THEN data is of type C2f_d75 (45.0)	
IF Value9 > 2.13812 AND Value8 <= 3.357657 AND Value9 > 3.229897 AND Value1 > 1.366637 THEN data is of type L1f_d75 (57.0)	IF Value7 > -1.376443 AND Value8 <= 1.7754 AND Value4 > 1.013684 AND Value9 <= 1.592093 AND Value5 > 1.159298 THEN data is of type nf_d75 (214.0)	IF Value7 > -0.705397 AND Value9 > 0.688517 AND Value5 <= 0.812005 AND Value1 > 0.140155 AND Value7 <= 0.91726 THEN data is of type L1f_d75 (53.0)	IF Value8 <= -0.63949 AND Value7 > -1.347346 AND Value9 <= -0.509831 AND Value8 > -1.165594 THEN data is of type C2f_d75 (50.0)	
IF Value8 > 2.137676 AND	IF Value8 > 1.156874 AND Value9 >	IF Value7 > -0.704267 AND	IF Value8 <= -0.63949 AND Value7 > -1.734761	

Value10 <= 3.257809 AND Value5 <= 1.15842 AND Value9 <= 2.43384 AND Value7 > 1.984442 THEN data is of type C2f_d75 (74.0)	1.784462 AND Value8 > 1.785327 THEN data is of type L1C2f_d75 (60.0/1.0)	Value8 > 0.262309 AND Value6 <= 0.157049 AND Value7 > 0.066132 AND Value8 <= 0.877655 THEN data is of type C2f_d75 (72.0)	AND Value9 > -1.189261 THEN data is of type L1f_d75 (46.0)	

Table 6.23: Rule set for duty cycle = 75%

Fig.6.20 shows the confusion matrix for the six operational cases for the 95% duty cycle operation and table 6.24 shows the corresponding rules.

a	b	c	d	e	f
1978	**0**	**0**	**3**	**19**	**0**
0	**2000**	**0**	**0**	**0**	**0**
0	**0**	**2000**	**0**	**0**	**0**
6	**0**	**0**	**1948**	**38**	**8**
45	**0**	**0**	**25**	**1923**	**7**
1	**0**	**0**	**18**	**9**	**1972**

Number of Rules generated: 95
Classification rate: 98.5%

where; a = no fault data (nf_d95), b = switch short circuit fault data (S1sh_d95), c = switch open circuit fault data (S1op_d95), d = inductor fault data (L1f_d95), e = capacitor fault data (C2f_d95), f = inductor & capacitor fault data (L1C2f_d95).

Figure 6.20: Confusion matrix for duty cycle 95% using |S1off| equation for SIMULINK

Rules 1-20	Rules 21-40	Rules 41-60	Rules 61-80	Rules 81-95
IF Value7 <= -2.637184 AND Value10 > -1.142861 THEN data is of type S1op_d95 (1961.0)	IF Value2 > 0.626867 AND Value7 <= 0.809163 THEN data is of type nf_d95 (329.0)	IF Value7 > 0.455861 AND Value8 > -0.59457 AND Value7 <= 0.625095 THEN data is of type L1f_d95 (109.0/2.0)	IF Value7 <= -0.630806 AND Value7 <= -1.172872 THEN data is of type L1C2f_d95 (25.0)	IF Value8 <= 0.045585 AND Value9 > 0.045306 AND Value1 > -0.088268 THEN data is of type L1f_d95 (42.0/1.0)
IF Value8 <= 0.677043 AND Value8 <= -1.169708 AND Value8 <= -2.666332 AND Value10 <= -1.193576 THEN data is of type L1C2f_d95 (362.0)	IF Value7 > 0.625869 AND Value9 > 1.031745 AND Value2 > 0.499526 AND Value8 <= 1.212235 THEN data is of type L1f_d95 (182.0)	IF Value8 <= -1.694168 AND Value8 > -2.051329 AND Value7 > -2.091728 THEN data is of type C2f_d95 (58.0)	IF Value1 <= -0.276381 AND Value3 <= -0.392438 THEN data is of type nf_d95 (178.0)	IF Value9 <= 0.045306 AND Value8 > -0.127272 AND Value7 > -0.221784 AND Value1 <= 0.039839 THEN data is of type nf_d95 (167.0)
IF Value8 <= 0.677043 AND Value8 <= -1.169708 AND Value2 > -0.637037 AND Value10 <= -1.307877 AND Value8 <= -1.573907 THEN data is of type L1C2f_d95 (163.0)	IF Value8 <= -1.169708 AND Value7 <= -2.436315 AND Value1 > -0.905795 THEN data is of type L1C2f_d95 (8.0)	IF Value3 > 0.154979 AND Value9 <= 0.454756 AND Value3 > 0.212125 AND Value7 > 0.198361 THEN data is of type nf_d95 (313.0/7.0)	IF Value9 <= -0.401876 AND Value1 <= -0.276381 THEN data is of type C2f_d95 (88.0)	IF Value1 <= -0.159183 AND Value2 > -0.190112 THEN data is of type nf_d95 (19.0)
IF Value8 <= 0.677043 AND Value7 > 0.768969 AND Value1 > 0.020332 THEN data is of type L1f_d95 (190.0)	IF Value8 <= -1.169708 AND Value9 <= -1.166303 AND Value8 > -1.373105 THEN data is of type C2f_d95 (63.0/1.0)	IF Value7 > 0.205767 AND Value7 > 0.506863 AND Value6 <= 0.600805 THEN data is of type L1C2f_d95 (56.0)	IF Value7 <= -0.40102 AND Value8 > -0.460738 THEN data is of type L1C2f_d95 (50.0/4.0)	IF Value2 <= -0.190289 AND Value1 <= -0.264245 THEN data is of type nf_d95 (12.0)
IF Value7 > 1.311257	IF Value8 > 0.625823	IF Value7 > 0.205767	IF Value8 <= -	IF Value7 <= -

AND Value10 <= 0.141873 THEN data is of type S1sh_d95 (920.0)	AND Value4 <= 0.251996 THEN data is of type L1C2f_d95 (92.0)	AND Value9 <= 0.450243 AND Value8 > 0.062318 AND Value1 <= 0.126384 THEN data is of type C2f_d95 (142.0)	0.402843 AND Value1 <= -0.161306 AND Value9 > -0.531803 THEN data is of type L1f_d95 (52.0/1.0)	0.22622 AND Value8 > -0.083194 THEN data is of type L1C2f_d95 (21.0)
IF Value8 > 1.155897 AND Value9 <= 0.917933 THEN data is of type S1sh_d95 (1080.0)	IF Value8 > 0.625823 AND Value7 > 1.07596 AND Value8 <= 0.971244 THEN data is of type L1f_d95 (37.0)	IF Value7 > 0.206038 AND Value8 <= 0.54681 THEN data is of type L1f_d95 (146.0/1.0)	IF Value1 <= -0.16151 AND Value7 <= -0.05171 AND Value3 <= -0.290643 THEN data is of type nf_d95 (86.0)	IF Value8 > -0.101225 AND Value9 <= 0.195207 AND Value1 > -0.094996 THEN data is of type C2f_d95 (33.0)
IF Value7 > 1.311373 AND Value10 > 1.636261 THEN data is of type L1C2f_d95 (668.0)	IF Value8 > 0.625823 AND Value7 > 0.80126 AND Value9 <= 1.059947 AND Value4 <= 0.660458 THEN data is of type C2f_d95 (263.0)	IF Value9 > 0.20347 AND Value1 <= 0.037085 THEN data is of type L1C2f_d95 (57.0)	IF Value1 <= -0.163635 AND Value7 <= -0.05457 AND Value8 > -0.299302 AND Value3 <= -0.128201 AND Value7 <= -0.134527 AND Value1 <= -0.291384 THEN data is of type nf_d95 (72.0)	IF Value9 <= -0.133951 AND Value7 > -0.407583 AND Value8 > -0.222919 AND Value7 <= -0.198678 THEN data is of type nf_d95 (13.0/2.0)
IF Value7 > 0.810922 AND Value3 <= 0.389009 AND Value7 > 0.882515 THEN data is of type L1C2f_d95 (367.0)	IF Value8 <= -1.181713 AND Value9 > -1.374232 THEN data is of type L1f_d95 (76.0)	IF Value7 <= -1.172872 AND Value2 <= -0.445863 AND Value9 <= -2.055462 AND Value3 > -1.015172 THEN data is of type C2f_d95 (46.0)	IF Value1 <= -0.163635 AND Value1 <= -0.29111 THEN data is of type C2f_d95 (71.0)	IF Value9 <= -0.133951 AND Value7 > -0.407583 THEN data is of type C2f_d95 (13.0)
IF Value7 > 0.810922 AND Value9 > 1.275538 AND Value6 > 0.617256 THEN data is of type L1f_d95 (333.0)	IF Value8 <= -1.278472 AND Value8 > -1.592075 AND Value7 > -1.666862 THEN data is of type C2f_d95 (62.0)	IF Value3 <= -0.619598 AND Value10 > -1.327143 THEN data is of type nf_d95 (367.0)	IF Value1 <= -0.163635 AND Value7 > -0.052873 THEN data is of type C2f_d95 (54.0)	IF Value8 <= 0.006874 AND Value1 <= -0.021521 THEN data is of type L1f_d95 (29.0)
IF Value7 > 0.810922 AND Value7 <= 1.326215 AND Value6 > 0.282689 AND Value7 > 1.031218 AND Value3 > 0.544401 THEN data is of type C2f_d95 (440.0/1.0)	IF Value8 <= -1.578577 AND Value9 <= -1.593835 AND Value8 > -1.818219 AND Value7 > -1.860039 THEN data is of type C2f_d95 (60.0)	IF Value8 <= -0.631393 AND Value3 <= -0.392528 AND Value8 > -0.986706 THEN data is of type C2f_d95 (115.0/1.0)	IF Value9 > 0.20657 AND Value2 <= 0.241199 THEN data is of type L1f_d95 (48.0)	IF Value1 <= 0.452794 THEN data is of type L1C2f_d95 (13.0/1.0)
IF Value8 <= -1.169708 AND Value2 > -0.440518 AND Value8 <= -1.189894 THEN data is of type L1C2f_d95 (67.0)	IF Value8 <= -1.578577 AND Value9 > -1.822549 THEN data is of type L1f_d95 (82.0)	IF Value8 <= -0.631393 AND Value3 <= -0.540172 AND Value2 <= -0.67899 AND Value9 > -2.232622 THEN data is of type L1f_d95 (56.0)	IF Value8 <= -0.247326 AND Value9 > -0.232934 THEN data is of type L1f_d95 (34.0)	
IF Value8 <= -1.169708 AND Value10 <= -0.433477 AND Value7 > -0.950573 THEN data is of type L1f_d95 (202.0/1.0)	IF Value7 > 0.625869 AND Value8 > -0.480843 AND Value8 > 0.451728 AND Value9 <= 0.80414 THEN data is of type C2f_d95 (142.0)	IF Value7 <= -0.629587 AND Value1 <= -0.57974 THEN data is of type C2f_d95 (78.0)	IF Value7 > -0.236325 AND Value3 <= -0.045234 AND Value9 > -0.045949 AND Value7 > -0.112501 THEN data is of type C2f_d95 (32.0)	
IF Value8 <= -1.169708 AND Value10 <= -0.498067 AND Value10 <= -2.361767 AND Value5 <= -0.854622 THEN data is of type C2f_d95 (64.0)	IF Value7 > 0.625869 AND Value8 > -0.480843 AND Value8 <= 0.952083 AND Value1 <= 0.611314 THEN data is of type L1f_d95 (139.0/1.0)	IF Value7 <= -0.629587 AND Value1 <= -0.413939 AND Value9 > -1.082693 THEN data is of type L1f_d95 (53.0)	IF Value3 <= -0.128201 AND Value7 > -0.177424 THEN data is of type C2f_d95 (27.0)	
IF Value8 <= -1.169708 AND Value10 <= -	IF Value5 > 0.256001 AND Value9 <=	IF Value7 <= -0.629587 AND	IF Value8 <= -0.247326 AND	

0.498067 AND Value8 <= -2.358288 AND Value1 <= -0.918435 THEN data is of type L1f_d95 (76.0)	0.624763 AND Value4 > 0.296852 AND Value5 > 0.456719 THEN data is of type nf_d95 (242.0)	Value7 <= -0.806808 AND Value9 > -0.873429 AND Value2 > -0.318464 THEN data is of type L1C2f_d95 (49.0/1.0)	Value2 <= 0.041735 THEN data is of type C2f_d95 (23.0/1.0)	
IF Value8 <= -1.169708 AND Value10 > -0.498067 THEN data is of type S1op_d95 (39.0)	IF Value7 > 0.455001 AND Value6 > -0.172213 AND Value9 <= 0.623125 AND Value8 > 0.276915 THEN data is of type C2f_d95 (118.0)	IF Value8 <= -0.631393 AND Value7 > -1.172872 AND Value10 > -0.865811 AND Value1 <= -0.261165 THEN data is of type L1f_d95 (115.0/1.0)	IF Value7 > -0.236325 AND Value8 > 0.045479 AND Value2 > 0.026347 AND Value2 <= 0.215913 THEN data is of type nf_d95 (169.0)	

Table 6.24: Rule set for duty cycle = 95%

6.4.2 Training rules on data of a particular duty cycle to test on another

The confusion matrices and rule-tables in the previous subsection showed that in general, with a 10-fold cross validation test, a classification rate of over 97% is achieved. However, trying to achieve a global rule set would warrant a set of rules generated for any duty cycles to hold up when trained on data for another. This subsection and the ones to follow display results for keeping one duty cycle as the base and training data streams of other duty cycles on it.

6.4.2.1 Training data – 10% duty cycle

Here, the $|S1off|$ equation output for the 10% duty cycle simulation is used to test rules for all other duty cycles as listed in table 6.19. The set of rules are identical to those in table 6.20 as this comparison checks (or tests) how well they match (or generalise) against rules for other duty cycles as seen in tables 6.21-6.24. The confusion matrix and classification rate reflect how well or badly one set of rules are generalised over others as shown in the software and hardware data comparison in section 6.3.5. Table 6.25 clubs together results of testing rules for other duty cycles after training them on rules for 10% duty cycle.

Training data set – Rules for 10% duty cycle		
Test data set list	**Confusion matrices**	**Statistics**
Test data – 25% duty cycle	**a b c d e f** **43 0 0 36 1746 175 a** **0 2000 0 0 0 0 b** **11 0 0 890 1020 79 c** **8 0 0 19 1907 66 d** **19 0 0 25 1820 136 e** **17 0 0 36 1869 78 f**	Correctly classified – 3960 (33%) Incorrectly classified – 8040 (67%)
Test data – 40% duty cycle	**a b c d e f** **9 0 0 5 1938 48 a** **0 2000 0 0 0 0 b** **2 0 0 966 1016 16 c** **2 133 0 35 1813 17 d** **4 168 0 9 1793 26 e** **3 558 0 31 1394 14 f**	Correctly classified – 3851 (32.09%) Incorrectly classified – 8149 (67.9%)
Test data – 75% duty cycle	**a b c d e f** **0 472 0 0 1520 8 a** **0 2000 0 0 0 0 b** **0 0 0 576 1422 2 c** **0 686 0 33 1277 4 d** **0 814 0 0 1185 1 e** **0 943 0 14 1041 2 f**	Correctly classified – 3220 (26.8%) Incorrectly classified – 8780 (73.1%)
Test data – 95% duty cycle	**a b c d e f** **0 0 0 0 1988 12 a** **0 859 0 0 1141 0 b** **0 0 0 306 1687 7 c** **0 193 0 15 1779 13 d** **0 0 0 1 1999 0 e** **0 788 0 3 1208 1 f**	Correctly classified – 2874 (23.95%) Incorrectly classified – 9126 (76.05%)
Average correct classification rate	28.96%	

Table 6.25: Generalisation results for data trained on rules for 10% duty cycle

6.4.2.2 Training data – 25% duty cycle

In this subsection, the base training data is the rules for 25% duty cycle and all other rules are tested against it. Table 6.26 shows results.

Training data set – Rules for 25% duty cycle		
Test data set list	**Confusion matrices**	**Statistics**
Test data – 10% duty cycle	**a b c d e f** **2000 0 0 0 0 0 a** **0 2000 0 0 0 0 b** **2000 0 0 0 0 0 c** **2000 0 0 0 0 0 d** **76 639 0 47 43 1195 e** **1035 0 0 680 285 0 f**	Correctly classified – 4043 (33.7%) Incorrectly classified – 7957 (66.3%)
Test data – 40% duty cycle	**a b c d e f** **466 0 0 92 370 1072 a** **0 2000 0 0 0 0 b** **246 0 480 0 0 1274 c** **17 400 0 339 71 1173 d** **136 448 0 10 121 1285 e** **23 693 0 69 23 1192 f**	Correctly classified – 4598 (38.3%) Incorrectly classified – 7402 (61.7%)
Test data – 75% duty cycle	**a b c d e f** **153 690 0 25 126 1006 a** **0 2000 0 0 0 0 b** **0 0 0 0 0 2000 c** **21 784 0 203 25 967 d** **41 920 0 10 25 1004 e** **3 991 0 132 1 873 f**	Correctly classified – 3254 (27.1%) Incorrectly classified – 8746 (72.9%)
Test data – 95% duty cycle	**a b c d e f** **367 0 0 67 321 1245 a** **27 1699 0 269 0 5 b** **0 0 0 0 0 2000 c** **43 528 0 373 81 975 d** **76 639 0 47 43 1195 e** **2 936 0 185 6 871 f**	Correctly classified – 3353 (27.94%) Incorrectly classified – 8647 (72.06%)
Average correct classification rate	31.76%	

Table 6.26: Generalisation results for data trained on rules for 25% duty cycle

6.4.2.3 Training data – 40% duty cycle

In this subsection, the base training data is the rules for 40% duty cycle and all other rules are tested against it. Table 6.27 shows results.

Training data set – Rules for 40% duty cycle		
Test data set list	**Confusion matrices**	**Statistics**
Test data – 10% duty cycle	**a b c d e f** **2000 0 0 0 0 0 a** **0 2000 0 0 0 0 b** **2000 0 0 0 0 0 c** **2000 0 0 0 0 0 d** **117 0 0 359 1102 422 e** **2000 0 0 0 0 0 f**	Correctly classified – 5102 (42.5%) Incorrectly classified – 6898 (57.5%)
Test data – 25% duty cycle	**a b c d e f** **1974 0 0 2 12 12 a** **0 2000 0 0 0 0 b** **204 0 1104 0 692 0 c** **392 0 0 660 749 199 d** **652 0 0 260 1000 88 e** **123 0 1 591 824 461 f**	Correctly classified – 7199 (59.9%) Incorrectly classified – 4801 (40.1%)
Test data – 75% duty cycle	**a b c d e f** **737 0 0 100 431 732 a** **0 1640 0 191 0 169 b** **0 0 2000 0 0 0 c** **24 229 0 477 43 1227 d** **175 222 0 65 169 1369 e** **50 720 0 57 7 1166 f**	Correctly classified – 6189 (51.5%) Incorrectly classified – 5811 (48.5%)
Test data – 95% duty cycle	**a b c d e f** **1671 0 0 1 326 2 a** **149 0 0 339 274 1238 b** **0 0 0 211 253 1536 c** **18 0 0 1171 269 542 d** **117 0 0 359 1102 422 e** **0 0 0 51 11 1938 f**	Correctly classified – 5882 (49.01%) Incorrectly classified – 6118 (50.99%)
Average correct classification rate	50.77%	

Table 6.27: Generalisation results for data trained on rules for 40% duty cycle

6.4.2.4 Training data – 75% duty cycle

In this subsection, the base training data is the rules for 75% duty cycle and all other rules are tested against it. Table 6.28 shows results.

Training data set – Rules for 75% duty cycle		
Test data set list	**Confusion matrices**	**Statistics**
Test data – 10% duty cycle	**a b c d e f** **2000 0 0 0 0 0 a** **0 901 0 0 0 1099 b** **2000 0 0 0 0 0 c** **2000 0 0 0 0 0 d** **596 0 0 375 805 224 e** **2000 0 0 0 0 0 f**	Correctly classified – 3706 (30.8%) Incorrectly classified – 8294 (69.2%)
Test data – 25% duty cycle	**a b c d e f** **1982 0 0 18 0 0 a** **0 996 0 0 0 1004 b** **1806 0 0 66 128 0 c** **1283 0 0 339 378 0 d** **1729 0 0 168 103 0 e** **477 0 0 455 1068 0 f**	Correctly classified – 3420 (28.5%) Incorrectly classified – 8580 (71.5%)
Test data – 40% duty cycle	**a b c d e f** **1939 0 0 4 38 19 a** **0 1141 0 0 0 859 b** **311 0 0 554 344 791 c** **461 0 0 1194 296 49 d** **687 0 0 330 934 49 e** **123 0 0 476 622 779 f**	Correctly classified – 5987 (49.9%) Incorrectly classified – 6013 (50.1%)
Test data – 95% duty cycle	**a b c d e f** **1948 0 0 4 38 10 a** **282 0 0 721 94 903 b** **0 0 1961 39 0 0 c** **293 0 0 1204 416 87 d** **596 0 0 375 805 224 e** **59 0 0 472 469 1000 f**	Correctly classified – 6918 (57.65%) Incorrectly classified – 5082 (42.35%)
Average correct classification rate	41.73%	

Table 6.28: Generalisation results for data trained on rules for 75% duty cycle

6.4.2.5 Training data – 95% duty cycle

In this subsection, the base training data is the rules for 95% duty cycle and all other rules are tested against it. Table 6.29 shows results.

Training data set – Rules for 95% duty cycle		
Test data set list	**Confusion matrices**	**Statistics**
Test data – 10% duty cycle	**a b c d e f** **2000 0 0 0 0 0 a** **0 962 0 0 0 1038 b** **2000 0 0 0 0 0 c** **2000 0 0 0 0 0 d** **9 0 0 2 1988 1 e** **2000 0 0 0 0 0 f**	Correctly classified – 4950 (41.25%) Incorrectly classified – 7050 (58.75%)
Test data – 25% duty cycle	**a b c d e f** **1916 0 0 14 70 0 a** **0 1223 0 0 0 777 b** **694 0 0 0 1306 0 c** **565 0 0 556 755 124 d** **885 0 0 408 707 0 e** **335 0 0 216 839 610 f**	Correctly classified – 5012 (41.76%) Incorrectly classified – 6988 (58.24%)
Test data – 40% duty cycle	**a b c d e f** **1878 0 0 6 116 0 a** **63 1447 0 101 6 383 b** **874 0 0 125 109 892 c** **36 0 0 1541 294 129 d** **292 0 0 497 1115 96 e** **11 0 0 214 77 1698 f**	Correctly classified – 7679 (63.99%) Incorrectly classified – 4321 (36.01%)
Test data – 75% duty cycle	**a b c d e f** **889 0 0 251 576 284 a** **18 1465 1 119 0 397 b** **309 0 1636 8 3 44 c** **5 40 0 604 5 1346 d** **198 0 0 49 355 1398 e** **25 67 0 34 28 1846 f**	Correctly classified – 6795 (56.6%) Incorrectly classified – 5205 (43.4%)
Average correct classification rate	50.90%	

Table 6.29: Generalisation results for data trained on rules for 95% duty cycle

6.4.2.6 Training data – 50% duty cycle

In this subsection, the base training data is the rules for 50% duty cycle and all other rules are tested against it. Table 6.30 shows results.

Training data set – Rules for 50% duty cycle		
Test data set list	**Confusion matrices**	**Statistics**
Test data – 10% duty cycle	**a b c d e f** **2000 0 0 0 0 0 a** **0 2000 0 0 0 0 b** **2000 0 0 0 0 0 c** **1871 0 0 129 0 0 d** **238 0 0 455 1157 160 e** **1467 0 0 533 0 0 f**	Correctly classified – 5286 (44.05%) Incorrectly classified – 6714 (55.95%)
Test data – 25% duty cycle	**a b c d e f** **1994 0 0 6 0 0 a** **0 2000 0 0 0 777 b** **1187 0 0 681 116 16 c** **783 0 0 904 269 44 d** **855 0 0 668 430 47 e** **267 0 0 773 826 134 f**	Correctly classified – 5462 (45.5%) Incorrectly classified – 6538 (54.5%)
Test data – 40% duty cycle	**a b c d e f** **1978 0 0 4 14 4 a** **0 2000 0 0 0 0 b** **0 0 1594 116 287 3 c** **43 0 0 1638 229 90 d** **192 0 0 445 1295 68 e** **19 0 1 308 174 1498 f**	Correctly classified – 10003 (83.35%) Incorrectly classified – 1997 (16.65%)
Test data – 75% duty cycle	**a b c d e f** **1077 0 0 90 823 10 a** **0 864 0 0 0 1136 b** **0 0 2000 0 0 0 c** **0 0 0 974 61 965 d** **179 0 0 164 554 1103 e** **10 0 0 58 13 1919 f**	Correctly classified – 7388 (61.6%) Incorrectly classified – 4612 (38.4%)
Test data – 95% duty cycle	**a b c d e f** **1953 0 0 1 44 2 a** **312 0 0 423 637 628 b** **0 0 800 280 0 920 c** **121 0 0 1530 194 155 d** **238 0 0 445 1157 160 e** **0 0 0 137 97 1766 f**	Correctly classified – 7206 (60.05%) Incorrectly classified – 4794 (39.95%)
Average correct classification rate	58.90%	

Table 6.30: Generalisation results for data trained on rules for 50% duty cycle

The train-and-test results with 50% duty cycle rule-set show the highest average correct classification rate of nearly 59%. It could be argued that if heuristics for 50% duty cycle are encoded and applied to a data stream, the performance might be comparable to the results between software-hardware as shown in 6.3.5 where the classification match is nearly 62%. It is important to note that in 6.3.5, even with a relatively low classification rate (62%), the performance of rules encoded and applied to a data stream was promising. An identical approach could be used where rules for the 50% duty cycle operation are encoded in a MATLAB .m file and data

streams for no fault and fault cases from all other duty cycle operations (as shown in table 6.19) are provided as a real-time input in order to assess the speed with which the rules are able to distinguish data. In this assessment too, the necessity to distinguish streams would be required between the no fault and fault cases as shown earlier for the software-hardware data comparison.

6.5 Discussion and issues

This research stems from the application of increased power electronics devices, especially converters within the proposed zonal shipboard power distribution architectures for US Navy warships. As explained in chapter 5, these power electronic converters form an integral part of the zonal topologies. The buck converter section was chosen through a detailed FMEA in 5.3 for analysis into automated fault diagnosis. The research is aimed at providing high level diagnostics to aid in decision support at system and sub-system levels and focuses on component level and incipient failures to provide a general framework for fault identification. Along with a detailed FMEA, modification of a SCA method for electrical circuits was shown in this chapter to produce numerical data that can aid in differentiating operating scenarios.

6.5.1 Rationale for using SCA alongside FMEA

The need to understand pertinent failures in a novel system without any prior benchmarking ushered this research into reliability analysis, in turn identifying FMEA as a valid starting point elaborated in chapters 4 and 5. Further, SCA being a known reliability analysis technique to diagnose design stage circuit faults was studied to check its applicability for the novel shipboard distribution architecture.

Thereafter, the proposed modification to conventional SCA detailed in 6.2 provided a means to conduct component level fault data analysis. This method uses a high-level approach with basic measurements such as input and output currents and voltages without the need for extra sensors. This systematic methodology thus gives an analysis technique stemming from well-known design-stage reliability analysis which is in turn able to provide diagnostic indicators. Further, since the explained SCA methodology can be derived for other converter circuits, its application to other types of power electronic converters is potentially extendable.

6.5.2 Relevance and benefits of proposed approach

Proposed naval shipboard power systems are envisioned to integrate the plug and play PEBB [9] based devices, automated diagnostics and reconfiguration systems among others. One approach for this integration could be by using multi-agent systems [37] that aim to provide robustness and extensibility. As mentioned in chapter 1, the reduction in numbers of onboard crew with increase in automation put added importance on enhanced communication systems with decision support besides the obvious crucial need for accurate fault diagnosis and monitoring.

The diagnostic indicators explained in this chapter arise from the changes in the measured voltages and currents during the various operating conditions (fault and various no-fault). This changing data in theory can be used to form diagnostic indicators distinguishable using heuristics. However, SCA provides a means of understanding circuit connectivity at a device level, component level and also on a subsystem/zonal level. This information when added to the already existing FMEA database increases the understanding for mitigating risks.

Modifying conventional SCA provides the potential for single-signal diagnostics for individual inter-connected devices. Further, the key to the technique lies in its potential extendibility to more complex systems (a zone in the case of notional shipboard systems followed by interconnected zones), where the circuit connectivity information coupled with a fault diagnostic indicator could provide valuable additions for crew's decision support which is an important application keeping in mind the heavy reduction in crew numbers on future ships. Also, a positive is that owing to the approach using one signal for diagnostics per device (or per zone), the potential for adding to the burden of the notional warship's communication network is minimal.

6.5.3 Fault introduction procedure in hardware circuit and avoiding false alarms

A hardware setup was used to simulate specific faults and failures that are known to occur in the semiconductor devices (typically open-circuit failures which usually have a pre-cursor of a rapid short-circuit time prior to bond wires arcing in plastic packages). In the passive components the simulated effects of electrolyte leakage in capacitors (an incipient fault) or rapid turn-to-turn failures in inductor windings is

carried out. These tests are realistic in terms of the overall impact on the performance of the converter circuit. The halving of net capacitance by parallel connected capacitors (and halving of net inductance by series connected inductors) is used to simulate respective fault cases. Whilst the step-changes are not representative of practical failure modes it provides an accelerated test method in order to assess the suitability of the proposed technique to detect and diagnose such faults. However it is acknowledged that the actual failure due to such incipient faults is a slower process potentially occurring over several hundred hours of operation. An alternative method for simulation of a capacitor fault of this type could be to employ differently aged capacitors in parallel, such that the progressive blocking of individual capacitors at designated instants in time would switch to the more 'aged' or worn-out capacitor with prior-estimated (or known) changes in related parameters [127]. This method potentially may provide more accurate capacitor fault data and is anticipated to be applied in future research plans involving the modified-SCA based methodology.

For the switch open and short circuit faults, the faults are introduced when the switch is open and closed respectively. However in a real system it is difficult to predict the switch's state when the passive component fails due to electrolyte leakage or inductor windings fault. In this case though, as fault introduction is manual, it is known that the faults for both the capacitor and inductor have been introduced when the switch S_1 is open (off state).

The counting scheme explained in sub-section 6.3.4 checks for consistency in the data stream thus reducing the possibility of an incorrect diagnosis and accounts for the natural off-state of the switch. Owing to the time scales of the data recorded (in microseconds) and computing the time needed to diagnose the data (below 0.5μs as shown earlier), the counting schemed does not have any major detrimental impact on the speed of diagnosis.

6.5.4 Results of training hardware data on software rules

Sub-section 6.3.5 elaborates on point 2 mentioned in the introduction (6.1), which is essentially testing the feasibility and validity of simulation-data generated rules for an actual data set. One obvious issue with this test result is the 62% classification rate. But on the other hand, a promising outcome is the ability to detect different

types of faults even with a reduced accuracy. Some important points need to be underlined here regarding these tests:

1. It may be possible to have a higher classification rate with changes in parameters such as range, window size, sampling rate, algorithm used etc. Works relating to these aspects though are out of the scope of this thesis. A simultaneous study of using different parameters could be carried out in the future.
2. It is also possible to get varying results by using different types of classifiers. Since the main aim of this research is to form a systematic risk mitigation methodology for the novel SPS which is able to inform work into fault diagnosis, the focus is not on types of data mining algorithms and classifiers.
3. The SIMULINK circuit is an acceptable tool to study the power electronic converter. Even then, there are certain fundamental differences which practically cannot be accounted for when comparing with a real hardware setup. Higher simulation accuracy could be achieved by using a high fidelity system like the RTDS. Further, the RTDS at CAPS-FSU is able to simulate in real-time the entire zonal MVAC system with its vital and non-vital loads. This provides the opportunity to analyse effects of faults at a device/component level on other devices as well as subsystems (zones) and system. Studying such interactions is vital to better understand effects of disturbances within the envisioned zonal SPS.
4. The confusion matrix in fig. 6.15(c) shows a lack of false negatives i.e. a fault is not wrongly indicated when there is none, which is a positive outcome. However, the subsequent studies of training rules of other duty cycles on the 50% duty cycle rule set shows several occurrences of false negatives. It remains to be seen how well the rules perform if encoded and run against a data stream containing random fault and no fault data from different duty cycle operations.

6.5.5 Observability condition and effective series resistance (ESR)

The experiments reported include four measurement signals namely the input current, input voltage and output current and output voltage. All other internal currents and voltages are computed using well known circuit laws and expressions (table 6.1). However, if quantities internal to a circuit are not measurable satisfactorily by indirect methods, then additional sensors may be needed to obtain these measurements. But as of now, the technique proposed does not have an explicit need to utilise more sensors for measurement than the standard number.

For low voltage supplies (typically mV), capacitor ESR can be the greatest contributor to voltage ripple in comparison with the voltage ripple across the

capacitive element of the capacitor. In the case studied in this research, the voltage supply is high enough and the relative contribution to voltage ripple from ESR is relatively small. In general, the technique is capable of including ESR in the algorithm and derivation process. The main change is in the modified-SCA that is performed, wherein ESR could be considered as a resistor in series with the capacitor. This added 'component' changes the determinant obtained from the modified SCA method, though the analysis and derivation technique to obtain the diagnostic indicator is fundamentally the same as proposed.

6.5.6 Scalability issue of proposed method

The advantage of utilising data from local measurements such as input/output measured currents and voltages as well as known circuit parameters avoids the use of additional sensors. Furthermore, the novel diagnosis method presented makes use of this local data for each converter to produce usable features from the determinant of the modified generalised connection matrix for the respective device. This is irrespective of the number of interconnected devices as each converter will have its own matrix. Thus, for a scaled up complex system with many power electronic converters, the modified matrix would be constructed separately for each device to provide localised diagnosis at the component level for each converter. This concept prevents the modified generalised connection matrix from becoming too large to pose any issues relating to computational burden.

6.5.7 Application of proposed method for other DC-DC converters

In order to form a topology independent approach, the proposed methodology is to be applied to DC-DC converter circuits such as the boost (DC-DC step-up) and buck-boost (DC-DC variable) converters. As a demonstration, the proposed modified-SCA approach is detailed in this subsection for the boost and buck-boost converters using the same symbols and representations for the buck converter.

6.5.7.1 Boost converter modified SCA

Fig. 6.21 shows the boost converter circuit in the form similar to fig. 6.5 for the buck converter prior to beginning SCA.

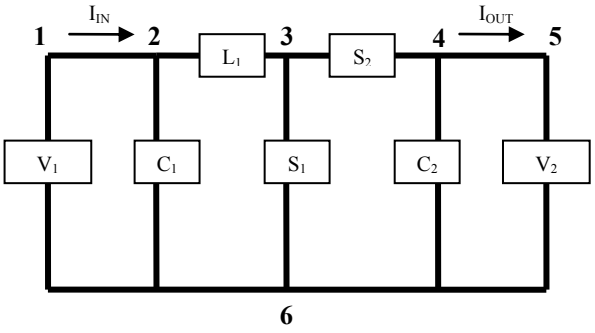


Figure 6.21: Boost converter circuit represented to conduct SCA

For the boost converter, when the switch S_1 is on, there are two separate loops through which a current path can be possible. These are shown in the fig. 6.22 along with their respective directed graphs and connection matrices.

The determinants of the matrices are,

$$ON\_state\_part2 = 1 - V_2^2 - 2I_{C2}^2 \times V_2 - 2I_{C2}^2$$

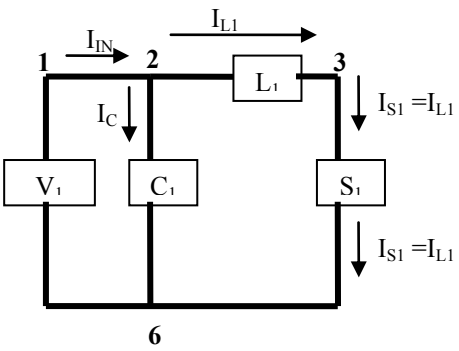
$$ON\_state\_part1 = 1 + I_{C1} \times I_{S1}^2 - I_{C1}^2 - V_1 \times I_{IN} \times I_{S1}^2 + V_1 \times I_{IN} \times I_{C1} - V_1^2$$

Ignoring the terms with higher order parts in both on-state equations, the final usable equation is,

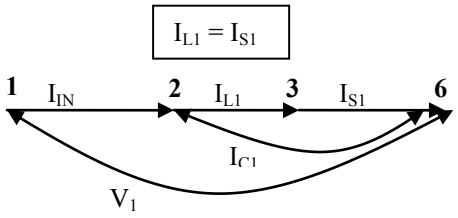
$$|S1on| = V_1 \times I_{IN} \times I_{C1}$$

Equation 6.4

The equivalent circuit during the switch's off state is shown in fig. 6.23 with the directed graph and connection matrix.



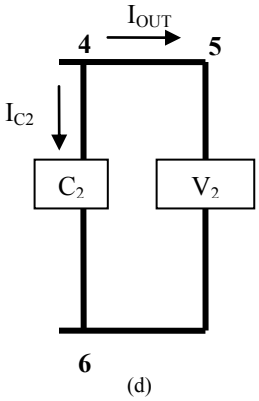
(a)



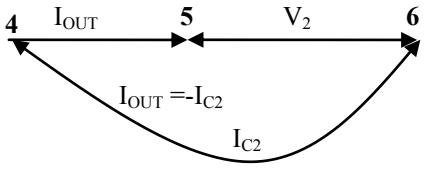
(b)

	1	**2**	**3**	**6**
1	1	I_{IN}	0	V_1
2	0	1	I_{S1}	I_{C1}
3	0	I_{S1}	1	I_{S1}
6	V_1	I_{C1}	0	1

(c)



(d)

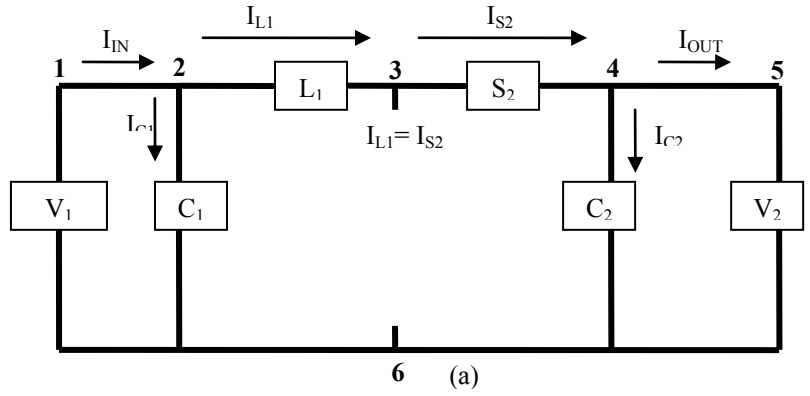


(e)

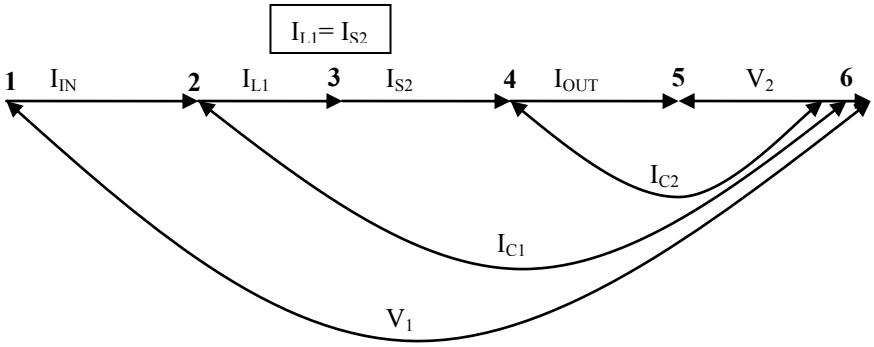
	4	**5**	**6**
4	1	$-I_{C2}$	I_{C2}
5	$-I_{C2}$	1	V_2
6	I_{C2}	V_2	1

(f)

Figure 6.22: (a) and (d) S1-ON state equivalent circuit, in which $I_{S1} = I_{L1}$ (b) and (e) corresponding modified directed graph (c) and (f) corresponding modified generalised connection matrix



(a)



(b)

	1	**2**	**3**	**4**	**5**	**6**
1	1	I_{IN}	0	0	0	V_1
2	0	1	I_{S2}	0	0	I_{C1}
3	0	0	1	I_{S2}	0	0
4	0	0	0	1	I_{OUT}	I_{C2}
5	0	0	0	0	1	V_2
6	V_1	I_{C1}	0	I_{C2}	V_2	1

(c)

Figure 6.23: (a) S1-OFF state equivalent circuit, in which $I_{S2} = I_{L1}$ (b) OFF state modified directed graph (c) OFF state modified generalised connection matrix

The determinant of the matrix is,

$$OFF\_state = 1 - V_1^2 - I_{C1}^2 + V_1 \times I_{IN} \times I_{C1} - I_{C2}^2 - I_{L1}^2 + I_{L1}^2 \times V_1^2 + I_{L1}^2 \times V_2^2 + I_{L1}^2 \times I_{C2} \times I_{OUT} \times V_2 - V_2^2 + V_2 \times I_{OUT} \times I_{C2} + V_2 \times I_{OUT} \times I_{S2}^2 \times V_1 + V_2 \times I_{OUT} \times I_{S2}^2 \times I_{C1} - V_2 \times I_{OUT} \times I_{S2}^2 \times I_{IN} \times V_1$$

Ignoring the terms with higher order parts, the final usable equation is,

$$|S1off| = V_1 \times I_{IN} \times I_{C1} + V_2 \times I_{OUT} \times I_{C2}$$

Equation 6.5

6.5.7.2 Buck-boost converter modified SCA

Using the identical approach, one can deduce the equations for a buck-boost converter. Fig. 6.24 shows the equivalent circuit for such a topology.

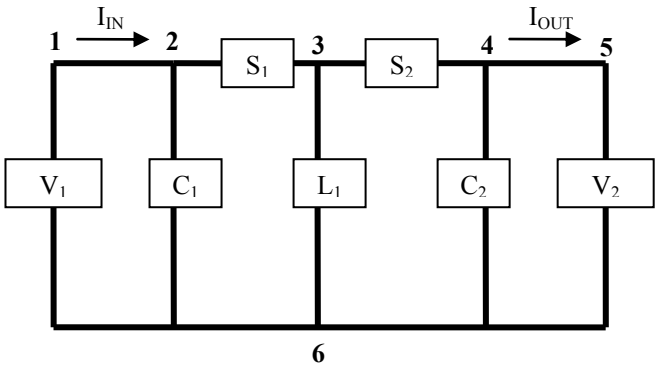


Figure 6.24: Buck-boost converter equivalent circuit

For the buck-boost converter, when the switch S_1 is on, there are two separate loops through which a current path can be possible which are very similar to the corresponding boost converter case. These are shown in the fig. 6.25 along with their respective directed graphs and connection matrices.

The determinants of the matrices are,

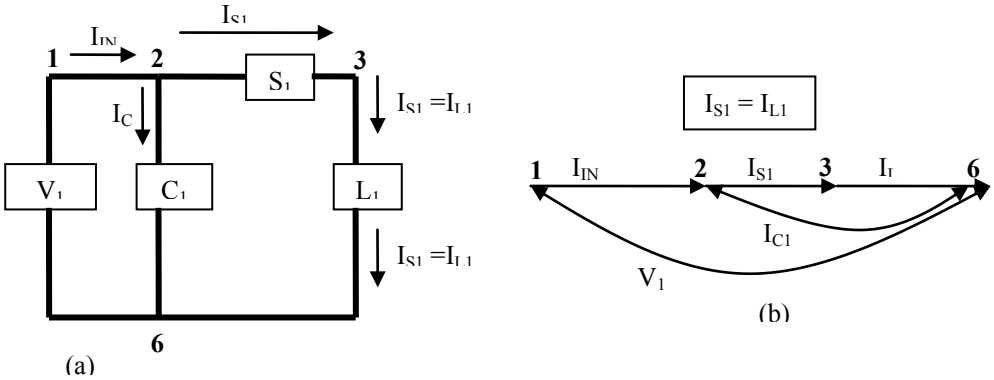
$$ON\_state\_part1 = 1 + I_{C1} \times I_{S1}^2 - I_{C1}^2 - V_1 \times I_{IN} \times I_{S1}^2 + V_1 \times I_{IN} \times I_{C1} - V_1^2$$

$$ON\_state\_part2 = 1 - V_2^2 - 2I_{C2}^2 \times V_2 - 2I_{C2}^2$$

Ignoring the terms with higher order parts in both on-state equations, the final usable equation is,

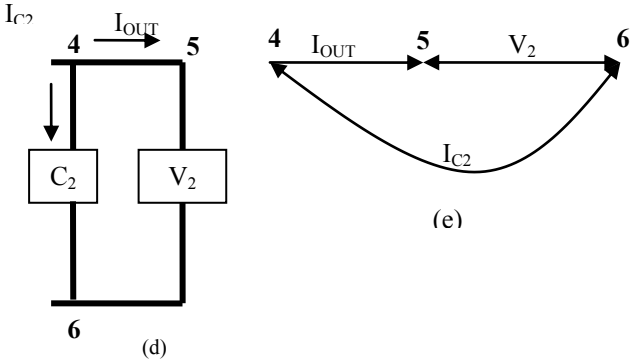
$$|S1on| = V_1 \times I_{IN} \times I_{C1}$$

Equation 6.6



	1	2	3	6
1	1	I_{IN}	0	V_1
2	0	1	I_{S1}	I_{C1}
3	0	I_{S1}	1	I_{S1}
6	V_1	I_{C1}	0	1

(c)

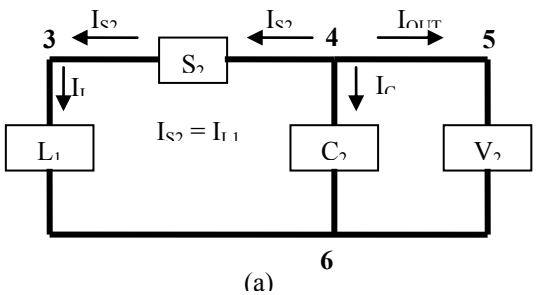


	4	5	6
4	1	$-I_{C2}$	I_{C2}
5	$-I_{C2}$	1	V_2
6	I_{C2}	V_2	1

(f)

Figure 6.25: (a) and (d) S1-ON state equivalent circuit, in which $I_{S1} = I_{L1}$ (b) and (e) corresponding modified directed graph (c) and (f) corresponding modified generalised connection matrix

The equivalent circuit during the switch's off state is shown in fig. 6.26 with the directed graph and connection matrix. The circuit has similarities with the corresponding state for the buck converter.



	3	4	5	6
3	1	0	0	I_{S2}
4	I_{S2}	1	I_{OUT}	I_{C2}
5	0	0	1	V_2
6	0	I_{C2}	V_2	1

(c)

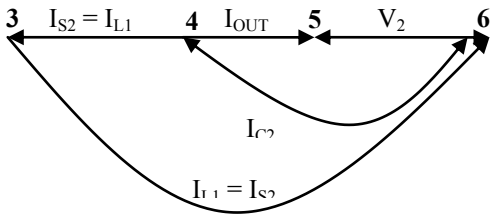


Figure 6.26: (a) S1-OFF state equivalent circuit, in which $I_{S2} = I_{L1}$ (b) OFF state modified directed graph (c) OFF state modified generalised connection matrix

The determinant of the matrix is,

$$OFF\_state = 1 - V_2^2 + V_2 \times I_{OUT} \times I_{C2} - I_{C2}^2 + I_{S2}^2 \times I_{C2}$$

Ignoring the terms with higher order parts, the final usable equation is,

$$|S1off| = V_2 \times I_{OUT} \times I_{C2}$$

Equation 6.7

These equations can be similarly tested using respective hardware setup alongside SIMULINK boost and buck-boost circuits using the same data preparation and classification techniques demonstrated for the buck converter in this chapter. The testing of this modified-SCA based methodology to generate single signal diagnostic indicators is an important part of future research plans.

6.5.8 Expanding rule set for different duty cycles

This chapter mainly focuses on demonstrating the use of the modified-SCA method for the buck converter's special operational case for duty cycle 50%. Similar studies comparing results from software (SIMULINK circuit) and hardware could be conducted for different duty cycles. In such a study, it is reasonable to assume that every duty cycle would produce different sets of rules.

In section 6.4, five values of duty cycle were used and respective rules generated in Weka. The same types of faults were introduced in the SIMULINK circuit for varying values of duty cycle shown in table 6.19. Tables 6.20 to 6.24 show the rules generated for every duty cycle operation of the buck converter circuit. The next six tables (6.25 to 6.30) show the comparison between making each duty cycle rule set the training data and testing it on every remaining rule set. This assessment gives an idea of how well the classifier is able to generalise heuristics over a range of threshold values which vary with difference in duty cycles that in turn affect values of measured voltages and currents used in the |*S1off*| equation. As explained in 6.4, the |*S1off*| equation is used for the assessment because the SIMULINK circuit has an ideal voltage source making the first term in the |*S1on*| equation (refer eq.6.2) zero owing to the computation of I_{C1} which is obtained after differentiating the input voltage, thus essentially becoming the |*S1off*| equation.

The average performance of using the 50% duty cycle rule set for training is higher than other rule sets. The correct classification average rate of 59% is comparable to the study in 6.3.5 for hardware data tested on software rules. This result is promising as it potentially could indicate a similar performance when rules are encoded and tested on data streams in a similar manner.

For further comparative study, the hardware setup used in 6.3.5 could be utilised at different duty cycle values to obtain real circuit data. This data would be used to generate rules using Weka and the same procedure would be followed to train and test heuristics to assess classification performance.

6.6 Summary and conclusions

This chapter demonstrated the use of SCA, a second chosen reliability analysis technique after the previous chapter elaborated the use of FMEA. A modification to conventional SCA was explained which helped produce usable equations, thus

enabling single-signal fault diagnosis for the buck converter. The diagnosis was performed using conditional if-else statements arising out of rules generated from the PART algorithm of data mining software Weka.

The method presented makes use of a model based approach, utilising local measurements without the need for extra sensors to compute a signature. These quantities are used to produce the usable equations derived from the determinant of the GCM that is obtained from the directed graph of the electrical circuit. The modification of using currents and voltages for constructing the directed graph helps to provide quantifiable numbers that aid in diagnosing various component level faults for the buck converter circuits examined. The proposed method tested on a SIMULINK model was verified using hardware data which showed that the signature distinguishes various single fault cases as well as one multiple fault case.

The marginal improvement in accuracy using the $|S1on|$ equation (eq. 6.2) is believed to be due to the fact that it contains two terms as opposed to the single term in the $|S1off|$ (eq. 6.2) equation. This extra information provided to the classifier via the $|S1on|$ equation is believed to increase the rate of discrimination. However, considering computational time and power needed for both computations, the $|S1off|$ equation needs half the efforts compared to the $|S1on|$ equation while providing a negligibly lower classification rate. Thus arguably, one could prefer using the $|S1off|$ equation as well for diagnosis.

Furthermore, there are fundamental differences between the SIMULINK model and hardware circuit owing to the lack of real-world parameters like line inductance, parasitic capacitance and imperfect square wave pulse. But the SIMULINK model used is within acceptable limits to generate additional fault data for cases which would be relatively unsafe to conduct on the hardware circuit for e.g. freewheeling-diode and capacitor short circuit faults.

The proposed technique provides a potential for a fast acting fault diagnostic system. In order to avoid false alarms, an additional piece of code employing a fault indication frequency counter was utilised. In the presented case this code checked batches of the data every 0.5ms and indicated a fault only if more than 10 events occurred every 0.5ms. This accounts for the natural off-state of the switch, which otherwise might trigger a fault indication as an open-circuit. The off-line application

of the heuristics for the switch failures produces permanent fault indications approximately within 4500 samples after the fault is introduced. With a 100ns sampling rate that means the fault is detected within 0.45ms of its introduction. For inductor and capacitor faults, the indication in both cases occurs well before 2200 samples after the fault inception i.e. within 0.22ms of its introduction.

Section 6.3 showed the detailed procedure to perform the modified SCA on a buck converter, prepare data, generate heuristics and test them. Illustrative plots showed the speed of diagnosing different fault cases using the proposed approach. Further, an important test involving cross-training of software rules and testing it on hardware data was undertaken, with the similar approach of checking feasibility of such a test on a real-time hardware data stream. A similar set of illustrative plots showed that this technique is able to diagnose different faults albeit at a marginally higher response time (on average over 0.2ms greater).

Section 6.4 expanded the analytical study to different values of duty cycle. Tables 6.20-6.25 show the generated heuristics for respective duty cycle values for the identical cases as studied before. Furthering the analysis to generalise, tables 6.26-6.30 showed confusion matrices when rule-set for one duty cycle was trained and tested for remaining rule-sets. In this comparison, the average performance for the 50% duty cycle rule-set was highest from the six duty cycle values considered (10%, 25%, 40%, 50%, 75% and 95%). This average correct classification rate of nearly 59% is a promising result which compares well with the performance of comparing with hardware rule-sets.

6.6.1 Future research plans

The proposed approach to generate heuristics for identified pertinent failures could be evaluated with data from sophisticated high fidelity software models. One possible method would be to employ converter models run on a real time digital simulator (RTDS). Advanced models on the RTDS could be able to better simulate circuit behaviour in presence of faults which are relatively unsafe to conduct on hardware circuitry. The data from such RTDS tests could be processed in the manner presented in this chapter to generate heuristics to diagnose pertinent component level faults. This could also positively aid the research into component level diagnostics for power electronic converters in more complex networks and on a real-time basis.

The work reported in this chapter used the classifier to train and test the same type of data separately i.e. either from the model or the hardware circuit. The next step is planned to be the evaluation of the classifier by training it on simulation data from a model and then testing it on data from a hardware setup. This evaluation will test the classifier's ability to generalise and form heuristics that could be encoded for diagnosis purposes as explained previously.

The extension of this research is aimed at conducting a similar approach for the other types of dc-dc converters namely the boost and buck-boost, preliminary analyses for which has been presented in sub-sections 6.5.7.1 and 6.5.7.2 respectively. This is with the view of developing a topology independent approach to detect and diagnose pertinent component level faults. Also, investigation is ongoing for application of the proposed method on a real-time basis for a buck converter hardware circuit. In addition to component level fault diagnostics, the applicability of the proposed method for sub-system (zone) and system-wide faults (for example ground faults) is also an aim for further study.

The next step perhaps is to implement the methodology on a real-time basis for example, using field programmable gate arrays [128]. Fig. 6.14 of subsection 6.3.4 shows the offline process to process data and apply diagnostic rules but also can form the blueprint for real-time diagnosis. Fig. 6.27 shows a fairly similar but lesser detailed form of a setup for real-time diagnostics. The pertinent factor to be assessed in such a real time investigation is the time required to obtain an accurate diagnosis. Keeping in mind that semiconductor faults occur over microseconds (thus practically impossible to prevent) and the other component faults studied (inductor, capacitor issues) typically take several hundred hours until failure, a result-time in the order of minutes seems reasonable.

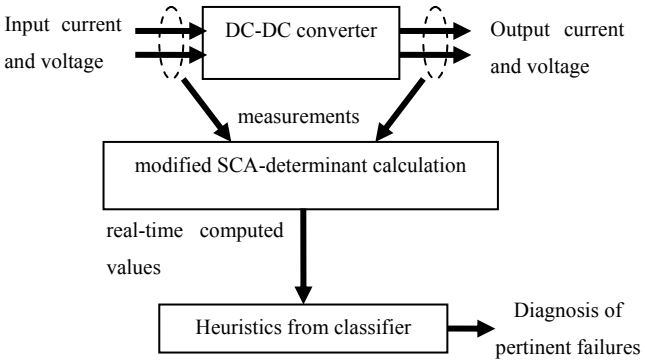


Figure 6.27: A real-time diagnostic setup following proposed modified SCA-based heuristics technique [70]

This research was conducted on a single isolated buck converter circuit with fixed parameters. Applying the proposed diagnosis technique in a grid connected environment is a matter of further investigation. This could ideally be done using the converter with loads (such as motors) the parameters of which can be changed while faults are introduced in the converter circuit. The feasibility of the presented technique will then be tested against issues relating to more complex networks as shown in the line diagram of fig. 6.28.

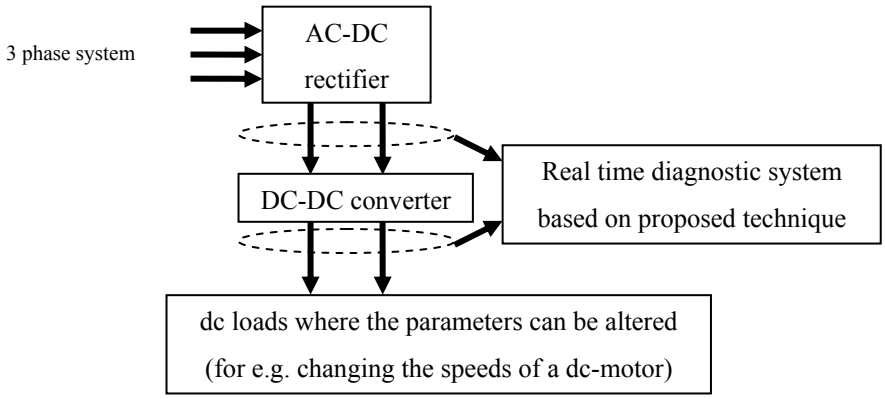


Figure 6.28: System with loads to test feasibility of proposed dc-dc converter diagnosis technique in a more complex set-up [70]

Another aspect of further work is focussed on assessing the generalisation capability of the classifier. This study was shown in section 6.4 which showed tabular results. An ideal outcome would be where rules generated for the 50% duty cycle case are able to distinguish and diagnose studied faults for other duty cycles. Similar variations could be attempted by altering loading and capacitor degradations.

This chapter detailed the use of SCA for this research and explained the research novelty of modifying the conventional analysis. A thorough demonstration of various derivations and tests was provided followed discussion of various issues alongside mentioning the relevance and benefits of the approach. Table 6.31 summarises the derived equations (eq. 6.2 to 6.7) for the three types of dc-dc power electronic converters using the proposed approach.

DC-DC converter type	Switch on-state equation	Switch off-state equation
Buck (step down)	$I_{C1} \times I_{IN} \times V_1 + V_2 \times I_{OUT} \times I$	$V_2 \times I_{OUT} \times I_{C2}$
Boost (step up)	$V_1 \times I_{IN} \times I_{C1}$	$V_1 \times I_{IN} \times I_{C1} + V_2 \times I_{OUT} \times I$
Buck-boost (variable)	$V_1 \times I_{IN} \times I_{C1}$	$V_2 \times I_{OUT} \times I_{C2}$

Table 6.31: Summary of modified-SCA based equations for dc-dc converters

The next chapter summarises this thesis along with future directions in this particular line of research work.

Chapter 7 Research Summary, On-going and Future Directions

7.1 Summary of chapters

This thesis details research conducted in the research arena of notional zonal SPS architectures. Specifically, the work reported in this thesis dealt with the development of a FACS for a novel SPS architecture by proposing the formulation of a systematic and generalised methodology incorporating FMEA, SCA, model based systems and heuristic generation. Chapter 1 clearly mentions the background of this research arena along with the justification and novelty of this particular thesis. This chapter presents a summary of the thesis and sheds some light on ongoing and future research plans within this field.

Chapter 2 offers a comprehensive literature review related to the major trends of work within this arena. As highlighted in the references, a major research thread is system reconfiguration, restoration and automatic mitigation of faults at the system level. Such faults are typically ground faults or faults at the main motor/generator/prime mover side. Research into the need for autonomous high level diagnostics providing decision support assistance to the reduced numbers of on-board crew, giving fault information and their risk mitigation for component level faults has been relatively ignored. This gap in research led the authors to conduct studies into component level diagnostics for the dc-dc power electronic converter since the proposed architectures are envisioned to include a large number of power electronic sub-systems which as of now is a relatively new and unproven technology for warships.

Chapter 3 mentions significant research within the power electronics domain. Power electronics research is vital owing to the fact that a large number of power electronics devices are anticipated to be used onboard the envisioned SPS. Further, this chapter elaborates on component level diagnostics and fault accommodation strategies, both of which are an important side to system-level risk assessment studies.

Chapter 4 emphasises the need to look into reliability analyses techniques for risk assessment aboard the notional SPS architecture. It is reasoned that FMEA forms the

logical starting point for a novel system where one can build understanding about types of faults and failures at various levels of the overall system. SCA is also outlined as a reliability analysis technique to be utilised for this research work. Chapter 5 shows detailed and exhaustive FMEA conducted for the novel SPS studied. An advantageous outcome of FMEA is a list of faults, remedial action for which can be prioritised based on severity. Further, FMEA at different levels of detail; F-FMEA at the system and subsystem level and H-FMEA at the component level helped narrow down this research to focus on the buck converter circuit. Once the buck converter which provides power into each zone of the SPS is identified and chosen as a critical piece of equipment, the next step was to assess various faults occurring within it and find means of diagnosing them.

Chapter 6 forms a key aspect of the novelty of this thesis, where the modification to conventional SCA is explained yielding in usable equations to distinguish faults. The proposed approach beginning with FMEA, feeds further research by providing information about pertinent failures at all levels (FMEA can be conducted at system, sub-system and device/component level), while the modified SCA methodology provides diagnosable features for faults for the shown buck converter type of circuit. Undertaken together as part of a systematic methodology as proposed, the FMEA and modified-SCA approach can be extended to other power electronic systems to provide component/device level fault data with diagnostics for informed decision making and remedial action. It could also potentially provide diagnosable features for zone and system level faults, which forms part of further research. Besides the buck, modified-SCA is also demonstrated on boost and buck-boost converters in an attempt to generalise the strategy for dc-dc converters. Fig.7.1 illustrates the methodology proposed in this research work centred on FMEA and modified-SCA.

7.2 Re-emphasizing benefits of FMEA

As reasoned through chapters 4 and 5, FMEA being a well established reliability analysis method is justified as a logical and feasible technique to be used for understanding faults and failures in a novel system (this case the zonal SPS). This thesis uses FMEA for the studied SPS using the tabular format and procedures mentioned in literature [71-74]. Following the conventions numerous beneficial outcomes were obtained that helped direct and inform the ensuing steps in this research.

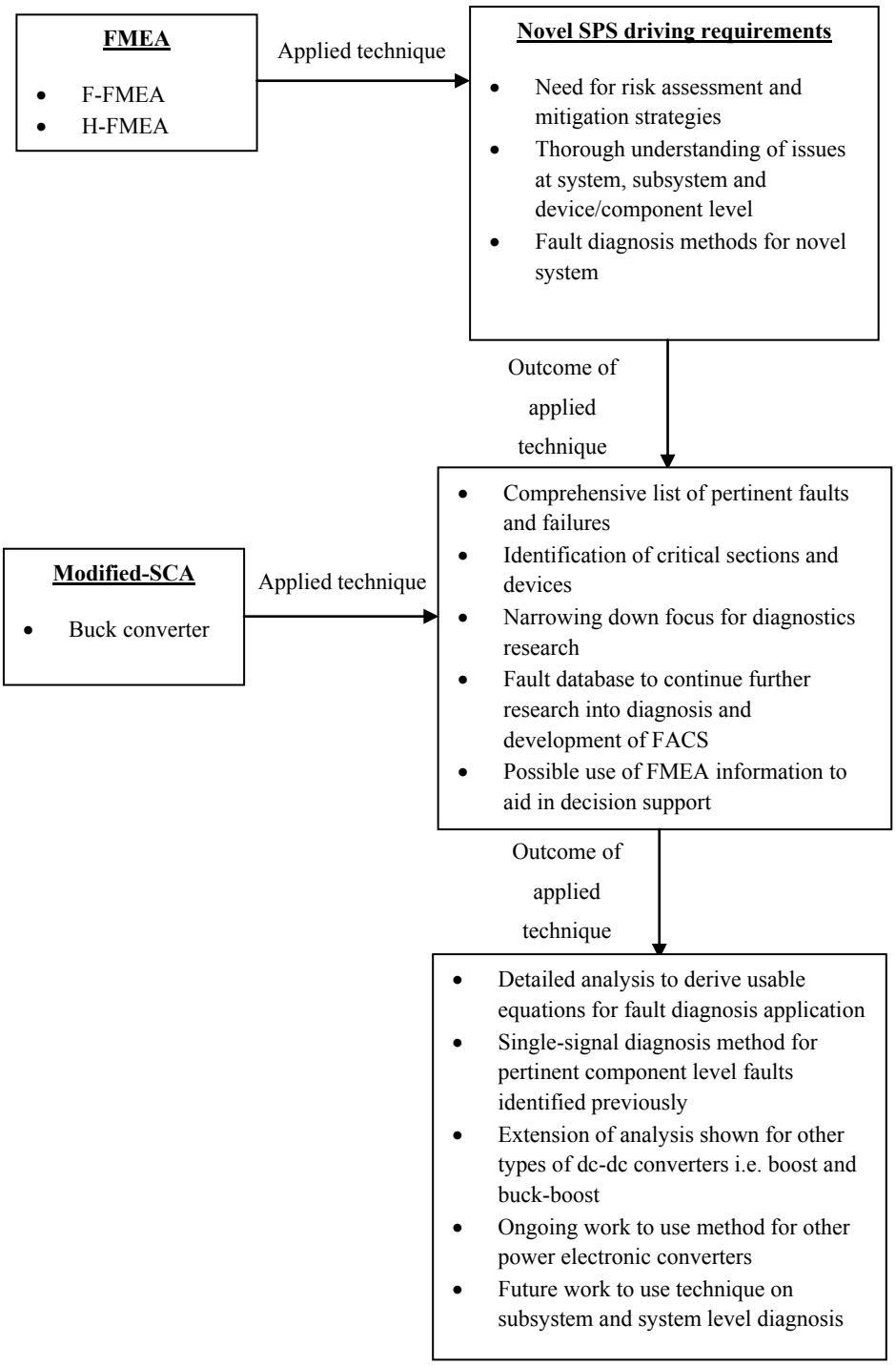


Figure 7.1: Methodology proposed in this thesis to address driving requirements of research arena

It is vital to re-emphasise the systematically progressive benefits underpinned by applying FMEA for this research:

1. A thorough understanding of the system's architecture, connectivity, and devices is obtained in the initial stages of FMEA as one begins breaking the overall network into smaller parts.
2. F-FMEA offers an understanding of fundamental functions of the subsystem thereby enabling one to gather information about basic dependencies of one subsystem on another. This information is further used to form the first high-level FMEA which helps identify the most critical devices and subsystems.
3. H-FMEA builds upon the understanding gained previously by providing information on component level faults within identified critical devices. This subpart of FMEA completes the analysis in the process informing research on pertinent failures at a functional (system) level as well as component (within device) level.
4. One therefore has an exhaustive list of failures that are known to occur within the notional SPS, with their respective severities. This enables further ranking of these issues so that they could be dealt with systematically. A direct application of this outcome was demonstrated in this thesis (chapter 5 and mainly 6) where the buck converter was chosen as a vital device followed by pertinent component level fault diagnosis studies.
5. Besides providing an understanding of critical sections/devices and pertinent faults, the FMEA database contains a detailed list of all known failures, causes and effects. To truly develop a comprehensive FACS capable of handling all known failures, there is need to address issues occurring within various other devices, subsections etc. of the network. For this purpose, one can utilise the FMEA information for future research.

Simply put, using FMEA not only helps begin and continue the research presented in this thesis, but also helps inform further research in this arena.

7.3 Revisiting the research novelty

Section 1.3 briefly touched upon the novelty of this research work. Chapter 4 suggests the application of FMEA and SCA for SPS risk assessment which paves the way for a thorough FMEA conducted on the system studied, shown in chapter 5. These preliminary studies to enable better understanding of risks aboard the notional SPS by using reliability analyses is a novel approach within this particular field that is shown to inform and direct further research into fault diagnosis. As mentioned, after chapter 5 details the application of the proposed systematic approach utilising

FMEA, chapter 6 is pivotal in further explaining the novelty of this research work using modified SCA. Overall, the novelty and contributions of this work is systematically explained through chapters 4, 5, 6 and the proposed methodology can be illustrated as shown in fig.7.1.

In chapter 6, a thorough explanation of the rationale for using SCA and its modification is explained to show a new approach in using a well established circuit-design method to aid in distinguishing component level faults. In a progressive manner (all of section 6.3), the chapter builds upon the idea of using well known SCA to produce numerical results by introducing actual circuit quantities in the derived equations. This data is shown to be useful to generate rules that can be encoded to differentiate faults. The classifier used employs the PART [13] algorithm in data-mining tool Weka[14] and outputs easily readable rules that can be utilised by formulating IF-THEN-ELSE statements in any coding language.

An offline testing of the rules generated is performed first on the same type of data i.e. rules generated using hardware/software data are used offline on a similar data stream. This helped ensure consistency and accuracy of the rules. Also, it helped give an idea of the time taken to indicate the existence of the fault. Plots for the various fault cases studied, compared with the output voltage show details of fault introduction and its indication instance (tables 6.9-6.12).

Then, an important check is performed, wherein rules trained on software data are tested on hardware data (section 6.3.5). This is a vital test, which aims to check feasibility of the following crucial aspect:

Whether or not the software data can be used as a general guide to anticipate issues within actual hardware setups.

The results show, that although the data classification rate is 62%, when the trained and tested rules are encoded, they are still able to indicate the occurrence of all the five faults introduced namely:- switch short circuit, switch open circuit, inductor fault, capacitor fault and inductor plus capacitor multiple fault. The reasoning presented for this relatively low classification rate in 6.4.4 mainly emphasises the need for a more detailed simulation tool (perhaps RTDS) and/or use of different classification algorithms, both aspects of which are outside the scope of

this particular thesis. Along with this issue, section 6.4 sheds light on other practical issues regarding the proposed approach.

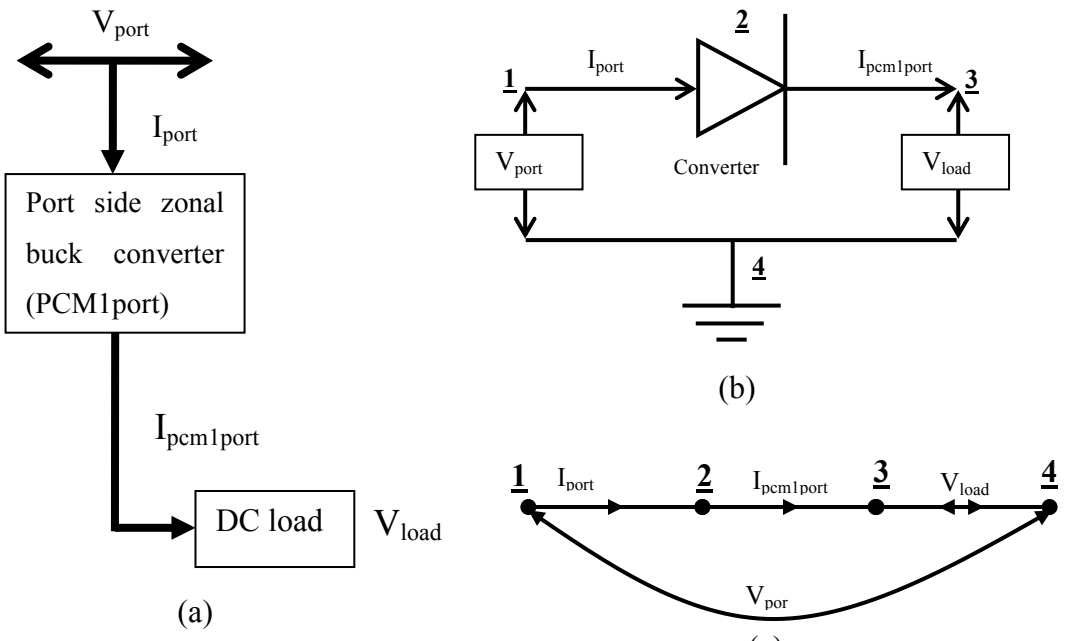
In summary and with reference to fig.7.1 the advantages of using the proposed approach for novel SPS FACS development are:

- Use of FMEA, ensures a thorough understanding of faults and risks at all system levels simultaneously producing valuable information databases which could be used for further continuation of this research.
- Use of modified SCA produces usable equations for vital devices to produce a single-signal fault diagnostic capability.
- The novelty is shown to be applicable to other types of dc-dc converters in subsection 6.4.7 where a similar approach yields sets of equations that can be targeted for further hardware data backed tests.
- There is scope of using the modified-SCA based novelty on the overall system that is broken down into smaller sub-parts by FMEA, where a similar current and voltage centred approach can be used to form usable equations. This is illustrated as an example in fig.7.2 wherein half of a typical modelled zone is shown on which the proposed approach is used.
- The proposed systematic methodology holds promise to enable development of the overall FACS for the notional SPS incorporating well developed research stemming from established reliability analyses as well as artificial intelligence based techniques.
- The detailed information gathered during this research can be used to form a reliable decision support system for onboard crew which is an added advantage.

7.4 Ongoing research that extends from this thesis

Current research focuses on extending the novelty of this work into forming single signal diagnosis for the remaining devices and sections of the studied SPS. Fig. 7.2 is an approximate example of one such application used at a zonal level. Ongoing work follows the methodology proposed in this research using modified-SCA followed by heuristic classification.

Major issues to be addressed in the ongoing work relate to modelling high fidelity simulations at a zonal level that incorporate detailed reflections of system level faults. Since the device level modified-SCA is complete, it is interesting to analyse how the component level faults affect the normal parameters across a zone. This brings into play aspects such as fault propagation, which are not possible to study on isolated tests conducted for this thesis.



	1	2	3	4
1	1	I_{port}	0	V_{port}
2	0	1	$I_{pcm1port}$	0
3	0	0	1	V_{load}
4	V_{port}	0	V_{load}	1

Determinant of GCM = $1 - V_{load}^2 - I_{port} \times I_{pcm1port} \times V_{port} \times V_{load} - V_{port}^2$

Meaningful term = $-\boldsymbol{I_{port}} \times \boldsymbol{I_{pcm1port}} \times \boldsymbol{V_{port}} \times \boldsymbol{V_{load}}$

(d)

Figure 7.2: Example of modified-SCA based approach applied at a zonal level (subsystem) (a)Port-side load supply connection (b) Equivalent diagram for modified-SCA (c) Directed graph (d) GCM and corresponding derivation of usable terms

Another aspect of generalising the presented research is to use the methodology on evolving notional SPS architectures such as the newer MVDC system (medium voltage direct current). These developments are promising in order to achieve the overall aim of creating an intelligent, robust FACS.

7.5 Future research

The proposed zonal SPS architecture is at a developmental stage which undergoes minor to major changes periodically as new research is applied. This fact makes it a challenge to provide a generic methodology to assess risks that is easily extendible to modifications to the fundamental architecture. As a result, further research within this field using the methodology proposed in this work has distinct parts as follows:

- **Existing notional SPS architecture** – The work detailed in this thesis uses FMEA and SCA to focus research onto the buck converter. It is vital to extend the same approach to other parts of the system listed within the FMEA's critical sections/devices and also onto the zone and system levels. This will help assess whether the proposed methodology can be generalised to other parts of the same studied system. In the process, it may be necessary to make modifications that could be incorporated iteratively.
- **New notional SPS architecture** – This thesis studied the MVAC zonal system while also mentioning the MVDC version. Once the proposed methodology is sufficiently generalised, the next step is to apply it for the newer MVDC zonal SPS. However, it is possible to conduct research using the proposed FMEA-SCA led methodology simultaneously on both architectures.

Within both the above mentioned parts, there are some common threads which need further exploration:

- **Modelling and simulation studies** – This is a vital branch of future research as its outcomes will enable reliable fault studies to be carried out on sophisticated simulation models that will closely represent the actual system.
- **Testing classifiers** – A large number of tools could be used to process the data generated. A meticulous study needs to be undertaken to search for the best performing classifiers which are able to produce most favourable results regarding time needed and ease of encoding rules.

Although the major focus regarding notional SPS is on continuing the evolution of current fault diagnosis and risk mitigation techniques for different devices, sections, architectures etc. as mentioned earlier, an important alternative is development of intelligent decision support capabilities. Along with having an accurate FACS, it is vital to aid onboard crew by providing them with clear, concise and correct assistance for decision-making and remedial-action.

The significant amount of fault related data obtained from FMEA and SCA could be put to use by employing methods used in a major topic within AI known as

natural language processing (NLP) to support decision making [129]. A number of NLP applications can be seen to perform successfully in biomedical applications [130].

The importance of looking at NLP for user support in engineering systems with increased complexity is elaborated by Ryan in [131]. Research in [132] is a comprehensive case study on application of NLP for industrial requirements. A detailed comparison of various techniques is conducted for the purpose of retrieving useful information from the subject related databases.

Well established techniques such as latent semantic analysis (LSA) [133, 134] and support vector machines (SVM) [135] to name a few, have been extensively used to develop reliable human user interaction modules. Ongoing research in this field aims at assessing various NLP techniques such as the already mentioned LSA, SVM by introducing modifications as appropriate to the type of data (engineering, medical etc.)

Such developments within NLP when reviewed in the context of a notional SPS having rich faults and risks related information offer a promising prospect for providing FACS with able decision support. Indeed, rigorous and thorough research specific to the use of NLP for the notional SPS is needed, which may be one of the threads followed in the near future along with work in fault diagnosis.

7.6 Overall conclusions

The research presented in this thesis is aimed at developing a robust FACS as the gross outcome. Notional SPS being a relatively new field of research, it was imperative to obtain an understanding of the risks within the architecture proposed and associated effects. Thereafter, work could be commenced on finding ways of mitigating or even eliminating these known risks.

For this purpose, FMEA was used to begin breaking the overall system down to better understand risks such as faults and failures that could occur at not only system/subsystem levels but also at device/component levels. Outcomes of FMEA helped inform and focus further research into finding ways to diagnose pertinent issues within critical devices. In this research, the buck converter was chosen for fault diagnosis related analysis.

Analysis on the buck converter used a modified version of SCA, which formed the main novelty of this research. The modified-SCA led analysis, helped produced single signal diagnosis capabilities for various component level faults that could happen within standard buck converter circuit. The data used for tests came from both software (SIMULINK) model and a hardware setup. Verification of the software model was carried out through comparisons which were followed by generating rules using the PART classification algorithm in Weka for each circuit. The classification results showed a high accuracy for differentiating various operating cases from each other.

The important cross-validation test was then carried out, wherein rules generated from software data were tested on corresponding hardware data. Although the accuracy of classification results were significantly lower than the previous case, encoding the rules however showed that they could still differentiate various different types of data (operating cases). This result was promising for conducting further research on the proposed methodology.

A vital part of rule encoding lay in avoiding false alarms by adopting a fault indication frequency check. This accounted for the natural off-state of the circuit as well as excessive fault triggers. Overall, this single-signal diagnosis was shown to be a fast scheme with no need for more than the usual required number of sensors. The entire proposed methodology can be summarised through fig. 7.1. This thesis also adequately addressed certain issues and possible remedies which are part of ongoing work.

Currently, refinements to power electronic device models is an important aspect to produce better quality simulation data which can compare well with actual hardware results.

Present work aims at continuing studies into better understanding risks for the notional SPS and its newer versions. Major aspects of ongoing work and planned studies in the near future are elaborated in 7.5. Once a thorough and satisfactory understanding of risks affecting the novel SPS is gained, the next step is aimed at developing multi-agent systems for computer-aided real-time condition monitoring and fault management (diagnosis and possible prognosis). Eventually, studies to

provide decision support utilising information from previous work within this field will be conducted, possibly making use of NLP techniques.

References

[1] C. G. Hodge and D. J. Mattick, "The electric warship," *Trans. IMarE.*, vol. 108, 1996.

[2] C. G. Hodge and D. J. Mattick, "The electric warship II," *Trans. IMarE.*, vol. 109, 1997.

[3] C. G. Hodge and D. J. Mattick, "The electric warship III," *Trans. IMarE.*, vol. 110, 1998.

[4] C. G. Hodge, D. J. Mattick, and J. M. Newell, "The electric warship IV," *Trans. IMarE.*, vol. 111, 1999.

[5] C. G. Hodge and D. J. Mattick, "The electric warship V," *Trans. IMarE.*, vol. 112, 2000.

[6] C. G. Hodge and D. J. Mattick, "The electric warship VI," *Trans. IMarE.*, vol. 113, 2001.

[7] G. T. Little, S. S. Young, and J. M. Newell, "The electric warship VII - the reality," *Marine Design and Operations*, vol. 82, 2002.

[8] C. G. Hodge, "Modern applications of power electronics to marine propulsion systems," in *14th International Symposium on Power Semiconductor Devices and ICs*, 2002, pp. 9 - 16.

[9] T. Ericsen, N. Hingorani, and Y. Khersonsky, "Power electronics and future marine electrical systems," *IEEE Trans. Industry Applications*, vol. 42, pp. 155-163, 2006.

[10] K. P. Logan, "Intelligent Diagnostic Requirements of Future All-Electric Ship Integrated Power System," *IEEE Trans. Industry Applications*, vol. 43, pp. 139-149, 2007.

[11] E. L. Zivi, "Integrated shipboard power and automation control challenge problem," presented at the IEEE Power Engineering Society Summer Meeting, 2002.

[12] J. de Kleer, "How circuits work," *Artificial Intelligence*, vol. 24, pp. 205-280, 1984.

[13] Y. Cao and J. Wu, "Dynamics of projective adaptive resonance theory model: the foundation of PART algorithm," *IEEE Trans. Neural Networks*, vol. 15, pp. 245-260, 2004.

[14] *Weka 3: Data Mining Software in Java*. Available: http://www.cs.waikato.ac.nz/ml/weka/

[15] J. V. Amy, Jr., "Considerations in the design of naval electric power systems," presented at the IEEE Power Engineering Society Summer Meeting, 2002.

[16] H. Hegner and B. Desai, "Integrated fight through power," presented at the IEEE Power Engineering Society Summer Meeting, 2002.

[17] J. G. Ciezki and R. W. Ashton, "Selection and stability issues associated with a navy shipboard DC zonal electric distribution system," *IEEE Trans. Power Delivery*, vol. 15, pp. 665-669, 2000.

[18] J. A. Momoh, S. S. Kaddah, and W. Salawu, "Security assessment of DC zonal naval-ship power system," presented at the Large Engineering Systems Conference on Power Engineering, 2001.

[19] S. Sankar and N. N. Schulz, "Intelligent Placement of Meters / Sensors for Shipboard Power System Analysis," presented at the IEEE Electric Ship Technologies Symposium, 2007.

[20] A. K. Srivastava, J. L. Bastos, N. N. Schulz, and H. L. Ginn, "AC/DC Power System Modeling and Analysis for Shipboard Applications," presented at the IEEE Power Engineering Society General Meeting, 2007.

[21] P. Pant, K. Schoder, and A. Feliachi, "An Integrated Electric Shipboard Power System Testbed," presented at the IEEE Electric Ship Technologies Symposium, 2007.

[22] A. Feliachi, K. Schoder, S. Ganesh, and H.-J. Lai, "Distributed control agents approach to energy management in electric shipboard power system," presented at the IEEE Power Engineering Society General Meeting, 2006.

[23] K. Huang, S. K. Srivastava, D. A. Cartes, and M. Sloderbeck, "Intelligent Agents Applied to Reconfiguration of Mesh Structured Power Systems," presented at the International Conference on Intelligent Systems Applications to Power Systems, 2007.

[24] J. A. Momoh, "Navy ship power system restoration using multi-agent approach," presented at the IEEE Power Engineering Society General Meeting, 2006.

[25] K. L. Butler, N. D. R. Sarma, and V. Ragendra Prasad, "Network reconfiguration for service restoration in shipboard power distribution systems," *IEEE Trans. Power Systems*, vol. 16, pp. 653-661, 2001.

[26] K. L. Butler-Purry and N. D. R. Sarma, "Self-healing reconfiguration for restoration of naval shipboard power systems," *IEEE Trans. Power Systems*, vol. 19, pp. 754-762, 2004.

[27] S. Srivastava and K. L. Butler-Burry, "Expert-system method for automatic reconfiguration for restoration of shipboard power systems," in *IEEE Proc. Generation, Transmission and Distribution*, pp. 253-260, 2006.

[28] M. E. Baran and N. Mahajan, "System reconfiguration on shipboard DC zonal electrical system," presented at the IEEE Electric Ship Technologies Symposium, 2005.

[29] J. M. Solanki and N. N. Schulz, "Using intelligent multi-agent systems for shipboard power systems reconfiguration," in *The 13th International Conference on Intelligent Systems Application to Power Systems*, pp. 6-10, 2005.

[30] K. C. Nagaraj, J. Carroll, T. Rosenwinkel, A. Arapostathis, M. Grady, and E. J. Powers, "Perspectives on Power System Reconfiguration for Shipboard Applications," presented at the IEEE Electric Ship Technologies Symposium, 2007.

[31] Z. Ding, S. K. Srivastava, D. A. Cartes, and S. Suryanarayanan, "Dynamic Simulation-Based Analysis of a New Load Shedding Scheme for a Notional Destroyer-Class Shipboard Power System," *IEEE Trans. Industry Applications*, vol. 45, pp. 1166-1174, 2009.

[32] L. Liu, K. P. Logan, D. A. Cartes, and S. K. Srivastava, "Fault Detection, Diagnostics, and Prognostics: Software Agent Solutions," *IEEE Trans. Vehicular Technology*, vol. 56, pp. 1613-1622, 2007.

[33] M. E. Baran and N. R. Mahajan, "DC distribution for industrial systems: opportunities and challenges," *IEEE Trans. Industry Applications*, vol. 39, pp. 1596-1601, 2003.

[34] R. Jayabalan and B. Fahimi, "Fault diagnostics in naval shipboard power system for contingency management and survivability," presented at the IEEE Electric Ship Technologies Symposium, 2005.

[35] R. Jayabalan and B. Fahimi, "Naval shipboard power system," presented at the IEEE Conference on Vehicle Power and Propulsion, 2005.

[36] K. Nareshkumar, M. A. Choudhry, J. Lai, and A. Feliachi, "Application of multi-agents for fault detection and reconfiguration of power distribution systems," presented at the IEEE Power and Energy Society General Meeting, 2009.

[37] E. M. Davidson, S. D. J. McArthur, S. K. Srivastava, and D. A. Cartes, "Development of an integrated control and monitoring architecture for shipboard power systems," presented at the IMarEST. All Electric Ship Conference, 2007.

[38] J. A. Momoh and A. S. Ishola-Salawu, "A new arcing fault modeling and detection technique for navy IPS power system," presented at the IEEE Power Engineering Society General Meeting, 2006.

[39] Y. Pan, M. Steurer, and T. Baldwin, "Feasibility study of noise pattern analysis based ground fault locating method for ungrounded DC shipboard power distribution system," presented at the IEEE Electric Ship Technologies Symposium, 2009.

[40] Y. Pan, M. Steurer, and T. L. Baldwin, "Ground Fault Location Testing of a Noise-Pattern-Based Approach on an Ungrounded DC System," *IEEE Trans. Industry Applications*, vol. 47, pp. 996-1002, 2011.

[41] M. Baran and N. R. Mahajan, "PEBB Based DC System Protection: Opportunities and Challenges," presented at the IEEE PES Transmission and Distribution Conference and Exhibition, 2006.

[42] M. E. Baran, S. Teleke, and S. Bhattacharya, "Overcurrent Protection in DC Zonal Shipboard Power Systems using Solid State Protection Devices," presented at the IEEE Electric Ship Technologies Symposium, 2007.

[43] R. Jayabalan and B. Fahimi, "Monitoring and fault diagnosis of cascaded multiconverter systems in hybrid electric vehicles," presented at the IEEE Conference on Vehicle Power and Propulsion, 2005.

[44] W. G. Fenton, T. M. McGinnity, and L. P. Maguire, "Fault diagnosis of electronic systems using intelligent techniques: a review," *IEEE Trans. Systems, Man, and Cybernetics, Part C: Applications and Reviews*, vol. 31, pp. 269-281, 2001.

[45] F. W. Fuchs, "Some diagnosis methods for voltage source inverters in variable speed drives with induction machines - a survey," presented at the IEEE 29th Annual Conference of the Industrial Electronics Society, 2003.

[46] K. Rothenhagen and F. W. Fuchs, "Performance of diagnosis methods for IGBT open circuit faults in three phase voltage source inverters for AC variable speed drives," presented at the European Conference on Power Electronics and Applications, 2005.

[47] B. Lu and S. Sharma, "A Literature Review of IGBT Fault Diagnostic and Protection Methods for Power Inverters," *IEEE Trans. Industry Applications*, vol. 45, pp. 1770-1777, 2009.

[48] P. Lezana, R. Aguilera, and J. Rodriguez, "Fault Detection on Multicell Converter Based on Output Voltage Frequency Analysis," *IEEE Trans. Industrial Electronics*, vol. 56, pp. 2275-2283, 2009.

[49] Y. L. Murphey, M. A. Masrur, Z. Chen, and B. Zhang, "Model-based fault diagnosis in electric drives using machine learning," *IEEE/ASME Trans. Mechatronics*, vol. 11, pp. 290-303, 2006.

[50] M. A. Masrur, Z. Chen, B. Zhang, and L. Murphey, "Model-Based Fault Diagnosis in Electric Drive Inverters Using Artificial Neural Network," presented at the IEEE Power Engineering Society General Meeting, 2007.

[51] M. A. Masrur, Z. Chen, and Y. Murphey, "Intelligent diagnosis of open and short circuit faults in electric drive inverters for real-time applications," *IET Power Electronics*, vol. 3, pp. 279-291, 2010.

[52] S. Khomfoi and L. M. Tolbert, "Fault diagnostic system for a multilevel inverters using a neural network," *IEEE Trans. Power Electronics*, vol. 22, pp. 1062–1069, 2007.

[53] S. Khomfoi and L. M. Tolbert, "Fault Diagnosis and Reconfiguration for Multilevel Inverter Drive Using AI-Based Techniques," *IEEE Trans. Industrial Electronics,* vol. 54, pp. 2954-2968, 2007.

[54] F. Zidani, D. Diallo, M. Benbouzid El Hachemi, and R. Nait-Said, "A Fuzzy-Based Approach for the Diagnosis of Fault Modes in a Voltage-Fed PWM Inverter Induction Motor Drive," *IEEE Trans. Industrial Electronics,* vol. 55, pp. 586-593, 2008.

[55] F. Wang, R. Lai, X. Yuan, F. Luo, R. Burgos, and D. Boroyevich, "Fault Detection and Protection of Three-Level Neutral-Point-Clamped PWM Voltage Source Converters," presented at the IEEE Industry Applications Society Annual Meeting, 2008.

[56] F. Wang, R. Lai, X. Yuan, F. Luo, R. Burgos, and D. Boroyevich, "Failure-Mode Analysis and Protection of Three-Level Neutral-Point-Clamped PWM Voltage Source Converters," *IEEE Trans. Industry Applications,* vol. 46, pp. 866-874, 2010.

[57] S. Y. Kim, K. Nam, H.-S. Song, and H.-G. Kim, "Fault Diagnosis of a ZVS DC–DC Converter Based on DC-Link Current Pulse Shapes," *IEEE Trans. Industrial Electronics,* vol. 55, pp. 1491-1494, 2008.

[58] A. M. R. Amaral and A. J. M. Cardoso, "Use of ESR to predict failure of output filtering capacitors in boost converters," presented at the IEEE International Symposium on Industrial Electronics, 2004.

[59] A. M. R. Amaral and A. J. M. Cardoso, "A Simple Offline Technique for Evaluating the Condition of Aluminum–Electrolytic–Capacitors," *IEEE Trans. Industrial Electronics,* vol. 56, pp. 3230-3237, 2009.

[60] Y.-M. Chen, H.-C. Wu, M.-W. Chou, and K.-Y. Lee, "Online Failure Prediction of the Electrolytic Capacitor for LC Filter of Switching-Mode Power Converters," *IEEE Trans. Industrial Electronics,* vol. 55, pp. 400-406, 2008.

[61] M. I. Afroz, D. M. Divan, R. G. Harley, and T. G. Habetler, "Real-Time Condition Monitoring of the Electrolytic Capacitors for Power Electronics Applications," presented at the IEEE 22nd Annual Applied Power Electronics Conference, 2007.

[62] M. M. Polycarpou and A. T. Vemuri, "Learning methodology for failure detection and accommodation," *IEEE Control Systems,* vol. 15, pp. 16-24, 1995.

[63] M. M. Polycarpou, "Fault accommodation of a class of multivariable nonlinear dynamical systems using a learning approach," *IEEE Trans. Automatic Control,* vol. 46, pp. 736-742, 2001.

[64] Y. Zhang and J. Jiang, "Integrated active fault-tolerant control using IMM approach," *IEEE Trans. Aerospace and Electronic Systems,* vol. 37, pp. 1221-1235, 2001.

[65] G. G. Yen and L.-W. Ho, "Online Multiple-Model-Based Fault Diagnosis and Accommodation," *IEEE Trans. Industrial Electronics*, vol. 50, pp. 296-312, 2003.

[66] R. R. Soman, E. M. Davidson, and S. D. J. McArthur, "Using functional failure mode and effects analysis to design the monitoring and diagnostics architecture for the zonal MVDC shipboard power system," presented at the IEEE Electric Ship Technologies Symposium, 2009.

[67] A. J. Mair, R. R. Soman, E. M. Davidson, S. K. Srivastava, K. Schoder, S. D. J. McArthur, *et al.*, "Intelligent distributed control for shipboard power systems based on fault diagnosis and condition monitoring," presented at the IMarEST. Engine As A Weapon III, 2009.

[68] A. J. Mair, R. R. Soman, E. M. Davidson, S. K. Srivastava, K. Schoder, S. D. J. McArthur, *et al.*, "Fault Classification and Accommodation in Shipboard Power Systems," in *International Simulation Conference*, 2009.

[69] A. J. Mair, R. R. Soman, P. C. Baker, E. M. Davidson, S. K. Srivastava, K. Schoder, *et al.*, "Progress in the development of adaptive control for shipboard power systems through modelling and simulations," in *Grand Challenges in Modelling and Simulation Conference*, 2010.

[70] R. R. Soman, E. M. Davidson, S. D. J. McArthur, J. E. Fletcher, and T. Ericsen, "Model-based methodology using modified sneak circuit analysis for power electronic converter fault diagnosis," *IET Power Electronics*, vol. 5, pp. 813-826, 2012.

[71] R. J. Mikulak, R. McDermott, and M. Beauregard, *The Basics of FMEA*, 2nd ed.: CRC Press.

[72] B. M. Tashjian, "The failure modes and effects analysis as a design tool for nuclear safety systems," *IEEE Trans. Power Apparatus and Systems*, vol. 94, pp. 97-103, 1975.

[73] J. M. Legg, "Computerized Approach for Matrix-Form FMEA," *IEEE Trans. Reliability*, vol. 27, pp. 254-257, 1978.

[74] S. A. Herrin, "Maintainability Applications Using the Matrix FMEA Technique," *IEEE Trans. Reliability*, vol. 30, pp. 212-217, 1981.

[75] H. B. Dussault, "Automated FMEA Status and Future," in *Annual Reliability and Maintainability Symposium*, pp. 1-5, 1984.

[76] C. J. Price, D. R. Pugh, M. S. Wilson, and N. Snooke, "The Flame system: automating electrical failure mode and effects analysis (FMEA)," in *Annual Reliability and Maintainability Symposium*, pp. 90-95, 1995.

[77] P. L. Goddard, "Software FMEA techniques," in *Annual Reliability and Maintainability Symposium*, pp. 118-123, 2000.

[78] S. M. Yacoub, H. H. Ammar, and T. Robinson, "A methodology for architectural-level risk assessment using dynamic metrics," in *11th International Symposium on Software Reliability Engineering*, pp. 210-221, 2000.

[79] Y. Papadopoulos, D. Parker, and C. Grante, "Automating the failure modes and effects analysis of safety critical systems," in *IEEE 8th International Symposium on High Assurance Systems Engineering*, pp. 310-311, 2004.

[80] R. Bono, R. Alexander, A. Dorman, Y.-J. Kim, and J. Reisdorf, "Analyzing reliability - a simple yet rigorous approach," *IEEE Trans. Industry Applications*, vol. 40, pp. 950-957, 2004.

[81] P. Luthra, "FMECA: an integrated approach," in *Annual Reliability and Maintainability Symposium*, pp. 235-241, 1991.

[82] Z. Yang, S. Bonsall, and J. Wang, "Fuzzy Rule-Based Bayesian Reasoning Approach for Prioritization of Failures in FMEA," *IEEE Trans. Reliability*, vol. 57, pp. 517-528, 2008.

[83] H. Gargama and S. K. Chaturvedi, "Criticality Assessment Models for Failure Mode Effects and Criticality Analysis Using Fuzzy Logic," *IEEE Trans. Reliability*, vol. 60, pp. 102-110, 2011.

[84] Y.-S. Lee, D.-J. Kim, J.-O. Kim, and H. Kim, "New FMECA Methodology Using Structural Importance and Fuzzy Theory," *IEEE Trans. Power Systems*, vol. 26, pp. 2364-2370, 2011.

[85] D. S. Savakoor, J. B. Bowles, and R. D. Bonnell, "Combining sneak circuit analysis and failure modes and effects analysis," in *Annual Reliability and Maintainability Symposium*, pp. 199-205, 1993.

[86] C. J. Price and N. Hughes, "Effective automated sneak circuit analysis," in *Annual Reliability and Maintainability Symposium*, pp. 356-360, 2002.

[87] N. Hughes, "Functional modelling of electrical schematics," presented at the The IEE Seminar on Railway System Modelling - Not Just for Fun, 2004.

[88] D. Qiu and B. Zhang, "Analysis of Step-down Resonant Switched Capacitor Converter with Sneak Circuit State," presented at the IEEE Power Electronics Specialists Conference, 2006.

[89] D. Qiu and B. Zhang, "Discovery of Sneak Circuit Phenomena in Resonant Switched Capacitor DC-DC Converters," presented at the IEEE Conference on Industrial Electronics and Applications, 2006.

[90] J. Li, D. Qiu, and B. Zhang, "Sneak Circuit Analysis for n-stage Resonant Switched Capacitor Converters Based on Graph Theory," presented at the IEEE 33rd Annual Conference of the Industrial Electronics Society, 2007.

[91] W. Tu, D. Qiu, B. Zhang, and J. Li, "Sneak Circuit Analysis in n-Stage Resonant Switched Capacitor Converters," presented at the IEEE International Workshop on Anti-counterfeiting, Security, Identification, 2007.

[92] L. Qu, B. Zhang, D. Qiu, and W. Tu, "Sneak circuit analysis method based on generalized connection matrix for power converters," presented at the International Conference on Electrical Machines and Systems, 2008.

[93] Z. Liping and Z. Tao, "The application of neural network for Sneak Circuit Analysis on the aircraft electrical system," presented at the IEEE Prognostics and System Health Management Conference, 2011.

[94] A. J. Mair, E. M. Davidson, S. D. J. McArthur, S. K. Srivastava, K. Schoder, and D. A. Cartes, "Machine learning techniques for diagnosing and locating faults through the automated monitoring of power electronic components in shipboard power systems," presented at the IEEE Electric Ship Technologies Symposium, 2009.

[95] *ONR Control Challenge Problem*. Available: http://www.usna.edu/EPNES/Challenge_Problem.htm

[96] IEEE, "IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships," in *IEEE Std 1709-2010*, pp. 1-54, 2010.

[97] B. Farhangi and K. L. Butler-Purry, "Transient study of DC Zonal Electrical Distribution System in Next Generation Shipboard Integrated Power Systems using PSCAD™," presented at the North American Power Symposium, 2009.

[98] J. Langston, S. Suryanarayanan, M. Steurer, M. Andrus, S. Woodruff, and P. F. Ribeiro, "Experiences with the simulation of a notional all-electric ship integrated power system on a large-scale high-speed electromagnetic transient simulator," presented at the IEEE Power Engineering Society General Meeting, 2006.

[99] S. Technologies, "DD(X) Notional Baseline Modeling and Simulation Development Report," 2003.

[100] Q. Shen, B. Ramachandran, S. K. Srivastava, M. Andrus, and D. A. Cartes, "Power and Energy Management in Integrated Power System," presented at the IEEE Electric Ship Technologies Symposium, 2011.

[101] C. A. G. Marques, M. V. Ribeiro, C. A. Duque, P. F. Ribeiro, and E. A. B. da Silva, "A Controlled Filtering Method for Estimating Harmonics of Off-Nominal Frequencies," *IEEE Trans. Smart Grid*, vol. 3, pp. 38-49, 2012.

[102] M. Kezunovic. (2010) Intelligent Design. *IEEE Power and Energy Magazine*. 37-44.

[103] M. Kezunovic, "Smart Fault Location for Smart Grids," *IEEE Trans. Smart Grid*, vol. 2, pp. 11-22, 2011.

[104] T. Popovic and M. Kezunovic. (2012) Measures of Value: Data Analytics for Automated Fault Analysis. *IEEE Power and Energy Magazine*. 58-69.

[105] P. Kankanala, S. C. Srivastava, A. K. Srivastava, and N. N. Schulz, "Optimal Control of Voltage and Power in a Multi-Zonal MVDC Shipboard Power System," *IEEE Trans. Power Systems,* vol. 27, pp. 642-650, 2012.

[106] D. Kastha and B. K. Bose, "Investigation of fault modes of voltage-fed inverter system for induction motor drive," *IEEE Trans. Industry Applications,* vol. 30, pp. 1028-1038, 1994.

[107] R. Letor and G. Candeloro Aniceto, "Short circuit behavior of IGBTs correlated to the intrinsic device structure and on the application circuit," *IEEE Trans. Industry Applications,* vol. 31, pp. 234-239, 1995.

[108] R. S. Chokhawala, J. Catt, and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Trans. Industry Applications,* vol. 31, pp. 256-263, 1995.

[109] M. Otsuki, Y. Onozawa, H. Kanemaru, Y. Seki, and T. Matsumoto, "A study on the short-circuit capability of field-stop IGBTs," *IEEE Trans. Electron Devices,* vol. 50, pp. 1525-1531, 2003.

[110] S. M. A. Cruz, M. Ferreira, A. M. S. Mendes, and A. J. M. Cardoso, "Analysis and Diagnosis of Open-Circuit Faults in Matrix Converters," *IEEE Trans. Industrial Electronics,* vol. 58, pp. 1648-1661, 2011.

[111] F. Richardeau, P. Baudesson, and T. A. Meynard, "Failures-tolerance and remedial strategies of a PWM multicell inverter," *IEEE Trans. Power Electronics,* vol. 17, pp. 905-912, 2002.

[112] M. A. Rodriguez-Blanco, A. Claudio-Sanchez, D. Theilliol, L. G. Vela-Valdes, P. Sibaja-Teran, L. Hernandez-Gonzalez, *et al.*, "A Failure-Detection Strategy for IGBT Based on Gate-Voltage Behavior Applied to a Motor Drive System," *IEEE Trans. Industry Applications,* vol. 58, pp. 1625-1633, 2011.

[113] H. Sheng, F. Wang, and C. W. Tipton, "A Fault Detection and Protection Scheme for Three-Level DC–DC Converters Based on Monitoring Flying Capacitor Voltage," *IEEE Trans. Power Electronics,* vol. 27, pp. 685-697, 2012.

[114] A. S. Farag, C. Wang, T. C. Cheng, G. Zheng, Y. Du, L. Hu, *et al.*, "Failure analysis of composite dielectric of power capacitors in distribution systems," *IEEE Trans. Dielectrics and Electrical Insulation,* vol. 5, pp. 583-588, 1998.

[115] P. Michalczyk, C. Friel, C. Vincent, J. P. Marret, J. M. Mexmain, D. R. de Cervens, *et al.*, "Failure mode analysis on capacitor energy banks," presented at the IEEE 14th International Digest of Technical Papers, 2003.

[116] L. Liu, Y. Guan, M. Wu, and L. Wu, "Failure prediction of electrolytic capacitors in Switching-Mode Power Converters," presented at the IEEE Prognostics and System Health Management Conference, 2012.

[117] A. M. R. Amaral and A. J. M. Cardoso, "On-line fault detection of aluminium electrolytic capacitors, in step-down DC-DC converters, using input current and output voltage ripple," *IET Power Electronics*, vol. 5, pp. 315-322, 2012.

[118] M. T. Rahimo and N. Y. A. Shammas, "Freewheeling diode reverse-recovery failure modes in IGBT applications," *IEEE Trans. Industry Applications*, vol. 37, pp. 661-670, 2001.

[119] M. T. Rahimo, "A comprehensive study of failure mode in IGBT applications due to freewheeling diode snappy recovery," presented at the IEEE 33rd Industry Applications Society Annual Meeting, 1998.

[120] "Summary of the `Guide for the protection of shunt reactors' ANSI C37.109," *IEEE Trans. Power Delivery*, vol. 6, pp. 116-118, 1991.

[121] W. K. Denson, "Reliability Assessment of Critical Electronic Components," IIT Research Institute1992.

[122] V. P. Bresfelean, "Analysis and Predictions on Students' Behavior Using Decision Trees in Weka Environment," presented at the 29th International Conference on Information Technology Interfaces, 2007.

[123] K. A. Jalil, M. H. Kamarudin, and M. N. Masrek, "Comparison of Machine Learning algorithms performance in detecting network intrusion," presented at the International Conference on Networking and Information Technology, 2010.

[124] F. E. Walker, "Sneak circuit analysis automation," in *Annual Reliability and Maintainability Symposium*, pp. 502-506, 1989.

[125] C. Turpin, P. Baudesson, F. Richardieu, F. Forest, and T. Meynard, "Fault management of multicell converters," *IEEE Trans. Industrial Electronics*, vol. 49, pp. 988-997, 2002.

[126] *Attribute relation file format*. Available: http://www.cs.waikato.ac.nz/~ml/weka/arff.html

[127] P. Venet, F. Perisse, M. H. E. Husseini, and G. Rojat. (2002) Realization of a smart electrolytic capacitor circuit. *IEEE Industry Applications Magazine*.

[128] S. Karimi, A. Gaillard, P. Poure, and S. Saadate, "FPGA-Based Real-Time Power Converter Failure Diagnosis for Wind Energy Conversion Systems," *IEEE Trans. Industrial Electronics*, vol. 55, pp. 4299-4308, 2008.

[129] E. D. Liddy, "NLP-supported decision-making," in *The Twenty-Third Annual International Computer Software and Applications Conference*, pp. 390-391, 1999.

[130] Y. Huang, D. Zisook, Y. Chen, M. Selter, P. Minardi, and J. Mattison, "Lessons learned in improving the adoption of a real-time NLP decision support system," presented at the IEEE International Conference on Bioinformatics and Biomedicine Workshops, 2011.

[131] K. Ryan, "The role of natural language in requirements engineering," in *IEEE International Symposium on Requirements Engineering*, pp. 240-242, 1993.

[132] D. Falessi, G. Cantone, and G. Canfora, "Empirical Principles and an Industrial Case Study in Retrieving Equivalent Requirements via Natural Language Processing Techniques," *IEEE Trans. Software Engineering*, vol. 39, pp. 18-44, 2013.

[133] S. Deerweter, S. T. Dumais, and G. W. Furnas, "Indexing by Latent Semantic Analysis," *Journal of the American Society for Information Science*, vol. 41, pp. 391-407, 1990.

[134] J. R. Bellegarda, "Exploiting latent semantic information in statistical language modeling," in *IEEE Proceedings*, pp. 1279-1296, 2000.

[135] Y.-f. Zhang and C. He, "Research of Text Classification Model Based on Latent Semantic Analysis and Improved HS-SVM," presented at the 2nd International Workshop on Intelligent Systems and Applications, 2010.