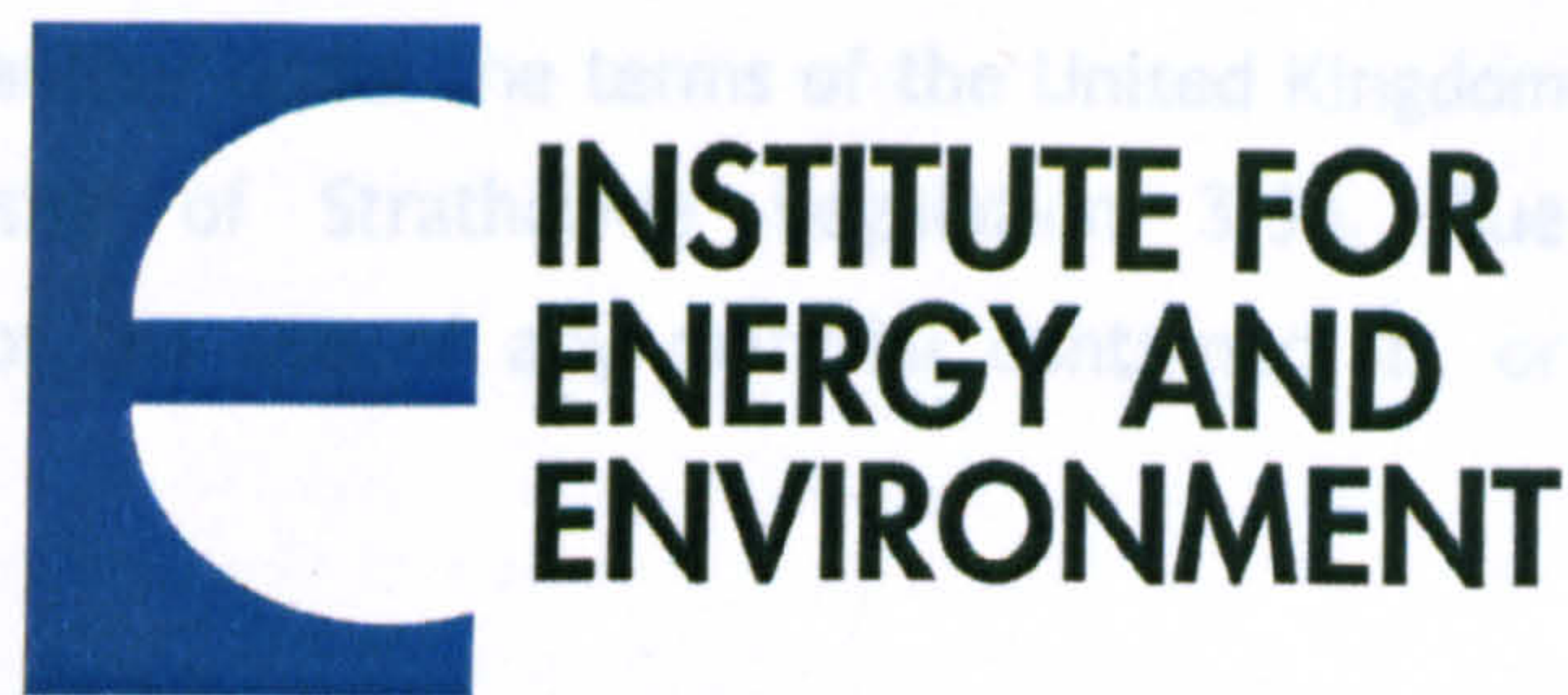


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Date: 27th March 2009

University of Strathclyde

Department of Electronic and Electrical Engineering

**Measurement, control and protection of
microgrids at low frame rates supporting
security of supply**

Volume 1

Andrew Roscoe

*A thesis presented in fulfillment of the requirements for the degree of Doctor of
Philosophy*

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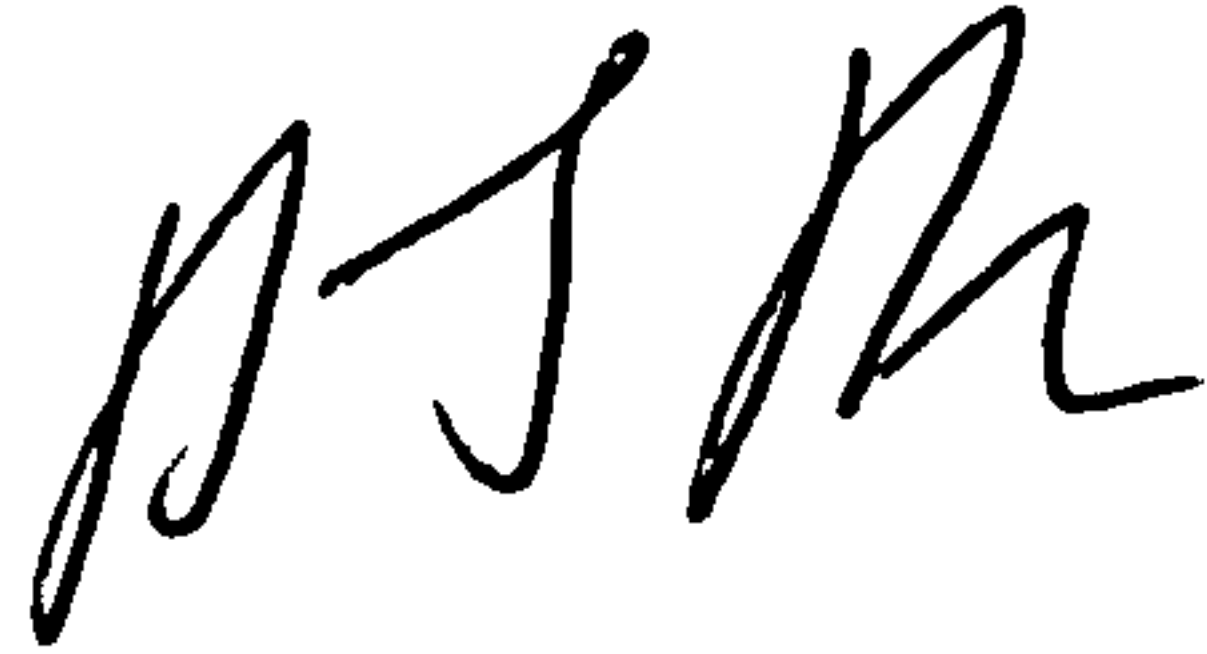
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Glossary of terms

AB or ABO	Vector produced from a three-phase voltage or current set after application of the Clarke Transformation
AC	Alternating Current
ADC	Analogue to Digital Converter
ADI	Applied Dynamics International
AVR	Automatic Voltage Regulator
CHP	Combined Heat and Power
Clarke-FLL hybrid	The frequency, amplitude and phase measurement system proposed by this thesis
CLTF	Closed Loop Transfer Function
CPU	Central Processing Unit (of a computer or microcontroller)
CT	Current Transformer
DAC	Digital to Analogue Converter
DFIG	Dual Fed Induction Generator
DC	Direct Current
DG	Distributed Generation
DNO	Distribution Network Operator
dq or $dq0$	Vector produced from a three-phase voltage or current set after application of the Park Transformation
ETS	(EU) Emissions Trading Scheme
FIR	Finite Impulse Response (filter)
FLL	Frequency Locked Loop
GPS	Global Positioning System (>30 Satellites provide position and accurate time information with 24-hour global coverage).
IGBT	Insulated Gate Bipolar Transistor
IIR	Infinite Impulse Response (filter)
LOM	Loss Of Mains
LPF	Low Pass Filter
NDZ	Non Detection Zone (normally, in the context of loss-of-mains detection)
OLTF	Open Loop Transfer Function
PF	Power Factor
PID	Proportional plus Integral plus Differential control loops.
PLL	Phase Locked Loop
POR	Phase Offset Relay
pu	per-unit
RMS	Root Mean Squared
ROC	Renewable Obligation Certificates
ROCOF	Rate Of Change Of Frequency
RTS	Real Time Station (Multi-processor simulation and control development system from ADI)
Sa/s	Samples per second (frame rate)
SNR	Signal to Noise Ratio
THD_v	Total Harmonic Distortion (of voltage)
UPS	Uninterruptible Power Supply
VT	Voltage Transformer

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Abstract

Increasing penetrations of distributed generation at low power levels within electricity networks leads to the requirement for cheap, integrated, protection and control systems. To minimise unit cost, algorithms for the measurement of AC voltage and current waveforms should be implemented on a single microcontroller, which also carries out all other protection and control tasks, including communication and data logging. This limits the frame rate of the major algorithms, although ADCs can be over-sampled using peripheral control processors on suitable microcontrollers. Measurement algorithms also have to be tolerant of poor power quality which may arise, even transiently, within a microgrid, battlefield, or disaster-relief scenario. This thesis analyses the potential magnitude of these interfering signals, and presents suitably tolerant architectures and algorithms for measurements of AC waveforms (amplitude, phase and frequency). These algorithms are shown to be robust and accurate, with harmonic content up to the level of 53% THD, and with the major algorithms executing at only 500 samples per second. This is achieved by the careful optimisation and cascaded use of exact-time averaging techniques, which prove to be useful at all stages of the measurements: from DC bias removal to low-sample-rate Fourier analysis to sub-harmonic ripple removal. Algorithms for three-phase nodal power flow analysis are benchmarked on the Infineon TC1796 microcontroller and require less than 8% of the 2000 μ s frame time, leaving the remainder free for other algorithms.

Furthermore, to optimise security of supply in a microgrid scenario, loss-of-mains must be detected quickly even when there is an accidental or deliberate balance between local active power generation and demand. The measurement techniques are extended to the detection of loss-of-mains using a new Phase Offset relay, in combination with a novel reactive power control technique to avoid the non-detection-zone. These techniques are tested using simulation, captured network transient events, and a real hardware microgrid including a synchronous generator and inverter.

1 Introduction

1.1 Distributed generation and microgrid background

The common model for western power networks within the last 50 years has been that of large systems dependent upon centralised power generation. Coal, nuclear, hydro, gas and oil-fired power stations of the multi-megawatt to multi-gigawatt scale have been built at convenient locations, and the electrical networks connected around them. The core of the UK electrical transmission grid is a 400kV and 275kV backbone which allows the electrical power to be moved with reasonable efficiency from generation to load. The coal, gas, nuclear and large hydro power stations which have provided the bulk of our electrical power are sensibly sited near to bulk fuel sources (coal mines, mountain lakes) and/or cold water supplies for cooling requirements (e.g. rivers, coastline). Some flexibility in siting relative to the fuel source locations is available for coal, gas, and nuclear power since the energy density of these fuels can justify transportation over large distances to reach the power station.

Over the coming years, it is predicted that these large centralised generators will become less dominant, and an increasing share of the generation mix will be provided by a large number of smaller scale generators, many of which will use renewable energy sources (DTI, 2007 and Ault, 2006). The reasons for this are:-

- The environmental taxes on fossil fuels and incentives for renewable energy sources. Examples of mechanisms currently active in the UK are the EU Emissions Trading Scheme (ETS) (DEFRA, 2008), and the UK Renewables Obligation which issues Renewables Obligation Certificates (ROCs).
- The poor efficiency of large power stations, due to large unrecovered heat losses.
- The gradual exhaustion of fossil fuel supplies, and the volatility of fossil-fuel prices in a global market. The UK, for example, is heavily reliant on imported natural gas from Norway and Russia. The natural gas wholesale cost increases of late 2005 provide a good example of market volatility and how vulnerable the UK is to sudden energy shortages due to the relative non-diversity of our current energy portfolio, coupled with limited UK gas storage capability. Much of our coal for power stations comes from Poland or even further afield. Even nuclear power, as proposed by the recent energy review (DTI, 2006 & 2007), does not present a long-term solution since the expected global sources of Uranium will be exhausted by approximately 2091 based upon the 2004 consumption rate (IAEA, 2007 & DTI, 2006). U_3O_8 prices more than doubled from \$10/lb in 2000 to \$21/lb in 2005, when the DTI energy review estimated the fuel cost to be 11% of the energy cost. Since

2005, the cost of U_3O_8 has risen to \$72/lb at 05/01/2007 (IAEA, 2007) and then to \$135/lb in July 2007. Clearly, nuclear fission represents only an expensive and short-term energy supply unless fuel reprocessing can be made much more efficient and/or the use of fast breeder reactors becomes politically acceptable.

To enable the reduction of dependence upon the diminishing fossil-fuel and nuclear-based resources, there are several solutions which can be implemented in parallel.

1. Increasing the proportion of renewable energy
2. Increasing the efficiency of thermal generation by using CHP (combined heat and power) schemes.
3. Reducing demand through taxation, real-time pricing schemes (Roscoe, 2004 & 2009c), behavioural attitudes, and the improved efficiency of equipment (EST, 2008).

General demand reduction measures are outside the scope of this thesis. Regarding the generation sources, one of the ways of achieving (1) is the installation of large windfarms at scales of up to and beyond 100MW (to date, up to 322MW on land (Scottish Power, 2006) and 520MW at sea (BBC, 2002)). Another way to achieve (1) and (2) is to install many thousands of small generators operating at the kW and MW scale, distributed within the electricity network, to replace relatively few GW-scale power stations that are retired. Such generation is commonly referred to as Distributed Generation (DG). The work of this thesis is primarily focussed at assisting the deployment of these smaller-scale generators.

The application of CHP schemes causes this distribution effect simply because generators must be sited near to the heat loads to minimise heat distribution costs. The extreme example of this is the application of domestic combined boiler/generator solutions. Another reason for the distribution of the new generators is due to the low energy density of fuels derived from renewable sources. For example, transporting of most biomass feedstock is not energy efficient over more than a few km (Cloonan, 2004), so the expectation will be for many small-scale power plants located by necessity where the resource exists. Solar, wave and wind-power installations must, by definition, be installed where the resource exists.

So, there are many drivers leading towards a network containing many thousands of small generators, some of which will be despatchable and some of which will be based upon stochastically varying resources. Most of the renewable sources will be largely

uncontrollable apart from generation curtailment, but hydroelectric and biomass/biogas plants or renewable schemes involving hydrogen storage can offer additional degrees of controllability depending upon the amount of locally stored feedstock.

The effects of this shift towards ubiquitous generation are many. One of the effects is that the risk of power outages may rise, due to winter demand peaks that cannot be met by installed renewable generation due to unfavourable weather conditions. Most of the renewable energy sources are not controllable, and it is (currently) not financially viable to store the electrical energy from wind, wave or solar installations due to the conversion losses and capital cost of adequate storage systems (Foote, 2005).

Any rise (or perceived rise) in the risk of power outages will lead to even more installations of distributed generation, by customers for whom outages, even for a few seconds, might be very expensive. During a power outage, the distributed generation can be used as an emergency generator to supply local loads in a power island.

Power networks that can be studied and controlled/protected in a localised manner can be termed microgrids. A microgrid may contain generation sources of many types, loads, electrical storage, and connection points to other microgrids or parent networks. At any time a microgrid might be islanded, connected to another microgrid, or connected to a much larger power system such as the UK national grid. Good examples of microgrid applications are:-

- Distributed generators and associated local loads within the UK distribution network
- Marine and Aeronautical power systems
- Disaster-relief power networks
- Battlefield power systems

Any electrical power system requires protection, and any generation source additionally requires control. Optimum management of a microgrid power system requires both protection and control. To research the overall goal of microgrid management, a laboratory demonstrator has been created at the University of Strathclyde. A schematic of this is shown in Figure 1-1. A significant microgrid control application has been created, which is outside the scope of this thesis (Roscoe, 2005, 2007 & 2008). While creating this application, difficulty was faced due to specific constraints and lack of established knowledge in two key areas. Without solutions to these two challenges, the effectiveness

of the microgrid control application to ensure security of supply to the local customers is significantly impaired. These two major areas are:-

- 1) Measurement of amplitude/phase/frequency with low frame rates within power systems experiencing poor power quality.
- 2) Reliable, timely detection of Loss-Of-Mains (LOM) especially when local active power generation is accidentally or deliberately balanced to local active power demand, while avoiding spurious (nuisance) tripping.

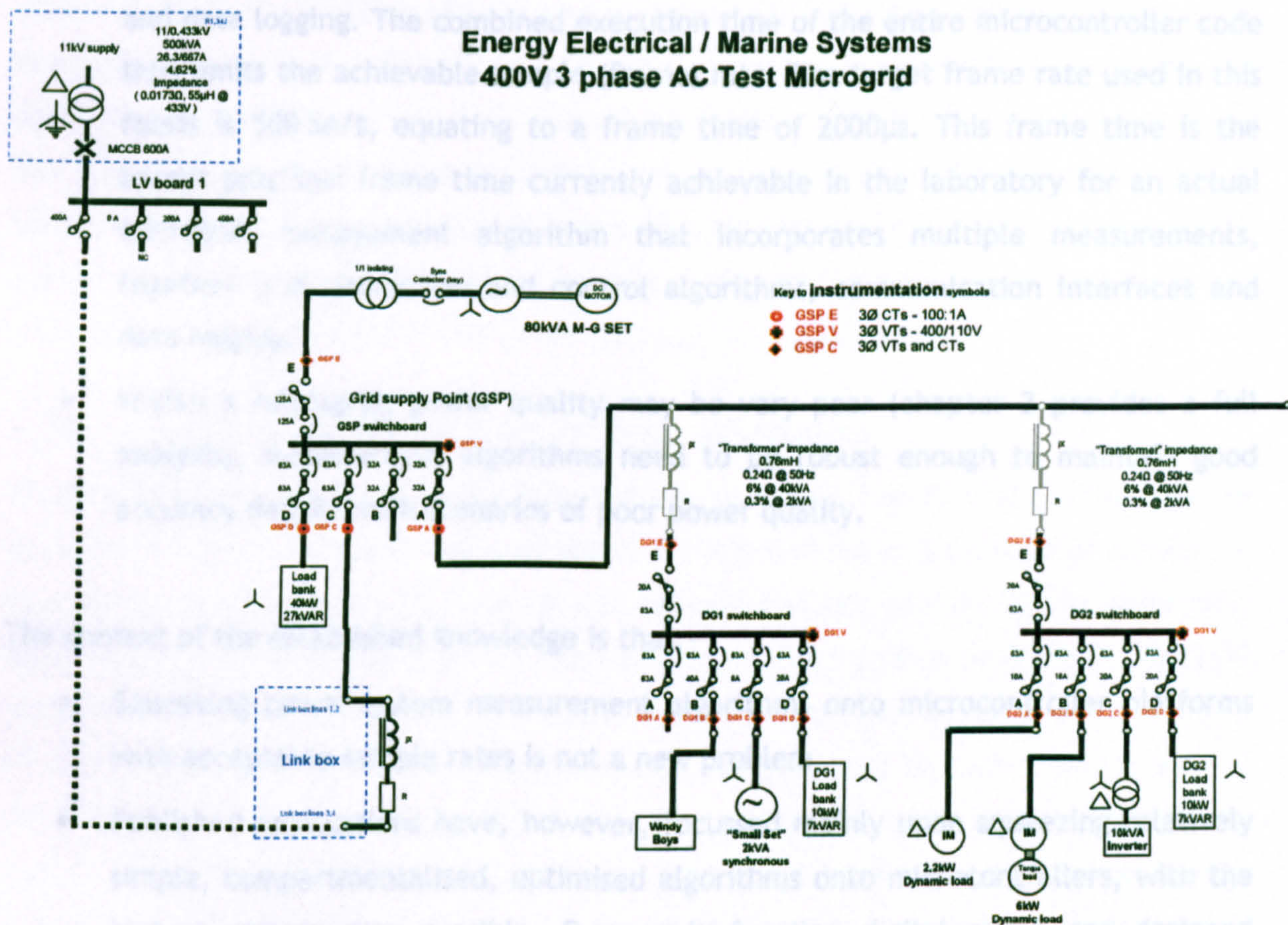


Figure 1-1 : 400V 3-phase microgrid laboratory; single-line diagram

1.2 Measurements at low frame rates

Within the context of large thermal power stations, protection and control can be implemented using large, expensive pieces of equipment, since the cost and size of the equipment is small compared to the rating and size of the power station. Within the scope of microgrid management, however, this is not true. Measurement, protection and control functions must be integrated within small, cheap pieces of hardware to become cost effective. The ideal solution is therefore for a single microcontroller to be able to manage all these tasks. The control tasks themselves (excluding those for inverter design) can easily accommodate low frame rates such as 100 Sa/s (samples per second) with a 10ms reaction time. For the measurement algorithms, however, the use of low frame rates is a

major concern since the AC waveform frequency is typically 50 Hz and this must be captured adequately by the algorithms. This thesis addresses the requirement of measuring AC signals using low frame rates down to 500 Sa/s.

The constraints on the measurements are:-

- Many measurement, protection and control algorithms need to be executed on a single microcontroller platform. The microcontroller code includes not only the required algorithms but also overheads including ADC sampling, communications and data logging. The combined execution time of the entire microcontroller code thus limits the achievable sample (frame) rate. The target frame rate used in this thesis is 500 Sa/s, equating to a frame time of 2000 μ s. This frame time is the lowest practical frame time currently achievable in the laboratory for an actual microgrid management algorithm that incorporates multiple measurements, together with protection and control algorithms, communication interfaces and data logging.
- Within a microgrid, power quality may be very poor (chapter 2 provides a full analysis). Measurement algorithms need to be robust enough to maintain good accuracy despite such scenarios of poor power quality.

The context of the established knowledge is that:-

- Squeezing power-system measurement algorithms onto microcontroller platforms with acceptable sample rates is not a new problem.
- Published applications have, however, focussed mainly upon squeezing relatively simple, compartmentalised, optimised algorithms onto microcontrollers, with the highest sample rate possible. Even multi-function digital relays are designed primarily to measure voltages and currents at just a single node.
- The speed and available memory within cheap microcontrollers is ever increasing. This offers new opportunities compared to methods previously proposed.
- Published academic research to date does not provide measurement algorithms which are tolerant enough to poor power quality, whilst also providing the low-latency response times required. The performance and tolerance of published algorithms is often difficult to assess due to poor graphical presentations (inappropriate scaling) within the referenced material.

The new approach adopted by this thesis is to create algorithms which can operate at very slow (and fixed) sample rates (down to 500 Sa/s, 10 samples per cycle at 50 Hz), with low

execution times, low latencies, and high accuracy.

A suitable target for execution speed is $<200\mu\text{s}$ for a three-phase, nodal voltage/current/balance and power flow analysis. Making such an algorithm execute at only 500 Sa/s appears at first glance to be an unnecessary step, since such an algorithm could be clocked at $1/200\mu\text{s} = 5000$ Sa/s which would make accuracy targets easier to achieve. However, the key point is that once such an algorithm is created, many such algorithms can be combined on a single processor, and the target frame rate still achieved. Thus, the creation of such new measurement algorithms (Roscoe, 2009), and a thorough assessment of their performance during dynamic and steady-state conditions, is a significant enabler for any microgrid control application. Additional useful by-products of this work are that the resulting algorithms can be used within multi-rate simulations to minimise simulation time, and that in future (due to microcontroller speed increases) the algorithms can be executed at higher sample rates and the accuracy will only improve from the analyses presented in this thesis.

1.3 Reliable detection of loss-of-mains

Within a microgrid scenario, to maximise security of supply, loss-of-mains (LOM) must be detected quickly and reliably. A loss-of-mains event is defined as a severing of connection to a parent network, when the local power network contains generation (and optionally load). Undetected, this condition can present risks of electrocution or damage. The LOM event must therefore be detected in a timely manner and suitable action taken. In the UK, ER G59/1 (ENA, 1991) currently forbids a distributed generator to back-feed any part of the distribution network during a LOM condition, and the LOM event must conventionally lead to a fast disconnection of the generator. However, within a customer's own private installation the detection of LOM may be used to trigger a managed transition into an islanded state, so long as no power is fed back into the public network. The ability to switch quickly to islanded mode allows a significant increase in the security-of-supply at the local level, by reducing the frequency and voltage excursions from nominal and hence the risk of local outages, even though such outages may be very short. To accomplish this effectively requires a fast and reliable method for LOM detection. Many published works present active methods for detecting this LOM condition, which rely on fast switching outputs from inverter-connected generation. For general application using rotating generators, a more passive method must be used. While methods such as monitoring dV/dt & power-factor have been proposed (Salman, 2000), methods using ROCOF (Rate of Change of Frequency) relays are the most well established and widely used. However, they suffer from two main drawbacks:-

- Inability to quickly detect the LOM condition when there is an exact or close

match between the local active and reactive power generation and demand. This is because when active and reactive power is balanced in this way, an unexpected LOM event causes only a very small (within the bounds of normal operation) change in frequency, which is not sufficient to trip LOM relays. Such a balanced of active power can be highly desirable within a microgrid, and may deliberately be targeted. This is because, when operated in this state, any subsequent deliberate transition to the islanded state results in only small frequency deviations, hence providing the highest chance that the local power island will survive the transition to islanded mode.

- Spurious tripping due to the relatively noisy measurement of ROCOF, which is a time-derivative of the measured frequency.

This thesis addresses both these issues, via two separate approaches in parallel. The first approach is the combined use of the novel accurate low sample-rate measurements with a new method to detect the LOM condition based upon estimations of the phase of the local power system relative to the parent network. This is substantially less noisy and more discriminatory than a ROCOF measurement. It can also be adapted to automatically de-sensitise itself during faults and thus avoid spurious trips. The second approach is a combination of a new design of control loop for DG power control in grid-connected mode, combined with a novel reactive power control strategy which allows successful detection of the LOM condition even when active power is exactly balanced (Roscoe, 2008b & 2009b). This works by causing a small shift in the active power balance subsequent to a LOM event and thus triggering an unstable control mode in the standard generator droop controllers. This strategy is applicable to all generators which allow control of reactive power (or power factor) without the need for power electronic devices or high frequency current injections.

1.4 Structure of this thesis

Chapter 2 describes the requirements for the measurement algorithms. These requirements encompass the required accuracy, response time (latency), tolerance to poor power quality, and constraints due to microcontroller hardware. Significant analysis is carried out to determine worst-case levels of “influence qualities” due to worst-case microgrid power quality. This accounts for such parameters as rate-of-change-of-frequency (ROCOF), harmonic content, inter-harmonics, unbalance, flicker, and instrumentation noise. The worst cases account for applicable power system standards in place today in the UK and the USA, in combination with practical assessments of whether these levels might be breached within non-standard power-system scenarios. The worst case power quality is found to be much poorer than normally experienced in the UK, although the

expectation would be that such poor power quality would only be experienced for short time periods.

Chapter 3 presents the selection and design of architectures and designs for algorithms to measure amplitude and phase, assuming that the signal frequency is known. Initially, some small building blocks are developed and characterised in isolation. The single most useful building block, which is used repeatedly throughout this thesis, is an exact-time averaging block. This block is developed from a MATLAB Simulink block, but significantly enhanced in this thesis both for mathematical accuracy and for execution speed. The use of the improved algorithm allows the creation of a useful new DC blocking algorithm with zero group delay, which offers better performance than a high-pass filter. More importantly, several architectures for the overall measurement of amplitude and phase are designed and compared. Some of these are based upon existing literature, but the best architecture for use in distribution networks is found to be a new architecture developed during chapter 3. This involves the use of $1\frac{1}{2}$ cycle measurements (1-cycle exact-time integration/averaging cascaded with an extra $\frac{1}{2}$ -cycle exact-time averaging) and offers excellent performance even at the lowest sample rates. A selection process is presented which recommends the best architecture to be employed based upon the target scenario.

Chapter 4 begins with the design and verification of a mathematical tool which can be used to predict the likely measurement error ripples due to aliased harmonics at a range of sample rates. This shows that the potential measurement ripple at the sample rates of interest, due to certain problematic harmonics, can be large relative to the desired specification. To mitigate this problem, two solutions are applied. Firstly, a very effective, novel, adaptive ripple-removal filter is designed and tested. Secondly, a front-end 6x oversampling (3000 Sa/s) FIR notch filter is designed using standard zero-pole placement techniques; this can be used to further reduce the measurement ripple when the input signal has high levels of distortion, requiring only very small amounts of processing at the 6x oversampled frame rate.

Chapter 5 builds directly upon the outputs of chapters 3 and 4, to create a large novel algorithm (called a “Clarke-FLL hybrid”) for the measurement of frequency (and amplitude and phase) within a 3-phase AC power system. Again, the cascaded use of the enhanced exact-time averaging techniques is found to be an extremely applicable technique. The Clarke-FLL hybrid is compared to seven other candidate algorithms for frequency measurement, and found to surpass them in terms of measurement accuracy and latency.

Chapter 6 presents the algorithmic design for a robust Phase Offset Relay (POR), which was initially proposed as an improved method for loss-of-mains detection in Dysko (2006), compared to traditional ROCOF and vector-shift relays. This thesis presents the first implementation of this relay in a robustly-coded form suitable for deployment on a microcontroller. The presented relay algorithm includes a new triggering subsystem which allows both trigger and trip thresholds to be set appropriately based upon known network behaviour. Also, the relay includes new software to detect balanced & unbalanced faults. When these are detected, the relay can de-sensitise itself via a temporary widening of trip setting to allow for post-fault power-system oscillations. This allows the relay to avoid spurious trips during distant and close-in network faults, providing much improved discrimination over existing LOM relays, without resorting to a complete disabling of the trip signal during such faults. This relay re-uses the novel signal processing techniques and measurement outputs developed during chapters 3-5. Substantial analysis, using both simulated and captured power system events, shows that this relay exhibits good sensitivity and discrimination.

Furthermore, analysis of power system stability is carried out in chapter 6, and combined with a new strategy for management of reactive power flow within a microgrid (Roscoe, 2008b & 2009b). This can be used to avoid the small non-detection-zone of the loss-of-mains detection algorithm, even when there is an accurate balance between locally produced active power and the local active power demand. The combination of the new control algorithm and the new loss-of-mains detection algorithm are rigorously tested using microcontroller hardware and the microgrid of Figure 1-1 (including both a synchronous generator and three-phase inverter).

Throughout this thesis, intermediate findings are highlighted where relevant. The main conclusions are summarised in chapter 7. Appendix A to Appendix H contain relevant supplementary information and additional coding details.

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2 System study of amplitude, phase and frequency measurement requirements within 3-phase AC microgrids

The measurement of amplitude, phase and frequency within microgrid power systems presents new problems. Traditional methods for measuring these parameters have been developed within the context of large, relatively stable power systems at high voltages where the waveforms are closely regulated and contain low levels of harmonic contamination. The new requirements for measurement algorithms within smaller power systems are analysed in the following sub-sections. The purpose of this chapter is to generate a set of requirements which such measurement algorithms will need to meet to be useful, accurate and robust within a microgrid scenario. The requirements encompass both the properties and qualities of the signals to be measured, and also the potential constraints on the measurement hardware. This may need to be substantially cheaper than existing equipment, and also to be integrated with many other software algorithms on an integrated micro-controller platform. The requirements also define suitable signals to be used as test inputs for any candidate algorithms.

2.1 Increased rates of change of frequency within microgrids

A major technical barrier to operating a small AC microgrid is the issue of inertia and system frequency stability. Within any AC power system, the frequency stability is a function of the inertia of the generators and loads, coupled with the magnitude of any load changes or generator prime mover power output changes. Restricting discussions to rotating generators for the time being, the maximum rate of change of frequency (ROCOF), in Hz/s, can be estimated for a hypothetical power system.

The per-unit inertia of a prime-mover & generator unit is given by H , in seconds, which is equal to the energy stored in the spinning unit at nominal speed divided by the nominal power rating (in VA) of the machine. Thus, if $H=0.5$ for a 1MVA generator, then the machine has 500kJ of stored energy when spinning at nominal speed.

H can be related to the inertia J in SI units (kgm^2) using the standard formula for stored energy in a flywheel:-

$$E = \frac{1}{2} J \omega^2$$

(2.1)

and then evaluating this at the nominal rotational speed to obtain

$$E_0 = \frac{1}{2} J \omega_0^2 \quad (2.2)$$

Where E_0 = stored energy at nominal speed (Joules)

ω_0 = nominal rotational speed in radians/s

J = moment of inertia of prime mover plus generator, in kgm^2

Then:-

$$H = \frac{\frac{1}{2} J \omega_0^2}{S_0} \quad (2.3)$$

or:-

$$J = \frac{2H \cdot S_0}{\omega_0^2} \quad (2.4)$$

Where H = the per-unit inertia of the generator

S_0 = the nominal rating (in VA) of the generator

Per-unit inertias of generators vary, depending upon the design and size of the generator and prime mover. For example, H might be as low as $<1\text{s}$ for small reciprocating engines coupled to synchronous generators, or as high as 10s for a large thermal GW-scale unit (Mullane, 2005).

Using these different values of H , and different sizes of power system, it is possible to perform an approximate analysis of frequency stability. The scenario to be analysed begins with a network which at some instant in time is in an equilibrium state with the sum total of all generator prime mover outputs matching the sum total of load powers. At this time the network frequency is assumed nominal, i.e. $f=f_0=2\pi\omega_0$. Then a new load is added or generator removed, which creates a generation/load imbalance. Within the immediate time following the load addition, the prime mover outputs do not change significantly, due to the response time of the governors, droop controls and throttle delays. By differentiating the standard equation for stored energy (2.1) we have:-

$$\frac{dE}{dt} = \frac{d}{d\omega} \left(\frac{1}{2} J \omega^2 \right) \frac{d\omega}{dt} \quad (2.5)$$

$$\Rightarrow \frac{dE}{dt} = J \omega \frac{d\omega}{dt}$$

which approximates to

$$\frac{dE}{dt} = J \omega_0 \frac{d\omega}{dt} \text{ when the generator is close to nominal speed.} \quad (2.6)$$

Note that (2.6) can be expanded into the familiar swing equation by substituting H for J and turning the energy flow from the machine dE/dt into a per-unit quantity, i.e.

$$\frac{dE}{dt} = \left(\frac{2H \cdot S_0}{\omega_0^2} \right) \omega_0 \frac{d\omega}{dt} \quad (2.7)$$

$$\frac{\frac{dE}{dt}}{S_0} = \frac{2H}{\omega_0} \frac{d\omega}{dt} \quad (2.8)$$

and finally to the familiar swing equation:-

$$\frac{2H}{\omega_0} \frac{d^2 \delta}{dt^2} = P_m - P_e \quad (2.9)$$

where P_m and P_e , and the imbalance between them (which equals $(dE/dt)/S_0$), are measured in per-unit quantities, and δ is the generator rotor angle, where of course $d\delta/dt$ is the rotational speed ω .

Returning to (2.6), this equation may be rearranged to give the rate of change of frequency by:-

$$\frac{d\omega}{dt} = \frac{1}{J \omega_0} \frac{dE}{dt} \quad (2.10)$$

and thence

$$\frac{df}{dt} = \frac{1}{4\pi^2 J f_0} \frac{dE}{dt}$$

(2.11)

where $f=2\pi\omega$ and $f_0=2\pi\omega_0$, which reveals the rate of change of frequency (ROCOF) as a result of a power imbalance in an electrical power system with inertia.

This equation may also be expressed in terms of H by substituting (2.4):-

$$\frac{df}{dt} = \frac{f_0}{2 \cdot S_0 \cdot H} \frac{dE}{dt}$$

and thence into per-unit quantities

$$\frac{df_{p.u.}}{dt} = \frac{\Delta P_{p.u.}}{2 \cdot H}$$

(2.12)

where $\Delta P_{p.u.}$ is the load-generation power imbalance in per-unit.

To compare expected ROCOF magnitudes in the current UK national grid, and a potential microgrid, estimations can be made of representative values of J and dE/dt . Within the national grid, the generators are generally large synchronous machines with inertias of the order of $H=5s$ (Mullane, 2005). The overall network generation rating is approximately 60GVA. This leads to $J \approx 6.1 \times 10^6 \text{ kgm}^2$ by (2.4). One of the largest potential generation/load imbalance scenarios would be an entire power station of size $\approx 2\text{GW}$ tripping off line. Immediately after the trip, the “missing” 2GW must be supplied to the loads from the inertia of the remaining on-line power stations. Thus, the sum total of energy in their rotors changes with $dE/dt = -2 \times 10^9 \text{ (-2GW)}$ and equation (2.11) reveals df/dt (ROCOF) to be about -0.17 Hz/s . Applying equation (2.11) to different scenarios shows how the expected ROCOF (due to generation-load imbalance) varies dramatically.

Clearly, frequency stability becomes much more of a problem as the size of a power system gets smaller, as reflected in the changes to the expected values of ROCOF. More specifically, the dynamic effects of frequency get much harder to manage as the maximum expected load or generation changes get larger as a proportion of the rotational inertia built into the system.

Scenario	Average per-unit inertia, H (s)	Power system rating	Total system inertia J (kgm ²)	Generation-load imbalance dE/dt	Expected ROCOF (Hz/s)
UK national grid, large load decrease of 100MW	5	60 GVA	6.1x10 ⁶	100 MW	0.01
UK national grid, sudden loss of large power station	5	60 GVA	6.1x10 ⁶	-2 GW	-0.17
1MVA microgrid, removal of 1 10kW load	2.5	1 MVA	51	10 kW	0.1
1MVA microgrid, sudden loss of a 100kVA generator	2.5	1 MVA	51	-100 kW	-1.0
2-generator 100kVA microgrid, removal of 1 kettle (3kW load)	2	100 kVA	4.1	3 kW	0.4
2-generator 100kVA microgrid, sudden loss of one generator	2	100 kVA	4.1	-50 kW	-6

Table 2-1 : Expected ROCOF rates for different power system events

In the case of the UK national grid, even with the loss of a 2GW power station, at -0.17 Hz/s this allows 3 seconds before the normal 1% frequency limit (49.5-50.5 Hz) boundary is crossed (assuming frequency was nominal before the event). For the largest generators in the system, prime mover governors and power outputs will not fully react within this 3 second timeframe (Kundur, 1994), but over 10 seconds most hydro and thermal plants will react according to droop controls, (Kundur, 1994 & Wood, 1996) allowing the frequency excursion to be contained within the 1-1.5Hz bracket, avoiding mass trips in the transmission system and at generation sites. For normal load changes, ROCOF is of the order of 0.01Hz/s. Generator droop controls with relatively slow bandwidths are easily adequate to adjust to such slow changes, while the half-hourly bidding system is a short enough timeframe to efficiently despatch the generators on a unit-by-unit basis.

Contrast this with the situation within a 100 kVA microgrid, where even the addition of a single 13A load causes a ROCOF of about 0.4 Hz/s. In this scenario, the generation systems must fully react within 5 seconds or frequency will drop below 48 Hz. Loss of 50kW of generation within the microgrid at full load would lead to a ROCOF in the region of -6 Hz/s. To avoid frequency dipping below 48Hz this will require immediate despatch of a replacement 50kW of spinning reserve, or immediate shedding of up to 50kW load within 0.3 seconds, or a combination of the two.

2.1.1 Summary of frequency measurement requirements (ROCOF and reaction time)

To allow effective control of microgrid equipment, a frequency measurement algorithm should be able to follow at least 10 Hz/s ramp rates without becoming confused or unlocked. This figure is derived by adding a guard band of 4 Hz/s to the peak value of Table 2-1, which shows that a 6 Hz/s figure could easily be reached within a 100kVA microgrid. Also, the required overall reaction time at 6 Hz/s to remain within the ideal 2Hz window is about 0.3 seconds, of which most will be required for switching or power output changes of prime movers or storage devices. To allow most of the 0.3s for power system output adjustments, the measurement time should be <0.1 second. This implies a measurement in the timeframe of 3-5 cycles.

2.2 Frequency measurement range requirement

BS EN 50160 (BSI, 2000) states that system frequency should always be between 47 and 52 Hz. However, it allows 42.5 to 57.5 Hz in power islands. A frequency measurement should be able to follow a wider range of scenarios. This is because the measurement may be applied at the terminals of an open-circuit machine which may be rotating slowly, or may be over-speeding. Ideally the measurement system would be able to measure from DC to 100 Hz. It must be borne in mind that many measurements will be made via VTs (Voltage Transformers) which have zero gain at DC, so the measurements below 10 Hz may not be possible in practice, although a software algorithm should ideally allow for it. Smaller ranges such as 40-70 Hz might be acceptable so long as the measurement always rails to the correct limit if frequency is outside the measurable range. Fully accurate performance must be achieved over the 40-70Hz range to allow for 50Hz and 60Hz systems. Much lower accuracy is acceptable outside this range since equipment will normally be quickly tripped by under/over-frequency if frequency strays so far from nominal. Also, the accuracy of frequency-dependent controls/algorithms such as synchronising checks and droop controls become irrelevant outside the 40-70Hz range.

2.3 Frequency measurement accuracy requirement

Frequency needs to be measured accurately enough so that all relaying and control functions can be carried out without ambiguity, spurious tripping, oscillation or cyclic control actions. The actual accuracy is made up of 2 factors:-

- absolute accuracy of the clock used within the measuring device. This will affect the absolute error of the measurement, via a DC error bias.
- additional error due to noise, THD, and sampling/algorithm behaviour. This will show up as noise/ripple on the measurement.

Accuracy of cheap crystal oscillators for CPU clocking, taking into account temperature effects, are generally in the range of $\pm 50\text{ppm}$ ($\pm 0.005\%$, equates to a $\pm 0.0025\text{Hz}$ error @50Hz). This magnitude of error is of no consequence for frequency measurement, and can effectively be neglected. Achieving a greater accuracy than this is possible by using oven-stabilised crystals, Rubidium timebases etc., but the expense is not justified in this case, since the additional measurement ripple/noise will dominate the accuracy of the measurement.

BS EN 61000-4-30 (BSI, 2003), which is really a requirement for power quality measuring devices, states that for “class A” performance, the accuracy needs to be $\pm 0.01\text{ Hz}$ (0.02 %). In BS EN 61000-4-30, the expectation is that this measurement is made by counting zero crossings or using a Fourier technique over a ≈ 10 -second sampling window (the window is allowed to be just less than or just greater than 10 seconds, to count an integer number of cycles). Note that a miscount of 1 cycle over 10 seconds would equate to an error of $1/(10 \cdot 50) = 0.2\%$ which is 10x the required accuracy specification. The frequency measurement for control and relaying purposes needs to react within 3-5 cycles (0.1 second), not over 10 seconds. Therefore, meeting a similar $\pm 0.01\text{Hz}$ accuracy specification using only $1/100^{\text{th}}$ of the time window lays down a significant challenge for a measurement system.

Harder upper limits to the measurement accuracy requirement can be estimated by analysing the measurement stability needed to avoid problems with control, protective relaying and load-shedding algorithms.

For control applications, one estimate of the required frequency accuracy is to imagine a grid-connected generator with 5% frequency droop. Thus, a 5% change in frequency causes a 1pu (1 per-unit) change in output power. Thus, to limit power flow fluctuations as a result of noisy/rippling frequency measurements to less than $\pm 0.01\text{pu}$, the frequency error/ripple would need to be less than $\pm 0.05\%$, i.e. $\pm 0.0005\text{ pu}$ ($\pm 0.025\text{ Hz}$ for a 50Hz system). This target of $\pm 0.01\text{pu}$ power output fluctuation is set at such a low level in order to both minimise wear on the prime mover (in conjunction with deadbands in the control system), and to reduce the potential for power system oscillations.

Other upper limits are that the frequency error must be $\ll 0.1\text{Hz}$, to avoid hysteresis/oscillatory problems with load shedding schemes where thresholds are often set in bands approximately 0.2 Hz apart (Moore, 1996b). Obviously, the frequency error should also be much, much, less than the smallest of the under/over-frequency trip limits set by

ER G59/1 (ENA, 1991) (see Table 2-9), which is 1% (0.5 Hz).

Also, if the frequency measurement is to be used to deduce a value of ROCOF for a loss-of-mains (LOM) relay, then the ROCOF might be determined by taking the difference in the output of the frequency algorithm over a 5-cycle timeframe (the proposed latency of the measurement), and dividing by 0.1 (the time which that 5 cycles takes). Thus, if the frequency measurement algorithm has an output ripple/noise of $\pm y$ Hz at any sample, then the ripple on the ROCOF measurement, at 50Hz, will be up to $\pm 2y/0.1$, i.e. $\pm 20y$. Thus, to achieve a ROCOF result with noise/ripple less than ± 0.1 Hz/s, the frequency measurement ripple/noise must be less than ± 0.005 Hz, or $\pm 0.01\%$. This may be an unreachable target in systems with significant harmonic content or instrumentation noise. This is one reason why ROCOF relays have such a poor reputation for spurious tripping, and it is why a different approach to the sensitive subject of LOM relays is proposed later in chapter 6.

Since ROCOF relays include a qualifying time for which the tripping threshold must be exceeded before a trip is registered, it is tempting to carry out a statistical analysis which would allow an increased level of noise on the frequency measurement. This would be done on the basis that the qualifying time requires a number of consecutive samples above a certain threshold, which would reduce the probability of a trip. The problem with this analysis, in the context of microgrids, is that the harmonic content of the waveforms may be high, and the instrumentation sample rate may be low. It will be shown later that in these environments, these effects and constraints can lead to low frequency ripples. These cannot be subjected to a statistical noise-like analysis, and thus the maximum tolerable ripple threshold of ± 0.005 Hz stands for low-frequency error ripples, if the measurement is to be used as the basis for a ROCOF calculation.

In summary, the loosest requirement for frequency measurement accuracy is for a noise/ripple error of $\pm 0.05\%$ (± 0.025 Hz for a 50Hz system), although a small additional DC error term equivalent to the crystal clock accuracy of about $\pm 0.005\%$, (± 0.0025 Hz for a 50Hz system) can be tolerated, since it will not introduce any rippling control signals. If a ROCOF calculation is to be made from the frequency measurement, however, then the required error magnitude drops to ± 0.005 Hz, or $\pm 0.01\%$.

2.4 Voltage amplitude measurement speed and accuracy requirements

For measurements of voltage amplitude, the required measurement speed and accuracy depends upon the application. This thesis will propose several different “taps” from a

single initial base measurement, with longer latency measurements having reduced ripple/noise errors. The output from the “taps” can be picked as required for different relaying and control actions.

Similarly to frequency measurements, all voltage magnitude error measurements will be subject to two forms of error:-

- Calibration error; which will be a fixed gain error, plus linearity errors of the VTs and imperfect front-end low-pass filter characteristics for off-nominal frequency inputs. These mechanisms include any interpolation errors between calibration table entries if the calibration tables include points for several off-nominal frequencies or amplitudes to account for filter or VT characteristics. The calibration errors will tend to show up as DC bias offsets on the measurements.
- Additional error due to noise, THD, and sampling/algorithm behaviour. This will generally manifest itself as noise/ripple on the measurement.

An initial hardware calibration might be possible to the 0.1% level using good equipment, and a full on-site closed-loop test conducted carefully. After all error mechanisms such as temperature, linearity etc are accounted for, the total errors due to calibration-related mechanisms could easily account for a 0.5% to 1% error. This error magnitude will appear as a reasonably stable DC bias on the measurement of fundamental by a Fourier technique. Common, economical VTs or voltage measurement transducers are available with $\approx 1\%$ off-the-shelf accuracy. For practical and economic reasons, on-site closed-loop calibration of a microgrid measurement/control system from VTs to digital sampled data will not be possible. The system will more likely be expected to be simply installed and then operated. Therefore, the overall system calibration errors will be the quoted VT accuracy plus the additional sampling hardware, which can be factory-calibrated. Calibration error for an economical measurement system will thus probably be in the region of 2%.

The fastest voltage-measurement outputs would be required for algorithms within the control systems of power-electronic devices, which are outside the scope of this thesis. Such measurements can be made in $\ll 1$ cycle timeframes if the voltage waveforms are assumed to be clean sinusoids, or within a 3-phase system that is balanced.

For under/over-voltage relaying applications, within the microgrid context, the total measurement speed should be less than 3 cycles (60ms), of which some time will be accounted for in the group delay of any anti-aliasing filters. The digital processing latency should thus be less than 2 cycles (40ms). The justification for this statement is presented

in section 2.7.5. Measurement accuracy in this case should be $\ll 0.1\text{pu}$, since this is the order of magnitude of the steps between tripping thresholds in tables Table 2-8 and Table 2-9. A sensible error would be $\pm 0.02\text{pu}$, at 1/5 of the smallest (10%) tripping threshold.

For control purposes, a longer timeframe can be allowed, but a reduced noise/ripple level is desirable. A timescale of 5 cycles (100ms) for a measurement is acceptable, considering that AVR control loops and field generators for synchronous generators will not generally react faster than this. To assess an acceptable voltage error level, a grid-connected generator with a 10% reactive droop slope setting is considered. If voltage changes by 10%, the reactive power output control of the generator will change by 1pu. Thus, to keep the reactive power output ripple within $\pm 0.01\text{pu}$, the voltage measurement ripple/noise must be within $\pm 0.1\%$, or $\pm 0.001\text{pu}$. This is a tough target for such a measurement in the context of microgrids and particularly where low sample rates are used. It is, however, a requirement to avoid reactive power ripples which could set up oscillations within a power system. A particular problem with the measurement of amplitude will later be seen to be potentially slow (sub-Hz) oscillations in the measured value of fundamental voltage magnitude, due to aliased harmonics in high-THD environments.

BS EN 61000-4-30 (BSI, 2003), the specification for power quality measurement, specifies an accuracy of 0.1%, 0.001pu, which is measured over a 10-cycle timeframe. This error level is the same as the desired error level deduced above, but the response time is slightly slower than proposed in this thesis, by a factor of 2. Most power quality measurement devices are capable of high sample rates (≥ 80 samples per cycle), since they are designed to accurately measure harmonics up to the 40th. As mentioned above, the main barrier to be overcome in this thesis, as far as amplitude measurement accuracy is concerned, is to achieve this accuracy with much lower sample rates, down to 10 samples per cycle.

2.5 Current amplitude measurement speed and accuracy requirements

The emphasis of this thesis is on the measurement of voltages. However, all the proposed algorithmic methods are equally applicable to the measurement of currents (and thus to power flows by combining the voltage and current measurements at a node). In terms of measurement speed, overcurrent detection within a graded distribution network protection system does not need to be sub-cycle, but should not take much longer than 1 cycle. The measurement algorithm accuracy requirement for overcurrent detection is quite loose. Therefore, for relaying a single-cycle measurement is probably the most appropriate, and inaccuracy introduced by the digital algorithm will be of no significant

concern unless it becomes greater than that of the CT due to calibration and/or non-linearity. For a protection CT the standard accuracy might be poor at 10% but the linearity good over a range up to 10pu overcurrent (for a 10P10 protection CT) or the accuracy might be better (0.1%) but the linearity poorer under fault conditions (for a Class 0.1 instrumentation CT). (ARW, 2008).

For measurement of power flows, accuracy is more important and measurement times can be longer. A measurement in 5 cycles to match the voltage measurement target is sensible. By far the biggest contributor to the accuracy of the current measurement will be the calibration and linearity of the CT (with associated instrumentation), and how the range of the ADC is set (relative to rated current and potential overcurrent ratio). This is discussed further in section 2.9.

2.6 Phase measurement speed and accuracy requirements

The measurement of phase is not required for fast relaying operations, so a 5-cycle measurement is perfectly acceptable. The phase measurement may be used for one of several purposes (outside of inverter control systems):-

- As a subsection of a frequency measurement algorithm, in which case the phase measurement may be made over 1-cycle and then transformed into a frequency measurement via the rate-of-change-of-phase, before being further filtered
- For the assessment of unbalance via the calculation of negative sequence. To keep unbalance measurements accurate to 0.1% requires the phase measurements from each of the 3 phases to be accurate to $\pm 0.1^\circ$. This is because a set of 3 genuine balanced phase voltages with identical magnitudes, but measured relative phases of 0° , -120.1° & -239.9° (i.e. with 0.1° phase errors), results in a calculated unbalance of 0.1%.
- For the assessment of relative phase angles and loss-of-mains (LOM) conditions, where a relative measurement between two points can be made. This requires the two measurements to be made by the same system, by two systems with intimate (low-latency) communication, or by two systems which can timestamp the phase measurements accurately enough that communication latency problems are avoided. This can be achieved, for example, with GPS timestamp information. An acceptable error on such a phase measurement would be of the order of $>1^\circ$ for LOM detection. If used to assess or control power or VAR flow across a transmission line of cable, an accuracy of $<1^\circ$ might be desirable.
- For the calculation of power angles between voltages and currents. These power

angles are required to determine power factor, and the proportions of real and reactive power flowing on each phase. A measured relative phase error of 1° between a voltage/current pair, when the power flow was at unity power factor, would result in a perceived reactive power flow of $\sin(1^\circ)=0.017\text{pu}$, or a power factor of 0.99985 and is of no concern. The biggest concern with the error in VAR flow measurement would be its effect on a voltage target for a generator in islanded mode (Frequency/Voltage control) with, for example, a 10% voltage droop slope. The resulting voltage target would be shifted by $10\% \times 0.017=0.0017\text{pu}$. This also is of little concern, and would not cause a violation of the flicker limits of Table 2-7 (section 2.7.4) at any ripple frequency. A 1° phase measurement error is thus perfectly acceptable for power flow calculations.

Thus, a sensible target accuracy for phase measurements is $\pm 0.1^\circ$, being the requirement to measure unbalance to within $\pm 0.1\%$.

2.7 Required tolerance to signals with poor power quality

The amplitude, phase and frequency measurements discussed in this thesis must remain robust and accurate under conditions of relatively poor power quality. The expected levels of such disturbances within the UK distribution systems are given in BS EN 50160 (BSI, 2000). An additional useful resource is BS EN 61000-4-30 (BSI, 2003), which describes standard “influence quantities” which measurements must tolerate while still meeting specification, if they are to achieve “class A” accuracy rating.

Within a microgrid, the disturbances such as voltage dips, unbalance, flicker and harmonic content may be significant. The mechanisms for this are described in the following sub-sections. Algorithms to measure amplitude, phase and frequency must be as immune as reasonably possible to these effects, such that the accuracies desired in sections 2.1 to 2.6 can still be met, even during times of worst-case expected interference.

2.7.1 Unbalance

According to BS EN 50160 (BSI, 2000), unbalance should be “within the range 0 to 2%” for “95% of the 10-minute mean RMS values” of unbalance. This does not give a limit on the peak levels of unbalance which may appear for shorter times. BS EN 50160 also states that in some areas, “up to about 3%” may occur.

Within a microgrid scenario, some analysis is required to estimate if much higher figures might be reached. The root cause of increased levels of unbalance will be the increased statistical probability of larger proportional mismatches between the loads on each phase,

coupled with the lower fault levels (higher impedances) within the microgrid. In a large power system, the changing load magnitudes tend to balance on all three phases as there are many thousands or millions of individual loads, split amongst the phases in networks configured by the distribution companies. Also, many of the loads will be balanced three-phase industrial or commercial pieces of equipment. Within a small power system, it is possible that all loads might be single-phase connected, and it is possible that many loads could be active on one phase while far fewer are active on the other two phases. The resulting unbalance can be mitigated by adding 3-phase transformers (Δ - Y_g or Y_g - Y_g) (Hong, 1997) although this option may be impractical due to cost, weight, size or losses.

In the analysis of unbalance, care must be taken to specify exactly what is meant by the term unbalance. The “true” definition of unbalance, as per BS EN 61000-4-30 (BSI, 2003), is that

$$Unbalance(\%) = 100 \times \frac{NegativeSequenceRMSMagnitude}{PositiveSequenceRMSMagnitude} \quad (2.13)$$

However, an alternative, given by the IEEE (1991) is

$$Unbalance(\%) = 100 \times \frac{MaximumRMSPhaseDeviationFromAverage}{AveragePhaseRMS} \quad (2.14)$$

There are key differences between these two formulae. The IEEE definition does not include any phase information (which is required to calculate the negative sequence RMS value), but the IEC definition does not include any zero sequence information. Therefore, it is useful to analyse both the IEC and IEEE unbalance values, and the zero sequence value, in any detailed examination of unbalance.

To determine potential unbalance levels within microgrids, two scenarios are considered:-

- a) a 100kVA microgrid which receives its power from a stiff balanced voltage source via a reactance of 0.1pu. This system would be representative of a grid-connected system connected through a delta-star transformer with 0.1pu leakage reactance
- b) a 100kVA islanded system connected to a synchronous generator with leakage reactance 0.1pu, via a delta-star transformer, also of leakage reactance 0.1pu. A similar system would be achieved with an inverter connected via an LCL filter which includes a delta-star transformer, with total filter reactance 0.2pu. These are both realistic topologies.

These scenarios were modelled in Simulink, and the results from the islanded cases were, unsurprisingly, found to be the worst cases for unbalance. The model for the islanded case is shown in Figure 2-1.

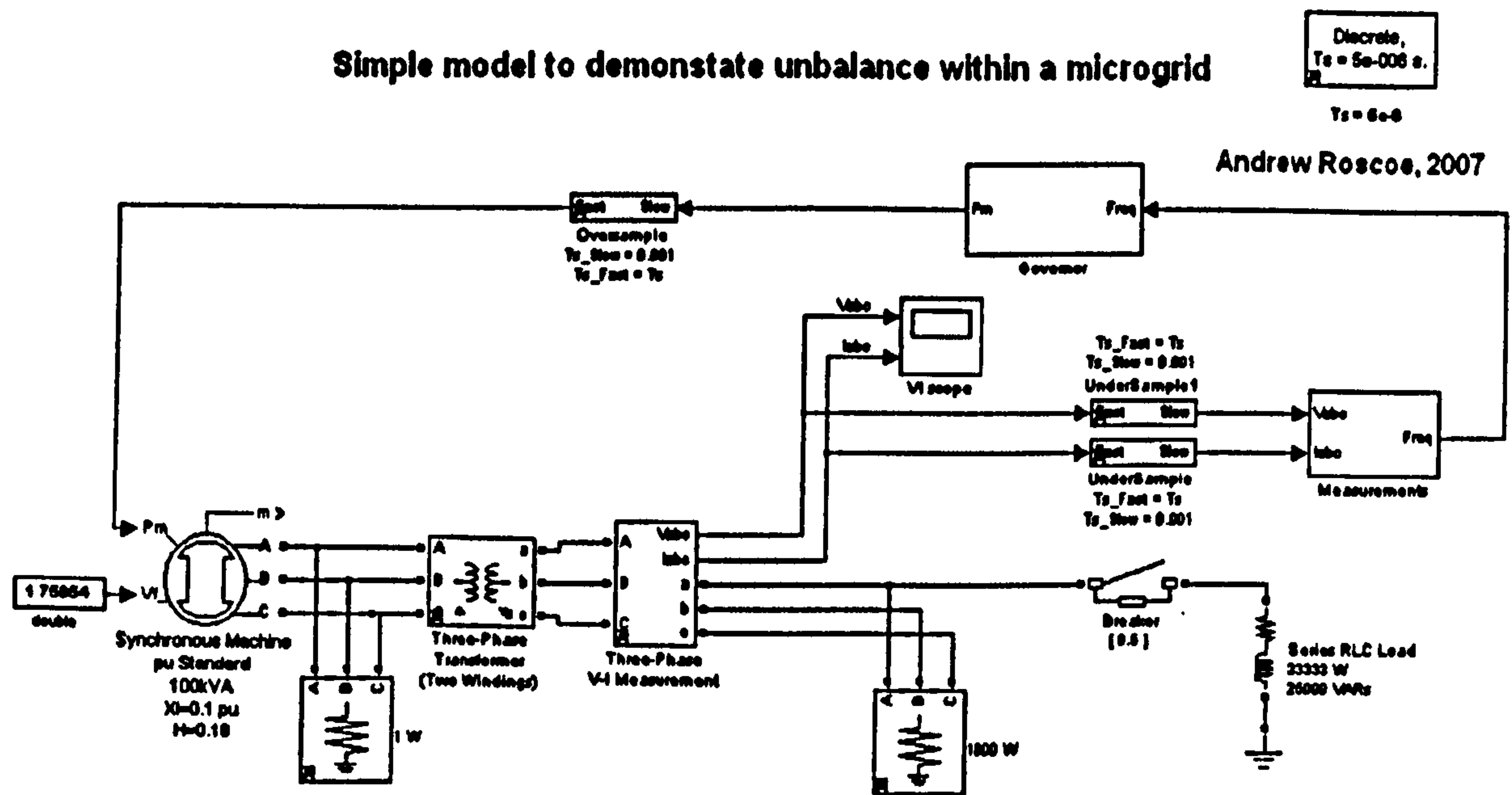


Figure 2-1 : Simulink model to evaluate scenarios of unbalance

The simulations began with very low loading on all three phases (just enough to keep the simulation stable at 5µs step time). During this initial phase, the load was balanced and the phase currents & voltages were also balanced; i.e. the negative sequence and zero sequence components of both current flows and voltages were zero. Then a large single-phase load was added to phase A. The vector magnitudes of the negative sequence and zero sequence components, relative to the positive sequence vector magnitude/phase were recorded, along with the unbalance as defined by the IEEE definition. The results are tabulated below.

Additional load on phase A	10000W	20000W	10000VAR	26667W +20000VAR (33.333kVA PF=0.8)
Normal Unbalance (%) Negative sequence RMS/ positive sequence RMS * 100	3.3 %	6.7 %	3.3 %	10.2 %
Negative sequence phase relative to positive sequence phase	-96°	-99°	-178°	-135°
Zero sequence unbalance (%) Zero sequence RMS / Positive sequence RMS * 100	0.6 %	1.1 %	0.6 %	1.7 %
Zero sequence phase relative to positive sequence phase	-93°	-95°	180°	-132°
IEEE unbalance (%)	2.2 %	4.5 %	4.3 %	11.2 %

Table 2-2 : Worst case unbalance and zero sequence scenarios

Notably, the unbalanced VAR loadings tend to cause a bigger unbalance between the phase RMS voltages, as reflected by the 10000W unbalance causing an IEEE unbalance of only 2.2% while a 10000VAR unbalance causes an IEEE unbalance of 4.3%. The unbalances of real power tend to cause a more subtle phase shifting effect between the phases, rather than a different RMS value on each phase. Unsurprisingly, the worst case is when the single phase is loaded at its nominal 1pu rating, which is one third of the overall three-phase rating of 100kVA, i.e. 33.333kVA, at a power factor of 0.8, while the two remaining phases are completely unloaded. In this condition, the unbalance reaches >10%, with an additional zero sequence effect of around 2%. This analysis justifies the use of these figures as upper limits on unbalance, during which a measurement device must operate at normal accuracy. The exact magnitudes and phases of the negative and zero sequence components for this worst case are used later in section 2.11 to recreate the unbalance voltage waveforms matching this worst scenario.

A further note on unbalance is that during single or two-phase faults, the system will be up to 100% unbalanced, with a negative sequence component approaching or equal in magnitude to the positive sequence component. These situations may appear only for a short duration, or may persist on a voltage measurement for much longer if, for example, fuses on 2 phases blow but the fuse on the third phase does not. This is a not uncommon situation (as has been experienced in the laboratory at Strathclyde). Any amplitude/phase/frequency measurement must be able to continue operation with sensible outputs during these unbalanced fault events. While even just a single phase measurement is valid, it is a requirement that a frequency measurement algorithm be able to continue operation, thus allowing amplitude/phase measurements on all three phases to also operate correctly. The accuracy of the frequency measurement algorithm may be reduced in this situation, but the algorithm must stay locked.

2.7.2 Harmonic content

The expected harmonic voltage content of LV systems is given by BS EN 50160 (BSI, 2000). The normal allowable levels of each individual harmonic on the voltage waveforms are shown in Figure 2-2. The total allowed voltage THD_v (Total Harmonic Distortion of voltage) should also be ≤ 8% for 95% of all 10-minute mean RMS values. This means that THD_v may be >8% for 5% of the 10-minute periods, and also that within the 10-minute periods, spot measurements of harmonics and THD_v may be significantly in excess of 8%. Generally, the expected levels of 2n (i.e. even) harmonics are low. The levels of 3n (i.e. 3rd, 6th, 9th etc.) harmonics are also desired to be low, since these set up large circulating currents in the delta windings of transformers (and are attenuated by this effect). This lower tolerance of 3n harmonics shows up most prominently in the specifications for 9th and 15th harmonics

which are well below the allowed values for 7th, 11th, 12th and 17th harmonics. The allowance of 3rd harmonic is also less than that of 5th harmonic. BS EN 50160 does not specify values for harmonics of higher order than 25, although it says they should be “small” and a value of <0.5% is implied.

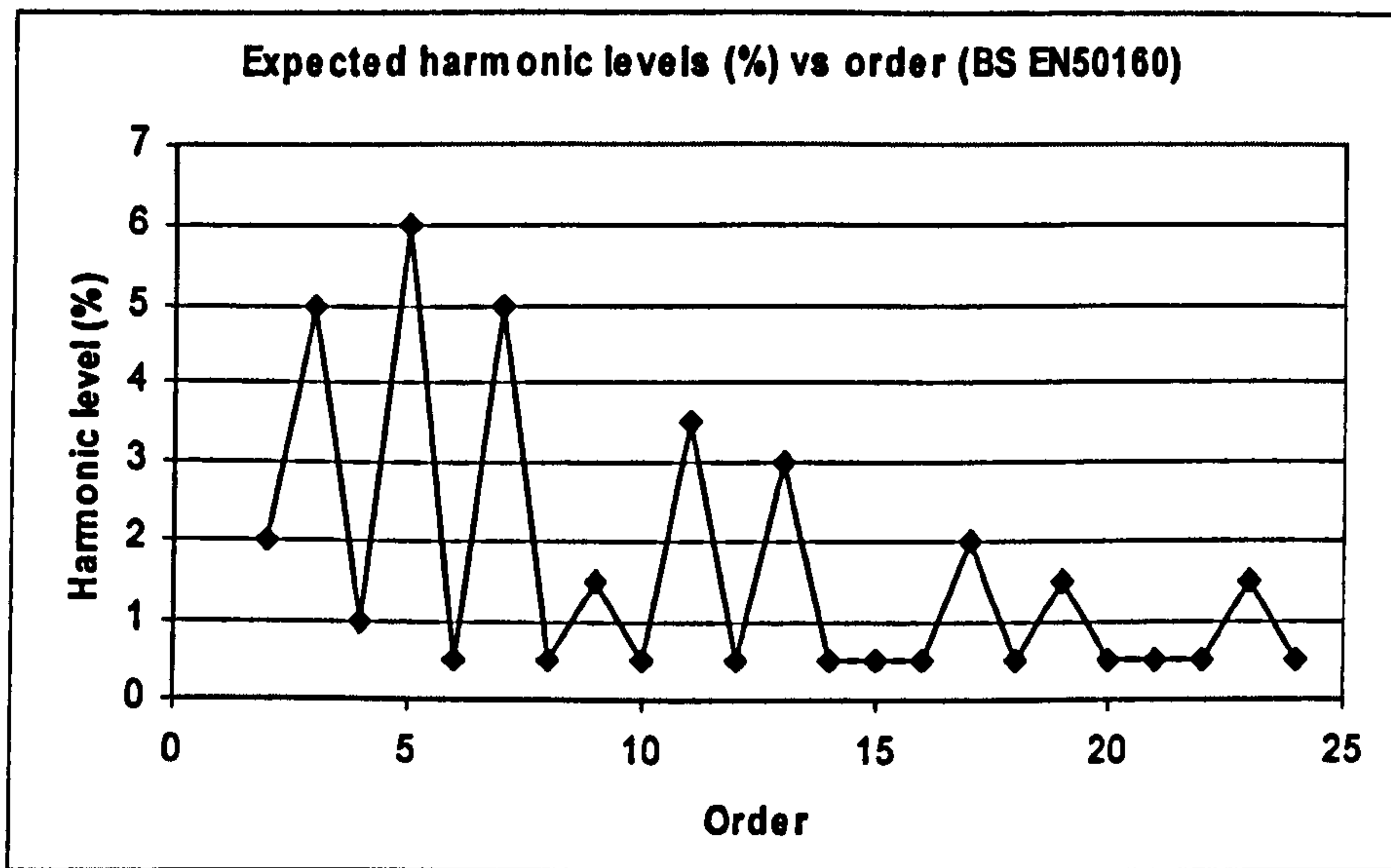


Figure 2-2 : Allowable harmonic levels under BS EN 50160 (BSI, 2000)

BS EN 61000-4-30 (BSI, 2003) expects instruments to meet specification with harmonic levels at “twice the values in IEC 61000-2-4, class 3” (BSI, 2002). Broadly, this equates to harmonics at a level 2.5x that of BS EN 50160, i.e. 2.5x the levels in Figure 2-2.

The chapter on harmonics in (CDA, 2007) suggests that common devices with the worst proportionate harmonic currents are:-

- Older PCs (~ 90% 3rd harmonic, ~70% 5th harmonic, ~50% 7th harmonic, ~30% 9th harmonic)
- Older Fluorescent lights with electronic ballasts (>70% 3rd harmonic, >40% 5th harmonic, ~40% 7th harmonic, ~40% 9th harmonic, ~30% 11th harmonic, ~25% 13th harmonic, ~20% 15th harmonic, ~15% 17th harmonic)
- Motor drives and UPS supplies

Some other devices such as welding equipment are worse, but are less numerous and also in use for shorter (and often sporadic) durations than the above equipment. The above equipment types are common, and are often running for many hours per day.

All these devices may be present within a microgrid scenario. By the list of “worst common devices” above, a valid worst case scenario could be considered as a 100kVA microgrid

feeding large numbers of older PCs and/or fluorescent lights. The microgrid could be supplied by a synchronous generator via a delta-star transformer, of total leakage reactance of 0.2pu (as in section 2.7.1). A relatively simple analysis is to calculate the resulting harmonic voltage levels as the voltage induced across a 0.2pu reactance due to dirty PC/lighting loads drawing a load of 1 pu current at the fundamental. Care must be taken to account for the fact that the source reactance will be larger by a factor of N for each harmonic number N. For example, this means that if the dirty load fundamental current is 1pu, with a harmonic current of 80% at the 3rd harmonic, this will cause a voltage harmonic at $1 \times 0.8 \times 0.2\text{pu} \times 3 = 0.48\text{pu}$, or 48%, due to the harmonic current flowing through the 0.2pu reactance. This will happen if the phases of the third harmonics are all the same; i.e. the load devices are all very similar. This could easily happen in a microgrid feeding PCs of similar brands and model, and similar lighting installations. Diversity in the loads connected would tend to reduce the resulting level of voltage harmonic, as any harmonic currents would become less correlated. Of course, the voltage distortion would also become less if the microgrid was “stiffer” which could be achieved by connection to a stiff parent power network via a transformer of higher rating (and therefore lower leakage reactance), or increasing the local generation capacity on-line.

Using this simple worst-case microgrid scenario, it is possible to estimate absolute worst-case harmonic levels within a microgrid containing only older PCs and fluorescent lights. Such a microgrid might exist if a data-centre was powered from a local generator in islanded mode.

Harmonic	Worst case harmonic current (relative to 1 pu fundamental)	Effective reactance (pu)	Worst case correlated voltage harmonic magnitude
3 rd	90%	0.6	54%
5 th	70%	1	70%
7 th	50%	1.4	70%
9 th	40%	1.8	72%
11 th	30%	2.2	66%
13 th	25%	2.6	65%
15 th	20%	3.0	60%
17 th	15%	3.4	51%

Table 2-3 : Potential worst case harmonic voltages within a microgrid, older PCs and fluorescent lights

It is evident that these potential levels are much worse than those specified by BS EN 50160. This microgrid would have severe problems due to the magnitude of the harmonic currents flowing and the increased transformer and generator core losses. These pieces of

equipment would have to be over-rated, the loads redesigned, or the proportion of older PCs and fluorescent lights lowered to make the microgrid viable.

Fortunately, the magnitude of this problem is mitigated somewhat by the appearance of BS EN 61000-3-2 (BSI, 2006) and also by the existence of ER G5/4, published by ENA (2005). G5/4 governs the harmonic currents from industrial and commercial equipment, and is specifically designed so that harmonic currents from new installations should not cause BS EN 50160 to be exceeded. BS EN 61000-3-2 addresses domestic and small appliances $\leq 16A$ per phase, most importantly PCs and fluorescent lighting circuits. The reason that BS EN 61000-3-2 addresses these appliances is because of the reasons shown above in Table 2-3 the large harmonic currents from older devices of these types, and the high probability that many of the same devices are operating for many hours at the same time within localised areas fed from the same transformers/feeders/generators. BS EN 61000-3-2 allows higher limits for appliances like tools, welding kits etc., on the assumption that these pieces of equipment are used less frequently, intermittently, and make up a small proportion of the load. PCs and fluorescent lighting circuits, however, are much more tightly regulated than the data from CDA suggests for older equipment. BS EN 61000-3-2 has been in force since 2001, so a reasonable assumption is that we can use the figures from BS EN 61000-3-2 for new analyses.

BS EN 61000-3-2 gives harmonic current specifications for PCs and fluorescent lights up to the 40th harmonic. The values for PCs are quoted (in BS EN 61000-3-2) in mA/W, which can be approximately converted into percentage harmonic currents. The specifications are shown in Table 2-4. The lighting specifications are much tighter than data from Table 2-3, but the lower order harmonic currents for PCs are still very high¹. This means that a microgrid consisting entirely of PCs would need to have an over-rated connection to a parent network, or increased generation on-line. However, a reasonable scenario for a microgrid might be to have 50% of the electrical load as PCs, and 50% as lights. Even this limited diversity of loads improves the situation. Data in Table 2-4 is given for up to the 39th harmonic. Although the harmonic currents at the higher harmonic numbers are small, in the region of 3%, these numbers get multiplied by the harmonic number N when converted into harmonic voltages, due to the reactance at the increased harmonic frequency.

¹ Actual measurements of such high levels of harmonic currents from domestic appliances can be seen in Appendix H, "Logged domestic voltage and current waveforms".

Harmonic	Fluorescent lighting harmonic currents (relative to fundamental)	PC harmonic currents (relative to fundamental)
2	2%	
3	30%	78.5%
5	10%	43.9%
7	7%	23.1%
9	5%	11.6%
11	3%	8.1%
13	3%	6.8%
15	3%	5.9%
17	3%	5.2%
19	3%	4.7%
21	3%	4.2%
23	3%	3.9%
25	3%	3.6%
27	3%	3.3%
29	3%	3.1%
31	3%	2.9%
33	3%	2.7%
35	3%	2.5%
37	3%	2.4%
39	3%	2.3%

Table 2-4 : Harmonic currents for fluorescent lights and PCs in BS EN 61000-3-2 (BSI, 2006)

However, it is reasonable to assume that at the 40th harmonic (2000Hz for a 50 Hz system), the harmonic currents summed from all PC and lighting loads are likely to be uncorrelated, even if the devices are similar. Therefore, if there are M separate PCs and lights within the microgrid, the effect of the harmonic currents at the 40th harmonic will be attenuated by $1/M$ due to the currents adding in an uncorrelated RMS rather than a coherent superposed manner. Within a 100kVA microgrid with PCs and lights of around 100W each, M will be about 1000, making the $1/M$ factor 0.031 at the 40th harmonic. A linear taper of this “correlation factor” can be applied between the 2nd to 40th harmonics, with the 2nd harmonics entirely correlated and the 40th harmonics entirely uncorrelated. This linear taper is estimated and not based on hard data. Not including a taper of this kind would, however, result in a vast overestimate of harmonic voltage levels (which will be seen to be very high even with the taper applied), so it is better to include an estimated taper function than not to apply one at all. When this factor is included, and using the example of a 100kVA microgrid with 50% PC loads and 50% lighting loads, the resulting voltage harmonics are shown in Figure 2-3 and Table 2-5.

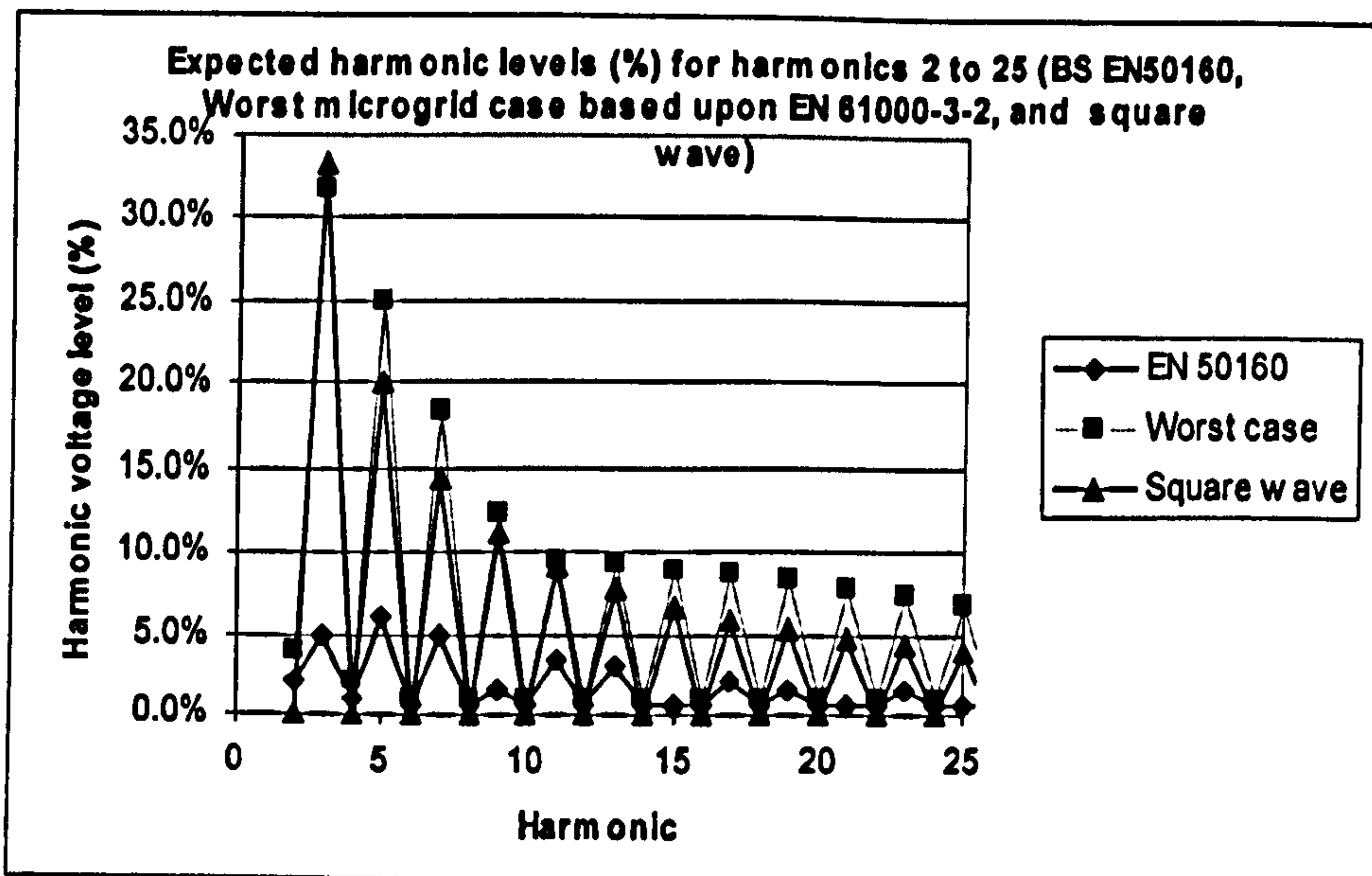


Figure 2-3 : Worst case harmonic voltage levels in a microgrid due to modern PCs and fluorescent lights

Order	BS EN50160	BS EN50160	Xfmr	Uncorrelation	PC	Lighting	Overall	Overall	Harmonic level (%)
	(%)	After multiplier	Effective Reactance		factor	harmonic currents	harmonic currents	harmonic currents	voltage harmonics
		(%)	pu		EN 61000-3-2				
2	2.0%	4.0%	0.4	1.000		2%	1.0%	0.4%	4.0%
3	5.0%	10.0%	0.6	0.975	78.5%	30%	52.9%	31.7%	31.7%
4	1.0%	2.0%	0.8	0.949			0.0%	0.0%	2.0%
5	6.0%	12.0%	1	0.924	43.9%	10%	24.9%	24.9%	24.9%
6	0.5%	1.0%	1.2	0.898			0.0%	0.0%	1.0%
7	5.0%	10.0%	1.4	0.873	23.1%	7%	13.1%	18.4%	18.4%
8	0.5%	1.0%	1.6	0.847			0.0%	0.0%	1.0%
9	1.5%	3.0%	1.8	0.822	11.6%	5%	6.8%	12.2%	12.2%
10	0.5%	1.0%	2	0.796			0.0%	0.0%	1.0%
11	3.5%	7.0%	2.2	0.771	8.1%	3%	4.3%	9.4%	9.4%
12	0.5%	1.0%	2.4	0.745			0.0%	0.0%	1.0%
13	3.0%	6.0%	2.6	0.720	6.8%	3%	3.5%	9.2%	9.2%
14	0.5%	1.0%	2.8	0.694			0.0%	0.0%	1.0%
15	0.5%	1.0%	3	0.669	5.9%	3%	3.0%	9.0%	9.0%
16	0.5%	1.0%	3.2	0.643			0.0%	0.0%	1.0%
17	2.0%	4.0%	3.4	0.618	5.2%	3%	2.5%	8.6%	8.6%
18	0.5%	1.0%	3.6	0.592			0.0%	0.0%	1.0%
19	1.5%	3.0%	3.8	0.567	4.7%	3%	2.2%	8.3%	8.3%
20	0.5%	1.0%	4	0.541			0.0%	0.0%	1.0%
21	0.5%	1.0%	4.2	0.516	4.2%	3%	1.9%	7.8%	7.8%
22	0.5%	1.0%	4.4	0.490			0.0%	0.0%	1.0%
23	1.5%	3.0%	4.6	0.465	3.9%	3%	1.6%	7.3%	7.3%
24	0.5%	1.0%	4.8	0.439			0.0%	0.0%	1.0%
25	0.5%	1.0%	5	0.414	3.6%	3%	1.4%	6.8%	6.8%
26	0.5%	1.0%	5.2	0.388			0.0%	0.0%	1.0%
27	0.5%	1.0%	5.4	0.363	3.3%	3%	1.1%	6.2%	6.2%
28	0.5%	1.0%	5.6	0.337			0.0%	0.0%	1.0%
29	0.5%	1.0%	5.8	0.312	3.1%	3%	0.9%	5.5%	5.5%
30	0.5%	1.0%	6	0.288			0.0%	0.0%	1.0%
31	0.5%	1.0%	6.2	0.261	2.9%	3%	0.8%	4.7%	4.7%
32	0.5%	1.0%	6.4	0.235			0.0%	0.0%	1.0%
33	0.5%	1.0%	6.6	0.210	2.7%	3%	0.6%	3.9%	3.9%
34	0.5%	1.0%	6.8	0.185			0.0%	0.0%	1.0%
35	0.5%	1.0%	7	0.159	2.5%	3%	0.4%	3.1%	3.1%
36	0.5%	1.0%	7.2	0.134			0.0%	0.0%	1.0%
37	0.5%	1.0%	7.4	0.108	2.4%	3%	0.3%	2.2%	2.2%
38	0.5%	1.0%	7.6	0.083			0.0%	0.0%	1.0%
39	0.5%	1.0%	7.8	0.057	2.3%	3%	0.2%	1.2%	1.2%
40	0.5%	1.0%	8	0.032			0.0%	0.0%	1.0%

Table 2-5 : Worst case harmonic voltage levels in a microgrid: 50% fluorescent lights, 50% computers, 0.2pu source impedance

Here, double the value of BS EN 50160 has been used to estimate the worst case even harmonics which are not specified within BS EN 61000-3-2. Notably, the expected level of voltage harmonics is not dissimilar to the levels which would synthesise a square wave. The potential harmonic levels are much worse than BS EN 50160 suggests or allows. If this scenario arose within a conventional UK distribution network, remedial action would be urgently required, either in the form of load removal/redesign, active harmonic cancellation, or stiffening of the grid connection (reduction of impedance).

To illustrate how the harmonic currents in this scenario would cause problems within a grid-connected network, a “K factor analysis” can be performed for the source transformer. The K factor (CDA, 2007) is calculated as

$$K = \sum_{h=2}^{h=h_{\max}} h^2 I_h^2 \quad (2.15)$$

where h is the harmonic number and I_h is the proportion of current at harmonic h , relative to the fundamental current magnitude. Performing this analysis on the data in Table 2-4 and Table 2-5, with an average harmonic current formed by a 50% loading of PCs and a 50% loading of lighting, leads to a K factor of 7.0. This means that the approximate core losses in the transformer will be 7 times the core current losses for sinusoidal currents. The transformer must therefore be significantly over-rated to avoid overheating and this is expensive.

The scenario of primary concern within the scope of this thesis is the islanded operation of a local power system containing “dirty loads” (with high harmonic current content). During normal operation, this power system would need to be grid-connected via a relatively low impedance path (i.e. a transformer of high rating) such that the resulting voltage harmonics did not cause violation of the BS EN 50160 limits. This power system might at times be operated in islanded mode using local generation only, for strategic or emergency reasons. The generator/transformer impedance may be significantly higher than the usual grid-connected path impedance. This will result in a lower fault level, and higher harmonic content of the voltage waveforms of the islanded system, by the mechanisms described above. Thus, in this islanded scenario, the harmonic voltage levels of Figure 2-3 and Table 2-5 could in theory arise, if only transiently, and despite the fact that BS EN 50160 would be significantly violated.

To create a consistent test waveform with the above harmonic content, the phases of the harmonics must also be set. Using the standard mathematical formula for synthesising a square wave:-

$$\frac{4}{\pi} \sin(\omega t) + \frac{1}{3} \sin(3\omega t) + \frac{1}{5} \sin(5\omega t) + \dots \text{ (square wave outputting -1 or +1)}$$

(2.16)

and considering that most rectification devices such as power supplies and fluorescent ballasts tend to draw most current at the peak of the cycle, it makes sense to add the odd harmonics with phase offsets of zero such that they add in a fashion which tends to form a sinusoid with the peak clipped. This in the extreme becomes a square wave. This most closely approximates the clipped peaks seen in practice due to such harmonic loads. The even harmonics are considered to have random phases and do not correlate in the same way as the odd harmonics. Applying the worst case expected odd and even harmonics in this manner results in the extremely poor voltage waveform shown in Figure 2-4. The THD_v of this waveform is 53%. Management of harmonic load currents will be important within microgrids to avoid abnormal waveforms such as this. However, the important point here is that measurement algorithms and control software should be able to cope with such poor waveforms, even if they occur transiently for only a few cycles, without becoming confused or giving inaccurate answers.

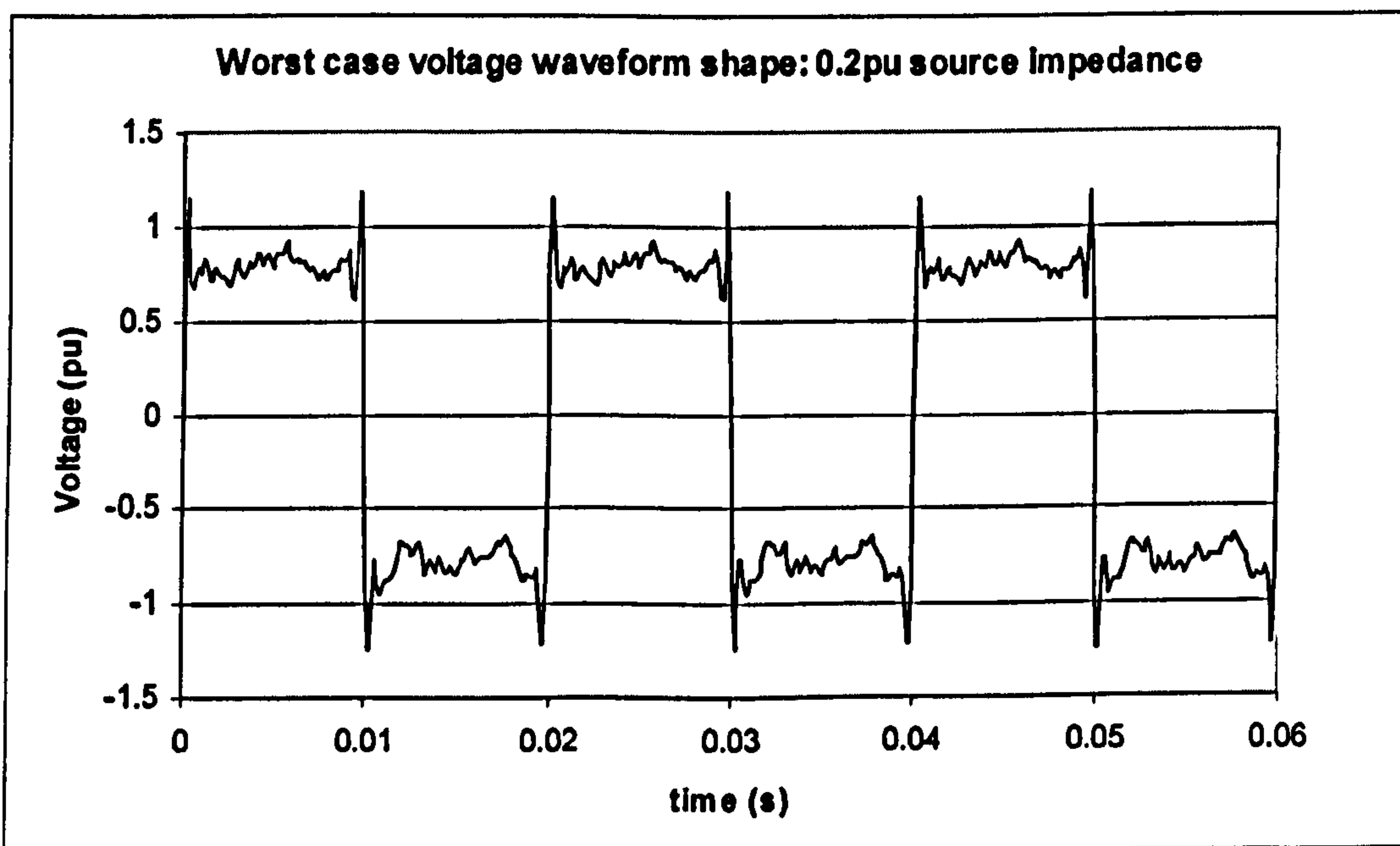


Figure 2-4 : Worst case voltage waveform shape expected within a microgrid: 50% fluorescent lights, 50% computers, 0.2pu source impedance

Although the voltage waveform in Figure 2-4 will be used in this thesis as the worst-case harmonic waveform to test measurement algorithms, its shape is worse than one would hope or expect to see on an AC microgrid for anything more than a few cycles. To demonstrate the way that this poor waveform could be improved in practice, the analysis of section 2.7.2 can be repeated, but using a 0.1pu source impedance instead of a 0.2pu source impedance. In practical terms, this would be achieved by transformer/generator

up-sizing, to reduce either transformer impedance or generator source reactance, or both. The scenario still contains the load made up of 50% fluorescent lights and 50% computers.

The THD_v of this waveform is 28.2%. Compared to Figure 2-4, this waveform is much improved but still highly undesirable.

Order	BS EN50160	BS EN50160	Xfmr	Uncorrelation factor	PC	Lighting	Overall	Overall	Harmonic level (%)
	(%)	After multiplier (%)	Effective Reactance pu		harmonic currents	harmonic currents	harmonic currents	voltage harmonics	Made at least 2x BS EN 50160 levels
					EN 61000-3-2				
2	2.0%	4.0%	0.2	1.000		2%	1.0%	0.2%	4.0%
3	5.0%	10.0%	0.3	0.975	78.5%	30%	52.9%	15.9%	15.9%
4	1.0%	2.0%	0.4	0.949			0.0%	0.0%	2.0%
5	6.0%	12.0%	0.5	0.924	43.9%	10%	24.9%	12.4%	12.4%
6	0.5%	1.0%	0.6	0.898			0.0%	0.0%	1.0%
7	5.0%	10.0%	0.7	0.873	23.1%	7%	13.1%	9.2%	10.0%
8	0.5%	1.0%	0.8	0.847			0.0%	0.0%	1.0%
9	1.5%	3.0%	0.9	0.822	11.6%	5%	6.8%	6.1%	6.1%
10	0.5%	1.0%	1	0.798			0.0%	0.0%	1.0%
11	3.5%	7.0%	1.1	0.771	8.1%	3%	4.3%	4.7%	7.0%
12	0.5%	1.0%	1.2	0.745			0.0%	0.0%	1.0%
13	3.0%	6.0%	1.3	0.720	6.8%	3%	3.5%	4.6%	6.0%
14	0.5%	1.0%	1.4	0.694			0.0%	0.0%	1.0%
15	0.5%	1.0%	1.5	0.669	5.9%	3%	3.0%	4.5%	4.5%
16	0.5%	1.0%	1.6	0.643			0.0%	0.0%	1.0%
17	2.0%	4.0%	1.7	0.618	5.2%	3%	2.5%	4.3%	4.3%
18	0.5%	1.0%	1.8	0.592			0.0%	0.0%	1.0%
19	1.5%	3.0%	1.9	0.567	4.7%	3%	2.2%	4.1%	4.1%
20	0.5%	1.0%	2	0.541			0.0%	0.0%	1.0%
21	0.5%	1.0%	2.1	0.516	4.2%	3%	1.9%	3.9%	3.9%
22	0.5%	1.0%	2.2	0.490			0.0%	0.0%	1.0%
23	1.5%	3.0%	2.3	0.465	3.9%	3%	1.6%	3.7%	3.7%
24	0.5%	1.0%	2.4	0.439			0.0%	0.0%	1.0%
25	0.5%	1.0%	2.5	0.414	3.6%	3%	1.4%	3.4%	3.4%
26	0.5%	1.0%	2.6	0.388			0.0%	0.0%	1.0%
27	0.5%	1.0%	2.7	0.363	3.3%	3%	1.1%	3.1%	3.1%
28	0.5%	1.0%	2.8	0.337			0.0%	0.0%	1.0%
29	0.5%	1.0%	2.9	0.312	3.1%	3%	0.9%	2.7%	2.7%
30	0.5%	1.0%	3	0.286			0.0%	0.0%	1.0%
31	0.5%	1.0%	3.1	0.261	2.9%	3%	0.8%	2.4%	2.4%
32	0.5%	1.0%	3.2	0.235			0.0%	0.0%	1.0%
33	0.5%	1.0%	3.3	0.210	2.7%	3%	0.6%	2.0%	2.0%
34	0.5%	1.0%	3.4	0.185			0.0%	0.0%	1.0%
35	0.5%	1.0%	3.5	0.159	2.5%	3%	0.4%	1.5%	1.5%
36	0.5%	1.0%	3.6	0.134			0.0%	0.0%	1.0%
37	0.5%	1.0%	3.7	0.108	2.4%	3%	0.3%	1.1%	1.1%
38	0.5%	1.0%	3.8	0.083			0.0%	0.0%	1.0%
39	0.5%	1.0%	3.9	0.057	2.3%	3%	0.2%	0.8%	1.0%
40	0.5%	1.0%	4	0.032			0.0%	0.0%	1.0%

Table 2-6 : Worst case harmonic voltage levels in a microgrid: 50% fluorescent lights, 50% computers, 0.1pu source impedance

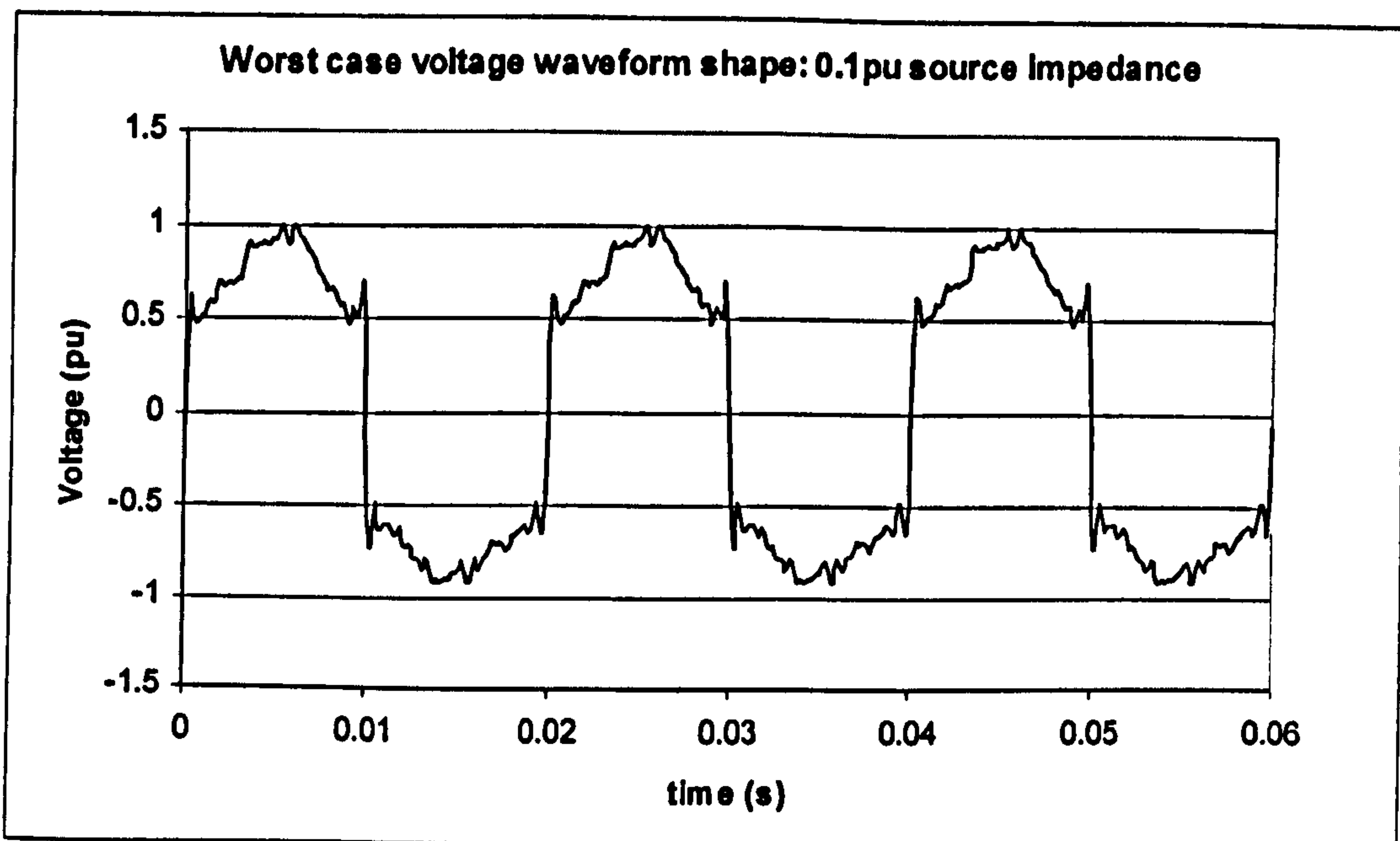


Figure 2-5 : Worst case voltage waveform shape expected within a microgrid: 50% fluorescent lights, 50% computers, 0.1pu source impedance

2.7.3 Inter-harmonic content

Inter-harmonics are caused from two main sources.

The first source is devices which switch at frequencies unrelated to the fundamental frequency. An example would be an inverter-connected generator. The switching transistors or IGBTs are connected to the power system via an LC or LCL filter which smoothes out the fast switching pulses to achieve an approximately smooth sinusoidal voltage and current waveform. Typically, the primary inductor has a reactance of ≈ 0.15 pu, and the LC filter cut-off frequency is set at around 500Hz for a sensible switching frequency which typically may be in the range 2-20kHz. The worst case voltage inter-harmonic results when the inverter is feeding an islanded power system, and the inverter is lightly loaded or open circuit, as the switching pulses are smoothed only by the LC filter and not by an LC-LR filter which is formed if a load R is added. The voltage gain of the LC filter is given by {B.4}. The worst case attenuation of a 2025Hz switching frequency with a 500Hz resonant LC frequency is therefore about 15 (24dB), leading to an inter-harmonic at 2025Hz of 6.5%. BS EN 50160 does not regulate these inter-harmonics as yet, although allowable levels are "under consideration, pending more experience". It does, however, correctly note that some inter-harmonics can be regarded as a form of flicker (see section 2.7.4).

Other inter-harmonics can be caused by devices which communicate via power lines. BS EN 50160 limits these signals to the levels shown in Figure 2-6, over 99% of a day, measured as

the three-second mean signal voltage levels. Note that this means the signals may transiently be higher than this. Also, multiple interfering signals may be present simultaneously with components at several frequencies, although Figure 2-6 gives no indication of the spectral density expected. This is a serious ambiguity in the BS EN 50160 specifications. A reasonable way of simulating such signals is to create a square wave at a sensible signalling bit rate. The square wave will introduce a spread of signals by equation (2.16). Since the maximum fundamental component of the signalling spectrum at the signalling bit rate might have a temporary maximum level twice that of Figure 2-6, then the square wave magnitude of the signalling voltage might be $2 \times 9\% \times 4/\pi = 23\%$ relative to the nominal voltage magnitude, at a frequency of 525Hz. This is a large interfering signal! It is hard to believe that such a signal would a) be acceptable and b) possibly be injected, due to the large power levels required from the signalling device. However BS EN 50160, as it stands, allows signals of this magnitude to be present on mains voltages.

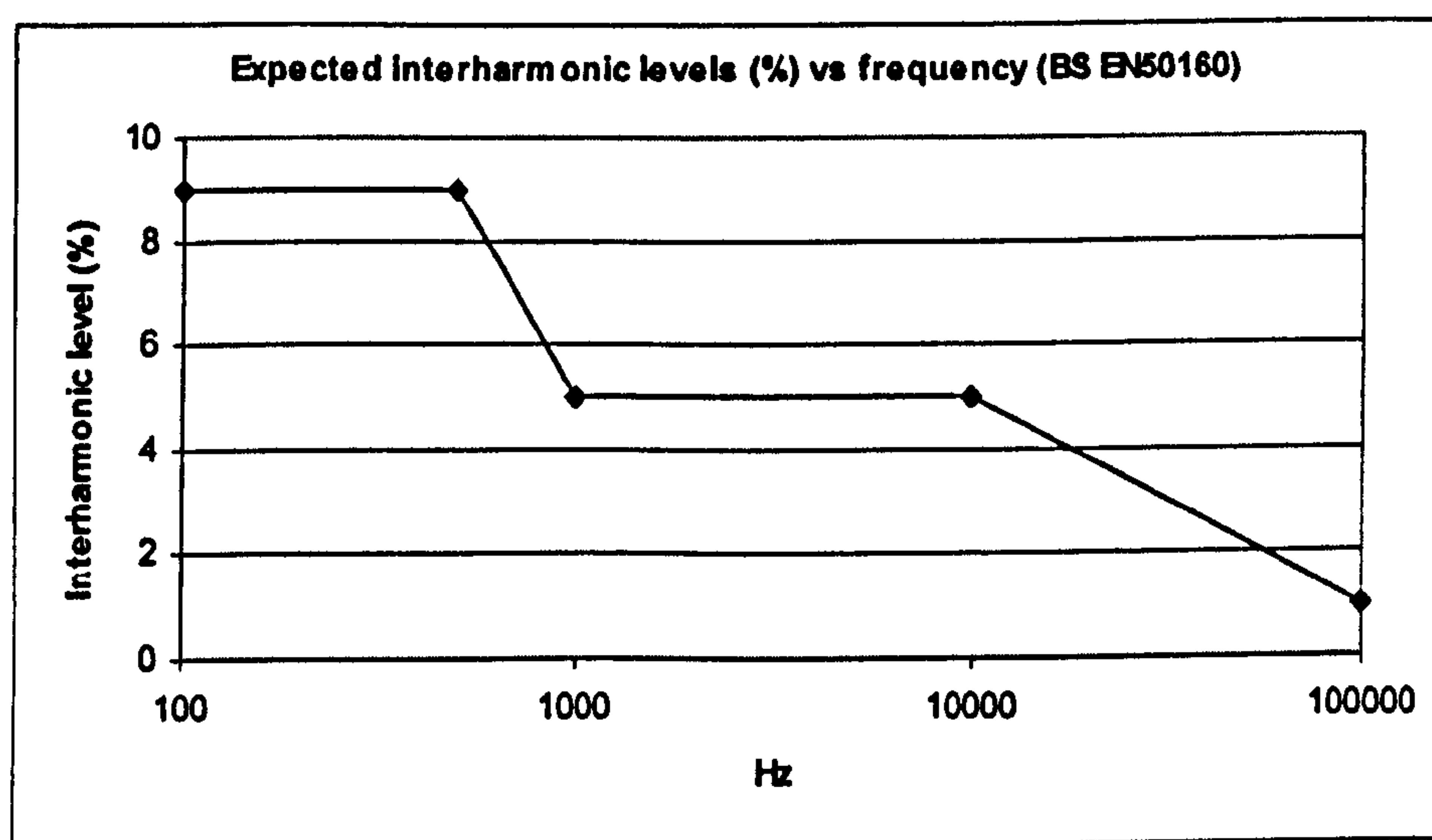


Figure 2-6 : Expected average inter-harmonic levels due to signalling, from BS EN 50160

In a worst-case voltage waveform, used to test measurement algorithms, the following interfering signals should therefore be included:-

- A 6.5% sinusoidal inter-harmonic at 2025Hz (to simulate inverter generation or local customer communication)
- A 23% square wave at 525Hz, to simulate utility power-line communication

2.7.4 Flicker

Flicker is a modulation of the voltage sine wave envelope at frequencies from <1Hz to >1000Hz. However at frequencies >25Hz the flicker can be regarded instead as an inter-harmonic, and at frequencies <<1Hz the flicker is not really repetitive but more a succession of steps in voltage. The analysis here focuses on the 0.1Hz to 25Hz band. The

primary concern of flicker is the “annoyance” it causes to people due to the varying brightness of incandescent light bulbs at frequencies within this band. The method of flicker measurement is relatively complicated, and is defined in BS EN 61000-4-15 (BSI, 1998). The measurement is designed to output numbers for P_{st} and P_{lt} , short and long-term average values, which represent the perceived annoyance caused by a flickering lamp. The allowed values of P_{st} and P_{lt} are laid down in BS EN 50160. P_{st} is measured over 10 minutes, and P_{lt} is an average of 12 consecutive P_{st} values over 2 hours. P_{lt} must be ≤ 1 for 95% of the time.

P_{st} and P_{lt} are determined statistically from the “real-time flicker sensation” output of a multi-stage filter, which includes a band-pass filter centred on 8.8Hz which is the most annoying flicker frequency to the human eye/brain (BSI, 1998). The filters were originally purely analogue devices, and digital implementations need to be coded carefully to accurately match the performance of the analogue equivalents. The statistical analysis is based upon empirical analysis and experiments with people subjected to different frequencies and depths of flicker.

The “real-time flicker sensation” output from block 4 of the flicker meter (BSI, 1998) is converted into P_{st} by the following formula:-

$$P_{st} = \sqrt{0.0314P_{0.1} + 0.0525P_1 + 0.0657P_3 + 0.28P_{10} + 0.08P_{50}} \quad (2.17)$$

where $P_{0.1}$, P_1 , P_3 , P_{10} , P_{50} are the real-time flicker levels exceeded for 0.1%, 1%, 3%, 10% and 50% of the time within a 10-minute window. Thus, a constant flicker level of 1.962 will lead to $P_{st}=1$, which is the BS EN 50160 limit. However, flicker levels of just below $1/0.0314=31.85$ which only occur for 0.1% or less of the 10 minute window (0.6 seconds) may not cause P_{st} to rise above 1 if the flicker level is very low for the remaining 99.9% of the time.

BS EN 61000-4-15 gives example values of steady sinusoidal and square-wave modulation depths and frequencies which cause P_{st} to equal 1. These are given in Table 2-7.

Analysis of the flicker meter specified by BS EN 61000-4-15 reveals that the real-time flicker sensation is proportional to the step magnitude squared. Thus, at 1620 steps per minute (13.5 Hz modulation), a step magnitude of $0.402\% \times \sqrt{31.85/1.962} = 1.62\%$ will give rise to a real-time flicker level of 31.85. A short-term flicker level this high for only 0.6 seconds will cause P_{st} calculated over 10 minutes to be 1, the BS EN 50160 limit. This

could be regarded as a worst-case acceptable flicker magnitude and frequency within a normal UK grid-connected system.

Voltage changes per minute	Step magnitude (% of nominal)
1	2.724%
2	2.211%
7	1.459%
39	0.906%
110 (0.9 Hz modulation)	0.725%
1620 (13.5 Hz modulation)	0.402%
4000	2.4%

Table 2-7 : Voltage step changes to cause Pst=1 in a 50Hz system

An alternative viewpoint is to examine microgrids with a weak network connection and a relatively large amount of installed wind generation. The inductive impedance of the network connection is not of prime importance, as we imagine that the wind turbines design allows them to operate at unity power factor. However, gusty wind will inevitably lead to fluctuating real power flows across this boundary, and a resulting fluctuating voltage magnitude due to the resistance of the network connection. A simple scenario is for a rural farm connected via an 11kV overhead line to a stiff grid. The maximum capacity of this line is >4MVA (see appendix C.1). Assuming that the actual connected load is 500kVA or less, then by equation {B.3}, the maximum line length could be 24km (setting k to 0.1 in {B.3}), which is a realistic line length in some rural areas. If the farm has 100kW of installed wind capacity, then gusty wind could cause a 100kW fluctuation in real power flow across this 24km line, equating to 5A RMS per phase. The resistance of the 24km line would be about 15Ω (by Tab. C-1). The resulting voltage drop between a single phase and neutral of the 11kV system at the farm connection would be $5A \times 15\Omega = 75V$ RMS. Relating this to the nominal phase-neutral value of $11000/\sqrt{3}$ gives a 1.2% fluctuation.

A second scenario is for a similar 100kW fluctuation to occur in a 400V cable-connected microgrid of capacity up to 200kVA. If the cable connection is 500m long, with $0.25\Omega/\text{km}$, then the 100kW power fluctuation causes a 144A RMS fluctuation, which leads to an 18V RMS drop in phase voltage. Expressed at a percentage of nominal 231V, this is almost 8%. Thus, one source of bad flicker may be encountered when the LV connection length is long, and there are substantial fluctuating power flows due intermittent generation or loads.

A reasonable limit on flicker step size is therefore 8%, partly by the analysis above and partly because larger steps will risk tripping due to under-overvoltage. It is unlikely that such steps will occur at the worst frequency for flicker (8.8Hz), but BS EN 61000-4-30 specifies that power quality meters must operate within specification with flicker levels of P_{st} up to 20. To achieve $P_{st}=20$ requires equation (2.17) to give 20. Reversing (2.17) leads to a constant level of real-time flicker of 785. At 13.5Hz, the constant repeating step magnitude to achieve a real-time flicker of 785 is $0.402\% \times J(785/1.962) = 8\%$! A square wave modulation at 13.5Hz of size 8% is an extremely unpleasant prospect, and, similarly to the worst-case harmonic and inter-harmonic levels deduced in sections 2.7.2 and 2.7.3, will hopefully never be encountered for any length of time. The fact remains, however, that such effects may appear, if only for a few cycles. Since the measurements addressed in this thesis are made on the same timescales of a few cycles, the measurements must be able to cope with these effects.

2.7.5 Tolerance to voltage dips and surges

Voltage dips and surges occur on power networks due to switching, faults, and other disturbances.

Electrical loads are generally designed to withstand voltage dips and surges of certain magnitudes and durations. There are several different design curves which have evolved over time (CDA, 2007), of which three are:-

- the CBEMA (Computer and Business Equipment Manufacturers Association) curve
- the ITIC (Information Technology Industry Council) curve.
- the ANSI IEEE 446

The curves are all similar. A copy of the CBEMA curve is shown in appendix C.2. Equipment is usually designed to operate without malfunction for the voltage dips and surges within the upper and lower bounds. Useful example points are that a 100% voltage dip should be survivable for 20ms, and that a 20% dip should be survivable for about 1 second. Of course, dips and surges of $\leq \pm 10\%$ must be survivable indefinitely since this is the steady-state voltage range specification. BS EN 50160 gives some more anecdotal information, which is that most dips have durations of <1 second and a depth of <60% (i.e. dips to $\geq 0.4pu$). In some areas where grids are weak, 10-15% dips can occur frequently.

A useful reference is IEEE 1547 (IEEE, 2003) which describes the current standard for interconnecting distributed generation to electric power systems in the US. The guidelines and required trip times given in this document are pertinent to microgrid applications. In

the future the requirements may become looser or tighter as microgrid and distribution network control technology advances, to account for higher penetrations of distributed generation. Table 1 of IEEE 1547 lists the required total clearing times (from the start of the abnormal condition to actual disconnection), for various voltage dips and surges. This table is recreated here:-

Voltage range (% of base voltage)	Maximum clearing time(s)
$V < 50$	0.16
$50 \leq V < 88$	2.00
$110 < V < 120$	1.00
$V \geq 120$	0.16

Table 2-8 : Under/Overvoltage clearing times required under IEEE 1547

A similar table is also contained within ER G59/1 (ENA, 1991), the guidelines for connecting distributed generation in the UK, up to 5MW or 20kV:-

Protection	Phases	Trip setting	Maximum clearing time(s)
Under-voltage	All	-10% (phase-neutral)	0.5
Over-voltage	All	+10% (phase-neutral)	0.5
Under-frequency	1	-6%	0.5
Over-frequency	1	+1%	0.5

Table 2-9 : Protective equipment and settings for LV supply arrangements

The required tripping times define the maximum allowable reaction time for voltage amplitude measurements which are used for over/undervoltage relaying. To meet the required tripping time, the reaction time of the measurement & digital processing plus the reaction time of the breaker must be less than the shortest time on Table 2-8 (160ms). Accounting for a time of between 40ms for an air-blast breaker (Laughton, 2003) and 100ms for an oil-filled breaker (Areva T&D, 2007) for contacts to open and arcs to be extinguished, then approximately 60ms still remains available for the latency of the measurement and processing. This is 3 cycles, of which some time will be lost due to the group delay within anti-aliasing filters etc. Therefore, the requirement for a <2 cycle digital processing time quoted in section 2.4 is justified. Provided the amplitude/phase measurements have a valid estimate of frequency, voltage measurement algorithms for under-voltage/over-voltage relaying activities should respond accurately within this timeframe.

In terms of frequency measurement, however, all the data above needs to be regarded in

a different way. Now, the requirement is that a frequency measurement algorithm must continue to give a sensible output during such events. The events may include a full 3-phase fault with all three phase voltages at 0pu. For allowable lengths of time, the local breaker should not be tripped, to allow local equipment which can ride through a brownout, to do so. If the frequency measurement algorithm cannot ride through the event, then one of a number of things may occur:-

- A spurious under/over-frequency trip
- A spurious under/over-voltage trip, due to amplitude/phase measurement algorithms being given the wrong value of frequency
- A spurious LOM (loss of mains) trip, if the loss-of-mains protective algorithm uses any combination of the frequency, amplitude or phase measurements, on any combination of phases.

So, if a full 3-phase to ground fault or momentary disconnection occurs, the frequency measurement algorithm must be able to hold its output at some last known "good" value, for a configurable time, before being forced to revert to an actual measured value. This action can be called "ride-through" and is highly desirable (Moore, 1996a & 1996b). The time limit should be configurable since the sources of information above give conflicting advice on how long this time should actually be. It will thus be an application-specific parameter. This time length will almost certainly be $\geq 20\text{ms}$, since the CBEMA curve suggests that local equipment is designed to ride through this length of brownout. The time length will probably be less than 0.5s, which is the longest tripping time for a 100% dip, specified by ER G59/1. IEEE 1574 is in the middle, with a figure of 160ms.

For dips which occur on only 1 or 2 phases, the requirement must be that the frequency measurement should continue to operate indefinitely with reasonable accuracy, as described in the section on unbalance (section 2.7.1)

Suitable requirements upon the frequency measurement algorithm for balanced (three-phase) dips and surges are thus:-

- maintain standard accuracy during 20% dips
- maintain reasonable accuracy during 60% dips up to 100ms (voltage at 40% of nominal)
- output a sensible value during 100% dips for 20ms using ride-through code (this time configurable within the algorithm so that it can be changed "in the field")

- recover to reasonable accuracy within 3-5 cycles after a dip, whenever voltage rises to 40% of nominal or above
- recover to standard accuracy within 3-5 cycles after a dip, whenever voltage rises to 80% of nominal or above

2.8 Loss of mains requirements

The requirements on frequency, amplitude and phase measurements for achieving adequate loss-of-mains detection are not immediately clear. Both G59 and IEEE 1547 are extremely vague on the acceptable algorithms and thresholds for such relaying, and the only definite information is that IEEE 1547 specifies a detection time limit of 2 seconds. Therefore, for the purposes of amplitude, frequency and phase measurement, a sensible approach is to make the measurements meet all the other requirements as well as possible, and then see how well the measurements can be applied to loss-of-mains detection. This topic is addressed in detail in chapter 6.

2.9 Measurement hardware and sample rate considerations

The measurement algorithms must be able to be made on hardware which is relatively cheap, small, and integrated with other measurement and control functions. This is because the target market for the algorithms is distributed generators and small microgrid power systems. As such, the emphasis is on many, cheap installations rather than few expensive ones. The cost of the measurement hardware and processor must be kept low so that it does not become a significant part of the system cost. Because of this, it is desirable to combine the measurement algorithms developed in this thesis with all the other local microgrid control algorithms into a single piece of code that operates on a single microcontroller at a fixed frame rate. This places limits on the frame rate since the overall process may contain much code. Other constraints on frame rate may be processing overheads such as data logging and communication with external devices. Experience at Strathclyde with microcontrollers shows that data logging in particular can be a severe constraint on frame rate, due to the access speeds of suitable memory areas. This is true even when logging decimation is high (i.e. logged data is only captured once every X frames), since the limit on frame rate is set by the longest potential frame time and not the average frame time.

Another constraint on the algorithms is that, in general, it will not be possible to synchronise the ADC sample points with zero crossings on the measured waveforms. Some specialised digital relays, and some power quality meters, use specialised sampling and CPU hardware which operates at variable frame rates (as described for example by Moore

(1996a)). The frame rate and sample timing can be determined by a PLL locked to the system frequency. This allows synchronisation of the zero crossings with sample times, and allows the number of samples per cycle to be kept constant. The hardware is specialised and costly, and also the PLL dynamics affect the dynamic performance of the system in a way which may not be appropriate in a microgrid with high rates of change of frequency as described in Table 2-1. Within the remit of this thesis, this approach is not available.

To make the algorithms function on more widely available (and cheaper) processing platforms, the ADC samples will therefore be taken at a fixed frame rate, synchronised to the fixed CPU frame rate. An achievable frame rate, based upon experience of integrated microgrid control algorithms at the University of Strathclyde, is 10 Sa/cycle or 500 Sa/s. This equates to a frame rate of 2ms, and allows relatively large microgrid control code algorithms to be executed successfully on realistic microcontroller systems, taking into account data logging and communication requirements.

The accuracy and quality of any measurements is affected by many mechanisms within the chain of hardware and software which forms the power system, instrumentation, and processing. In summary, these errors and mechanisms are:-

- Actual noise, spikes and harmonics present on the power system voltages and currents.
- The accuracy of voltage and current transducers (VTs, CTs, plus their burdens, or other measurement devices such as optical or Hall-effect sensors). Amplitude accuracy, phase accuracy/lag and linearity are all defined by the design of the transducers.
- Noise, interference and cross-talk in cables.
- Amplitude accuracy, phase accuracy/lag, linearity and noise in any instrumentation/isolation amplifiers and anti-aliasing filters.
- Amplitude accuracy, timing skews/jitter and bit noise of ADC measurements.
- Errors due to sample rate (interpolation), mathematical approximations, and aliased harmonics within the digital processing system (mathematical algorithms).

To estimate the signal/noise ratio of relatively cheap measurement hardware, measurements were taken of the voltage measurement instrumentation circuits at the University of Strathclyde. The instrumentation consists of three-phase 400V/110V star-star VTs, with each phase connected via lengthy, shielded, treble twisted-pair cables through an electrically noisy environment to a set of isolation amplifiers. These are based upon the

ISO124P isolator, with some additional components including an amplifier/filter stage with a basic 741 op-amp and a 3kHz low-pass filter which attenuates the 500kHz modulation used within the ISO124P. The Gaussian and 500kHz noise from these amplifiers after filtering is approximately 20mV RMS, with the 1pu (peak) signal amplitude set to $\pm 5V$. This equates to a noise level of approximately 0.005pu RMS, or a signal-to-noise ratio of 200 (46dB) which is relatively poor, and presents a sensible worst value to an expected hardware noise specification. It could almost certainly be improved using circuits designed commercially, and/or by lowering the cut-off frequency of the low-pass filter. A worst case noise level (for a voltage measurement) is therefore 0.5% of the nominal measured signal level. Note that for current measurements, the noise level may be significantly higher. This is due to:-

- The ADC range which may need to encompass much larger over-ranges than $\pm 2pu$ to be able to measure fault currents
- The current flowing in a system will often be at a level $\ll 1pu$, when loads or generation levels are at only a fraction of the branch capacity.

A conventional ADC resolution is 12 bits. A sensible signal scaling (for a voltage input) is that a 1pu peak-peak input signal voltage spans half the range of the ADCs, allowing for linear measurements up to $\pm 2pu$, but with higher signals clipped to the 2pu peak positive or negative values. In this work, ADC non-linearity effects are ignored, the justification being that the harmonic distortion content of the expected signals (possibly $\gg 8\%$ THD) is far larger than any reasonable ADC non-linearity specification. With many practical ADC setups, the lowest bits of the ADC can become unusable depending upon the hardware, software application, and the care with which it is set up. Therefore, a sensible precaution is to allow for an additional RMS quantisation noise of an RMS magnitude equal to 2x the LSB (least significant bit). This effectively scrambles the 2 least significant bits and means that only the top 10 bits are really usable.

It is contextually useful here to tabulate and compare the effective RMS noise levels from actual noise and from ADC quantisation noise. Here, the RMS noise due to a quantisation step of size a is given by $\sqrt{a^2/12}$ which is derived from the standard formula for the standard deviation of a uniform distribution. A further, easy to derive formula is that

$$\frac{x}{S} = N \cdot 2^b \cdot \sqrt{3} \quad (2.18)$$

where the ADC input is scaled over the range $-x$ to $+x$ pu, S is the actual per-unit input signal input, there are b usable ADC bits, and N is the noise equivalent per-unit RMS value

(relative to signal level S). Some possible scenarios are:-

RMS noise (pu)	Equivalent quantisation noise	Potential scenario
0.000282	1pu input, 12 bits over -2 to +2 range	Best possible from a 12-bit ADC
0.00113	1pu input, 10 usable bits over -2 to +2 range	Unusable (noisy) 2 LSBs
0.005	1pu input, 12 bits scaled over -35 to +35 pu range OR 0.28pu input from a CT, 12 bits scaled over -10 to +10 pu range for overcurrent measurement.	Measurement of 1pu current in setups with wide range inputs, OR, Measurement of small current flows.

Table 2-10 : Equivalent noise contributions of ADC quantisation effects

The effective RMS noise with a 12-bit ADC will therefore never be less than 0.000282pu. It may be as high as 0.005pu (-46dB) for measurements on poorly instrumented systems (Table 2-10). For current measurements, the RMS noise may be significantly higher on a per-unit basis, where low levels of current are measured and/or the ADC range is configured to measure wide ranges of over-current.

2.10 Overall amplitude and frequency measurement specifications (for voltage measurements)

The previous sections can be summarised into the requirement specifications for measurements of 3-phase voltage amplitude, phase and frequency. These requirements apply to measurements of these dynamic parameters within microgrid scenarios. In these scenarios, ROCOF rates are potentially high, power quality is potentially very poor, and response times must be appropriate for the required trip times and control dynamics. For relaying actions, accuracy must be appropriate to avoid spurious trips and missed trips. For control actions, measurements must contain very low levels of ripple to avoid passing this ripple back (potentially amplified due to droop controls) to prime mover or generator controls.

Description	Target
Absolute error	±0.02pu pk
Ripple and noise (ignoring DC biased in the absolute error)	±0.02pu pk
Response time (latency)	2 cycles
Measurable range	0.01 to 2pu

Table 2-11 : Voltage amplitude measurement specifications (relaying)

Description	Target
Absolute error	± 0.02 pu pk
Ripple and noise (ignoring DC biased in the absolute error)	± 0.001 pu pk (may not be achievable at the lowest sample rates with high THD levels)
Response time (latency)	5 cycles
Measurable range	0.01 to 2 pu

Table 2-12 : Voltage amplitude measurement specifications (control)

Description	Target
Absolute error	$\pm 0.1^\circ$ (probably only achievable with closed-loop calibration of the entire measurement system)
Ripple and noise (ignoring DC biased in the absolute error)	$\pm 0.1^\circ$
Response time (latency)	5 cycles
Measurable range	0.8 pu to 2 pu voltage magnitude

Table 2-13 : Phase measurement specifications (control/instrumentation)

Description	Target
Absolute error	± 0.025 Hz pk
Ripple and noise at steady state, 1 pu on all phases, at or near nominal frequency (ignoring DC bias in the absolute error)	± 0.025 Hz pk (± 0.0005 pu) for standard uses ± 0.005 Hz pk for ROCOF relays (may not be achievable at the lowest sample rates with high THD levels)
Response time (latency)	5 cycles (0.1 seconds)
Measurable range	40 \leq Freq \leq 70 with full accuracy. Also 30 \leq Freq \leq 80 with reduced accuracy of ± 0.25 Hz (to cope with underspeed/overspeed). Also 10 \leq Freq \leq 100 with further reduced accuracy of ± 0.5 Hz (to cope with underspeed/overspeed). Must not measure a sub-harmonic or harmonic. Must rail to the correct upper or lower limit if frequency is outside the measurable range.
Ride-through capability	For a configurable time, during 3-phase dips to less than 0.05 pu, a ride-through action must hold the last known "good" frequency measurement, until the configurable timer elapses or the dip finishes, whichever occurs first.

<p>Allowance for reduced accuracy during sustained low voltage events</p>	<p>Maintain standard accuracy during 20% dips</p> <p>Maintain slightly reduced accuracy during single or two-phase faults. Ideally to $\pm 0.010\text{Hz}$ for single-phase faults and $\pm 0.015\text{Hz}$ for two-phase faults.</p> <p>Maintain reasonable accuracy of $\pm 0.25\text{Hz}$ during three-phase dips up to 60% (voltage at 40%-80% of nominal)</p> <p>Maintain reasonable accuracy of $\pm 0.5\text{Hz}$ during three-phase dips up to 95% (voltage at 5%-40% of nominal)</p> <p>Allow an extra ripple/noise on the measurement equal to the steady-state specification, for each phase dropped below 5% of nominal voltage.</p> <p>Recover to standard accuracy within 5 cycles after a dip, whenever voltage rises to 80% of nominal or above.</p>
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Table 2-14 : Frequency measurement specifications

Description	Target
Sample rate	500 Sa/s (nominally 10 Sa/cycle) if possible
Maximum system ROCOF	10Hz/s
Unbalance	10% negative sequence, plus 2% zero sequence
Harmonic distortion tolerable while meeting steady state accuracy	Harmonics as described in Figure 2-3 and Figure 2-4, section 2.7.2. THD 53%
Inter-harmonic distortion	6.5% sinusoidal inter-harmonic at 2025Hz plus 23% square wave at 525Hz
Flicker	8% step flicker at 13.5Hz
Sudden phase jumps due to switching of loads	10 degrees, which would be experienced by removal of a 1pu power flow across a 17% pu reactance transformer/transmission line combination. NOTE: Frequency measurement output will transiently be in error subsequent to such a disturbance.
ADC quantisation noise	12-bit ADC scaled so that nominal input signal at 1pu spans half the ADC range, with clipping to the 2pu +ve and -ve peak signal levels. 12, with 2 bits additional RMS ADC sampling noise
Gaussian noise level (RMS) due to pre-ADC instrumentation and filtering	0.5% pu RMS (46dB SNR)

Table 2-15 : Range of interfering influence qualities and constraints

2.11 Generation of suitable test waveforms.

To simplify testing, four waveforms of length 60 seconds have been generated, against which candidate algorithms can be tested. The waveforms are designed to test the criteria of Table 2-11 to Table 2-14, under the interfering influences described in Table 2-15. The signal distortions of Table 2-15 are switched on and off so that the effects of all the influences upon a given algorithm performance can be analysed from a single simulation.

Waveform 1 contains some extremely dynamic ROCOF events up to ± 10 Hz/s, plus a 10° phase jump, and also tests the full frequency range from DC to 100Hz. It is the main test waveform for the frequency measurement algorithms (see section 5.7).

Waveform 2 tests frequency and amplitude measurements with a much lower level of ROCOF (0.2Hz/s) and over a more restricted range of 44 to 55 Hz. This waveform is useful for verifying that there are no particular problems at particular frequencies.

Waveforms 1B and 2B contain reduced levels of THD_v and instrumentation noise, and also have no flicker applied. These are used to verify the performance of the amplitude measurements in chapter 4.6. Waveform 1B is similar to Waveform 1, but with the following changes:-

- Flicker is not applied. This is because the flicker is (quite correctly) picked up by the amplitude measurement, making assessment of the steady-state accuracy difficult under conditions of large flicker step magnitudes.

THD_v is reduced from 53% to 28%, as per

- Table 2-6. The instrumentation noise is reduced from 0.005pu RMS to 0.001pu RMS (60dB SNR), and the additional ADC quantisation noise is reduced from 2 bits RMS to 1 bit RMS. As will be shown in chapter 3, section 4.7, meeting the ± 0.001 pu amplitude measurement ripple specification is only possible for signals with this level of THD (or less), and by achieving improved instrumentation noise levels. The amplitude measurements are still robust and stable under the conditions of 53% THD_v and 46dB SNR, but the accuracy/ripple at steady state is about ± 0.003 pu.

Waveform 2B is similar to Waveform 2 in the same way that Waveform 1B is similar to Waveform 1; with the same modifications to flicker, THD and instrumentation noise.

2.11.1 Waveform 1

Time	Description	Purpose / Test
0-1	NOTHING (Instrumentation/ADC noise only)	Simulate no connection to network
1-2	42 Hz, 1pu on all phases	Deliberate off-nominal frequency.
2-3	NOTHING (Instrumentation/ADC noise only)	Simulate disconnection from network
4-8	51.282 Hz (9.75 samples/cycle), with instrumentation/ADC noise	Test settling time to a new frequency
8-9	with unbalance added	Adds ripple to 3-phase measurements
9-9.5	with harmonics added	Disturbs all algorithms
9.5-10	with inter-harmonics added	Simulate mains signalling
10-10.5	with flicker added	Simulate worst case local flicker sources
10.5	phase jump 10 degrees	Simulate network switching
11	begin a +1 Hz/s ramp until 14 seconds	Dynamic frequency for following faults
11-11.04	3-phase dip 100%	Ride-through ability
11.5-11.75	3-phase dip 95%	Very low signal levels (low SNR)
12-12.25	3-phase dip 60%	Intermediate signal levels (low SNR)
13-13.5	drop phase A	Sustained single phase fault
13.5-14	drop phase B (and A)	Sustained two phase fault
14	stop +1 Hz/s ramp at 54.282	
15	dip 20% (all phases) and hold	Sustained marginal voltage level
16-30	ramp frequency down at -0.66 Hz/s to 45 Hz	Gradual frequency slide
30-31	ramp frequency up at 10Hz/s to 55Hz	Fast +ve ROCOF
31-32.5	45Hz	Sudden frequency step, check locking
32.5-37	ramp frequency down to 0 at -10 Hz/s	Fast -ve ROCOF, low frequencies
37-38	0Hz	
38-39	100Hz	Sudden frequency step, check locking
39-49	100 Hz down to 0Hz at -10Hz/s	Fast -ve ROCOF
49-50	0Hz	
50-60	0Hz to 100Hz at 10Hz/s	Fast +ve ROCOF

Table 2-16 : Waveform 1 to test measurement algorithms

2.11.2 Waveform 2

Time	Description	Purpose / Test
0-1	NOTHING (instrumentation/ADC noise only)	Simulate no connection to network
1-2	44 Hz, 1pu on all phases	Test settling time to a new frequency
2-3	with unbalance added	Adds ripple to 3-phase measurements
3-3.5	with harmonics added	Disturbs all algorithms
3.5-4	with inter-harmonics added	Simulate mains signalling
4-5	with flicker added	Simulate worst case local flicker sources
5-60	ramp frequency up at -0.2 Hz/s to 55 Hz	Test expected frequency range

Table 2-17 : Waveform 2 to test measurement algorithms

2.12 References for chapter 2

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3 Measurement of voltage or current amplitudes & phases

The details of the measurement of voltage or current amplitude/phase within 3-phase power systems are often overlooked. However, accurate measurements are a pre-requisite for any control or protection system. Making these measurements within digital systems requires stages of hardware filtering, sampling and software algorithms. The concepts, ideas, and algorithms employed for these basic algorithms have much in common to those for more complex techniques such as frequency measurement. For this reason, it is useful to examine the “simple” measurement of amplitude and phase of single-phase waveforms in detail, before trying to create an optimal frequency measurement. The shape of the waveforms and design of the measurement stages/algorithm all affect the uncertainty of the answers. In this chapter, algorithms are developed and then the resulting measurement errors are analysed under different conditions of influence qualities (poor power quality, measurement noise, sampling quantisation, low sample rates etc.).

As will be shown in this chapter, there are many different ways to optimise and embellish an algorithm for a seemingly simple measurement of amplitude. Several techniques can be applied in series or parallel, and the interaction of these techniques can be complex. The work in this chapter analyses several techniques and their interactions. An extremely useful product of this work is a suite of algorithms together with a selection matrix which explains the relative benefits and drawbacks of each algorithm versus the computational expense.

The single most useful algorithmic block which re-appears throughout this work is the averaging (or integration) of a quantity over an exact time period. For power system analysis, an obviously useful time period to average/integrate over is a multiple of cycles. This technique was introduced in the MATLAB SimPowerSystems blockset, which in turn is used by Jovicic (2003). This thesis improves upon the MATLAB algorithms for such averaging, both in terms of numerical accuracy and also computational speed, but more importantly introduces the new concept of cascading these averaging stages. It is shown that cascading extra averaging stages of multiples of half-cycles, after an initial single-cycle stage, can be used to almost completely eliminate the interpolation/integration errors due to low sample rate. In addition, the noise reduction properties of such cascaded stages are shown to be superior to other filter types of comparable latency. The cascaded exact-time averaging technique can also be used to build further useful signal processing stages which are developed during the course of this thesis: for example a novel DC blocking technique with zero latency (see section 3.4.4.2),

and an adaptive ripple removal filter (see section 4.3).

During the entire of this chapter, it is important to bear in mind that the amplitude/phase measurements themselves all rely on an estimate of the waveform frequency. In this chapter, the correct frequency is passed directly into the algorithms for most of the simulations. This is possible in a simulation environment where the waveforms are directly synthesised so the frequency is defined and known exactly. In sections 4.1 and 4.6, closed-loop simulations are carried out to determine the latency effects which result due to unavoidable lags in frequency measurement which occur, for example, when a “dead” part of a network is suddenly connected to a “live” network of initially unknown frequency and voltage magnitude/phase.

The path followed in this chapter is:-

- Examination of documented methods.
- Introduce the exact-time-period averaging algorithms in detail, including the substantial improvements made during this thesis, with comparisons to low-pass, Kalman slew-rate filtering techniques.
- Design/analyse the analogue front end and digital pre-processing, including a new DC blocking technique using the exact averaging block.
- Start with the SimPowerSystems “Discrete Fourier” block.
- Modify this for variable frequency operation and computational speed improvement, and incorporate the improved exact-time-period averaging algorithm. Examine the interpolation errors using pure sinusoid waveforms. Extend the averaging algorithm to use second-order interpolation and integration. This is shown to at least half the interpolation error in the absence of noise and harmonic contamination.
- Exploration of second harmonic cancellation techniques.
- Add post-Fourier averaging periods of exact multiples of half-cycles or cycles. This forms a cascade of filters which reject ripple at the fundamental or its harmonics. This novel application is shown to be more effective than second harmonic cancellation, for outputs which can afford a measurement time of $1\frac{1}{2}$ cycles (or more) within the digital environment.
- Explore the use of half-cycle initial Fourier correlations instead of full-cycle correlations, to allow lower quality responses with a $\frac{1}{2}$ cycle digital measurement time.
- Examine the relative dynamic and steady-state performances of the combinations

of techniques against:-

- Unaliased Harmonics
 - Noise and ADC quantisation
 - Frequency measurement error
- Creation a selection matrix which explains the relative benefits and drawbacks of each algorithm combination versus the approximate computational expense.
 - Analysis of the error magnitudes produced due to an inaccurate frequency estimate.

3.1 Documented methods relevant to chapters 3 & 4

There are relatively few publicly available written references on (specifically) the measurement of amplitude and phase in 3-phase AC power systems. Generally, algorithms used in industry are regarded as intellectual property and are not shared in the public domain. There are, however, a growing number of works which encompass the combined problems of frequency measurement and amplitude/phase measurement. Several such references used in chapters 3 & 4 are also relevant to chapter 5 (frequency measurement).

The specific problems addressed within this thesis, particularly low sample rates, very high harmonic content, instrumentation noise and ADC characteristics, do not appear to be addressed together by any known author, although some authors consider one or two of these problems in isolation.

In Johns (1995) the “classic” two-sample and three-sample techniques are described. These methods clearly break down when harmonic contamination such as described in section 2.7 is present. Also described in Johns (1995) are some methods for least-squares fitting of a fundamental component, some harmonic components and a decaying DC term to AC waveforms. In the final analysis, this boils down to a set of Fourier transformations plus a further analysis of a decaying DC term. Also in Johns (1995) are interesting differential-equation based algorithms where the differential equations are loaded with measured parameters of transmission lines. This is really an impedance measurement technique rather than an amplitude/phase measurement. The three-phase sampled measurements are processed to determine the RLC impedances, which are particularly relevant during faults. These techniques are primarily aimed at detecting faults in high-voltage transmission lines, potentially with sub-cycle measurement times. This is relevant in a transmission system where the protection is fast “unit” protection, the waveforms are generally clean sinusoids, and fault currents cannot be tolerated for many cycles before transmission lines sag or melt. Thus these techniques are interesting but not

particularly relevant to the problem addressed by this thesis, which is concerned with LV systems, graded protection systems with longer tripping times, and dirty waveforms of voltage and current.

Petrovic (2000) described using extremely slow (4 to 96Hz) but extremely high precision ADCs to make amplitude measurements. The assumption is that the power system is “inert” and therefore the measurement is made over many cycles. This is not the scenario presented in this thesis so the reference is not pursued further.

Aghazadeh (2005) presents a method for amplitude measurement based upon Kalman filters. (Also in this paper is a proposed zero-crossing based frequency measurement referred to in chapter 5). The method shows “unavoidable” transient deviation errors of up to 0.5pu when frequency changes, which is unacceptable.

Lin (2005) describes an interesting algorithm (for both amplitude and frequency measurement) based upon adaptations of wavelet transforms. The sample rate used is also suitable, at 600Sa/s, and this method might be worth more analysis in the future. No noise or ADC quantisation is applied, however, and the scales on the graphs do not allow a good analysis of the performance. His proposed method is compared to a Fourier analysis (which is the proposed base measurement used in this thesis), but this appears to have been coded very poorly (either accidentally or deliberately) to give bad results for comparison.

Some of the most relevant references found to date are actually the standard library blocks within the MATLAB SimPowerSystems blockset. These are described further in section 3.5 and form a useful starting point for the work of this thesis. Also, Jovcic (2003) presents a PLL design which includes a second harmonic cancellation scheme which has benefits in certain scenarios. This is discussed further in section 3.8.

Apart from the original SimPowerSystems blocks and the work taken from Jovcic, all the methods presented in chapters 3 & 4 are necessarily novel work carried out during the course of this thesis, due to the scarcity of relevant references found.

3.2 Averaging signals over exact time periods

This section explains how to average a signal over an exact time period within a digital system with a fixed frame rate. This technique proves to be useful in many ways, for example:-

- During Fourier correlations or RMS measurements of AC waveforms, the mathematical equation for the measurement requires definite integration (i.e. averaging) over exact periods which are multiples of cycles (or half cycles).
- Ripple can be present on measured signals. This ripple is often at the fundamental frequency f or its second (or higher) harmonic. Desired averaging times are often therefore, multiples of $1/f$ seconds, or multiples of $1/(2f)$ seconds if the lowest expected ripple frequency is at twice the fundamental. Later, in section 4.3, a novel ripple-removal filter is introduced which can use averaging times not necessarily equal to integer multiples of $1/(2f)$ to remove ripple at inter-harmonic or sub-harmonic frequencies.

The problem with exact-time averaging within a fixed-frame-rate system is that the desired time period to average over is normally not a convenient integral multiple of the frame time. Thus, interpolation techniques are required to address the “part-sample” problem. This is the reason that some specialised digital relays and power quality meters actually adjust their system clocks in such a way that an exact number of samples occur during one cycle, as described in section 2.9.

Within fixed-frame-rate systems, this technique is not available and an interpolation technique must instead be used. SimPowerSystems already has such a block which addresses this problem (with limitations), called “Discrete Variable Frequency Mean value”. The idea of this block is shown below:-

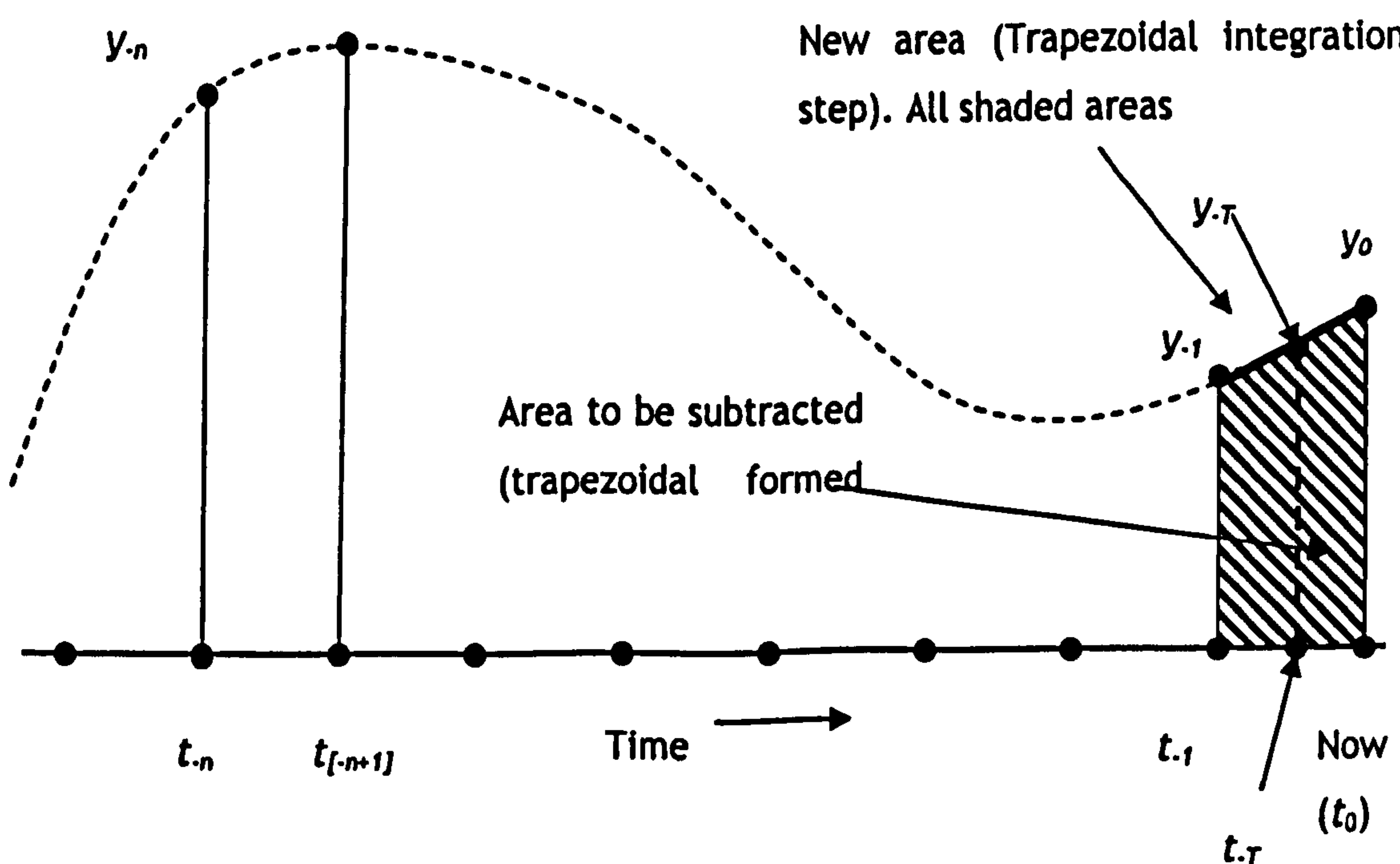


Figure 3-1 : SimPowerSystems “Discrete Variable Frequency Mean value”

The block works as follows:-

- Each new sample comes in as y_0 at time t_0 .
- A continuous trapezoidal integration process accumulates the integral formed by y_{-1} , y_0 , t_0 , and t_{-1} .
- The value of the integration is stored in a rolling buffer, big enough to store enough samples to cope with the longest required averaging time.
- The old value of the rolling integration at time t_{-n} is pulled from the buffer, and subtracted from the accumulated integration at t_0 . This reveals the definite integral from t_{-n} to t_0 .
- This is then corrected to give the definite integral from t_{-n} to t_T , where T is determined by the exact non-integer number of frame times which fit into the desired averaging time. The correction is applied by linearly interpolating between y_{-1} and y_0 , and using this to calculate the value of y_T , and thus the area of the trapezoid formed by y_T , y_0 , t_0 , and t_T can be calculated and subtracted from the integral from t_{-n} to t_0 .
- Thus, the final output is the definite integral from t_{-n} to t_T , which can be converted to an average by dividing by the desired averaging time $(t_T - t_{-n})$.

This algorithm, as implemented within SimPowerSystems, has a few shortfalls which can be significantly improved upon. These are described below:-

1. The output is "out of date" by between 0 and a full sample. The value depends upon the fraction of a full-cycle (T in the diagram above), which must be back-tracked to. This could be a disastrous effect if the averaging block is used inside a PLL which is being used, for example, as part of an inverter drive. It could introduce up to a full frame lag into the control system, severely affecting performance. Worse still, the lag is variable depending upon the resulting value of T , which means that any control system dynamics would be varying "at random" as T varied. The solution is to move the interpolation to the samples which are the oldest, so that the newest sample is used without interpolation. The measurement is thus always exactly coherent with the most recent sample, and thus also the processor clock.
2. To reduce interpolation errors, the linear interpolation and trapezoidal integration can be replaced using a 2nd-order polynomial fitting technique.
3. If a signal with any DC component is input, over time the integrator will eventually

lose precision and saturate. This is generally not a problem in the simulation environment where relatively few seconds elapse and the arithmetic is often 64-bit precision. In a real-time environment, run-times may be tens of thousands of hours, using 32-bit precision arithmetic (or less). Additionally, to average a result of phase, the risk of integrator wind-up is serious since the input phase must be un-wrapped before being averaged. To enable the algorithms to work in these cases a system of twin integrators is required with a “tick-tock” type “reset and use” system is required. This technique is described in detail below.

3.2.1 Improving the latency of the exact-time averaging

To address the first point, the algorithm can be modified in the following way:-

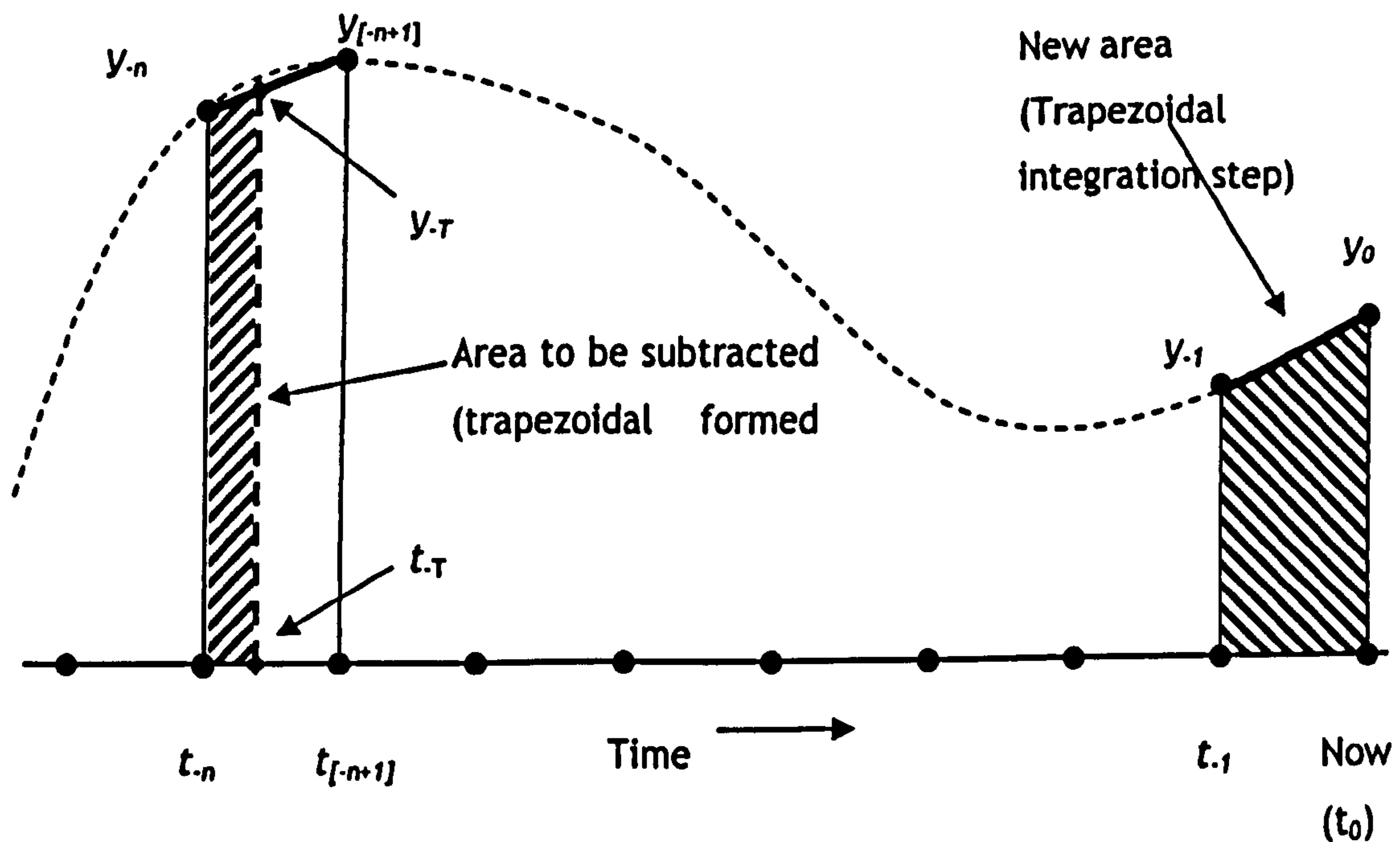


Figure 3-2 : Improved exact-time averaging technique

The interpolation and subtracted part-sample area can be moved from the most recent sample to the oldest, as shown in Figure 3-2. This means that the result is always coherent with the frame clock. The other calculations are basically identical. A slight complication is that now two buffers are required. The buffers are the same length. One buffer contains the rolling integral values as before. The second buffer contains the sampled values y_0 to y_n , and has a “two-tap” output so that the values y_n and $y_{[-n+1]}$ can both be retrieved for the calculation of the area to be subtracted via interpolation to y_{-T} . The “two-tap” buffering algorithm can be implemented in Simulink by the following piece of code:-

Variable discrete delay with two taps

Andrew Roscoe, July 2005

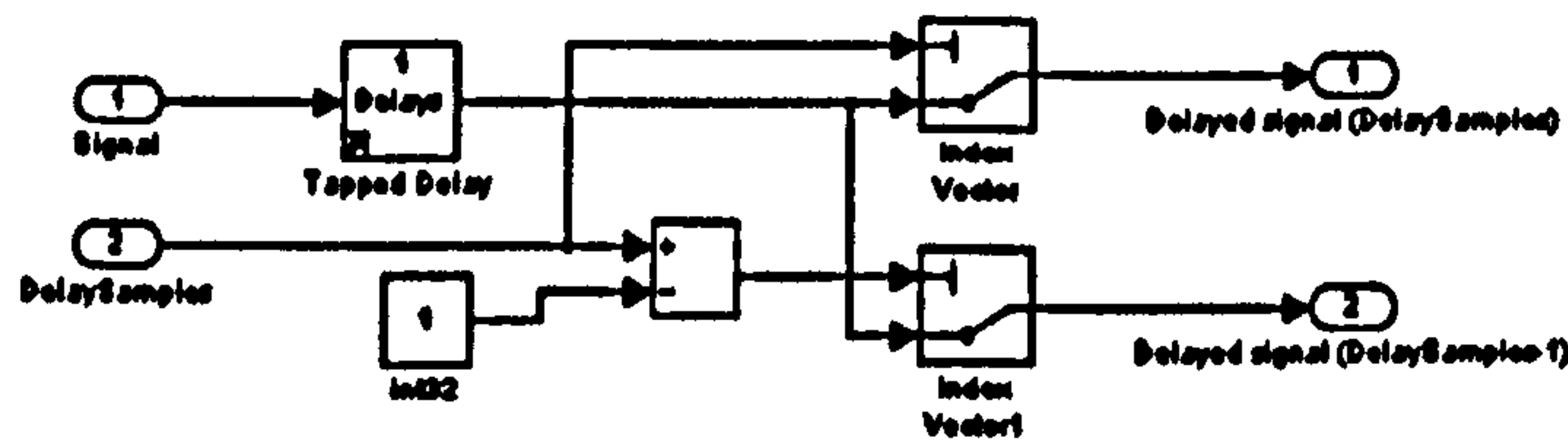


Figure 3-3 : Buffer (2 taps) for linear interpolation

However, when compiled into C code for execution on target hardware platforms (e.g. the Infineon TC1796 microcontroller) using the MATLAB Real-Time-Workshop module, this block results in a "MEMCOPY" assembler instruction which can be very costly in terms of CPU time, with execution time increasing with increasing buffer size. To address this, MATLAB SimPowerSystems contains an S-Function version of a "single-tap" buffer block called "Discrete Variable Transport Delay". This executes orders of magnitude faster, and the execution time is independent of the buffer size. During this thesis, new delay/buffer S-Functions were produced. These use a fixed memory space and moving pointers both to add and to tap off the input and output data. Optimised codings for the simple "one-tap" buffer, the "two-tap" buffer and also the "three-taps" buffer (required for 2nd order interpolation presented below) have all been generated. The delay buffer S-functions produced during this thesis execute up to 3 times faster than the equivalent MATLAB SimPowerSystems S-function buffer block "Discrete Variable Transport Delay". For details on the benchmarking of these S-Functions and example S-Function code ("c" and "tlc" files), the reader is directed to Appendix G.

The overall algorithms (Simulink code plus S function calls) for the 2nd order averaging blocks are presented in the next section. The 1st-order algorithms are very similar but simpler.

3.2.2 Extension to 2nd order interpolation

The entire algorithm can be extended to use a 2nd order quadratic technique to minimise the interpolation errors. The idea is simply to use 3 points to fit a quadratic and thus to obtain a more accurate measure of the area/average.

arrangement of twin integrators in a tick-tock arrangement has been implemented. To explain this, it is easiest to present the actual Simulink coding. The 2nd order block is used as an example.

Variable exact time period info, for averaging and delta calculations using 2nd order interpolation for the part-sample periods

Andrew Roscoe, 2007

$$\text{MaxDelaySamples} = \text{ceil}(\text{dMax}/\text{Tps}) + 1;$$

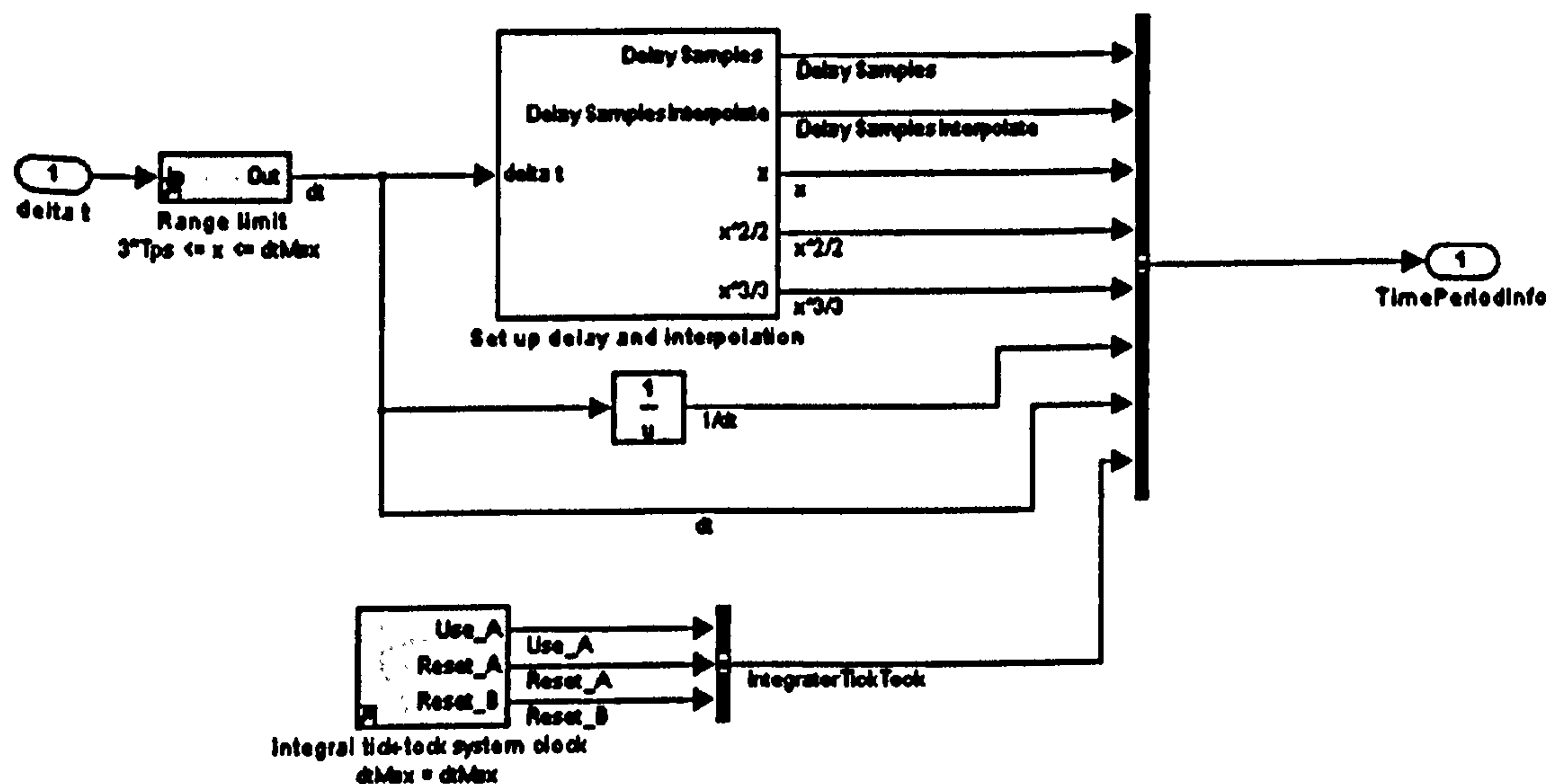


Figure 3-5 : Re-usable pre-calculations for 2nd order averaging

Figure 3-5 shows the re-usable pre-calculation signals for the buffering, curve fitting and interpolations, plus timing signals for the tick-tock integrator. The input to the algorithm is the time over which the averaging is required. This block is re-usable in that the *TimePeriodInfo* output can be passed to many blocks which need to average different signals but over the same time period. The detail inside the "Set up delay" block is shown below in Figure 3-6.

The outputs from this block are:-

- the number of integer samples to delay inside the integration buffer, *DelaySample*)
- the number of integer samples to delay inside the sample (y) buffer, *DelaySamplesInterpolate*
- The precalculated values of x , $x^2/2$, and $x^3/3$

Calculate the value x required for 2nd order interpolation

x is the time after the middle sample (y2) of the three used for curve fitting.
 The sample y2 is assigned time=0
 The sample y1 is assigned time=-1
 The sample y3 is assigned time=1

Andrew Roscoe, 2007

NOTE. The DelaySamples for the interpolation goes back one further.
 This is so that the interpolation for the extra area removal works with the same three samples that the area addition inside the original integration worked with.

Therefore
 $x = \text{DelaySamples} \cdot \text{Idealsamples}$
 where Idealsamples is the number of non-integer samples in the past which we require to interpolate to
 and DelaySamples+1 is the actual (integer) number of samples which are held in the buffer.

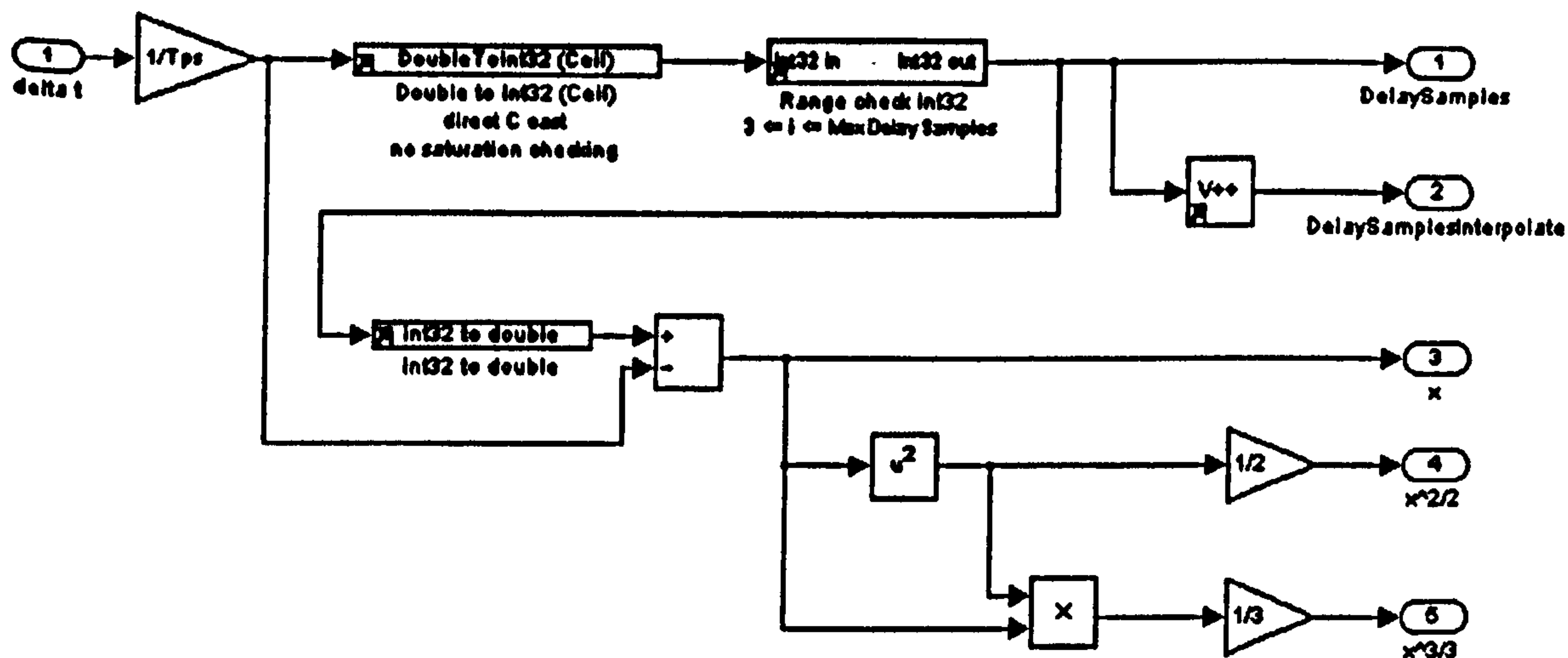


Figure 3-6 : Re-usable pre-calculations for 2nd order averaging, detail

Note that to simplify the arithmetic, the quadratic curve fitting and interpolation is normalised to operate as if the three points were at [-1, y1], [0, y2] and [1, y3]; i.e. with a frame time of 1 second. Thus x, as output from this block, is the time value at which the interpolation is required, and is in the range $0 < x < 1$. The final answer is corrected (de-normalised) by multiplying by the actual frame time at the very end.

Clock for Tick-tock definite integral implementation

Andrew Roscoe, 2007

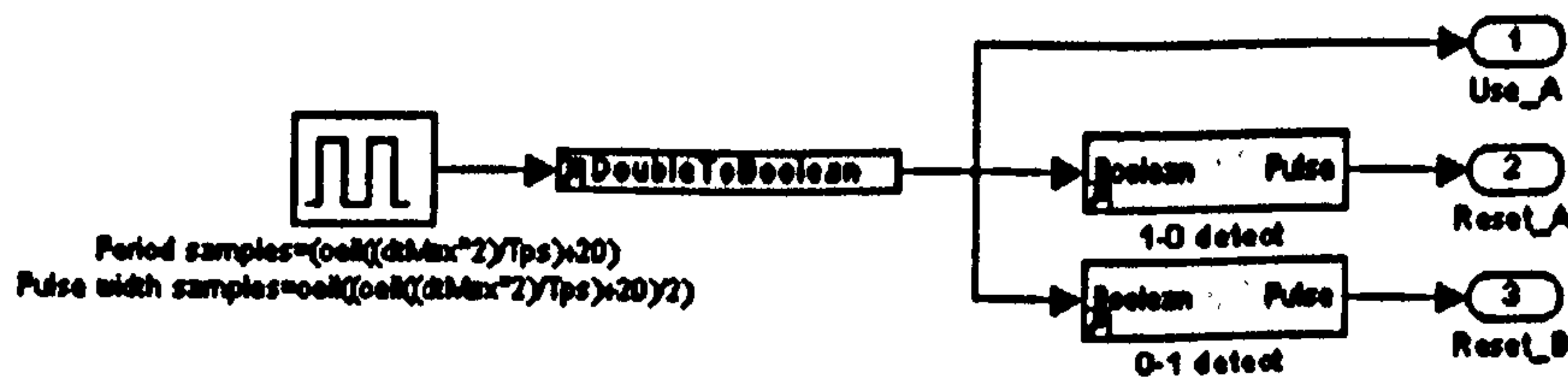


Figure 3-7 : Re-usable pre-calculations for 2nd order averaging, tick-tock timing

Figure 3-7 shows the final part of the pre-calculation. The primary output is a Boolean output which signifies whether to use path A (or path B) of the twin integrators (see Figure 3-8). Also, there are two reset signals which reset the integrators when they become

inactive. The signal timing is such that before each integrator output is used, it must be fully loaded and settled with valid signal values after being reset. The fastest tick-tock clock can therefore be $dtMax^2$ where $dtMax$ is the longest allowed averaging time (and hence also sets the required buffer size). In practice, a slightly slower clock is used to guarantee clean handovers between the pair of integrators.

The remainder of the 2nd order averaging algorithm is now described. The inputs to the block are the signal to be averaged, and the *TimePeriodInfo* data from Figure 3-5.

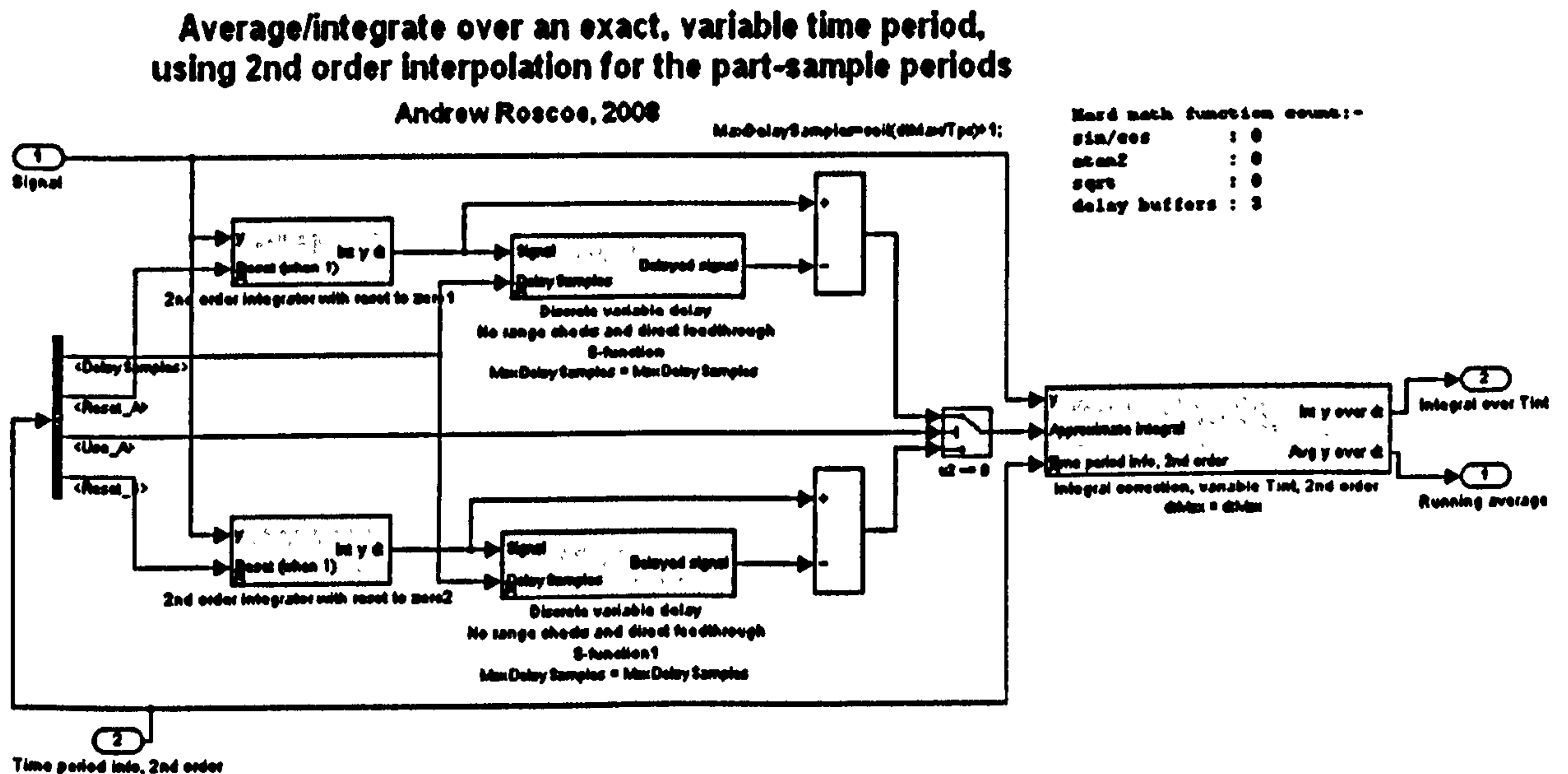


Figure 3-8 : 2nd order exact-time averaging block, tick-tock system

The integration has two paths, A and B. Each is used for a certain time, then reset, then preloaded with valid signal data, then used, etc. The two paths together produce a seamless output with no risk of integrator wind-up.

2nd order integrator with reset

Integrates the signal (timedep Tps)

Andrew Roscoe, 2007

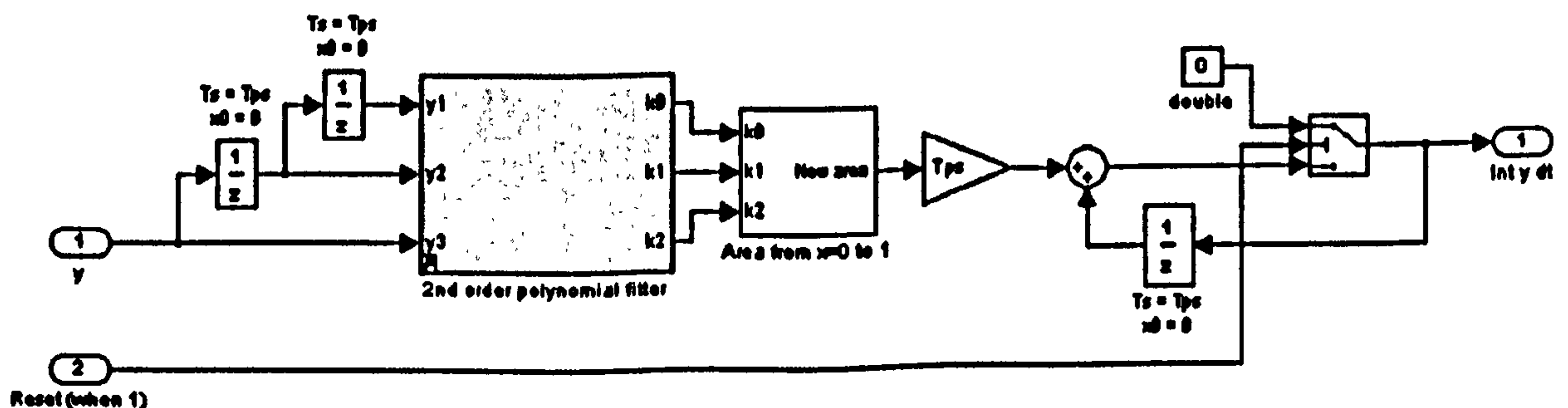


Figure 3-9 : 2nd order exact-time averaging block, 2nd order integrator

The integrator accumulates the integral of the signal by curve fitting and evaluation of the integral of this curve. For computational simplicity, the three most recent sampled points are here considered to lie at $[-1, y_{-1}]$, $[0, y_0]$ and $[1, y_1]$. The correction for this normalisation is carried out later in Figure 3-9 by the multiplication by Tps (the frame time).

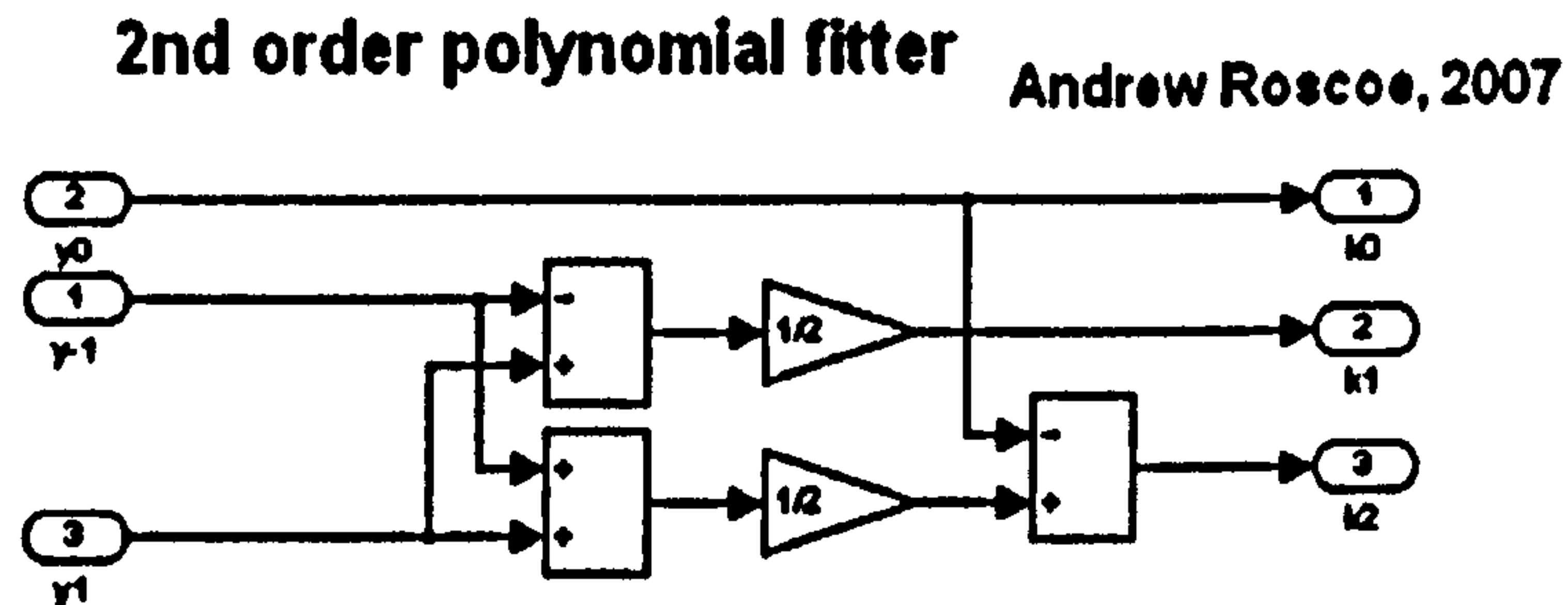


Figure 3-10 : 2nd order exact-time averaging block, quadratic curve fitting

The quadratic curve fitting requires only simple arithmetic, as shown in Figure 3-10, which evaluates:

$$k0 = y_0$$

$$k1 = \frac{y_1 - y_{-1}}{2}$$

$$k2 = \frac{y_1 + y_{-1}}{2} - y_0$$

Where $k0$, $k1$ & $k2$ allow $y(t)$ to be estimated within the region $-1 < t < 1$, by using

$$y = k0 + k1 \cdot t + k2 \cdot t^2$$

(3.1)

2nd order integrator from $x=0$ to 1, given $k0, k1, k2$

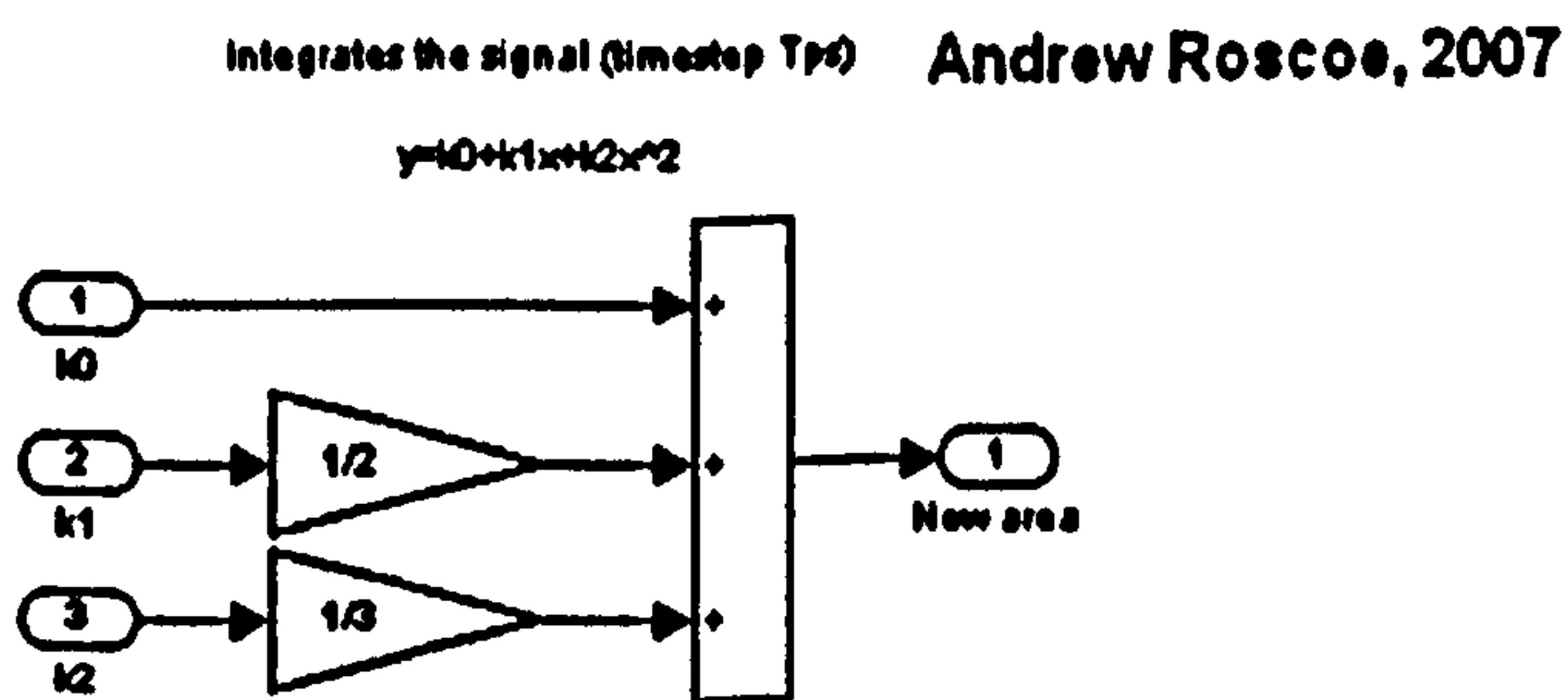


Figure 3-11 : 2nd order exact-time averaging block, quadratic curve integration

The new area to be integrated, between $t=0$ and $t=1$ (see Figure 3-4) can be calculated from $k0$, $k1$, $k2$ with only 2 multiplications and 2 additions, as shown in Figure 3-11. This numerically evaluates the integral of equation (3.1).

$$\int_0^1 (k_0 + k_1 \cdot t + k_2 \cdot t^2) \cdot dt = \left[k_0 \cdot t + \frac{k_1 \cdot t^2}{2} + \frac{k_2 \cdot t^3}{3} \right]_0^1 = k_0 + \frac{k_1}{2} + \frac{k_2}{3}$$

The output of the blocks described in Figure 3-9 to Figure 3-11 is a running integration. There are two sets of these blocks forming the tick-tock system, plus a buffer in each path which allows the definite integral to be calculated (see Figure 3-8). The final piece of the algorithm is the correction for part-sample effects, by the "Integral correction" block, which requires a final (3rd) delay buffer.

Correct integration/averaging an exact time period, using 2nd order interpolation for the part-sample periods Andrew Roscoe, 2008

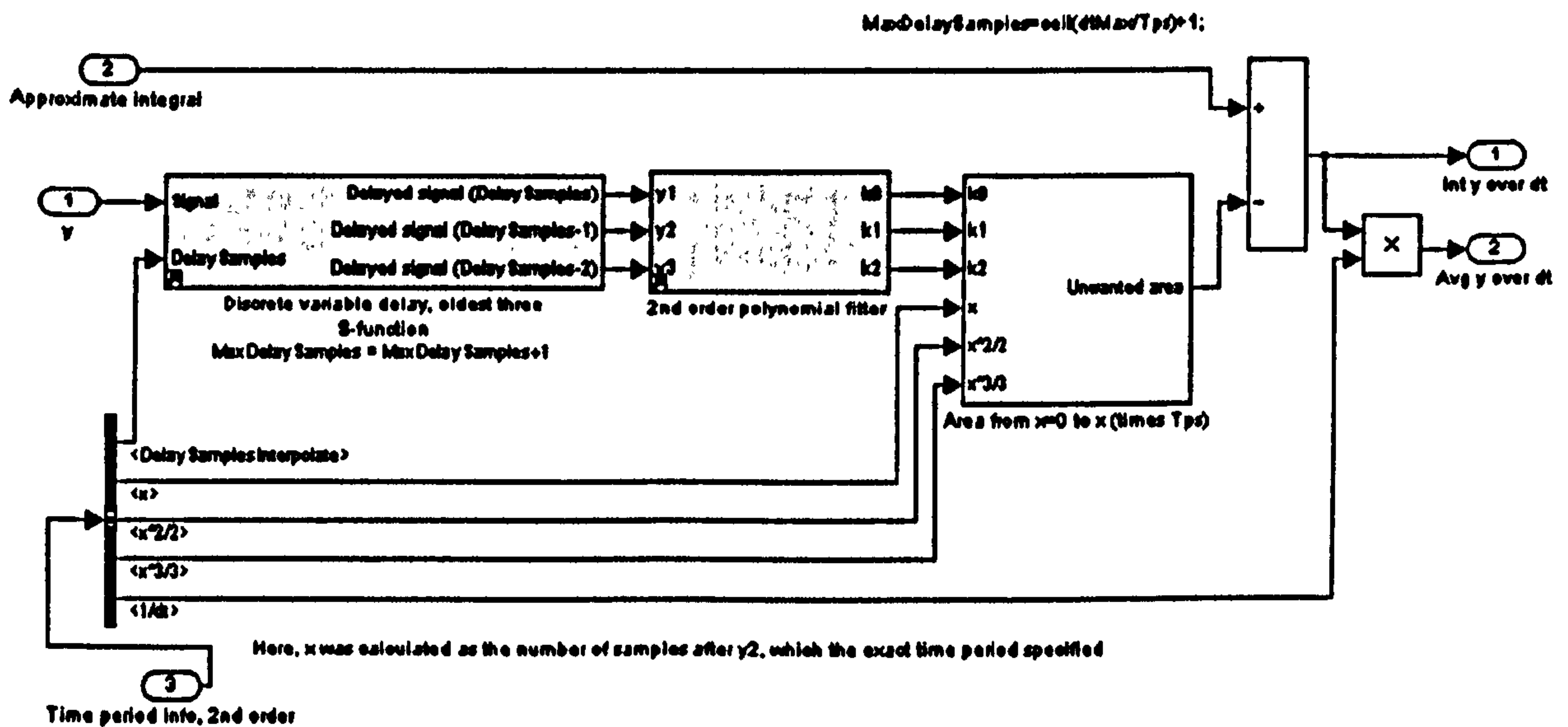


Figure 3-12 : 2nd order exact-time averaging block, definite integral calculation

Figure 3-12 shows the code used to carry out the process described in Figure 3-4. The final piece to be described is the detailed calculated of the area to be removed for correction of the part-sample period not required (Figure 3-13). It can be seen that this integration only requires simple calculations, by re-using the pre-calculated values of x, x²/2, and x³/3.

2nd order integrator from x=0 to x, given k0, k1, k2

Integrates the signal (Times Tps) Andrew Roscoe, 2007

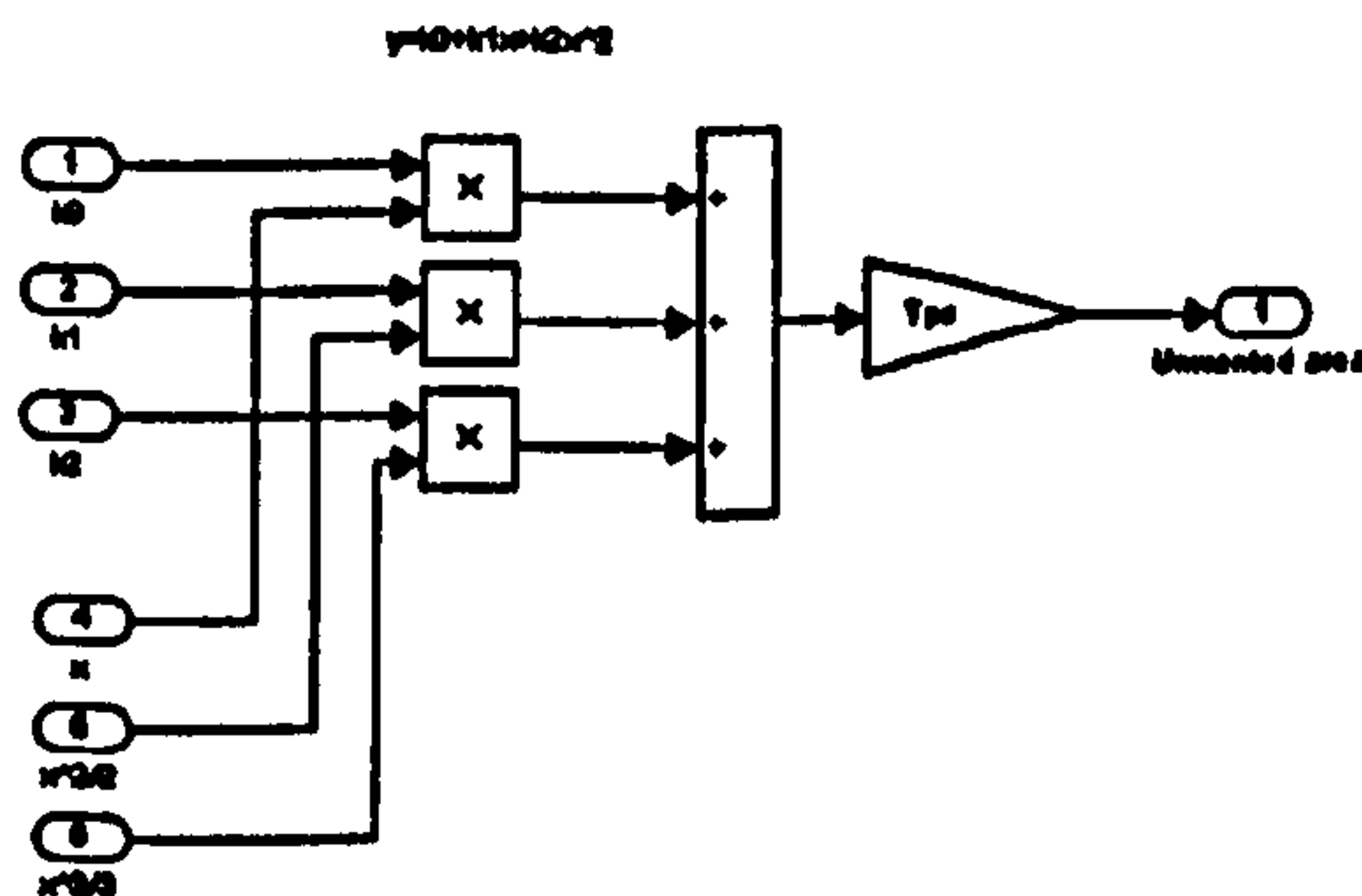


Figure 3-13 : 2nd order exact-time averaging block, definite integral correction area

The final results are the integral (and average) of the signal value over the exact time period desired. The linear interpolation coding is similar but slightly more straightforward due to the use of linear interpolation instead of quadratic curve fitting. With linear interpolation, the calculations are simpler, and also more of them can be pre-calculated and shared amongst many blocks using the same averaging period.

3.2.4 Averaging of phase

Averaging of variables which contain phase information requires special care. The input phase to the averaging algorithm is generally (but not necessarily) in the range $-\pi < \varphi < \pi$. Great care must be taken so that the phase wrapping effect at the $\pm\pi$ boundary does not corrupt the averaged result. The averaged result should also always be in the range of $-\pi < \varphi < \pi$. Extending the algorithm from that of Figure 3-8 to cope with phase, results in the algorithm of Figure 3-14 and Figure 3-15. The input phase must be "un-wrapped" before integrating, and re-wrapped before being output. Loss-of-precision errors are avoided by the tick-tock system which not only resets the integrators but also resets the un-wrapping code which otherwise can easily saturate when executed in real-time for many seconds/hours.

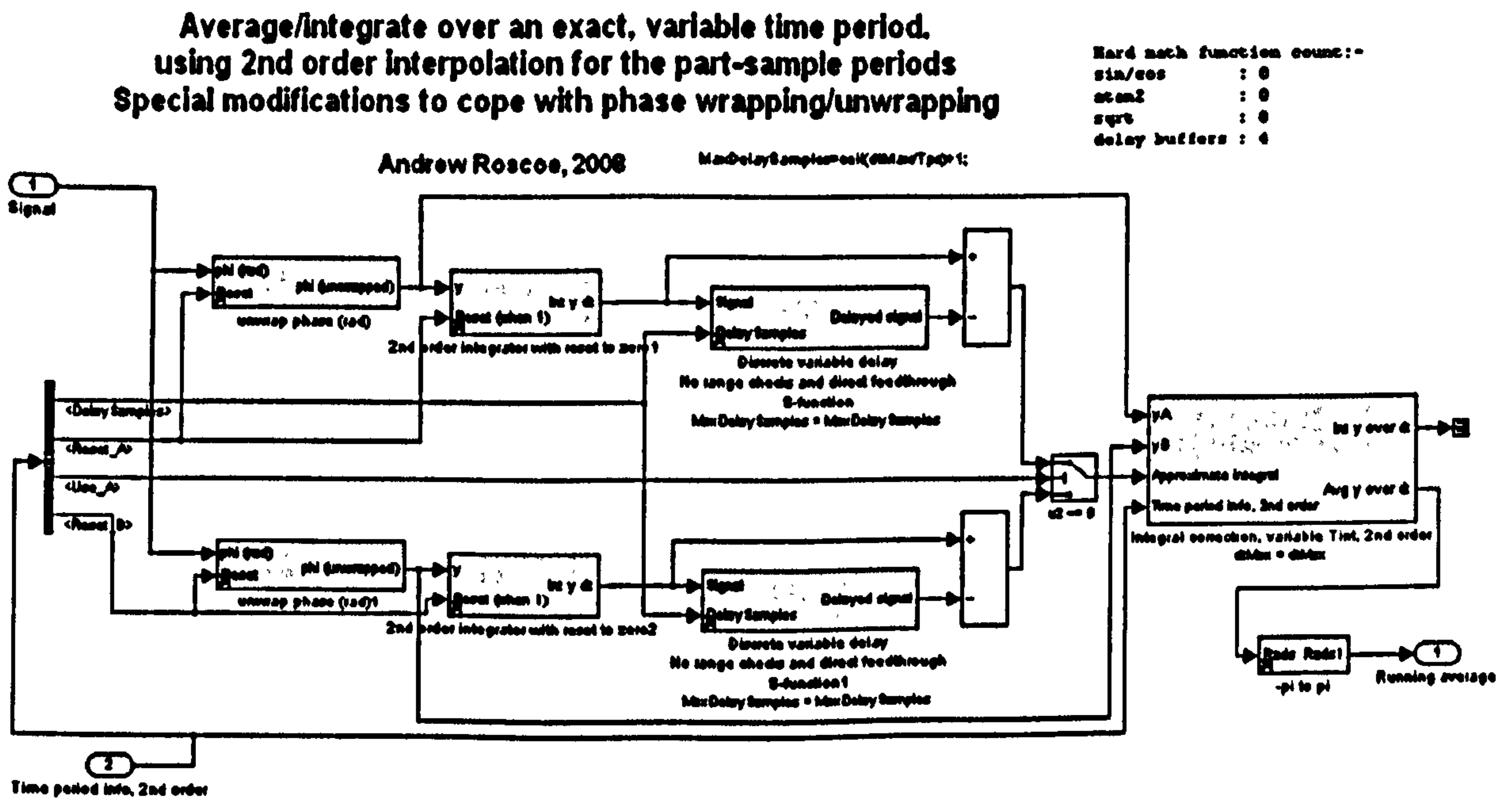


Figure 3-14 : 2nd-order exact-time averaging extended to variables measuring phase (a)

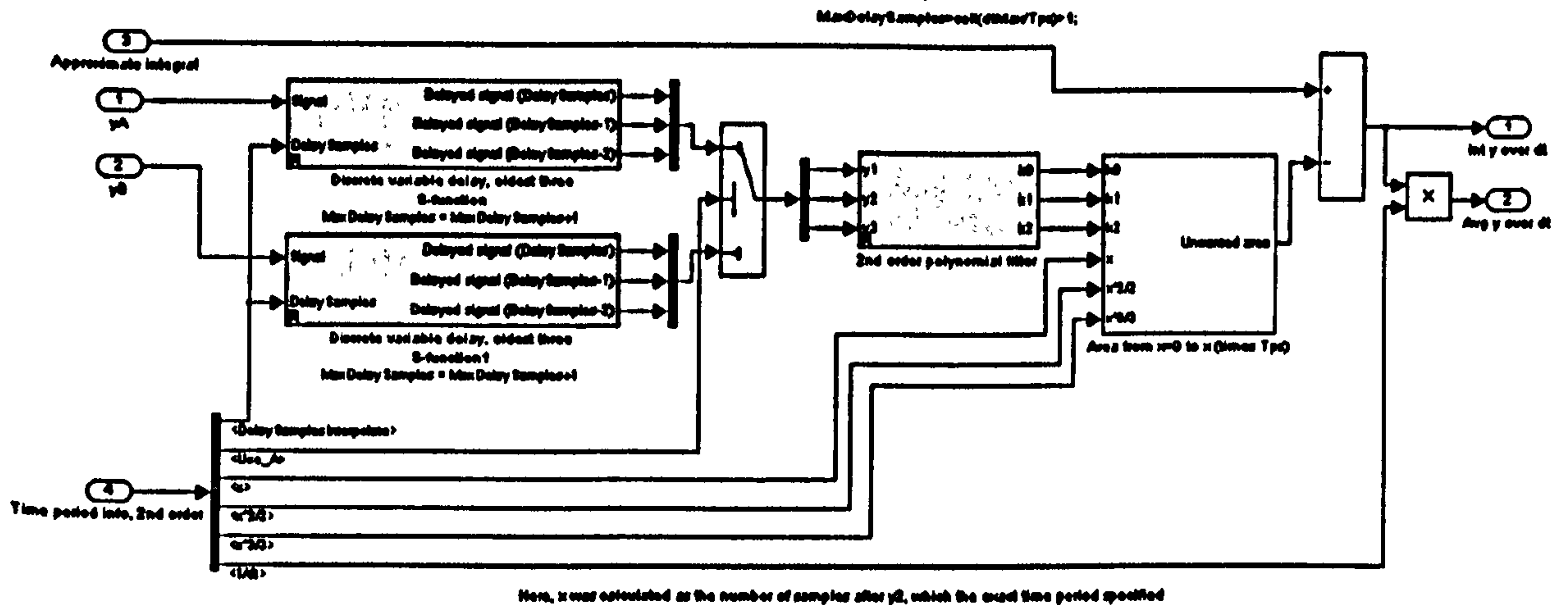


Figure 3-15 : 2nd-order exact-time averaging extended to variables measuring phase (b)

3.3 Comparison of exact time period averaging techniques with low-pass/Kalman filters and slew rate filters

Ever-present problems in measurements of AC power system parameters are:-

- Noise
- Ripples due to sampling, harmonic, and aliasing effects

To cope with these effects, several filtering techniques are considered during this thesis

- Low-pass filtering
- Kalman filtering
- Slew-rate limiting
- Exact-time averaging

Some references including Dash (2000) advocate the use of Kalman filtering. This was briefly investigated. At the core of the Kalman filter, however, is an algorithm which is a tunable low-pass filter (Welch, 2001), which can be adapted to different noise conditions. Low-pass filters have been investigated thoroughly, and this thesis proposes that the use of exact-time averaging techniques is more suitable within the power systems domain than the low-pass filter. Low-pass filters and Kalman filters can be simpler to implement in real-time, being IIR filters which require only a single state to be stored in memory. The averaging techniques described in section 3.2 are FIR filters which require buffering of data streams in memory. It is proposed that these buffers are nowadays relatively easy to implement on even the smallest modern microcontrollers, where many kB of RAM is available with acceptable access speeds. Traditionally, this has been a limitation on historic computer systems with limited RAM memory.

To illustrate the relative performance of low-pass, exact-time-averaging, and slew-rate filters, a simple Simulink model has been created. This allows the following four scenarios to be presented to filters:-

- A step function from 0 to 1 at $t=1$ second
- An impulse of value 1 at time $t=1$ second
- Gaussian noise, RMS value 1
- A ripple (sine wave) at a worst frequency for the exact-time averaging algorithms, which results in the biggest interpolation errors. These worst frequencies are such that the desired averaging time equates to $n+\frac{1}{2}$ sample periods where n is any integer.

The frame rate is set at 500 Sa/s (nominally 10 samples/cycle for a 50Hz input waveform). A worst input frequency for ripple in this case is one where only 9.5 samples occur during a cycle, i.e. 52.632Hz. A worst time period for averaging is therefore a multiple of 1/52.632 second.

The first analysis is to compare the 1st-order exact-time period averaging block with the original SimPowerSystems “Discrete Variable Frequency Mean value” block. In the case shown below, the step function is presented to the two blocks, which both have averaging times set to 1/52.632 seconds (9.5 samples). It can be seen in Figure 3-16 that the SimPowerSystems block outputs have additional $\frac{1}{2}$ cycle latency relative to the new 1st order averaging block.

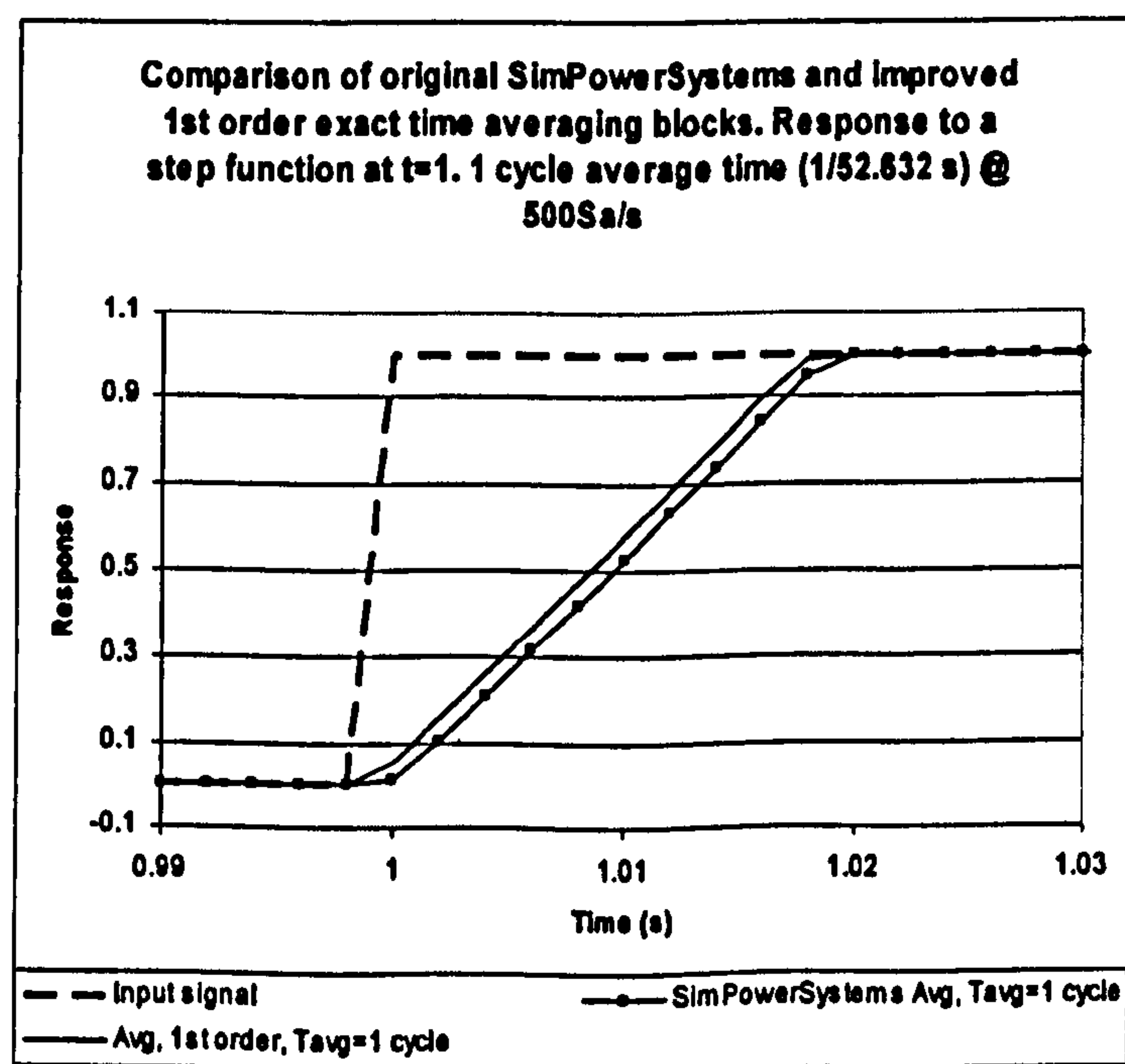


Figure 3-16 : Improved latency of the exact-time integration block over the SimPowerSystems block

Next, a wider range of filters are further compared for performance. The desired time to obtain a settled result after a transient (step function), is set at 5 cycles ($5/52.632=0.095$ seconds):-

- Low-pass filter, with a "5RC" time of 0.095 seconds, hence $F_c=8.38\text{Hz}$ by {B.5}
- Exact-time period average block, 1st order, set to 0.095s
- Exact-time period average block, 2nd order, set to 0.095s
- Slew-rate limiter, with rate limited to $1/0.095\text{s} = 10.526/\text{s}$
- Cascaded pair of 1st order exact-time period average blocks, set to 2.5 cycles and 2.5 cycles averaging time periods (0.0475s each)
- Cascaded pair of 1st order exact-time period average blocks, set to 1 cycle and 4 cycle averaging time periods
- Cascaded trio of 1st order exact-time period average blocks, set to 1 cycle, 0.5 cycle and 3.5 cycle averaging time periods

3.3.1 Step response of filters

The first comparison is the response to the step function at $t=1$ second. Analysis of Figure 3-17 and Figure 3-18 shows that all of the exact-time average filters, and the slew-rate filter, are fully settled by the required time ($t=1$ second + 0.095 seconds), or a sample or two after it. This would be expected for the FIR filters. The low-pass filter, however, despite its faster initial rise-time, is only 99.3% ($100*(1-e^{-5})$) settled at this time.

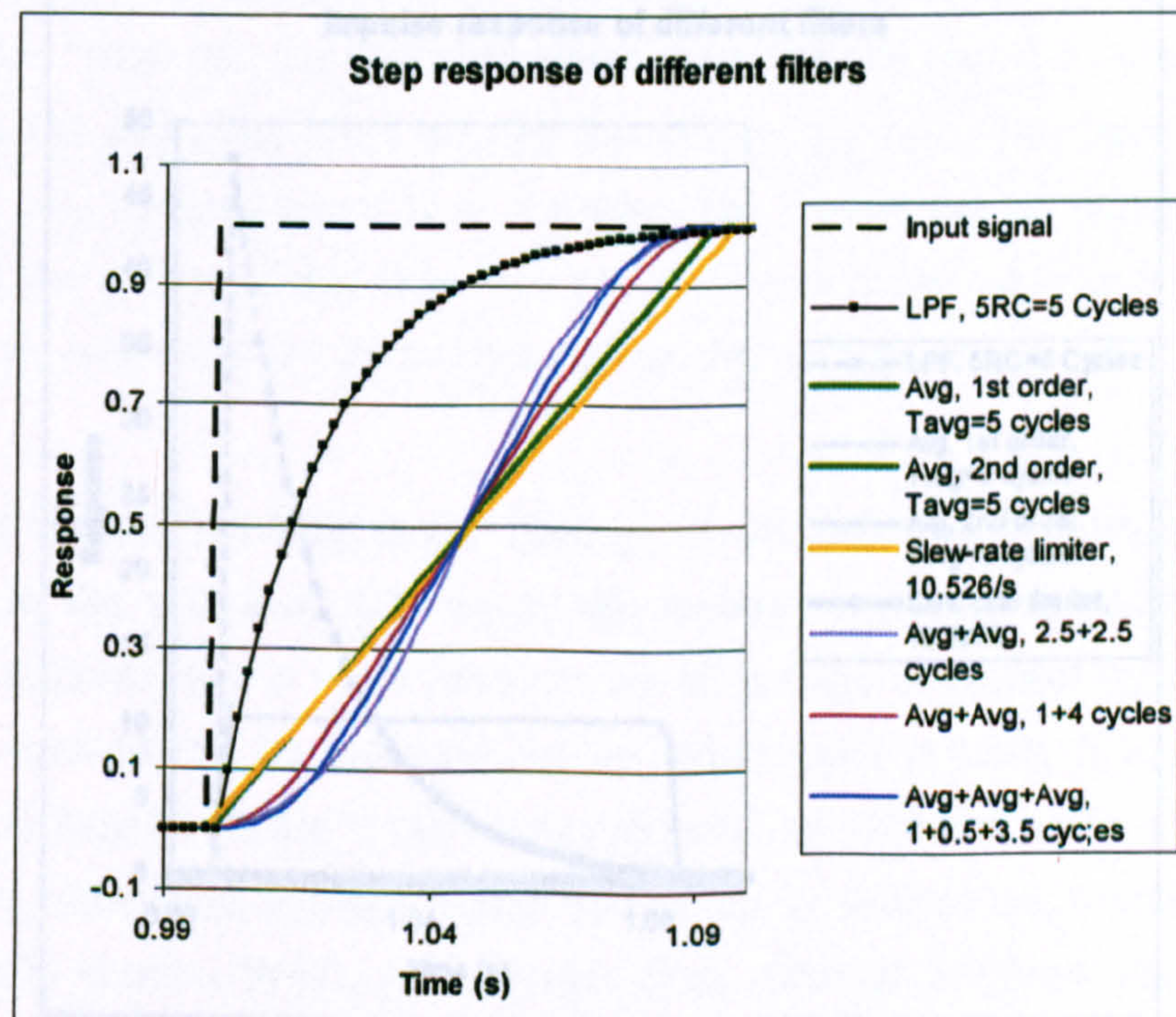


Figure 3-17 : Step response of different filters

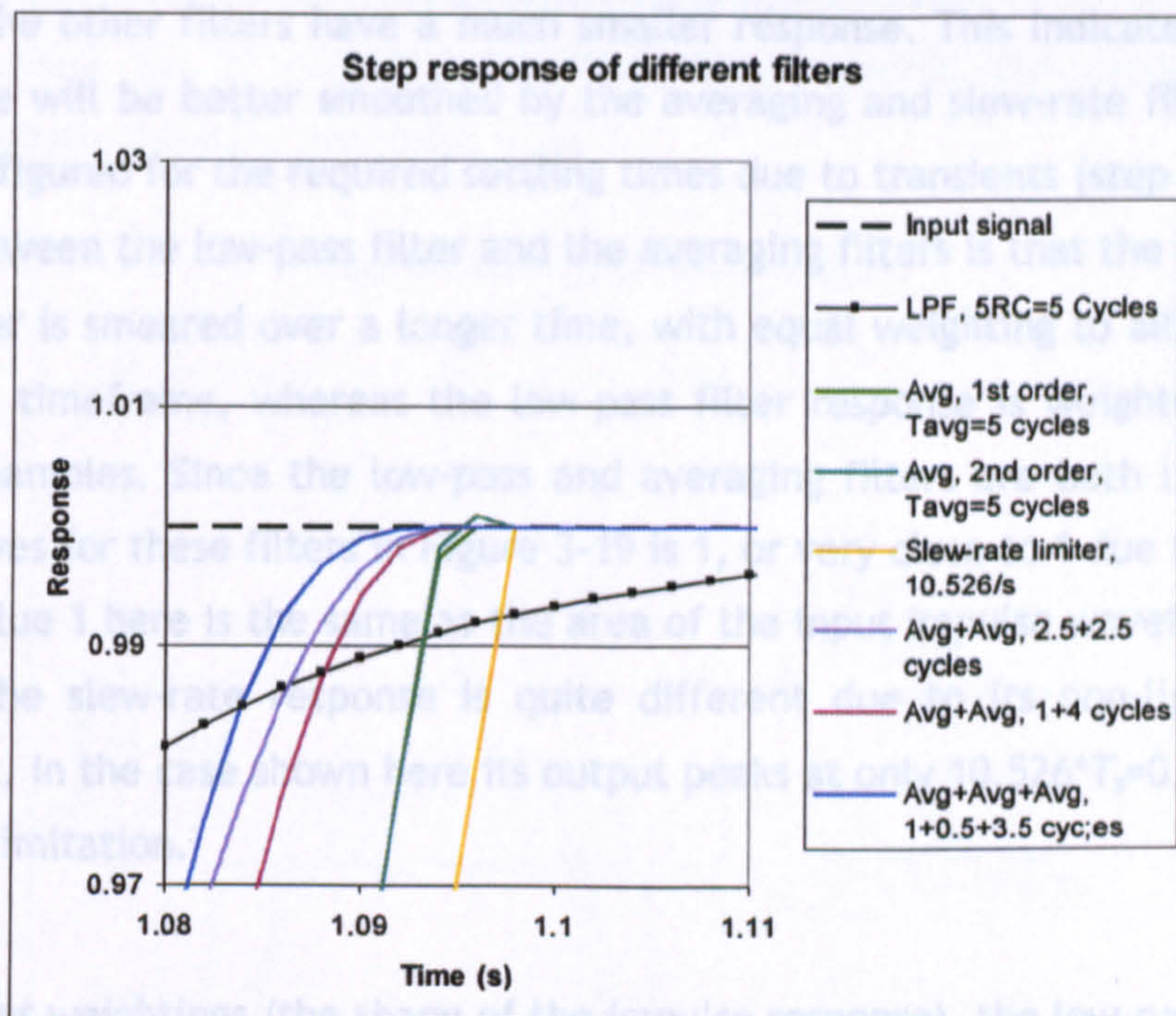


Figure 3-18 : Step response of different filters, zoomed in

3.3.2 Impulse response of filters

The next analysis of the filters is the response to an impulse function at $t=1$ second, which is made up of a single sample of amplitude $1/T_s=500$, where T_s is the sample time (frame time) of $1/500$ s.

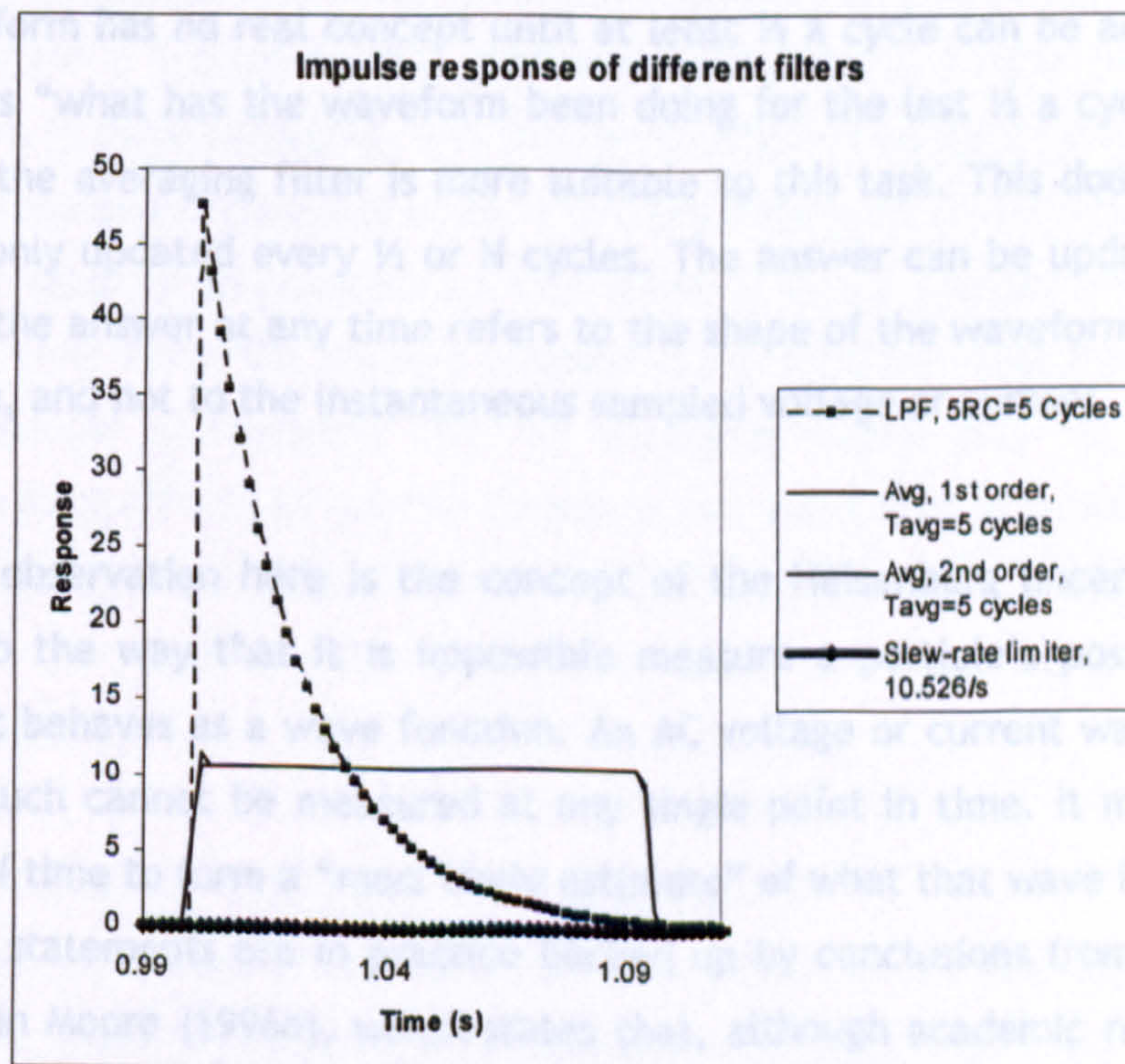


Figure 3-19 : Impulse response of different filters

Figure 3-19 clearly shows that the low-pass filter has the largest peak impulse response. By comparison, the other filters have a much smaller response. This indicates that sampled spikes of noise will be better smoothed by the averaging and slew-rate filters, when the filters are configured for the required settling times due to transients (step functions). The difference between the low-pass filter and the averaging filters is that the response of the averaging filter is smeared over a longer time, with equal weighting to all the samples in this averaging timeframe, whereas the low-pass filter response is weighted towards the more recent samples. Since the low-pass and averaging filters are both linear, the area under the curves for these filters in Figure 3-19 is 1, or very close to 1 due to interpolation errors. The value 1 here is the same as the area of the input impulse waveform of $1/T_s$ for T_s seconds. The slew-rate response is quite different due to its non-linearity via the clipping effect. In the case shown here its output peaks at only $10.526 \cdot T_s = 0.021052$, due to the slew rate limitation.

Due to the filter weightings (the shape of the impulse response), the low-pass filter gives a higher weighting to more recent inputs than to older inputs. The averaging filter weighting is constant for the defined averaging period. A low-pass filter (or Kalman filter) is thus the correct approach when the desired output is “what is the system doing right now?”. The averaging filter, however, is more appropriate to use when the desired output is “what has the system been doing for the last x seconds?”. The Kalman filter, being an extension of a low-pass filter, is thus ideal for tasks such as spacecraft position estimation, which was the first implementation of such a filter. However, within AC power systems the measurement of an AC waveform has no real concept until at least $\frac{1}{2}$ a cycle can be accumulated. The question is thus “what has the waveform been doing for the last $\frac{1}{2}$ a cycle or N cycles”, and therefore the averaging filter is more suitable to this task. This does not mean that the answer is only updated every $\frac{1}{2}$ or N cycles. The answer can be updated many times per cycle, but the answer at any time refers to the shape of the waveform over a previous amount of time, and not to the instantaneous sampled voltage or current.

An interesting observation here is the concept of the Heisenberg uncertainty principle, which refers to the way that it is impossible to measure a particle's position or velocity exactly when it behaves as a wave function. An AC voltage or current waveform is also a wave, and as such cannot be measured at any single point in time. It must be analysed over a period of time to form a “most likely estimate” of what that wave is actually doing. Such academic statements are in practice backed up by conclusions from field testing of relays such as in Moore (1996a), which states that, although academic researchers often strive for the fastest-responding measurement, brief sub-cycle transients and events must not lead to spurious tripping.

3.3.2.1 Impulse response of cascaded averaging filters

A further relevant set of results is obtained by comparing the (convolved) impulse response of various cascaded averaging filters.

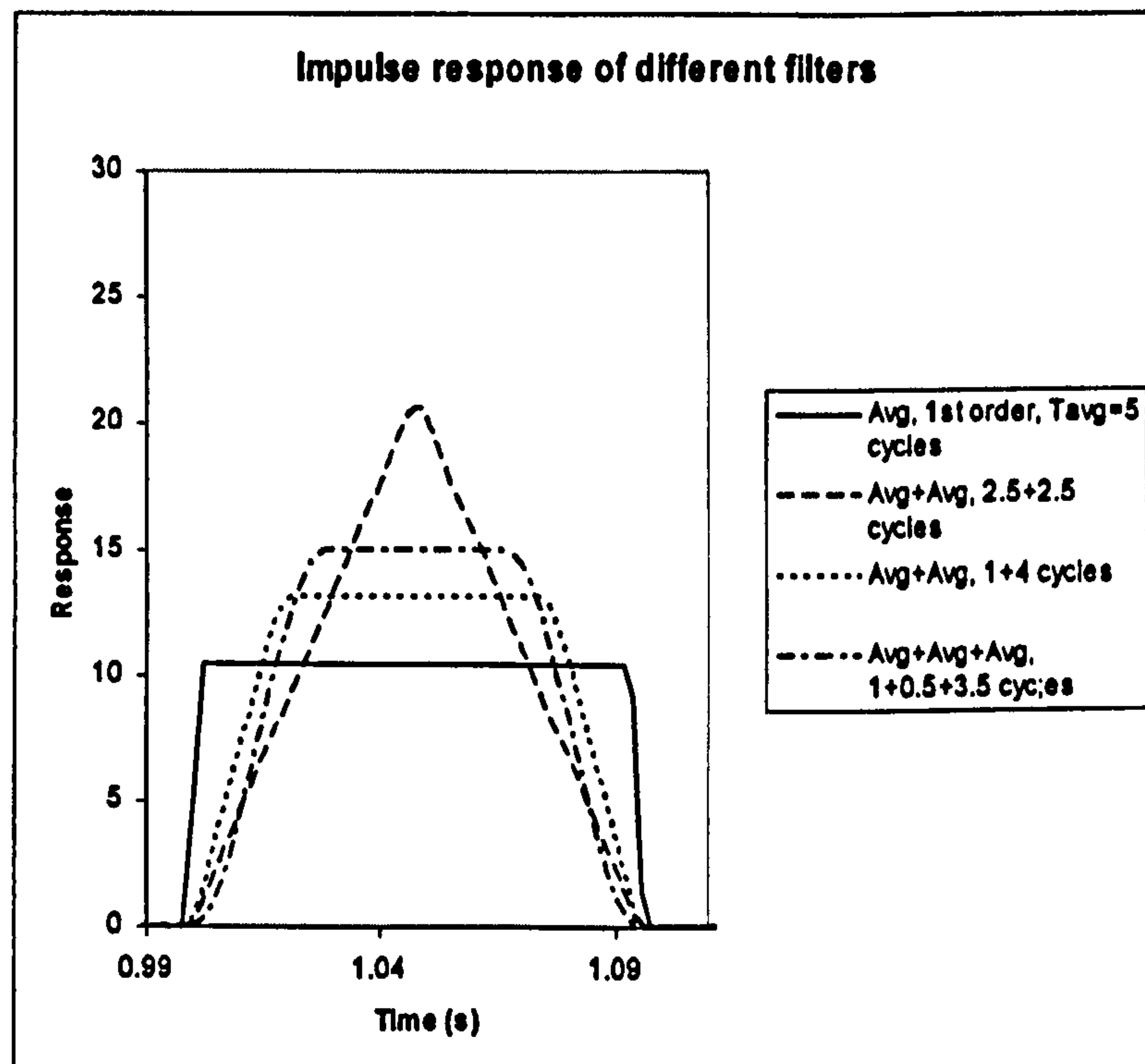


Figure 3-20 : Impulse response of different cascaded averaging filters

All the filter combinations in Figure 3-20 have the same total setting time of 5 cycles, but the cascading is different. This is highly relevant for later sections such as section 3.9 and section 4.3, where a 1-cycle Fourier correlation (involving a 1-cycle averaging) can be followed up by a $\frac{1}{2}$ cycle averaging, and then by subsequent stages of averaging to provide the optimum response to ripple and noise. The peak magnitude of the impulse response for a lone average filter is proportional to $1/N$ where N is the number of samples (or the length of time) over which the average is taken. It can be shown that the peak magnitude of the response of a cascaded pair of averaging filters will be proportional to $1/\max(N1, N2)$ where $N1$ and $N2$ are the lengths of the two filters in samples (see appendix B.4). Thus, for the cascaded pair of filters of length 2.5 cycles each, the peak magnitude is twice that of the lone 5-cycle filter. The other cascaded combinations provide intermediate results.

3.3.3 Frequency response of digital filters

To reinforce the statements of section 3.3.2, the bode plots for the digital low-pass and digital averaging filters can be compared. Below are shown the zero & pole positions and the bode plot for the low-pass filter with "5RC" set to 0.095 seconds ($F_c=8.38$ Hz by {B.5}).

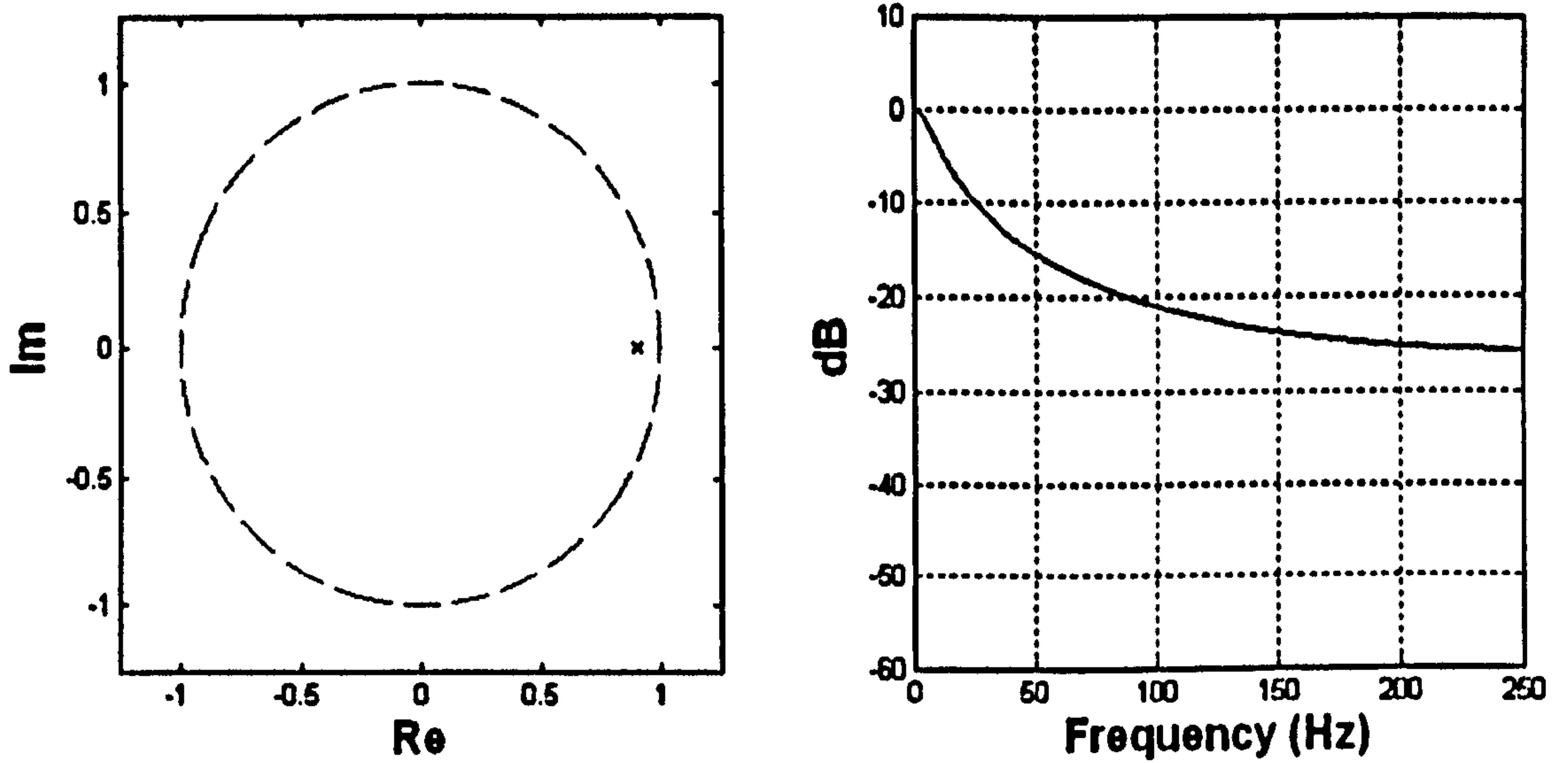


Figure 3-21 : Single pole and bode plot for low-pass filter with $F_c=8.38$ Hz ($"5RC"=0.095s$), $T_s=1/500$ s

The low-pass filter shows relatively poor attenuation of signals above 100Hz, when compared to the equivalent plot (below) for the single-stage averaging filter with 47 samples of averaging (equivalent to averaging over 0.094s).

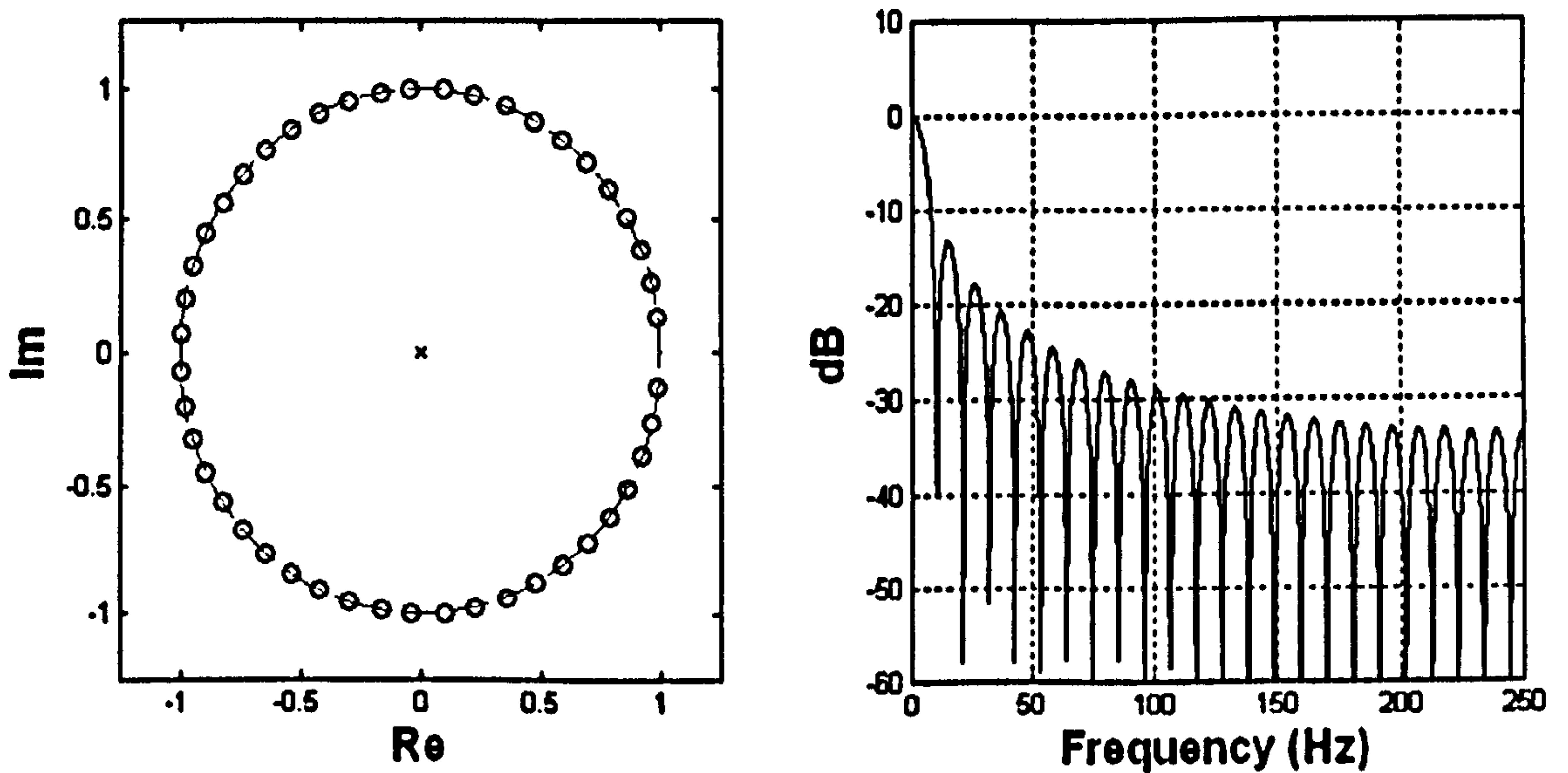


Figure 3-22 : Poles, zeros and bode plot for averaging filter with 47 samples, $T_s=1/500$

This is a filter with 47 zeros and 47 poles. The poles are all at $0+0j$, and the zeros are scattered around the unit circle. As such, it forms a comb filter with many notches.

Figure 3-22, when compared to Figure 3-21, explains why the averaging filter is much more effective at removing noise than the low-pass filter. The averaging filter has >5 dB better attenuation across the range, particularly at the notch frequencies.

Referring back to section 3.3.2.1, the case of the two cascaded averaging filters can also be analysed. This is done by using 2 off, 23-sample averaging filters in cascade (0.092s total response time). When transformed into the z domain, this results in 46 poles at $0+0j$, and 46 zeros on the unit circle (see Figure 3-23). As distinct from Figure 3-22, however, the zeros form only 23 distinct zeros, in 2 sets of identical pairs overlaying each other. Thus, the number of notches is halved, but the attenuation between them is improved. This filter combination shows up 30dB better attenuation than the low-pass filter for frequencies approaching half the Nyquist frequency. Thus, a cascaded pair of equal-length averaging filters is much, much better at attenuating unwanted Gaussian (broadband) noise signals than a low-pass filter, when the averaging filter latency (response) time is set equal to the low-pass filter "5RC" time.

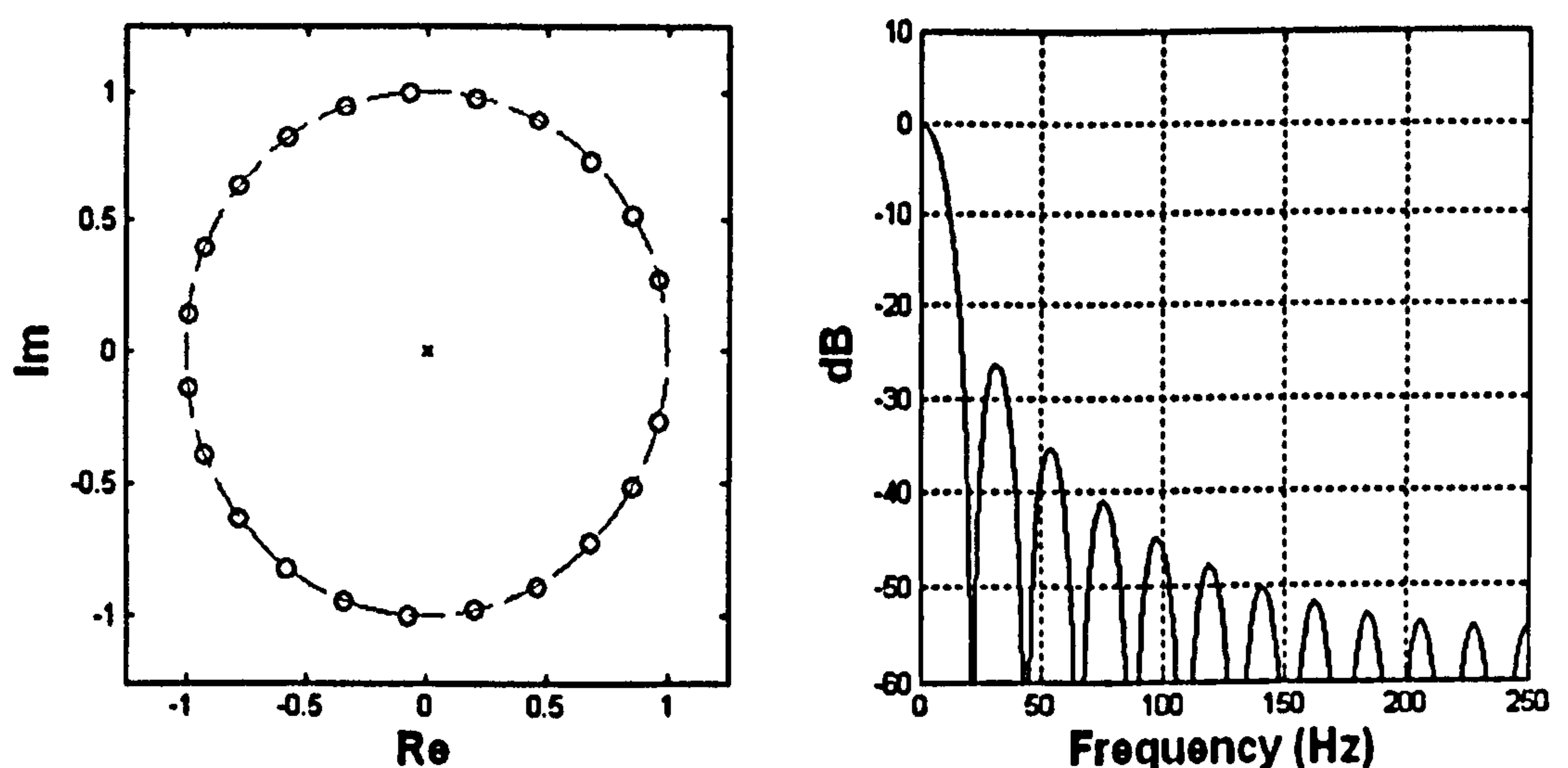


Figure 3-23 : Poles, zeros and bode plot for 2 cascaded averaging filters with 23 samples, $T_s=1/500$ s

3.3.4 Noise rejection of filters

In the case of a single averaging filter, length 5 cycles, an individual noise spike entering the filter immediately affects the output by a weighting which then stays constant for the duration of the filter length. After this time, the noise spike effect is then totally removed from the filter output. The bandwidth of the noise at the output is unchanged, but the magnitude is reduced. This leads to a smoother output than the low-pass filter, due to the lower peak magnitude of the impulse response, and in particular the fact that a noise spike entering the low-pass filter is immediately (technically, with a one-sample delay) passed to the output by the low-pass filter's maximum weighting.

By comparison, the cascaded average filters create a filter with gradually ramping weightings, which ramp from zero up to a peak, then a decreasing weighting towards the end of the impulse response. This is akin to the Hanning or other raised-cosine window

functions which provide improvements over a uniform window when carrying out Fourier transforms. The result is that the noise is much better attenuated by these cascaded filters.

The graphs below show the outputs from the example filters, when the input signal is Gaussian noise with an RMS value of 1. The low-pass filter and slew-rate filters are still configured to have 5RC times of 5 cycles and slew rates of 1 over 5 cycles, respectively, which are designed to match the response of the exact-time averaging filters for the unit step scenario. Due to the nature of the data and to add clarity, the data is presented on several separate graphs with the same scales for comparison.

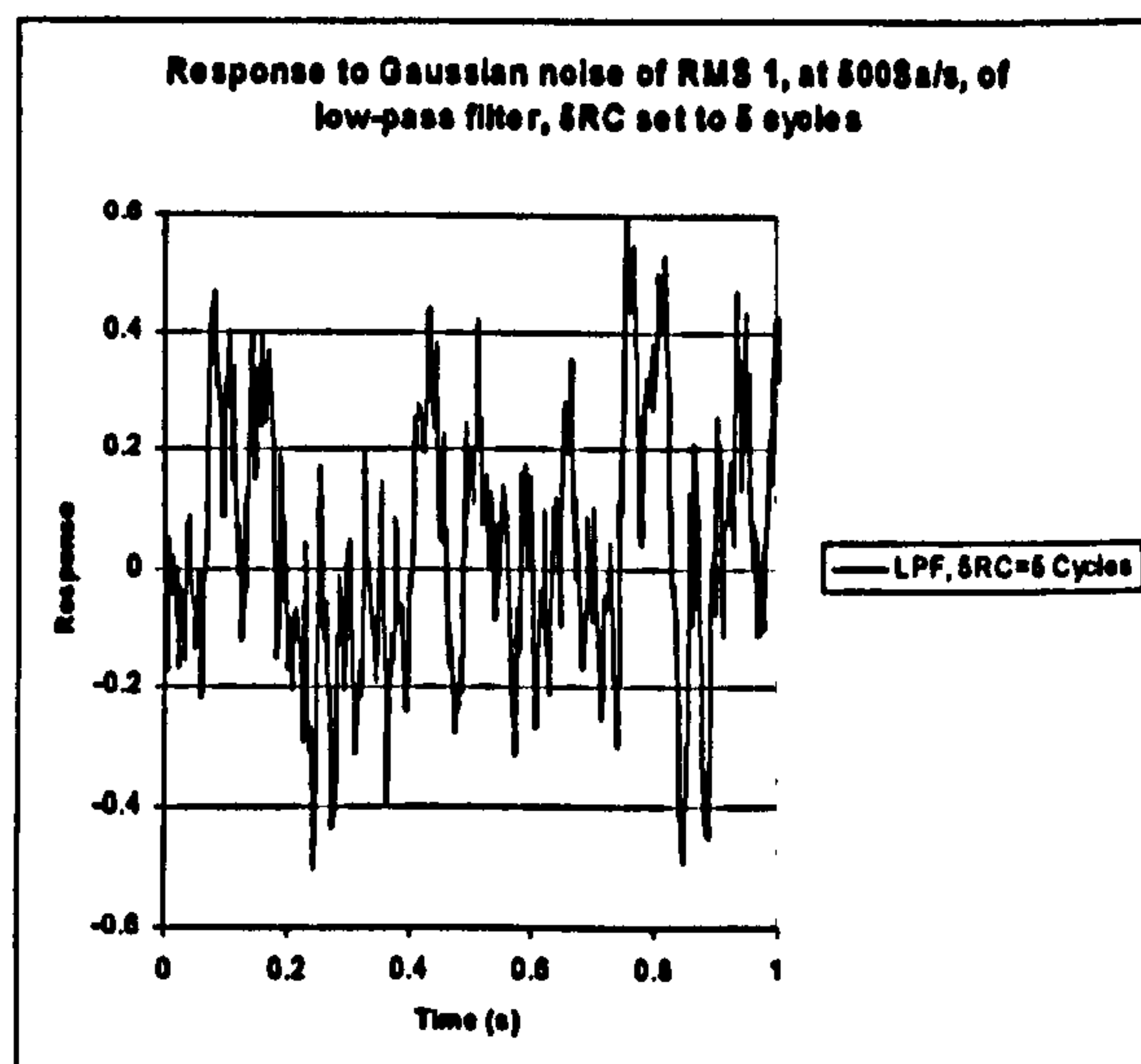


Figure 3-24 : Response to noise of the low-pass filter

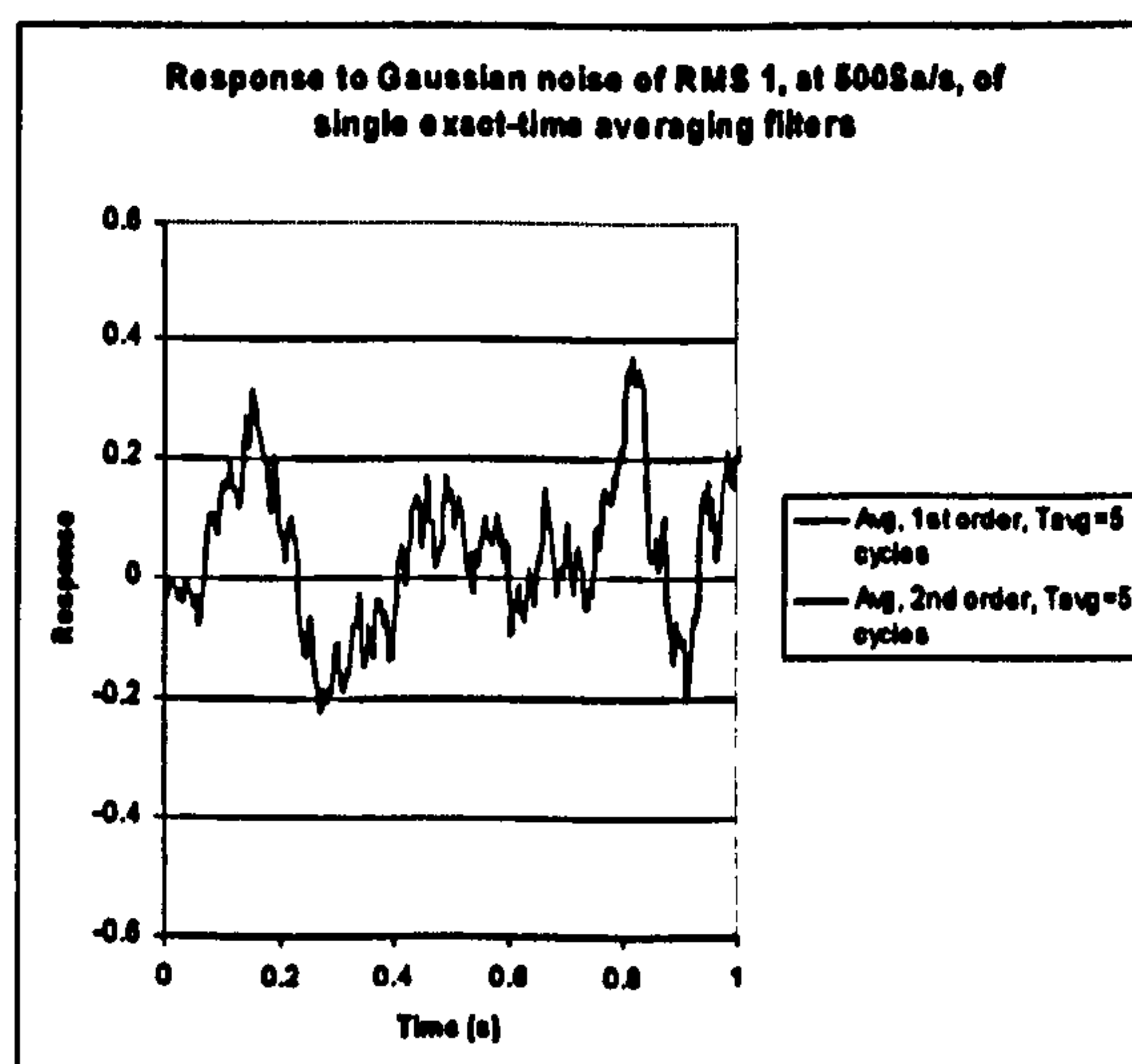


Figure 3-25 : Response to noise of the un-cascaded 1st and 2nd order exact-time averaging filters

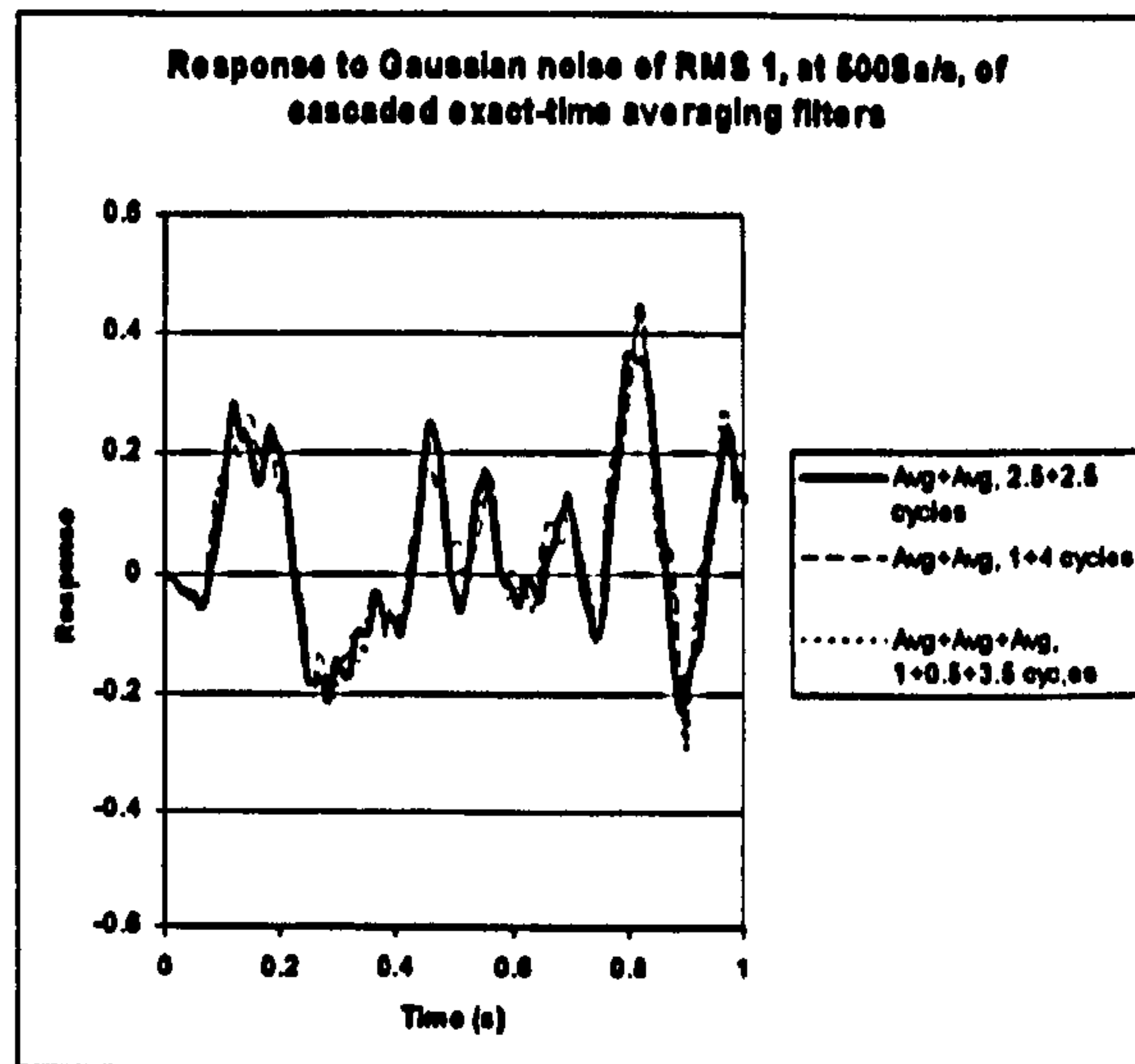


Figure 3-26 : Response to noise of the cascaded exact-time averaging filters

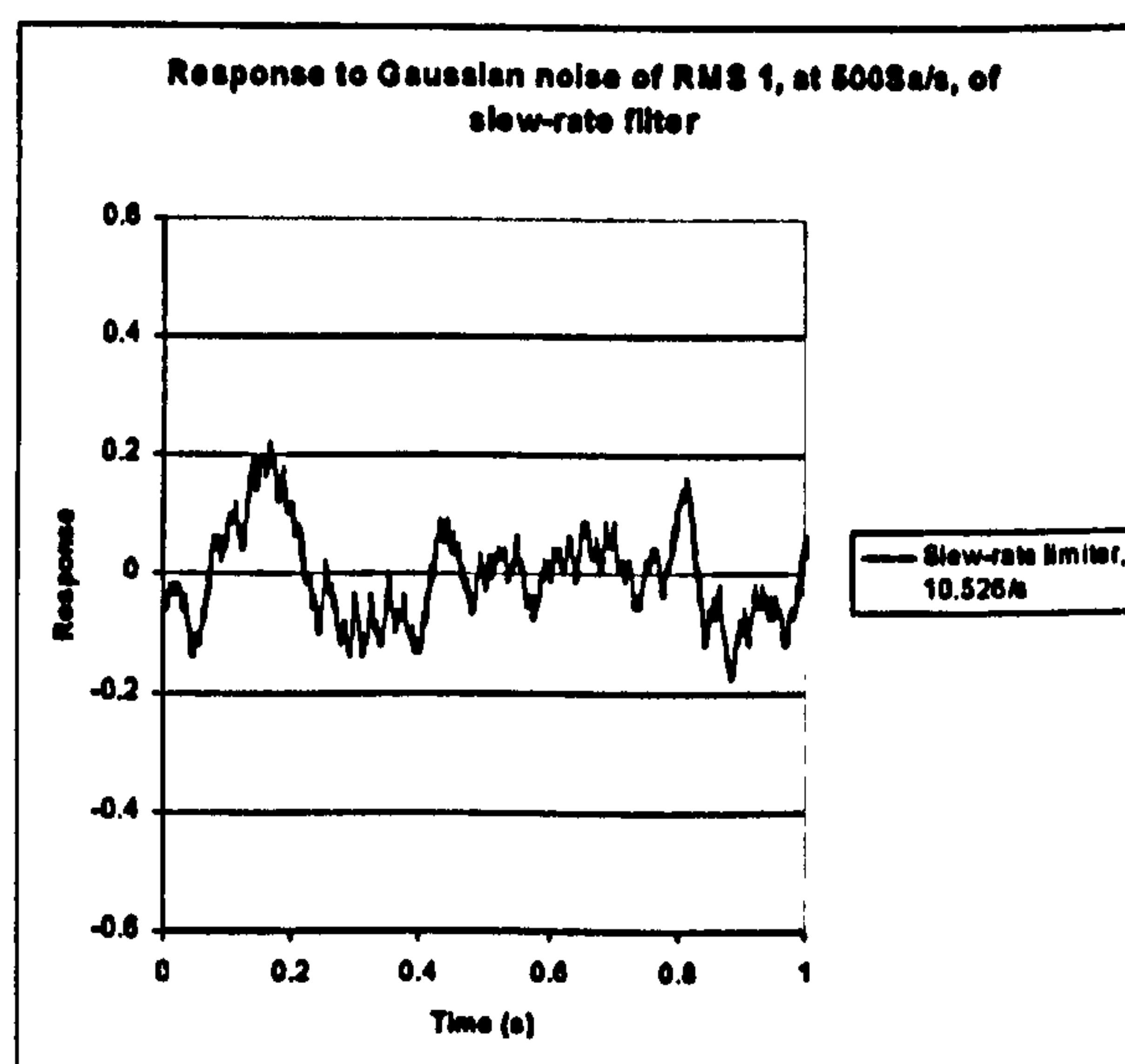


Figure 3-27 : Response to noise of the slow-rate filter

The findings from Figure 3-24 to Figure 3-26 are as expected. The averaging filter reduces the noise better than the low-pass filter. The 1st and 2nd order averaging filters have almost identical performance in noisy environments. The output from the cascaded averaging filters in Figure 3-26 are of the same overall magnitude as the un-cascaded filter shown in Figure 3-25, because the lower frequency noise components are attenuated identically. However, Figure 3-25 contains high-frequency noise which has been removed on Figure 3-26 by the superior noise attenuation of the cascaded filter.

Figure 3-27 shows the performance of the slow-rate filter for the same noise input. The slow rate filter, in this case, performs better than all the other filters.

3.3.5 Ripple rejection of filters

The final input signal analysed is a ripple of peak amplitude 1 at a known frequency. In this case this frequency is 52.632 Hz. This frequency is chosen because it is the frequency at which the exact-time averaging blocks work worst, as the interpolation errors are greatest due to having 9.5 samples per cycle at 500 Sa/s.

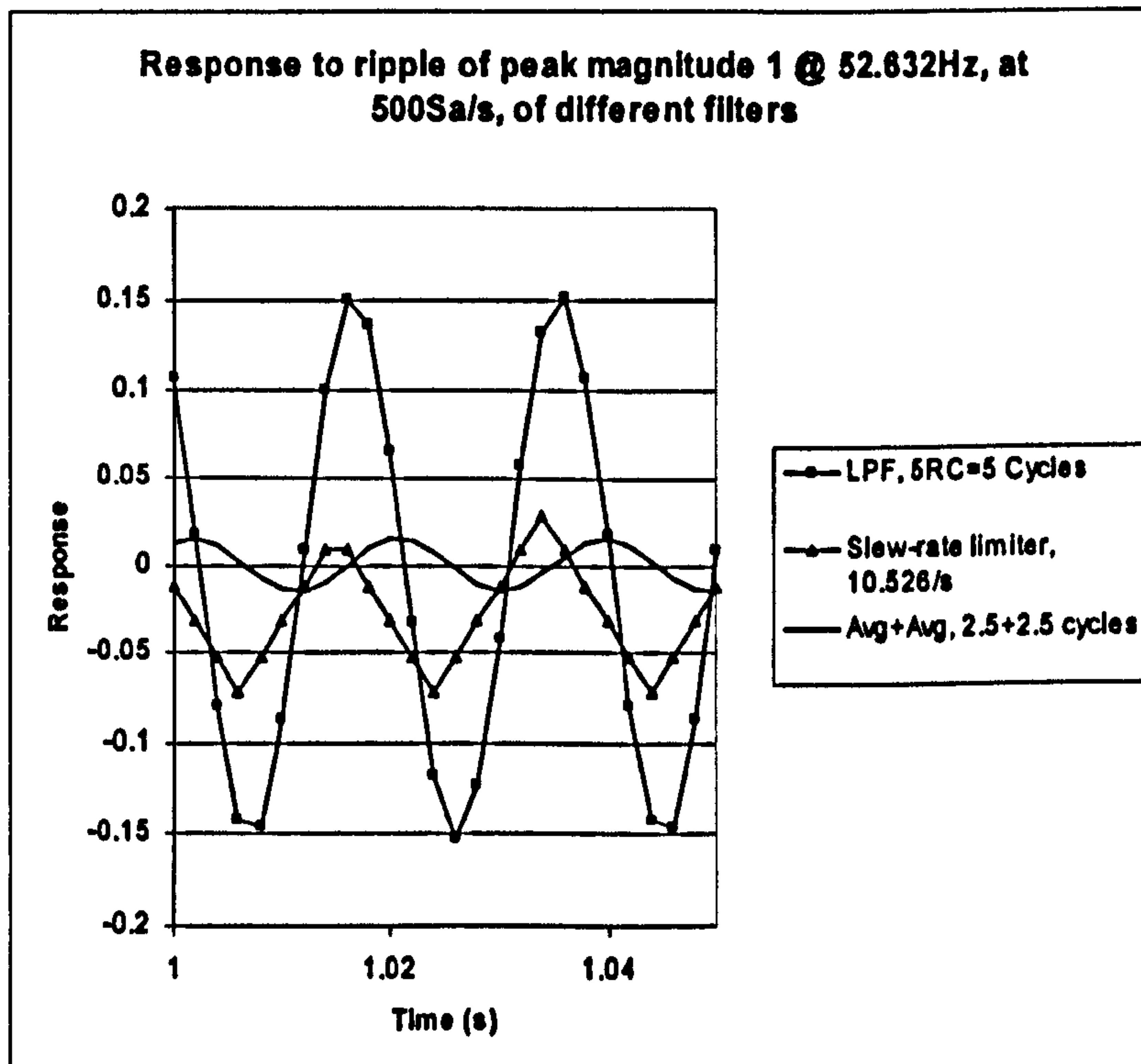


Figure 3-28 : Response to ripple of unsuitable ripple rejection filters

The filters whose outputs are shown in Figure 3-28 are not suitable for rejecting ripple. The low-pass filter has the worst response. The slew-rate limiter filter has a poor ripple, plus a DC offset appears due to the filter's non-linearity (clipping). The cascaded averaging filters with times of 2.5 cycles plus 2.5 cycles are also relatively ineffective. This is because each filter does not span a time which is an integer multiple of the ripple period.

In contrast, the filter combinations shown in Figure 3-29 are very suitable filters for ripple rejection.

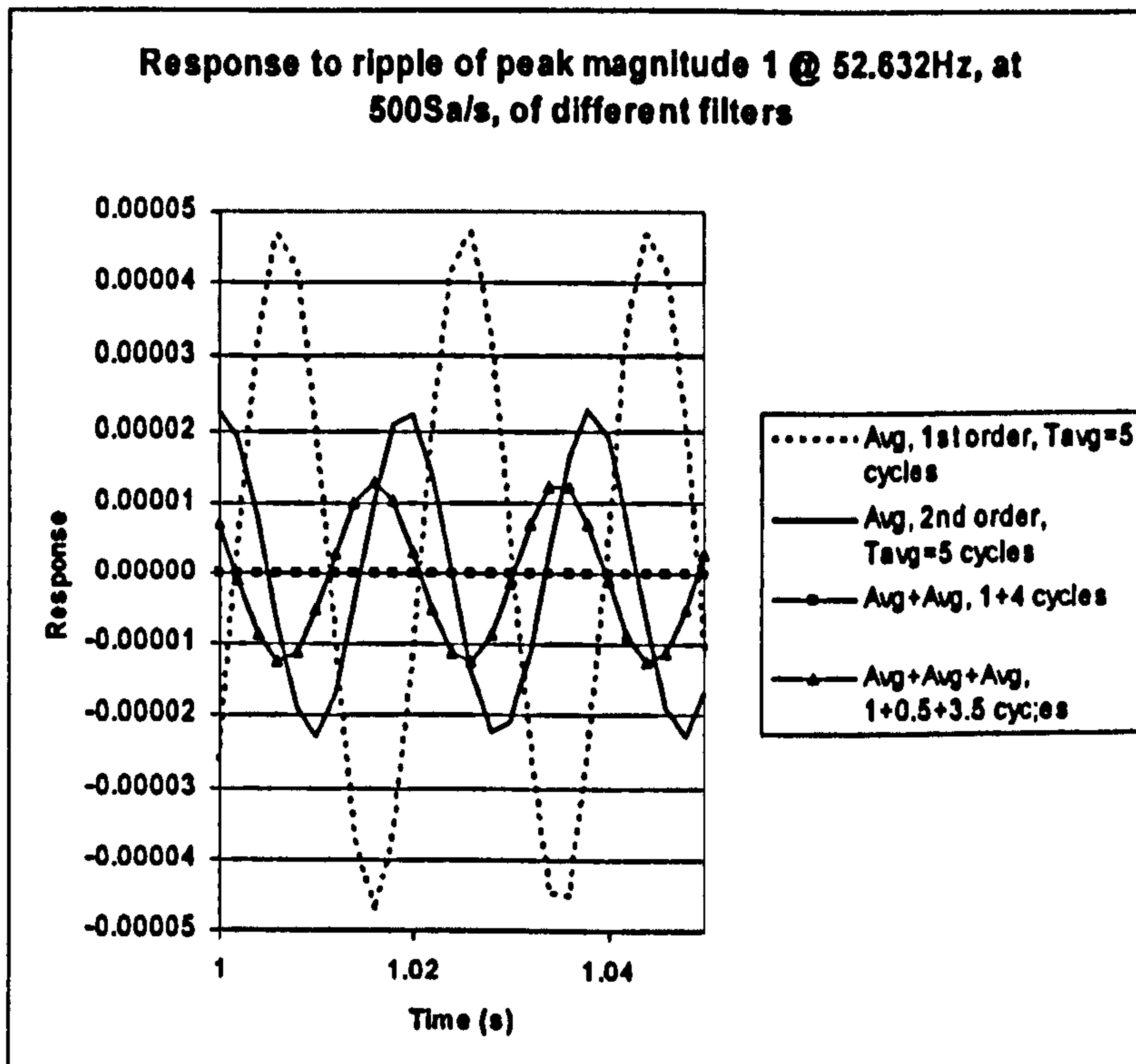


Figure 3-29 : Response to ripple of suitable ripple rejection filters

The exact-time averaging filters which use at least one section with a time average setting equal to an integer multiple of the ripple period, all provide excellent ripple rejection. The un-cascaded 1st order filter provides ≈ 86 dB of rejection. The equivalent 2nd order filter provides ≈ 94 dB of rejection. Cascading of multiple filters, each with time average settings equal to an integer multiple of the ripple period, provides even greater ripple rejection. The ripple is “entirely” rejected by the 1+4 cycle cascaded filter. Note that the 1+0.5+3.5 cycle filter does not perform as well as the 1+4 cycle filter, due to the non-integer cycle period timeframes used for the 2nd and 3rd averaging sections.

In reality, ripple rejection will be unlikely to be fully effective to these quoted levels, due to other noise and interfering effects which will affect both the ripple rejection itself, and also the measurement of frequency (or ripple frequency), so that the input time period for the exact-time average filter will usually be slightly in error.

3.3.6 Findings from this section

- The exact time-period averaging blocks are extremely effective at removing ripple(s) from signals if the fundamental ripple frequency is known.
- The 2nd-order exact-time averaging block removes ripple about 6dB better than the 1st-order block (a further halving of ripple magnitude). However, in the presence of noise, the advantage is lost.

- The exact-time-period averaging blocks out-perform low-pass filters both in their step response and noise response characteristics.
- Cascaded averaging blocks can be used both to reduce Gaussian noise at the output, and to provide further rejection of unwanted ripple at known frequencies.
- Slew-rate filters can offer very good noise reduction in some scenarios. The filter is non-linear, however, which can cause disastrous DC errors at the output for asymmetrically rippling inputs or for symmetrical input signals at certain frequencies relative to the sample rate. To counter this non-linearity the slew-rate limit can be widened but this degrades the noise rejection performance. Also, if the limiting slew-rate is too high relative to the noise or ripple, the filter becomes completely useless as noisy signals pass straight through. There are some scenarios where a slew-rate filter may be the most effective solution, but these have to be carefully examined and justified. An alternative acceleration-limiting filter was also investigated. This has appeal for a number of reasons, but this filter can oscillate under certain input conditions. Therefore it was not deemed robust enough to include in any solutions presented in this thesis.
- Low-pass filters do not provide the best solution for responses to steps, noise, or ripple. Kalman filters, being at root a type of variable low-pass filter, are thus unlikely to offer a good solution.

3.4 Analogue front-end, ADC and digital pre-processing design/considerations, including a novel DC blocking technique

The sampling hardware should incorporate hardware anti-aliasing filters before the ADC stage, to minimise the measurement errors due to aliased harmonics (see section 4.2). Gaussian noise and DC offsets will be introduced by electronic components both before and during the low-pass filtering stage (which probably also includes amplifiers, isolators etc.). The ADC stage will also introduce quantisation noise, small amounts of non-linearity, and some DC offset.

After the data has been sampled, gain and ADC channel-channel timing skew calibration corrections can be applied. Then, a sensible precaution is the inclusion of a digital high-pass filter, of some form. This filter has two potential purposes:-

- It can be used to flatten the gain vs. frequency relationship of the overall (analogue+digital) filter response around the nominal frequency point, thus minimising any gain calibration correction factors.
- It removes DC bias error components which are introduced by instrumentation

amplifiers and the ADCs. These can corrupt an all-harmonic RMS measurement since the 0th harmonic is a valid component. Also, as will be seen in section 3.11, any DC bias can also corrupt fast ½-cycle current measurements.

After careful consideration, this thesis proposes the use of a novel DC blocking filter rather than a digital high-pass filter. In the sections which follow, the analogue anti-aliasing filter is designed. Then, the calibration and digital high-pass options are considered and designed.

3.4.1 Low-pass anti-aliasing filter design

To design the low-pass filter, a trade-off is made between the rejection of aliased harmonics versus distortion of the desired signal below the Nyquist frequency. A sensible compromise is a 2nd order low-pass filter with a cut-off frequency set to 1/3rd of the Nyquist frequency. The filter is implemented as two first-order RC filters cascaded, rather than a single LC filter. This avoids the need for damping, due to the positive gain hump at resonance of an LC filter. At the cut-off frequency, the gain is -6dB, and at the Nyquist frequency the gain is -20dB (voltage amplitudes for unwanted harmonics reduced to <10% of their unfiltered voltage amplitudes. Gain reduces at 40dB/decade for higher frequencies. Scaling the filter cut-off frequency to the Nyquist frequency allows instruments with higher sample rates to process the higher order harmonics successfully, which will improve the measurements of all-harmonic RMS and THD if the instrumentation is noise-free and linear enough.

An increased filter order or decreased cut-off frequency would reject more higher-order harmonics, although attention must be paid to the group delay introduced by the filter. A 1st order low-pass filter set to a cut-off frequency of 125Hz (½ of the Nyquist frequency at 10 samples per cycle) will introduce a phase lag of 21.8° to a 50Hz input waveform. Two low-pass filters cascaded will double the lag to 43.6°, or 1/8th of a cycle. For this reason, the filter cut-off frequency should not be decreased below about 125Hz, which becomes relevant for sample rates of less than 750 samples/s, i.e. less than 15 samples per cycle at 50Hz. The resulting formula for calculating a suitable low-pass filter cut-off frequency for a nominally 50Hz system is thus:-

$$F_{CLPF} = \frac{\text{SamplesPerCycle} \times 50}{6} = \frac{F_{Nyquist}}{3} \text{ if } \text{SamplesPerCycle} \geq 15$$

$$F_{CLPF} = 125 \text{ otherwise}$$

(3.2)

By equation {B.4}, the gain of the two cascaded low-pass filters should be:

$$Gain = \frac{1}{\left(\sqrt{1 + \left(\frac{F}{F_{cLPF}}\right)^2}\right)^2} = \frac{1}{1 + \left(\frac{F}{F_{cLPF}}\right)^2} \quad (3.3)$$

The ideal phase lag through the filters can also be calculated from equation {B.4} as:

$$Phaselag = 2 \arctan\left(\frac{F}{F_{cLPF}}\right) \quad (3.4)$$

The physical realisation of the filter may be active or passive circuits, quite likely a cascaded pair of operation amplifiers with capacitive elements in the feedback paths. Thus, the filters may introduce Gaussian noise into the signal. Also, prior to the low-pass filters is likely to be an isolation amplifier (optical or capacitive barrier). Some of these devices operate by chopping the signal at high frequency, and some of these high frequency components will appear as Gaussian noise at the filter output (and in the sampled waveforms) due to parasitic component behaviour and aliasing. These types of noise are included in the overall measurement requirements in section 2.9.

3.4.1.1 Time response of the anti-aliasing filter (and ADC)

The time response of the anti-aliasing filter can be visualised most easily by direct simulation. The test scenario is a 1pu input sinusoid at nominal frequency, which undergoes a 2 cycle brownout, beginning and ending at the peak of the cycle, so as to cause greatest disturbance to the filters. This waveform is generated at a high sample rate in simulation, to simulate analogue hardware. (An analysis of the sample rate required to accurately model an analogue filter is given in appendix B.2.2). The delay due to sampling can also be shown by using the Simulink “rate transition” block to simulate sampling. Two cases are shown here:-

- 10 samples per cycle, 2 cascaded low-pass filters with cut-off frequencies of 125Hz
- 30 samples per cycle, 2 cascaded low-pass filters with cut-off frequencies of 250Hz

At 10 samples per cycle (see Figure 3-30), the phase lag of filter is 43.6° when the input is a steady sine wave at nominal frequency. This is not a problem so long as all voltage and current inputs on all phases are processed using the same, matched (or calibrated) sets of filters so they remain coherent. Exact measurement and calibration of this phase lag might be important if the measured phases of the inputs compared to an absolute time reference

(e.g. GPS clock) are to be used to communicate phase information to other similar, distant control devices/relays. This might be relevant for a loss-of-mains or islanding detection system based upon relative phase measurements at different, distant nodes within a power system.

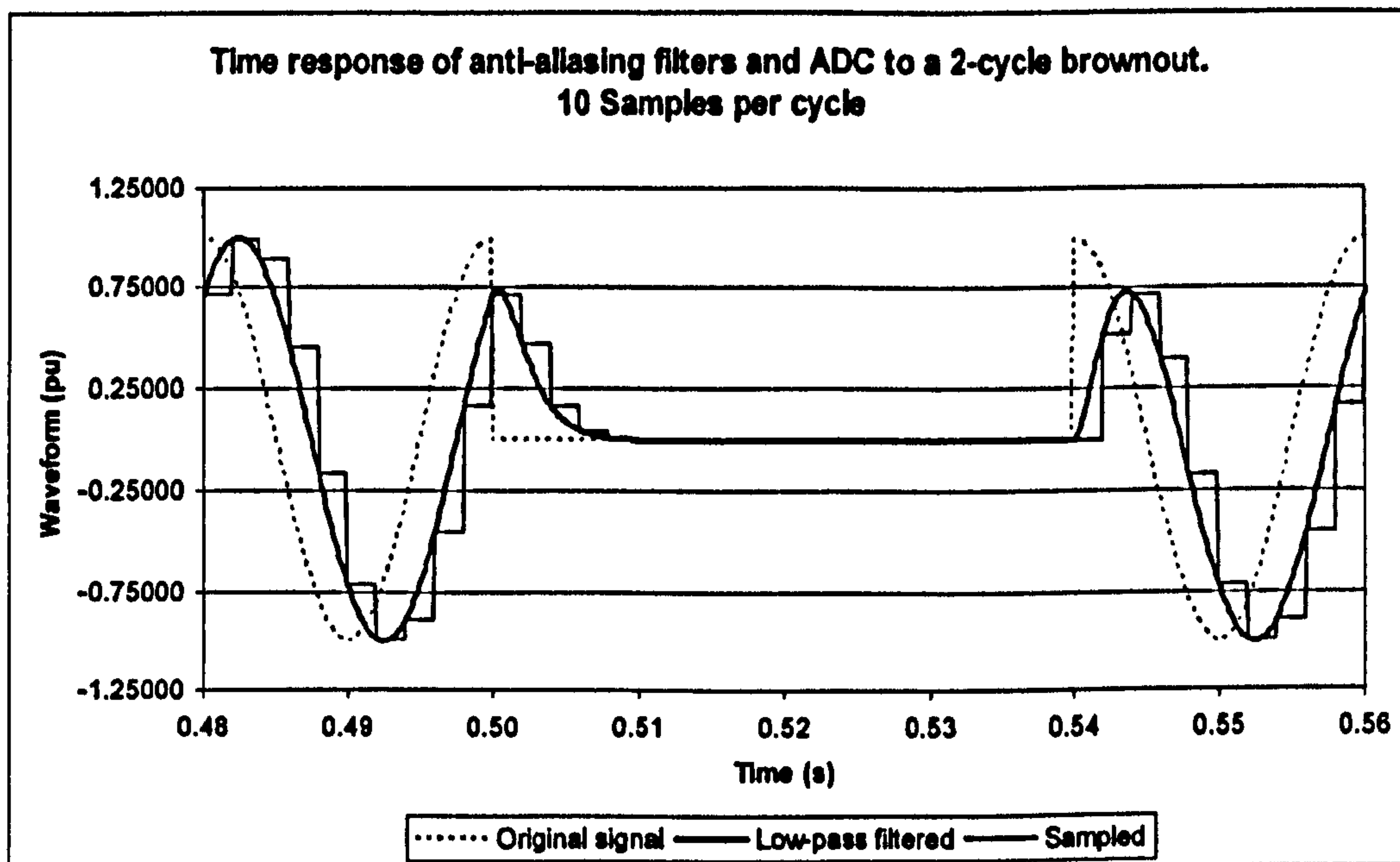


Figure 3-30 : Low-pass filter response and sampling delay at 10 samples per cycle

When a sudden perturbation occurs, the time response of the 2 low-pass filters with 125Hz cut-off frequency, plus ADC sampling, is approximately 0.01 second (½ a cycle).

A way of more theoretically calculating the “reaction time” is that the average “reaction time” of the cascaded pair of low-pass filters and sampling at some frequency F will be:-

$$\text{“SteadyStateReactionTime”} = \frac{2 \arctan\left(\frac{F}{F_{CLPF}}\right)}{2\pi F} + \frac{T_s}{2} \quad (3.5)$$

Which accounts for the steady-state phase lag from equation (3.4) plus the average sampling delay (which will be half of the sample rate). For 50Hz, at 500Sa/s, with a low-pass cut-off at 125Hz, this equates to only 0.0034s (1/6th of a cycle)

During a transient, the “reaction time” appears to be larger than the steady state value calculated by this equation. This is due to the exponential decay nature of the filter after a step function input. The “worst case transient reaction time” can be re-evaluated by taking the “5RC” value of the 2 low-pass filters, which is the time taken to settle to 99.3% (1-e⁻⁵) of a step function input. In this case we obtain

$$\text{"SteadyStateReactionTime"} = \frac{1.44 \times 5}{2\pi \cdot F_{cLPF}} + \frac{T_s}{2} \quad (3.6)$$

where 1.44 is the factor by which the settling time for a cascaded pair of low-pass filters takes to settle to 99.3% of the step function value, compared to a single low-pass filter. (This value found by experimental simulation). This evaluates, at 500Sa/s, with a low-pass cut-off at 125Hz, to 0.010s (½ a cycle), and matches the estimated value from the simulation in Figure 3-30. This result is quite conservative, and accounts for a complete settling of the filter to a transient input. The filter "reaction time" must be borne in mind when accounting for the total latency of the measurement system, which will be made up of this time plus the digital processing/averaging time. The total time will be of most relevance where fast-acting relay action is required.

At 30 samples per cycle, the response time of the filters decreases below 0.005 second (¼ cycle), as shown in Figure 3-31. This is due both to the higher cut-off frequency of the analogue filters, plus the reduced sampling delay. At higher sample rates, the latency decreases further towards zero.

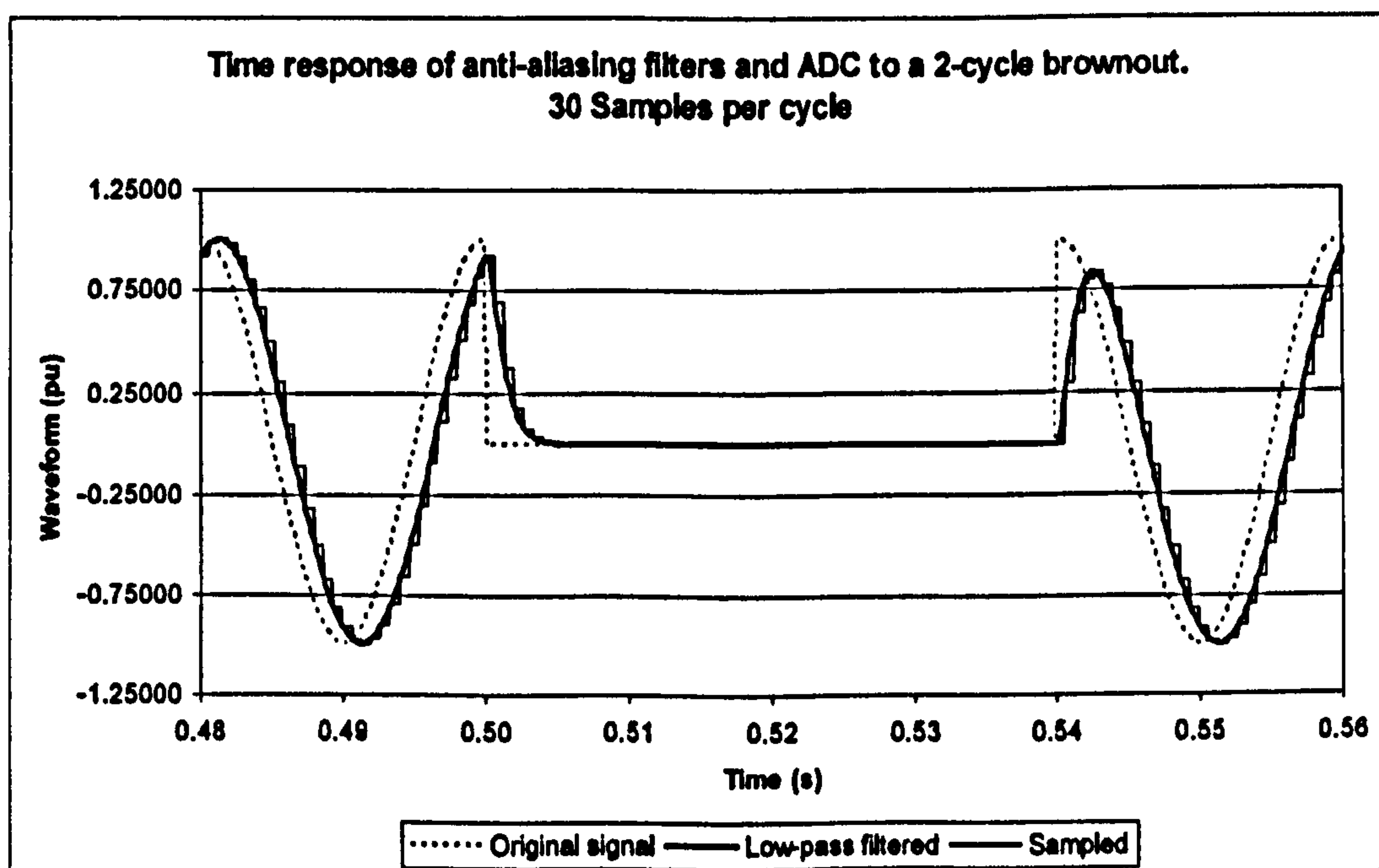


Figure 3-31 : Low-pass filter response and sampling delay at 30 samples per cycle

3.4.2 ADC effects

The ADC introduces quantisation noise. Typically an ADC has 12 bits. Modelling this in a theoretical form is difficult, but introducing the effect to a simulation is relatively easy. For voltage measurements, the scaling can be set so that, for example, 2pu +ve or -ve peak values cause 0 or 0xFFF ($2^{12}-1$) full-scale readings on the ADC. This means that the

nominal -1pu to +1pu voltage range is divided into 2^{11} discretised values, and so the introduced errors are very small. For current measurements, the maximum measurable current (without saturation of the CTs, instrumentation, or ADCs) must be decided, and the ADC scaling set from there. ADC quantisation can therefore be significant if the actual current flowing is small relative to the peak measurable current. A real ADC also has slight non-linearities, which are not addressed in this thesis, (nor are VT and CT saturation/linearities), since this analysis is focussed on the errors due to digital processing. The ADC non-linearity is also small compared to the potential maximum harmonic content of the input signals (section 2.7.2). In addition to the theoretical quantisation noise, often the noise within the ADC hardware actually makes the lowest bit(s) of the ADC random. Allowance for this is made in the measurement requirements in section 2.9.

3.4.3 Post-ADC calibrations/corrections

After the signal has been sampled, there are several tasks to perform before the Fourier analysis is carried out:-

1. Removal of DC bias components which are introduced by instrumentation amplifiers and the ADCs.
2. Correct the input signals for relative phase offsets, due to ADC channel-channel time skews (if the ADCs are multiplexed) or different VT/CT performances.
3. Amplitude calibrations for each measurement channel and (calculation of) the overall phase calibration of the input signals. The calibration coefficients can be based upon manual "one-time" measurements at just one (nominal) frequency or at several frequencies. This corrects for the gains of all hardware including VTs, filters, and ADC etc. It might be sufficient to use a single frequency if the gain of the VTs is flat enough, and if the filters are manufactured to a tight enough tolerance. If this is not the case, then several frequencies may need to be calibrated and interpolation used between the calibrated frequencies.
4. Amplitude and (calculation of) phase correction for off-nominal frequency inputs to correct for known gain & phase response transfer functions of the anti-aliasing filters and any post-ADC digital filters (such as the DC block).

The calibration values for steps 2 & 3 can be measured and/or deduced from specifications at or before installation, and stored in a table within the measurement computer system. The calibration values for step 4 can be deduced by inverting equations (3.3) and (3.4), and by using similar techniques for any digital post-ADC filters.

The application of the gain corrections from steps 3 and 4 is straightforward since this involves purely a multiplication of the sampled signal value by the calibration value. The application of the phase corrections requires substantially more care.

The method of application, particularly the ADC time-skews, varies depending upon the way that the sampled waveforms will be analysed. It can be achieved in two ways:-

1. by delaying the input signals appropriately and interpolating between samples so that each input signal then appears to be coherent (2nd order interpolation has been shown to work well). This is definitely the appropriate way to deal with the small ADC channel-channel time-skews within inverter control systems which convert 3-phase sampled data directly into the dq frame without a Fourier analysis stage.
2. by carrying out Fourier analysis of each sampled channel directly, and then applying a post-correction to the measured phase of the data.

During this thesis, both methods have been used. The additional factors which influence the choice of method include the computational effort required for subsequent algorithms such as the processing of Fourier measurements of 3-phase signals into the positive and negative sequence components. When all things are considered, the best method is to use both techniques together. Firstly, the small relative time skews between all voltage and current measurements (ADC channels) at a single node should be corrected up front via the first method. This allows calculation right through to the sequence analysis with minimal trigonometric calculations. The overall larger common (absolute) time skew for all these channels (relative to some known/fixed reference) should be corrected at the end, after all magnitudes/phases and sequence analysis is complete.

3.4.4 DC block / high-pass filter design

Immediately after the ADC (and before application of any calibrations) a DC block is desirable. This removes DC bias error components which are introduced by instrumentation amplifiers and the ADCs. Two possible options are compared in the following sections. The first is a digital 1st-order high-pass filter. The second is a novel DC blocking algorithm based upon the exact-time averaging technique previously introduced.

3.4.4.1 Digital high-pass filter option

A high-pass filter blocks the DC component but can also be used to flatten the gain of the entire cascaded filter section (low-pass + digital high-pass) vs. frequency around the nominal frequency point. Appendix B.3 and equation {B.9} show how the required cutoff

frequency of the high-pass filter F_{CHPF} can be calculated to achieve this goal at nominal frequency f , when cascaded with two low-pass filters with cutoff frequencies of F_{CLPF} .

For 10 samples per cycle (500 Sa/s), with the 2 low-pass filters set at 125 Hz ($\frac{1}{2}$ Nyquist) and $f=50$ Hz, this results in a high-pass filter cut-off frequency of 30.86Hz and an overall response shown below (normalised to 0dB @ 50Hz).

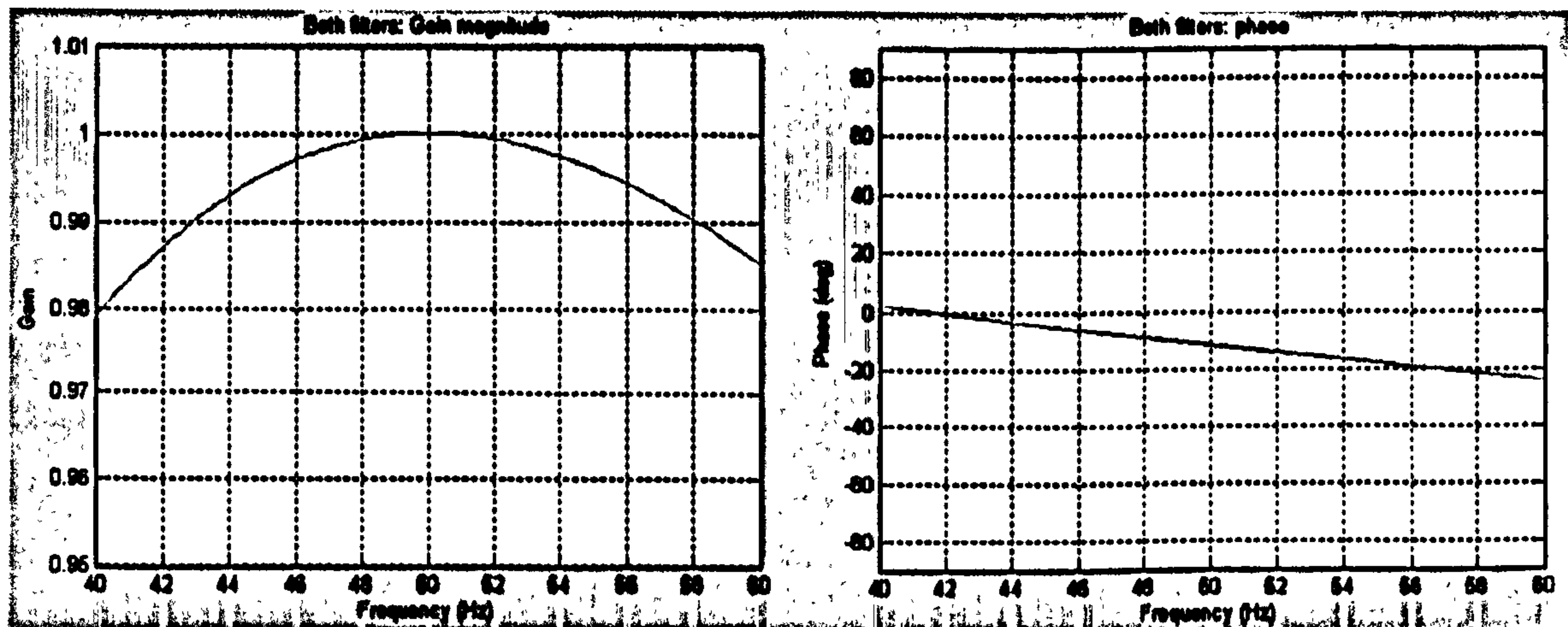


Figure 3-32 : Low-pass / High-pass filter combination for 500 Sa/s

Note that the overall steady-state phase response has been “improved” from a 44° lag at 50Hz (due to the low-pass filters alone, see section 3.4.1) to only a 10° lag. However, the actual response of the system to sudden changes in input will still be lagged in time by approximately the original time lag group delay of the low-pass filters ($1/8^{\text{th}}$ of a cycle) plus the ADC sampling lag, plus the group delay of the digital high-pass filter.

At higher sampling frequencies, the low-pass filter cut-off frequency can be increased and the high-pass cut-off frequency required for the flat gain condition decreases. The flatness of the gain curve improves. For example, at 30 samples per cycle (1500 Sa/s at 50Hz), the low-pass cut-off is 250Hz and the high-pass cut-off is 14.43Hz. The resulting filter response is as below:

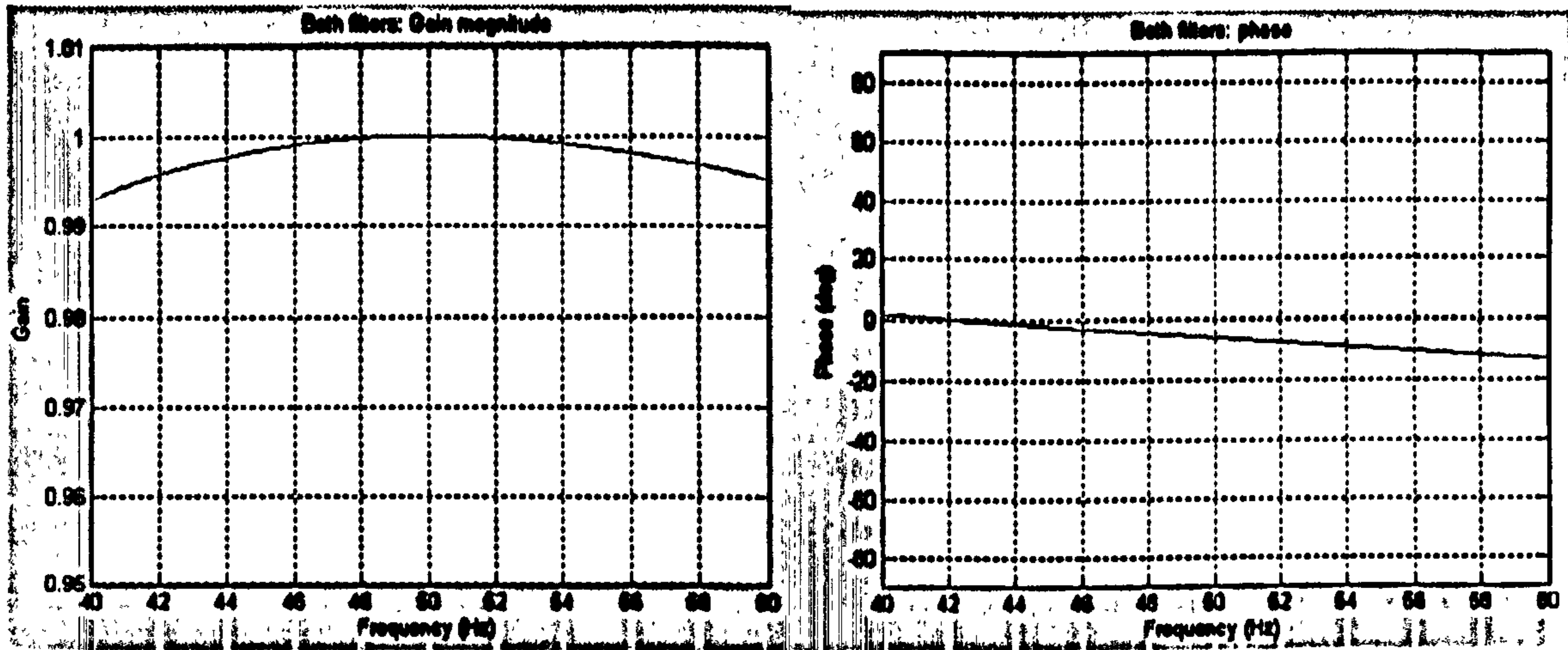


Figure 3-33 : Low-pass / High-pass filter combination for 1500 Sa/s

3.4.4.2 Novel DC blocking technique option

An alternative to the digital high-pass filter is a novel DC block, designed using the blocks described in section 3.2. The idea is to measure the amount of DC present on the input signal, and then subtract this from the input signal. This means that the DC blocking filter has absolutely zero propagation delay for AC signals. The rationale for using this block instead of a standard high-pass block is:-

1. That the exact-time averaging blocks can be used to reject “ripple”, orders of magnitude better than the high-pass filter. Since the input signal is expected to be a sine wave, the entire input signal is in fact “ripple”.
2. That the DC offset of the sampled data is expected to be relatively constant, due to component behaviour within the instrumentation (mainly isolation amplifier offsets and operational-amplifier offsets). Thus, the measured DC offset term can be smoothed using a slew-rate filter with a low maximum slew rate setting. Such a slow slew-rate filter rejects noise extremely well, as shown in section 3.3.4.
3. That, although flattening the overall filter gain at nominal frequency by using a high-pass filter is desirable, it is not essential since the low-pass filter gain slope can be corrected during calibration as described in section 3.4.3.

The design of the DC blocking filter is shown below:-

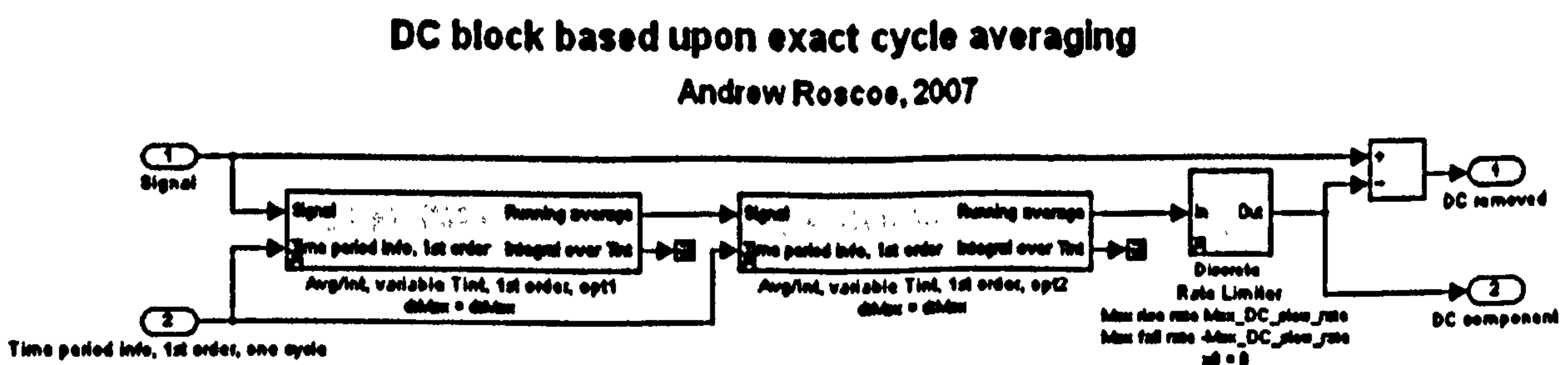


Figure 3-34 : DC block

This block averages the input signal over 2 cascaded cycles. This produces a DC output with virtually zero interpolation ripple (see section 3.3.5) for an input signal which is made up of a fundamental plus harmonics, assuming the measurement of the signal frequency is correct. A departure from these assumptions, such as noise, inter-harmonics, sub-harmonics, or inaccurate frequency estimation, results in an averaged, bandwidth-limited but slightly rippling signal from the two cascaded average filters. Next, a slew rate filter can safely be used in this application to further reduce the effects of noise. The slew rate limit could be reduced to very low levels $\ll 0.1$ pu/s, since the DC offset of the instrumentation will be almost static. However, to speed up settling of the filter both in reality and in simulation, a value of 0.1 pu/s for the slew-rate limit is a sensible compromise. This setting also influences the behaviour of the block during faults which might exhibit a decaying DC component on the measured waveforms (voltage or current). By setting the slew rate to 0.1 pu/s, the DC component will initially be passed straight through the DC block to further processing, but after 1 second the block will filter out 0.1 pu of the DC component (if the DC component is still >0.1 pu). If it is desired to measure DC components during faults with high accuracy, but still remove DC bias due to instrumentation, then the slew rate should be set $\ll 0.1$ pu/s. On the other hand, if removal of the bulk of DC components even during faults is desired, then the slew rate should be set to $\gg 0.1$ pu/s.

To illustrate the benefit of this filter over the high-pass filter described in 3.4.4.1, a simple Simulink simulation was created. This operates at 500Sa/s, 10Sa/cycle @ 50Hz. The input is a synthesised sine wave of 1pu peak amplitude at 52.6316Hz into a high-pass filter and the DC blocking filter. This frequency is the worst frequency for interpolation ripple within the averaging blocks as there are 9.5 samples per cycle. The high-pass filter cut-off frequency is 30.86Hz (see section 3.4.4.1). A large DC offset (0.25pu) is applied to the signal. The DC blocking filter thus takes 0.25 seconds to initially settle. At $t=5$ s, a hard fault is simulated, and the fault is removed at $t=5.1$ s.

Figure 3-35 shows the response of the two filters at the instigation of the fault. On this graph, the input signal has been adjusted downwards by the DC bias of 0.25pu for the purposes of plotting, to create a reference (correct) value. Clearly, the DC blocking filter tracks the reference signal exactly, as the traces are indistinguishable. The high-pass filter, on the other hand introduces small lags in the signal during normal operation, and also causes lag and decay effects during fault conditions.

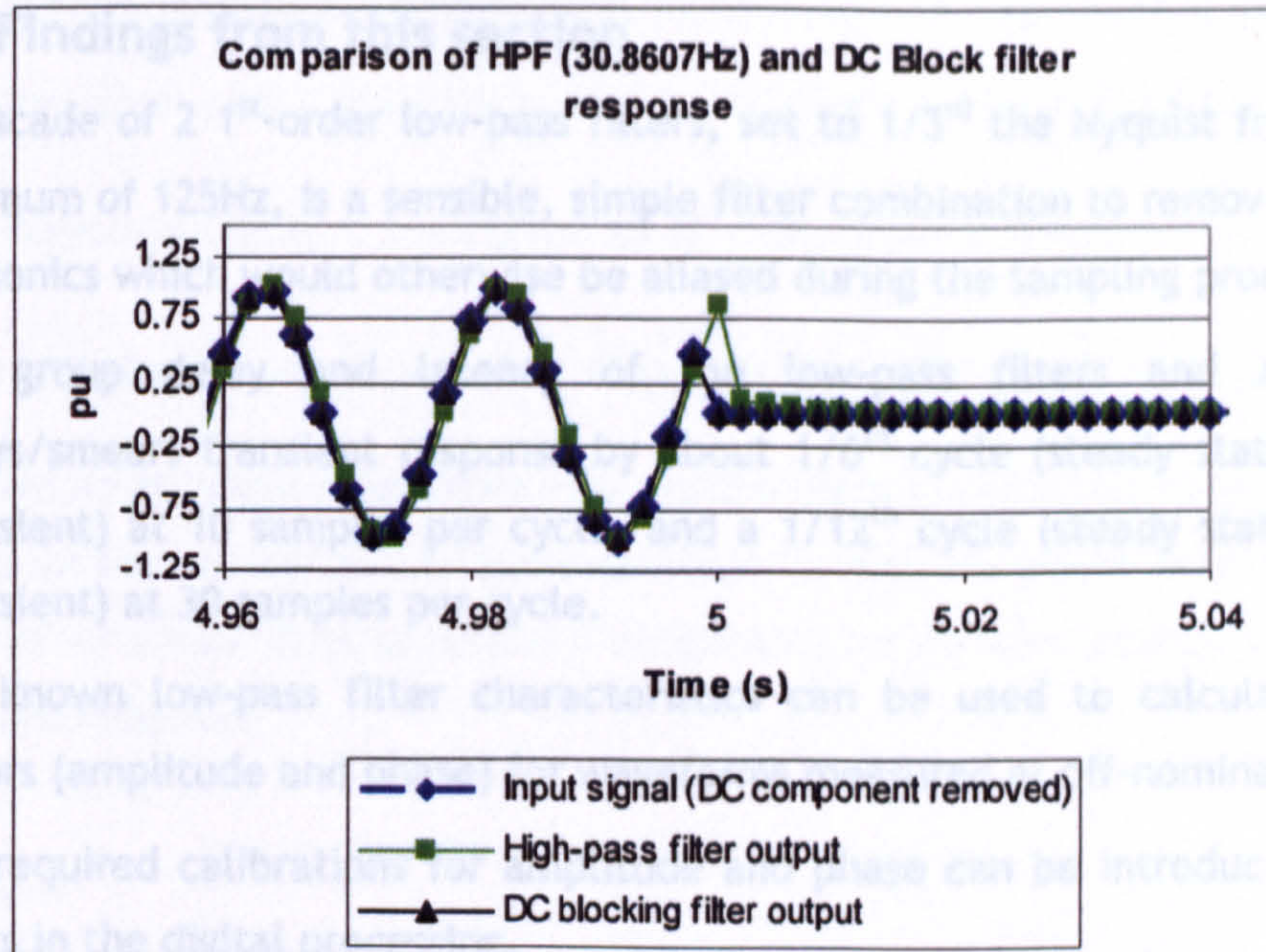


Figure 3-35 : DC block vs. high-pass filter performance

Figure 3-36 shows the errors from the two filter types, which are deduced by subtracting the reference signal value from the filter outputs. The DC Block has a peak error of <math><0.005\text{pu}</math>, whereas the high-pass filter has a peak error of almost 1pu, due to lag in the filter.

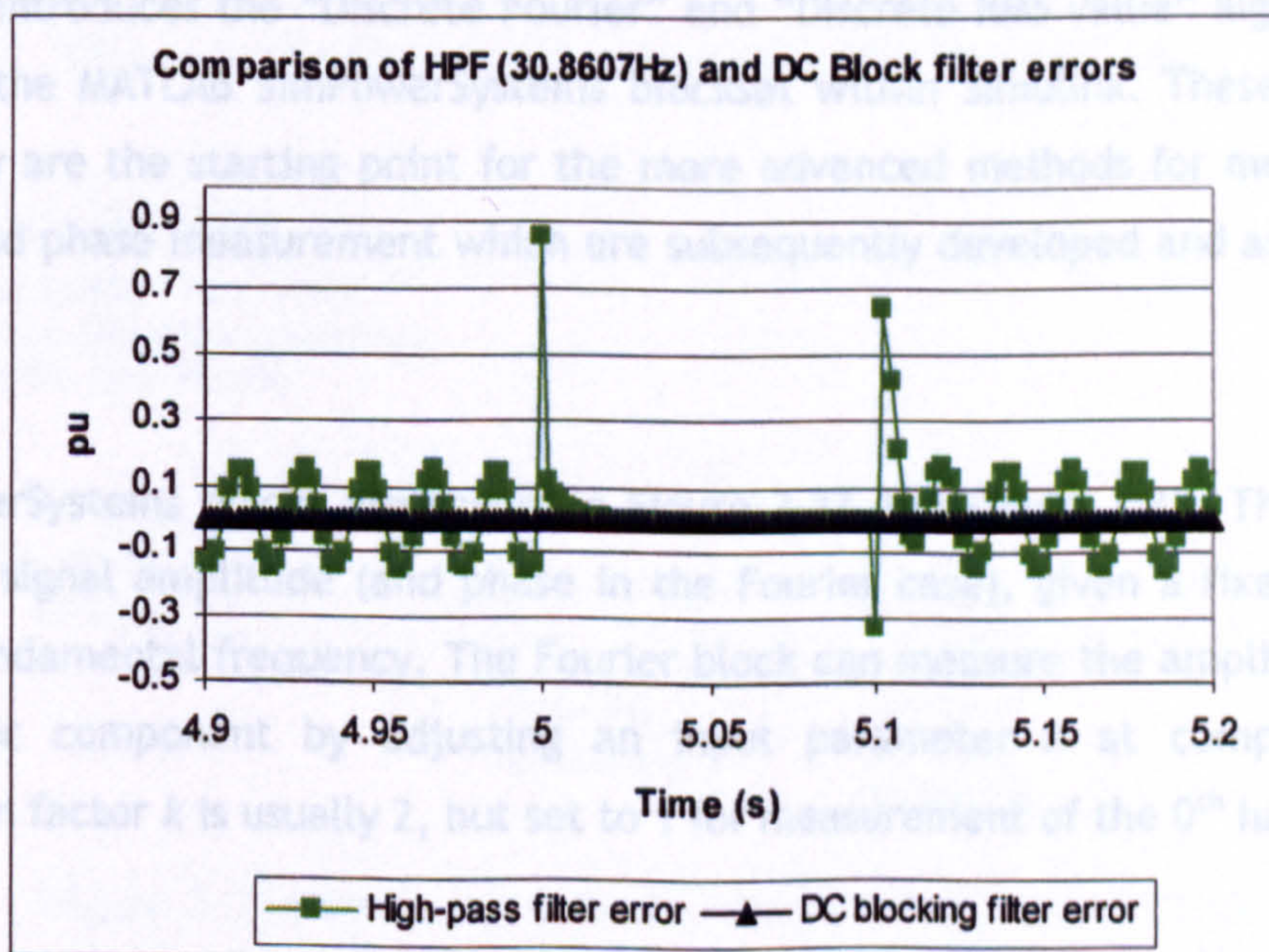


Figure 3-36 : DC block vs. high-pass filter errors

3.4.5 Findings from this section

- A cascade of 2 1st-order low-pass filters, set to 1/3rd the Nyquist frequency, or a minimum of 125Hz, is a sensible, simple filter combination to remove higher-order harmonics which would otherwise be aliased during the sampling process.
- The group delay and latency of the low-pass filters and ADC sampling delays/smears transient response by about 1/6th cycle (steady state) to 1/2 cycle (transient) at 10 samples per cycle, and a 1/12th cycle (steady state) to 1/4 cycle (transient) at 30 samples per cycle.
- The known low-pass filter characteristics can be used to calculate correction factors (amplitude and phase) for waveforms measured at off-nominal frequencies.
- The required calibrations for amplitude and phase can be introduced at sensible points in the digital processing.
- A novel DC block, built using a cascade of 2 exact-time averages and a slew-rate limiter, provides a much better way of removing unwanted instrumentation DC bias from signals, than a digital high-pass filter.

3.5 SimPowerSystems Fourier and RMS measurement blocks

This section introduces the “Discrete Fourier” and “Discrete RMS value” algorithms which are part of the MATLAB SimPowerSystems blockset within Simulink. These are relevant because they are the starting point for the more advanced methods for measurement of amplitude and phase measurement which are subsequently developed and analysed in this thesis.

The SimPowerSystems blocks are shown in Figure 3-37 and Figure 3-38. They measure a single-phase signal amplitude (and phase in the Fourier case), given a fixed estimate of the signal fundamental frequency. The Fourier block can measure the amplitude/phase of any harmonic component by adjusting an input parameter n at compile-time. The multiplication factor k is usually 2, but set to 1 for measurement of the 0th harmonic.

The algorithm evaluates the expression

$$F = \frac{k}{T} \left[\int_{t_0-T}^{t_0} y(t) \cdot \sin(\phi) \cdot dt + j \int_{t_0-T}^{t_0} y(t) \cdot \cos(\phi) \cdot dt \right]$$

where $\phi = 2\pi \cdot nf \cdot t$, f is the estimate of frequency, t_0 is “now” and T is the integration time ($1/f$ for a single-cycle measurement).

In the case of the fundamental measurement (with $n=1$), the magnitude is then given by $\theta = |F|$ and the signal phase (relative to the correlating waveform) is given by $\theta = \angle F$. Notably, the "absolute phase" is then given by $(\theta + \phi)$ and the fundamental may be estimated by $|F| \cdot \sin(\theta + \phi)$. A packet of data containing the phase $(\theta + \phi)$, the frequency f and an accurate timestamp (e.g. from a Global Positioning system) can be passed to distant protection/control systems. Upon receipt, the phase data can be compared to other similar data accurately, accounting for variable latencies in the communications channels.

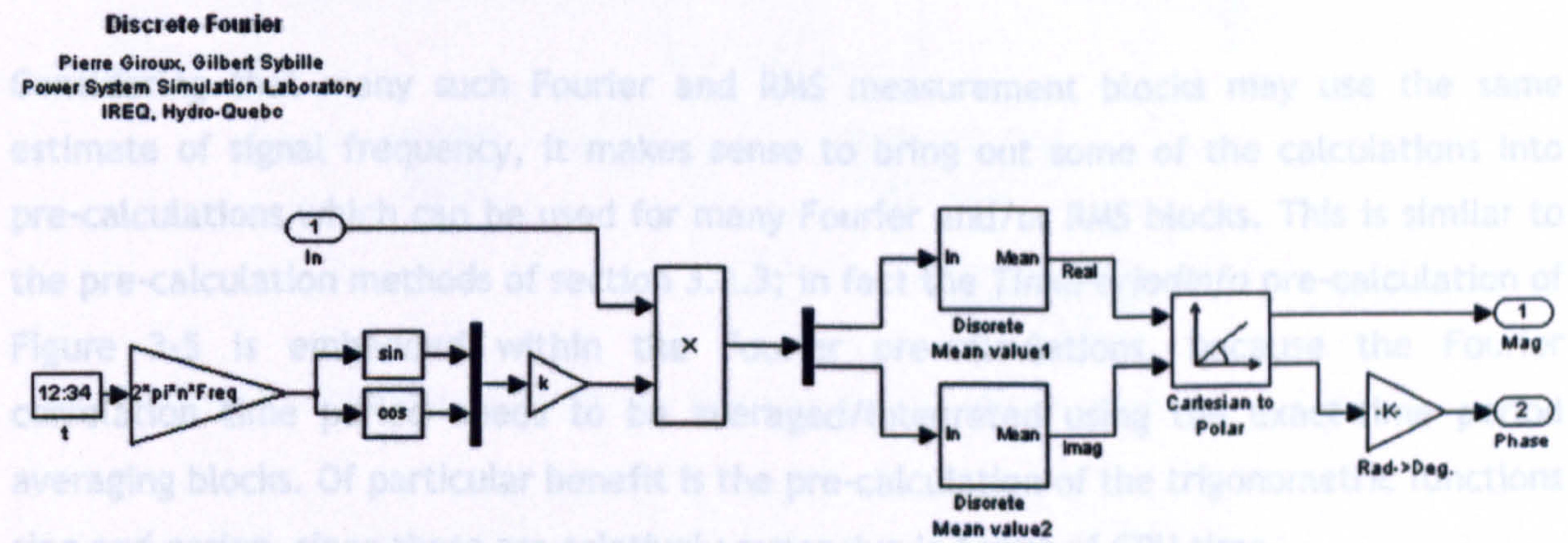


Figure 3-37 : SimPowerSystems "Discrete Fourier" block

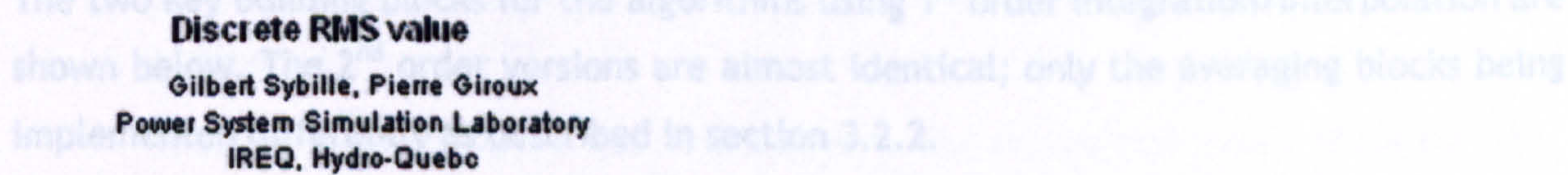


Figure 3-38 : SimPowerSystems "Discrete RMS value" block

3.6 Development of simplest Fourier and RMS amplitude measurement block (1st and 2nd order integration & interpolation)

The obvious improvement to these blocks is to make the parameter *frequency* a dynamic input rather than one that has to be fixed at compile-time. Due to work in the previous sections, this can now easily be done by substituting the new exact-time averaging/integration blocks developed in section 3.2. These new blocks not only allow dynamic setting of the *frequency* parameter, but also add the computational robustness required for real-time safety-critical deployment (which is not present in the existing SimPowerSystems blocks).

Considering that many such Fourier and RMS measurement blocks may use the same estimate of signal frequency, it makes sense to bring out some of the calculations into pre-calculations which can be used for many Fourier and/or RMS blocks. This is similar to the pre-calculation methods of section 3.2.3; in fact the *TimePeriodInfo* pre-calculation of Figure 3-5 is embedded within the Fourier pre-calculations, because the Fourier correlation time period needs to be averaged/integrated using the exact-time period averaging blocks. Of particular benefit is the pre-calculation of the trigonometric functions sine and cosine, since these are relatively expensive in terms of CPU time.

The two key building blocks for the algorithms using 1st order integration/interpolation are shown below. The 2nd order versions are almost identical; only the averaging blocks being implemented differently as described in section 3.2.2.

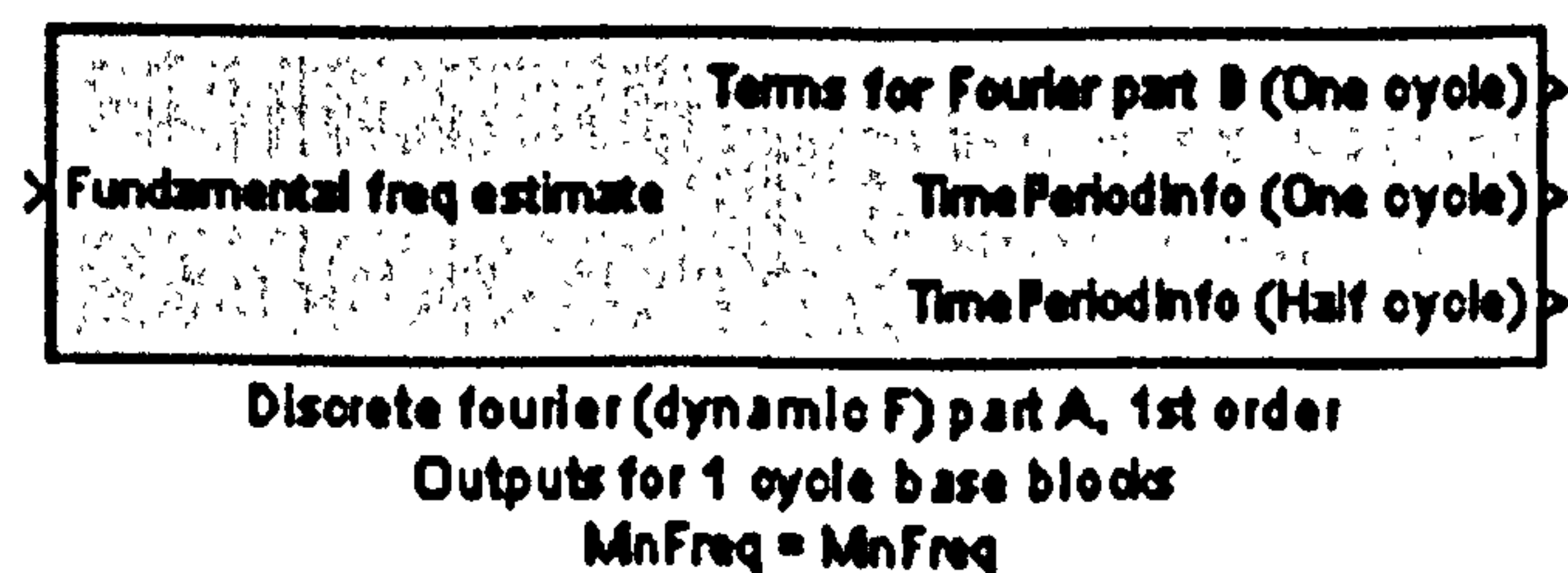


Figure 3-39 : Pre-calculations (part A) for Fourier analysis block (overview)

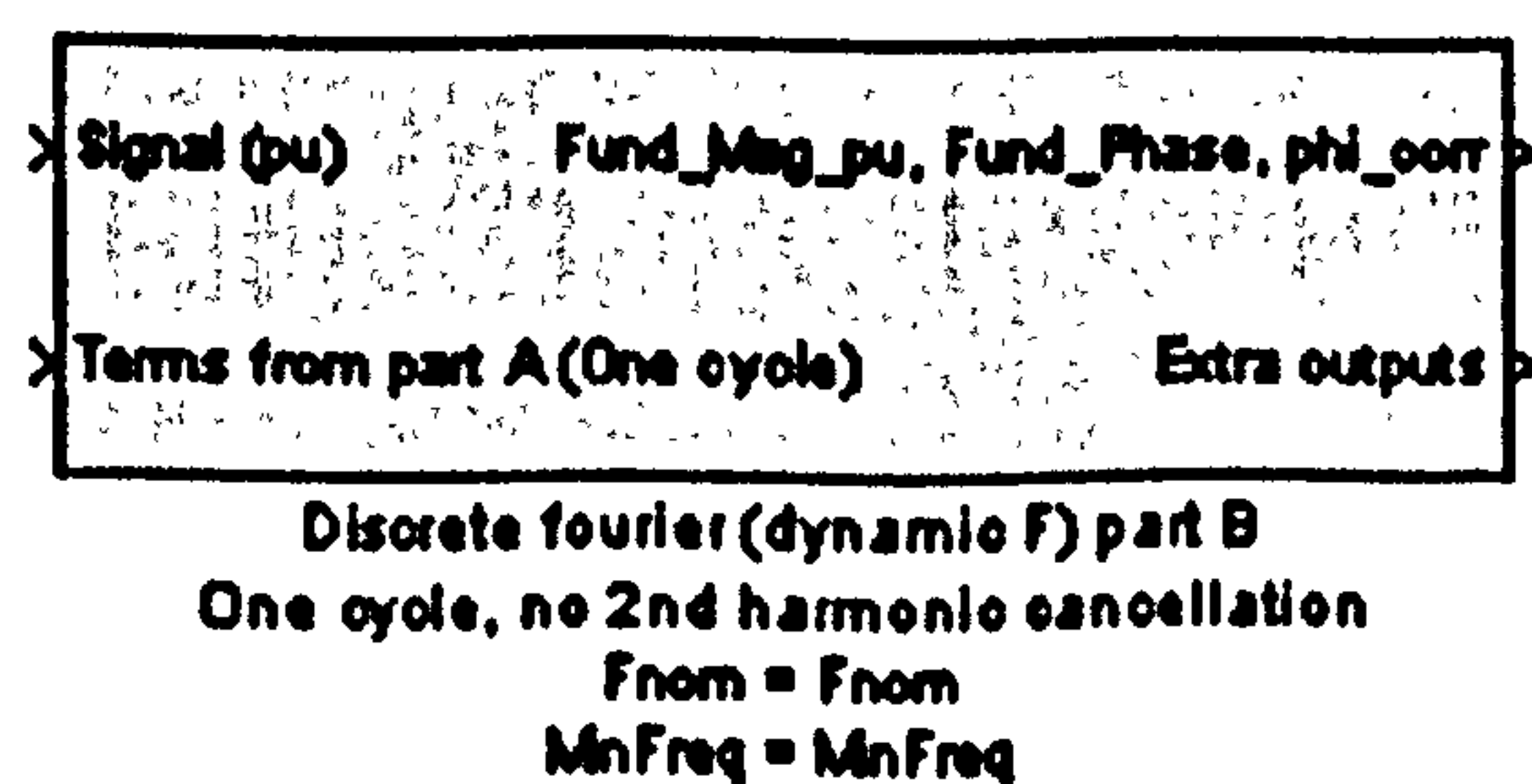


Figure 3-40 : Simplest Fourier analysis block (part B) (overview)

Inside the pre-calculation block (part A), there are no surprises. The reader may for now ignore the “half-cycle” output, which is described in later sections.

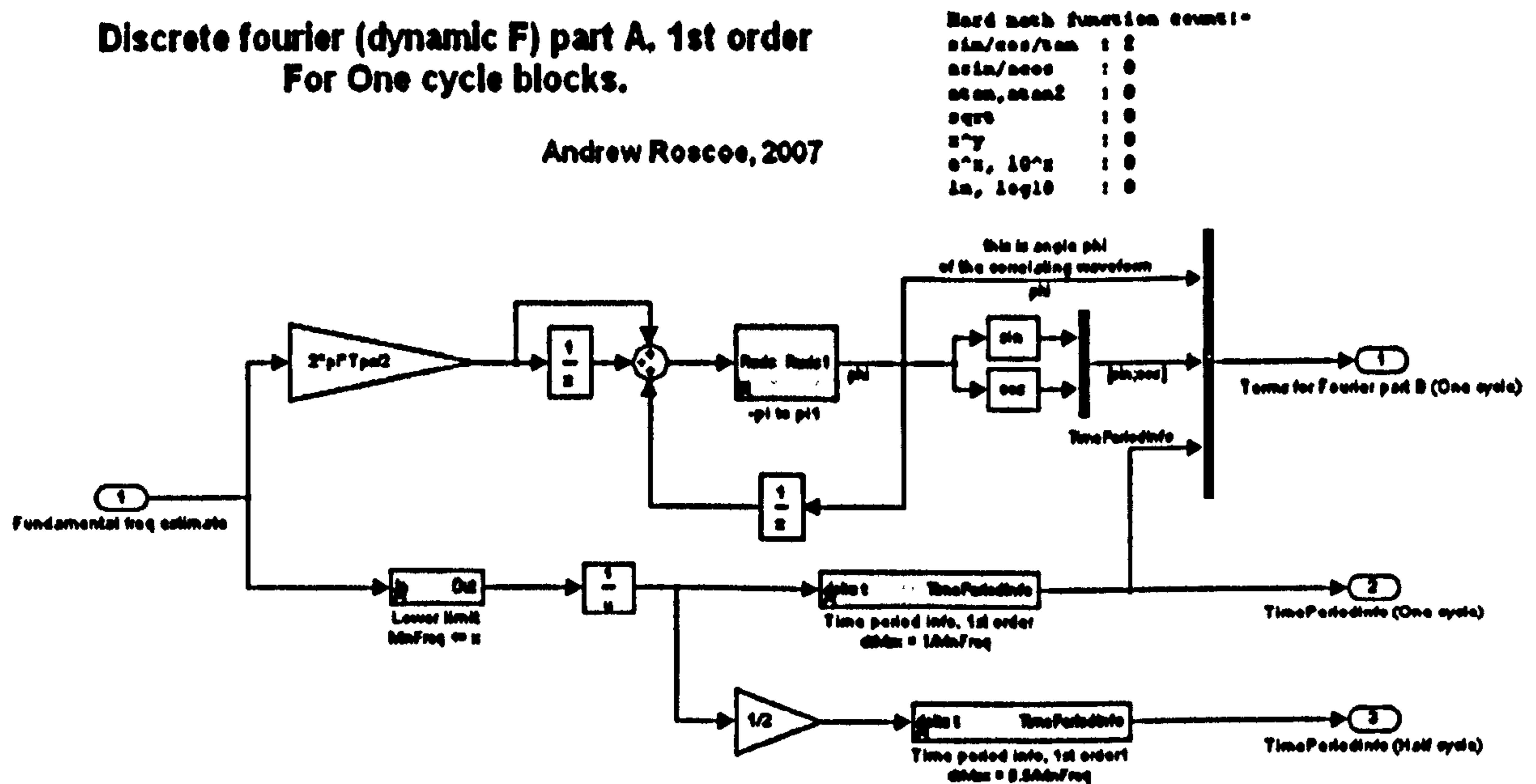


Figure 3-41 : Pre-calculations (part A) for Fourier analysis block (detail)

Similarly, inside the Fourier calculation of Figure 3-42, (here called “part B”), the core code is familiar and closely resembles Figure 3-37. The differences are:-

- The averaging blocks are replaced by the better, newly developed blocks (see section 3.2).
- There are references to “no cancellation”. The reader can ignore these for now, as they discriminate this algorithm from a more complex algorithm explored in section 3.8.
- There is code which detects rapid changes of amplitude. This is done by using a two-sample differentiator block. This is done so as to give a fast warning of transient conditions.
- There are several additional outputs from the block, such as the transient detection etc. These are used for debug purposes, algorithms using 2nd harmonic cancellation (see section 3.8), and also frequency measurement algorithms (see section 5.4.2).
- The meaning of the “phase” output is clarified. Unmodified, this output gives the phase of the measured signal, relative to the phase of the pre-calculated sine/cosine correlation waveforms in the “part A” pre-calculated data. Thus, the phase outputs of any similar Fourier blocks using the same “part A” data can be

compared directly together in a relative manner. Also, if the phase output *Fund_phase_rel_phi_corr* is added to the correlation waveform phase *phi_corr*, then Φ_{abs} , the absolute phase of the input signal relative to a positive-going zero crossing, is determined. This value can be used to recreate an estimate of the signal fundamental via $\sin(\Phi_{abs})$ times the measured amplitude. Φ_{abs} can also be extremely useful to pass between remote systems to compare phases between AC waveforms at different locations on a network, being measured by different instrumentation systems which have unsynchronised CPU clocking crystals. This information must, however, be qualified by an accurate timestamp (from the GPS system, for instance) and also the estimate of frequency. In this way, communication delays can be backed out of the data to enable an exact comparison of relative phases to be made.

Discrete Fourier analysis, with a single cycle base

Andrew Roscoe, 2007

Hard math function count:-
 sin/cos/tan : 0
 asin/acos : 0
 atan,atan2 : 1 (Cart to polar)
 sqrt : 1 (Cart to polar)
 x^y : 0
 e^x, 10^x : 0
 ln, log10 : 0

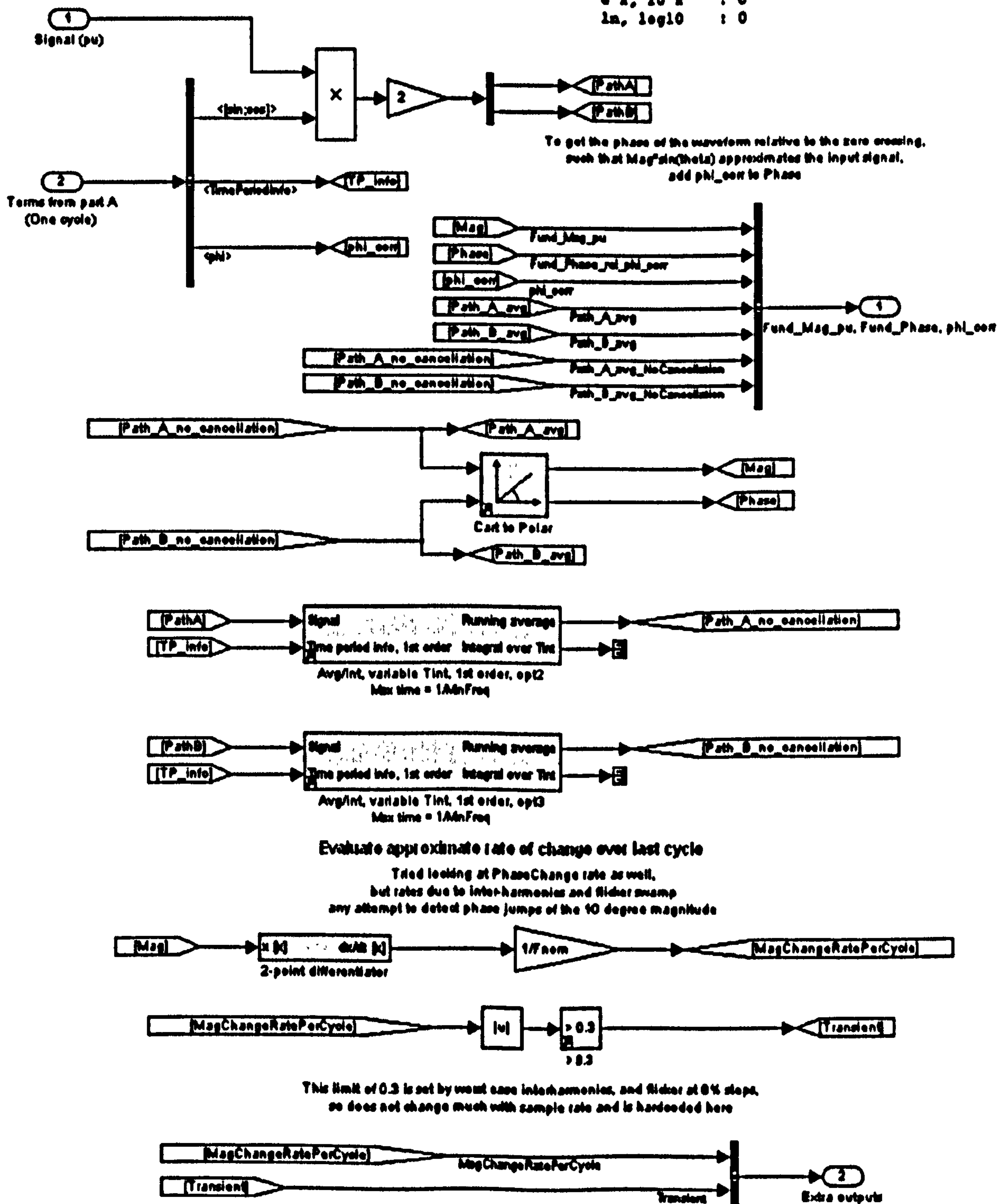


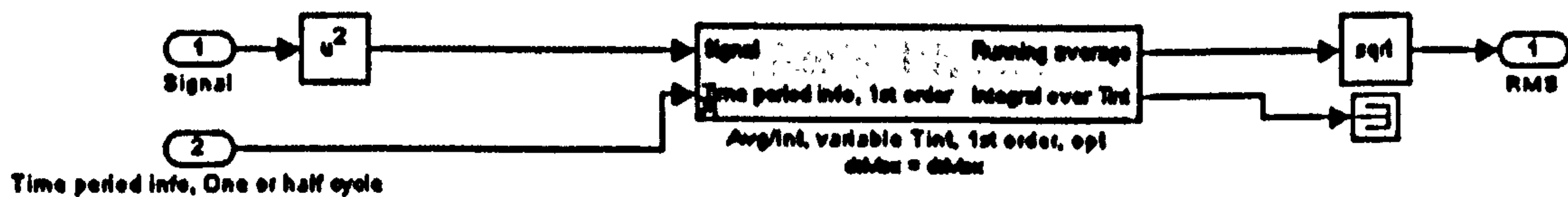
Figure 3-42 - Fourier analysis, "part B", detail

The fundamental magnitudes measured by the Fourier block of Figure 3-42 are output as peak amplitude values. These can be converted to RMS amplitude values by dividing by $\sqrt{2}$.

The all-harmonic RMS measurement block, by comparison, is much simpler. It is identical to the original SimPowerSystems block of Figure 3-38, except that the new averaging algorithms are substituted, using either 1st or 2nd order integration/interpolation.

RMS over an exact, variable time period, using 1st order interpolation for the part-sample periods

Andrew Roscoe, 2007



```

Hard math function count:-
sin/cos/tan      : 0
asin/acos       : 0
atan,atan2      : 0
sqrt            : 1
x^y            : 0
e^x, 10^x      : 0
ln, log10      : 0

```

Figure 3-43 : All-harmonic RMS calculation evaluation

The algorithm evaluates the expression

$$RMS = \sqrt{\frac{1}{T} \int_{t_0-T}^{t_0} y^2(t) \cdot dt} \quad (3.7)$$

where t_0 is "now" and T is the integration time ($1/f$ for a single-cycle measurement).

THD can be calculated from the RMS amplitude of the fundamental (V_1) and the all-harmonic RMS amplitude V_{All} , by the following relationship

$$THD(\%) = 100 \times \frac{\sqrt{V_{All}^2 - V_1^2}}{V_1} \quad (3.8)$$

where the RMS amplitude of the harmonic content V_h (everything except the fundamental, i.e. DC bias plus 2nd, 3rd, 4th, and all higher harmonics) is

$$V_h = \sqrt{V_{All}^2 - V_1^2} \quad (3.9)$$

In cases where the input waveform has already been passed through a DC blocking stage, the measurement of V_{All} , THD, and V_h will not include the DC bias (0th harmonic).

3.7 Amplitude measurement errors due to integration and interpolation at low sample rates, using pure sinusoid inputs

The 1st and 2nd order algorithms described in section 3.6 produce perfect results if the input is a perfect sinusoid at nominal frequency, so that the number of samples per cycle is an integer number. This is true even when the samples do not fall at the zero crossings, as the interpolation errors at the beginning and end of each measurement timeframe cancel each other out. However, when the actual frequency does not result in a period which equals an integer number of sample times, the measurements exhibit integration/interpolation errors which show up as ripples. The worst input frequencies have been found to be those which result in $N \pm \frac{1}{2}$ samples per cycle, where N is an integer. For example, with nominal settings of F_{nom} Hz and N samples per cycle, the worst expected input frequencies can be calculated by

$$F_{worst} = \frac{F_{nom} N}{\left(N \pm \frac{m}{2}\right)} \text{ where } m \text{ is any sensible odd integer to give a positive frequency} \quad (3.10)$$

So, for 50 Hz and 10 samples per cycle, the worst frequencies closest to 50 Hz would be 47.619 and 52.632 Hz (10.5 and 9.5 samples per cycle). At these frequencies, it does not matter what the phase of the incoming signal is relative to the sampling points, the ripple errors are always of the same magnitude. For example, the start (zero crossing) of a cycle at 52.626Hz may fall exactly on a sample point. In this case the end (next zero crossing) of the cycle will fall exactly between two sample points, resulting in an interpolation error. Conversely, if the start (zero crossing) of a cycle at 52.626Hz falls exactly between two sample points, then the end (next zero crossing) of the cycle will fall exactly on a sample point. This results in the same interpolation error. Phases in between these two examples result in the same interpolation error magnitude.

However, due to the effects of lowering the number of samples per cycle at higher frequencies, the interpolation error amplitude will be larger at, say, 52.632 Hz than 47.619 Hz, simply because there are less samples per cycle at 52.632 Hz and the interpolation takes place over longer timeframes. Thus, the actual performance vs. frequency will be a combination of the predictions of equation (3.10), plus a tendency for ever higher errors at ever higher input frequencies (and in the presence of higher-order harmonics).

To evaluate the actual measurement errors of the single-cycle Fourier measurement blocks due to integration and interpolation, a Simulink model was created. This is a multi-rate simulation designed to test all aspects of the algorithms described above, by synthesising input waveforms at desired sample frequencies with variable amounts of Gaussian noise and harmonic distortion. Allowance is also made to simulate the effects of analogue and digital filtering, before and after the ADC stage, plus the effects of ADC discretisation. These effects are all described in section 3.4.

This model can be executed repeatedly from a pair of MATLAB scripts which first run multiple instances of the simulation across a wide range of scenarios to create a data file, and then plot the results. Using this setup, the graph below shows the maximum interpolation errors against input frequency, when using 10 samples per cycle (50 Hz nominal frequency, 500 Sa/s) and inputs of pure sinusoids between 45 and 55 Hz. In this set of simulations, the anti-alias filter response, Gaussian noise, ADC quantisation effects and DC bias/block are not modelled so as to focus purely on the algorithm integration/interpolation error. The Simulink model uses the Fourier blocks from section 3.6 (both 1st and 2nd order versions), correlating the input waveform over exactly one cycle. The results are shown in Figure 3-44.

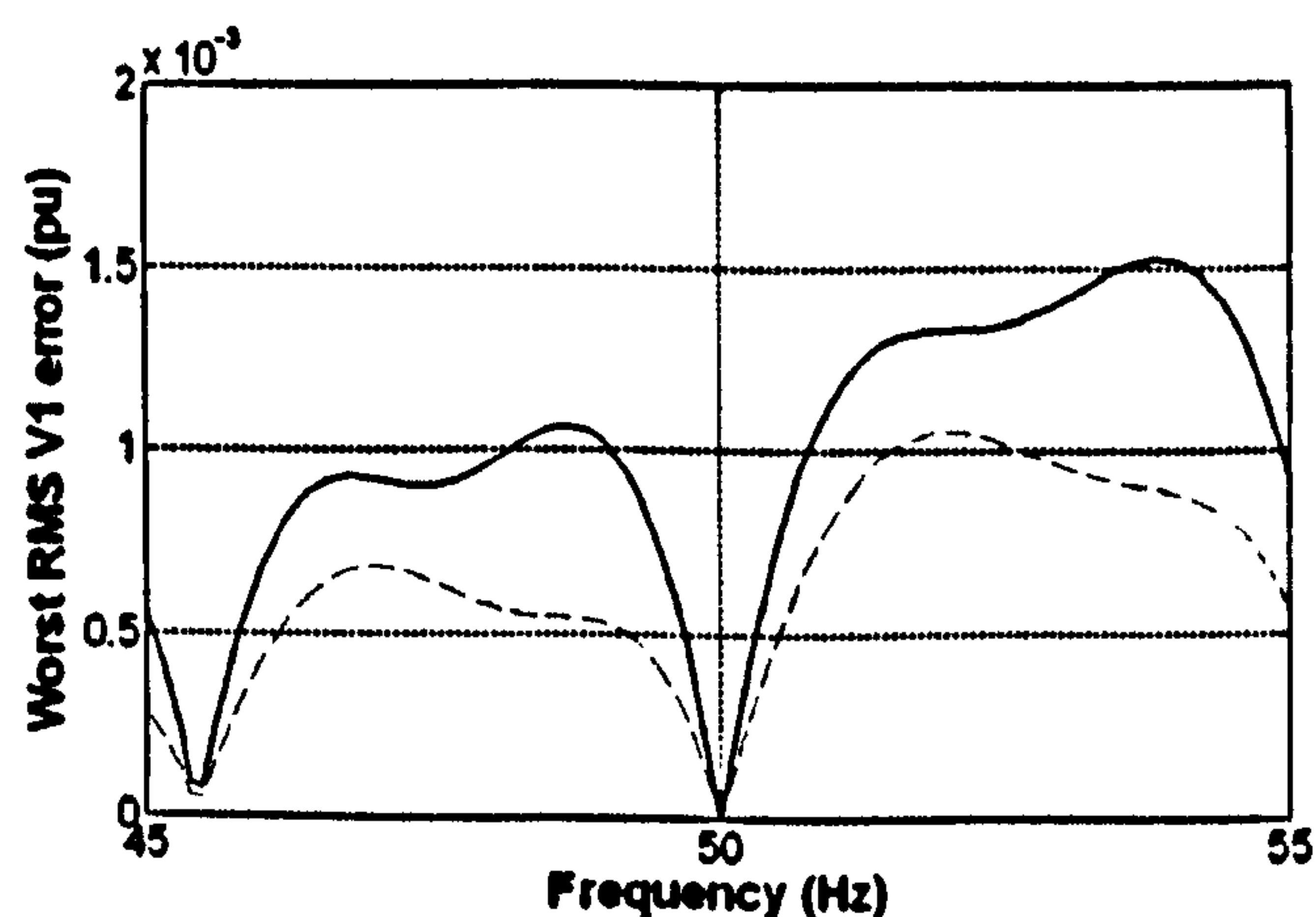


Figure 3-44 : Fourier analysis of fundamental. RMS errors due to integration & interpolation @ 10 Sa/cycle. 1st order (solid) and 2nd order (red dashes) methods.

The error magnitudes shown in Figure 3-44 (and following) plots are the RMS of the instantaneous ripple error values, with the mean of the “root mean squared” evaluated over one cycle.

Note that the 2nd order methods reduce the errors compared to the 1st order methods, but that the improvement is no better than a factor of 2 at any point.

It is important to note that in this, and all other simulations in this chapter, it is assumed that the signal frequency is known. Thus, most error analyses shown in this chapter do not account for errors in the frequency measurement. Of course, if the frequency is not known then additional errors will be present. This error will be largest when a “dead” power system is initially connected via a breaker to a “live” power system. In this case, several cycles may elapse before the frequency measurement is accurate. During this time the amplitude and phase measurements will also be in error. These errors are examined in section 4.1. During brief voltage dips, the amplitude/phase measurement error can be minimised by implementing “ride-through” capability into the frequency measurement algorithm. This is specified in section 2.7.5 and implemented in section 5.4.2.

Exploring a range values of samples-per-cycle from 10 to 30, and finding the worst case errors obtained for any input frequency between 45 and 55 Hz results in Figure 3-45. Note that as the number of samples per cycle increases, the frequencies at which the errors peak occur get closer to 50Hz (and hence more likely to be observed), but that the magnitude of the errors decreases (compare Figure 3-44 and Figure 3-48).

It was anticipated that the benefit of the 2nd order methods would decrease as the number of samples per cycle was increased, even for a pure sinusoidal input. However, this proves not to be the case, on a proportionate basis. Upon further examination, it has been found that the 2nd order methods do not work at their best at the low sample rates near 10 Sa/cycle. This is because the integrations within the Fourier and all-harmonic RMS blocks end up integrating \sin^2 or \cos^2 type functions which have a frequency of twice nominal (100 Hz). There are only 5 Sa/cycle in these waveforms, and the 2nd order curve fitting errors are relatively large. The advantage of the 2nd order methods over the 1st order actually increases (proportionately) as the number of samples per cycle increases.

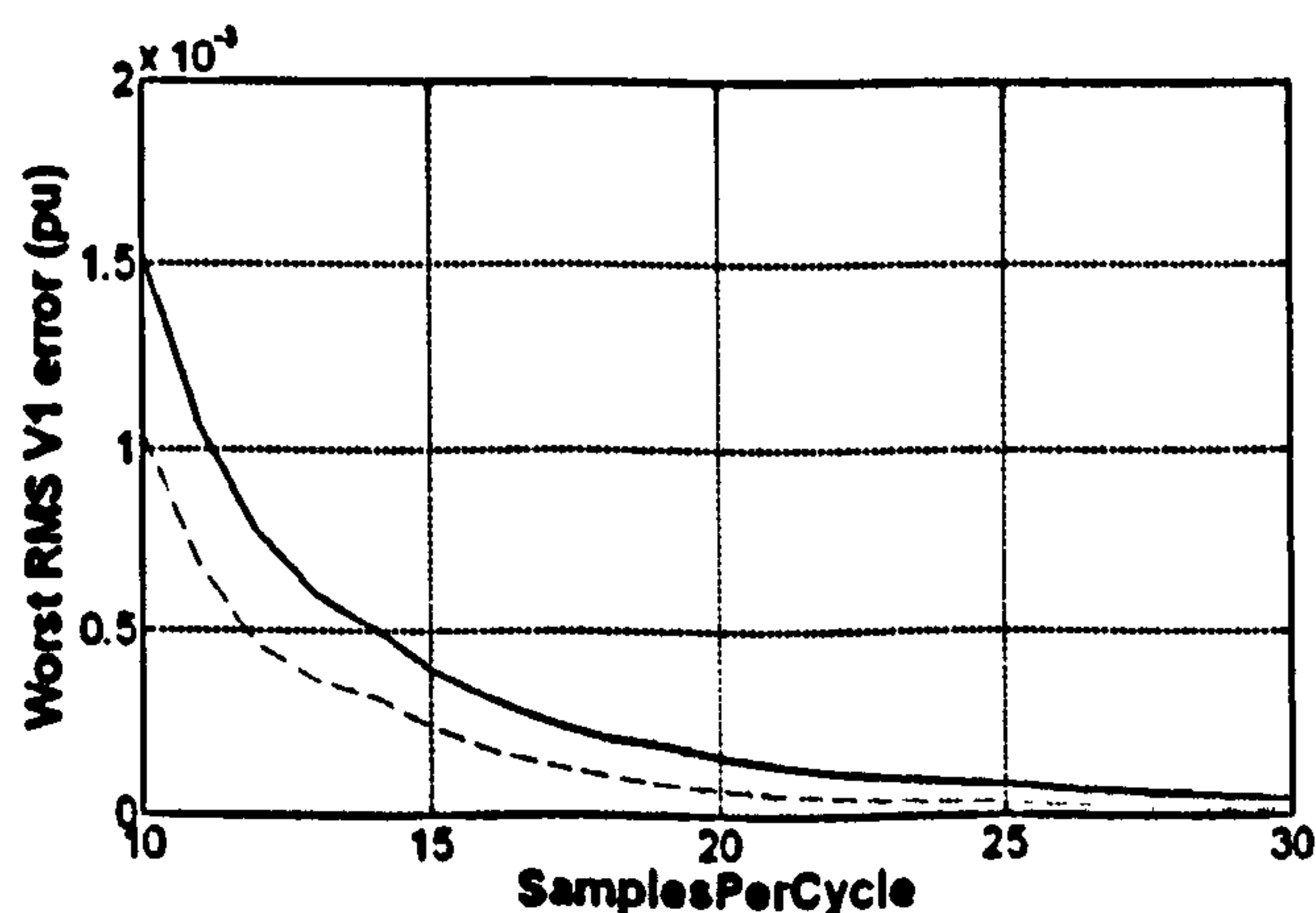


Figure 3-45 : Fourier analysis of fundamental. Largest RMS errors due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods.

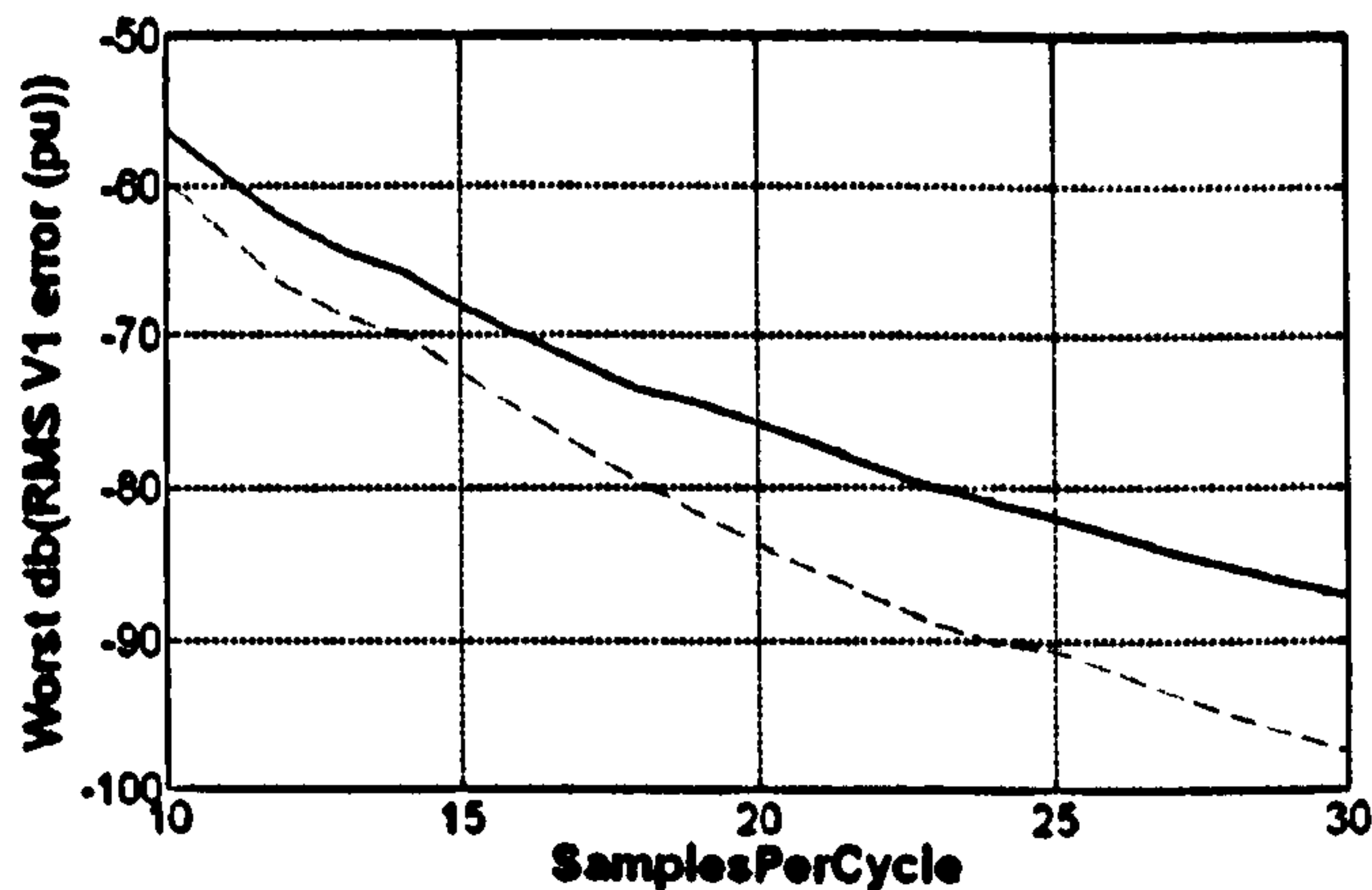


Figure 3-46 : Fourier analysis of fundamental. Largest dB(RMS errors) due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods.

The slope for the 1st order method error is approximately -56dB to -87dB for a 3-fold increase in sample rate. This is a factor of 35x, which means that the error magnitude follows approximately an $N^{-3.2}$ relationship where $3.2 = \ln(35)/\ln(3) = 3.2$. For the 2nd order method, the relationship is approximately $N^{-3.9}$

The ripple frequency of the error is always at twice the input frequency (shown by Figure 3-47). Thus turns out to be an exceptionally useful property and is exploited fully during the rest of this thesis (see sections 3.3.5 & 3.9 for example). The exception, for a pure sinusoid input, is when an integer number of samples spans on cycle period. In this case, the interpolation & integration error is zero and the ripple frequency is also zero (undefined). In the case of Figure 3-47, with 500 Sa/s sampling, this occurs for a 50 Hz input signal.

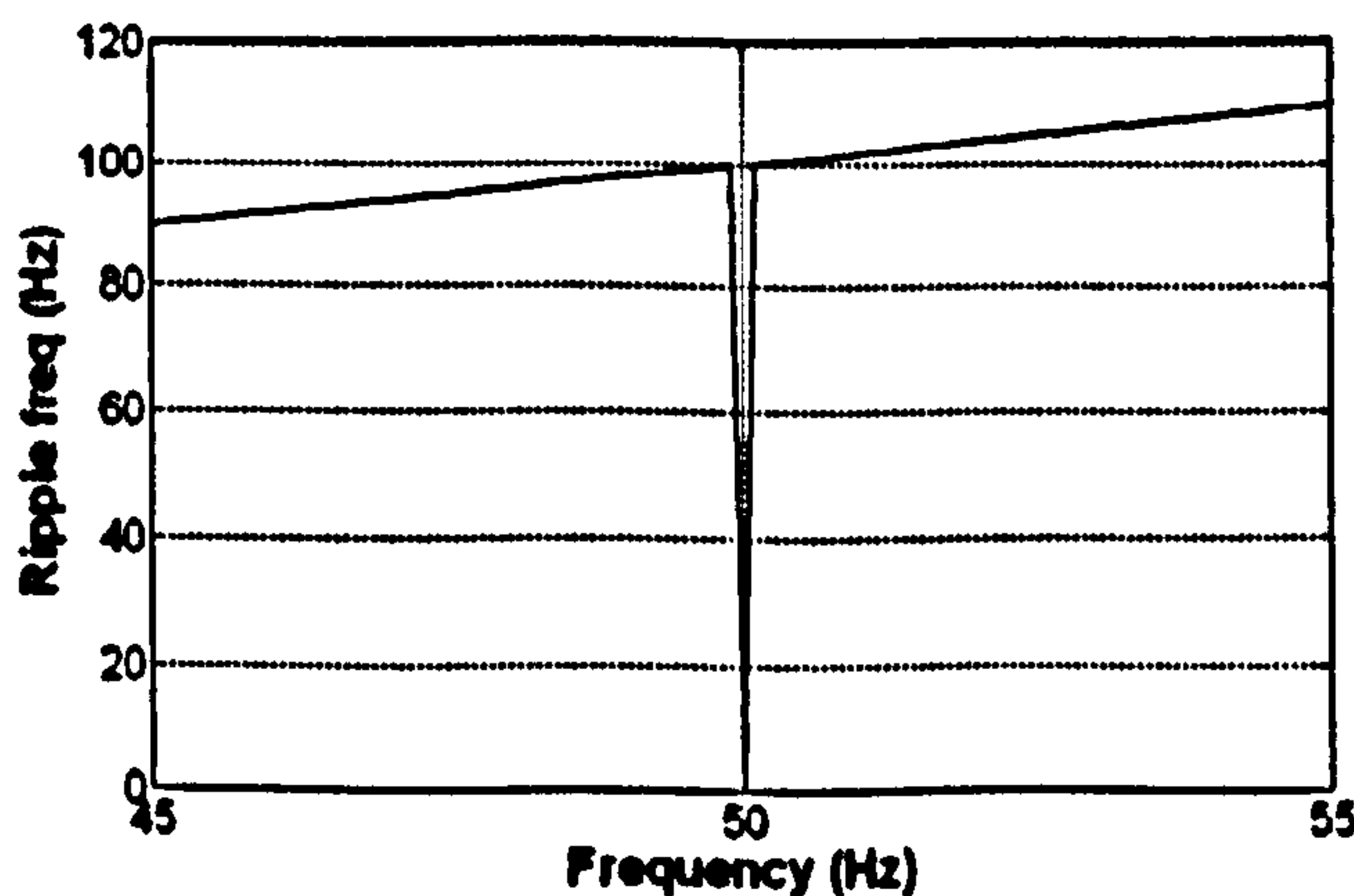


Figure 3-47 : Fourier analysis of fundamental. Ripple frequencies of largest errors due to integration & interpolation over the 45-55Hz range.

To further indicate the reduction of error magnitude and the increasing relative effectiveness of the 2nd order method, Figure 3-48 below shows the analysis technique of

Figure 3-44 repeated, but with sample rate increased from 500 Sa/s (10 samples per cycle) to 1500 Sa/s (30 samples per cycle). The worst error magnitudes for the 1st order method have been reduced from 0.0015 pu to 0.00004 pu, i.e. by a factor of 40. The worst error magnitudes for the 2nd order method have been reduced from 0.001 pu to 0.000012 pu, i.e. by a factor of 80.

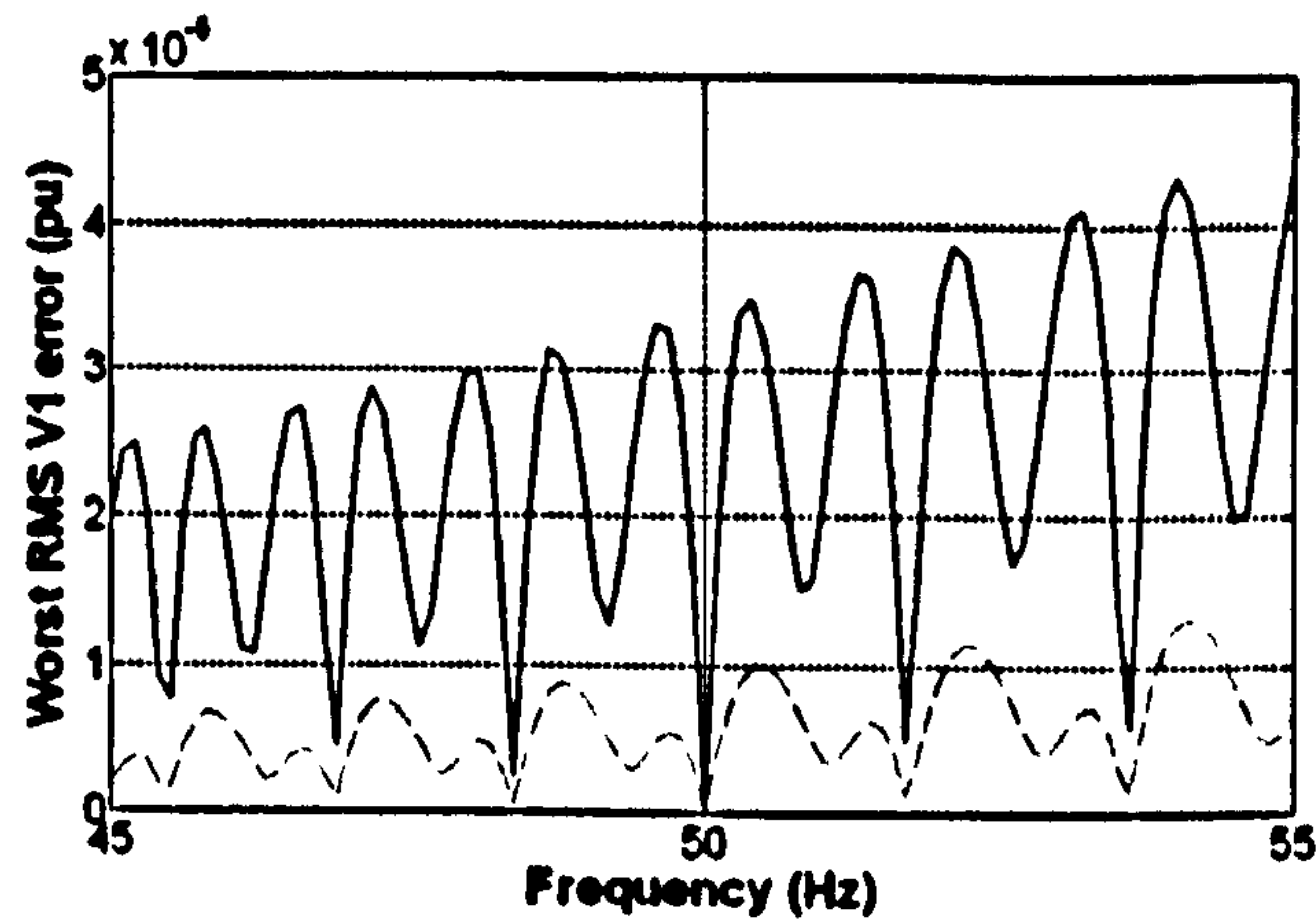


Figure 3-48 : Fourier analysis of fundamental. RMS errors due to integration & interpolation @ 30 Sa/cycle. 1st order (solid) and 2nd order (red dashes) methods.

The reductions in error magnitude versus sample rate for the all-harmonic measurements (and hence THD measurements) behave in a similar fashion to the error magnitudes for the Fourier fundamental measurements, as shown in Figure 3-49 and Figure 3-50.

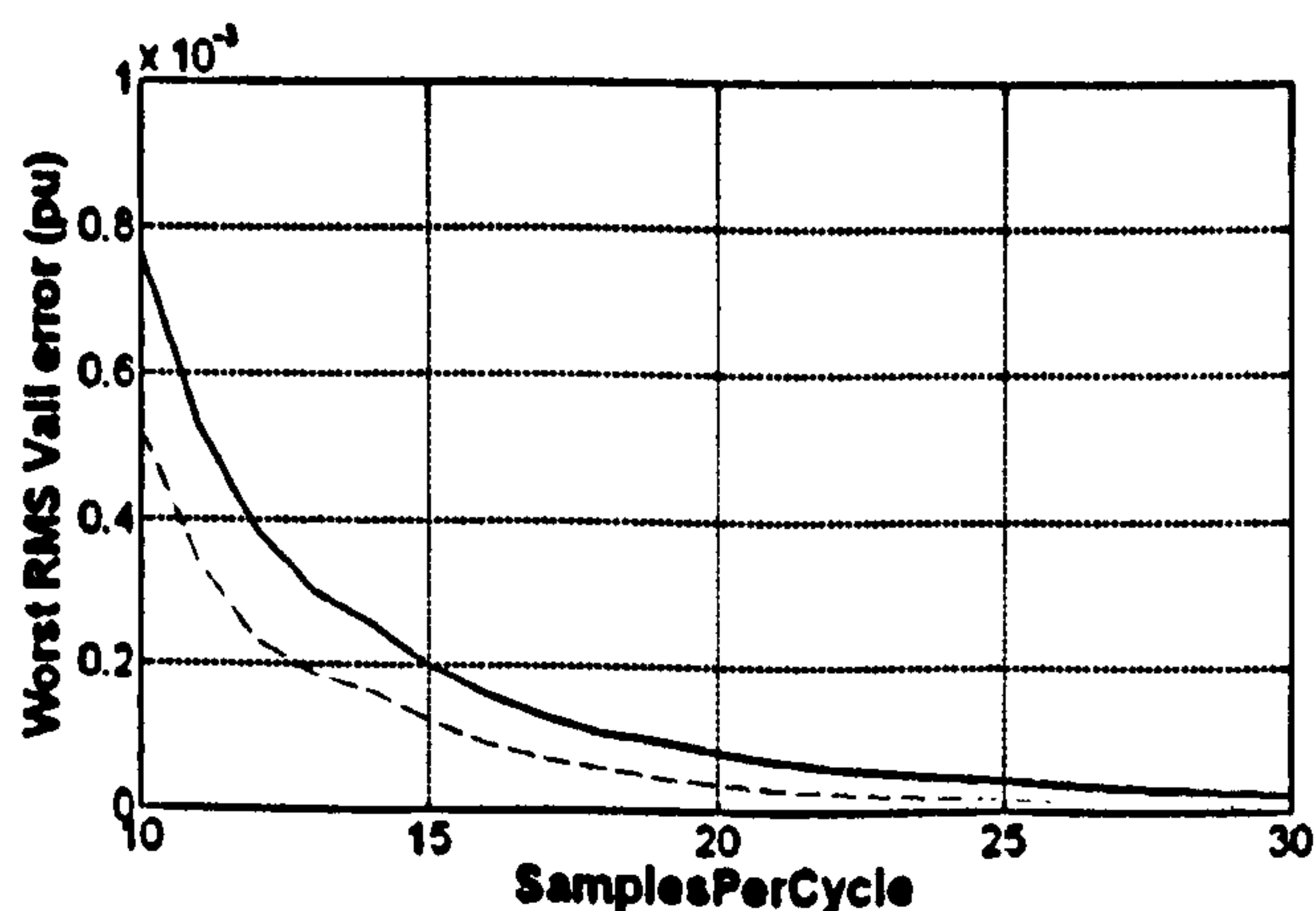


Figure 3-49 : All-harmonic analysis. Largest RMS errors due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods.

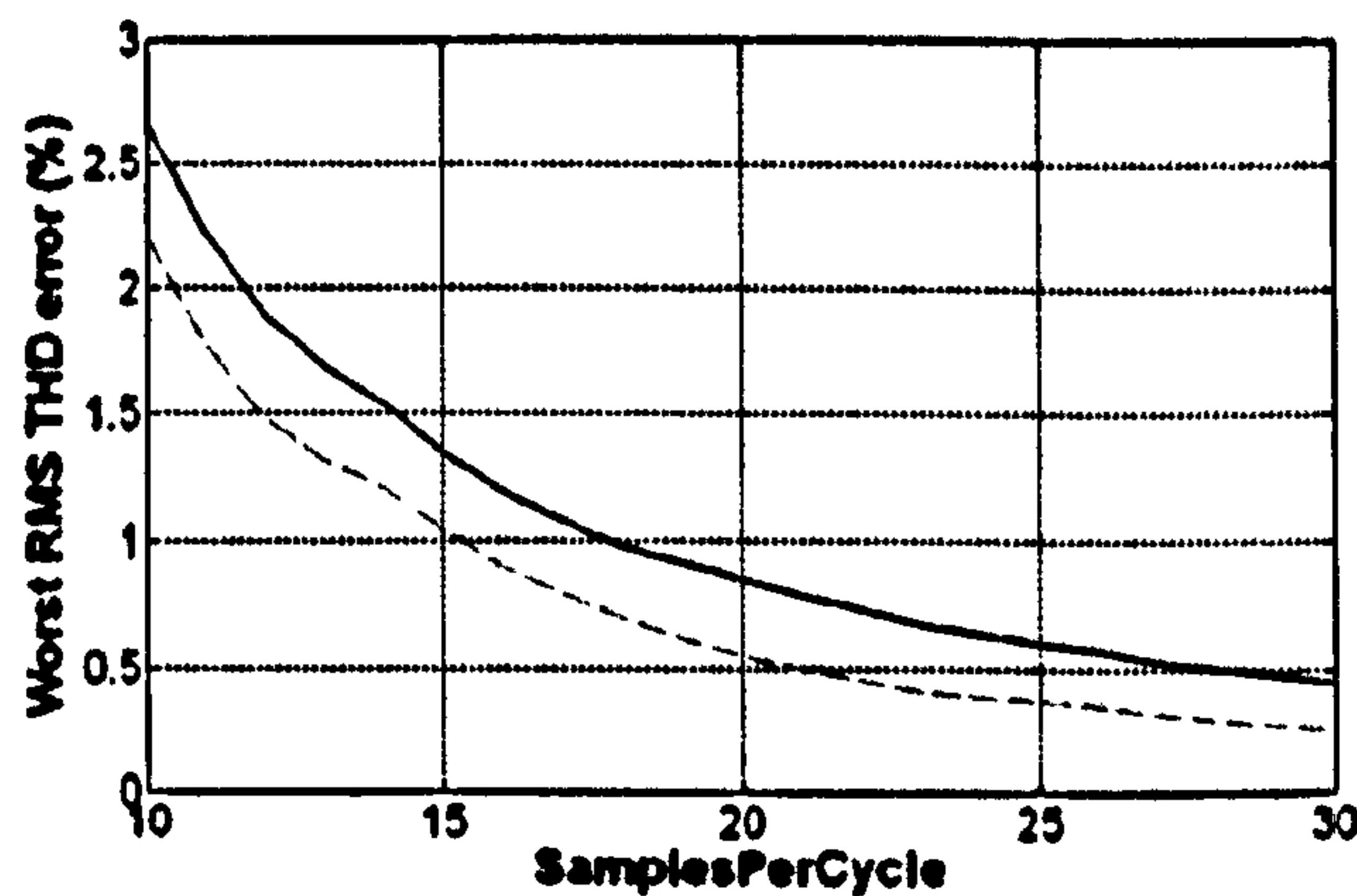


Figure 3-50 : THD analysis. Largest RMS errors due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods.

The THD measurement is extremely susceptible to errors in the measurements of the all-harmonic or fundamental RMS values. THD is calculated in the model above by equation (3.8). The effect of the measurement errors on the THD calculation can be demonstrated by imagining a 0.0001pu error in the estimation of V_{All} . This might produce a THD error of $100 \cdot \sqrt{(1.0001^2 - 1)} / 1 = 1.4\%$. This is a significant error in the THD measurement, considering that the BS EN 50160 specification is for 8% THD. The THD measurements made using the low sample rates in this document should be used as a guide rather than a measure. For an accurate measure of THD, a much higher sample rate needs to be used. In the context of the work in this thesis, this is useful to know but does not present a problem, since the aim is to produce algorithms for protection and control, not for power quality measures. The measurement of THD is thus not of primary concern.

3.7.1 Findings from this section (considering pure sinusoid inputs only)

- The extension to second order reduces the magnitude of the errors. At 10Sa/cycle the errors are reduced to about 66% of the errors from the 1st order methods. At 30Sa/cycle the error reduction improves to 30% of the 1st order methods.
- For any sampling rate of 10Sa/cycle or more, the Fourier and all-harmonic errors due to integration/interpolation using the 2nd order methods are less than 0.002pu. At 16 Sa/cycle, the largest error is about 0.0004pu, although the resulting THD error might still be as high as 1.25%.
- Although the Fourier and all-harmonic RMS errors are very small for pure sinusoid inputs, even at 10Sa/cycle, the 2nd order methods initially appear to be worth using since the THD measurement error is improved significantly from 2.7% to 2.2%. However, it is shown later that second harmonic cancellation can reduce the interpolation errors in the initial single-cycle Fourier correlation by much larger factors (see section 3.8). Also, again shown later, post-averaging stages using

cascaded 1st-order averaging filters can make the advantage of the 2nd order techniques redundant (see section 3.9). Also, the relatively small size of the integration/interpolation errors (for both 1st and 2nd order methods) and the additional error effects due to noise/harmonics (see section 3.13) mean that the 2nd order methods do not add much overall benefit given the additional processing overhead relative to the 1st-order methods.

- Referring to Figure 3-47, it can be observed that the ripple frequencies of the errors from a single-cycle Fourier transformation block, due to integration and interpolation, appear at twice the input frequency. This turns out to be a very useful and predictable property, and is used to good effect in section 3.9 which subsequently forms the basis of excellent measurement algorithms.

3.8 Addition of active 2nd harmonic cancellation

Referring to Figure 3-47, it can be observed that the ripple frequencies of the errors from a single-cycle Fourier transformation block, due to integration and interpolation, appear at twice the input frequency. The reason for this can be explained by referring to Figure 3-42, which shows the Fourier correlation. The correlation is made by taking a reference wave at the supposed frequency f , and then correlating $\sin(2\pi f)$ and $\cos(2\pi f)$ against the actual waveform which, for a pure sinusoid signal, is of the form $V\sin(2\pi f + \Phi)$ where Φ might be any number.

This gives the following correlations

$$\begin{aligned} V \cdot \sin(2\pi f + \phi) \cdot \sin(2\pi f) &= \frac{\cos((2\pi f + \phi) - 2\pi f) - \cos((2\pi f + \phi) + 2\pi f)}{2} = \frac{\cos(\phi) - \cos(4\pi f + \phi)}{2} \\ V \cdot \sin(2\pi f + \phi) \cdot \cos(2\pi f) &= \frac{\sin((2\pi f + \phi) + 2\pi f) + \sin((2\pi f + \phi) - 2\pi f)}{2} = \frac{\sin(4\pi f + \phi) + \sin(\phi)}{2} \end{aligned} \quad (3.11)$$

The correlations therefore have a DC term plus a 2nd harmonic term. Fourier analysis needs to average/integrate these values over (traditionally) a full cycle. Over this timeframe, the second harmonic term disappears if the interpolation errors are small. However, at low sample rates the interpolation within the exact time-frame averaging has to cope with a signal at twice fundamental. For a system working at 10 samples per cycle, the 2nd harmonic has thus only 5 samples per cycle, resulting in the interpolation errors shown on Figure 3-44 and Figure 3-45.

There are two ways of reducing these interpolation errors:-

1. Addition of a stage of passive additional averaging after the initial Fourier correlation. The additional averaging should be over a timeframe of an exact multiple of ½ a cycle, so as to remove the 2nd harmonic interpolation errors, by the processes described in section 3.3.5.
2. The use of an active 2nd harmonic cancellation scheme. The measured values of amplitude and phase (V and Φ in equation (3.11) and Figure 3-42) are fed back into the measurement block. The approximate second harmonic terms due to the fundamental are then generated and subtracted before the Fourier correlation averaging stage. This removes the second harmonic term up front, so the averaging stages average predominantly DC terms, and thus the linear interpolation becomes much more accurate.

The first of these methods (passive cascaded averaging) is analysed later in section 3.9.

The 2nd harmonic cancellation scheme is based upon an algorithm described in a PLL design by Jovcic (2003). This is the only work found to date, aside from the SimPowerSystems blocks, which addresses the problems due to interpolation at low sample rates. Jovcic's scheme only needs to create a single cancelled waveform within the single-phase PLL for phase detection. Applying the 2nd harmonic cancellation to a full Fourier analysis described here requires the technique to be adapted so that both the cancellation terms determined from (3.11) to be applied. To do this, an estimate of the fundamental magnitude and phase must be fed back into the Fourier correlation. This requires additional sine and cosine calculations within each Fourier "part B" block, to be applied to the paths "A" and "B" shown in Figure 3-51. Paths "A" and "B" refer to the two correlation averages; path "A" is the signal times the sine correlation term, while path "B" is the signal times the cosine correlation term. The 2nd harmonic cancellation terms cannot be pre-calculated, so the additional burden on the CPU is significant considering that 3 analyses will be required (6 additional sine/cosine calculations) for each set of 3 phase signals such as V_a , V_b , V_c etc.¹

The procedure for deriving the 2nd harmonic correction terms is as follows:

The signal V_{in} is assumed to be predominantly made up of the fundamental, i.e. $V_{in}=V\sin(\Phi)$ where Φ is of the form $\Phi=2\pi f$ plus an arbitrary phase offset. At any point in time, the input signal V_{in} will be approximately $V_e\sin(\Phi_e)$ where V_e and Φ_e are the estimated magnitude and phase of the input. Care must be taken here because Φ_e must be an absolute phase relative to the positive-going zero crossing, and not simply the phase of the input relative to the correlating coefficients. The correlating Fourier coefficients are $\sin(phi_corr)$ and $\cos(phi_corr)$, where phi_corr is an angle rotating at the estimated frequency of the signal. During the Fourier correlation, path A evaluates as

¹ The 2nd harmonic cancellation in the Jovcic PLL is added in a convoluted manner by synthesising a signal made up of $\sin(50^\circ(\Phi_e+phi_corr))\cos(52^\circ(\Phi_e+phi_corr))$ which gives components at 102°F and 2°F. The 102°F component is then filtered out using a digital low-pass filter. It is not clear why such a method is used, and it does not work at discrete sample rates as the 102°F component aliases back onto other unwanted frequencies. It is much simpler to directly synthesise the cancellation components.

$$Path_A = V \times \sin(phi_corr) \approx V_e \times \sin(\phi_e) \times \sin(phi_corr)$$

$$Path_A \approx \frac{V_e}{2} (\cos(\phi_e - phi_corr) - \cos(\phi_e + phi_corr))$$

(3.12)

which is made up of the desired DC term

$$\frac{V_e}{2} \cos(\phi_e - phi_corr)$$

and the undesired 2nd harmonic AC term

$$-\frac{V_e}{2} \cos(\phi_e + phi_corr)$$

For path A, the correction term is thus the negative, to cancel it out

$$+\frac{V_e}{2} \cos(\phi_e + phi_corr)$$

(3.13)

For path B, the analysis is similar and results in a correction term of

$$-\frac{V_e}{2} \sin(\phi_e + phi_corr)$$

(3.14)

The algorithm for the Fourier analysis with 2nd-harmonic cancellation is shown below in Figure 3-51, which can be compared to the un-cancelled version in Figure 3-42. There are two major additions for the 2nd harmonic cancelled block:-

1. The calculation of the cancellation terms at the 2nd harmonic, and their addition into the path averaging sections "A" and "B". This calculation is shown in Figure 3-52
2. The path averaging sections "A" and "B" are duplicated into two pairs; an un-cancelled pair and a cancelled pair. The reason for this requires significant explanation which follows below.

**Discrete Fourier analysis, with a single cycle base
Uses 2nd harmonic cancellation to minimise ripple at the output**

Andrew Roscoe, 2007

```

Hard math function count:-
sin/cos/atan : 2 (Cancellation)
atan/acos    : 0
atan/asin    : 1 (Cart to polar)
sqrt         : 1 (Cart to polar)
sqrt        : 0
sqrt, 10^n   : 0
ln, log10    : 0
    
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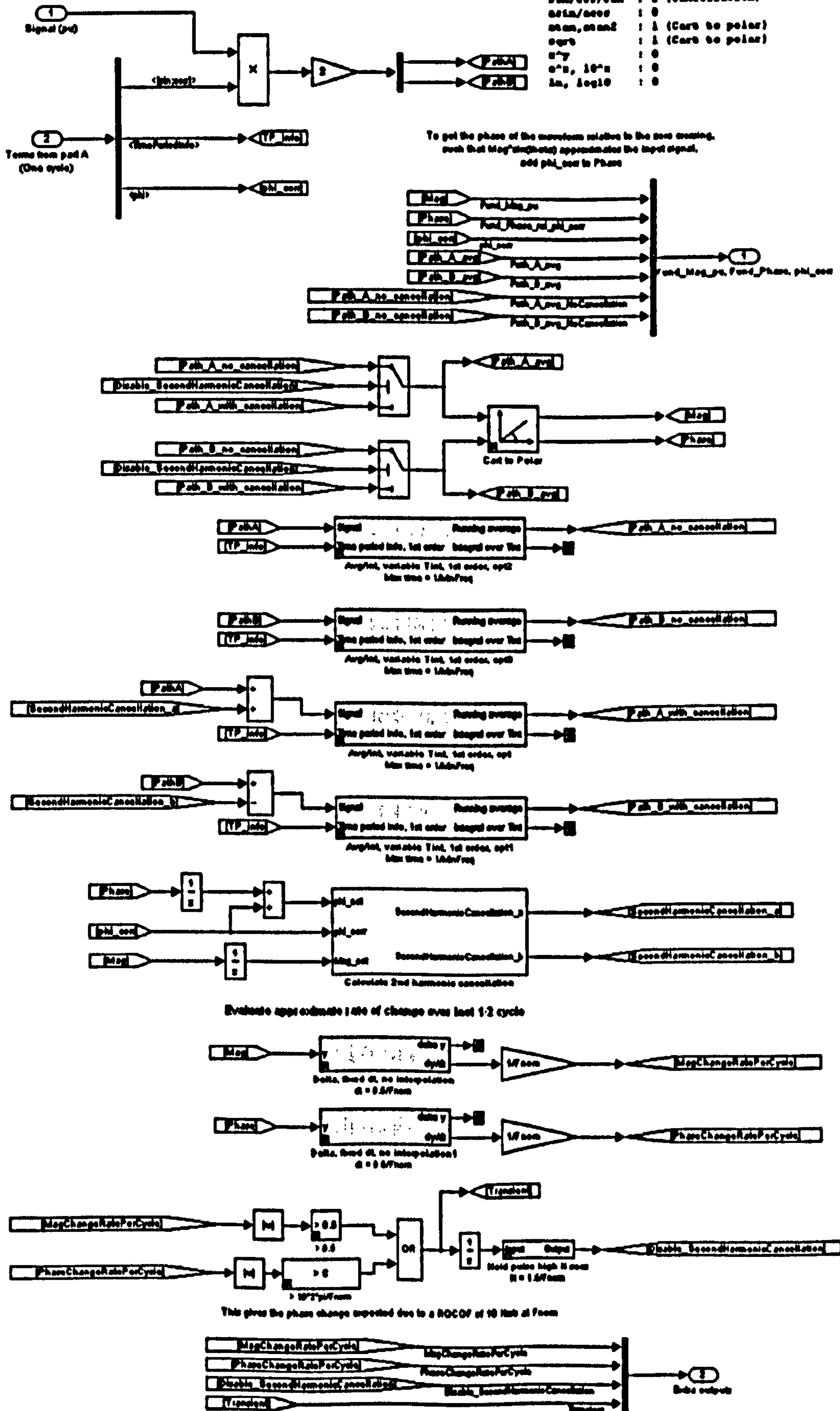


Figure 3-51 : Fourier measurement "part B" with 2nd harmonic cancellation (1st order)

Calculate 2nd harmonic cancellation quantities

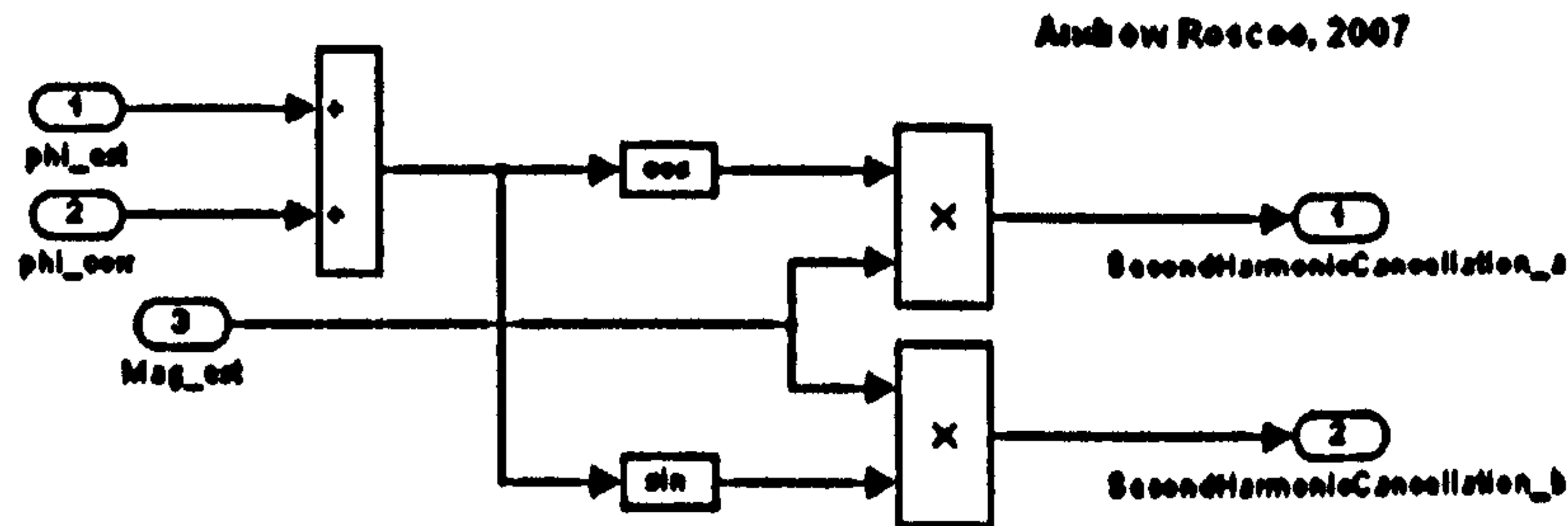


Figure 3-52 : Calculation of 2nd harmonic cancellation terms

As will be shown shortly, the ability of the 2nd harmonic cancellation algorithm to remove ripple due to interpolation of the waveform fundamental, under steady-state conditions, is extremely good. There are two weaknesses, however.

1. The 2nd harmonic cancellation technique only reduces interpolation ripple due to the fundamental signal component, and does not remove interpolation ripple which arises due to higher order harmonic components
2. The 2nd harmonic cancellation involves feeding back of the measured signal amplitude and phase into the algorithm. In this way it has an IIR (infinite impulse) response, and under transient conditions such as sudden signal amplitude change, the magnitude and phase outputs of the algorithm ring and oscillate before eventually settling.

Point 2 can be addressed for transient conditions by using the two pairs of path “A” and “B” integrators, which are shown in Figure 3-51. The idea is that when a transient is detected, the algorithm resorts to an un-cancelled mode of operation. This removes the IIR characteristics and allows the entire algorithm to settle completely within the timeframe of one averaging timeframe (1 cycle in this case). When this is complete, the cancellation mode can be re-engaged. At first glance, it would appear that this can be done with just a single pair of integrators, by feeding them with un-cancelled or cancelled signals as appropriate. However, this results in an undesirable transient in the output due to the sudden change in the inputs to the averaging filters as the second harmonic is added (or taken away). Therefore, to achieve a smooth handover, 2 pairs of integrators are required. One pair is always with-cancellation, and the other without. A mode flag determines which pair of integrators to use.

To illustrate this dynamic behaviour for a sudden increase in signal amplitude, a small Simulink model was created. This applies a 1pu signal at the worst frequency for interpolation errors (52.632Hz), then a short voltage dip to 0.25pu between 0.1 and 0.2

seconds. In this case the front-end low-pass filters, ADC sampling (but not quantisation noise) plus DC block are all modelled accurately, to show the true dynamic response at 500 Sa/s, nominally 10 Sa/cycle at 50 Hz. Several algorithms are compared here:

- The single-cycle, 1st order algorithm without cancellation from section 3.6
- A single-cycle, 1st order algorithm with cancellation always active
- The single-cycle, 1st order algorithm with the automatic cancellation decision algorithm shown in Figure 3-51

The graphs below show the same data, first in broad view and then zoomed in.

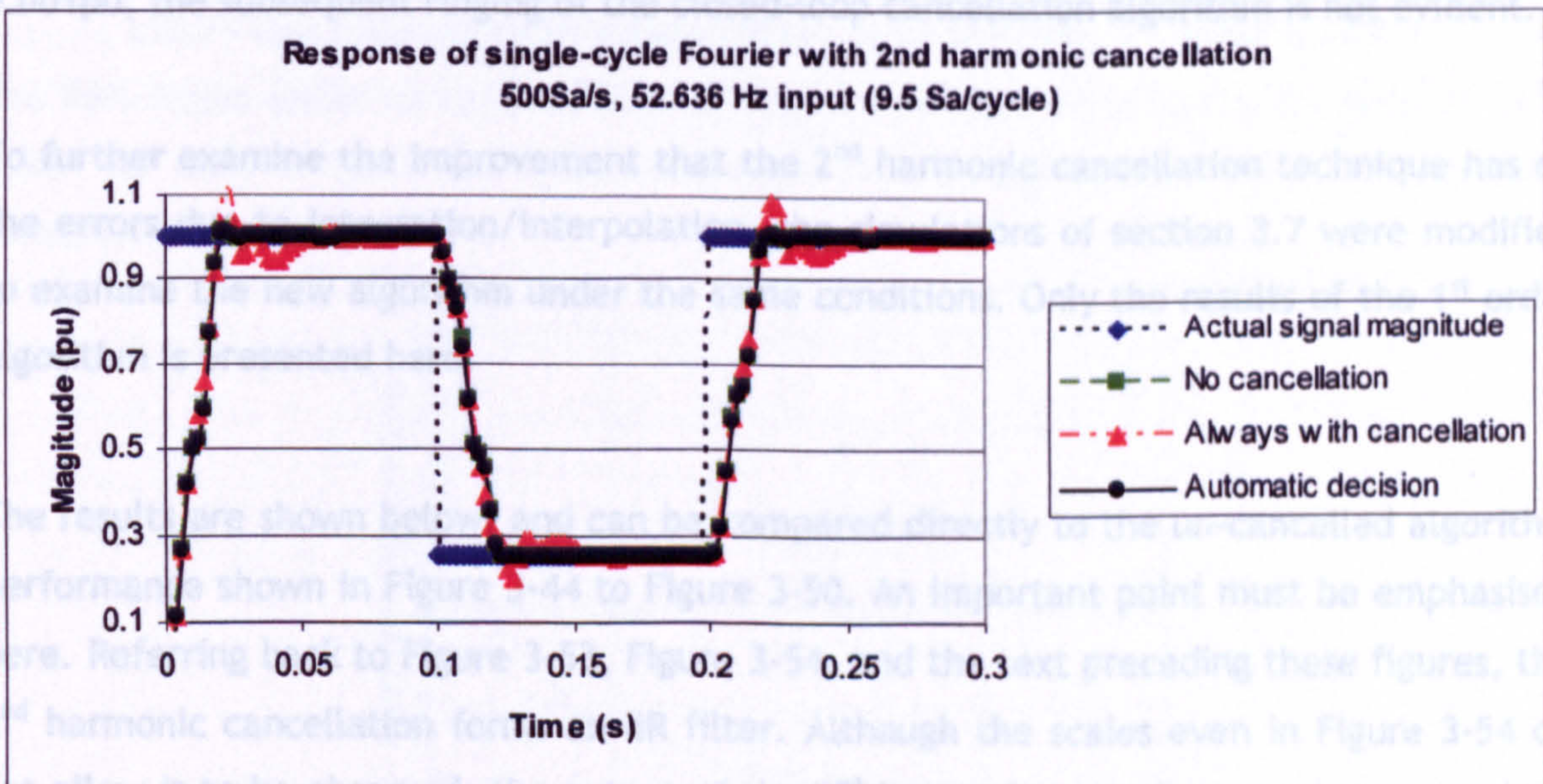


Figure 3-53 : Dynamic response of single-cycle Fourier analyses with 2nd harmonic cancellation

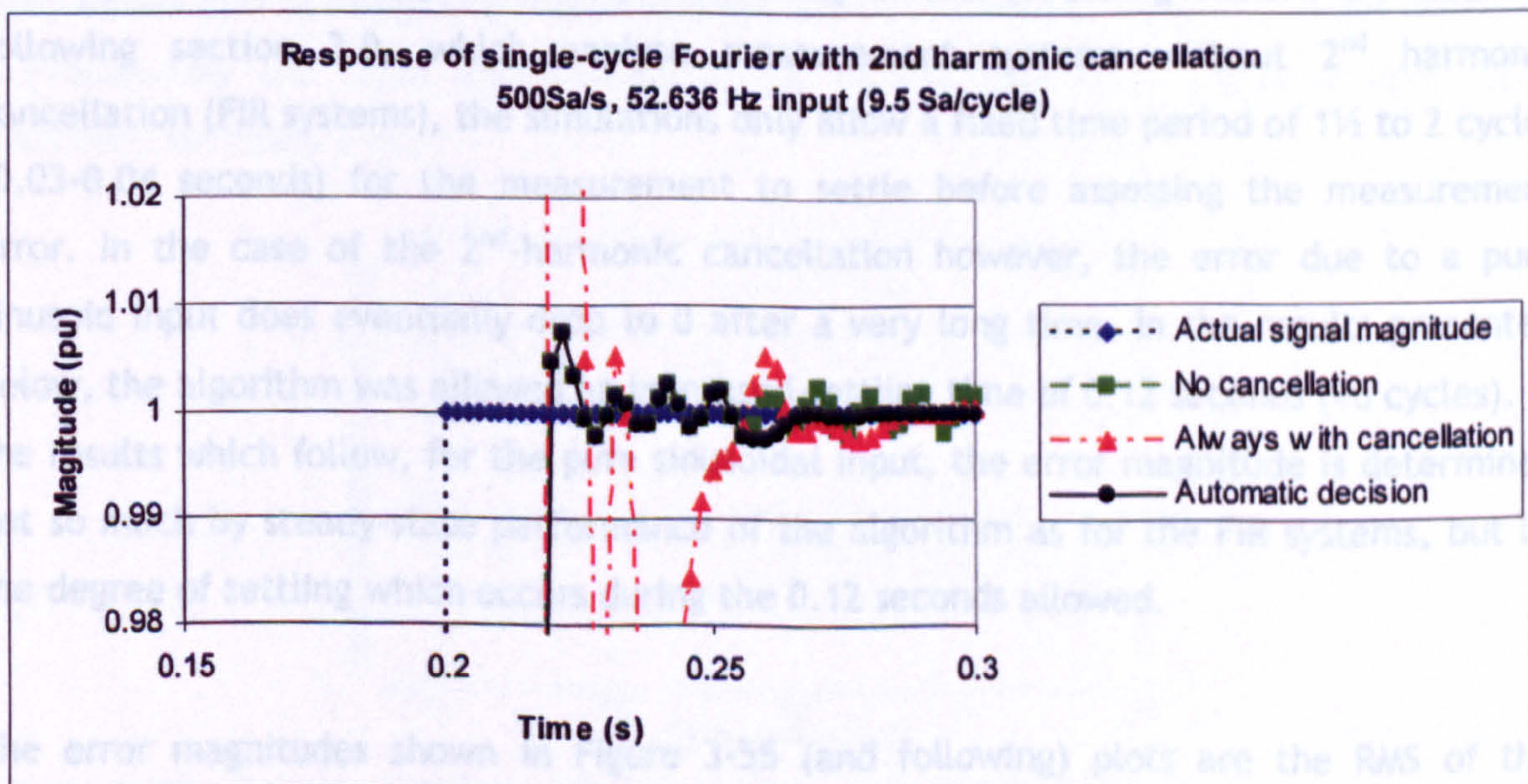


Figure 3-54 : Dynamic response of single-cycle Fourier analyses with 2nd harmonic cancellation, zoomed in.

Clearly, the "Always with cancellation" algorithm shows a poor settling characteristic, with ringing to the 0.01pu error level for 50ms (2.5 cycles) after the transient occurs. The "No cancellation" algorithm shows a much quicker settling to this level, within 20ms. These times include the low-pass filter and sampling delays, as these are modelled here. The "No cancellation" algorithm does, however, continue to exhibit a perpetual error, rippling at the 0.0016pu RMS level, at 2×52.632 Hz, due to the interpolation error. This links to the simulation results in Figure 3-44 , Figure 3-45 and Figure 3-47. The best result is the algorithm with automatic selection of cancelled and non-cancelled path averages. This shares the fast settling of the "No cancellation" algorithm, but once this is settled, it changes over to "Cancelled" operation. Because the output is already settled within about 0.001pu, the subsequent ringing of the closed-loop cancellation algorithm is not evident.

To further examine the improvement that the 2nd harmonic cancellation technique has on the errors due to integration/interpolation, the simulations of section 3.7 were modified to examine the new algorithm under the same conditions. Only the results of the 1st order algorithm is presented here.

The results are shown below, and can be compared directly to the un-cancelled algorithm performance shown in Figure 3-44 to Figure 3-50. An important point must be emphasised here. Referring back to Figure 3-53, Figure 3-54, and the text preceding these figures, the 2nd harmonic cancellation forms an IIR filter. Although the scales even in Figure 3-54 do not allow it to be observed, the output of the 2nd harmonic cancellation scheme continue to ring in a damped fashion for an "infinite" amount of time, even after implementation of the improvements for dynamic response. Thus, in the preceding section 3.7 and the following section 3.9, which analyse measurement systems without 2nd harmonic cancellation (FIR systems), the simulations only allow a fixed time period of 1½ to 2 cycles (0.03-0.04 seconds) for the measurement to settle before assessing the measurement error. In the case of the 2nd-harmonic cancellation however, the error due to a pure sinusoid input does eventually drop to 0 after a very long time. In the results presented below, the algorithm was allowed an increased settling time of 0.12 seconds (=6 cycles). In the results which follow, for the pure sinusoidal input, the error magnitude is determined not so much by steady-state performance of the algorithm as for the FIR systems, but by the degree of settling which occurs during the 0.12 seconds allowed.

The error magnitudes shown in Figure 3-55 (and following) plots are the RMS of the instantaneous ripple error values, with the mean of the "root mean squared" evaluated over one cycle.

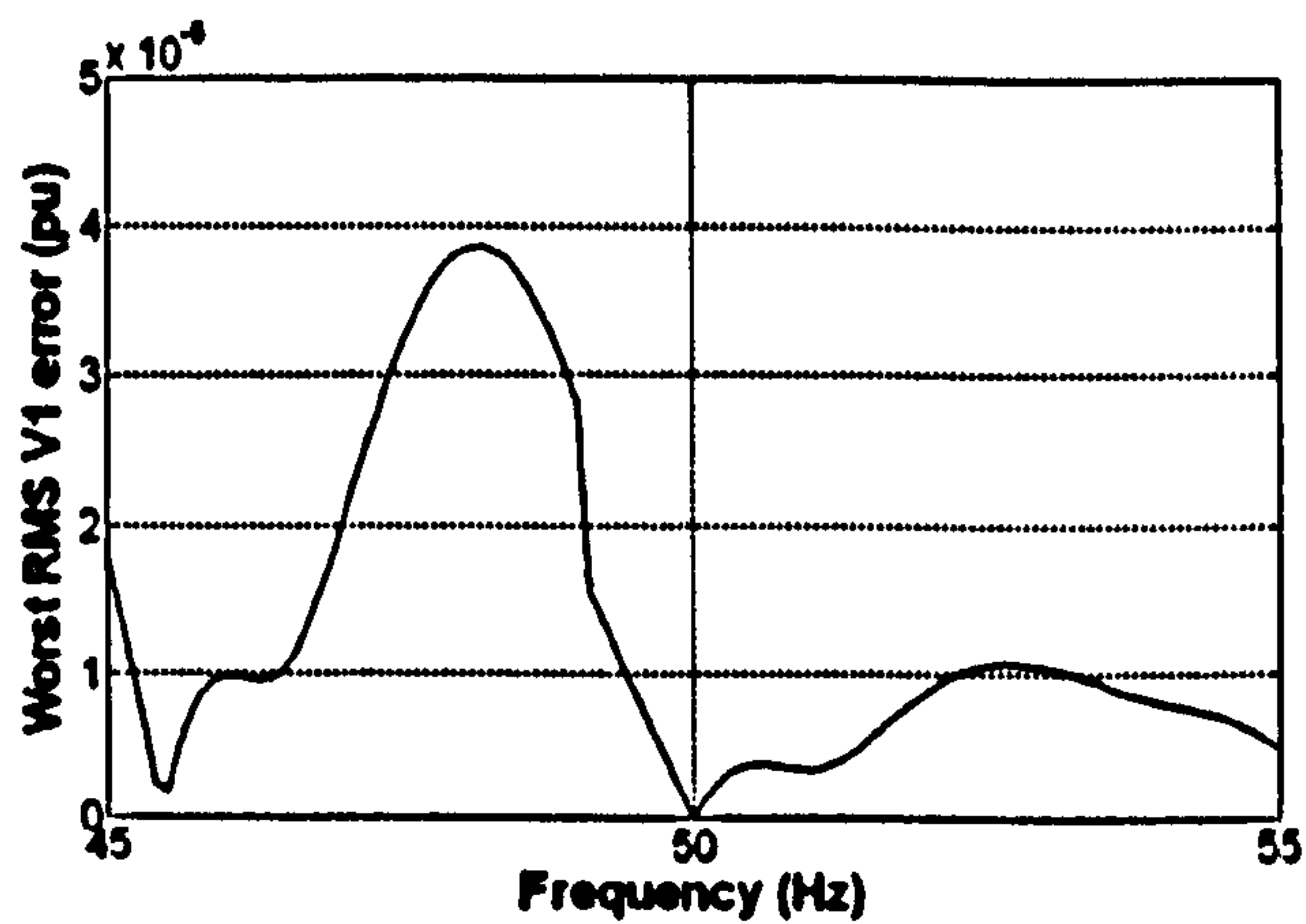


Figure 3-55 : Fourier analysis of fundamental, using 2nd harmonic cancellation. RMS errors due to integration/interpolation @ 10 Sa/cycle. 1st order method.

The RMS ripple errors on the fundamental measurement at 10 Sa/cycle are reduced from $1.6e^{-3}$ to $4e^{-5}$, a factor of ≈ 40 , compared to the algorithm without 2nd harmonic cancellation.

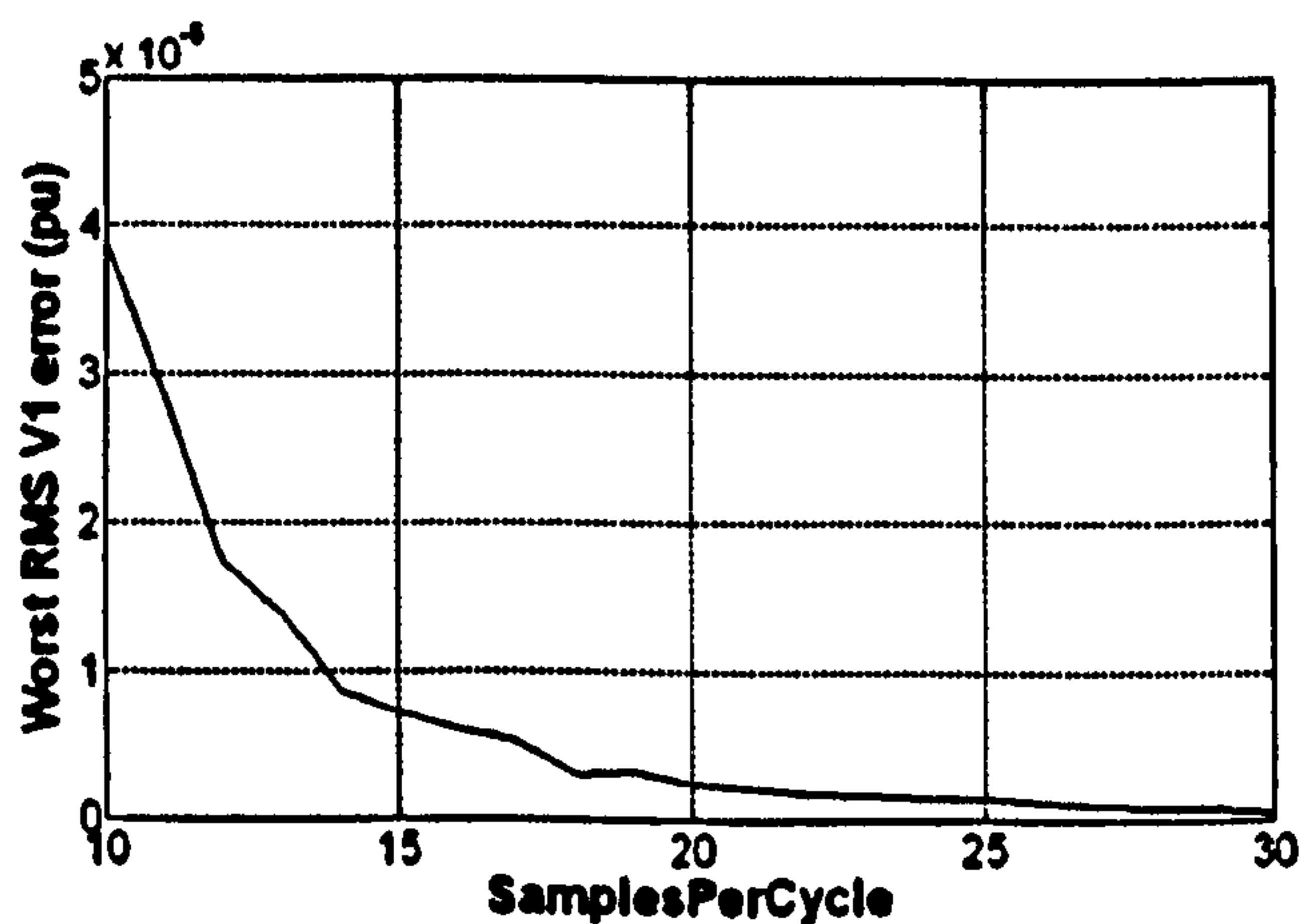


Figure 3-56 : Fourier analysis of fundamental, using 2nd harmonic cancellation. Largest RMS errors due to integration/interpolation over the 45-55Hz range. 1st order method.

Approximately the same improvement factor of ≈ 40 applies to higher sample rates, compared to Figure 3-45.

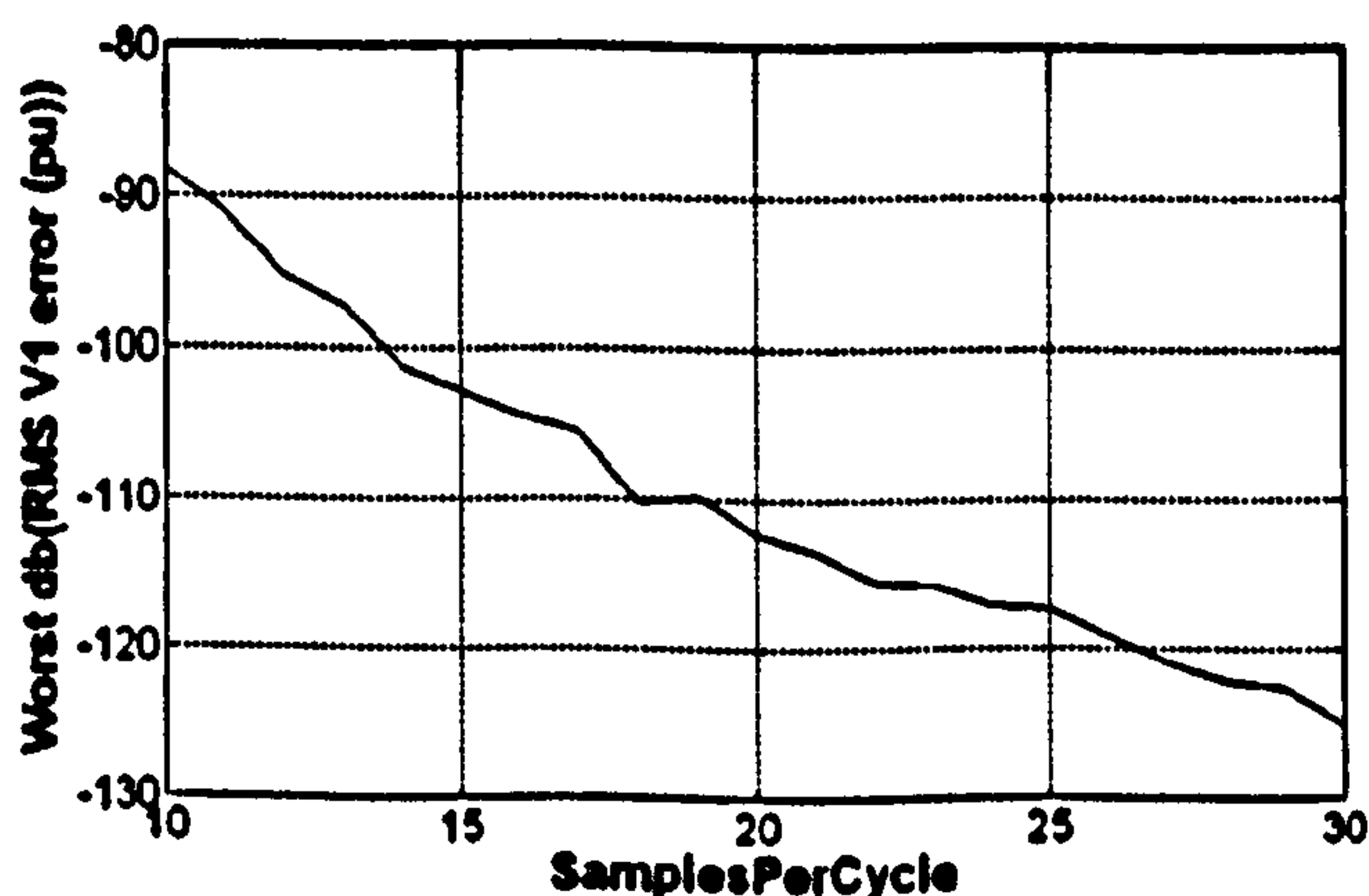


Figure 3-57 : Fourier analysis of fundamental, using 2nd harmonic cancellation. Largest dB(RMS errors) due to integration/interpolation over the 45-55Hz range. 1st order method.

By the same calculation method as shown under Figure 3-46, the error relationship follows a relationship of approximately $N^{-3.9}$

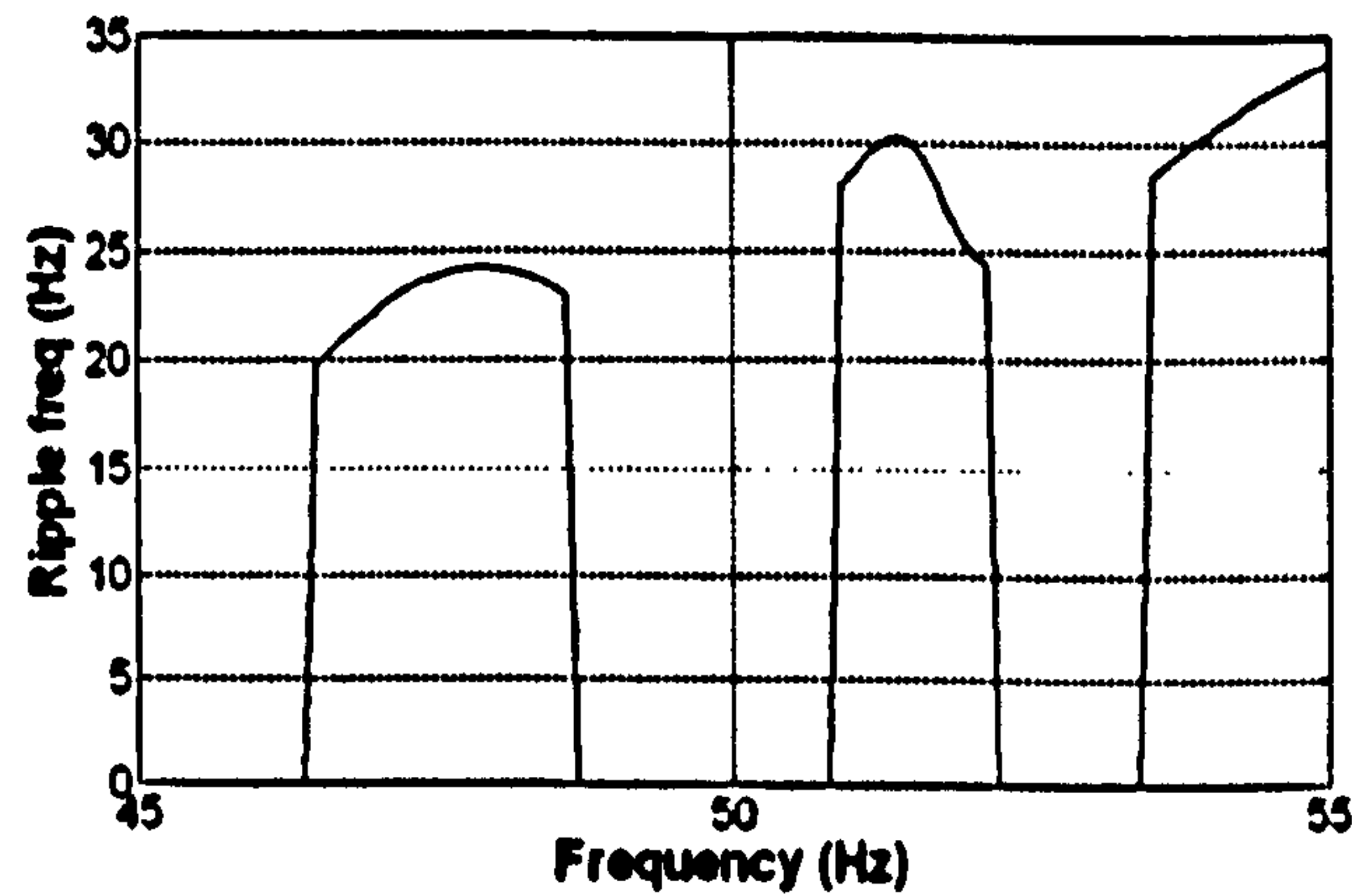


Figure 3-58 : Fourier analysis of fundamental, using 2nd harmonic cancellation. Ripple frequencies of largest errors due to integration/interpolation over the 45-55Hz range. 1st order method.

Note, however, that the frequency of the remaining error is no longer at twice the input frequency, which was the relationship shown from Figure 3-47 for the un-cancelled algorithm. This is because the ripple frequency is modified by the IIR ringing effect introduced by the 2nd harmonic cancellation. This has important (bad) consequences for the effectiveness of subsequent cascaded averaging filters.

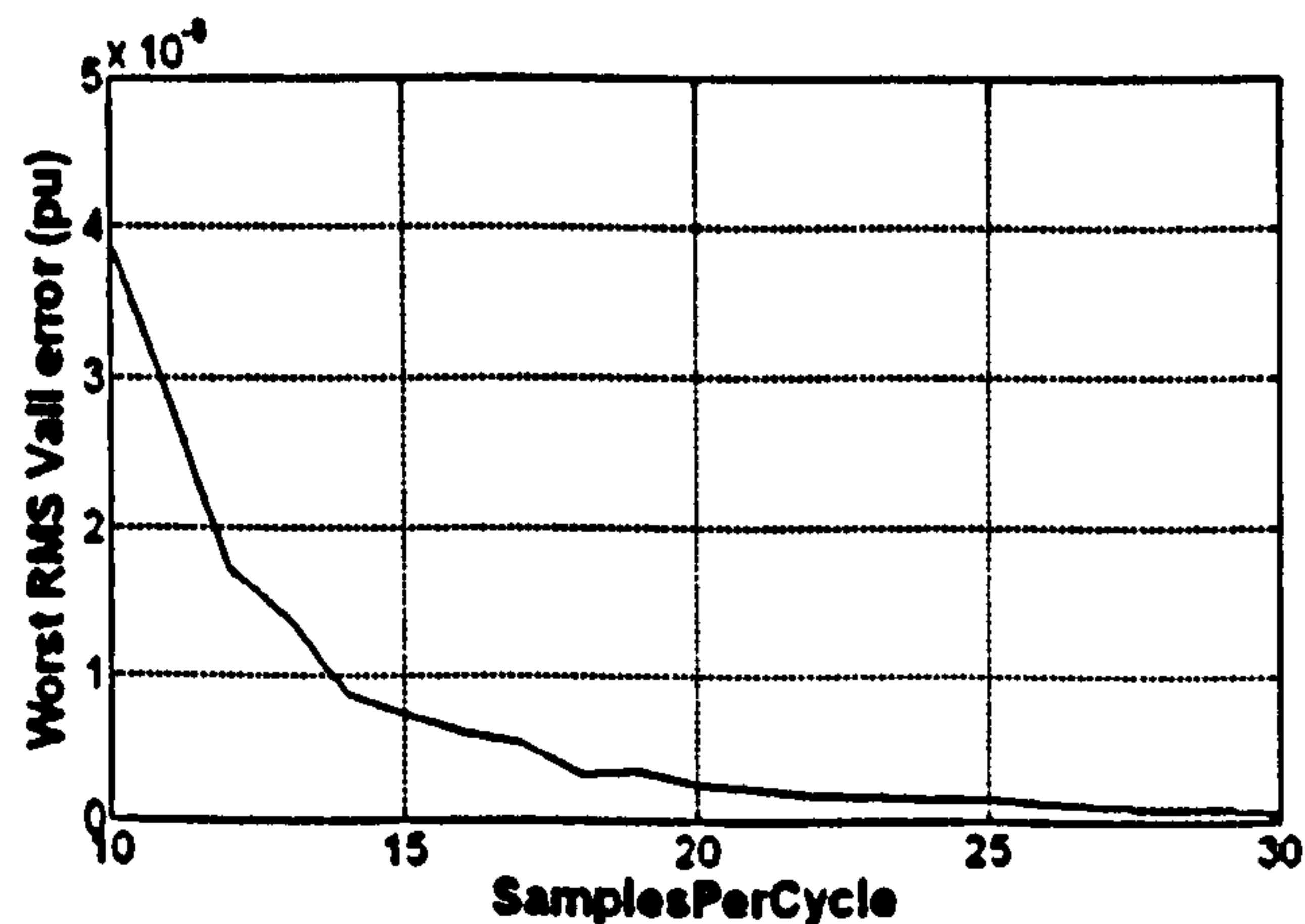


Figure 3-59 : All-harmonic analysis, using 2nd harmonic cancellation. Largest RMS errors due to integration/interpolation over the 45-55Hz range. 1st order method.

The magnitude of the ripples on the all-harmonic RMS measurement are reduced by a factor of ~20, compared to Figure 3-49

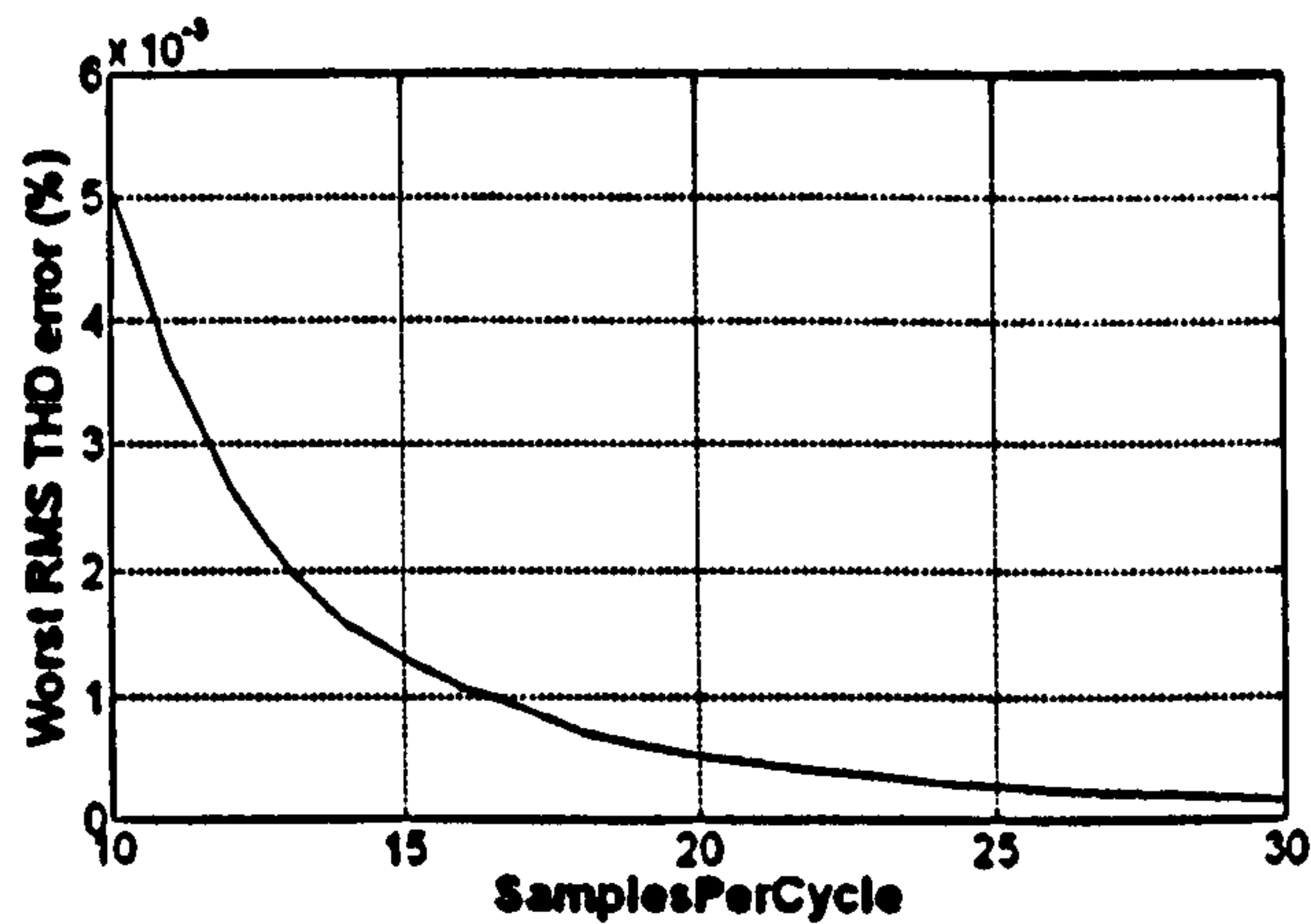


Figure 3-60 : THD analysis, using 2nd harmonic cancellation. Largest RMS errors due to integration/interpolation over the 45-55Hz range. 1st order method.

The errors on the THD measurement, for pure sinusoid inputs, are reduced by a massive factor of ~500 compared to Figure 3-50. This is to do with a different way that THD is calculated by the 2nd harmonic cancellation algorithm. Referring back to Figure 3-43, equations (3.8) and (3.9), and Figure 3-51, the method for calculating the all-harmonic RMS value and the THD value, using 2nd harmonic cancellation, becomes:

- Calculate an estimate of the signal value at the sample time. This is done in a similar but simpler fashion to the calculation of the Path A and Path B cancellation terms. In this case, the fundamental input signal is estimated to be simply $V_e \cdot \sin(\Phi_e)$ where V_e and Φ_e are the estimated magnitude and phase of the input, fed back from the algorithm output. This value can be subtracted from the input signal to give a new value V_h . This signal V_h is the estimate of the harmonic content in real time. This is then passed through an RMS measurement block exactly the same as shown in Figure 3-43, with an integration period of 1 cycle. The output is the estimate of V_h , the RMS magnitude of all the non-fundamental components of the input signal. This leads to estimates of the all-harmonic value V_{All} and THD , via re-arrangement of equations (3.8) and (3.9).

It was attempted to roll this style of THD calculation back into the non-cancelled algorithms of section 3.6, but this was not effective. Further subsequent analysis shows that the extremely good result of Figure 3-60 is a particular corner case for the 2nd harmonic cancellation scheme, and the errors are so small only for the case of exactly sinusoidal inputs in steady state. Harmonic contamination, noise, or the presence of dynamic signals degrades the THD accuracy substantially.

3.8.1 Findings from this section

- 2nd harmonic cancellation can be used to significantly reduce the rippling

interpolation error at 2^*f , for a 1 single cycle Fourier transform or RMS calculation output, if the input waveform has low harmonic content. The error reduction, compared to the algorithm without cancellation, is a factor of ≈ 40 for the fundamental measurement, and ≈ 20 for the all-harmonic RMS measurement, for a pure sinusoid input.

- The algorithm, being an IIR system with a feedback path, can exhibit ringing under transient conditions. A novel algorithm involving detection of transients and mode-switching between “cancelled” and “non-cancelled” operation can be used to limit this ringing.

3.9 Addition of a $\frac{1}{2}$ cycle passive cascaded averaging stage

As described at the beginning of section 3.8, the ripple frequencies of the errors from a single-cycle Fourier transformation block, due to integration and interpolation, appear at twice the input frequency. So far, methods for reducing this which have been discussed are the extension to 2nd order integration/interpolation, and the addition of a 2nd harmonic cancellation scheme. In this section, a third option is described. The third option is available if the acceptable latency of the measurement inside the digital system (after low-pass filtering, sampling and pre-filtering) is $1\frac{1}{2}$ cycles or more.

The idea is extremely simple but novel. Since the remaining errors due to integration/interpolation, at the output of a single-cycle un-cancelled Fourier transform block, ripple at 2^*f or multiples of 2^*f (if higher-order harmonics are present), then a subsequent, cascaded averaging step of $\frac{1}{2}$ a cycle period will reject this ripple. This was previously described in section 3.3.5. This subsequent averaging stage also serves to further filter and bandwidth-limit the effects of noise, as described in section 3.3.4.

The algorithm described here and shown below can be named in an abbreviated way as “1(NC)+0.5, 1st order”, which means that a 1-cycle (Non-Cancelled - without 2nd harmonic cancellation) base measurement (Fourier transformation and/or RMS/THD calculation) is followed by an additional $\frac{1}{2}$ cycle averaging, where all the averaging blocks are implemented using 1st order integration/interpolation. This algorithm builds directly on that shown in Figure 3-42, which is included as a library block within the “1(NC)+0.5, 1st order” block.

**Discrete Fourier analysis, with a single cycle base
 Plus a further half-cycle averaging
 Makes a 1(NC)+0.5 system Andrew Roscoe, 2007**

Hard math function count:-
 sin/cos/tan : 0
 asin/acos : 0
 atan, atan2 : 1
 sqrt : 3
 s^y : 1
 e^x, 10^x : 0
 ln, log10 : 0

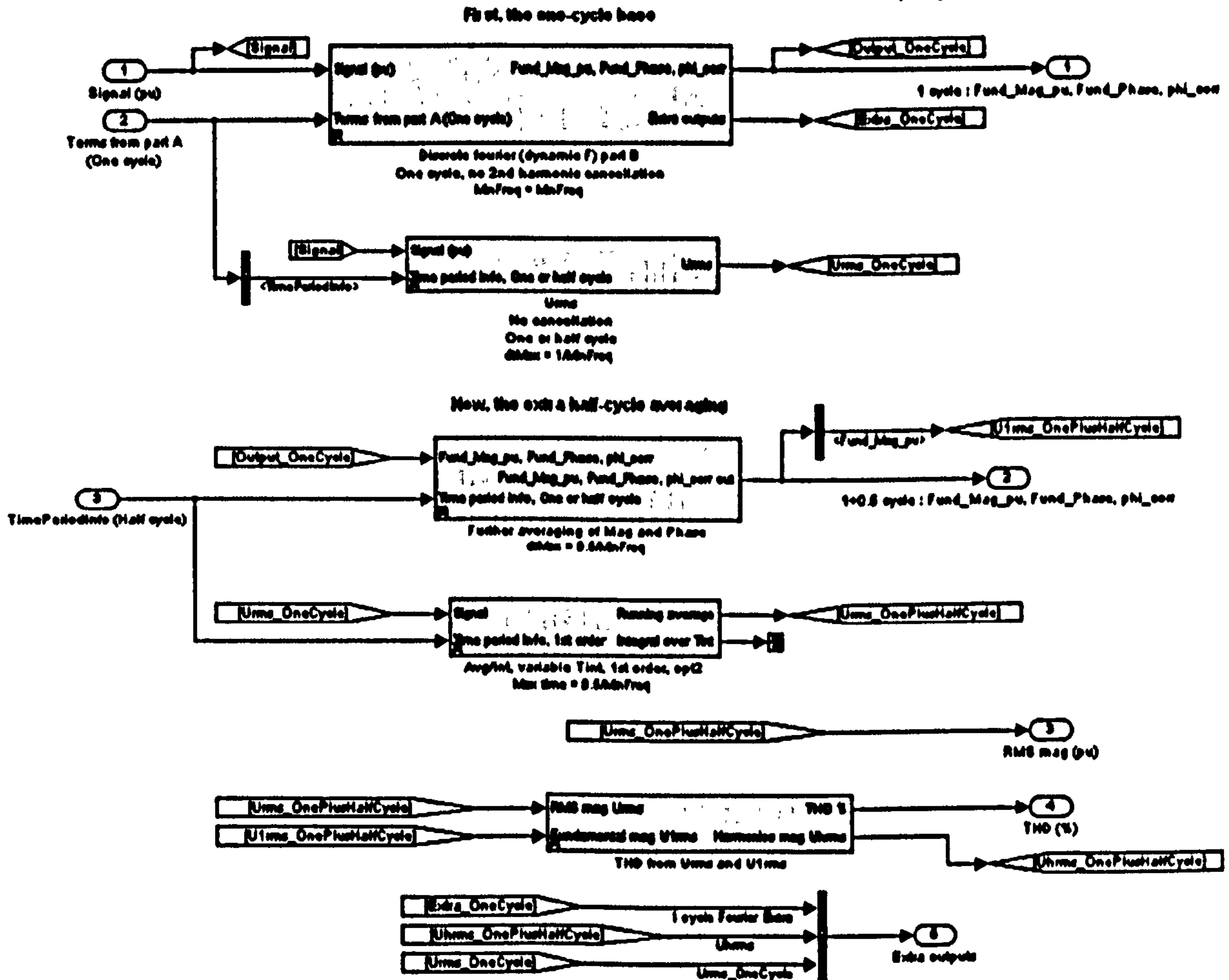


Figure 3-61 : 1(NC)+0.5 measurement algorithm detail, 1st order

Figure 3-61 is relatively self-explanatory, and most of the lower level blocks have either been previously described or contain only basic THD calculations. There are 3 points of note:-

- The algorithm outputs measurements of the fundamental magnitude/phase & RMS on both a 1-cycle and a 1+0.5 cycle basis. These can be used as appropriate for subsequent functions which may prioritise measurement speed (use the 1 cycle output) or measurement ripple minimisation (use the 1+0.5 cycle output). The THD calculation is only carried out on the 1+0.5 cycle basis, since THD is not required for fast relaying actions.
- The algorithm above applies the extra ½-cycle averaging to the magnitude and phase outputs from the first 1-cycle Fourier correlation. A very marginal reduction in ripple at the 1+0.5 cycle output can be achieved by instead averaging the “Path A & B” averages from the Fourier transform block (see Figure 3-42, and also

Figure 3-69). In some circumstances this is not the best option, however, since it requires an additional Cartesian-to-polar transformation in the $\frac{1}{2}$ cycle averaging, which is reasonably CPU-intensive as it uses both an "atan2" and a "sqrt" function. It should be mentioned, however, that this method must be used for extra $\frac{1}{2}$ cycle averaging if the initial Fourier block implements 2nd harmonic cancellation as described in section 3.8. This option is described in section 3.10. Also, and of most relevance, use of this "path averaging" technique can actually reduce the overall CPU loading, despite the extra up-front calculation at this stage. The reason for this is that common operations subsequent to the Fourier calculations are sequence analysis (+ve, -ve, zero) for 3-phase voltage waveforms, and also power calculations (P, Q & S), from 3-phase voltage and current sets. It turns out that doing the path averaging means that many sine/cosine evaluations can be saved later on, by re-using the results of the path average directly, in combination with the magnitude and phase of the final result. The sine and cosine of the voltage and current phase angles can be deduced directly from the path A and path B averages and the hypotenuse (voltage magnitude), by the use of simple division operations.

- Inside the "Further Averaging of Mag and Phase" block, of Figure 3-61, the averaging of phase requires careful implementation to avoid problems with phase wrapping at the $-\pi$ and $+\pi$ boundaries (see section 3.2.4).

As in the previous section, the simulations of section 3.7 were again modified to examine the new algorithm under the same conditions. Results from both the 1st and 2nd order algorithms are presented below. These can be compared directly to the un-cancelled performance in Figure 3-44 to Figure 3-50 and the 2nd-harmonic cancellation performance in Figure 3-55 to Figure 3-60.

The error magnitudes shown in Figure 3-62 (and following) plots are the RMS of the instantaneous ripple error values, with the mean of the "root mean squared" evaluated over one cycle.

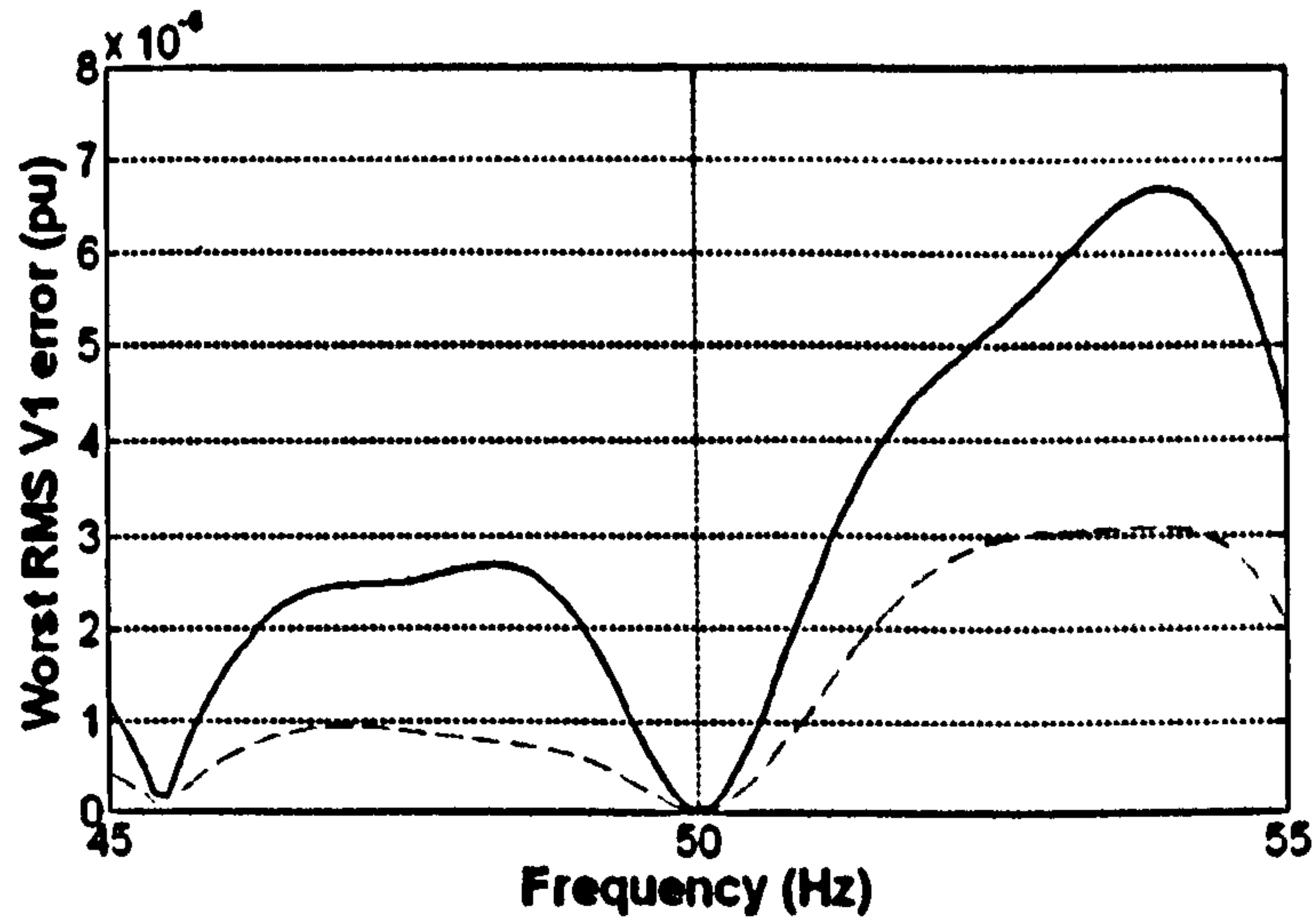


Figure 3-62 : Fourier analysis of fundamental. RMS errors due to integration & interpolation @ 10 Sa/cycle. 1st order (solid) and 2nd order (red dashes) methods with additional half-cycle averaging

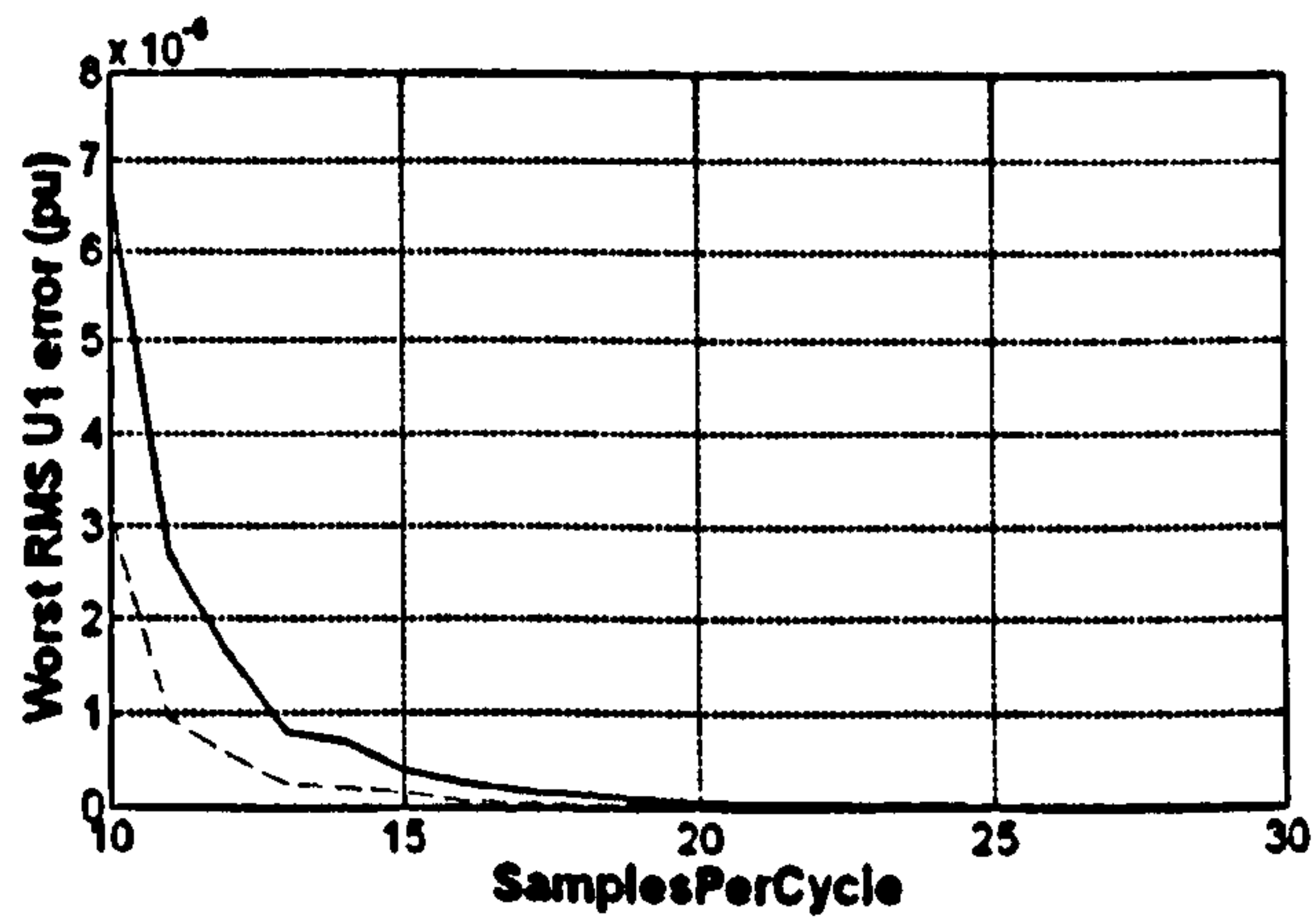


Figure 3-63 : Fourier analysis of fundamental. Largest RMS errors due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods with additional half-cycle averaging

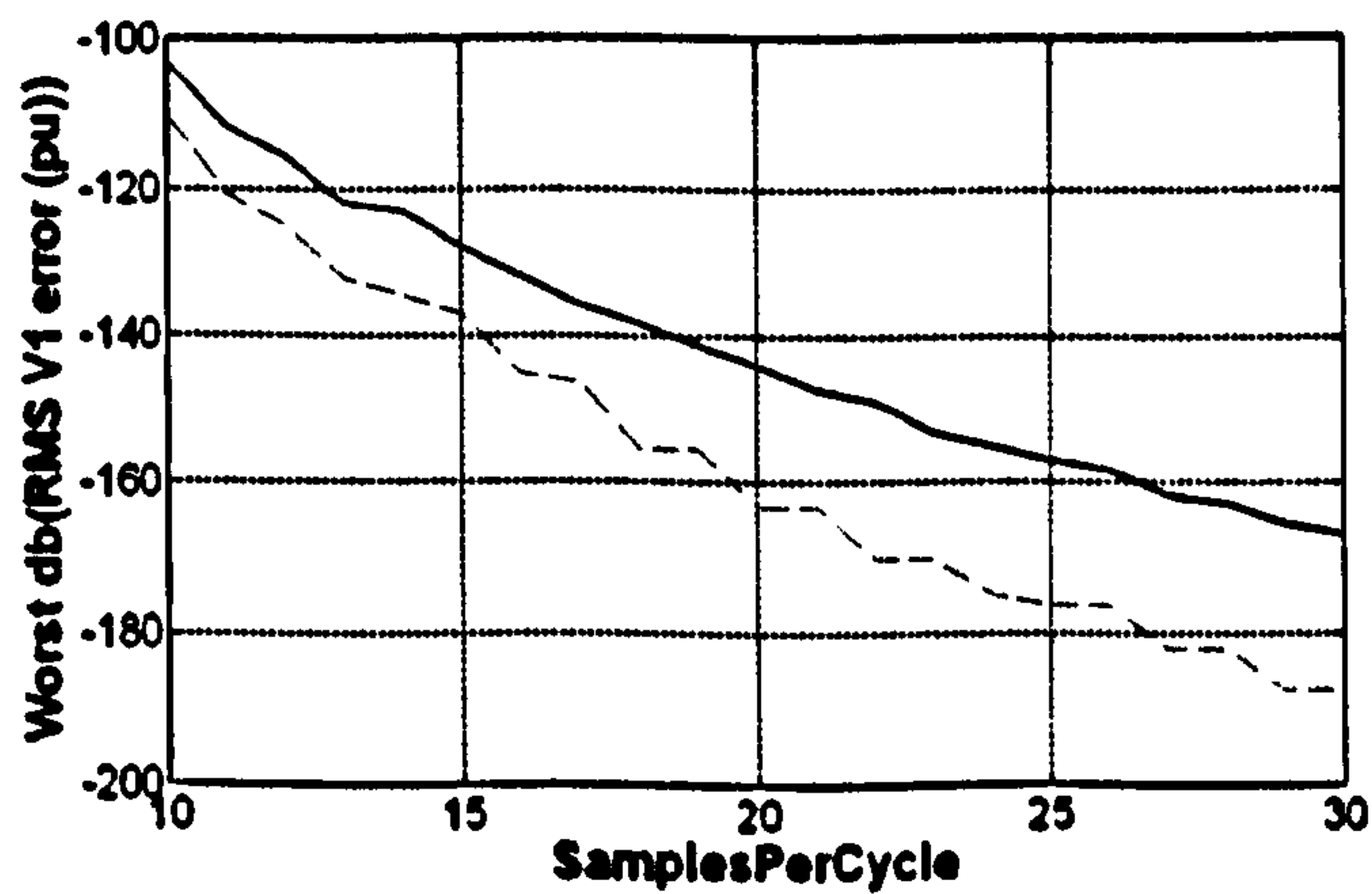


Figure 3-64 : Fourier analysis of fundamental. Largest dB(RMS errors) due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods with additional half-cycle averaging

Following the calculations under Figure 3-46 & Figure 3-57, the error magnitude follows a relationship of approximately $N^{-6.7}$ for the 1st order method, and N^{-8} for the 2nd order method.

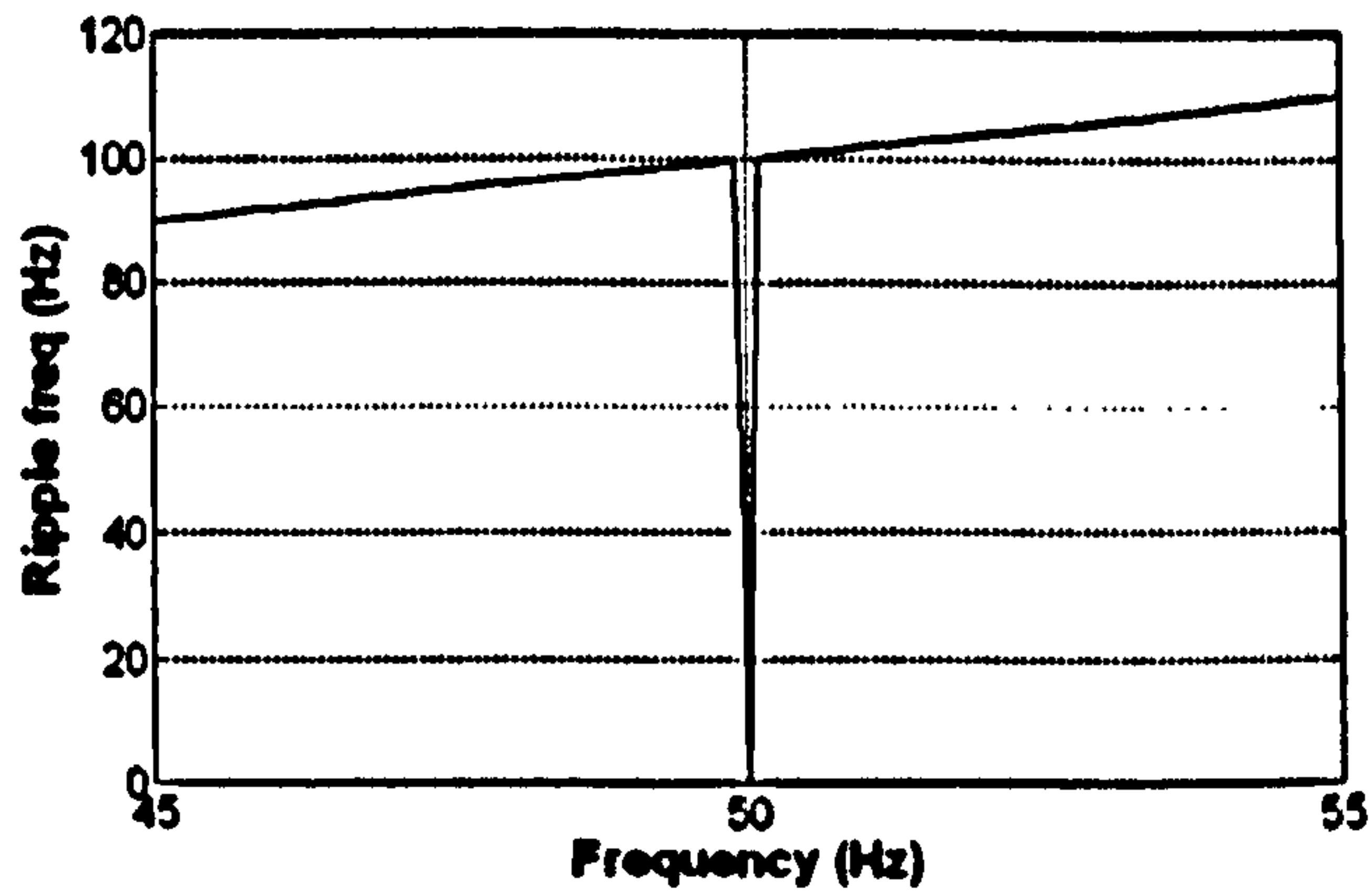


Figure 3-65 : Fourier analysis of fundamental. Ripple frequencies of largest errors due to integration & interpolation over the 45-55Hz range. 1st order method with additional half-cycle averaging

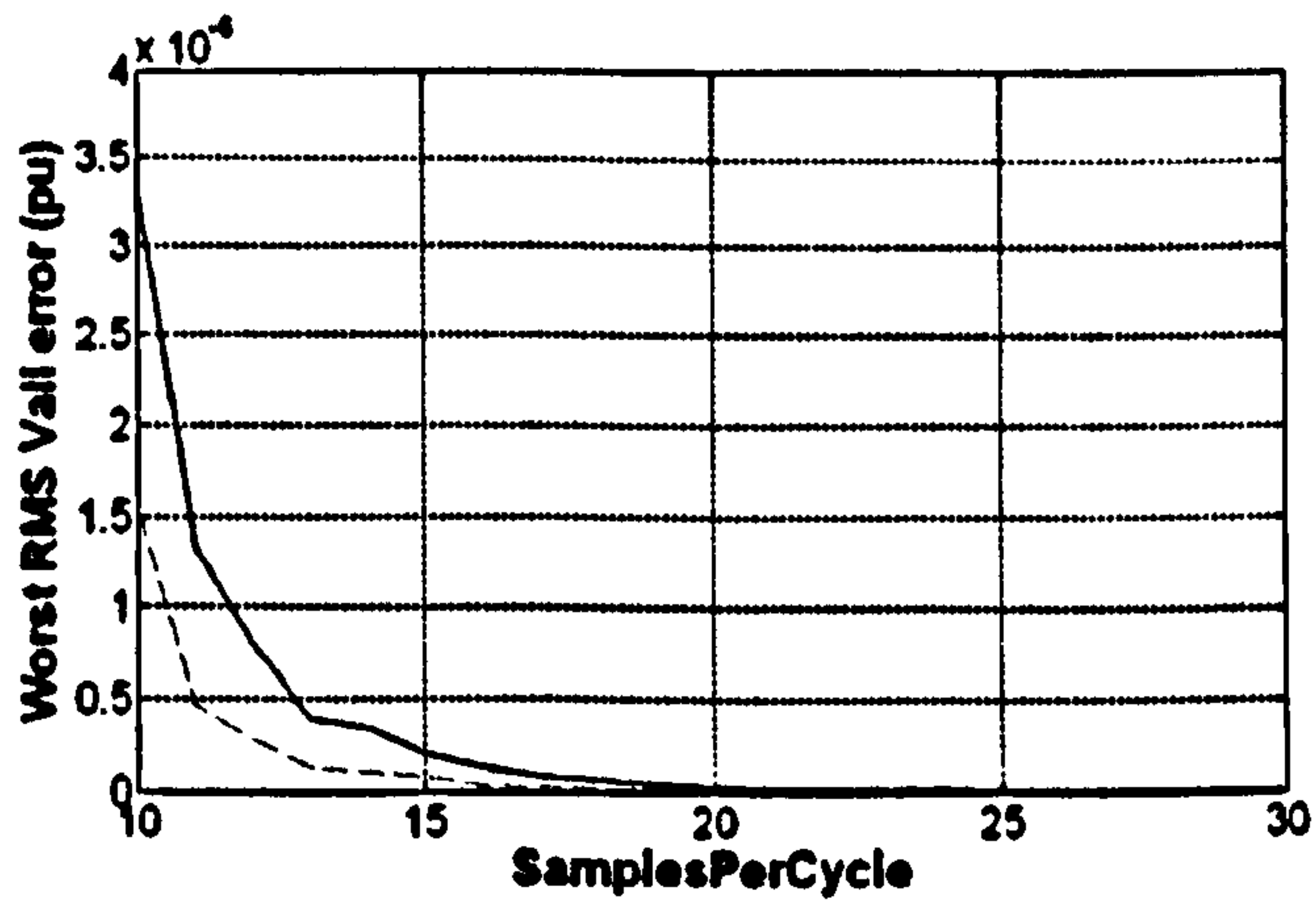


Figure 3-66 : All-harmonic analysis. Largest RMS errors due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods with additional half-cycle averaging

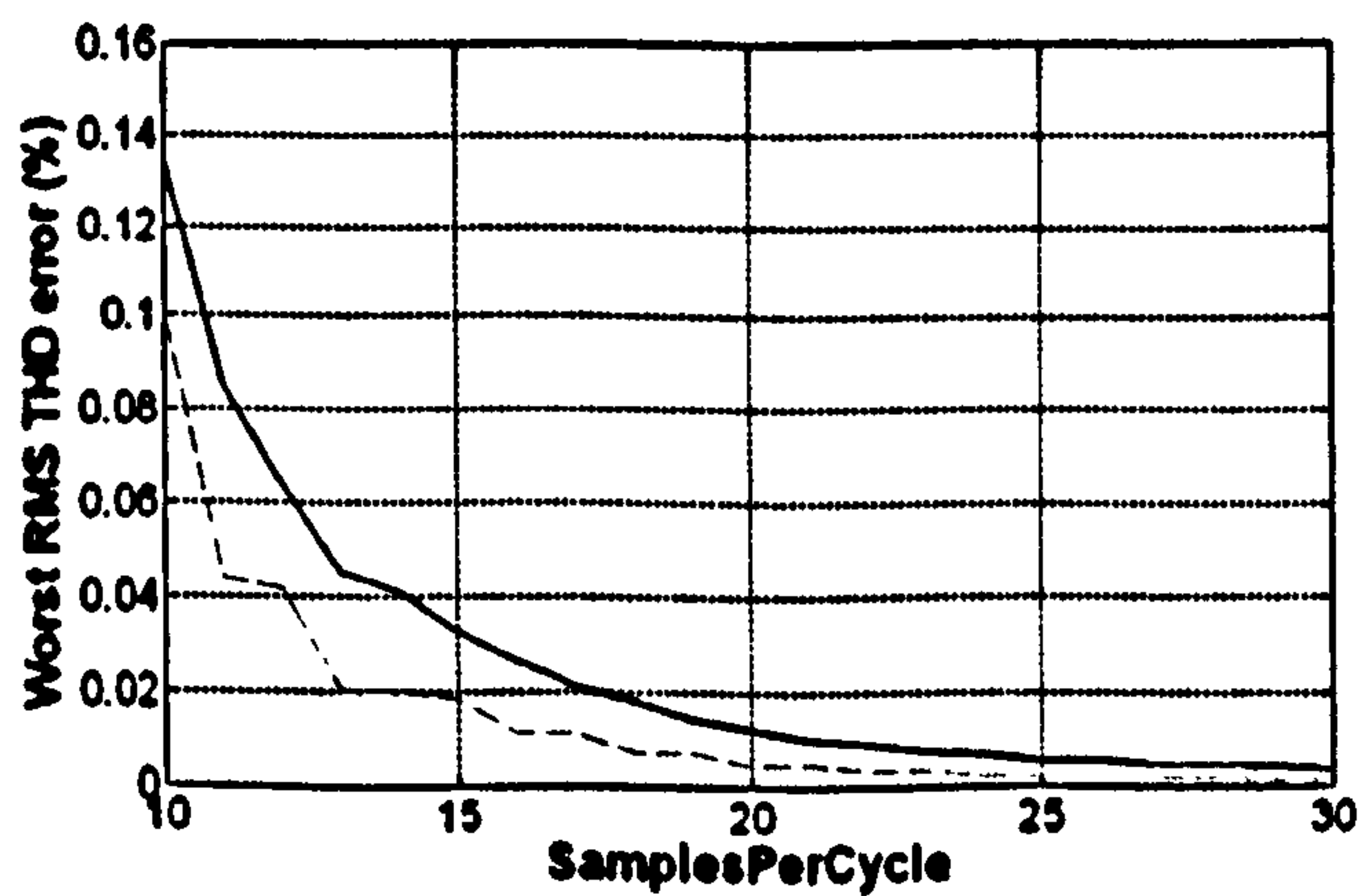


Figure 3-67 : THD analysis. Largest RMS errors due to integration & interpolation over the 45-55Hz range. 1st order (solid) and 2nd order (red dashes) methods with additional half-cycle averaging

3.9.1 Findings for this section

- The integration and interpolation errors for the Fourier fundamental and all-harmonic RMS measurements are practically eliminated, to less than $<0.00001\text{pu}$, for all values of samples per cycle ≥ 10 Sa/cycle, and for both 1st and 2nd order methods. The reduction in ripple due to integration/interpolation, compared to the standard 1-cycle un-cancelled algorithm, is a factor of ≈ 200
- If a measurement latency within the digital system of $1\frac{1}{2}$ cycle can be tolerated for precision measurements, then the interpolation ripple error performance of the “1(NC)+0.5, 1st order” algorithm surpasses the 1-cycle 2nd harmonic cancellation algorithm performance by a factor of ≈ 5 , while requiring substantially less expensive CPU operations due to the lack of need for 2nd harmonic waveform generation.
- With these algorithms, there is no need (or benefit) in synchronising the samples with the zero crossings by using expensive variable sample rate hardware, locked to the fundamental. Indeed, a non-integer number may be chosen for the nominal value of samples per cycle, without any significant detriment to the measurement quality due to integration and interpolation errors.
- The THD measurements are reduced to the $<0.2\%$ level, which is an acceptable error level.
- It has been shown that the “1(NC)+0.5” system, both 1st and 2nd order versions, produces excellent results with a well-defined FIR response which settles fully within $1\frac{1}{2}$ cycles. The $1\frac{1}{2}$ cycle output errors due to integration/interpolation errors on the measurements of fundamental and all-harmonic RMS amplitude for pure sinusoid inputs are at levels less than $-100\text{dB}(\text{pu})$, even for sample rates as low as 500 Sa/s, i.e. 10 Sa/cycle @ 50Hz.

3.10 The combination of 2nd harmonic cancellation with extra $\frac{1}{2}$ cycle averaging

To try and create an optimal integrated measurement algorithm, which provides both quick measurement on the 1-cycle timeframe, plus the option of slower but more accurate (less noise & ripple) measurements, the obvious temptation is to try and combine the benefits of the 1-cycle 2nd harmonic cancellation algorithm with the 1(NC)+0.5 cycle algorithm (1 cycle base measurement, Non-Cancelled, with additional $\frac{1}{2}$ cycle averaging) from section 3.9. An additional idea explored was to use the output of the additionally-averaged outputs to feed back as the amplitude and phase estimates used to form the 2nd harmonic cancellation within the base Fourier stage. The idea here is that the further averaged results would have less noise and ripple, and thus the initial 2nd harmonic

cancellation stage would perform even better.

It turns out that these ideas do not provide reductions in noise or ripple. Substantial simulations were performed before this was fully understood. These do not need to be presented here in detail, since the reasons for the disappointing performance can be explained (with some hindsight) by referring back to Figure 3-47 and Figure 3-58.

The outputs of the non-cancelled 1-cycle base measurement stages contain integration/interpolation ripple at 2 times the fundamental frequency, as shown in Figure 3-47. Thus, the "1(NC)+0.5" system is able to reduce the integration/interpolation ripple to very low levels by applying an extra averaging stage of $\frac{1}{2}$ cycle period duration (see Figure 3-63). This is not the case when the base measurement stage uses active 2nd-harmonic cancellation. The ripple due to integration/interpolation errors from the initial 1-cycle base stage is at a variety of frequencies as shown in Figure 3-58. This is due to the IIR characteristics of the 2nd-harmonic cancellation feedback system. Thus, an additional $\frac{1}{2}$ -cycle averaging does not reduce the ripple so effectively. So, although the ripple from the 1-cycle base stage with 2nd harmonic cancellation is less than the equivalent non-cancelled 1-cycle base stage without cancellation, the "1(C)+0.5" system does not give an overall better performance at its $1\frac{1}{2}$ cycle output port than the "1(NC)+0.5" system. Note that in the case of a pure sinusoid input at fixed frequency only, a "1(C)+0.5" system can give the best results. However, as soon as any harmonic content, noise or dynamically changing conditions arise, the "1(NC)+0.5" system outperforms the "1(C)+0.5" system. The performance of the "1(C)" and "1(C)+0.5" algorithms under such conditions is compared to other algorithms in section 3.13.

Feeding back the additionally-averaged magnitude and phase outputs into the 2nd-harmonic cancellation was also found not to be of any extra benefit over the 1-cycle feedback process shown in Figure 3-51, to counteract the effects of either harmonic contamination or noise on the input signal. The additional delay in the feedback loop also degraded the performance of the algorithm under dynamic conditions from the response shown in Figure 3-53 & Figure 3-54, which is highly undesirable.

Therefore, if it is desired to obtain a 1-cycle output with 2nd-harmonic cancellation, plus also a more accurate result in $1\frac{1}{2}$ cycles, the best system is a parallel pair of systems, with a 1(C) system and a totally separate 1(NC)+0.5 path. Such an algorithm is shown below, of the 1st order variety. The RMS and THD calculations are only output on the $1\frac{1}{2}$ cycle timeframe using the non-cancelled path, since this removes the need for the alternative

RMS/THD derivation which is described under Figure 3-60, and thus saves an expensive sine operation, plus several delay buffer blocks.

Discrete Fourier analysis, with a single cycle base.
Uses 2nd harmonic cancellation to minimise ripple at the 1-cycle output.
Plus a further half-cycle averaging of non-cancelled 1-cycle calculations.
Makes a two parallel systems:
A 1(C) system with fundamental calculation.
A 1(NC)+1 system for fundamental, RMS and THD calculation.

Hard math function count:-	
sin/cos/atan	: 8
asin/acsc	: 0
atan, atan2	: 2
sqrt	: 4
n^y	: 0
e^x, 10^x	: 0
ln, log10	: 0

Andrew Roscoe, 2007

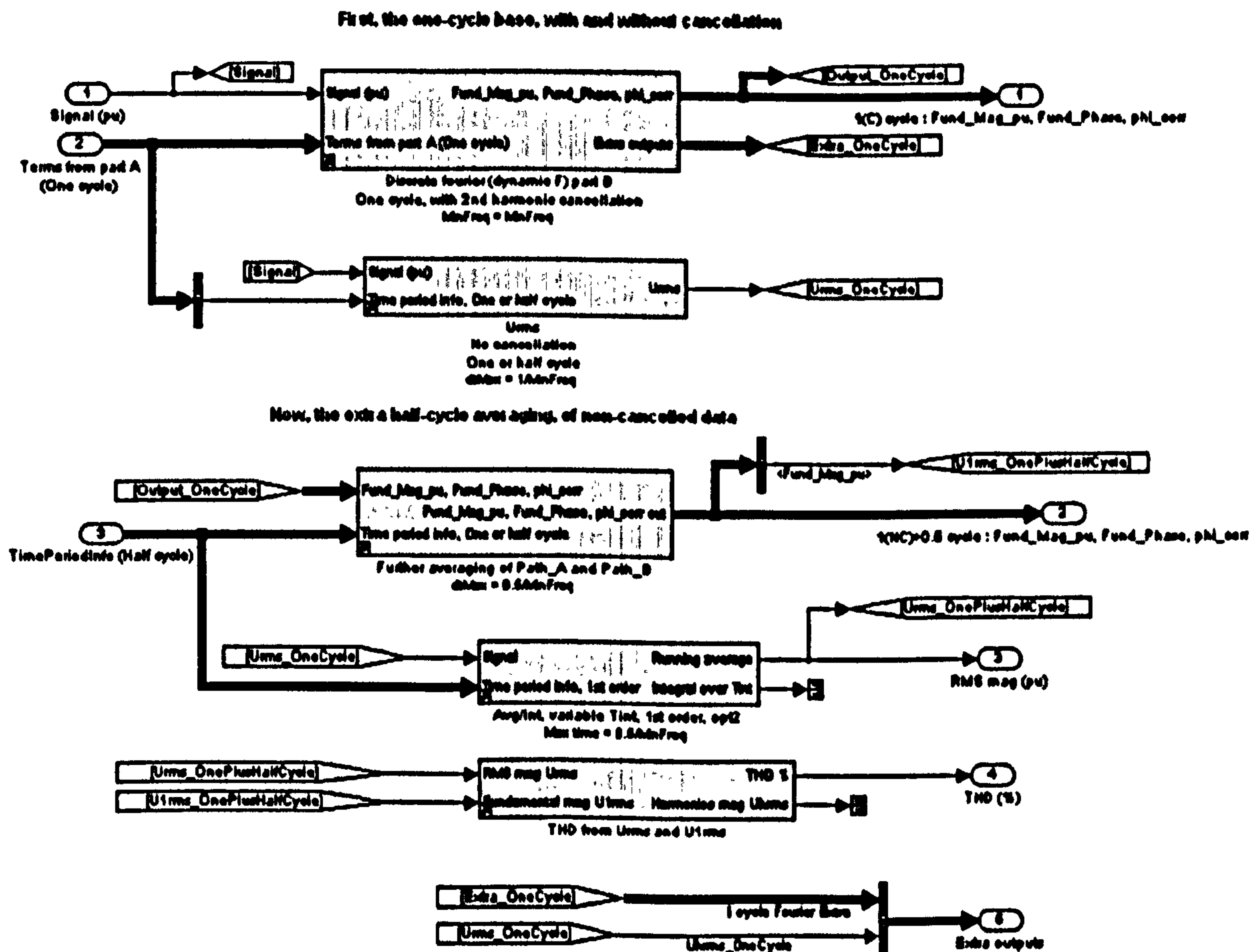


Figure 3-68 : Combined 1(C) and 1(NC)+0.5 measurement algorithm

All the blocks within this algorithm have previously been described, except for the “Further averaging of Path_A and Path_B” block (although it was referred to in the findings to section 3.9). This is shown below. Note that this requires an additional atan2 and sqrt function, and is thus reasonably CPU intensive. Over and above the un-cancelled “1(NC)+0.5” system, which requires 4 “hard” math operations¹, the “1(C)” in parallel with the “1(NC)+0.5” system requires 8 “hard” maths operations. 2 of these are the sine/cosine for the 2nd-harmonic cancellation, and 2 of these are required for additional path

¹ See section 3.13.1, Table 3-3 for the list of “hard” maths functions

atan2/sqrt functions required for the Cartesian to polar transformation inside the extra path averaging.

Add further averaging to Fourier fundamental magnitude and phase outputs
Using Path_A and Path_B requires additional "Cart to Polar" transform
but results in slightly more accurate results.
It is also required if the first block is a 2nd harmonic cancelled block

```

Hard math function count:-
atan/atan2      : 0
atan/atan       : 0
atan/atan2      : 2 (Cart to polar)
sqrt            : 2 (Cart to polar)
sqrt            : 0
atan2, atan     : 0
atan, atan2     : 0

```

Andrew Reeves, 2007

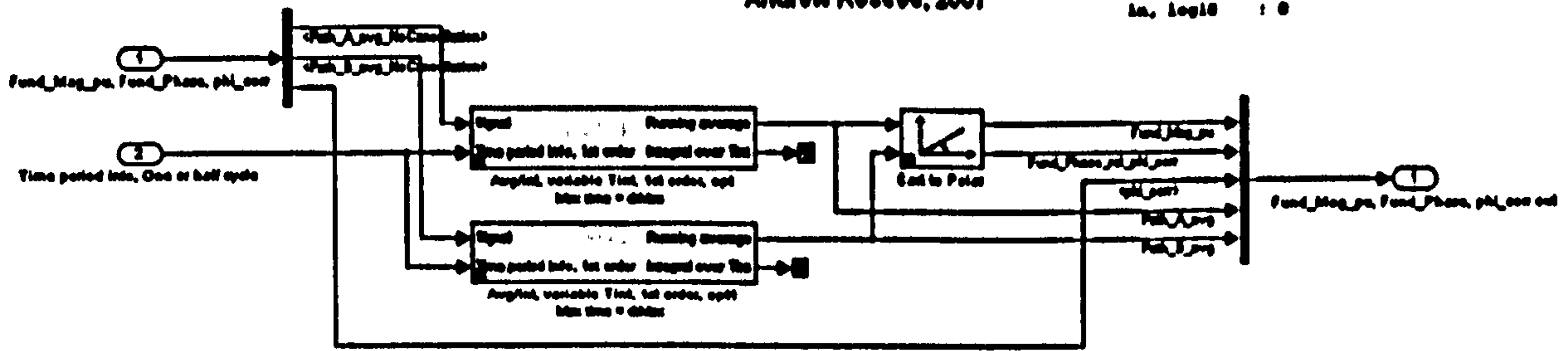


Figure 3-69 : Path averaging for the combined 1(C) and 1(NC)+0.5 measurement algorithm

3.10.1 Findings from this section

- The ripple from the 2nd-harmonic cancelled base measurement blocks is not always at 2*Fundamental or harmonics of this frequency. This is due to the IIR response of the algorithm.
- A subsequent ½ cycle averaging stage does not, therefore, have anywhere near as much additional benefit as it does for the un-cancelled 1-cycle base measurements.
- Where the most accurate 1-cycle base measurements are required, the 2nd harmonic cancelled algorithms are the best (requiring extra CPU effort to carry out this task).
- Where measurement latency in the digital system of 1½ cycles or more can be tolerated, then either the non-cancelled path of the algorithm should be used for further averaging, or a non-cancelled base stage should be used.
- If minimising ripple is not of the highest priority from the initial 1-cycle base measurement, then algorithm execution time, complexity, and robustness during dynamic events can be improved by not using the 2nd-harmonic cancelled base stage, and using the simpler un-cancelled base stage of section 3.6.

3.11 Base measurement stages of ½ cycle duration

The mathematical expressions for Fourier and RMS measurements allow the measurements to be made over timeframes other than 1 cycle. Normally, however, it would be expected that the timeframe of the measurements would be ≥ 1 cycle, and often the measurement time cannot be set to exact multiples of the fundamental cycle period as is being done in this thesis. In this case, Fourier windowing techniques such as Hanning windows are used

to minimise the ripple magnitude due to the effect of non-integer numbers of cycles appearing inside the analysis window.

The analysis of power systems waveforms is rather a specialised field because the desire is to measure the size/phase/frequency of a nominally sinusoidal waveform with latencies of the order of <1 to 10 cycles. For protective relaying of overcurrent, measurement latencies of <1 cycle (or as small as reasonably possible) are desirable. To do this, techniques such as the 2 and 3-sample algorithms from Johns (1995) have been developed. These can give an estimation of signal amplitude in $\ll 1$ cycle for sinusoidal signals. These kinds of techniques can be used on HV & EHV transmission lines where the THD is low, and fast tripping times are very important since the protection is likely to be of the "unit" variety, designed primarily to protect the line from melting/sagging which it may do very quickly under fault conditions due to the low per-unit impedance.

Under the influence of harmonic contamination and flicker levels such as those described in section 2.7, however, the outputs such sub-cycle algorithms become corrupt. Within a microgrid context, the scenario and priorities are different. THD on the voltage & current waveforms is much higher, but longer tripping times can be tolerated since the protection will be part of a graded protection scheme, the per-unit impedances are higher, and the distribution/switching/breaking/protection equipment will be designed to carry rated fault current for certain times without damage. This means that a measurement latency of $\ll 1$ cycle (much less than one cycle) is not required for protection purposes within a microgrid. However, a <1 cycle measurement latency (somewhat less than a cycle digital response time) may be desirable, especially when the minimum achievable latency is limited by the filtering and ADC sampling latencies shown in Figure 3-30 & Figure 3-31.

An intermediate solution, between a $\ll 1$ cycle and a 1-cycle measurement, is a Fourier or RMS calculation over exactly $\frac{1}{2}$ cycle (Johns, 1995). To do this, any of the algorithms from section 3.6 or section 3.8, 1st or 2nd order, can be adapted to operate with on a $\frac{1}{2}$ -cycle base measurement basis. These algorithms have been coded as Simulink blocks and analysed in detail. The code does not need to be presented or described here due to its total similarity to those algorithms already described. Only the time periods for all the base stage averaging processes are different, being halved.

The performance of some of these blocks is presented together with other blocks in section 3.13. Here, it is useful to describe their properties in words. Figure 3-70 to Figure 3-77 show plots which corroborate these statements.

3.11.1 Properties of the ½ cycle base measurement stage

- The integration/interpolation errors are larger than for the 1-cycle equivalent base stages. This is not because the interpolation errors are larger, but because the timeframe is half as long which leads to an average calculation in which the interpolation error is not “spread” over as long a timeframe. The worst frequencies for integration/interpolation errors occur at

$$F_{worst} = \frac{F_{nom} \frac{N}{2}}{\left(\frac{N}{2} \pm \frac{m}{2}\right)}$$

(3.15)

where m is any sensible odd integer to give a positive frequency. This can be compared directly to equation (3.10). The worst frequencies are roughly twice as far apart as for the 1-cycle base measurements.

- Theoretically, odd harmonics present on the input signal will be rejected by a ½-cycle analysis. However, odd harmonics do increase the interpolation error (as they do for the 1-cycle base measurements).
- Even harmonics present on the input signal will not be rejected by a ½-cycle analysis. Thus, any input signal containing even harmonics will produce a ripple at the output of the ½-cycle block. This ripple consists of the theoretical ripple output due to the harmonic, plus the additional integration/interpolation ripple.
- DC offsets on the input signal are a special case of an even harmonic. They are effectively the 0th harmonic, and a DC level of x produces a theoretical ripple magnitude equivalent to that of any non-DC even harmonic at a peak amplitude of $2x$. Thus, even small DC offsets can lead to large ripples at the output of the ½-cycle base stages. Fortunately, this effect can be ignored for the practical applications described in this thesis, as DC offsets can be removed by the DC blocking filter designed in section 3.4.4.2. The exception is during a hard fault when the current or voltage waveforms may contain genuine DC offsets for a few cycles. During this time, the DC blocking filter will allow the DC through, so a user of such ½-cycle blocks should allow for this.
- It is possible to use a 2nd-harmonic cancelled version of the ½-cycle base measurement block. This, however, is susceptible to relatively large ripple/ringing when even harmonics (or stray DC) are applied (see Figure 3-70). Its performance under these conditions is worse than the non-cancelled version. Thus, this is not a good candidate algorithm to use within the microgrid context.

- Half-cycle base measurement stages can also be used as the core of fast-responding PLLs. These are of course noisier than 1-cycle PLLs, and susceptible to ripple due to the presence of even harmonics.

3.12 “0.5(NC)+1” systems

In the previous section, the $\frac{1}{2}$ -cycle base measurement was introduced. This offers a faster measurement than the 1-cycle base measurement for protective over-current relaying purposes. The 2nd-harmonic cancelled version of the $\frac{1}{2}$ -cycle base block has not been found to be a sensible algorithm to use within the microgrid context, due to signal contamination by even harmonics. The un-cancelled $\frac{1}{2}$ -cycle base measurement, however, can be used as the base for accurate measurements. The idea is that the simple, un-cancelled $\frac{1}{2}$ -cycle base measurement is applied first. This will output more ripple than the equivalent 1-cycle base measurement, both due to integration/interpolation errors of the fundamental and harmonics, plus much larger ripples due to even harmonic and DC contamination. The signal output, even with this ripple added, will still be usable for fast-acting protective over-current relays with trip settings high enough above 1pu to avoid spurious tripping due to the ripple.

The ripple which is output from the $\frac{1}{2}$ -cycle base measurement blocks turns out to be at frequencies of multiples of $1 \cdot f$. Now, recalling that the 1-cycle base measurements contain ripple at $n \cdot 2 \cdot F$, which can be almost entirely removed by further averaging over a time period $1/(2 \cdot F)$, it can be seen that the ripple from the $\frac{1}{2}$ -cycle base measurements can be almost totally removed by further averaging over a time period of exactly $1/f$. Thus, where a “1(NC)+0.5” system which outputs virtually no ripple due to sampling effects was created in section 3.9, a new algorithm which can be called “0.5(NC)+1” appears to be an equally valid method to achieve robust measurements at low sample rates, with virtually zero integration/interpolation errors. The classification “0.5(NC)+1” here means “ $\frac{1}{2}$ -cycle base Fourier measurement (no 2nd-harmonic cancellation) followed by 1-cycle averaging”. This algorithm set has been coded in Simulink, and the results are compared with other methods in the next section.

3.12.1 Findings from this section

- The “0.5(NC)+1” measurement system is a viable measurement system, offering almost identical performance to the “1(NC)+0.5” system in the presence of harmonics and noise.

3.13 Summary of viable measurement systems and their comparisons under conditions of harmonics and noise

Thus far in section 3, several competing measurement systems have been proposed for the measurement of Fourier amplitude, phase, RMS & THD. Most emphasis is placed upon the Fourier measurements, but the algorithmic processes and relative errors have also been examined for RMS and THD measurements. This section briefly reviews the proposed systems, and compares their performance under a suite of test conditions. The viable methods proposed thus far are:-

Classification	1(NC)	1(C)	1(NC)+0.5	0.5(NC)	0.5(NC)+1
Base measurement (Fourier or RMS/THD) cycles	1	1	1	½	½
Active 2 nd harmonic cancellation within the base measurement ?	No	Yes	No	No	No
Further averaging (of non-cancelled path averages for base stages with 2 nd harmonic cancellation)	-	-	½ cycle	-	1 cycle
For	Robust, simple	Lowest possible ripple for sinusoidal input, with a 1-cycle measurement time. 1(NC) outputs also available.	Very low ripple for all un-aliased harmonics on input	Fast response for over-current relaying	Very low ripple for all un-aliased harmonics on input
Against		Extra CPU overhead, complexity. Cancellation not as effective when harmonics present.		Large ripples on output for even harmonics or DC on input	
Worst RMS Ripple (pu) on Fourier amplitude measurements due to a pure sinusoid input, for 1 st order algorithms. [2 nd order algorithms up to a factor of 2 smaller]	0.0016	0.00004	0.000007	0.0035	0.000008

Table 3-1 : Viable measurement architectures

Plus, the 6th final option is available of using a 1(C) base measurement stage, but following this through to obtain the "1(NC)+0.5" solution, since the "1(NC)" algorithm is a subset of the "1(C)" algorithm, and the "1(NC)" outputs are therefore available from the "1(C)" algorithm for further averaging.

These 6 viable options, plus the un-recommended “0.5(C)” option (for comparison only), are now subjected to further rounds of testing. This testing involves addition of Gaussian noise and harmonic contamination, and examination of the resulting worst RMS ripple errors of the algorithms for any input frequency in a range wide enough to catch the worst expected integration/interpolation errors. Two sample rates are examined: 500 Sa/s (10 Sa/cycle @ 50 Hz), and 1000 Sa/s (20 Sa/cycle @ 50Hz). The examined input frequency ranges are 44 to 56 Hz for the 500 Sa/s case, and 47 to 53Hz for the 1000 Sa/s case. This allows for full coverage of the worst frequencies for all systems with both the 1-cycle and ½-cycle base measurements, by equations (3.10) & (3.15).

The Gaussian noise simulates ADC quantisation at the 0.000282pu RMS level, or the worst case 0.005pu RMS instrumentation noise level anticipated for a voltage measurement channel (see section 2.9). The harmonics added in this round of testing are un-aliased. For the 500 Sa/s case, the 2nd and 3rd harmonics are considered. For the 1000 Sa/s case, the 2nd, 3rd and 5th harmonics are considered. The aliased harmonics have a different effect on the performance of all the blocks, which is examined later in section 4.2. In this set of simulations, the anti-alias filter response is not modelled so as to focus purely on the algorithm integration/interpolation errors. The DC block algorithm, however, is included into the simulation, to validate its performance (see section 3.4.4.2). A 0.02pu DC bias is applied to all measurement inputs.

The harmonic levels for the contaminating harmonics are chosen to be 2 times the BS EN 50160 specification for long-term average values:-

Harmonic	Harmonic frequency for 50Hz nominal fundamental	BS EN 50160 specification	Applied level in this analysis2
2nd	100 Hz	2%	4%
3rd	150 Hz	5%	10%
5th	250 Hz (therefore is aliased for 500 Sa/s systems when nominal frequency > 50 Hz)	6%	12%

Table 3-2 : Harmonic levels applied for analysis of viable blocks

The analysis is carried out by a Simulink model containing the appropriate signal generation and analysis library blocks. The analysis and spreadsheet includes results for Fourier amplitude/phase errors, RMS errors and THD errors. Only the Fourier amplitude error measurements are shown here for brevity. The relative sizes of the other types of

errors are broadly proportionate to the Fourier amplitude errors, so the decision process for the selection of the best blocks can reasonably be shown using only the Fourier errors.

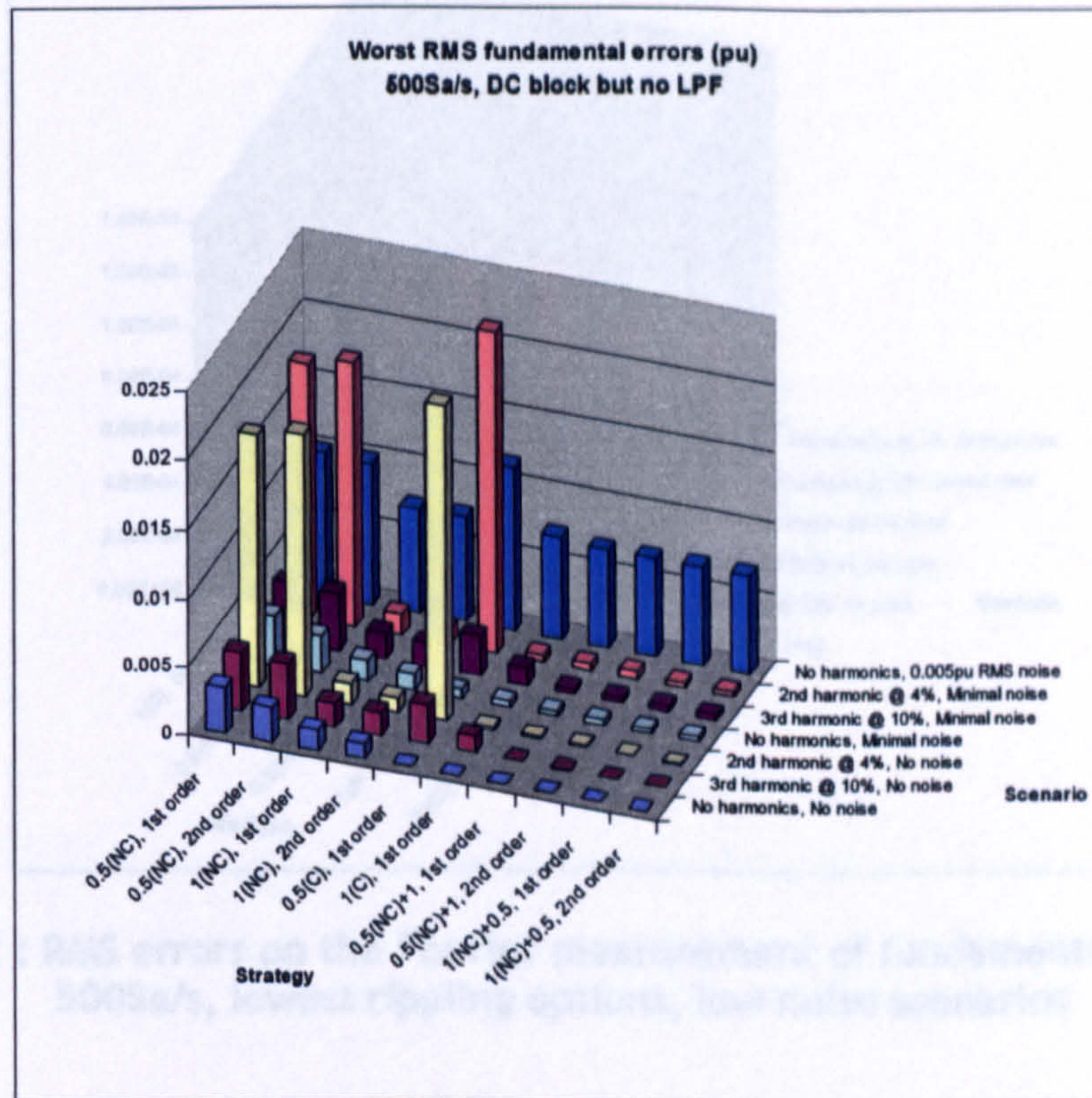


Figure 3-70 : RMS errors on the Fourier measurement of fundamental amplitude, 500Sa/s, all viable options and scenarios

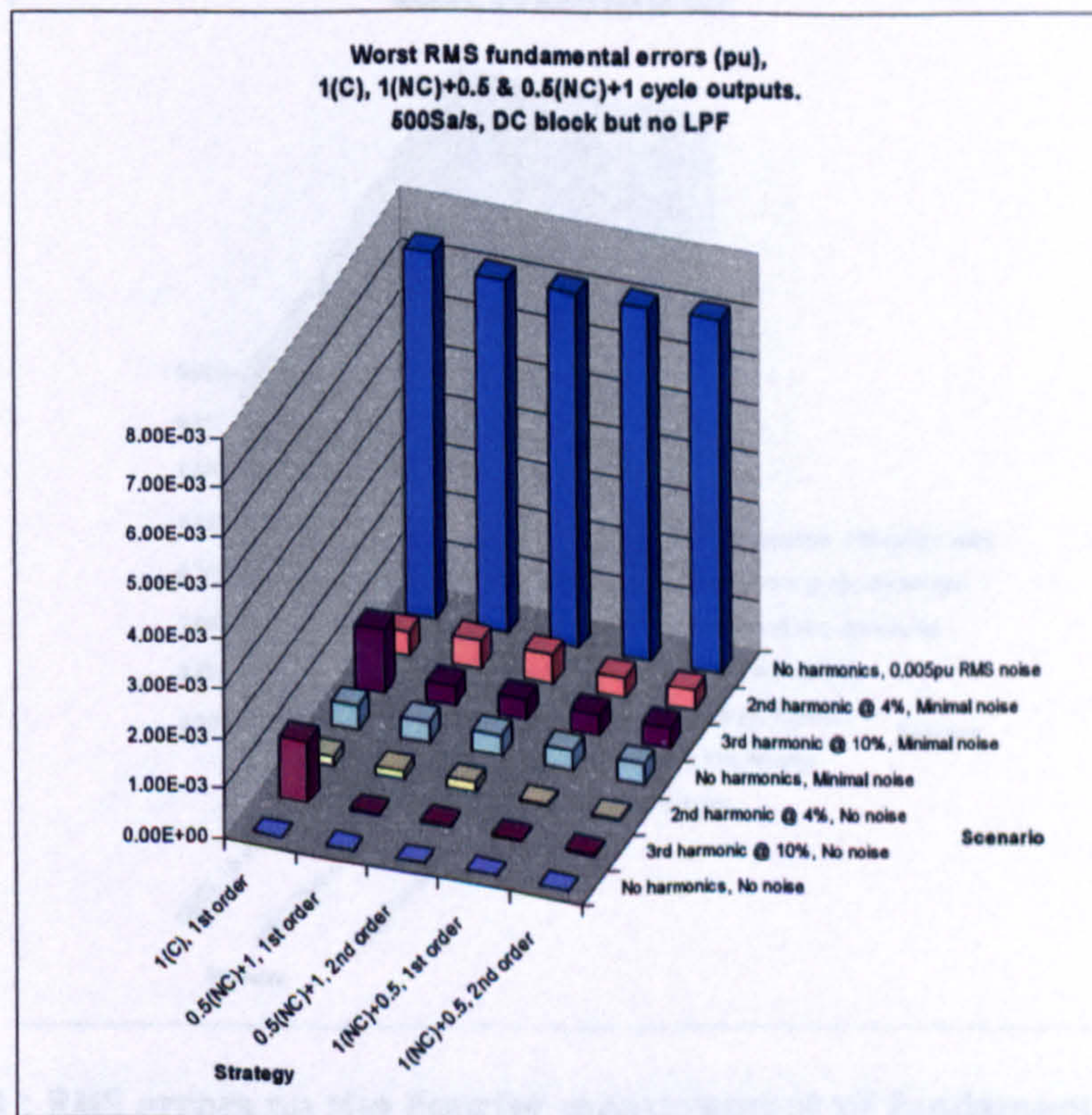


Figure 3-71 : RMS errors on the Fourier measurement of fundamental amplitude, 500Sa/s, lowest rippling options, all scenarios

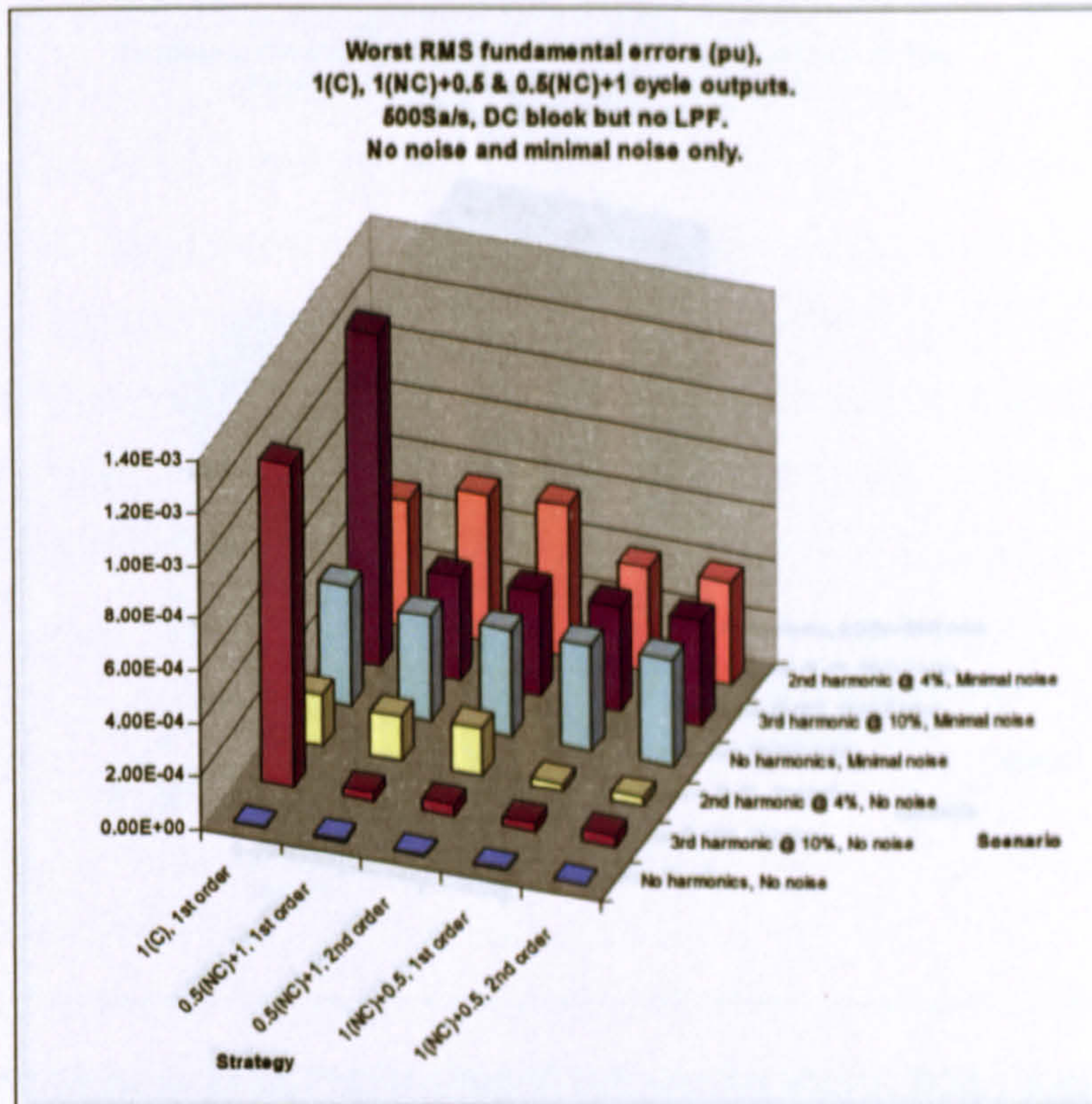


Figure 3-72 : RMS errors on the Fourier measurement of fundamental amplitude, 500Sa/s, lowest rippling options, low noise scenarios

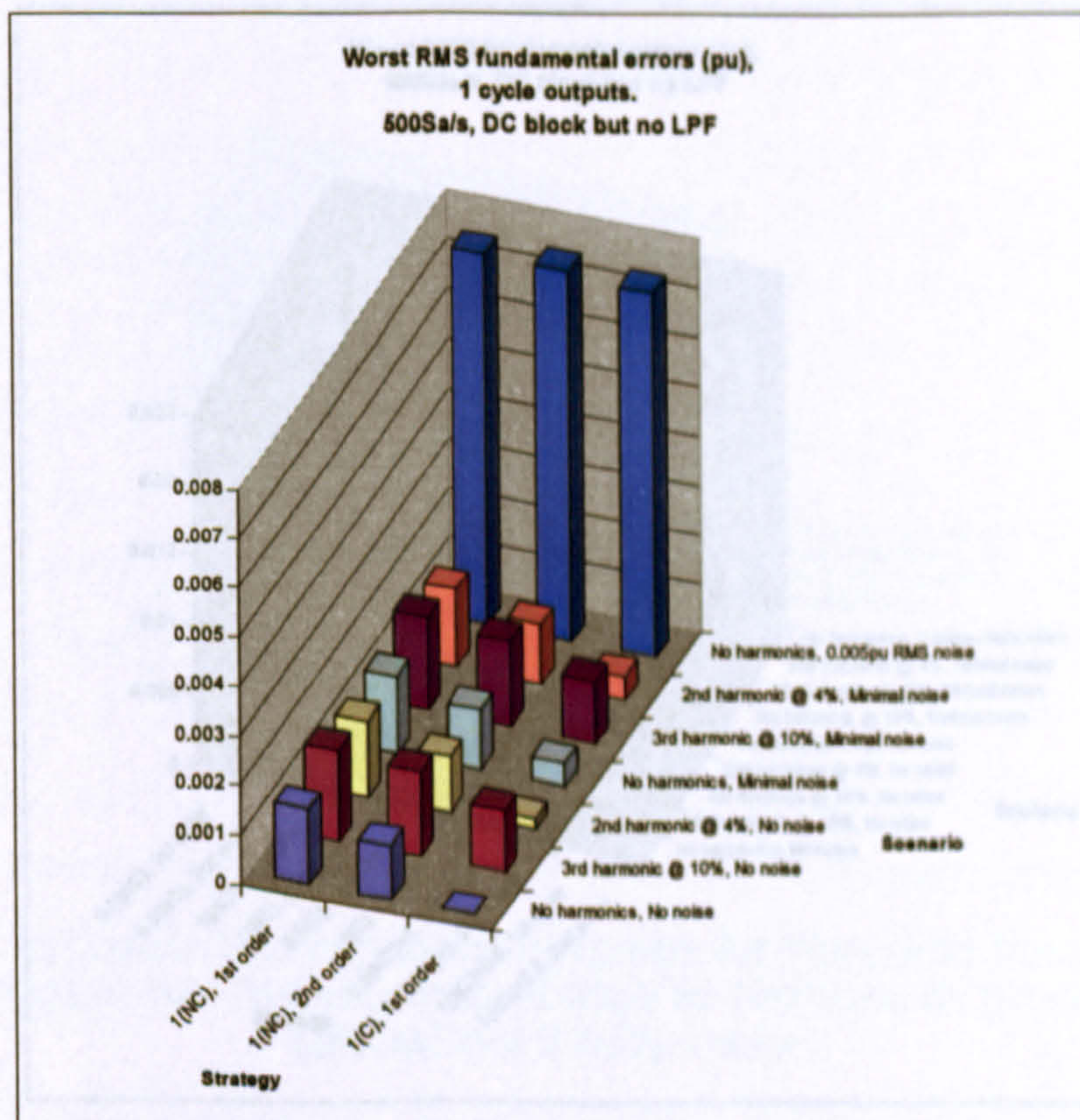


Figure 3-73 : RMS errors on the Fourier measurement of fundamental amplitude, 500Sa/s, 1-cycle latency measurements, all scenarios

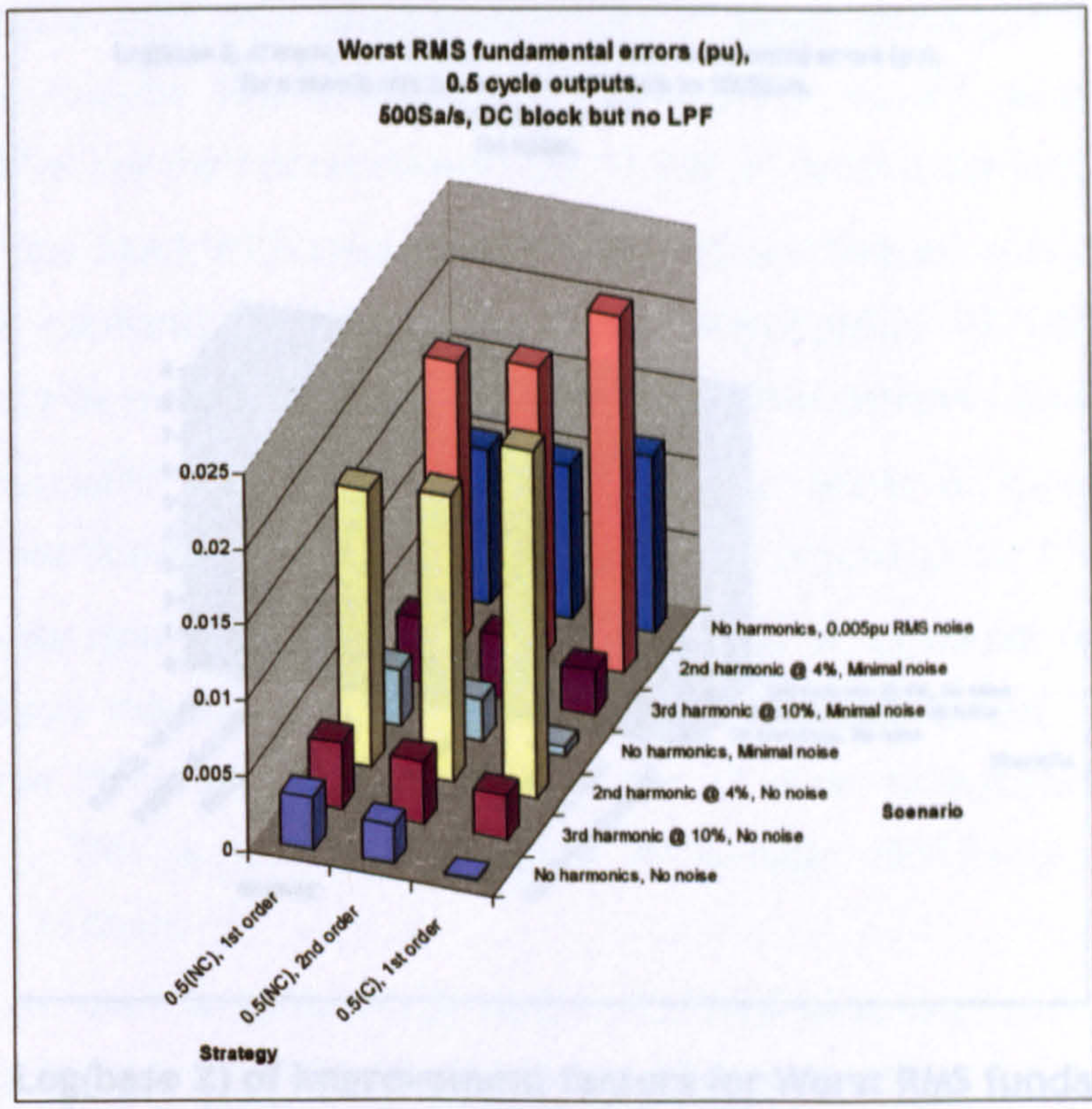


Figure 3-74 : RMS errors on the Fourier measurement of fundamental amplitude, 500Sa/s, 1/2-cycle latency measurements, all scenarios

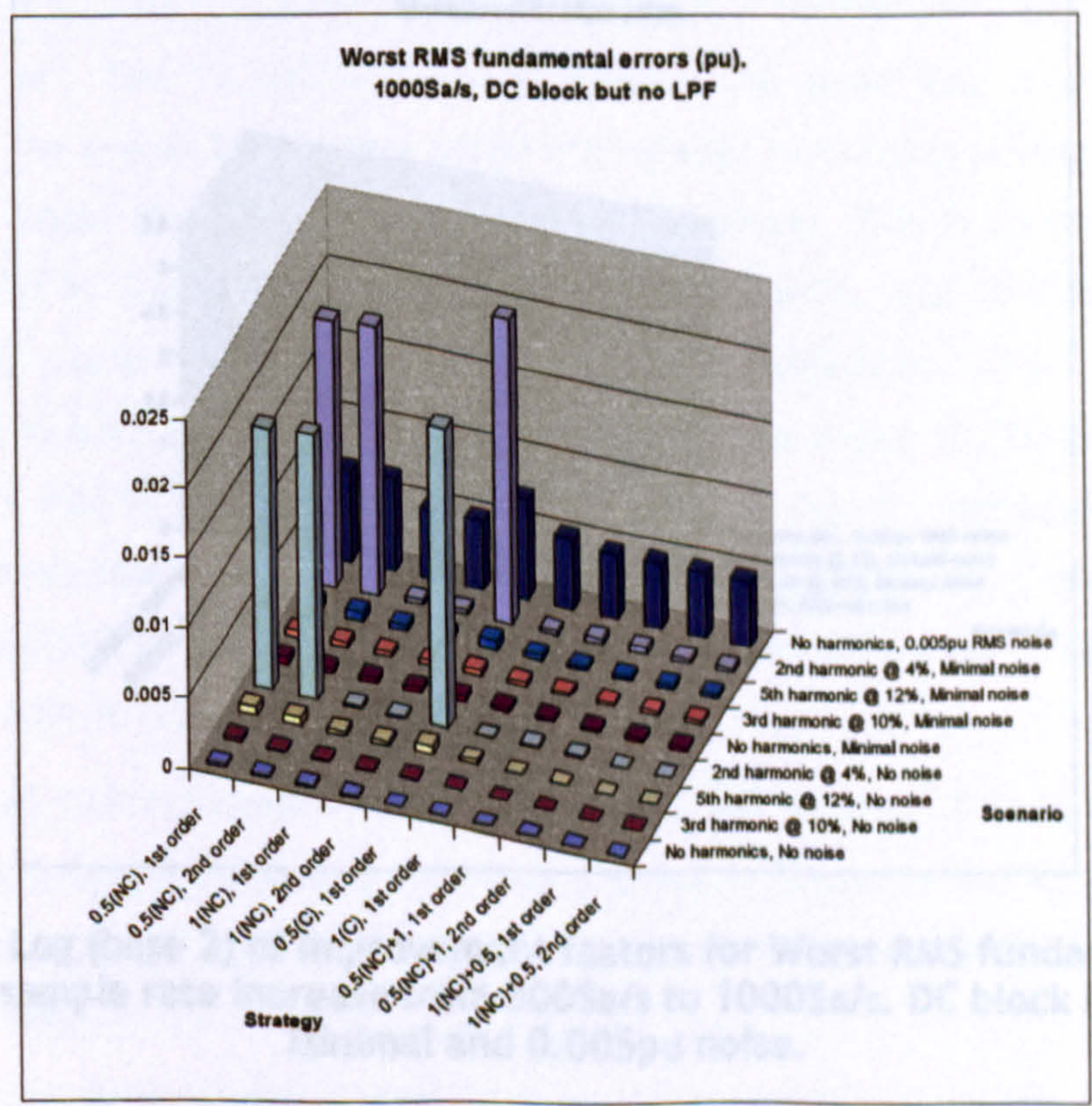


Figure 3-75 : RMS errors on the Fourier measurement of fundamental amplitude, 1000Sa/s, all viable options and scenarios

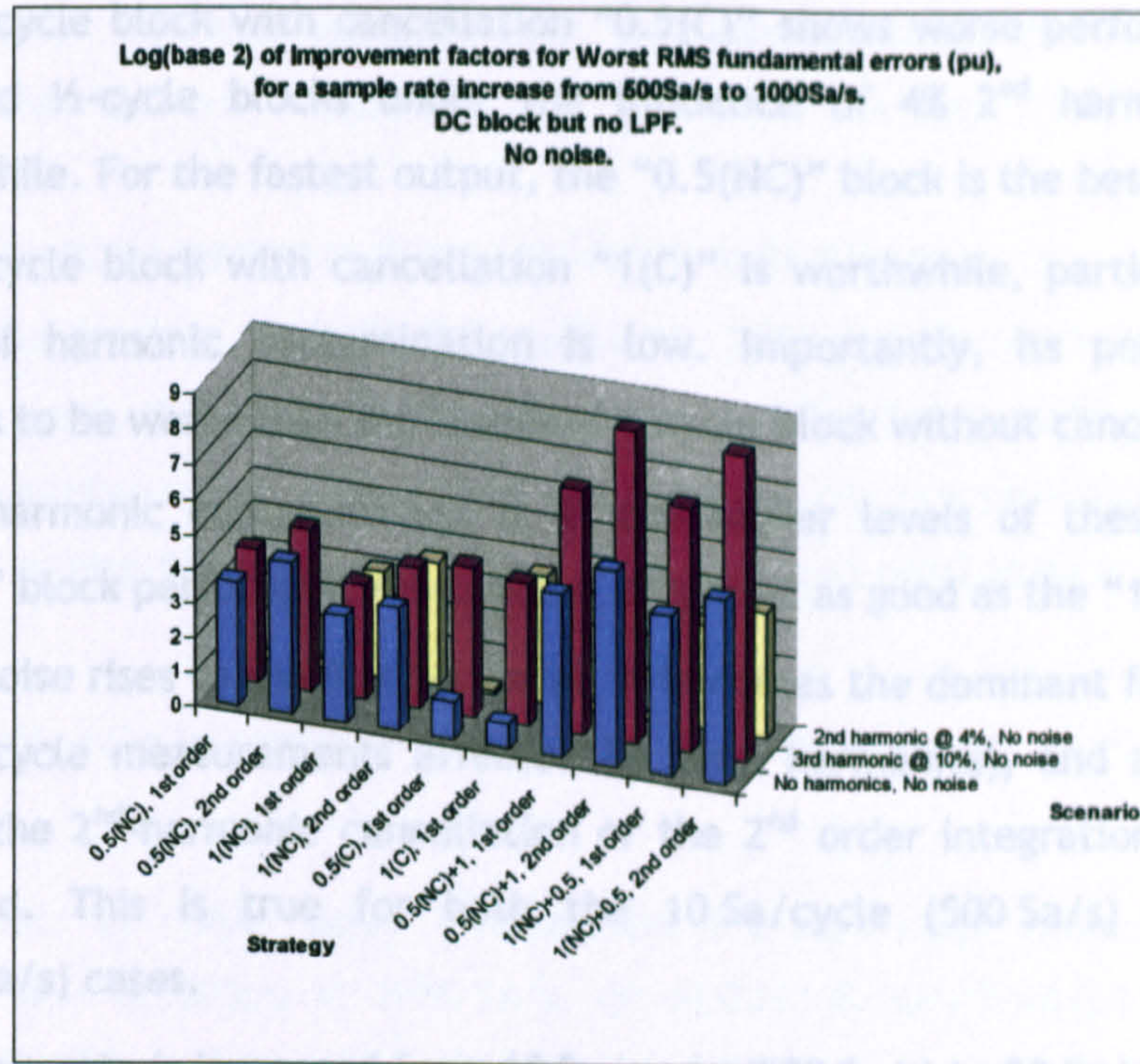


Figure 3-76 : Log(base 2) of Improvement factors for Worst RMS fundamental errors (pu), for a sample rate increase from 500Sa/s to 1000Sa/s. DC block but no LPF. No noise.

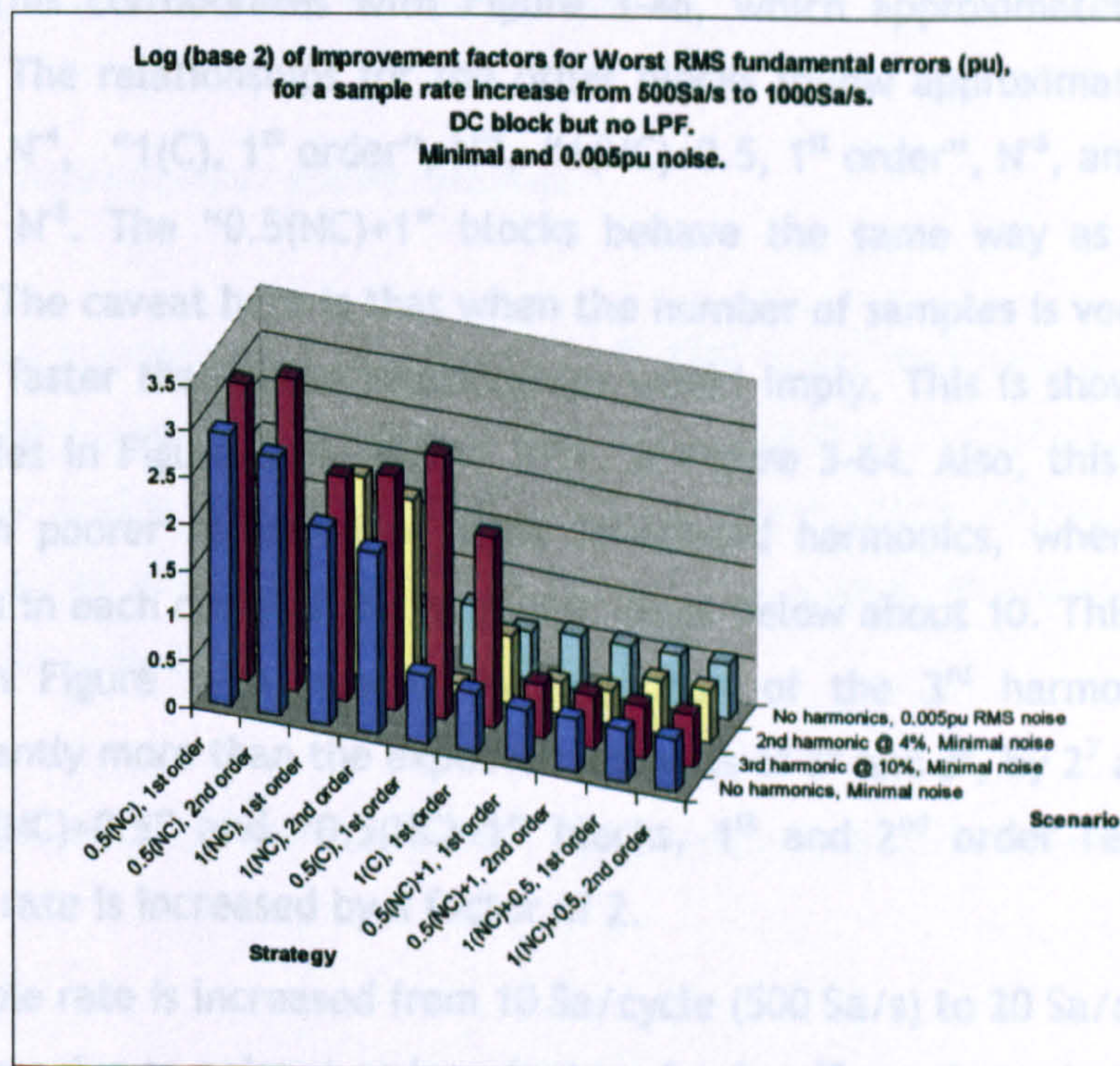


Figure 3-77 : Log (base 2) of Improvement factors for Worst RMS fundamental errors (pu), for a sample rate increase from 500Sa/s to 1000Sa/s. DC block but no LPF. Minimal and 0.005pu noise.

The data shown in Figure 3-70 to Figure 3-77, together with that of Figure 3-46, Figure 3-57, & Figure 3-64, enables some deductions to be made about the relative merits of the different measurement architectures:-

- The ½-cycle block with cancellation “0.5(C)” shows worse performance than the standard ½-cycle blocks under the influence of 4% 2nd harmonic, so is not worthwhile. For the fastest output, the “0.5(NC)” block is the best.
- The 1-cycle block with cancellation “1(C)” is worthwhile, particularly when the level of harmonic contamination is low. Importantly, its performance never appears to be worse than the standard 1-cycle block without cancellation “1(NC)”.
- When harmonic contamination is at the higher levels of these scenarios, the “1(NC)” block performance is as good, or almost as good as the “1(C)” blocks.
- When noise rises to the 0.005pu level, it becomes the dominant factor (apart from the ½-cycle measurements affected by even harmonics), and all advantages of either the 2nd-harmonic cancellation or the 2nd order integration/interpolation is removed. This is true for both the 10 Sa/cycle (500 Sa/s) and 20 Sa/cycle (1000 Sa/s) cases.
- As sample rate is increased from 10 Sa/cycle (500 Sa/s) to 20 Sa/cycle (1000 Sa/s), the magnitude of the integration/interpolation errors from the 1-cycle, 1st order, non-cancelled block “1(NC), 1st order” drop by a factor of ≈ 8 , i.e. as a function of $\approx N^3$. (This corroborates with Figure 3-46, which approximately follows an N^3 curve). The relationships for the other blocks follow approximately: “1(NC), 2nd order”, N^4 , “1(C), 1st order”, N^4 , “1(NC)+0.5, 1st order”, N^6 , and “1(NC)+0.5, 2nd order”, N^8 . The “0.5(NC)+1” blocks behave the same way as the “1(NC)+0.5” blocks. The caveat here is that when the number of samples is very low, the errors change faster than these relationships would imply. This is shown by slight non-linearities in Figure 3-46, Figure 3-57, & Figure 3-64. Also, this effect manifests itself in poorer rejection of some un-aliased harmonics, when the number of samples in each cycle of the harmonic drops below about 10. This effect shows up well on Figure 3-76, where the rejection of the 3rd harmonic improves by significantly more than the expected amounts of 2^6 and 2^8 , by 2^7 and 2^9 in fact, for the “1(NC)+0.5” and “0.5(NC)+1” blocks, 1st and 2nd order respectively, when sample rate is increased by a factor of 2.
- As sample rate is increased from 10 Sa/cycle (500 Sa/s) to 20 Sa/cycle (1000 Sa/s), the errors due to noise drop by a factor of only $\approx \sqrt{2}$, as the reduction is simply due to the number of samples in the averaging, and the application of the “random walk” effect.
- Therefore, as the number of sample-per-cycle N increases, the relative importance of the integration/interpolation errors compared to the noise errors decreases proportionately to at least $N^{2\frac{1}{2}}$ for the “1(NC), 1st order” block, and by even more than this for the more complex blocks. The exponent $2\frac{1}{2}$ here derives from the N^3

relationship between sample rate and interpolation error, times the \sqrt{N} relationship between sample rate and noise error, for the “1(NC), 1st order” block.

3.13.1 Selection process for algorithm selection

Gathering all the findings and all the algorithm CPU requirements from sections 3.6 through to this point, it is now possible to create a selection process, which provides a clear path to a decision about which set of algorithms to use in a particular application. To select the most appropriate algorithm, these four questions need to be answered:-

1. Is the sample rate less than 16 samples per cycle? (800 Sa/s @ 50 Hz)?
2. Is the effect of noise “small”? Guidelines are that noise should be $<0.001\text{pu}$ @ 500 Sa/s, or $<0.0002\text{pu}$ at 1000 Sa/s, or $<0.001/(R/500)^{2.5}$ where R is some other sample rate. The relationship with exponent 2½ was deduced amongst the findings in section 3.13. When noise is too large, the gain of the cancellation algorithms and 2nd order interpolation is lost. The noise is set by the quality of the instrumentation hardware, and is generally a fixed quantity.
3. Is ½ cycle measurement speed required?
4. Is a 1-cycle measurement speed required? AND is the harmonic content sometimes small? If the harmonic content is always bad (verging on BS EN 50160 violations) then the answer to this question is “No”. However, even within microgrids the harmonic content may be quite low, even if this is not true always. In this case, the answer to this question may be “Yes”

Now, use the flowchart in Figure 3-78 with the answers to questions 1-4 and complete the process.

The computational effort required to carry out the various algorithms varies by algorithm. For a full analysis, the reader should refer to sections 3.6 to 3.12 which describe the algorithms. A simplistic comparison of the computational effort can be made by comparing the numbers of “hard” maths functions required for each algorithm. In Table 3-3 below, the functions which are identified as “hard” are listed. These present significantly larger burdens on a CPU than multiplication/addition/subtraction processes (see also Appendix G).

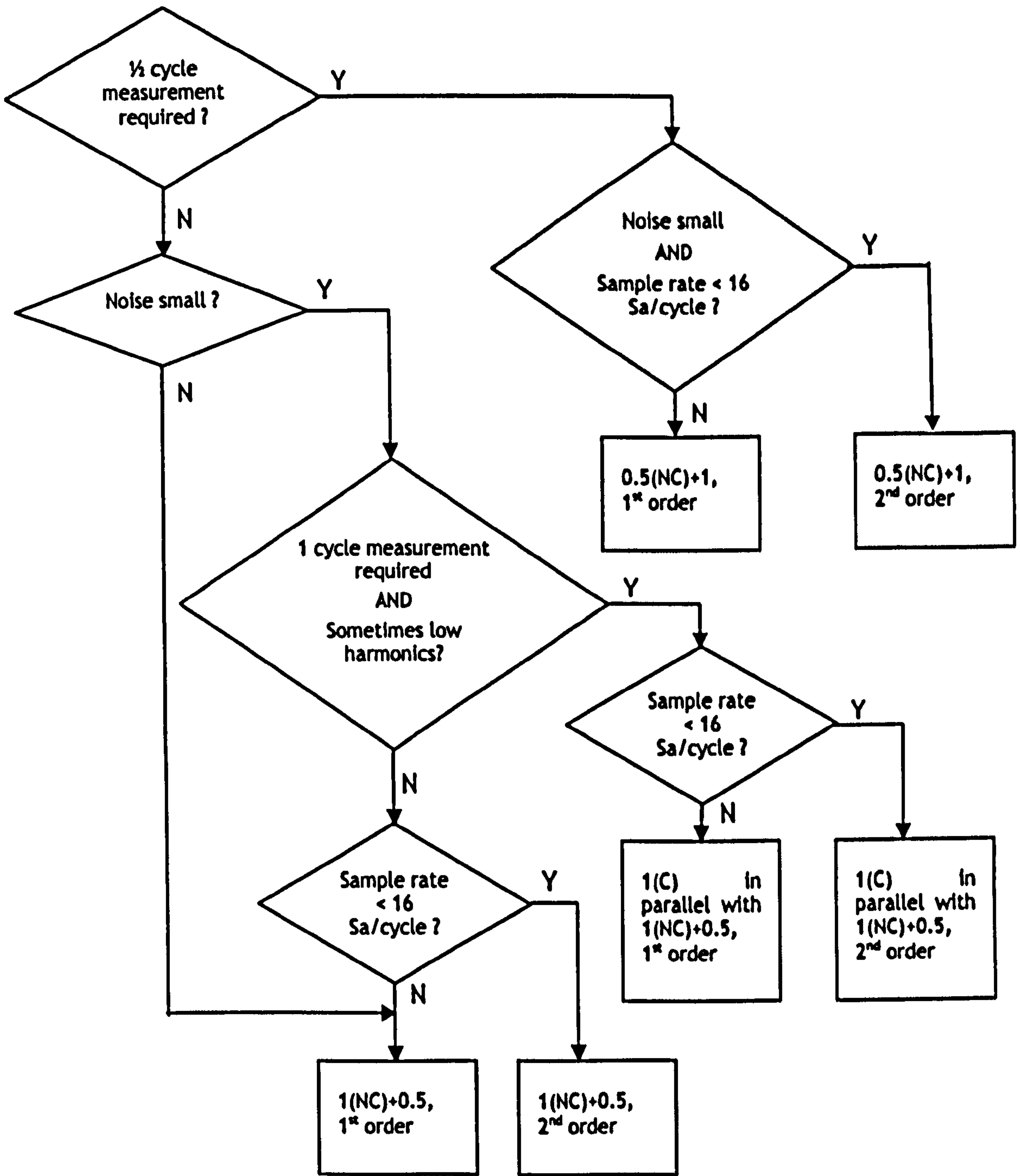


Figure 3-78 : Selection flowchart for measurement algorithm selection

sine/cosine/tangent
arcsin/arccos
atan/atan2
sqrt
x^y (y not Integer)
$e^x, \ln(x), 10^x, \log_{10}(x)$

Table 3-3 : "hard" maths functions

In Table 3-4, the number of these “hard” maths functions required for each algorithm (per measurement channel) is listed. The two columns describe the number of function evaluations required, both with all-harmonic RMS & THD calculations, and also for a stripped-down algorithm with the all-harmonic RMS & THD calculations removed. Note that all 2nd order algorithms have the same number of “hard” math functions as their 1st order counterparts, but that there are additional CPU operations required as described in section 3.2.2, so the 2nd order blocks should only be used where there is definite benefit.

For all the algorithms, the “Part A” data requires a “hard” math function count of 2 (sine and cosine) (see section 3.6). This is unavoidable, is common to all proposed measurement systems, and can be re-used for many measurement blocks at the same frequency. Therefore, it is not included in the counts of “hard” math functions below.

Algorithm	“Hard” math function count per measurement channel. including all-harmonic RMS and THD calculations	“Hard” math function count per measurement channel. without all-harmonic RMS and THD calculations
1(C) in parallel with 1(NC)+0.5, 2 nd order	8	6
1(C) in parallel with 1(NC)+0.5, 1 st order	8	6
1(NC)+0.5, 2 nd order	4	2
1(NC)+0.5, 1 st order	4	2
0.5(NC)+1, 2 nd order	4	2
0.5(NC)+1, 1 st order	4	2

Table 3-4 : “Hard” maths functions for different measurement algorithms

3.14 Final selection of algorithms for further development and testing in this thesis

The applications most of interest within the scope of this thesis are those with the following properties:-

- Voltage measurements (amplitude, phase, RMS, THD, frequency), at 500 Sa/s or slightly above, with measurement latencies of 1.5 to 5 cycles, in an environment where the noise level is currently ≈ 0.005 pu (significant), and harmonic contamination may be (but is not always) high. From Figure 3-78, the appropriate algorithm is therefore “1(NC)+0.5, 1st order”. With a lower noise level, the “1(NC)+0.5, 2nd order” algorithm might also become appropriate.

Therefore, the two most relevant blocks “1(NC)+0.5, 1st order” and “1(NC)+0.5, 2nd order” are explored further in the next section, and are also used as the prime building blocks within the frequency measurement algorithms of section 5. To remind the reader, these classifications translate as:-

- “1(NC)+0.5, 1st order” = A Fourier transformation over exactly 1 cycle, with no 2nd-harmonic cancellation, with a subsequent ½ cycle averaging of the results, using 1st order integration and interpolation techniques throughout.
- “1(NC)+0.5, 2nd order” = ditto, but using 2nd order integration and interpolation techniques throughout.

The next chapter goes on to deal with two further error mechanisms:-

- Errors due to inaccurate estimates of signal frequency
- Errors due to aliased harmonics

3.15 References for chapter 3

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4 Higher order harmonics and aliasing, and the effects of frequency measurement error

This chapter follows directly from the work of chapter 3. The topics covered are:

- Assessment of the algorithm performance due to frequency measurement error.
- Assessment of the algorithm performance against aliased harmonics, accounting for the actual performance of the anti-aliasing filters which do not remove all signal components above the nyquist frequency (see section 3.4.1).
- The response of the algorithm outputs under the influence of aliased harmonics is found to be a ripple, with a frequency which may be sub-fundamental. For measurements which can afford a longer measurement time than $1\frac{1}{2}$ cycles, a novel ripple-removal filter is designed, based yet again on the exact-time-period averaging blocks.
- Overall findings and guideline error-magnitude error levels are presented.
- To meet the toughest amplitude measurement ripple specifications at waveforms of up to 28-53% THD_v, with the main algorithm running at 10 samples per cycle (500 Sa/s), a digital oversampling at 3kHz and a simple 6-tap FIR filter is required at the front end. This filter is designed and tested with the whole algorithm to verify the improved performance. Methods to achieve this oversampling inside economical microcontroller solutions are described.

4.1 The effect of frequency measurement error

In the previous chapter, the measurement block inputs were fed with the test input signal, plus the actual signal frequency. This is possible in simulations where the input signal is synthesised directly. In real scenarios the frequency must be measured, and this measure of frequency will always be in error by some amount. The worst frequency error which would be expected from the measurement algorithms proposed in chapter 5, in the microgrid context, was defined by the requirements of Table 2-14. This worst reasonably expected error is caused by a 5-cycle response measurement, with a ROCOF rate of 10 Hz/s; this equates to $10 \cdot 5 / 50 = 1$ Hz for a 50 Hz system. To examine the effect of this magnitude of error on the amplitude/phase measurements, the simulation from the previous section 3.13 can be re-used. The only difference is that now a ± 1 Hz frequency error is introduced onto the estimate of frequency passed into the measurement algorithms. The resulting errors are shown below in Figure 4-1, compared to the errors resulting from pure sinusoid inputs and 0.005pu RMS noise (without frequency errors, from section 3.13) to give context.

Before analysing the chart, the results can be qualitatively described as follows:

- The result of the frequency measurement error is that the initial Fourier transformation block exhibits ripple. For the 1-cycle base Fourier measurement, this ripple is at exactly 2x the actual signal frequency. It was expected that this ripple might show up at a combination of mixed frequencies such as N times the frequency estimate \pm M times the actual signal frequency. However, careful analysis of the ripple using Fourier transformation confirms that the ripple is almost entirely confined to a single frequency at 2x the actual signal frequency (see Table 4-1), just as was the ripple due to interpolation. If the initial Fourier measurement base block is of $\frac{1}{2}$ -cycle duration, then the ripple is at the fundamental. Thus, the "1(NC)", "1(C)", and "0.5(NC)" base measurement block outputs all exhibit substantial ripple due to frequency measurement error. This effect was also noted by Moore (1996b), in a relay which could not adapt well to frequencies off-nominal due to processing limitations. Very small ripples also appear at 0 Hz and integer multiples of the signal frequency, but (somewhat surprisingly) ripples do not appear at, for example, the signal frequency \pm the frequency estimate. This is extremely useful since such ripples could have very low frequencies and be hard to remove.
- Due to the post-averaging stages, i.e. the extra $\frac{1}{2}$ -cycle averaging after the initial 1-cycle base block, the ripple is mostly removed. This works for both the "1+0.5" cycle and the "0.5+1" cycle systems. However, the ripple removal is not perfect because the ripple removal filter is also fed with the wrong measured frequency.

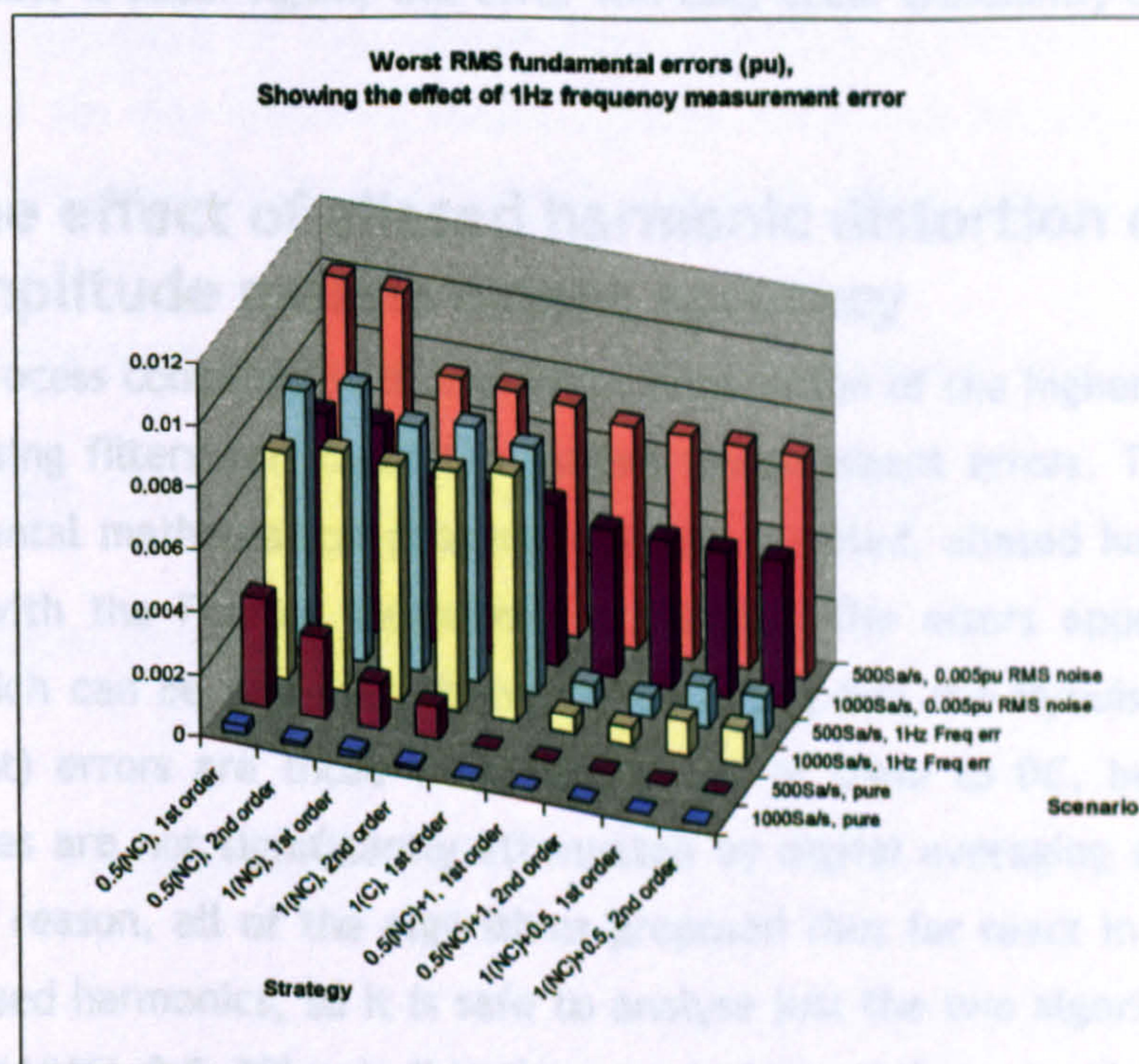


Figure 4-1 : Worst RMS errors on the measurement of fundamental amplitude, due to ± 1 Hz frequency measurement errors

Sample rate	Signal frequency	Frequency estimate	RMS Ripple magnitude	Ripple frequency
500 Sa/s	50	49	0.00717	100 Hz
500 Sa/s	51	50	0.00603	102 Hz
500 Sa/s	51	51	0.00114	102 Hz
500 Sa/s	52	51	0.00487	104 Hz
1000 Sa/s	52	51	0.00656	104 Hz

Table 4-1 : Ripple from 1-cycle Fourier measurement, due to frequency estimate error

The results show that the error magnitude due to frequency measurement error is not dependent upon the sample rate. The worst error magnitudes, at the outputs of the ½ and 1-cycle latency measurement blocks, are of the same order as the errors due to 0.005pu RMS noise for the 500Sa/s case. For higher sample rates, the error due to frequency measurement error becomes dominant over the effect of the 0.005pu RMS noise. This is because the error due to noise drops as $1/\text{SampleRate}$ whereas the error due to frequency measurement error stays constant. The worst error for the ½-cycle latency measurement block is 0.008pu RMS, which is acceptable, considering that this will only occur transiently during the fastest ROCOF events.

The worst error at the 1½-cycle outputs is only 0.0012pu RMS, which is of no concern. This shows that the second stages of averaging perform relatively well, even when the wrong frequency estimate is used. Again, this error will only occur transiently during the fastest ROCOF events.

4.2 The effect of aliased harmonic distortion on amplitude measurement accuracy

The sampling process combined with imperfect attenuation of the higher-order harmonics in the anti-aliasing filters can cause the largest measurement errors. These errors arise due to fundamental mathematical properties of the sampled, aliased harmonics and how they interact with the Fourier measurement process. The errors appear as ripples at frequencies which can be anywhere between 0 Hz (DC) and the Nyquist frequency. The worst (dominant) errors are those which appear at or close to DC, because these low frequency ripples are not significantly attenuated by digital averaging stages of 1 or 1½ cycles. For this reason, all of the algorithms proposed thus far react in almost the same way to the aliased harmonics, so it is safe to analyse just the two algorithms “1(NC)+0.5, 1st order” and “1(NC)+0.5, 2nd order” in the next section, and assume that the errors from aliased harmonics will be about the same for all the other algorithms proposed thus far.

To analyse the measurement errors due to aliased harmonics, it is possible to again use the same setup described in section 3.7. However, due to the combination of number of possible frequencies, samples per cycle and harmonic numbers, the required test run to gather all the data would take an unacceptably long time. To address this, the approximate errors are deduced mathematically, and the formulae cross-checked against the simulation to determine accuracy. From this, the most sensible values of samples-per-cycle to use (to attain optimum accuracy) can be much more quickly identified. For these optimal values, the harmonics which cause the worst effects can also be predicted and then analysed further using the full simulation.

One point should be reinforced here. In the error analyses below, if the interfering harmonic is at a frequency which is an integer multiple of the fundamental frequency (which it usually is), then measurement error and ripple will be zero if the harmonic is not aliased (aside from interpolation error). The errors, however, are not zero when the original harmonic is aliased due to sampling. This occurs if the harmonic frequency is above the Nyquist frequency. The harmonic then appears in the digital domain as a signal which is not at an integer multiple of the fundamental frequency.

4.2.1 Theoretical aliasing effects and ripple frequency of the Fourier and RMS measurements due to harmonic contamination

If the sampling frequency of the measurement device is f_s , in Sa/s, then the Nyquist frequency is $f_s/2$ Hz. Any harmonic which appears above this frequency will be aliased upon sampling. The frequency at which the alias appears in the digitally sampled data can be calculated as follows:

Imagine an incoming harmonic at frequency f_h , which is above the nyquist frequency $f_s/2$.

Set $p = \frac{f_h}{f_s}$ modulo 1 (modulo being the real-number remainder function)

Now, find the aliased frequency f_a by

$$f_a = f_s(1 - p) \quad \text{if } p > 0.5$$

$$f_a = f_s p \quad \text{otherwise}$$

$$\text{and } \omega_a = 2\pi f_a$$

(4.1)

An example of this effect is if $f_s = 500$ Sa/s, with a fundamental f_f at 50 Hz (10 samples per

cycle), then the 11th harmonic at $f_h=550\text{Hz}$ will result in $p=550/500$ modulo 1 which equals 0.1, resulting in an aliased frequency f_a of $500 \cdot 0.1=50\text{ Hz}$ which exactly overlies the fundamental.

The expected ripple frequency of the Fourier and RMS measurement ripples described in sections 4.2.2 and 4.2.3 will be:-

$f_{\text{ripple}} = |f_f - f_a|$ where f_a is the aliased frequency resulting from the actual harmonic at frequency f_h , and f_f is the fundamental frequency of the main waveform.

As in the example above, when $f_f=f_a$ then f_{ripple} is 0. In this special case, a ripple is not seen but a constant (DC) error appears on any measurements.

4.2.2 Theoretical effect of harmonic and inter-harmonic distortion on measurement of the Fourier fundamental.

The Fourier measurement of the fundamental component is made by correlating the measured waveform against a sine/cosine pair at the fundamental frequency f_f ($\omega_f=2\pi f_f$). In the analysis, we only need to consider the sin component since the phase can be set such that the cosine component is zero due to symmetry.

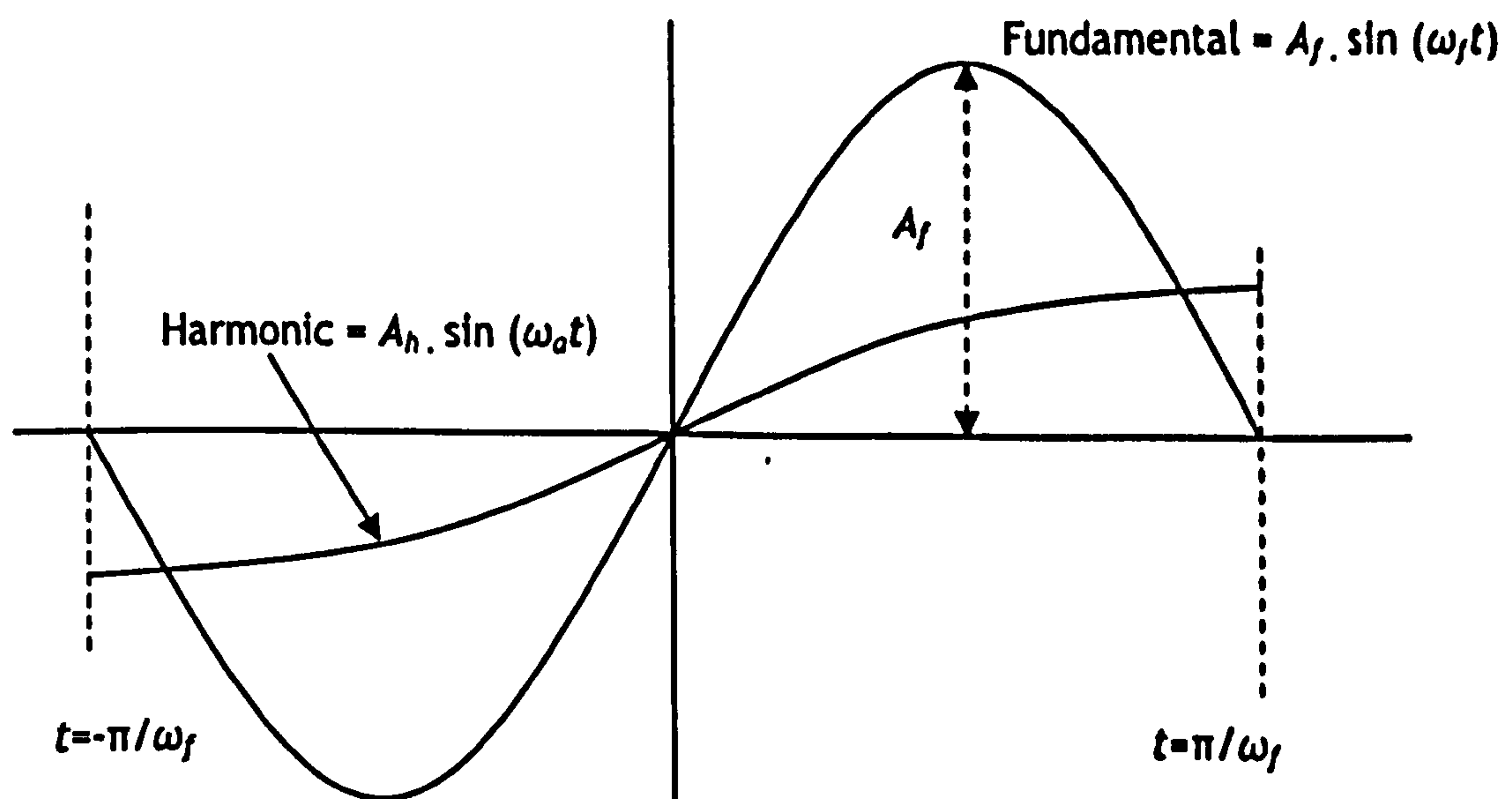


Figure 4-2 : Derivation of the formula for fundamental amplitude errors due to a harmonic, sub-harmonic or inter-harmonic

The fundamental component magnitude (at ω_f) is calculated as

$$A_{f_meas} = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} y(t) \cdot \sin(\omega_f t) \cdot dt$$

$$T = \frac{2\pi \cdot N}{\omega_f}$$

Where $y(t)$ is the measured waveform and N is the integer number of whole cycles. N is normally 1, but can be more to reduce noise at the expense of latency.

It is useful here to define K , since this allows simplification of the subsequent equations.

$$K = \frac{\omega_f}{N\pi} = \frac{2}{T}$$

(4.2)

The worst case for harmonic addition is when the aliased harmonic is most correlated with the fundamental, with the zero crossings aligned as shown in Figure 4-2. In this instance, the contribution to A_{f_meas} due to the harmonic at amplitude A_h , with (aliased) frequency f_a ($\omega_a = 2\pi f_a$), will be:

$$A_{f_meas} = K \int_{-\frac{1}{K}}^{\frac{1}{K}} A_h \cdot \sin(\omega_a t) \cdot \sin(\omega_f t) \cdot dt$$

This can be solved by using the identity $\sin(a) \cdot \sin(b) = \frac{1}{2}(\cos(a-b) - \cos(a+b))$ to give

$$A_{f_meas} = K \cdot A_h \cdot \left(\left(\frac{\sin\left(\frac{\omega_a - \omega_f}{K}\right)}{(\omega_a - \omega_f)} \right) - \left(\frac{\sin\left(\frac{\omega_a + \omega_f}{K}\right)}{\omega_a + \omega_f} \right) \right)$$

This expression may be re-expressed in terms of frequency f instead of ω as follows:

$$K_{freq} = \frac{f_f}{N\pi} = \frac{K}{2\pi}$$

$$A_{f_meas} = K_{freq} \cdot A_h \cdot \left(\left(\frac{\sin\left(\frac{f_a - f_f}{K_{freq}}\right)}{(f_a - f_f)} \right) - \left(\frac{\sin\left(\frac{f_a + f_f}{K_{freq}}\right)}{f_a + f_f} \right) \right)$$

The resulting per-unit error on the measurement of fundamental amplitude can be calculated by setting A_h to the per-unit amplitude of the interfering harmonic (e.g. 0.05 for 5%), and calculating the absolute value of A_{f_meas} .

4.2.3 Theoretical effect of harmonic and inter-harmonic distortion on measurement of the all-harmonic RMS value.

The all-harmonic RMS measurement of the input waveform is made by a standard RMS process on the waveform. The worst cases are where the interfering harmonic peaks (or troughs) coincide with the peaks of the fundamental waveform.

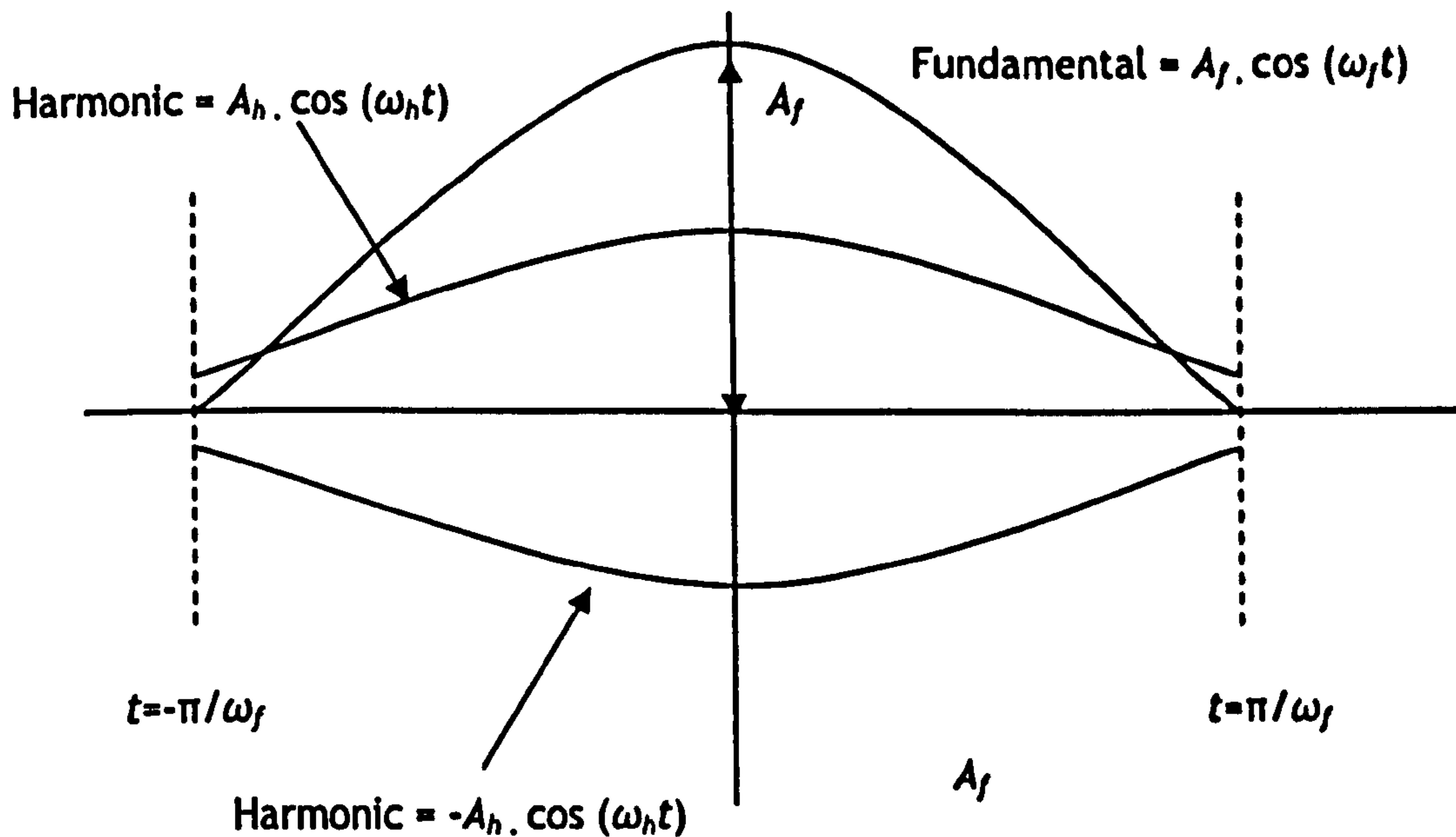


Figure 4-3 : Derivation of the formula for fundamental amplitude errors due to a harmonic, sub-harmonic or inter-harmonic

The RMS magnitude is calculated as A_{RMS_meas} , which here we wish to give the peak value of the real waveform; i.e. we would wish $A_{RMS_meas} = A_f$ if there were no harmonics present. Thus, there is a factor of $\sqrt{2}$ in the equation below, which does not appear in (3.7). This accounts for the transformation from RMS to peak values.

$$A_{RMS_meas} = \sqrt{2} \sqrt{\frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} y^2(t) \cdot dt} = \sqrt{\frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} y^2(t) \cdot dt}$$

$$T = \frac{2\pi \cdot N}{\omega_f}$$

Where $y(t)$ is the measured waveform, and N is the integer number of whole cycles. N is normally 1, but can be more to reduce noise at the expense of latency.

It is useful here to define K , since this allows simplification of the subsequent equations.

$$K = \frac{\omega_f}{N\pi} = \frac{2}{T}$$

(4.3)

The worst case for harmonic addition is when the peaks and troughs of the fundamental and the interfering harmonic are aligned as shown in Figure 4-3. The alignment of peaks is considered below. The alignment of a peak with a trough can be considered later with the same equations but by using a negative value of A_h . In this instance, the final answer A_{RMS_meas} due to the fundamental at f_f , A_f plus the harmonic at amplitude A_h , (aliased) frequency f_a ($\omega_a = 2\pi f_a$), will be:

$$A_{RMS_meas} = \sqrt{\frac{1}{K} \int_{\frac{1}{K}}^{\frac{1}{K}} (A_f \cdot \cos(\omega_f t) + A_h \cdot \cos(\omega_a t))^2 \cdot dt}$$

This can be solved by expanding and using the identities $\cos^2(a) = \frac{1}{2}(1 + \cos(2a))$ & $\cos(a) \cdot \cos(b) = \frac{1}{2}(\cos(a+b) + \cos(a-b))$ to give

$$A_{RMS_meas} = \sqrt{A_f^2 + A_h^2 \left(1 + \frac{K \sin\left(\frac{2\omega_a}{K}\right)}{2\omega_a} \right) + 2KA_f A_h \left(\frac{\sin\left(\frac{\omega_f + \omega_a}{K}\right)}{\omega_f + \omega_a} + \frac{\sin\left(\frac{\omega_f - \omega_a}{K}\right)}{\omega_f - \omega_a} \right)}$$

is expression may be re-expressed in terms of frequency F instead of ω as follows:

$$K_{freq} = \frac{f_f}{N\pi} = \frac{K}{2\pi}$$

$$A_{RMS_meas} = \sqrt{A_f^2 + A_h^2 \left(1 + \frac{K_{freq} \sin\left(\frac{2f_a}{K_{freq}}\right)}{2f_a} \right) + 2K_{freq} A_f A_h \left(\frac{\sin\left(\frac{f_f + f_a}{K_{freq}}\right)}{f_f + f_a} + \frac{\sin\left(\frac{f_f - f_a}{K_{freq}}\right)}{f_f - f_a} \right)}$$

The per-unit error can be calculated by setting A_f to 1, and A_h to the per-unit amplitude of the interfering harmonic (e.g. 0.05 for 5%), and calculating the value of A_{RMS_meas} . The error is the absolute difference between of A_{RMS_meas} and the actual RMS value which can be calculated as

$$A_{RMS_actual} = \sqrt{A_f^2 + A_h^2} = \sqrt{1 + A_h^2} \text{ when } A_f \text{ is set to 1.}$$

The per-unit RMS errors are thus

$$A_{RMS_error} = \left| \sqrt{1 + A_h^2} - A_{RMS_meas} \right| \text{ with } A_f \text{ set to 1.}$$

Note that for each harmonic frequency and amplitude, A_h should be set to both the +ve and -ve value for the harmonic amplitude of interest, and the worst case result taken.

4.2.4 Comparison of theoretical to simulated results for harmonic contamination

Using the formulae derived in sections 4.2.1 through 4.2.3, the following 3 predictions were made (Figure 4-4 to Figure 4-6). The scenario here is:-

- Nominal frequency 50Hz
- 10 Samples per cycle (500 Sa/s)
- 11th harmonic added, at 0.035pu (the BS EN 50160 (BSI, 2000) specification). The harmonic is not considered in this example to be attenuated by any low-pass anti-alias filter.
- Actual input frequency varied from 45 to 55Hz
- Measurements made over 1 whole cycle

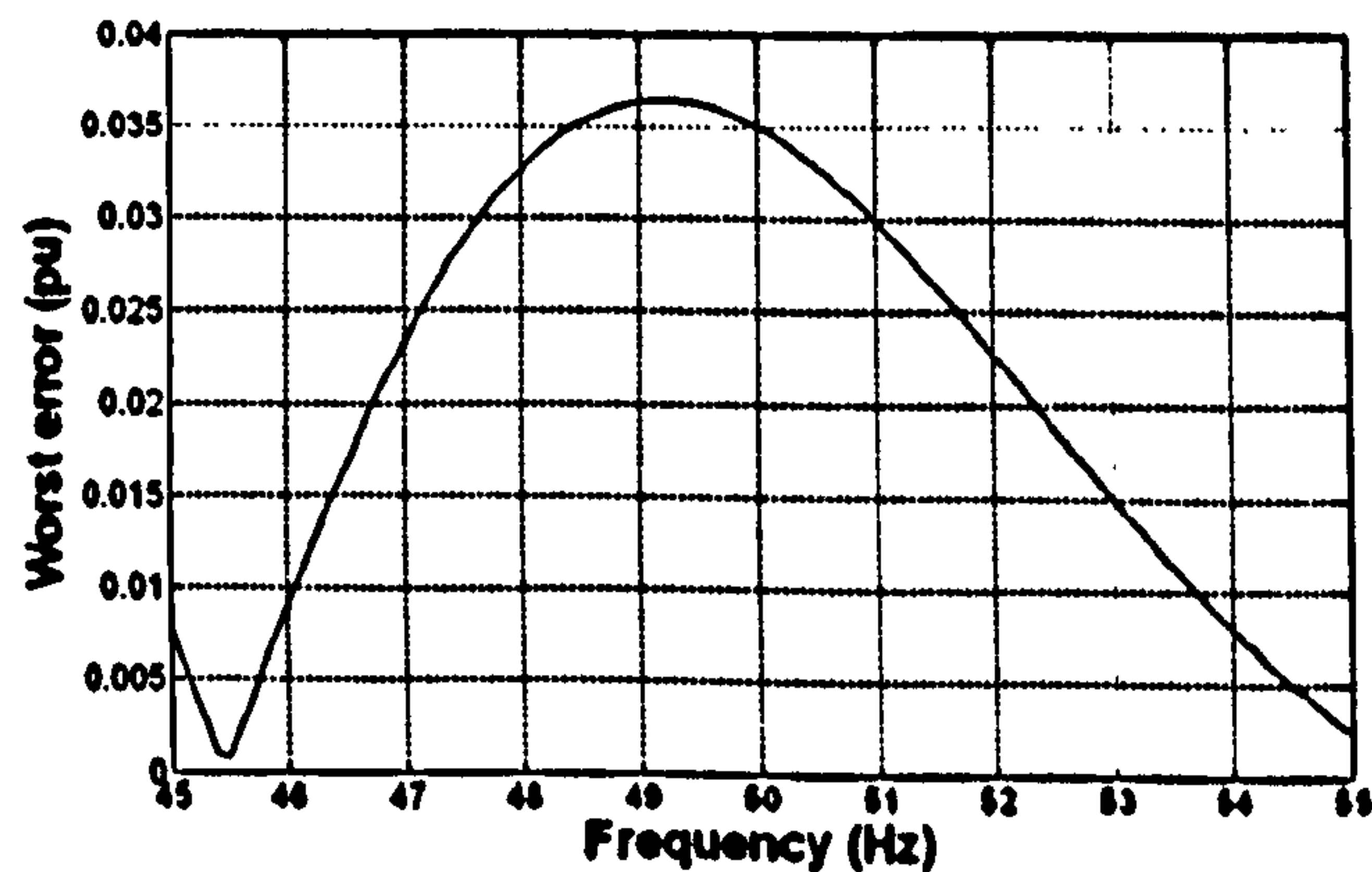


Figure 4-4 : Prediction of errors on the Fourier fundamental measurement at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz

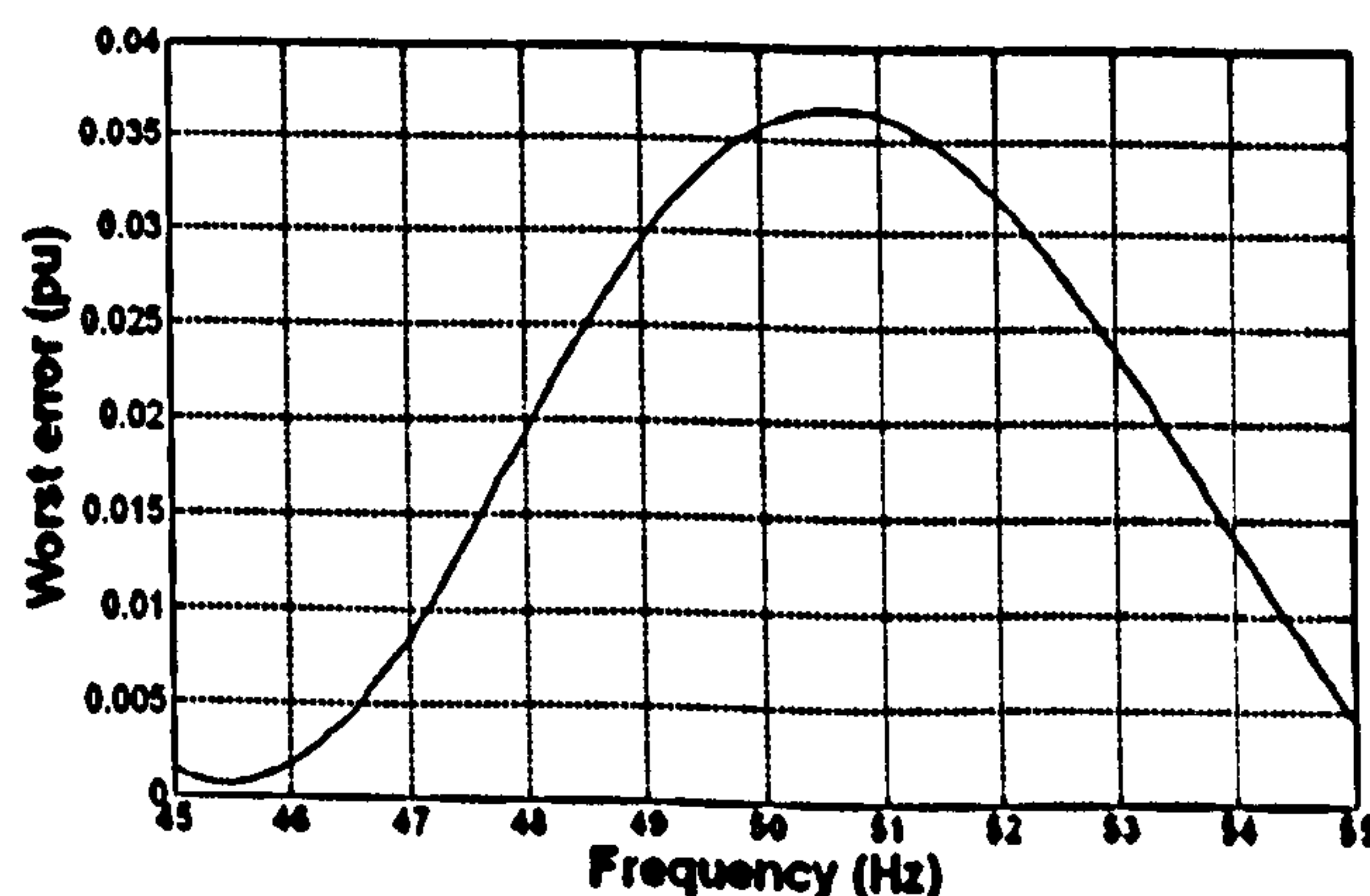


Figure 4-5 : Prediction of errors on the all-harmonic RMS measurement at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz

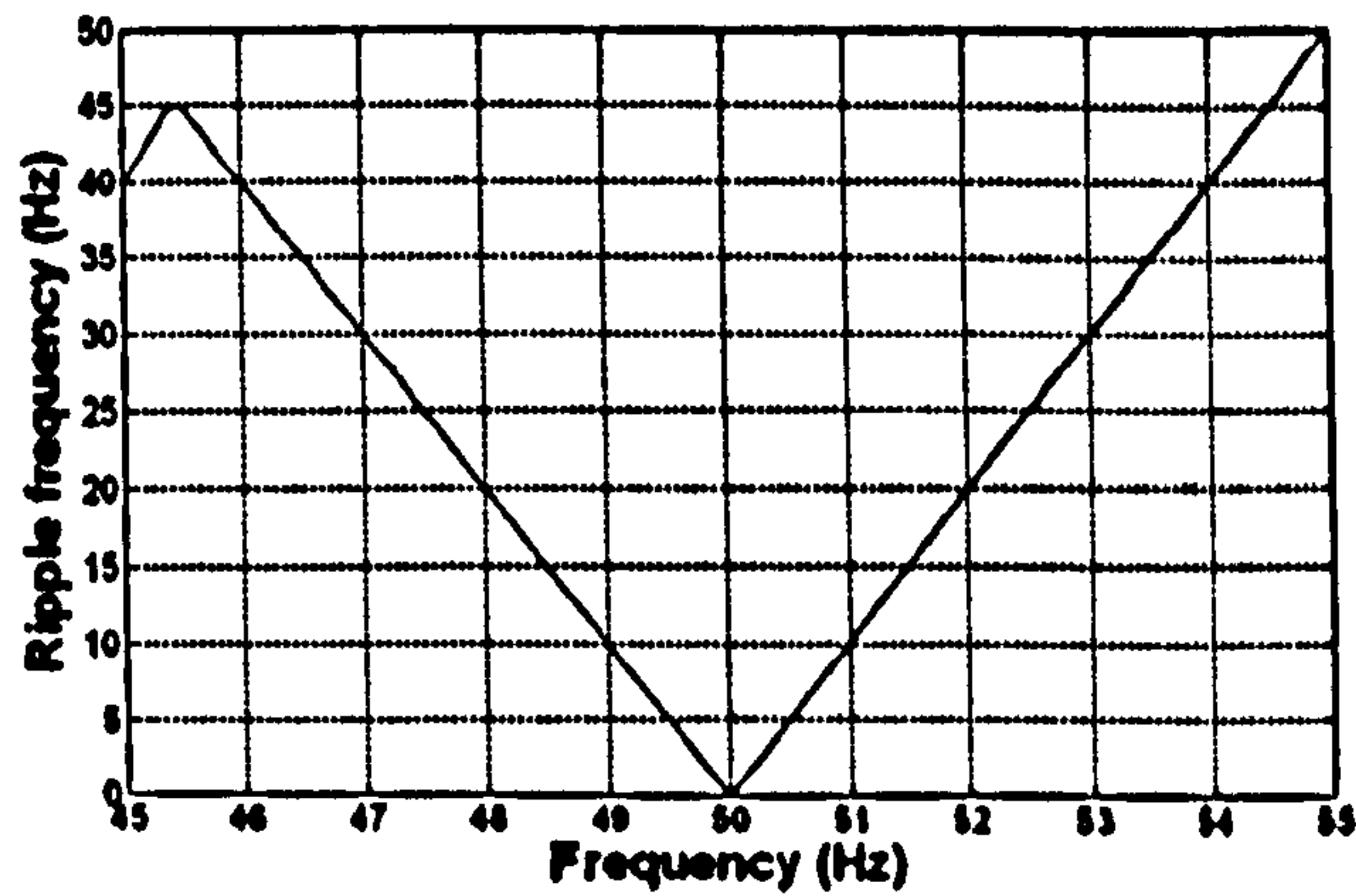


Figure 4-6 : Prediction of ripple frequencies on measurements at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz

A set of simulations using the model/test script described in section 3.7 produces the following graphs. Both 1st and 2nd order interpolation/integration algorithm results (see sections 3.2.2 and 3.7) are shown in the graphs below. They produce very similar results in the scenarios presented here, because the potential errors due to aliased harmonics are larger than the interpolation & integration errors. The ripple frequencies (Figure 4-9) match those predicted (Figure 4-6) exactly. The magnitude and shape of the error plots matches well, but not exactly. This is due to additional properties of the actual measurement algorithms which are not predicted by the theoretical alias analysis. The most important of these properties are the integration and interpolation errors which interact with the interfering harmonic. These errors have been thoroughly investigated in section 3.7. Although the match of Figure 4-4 & Figure 4-5 to Figure 4-7 & Figure 4-8 is thus not perfect, it is good enough to justify use of the mathematical models to predict the approximate magnitudes of errors, and for what input frequencies they will appear at different sample rates. This is extremely useful as a design tool, as will be seen in section 4.2.5.

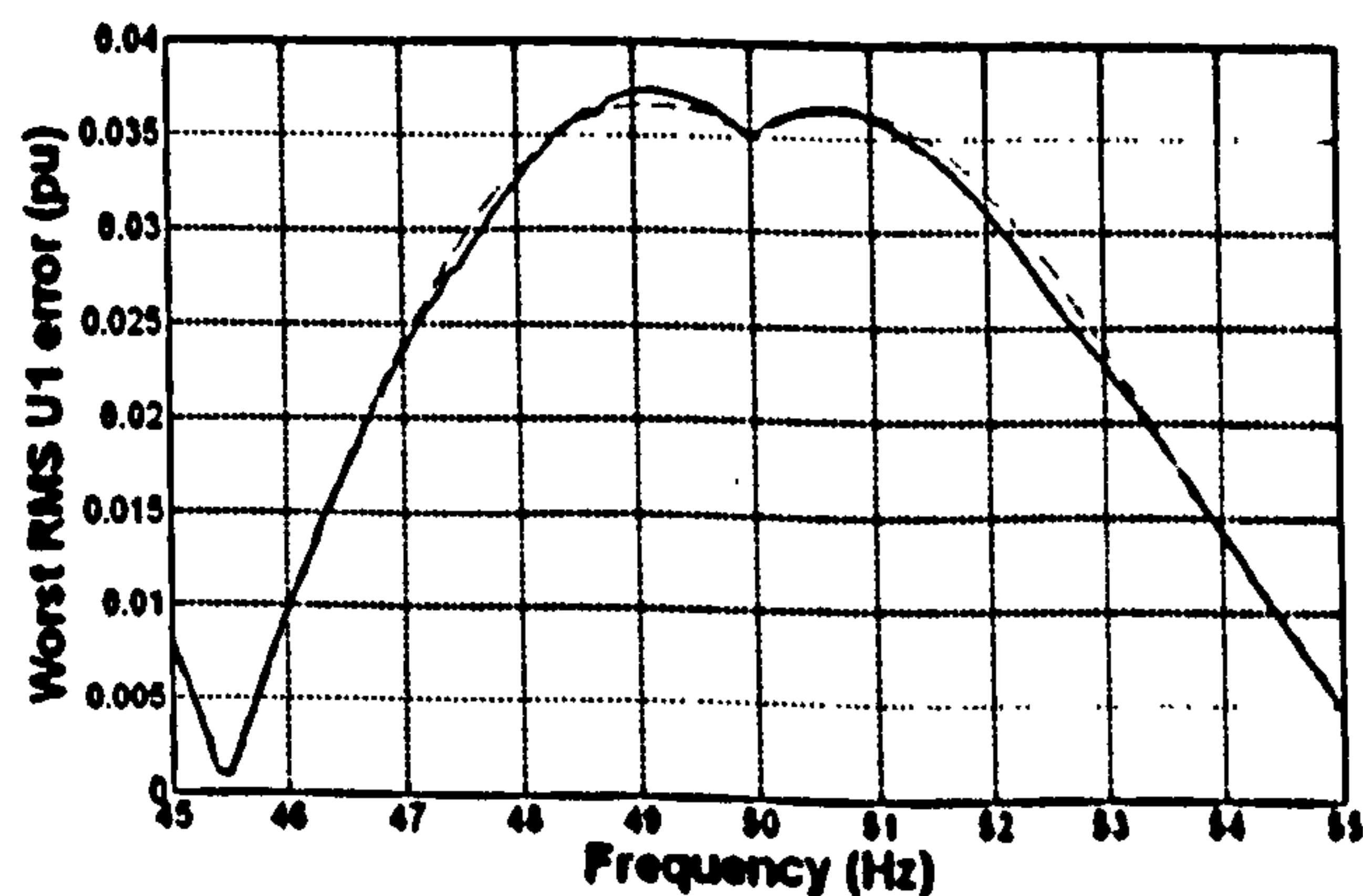


Figure 4-7 : Simulation of errors on the Fourier fundamental measurement at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz. 1st order (solid) and 2nd order (red dashes) methods

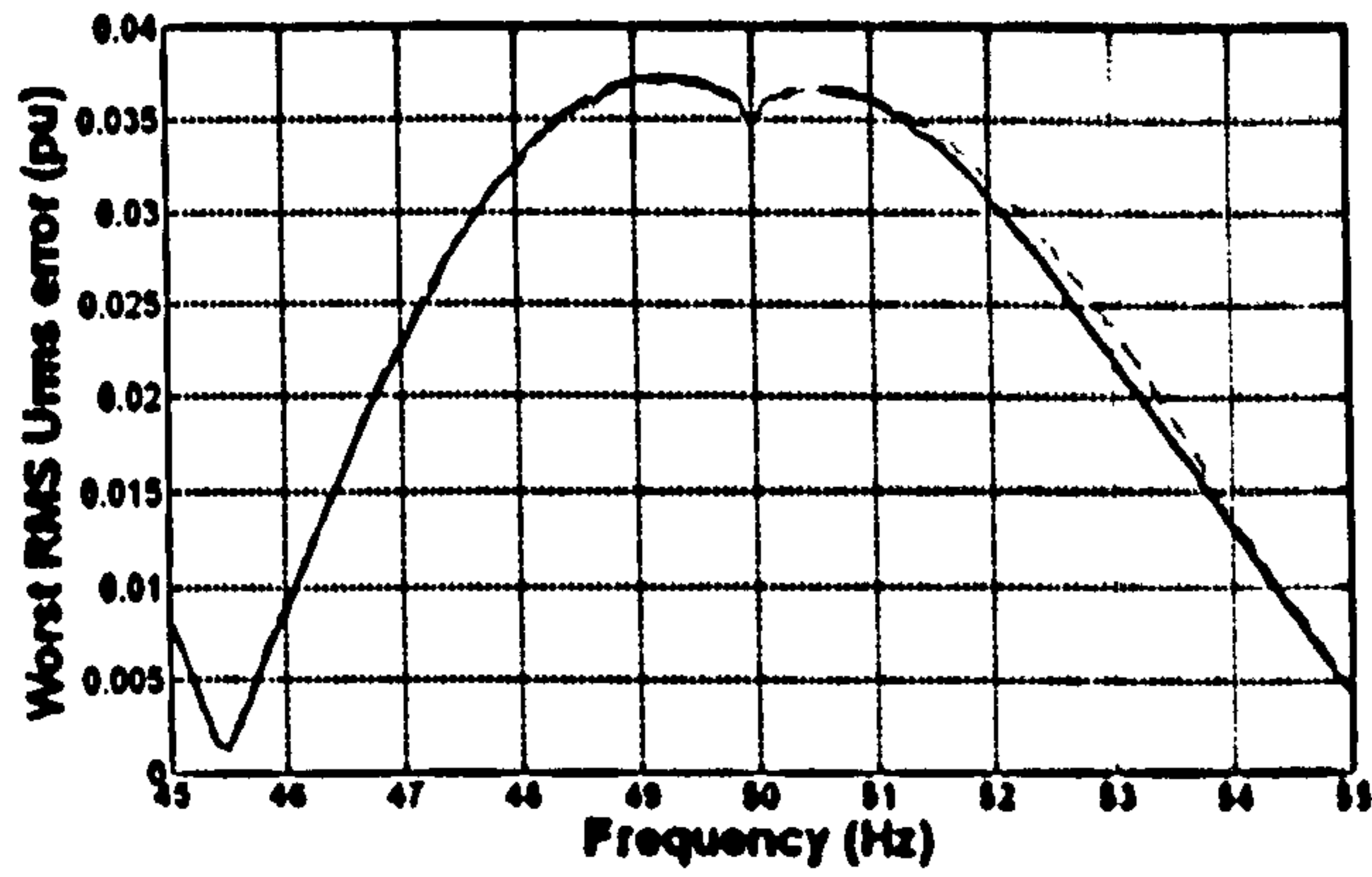


Figure 4-8 : Simulation of errors on the all-harmonic RMS measurement at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz. 1st order (solid) and 2nd order (red dashes) methods

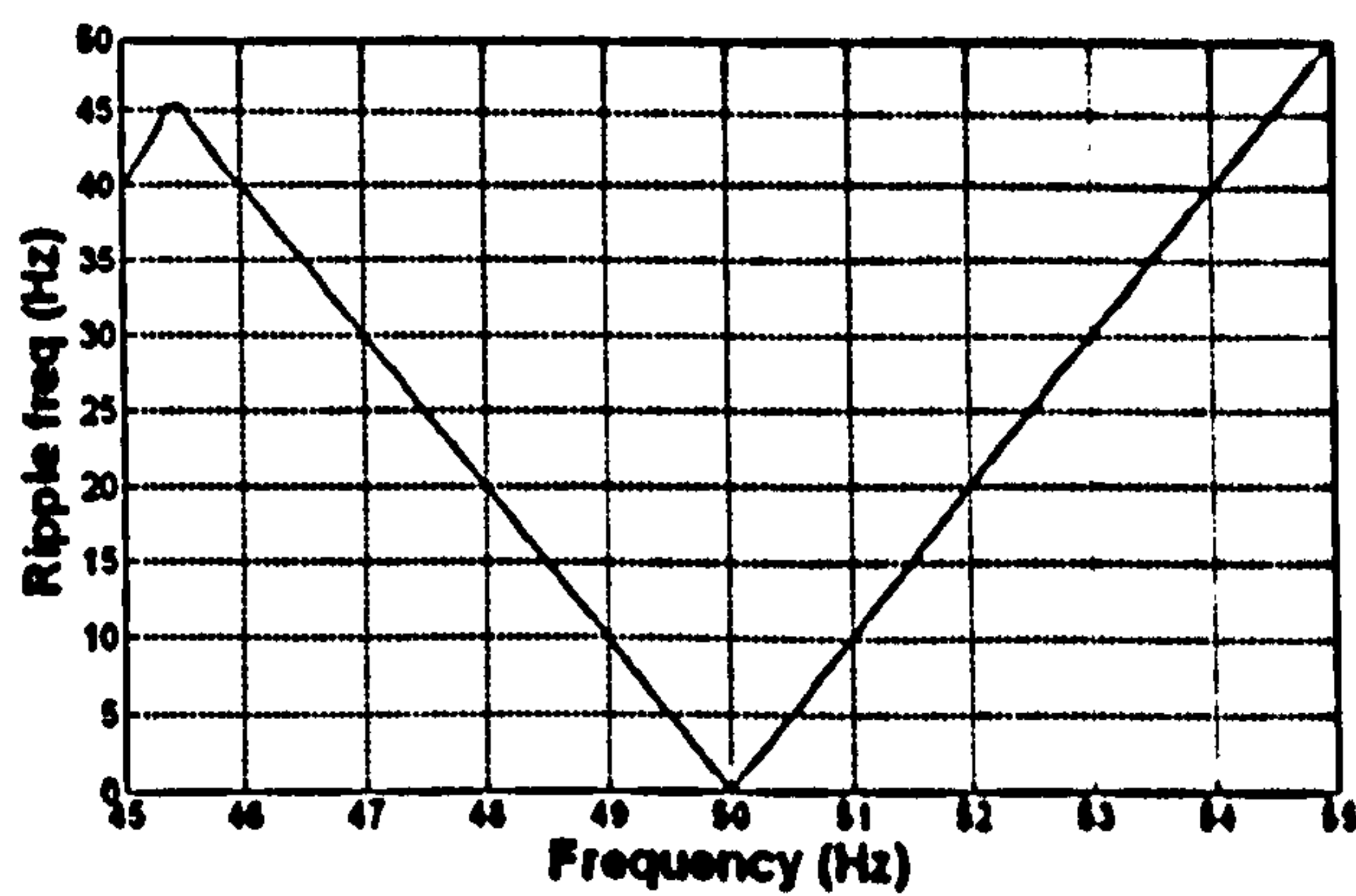


Figure 4-9 : Simulation of ripple frequencies on measurements at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz.

To double-check the quality of the agreement between prediction and simulation, the prediction software was used to predict that the 23rd harmonic would cause an appreciable effect at 26 samples per cycle. This is just one interesting combination picked from a choice of many. With the 23rd harmonic at the 1.5% level as per BS EN 50160 (BSI, 2000), the predictions for errors are shown in Figure 4-10 and Figure 4-11.

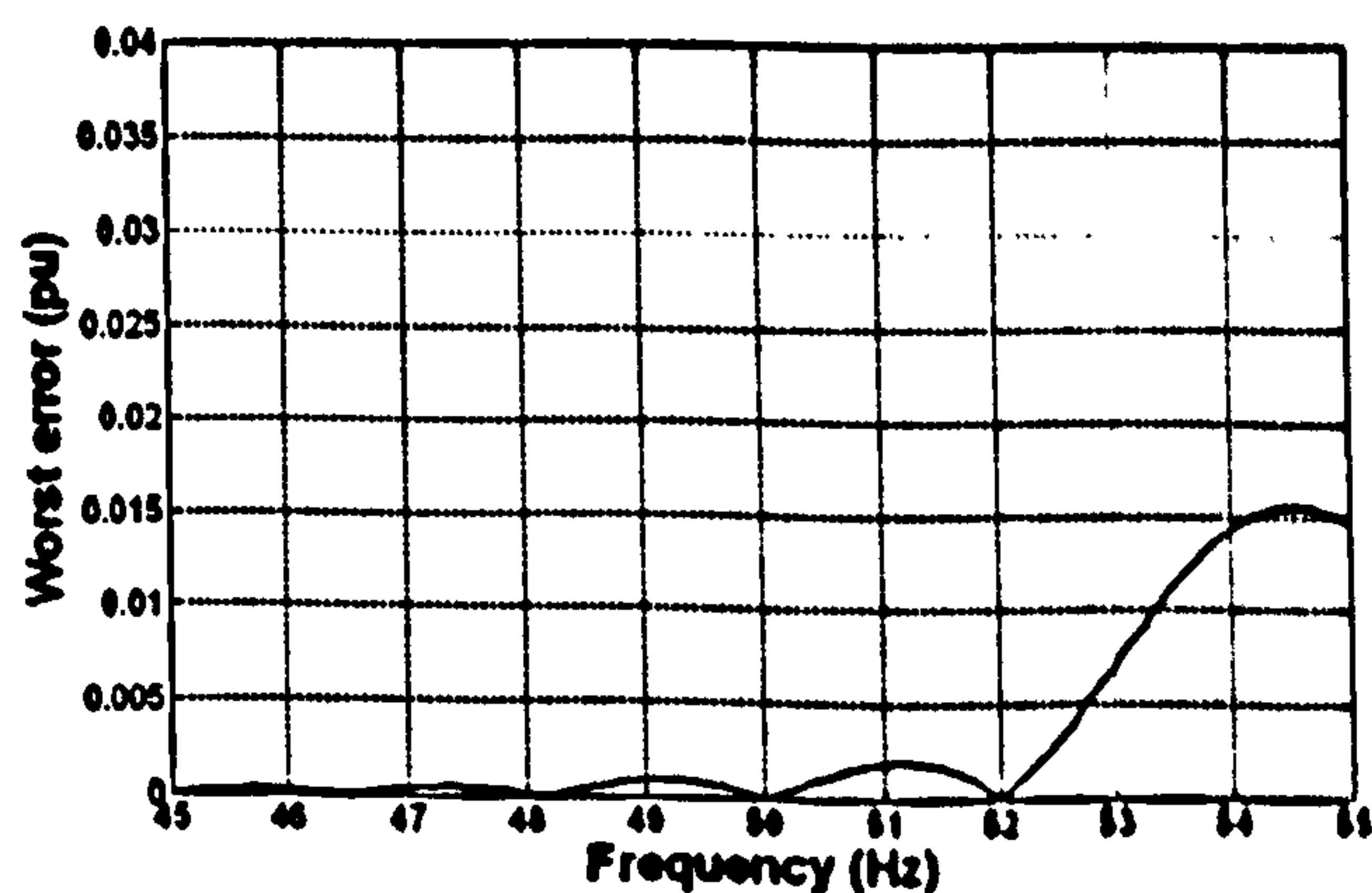


Figure 4-10 : Prediction of errors on the Fourier fundamental measurement at 1300Sa/s due to 23rd harmonic @ 1.5%, for input frequencies in the range 45-55Hz

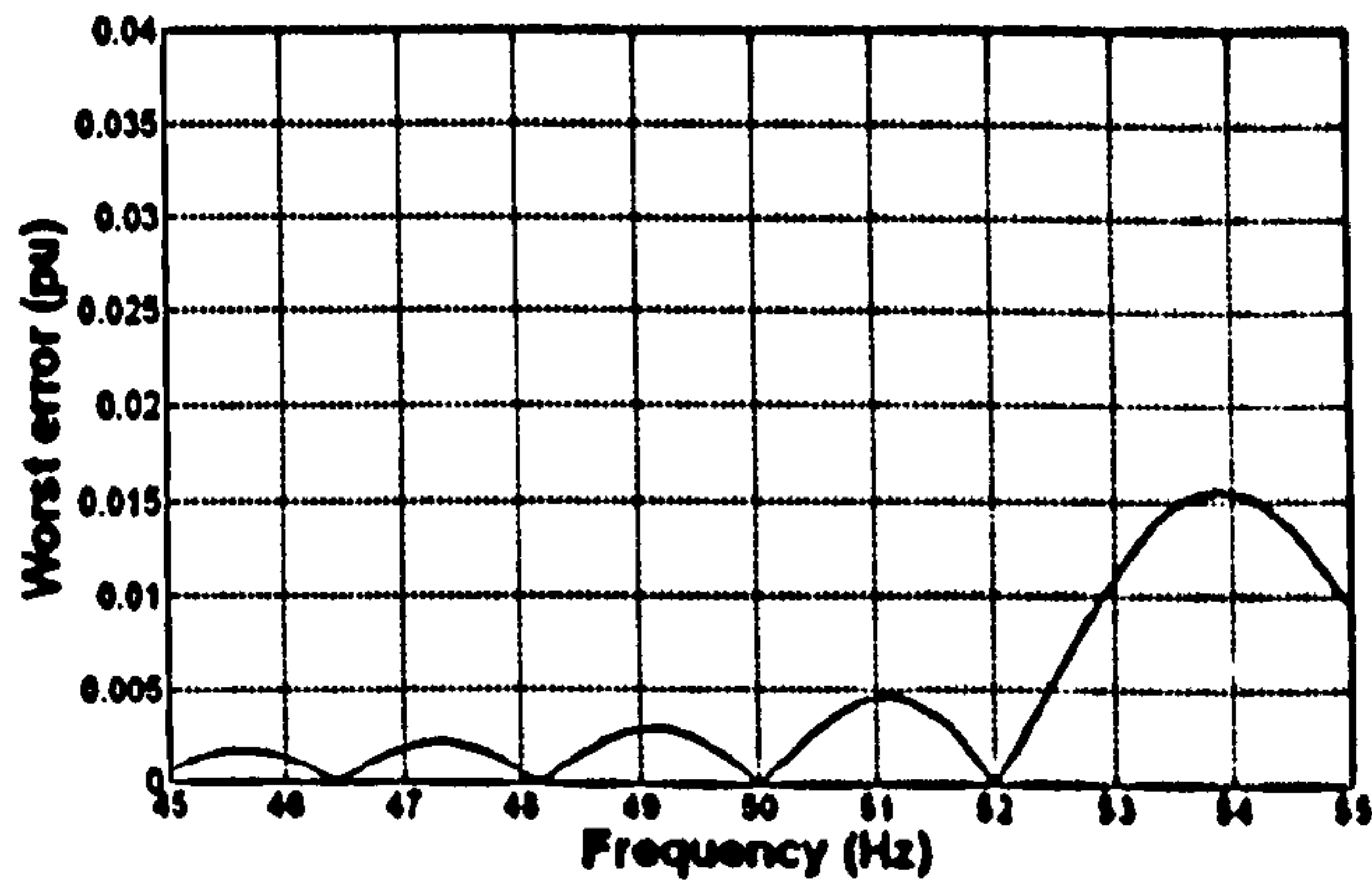


Figure 4-11 : Prediction of errors on the all-harmonic RMS measurement at 1300Sa/s due to 23rd harmonic @ 1.5%, for input frequencies in the range 45-55Hz

The simulated results are shown below in Figure 4-12 and Figure 4-13. The agreement between prediction (Figure 4-10 & Figure 4-11) and actual simulation is again good. This provides more evidence that the prediction tools (which execute much more quickly than the simulation sets) are valid. This means that the prediction tools can be used to predict error levels for given scenarios of sample rate and harmonic contamination. This is carried out in section 4.2.5.

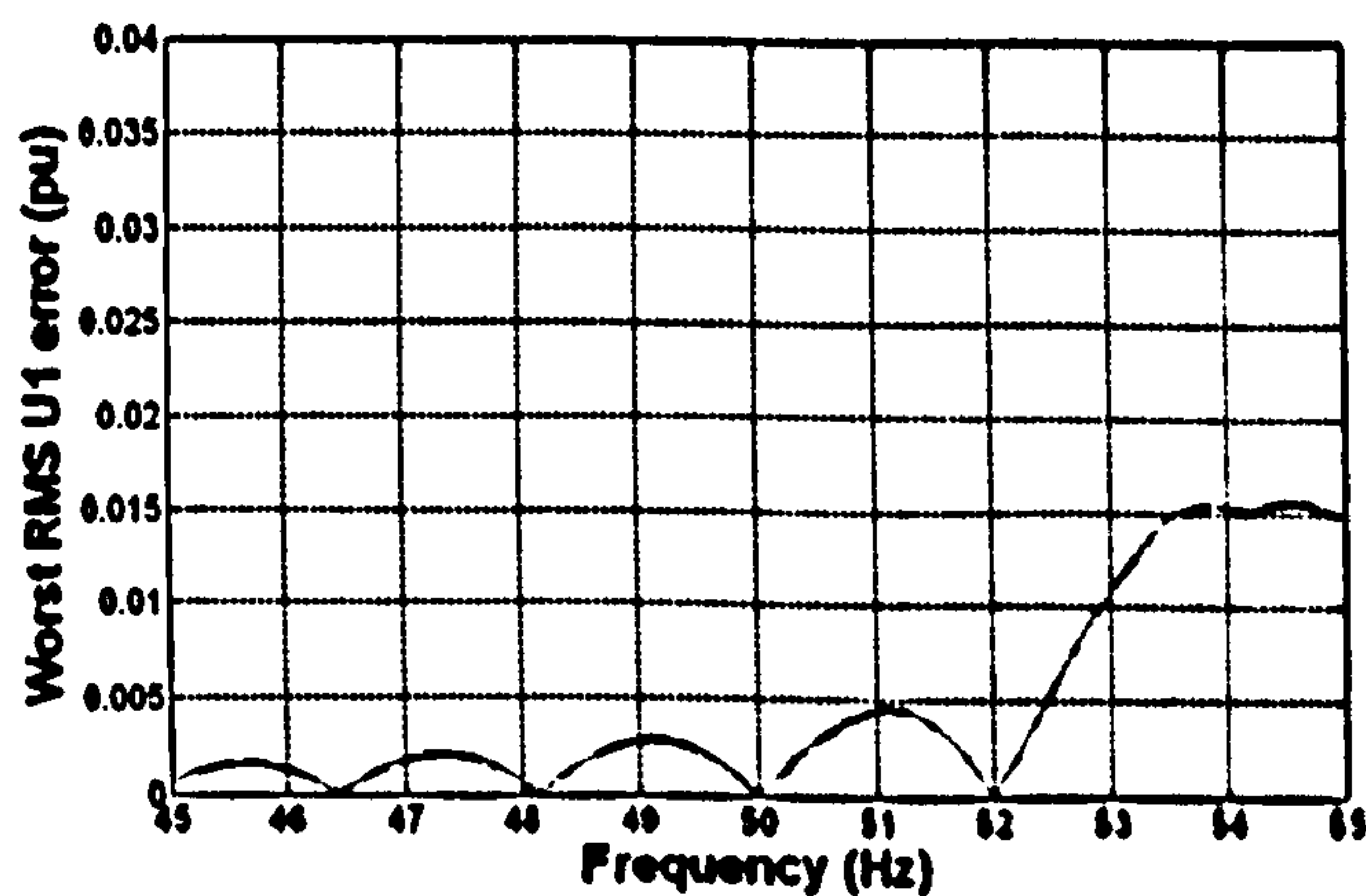


Figure 4-12 : Simulation of errors on the Fourier fundamental measurement at 1300Sa/s due to 23rd harmonic @ 1.5%, for input frequencies in the range 45-55Hz. 1st order (solid) and 2nd order (red dashes) methods

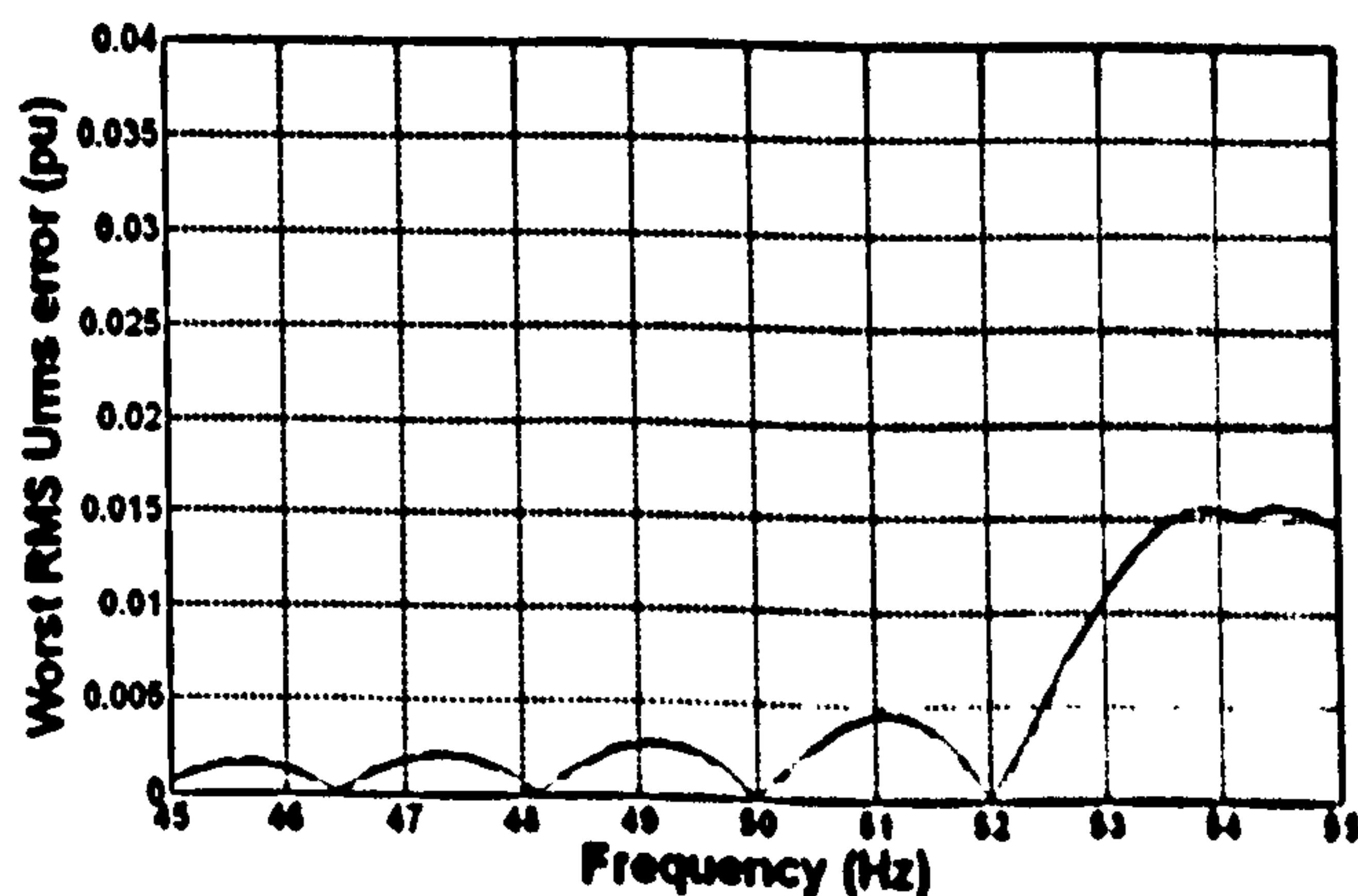


Figure 4-13 : Simulation of errors on the all-harmonic RMS measurement at 1300Sa/s due to 23rd harmonic @ 1.5%, for input frequencies in the range 45-55Hz. 1st order (solid) and 2nd order (red dashes) methods

4.2.5 Prediction of errors at different sample rates

Having established a set of tools to predict the errors due to harmonic contamination, these tools can be used to quickly explore the relationship between these errors and the sampling rate. Before this is done, a final touch is to add models of the low-pass anti-aliasing filter stages described in section 3.4. The tools can then be repeatedly executed using a MATLAB script, to examine the following space of scenarios:-

- All values of samples per cycle from 10 to 30
- All harmonics from 2 to 40
- Individual harmonic amplitudes set to either a multiple of the BS EN 50160 (BSI, 2000) levels (see Figure 2-2, using values of 0.5% for all harmonics above the 24th), or to the worst-case microgrid harmonic voltage amplitudes outlined in section 2.7.2
- All values of input frequency in 0.1Hz steps, from 45 to 55 Hz

The entire resulting dataset can be summarised and cut in a number of different ways to show the effects of the harmonics and the different sample rates.

4.2.5.1 Errors due to aliased and un-aliased harmonics at 2x the BS EN 50160 levels

In the plots shown below, the point plotted for each value of samples-per-cycle shows the maximum error which we would expect to see by applying all the harmonics 2 to 40 at levels twice those of BS EN 50160 (BSI, 2000), simultaneously. This corresponds to a THD of 22.8% and would violate the overall 8% THD specification of BS EN 50160 by a factor of more than 2. At each value of sample-per-cycle, the values of the errors are calculated by the following process:

- Select each of the input frequency values in turn from the range 45-55 Hz
- calculate the RSS (Root sum of squares) of all the errors due to every even harmonic 2-40 at this input frequency, (even harmonics are likely to be uncorrelated)
- then linearly add the errors due to every odd harmonic (odd harmonics are likely to be correlated due to saturation and distortion effects)
- repeat for all input frequencies at this value of samples-per-cycle
- select the worst value of RSS error found

Note that this treatment by RSS of the even harmonics plus linear summing of the correlated odd harmonics matches the rationale used to generate the expected microgrid harmonic levels in section 2.7.2.

First, the predicted errors on the Fourier fundamental calculation are shown in Figure 4-14, and then the predicted errors on the all-harmonic RMS measurement in Figure 4-15.

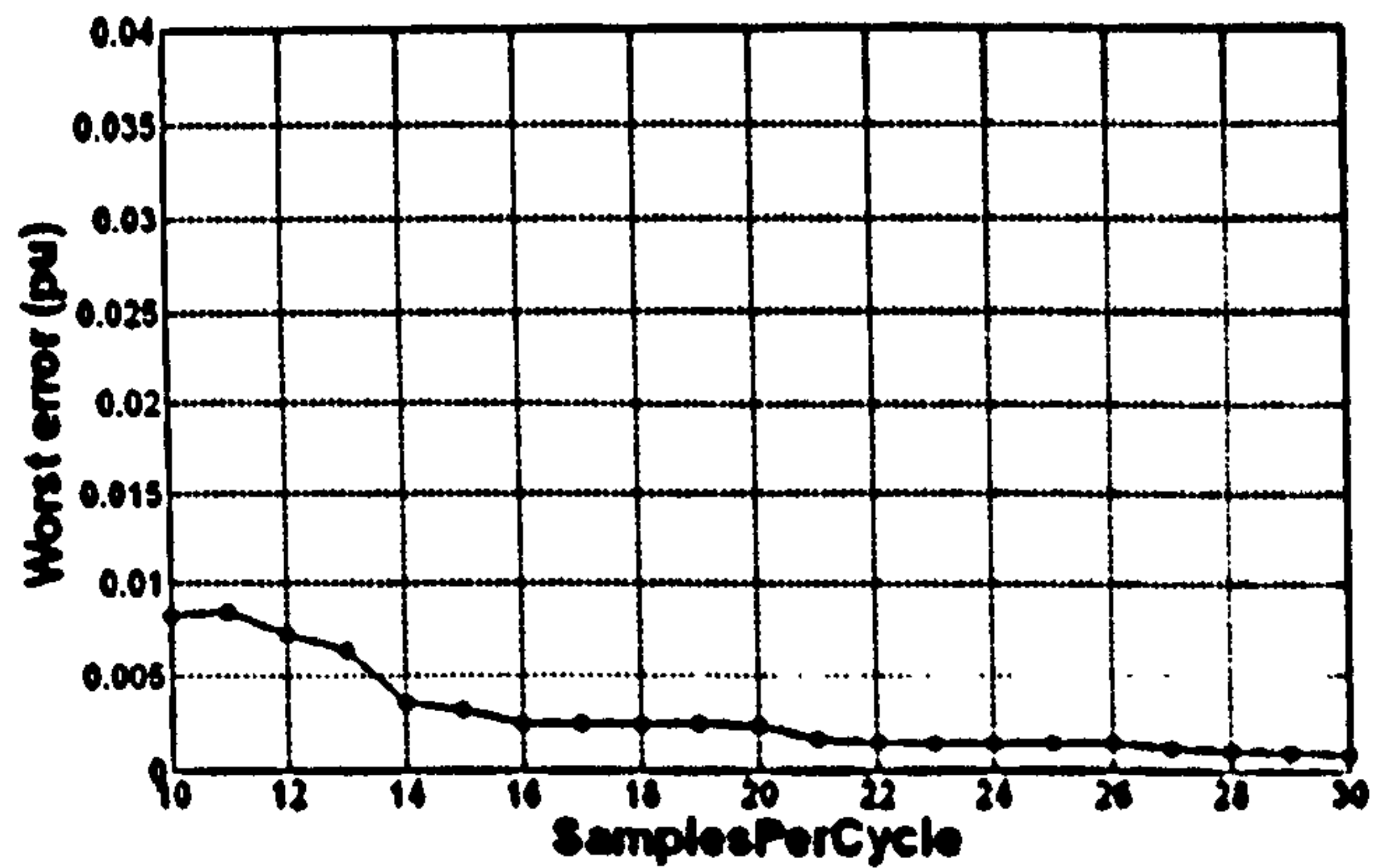


Figure 4-14 : Prediction of worst overall errors on Fourier fundamental measurements, due to 2x BS EN 50160 level harmonics 2-40 applied all at once

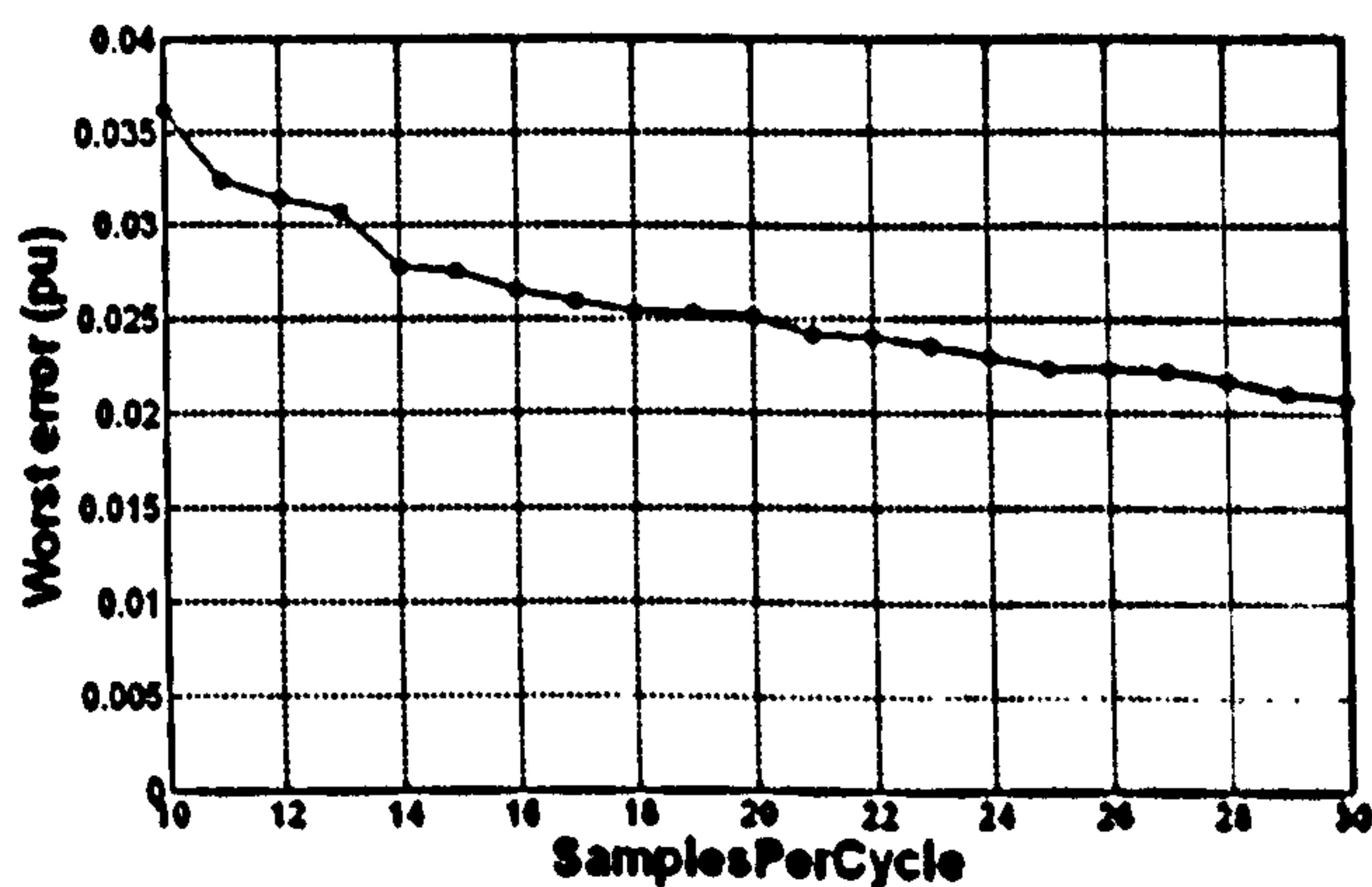


Figure 4-15 : Prediction of worst overall errors on all-harmonic RMS measurements, due to 2x BS EN 50160 level harmonics 2-40 applied all at once

The worst expected errors on the Fourier fundamental measurement are <0.01 pu for all values of sample-per-sample. The all-harmonic RMS errors are considerably larger, up to 0.04 pu at 10 samples per cycle. The larger all-harmonic RMS errors, particularly at the low sample rates, are caused by the attenuation of the harmonic content by the anti-aliasing filters. Even at 30 samples per cycle, the filter cut-off frequency is only 250 Hz ($1/3^{\text{rd}}$ of the Nyquist frequency which is $1/2$ of 50×30). Therefore all harmonics of 5th and above are well attenuated and are not then measurable by the all-harmonic RMS algorithm. The all-harmonic RMS measurement tends therefore to give a lower result than the actual waveform RMS value. This will also cause an incorrectly low THD readout. The required sample rate to record an accurate all-harmonic RMS measurement for everything up to the 40th harmonic would then be approximately defined by being able to set the anti-aliasing filter cutoff frequency to $40 \times 50 \text{ Hz} = 2 \text{ kHz}$. This would imply a Nyquist frequency of about 3x this amount (6kHz) and therefore a sample rate of about 12 kSa/s,

or 240 samples per cycle.

This can be verified by a repeat analysis over a wider range of samples per cycle, which shows that the all-harmonic RMS measurements do become accurate to the 0.0025pu level for 2x BS EN 50160 (BSI, 2000) harmonic inputs at around the 240 sample per cycle rate, with a low-pass filter cut-off frequency of 2kHz (Figure 4-16).

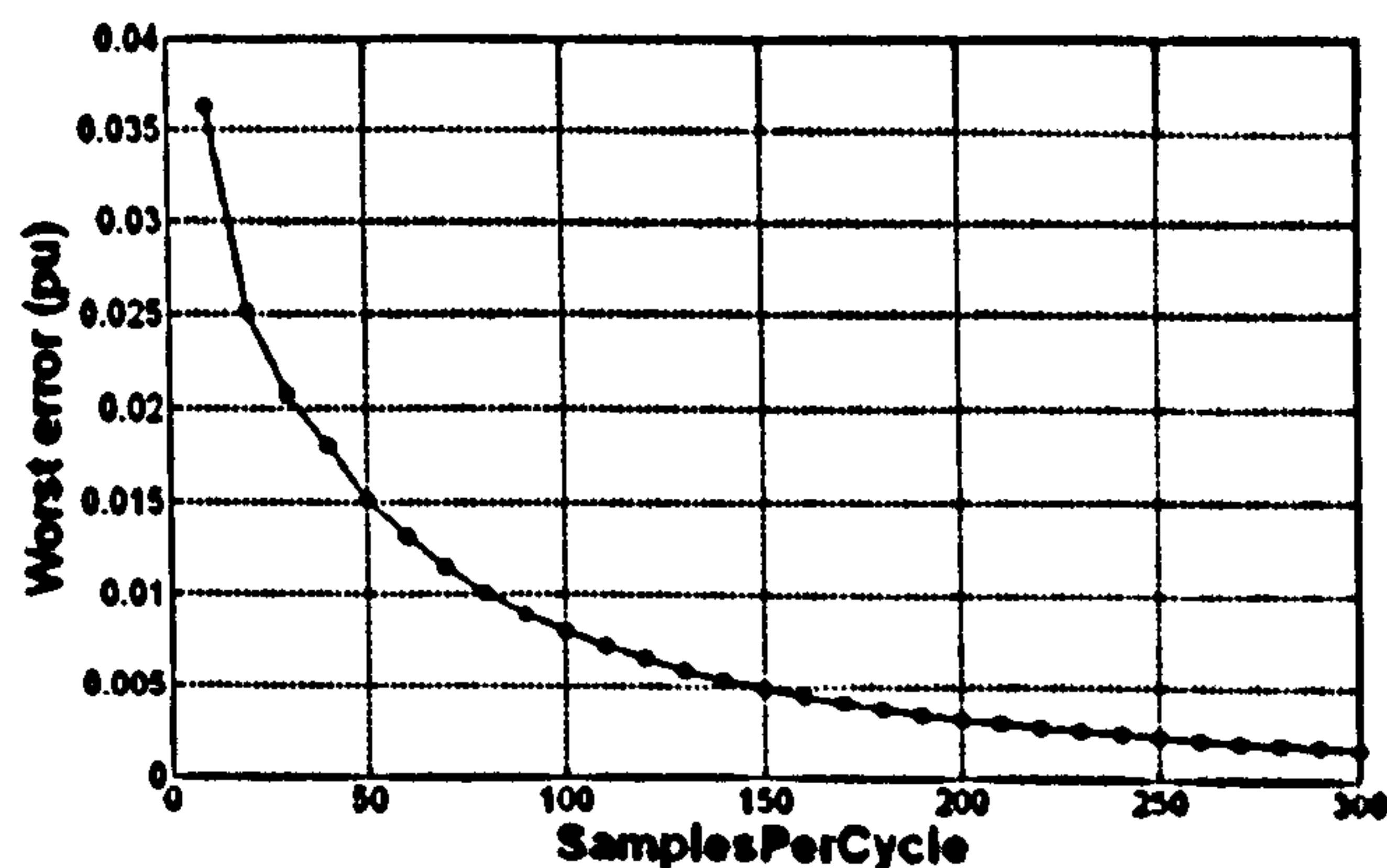


Figure 4-16 : Prediction of worst overall errors on all-harmonic RMS measurements, due to 2x BS EN 50160 level harmonics 2-40 applied all at once. 10-300 Sa/cycle

Even at this sample rate and error level, by equation (3.8), the THD error due to a 0.0025pu error on the RMS measurement would be 7%. To achieve <1% accuracy in the THD measurement of harmonics up to the 40th, the sample rate required is about 2000 samples per cycle (100 kSa/s) to give an RMS error of 0.00005pu (Figure 4-17). An alternative would be to measure each of the harmonic amplitudes separately using Fourier fundamental measurements. This would require 40 Fourier measurements to measure up to the 40th harmonic (or an FFT process to measure all concurrently), with a sample rate of approximately $10 \cdot 40 = 400$ Samples per cycle, 20 kSa/s (A sample rate of 128 Samples per cycle is used in just this way in Kuhlmann (2007)). Even then, the answer would only be accurate upon the assumption that no inter-harmonics existed. Since modern power-electronic devices inject harmonics at frequencies which are locked to quartz clocks and not the system frequency, such an assumption is invalid. The kinds of sample rate and required processor speed mentioned above are outside the aim and scope of this document.

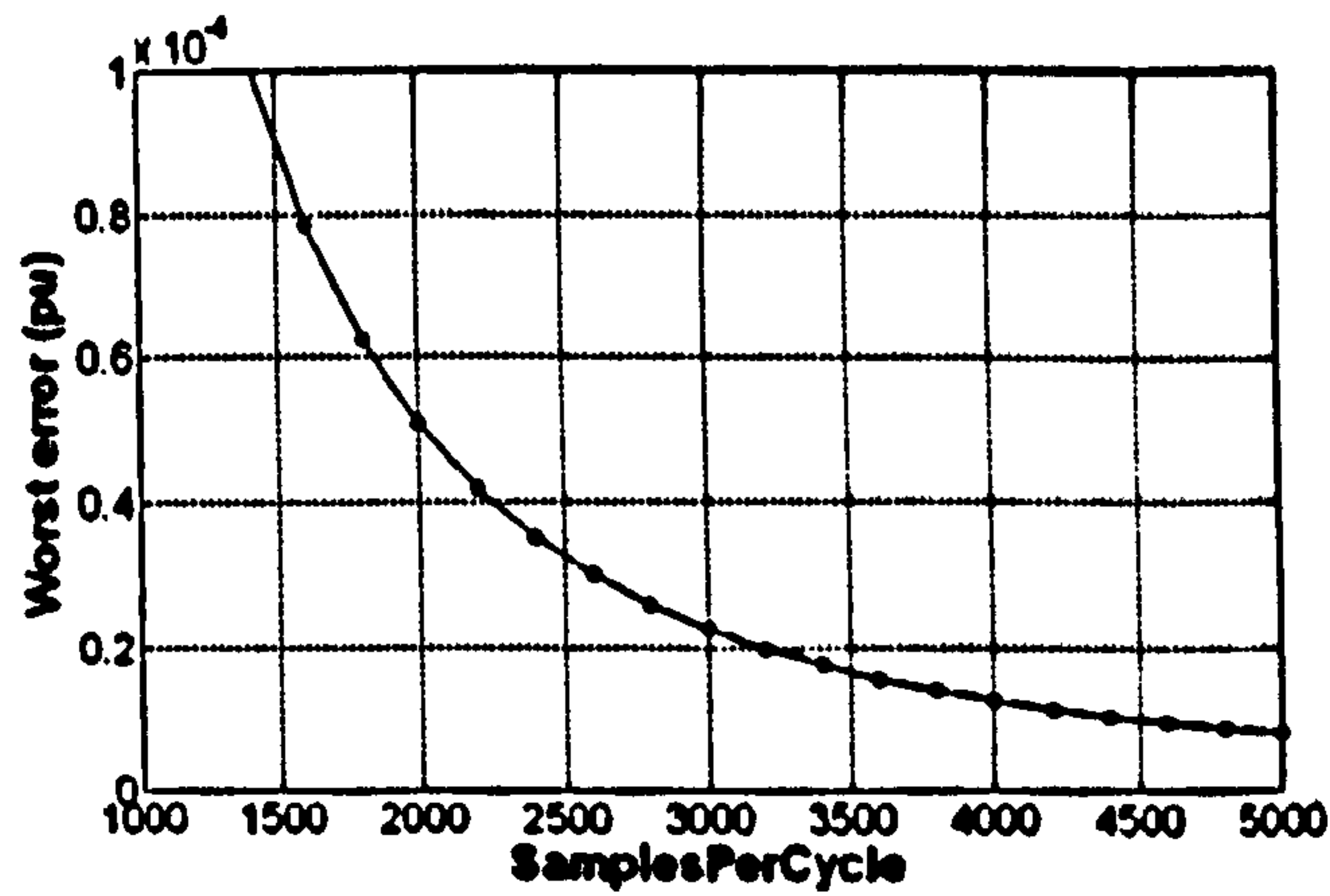


Figure 4-17 : Prediction of worst overall errors on all-harmonic RMS measurements, due to 2x BS EN 50160 level harmonics 2-40 applied all at once. 200-5000 Sa/cycle

Sample rates as low as 10 samples-per-cycle are therefore viable within a microgrid scenario, but only the measurements of Fourier fundamental will be robust and accurate. With high levels of harmonics the all-harmonic RMS measurements might be in error by up to 4% under the scenario described, which is an unacceptably large error. THD errors are even larger.

4.2.5.2 Errors due to aliased and un-aliased harmonics at worst microgrid levels

Finally, the predicted error analysis is repeated but for the worst case microgrid harmonic content scenario described in section 2.7.2. This waveform has a THD_v of 53%. The errors on the Fourier fundamental measurement at 10 samples per cycle are ±0.02pu which is quite large (Figure 4-18). The errors on the all-harmonic RMS measurement are much larger, of the order of 0.15pu, which makes the RMS measurements totally unusable (Figure 4-19).

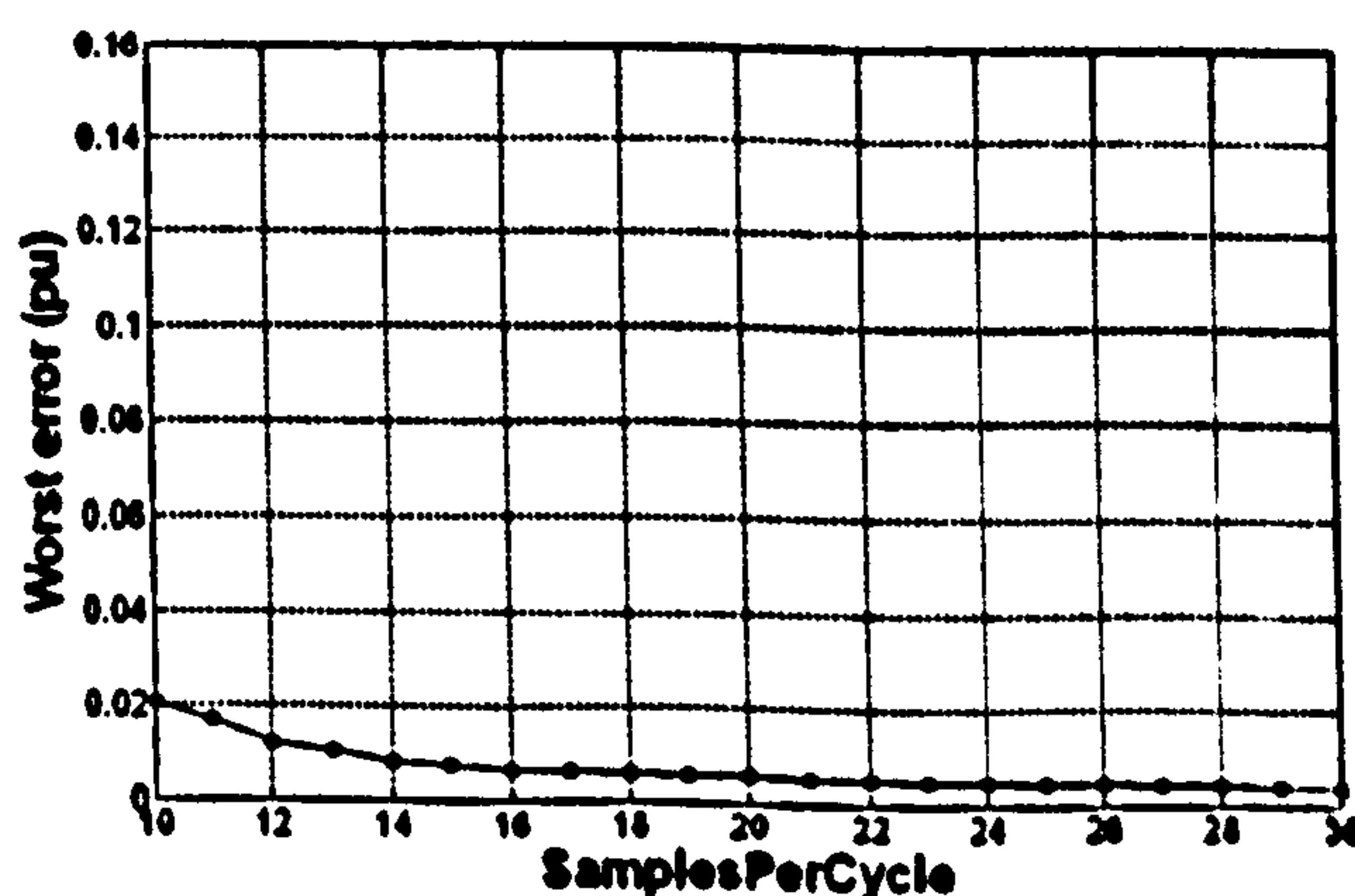


Figure 4-18 : Prediction of worst overall errors on Fourier fundamental measurements, due to worst case microgrid harmonics 2-40 applied all at once

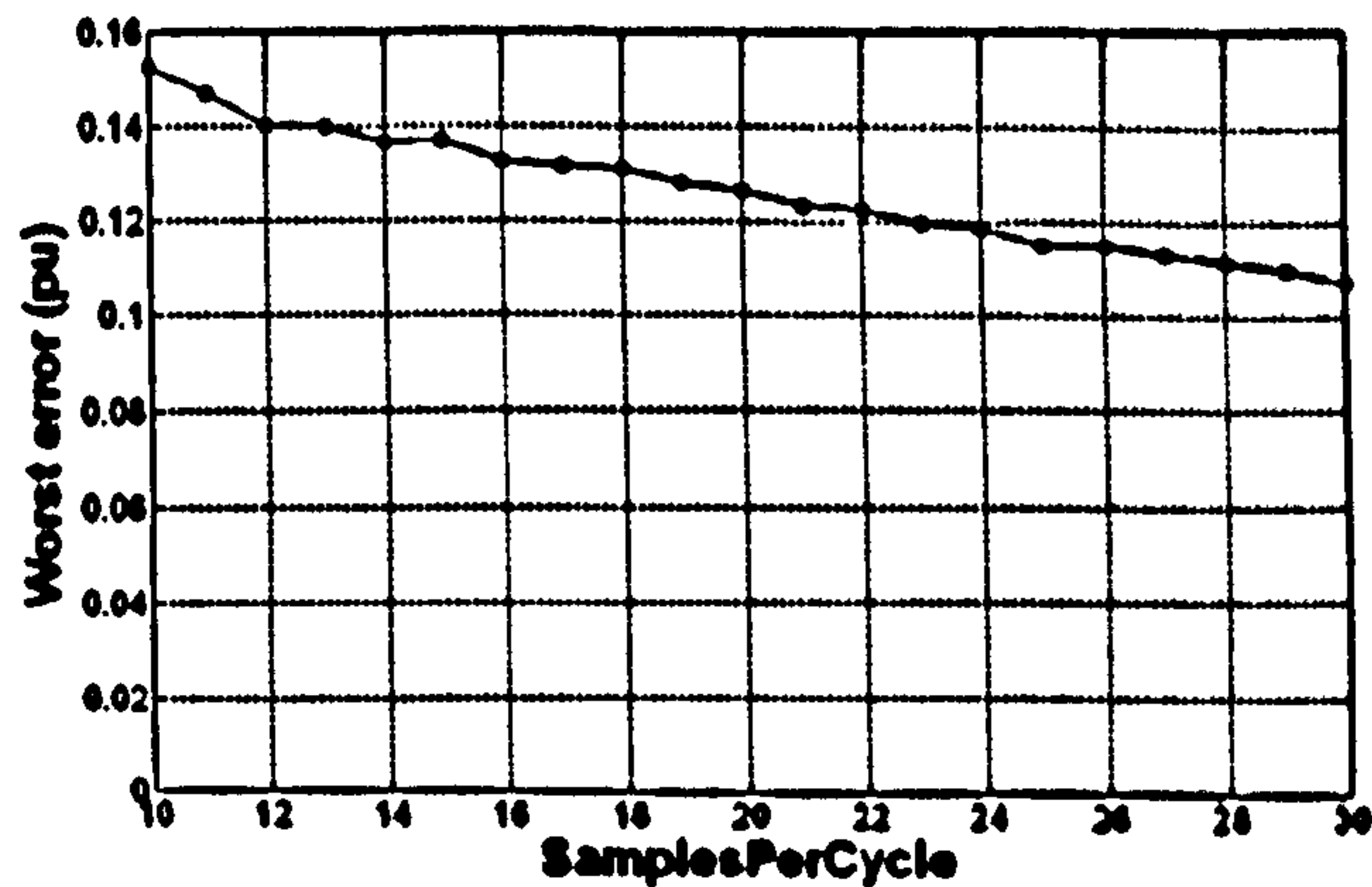


Figure 4-19 : Prediction of worst overall errors on all-harmonic RMS measurements, due to worst case microgrid harmonics 2-40 applied all at once

4.2.6 Validation of the predicted performance at 10Sa/cycle using simulation

The results of section 4.2.5 can be compared to results obtained using the discrete-time simulation model described in section 3.7, this time using waveforms contaminated by harmonics which become aliased (whereas in section 3.7 the waveforms contained no harmonics which were aliased). When this simulation is executed using waveforms containing the worst-case microgrid harmonic levels from section 2.7.2, the results presented below are obtained (Figure 4-20 to Figure 4-23). In these results, the effects of the anti-aliasing filters, noise at 0.005pu RMS, ADC quantisation and DC block have all been included. The measurement is a single 1-cycle Fourier measurement block, without any post-averaging. This is representative for the 1½ cycle algorithms too, since the largest magnitude errors due to aliasing tend to have the lowest ripple frequencies which are not effectively attenuated by the short ½-cycle post-averaging stages in the 1½-cycle algorithms.

The results of Figure 4-20 and Figure 4-22 show good agreement with the predicted errors in Figure 4-18 and Figure 4-19 since the harmonic content at these levels is by far the biggest contributor to error. Due to the levels of harmonics, noise, and ADC quantisation, the 2nd order algorithm does not produce any better results than the 1st order algorithm, but the errors are also no worse. The THD error is as high as 50%

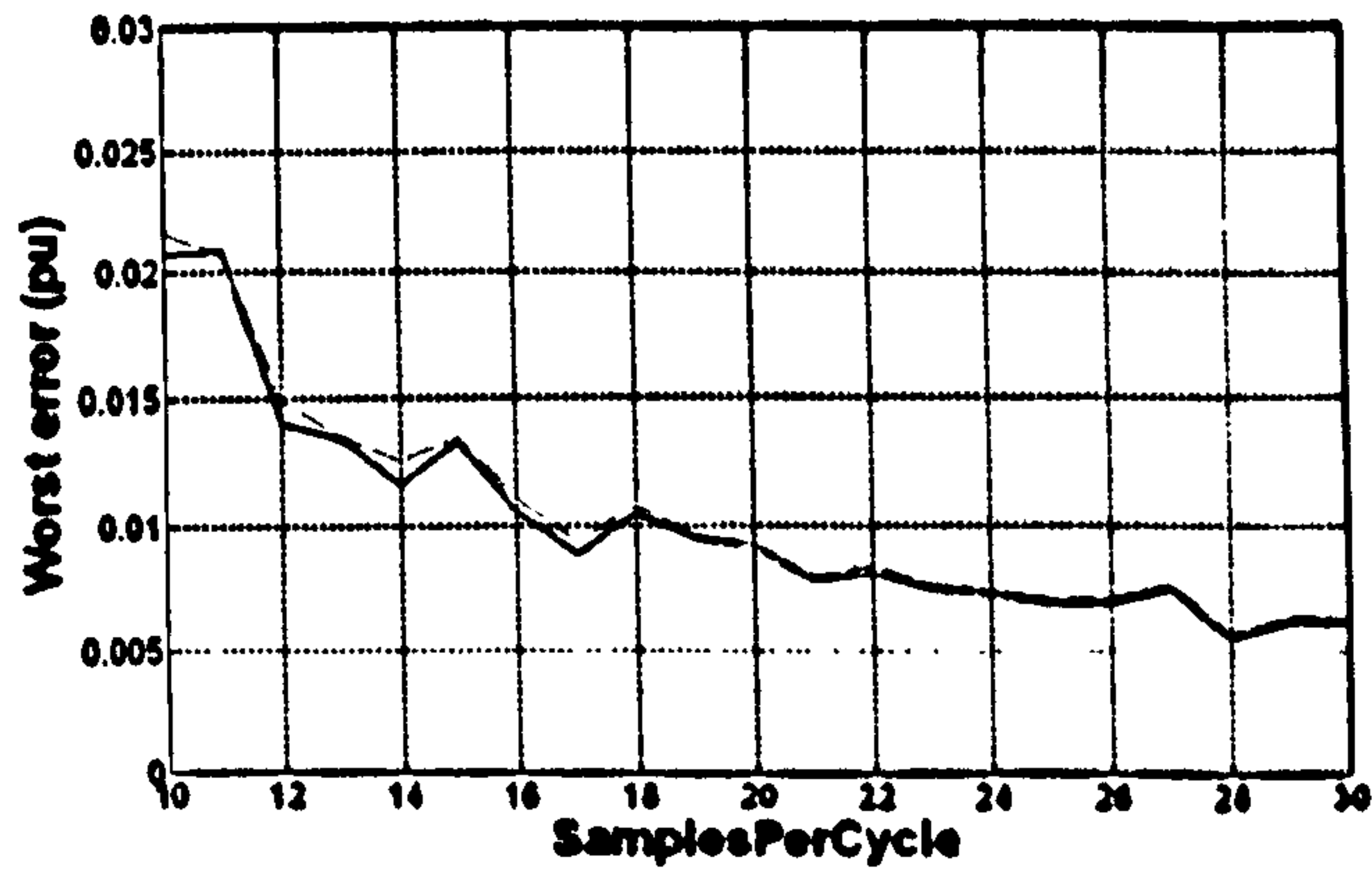


Figure 4-20 : Simulation of worst overall errors on Fourier fundamental measurements, due to worst case microgrid harmonics 2-40 applied all at once, plus noise and ADC quantisation. 1st order (solid) and 2nd order (red dashes) methods

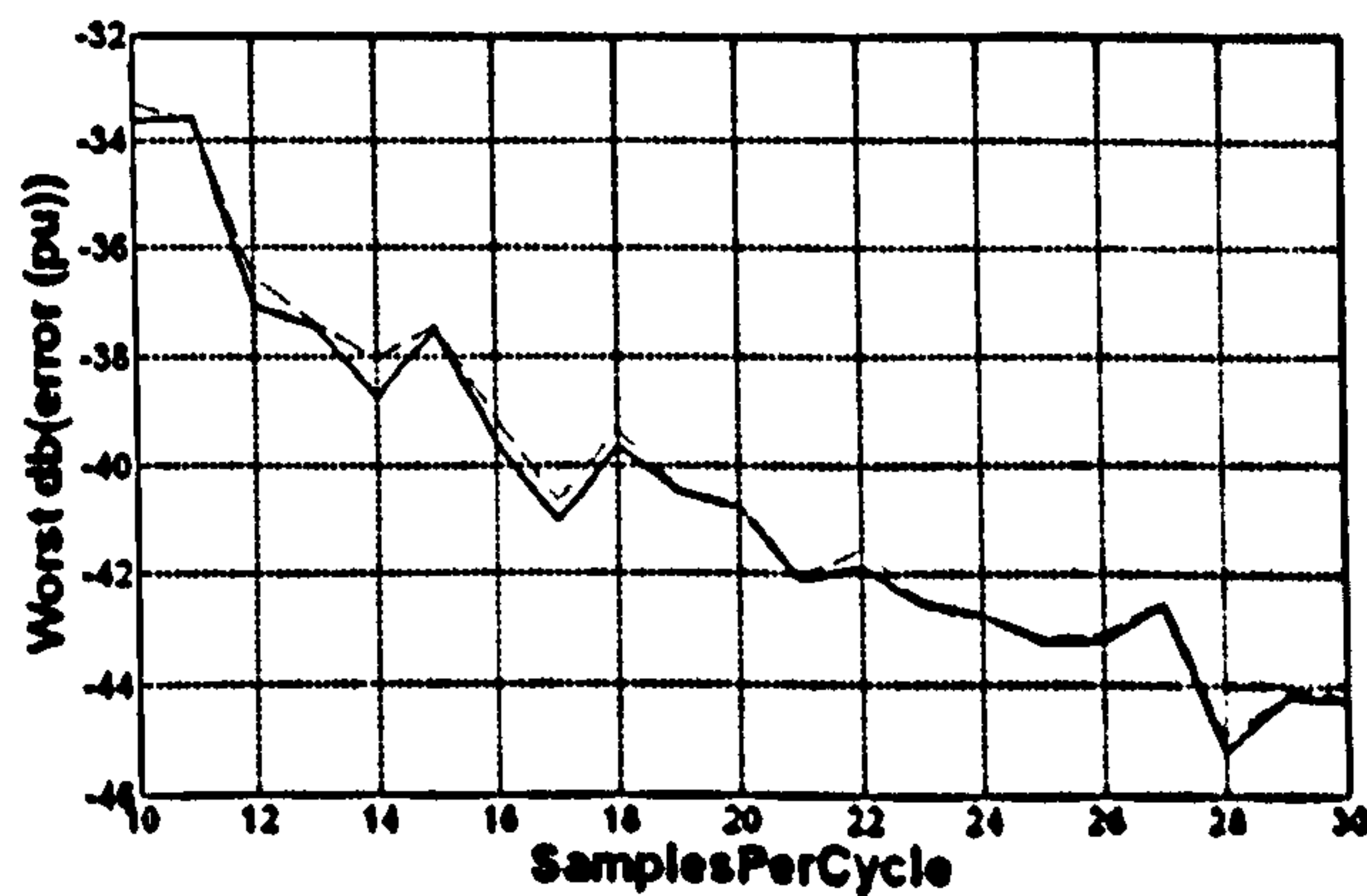


Figure 4-21 : Simulation of worst overall dB(pu errors) on Fourier fundamental measurements, due to worst case microgrid harmonics 2-40 applied all at once, plus noise and ADC quantisation. 1st order (solid) and 2nd order (red dashes) methods

By Figure 4-21, the rate of decrease of errors is approximately 10dB (a linear factor of 3) for a 3-fold increase in sample rate. This means that error is approximately proportional to SampleRate^{-1} .

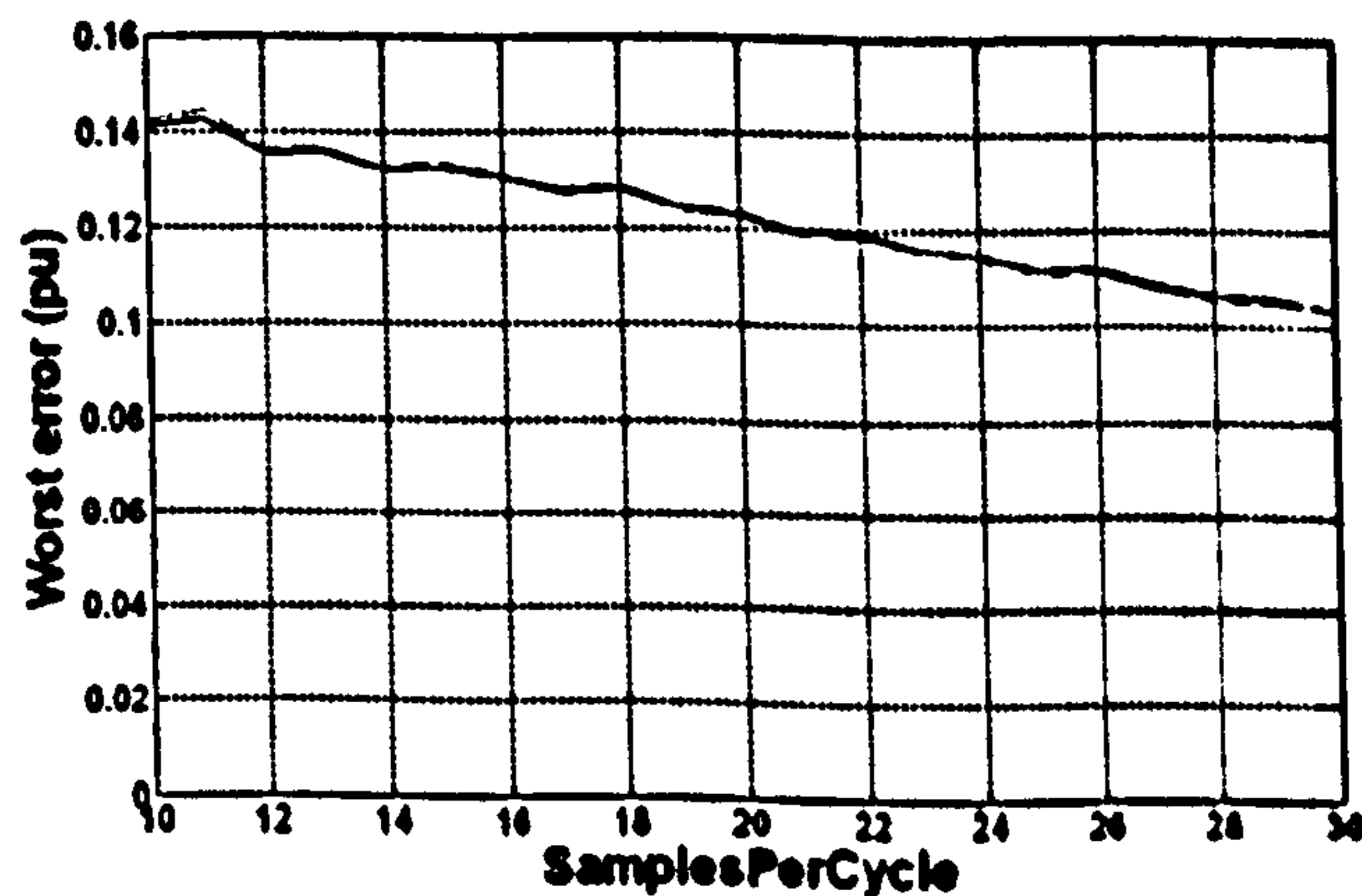


Figure 4-22 : Simulation of worst overall errors on all-harmonic RMS measurements, due to worst case microgrid harmonics 2-40 applied all at once, plus noise and ADC quantisation. 1st order (solid) and 2nd order (red dashes) methods

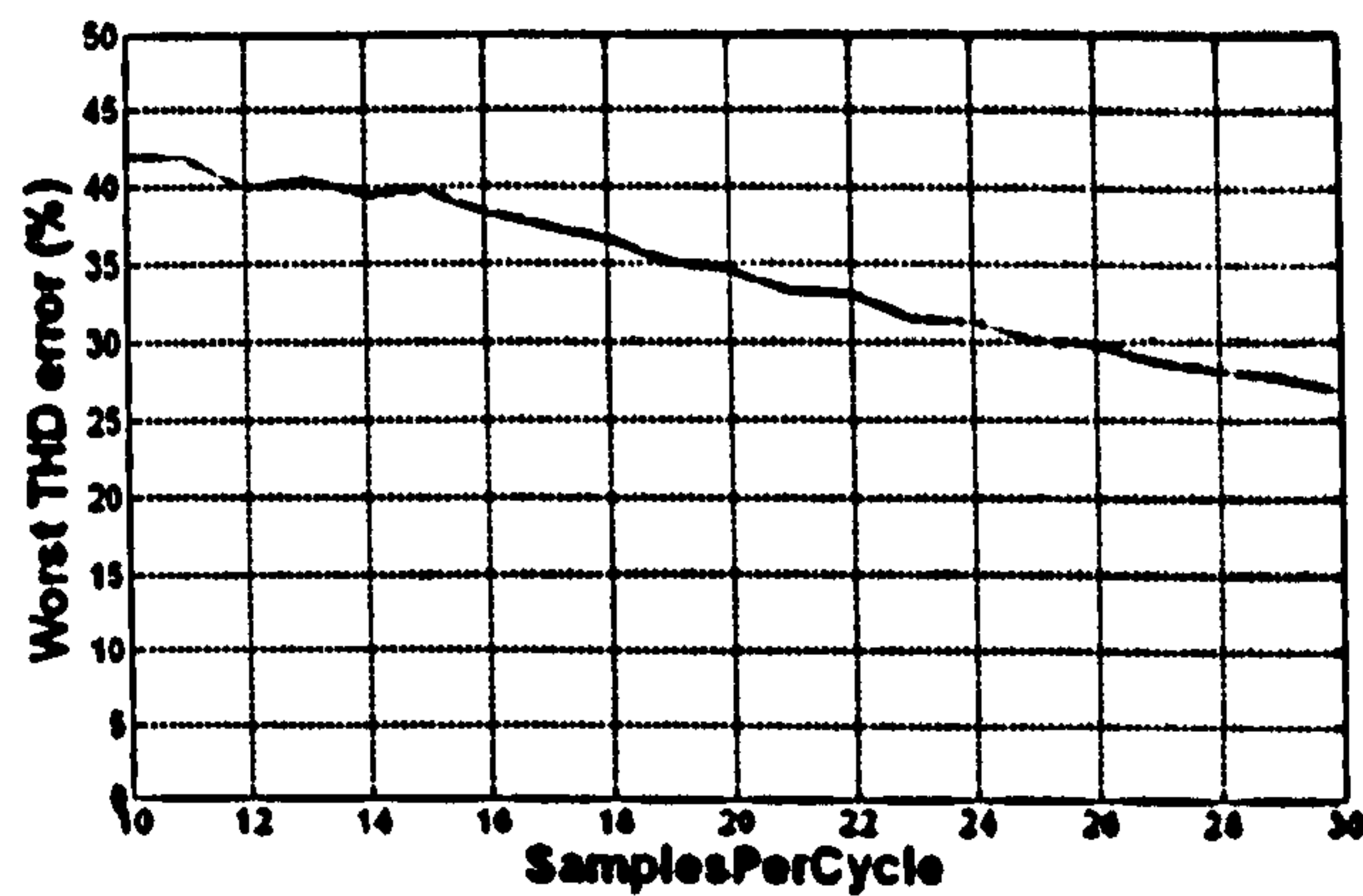


Figure 4-23 : Simulation of worst overall errors on THD measurements, due to worst case microgrid harmonics 2-40 applied all at once, plus noise and ADC quantisation. 1st order (solid) and 2nd order (red dashes) methods

4.2.7 Findings from this section

- The effect of harmonic contributions and aliasing effects can be effectively predicted using the tools generated in this section.
- Sample rates as low as 10 samples per cycle will give errors less than about 0.01pu on the Fourier fundamental measurements, for input waveforms containing harmonics at twice the allowed levels for individual harmonics specified by BS EN 50160, to a total of 22.8% THD. For the worst-case microgrid scenario (53% THD), the worst error is -0.02pu.
- The errors induced onto the all-harmonic RMS measurements are much larger due to the attenuation of the harmonics by the anti-aliasing filters. Only by raising sample rates to 240 samples per cycle will the all-harmonic RMS measurement become accurate to the 0.0025pu level, for 2x BS EN 50160 harmonic levels. Sample rate needs to be raised to ~100 kSa/s in order to record an accurate THD measurement to within 1%.
- A sample rate of 16 samples per cycle produces a good trade-off between sample rate and performance, although of course performance increases as sample rate is increased further. This is because at 15 samples per cycle, the 13th harmonic can contribute, and at 2x BS EN 50160 levels this might have amplitudes of 6%. At 16 samples per cycle, for input frequencies in the range 45-55Hz, the 13th harmonic can no longer alias directly onto the input frequency. Other higher-order harmonics can, but they are much lower magnitude as expected under BS EN 50160.
- The errors due to harmonics cannot be reduced by using the 2nd order algorithms, cancellation techniques, or fixed ½ or 1-cycle post-averaging. The worst errors can, however, be reduced significantly by the use of a novel anti-ripple filter

which is introduced later in section 4.3.

- Since this thesis is targeting low sample-rate algorithms in microgrid scenarios with potentially high levels of harmonics, any critical algorithms should key off the Fourier fundamental measurements, since these remain accurate. The all-harmonic RMS and THD measurements should be used only for indication purposes.

4.2.8 Effect of increasing the number of base measurement cycles

Increasing the number of base Fourier/RMS measurement cycles does not decrease the magnitude of the largest errors due to aliased harmonic contamination - It simply narrows the frequency windows over which those largest errors occur. Referring back to Figure 4-4 & Figure 4-5, repeating the analysis (which excludes the effect of anti-aliasing filters, ADC and DC block) but with the measurements taken over exactly 5 cycles results in the following two plots:

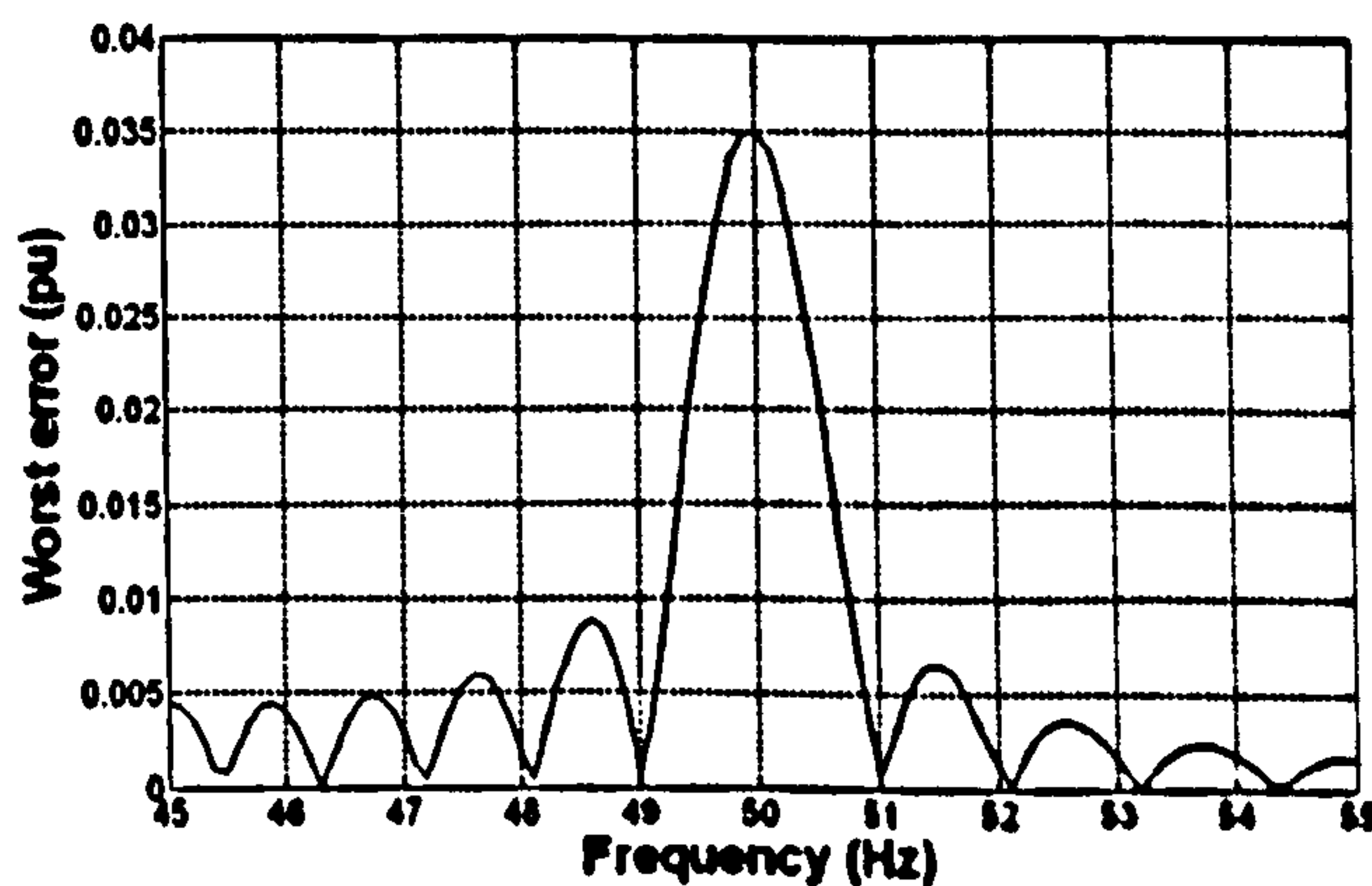


Figure 4-24 : Prediction of errors on the Fourier fundamental measurement at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz, using 5 cycles

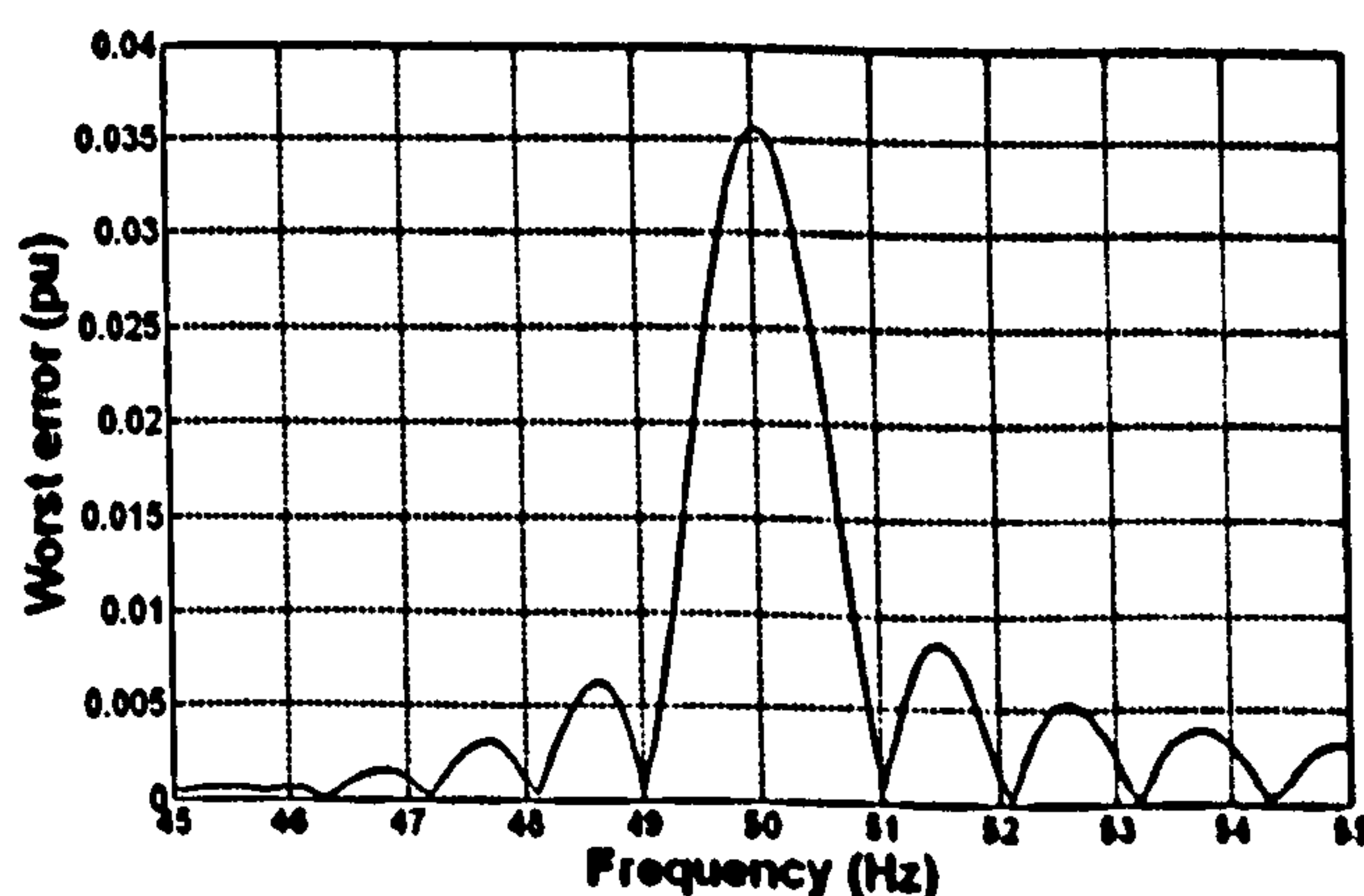


Figure 4-25 : Prediction of errors on the all-harmonic RMS measurement at 500Sa/s due to 11th harmonic @ 3.5%, for input frequencies in the range 45-55Hz, using 5 cycles

It can be seen that the peak error is still 0.035pu, but the error occurs in a tighter

frequency band due to the longer sampling window. Because the frequency windows at which the peak errors appear are smaller, there is less chance of different harmonics causing coincident peak errors through aliasing. However, the overall performance is dominated by the error from the worst aliased harmonic, so this effect does not help to reduce the potential peak error. This has been verified by re-running the simulations of section 4.2.6 but with 5 cycles of Fourier and RMS integration. The overall worst errors are not reduced significantly.

4.2.8.1 Findings for this section

- Increasing the number of measurement cycles does not help reduce the magnitude of the errors; it simply tightens the windows of input frequency over which the worst errors occur.

4.3 Addition of a novel ripple-removal filter to minimise aliased harmonic effects

Thus far in chapters 3 & 4, there are several key findings which have been made. These findings suggest that some of the targets of chapter 2 are likely to be met with ease, but that other targets are difficult to meet. In terms of voltage measurement accuracy, the worst case ripple errors at the outputs of a 1 or 1½-cycle measurement at a sample rate of 500 Sa/s (10 samples per cycle) are approximately ± 0.02 pu due to aliased harmonics, anti-aliasing filters, noise, ADC quantisation and processing (see Figure 4-20). This is sufficient to meet the target for relaying operations given in Table 2-11, but much too large to meet the desired ± 0.001 pu specification of Table 2-12 for control applications. Table 2-12 does, however, allow up to 5 cycles for a measurement used for control purposes, in order to allow further attenuation of such errors. This additional time available for the measurement can be used advantageously.

Referring back to Figure 4-4 and Figure 4-6, it has been found that the largest errors due to aliased harmonics tend to occur as sub-harmonic ripple on the measurements. These errors are also larger than any errors due to integration/interpolation, noise, ADC quantisation, and un-aliased harmonics. The worst case (largest ripple magnitude) is when the ripple frequency falls very close to (but not exactly at) 0 Hz. In this case, only very long (more than 5 periods) stages of post-processing can remove the error. A special case is where the ripple frequency falls at 0 Hz exactly. In this case, there is no ripple on the measurement output, but a fixed absolute error is incurred. Intermediate frequency ripples, however, can be removed entirely by a further stage of exact-time averaging over a time of $1/f_R$ seconds, where the ripple occurs at f_R Hz.

The problem in the case of aliased harmonics is that the ripple can occur at any "random" frequency, dependent upon the input signal harmonic content. The maximum time length of the FIR filter is also limited by the maximum latency which we require of the measurement. For control purposes, according to Table 2-12, the measurement time latency requirement is 5 cycles (100ms). This allows for the 1½ cycle measurement blocks proposed thus far, plus an additional 3½ cycles of post-processing. This means that, for a 50 Hz system, a final post-averaging filter of maximum time length $3.5/50=70\text{ms}$ could be applied. This filter could, in theory, be used to entirely reject ripple down to 14.3 Hz. Allowing longer latencies would obviously allow even lower frequency ripples to be rejected, with further benefit. Remember, however, that it will never be possible to remove the DC errors at 0 Hz ripple.

4.3.1 Design of a novel, adaptive, ripple-rejection filter

Such a novel filter to reject ripple at unknown frequencies, using the FIR exact-time averaging blocks from section 3.2, has been developed during the course of this thesis. Its design is shown below. This filter provides additional noise rejection as well as ripple rejection.

Adaptive ripple removal filter, using a FIR exact-time averaging stage
 Andrew Roscoe, 2007

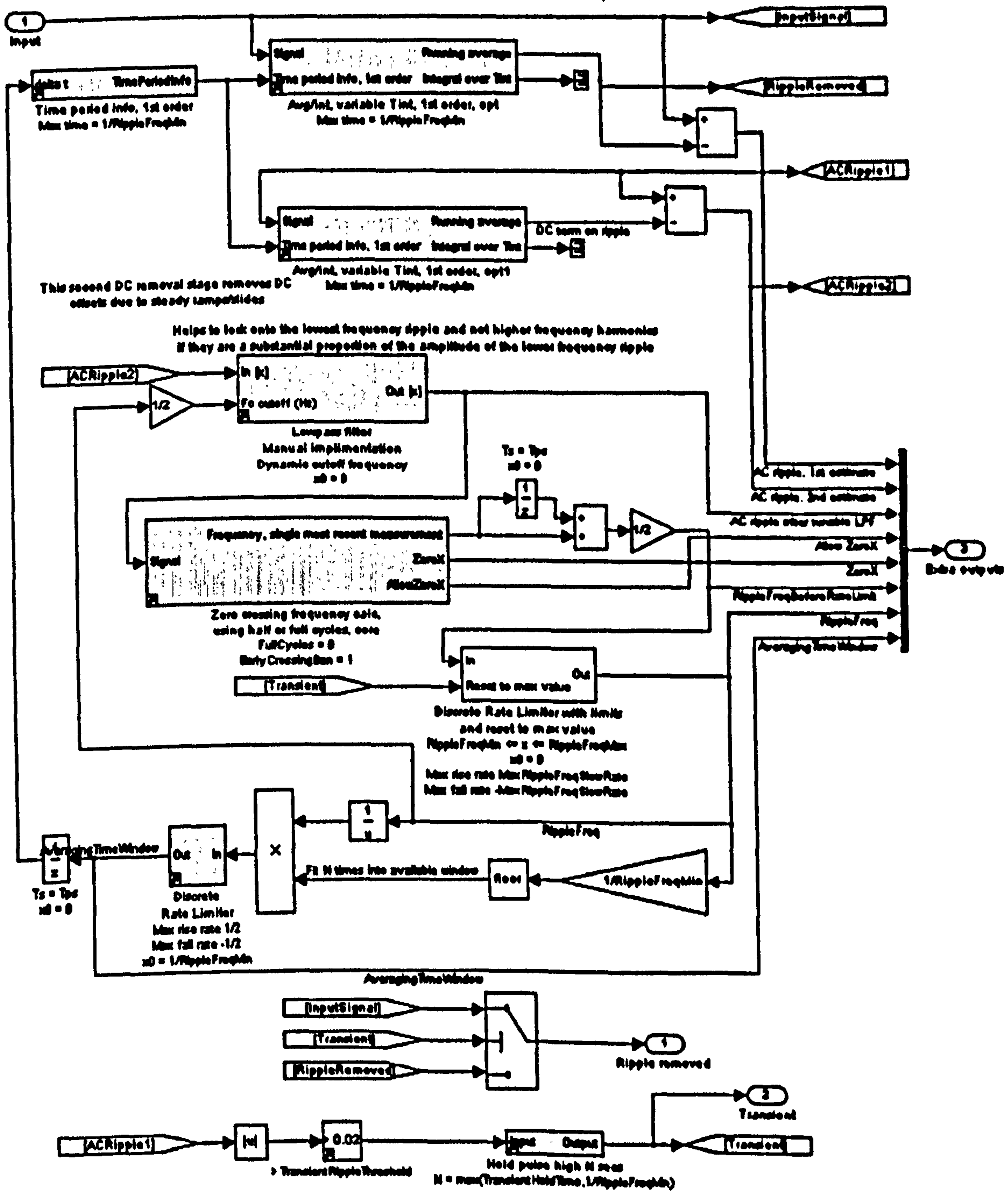


Figure 4-26 : Design of a novel, adaptive FIR ripple-removal filter

The design of the algorithm shown in Figure 4-26, at the core, uses a single exact-time averaging block to filter the signal. The maximum time length of this filter (and thus its maximum contribution to measurement latency) is set by the reciprocal of the parameter *RippleFreqMin*, which is set at compile-time. The trick inside this filter is the determination of the actual time length to average over. The processes can be summarised as follows:

1. Perform the exact-time averaging, using the determined time length (fed back from step 8).
2. The input signal minus the averaged signal reveals the 1st estimate of the AC ripple. This 1st estimate of AC ripple remains at a non-zero level during steady ramps of the input signal, which is undesirable. Therefore, this signal is averaged again over the same timeframe, and a second subtraction is performed to give a 2nd estimate of AC ripple. This 2nd estimate is zero for a steady linear ramp on the input signal.
3. Low-pass filter the AC ripple signal through a single, 1st-order low-pass filter with a dynamically adjustable cut-off frequency. This cut-off frequency is set to $\frac{1}{2}$ the current estimate of ripple frequency (fed back from step 8). This reduces noise and attenuates ripple at higher frequencies. The idea is to try and pick the lowest ripple frequency from the signal, without carrying out a full FFT in real-time (which would require a large amount of CPU time).
4. Measure the frequency of the low-pass filtered AC ripple signal, using zero crossings. The detail of the zero crossings algorithm to do this is shown in Fig. E-8.
5. Slew-rate limit the measured ripple frequency, and limit the frequency within the bounds $RippleFreqMin \leq F \leq RippleFreqMax$
6. The smallest time average window required to reject the ripple frequency f would be $1/f$. However, instead, when the ripple frequency f is large, this might result in a small averaging window, which is not ideal for noise rejection. Therefore, a further step calculates the number of integer windows of length $1/f$ that can be fitted inside the allowed time window $1/RippleFreqMin$. The desired averaging time window is thus $1/f \cdot \text{floor}(f/RippleFreqMin)$.
7. The result from step 6 above is that the averaging time window may jump suddenly when the floor() function crosses an integer threshold. This can cause high-bandwidth steps at the output (sudden jumps), which may be undesirable. Thus, a second slew rate filter is inserted. The maximum rate for this is calculated as a maximum time window change of $0.5/RippleFreqMin$ (the biggest step we would expect to make) divided by the time required to settle. This is $1/RippleFreqMin$, the maximum time length of the averaging stage. Thus the slew rate turns out to be simply $\frac{1}{2}$.
8. Feed back the result to the rest of the algorithm, with the required 1-sample state delay

The exceptions to this process occur when a transient is detected in the input waveform. This is determined by a threshold set on the magnitude of the AC signal content. When this

occurs, the following process over-ride occurs:-

- The first slew-rate filter is reset to the parameter *RippleFreqMax*. This tends to set the averaging time window up towards the maximum allowed length (as many integer ripple periods can be fit into the maximum time window).
- The input is fed directly to the output, bypassing the averaging stage entirely. This happens for at least $1/RippleFreqMin$ seconds, the maximum time taken for the averaging filter to settle to the new input value. The filter thus has zero latency during the transient events. This is highly desirable!
- Optionally, the reset/bypass state can be held for an additional pre-determined time period. This extends the amount of time following transient detection, for which the slew rate filter is forced to hold the value *RippleFreqMax*, and the input is fed directly to the output.

To test this block, a simple Simulink simulation is used. This simulation applies the following “genuine” signal:

- A signal of amplitude 1, with a dip from 1.0 to 0.8 between 7 & 7.03 seconds, and a rise from 0.8 to 1 again between 7.1 & 7.13 seconds. This simulates the way a voltage dip would be measured by a 1½-cycle Fourier measurement block.

To this “genuine” signal, two errors are added, both of 0.01pu peak magnitude. One is at a fixed ripple frequency of 75Hz. The other is at a variable frequency which starts at 100Hz, ramps down to 0Hz at $t=5s$, and then back up to 100Hz at $t=10s$, the end of the simulation.

The ripple removal filter is set with the following parameters:

- *RippleFreqMin* = $50/3.5$ (14.3 Hz), a maximum time length of 3.5 cycles at 50Hz, or 70ms
- *RippleFreqMax* = 100
- *MaxRippleSlewRate* = 500
- *TransientRippleThreshold* = 0.05
- *TransientHoldTime* = 0 (clipped up to $1/RippleMinFreq$ = 70ms inside the algorithm)

The ripple remover succeeds in removing most of the ripple due to both the interfering ripple signals, as can be seen in Figure 4-27 to Figure 4-29. The main points to note are:-

- At $t=7s$ and $t=7.1s$, the filter detects the transient. For 70ms after each of these

points the signal passes straight through the filter with zero latency. In this simulation, the transient events merge together as the fall and rise are close together.

- At other times, the ripple is mostly removed.
- An exception is the first 70ms of the simulation, when essentially a transient is detected due to the sudden application of the waveform.
- Another exception is at about $t=5s$ (see Figure 4-28 & Figure 4-29). During this time, the frequency of one of the rippling error input waveforms is close to 0Hz, DC. This means that the averaging filter cannot remove it within the allowed timeframe.
- The algorithm is correctly able to lock on to the lower frequency of the two rippling error waveforms, even though they are at the same amplitude. The filter tracks the variable rate ripple error when it drops below 75Hz, and it tracks the 75Hz ripple error when the variable rate ripple error frequency rises above 75Hz.

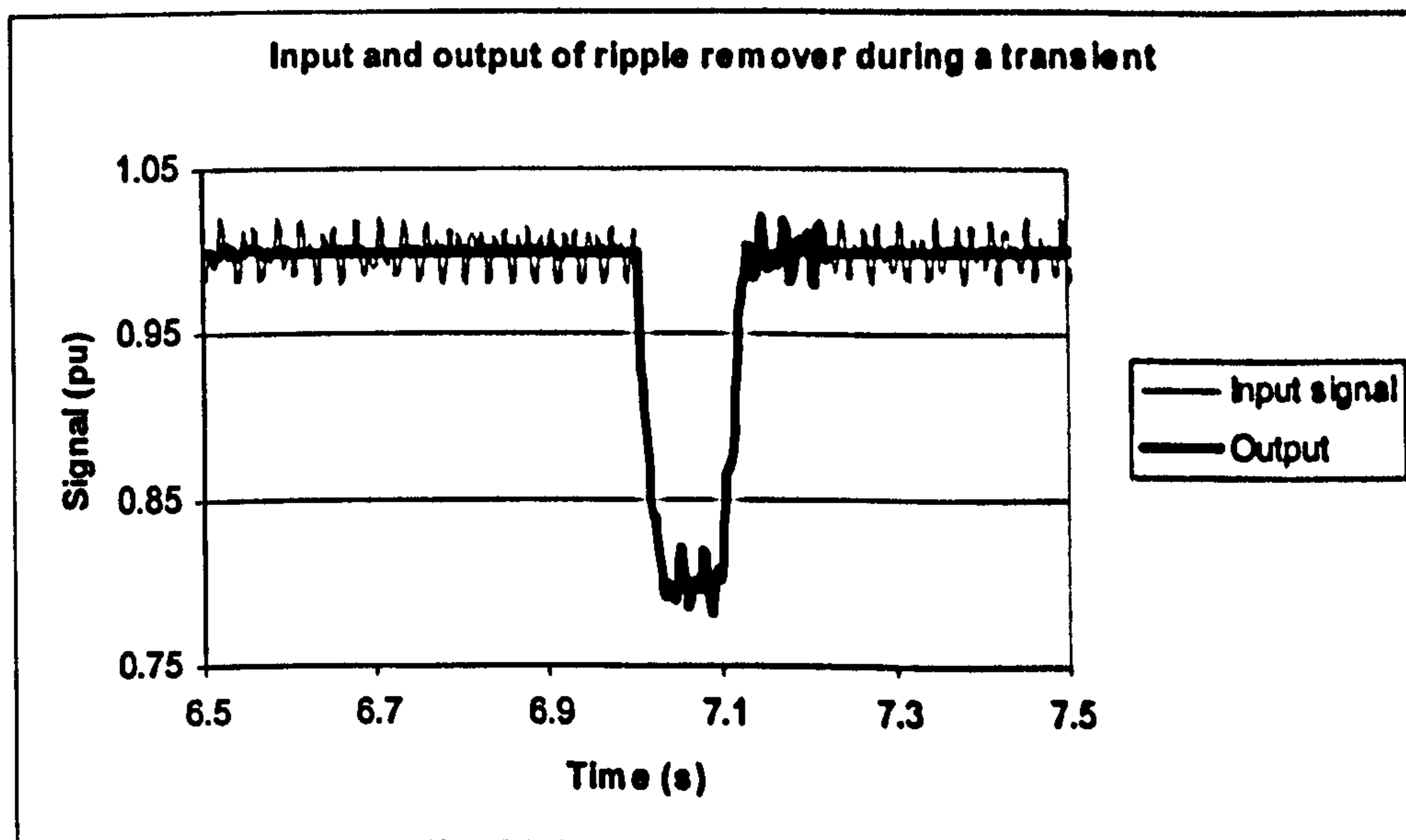


Figure 4-27 : Input and output of a ripple removal filter during a transient

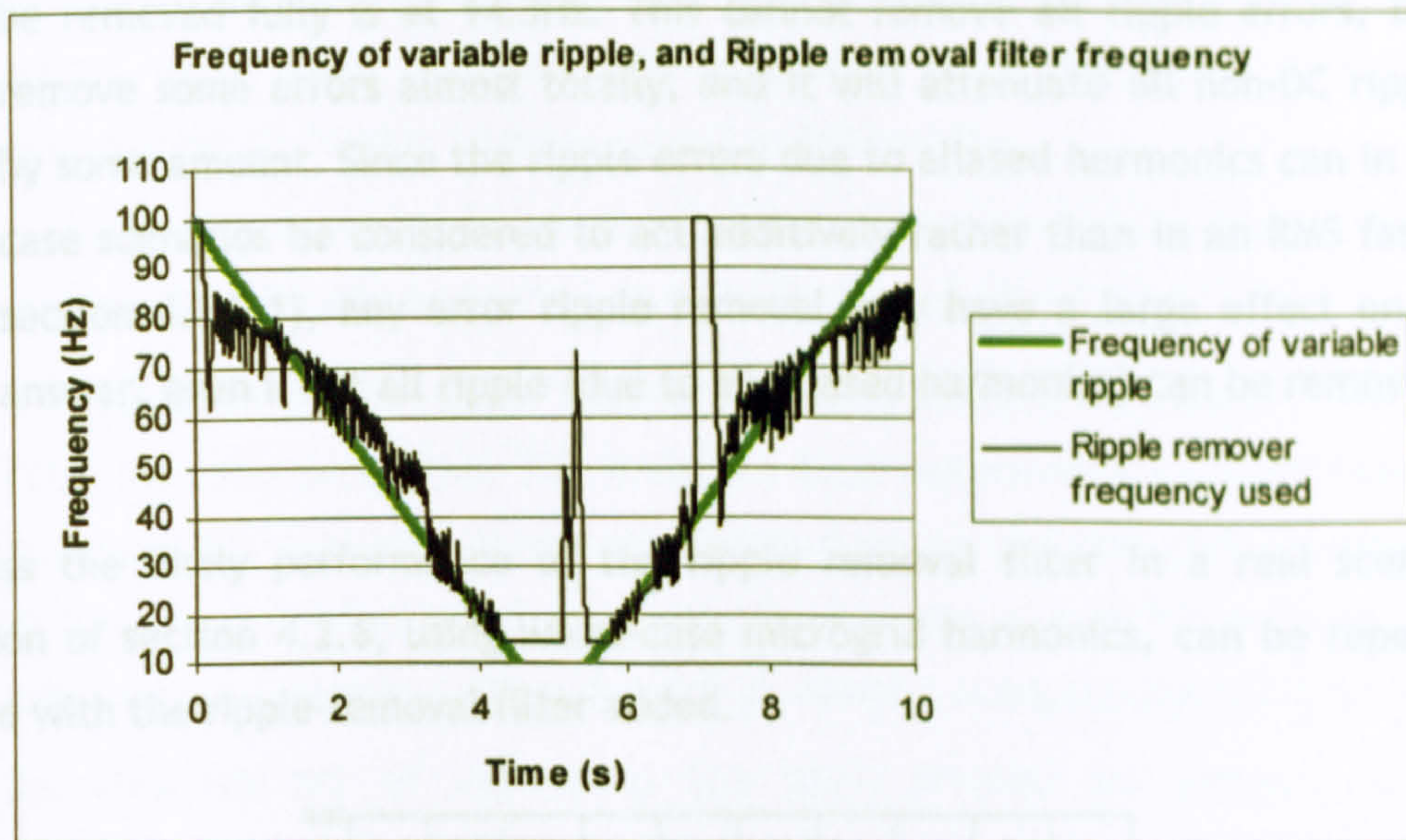


Figure 4-28 : Frequency of variable ripple vs. actual Ripple removal frequency

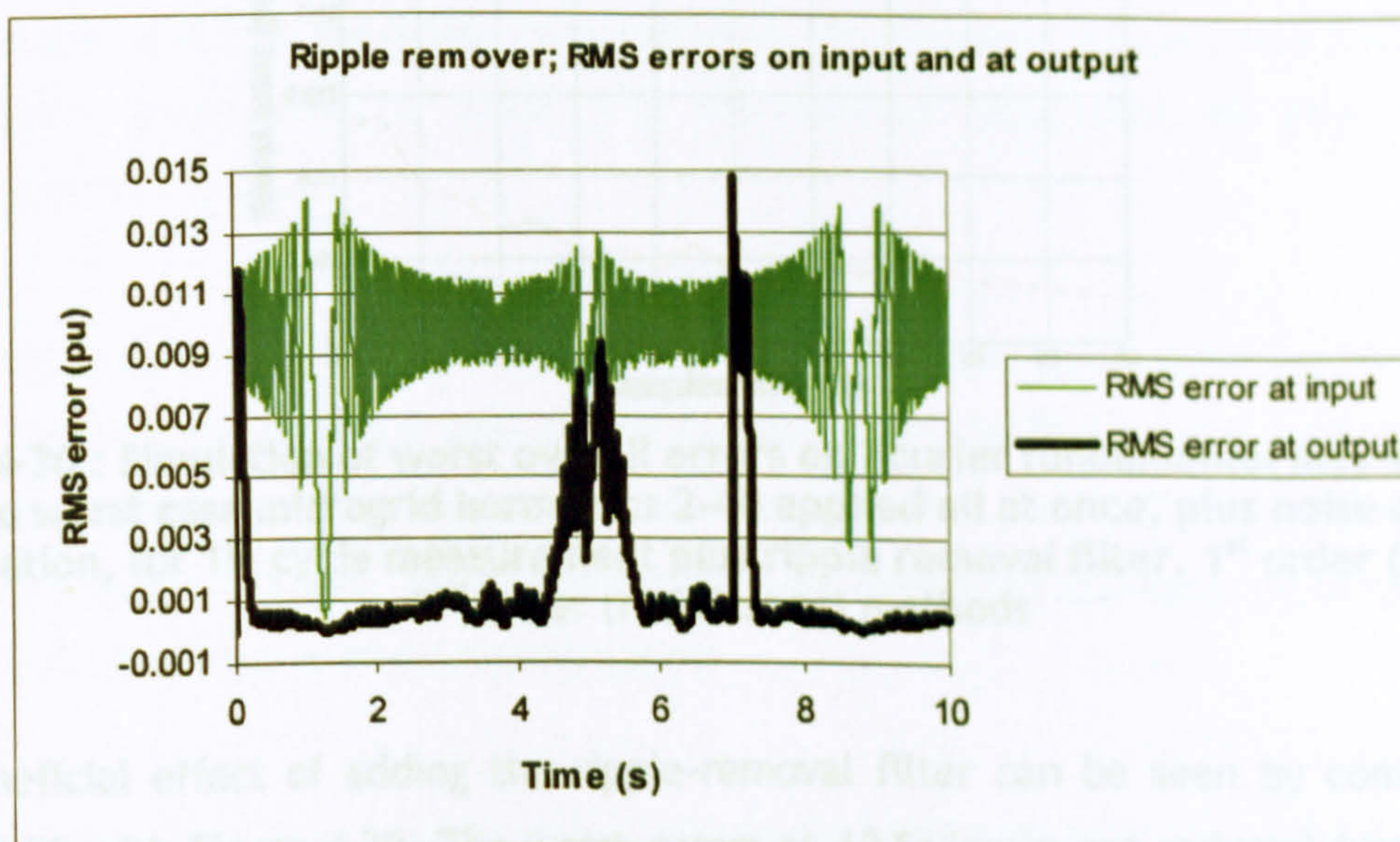


Figure 4-29 : Demonstration of ripple attenuation using the ripple removal filter

4.3.2 Assessment of errors on the fundamental amplitude and phase measurement using a 5-cycle latency measurement and worst-case microgrid harmonics at 500Sa/s

To create a lowest-ripple 5-cycle latency measurement of fundamental voltage or current amplitude, which can be used for delicate control purposes within environments of high harmonic content and noise, at low sample rates, the proposed method is therefore:-

- use a $1\frac{1}{2}$ cycle measurement algorithm made up of a base Fourier stage over 1 cycle (without 2nd harmonic cancellation), followed by an additional $\frac{1}{2}$ -cycle averaging ...
- followed by an adaptive ripple-removal filter, of maximum latency $3\frac{1}{2}$ cycles. This means that the lowest error ripple frequency due to aliased harmonics which can

be removed fully is at 14.3Hz. This cannot remove all ripple errors, but it can remove some errors almost totally, and it will attenuate all non-DC ripple errors by some amount. Since the ripple errors due to aliased harmonics can in the worst case scenarios be considered to act additively rather than in an RMS fashion (see section 4.2.5.1), any error ripple removal may have a large effect on the final answer, even if not all ripple (due to all aliased harmonics) can be removed.

To assess the likely performance of the ripple removal filter in a real scenario, the simulation of section 4.2.6, using worst-case microgrid harmonics, can be repeated, but this time with the ripple-removal filter added.

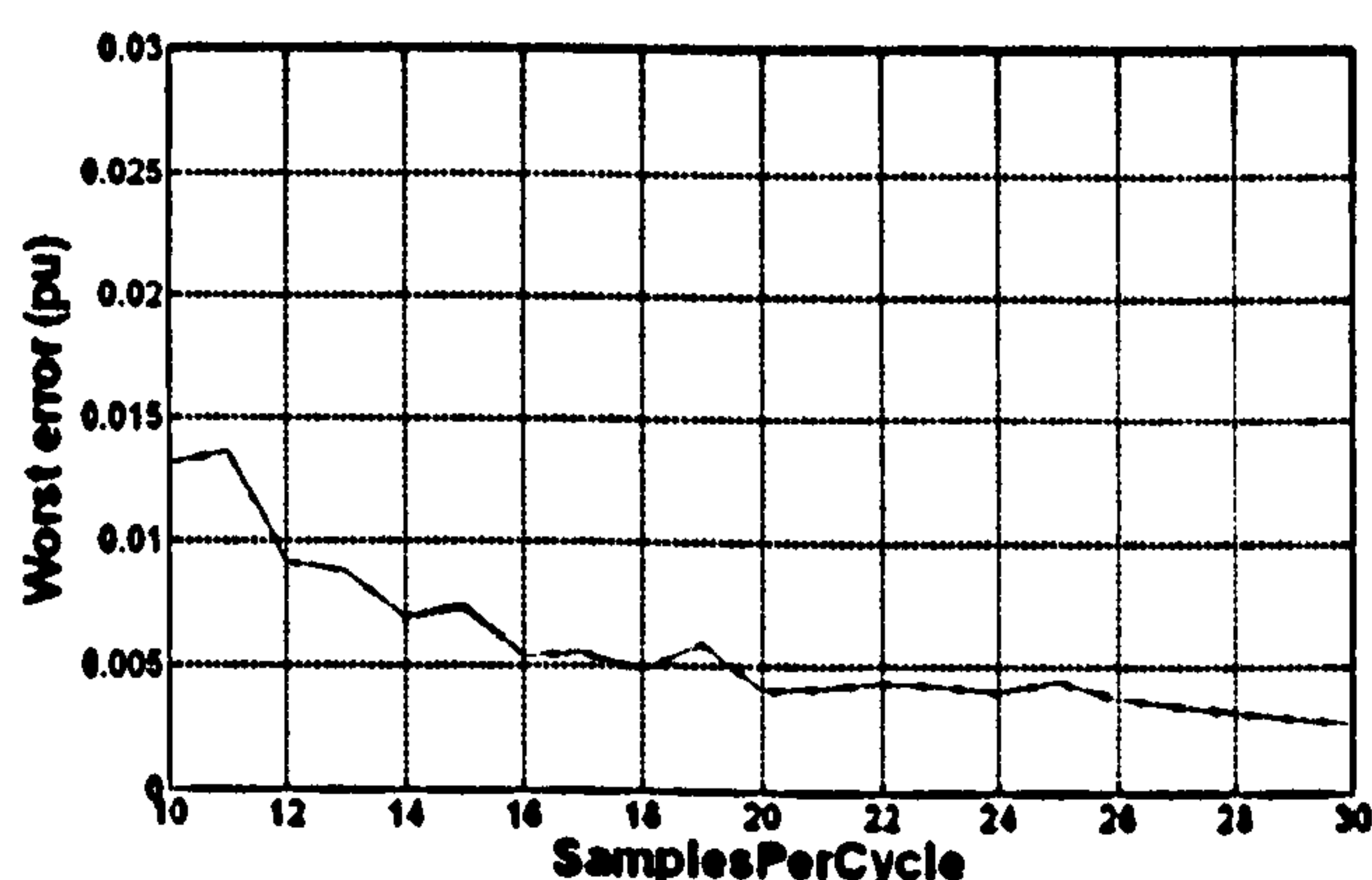


Figure 4-30 : Simulation of worst overall errors on Fourier fundamental measurements, due to worst case microgrid harmonics 2-40 applied all at once, plus noise and ADC quantisation, for 1½ cycle measurement plus ripple removal filter. 1st order (solid) and 2nd order (red dashes) methods

The beneficial effect of adding the ripple-removal filter can be seen by comparison of Figure 4-30 with Figure 4-20. The worst errors at 10 Sa/cycle are reduced from 0.021 to 0.013pu.

4.4 Summary of key findings without ADC oversampling

Methods for Fourier and all-harmonic amplitude have been presented in, which incorporate a number of novel features based on robust FIR filters:-

- Adaptions of an existing SimPowerSystems block which provide more robust and accurate methods of evaluating exact-time average values.
- The application of these filters in Fourier measurement stages with extra novel cascaded averaging steps to create measurements with a latency of 1½ cycles. This almost entirely eliminates integration/interpolation ripple and the effects of errors on the frequency measurement, even at sample rates as low as 10 samples per cycle.
- The option of tapping off lower-latency measurements with ½-cycle and 1-cycle

timeframe is included in the blocks. This includes the option of a 1-cycle latency output with lower integration/interpolation error by using a 2nd-harmonic cancellation technique adapted from a published PLL.

- A selection process has been designed to choose the appropriate combination of measurement blocks to use in a given scenario (section 3.13.1).
- The option of extending the post-processing with a novel, adaptive ripple-removal filter has been presented. This creates a total measurement system consisting of 3 cascaded FIR averaging stages of lengths 1-cycle, ½-cycle and approximately 3½ cycles, each implemented in a specific way for a specific purpose. The total measurement latency (within the digital domain) is approximately 5 cycles.
- An effective set of algorithms has been created to measure fundamental amplitude and phase. Their performance tabulated below is limited due to the extremely strict constraints being applied in this thesis: low sample rates, high noise, and high harmonic contamination. In scenarios which allow higher sample rates, lower noise, or lower THD, the identical algorithms will give much more accurate results.

Sample rates down to 10 samples per cycle (500 Sa/s) have been shown to be usable, so long as any controls or relays key off the fundamental amplitude measurement, and not the all-harmonic RMS measurement. The all-harmonic RMS and THD measurements should be used for indication only, unless the sample rate used is much higher (and the low-pass filter cutoff frequency is raised significantly).

The worst case errors in a microgrid scenario are dominated by the effects of aliased harmonics. The magnitude of the worst case errors including all effects such as ADC quantisation, un-aliased harmonics, aliased harmonics, integration/interpolation error, and frequency measurement error, for a 10 sample-per-cycle system at nominally 50Hz in the presence of 53% THD_v harmonics are approximately:

	Fundamental amplitude error (peak pu)	Fundamental amplitude ripple magnitude (±pu)	Fundamental phase error (peak degrees)
0.5-cycle latency measurement "0.5(NC)"	0.042	0.042	3.2
1-cycle latency measurement "1(NC)"	0.021	0.019	1.4
1-cycle (with 2 nd harmonic cancellation) "1(C)"	0.021	0.020	1.5
1.5-cycle latency measurement "1(NC)+0.5"	0.018	0.017	1.2
5-cycle latency measurement "1(NC)+0.5+RippleRemoval"	0.013	0.013	0.8

Table 4-2 : Worst case Fourier fundamental measurement errors for voltage waveforms with up to 53% THD_v, at 500Sa/s

In Table 4-2, the conditions are:-

- Harmonics applied as per Table 2-5, $THD_V=53\%$
- Anti-alias filter using a 2nd order low-pass filter (2 cascaded RC filters), $f_c=125\text{Hz}$
- Instrumentation noise (Gaussian), post-filtering, 0.005pu RMS (46dB SNR)
- ADC scaling over -2 to +2 pu, with 12 bits, with 2 bits RMS ADC noise (over and above normal quantisation noise)
- ADC sampling and processing at 500 Sa/s (nominally 10 Sa/cycle @ 50Hz)

As described above and in section 2.7.2, this is a very extreme test, and any microgrid operating with such voltage harmonic content for any length of time would suffer from severe problems such as transformer heating/loss etc.

It is also important to stress that these are the worst absolute (instantaneous) errors found for any input frequency in the range 45 to 55 Hz. Thus, normally, even for the worst input frequency, the RMS error is less than this figure by at least a factor of $\sqrt{2}$ and usually by a greater factor. When the data is examined across the range of input frequencies, it is also possible to see that the largest errors only occur at certain input frequencies. These frequencies are the ones at which harmonics alias onto perfectly onto the fundamental, to produce an almost DC error term which cannot be removed by the ripple-removal filters. This shows up on Figure 4-31 and Figure 4-32 below. Figure 4-31 shows the amplitude errors from the "1(NC)+0.5" and "1(NC)+0.5+Ripple removal" measurement systems. The worst input frequency in this case is around 50Hz, where, for example, the 11th harmonic can alias directly onto the fundamental, as $f_{Nyquist}$ is 250 Hz. At other input frequencies, the ripple removal filter can successfully attenuate the errors by much larger amounts.

An additional point of note is that during the above experiment, the threshold for transient detection within the ripple filter can be set as low as about 0.02pu without causing any spurious transient detections. This means that the ripple-removal filter can be applied to the 1½-cycle measurement, and any transient of $> \pm 0.02\text{pu}$ magnitude will be tracked with only the 1½-cycle latency, as the ripple removal filter will pass the data straight through during the transient. During steady-state operation, the ripple-removal filter will automatically switch on and provide an output with much lower ripple, suitable for control purposes.

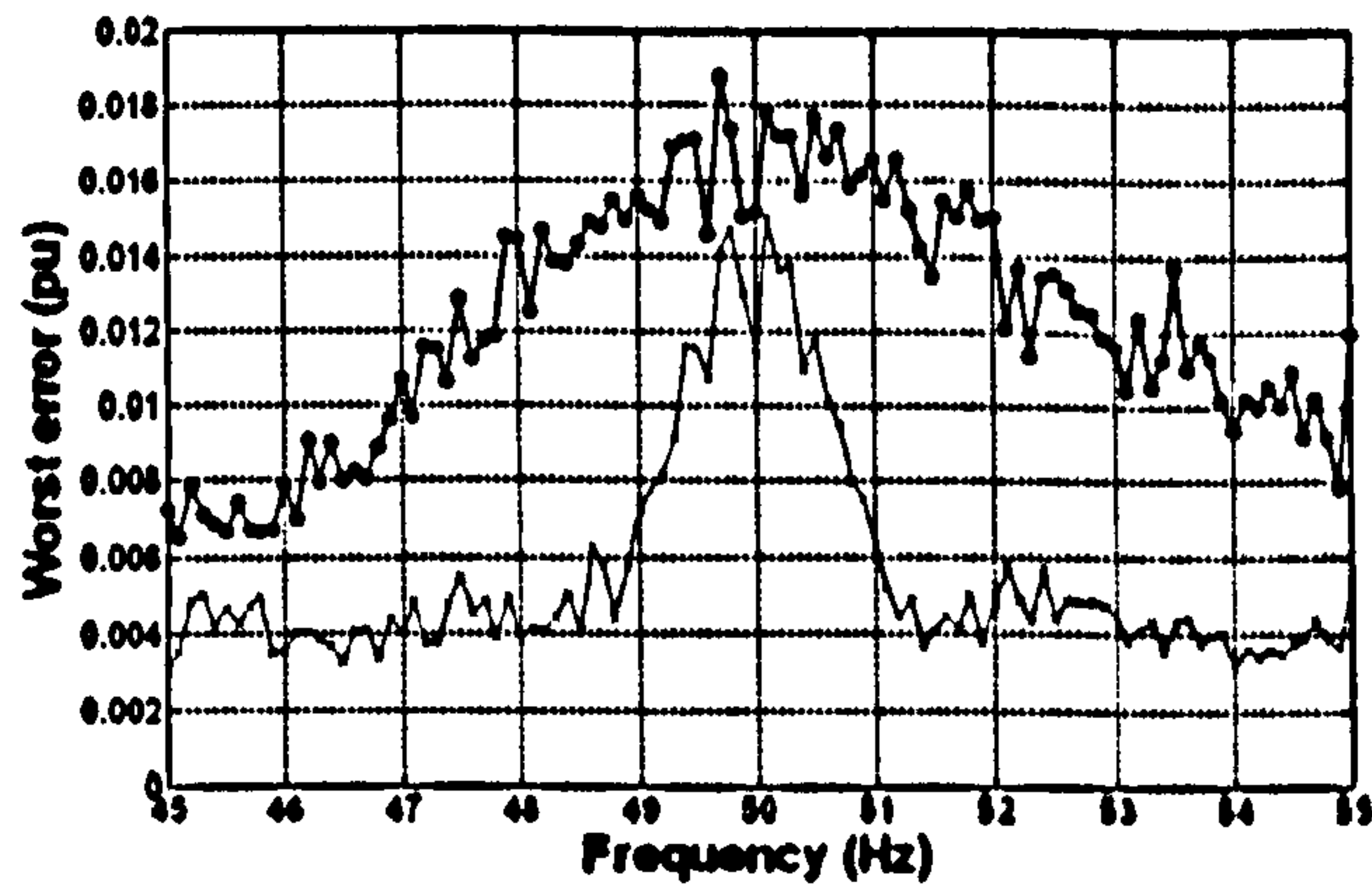


Figure 4-31 : Worst case Fourier fundamental amplitude measurement errors (pu) for voltage waveforms with up to 53% THD_v, at 500Sa/s, against input frequency. Without (black o) and with (blue x) ripple removal filter

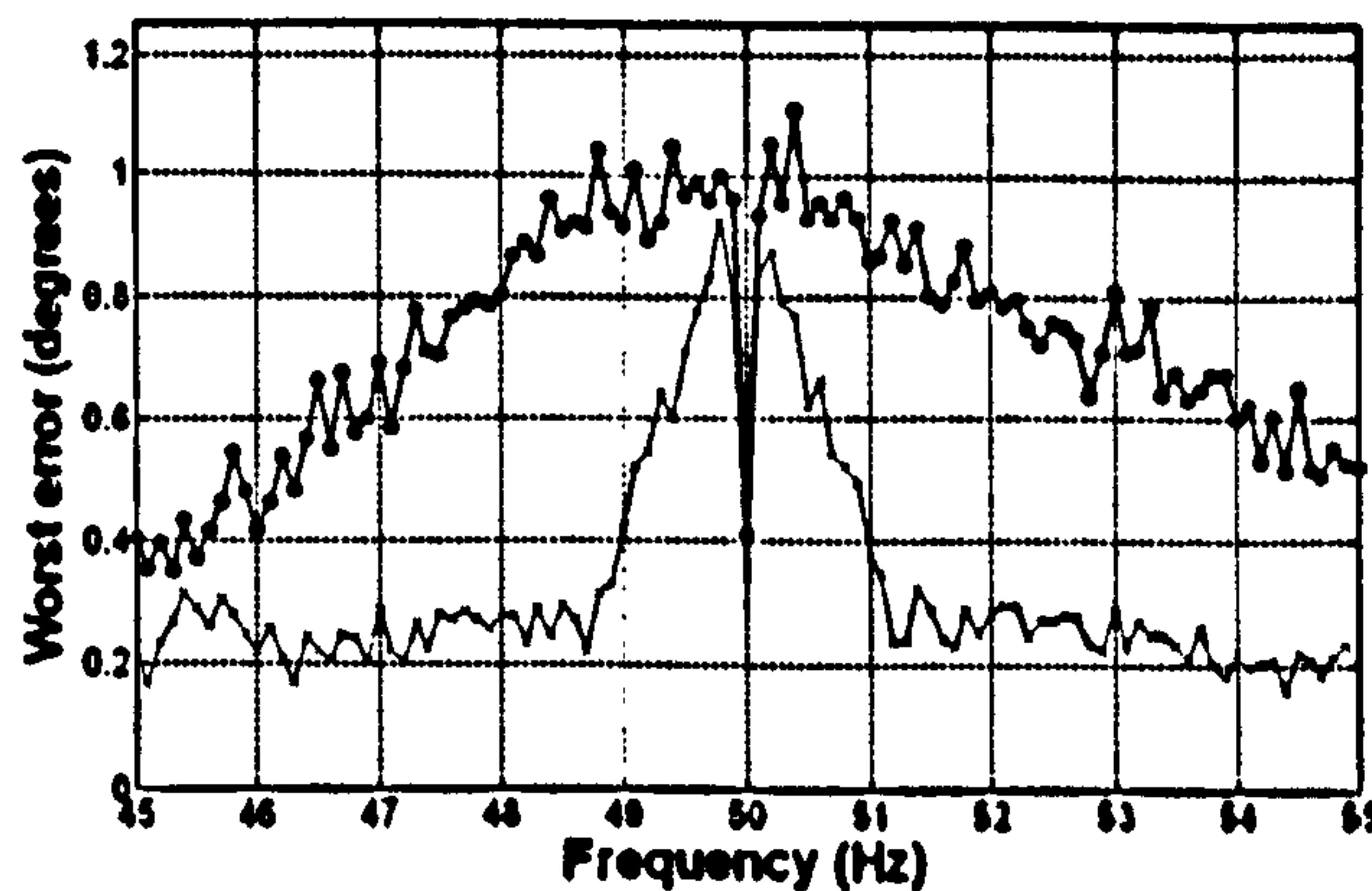


Figure 4-32 : Worst case Fourier fundamental phase measurement errors (degrees) for voltage waveforms with up to 53% THD_v, at 500Sa/s, against input frequency. Without (black o) and with (blue x) ripple removal filter

When the phase error is examined against frequency, a slightly different phenomena is observed. In this case the errors are again worst around 50Hz, but at exactly 50Hz the error appears to drop sharply. This is because, in the applied waveform, the odd harmonics are all applied at a coherent zero phase relative to the fundamental, which gives the worst case amplitude errors (see sections 2.7.2 and 4.2.2). If these phases were randomised a little, then Figure 4-32 would not show the dip at exactly 50Hz, and the figure should be interpreted as if that were the case.

The analysis can easily be repeated with a scenario which is relaxed to the harmonic content listed in

Table 2-6, (THD_v=28.2%). This waveform still contains approximately double the THD which would arise if all harmonics 2-40 were added together at the maximum individual levels allowed under BS EN 50160. This exceeds the total BS EN 50160 specification for total THD (8%) by a factor of 3.5, and is still a severe test scenario. Under these conditions, the

table of worst expected errors reduces to:

	Fundamental amplitude absolute error (peak pu)	Fundamental amplitude ripple magnitude (\pm pu)	Fundamental phase error (peak degrees)
0.5-cycle latency measurement "0.5(NC)"	0.039	0.035	2.5
1-cycle latency measurement "1(NC)"	0.014	0.013	1.0
1-cycle (with 2 nd harmonic cancellation) "1(C)"	0.017	0.014	1.0
1.5-cycle latency measurement "1(NC)+0.5"	0.012	0.012	0.8
5-cycle latency measurement "1(NC)+0.5+RippleRemoval"	0.009	0.009	0.6

Table 4-3 : Worst case Fourier fundamental measurement errors for voltage waveforms with up to 28.2% THD_v, at 500Sa/s

The data from Table 4-2 and Table 4-3 should not be used to predict approximate errors for THD levels below 28.2% via extrapolation based upon a lower known THD level. This is because below this level, the noise and ADC noise/quantisation errors may become dominant (see Figure 3-70 and Figure 3-71). Increasing the sample rate or decreasing the instrumentation noise can both reduce these errors. Increasing the sample rate initially will cause the errors to vary approximately with SampleRate^{-1} , as shown by Figure 4-21. This rate is a combination of the decrease in noise error which varies with $\text{SampleRate}^{-1/2}$ and the decrease in errors due to aliased harmonics, integration/interpolation etc which falls faster than SampleRate^{-1} . The errors due to aliased harmonics drop almost completely to zero when sample rate is above 80 samples per cycle, this is because above this level all the harmonics 2-40 are not aliased. Only the harmonics above 40 will still cause problems.

Below, a third table shows how the error magnitudes change for the 28.2% THD_v case, if the instrumentation is improved:

- Instrumentation noise is lowered from 0.005pu to 0.001pu RMS (46dB to 60dB SNR)
- ADC noise (above normal quantisation) is reduced from 2 bits RMS to 1 bit RMS
- Sample rate is increased from 10 Sa/cycle to 16 Sa/cycle @ 50 Hz (800 Sa/s)

	Fundamental amplitude error (peak pu)	Fundamental amplitude ripple magnitude (\pm pu)	Fundamental phase error (peak degrees)
0.5-cycle latency measurement "0.5(NC)"	0.028	0.028	1.5
1-cycle latency measurement "1(NC)"	0.004	0.004	0.25
1-cycle (with 2 nd harmonic cancellation) "1(C)"	0.004	0.004	0.25
1.5-cycle latency measurement "1(NC)+0.5"	0.003	0.003	0.25
5-cycle latency measurement "1(NC)+0.5+RippleRemoval"	0.002	0.002	0.2

Table 4-4 : Worst case Fourier fundamental measurement errors for voltage waveforms with up to 28.2% THD_v, at 800Sa/s

Clearly, comparing Table 4-3 with Table 4-4, the decrease in noise, and particularly the increase in sample rate to 16 Sa/cycle, reduce the worst case errors and ripple substantially. This was predicted in section 4.2.7

Also, it can be seen that the ripple magnitudes are almost identical to the peak absolute error magnitudes. This is because the worst errors usually occur due to low-frequency (sub-14Hz) ripples. These don't cause any DC offset to the overall measurement, hence the absolute error peak magnitude is almost identical to the 1-sided ripple magnitude.

An important conclusion at this point is that the outputs of the 1½-cycle and 5-cycle measurements meet all but one of the requirements laid down in section 2.10. The amplitude ripple target of $\pm 0.001\text{pu}$ with a 5-cycle measurement for control purposes (Table 2-12) cannot be met by a digital measurement using sampling at below 17 samples per cycle for the worst microgrid harmonic content cases with 53% or 28% THD_v. This is due to low-frequency ripples on the Fourier amplitude measurements caused by aliased harmonics. Ripple at >14Hz can be removed by the ripple removal filter, but when the ripple is at lower frequencies than this, approaching DC, the ripple cannot be removed by the post-filtering within the allowable 5-cycle measurement latency time. There are 3 possible solutions to this problem:-

- 1) Increase the sample rate of the entire system above 16 samples per cycle. This may not be possible, due to the overall CPU burden.
- 2) Increase the performance of the analogue-anti-aliasing filters. Designing such an analogue filter with increased attenuation above the cut-off frequency, without increasing the group delay significantly, is an extremely difficult or impossible task. Such a filter would need to be individually designed for any specified cut-off frequency, taking into account circuit layout and parasitic component tolerances which may change between component batches (Kuhlmann, 2007).
- 3) A third solution is to clock the ADC at a higher rate than 16 samples per cycle and perform a very simple digital pre-processing/filtering task at this higher sample rate to remove the harmonics which would otherwise cause the worst errors. Then the data can be down-sampled and passed to the above algorithms at sample rates down to 10 samples per cycle. This solution is the chosen method, and is examined in further in section 4.5.

A further summary revision of findings thus far is that:-

- The sample rate does not need to be an integer multiple of the nominal frequency and synchronisation with zero-crossings is not required.
- For simulation purposes, the 2nd order algorithms are useful for reducing the ripple on the measurements due to integration and interpolation.
- In real applications with noise and harmonic content, the advantage of the 2nd order algorithms is usually lost. The dominant effects are noise content, ADC quantisation, and aliased harmonics above the Nyquist frequency. The 2nd order algorithms can still safely be used since they do not produce any worse results than the 1st order algorithms.
- The 1-cycle latency algorithm using 2nd harmonic cancellation can produce worse results than the 1-cycle latency algorithm without cancellation, under conditions of high noise and THD (see Table 4-3). This is due to oscillations which may result due to the FIR nature of the cancellation algorithm. Therefore, unless instrumentation noise and harmonic content is low, this technique is best avoided. It also adds significantly to the burden on the CPU.
- The all-harmonic RMS measurements at 10 samples per cycle can be inaccurate by up to 15% in the worst-case microgrid scenario described, with a tendency to read low. The error cannot be removed by post-processing averaging.
- THD measurement at 10 sample per cycle can be in error by as much as 50% in the scenario described (normally reading low), and the error cannot be removed by post-processing averaging.

4.5 Addition of ADC over-sampling and notch pre-filtering stage before down-sampling

In the previous section, it was concluded that the only available way to achieve the amplitude measurement ripple target (for control purposes) of $\pm 0.001\text{pu}$ (from Table 2-12), while clocking the bulk of the algorithm at 16 samples per cycle or slower, is to apply some simple ADC oversampling and pre-filtering to remove the worst harmonics, before down-sampling to the normal clock rate in the main algorithms.

A repeat of the analysis of section 4.2.5.2 (which is a prediction of the magnitude of the expected errors, and does not account for the ripple removal filter of section 4.3), allows us to predict the worst offending aliased harmonics for any proposed sample rate of the main algorithms. Taking a target of 10 samples per cycle with a 50 Hz nominal frequency, this is a sample rate of 500 Sa/s. The analysis under this scenario shows the magnitudes of the errors (ripples) due to different harmonics becoming aliased when sampled at this rate. The results are shown below in Figure 4-33.

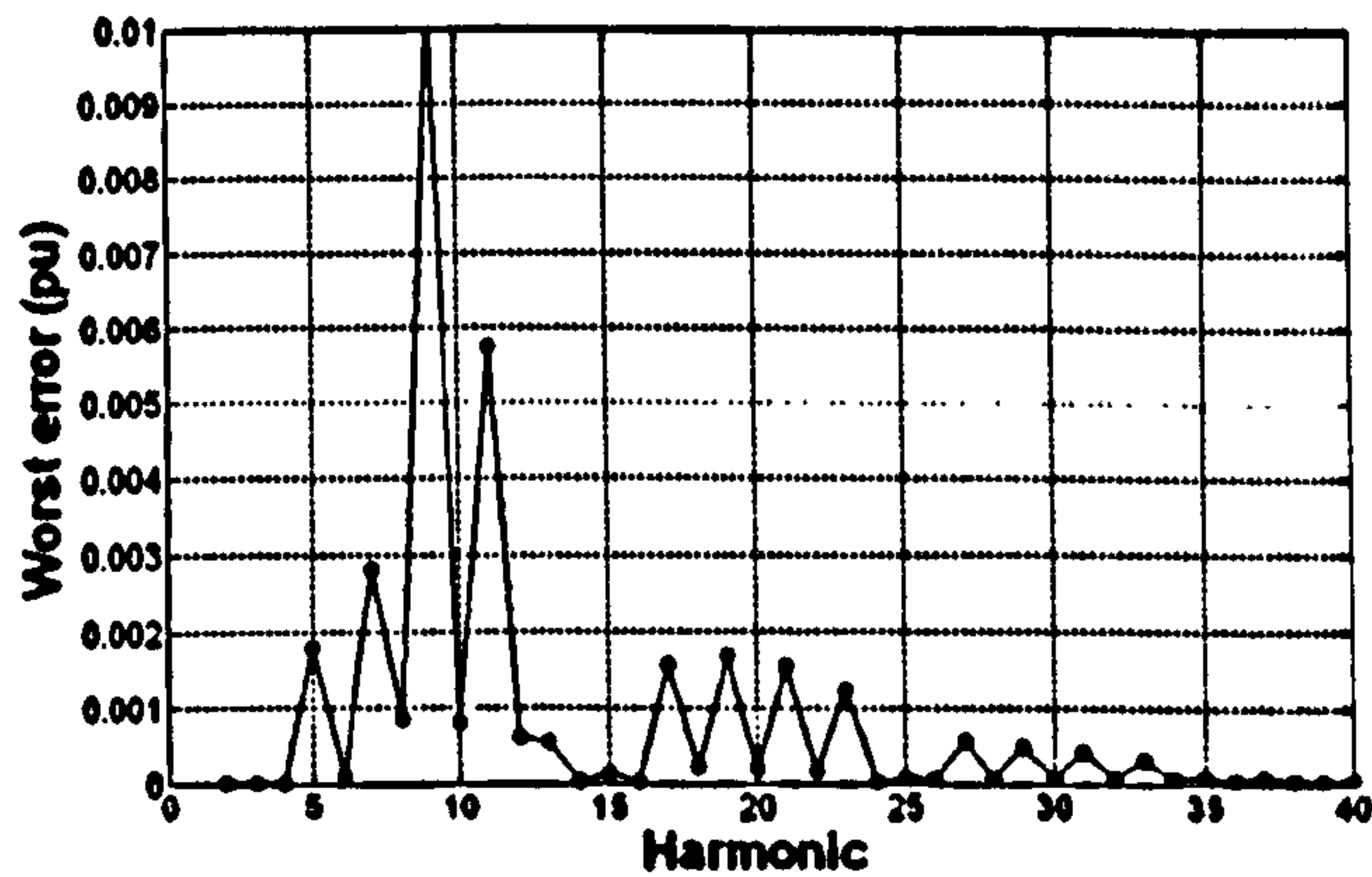


Figure 4-33 : Relative effect of aliased harmonics on errors/ripple, ignoring the effect of the ripple-removal filter

The target is to get below ± 0.001 pu ripple, therefore it may be necessary to remove all the following harmonics: 5th, 7th, 9th, 11th, 17th, 19th, 21st & 23rd.

However, further analysis of the potential ripple frequencies due to the aliased harmonics, for any fundamental in the range 45 to 55Hz, shows that the ripples due to some of these harmonics can be removed using the ripple removal filter. Only those that can result in ripples at frequencies of less than ≈ 15 Hz will pass un-attenuated through the ripple removal filter.

Harmonic	Harmonic frequency range for fundamentals in the range 45-50-55Hz	Expected maximum ripple error magnitude due to digital processing at 500Sa/s (10Sa/cycle @ 50Hz), For any fundamental in the range 45-55Hz	Lowest ripple frequency after Fourier analysis, due to digital processing at 500Sa/s (10Sa/cycle @ 50Hz), For any fundamental in the range 45-55Hz. Also, harmonic frequency "danger" range to cause <15Hz ripple.	Needs to be removed?
5 th	225-250-275 Hz	0.002	170	NO
7 th	315-350-385 Hz	0.003	60	NO
9 th	405-450-495 Hz	0.01	0 (436.5 to 463.5 Hz danger area)	YES, by 20dB in danger area
11 th	495-550-605 Hz	0.006	0 (533.5 to 566.5 Hz danger area)	YES, by 15dB in danger area
17 th	765-850-935 Hz	0.0015	15	YES, by 3.5dB
19 th	855-950-1045 Hz	0.0015	0	YES, by 3.5dB
21 st	945-1050-1155 Hz	0.0015	0	YES, by 3.5dB
23 rd	1035-1150-1265 Hz	0.0012	0	YES, by 1.6dB

Table 4-5 : Harmonics to attenuate using over-sampling and pre-filtering

So, there are 6 harmonics which, if removed from the final signal at 500 Sa/s, should allow the $\pm 0.001\text{pu}$ ripple specification to be approached. This needs an initial ADC sampling of at least 60 Sa/cycle, 3000 Sa/s, i.e. 6x over-sampling, to be able to successfully capture and filter the 23rd harmonic of a 55 Hz input waveform. The harmonics of greatest significance are the 9th and 11th. (To remove only these two harmonics would require at least 3x over-sampling at 1500 Sa/s).

The next step is to design a filter to reject these harmonics, remembering that each may appear over a range of frequencies for a fundamental in the range 45Hz to 55Hz. The down-sampling factor from a 3000 Sa/s ADC to the 500 Sa/s main processing is 6. This factor sets the number of FIR samples/weightings which are used, and also (after subtracting 1) the number of zeros which can be placed during the FIR filter design.

Note that there are 6 harmonics to be removed, but only 5 available zeros, which must occur in conjugate pairs. Therefore, some of the zeros must be placed strategically to cover multiple harmonics. From Table 4-5, and accounting for the fact that the Nyquist frequency of the 3000 Sa/s ADC system is 1500 Hz, the location of the zeros is chosen to be:-

- 1500Hz (single zero, conjugate of itself)
- $\pm 467\text{Hz}$ (pair of zeros, to cover the lower frequencies of the 9th)
- $\pm 840\text{Hz}$ (pair of zeros, to cover the higher frequencies of the 9th, the 11th, and the higher harmonics)

Such a filter can be designed and optimised using a MATLAB script. It's zeros, poles, and bode plot are shown below. The dashed red line on the bode plot of Figure 4-34 is the specification for required attenuation, defined by Table 4-5. The FIR weightings of the 6 samples are:-

- 0.23850705983587, 0.06142383205831, 0.20006910810582, 0.20006910810582, 0.06142383205831, 0.23850705983587

Note that due to the attenuation at 50Hz, the weightings must also be multiplied by the required value to bring gain at 50Hz back to unity (0dB). Additionally, a polynomial of order 2 can be fitted in the region of 40-50-60Hz to create a fitted function for the gain correction, which covers eventualities when the input signal is not at 50Hz. This process should also be used to correct the phase of the measured waveforms, although the phase correction only requires a linear slope. For the filter designed above, the correction terms

determined by this process are:-

- Gain correction = $0.00000796849357 \cdot f^2 - 0.00003983954291 \cdot f + 1.00072712529167$
- Phase correction (radians) = $0.00523598775598 \cdot f$

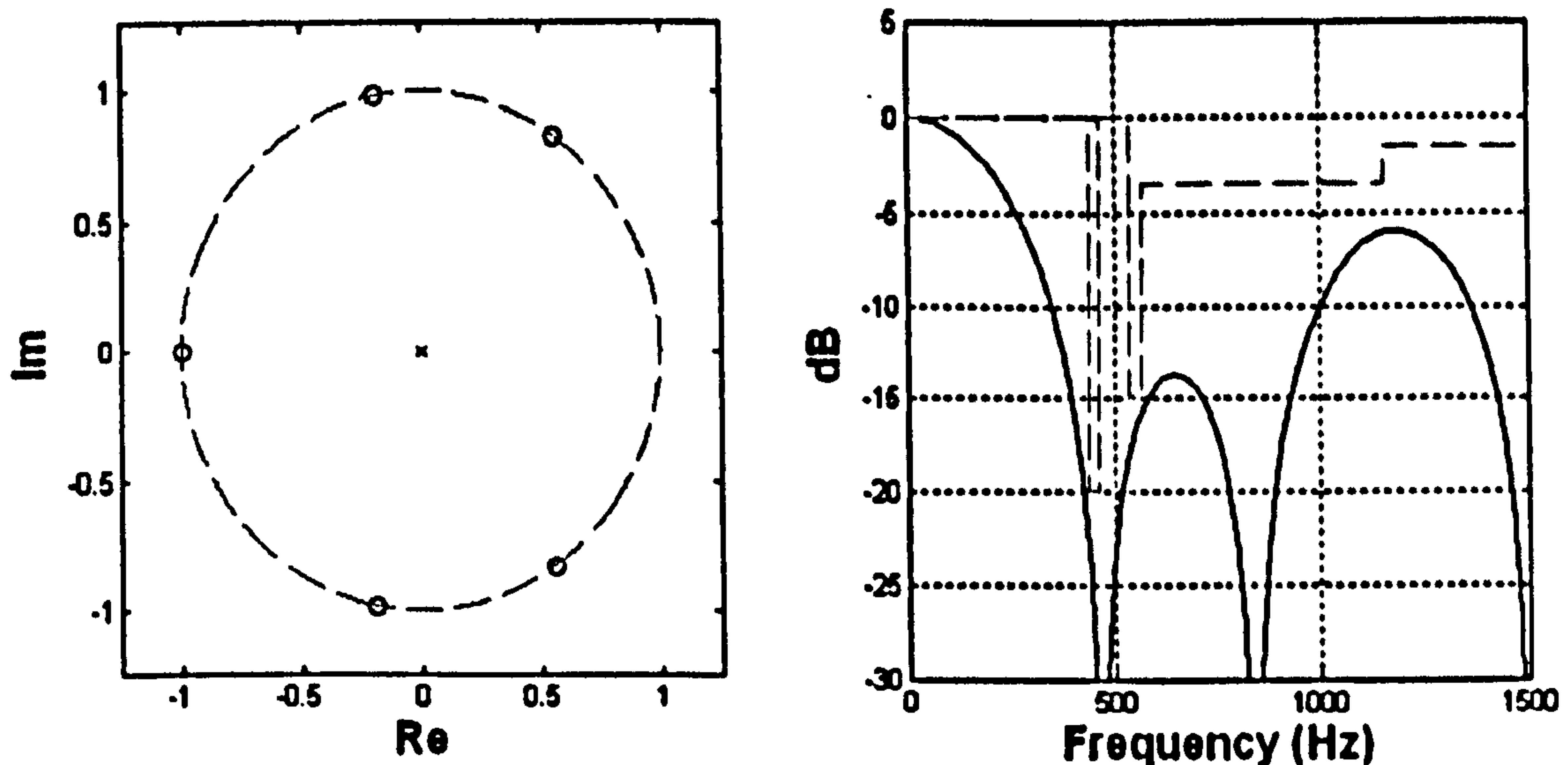


Figure 4-34 : Zeros, poles and bode plot for 3000 Sa/s over-sampling pre-filter (Nyquist frequency 1500 Hz)

Thus, it can be seen that a 6-times over-sampling at the ADC, at 3000 Sa/s, combined with a very simple 6-sample (5-zero) FIR filter, can be used to notch out the worst problem harmonics. After this step, the output of the FIR filter can be down-sampled so that 1 of every 6 results is forwarded to the main processing algorithms at 500 Sa/s. This should allow the main Fourier-based/averaging/ripple removal algorithms at 500 Sa/s to meet or come close to the ± 0.001 pu ripple specification. Note, the measurements of all-harmonic RMS and THD will definitely be invalid when using this pre-filter, since the 5th and 7th harmonics have been deliberately notched out of any subsequent signal analysis.

Such a process can be carried out on a commercial micro-controller such as the TC1796 by using the peripheral control processor for the ADC and over-sampled algorithms, and then passing the data to the main processor for the lower sample-rate, higher burden algorithms. On the ADI RTS, such a system can be implemented by clocking one of the processor cards, which handles the ADC/DAC inputs/outputs and also carries out the pre-filtering, at the over-sampled rate. The filtered data is then passed via the internal VME bus to one of the other processors at the lower clock frequency (500 Sa/s).

On the ADI RTS at present, the highest theoretical ADC clock rate is 1562.5 Sa/s due to the pas9737 ADC cards which take at least $64 \cdot 10 \mu s = 640 \mu s$ ($1/1562.5$ s) to multiplex though all 64 channels each frame. Therefore, for proving these algorithms on the ADI RTS, the pre-

filtering must be redesigned to allow for only a 1500Sa/s (3x) oversampling, relative to the main 500 Sa/s algorithms. This will not allow the overall measurement system to meet the ± 0.001 pu ripple specification for 53% THD waveforms, but for cleaner waveforms it will give the best results possible with the current hardware constraints. Since THD on the Strathclyde microgrid at present is normally better than 5%, this does not present a problem in the short term.

For the 1500 Sa/s (3x over-sampling) version, the zeros are placed at ± 482 Hz. The filter weights are [0.34883448605115, 0.30233102789770, 0.34883448605115]

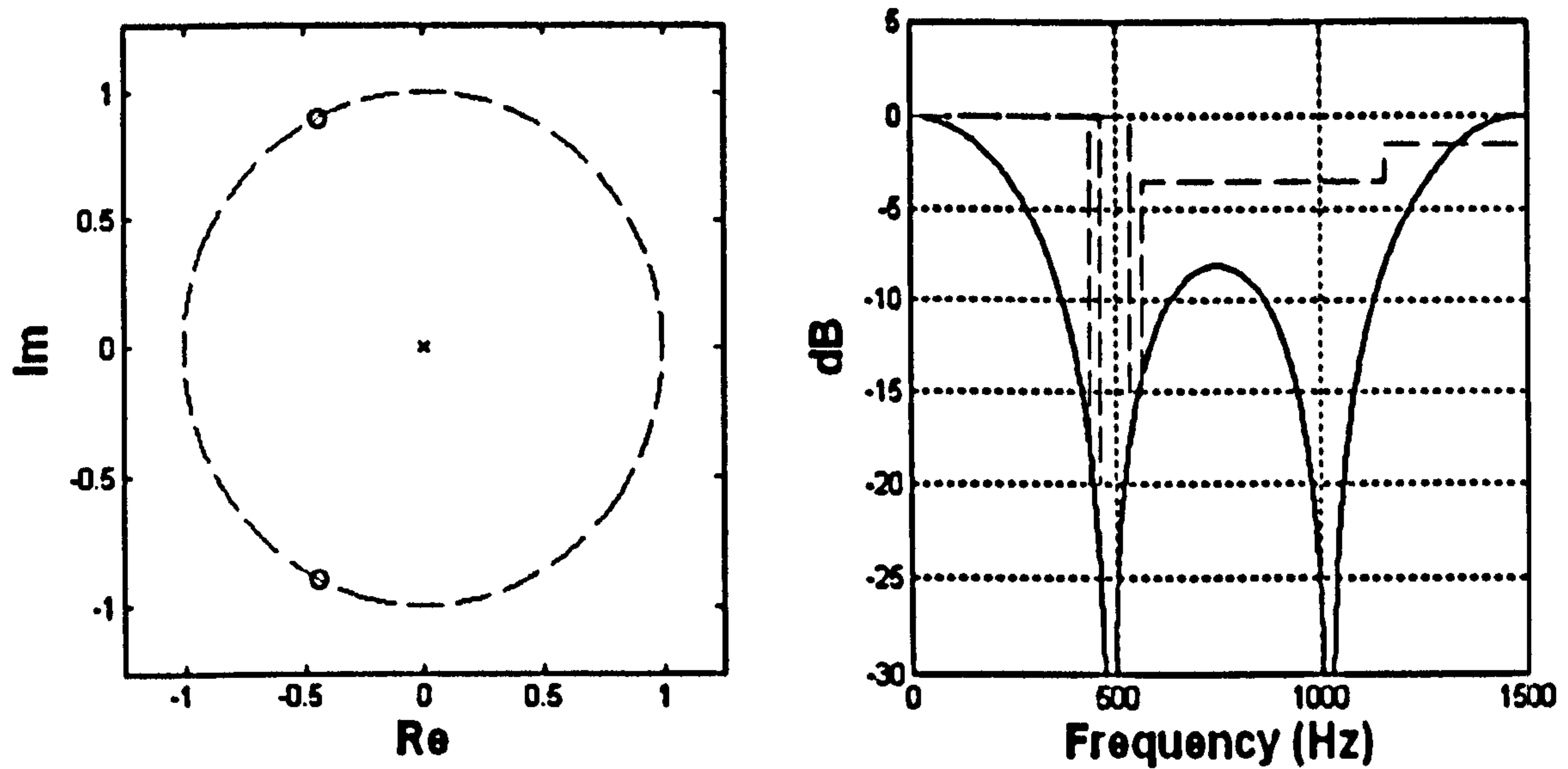


Figure 4-35 : Zeros, poles and bode plot for 1500 Sa/s over-sampling pre-filter (Nyquist frequency 750 Hz)

4.5.1 Analysis of performance improvement using 3000Sa/s over-sampled ADC and FIR pre-filtering

ADC over-sampling and FIR pre-filtering at 3000 Sa/s was added to the simulations of section 4.4. This results in the following table of errors for the worst microgrid case. This table is generated using the identical test conditions to those used for Table 4-2.

	Fundamental amplitude error (peak pu)	Fundamental amplitude ripple magnitude (\pm pu)	Fundamental phase error (peak degrees)
0.5-cycle latency measurement "0.5(NC)"	0.027	0.025	1.8
1-cycle latency measurement "1(NC)"	0.0100	0.0075	0.55
1-cycle (with 2 nd harmonic cancellation) "1(C)"	0.0080	0.0072	0.52
1.5-cycle latency measurement "1(NC)+0.5"	0.0045	0.0040	0.27
5-cycle latency measurement "1(NC)+0.5+RippleRemoval"	0.0028	0.0023	0.17

Table 4-6 : Worst case Fourier fundamental measurement errors for voltage waveforms with up to 53% THD_v, at 500Sa/s, using 6x over-sampled FIR pre-filter

An additional point of note is that during the above experiment, the threshold for transient detection within the ripple filter can be set as low as about 0.005pu without causing any spurious transient detections. This means that the ripple-removal filter can be applied to the 1½-cycle measurement, and any transient of $> \pm 0.005\text{pu}$ magnitude will be tracked with only the 1½-cycle latency, as the ripple removal filter will pass the data straight through. During steady-state operation, the ripple-removal filter will switch on automatically and provide an output with much lower ripple, suitable for control purposes.

As Table 4-6 shows, the required ripple specification of $\pm 0.001\text{pu}$ is still not quite met at the 5-cycle measurement output. If, however, the instrumentation noise level can be dropped from 0.005pu RMS (46dB SNR) to 0.001pu RMS (60dB SNR), the additional ADC bit noise is dropped from 2 bits RMS to 1 bit RMS, and the THD_v of the waveform is dropped from 53% to 28%, the specification for $\pm 0.001\text{pu}$ ripple on the Fourier amplitude measurement can finally be met. The results are shown in Table 4-7.

	Fundamental amplitude error (peak pu)	Fundamental amplitude ripple magnitude ($\pm\text{pu}$)	Fundamental phase error (peak degrees)
0.5-cycle latency measurement "0.5(NC)"	0.025	0.023	1.4
1-cycle latency measurement "1(NC)"	0.0051	0.0041	0.27
1-cycle (with 2 nd harmonic cancellation) "1(C)"	0.0035	0.0031	0.22
1.5-cycle latency measurement "1(NC)+0.5"	0.0017	0.0014	0.10
5-cycle latency measurement "1(NC)+0.5+RippleRemoval"	0.0011	0.0010	0.08

Table 4-7 : Worst case Fourier fundamental measurement errors for voltage waveforms with up to 28.2% THD_v, at 500Sa/s, using 6x over-sampled FIR pre-filter

4.6 Verification of amplitude measurement errors with closed-loop frequency measurement

In chapters 3 & 4, apart from the analysis of 4.1, it was assumed that the measurement of frequency was perfect. In chapter 5, a frequency/amplitude/phase measurement algorithm (the Clarke-FLL hybrid) is designed and presented. In the following section, the amplitude measurement accuracy of this is further tested in a closed-loop situation using suitable test waveforms.

First, test waveform 1B is used (see section 2.11.1). This waveform has 28% THD_v, plus

unbalance and inter-harmonics, plus dynamic frequency and voltage dip events as described in Table 2-16. The frequency profile is shown in Figure 5-18.

The specification lines for the fundamental amplitude measurement on each of the three phases were set at ± 0.001 pu from the actual applied values (matching the original requirement from Table 2-12), unless frequency was less than 10 Hz in which case a much wider specification was set. Accuracy is not good below 10 Hz, due to the finite length of the correlation/averaging buffers inside the Fourier analysis which are set to ≈ 50 samples long (i.e. a 10 Hz signal with a sample rate of 500 Sa/s can be measured accurately). From $t=8$ s onwards in the simulations, the magnitudes on each phase are different to each other due to the negative sequence component applied. The specification lines take into account an allowed reaction time of 40ms (nominally 2 cycles at 50Hz, see Table 2-11). This timeframe accounts for the hardware filtering and ADC, plus the $1\frac{1}{2}$ cycle measurement time within the main algorithm (see section 4.7). A ripple-removal filter with maximum latency of 70ms was used (see section 4.3). To meet the reaction time specification of 40ms during transient effects, this filter has to switch itself out automatically and pass the signal straight through.

The cumulative error score for the magnitude measurements, as determined by the same scoring system given in section 5.7 for the frequency tests, is of the order of 0.5 to 0.65 during the waveform 1B test. This means that, on average, over the 60 seconds of the test, the measurement was 50% outside the specification window of ± 0.001 pu. Closer analysis reveals when and why this occurs.

First, a plot of the phase A voltage magnitude measurement against the specification is shown for the first 16 seconds of the simulation. During this time there are significant amplitude variations due to dips on one, two and three phases.

On all the graphs which follow, the traces are identified as follows:-

- Black solid line : Measurement
- Red dash-dot : Actual synthesised signal amplitude
- Blue dashes : Lower and Upper limit lines

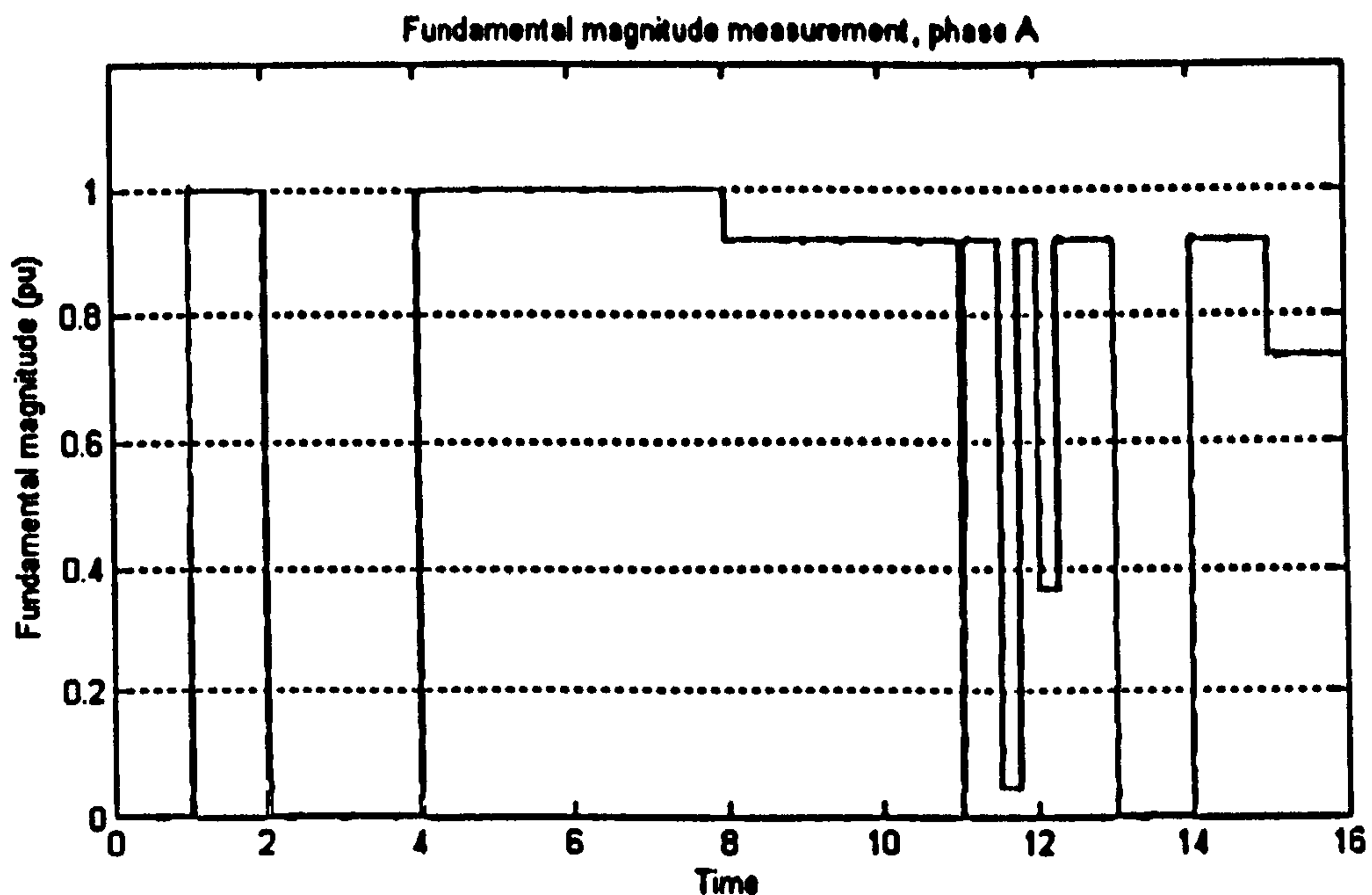


Figure 4-36 : Amplitude measurements, waveform 1B, phase A, t=0 to 16s

Figure 4-36 show the overall shape of the signal magnitude on phase A, and that the measurement follows the signal. The scales do not allow the errors to be examined in detail (no deviations from specification are apparent), and this figure merely gives an overview of the scenario. The plots for the phase B & C measurements look almost identical, and are not shown here. For a more meaningful analysis, the actual measurement errors can be shown at significantly higher magnification for several interesting parts of the scenario. These plots are shown in Figure 4-37 to Figure 4-39.

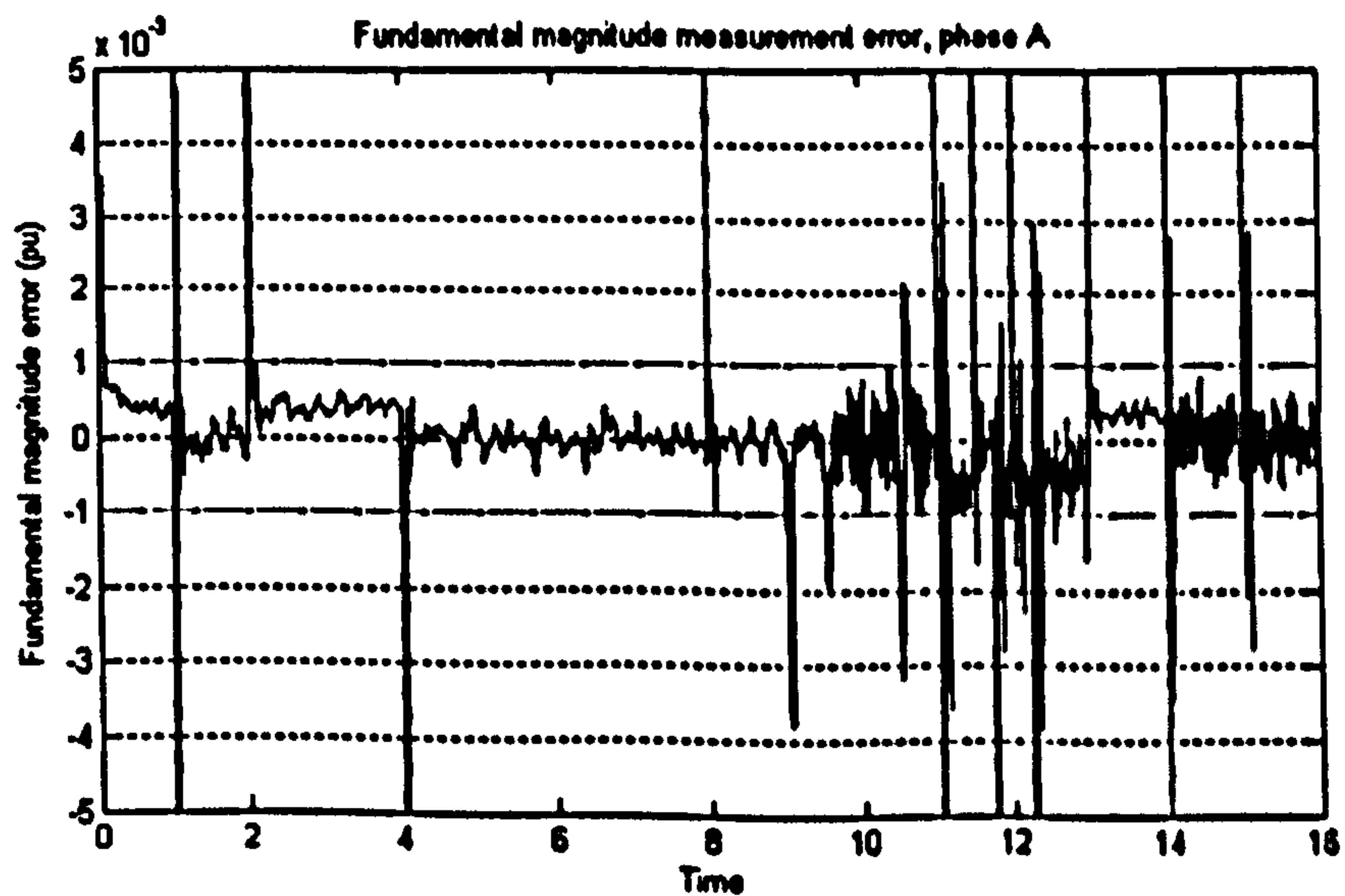


Figure 4-37 : Amplitude measurement errors, waveform 1B, phase A only, t=0 to 16s
The errors, normalised to the actual signal magnitudes, are generally within bounds, save for brief excursions during settling after transients. Even during transients the error is

mostly within specification, since the specifications (blue dashed lines) allow 40ms reaction time, and are significantly wider than ± 0.001 pu during transients. The plots for phases B & C are almost identical.

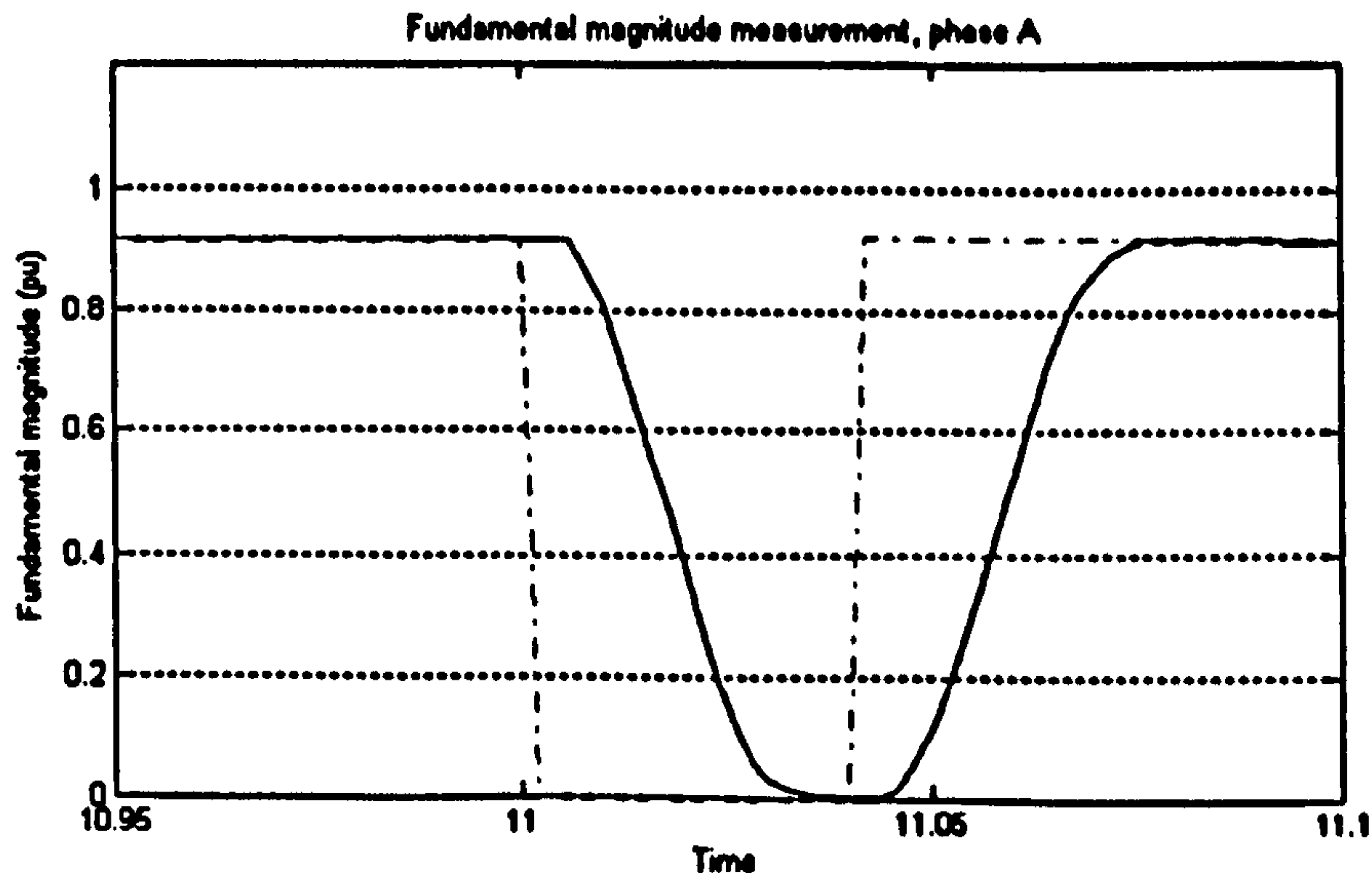


Figure 4-38 : Amplitude measurements, waveform 1B, phase A only, three-phase fault response

To show the measurement latency in detail, the plot above shows the timeframe of the brief three-phase fault (100% dip on all three phases) between $t=11$ s and $t=11.04$ s. The plots for phases B & C are almost identical.

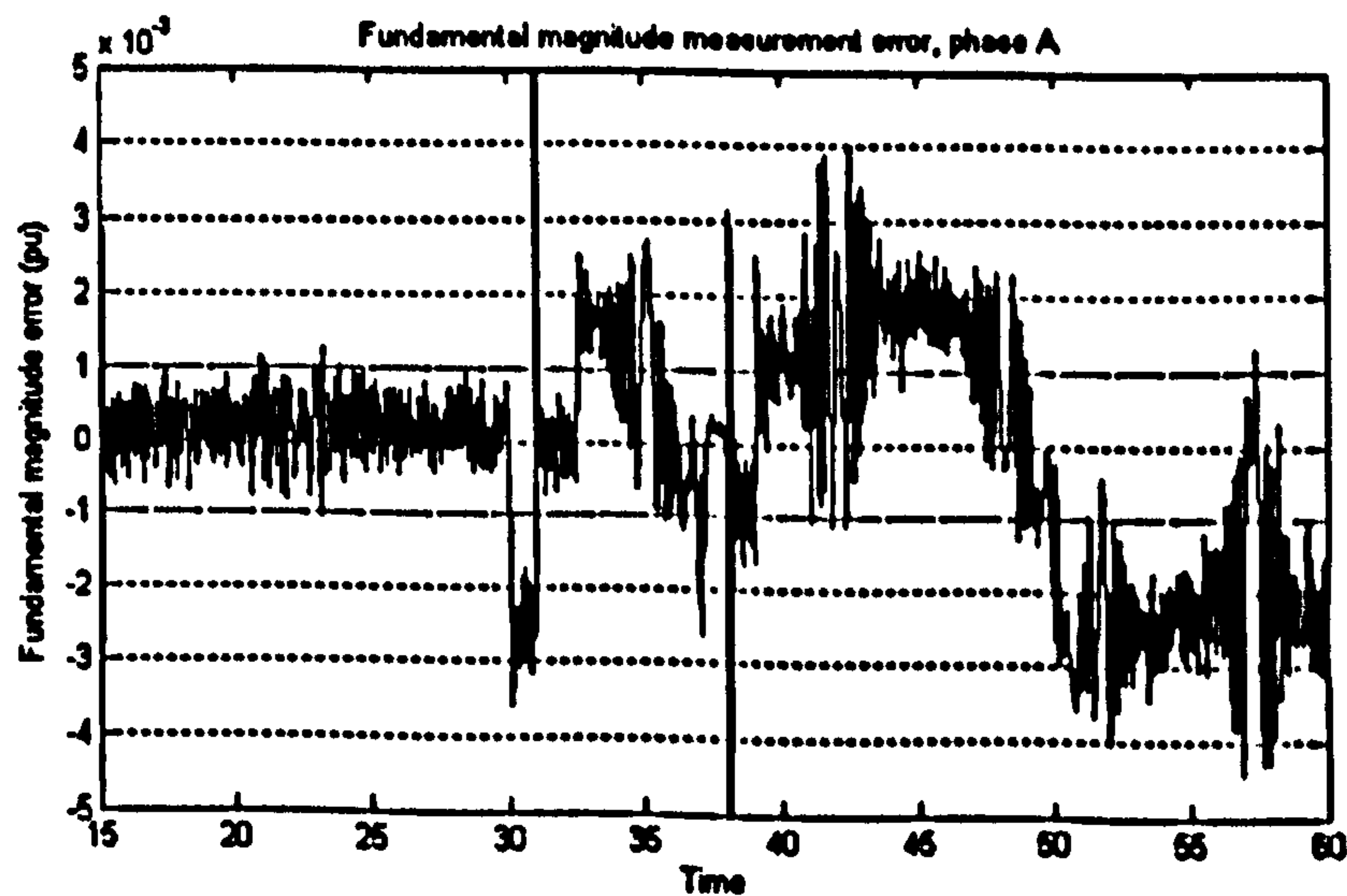


Figure 4-39 : Amplitude measurement errors, waveform 1B, phase A only, $t=15$ to 60 s

The plot above shows the measurement errors over the part of the simulation where the magnitudes are constant, but the frequency changes rapidly (see Figure 5-18). The main point of note is that the absolute specification is violated during the 10 Hz/s frequency ramps, by about a factor of 2. However, much of the ROCOF-induced violation consists of a

DC bias term, which will not cause ripples in any drooped control system. The plots for phases B & C are almost identical.

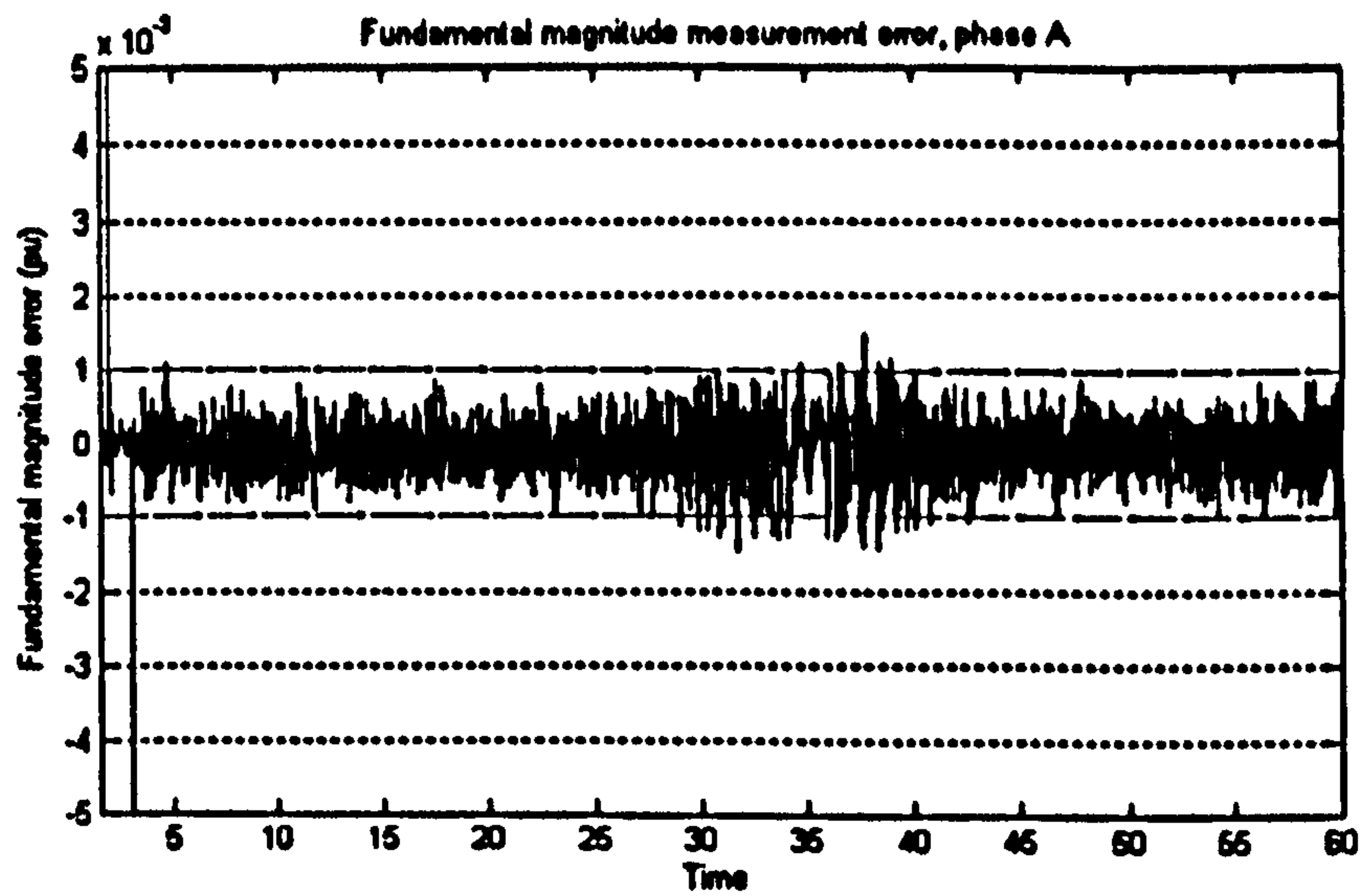


Figure 4-40 : Amplitude measurement errors, waveform 2B, phase A only, t=1.5 to 60s

The plot above shows the measurement errors for waveform 2B (see section 2.11.2), where the signal magnitudes are constant, but the frequency changes slowly (see Figure 4-41). Generally, the specification is met. Slight violations occur during the initial onset of unbalance at t=2s ($\approx 0.003\text{pu}$) and for certain worst input frequencies in the 49-51Hz bracket (t=30s to t=40s in the simulation, see Figure 4-41), due to the aliased harmonics (mainly the 9th and 11th) which are not fully attenuated within the over-sampled FIR filter (see section 4.5 and Figure 4-31). The plots for phases B & C are almost identical.

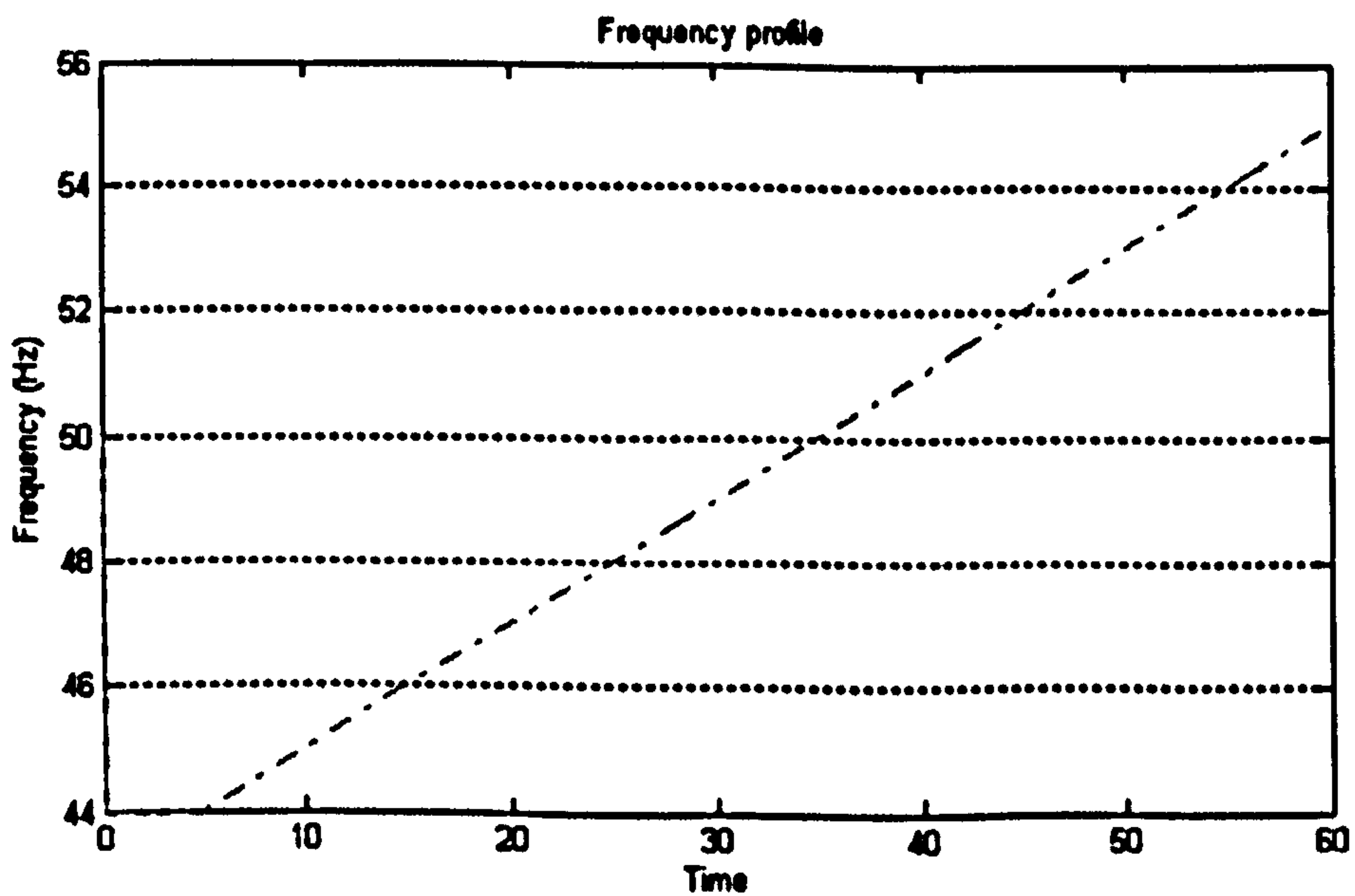


Figure 4-41 : Frequency profile, waveform 2B

The closed-loop frequency measurement does not add any serious problems to either the latency or the ripple of the amplitude measurements. The largest effect is during rapid frequency changes. At a ROCOF of 10 Hz/s, and absolute amplitude error rises to about 0.002pu (see Figure 4-39). However, the error tends to be a constant bias due to the frequency ramp, and is not an additional ripple error. This should not cause an oscillation problem within droop-controlled systems, and is thus tolerable.

The biggest ripple errors still occur, as found earlier, at the “worst frequencies” where aliased harmonics from high-THD waveforms fold back toward the fundamental. For main algorithms operating at 500 Sa/s, with nominal frequencies of 50 Hz, the 9th and 11th harmonic cause the worst problems. This is because for input frequencies near 50 Hz, they arise at about 450 Hz and 550 Hz respectively. These alias upon sampling at 500 Sa/s to almost exactly 50 Hz, and then cause beating with the genuine signal which is close to 50 Hz. The resulting ripple has been significantly reduced from potentially much higher levels by the use of the over-sampled FIR filter of section 4.5, and the novel ripple-removal filter of section 4.3.

Because the ripple-removal filter automatically switches itself out during transients (see sections 4.3 & 4.4 and Figure 4-38), the results shown in this section, which are taken from the output of the ripple-removal filter, generally meet both the low-ripple control requirements (Table 2-12) which require (up to) 5-cycle averaging, and the fast-acting relaying requirements (Table 2-11) which require 1½-cycle digital latency.

4.7 Overall findings from chapters 3 & 4, Amplitude/Phase measurement

Several different measurement architectures have been investigated and compared. The algorithm which is most appropriate depends upon the scenario (which is defined by the AC waveform quality and the measurement/computational hardware constraints). An extremely useful architecture selection process has been created (section 3.13.1). The primary focus of this thesis is upon achieving the best performance in conditions of instrumentation noise and high harmonic content, using the minimum sample rate possible for the bulk of the processing (500 Sa/s target). These constraints have influenced the selection of the optimal measurement architecture.

The architecture is based around cascaded use of FIR filters. FIR filters result in a robust, inherently stable algorithm with a minimum of settling ripple. They have also been shown (see section 3.3) to perform substantially better at noise removal than IIR low-pass

filtering techniques. The cascading of the FIR filters also serves to additionally limit the bandwidth of noise due to the windowing effect caused by the convolution of the filter impulse responses. The overall measurement strategy (with the main algorithms at 500 Sa/s) is shown in Figure 4-42, and includes the following stages:-

- A pair of cascaded RC filters for each phase (implemented by active or passive analogue circuits) with $F_c=125\text{Hz}$ ($\frac{1}{2}$ Nyquist at 500Sa/s). The filter cut-off frequency cannot be set much lower, or the filter order increased, due to the group delay which is incurred and its effect on transient response.
- ADC 6x oversampling (3000 Sa/s) or 3x oversampling (1500 Sa/s), with the ADC ranged over the -2 to +2 peak voltage span.
- FIR pre-filtering using a simple 6-tap (3kSa/s) or 3-tap (1.5kSa/s) FIR filter to notch out the worst problem harmonics which can alias back onto the fundamental in a 500Sa/s system. The filter notches out the most problematic 9th & 11th harmonics, and also to generally reduce the higher order harmonics.
- Down-sample to 500 Sa/s and pass data to the main processor.
- Removal of DC bias due to instrumentation, using a novel DC block based upon FIR averaging filters (section 3.4.4.2) which can be used over arbitrary timeframes, not necessarily integer multiples of the sample time. This filter has a zero group delay for the AC signals.
- Correction for gain slopes in the analogue low-pass filter and FIR filter, ADC channel-channel timing skews, and calculation of phase corrections which can be applied later in the process.
- Fourier correlations over a single or a half-cycle, optimised for speed, robustness, and re-use of calculations. Again, this uses the FIR averaging filter over an arbitrary timeframe.
- Additional averaging over a half or single cycle (using the FIR averaging filter again). This creates a $1\frac{1}{2}$ cycle latency measurement which has virtually zero integration/interpolation error despite the low sample rate used (500Sa/s) (see section 3.9).
- Further averaging using a novel, adaptive ripple-removal filter which adjusts its latency from 0 (during transients $>\pm 0.005\text{pu}$) to 3.5 cycles (70ms) so as to remove as much of the remaining ripple and noise as possible (see section 4.3). This algorithm again uses the FIR averaging filter which can average over an exact timeframe.
- Sequence and power flow analysis
- Final absolute phase calibrations

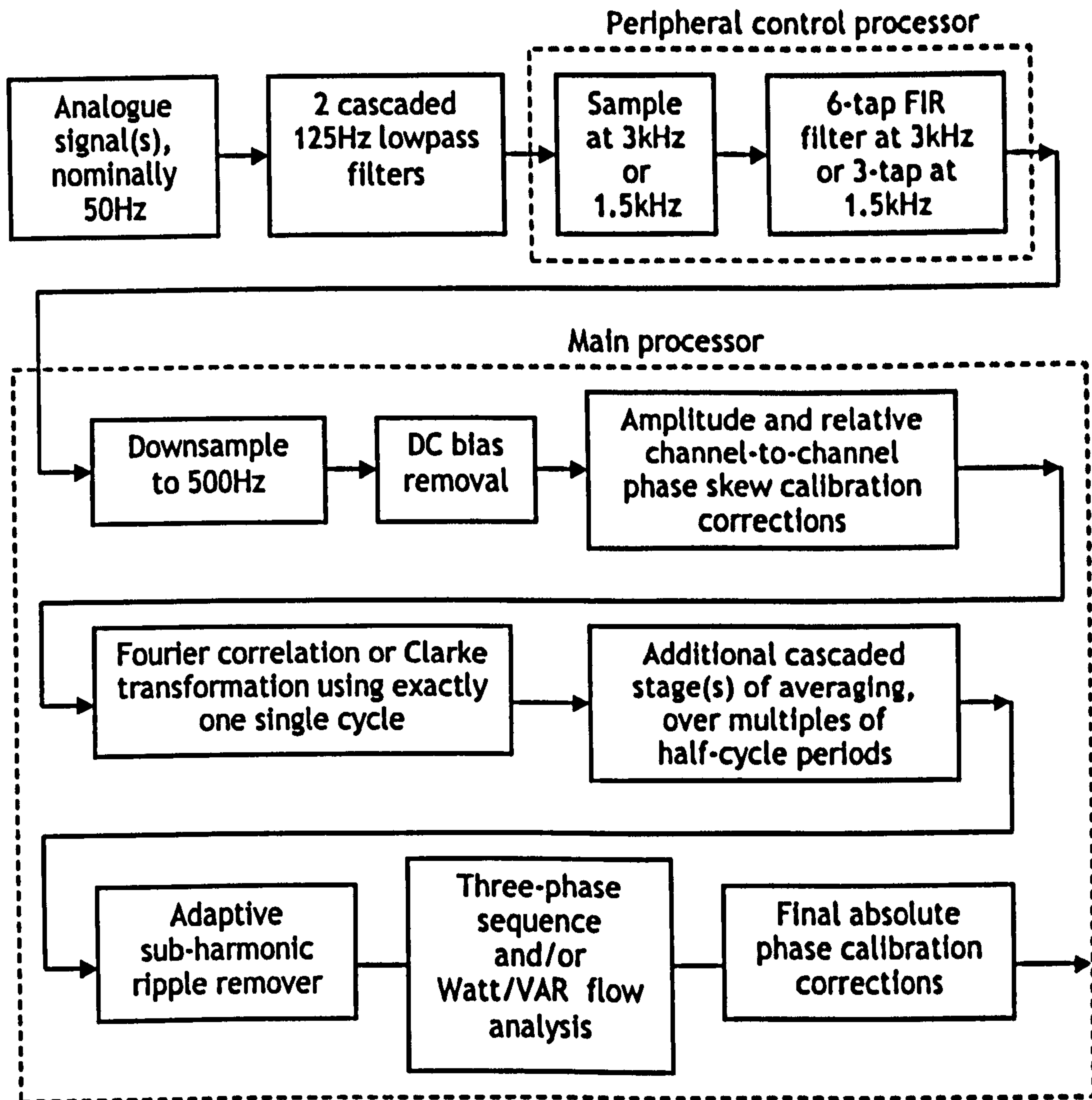


Figure 4-42 : Summary of the optimal measurement configuration for amplitude and phase measurement.

The final output is a $\approx 5\frac{1}{2}$ -cycle latency measurement (≈ 2 -cycle during transients) of extremely high precision and low ripple. The absolute error is limited mainly by the accuracy to which the peripheral hardware (VTs, isolation amplifiers, low-pass filters etc.) can be calibrated. The ripple error is dominated by the harmonic and noise content which remains after all the processing. The actual measurement latency is slightly longer than the 5 cycles taken by the main digital algorithms. This is due to an additional $\frac{1}{6}$ th cycle (steady state) to $\frac{1}{2}$ cycle (transient) latency due to the analogue anti-aliasing filter section which is a pair of cascaded low-pass filters with cut-off set to $f_c=125$ Hz as described in section 3.4.5. A further latency of $\frac{5}{12}$ ^{ths} of a sample¹ (at 500 Sa/s) ($\frac{1}{24}$ th of a cycle)

¹ The delay is calculated by $(6-1)/2/6$ where 6 is the over-sampling rate. This is the time from the latest sample back to the middle of the last set of over-samples leading up to the current sample.

delay is incurred in the ADC/pre-filtering section which executes at 3000 Sa/s (6x over-sampling).

The total measurement latency for the 5-cycle measurement will thus be approximately $5 + \frac{1}{2} + \frac{1}{24} = 5.54$ cycles. However, as described in 4.3, $3\frac{1}{2}$ cycles of the 5 cycle digital processing time is due to a ripple-removal filter. When a voltage transient of greater than 0.005pu occurs, this filter automatically detects the transient and passes the measured signal straight through un-filtered. Thus, during transient events, the latency of the total measurement system drops from 5.54 to 2.04 cycles.

For the most time-critical measurements, the $1\frac{1}{2}$ cycle measurement can be tapped off before the $3\frac{1}{2}$ cycle ripple removal filter. This results in a measurement with a latency of about 2.04 cycles at all times, with increased ripple and noise.

This measurement architecture, which is fully implemented and tested within this thesis, allows "Class A" measurement accuracies to be achieved but at a low frame rate and with short measurement latencies. The performance is summarised in Table 4-8 below.

	BS EN 61000-4-30 "Class A" performance	Performance of architecture developed in this thesis, normal scenario	Performance of architecture developed in this thesis, worst case scenario
Scenario	Harmonics up to 20% THD (twice times BS EN 61000-4-3 table 5, class 3) (BSI, 2002)	THD up to 28% Instrumentation noise level (before the ADC) at or below 0.001pu RMS (60dB SNR). A 12-bit ADC with a bit noise of no more than 1 bit RMS.	THD up to 53%. Instrumentation noise level (before the ADC) at or below 0.005pu RMS (46dB SNR). A 12-bit ADC with a bit noise of no more than 2 bits RMS.
Voltage measurement	$\pm 0.1\%$ (± 0.001 pu) A measurement time of 10 cycles (200ms), assuming steady state frequency	accuracy/ripple of ± 0.0011 pu/ ± 0.0010 pu respectively. A settling time of 2 cycles (40ms) during transients and 5.5 cycles (110ms) normally. Voltage amplitude error widens to ± 0.003 pu with ROCOF rates of ± 10 Hz/s, and proportionately with lower ROCOF rates.	accuracy/ripple of ± 0.0028 pu/ ± 0.0023 pu respectively. A settling time of 2 cycles (40ms) during transients and 5.5 cycles (110ms) normally. Voltage amplitude error widens to ± 0.003 pu with ROCOF rates of ± 10 Hz/s, and proportionately with lower ROCOF rates.

Table 4-8 : Performance of voltage amplitude measurement architecture proposed by this thesis, versus standard "Class A" performance

All but one of the original requirements for the measurement of fundamental amplitude and phase (section 2.10, Table 2-11 and Table 2-12) have been fully met by the algorithms presented in this chapter, for even the worst cases of harmonic content and instrumentation noise, with frame rates down to 10 samples per cycle. The hardest

specification to meet is the requirement for low ripple/noise on the Fourier measurement of amplitude, for measurements with 5-cycle latencies which are used for control purposes. The largest set of constraints on meeting this specification has been shown to be high harmonic content (THD above 28%) which might appear (even transiently), combined with low sample rates inside the main processing algorithms. Noise and ADC quantisation are also subsidiary contributors to the error ripple.

The original requirement was set at $\pm 0.001\text{pu}$ (Table 2-12), which is derived from the desire to keep reactive power output ripples to within a $\pm 0.01\text{pu}$ ripple range, where the reactive power ripples are caused by voltage measurement ripple, with a 10% voltage droop slope. Alongside this requirement, the original hardware constraints proposed in Table 2-12 were a main sample rate of 10 Sa/s, instrumentation noise at 0.005pu RMS (46dB SNR), and 2 bits of ADC noise. In this scenario, the algorithms presented give ripple of the order of $\pm 0.0023\text{pu}$ (Table 4-6) for waveforms with THD_v up to 53%. This would not be disastrous and could certainly be tolerated for short periods of time.

If the input waveforms have a THD_v up less than 28%, combined with a small improvement in the instrumentation performance, then the $\pm 0.001\text{pu}$ target is met (Table 4-7 & Table 4-8) and the architecture accuracy/ripple then meets the requirements for Class A performance, but with substantially lower measurement latency than Class A allows, and using a very low frame rate.

The phase measurement errors are within 0.18° (Table 4-6) for all scenarios up to 53% THD_v , and within 0.08° (the original requirement of Table 2-13) for the improved scenario with THD_v up to 28% (Table 4-7). This measurement of phase can therefore be used as the basis for a robust frequency measurement. This is investigated fully in chapter 5.

4.8 References for chapter 4

BSI, British Standards. (2000). Voltage characteristics of electricity supplies by public distribution systems. BS EN 50160:2000. ISBN 0 580 35925 5

BSI, British Standards. (2002). Electromagnetic compatibility (EMC) – Part 2-4: Environment – Compatibility levels in industrial plants for low-frequency conducted disturbances. BS EN 61000-2-4:2002. ISBN 0 580 40489 7

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