DEPARTMENT OF ELECTRONIC & ELECTRICAL ENGINEERING

University of Strathclyde Engineering

TRANSIENT FAULT LOCATION IN LOW VOLTAGE UNDERGROUND DISTRIBUTION NETWORKS

THESIS PRESENTED TO

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By

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DECLARATION OF AUTHENTICITY AND AUTHOR'S RIGHTS

This thesis is composed by the author and is the result of author's original research. Where appropriate, the acknowledgements have been made to the work of others.

Signed:

Date:

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Abstract

This thesis presents a novel approach to automatic transient fault location in Low Voltage Underground Distribution Networks (LVUDN). A transient fault is the first stage of development of a fault condition which is indicative of a threat to power network security, but is not significant enough to trip the protection system. The proposed approach is based on time domain reflectometry (TDR), enhanced by pulse compression, wavelet transform and adaptive filters.

The thesis provides a review of the properties of faults in LVUDN and of the characteristics of typical underground cables used in LVUDN. Advantages and restrictions of existing fault location techniques were discussed. Advanced signal processing tools such as pulse compression, adaptive filter and wavelet transform were also investigated.

A pulse compression enhanced TDR acquisition methodology was developed and a self-comparing scheme was proposed to detect the timely change of the enhanced TDR waveform, thereby providing the corresponding required deviation-threshold to trigger the system and finally to calculate the fault distance. The pulse-compression technique provides better resolution and detection range, and side lobes are suppressed by applying wavelet transform. The deviation trigger is further enhanced by adaptive filtering for better noise rejection.

A fully-customised, prototype fault locator and software were developed to implement the pulse compression, wavelet transform and adaptive based automatic transient fault location system. The prototype fault locator was tested in a live LVUDN and the results were evaluated.

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Acronyms

ADC	Analog To Digital Convertor
Avalon MM	Avalon Memory Mapped
Avalon ST	Avalon Streaming Interface
CATV	Community Antenna Television
CMOS	Complementary Metal Oxide Semiconductor
CNE	Combined Neutral Earth
CPU	Central Processor Unit
DAC	Digital To Analog Convertor
DC FIFO	Duel-Clock First In First Out
DDR	Double Date Rate
DDS	Direct Digital Synthesis
DMA	Direct Memory Access
DSP	Digital Signal Processing
DTMF	Dual-Tone Multi-Frequency
DUT	Device Under Test
DWT	Discrete Wavelet Transform
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
EPR	Ethylene-Propylene Rubber
FFT	Fast Fourier Transform
FIFO	First In First Out
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
FT	Fourier Transform
FWT	Fast Wavelet Transform
GPIO	General Purpose Input/Output
GSPS	Giga-Samples Per Second
IIR	Infinite Impulse Response
IO	Input And Output
IP	Intelligence Property
JTAG	Joint Test Action Group
LFM	Linear Frequency Modulation
LMS	Least Mean Square
LSB	Least Significant Bit
LV	Low Voltage
LVDS	Low-Voltage Differential Signalling
LVUDN	Low Voltage Underground Distribution Network
MDPE	Medium Density Polyethylene
MIMO	Multiple-Input And Multiple-Output
MIPS	Million Instructions Per Second
MMSE	Minimum Mean Squared Error
MSB	Most Significant Bit

MSPS	Million Samples Per Second
NLMS	Normalised Least Mean Square
OHT	Overhead Transmission
OPAMP	Operational Amplifier
PCB	Printed Circuit Board
PE	Polyethylene
PGA	Programmable Gain Amplifier
PICAS	Paper Insulated Corrugated Aluminium Sheath
PILC	Paper Insulated Lead Covered
PLL	Phase-Locked Loop
PTFE	Poly Tetra Fluoro Ethylene
PVC	Polyvinyl Chloride
QAM	Quadrature Amplitude Modulation
RAM	Random Access Memory
RF	Radio Frequency
RLS	Recursive Least Squares
SDRAM	Synchronous Dynamic Random Access Memory
SGDMA	Scatter Gather Direct Memory Access
SNR	Signal To Noise Ratio
SSRAM	Synchronous Static Random Access Memory
STFT	Short-Time Fourier Transform
TDL	Tapped Delayed Line
TDR	Time Domain Reflectometry
TEM	Transverse Electromagnetic
USB	Universal Serial Bus
VF	Velocity Factor
VGA	Variable-Gain Amplifier
VOP	Velocity Of Propagation
VSWR	Voltage Standing Wave Ratio
XLPE	Cross-Linked Polyethylene

1 Introduction

1.1 Background

Underground cables are widely used in the UK for electricity distribution. Compared to overhead transmission lines, the underground cable system offers a large range of advantages including high level of personnel and public safety, low electromagnetic interference, weather proofing and minimal visual impact. Many of the underground cables installed are approaching the end of their design-life. Due to limitations on human and financial resources, the Distribution Network Operators (DNOs) will normally keep these aged cables in service to extend their service lifetime. However, the aged cables are prone to develop faults, which results in loss of power supply. This leads to customer minutes lost - a parameter that is monitored by the Electricity Regulator (ER). Hence, it becomes desirable to know where in the power network a fault might be developing.

The early stage of a cable fault is characterised by the occurrence of a transient fault. Transient faults show mild fault symptoms, such as an irregular voltage dip or spikes in one or several power cycles, but the impact is too small to cause fuse operation or power failure. Transient faults will generally last for some time before developing into severe fault stages, which ultimately lead to service disruption or power blackout. It is therefore necessary to develop an online monitoring system to detect and locate transient faults, especially in extended lifetime underground power cable networks.

Conventional cable condition testing and fault pre-location techniques such as time domain reflectometry (TDR) require de-energized measurement and disconnection of

peripheral connections; due to the high amount of noise introduced by modern switching-mode power supplies (SMPS) and cable joints. Furthermore, conventional pre-locating techniques are only employed when obvious symptoms are observed, for example when a regular fuse has tripped, causing service disruption.

1.2 The Objectives of the study

The objectives of this study are inspired by the incentive of achieving online transient fault detection and location for low voltage underground cables, and continuous development of modern smart grids. They can be described from several aspects:

- To study and investigate the nature of transient faults and their behaviour in underground cables. Characterize underground power cables by their high-frequency response, which is used by many popular fault-locating techniques.
- To review and analyse current techniques and experience in the cable fault pre-locating industry, including the most popular technique: time domain reflectometry (TDR).
- To identify the feasibility of the use of TDR in online transient fault monitoring and location. Address the restrictions and limitations of the current TDR technique, and explore the potential workarounds by application of novel signal processing tools.
- To develop a complete method for online transient fault monitoring and location. Verify the method with hardware prototype in real underground power cable.

1.3 Summary of Original Contributions

This study is a contribution to the area of cable fault location in low voltage underground distribution networks. The main original contributions are summarized as follows:

- The high-frequency characteristics of underground cables are investigated, including the impedance and attenuation analysis using a network analyser and pulse TDR equipment. There are only very limited number of articles about these properties and most of them are based on theoretical simulation but no test results. This study offers a better understanding of the power cable behaviour at a wide range of frequencies, and the results help to improve the travelling wave based fault locating technique.
- Transient fault activity in underground power cables is studied and the mechanisms are provided. The feasibility of using the existing travelling wave based technique for online monitoring and fault location is also investigated, and the necessary improvements for successful application are presented. The results together with the above study formed the basis for development of a novel transient fault locating technique.
- A novel pulse compression enhanced TDR transient fault monitoring and locating method is described. This method is verified based on a prototype built during the research and further improved noise rejection capability by employing the adaptive filtering wavelet transform technique.
- A hardware prototype TFM1000 transient fault monitoring and locating system is developed to implement the proposed technique. The system utilises the latest System-On-Programmable-Chip (SoPC) technique to benefit from a

fully configurable digital signal processor with a fast real-time hardware processing system. The schematic design, component considerations, printed circuit board (PCB) layout, assembly, firmware design, and software design are displayed in detail. The system has been successfully tested in a real 240 V live underground power cable network with transient fault, and the results are discussed.

1.4 Presentation of Thesis

The subsequent chapters are presented as follows:

Chapter 2 reviews the current cable fault locating techniques and their underpinning fundamentals and theories. The underground cable structure and fault classification are also presented. Information on novel signal processing tools such as adaptive filtering, wavelet analysis and the pulse compression technique are also provided.

Chapter 3 presents the nature and generic detection methods of transient faults. Some common underground cables were characterized at the frequency up to 50 Mhz, which underpins the technique proposed in this thesis.

Chapter 4 displays the development of a novel pulse compression based and self-comparing technique for monitoring and addressing transient faults in underground power cable networks. Live energized measurements in real underground power cable networks are also presented.

Chapter 5 details the design of an experimental prototype of an online transient fault monitoring and location system. The hardware, firmware and software design are presented.

The transient fault monitoring and location technique is further enhanced in Chapter 6 by the introduction of post signal processing techniques based on advanced signal processing tools including adaptive filtering and wavelet based analysis. Test results based on a real power cable network are shown and compared. An alternative method is also presented and discussed.

Finally, conclusions are drawn and recommendations for future work are discussed in Chapter 7, including how the technique and system discussed in this thesis should be deployed, and directions for further development towards a more robust and reliable system.

2 Background and Literature Review

2.1 Introduction

The review in this chapter serves two purposes: it offers a background to all aspects of the design of innovative transient fault location systems, and it also contains a review of issues that will be addressed in this study.

This starts with transmission line theory in section 2.2, which forms the very basis and underpinning foundation of the technique proposed in this study. As the study is based on underground cables, a review of the mechanical structure and electrical characteristics of underground power cables follows in section 2.3. In Section 2.4, cable faults in LVUDN are classified into four types and discussed. Section 2.5 reviews current techniques for fault location in LVUDN and other power cables; applications, advantages and limitations are also discussed. Finally, in section 2.6, advanced signal processing tools such as adaptive filters, wavelet transforms and the pulse compression technique are presented and discussed in detail.

2.2 Transmission Line Theory

Prior to explanation of the cable characteristics and the following fault locating techniques, an understanding of the properties of transmission lines is necessary.

2.2.1 Transmission line model and Primary Coefficients

The design of underground cables varies to satisfy different requirements. Basically, an underground cable is comprised of a conductor and a dielectric [1]. The conductor

offers a path for electrical energy (current), while the dielectric provides electrical insulation by preventing direct contact between conductors, and between either of the conductors and other conducting objects. Therefore, underground cables that consist of at least two parallel conductors can also be classified as transverse electromagnetic (TEM) transmission lines [2]. A TEM transmission line can be modelled with a well-known lumped-element model, which contains four basic elements. A schematic of the cable model is shown in Figure 2-1:

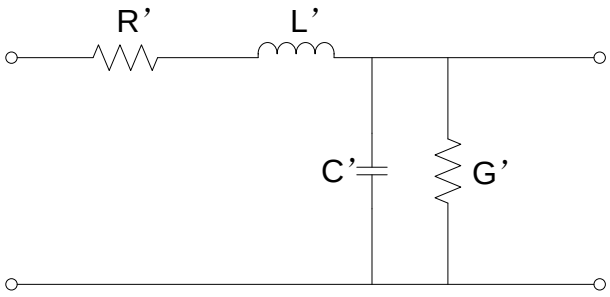


Figure 2-1: RLGC Transmission line lumped model

Where:

R’ is the series resistance per unit length that exists because of the resistance of the conductor, in Ω/m

L’ is the series inductance per unit length that exists because whenever current flows in a conductor, a magnetic field is produced around the conductor, in H/m

G’ is the shunt conductance per unit length and is due to the leakage current between the conductors, in S/m

C’ is the capacitance per unit length that exists between the conductors of a transmission line because there is a voltage between the conductors, thus creating an electrostatic field that can be represented by the parallel plates of a capacitor, in F/m

The quantities *R*, *L*, *C* and *G* per unit length are well known as the primary coefficients or the primary line constants of a transmission line.

2.2.2 Secondary Coefficients

The behaviour of a transmission line could also be described in terms of the current and voltage waves which propagate along it. This offers a better way to represent the performance of a transmission line and known as secondary coefficients. These coefficients are:

Characteristic impedance Z_0

Attenuation coefficient α

Phase change coefficient β

Phase velocity of propagation v_p

2.2.3 Characteristic Impedance

The impedance at any point looking down the infinitely long line is equal to the characteristic impedance Z_0 [2].

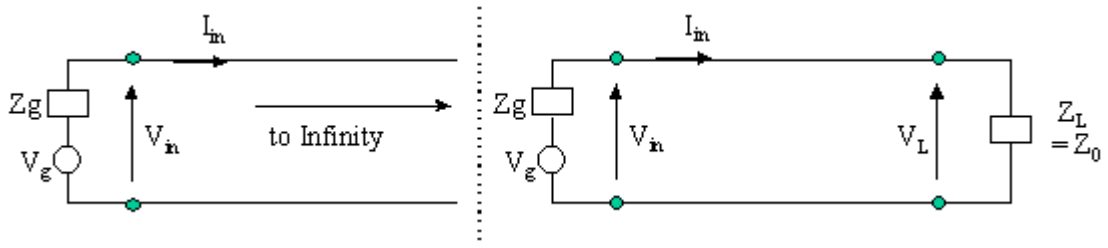


Figure 2-2: Characteristic impedance

The characteristic impedance can be calculated from the impedance of each of these RLGC 'T' elements [2]:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.1}$$

A transmission line that is terminated with its characteristic impedance Z_0 is called a matched line [2], i.e. it is correctly terminated.

2.2.4 Propagation Coefficient

The relationship between the voltage V_o (or current I_o) at the output of a transmission line and the voltage V_i (or current I_i) at the input end is governed by the propagation coefficient of the line [2].

The propagation coefficient, per unit length, can be calculated by considering the output/input power ratio of each individual elemental symmetrical T section which composes the transmission line [2]:

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.1}$$

In general, γ is a complex quantity which has a real part and an imaginary part, therefore it can be written as

$$\gamma = \alpha + j\beta \tag{2.2}$$

The real part of γ is called the attenuation coefficient (α) and has units of nepers per unit length, (1 neper = 8.68 decibels). The amplitude of a current or voltage wave is exponentially attenuated as it propagates along a line, because of losses in the line. There are three main types of losses:

(a) Conductor losses (i.e. I^2R losses);

(b) Dielectric losses; and

(c) Radiation losses (radiation losses occur if the conductor separation is an appreciable fraction of the signal wavelength. This does not occur in coaxial

cables if the outer conductor is made of solid copper, but some loss occurs if a braided outer conductor is used. Radiation losses are negligible if the correct cable is used).

The imaginary part of γ is called the phase change coefficient (β) and has units of radians per unit length. A current or a voltage wave experiences a progressive phase lag relative to its phase at the sending end of the line when it travels along a line. The phase change coefficient β is the number of radians (or degrees) phase lag per metre. This does not affect the amplitude or power of the wave.

The equation (2.2) for γ can also be used to find the phase velocity of propagation of signals on the line.

2.2.5 Velocity of Propagation

A sinusoidal wave travelling along a transmission line travels with a velocity called the phase velocity $v_p = \lambda f$ [2]. Normally v_p is represented as a velocity factor (VF), where

$$VF = \frac{v_P}{c} \tag{2.2}$$

By examining equation (2.2), at high frequencies jωL will be much greater than R, and jωC will be much greater than G, so that R and G can be ignored [2]. This gives, at high frequencies:

$$\alpha \approx \frac{1}{2}\left(\frac{R}{Z_0} + GZ_0\right) \tag{2.3}$$

The imaginary part is:

$$\beta \approx \omega(LC)^{\frac{1}{2}}\left(1 - \frac{RG}{4\omega^2 LC}\right) \tag{2.4}$$

At very high frequencies this reduces to:

$$\beta \approx \omega(LC)^{\frac{1}{2}} \tag{2.5}$$

A number of conclusions can be drawn from these expressions:

- The attenuation coefficient, the rate at which a signal is attenuated as it travels along the line, depends very much on the values of R and G, as one would expect. The earlier description of a lossless line as one in which R and G are equal to, or close to, zero is justified.

- The value of the phase change coefficient does not have a purely linear dependence on the frequency of the signal. Note that $v_p = \omega / \beta$ so that the speed of a signal is:

$$v_p \approx \frac{(LC)^{-\frac{1}{2}}}{1 - \frac{RG}{4\omega^2 LC}} \tag{2.6}$$

  From (2.6) it is clear that the speed of the signal depends upon its frequency; a higher frequency signal propagates slower. If the input signal is a complex one, it can be broken down into a number of sine wave (Fourier) components. When the signal reaches the output end of the cable, the phase (time) relationship components will have changed, producing a distorted version of the input signal.

2.2.6 Terminated Transmission Lines

2.2.6.1 Matched Transmission Line

If a transmission line is terminated with its characteristic impedance, it is said to be matched [2], and the input impedance of the line will be equal to Z_0. If the line is not loss free (lossy line), the amplitude of the signal transmitted from the source to the

load will be exponentially attenuated due to the non-zero attenuation constant α. Part of the energy of the input signal will be lost in the transmission line.

2.2.6.2 Mismatched Transmission Lines

When the transmission line is terminated by a load impedance Z_L which is different from the characteristic impedance Z_0 of the line, then this line is said to be mismatched [2]. In such a situation, the power which arrives at the far end of the line (i.e. the load) is not fully absorbed by the load. Part of the energy is reflected back towards the sending end of the line. When the reflected power arrives at the sending end, it is either fully absorbed by the source impedance if the sending end is matched (i.e. if generator impedance $Z_g = Z_0$) and no more reflection will occur, or it will be reflected back again towards the load if the source impedance is not equal to Z_0. In this case, the reflected power keeps reflecting at each end of the line until fully attenuated.

The transmission line allows the transmission of energy in the form of incident waves moving from the source to the load. If the load impedance equals the characteristic impedance, Z_0, of the line, the full signal power is absorbed by the load. If the load impedance is not equal to Z_0, then the signal is partially or fully reflected, in the form of a reflected wave moving back towards the source. These incident and/or reflected waves are called travelling waves.

When a reflected voltage wave occurs in the line it is added to the incident voltage wave (a phasor sum at each point along the line). A new resultant type of voltage wave is thus created, which varies in amplitude along the line. This resultant wave is called a standing wave. This standing wave has minima and maxima that are fixed in position in relation to the load. The shape of the standing wave has a pattern that repeats every $\lambda/2$ distance away from the load.

2.2.7 The Reflection Coefficient

When the line is not matched, reflection occurs at the mismatch. Thus, depending upon the load impedance, part or the entire incident wave is reflected at the load. The reflected voltage is given by $V_R = \rho_V V_I$ or $\rho_V = V_R / V_I$ where ρ_V is called the voltage reflection coefficient, i.e. it is the fraction of the incoming voltage which is reflected.

The current reflection coefficient is $\rho_I = I_R / I_I \ (= -\rho_V)$

Also, $\rho_I = -\rho_V$ by substituting for V_R and V_I in the equation for ρ_I, (noted that $I_R = -V_R / Z_0$).

$$Z_x = Z_0 \frac{1+\rho_v e^{-2\gamma x}}{1-\rho_v e^{-2\gamma x}} \tag{2.7}$$

Since Z_x is the impedance of any point along the line, at a distance x from the load, setting x = 0 yields $Z_x = Z_L$.

This gives:

$$Z_L = Z_0 \frac{1+\rho_v}{1-\rho_v} \tag{2.8}$$

From this we obtain the expression for the voltage reflection coefficient in terms of Z_L and Z_0:

$$\rho_v = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.9}$$

and since $\rho_V = -\rho_I$, the current reflection coefficient is:

$$\rho_i = \frac{Z_0 - Z_L}{Z_L + Z_0} \tag{2.10}$$

By applying (2.9) and (2.10) to the case of a short-circuited transmission line, where $Z_L = 0$, it is obvious that $\rho_V = -1$ and $\rho_I = +1$. That is, at short-circuit, the reflected voltage is equal in magnitude to the voltage arriving at short-circuit and is 180 degrees out of phase with it.

Similarly, at short-circuit, $I_R = I_I$.

Thus, this theoretical analysis confirms that the voltage and current distribution along a short-circuited transmission line are as discussed previously.

The above reasoning can also be applied to the open-circuited transmission line where $Z_L = \infty$. In this case, $\rho_V = +1$ and $\rho_I = -1$.

2.3 Underground Cable Characteristics

It is necessary to describe the mechanical structure and electric characteristics of underground cables, as this will facilitate understanding of both the nature of faults, and the basis of fault location techniques.

Underground cables are specified, designed, manufactured and tested in order to satisfy different requirements and applications. There are a large number of different cables on the market. Major considerations on choice of cable are listed in Table 2-1.For financial reasons, design engineers would normally choose the cable specified to meet their minimum system requirement.

Table 2-1: Considerations on the choice of cable

Electrical	Mechanical
Voltage	Climate and environment
Current	Stress along the cable
Impedance (Frequency)	

Cable characteristics are decided by the choice of the material and structure. The characteristics are fixed once the cable has been manufactured and assembled via the

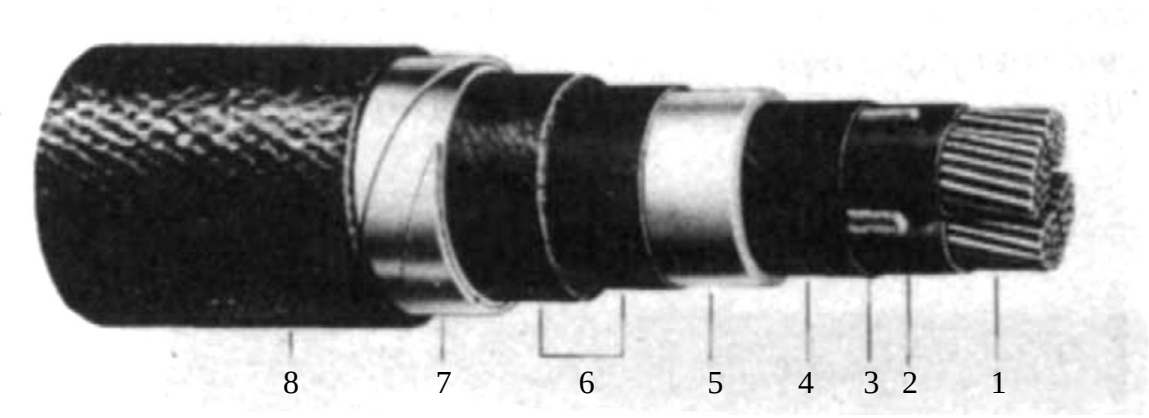
production line. However, if the structure or design properties of a given cable were to change during the production process, then this cable would no longer maintain its original design characteristics, and may fail to meet certain requirements.

The characteristics of a cable can be divided into two categories: mechanical characteristics (structure/material of cable), and electrical characteristics. This section will introduce the typical structure/material of underground cables, as well as discuss the electrical characteristics.

2.3.1 Structure of underground cables

Basically a power cable is comprised by a conductor and a dielectric [1]. The conductor offers a path for electric energy (current), while the dielectric providing electrical insulation by preventing the conductors from direct contact of other objects. Typically, an underground cable might also incorporate a protective material to provide mechanical reinforcement.

The conductor of the cable can be either solid or stranded. The most widely used cable conductor materials are copper and aluminium. A stranded conductor comprises a number of wires assembled in helical layers around a central wire or group of wires; this provides flexibility for storage, installation and handling [3]. Generally, solid conductors provide better soldering and jointing properties, and are mechanically and electrically more reliable due to the larger cross-sectional area. Flexibility is the major issue in many cases however, and thus the used of solid conductors is limited. Figure 2-3 is an example of a four-core lead sheathed cable. Figure 2-4 shows a solid aluminium three-phase LV trunk cable.



1. Shaped stranded conductor	5. Sheath, lead or lead alloy
2. Impregnated paper insulation	6. Bedding
3. Filler	7. Steel tape armour
4. Impregnated paper belt	8. Serving

Figure 2-3: Four-core lead sheathed cable, steel tape armoured. Specified for 600/1000V systems

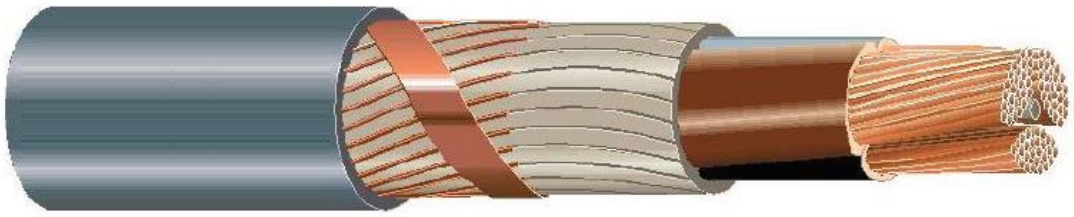


Figure 2-4: Three-core PVC insulated waveform trunk cable. Specified for 600/1000V systems

Another component of underground cables is the dielectric used for insulation. Paper insulation was used from 1890 [4]. Paper is an inexpensive material and a good electrical dielectric, but only when dried. Thus, changes have been made to use impregnants, such as mineral oil or compounds, to avoid moisture absorption by the paper.. As the research and development of cables continued, synthetic polymers have since replaced paper for insulation [5].

The choice of insulation is important, as most problems in cables are due to insulation failure. Materials for electrical power cable insulation can be classified as thermoplastics or thermosets [1]. Thermoplastics melt with heat, while thermosets have better heat tolerance. Presently, polyethylene (PE) is a common insulation material, made from thermoplastic and two other thermosets. Two constitutional formulas are possible for PE, one is cross-linked polyethylene (XLPE), and the other is ethylene-propylene rubber (EPR) [6]. The PE is more economic, and the chemicals used to make it are more resistant to moisture. Normally, PE can withstand up to 70 ℃, and thus it was confined to low voltage cables. For higher temperature and overload tolerance, XLPE and EPR can be selected as they can cope with 90 ℃ overloads. A different type of thermoplastic that can be used is polyvinyl chloride (PVC), which is mechanically strong, and resistant to flame, abrasion and moisture [1].

Armouring and sheathing are also seen in underground cables. Armouring is used to protect the cable from penetration by gnawing from animals, sharp objects or crushing forces. Power cables are usually armoured to carry earth fault currents, and to give some protection against mechanical damage, both during installation and service. Two types of armour utilized in the UK are galvanized steel wire and aluminium strips [4].

Sheathing is a tubular metallic covering over the insulation, which is used as a moisture barrier. Lead and aluminium are common sheathings. Lead is one of the oldest sheathing materials used on power cables [1]. However, the disadvantages of lead are that it is heavy, and it is prone to fatigue failure from vibration. Aluminium is also used for sheathing because it is lighter than lead, and also has good mechanical properties for this purpose.

2.3.2 Electrical Characteristic Measurement of Underground Cables

There are many electrical parameters for electronic cables, but not all of these parameters are well considered in all applications. For example, a domestic electrical engineer will satisfy the requirement of voltage (V) and current (I) rating when choosing the distribution cable from switching room to house, without considering the reflection coefficient. However, in the case of a cable fault (or in troubleshooting), there may be some high frequency signals transmitted along the cable. To understand the characteristics of high frequency signals travelling along power cables, it is necessary to have the cable impedance (Z_0) and reflection coefficient (Γ) data to hand (which can be derived from the primary coefficients $R'L'G'C'$).

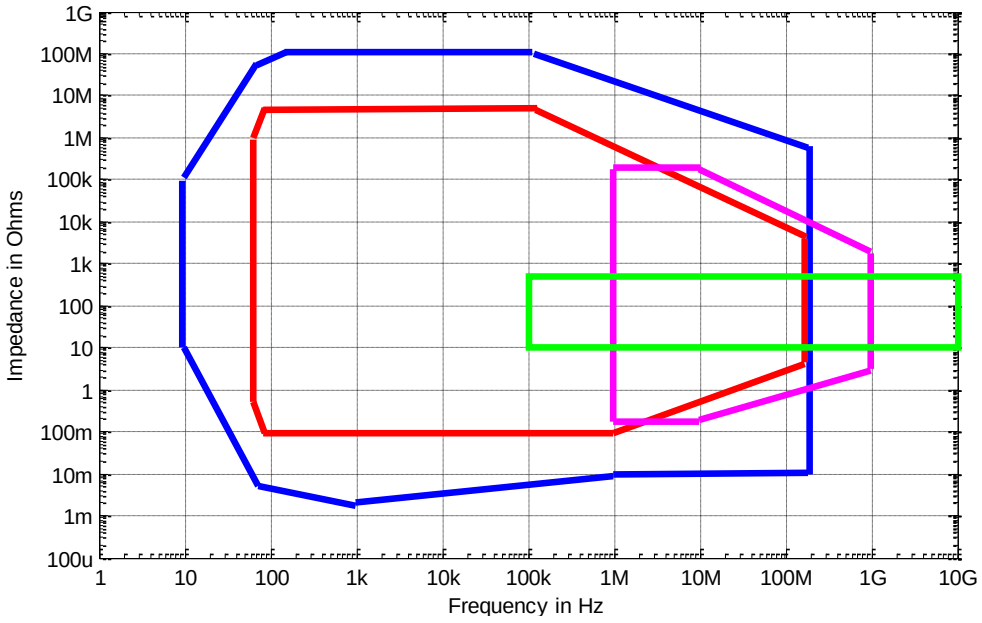
2.3.2.1 Impedance measurement

Modern impedance measurement instruments can measure the complex impedance vector and produce an output detailing the real and imaginary parts simultaneously. Such equipment normally comes with a wide frequency coverage from 10 Hz to 10 GHz [7]. In many cases, the impedance is a primary parameter when investigating and characterizing electronics components, materials and communication cables [8].

There are many approaches available to measure complex impedance. Practical methods include: network analysis, current-voltage (I-V), radio frequency current-voltage (RF I-V), resonant and bridge [7]. The resonant method has good accuracy in inductance measurement; however it requires resonance reference tuning and is not cost effective. The bridge method achieves high precision, but it needs special balancing.

The auto-balancing bridge method, transmission/reflection (including Γ, S-parameter, π model) method, and I-V, RF I-V methods are compared and contrasted in [9]. The

method with the highest precision is the auto-balancing bridge, which also exhibits a broad impedance range from several $m\Omega$ to hundreds of $M\Omega$, covering the frequency range from a few Hz to 110 MHz. The transmission/reflection method has the widest frequency coverage from 5 Hz to 110 GHz, but it achieves good accuracy only near 50 Ω or 75 Ω. The I-V and RF I-V approach may be considered as a compromise between the auto-balancing bridge and the transmission/reflection method; it delivers good precision from several $m\Omega$ to several $M\Omega$, with frequency coverage from 40 Hz to 3 GHz. An analysis and comparison diagram is also provided in [9], as in the following figure.



Blue: Auto-balancing bridge method, Red: I-V method,

Magenta: RF I-V method, Green: Transmission/reflection method

Figure 2-5: Impedance measurement methods and coverage [9]

The impedance of a power cable is not normally specified in the datasheet, however, the author of this thesis used to work for a fault locating company, and based on this experience, the impedance of parallel conductor power cables generally lays between 25 Ω and 75 Ω, while for twisted power cables the impedance may be higher, up to

150 Ω. Hence, as a rule of thumb, the impedance of power cables is in the range between 25 Ω and 150 Ω, within the range of the industrial measurement methods mentioned above.

Considering the fact that the frequency for investigation in this thesis is within the range 50 Hz to 100 MHz, as well as the availability of equipment and instrumentation, a HP/Agilent 4395A spectrum analyser with impedance analysis option (4395A-010), 43961A I/V impedance test kit, and 87512A transmission/reflection test kit are used for analysis of the cable impedance.

The HP/Agilent 4395A spectrum analyser provides two possible techniques to measure the impedance. With the 43961A test kit connected, I/V impedance measurement can be performed. Transmission/reflection measurement is also possible via utilisation of the 87512A test kit. The theoretical and practical test results of both techniques are discussed and concluded in this section.

Theory of V/I impedance measurement (V/I Method)

The basis of the complex impedance method is to measure both the voltage across the device under test (DUT) and the current through the DUT, and thereby calculate the impedance using Ohm's law.

According to DC Ohm's law:

$$R = \frac{V}{I} \tag{2.11}$$

Note that *R*, *V* and *I* are all scalars.

By substituting with AC voltage and current component [10]:

$$\vec{Z} = \frac{\vec{V}}{\vec{I}} \tag{2.12}$$

Note that *Z*, *V* and *I* are all vectors.

A basic diagram of measurement may be drawn as in Figure 2-6.

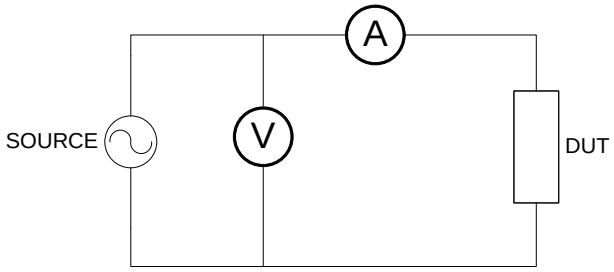


Figure 2-6: Basic impedance measurement Diagram

The basic method is not practical as the impedance of the current-measuring device will affect the result, and measuring voltage and current simultaneously is not preferred.

If the ammeter is replaced by a known value pure resistor, e.g. 50 Ω, the circuit becomes a basic I/V impedance measurement circuit:

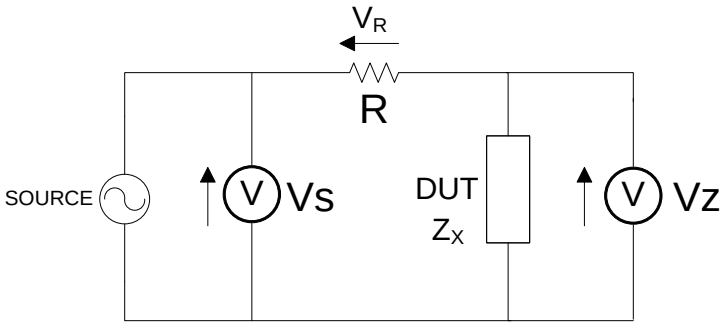


Figure 2-7: Basic I/V impedance measurement

Where:

Vs is the voltage applied to the measurement circuit

Vz is the voltage across the DUT

Because the complex impedance Z_X of the DUT can also be represented with a resistance R_X in series with a reactance jX_X, a vector diagram is shown in Figure 2-8 to represent the voltage relationship:

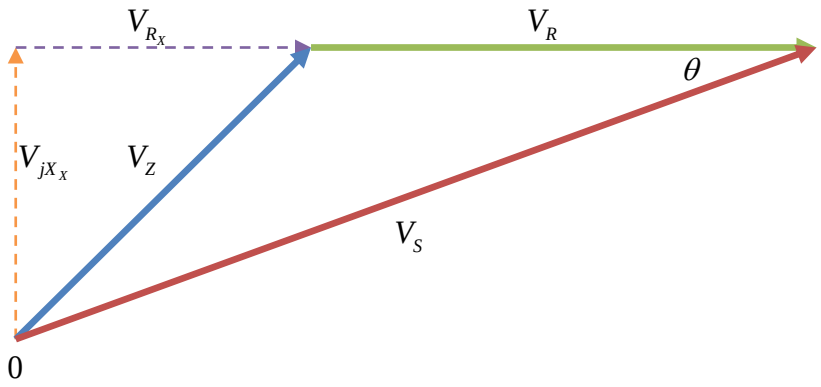


Figure 2-8: Vector diagram for impedance calculation

From the vector diagram and applying Kirchhoff's voltage law (KVL):

$$\vec{V}_S = \vec{V}_R + \vec{V}_Z \tag{2.13}$$

With Ohm's law:

$$\vec{V}_Z = \vec{I}_Z \times Z_X = \frac{\vec{V}_R}{R} \times Z_X \tag{2.14}$$

By substituting (2.13) into (2.14):

$$Z_X = \frac{\vec{V}_Z}{\vec{V}_S - \vec{V}_Z} \times R \tag{2.15}$$

By using such a method, only two synchronized voltage measurement paths, $\vec{V}_S$ and $\vec{V}_Z$, are required for calculating the impedance.

In some cases, the voltage of the reference resistor $\vec{V}_R$ is measured instead of the source voltage $\vec{V}_S$. In this case, a special differential amplifier or single-ended voltage calculation [11] is essential for measuring $\vec{V}_R$, and sometimes an RF transformer is applied to form a high-end sensor [12]. Due to the added complexity, measuring $\vec{V}_R$ is not preferred.

The theory of I/V impedance measurement has been discussed in this section, however it is necessary to remember the cable characteristic impedance is based on

the input impedance of an infinitely long cable. In practice, it is not always possible for a cable to be infinitely long. An alternative approach is calculation using the open/short method:

The input impedance of a short-circuited transmission line is [2]:

$$Z_{SC} = jZ_0 \tan(\beta l) \tag{2.16}$$

The input impedance of an open-circuit transmission line is:

$$Z_{OC} = -jZ_0 \cot(\beta l) \tag{2.17}$$

Multiplying (2.16) and (2.17), we have:

$$Z_0 = \sqrt{Z_{SC} Z_{OC}}$$

Or:

$$|Z_0| = \sqrt{|Z_{SC}| \bullet |Z_{OC}|} \ (\Omega) \tag{2.18}$$

and

$$\theta_{Z_0} = \frac{\theta_{Z_{SC}} + \theta_{Z_{OC}}}{2} \ \text{(Degrees)} \tag{2.19}$$

The attenuation constant α and phase constant β can also be derived from the short-circuit and open-circuit input impedances [7]:

$$\alpha = 8.6859 \times \frac{1}{2l} \ln \sqrt{\frac{(1+R)^2 + X^2}{(1-R)^2 + X^2}} \ \text{(dB/m)} \tag{2.20}$$

$$\beta = \frac{1}{2l}\left(\pi - \arctan\frac{R+1}{X} + \arctan\frac{R-1}{X} \right) \ \text{(rad/m)} \tag{2.21}$$

Where:

$$1 \text{ Np} = \frac{20}{\ln 10} = 8.6859 \text{ dB}$$

l is the length of the cable in meters (m)

$$R = \sqrt{\frac{Z_{SC}}{Z_{OC}}} \cos\left(\frac{\theta_{Z_{SC}} - \theta_{Z_{OC}}}{2}\right) (\Omega)$$

$$X = \sqrt{\frac{Z_{SC}}{Z_{OC}}} \sin\left(\frac{\theta_{Z_{SC}} - \theta_{Z_{OC}}}{2}\right) (\Omega)$$

Theory of transmission/reflection impedance measurement

Network analysers with appropriate transmission/reflection kit are able to measure the characteristics of DUT against frequency [13]. An HP/Agilent 4395A network analyser with the 87512A transmission/reflection test kit provides the capability to characterize 50 Ω or 75 Ω DUTs, with frequency coverage from DC to 2 GHz. This measurement setup outputs the scattering parameters (S- parameters) to characterize the DUT.

The scattering parameters (or S- parameters) describe linear electrical characteristics in the steady state [14]. Other parameters are also available to describe the electrical properties, e.g. Z, Y and ABCD parameters, however the S-parameters are considered easiest to measure, and more applicable in high frequency analysis [15]. For a lossy, unmatched TEM transmission line, the S-parameter can be calculated as [16]:

$$S = \frac{1}{D_S}\begin{bmatrix} (Z_C^2 - Z_0^2)\sinh\gamma l & 2Z_C Z_0 \\ 2Z_C Z_0 & (Z_C^2 - Z_0^2)\sinh\gamma l \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \qquad (2.22)$$

Where:

$D_S = 2Z_C Z_0 \cosh\gamma l + (Z_C^2 + Z_0^2)\sinh\gamma l$

l is the length of the transmission line,

γ is the propagation constant of the transmission line,

Z_C is the characteristic impedance of the transmission line,

Z_0 is the impedance of the measuring equipment

The propagation constant γ and characteristic impedance Z_C can be extracted from (2.22)[17, 18]:

$$\gamma = \frac{1}{l}\cosh^{-1}\left(\frac{1-S_{11}^2+S_{12}^2}{2S_{12}}\right) \tag{2.23}$$

$$Z_C = Z_0\sqrt{\frac{(1+S_{11})^2-S_{12}^2}{(1-S_{11})^2-S_{12}^2}} \tag{2.24}$$

It should also be noted that γ, Z_C and the S-parameters are frequency-dependent, and only valid for a given measuring frequency.

2.4 Cable Faults Classification

A fault in a power cable may occur due to insulation failure or imperfect connection of a conductor. These faults can progress with time and cause electrical failure. The progress of the fault may generally be divided into 4 stages [6]:

- Transient faults
- Intermittent faults
- Persistent faults
- Permanent faults

A transient fault is the early stage of a fault condition. Transient faults generally only last for a fraction of a power cycle, and cause neither immediate power failure, nor service disruption. Because the impact on the power network is so small, transient faults may not cause fuses to operate (Figure 2-9).

If the transient fault is missed/neglected for a prolonged period, excessive damage to the cable further deteriorates the structure, and eventually the transient arcing process draws enough current to trip the fuse. This fault can be defined as an intermittent fault, if the fuse does not operate immediately after replacement. It may take weeks or

months for the fuse to rupture due to an intermittent fault. An intermittent fault develops into a persistent fault if the damage to the cable causes the fuse to blow frequently, but the cable does not appear to be faulty in low voltage resistance measurements.

Transient, intermittent and persistent faults generally occur due to potential arcing activity in the cable structure [6]. The arcing process will create excessive heat and change the properties and structure of the cable, eventually resulting in permanent faults. The permanent fault could be a low resistive fault (short-circuit fault) or a high resistive fault (open-circuit fault). Low resistive faults could occur due to excessive carbon deposition along the fault path, or due to excessively high temperature causing the metal to weld together and become a metallic contact. A high resistive fault may be caused by excessive heat breaking the conductor connection.

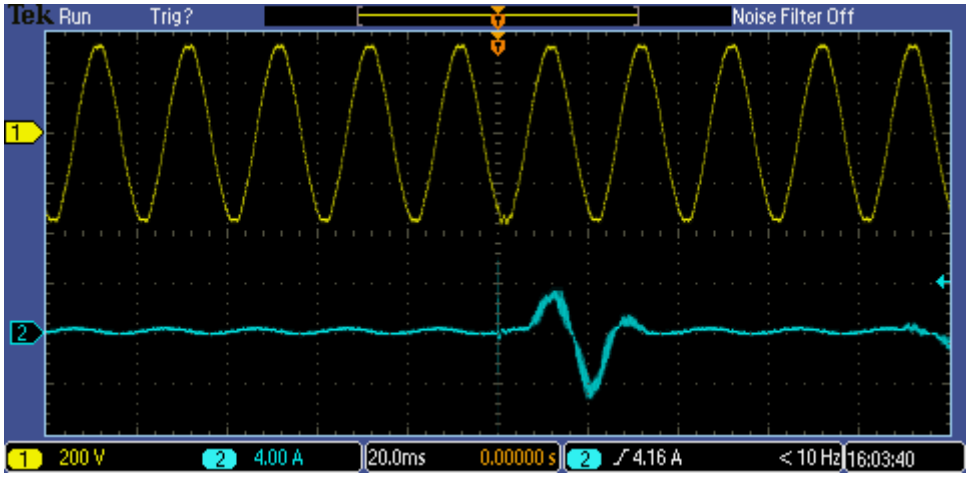


Figure 2-9: A power network with a transient fault activity captured at the duration of ~20us

2.5 Fault location technologies

Plenty of cable fault location technologies have been developed over the past few decades. These technologies or methods may be classified by the purpose of a generic fault locating procedure:

Basic-testing – to find the properties of a fault

- DC or very low frequency (VLF) test – determine the fault voltage and failure conductor/phase
- Sheath fault test – determine health of sheath insulation

Pre-Locating – to give approximate distance to fault

- Time domain reflectometry method – based on the signal travel time from pin point to fault point
    - Acoustic TDR
    - LV TDR method
    - Impulse reflection (with fault igniting device)
- Voltage drop method – based on voltage drop across cable impedance
    - Transient gradient method
    - Resistance bridge method

Fault pinpointing – to precisely locate the fault point

- Audio frequency
    - Twist field method
    - Minimum turbidity method
    - Acoustic field method
- Electromagnetic
    - Electromagnetic surge method

Fault conversion – transform the fault to final state (permanent fault)

- High power surge/DC burning

Signal routing

- Blocking inductor

2.5.1 Basic testing

The VLF or DC high potential withstand (HIPOT) testing are techniques to examine cable defects [19]. The basis of HIPOT testing is to apply a DC or VLF high voltage (normally in the range from 1.5 U_0 to 3 U_0), and check whether the cable could withstand the voltage; this will yield a pass-or-fail result. DC HIPOT testing is seldom used because it is proven to damage the cable, and now the VLF HIPOT method is very commonly applied because industry recognizes VLF HIPOT testing as non-destructive.

The DC or VLF HIPOT tests can only show the existence of a defect, and cannot locate the fault. A sheath fault test is a technique for detecting the leakage between conductor (metallic armour or cores) and earth, by applying high voltage and examining the resistance. Similarly, a sheath fault test does not provide information regarding the location of a fault.

2.5.2 Voltage drop method

It is known from Ohm's law that when a current flows through a resistor, it will result in a potential drop across the resistor, that is:

$$V = I \times R \tag{2.24}$$

The fact that the conductor in a cable normally has a constant cross-sectional area means that the resistance of the conductor can be calculated by:

$$R = \rho \frac{l}{A} \tag{2.24}$$

Where:

ρ is the specific electrical resistance of the conductor material

l is the length of the conductor

A is the cross-sectional area of the conductor

By combining (2.24) and (2.24), the voltage across a conductor is:

$$V = I \times \rho \frac{l}{A} \tag{2.24}$$

Or:

$$V \propto l$$

In other words, the voltage difference across a cable is proportional to the length of the cable, for a given current.

This property is used in the transient gradient method and the resistance bridge method to locate cable faults.

2.5.2.1 Transient Gradient Method

The transient gradient method is a common technology for cable fault location over the past decades [6]. The theory of this method is to measure the voltage drop before and after the fault. A simplified diagram is shown in Figure 2-10. A part of the cable network has 5 access points (e.g. busbar in substation, feeder pillars or a cable joint) from A to E, this part is used for reference and there is a fault between C and D, as shown in Figure 2-10a. The equivalent circuit diagram is shown in Figure 2-10b. As the major current is flowing through Z_{AB}, Z_{BC}, Z_{CF} and Z_{Fault}, the measured voltage should be decreasing when approaching the fault. This voltage drop stops after the fault point as the following circuit does not draw any current, hence voltage remains

constant. The voltage plot of each access point is shown in Figure 2-11. The point of intersection of the “gradient before fault” line and the “gradient after fault” line represents the theoretical distance to the fault. The slope of the “gradient before fault” line depends on the current to the fault. Higher current will result in a higher voltage drop, and thereby a steeper slope.

The transient gradient method can also be applied to locate transient faults. Multiple voltage readings must be taken simultaneously around the fault area. These voltage readings are valid only when the transient fault is igniting.

The success of the transient gradient method relies on the type of fault, the location of the voltage reading point, and the complexity of current flow. A high resistance (open) fault will result in a consistent gradient before and after the fault, and therefore the fault point cannot be seen. Voltage reading points are limited with this method, especially for LVUDN, and they may not be spread in ideal distance. The current flow must be simply directed from the source to the load. A complex current flow (e.g. return current) in the diagnostic path will cause the voltage reading plot to carry unnecessary information and lead to an incorrect result. The voltage must be read between the conductors where the fault exists; for example, the voltage reading must be in phase R and phase Y, if the fault is between phase R and Y.

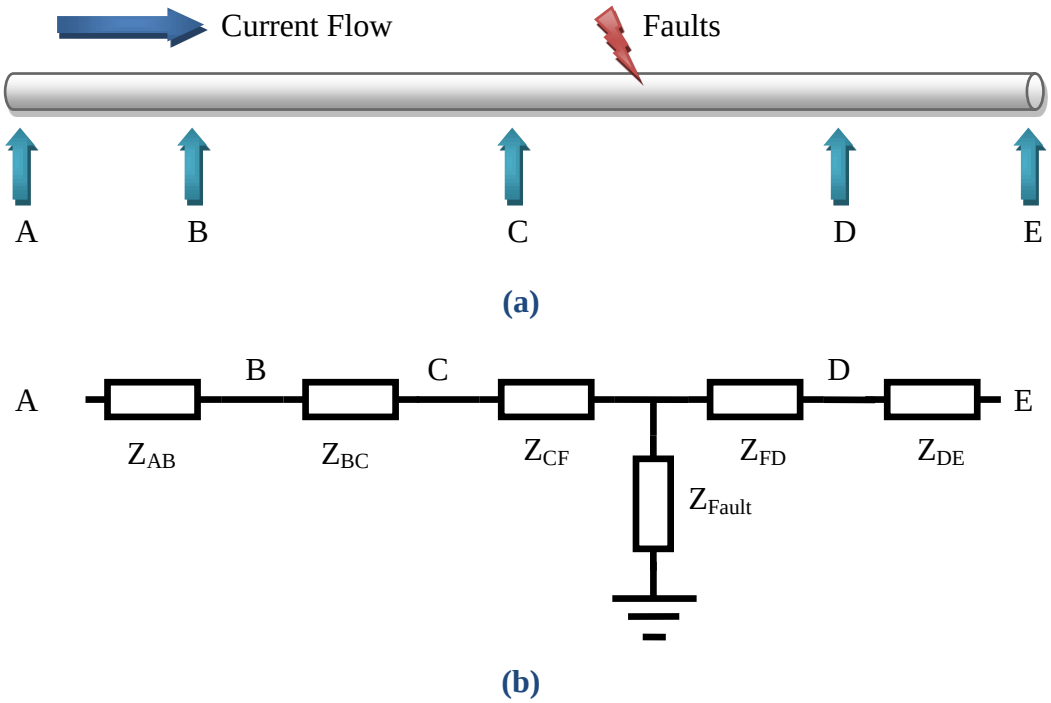


Figure 2-10: Equivalent diagram of gradient method

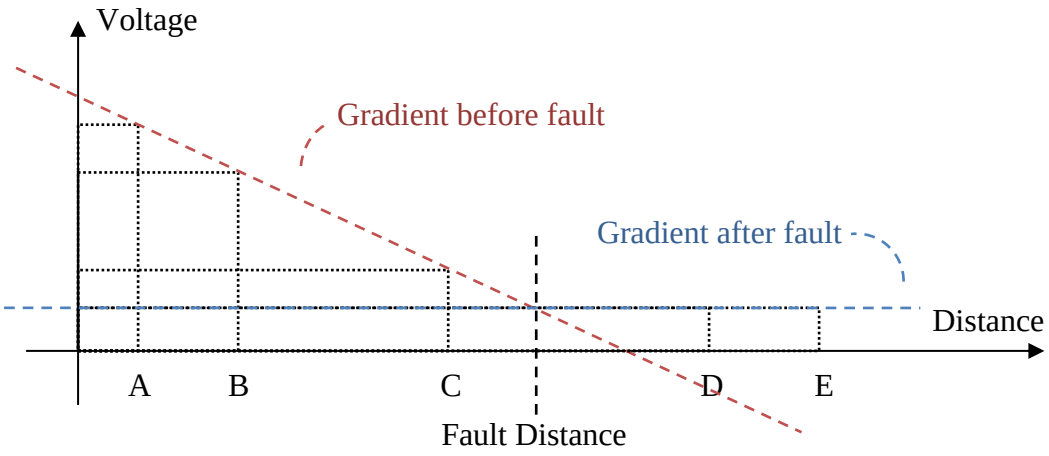


Figure 2-11: Fault distance calculation of gradient method

2.5.2.2 Resistance Bridge Method

The resistance bridge method is a technique that is commonly used to locate medium or high resistance faults. As many high resistance faults induce neither significant impedance change nor observable reflection, travelling wave methods are not applicable, since they require reflection from the fault.

The resistance bridge method uses the fact that the resistance of the cable conductor is proportional to the length of the conductor. The location of the fault can be calculated by precisely measuring two resistances of the conductor to the fault. Many bridge configurations are available to locate faults, in which three popular configurations are: Murray loop, Inverted loop and Hilborn loop [6, 20].

2.5.2.2.1 Murray Loop Bridge Method

The Murray loop bridge was a commonly-used technique to locate cable faults in the past century, and is still being used today [20, 21]. This method can only be employed, when:

- Only a single fault exists
- Good return is available (e.g. one conductor is intact)
- The fault resistance is lower than the cable insulation resistance
- The fault is a shunt fault and the cable conductors are not open
- The conductors are of the same type (have uniform R')

A simplified schematic is shown in Figure 2-12.

By alternating the value of the arm resistors Ra and Rb, the bridge will be brought to balance. Note that the resistance of the good conductor Rg is proportional to the cable length L:

$$\frac{Rx}{Rg+Ry}=\frac{Ra}{Rb} \tag{2.24}$$

Therefore:

$$L_{fault} = 2 \times L \times \frac{Ra}{Rb} \tag{2.24}$$

The accuracy of the Murray loop method could reach 0.1%, when no other interference exists. The sensitivity of this method depends on the sensitivity of the galvanometer and the current drawn by the fault [6]. The accuracy may be increased by using higher bridge source voltage, such that the galvanometer can better indicate the balancing of the bridge.

A similar technique, the Varley loop, is also available. The Varley loop method uses fixed value of Ra and Rb and introduces a variable resistor in the faulted leg. This method is more accurate for high resistance faults [22].

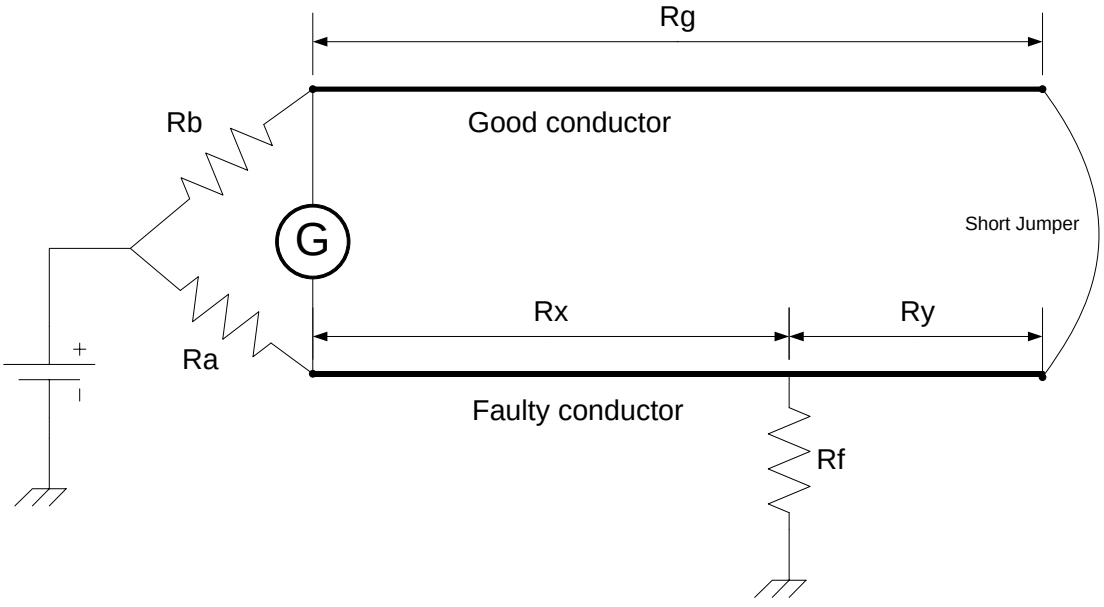


Figure 2-12: Simplified schematic of Murray Loop Bridge Method

2.5.2.2.2 Inverted Loop Method

If the galvanometer and source are swapped, this set-up is known as the Inverted Loop method, as shown in Figure 2-13. Instead of driving through arm resistors, the

source of the inverted loop method drives the conductors directly. As the resistance of the conductor is usually very low, a high-current, low-voltage power source must be employed in this method. For example, a 5 V source connected across a 95 sq.mm conductor XLPE cable may produce 50 A current. To avoid unnecessary voltage drops, a high-current short jumper and heavy-duty diagnostic leads capable of carrying such high current should be used; otherwise the potential drop in these wires will alter the result.

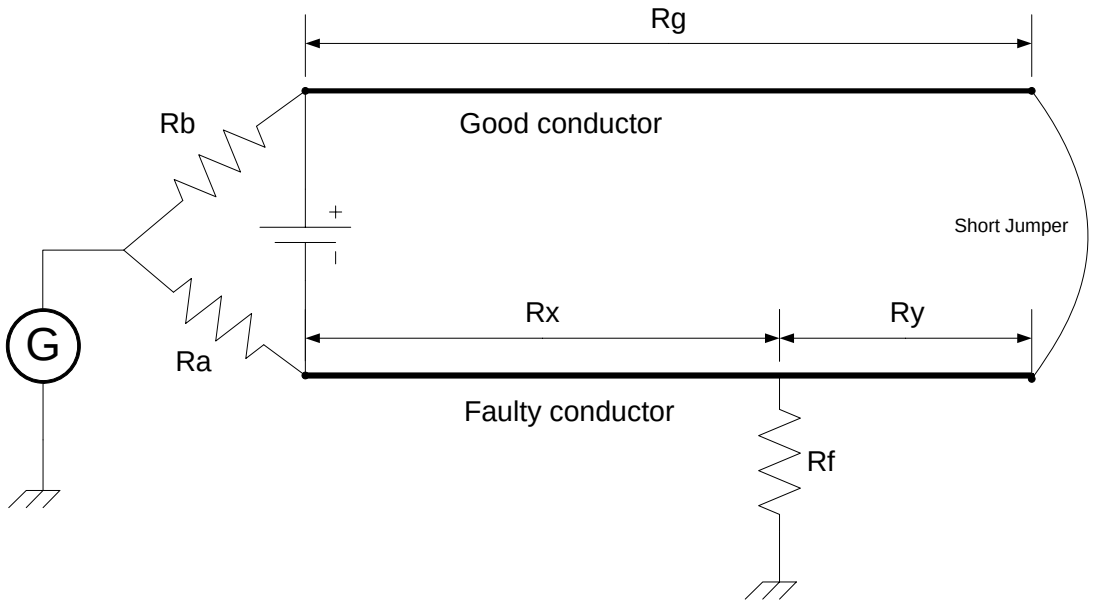


Figure 2-13: Simplified schematic of Inverted Loop Method

There are some precautions that need to be considered when employing the inverted loop method [6]:

- This method is effective for locating high resistance faults, but the fault resistance cannot be higher than the insulation resistance
- The shunt capacitance in a long cable will result in a long rise time
- The test time should not be too long as the cable is carrying very high current

2.5.2.2.3 Hilborn Loop Method

If a good return path (good conductor) is not available, the Hilborn loop method can be applied, providing that a pair of identical conductors is useable to reach the remote end. As shown in Figure 2-14, the Hilborn loop method requires two auxiliary conductors with resistance r, to make the bridge directly to the faulty cable.

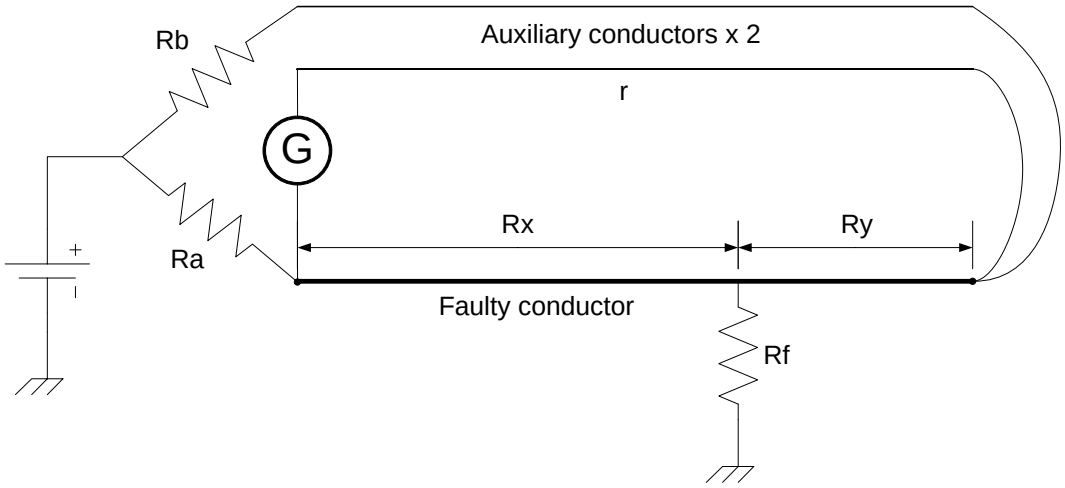


Figure 2-14: Simplified schematic of Hilborn Loop Method

The fault distance is given when the bridge is at balance [6]:

$$L_{fault} = \frac{Ra}{Ra + Rb + r} \times L \tag{2.24}$$

The main advantages of the Hilborn loop method are:

Because *r* is usually small compared to Ra and Rb, the resistance of the auxiliary conductor *r* is not important.

The bridge is directly connected to the faulty conductor and thereby provides an accurate result.

This method can also be employed when two cores of the cable are available, and known to be intact.

2.5.3 Fault Pinpointing

2.5.3.1 Audio Frequency Methods

Audio frequency methods are powerful tools to pinpoint most underground cable faults, and are still in used today [6]. By applying a high energy audio frequency signal to the cable, signals emitted from the cable can be picked up and recognized. This emitted signal changes according to the cable properties and the fault. By monitoring this change along the cable, the fault can be located. The most common audio frequency methods are:

- Step voltage method for low resistive earth contacting faults.
- Twist method for low resistive fault in twisted cables

Nearly all audio frequency fault locators offer the option to choose appropriate output frequencies. An important factor that affects the choice of frequency is the induction effect. Higher frequency results in higher inductive coupling effect (crosstalk). Lower frequencies provide a good diagnostic effect while minimising the coupling effect, which is suitable for direct signal coupling (have access to conductors). Higher frequencies offers good signal coupling to the cable for audio frequency generator.

2.5.3.1.1 Step voltage method

The step voltage method works on the principle of ground resistance, as shown in Figure 2-15.

This method locates the fault by the following procedure:

- Disconnect the cable from any load, and ground other healthy cores/sheath.
- Apply an audio frequency pulse generator to one end of faulty connector.

- Insert two probe of detector into ground, watching the potentiometer together with headphones. The volume of headphone and potentiometer should increase when probing towards the fault.
- Keep walking along the cable, until the volume decreases and the potentiometer returns to zero, mark the point.
- If the volume is heard to be increasing and the potentiometer is moving to the negative side, then the point marked in the previous step is the fault point.

It should be noted that the route of the cable must be known prior to pinpointing the fault. Where a good contact to soil is not possible (e.g. cement surface), wrapping the probe with a wet towel and increasing the audio frequency generator voltage may be helpful to get a clear audio signal.

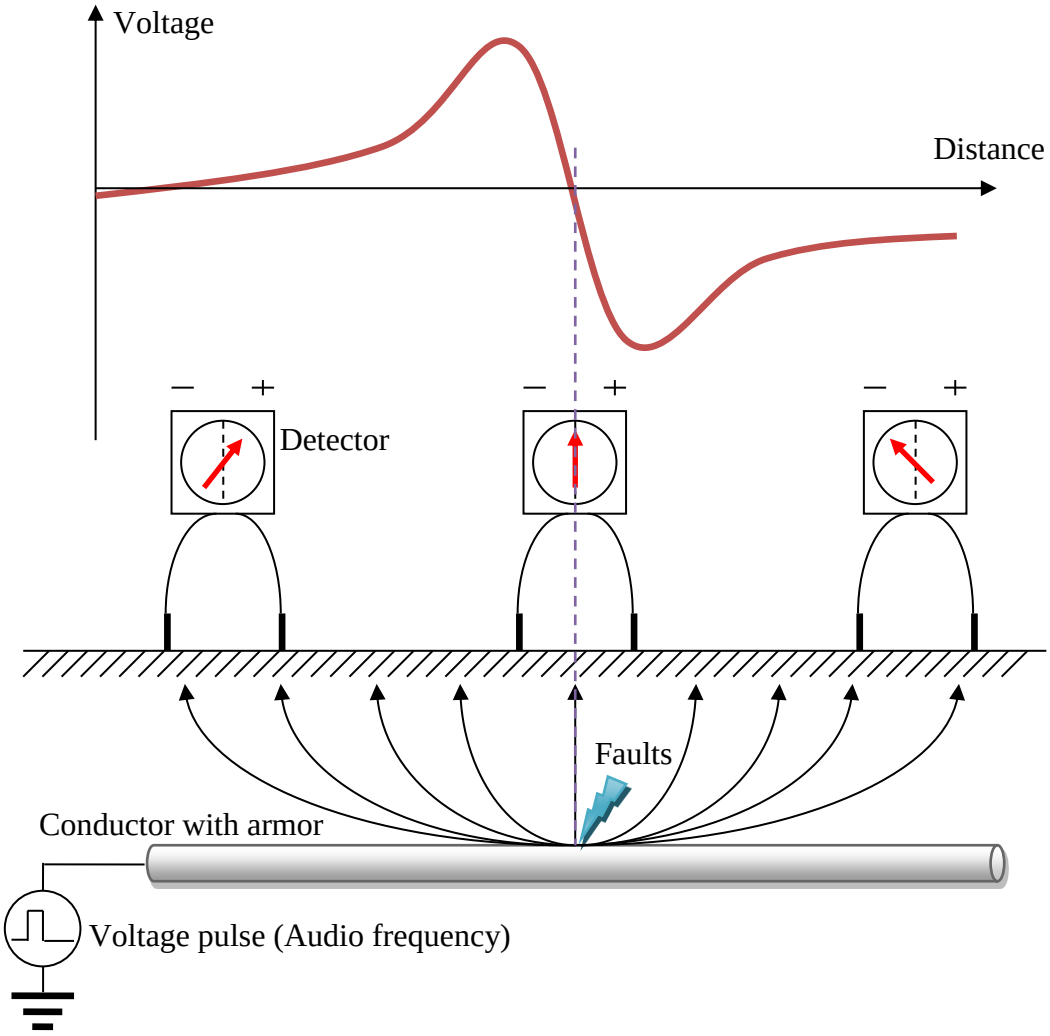


Figure 2-15: Illustration of Step Voltage method

2.5.3.1.2 Twist method

The twist method is the most well-known audio frequency technique in pinpointing low resistive faults. This method uses the fact that most cores of cable are longitudinally twisted. The audio frequency is normally set to a higher frequency band such that an over-ground receiver can clearly pick up the signal emitted from an underground cable. As shown in Figure 2-16, the audio frequency generator is connected to the pair of cores that contains the fault. The current will flow from one core to the fault and return by another core. The magnitude of current depends on the

fault resistance; the higher the fault resistance in the cable, the lower the current flow in the core pair. A high power audio frequency generator is required when the fault has high resistance. Current flow in the twisted conductor produces a changing magnetic field direction along the cable. Hence maxima and minima can be observed when moving the detector probe along the cable trace. When the detector probe is passing the fault, the audio signal is heard tailing off to a very low level.

Similar to the step voltage method, the cable under diagnostic must be traced and marked before fault locating. A very important advantage offered by the twist method is the capability to locate the fault in multi T-joint cable networks, based on the fact that the signal is always travelling in the direction of the fault.

Other configurations of detector probe are available, based on the direction of the audio frequency pickup coil. For example, a vertically placed receiver coil will produce the maxima at the point where the horizontally placed receiver coil (Figure 2-16) is producing minima.

One of the disadvantages of using a single receiver coil is interference from adjacent signal paths, such as earth links in the cable. A differential double coil method can be employed to minimize the interference. In the two-coil configuration, the distance between coils is intentionally set to be equal to the cable twist length, such that the common mode interference in both coils can be cancelled out, leaving only the difference between audio frequency diagnostic signals.

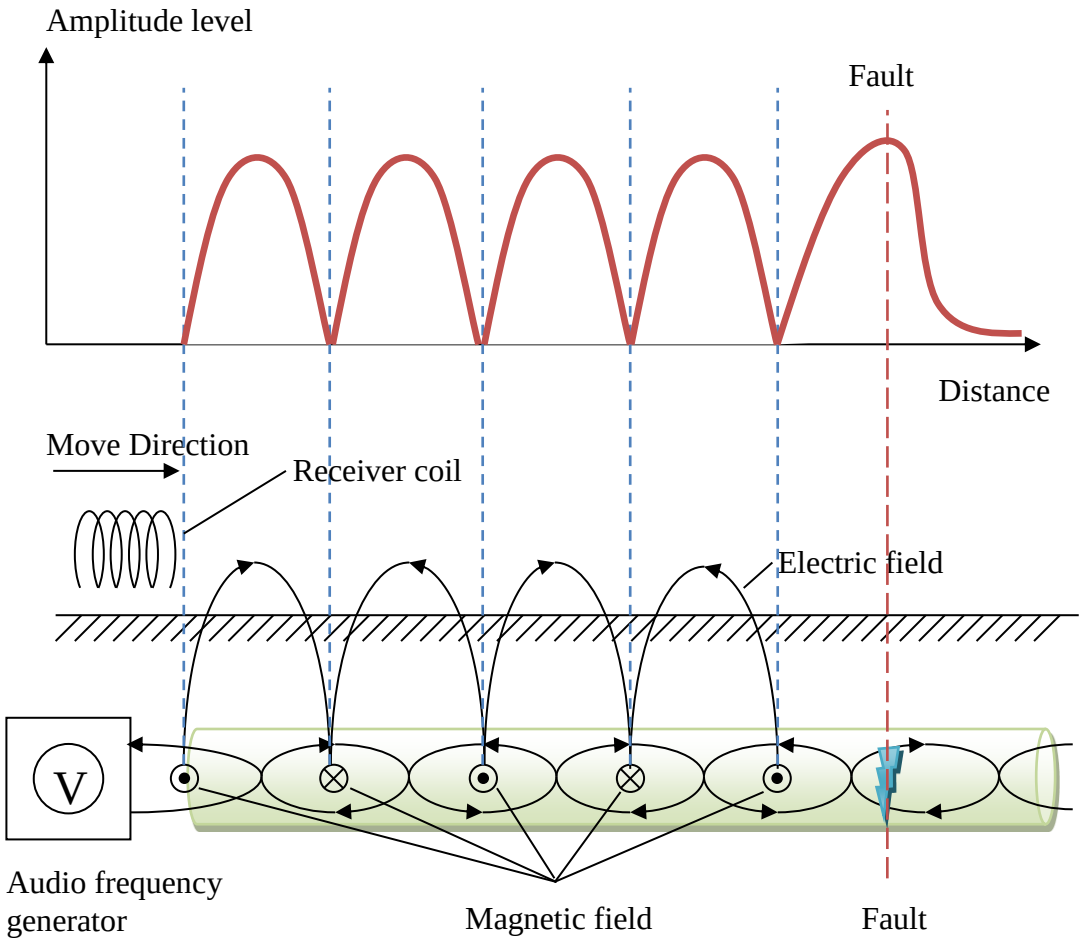


Figure 2-16: Illustration of Twist Method

2.5.4 Time Domain Reflectometry Method

2.5.4.1 Theory

Time domain reflectometry (TDR), which is also known as cable radar, is a technique utilizing transmission line theory and pulse reflection principles to detect impedance changes along a cable. It works similar to the principle of radar; by transmitting a pulse down a cable circuit and looking for return signals. The time it takes the pulse to travel down the cable and back is proportional to the distance, as shown in Figure 2-17.

TDR is one of the most common methods used for locating cable faults [6, 23-30]. The procedure for locating a fault using the TDR method is:

- The TDR system transmits a pulse along the cable under diagnostic
- This pulse is reflected back to the TDR system due to an impedance change in the cable
- This reflected pulse will be captured by the TDR system
- The time taken for the reflection to be captured is measured and converted to distance
- The reflected pulse shape is analysed to identify the impedance mismatch and hence the fault type.

The impedance change may be due to a shunt fault (e.g. short circuit) or a series fault (e.g. open circuit or end of cable).

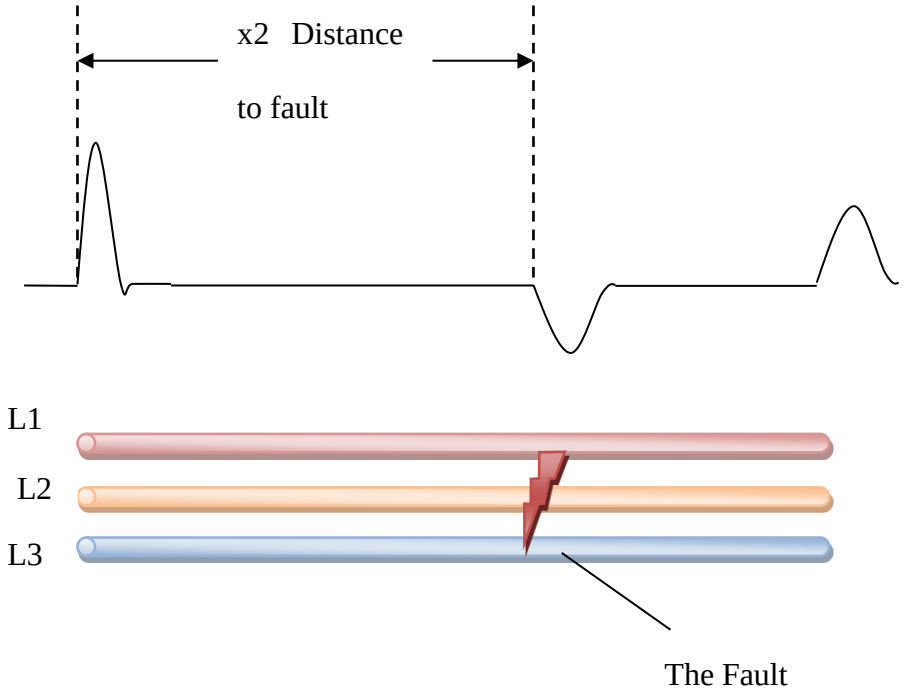


Figure 2-17: Illustration of Time Domain Reflectometry (TDR)

To calculate the fault distance D, it is essential to know the velocity of propagation (v_p) of the cable. Represented as a fraction of the speed of light, the propagation velocity can also be expressed as a velocity factor (VF). The v_p and VF depend upon

the cable dielectric, and can be estimated by using equation from an ideal (lossless) cable:

$$v_p = \frac{c}{\sqrt{\varepsilon}} \tag{2.24}$$

or,

$$VF = \frac{1}{\sqrt{\varepsilon}} \tag{2.24}$$

Where

c is the velocity of light in free space (2.998×10^8 m/s)

ε is the relative permittivity of the dielectric in the cable

Hence the distance to the fault D can be calculated from:

$$D = \frac{t \times v_p}{2} \tag{2.24}$$

2.5.4.1.1 Velocity Factor

Table 2-2 lists typical velocity factors for cables with different types of dielectric [6].

The v_p changes with:

- Cable impedance
- Design/structure/dielectric
- Service time of cable (age)
- Temperature
- Humidity
- Manufacturing variant

The VF for the cable should ideally be measured prior to the fault location. An easy way to achieve this is to measure the VF for a sample length of cable which is of the same type as the cable under diagnostic. Where the VF is unknown, TDR may still be applied by:

- Measuring from both ends and calculating the ratio of the transit times to the fault location, and then multiplying by the total cable length
- Using typical figures for the cable type; e.g. use 0.66 for 50 Ω coaxial cable

Table 2-2: Velocity factor list for common materials[31]

Dielectric	VF
Impregnated paper	0.5-0.57
Dry paper	0.72-0.88
PE	Approximately 0.66
XLPE	0.51-0.62
PVC	0.50-0.58
PTFE	Approximately 0.71
PILC	0.49-0.54
Air	Approximately 0.94

2.5.4.1.2 Pulse widths

Modern TDR systems offer the possibility to select the pulse width settings. Generally, the TDR pulse amplitude for a certain system is fixed at a low level (e.g. 5 V) to avoid damage to other equipment in the network. Therefore, the pulse width decides the energy of the pulse. The longer the pulse width, the more energy, and hence the further the signal will travel. Longer pulses can therefore be used to alleviate problems of attenuation and "spread" associated with transmission line effects, as

illustrated in Figure 2-18. Cables that are designed for higher frequencies (e.g. RF coaxial cable) cause less attenuation to the signals.

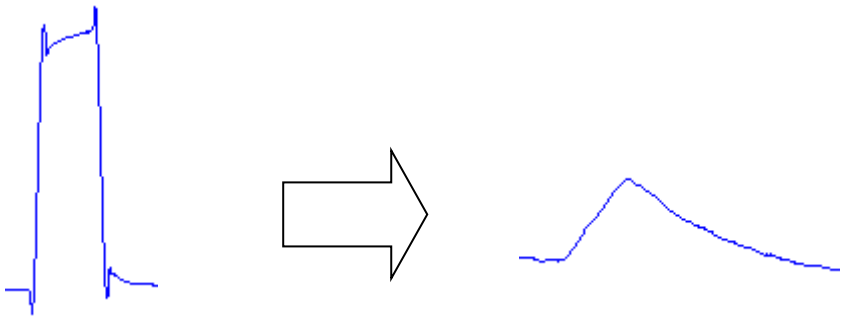


Figure 2-18: A rectangular pulse is distorted due to cable loss and attenuation

Another consideration for choosing pulse width is the deadzone. The concept of a deadzone is borrowed from the military radar industry, and it refers to those areas where faults cannot be detected. The pulse generator is driving the cable during transmission of the interrogation pulse, and hence the TDR is "blinded" during this period; therefore the deadzone may be hidden within the blinded period if the fault is close to the TDR system. The user must take all factors into account to select appropriate pulse width. Narrower pulses, for example, will offer a more clear view to consecutive faults; however they will not travel as far as wider pulses.

Aside from the deadzone caused by the blinded period, faults behind a fault may also be hidden in a deadzone, due to most of the transmitted energy being reflected by the first fault. Thus, a very important procedure to use TDR is to fix the nearest fault (first fault) before inspection of any further faults.

Table 2-3 shows the typical deadzone and fundamental frequency for different pulse widths.

Table 2-3: Typical dead zone and fundamental frequency for different pulse widths

Pulse Width	Dead Zone (VF=0.667)	Fundamental Frequency
<1 ns	<2 m	>1 GHz
5ns	10m	200MHz
10ns	20m	100MHz
100ns	200m	10MHz
1μs	2km	1MHz
10us	20km	100kHz
100us	200km	10kHz
500us	1,000km	2kHz

2.5.4.1.3 Reflection Coefficient for Faults

As discussed previously in section 2.2.3, a power cable can be considered as a TEM line where the characteristic impedance is defined as:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

The value of Z_0 for power cables mostly lays between 15 to 80 Ohms [6].

For any point of a TEM transmission line, the ratio of amplitude of reflected voltage wave to incident voltage wave is known as the reflection coefficient Γ.

Assuming that the impedance before a point of interest in a cable is Z_0^-, and accordingly the impedance after a point is Z_0^+, the voltage reflection coefficient Γ_V is given by:

$$\Gamma_V = \frac{V_0^-}{V_0^+} = \frac{Z_0^+ - Z_0^-}{Z_0^+ + Z_0^-} = |\Gamma_V| e^{j\theta_r} \quad (2.25)$$

Where:

$|\Gamma_V|$ is the magnitude of Γ_V, $|\Gamma_V| \leq 1$

θ_r is the phase angle

For a series fault, the impedance change on the cable is caused by the fault impedance in series with the characteristic impedance of the remaining cable, as shown in Figure 2-19. The impedance before the fault is given by:

$$Z_0^- = Z_0 \quad (2.25)$$

And the total impedance after the fault is:

$$Z_0^+ = Z_0 + Z_f \quad (2.25)$$

Hence the voltage reflection coefficient at the fault can be calculated by:

$$\Gamma_{Vseriesfault} = \frac{Z_0 + Z_f - Z_0}{Z_0 + Z_f + Z_0} = \frac{Z_f}{2Z_0 + Z_f} \quad (2.25)$$

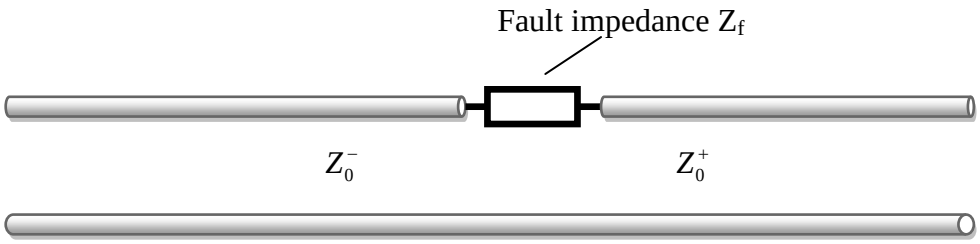


Figure 2-19: Illustration of series fault

For shunt faults, the impedance change on the cable is the parallel combination of the fault impedance and the characteristic impedance of the remaining cable, as shown in Figure 2-20. Therefore, the total impedance after the fault can be calculated by:

$$Z_0^+ = Z_0 \,||\, Z_f = \frac{Z_0 Z_f}{Z_0 + Z_f} \tag{2.25}$$

And the reflection coefficient for shunt faults is:

$$\Gamma_{Vshuntfault} = \frac{\frac{Z_0 Z_f}{Z_0 + Z_f} - Z_0}{\frac{Z_0 Z_f}{Z_0 + Z_f} + Z_0} = -\frac{Z_0}{2Z_f + Z_0} \tag{2.25}$$

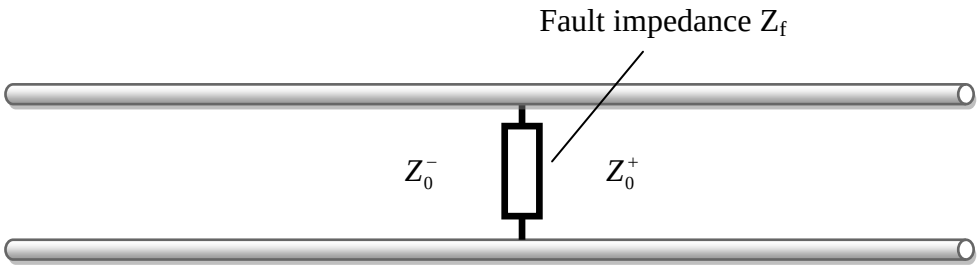


Figure 2-20: Illustration of parallel fault

A reflection diagram is plotted in Figure 2-21 to illustrate the relationship between fault impedance and reflection ratio. It can be concluded that a high reflection coefficient results from low impedance shunt faults or high impedance series faults. Two extreme cases for full reflection would be short faults and open faults.

It should be taken in to account that any impedance change in the cable will cause reflection, this includes loads, change in cable structure (e.g. split into a fuse box), waterlogged zones, cable joints, and end of cable. Cable joints and end of cable are the main causes of reflections which may lead to misinterpretation of the result.

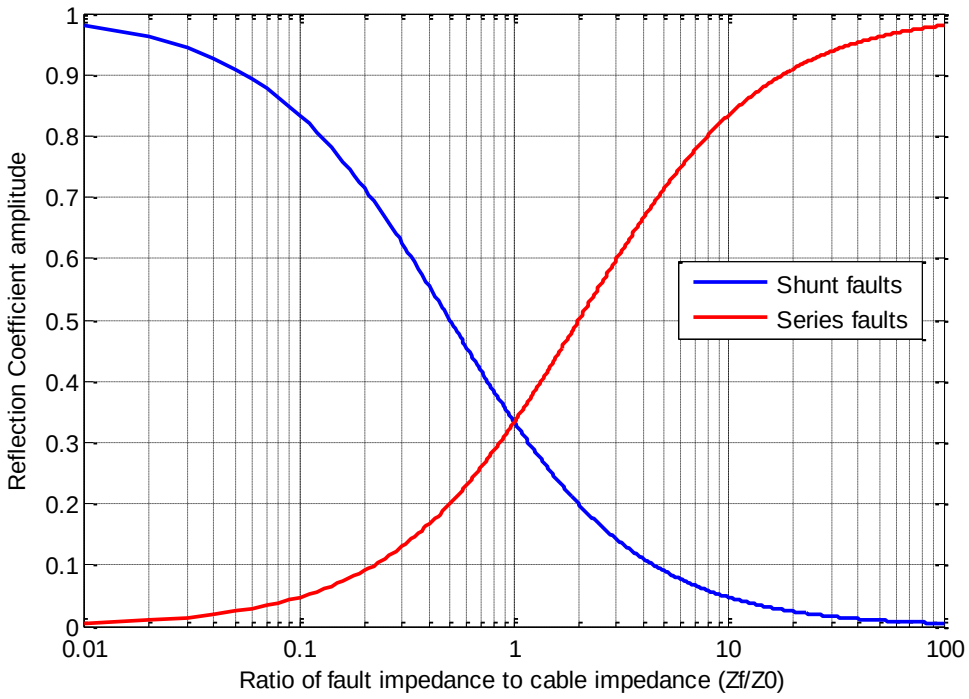


Figure 2-21: Reflection diagram of shunt faults and series faults

2.5.4.2 LV TDR method

TDR systems that use pulses of comparatively lower voltage may be classified as low voltage TDR (LV TDR) systems; most TDR products on the market are referred to as LV TDR.

There are many advantages for using LV TDR:

- Easy to implement as there is no high voltage circuit
- Low cost due to less components
- No damage to the cable and connected apparatus (e.g. meter)
- May be used while the cable is live
- Generally, no other equipment is required

However, use of a low voltage interrogation pulse does introduce some measurement limitations. As power cables are not designed to carry high frequency signals, high

attenuation of TDR signals will occur. The energy of the transmitted TDR pulse and subsequent reflections will be attenuated and dissipated as they traverse long power cables.

The success of TDR to address faults in LVUDN relies on the simplicity of the cable circuit being diagnosed. This is because T-joints in a cable network and parallel circuits at the diagnostic point could result in acquisition of a complicated waveform, therefore inducing inaccuracy in pre-locating faults. The system developed by Komoda et al. can address cable networks with three-phase tees [24], but without simultaneous investigation of single-phase tees. Navaneethan addressed the TDR in LVUDN with tees using the technique presented in [32], and [33] details TDR based upon novel combined logic. This system is further developed [34], and refined based on experimental results [35]. This approach systematically analyses the effect of T-joints in the power cable on TDR, and concentrates on the use of post-processing tools to overcome the restriction of TDRs.

2.5.4.3 Impulse Reflection method

The LV TDR method cannot be employed when a shunt fault is a high resistance fault, or when a series fault is a low resistance fault. This limitation can be overcome by utilising the impulse reflection method. The theory of the impulse reflection method is same as the LV TDR method, except that a high voltage surge generator is employed in this technology. The use of a high voltage surge generator serves the purpose of converting a high resistance fault to a low resistance fault that can be addressed by TDR. According to the coupling technique, the impulse reflection method may be classified into two categories: impulse voltage method and impulse current method.

The theory of the impulse reflection method is shown in Figure 2-22. The procedure is as follows: a surge generator (SG) releases a high voltage pulse into a cable. The pulse that travels along the cable may cause the fault point to flash over. The arcing fault generally lasts for a certain amount of time, and the impedance discontinuity created by the fault will cause the pulse to be reflected back to the source. These transient activities will be picked up by a low voltage measurement device, via a current or voltage coupling circuit.

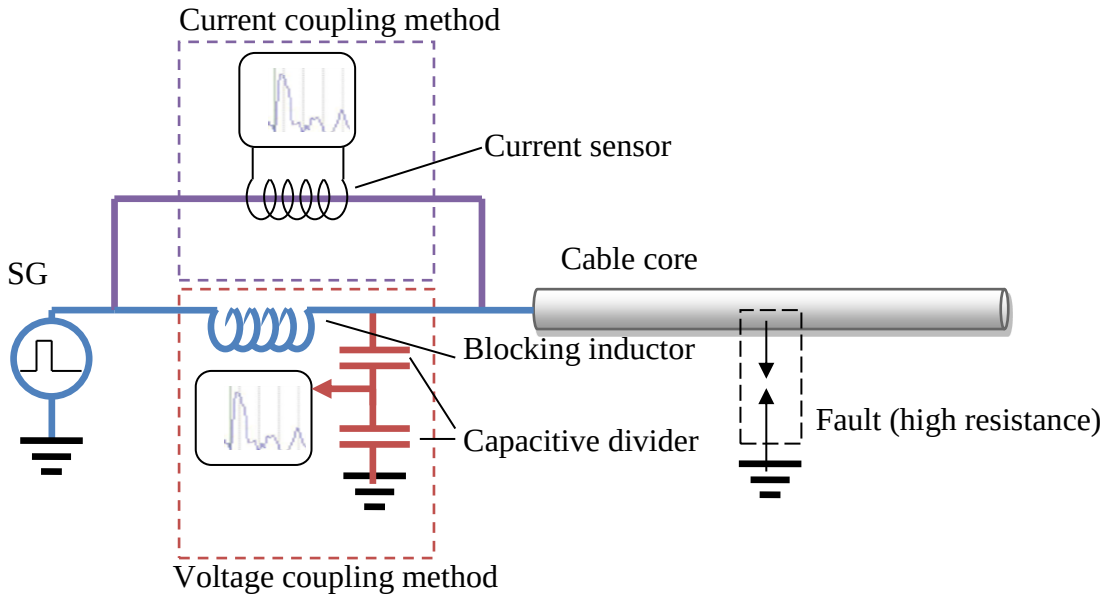


Figure 2-22: Impulse reflection with 1) Current coupling 2) Voltage coupling

It should be noted that a blocking inductor is required for the impulse voltage method. The blocking inductor acts as the output impedance of the surge generator, so that the voltage can be measured via a capacitive divider. The blocking inductor will reduce the efficiency of the surge generator, and the inductive delay will make the acquisition waveform more complex. Besides, due to direct electrical connection to the high voltage paths, the voltage coupling method (impulse voltage method) requires a series of safety precautions. Therefore, the impulse current method is more popular in

industry, due to its inherently safe nature, and removal of the requirement to use a blocking inductor [6, 23, 36]. In some circumstances where the fault requires very high breakdown energy, the voltage coupling method with a DC high voltage generator can be employed. In this case the fault may last until the DC high voltage generator is switched off, and the fault can be considered as an intermittent fault.

A reflection graph can be plotted in Figure 2-23. The high voltage pulse (or DC step) transmitted along the cable from A to B ignites the fault at position F. Generally, this fault will last long enough to cover a full diagnostic acquisition process. The arcing process is a very low resistance fault, and the pulse will be reflected and re-reflected between A and F, similar reflection activity is also occurring between F and B. Therefore, a typical waveform acquired at point A can be plotted, as shown in Figure 2-24.

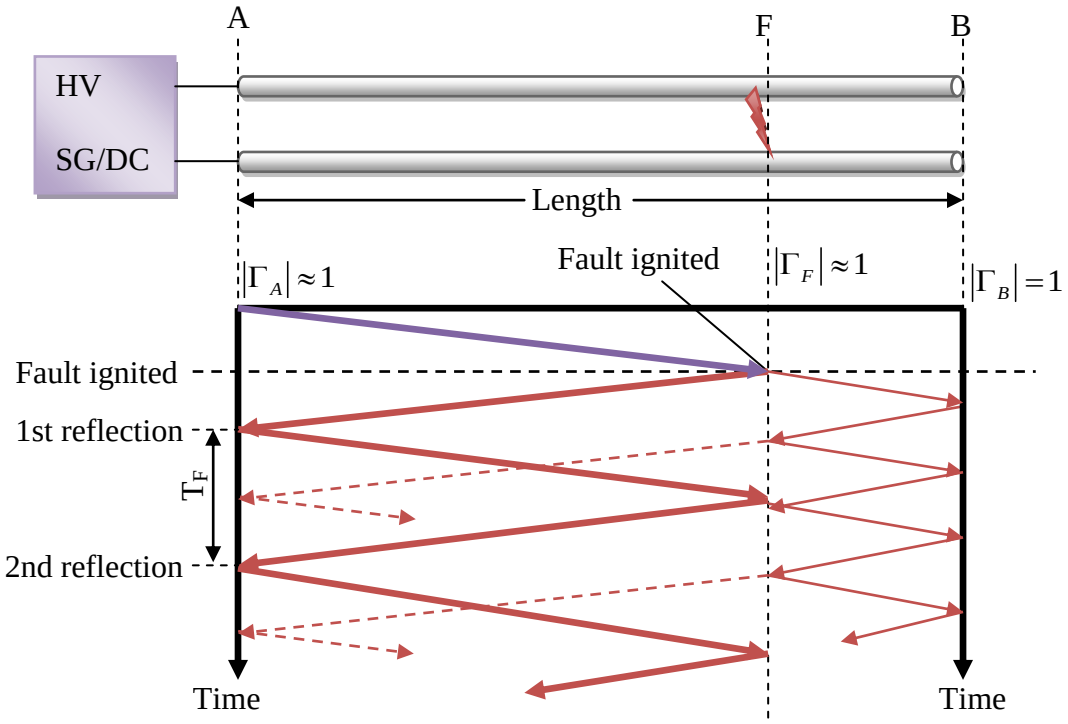


Figure 2-23: Bounce diagram for a cable with shunt fault

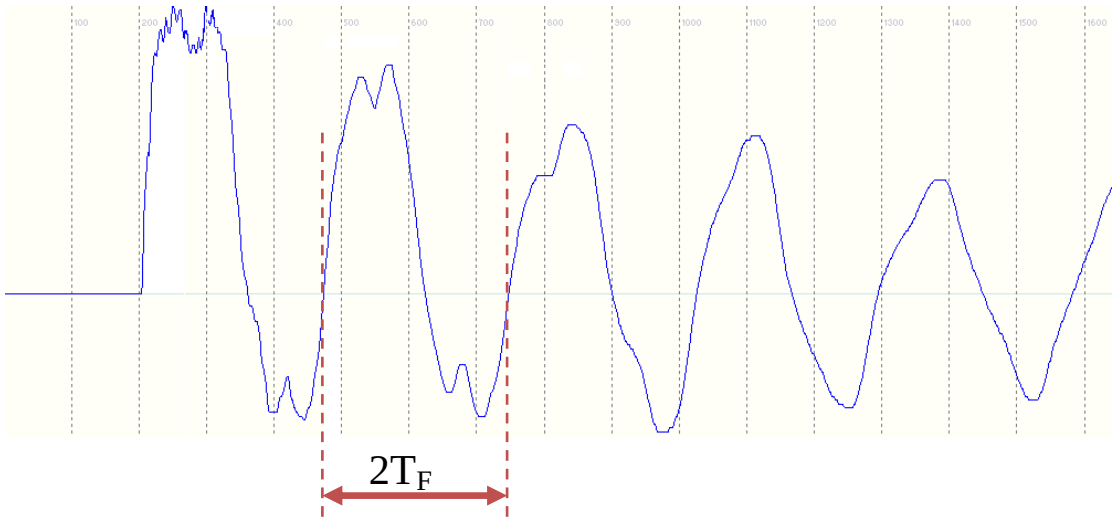


Figure 2-24: Example of a TDR waveform by impulse method

The reflection and re-reflection process diminishes the amplitude of the pulse because of the cable loss. It is important to note that, in most cases, the fault is not immediately ignited when the surge voltage arrives at the fault point, hence the fault ionization delay should not be considered as the edge for calculating the fault location. Any clear rising edge can be used to work out the location of the fault. The example in Figure 2-24 uses the time between the first reflection and the second reflection to calculate the fault distance. The remaining calculation is exactly the same as that used in the LV TDR method.

Apart from the limitations posted by all TDR techniques, the impulse reflection method can also be restricted by the ignition time. The ignition time is the time taken for the high voltage application to ignite the fault. This time is dependent upon the condition of the fault; it tends to be longer for transient faults, and shorter for intermittent faults.

2.5.4.4 Acoustic TDR

In the case when the cable circuit is simple (i.e. no T-joints) and short, the electrical coupling circuit of impulse reflection can be significantly simplified to an acoustic pickup device (e.g. microphone or piezoceramics). This technique is known as acoustic TDR [37]. The operation of this procedure is similar to that for detecting earthquakes. The diagram in Figure 2-25 shows the theory of operation. The surge generator or DC generator apply the high voltage to the cable; after some time, the fault breaks down and generates both electromagnetic and acoustic signals. The electromagnetic and acoustic signals will be radiated in all directions at different speeds, for instance V_E and V_A, respectively. Because the electromagnetic wave travels much faster than acoustic speed, the time difference for electromagnetic trigger and acoustic trigger at the sending end can be used to calculate the fault distance D:

$$D_{Fault} = V_A \times T_D \tag{2.25}$$

It should be noted that the cable cannot be too long; otherwise high attenuation to the acoustic wave will result in unsuccessful fault location.

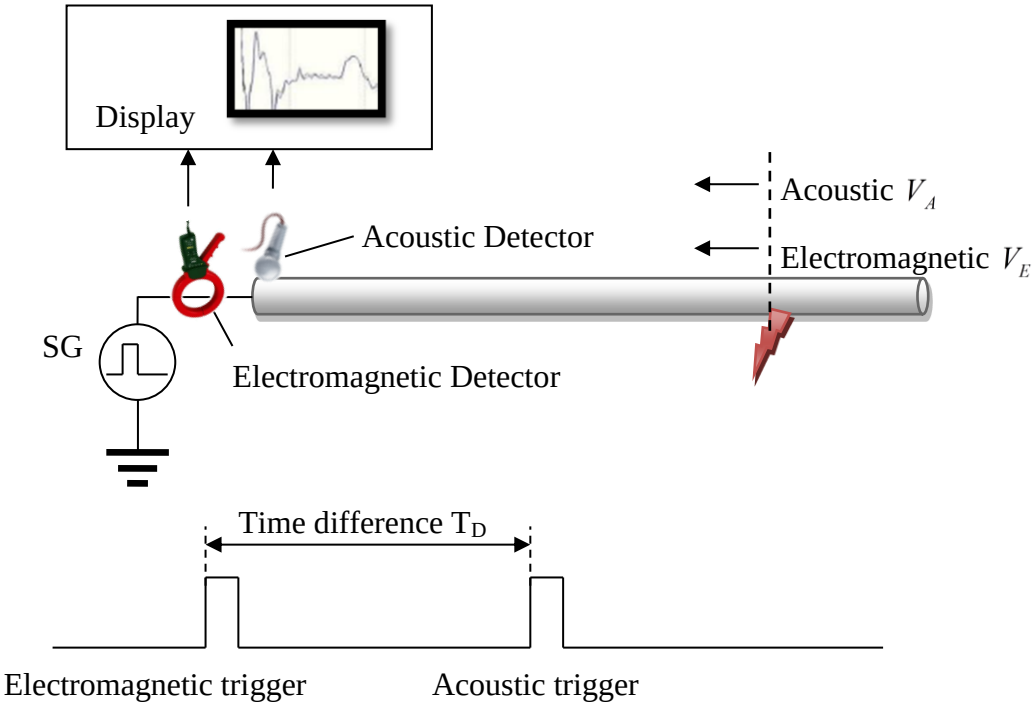


Figure 2-25: Illustration of acoustic TDR

2.6 Advanced Signal Processing Tools

Modern signal processing tools have been developed for years and play an important role in a wide range of applications, including audio and video processing, industrial control, communication systems, and military apparatus. It is therefore necessary to review the advanced signal processing tools to be used in this research. The tools to be reviewed are digital filters for filtering, wavelet transform for signal analysis, and fuzzy logic for decision making.

2.6.1 Digital Filters

In signal processing, a filter removes unwanted parts of the signal, such as random noise. This effectively extracts the useful parts of the signal i.e. signals lying within a useful frequency range.

Digital filters may be classified into two major types: constant coefficient filters and adaptive filters. As the name suggests, the coefficients of constant filters are designed beforehand, and no feedback to the filter coefficient is given. These filters are commonly used with prior knowledge to the input signals and filter performance. For the inputs that contain uncertain frequencies, adaptive filters would be more robust, due to the filter ability to adjust its coefficient by means of a feedback loop.

2.6.1.1 Constant Coefficient Digital Filters

Typical constant coefficient digital filters are finite impulse response (FIR) filters and infinite impulse response (IIR) filters. FIR filters are one of the primary types of filter used in digital signal processing (DSP). FIR filters are said to be finite because the impulse response to the input is within a finite time interval. A typical transfer function in Z-transform for FIR can be represented as [38]:

$$G(z) = \frac{y(z)}{x(z)} = g_0 + g_1 z^{-1} + g_2 z^{-1} + ... + g_n z^{-n} \quad (2.25)$$

Where:

$G(z)$ is the transfer function (response) of the filter

$x(z)$ is the input to the filter

$y(z)$ is the output from the filter

g_n is the gain in the nth delay

z^{-n} is indicating the nth delay

The implementation flow chart of the FIR filter is then shown in Figure 2-26.

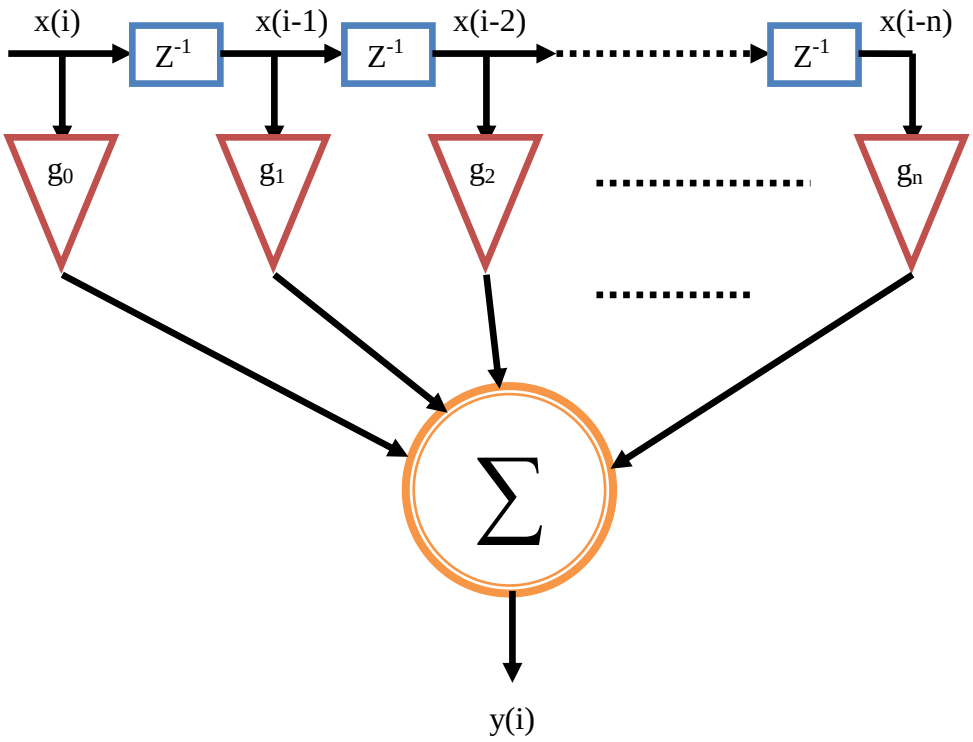


Figure 2-26: FIR implemented by Tapped Delayed Line (TDL)

From both the transform function and implementation flow chart, it can be seen that the output of an FIR filter is dependent upon the filtering coefficient (g_n) and the input (x(i)). The FIR filter has many advantages: it is stable, and can be easily designed to meet the expected performance (e.g. linear response).

The other type of constant coefficient digital filter is IIR. The transfer function of an IIR filter is [38]:

$$G(z)=\frac{y(z)}{x(z)}=\frac{a_0+a_1z^{-1}+a_2z^{-1}+...+a_nz^{-n}}{1+b_1z^{-1}+b_2z^{-1}+...+b_mz^{-m}} \tag{2.25}$$

Where:

a_n is the gain of input in the n[th] delay

b_m is the gain of output in the m[th] delay

By observing the transfer function of an IIR filter it can be seen that:

- The numerator of $G(z)$ $(a_0+a_1z^{-1}+a_2z^{-1}+...+a_nz^{-n})$ is exactly the same as that for the FIR, which further suggests that IIR contains an FIR
- The denominator part of $G(z)$ $(1+b_1z^{-1}+b_2z^{-1}+...+b_mz^{-m})$ suggests the output y(i) will be used to provide an infinite feedback (recursive) loop to itself.

These concepts are further illustrated via an implementation flow chart, as shown in Figure 2-27. The most significant difference of IIR to FIR is that IIR uses a feedback loop which would provide a non-zero response ($b_m \neq 0$) to the output over an infinite length of time.

Compared to FIR implementation, the IIR implementation can meet a given filter specification with less computation than an FIR implementation, but IIR filters induce nonlinear phase and are more sensitive to numerical problems.

The algorithm and coefficient of FIR/IIR filters are well developed and can be easily designed and evaluated in MATLAB.

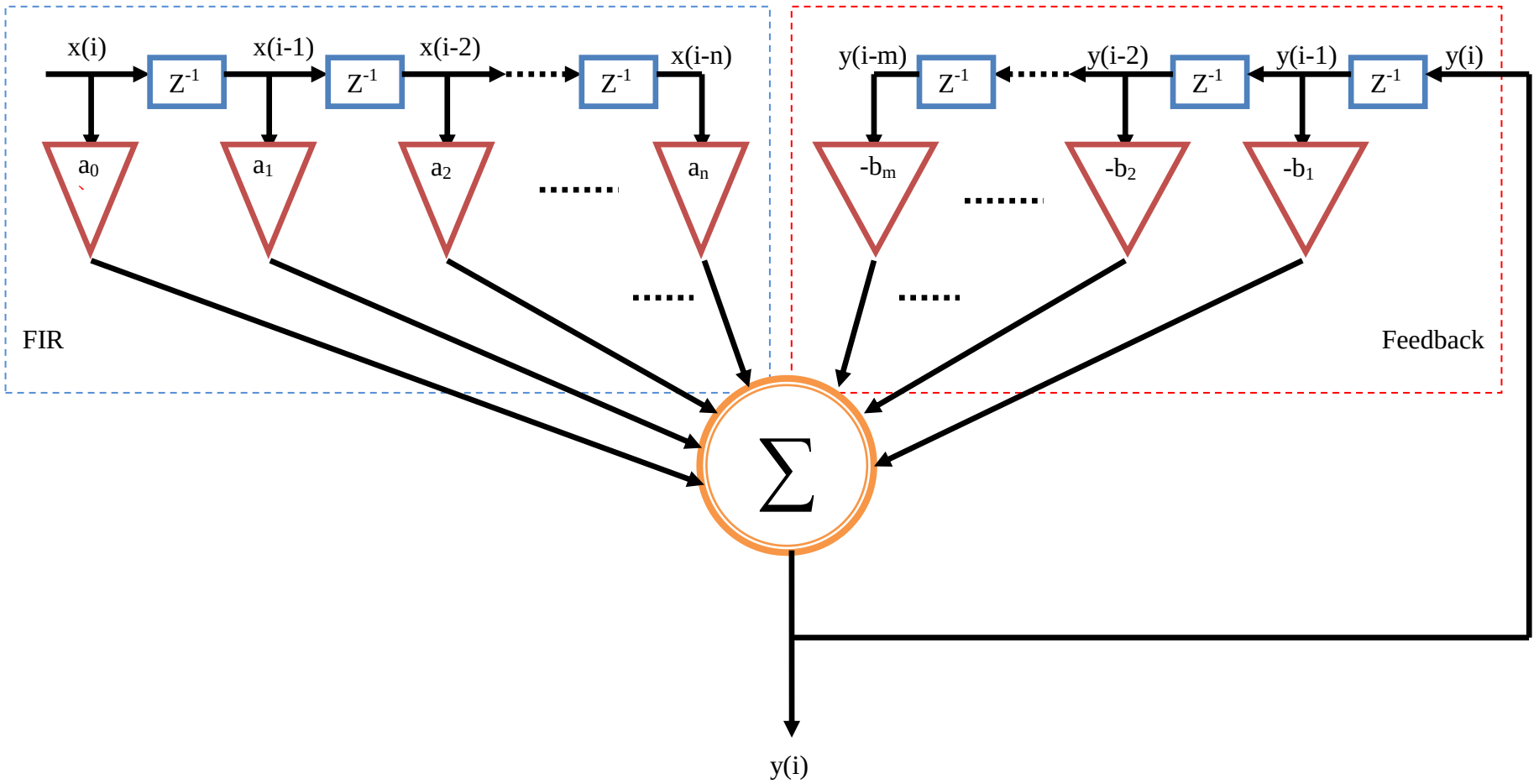


Figure 2-27: Block diagram of IIR filter

2.6.1.2 Adaptive filters

An adaptive filter is a type of filter that has coefficients that are updated by an adaptive algorithm, driven by an error signal. In contrast to constant coefficient filters, adaptive filters self-adjust their characteristic (transfer function) in accordance with a certain criterion. The process of adjusting the filtering coefficient to achieve the criterion is called the cost function. The cost function is the key algorithm to adapt the filter coefficient to its optimum state [39].

A great number of applications have been developed based on adaptive filters, including acoustic engineering (echo cancellations [39, 40], noise cancellation [39]), communication (multiple-input and multiple-output MIMO system equalization [41]), military applications (radar signal processing [39, 40]) and biomedical signal enhancement [39].

There are plenty of adaptive filtering configurations available [42], the most common implementations being least mean squares (LMS) and recursive least squares (RLS).

2.6.1.3 Basic Linear Adaptive Filters

The basic structure of an adaptive filter is shown in Figure 2-28. It consists of an input signal $x(n)$, a desired (reference) signal $d(n)$, an output filtered signal $y(n)$, and an error signal $e(n)$ which are related as shown in equation (2.26).

$$e(n) = d(n) - y(n) \tag{2.26}$$

Where:

$$y(n) = Filter[x(n)] \tag{2.27}$$

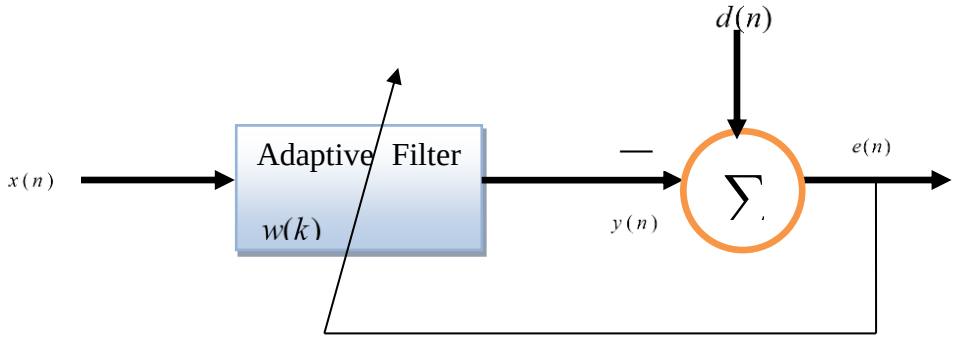


Figure 2-28: Adaptive Filter

The adaptive linear filter can also be characterized as a Tapped Delay Line (TDL), as shown in

Figure 2-29:

$$y(n) = \sum_{k=0}^{N-1} w(k)x(n-k) \qquad (2.28)$$

Where:

$x(n)$ represents the sequence of the input data

$w(k)$ represents the weights (filter coefficients)

N represents the number of taps (weights) in the adaptive filter

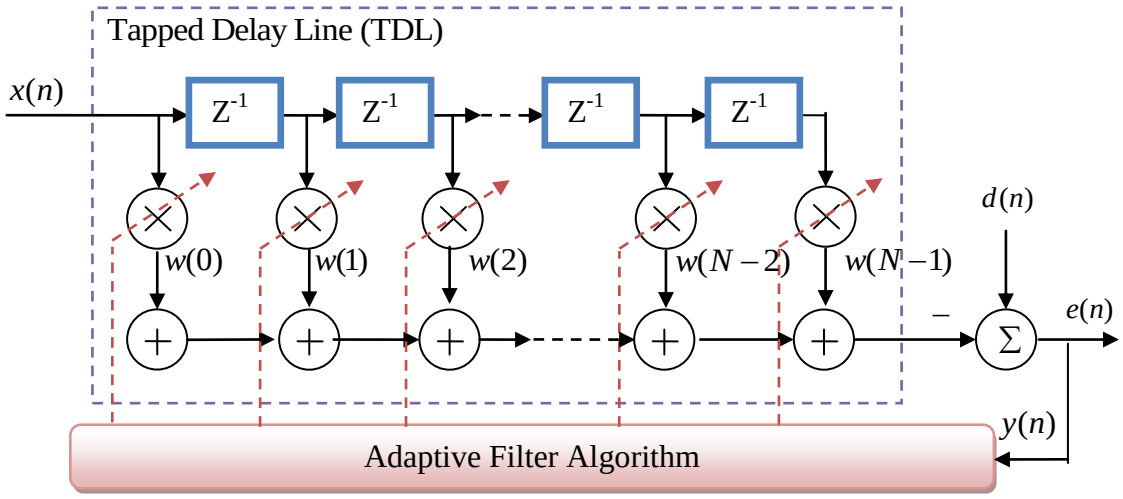


Figure 2-29: Adaptive linear filter can also be characterized as TDL

The expression of the above adaptive transfer function follows the same style as the correlation algorithm, this implying that the adaptive filter is iteratively exploiting the relationship between $x(n)$ and $d(n)$, such that the output approximates the desired signal $d(n)$ [39, 42].

The error signal $e(n)$ is given by:

$$e(n) = d(n) - y(n) = d(n) - \mathbf{w}^T\mathbf{x}(n) \tag{2.29}$$

The mean squared error (MSE) is given by $E[e^2(n)]$ and its relationship to desired signal $d(n)$ can be shown as [42]:

$$MSE = \xi = E[e^2(n)] = E[d^2(n)] + \mathbf{w}^T\mathbf{R}\mathbf{w} + 2\mathbf{P}^T\mathbf{w} \tag{2.30}$$

Where:

$E[...]$ is the statistical expectation operator

$E[d^2(n)]$ is the variance of $d(n)$

$\mathbf{P} = E[d(n)\mathbf{x}(n)]$ is the m length cross-correlation vector

$\mathbf{R} = E[\mathbf{x}(n)\mathbf{x}^T(n)]$ is the $m \times m$ auto-correlation matrix.

A plot of the MSE against the filter coefficients $w(0)$ and $w(1)$, as shown in Figure 2-30, is parabola-shaped with a unique vertex; this figure is known as the performance surface, and all values are positive.

The gradient of the MSE is given by:

$$\nabla(\xi) = \frac{\partial \xi}{\partial \mathbf{w}} = 2\mathbf{R}\mathbf{w} - 2\mathbf{P} \tag{2.30}$$

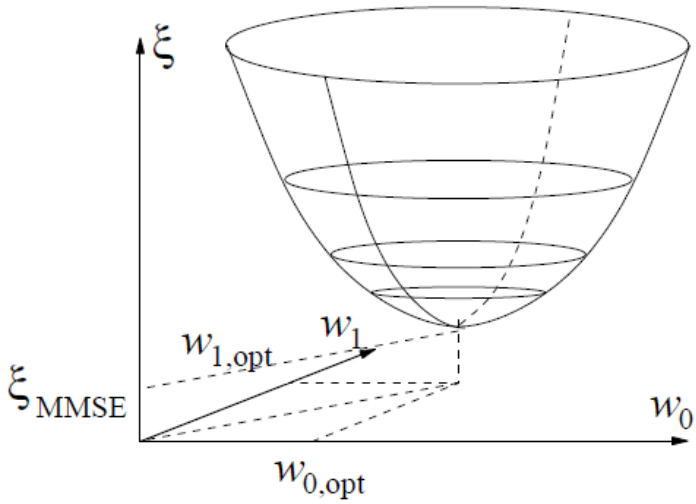


Figure 2-30: MMSE and adaptive filter coefficients

To find the minimum value of the *MSE*, the gradient is set to zero and the filter weight vector has its optimum value:

$$\mathbf{w}_{opt} = \mathbf{R}^{-1}\mathbf{P} \tag{2.31}$$

This is commonly known as the Wiener-Hopf solution [43]. However, this optimum solution is valid only if $\mathbf{R}$ is invertible, and there are many restrictions [44]:

- Confident estimation of $\mathbf{R}$ and $\mathbf{P}$ requires long time windows.
- Inversion of $\mathbf{R}$ is of computational order $O(L^3)$, this is very complex and time consuming.
- Even if $\mathbf{R}$ has full rank, it may be ill-conditioned, and if the signals are non-stationary, both $\mathbf{R}$ and $\mathbf{P}$ will change with time, this results in unstable filter performance.

Thus, for real-time applications such as transient signal conditioning, a faster method for obtaining the optimum coefficient w_{opt} is required. A widely used method for optimization is the steepest descent algorithm [39, 42, 44]. The steepest descent is an optimized method to minimize the value of a cost function depending on a number of independent parameters.

2.6.1.4 Least Mean Square (LMS) Algorithm

Least mean square (LMS) algorithm is one of the most famous classes of adaptive filters, invented by Bernard Widrow et. al in the 1960s [45]. The LMS algorithm utilizes the iterative approach to approximate towards the optimal solution instead of calculating w_{opt}. The LMS algorithm is started by assigning an initial guess value to the filter coefficient, which is usually zero. The algorithm then calculates the gradient vector, and the algorithm computes the next guess of the optimum filter coefficient towards the negative change of gradient. The above guess progress can be represented by this MSE cost function:

$$w(k+1) = w(k) - \mu\nabla(n) \tag{2.32}$$

Where:

$w(k)$ is the weight

μ is the step size of the guess (convergence) process

$\nabla(n)$ is the true gradient derived from the instant squared error $|e(n)|^2$

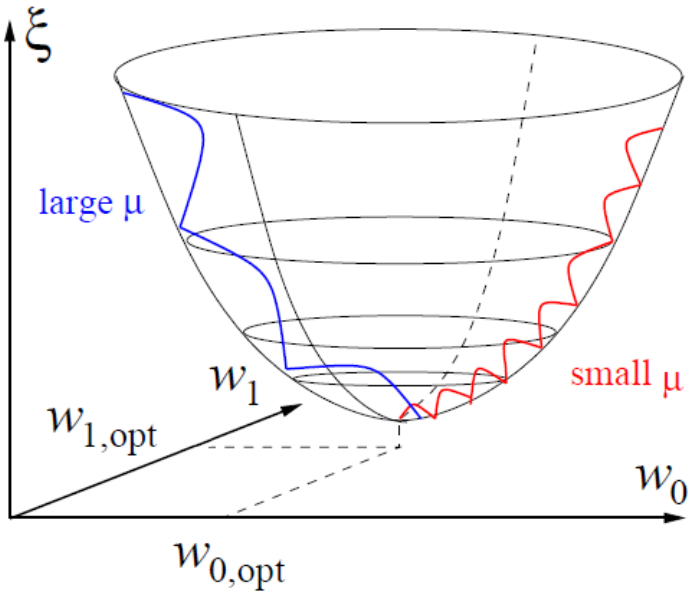


Figure 2-31: Approach MMSE by using larger step size and small step size

There is a trade-off in selection of the step size μ, between convergence speed and stability. As shown in Figure 2-31, large step size μ (blue) offers a faster tracking speed towards w_{opt}, however large μ may result in potential instability if the variant for each step is too large. Small step size μ (red) provides a good approximation to w_{opt}, however it may require excessive time for convergence.

The weight update can be re-written as:

$$w(k+1) = w(k) - \mu\left(\frac{\partial}{\partial w^*(k)} e(n)e^*(n)\right) \tag{2.33}$$

The calculation of the gradient is as follows:

$$\frac{\partial}{\partial w^*(k)} e(n)e^*(n) = \frac{\partial e(n)}{\partial w^*(k)} e^*(n) + e(n)\frac{\partial e^*(n)}{\partial w^*(k)} = -x(n)e^*(n) + 0 \tag{2.34}$$

Hence:

$$w(k+1) = w(k) + \mu e^*(n)x(n) \tag{2.35}$$

This is the typical LMS algorithm developed by Widrow et, al [45]. This is also known as the method of steepest descent. The most significant benefit provided by the LMS algorithm is that the time-consuming matrix inversion is no longer required, having been replaced by an iterative estimation.

By using an LMS algorithm, the filtering coefficients are adjusted iteratively towards the optimum performance with time, and eventually the weights converge. The condition of convergence is given as [44]:

$$0 < \mu < \frac{2}{L\sigma_{xx}^2} \leq \frac{2}{\lambda_{MAX}} \tag{2.35}$$

Where:

λ_{MAX} is the maximum eigenvalue of the input signal auto-correlation matrix.

L is the filter length .

σ_{xx}^2 is the variance of the input signal.

This also further suggests that the filter length L is in inverse-proportion to the maximum step size. The filter becomes unstable if the step size is placed outside of the convergence condition. Also, practically, the filtering coefficient may fluctuate around w_{opt} because the step size is fixed and not likely to be an integral multiple of the difference between w_{opt} and $w_{initial}$.

2.6.1.5 Normalised LMS (NLMS) Algorithm

The maximum step size in a standard LMS algorithm must be designed to cope with maximum input signal power; otherwise the algorithm will experience a gradient noise amplification problem [42]. However, in case the input signal is subjected to variant input signal power, the convergence speed is very slow when the input signal is of low power, as the maximum step size has been designed for highest input power. A normalized LMS (NLMS) algorithm can be employed to overcome this limitation. NLMS uses a variable step size that is normalized in accordance the input power.

The updated weight vector is given by [42]:

$$w(k+1) = w(k) + \frac{\hat{\mu}}{a + \|x(n)\|^2} e^*(n)x(n) \tag{2.35}$$

Where:

$\hat{\mu}$ is the adaptation constant

a is a positive small constant

$\|x(n)\|^2$ is the squared norm of the input vector

The adaptation constant $\hat{\mu}$ is assigned to control the step change of the weight vector iteratively, and this number must be positive to avoid change of convergence direction. The effective value of $\hat{\mu}$ is given as [39]:

$$0 < \hat{\mu} < 2 \tag{2.36}$$

The positive small constant a is used to prevent the update weight ($\frac{\hat{\mu}}{a + \|x(n)\|^2}$) from being unstable when the squared norm $\|x(n)\|^2$ is very small (i.e. when the input signal power is very small).

2.6.1.6 Recursive Least Square (RLS) Algorithm

The recursive least squares (RLS) algorithm is developed based on the least squares method. Reviewing the optimum weight vector equation provided by Wiener-Hopf:

$$\mathbf{w}_{opt} = \mathbf{R}^{-1}\mathbf{P} \tag{2.36}$$

Based on the equation above, the RLS method employs the following update step:

$$\mathbf{w}_{n+1} = \mathbf{R}^{-1}\mathbf{p}_n \tag{2.36}$$

Where the parameters are recursively defined as [44]:

$\mathbf{R}_n = \sum_{i=0}^{n} \beta^i \mathbf{x}[n-i]\mathbf{x}^T[n-i] = \beta\mathbf{R}_{n-1} + \mathbf{x}_n\mathbf{x}_n^T$, and

$\mathbf{p}_n = \sum_{i=0}^{n} \beta^i d^*[n-i]\mathbf{x}[n-i] = \beta\mathbf{p}_{n-1} + d_n^*\mathbf{x}_n$ †

By assigning $\mathbf{S}_n = \mathbf{R}_n^{-1}$, the RLS algorithm updates the $\mathbf{S}_n$ using matrix inversion lemma. This matrix inversion lemma is also known as the Woodbury matrix identity [46]:

$$(\mathbf{A}+\mathbf{BCD})^{-1} = \mathbf{A}^{-1} - \mathbf{A}^{-1}\mathbf{B}(\mathbf{C}^{-1}+\mathbf{DA}^{-1}\mathbf{B})^{-1}\mathbf{DA}^{-1} \tag{2.36}$$

By substituting $\mathbf{A} = \beta\mathbf{R}_{n-1}, \mathbf{B} = \mathbf{x}_n, \mathbf{C} = \mathbf{I}$(1-by-1 identity matrix) and $\mathbf{D} = \mathbf{x}_n^T$ into the Woodbury matrix identity (2.36), noting that $\mathbf{S}_n = \mathbf{R}_n^{-1}$:

† d^* is the conjugate transpose of d

$$\mathbf{S}_n = \frac{1}{\beta}\left(\mathbf{S}_{n-1} - \frac{\mathbf{S}_{n-1}\mathbf{x}_n\mathbf{x}_n^T\mathbf{S}_{n-1}}{\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n}\right) \tag{2.36}$$

Therefore the filter weight update step becomes:

$$\begin{aligned}
\mathbf{w}_{n+1} &= \mathbf{R}^{-1}\mathbf{p}_n = \mathbf{S}_n\mathbf{p}_n \\
&= \frac{1}{\beta}\left(\mathbf{S}_{n-1} - \frac{\mathbf{S}_{n-1}\mathbf{x}_n\mathbf{x}_n^T\mathbf{S}_{n-1}}{\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n}\right)(\beta\mathbf{p}_{n-1} + d_n^*\mathbf{x}_n) \\
&= \mathbf{S}_{n-1}\mathbf{p}_{n-1} + \frac{1}{\beta}\frac{\mathbf{S}_{n-1}\mathbf{x}_n d_n^*(\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n) - \mathbf{S}_{n-1}\mathbf{x}_n\mathbf{x}_n^T\mathbf{S}_{n-1}(\beta + \mathbf{x}_n d_n^*)}{\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n} \\
&= \mathbf{w}_n + \frac{\mathbf{S}_{n-1}\mathbf{x}_n(d_n^* - \mathbf{x}_n^T\mathbf{w}_n)}{\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n} \\
&= \mathbf{w}_n + \frac{\mathbf{S}_{n-1}\mathbf{x}_n e_n^*}{\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n}
\end{aligned} \tag{2.36}$$

Thus, the RLS algorithm can be summarized as:

$$\mathbf{w}_{n+1} = \mathbf{w}_n + Ke_n^* \tag{2.36}$$

$$\mathbf{S}_n = \frac{1}{\beta}(\mathbf{S}_{n-1} - K\mathbf{x}_n^T\mathbf{S}_{n-1}) \tag{2.36}$$

Where:

$$K = \frac{\mathbf{S}_{n-1}\mathbf{x}_n}{\beta + \mathbf{x}_n^T\mathbf{S}_{n-1}\mathbf{x}_n} \tag{2.36}$$

2.6.1.7 Computation Speed

Even though the RLS algorithm requires more complex matrix calculation, its computation speed is proven to be faster than the LMS algorithm [47]. As shown in Figure 2-32, an example is given for LMS and RLS algorithm to converge under the same white noise input. It can be seen that the RLS algorithm runs 28% faster than the LMS algorithm.

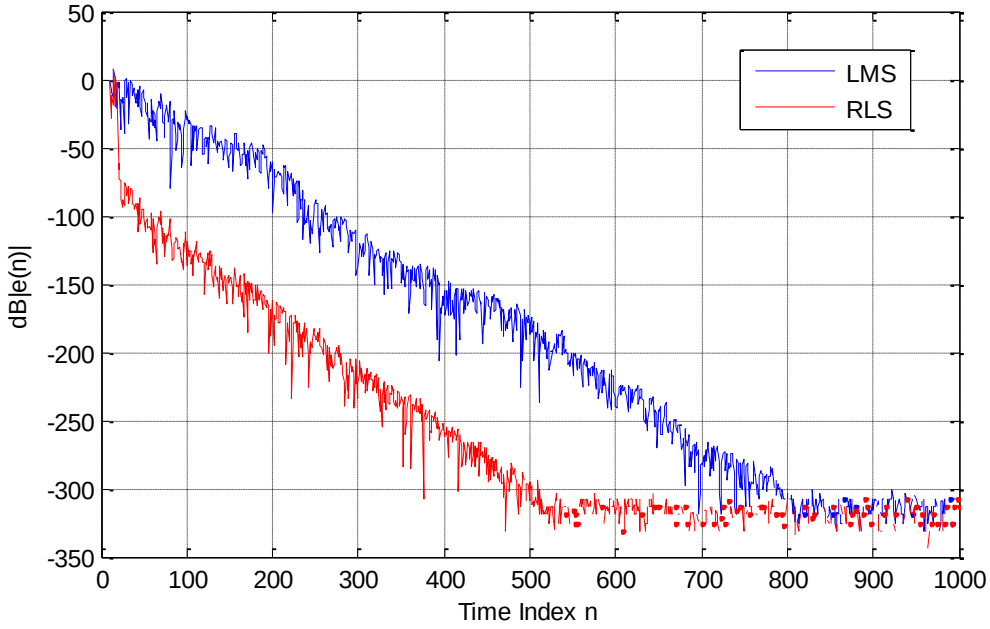


Figure 2-32: Performance compare of LMS and RLS algorithms

The performance and computation of LMS, NLMS and RLS adaptive algorithms are also provided in Table 2-4.

Algorithms	LMS	NLMS	RLS
Addition(+)/Subtraction(-)	2N	3N	$2N^2+2N$
Multiplication (*)	2N+ 1	3N+l	$2N^2+4N$
Division (/)	0	1	1
Data Storage	2N+3	2N+4	N^2+4N+4

Table 2-4: Computation complexity compare by LMS, NLMS and RLS algorithms

2.6.2 Fourier Transform

The Fourier transform (FT) is a mathematical decomposition operation that is able to interpret a time domain signal to a frequency domain signal (frequency spectrum). This property is extremely important, as it enables exploration of the frequency

composition of a time-based signal, and makes FT useful for a wide range of applications in signal processing.

The Fourier transform is based on the study of Fourier series, which is a branch of Fourier analysis. The Fourier series was first introduced by Joseph Fourier in 1807. The Fourier series defines that any periodic signal is a sum of a series of simple sinusoidal (sine and cosine) signals. In mathematics, that is [38]:

For any periodic signal $f(t)$ with period T, it can be expressed by a sum of sinusoidal simple waves:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(nx) + b_n \sin(nx)] \tag{2.36}$$

Where:

$$a_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \cos(nt)\, dt, \quad n \geq 0$$

$$b_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \sin(nt)\, dt, \quad n \geq 1$$

And:

$$a_0 = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)\, dt = \text{average value of } f(t) \text{ over period T}$$

By replacing the sines and cosines in the sinusoidal series by using Euler's formula, the exponential Fourier series is obtained:

$$f(t) = \sum_{n=-\infty}^{\infty} c_n e^{jnt} \tag{2.36}$$

Where c_n describes the Fourier coefficients, given by:

$$c_n = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) e^{-jnt}\, dt \tag{2.36}$$

The Fourier coefficient is the desired result of FT that contains the frequency domain information of the original signal $f(t)$.

2.6.2.1 Fast Fourier Transform (FFT)

The fast Fourier transform (FFT) is a special method to efficiently compute the discrete Fourier transform (DCT). The FFT is commonly seen as a computer algorithm to convert a discrete signal from the time domain to the frequency domain.

Figure 2-33 shows an example of a 50 Hz sine wave signal and its frequency spectrum calculated by FT. Another example is shown in Figure 2-34, a dual-tone multi-frequency signalling (DTMF) telephone keypad "1" signal, which is the composition of 1209 Hz and 697 Hz sine waves.

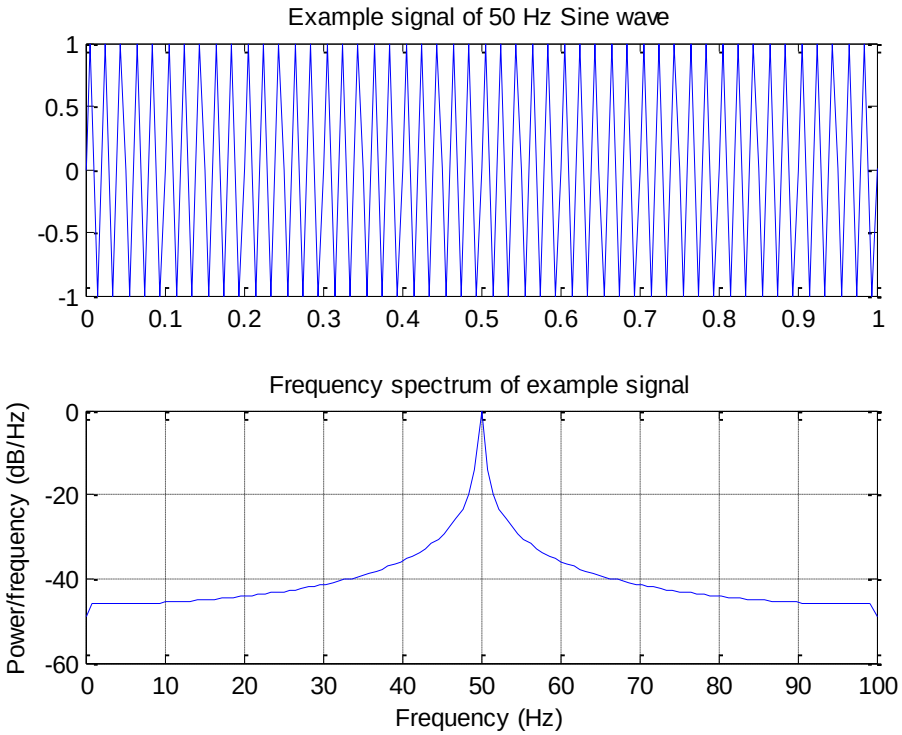


Figure 2-33: Time domain waveform and frequency spectrum of 50Hz sine wave with unity amplitude

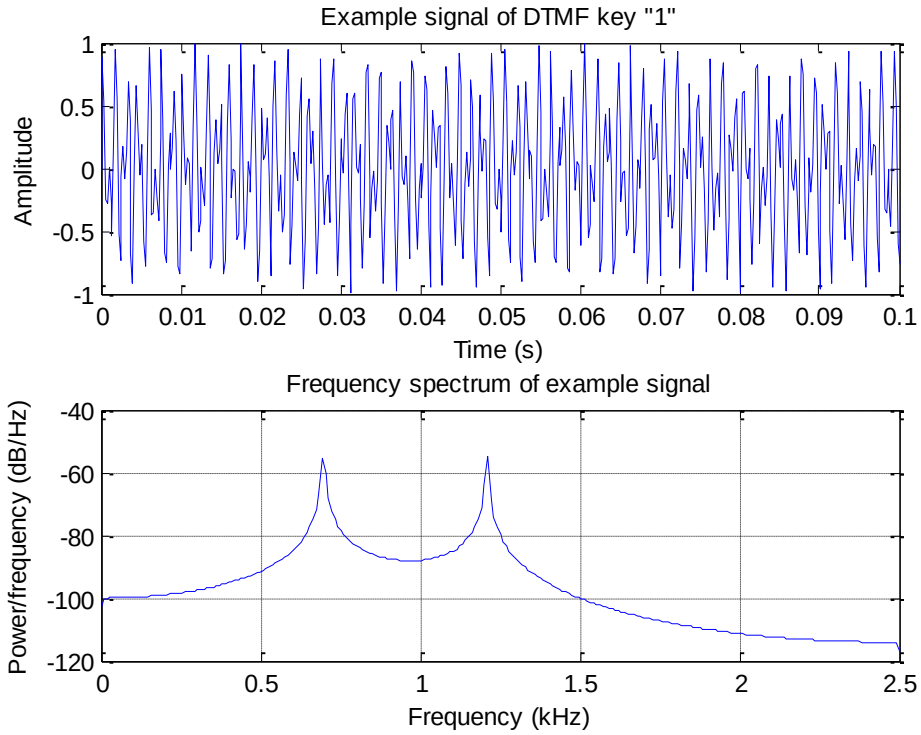


Figure 2-34: Time domain waveform and frequency spectrum of DTMF tone "1"

2.6.3 Wavelet Transform Theory

Wavelet transform (WT) theory covers a wide mathematical background, including harmonic analysis, real function theory, functional analysis, and matrix algebra theory. The WT concept was proposed by French oil industrial engineer J. Morlet in 1974, and is becoming an important technique in signal analysis, speech synthesis, computer vision, data compression, and many other engineering applications.

Compared with the Fourier transform, the WT can address both the time-domain and frequency-domain of a signal; whist the Fourier transform only provides global frequency information, and cannot assess the change in time-domain.

2.6.3.1 Similarities and differences between Short-Time Fourier Transform (STFT) and Wavelet Transform

The short-time Fourier transform is derived from the Fourier transform by replacing the sinusoidal wave series with the product of a sinusoid and a time-based window.

The mathematical definition of STFT is given by:

$$\mathbf{STFT}\{x(t)\} \equiv \langle x, g_{\tau,\omega} \rangle = \int_{-\infty}^{\infty} x(t) g(t-\tau) e^{-j\omega t}\, dt \qquad (2.36)$$

where the symmetric finite energy window g is defined as [48]:

$$g_{\tau,\omega}(t) = e^{j\omega t} g(t-\tau) \qquad (2.36)$$

And the spectrogram of STFT is the magnitude squared:

$$\text{spectrogram}\{x(t)\} \equiv |X(\tau,\omega)|^2 \qquad (2.36)$$

Therefore a Heisenberg box diagram can be draw in Figure 2-35 in order to represent the time and frequency localisation of an atom (element) of STFT [48]:

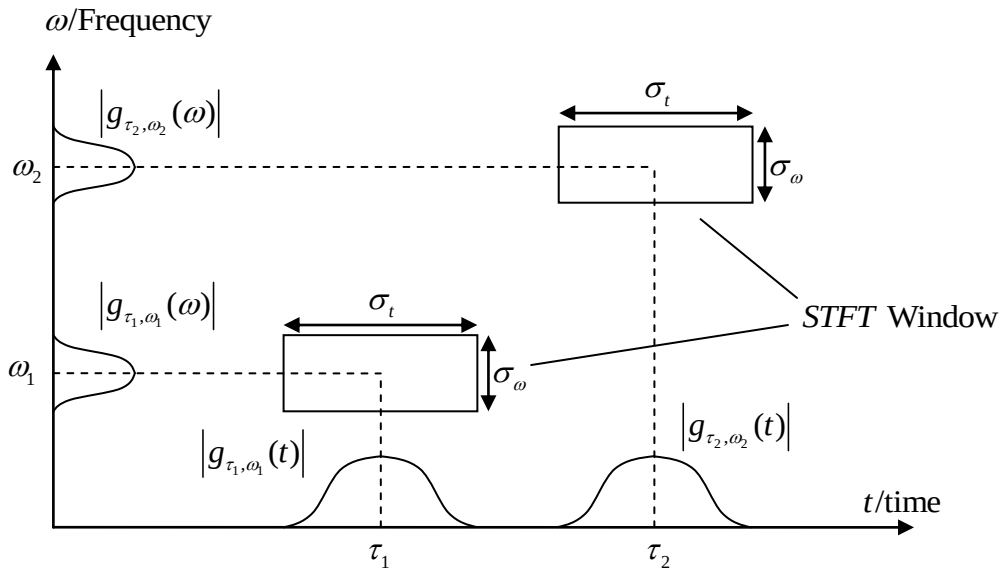


Figure 2-35: Heisenberg box example for STFT with two arguments: time and frequency

Similar to STFT, the WT is also derived from Fourier transform. However, instead of replacing with the product of a sinusoid and a time-based window, WT uses dilations and translations of a base atom called a wavelet to replace the sinusoidal wave series of the Fourier transform.

The wavelet transform is defined by:

$$\mathrm{WT}\{x(t)\} \equiv \langle x, \psi_{\tau,s} \rangle = \int_{-\infty}^{\infty} x(t)\psi^*(\frac{t-\tau}{s})dt \tag{2.36}$$

The base atom is given as:

$$\psi_{\tau,s}(t) = \frac{1}{\sqrt{s}}\psi\left(\frac{t-\tau}{s}\right) \tag{2.36}$$

Where the base atom is a special, real function which is integrated in zero, is symmetric in the y-axis, and has finite energy. It can be written in mathematical form:

$$\int_{-\infty}^{\infty} \psi(t)dt = 0 \text{ (Average in zero)} \tag{2.36}$$

and

$$C_{\psi} = \int_{-\infty}^{\infty} \frac{|\psi(s)|^2}{s} ds < \infty \tag{2.36}$$

It should be noted that while the time spread is proportional to the scale *s*, the frequency spread is inversely proportional to *s*. The Heisenberg box diagram of WT is shown in Figure 2-36:

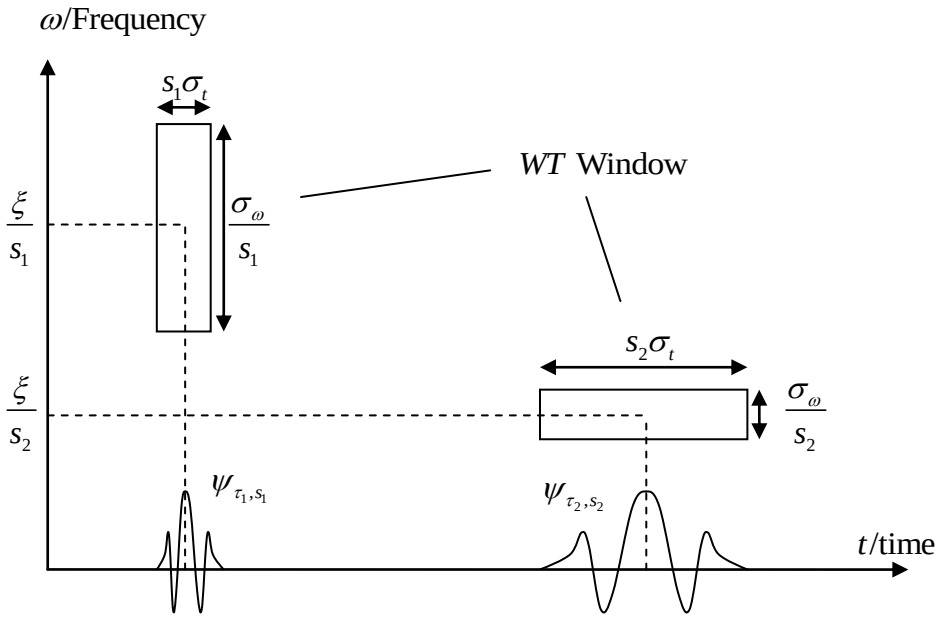


Figure 2-36: Heisenberg box example for WT with two arguments: time and scale

The most significant difference between STFT and WT is that WT windows are *localised in both the time and frequency planes*. Figure 2-37 is an example to represent this by comparison of the time-frequency tiles coverage of STFT and WT. This feature makes WT applicable to explore details of the frequency spectrum in time base. By alternating the coefficient of different time series, the WT transform can magnify/delete some time-frequency information, which makes it very useful in many applications, such as data compression, noise removal, and detecting of singularities. Meanwhile, the STFT has a fixed window, which further results in a fixed resolution for all frequencies. The fixed resolution would post some problems while exploring the spectral components of different frequencies.

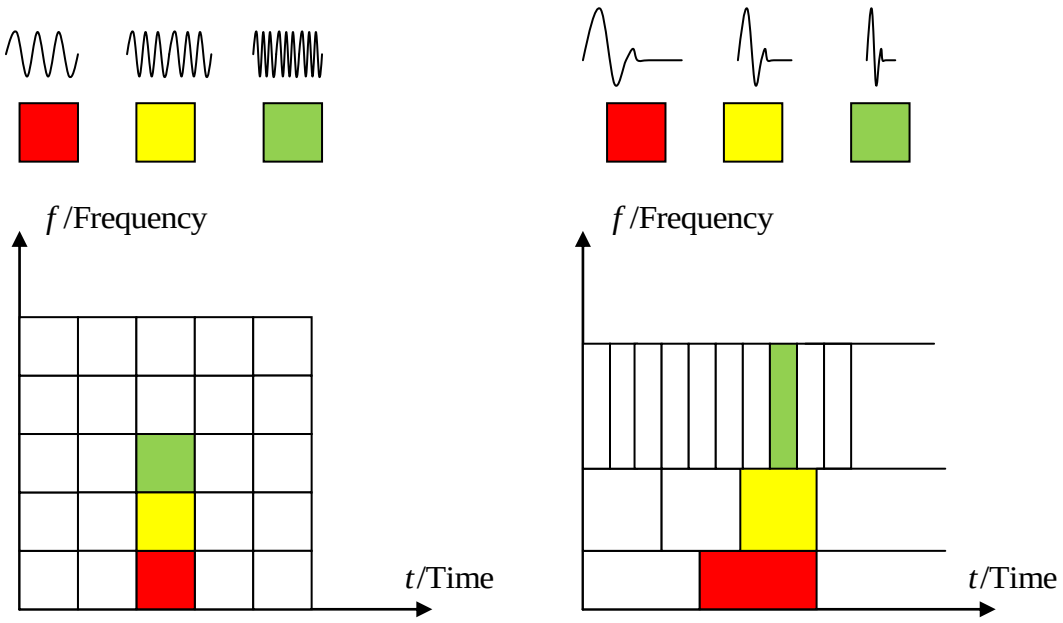


Figure 2-37: Fourier basis (left) and Wavelet basis (right) time-frequency tiles coverage in time-frequency plane. The coverage tiles of WT is localised in time and frequency plane

2.6.3.2 Discrete Wavelet Transform (DWT)

The wavelet transforms discussed above are often referred to as continuous wavelet transform (CWT), because the parameters s and τ are continuous. Therefore, the WT becomes a discrete wavelet transform (DWT) when the parameter s and τ are discrete values. One way to discretise the scale and time parameters s and τ is by applying Nyquist's rule [49]. Assuming two scales $s_0 < s_1$ with corresponding frequencies $f_0 > f_1$, Nyquist's rule defines that the wavelet coefficients at s_1 can be sub-sampled at the $\left(\frac{f_1}{f_1}\right)^{th}$ order of scale s_0. Therefore, by letting $s = s_0^a$ and $\tau = k\tau_0^b T$ (a, b are integers), and substituting into the wavelets definition in Equation (2.36), this yields:

$$\psi_{a,b}(t) = \frac{1}{\sqrt{s_0^a}} \psi\left(\frac{t - k\tau_0^b T}{s_0^a}\right) \tag{2.36}$$

Therefore the wavelet coefficients can be derived as:

$$C_{a,b}(x) = \sum_{-\infty}^{\infty} x(t)\psi^{*}_{a,b}(t)dt \tag{2.36}$$

And the original signal can be reconstructed by [50]:

$$x(t) = \sum_{a}\sum_{b} C_{a,b}(x)\psi_{a,b}(t) \tag{2.36}$$

2.6.3.3 Fast Wavelet Transform (FWT)

The fast wavelet transform (FWT) was introduced by Mallat in 1989 [51]. This algorithm is based on DWT and is considered "fast" because the coefficient can be obtained from a level-by-level scheme rather than directly using Equation (2.36). This scheme is a subband coding scheme.

The subband coding scheme is implemented with a low pass filter and a high pass filter, as shown in Figure 2-38.

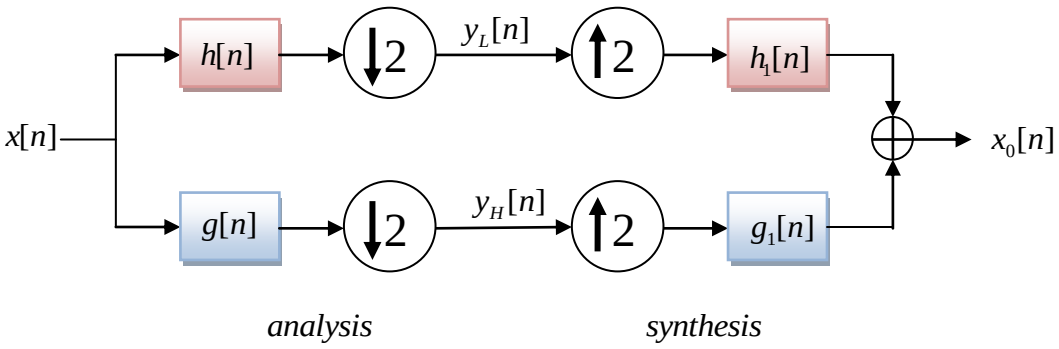


Figure 2-38: The Subband Coding Scheme of FWT

Where $h[n]$ and $g[n]$ are the impulse response of the low pass filter and the high pass filter, respectively. The whole process may be split into 2 parts: analysis and synthesis. In the analysis process, the original signal $x[n]$ will be passed through a low pass

filter $h[n]$ and a high pass filter $g[n]$, then down-sampled by a factor of 2, yielding $y_L[n]$ and $y_H[n]$. The result of the analysis process is then up-sampled by a factor of 2, passed through synthesis filters $h_1[n]$ and $g_1[n]$, and added together to reconstruct the original signal. The reconstructed signal $x_0[n]$ is not identical to the original signal $x[n]$, unless the filters meet some specific criteria.

A tree style cascading filter bank is applied to produce multi coefficients, as shown in Figure 2-39. The decomposition process must be a multiple of 2^n, where n is the number of levels. At each level, the coefficient is produced with a high pass filter and then down-sampled. The whole process is also termed *filter banks*. There are a number of research investigations regarding methods to obtain perfect filter banks.

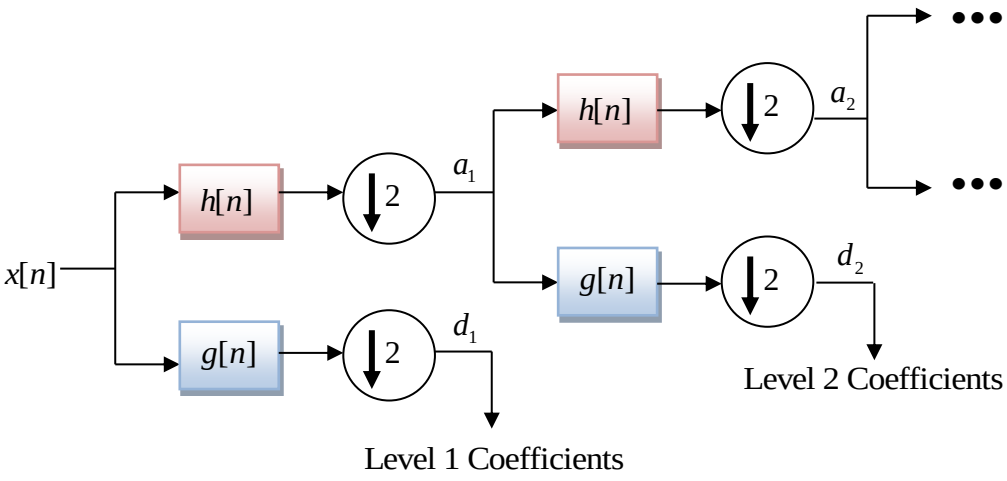


Figure 2-39: Produce WT coefficients by using tree style cascading filter bank

An example is shown in Figure 2-40 to illustrate how a WT can help to explore the transients in a 50 Hz voltage waveform, polluted by transient noise and 20 kHz – 100 kHz random switching noise (which is very common due to switching mode power supplies).

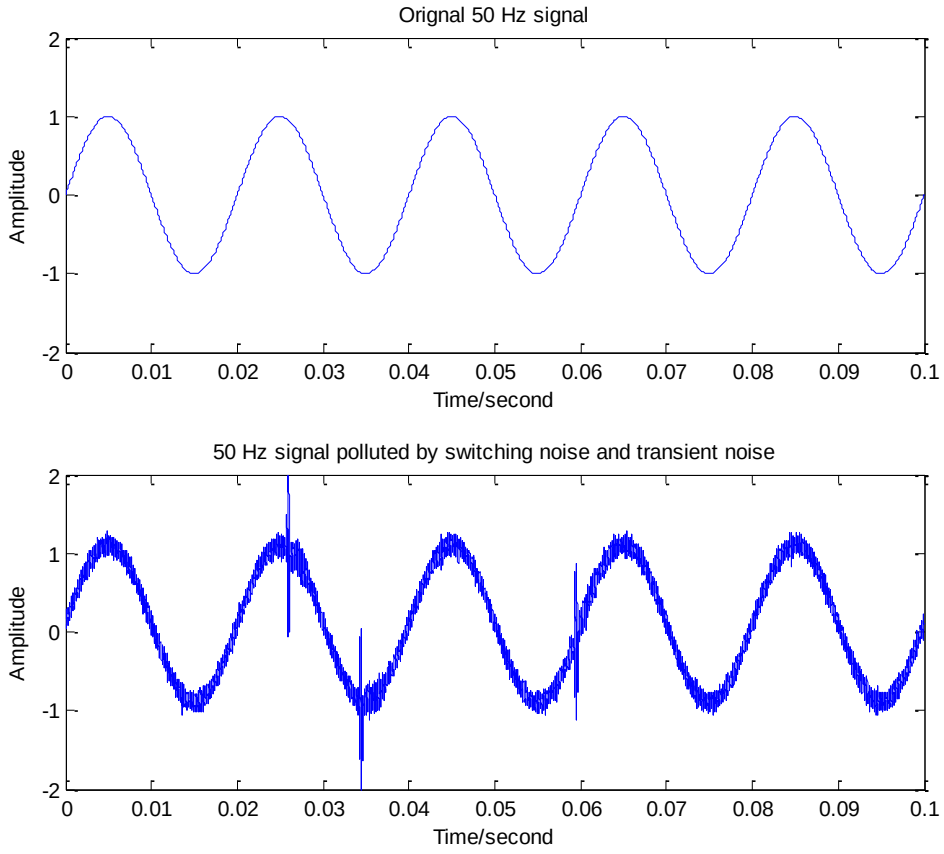


Figure 2-40: Example 50 Hz sinusoidal signal (a), and with switching noise and transient noise (b)

There are 2 purposes for applying a WT technique to the noisy sinusoidal signal: to extract the transient effect; and to remove all noise. In this example, the Symlets wavelet family at decomposition level 8 is used. The decomposition tree (filter banks) is shown in Figure 2-41. According to this decomposition tree, the details of all main signals are plotted in Figure 2-42. It should be noted that the reconstructed signal can be obtained by:

$$ss = a_8 + d_8 + d_7 + d_6 + d_5 + d_4 + d_3 + d_2 + d_1 \quad (2.36)$$

The transient noise is easy to explore by examining signals d_6, d_7 and d_8. The denoising process is relatively simple in this case, because the spectrums of the main noises (> 20 kHz) are far away from the original signal (50 Hz); therefore, the

optimised denoising method is to remove the high frequency components from d_1 to d_8, as shown in Figure 2-43.

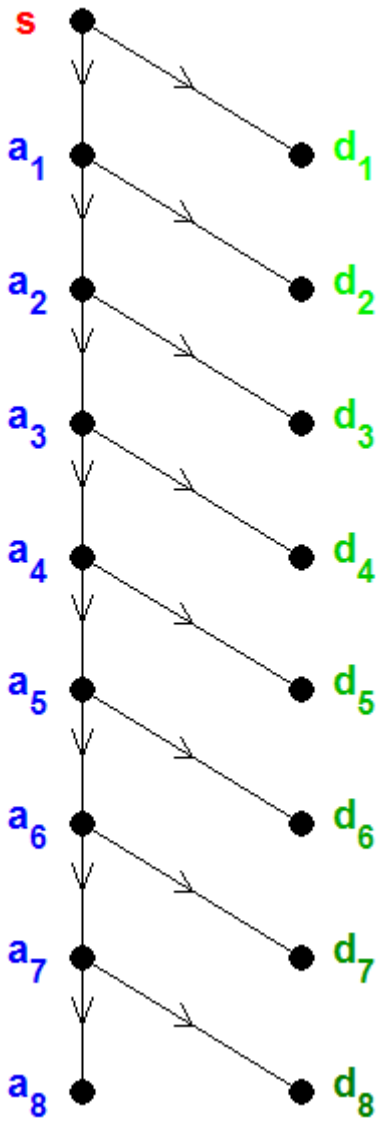
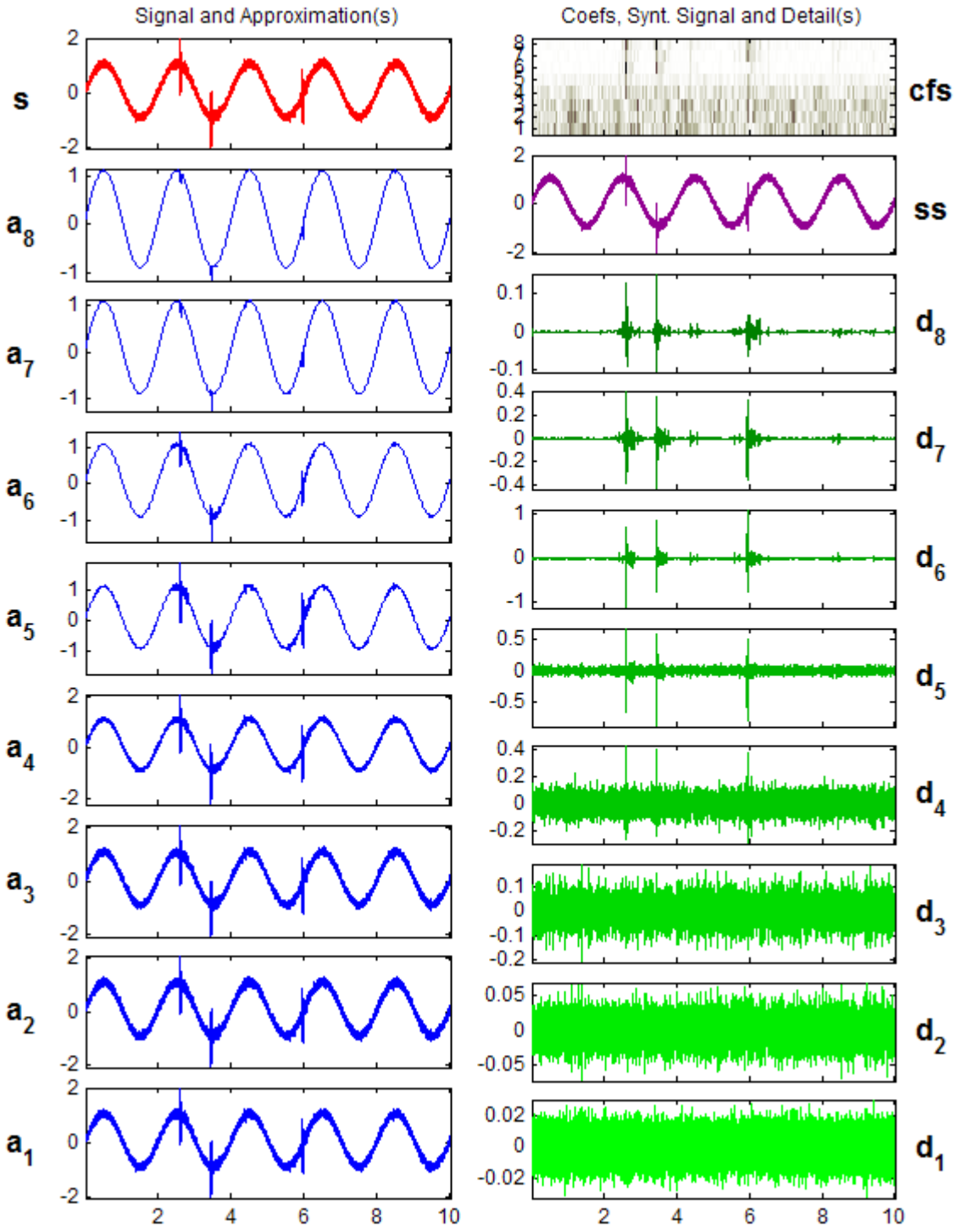


Figure 2-41: The 8 level decomposition tree of filter banks



s: original signal

a_1-a_8: approximations of the signal

cfs: coefficients of the synthesis filter

ss: reconstruction signal

d_1-d_8: decomposition of the signal

Figure 2-42: The decomposed signals in different step

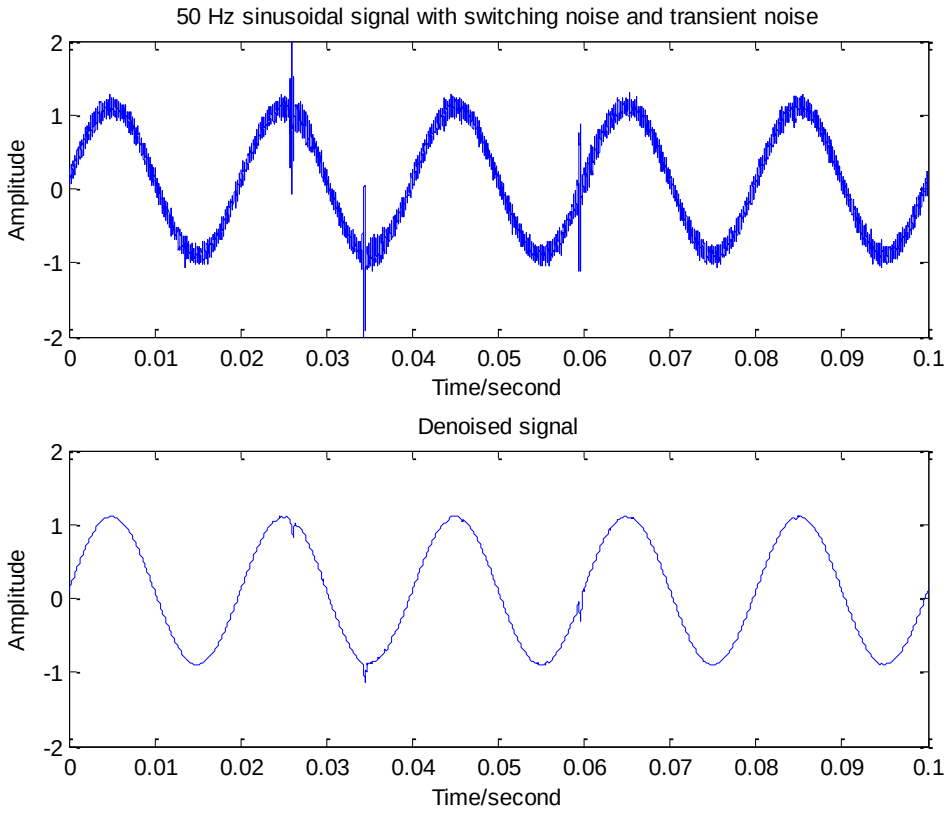


Figure 2-43: The 50 Hz sinusoidal signal before (a) and after (b) denoising process

2.6.4 Pulse Compression

Pulse compression is a signal processing technique to transmit a long duration pulse-shape signal with bandwidth corresponds to that of a short duration pulse. Pulse compression works by two processes [52]:

- Encoding: modulating the transmitted pulse
- Compression: recognising the transmitted pulse in the received signal by performing a correlating operation.

The pulse compression technique was widely used in applications including radar detection, sonar and echography, because the detection capability is increased, while

retaining the benefits of good range resolution and accuracy provided by short pulse systems.

2.6.4.1 Range Resolution and Energy

In radar systems, the range resolution is a parameter that describes the capability to distinguish targets that are in close proximity to each other. In an ideal scenario, the radar is expected to see the target at any location. However, in real cases, due to the limitation of components, a radar system is normally operated between minimum range $R_{\min}$ and maximum range $R_{\max}$. The detection range is then divided into N range bins, and the width of each bin is the range resolution ΔR. Targets within the range resolution distance ΔR would be recognised as the same target.

The range resolution depends on the pulse width of the signal [53]. An example is shown in Figure 2-44, a long pulse may result in bad range resolution as part of the reflection of the far target is hidden in the reflection shape of the near target (shaded area has the return from both targets). Since the radar bandwidth B is in inversely proportional to the pulse length τ, then:

$$\Delta R = \frac{v\tau}{2} = \frac{v}{2B} \tag{2.36}$$

The transmission speed v is equal to the speed of light c, if the travelling medium is free air.

As the pulse transmission speed v is fixed in a certain medium, the radar engineer normally minimises the pulse width and increases the bandwidth in order to achieve fine range resolution. However, a short pulse width normally results in reduced average transmitted power, and requires a very high bandwidth of the transmitting/receiving component.

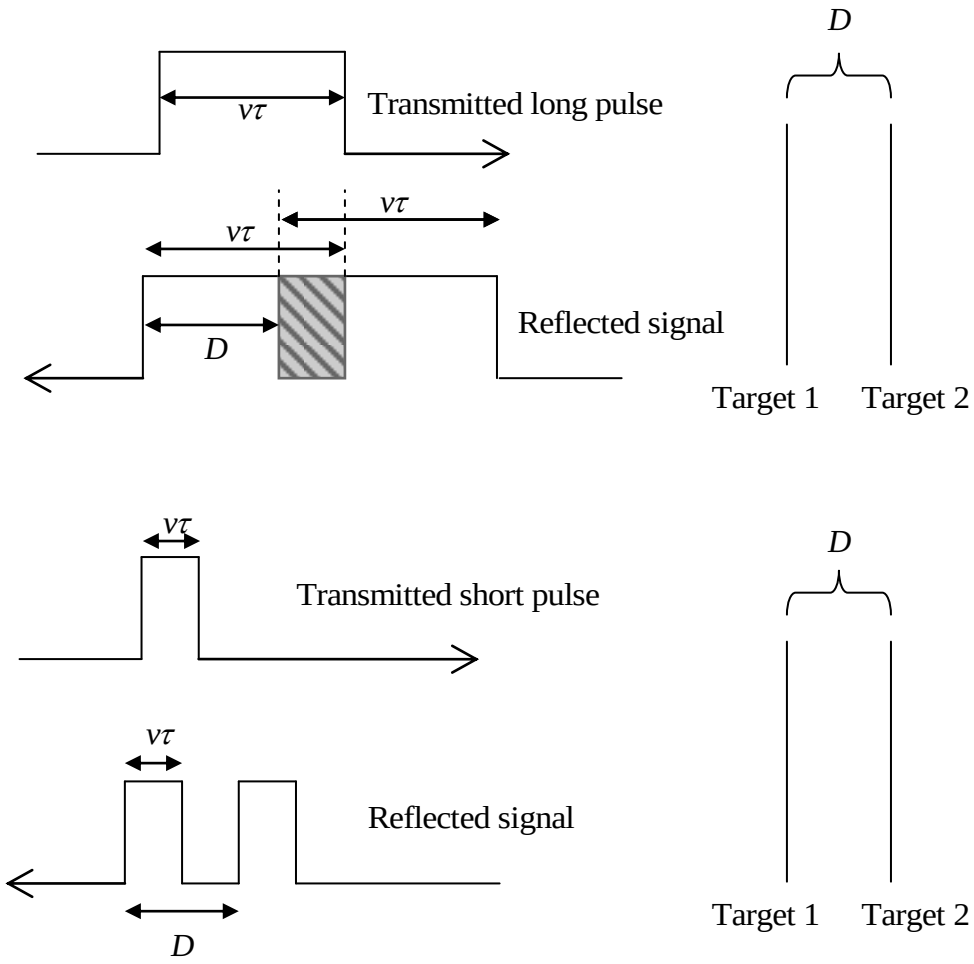


Figure 2-44: Pulse width and range resolution

2.6.4.2 The Compromise of Pulse Compression

The energy issue suffered by short pulses in radar systems can be resolved by applying pulse compression technology. The key of using pulse compression is modulating or encoding a long duration pulse to contain sufficient bandwidth B. It should be noted that the energy content of a modulated pulse before compression is comparable to that of a simple sinusoidal pulse with the same duration, which is much more than the energy content of a short pulse. For example, consider the design of a cable radar with required pulse energy $E = 1\,\text{mJ}$. According to the energy equation:

$E = P \bullet \tau$, the conventional approach using rectangular short pulse with pulsing duration of 1 μs requires the transmitter power:

$$P = \frac{E}{\tau} = \frac{1\text{ mJ}}{1\text{ us}} = 1\text{ kW}$$

The pulse compression approach with modulated pulse duration 1 ms only requires transmitter power:

$$P = \frac{E}{\tau} = \frac{1\text{ mJ}}{1\text{ ms}} = 1\text{ W}$$

This can be represented in an energy plot, as shown in Figure 2-45.

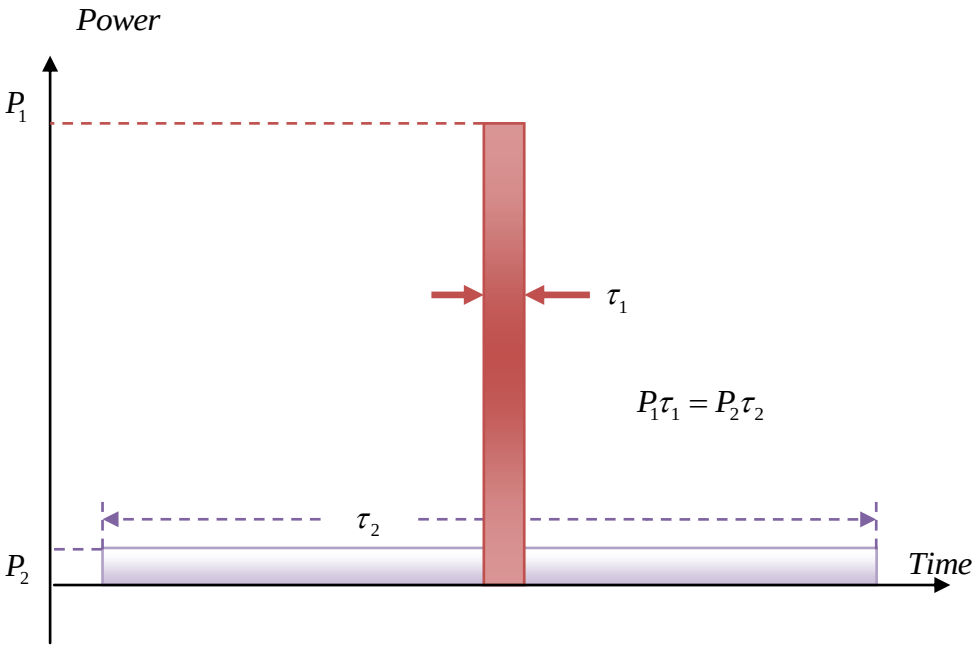


Figure 2-45: Energy carried by long-duration, low power pulse will be comparable to that of short-duration, high power pulse

2.6.4.3 Pulse Coding and Modulation

Pulse compression offers a technique to obtain the range resolution of a short pulse, while achieving the average transmitted energy of a relatively long pulse. To achieve a good compression result, the long pulse-like incident signal must be encoded to

maintain the high bandwidth corresponding to a short pulse. This encoded pulse will be passed to a matched filter that has a frequency response corresponding to the encoded pulse. By doing so, the long pulse-like signal is compressed and produces a result comparable to that of a short pulse.

The pulse compression technique may be divided into two categories: analogue pulse compression and digital pulse compression. Analogue pulse compression normally utilises a continuous waveform (CW) as the incident pulse, and processes the return signal continuously. Linear frequency modulation with correlation processing is a typical analogue pulse compression technology which is found in a number of radar applications. Digital pulse compression employs digital coding techniques to code the incident pulse and process the result in a digital form. It should be noted that although the digital information is carried by the incident pulse, the baseband signal that represents this incident pulse is continuous, as there are no real digital signals in the real world. The coding technique in digital pulse compression includes frequency codes (Costas codes), binary phase codes (Barker codes), and poly-phase codes (Frank codes) [54]. Amongst these digital coding techniques, the binary phase coding technique is the simplest and most straightforward in implementation. Barker codes are a family of the binary phase coding method that comes with a unique property: the compressed waveform has constant side lobe levels.

Brief discussion, comparison and examples of linear frequency modulation and Barker coding are given in the following section, as these are the two most important techniques for pulse compression.

2.6.4.3.1 Linear Frequency Modulation (LFM)

Linear frequency modulation (LFM) is the main coding approach for analogue pulse compression. The LFM is also called a chirp pulse, because the

frequency is modulated linearly like a chirp. The frequency change could sweep upwards (up-chirp) or downwards (down-chirp), as shown in Figure 2-46. The LFM waveform is also called an uncompressed pulse.

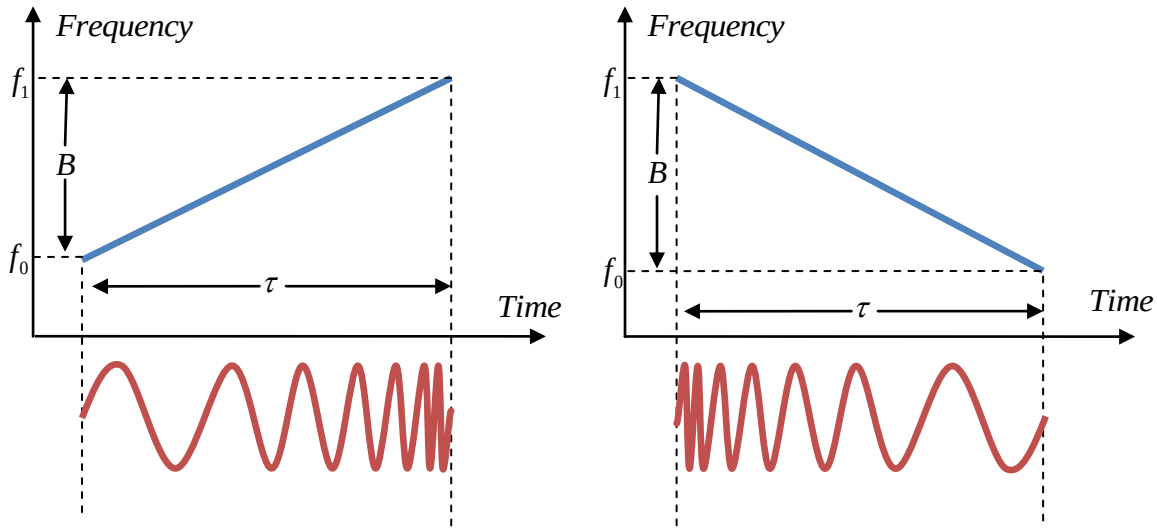


Figure 2-46: Typical LFM waveforms. Left: up-chirp; Right: down-chirp

A typical LFM waveform can be represented in this mathematical expression:

$$y(t) = rect\left(\frac{t}{\tau}\right) Ae^{j\pi\beta t^2} \tag{2.36}$$

Where:

A is the amplitude

β is the frequency sweep rate

$rect$ denotes a rectangular window of width τ

The bandwidth B of the LFM waveform is only dependent on the range of frequencies:

$$B = f_{Highest} - f_{Lowest} \tag{2.36}$$

The wider the frequency range swept, the higher the bandwidth.

The compression process requires a compression filter that performs a correlation between the uncompressed pulse and received signals. The recognition of the original uncompressed pulse is achieved by passing the received pulse through a pulse

compression filter. The presence of the original uncompressed pulse will then be recognised once the compression process has completed. The above correlation process can also be represented by a received signal being passed to a matched filter, whereby the correlation between the received signal and the matched filter (of the uncompressed pulse) is obtained.

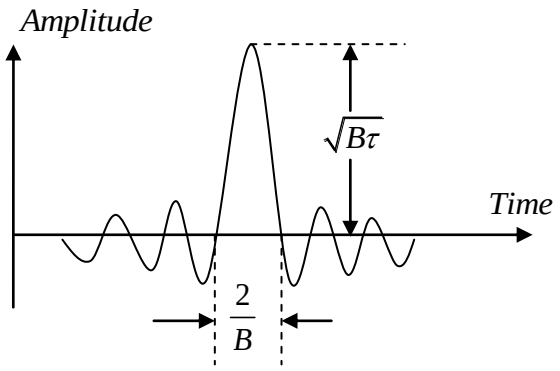


Figure 2-47: Typical output after a LFM waveform has been passed a pulse compression (Matched) filter

The compression of the LFM pulse gives an output that has a shape similar to the SINC function[†]. Figure 2-47 shows a typical output (compressed pulse) by passing a LFM pulse (uncompressed pulse) through a pulse compression filter. The amplitude of the main slope is equal to the geometric mean between bandwidth and uncompressed pulse width, whilst the width is the inverse of the bandwidth. The product of the bandwidth and the uncompressed pulse width is known as the pulse compression ratio γ:

$$\gamma = B \times T \tag{2.36}$$

[†] $SINC(x) = \frac{\sin x}{x}$

By tuning the bandwidth and pulse width of an uncompressed pulse, a high pulse compression ratio of the output can be achieved, resulting in an equivalent to a very narrow width but high amplitude output.

It should be noted that up-chirp and down-chirp signals with the same pulse width and bandwidth yield identical compression outputs.

An example of LFM modulation is given to further illustrate the LFM pulse compression. Figure 2-48 shows the real part, image part and 3D plots of a LFM chirp with unity amplitude, width of 40 μs, sweeping from 1 MHz to 2 MHz. The compressed result is presented in Figure 2-49, which shows a clear, sharp result after pulse compression.

This is not realistic however, as the uncompressed pulse may be affected by noise or attenuation in the real word. Noise and attenuation are problems that significantly affect the result of most cable TDR equipment. Hence, a random white noise corresponding to 50% of the original amplitude (SNR = 10 dB) is added to the uncompressed signal, as shown in Figure 2-50. The results are presented in Figure 2-51, which shows that the pulse compression is more robust towards the noise, while the peak amplitude and range resolution is still clearly visible.

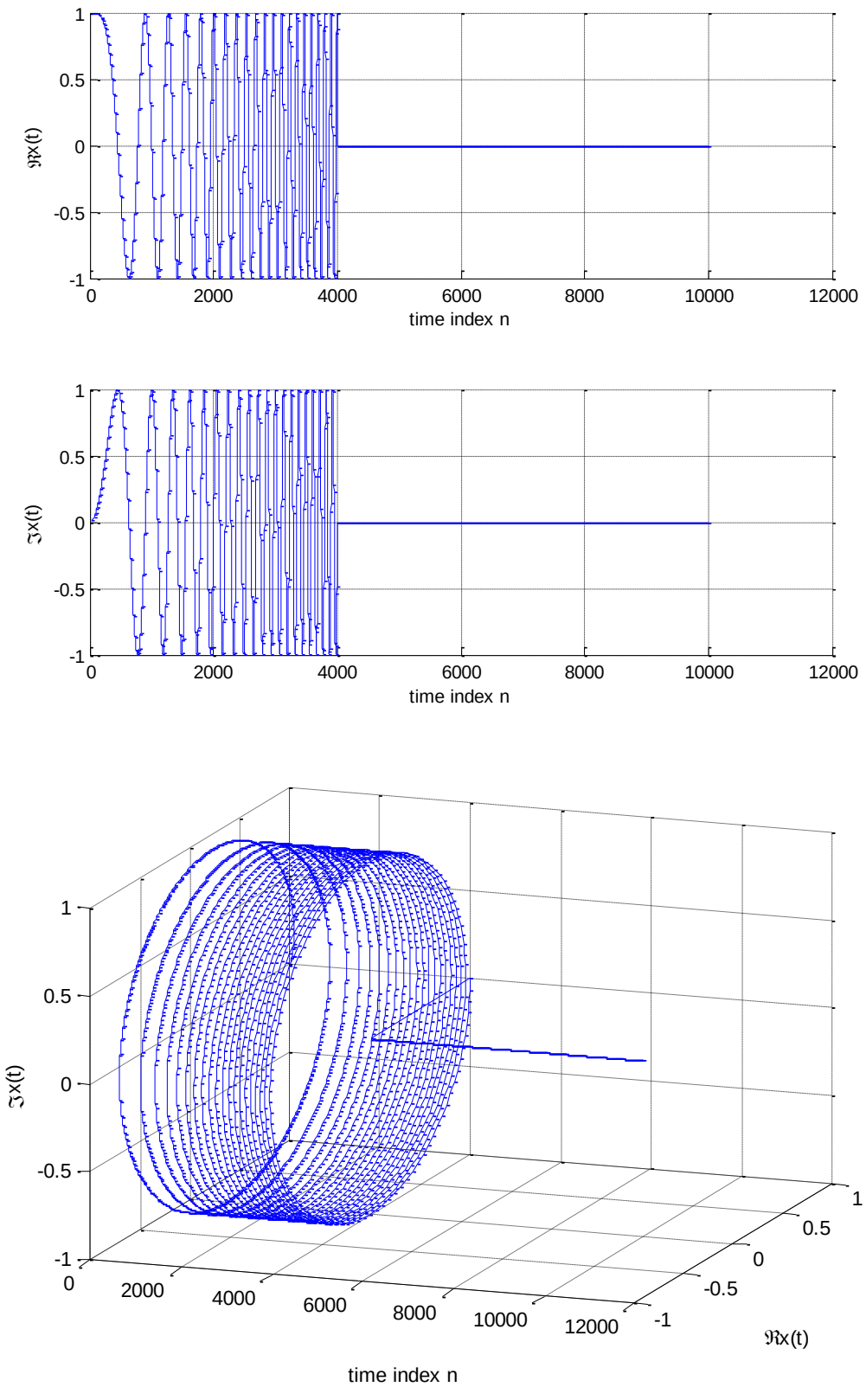


Figure 2-48: The real (a), image (b) and 3D plot (c) of a typical LFM chirp

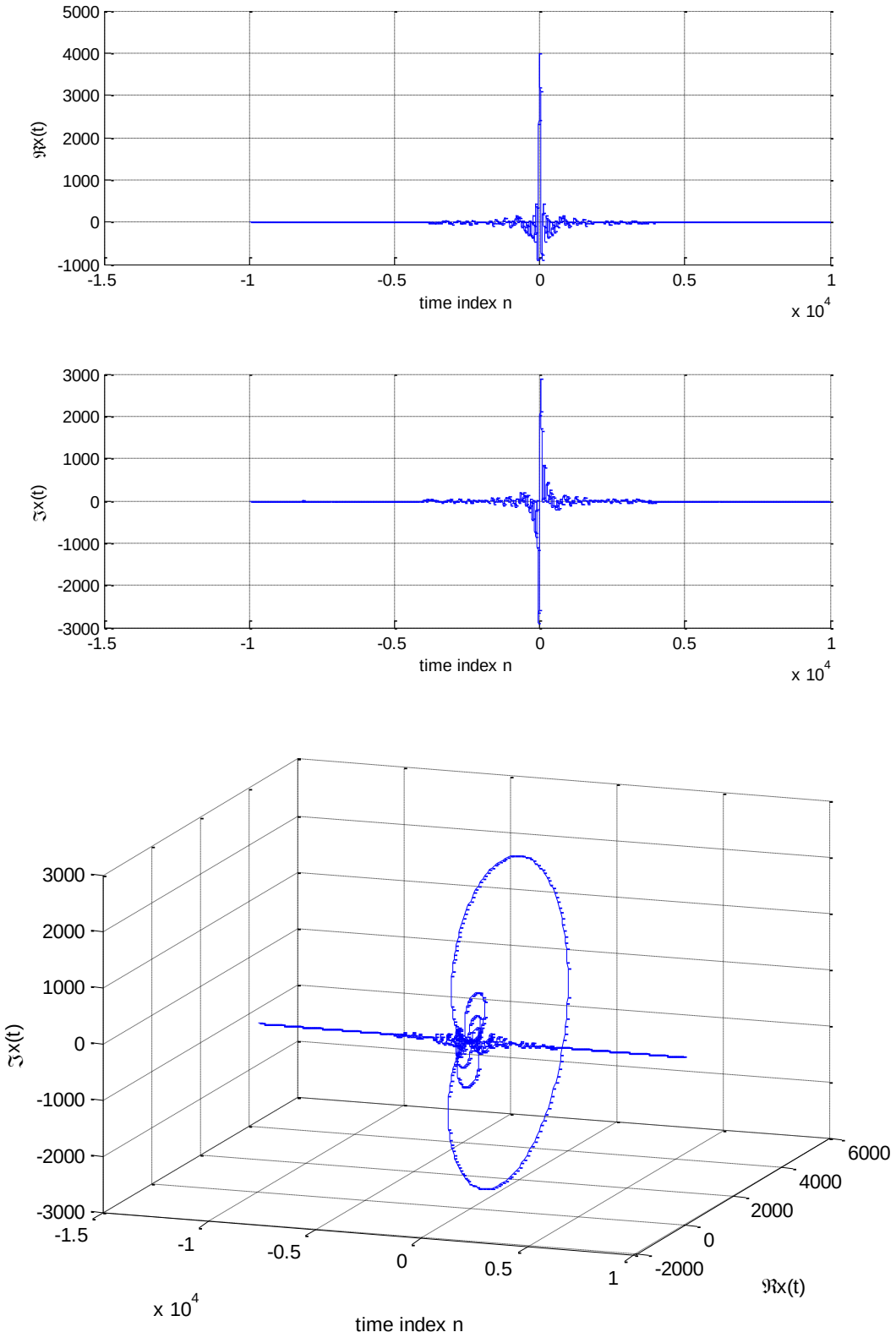


Figure 2-49: The real (a), image (b) and 3D plot (c) of the LFM chirp after passing a matched filter (compressed)

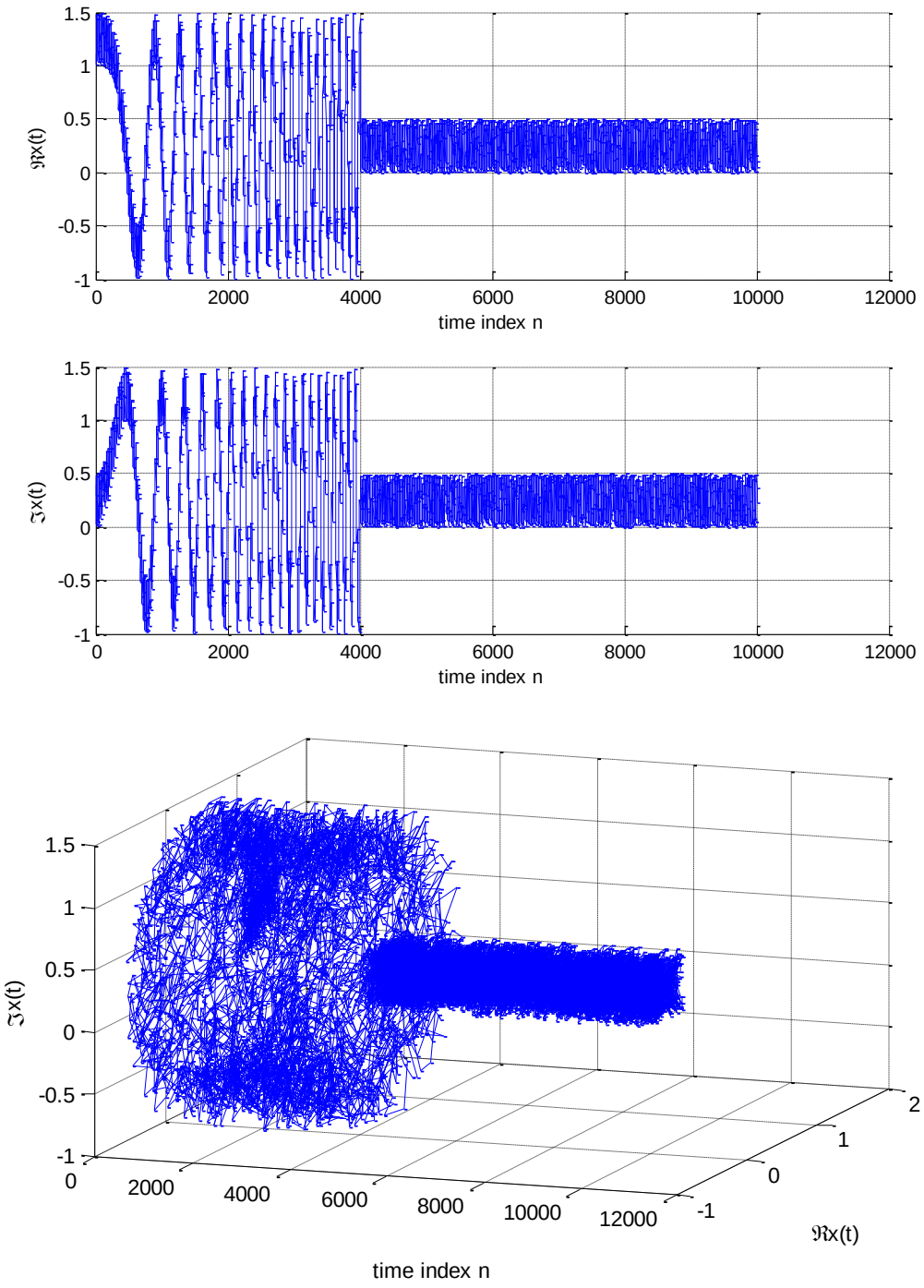


Figure 2-50: The real (a), image (b) and 3D plot (c) of a typical LFM chirp in present of noise (SNR = 6dB)

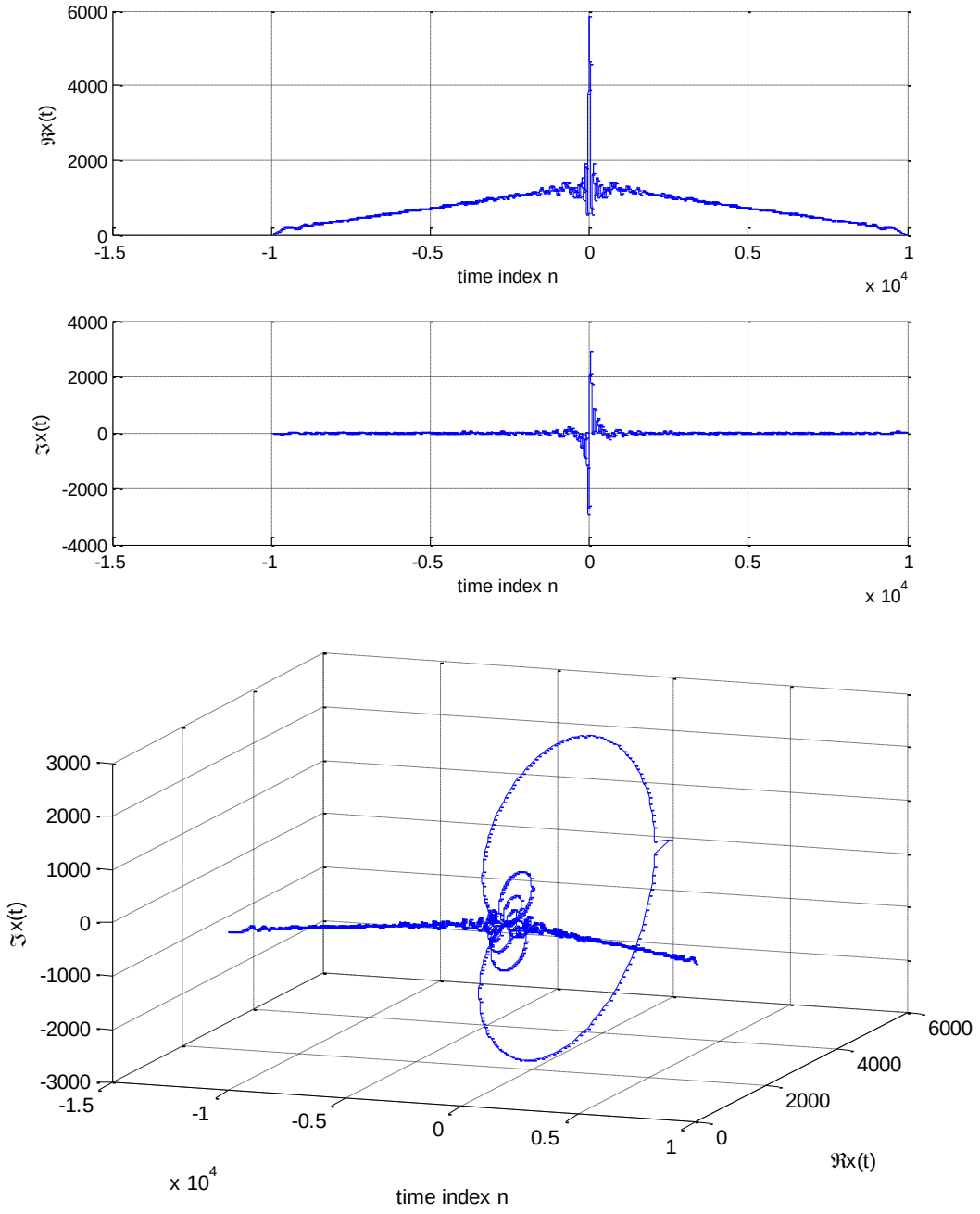


Figure 2-51: The real (a), image (b) and 3D plot (c) of a compressed signal from a LFM chirp with noise (SNR = 6dB)

However, pulse compression has side effects. The most significant side effect is side lobes. Side lobes can be controlled by use of amplitude weighting, i.e. replacement of the constant amplitude A in (2.36) with a suitable weighting function, e.g. Hamming

window. However, the use of a weighting window will result in energy loss, leading to a decrease in the signal-to-noise ratio (SNR) and increase in the main lobe width. A narrower window normally results in less side lobe, but higher main lobe width, as shown in Figure 2-52 and Figure 2-53.

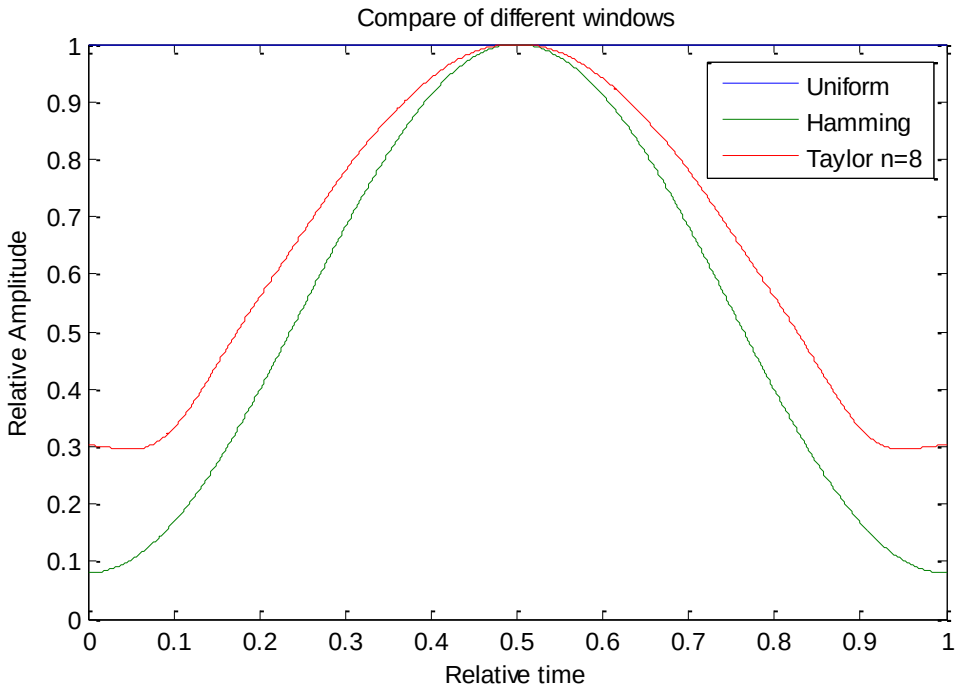


Figure 2-52: The uniform window, Hamming and Taylor window

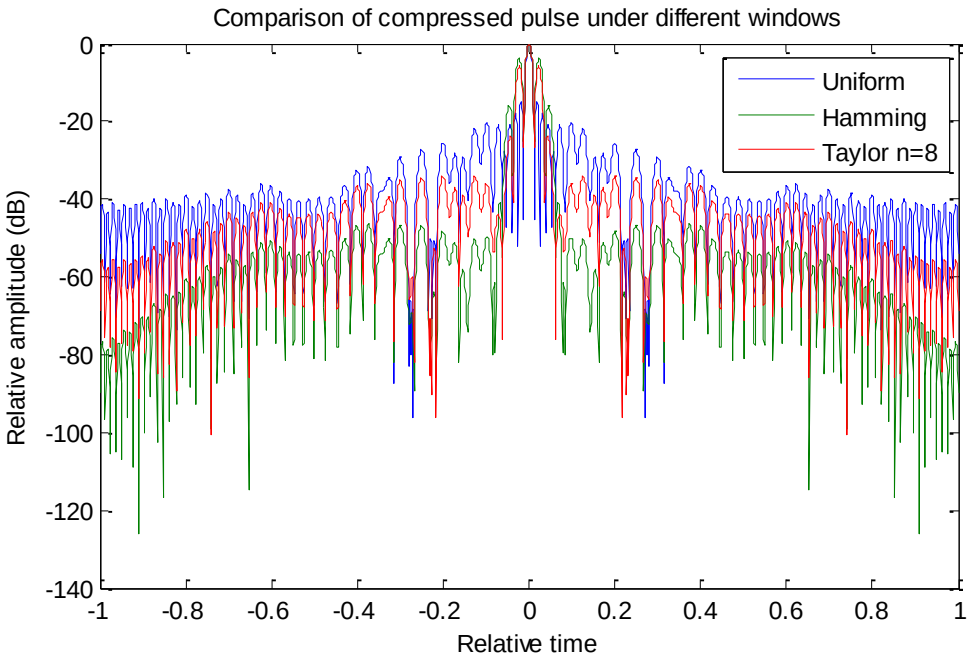


Figure 2-53: The Amplitude of compressed LFM example by different windows

Some popular weighting functions and their key characteristics are listed in the following Table 2-5 [55].

Table 2-5: Key output characteristic of pulse compression by using different window functions

Weighting window	Peak Sidelobe Level (dB)	SNR Loss (dB)	Relative Mainlobe Width
Uniform (rectangular)	-13.2	0	1
$0.33+0.66\cos^2\left(\frac{\pi f}{\beta}\right)$	-25.7	0.55	1.23
$\cos^2\left(\frac{\pi f}{\beta}\right)$	-31.7	1.76	1.65
Taylor (n = 8)	-40	1.14	1.41
Hamming	-42.8	1.34	1.5

2.6.4.3.2 Barker codes

The uncompressed pulse could be modulated such that the phase is altered at 180 degrees (or π radians), and the alternation is relative to a binary phase sequence. This

modulation is known as a binary phase code. Figure 2-54 illustrates a binary phase code of length 7.

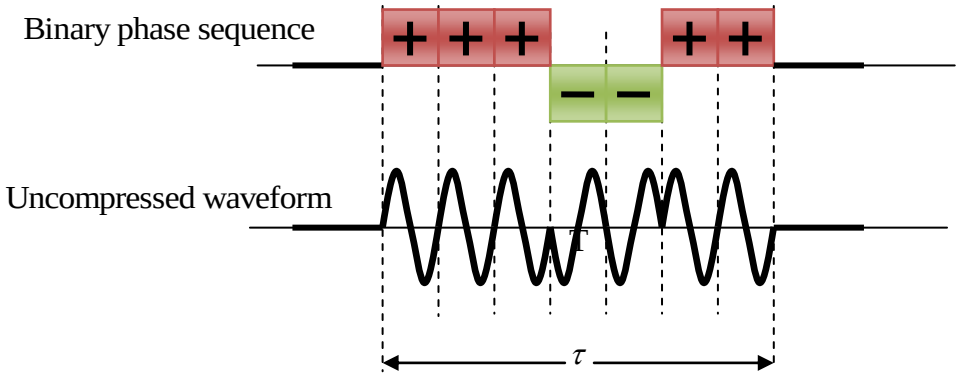


Figure 2-54: An example of binary phase code of length 7

The bandwidth of a binary phase code is the inverse of the sub-pulse duration τ, and the pulse compression ratio is equal to the uncompressed pulse duration T divided by τ. That is:

$$Bandwidth\ B = \frac{1}{\tau}$$

$$PulseCompressionRatio = \frac{T}{\tau}$$

Barker codes are a family of the binary phase coding method that comes with a unique property: the compressed waveform has constant side lobe levels. There are only seven Barker codes, as listed in Table 2-6. Note that the Barker codes of length n will be denoted as B_n [54].

Table 2-6: Barker codes

Code Symbol	Code Length	Binary sequence	Side lobe reduction (dB)
B_2	2	+ - or ++	6.0
B_3	3	+ + -	9.5
B_4	4	+ + - + or + + + -	12.0
B_5	5	+ + + - +	14.0
B_7	7	+ + + - - + -	16.9
B_{11}	11	+ + + - - - + - - + -	20.8
B_{13}	13	+ + + + + - - + + - + - +	22.3

The generation and compression process can be implemented by a suitable tapped delay line (TDL). An example of generation and compression of Barker code of length 7 using TDL is shown in Figure 2-55. A basic rectangular pulse is modulated by passing it though a generation TDL which is in reverse order of the according Barker sequence. The modulated pulse is then transmitted to a channel. An appropriate receiver will pick up the received signals and have them compressed by a matched filter TDL. An ideal waveform of a compressed signal is shown in Figure 2-56. It should be noted that signal shapes other than rectangular pulse may be used to provide better side lobe reduction or larger compression ratio [54], however this is not investigated due to the significat complexity introduced.

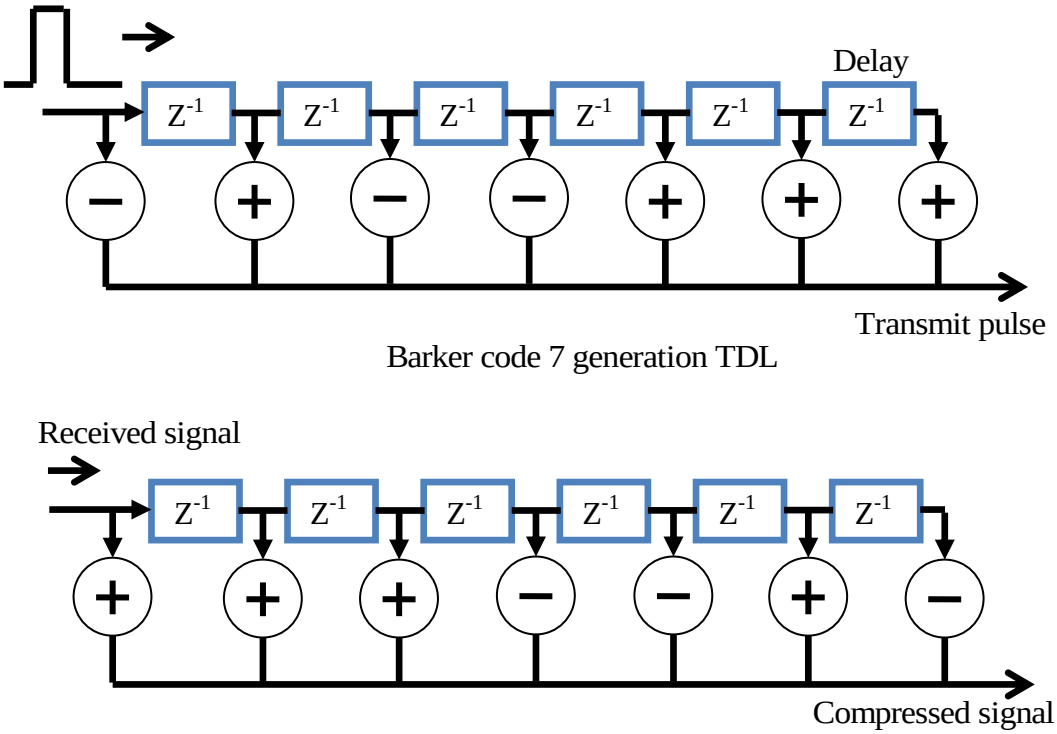


Figure 2-55: Barker code B_7 generation and compression using TDL

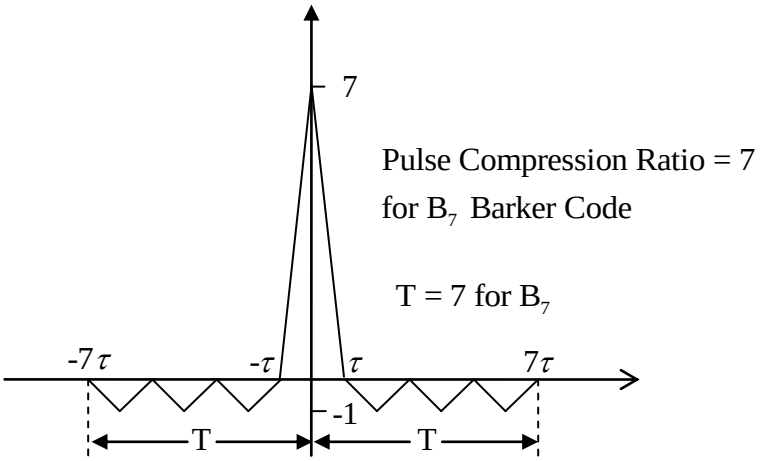


Figure 2-56: Compressed signal encoded by Barker Code B_7

3 Analysis and Characterization of Transient Faults in LVUDN

3.1 Introduction

In practice, a large proportion of the permanent faults in power networks develop from intermittent faults which do not result in a permanent outage. Therefore, the best timing for fault location is when the fault is still in the transient stage, when the fault can be detected but is not so severe as to cause service disruption. A technique to detect and locate transient faults is desired by Distribution Network Operators (DNOs), because this will provide DNOs with valuable time to prepare manual labour, tooling and spares for the particular section of the cable network that requires attention. Unlike persistent or permanent faults however, transient faults may not appear in the first instance, or may not be replicable during the inspection; this will add extra complexity to the fault location process. The characteristics of transient faults and their behaviour in LVUDN are also investigated in this chapter.

3.2 Nature of Transient Faults

As previously described in session 2.4, a transient fault is mainly caused by failure of the main insulation of the cable. Reasons for this may vary, for example: ageing, moisture penetration, high difference in temperature (bad weather), or earthquake. The transient arcing process is normally monitored by measuring the voltage across

and current through the region of transient activity. An important property of arcing activity is that the relationship between voltage and current is not linear [56].

In general, higher current flow will lead to a higher rate of vapour emission from the discharge electrode, and a higher degree of ionization of ambient gas (if arcing in non-vacuum environment). These processes will result in higher current-carrying capability of the discharge channel; the equivalent resistance therefore decreases. In practice, LVUDN are designed to hold a very high current (>50 A), hence transient faults in such cables may be considered as a transient short-circuit.

Transient faults developed in underground cable networks are mainly electrical arcing caused by poor insulation or poor conductor contact. An electrical arc is a plasma channel, induced between conductors within the cable. A plasma channel in a low voltage (LV) power network is considered as self-extinguishing [57], and therefore does not immediately present a hazard. Nevertheless, plasma channels have temperatures of up to 25000 K during arcing; such considerably high temperatures will damage the equipment and eventually cause a permanent fault. In some cases, an arcing fault will result in the occurrence of an explosion in an underground cable network duct.

Self-extinguishing of arcs in the LV network is due to either low driving voltage, or post-arc column deionization phenomenon within the insulation decomposition gases. One investigation has revealed that such faults may be sustained for some time, or periodically reignite for minutes; significant heat and gases were generated thereafter [58]. These gases could obviously be a hazard if accumulated with air to the minimum explosive concentration in ducts.

However, although weak arcing failures do self-extinguish in many cases, the cumulative damage caused by repeated transient faults would eventually cause extensive damage to the cable, or to accessories nearby the fault point.

Koch et al. addressed the mechanism of arcing faults on low-voltage cables in ducts [59]. Transient faults normally begin with either a phase-to-neutral arc or phase-to-ground arc. In a wet environment, moisture infiltrates into gaps or cracks in deteriorated insulation between conductors. The moisture will conduct under a certain voltage, leading to liquid breakdown via the formation of a plasma channel which immediately develops into a full-current arcing fault. This process turns electrical energy into heat energy in a limited space around the arcing position. If the arcing fault persists, the large amount of heat energy generated will result in worse degradation of the cable insulation and evaporation of conductor material. Even though erosion (oxidation) of the conductor and creation of insulation decomposition gases will prevent or even stop arcing, adjacent insulation materials still suffer thermal degradation due to the heat, and this may cause the arc to reignite in the form of gas breakdown or surface discharge. The fault may be shown as intermittent arcing spots separated by a comparatively long time, whereas accumulated damage to the cable may lead to a phase-to-phase discharge and result in a permanent three-phase fault. Thus, an effective protection system or fault location method for underground cables should possess the capability to address the interrupted character of transient faults.

3.2.1 Transient activity detection methods

3.2.1.1 Time domain analysis

Time domain analysis is a way to examine voltage and current waveforms in the time domain. Lee utilized the ratio of zero-sequence and positive-sequence current characteristics to detect arcing [60], while Sultan used the half-cycle current asymmetry characteristic to address this issue [61]. Benner detected arcing by analysing randomness in the behaviour of the arcing current [62].

Typically, instantaneous phase or line current is analysed, in order to monitor the peak current caused by an arcing fault. This current has the shape of a spike with a huge magnitude compared with the magnitude of the current under normal load. However, the spike only lasts for a very short time. Additionally, under normal working conditions, e.g. a large power inductive motor being switched off, the shape of the spike also appears in the phase current waveforms.

3.2.1.2 Frequency domain analysis

For the frequency domain, phase current waveform harmonic analysis is a way to detect arcing [63, 64]. The crest factor can also be utilised to evaluate waveform distortion [65].

The harmonic components of the phase and neutral currents during arcing failure are different from those under normal conditions. Therefore, frequency domain analysis attempts to identify arcing faults by comparing harmonic contents. Harmonic contents of waveforms are derived from time domain signals by using fast Fourier transforms (FFT). To calculate the FFT, a length of time domain data must be recorded and the frequency components will be based on this length of time. Charytoniuk described the following harmonic component changes as being indicative of an arcing fault [57]:

- DC component appearing in phase currents;
- Level of second harmonic increases sharply in phase current and neutral currents.

3.2.1.3 Time-frequency domain analysis

The time–frequency method detects the fault by interpreting transient arcing behaviour in both the time and frequency domain via the use of wavelet transforms [66].

The purpose of time-frequency analysis is to examine frequency behaviour changes over time. Bruce introduced a method of wavelet transformation that decomposes the input signal into a set of components [67]. By detecting the transient components that summed to the normal current, an arcing fault could be identified.

The analysis started with division of the transient signals into some components of a wavelet transformation. The transient detection capability depends on the type of wavelet family, order of the wavelet, and robustness of decomposition.

3.2.2 Transient fault identification in LVUDN

To identify the transient fault in LVUDN, a problem that requires attention is the discriminability of transient faults from switch loads. Modern switching-mode power supplies (SMPS) will generate a switching noise similar to transient faults. The online fault monitor must be able to cope with such noise, as filters will also remove the signal generated by transient faults.

Examples of transient faults in the LVUDN are shown in Figure 3-1 and Figure 3-2. A typical transient normally will not continuously last for one cycle since the arc extinguishes around the zero crossing point.

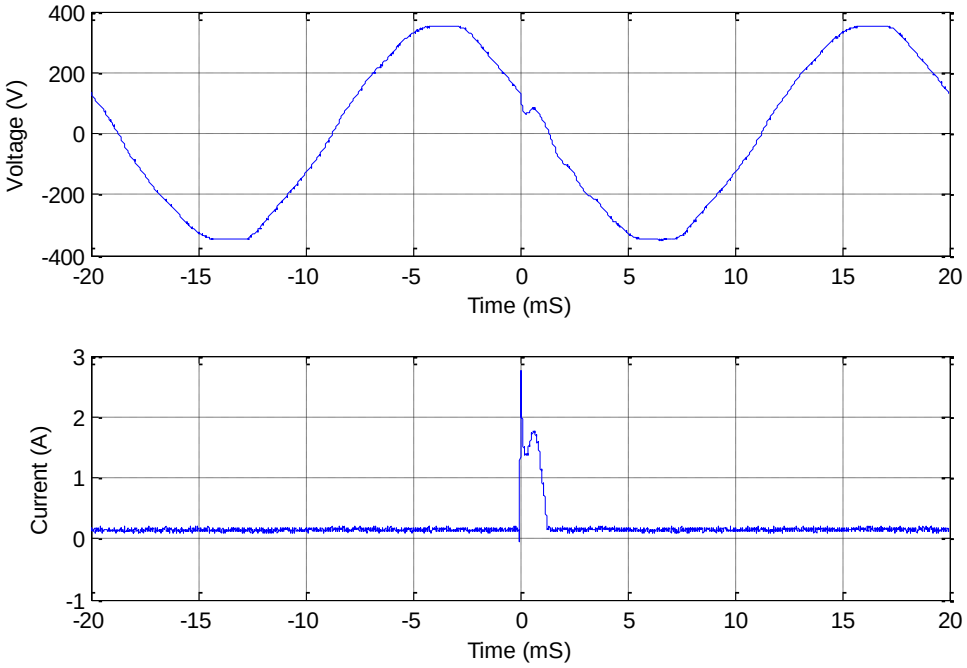


Figure 3-1: A short transient activity captured in real power cable

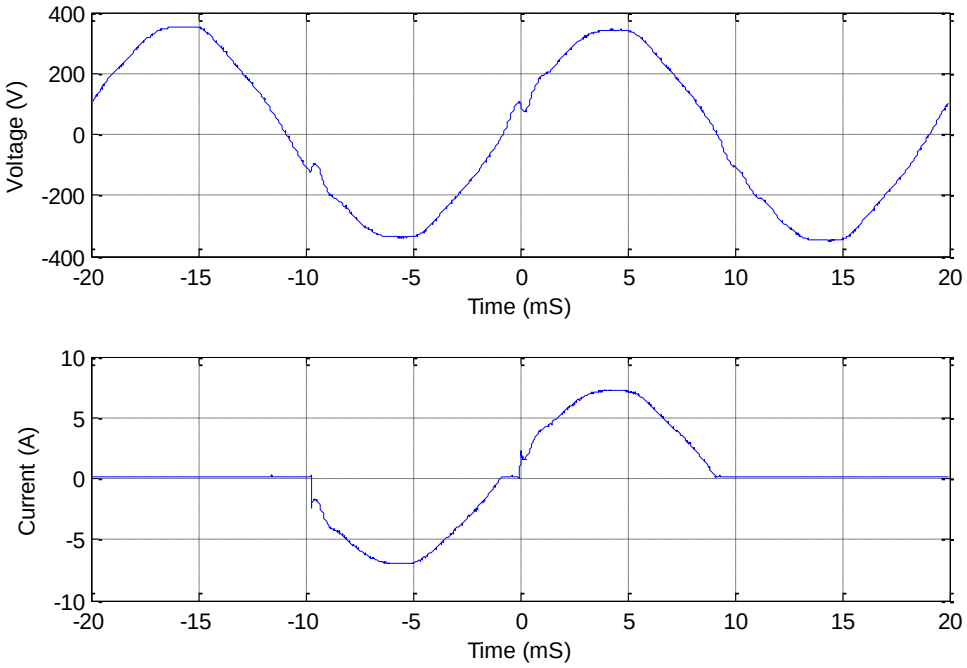


Figure 3-2: A longer transient activity captured in real power cable

3.3 Power Cable High Frequency Characteristic Study

In this section, a number of real power cables were tested to provide a better understanding of the cable characteristics under high frequency (RF) signals. Unlike coaxial signal cables, most power cables are only designed for low frequency (50-60 Hz) energy transfer, and therefore the high frequency performance is un-clarified. However, understanding of the high frequency characteristics of power cables is highly desirable in development of a fault locating technique using high frequency TDR interrogation signals.

The high frequency power cable impedance was measured by two different methods, namely: the I/V method; and the transmission/reflection method. The results of both methods will be compared and discussed. High frequency transmission losses (attenuation) were measured using an S-parameter toolkit, accurate up to 500 MHz. Additionally, a range of TDR tests were performed under different cable network configurations, to investigate the relationship between reflection and cable characteristics.

The HP/Agilent 4395A spectrum analyser supports instrument BASIC (iBASIC), which significantly eases the measurement procedure. An automatic measurement program, available to view in Appendix 9.1, was used to measure cable characteristics using the I/V method (HP 43961A test kit). The measurements utilising the transmission/reflection method were performed together with the author's colleague, Faisal Peer Mohamed.

3.3.1 Cable profile

Three types of underground power cable were tested. These cables were commonly used in underground power networks in Scotland.

3.3.1.1 Paper Insulated Corrugated Aluminium Sheath (PICAS) CABLE

Paper-insulated corrugated aluminium sheath (PICAS) cable was the standard circuit cable of ScottishPower on the power network. It became obsolete from October 2003, and replaced by 3-core XLPE cable. The PICAS cables utilised in the tests were manufactured in 2004, in the length of 65.3 meters.

Cable Construction

A. Aluminium conductor - 3× stranded sector shaped
B. Layers of paper insulation impregnated with mineral oil compound, thickness 3.4 mm between conductor and sheath
C. Corrugated Aluminium sheath (bitumen coated)
D. Red PVC oversheath

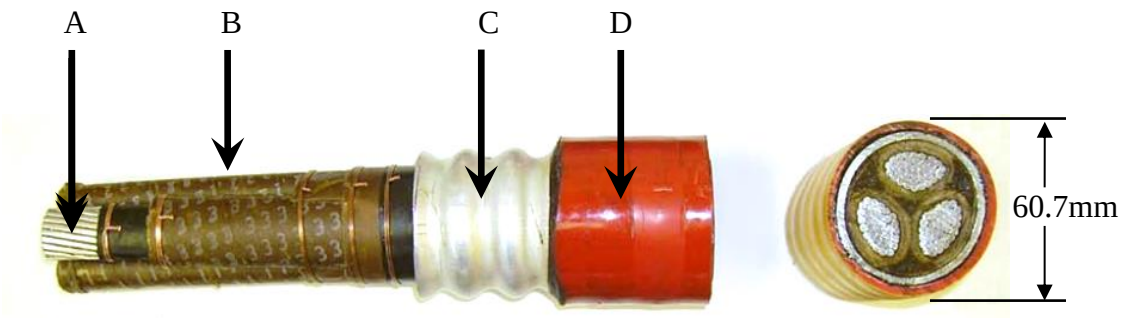


Figure 3-3: Structure of ScottishPower PICAS Cable

3.3.1.2 Cross Linked Polyethylene (XLPE) CABLE

At the time of writing this thesis, the three-core XLPE cable is still one of the standard underground power cables on the network of ScottishPower. This cable is

also used to terminate overhead line poles. The XLPE cables involved in the test were manufactured in 2010, in the length of 24.0 meters.

Cable Construction

A. Aluminium conductors – 3 x 185 mm solid round
B. XLPE insulation – thickness 3.4 mm on each core
C. Copper wire earth screen
D. Red MDPE oversheath

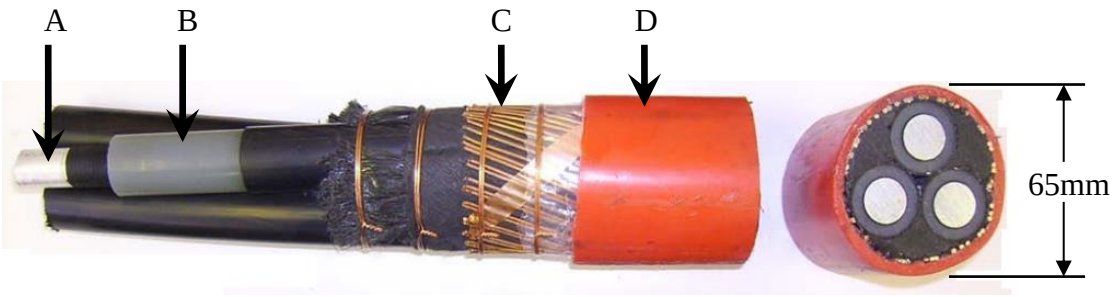


Figure 3-4: Structure of ScottishPower XLPE Cable

3.3.1.3 3-Core Waveform Combined Neutral Earth (CNE) Mains Cable

The waveform combined neutral earth (CNE) cable is the present standard low voltage cable used by ScottishPower. If examining the cross-section along the cable length, the neutral/earth wires (D in Figure 3-5) in the cable are in similar shape as a wave formation, hence the term "waveform". The 3-core waveform CNE cables involved in the test were mainly manufactured in 2008, in various lengths.

Cable Construction

A. Aluminium conductor - 3 × solid sector shaped
B. XLPE insulation, thickness = 1.6 mm for 185 mm^2 conductors. Live cores coloured: Brown, Black, Grey as per CENELEC[‡].
C. Rubber bedding layer

[‡] European Committee for Electrotechnical Standardization, http://www.cenelec.eu/

D. Copper neutral / earth wires

E. PVC oversheath

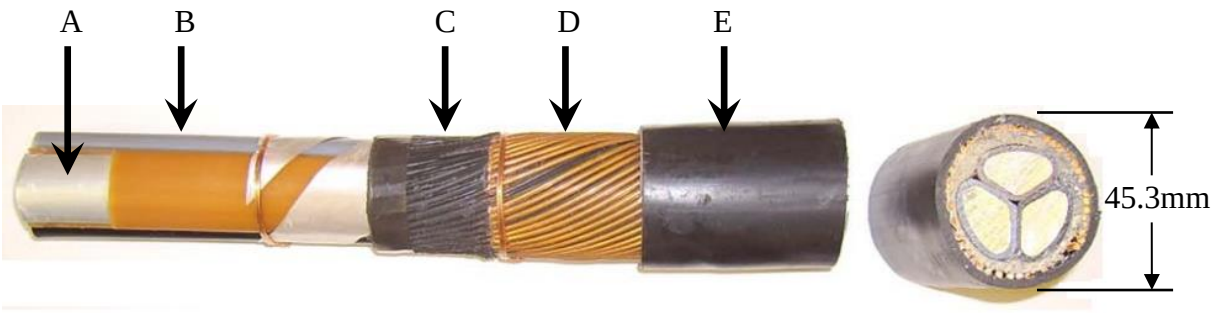


Figure 3-5: Structure of ScottishPower LV Waveform CNE Cable

3.3.2 High Frequency Impedance of Power Cables

3.3.2.1 V/I Method

The impedance measurement results by the V/I method for the 3 different types of cable are shown in Figures 3.6-3.11, as summarised in Table 3-1. The measurement results show that there is a slight difference between the phase-to-phase and phase-to-neutral results, because of the different electrical structure. The phase plots also suggest that these cables are inductive for low frequency signals up to around 150 MHz, and become capacitive for higher frequencies.

Table 3-1: List of impedance measurement plots by using V/I method

Cable Type	Phase to Phase	Phase to Neutral
185 mm^2 Waveform CNE	Figure 3-6	Figure 3-7
185 mm^2 PICAS	Figure 3-8	Figure 3-9
185 mm^2 XLPE	Figure 3-10	Figure 3-11

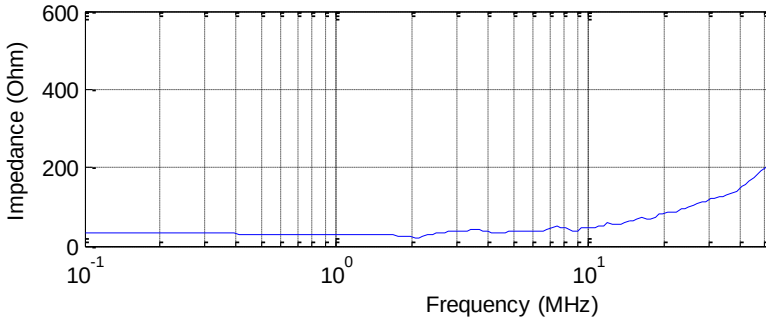


Figure 3-6: Impedance vs. Frequency between phase-to-phase conductors of 185mm^2 Waveform CNE cable

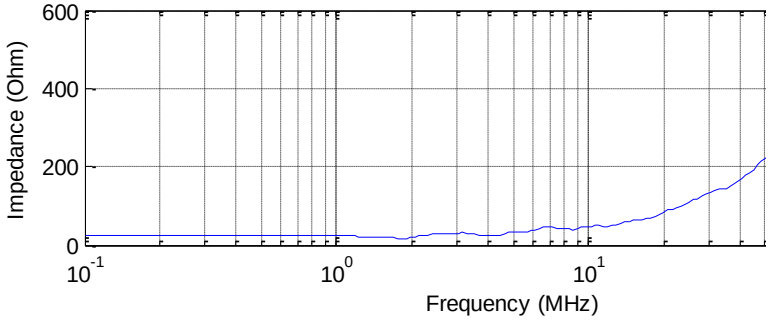


Figure 3-7: Impedance vs. Frequency between phase-to-neutral conductors of 185mm^2 Waveform CNE cable

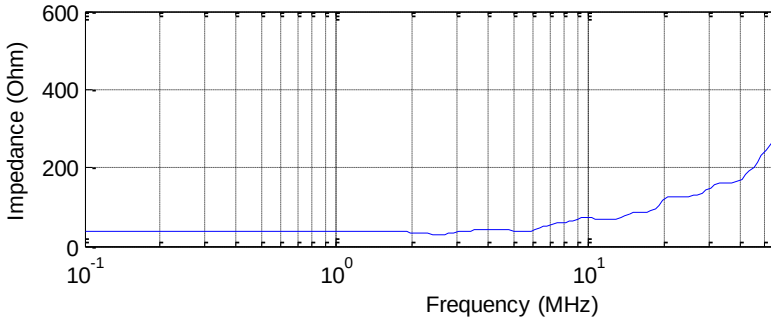


Figure 3-8: Impedance vs. Frequency between phase-to-phase conductors of 185mm^2 PICAS cable

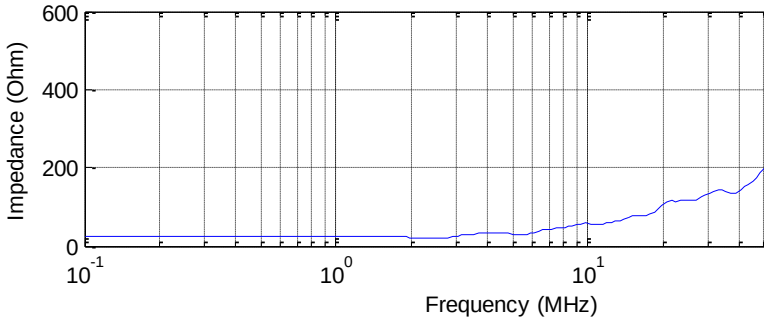


Figure 3-9: Impedance vs. Frequency between phase-to-neutral conductors of 185mm^2 PICAS cable

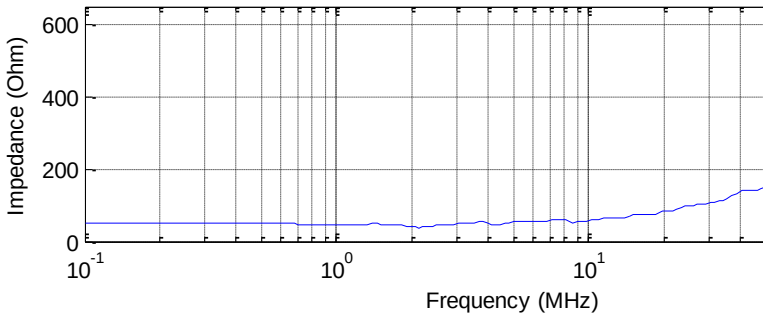


Figure 3-10: Impedance vs. Frequency between phase-to-phase conductors of 185mm^2 XLPE cable

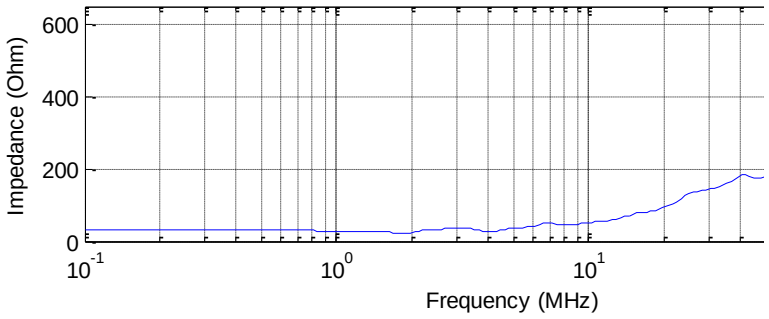


Figure 3-11: Impedance vs. Frequency between phase-to-neutral conductors of 185mm^2 XLPE cable

3.3.3 High Frequency Attenuation of Power Cables

Cable attenuation at high frequencies was also tested. Generally, the attenuation is represented using the units dB/100 feet or dB/10 m. The attenuation is therefore a length multiplier. For example, a 50 MHz signal in a 10-m-long, 185 mm^2 waveform CNE cable is attenuated by −7dB, as shown in Figure 3-12, so the attenuation for this signal in 20 m length cable would have twice the loss shown above, that is -14 dB.

The attenuation plots are listed in Table 3-2.

The results show increasing attenuation attribute for power cables up to the corner frequency, from which the cable appears to become capacitive and hence result in low attenuation at higher frequencies.

Table 3-2: List of attenuation plots

Cable Type	Phase to Phase	Phase to Neutral
185 mm^2 Waveform CNE	Figure 3-12	Figure 3-13
185 mm^2 PICAS	Figure 3-14	Figure 3-15
185 mm^2 XLPE	Figure 3-16	Figure 3-17

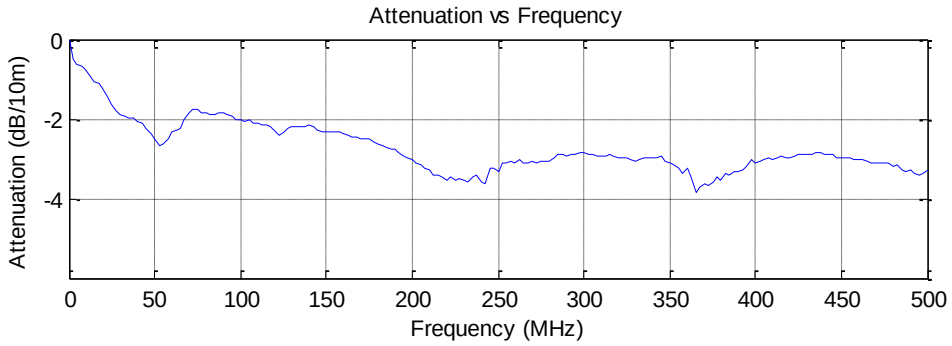


Figure 3-12: Attenuation vs. Frequency between phase-to-phase conductors of 185mm^2 Waveform CNE cable

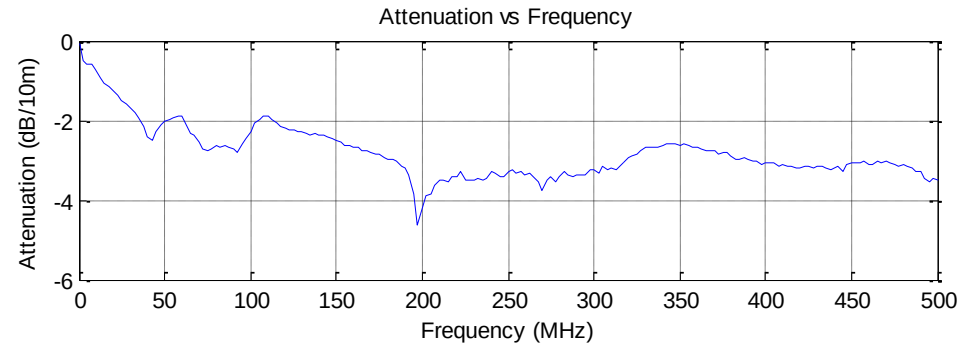


Figure 3-13: Attenuation vs. Frequency between phase-to-neutral conductors of 185mm^2 Waveform CNE cable

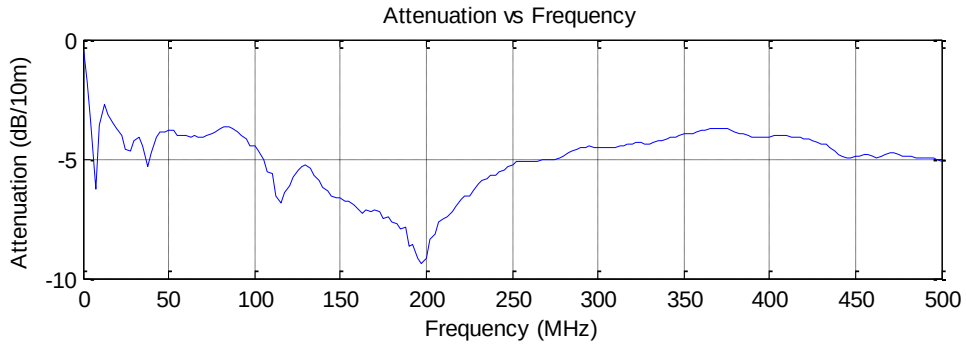


Figure 3-14: Attenuation vs. Frequency between phase-to-phase conductors of 185mm^2 PICAS cable

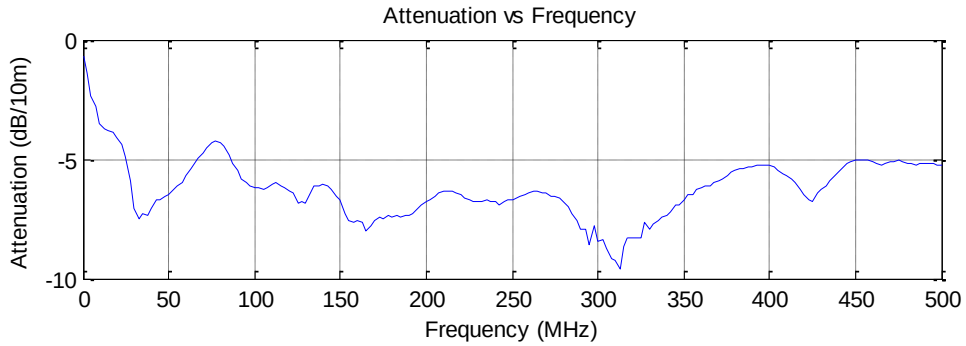


Figure 3-15: Attenuation vs. Frequency between phase-to-neutral conductors of 185mm^2 PICAS cable

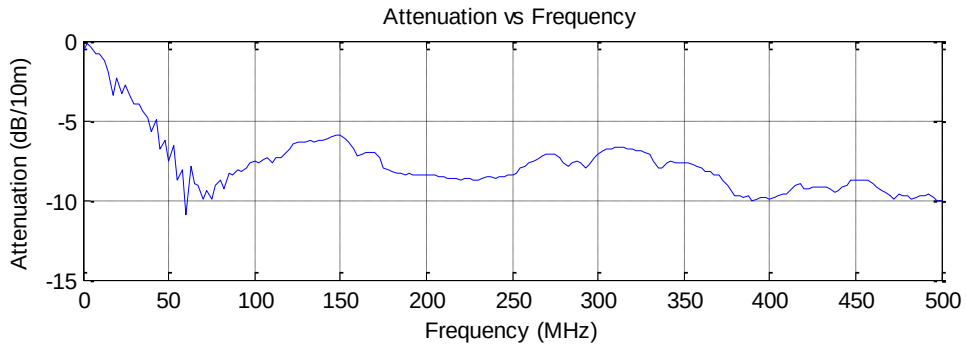


Figure 3-16: Attenuation vs. Frequency between phase-to-phase conductors of 185mm^2 XLPE cable

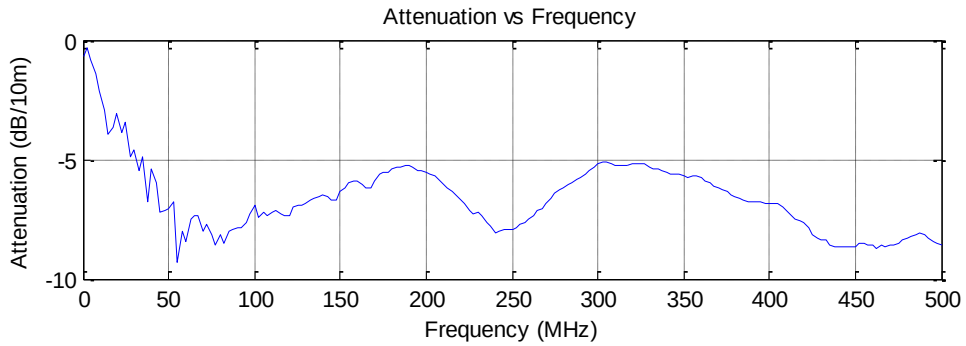


Figure 3-17: Attenuation vs. Frequency between phase-to-neutral conductors of 185mm^2 XLPE cable

3.3.4 TDR Test

The use of TDR in real LVUDN power cables is also studied in order to further explore the characteristics of power cables. Three cable networks were constructed to simulate 3 different scenarios. The cable networks were all based on the 185 mm^2 waveform CNE cable described in section 3.3.1.3.

As illustrated in Figure 3-18, a signal generator is connected to the cable network under test through a high frequency current probe. One input of the oscilloscope is

connected to the current probe while another input is directly connected to the output of the current probe.

The signal generator is a 14-bit, 50 MHz arbitrary waveform generator G5100A, made by Picotest. The oscilloscope is a MSO2024 model, by Tektronix. The high frequency current probe is custom-made by the author, with 0.1 Ohm internal impedance, 50 A maximum input/output current, 10 A/V gain, and 103 MHz output bandwidth (-3dB).

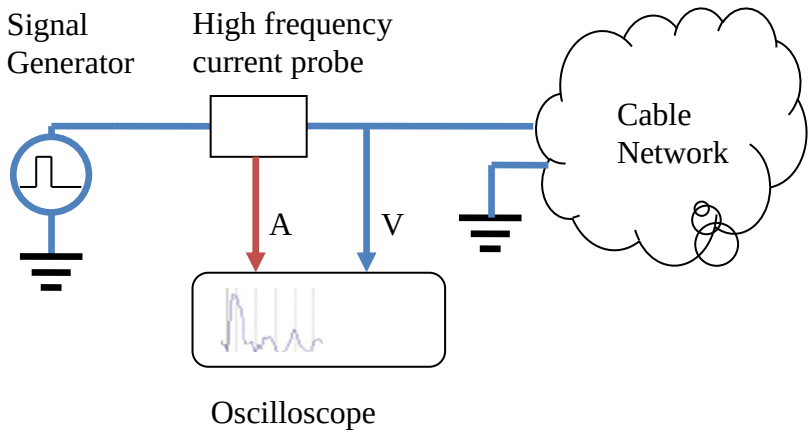


Figure 3-18: Schematic of TDR test

Three scenarios were created for the TDR test. Scenario 1 is made by a simple section of cable. Scenario 2 is three cables with different length jointed together to simulate s T-joint. Scenario 3 is representing a complex LVUDN.

3.3.4.1 Scenario 1: Simplest Cable Network

Figure 3-19: Schematic of Scenario 1.

Scenario 1 is the simplest cable network with only a 100 m single cable, as seen in Figure 3-19. The test equipment was connected to one pair of conductors at one end of the cable (near end). The according conductor pair at the other end (far end) is either left open or shorted by a short jump wire (VF=0.57).

The time taken for a signal travel from one end of the cable to the other is:

$$T = \frac{l}{v} = \frac{100m}{0.57c} = 585 \times 10^{-9} s = 585ns$$

Therefore the tests in this scenario have been separated into 3 different pulse lengths:

- 500 ns (pulse length shorter than pulse return time 2T)
- 1000 ns (pulse length approximate 2T)
- 5 µs (pulse length is longer than 2T)

3.3.4.1.1 Case 1: TDR using pulse length of 500ns, Far end open circuit (O/C) and short circuit (S/C).

Figure 3-20 shows the voltage (a) and current (b) reflection waveform for two different loads.

It can be seen from the voltage waveform that a high impedance load (open circuit) generates a positive reflection, whilst the low impedance load (short circuit) results in a negative reflection. The result perfectly matches the transmission line theory in Chapter 2.

By multiplying the voltage by current, the transient power at a certain time is presented in Figure 3-21. Note that the negative section of the current waveform indicates that current is being transmitted into the test equipment. Similarly, the negative section in the power waveform indicates that the direction of power-flow is towards the test equipment. From the transient power plot it can be seen that nearly

the same power is reflected in the two extreme cases of load, namely: open circuit ($\Gamma_L = 1$); and short circuit ($\Gamma_L = -1$).

Since the transmitted and reflected pulses are clearly separated, the energy content can be calculated by taking the time integral of the transient power, as shown in Figure 3-22. The results are displayed in Table 3-3.

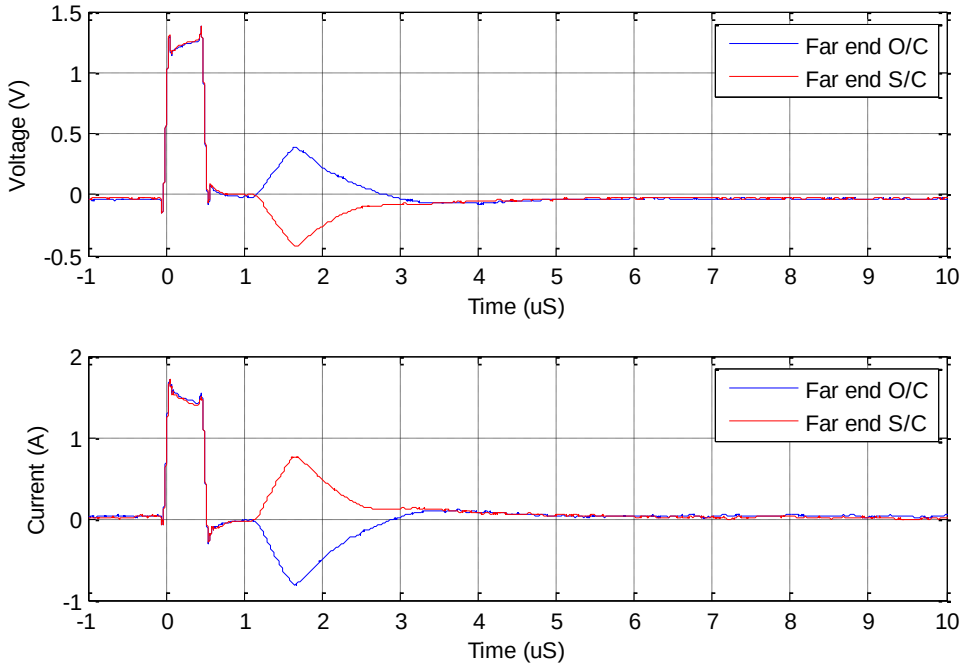


Figure 3-20: Voltage (a) and current (b) reflection waveform of 500ns pulse in 100m cable, Case 1, Scenario 1.

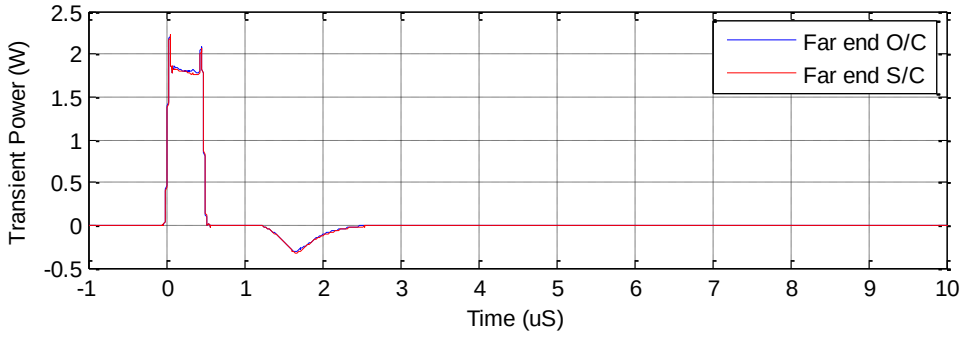


Figure 3-21: Transient Power of Case 1, Scenario 1.

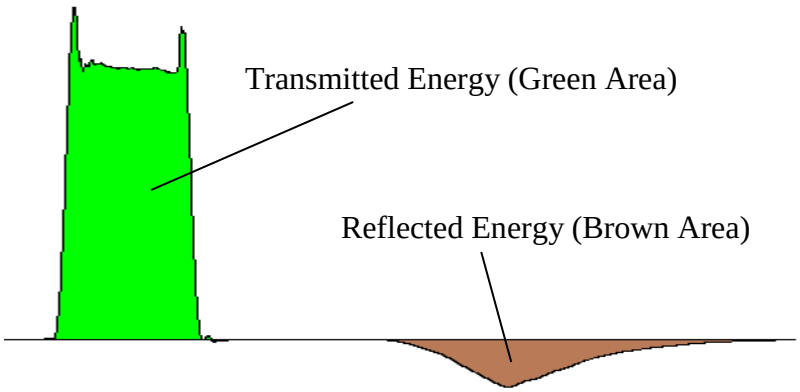


Figure 3-22: Illustration of transmitted energy calculation

Table 3-3: Transmission and reflection energy of Case 1, Scenario 1.

Item	Far end O/C	Far end S/C
Transmitted Energy (uWh)	0.8818	0.8723
Reflected Energy (uWh)	0.1699	0.1847
Energy Loss:	80.7%	78.8%

3.3.4.1.2 Case 2: TDR using pulse length increased to 1000ns, Far end open circuit (O/C) and short circuit (S/C).

Similar tests were repeated in Case 2. The pulse length in this case is extended to 1000 ns. Figure 3-23 displays the voltage (a) and the current (b) reflection waveform for both O/C and S/C. The transient power is shown in Figure 3-24. As the power of the interrogation and reflection pulses is still clearly distinguishable, the transmitted and reflected energy is listed in Table 3-4.

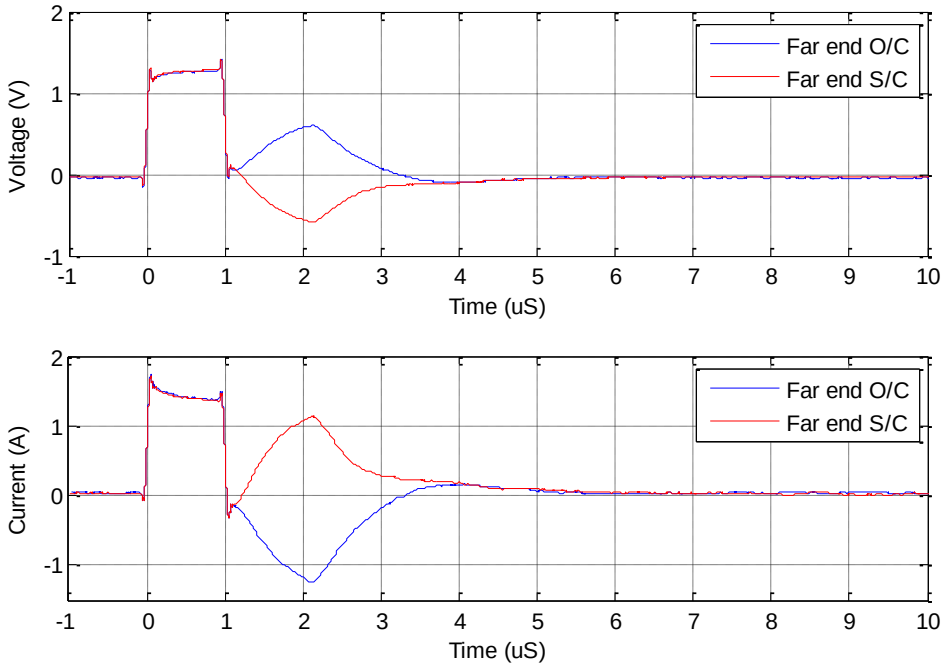


Figure 3-23: Voltage (a) and current (b) reflection waveform of 1000ns pulse in 100m cable, Case 2, Scenario 1.

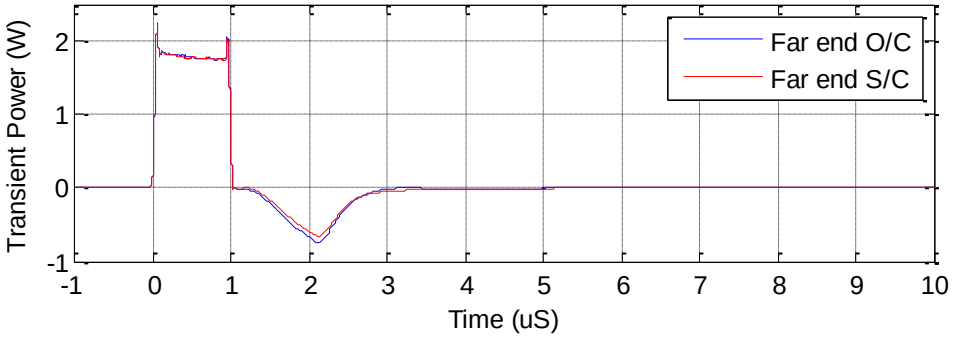


Figure 3-24: Transient Power of Case 2, Scenario 1.

Table 3-4: Transmission and reflection energy of Case 2, Scenario 1.

Item	Far end O/C	Far end S/C
Transmitted Energy (uWh)	1.7648	1.7594
Reflected Energy (uWh)	0.5791	0.5233
Energy Loss:	67.2%	70.3%

3.3.4.1.3 Case 3: TDR using pulse length increased to 5us, Far end open circuit (O/C) and short circuit (S/C)

In Case 3, the pulse length is adjusted to 5 us. As the transmitted and reflected pulse is overlapped (Figure 3-25), the transient power and energy are not calculated.

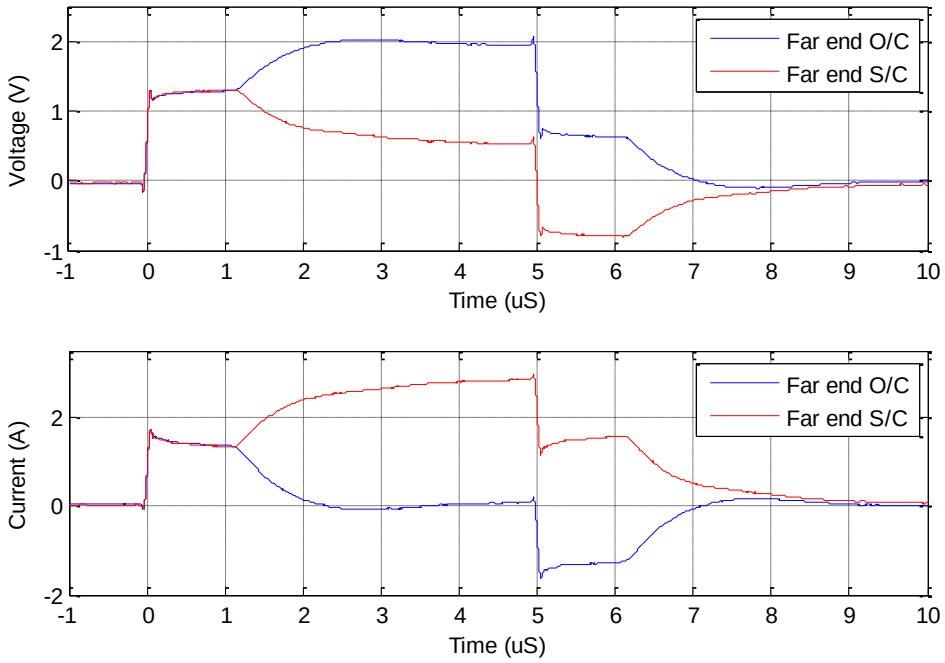


Figure 3-25: Voltage (a) and current (b) reflection waveform of 1000ns pulse in 100m cable, Case 3, Scenario 1.

3.3.4.1.4 Discussion of Scenario 1

In this case, the simplest example for the use of TDR in LVUDN is demonstrated. As described in Chapter 2, the TDR technique uses "edges" to detect the change of impedance. In an ideal lossless cable, the reflection should be in exactly the same shape as the incident (transmitted) pulse. However, the sharp edges in the incident pulse are "smoothed" into a slope in the reflected pulse due to cable attenuation and distortion. This is unwanted in TDR cable fault locating systems. By comparing Table 3-3 and Table 3-4, it can be seen that the transmitted energy is proportional to the length of the interrogation pulse; the longer the pulse width, the higher the energy content. It can also be seen that the reflected energy is mainly due to the degree of

change, and not the direction of change. In other words, the reflected energies are nearly the same for either the cable impedance increased to maximum (infinity, open circuit), or the cable impedance decreased to minimum (zero, short circuit). The reflection loss for 500 ns pulse width in case 1 was around 80%, and this decreased to about 70% for 1000 ns pulse width in case 2. This further suggests that the underground cable is not designed for high frequencies, and suffers from higher attenuation at higher frequencies. Case 3 shows that although a more complex reflected waveform results, it is possible to use longer incident pulse width to detect a cable fault.

3.3.4.2 Scenario 2: Cable Network with T-Joint

Scenario 2 introduces the T-joint for TDR testing, as shown in Figure 3-26. Both far ends are left opened. Three different pulse widths: 500 ns, 1000 ns, and 5 us, are used for the interrogation pulse, creating 3 cases. The time axis (x-axis) is translated to distance by performing the conversion from time (t) to distance (D):

$$D(m) = t(s) \times \frac{v}{2} = t \times \frac{c \times VF}{2} \tag{3.0}$$

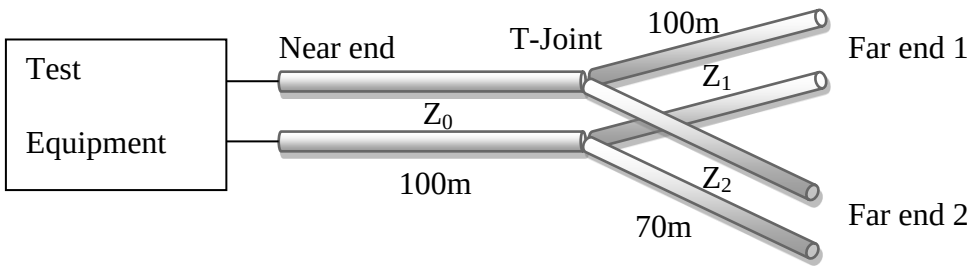


Figure 3-26: Schematic of Scenario 2

3.3.4.2.1 Case 1: TDR using pulse length 500nS, 2 far ends all open circuit (O/C)

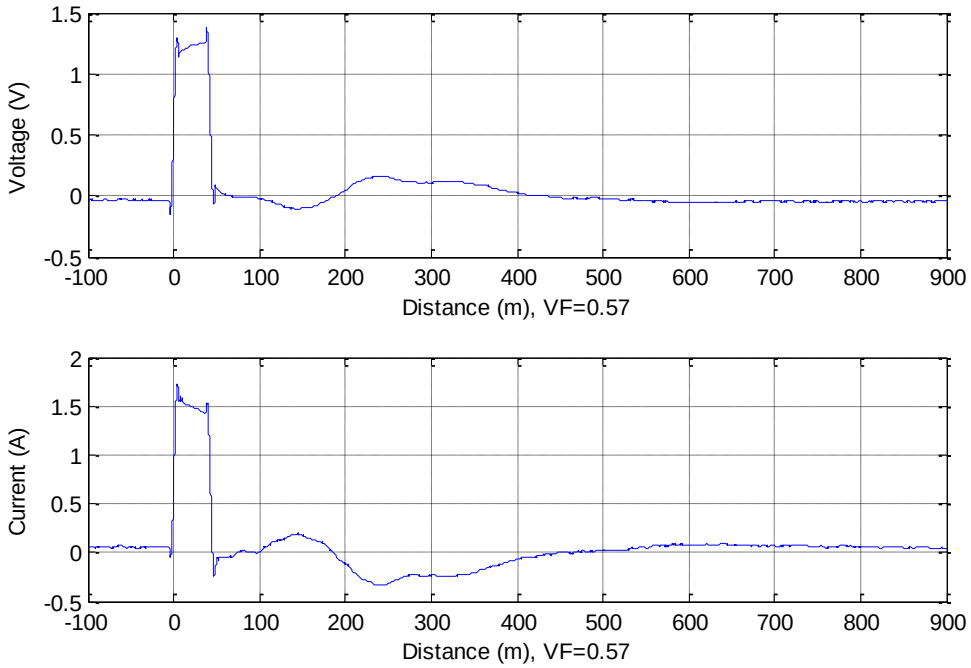


Figure 3-27: Voltage (a) and current (b) reflection waveform of 500ns pulse in 100m cable with T-joint, Case 1, Scenario 2.

3.3.4.2.2 Case 2: TDR using pulse length 1000nS, 2 far ends all open circuit (O/C)

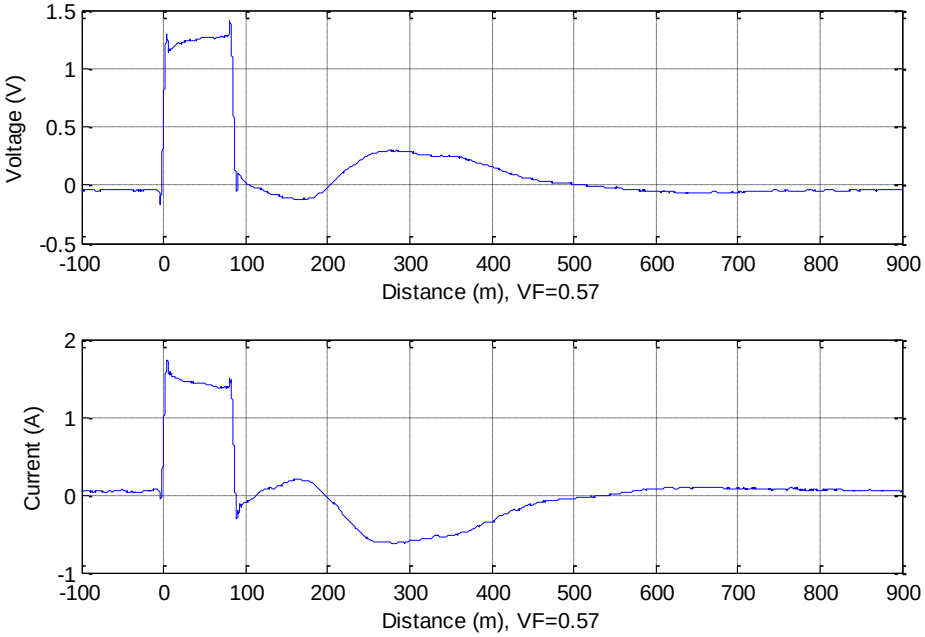


Figure 3-28: Voltage (a) and current (b) reflection waveform of 1000ns pulse in 100m cable with T-joint, Case 2, Scenario 2.

3.3.4.2.3 Case 3: TDR using pulse length 5uS, 2 far ends all open circuit (O/C)

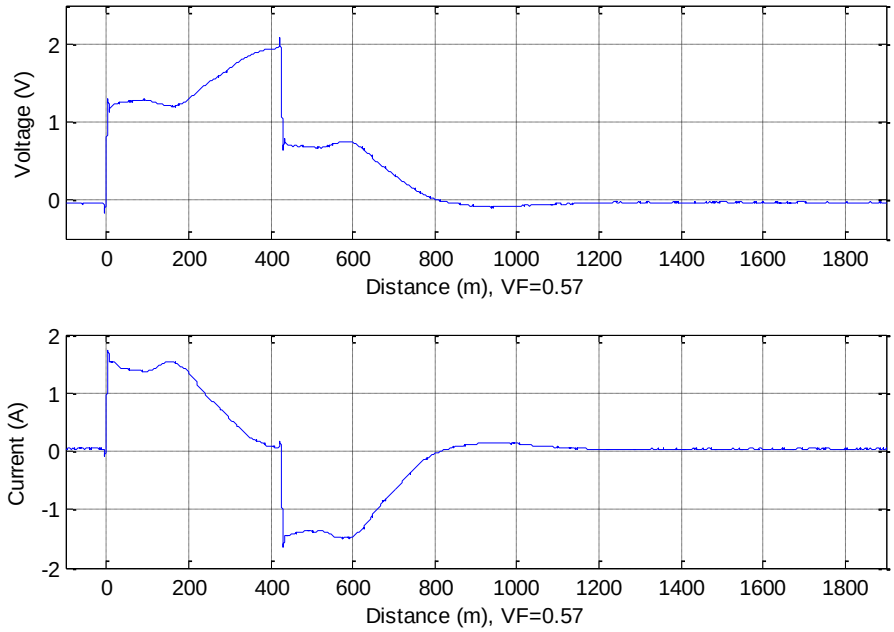


Figure 3-29: Voltage (a) and current (b) reflection waveform of 5us pulse in 100m cable with T-joint, Case 3, Scenario 2.

3.3.4.2.4 Discussion of Scenario 2

As described in Chapter 2, the impedance at the T-joint is (Z_0=Z_1=Z_2 for the same cable):

$$Z_{\text{T-joint}} = Z_1 \,||\, Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2} = \frac{Z_0}{2} \tag{3.0}$$

Therefore the voltage reflection at the T-joint:

$$\Gamma_{\text{T-joint}} = \frac{Z_{\text{T-joint}} - Z_0}{Z_{\text{T-joint}} + Z_0} = -\frac{1}{3}$$

Hence for TDR testing in the LVUDN, the T-joint causes a low impedance reflection, as seen in Figure 3-27 and Figure 3-28. The T-joint will cause an even more complex waveform in LVUDN if using a longer pulse, as illustrated in Figure 3-29. This is not preferred by any TDR technique. In practise, the TDR based cable fault locator utilises either short pulse width or step pulse (infinity pulse width) to minimise the complexity.

3.3.4.3 Scenario 3: Complex Cable Network with Multiple T-Joints

Scenario 3 is a TDR test based on a real LVUDN, represented schematically in Figure 3-30. One end of the network was open for connection of the testing equipment, and the other end was used for inputting a fault. This fault can be a transient fault simulated by a spark gap, a short-circuit fault, or an open-circuit fault.

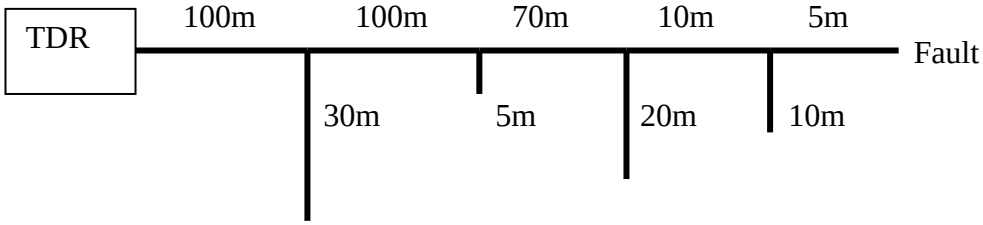


Figure 3-30: Schematic of Scenario 3 (length not to scale)

Similar to previous tests, scenario 3 has been divided into 4 cases based on the pulse width: 500 ns, 1000 ns, 5 us, and step pulse (infinity pulse width).

T-joints and multiple terminals in the cable network will cause reflection and result in a complex waveform. Assessment of cable condition directly from the reflection waveform is not possible for a complex network. In order to study the characteristics of the LVUDN, the difference waveform is computed by taking the difference of the voltage reflection waveform between two extreme fault conditions (O/C and S/C).

The fault distance is then extracted from the difference waveform. This distance can be calculated by using the zero-crossing gradient method described in [6]. Using the zero-crossing gradient method, the fault distance is calculated by using the first zero of significant gradient in the difference waveform.

3.3.4.3.1 Case 1: TDR using pulse length 500ns, fault point open circuit (O/C) and short circuit (S/C)

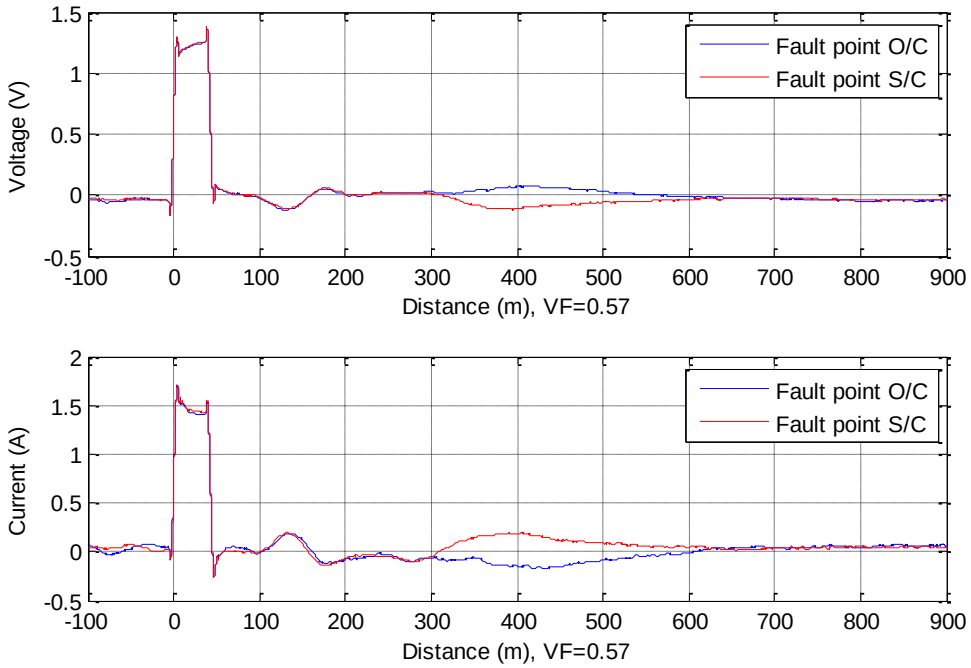


Figure 3-31: Voltage (a) and current (b) reflection waveform of 500ns pulse in complex network, Case 1, Scenario 3

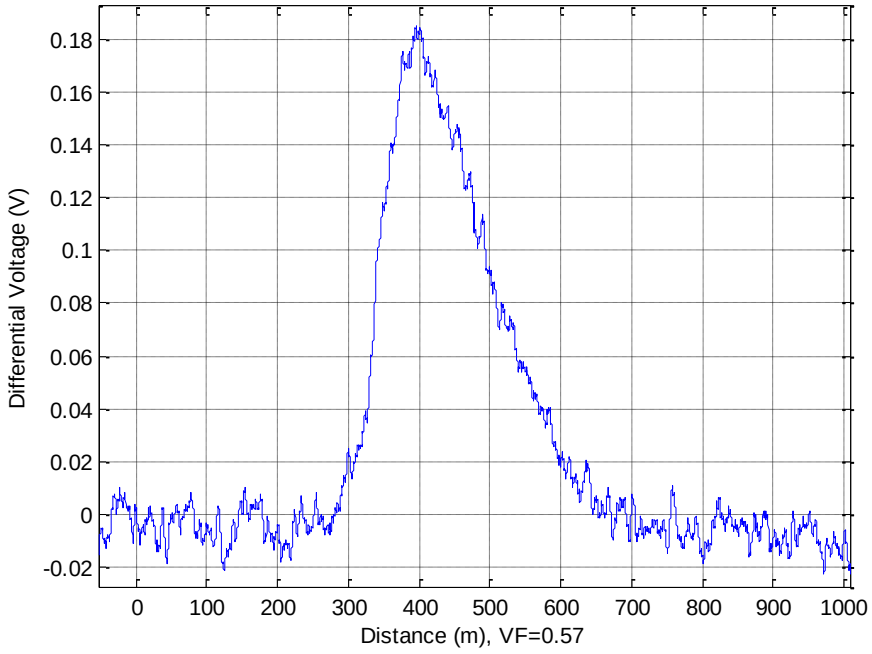


Figure 3-32: Difference between O/C and S/C fault waveform, Case 1, Scenario 3

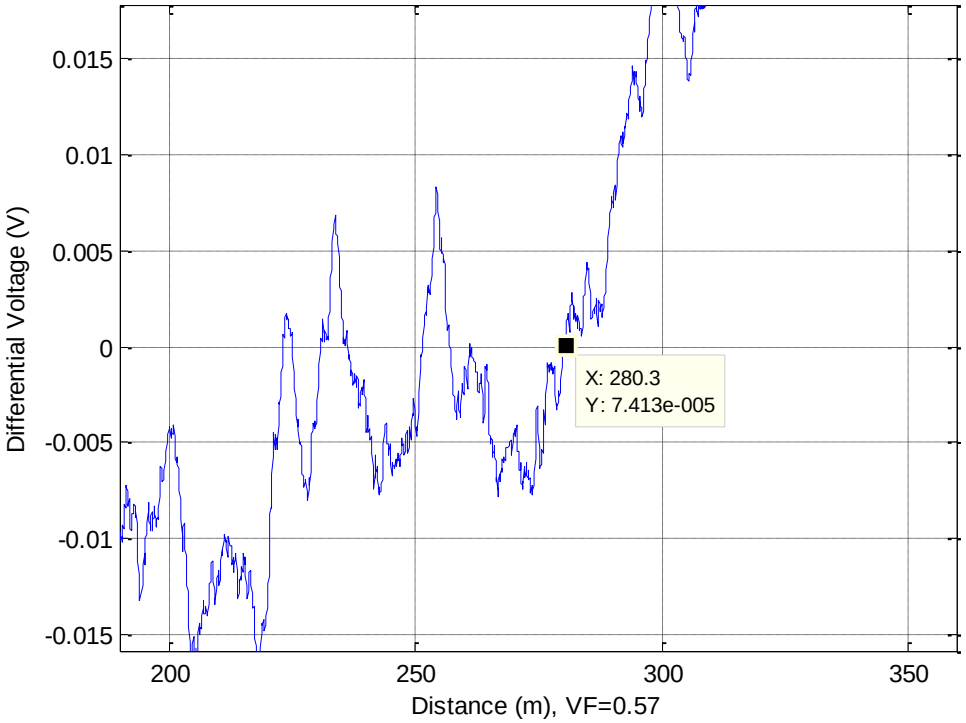


Figure 3-33: Difference between O/C and S/C fault waveform, Case 1, Scenario 3 (Zoomed)

3.3.4.3.2 Case 2: TDR using pulse length 1000ns, fault point open circuit (O/C) and short circuit (S/C)

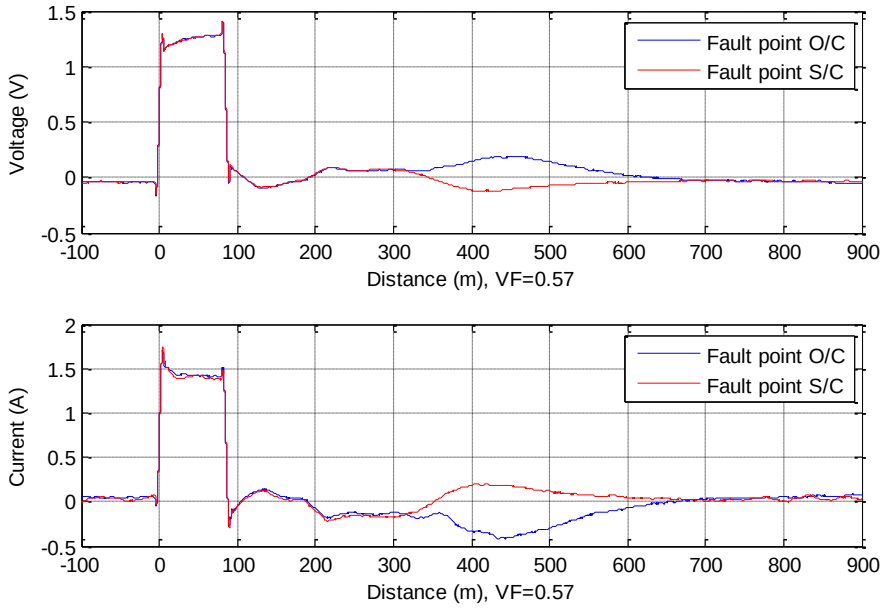


Figure 3-34: Voltage (a) and current (b) reflection waveform of 1000ns pulse in complex network, Case 2, Scenario 3.

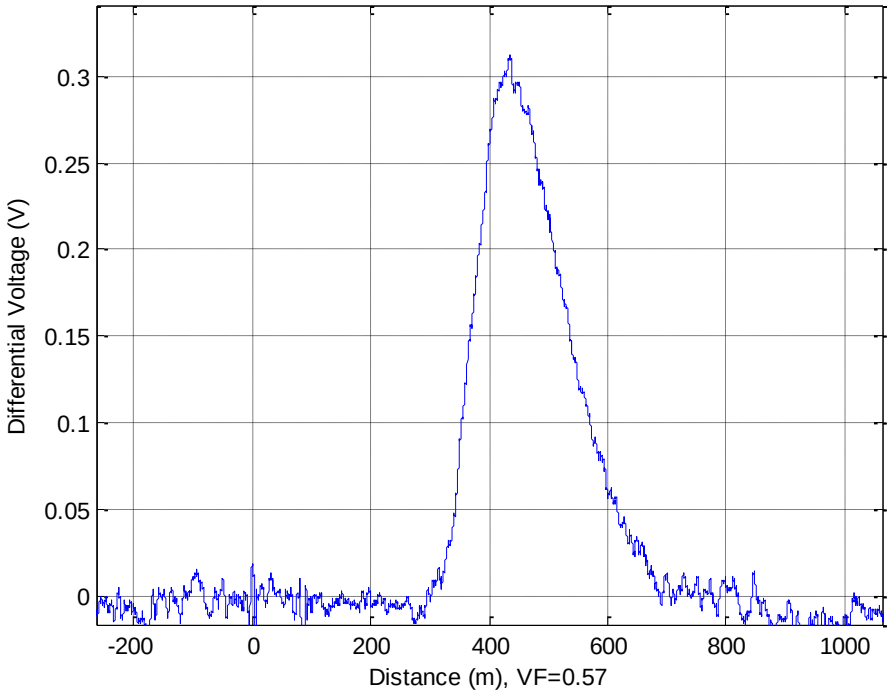


Figure 3-35: Difference between O/C and S/C fault waveform, Case 2, Scenario 3

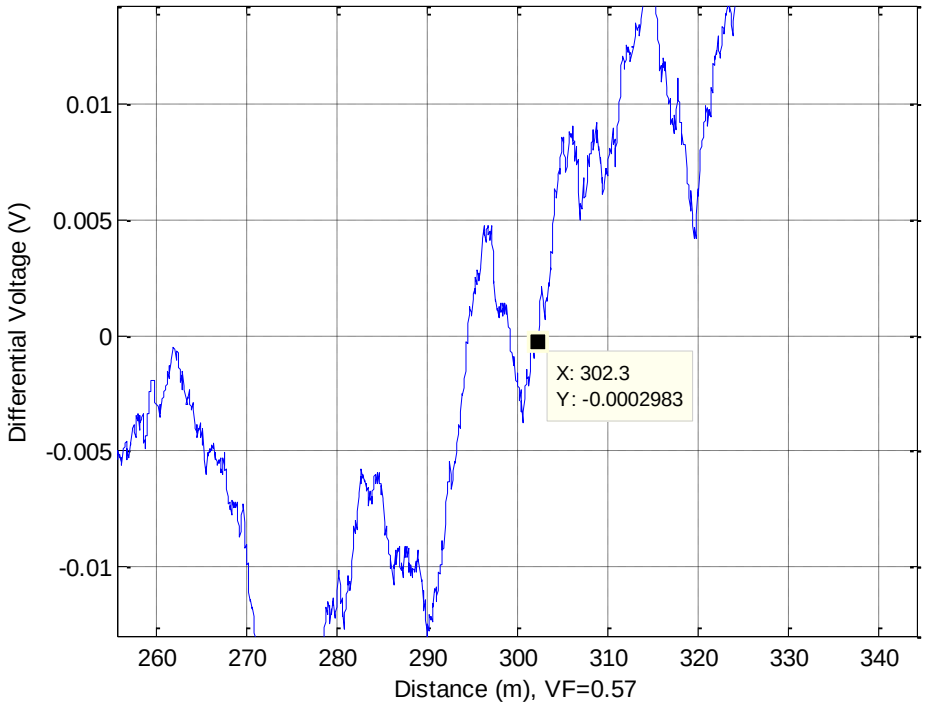


Figure 3-36: Difference between O/C and S/C fault waveform, Case 2, Scenario 3 (Zoomed)

3.3.4.3.3 Case 3: TDR using pulse length 5us, fault point open circuit (O/C) and short circuit (S/C)

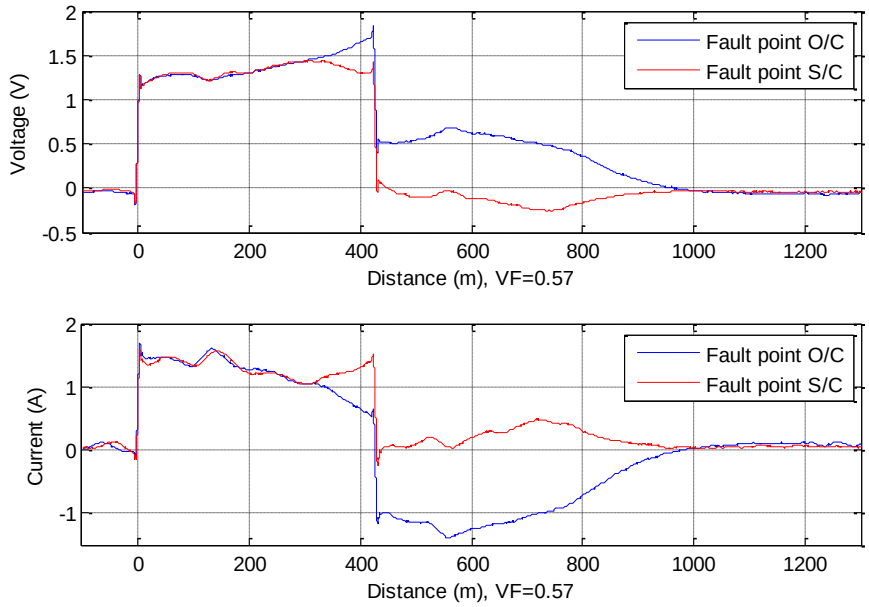


Figure 3-37: Voltage (a) and current (b) reflection waveform of 5us pulse in complex network, Case 3, Scenario 3.

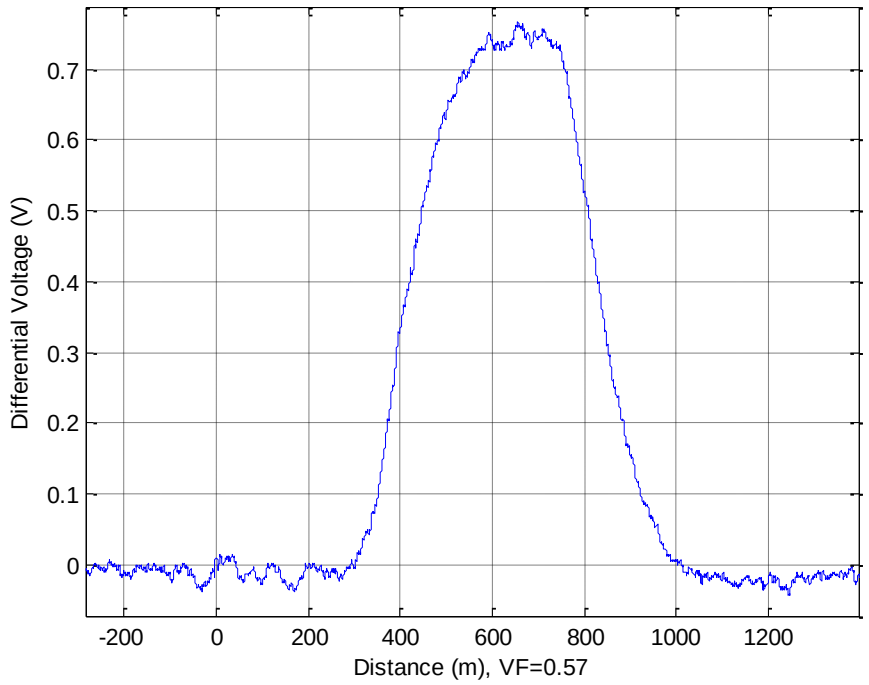


Figure 3-38: Difference between O/C and S/C fault waveform, Case 3, Scenario 3

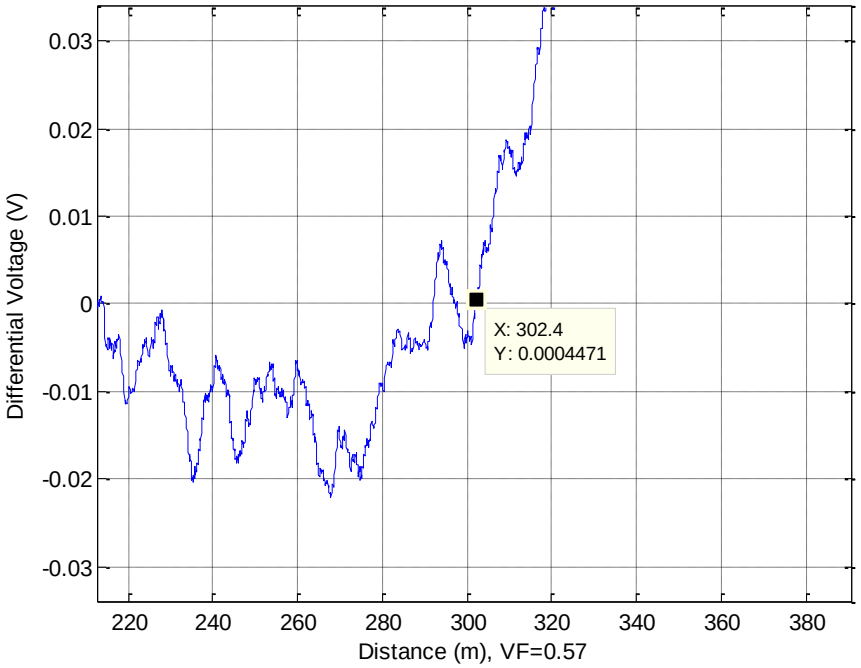


Figure 3-39: Difference between O/C and S/C fault waveform, Case 3, Scenario 3 (Zoomed)

3.3.4.3.4 Case 4: TDR using infinity pulse length (step), fault point open circuit (O/C) and short circuit (S/C)

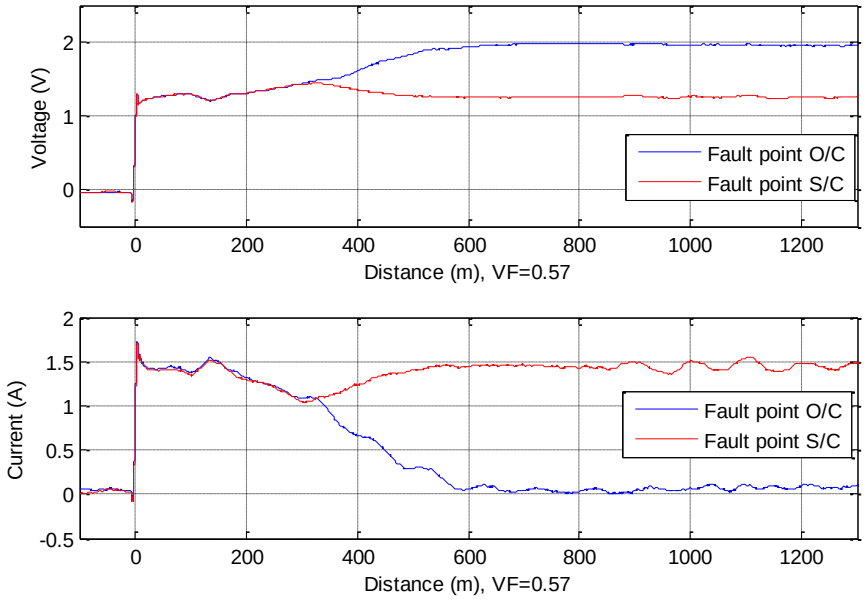


Figure 3-40: Voltage (a) and current (b) reflection waveform of step pulse in complex network, Case 4, Scenario 3.

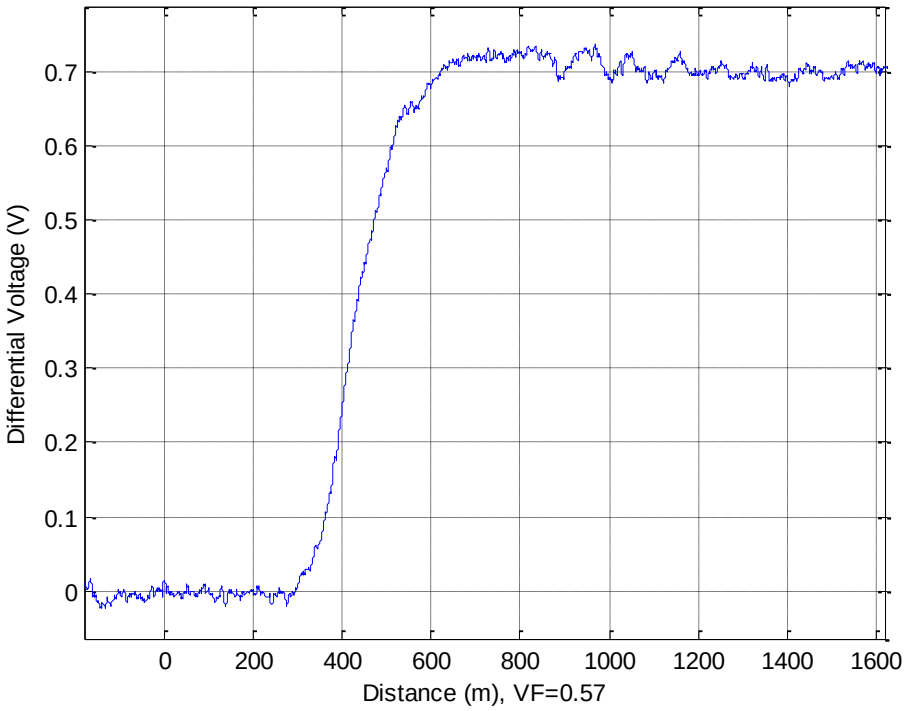


Figure 3-41: Difference between O/C and S/C fault waveform, Case 4, Scenario 3

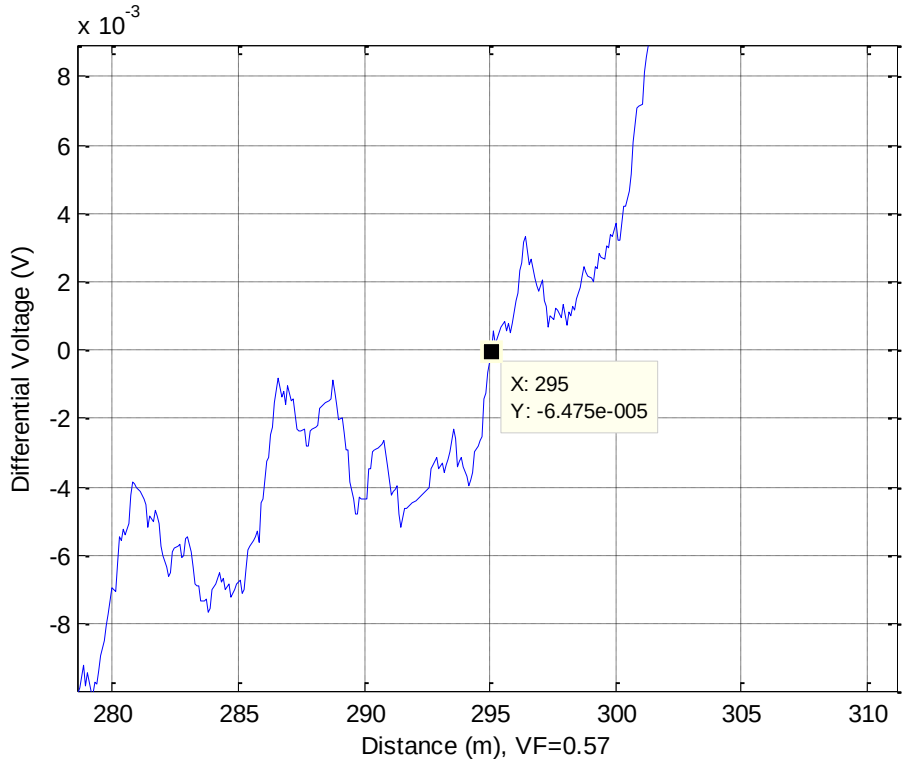


Figure 3-42: Difference between O/C and S/C fault waveform, Case 4, Scenario 3 (Zoomed)

3.3.4.3.5 Discussion of Scenario 3

As mentioned above, it is very difficult to diagnose the cable fault by directly examining the reflection waveform.

The reflection waveform in Figure 3-31 of Case 1 shows the complexity cause by T-joints and multiple cable ends. The complexity further increases if using longer pulse width (Figure 3-34 of Case 2 and Figure 3-37 of Case 3). The complexity is reduced, however, if the interrogation pulse width is significantly longer, for example infinity pulse width as shown in Figure 3-40 of Case 4.

A fault in a complex cable network can be identified by exploring the difference of reflection waveforms before the fault and during the fault, as shown in Figure 3-32, Figure 3-35, Figure 3-38 and Figure 3-41 for Cases 1, 2, 3 and 4, respectively. The result of each case is shown in Figure 3-33, Figure 3-36, Figure 3-39 and Figure 3-42. A summary with distance and error for each case is listed in Table 3-5.

The minimum error is achieved by using the short pulse in Case 1. The error increases because the falling edge of the longer pulse will affect the result, as shown in Case 2 and Case 3. Case 4 utilises a step pulse, hence there is no falling edge within the detection range, giving a comparatively better result. However, a step pulse is only suitable for use on de-energized cables because of the low frequency and high magnitude DC component, which make the step signal difficult to couple into the cable network.

From Table 3-5 it can also be seen that the difference amplitude is proportional to the pulse width, with longer pulse width indicating more energy is being transmitted into the cable.

Table 3-5: Compare of fault locating result by each case.

Case Number	Pulse Width	Difference Amplitude	Actual Fault Distance	Calculated Fault Distance	Error
1	500ns	~0.18V	285m	280.3m	-1.65%
2	1000ns	~0.3V	285m	302.3m	+6.07%
3	5us	~0.7V	285m	302.4m	+6.10%
4	Infinity	~0.7V	285m	295.0m	+3.51%

3.4 Conclusions

Most of the transient faults in underground power cables are due to defective insulation, resulting from the severe environments where the cables are installed. The transient effect results in a fast voltage collapse, and the fault shortly recovers due to self-extinguishing of the plasma channel built up during the arcing event, aided by the zero-crossing property of the AC voltage waveform. The transient fault appears as a short-duration, high-frequency, low-impedance fault if examined by travelling wave based fault locating methods, including time domain reflectometry (TDR). The TDR using a longer duration interrogation pulse is effectively a lower frequency travelling method, whilst the TDR with shorter pulse is using a higher frequency signal. Longer pulse TDR has a better detection distance, while shorter pulse TDR has a better range resolution. However, underground power cables are only specified for low frequency power transmission, and post large attenuation to high-frequency signals. The high frequency characteristics are investigated in this chapter, underpinning the basis of the proposed method presented in the following chapters. Besides the attenuation, the conventional pulse TDR method is not suitable for transient fault monitoring, as switching noise will significantly increase the complexity of interpretation of the results, leading to large errors.

4 A Novel Pulse Compression Enhanced Fault Locator

4.1 Introduction

Time domain reflectometry (TDR) is widely used for fault pre-location in electrical cable networks. It works in a similar way to the principle of radar; by transmitting an interrogation pulse down a cable and monitoring the reflected signals. TDR employs transmission line theory and pulse reflection principles to detect impedance mismatches along a cable. Impedance changes along a cable are mainly due to a fault on the cable, cable terminations, or cable joints.

The success of TDR to address faults relies on the simplicity of the cable circuit being diagnosed. For example, TDR is largely successful for fault location on overhead transmission (OHT) lines. As OHT is normally used for long-distance transmission, its circuitry is relatively simple, with a small number of joints. However, TDR has limitations when used on underground cable networks. There are two reasons: on the one hand, the conductors of underground cables are close to each other, which results in high capacitance and leads to high attenuation; on the other hand, underground cables are normally designed for short-distance electricity distribution, hence they come with multiple T-joints in implementation. Attenuation and the T-joints will distort the interrogation pulse and add significant complexity to the reflected signals.

Additionally, conventional TDR equipment only has limited functionality when locating transient faults. A transient fault is the early stage of a fault and will generally only last for a fraction of a power cycle, causing neither immediate power failure, nor service disruption. Because impact to the power network is small, a

transient fault may not cause fuse operation. The occurrence of a transient fault is difficult to predict, hence to address transient faults, conventional TDR generally employs a high voltage surge generator to initiate the fault, and which requires a high-power blocking inductor and disconnection of the power supply/customer loads. The high-power blocking inductor ensures that the high voltage surge pulse is only injected into the cable circuit under test, whist disconnection of the power supply and load prevents dedicated equipment (e.g. digital electricity meter) from being damaged by the high voltage surge. None of these requirements are preferable to network operators.

This chapter presents an innovative, pulse compression enhanced, fault location system, to overcome restrictions posed by conventional TDR. The key aspect of this technique comprises the combination of improvement of the TDR detection distance and range resolution by using pulse compression technology; and comparison of signals from the same pair of cables under test at 2 different instances.

In section 4.2, an overview of the pulse compression enhanced fault location system is displayed. Section 4.3 explains the reason why pulse compression is employed, and how it has been used to enhance the location of faults; the implementation is also discussed in detail. In section 4.4, a self-comparing scheme for locating transient faults is introduced. The calculation of fault distance is demonstrated in section 4.5; pulse compression is used to enhance the range resolution and detection distance, and the self-comparing scheme is used to identify the transient activities in underground cables.

The performance of the system is also evaluated using test data in section 4.5, and analysis of these results is given. The tests were based on the fully customized hardware TFM1000 presented in Chapter 5; Section 4.6 shows how the parameters of

pulse compression and the self-comparing scheme were optimized, and the results are shown.

4.2 Overview

Figure 4-1 illustrates a general diagram of the pulse compression enhanced fault location system. Instead of having multiple transceivers for multi-conductor cable networks, cable testing in this system is always based on two electrical conductors, and signal routing circuitry is included to select all possible pairs in multi-conductor cables. The transceiver is indirectly connected to a pair of cables under test through a coupler which allows only high frequency signals (i.e. the interrogation pulse) to pass to/from the cable pair under test. The coupler also provides an attenuated output to the instrument for monitoring low frequency voltage signals (e.g. 50 Hz voltage waveform). The cable under test may be energized (under working condition) during testing.

A digital storage transceiver with arbitrary signalling capability is connected to the coupler and controlled by a processor. The transceiver comprises an arbitrary signalling transmitter and a digitizing receiver. The transmitter converts the digital interrogation pulse waveform in the storage to analogue signals, while the digitizer samples the analogue signals (reflected signals) into digital waveforms and stores in the storage memory. Both the interrogation waveform (reference signal) and reflected signal are copied to the signal processing unit for the pulse compression operation. The transceiver is configured and triggered by the processor.

The pulse compression computation is completed by the processor and the compressed output is fed to the self-comparing scheme, as shown in Figure 4-2. The self-comparing scheme stores a number of compressed reflected signals in a time

interval which are subsequently used to compute an average signal as a reference signal, and computes the deviation against the latest compressed reflection signal. This deviation waveform will be compared against a threshold, to identify whether the deviation is significant enough to represent a fault.

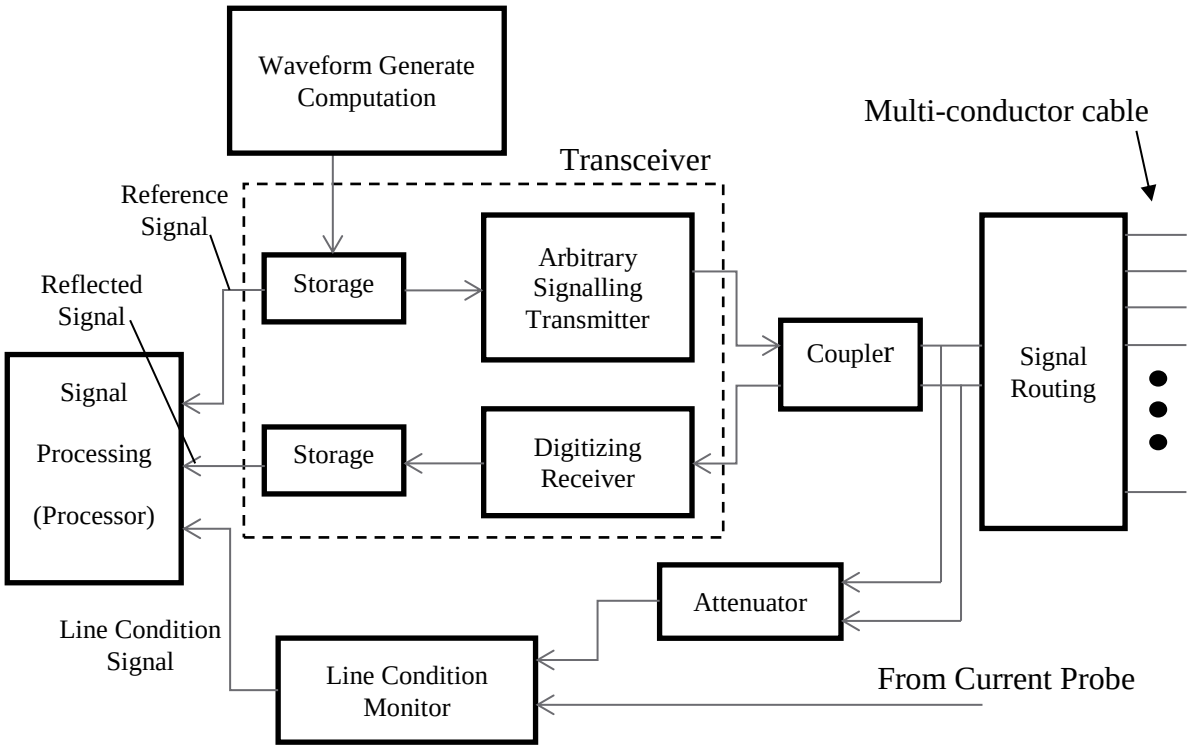


Figure 4-1: General diagram of fault locator

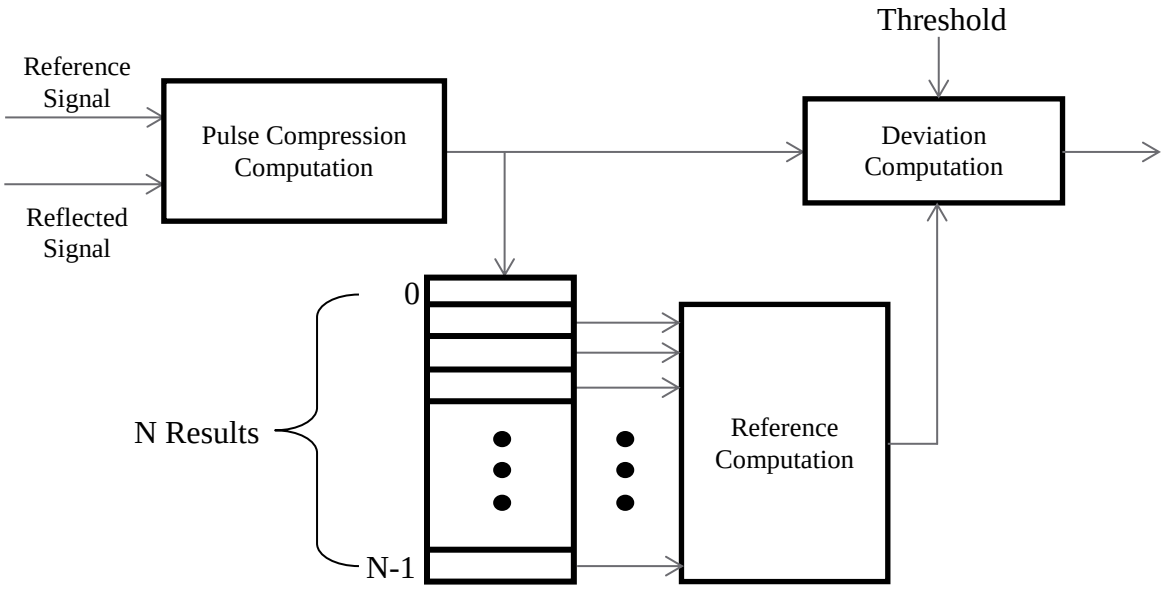


Figure 4-2: The self-comparing scheme

4.3 Pulse Compression

4.3.1 Why Pulse Compression?

In accordance with the pulse compression enhanced fault location technique, the interrogation pulse-like waveform is a modulated, high-bandwidth signal. This signal will have energy content comparable to that of a long-duration rectangular pulse, but with high bandwidth corresponding to that of a short-duration pulse. The presence of the modulated signal is then recognised from the reflection signals and gives a narrow width but high amplitude output, which will significantly aid the identification of faults in the cable under test. The above recognition process is implemented by a pulse compression module. It should be noted that, if the transmitter is configured to send a simple rectangular pulse, then it becomes a conventional TDR operation.

Considering the simple network scenario of a TDR test in section 3.3.4.1, it is obvious that the incident pulse was a sharp edge of rectangular shape; however its reflected waveform became a triangular-like pulse because of cable attenuation and loss. The result for far end open circuit (O/C) or short circuit (S/C) is presented in Figure 4-3.

By replacing the incident pulse in the above scenario by a linear frequency modulation (LFM) modulated pulse in Figure 4-4 (a), the reflected pulse can be recorded, as displayed in Figure 4-4 (b). The pulse compression can be performed by taking cross-correlation between the reflected pulse and the incident pulse, as shown in Figure 4-5; a zoomed result is presented in Figure 4-6. Instead of looking for "start of change" points, as in conventional TDR techniques, the peaks (spikes) in the output waveform following application of the pulse compression technique represents the point of possible fault.

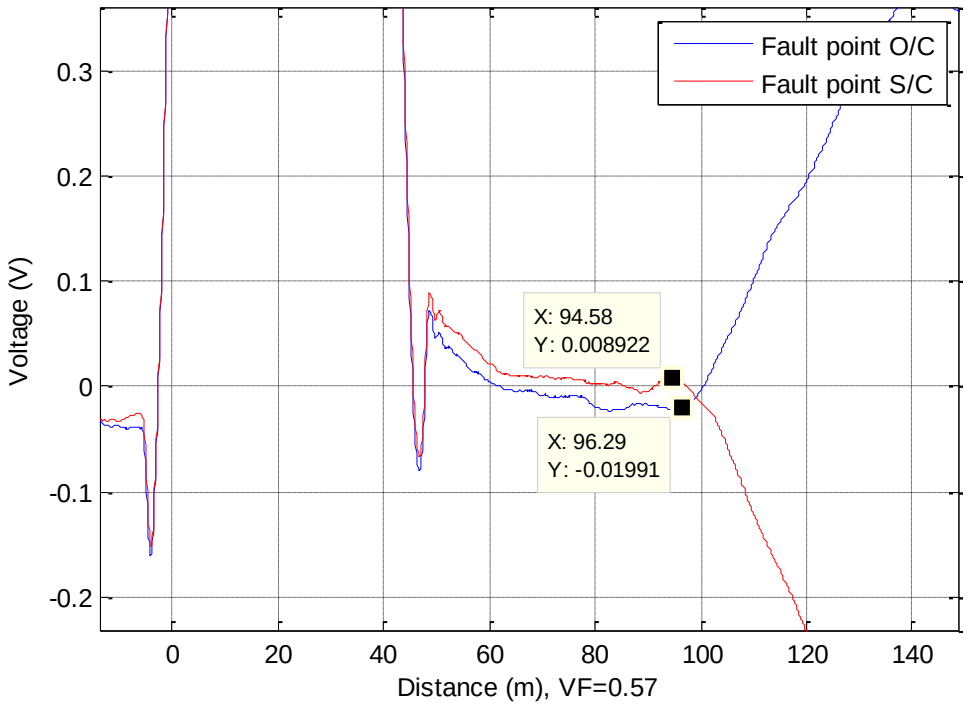


Figure 4-3: TDR result from the simple network scenario of section 3.3.4.1

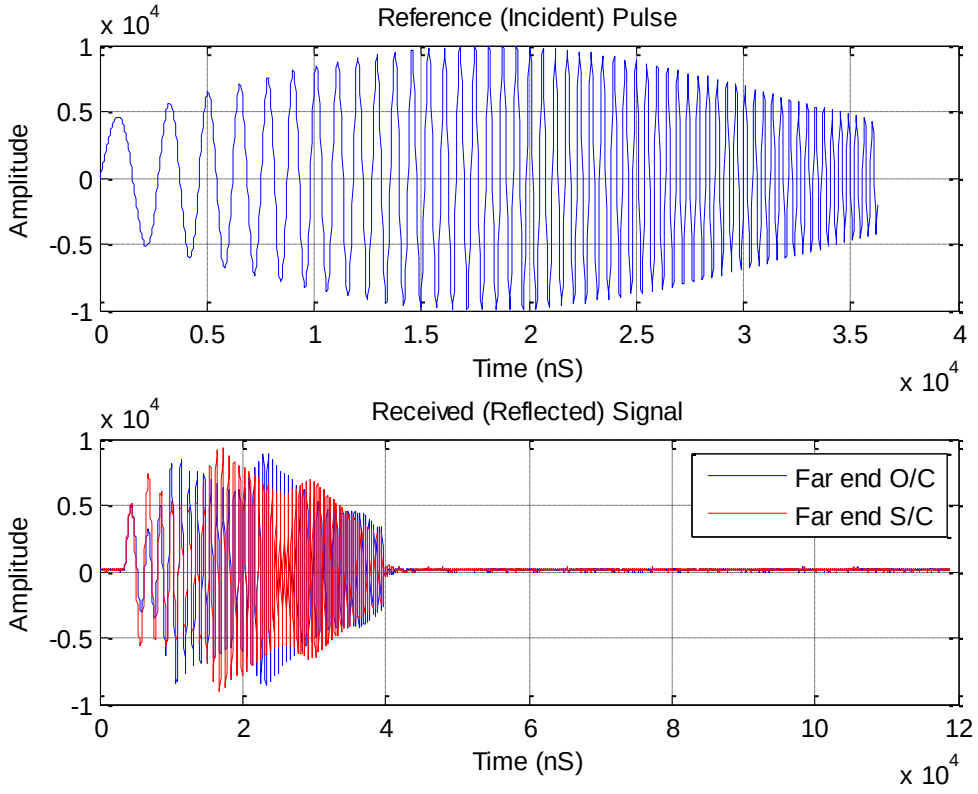


Figure 4-4: The encoded interrogation pulse (a) and according uncompressed reflection (b)

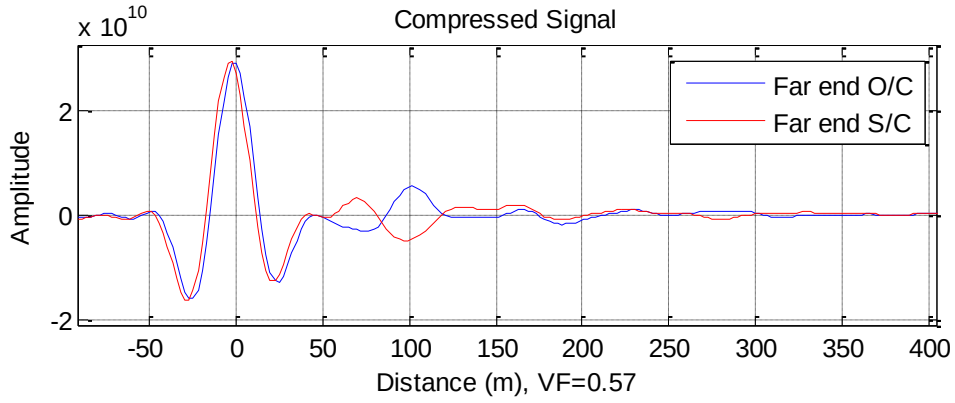


Figure 4-5: The compressed result

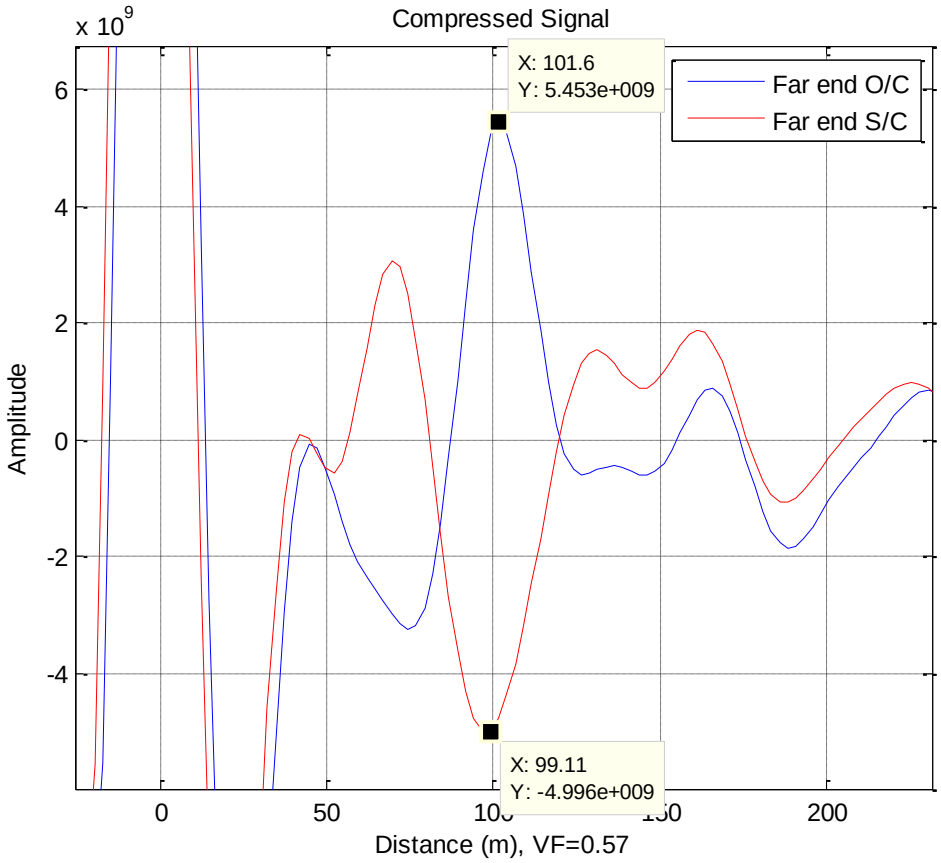


Figure 4-6: Compress result (zoomed)

4.3.2 Pulse Encoding and Decoding Process

The key to successful application of pulse compression is encoding the frequency information (bandwidth) to the interrogation signal appropriately. As mentioned in Section 2.6.4, there are many ways to encode the pulse. There is a trade-off in determining the coding method and its parameters. The more frequency information is encoded in the incident interrogation signal, the sharper is the output. However, an interrogation signal that was encoded with a high volume of frequency information will add significant complexity to both the transceiver hardware, and computation of the pulse compression. This will cause excessive pulse compression processing time.

In this thesis, a popular method called linear frequency modulation (LFM) is the preferred coding method.

The whole encoding and decoding process actually comprise two steps: Pulse encoding and pulse compressing (decoding).

4.3.2.1 Pulse Encoding Process

A flowchart for generation of the encoded pulse is illustrated in Figure 4-7. The procedure for this process is as follows:

1. The pulse encoding process is initialised by the Pulse Generation Command.
2. If no pulse parameters are given, use default parameters. The default parameters are:

$$\text{Bandwidth } B = f_H - f_L = 20MHz$$

$$\text{Frequency sweep rate } \beta = \frac{B}{\tau} = \frac{20MHz}{5us} = 4\times10^{12}\, Hz/s$$

   Amplitude = 10000, in considering that the 16-bit hardware data width is used
3. If Quadrature Amplitude Modulation (QAM) is used, generate the LFM encoded pulse based on equation (2.36) in Section 2.6.4. The complex output will be passed to the Digital QAM module and this will form higher bandwidth signals. Currently QAM is not implemented. See Chapter 7 *recommendations for future work* for additional information on QAM.
4. If QAM is not used, only the real part of the output of the (2.36) is used.
5. The encoded pulse will be stored in an output buffer and passed to the pulse compressing algorithm as a reference signal.

It should be noted that equation (2.36) may be windowed by multiplying a window function to minimise the side lobe effect.

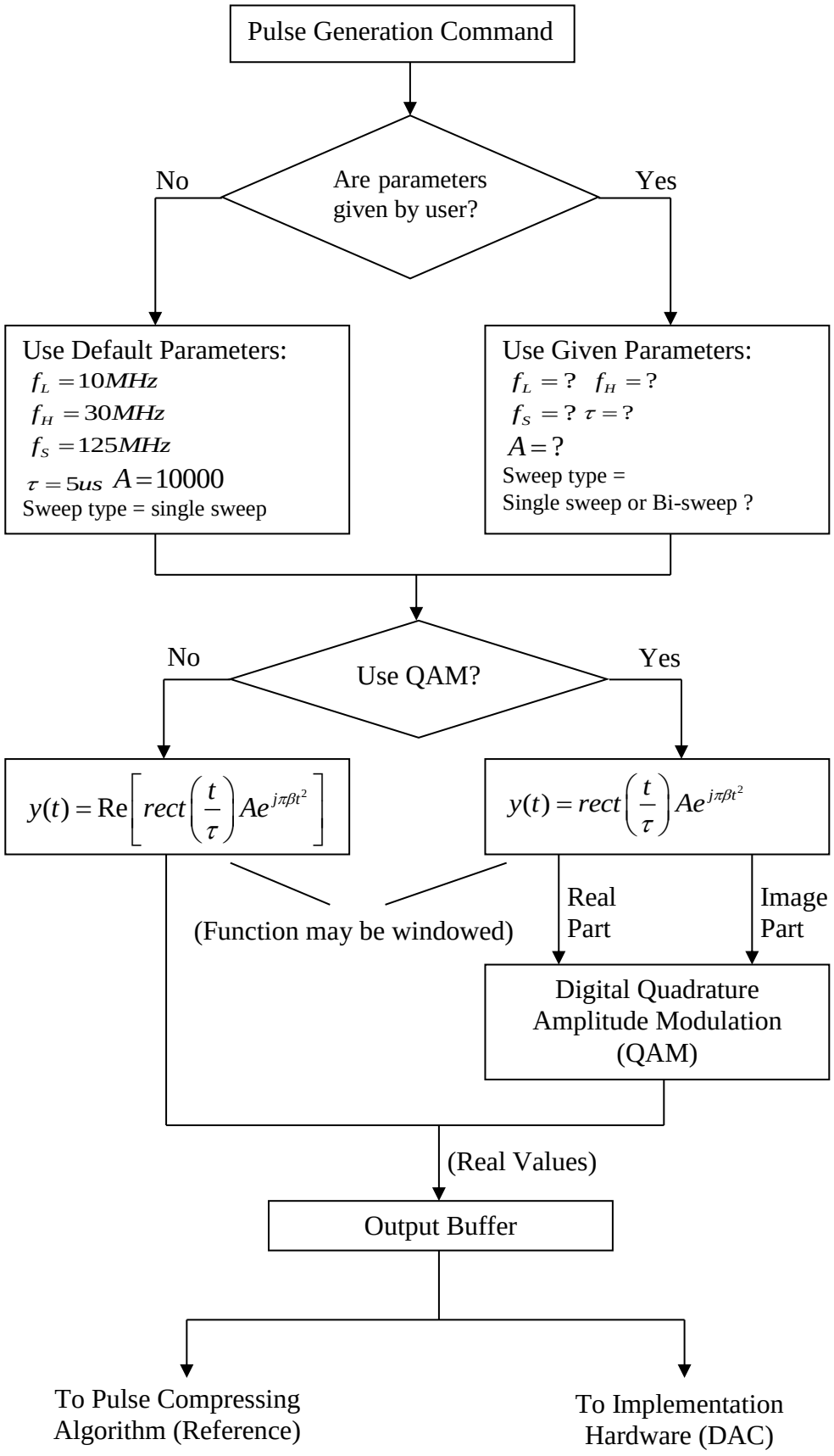


Figure 4-7: Pulse generation process

4.3.2.2 Pulse Compressing Process

The pulse compression is performed by matching the characteristics of the interrogation waveform (reference signal) from the reflected signals. This matching process can produce a sharp output, which is a significant advantage for locating cable faults in multi-T (high attenuation) underground cable networks.

The matching process is carried out by using a well-known algorithm in signal processing called cross-correlation. Cross-correlation is a mathematical operation to address the similarity of two waveforms [68]. That is, the output of the cross-correlation process reaches its maximum when two signals display maximum similarity at a certain time. There are two mathematical forms of cross-correlation: continuous cross-correlation, and discrete cross-correlation. The term "cross-correlation" in this thesis refers to discrete cross-correlation, unless otherwise specified.

The mathematical definition of discrete cross-correlation is:

$$(x \star y)[n] \stackrel{\text{def}}{=} \sum_{m=-\infty}^{\infty} x^*[m]\, y[n+m]. \tag{4.0}$$

Where:

$\star$ denotes the cross-correlation operation, and

x^* denotes the complex conjugate of x.

Figure 4-8 illustrates the process of pulse compressing. Extra decoding is required if QAM is used. If QAM is not used, the pulse compressing process is straightforward, and can be simplified to a cross-correlation operation.

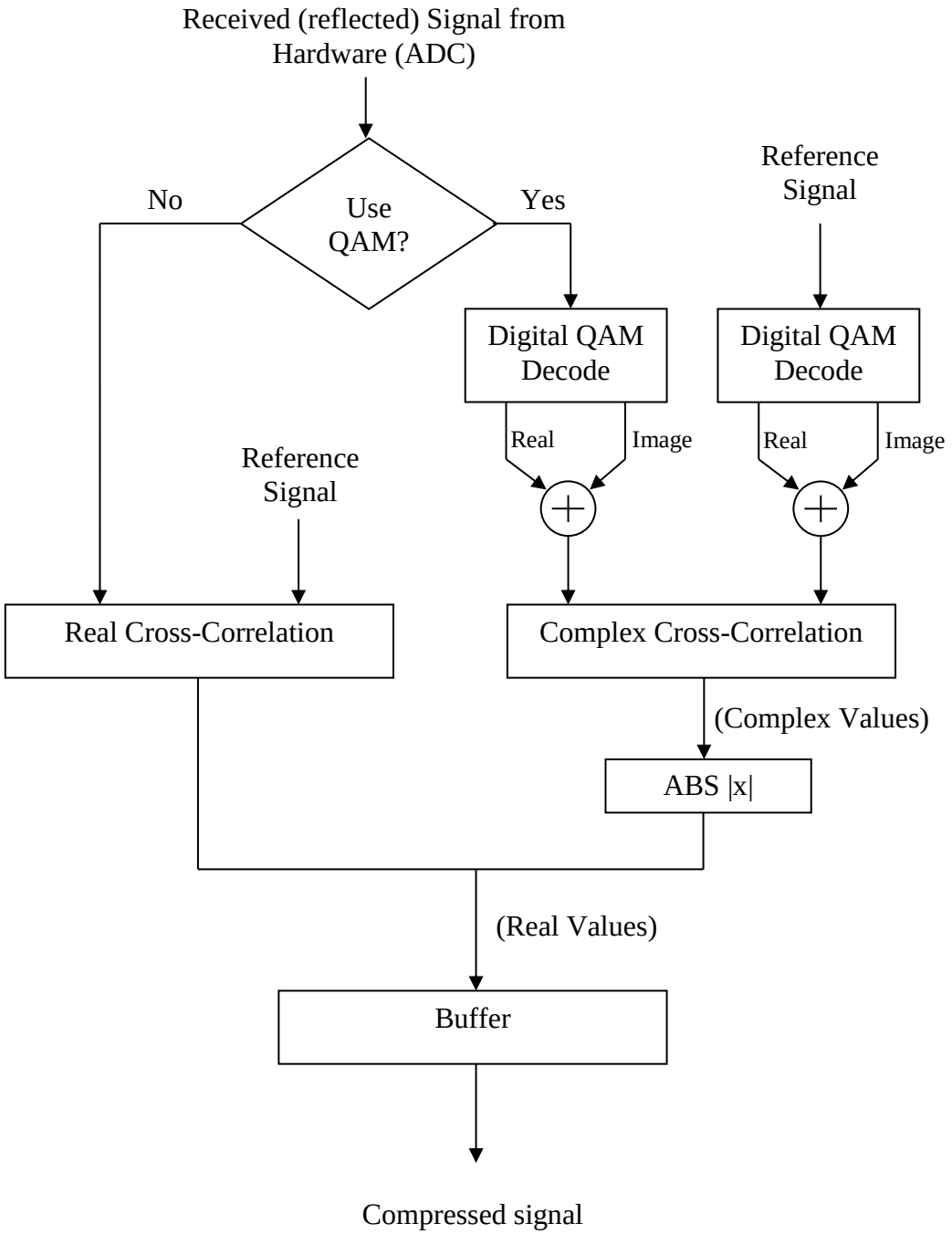


Figure 4-8: Pulse compression process

4.3.3 Optimisation of Pulse Compression parameters

As mentioned earlier, compared to conventional TDR, there is a significant increase in complexity when using pulse compression based TDR. The complexity is increased on both the hardware and software (algorithm). The implementation complexity is directly related to the pulse compression parameters, and therefore it is important to select appropriate values for these parameters in the pulse compression algorithm. To design a LFM pulse, the following parameters need to be considered.

4.3.3.1 Design of sweep frequency

Before considering the sweep frequency of the interrogation pulse, it should be noted that there is a trade-off between working frequency and cable network attenuation. As described in Chapter 3, power cables are designed for low-frequency (50 Hz-60 Hz) energy transfer, and cause high degree of attenuation to RF signals. However, higher working frequency (bandwidth) enables the choice of shorter pulse durations, and achieves higher range resolution after compression; both are desired advantages in cable fault location. As mentioned in Chapter 2, the bandwidth is equal to the sweeping frequency range, namely:

$$Bandwidth = f_H - f_L$$

For a ±5V output level, it is found that the TFM1000 can still produce acceptable results for an attenuation of -30 dB. The output distance can be further extended by increasing the output level. Thus, for a cable with the attenuation profile shown in Figure 4-9, the maximum location distance when using the maximum sweeping frequency $f_H = 20MHz$:

$$\left.\begin{array}{l} A(20MHz) = -1.247dB/10m \\ A(20MHz) * d \geq -30dB \end{array}\right\} => d \leq 240m$$

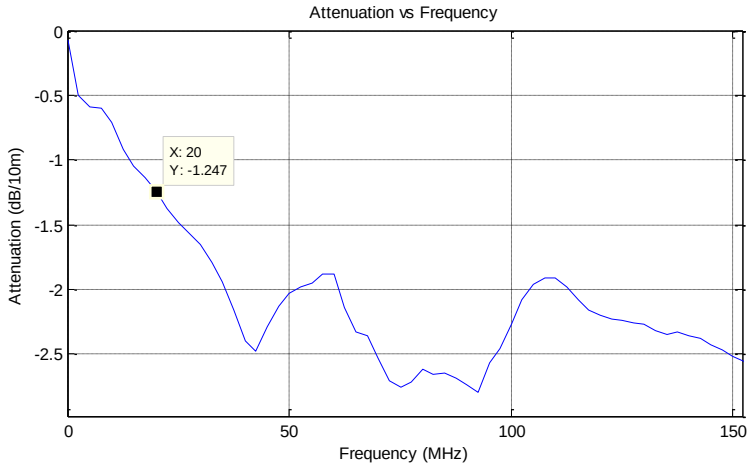


Figure 4-9: Attenuation plot of a power cable

When the bandwidth is defined as the length of the interrogation pulse, it will not have any effect on the final compressed waveform; hence, the pulse length should be as short as possible, from a time-saving point of view. However, in practice, the pulse width is limited by hardware capability. The DAC of the pulse generating system of the TFM1000 has a sampling rate of 1 GSPS. Although the maximum output frequency defined by Nyquist sampling theory is equal to 500 MSPS, as a general rule of thumb, the sampling rate should be at least 10 times higher than the maximum output frequency to produce a good shape of the output waveform. Therefore, the pulse length in this research is fixed to 10 μs, with sweep frequency no more than 20 MHz. This is equivalent to $\frac{1GSPS}{20MHz} = 50$ sampling points per signal cycle.

4.3.3.2 Design of sweep type

For easier implementation, linear frequency modulation is used in this research, in other words, the sweep frequency of the interrogation pulse is increased linearly with time. A non-linear sweep may be used to further suppress the side lobes; this has not been investigated however, due to time restraints.

4.3.3.3 Design of window

As mentioned in Chapter 2, the window function is used for suppressing the side lobes generated during the pulse compression process. Experiments have been carried out in order to find a suitable window for pulse compression in power cables.

Figure 4-10 shows a number of main lobes in pulse compression in real XLPE cables, with different weight windows. A uniformly-distributed noise was also injected into the cable to simulate noise. The signal to noise ratio (SNR) was set to 6 dB, i.e. the amplitude of noise was 50% of the signal amplitude. Such a strong noise is enough to corrupt the rectangular incident pulse used by conventional TDR systems.

Observing these windows, it can be concluded that the best result in this case is achieved by a Kaiser-Bessel window ($\pi\alpha = 8$), which provides better side lobe attenuation, as well as smaller main lobe attenuation.

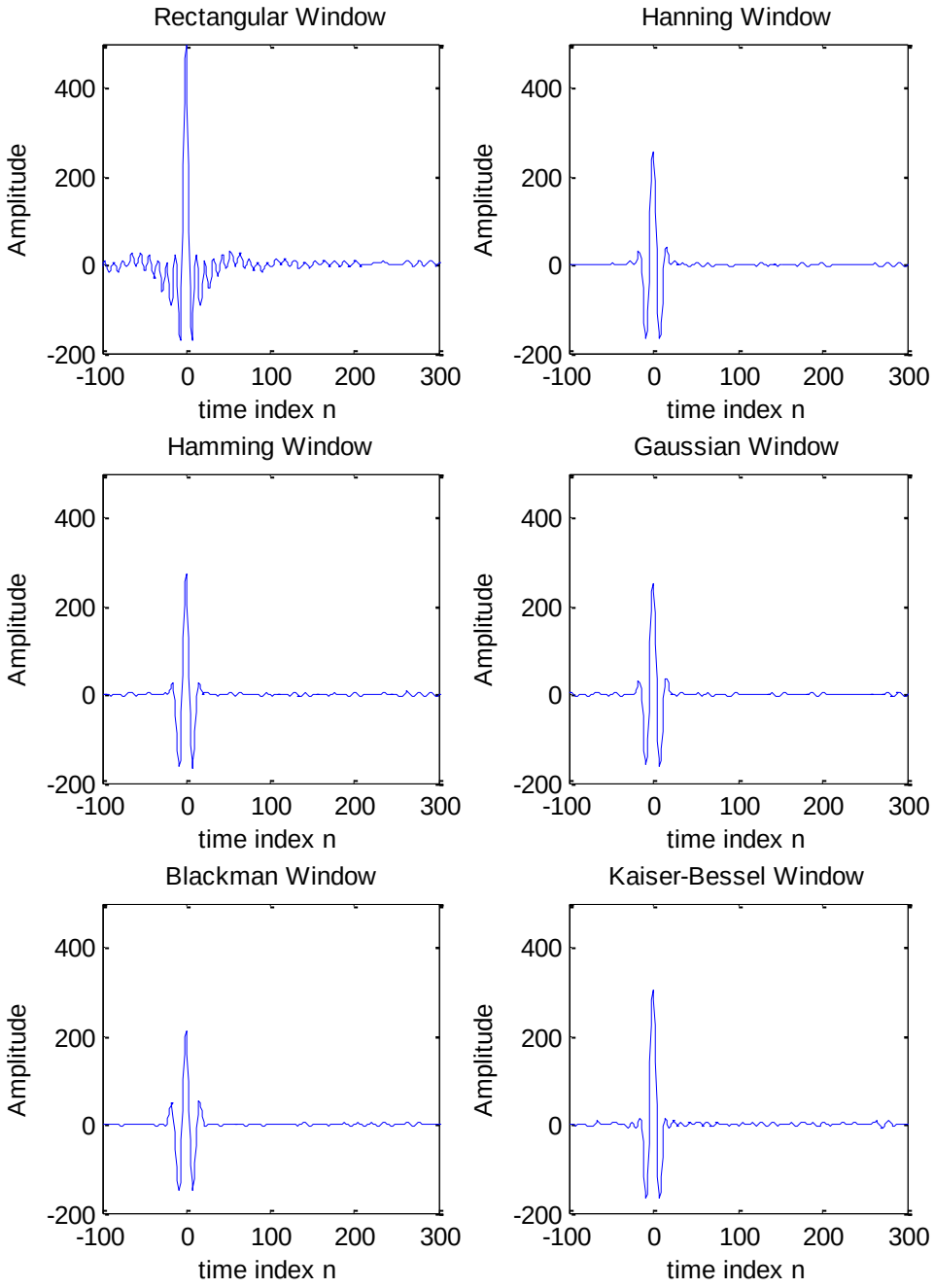


Figure 4-10: Main lobe of different weight windows in real XLPE cable with noise (SNR = 6dB).

4.4 The Self-Compare Scheme for Transient Faults

A self-compare scheme is used to address transient faults, as illustrated in Figure 4-2.

The self-compare scheme is based on deviation detection, and it works as follows:

1) An enhanced TDR operation is performed and the result is "pushed" into the number 0 slot of FIFO[§] memory. The data in this slot will be pushed to the next slot. This process is repeated until the data in the last slot (N-1 slot) is overwritten by the data of the previous slot. A timestamp is also attached to the result to indicate the time of the TDR operation.
2) The previous N-1 results are then averaged to create a reference signal to represent the previous state.
3) The deviation between the latest result in step 1 and reference signal in step 2 are calculated, as shown in Figure 4-12.
4) The deviation in step 3 is compared against a threshold. The deviations that exceed the threshold are marked "high risk", and may contain the location of faults. The setting of threshold level depends on the required sensitive and noise on the cable, and this will be based on the experimental test on the cable network under test. Lower threshold level results more sensitive to small deviation.

It can be understood that this scheme attempts to continuously monitor the time change of reflected waveforms of a TDR test. As the TDR reflection waveform is actually a time collection of network impedance changes, the reflection also varies according to the characteristics of the cable network under test. Changes in the characteristics of the cable network may be due to disconnection of equipment, operation of a switch, a new user load, or a fault. The fault can normally be distinguished by examining the location, and the significance of the change.

[§]FIFO = First In First Out

There are 3 aspects that need to be considered when using the self-comparing scheme: Time interval between acquisitions, reference computation algorithm, and threshold.

Time interval between acquisitions:

The acquisition process of TDR enhanced with pulse compression only lasts for a small amount of time (usually <100 μS), significantly shorter than a power cycle (20 ms for 50 Hz system). Therefore, the enhanced TDR operation is performed in a fixed time interval to cover the power cycle. The time interval should be small enough to catch a possible fault, but not add too much computation complexity. Considering that transient faults usually last longer than 1 ms, the acquisition time interval is selected to be 1 ms. This results in 20× TDR acquisitions per power cycle, as depicted in Figure 4-11.

Reference computation algorithm:

A number of previous TDR waveforms (N) are used to calculate a reference waveform, and this waveform will be compared against the latest TDR waveform to generate the deviation. Larger N will give better stability, as the reference is calculated based on a large number of previous samples. However, larger N will also add additional computational complexity to the system. To simplify the design, the reference waveform is the arithmetic mean of the previous N=15 waveforms. However, it could be further enhanced by using an adaptive filter to increase the dynamic performance.

As mentioned above, the deviation is a time-collection of network impedance changes between the latest "characteristic map" (TDR waveform) and the pervious "characteristic map" (reference waveform). Hence, the threshold is also a function of time, currently defined by the user. If the deviation is significant enough and exceeds the threshold, it means a change of electrical connection has occurred.

The threshold currently used has an exponential-reduction-like shape, due to the attenuation of the cable. Conventional TDR normally uses a fixed threshold to detect the key change of signals, and faults at the far end may be omitted. However, in the future the value of the threshold is expected to be self-adaptive to distance, voltage, pulse type and fault type. For example, the threshold for a cable network containing a large number of T-joints should look like a steep, exponentially-attenuated function, to represent the attenuation caused by T-joints; but for a simple cable network like OHT, the threshold can be fixed due to the lower attenuation.

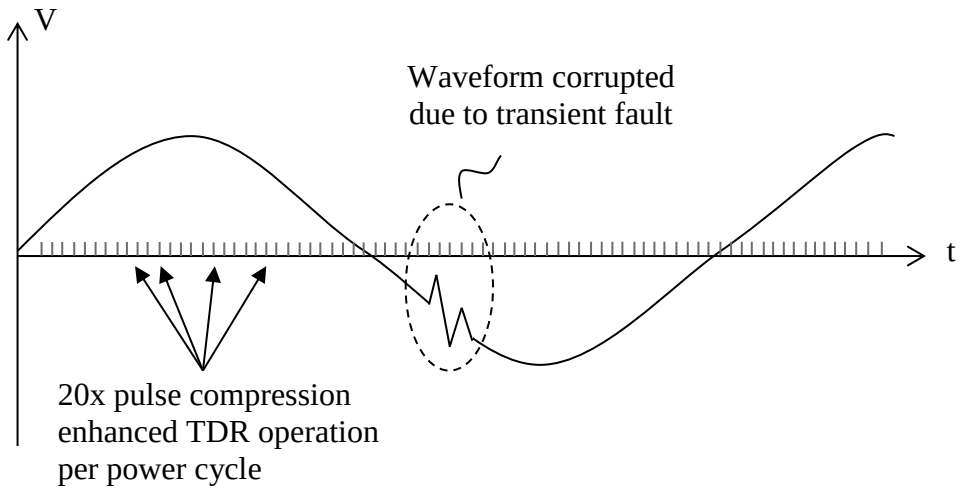


Figure 4-11: Pulse compression enhanced TDR operation in a power cycle

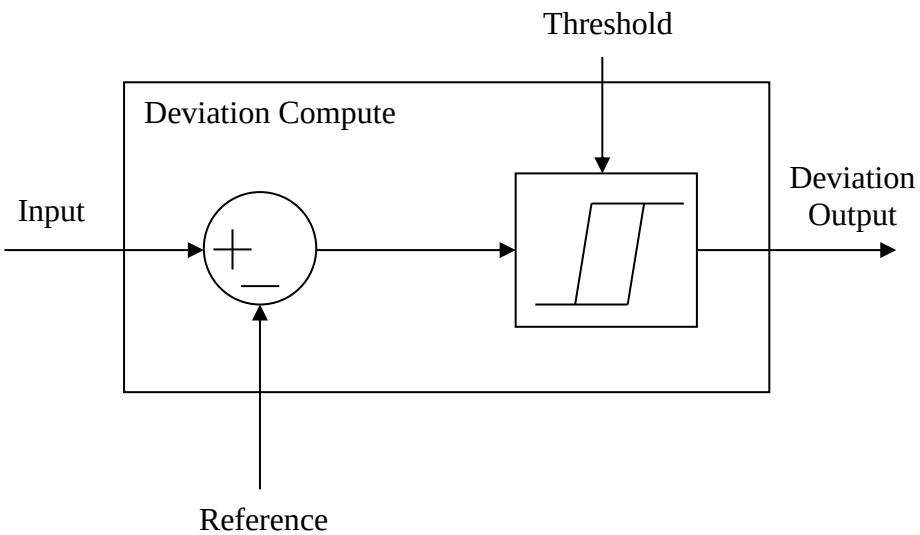


Figure 4-12: Simple deviation calculation

4.5 Analysis of Algorithm Performance

This section provides performance analysis of the pulse compression and self-comparing scheme, based on the fault location system that was designed in this chapter. Due to the restricted access to the cable test yard and limited number of test rigs, two different cable networks are tested, and the performance is determined by comparing the calculated fault distance against the actual fault distance.

Figure 4-13 displays the cable network configuration of dataset 1. The network was constructed using 185 mm^2 waveform CNE cables, described in Chapter 3. The TFM1000 was connected to the test port of the network where the cable network was energized. A controlled spark gap was connected to a test point located xx m from the far end, in order to simulate the transient fault. There was no load on the other ends of the cable network. A high frequency 1 kHz – 10 MHz white noise, of amplitude $0.32 * V_{PP-Pulse}$, was injected into the cable network, to simulate the switching noise caused by switching power supplies in real cable networks. Therefore, the equivalent signal-to-noise ratio applied to the input of the TFM1000 is approximately equal to:

$$SNR \approx 1/0.32 \approx 3.125 \approx 10dB .$$

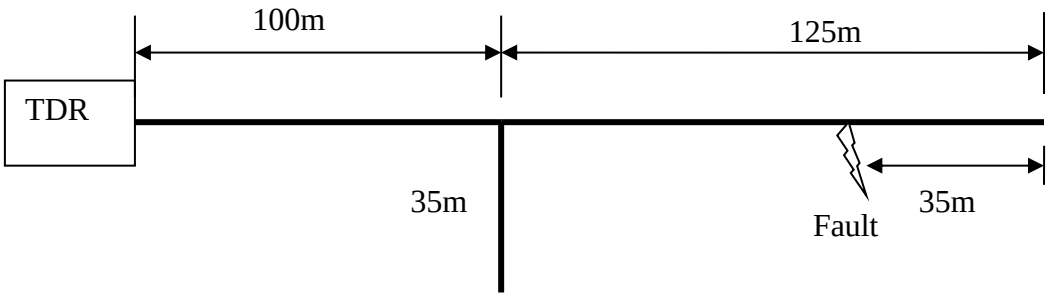


Figure 4-13: Cable network configuration of dataset 1

Figure 4-14 shows the voltage and current waveforms recorded at the energized end (TDR end) containing the activity of the transient fault. For ease of understanding, the zero of the time axis is aligned to the moment where a transient fault was triggered.

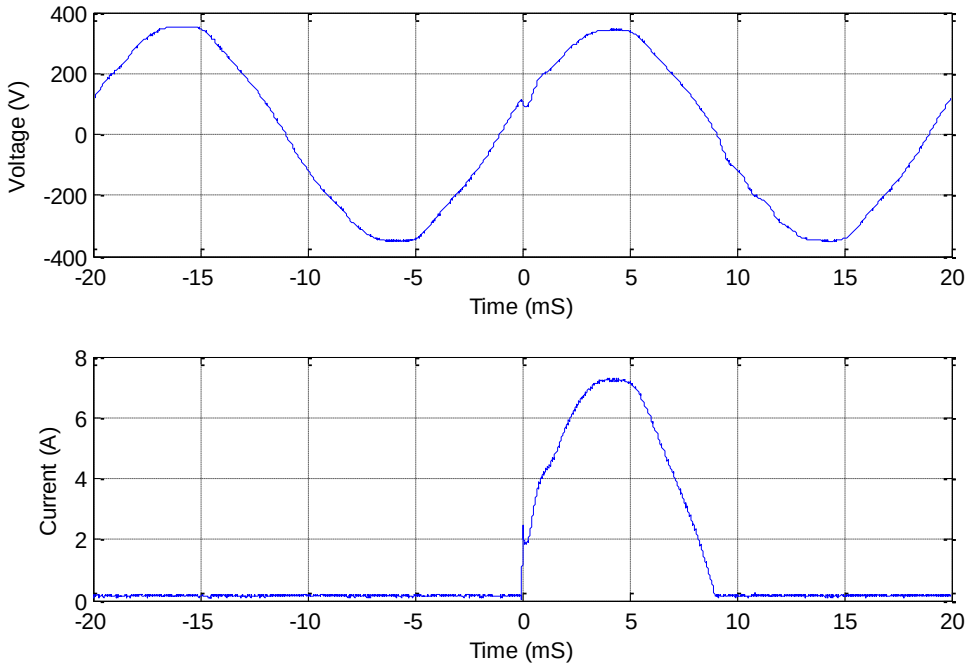


Figure 4-14: Voltage and current recorded on the transient fault of dataset 1

The interrogation pulse is a LFM pulse of length 10 μs, sweeping from 1 MHz to 15 MHz. As shown in Figure 4-15 (a), the 15 previously-compressed signals were averaged, and used as the reference signal. It can be seen from the latest received signal shown in Figure 4-15 (b) that the cable network is very noisy, and the conventional TDR method is not likely be able to discriminate a fault with such a high level of noise.

The enhanced TDR process is performed every 1 ms, and the latest reflected signal will be compressed and compared with the reference signal, as per the self-comparing scheme. The TFM1000 will be triggered when a significant deviation is detected between the latest reflected signal and the reference signal. Figure 4-16 shows both the uncompressed and compressed reflected signal when the TFM1000 was triggered

because of the detection of significant deviation, shown in Figure 4-17. In this case, the deviation is because of the transient fault, and the corresponding distance to the TFM1000 is shown in the zoomed version of the deviation map (see Figure 4-18). The fault distance shown in the deviation map is 189.6 m, and the actual distance to the fault is 100 m+125 m−35 m=190 m. Therefore the accuracy of the location is:

$$Accuracy = \frac{189.6 - 190}{190} \times 100\% = -0.21\%$$

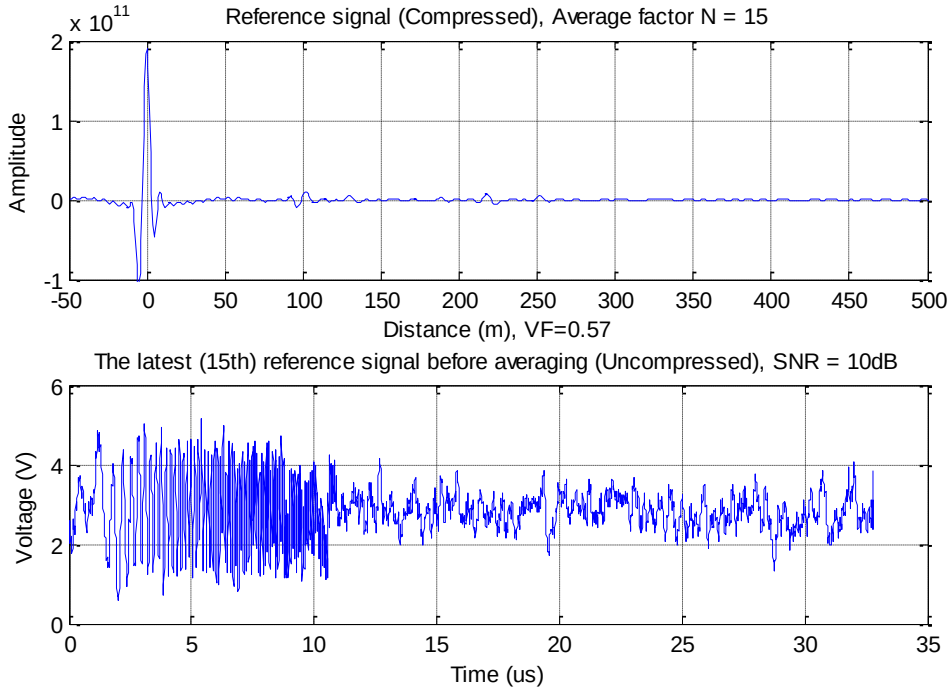


Figure 4-15: The reference signal (a) and the latest uncompressed reflected signal (b) used for computing the reference.

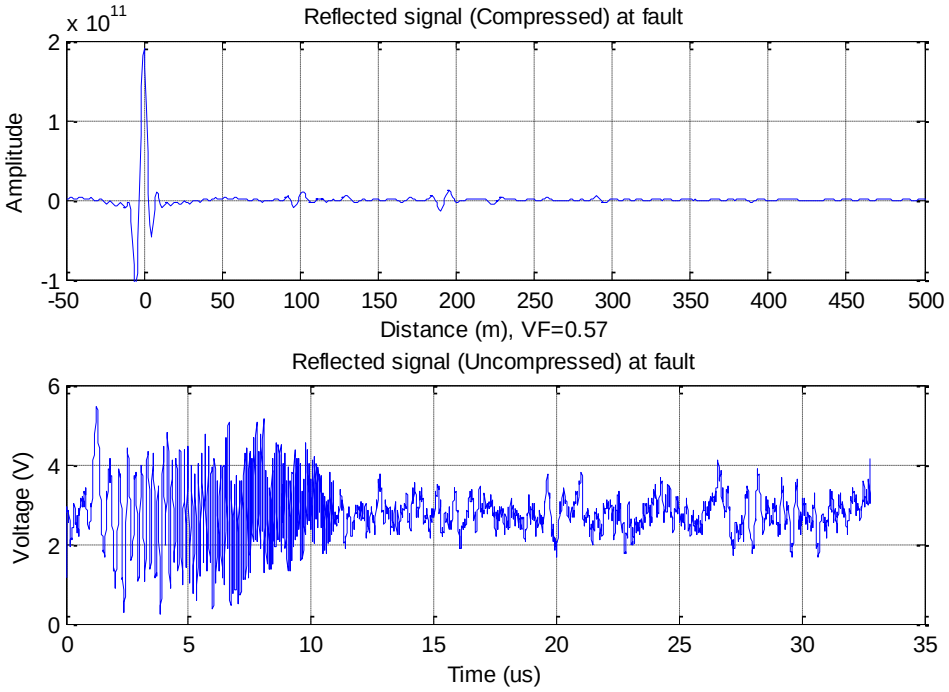


Figure 4-16: The compressed (a) and uncompressed (b) reflected signal when TFM1000 was triggered.

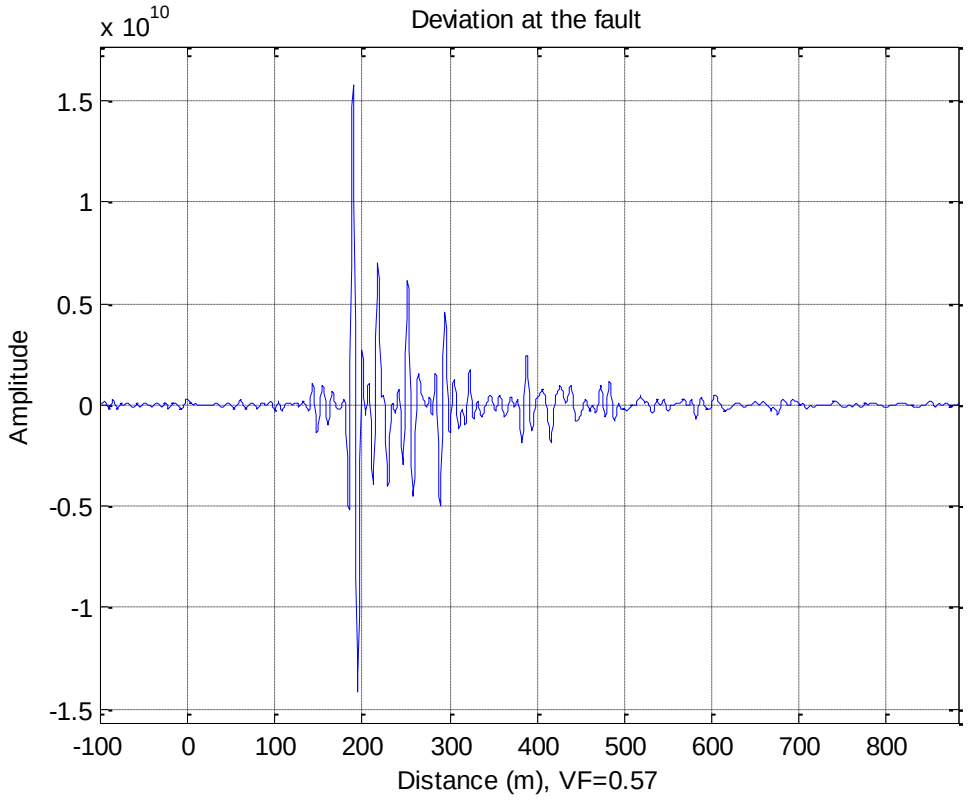


Figure 4-17: The deviation between reference signal and compressed, triggered reflected signal

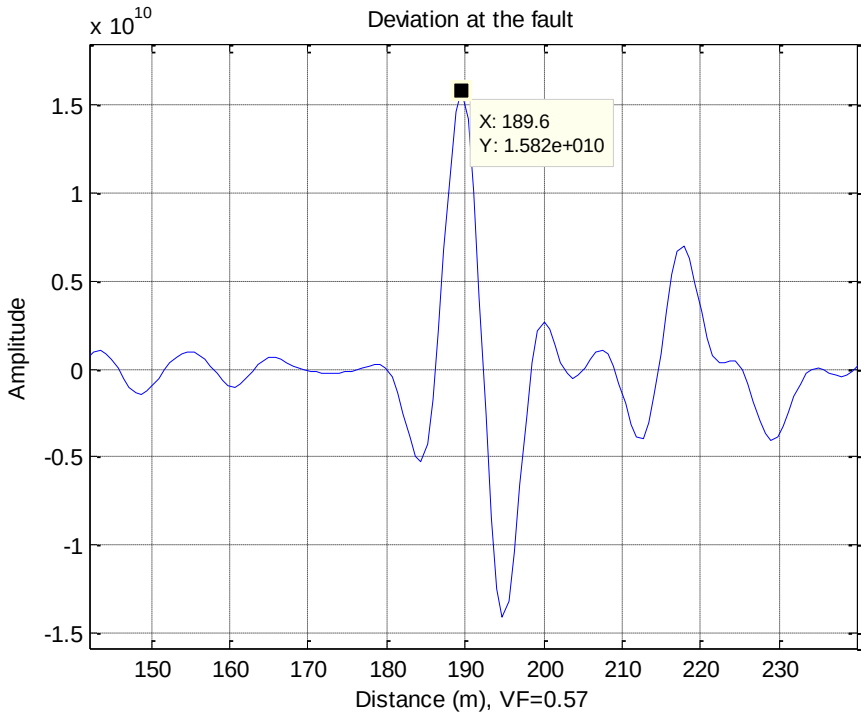


Figure 4-18: The deviation between reference signal and compressed, triggered reflected signal (Zoom in)

Dataset 2 was acquired based on the same cable network described in Section 3.3.4.3, excepting that a real load was added. The configuration can be found in Figure 4-19. The load used for the test is a Dell GX280 computer. The switching mode power supply (SMPS) of this computer is a typical AC-DC SMPS with power factor correction (PFC). PFC is used to compensate the power factor and is normally designed for full load, hence under a normal load the phase is advanced (capacitive), as depicted in Figure 4-20. The switching frequency under normal load is measured at 70 kHz. This switching noise will significantly affect the result given by a conventional TDR device.

The voltage and current waveforms when the transient was detected are displayed in Figure 4-21. As seen from the figure, the transient fault only lasts for half of a power cycle, no fuse is blown, and the computer is working as normal during the fault.

Similar to dataset 1, the reference signal is shown in Figure 4-22, and the triggered signal is represented in Figure 4-23.

Figure 4-24 and Figure 4-25 display the deviation when triggered, and the distance to the first significant departure, respectively. The actual fault distance is 285 m from the test point, and the first significant departure is 285.5 m. Therefore, the accuracy is:

$$Accuracy = \frac{285.5 - 285}{285} \times 100\% = 0.18\%$$

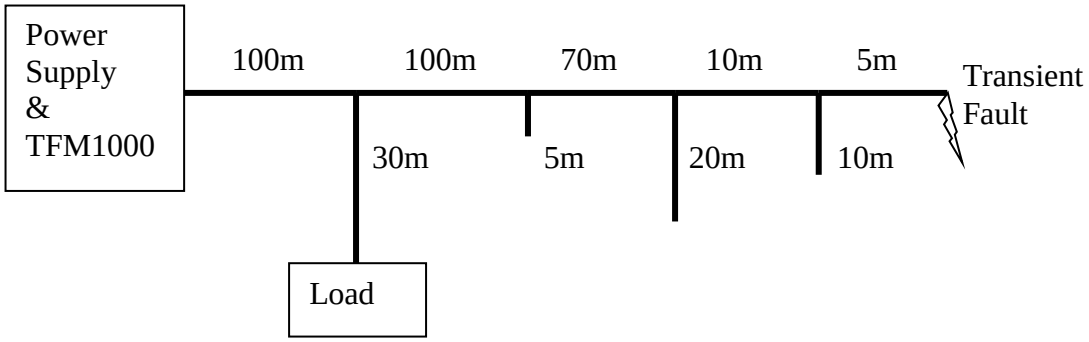


Figure 4-19: Cable network configuration of dataset 2

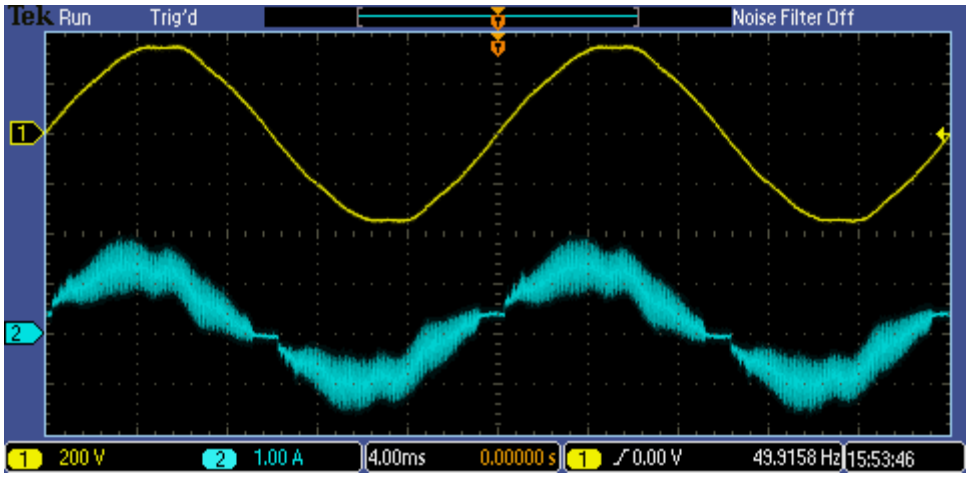


Figure 4-20: The voltage and current waveform of Dell GX280 computer in normal state.

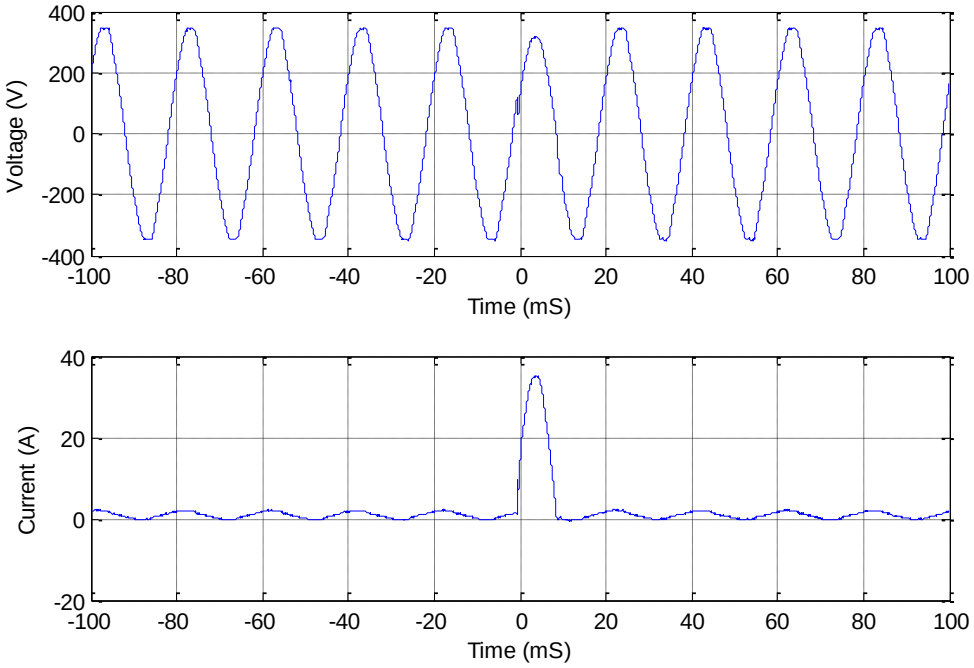


Figure 4-21: Voltage and current recorded on the transient fault of dataset 2

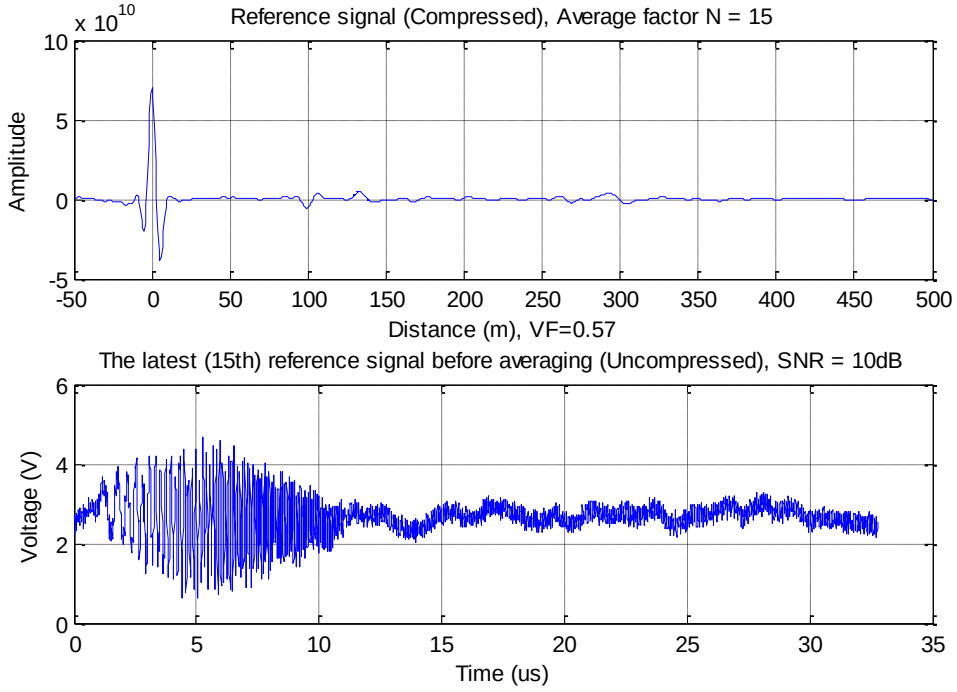


Figure 4-22: The reference signal (a) and the latest uncompressed reflected signal (b) used for computing the reference.

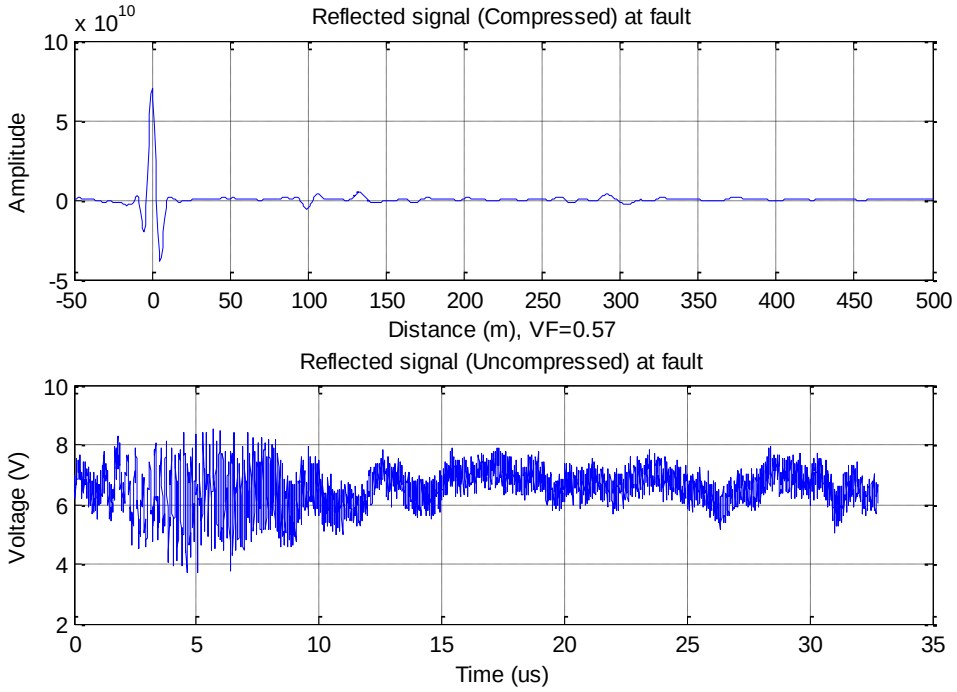


Figure 4-23: The compressed (a) and uncompressed (b) reflected signal when TFM1000 was triggered.

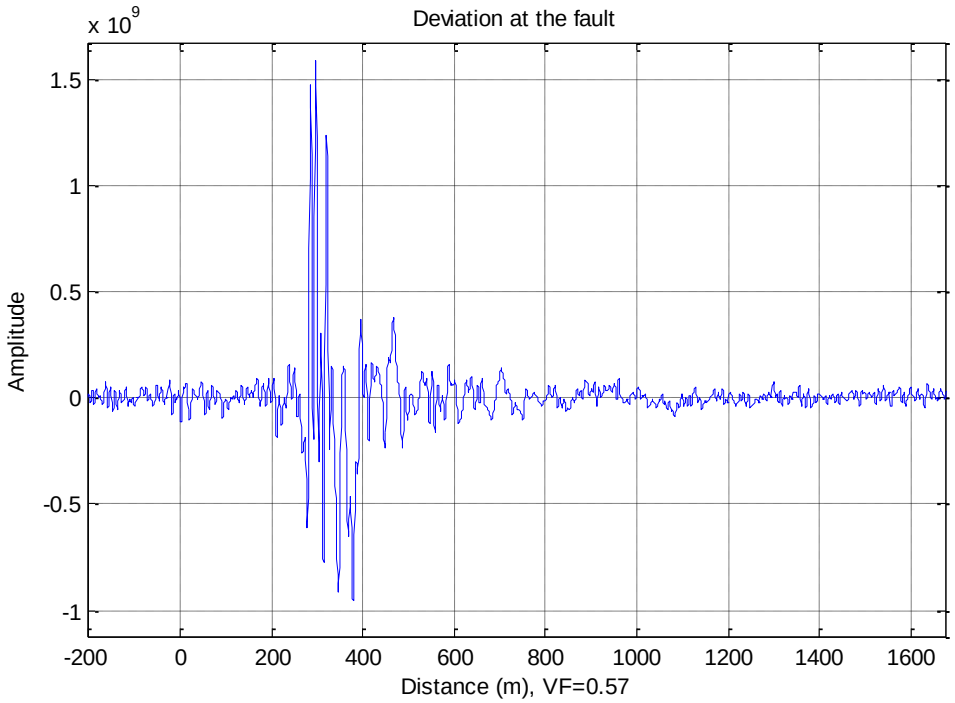


Figure 4-24: The deviation between reference signal and compressed, triggered reflected signal

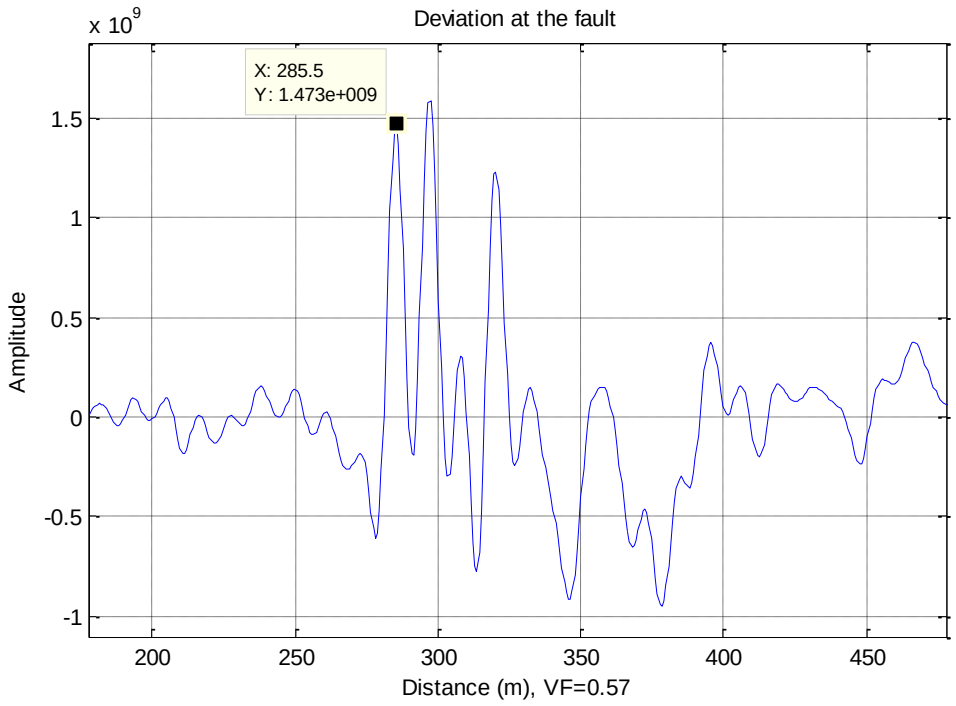


Figure 4-25: The deviation between reference signal and compressed, triggered reflected signal (Zoom in)

4.6 Conclusion

Pulse compression techniques were applied to enhance TDR based cable fault locating techniques, and successful results were obtained. The pulse compression process provides the capability of using longer interrogation pulses to achieve good detection range, while providing range resolution comparable to TDR with shorter pulses. The pulse compression is in fact a correlation process, achieved by matching the characteristics of the interrogation signal from acquired waveforms. Therefore, this algorithm has high immunity to noise, unless the noise character is exactly the same as the interrogation signal. A self-comparing scheme is introduced to monitor the time change of the network electricity connections, depicted by the reflected waveforms. The proposed method, based on pulse compression techniques and a self-

comparing scheme, is discussed and validated on a real underground cable network with transient faults.

The performance of the algorithm was tested in a 240 V underground cable network with an artificial transient fault, created by drilling a small hole to the phase conductor and then exposing to moisture. Accuracy to within 1% error was achieved, demonstrating the robustness of the algorithm, especially when dealing with noisy and complicated TDR networks.

In practical applications, knowledge of the velocity of propagation of the cables installed in the underground network is required; this can be calculated by testing the reflection time using a known length of cable of the same type.

5 Development of Encoded TDR test prototype

5.1 Introduction

This chapter presents a new prototype fault locator (TFM1000) that enables transient fault monitoring and location in live LVUDN. The technical specification and parameters are mainly designed to meet the implementation requirement in Chapter 5. The considerations and motivations of this new prototype fault locator TFM1000 are discussed in section 5.2. In section 5.3, the design of the main subsystems of the TFM1000 prototype are presented and discussed in detail. Section 5.4 shows the hardware design process of the prototype fault locator TFM1000. Details of the firmware and software development then follow in section 5.5 and section 5.6, respectively. In section 5.7, laboratory test results are presented. A summary and conclusions are also given at the end of this chapter.

5.2 Considerations

All TDR systems comprise pulse generation and pulse sampling circuitry. These circuits have a number of variants according to their specified applications. None of the pulse generation circuits of existing cable fault locator systems are applicable for generating an encoded pulse (compressible pulse) for LVUDN. Hence, a totally new design is required to implement the innovative fault locating technique proposed in this thesis. The hardware computing capability of the prototype fault locator

TFM1000 must be robust to meet the computing requirements; however, the full design is desired to be cost-effective.

With the rapid development of semiconductor technology and manufacturing processes, a massive number of transistors on a single chip have become available, thereby giving an integrated circuit more inherent capabilities than before. This allows encoded pulse circuitry in miniaturization and digitization.

A direct digital synthesizer (DDS) is a type of circuitry (or device) used to synthesize arbitrary waveforms from a known reference frequency [70]. High frequency resolution, high amplitude stability in phase change, and fast switch over are the main advantages of the DDS technique [71]. Thus, DDS is chosen as the frequency synthesizer for encoded pulse TDR in this thesis.

Modern developments in the integrated circuit (IC) fabrication process have further lead to successful development in large-scale field-programmable gate arrays (FPGA). As the name implies, “field-programmable” indicates that the designer can customize or configure the FPGA device after manufacturing. Based on the “programmable” property of FPGA, a system-on-chip (SoC) design concept has been developed. SoC serves the objective to integrate all functional components of an electronic system onto a single chip. Compared to systems built with individual functional circuitry, SoC systems post many benefits including significantly reduced size, effective lower costs, high performance in power efficiency, and low EMI. Because the supporting components and wirings for individual functional circuitry are not required, SoC also act to minimize the crosstalk and delaying effect. A SoC combination may also include a processor, an interface, an analogue driver or even a voltage regulator [72] in a single semiconductor die.

FPGA is derived from the combination of programmable read-only memory (PROM) and programmable logic devices (PLD). There is a trend for modern FPGAs to be built with embedded processors for adaption to SoC, this is also known as "system-on-programmable-chip" (SoPC). SoPC may be recognized as a special case of SoC.

An IP core-based (intellectual property core) design concept also comes with SoPC. The "IP core" is a hardware description of logic or data that can be used in FPGA to achieve a specific function. These IP cores may be re-customized to satisfy the requirements of a specified application [73]. A number of IP cores in different functions will be synthesized and assembled together to form a complete SoPC. The most important advantage of the IP core-based SoPC design is that there is no need to redesign the whole system, if a part or some parts of the system are changed. The only requirement is to commit the change to the target IP core and re-synthesize and assemble the system. This makes SoPC design very flexible and efficient. For example, a SoPC is currently driving a motor controller; however, for some reason, only a similar type of motor controller, but with different driving logic, is available. To adopt the new motor controller, only the motor controller IP core needs to be modified, and no other changes are required.

This thesis employed a SoPC system, developed by Altera and based on a Cyclone III FPGA, as the core of the whole encoded pulse TDR system, to complete the main tasks of signal generation, data sampling, data processing, and data storage control.

5.3 System Architecture

5.3.1 General

The system may be split into two major subsystems: digital and analogue. The digital part was mainly incorporated of a central processing unit (CPU) and data storage unit, whilst the baseband signals were processed in the analogue part. The digital world and analogue world are linked together by a digital-to-analogue converter (DAC) [74] and an analogue-to-digital converter (ADC). It should be noted that the DAC/ADC is an analogue component as well as a digital component.

The analogue system block diagram is shown in Figure 5-1. The main components of the analogue system are: ADC for signal digitising and sampling, DAC and reconstruction filter (low pass filter) for analogue waveform generation, balancing circuit and signal routing circuit.

All the data are processed and stored in the digital system; hence the digital system contains a CPU for data processing and some storage element. As shown in Figure 5-2, the elements of the digital system are interconnected by a high speed Avalon MM bus and a low speed SPI bus.

The DAC (AD9779A) has two separated output channels, each channel being connected to a DC offset adjust circuit and a reconstruction low pass filter. The purpose of the reconstruction filter is to remove quantisation noise and construct a smooth analogue signal from the output of the DAC to represent the original desired signal. This is because the output signal of a DAC has a stair step type waveform containing high frequency components, which causes aliasing problems. One of the DAC output channels was unimplemented and reserved as an auxiliary output for future use.

The signal acquisition part contains an LTC2208 ADC and multi-stage amplifying circuit. The first stage amplifier is a unity gain, high bandwidth instrument amplifier. The signal passing the first stage will be attenuated by 20 dB and passed to a variable gain amplifier (VGA); the gain of the VGA is controlled digitally, from -−20 dB to 20 dB. The signal will be passed to a unity gain ADC driver and an anti-aliasing filter, before finally reaching the ADC.

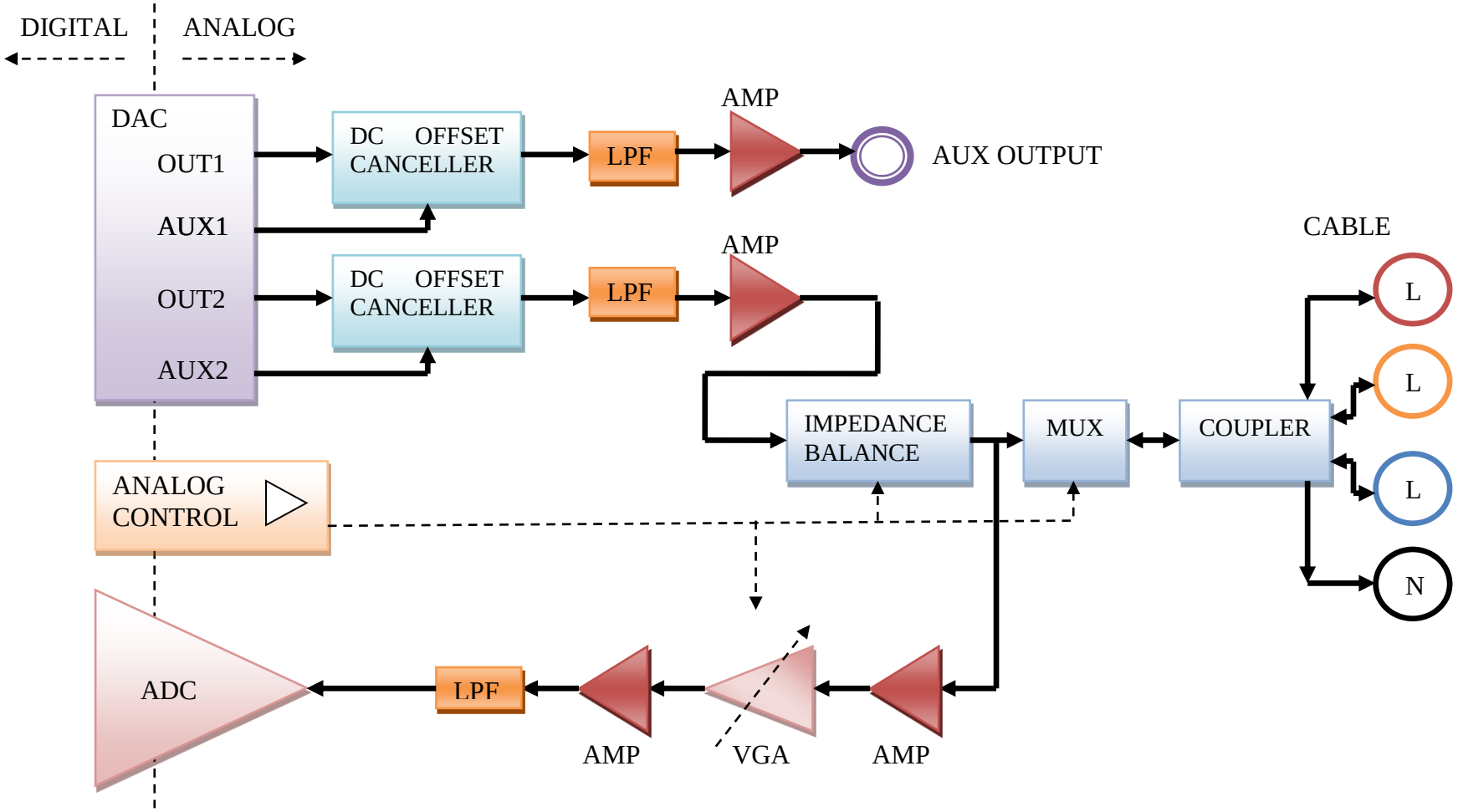


Figure 5-1: Analog subsystems

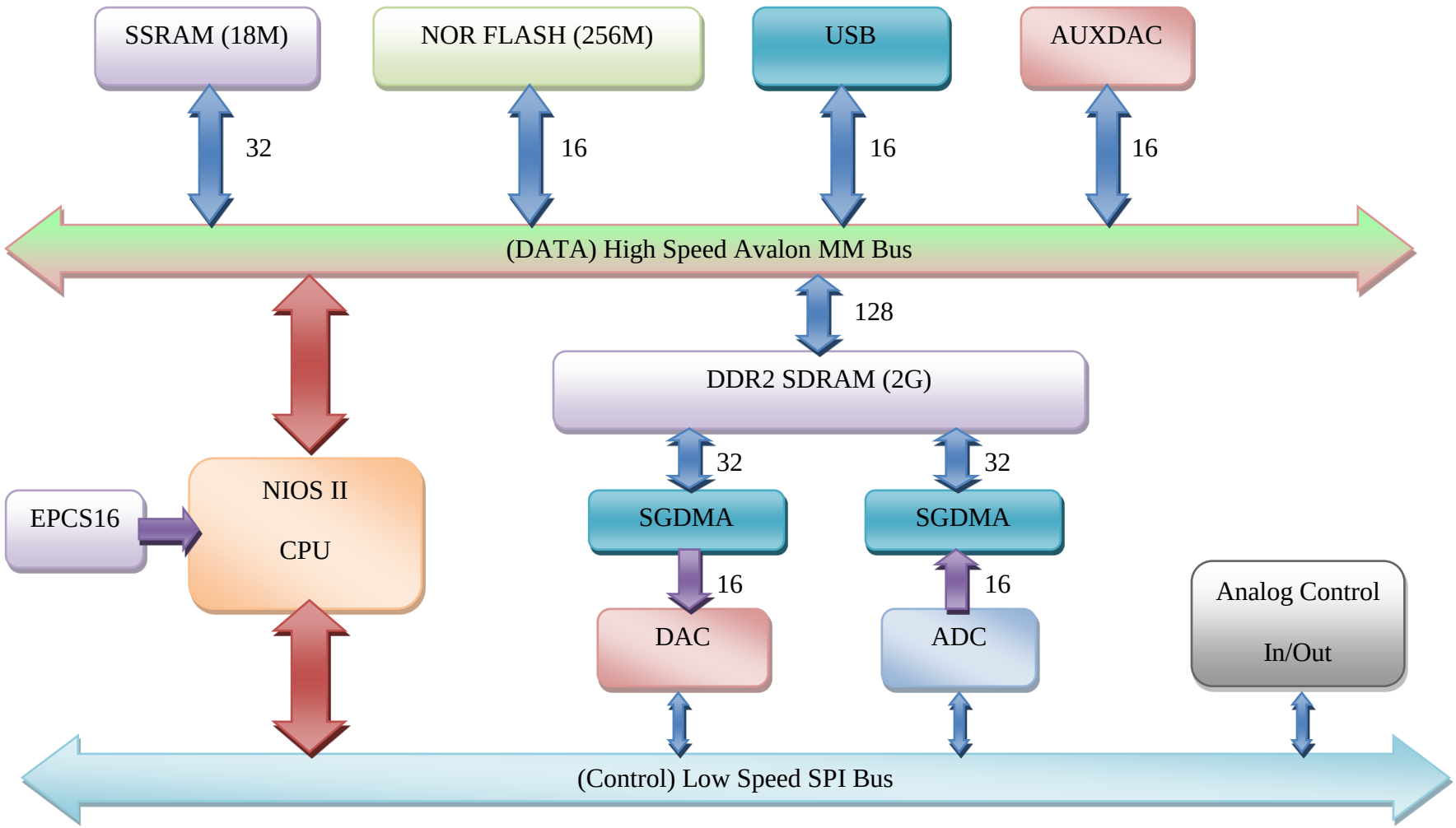


Figure 5-2: Digital subsystems (number represents the bus width)

5.3.2 Acquisition subsystem

The acquisition subsystem is the "eye" and the most important subsystem. The role of the acquisition subsystem includes: conditioning the input analogue signals to a suitable level, and converting the analogue signal to a digital signal.

As shown in Figure 5-3, the acquisition subsystem was designed in a multi-stage structure. The instrument buffer offers a high impedance input. The variable gain amplifier (VGA) scales the signal to a suitable level. The ADC buffer drives an antialiasing filter to prevent the ADC from producing aliasing data.

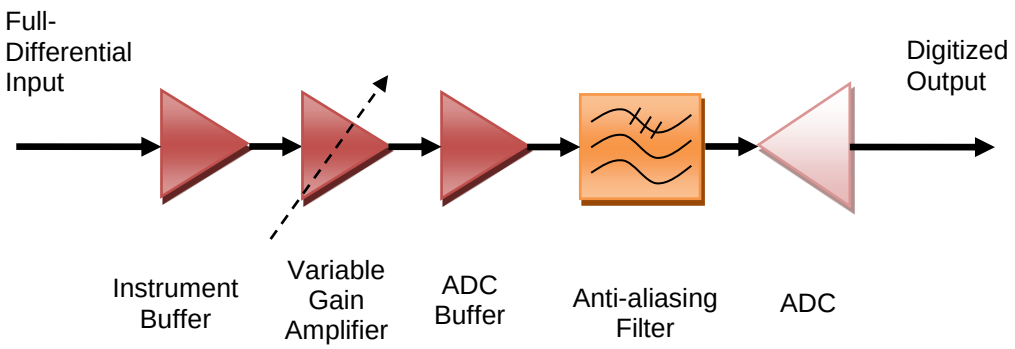


Figure 5-3: Block diagram of acquisition subsystem

5.3.2.1 ADC Selection

An analogue-to-digital converter (ADC) is the core component in the acquisition subsystem. As shown in Figure 5-4, the ADC represents an analogue signal by pre-defined digital voltage levels. The ADC can be classified by converting fundamentals. Every type of ADC has its own advantages and disadvantages, and hence different applications. The popular ADC types in the current market are flash, SAR, and sigma-delta ADCs.

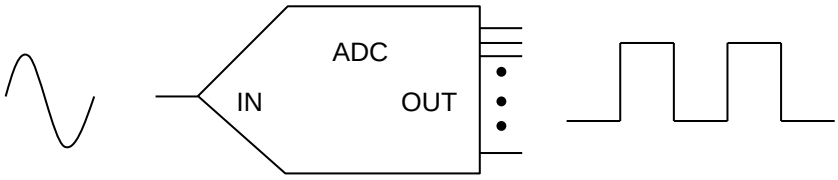


Figure 5-4: Illustration of ADC function

The classification of popular architecture of ADCs is shown in Figure 5-5. According to the expected specifications, the sampling rate is expected to be no lower than 100 MHz, while the resolution is no lower than 16-bit. The suitable ADC architectures are therefore flash ADCs and pipelined ADCs. Other types of ADC are not considered, either due to lack of sampling speed, or low sample resolution.

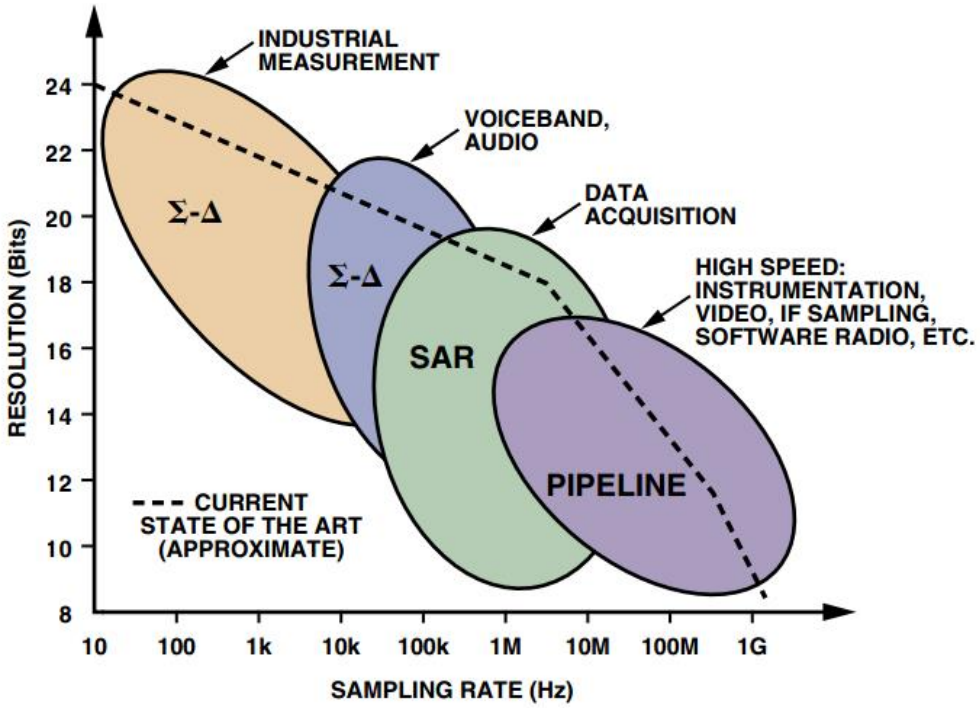


Figure 5-5: Classification of ADC by architectures, application, resolution and sampling rates[75].

Flash ADCs are also known as parallel ADCs; this is the fastest way for signal digitizing [76]. Flash ADCs employ a series of cascading high-speed comparators; each comparator is connected to a resistive-divider for the reference voltage in one

comparison arm, and to the analogue input in the other comparison arm. The conversions for each bit are performed simultaneously, hence the fast sampling speed. However, because the number of the internal precise comparing elements must be increased by a factor of 2 for every extra bit of resolution, it is difficult for a flash ADC to be made in higher resolution than 12-bit. Flash ADCs in this resolution range are normally very expensive and power consuming.

Pipelined ADCs contain a small portion of parallel structure, similar to flash ADCs. Pipelined ADCs divide the whole resolution into several parallel stages, these stages being pipeline-connected to form the final resolution. An example of a pipelined ADC is shown in Figure 5-6. The Max1200 ADC has the 16-bit full resolution divided into 4 stages. Each stage performs only 4 bits of digitizing. The top sampling speed of this architecture cannot be made as fast as flash ADCs, however the pipelined structure eases the manufacturing process, and usually consumes lower power than flash ADC because it requires less precise comparing elements. Most importantly, the pipelined ADC is capable of providing high resolution (≥16-bit), with a good sampling speed (≥100 MSPS).

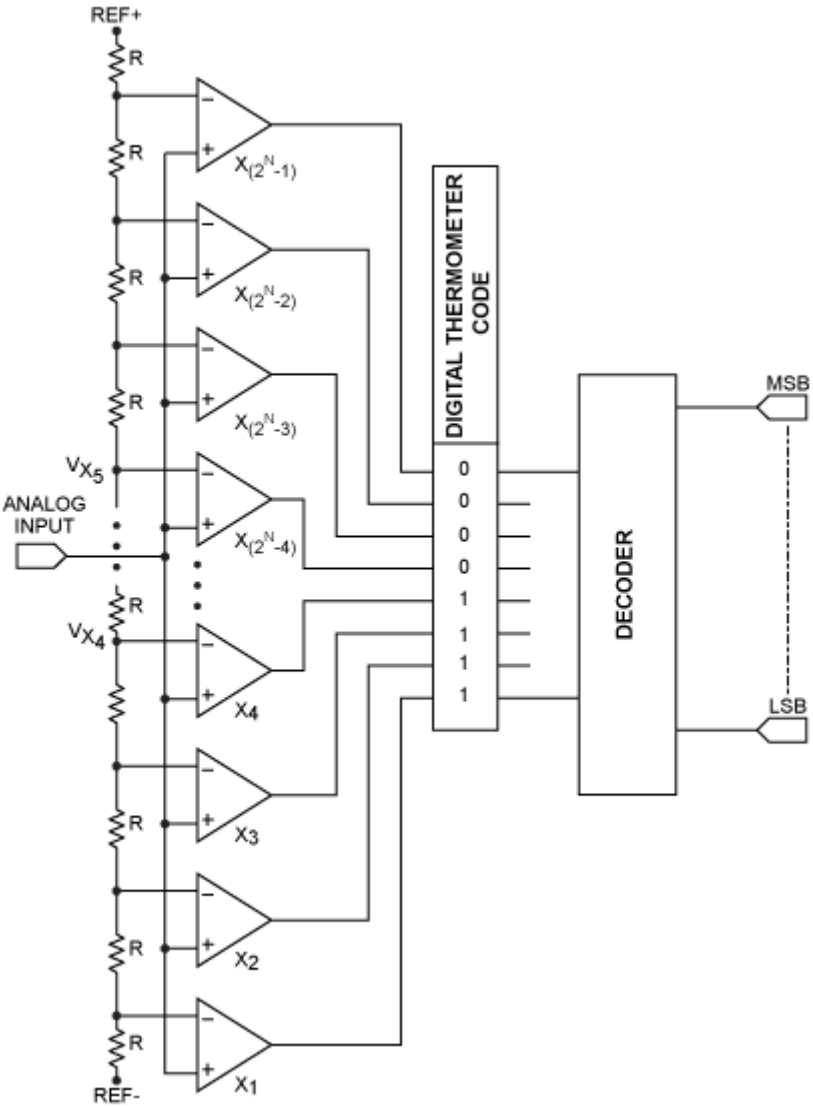


Figure 5-6: Flash ADC Architecture [76].

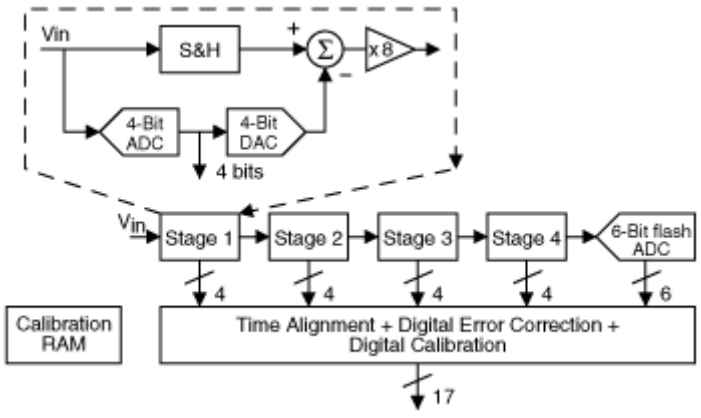


Figure 5-7: Example Architecture of Pipelined ADC[77].

Considering the required specifications, structure and cost, a pipelined ADC, LTC2208 from Linear Technology, was selected as the digitizing component for this project. The specifications of this ADC are well-matched to the project requirements, as summarised in Table 5-1.

Table 5-1: Criteria specifications of LTC2208.

	LTC2208
Analog Input	Fully-Differential Front End
Sampling Rate	Up to 130 MSPS
Resolution	16-bit
-3dB Bandwidth	700 MHz
Power Consumption	Low power dissipation of 1.25W
Other Features	Internal Dither, Programmable Gain, Single 3.3V power supply and wide-range 0.5 to 3.6V logic output level. LVDS and CMOS support. Clock duty cycle stabilizer. Flexible output format: offset binary or two's complement

5.3.2.2 Anti-aliasing Filter

An anti-aliasing filter is a low pass filter for removing the frequency components over the Nyquist frequency before the signal sampler, to satisfy the sampling theorem [78]. The well-known Nyquist frequency is the maximum frequency for non-aliasing sampling in a discrete signal sampling system. This frequency is equal to half of the sampling frequency.

Ideally, the anti-aliasing filter should remove the frequency components higher than the Nyquist frequency from input signals before an ADC. However, this is not practical and not necessary, for two reasons:

1. The analogue low-pass filters have a transition-band (Figure 5-8). This transition-band varies according to structure (type) of filter, but generally smaller transition-band leads to more complex filter structure, and this may distort the input signals.
2. If the input signal only has a small proportion of the overall frequency components over the Nyquist frequency, the aliasing effect is not significant.

Therefore, a two-stage RC low-pass filter is employed as the anti-aliasing filter in this design. The according schematic and characteristic curve are presented in Figure 5-9 and Figure 5-10, respectively.

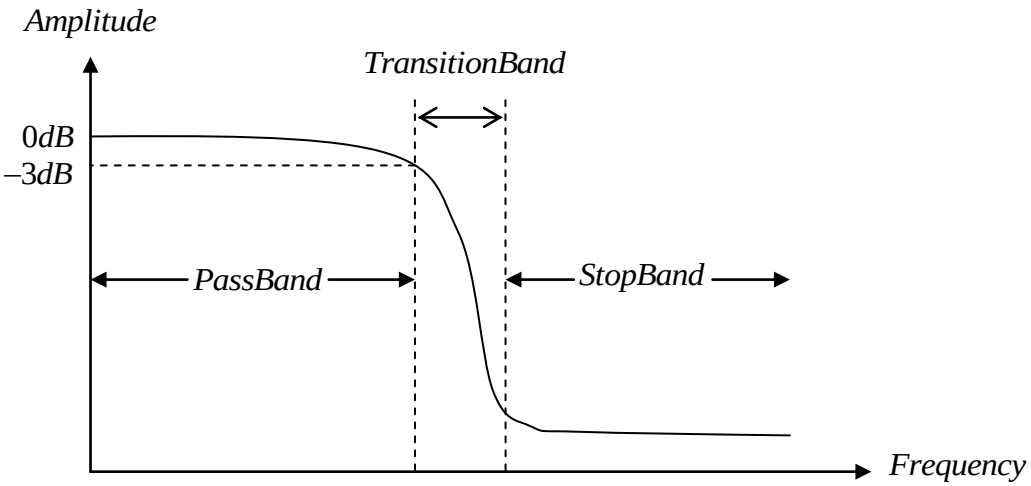


Figure 5-8: The Transfer Curve of Typical Analog Low-pass Filter

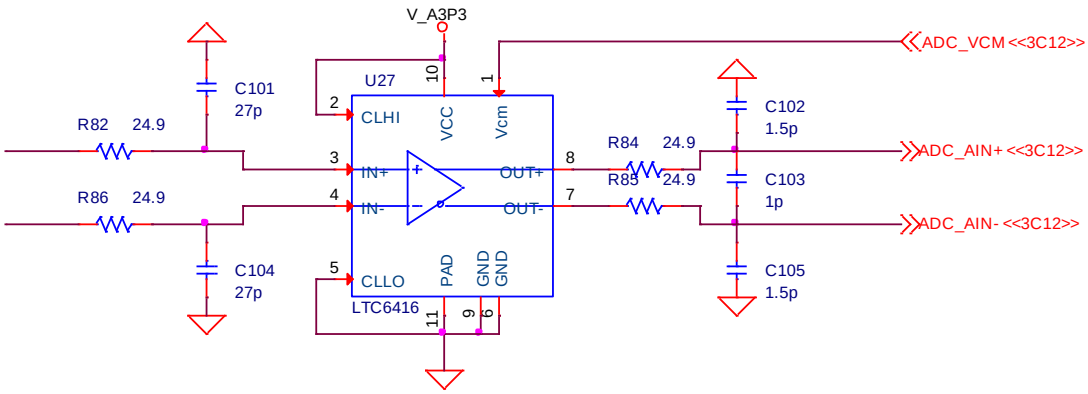


Figure 5-9: Schematic of 2-stage Anti-aliasing Filter

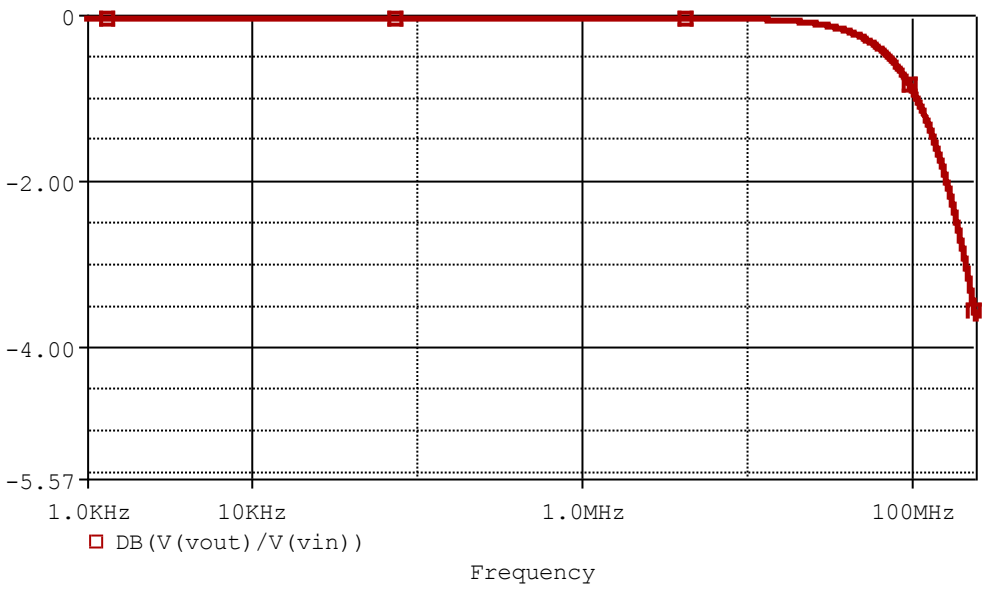


Figure 5-10: Transfer Curve of Anti-aliasing filter

5.3.2.3 ADC Amplifier and Buffers

The design in this thesis employs 3 stages of amplification. The first stage is an instrument amplifier, providing high input impedance and acting as an overvoltage protection. The second stage is a variable-gain amplifier (VGA). The name of VGA is self-explanatory; the VGA can change the gain according to the input levels, whereby the output is able to be maintained at the optimum level. The gain of the VGA is

controlled by two analogue voltage levels, generated by an auxiliary DAC. The last stage is an ADC buffer, working at the same voltage level as the ADC. The ADC buffer serves the purpose of overvoltage clipping, as well as driving the anti-aliasing filter.

5.3.2.3.1 Instrument Amplifier

The instrument amplifier is composited of 3 Operational Amplifiers (OPAMPs). The block diagram is presented in Figure 5-11. It can be seen that the differential inputs are connected to the non-inverting arm of the OPAMP, which generally has input impedance over 100 kΩ. The overall gain of this amplifier is given as:

$$Gain = \frac{Vout}{Vin} = \frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}} = \frac{R2}{R1} \times \left(1 + 2 \times \frac{R5}{R6}\right)$$

Providing that:

$$R1 = R3, R2 = R4, R5 = R7$$

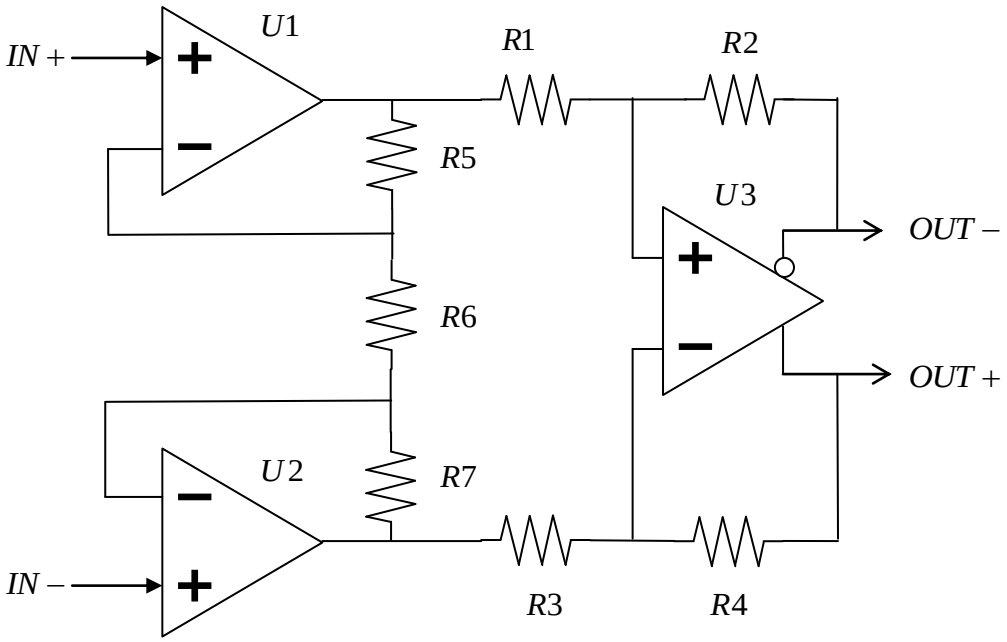


Figure 5-11: Block Diagram of Instrument Amplifier

Type LM6172 and LMH6552 ICs from Texas Instruments were selected to implement the instrument amplifier. The LM6172 is a dual (two OPAMP elements on one chip), high speed, low distortion, voltage feedback amplifier. The LMH6552 is a full-differential high performance amplifier.

The schematic and component values are shown in Figure 5-12, and the specifications of each amplifier stage are listed along with the overall performance in Table 5-2.

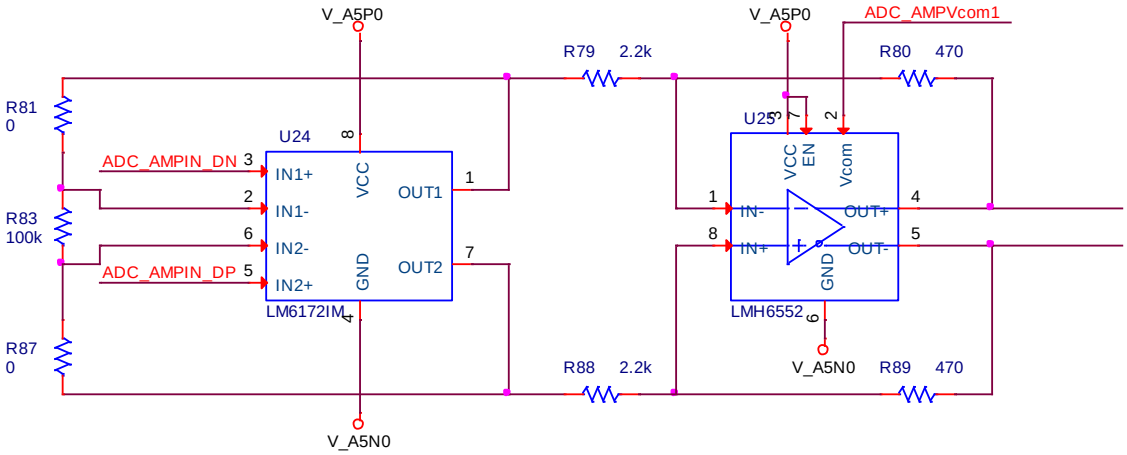


Figure 5-12: Schematic of Instrument Amplifier

Table 5-2: Specifications of Each Stage Instrument Amplifier

	Stage 1	Stage 2	Stage 1+ 2
	LM6172	LMH6552	Overall
Gain	1	0.214	0.214
-3dB Bandwidth	100MHz	1.5GHz	100MHz
Slew Rate	3000V/us	3800V/us	3000V/us
Power Supply	±5V	±5V	-
Output Common Mode Voltage	-	1.6V	1.6V
Input Voltage Range	±3.7V	±3.8V	±3.7V
Output Voltage Swing	-3.3V to +3.4V	±3.8V	-0.70V to +0.72V*
Absolute Output Voltage Level	-	-	+0.90V to +2.32V

5.3.2.3.2 Variable-Gain Amplifier

There is an optimum input range for an ADC. The LTC2208 ADC has an input range of 2.25 V (or 1.5 V with internal PGA on). If the input voltage range is smaller than the optimum level then it suggests that the range resolution is not fully used. For example, if a signal with maximum input range of 1 V was feeding the LTC2208 (16-bit resolution for 2.25 V full input range, PGA off), then the digital output swing would be:

$$DigitaloutputSwing = \frac{1V}{2.25V} \times (0xFFFF + 1) = 0x71C7$$

* Based on Input voltage range, Output voltage swing and Gain.

Where 0*xFFFF* is the maximum output value of the 16-bit ADC in hexadecimal (Hex) format.

As 15 bits are required to represent 0x71C7, this leads to 1-MSB (most significant bit) being unused, and half of the digital output range is wasted. Therefore, the VGA is employed to increase the dynamic output range by amplifying the input signal to a suitable level.

The block diagram of the VGA circuitry is shown in Figure 5-13. The IC selected to implement the VGA is type LTC6412 from Linear Technology. The LTC6412 has maximum 800MHz -3dB bandwidth and gain range from -14dB to +17dB. The gain input of the VGA is connected to the output of a 12-bit DAC, MCP4822 from Microchip. The output voltage of the MCP4822 is configured by an SPI* bus, with range from 0 V to 2.048 V in $2^{12} = 4096$ steps.

Therefore the minimum voltage step is:

$$\Delta V_{DAC} = \frac{2.048V - 0V}{2^{12}} = 5 \times 10^{-4} V$$

The gain control slope of the LTC6412 is typically 32.9 dB/V, resulting in the gain step of the VGA circuitry being:

$$\Delta Gain_{VGA} = 5 \times 10^{-4} V \times 32.9 dB / V = 0.01645 dB$$

* Serial Peripheral Interface, a well-known data protocol developed by Motorola.

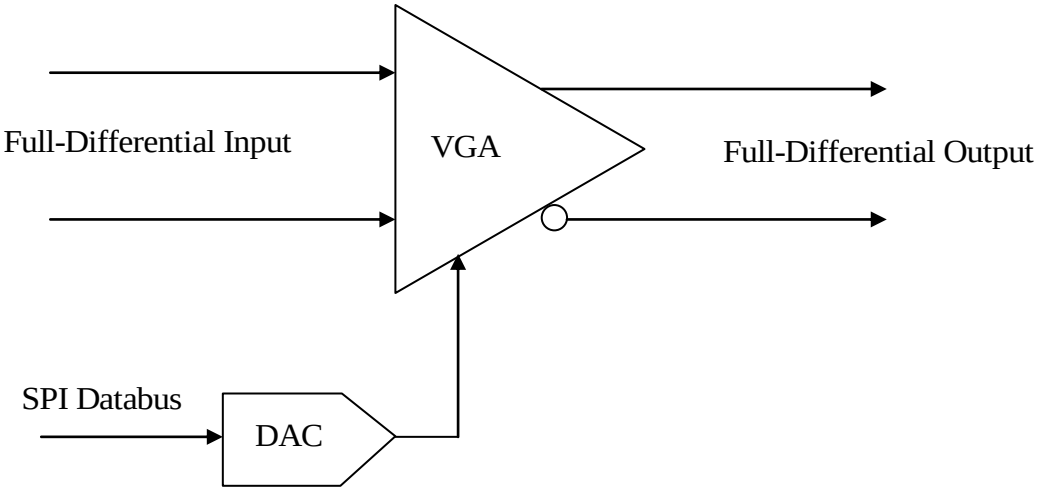


Figure 5-13: Configuration of Variable Gain Amplifier

5.3.2.3.3 ADC Buffer

As mention in section 5.3.2.2, the ADC buffer protects the ADC and filters out the aliasing signal components. The amplifier selected to implement this buffer is type LTC6416 from Linear Technology. The ADC buffer output clipping voltage is set to 0 V to 3.3 V, therefore the input voltage of the ADC will be clamped within the range of 0 V to 3.3 V.

5.3.3 Signal Generation Subsystem

5.3.3.1 Direct Digital Synthesis

Conventional TDR products generally employ a rectangular pulse as the interrogation pulse; therefore the according pulse generation circuitry is simple. However, these rectangular pulse generators are not competent for encoded TDR, because the encoded pulse requires high-bandwidth, precise incident signals for a clear pulse compression process. Direct digital synthesis (DDS) technology is a very suitable method to generate encoded TDR pulses. In short, the DDS technique serves the purpose of frequency- and phase-tuneable signal generation, by using a series of digital data processes that utilise the same reference clock [79]. Figure 5-14 displays a

typical DDS structure. It can be easily understood from the figure that the signal is generated in the digital domain and then converted to an analogue output signal by a DAC. There are two digital inputs to the DDS configuration: the frequency-tuning word M, and the phase-tuning word P.

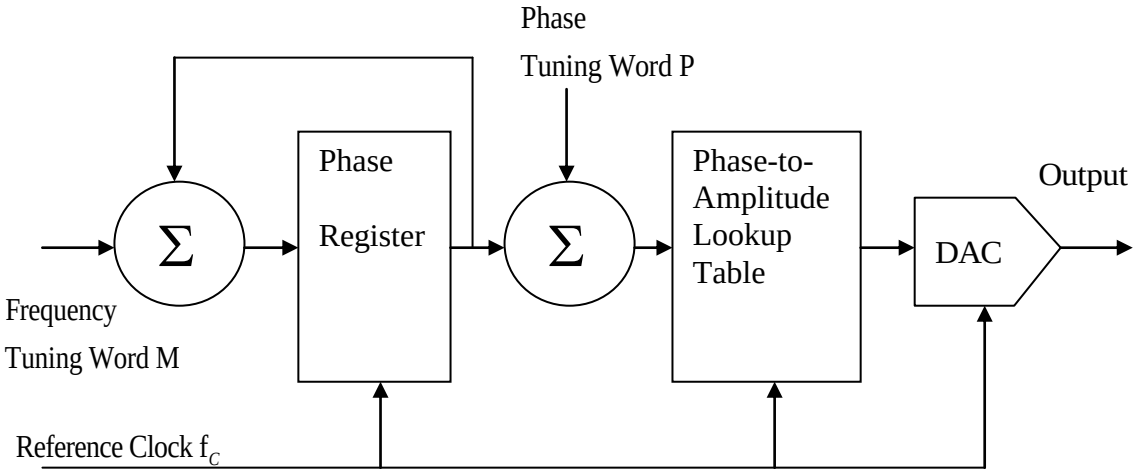


Figure 5-14: A Typical Direct Digital Synthesis

The DDS in the above configuration works as per the following sequence:

1. The DDS controller fills up a full period of the desired output signal to the Phase-to-Amplitude Lookup Table. E.g. if the output signal is a sinusoidal signal with amplitude A, then the table will be filled with a full sine period from 0~2π, with amplitude A.
2. The DDS controller sets the frequency-tuning word M and phase-tuning word P.
3. The DDS controller clocking the whole DDS system by reference clock fc.
4. The phase for every reference clock cycle will be accumulated with frequency tuning world M.
5. The accumulated phase is added with phase tuning word P to work out the current phase.

6. The current phase will be converted to according amplitude and sent to DAC for conversion.
7. During the DDS generation, the controller may alter frequency tuning word M to change the output frequency, or modify phase tuning word P to select the output phase.

It should be noted that the Nyquist rule still applies, that is, the output frequency must not exceed 1/2 of the reference clock frequency.

In considering that the interrogation signal for encoded TDR is of finite length, the accumulating DDS configuration in this thesis is modified and shown in Figure 5-15. Compared with typical DDS, the modifications are:

- The frequency tuning word is fixed to 1
- The phase tuning word P is removed (equivalent to P=0).

Therefore, the phase pointer to the lookup table will move to the next phase because the accumulator has been configured to self-add 1 for the modified DDS. Compared to the typical DDS, this configuration requires a very large size of lookup table, because the information in the lookup table comprises not only a period of the output signal, but rather the whole length of the output signal. This type of configuration is challenging to implement in hardware; however, it can be easily implemented in this case, as the system in this thesis employs a high data throughput FPGA with DSP structure. The detailed implementation is described in the following section in 5.5 <Firmware Development>.

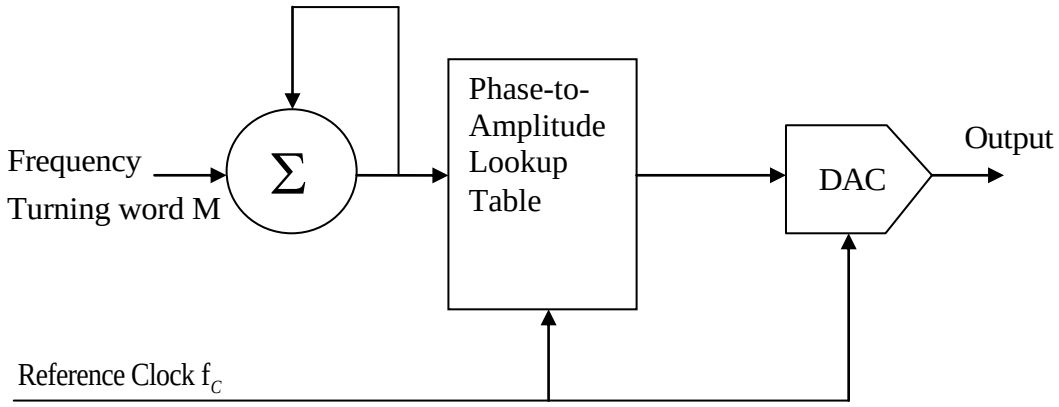


Figure 5-15: Modified DDS for Encoded TDR

5.3.3.2 DAC Selection

The DAC is the most essential part of the signal generation system. Type AD9779A from Analog Devices is an ideal DAC for this application. It has the following key specifications, listed in Table 5-3. An internal functional block diagram is shown in Figure 5-16 for better illustration.

Table 5-3: Key Specifications of AD9779A[80]

Maximum output data rate	1 GSPS (samples per second)
Resolution	16-bit
Output type	Current DAC
No. of Output Channel	2 Channels
Configuration Bus	SPI
Power Consumption	Low power: 1.0 W @ 1 GSPS, 600 mW @ 500 MSPS
Other Key Feature	- Novel digital output interpolator - 2x Auxiliary DAC - Digital inverse sinc filter - High performance PLL clock multiplier - Multi-chip Synchronisation

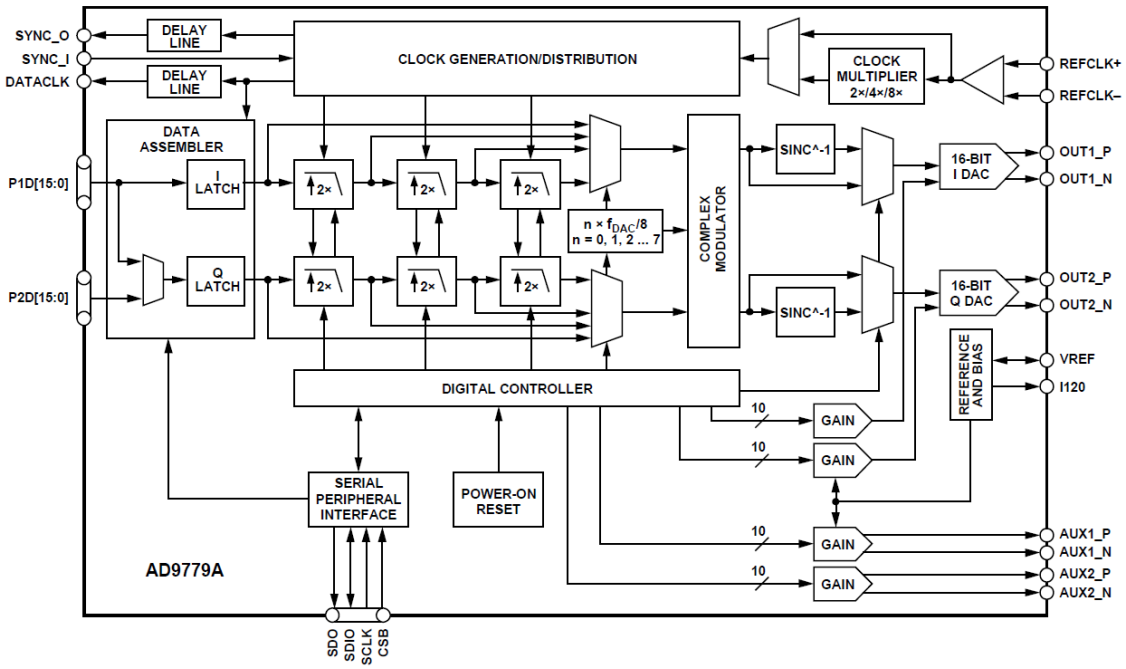


Figure 5-16: Functional Block Diagram of AD9779A

5.3.3.3 Re-construction Filter

As is well-known, the DAC converts a digital number into a physical analogue signal. In the real word, as the digital number always comes with finite-precision, the output of the DAC is also represented by the same precision steps. For example, a 16-bit DAC has $2^{16} = 65536$ digital precisions; hence the output will be represented by 65536 voltage steps throughout the full output dynamic range. The according minimum voltage step can be calculated:

$$\Delta V = \frac{V_{\max} - V_{\min}}{2^{No.ofbits}} \text{ for a voltage output DAC, and}$$

$$\Delta I = \frac{I_{\max} - I_{\min}}{2^{No.ofbits}} \text{ for a current output DAC.}$$

The differences between the desired signal and actual DAC output step are the quantization noise. The quantization noise can be minimised by passing the DAC output through a low-pass filter. The cut-off frequency of the low-pass filter should be set to the maximum frequency of the desired signal.

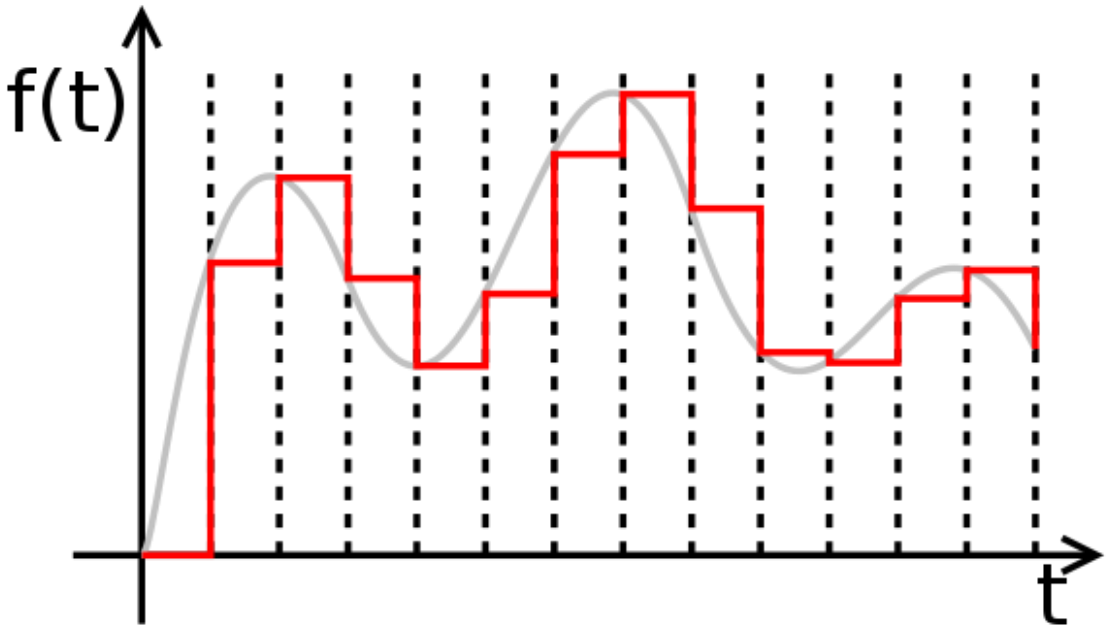


Figure 5-17: Practical Output of An DAC (red) against the desired signal (grey) [81]

The re-construction filter in this design comprises a current-to-voltage convertor and a differential LC filter, as shown in Figure 5-18. Part A is the current-to-voltage convertor for converting the current output of the AD9779A to a voltage signal. The signal will then pass through a low-pass filter in part B to remove the quantization noise.

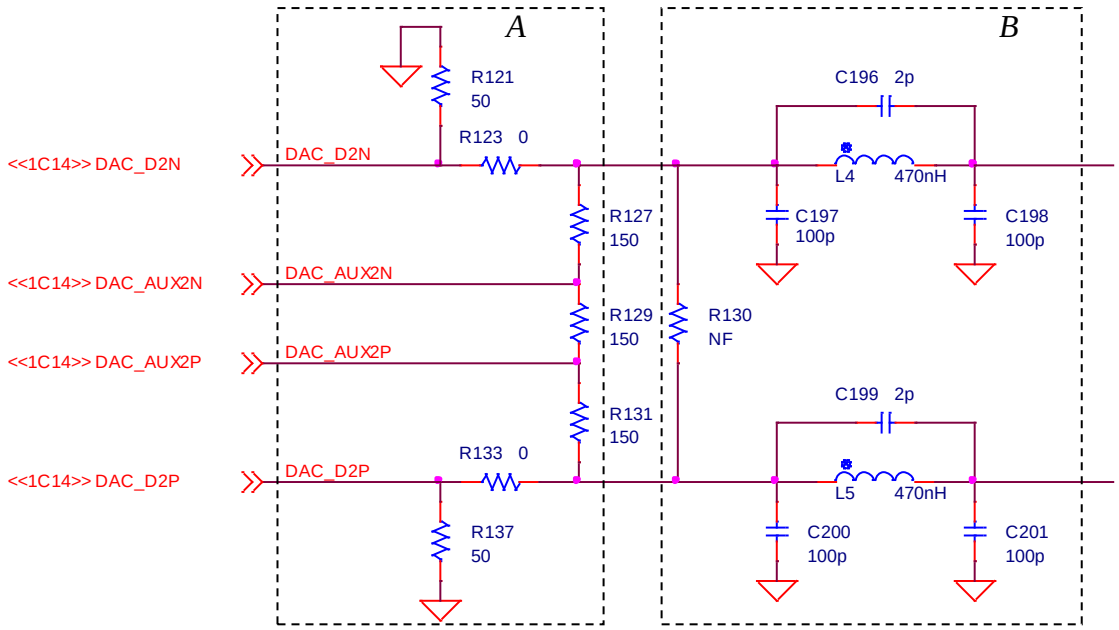
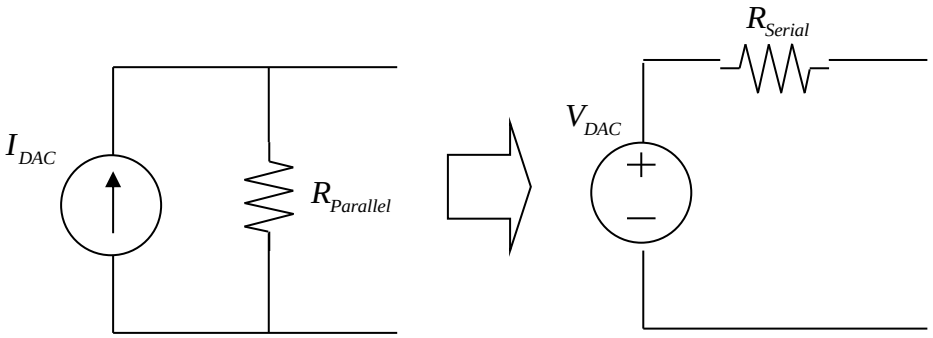


Figure 5-18: The DAC Re-construction filter. A) Current to voltage convertor; B) Differential Low-pass Filter

By applying Thévenin's theorem, the Thévenin equivalent circuit of the output of the DAC is:

$$R_{Serial} = R_{Parallel} = (50+50) \,||\, (150+150+150) = 81.81\Omega$$



The low-pass filter is a Butterworth symmetrical π-network LC filter (e.g. C197, C198 and L4) in parallel with a high pass capacitor (e.g. C196).

The equivalent output impedance of the low-pass filter can be calculated, noting that the input resistance of the DAC amplifier is set to 357 Ω (recommended by manufacturer).

$$R_{equivalent} = (357 + 357) \| 300 = 211.2\Omega$$

The output curve of the DAC re-construction filter is shown in Figure 5-19. The -3dB cut-off frequency is set to 30 MHz.

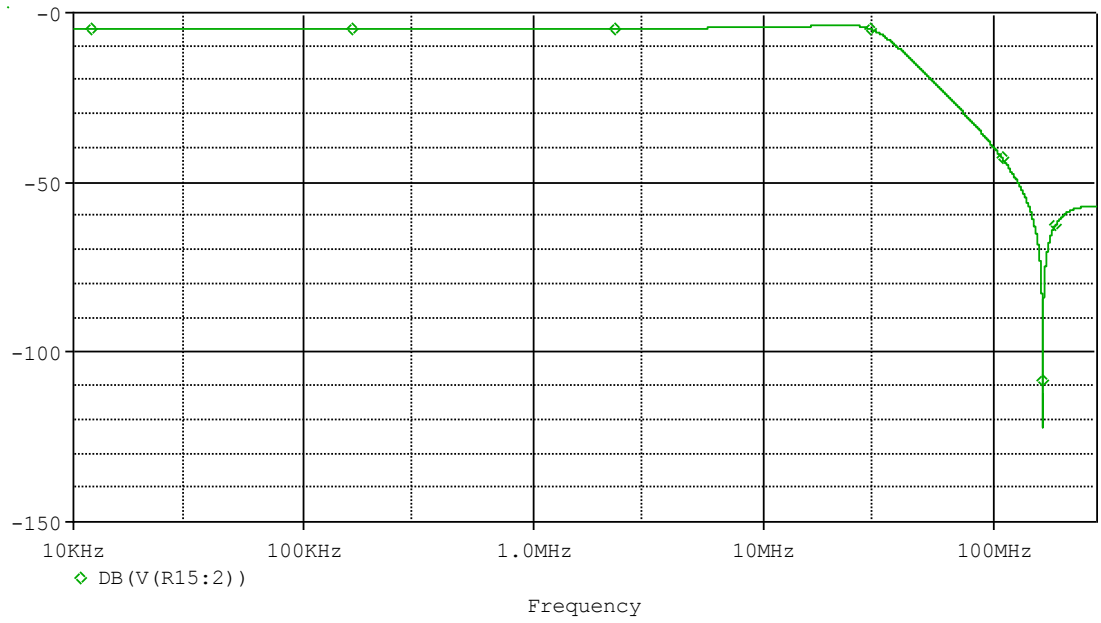


Figure 5-19: Transfer Curve of DAC Re-construction Filter

5.3.3.4 DAC Amplifier

The DAC amplifier provides a low impedance output as well as isolation between the DAC and following circuitry. The LMH6552 IC from National Semiconductor is selected as the DAC Amplifier. The LMH6552 is a 1.5 GHz bandwidth, fully differential OPAMP. The key specifications include:

- 1.5 GHz −3 dB small signal bandwidth (Gain = 1)
- 1.25 GHz −3 dB large signal bandwidth (Gain = 1)
- 800 MHz bandwidth (Gain = 4)
- 450 MHz 0.1 dB flatness
- 3800 V/μs slew rate
- 5 V to 12 V operation

The gain of the DAC amplifier was set to 1, with supply voltage of ±5 V, as shown in Figure 5-20.

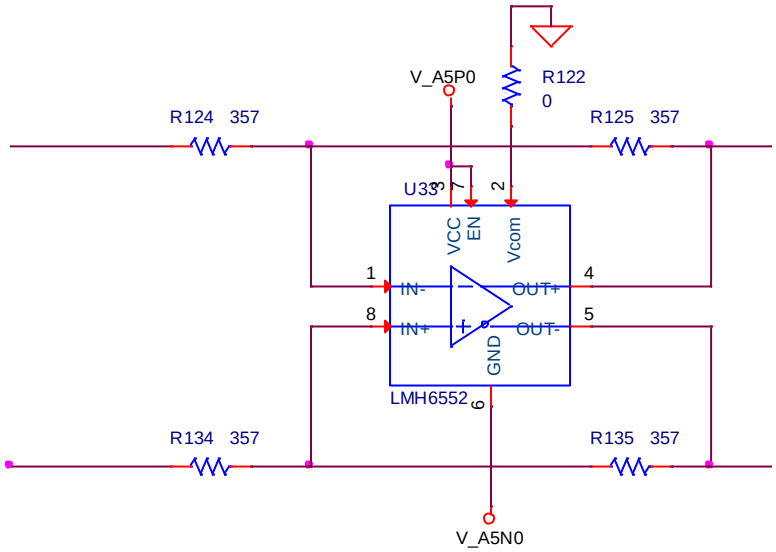


Figure 5-20: Schematic of DAC Amplifier

The schematic of the full DAC re-construction filter can be found in appendix.

5.3.4 Data Storage

The system incorporates 5 types of memory for data storage:

- DDR2 SDRAM
- Synchronized SRAM
- Parallel NOR Flash
- Serial EEPROM
- RAM constructed by logic elements in FPGA (M9K)

Synchronous dynamic random access memory (SDRAM) is a dynamic random access memory (DRAM) where the working frequency is synchronized with the controller; DDR SDRAM is a special SDRAM where its access to the data can occur on both clock edges, hence double data rate (DDR). The numbering after the term “DDR”

indicates the generation. The DDR2 SDRAM is a high-speed, high-capacity memory with high data throughput rate; however, it suffers from high latency because the DRAM requires a refresh process at a certain time interval to prevent the data being lost. The high latency will lead to long delays when initializing a read or write command; this makes the DDR2 SDRAM ideal for large data block transfer.

Synchronized SRAM (static-RAM) comes with similar speed and data throughput as SDRAM. The difference between SRAM and DRAM is that a SRAM is built using a different technique that does not require a refresh process. This will result in a significant cost increase, but with the benefit of low latency. Synchronized SRAM is also called SSRAM. A suitable application for SSRAM is frequent accessing of small data blocks.

M9K is a special type of memory block, integrated in Altera FPGAs. The performance is similar to SRAM, but at higher speed and with flexible accessibility. When compared with other types of memory block, a significant difference is that each M9K memory block has two access ports, as shown in Figure 5-21. The access ports are independent, offering a very flexible configuration. For example, it can be easily configured as a dual-clock FIFO, for interfacing the data between two clock domains.

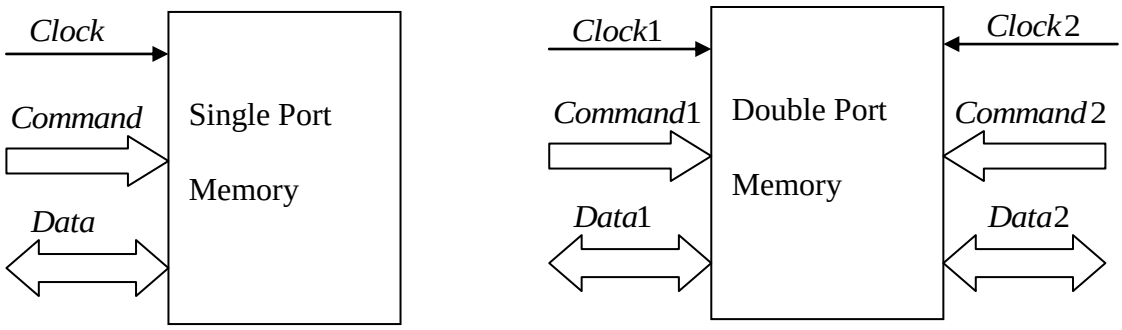


Figure 5-21: Single Port Memory (Left) and Double Port Memory (Right)

Parallel NOR flash and serial EEPROM are non-volatile memories. The information stored in the non-volatile memory is durable, and can generally last for more than 10 years. Parallel NOR flash utilises a parallel data interface, whilst serial EEPROM accesses the data using a serial protocol. These non-volatile memories are used for storing the initializing data (e.g. programs, parameters), or data that would not require frequent access.

The characteristics and part numbers of each memory type are summarised in Table 5-4 for better illustration.

Table 5-4: Compare of 5 types of storage device

Type	DDR2 SDRAM	Synchronized SRAM	M9K (EP3C40)	Parallel NOR Flash	Serial EEPROM
Speed	High	High	Ultra-high	Low	Low
Latency	High	Low	Low	High	High
Data Throughput	High	High	High	Medium	Low
Non-volatile	No	No	No	Yes	Yes
Access Port	Single	Single	Double	Single	Single
Cost	Low	High	-	Low	High
Part Number	43DR16640	GS816032BGT	-	S29GL256P	EPCS16
Manufacturer	ISSI		(Altera)		Altera
Size (bits)	2G	18M	126x9K*	256M	16M
Usage	TDR data, Line voltage, Line current waveform	Processor program, Temporary exchange data	Glue logic within FPGA	Processor program, Initial parameters, Selected data	FPGA configuration

* 126 M9K memory blocks, each M9K has 9kbits, totally 1134kbits.

5.3.5 USB Communication

A reliable and high-speed data communication to the PC is necessary for monitoring the transient event. RS232, parallel LPT and USB are commonly seen in PCs for providing communications. USB is selected as the communication link because of the speed, accessibility and reliability.

A CY7C68013A USB controller from Cypress is chosen for implementation of the USB communication. The CY7C68013 can provide a transfer channel between a PC and FPGA with speed up to 96 MByte/s.

The CY7C68013A incorporates an enhanced 8051 microcontroller, and 4 kB USB FIFO buffer. For maximum throughput and transfer speed, the CY7C68013A is configured to slave FIFO mode. In this mode, the 8051 microcontroller is used for configuring the device, but does not participate in the data transfer. In other words, the data from/to the USB host will be directly transferred to/from the FIFO, as shown in Figure 5-22.

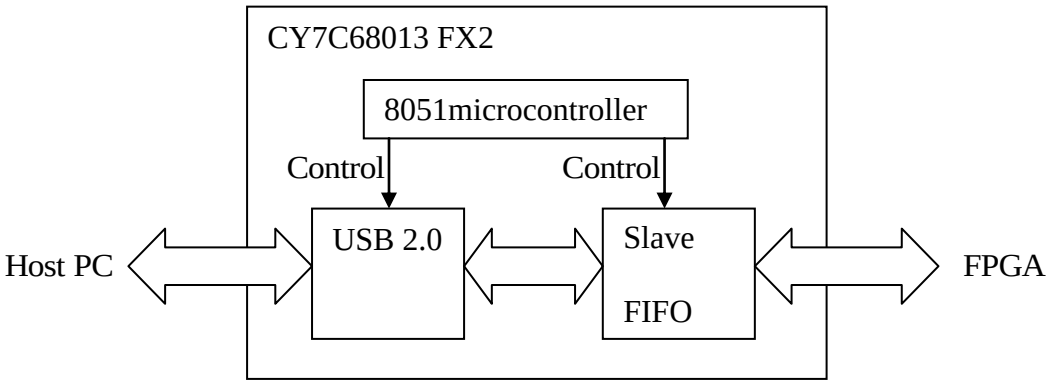


Figure 5-22: Block Diagram of CY7C68013 on Slave FIFO Mode

The signals at the interface of the slave FIFO contain:

- Empty flag output
- Full flag output

- 16-bit bi-directional data bus
- 2-bit FIFO address input
- Synchronized Clock output (48 MHz)

5.3.6 Impedance Balance Bridge

In order to match the impedance of the cable, a variable impedance bridge is placed after the DAC. Since the output is based on differential signals, the impedance is added on both positive and negative arms.

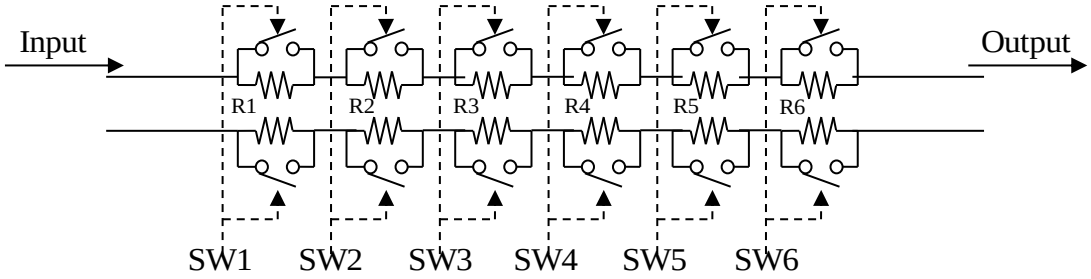


Figure 5-23: Block diagram of Impedance Balance Bridge

There are 6 pairs of resistors connected serially, and each resistor is in parallel with a semiconductor solid-state switch, as shown in Figure 5-23. Each control block contains two switches, which result in very low resistance of the resistor pair when the solid-state switch is in "on-state". This will provide $2^6 = 64$ combinations of resistance. Optimum resistance values are provided in Table 5-5.

Table 5-5: An optimum value of the resistor in impedance balance bridge

Resistor	R1	R2	R3	R4	R5	R6
Value (Ω)	2.000	3.900	8.200	16.00	33.00	65.00

The according results can be illustrated by listing the combinations in Table 5-6, with the plot in Figure 5-24.

All resistors have 0.1% tolerance, with standardized package size code of 0603 (1.6 mm × 0.8 mm).

The switch is implemented with an ASSR-1611-301E opto-isolation, solid-state, bi-directional switch from Avago Technologies. The typical turn-on resistance is 65 mΩ.

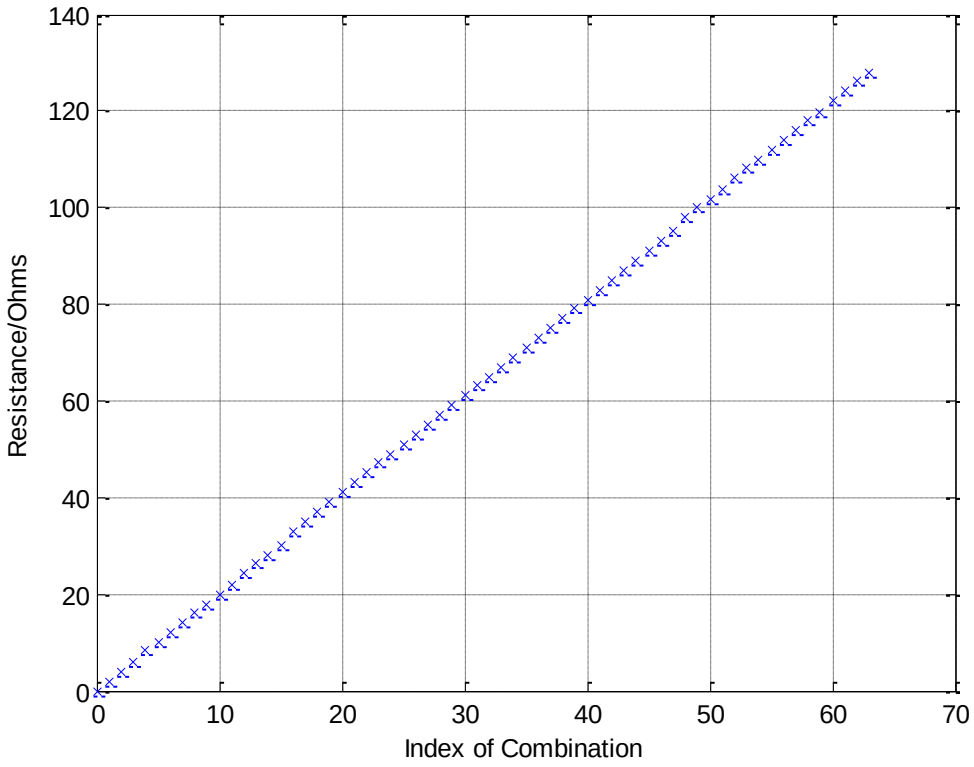


Figure 5-24: Combination plot of the balance impedance bridge

Table 5-6: Combination of the resistor value in impedance balance bridge

Index	SW1	SW2	SW3	SW4	SW5	SW6	Resistance
1	ON	ON	ON	ON	ON	ON	0
2	OFF	ON	ON	ON	ON	ON	2
3	ON	OFF	ON	ON	ON	ON	3.9
4	OFF	OFF	ON	ON	ON	ON	5.9
5	ON	ON	OFF	ON	ON	ON	8.2
6	OFF	ON	OFF	ON	ON	ON	10.2
7	ON	OFF	OFF	ON	ON	ON	12.1
8	OFF	OFF	OFF	ON	ON	ON	14.1
9	ON	ON	ON	OFF	ON	ON	16
10	OFF	ON	ON	OFF	ON	ON	18
11	ON	OFF	ON	OFF	ON	ON	19.9
12	OFF	OFF	ON	OFF	ON	ON	21.9
13	ON	ON	OFF	OFF	ON	ON	24.2
14	OFF	ON	OFF	OFF	ON	ON	26.2
15	ON	OFF	OFF	OFF	ON	ON	28.1
16	OFF	OFF	OFF	OFF	ON	ON	30.1
17	ON	ON	ON	ON	OFF	ON	33
18	OFF	ON	ON	ON	OFF	ON	35
19	ON	OFF	ON	ON	OFF	ON	36.9
20	OFF	OFF	ON	ON	OFF	ON	38.9
21	ON	ON	OFF	ON	OFF	ON	41.2
22	OFF	ON	OFF	ON	OFF	ON	43.2
23	ON	OFF	OFF	ON	OFF	ON	45.1
24	OFF	OFF	OFF	ON	OFF	ON	47.1
25	ON	ON	ON	OFF	OFF	ON	49
26	OFF	ON	ON	OFF	OFF	ON	51
27	ON	OFF	ON	OFF	OFF	ON	52.9
28	OFF	OFF	ON	OFF	OFF	ON	54.9
29	ON	ON	OFF	OFF	OFF	ON	57.2
30	OFF	ON	OFF	OFF	OFF	ON	59.2
31	ON	OFF	OFF	OFF	OFF	ON	61.1
32	OFF	OFF	OFF	OFF	OFF	ON	63.1
33	ON	ON	ON	ON	ON	OFF	65
34	OFF	ON	ON	ON	ON	OFF	67
35	ON	OFF	ON	ON	ON	OFF	68.9
36	OFF	OFF	ON	ON	ON	OFF	70.9
37	ON	ON	OFF	ON	ON	OFF	73.2
38	OFF	ON	OFF	ON	ON	OFF	75.2
39	ON	OFF	OFF	ON	ON	OFF	77.1
40	OFF	OFF	OFF	ON	ON	OFF	79.1
41	ON	ON	ON	OFF	ON	OFF	81
42	OFF	ON	ON	OFF	ON	OFF	83
43	ON	OFF	ON	OFF	ON	OFF	84.9
44	OFF	OFF	ON	OFF	ON	OFF	86.9
45	ON	ON	OFF	OFF	ON	OFF	89.2
46	OFF	ON	OFF	OFF	ON	OFF	91.2
47	ON	OFF	OFF	OFF	ON	OFF	93.1
48	OFF	OFF	OFF	OFF	ON	OFF	95.1
49	ON	ON	ON	ON	OFF	OFF	98
50	OFF	ON	ON	ON	OFF	OFF	100
51	ON	OFF	ON	ON	OFF	OFF	101.9
52	OFF	OFF	ON	ON	OFF	OFF	103.9
53	ON	ON	OFF	ON	OFF	OFF	106.2
54	OFF	ON	OFF	ON	OFF	OFF	108.2
55	ON	OFF	OFF	ON	OFF	OFF	110.1
56	OFF	OFF	OFF	ON	OFF	OFF	112.1
57	ON	ON	ON	OFF	OFF	OFF	114
58	OFF	ON	ON	OFF	OFF	OFF	116
59	ON	OFF	ON	OFF	OFF	OFF	117.9
60	OFF	OFF	ON	OFF	OFF	OFF	119.9
61	ON	ON	OFF	OFF	OFF	OFF	122.2
62	OFF	ON	OFF	OFF	OFF	OFF	124.2
63	ON	OFF	OFF	OFF	OFF	OFF	126.1
64	OFF	OFF	OFF	OFF	OFF	OFF	128.1

5.3.7 Input/Output

The TDR testing is based on two wires. A routing matrix is introduced for selecting the pair under test from all possible combinations, in case the system under test contains multiple-conductor cables. Rather than directly connect to a pair of cables under test, the prototype in this thesis utilises a coupler to allow high frequency signals (e.g. interrogation pulse) to pass to/from the cable under test. The coupler also provides an attenuated output to the instrument for monitoring low frequency voltage signals (e.g. 50 Hz voltage waveform).

5.3.7.1 I/O Matrix

The I/O Matrix can select all possible pairs from power systems with up to 4 conductors. The block diagram is shown in Figure 4-25.

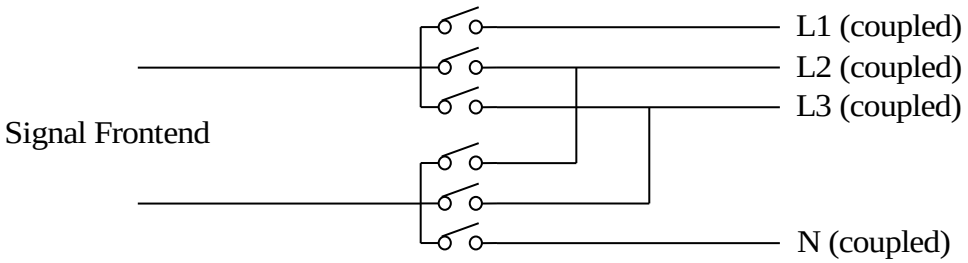


Figure 5-25: Block Diagram IO Routing Matrix

5.3.7.2 I/O High Voltage Coupling

A high voltage coupling circuit is used for interfacing the low voltage TDR transceiver to power systems. As the power system may be energized, the coupling circuit should:

- present low resistance to high frequency interrogation signals.
- present high resistance (high attenuation) to low frequency mains voltage.

The coupler is implemented using a RC high-pass configuration. The schematic of a single phase coupler is displayed in Figure 5-26. It can be easily understood that the voltage drop of the coupler is (assuming the high voltage side is the input):

$$V_{OUT} = V_{R3} = V_{IN} \times \frac{R3}{R3 + (\frac{1}{j\omega C1} \| R1) + (\frac{1}{j\omega C2} \| R2)}$$

And the through impedance to a differential signal is:

$$Z = (\frac{1}{j\omega C1} \| R1) + (\frac{1}{j\omega C2} \| R2)$$

Where ω is the signal frequency in radians.

By assigning R1 = R2 = 1MΩ, C1 = C2 = 10nF, R3 = 500Ω:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R3}{R3 + (\frac{1}{j\omega C1} \| R1) + (\frac{1}{j\omega C2} \| R2)} \approx 2.5 \times 10^{-4}$$

And through impedance:

$$Z \approx \begin{cases} 15\Omega \text{ on } 1\text{MHz} \\ 1.6\Omega \text{ on } 10\text{MHz} \\ 0.8\Omega \text{ on } 20\text{MHz} \end{cases}$$

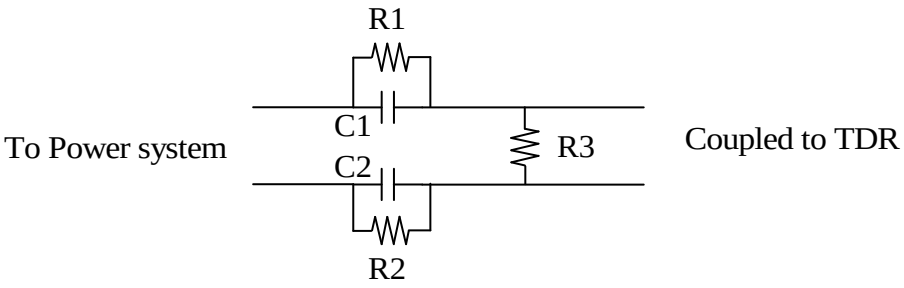


Figure 5-26: The Schematic of Single Phase Coupler

5.3.8 Power Conversion

Considering the fault location system in this thesis may be deployed in an extreme environment, the power input is designed to take a wide range of supply voltage. A conversion map is shown in

Figure 5-27. The power supplies to the digital circuitry and to the analogue circuitry are separated by an LC filter. The LC filter will prevent voltage spikes in the digital circuit, due to rapid change of logic (voltage) level, from entering the analogue circuit.

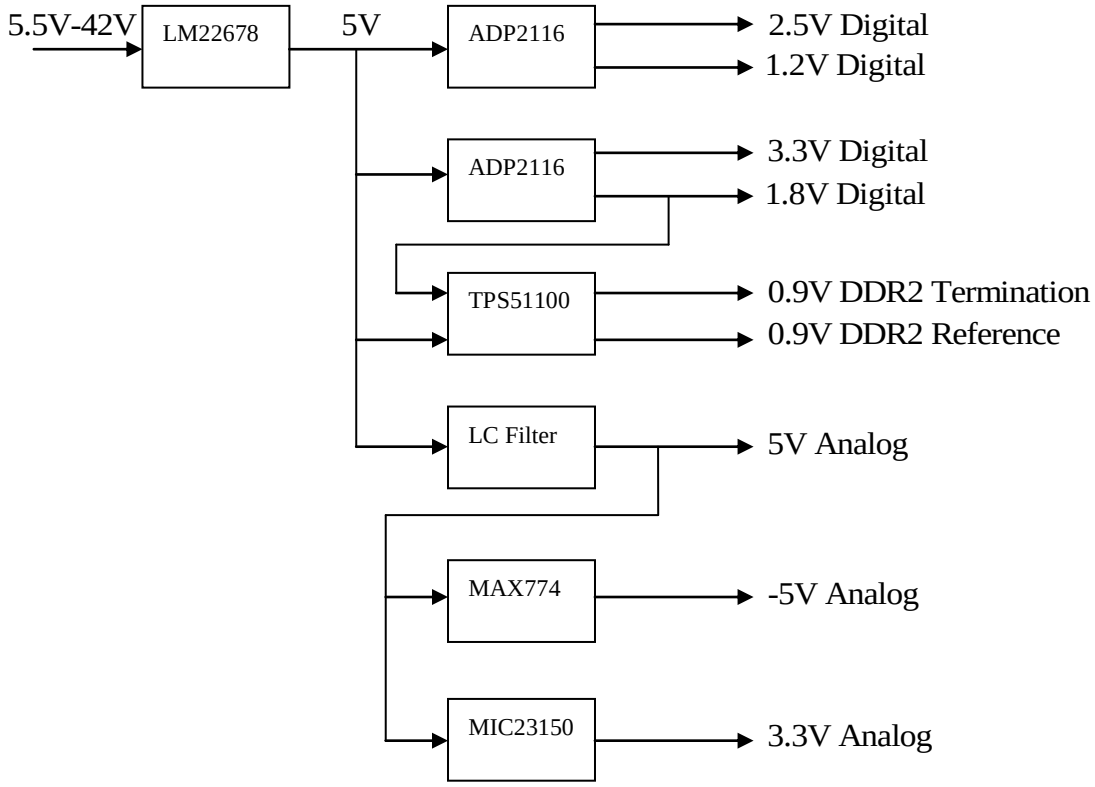


Figure 5-27: Power Conversion Configuration

5.4 Hardware Development

5.4.1 General

The hardware is one of the most important parts of this research. The design can be divided into 3 stages:

- Schematic Design: Split the ideas into small parts and source appropriate electronic devices/components for implementation. Then create logic connection between the devices/components. The connection logic is also commonly known as Netlist.
- PCB Layout: According to the dimensions of all electronic components, create a printed circuit board based on the netlist.
- Assemble: Populate the components to a PCB board and use a method to fix the electronic connections (which is mainly soldering).

The computer aided design package used for the hardware development is Cadence Allegro, version 16.5.

5.4.2 Schematic

The schematics were created from ascent hierarchy to descent hierarchy. A schematic logic map can be used to represent the hierarchy. The detailed schematic can be found in appendix 9.2.

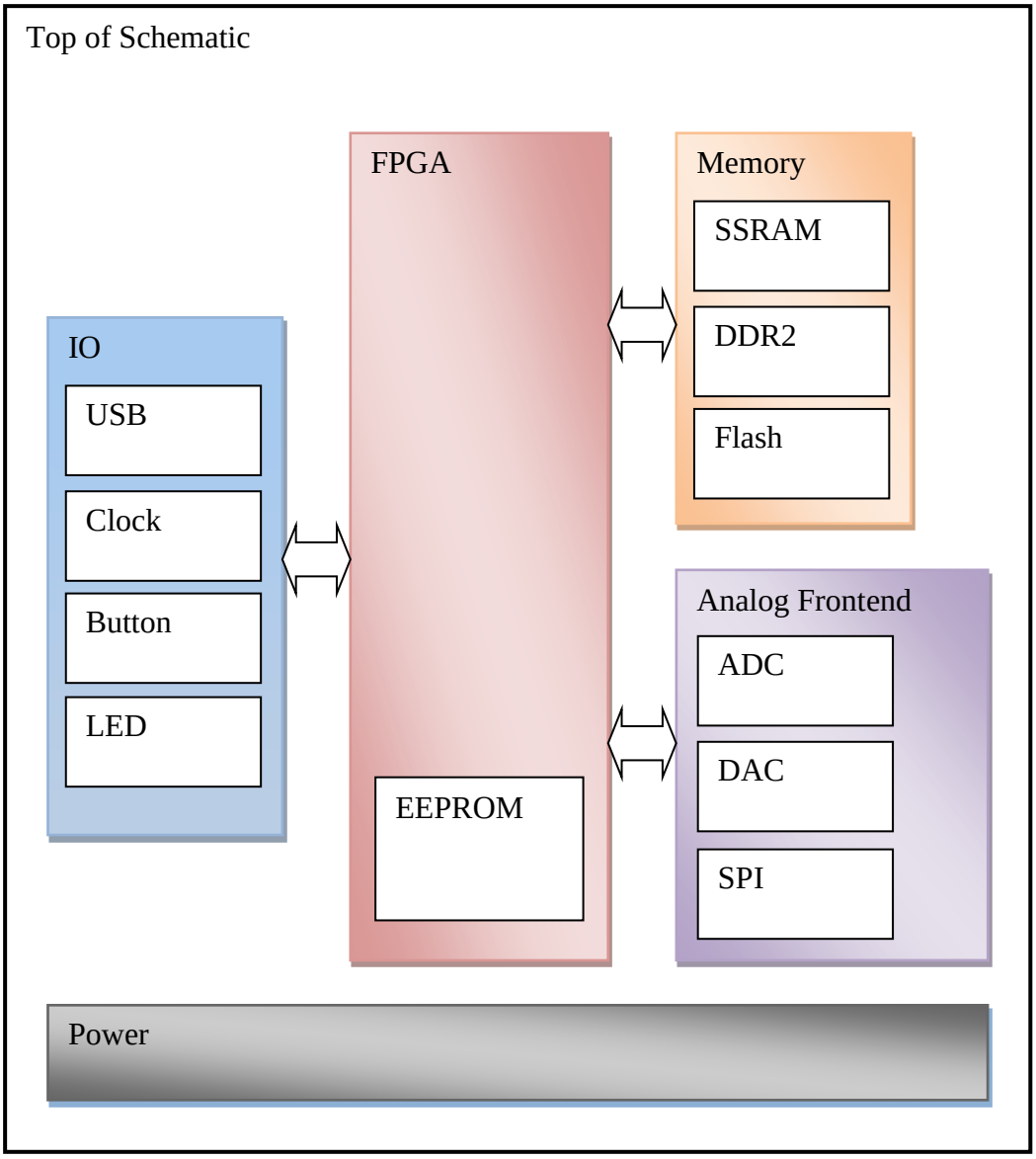


Figure 5-28: The hierarchy of schematic

5.4.3 PCB Layout

To ensure that the hardware implementation precisely follows the design specifications, several practical precautions and constraints were applied:

- Minimum distance between differential signals and other signals: 0.254mm
- Maximum difference in a differential pair: 0.127mm
- Minimum trace width: 0.1mm
- Minimum copper distance: 0.1mm

- All traces to DDR2 memory are of equal length.

The PCB was designed to be a 6-layer structure, with FR4 as the dielectric. In the interest of cost reduction, there are no buried or blind vias. The layer configuration is shown in Figure 5-29. The layout plan on each layer is:

- TOP: High speed signals
- GND: Ground plane, all ground signals were connected to this plane
- S1, S2: Mid-speed to low speed signals, auxiliary signals
- POWER: Power plane, all power signals were route within this plane
- BOTTOM: High speed signals.

	Subclass Name	Type	Material	Thickness (MM)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MM)
1		SURFACE	AIR			1	0			
2	TOP	CONDUCTOR	COPPER	0.035	595900	4.5	0	☐		0.1300
3		DIELECTRIC	FR-4	0.358	0	4.5	0.035			
4	GND	PLANE	COPPER	0.035	595900	4.5	0.035	☒	☒	
5		DIELECTRIC	FR-4	0.358	0	4.5	0.035			
6	S1	CONDUCTOR	COPPER	0.035	595900	4.5	0.035	☐		0.1300
7		DIELECTRIC	FR-4	0.358	0	4.5	0.035			
8	S2	CONDUCTOR	COPPER	0.035	595900	4.5	0.035	☐		0.1300
9		DIELECTRIC	FR-4	0.358	0	4.5	0.035			
10	POWER	PLANE	COPPER	0.035	595900	4.5	0.035	☒	☒	
11		DIELECTRIC	FR-4	0.358	0	4.5	0.035			
12	BOTTOM	CONDUCTOR	COPPER	0.035	595900	4.5	0	☐		0.1300
13		SURFACE	AIR			1	0			

Figure 5-29: The Layer Configuration of PCB

The final dimensions of the PCB were 240 mm × 130 mm, thickness 2.0 mm. The component layout plan is shown in Figure 5-30. A transparent overview of the layout is also displayed in Figure 5-31. A picture of the final PCB is shown in Figure 5-32.

<table>
<tr><td colspan="2">USB</td><td colspan="3">Power</td><td rowspan="4"></td></tr>
<tr><td rowspan="2">JTAG
EEPROM</td><td rowspan="2">FPGA</td><td rowspan="2">DAC</td><td rowspan="2">Signal Generation</td></tr>
<tr><td rowspan="2">SSRAM</td></tr>
<tr><td rowspan="2">FLASH</td><td rowspan="2">DDR2</td><td rowspan="2">ADC</td><td rowspan="2">Acquisition</td><td rowspan="2">Routing and
Coupling</td></tr>
</table>

Figure 5-30: The PCB Layout Plan by functional areas

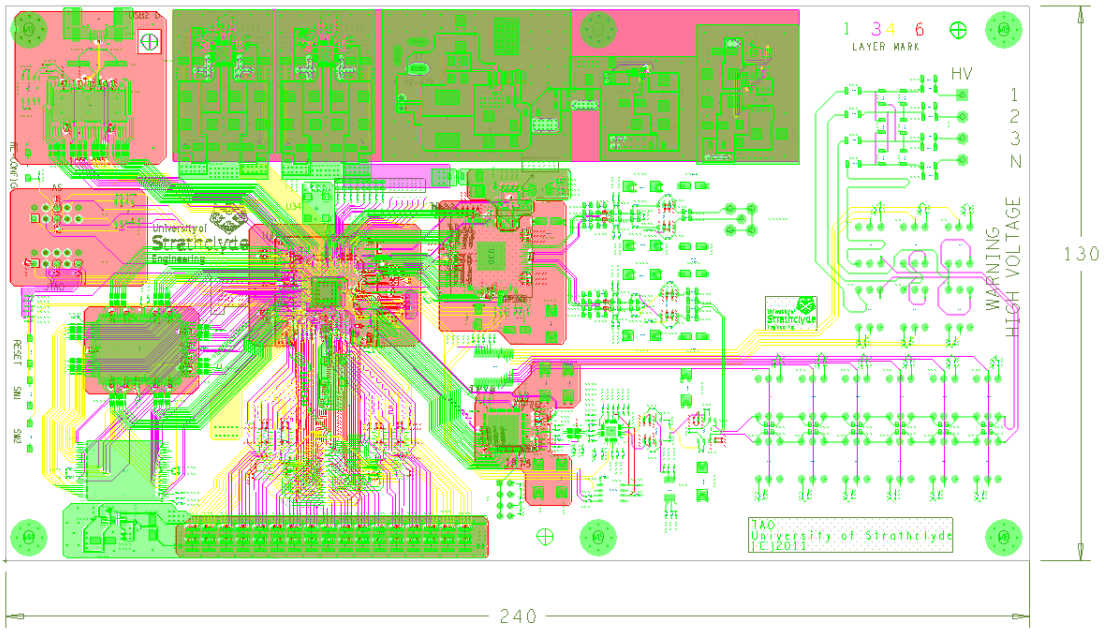


Figure 5-31: A Transparent Overview of PCB Layout

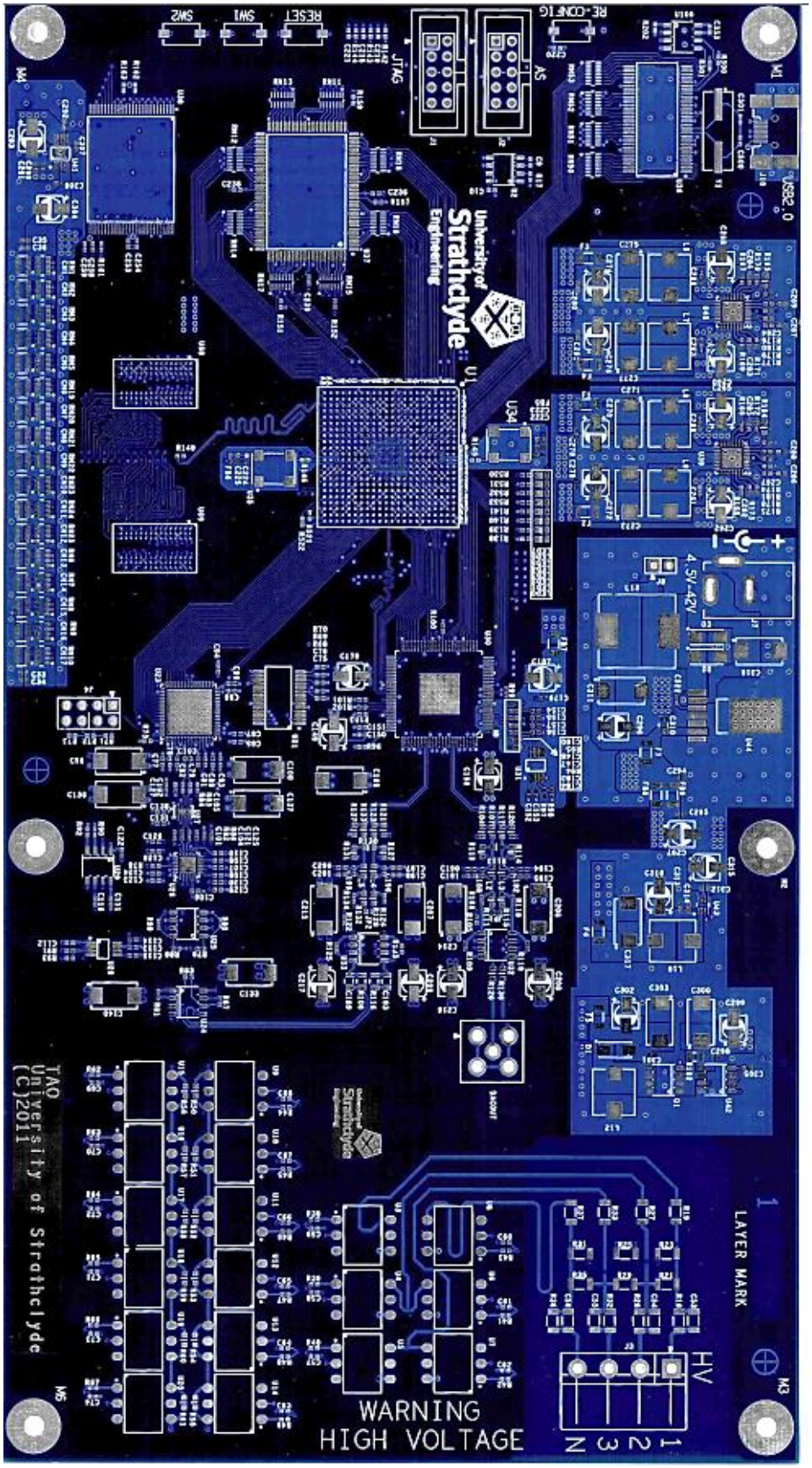


Figure 5-32: Final PCB

5.4.4 Assembling

All components were manually populated and soldered to the PCB by the author. Figures 4-33 and 4-34 show the finished PCB. An enclosure was also made, with ventilation fan and connector lead, as shown in Figures 4-35 and 4-36.

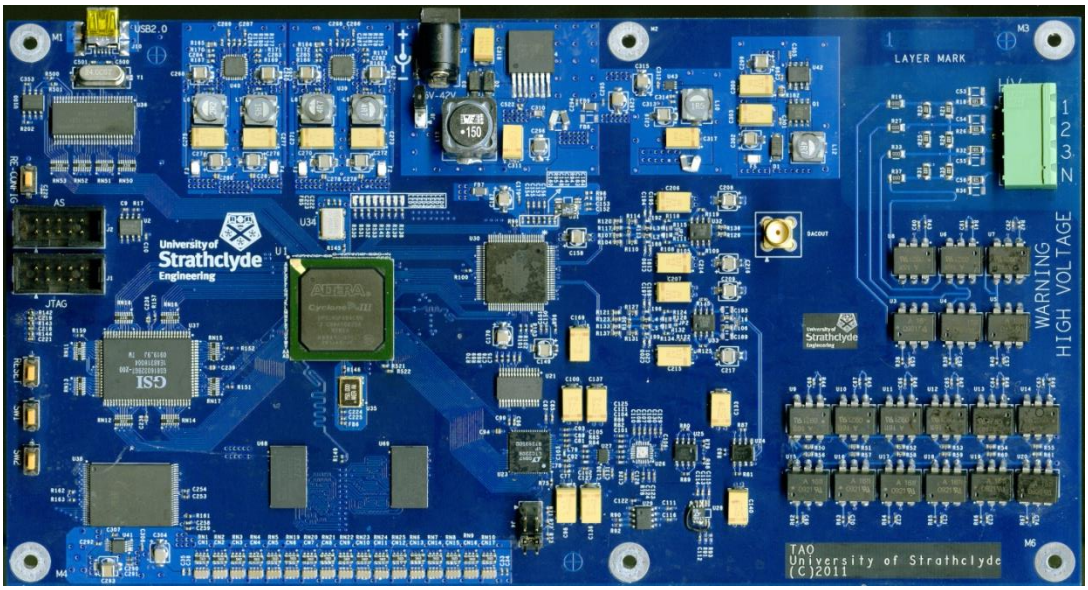


Figure 5-33: The assembled PCB (front)

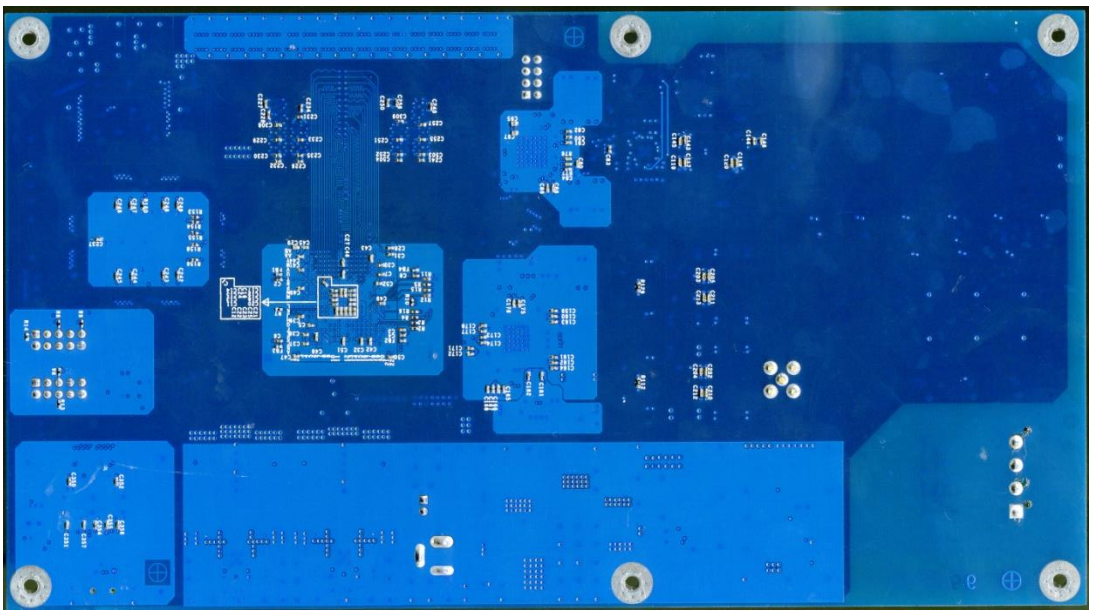


Figure 5-34: The assembled PCB (back)

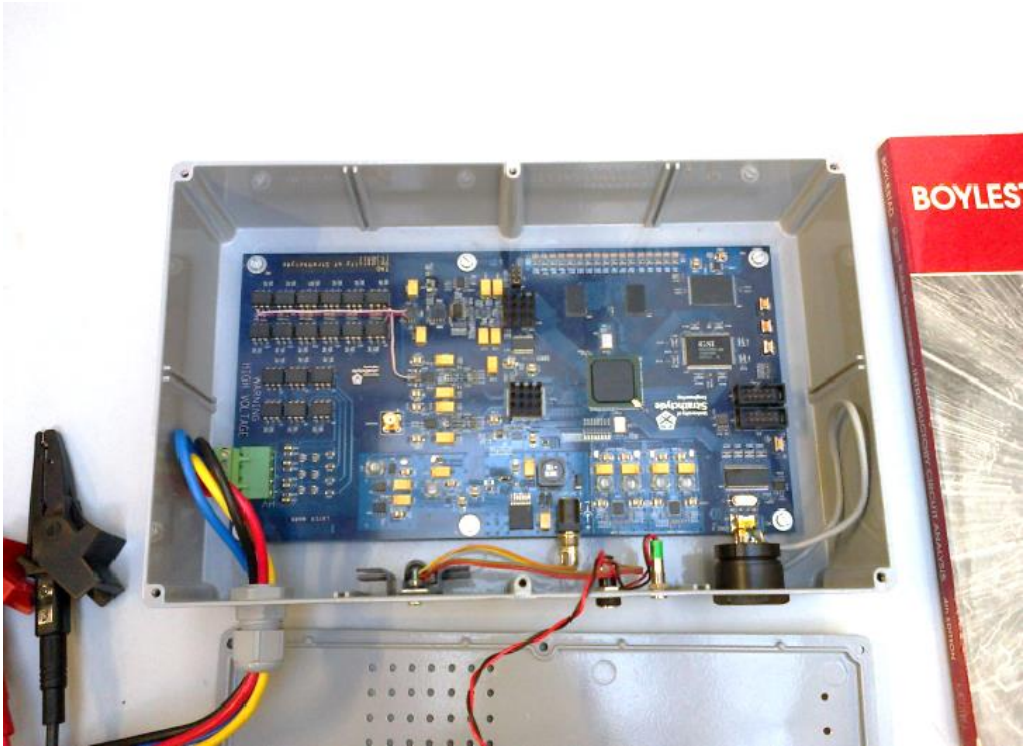


Figure 5-35: TFM1000 (case open)

Figure 5-36: TFM1000 (fully assembled)

5.5 Firmware Development

5.5.1 General

The SoPC plan is displayed in Figure 5-37. As the functionality for each part has already been described in section 5.4, this section only presents the technical detail and design parameters for each of the IP blocks.

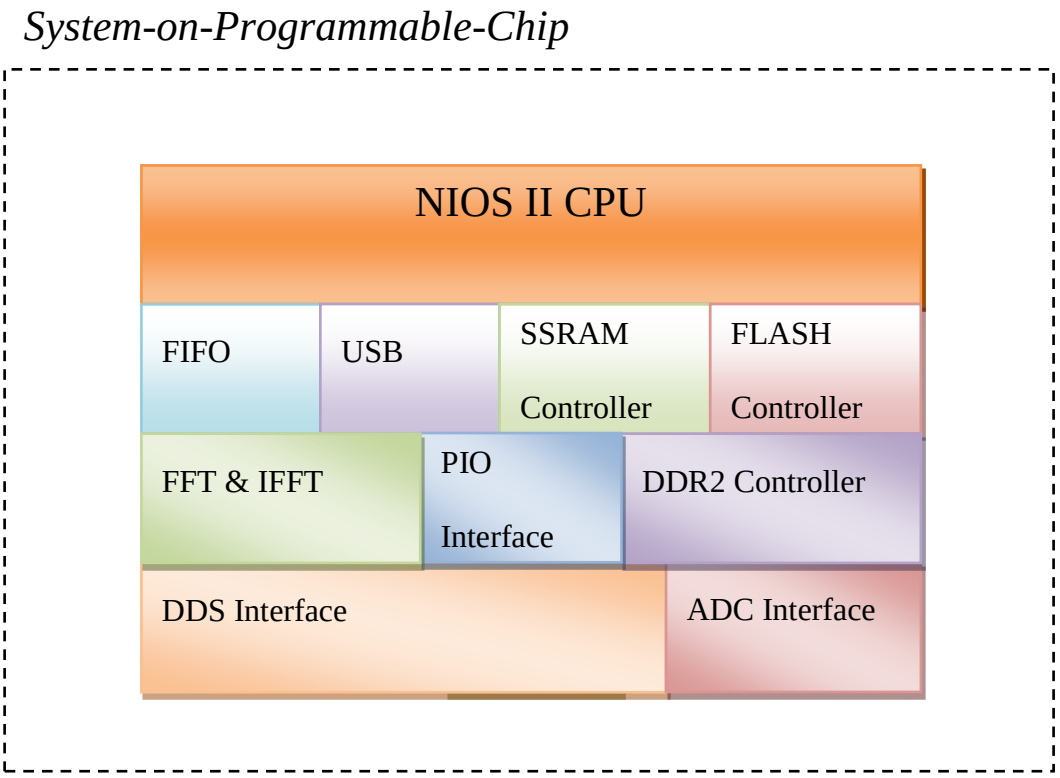


Figure 5-37: SoPC Plan

5.5.2 Clock Distribution

All clock frequencies are derived from two oscillators, 50 MHz and 125 MHz. The ADC clock is internally connected to the 125 MHz oscillator input, therefore the working frequency of the ADC is 125 MHz. The 125 MHz signal frequency will also be multiplied by 4 in a phase-lock loop (PLL), and this feeds a 500 MHz working

clock signal to the DAC. The 50 MHz oscillator drives a PLL to give synchronized 200 MHz and 100 MHz clock outputs. The main processing unit, including CPU and SSRAM, runs at 100 MHz, provided by this clock.

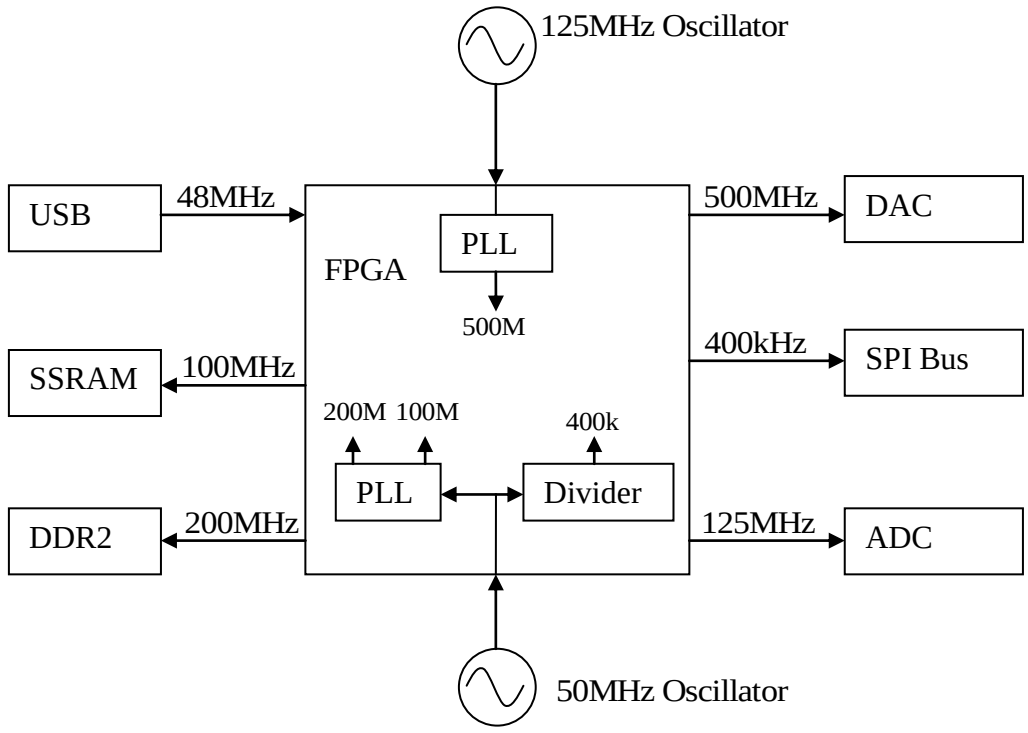


Figure 5-38: Clock Distribution

5.5.3 CPU and supporting peripherals

The CPU selected for implementation was a 32-bit NIOS II/f RISC CPU, developed by Altera. The parameters of the NIOS II embedded CPU should be configured to suit the application. The design is based on the Altera QSYS 11.1 SP1 software environment, and the CPU design follows these steps:

- Plan the CPU parameter
- Plan the CPU peripheral interface
- Generate the CPU IP

The following section will describe the considerations and design of CPU parameter and peripheral interface. The detailed procedures are not listed and reference should be made to the software manual when required.

5.5.3.1 The NIOS II CPU Parameters

Before proceeding to any other CPU parameter plans, the basic parameters must be considered:

1. Bit width: In the consideration that the data amount feeding to the CPU is fairly large, the bit width of the CPU is designed to be 32-bit. This width will naturally match the processing memory (SSRAM, in 32-bit) and offer the maximum bandwidth between the CPU and SSRAM.
2. Address width: In a NIOS II embedded system, larger address width means larger maximum data fetch capability. However, too large address width will consume a large number of LEs (logic elements) and lead to a significant reduction of maximum CPU working frequency (f_{max}). Considering the maximum memory address width* of the DDR2 memory, the data width of NIOS CPU is 32-bit.
3. Internal data cache: The internal data cache is the fastest form of storage in NIOS II embedded systems. The internal data cache also refers to Level 1 Cache (L1 Cache). The L1 resides within CPU IP and acts as a buffer between CPU and external memory, which provides a zero wait-state (delay) interface for the CPU data execution unit. The LEs in a FPGA are very limited, therefore the size of the L1 cache is configured to 4K Bytes for instructions and 4K Bytes for data.

* DDR2 memory has 2Gbit data capacity, maximum address = 2 Gbit * (1024*1024*1024) bits/G = 0x80000000 (hex), this will require 32-bit address width.

4. Embedded hardware arithmetic operation: The arithmetic operation can be split into two types: Fix-point (integer) calculation and Float-point (fraction) calculation. Where hardware arithmetic operation is not available, the CPU will use the software method (basic method) to accomplish the calculation, however this will consume many clock cycles. An example of a fix-point multiplication operation in a NIOS II CPU is shown in the Table 4-7. It can be understood that increased performance is achieved by use of additional LEs. Considering the CPU will perform heavy data calculations, both the fix-point and float-point hardware arithmetic operation are included. It should be noted that the fix-point hardware add and subtract are naturally embedded as a basic arithmetic operation method of the CPU.

Table 5-7: Compare of footprint and performance for hardware multiplier

Fix-point Multiplication Operation		
Option	Additional LEs Used	Clock Cycles to complete
None (software)	0	>250
Hardware Multiplier	>400	16

Other parameters of this CPU are selected and listed as follows:

- Instruction Cache and Data Cache
- Dynamic Branch Prediction
- Barrel Shifter
- Memory Management Unit

As mentioned, the clocking rate of this CPU is 100 MHz, this will offer the Million Instructions Per Second (MIPS) speed of 100 MHz x 1.109MIPS/MHZ = 110.9 MIPS [82].

5.5.3.2 The NIOS II CPU Peripheral Interface

Other IPs in an embedded SoPC system are connected to NIOS II CPU IP via the CPU interface(s), rather than being directly connected to the CPU core. There are two types of interface of the NIOS II CPU in this system: JTAG port and Avalon Bus.

1. JTAG Port: JTAG (Joint Test Action Group) is referred to a well-known standardised test interface defined by IEEE 1149.1. The JTAG port in the CPU can be connected to an external JTAG hardware* to perform:
    a. Software download
    b. Set breakpoints for debugging
    c. Set data triggers for debugging
2. Avalon Bus: The Avalon Bus is a featured interface for Altera NIOS II embedded systems. Avalon MM (memory-mapped) is a special type of Avalon Bus which offers a convenient interface to external data with addresses (e.g. memory). The processor contains two Avalon MM buses, one is designed for generic data transfer, and the other is specially used to transfer CPU instructions.
3. Custom Instruction Master: This is a special port for interfacing NIOS II CPU to special hardware instructions, for example hardware that contain CPU instructions for float-point arithmetic operation.

An overview of the CPU interface is displayed in Figure 5-39.

* The JTAG external hardware for this system is Altera USB-Blaster.

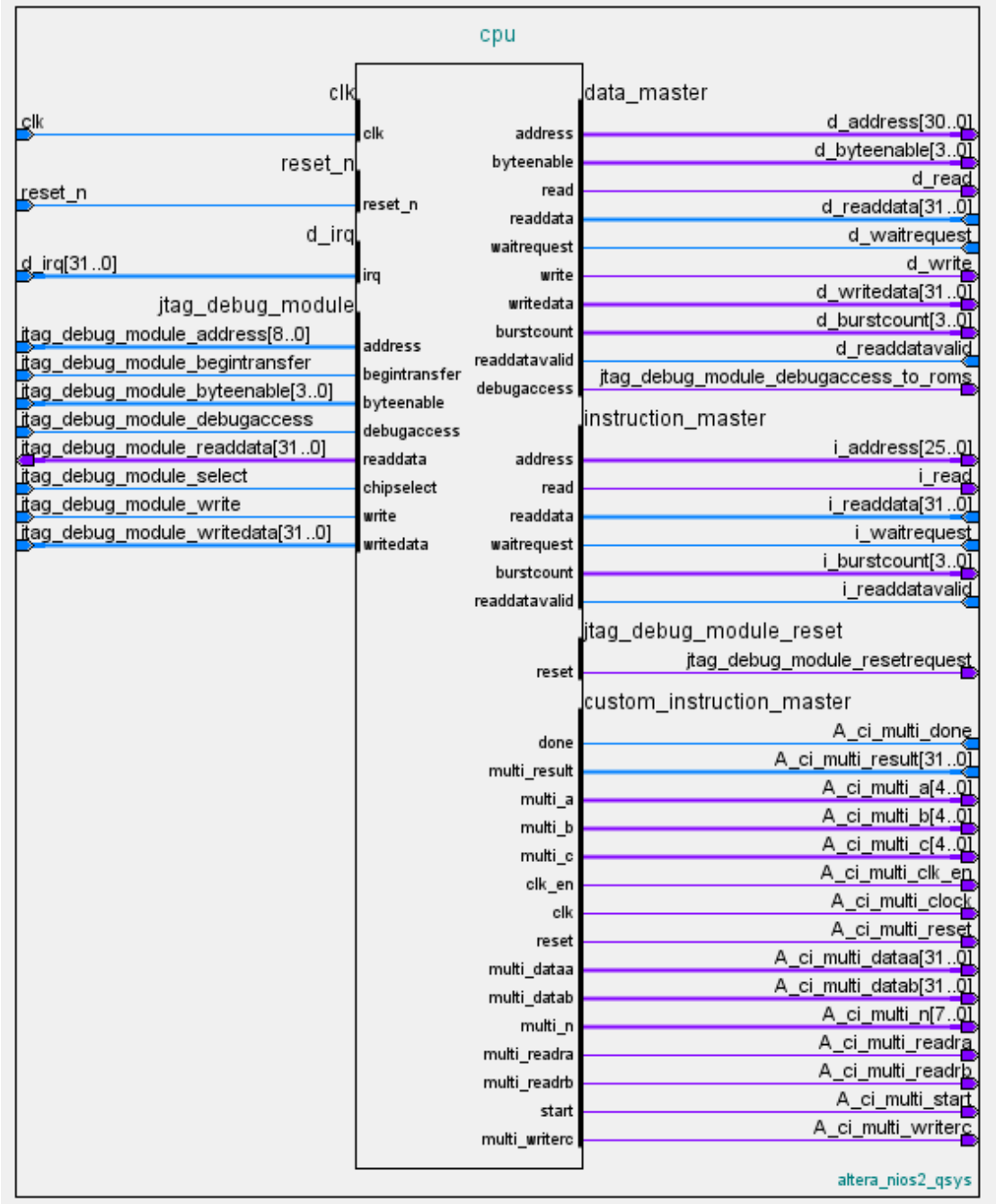


Figure 5-39: The 32-bit NIOS II CPU Signals Diagram

5.5.4 ADC IP

The analogue signals were digitized in the acquisition sytem to form a 125 MHz, 16-bit, digital output stream. The data-stream feeds directly into the ADC IP. The overall input data flow rate can be calculated as:

Input data rate = 125 MHz x 16-bit = 2000 Mbit/s

This is a relatively high data rate for embedded systems. The processing rate of the ADC is essential to accomplish the acquisition without dropping the data. Generally, there are 2 input methods for embedded processors:

- Direct method: the data flow rate of the processor (CPU) must be faster than that of the input device. In this method, the CPU waits for a valid input and reads the input data directly.
- Indirect method: the input data were stored in an external buffer until enough data was transferred, then the external controller must inform the CPU to fetch the data from the buffer.

The direct method offers minimum latency; however, it will consume CPU time when waiting for the valid input. The indirect method is selected in this case. The input data is processed as follows: The ADC IP converts the 16-bit input data to 32-bit data width by combining every 2 data bits. The 32-bit input data are then transferred to a pre-defined address in the DDR2 memory, via a robust, 200 MHz Avalon ST data bus. Once enough data are transferred, the ADC IP generated an interrupt to inform the CPU to process the data; meanwhile, the ADC IP will store the next group of data in another pre-defined address in the DDR2 memory. This is also known as ping-pong buffering.

The ADC IP interfaced to 3 groups of data:

- Control Signals to/from Avalon MM bus, referenced to CPU clock (100 MHz)

- Data stream to Avalon ST bus, referenced to DDR2 clock (200 MHz)
- Data input from acquisition subsystem, referenced to ADC clock (125 MHz)

As 3 groups of signals were referenced to different clock domains, it was not possible to move the data directly from one clock domain to another. The glue logic between different clock domains was done using a Dual-Clock First In First Out (DC FIFO) buffer. As the name implies, the DC FIFO is a special type of buffer, which has two seperated ports for writing and reading the data. The write port and read port can be referenced to different clocks. As shown in Figure 5-40, data were moved into the DC FIFO from the write port, and the write data were referenced to the write clock. The first data written from the write port will be first pulled from the read port, hence "first in first out". The actural DC FIFO is more complex because the write may have an overflow issue, whilst the read may suffer underflow when nothing is stored in the DC FIFO.

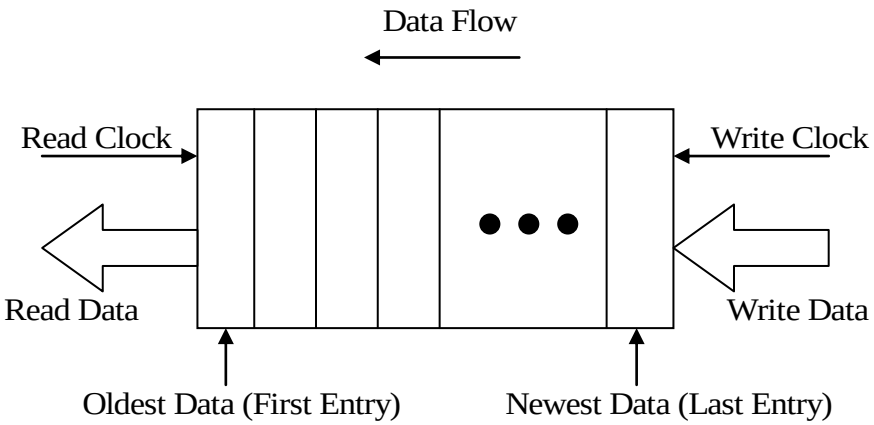


Figure 5-40: Block Diagram of a Duel Clock FIFO Buffer

An internal block diagram of the ADC IP is shown in Figure 5-41. The controlling data are issued by the CPU, and written into the internal control register of the ADC IP via the Avalon MM bus. The input logic and output logic read the according

control register, and complete their tasks individually without the need of interpretation by the CPU.

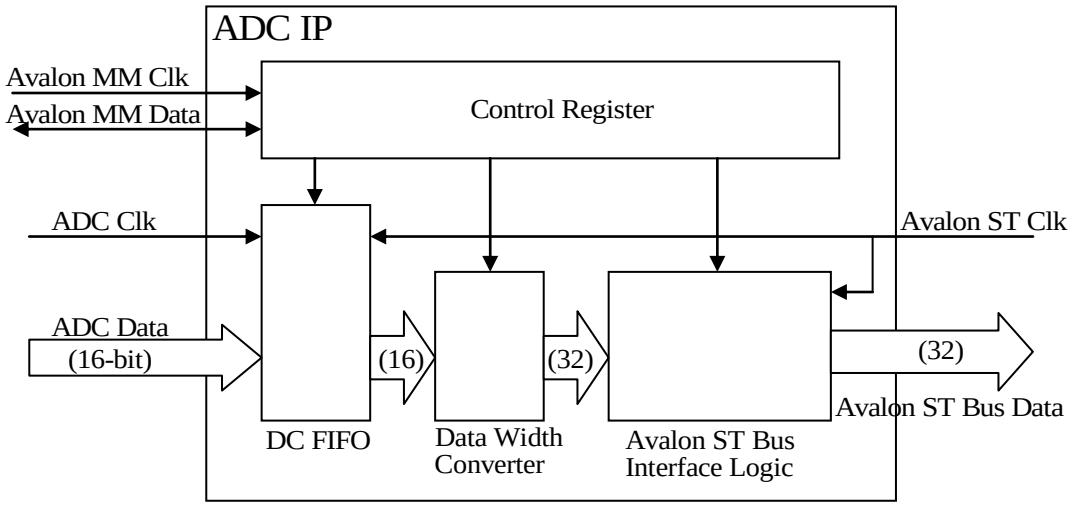


Figure 5-41: Block Diagram of ADC IP

The control register of the ADC IP are listed in Table 5-8.

Table 5-8： Control Register of ADC IP

Name	Avalon MM Address	Value on Reset	Description
Reset	0x0000 0000	0	Set this bit to reset the ADC IP and load default control register value.
Prescaler[15:0]	0x0000 0001	0	The ADC output clock prescaler. Actual ADC clock = 125MHz / (Prescaler+1)
Fifo Reset	0x0000 0002	0	Set this bit to clear the DC FIFO and all other data buffers within ADC IP.
ADC Data[15:0]	0x0000 0003	-	Read only register. Read the ADC value sampled at the time of reading this register.
Error	0x0000 0004	-	Read only register. This bit will automatically set when there is an error occurred during the data transfer. Reset the ADC IP will clear this bit.

The ADC IP was written by Verilog HDL language and compiled and packed into an external IP package. The ADC IP package can be easily added into a SoPC design and connected to other components to form a full SoPC system. The signal diagram of the ADC IP is shown in Figure 5-42.

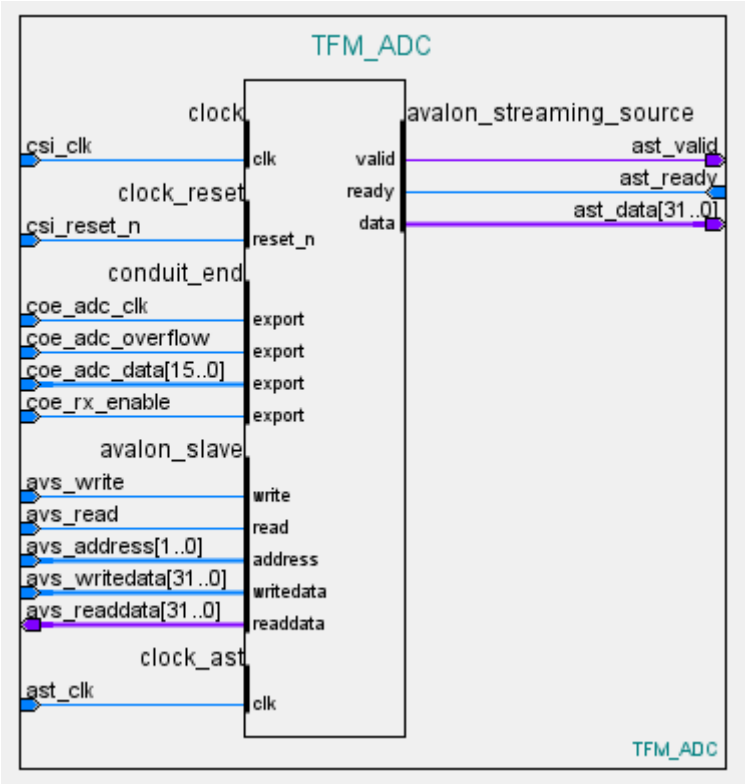


Figure 5-42: Signal diagram of ADC IP package

5.5.5 DAC IP

The above ADC IP processes the input data from the acquisition system and sends it to the Avalon ST Bus. The DAC IP works in the opposite way: fetching the data from the Avalon ST bus, and transmitting it to the digital input port of the signal generation system. A block diagram is shown in Figure 5-43. It can be found that the internal

composition of the DAC IP is similar to the ADC IP, except that the direction of the signal is reversed.

A description of the control register can be found in Table 5-9, and the signal diagram is shown in Figure 5-44.

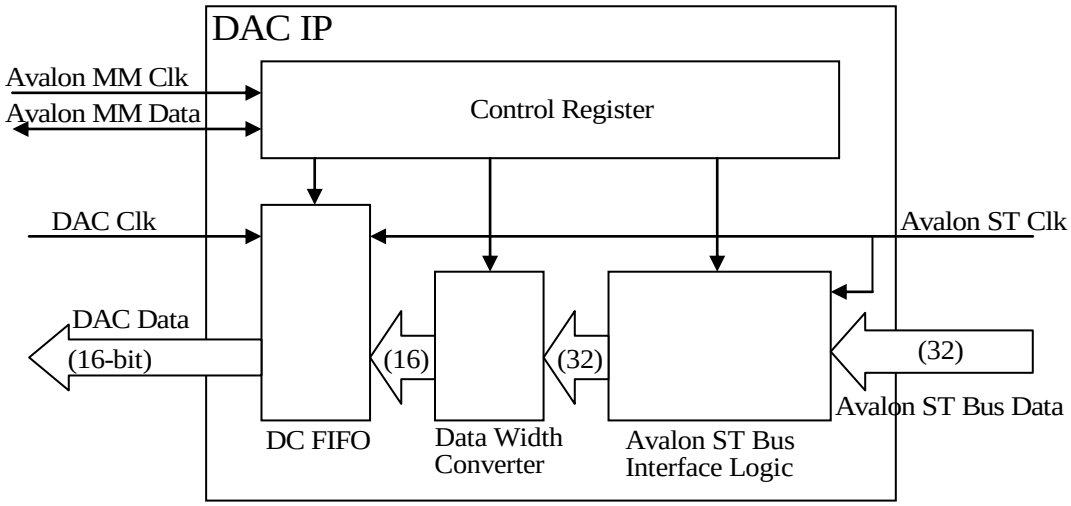


Figure 5-43: Block Diagram of DAC IP

Table 5-9: Control Register of DAC IP

Name	Avalon MM Address	Value on Reset	Description
Reset	0x0000 0000	0	Set this bit to reset the DAC IP and load default control register value.
Fifo Reset	0x0000 0001	0	Set this bit to clear the DC FIFO and all other data buffers within DAC IP.
Error	0x0000 0002	-	Read only register. This bit will automatically set when there is an error occurred during the data transfer. Reset the DAC IP will clear this bit.

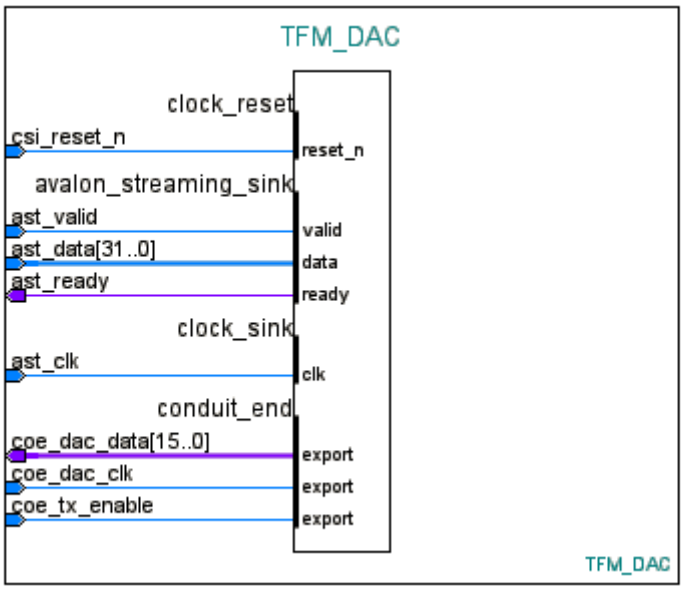


Figure 5-44: Signal diagram of DAC IP package

5.5.6 USB Firmware

The USB firmware includes an internal program in the CY7C68013A USB controller, and a USB IP in SoPC.

As described in section XX, the CY7C68013A USB controller works on slave FIFO mode. In this mode, the internal program is not involved in the data transfer, rather only in configuring of the USB controller. Therefore, the data via USB is mainly processed by USB IP. Hence this section is focused on the USB IP. The internal program, with detailed comments on the USB controller, can be found in the source code.

The USB IP has two main roles: assisting the CPU to exchange the data to the USB bus, and to interface the uni-directional USB data into the bi-directional Avalon MM bus. As shown in Figure 5-45, the USB IP contains 4 parts:

- Avalon MM bus interface logic: Converts the signal according to the Avalon MM bus standard.

- DC FIFO (with build-in data width converter): Bridge Avalon MM bus (Avalon MM clock with 32-bit data width) and USB controller (USB clock with 16-bit data width).
- USB Control State machine: asynchronously exchanges the data between the Avalon Bus and the USB Controller.
- USB Controller Interface Logic: Converts the signal according to the USB controller interface standard.

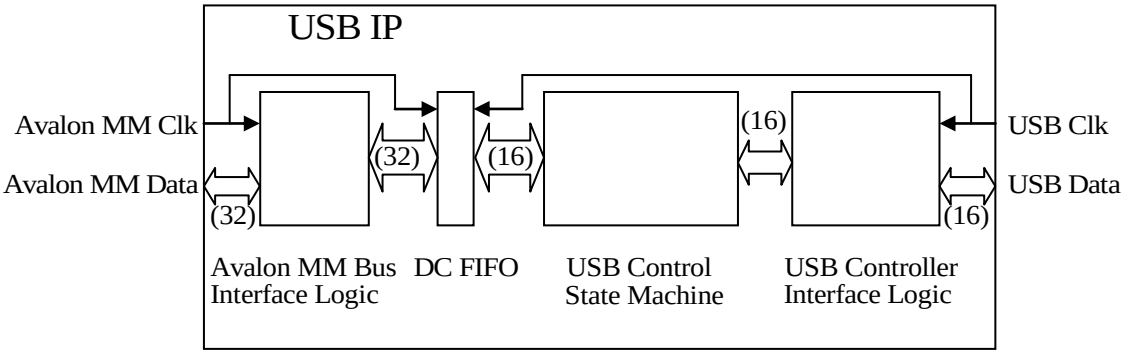


Figure 5-45: Block Diagram of USB IP

The USB bus employs a half-duplex communication protocol. This indicates that the USB bus can only transmit data or receive data at a certain time. However, the Avalon MM bus is a full-duplex, and able to transmit and receive data at the same time. Therefore, extra logic is required to synchronise the data between the USB bus and the Avalon Bus. This is achieved by using a USB control state machine, as shown in Figure 5-46.

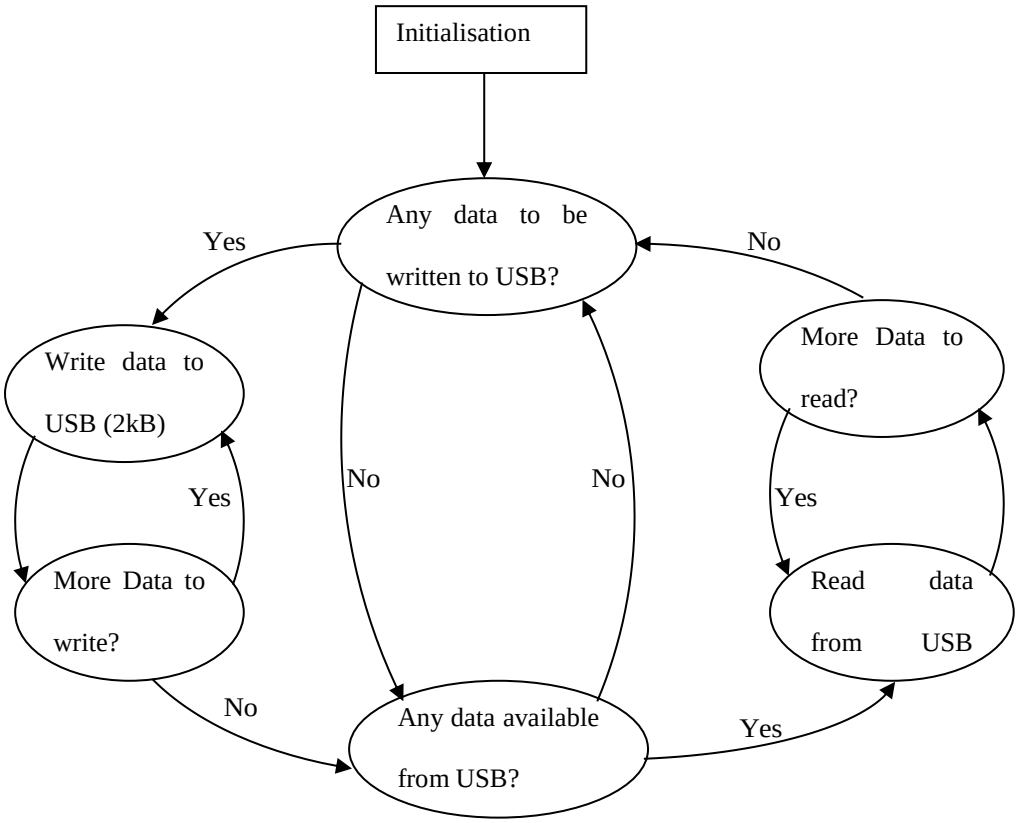


Figure 5-46: Flow diagram of USB control state machine

As seen in the diagram, the state machine continuously checks whether a transfer is required between the Avalon MM bus and the USB bus.

To avoid data loss, the data written from the Avalon MM bus will be stored in an internal DC FIFO buffer at the first moment. Once the state machine detects this data, it will be divided into 2kByte blocks (USB2.0) or 512Byte blocks (USB1.1), and transfer to the USB controller. The USB controller will complete the remaining data transfer to the PC.

Vice versa, when data is available from the USB bus, the state machine will move the data to the DC FIFO buffer, and notify the Avalon MM bus to fetch this data.

The Avalon MM registers were designed as per Table 4-10.

Table 5-10: Avalon MM registers of USB IP

Name	Avalon MM Address	Value on Reset	Description
USB Data	0x0000 0000	0	Read from this address will read the data from USB; Write to this address will write the data to USB.
In Buffer Used	0x0000 0001	0	Read only register. Read the number of 32-bit word used in the DC FIFO input (PC to FPGA) buffer.
Out Buffer Used	0x0000 0002	0	Read only register. Read the number of 32-bit word used in the DC FIFO output (FPGA to PC) buffer.
Error	0x0000 0003	0	Read only register. This bit will automatically set when there is an error in USB IP. Reset the USB IP will clear this bit.

The signal diagram of the USB IP package is provided in Figure 5-47.

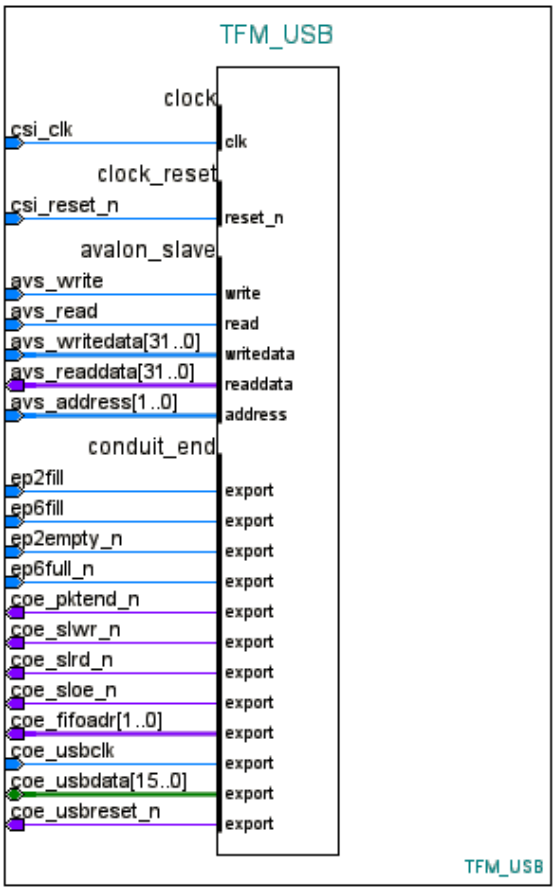


Figure 5-47: Signal diagram of USB IP package

5.5.7 Scatter Gather Direct Memory Access (SGDMA)

In computer systems, Direct Memory Access (DMA) is designed for moving the data between systems (mainly memory and hard drive) without the participation of the CPU. By using DMA, the CPU is free from moving data, and has more time to process the useful data.

Scatter Gather Direct Memory Access (SGDMA) is an IP available in the Altera SoPC system to transfer data between the Avalon MM data bus and the Avalon ST data bus. The original SGDMA IP is very complex and difficult to configure. To simplify the use, user "JCJB" in an Altera forum has rewritten the code, and released a package named "Modular SGDMA".

The SGDMA consists of 3 IP packages: Dispatcher, Read Master and Write Master. Dispatcher is used to send commands to Read Master or Write Master. The Read Master is used to transfer data from the Avalon St Bus to the Avalon MM bus, and Write Master is used for transferring data from the Avalon MM bus to the Avalon ST bus.

There are 3 different combinations to suit different applications:

- Combination MM-MM: Data Move between Avalon MM bus to Avalon MM bus. Requires a Dispatcher, a Read Master and a Write Master.
- Combination MM-ST: Data Move from Avalon MM bus to Avalon ST bus. Requires a Dispatcher, and a Write Master.
- Combination ST-MM: Data Move from Avalon ST bus to Avalon MM bus. Requires a Dispatcher, and a Read Master.

In this prototype, data is required to be moved from the acquisition system to the DDR2 memory, therefore a ST-MM combination is needed. Additionally, a ST-MM

combination is also required to transfer data from the DDR2 memory to the DAC of the signal generation system.

5.6 Software Development

An application (TFM Console) and USB driver running on a PC (personal computer) were developed, to control, manage and collect data from the TFM1000.

Communication between the TFM Console and the TFM1000 is via a USB link. The abstract block diagram is displayed in Figure 5-48. As per the USB2.0 standard[*], the USB communication is always initialised by the host. As shown in the figure, the top layer is the TFM Console initialising the write/read command, and sending to the USB Driver. The USB driver interprets the data, and calls the related USB operation APIs (application programming interface) of the operating system. The operating system will further translate the data into physical data bits, and operate the USB hardware in the PC to transmit the data to the USB device (CY7C68013A), via the USB link. The data in the CY7C68013A will soon be detected by the USB IP, and transferred to the CPU of the TFM1000.

Although the USB2.0 link is physically implemented by only 4 wires (VCC, Data+, Data- and GND), the protocol is very complex. The USB driver is developed based on FX2LP Demo, provided by the USB controller manufacturer Cypress Semiconductor. The application (TFM Console) is developed under the Microsoft Visual Studio and .NET Framework v4 platform. The TFM Console and USB driver are both

[*] http://www.usb.org

compatible with the most popular Microsoft operating systems, including Windows® XP, Windows® Vista and Windows® 7*.

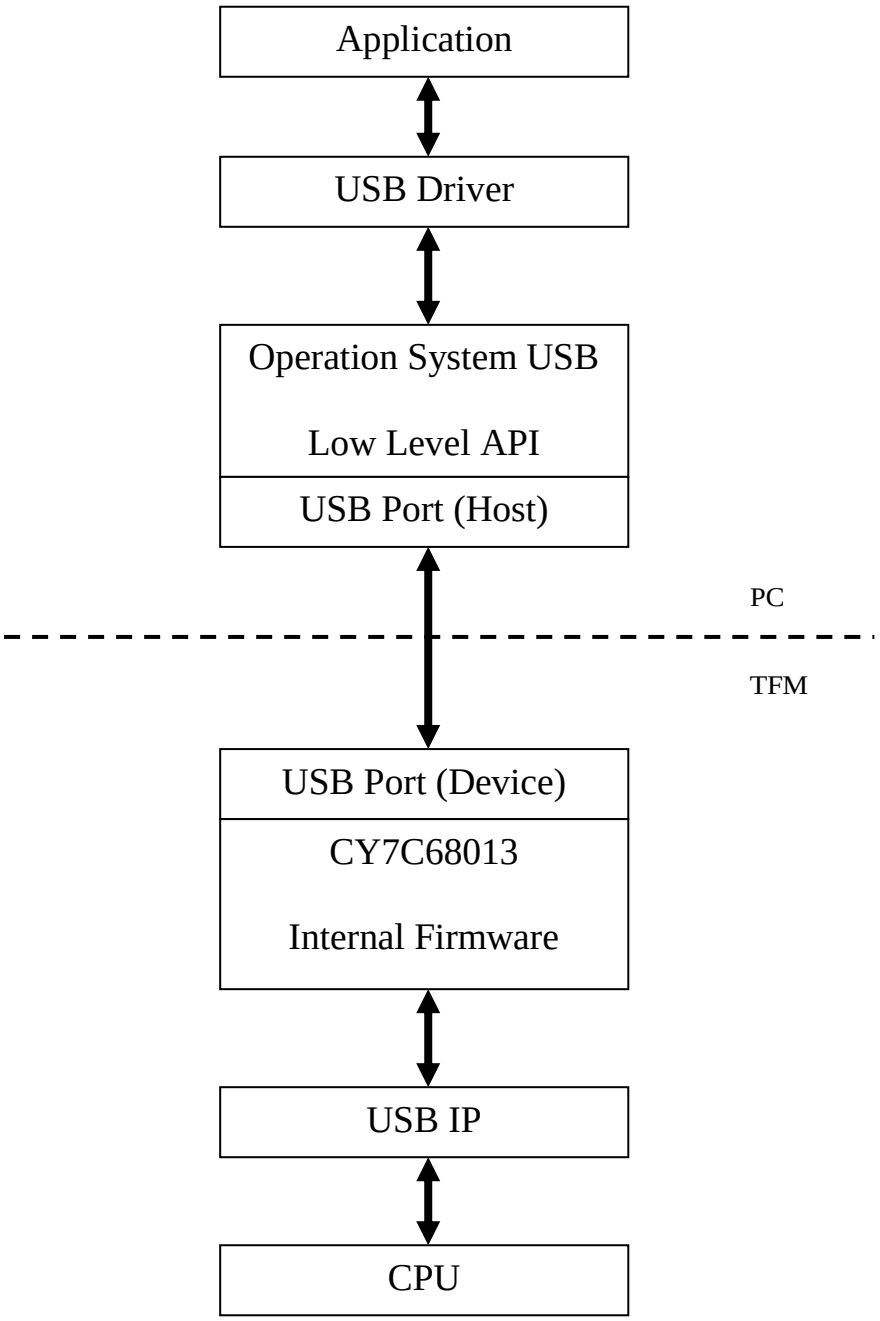


Figure 5-48: USB communication block diagram

* Windows is registered trademark of Microsoft

The main interface of the TFM Console is shown in Figure 5-49. It can be divided into 3 regions: waveform display, data logging, and operation.

In the waveform display the user can view, move, and zoom a waveform to any scale. The data logging lists all operations and communication status with a timestamp.

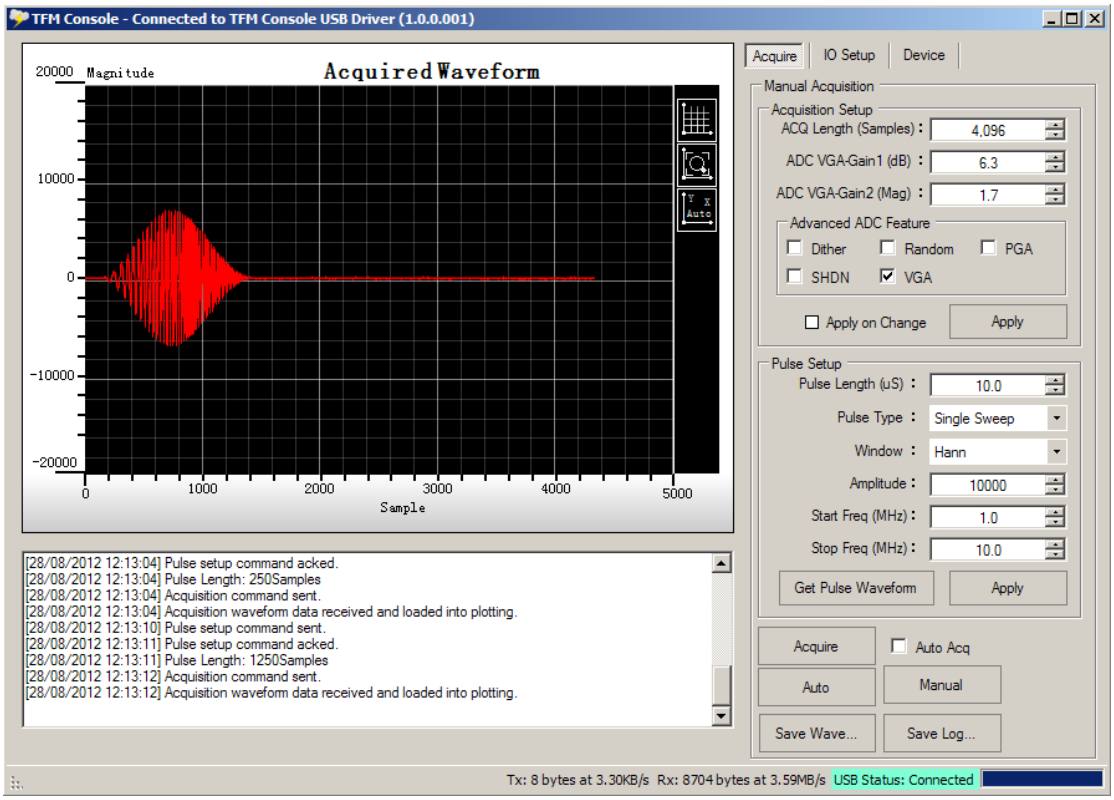


Figure 5-49: Main window of TFM Console

The operation area has 3 pages: Acquire, IO Setup and Device. The function of each page is listed as follows:

The Acquire page configures the acquisition subsystem and signal generation subsystem. All essential parameters in the acquisition subsystem are configurable, including acquisition length, gain of analogue frontend, and advanced ADC features. The part “Pulse Setup” configures the pulse length, pulse type, amplitude and frequency of the reference pulse. This reference pulse can be downloaded by clicking the “Get Pulse Waveform” button.

The “Acquire” button can perform signal acquisition. The “Auto” button will command the TFM1000 to automatically enter transient fault monitoring/locating mode. The “Manual” button can be used to manually trigger the fault acquisition, even if no fault is detected.

The IO (Input and Output) Setup page is used for configuring the IO balance impedance, as well as selecting the input pair under test. A snapshot is displayed in Figure 5-50.

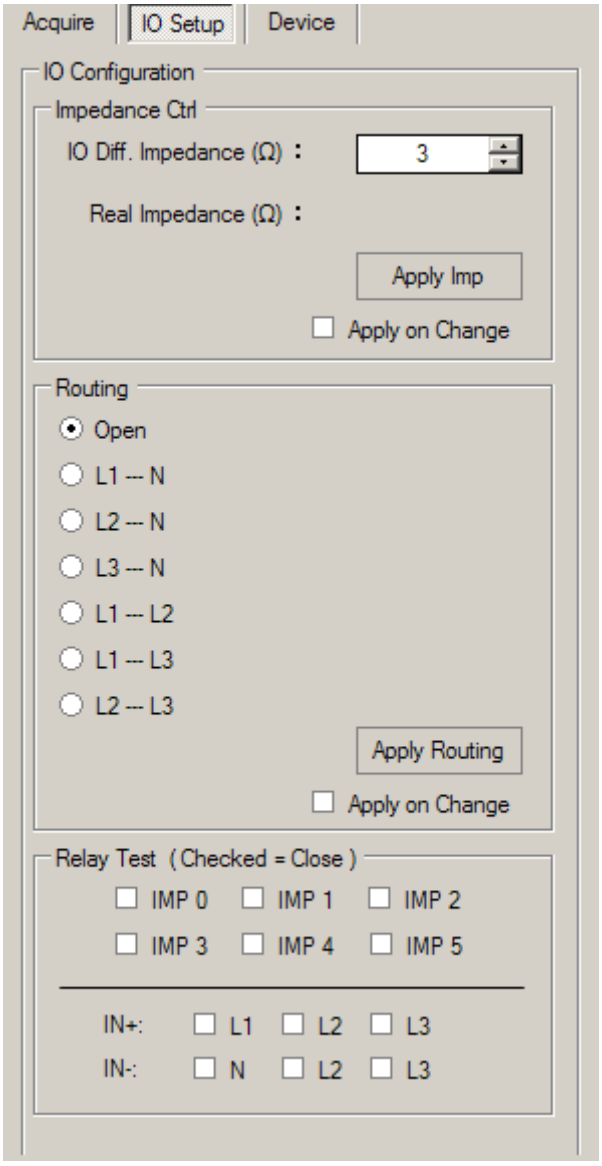


Figure 5-50: IO Setup page

5.7 Experimental Test

Some acquisition examples are presented, along with the output waveform captured by a Tektronix MSO2024 for verification. These test waveforms were configured and generated by using the manual pulse output mode.

Test 1: Generating a rectangular pulse, pulse width 10 μs, output impedance 50 Ω.

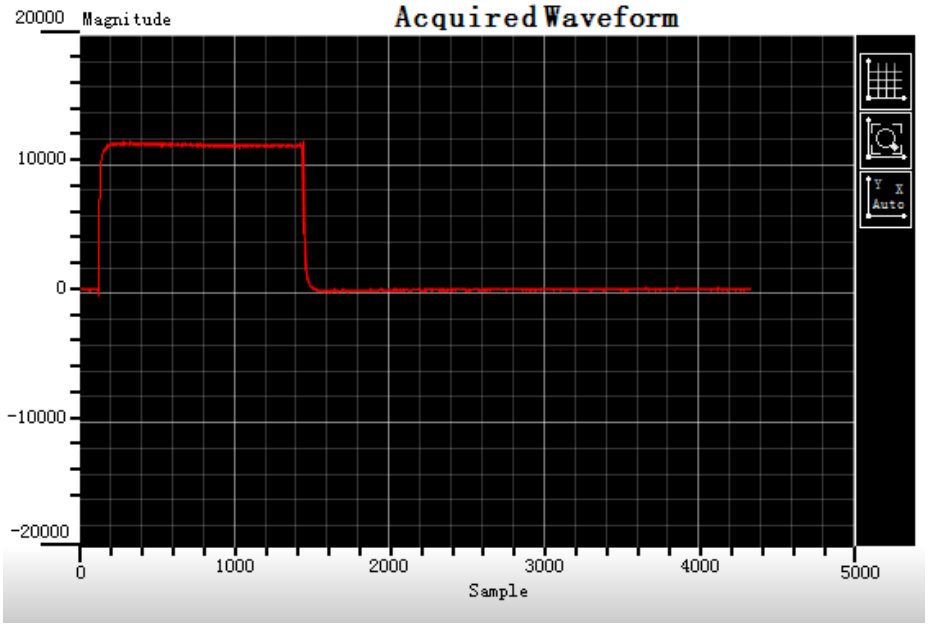


Figure 5-51: Output of test 1 by TFM Console

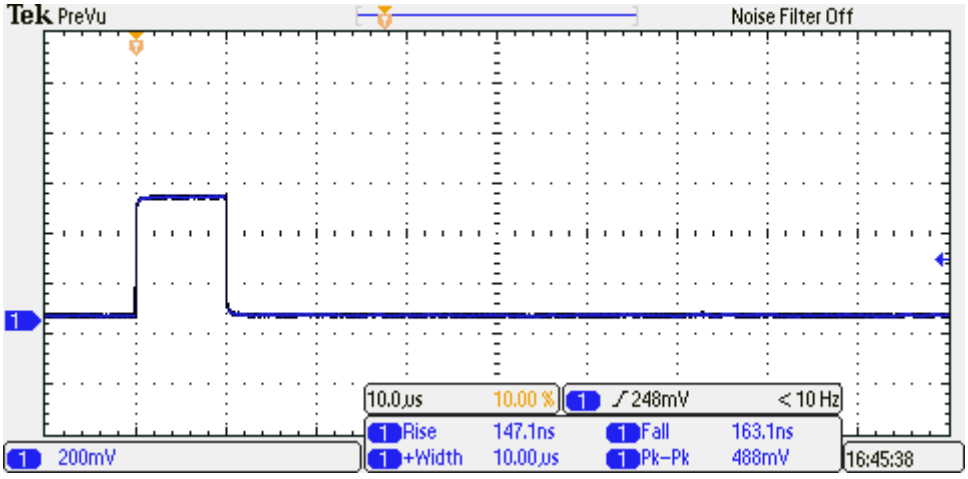


Figure 5-52: Output of test 1 by MSO2024

Test 2: Generating a fixed frequency 20 MHz sine pulse, pulse width 1 μs, output impedance 2 Ω

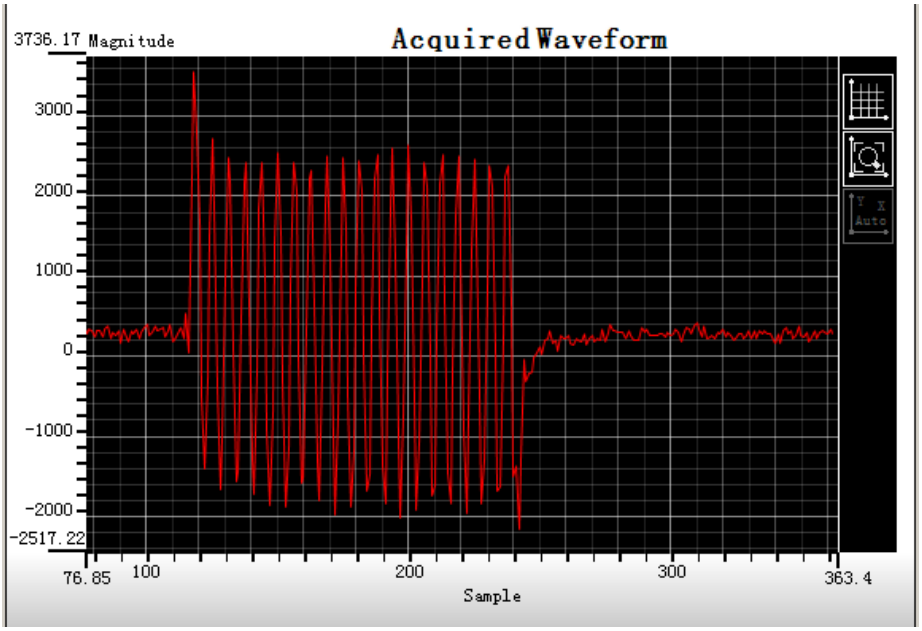


Figure 5-53: Output of test 2 by TFM Console

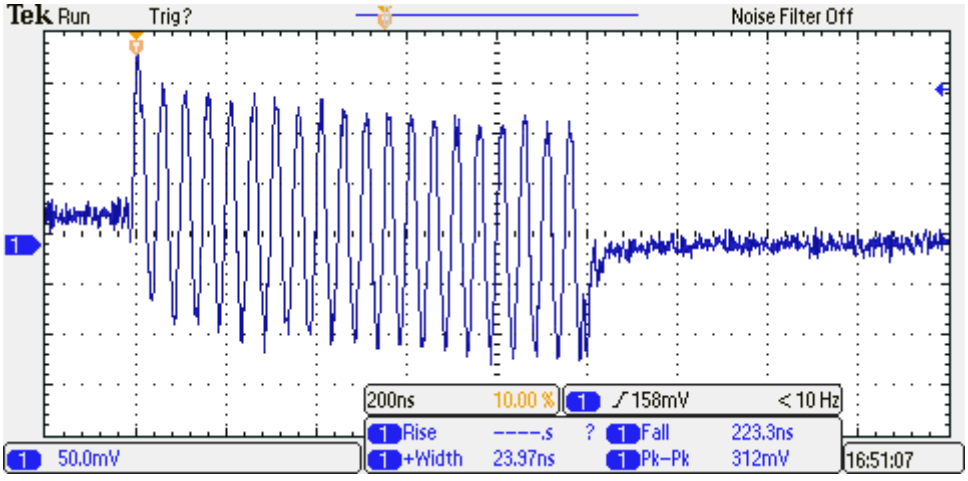


Figure 5-54: Output of test 2 by MSO2024

Test 3: Generating a chirp pulse, sweep from 10 MHz to 20 MHz, pulse width 10 μs, windowed by Hann function, output impedance 50 Ω

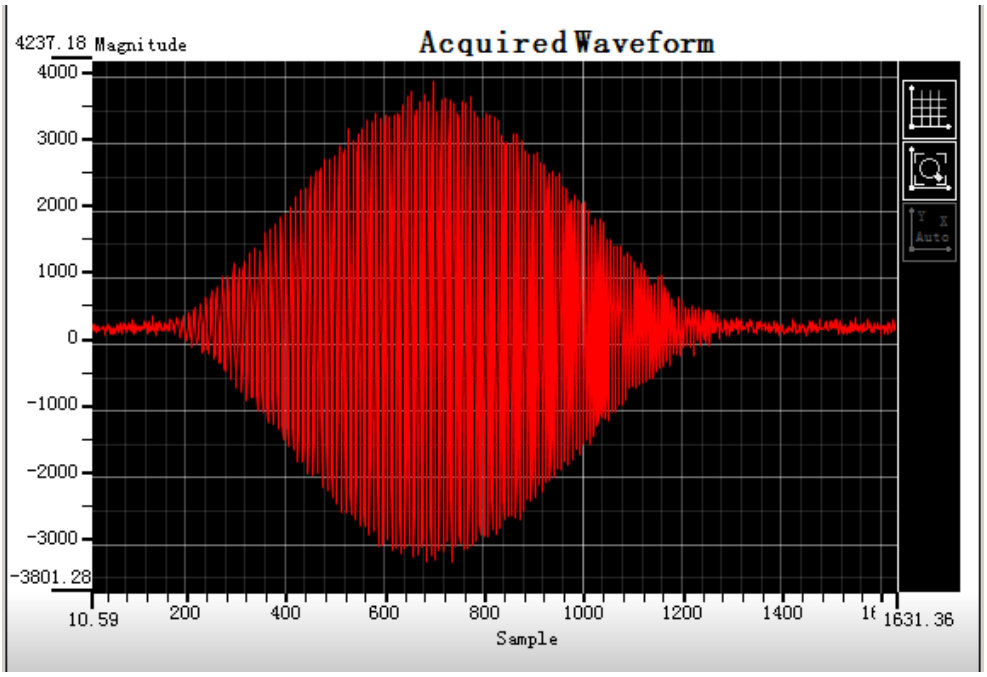


Figure 5-55: Output of test 3 by TFM Console

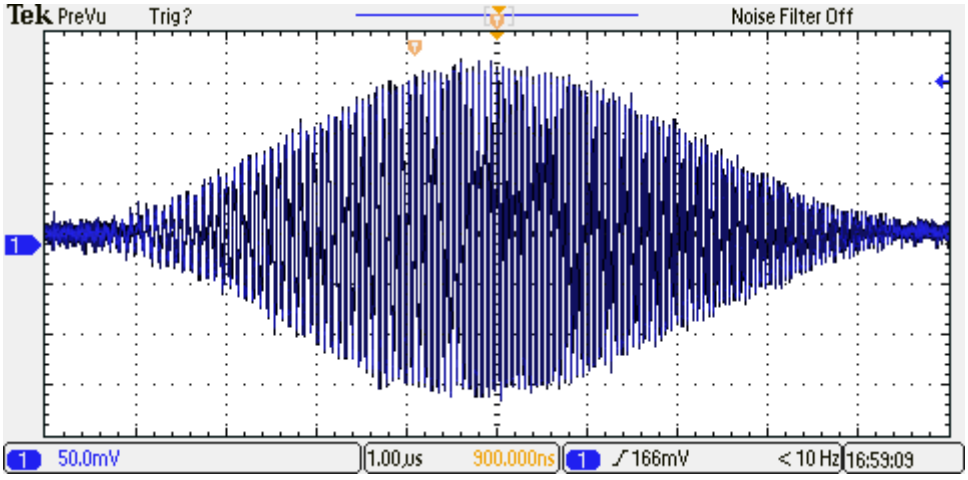


Figure 5-56: Output of test 3 by MSO2024

Test 4: Generating a bi-sweep chirp pulse, sweep from 10 MHz to 20 MHz then back to 10 MHz, pulse width 3.6 μs, windowed by Gaussian function, output impedance 50 Ω

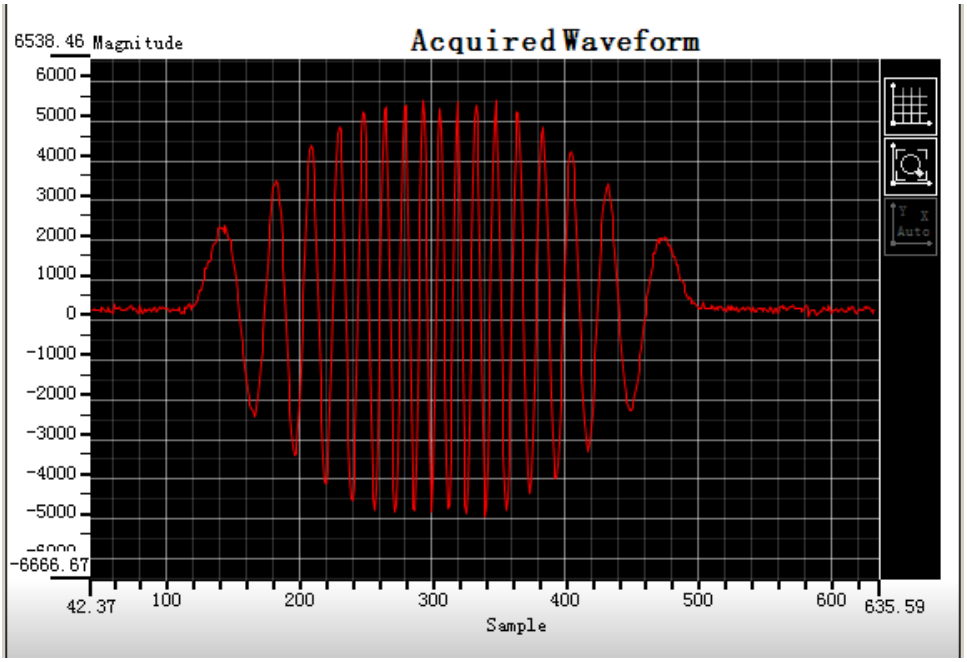


Figure 5-57: Output of test 4 by TFM Console

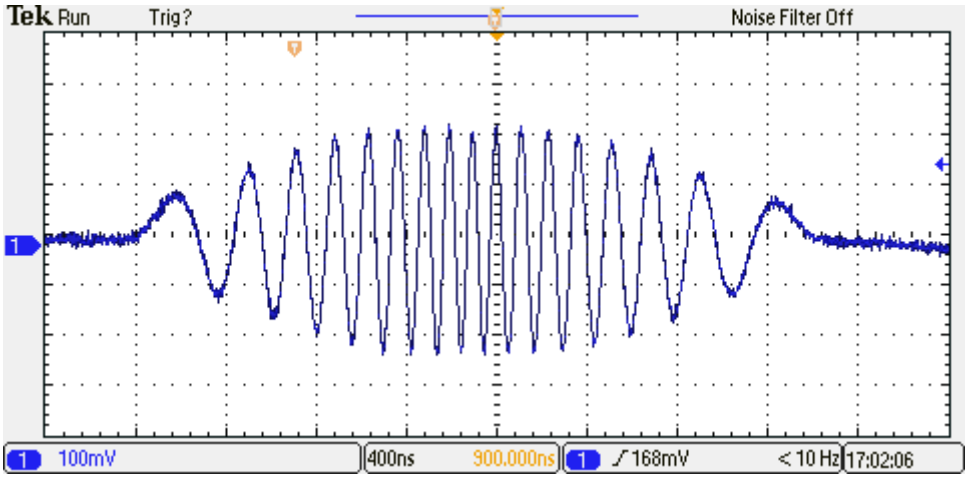


Figure 5-58: Output of test 4 by MSO2024

5.8 Summary

The specifications for essential elements are listed in Table 5-11.

Table 5-11: Summary of essential components

NIOS II CPU	The NIOS II/f CPU is a soft (SoPC) CPU implemented in an Altera Cyclone III FPGA, model EP3C40F484C6N. The clocking rate of this CPU is 100 MHz, which offers the Million Instructions Per Second (MIPS) speed of 100 MHz x 1.109 MIPS/MHZ = 110.9 MIPS [82]. The NIOS II CPU is in charge of the following tasks: • Control and modulate all components in the SoPC system. • Waveform Generation, pre-processing and post-processing. • Transfer the data between components.
NOR Flash Memory (for user program and data)	A NOR flash chip S29GL256P10TFI010, manufactured by Spansion, is used for storing non-violated data. This chip was configured to Common Flash Interface (CFI) mode to interface the 16-bit Avalon MM data bus. This memory has storage capacity of 256 Mb, with random access time 110 ns per word. User program (CPU codes), initialisation parameters and post-processed data (waveforms that contain a fault) will be stored in this memory, because these data are safe when the system is powered off.
Flash Memory (For configuration of FPGA)	An Altera EPCS16 memory is used to configure the FPGA when powering up. This memory device contains 16 Mb HDL data to setup the FPGA using Altera Active Serial (AS) configuration scheme. It should be noted that this device cannot be seen by user programs.
SSRAM	A GS816032B Synchronised Static Random Access Memory (SSRAM) is used to store temporary variable and inter-computational data. The SSRAM is synchronised to the CPU clock, making it an ideal device to store temporary data that require fast read/write speeds. This memory is interfaced to a 32-bit Avalon MM data bus, and is able to store 2 Mbit data.
DDR2 SDRAM	Two IS43DR16640A chips combined to form the 32-bit, 2 Gb DDR2 SDRAM memory. This memory runs at 200 MHz, however as SDRAM requires a refresh process and has a read/write latency, the equivalent performance is slower than

	SSRAM. Because of the high storage capacity, the DDR2 SDRAM is used to store pre-process and post-process waveforms, which are huge in size.
DAC (digital interface)	An Analog Devices AD9779A dual channel 16-bit, 1GSPS DAC is used to convert the digital data stream to an analogue waveform. The DAC is the essential component of the Direct Digital Synthesis (DDS) system.
ADC (digital interface)	LTC2208 from Linear Technology is chosen as the system ADC. This ADC is a 16-bit A/D converter for digitising high frequency signals. The maximum sampling rate of this ADC is 130 MHz
USB	The USB is powered by a Cypress CY7C68013A USB2.0 high speed controller. The USB controller is interfaced to the 16-bit Avalon MM bus, and offers a data exchange channel to the PC, with data rate up to 96 MB/s.
Analogue Control	Analogue control is realised by a MCP23S17 SPI port extender from Microchip. The chip offers two 8-bit GPIO ports which control the signal routing and the balance control of the analogue frontend. This module is interfaced to the SPI bus.

6 Improve fault location using advanced signal processing tools and alternative methods.

6.1 Introduction

The wavelet transform and adaptive filters are the most useful tools in advanced signal processing.

This chapter improves the fault location technique described in Chapter 5 by using the wavelet transform to suppress the side lobes introduced by pulse compression, and by employing adaptive filters to record only significant changes in deviation.

An alternative fault location method using the response differences between multiple cable pairs is also present and discussed.

6.2 Improve fault location accuracy with WT

Pulse compression provides the TDR system with good resolution and detection range. A certain degree of noise rejection is also attained, due to the nature of the correlation computation in LFM pulse compression. In practise however, pulse compression in power cables causes the spectrum leak effect. In other words, the multi-frequency-containing spectrum of the interrogation pulse may be shifted or partly attenuated due to cable loss and dispersion. This will cause loss of bandwidth and increase of side lobes after the compression, affecting the location accuracy. The wavelet transform is employed to address these limitations by parameterised re-composition of the

compressed signal. This will ensure that only those signals containing the relevant frequency component are investigated, potentially benefitting the deviation control.

In implementation, based on the self-comparing scheme presented in Figure 4-2, the wavelet transform process was inserted between the output of pulse compression and the input of deviation control. The wavelet transform process is illustrated in Figure 6-1. The compressed signal will be de-composed into N scales via fast wavelet transform (FWT). Each de-composed scale a_N and d_i (i=1,2…N) will be multiplied by a controlling parameter (weight) g_j (j=0,1,2…N), respectively. The weighted scales are added together to re-compose the signal, according to the controlling parameters.

It can be understood that when the controlling parameter of a scale is larger than 1, the weight of this scale in the composite signal is increased, and vice versa. When $g_0 = g_1 = ... = g_N = 1$, the composite signal is approximate the original signal.

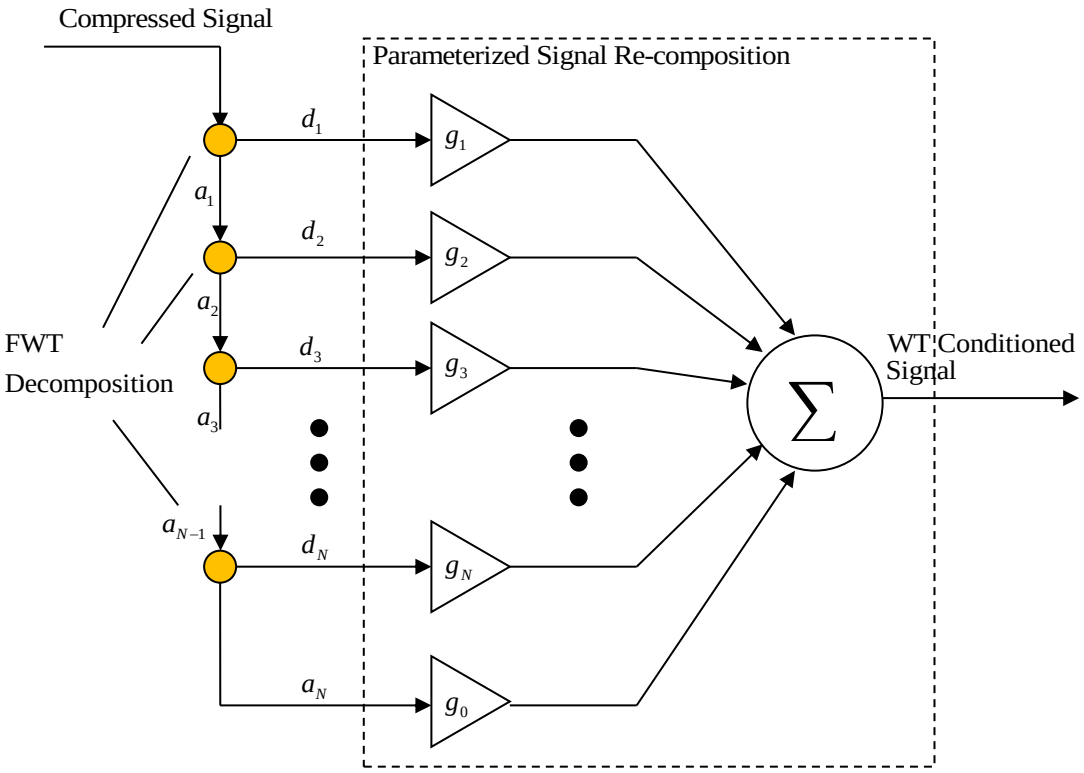


Figure 6-1: Wavelet Transform process

6.3 Improve deviation control with Adaptive Filter

The deviation computing method described in Chapter 5 is implemented simply by subtracting the current TDR waveform from the reference TDR waveform. This is also known as the compare and contrast (C&C) method.

It can be understood that the subtracting operation in the C&C method may magnify a periodic noise, if the period of the noise is approximately equal to the interval between TDR samples. This can be overcome by using an adaptive filter. As the adaptive filter has time-varying and self-adjusting characteristics, the periodic noise applied to the input of the adaptive filter will update the adaptive coefficients, resulting in the noise being adaptively removed from the output of the adaptive filter, and therefore potentially enhancing the accuracy of the end result.

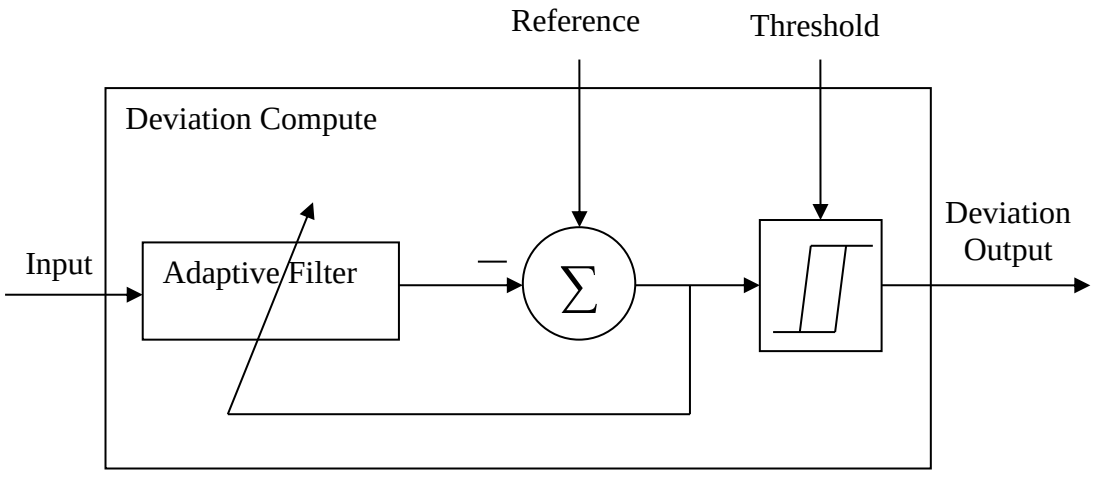


Figure 6-2: Adaptive deviation calculation

6.4 Analysis of algorithm performance with WT and AF enhanced fault location

The following analyses are based on the cable test network described in Section 4.4. The adaptive filter uses the previous enhanced TDR waveform as a reference, and the latest input waveform as the input. The adaptive filter will produce an error waveform as the deviation output. During the adaptive filtering process, the adaptive filter will try to adjust its coefficient to adapt the latest input to the previous waveform, reducing the noise during the adapting process. Once the first reflection waveform containing a significant change has been input, the adaptive filter will not be able to adapt to the change, yielding an error waveform. Only large changes will appear in the error waveform, and noise will be filtered out.

Figure 6-3 and Figure 6-10 show the deviation waveforms produced by the conventional C&C method, and by the adaptive method on dataset 1 and dataset 2, respectively. By inspecting close to the zoomed version of the deviation waveform in Figure 6-4 and Figure 6-11, it can be found that the deviation yielded by the adaptive method is smoother and less noisy while still maintaining a clear identification of the key deviation “spikes”, which are the main lobes of the compressed reflected waveform. The disadvantage when using the adaptive method is the reduced main lobe because of the nature of the filter. In general, the advantages of the adaptive method outweigh its disadvantages, especially in a noisy environment.

In addition to adaptive filtering, the wavelet transform can be used to further enhance the result. As mentioned earlier, a TDR waveform contains many discontinuities because of the reflection due to impedance change at T-joints, loads and faults. The deviation waveform focused on the time change of the discontinuities therefore

represents the change on tees, loads and faults along the cable network. The key to interpret a deviation waveform is by identifying sharp variations. The wavelet transform can aid identification of sharp variations by splitting the waveform into short-duration, high-frequency components and long-duration, low-frequency components, and then re-composing the waveform with different weight scales.

Figure 6-5 shows the 4-level decomposition waveforms of dataset 1 by using Symlets 3 wavelet families. Decomposed waveforms d_1, d_2, d_3 and d_4 were scaled in order to suppress with less significant change. As shown in Figure 6-6, the weights of each de-composed scale were adjusted to suppress the component within the blue broken line.

The re-composition process is done by adding all weighted de-composition scales. Figure 6-8 shows the re-composed signal and the original signal. It can be seen that the re-composed signal gives a clear indication of the fault position, as the noise has been significantly suppressed. This can be further interpreted by using the wavelet coefficient map shown in Figure 6-7. The brighter colours in the wavelet coefficient map indicate larger proportion of the signal. As shown in Figure 6-7, the wavelet transform process focuses on the significant changes, and suppresses less significant components. Figure 6-9 gives the final result after processing of dataset 1, by applying adaptive filtering and the wavelet transform technique to the pulse compression enhanced TDR system.

The wavelet transform was also applied to dataset 2. Figure 6-12 shows the decomposition map of the deviation waveforms of dataset 2. The de-composed signals were re-scaled as shown in Figure 6-13, and only significant changes remained after wavelet re-composition, as depicted in Figure 6-14. Figure 6-15 compares the de-noised signal after the wavelet transform against the original signal. Figure 6-16 and

Figure 6-17 show the final results following processing of dataset 2 using the enhanced technique described in this chapter.

The results are summarized in the Table 6-1:

Table 6-1: Summary of result

Dataset	Actual fault distance	C&C Method		Adaptive + WT Method	
		Fault Dist.	Accuracy	Fault Dist.	Accuracy
1	190m	189.6m	-0.21%	189.8m	-0.10%
2	285m	285.5m	0.18%	285.1m	0.04%

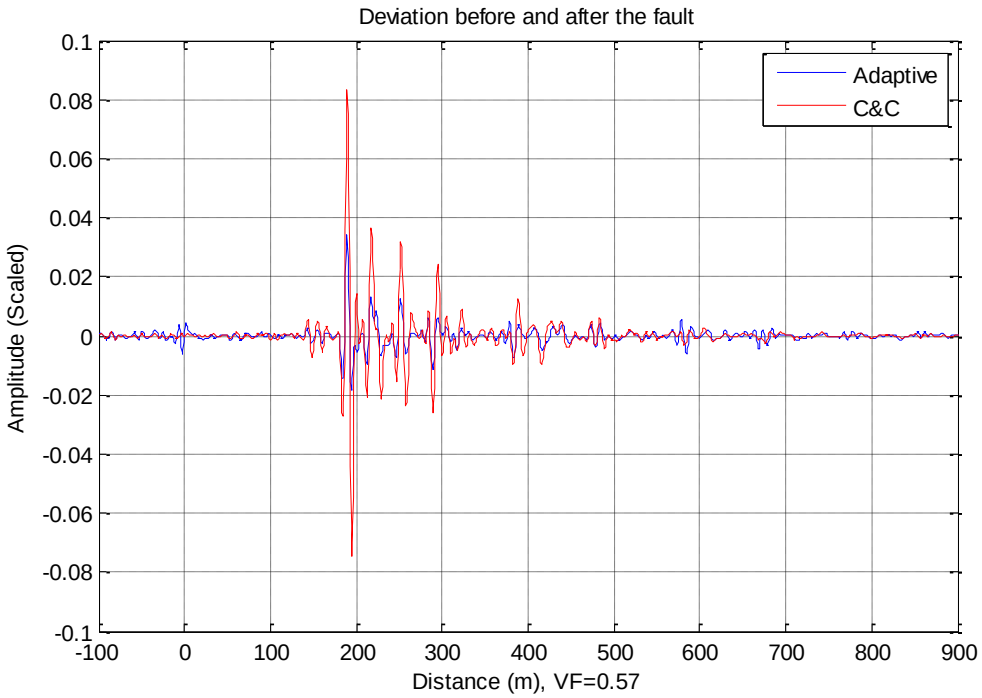


Figure 6-3: Deviation waveforms produced by C&C method and adaptive method of dataset 1

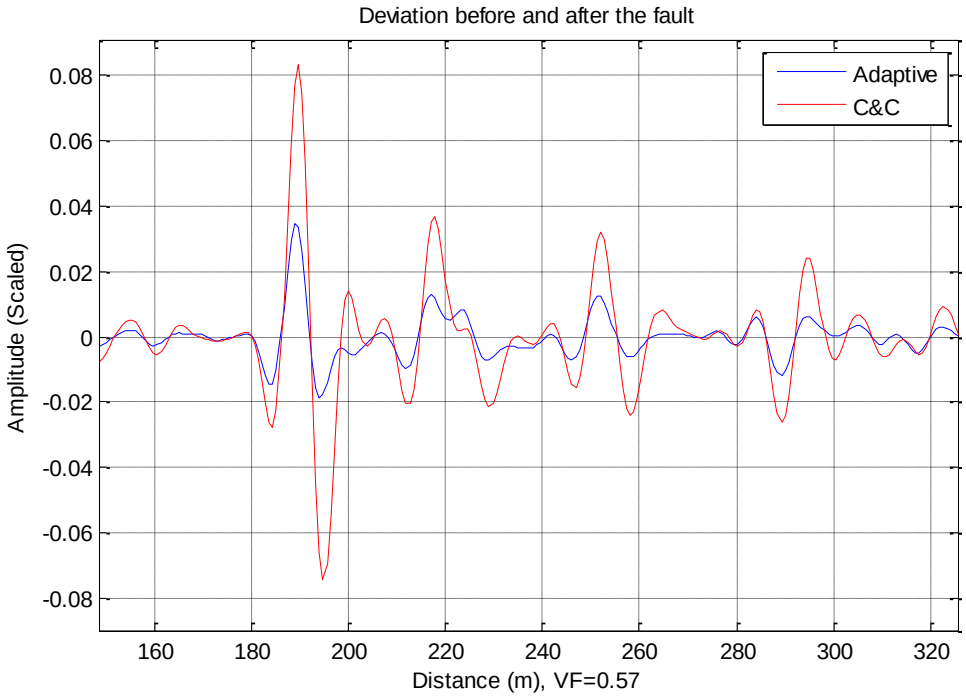


Figure 6-4: Deviation waveforms produced by C&C method and adaptive method of dataset 1 (Zoomed in)

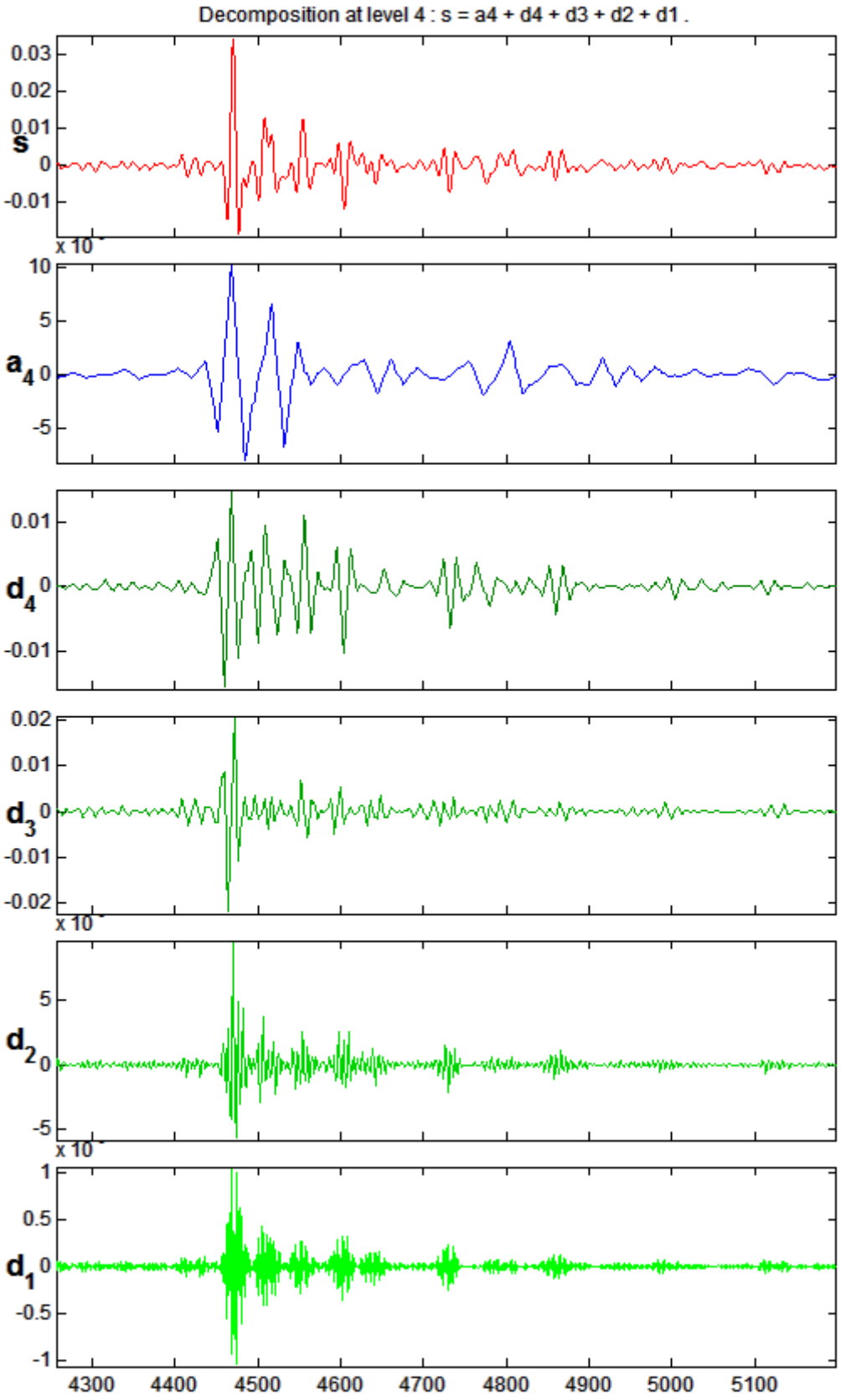


Figure 6-5: Decomposition map of dataset 1

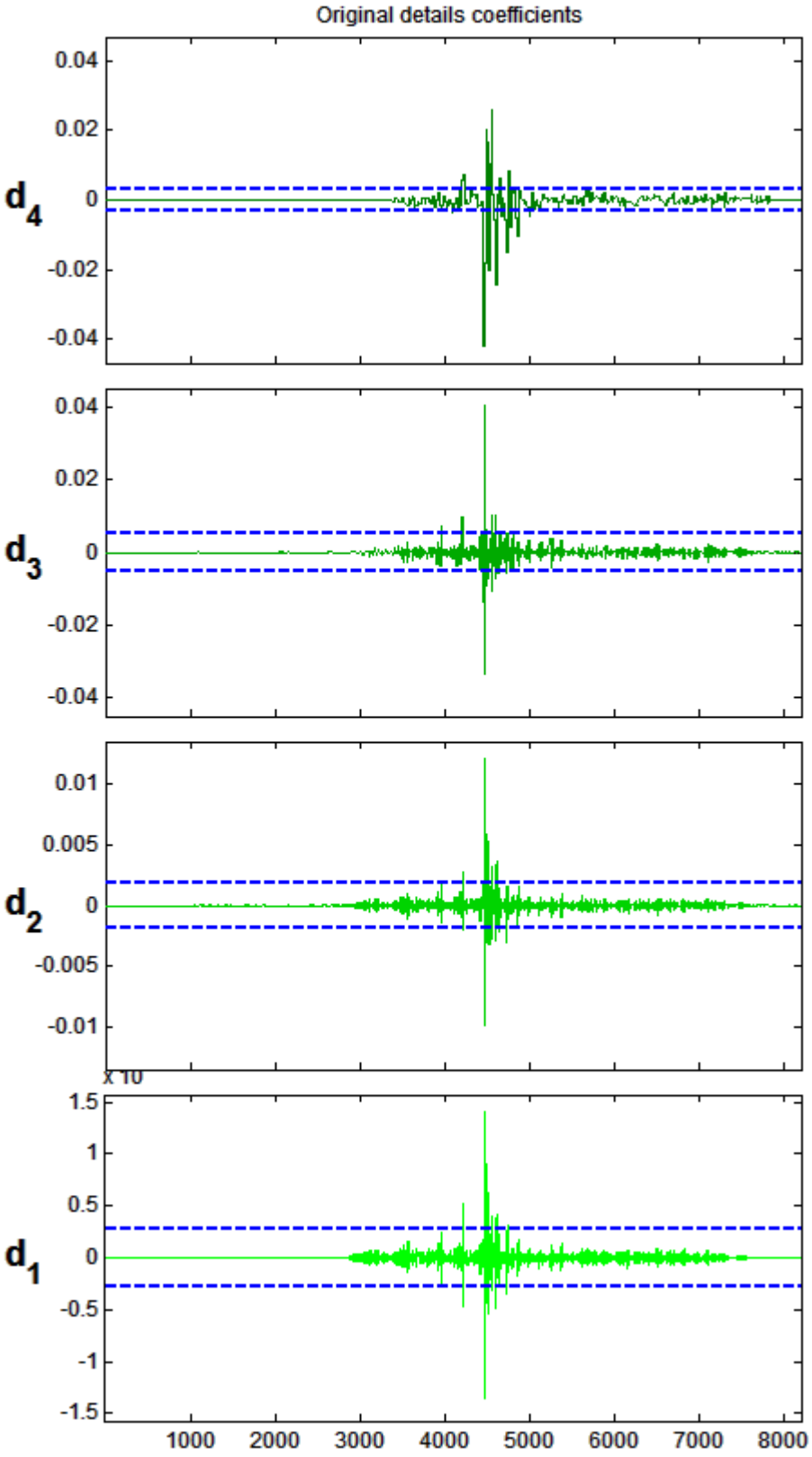


Figure 6-6: Wavelet rescaling of dataset 1

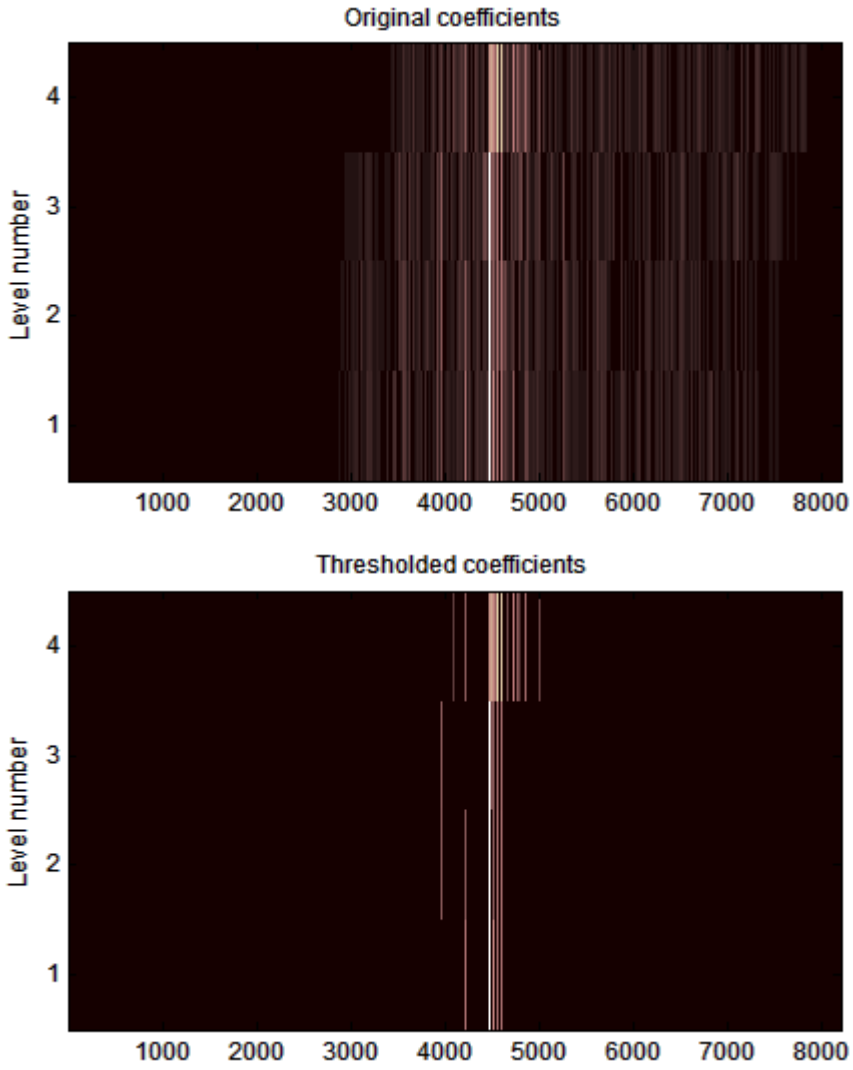


Figure 6-7: Wavelet coefficient map of dataset 1, before wavelet rescaling (a) and after wavelet rescaling (b). X-axis is representing number of samples (time). Brighter area indicating larger magnitude signal.

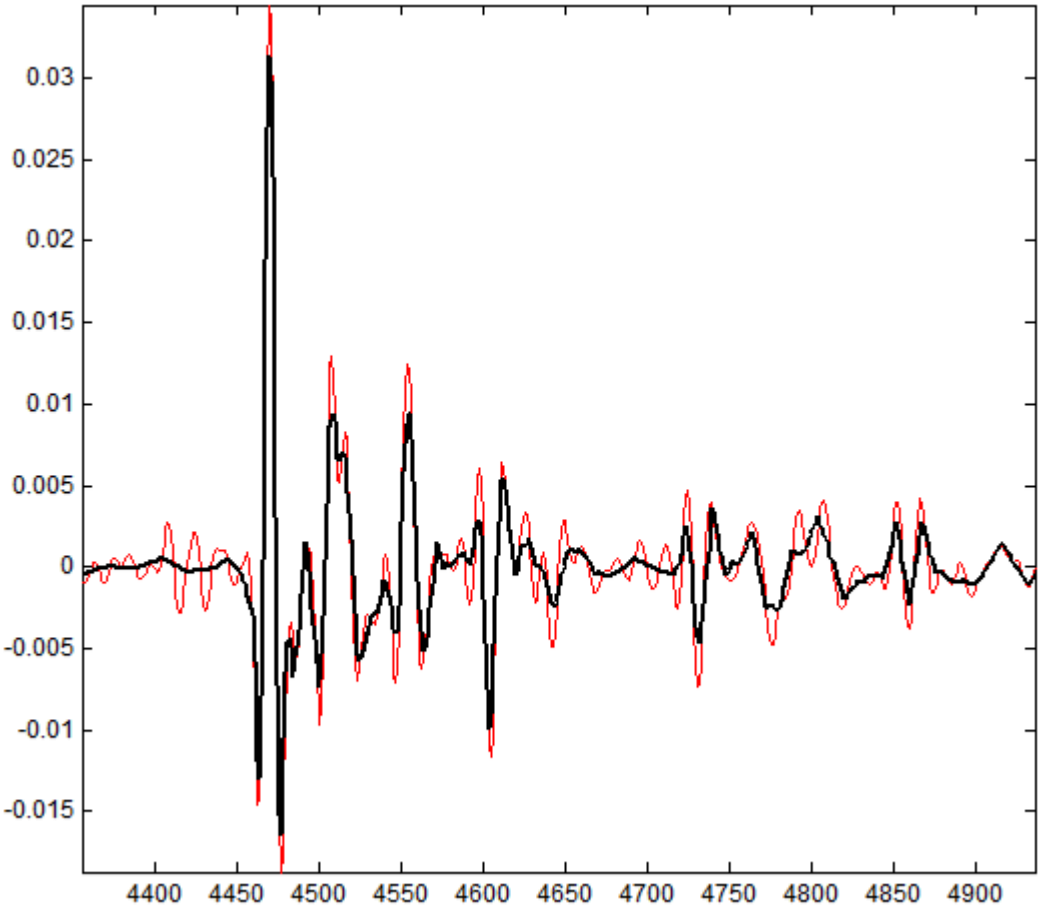


Figure 6-8: The deviation signal of dataset 1 before (a) and after (b) wavelet transform enhancement

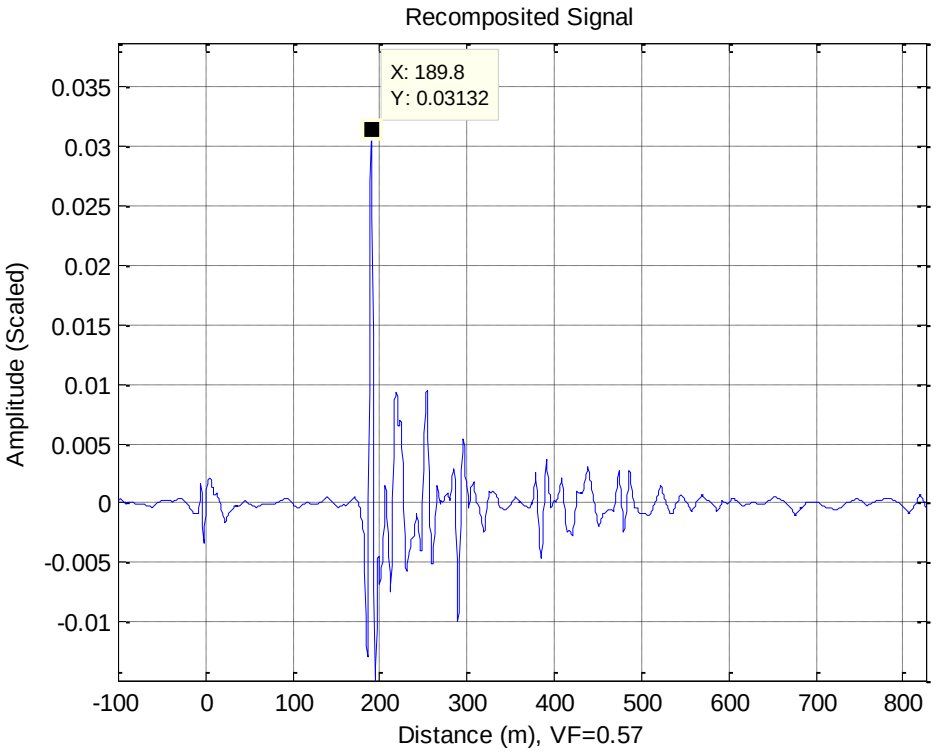


Figure 6-9: Final deviation waveform of dataset 1 after adaptive and wavelet enhancement

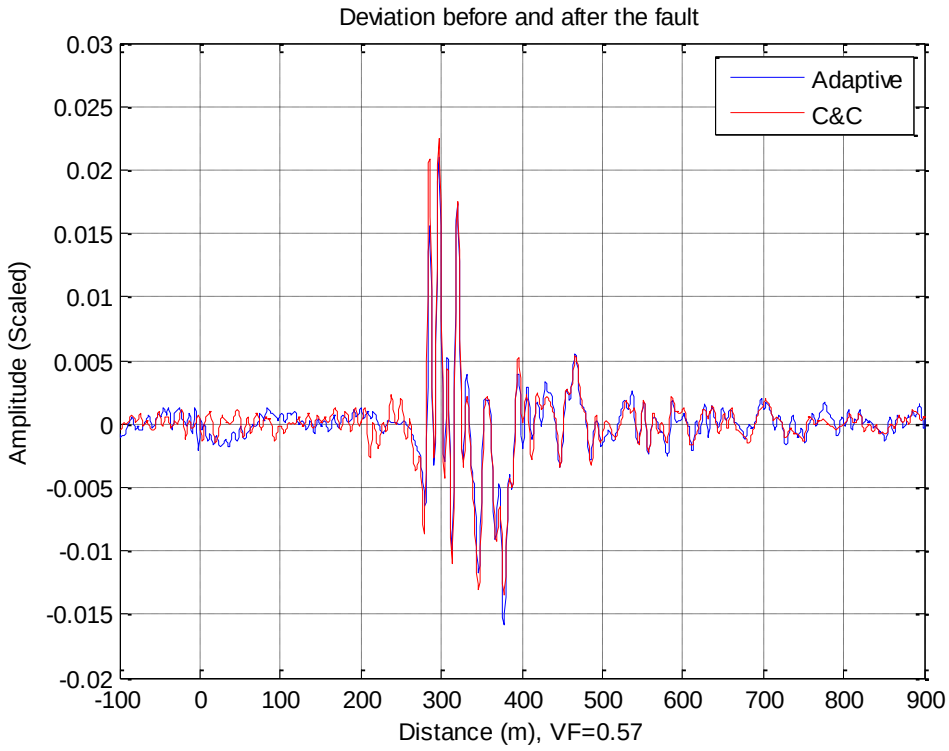


Figure 6-10: Deviation waveforms produced by C&C method and adaptive method of dataset 2

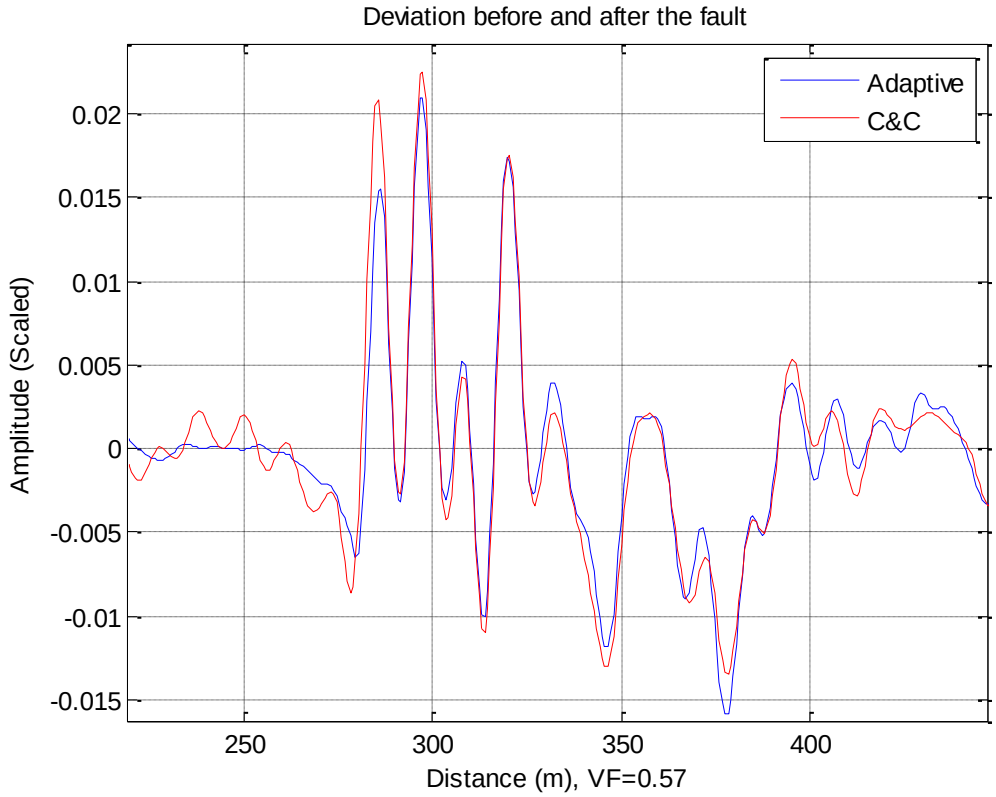


Figure 6-11: Deviation waveforms produced by C&C method and adaptive method of dataset 2 (Zoomed in)

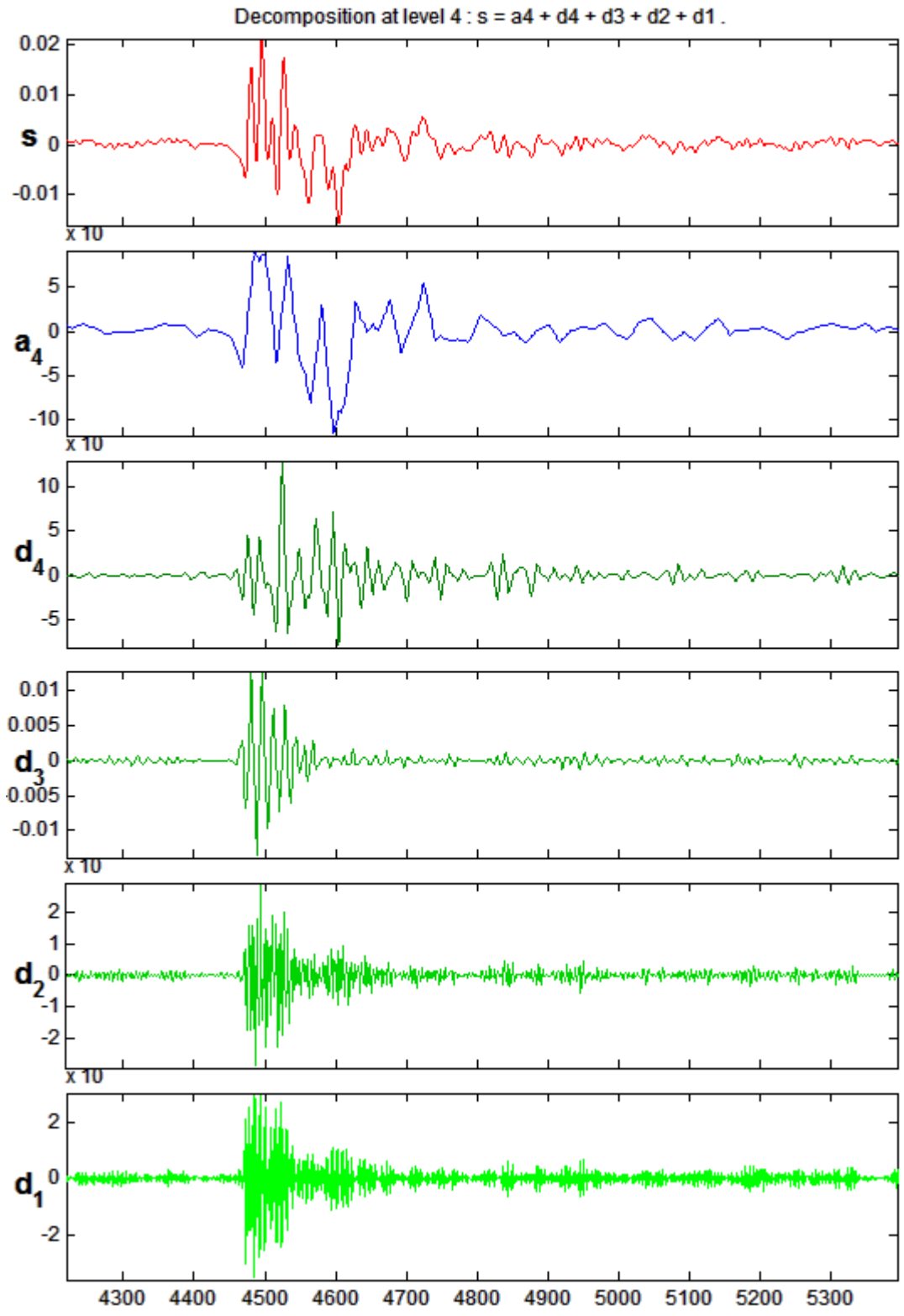


Figure 6-12: Decomposition map of dataset 2

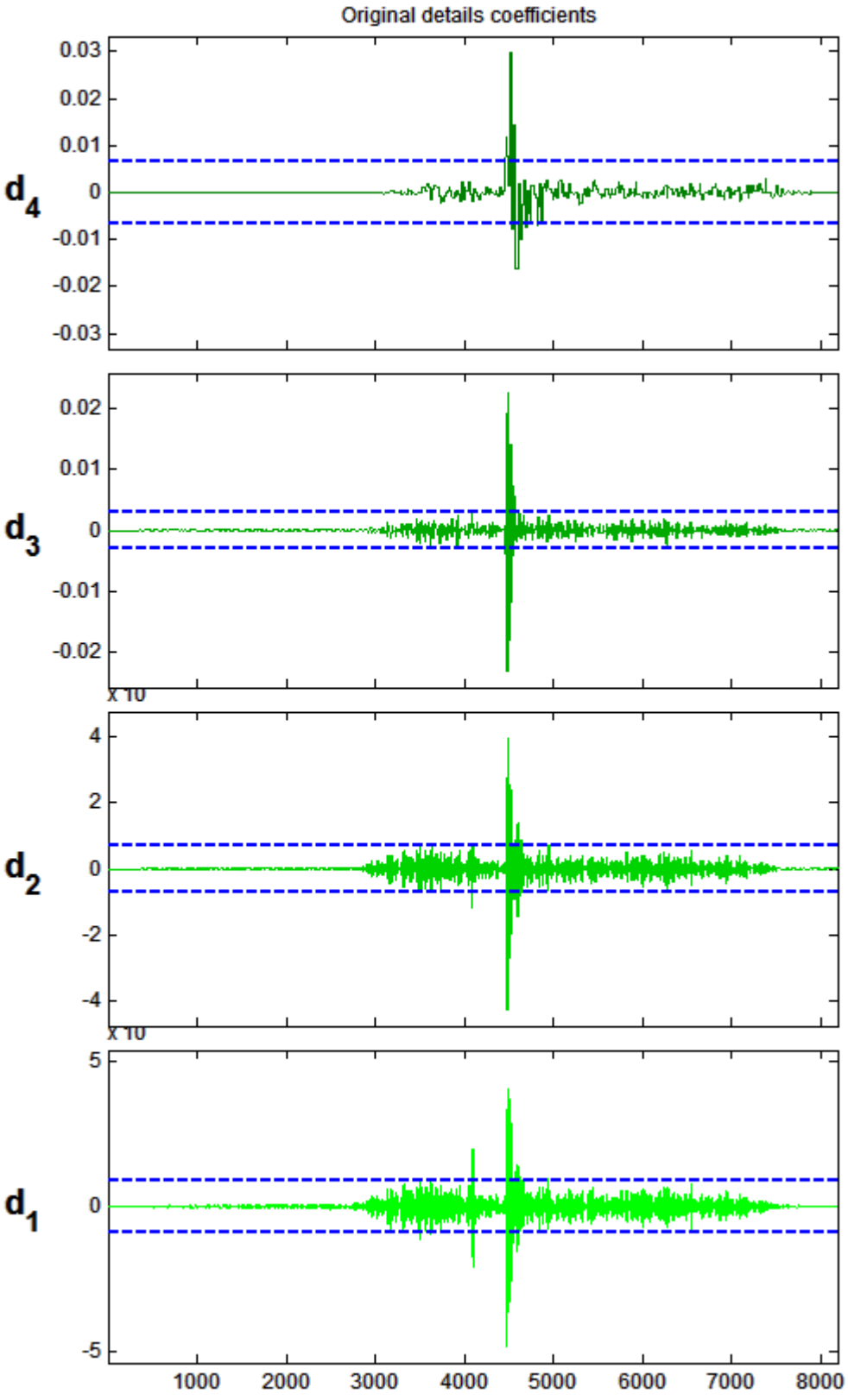


Figure 6-13: Wavelet rescaling of dataset 2

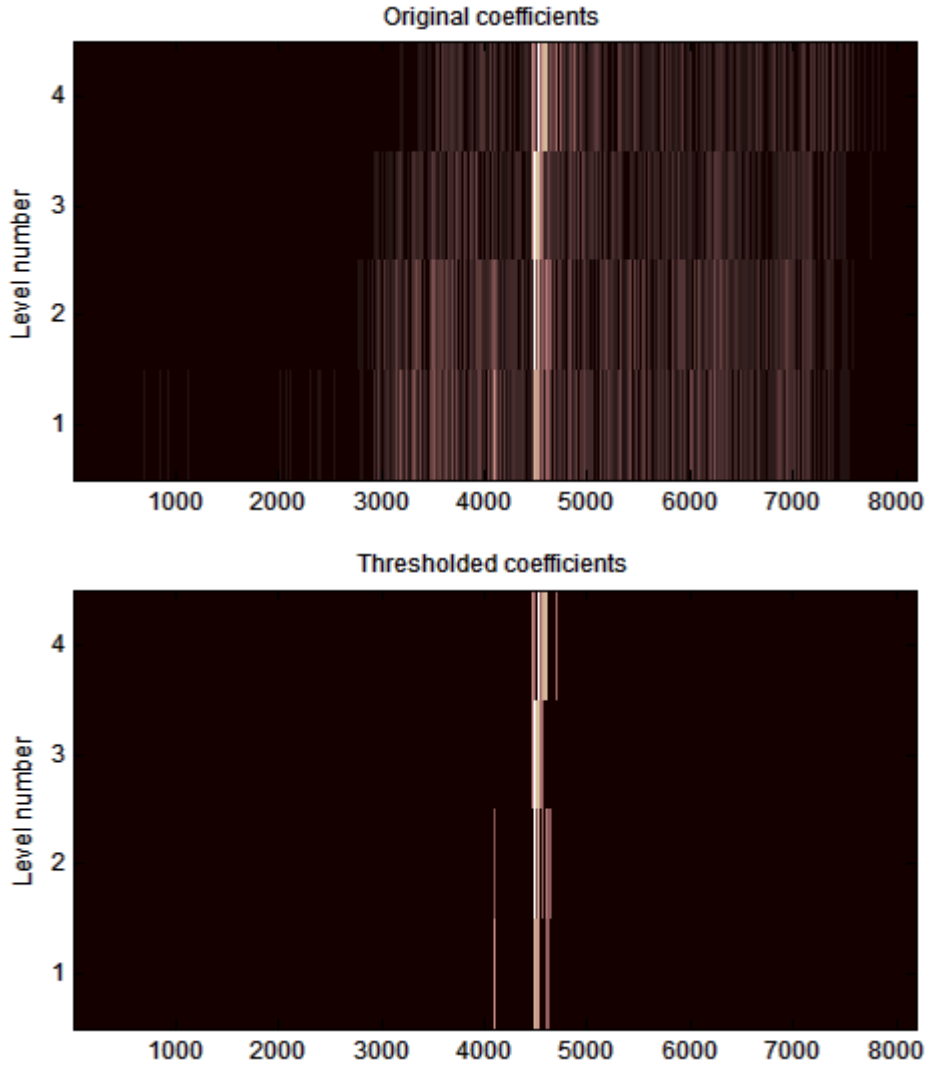


Figure 6-14: Wavelet coefficient map of dataset 1, before wavelet rescaling (a) and after wavelet rescaling (b)

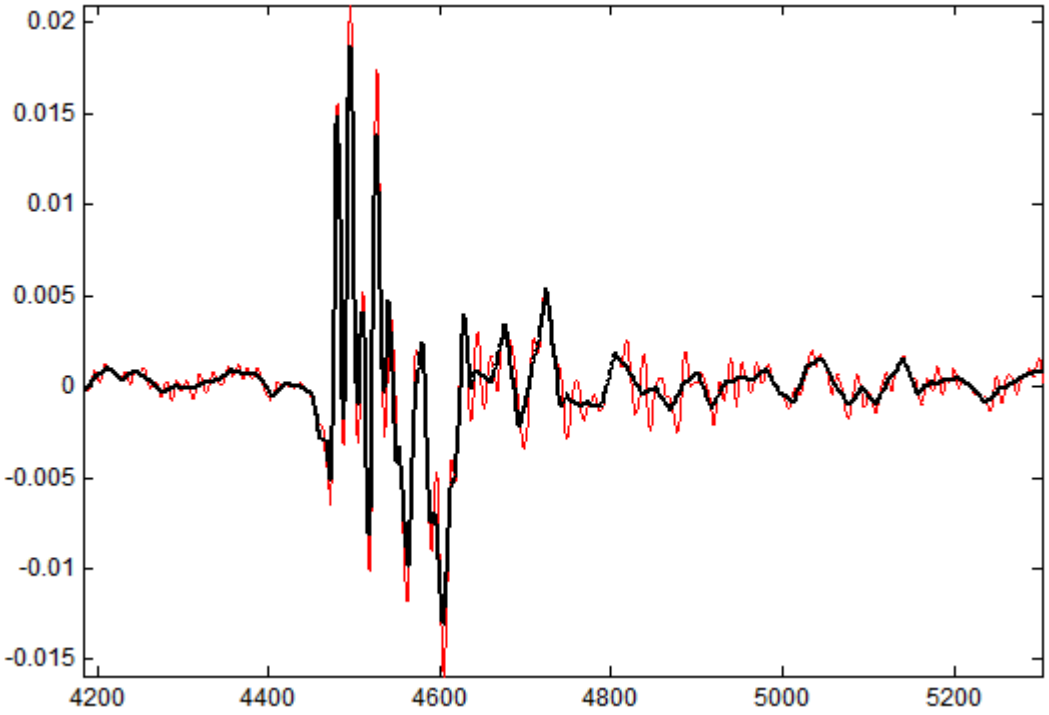


Figure 6-15: The deviation signal of dataset 2 before (a) and after (b) wavelet transform enhancement

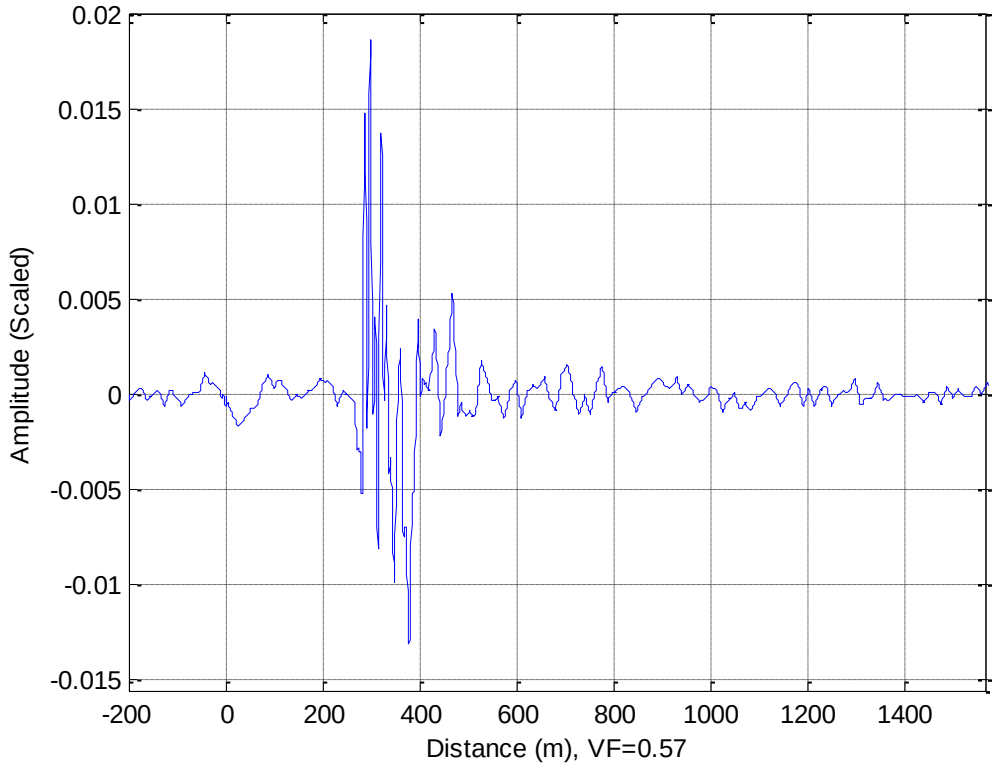


Figure 6-16: Final deviation waveform of dataset 2 after adaptive and wavelet enhancement

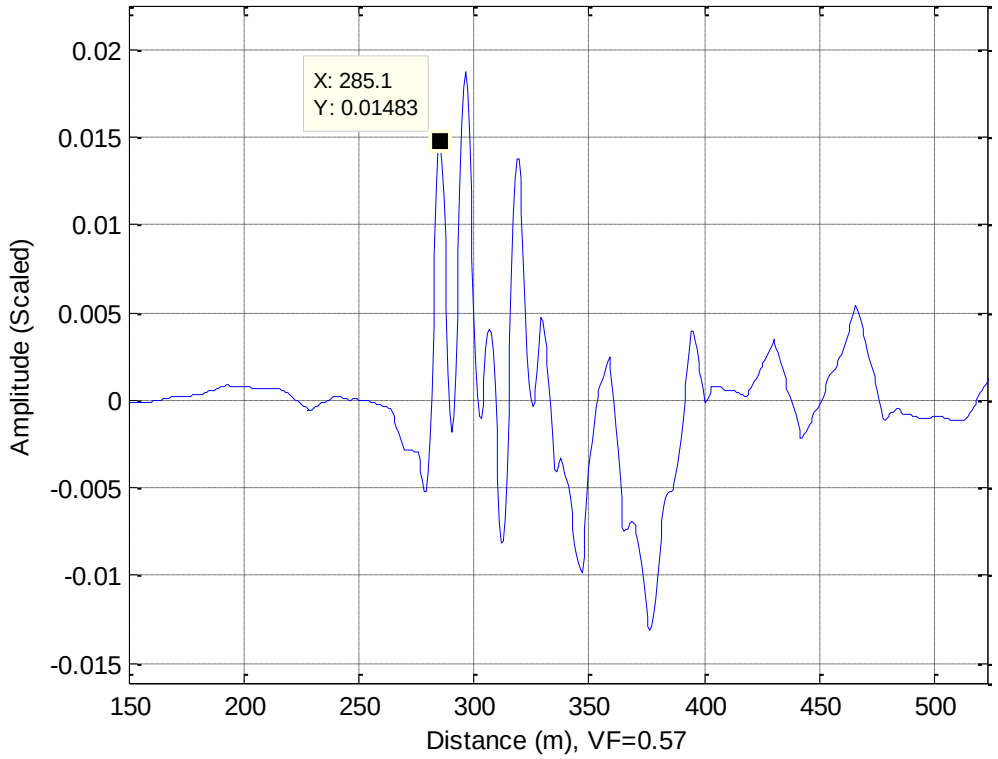


Figure 6-17: Final deviation waveform of dataset 2 after adaptive and wavelet enhancement (Zoomed in)

6.5 Alternative Method

6.5.1 Multi-phase comparing method

Where access is possible, the fault location may be identified by comparing the TDR reflection between different cable pairs of a multi-conductor cable network. This method is widely used by TDR based fault locating equipment, including many famous brands. However, this method is only suitable if a fault does not exist in all cable pairs of the cable network under test. For example, if one of the 3-phase cables were short-circuited and all conductors were melted and joined together, the reflections associated with different cable pairs would then change at the same time,

and no significant differences could be found by comparing the reflection waveforms of different cable pairs.

The disadvantage of this method is that the impedance of each cable pair is not exactly identical, and this will lead to inaccuracies in the results.

6.6 Conclusion

In this chapter, a new adaptive and wavelet enhanced fault location technique based on pulse compression TDR is presented. Following this approach, the data is obtained using the pulse compression TDR, and then post-processed using the wavelet transform, after applying adaptive filtering to monitor major changes. The Symlets 3 wavelet family originally has a sharp tip signature, which is very suitable in exploring the spike-like output waveform from the pulse compression process. The wavelet process shows good results in two different network configurations; however, for practical use, the weight of each decomposition level needs to be tuned according to the interrogation signal composition. Adaptive filtering affords the algorithm a certain degree of adjustment to slow changes in the network. The change may be due to temperature, humidity, load noise, or condition of the cable. This makes the adaptive algorithm capable of being deployed for long-time monitoring. However, the adaptive filter will generate a small tip around the zero point, as the reference spike in the compressed waveform is actually high bandwidth and a limited length adaptive filter is unable to handle such a high bandwidth signal. The advantages of adaptive filtering outweigh the disadvantages in this application, as shown in the results. The output shows that the accuracy of the combined method proposed here has less than 0.1% error, providing that precise knowledge of the velocity factor of the cable is known.

7 Conclusions and Future works

7.1 Conclusions

Cable fault locating techniques have been under development for decades. Conventional fault locating equipment, including many expensive fault locators provided by sound brands, is of an “after the event” manner. This is in contrast to the modern trend towards the development of fault locating techniques to continuously monitor the network condition, and to give the first alarm before the occurrence of wholesale failure. This is also desirable for construction of the next generation smart grids.

Chapter three investigated cable transient faults, which are commonly caused by poor insulation. The transient activity in distribution voltage cable networks appears as a low impedance arcing fault, but is self-extinguished in the first stage as oxides prevent the plasma channel from expanding, aided by the zero-crossing property of an AC supply. As transient faults are short in duration and low impedance, they can be addressed by a time domain reflectometry (TDR) based method, providing that the problems of high noise content generated by the transient activity and high attenuation of underground cable networks are solved.

Chapter four displayed a fully integrated hardware prototype TFM1000, successfully implementing the algorithms presented in this thesis. The soft core DSP with hardware acceleration in FPGA shows robustness and computational power. This is achieved by combining the flexibility of DSP, and the sequential/combinational logic capability of FPGA. For certain fix-point arithmetic, FFT or FIR filter for instance, implementation speed by using sequential logic in FPGA is significantly faster than

DSP. It is noteworthy that the maximum clock speed Fmax of the NIOS II soft processor depends upon the speed of the logic element inside the FPGA. The manufacturer marked maximum speed for a NIOS II core in the Altera Cyclone III series FPGA is around 160 MHz. However, due to the speed of external components and other FPGA functions, the NIOS II soft core cannot run at maximum speed. The maximum stable CPU running frequency in the TFM1000 was determined by test to be 120 MHz. If more computational power were required in further development, alternative high performance FPGAs such as the Stratix IV family may be considered. The total hardware cost for the TFM1000 was less than £500 (in the year 2011).

Chapter five presented a novel pulse compression enhanced method for transient fault monitoring and location. Using this method, pulse compression is the essential technique to enhance the TDR range resolution and noise immunity capability. Besides pulse compression, a self-comparing scheme was introduced to continuously monitor the reflection waveform of the cable network. To successfully employ this method, the following factors should be carefully considered:

- Select proper pulse compression parameters according to the cable network to be monitored. Improper parameters will result in high attenuation or low resolution. The factors to be considered include the high-frequency attenuation of the cable, the density of T-joints, the type of load, and the level of background noise.
- Obtain precise value of velocity of propagation of the cable type installed in the network. This value may be acquired directly from the manufacture's datasheet, or by measuring using a known length of cable of the same type.
- The measured fault distance is the 1-dimensional electrical length from the fault point to the measurement point. In complex cable networks, fault point in

the measured waveform may correspond to more than one physical point. In such cases, the solution is to use multiple units to determine the precise location, or to move the fault locator to another suitable measuring point according to the cable installation layout map.

The novel pulse compression enhanced fault location method with self-comparing scheme was tested in two different, live, real cable networks of different complexity; the results show satisfactory performance, with measurement error of less than 1%.

In Chapter six, the above method was further strengthened by employing adaptive filters and the wavelet transform. The resulting improvements can be viewed from two aspects. From one aspect, the adaptive filter enhanced the self-comparing scheme by providing adaptive capability. From the other aspect, the final result is processed by the wavelet transform to provide better observation.

The adaptive filter works by attempting to filter the input signal to match the reference signal (based on a number of previous waveforms). When the difference between the input signal and the reference signal is small, the filter will gradually adjust the filter coefficients, minimising the difference in the output. However, when the difference is significant, the adaptive filter is unable to instantly adjust and will output the difference. This is an advantage when the fault locator is deployed for long-term monitoring, due to the fact that cable parameters may change with the environment, and the adaptive self-comparing regime can prevent mis-triggering due to the accumulated change over a long period of time. The primary parameters of the adaptive filter are filter structure, length, and step size. Different filter structures, such as LMS and RLS, and their advantages and disadvantages have already been discussed in chapter two. The filter length and the step size can affect the accuracy of

prediction and convergence speed, respectively, and these parameters should be carefully selected according to the application.

The purpose of introducing the wavelet transform is to provide a better result by selective observation of the signal on multiple scales. As mentioned in Chapter 2, the wavelet transform is localized in both the frequency and time domain; therefore, it can be used to extract better time resolution for high frequency components, which are likely due to the discontinuities because of T-joints, loads, and faults. In addition, the wavelet transform can also filter out the noise and provide a more "clean" result.

Tests of the adaptive and wavelet enhanced algorithm were performed based upon the same cable networks described in chapter five. The results show that the error rate is further reduced to less than 0.1%. This further suggests that the adaptive filter and wavelet transform enhanced pulse compression TDR method gives a clearer output, which further reduces the complexity and increases the fault identification capability.

7.2 Recommendations for Future work

The following technologies were noted during the research, however were not expanded upon due to time limitations; they are recommended for further possible improvements.

Quadrature Amplitude Modulation (QAM): QAM is a widely used technique in communication systems. By using QAM, it is possible to modulate the two individual carrier signals into one analogue channel without interference with each other. This technique may make it possible to enhance the bandwidth of the pulse compression, by using a complex chirp signal as the reference pulse. There are two possible ways to implement QAM based on current hardware. On the one hand, it is possible to modify

the signalling sequence generator, so that the real and imaginary part can be transmitted in turn. However this will cause the sampling rate to be reduced by half due to the fact that the frontend is required to transmit/receive twice for a complex number. On the other hand, it is possible to add another set of DAC/ADC in the system. One DAC is used for generating the real part whilst the other one is for generating the complex part. The complex output will be shifted -90 degree and mixed with the real output by the analog quadrature modulator (e.g. AD8349 from Analog Devices), and then send to the following transmission circuitry. Similarly, the receiving end performs the inverse QAM and the real part and complex part will be fed to two ADCs. This will add complexity to the hardware circuitry but will maintain maximum performance.

Non-linear frequency modulation: Apart from the linear frequency modulation used in this thesis, non-linear frequency modulation may be used to improve the bandwidth and reduce the side lobes because of the increasing cross-correlation recognition from noise. The use of non-linear frequency modulation may introduce complexity and add unpredictable behaviour to the compression process however the advantage normally outweighs the disadvantage.

Novel windows: As described in previous chapters, the window function can aid suppression of side lobes associated with the pulse compression computation. Besides the conventional types of window, novel windows are becoming popular due to enhanced selectivity. However, novel windows are likely to be application-specific, and therefore their behaviour in pulse compression must be determined before application.

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9 Appendices

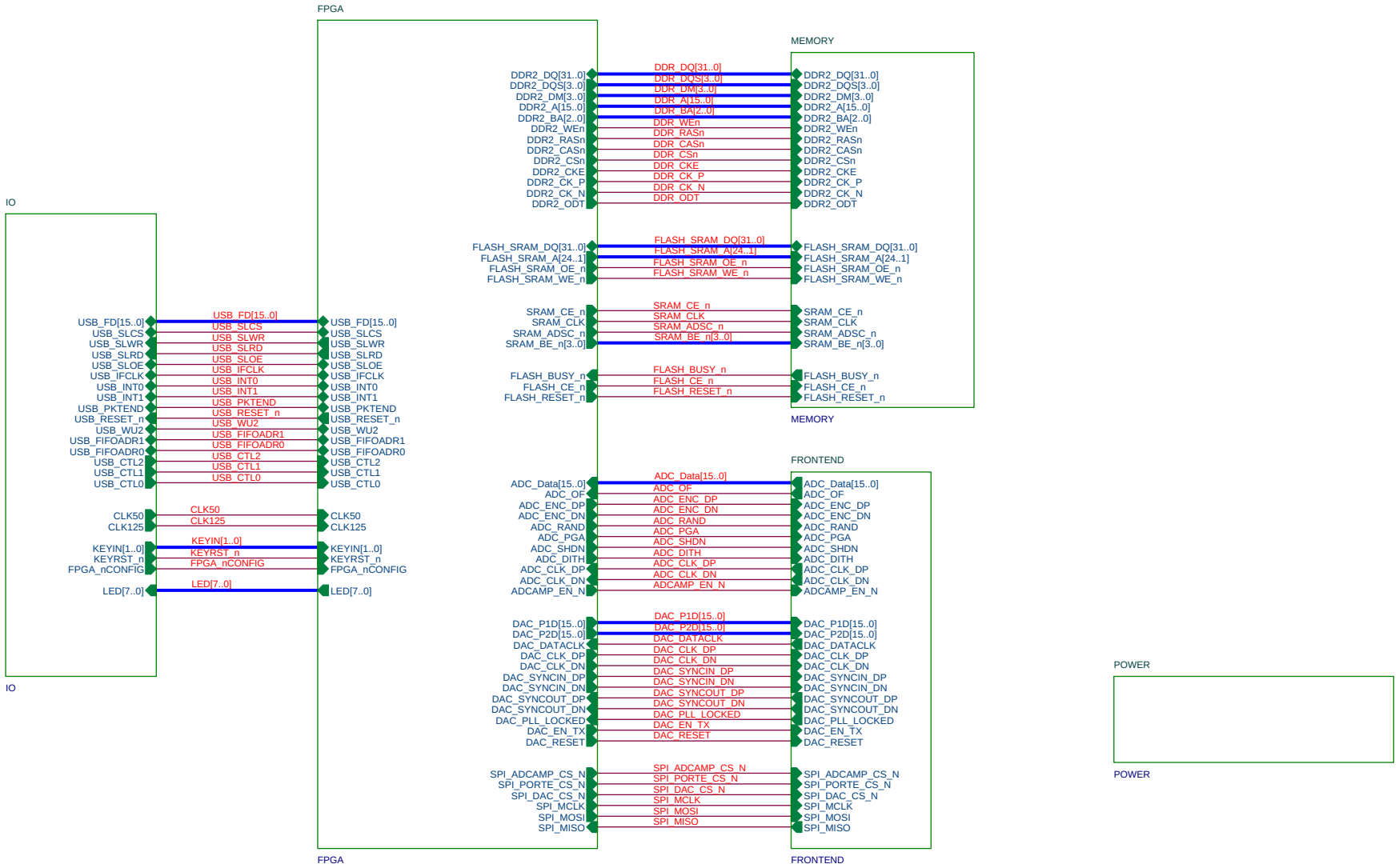
9.1 Automatic cable impedance code

```
CLEAR SCREEN
 ASSIGN @Hp4395 TO 800
 OUTPUT @Hp4395;"PRES"
 OUTPUT @Hp4395;"ZA"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 !
 ! Interrupt Operation Set-up
 OUTPUT @Hp4395;"CLES"
 OUTPUT @Hp4395;"*SRE 32;*ESE 36"
 ON INTR 8 GOSUB Err_report !
 ENABLE INTR 8;2 !
 !
 OUTPUT @Hp4395;";DISA BASS"
 BEEP
 DISP "CONNECT 43961A KIT THEN PRESS Continue"
 GOSUB Keyin
 !
 GOSUB Setup
 GOSUB Calibration
 GOSUB Measure
 GOTO Ending
 !
 Setup:!
 DISP "Initialising Measurement"
 OUTPUT @Hp4395;"POIN 801"
 OUTPUT @Hp4395;"POWE 3"
 OUTPUT @Hp4395;"SWPT LOGF"
 OUTPUT @Hp4395;"STAR 10"
 OUTPUT @Hp4395;"STOP 250E6"
 OUTPUT @Hp4395;"BW 300"
 OUTPUT @Hp4395;"CHAN1"
 OUTPUT @Hp4395;"MEAS IMAG"
 OUTPUT @Hp4395;"AVER ON"
 OUTPUT @Hp4395;"AVERFACT 8"
 OUTPUT @Hp4395;"CHAN2"
 OUTPUT @Hp4395;"MEAS IPH"
 OUTPUT @Hp4395;"AVER ON"
 OUTPUT @Hp4395;"AVERFACT 8"
 OUTPUT @Hp4395;"DUAC ON"
 OUTPUT @Hp4395;"COUC ON"
 OUTPUT @Hp4395;"MKRCOUP ON"
 OUTPUT @Hp4395;"CHAN1"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 RETURN
 !
 Calibration: !
 BEEP
 OUTPUT @Hp4395;"USKEY"
 DISP "DO CALIBRATION? YES/NO"
 Cal_confirm: !
 ON KEY 1 LABEL "YES" GOTO Cal_start
 ON KEY 2 LABEL "" GOTO Calibration
 ON KEY 3 LABEL "NO" GOTO Cal_end
 ON KEY 4 LABEL "" GOTO Calibration
 ON KEY 5 LABEL "" GOTO Calibration
 ON KEY 6 LABEL "" GOTO Calibration
 ON KEY 7 LABEL "" GOTO Calibration
 ON KEY 8 LABEL "" GOTO Calibration
 GOTO Cal_confirm
 Cal_start: !
 OFF KEY
 OUTPUT @Hp4395;"CALK APC7"
 OUTPUT @Hp4395;"BW 300;AVERFACT 8;AVER ON"
 DISP "PRESS Continue FOR OPEN CALIBRATION"
 GOSUB Keyin
 DISP "OPEN CALIBRATION IN PROGRESS..."
 OUTPUT @Hp4395;"CALI IMP"
 OUTPUT @Hp4395;"CLASIMPA"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 DISP "PRESS Continue FOR SHORT CALIBRATION"
 GOSUB Keyin
 DISP "SHORT CALIBRATION IN PROGRESS..."
 OUTPUT @Hp4395;"CLASIMPB"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 DISP "PRESS Continue FOR LOAD CALIBRATION"
 GOSUB Keyin
 DISP "LOAD CALIBRATION IN PROGRESS..."
 OUTPUT @Hp4395;"CLASIMPC"
 OUTPUT @Hp4395;"*WAI"
 OUTPUT @Hp4395;"SAVIMP"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 !
 DISP "CONNECT 16093A AND PRESS Continue"
 GOSUB Keyin
 OUTPUT @Hp4395;"FIXT HP16193"
 OUTPUT @Hp4395;"MODIFIX"
 OUTPUT @Hp4395;"FIXE 3.4E-3"
 OUTPUT @Hp4395;"LABEFIX ""16093A"""
 OUTPUT @Hp4395;"FIXKDONE"
 !
 !
 DISP "PRESS Continue FOR OPEN COMPENSATION"
 GOSUB Keyin
 DISP "OPEN COMPENSATION IN PROGRESS..."
 OUTPUT @Hp4395;"COMP;COMCA"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 DISP "PRESS Continue FOR SHORT COMPENSATION"
 GOSUB Keyin
 DISP "SHORT COMPENSATION IN PROGRESS..."
 OUTPUT @Hp4395;"COMCB"
 OUTPUT @Hp4395;"*WAI"
 OUTPUT @Hp4395;"SAVCOM"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 Cal_end:  !
 !
 RETURN
 !
 Measure:!
 Numberoffile=0
 Testset: !
 Numberoffile=Numberoffile+1
 CLEAR SCREEN
 DISP "PREPARING DISK..."
 OUTPUT @Hp4395;";STODDISK"
```

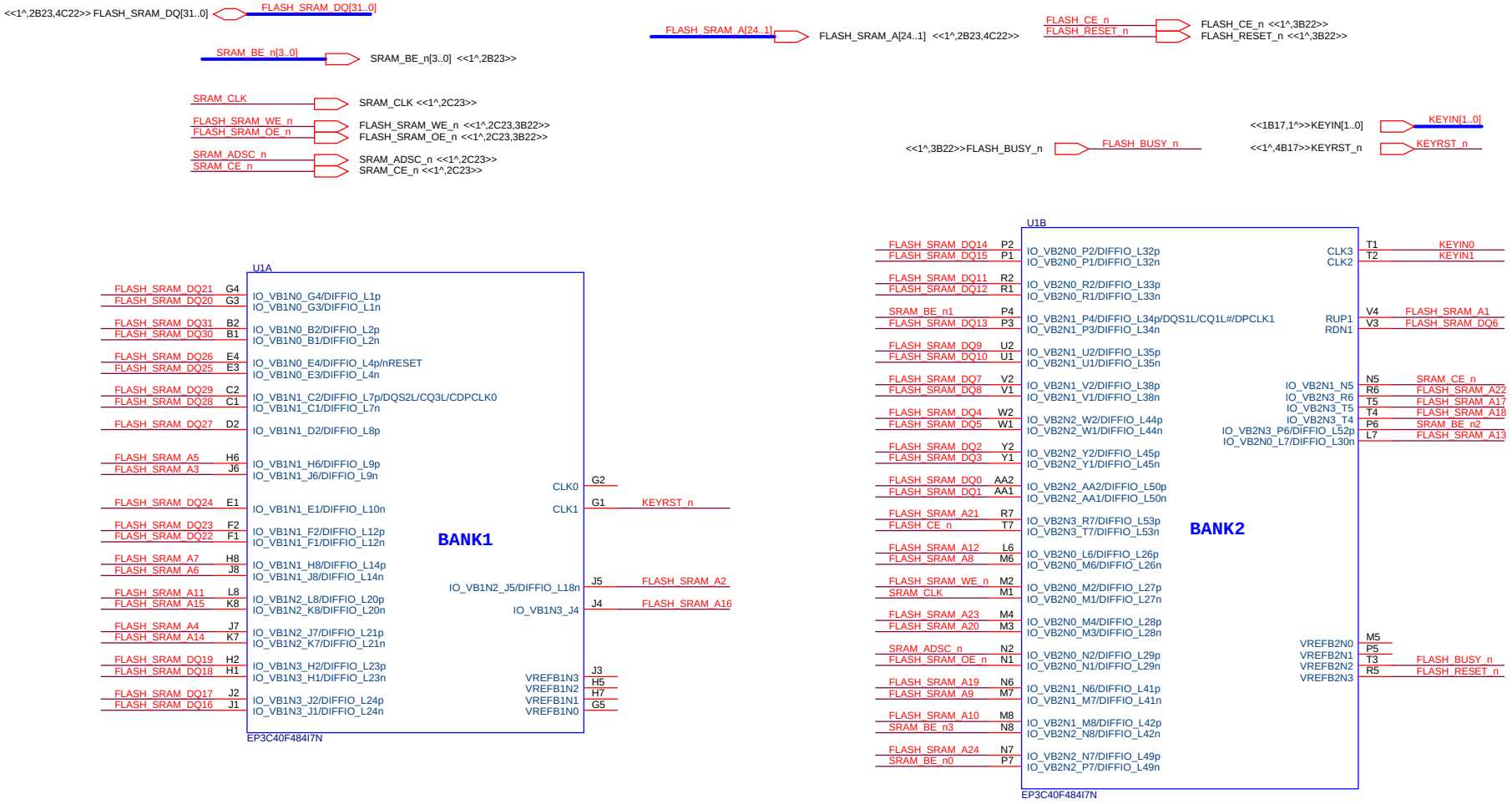
```
 IF Numberoffile>1 THEN
 OUTPUT @Hp4395;";CHAD ""..""""
 END IF
 OUTPUT @Hp4395;";CRED
""SET";CHR$(48+Numberoffile);"""""
 OUTPUT @Hp4395;";CHAD
""SET";CHR$(48+Numberoffile);"""""
 BEEP
 DISP "SETUP UP FOR OPEN-END
MEASUREMENT No.";CHR$(48+Numberoffile)
 GOSUB Keyin
 DISP "OPEN MEASUREMENT IN PROGRESS..."
 !
 OUTPUT @Hp4395;"REST"
 FOR I=2 TO 1 STEP -1
 OUTPUT @Hp4395;"CHAN";CHR$(48+I)
 OUTPUT @Hp4395;"*WAI"
 OUTPUT @Hp4395;"NUMG 1"
 OUTPUT @Hp4395;"*WAI"
 OUTPUT @Hp4395;"AUTO"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 NEXT I
 !
 DISP "SAVING OPEN Z TO DISK NOW..."
 GOSUB Pre_mem
 OUTPUT @Hp4395;";SAVDTIF ""OPNTIF"""
 OUTPUT @Hp4395;";SAVDASC ""OPNIMP"""
 OUTPUT @Hp4395;";FILC
""OPNTIF.TIF"",""MEMORY"",""OPNTIF.TIF"",""DISK
"""
 OUTPUT @Hp4395;";FILC
""OPNIMP.TXT"",""MEMORY"",""OPNIMP.TXT"",""DI
SK"""
 !
 BEEP
 DISP "SETUP UP FOR SHORT-END
MEASUREMENT No.";CHR$(48+Numberoffile)
 GOSUB Keyin
 DISP "SHORT MEASUREMENT IN PROGRESS..."
 !
 FOR I=2 TO 1 STEP -1
 OUTPUT @Hp4395;"CHAN";CHR$(48+I)
 OUTPUT @Hp4395;"*WAI"
 OUTPUT @Hp4395;"NUMG 1"
 OUTPUT @Hp4395;"*WAI"
 OUTPUT @Hp4395;"AUTO"
 OUTPUT @Hp4395;"*OPC?"
 ENTER @Hp4395;Dummy
 NEXT I
 !
 DISP "SAVING SHORT Z TO DISK NOW..."
 GOSUB Pre_mem
 OUTPUT @Hp4395;";SAVDTIF ""SHTTIF"""
 OUTPUT @Hp4395;";SAVDASC ""SHTIMP"""
 OUTPUT @Hp4395;";FILC
""SHTTIF.TIF"",""MEMORY"",""SHTTIF.TIF"",""DISK"
""
 OUTPUT @Hp4395;";FILC
""SHTIMP.TXT"",""MEMORY"",""SHTIMP.TXT"",""DI
SK"""
 BEEP
 OUTPUT @Hp4395;"USKEY"
 DISP "MEASURE ANOTHER CABLE? YES/NO"
 Mea_key: !
 ON KEY 1 LABEL "YES" GOTO Testset
 ON KEY 2 LABEL "" GOTO Mea_key
 ON KEY 3 LABEL "NO" GOTO Measure_end
 ON KEY 4 LABEL "" GOTO Mea_key
 ON KEY 5 LABEL "" GOTO Mea_key
 ON KEY 6 LABEL "" GOTO Mea_key
 ON KEY 7 LABEL "" GOTO Mea_key
 ON KEY 8 LABEL "" GOTO Mea_key
 GOTO Mea_key
 !
 Measure_end: !
 OFF KEY
 !
 DISP "Measurement complete"
 !
 RETURN
 !
 Err_report: !
 OUTPUT @Hp4395;"OUTPERRO"
 ENTER @Hp4395;Err,Err$
 BEEP
 PRINT "ERROR DETECTED!"
 PRINT Err,Err$
 !
 A=SPOLL(@Hp4395)
 OUTPUT @Hp4395;"*ESR?"
 ENTER @Hp4395;Estat
 ENABLE INTR 8 ! \ When iBASIC is used, change
"7" to "8"
 RETURN
 !
 Keyin: !
 OUTPUT @Hp4395;"USKEY"
 ON KEY 1 LABEL "" GOTO Keyin
 ON KEY 2 LABEL "Continue" GOTO Keyin_end
 ON KEY 3 LABEL "" GOTO Keyin
 ON KEY 4 LABEL "" GOTO Keyin
 ON KEY 5 LABEL "" GOTO Keyin
 ON KEY 6 LABEL "" GOTO Keyin
 ON KEY 7 LABEL "" GOTO Keyin
 ON KEY 8 LABEL "" GOTO Keyin
 GOTO Keyin
 Keyin_end: !
 OFF KEY
 RETURN
 !
 Pre_mem: !
 OUTPUT @Hp4395;";STODMEMO"
 OUTPUT @Hp4395;";DISF DOS"
 OUTPUT @Hp4395;";INID"
 OUTPUT @Hp4395;";STODMEMO"
 OUTPUT @Hp4395;";SAVRAW OFF"
 OUTPUT @Hp4395;";SAVCAL ON"
 OUTPUT @Hp4395;";SAVDAT OFF"
 OUTPUT @Hp4395;";SAVMEM OFF"
 OUTPUT @Hp4395;";SAVDTRC ON"
 OUTPUT @Hp4395;";SAVMTRC OFF"
 RETURN
 !
 Ending:!
 DISP "Program Finish"
 END
```

9.2 Schematic of TFM1000

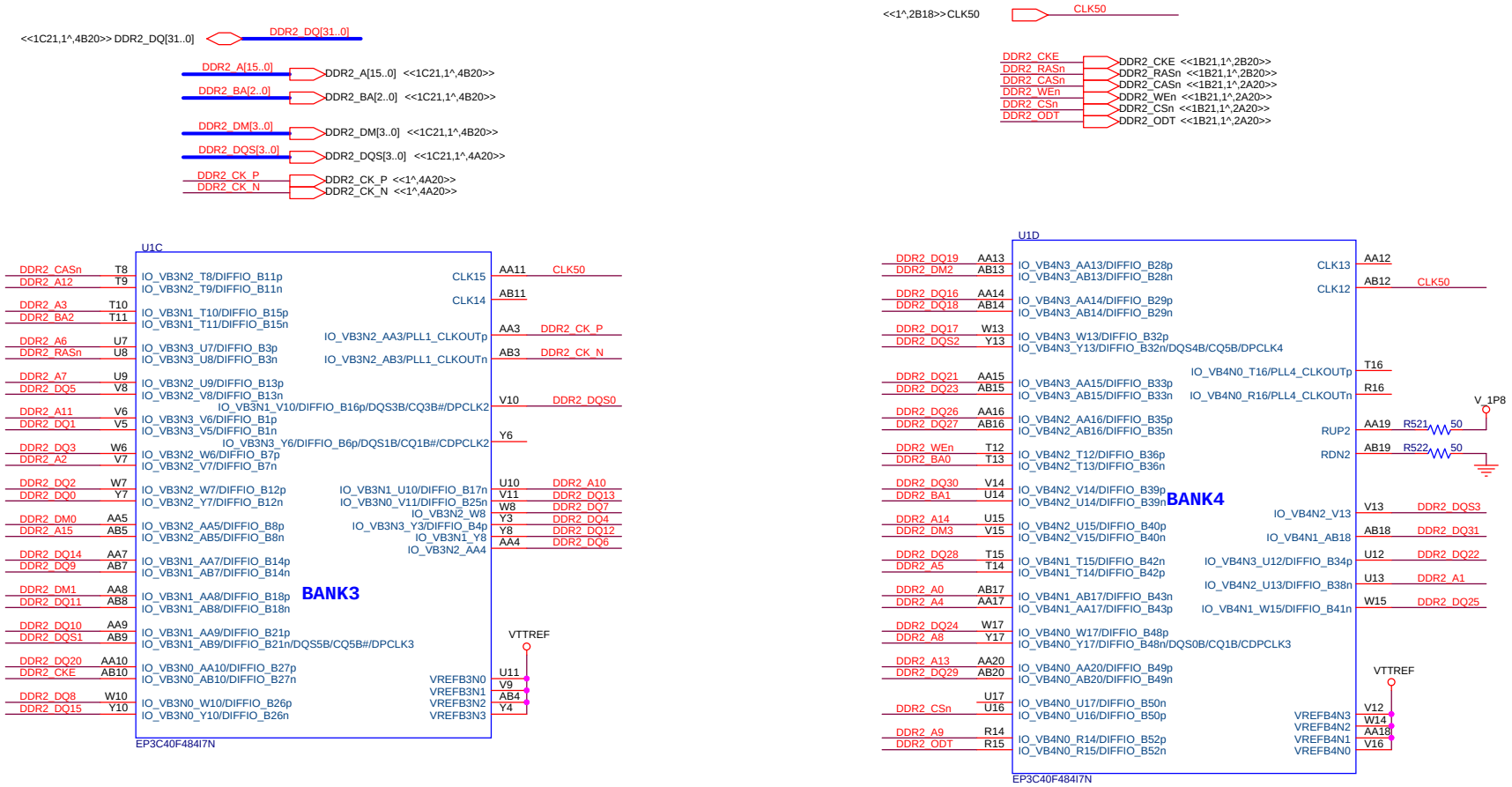
(24 Pages)



University of Strathclyde		
Title: Transient Fault Monitor		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
Date: Sunday, November 18, 2012	Sheet 1 of 24	



University of Strathclyde		
Title: FPGA - BANK 1 & BANK 2		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
Date: Sunday, November 18, 2012	Sheet 2 of 24	



University of Strathclyde		
Title: FPGA - BANK 3 & BANK 4		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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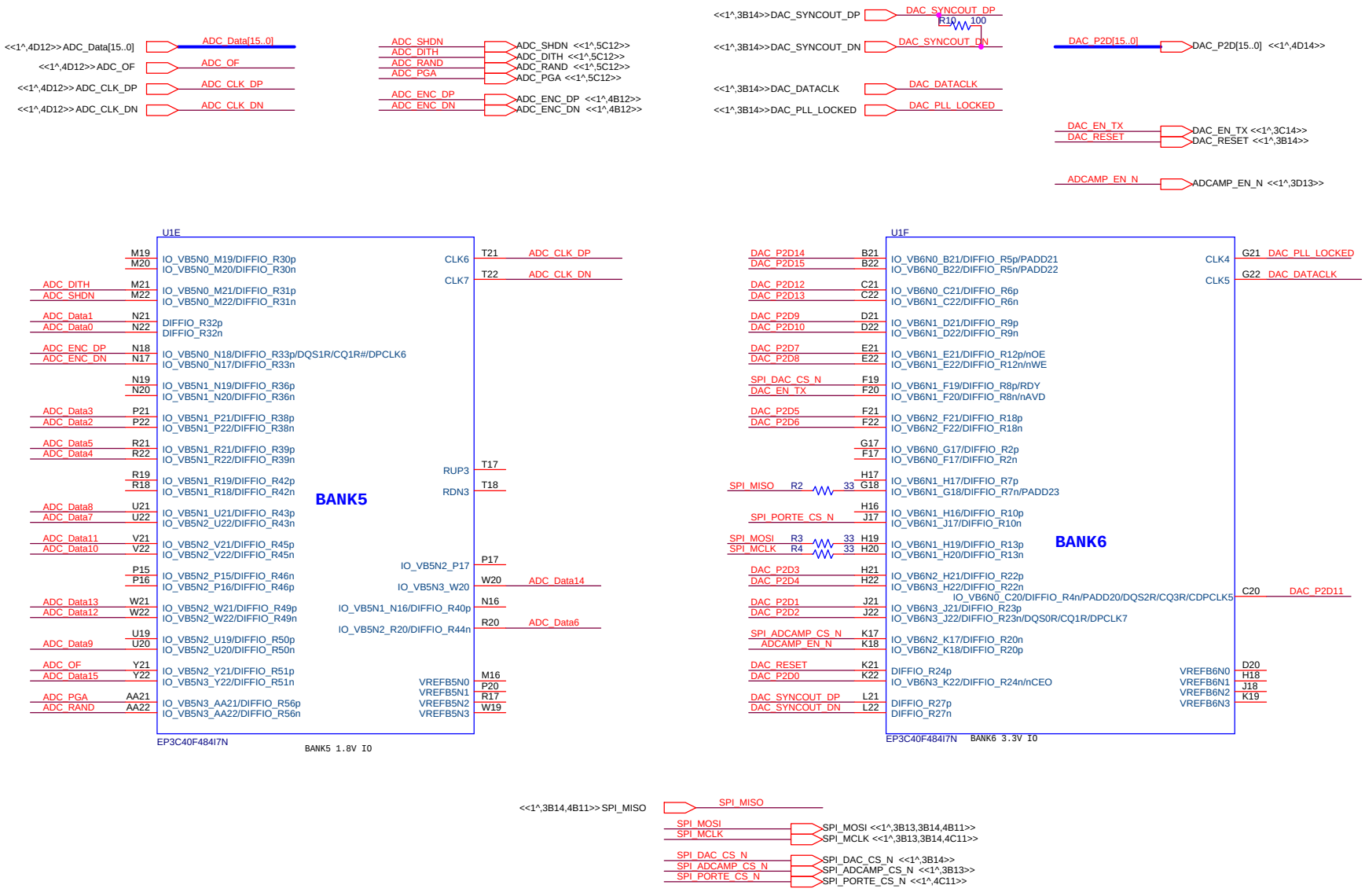

University of Strathclyde		
Title: FPGA - BANK 5 & BANK 6		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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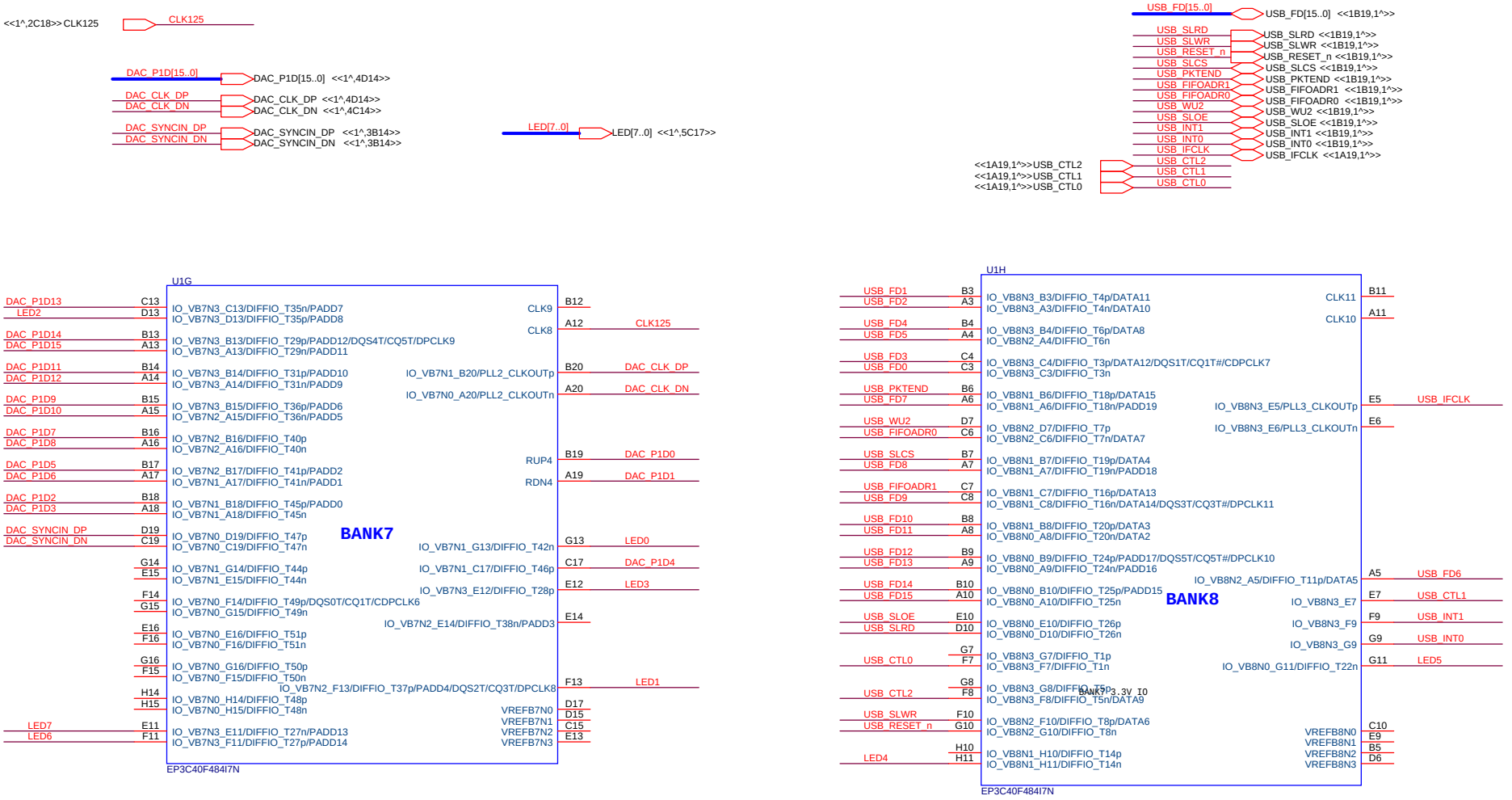

University of Strathclyde	
Title	FPGA - BANK 7 & BANK 8
Size A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012
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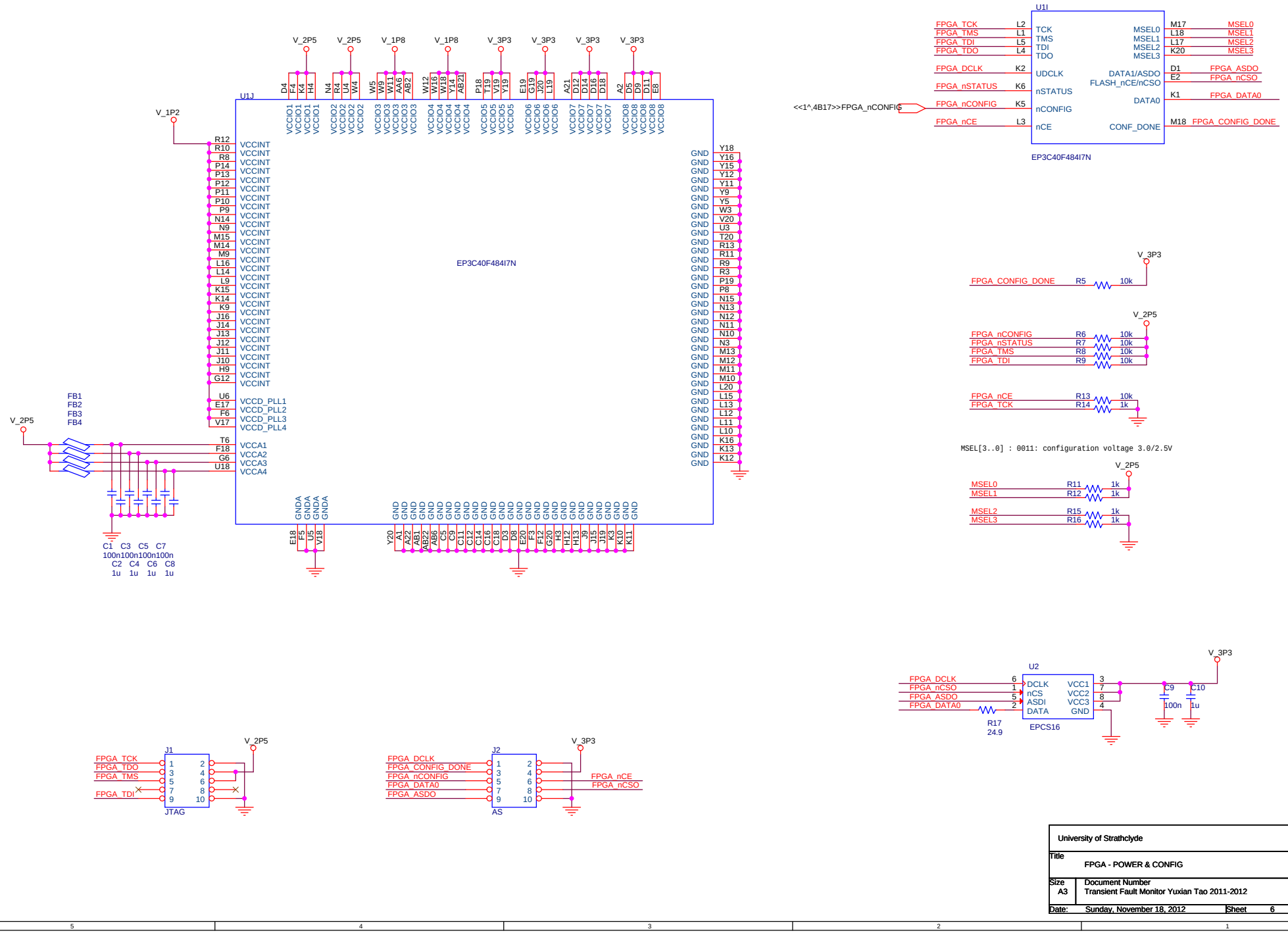
U1J
EP3C40F484I7N
V_1P2
V_2P5
V_1P8
V_3P3
U1I
EP3C40F484I7N
FPGA_TCK
FPGA_TMS
FPGA_TDI
FPGA_TDO
FPGA_DCLK
FPGA_nSTATUS
FPGA_nCONFIG
FPGA_nCE
<<1^,4B17>>FPGA_nCONFIG
MSEL0
MSEL1
MSEL2
MSEL3
FPGA_ASDO
FPGA_nCSO
FPGA_DATA0
FPGA_CONFIG_DONE
R5 10k
R6 10k
R7 10k
R8 10k
R9 10k
R13 10k
R14 1k
MSEL[3..0] : 0011: configuration voltage 3.0/2.5V
R11 1k
R12 1k
R15 1k
R16 1k
FB1
FB2
FB3
FB4
C1 C3 C5 C7
100n100n100n100n
C2 C4 C6 C8
1u 1u 1u 1u
J1
JTAG
J2
AS
U2
EPCS16
R17
24.9
C9
100n
C10
1u
University of Strathclyde
Title
FPGA - POWER & CONFIG
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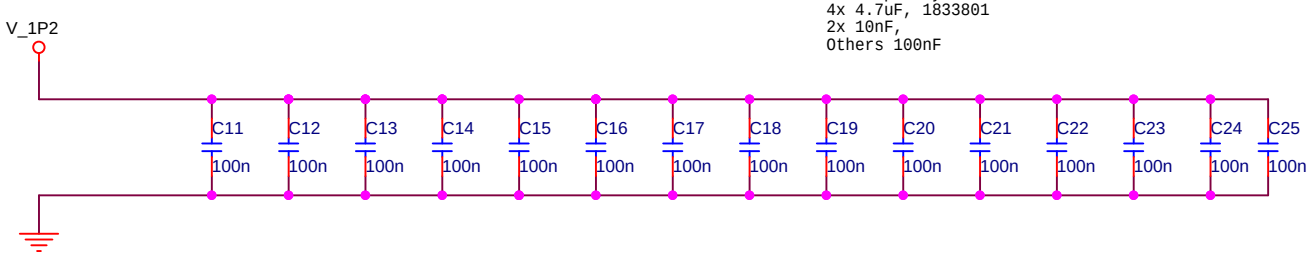
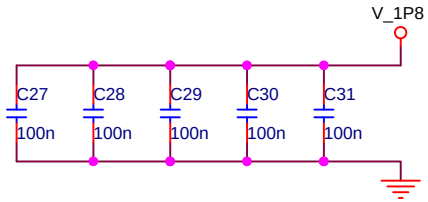
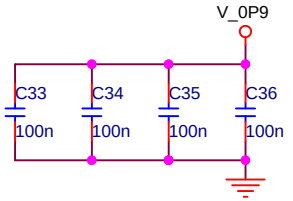
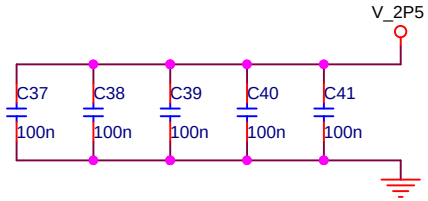
24

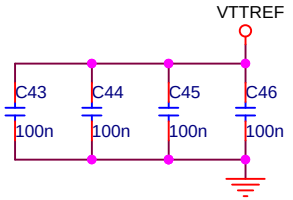
The capacity varied:
4x 4.7uF, 1833801
2x 10nF,
Others 100nF

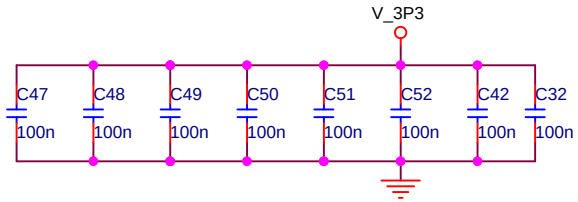












University of Strathclyde		
Title: FPGA - Decoupling		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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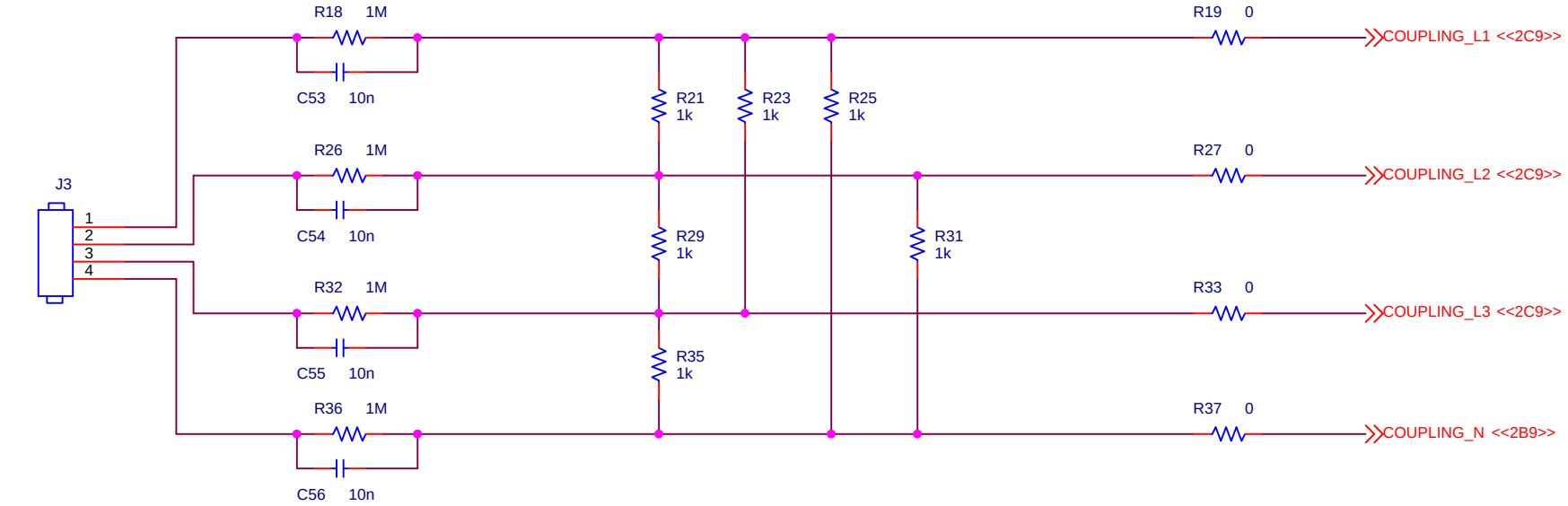

According Plug:
RS Stock No. 710-0150 Manufacturer Tyco Electronics Manufacturers Part No. 282807-4

University of Strathclyde		
Title: FRONTEND - COUPLING		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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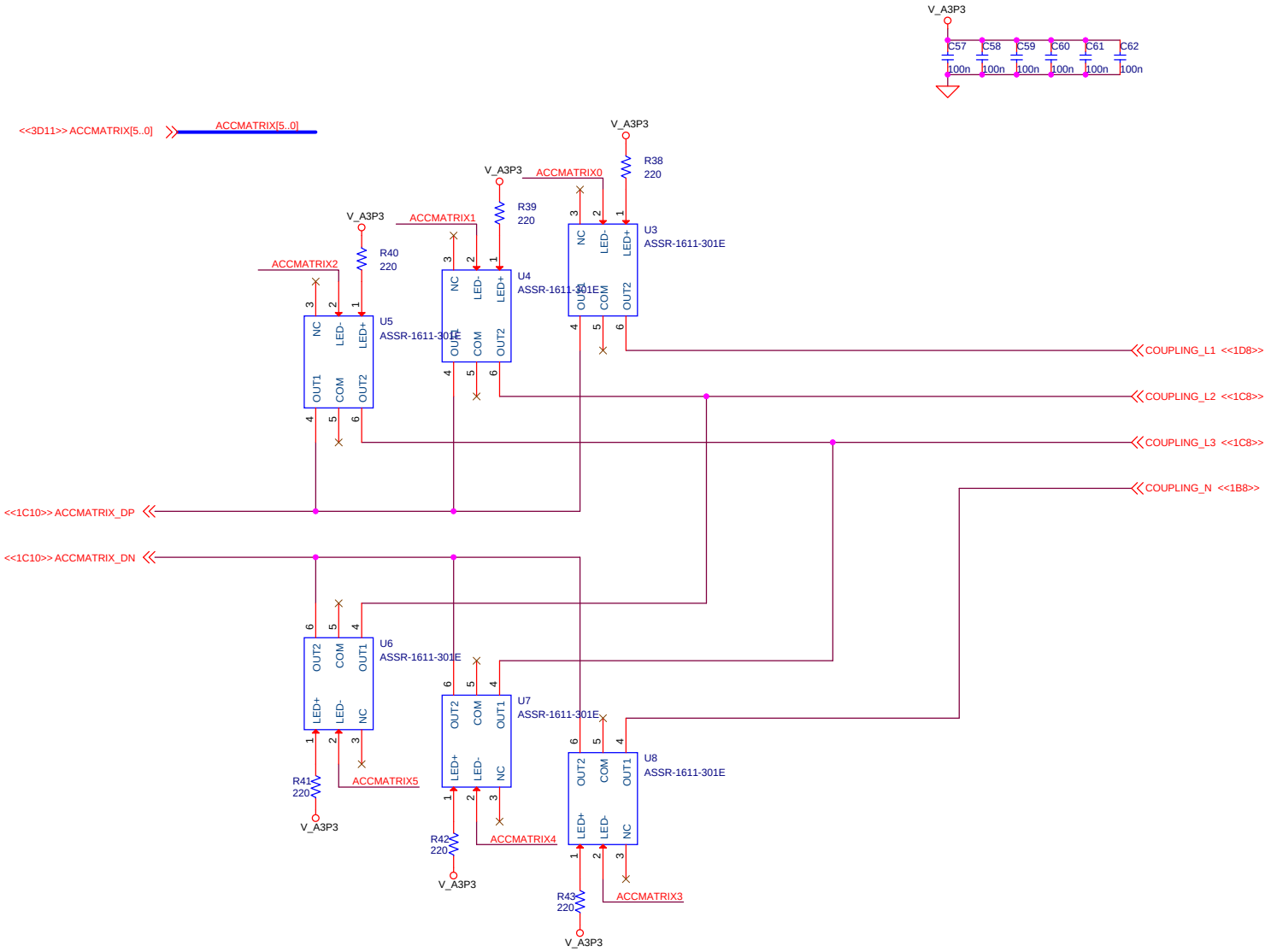

University of Strathclyde		
Title: FRONTEND - ACCESS MATRIX		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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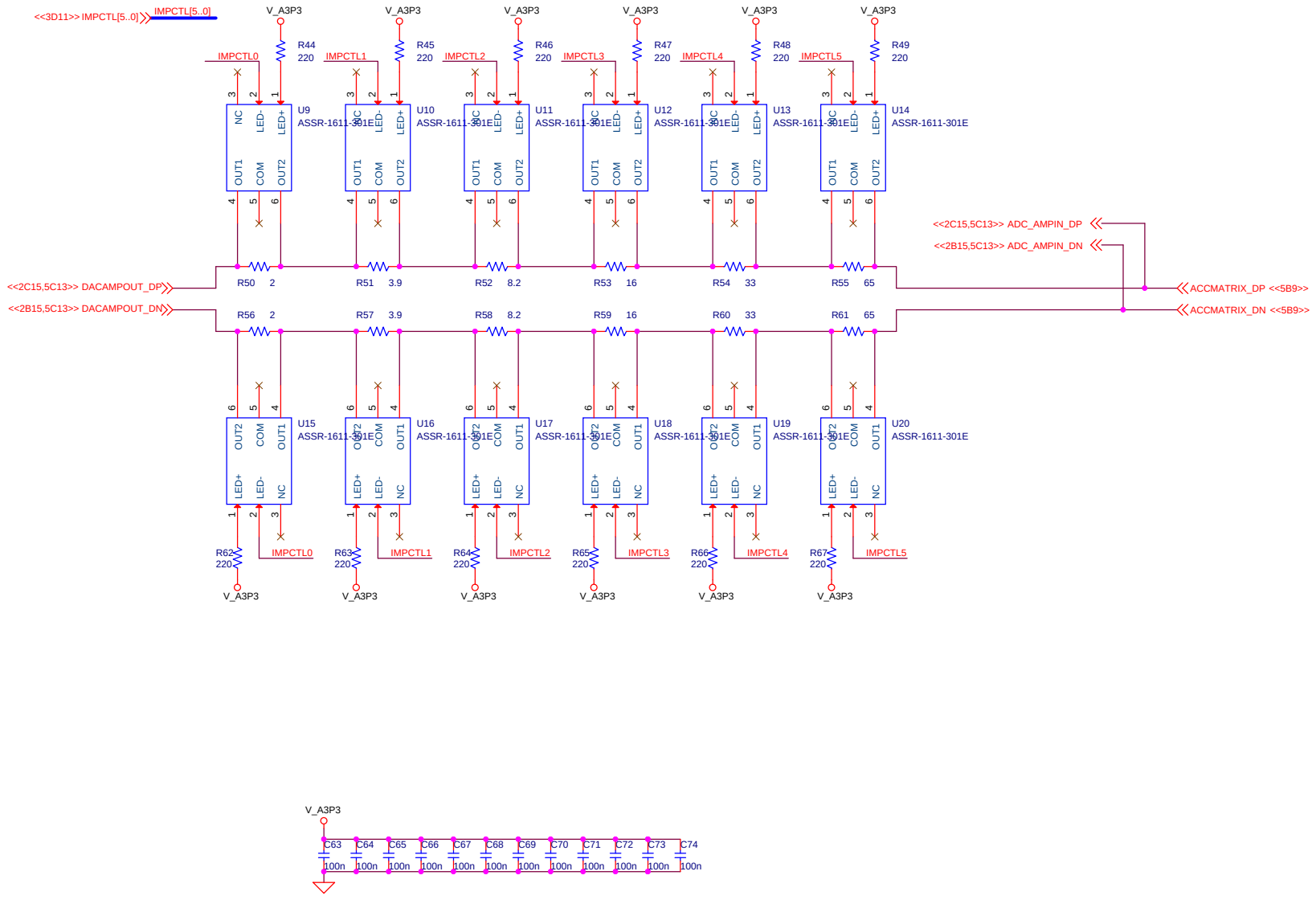

University of Strathclyde		
Title: FRONTEND - IMPEDANCE		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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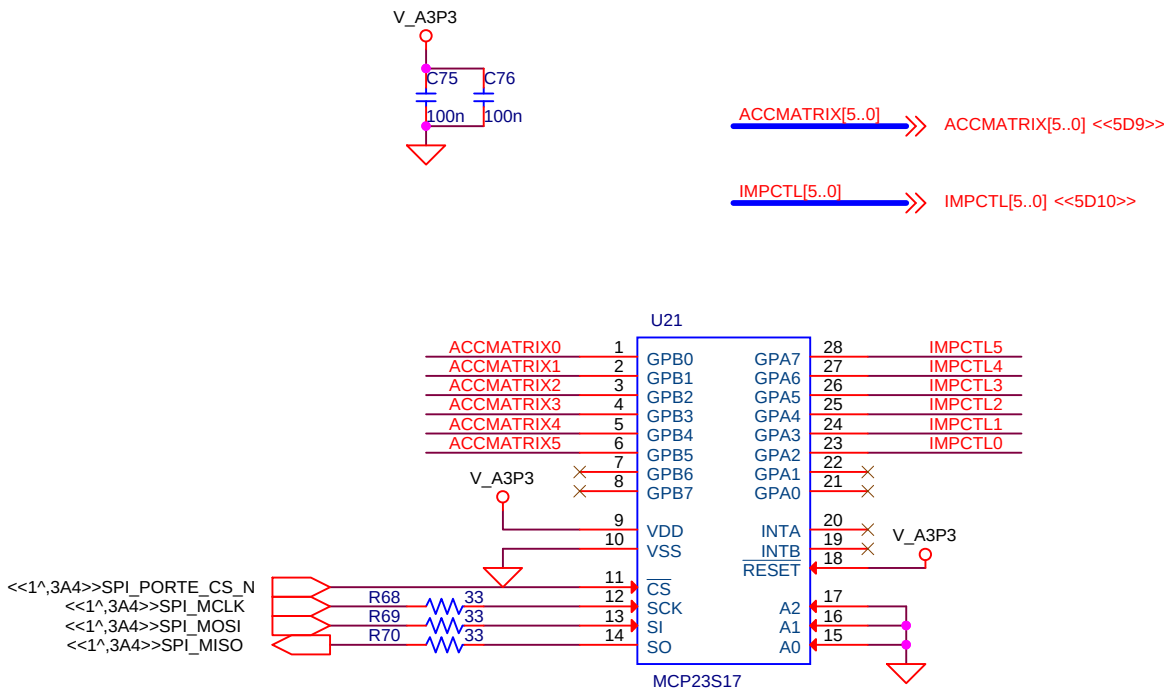

University of Strathclyde		
Title: FRONTEND - SPI PORT EXTENDER		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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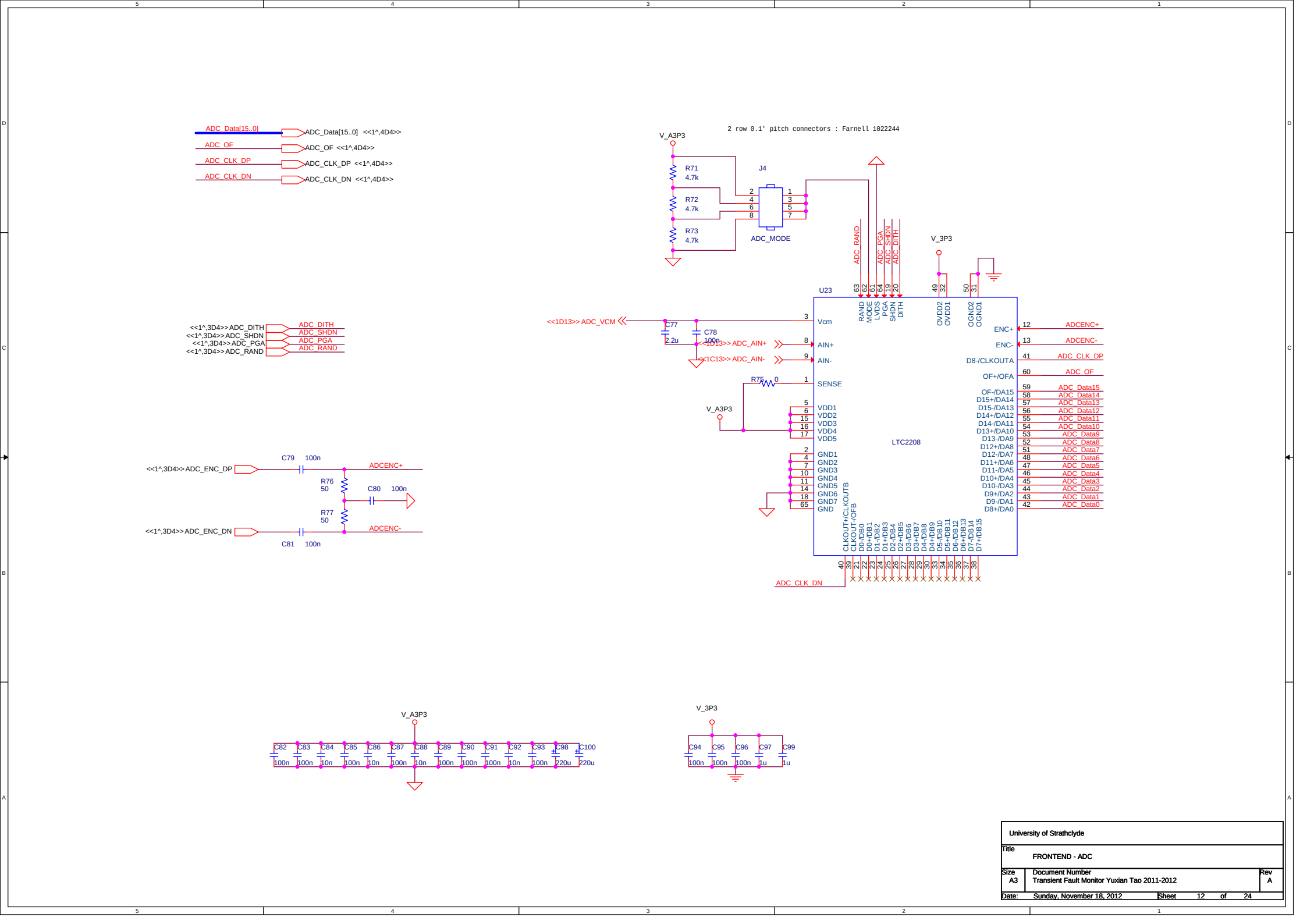

University of Strathclyde		
Title: FRONTEND - ADC		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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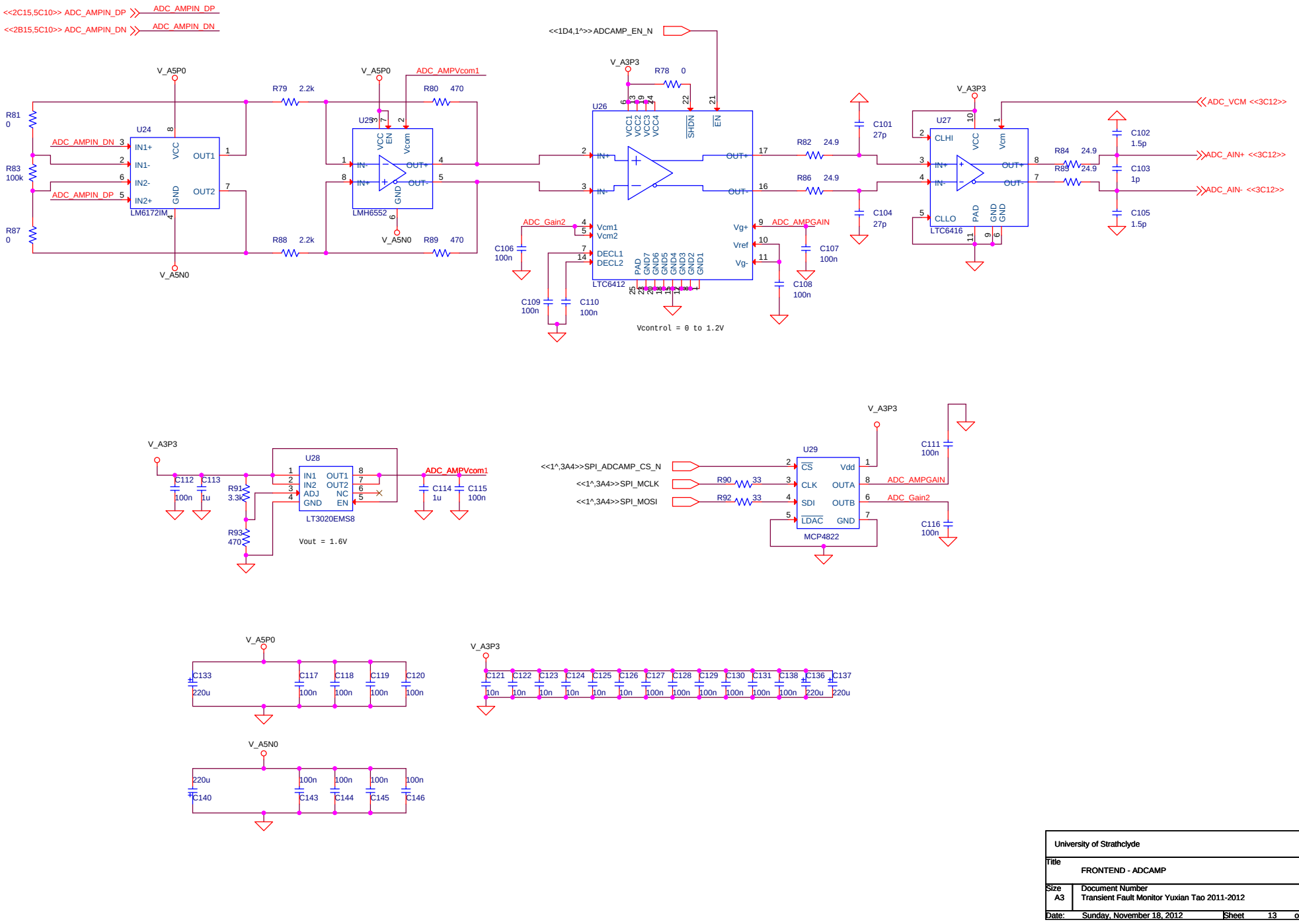

University of Strathclyde		
Title: FRONTEND - ADCAMP		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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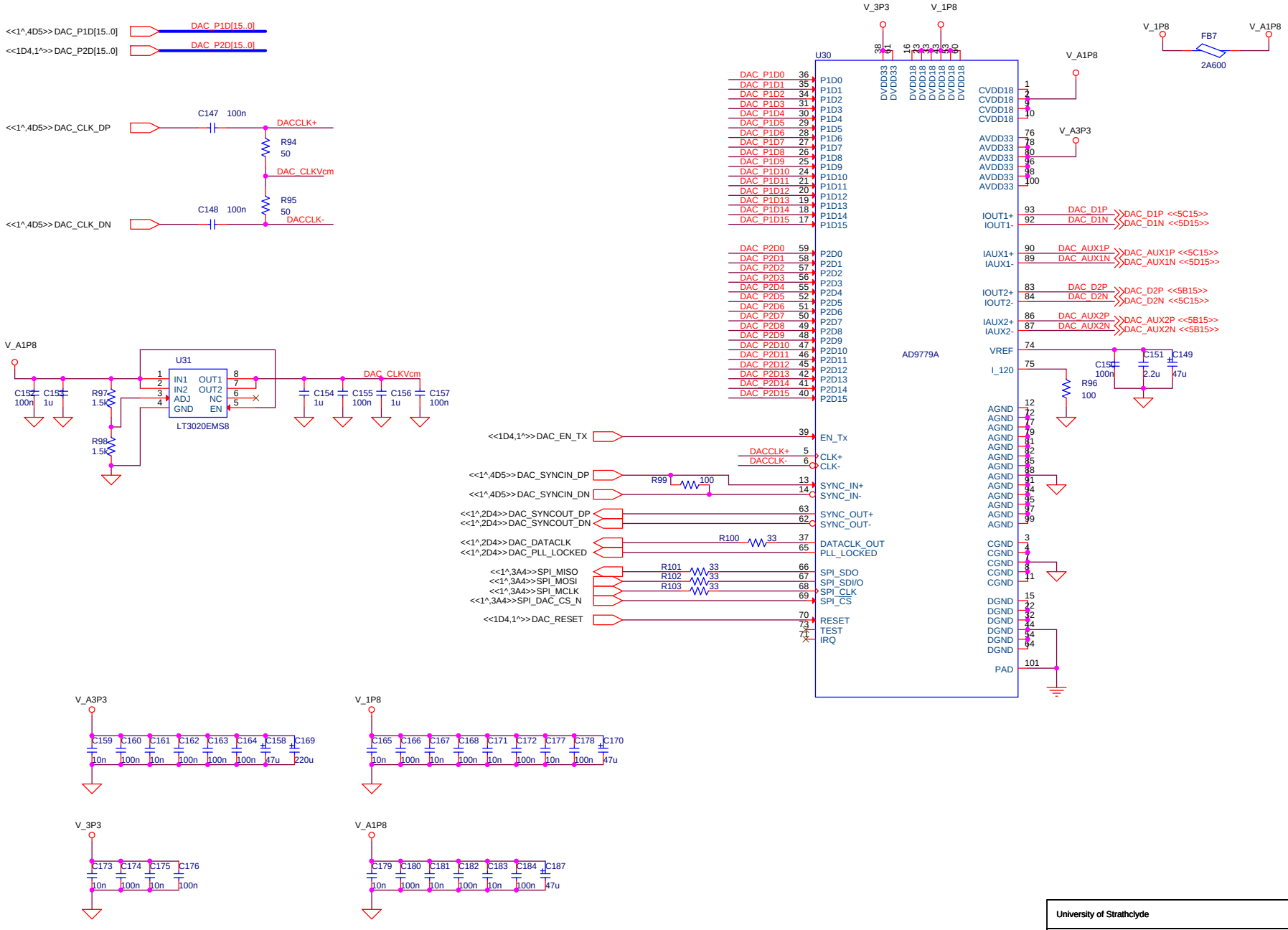

University of Strathclyde		
Title: FRONTEND - DAC		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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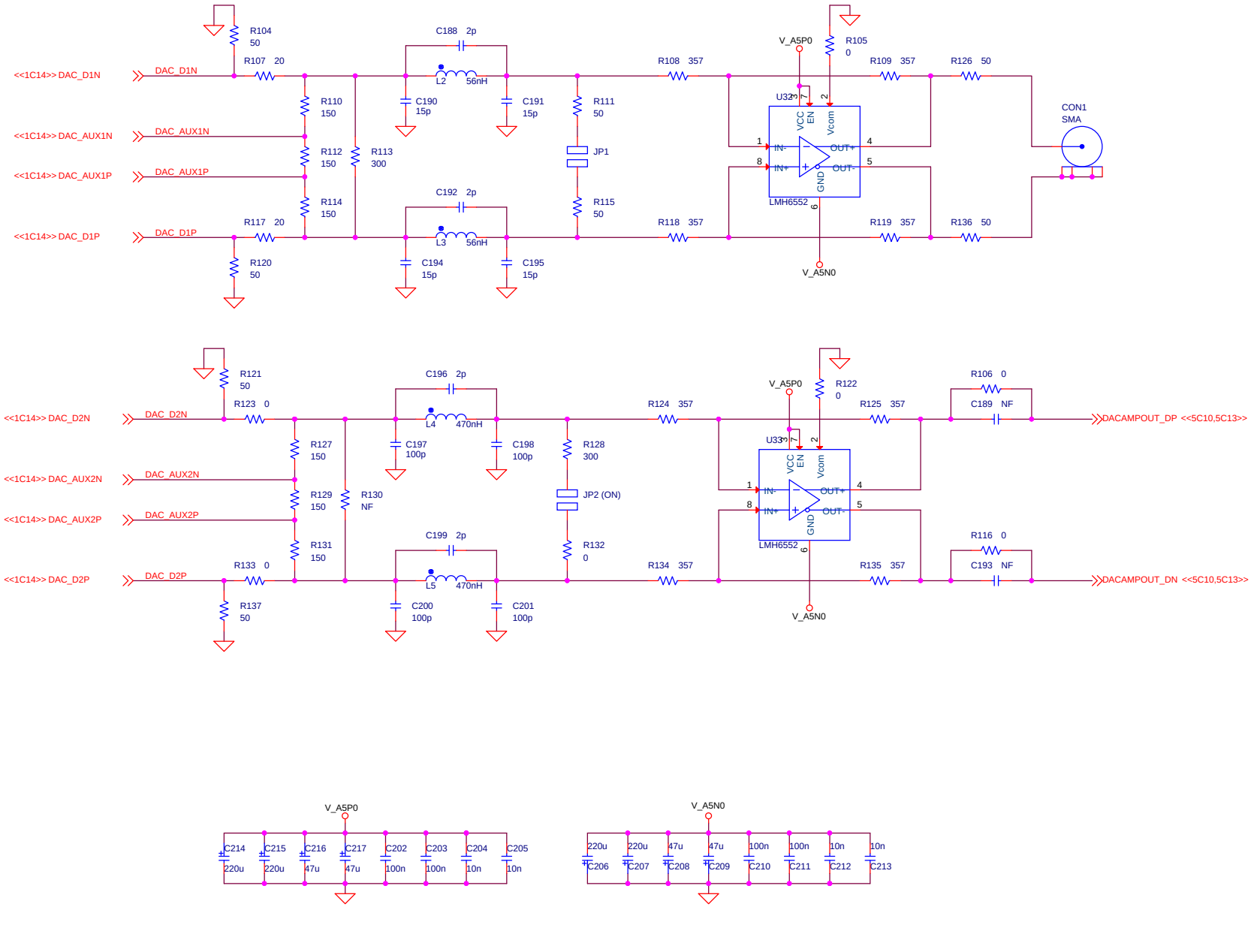

University of Strathclyde		
Title: FRONTEND - DACAMP		
Size: A3	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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Title: IO - CONNECTOR		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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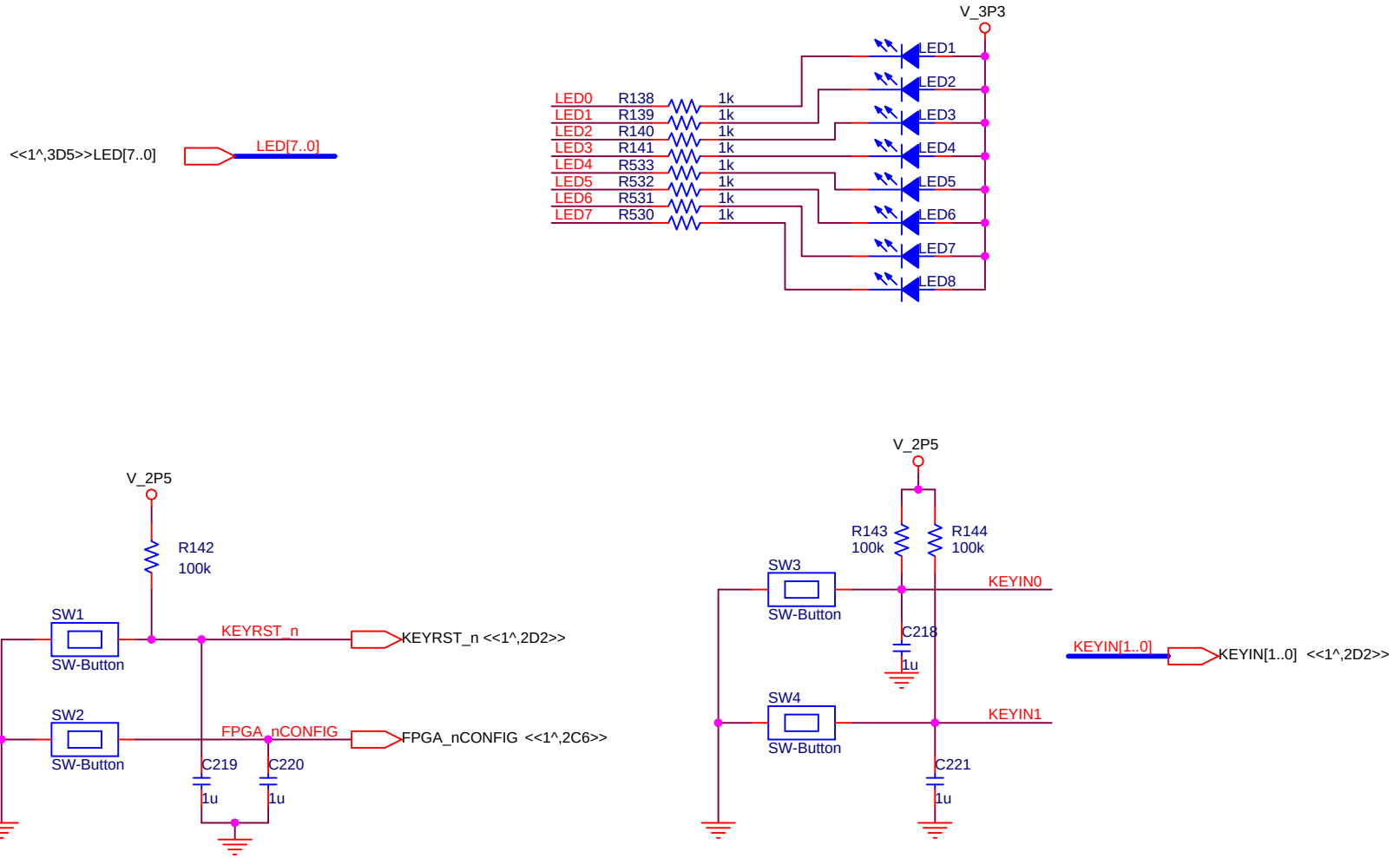

University of Strathclyde		
Title: IO - LED & BUTTON		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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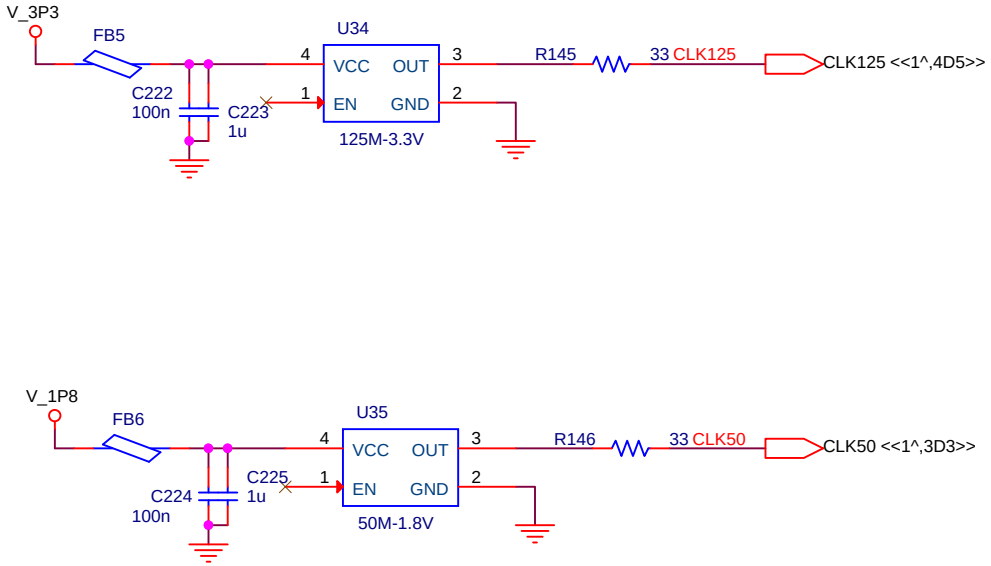
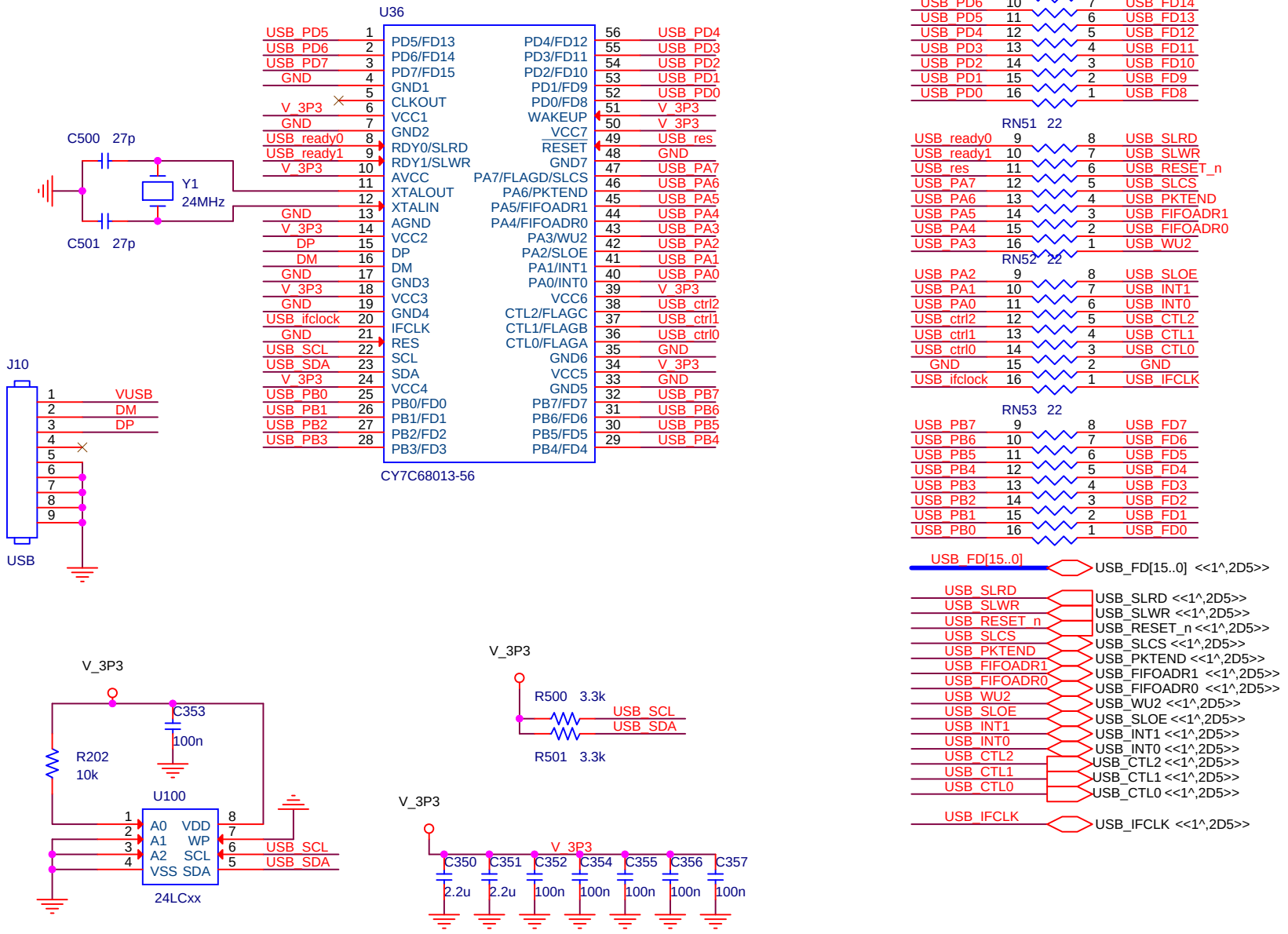


University of Strathclyde		
Title: IO - XTAL		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
Date: Sunday, November 18, 2012	Sheet 18 of 24	



University of Strathclyde	
Title	IO - USB
Size A4	Document Number Transient Fault Monitor Yuxian Tao 2011-2012 — Rev A
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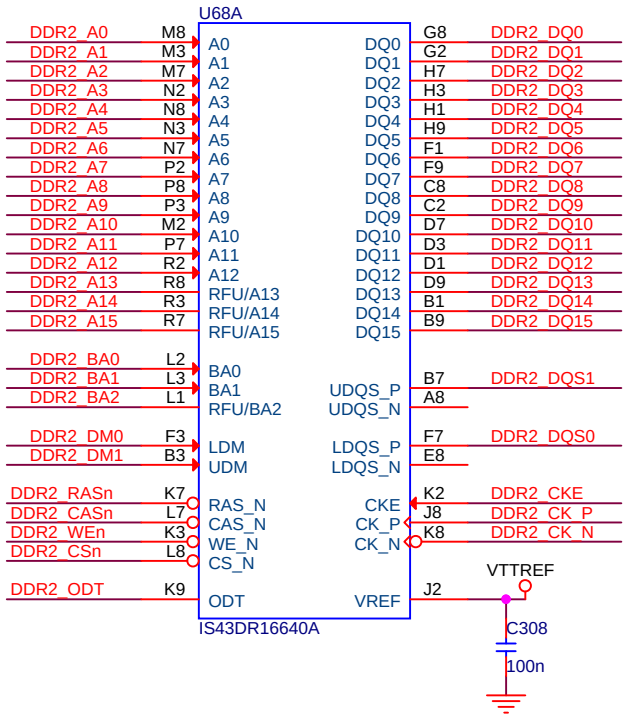

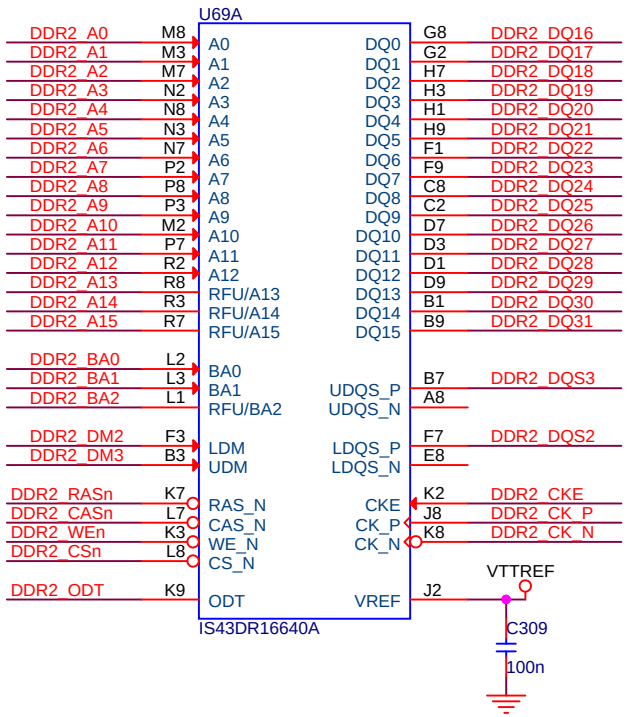

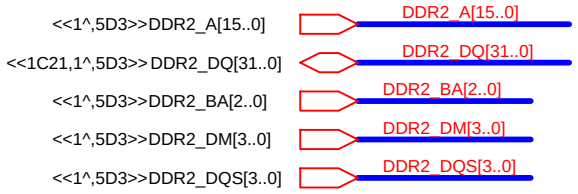

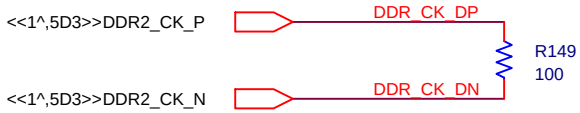

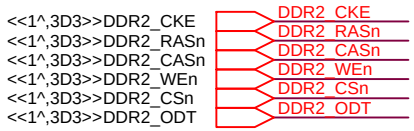

University of Strathclyde		
Title: MEMORY - DDR2		
Size: A4	Document Number: Transient Fault Monitor Yuxian Tao 2011-2012	Rev: A
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Manufacturer: YAGEO (PHYCOMP)
Order Code: 9234985
Manufacturer Part No: TC164-JR-0756RL

V_1P8

U68B

IS43DR16640A

U69B

IS43DR16640A

V_0P9

DDR2_DQ12	4	5	56	RN1
DDR2_DQ14	3	6		
DDR2_DQ9	2	7		
DDR2_DM1	1	8		
DDR2_DQ11	4	5	56	RN2
DDR2_DQ10	3	6		
DDR2_DQS1	2	7		
DDR2_DQ8	1	8		
DDR2_DQ15	4	5	56	RN3
DDR2_DQ13	3	6		
DDR2_DQ4	2	7		
DDR2_DQ6	1	8		
DDR2_DQ1	4	5	56	RN4
DDR2_DM0	3	6		
DDR2_DQ3	2	7		
DDR2_DQ2	1	8		
DDR2_DQS0	4	5	56	RN5
DDR2_DQ0	3	6		
DDR2_DQ7	2	7		
DDR2_DQ5	1	8		
DDR2_DQ20	4	5	56	RN6
DDR2_DQ22	3	6		
DDR2_DQ17	2	7		
DDR2_DM2	1	8		
DDR2_DQ19	4	5	56	RN7
DDR2_DQ18	3	6		
DDR2_DQS2	2	7		
DDR2_DQ16	1	8		
DDR2_DQ23	4	5	56	RN8
DDR2_DQ21	3	6		
DDR2_DQ28	2	7		
DDR2_DQ30	1	8		
DDR2_DQ25	4	5	56	RN9
DDR2_DM3	3	6		
DDR2_DQ27	2	7		
DDR2_DQ26	1	8		
DDR2_DQS3	4	5	56	RN10
DDR2_DQ24	3	6		
DDR2_DQ31	2	7		
DDR2_DQ29	1	8		
	4	5		
DDR2_CKE	3	6	56	RN19
DDR2_BA2	2	7		
DDR2_A10	1	8		
DDR2_A3	4	5	56	RN20
DDR2_A7	3	6		
DDR2_A12	2	7		
DDR2_RASn	1	8		
DDR2_CASn	4	5	56	RN21
DDR2_A2	3	6		
DDR2_A6	2	7		
DDR2_A11	1	8		
DDR2_A15	4	5	56	RN22
DDR2_A13	3	6		
DDR2_A8	2	7		
DDR2_A4	1	8		
DDR2_A0	4	5	56	RN23
DDR2_CSn	3	6		
DDR2_ODT	2	7		
DDR2_A14	1	8		
DDR2_A9	4	5	56	RN24
DDR2_A5	3	6		
DDR2_A1	2	7		
DDR2_BA0	1	8		
DDR2_BA1	4	5	56	RN25
DDR2_WEn	3	6		
	2	7		
	1	8		

CN1 0.1U
CN2 0.1U
CN3 0.1U
CN4 0.1U
CN5 0.1U
CN6 0.1U
CN7 0.1U
CN8 0.1U
CN9 0.1U
CN10 0.1U
CN11 0.1U
CN12 0.1U
CN13 0.1U
CN14 0.1U
CN15 0.1U
CN16 0.1U
CN17 0.1U

Manufacturer: AVX
Order Code: 1396617
Manufacturer Part No: W3A4YC104MAT2F

V_1P8

C226 C227 C228 C229 C230 C231 C232 C233 C234 C235
10n 100n 100n 100n 100n 100n 100n 100n 100n 1u

V_1P8

C250 C241 C240 C251 C256 C255 C257 C503 C504 C252
10n 100n 100n 100n 100n 100n 100n 100n 100n 1u

<<1^,5D3>> DDR2_A[15..0] — DDR2_A[15..0]
<<1^,4B20,5D3>> DDR2_DQ[31..0] — DDR2_DQ[31..0]
<<1^,5D3>> DDR2_BA[2..0] — DDR2_BA[2..0]
<<1^,5D3>> DDR2_DM[3..0] — DDR2_DM[3..0]
<<1^,5D3>> DDR2_DQS[3..0] — DDR2_DQS[3..0]

<<1^,3D3>> DDR2_CKE — DDR2_CKE
<<1^,3D3>> DDR2_RASn — DDR2_RASn
<<1^,3D3>> DDR2_CASn — DDR2_CASn
<<1^,3D3>> DDR2_WEn — DDR2_WEn
<<1^,3D3>> DDR2_CSn — DDR2_CSn
<<1^,3D3>> DDR2_ODT — DDR2_ODT

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Title: MEMORY - DDR2 POWER AND TERMS

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FLASH_SRAM_DQ[31..0] FLASH_SRAM_DQ[31..0] <<1^,2B23,5D2>>

FLASH_SRAM_A[24..1] FLASH_SRAM_A[24..1] <<1^,3D2>>

IO Requirement:
3 individual 2.5V
24 shared ADDs 2.5V

V_2P5

FLASH_CE_n R161 4.7k

FLASH_RESET_n R162 4.7k

FLASH_BUSY_n R163 4.7k

U38

V_3P3 43 VCC

V_2P5 29 VIO

FLASH_SRAM_A1	31	A0	
FLASH_SRAM_A2	26	A1	
FLASH_SRAM_A3	25	A2	
FLASH_SRAM_A4	24	A3	
FLASH_SRAM_A5	23	A4	
FLASH_SRAM_A6	22	A5	
FLASH_SRAM_A7	21	A6	
FLASH_SRAM_A8	20	A7	
FLASH_SRAM_A9	10	A8	
FLASH_SRAM_A10	9	A9	
FLASH_SRAM_A11	8	A10	
FLASH_SRAM_A12	7	A11	
FLASH_SRAM_A13	6	A12	
FLASH_SRAM_A14	5	A13	
FLASH_SRAM_A15	4	A14	
FLASH_SRAM_A16	3	A15	
FLASH_SRAM_A17	54	A16	
FLASH_SRAM_A18	19	A17	
FLASH_SRAM_A19	18	A18	
FLASH_SRAM_A20	11	A19	
FLASH_SRAM_A21	12	A20	
FLASH_SRAM_A22	15	A21	
FLASH_SRAM_A23	2	A22	
FLASH_SRAM_A24	1	A23	

S29GL256P10TFI010

		BYTE	53
		DQ0	35 FLASH_SRAM_DQ0
		DQ1	37 FLASH_SRAM_DQ1
		DQ2	39 FLASH_SRAM_DQ2
		DQ3	41 FLASH_SRAM_DQ3
		DQ4	44 FLASH_SRAM_DQ4
		DQ5	46 FLASH_SRAM_DQ5
		DQ6	48 FLASH_SRAM_DQ6
		DQ7	50 FLASH_SRAM_DQ7
		DQ8	36 FLASH_SRAM_DQ8
		DQ9	38 FLASH_SRAM_DQ9
		DQ10	40 FLASH_SRAM_DQ10
		DQ11	42 FLASH_SRAM_DQ11
		DQ12	45 FLASH_SRAM_DQ12
		DQ13	47 FLASH_SRAM_DQ13
		DQ14	49 FLASH_SRAM_DQ14
		DQ15	51 FLASH_SRAM_DQ15

<<1^,2D2>>FLASH_CE_n
<<1^,5D2>>FLASH_SRAM_OE_n
<<1^,5D2>>FLASH_SRAM_WE_n
<<1^,2D2>>FLASH_RESET_n
<<1^,3D2>>FLASH_BUSY_n

FLASH_CE_n	32	CE	
FLASH_SRAM_OE_n	34	OE	
FLASH_SRAM_WE_n	13	WE	
FLASH_RESET_n	14	RESET	
	16	WP	
FLASH_BUSY_n	17	BUSY	

NC1	27	
NC2	28	
NC3	30	
NC4	55	
NC5	56	

VSS1 33 VSS2 52

V_3P3 C253 100n C254 1u

V_2P5 C258 100n C259 1u

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Title: MEMORY - FLASH			
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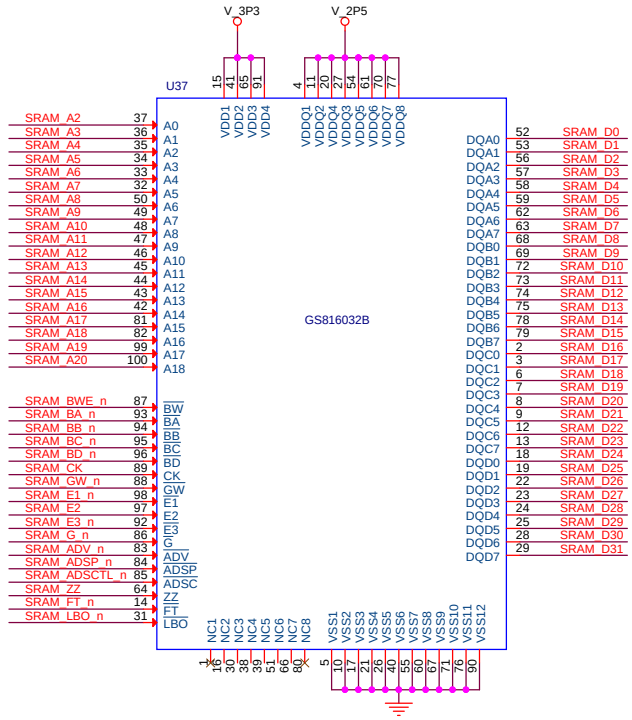

Manufacturer: YAGEO (PHYCOMP)
Order Code: 1377041
Manufacturer Part No: YC248-JR-0722RL

RN11 22
SRAM_A15 SRAM_A16 SRAM_A2 SRAM_A3 SRAM_A4 SRAM_A5 SRAM_A6 SRAM_A7
FLASH_SRAM_A15 FLASH_SRAM_A16 FLASH_SRAM_A2 FLASH_SRAM_A3 FLASH_SRAM_A4 FLASH_SRAM_A5 FLASH_SRAM_A6 FLASH_SRAM_A7

RN13 22
SRAM_A8 SRAM_A9 SRAM_A10 SRAM_A11 SRAM_A12 SRAM_A13 SRAM_A14
FLASH_SRAM_A8 FLASH_SRAM_A9 FLASH_SRAM_A10 FLASH_SRAM_A11 FLASH_SRAM_A12 FLASH_SRAM_A13 FLASH_SRAM_A14

RN15 22
SRAM_A20 SRAM_A19 SRAM_E1_n SRAM_BD_n SRAM_BC_n SRAM_BB_n SRAM_BA_n
FLASH_SRAM_A20 FLASH_SRAM_A19 SRAM_CE_n SRAM_BE_n3 SRAM_BE_n2 SRAM_BE_n1 SRAM_BE_n0
SRAM_CE_n <<1^,5D2>>

RN17 22
SRAM_CK SRAM_BWE_n SRAM_G_n SRAM_ADSCTL_n SRAM_A18 SRAM_A17
SRAM_CLK FLASH_SRAM_WE_n FLASH_SRAM_OE_n SRAM_ADSC_n FLASH_SRAM_A18 FLASH_SRAM_A17
SRAM_CLK <<1^,5D2>>
FLASH_SRAM_WE_n <<1^,5D2>>
FLASH_SRAM_OE_n <<1^,5D2>>
SRAM_ADSC_n <<1^,5D2>>

RN12 22
SRAM_D8 SRAM_D9 SRAM_D10 SRAM_D11 SRAM_D12 SRAM_D13 SRAM_D14 SRAM_D15
FLASH_SRAM_DQ8 FLASH_SRAM_DQ9 FLASH_SRAM_DQ10 FLASH_SRAM_DQ11 FLASH_SRAM_DQ12 FLASH_SRAM_DQ13 FLASH_SRAM_DQ14 FLASH_SRAM_DQ15

RN14 22
SRAM_D16 SRAM_D17 SRAM_D18 SRAM_D19 SRAM_D20 SRAM_D21 SRAM_D22 SRAM_D23
FLASH_SRAM_DQ16 FLASH_SRAM_DQ17 FLASH_SRAM_DQ18 FLASH_SRAM_DQ19 FLASH_SRAM_DQ20 FLASH_SRAM_DQ21 FLASH_SRAM_DQ22 FLASH_SRAM_DQ23

RN16 22
SRAM_D24 SRAM_D25 SRAM_D26 SRAM_D27 SRAM_D28 SRAM_D29 SRAM_D30 SRAM_D31
FLASH_SRAM_DQ24 FLASH_SRAM_DQ25 FLASH_SRAM_DQ26 FLASH_SRAM_DQ27 FLASH_SRAM_DQ28 FLASH_SRAM_DQ29 FLASH_SRAM_DQ30 FLASH_SRAM_DQ31

RN18 22

4.7k PD on ADSCTL_n

V_2P5
SRAM_CE_n SRAM_ADV_n SRAM_ADSP_n SRAM_GW_n SRAM_E2 SRAM_FT_n SRAM_E3_n SRAM_LBO_n SRAM_ZZ
FLASH_SRAM_OE_n
R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 4.7k

FLASH_SRAM_A[24..1] FLASH_SRAM_A[24..1] <<1^,3D2>>
SRAM_BE_n[3..0] SRAM_BE_n[3..0] <<1^,5D2>>
FLASH_SRAM_DQ[31..0] FLASH_SRAM_DQ[31..0] <<1^,4C22,5D2>>

V_3P3
C236 C237 C238 C239 10n 100n 100n 100n

V_2P5
C242 C243 C244 C245 C246 C247 C248 C249 100n

IO Requirement:
3 individual 2.5V
2 (OE/WE) shared 2.5V
32 shared DQs 2.5V

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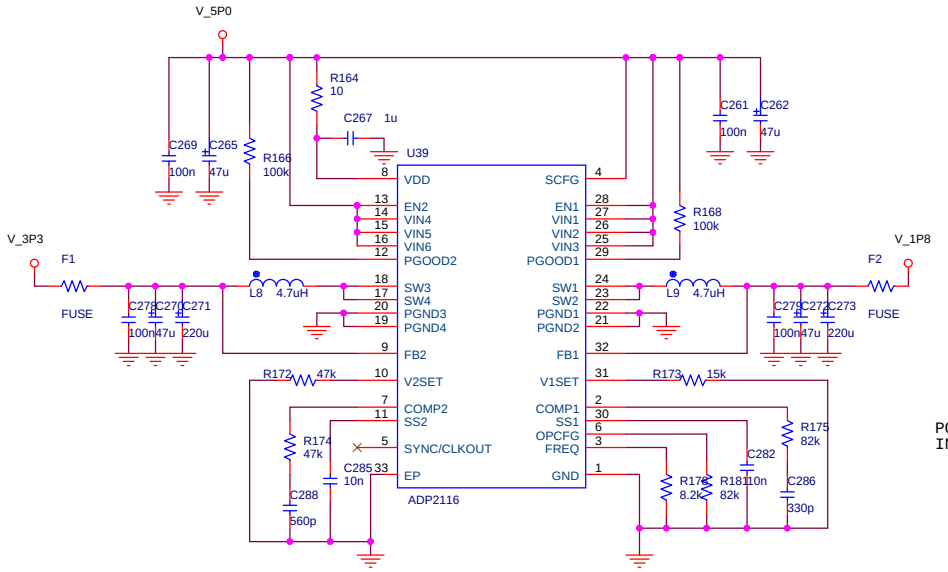
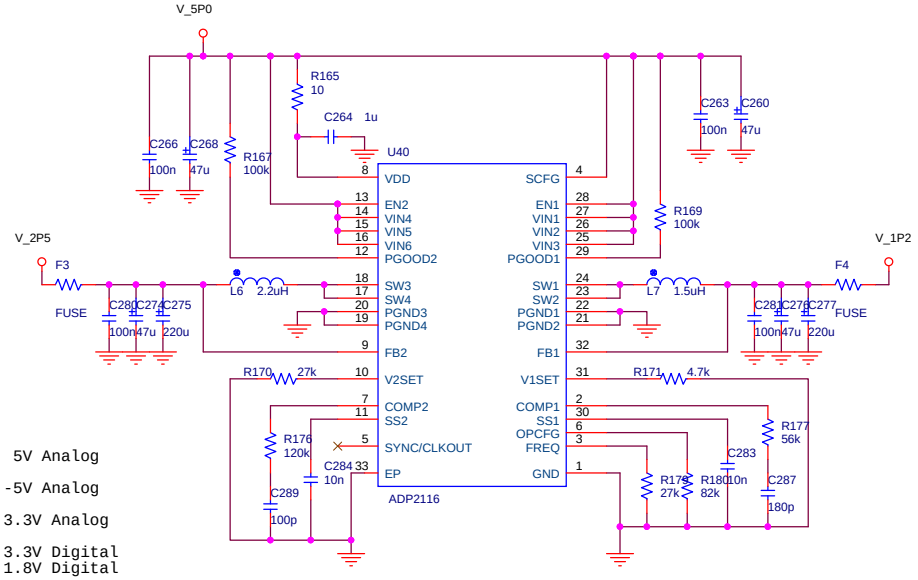
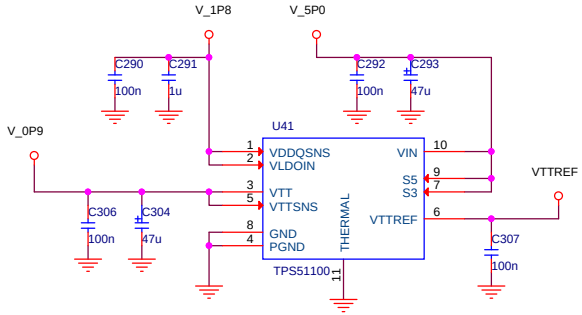
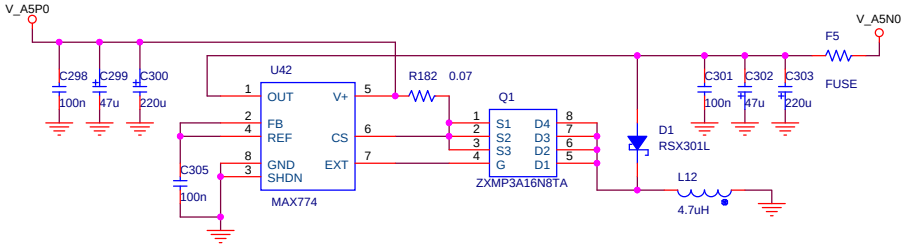
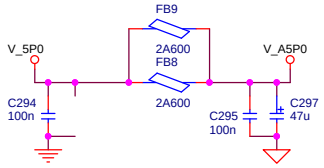


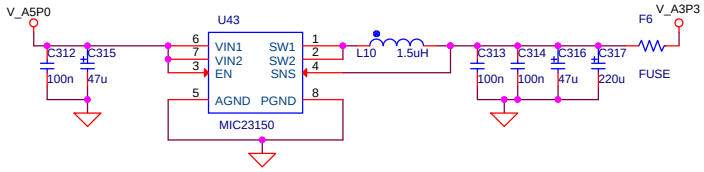


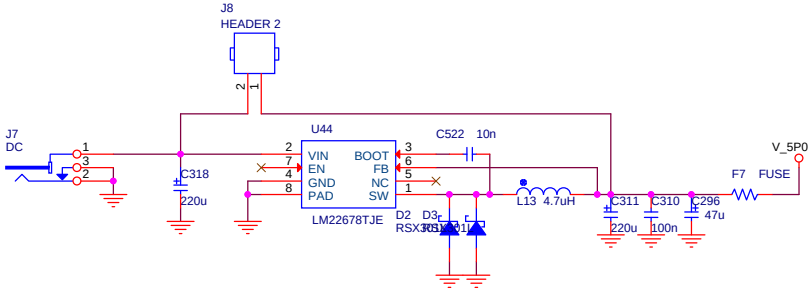
POWER MAP:
INPUT -> 5V +--> 5V Analog
|
+--> -5V Analog
|
+--> 3.3V Analog
|
+--> 3.3V Digital
+--> 1.8V Digital
|
+--> 2.5V Digital
+--> 1.2V Digital
|
+--> 1.8V DDR Term
+--> 0.9V DDR Term
+--> 0.9V DDR REF

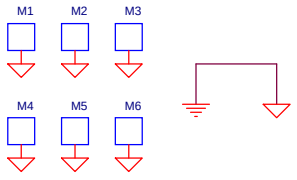












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Title: POWER - POWER SUPPLY		
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