# High-efficiency voltage source converters with silicon super-junction MOSFETs

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Signed:

Date:

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# Abstract

High-efficiency power converters have the benefits of minimising energy consumption, reducing costs, and realising high power densities. The silicon super-junction (SJ) MOSFET is an attractive device for high-efficiency applications. However, its highly non-linear output capacitance and the reverse recovery properties of its intrinsic diode must be addressed when used in voltage source converters (VSCs).

The research in this thesis aims at addressing these two problems and realising high efficiency. Initially, state-of-art techniques in the literature are reviewed. In order to develop a solution with simple hardware, no major auxiliary magnetic components, and no onerous timing requirements, a dual-mode switching technique is proposed. The technique is demonstrated using a SJ MOSFET based bridge-leg circuit. The hardware performance is then experimentally investigated with different power semiconductor device permutations. The transition conditions between the two switching modes do not have to be tightly set in order to maintain a high efficiency. The dual-mode switching technique is then further investigated with a current transformer (CT) arrangement embedded in the MOSFET's gate driver circuit in order to control the profile of the MOSFET's incoming drain current at turn-on. The dual-mode switching technique, with or without a CT scheme, is shown to achieve high efficiency with minimal additional hardware.

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# Abbreviations

| | |
|---|---|
| **3-D** | Three-Dimensional |
| **AC** | Alternating Current |
| **ARCP** | Auxiliary Resonant Commutated Pole |
| **BCM** | Boundary Conduction Mode |
| **BJT** | Bipolar Junction Transistor |
| **CCM** | Continuous Conduction Mode |
| **CPU** | Central Processing Unit |
| **CSC** | Current Source Converter |
| **CT** | Current Transformer |
| **DC** | Direct Current |
| **DCI** | Drain Current Injection |
| **DCM** | Discontinuous Conduction Mode |
| **DSP** | Digital Signal Processing |
| **EMI** | Electromagnetic Interference |
| **FFT** | Fast Fourier Transformer |
| **FOM** | Figure of Merit |
| **FPGA** | Field-Programmable Gate Array |
| **GaN** | Gallium Nitride |
| **GTO** | Gate Turn-off Thyristor |
| **HEMT** | High-Electron-Mobility Transistor |
| **HEXFET** | Hexagonal Field-Effect Transistor |
| **IC** | Integrated Circuit |
| **IGBT** | Insulated-Gate Bipolar Transistor |
| **JFET** | Junction-Gate Field-Effect Transistor |
| **MCU** | Microcontroller Unit |
| **MOSFET** | Metal–Oxide–Semiconductor Field-Effect Transistor |
| **NPC** | Neutral-Point Clamped |
| **NPT-IGBT** | Non-Punch Through IGBT |

| | |
|---|---|
| **NTC** | Negative Temperature Coefficient |
| **PAD** | Pulse Active Desaturation |
| **PCB** | Printed Circuit Board |
| **PF** | Power Factor |
| **PFC** | Power Factor Correction |
| **PTC** | Positive Temperature Coefficient |
| **PT-IGBT** | Punch Through IGBT |
| **PWM** | Pulse-Width Modulation |
| **RMS** | Root Mean Square |
| **SBD** | Schottky Barrier Diode |
| **SCE** | Source Charge Extraction |
| **SCM** | Synchronous Conduction Mode |
| **Si** | Silicon |
| **SiC** | Silicon Carbide |
| **$SiO_2$** | Silicon Dioxide |
| **SJ** | Super-Junction |
| **SMPS** | Switching-Mode Power Supply |
| **SoC** | System on Chip |
| **SOIC** | Small Outline Integrated Circuit |
| **SPWM** | Sinusoidal Pulse Width Modulation |
| **SSR** | Slow-Switching Ratio |
| **TCM** | Triangle Current Mode |
| **THD** | Total Harmonic Distortion |
| **TR** | Transistor |
| **UK** | United Kingdom |
| **VDMOS** | Vertical Diffused MOSFET |
| **VSC** | Voltage Source Converter |
| **VVMOS** | Vertical V-groove MOSFET |
| **WBG** | Wide Band-Gap |
| **ZVS/ZCS** | Zero Voltage/Current Switching |
| **ZSC** | Z-Source Converter |

# Symbols

| Symbol | Description | Units |
|---|---|---|
| $\mu_0$ | Permeability of free space, = $4\pi\times10^{-7}$ | Henries/metre (H/m) |
| $\mu_r$ | Relative permeability | [no units] |
| $A$ | Area | Square metres ($m^2$) |
| $C$ | Capacitance | Farads (F) |
| $C_{iss}$ | Input capacitance | Farads (F) |
| $C_{oss}$ | Output capacitance | Farads (F) |
| $C_{rss}$ | Reverse capacitance | Farads (F) |
| $D_{ext}$ | External diode | [no units] |
| $D_s$ | Series diode | [no units] |
| $D_{temp}$ | Temperature rise | Degrees Centigrade (°C) |
| $e$ | Constant electron charge, = $1.602\times10^{-19}$ | Coulombs (C) |
| $E_{on}$ | Turn-on energy | Joules (J) |
| $E_{oss}$ | Co-energy | Joules (J) |
| $f$ | Frequency | Hertz (Hz) |
| $I$ | Current | Amperes (A) |
| $L$ | Inductance | Henries (H) |
| $l$ | Length | Metres (m) |
| $L_m$ | Magnetising inductance | Henries (H) |
| $m$ | Modulation index | [no units] |
| $N$ | Turns ratio | [no units] |
| $P$ | Power | Watts (W) |
| $P_d$ | Power dissipation | Watts (W) |
| $Q$ | Charge | Coulombs (C) |
| $Q_{oss}$ | Output capacitance charge | Coulombs (C) |
| $Q_{rr}$ | Reverse recovery charge | Coulombs (C) |
| $R$ | Electrical resistance | Ohms (Ω) |
| $R_{DS(on)}$ | On-state resistance | Ohms (Ω) |

| | | |
|---|---|---|
| $R_{DS(on)} \times A$ | Specific on-state resistance | $m\Omega \times cm^2$ |
| $R_{gate}$ | Gate resistance | Ohms ($\Omega$) |
| $R_{\theta hsa}$ | Thermal resistance | Ohms ($\Omega$) |
| $T$ | Temperature | Degrees Centigrade (°C) |
| $t$ | Time | Seconds (S) |
| $T_j$ | Junction temperature | Degrees Centigrade (°C) |
| $V$ | Voltage | Volts (V) |
| $V_{AV}$ | Avalanche voltage | Volts (V) |
| $V_{BR}$ | Breakdown voltage | Volts (V) |
| $V_{CE}$ | Collector-emitter voltage | Volts (V) |
| $V_{DS}$ | Drain-source voltage | Volts (V) |
| $V_{GE}$ | Gate-emitter voltage | Volts (V) |
| $V_{GS}$ | Gate-source voltage | Volts (V) |
| $V_{MP}$ | Miller plateau voltage | Volts (V) |
| $V_{th}$ | Threshold voltage | Volts (V) |
| $\delta$ | Duty cycle | [no units] |
| $\eta$ | Efficiency | [no units] |
| $\sigma$ | Conductivity | Siemens/metre (S/m) |

# Publications

- Z. Feng, N. McNeill, and B. Williams, “A high-efficiency super-junction MOSFET based inverter-leg configuration using a dual-mode switching technique,” in *Proc. IEEE 34th Annu Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, Mar. 2019, pp. 2467-2474.

- Z. Feng, N. McNeill, and B. Williams, “Control of incoming drain currents drawn by super-junction MOSFETs in voltage source bridge-legs,” in *Proc. 9th Int. Conf. Renewable Energy Res. Appl.*, Glasgow, UK, Sep. 2020, pp. 93-100.

- A. Elwakeel, Z. Feng, N. McNeill, M. Zhang, B. Williams, and W. Yuan, “Study of power devices for use in phase-leg at cryogenic temperature,” *IEEE Trans. Appl. Supercond.*, vol. 31, no. 5, pp. 1–5, Aug. 2021.

# Chapter 1

# Introduction

## 1.1. Power electronics

On 27 June 2019, the UK government passed the net zero emissions law which commits to a legally binding target of net zero emissions by 2050 [1]. In order to achieve this ambition, the recognition of power electronics is inevitable. Power electronics has gone through rapid technological advancement during the last decades, and its applications are fast expanding in industrial, commercial, residential, military and utility environments [2].

In power electronics technology, high-efficiency power electronic converters have the benefits of minimising energy dissipation, and realising high gravimetric and volumetric power densities. Costs are reduced because of the lower energy wastage and the reduced cooling requirements. The advantages of the high-efficiency converters make them important in protecting the environment. The critical applications of high-efficiency power electronics converters include:

- Industrial machine drives
- Renewable energy systems: grid-tie inverters
- Transportation: automotive, aerospace
- Grid schemes, DC transformers

The silicon super-junction (SJ) MOSFET is an attractive device for high-efficiency applications. However, its highly non-linear output capacitance and the reverse recovery

properties of its intrinsic diode must be addressed when used in voltage source converters (VSCs). In this thesis, techniques are presented and validated for tackling these challenges.

## 1.2. Organisation of the thesis

The thesis is organised as follows.

### 1.2.1. Chapter 2

A review of the key silicon and wide band-gap (WBG) devices is given. Then, several recently emerged WBG devices will be discussed under their different types of materials, namely Silicon carbide (SiC) and Gallium nitride (GaN). The structure and operating principles of the silicon SJ MOSFET will be introduced. The advantages of the SJ MOSFET will be discussed against the background of the other candidate devices.

### 1.2.2. Chapter 3

The challenges encountered when using the SJ MOSFET in VSCs will be discussed. Then literature on using the SJ MOSFET in VSCs is reviewed, which covers the prior art on how the challenges presented by the intrinsic diode and output capacitance have been addressed. Alternative topologies to the VSC where the problems presented by the intrinsic diode and output capacitance of the SJ MOSFET are not problematic will be discussed. The reasons for the predominance of the VSC despite the benefits of these other topologies are discussed. At the end of the chapter, the research area which fills gaps left by previous techniques is identified, and key objectives are outlined.

### 1.2.3. Chapter 4

A dual-mode switching technique operating in conjunction with SJ MOSFET intrinsic diode deactivation circuitry is proposed. The technique is demonstrated in an 800-W inverter-leg configuration operating from a 400-V DC voltage and switching at 20 kHz. Intended applications include machine drives. No forced cooling is needed, and the full-load efficiency is measured at 98.7 %, against a measured benchmark efficiency of 97.5 % when using conventional fast-switching silicon IGBTs and fast recovery diodes.

### 1.2.4. Chapter 5

In Chapter 4, the dual-mode switching technique addresses the detrimental influence of the SJ MOSFET's output capacitance and functions in conjunction with intrinsic diode deactivation circuitry. The intrinsic diode deactivation circuitry uses two ancillary power devices connected around each SJ MOSFET. Power device selection is addressed in this chapter and practical efficiency measurements are recorded when using different device permutations with the dual-mode switching technique described in Chapter 4. All the device permutations are designed for a 1-kW inverter-leg operating at 420-V DC and switching at a series of frequencies from 15 kHz, 20 kHz, 25 kHz, 30 kHz up to 35 kHz. The full-load efficiency is evaluated for each scenario.

### 1.2.5. Chapter 6

MOSFET switching speeds are normally controlled by simply setting the device's external gate resistance to an appropriate value. This tends to yield a triangular incoming drain current profile. The peak current reached can be limited by simply using a large resistance in series with the gate of MOSFET, as in the slow-switching mode discussed in Chapter 4. However, this increases the power dissipation in the MOSFET. Furthermore, the turn-on propagation delay time is increased.

As an alternative, a gate driver circuit is developed that yields an approximately rectangular incoming drain current profile. Benefits include a lower peak incoming drain current and lower gate propagation delays for a given power dissipation in the device. SJ MOSFETs with proposed gate driver and conventional gate driver are used in 400-V bridge-leg and switched at 20 kHz. The triangular and rectangular incoming drain current profiles are compared when using different gate resistance values.

### 1.2.6. Chapter 7

Conclusions are given and areas are identified for further research.

### 1.2.7. Appendix A

Experimental data, including thermal recordings and exemplifying waveforms, are included in Appendix A.

### 1.2.8. Appendix B

Gate driver circuits were designed as part of the research project. Design and test details of a gate driver circuit with optical isolation, and a dual-mode gate driver circuit are included in Appendix B.

### 1.2.9. Appendix C

The microcontroller coding used in the experiments is included in Appendix C.

# Chapter 2

# Overview of power electronic devices

## 2.1. Introduction

There are three elements in power electronics technology: power electronics devices, power electronics circuits and power electronics system control, among which power electronics devices have a fundamental importance. Understanding the characteristics of the devices helps make an informed device selection in circuit applications. Correspondingly, system control strategies will be better designed with good knowledge of devices.

Since the establishment of power electronics technology, power electronics devices have evolved and changed. Nowadays, there are enormous types and numbers of power electronics devices being manufactured every year. Some global-leading manufacturers include Infineon, ABB, Dynex Semiconductor, NXP, On Semiconductor, IXYS Corporation, STMicroelectronics, Cree Inc., Rohm Semiconductor, Toshiba, Fuji Electric, Mitsubishi Electric.

In general, power electronic devices can be categorised into three families according to their degree of controllability: diodes, thyristors and transistors. Diodes are uncontrollable devices, whose turn-on and -off cannot be controlled and only depend on external circuit conditions. Thyristors are partially controllable devices, which means only their turn-on can be controlled by desired signals while turn-off cannot (an exception is the gate turn-

off thyristor, or GTO). Transistors are fully controllable devices, and both turn-on and turn-off can be controlled by desired signals. The transistors become the most significant power electronics devices due to their control flexibility. Among all, two types of transistors are extensively used in power electronics circuits, namely metal-oxide-semiconductor field-effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT) [3]. Both will be introduced in this chapter.

Wide band-gap (WBG) devices are attracting much interest due to their advantageous intrinsic qualities. The commercially successful WBG devices and their comparison with conventional silicon (Si) devices will be included in this chapter.

Super-junction (SJ) MOSFET, the object of the thesis, is a variant of vertical MOSFET. There will be a focus on the SJ MOSFET at the last of this chapter, where its structure and characteristics are discussed.

## 2.2. Silicon power MOSFET

Early power MOSFETs had a planar structure which led to a high on-state resistance $R_{DS(on)}$ and low utilisation of the manufacturing material – monocrystalline silicon. After adopting the vertical structure in the 1970s, power MOSFETs improved significantly in voltage breakdown characteristics and current abilities. Then their potentials for power electronic applications have been available since the early 1980s [4].

As in Figure 2.1, a power MOSFET has three terminals: gate (G), source (S) and drain (D). Between terminals, there is vertically oriented four-layer structure of alternating p-type and n-type doping for a single cell of the many paralleled cells of a complete device. The density of cells in one complete device can vary from 200,000 to 1,000,000 per $cm^2$, depending on the voltage rating of the device [3]. For each one cell, according to the fabrication sequence, it can be categorised as VDMOS (vertical diffused MOSFET) and VVMOS (vertical V-groove MOSFET). According to the methods of conductivity control, it can be categorised as an enhancement-mode or depletion-mode MOSFET. According to the types of channel carriers, it can be categorised as p-channel MOSFET with the carrier of holes, or n-channel MOSFET with the carrier of electrons. Figure 2.2 shows the

circuit symbols for an enhancement n-channel, an enhancement p-channel, a depletion n-channel, and a depletion p-channel MOSFET. In these circuit symbols, the direction of the arrow indicates the direction of the pn junction between body region and channel. For example, the body region of an n-channel MOSFET is p-type, and the channel is n-type, so the arrow is pointing into the channel from the body as in Figure 2.2 (a), (c). Conversely, the arrow in the p-channel MOSFET is pointing outwards from the channel to the body as in Figure 2.2 (b), (d). In all four circuit symbols, the body region and the source terminal are connected because of the body-source short as illustrated in Figure 2.1. The dashed-line channel indicates the channel is to be enhanced, which stands for an enhancement-mode MOSFET as in Figure 2.2 (a), (b). The full-line channel indicates the channel is to be depleted, which stands for a depletion-mode MOSFET as in Figure 2.2 (c), (d).

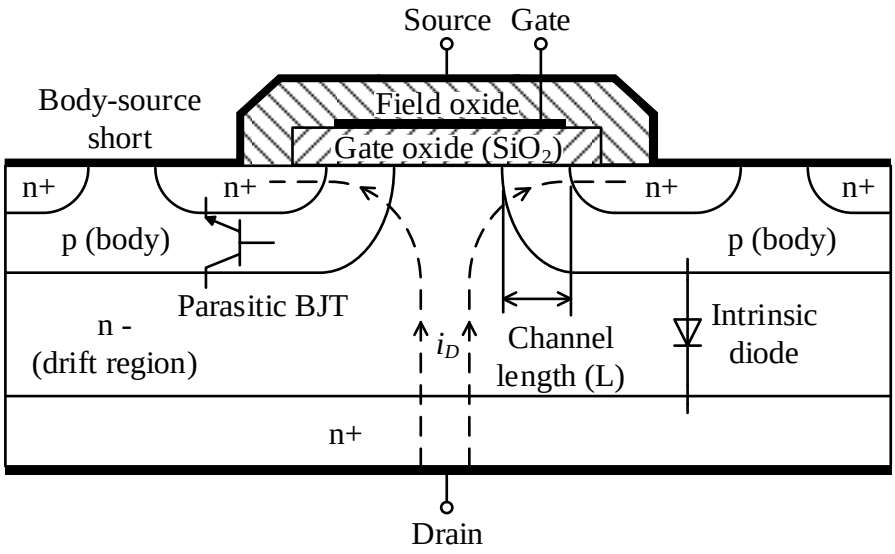



*Figure 2.1 Vertical cross-section of an n-channel MOSFET adapted from* [4].

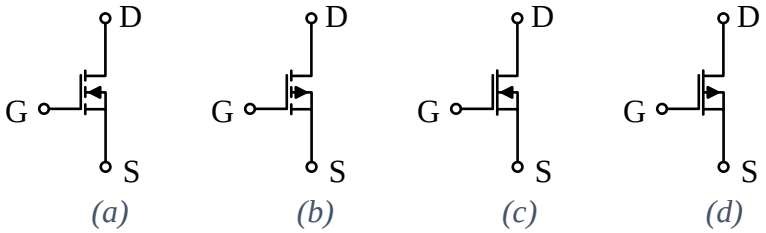



*Figure 2.2 Circuit symbols for (a) enhancement n-channel, (b) enhancement p-channel, (c) depletion n-channel, (d) depletion p-channel MOSFET.*

N-channel MOSFETs are more widely used than p-channel, for they have the benefits of smaller $R_{DS(on)}$ when under same power ratings. Because from the perspective of physical materials, the conductivity $\sigma$ of doped silicon equals

$$\sigma = \frac{1}{\rho} = en\mu_n + ep\mu_p \tag{2.1}$$

where $\rho$ is the resistivity of doped silicon, constant electron charge $e$ = $1.602\times10^{-19}$ C, $n$ and $p$ are the concentration of carrier electrons and holes, $\mu_n$ and $\mu_p$ are the mobility of the carrier electrons and holes which stand for the degree of difficulty for carriers to drift in the electric field. In actuality, the movement of carrier holes is the consequence of the movement of covalence electrons, which is more difficult than the movement of free electrons. This causes $\mu_n$ to be bigger than $\mu_p$. So according to (2.1), the conductivity of n-channel is better than p-channel. Furthermore, it also explains that the common-emitter current gain $\beta$ of NPN BJT (bipolar junction transistor) is bigger than PNP BJT. Figure 2.3 shows the subcategories of commercialised MOSFETs manufactured by Infineon. In Figure 2.3, the n-channel MOSFETs detail in more categories due to their broad industrial applications. P-channel MOSFETs, on the contrary, have much less number in commercial manufacture.


*Figure 2.3 Subcategories of commercialised MOSFETs from Infineon* [5].

### 2.2.1. Structure

As shown in Figure 2.1, the gate region of the MOSFET is composed of the gate metallisation, the silicon dioxide ($SiO_2$) layer underneath the gate conductor which is termed as gate oxide, and the silicon substrate beneath the gate oxide. The gate oxide provides a very well isolation between gate and source.

Take an enhancement n-channel MOSFET as an example. After applying a positive voltage $V_{GS}$ between gate and source, the major carrier holes (in p body region, carrying positive electricity) are pushed away from the interface of the gate oxide and the silicon substrate under the function of the electric field, thus creating a layer which is depleting holes, hence the name depletion layer. The depletion layer is enhanced as further increasing $V_{GS}$, and the electric field begins to attract free electrons (minority carrier in p body region, carrying negative electricity) as well as push away holes. A new layer then occurs when the density of the free electrons is exceeding than the density of holes. This new layer has the proprieties of n-type rather than p-type, so it is termed as inversion layer. When $V_{GS}$ reaches the threshold voltage $V_{GS(th)}$, the enhanced inversion layer starts to provide a current path between the $n^+$ source region and the $n^-$ drift region. Currently the MOSFET still in the pinch-off state. This path eventually forms a channel to allow the current to flow freely between drain and source. The MOSFET is entirely on when the channel is formed. The length of the channel $L$ is illustrated in Figure 2.1.

Because of the $n^+pn^-n^+$ four-layer structure of the n-channel MOSFET, there unavoidably form a parasitic NPN BJT between drain and source. In order to avoid the turn-on of the parasitic BJT, the p body region, which is the base of the BJT, is shorted to the source terminal, which is the emitter of the BJT, by overlapping the source metallisation onto the p body region.

Even with the body-source short, there is also a body diode, or called intrinsic diode, presenting a reverse current path in MOSFET when no gate voltage is added ($V_{DS} < 0$, $V_{GS} = 0$). The anode of the intrinsic diode is connected to p body region and the cathode is connected to $n^-$ drift region. From the perspective of external circuit characteristics, the

intrinsic diode is anti-parallel with the MOSFET as in Figure 2.4. However, the reverse recovery of the intrinsic diode is problematic, especially when used in voltage source converters (VSCs).

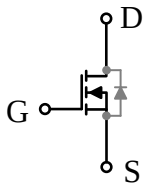



*Figure 2.4 An enhancement n-channel MOSFET with its intrinsic diode.*

In Figure 2.1, there is also an overlap of the gate metallisation across the $n^-$ drift region where it protrudes to the silicon substrate between the p body regions. This overlapping allows the gate-source bias to enhance the conductivity of the $n^-$ drift region by creating an accumulation layer where additional free electrons are attracted to the interface between the $n^-$ drift region and the gate oxide [4].

As mentioned in Section 2.2, a complete MOSFET is composed of many paralleled cells. A good layout of these cells will reduce the carriers' route length and improve conductivity. The hexagonal field effect transistor (HEXFET) with a hexagonal cellular structure is an example of this. HEXFET was introduced by International Rectifier as a trademark since 1979. The HEXFET cell density has been optimised for each voltage range to provide lower $R_{DS(on)}$ per unit area [6]. As shown in Figure 2.5, the cellular structure is built by hexagonal FET with adjacent cell sharing the gate contact and oxide layer above the "neck" area which separates the cells. With the positive gate bias, the "transistor current" flows towards the "neck" between two adjacent channels. There it splits and flows laterally to the corresponding sources [7]. This structure design makes the current path in p body region as short and wide as possible to remain a low resistance. Except for hexagonal cellular structure, others like square cellular structure has also been designed.

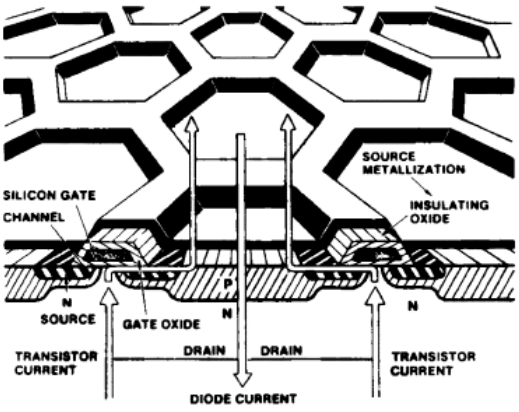



*Figure 2.5 Cellular structure of HEXFET* [8].

### 2.2.2. Static output characteristics

Figure 2.6 shows the static output characteristics of a power MOSFET. The curves lie in the first and third quadrants and show the drain current $i_D$ as a function of drain-source voltage $V_{DS}$ and gate-source voltage $V_{GS}$. There are six regions of MOSFET's static state, which indicated by curves and dash-dotted lines in Figure 2.6.

In the first quadrant, both $i_D$ and $V_{DS}$ are positive. As $V_{GS}$ increases from zero, initially $i_D$ does not increase significantly, and the device is in the cut-off region (Region 1). When $V_{GS}$ reaches threshold voltage $V_{GS(th)}$, the channel has been formed then $i_D$ starts to increase noticeably. As $V_{GS}$ increases further, the device enters forward resistance region (Region 2) or so-called linear region. In this region, increasing $V_{DS}$ is increasing the electric field over the channel, then the drift speed of carriers in the channel is increased which leads to the proportionally increase of $i_D$. So, the $R_{DS(on)}$ (equal to $V_{DS} / i_D$) is fixed.

The boundary between the linear region and saturation region (Region 3) is $V_{DS} = V_{DSC} = V_{GS} - V_{GS(th)}$. $V_{DSC}$ is critical saturation drain voltage. When the device is in the saturation region, the drift speed of channel carriers is at their limits, even further increasing the electric field. So, $i_D$ is independent of $V_{DS}$. The only way to increase $i_D$ is to increase $V_{GS}$. When the $V_{DS}$ is larger than breakdown voltage $BV_{DSS}$, the reverse-biased pn junction of the intrinsic diode will have avalanche breakdown and destroy the device (Region 4).

In the third quadrant, both $i_D$ and $V_{DS}$ are negative. When $V_{GS}$ = 0, there is no channel formed and the intrinsic diode is conducting in reverse direction (Region 6). When $V_{GS} > V_{GS(th)}$, a conducting channel is formed as in first quadrant, and the device is in the reverse resistance region (Region 5). It is similar to the linear region, only with a reverse current.

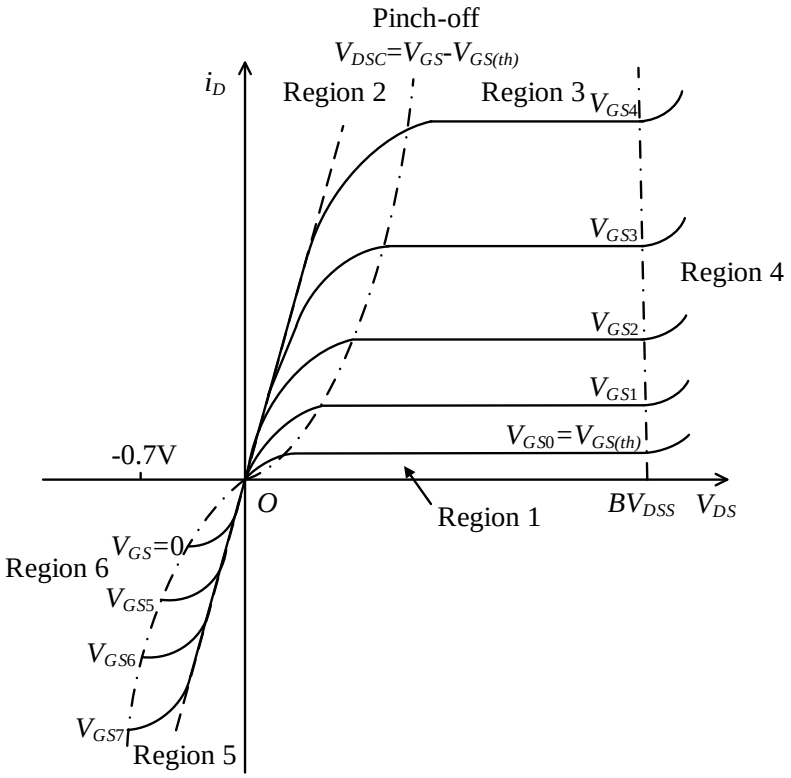



*Figure 2.6 Static output characteristics of power MOSFET where $V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > V_{GS0} = V_{GS(th)}$, $V_{GS7} > V_{GS6} > V_{GS5} > V_{GS(th)} > 0$, Region 1 is cut-off region, Region 2 is forward resistance region (linear region), Region 3 is saturation region, Region 4 is avalanche breakdown region, Region 5 is reverse resistance region, Region 6 is intrinsic diode conducting region.*

When the device is in the saturation region, $i_D$ will change with $V_{GS}$ as in Figure 2.7, which is the MOSFET's transfer characteristics. After $V_{GS}$ reaches $V_{GS(th)}$, the $i_D$ versus $V_{GS}$ characteristic becomes linear, the slope being the transconductance $g_m$ which equals to

$$g_m = \frac{i_D}{(V_{GS} - V_{GS(th)})}. \tag{2.2}$$

In Figure 2.7, when $i_D$ is smaller than boundary current $I_{DQ}$, it has the positive temperature coefficient (PTC) meaning under the same $V_{GS}$, $i_D$ increases when junction temperature $T_j$ increases. When $i_D$ is bigger than $I_{DQ}$, it has the negative temperature coefficient (NTC) meaning $i_D$ decreases when junction temperature $T_j$ increases. The characteristics of NTC at large $i_D$ makes MOSFET have good thermal stability and advantageous in parallel working.

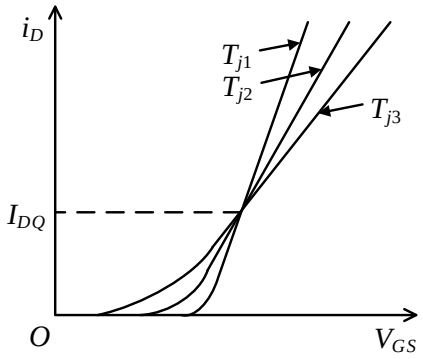



*Figure 2.7 Transfer characteristics of power MOSFET where junction temperature $T_{j1} < T_{j2} < T_{j3}$.*

## 2.2.3. On-state resistance

The conduction loss $P_{on}$ of a power MOSFET is given by

$$P_{on}=V_{DS}\cdot i_D=i_D^2\cdot R_{DS(on)} \tag{2.3}$$

According to (2.3), for a given drain current, $R_{DS(on)}$ is a crucial parameter because it determines the conduction losses. As in Figure 2.8, $R_{DS(on)}$ has several elements in series: source region resistance $R_S$, channel resistance $R_{CH}$, accumulation region resistance $R_A$, pinch-off resistance $R_{JFET}$, drift region resistance $R_D$, and drain region resistance $R_N$. $R_S$ is the sum of $n^+$ source region resistance and Ohmic contact resistance formed by source terminal metallisation. $R_N$ is the sum of $n^+$ drain region resistance and Ohmic contact resistance formed by drain terminal metallisation. $R_S$ and $R_N$ are very small, which leads to $R_{DS(on)}$ being approximated as

$$R_{DS(on)}=R_{CH}+R_A+R_{JFET}+R_D \tag{2.4}$$

Except for channel resistance $R_{CH}$, which can be influenced by the gate-source voltage $V_{GS}$, all the resistance elements depend on the structure parameter of the device including $R_{CH}$. For example, the channel resistance $R_{CH}$ increases as the length $L$ of the channel becomes longer. The accumulation region resistance $R_A$ is defined by the area of the gate.

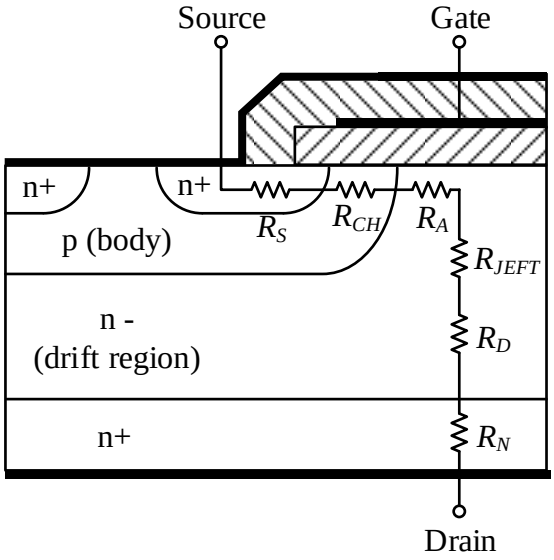



*Figure 2.8 On-state resistance compositions of an n-channel MOSFET.*

At lower breakdown voltages (a few hundred volts or less), all components contribute more or less equally to the total $R_{DS(on)}$. The device manufacturer attempts to minimise the contributions by using the heaviest doping in each region consistent with other requirements such as breakdown voltage requirements. When the breakdown voltage is higher than a few hundred volts, the drift region resistance dominates.

When the gate-source voltage increases, the on-state resistance decreases. This change is quite evident for devices with low breakdown voltage while having a limited impact on high breakdown voltage device. Moreover, the on-state resistance has a positive temperature coefficient (PTC). The rise of junction temperature causes the electron mobility to drop, which increases the resistance. Because the drift region is more sensitive to the change of the electron mobility, higher breakdown voltage leads to higher PTC. The third influencing factor is the breakdown voltage. Higher breakdown voltage can increase the thickness of the drift region which increases the drift region resistance. The last

influencing factor is the drain current. When the drain current builds up, the drain-source voltage is increasing. With the same gate-source voltage, the $R_{DS(on)}$ is bigger.

Because $R_{DS(on)}$ usually has a magnitude of mΩ, the voltage drop across the MOSFET would also be consequently small. Given the conduction voltage drop of a power diode usually is around 1 V, even the conduction voltage drop of a Schottky diode is around 0.6-0.8 V, when having the same current going through the device, the MOSFET will have significantly smaller conduction losses which leads to higher overall efficiency. Small conduction voltage makes bidirectional device MOSFET advantageous when using as a rectification device by replacing diodes, which is termed as the synchronous rectification of the MOSFET.

Some techniques have been applied to improve the on-state resistance. An easy way is to decrease the conductivity path. The VVMOS is an example, which changes the shape of the gate to a V-shaped groove and eliminates the pitch-off resistance significantly. And a very successful example is the super-junction (SJ) MOSFET, which will be discussed in detail later.

### 2.2.4. Switching characteristics

The MOSFET has equivalent capacitances between its terminals, namely $C_{gs}$, $C_{gd}$, $C_{ds}$, as shown in Figure 2.9. When output between drain and source is short-circuited, the input capacitance $C_{iss}$ equals to the sum of the $C_{gd}$ and $C_{gs}$; the common source output capacitance $C_{oss}$ equals to the sum of the $C_{gd}$ and $C_{ds}$. The reverse transfer capacitance $C_{rss}$ equals to $C_{gd}$. There is a resistor $R_g$ connected to the gate, which is the representative of the sum of the output impedance of voltage source $v_g$ and internal gate resistance of MOSFET. $R_g$ forms the input circuit with $C_{iss}$. The time constant $\tau$ of the input circuit is given by

$$\tau = R_g \cdot C_{iss} = R_g \cdot (C_{gs} + C_{gd}) \tag{2.5}$$

Because of the Miller effect, $C_{gd}$ will become effectively $1+A_v$ times bigger when the MOSFET is in the saturation region ($-A_v$ is the voltage gain of the inverting amplifier, $A_v >> 1$). This effect generates the Miller Plateau during turn-on. Changing $R_g$ will change

the duration of the Miller Plateau accordingly. A small $R_g$ will cause a fast switching period, but the overshoot voltage will also occur during switching and probably cause an EMI (electro-magnetic interference) issue. A large $R_g$ increases the turn-on time and cause delays in switching responses, but the switching curve will be smooth. In practical applications, the value of $R_g$ is reasonably chosen and usually recommended by manufacturer's reference.

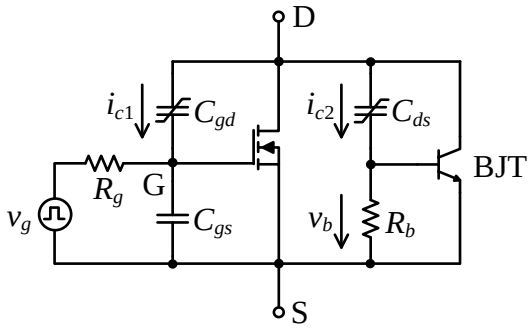



*Figure 2.9 Switching equivalent circuit of an n-channel MOSFET.*

Figure 2.10 shows the typical capacitances of the IPW60R041P6 MOSFET as a function of drain-source voltage $V_{DS}$. The change of $C_{iss}$ is not significant during the increase of $V_{DS}$. The $C_{oss}$ continuously decreases when $V_{DS}$ increase. As increasing $V_{DS}$, $C_{rss}$ decreases rapidly at first but starts to increase after $V_{DS}$ reaches a few tens of volts.

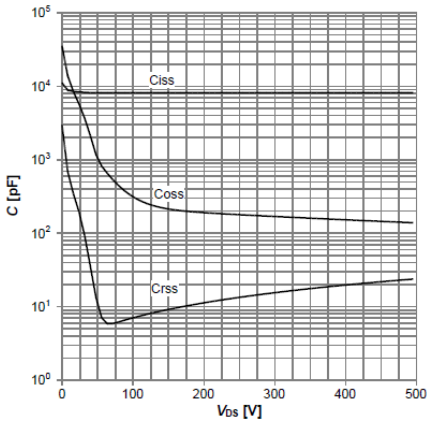



*Figure 2.10 Typical capacitances of IPW60R041P6 as a function of $V_{DS}$ under the conditions of $V_{GS}$ = 0 V, f = 1 MHz* [9].

Because of the NTC at large drain current, there is impossible for the heat feedback but possible for high d*v*/d*t* to cause the secondary breakdown of the device. In Figure 2.9,

when the voltage source $v_g$ increases, there will be displacement currents $i_{c1}$ and $i_{c2}$ going through $C_{gd}$ and $C_{ds}$, both of which will misconduct the device. Assuming the device is off and $v_g = 0$, according to the Miller effect, the $i_{c1}$ will completely go through $R_g$ and create a positive gate-source voltage $V_{GS}$ which equals to

$$V_{GS}=i_{c1}\cdot R_g=C_{gd}\cdot\frac{dV_{DG}}{dt}\cdot R_g. \tag{2.6}$$

When $\mathrm{d}V_{DG}/\mathrm{d}t$ is big enough, $V_{GS}$ reaches the threshold voltage $V_{GS(th)}$ and the device will be misconducted. In order to avoid false turning on, the gate and source terminals should not be open circuit, or a negative voltage should be added to $V_{GS}$. The threshold voltage $V_{GS(th)}$ is dropping when temperature increases, so the device should avoid running under high temperatures.

As mentioned in Section 2.2.1, there is a short circuit between the p body region and source terminal to deactivate the parasitic BJT. However, this short circuit cannot be perfect so $R_b$ is used to model p-body resistance. When the current in the device is negative, the current will flow from source through $R_b$ to drain. After passing the base of the parasitic BJT, current will continue going through the pn junction of the intrinsic diode. When the current in the device is positive, the displacement circuit $i_{c2}$ will create a voltage drop across the $R_b$ which equals to

$$V_b=i_{c2}\cdot R_b=C_{ds}\cdot\frac{\mathrm{d}V_{DG}}{\mathrm{d}t}\cdot R_b. \tag{2.7}$$

When $\mathrm{d}V_{DS}/\mathrm{d}t$ is big enough, the $V_b$ could turn on the parasitic BJT and consequently have current flow from drain to source. Concretely, when $V_{DS}$ increases to the avalanche breakdown voltage of the collector junction of BJT, and the emitter junction turns on by $\mathrm{d}V_{DS}/\mathrm{d}t$, then the electrons injection from collector to base will accelerate the avalanche in emitter region. The holes created by avalanche will flow to emitter through $R_b$, which makes further increase of $V_b$ and injection in the emitter region. A positive current feedback has formed, and the process is called avalanche multiplication. In order to avoid avalanche multiplication which damages the device, $R_b$ must be designed very small.

While $R_b$ has positive correlation to breakdown voltage and junction temperature, a compromise has to be made [4].

## 2.3. IGBT

Bipolar device power BJT and unipolar device power MOSFET have their attributes and weaknesses. Power BJT beats MOSFET in terms of on-state voltage drop and breakdown capacity due to its conductance modulation effect. Power MOSFET has better switching frequency and input impedance characteristics because it frees from minority carrier storage effect which affects BJT. More importantly, voltage-control MOSFET is convenient to implement and requires lower power to drive. The power BJT is a current-controlled device and needs a high driving power. The complementary characteristics in these two devices lead to an attempt to new devices combining advantages of both. There emerges IGBT which is one of the new devices.

Figure 2.11 shows the vertical cross-section of an n-channel IGBT. Comparing to Figure 2.1, the IGBT has similarities with MOSFET, like three terminals: gate (G), collector (C) and emitter (E). Nevertheless, IGBT has one more region – $p^+$ injecting region at the bottom connecting with the terminal collector. This extra region creates an extra junction $J_1$ which makes IGBT has three junctions $J_1$, $J_2$ and $J_3$ in total. The $n^+$ buffer region between the $n^-$ drift region and the $p^+$ injecting region is not essential for the operation of the IGBT and some are made without it. IGBT with this region is termed as NPT-IGBT (non-punch through IGBT) while IGBT without this layer is termed as PT-IGBT (punch through IGBT) [4].

Figure 2.12 shows the circuit symbols for an enhancement n-channel, an enhancement p-channel, a depletion n-channel, a depletion p-channel IGBT. The direction of the arrow indicates the direction of pn junction of $J_3$. Like MOSFET, the dashed-line channel indicates the channel is to be enhanced, which stands for enhancement mode. The full-line channel indicates the channel is to be depleted, which stands for depletion mode.

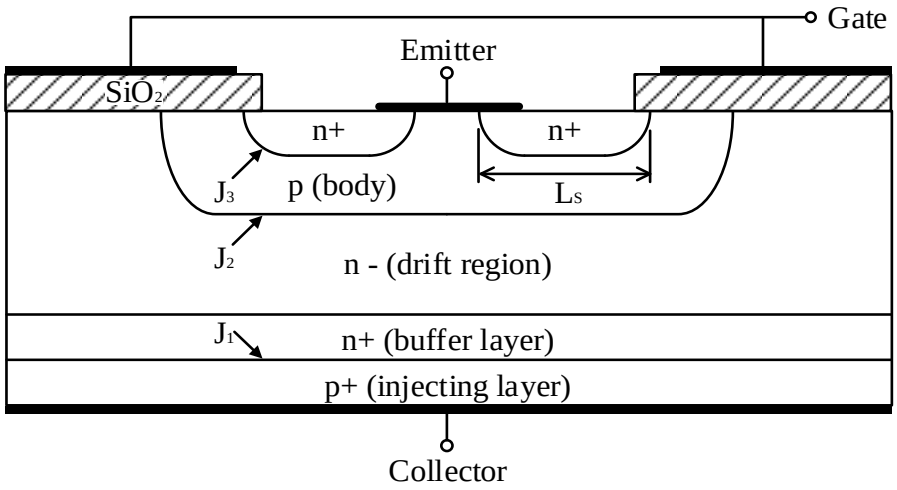



*Figure 2.11 Vertical cross-section of an n-channel IGBT adapted from* [4].

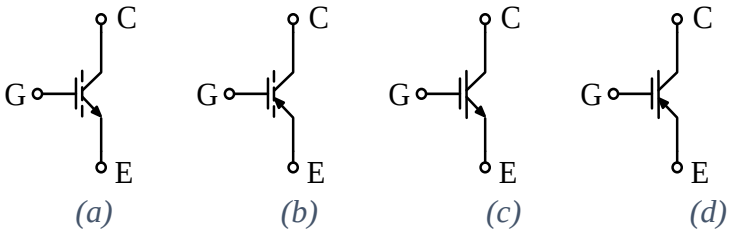



*Figure 2.12 Circuit symbols for (a) enhancement n-channel, (b) enhancement p-channel, (c) depletion n-channel, (d) depletion p-channel IGBT.*

### 2.3.1. Structure

Similar to MOSFET, the gate-emitter voltage $V_{GE}$ of IGBT controls the states of the device. Even collector-emitter voltage $V_{CE}$ is positive, if no voltage is added between gate and emitter, there is no channel formed and no current flow between collector and emitter. The forward blocking voltage of device depends on the avalanche breakdown voltage of $J_2$. Only when $V_{GE}$ is bigger than threshold voltage $V_{GE(th)}$ there forms an inversion layer in the p body region and the channel. Then device is forward conducting.

Adding p+ injecting region contributes to the conductivity modulation when the device is conducting. The conductivity improves because high-level injection of minority carriers' holes from p+ injecting region to n- drifting region. $N^-$ drift region is flooded with carries (n = p) like pin diode. This increases the conductivity of the drift region and significantly

reduce the drift region resistance, which is why the IGBTs can be used in high voltage applications [3].

Besides, adding $p^+$ injecting region makes the minority carriers in $n^-$ layer cannot be pull out by connected terminal like MOSFET. When the device turns off, the minority carriers in $n^-$ layer can only disappear by natural recombination which causes the current trailing effect in IGBT. The trailing current is undesirable because the turn off losses will be increased since the collector-emitter $V_{CE}$ is quite high at its off state. As in Figure 2.13, PT-IGBT has heavily doped $n^+$ buffer region which can enhance the removal of the minority carriers in the drift region and thus shorten the time of the trailing current. While NPT-IGBT minimise the trailing current by designing the IGBT such that the MOSFET section can take as much current as possible when device turns off. In this way, most of the current in MOSFET section will disappear immediately and leaving only small part of remaining charge for the BJT part as the trailing current.

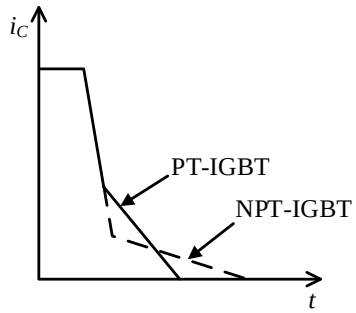



*Figure 2.13 Tail currents of NPT-IGBT and PT-IGBT.*

While nowadays, some state-of-art IGBTs can have MOS-like turn off characteristics, like trench-/field-stop IGBT from Infineon. The FS IGBT does not have as thick a drift region as the NPT-IGBT but implements a field-stop layer. Trench IGBT adopts a trench gate structure, which increases the channel density and reduce the forward voltage drop significantly [10].

Unlike the MOSFET which can provide a reverse current path, the IGBT cannot conduct in reverse direction. When $V_{CE}$ is negative, junction $J_1$ is reverse biased. No matter if there is a channel or not, the current cannot flow between collector and emitter. At this moment, the device is reverse blocking.

### 2.3.2. Equivalent circuit

As mentioned in Section 2.3, IGBT is the combination of the MOSFET and the BJT. With further explanation, it is a MOSFET-driven BJT. Its equivalent circuit is shown in Figure 2.14 where $i_D$ is the current going through the MOSFET and the $i_T$ is the current going through the BJT. It is obvious that the collector current can be calculated as

$$i_C=i_T+i_D=\beta i_D+i_D=(1+\beta)i_D \tag{2.8}$$

where $\beta$ is the BJT's common emitter current gain.

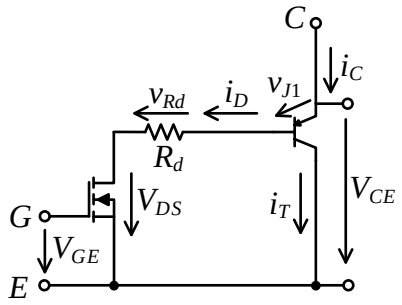



*Figure 2.14 Equivalent circuit of IGBT.*

From another angle to see the current tailing effect. In Figure 2.14, when $V_{GE}$ = 0 V, the MOSFET turns off and $i_D$ drops to zero. While $i_T$ can only disappear as in an open-base BJT which cause the tailing current when IGBT turns off.

### 2.3.3. Switching characteristics

Figure 2.15 shows a switching equivalent circuit of IGBT which is more accurate than Figure 2.14 when analysing switching process. IGBT also has equivalent capacitances between its terminals, namely $C_{ge}$, $C_{gc}$, $C_{ce}$. When output between collector and emitter is short-circuited, the input capacitance $C_{iss}$ equals the sum of the $C_{gc}$ and $C_{ge}$; the common emitter output capacitance $C_{oss}$ equals the sum of the $C_{gc}$ and $C_{ce}$. The reverse transfer capacitance $C_{rss}$ equals $C_{gc}$. The resistance $R_g$ represents of the sum of output impedance of voltage source $v_g$ and internal gate resistance of IGBT.

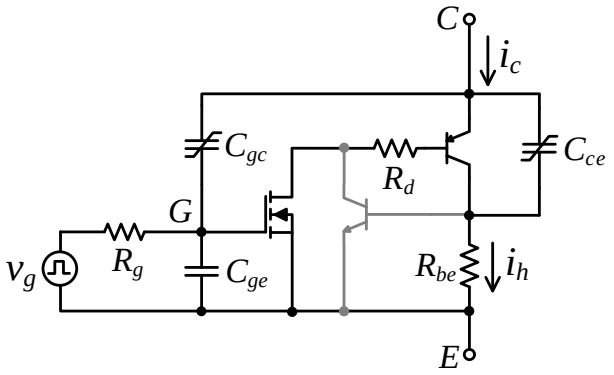



*Figure 2.15 Switching equivalent circuit of IGBT.*

The equivalent capacitances of the IGBT are smaller than those of a similarly rated MOSFET, especially $C_{oss}$ and $C_{iss}$. Because IGBT has the conduction modulation effect, so its allowable current density is about 20 times that of the MOSFET. This makes IGBT has smaller chip area than MOSFET when they are about same capacity, and a smaller chip area leads to smaller capacitances. An example is shown in Table 2.1. Both devices are manufactured by Infineon and have voltage rating of 600 V, current rating of 60 A. It is obvious that the capacitance of the IGBT is much smaller than MOSFET.

*Table 2.1 Capacitances of IGBT IKW30N60H3 and MOSFET IPW60R045CPA.*

| Device | Number | Key performance | $C_{iss}$/pF | $C_{oss}$/pF | $C_{rss}$/pF |
|---|---|---|---|---|---|
| IGBT | IKW30N60H3 | $V_{CE}$ = 600 V, $I_C$ = 60 A @$T_j$= 25℃ | 1630 | 107 | 50 |
| MOSFET | IPW60R045CPA | $V_{DS}$= 600 V, $I_D$= 60 A @ $T_j$=25℃ | 6800 | 320 | 7 |

* The test conditions for the IKW30N60H3 are $V_{CE}$ =25 V, $V_{GE}$ = 0 V, $f$ = 1 MHz [11].

* The test conditions for the IPW60R045CPA are $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $f$ = 1 MHz [12].

IGBT has the static and dynamic latch-up effects. Static latch-up is caused by having a large enough lateral voltage drop in drift region and then active the parasitic $N^+PN^-$ BJT. In the normal working state, the forward voltage drop across $J_3$ is small so the $N^+PN^-$ BJT is not working. As in Figure 2.15, when the collector current $i_c$ is large enough, a lateral current $i_h$ is created because most of the holes injected into the n- drift region are injected at the p body region under the channel and flow to the emitter along the bottom of n+ source. When $i_h$ in p body across shunting resistor $R_{be}$ and the voltage drop is over 0.7 V the $N^+PN^-$ BJT turns on.

There is a critical latch-up current $I_{cg}$ in static latch-up and when the collector current $i_c$ is bigger than $I_{cg}$, the IGBT is latched. When in latch-up, the gate voltage loses the control ability of the device and the only way to turn off the device is forced commutation of the current [4]. $I_{cg}$ is affected by the structure parameters. To avoid static latch-up, a peak drain current is often provided in manufacturer's datasheet to allow the device work safely. Besides, lower shunting resistance $R_{be}$ can avoid latch up. The voltage drop across $R_{be}$ needs to be lower than 0.7 V to avoid the forward bias of the $N^+P$ junction. The structure of the device needs to be designed to have a small $R_{be}$.

Dynamic latch up occurs when device turns off. At the turning off process, increasing $V_{CE}$ mainly bear on junction $J_2$, a high $dV_{CE}/dt$ will cause a growing displacement current through junction, which stimulates the turn on of $N^+PN^-$ BJT. Dynamic latch up is also influenced by collector current $i_c$ and the junction temperature $T_j$ before turn-off.

## 2.4. Wide band-gap devices

### 2.4.1. Silicon limits and wide band-gap materials

Silicon is the most widely used semiconductor for several decades. However, under the demands of high-voltage, high-temperature, high-frequency power conversion, Si has reached its limitations for continuous development of the fabrication. While wide band-gap (WBG) devices show their superior material properties than Si. Of the wide band-gap materials, Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most promising as a consequence of their outstanding properties, commercial availability of starting material, and maturity of their technological processes [13]. Figure 2.16 highlights some key properties of SiC and GaN compared to Si.

In Figure 2.16, WBG materials SiC and GaN show superior material properties compared to Si, enabling potential power devices operating at higher voltage, higher temperature and higher frequency. There is an increasing variety of device types available in both SiC and GaN, and it is expected to approach commodity status as the best-in-class solutions become clear [15]. A brief introduction in the following sections will cover several most used WBD in power electronics technology.

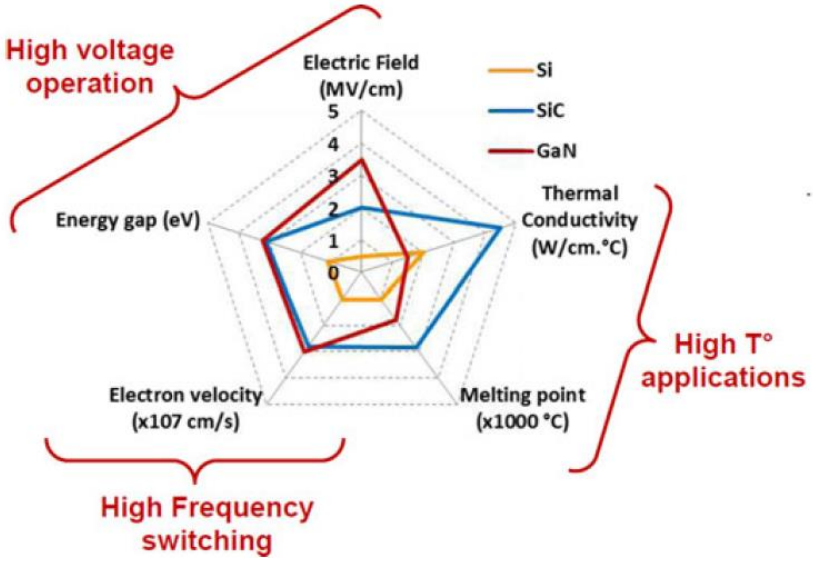



*Figure 2.16 Key electrical and thermal normalised characteristics of Si, SiC and GaN at room temperature* [14].

## 2.4.2. SiC devices

Compared to Si, SiC has greater thermal conductivity, higher critical electric field for breakdown and saturation electron drift velocity, and lower intrinsic carrier concentration [16]. All these benefits make the SiC devices have a lot of advantages than Si. However, the commercially available SiC devices are still not in mass production, which makes SiC devices costly than their Si counterparts. However, from a systematic perspective, the additional cost of SiC devices is negligible when they advantageous in many ways [17].

Among the commercially available SiC devices, SiC Schottky diodes are well-established devices and already competing with their Si counterparts. Leading manufacturers of SiC Schottky diodes include Infineon, Cree, IXYS, Microsemi, and STMicroelectronics, etc. SiC Schottky diodes have excellent robustness and proof of reliability. They often applied with Si SJ MOSFET and Si IGBT due to their low reverse recovery [18-20].

Apart from SiC diodes, SiC power transistors are well suited for high-voltage and, especially high-temperature applications. There are three most successful SiC power transistors: SiC JFET (junction-field-effect transistor), SiC BJT, and SiC MOSFET with SiC IGBT currently emerging. In the 600V voltage range, SiC power transistors are

enormously challenged by Si MOSFET and Si IGBT. When reaching 1200-1700 kV, the conduction loss of Si MOSFET becomes significant, and the switching losses of Si IGBT is large at high switching frequencies. However, SiC JFET is an excellent alternative for this voltage range because its ultralow specific on-resistance and ability to operate at high temperature and high frequencies [13]. Commercially available SiC JFET are mainly rated at 1200 V and higher voltages up to 1700V are available on the market. The current rating of normally-on SiC JFET is up to 48 A with a typical on-state resistance of 100, 85, 45 mΩ. The current rating of normally-off SiC JFET is up to 30 A and the on-state resistance of 100, 63 mΩ can be found [21]. SiC JFET has normally-on and normally-off types. The normally-on SiC JEFT is well established with a low-voltage MOSFET in a cascode topology, while normally-off SiC JFET still suffer from high resistive channels that will need further improvements.

The SiC BJT is a current-driven normally-off bipolar device. An important parameter of BJT is common-emitter current gain $\beta$, defined by the ratio of the collector current to the base current in the forward-active region. The available SiC BJT has a voltage range up to 1200 V and a current range from 6 to 40 A. The improved surface passivation technique contributes to device with 50A current rating at 100℃ and $\beta$ exceeding 100 [21]. Even though BJT is a current-controlled device, SiC BJT is still competitive for its advantages, such as low specific on-state resistance, positive temperature coefficient of the on-state resistance, fast switching speed, and are free from gate oxide [22].

The SiC MOSFET is the most recent SiC devices, which was released in 2010 from Cree at first and followed by other manufactures. SiC MOSFET has been recently commercialised up to 1200 V with a current rating of 10-20 A and the on-state resistances of 80 mΩ and 160 mΩ are available on the market [21]. For non-commercialised devices, a state-of-the-art 3.3-kV 400-A SiC MOSFET has been investigated in [23], where converter-level evaluation results revealed significant superiority of 3.3-kV SiC MOSFET in medium-voltage drives. Compared with Si counterparts, SiC MOSFET show a significant decrease in gate charge $Q_g$ and on-state resistance $R_{DS(on)}$. The effect of smaller $Q_g$ leads to a faster switching capability [15].

Even the advantages of SiC devices over their Si counterparts are quite clear, the selection of SiC devices and how they suit in particular applications are still under investigation [24-26].

### 2.4.3. GaN devices

At present, GaN-based devices are already commercialised in the photonics area, while this semiconductor material is still in a first stage concerning power application due to the lack of commercial high-quality free-standing GaN substrates [13]. Most of GaN devices are grown on Si, SiC and sapphire substrates, and the economically advantageous vertical structure of GaN is difficult to fabricate. Even so, GaN devices still are very promising with their high-frequency switching capability [27].

Limited availability of GaN substrate makes GaN family much less in contrast to SiC. The majority of commercially existing GaN power devices are GaN HEMT (High-electron-mobility transistor) and HEMT-derivatives. GaN HEMT has remarkable trade-off between specific on-resistance and breakdown voltage and are already commercially available up to 600 V. Their performance of the square breakdown voltage per specific on-resistance FOM ($V_{BR}^2 / R_{on}$) is projected 100 times over Si power devices. The combination of high speed and low-loss switching performance makes these devices vary attractive for switching power supplies with ultrahigh bandwidth (in the megahertz range) and as microwave power devices for base station of cellular phone [13].

However, GaN HEMTs are intrinsically normally-on devices, so several techniques including cascode topology have been developed allowing the integration of normally-off HEMTs [28-31].

### 2.4.4. Summary

WBG devices have many prospective applications including transportation electrification, downhole drilling and renewable energy [21]. The application of WBG devices as battery interface, motor controller, etc., in a hybrid electric vehicle will contribute to the whole powertrain system not only by their high-temperature, high-power density, and high-efficiency, but also be beneficial to the further development from their reduced volume

and light weight [32-36]. The need for high-temperature converters in downhole drilling can also be met by using WBG devices. The efficiency of photovoltaic inverters can be improved by implementing WBG devices. Because of the high blocking voltage and higher efficiency, the WBG devices also play an important part in future electrical power grids such as high-voltage dc transmission, static compensators and solid-state power transformers [16].

Although the attributes of WBG devices are evident, processing is more difficult than with Si and some of the parameters vary significantly with a wide operating (and processing) temperature. For example, SiC sublimes at high temperature characteristics around 1800℃, while Si melts at a lower temperature of 1415℃ [3]. And even GaN theoretically offers better high frequency and high-voltage performances, the lack of good-quality bulk substrates needed for vertical devices and the lower thermal conductivity makes SiC more suited for high-voltage devices [13]. WBG devices also have practical application issues, for example, d$v$/d$t$-induced conduction and gate threshold shift can be problems with the SiC MOSFET [37]. Furthermore, the modelling and electrothermal characterisation tools for the WBG devices are still under development. The design of their packaging, drivers, controllers still needs much research effort [38].

## 2.5. SJ MOSFET

The silicon SJ MOSFET is a variant of the traditional vertical MOSFET and it is the first device to break the silicon limitation for its “super-junction” structure. The super-junction based vertical device was proposed firstly in 1980, and commercial products according to this were developed in the late 1990s [39-41] with two successful representatives CoolMOS and MDMesh from leading manufactures Infineon, and STMicroelectronics, respectively [42].

SJ MOSFET dominants the voltage rating of 600 V-800 V, where it challenges its Si competitor IGBT. SJ MOSFET also is compared with successful WBG devices [43] such as SiC JEFT [44], SiC MOSFET [45] and GaN HEMT [46] more often than ever, especially under its continuous development towards wider voltage ratings.

## 2.5.1. Structure

As discussed in Section 2.2.3, the $R_{DS(on)}$ of MOSFET will be mainly dominated by drift region resistance when the breakdown voltage reaches hundreds of volts. The seemingly irreconcilable contradiction between the high $R_{DS(on)}$ and high breakdown voltage triggered the invention of 'super-junction' technique.

Figure 2.17 shows the vertical cross-section of a CoolMOS structure using a planar gate. Comparing Figure 2.1 and Figure 2.17, instead of a low doped n-drift region in a conventional power MOSFET, CoolMOS has a 10 times to even 100 times highly doped n-drift region which consists additional p columns extend from 'p-well' region [42]. Through designing the width and pitch of the p-well region, rather than having an exponential relationship between the specific on-state resistance $R_{DS(on)} \times A$ and the breakdown voltage $V_{BR}$, $R_{DS(on)} \times A \approx V_{BR}^{2.4\text{-}2.6}$ as the limitation for conventional power MOSFET, super-junction technique leads to a linear relationship between $R_{DS(on)} \times A$ and $V_{BR}$. Having low $R_{DS(on)}$ while maintaining a high breakdown voltage is the most striking feature of SJ MOSFET and makes it the first device to break the silicon limitation. For example, a 1000V CoolMOS will achieve an $R_{DS(on)}$ reduction in a range of one order of magnitude versus conventional power MOSFET [40, 41].

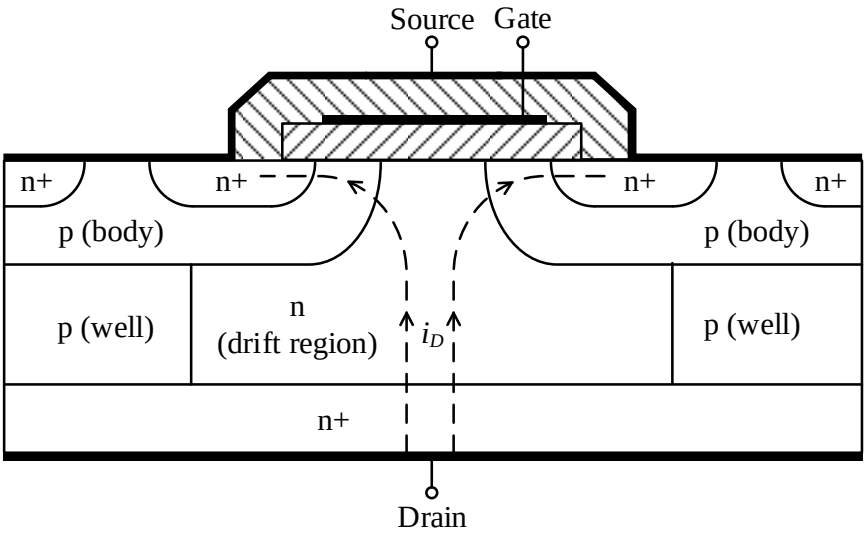



*Figure 2.17 Vertical cross-section of a CoolMOS structure using a planar gate.*

Figure 2.18 shows the specific on-state resistance for different SJ devices under Si limitation. The specific on-state resistance of CoolMOS generation C7 is 8 mΩcm$^2$ at 600 V, which is 5 times lower from the first generation CoolMOS S5. It also shows a clear trend of further decrease the specific on-state resistance for future generations [42].

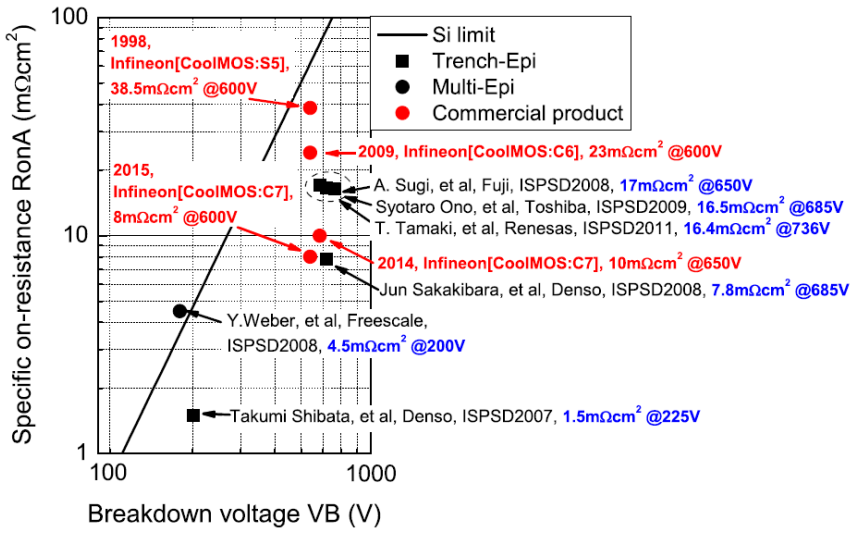



*Figure 2.18 Specific on-state resistance against breakdown voltage of different SJ devices* [42].

## 2.5.2. Summary

Except for the feature of low $R_{DS(on)}$, SJ MOSFET also has other advantages, which can be summarised as follows:

- Voltage-driven device.
- Robust gate-source junction.
- Synchronous rectification (reverse conduction) is possible.
- Good short-circuit times [47].
- Mature technology, high reliability, well-established.

All the above makes SJ MOSFET an important device in high-efficiency power electronics converters and thus the SJ MOSFET is selected for the investigation in this thesis. Using SJ MOSFET in power electronics circuits will be discussed in detail in Chapter 3.

# Chapter 3

# Switching behaviour of the Super-Junction MOSFET

## 3.1. Introduction

This chapter introduces the switching behaviour of the SJ MOSFET and reviews techniques for using the device in VSCs. The SJ MOSFET has a "super-junction" structure which makes it advantageous in having a high breakdown voltage while maintaining a low $R_{DS(on)}$. However, when using a SJ MOSFET in a VSC, the reverse recovery of its intrinsic diode and nonlinear output capacitance are problematic. Hardware and software techniques for addressing these two problems are reviewed. Advantages and limitations of alternative topologies, such as using combined single-ended converters to form a VSC, the current source converter, and the Z-source converter, are reviewed. A discussion section follows, which compares the reviewed techniques from the particular perspectives of how they address the issues presented by the reverse recovery and nonlinear output capacitance. At the end of the chapter, the research area which fills gaps left by previous techniques is identified and key objectives are outlined.

## 3.2. Problems with using the SJ MOSFET in a VSC

### 3.2.1. Reverse recovery of intrinsic diode

As discussed in Chapter 2, the intrinsic diode of the power MOSFET has adverse reverse recovery characteristics because a significant amount of excess injected charge needs to be extracted from the drift region before it establishes the blocking capability. This reverse recovery is intrinsic to the vertical structure and inevitable in all power MOSFETs.

The intrinsic diodes of the silicon MOSFET, CoolMOS (Infineon trademark for its super-junction MOSFET) and SiC MOSFET are compared in [48], all of which devices have similar power ratings. The CoolMOS's switching losses attributable to its intrinsic diode are the largest because of its super-junction architecture, which means that the drift region has higher doping and passes more reverse charge. The SiC MOSFET has the lowest switching energy because of the least reverse charge and the silicon power MOSFET exhibits intermediate performance.

In general, the poor reverse recovery characteristics of SJ MOSFET intrinsic diode will lead to a high d$v$/d$t$, d$i$/d$t$, parasitic BJT latch-up, voltage and current oscillation and potentially damage the device [49]. When used in single-ended converters in conjunction with a SiC Schottky diode, reverse recovery is eliminated and the SJ MOSFET has excellent conduction and switching performance [50]. However, when used in a VSC, simply pairing it with fast-recovery anti-parallel diodes is not normally feasible, and the problematic intrinsic diode and output capacitance $C_{oss}$ must be addressed, otherwise the benefits of the SJ MOSFET such as its low $R_{DS(on)}$, will be offset.

### 3.2.2. Nonlinear output capacitance

In a VSC, even if the intrinsic diode has been deactivated, the highly nonlinear output capacitance of the SJ MOSFET still needs to be addressed. As shown in Figure 3.1, the output capacitance $C_{oss}$ of the SJ MOSFET is highly nonlinear. The reason is related to the SJ structure. At a low drain-source voltage $V_{DS}$, the output capacitance $C_{oss}$ is defined by the 3-D surface of the blocking p-n junction. Increasing the p-columns per unit area will lead to a wider low voltage range of $C_{oss}$; At high $V_{DS}$, $C_{oss}$ is modelled as a plate

capacitor, the plate distance of which is the width of the space charge layer needed for a given $V_{DS}$, the plate size of which is the active area of the device; The $C_{oss}$ transition between low and high $V_{DS}$ is related to the lateral depletion of neighbouring p and n columns [42]. With every step forward within the super-junction process, this transition voltage range tends to narrow down and the curve of $C_{oss}$ will become more nonlinear. This change is observed by comparing three subsequent generations of SJ technology in Figure 3.1.

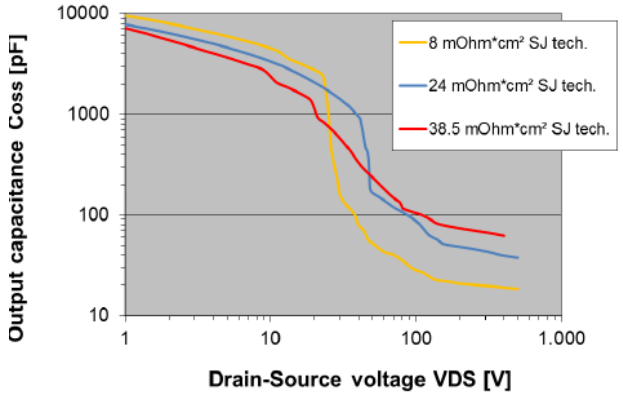



*Figure 3.1 Characteristic output capacitance of three subsequent generations of SJ technologies* [42].

The *Q-V* characteristics of the nonlinear $C_{oss}$ of a typical SJ MOSFET can be approximated as a rectangular curve, as seen in Figure 3.2. (How this curve is generated will be discussed in Chapter 4). The area above the curve, limited by the peak $Q_{oss}$ and peak $V_{DS}$, is the self-discharge energy, which represents the power dissipated in the MOSFET's channel when discharging its own $C_{oss.}$ The area beneath the curve is the co-energy $E_{oss}$, representing the power dissipated in the MOSFET when it fully charges the complementary device's $C_{oss}$. For example, in a VSC bridge-leg, when the low-side MOSFET initially turns on, it supports virtually the full rail voltage and the complementary high-side MOSFET supports barely zero voltage. According to the *Q-V* curve, the $C_{oss}$ of the high-side MOSFET is high, which leads to the low-side MOSFET supporting high voltage and sourcing a large amount of charge $Q_{oss}$ to charge the high-side $C_{oss}$. All the co-energy $E_{oss}$ during the charging will be dissipated in the low-side MOSFET which leads to low efficiency.

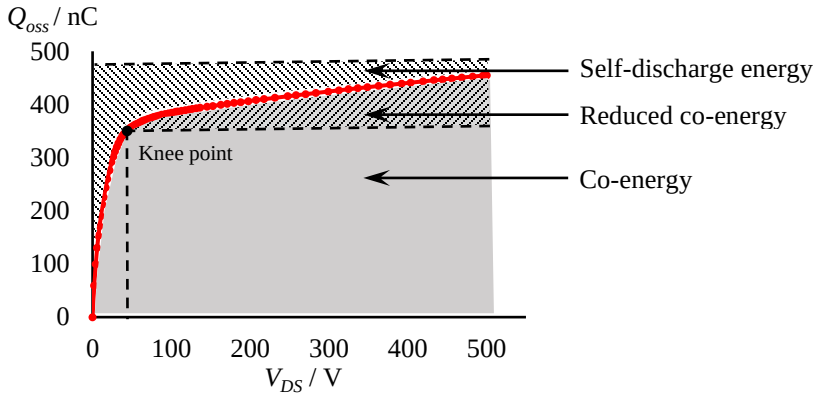



*Figure 3.2 Q-V characteristic of a typical SJ MOSFET IPW60R041P6's $C_{oss}$.*

*Table 3.1 Key data of Q-V curve in Figure 3.2.*

| $V_{DS}$ (V) | $Q_{oss}$ (nC) | Reduced co-energy (nJ) | Reduced co-energy/Co-energy (%) |
|---|---|---|---|
| 500 | 455 | 0 | 0 |
| 450 | 447 | 273.55 | 0.14 |
| 400 | 441 | 773.18 | 0.38 |
| 350 | 432 | 1966.63 | 0.97 |
| 300 | 424 | 3446.27 | 1.71 |
| 250 | 415 | 5565.25 | 2.76 |
| 200 | 406 | 8135.79 | 4.03 |
| 150 | 397 | 11116.28 | 5.50 |
| 100 | 384 | 16052.69 | 7.94 |
| 50 | 358 | 27289.34 | 13.51 |
| 0 | 60 | 201998.53 | 100 |

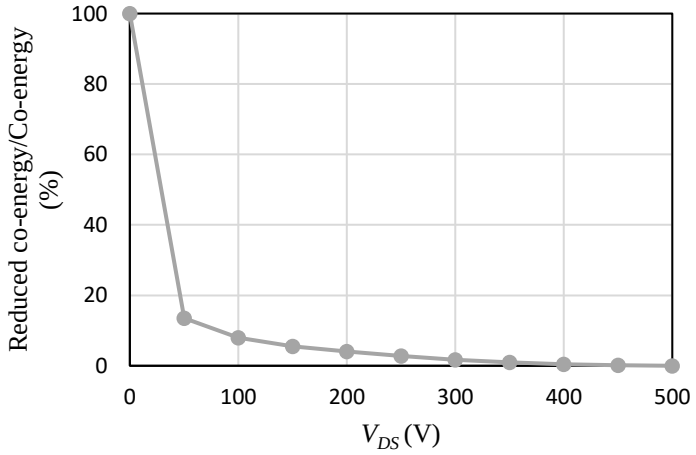



*Figure 3.3 Reduced co-energy/Co-energy as a function of $V_{DS}$.*

Due to the rectangular shape of the *Q*-*V* curve, a "knee point" exists. As seen in Figure 3.2, the voltage at the knee point has a magnitude of tens of volts, which is fixed and defined by its $C_{oss}$. For MOSFET IPW60R041P6, it is estimated as 42.37 V. When discharging $C_{oss}$ to around the knee point, but before reaching it, the co-energy is reduced to a much smaller area than the whole energy under the curve when discharging $C_{oss}$ down to zero. It is noted how abruptly the co-energy changes at around the knee point. Thus, a reduced co-energy can be realised by controlling the discharging voltage level of $V_{DS}$. Table 3.1 shows the data of $V_{DS}$ and reduced co-energy from Figure 3.2. The reduced co-energy is merely around 10% of the co-energy before the voltage discharged down to the "knee point". Figure 3.3 shows the sensitivity between the co-energy and the $V_{DS}$, where the percentage of reduced co-energy in full co-energy changes rapidly when $V_{DS}$ discharged down to 42.37 V

The output capacitance $C_{oss}$, which is given by the gradient of the curve, also changes abruptly around the knee point. High d*v*/d*t*, d*i*/d*t* will occur during the rapid change in $C_{oss}$. Lowering the dissipated energy during the charging/discharging of $C_{oss}$, and avoiding the consequent high d*v*/d*t*, d*i*/d*t* caused by nonlinearity of $C_{oss}$ are the keys to achieving high efficiency.

### 3.2.3. Summary

Since there are two problems when using SJ MOSFET in VSC, solutions should be formulated accordingly. The methods to address the reverse recovery of intrinsic diode in traditional power MOSFET can also be applied to the SJ MOSFET. The key methods for addressing the reverse recovery of intrinsic diode when using SJ MOSFET in a VSC are as follows:

(a) Deactivate the intrinsic diode and replace it with another external diode that has excellent reverse recovery characteristics.
(b) Control the commutation between the MOSFET channel and the intrinsic diode. The intrinsic diode is no longer in operation thus the reverse recovery charge will be avoided.

(c) Turn the intrinsic diode off naturally, which means the current in the MOSFET will drop to zero before the intrinsic diode starts to turn off.

In order to address the nonlinear output capacitance of using SJ MOSFET in VSC, some key concepts are as follows:

(a) Avoid fully discharging the $C_{oss}$, since the co-energy to be managed will be significantly reduced if $C_{oss}$ only has to be charged from above the knee point.
(b) Supply, or mostly supply, the charge $Q_{oss}$ from an alternative source in the power converter circuit rather than from the supply rail via the complementary device to reduce the power dissipation in the MOSFETs.
(c) Limit the d$i$/d$t$ by controlling the charging current from the supply rail inductively, by, for example, using a snubber or LC resonant current.

Some techniques in the literature were proposed based on one or more ideas from above. These techniques are categorised as either hardware-based or software-based in the following sections.

## 3.3. Hardware techniques for facilitating the use of the SJ MOSFET in the VSC

### 3.3.1. Intrinsic diode deactivation

By deactivating the intrinsic diode, the problematic reverse recovery can be avoided. In this section, techniques for adding additional devices around the SJ MOSFET to form different switching cell ("device module") permutations are discussed. Connecting a diode in antiparallel with a low-voltage MOSFET is introduced as a basic technique, and four other SJ MOSFET-based device modules are then reviewed.

#### 3.3.1.1. Anti-parallel diode

For a typical MOSFET, the forward voltage drop across its intrinsic diode is typically 1.1 V when the device is freewheeling. A typical Si Shottky diode has a lower forward voltage drop of typically 0.45 V, and passes less recovery charge. When using an external

Si Schottky diode $D_{ext}$ in anti-parallel with a MOSFET $TR1$, as in Figure 3.4, the freewheeling current, rather than flowing into the intrinsic diode, will preferentially flow through the external anti-parallel diode due to the lower forward voltage drop it presents. Better reverse recovery can also be achieved. However, when high-frequency operation is required, the stray inductances tend to inhibit the freewheeling current commutation from the MOSFET into the external Schottky anti-parallel diode at MOSFET turn-off [51].

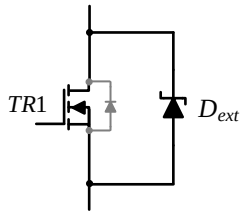



*Figure 3.4 Low-voltage MOSFET with Schottky diode in anti-parallel.*

The anti-parallel diode technique is simple to implement and is commercially available in co-packages. The FETKY MOSFET family integrates a MOSFET and a Schottky diode into one package for the benefits of reduced parasitic inductances, savings in footprint area, more convenient routing of PCB tracking, and a lower total system cost [52]. Typical products include the IRF7807VD1 from International Rectifier [53] and the NTHD3101F from ON Semiconductor [54]. MOSFETs used with integrated anti-parallel Schottky diodes usually have a low voltage rating of 20-30 V and are typically deployed in a SOIC-type package.

#### 3.3.1.2. Series and anti-parallel diode combination

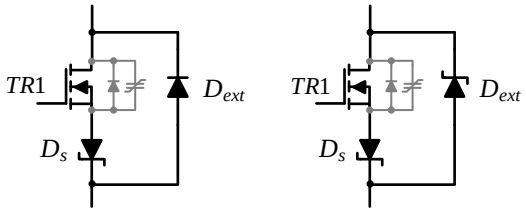



*Figure 3.5 SJ MOSFET with series and anti-parallel diodes. Left: Si fast recovery diode in anti-parallel. Right: SiC Schottky diode in anti-parallel.*

At high voltages, typically more than 300 V, Si Schottky diodes with both the required low forward voltage drop and high blocking voltage are not available, due to the unipolar conduction and relatively low doping in the drift region [42]. The Si Schottky diode is

therefore no longer suitable as an anti-parallel diode when an SJ MOSFET is the main switch because the SJ MOSFET is primarily rated for voltages of 500 - 800 V. Diodes rated for this voltage range include the SiC Schottky diode and the Si fast recovery diode. The typical forward voltage drop across the SiC Shottky diode is 1.2-1.5 V, and for the Si fast recovery diode it is 1.3-3.6 V, both of which are above the voltage drop across the SJ MOSFET's intrinsic diode. The configuration in Figure 3.4 is consequently not suitable at high voltages.

In Figure 3.5, *TR*1 is the SJ MOSFET. The series diode $D_s$ blocks the freewheeling current from flowing into the intrinsic diode. The external diode $D_{ext}$ can be either a Si fast recovery diode or a SiC Schottky diode. $D_s$ conducts the drain current when *TR*1 is on. $D_s$ only needs to have a low voltage rating. Integrated commercial products include the IXKF 40N60SCD1 module from IXYS [55] which co-packages a series Schottky diode and an ultra-fast anti-parallel diode with a 600-V rated CoolMOS device. However, literature showing its use in a simple hard-switched VSC application has not been found. This is attributed to the problems presented by the SJ MOSFET's nonlinear output capacitance, which must be taken into account before implementing it in a VSC. Another limitation of the circuit in Figure 3.5 is that operation of modules in parallel for high-power applications is challenging because the forward voltage drop of the series diode has a negative temperature coefficient [56].

#### 3.3.1.3. Synchronous rectification and anti-parallel diode

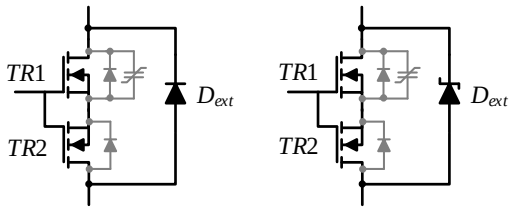



*Figure 3.6 SJ MOSFET with synchronous rectifier and anti-parallel diode. Left: Si fast recovery diode in anti-parallel. Right: SiC Schottky diode in anti-parallel.*

In Figure 3.6, power is dissipated in $D_s$ when it is conducting the drain current. Furthermore, the benefit of reverse conduction through *TR*1 is lost [57] as during the freewheeling period the reverse current flows through the anti-parallel diode, and not

*TR*1's channel. This power dissipation can be significant when the drain current is high. A Si low-voltage MOSFET with a low $R_{DS(on)}$ can be used to replace $D_s$ and realise synchronous rectification [58]. As shown in Figure 3.6, both *TR*1 and *TR*2 operate in synchronicity. *TR*2 can be a low-voltage MOSFET which allows for a low $R_{DS(on)}$ value for a given die size [51]. The low $R_{DS(on)}$ of *TR*2 will reduce the power dissipation when both switches are on, and consequently increase the efficiency.

#### 3.3.1.4. Cascode topology

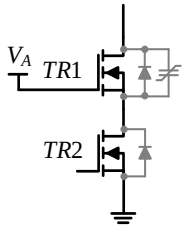



*Figure 3.7 SJ MOSFET in cascode topology.*

The cascode configuration with a low-voltage silicon MOSFET has been shown to work well with normally-off GaN devices [28-31]. Several papers from J. Rodríguez *et al.* have investigated using the SJ MOSFET in a cascode topology [59-64]. As shown in Figure 3.7, a fixed voltage is connected to the gate of the SJ MOSFET *TR*1, and a low-voltage MOSFET *TR*2 is connected between the source of *TR*1 and the module ground. When *TR*2 is off, *TR*1 supports most of the rail voltage and *TR*2 blocks a voltage that is equal to or lower than the avalanche voltage of its intrinsic diode ($V_{AV}$). The gate-source voltage of *TR*1 is then $V_A$ - $V_{AV}$, which must be lower or equal to 0 V to provide the off-state. When *TR*2 is on, the gate-source voltage of *TR*1 is the difference between $V_A$ and the (very low) voltage drop across *TR*2, which should be arranged to be above the threshold voltage of *TR*1 to turn it on [59].

In [60-64], the SJ MOSFET in cascode configuration was used in a boost converter and benchmarked with the SJ MOSFET with a traditional gate driver configuration. In [64] the boost converter operates with an output voltage of 50 V and the highest power of 500 W, which is lower than the dominate voltage ranges of the SJ MOSFET. Even though the the reverse recovery charge of the intrinsic diode is essentially eliminated with the

cascode configuration, it still does not address the problem of the nonlinear output capacitance of the SJ MOSFET. This means the technique is not readily extendable, by itself, for use in VSC bridge-legs operating at typical voltages of 400 V encountered sy SJ MOSFETs.

#### 3.3.1.5. Series MOSFET and anti-parallel diode

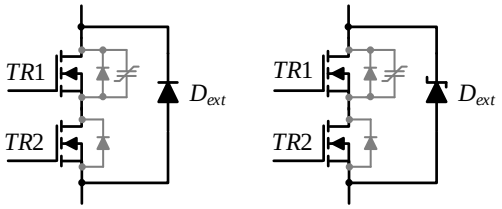



*Figure 3.8 SJ MOSFET with series MOSFET and anti-parallel diode. Left: Si fast recovery diode in anti-parallel. Right: SiC Schottky diode in anti-parallel.*

In Figure 3.8, two SJ MOSFETs, *TR*1 and *TR*2 are connected in series and used with an anti-parallel diode $D_{ext}$. The gate signals of *TR*1 and *TR*2 are synchronous, but the two gate are not referened to the same voltage potential. When both MOSFETs are freewheeling, the voltage drop across them is now the sum of the voltage drop across their two intrinsic diodes, and not only the one intrinsic diode as in Figure 3.4. The premise of this configuration actively deactivating the intrinsic diode is that this aggregate voltage drop is higher than the forward voltage drop of the anti-parallel diode, then the freewheeling current will flow through the external diode rather than the intrinsic diodes. This generally not possible at room temperature, but can be realised when the temperature drops to cryogenic levels [65].

A figure of merit (FOM) [66] related to the power losses of SJ MOSFET can be defined as

$$\text{FOM} = R_{DS(on)} \times Q_{oss}. \tag{3.1}$$

If the die size of the SJ MOSFET is doubled, the $R_{DS(on)}$ value is halved, but the $Q_{oss}$ becomes doubled which makes the FOM keeps to a constant value. The $R_{DS(on)}$ has a positive temperature coefficient and decreases with temperature but the $Q_{oss}$ is not significantly affected by temperature. According to (3.1), the FOM will consequently

decrease with temperature as well. The SJ MOSFET incurs lower power losses at cryogenic temperature (77 K) than at room temperature.

[65] has investigated this configuration in cryogenic temperature and discussed the limitations of it. The paper compared the forward voltage drop of two series-connected 600 V/50 A C 7 CoolMOS intrinsic diodes and one 1200 V/99 A SiC Schottky barrier diode (SBD) from Microsemi at 77 K. The voltage drop across the SiC SBD is only lower than the two series intrinsic diodes when the forward current is lower around 31 A. When the current higher than 31 A, multiple SBDs need to be added to avoid the conduction of the intrinsic diodes. While using many SBD will increase the size, weight, cost, switching losses etc. which lead the best solution back to the configuration in Figure 3.6.

#### 3.3.1.6. Summary

Intrinsic diode deactivation techniques using additional devices around the SJ MOSFET to form a "device module" have been presented in this section. The selection of the appropriate devices is the key to deactivating the intrinsic diode. With respect to the device selection process, the FOM [66, 67] is a useful tool. The device modules only deactivate the intrinsic diode, but do not, in themselves, address the problem of nonlinear output capacitance. They should be used in conjunction with other techniques which address the nonlinear output capacitance before their implementation in VSC.

### 3.3.2. Snubber circuits

Snubber circuits can address the nonlinear output capacitance of the SJ MOSFET when used in conjunction with intrinsic diodes deactivation circuitry in [68-72]. As in Figure 3.9, a linear snubber inductor $L_s$ is used in series with SJ MOSFETs, *TR*1 and *TR*3, in a VSC bridge-leg. The intrinsic diodes of *TR*1 and *TR*3 are deactivated by the configuration in Figure 3.6. During the operation of the bridge-leg, the charging current into $C_{oss}$ in either *TR*1 or *TR*3 is controlled by $L_{s.}$ The consequent energy stored in $L_s$ is recovered by a secondary winding $N_r$. An SMPS then returns this energy back to the rail $V_{dc}$. The snubber inductor with a modified delay time was used in a 330-V, 210-W buck converter in [68]. This snubber inductor in conjunction with the intrinsic diode deactivation circuitry has

been demonstrated in various VSC converters such as 720-V, 3-kW three-level NPC in [69], 400-V, 1.5-kW three-phase inverter in [70], and 600-V, 3-kW three-level T-type converter in [72]. One SMPS can be used to recover the energy when there are multiple bridge-legs [73]. It is reported that the losses of the snubber inductor can be a limitation when used in high-frequency applications [74].

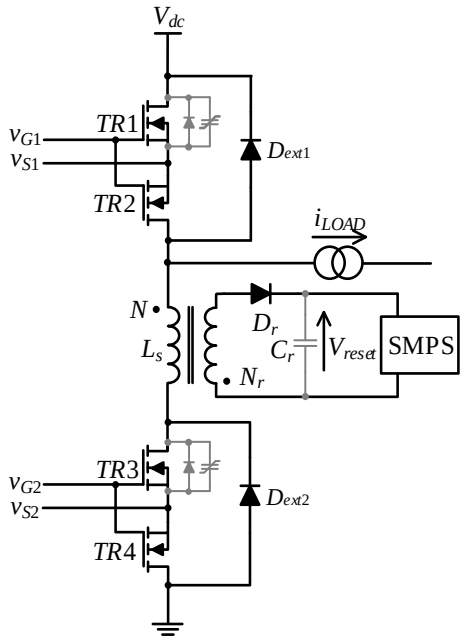



*Figure 3.9 SJ MOSFET bridge-leg with a series inductor in conjunction with intrinsic diode deactivation circuitry.*

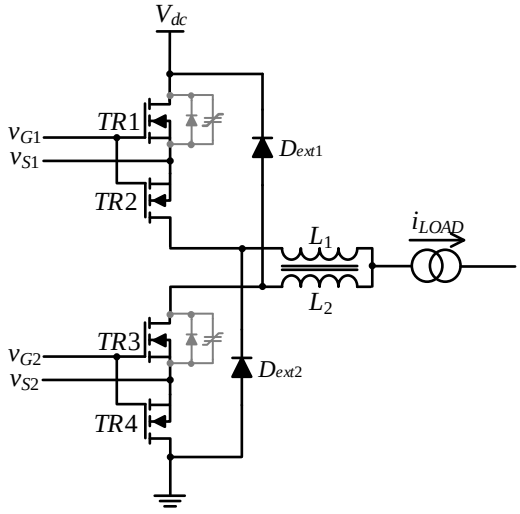



*Figure 3.10 SJ MOSFET bridge-leg with split inductor in conjunction with intrinsic diode deactivation circuitry.*

In Figure 3.10, a split inductor is used in a SJ MOSFET based bridge-leg, which works with the intrinsic diode deactivation circuit in Figure 3.6. Unlike the circuit in Figure 3.9, where the energy stored in $L_s$ is recovered into the rail voltage, the energy stored in the split inductor is dissipated in the parallel diodes. [75] uses this configuration in a 400-V 708-W buck converter switching at 50 kHz.

Compared to the traditional inductor in the single-ended converters, the inductors in both Figure 3.9 and Figure 3.10 only have to limit the d$v$/d$t$ caused by the charge/discharge of $C_{oss}$, not the reverse charge of the intrinsic diode. Thus the value of the inductance can be small in practice and implemented with air-cored coils.

### 3.3.3. Auxiliary bridge-leg

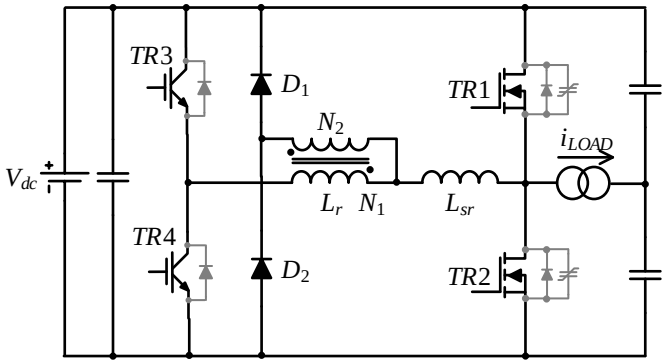



*Figure 3.11 SJ MOSFET bridge-leg with IGBT as the auxiliary switch.*

The auxiliary resonant commutated pole (ARCP) inverter in [76-78] uses extra power devices and inductance to address the problems of presented by the intrinsic diode and output capacitance of the main power devices. The main switches in the ARCP circuit turn on under ZVS conditions and the auxiliary switches only operate during the switching transition with ZCS conditions. This technique has been used with SJ MOSFET-based bridge-legs by J.-S. Lai *et.al.* in [79-82].

Figure 3.11 shows an SJ MOSFET main bridge-leg with a coupled-inductor and auxiliary bridge-leg. The coupled inductor $L_r$ is used to avoid capacitor voltage balance issue and reverse voltage blocking device requirement [83]. $L_{sr}$ is the leakage inductance of the $L_r$ as the resonant inductor. *TR*3 and *TR*4 in the auxiliary bridge-leg are IGBTs, because the

auxiliary bridge-leg conducts high resonant peak currents, and IGBTs have a constant voltage drop and low conduction losses at high currents. $D_1$ and $D_2$ are fast recovery diodes, which are used for resetting the LC resonant current. In order to establish a zero-voltage turn-on condition for the SJ MOSFETs, the resonant inductor $L_r$ should be designed with a turns ratio $N_2 > N_1$. The gate signals of IGBTs can be complementary PWM signals, and the SJ MOSFETs are turned on and off following the IGBTs with a delay time $t_{dly}$. $t_{dly}$ is smaller than the dead time of bridge-leg and both times need to be set according to the design of the circuit.

[79] uses this technique, and a peak efficiency of 97.5% was reached with a 2.5-kW 380-V bridge-leg operating at 20 kHz. This has been extended to a three-phase full-bridge converter in [80] with custom modules, which minimises parasitic losses.

The coupled inductor in Figure 3.11 has the problem of resetting which might cause the saturation of the magnetic core [84]. A further approach is presented in [81, 82], where two coupled-inductors are used in each leg of a three-phase half-bridge inverter, which effectively avoids the magnetising current circulating loop and eliminates the need for a saturable inductor with additional core loss.

### 3.3.4. LLC resonant converter

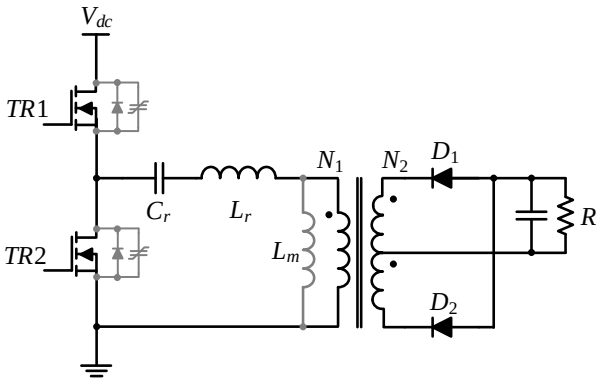



*Figure 3.12 LLC resonant half-bridge converter using SJ MOSFETs.*

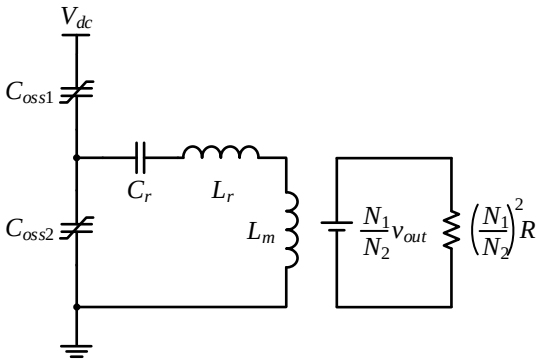



*Figure 3.13 Resonant components of the circuit in Figure 3.12.*

The LLC resonant converter topology is widely used in SMPS. An SJ MOSFET based half-bridge LLC is shown in Figure 3.12. Half-bridge topology and secondary diodes are analysed here to simplify the circuit. The secondary side diodes function as the full-wave rectifier, which can be replaced by MOSFETs to realise the synchronous rectification and decrease on-state losses. LLC resonant converter could eliminate the reverse recovery loss of the diodes and realise the soft turn-on of the switches, which makes SJ MOSFET a suitable choice to implement [85-87].

Figure 3.13 shows the resonant components of the LLC circuit in Figure 3.12. The output capacitance of *TR*1 and *TR*2 are used as resonant components. The ZVS turn-on is achieved by using the energy stored in inductor $L_r$ and the magnetising inductance of the transformer $L_m$, to discharge the output capacitance $C_{oss1}$, $C_{oss2}$ through resonant action. When both *TR*1 and *TR*2 are off during the deadtime, and *TR*1 is about to next turn on, $C_{oss2}$ is discharged down to zero and $C_{oss1}$ is fully charged to $v_{in.}$ If an appropriate resonant current $i_r$ can be provided to discharge $C_{oss1}$, which make the switch-node voltage increase and eventually reach $v_{in}$, then ZVS can be realised for *TR*1. And *TR*2 the same [88, 89]. [90] has reached an efficiency of 97% for a 10-kW full-bridge LLC resonant converter using SJ MOSFETs. Frequencies over 100 kHz can be used to realise a compact design.

### 3.3.5. Intelligent commutation schemes

Hardware techniques using auxiliary circuits embedded in the MOSFET gate driver circuits to actively assist in commutation are categorised here as intelligent commutation schemes. Three schemes for use with SJ MOSFETs in VSCs are discussed in this section.

### 3.3.5.1. Drain current injection

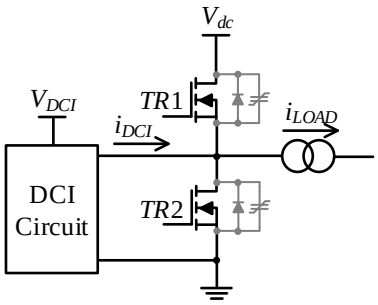



*Figure 3.14 SJ MOSFET based bridge-leg with outlined drain current injection circuit and indicated injection current.*

The concept of drain current injection (DCI) is to inject current into the drain of the synchronous rectifier device in a VSC immediately prior to the device being commutated. As in Figure 3.14, when the load current is positive and *TR*2 is about to turn off, the injection current $i_{DCI}$, built up by the DCI circuit, is redirected into the drain terminal of the *TR*2. *TR*2 then turns off after a delay. There are two advantages of this drain current injection when turning off *TR*2: the reverse recovery charge of *TR*2's intrinsic diode $Q_{rr}$ can be avoided since the intrinsic diode is not involved in the commutation; the bulk of the charge required by *TR*2's output capacitance $Q_{oss}$ will be sourced from a low voltage power source $V_{DCI}$ rather than the higher rail voltage $V_{dc}$. The $Q_{oss}$ supplied by $V_{DCI}$ will be enough to charge the output capacitance to above the knee point of the *Q*-*V* curve. Thus only a reduced co-energy needs to be dissipated by the incoming device, *TR*1 in this case.

The $i_{DCI}$ sourced by a DCI circuit can be built up by a boost-type converter as in [91], or with a full-bridge as in [92]. The latter can return excess the inductor energy back into the $V_{DCI}$ rail when the injection action has elapsed. $i_{DCI}$ needs to exceed the load current to reverse the current in the MOSFET and partially charge its output capacitance. The blocking voltage rating for the DCI components needs to be sufficiently high to prevent avalanching below the knee voltage in Figure 3.2 [93]. The timing of the injection needs to be pre-designed to maximise the efficiency, and delays are required to establish the current.

### 3.3.5.2. Pulse active desaturation

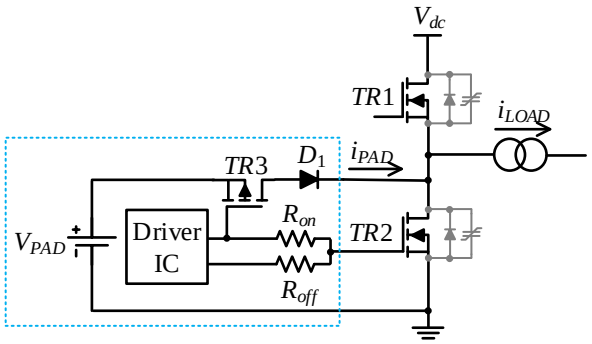



*Figure 3.15 SJ MOSFET based bridge-leg with pulse active desaturation circuit (in dotted box).*

A pulse active desaturation (PAD) circuit is proposed in [94] to reduce the commutation losses due to the nonlinear output capacitance of the SJ MOSFET. Essentially, the action is similar to that of the DCI circuit, except that the reverse current into the MOSFET is supplied from a dissipative source, unlike the DCI techniques where the current is built up in an inductor. It is pointed out that the switch *TR*3 in the PAD circuit in [94] is a P-channel MOSFET. The signal for *TR*3 is given by the high output of the driver IC on the turn-on path. So the turn-on of *TR*3 will be synchronous with *TR*2 and the turn-off of *TR*3 will be immediate, thus unwanted consumption from the driver supply can be avoided.

By adapting the gate driver to the PAD circuit, the gate driver functions as a predictive gate driver [95]. No high-voltage experimental results were given in [95], so further investigation of PAD is needed.

### 3.3.5.3. Source charge extraction

Figure 3.16 shows a bridge-leg with one device, *TR*2 acting as the freewheeling device and equipped with a series MOSFET *TR*3, an external diode $D_{ext}$ and the source charge extraction (SCE) circuit. The device module formed by *TR*2, *TR*3 and $D_{ext}$, as in Figure 3.6, deactivate the intrinsic diode of *TR*2. The SCE circuit operates collaboratively with the device module. The SCE circuit presented in [93] is demonstrated in a buck converter. By turning on the *TR*4 when the load current is freewheeling through $D_{ext}$, the SCE starts to act and charges the output capacitances of *TR*2 and *TR*3. *TR*4 turns off at the end of the

deadtime and $D_1$ then conducts. When $TR1$ turns on, it continues to charge the output capacitance of $TR2$ to $V_{dc}$. As with DCI, most of the charge into the output capacitance of the $TR2$ is supplied by $V_{SCE}$. Importantly, this means that the output capacitance needs to be charged above the knee point in Figure 3.2, so the reduced energy dissipated in the complementary device can be thus realised.

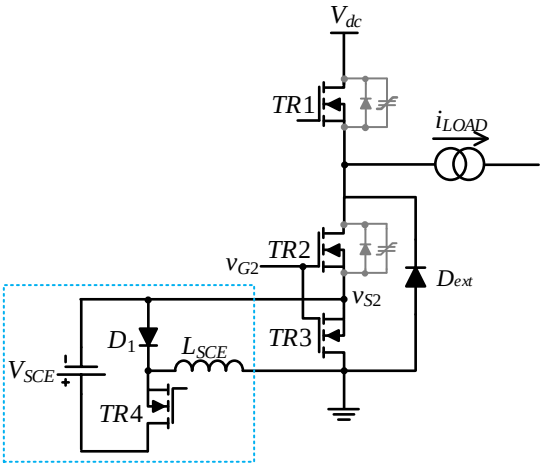



*Figure 3.16 SJ MOSFET based bridge-leg with source charge extraction circuit (in dotted box).*

Both SCE and DCI need to use SiC Schottky diode to benefit from its excellent reverse performance. SCE does not require as high current rating of the diode as DCI, however adding series MOSFET and external diode in the bridge-leg will introduce additional losses. But the series MOSFET $TR3$ provides a path to build the $C_{oss}$-charging current, which results in a faster-charging speed [93]. The activation of the SCE lays within the deadtime of the complementary signals which avoid the control complexity as in DCI.

### 3.3.5.4. Summary

In summary, the DCI, PAD and SCE techniques use additional circuitry embedded in the gate driver circuit to supply most of $Q_{oss}$ from a low voltage source rather than the higher rail voltage $V_{dc}$. They inject charge at the drain terminal of the MOSFET, so rather than having the commutation between the MOSFET channel and its intrinsic diode, the commutation happens between two MOSFET channels which avoid the activation of the intrinsic diode. SCI uses device module to deactivate the intrinsic diode in order to avoid

the $Q_{rr}$ and uses an additional circuit to supply most of $Q_{oss}$, with the fact that $Q_{oss}$ is much larger than $Q_{rr}$.

The reasons for not supplying the full $Q_{oss}$, but only charging $C_{oss}$ to above the 'knee point' are:

(a) Most $Q_{oss}$ has been supplied from the low voltage source, the remaining charge that needs to be supplied from the rail voltage is much smaller.
(b) The value of the $C_{oss}$ becomes much smaller after the knee point, and the high d$v$/d$t$ and d$i$/d$t$ have already been avoided.

## 3.4. Software techniques for facilitating the use of the SJ MOSFET in the VSC

### 3.4.1. Deadtime optimisation

In a VSC bridge-leg, when the low-side device is freewheeling, the freewheeling current will start to decrease when the high-side device turns on. If the low-side device turns off when the freewheeling current drops to zero, then its intrinsic diode will turn off naturally and the reverse recovery can be avoided. Turning off the low-side device any sooner will leave some part of the load current remaining in the intrinsic diode. Turning off the low-side device any later will cause shoot-through of the bridge-leg. The deadtime optimisation is to set an optimum deadtime to turn off the low-side device so the intrinsic diode turns off naturally and the reverse charge can be avoided.

Deadtime optimisation only avoids the reverse charge of the intrinsic diode but does not by itself address the nonlinear output capacitance. However, [96] and [97] applied the deadtime optimisation technique on a 5-kW 400-V SJ MOSFET based bridge-leg in conjunction with the snubber in Figure 3.9 to limit the charging of the $C_{oss}$. An efficiency of 99% was achieved in [96]. In [97], when benchmarked with an IGBT, the proposed technique results in a loss reduction of approximately 50%.

### 3.4.2. Phase-shift modulated bridge

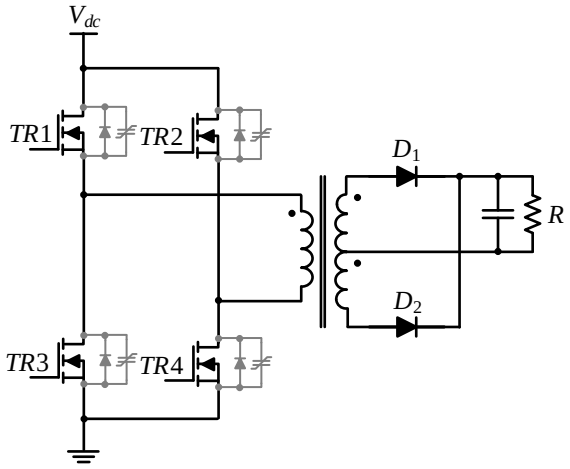



*Figure 3.17 SJ MOSFET based full-bridge converter.*

The phase-shifted full bridge has a long history of usage as the post-PFC converter [98-100]. It has the advantage of ZVS of main switches, fixed-frequency PWM operation, and wide voltage operating range. The discussion of phase-shift modulation gives a supplement of the prior art techniques and references.

In Figure 3.17, there is a SJ MOSFET based isolated full-bridge converter. Applying phase-shift modulation to the full-bridge will also deactivate the intrinsic diode and supply the charge to the output capacitance. The devices on the same bridge-leg (*TR*1 and *TR*3, *TR*2 and *TR*4) always have complementary signals to avoid the shoot-through. If *TR*1 and *TR*4 are in phase, which makes *TR*2 and *TR*3 in phase as well, the maximum output voltage will achieve. By changing the phase between the *TR*1 and *TR*4, ZVS for the SJ MOSFET will be achieved. [101] uses the 900 V CoolMOS in 6 kW dual active bridge and phase-shift modulation is used to realise the ZVS of the devices. [102] also use the same technique in the full bridge converter.

### 3.4.3. Synchronous conduction mode

As shown in Figure 3.18, there are four operating modes for a DC/DC converter: continuous conduction mode (CCM), boundary conduction mode (BCM), discontinuous conduction mode (DCM) and synchronous conduction mode (SCM). For a unidirectional

DC/DC converter, the inductor current will always above zero in the CCM. If the inductor current drops to zero before the switch next turns on, this is the DCM. The BCM is the boundary between the two. Compared to the CCM, BCM/DCM will have smaller inductor size and the intrinsic diode of the freewheeling device in BCM/DCM will turn off naturally [103, 104]. However, operating in the BCM/DCM will have a high peak-to-peak current ripple which may lead to a large RMS current. The ripple current will cause a large variation in the flux density and increase the magnetic component core losses. Both CCM and DCM can be achieved with a constant switching frequency while BCM and SCM require a variable switching frequency [105].

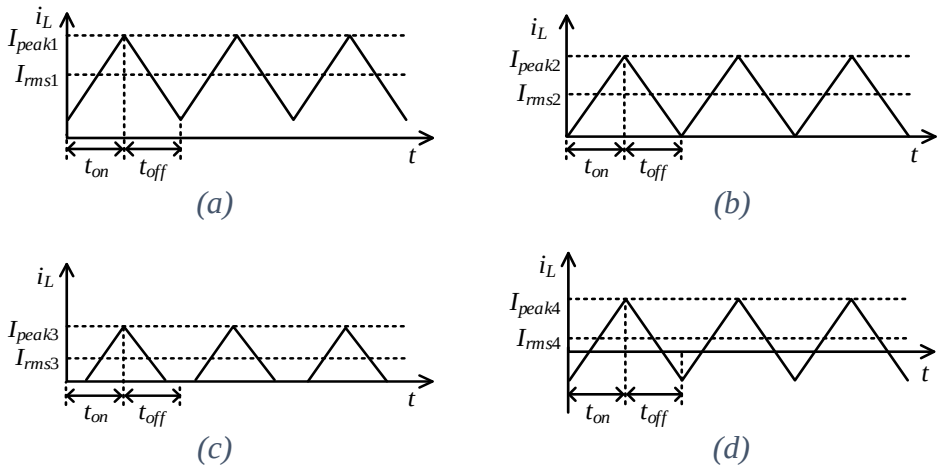



*Figure 3.18 Load current in different operation modes: (a) Continuous conduction mode, CCM; (b) Boundary conduction mode, BCM; (c) Discontinuous conduction mode, DCM; (c) Synchronous conduction mode, SCM.*

For a bidirectional DC/DC converter, the choke current can be allowed to reverse every switching cycle and become negative, which is the SCM (or triangular current mode (TCM)). The peak current and the RMS current in the choke are both higher than is the case with CCM operation, and the variable switching frequency of SCM adds difficulties in filtering. However, if the SJ MOSFET is used a bridge-leg operating in the SCM, the reverse load current will source the charge $C_{oss}$ during the deadtime, and the pre-charging of the $C_{oss}$ will create a ZVS condition for the MOSFET that is turning on. Three arrangements which use SCM for SJ MOSFET-based VSCs are introduced as follows.

### 3.4.3.1. Coupled inductor

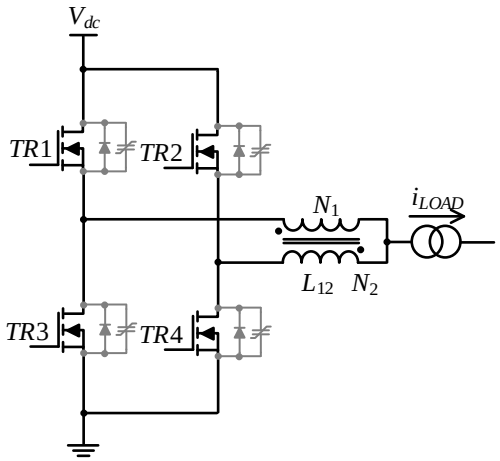



*Figure 3.19 SJ MOSFET based phase-legs with a coupled-inductor.*

In [106-108], SCM is used in a four-phase interleaved bidirectional DC/DC converter, which has two pairs of phase-legs as shown in Figure 3.19. Every two phase-legs in a pair are connected by a coupled inductor and each phase-leg in the pair is operated 180° out of phase with respect to the other. The two pairs are phase-shifted from each other by 90° in order to achieve interleaving. The SCM is achieved by designing the value of the inductor. And the use of coupled inductor will increase the utilisation of the magnetic core.

### 3.4.3.2. Capacitive turn-off snubber

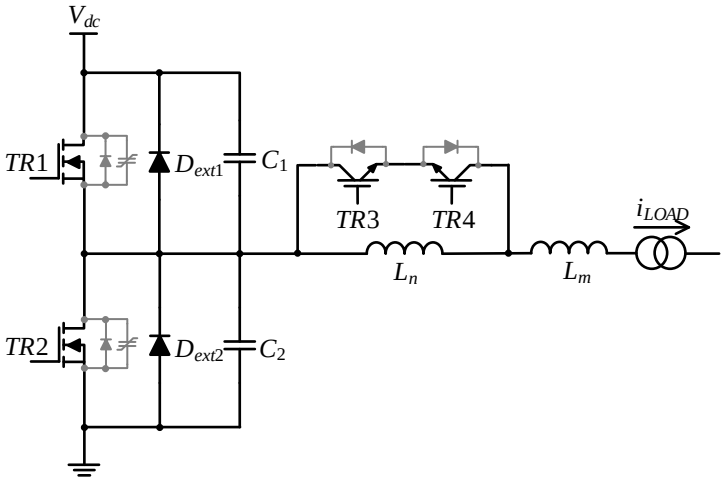



*Figure 3.20 SJ MOSFET bridge-leg with capacitive turn-off snubber and parallel diodes.*

A capacitive turn-off snubber is introduced in [109]. As in Figure 3.20, a capacitor is connected in parallel to each SJ MOSFET to slow down the voltage rise of its turn-off. The energy stored in the snubber capacitor during turn-off is recovered in a resonant fashion before MOSFET next turns on. The snubber brings the benefits of soft-switching without increasing stress on the MOSFETs.

Compared to the previous snubber circuits, no series switch or diode is connected with SJ MOSFET and only external diodes in place which are SiC diodes. The SiC diodes perform very well in parallel, in fast current commutation and it takes 0.6 μs for current slowly commutates from SiC diodes to the intrinsic diodes in the experiments of [109]. When Si diodes are used, ringing slightly increased during commutation and commutation is slower due to its lower forward drop than SiC diode. It was also discussed in [109] that the deadtime between two complementary SJ MOSFETs will have an impact on the current commutation from the parallel diodes to the intrinsic diodes, but it has no impact on the current commutation from the snubber capacitor to the parallel diode.

A similar technique was used in [110], but rather than use two IGBTs as in Figure 3.20, [110] uses one inductor to replace the *TR*4 and a diode is connected in series to control the current flow.

#### 3.4.3.3. Dual converter circuits

Dual converter circuits are essentially VSC composed of single-ended converters. Since the SJ MOSFET has an excellent performance in single-ended converters such as buck, the dual buck converter will also perform well with SJ MOSFET. Figure 3.21 shows a dual buck converter where two buck converters are combined to supply positive and negative base-frequency components of the AC current $i_L$. Buck converter (*TR*1, $D_1$) sources positive current half-cycles into the load with *TR*2 operating in low frequency. The other buck converter (*TR*4, $D_4$) sources negative current half-cycles into the load with *TR*3 operating in low frequency.

[111] proposed an SJ MOSFET based three-phase inverter with each phase contains a dual-buck converter. [112] replaced the freewheeling diode with the SiC MOSFET and a modest efficiency improvement is attained.

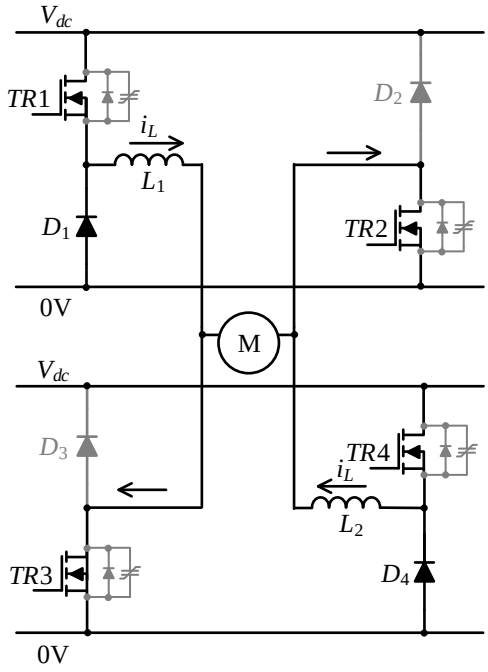



*Figure 3.21 SJ MOSFET based dual buck converter.*

## 3.5. Alternative topologies to the VSC

The SJ MOSFET is well established in single-ended converters such as buck and boost [50] converter but as discussed in this chapter, challenges exist when using it in VSCs. However, it has been shown to work well in the current source converter (CSC) and Z-source converter (ZSC, or impedance source converter).

### 3.5.1. Current source converter

The CSC has a particularly advantageous application in machine drives, for it can reduce winding insulation stresses as they are not subjected to high d*v*/d*t*s. As in Figure 3.22, a CSC is shown using SJ MOSFETs. Because of the inductor at the input side and the capacitor at the output side, during the operation of the CSC, the SJ MOSFETs do not need to conduct in reverse which avoids the reverse recovery of the intrinsic diode. When the SJ MOSFET turns on, it does not need to support the charge for the output capacitance

in a complementary device. [113] uses SJ MOSFET based CSC with SiC Schottky diodes and benchmark with voltage source inverter. Experimental results show that the CSC has improved turn-on switching losses and the turn-on switching losses is much lesser than current source inverter by a magnitude.

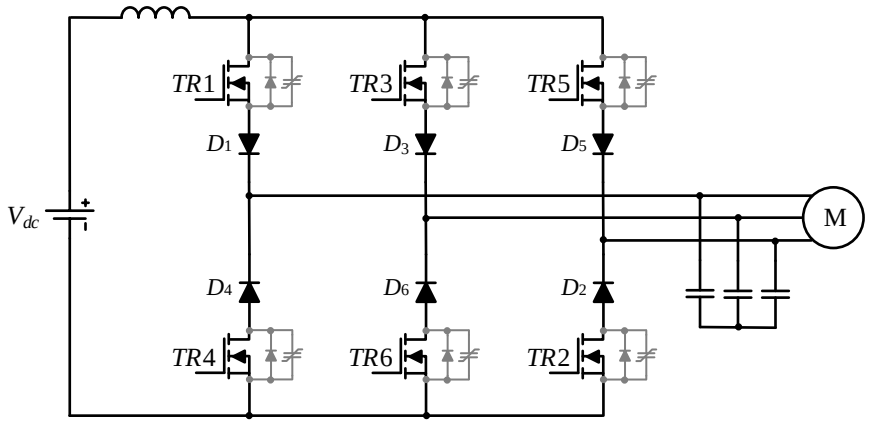



*Figure 3.22 SJ MOSFET based current source converter.*

## 3.5.2. Z-source converter

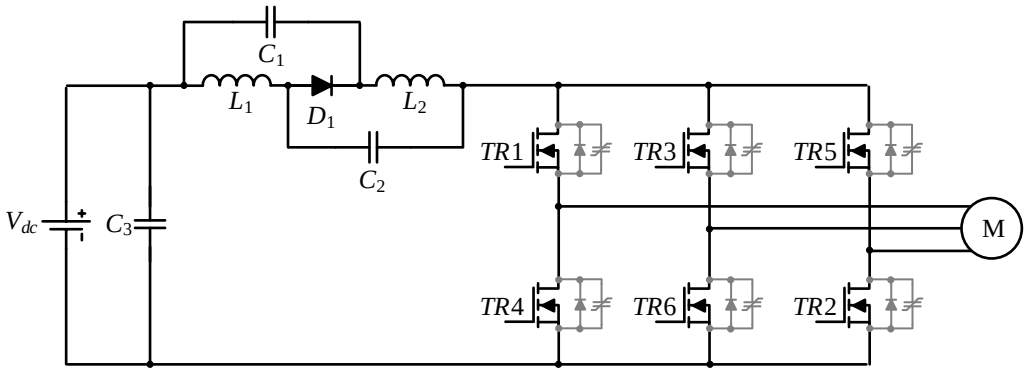



*Figure 3.23 SJ MOSFET based Z-source converter.*

The ZSC provides DC/AC power conversion and can act like a buck or a boost converter. Figure 3.23 shows a ZSC using the SJ MOSFETs. When the output capacitance of the SJ MOSFET needs to be charged during the operation of the ZSC, $L_1$ and $L_2$ provide highly turn-on snubber and effectively limiting the charging current. [114] uses SJ MOSFET based ZSC under a power of 1.5 kW and the results show that a quasi-ZSC performs well using SJ MOSFET, in contrast to other VSCs.

### 3.5.3. Summary

CSC has high losses at low-load, difficult in reversing the direction of power flow. Voltage transmission is the mainstream so the CSC is inconvenient in practical. ZSC requires large passive components and also has difficulty in reversing the direction of power flow without additional complexity. For these reasons, the VSC is likely to remain highly prevalent in most applications.

## 3.6. Discussion

### 3.6.1. Comparison of reviewed techniques

The reviewed techniques of using SJ MOSFET in VSC are compared in Table 3.2. The CSC and ZSC are not included, but the discussion of them in Section 3.5 shows an alternative option of using SJ MOSFET in converters other than VSCs.

Table 3.2 also only exclusively include the techniques applied in DC/AC power conversion. The LLC converter and the phase shift modulation, both of which for DC/DC power conversion, are discussed but not included. However, the discussion of the LLC converter and phase shift modulation provides an effective range of references and perspectives towards addressing the problems of using SJ MOSFET in VSCs.

*Table 3.2 Summary of reviewed techniques of using SJ MOSFET in VSC.*

| Techniques | | Reverse recovery of intrinsic diode | | | Nonlinear output capacitance | | Applications in literature |
|---|---|---|---|---|---|---|---|
| | | Intrinsic diode deactivation | Controlled commutation | Naturally turn off | Supply $Q_{oss}$ | LC resonant | |
| Device module | Series and anti-parallel diodes | √ | | | | | - |
| | Synchronous rectification and anti-parallel diode | √ | | | | | [68-73] |
| | Cascode topology | √ | | | | | [59-64] |
| | Series MOSFET and anti-parallel diode | √ | | | | | [76] |
| Snubber circuits | | √* | | | | √ | [66-73], [75] |
| Auxiliary bridge-leg | | √ | √ | | | √ | [79-82] |
| Intelligent commutation scheme | Drain current injection | √ | √ | | √ | | [91, 92] |
| | Pulse active desaturation | √ | √ | | √ | | [94] |
| | Source charge extraction | √ | √ | | √ | | [93] |
| Deadtime optimisation | | √ | | √ | | √ | [96, 97] |
| Synchronous conduction mode | Coupled inductor | | | √ | | √ | [106-108] |
| | Turn-off snubber | | | √ | | √ | [109, 110] |
| Dual-converter circuits | | | | √ | | √ | [111, 112] |

| Techniques | | Number of components per bridge-leg | Additional devices in the circuit | Realisation of digital control | Current feedback and sensing requirements | Comments |
|---|---|---|---|---|---|---|
| Device module | Series and anti-parallel diodes | Six | Two diodes | - | - | Cost of additional devices but the problem of nonlinear $C_{oss}$ is not addressed |
| | Synchronous rectification and anti-parallel diode | Six | MOSFET and diode/two diodes | - | - | Cost of additional devices, including switching components, but the problem of nonlinear $C_{oss}$ is not addressed |
| | Cascode topology | Two | MOSFET | - | - | |
| | Series MOSFET and anti-parallel diode | Six | MOSFET and diode | - | - | |
| Snubber circuits | | Six | Linear inductor and SMPS for core resetting | Normal | Open-loop | Require additional devices and linear inductor (*can implement intrinsic diode deactivation with deadtime optimisation) |
| Auxiliary bridge-leg | | Two | Two IGBTs, two diodes, inductor | Deliciated switching signals between IGBT and MOSFET | - | Introduce an additional bridge-leg and coupled inductor, requires modified switching signals |
| Intelligent commutation scheme | Drain current injection | Two | Two MOSFETs, two diodes | Deliciated switching signals for additional MOSFETs | Hall-effect probe and Rogowski coil | Use auxiliary circuitry to provide the $Q_{oss}$ and control the commutation |
| | Pulse active desaturation | Two | p-MOSFET, diode | Separated switching signals | - | |
| | Source charge extraction | Two | MOSFET, diode, inductor | Two separate signal generators | - | Require additional devices around the main switch and auxiliary circuitry to provide the $Q_{oss}$ |
| Deadtime optimisation [97] | | Two | Linear inductor | MATLAB controlled signal generator with deadtime adjustment circuit | Rogowski for drain current sensing | Require linear inductor, and the deadtime is adjusted to turn off intrinsic diode naturally |
| Synchronous conduction mode | Coupled inductor | Two | Coupled inductor | Digital control board with DSP TMS320F2808 | Automatic measurement function of the digital oscillograph | Additional switching devices and control is complicated. |
| | Turn-off snubber | Two | Two IGBTs, inductor, two diodes, capacitors | - | - | Combination of CCM and SCM |
| Dual-converter circuits | | - | Eight components to realise AC outputs | DSP TMS320F28335 | - | VSC composed of single-ended converters |

### 3.6.2. Limitations of the literature and proposed research areas

From the perspective of the hardware cost, the techniques in Table 3.2 generally need to use magnetic components to provide a desired resonant current for charging, or partially charging, the SJ MOSFET's output capacitance. Involving magnetic components means the increase of the size and losses, which also introduces the problem of the magnetic core resetting.

From the perspective of the software cost, well-defined signals for the intelligent commutation schemes need to be provided for the auxiliary circuitry during the commutation. The key of intelligent commutation schemes work is the accurate timing of injecting or extracting charge. For deadtime optimisation, precise switching time for the main switches is essential. Any excess advance or delay will cause shoot-through of the bridge-leg or result in incomplete intrinsic diode deactivation, both of which lead to low efficiency.

It should be noticed that it is difficult to achieve soft-switching for SJ MOSFET in all condition due to the intrinsic diode tends to introduce delay in resonant process, and thus delay the zero-voltage crossing [71].

In order to develop a solution with simple hardware, no auxiliary magnetic components and no onerous timing requirements, a dual-mode switching technique is proposed in Chapter 4. In Chapter 5 the performance of this technique is investigated with alternative power device permutations. The dual-mode switching technique is further investigated in Chapter 6 with current transformer (CT) scheme. The CT scheme will provide the drain current feedback to the gate signals. The dual-mode switching technique, with or without CT scheme, will achieve high efficiency with minimal hardware addition. The transition between the two switching modes has a wide allowable range when still maintain a satisfactory efficiency, which will have enough safety margin and no strict timing requirements during the switching process.

# Chapter 4

# High-efficiency super-junction MOSFET based inverter-leg configuration using a dual-mode switching technique

## 4.1. Introduction

When using SJ MOSFET in VSCs, in order to develop a solution with simple hardware, no auxiliary magnetic components and no onerous timing requirements, a dual-mode switching technique is proposed. The dual-mode switching technique to address the detrimental influence of the SJ MOSFET's output capacitance. The technique uses minimal extra hardware, and functions in conjunction with intrinsic diode deactivation circuitry. The circuit is designed for an 800-W inverter-leg circuit operating from a 400-V DC supply voltage and switching at 20 kHz. The full-load efficiency is approximately 98.7 %, and no forced cooling is needed.

## 4.2. Dual-mode switching technique

### 4.2.1. Intrinsic diode deactivation

Figure 4.1 shows an inverter bridge-leg that incorporates intrinsic diode deactivation circuitry. The series diodes $D_s$ prevent reverse current flowing into the SJ MOSFETs when they would otherwise be functioning as the freewheeling elements. The external diodes

$D_{ext}$ in anti-parallel are SiC Schottky diodes, which replace the function of the intrinsic diodes and can be chosen to have excellent reverse recovery characteristics.

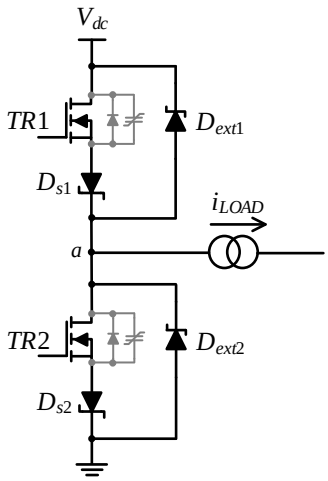



*Figure 4.1 Voltage source inverter-leg based around SJ MOSFETs equipped with intrinsic diode deactivation circuitry.*

### 4.2.2. Non-linear SJ MOSFET output capacitance

Even if the problem of the intrinsic diodes is addressed, the highly non-linear output capacitance of SJ MOSFET remains a challenge. Figure 4.2 shows the input capacitance $C_{iss}$, output capacitance $C_{oss}$ and reverse capacitance $C_{rss}$ against the drain-source voltage $v_{DS}$ on semi-logarithmic coordinates from the manufacturer's datasheet of a typical SJ MOSFET, IPW60R041P6. It can be observed from Figure 4.2 that $C_{oss}$ drops rapidly when $v_{DS}$ increases from 0 V to around 100 V. The curve then becomes slightly flatter, and $C_{oss}$ then gradually decreases until $v_{DS}$ reaches its limitation. Such drastic changes of $C_{oss}$ will be more pronounced when plotted on linear coordinates.

To observe the amount of charge required during the charging and discharging of the non-linear $C_{oss}$, the $Q$-$V$ characteristics of $C_{oss}$ need to be obtained. According to the definition of capacitance, $C_{oss}$ is given by

$$C_{oss} = \frac{Q_{oss}}{v_{DS}} \tag{4.1}$$

where the $Q_{oss}$ is the charge in $C_{oss}$. However, as seen in Figure 4.2, $C_{oss}$ varies when $v_{DS}$ changes. Rearranging (4.1) gives the incremental charge d$Q_{oss}$ :

$$\mathrm{d}Q_{oss} = C_{oss} \cdot \mathrm{d}v_{DS} \tag{4.2}$$

and $Q_{oss}$ is therefore given by

$$Q_{oss} = \int C_{oss}\, \mathrm{d}v_{DS}. \tag{4.3}$$

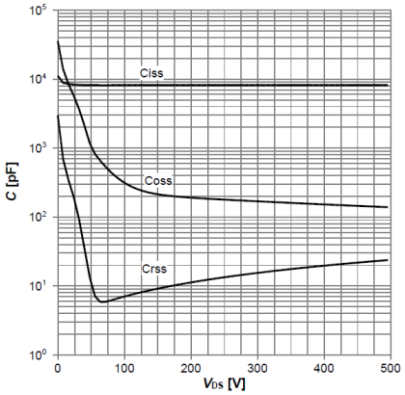



*Figure 4.2 Typical inter-terminal capacitances of a SJ MOSFET, in this case, the IPW60R041P6* [9].

The non-commercial open-source software *Engauge Digitizer* was used to acquire data of $C_{oss}$ from Figure 4.2. The *Engauge Digitizer* tool accepts image files containing graphs and recovers the data points from those graphs [115]. After inputting the data, $Q_{oss}$ can be acquired by integrating $C_{oss}$ with respect to $v_{DS}$ according to Equation (4.1). The *Q-V* characteristic of $C_{oss}$ is thus obtained and is shown in Figure 4.3.

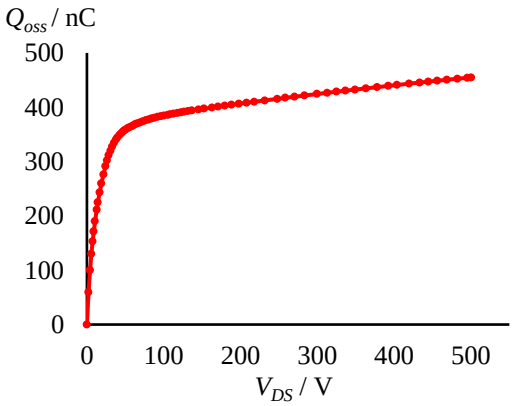



*Figure 4.3 Q-V characteristic of IPW60R041P6's $C_{oss}$.*

As seen in Figure 4.3, $C_{oss}$ is highly non-linear and can be approximated as a rectangular

*Q*-*V* curve. Consider when the load current $i_{LOAD}$ in Figure 4.1 is positive, *TR*1 is off and $i_{LOAD}$ is flowing through $D_{ext2}$. If *TR*2 is turned on when *TR*1 is off, then it fully self-discharges its $C_{oss}$. When *TR*1 next turns on, it therefore has to recharge the $C_{oss}$ of *TR*2 from 0 V up to the DC link voltage $V_{dc}$. A relatively large charge has to be sourced before inverter-leg output voltage $v_a$ reaches the 'knee point' in Figure 4.4 where $C_{oss}$ drops rapidly. A high d*v*/d*t* then occurs and consequences include EMI and parasitic oscillations. The switching energy dissipated in *TR*1 due to charging $C_{oss}$ is a minimum of $Q_{oss}V_{dc}$ which is approximated by the area (co-energy) lying under the *Q*-*V* curve.

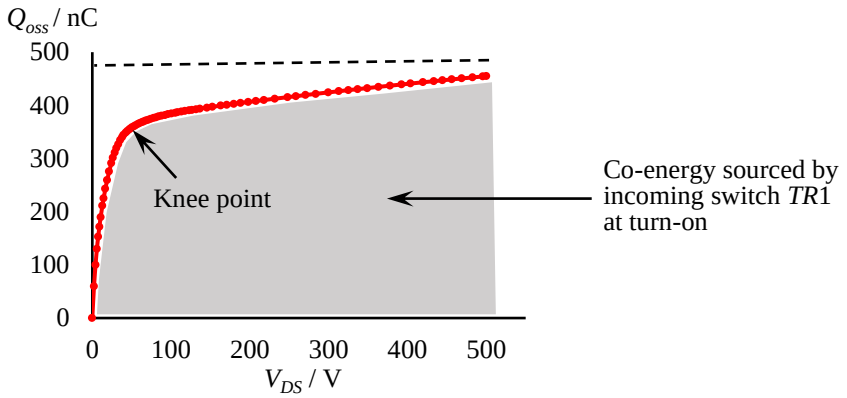



*Figure 4.4 Effect of fully discharging the $C_{oss}$ of the IPW60R041P6.*

In order to minimise switching losses and avoid the associated problems, the inverter-leg needs to operate with unipolar PWM modulation to avoid discharging $C_{oss}$ of *TR*2. With a positive $i_{LOAD}$, only *TR*1 switches and *TR*2 is held off throughout the switching cycle. By holding *TR*2 off, its $C_{oss}$ capacitance only partially discharges, down to the reverse breakdown voltage $V_{BR}$ of Schottky diode $D_{s2}$ as shown in Figure 4.5. Importantly, $V_{BR}$ is typically such that the $C_{oss}$ capacitance is not discharged to below the knee point in Figure 4.6. The energy dissipation in *TR*1 due to charging $C_{oss}$ is now approximated by the smaller shaded area.

Furthermore, the gradient of the *Q*-*V* curve of $C_{oss}$ is lower at $V_{BR}$ than it is at 0 V. When the incoming device *TR*1 turns on, *TR*2 therefore presents a lower capacitance, and *TR*1 consequently sources a smaller transient current.

Similarly, when $i_{LOAD}$ is negative, only *TR*2 switches and *TR*1 is held off throughout the

switching cycle. However, a problem arises as $i_{LOAD}$ transitions through zero, and bipolar switching is desirable in this region to avoid distortion due to $i_{LOAD}$ becoming discontinuous.

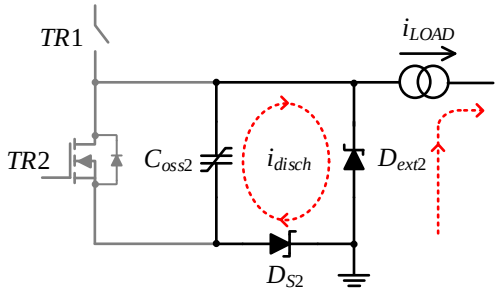



*Figure 4.5 Discharge route for $C_{oss}$ of TR2 when TR1 is off and $D_{ext2}$ is freewheeling. The circuit is operating with a positive $i_{LOAD}$ and only TR1 is being driven on and off. Provided that TR2 is not turned on during the freewheeling period, $C_{oss}$ is only discharged down to the breakdown voltage $V_{BR}$ of $D_{S2}$.*

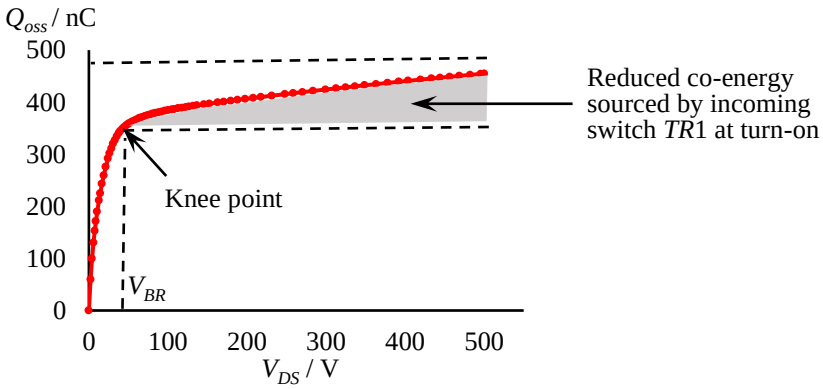



*Figure 4.6 Effect of only partially discharging the $C_{oss}$ of the IPW60R041P6.*

### 4.2.3. Proposed dual-mode switching technique

With an AC load current such as that in an inverter, a dual-mode switching control technique is proposed. In the so-called fast-switching mode, unipolar PWM modulation is selected for either *TR*1 or *TR*2 according to the direction of $i_{LOAD}$. In this mode, the MOSFETs are driven in the normal way with rapid switching transitions for low losses. However, at low $i_{LOAD}$ magnitudes, bipolar PWM modulation is enabled to reduce distortion in the AC current. The problem of high peak currents due to supplying high charges into fully-discharged $C_{oss}$ that occurs with bipolar modulation is addressed by turning the SJ MOSFETs on slowly (so-called slow-switching mode), and thereby limiting

the d$i$/d$t$ in the current conducted by the incoming MOSFET. Importantly, whilst this incurs losses, enabling the slow-switching mode only at low $i_{LOAD}$ magnitudes means aggregate power losses in the circuit are low. Simply switching an inverter slowly with SJ devices under all current levels leads to low efficiency due to the $R_{DS(on)}Q_{oss}$ product exhibited by a die area fabricated using silicon SJ technology [66].

Figure 4.7 shows the same $Q_{oss}$ for different $I_{LOAD}$ values and different current slew rates, d$i$/d$t$, where lower $I_{LOAD}$ and lower slew rate lead to lower $I_{peak}$. In the slow-switching mode, this becomes an advantage when operating bipolar PWM modulation under low load current. To change between the fast-switching mode and slow-switching mode, different gate resistances are enabled in the charging path for the MOSFET's input capacitance.

Table 4.1 summarises the dual-mode switching technique and different scenarios where each mode applies.

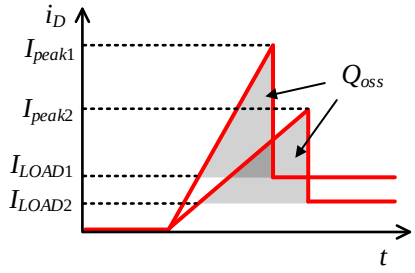



*Figure 4.7 Same $Q_{oss}$ under different $I_{LOAD}$ and different slew rate where load current $I_{LOAD1} > I_{LOAD2}$, peak current $I_{peak1} > I_{peak2}$.*

*Table 4.1 Dual-mode switching technique.*

| Dual-mode | Modulation | Switching speed | $i_{LOAD}$ |
|---|---|---|---|
| Fast-switching mode | Unipolar | Fast | High magnitudes |
| Slow-switching mode | Bipolar | Slow | Low magnitudes |

## 4.2.4. Dual-mode gate driver circuit

A gate driver circuit was designed to realise the dual-mode switching technique in the inverter-leg. As given by Equation (4.4), the d$v$/d$t$ of the driven SJ MOSFET is determined by the gate current $I_{gate}$ and SJ MOSFET reverse capacitance $C_{rss}$ which equals to $C_{gd}$. $I_{gate}$

depends on the Miller plateau voltage $V_{MP}$ and total gate resistance. This resistance consists of two parts, the internal gate resistance of the SJ MOSFET $R_{g(SJ\ MOS)}$ and the changeable external gate resistance $R_{gate}$ on the driver board. By varying $R_{gate}$, the d$v$/d$t$ will change according to

$$\frac{\mathrm{d}v}{\mathrm{d}t} = \frac{I_{gate}}{C_{rss}} = \frac{V_{MP}}{R_{g(SJ\ MOS)} + R_{gate}} \cdot \frac{1}{C_{gd}} \tag{4.4}$$

In the driver circuit arrangement in Figure 4.8, two different paths are set: a slow-switching path and a fast-switching path. In the slow-switching path, the slow-switching resistor $R_s$ is 220 Ω. In the fast-switching path, the fast-switching resistor $R_h$ is selected as 10 Ω. The turn-off resistor $R_r$ is also 10 Ω. The fast-switching path is active only when the enable signal is on. When the slow-switching mode is selected, only the slow-switching driver operates and the SJ MOSFET's input capacitance is charged at turn-on via the relatively high-value resistance $R_s$. When the fast-switching path is enabled, the gate is charged more rapidly via the parallel combination of $R_s$ and the much smaller resistance $R_f$.

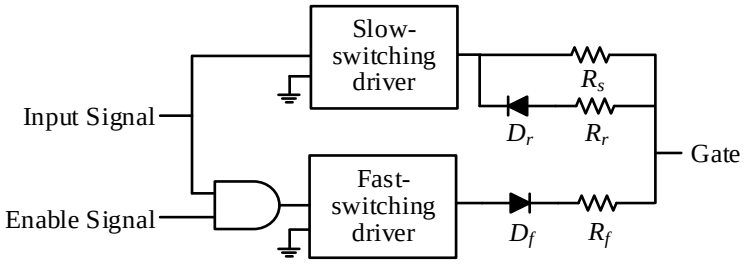


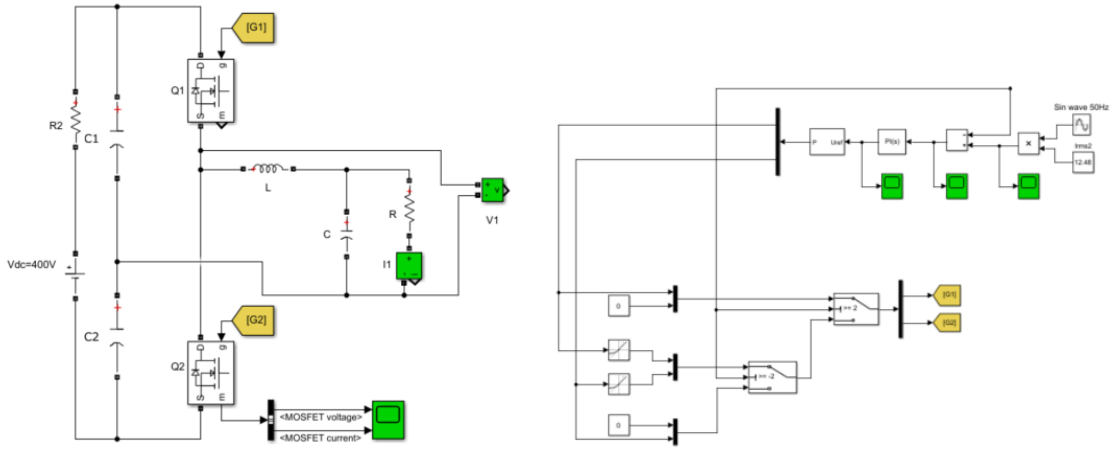

*Figure 4.8 Gate driver circuit arrangement for dual-mode switching technique.*

## 4.3. Simulation

Because the connection of multiple models may not provide the accuracy offered by stand-alone device model, the SPICE model is not used for the simulation. Software like Pspice using SPICE models are not compatible with the complexity of the circuit topologies be analysed, thus MATLAB Simulink was selected for the circuit level simulation.

Simulation of a 400-V, 800-W single-phase inverter switching at 20 kHz with the dual-mode switching technique applied was built in MATLAB Simulink. Figure 4.9 (a) shows

the power circuit of the single-phase inverter and Figure 4.9 (b) is the logic circuit of the dual-mode switching technique. The reference of the output current was set to a sinusoidal wave with a peak current of 12.48 A. When the magnitude of the output current is lower than 2 A, the slow-switching mode is selected. Otherwise, the fast-switching mode is selected.




*(a)* *(b)*

*Figure 4.9 Simulation circuits of using dual-mode switching technique in an inverter. (a) Power circuit; (b) logic circuit of dual-mode switching technique.*

Simulation results are shown in Figure 4.10. For clarity, the switching frequency was set at 2 kHz rather than 20 kHz. Figure 4.10 (a) shows the overall load current $i_{LOAD}$ and the gate signals. When $i_{LOAD} > 2$ A, *TR*1 is fast switching and *TR*2 is held off as in Figure 4.10 (b). When 2 A < $i_{LOAD}$ < 2 A, *TR*1 and *TR*2 are both in slow switching in a standard complementary manner as in Figure 4.10 (c). When $i_{LOAD} < 2$ A, *TR*2 is fast switching and *TR*1 is held off as in Figure 4.10 (d).

With reference to Figure 4.10 (a), the slow-switching ratio (SSR) is defined as the proportion of the total period of the fundamental waveform that is occupied by the slow-switching period $t_s$. By changing the SSR ratio, the percentage of two modes in one switching period is also changed. Considering the effect of charging and discharging of the $C_{oss}$, a smaller SSR is expected to have smaller overshoot in inverter-leg output voltage $v_a$ and lead to higher overall efficiency, under one precondition, there is not any distortion caused by discontinuous output current $i_{LOAD}$.

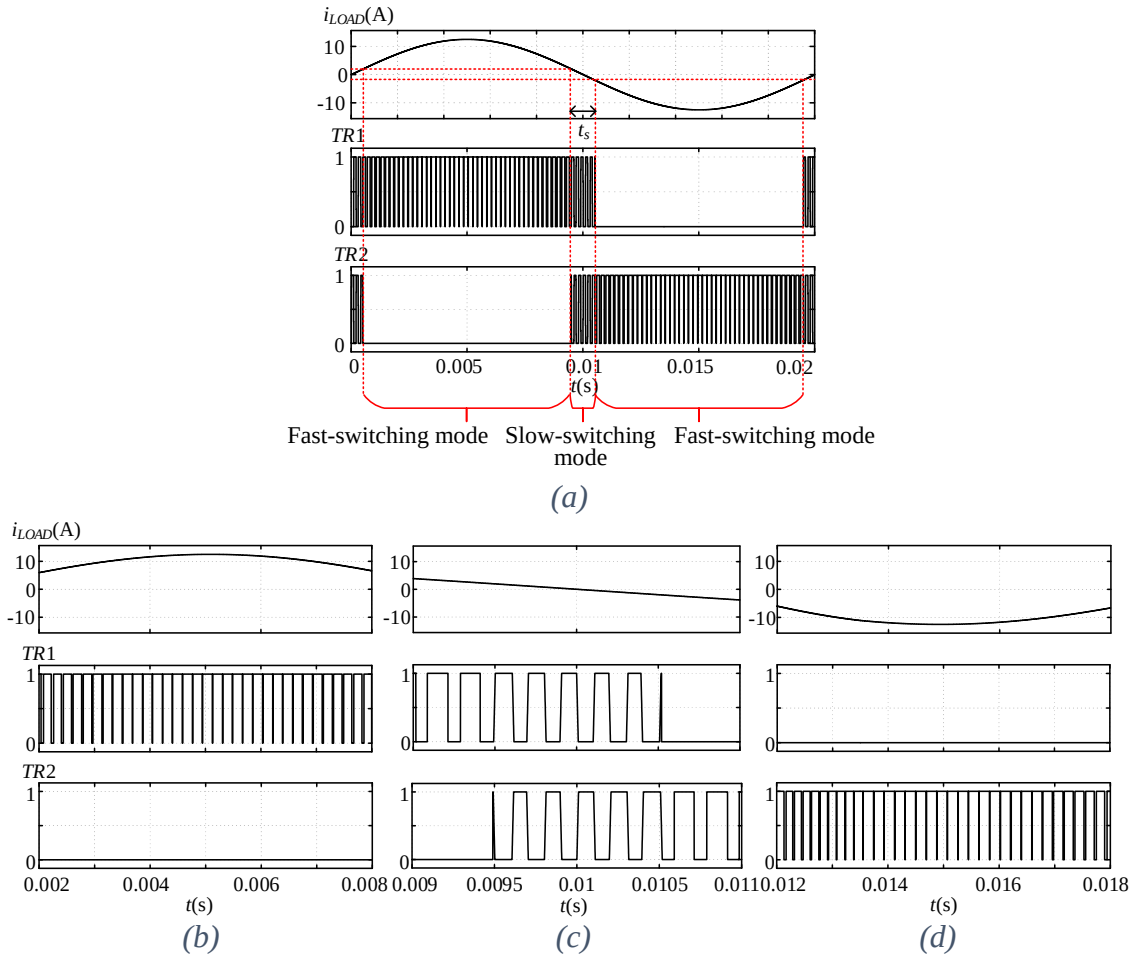



*Figure 4.10 Simulation results of using dual-mode switching technique in an inverter. (a) Overall $i_{LOAD}$ and gate signals; (b) fast-switching mode: TR1 is fast switching and TR2 is held off; (c) slow-switching mode: both TR1 and TR2 are slow switching; (d) fast-switching mode: TR2 is fast switching and TR1 is held off.*

# 4.4. Experimental hardware

## 4.4.1. Power circuit and device selection

Figure 4.11 shows the circuit configuration used for experimentation, Figure 4.12 shows the experimental hardware, and details of the power components are given in Table 4.2. Although most intended applications such as machine drives are of a three-phase type, a single inverter-leg was used for experimental purposes, and one end of the load is connected to Point 'b' at the supply's centre-point. The total supply voltage $V_{dc}$ (equal to $V_{dc1}$ + $V_{dc2}$ in Figure 4.11) was 400 V. The power throughput was approximately 800 W

at a load current $i_L$ of 7.07 A. The switching frequency $f_{sw}$ was 20 kHz for all the experimentation. Whilst this frequency is relatively high for many typical machine-driven applications, it yields low perceived acoustic noise levels.

For a benchmark with the proposed technique, the circuit was also operated with high-quality IGBTs co-packaged with fast-recovery anti-parallel silicon diodes. These were used to replace the SJ MOSFETs, operating under the same conditions. Figure 4.13 shows the circuit configuration of the IGBT-based inverter-leg. Except for *TR*1 and *TR*2 being changed to IKW20N60TFKSA1, other components remain the same as in Table 4.2.

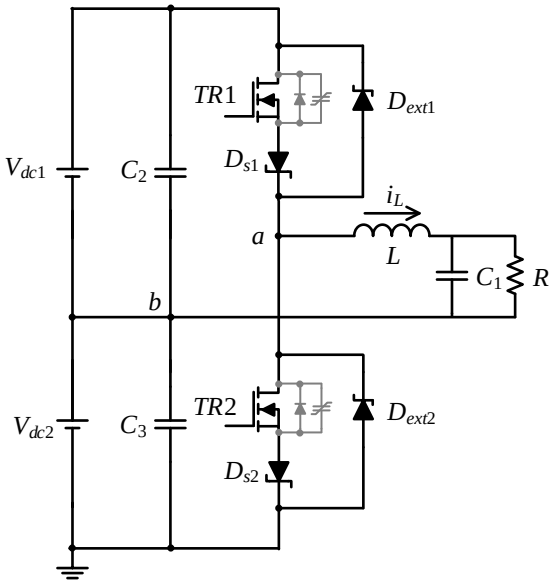



*Figure 4.11 SJ MOSFET-based single-phase inverter-leg.*

*Table 4.2 Device data of circuit in Figure 4.11.*

| | |
|---|---|
| *TR*1, 2 | IPW60R041P6FKSA1 |
| $D_{s1}$, $D_{s2}$ | MBR3060PT |
| $D_{ext1}$, $D_{ext2}$ | SCS220AEC |
| *L* | 1 mH (25 A) |
| $C_1$ | 50 µF (450 V) |
| $C_2$, $C_3$ | 470 µF (630 V) |
| *R* | A series-connected *RL* load of 0.8 kVA was supplied. The load was at a power factor *PF* close to one |

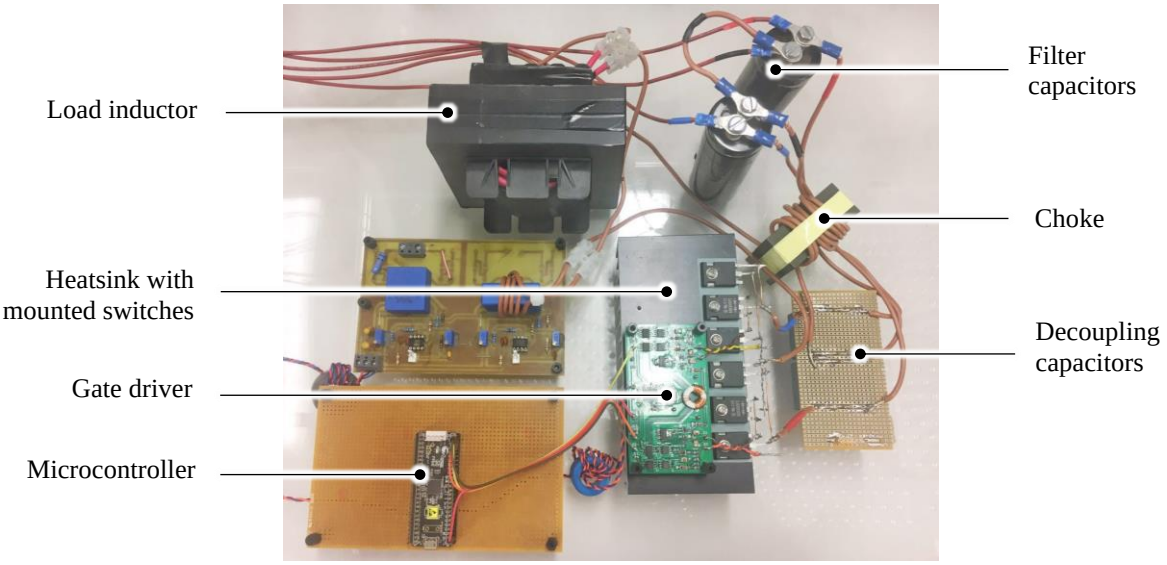



*Figure 4.12 Experimental hardware.*

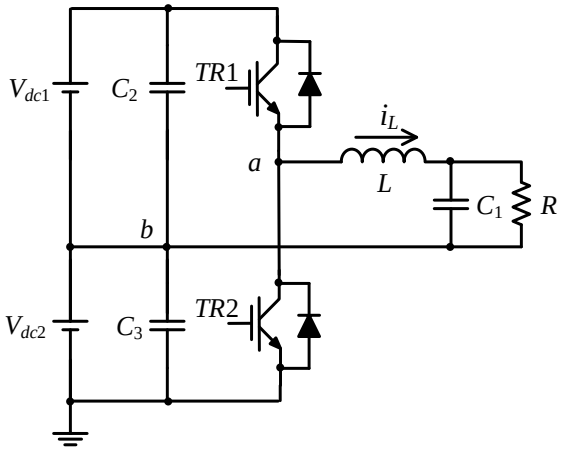



*Figure 4.13 IGBT-based single-phase inverter used for a benchmark with the proposed technique.*

## 4.4.2. Dual-mode gate driver design

Figure 4.14 shows the gate driver circuit in outline form. The input and enable signals, as shown in Figure 4.8, are transmitted to the driver circuit of each power device via HCPL-0302-000E optocouplers. Although the optocouplers used have a high output current capability, IXDN614 driver ICs were nonetheless included to increase this if required during experimentation. Signal diodes 1N4148TR are used to control the flow direction of the gate current.

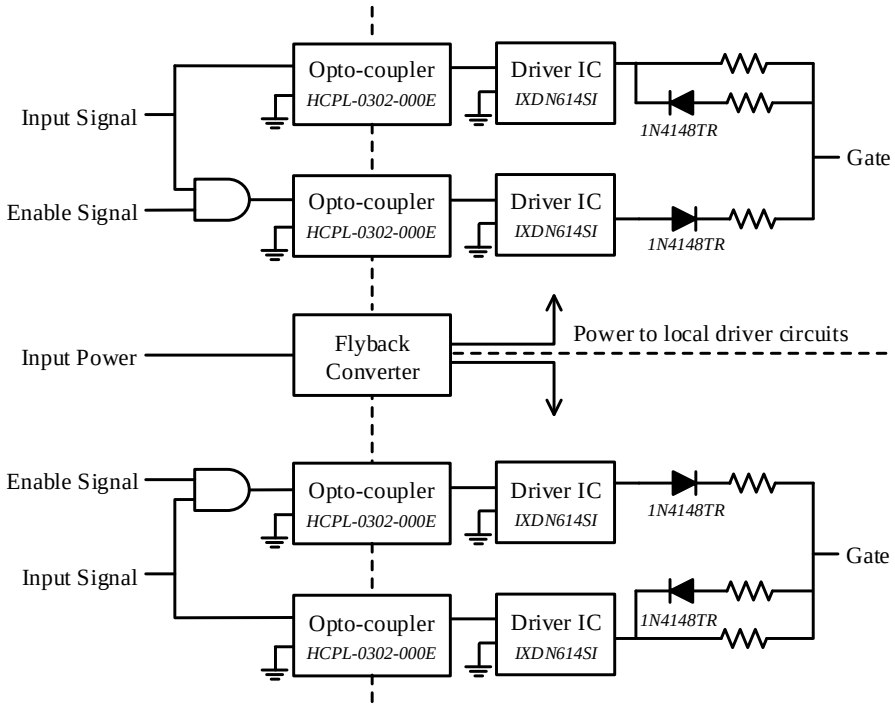



*Figure 4.14 Outline diagram of the dual-mode gate driver used to drive two power devices in an inverter-leg.*

Power for each driver circuit is transmitted by means of a flyback converter incorporating a small toroidal transformer with two secondary windings, and its topology is shown in Figure 4.15. The flyback transformer provides Galvanic isolation and its turns ratio was set at 6:39:39 in order to align with the power requirements of all devices onboard. In Figure 4.15, when the MOSFET on the primary side is on, the power from the DC power supply $V_{cc}$ stored in the magnetic inductance of the primary side. Since the diodes on the secondary side are reverse blocking at this moment, no current flows in the secondary side. When the MOSFET is off, the diodes are forward biased and the power transmitted from the primary side to the secondary side according to the magnetic induction. The voltage and current of the secondary side are defined by the turns ratio and duty factor.

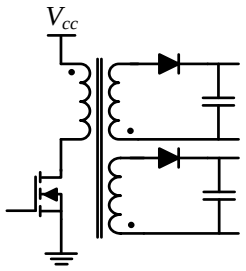



*Figure 4.15 Flyback converter onboard as the isolated power supply.*

The gate signal of the MOSFET in flyback converter is provided by a NOT-gate oscillator in Figure 4.16 (a). When the oscillator output is positive, the output of gate B is negative. The input of the gate A is also negative because the voltage across the capacitor cannot be changed abruptly. After a while, the resistor $R$ charges the left side of the capacitor to positive, then the input of the gate A is positive which leads to a negative output of the oscillator. Then the output of gate B is positive, and another oscillating process starts by the resistor discharges the capacitor. So each oscillating period is determined by the sum of RC charging and discharging time.

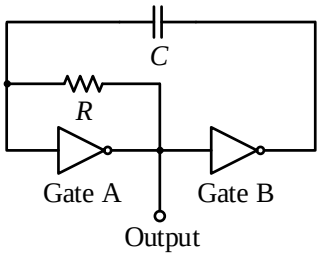
The RC charging time $tw_1 = RC$ and discharging time $tw_2 = 1.2RC$, which gives an oscillatory period $T$ equal to

$$T = tw_1 + tw_2 = 2.2RC. \tag{4.5}$$

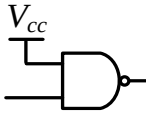
The value of the resistor and capacitor selected in the oscillator are $R$ = 1 kΩ, $C$ = 220 pF. Then oscillatory frequency $f$ is

$$f = \frac{1}{T} = \frac{1}{2.2RC} = \text{ 2 MHz.} \tag{4.6}$$

The two NAND gates of logic IC 74AC00SC function as NOT gates by connecting one of their pins to the $V_{cc}$ as shown in Figure 4.16 (b) and (c). The reason for this is the enable signals onboard can use the other two gates of the same IC thus the minimisation of the hardware is achieved.




(a)

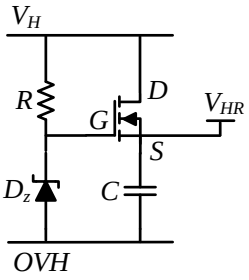



(b)

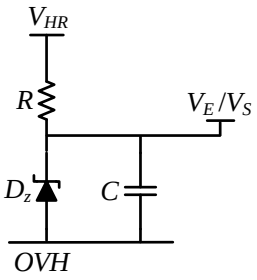
| Input | | Output |
|---|---|---|
| 1($V_{CC}$) | 1 | 0 |
| | 0 | 1 |

(c)

*Figure 4.16 NOT-gate oscillator and $V_{cc}$ connected NAND gate with its logic table.*




(a)




(b)

*Figure 4.17 Details of circuitry within high-side gate drivers. (a) Source follower circuit to provide regulated supply voltage. (b) Zener diode circuit used to split supply voltage in order that MOSFET can be driven with a negative off-state gate-source voltage.*

A source follower in Figure 4.17 (a) was used to regulate the output voltage from the flyback converter and provide a stable voltage $V_{HR}$ to the ICs. The MOSFET in the source follower module is in its saturation region. $V_{HR}$ is connected to the source of the MOSFET. The gate voltage $v_g$ is held at the Zener voltage $V_Z$ of Zener diode $D_z$.

When the source voltage $v_s$ is too low and the gate-source voltage $v_{gs}$ becomes larger than the threshold voltage $V_{th}$, the MOSFET will tend to turn on and thereby maintain the source voltage at $V_{HR}$. Then $v_s$ will tend to rise until $v_{gs}$ becomes lower than $V_{th}$ and the charging is cut off by the MOSFET. $V_{HR}$ is therefore equal to $V_Z$-$V_{th}$.

In order to avoid d$v$/d$t$-induced turn-on as explained in Section 2.2.4 of Chapter 2, a negative voltage is applied to the gate of the MOSFET with respect to its source when it

is off. For this purpose, $V_{HR}$ is split using the Zener diode circuit shown in Figure 4.17 (b). Figure 4.18 shows the dual-mode gate driver board. More details and testing results of the driver board are included in Appendix B.

*Figure 4.18 Dual-mode gate driver board.*

## 4.5. Losses calculation

As all the devices have been selected in Section 4.4.1, the total power dissipation can be estimated. The circuit's operating conditions are: $P$ = 800 W, $V_{dc}$ = 400 V, $f_{sw}$ = 20 kHz. The modulation index $m$ is set to 0.8. The peak fundamental output voltage $V_{peak}$ is given by

$$V_{peak} = \frac{m}{2} V_{dc} = \frac{0.8}{2} \times 400 = 160 \text{ V} \tag{4.7}$$

and the RMS output voltage $V_{o(RMS)}$ is given by

$$V_{o(RMS)} = \frac{V_{peak}}{\sqrt{2}} = 113 \text{ V}. \tag{4.8}$$

The output current $I_o$ is calculated from

$$I_o = \frac{P}{V_{o(RMS)}} = 7.08 \text{ A} \tag{4.9}$$

and $I_o$ has a peak value $I_{peak}$ of 10.01 A.

The forward voltage drop $V_{F(ext)}$ for $D_{ext}$ is estimated at 1.06 V from the manufacturer's datasheet. The power dissipation $P_{ext}$ in this device is given by

$$P_{ext} = V_{F(ext)} I_{peak} \left( \frac{1}{\pi} - \frac{V_{peak}}{2V_{dc}} \right). \quad (4.10)$$

Putting the data into (4.10) yields $P_{ext}$ = 1.26 W.

The forward voltage drop $V_{F(s)}$ for $D_s$ is estimated at 0.5 V from the manufacturer's datasheet. The power dissipation $P_s$ in this device is given by

$$P_s = V_{F(s)} I_{peak} \left( \frac{1}{\pi} + \frac{V_{peak}}{2V_{dc}} \right). \quad (4.11)$$

Putting the data into (4.11) yields $P_s$ = 2.62 W.

For the IPW60R041P6FKSA1 MOSFET, the nominal on-state resistance $R_{DS(on)}$ is 41 mΩ. The conduction losses $P_{cond}$ are given by

$$P_{cond} = R_{DS(on)} I_{peak}^2 \left( \frac{1}{4} + \frac{4V_{peak}}{3\pi V_{dc}} \right). \quad (4.12)$$

Putting the data into (4.12) yields $P_{cond}$ = 0.70 W.

Adding the results from (4.10), (4.11) and (4.12) yields a total power dissipation attributable to conduction losses of 4.68 W. We have not quantified the switching losses here, and these are assessed experimentally.

For the IKW20N60TFKSA1 IGBT, the on-state conduction voltage drop is estimated as $V_{CE(sat)}$ = 1.5 V from the manufacturer's datasheet. The conduction loss $P_{cond(IGBT)}$ in this device is given by

$$P_{cond(IGBT)} = V_{CE(sat)} I_{peak} \left( \frac{1}{\pi} + \frac{V_{peak}}{2V_{dc}} \right). \quad (4.13)$$

Putting the data into (4.13) yields $P_s$ = 7.86 W.

The anti-parallel diode conduction loss $P_{cond(diode)}$ in the IKW20N60TFKSA1 IGBT is estimated using

$$P_{cond(diode)} = V_F I_{peak} \left( \frac{1}{\pi} - \frac{V_{peak}}{2V_{dc}} \right) \tag{4.14}$$

where $V_F$ is the estimated forward voltage drop of the diode. $V_F$ was taken as 1.4 V from the manufacturer's datasheet. Putting the data into (4.14) yields $P_{cond(diode)}$ = 1.66 W. Adding $P_{cond(IGBT)}$ and $P_{cond(diode)}$ yields a total conduction loss of 9.52 W. If $k_{sw}$ is the switching energy dissipation per Ampere, then the switching loss $W_{sw}$ is given by

$$W_{sw} = \frac{2 f_{sw} k_{sw} I_{peak}}{\pi}. \tag{4.15}$$

$k_{sw}$ was estimated at 60 μJ/A, from the graphical data in the manufacturer's datasheet. Putting the data into (4.15) yields $W_{sw}$ = 7.65 W. Adding the conduction and switching losses gives an expected loss in the IGBT-based circuit of 17.17 W.

## 4.6. Software

The dual-mode technique uses the microcontroller to generates two complementary 20-kHz PWM output signals based on a 50-Hz fundamental-frequency sinusoidal modulation signal. According to a pre-set SSR value, the microcontroller controls the enable signal to select between the slow-switching mode and fast-switching mode according to different SSR values.

Several various microcontroller options were considered, and their key features are displayed in Table 4.3. Besides the consideration from the perspective of the function and cost, coding language, embedded development environment, access to the products, application supports are also under consideration. In the end, the PSoC 5LP from Cypress was selected for implementation.

*Table 4.3 Various microcontroller options and their key features*

| **Manufacturer** | Microchip Technology | Cypress<br>(part of Infineon now) | STMicroelectronics | Texas Instruments | Xilinx |
|---|---|---|---|---|---|
| **Part number** | dsPIC® 33<br>Digital Signal Controller | PSoC® 5LP<br>Programmable System-on-Chip | STM32F7 series<br>Very high performance MCU | TMS320F2837xD<br>C2000™ family MCU | Zynq®-7000 SoC family |
| **Architecture** | 16-bit dsPIC® DSC core | 32-bit ARM Cortex-M3 core | 32-bit ARM Cortex-M7 core | Dual TMS320C28x 32-bit cores | Single/Dual-core ARM Cortex-A9 MPCore™ |
| **Frequency** | 70 MHz | 80 MHz | 216 MHz | 200 MHz | up to 1GHz |
| **Speed** | 70 MIPS | 100 MIPS | 462 DMIPS | 800 MIPS | 3300 MIPS |
| **Cost*** | Chip scale<br>£1.48-7.69 | Chip scale<br>£7.81-14.11<br><br>Prototyping kit<br>£12.52<br><br>Development kit<br>£77.19 | Chip scale<br>£9.72-10.97<br><br>STM32F746G-DISCO-Development Board<br>£46.02 | C2000 Delfino MCU F28379D LaunchPad™ development kit<br>£34.79<br><br>C2000 Delfino MCU experimenter kit<br>£216.00 | Xilinx Zynq-7000 SoC ZC702 Evaluation Kit<br>$895<br><br>Xilinx Zynq-7000 SoC ZC706 Evaluation Kit<br>$2495 |
| **Highlights** | The performance of a DSP with the simplicity of an MCU in a single-chip. | Programable routing and interconnect. Configurable analogue and digital peripherals enable custom functions. | Implementing a single floating point unit (SFPU) precision, a full set of DSP instructions and a memory protection unit (MPU) to enhance application security. | An independent 32-bit floating-point processor CLA free the main CPU during service time-critical functions. | Integrating the software programmability of an ARM-based processor with the hardware programmability of an FPGA. |
| **Applications** | Motor drive & control; Automotive; Power management; Communications & networking; Consumer electronics; Computers & Peripherals | | | Advanced closed-loop control applications. | Multi-axis motor control; Machine vision; Programmable logic controller |

* The cost is based on the prices on Farnell and manufacturers' website in 2020.

The microcontroller used in the experimental rig, shown in the bottom-left corner of Figure 4.12, is a CYPRESS PSoC 5LP, CY8C5888LTI-LP097 68-QFN type. Compared with other microcontrollers, the PSoC 5LP from CYPRESS is very well integrated for its low-cost programmer and design flexibility. This ARM Cortex-M3 CPU based SoC combines high-precision and programmable analogue and digital peripherals [116]. The combination of configurable analogue and digital peripherals circuitry, which are represented by a block called component in microcontroller's development software *PSoC Creator*, is the basis of the PSoC platform. All the components in *PSoC Creator* can either be found in the pre-built library or customised.

*Figure 4.19 CY8CKIT-059 PSoC® 5LP prototyping kit with onboard programmer and debugger* [116].

Figure 4.20 shows the TopDesign in the *PSoC Creator* which reveals the overall design for peripherals circuitry. The combination of the code and the TopDesign in the PSoC realises the required function. The PWM component in TopDesign is used to generate the PWM waveform, which has 12 MHz Clock. The resolution of PWM components is 16-bit and the Period is set to 599 which equals to 50 µs. The dead band is set to 12 clock cycles which is 1 µs. By changing the compare value of the PWM component according to the code, two complementary PWM outputs are generated. The enable single is controlled by the combination of the code and the logic gate circuitry in the TopDesign. The code for the PSoC can be found in Appendix C.

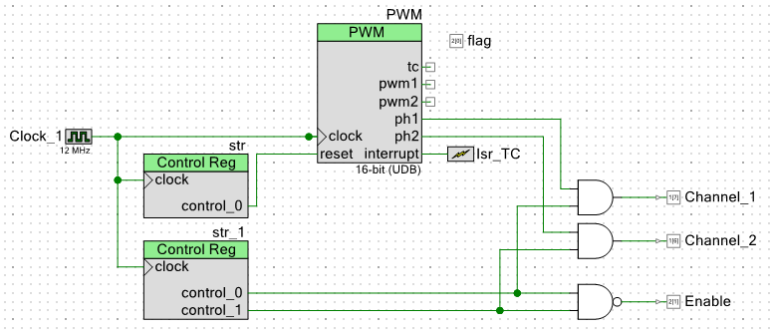



*Figure 4.20 TopDesign in PSoC Creator.*

# 4.7. Experimental results

## 4.7.1. Preliminary experimental results

Preliminary experimental results are obtained when using the SJ MOSFET inverter-leg in DC mode as in Figure 4.21. All the devices are the same as in Table 4.2 except for the resistive load *R*. The load *R* is three aluminium-clad power resistors of 10 Ω, 2.2 Ω and 1 Ω in series, which gives a resulting resistance of 13.2 Ω.

Figure 4.22 shows initial waveforms, where the circuitry is supplied from a reduced voltage of 60 V DC and both the slow-switching technique and the *TR*2 being held off improve the overshoot current and overshoot voltage. The worst situation is when fast switching both *TR*1 and *TR*2. The overshoot voltage reaches 196 V, which is more than three times the DC supply voltage.

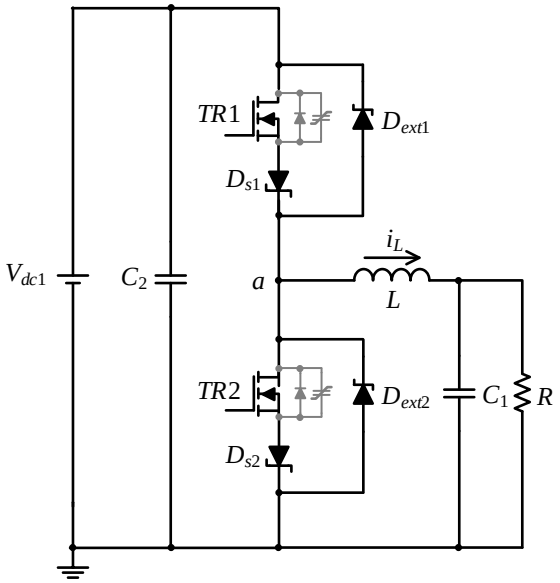



*Figure 4.21 Using SJ MOSFET inverter-leg in DC mode.*

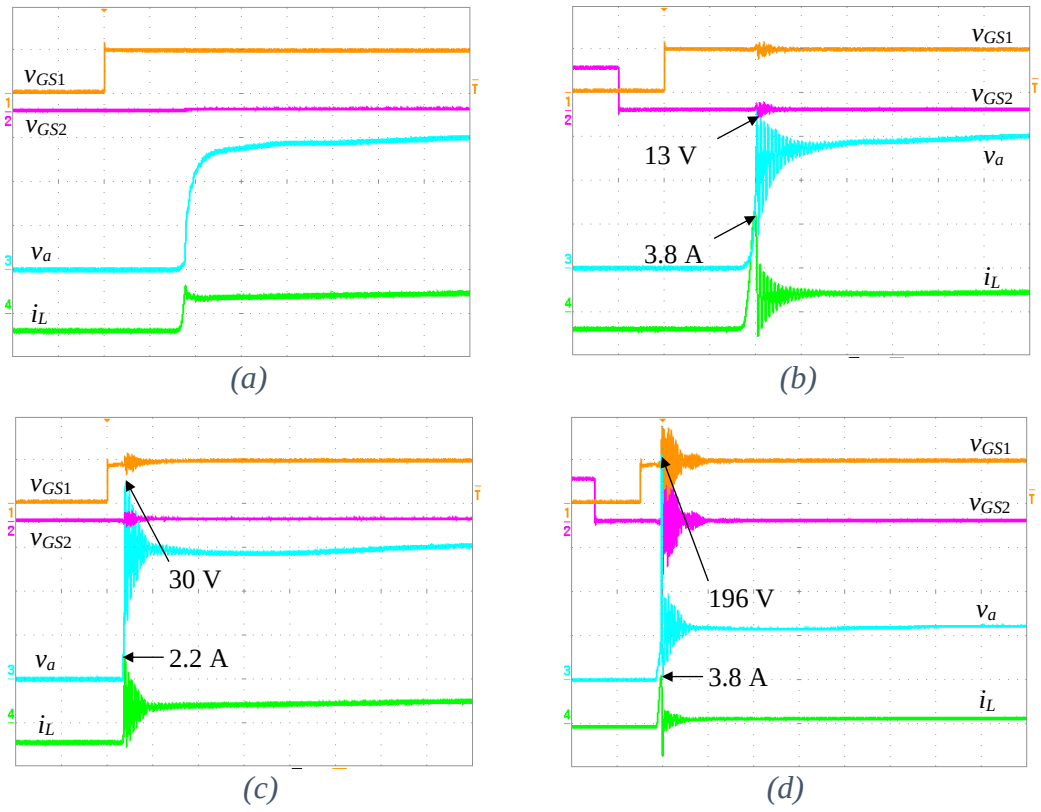



*Figure 4.22 Experimental results of using SJ MOSFET inverter-leg in DC mode. (a) Slow switching for TR1 and TR2 is held off; (b) slow switching for both TR1 and TR2; (c) fast switching for TR1 and TR2 is held off; (d) fast switching for both TR1 and TR2. Scales are $v_{GS1}$ = 5 V/div., $v_{GS2}$ = 5 V/div., $v_a$ = 20 V/div., $i_L$ = 2 A/div. for (a), (b), (c). $v_{GS1}$ = 5 V/div., $v_{GS2}$ = 5 V/div., $v_a$ = 50 V/div., $i_L$ = 10 A/div. for (d). Time scale = 1 µs/div for all.*

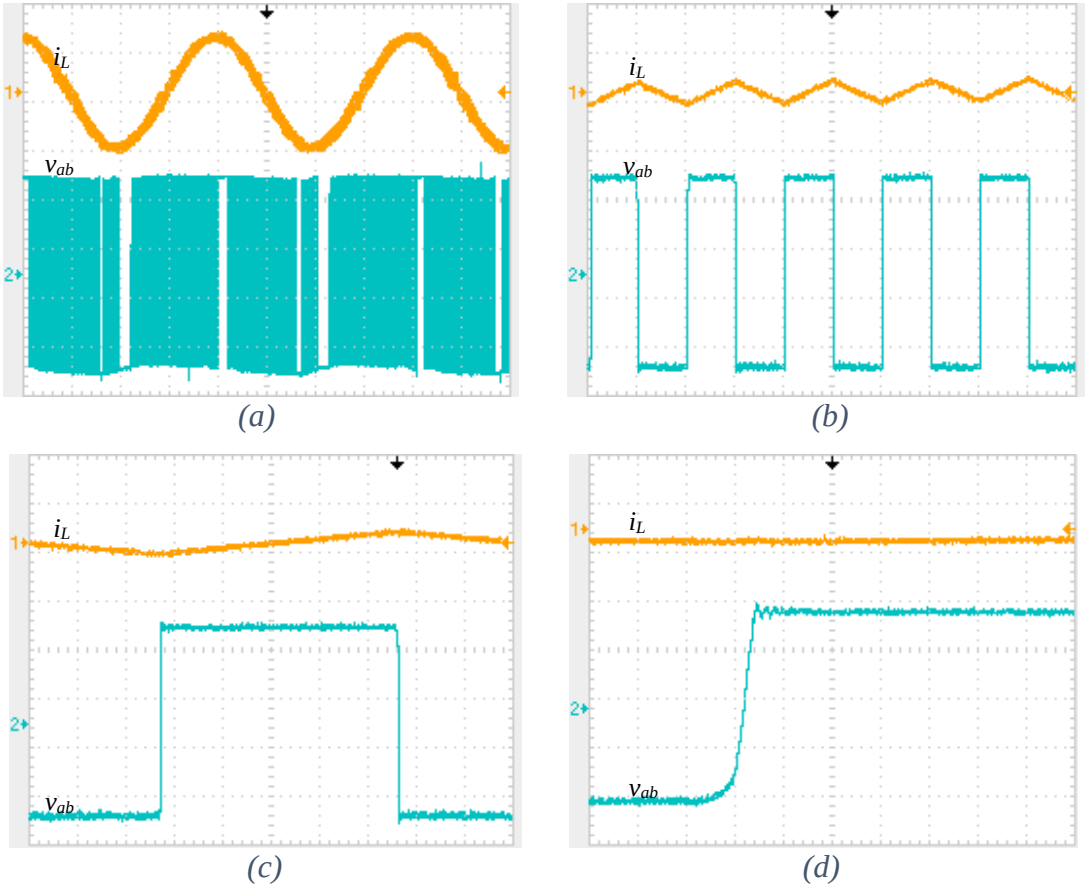
### 4.7.2. Results with proposed technique

Figure 4.23 shows waveforms from the circuit in Figure 4.11 when SSR = 0.1. Figure 4.23 (a) shows base-frequency waveforms of $i_L$ and $v_{ab}$.

In Figure 4.23 (b), $i_L$ is transitioning through zero twice per switching cycle, so both *TR*1 and *TR*2 are operating in the synchronous conduction mode where soft switching naturally occurs [58]. The slow-switching mode is nonetheless needed at low $i_L$ magnitudes to allow operation in the continuous conduction mode with bipolar switching prior to enabling unipolar switching. Figure 4.23 (c), (d), (e) show expanded waveforms of this operating mode, during which the rise- and fall-times of $v_{ab}$ are measured as 103 ns and 132 ns respectively.

In Figure 4.23 (f), $i_L$ is positive and above the threshold value at which unipolar switching is enabled, so *TR*1 is fast switching and *TR*2 is held off. Figure 4.23 (g) shows expanded waveforms in this mode. A negative-going overshoot voltage of approximately 52 V appears in $v_{ab}$ when *TR*1 turns off. When *TR*1 is off, $D_{ext2}$ is in its freewheeling period. On the positive-going transition of $v_{ab}$, the overshoot voltage reaches approximately 40 V.

In Figure 4.23 (h), $i_L$ is negative and below the threshold value at which unipolar switching is enabled, so *TR*2 is fast switching and *TR*1 is held off. Figure 4.23 (i) shows expanded waveforms in this mode. A positive-going overshoot voltage of approximately 40 V appears in $v_{ab}$ when *TR*2 turns off. When *TR*2 is off $D_{ext1}$ is in its freewheeling period. On the negative-going transition of $v_{ab}$, the overshoot voltage reaches approximately 45 V. The rise time and the fall time of $v_{ab}$ are 22.7 ns and 41.5 ns respectively.



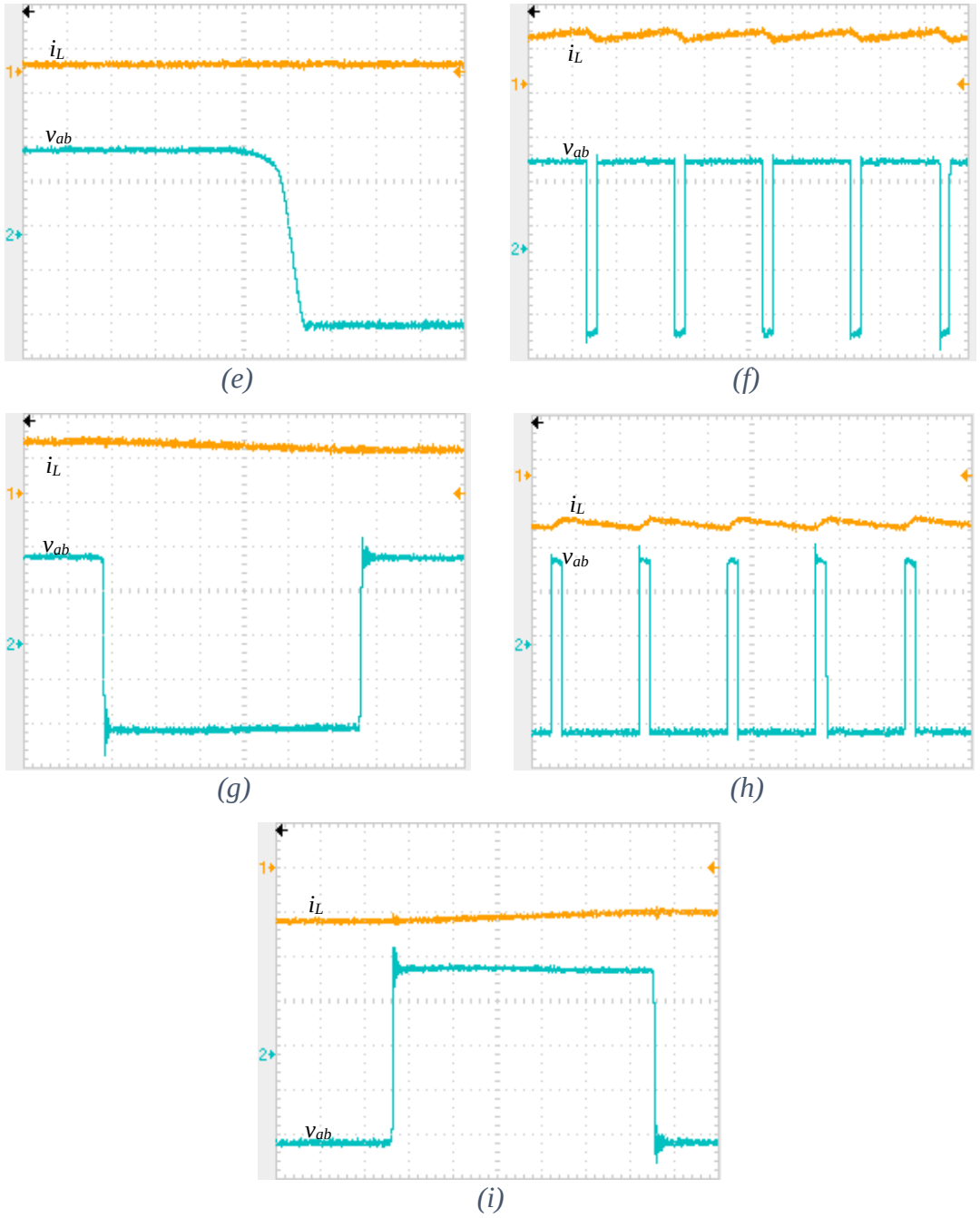



*Figure 4.23 Waveforms of $i_L$ and $v_{ab}$. Scales are $i_L$ = 10 A/div., $v_{ab}$ = 100 V/div. for all. Time scales are 5 ms/div for (a), 25 µs/div for (b), (f), (h), 5 µs/div for (c), 250 ns/div for (d), (e), 1 µs/div for (g), (i).*

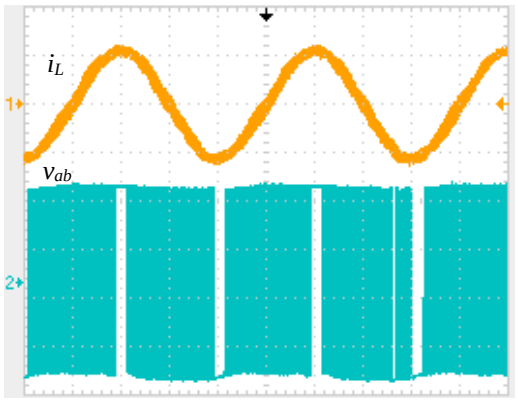
### 4.7.3. Results with IGBTs

Figure 4.13 shows the circuit in which the SJ MOSFETs and associated diodes in Figure 4.11 were replaced by IGBTs co-packaged with fast recovery anti-parallel diodes. This

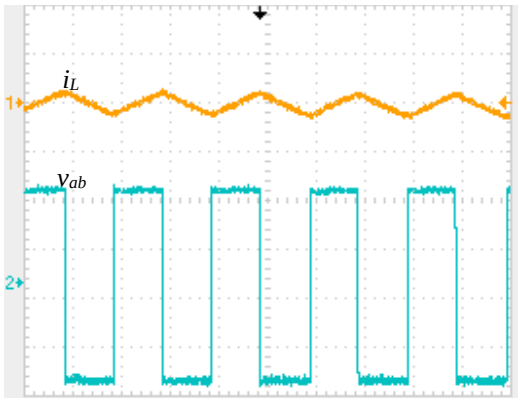
circuit was operated under the same conditions as the circuit in Figure 4.11. The IGBTs were driven with standard complementary fast-switching gate signals at 20 kHz.

Figure 4.24 shows waveforms from the circuit in Figure 4.13. Figure 4.24 (a) shows base-frequency waveforms of $i_L$ and $v_{ab}$. In Figure 4.24 (b), $i_L$ is transitioning through zero twice per switching cycle. Figure 4.24 (c), (d) shows expanded waveforms of (b).

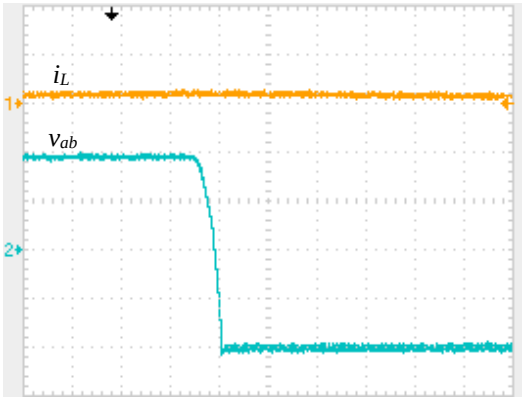
In Figure 4.24 (e), $i_L$ reaches its highest peak. Figure 4.24 (f) shows expended waveforms of (e) and the rise time and the fall time of $v_{ab}$ are 88.3 ns and 73.1 ns respectively. In Figure 4.24 (g), $i_L$ reaches its lowest peak. Figure 4.24 (h) shows expended waveforms of (g) and the rise-time and fall-time of $v_{ab}$ are 81.7 ns and 76.0 ns respectively.



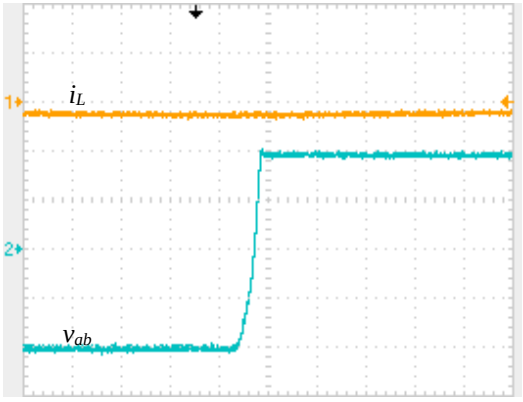

*(a)*




*(b)*




*(c)*




*(d)*

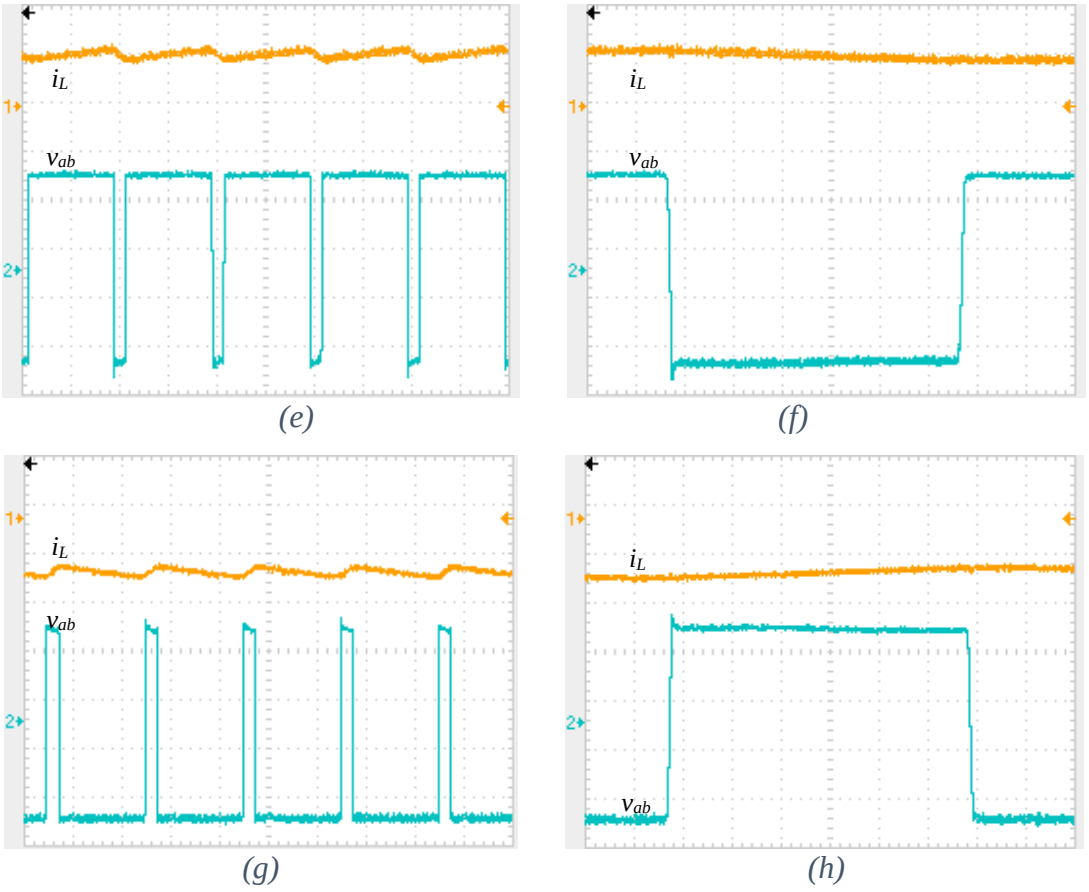



*Figure 4.24 Waveforms of $i_L$ and $v_{ab}$. Scales are $i_L$ = 10 A/div., $v_{ab}$ = 100 V/div. for all. Time scales are 5 ms/div for (a), 25 µs/div for (b), (e), (g), 500 ns/div for (c), (d), 1 µs/div for (f), (h).*

### 4.7.4. Thermal superposition

In order to estimate the efficiencies of the circuits in Figure 4.11 and Figure 4.13, thermal superposition was used to measure the power dissipated by the power devices on the heatsink [3]. This technique is particularly suited for high-efficiency measurements, such as those required here. The main steps are as follows:

1. A DC current is passed through one or more of the power devices on the heatsink and the voltage across the devices is measured. As the current and voltage are DC quantities, the power dissipation $P_d$ in the devices can be accurately determined as

$$P_d = V_{dc} \cdot I_{dc}. \tag{4.16}$$

2. The temperature rise $D_{temp}$ of the heatsink above ambient is recorded when it has reached its thermal steady-state. The thermal resistance $R_{\theta hsa}$ of the heatsink to ambient is then calculated using

$$R_{\theta hsa} = \frac{D_{temp}}{P_d}. \tag{4.17}$$

3. The circuit under test is then run on the heatsink and the temperature rise above the ambient is recorded when it has reached its thermal steady-state value. The estimated power dissipation $P_{est}$ is given by

$$P_{est} = \frac{D_{temp}}{R_{\theta hsa}}. \tag{4.18}$$

As $P_{est}$ has now been obtained, the percentage efficiency $\eta$ (%) of the circuit can be calculated from

$$\eta\,(\%) = \frac{P_{in} - P_{est}}{P_{in}} \times 100 \tag{4.19}$$

where $P_{in}$ is the input power drawn by the circuit under test.

Using the thermal superposition technique, the $R_{\theta hsa}$ of the heatsink is determined prior to operating the experimental circuits. The heatsink's $R_{\theta hsa}$ is selected as such that $D_{temp}$ was typically 20 °C during measurements, which gives a reasonable temperature swing for the purpose of measurement accuracy. Therefore, the selected heatsink was experimentally evaluated to make sure it gave a reasonable temperature rise for measurement purposes, whilst keeping the power devices cool.

The evaluated heatsink has a volume of 16.0×7.4×3.9 $cm^3$ with 16 straight fins run the entire length of it. It is made of aluminium alloy with matt-black anodised surfaces for the purpose of radiating more efficiently than shiny bare metal. All the devices mounted onto the heatsink are in TO-247 packages, and six M3 screw holes were drilled and tapped evenly along it to allow for fastening the devices as shown in Figure 4.11. Thermal interface sheeting was located between the devices and the heatsink to provide electrical isolation whilst retaining good thermal conductivity.

In Figure 4.11, when there is no gate voltage applied to SJ MOSFETs, they will block the input voltage and thus no current will flow across the inverter-leg. In order to have current go through the inverter bridge-leg and consequently dissipate power through the heatsink, a power supply was connected to the inverter bridge-leg in the reverse direction, where the external diodes provide the current path. The power supply was run as in the constant-current mod, and the DC voltage $V_{dc}$ and DC current $I_{dc}$ across the bridge-leg were measured as 2.384 V and 9.85 A. Table 4.4 shows the temperature measurements over time where $D_{temp}$ is the temperature rise of the heatsink above ambient and $D_t$ is the time in minutes. The tool used to measure temperature is the thermal camera from FLIR. The data of $D_{temp}$ and $D_t$ were drawn in Figure 4.25 to help judging the thermal time constant of the heatsink, and how long it takes to approach the thermal steady-state.

*Table 4.4 Temperature measurements for the evaluated heatsink.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 45.9 | 24.1 | 21.8 |
| 2 | 10 | 54.3 | 25.3 | 29 |
| 3 | 20 | 58.7 | 25.3 | 33.4 |
| 4 | 30 | 61.2 | 25.1 | 36.1 |
| 5 | 40 | 62.3 | 25.5 | 36.8 |
| 6 | 50 | 63.1 | 25.6 | 37.5 |
| 7 | 60 | 63.3 | 25.7 | 37.6 |

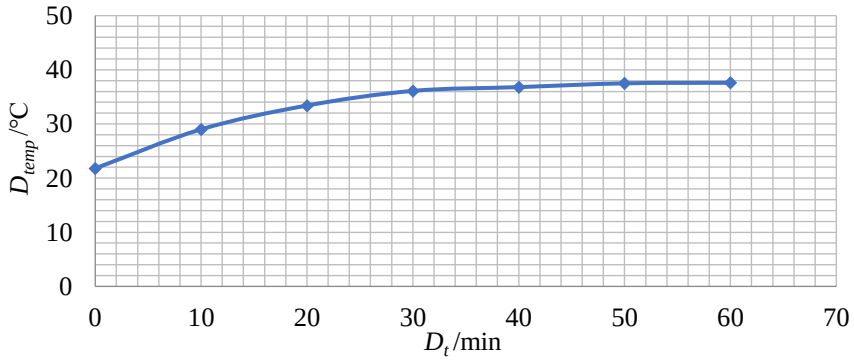



*Figure 4.25 Temperature rise against time for the evaluated heatsink.*

The temperature rise $D_{temp}$ is calculated as 37.55 ℃ by averaging the last three measurements after heatsink reaches its thermal steady-state. Because the power dissipation $P_d$ in the devices can be accurately determined as

$$P_d = V_{dc} \cdot I_{dc} = 23.48 \text{ W}. \tag{4.20}$$

The thermal resistance $R_{\theta hsa}$ of the heatsink to ambient is then calculated using

$$R_{\theta hsa} = \frac{D_{temp}}{P_d} = 1.60 \text{ ℃/W}. \tag{4.21}$$

So, according to the design of the circuit in Section 4.4.1, the evaluated heatsink is suitable for use in the experiments to provide good accuracy in thermal measurements. Its measured thermal resistance of 1.60 ℃/W was used to subsequently determine $P_{est}$.

After evaluating the heatsink, the circuit under test is then run and the temperature rise above the ambient is recorded when heatsink reaches its thermal steady-state. Table 4.5 shows the temperature measurements over time when the inverter-leg is running with the SSR = 0.1. The data of $D_{temp}$ and $D_t$ were drawn in Figure 4.26 to help with the judgement of the thermal steady-state. Figure 4.27 shows the thermal images of heatsink's thermal steady-state.

*Table 4.5 Temperature measurements when SSR = 0.1*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 34.3 | 21.1 | 13.2 |
| 2 | 10 | 35.5 | 24.1 | 11.4 |
| 3 | 20 | 39 | 24.7 | 14.3 |
| 4 | 30 | 40.7 | 24.7 | 16 |
| 5 | 40 | 41.7 | 24.9 | 16.8 |
| 6 | 50 | 42.2 | 25.4 | 16.8 |
| 7 | 60 | 42.9 | 25.7 | 17.2 |
| 8 | 70 | 43.1 | 25.3 | 17.8 |
| 9 | 75 | 43.3 | 25.3 | 18 |
| 10 | 80 | 42.8 | 24.7 | 18.1 |
| 11 | 85 | 43.7 | 25.5 | 18.2 |
| 12 | 90 | 43.1 | 25.4 | 17.7 |

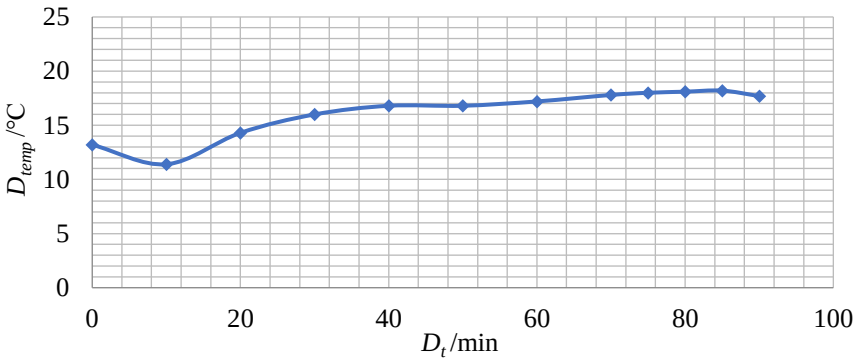



*Figure 4.26 Temperature rise against time when SSR = 0.1.*

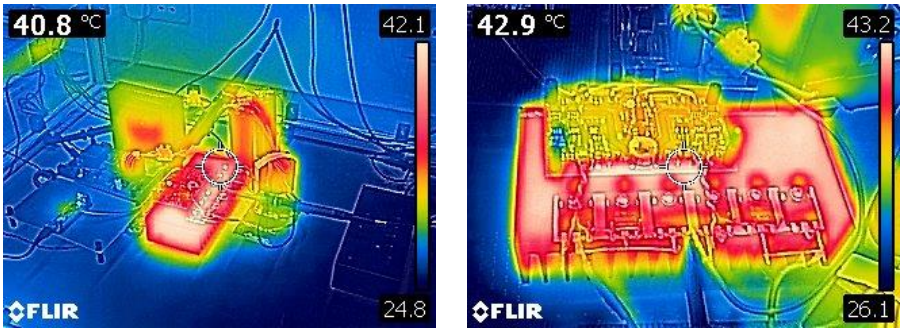



*Figure 4.27 Thermal images of SJ MOSFET-based single-phase inverter when SSR = 0.1.*

The temperature rise $D_{temp}$ is calculated as 18.00 °C by averaging the last three measurements after heatsink reaches its thermal steady-state. The estimated power dissipation $P_{est}$ is given by

$$P_{est} = \frac{D_{temp}}{R_{\theta hsa}} = 11.25 \text{ W}. \tag{4.22}$$

The input voltage $V_{in}$ and current $I_{in}$ drawn by the circuit under test are 400 V and 2.13 A, so the input power $P_{in}$ is

$$P_d = V_{in} \cdot I_{in} = 853 \text{ W}. \tag{4.23}$$

As $P_{est}$ and $P_{in}$ have now been obtained, the percentage efficiency $\eta$ (%) of the circuit can be calculated from

$$\eta\,(\%) = \frac{P_{in} - P_{est}}{P_{in}} \times 100 \;=\; 98.68. \tag{4.24}$$

Similar to the previous scenario of inverter-leg operating with SSR = 0.1, temperature measurements are recorded when inverter-leg is running with different SSR and complementary soft switching. The input voltage $V_{in}$ and input current $I_{in}$ drawn by the circuit under each scenario are also recorded. All the corresponding data are shown in Appendix A. The power dissipation $P_{est}$ and the efficiency are calculated according to Equation (4.18) and Equation (4.19). Table 4.6 summarises the results.

### 4.7.5. Total harmonic distortion

In order to experimentally assess the potential effects on waveform fidelity of introducing the proposed technique, the total harmonic distortion (THD) in the load current was evaluated. This was repeated for the benchmark IGBT-based circuit. Table 4.6 gives results. The THD was obtained by analysing the downloaded oscilloscope waveform data with the MATLAB Powergui FFT Analysis Tool. In the Analysis Tool Preferences, the fundamental frequency of the analysed signal is 50 Hz and the maximum frequency evaluated by the FFT analysis is 15 kHz so that higher harmonics than switching frequency 20 kHz will be easily filtered.

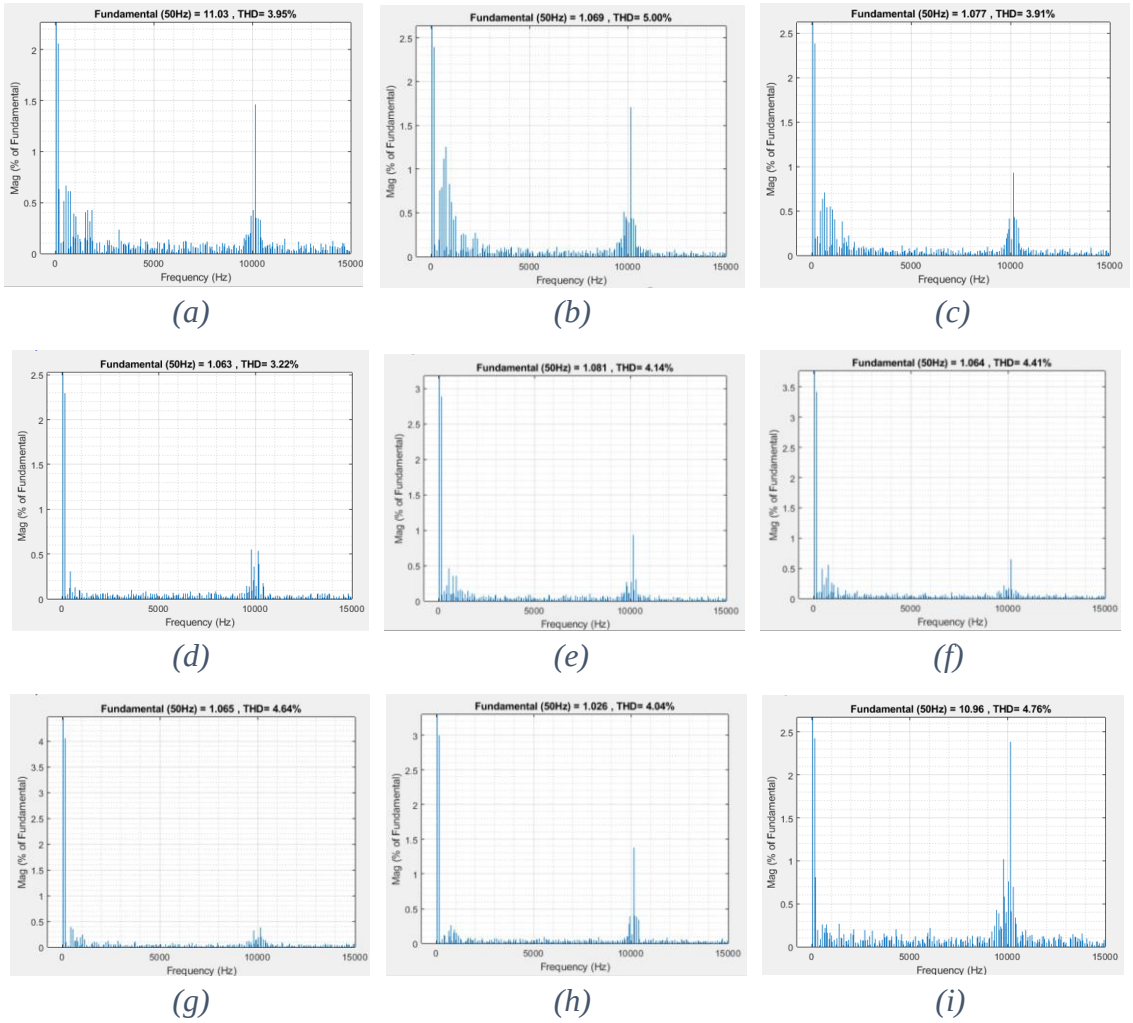
Select the maximum frequency for THD computation equals to the maximum frequency in FFT analysis. The percentage THD in the input signal was then calculated using:

$$\text{THD}\ (\%) = \frac{\sqrt{\sum_{i=2}^{n} M_i^2}}{M_1} \times 100 \tag{4.25}$$

where $M_i$ is the root mean square (RMS) value of the harmonic magnitude corresponding to the $i^{th}$ harmonic order.

Figure 4.28 shows the harmonics in the output current of the SJ MOSFET inverter-leg operating with different SSR and IGBT based inverter-leg. The highest magnitude of harmonics is 50 Hz component, which is the basic frequency of output current. However, there is also a noticeable 10 kHz harmonic component occurred in every circuit, regards of devices and controlling SSR, which could be caused by the ringing of the parasitic elements in the hardware loop. The importance of Figure 4.28 is it shows that the there is

no major difference in output THD between SJ MOSFET based inverter-leg with dual-mode switching and IGBT based inverter-leg, as long as the consistency has been satisfied in measurements.




*(a)* *(b)* *(c)*

*(d)* *(e)* *(f)*

*(g)* *(h)* *(i)*

*Figure 4.28 Harmonics in output current of SJ MOSFET-based inverter-leg switching at 20kHz when (a) SSR = 0.1, (b) SSR = 0.2, (c) SSR = 0.3, (d) SSR = 0.4, (e) SSR = 0.5, (f) SSR = 0.6, (g) SSR = 0.7, (h) SSR = 1; (i) Harmonics in output current of IGBT-based inverter-leg switching at 20kHz.*

*Table 4.6 Experimental Results with inverter-leg switching at 20 kHz.*

| **Circuit configuration** | **SSR ratio** | **$D_{temp}$ /°C** | **Input voltage /V** | **Input current /A** | **Input power /W** | **Power dissipation /W** | **Estimated efficiency /%** | **THD /%** |
|---|---|---|---|---|---|---|---|---|
| SJ MOSFETs in proposed circuit in Figure 4.11, with proposed dual-mode switching technique implemented. | 0.1 | 18.00 | 400 | 2.13 | 852 | 11.26 | 98.68 | 3.95 |
| | 0.2 | 17.57 | 400 | 2.06 | 824 | 10.98 | 98.67 | 5.00 |
| | 0.3 | 17.87 | 400 | 2.04 | 816 | 11.18 | 98.63 | 3.91 |
| | 0.4 | 17.27 | 400 | 2.01 | 804 | 10.80 | 98.66 | 3.22 |
| | 0.5 | 18.13 | 400 | 2.02 | 808 | 11.34 | 98.60 | 4.14 |
| | 0.6 | 19.55 | 400 | 2.01 | 804 | 12.23 | 98.48 | 4.41 |
| | 0.7 | 20.53 | 400 | 1.98 | 792 | 12.84 | 98.38 | 4.64 |
| SJ MOSFETs in circuit in Figure 4.11, with complementary slow switching implemented under all conditions. | 1 | 27.27 | 400 | 1.88 | 752 | 17.05 | 97.73 | 4.04 |
| IGBTs in circuit in Figure 4.13 with standard complementary fast switching implemented. | — | 33.93 | 400 | 2.13 | 852 | 21.22 | 97.51 | 4.76 |

Figure 4.29 shows the efficiency results from Table 4.6 presented in a bar chart format. When the dual-mode technique is applied to the SJ MOSFET-based inverter-leg, the efficiency shows an increasing trend as the SSR ratio is reduced. The highest efficiency reaches approximately 98.7 % as the SSR ratio approaches 0.1, while the efficiency of the IGBT-based inverter-leg is only 97.5 %.

Figure 4.30 shows the THD analysis results from Table 4.6 presented in a bar chart format. With the maximum frequency for THD computation set at 15 kHz, the THD in the output current when using SJ MOSFET-based inverter-leg at an SSR ratio of 0.1 is 3.95 %. The THD in the output current when using the IGBT-based inverter-leg is 4.76 %. Applying the dual-mode technique can improve efficiency while exhibiting a similar output current quality.

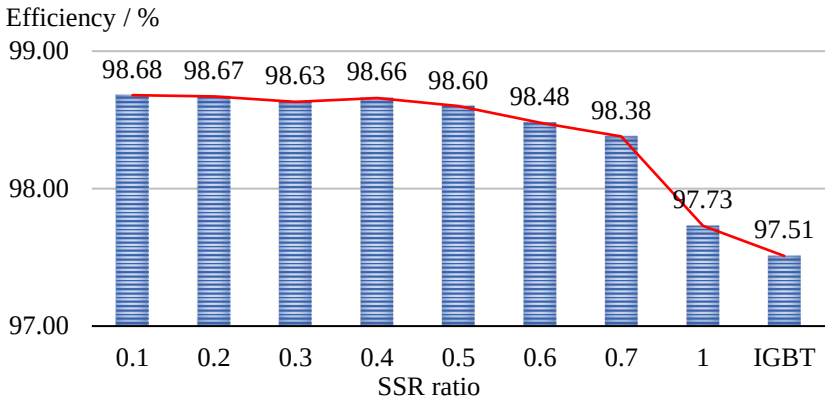



*Figure 4.29 Efficiency results.*

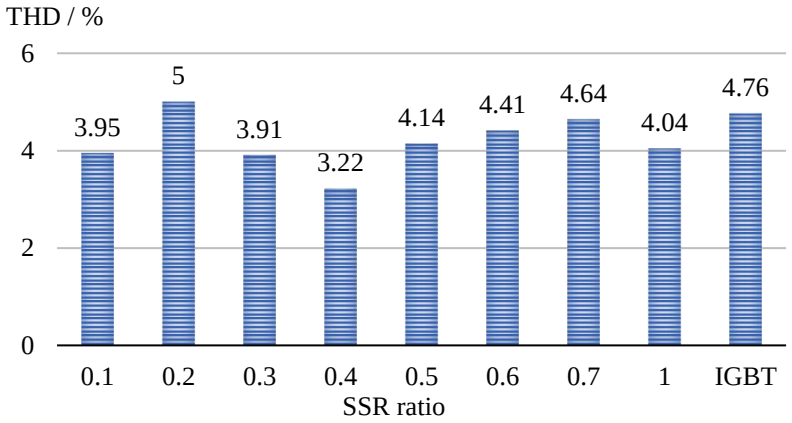



*Figure 4.30 THD results.*

## 4.8. Discussion

The following points are noted.

- The circuitry is intended for use in machine drive applications, and the quoted efficiencies therefore do not account for any choke losses.
- The inverter-leg was operated under open-loop control with gate drive signals generated by the microcontroller. A higher THD is therefore expected than if the circuit were to be operated under closed-loop current control, as is normally the case in typical applications such as machine control.
- The load was at a power factor close to one. No current sensing was incorporated into the proposed scheme. With variable power factors, current sensing would be required to inform the control circuitry which of the three modes, as defined in Figure 4.10, the circuitry should be operating in.
- Silicon Schottky diodes were used in locations $D_{s1}$ and $D_{s2}$. Whilst this is a simple arrangement, and was used for experimentation, losses are nonetheless incurred by the forward voltage drop of the diode when in conduction. An alternative solution is to replace the diodes with low-voltage anti-series MOSFETs [58]. These MOSFETs can readily be controlled such that they conduct in reverse as synchronous rectifiers when a drain current is flowing into the main MOSFETs, thereby further reducing losses. Further discussion will be included in Chapter 5.
- The dual-mode switching technique evaluated here is based on the half-bridge inverter, which is easily extendable to a full-bridge or a three-phase inverter. With the same input power and modulation, the output voltage of the full-bridge inverter is double than half-bridge inverter. And also, the three-time harmonics of the line-to-line voltage in a three-phase system will be counteracted.
- Dual-mode has achieved the high efficiency with minimum hardware. The only additional hardware on the gate driver are opto-couplers and drive ICs. The

driver IC here is just for the experimental reason to enhance the current ability. The opto-coupler has a cost of around £ 2.96.

- The improved efficiency will save cost on cooling. The different power dissipation between SJ MOSFET with dual-mode switching and IGBT is around 10 W in Table 4.6. Assume the heatsink has a temperature rise of 50 ℃, an additional heatsink of thermal resistance 5 ℃/W needs to be in use. This will introduce additional cost, no to mention using forced cooling to dissipate the extra power.
- Not using any magnetic components further saves the volume, this benefits for the shipping cost, cooling cost, maintenance cost as well.
- The resolution of the experimental data needs to be improved to further investigate the harmonic currents FFT results.

## 4.9. Conclusion

The highly non-linear output capacitance and reverse recovery characteristic of the super-junction MOSFET intrinsic diode have been addressed for the device when used in voltage source converters. A dual-mode switching control technique was proposed to address the disadvantages of the output capacitance. This technique operates in conjunction with intrinsic diode deactivation circuitry. The technique was demonstrated in an 800-W inverter-leg configuration operating from a 400-V DC supply voltage and switching at 20 kHz. The full-load efficiency reached approximately 98.7 %, and no forced cooling was needed.

# Chapter 5

# Alternative ancillary power device selection for super-junction MOSFET based inverter-leg configuration

## 5.1. Introduction

In Chapter 4, the dual-mode switching technique addressed the detrimental influence of the SJ MOSFET's output capacitance, and the technique functions in conjunction with intrinsic diode deactivation circuitry. This circuitry uses two ancillary power devices connected around each SJ MOSFET. Selection of these devices is addressed in this chapter, and practical experimental results for different device permutations are given. All device permutations are designed for a 1-kW inverter-leg operating with a 420-V DC rail voltage and switching at a series of frequencies from 15 kHz, 20 kHz, 25 kHz, 30 kHz up to 35 kHz. The full-load efficiency is evaluated for each scenario, and no forced cooling is needed.

## 5.2. Power device selection

In Chapter 4, SJ MOSFETs were used with low-voltage Si Schottky diodes as the series devices, and SiC Schottky diodes as the anti-parallel devices. This device permutation was used to deactivate the intrinsic diode of the SJ MOSFET, and functions with the dual-mode switching technique [117].

### 5.2.1. Synchronous rectification

As discussed in Section 2.2.3 of Chapter 2, when replacing the diodes with an active switching device such as a MOSFET, synchronous rectification can be realised which consequently leads to lower power losses and a higher efficiency due to reduced conduction losses. Based on this consideration, the series diode $D_s$ in Figure 4.1 can be replaced by a MOSFET. The MOSFET will be connected in anti-series with the main switch, and its gate signal is synchronous with that of the main switch. A low-voltage silicon MOSFET is selected for this purpose.

### 5.2.2. Si versus SiC devices

As discussed in Section 2.4.2 of Chapter 2, the SiC Schottky diode is well-suited to various applications and has excellent characteristics. But SiC devices normally cost more than their silicon counterparts, which makes all-silicon permutations advantageous in cost. Thus, Si PN fast recovery diode is selected to replace $D_{ext}$ in Figure 4.1, lowering the overall cost while maintaining good reverse recovery characteristics. Using a Si fast recovery PN diode as the anti-parallel device yields an all-silicon solution.

### 5.2.3. Device permutations

As an alternative device selection of Figure 4.1, low-voltage MOSFETs can be used as the anti-series devices [58], and Si fast recovery PN diodes can be used as anti-parallel devices. The candidate module permutations are shown in Figure 5.1 where each module can be used in the inverter-leg in Figure 4.1.

Specifically, Figure 5.1 (a) uses a low-voltage Si Schottky diode as the series device, and a Si fast recovery PN diode as the anti-parallel device. Figure 5.1 (b), the same as Figure 4.1, uses a low-voltage Si Schottky diode as the series device, and a SiC Schottky diode as the anti-parallel device. Figure 5.1 (c) uses a low-voltage Si MOSFET as the anti-series device, and a Si fast recovery PN diode as the anti-parallel device. Figure 5.1 (d) uses a low-voltage Si MOSFET as the anti-series device, and a SiC Schottky diode as the anti-parallel device.

All four device permutations are operated with the dual-mode switching technique. When using Module (a) or (b) in the inverter-leg, the SJ MOSFET is in series with a

low-voltage Si Schottky diode $D_s$. As shown in Figure 4.5, when the circuit is operating with a positive $i_{LOAD}$, only *TR*1 is being driven on and off. In the fast-switching mode, provided that *TR*2 is not turned on during the freewheeling period, $C_{oss}$ of *TR*2 is only discharged down to the breakdown voltage $V_{BR}$ of $D_s$.

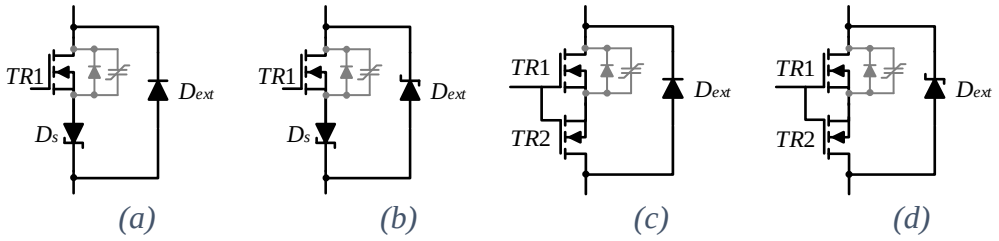



*Figure 5.1 Candidate device permutations for the switch module locations in Figure 4.1.*

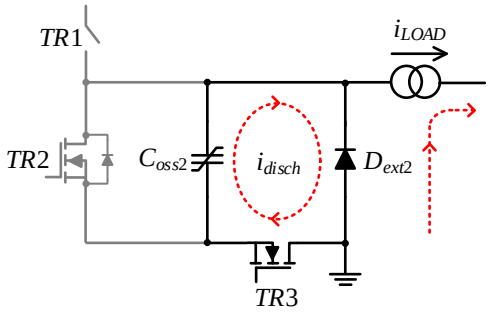



*Figure 5.2 Discharge route for $C_{oss2}$ of TR2 when TR1 is off and $D_{ext2}$ is freewheeling. The circuit is operating with a positive $i_{LOAD}$ and only TR1 is being driven on and off. Provided that TR2 is not turned on during the freewheeling period, $C_{oss}$ is only discharged down to the breakdown voltage $V_{(BR)DSS}$ of TR3.*

When using Module (c) or (d) in the inverter-leg, the SJ MOSFET has a low-voltage MOSFET in the anti-series location. As shown in Figure 5.2, in the fast-switching mode, the $C_{oss}$ of *TR*2 is discharged down to the low-voltage MOSFET's breakdown voltage $V_{(BR)DSS}$. Similar to Figure 4.6, $V_{(BR)DSS}$ is typically such that the $C_{oss}$ capacitance is not discharged to below the 'knee point'. Also, the gradient of the *Q*-*V* curve of $C_{oss}$ is lower at $V_{(BR)DSS}$ than it is at 0 V. When the incoming device *TR*1 turns on, the *TR*2 therefore presents a lower capacitance, and the *TR*1 consequently sources a smaller transient current.

### 5.2.4. Device data

All four modules in Figure 5.1 can be divided into two categories according to their material: all silicon permutations: Modules (a), (c); combined silicon and SiC permutations: Modules (b), (d). The devices used for experimentation in the four

modules are listed in Tables 5.1 - 5.5. Their key parameters are taken from the manufacturers' datasheets.

*Table 5.1 SJ MOSFET* [9].

| | |
|---|---|
| Manufacturer | Infineon |
| Series | 600 V CoolMOS™ P6 Power Transistor |
| Part number | IPW60R041P6 |
| $V_{DS}$ | 650 V ($@T_{j,max}$) |
| $R_{DS(on),max}$ | 41 mΩ ($V_{GS}$ = 10 V, $I_D$ = 35.5 A, $T_j$ = 25 °C) |
| $C_{iss}$ | 8180 pF ($V_{GS}$ = 0 V, $V_{DS}$ = 100 V, $f$ = 1 MHz) |
| Cost* | £ 10.20 |

*Table 5.2 Low-voltage Si Schottky diode* [118].

| | |
|---|---|
| Manufacturer | Taiwan Semiconductor |
| Series | 30.0 AMPS. Schottky Barrier Rectifiers |
| Part number | MBR3060PT |
| $V_{DC}$ | 60 V (Maximum DC blocking voltage) |
| $I_R$ | 1.0 mA (Maximum instantaneous reverse current $@T_C$ = 25 °C) |
| Cost* | £ 1.63 |

*Table 5.3 Si fast recovery PN diode* [119].

| | |
|---|---|
| Manufacturer | IXYS |
| Series | Fast Recovery Epitaxial Diode |
| Part number | DSEI30-06A |
| $V_{RRM}$ | 600 V |
| $I_{FAV}$ | 37 A |
| $t_{rr}$ | 35 ns |
| Cost* | £ 2.98 |

*Table 5.4 SiC Schottky diode* [120].

| | |
|---|---|
| Manufacturer | ROHM |
| Series | SiC Schottky Barrier Diode |
| Part number | SCS220AE |
| $V_R$ | 650 V (DC reverse voltage) |
| $I_F$ | 20 A (Continuous forwad current) |
| $Q_c$ | 31 nC (Total capacitive charge) |
| Cost* | £ 8.36 |

*Table 5.5 Low-voltage Si MOSFET* [121].

| | |
|---|---|
| Manufacturer | International Rectifier |
| Series | HEXFET® Power MOSFET |
| Part number | IRFB7546PBF |
| $V_{DSS}$ | 60 V |
| $R_{DS(on)}$ | 6.0 mΩ (typ.) 7.3 mΩ (max.) |
| $I_D$ | 75 A (Continuous Drain Current, @$V_{GS}$ = 10 V, $T_C$ = 25 °C) |
| $C_{iss}$ | 3000 pF ($V_{GS}$ = 0 V, $V_{DS}$ = 25 V, $f$ = 1.0 MHz) |
| Cost* | £ 0.937 |

* All costs are based on the prices on Farnell or Mouser in 2020.

Each half-bridge inverter-leg contains two modules and other components in the circuit remain the same when implementing different modules.

### 5.2.5. Switching speed consistency

When testing the inverter-leg with Module (a) or (b), the gate resistances in the driver circuit in Figure 4.8 were $R_s$ = 100 Ω and $R_f$ = $R_r$ = 10 Ω. These need to be commensurately reduced when testing Modules (c) and (d) to allow for the increased gate-source capacitance being driven with low-voltage MOSFET in place. By changing the gate resistance, the same voltage trajectories at the gate-source junction of *TR*1 is maintained, and ideally, the same switching speeds are maintained whether *TR*1 is operating with $D_s$ or *TR*2 in series.

For the purpose of experimental comparisons, the gate resistances were set to give modest switching speeds. The trade-offs between the switching losses, and EMI and transient current and voltage peaks would normally be investigated further in a practical converter design. In [122] and [50] where a low-voltage MOSFET is used in anti-series with the main MOSFET, delays are introduced between the MOSFETs' gate drive signals. However, the gates of the MOSFETs in Modules (c) and (d) in Figure 5.1 were connected directly together and were driven by the same signal.

When only driving SJ MOSFET, the gate resistances in Figure 4.8 and the gate-source capacitance of SJ MOSFET $C_{iss\_SJ\ MOS}$ have formed RC circuits, which are charged or discharged during the turn-on and turn-off. The time constant $\tau$ of the CR circuits equals to, respectively,

$$\tau_f = R_f C_{iss\_SJ\,MOS}. \tag{5.1}$$

$$\tau_s = R_s C_{iss\_SJ\,MOS}. \tag{5.2}$$

$$\tau_r = R_r C_{iss\_SJ\,MOS}. \tag{5.3}$$

When testing Modules (c) and (d), the gate of SJ MOSFET and low-voltage MOSFET both are connected to the driver circuit. The low-voltage MOSFET is anti-series with the SJ MOSFET, which makes the gate-source capacitance of two switches are connected in parallel. Then the capacitance that needs to be charged in the RC circuit during turn-on is the sum of $C_{iss\_SJ\,MOS}$ and the gate-source capacitance of low-voltage MOSFET $C_{iss\_LV\,MOS}$. The time constant $\tau$ of the CR circuits changes to, respectively,

$$\tau_f = R_{f(new)} (C_{iss\_SJ\,MOS} + C_{iss\_LV\,MOS}) \tag{5.4}$$

$$\tau_s = R_{s(new)} (C_{iss\_SJ\,MOS} + C_{iss\_LV\,MOS}) \tag{5.5}$$

$$\tau_r = R_{r(new)} (C_{iss\_SJ\,MOS} + C_{iss\_LV\,MOS}) \tag{5.6}$$

where $R_{f(new)}$, $R_{s(new)}$ and $R_{s(new)}$ are new resistances in the driver circuits. In order to remain the same $\tau_f$, putting (5.1) into (5.4) and rearranging it gives

$$R_{f(new)} = \frac{C_{iss\_SJ\,MOS}}{C_{iss\_SJ\,MOS} + C_{iss\_LV\,MOS}} \cdot R_f. \tag{5.7}$$

Similarly, putting (5.2) into (5.5) and rearranging it gives

$$R_{s(new)} = \frac{C_{iss\_SJ\,MOS}}{C_{iss\_SJ\,MOS} + C_{iss\_LV\,MOS}} \cdot R_s. \tag{5.8}$$

Putting (5.3) into (5.6) and rearranging it gives

$$R_{r(new)} = \frac{C_{iss\_SJ\,MOS}}{C_{iss\_SJ\,MOS} + C_{iss\_LV\,MOS}} \cdot R_r. \tag{5.9}$$

According to Tables 5.1 and 5.6, the $C_{iss\_SJ\,MOS}$ of SJ MOSFET IPW60R041P6 is 8180 pF, the $C_{iss\_LV\,MOS}$ of low-voltage MOSFET IRFB7546PBF is 3000 pF. Putting all the data into (5.7), (5.8) and (5.9) gives $R_{s(new)}$ = 73.17 Ω, $R_{f(new)} = R_{r(new)}$ = 7.32 Ω.

## 5.3. Experimental hardware

Figure 5.3 shows the circuit when using Module (a) in the single-phase inverter-leg and its device data are shown in Table 5.6. The circuit with the implementation of Module (b) is shown in Figure 4.11 and its device data in Table 4.2. Figure 5.4 shows the circuit when using Module (c) in the single-phase inverter-leg and its device data are shown in Table 5.7. Figure 5.5 shows the circuit when using Module (d) in the single-phase inverter-leg and its device data are shown in Table 5.8. Figure 5.6 shows the experimental hardware, with the key components labelled.

The inverter-leg was designed to run with an input voltage $V_{dc}$ = 420 V (equal to $V_{dc1}$ + $V_{dc2}$ ) and a total power of 1 kW. Simple sinusoidal PWM was applied with a series of frequencies from 15 kHz, 20 kHz, 25 kHz, 30 kHz up to 35 kHz. With respect to *TR*1, the modulation depth was set such that it operated between a maximum and minimum duty cycle $\delta$ of 0.9 and 0.1. The microcontroller implemented the slow-switching mode for 0.4 < $\delta$ < 0.6 (equals to SSR = 0.1 in Chapter 4). As the power factor is close to one, then $i_{LOAD}$ is known to be in phase with the output voltage and, therefore, average duty cycle. Consequently, the fast-switching mode can be implemented for $\delta$ < 0.4 and $\delta$ > 0.6 with confidence that $i_{LOAD}$ is not close to zero, and that it is definitely negative or positive respectively.

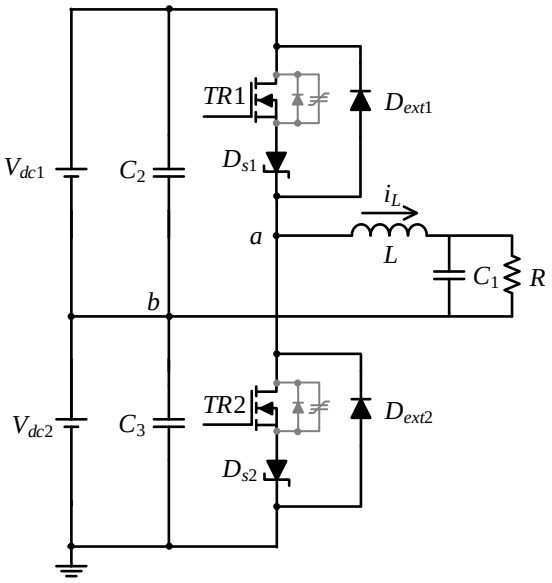



*Figure 5.3 Using Module (a) in the single-phase inverter-leg.*

*Table 5.6 Device data in Figure 5.3.*

| | |
|---|---|
| *TR*1, 2 | IPW60R041P6FKSA1 |
| $D_{s1}$, $D_{s2}$ | MBR3060PT |
| $D_{ext1}$, $D_{ext2}$ | DSEI30-06A |
| *L* | 1 mH (25 A) |
| $C_1$ | 50 µF (450 V) |
| $C_2$, $C_3$ | 470 µF (630 V) |
| *R* | A series-connected *RL* load of 0.8 kVA was supplied. The load was at a power factor *PF* close to one |

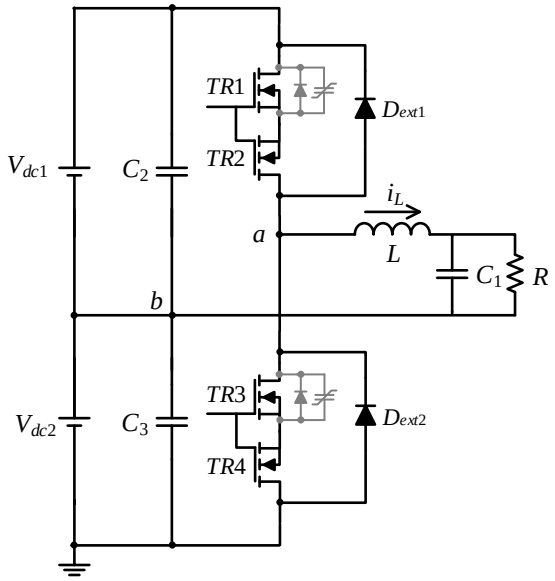



*Figure 5.4 Using Module (c) in single-phase inverter-leg.*

*Table 5.7 Device data in Figure 5.4.*

| | |
|---|---|
| *TR*1, 3 | IPW60R041P6FKSA1 |
| *TR*2, 4 | IRLB3036PBF/ IRFB7546PBF |
| $D_{ext1}$, $D_{ext2}$ | DSEI30-06A |
| *L* | 1 mH (25 A) |
| $C_1$ | 50 µF (450 V) |
| $C_2$, $C_3$ | 470 µF (630 V) |
| *R* | A series-connected *RL* load of 0.8 kVA was supplied. The load was at a power factor *PF* close to one |

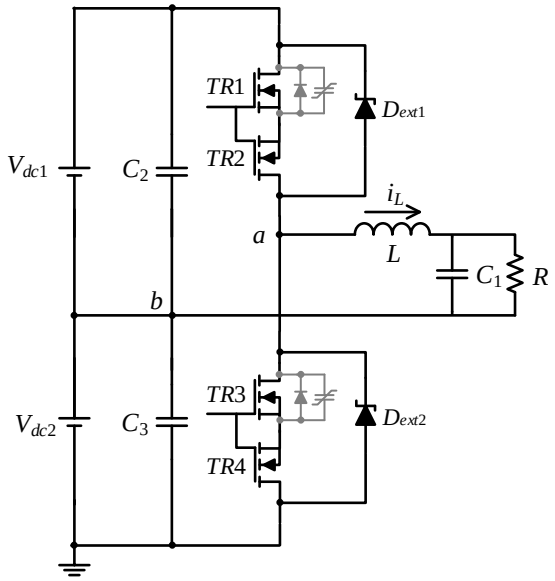



*Figure 5.5 Using Module (d) in single-phase inverter-leg.*

*Table 5.8 Device data in Figure 5.5.*

| | |
|---|---|
| *TR*1, 3 | IPW60R041P6FKSA1 |
| *TR*2, 4 | IRLB3036PBF/ IRFB7546PBF |
| $D_{ext1}$, $D_{ext2}$ | SCS220AEC |
| *L* | 1 mH (25 A) |
| $C_1$ | 50 µF (450 V) |
| $C_2$, $C_3$ | 470 µF (630 V) |
| *R* | A series-connected *RL* load of 0.8 kVA was supplied. The load was at a power factor *PF* close to one |

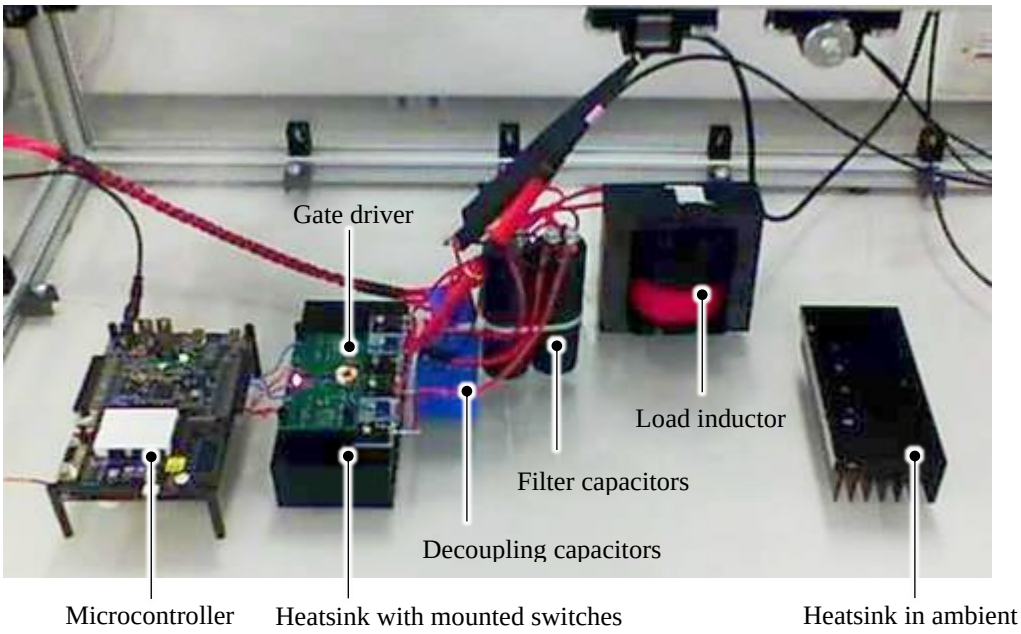



*Figure 5.6 Experimental hardware with key components labelled.*

## 5.4. Loss calculations

As all of the devices have been selected in Section 5.3.2, the total conduction power dissipation can be estimated. The circuit's operating conditions are: $P$ = 1 kW, $V_{dc}$ = 420 V. The modulation index $m$ is set to 0.9. The peak fundamental output voltage $V_{peak}$ is given by

$$V_{peak} = m \cdot \frac{V_{dc}}{2} = 0.9 \times \frac{420}{2} = 189 \text{ V} \tag{5.10}$$

and the RMS output voltage $V_{o(RMS)}$ is given by

$$V_{o(RMS)} = \frac{V_{peak}}{\sqrt{2}} = 133.64 \text{ V}. \tag{5.11}$$

The output current $I_o$ is calculated from

$$I_o = \frac{P}{V_{o(RMS)}} = 7.48 \text{ A} \tag{5.12}$$

and $I_o$ has a peak value $I_{peak}$ of 10.58 A.

### 5.4.1. Module (a)

With a Si fast recovery DSET30-60A PN diode in parallel, the forward voltage drop $V_{F(ext)}$ for $D_{ext}$ is estimated at 1.03 V from the manufacturer's datasheet. The power dissipation $P_{ext}$ in this device is given by

$$P_{ext} = V_{F(ext)} I_{peak} \left( \frac{1}{\pi} - \frac{V_{peak}}{2V_{dc}} \right). \tag{5.13}$$

Putting the data into (5.13) yields $P_{ext}$ = 1.02 W.

With a Si Schottky MBR3060PT diode in series, the forward voltage drop $V_{F(s)}$ for $D_s$ is estimated at 0.46 V from the manufacturer's datasheet. The power dissipation $P_s$ in this device is given by

$$P_s = V_{F(s)} I_{peak} \left( \frac{1}{\pi} + \frac{V_{peak}}{2V_{dc}} \right). \tag{5.14}$$

Putting the data into (5.14) yields $P_s$ = 2.64W.

For the IPW60R041P6FKSA1 MOSFET, the nominal on-state resistance $R_{DS(on)}$ is 41 mΩ. The conduction losses $P_{cond}$ are given by

$$P_{cond} = R_{DS(on)} I_{peak}^2 \left( \frac{1}{4} + \frac{4V_{peak}}{3\pi V_{dc}} \right). \quad (5.15)$$

Putting the data into (5.15) yields $P_{cond}$ = 2.02 W. Adding the results from (5.13), (5.14) and (5.15) yields a total power dissipation attributable to conduction losses of 5.68 W.

### 5.4.2. Module (b)

With the SCS220AE SiC Schottky diode in parallel, the forward voltage drop $V_{F(ext)}$ for $D_{ext}$ is estimated at 1.05 V from the manufacturer's datasheet. The power dissipation $P_{ext}$ in this device is given by

$$P_{ext} = V_{F(ext)} I_{peak} \left( \frac{1}{\pi} - \frac{V_{peak}}{2V_{dc}} \right). \quad (5.16)$$

Putting the data into (5.16) yields $P_{ext}$ = 1.04 W.

With silicon Schottky diode MBR3060PT in series, the power dissipation $P_s$ in this device is the same as (5.14), which is 2.64 W. For the IPW60R041P6FKSA1 MOSFET, the conduction losses $P_{cond}$ is same as (5.15) which equals to 2.02 W. Adding the results from (5.14), (5.15) and (5.16) yields a total power dissipation attributable to conduction losses of 5.7 W.

### 5.4.3. Module (c)

With silicon fast recovery DSET30-60A PN diode in parallel. The power dissipation $P_{ext}$ in this device is given by (5.13), which is 1.02 W.

For the IPW60R041P6FKSA1 MOSFET, the nominal on-state resistance $R_{DS(on)}$ is 41 mΩ. For the IRFB7546PBF MOSFET, the nominal on-state resistance $R_{DS(on)}$ is 6.0 mΩ. Both switches active at the same time and the conducting current through them are exactly the same. The conduction losses $P_{cond}$ of both switches are given by

$$P_{cond} = R_{DS(on)} I_{peak}^2 \left( \frac{1}{4} + \frac{4V_{peak}}{3\pi V_{dc}} \right) \quad (5.18)$$

where the $R_{DS(on)}$ is the sum of the on-state resistance of IPW60R041P6FKSA1 and IRFB7546PBF. Putting the data into (5.18) yields $P_{cond}$ = 2.32 W.

Adding the results from (5.13) and (5.18) yields a total power dissipation attributable to conduction losses of 3.34 W.

### 5.4.4. Module (d)

With a SCS220AE SiC Schottky diode in parallel, the power dissipation $P_{ext}$ in this device is given by (5.16) which is 1.04 W. The conduction losses $P_{cond}$ of the IPW60R041P6FKSA1 and IRFB7546PBF are given by (5.18) which is 2.32 W Adding the results from (5.16) and (5.18) yields a total power dissipation attributable to conduction losses of 3.36 W.

The conduction losses of different modules above are summarised in Table 5.9. The switching power dissipation is related to many factors, such as switching frequency, SSR (percentage of soft-switching mode during one switching period). SJ MOSFET is also partially discharged during the fast-switching mode as in Figure 4.5 and Figure 5.1, which makes it is more difficult to estimate. So we have not quantified the switching losses here, and these are assessed experimentally. In Table 5.9, the total cost for each module was calculated as the sum of the cost of the three different devices.

*Table 5.9 Summary for each module in Figure 5.1.*

| Module | Conduction losses (W) | Estimated switching losses behaviour | Total cost (£) |
|---|---|---|---|
| (a) | 5.68 | Switching behaviour less influenced by frequency | 14.81 |
| (b) | 5.7 | Better performance of SiC diode at high frequency | 20.19 |
| (c) | 3.34 | Increased switching power in MOSFET at high frequency | 14.12 |
| (d) | 3.36 | Increased switching power in MOSFET at high frequency, while better performance of SiC diode at high frequency | 19.50 |

## 5.5. Software

The microcontroller at the bottom left of Figure 5.6 is the PSoC type from Cypress. The primary function of the microcontroller here is: (a) generating a series of PWM signals based on a 50-Hz fundamental-frequency sinusoidal modulation signal; (b) realising the dual-mode switching technique by controlling the enable signal. Section 4.7 of Chapter 4 has been discussing how to implement dual-mode switching technique by the cooperation of logic peripheral circuit and code of PSoC microcontroller. Different from the application in Chapter 4 that the PSoC only needs to generate a fixed frequency SPWM (20 kHz), the frequency of SPWM need to be

generated here vary from 15 kHz to 35 kHz, so the CY8C5868AXI-LP035 type of PSoC was selected.

In the logic peripheral circuit, the TopDesign (peripheral circuit design in *PSoC Creator*) here is similar to Figure 4.20, except the system clock was improved from 12 MHz to 48 MHz. In the PWM component, the dead-time of the complementary output signal was also set to 1 μs. There are two options for the resolution of the PWM component, 8-bit and 16-bit. The limitation of resolution r is given by

$$(2^r - 1) \cdot \frac{1}{f_{clock}} \geq \left(\frac{1}{f_{sw}}\right)_{max} \tag{5.20}$$

where the clock of the PWM component $f_{clock}$ is 48 MHz, $f_{sw}$ was selected as 15 kHz to realise the maximum value of $1/f_{sw}$. The limitation of resolution is $r \geq 8.33$, which leads to the selected resolution is 16-bit.

The period of the PWM component needs to be set to appropriate numbers to generate the desired frequency. This number is critical and used multiple times in the code. The period of the PWM component $p$ is given by

$$(p + 1) \cdot \frac{1}{f_{clock}} = \frac{1}{f_{sw}}. \tag{5.21}$$

When $f_{sw}$ is equal to 15 kHz, 20 kHz, 25 kHz, 30 kHz and 35 kHz, then $p$ is equal to 3199, 2399, 1919, 1599 and 1370 respectively.

In the code, the modulation index improved from 0.8 to 0.9 to provide a higher bus voltage utilization. By changing the compare value of the PWM component in the interrupt code, the time that the output signal stays high will change accordingly. A flag was set at the beginning and the ending of the interrupt code. The duration of the flag indicates the duration of the interrupt code, which also defines the theoretical limitation of the highest frequency signal that can be generated by the PSoC. The period of the flag was experimentally evaluated as 10 μs with an oscilloscope, which equates to 100 kHz. This leaves enough margin than 35 kHz. So the CY8C5868AXI-LP035 type selected here is qualified in the implementation.

All the compare value comes that need to be given to the PWM component during the interrupt is from a lookup table in the code. This lookup table contains enough number

and precision of the data of a 50-Hz sine wave. The frequency of the output signal defines how many data is going to be evenly selected from the table. Every time the main function goes into the interrupt, one data from the table is given to the compare value of the PWM component. By varying the frequency of interrupt, the frequency of the output signal will change accordingly. $f_{sw}$ is the frequency of SPWM that need to be generated, $n$ is the number of the date that selected from the sin table and given to the PWM component.

$$n = \frac{f_{sw}}{f_{sin}} \tag{5.19}$$

where the $f_{sin}$ is 50Hz. When $f_{sw}$ is equal to 15 kHz, 20 kHz, 25 kHz, 30 kHz and 35 kHz, then $n$ is equal to 300, 400, 500, 600 and 700 respectively. The coding of PSoC can be found in Appendix C.

## 5.6. Experimental results

The circuits in Figures 5.3, 4.11, 5.4 and 5.5 were run at a series of frequencies, and the experimental results are given in this section. The temperature rise of the heatsink (see Figure 5.6) above the ambient was recorded in each case when the heatsink reaches its thermal steady state. Thermal superposition was used to infer the power device losses. Input power was recorded from the power supply. The dissipated power and the efficiency are calculated for each scenario. The heatsink used here is the same one used in Chapter 4, so its thermal resistance was 1.60 °C/W.

### 5.6.1. Module (a)

Table 5.10 shows the experimental results when running the circuit in Figure 5.3 at a series of frequencies. Figure 5.7 shows exemplifying thermal photographs taken with a FLIR C5 thermal camera when the heatsink temperature has reached its steady state.

### 5.6.2. Module (b)

Table 5.11 shows the experimental results when running the circuit in Figure 4.11 at a series of frequencies.

### 5.6.3. Module (c)

Table 5.12 shows the experimental results when running the circuit in Figure 5.4 at a series of frequencies.

### 5.6.4. Module (d)

Table 5.13 shows the experimental results when running the circuit in Figure 5.5 at a series of frequencies.

*Table 5.10 Experimental results of Module (a).*

| Frequency /kHz | $D_{temp}$/°C | Input Power | | Dissipation Power /W | Efficiency /% |
|---|---|---|---|---|---|
| | | Voltage/ V | Current/ A | | |
| 15 | 20.07 | 420 | 2.41 | 12.54 | 98.76 |
| 20 | 22.47 | 420 | 2.36 | 14.04 | 98.58 |
| 25 | 25.43 | 420 | 2.32 | 15.89 | 98.37 |
| 30 | 27.70 | 420 | 2.28 | 17.31 | 98.19 |
| 35 | 31.47 | 420 | 2.24 | 19.67 | 97.91 |

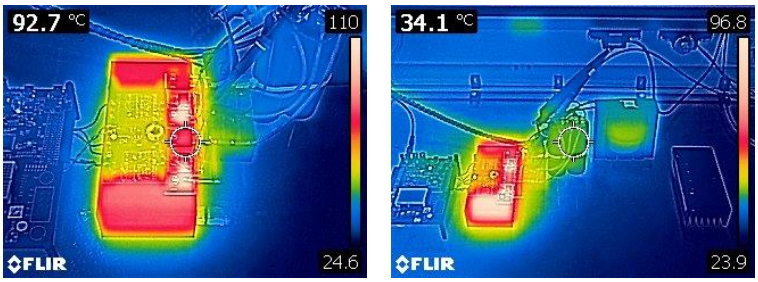



*Figure 5.7 Thermal photographs of heatsink (left), circuitry (right) when running the circuit in Figure 5.3.*

*Table 5.11 Experimental results of Module (b).*

| Frequency /kHz | $D_{temp}$/°C | Input Power | | Dissipation Power /W | Efficiency /% |
|---|---|---|---|---|---|
| | | Voltage/ V | Current/ A | | |
| 15 | 18.13 | 420 | 2.41 | 11.33 | 98.88 |
| 20 | 20.83 | 420 | 2.36 | 13.02 | 98.69 |
| 25 | 22.23 | 420 | 2.32 | 13.89 | 98.57 |
| 30 | 24.40 | 420 | 2.28 | 15.25 | 98.41 |
| 35 | 26.90 | 420 | 2.24 | 16.81 | 98.21 |

*Table 5.12 Experimental results of Module (c).*

| Frequency /kHz | $D_{temp}$/°C | Input Power | | Dissipation Power /W | Efficiency /% |
|---|---|---|---|---|---|
| | | Voltage/ V | Current/ A | | |
| 15 | 16.60 | 420 | 2.44 | 10.38 | 98.99 |
| 20 | 19.23 | 420 | 2.36 | 12.02 | 98.80 |
| 25 | 22.80 | 420 | 2.35 | 14.25 | 98.56 |
| 30 | 25.70 | 420 | 2.32 | 16.06 | 98.35 |
| 35 | 28.50 | 420 | 2.29 | 17.81 | 98.15 |

*Table 5.13 Experimental results of Module (d).*

| Frequency /kHz | $D_{temp}$/°C | Input Power | | Dissipation Power /W | Efficiency /% |
|---|---|---|---|---|---|
| | | Voltage/ V | Current/ A | | |
| 15 | 14.25 | 420 | 2.43 | 8.90 | 99.13 |
| 20 | 16.07 | 420 | 2.39 | 10.04 | 99.00 |
| 25 | 18.00 | 420 | 2.35 | 11.25 | 98.86 |
| 30 | 20.93 | 420 | 2.33 | 13.08 | 98.66 |
| 35 | 23.13 | 420 | 2.29 | 14.46 | 98.50 |

## 5.7. Experimental results analysis

### 5.7.1. Comparison between Module (a) and Module (b)

Experimental results of Module (a) and Module (b) are compared in Figures 5.8 and 5.9. Module (a) is presented in blue lines and Module (b) is presented in orange lines. Linear trend-lines and their equations are superimposed. The difference between the two modules is that Module (a) uses Si fast recovery PN diode DSEI30-06A as the external diode, while Module(b) uses a SCS220AE SiC Schottky diode in this location.

Calculating according to the equations, the intersection of the two linear trend-lines is around 4 kHz. So we can predict, the dissipated power of Module (a) is smaller than that of Module (b) when the frequency is less than 4 kHz, while the dissipation power of Module (a) is more significant when the frequency higher than 4 kHz. As the frequency increase, the dissipation power of both modules increases, while the rise of Module (a) is more evident. This is also reflected in the coefficients of “x” in the equations. The efficiency of Module (b) is 98.21 % at 35 kHz, while Module (a) is only 97.91 % at the same frequency.

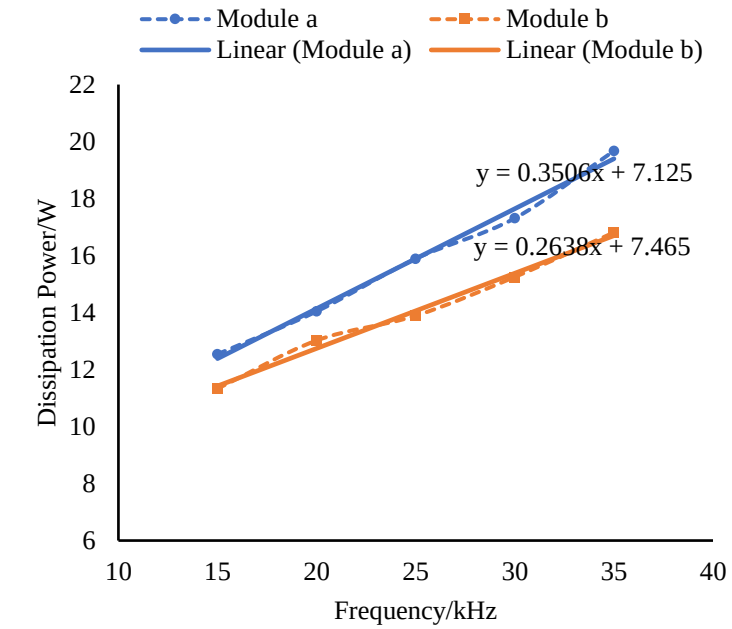



*Figure 5.8 Dissipated power of Modules (a) and (b). Linear trend-lines and their equations are superimposed.*

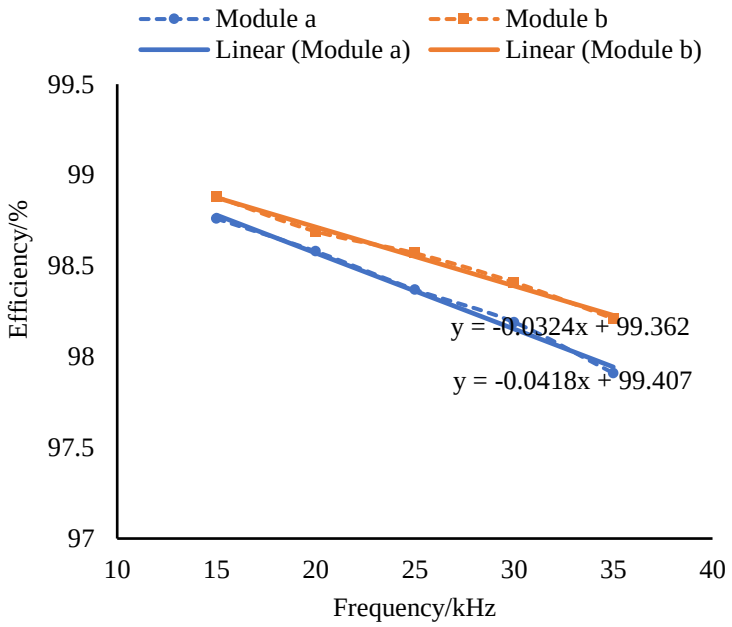



*Figure 5.9 Efficiencies of Modules (a) and (b). Linear trend-lines and their equations are superimposed.*

### 5.7.2. Comparison between Module (c) and Module (d)

Experimental results from Module (c) and Module (d) are compared in Figures 5.10 and 5.11. Module (c) is presented in red lines and Module (d) is presented in green lines. Linear trend-lines and their equations are superimposed. Both modules are equipped with IRFB7546PBF as the anti-series device. Module (c) uses a DSEI30-

06A Si fast recovery PN diode as the external diode, while Module (d) uses a SCS220AE SiC Schottky diode.

According to the equations of the linear trend-lines, there is no intersection point in the first quadrant. So we can predict, Module (d) has an advantage in power dissipation at all frequencies.

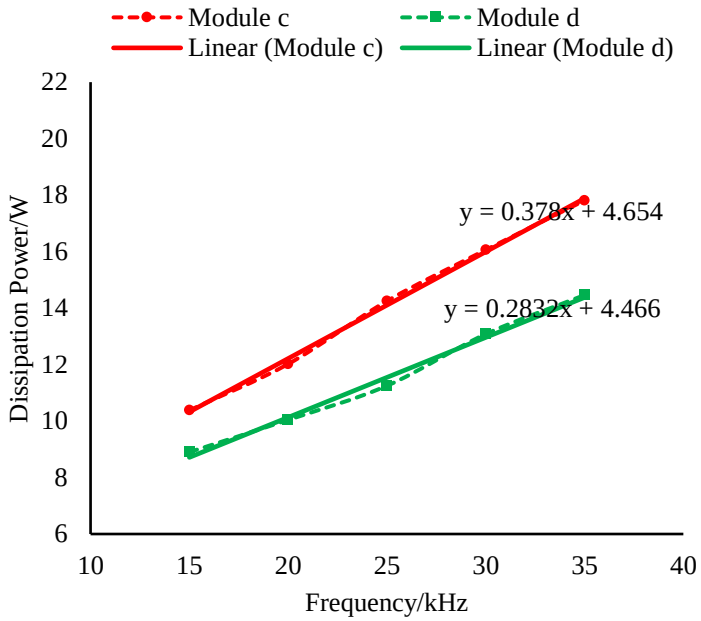



*Figure 5.10 Dissipated power of Modules (c) and (d). Linear trend-lines and their equations are superimposed.*

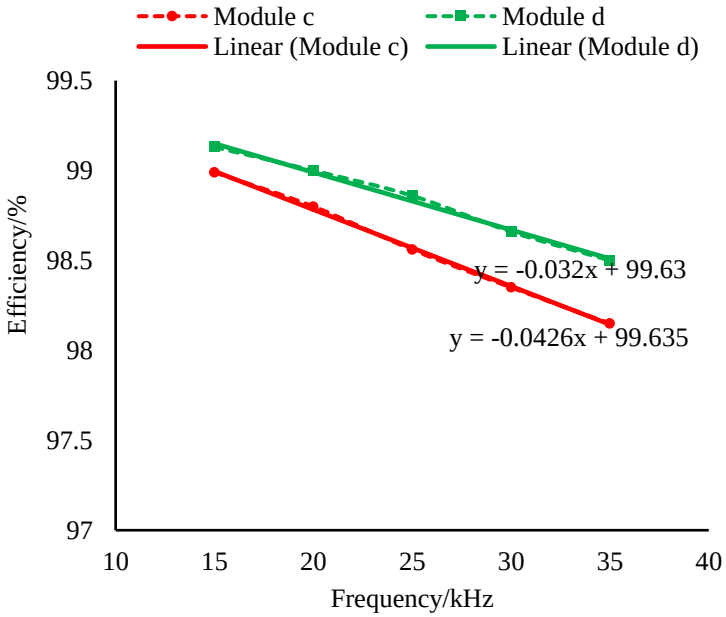



*Figure 5.11 Efficiencies of Modules (c) and (d). Linear trend-lines and their equations are superimposed.*

### 5.7.3. Comparison between Module (a) and Module (c)

Experimental results of Module (a) and Module (c) are compared in Figures 5.12 and 13. The difference between the two modules is that Module (a) uses Si Schottky diode MBR3060PT in series and Module (c) uses low-voltage MOSFET IRFB7546PBF in anti-series.

Calculating according to the equations, the intersection of the two linear trend-lines is around 90 kHz. So we can predict, the power dissipation of Module (a) is larger than Module (c) when the frequency is lesser than 90 kHz, while the power dissipation of Module (a) will be less than Module(c) when the frequency goes higher than 90 kHz.

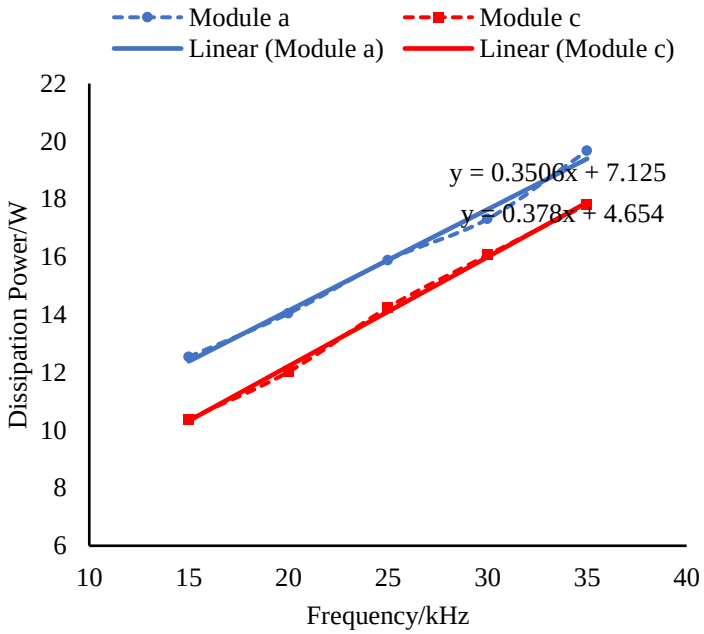



*Figure 5.12 Dissipated power of Modules (a) and (c). Linear trend-lines and their equations are superimposed.*

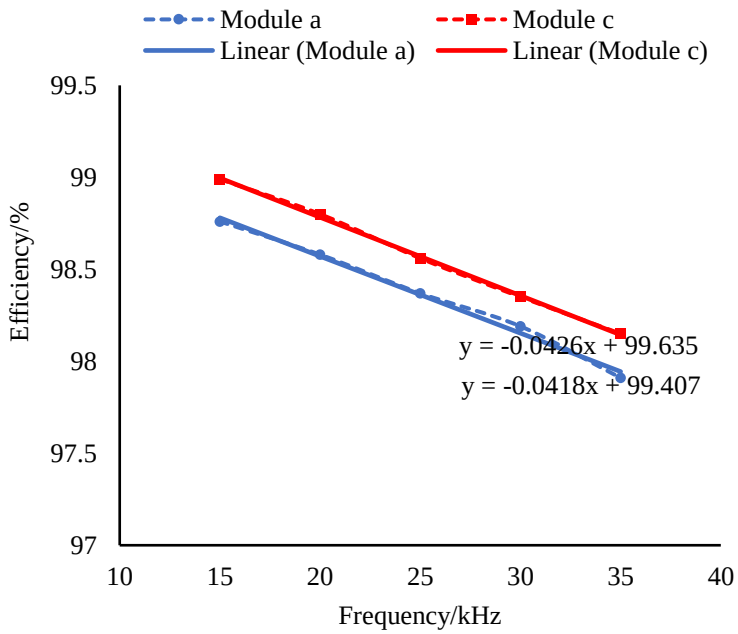



*Figure 5.13 Efficiencies of Modules (a) and (c). Linear trend-lines and their equations are superimposed.*

### 5.7.4. Comparison between Module (b) and Module (d)

Experimental results of Module (b) and Module (d) are compared in Figures 5.14 and 5.15. The difference between two modules is that Module (b) uses an MBR3060PT Si Schottky diode in series and Module (d) uses a low-voltage IRFB7546PBF MOSFET in anti-series.

Calculating according to the equations, the intersection of the two linear trend-lines is around 155 kHz. So we can predict, the dissipation power of Module (b) is smaller than Module (d) when the frequency is less than 155 kHz, while the power dissipation of Module (d) will be more than Module (b) when the frequency goes higher than 155 kHz.

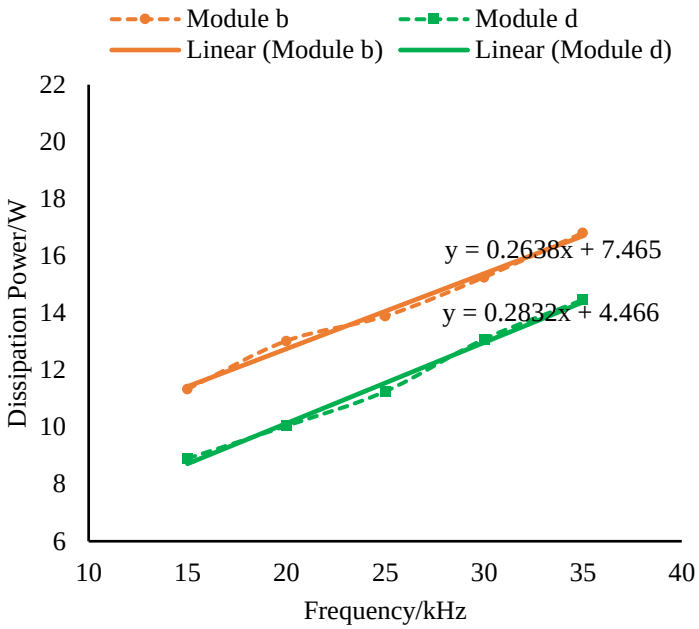



*Figure 5.14 Dissipated power of Modules (b) and (d). Linear trend-lines and their equations are superimposed.*

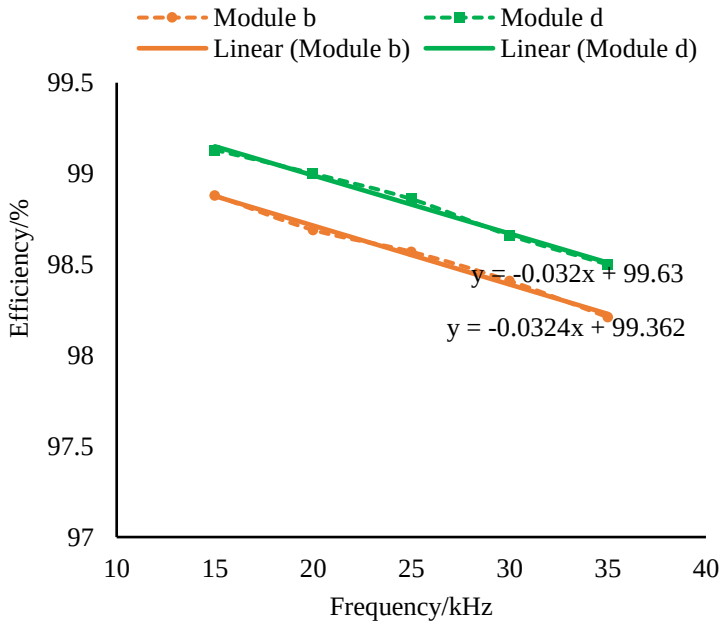



*Figure 5.15 Efficiencies of Modules (b) and (d). Linear trend-lines and their equations are superimposed.*

## 5.8. Discussion

Table 5.14 summarises the experimental results of four modules and the following points are noted.

*Table 5.14 Experimental results summary for four modules.*

| Module configuration | | (a) | (b) | (c) | (d) |
|---|---|---|---|---|---|
| Conduction losses (W) | Calculation | 5.68 | 5.7 | 3.34 | 3.36 |
| | Experiment | 7.125 | 7.465 | 4.654 | 4.466 |
| Total losses behaviour | | Better than (b) when $f$ < 4 kHz; Better than (c) when $f$ > 90 kHz | Better than (a) when $f$ > 4 kHz; Better than (d) when $f$ > 155 kHz | Better than (a) when $f$ < 90 kHz | Always better than (c); Better than (b) when $f$ < 155 kHz |
| Best efficiency | | When $f$ > 155 kHz, (b) has the best efficiency<br>When $f$ < 155 kHz, (d) has the best efficiency | | | |

- The conduction losses of each module can be experimentally estimated as the intersection of their losses curve with the vertical axis. This number is reflected in the equations of linear trend-lines. Tables 5.1 4summarise the theoretical and practical conduction losses of each module. It is evident that the practical conduction losses are more significant than the theoretical losses for all modules. This may come from the effect of temperature on $R_{DS(on)}$ which did not take into account in the calculations.

- The dissipated power increases as the frequency increases in all modules. The dissipation power and the frequency have a linear relationship. This is because the conduction losses do not change with the frequency but the switching frequency changes linearly with the frequency. The results of frequencies from 15 Hz to 35 Hz can provide a precise prediction of higher frequencies.

- By comparing Module (a) and (b), Module (c) and (d), only the external device is different and other devices remain the same. Through the Section 5.7.1 and 5.7.2, modules with a SCS220AE SiC Schottky diode (Modules (b), (d)) have better performance than modules with a DSEI30-06A Si fast recovery PN diode (Module (a), (c)) at all frequencies.) This advantage is more obvious at high frequencies. This proves SiC devices, even more costly, are more advantageous than their Si counterparts in high-frequency applications. When the frequency is low and the cost is the primary consideration, Si devices are still the mainstream.

- By comparing Module (a) and (c), Module (b) and (d), only the series device is different and other devices remain the same. Through the Section 5.7.3 and 5.7.4, modules with a low-voltage IRFB7546PBF MOSFET (Module (c), (d)) have better performance than modules with Si Schotty diode MBR3060PT (Module (a), (b)) when frequency lower than tens of kHz. This is because the low-voltage MOSFETs have smaller conduction losses than diodes. When the frequency becomes higher, the switching losses of the low-voltage MOSFETs increases so the power dissipation of Module (c), (d) becomes more prominent than Module (a), (b). Besides, including more active switches in the circuits adds more requirements and complexity in the driver circuit. The power consumption of the driver circuit will increase as well. Therefore, it needs to compromise and chose according to practical demand.
- All the efficiencies have been calculated with the neglect of passive devices in the circuits.
- Experiments were conducted in the room temperature. Informed by these results, two of these permutations is selected for further evaluation in a cryogenic power electronic system at 77 K [123].

## 5.9. Conclusion

Alternative device selection is presented and experimentally evaluated in this chapter for a 1-kW 420-V inverter-leg switched at a series of frequencies, namely 15 kHz, 20 kHz, 25 kHz, 30 kHz and 35 kHz. Different modules are operating with the dual-mode switching technique in the inverter-leg. Losses and efficiencies of each scenario are calculated and compared. Each module has its advantages and weaknesses. The suitability of each module under different frequencies has been discussed.

# Chapter 6

# Control of incoming drain currents drawn by super-junction MOSFETs in voltage source bridge-legs

## 6.1. Introduction

When a MOSFET in a voltage source bridge-leg turns on, a charging current has to be sourced into the output capacitance of the complementary freewheeling MOSFET, even if its intrinsic diode has been deactivated. The peak incoming drain current in the MOSFET turning on can be limited by simply using a large resistance in series with its gate as in the slow-switching mode discussed in Chapter 4. However, this increases the power dissipation in the MOSFET. Furthermore, the turn-on propagation delay time is increased. This chapter presents a gate driver circuit for profiling the MOSFET's incoming drain current to provide an improved trade-off between the incoming peak current, turn-on power dissipation, and delay time.

SJ MOSFETs with proposed gate driver and conventional gate driver are used in 400-V bridge-leg and switched at 20 kHz. Triangular incoming drain current profile and rectangular incoming drain current profile are present and compared under different gate resistances.

## 6.2. Issues with incoming current profile in slow-switching mode

In Figure 6.1, the turn-on action of *TR*2 in is considered when the bridge-leg has $i_{LOAD}$ flowing into its mid-point. $i_{LOAD}$ is taken as being low, and hence the converter is operating in the slow-switching mode. If the intrinsic diode of *TR*1 has been deactivated effectively by the circuitry in Figure 4.1, *TR*1's equivalent circuit can be approximated solely by its output capacitance $C_{oss1}$. The reverse recovery charge of $D_{ext2}$ is low in comparison with that drawn by $C_{oss1}$, so $D_{ext2}$ is neglected here.

If *TR*2 turns on when *TR*1 is off, the $C_{oss}$ of *TR*1 is charged to the DC link voltage $V_{dc}$. If *TR*1 is turned on when *TR*2 is off, then *TR*1 fully self-discharges its $C_{oss}$ down to 0 V and this $C_{oss}$ has to be recharged when *TR*2 next turns on.

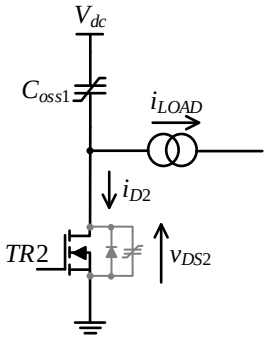



*Figure 6.1. Equivalent circuit from bridge-leg in Figure 4.1 when $i_{LOAD}$ is negative and TR2 is turning on, and the intrinsic diode of TR1 has been deactivated.*

### 6.2.1. Triangular current profile

In Figure 6.1, the peak incoming drain current $i_{D2}$ is limited by using a large gate resistance. A feature of this arrangement is the inherently triangular incoming drain current profile with respect to time, as shown in Figure 6.2. When the gate-source voltage $v_{GS}$ reaches its threshold level $V_{GS(th)}$ at Point A, the MOSFET has the full supply voltage $V_{dc}$ across its drain-source terminals. It then begins to conduct whilst in the pinch-off condition, and still supports virtually all of $V_{dc}$. $i_{D2}$ rises approximately linearly until the bulk of $Q_{oss}$ has been supplied into $C_{oss1}$ at Point B. During this phase $v_{GS}$ has increased in an approximately linear manner with respect to time as the change in $v_{GS}$ has been over only a small section of an exponential curve. At Point B $C_{oss1}$ falls

abruptly and, in moving to Point C, $i_{D2}$ falls to the steady-state load current level and $v_{DS2}$ falls from the rail voltage to virtually zero.

A disadvantage of the triangular current profile is that the overshoot current $I_{os}$, as defined in Figure 6.2 (c), is high. When $C_{oss1}$ falls, a large current has been established in both *TR*1 and *TR*2. Interrupting this current results in a high-frequency oscillation in the voltage at the source of *TR*1. This, in turn, can result in a transient voltage exceeding $V_{dc}$ appearing across *TR*1, and an EMI signature with a raised high-frequency content. $I_{os}$ can be reduced by switching more slowly to address these problems shown in Figure 4.7. However, this incurs increased losses in the MOSFET as it spends more time with the rail voltage across it whilst conducting both $i_{LOAD}$ and the $C_{oss}$-charging current.

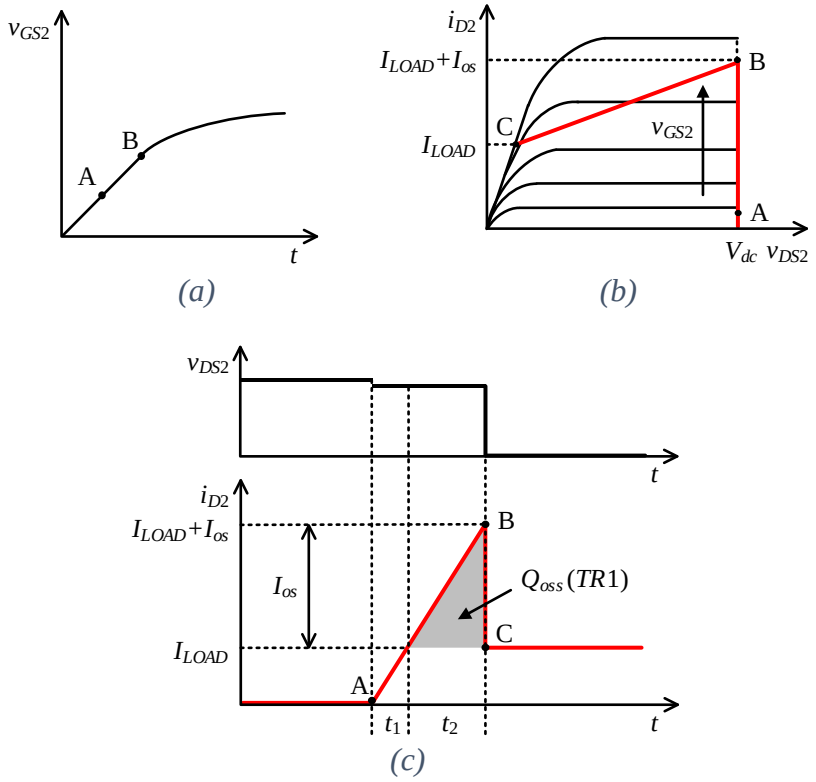



*Figure 6.2. Idealised behaviour of SJ MOSFET in bridge-leg at TR2 turn-on, showing its incoming drain current profile. (a) $v_{GS2}$ as a function of time. (b) $i_{D2}$ as a function of $v_{DS2}$. (c) $v_{DS2}$ as a function of time, $i_{D2}$ as a function of time.*

Using a large gate resistance to reduce the turn-on speed of a MOSFET has a further disadvantage as the time delay *D* between the gate signal from the driver IC going high and the MOSFET's gate voltage reaching its threshold value becomes lengthened.

Distortion results in the output voltage and current due to this propagation delay between the MOSFET being signalled on and its drain-source voltage falling.

With respect to the waveforms in Figure 6.2 (c), $Q_{oss}$ is given by

$$Q_{oss} = \frac{t_2 I_{oss}}{2}. \tag{6.1}$$

(6.1) is rearranged to give

$$t_2 = \frac{2Q_{oss}}{I_{os}}. \tag{6.2}$$

The rate of rise of $i_{D2}$ is taken as being the same during the intervals $t_1$ and $t_2$, and therefore

$$\frac{I_{LOAD}}{t_1} = \frac{I_{os}}{t_2}. \tag{6.3}$$

(6.3) is rearranged to give

$$t_1 = \frac{I_{LOAD}}{I_{os}} t_2. \tag{6.4}$$

Putting the result from (6.2) into (6.4) gives

$$t_1 = \frac{2I_{LOAD} Q_{oss}}{{I_{os}}^2}. \tag{6.5}$$

The results from (6.2) and (6.5) are added to give the total time $T_{TOTAL}$ for $i_{D2}$ to rise from 0 A to $I_{LOAD} + I_{os}$:

$$T_{TOTAL} = \frac{2Q_{oss}}{I_{os}} \left( \frac{I_{LOAD}}{I_{os}} + 1 \right). \tag{6.6}$$

The turn-on energy dissipation $E_{on(tri)}$ in $TR2$ with a triangular incoming drain current trajectory is given by

$$E_{on(tri)} = V_{dc} \left( \frac{I_{LOAD} + I_{os}}{2} \right) T_{TOTAL}. \tag{6.7}$$

Putting the result from (6.6) into (6.7), and rearranging yields

$$E_{on(tri)} = V_{dc} Q_{oss} \left( 1 + \frac{2I_{LOAD}}{I_{os}} + \frac{{I_{LOAD}}^2}{{I_{os}}^2} \right). \tag{6.8}$$

## 6.2.2. Rectangular current profile

Compared to the triangular profile, a rectangular profile, Figure 6.3, would be expected to yield lower turn-on losses for a given overshoot current.

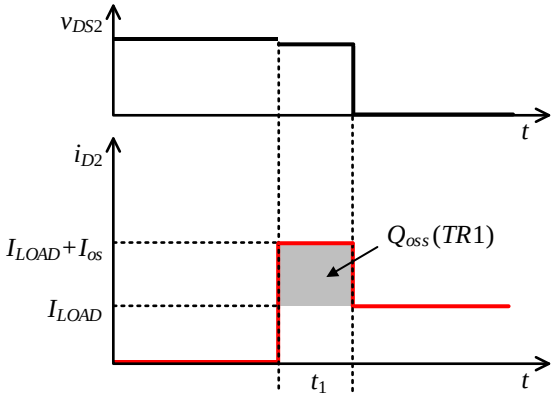



*Figure 6.3 Idealised rectangular incoming drain current profile.*

With respect to the waveforms in Figure 6.3, $Q_{oss}$ is given by

$$Q_{oss} = t_1 I_{os}. \tag{6.9}$$

(6.9) is rearranged to give

$$t_1 = \frac{Q_{oss}}{I_{os}}. \tag{6.10}$$

The turn-on energy dissipation $E_{on(rec)}$ in $TR2$ with a rectangular incoming drain current trajectory is given by

$$E_{on(rec)} = V_{dc}(I_{LOAD} + I_{os})t_1. \tag{6.11}$$

The result from (6.10) is put into (6.11) to yield

$$E_{on(rec)} = V_{dc}Q_{oss}\left(1 + \frac{I_{LOAD}}{I_{os}}\right). \tag{6.12}$$

Figure 6.4 shows $E_{on(tri)}$ and $E_{on(rec)}$ plotted against overshoot current $I_{os}$ for triangular and rectangular trajectories for some representative conditions. These were $V_{dc}$ = 400 V, $I_{LOAD}$ = 3 A, and $Q_{oss}$ = 300 nC. (6.8) and (6.12) were used to calculate the turn-on energies.

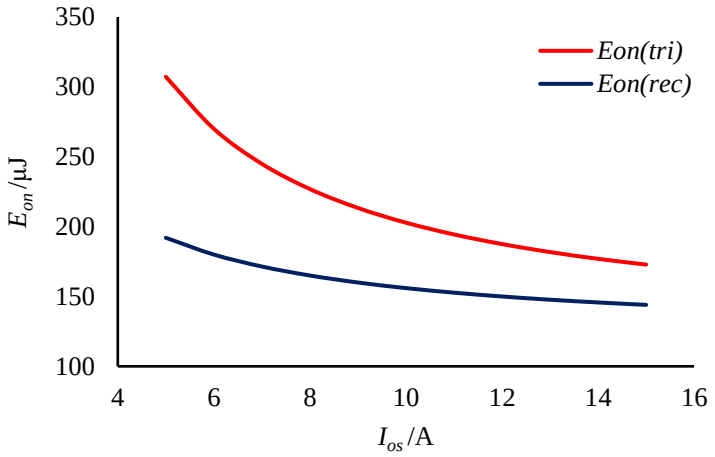



*Figure 6.4 Expected turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ shown against $I_{os}$.*

## 6.3. Proposed circuitry for realising rectangular incoming drain current profile

A technique was presented in [124] for controlling the incoming diode recovery current profile drawn by a MOSFET in a single-ended converter. As shown in Figure 6.5, a current transformer (CT) is used to provide a diode recovery current control arrangement. When $Q_1$ turns on, the load current is commutated from $D_1$ to $Q_1$, a voltage drop across $R_2$ is developed as a function of the current in the primary conductor of the CT. With an appropriately chosen $R_2$ and CT turns-ratio, the drain current of $Q_1$ will be limited to a set value during the diode recovery period.

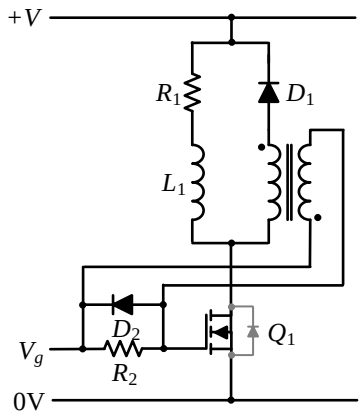



*Figure 6.5 Circuitry from* [124].

In this chapter, the technique in [124] is extended to a VSC bridge-leg where the incoming drain currents in two SJ MOSFETs have to be controlled. Also, resetting of the CT is addressed; the technique is applied in conjunction with a dual-mode gate

driver arrangement; its efficacy is experimentally compared with that of a traditional arrangement where the incoming current profile is determined by simply setting the gate resistance to a desired value. A feature of the arrangement in [124] is that the CT is used to both detect the recovery current and control it. Other techniques can be used for sensing currents in power devices, for protection against short-circuits or to obtain the current profile for active shaping of currents during switching transients. Methods include the use of a Rogowski coil [125] and detection of the voltage developed across the parasitic emitter inductance of an IGBT [126], [127]. The advantage of the CT here is that its output can be used to directly control the MOSFET's drain current, without the need for integrators and other conditioning circuitry.

Figure 6.6 and Figure 6.7 show the proposed circuitry. In Figure 6.6 it is seen that the primary winding of each CT is connected directly in series with each MOSFET. As shown in Figure 6.7, the CT in each case acts to limit the gate voltage. This differs from [124] where the primary conductor of the CT limiting the current flow into a MOSFET was connected in series with the freewheeling element sourcing the incoming recovery current. It is noted that the current being directly controlled with the proposed arrangement is therefore not the reverse current through the freewheeling element, as in [124], but is the peak current $I_{pk}$ ($I_{LOAD}$+$I_{os}$) in the incoming MOSFET. As shown in Figure 6.3, $I_{pk}$ is composed of both $i_{LOAD}$ and the reverse current into the freewheeling element.

Neglecting any magnetising current drawn by the CT, the secondary current $i_2$ is related to the primary current $i_1$ by

$$\frac{i_2}{i_1} = \frac{N_1}{N_2} \tag{6.13}$$

where $N_1$ and $N_2$ are the CT's primary and secondary turns numbers, respectively. If $i_1 = I_{\mathrm{pk}}$ then:

$$i_2 = \frac{N_1}{N_2} I_{pk}. \tag{6.14}$$

At turn-on in the slow-switching mode, only Output A of the driver IC goes high initially, and $i_2$ circulates in Loop 1 shown in Figure 6.7 (a). The voltage $v_{Rg}$ across the resistance $R_g$ during this interval is given by

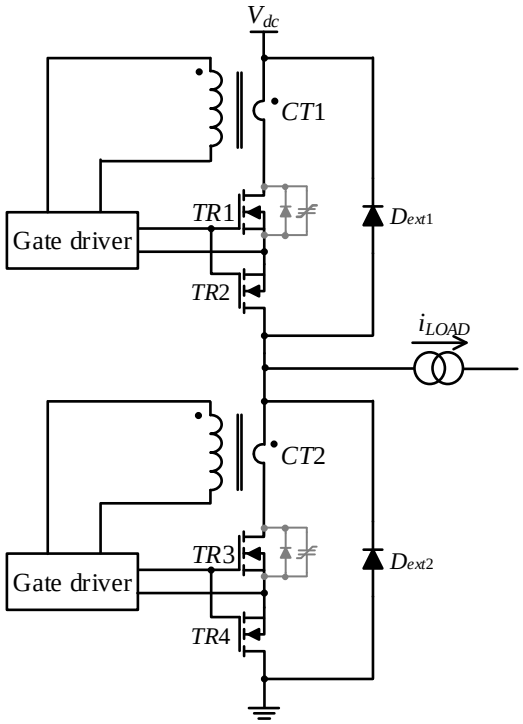



*Figure 6.6 Bridge-leg equipped with proposed circuitry.*

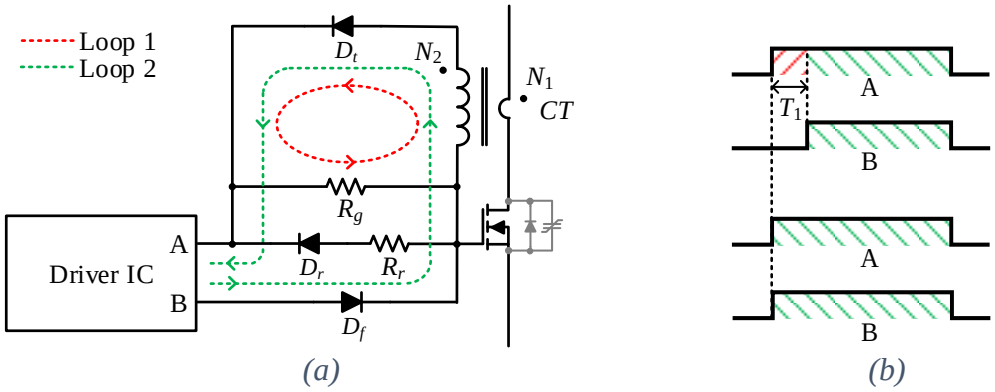



*Figure 6.7 (a) Local gate driver circuit. (b) Two output signals, A and B, are produced by the driver IC. In the slow-switching mode, a delay time $T_1$ is introduced. In the fast-switching mode, A and B are synchronous.*

$$v_{Rg} = R_g i_2. \tag{6.15}$$

Putting the result from (6.14) into (6.15) gives

$$v_{Rg} = R_g \frac{N_1}{N_2} I_{pk}. \tag{6.16}$$

To maintain the MOSFET in its pinch-off region, the voltage $v_{Rg}$ across $R_g$ is approximately by

$$v_{Rg} = V_{DRI} - V_{GS(th)} \tag{6.17}$$

where $V_{DRI}$ is the high-state output voltage produced by the driver IC in Figure 6.7 (a) and $V_{GS(th)}$ is the MOSFET's gate threshold voltage. If this result is put into (6.16) which is rearranged, then

$$I_{pk} = \frac{N_2(V_G - V_{GS(th)})}{N_1 R_g}. \tag{6.18}$$

After sufficient time is allowed for the turn-on action to elapse, Output B goes high. This clamps the MOSFET's gate to $V_{DRI}$ via a low impedance route. It also allows $i_2$ to circulate in the short-circuit loop, Loop 2, for the rest of the MOSFET's on-time. This minimises the current driven into the CT's magnetising branch. At turn-on in the fast-switching mode, Outputs A and B rise simultaneously, and the output terminals of the CT are again short-circuited.

When *TR*1 is off, Outputs A and B are low. When *TR*1 is off and also acting as the freewheeling device, the charge $Q_{oss}$ flows through the CT's primary winding when the complementary MOSFET turns on. Again, Outputs A and B present a short-circuit.

# 6.4. Experimental rig and results

## 6.4.1. Design of current transformer

The circuitry in Figure 6.6 and Figure 6.7 was prototyped. CT1 and CT2 were each assembled with a TN9/6/3 toroidal core in 3F3 material, and with $N_2$ formed with 50 turns of 0.2-mm diameter copper wire. The primary conductor was passed once through the CT's aperture giving $N_1$ = 1. As the parameters of the CT are now determined, the magnetising inductance of the CT can be calculated.

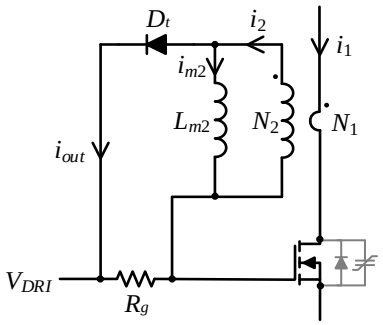



*Figure 6.8 Current transformer in Figure 6.6 with its magnetising branch.*

As shown in Figure 6.8, $L_{m2}$ represents the magnetising branch of the CT referred to the secondary side. $i_{m2}$ is the magnetising current. $L_{m2}$ is calculated from

$$L_{m2} = \frac{A_e \mu_0 \mu_r N_2^2}{l_e} \tag{6.19}$$

where the effective length $l_e$ = 22.9 mm, effective area $A_e$ = 4.44 mm$^2$, relative permeability $\mu_r$ = 1800 according to the manufacturer's datasheet. The magnetic permeability of free space $\mu_0 = 4\pi \times 10^{-7}$ H/m. $N_2$ = 50 turns. Putting the data into (6.19) gives $L_{m2}$ = 1.097 mH.

$i_{m2}$ will build up in $L_{m2}$ when the SJ MOSFET in Figure 6.8 is on and there is current flowing in the primary side of the CT. The peak current $i_{m2(\text{peak})}$ reached by $i_{m2}$ is given by

$$i_{m2(peak)} = \int_0^T \frac{V_{Rg}}{L_{m2}} dt. \tag{6.20}$$

If $V_{DRI}$ = 15 V and $V_{GS(th)}$ is approximately 3 V then, according to (6.17), $V_{Rg}$ is 12 V. $T$ is pessimistically estimated at 1 µs to control a worst-case switching transient. Putting the data into (6.20) yields $i_{(m2)peak}$ = 10.9 mA. Compared with the ideal secondary current, the current in the magnetising branch can be neglected without an appreciable loss in accuracy.

In [128], a CT is used to measure the drain current of a 10-kV SiC MOSFET for over-current monitoring purposes. The CT's primary current in [128] has a low-frequency component, and the core is consequently gapped to avoid saturation. The primary currents in the CTs in Figure 6.6 also have a low-frequency component. However, these currents are in the form of a series of return-to-zero pulses and the core can be reset between pulses. An un-gapped core can therefore be used without saturation occurring. As seen in Figure 6.6 and Figure 6.7, the CT is operated without discrete reset circuitry, and reset occurs by means of the resonant action between the magnetizing inductance and the CT's parasitic capacitance during the MOSFET's off-times [129].

### 6.4.2. Design of other components in the circuit

$R_g$ was varied experimentally to set $I_{pk}$, as determined by (6.18). Key data for the bridge-leg and gate driver circuits are given in Table 6.1 and Table 6.2. $D_r$ and $D_f$ are signal diodes and $D_t$ must be sized to support the peak secondary voltage which occurs when MOSFET turns off, so it needs to be a high voltage diode. Then Schottky diode GB01SLT12-214 with breakdown voltage of 1200 V is selected.

*Table 6.1 Bridge-Leg Components for Circuitry in Figure 6.6.*

| | |
|---|---|
| $D_{ext1,2}$ | SCS220AE |
| *TR*1, 3 | IPW60R041P6 |
| *TR*2, 4 | IRFB7546PBF |

*Table 6.2 Driver Circuit Components for Circuitry in Figure 6.7.*

| | |
|---|---|
| $R_r$ | 10 Ω |
| $D_{r,f}$ | 1N4148TR |
| $D_t$ | GB01SLT12-214 |
| Driver IC | IXDN614SI |

### 6.4.3. Experimental circuitry for DC tests

Initially, DC tests were carried out using the simplified circuits in Figure 6.9 in order to evaluate the circuitry. The ancillary devices used with *TR*2 and CT1 in Figure 6.6 were omitted for these tests as they have little influence on the turn-on behaviour of *TR*2 in this mode. In each case, *TR*1 and *TR*2 were switched in a complementary manner, as occurs in the slow-switching mode. Consequently, the $C_{oss}$ of *TR*1 is fully discharged when *TR*2 is off. For simplicity, a MBR3060CT Schottky diode was used as the anti-series element in these tests instead of a MOSFET as shown in Figure 6.6. The supply voltage $V_{dc}$ was 400 V. The gate driver circuits for *TR*1 and *TR*2 applied an on-state gate-source voltage $v_{GS}$ of 12 V. The off-state $v_{GS}$ was -3 V, and it was negative to prevent d*v*/d*t*-induced simultaneous conduction through *TR*1 and *TR*2. The delay time *D* was defined as the interval between $v_{DRI}$ rising and $v_{DS2}$ falling to its 50%-level of 200 V.

Figure 6.10 shows the experimental hardware in DC tests. The CT is labelled and used the TN9/6/3 – 3F3 core described in Section 6.4.1.

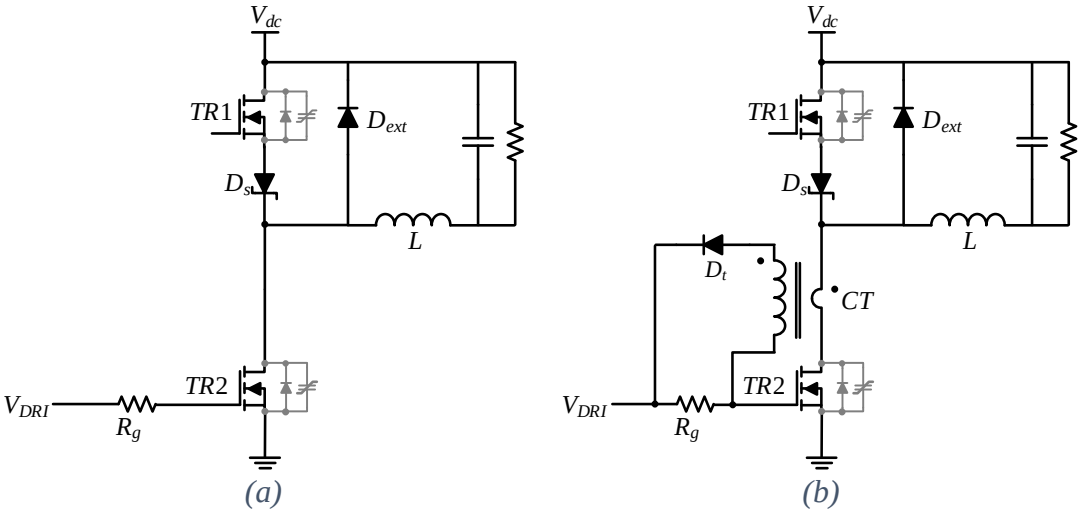



*Figure 6.9 Experimental circuits for evaluating methods for controlling incoming drain current profile into SJ MOSFET at turn-on. (a) Simple resistance in series with gate for charging SJ MOSFET input capacitance. (b) Negative feedback from current transformer.*

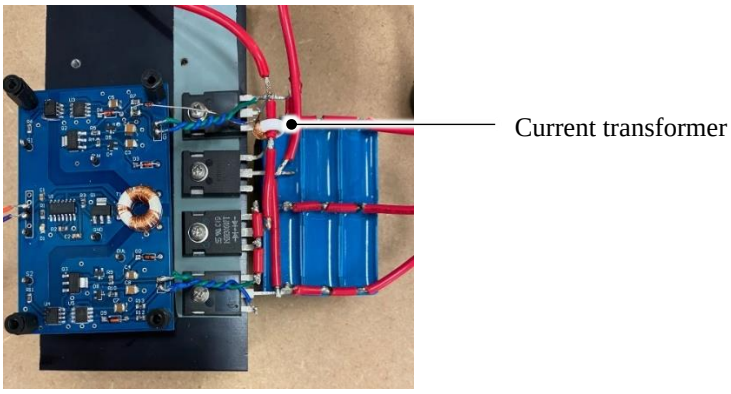



*Figure 6.10 Experimental hardware in DC tests with labelled current transformer.*

### 6.4.3.1. Tests with simple resistor in series with MOSFET's gate terminal

$R_g$ in Figure 6.9 (a) was set at 160 Ω, 220 Ω, 300 Ω, and 360 Ω. Readings of turn-on energy dissipation $E_{on(tri)}$, peak current $I_{pk}$, and delay time $D$ were taken for $i_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A. Tables 6.3-6.6 show the experimental results.

Figure 6.11 shows exemplifying waveforms with various $R_g$ when $i_{LOAD}$ = 3 A. $w_{inst}$ is the instantaneous power dissipation in $TR2$ and was obtained by multiplying $i_{D2}$ and $v_{DS2}$ using the oscilloscope "MATH" function. The integral of $w_{inst}$ equals to turn-on energy dissipation $E_{on(tri)}$. Figure 6.12 shows the relationship between $E_{on(tri)}$ and $I_{os}$ for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A. Figure 6.13 shows the relationship between $E_{on(tri)}$ and

$I_{pk}$ for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A. Figure 6.14 shows the relationship between $E_{on(tri)}$ and $D$ for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A.

*Table 6.3 Experimental results of circuitry in Figure 6.9 (a) with $R_g$ = 160 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 13 | 9 | 1.07 |
| 3 | 11.95 | 8.95 | 1.06 |
| 2 | 10.7 | 8.7 | 1.05 |
| 1 | 9.25 | 8.25 | 1.04 |

*Table 6.4 Experimental results of circuitry in Figure 6.9 (a) with $R_g$ = 220 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 11.25 | 7.25 | 1.46 |
| 3 | 10.1 | 7.1 | 1.45 |
| 2 | 8.95 | 6.95 | 1.44 |
| 1 | 7.6 | 6.6 | 1.43 |

*Table 6.5 Experimental results of circuitry in Figure 6.9 (a) with $R_g$ = 300 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 9.65 | 5.65 | 1.97 |
| 3 | 8.75 | 5.75 | 1.96 |
| 2 | 7.25 | 5.25 | 1.93 |
| 1 | 6 | 5 | 1.91 |

*Table 6.6 Experimental results of circuitry in Figure 6.9 (a) with $R_g$ = 360 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 9.05 | 5.05 | 2.37 |
| 3 | 7.9 | 4.9 | 2.34 |
| 2 | 6.65 | 4.65 | 2.3 |
| 1 | 5.5 | 4.5 | 2.28 |

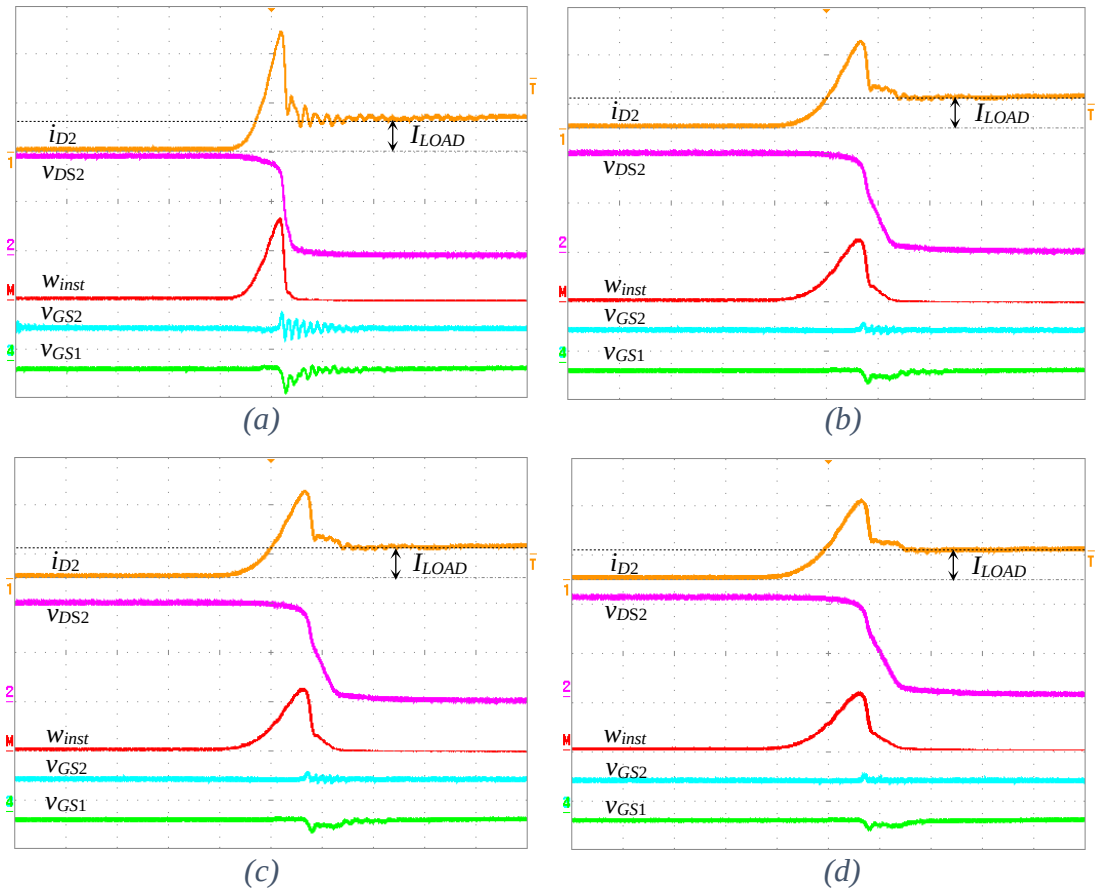



*Figure 6.11 Exemplifying waveforms from the scheme in Figure 6.9 (a) with (a) $R_g$ = 160 Ω; (b) $R_g$ = 220 Ω; (c) $R_g$ = 300 Ω; (d) $R_g$ = 360 Ω and $I_{LOAD}$ = 3 A. Scales: $i_{D2}$ = 5 A/div., $v_{DS2}$ = 200 V/div., $w_{inst}$ = 2.5 kW/div., $v_{DRI}$ = 20 V/div. Time scale = 200 ns/div.*

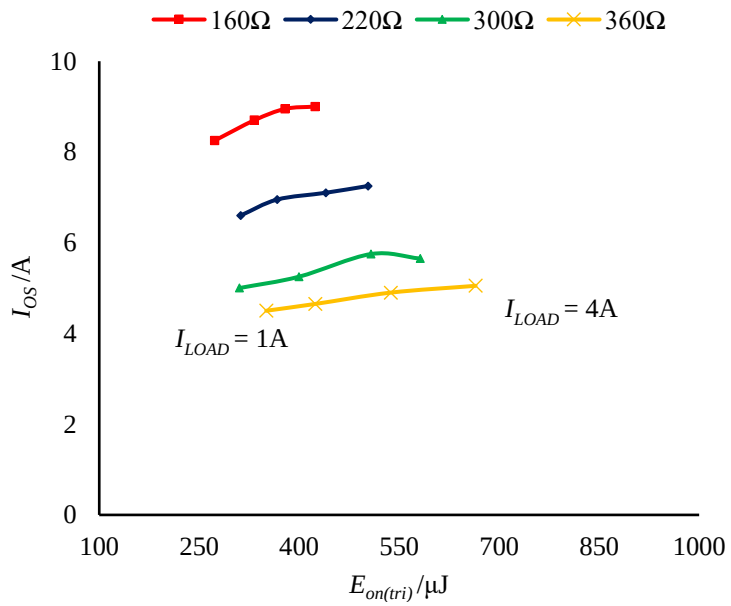



*Figure 6.12 Relationship between turn-on energy dissipation $E_{on(tri)}$ and overshoot current $I_{os}$.*

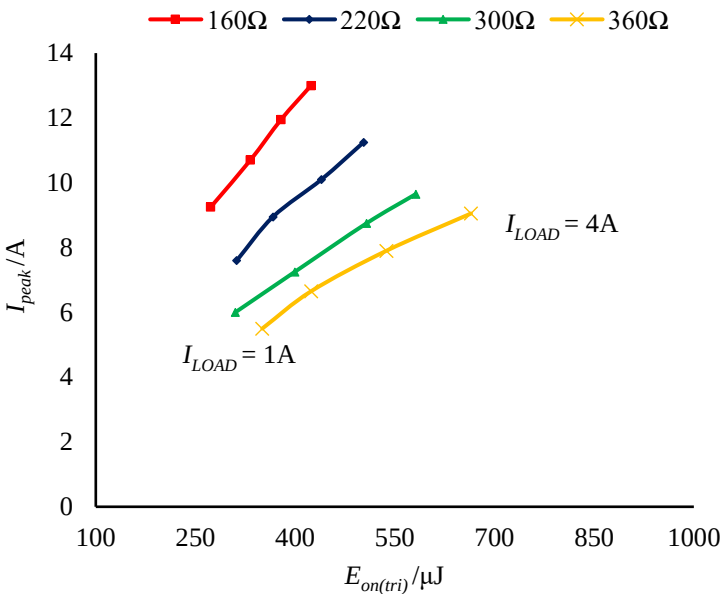



*Figure 6.13 Relationship between turn-on energy dissipation $E_{on(tri)}$ and peak current $I_{pk}$.*

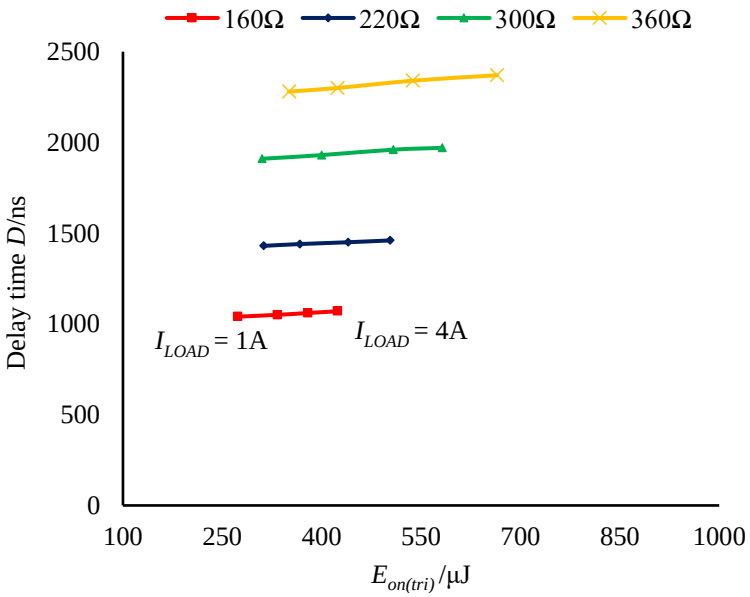



*Figure 6.14 Relationship between turn-on energy dissipation $E_{on(tri)}$ and delay time $D$.*

### 6.4.3.2. Tests with CT arrangement

$R_g$ in Figure 6.9 (b) was set at 39 Ω, 47 Ω, 56 Ω, and 68 Ω. Readings of turn-on energy dissipation $E_{on(rec)}$, peak current $I_{pk}$, and delay time $D$ were taken for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A. Tables 6.7-6.10 show the experimental results of them. Figure 6.15 shows exemplifying waveforms with various $R_g$ when $I_{LOAD}$ = 3 A. Figure 6.16 shows the relationship between $E_{on(rec)}$ and $I_{os}$ for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A. Figure 6.17

shows the relationship between $E_{on(rec)}$ and $I_{pk}$ for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A. Figure 6.18 shows the relationship between $E_{on(rec)}$ and $D$ for $I_{LOAD}$ = 1 A, 2 A, 3 A, and 4 A.

*Table 6.7 Experimental results of circuitry in Figure 6.9 (b) with $R_g$ = 39 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 9.65 | 5.65 | 386 |
| 3 | 9.65 | 6.65 | 362 |
| 2 | 9.35 | 7.35 | 348 |
| 1 | 9.15 | 8.18 | 338 |

*Table 6.8 Experimental results of circuitry in Figure 6.9 (b) with $R_g$ = 47 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 7.9 | 3.9 | 474 |
| 3 | 7.9 | 4.9 | 444 |
| 2 | 7.6 | 5.6 | 414 |
| 1 | 7.35 | 6.35 | 396 |

*Table 6.9 Experimental results of circuitry in Figure 6.9 (b) with $R_g$ = 56 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 6.75 | 2.75 | 606 |
| 3 | 6.75 | 3.75 | 536 |
| 2 | 6.65 | 4.65 | 502 |
| 1 | 6.45 | 5.45 | 474 |

*Table 6.10 Experimental results of circuitry in Figure 6.9 (a) with $R_g$ = 68 Ω.*

| Load current $I_{LOAD}$/A | Peak current $I_{pk}$/A | Overshoot current $I_{os}$/A | Delay time $D$/ns |
|---|---|---|---|
| 4 | 5.7 | 1.7 | 824 |
| 3 | 5.9 | 2.9 | 674 |
| 2 | 5.7 | 3.7 | 604 |
| 1 | 5.6 | 4.6 | 566 |

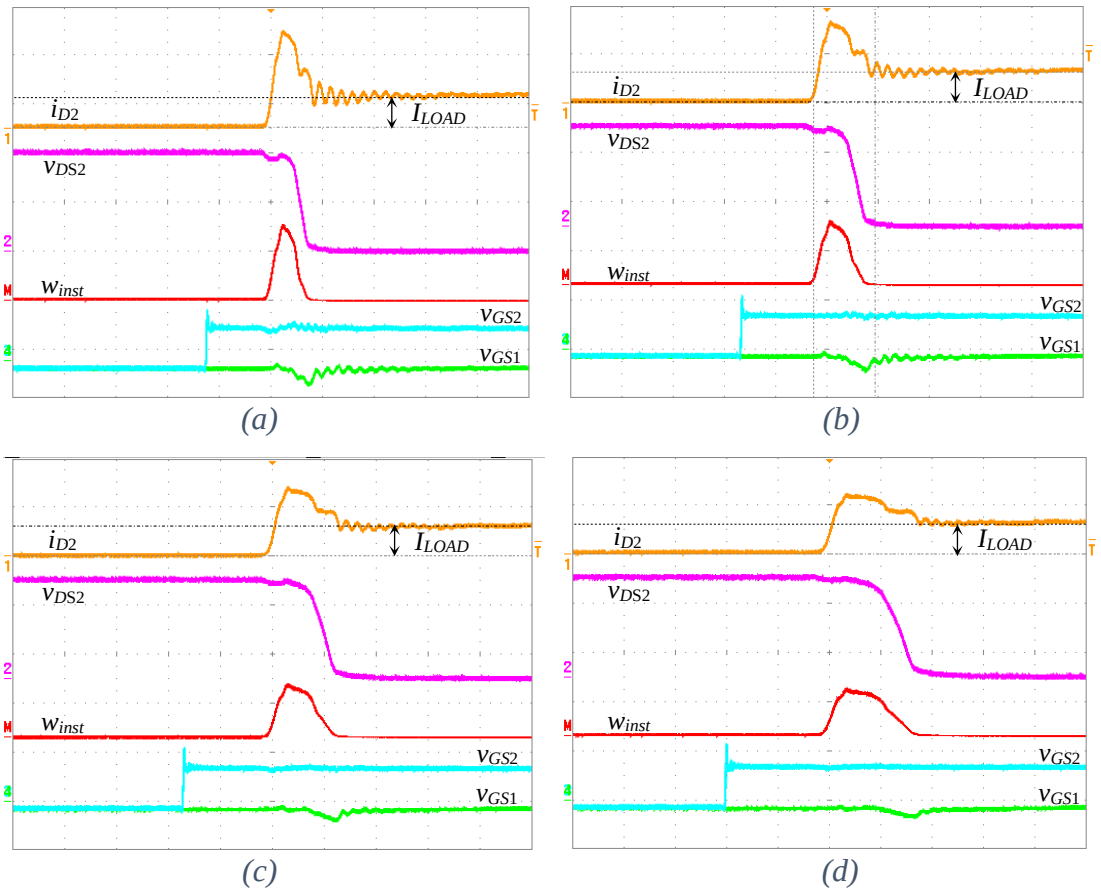



*Figure 6.15 Exemplifying waveforms from the CT scheme in Figure 6.9 (b) with (a) $R_g$ = 39 Ω; (b) $R_g$ = 47 Ω; (c) $R_g$ = 56 Ω; (d) $R_g$ = 68 Ω and $I_{LOAD}$ = 3 A. Scales: $i_{D2}$ = 5 A/div., $v_{DS2}$ = 200 V/div., $w_{inst}$ = 2.5 kW/div., $v_{DRI}$ = 20 V/div. Time scale = 200 ns/div.*

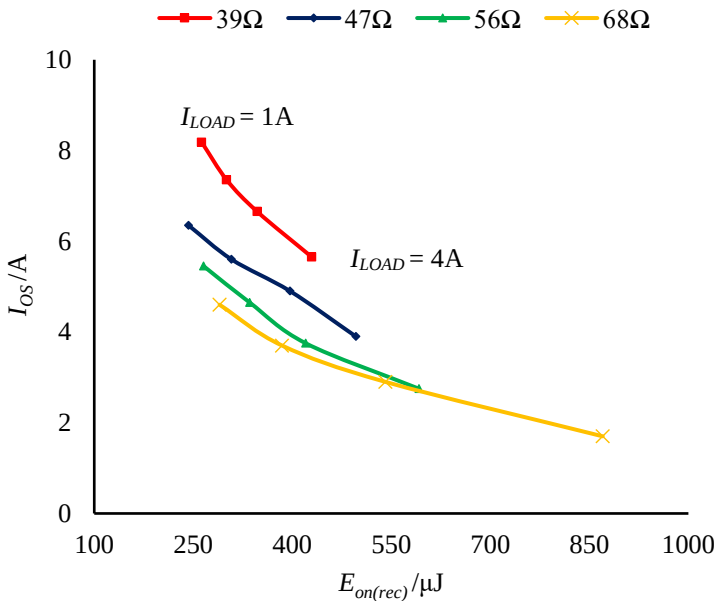



*Figure 6.16 Relationship between turn-on energy dissipation $E_{on(rec)}$ and overshoot current $I_{os}$.*

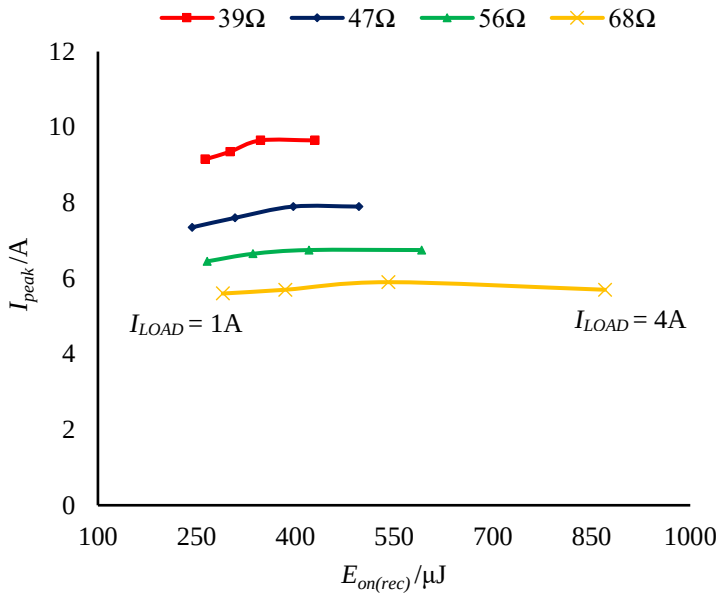



*Figure 6.17 Relationship between turn-on energy dissipation $E_{on(rec)}$ and peak current $I_{pk}$.*

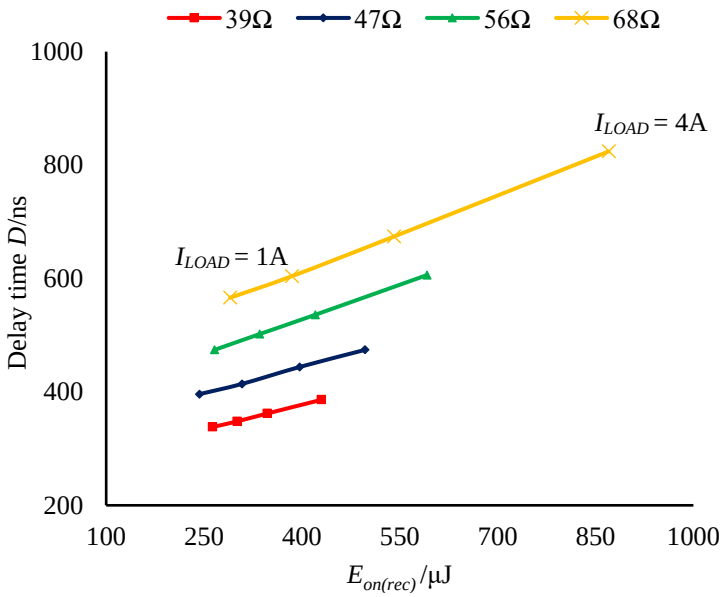


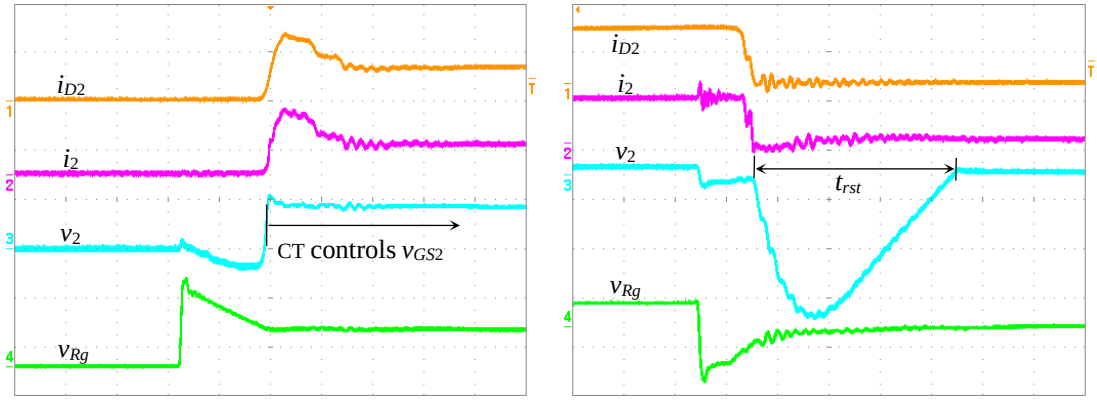

*Figure 6.18 Relationship between turn-on energy dissipation $E_{on(rec)}$ and delay time $D$.*

### 6.4.3.3. Waveforms from current transformer circuitry

Exemplifying waveforms from the CT circuitry in Figure 6.9 (b) were taken with $R_g$ = 56 Ω and $I_{LOAD}$ = 3 A. $i_2$ and $v_2$ are the CT's secondary current and voltage respectively.

Figure 6.19 (a) shows the waveforms when *TR*2 in Figure 6.9 (b) turns on. The peak magnetising current drawn by the CT during the transient turn-on period is very small,

and $i_2$ is consequently an accurate replica of the primary current $i_{D2}$ during this period. Figure 6.19 (b) shows the waveforms when *TR*2 in Figure 6.9 (b) turns off. The approximately half-sinusoidal oscillation of $v_2$ is due to the resonant action between the CT's magnetising inductance and parasitic lumped capacitance during reset. The half-sinusoidal oscillation elapses over a time $t_{rst}$ which was 816 ns.




*(a)* *(b)*

*Figure 6.19 Exemplifying waveforms from the circuitry in Figure 6.9 (b) with $R_g$ = 56 Ω and $I_{LOAD}$ = 3 A. (a) at TR2 turn-on (b) at TR2 turn-off. Scales for (a): $i_{D2}$ = 5 A/div., $i_2$ = 0.1 A/div., $v_2$ = 10 V/div., $v_{Rg}$ = 10 V/div. Scales for (b): $i_{D2}$ = 5 A/div., $i_2$ = 0.1 A/div., $v_2$ = 40 V/div., $v_{Rg}$ = 10 V/div. Time scale for both = 200 ns/div.*

### 6.4.3.4. Comparison of results

Figure 6.20 shows turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ plotted against overshoot current $I_{os}$ at load current $I_{LOAD}$ = 3 A. Figure 6.21 shows $E_{on(tri)}$ and $E_{on(rec)}$ plotted against delay time $D$, also at $I_{LOAD}$ = 3 A. In Figure 6.20, under the same $I_{os}$, the turn-on energy dissipation $E_{on(rec)}$ of the rectangular trajectories is less than that of the triangular trajectories $E_{on(tri)}$. When $R_g$ is made smaller, both $E_{on(tri)}$ and $E_{on(rec)}$ decrease and $I_{os}$ increase consequently. In Figure 6.21, the $D$ of the rectangular trajectories only has magnitudes of hundreds of nanoseconds, but the $D$ of the triangular trajectories is greater.

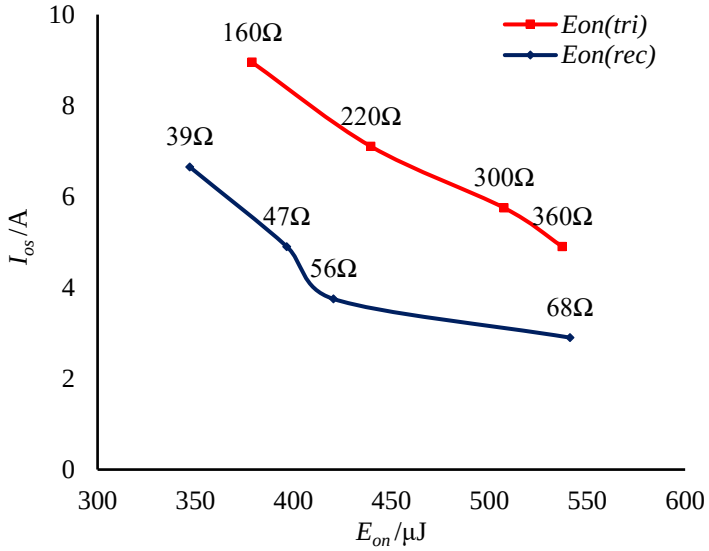



*Figure 6.20 Turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ shown against overshoot current $I_{os}$ for a load current of 3 A.*

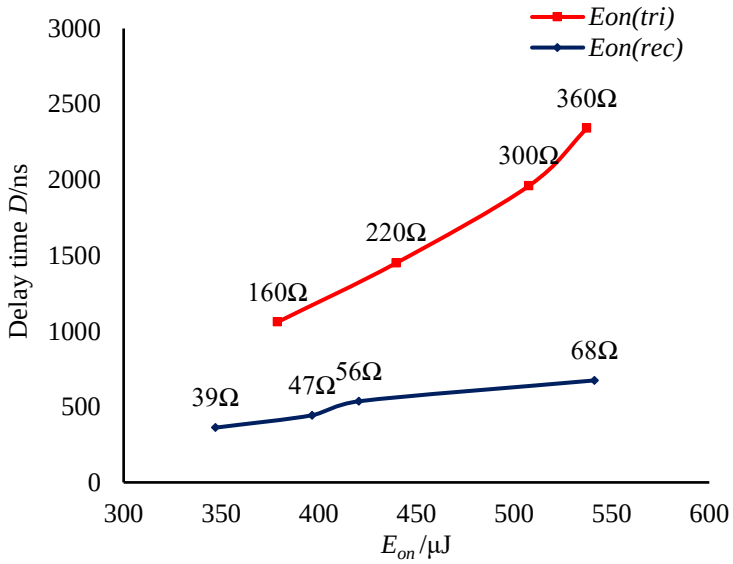
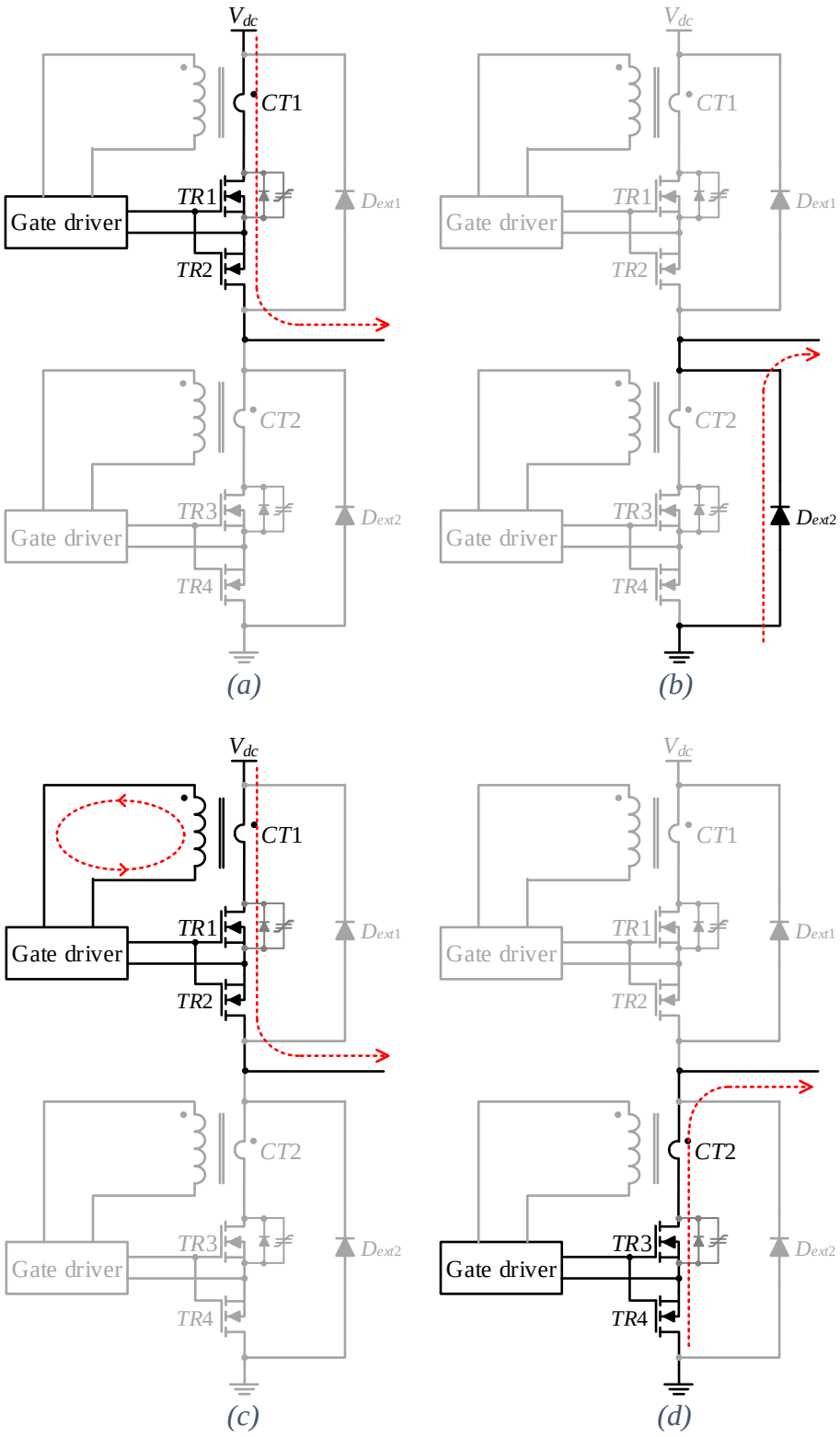



*Figure 6.21 Turn-on energies $E_{on(tri)}$ and $E_{on(rec)}$ shown against delay time D for a load current of 3 A.*

## 6.4.4. Experimental circuitry for AC tests

AC tests were carried out using the bridge-leg in Figure 6.6. The gate driver was adapted to the scheme in Figure 6.7 (a). Switching signals were generated according to Figure 6.7 (b), where the delay in the slow-switching mode was 1 µs and the deadtime was set as 500 ns at 20 kHz. The CY8C5868AXI-LP035 type of PSoC was selected to realise the dual-mode switching signals with CT schemes under AC tests. The key code and TopDesign in *PSoc Creator* can be found in Appendix C.

The eight different circuit operating states are shown in Figure 6.22, where the active components in each state are highlighted in black. Details of the operating states are explained in Table 6.11 Operation status of the bridge-leg in Figure 6.6 under AC tests..



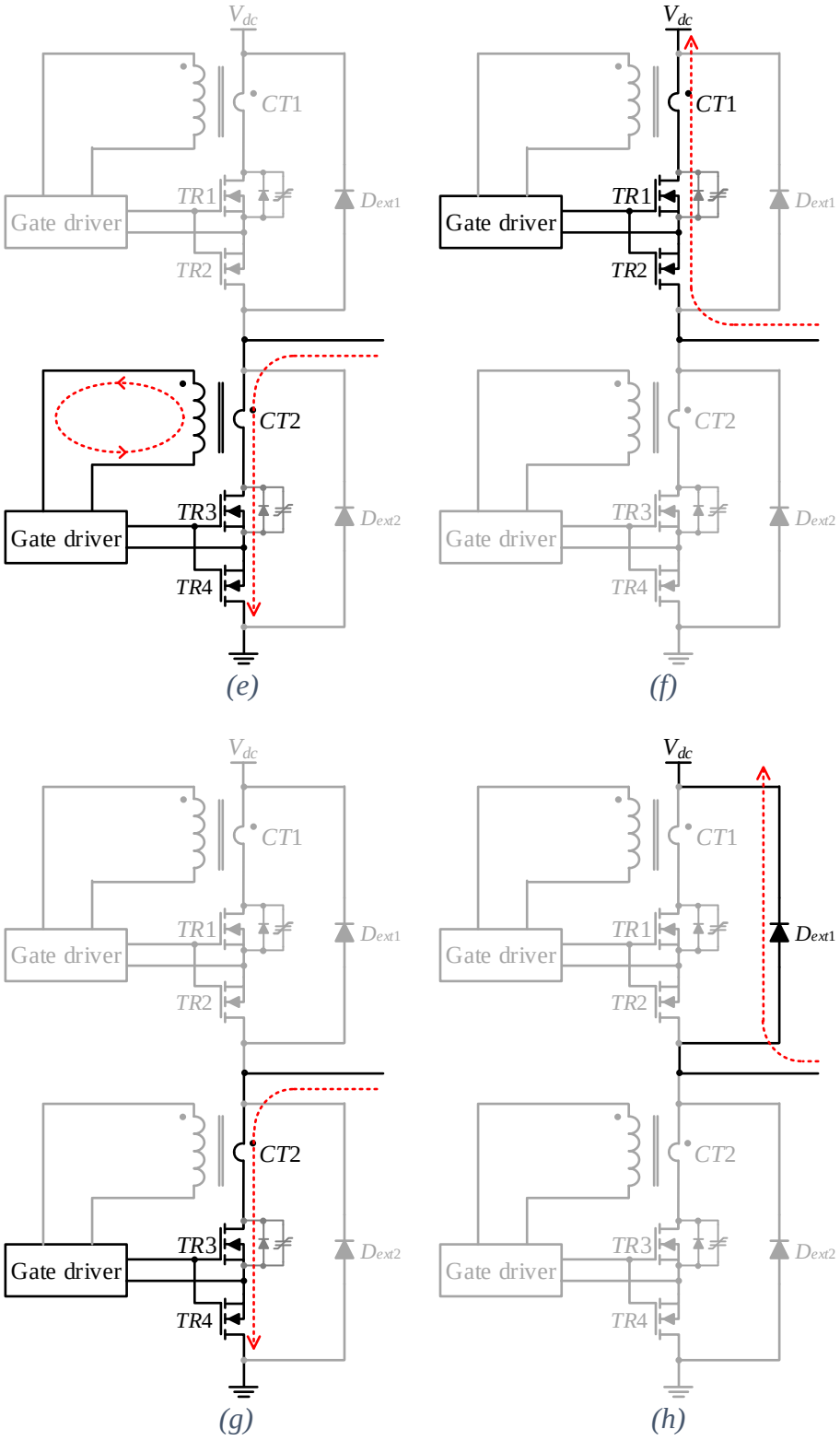
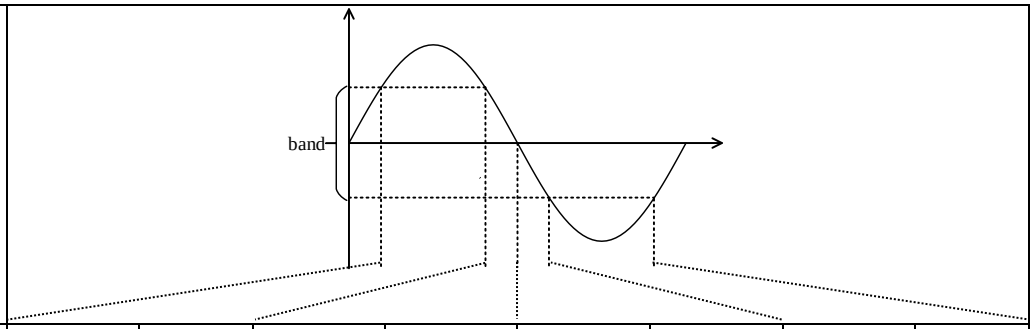



*Figure 6.22 Circuit operation status of the bridge-leg in Figure 6.6 under AC tests. Details are explained in Table 6.11.*

*Table 6.11 Operation status of the bridge-leg in Figure 6.6 under AC tests.*

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Load current |  | | | | | | | |
| Operation status | (a) | (b) | (c) | (d) | (e) | (f) | (g) | (h) |
| Polarity | Positive | | | | Negative | | | |
| Switching mode | Fast-switching | | Slow-switching | | Slow-switching | | Fast-switching | |
| Switches in operation | *TR*1,2 | | *TR*1,2 and *TR*3,4 | | | | *TR*3,4 | |
| Current transformer | Secondary CT1 short-circuit/ Loop 2 | - | Secondary CT1 in Loop1 | Secondary CT2 cut off by diode $D_t$ | Secondary CT2 in Loop1 | Secondary CT1 cut off by diode $D_t$ | Secondary CT1 short-circuit/ Loop 2 | - |

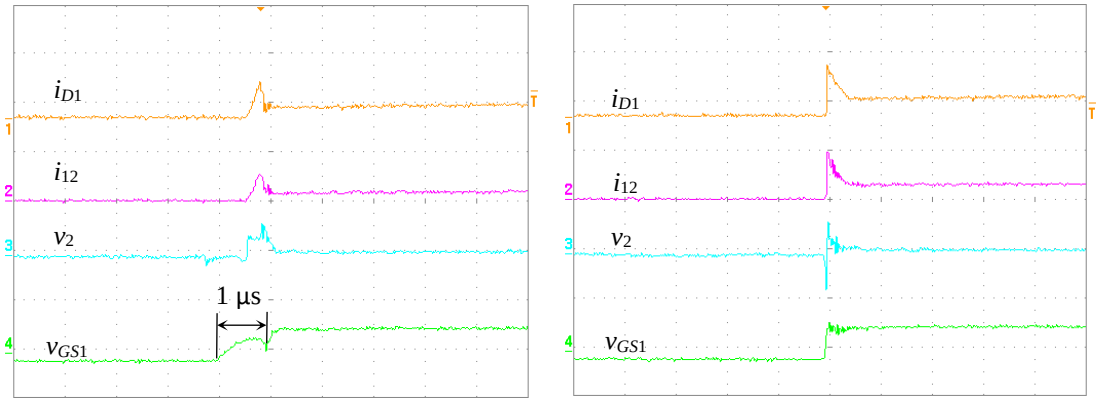
Under AC tests, the supply voltage $V_{dc}$ was 400 V. Two current transformers were the same as the one used in DC tests. Except for the components been listed in Table 6.1 and 6.2, the $R_g$ in Figure 6.7 was set as 56 Ω. The SSR was set as 0.5, which was selected based on two considerations. One, the band for slow-switching mode (as illustrated in Table 6.11) is wide enough to make sure there is no discontinuous load current during the whole switching period; Two, no significant efficiency drop was found when SSR increased from 0.1 to 0.5 in Chapter 4, so the losses that may be associated with the increased SSR is tolerated. A series connected *RL* load of 0.8 kVA was supplied. The load was at a power factor *PF* close to one.

Figure 6.23 (a) shows the waveforms when the load current is measured as 1.88 A, where $i_{D1}$ is the drain current of the *TR*1, $i_{12}$ is the secondary current of CT1, $v_2$ is the secondary voltage of CT1, $V_{GS1}$ is the gate-source voltage of *TR*1. The *TR*1 is in slow-switching mode as in operation status (c). The 1 μs delay in slow-switching mode is identified on $v_{GS}$. During this delay, there is a 8.32 V voltage stage of $v_2$ established by the $R_g$ in the secondary of CT1, which limit the peak of the $i_{D1.}$ After 0.36 μs, the $i_{D1}$ drops to the load current then $v_2$ starts to decline.

Figure 6.23 (b) shows the waveforms when the load current is measured as 3.70 A. The *TR*1 is in the fast-switching mode as in operating state (d). Compared with Figure

6.23 (a), $i_{D1}$ has a triangular trajectory while the $i_{D1}$ in Figure 6.23 (a) has a rectangular trajectory.

Exemplifying waveforms of different operation status were recorded from the oscilloscope as in Figure 6.24, where $i_{D1}$ is the drain current of the *TR*1, $i_{12}$ is the secondary current of CT1, $v_{Dext1}$ is the voltage across the external diode $D_{ext1}$, $v_{GS1}$ is the gate-source voltage of *TR*1. Figure 6.24 (a) demonstrates the operation (a) and (b), where the fast-switching mode is enabled. The drop of $i_{12}$ in Figure 6.24 (a) is caused by the magnetising current of the CT1. Figure 6.24 (b) demonstrates the operation (c) and (d) with the slow-switching mode enabled and load current is still positive. In Figure 6.24 (c), the load current across the zero and the bridge-leg is in synchronous conduction mode which demonstrates operation (c), (d), (e) and (f). Figure 6.24 (d) demonstrates the operation (e) and (f) with slow-switching mode enabled and load current is negative. In Figure 6.24 (e), there is no current flowing through *TR*1 and CT1 is because *TR*1 in this situation is held off with only *TR*3,4 operating, which is the demonstration of operation (g), (h). Figure 6.24 (f) shows the overall sinusoidal current waveforms.




*(a)* *(b)*

*Figure 6.23 Exemplifying waveforms (a) when load current is 1.88 A and TR1 is in slow-switching mode. (b) when load current is 3.70 A and TR1 is in fast-switching mode. Scales: $i_{D1}$ = 10 A/div., $i_{12}$ = 250 mV/div., $v_2$ = 20 V/div., $v_{GS1}$ = 20 V/div. Time scale = 1 µs/div.*

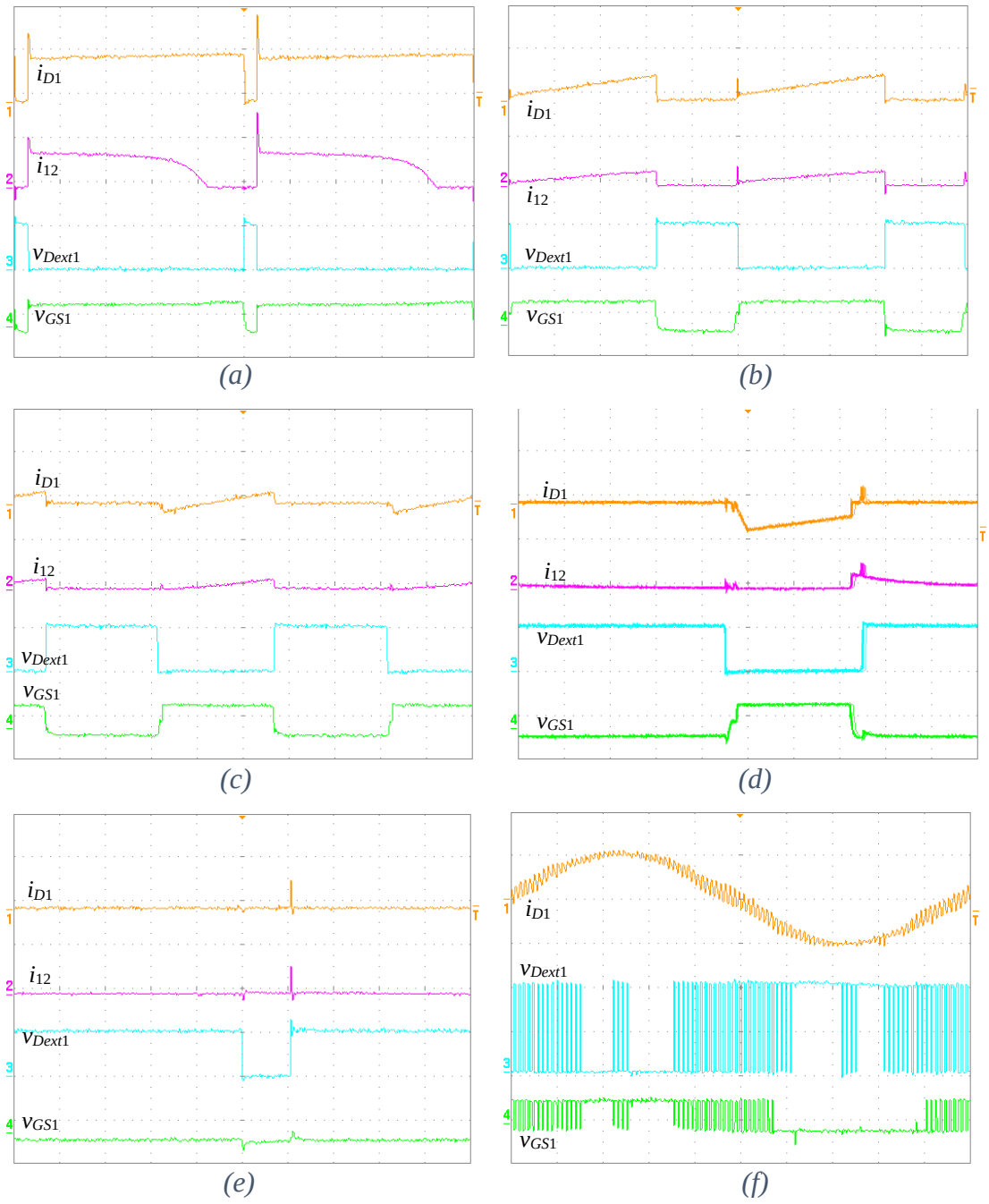
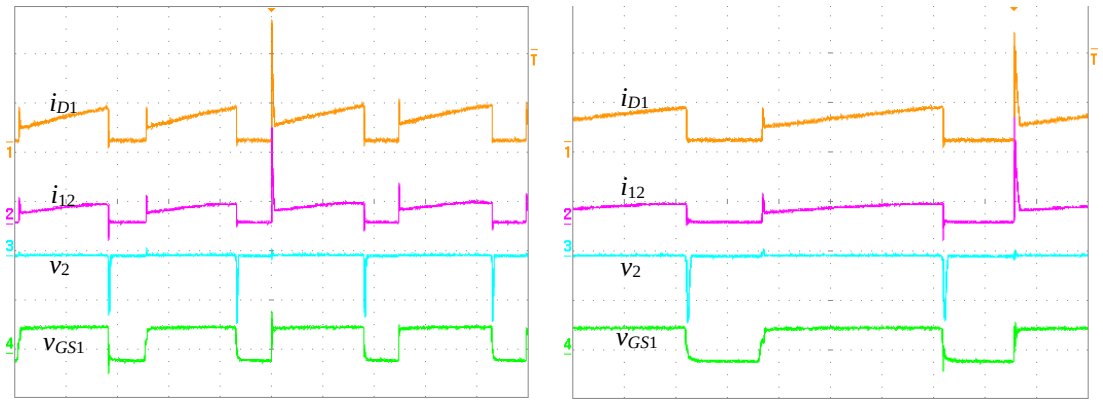



*Figure 6.24 Exemplifying waveforms of operation status in Figure 6.22. Scales: $i_{D1}$ = 10 A/div., $i_{12}$ = 250 mV/div., $v_{Dext1}$ = 200 V/div., $v_{GS1}$ = 20 V/div. (a, b, c) Time scale = 10 µs/div. (d, e) Time scale = 5 µs/div. (f) Time scale = 2 ms/div.*




*(a)* *(b)*

*Figure 6.25 Exemplifying waveforms of transition between operation status. Scales: $i_{D1}$ = 10 A/div., $i_{12}$ = 250 mV/div., $v_2$ = 100 V/div., $v_{GS1}$ = 20 V/div. (a) Time scale = 20 μs/div. (b) Time scale = 10 μs/div.*

The transition between the fast-switching and slow-switching modes was also recorded by oscilloscope and shown in Figure 6.25. Figure 6.25 (a) and (b) both show the transition between fast-switching and slow-switching with a positive load current, more specifically, the transition between operation (a), (b) and operation (c), (d). The transition happens when the load current was around 2.7 A. The peak current of last slow-switching cycle has a magnitude of 6.25 A, which shows good agreement with the results in Figure 6.17. The first switching cycle entering fast-switching after slow-switching has a current spike, which never appears before or after. This spike is caused by the charging of the *TR*3's $C_{oss}$, which was fully discharged in last slow switching cycle. Thereafter, this $C_{oss}$ is only partially discharged each cycle. When measured by the scope, the spike can reach 18 A even higher than the peak of maximum load current which was 15 A. However, it only appears once for each SJ MOSFET every base-frequency cycle, so its influence on efficiency and EMI is moderate.

## 6.5. Discussion

The following points are noted.

- A conventional gate driver and a gate driver with negative feedback applied to the gate signal by means of a CT have been compared. Improved trade-offs between incoming peak current, turn-on power dissipation, and delay time are obtained with the latter.

- Both the conventional and CT circuits are simple, without features such as stepped gate voltage waveforms. The proposed circuitry does not use active gate control [127], [130], and standard gate driver ICs can be used. Whilst the CT is an additional component, it uses a low-cost, compact, and un-gapped toroidal core with no safety-isolation requirements.
- Whilst the turn-on loss is reduced for a given overshoot current and propagation delay time, it is noted that a loss is incurred by the CT's secondary current flowing through the diodes $D_t$ and $D_f$ in Figure 6.7 (a) when the MOSFET is conducting. Both losses have to be evaluated in a practical converter design.

## 6.6. Conclusion

A gate driver circuit for super-junction MOSFETs in voltage source bridge-legs has been presented. The circuit controls the MOSFETs' incoming drain current profiles. Compared to conventional driver circuits, an improved trade-off between the incoming peak current, turn-on power dissipation, and delay time has been demonstrated. Further work will entail modelling the switching action to address the non-idealises of the proposed scheme. This will allow the turn-on trajectories of the MOSFET's drain current and drain-source voltage to be predicted more accurately.

# Chapter 7
# Conclusion

## 7.1. Conclusion

Converter efficiency maximisation is a driving factor in the power electronics industry, for high-efficiency power conversion has benefits of minimising energy consumption, reducing costs, and realising high power densities. These benefits make high-efficiency conversion important in applications such as renewable energy systems, and hybrid and electric vehicles. In order to achieve high efficiency and low overall losses, power semiconductor device options include wide band-gap (WBG) devices such as SiC MOSFETs and GaN HEMTs, and silicon super-junction (SJ) devices, of which the SJ MOSFET is well established. Whilst exhibiting excellent performance against many criteria [21], WBG devices are costly and exhibit practical application issues. For example, d$v$/d$t$-induced conduction and gate threshold shift can be problems with the SiC MOSFET [37]. Conversely, the silicon SJ MOSFET has a low on-state resistance $R_{DS(on)}$, is fast-switching and exhibits good short-circuit withstand times [47]. The SJ MOSFET also offers a high degree of manufacturability and established reliability [42].

SJ MOSFETs perform well in single-ended power converters when switching in conjunction with SiC Schottky diodes operating as the freewheeling element [50]. However, the reverse recovery behaviour of the intrinsic diode and the non-linear output capacitance $C_{oss}$ of the SJ MOSFET present challenges when used in voltage source converters (VSCs). The reverse recovery charge of the intrinsic diode is significant when the SJ MOSFET operates as a freewheeling device. Furthermore, the

non-linear $C_{oss}$ causes excessive-high d$v$/d$t$, especially at high voltage, which may lead to EMI or induce parasitic oscillations and potentially destroy the device [27].

The research undertaken in this thesis has addressed these problems. In order to develop a solution with simple hardware, no auxiliary magnetic components and no onerous timing requirements, a dual-mode switching technique was proposed in Chapter 4. In Chapter 5, the performance of this technique was investigated with alternative power device permutations. The dual-mode switching technique was further investigated in Chapter 6 with the current transformer (CT) scheme. The dual-mode switching technique, with or without a CT scheme, achieves high efficiency with minimal additional hardware. The transition conditions between the two switching modes has a wide allowable range when maintaining a satisfactory efficiency, so the technique presents no challenging control or sensing requirements.

The key contributions of the thesis are summarised as follows.

- A dual-mode switching control technique was proposed to address the disadvantages of the output capacitance when using SJ MOSFETs in VSCs. This technique operates in conjunction with intrinsic diode deactivation circuitry. The technique was demonstrated in an 800-W inverter-leg configuration operating from a 400-V DC supply voltage and switching at 20 kHz. The full-load efficiency reached approximately 98.7%, against a measured benchmark efficiency of 97.5% when using conventional fast-switching silicon IGBTs and fast recovery diodes. No forced cooling was needed.

- A dual-mode gate driver was designed to realise the dual-mode switching technique. In the driver circuit arrangement, two different paths are set: a slow-switching path and a fast-switching path. The fast-switching path is active only when the enable signal is on. When the slow-switching mode is selected, only the slow-switching driver operates and the SJ MOSFET's input capacitance is charged at turn-on via the relatively high-value resistance $R_s$. When the fast-switching path is enabled, the gate is charged more rapidly via the parallel combination of $R_s$ and the much smaller resistance $R_f$.

- The dual-mode switching technique addresses the detrimental influence of the SJ MOSFET's output capacitance and functions in conjunction with intrinsic diode deactivation circuitry. This circuitry uses two ancillary power devices connected around each SJ MOSFET. The selection of these devices when using the dual-mode switching technique was addressed, and practical experimental results for different device permutations were given. All the permutations were evaluated in a 1-kW inverter-leg operating at 420-V DC and switching at a series of frequencies from 15 kHz, 20 kHz, 25 kHz, 30 kHz up to 35 kHz. The full-load efficiency is evaluated for each scenario.
- MOSFET switching speeds are normally controlled by simply setting the device's external gate resistance to an appropriate value. This tends to yield a triangular incoming drain current profile. The peak incoming drain current in the MOSFET turning on can be limited by simply using a large resistance in series with its gate as in the slow-switching mode. However, this increases the power dissipation in the MOSFET. Furthermore, the turn-on propagation delay time is increased. A dual-mode switching technique with a current transformer (CT) scheme has been proposed to yield an approximately rectangular incoming drain current profile. An improved trade-off between the incoming peak current, turn-on power dissipation, and switching propagation delay time is attained.
- A gate driver circuit was developed to realise the dual-mode switching technique with a CT scheme that yields an approximately rectangular incoming drain current profile. SJ MOSFETs with proposed gate driver and conventional gate driver are used in 400-V bridge-leg and switched at 20 kHz. Triangular incoming drain current profile and rectangular incoming drain current profile are achieved by different gate drivers and compared when changing the value of gate resistances.

## 7.2. Future research

Based on the research results discussed in this thesis, some related research fields have been inspired. Extended applications of the proposed technique and different

experimental methods are also worth investigating in the future. Some key points of future work are summarised as follow:

### 7.2.1. Dual-mode switching technique

- The dual-mode switching technique was experimentally evaluated by SJ MOSFET based inverter-leg. The inverter-leg was operated under open-loop control with gate drive signals generated by the microcontroller. Therefore, a higher THD in outputs is expected than if the circuit were to be operated under closed-loop current control, as is normally the case in applications such as machine control.

- The load used in experiments was at a power factor close to one. No current sensing was incorporated into the proposed techniques. With variable power factors, a rudimentary form of current sensing would be required to inform the control circuitry which of the modes the circuitry should be operating in.

- The SJ MOSFET inverter-leg is a half-bridge topology, which can be easily extendable to a full-bridge or a three-phase inverter. With the same input power and modulation, the output voltage of the full-bridge inverter is double of the half-bridge. In a three-phase system, the three-time harmonics of the line-to-line voltage will be counteracted.

### 7.2.2. Alternative device permutations

- The exact determination of power losses is important for high-efficiency applications. Thermal superposition was used to measure the power dissipated by the power devices on a heatsink. Calorimetric methods allow the direct thermal measurement of losses occurring in the power electronics system [131-133]. If the circuitry is intended for use in machine-drive applications, and the quoted efficiencies therefore do not account for any choke losses, the thermal superposition method is suitable. If the circuitry is intended for use in other systems where choke losses are included, then the calorimetric method needs to be introduced. However, the calorimetric method is very costly to implement.

- Cryogenically-cooled power electronics systems expand in more and more applications, such as spacecraft-based electronic systems and superconducting

machines [65, 134-137]. The experiments of device permutations are conducted in the room temperature. Informed by these results, two of these permutations were selected for further evaluation in a system at 77 K [123]. Cryogenic temperature can cause significant change on the characteristics of different power electronics components and further investigation need to be conducted. It is noted that, unlike SiC devices, the SJ MOSFET's on-state resistance falls by typically a factor of five when operated at cryogenic temperatures. Whilst its breakdown voltage typically drops by 25%, the net effect is that improved efficiency is nonetheless attainable.

### 7.2.3. Control of incoming drain current profile

- Whilst the dual-mode switching technique with CT scheme is achieved by proposed gate driver and the turn-on loss is reduced for a given overshoot current and propagation delay time, a loss is incurred by the CT's secondary current flowing through the diodes $D_t$ and $D_f$ in Figure 6.7 (a) when the MOSFET is conducting. Both losses have to be evaluated in a practical converter design.

- Further work will entail modelling the switching action to address the non-ideal aspects of the proposed scheme. This will allow the turn-on trajectories of the MOSFET's drain current and drain-source voltage to be predicted more accurately.

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# Appendix A

# Experimental data

## A.1 Temperature measurements of inverter-leg in Figure 4.11 operating with different SSR

Similar to the previous scenario of inverter-leg in Figure 4.11 operating with SSR = 0.1, temperature measurements are recorded when inverter-leg is running with different SSR and complementary soft switching. Tables A.1, A.2, A.3, A.4, A.5, A.6 show the temperature measurements over time when the inverter-leg is operating with SSR = 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, respectively. The corresponding $D_{temp}$ is drawn in Figures A.1, A.2, A.3, A.4, A.5, A.6. Table A.7 shows the temperature measurements over time when the inverter-leg is driven under complementary soft switching, which equals to SSR = 1. The $D_{temp}$ of complementary soft switching is drawn in Figure A.7.

*Table A.1 Temperature measurements of inverter-leg in Figure 4.11 when SSR = 0.2.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 30.9 | 23.7 | 7.2 |
| 2 | 13 | 37.4 | 24.9 | 12.5 |
| 3 | 23 | 39.4 | 24.8 | 14.6 |
| 4 | 33 | 41.3 | 25.6 | 15.7 |
| 5 | 43 | 42.8 | 26.2 | 16.6 |
| 6 | 53 | 41.6 | 25.3 | 16.3 |
| 7 | 63 | 42.6 | 25 | 17.6 |
| 8 | 73 | 43.3 | 25.9 | 17.4 |
| 9 | 83 | 43.1 | 25.4 | 17.7 |

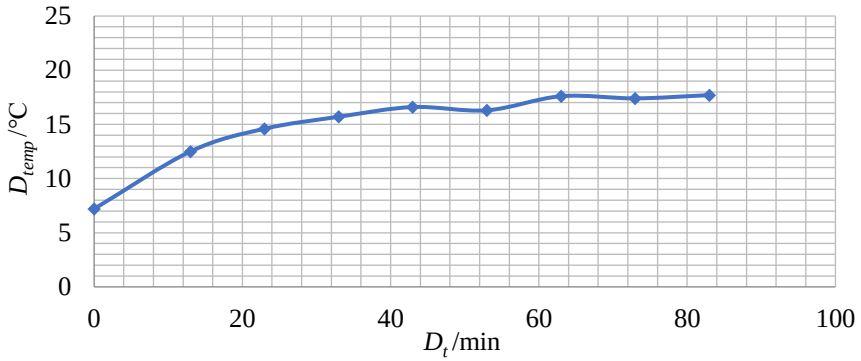



*Figure A.1 Temperature rise against time according to data in Table A.1.*

*Table A.2 Temperature measurements of inverter-leg in Figure 4.11 when SSR = 0.3.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 28.6 | 22.8 | 5.8 |
| 2 | 10 | 35.2 | 24.3 | 10.9 |
| 3 | 20 | 38.7 | 25 | 13.7 |
| 4 | 30 | 40.5 | 24.8 | 15.7 |
| 5 | 40 | 42.1 | 25.3 | 16.8 |
| 6 | 50 | 42.6 | 25 | 17.6 |
| 7 | 60 | 43.4 | 25.4 | 18 |
| 8 | 70 | 43.5 | 25.6 | 17.9 |
| 9 | 80 | 43.3 | 25.6 | 17.7 |

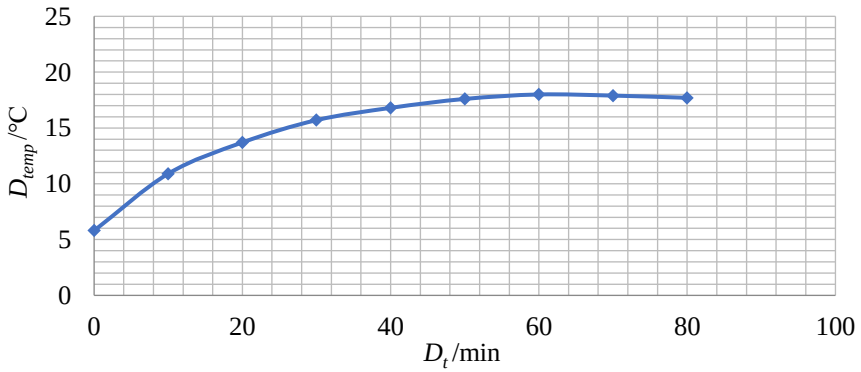



*Figure A.2 Temperature rise against time according to data in Table A.2.*

*Table A.3 Temperature measurements of inverter-leg in Figure 4.11 when SSR = 0.4.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 32.1 | 24.3 | 7.8 |
| 2 | 12 | 37.9 | 24.7 | 13.2 |
| 3 | 22 | 40.1 | 25.1 | 15 |
| 4 | 32 | 41.8 | 25.3 | 16.5 |
| 5 | 42 | 42.8 | 25.6 | 17.2 |
| 6 | 52 | 43.4 | 25.9 | 17.5 |
| 7 | 62 | 43.4 | 26.4 | 17 |
| 8 | 72 | 43.6 | 26.3 | 17.3 |

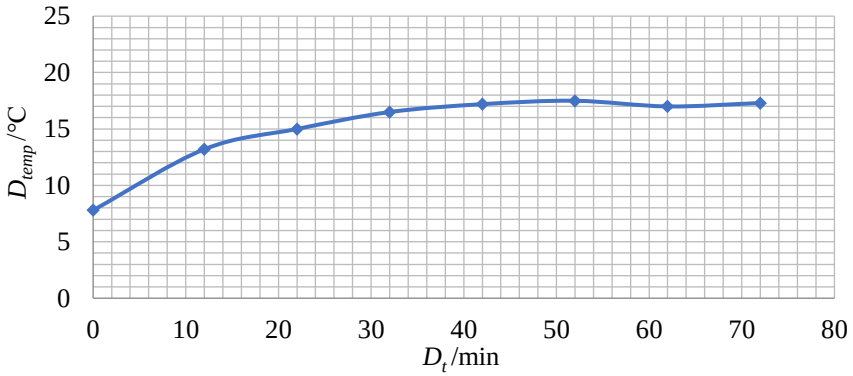



*Figure A.3 Temperature rise against time according to data in Table A.3.*

*Table A.4 Temperature measurements of inverter-leg in Figure 4.11 when SSR = 0.5.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 25.7 | 23.4 | 2.3 |
| 2 | 10 | 33.1 | 24.1 | 9 |
| 3 | 20 | 38.4 | 25.1 | 13.3 |
| 4 | 30 | 41.1 | 25.5 | 15.6 |
| 5 | 40 | 42.2 | 25.1 | 17.1 |
| 6 | 50 | 43.9 | 26 | 17.9 |
| 7 | 55 | 43.7 | 25.9 | 17.8 |
| 8 | 60 | 44.4 | 25.8 | 18.6 |
| 9 | 65 | 44.2 | 26.2 | 18 |

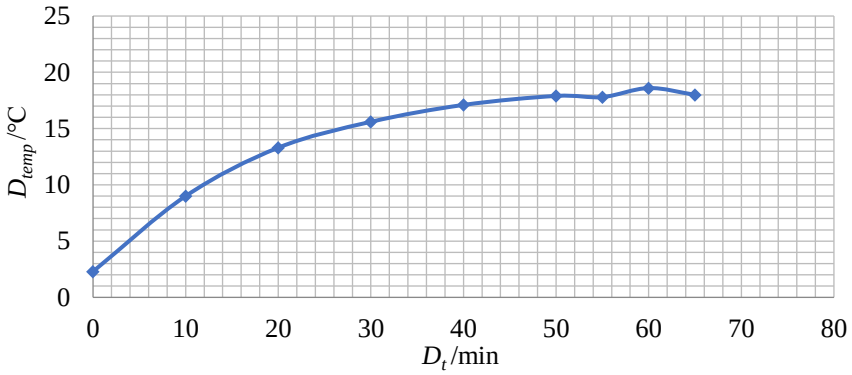



*Figure A.4 Temperature rise against time according to data in Table A.4.*

*Table A.5 Temperature measurements of inverter-leg in Figure 4.11 when SSR = 0.6.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 27.2 | 23.7 | 3.5 |
| 2 | 10 | 35.1 | 24.5 | 10.6 |
| 3 | 20 | 39.3 | 24.7 | 14.6 |
| 4 | 30 | 42.7 | 25.5 | 17.2 |
| 5 | 40 | 44.2 | 25.9 | 18.3 |
| 6 | 50 | 44.6 | 25.6 | 19 |
| 7 | 60 | 45.2 | 25.5 | 19.7 |
| 8 | 70 | 45.2 | 25.8 | 19.4 |

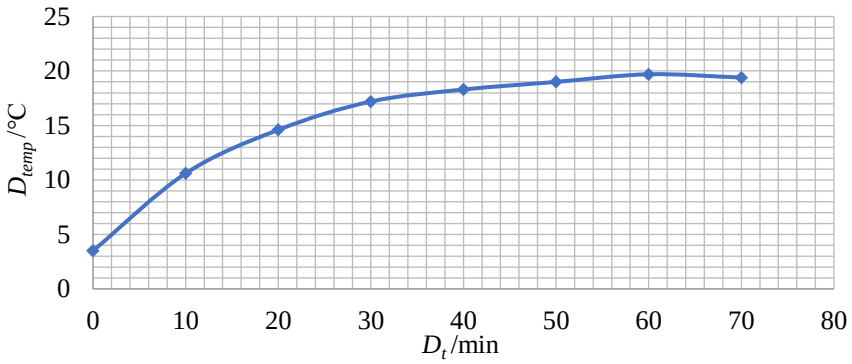



*Figure A.5 Temperature rise against time according to data in Table A.5.*

*Table A.6 Temperature measurements of inverter-leg in Figure 4.11 when SSR = 0.7.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 26.5 | 24.3 | 2.2 |
| 2 | 10 | 36.1 | 24.8 | 11.3 |
| 3 | 20 | 41 | 25 | 16 |
| 4 | 30 | 43.8 | 25.2 | 18.6 |
| 5 | 40 | 45.3 | 25.5 | 19.8 |
| 6 | 50 | 46.1 | 25.7 | 20.4 |
| 7 | 60 | 46.7 | 26.4 | 20.3 |
| 8 | 70 | 46.8 | 25.9 | 20.9 |

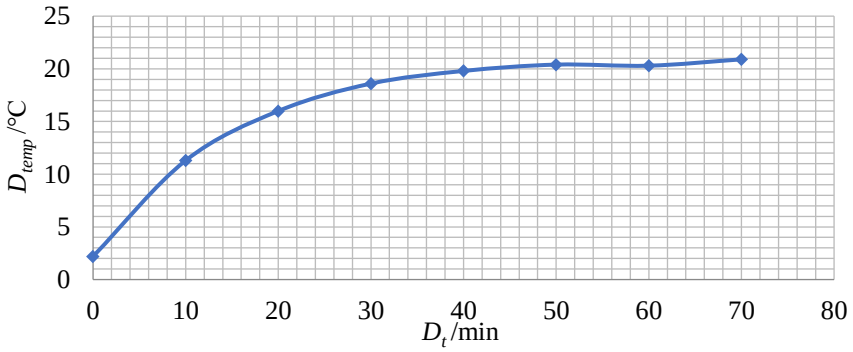



*Figure A.6 Temperature rise against time according to data in Table A.6.*

*Table A.7 Temperature measurements of inverter-leg in Figure 4.11 under complementary soft switching (SSR = 1).*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 31.8 | 23.5 | 8.3 |
| 2 | 10 | 42.2 | 24.7 | 17.5 |
| 3 | 20 | 47.4 | 24.9 | 22.5 |
| 4 | 30 | 50.2 | 25.7 | 24.5 |
| 5 | 40 | 51.2 | 25.5 | 25.7 |
| 6 | 50 | 52.2 | 25.4 | 26.8 |
| 7 | 60 | 52.9 | 25.7 | 27.2 |
| 8 | 70 | 53.2 | 26 | 27.2 |
| 9 | 80 | 53.2 | 25.8 | 27.4 |

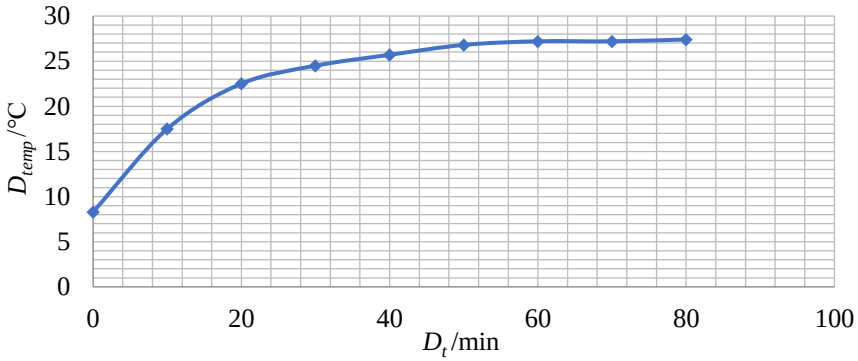



*Figure A.7 Temperature rise against time according to data in Table A.6.*

The temperature measurements of IGBT based inverter-leg in Figure 4.13 are shown in Table A.8. And Figure A.8 shows the curve of the $D_{temp.}$

*Table A.8 Temperature measurements with IGBT based inverter.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 42 | 25.4 | 16.6 |
| 2 | 12 | 49.6 | 24.3 | 25.3 |
| 3 | 22 | 54.7 | 25.4 | 29.3 |
| 4 | 42 | 59 | 25.1 | 33.9 |
| 5 | 52 | 59.6 | 25.7 | 33.9 |
| 6 | 62 | 59.9 | 25.9 | 34 |

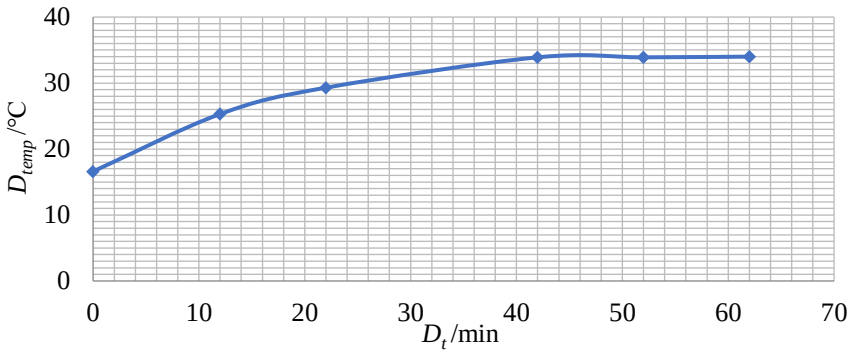



*Figure A.8 Temperature rise against time according to data in Table A.7.*

# A.2 Temperature measurements of alternative device modules in Figure 5.1 at different frequencies

## A.2.1 Temperature measurements of using Module (a) in inverter-leg

Temperature measurements are recorded when using Module (a) in an inverter-leg, as in Figure 5.3, and running at different frequencies. Tables A.9, A.10, A.11, A.12, A.13 show the temperature measurements over time when the inverter-leg is operating under the frequency of 15 kHz, 20 kHz, 25 kHz, 30 kHz, 35 kHz, respectively. The corresponding $D_{temp}$ is drawn in Figures A.9, A.10, A.11, A.12, A.13.

*Table A.9 Temperature measurements when Figure 5.3 switched at 15 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 31.7 | 23.1 | 8.6 |
| 2 | 12 | 37.9 | 23.2 | 14.7 |
| 3 | 23 | 41.4 | 24 | 17.4 |
| 4 | 34 | 43.3 | 24.5 | 18.8 |
| 5 | 47 | 43.5 | 24.3 | 19.2 |
| 6 | 60 | 44.4 | 24.8 | 19.6 |
| 7 | 74 | 45.1 | 25.2 | 19.9 |
| 8 | 80 | 45.4 | 25.1 | 20.3 |
| 9 | 90 | 46 | 26 | 20 |
| 10 | 100 | 45.9 | 26 | 19.9 |

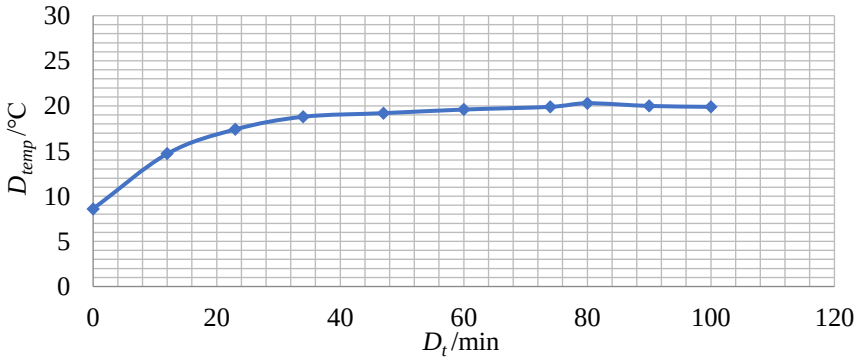



*Figure A.9 Temperature rise against time according to data in Table A.9.*

*Table A.10 Temperature measurements when Figure 5.3 switched at 20 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 38.2 | 23.3 | 14.9 |
| 2 | 21 | 45.9 | 25.4 | 20.5 |
| 3 | 30 | 45.9 | 25.2 | 20.7 |
| 4 | 40 | 47 | 25.5 | 21.5 |
| 5 | 50 | 47.4 | 25.9 | 21.5 |
| 6 | 60 | 48.8 | 26.2 | 22.6 |
| 7 | 70 | 48.4 | 25.8 | 22.6 |
| 8 | 80 | 48.1 | 25.9 | 22.2 |

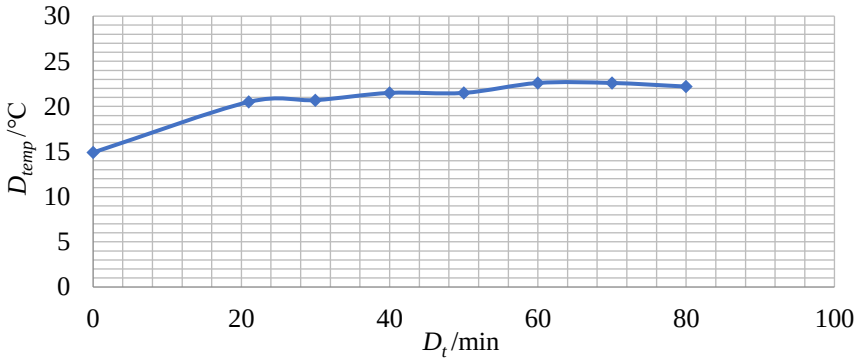



*Figure A.10 Temperature rise against time according to data in Table A.10.*

*Table A.11 Temperature measurements when Figure 5.3 switched at 25 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 45.7 | 26.2 | 19.5 |
| 2 | 10 | 48.9 | 26.2 | 22.7 |
| 3 | 24 | 50.6 | 25.7 | 24.9 |
| 4 | 34 | 50.5 | 26.2 | 24.3 |
| 5 | 44 | 51.6 | 26.3 | 25.3 |
| 6 | 54 | 51.8 | 26.3 | 25.5 |
| 7 | 64 | 51.6 | 26 | 25.6 |
| 8 | 74 | 51.9 | 26.7 | 25.2 |

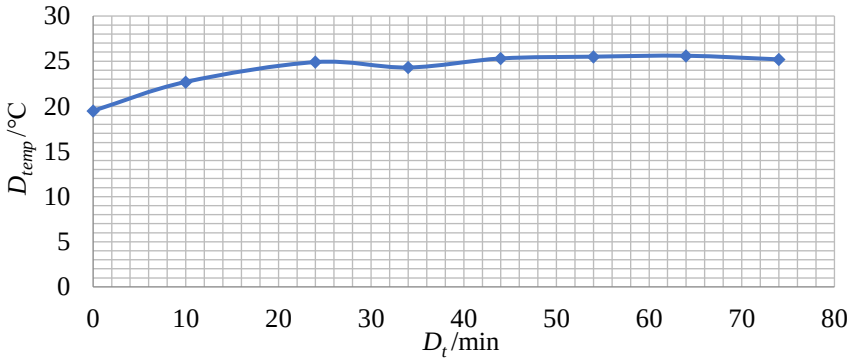



*Figure A.11 Temperature rise against time according to data in Table A.11.*

*Table A.12 Temperature measurements when Figure 5.3 switched at 30 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 47.9 | 26.3 | 21.6 |
| 2 | 10 | 51.8 | 26.2 | 25.6 |
| 3 | 20 | 52.4 | 26.5 | 25.9 |
| 4 | 32 | 53.3 | 26.4 | 26.9 |
| 5 | 40 | 54.3 | 26.5 | 27.8 |
| 6 | 50 | 53.4 | 26.2 | 27.2 |
| 7 | 60 | 55 | 26.9 | 28.1 |

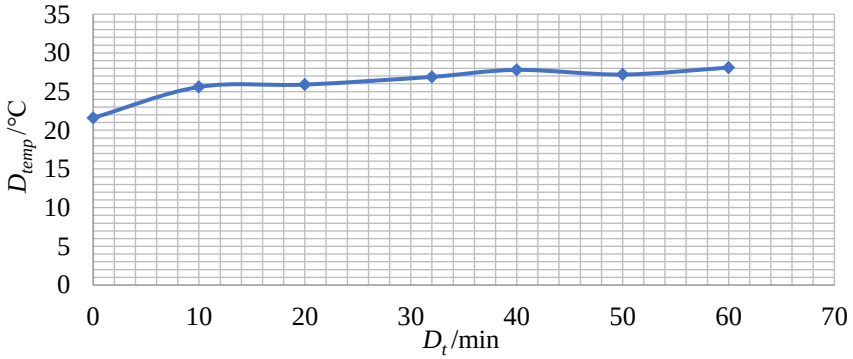



*Figure A.12 Temperature rise against time according to data in Table A.12.*

*Table A.13 Temperature measurements when Figure 5.3 switched at 35 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 43.8 | 21.1 | 22.7 |
| 2 | 11 | 51.3 | 23.1 | 28.2 |
| 3 | 20 | 53.5 | 24.2 | 29.3 |
| 4 | 30 | 54.1 | 23.7 | 30.4 |
| 5 | 40 | 54.7 | 24.1 | 30.6 |
| 6 | 50 | 55.4 | 24.6 | 30.8 |
| 7 | 60 | 55.9 | 24.9 | 31 |
| 8 | 70 | 56.3 | 24.8 | 31.5 |
| 9 | 80 | 57 | 25.2 | 31.8 |
| 10 | 95 | 56.3 | 25.3 | 31 |
| 11 | 100 | 57.6 | 26 | 31.6 |

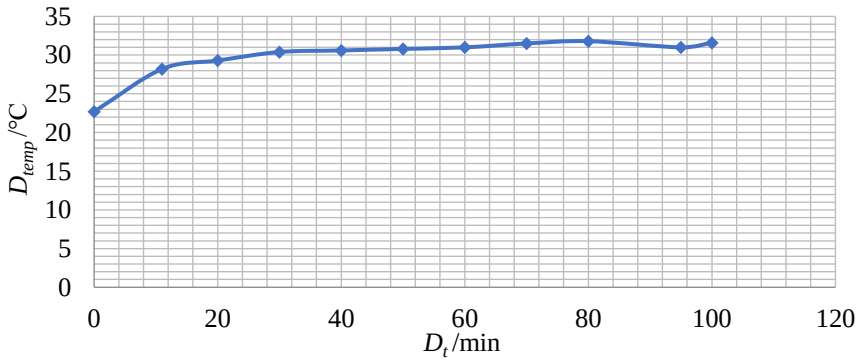



*Figure A.13 Temperature rise against time according to data in Table A.13.*

## A.2.2 Temperature measurements of using Module (b) in inverter-leg

Temperature measurements are recorded when using Module (b) in an inverter-leg, as in Figure 4.11, and running at different frequencies. Tables A.14, A.15, A.16, A.17, A.18 show the temperature measurements over time when the inverter-leg is operating under the frequency of 15 kHz, 20 kHz, 25 kHz, 30 kHz, 35 kHz, respectively. The corresponding $D_{temp}$ is drawn in Figures A.14, A.15, A.16, A.17, A.18.

*Table A.14 Temperature measurements when Figure 4.11 switched at 15 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 30.8 | 23.1 | 7.7 |
| 2 | 8 | 35.4 | 23.9 | 11.5 |
| 3 | 13 | 36.9 | 23.5 | 13.4 |
| 4 | 18 | 38.1 | 24 | 14.1 |
| 5 | 23 | 38.2 | 23.4 | 14.8 |
| 6 | 28 | 39.7 | 24.3 | 15.4 |
| 7 | 33 | 40.3 | 24 | 16.3 |
| 8 | 38 | 40.7 | 24 | 16.7 |
| 9 | 43 | 42.3 | 24.6 | 17.7 |
| 10 | 48 | 42.3 | 24.2 | 18.1 |
| 11 | 54 | 42.5 | 24.2 | 18.3 |
| 12 | 58 | 42.6 | 24.6 | 18 |

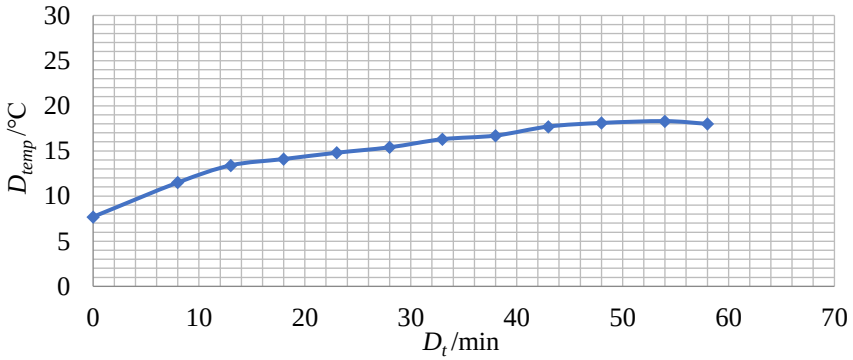



*Figure A.14 Temperature rise against time according to data in Table A.14.*

*Table A.15 Temperature measurements when Figure 4.11 switched at 20 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 32.1 | 22.2 | 9.9 |
| 2 | 10 | 36.6 | 22.7 | 13.9 |
| 3 | 20 | 40.1 | 23.2 | 16.9 |
| 4 | 30 | 42.1 | 23.3 | 18.8 |
| 5 | 43 | 42.1 | 22.9 | 19.2 |
| 6 | 50 | 43.8 | 24 | 19.8 |
| 7 | 62 | 44.4 | 23.8 | 20.6 |
| 8 | 70 | 44.6 | 24 | 20.6 |
| 9 | 80 | 44.9 | 24 | 20.9 |
| 10 | 95 | 45.7 | 24.9 | 20.8 |
| 11 | 100 | 45.8 | 25 | 20.83 |

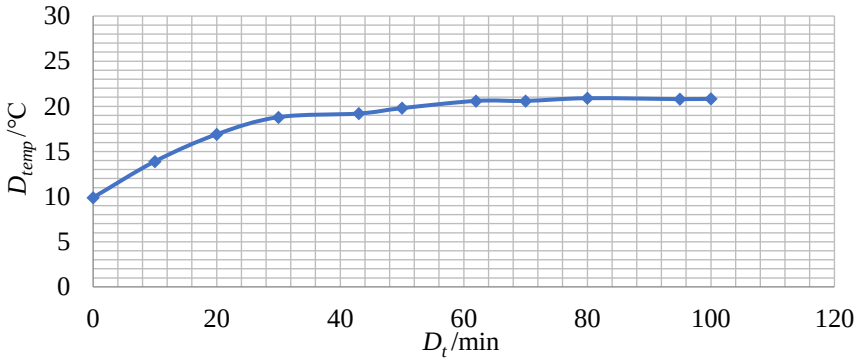



*Figure A.15 Temperature rise against time according to data in Table A.15.*

*Table A.16 Temperature measurements when Figure 4.11 switched at 25 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 33.7 | 24 | 9.7 |
| 2 | 10 | 38.4 | 23.9 | 14.5 |
| 3 | 20 | 42.3 | 24.5 | 17.8 |
| 4 | 30 | 45.1 | 24.9 | 20.2 |
| 5 | 43 | 46.3 | 25.1 | 21.2 |
| 6 | 50 | 46.3 | 25 | 21.3 |
| 7 | 60 | 46.9 | 25.6 | 21.3 |
| 8 | 70 | 47.4 | 25.7 | 21.7 |
| 9 | 80 | 47.4 | 25.5 | 21.9 |
| 10 | 90 | 47.7 | 25.6 | 22.1 |
| 11 | 101 | 48.2 | 26 | 22.2 |
| 12 | 110 | 47.7 | 25.5 | 22.2 |
| 13 | 120 | 47.9 | 25.6 | 22.3 |

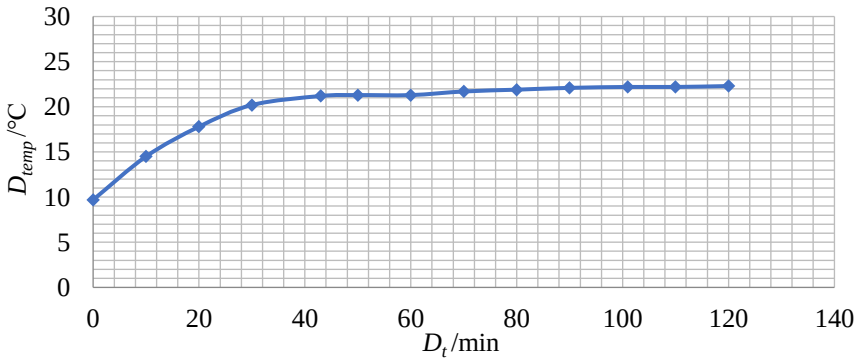



*Figure A.16 Temperature rise against time according to data in Table A.16.*

*Table A.17 Temperature measurements when Figure 4.11 switched at 30 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 43.2 | 26.3 | 16.9 |
| 2 | 10 | 46.2 | 25.7 | 20.5 |
| 3 | 20 | 48.9 | 26.4 | 22.5 |
| 4 | 30 | 49.7 | 26.3 | 23.4 |
| 5 | 40 | 49.8 | 26.3 | 23.5 |
| 6 | 50 | 50.4 | 26.4 | 24 |
| 7 | 60 | 51 | 26.7 | 24.3 |
| 8 | 70 | 50.9 | 26.4 | 24.5 |
| 9 | 80 | 50.2 | 25.9 | 24.3 |
| 10 | 90 | 50.9 | 26.8 | 24.1 |
| 11 | 100 | 50.9 | 26.1 | 24.8 |

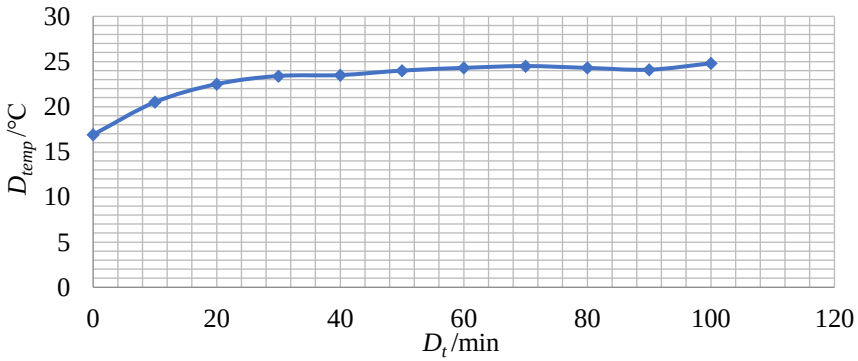



*Figure A.17 Temperature rise against time according to data in Table A.17.*

*Table A.18 Temperature measurements when Figure 4.1 switched at 35 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 46.7 | 26.6 | 20.1 |
| 2 | 10 | 50.2 | 26.3 | 23.9 |
| 3 | 22 | 51.7 | 26.3 | 25.4 |
| 4 | 30 | 53.2 | 26.3 | 26.9 |
| 5 | 40 | 53.3 | 26.6 | 26.7 |
| 6 | 50 | 53.5 | 26.7 | 26.8 |
| 7 | 60 | 53.7 | 26.6 | 27.1 |
| 8 | 70 | 53.4 | 26.6 | 26.8 |

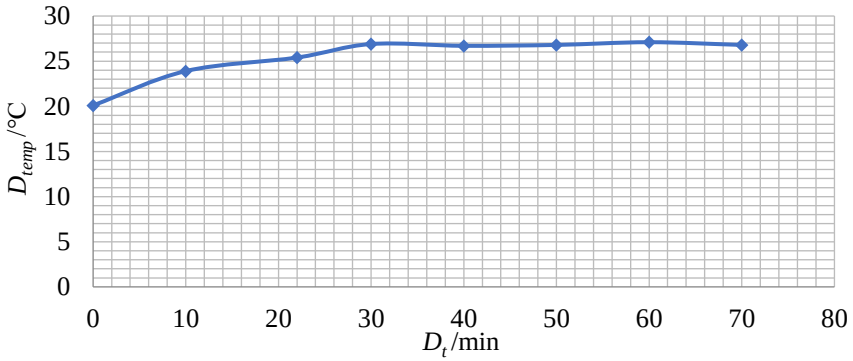



*Figure A.18 Temperature rise against time according to data in Table A.18.*

## A.2.4 Temperature measurements of using Module (c) in inverter-leg

Temperature measurements are recorded when using Module (c) in an inverter-leg, as in Figure 5.4, and running at different frequencies. Tables A.19, A.20, A.21, A.22, A.23 shows the temperature measurements over time when the circuit is operating under the frequency of 15 kHz, 20 kHz, 25 kHz, 30 kHz, 35 kHz, respectively. The corresponding $D_{temp}$ is drawn in Figures A.19, A.20, A.21, A.22, A.23.

*Table A.19 Temperature measurements when Figure 5.4 switched at 15 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 39.2 | 23.9 | 15.3 |
| 2 | 10 | 39.8 | 23.8 | 16 |
| 3 | 20 | 40.4 | 23.9 | 16.5 |
| 4 | 30 | 40.5 | 23.9 | 16.6 |
| 5 | 35 | 40.6 | 24 | 16.6 |

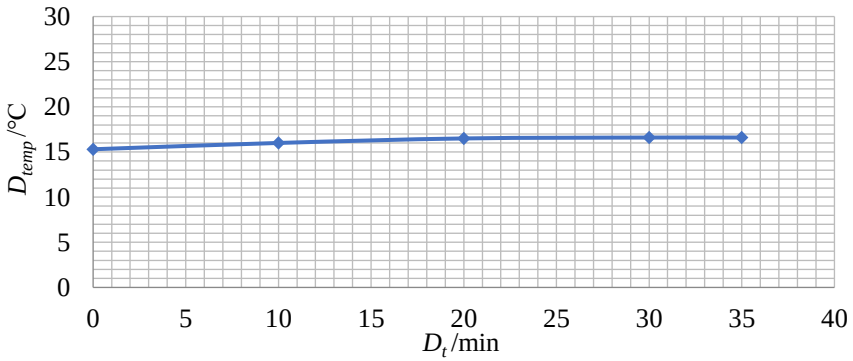



*Figure A.19 Temperature rise against time according to data in Table A.24.*

*Table A.20 Temperature measurements when Figure 5.4 switched at 20 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 42 | 23.2 | 18.8 |
| 2 | 11 | 42.9 | 23.8 | 19.1 |
| 3 | 20 | 43 | 23.6 | 19.4 |
| 4 | 30 | 43.4 | 24.2 | 19.2 |

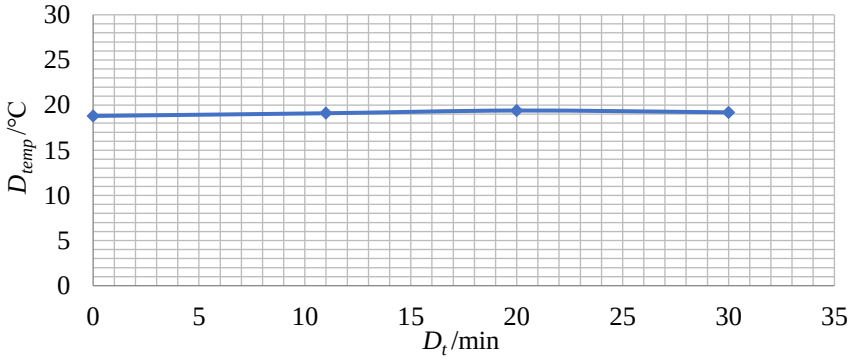



*Figure A.20 Temperature rise against time according to data in Table A.25.*

*Table A.21 Temperature measurements when Figure 5.4 switched at 25 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 30.1 | 21.3 | 8.8 |
| 2 | 10 | 37.6 | 21.7 | 15.9 |
| 3 | 23 | 41.7 | 22.5 | 19.2 |
| 4 | 34 | 43.5 | 23.9 | 19.6 |
| 5 | 40 | 44.3 | 22.9 | 21.4 |
| 6 | 60 | 45.7 | 22.9 | 22.8 |
| 7 | 74 | 46.4 | 23.4 | 23 |
| 8 | 80 | 46 | 23.4 | 22.6 |

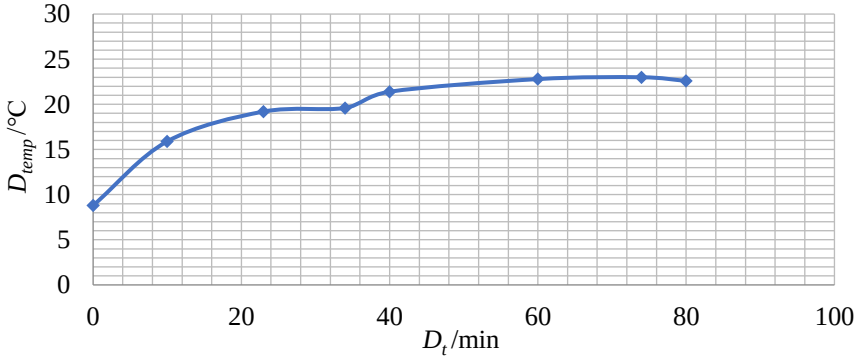



*Figure A.21 Temperature rise against time according to data in Table A.26.*

*Table A.22 Temperature measurements when Figure 5.4 switched at 30 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 47.3 | 24.8 | 22.5 |
| 2 | 10 | 49.8 | 25.3 | 24.5 |
| 3 | 20 | 50.3 | 25.2 | 25.1 |
| 4 | 30 | 50.3 | 25.1 | 25.2 |
| 5 | 40 | 51.1 | 25.6 | 25.5 |
| 6 | 50 | 51 | 25.2 | 25.8 |
| 7 | 55 | 51.1 | 25.4 | 25.7 |
| 8 | 60 | 51.4 | 25.8 | 25.6 |

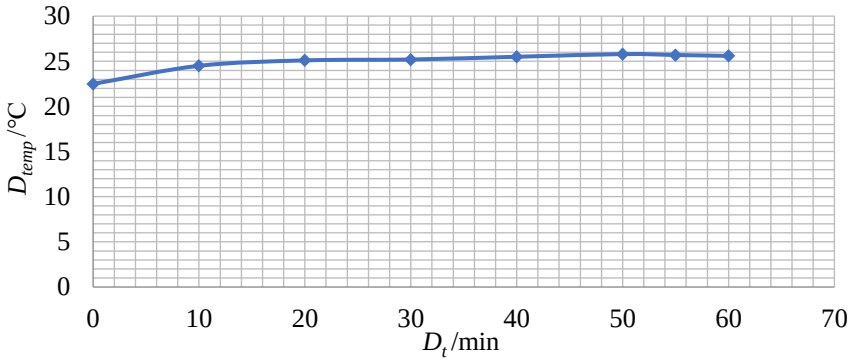



*Figure A.22 Temperature rise against time according to data in Table A.27.*

*Table A.23 Temperature measurements when Figure 5.4 switched at 35 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 36.2 | 22.7 | 13.5 |
| 2 | 10 | 43.3 | 22.7 | 20.6 |
| 3 | 20 | 47.8 | 23 | 24.8 |
| 4 | 33 | 51 | 24 | 27 |
| 5 | 40 | 51.4 | 24 | 27.4 |
| 6 | 55 | 52.9 | 24.5 | 28.4 |
| 7 | 60 | 53.2 | 24.6 | 28.6 |
| 8 | 65 | 53.5 | 25 | 28.5 |

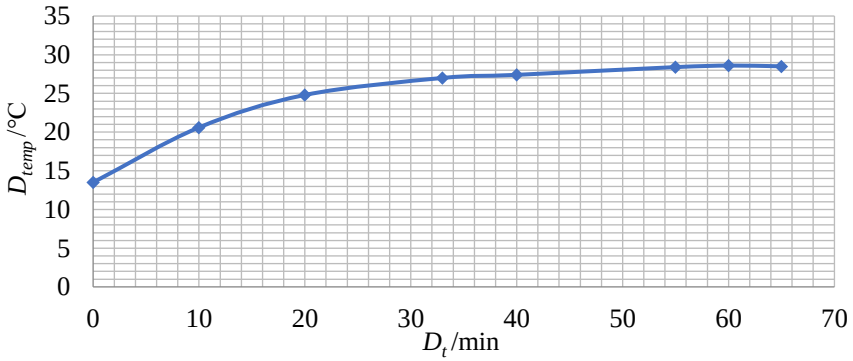



*Figure A.23 Temperature rise against time according to data in Table A.28.*

## A.2.6 Temperature measurements of using Module (d) in inverter-leg

Temperature measurements are recorded when using Module (d) in an inverter-leg, as in Figure 5.5, and running at different frequencies. Tables A.24, A.25, A.26, A.27, A.28 show the temperature measurements over time when the circuit is operating under the frequency of 15 kHz, 20 kHz, 25 kHz, 30 kHz, 35 kHz, respectively. The corresponding $D_{temp}$ is drawn in Figures A.24, A.25, A.26, A.27, A.28.

*Table A.24 Temperature measurements when Figure 5.5 switched at 15 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 24.8 | 21.4 | 3.4 |
| 2 | 12 | 30.9 | 22.5 | 8.4 |
| 3 | 27 | 34 | 22.5 | 11.5 |
| 4 | 36 | 35.5 | 22.7 | 12.8 |
| 5 | 42 | 36.4 | 22.8 | 13.6 |
| 6 | 57 | 36.8 | 22.7 | 14.1 |
| 7 | 62 | 37.4 | 23.2 | 14.2 |
| 8 | 67 | 37.7 | 23.2 | 14.5 |
| 9 | 80 | 38.2 | 24 | 14.2 |

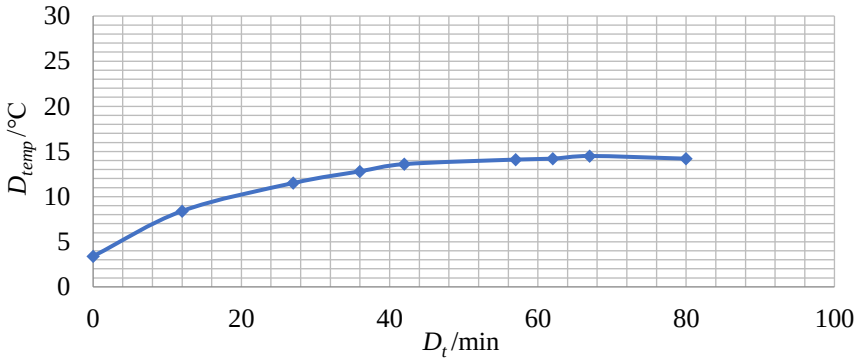



*Figure A.24 Temperature rise against time according to data in Table A.34*

*Table A.25 Temperature measurements when Figure 5.5 switched at 20 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 34.6 | 23.3 | 11.3 |
| 2 | 10 | 37.6 | 23.4 | 14.2 |
| 3 | 22 | 38.6 | 23.5 | 15.1 |
| 4 | 30 | 39 | 23.7 | 15.3 |
| 5 | 47 | 39.9 | 23.7 | 16.2 |
| 6 | 52 | 40.2 | 24.3 | 15.9 |
| 7 | 57 | 40.6 | 24.5 | 16.1 |

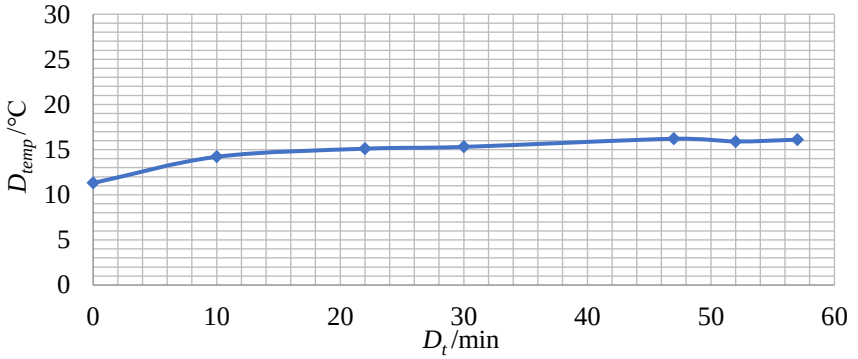



*Figure A.25 Temperature rise against time according to data in Table A.35.*

*Table A.26 Temperature measurements when Figure 5.5 switched at 25 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 39.7 | 25.4 | 14.3 |
| 2 | 10 | 40.1 | 24.7 | 15.4 |
| 3 | 20 | 41.5 | 25.3 | 16.2 |
| 4 | 30 | 42.3 | 24.7 | 17.6 |
| 5 | 40 | 43.2 | 25.3 | 17.9 |
| 6 | 50 | 43 | 24.8 | 18.2 |
| 7 | 60 | 42.7 | 24.7 | 18 |

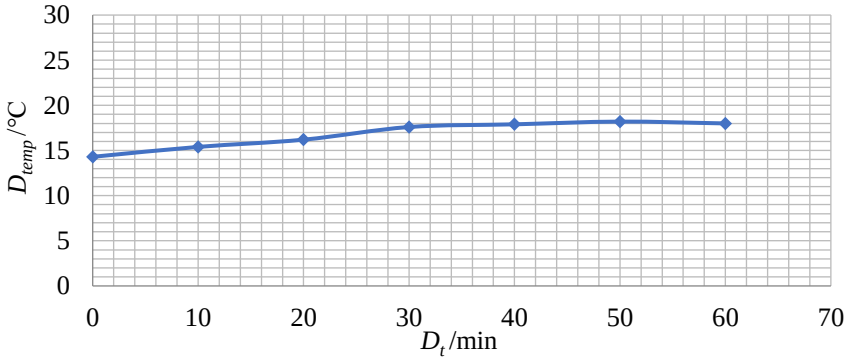



*Figure A.26 Temperature rise against time according to data in Table A.36.*

*Table A.27 Temperature measurements when Figure 5.5 switched at 30 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/℃ |
|---|---|---|---|---|
| | | Heatsink/℃ | Ambient/℃ | |
| 1 | 0 | 41.7 | 23.7 | 18 |
| 2 | 22 | 43.6 | 23.3 | 20.3 |
| 3 | 32 | 44.2 | 23.7 | 20.5 |
| 4 | 42 | 44.4 | 23.3 | 21.1 |
| 5 | 52 | 44.6 | 23.8 | 20.8 |
| 6 | 57 | 44.6 | 23.7 | 20.9 |

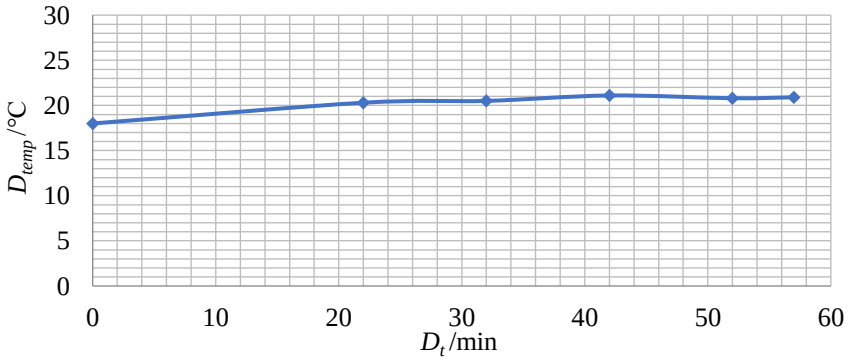



*Figure A.27 Temperature rise against time according to data in Table A.37.*

*Table A.28 Temperature measurements when Figure 5.5 switched at 35 kHz.*

| NO | $D_t$/min | Temperature | | $D_{temp}$/°C |
|---|---|---|---|---|
| | | Heatsink/°C | Ambient/°C | |
| 1 | 0 | 24 | 20.9 | 3.1 |
| 2 | 10 | 33 | 21.5 | 11.5 |
| 3 | 25 | 40.2 | 21.8 | 18.4 |
| 4 | 35 | 42.8 | 21.9 | 20.9 |
| 5 | 45 | 44.9 | 22.6 | 22.3 |
| 6 | 55 | 45.3 | 22.5 | 22.8 |
| 7 | 65 | 46.4 | 23.3 | 23.1 |
| 8 | 75 | 46.3 | 23.1 | 23.2 |
| 9 | 80 | 46.5 | 23.4 | 23.1 |

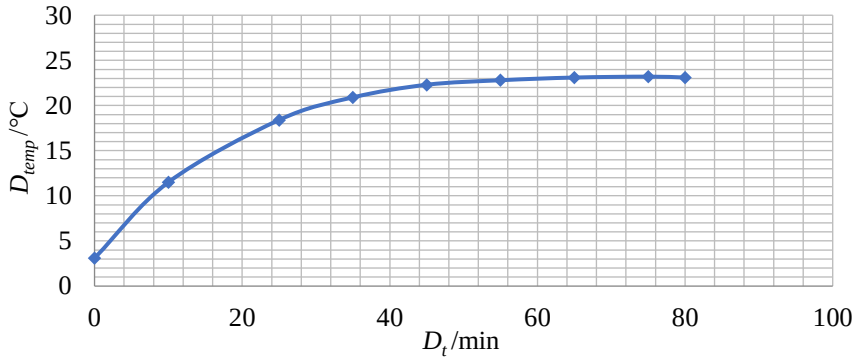



*Figure A.28 Temperature rise against time according to data in Table A.38.*

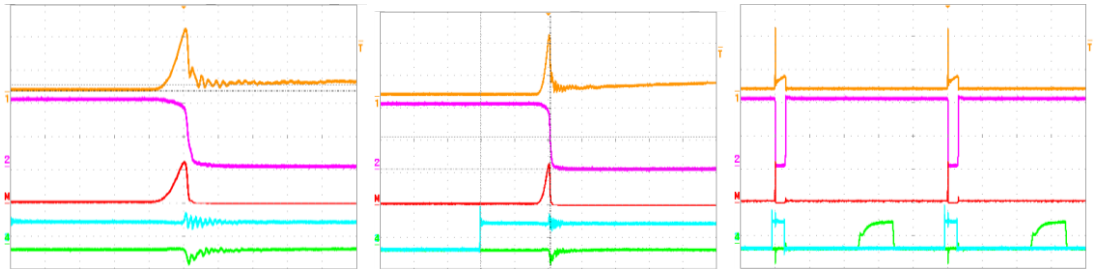
# A.3 Scope waveforms of DC tests in Chapter 6

## A.3.1 DC tests with simple resistor in series with MOSFET's gate terminal

Scope waveforms were taken when testing the circuit in Figure 6.9 (a). $R_g$ of the circuit in Figure 6.9 (a) was set at 160 Ω, 220 Ω, 300 Ω, and 330 Ω. $I_{LOAD}$ varies from 1 A, 2 A, 3 A, 4 A for a fixed $R_g$. The scope waveforms are, *TR*2 drain current $i_{D2}$ (yellow), *TR*2 drain-source voltage $v_{DS2}$ (pink), instantaneous power dissipation in *TR*2 $w_{inst}$ (red, multiplying $i_{D2}$ and $v_{DS2}$ using the oscilloscope "MATH" function), Drive IC signal $v_{DRI}$ of *TR*2 (blue) and *TR*1 (green) from top to bottom. Scales are $i_{D2}$ = 5 A/div., $v_{DS2}$ = 200 V/div., $w_{inst}$ = 2.5 kW/div., $v_{DRI}$ = 20 V/div. Time scales are indicated under figure names.

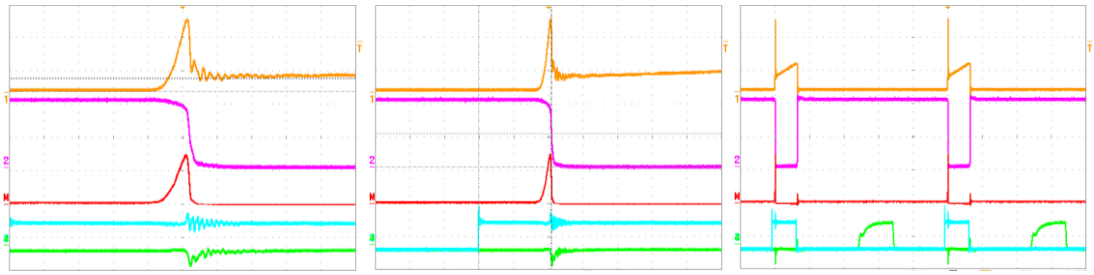
### A.3.2.1 *Rg* = 160 Ω

Figure A.29, A.30, A.31, A.32 shows the scope waveforms of the circuit in Figure 6.9 (a) when $R_g$ = 160 Ω and $I_{LOAD}$ = 1 A, 2 A, 3 A, 4 A, respectively.



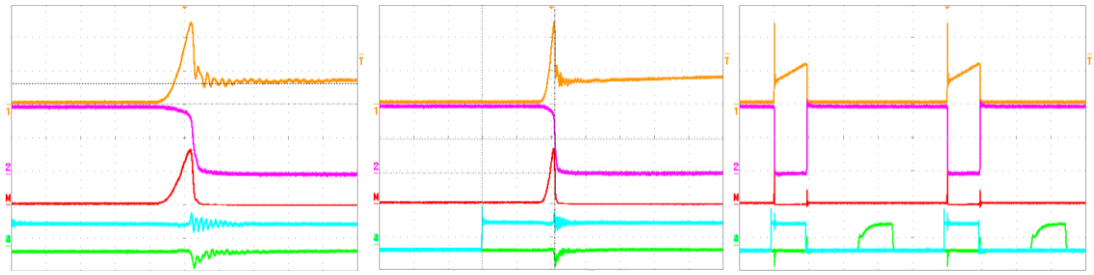
*(a)* *(b)* *(c)*

*Figure A.29 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 160 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



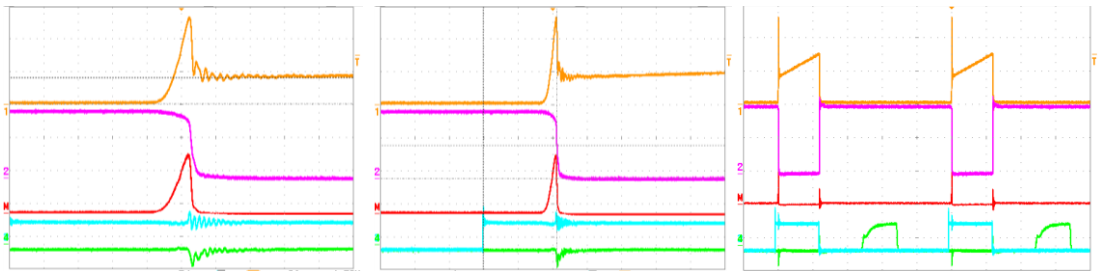
*(a)* *(b)* *(c)*

*Figure A.30 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 160 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



*(a)* *(b)* *(c)*

*Figure A.31 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 160 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

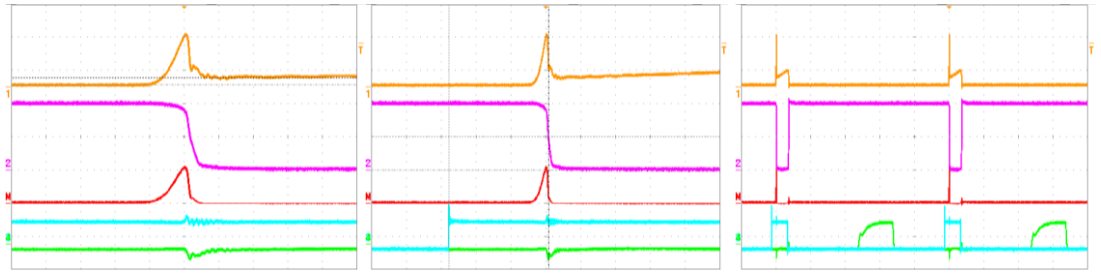


(a) (b) (c)

*Figure A.32 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 160 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

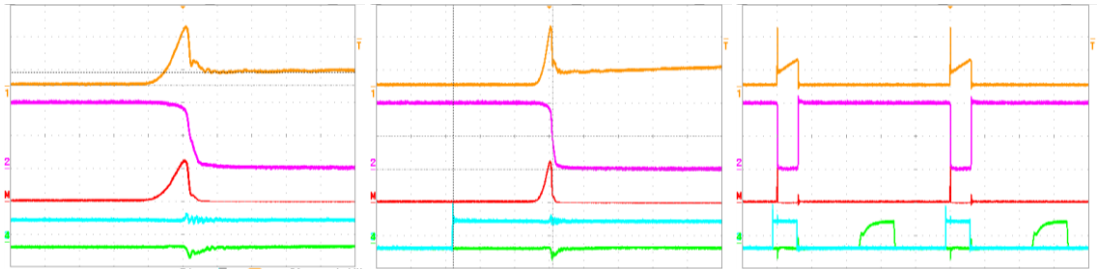
### A.3.2.2 *Rg* = 220 Ω

Figures A.33, A.34, A.35, A.36 show the scope waveforms of the circuit in Figure 6.9 (a) when $R_g$ = 220 Ω and $I_{LOAD}$ = 1 A, 2 A, 3 A, 4 A, respectively.



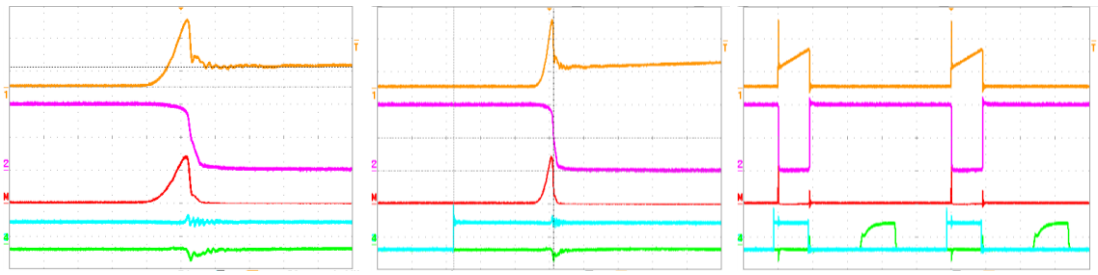
(a) (b) (c)

*Figure A.33 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 220 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



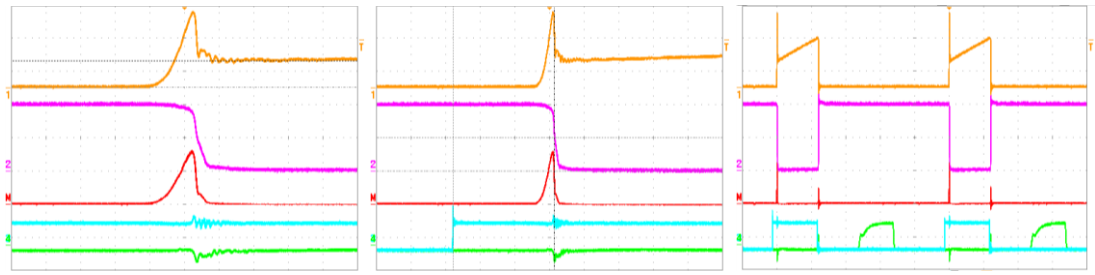
(a) (b) (c)

*Figure A.34 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 220 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

*Figure A.35 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 220 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

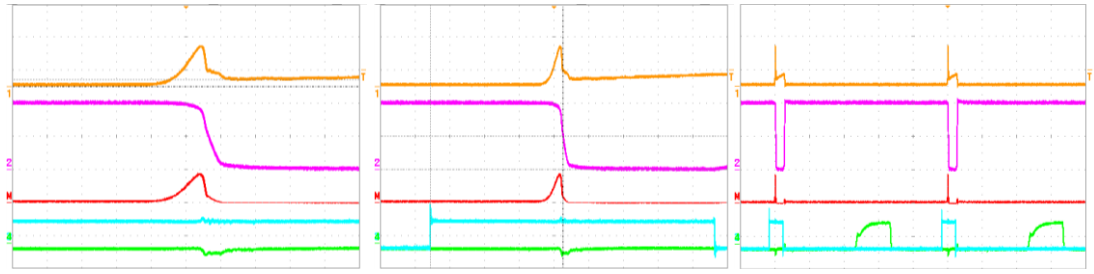


(a) (b) (c)

*Figure A.36 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 220 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

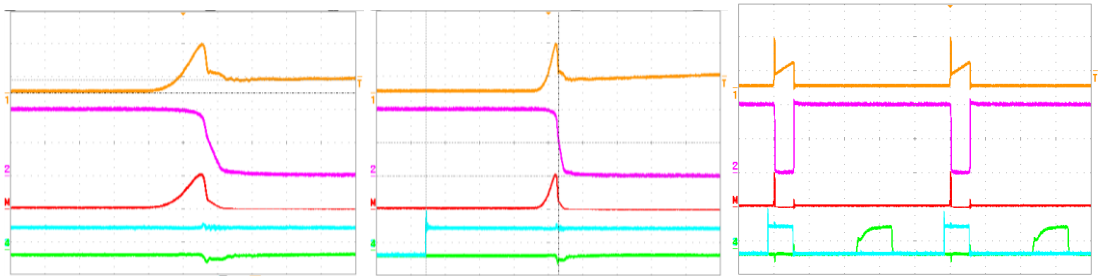
### A.3.2.3 *Rg* = 300 Ω

Figures A.37, A.38, A.39, A.40 show the scope waveforms of the circuit in Figure 6.9 (a) when $R_g$ = 300 Ω and $I_{LOAD}$ = 1 A, 2 A, 3 A, 4 A, respectively.



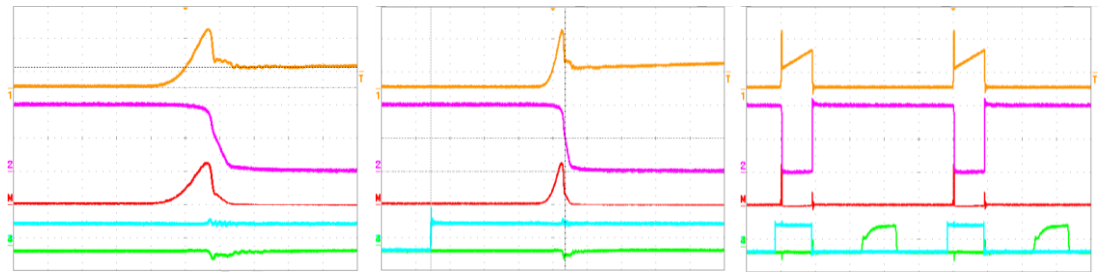
(a) (b) (c)

*Figure A.37 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 300 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



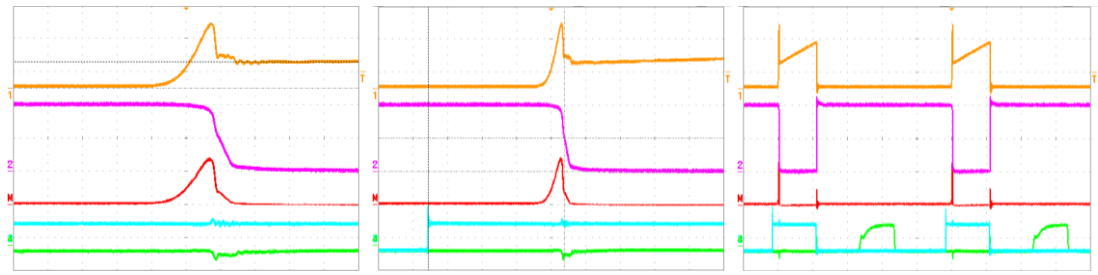
(a) (b) (c)

*Figure A.38 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 300 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

*Figure A.39 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 300 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

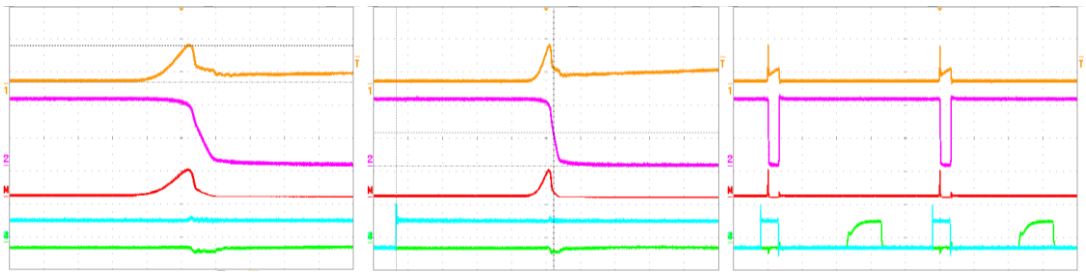


(a) (b) (c)

*Figure A.40 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 300 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

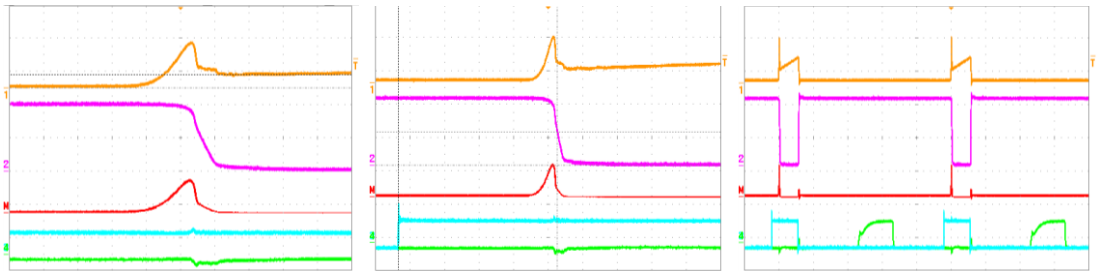
### A.3.2.4 *Rg* = 360 Ω

Figures A.41, A.42, A.43, A.44 show the scope waveforms of the circuit in Figure 6.9 (a) when $R_g$ = 360 Ω and $I_{LOAD}$ = 1 A, 2 A, 3 A, 4 A, respectively.



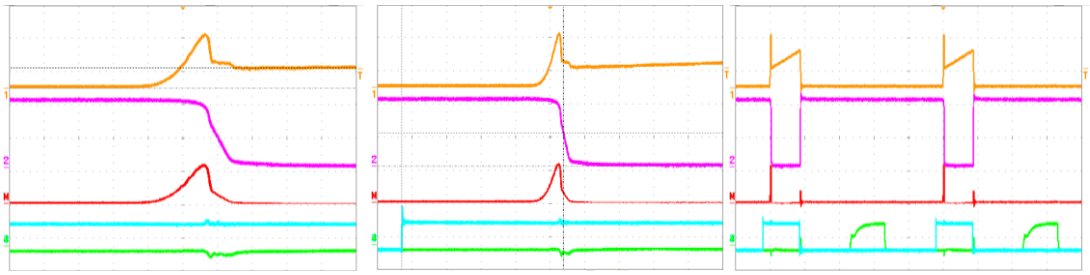
(a) (b) (c)

*Figure A.41 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 360 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



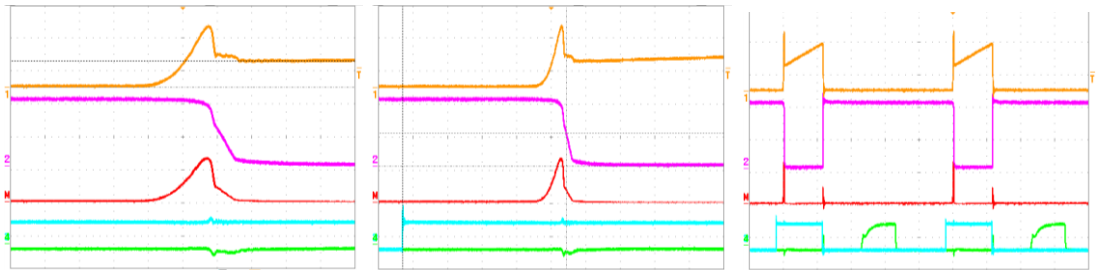
(a) (b) (c)

*Figure A.42 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 360 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

*Figure A.43 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 360 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

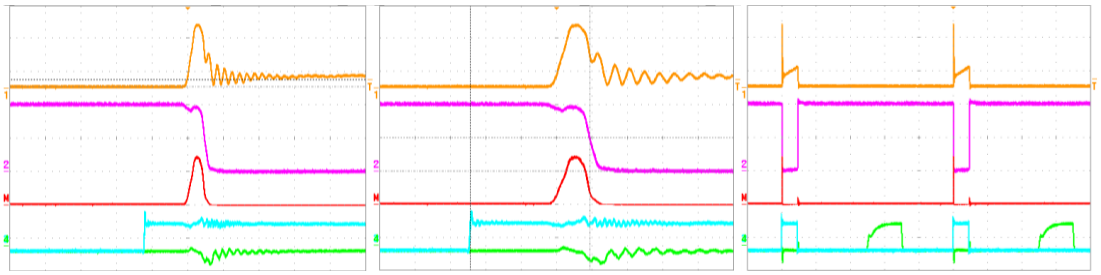
*Figure A.44 Exemplifying waveforms of circuit in Figure 6.9 (a) when $R_g$ = 360 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 500 ns/div., (c) = 10 µs/div.*

## A.3.1 DC tests with CT scheme

Scope waveforms were taken when testing the CT scheme in Figure 6.9 (b). $R_g$ of the circuit in Figure 6.9 (b) was set at 39 Ω, 47 Ω, 56 Ω, and 68 Ω. $I_{LOAD}$ varies from 1 A, 2 A, 3 A, 4 A for a fixed $R_g$. The scope waveforms are, *TR*2 drain current $i_{D2}$ (yellow), *TR*2 drain-source voltage $v_{DS2}$ (pink), instantaneous power dissipation in *TR*2 $w_{inst}$ (red, multiplying $i_{D2}$ and $v_{DS2}$ using the oscilloscope "MATH" function), Drive IC signal $v_{DRI}$ of *TR*2 (blue) and *TR*1 (green) from top to bottom. Scales are $i_{D2}$ = 5 A/div., $v_{DS2}$ = 200 V/div., $w_{inst}$ = 2.5 kW/div., $v_{DRI}$ = 20 V/div. Time scales are indicated under figure names.

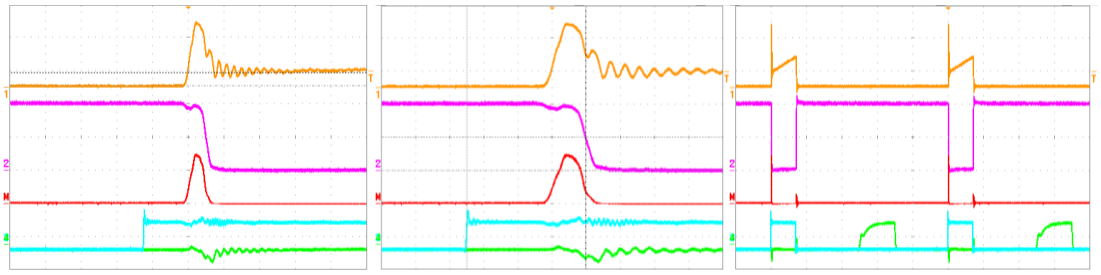
### A.3.1.1 *Rg* = 39 Ω

Figures A.45, A.46, A.47, A.48 show the scope waveforms of the scheme in Figure 6.9 (b) when $R_g$ = 39 Ω and $I_{LOAD}$ = 1 A, 2 A, 3 A, 4 A, respectively.



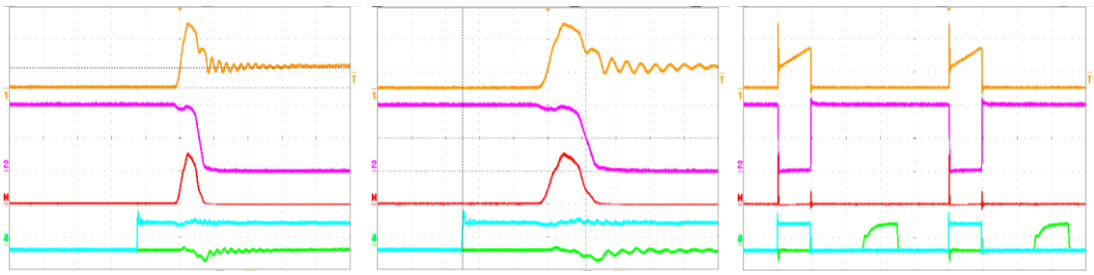
(a) (b) (c)

*Figure A.45 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 39 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



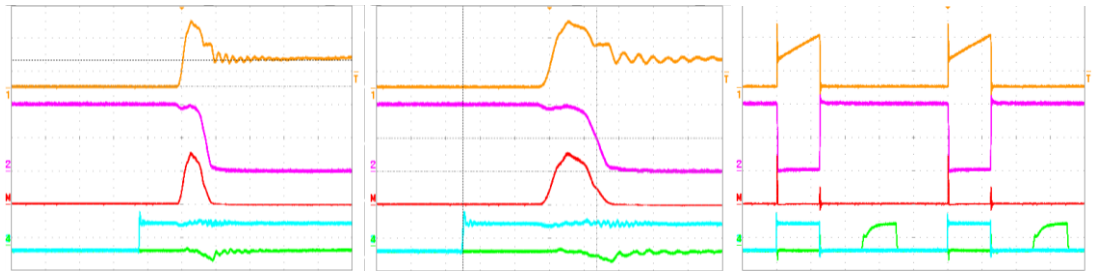
(a) (b) (c)

*Figure A.46 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 39 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

*Figure A.47 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 39 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

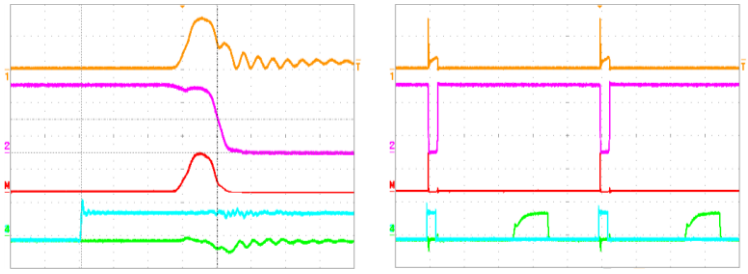


(a) (b) (c)

*Figure A.48 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 39 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

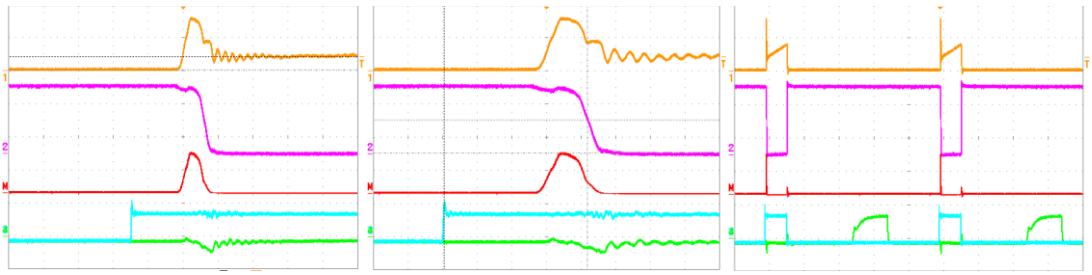
### A.3.1.2 *Rg* = 47 Ω

Figures A.49, A.50, A.51, A.52 show the scope waveforms of the scheme in Figure 6.9 (b) when $R_g$ = 47 Ω and $I_{LOAD}$ = 1 A, 2 A, 3 A, 4 A, respectively.



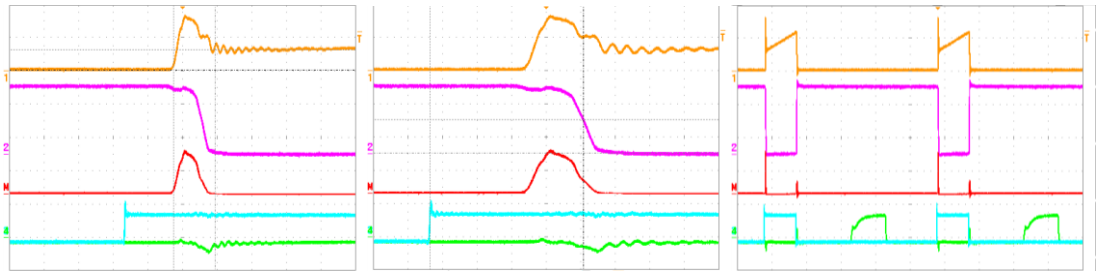
(a) (b)

*Figure A.49 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 47 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 100 ns/div., (b) = 10 µs/div.*



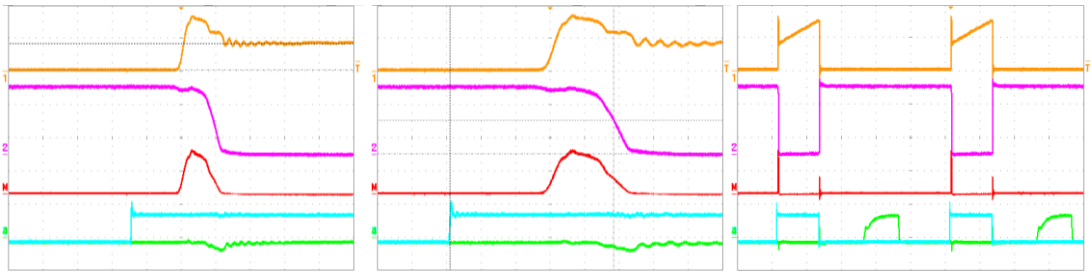
(a) (b) (c)

*Figure A.50 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 47 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

*Figure A.51 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 47 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

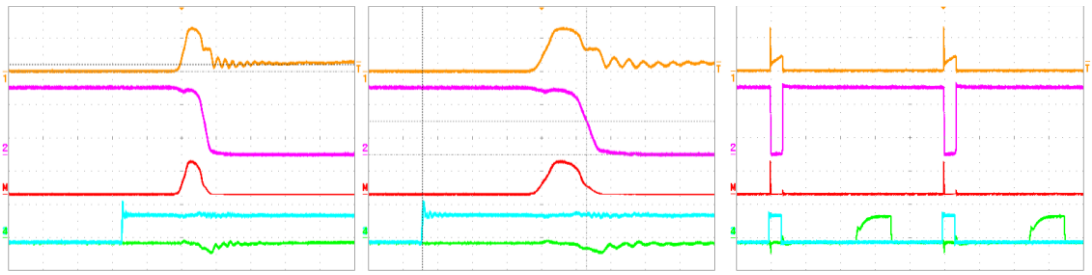


(a) (b) (c)

*Figure A.52 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 47 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

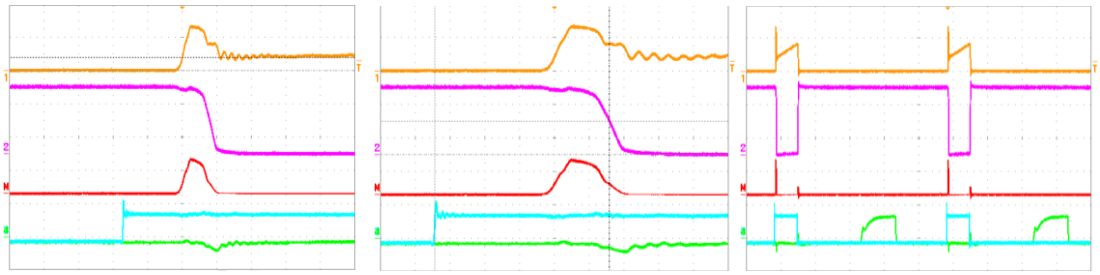
### A.3.1.3 *Rg* = 56 Ω

Figures A.53, A.54, A.55, A.56 show the scope waveforms results of scheme in Figure 6.9 (b) when $R_g$ = 56 Ω and $I_{LOAD}$ of 1 A, 2 A, 3 A, 4 A, respectively.



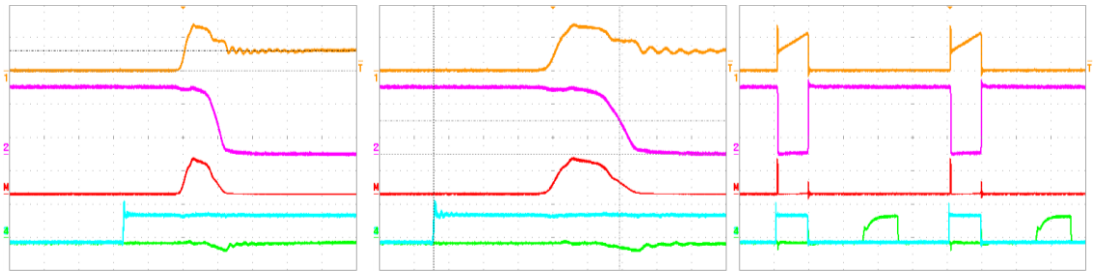
(a) (b) (c)

*Figure A.53 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 56 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



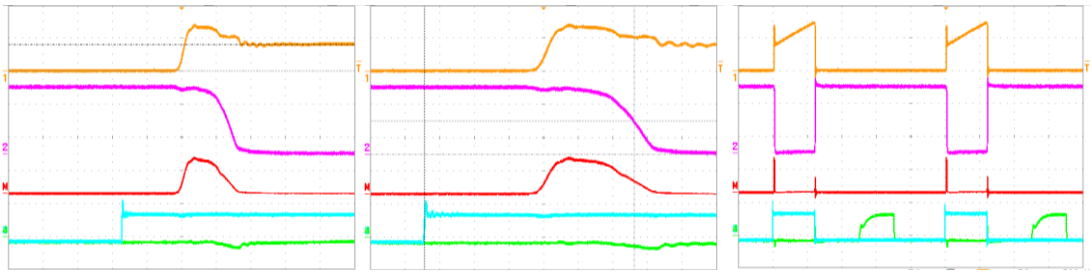
(a) (b) (c)

*Figure A.54 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 56 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



(a) (b) (c)

*Figure A.55 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 56 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

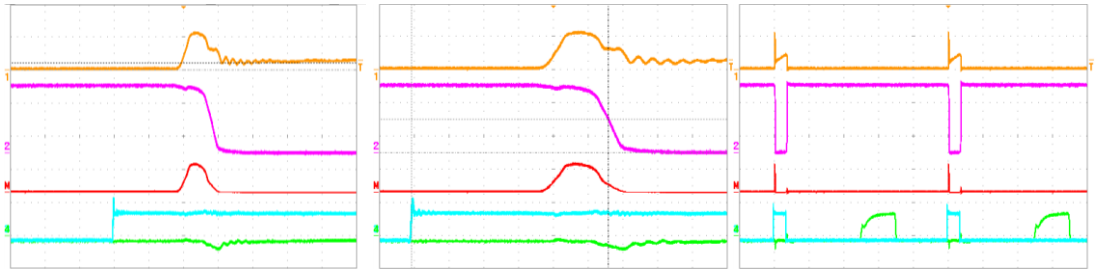


(a) (b) (c)

*Figure A.56 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 56 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

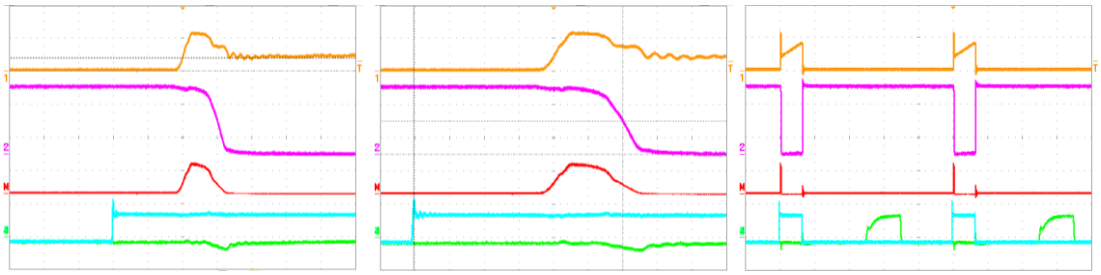
### A.3.1.4 *Rg* = 68 Ω

Figures A.57, A.58, A.59, A.60 show the scope waveforms of the scheme in Figure 6.9 (b) when $R_g$ = 68 Ω and $I_{LOAD}$ of 1 A, 2 A, 3 A, 4 A, respectively.



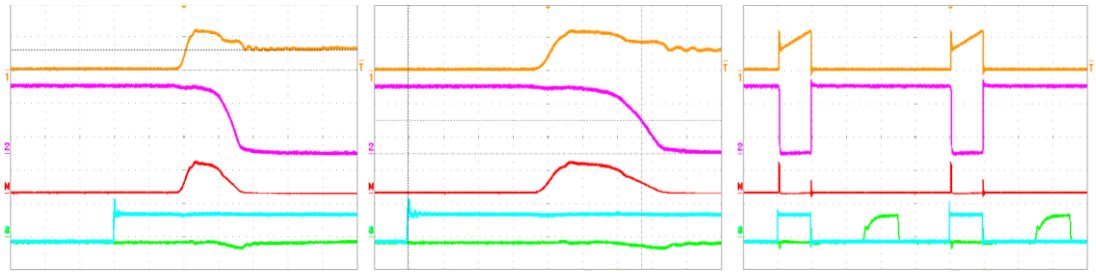
*(a)* *(b)* *(c)*

*Figure A.57 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 68 Ω and $I_{LOAD}$ = 1 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



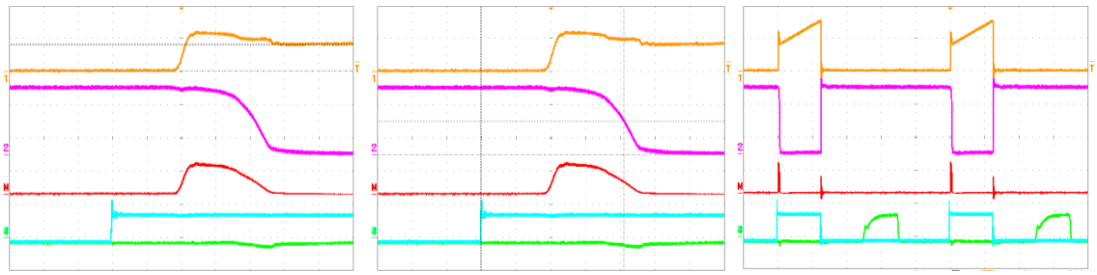
*(a)* *(b)* *(c)*

*Figure A.58 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 68 Ω and $I_{LOAD}$ = 2 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



*(a)* *(b)* *(c)*

*Figure A.59 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 68 Ω and $I_{LOAD}$ = 3 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*



*(a)* *(b)* *(c)*

*Figure A.60 Exemplifying waveforms of scheme in Figure 6.9 (b) when $R_g$ = 68 Ω and $I_{LOAD}$ = 4 A. Time scales are (a) = 200 ns/div., (b) = 100 ns/div., (c) = 10 µs/div.*

# Appendix B

# Gate driver design

## B.1 Optical gate driver

Optical gate driver provides optical isolation between the control signal source and the IGBT or MOSFET gate by means of two opto-couplers. One driver contains two channels on board, which is convenient for using in a bridge-leg to provide complementary signals. Two channels share the same power supply. Driver IC IXDN614SI is used in each channel to enhance the output current ability.

The Table B.1 shows the components lists of the optical gate driver. Figure B.1 shows its schematic drawn in Altium Designer. Figure B.2 is the practical photo with labelled measurements.

*Table B.1 BOM of the optical gate driver.*

| Identifier | Description | Manufacturer | Mfrs. Part no. | Supplier | Order code | Qty. | Unit cost | Sub-total |
|---|---|---|---|---|---|---|---|---|
| R1, 2 | Resistor 1k Ω | TT Electronics/Welwyn | WCR0805-1K0FI | Farnell | 1099800 | 2 | 0.0168 | 0.0336 |
| R3 | Resistor 22 Ω | TT Electronics/Welwyn | WCR0805-22RFI | Farnell | 1099789 | 1 | 0.0196 | 0.0196 |
| R4, 5, 9, 10 | Resistor 10k Ω | TT Electronics/Welwyn | WCR0805-10KFI | Farnell | 1099807 | 4 | 0.0196 | 0.0784 |
| R6, 11 | Resistor 470 Ω | TT Electronics/Welwyn | WCR0805-470RFI | Farnell | 1099798 | 2 | 0.0168 | 0.0336 |
| R7, 12 | Resistor 10 Ω | TT Electronics/Welwyn | WCR0805-10RFI | Farnell | 1099787 | 2 | 0.0196 | 0.0392 |
| R8, 13 | Resistor 100 Ω | TT Electronics/Welwyn | WCR0805-100RFI | Farnell | 1099793 | 2 | 0.0196 | 0.0392 |
| C1 | Capacitor 1 µF | Multicomp | MC0805B105K100CT | Farnell | 2320857 | 1 | 0.253 | 0.253 |
| C2 | Capacitor 220 pF | Multicomp | MCSH21B221K250CT | Farnell | 1856450 | 1 | 0.0988 | 0.0988 |
| C3, 4, 5, 7 | Capacitor 10 µF | Samsung Electro-Mechanics | CL32B106KLULNNF | RS | 766-1194 | 4 | 0.334 | 1.336 |
| C6, 8 | Capacitor 47 µF | Murata | GRM32ER71A476ME15L | RS | 820-2908 | 2 | 1.624 | 3.248 |
| D1 | Red LED 1.8 V | ROHM | SML-211UTT86 | RS | 700-7907 | 1 | 0.4 | 0.4 |
| D2, 3, 6, 9 | Signal diode | On Semiconductor | 1N4148TR | Farnell | 9843680 | 4 | 0.0527 | 0.2108 |
| D4, 7 | Zener diode 18 V | Diodes Inc. | BZX84C18 | Farnell | 1902449 | 2 | 0.0981 | 0.1962 |
| D5, 8 | Zener diode 3.9 V | Diodes Inc. | BZX84C3V9 | Farnell | 1902458 | 2 | 0.0981 | 0.1962 |
| Q1, 2, 3 | MOSFET, N-Channel, 5.1 A, 55 V, 0.0462 ohm | Infineon | IRFL024ZPBF | RS | 650-4463 | 3 | 0.934 | 2.802 |
| U1 | Quad 2-input NAND gate | Fairchild Semiconductor | 74AC00SC | Farnell | 1014139 | 1 | 0.449 | 0.449 |
| U2, 4 | Opto-coupler | Broadcom Inc. | HCPL-0302-000E | Farnell | 9130160 | 2 | 1.11 | 2.22 |
| U3, 5 | Driver IC | IXYS | IXDN614SI | Mouser | 849-IXDN614SI | 2 | 3.23 | 6.46 |
| T1 | Transformer Core, Toroid, 3C90, 30.1 mm, 12.2 mm² | Ferroxcube | TN13/7.5/5-3C90 | Farnell | 178504 | 1 | 0.294 | 0.294 |
| | | | | | **Sum** | **£18.4076** | | |

*All costs are based on the prices on Farnell or Mouser in 2019.

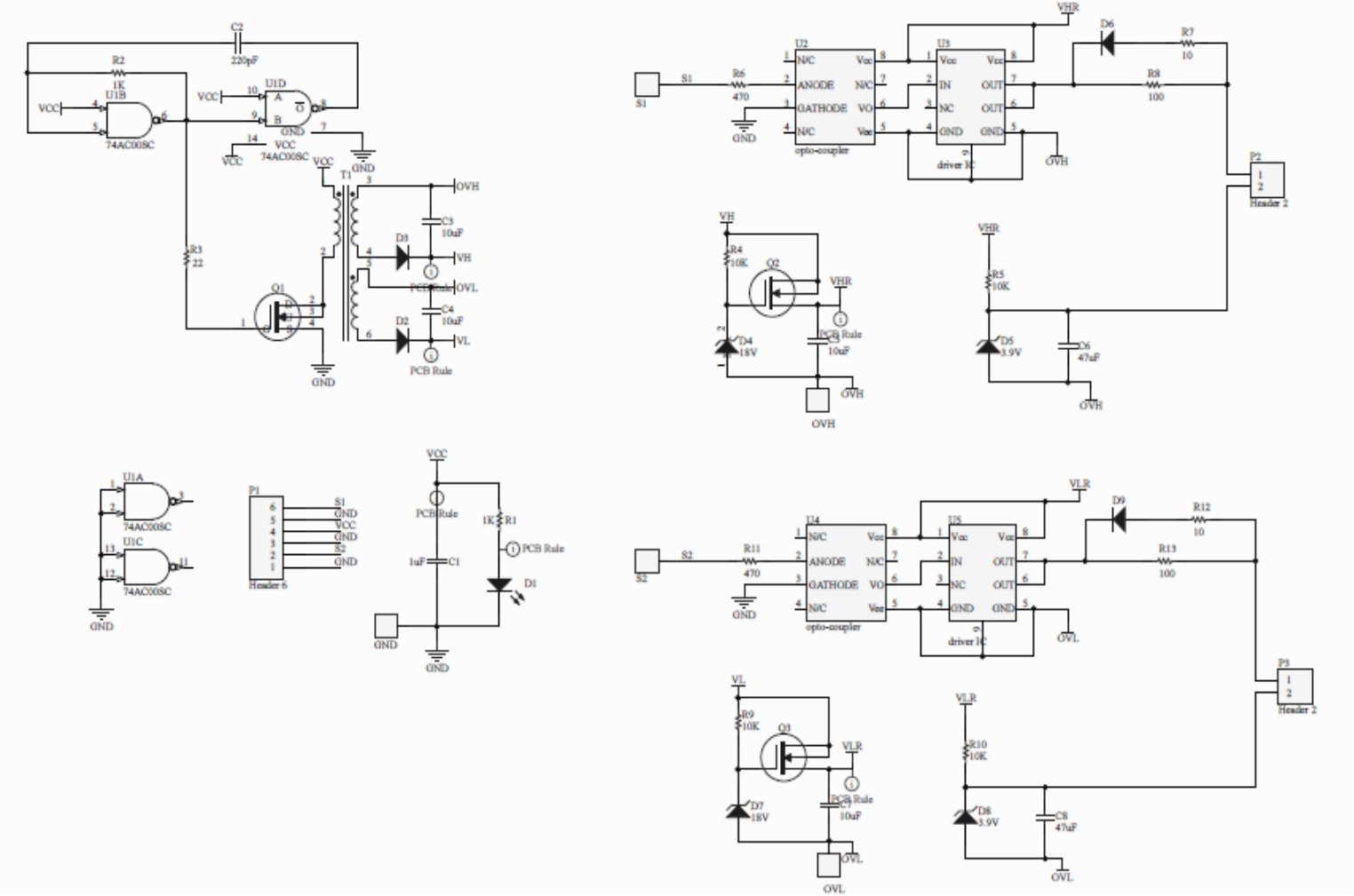



*Figure B.1 Schematic of optical gate driver board.*

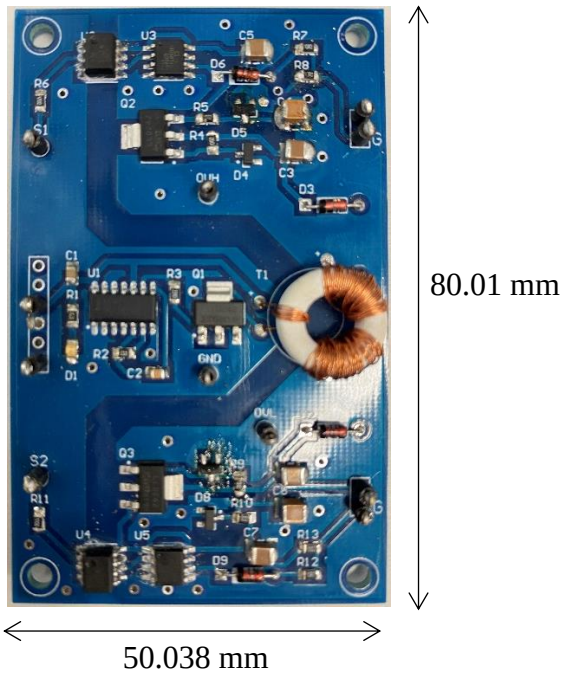
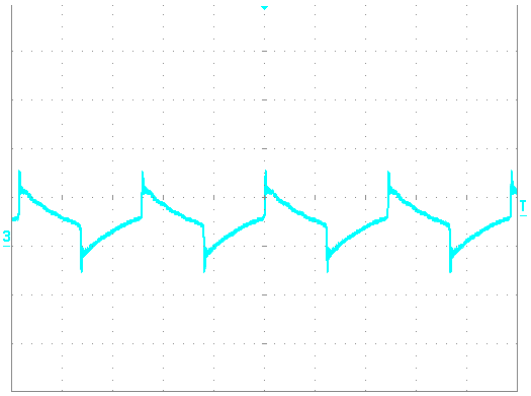



*Figure B.2 Photo of optical gate driver board with measurements labelled.*

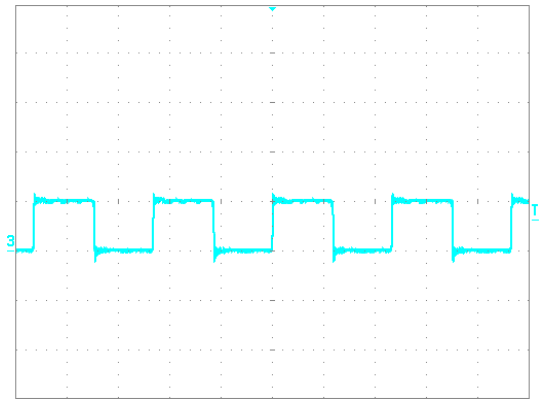
## B.1.1 Gate driver test data

1) Apply +5V DC supply between VCC and GND, when the input signal is rectangular wave with $V_{PP}$ = 5 V, $f$ = 20 kHz, $\delta$ = 50 %, nominal supply current is around 0.07 A. Supply current will increase after connecting switches at output or increase the frequency of the input signal.

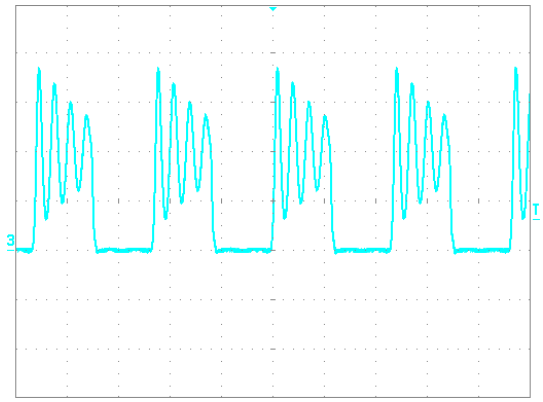
2) Test the capacitor charging voltage of the oscillation circuit from the pin 5 of the NAND gate IC. Signal scale = 5 V/div. Time scale = 200 ns/div.



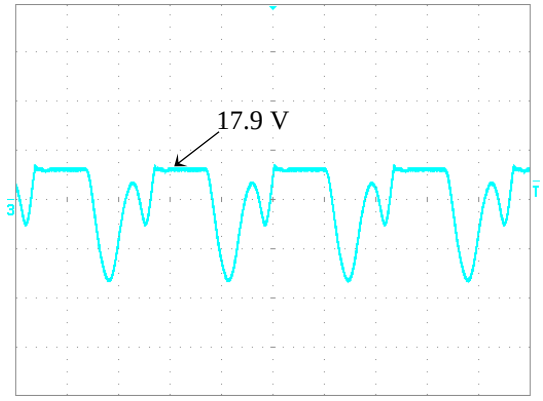
3) Test the output of oscillation circuit from the pin 8 of the NAND gate IC. Test signal scale = 5 V/div. Time scale = 200 ns/div. The frequency of the test signal is 2 MHz.



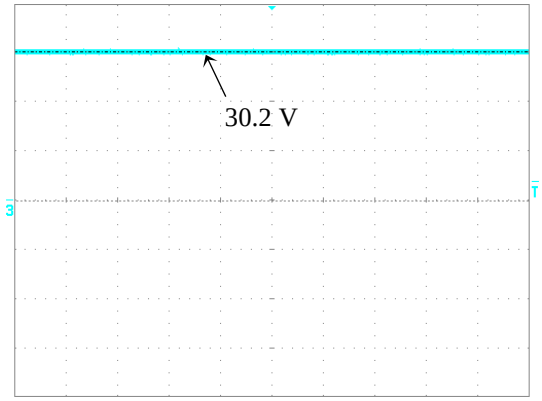
4) Test the Drain of MOSFET Q1. Test signal scale = 5 V/div. Time scale = 200 ns/div. The frequency of the test signal is 2 MHz.



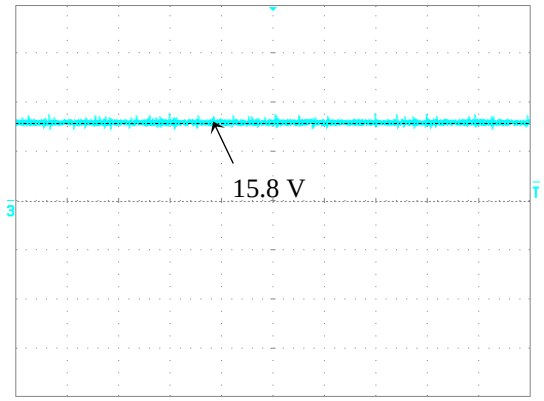
5) Test the secondary output of the flyback transformer T1. Test signal scale = 50 V/div. Time scale = 200 ns/div.



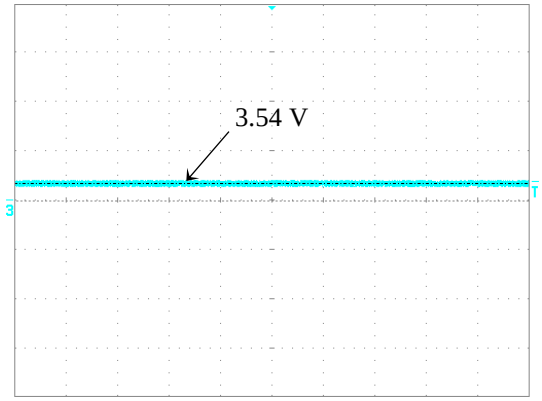
6) Test the voltage between VH and OVH.



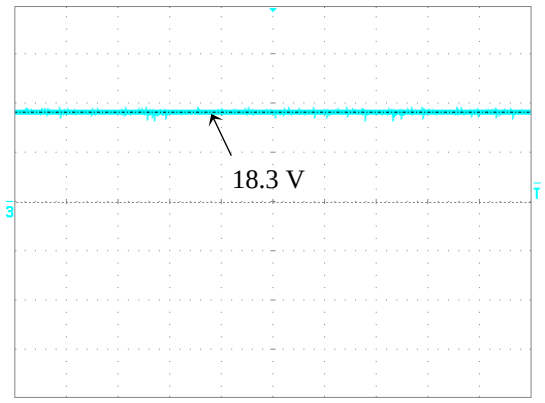

7) Test the voltage between VHR and OVH.



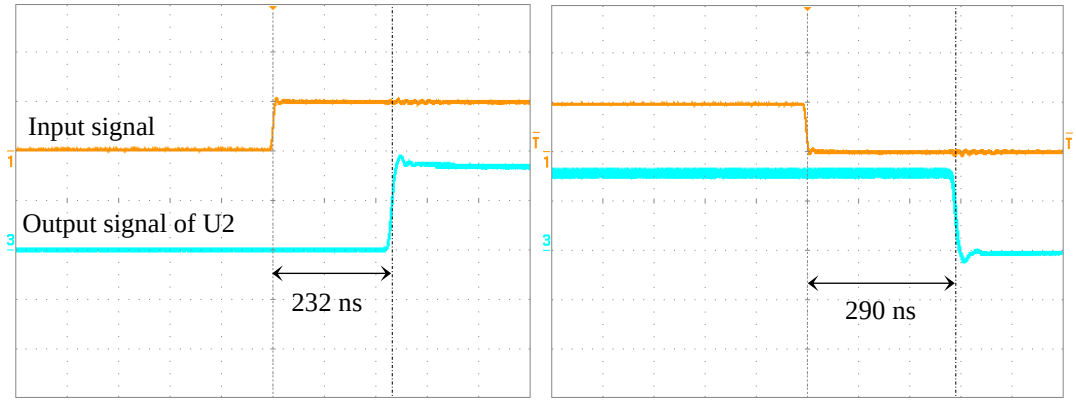

8) Test the voltage across the Zener diode D5.



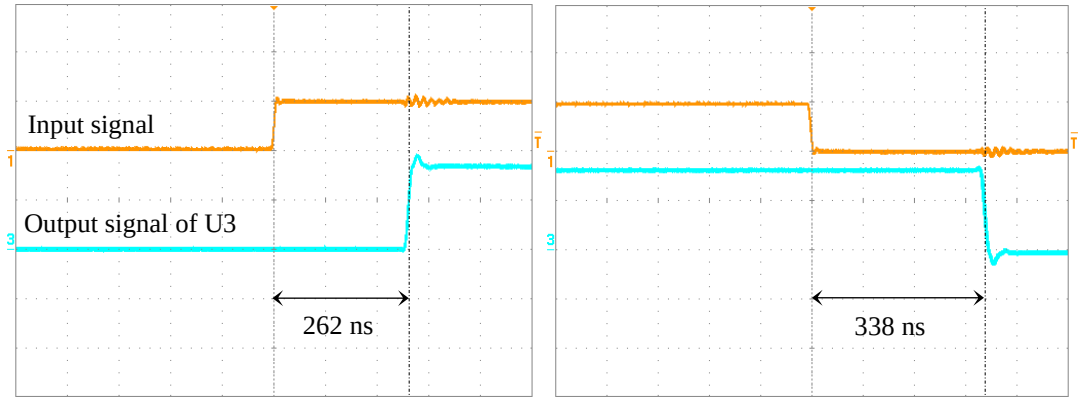

9) Test the voltage across the Zener diode D4.



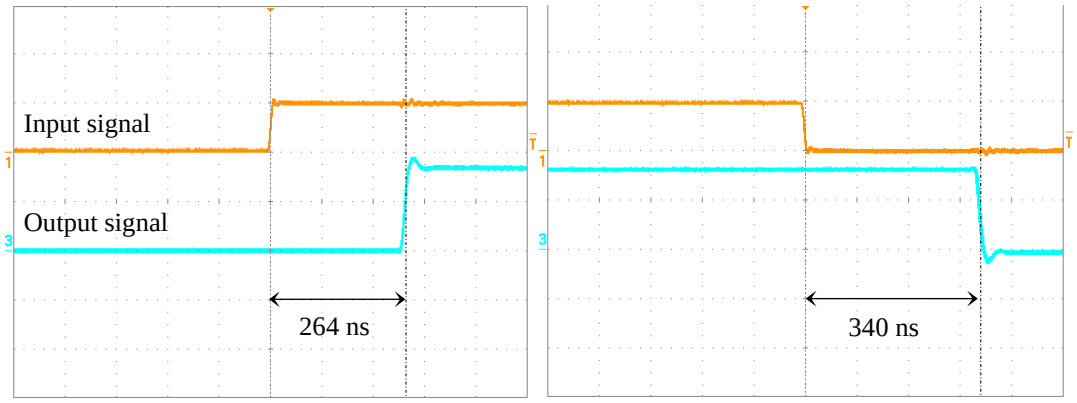

10) Test the input signal and the output signal of opto-coupler U2 at the rising edge and the falling edge. Signal scales = 5 V/div. Time scale = 100 ns/div.




11) Test the input signal and the output signal of Driver IC U3 at the rising edge and the falling edge. Signal scales = 5 V/div. Time scale = 100 ns/div.



12) Test the input signal and the output signal of driver board at the rising edge and the falling edge. Signal scales = 5 V/div. Time scale = 100 ns/div.




# B.2 Dual-mode gate driver

In the gate driver board arrangement in Figure 4.14, the signal *S*1 and *S*2 are two complementary input gate signals. EN is the enable signal for fast-switching mode. The *R*9 and *R*16 are 10Ω and they are the gate resistors in the fast-switching path. The *R*7 and *R*14 are 220Ω and they are gate resistors in the slow-switching path. The *R*6 and *R*13 are 10Ω and they are in the reverse path. The signal will go through the fast-switching path only when the EN signal is on. When the EN signal is off, the gate signals will go through the slow-switching path.

The Table B.2 shows the components lists of the dual-mode driver. Figure B.3 shows its schematic drawn in Altium Designer. Figure B.4 is the practical photo with labelled measurements.

*Table B.2 BOM of the dual-mode gate driver.*

| Identifier | Description | Manufacturer | Mfrs. Part no. | Supplier | Order code | Qty. | Unit cost | Sub-total |
|---|---|---|---|---|---|---|---|---|
| R1, 17 | Resistor 1k Ω | TT Electronics/Welwyn | WCR0805-1K0FI | Farnell | 1099800 | 2 | 0.0168 | 0.0336 |
| R2 | Resistor 22 Ω | TT Electronics/Welwyn | WCR0805-22RFI | Farnell | 1099789 | 1 | 0.0196 | 0.0196 |
| R3, 4, 10, 11 | Resistor 10k Ω | TT Electronics/Welwyn | WCR0805-10KFI | Farnell | 1099807 | 4 | 0.0196 | 0.0784 |
| R5, 8, 12, 15 | Resistor 470 Ω | TT Electronics/Welwyn | WCR0805-470RFI | Farnell | 1099798 | 4 | 0.0168 | 0.0672 |
| R6, 9, 13, 16 | Resistor 10 Ω | TT Electronics/Welwyn | WCR0805-10RFI | Farnell | 1099787 | 4 | 0.0196 | 0.0784 |
| R7, 14 | Resistor 100 Ω | TT Electronics/Welwyn | WCR0805-100RFI | Farnell | 1099793 | 2 | 0.0196 | 0.0392 |
| C1 | Capacitor 1 µF | Multicomp | MC0805B105K100CT | Farnell | 2320857 | 1 | 0.253 | 0.253 |
| C2 | Capacitor 220 pF | Multicomp | MCSH21B221K250CT | Farnell | 1856450 | 1 | 0.0988 | 0.0988 |
| C3, 4, 5, 7 | Capacitor 10 µF | Murata | GRM32ER7YA106KA12L | Farnell | 1735537 | 4 | 0.96 | 3.84 |
| C6, C8 | Capacitor 47 µF | Murata | GRM32ER71A476ME15L | Farnell | 1797018 | 2 | 1.35 | 2.7 |
| D1, 2, 5, 8, 9, 10 | Signal diode | On Semiconductor | 1N4148TR | Farnell | 9843680 | 6 | 0.0527 | 0.3162 |
| D3, 6 | Zener diode 18 V | Diodes Inc. | BZX84C18 | Farnell | 1902449 | 2 | 0.0981 | 0.1962 |
| D4, 7 | Zener diode 3.9 V | Diodes Inc. | BZX84C3V9 | Farnell | 1902458 | 2 | 0.0981 | 0.1962 |
| D11 | Red LED 1.8 V | ROHM | SML-211UTT86 | RS | 700-7907 | 1 | 0.4 | 0.4 |
| Q1, 2, 3 | MOSFET, N-Channel, 5.1 A, 55 V, 0.0462 ohm | Infineon | IRFL024ZPBF | RS | 650-4463 | 3 | 0.934 | 2.802 |
| U1 | Quad 2-input NAND gate | Fairchild Semiconductor | 74AC00SC | Farnell | 1014139 | 1 | 0.449 | 0.449 |
| U2, 4, 6, 8 | Opto-coupler | Broadcom Inc. | HCPL-0302-000E | Farnell | 9130160 | 4 | 1.11 | 4.44 |
| U3, 5, 7, 9 | Driver IC | IXYS | IXDN614SI | Mouser | 849-IXDN614SI | 4 | 3.23 | 12.92 |
| T1 | Transformer Core, Toroid, 3C90, 30.1 mm, 12.2 mm² | Ferroxcube | TN13/7.5/5-3C90 | Farnell | 178504 | 1 | 0.294 | 0.294 |
| | | | | | **Sum** | **£29.2218** | | |

*All costs are based on the prices on Farnell or Mouser in 2018.

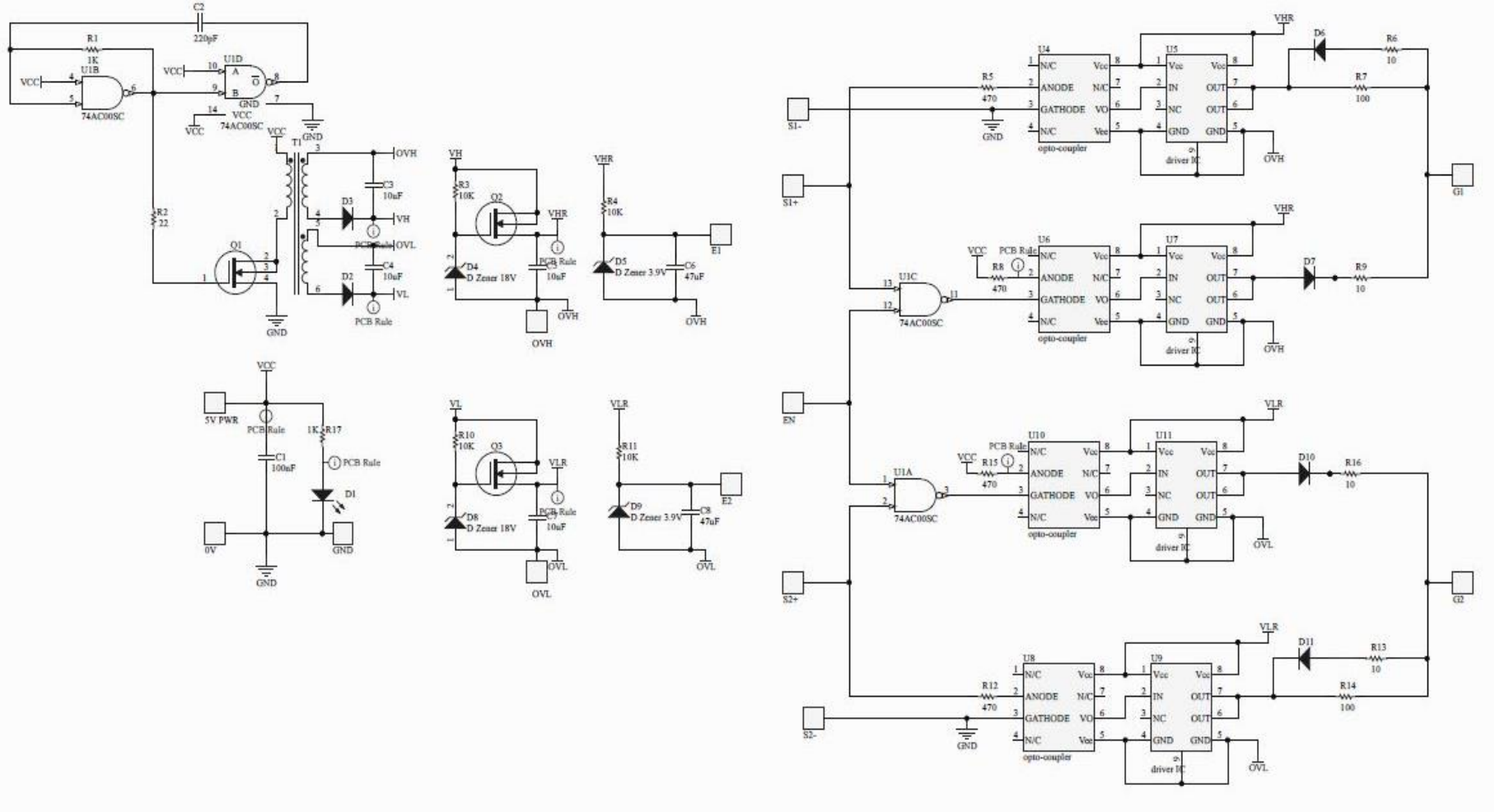



*Figure B.3 Schematic of dual-mode gate driver board.*

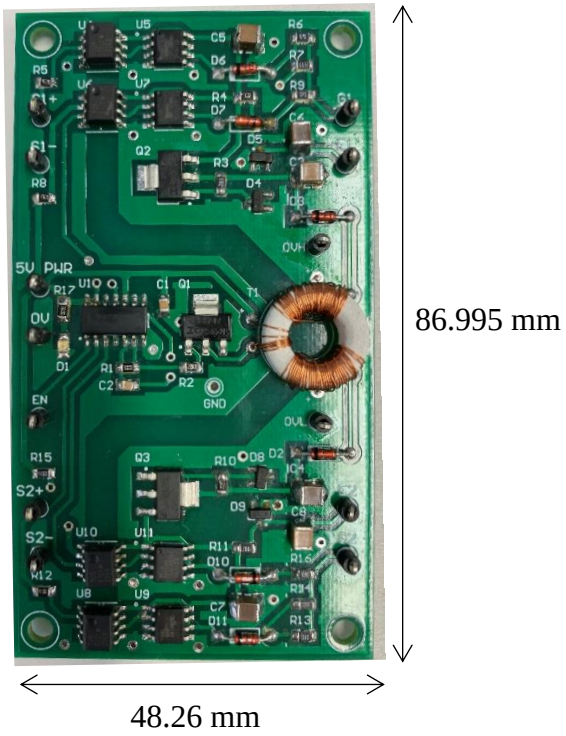



*Figure B.4 Photo of dual-mode gate driver board with measurements labelled.*

# Appendix C

# Coding of microcontroller

This Appendix contains the coding of the microcontroller PSoC when implementing it as the microcontroller in the previous chapters. Only the key sentences are shown in some sections.

## C.1 Coding of complementary 20 kHz SPWM

```
#include <project.h>
#include <math.h>
#include <stdio.h>
int16 i=0, m;
int32 output;
float sin_table[400]={0,                  0.0157073173118207,  0.0314107590781283,
 0.0471064507096427,  0.0627905195293134,  0.0784590957278449,  0.0941083133185143,
 0.109734311091045,   0.125333233564304,   0.140901231937583,   0.156434465040231,
 0.171929100279410,   0.187381314585725,   0.202787295356513,   0.218143241396543,
 0.233445363855905,   0.248689887164855,   0.263873049965373,   0.278991106039229,
 0.294040325232304,   0.309016994374947,   0.323917418198149,   0.338737920245291,
 0.353474843779257,   0.368124552684678,   0.382683432365090,   0.397147890634781,
 0.411514358605109,   0.425779291565073,   0.439939169855915,   0.453990499739547,
 0.467929814260573,   0.481753674101715,   0.495458668432408,   0.509041415750371,
```

```
0.522498564715949,  0.535826794978997,  0.549022817998132,  0.562083377852131,
0.575005252043279,  0.587785252292473,  0.600420225325884,  0.612907053652977,
0.625242656335705,  0.637423989748690,  0.649448048330184,  0.661311865323652,
0.673012513509773,  0.684547105928689,  0.695912796592314,  0.707106781186548,
0.718126297763189,  0.728968627421412,  0.739631094978610,  0.750111069630460,
0.760405965600031,  0.770513242775789,  0.780430407338330,  0.790155012375690,
0.799684658487091,  0.809016994374948,  0.818149717425024,  0.827080574274562,
0.835807361368270,  0.844327925502015,  0.852640164354092,  0.860742027003944,
0.868631514438191,  0.876306680043864,  0.883765630088694,  0.891006524188368,
0.898027575760616,  0.904827052466020,  0.911403276635445,  0.917754625683981,
0.923879532511287,  0.929776485888252,  0.935444030829867,  0.940880768954226,
0.946085358827545,  0.951056516295154,  0.955793014798330,  0.960293685676943,
0.964557418457798,  0.968583161128631,  0.972369920397677,  0.975916761938747,
0.979222810621766,  0.982287250728689,  0.985109326154774,  0.987688340595138,
0.990023657716558,  0.992114701314478,  0.993960955455180,  0.995561964603080,
0.996917333733128,  0.998026728428272,  0.998889874961970,  0.999506560365732,
0.999876632481661,  1,                  0.999876632481661,  0.999506560365732,
0.998889874961970,  0.998026728428272,  0.996917333733128,  0.995561964603080,
0.993960955455180,  0.992114701314478,  0.990023657716558,  0.987688340595138,
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0.739631094978610,  0.728968627421411,  0.718126297763189,  0.707106781186548,
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0.649448048330184,  0.637423989748690,  0.625242656335705,  0.612907053652976,
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0.263873049965373,  0.248689887164855,  0.233445363855905,  0.218143241396542,
0.202787295356512,  0.187381314585725,  0.171929100279410,  0.156434465040231,
0.140901231937582,  0.125333233564304,  0.109734311091045,  0.0941083133185144,
0.0784590957278446, 0.0627905195293131, 0.0471064507096425  0.0314107590781282,
0.0157073173118207, 0,                  -0.0157073173118205, -0.0314107590781280,
-0.0471064507096423, -0.0627905195293129, -0.0784590957278444, -0.0941083133185141,
-0.109734311091045,  -0.125333233564304,  -0.140901231937582,  -0.156434465040230,
-0.171929100279409,  -0.187381314585724,  -0.202787295356512,  -0.218143241396542,
```

```
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-0.294040325232304,  -0.309016994374947,  -0.323917418198149,  -0.338737920245291,
-0.353474843779257,  -0.368124552684678,  -0.382683432365089,  -0.397147890634780,
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-0.467929814260573,  -0.481753674101715,  -0.495458668432407,  -0.509041415750371,
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-0.718126297763189,  -0.728968627421411,  -0.739631094978610,  -0.750111069630459,
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-0.898027575760616,  -0.904827052466019,  -0.911403276635445,  -0.917754625683981,
-0.923879532511287,  -0.929776485888252,  -0.935444030829867,  -0.940880768954226,
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-0.979222810621766,  -0.982287250728689,  -0.985109326154774,  -0.987688340595138,
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-0.996917333733128,  -0.998026728428272,  -0.998889874961970,  -0.999506560365732,
-0.999876632481661,  -1,                  -0.999876632481661,  -0.999506560365732,
-0.998889874961970,  -0.998026728428272,  -0.996917333733128,  -0.995561964603080,
-0.993960955455180,  -0.992114701314478,  -0.990023657716558,  -0.987688340595138,
-0.985109326154774,  -0.982287250728689,  -0.979222810621766,  -0.975916761938748,
-0.972369920397677,  -0.968583161128631,  -0.964557418457798,  -0.960293685676943,
-0.955793014798330,  -0.951056516295154,  -0.946085358827545,  -0.940880768954226,
-0.935444030829868,  -0.929776485888252,  -0.923879532511287,  -0.917754625683982,
-0.911403276635445,  -0.904827052466020,  -0.898027575760616,  -0.891006524188368,
-0.883765630088694,  -0.876306680043864,  -0.868631514438192,  -0.860742027003944,
-0.852640164354093,  -0.844327925502015,  -0.835807361368270,  -0.827080574274562,
-0.818149717425024,  -0.809016994374948,  -0.799684658487091,  -0.790155012375691,
-0.780430407338330,  -0.770513242775790,  -0.760405965600031,  -0.750111069630460,
-0.739631094978610,  -0.728968627421412,  -0.718126297763189,  -0.707106781186548,
-0.695912796592315,  -0.684547105928689,  -0.673012513509774,  -0.661311865323652,
-0.649448048330184,  -0.637423989748690,  -0.625242656335705,  -0.612907053652977,
-0.600420225325884,  -0.587785252292473,  -0.575005252043279,  -0.562083377852131,
-0.549022817998132,  -0.535826794978997,  -0.522498564715949,  -0.509041415750372,
-0.495458668432408,  -0.481753674101715,  -0.467929814260574,  -0.453990499739547,
-0.439939169855915,  -0.425779291565073,  -0.411514358605109,  -0.397147890634781,
-0.382683432365090,  -0.368124552684678,  -0.353474843779257,  -0.338737920245291,
-0.323917418198150,  -0.309016994374948,  -0.294040325232304,  -0.278991106039230,
-0.263873049965373,  -0.248689887164855,  -0.233445363855906,  -0.218143241396542,
-0.202787295356512,  -0.187381314585725,  -0.171929100279410,  -0.156434465040231,
-0.140901231937583,  -0.125333233564305,  -0.109734311091046,  -0.0941083133185149,
```

```
-0.0784590957278456, -0.0627905195293133, -0.0471064507096426, -0.0314107590781284,
-0.0157073173118208};

/*******************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
* Handles the Interrupt Service Routine for the PWM Component.
*
*******************************************************************************/
CY_ISR(Isr_TC_Handler)
{
    flag_Write(1);

    PWM_ReadStatusRegister();

    m=0.8*300*(sin_table[i])+300;

    PWM_WriteCompare1(m);
    PWM_WriteCompare2(m);

    i++;
    if(i==400){i=0;}

    flag_Write(0);
}

/*******************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
*  This function:
*  1. Sets up and enables the PWM interrupt.
*  2. Starts the PWM Component.
*
*******************************************************************************/
int main()
{

    str_Write(1);

    /* Start the PWM Component */
    PWM_Start();
```

```
    PWM_WritePeriod(599);

    /* Enable the global interrupt */
    CyGlobalIntEnable;

    /* Enable the Interrupt component connected to the PWM interrupt output */
    Isr_TC_StartEx(Isr_TC_Handler);

    str_Write(0);
    str_1_Write(11);

    for(;;)
    {

    }
}
```

## C.2 Coding of dual-mode switching technique based on complementary 20 kHz SPWM with different SSR

### C.2.1 SSR=0.1

```
#include <project.h>
#include <math.h>
#include <stdio.h>

#define  up_band   324
#define  low_band  276

int16 i=0, m;
float sin_table[400]={0,                  0.0157073173118207,  0.0314107590781283,
 0.0471064507096427,  0.0627905195293134,  0.0784590957278449,  0.0941083133185143,
 0.109734311091045,   0.125333233564304,   0.140901231937583,   0.156434465040231,
 0.171929100279410,   0.187381314585725,   0.202787295356513,   0.218143241396543,
 0.233445363855905,   0.248689887164855,   0.263873049965373,   0.278991106039229,
 0.294040325232304,   0.309016994374947,   0.323917418198149,   0.338737920245291,
 0.353474843779257,   0.368124552684678,   0.382683432365090,   0.397147890634781,
 0.411514358605109,   0.425779291565073,   0.439939169855915,   0.453990499739547,
 0.467929814260573,   0.481753674101715,   0.495458668432408,   0.509041415750371,
 0.522498564715949,   0.535826794978997,   0.549022817998132,   0.562083377852131,
```

```
0.575005252043279,  0.587785252292473,  0.600420225325884,  0.612907053652977,
0.625242656335705,  0.637423989748690,  0.649448048330184,  0.661311865323652,
0.673012513509773,  0.684547105928689,  0.695912796592314,  0.707106781186548,
0.718126297763189,  0.728968627421412,  0.739631094978610,  0.750111069630460,
0.760405965600031,  0.770513242775789,  0.780430407338330,  0.790155012375690,
0.799684658487091,  0.809016994374948,  0.818149717425024,  0.827080574274562,
0.835807361368270,  0.844327925502015,  0.852640164354092,  0.860742027003944,
0.868631514438191,  0.876306680043864,  0.883765630088694,  0.891006524188368,
0.898027575760616,  0.904827052466020,  0.911403276635445,  0.917754625683981,
0.923879532511287,  0.929776485888252,  0.935444030829867,  0.940880768954226,
0.946085358827545,  0.951056516295154,  0.955793014798330,  0.960293685676943,
0.964557418457798,  0.968583161128631,  0.972369920397677,  0.975916761938747,
0.979222810621766,  0.982287250728689,  0.985109326154774,  0.987688340595138,
0.990023657716558,  0.992114701314478,  0.993960955455180,  0.995561964603080,
0.996917333733128,  0.998026728428272,  0.998889874961970,  0.999506560365732,
0.999876632481661,  1,                  0.999876632481661,  0.999506560365732,
0.998889874961970,  0.998026728428272,  0.996917333733128,  0.995561964603080,
0.993960955455180,  0.992114701314478,  0.990023657716558,  0.987688340595138,
0.985109326154774,  0.982287250728689,  0.979222810621766,  0.975916761938747,
0.972369920397677,  0.968583161128631,  0.964557418457798,  0.960293685676943,
0.955793014798330,  0.951056516295154,  0.946085358827545,  0.940880768954226,
0.935444030829867,  0.929776485888252,  0.923879532511287,  0.917754625683981,
0.911403276635445,  0.904827052466020,  0.898027575760616,  0.891006524188368,
0.883765630088693,  0.876306680043864,  0.868631514438191,  0.860742027003944,
0.852640164354092,  0.844327925502015,  0.835807361368270,  0.827080574274562,
0.818149717425023,  0.809016994374948,  0.799684658487090,  0.790155012375690,
0.780430407338330,  0.770513242775789,  0.760405965600031,  0.750111069630459,
0.739631094978610,  0.728968627421411,  0.718126297763189,  0.707106781186548,
0.695912796592314,  0.684547105928689,  0.673012513509773,  0.661311865323652,
0.649448048330184,  0.637423989748690,  0.625242656335705,  0.612907053652976,
0.600420225325884,  0.587785252292473,  0.575005252043278,  0.562083377852131,
0.549022817998132,  0.535826794978997,  0.522498564715949,  0.509041415750371,
0.495458668432407,  0.481753674101715,  0.467929814260573,  0.453990499739546,
0.439939169855915,  0.425779291565073,  0.411514358605109,  0.397147890634781,
0.382683432365089,  0.368124552684678,  0.353474843779257,  0.338737920245291,
0.323917418198149,  0.309016994374947,  0.294040325232304,  0.278991106039229,
0.263873049965373,  0.248689887164855,  0.233445363855905,  0.218143241396542,
0.202787295356512,  0.187381314585725,  0.171929100279410,  0.156434465040231,
0.140901231937582,  0.125333233564304,  0.109734311091045,  0.0941083133185144,
0.0784590957278446, 0.0627905195293131, 0.0471064507096425  0.0314107590781282,
0.0157073173118207, 0,                  -0.0157073173118205, -0.0314107590781280,
-0.0471064507096423, -0.0627905195293129, -0.0784590957278444, -0.0941083133185141,
-0.109734311091045, -0.125333233564304, -0.140901231937582, -0.156434465040230,
-0.171929100279409, -0.187381314585724, -0.202787295356512, -0.218143241396542,
-0.233445363855905, -0.248689887164855, -0.263873049965373, -0.278991106039229,
```

```
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-0.353474843779257,  -0.368124552684678,  -0.382683432365089,  -0.397147890634780,
-0.411514358605109,  -0.425779291565072,  -0.439939169855915,  -0.453990499739546,
-0.467929814260573,  -0.481753674101715,  -0.495458668432407,  -0.509041415750371,
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-0.575005252043278,  -0.587785252292473,  -0.600420225325884,  -0.612907053652976,
-0.625242656335705,  -0.637423989748689,  -0.649448048330184,  -0.661311865323652,
-0.673012513509773,  -0.684547105928688,  -0.695912796592314,  -0.707106781186548,
-0.718126297763189,  -0.728968627421411,  -0.739631094978610,  -0.750111069630459,
-0.760405965600031,  -0.770513242775789,  -0.780430407338329,  -0.790155012375690,
-0.799684658487090,  -0.809016994374947,  -0.818149717425023,  -0.827080574274562,
-0.835807361368270,  -0.844327925502015,  -0.852640164354092,  -0.860742027003943,
-0.868631514438191,  -0.876306680043863,  -0.883765630088693,  -0.891006524188368,
-0.898027575760616,  -0.904827052466019,  -0.911403276635445,  -0.917754625683981,
-0.923879532511287,  -0.929776485888252,  -0.935444030829867,  -0.940880768954226,
-0.946085358827545,  -0.951056516295154,  -0.955793014798330,  -0.960293685676943,
-0.964557418457798,  -0.968583161128631,  -0.972369920397676,  -0.975916761938747,
-0.979222810621766,  -0.982287250728689,  -0.985109326154774,  -0.987688340595138,
-0.990023657716558,  -0.992114701314478,  -0.993960955455180,  -0.995561964603080,
-0.996917333733128,  -0.998026728428272,  -0.998889874961970,  -0.999506560365732,
-0.999876632481661,  -1,                  -0.999876632481661,  -0.999506560365732,
-0.998889874961970,  -0.998026728428272,  -0.996917333733128,  -0.995561964603080,
-0.993960955455180,  -0.992114701314478,  -0.990023657716558,  -0.987688340595138,
-0.985109326154774,  -0.982287250728689,  -0.979222810621766,  -0.975916761938748,
-0.972369920397677,  -0.968583161128631,  -0.964557418457798,  -0.960293685676943,
-0.955793014798330,  -0.951056516295154,  -0.946085358827545,  -0.940880768954226,
-0.935444030829868,  -0.929776485888252,  -0.923879532511287,  -0.917754625683982,
-0.911403276635445,  -0.904827052466020,  -0.898027575760616,  -0.891006524188368,
-0.883765630088694,  -0.876306680043864,  -0.868631514438192,  -0.860742027003944,
-0.852640164354093,  -0.844327925502015,  -0.835807361368270,  -0.827080574274562,
-0.818149717425024,  -0.809016994374948,  -0.799684658487091,  -0.790155012375691,
-0.780430407338330,  -0.770513242775790,  -0.760405965600031,  -0.750111069630460,
-0.739631094978610,  -0.728968627421412,  -0.718126297763189,  -0.707106781186548,
-0.695912796592315,  -0.684547105928689,  -0.673012513509774,  -0.661311865323652,
-0.649448048330184,  -0.637423989748690,  -0.625242656335705,  -0.612907053652977,
-0.600420225325884,  -0.587785252292473,  -0.575005252043279,  -0.562083377852131,
-0.549022817998132,  -0.535826794978997,  -0.522498564715949,  -0.509041415750372,
-0.495458668432408,  -0.481753674101715,  -0.467929814260574,  -0.453990499739547,
-0.439939169855915,  -0.425779291565073,  -0.411514358605109,  -0.397147890634781,
-0.382683432365090,  -0.368124552684678,  -0.353474843779257,  -0.338737920245291,
-0.323917418198150,  -0.309016994374948,  -0.294040325232304,  -0.278991106039230,
-0.263873049965373,  -0.248689887164855,  -0.233445363855906,  -0.218143241396542,
-0.202787295356512,  -0.187381314585725,  -0.171929100279410,  -0.156434465040231,
-0.140901231937583,  -0.125333233564305,  -0.109734311091046,  -0.0941083133185149,
-0.0784590957278456, -0.0627905195293133, -0.0471064507096426, -0.0314107590781284,
```

```
-0.0157073173118208};

/*******************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
* Handles the Interrupt Service Routine for the PWM Component.
*
*******************************************************************************/
CY_ISR(Isr_TC_Handler)
{
    flag_Write(1);

    PWM_ReadStatusRegister();

    m=0.8*300*(sin_table[i])+300;

    PWM_WriteCompare1(m);
    PWM_WriteCompare2(m);

    if( m > up_band)
    {
        str_1_Write(10);
    }

    if(( m <= up_band)&&( m >= low_band))
    {
        str_1_Write(11);
    }

    if( m < low_band)
    {
        str_1_Write(01);
    }

    i++;
    if(i==400){i=0;}

    flag_Write(0);
}

/*******************************************************************************
* Function Name: Isr_TC_Handler
*******************************************************************************
```

```
154 *
155 * Summary:
156 *  This function:
157 *  1. Sets up and enables the PWM interrupt.
158 *  2. Starts the PWM Component.
159 *
160 ********************************************************************************/
161 int main()
162 {
163
164     str_Write(1);
165
166     /* Start the PWM Component */
167     PWM_Start();
168     PWM_WritePeriod(599);
169
170     /* Enable the global interrupt */
171     CyGlobalIntEnable;
172
173     /* Enable the Interrupt component connected to the PWM interrupt output */
174     Isr_TC_StartEx(Isr_TC_Handler);
175
176     str_Write(0);
177     str_1_Write(11);
178
179     for(;;)
180     {
181     }
182
183 }
```

## C.2.2 SSR = 0.2

```
1 #define  up_band   348
2 #define  low_band  252
```

## C.2.3 SSR = 0.3

```
1 #define  up_band   372
2 #define  low_band  228
```

### C.2.4 SSR = 0.4

```
#define  up_band   396
#define  low_band  204
```

### C.2.5 SSR=0.5

```
#define  up_band   420
#define  low_band  180
```

### C.2.6 SSR=0.6

```
#define  up_band   444
#define  low_band  156
```

### C.2.7 SSR=0.7

```
#define  up_band   492
#define  low_band  108
```

## C.3 Coding of dual-mode switching technique based on complementary 15 kHz SPWM when SSR = 0.1

```
#include <project.h>
#include <math.h>
#include <stdio.h>

#define  up_band   1919
#define  low_band  1279

int16 i=0, m;
float sin_table[300]={0,                  0.0210124511284754,  0.0420156237500571,
0.0630002434549789,  0.0839570440259202,  0.104876771529707,   0.125750188403588,
0.146568077534282,   0.167321246327997,   0.188000530769618,   0.208596799469283,
0.229100957694542,   0.249503951386338,   0.269796771157024,   0.289970456268657,
0.310016098589803,   0.329924846529121,   0.349687908943976,   0.369296559022357,
0.388742138136397,   0.408016059665773,   0.427109812789322,   0.446014966243175,
0.464723172043769,   0.483226169174079,   0.501515787231454,   0.519583950035434,
```

```
0.537422679193963,  0.555024097626425,  0.572380433041942,  0.589484021371395,
0.606327310151662,  0.622902861860577,  0.639203357201126,  0.655221598333444,
0.670950512053178,  0.686383152914818,  0.701512706298604,  0.716332491419678,
0.730835964278124,  0.745016720548617,  0.758868498408392,  0.772385181302290,
0.785560800643656,  0.798389538449896,  0.810865729911540,  0.822983865893657,
0.834738595368536,  0.846124727778551,  0.857137235328163,  0.867771255204052,
0.878022091722401,  0.887885218402375,  0.897356279964893,  0.906431094255788,
0.915105654092536,  0.923376129033713,  0.931238867070408,  0.938690396238849,
0.945727426153523,  0.952346849460122,  0.958545743207658,  0.964321370139157,
0.969671179900357,  0.974592810165871,  0.979084087682323,  0.983143029227997,
0.986767842488569,  0.989956926848547,  0.992708874098054,  0.995022469054655,
0.996896690099946,  0.998330709630677,  0.999323894424192,  0.999875805918045,
0.999986200403657,  0.999655029133931,  0.998882438344777,  0.997668769190539,
0.996014557593349,  0.993920534006479,  0.991387623091797,  0.988416943311459,
0.985009806434027,  0.981167716955231,  0.976892371433627,  0.972185657741440,
0.967049654230938,  0.961486628816687,  0.955499037974103,  0.949089525654746,
0.942260922118821,  0.935016242685415,  0.927358686401021,  0.919291634626925,
0.910818649546093,  0.901943472590214,  0.892670022787583,  0.883002395032577,
0.872944858277456,  0.862501853647320,  0.851677992479032,  0.840478054284980,
0.828906984642578,  0.816969893010442,  0.804672050472194,  0.792018887408900,
0.779015991101168,  0.765669103261961,  0.751984117501218,  0.737967076723404,
0.723624170459130,  0.708961732132033,  0.693986236262114,  0.678704295606772,
0.663122658240795,  0.647248204576604,  0.631087944326053,  0.614649013405138,
0.597938670782979,  0.580964295276463,  0.563733382291966,  0.546253540515591,
0.528532488553389,  0.510578051523038,  0.492398157598494,  0.474000834509128,
0.455394205994911,  0.436586488219197,  0.417585986140696,  0.398401089846241,
0.379040270845959,  0.359512078332490,  0.339825135405907,  0.319988135265998,
0.300009837373588,  0.279899063582616,  0.259664694244646,  0.239315664287558,
0.218860959270131,  0.198309611414277,  0.177670695616667,  0.156953325441506,
0.136166649096247,  0.115319845391994,  0.0944221196904026,  0.073482699838847,
0.052510832095665,  0.0315157770472698,  0.0105068055189363, -0.0105068055189361,
-0.03151577704727, -0.0525108320956652, -0.0734826998388472, -0.0944221196904028,
-0.115319845391994, -0.136166649096247, -0.156953325441506, -0.177670695616667,
-0.198309611414277, -0.218860959270131, -0.239315664287558, -0.259664694244646,
-0.279899063582616, -0.300009837373588, -0.319988135265998, -0.339825135405908,
-0.35951207833249, -0.379040270845959, -0.398401089846242, -0.417585986140697,
-0.436586488219197, -0.455394205994911, -0.474000834509128, -0.492398157598494,
-0.510578051523038, -0.528532488553389, -0.54625354051559,  -0.563733382291966,
-0.580964295276463, -0.597938670782979, -0.614649013405138, -0.631087944326053,
-0.647248204576604, -0.663122658240795, -0.678704295606772, -0.693986236262114,
-0.708961732132034, -0.723624170459131, -0.737967076723404, -0.751984117501218,
-0.765669103261961, -0.779015991101168, -0.792018887408900, -0.804672050472194,
-0.816969893010442, -0.828906984642578, -0.84047805428498,  -0.851677992479033,
-0.862501853647321, -0.872944858277456, -0.883002395032577, -0.892670022787583,
-0.901943472590214, -0.910818649546093, -0.919291634626925, -0.927358686401021,
```

```
-0.935016242685415, -0.94226092211882,   -0.949089525654746,  -0.955499037974103,
-0.961486628816687, -0.967049654230938,  -0.97218565774144,   -0.976892371433627,
-0.981167716955231, -0.985009806434027,  -0.988416943311459,  -0.991387623091797,
-0.993920534006479, -0.996014557593349,  -0.997668769190539,  -0.998882438344777,
-0.999655029133931, -0.999986200403657,  -0.999875805918045,  -0.999323894424192,
-0.998330709630677, -0.996896690099946,  -0.995022469054655,  -0.992708874098054,
-0.989956926848547, -0.986767842488569,  -0.983143029227997,  -0.979084087682323,
-0.974592810165871, -0.969671179900357,  -0.964321370139156,  -0.958545743207658,
-0.952346849460122, -0.945727426153523,  -0.938690396238848,  -0.931238867070408,
-0.923376129033713, -0.915105654092536,  -0.906431094255788,  -0.897356279964892,
-0.887885218402376, -0.878022091722401,  -0.867771255204052,  -0.857137235328163,
-0.846124727778552, -0.834738595368536,  -0.822983865893657,  -0.81086572991154,
-0.798389538449896, -0.785560800643656,  -0.77238518130229,   -0.758868498408392,
-0.745016720548617, -0.730835964278124,  -0.716332491419678,  -0.701512706298604,
-0.686383152914817, -0.670950512053178,  -0.655221598333443,  -0.639203357201126,
-0.622902861860577, -0.606327310151662,  -0.589484021371394,  -0.572380433041942,
-0.555024097626425, -0.537422679193962,  -0.519583950035433,  -0.501515787231453,
-0.483226169174079, -0.464723172043768,  -0.446014966243175,  -0.427109812789322,
-0.408016059665773, -0.388742138136397,  -0.369296559022357,  -0.349687908943976,
-0.329924846529122, -0.310016098589803,  -0.289970456268657,  -0.269796771157024,
-0.249503951386338, -0.229100957694542,  -0.208596799469283,  -0.188000530769618,
-0.167321246327996, -0.146568077534282,  -0.125750188403587,  -0.104876771529707,
-0.0839570440259198,-0.0630002434549785, -0.0420156237500566, -0.0210124511284757,
-0.00000000000000024493};

/*******************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
* Handles the Interrupt Service Routine for the PWM Component.
*
*******************************************************************************/
CY_ISR(Isr_TC_Handler)
{
    flag_Write(1);

    PWM_ReadStatusRegister();

    m=0.9*1599*(sin_table[i])+1599;

    PWM_WriteCompare1(m);
    PWM_WriteCompare2(m);

    if( m > up_band)
```

```
106         {
107             str_1_Write(10);
108         }
109 
110         if(( m <= up_band)&&( m >= low_band))
111         {
112             str_1_Write(11);
113         }
114 
115         if( m < low_band)
116         {
117             str_1_Write(01);
118         }
119 
120         i++;
121         if(i==300){i=0;}
122 
123         flag_Write(0);
124     }
125 
126     /*******************************************************************************
127     * Function Name: Isr_TC_Handler
128     ********************************************************************************
129     *
130     * Summary:
131     *  This function:
132     *  1. Sets up and enables the PWM interrupt.
133     *  2. Starts the PWM Component.
134     *
135     *******************************************************************************/
136     int main()
137     {
138 
139         str_Write(1);
140 
141         /* Start the PWM Component */
142         PWM_Start();
143         PWM_WritePeriod(3199);
144 
145         /* Enable the global interrupt */
146         CyGlobalIntEnable;
147 
148         /* Enable the Interrupt component connected to the PWM interrupt output */
149         Isr_TC_StartEx(Isr_TC_Handler);
150 
```

```
151       str_Write(0);
152       str_1_Write(11);
153
154       for(;;)
155       {
156       }
157
158   }
```

## C.4 Coding of dual-mode switching technique based on complementary 25 kHz SPWM when SSR = 0.1

```
1   #include <project.h>
2   #include <math.h>
3   #include <stdio.h>
4
5   #define  up_band   1151
6   #define  low_band  767
7
8   int16 i=0, m;
9   float sin_table[500]={0,
10   0.0125912209984566,  0.0251804457201385,  0.0377656782047709,  0.0503449231250287,
11   0.0629161861028862,  0.0754774740258155,  0.0880267953627852,  0.100562160480008,
12   0.113081581956387,   0.125583074898612,   0.138064657255855,   0.150524350134013,
13   0.162960178109456,   0.175370169542214,   0.18775235688858,    0.200104777013045,
14   0.21242547149955,    0.224712486961982,   0.236963875353873,   0.249177694277252,
15   0.261352007290607,   0.273484884215892,   0.285574401444556,   0.297618642242511,
16   0.309615697054031,   0.321563663804496,   0.333460648201961,   0.345304764037483,
17   0.357094133484172,   0.368826887394914,   0.380501165598708,   0.392115117195597,
18   0.403666900850109,   0.415154685083199,   0.426576648562618,   0.437930980391677,
19   0.449215880396357,   0.460429559410714,   0.471570239560547,   0.48263615454527,
20   0.493625549917948,   0.50453668336346,    0.515367824974731,   0.526117257527001,
21   0.536783276750087,   0.547364191598579,   0.557858324519953,   0.568264011720537,
22   0.578579603429298,   0.588803464159403,   0.598933972967519,   0.608969523710807,
23   0.618908525301566,   0.628749401959493,   0.638490593461515,   0.648130555389156,
24   0.657667759373395,   0.667100693336983,   0.676427861734175,   0.685647785787841,
25   0.694759003723921,   0.703760071003178,   0.712649560550228,   0.721426062979791,
26   0.730088186820146,   0.738634558733738,   0.747063823734919,   0.75537464540477,
27   0.763565706102986,   0.771635707176781,   0.779583369166782,   0.787407432009883,
28   0.79510665523902,    0.802679818179844,   0.810125720144247,   0.817443180620733,
29   0.824631039461575,   0.831688157066758,   0.83861341456465,    0.845405713989399,
30   0.852063978455007,   0.858587152326065,   0.864974201385123,   0.871224112996653,
```

```
 0.877335896267606,  0.883308582204506,  0.889141223867081,  0.8948328965184,
 0.90038269777148,   0.905789747732357,  0.911053189139591,  0.916172187500177,
 0.921145931221853,  0.925973631741772,  0.930654523651526,  0.935187864818497,
 0.939572936503519,  0.943809043474828,  0.947895514118295,  0.951831700543896,
 0.955616978688443,  0.959250748414519,  0.962732433605629,  0.966061482257539,
 0.969237366565798,  0.972259583009414,  0.975127652430686,  0.977841120111175,
 0.980399555843794,  0.982802554001014,  0.985049733599182,  0.987140738358913,
 0.989075236761586,  0.990852922101899,  0.992473512536499,  0.993936751128663,
 0.995242405889039,  0.996390269812421,  0.997380160910576,  0.998211922241088,
 0.99888542193225,   0.999400553203966,  0.999757234384681,  0.99995540892433,
 0.999995045403306,  0.999876137537437,  0.999598704178987,  0.999162789313664,
 0.998568462053647,  0.997815816626628,  0.996904972360875,  0.995836073666312,
 0.99460929001162,   0.993224815897374,  0.991682870825204,  0.989983699262992,
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-0.125583074898611,  -0.113081581956386,  -0.100562160480008,  -0.088026795362785,
-0.0754774740258149, -0.0629161861028862, -0.0503449231250285, -0.0377656782047703,
-0.0251804457201385, -0.0125912209984563, -0.00000000000000024493};

/*******************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
* Handles the Interrupt Service Routine for the PWM Component.
*
*******************************************************************************/
CY_ISR(Isr_TC_Handler)
{
    flag_Write(1);

    PWM_ReadStatusRegister();

    m=0.9*959*(sin_table[i])+959;

    PWM_WriteCompare1(m);
    PWM_WriteCompare2(m);

    if( m > up_band)
    {
        str_1_Write(10);
    }

    if(( m <= up_band)&&( m >= low_band))
    {
        str_1_Write(11);
    }

    if( m < low_band)
```

```
166         {
167             str_1_Write(01);
168         }
169 
170         i++;
171         if(i==500){i=0;}
172 
173         flag_Write(0);
174     }
175 
176     /*******************************************************************************
177     * Function Name: Isr_TC_Handler
178     ********************************************************************************
179     *
180     * Summary:
181     *  This function:
182     *  1. Sets up and enables the PWM interrupt.
183     *  2. Starts the PWM Component.
184     *
185     *******************************************************************************/
186     int main()
187     {
188 
189         str_Write(1);
190 
191         /* Start the PWM Component */
192         PWM_Start();
193         PWM_WritePeriod(1919);
194 
195         /* Enable the global interrupt */
196         CyGlobalIntEnable;
197 
198         /* Enable the Interrupt component connected to the PWM interrupt output */
199         Isr_TC_StartEx(Isr_TC_Handler);
200 
201         str_Write(0);
202         str_1_Write(11);
203 
204         for(;;)
205         {
206         }
207 
208     }
```

# C.5 Coding of dual-mode switching technique based on complementary 30 kHz SPWM when SSR = 0.1

```
#include <project.h>
#include <math.h>
#include <stdio.h>

#define  up_band   959
#define  low_band  639

int16 i=0, m;
float sin_table[600]={
 0,                  0.010489265585975,  0.020977377061983,  0.0314631804450411,
 0.0419455220061205, 0.0524232483970888, 0.0628952067776104, 0.0733602449419907,
 0.0838172114459504, 0.0942649557333169, 0.104702328262617,  0.115128180633558,
 0.125541365713385,  0.135940737763095,  0.146325152563502,  0.156693467541132,
 0.167044541893937,  0.177377236716816,  0.187690415126926,  0.197982942388771,
 0.208253686039053,  0.218501516011274,  0.228725304760078,  0.238923927385308
 0.24909626175578,   0.259241188632745,  0.269357591793039,  0.27944435815189,
 0.289500377885424,  0.299524544552705,  0.309515755217548,  0.319472910569832,
 0.329394915046465,  0.339280676951926,  0.349129108578382,  0.358939126325364,
 0.368709650818996,  0.378439607030753,  0.388127924395748,  0.397773536930519,
 0.40737538335032,   0.416932407185891,  0.426443556899698,  0.435907786001632,
 0.445324053164152,  0.454691322336862,  0.464008562860499,  0.473274749580342,
 0.482488862959,     0.491649889188596,  0.50075682030231,   0.509808654285283,
 0.51880439518487,   0.527743053220217,  0.536623644891169,  0.545445193086482,
 0.554206727191328,  0.562907283194095,  0.571545903792451,  0.580121638498676,
 0.58863354374424,   0.597080682983626,  0.605462126797369,  0.613776952994325,
 0.622024246713133,  0.630203100522876,  0.638312614522925,  0.646351896441953,
 0.654320061736106,  0.662216233686333,  0.670039543494844,  0.677789130380706,
 0.68546414167455,   0.693063732912389,  0.700587067928534,  0.708033318947594,
 0.715401666675553,  0.722691300389918,  0.729901418028917,  0.737031226279754,
 0.744079940665889,  0.751046785633355,  0.757930994636093,  0.764731810220288,
 0.771448484107713,  0.778080277278061,  0.784626460050256,  0.79108631216274,
 0.797459122852718,  0.803744190934367,  0.809940824875981,  0.816048342876063,
 0.822066072938336,  0.82799335294569,   0.833829530733024,  0.839573964159008,
 0.845226021176736,  0.850785079903265,  0.856250528688044,  0.861621766180209,
 0.866898201394751,  0.872079253777538,  0.877164353269194,  0.882152940367821,
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```

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0.999721502710217,   0.99941896705597,    0.999006467612394,   0.998484049765862,
0.997851770996819,   0.997109700873456,   0.996257921044055,   0.9952965252280080,
0.994225619205504,   0.99304532080589,    0.991755759894707,   0.9903570783594,
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-0.0733602449419898, -0.0628952067776105, -0.0524232483970889, -0.0419455220061206,
-0.0314631804450412, -0.0209773770619823, -0.0104892655859743,
-0.00000000000000244929};

/********************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
* Handles the Interrupt Service Routine for the PWM Component.
*
********************************************************************************/
CY_ISR(Isr_TC_Handler)
{
    flag_Write(1);

    PWM_ReadStatusRegister();

    m=0.9*799*(sin_table[i])+799;
```

```
176
177       PWM_WriteCompare1(m);
178       PWM_WriteCompare2(m);
179
180       if( m > up_band)
181       {
182           str_1_Write(10);
183       }
184
185       if(( m <= up_band)&&( m >= low_band))
186       {
187           str_1_Write(11);
188       }
189
190       if( m < low_band)
191       {
192           str_1_Write(01);
193       }
194
195       i++;
196       if(i==600){i=0;}
197
198       flag_Write(0);
199   }
200
201   /*******************************************************************************
202   * Function Name: Isr_TC_Handler
203   ********************************************************************************
204   *
205   * Summary:
206   *  This function:
207   *  1. Sets up and enables the PWM interrupt.
208   *  2. Starts the PWM Component.
209   *
210   *******************************************************************************/
211   int main()
212   {
213
214       str_Write(1);
215
216       /* Start the PWM Component */
217       PWM_Start();
218       PWM_WritePeriod(1599);
219
220       /* Enable the global interrupt */
```

```
    CyGlobalIntEnable;

    /* Enable the Interrupt component connected to the PWM interrupt output */
    Isr_TC_StartEx(Isr_TC_Handler);

    str_Write(0);
    str_1_Write(11);

    for(;;)
    {
    }

}
```

## C.6 Coding of dual-mode switching technique based on complementary 35 kHz SPWM when SSR = 0.1

```
#include <project.h>
#include <math.h>
#include <stdio.h>

#define  up_band   821.5
#define  low_band  547.5

int16 i=0, m;
float sin_table[700]={0,                    0.00898869913465449, 0.0179766719973021
 0.0269631923746177,  0.0359475341706344,  0.044928971465411,   0.0539067785736854,
 0.0628802301035085,  0.0718486010148547,  0.0808111666782039,  0.0897672029330904,
 0.0987159861466141,  0.107656793271909,   0.116588901906562,   0.125511590350986,
 0.134424137666728,   0.143325823734723,   0.152215929313476,   0.161093736097175,
 0.169958526773732,   0.178809585082738,   0.187646195873338,   0.196467645162011,
 0.205273220190261,   0.214062209482205,   0.222833902902062,   0.231587591711527,
 0.240322568627038,   0.249038127876924,   0.257733565258428,   0.266408178194608,
 0.275061265791101,   0.283692128892757,   0.292300070140129,   0.300884394025816,
 0.309444406950663,   0.317979417279797,   0.326488735398518,   0.334971673768009,
 0.343427546980898,   0.351855671816628,   0.360255367296669,   0.368625954739534,
 0.376966757815617,   0.38527710260184,    0.393556317636104,   0.401803733971544,
 0.410018685230574,   0.418200507658737,   0.426348540178325,   0.434462124441804,
 0.442540604884999,   0.450583328780066,   0.458589646288232,   0.466558910512298,
 0.474490477548911,   0.482383706540586,   0.490237959727492,   0.498052602498974,
 0.505827003444837,   0.513560534406356,   0.521252570527035,   0.528902490303092,
 0.536509675633676,   0.544073511870806,   0.55159338786904,    0.559068696034848,
```

```
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0.62424248500937,   0.63123951334798,   0.638185538579102,  0.645079999475396,
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-0.0359475341706345, -0.026963192374617,  -0.0179766719973015,-0.00898869913465382
-0.000000000000002449294};

/*******************************************************************************
* Function Name: Isr_TC_Handler
********************************************************************************
*
* Summary:
* Handles the Interrupt Service Routine for the PWM Component.
*
*******************************************************************************/
CY_ISR(Isr_TC_Handler)
{
    flag_Write(1);

    PWM_ReadStatusRegister();

    m=0.9*684.5*(sin_table[i])+684.5;

    PWM_WriteCompare1(m);
    PWM_WriteCompare2(m);

    if( m > up_band)
```

```
206         {
207             str_1_Write(10);
208         }
209 
210         if(( m <= up_band)&&( m >= low_band))
211         {
212             str_1_Write(11);
213         }
214 
215         if( m < low_band)
216         {
217             str_1_Write(01);
218         }
219 
220         i++;
221         if(i==700){i=0;}
222 
223         flag_Write(0);
224     }
225 
226     /*******************************************************************************
227     * Function Name: Isr_TC_Handler
228     ********************************************************************************
229     *
230     * Summary:
231     *  This function:
232     *  1. Sets up and enables the PWM interrupt.
233     *  2. Starts the PWM Component.
234     *
235     *******************************************************************************/
236     int main()
237     {
238 
239         str_Write(1);
240 
241         /* Start the PWM Component */
242         PWM_Start();
243         PWM_WritePeriod(1370);
244 
245         /* Enable the global interrupt */
246         CyGlobalIntEnable;
247 
248         /* Enable the Interrupt component connected to the PWM interrupt output */
249         Isr_TC_StartEx(Isr_TC_Handler);
250 
```

```
251         str_Write(0);
252         str_1_Write(11);
253
254         for(;;)
255         {
256         }
257
258     }
```

## C.7 Coding of dual-mode switching technique for proposed CT scheme based on complementary 20 kHz SPWM when SSR = 0.1

```
1         n=m-48;
2         PWM_1_WriteCompare1(m);
3         PWM_1_WriteCompare2(n);
```

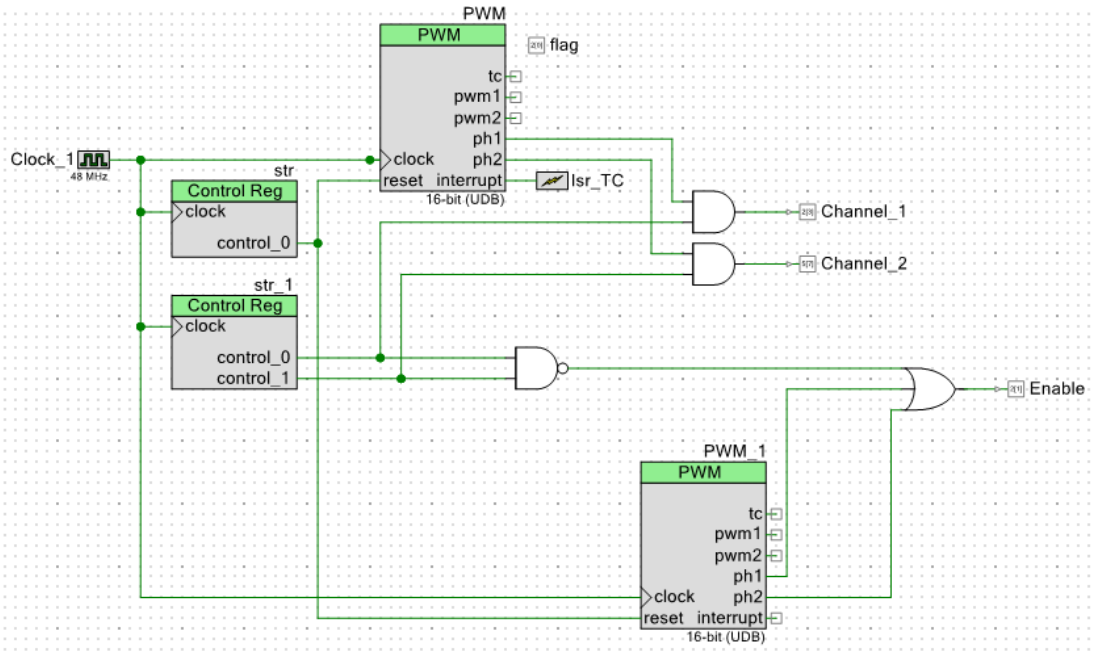


*Figure C.1 TopDesign in PSoC Creator with code of Section C.7.*