University of Strathclyde, Department of Electronic and Electrical Engineering

Enhanced Ultra Low Noise Design Techniques For Multiple Output Isolated DC-DC Converters.

By

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A thesis presented in fulfilment of the requirements for the degree of Master of Philosophy

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"All mathematical sciences are founded on relations between physical laws and laws of numbers, so that the aim of exact science, is to reduce the problems of nature to the determination of quantities by operations with numbers".

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Abstract

This thesis investigates an active gate control technique intended for a low power multiple output 3 Watt dc/dc converter for a space application and the resultant trade-off between conversion efficiency and output noise.

Controlling the slew-rate of the drain-source voltage of the primary MOSFET devices affects conduction, turn-on, and turn-off losses and this is assessed in the prototype converter. This reveals that as the slew-rate is reduced the turn-on and turn-off losses increase as the device takes longer to transit from the off-state to the saturated on-state and vice-versa. The purpose of assessing the switch losses are two-fold; firstly, in order to assess the compromise that is made between switching energy loss and output voltage noise (as decreasing the slew-rate also decreases the output voltage noise). Secondly, to evaluate how the transformer winding topology affects the device losses. Analysis of the MOSFET energy losses are compared with three different transformers: two use the same winding technique but have different permeabilites and the third uses a new winding technique which reduces the energy loss when used with an advanced MnZn ferrite push-pull transformer.

When compared with standard-wound transformers, the transformer using the new winding technique displays lower switching losses and this is attributed to the technique of winding individual primary layers interleaved with the secondary windings. This leads to lower leakage inductance and lower interwinding capacitance both of which reduce the turn-on and turn-off losses in the primary switching device. This results in improved overall system efficiency.

From the experimental data, the higher order harmonics from the 5th to the 10th are attenuated more as the time to slew is increased from 400ns to 900ns. Therefore, the voltage slew-rate limiting technique has an impact on the higher order harmonics but has no impact on the lower order harmonics. Control of the slew rate qualitatively allows for a reduction in conducted noise levels at the expense of increased switch loss. From a systems perspective it is more important to have lower energy switching losses.

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List of Symbols

Parameter	Symbol	Unit
Magnetic flux density	В	tesla, (T)
Magnetic field intensity	Н	Ampere m^{-1} , (Am^{-1})
Initial permeability	$\mu_i = \frac{B}{H}$	henry m^{-1} , (Hm^{-1})
Permeability relative	μ _r	henry m^{-1} , (Hm^{-1}) $\mu = \mu_0 \mu_r$
		$\mu - \mu_0 \mu_r$
Effective magnetic area of core	A _c	<i>m</i> ²
Mean magnetic path length	le	т
Magnetic flux	Φ	weber ,(Wb)
Magnetic potential	m.m.f	ampere
Inductance	L	henry, (H)
Inductance index	AL	nH turn ⁻²
Number of turns	N	
Mean length of turn	L _t	m
Current density	J	ampere m^{-2} , (Am^{-2})
Resistivity	ρ	$ohm - m, (\Omega - m)$
Energy	W	joule , (J)

Sourced from IEC magnetics standard 50(221

List of Abbreviations

Abbreviation	Definition
AC	Alternating current
CCD	Charge couple device
ССМ	Constant current mode
СМ	Current mode
CMOS	Complementary metal oxide semiconductor
BJT/ MOSFET	Bipolar junction transistor metal oxide semiconductor
dBm	Relative to a mW
DC	Direct current
DCM	Discontinuous current mode
EMC	Electro magnetic compatability
EMI	Electro magnetic interference
ESR	Equivelent series resistance
FPA	Focal plane assembly
Ga As MESFET	Gallium arsenide metal epitaxial field effect transistor
IM	Interconnect module
MMIC	Monolithic microwave integrated circuit
Mn-Zn	Manganese zinc ferrimagnetic material
MOSFET	Metal oxide field effect transistor
Np	Normal turns in the primary
Ns	Normal turns in the secondary
PEM	Proximity electronic module
PWM	Pulse width modulation
QSW	Quasi square wave
Rds	Resistance between the drain and source
THD	Total Harmonic Distortion
VHF	Very high Frequency
VLSI	Very large scale integration
ZVS	Zero voltage switching

Chapter One

1.1 Introduction

The research reported in this thesis investigates the impact of slew-rate limiting on the output noise and the efficiency of a multiple-output, push-pull switched-mode power supply. The power supply has been designed to power a CCD array operating in an observation satellite and the operational requirements of the CCD require an ultra-low noise source of power. Any noise present on the power supply is directly coupled into the CCD and significantly reduces the signal-tonoise ratio of the resulting data. Therefore, minimisation of noise is a major objective. Likewise, as the system operates in a power limited environment, any noise mitigating schemes must also reduce power consumption hence the additional focus of the work on the efficiency of the power supply.

The research considers suitable topologies that would produce ultra low noise power supplies but with high efficiency. This is achieved by analysis of the switching waveforms and analysing generated waveforms.

Table 1.1 identifies four different candidate low noise dc/dc converters that can be employed to power the CCD optical arrays. This data was extracted from recent literature on high-efficiency low-noise power supply techniques. When reviewing all of the features outlined in Table 1.1 and the relevant literature, it was found that voltage slew rate control lowers the conducted and radiated noise and that quoted efficiency figures were superior to the other three options. The voltage slew control IC controls the power MOS FET dv/dt by using an external 'Miller' capacitor that lowers input common mode noise by integrating capacitive feedback onto the output stage.

The break through in reducing the conducted harmonic emissions was verified in the experimental push-pull control circuit where conducted harmonic noise from dc to1GHz was reduced by a factor of 3. This reduction suggests that this is an improvement over a charge pump technique. Furthermore by implementing a trapezoidal primary voltage waveform it is possible to lower the magnitude of the high frequency switching harmonic spectra. Advanced ferrite core materials also have attenuation properties at the fundamental of the switching frequency. It is envisaged that by employing this technique there will be no necessity for external filters. However there will be a trade-off in the conversion efficiency when utilising slew rate limiting and this is investigated. This technique lends itself to distributed power systems where multiple dc outputs are required as defined in the EADS requirement specification [1] for the GAIA platform.

Features	H bridge drive	Resonant	Charge	Gate_drive_slew control		
	Patent	QSW ZVS	Pump	LT1683 Patent 5952817		
	5815381	Reference [Low	LT 3487&TI	And LT1738.		
	Ref [15] [low	power only] Ref	TPS 65030	Reference [18]		
	power only]	[10]	Reference [16]			
Voltage	Good from	Good from	Good from	Good from Vin +20Vdc to		
input	+21.6Vdc to	+18Vdc to +32Vdc	Vin range + 2.3Vdc	+32Vdc		
regulation	26.4Vdc		to+16Vdc			
Voltage		Both current and	Boost and inverting	yes		
step up		voltage are step up	only multiples of input			
			voltage			
Current		High_Q inductor	Only in discrete			
step up		and ferrite	fractions of input			
			current			
Primary		80% simulated	77%. Fixed switching	>80% (x2) & (x3) Fixed		
power	At 80% load	switching	frequency 2MHz.	switching frequency		
conversion	max for Vo of	frequency 150kHz	Current mode operation	37kHz.Peak current mode		
[n]	+3.3Vdc	to 500KHz		of PWM. Continuous		
		Current mode		conduction mode or		
		operation of PWM		discontinuous mode.		
Inductor	yes	yes	yes	yes		
required						
Output	Conducted	Compliance to	Conducted emissions	Conducted emissions		
noise and	emissions	ETSI 300/339	-33dBm	measured - 96dBm from		
ripple	- 63dBm			10kHz to 1GHz on x1,x2		
Voltage	Good for two	Good for one		Good for three		
output	decades 1%	decade only		decades 0.7%		
regulation	Fixed outputs					
Shutdown	high	high	8µA for dual outputs	Very low 24µA for five		
Quiescent				output voltages		
current						
L	1					

Table 1.1 Four recent topologies that were considered to supply DC power to the CCD arrays.

1.2 The structure of the thesis.

This thesis is presented in five chapters.

Chapter One Section 1.1 identifies how the slew rate limiting affects the noise output and losses in a push- pull topology. Section 1.3 identifies the key outcomes of this research. A literature review is provided in section 1.4 and section 1.5 explains the motivation for this research.

Chapter Two explores the function of the basic buck derived push pull topology. It evaluates the advantage and disadvantage of the slew rate limiting method when applied to a buck derived push pull topology. A description of the experimental linear ramping operation is provided along with a block diagram of the slew control device to show how the attenuation of the harmonics is achieved.

Fixed frequency current mode control operation for continuous mode and discontinuous mode is discussed. A timing diagram of the primary switching current, including the necessary dead time, is shown. This includes also the timing of the MOS FET drive signals. The distinct advantage of the voltage slew gate drive technique is explained.

Measurements of the (X2) four layer PCB voltage slew control method were made on three separate toroid transformers with different permeabilities for line and load regulation and efficiency. A summary of measurements is provided illustrating which transformer is most effective in terms of efficiency and power loss. Data is provided in appendix D.

Chapter Three investigates the impact of voltage slew rate limiting on the switching device losses for a buck derived push pull circuit. The conduction losses, turn on and turn off losses, are measured for one of the push-pull MOS FET devices. The resultant energy losses in (nJ) for all three toroid transformers are quantified and presented, versus the slew time. The summary identifies the lowest measured losses from the three transformers.

Chapter Four determines the impact of voltage slew rate limiting on the output noise for a buck derived push pull circuit. An experimental method for all three toroid transformers is described using a spectrum analyser that measures the 1st to the 10th harmonic of the secondary switching frequency, versus the slew rate setting from 400ns to 900ns. The attenuation results of the conducted noise are presented. This is in order to determine which transformer provides the lowest noise output. Total harmonic distortion is also investigated. The summary compares harmonic attenuation versus slew rate setting. Finally, spectrum analysis provides information on broad band harmonic attenuation with the measurements made from 0 Hz to 1 GHz. This detailed data is provided in appendix B.

Chapter Five summarises the work and its contributions, and proposes further research directions.

1.3 The key outcomes of this research

The key outcome of chapter three is that the measured results of varying the voltage slew rate clearly demonstrates that, when the voltage slew rate is adjusted to 400ns, the conduction losses are at a minimum. In addition, at this slew rate the turn on and turn off losses are also minimized. So, as the slew rate is decreased (that is, it takes longer to slew from on-off and vice-versa), the turn-on and turn-off losses increase. In addition, the results presented in Chapter 3 identify which transformer core yields the lowest switching device losses.

The key outcomes of Chapter Four are found from comparisons of the high frequency spectra with different slew-rate settings. It is found that the higher order harmonics from the 6th to the 10th can be attenuated as the slew rate is decreased. This correlates with the expected frequency of the 2nd breakpoint in the frequency spectrum that the trapezoidal switching waveform generates. Therefore, this particular voltage slew-rate limiting system has an impact on the higher order harmonics. It is also verified that slew-rate limiting has little impact on the magnitude of the 1st to the 5th harmonics in the chosen system.

1.4 Literature Review

Background research into a suitable switching waveform and low power consumption

This literature review considers the system arrangement and the compliance for low power consumption, including very low noise, on the output of each DC bias voltage.

At the outputs of the seventeen isolated dc/dc converters, plus the interconnecting flat copper Kapton/Mylar type cable in paper [1]. These two factors can lead to a higher level of magnitude of conducted emissions.

Before testing commences, a detailed test plan, including the EMC assessment reports, must be submitted to the recognised EMC compliance laboratory for approval. Failure in any one step of the test plan can mean repeating the whole suite of measurements. This is excessively expensive to electronic engineering companies in time and money. Consider also that, the higher the desired efficiency, using conventional fast switching techniques can lead to EMC and EMI failure. To overcome this EMC and EMI risk scenario, the literature review was started on the principal understanding that fast transitions in turn on and turn off times in most primary current waveforms can cause a higher magnitude of frequency harmonics, with the accompanying output voltage ripple and noise [2].

From history and usage, the trend of most failures in EMC testing of dc/dc converters is in conducted ripple and noise. This allowed an overview of what was feasible in switching efficiency, power dissipation and the ability of the proposed dc/dc converter to operate and maintain isolated, multiple output dc voltages with a high degree of stability for a hazardous space environment application [4].

The research goal was to better the primary requirement specification [1]. The reason for this is that multiple parallel dc/dc converters can emit higher order emissions if using conventional pulse width modulation waveform methods [5].

The literature search was split into four categories of interest and evidence of simulated and practical results.

The first category relates to DC-DC converters that operate in a space hostile radiation environment [1] to [4].

The second category are related to reducing the conducted emissions from ripple and noise [5],[6],[7],[8].

The third category investigates control techniques that can produce low current bias voltages to the CCD optical detector array efficiently. Power saving techniques at low power can be performed by the use of pulse frequency modulation (PFM). In the operation with PFM, pulses of current are transferred to the load via a second order filter. Voltage regulation is obtained by varying the time delay between pulses, hence the power circuit will be operating in the discontinuous mode. [5], [9] and [20]. Also included in this part of the review was the need to minimise power dissipation and find methods that would improve the conversion efficiency. If implementing (PFM) the control circuit does not require the feedback amplifier as used in (PWM) control circuits. Instead the use of a system that compares the output voltage to a reference which initiates current pulses when the output voltage is low. One major drawback to these aforementioned controllers is that they inherently produce large conducted and radiated harmonic emissions at light loads.

The fourth category considers the transformer ferrite material that will reduce the core power dissipation when applying the Dowell and modified Steinmetz equations [21], [22].

A novel, buck control system in extending the battery life cycle is discussed [10], using a soft switching dc-dc converter at light loads in the order of less than 100mA. This type of circuit employs a load-dependent, hopping or skip mode strategy to provide nominal conversion efficiencies from 72% to 77% at 100mA. In order to maintain this range of efficiency, the circuit replaces the error amplifier with a hysteric Schmitt comparator. This, in turn, is fed to the control circuit that provides the dead time and has an in-built gate driver circuit. There are trade-offs between conduction and switching losses to maintain reasonable efficiency. During light loads, the converter hops from CCM to synchronous

DCM. The topology is confirmed as quasi-square-wave ZVS resonant and has only one resonant capacitor. However the efficiency characteristics roll off at \leq 70mA to 71%. The power dissipation is < 55mW for a load current of 100mA when using one single output. For the requirement of this study it equates to 275mW. This figure is comparatively low. Nevertheless the harmonics of ripple and noise from this type of converter would present a problem at light loads. A second order filter would have to be implemented. A study would also have to be made on the suitability of galvanic isolation between the primary and secondary windings.

The next step was to review the properties of different technologies and switching characteristics of BJT/MOSFET and MESFET/HMT structures. GaAs MESFETS are applied in the design of RF amplifiers. The feasibility of using these devices in VHF DC-DC converters was reported in [11]. Employing high frequency assembly techniques provided high target conversion efficiency yielded a theoretical 80% for a 3W load. There is an advantage in using GaAs MESFET when switching at 50MHz. The inherent disadvantage is that the breakdown voltage is smaller in comparison to a MOSFET. Thin-film, hybrid techniques on a very small MMIC package appears attractive but expensive. However, for space application, there are many space qualified MMIC packages that vary in packaging size. The author of this paper makes the assumption that ferrite inductors, instead of air cores, contribute to minimising the magnitude of EMI emissions, without demonstrating empirical and simulated results. A further disadvantage is that thin-film, hybrid techniques at VHF frequencies must reduce the chance of parasitic oscillations taking place. Moreover, the power losses associated with HF magnetic properties do not increase and skin effect related losses have to be analysed in this part of the frequency domain.

Thales in Belgium and EADS (Matra Marconi Space) in England have, over recent years, been involved with the design implementation of space craft DC/DC converters. When including low power dissipation, the preferred topology has been push pull because the target measured efficiency is reported as 95% at higher power output loads. With synchronous rectification, the calculated losses of the

push-pull transformer, centre tapped, core and copper losses, are explained in detail in [12].

For a higher power output, assuming the author is using a trapezoidal waveform to switch the primary current, the core losses are less when switching at a nominal switching frequency of 100kHz at a flux density of 200mT. The author explains that he only used one type of ferrite material (PC45) that has the lowest losses $<300 \text{ Pcv}(kW/m^3)$ between the range of $+60 \ ^{\circ}C$ to $+80 \ ^{\circ}C$. Since this paper was written, TDK have brought out an advanced manganese zinc, low loss, high saturation, magnetic flux density ferrite for power transformers which maintains a flat profile core loss of 380 Pcv(kW/m³) from $-40 \ ^{\circ}C$ to $+140 \ ^{\circ}C$.

The paper [13] examines, by emulation of half turns, where the fundamental frequency of the voltage ripple equals that of the switching frequency. The turns ratio between the primary and each secondary can be improved and adjusted when fractions of turns can be incorporated into the windings. The benefit of half turns will probably result in a smaller number of primary and secondary turns hence reduced DC and AC losses. The drawback of this method is that the real fractional turns introduce a significant amount of leakage inductance which would have an effect on the cross regulation performance of the dc output voltages.

This is important as there are two revisions of toroid transformer that have different leakage inductance values and different inter-winding capacitance values. In this application the turns ratio needs to be very precise, otherwise a low secondary *Vout* or a high *Vout* occurs. A high *Vout* means a significant additional power loss in the low drop out linear regulators.

Through experimentation, detailed in [13], the control loop is designed to have a fast dynamic response; i.e. high loop gain at high frequency; then it may adjust the duty cycle during every single period of the ripple waveform. The result would be a smaller pulse width for the switch that conducts when the larger winding section is on. This leads to a control problem effectively producing unequal times between the two active intervals of the switching cycle. The author explains two solutions to this problem; by decreasing the gain of the error amplifier at the switching frequency (i.e. adjusting the control loop response to be slower); or by

reducing the ESR of the output capacitor because emulated fractional turns tend to cause higher output ripple. The passive output filter components need to be adjusted to reduce the magnitude of ripple.

In [14] the author analyses the proximity effect factors when used in a push-pull circuit. The proximity effect is understood to be that every winding has an associated field and when this couples on nearby windings, the charge distribution changes and eddy currents are created.

To solve this problem the solution is to design the point of minimum ac winding resistance of multilayered windings for general waveforms used in switch mode power supplies. The optimum winding layer thickness can be determined by knowing the number of layers and the number of harmonics related to the rise time, including the duty cycle. By selecting copper foil the a.c. resistance was much reduced in comparison to a single layer of copper wire. It is believed that in the low power and low switching frequency operation, the proximity effect factors will not present problems in this application.

A technique used to attenuate radiated EMI and improve supply transient immunity and load transient immunity with over voltage protection [15], outlines isolated DC/DC converters in the range of 3 to 10 watt. These are capable of producing 3 W using a standard high density 24 pin JEDEC package with provision for external synchronisation. The PWM topology is a push pull drive which operates at double the switching frequency. By definition this means that each half cycle has the energy transferred across the transformer leaving very little residual DC flux. As a result, the maximum flux density is not controlled by the B and H saturation characteristic but only the maximum acceptable core loss. With a very small ferrite toroidal transformer core, the volume to surface area is minimised. Consider also that the actual power loss is determined by the volume of the ferrite and the flux in the core. By minimising the volume for a given flux, the power loss is minimised. Volume is proportional to R^3 . Surface area is proportional to R^2 . Power loss is proportional to the volume of a given flux density. The limitations of this design are in the single, regulated output, rather than a multiple output and the fact that it uses a monostable on the secondary side

that could be prone to latch up in the event of radiation between 25krads(Si) and 125krads(Si).

Current mode charge pumps with less than 1mV ripple on the +3.3Vdc output voltage were reported in [16]. This equates to -47dBm. They claim that most of the voltage output ripple in such charge pumps is caused by recharging of the fraction of the flying capacitors. This charge loss and ripple can be decreased in feed forward or feedback compensation structures. While their feedback compensation structure promises much better results, it should be noted that all results presented in this paper are simulated.

A progressive method of reducing conductive harmonic ripple and noise is outlined in [17]. An advanced current mirror driver circuit for a 2MHz switching non-isolated step-down buck dc/dc converter is used. This control circuit provides a pulse width modulator to regulate the output dc voltage. The current mirror driver method is used to keep the current transition low during switching and dampen the switching noise. The control circuit reduces EMI and high frequency noise using a biphase output from the PWM control device that drives two current mirror drivers into a complementary set of N channel and P channel MOSFETS. The output ripple and noise is effectively reduced by the use of only one second order filter at the output. This produces results of the current mirror driver that have even lower $\frac{di}{dt}$ during turn on and turn off than the previous two drivers. The spectra of high frequency harmonic ripple and noise at 200MHz was -70dBm; at 400MHz -90dBm; at 600MHz -100dBm, then flat at this figure to 1GHz. The input voltage was four volts indicating that this converter was intended for battery operation, with a single output voltage of 2Vdc fed into a 200mA load. The switching frequency varied from 500 kHz to 2MHz, thus producing the higher spectra of noise and ripple below 200MHz. This noise level averaged -85dBm at 100MHz. The control circuit employs a linear current source that has a gate delay line for each gate. The current source N channel MOSFETS are controlled digitally. The authors conclude from their results that the current mirror driver achieves a linear current transition during switching without the necessity of extra inductive or capacitive passive components.

The patent [18] is exclusive by the nature of its control circuit. It provides a method for driving an inductive and capacitive load using an active gate drive with dual feedback loops that perform the current and voltage slew. This produces a mechanism for all multiple secondary dc output voltages to be isolated from the primary, using a push-pull topology. It also satisfies the load requirements of the optical arrays using Charge Coupled Devices. The main reason for this is that the conducted harmonic ripple and noise measurements taken from the first experimental model, when compared with reference [18], illustrated that the lower and upper harmonics of ripple and noise from dc to 1GHz were considerably better. In addition, it would allow for an innovative way of winding a multiple-output, low-loss toroid transformer to reduce dynamic cross regulation by lowering the leakage inductance and interwinding capacitance. Poor performance on cross regulation can occur when secondary windings of high dc voltage are mixed with low secondary dc voltages.

A programmable voltage slew rate limiting and a current slew rate method for a buck switching regulator is reported [19]. The slew rate limiting circuits can be used in buck push-pull switching regulators that provide either current programmed or duty cycle control to a maximum of 50%. The main features of this type of buck regulator is that it has high efficiency with resulting ultra low noise output < $100 \mu V_{p-p}$, because of the slew rate limiting effects used. It also has a low shutdown current of $12 \mu A$. The limitations are that when it is used in an isolated converter configuration, all secondaries would have to employ low drop out voltage linear regulators.

This switching capacitor topology provides a method to reduce peak to peak ripple and noise at the output of the switching module and also ensures that the input supply current does not vary. This is brought about when two switching circuits, with the correct phase difference, are then combined and fed to the linear regulator. This supplies a steady current to the linear regulator and output ripple and noise is further reduced by bringing in synthesized ripple and noise in an opposite phase through the linear regulator. A delay control is used between control generator 1 and control generator 2. The operation of a CMOS hybrid VLSI circuit, using a fixed switching frequency that can regulate two output voltages with a switching efficiency minimum of 89% to a maximum of 95% for conditions of light load is described [20]. The output in this experimental case was 45mA. It also has the option of controlling the delay by implementing an external, second order, low-pass filter. The principle control loop uses PWM and implements a phase lock loop charge pump and dual output hybrid delay line / counter PWM technique. To prove the stability of the system, the author plots the Nyquist plot of the linear transfer function that shows the response is slow but not unstable.

When the converter is switched at 500 kHz with 256 discrete levels of duty cycle resolution, the converter consumes less than 45μ A. The circuit operates a PWM signal from digital inputs that are in line with small, low power voltage converters that have a low power dissipation of 100µW. The trade off is in the conducted emissions ripple which is quoted as 42mV P-P. The author makes no reference in the ripple measurement as to whether he used the full bandwidth of the oscilloscope when taking this measurement. So it becomes difficult to quantify and compare this figure with other authors' work. By implementing an external low pass filter with an attenuation factor of 100, this would reduce it to 420µVP-P.

In [21], the experimental and verification of losses in Ferrimagnetic material is assessed. The authors explain the experiment with a 3C85 ferrite core. Using a constant triangular re-magnetisation cycle the measured core losses are compared to different calculations. The triangular re-magnetisation cycle has a varying delay time. The flux density B is 200mT; the frequency is 20kHz and temperature 100° C. By the use of the Modified Steinmetz equation, the author explains that, by experimental verification, it is possible to obtain accurate results which indicate that by increasing the duty cycle beyond 0.75 the power losses increase in mW, when measured with this type of material. This empirical approach is significant in that it allows the calculation of the losses in the time domain for arbitrary waveforms of flux while implementing the available set of parameters of the classical Steinmetz equation.

The benefits of implementing Nanocrystalline (FeSiBCUnB) alloys in two toroid transformer experiments are outlined in [22]. Nanocrystalline alloys are linked to amorphous soft magnetic material toroids that are used in mag-amp regulators and push-pull topologies. Noise emanating from the output of the full wave rectifying diodes is reduced. The reason for this is because the saturable reactors (Mag-Amp) are connected in series with these rectifying diodes. The main benefits are in: (i) reducing the size of the toroids because of their high saturation magnetisation usually (\approx 1.2 to 1.3 Tesla) and: (ii) high frequency performance up to 1MHz with low losses and high permeability. It was also noted that the properties of this material exhibit high Curie temperatures (600°C). This would make it preferable for embedded applications because of the high temperature stability characteristic of up to 200°C. The author uses the Dowell method for calculating the resistance and leakage current. The calculation can also use Litz wire, including proximity and skin effects.

The authors of paper [23] measure the magnitude of impedance versus frequency and the phase angle versus frequency for four Mn-Zn toroid cores that have the same radius. The difference is that each have different height profiles. An advantage in using Mn-Zn material is that the toroid has permeabilities (μ) greater than 2000. For this type of ferrite material the magnetic flux characteristic is confined to the core which provides one advantage in limiting EMI. In addition to the reduction in EMI the authors explain that the purpose of the winding technique is to reduce the influence of stray capacitance between turns at high frequency. The magnetic field in the core is calculated including the electric field in the core. Relative and complex permeability values versus frequency is graphically shown and explained. Measured results were furnished by the use of an HP 4194A impedance analyser.

Charge coupled devices have inherent clock feed through noise [25], which would have led to failure of Electro Magnetic Capability and Electro Magnetic Interference compliance tests when using conventional switching techniques for the dc/dc converter.

1.5 Motivation for the research-the ESA Gaia IM module documentation.

The ESA Gaia imaging system mission is to create a precise three-dimensional map of around one billion stars throughout our galaxy and beyond. In the process it will map their motions which encode the origin and subsequent evolution of the galaxy. Through comprehensive photometric classification, it will provide the detailed physical properties of each star observed: characterizing their luminosity, temperature, gravity, and elemental composition. This massive stellar census will provide the basic observational data needed to tackle an enormous range of important problems related to the origin, structure, and evolutionary history of our galaxy. At the heart of the imaging system is an array of CCDs. The power supply for each CCD is based on dc/dc converters located in both the Interconnection modules IM1 and IM2. See fig 1.1

This thesis presents research on voltage slew rate limiting and its effects on output noise and energy losses. There is a need to define more precisely the energy loss characteristics when slew rate limiting is used in an experimental buck derived push pull circuit.

Since the satellite power supply system provides seventeen identical dc/dc converters it also is important to investigate comparisons of all known generated switching waveforms and understand which waveform offers a lower conducted harmonic content and optimizes efficiency. This necessitates the identification and listing of all known harmonic noise generation sources within the power system. On completion of this study it is then possible to determine the most suitable push pull transformer for low power dissipation with high conversion efficiency.

A charge coupled device image sensor has the capability of converting light photons into discrete packets of electron charge, limited by the image area format used in individual pixels, then transferring the signal charge by sequential clocking an array of gates to the video output signals. The data transfer is on two corresponding clock signals. The dc bias voltages for the CCD PEM cells are Vccd + 35Vdc, Vckd1 + 15Vdc, and Vckd 2 -6Vdc. The *Vvideo* bias voltage is +6.5Vdc and the *Vdd* bias voltage is +3.3Vdc. The power consumption table for one PEM cell is shown in table 1.2.

The original challenge of research into ultra low noise and low power dissipation began in July and August of 2006 in Belgium for a combination of high and low dc output voltages. This was from the original EADS-Astrium IM module requirement specification [1] that is linked to the ESA Gaia satellite optical focal plane platform. In addition to this requirement is the Gaia EMC & EMI specification [2].

1.6 The Gaia imaging system configuration

The Front-End Electronics is made of two different parts: the CCD proximity electronics (called PEM for Proximity Electronics Module) and the Interconnection Module (IM) which performs the interfaces between one PEM/CCD row and the processing chains. One PEM cell is dedicated to one CCD optical detector array. There are a total of seventeen PEM cells requiring seventeen isolated dc/dc converters. Each dc/dc converter output consists of five separate isolated DC bias voltages.

From a mechanical point of view, the CCDs are mounted on a support structure, controlled at a cryogenic temperature [3]. The PEM are mounted on a dedicated PEM support structure, and the IM are mounted above the PEM, contained on the support structure Fig 1.1. The IM can see directly into deep space through a radiator plate. A minor part of the power dissipated by the PEM is conducted through the IM, and the rest is dissipated through to a radiator located on the PEM support structure sides.

When IM1 and IM2 are connected together, this represents the interconnection of 17 isolated dc/dc converters to each PEM cell optical array. Fourteen of these dc/dc converters are contained in IM-1. The other three dc/dc converters are in IM-2.

The load is the CCD optical arrays [PEM] Cells which are a constant current load as illustrated in Table 1.2 Each PEM cell has five regulated DC output voltages which are fundamental to the system design.

Power	Vdc	min[mA]	Po[mW]	nom[mA]	Po[mW]	Max[mA]	Po[mW]
Vccd	+35	2	70	5	175	10	350
Vckd1	+15	30	450	50	750	80	1200
Vckd2	-6	5	30	15	90	20	120
Video	+6.5	30	195	55	357	100	650
Vdd	+3.3	50	165	100	333	150	495
$\Sigma Pout$			min 910		nom1705		max 2815

Table 1.2: One PEM cell power supply DC output characteristics.



Fig 1.1 The IM module is part of the optical focal plane platform assembly. The three dimensional colour images are reproduced by kind permission of EADS-Astrium, Toulouse, France.

The five isolated dc bias voltages are applied to each CCD optical detector array (Pem cell). The length of cable is approximately 30cm interconnecting from the output of the individual dc/dc converters contained in the IM modules to the PEM cell loads. This transmission line interconnect is illustrated in figure 1.2.



Figure. 1.2 The source destination of one PEM Cell, identifying the transmission line interconnect wiring with the load capacitance values in μ F for the five CCD dc bias voltages.



Figure 1.3 Showing four of the PEM cells CCD detector arrays in their mechanical handling Jigs. Courtesy of e2v technologies [UK] Ltd.

The three dimensional colour images above are four of the Gaia CCD in their mechanical handling jigs. For dimensional purposes it is possible to gain a size perspective against the two Euro coin shown between the D connectors. The physical size of the individual CCD array is 45mm by 60mm. This provides an aspect ratio of 1.33 for the optical line of sight. They are amongst the largest CCDs ever manufactured for a space environment in the United Kingdom.

1.7 Summary

This chapter has introduced the key areas of research investigated in the thesis which include:

- (i) The assessment of the effects of voltage slew rate limiting on output harmonics and noise with two advanced Mn-Zn transformer materials when applied in a experimental buck derived push pull circuit.
- (ii) The measurement of converter efficiency and losses.
- (iii) The assessment of the effects of voltage slew rate limiting on the attenuation of the high frequency switching harmonic spectra. It is envisaged that by employing this technique there will be no necessity for external filters. However, there will be a trade-off in the conversion efficiency which will be investigated.
- (iv) The design of a push-pull converter with multiple dc outputs that meets the EADS requirement specification [1].

The structure of the thesis is introduced and the motivation for the work presented. The literature review considers recently published research papers and other publications which demonstrate low noise control techniques that have high converter system efficiency intended for a space environment. Low power consumption converters are also investigated along with the magnetic properties of Mn-Zn ferrite cores. After reviewing all these research papers it was found that voltage slew rate limiting offered the best technique for reducing the magnitude of common mode harmonic noise.

The motivation for this work is to prove that a switching control circuit using a pulse width modulated hard-switched converter, in conjunction with a voltage slew rate limiting circuit, that could produce ultra low noise power supplies to power space qualified CCD arrays.
1.8 References.

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Chapter Two

Basic buck derived push pull topology

2.1 Introduction

This chapter describes the buck-derived push-pull circuit which is used in this research, and the transformers used to compare performance. The chapter also reviews the means of adjusting the slew rate of the primary voltage waveform with a view to investigating the impact it has on output noise and ripple, and primary MOSFET switching loss. The circuit is operated as an experimental regulated DC-DC converter with a dc source voltage of +28Vdc, providing five multiple outputs, in the continuous mode of operation. The converter provides five regulated dc outputs with a total output power of 3 W.

The push-pull circuit is shown in figure 2.1. The output voltage is determined by the turns ratio between the primary and secondary windings of the split-wound transformer and the duty ratio of the MOSFET devices. The rectified voltage is then filtered by two second-order LC filters which attenuate switching frequency harmonics. The output voltage (+3.3Vdc) is maintained by a closed-loop feedback system where the voltage feedback signal is coupled into the control circuit via an opto-isolator. The internal transconductance error amplifier contained with the control IC then sets the duty cycle δ accordingly. The value of δ will be adjusted to maintain the output voltage at the desired value regardless of the voltage at the other outputs and the input voltage.

Multiple outputs are simple to provide when using transformers. The design of the DC-DC converter will use surface mount components to improve density and transformer optimisation is required to provide the different bias dc voltages required for the IM modules. Reducing the weight of the push pull transformer becomes an important goal for space qualification.



Figure 2.1. Block diagram of the basic buck derived isolated push- pull topology.

The push pull circuit has the advantage of a centre tapped primary transformer and utilises only two MOSFET switches. FET2 applies a positive voltage across the primary and during the on state of FET2 the core flux increases. FET1 decreases the flux. The two switches must be controlled to ensure that there is no net DC flux build up in the transformer during each switching cycle. The transformer must also have sufficient inductance and cross sectional area as not to enter a saturated state.

When FET 2 is on the diode D1 conducts and D2 is in the off state. The diode states are reversed when FET1 is on. When both controllable MOSFET switches are off the diodes are on and share equally the filter inductor current. The dc voltage transfer function of the push-pull converter is :

$$=\frac{V_{out}}{V_{in}}$$
(2.0)

$$= 2 \frac{N2}{N1} \left[\frac{t}{T} \right]$$
(2.1)

The slew control reduces higher frequency components of the ripple current in the output capacitor. The capacitor ESR and the magnitude of the output ripple current controls the fundamental component. Therefore

$$Cout = \frac{1}{\frac{\Delta Vout}{\Delta I_L (\text{max})} - ESR} * \frac{\delta (\text{min})}{f}$$
(2.2)

This equation is referenced to page 20 of the Linear Technology data sheet for the LT1683 peak current PWM control device.

2.2 Slew-rate control of the primary MOSFET voltage and its impact on the output spectrum

A trapezoidal waveform with slewed edges is shown in Figure 2.2 along with the envelope of generated harmonics. The envelope rolls off at 20dB/decade from the nominal switching frequency with a second break point occurring at $1/(\pi.tslew)$ where *tslew* is the transition time of the slewed edge. This second break point is significant and can be adjusted using the rise and fall time of the primary voltage waveform. The purpose of this research is to investigate how the adjustment of slew-rate affects the device losses and the output voltage noise and ripple.





The fundamental switching frequency of the prototype converter is 75.636 kHz. The slew rate control system has been designed such that the slew-rate can be varied from 400ns to 900ns. The break point between the 20dB/decade and 40dB/decade slopes can then be moved from 796 kHz (at 400ns) to 353 kHz (at 900ns). Therefore it is expected that switching harmonics from the 5th harmonic can be affected by adjustment of the slew-rate setting and harmonics below this value will be unaffected by changes in the slew-rate setting.

2.3 The LT1683 CMOS Push Pull DC-DC Controller

The control of the MOSFET voltage and current slew rates are achieved via two feedback loops that are provided on the Linear Technology LT1683 device, as shown in figure 2.3. One loop controls the n channel MOSFET drain dv/dt and the other loop controls the n channel MOSFET di/dt. Feedback for the voltage slew rate control uses an external capacitor between Cap A or Cap B pins and the respective n channel MOSFET drain. These integrating capacitors close the voltage feedback loop. The external *Rvsl* potentiometer to ground is selected at nominal 20k Ω , which sets the voltage slew rate for the drains of FET1 and FET2. The time to slew between the on and off states on the MOSFET drain voltage will determine how harmonics are reduced from this source The voltage slew rate is thus inversely proportional to both the value of capacitor and *Rvsl*, and the input voltage of +28Vdc. The complete circuit diagram is included in the Appendix A.1.1 page 88.

The current slew feedback loop consists of the voltage across the external sense resistor, which is internally amplified and differentiated. The derivative is limited to a value set by a variable trim potentiometer *Rcsl*. In this circuit the current slew-rate control is fixed.



Figure 2.3. Block diagram of the voltage and current slew rate control loops on the Linear LT 1683 device. Courtesy of Linear Technology.

For the current sense resistor the peak current was chosen to be 386mA. The current sense resistor is then

$$\frac{R}{sense} = \frac{0.1}{0.386} = 260m\Omega$$
(2.3)

Two control loops are combined internally so that a smooth transition from current slew control to voltage slew control results. The sequence of this is when turning on; the driver current will slew before the voltage. When turning off, the voltage will slew before the current. For operational conditions it is desirable to have similar values for *Rvsl* and *Rcsl*. By decreasing the slew rate of the primary voltage waveform a reduction in the magnitude of harmonic noise can be effected but is traded with a slight decrease in the conversion efficiency of the dc/dc converter. The harmonics can be reduced by means of regulating the slew rates of both voltage and current in the switching control device integrated circuit. This

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result decreases the necessity to have higher order common mode and differential mode cascaded power filter circuit elements in the input filter.

When the power MOSFET switch turns off the opposite sequence occurs. Care must be taken to ensure that each MOSFET conducts for exactly equal voltsecond period or a dc component will be applied to the to the transformer primary, which will cause the transformer to saturate. Unequal MOSFET switching and unequal MOSFET gate drive voltages can also cause the transformer to saturate. The peak current mode topology used solves this problem by monitoring the current in each of the push-pull MOSFETs on a pulse by pulse basis and forces alternate current pulses to have equal amplitude. By implementing slope compensation, as in the case with this PWM controller, stability for high duty cycles (δ) is guaranteed. The maximum duty ratio for the controlled device is 0.45.

The voltage that appears across the input of the first second order LC filter has a peak value equal to the input voltage multiplied by the turns ratio between the primary and the secondary. This voltage is applied until the MOSFET is turned off by the fixed frequency current mode PWM controller. Next there must be a mandatory "dead time" when neither FET is conducting. This is because it takes a finite time for the MOSFETS to stop conducting current. In the prototype dc-dc converter, multiple outputs are provided by using multiple secondary windings. Each secondary winding is isolated with a regulated output.

2.4 The advantage of voltage slew methods

The report [1] identified a low noise topology utilising a variable voltage and slew gate drive control topology originated by Brewster and Nelson of Linear Technology. A comprehensive route for investigating the development of a multiple output CCD dc bias supplies is provided in [18].

The principal reason for attenuating the harmonics over the extended bandwidth is that any switching harmonic noise can be detected by the CCD optical detector arrays. This would result in impaired optical pixel resolution and appears as white noise on the display. The converter efficiency is a trade-off with the slew rate. Other factors that affect this efficiency optimisation are:

- High frequency ferrite core losses and proximity effects between multiple windings in the transformer.
- Transformer I^2r copper losses in all of the windings.
- Transformer leakage inductance.
- Transformer distributed winding capacitance between the primary and secondary.
- Transformer turns ratio error due to insufficient coupling between the windings.
- MOSFET switching losses composed of conduction, turn-on and turn- off losses.
- Balancing a low $R_{ds,on}$ with the gate charge of the MOSFET.
- Rectifying Schottky diode losses composed of forward voltage drop and reverse leakage current and also affects of high junction capacitance.
- Rectifier diode ultra fast recovery rectifier diode reverse capacitance losses.
- The output inductor dc resistance.

2.5 Experimental set-up for assessment of the DC-DC converter.

The purpose of the test rig system is threefold:

- To measure both input and output power of the DC-DC converter. This will characterise the efficiency of the converter with three different transformer rectifier boards. Relevant data can be found in appendix D.
- (ii) The MOSFET energy losses and power losses due to variations of the slew rate. Both (i) and (ii) are discussed in chapter three with the measured results.
- (iii) Measurement of the output noise spectrum when the slew rate is varied. This is discussed in chapter 4. The experimental set-up for the voltage slew control and output ripple noise experiments is shown in figure 2.4, for full and minimum resistive load as reference in table 4.2, page 73.



Figure 2.4 Apparatus used to detect switching energy losses and low conducted noise from the output of the low power DC-DC converter.

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2.6 Description of the multiple output transformer for all three transformers.

The push pull topology is selected because the push pull transformer does not store any energy and the output current is drawn only when either of the power MOS FET are conducting. The selection of the core material is based on low loss with high saturation flux density. The flux excursion has a variation from +B to -B, which is chosen to allow maximum usage of the MnZn transformer core. The chosen material has a stable and high permeability through the space environment temperature range. MnZn ferrite cores have the high permeabilities that are desirable in this case and they can be used at low frequencies below 5MHz. Toroid transformers have lower height profiles when compared with the conventional RM Pot cores. This becomes important, as in this case, when multilayered windings are required as this can raise the height profile.

Two different types of ferrite permeability were used (i) in order to gain an understanding of which transformer offered the highest attenuation to the ripple noise level, and (ii) which offered the best overall conversion efficiency. Three toroid high frequency transformers were constructed: Aerostanrew(mod1), Etal-A and Etal-B.

Both the Aerostanrew (mod 1) transformer and the Etal-A transformer used core materials with an initial permeability of 3000. The Etal-B transformer has an initial permeability of 2500. Construction techniques differed between the Aerostanrew transformer and both Etal transformers in order to understand what impact this has on the performance of each individual transformer. Due to the high permeability it was thought that this would increase the conversion efficiency over the lower permeability core material, and improve the output noise and ripple magnitude. All three transformers had identical primary and secondary turns, according to the power requirements listed in chapter 1. Details of the core geometry are listed in table 2.1.

Table 2.1. Core geometry of the three transformers: Aerostanrew (Mod1), Etal-A and Etal-B. (Data extracted from Magnetics Butler, PA).

Toroid Ferrite Core Data	Aerostanrew (mod 1)	Etal-B
Parameters	Etal -A	
	Quoted manufacturer values	Magnetics
	Magnetics F grade	Pgrade
Outside dimension	15.9 mm	16.26 mm
Inside dimension	8.89 mm	8.50 mm
Height	4.7 mm	4.83 mm
Le (path length)	36.8 mm	36.8mm
Ae	0.153cmsq	0.153cmsq
Ui Initial permeability	3000	2500
Weight	2.8gms	2.8gms
Toroid type	ZF41605-TC	ZP 41605- TC
Note the P grade has the		
lowest core losses between		
-30°C to +90°C		

Winding details

The originality of the multiple output toroid transformer design is in the interleaving of bifilar windings introduced to the primary and five, isolated, secondary windings. Two of the secondary windings on the Aerostanrew (mod1) transformer use the Skeining method on windings 2 and windings 4. Winding 2 is associated with +35Vdc rail and winding 4 is associated with the +6.5Vdc winding. Bifilar windings guarantee that the turns will be identical which is important in providing an accurate turns ratio for the linear drop out regulators. Consider if the turns ratio is incorrect a high secondary dc voltage means a power loss in the low drop out regulators. Bifilar windings will also reduce the I^2R copper losses in all windings.

The secondary windings are evenly spaced in the same winding volume as opposed to discrete secondary windings wound on top of each other. This winding technique was chosen to reduce the leakage inductance and interwinding capacitance. It is expected that this winding technique will be an improvement on the coupling achieved on the Etal-A and Etal- B transformers. A comparison of the toroid high frequency Aerostanrew(mod1) transformer and the two Etal transformer constructions is detailed in this section. This includes measured primary inductance of all five secondary windings. The measured wire resistance in contained separately in the magnetic design in appendix c. Shown in table 2.2 is the number of turns for both primary and secondary windings with the corresponding calculated output voltage.

Table 2.2 Winding details for all three toroid high frequency transformers Aerostanrew (mod1), Etal-A and Etal-B.

(Vin x Ns/Np)	Np	Ns	turns ratio (Ns/Np)	Isolated wdgs	V(out) rms dc
nominal 28V	27	37	1.37	1	38.37
	Split primary wdgs	18	0.66	2	18.66
		8	0.30	3	8.3
		7	0.26	4	7.26
		4	0.148	5	4.1
Vin min 26V	27	37	1.37	1	35.63
		18	0.66	2	17.3
		8	0.30	3	7.8
		7	0.26	4	6.76
		4	0.148	5	3.85

Line and load regulation measurements were conducted on the regulated +3.3Vdc and the other four non-regulated voltage rails to determine that the experimental DC- DC converter would make or exceed the power requirements outlined in table 1.2 Chapter 1. This was performed for all three transformers prior to designing in the post regulators for the non-regulated secondary windings.

Since secondary windings 3 and 5 draw the most load current, Schottky barrier rectifiers were utilised as these have a low forward voltage drop thus reducing power loss. The only drawback is the leakage current increases rapidly with temperature; for example, at 25°C the leakage current is 0.1mA but increases to 12.5mA at 100°C.

It is also relevant to keep the reverse capacitance small versus the reverse voltage, as this has an impact on the magnitude of noise and ripple, due to reverse recovery of the rectifier diodes. The other windings have low load current properties. This low load current lends itself to using ultra fast recovery rectifiers that have fast reverse recovery times of 25ns rather than Schottky diodes. Figures 2.5 to 2.7 show photographs of each of the transformer boards with their associated rectifiers.



Figure 2.5 The Aerostanrew (mod1) transformer with the Microsemi full wave rectifier diodes connected to the board.

Aerostanrew (mod 1) toroid transformer

To increase the flux linkage coupling between the primary and all secondary windings the first the primary windings of 14+14 turns is wound on the inner of the core. Then the other split primary winding of 13+13 turns is wound on the outer of the core . All windings are wound bifilar and are evenly distributed around the core. The windings on W1a and W1b is a continuous winding. The turns of windings two and four are evenly spaced within the turns of winding 1a.

The primary inductance for the Aerostanrew (mod1) and the Etal -A is calculated using :-

$$Lp = Np^2 * Al \tag{2.4}$$

Note the *Al* value of the toroid transformer is referenced to the magnetics part number ZF41605TC.

Therefore
$$Lp = 54^2 * 1650 * 10^{-9} = 4.8 \text{mH}$$
 (2.5)

The calculated primary inductance agrees with the measured inductance value as shown in Table 2.3.

Table 2.3Summary of the manufactured high frequency transformer identifyingthe number of turns per windings including inductance with wire length.

Wdg	Turns	Wire	Wire	Nominal	Nominal total primary	Wire length
#	mod	mod	mod	Inductance	Inductance	
	(1)	(1)	(1)	across each	@36Khz	(mm)
	od:	od:	od:	wdgs	(mod1)	
	(mm)	(mm)	(mm)	measured@36		
	bifilar	single	bifilar	Khz		
				(mod 1)		
1a	14 +14.	0.25	0.375		4.8mH	350 + 350
					across pins 1 and 3	
2	37 + 37	0.1	0.2	9.35mH		760+760
3	18 + 18	0.25	0.5	2.23mH		400+400
4	9 + 9	0.1	0.2	579µH		225+225
5	8 + 8	0.25	0.5	456μΗ		200+200
6	5 + 5	0.315	0.63	175µH		150+150
1b	13 + 13	0.25	0.375			325+325

It should be noted that this toroid has no insulation barrier between the primary and secondary windings hence the tight coupling factor of K = > 0.9. The galvanic insulation barrier between primary and secondary winding relies on the insulation of the copper wires which is effective to 500Vdc only.



Figure 2.6 Etal-A transformer with the Farnell full wave rectifier diodes connected to the board.

Etal –A toroid transformer.

The primary is wound above the secondary winding with a clear insulation layer washer of $\cong 0.25$ mm thick between both windings. This clear insulation washer is also used at the bottom of the toroid, separating the primary windings from the secondary windings. This reduces the flux linkage between primary and secondary and also reduces the coupling factor K. By introducing this insulation washer the insulation between primary and secondary is raised to >500Vdc. It should also be noted that the introduction of the insulation washer will increase the wound height of the toroid to 0.5mm. That will effect a small rise in temperature of this toroid core.



Figure 2.7 Etal-B transformer with the Farnell full wave rectifier diodes connected to the board.

Etal –B toroid transformer.

This toroid transformer uses identical construction methods and insulation properties to the Etal- A transformer but has a lower initial permeability and uses P grade ferrite material only.

Magnetising inductance

The magnetising current (*Imag*) for a push-pull transformer is added to the MOSFET peak current at turn on. This equation is defined $V_L = L \frac{\Delta i}{t_{on}}$

transposing this formula to determine $L = \frac{VL * t_{on}}{\Delta i}$ as $VL = V_{in} = 28V$. Hence

$$Imag = \frac{V \operatorname{Pr} \operatorname{imary peak} * On \operatorname{time}}{L \operatorname{Inductance of one split primary winding}}$$
(2.4)

$$Imag = \frac{28 * 5.7 * 10^{-6}}{5.32 \text{mH}} = 31 \text{mA}$$
(2.5)

The mag current of 31 mA represents 8% of the total primary peak current which is 386mA pk as shown in figure 2.8.



Figure 2.8 Shows the gate voltages and the primary current of winding 1. The Y axis represents a gate voltage of 12 volts and a peak primary switching current(x10) of 386mA. The non conduction time in the X axis is 4.6μ s.

This is for the Aerostanrew (mod1) toroid where $\mu i = 3000$ and Vin nominal is +28Vdc. It is important to compare this result with with the ETAL-B toroid that has a different initial permeability $\mu i = 2500$. The current waveform using this toroid at turn on is 6.68us.

Since the Etal-B transformer uses a lower permeability material more magnetising current is required for the same number of turns, in this case 22.3mA. This magnetising current represents 9.75% of the total primary peak current which is 400mA pk. This measurement is for the Etal-B toroid where $\mu i = 2500$ and Vin nominal is +28Vdc.

Transformer winding for low leakage inductance.

Measuring leakage inductance is achieved by shorting each secondary and measuring the inductance at the primary. For all three transformers the intention was to have low leakage inductance to lower distortion of the rise time or leading edge of the trapezoidal switching wave form. A comparison of low leakage inductance is shown in table 2.4. The short leading current edge time as shown in

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figure 2.8 takes 2μ S to reach 386mA. This example is for the toroid high frequency Aerostanrew (mod1) transformer.

To reduce distortion at the top of the pulse on the trapezoidal switching waveform, the primary inductance is selected to be high with a lower number of turns and a high A_1 value.

This implies a nominal initial permeability of 3000 for the MnZn transformer ferrite core, as shown in Table 2.1. On investigating Table 2.4, it is noted that in the Aerostanrew (mod1) transformer, the control secondary winding 6 (column1) has a higher leakage inductance by a factor of 32 when compared with the same winding on the Etal-A transformer. In addition the leakage inductance on the Aerostanrew (mod1) transformer for winding 4 when compared with the Etal-A transformer has an increased leakage inductance by a factor of 7.7. Using the same analytical process, winding 5 also has an increase in leakage inductance by a factor of 8.7. The other secondary windings of all three toroid transformers demonstrate insignificant differences in leakage inductance. The reason for the increase in leakage inductance is due to the separation of the primary and secondary winding on the core. Coil separation of the windings allows higher isolation between input and output at the cost of higher leakage inductance.

Measured	Results in (µH)	Results in (µH)	Results in (µH)
leakage	Aero (mod1)	Etal-A	Etal –B
inductance			
Wdg 2	2.0	2.7	3.14
Wdg 3	2.02	1.65	1.22
Wdg 4	7.7	1.0	0.8
Wdg 5	4.78	0.55	0.61
Wdg 6	11.6	0.36	0.373

Table 2.4 Summary comparison of the leakage inductance for all three toroid high frequency transformers.

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Within the high frequency toroid transformer, distributed between the primary and secondary windings, are parasitic capacitances. These capacitances may affect the performance in the form of a low self resonant frequency with reduced rise times and ringing taking place. Since it is desirable to reduce this capacitance effect, a summary comparison, Table 2.5, is shown for all three transformers. The method used to measure distributed capacitance is to short the primary windings and then short the secondary windings. Using a calibrated Fluke capacitance meter, the capacitance between the primary and individual secondaries are then measured in turn.

Using the numerical distributed capacitance results in Table 2.5, for winding 5 the capacitive coupling for this interleaved winding on the Aerostanrew (mod 1) is worse by a factor of 1.9, when compared to the Etal-A transformer. However for windings 2 and 3 of Etal-A transformer the distributed capacitance is higher by a factor of 3.5 when compared to the Aerostanrew (mod1) transformer. Comparing the Aerostanrew (mod1) transformer for winding 3 the Etal-B distributed capacitance is also higher by a factor of 1.29.

Table 2.5 Summary comparison of the distributed capacitance for all three toroid high frequency transformers.

Measured	Capacitance results	Capacitance results	Capacitance results in
distributed	in (pF)	in (pF)	(pF)
winding	Aero (mod1)	Etal -A	Etal –B
capacitance from			
primary to			
secondary.			
Wdg 2	41	146	51.74
Wdg 3	41	109	52.8
Wdg 4	19	19.2	15.11
Wdg 5	30	15.5	22.8
Wdg 6	19	14.3	20.3

2.7 Summary

The major distinction between Aerostanrew(mod1) toroidal transformer and the Etal series of toroidal transformers is that Aerostanrew increases the flux linkage by not using insulating washers between the primary and secondary windings.

In addition the coupling factor K is increased beyond 0.9. On the specific windings the interwinding capacitance of the Aerostanrew (mod1) toroidal transformer is less when compared to that of the Etal series of toroidal transformers, as outlined in table 5.

The calculated core losses for the Magnetics P ferrite are significantly lower than the Fgrade material.

There is a trade-off between copper losses on bifilar windings and a lower rather than a higher dc isolation voltage. This is because of the number of twist per turn when implementing bifilar windings will lower the the dc isolation voltage.

The reason why the particular buck derived push-pull topology is adopted here over other topologies are for the following reasons:

- Two conduction cycles of alternating conversion switches MOSFET Q3, and MOSFET Q4, that permit the average current levels in each set to be reduced by less than fifty percent when comparing with single switch topologies.
- When both MOSFET are switched off the full wave rectifier diodes operate in parallel, with the result that the secondary currents are summed at the input of the inductor allowing the inductor current to be continuous.
- Drain current is reduced as a function of the turns ratio $=\frac{N2}{N1}$.
- Full wave rectification Schottky diode power dissipation losses are considerably lower because of the lower forward voltage.

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- Good line and load regulation prevail at the minimum dc source voltage.
- Cross conduction of MOSFET Q3 and MOSFET Q4 are not possible because of the advanced CMOS peak current mode controller used.
- By implementing a higher initial permeability of μi 3000 it is possible to achieve empirical efficiency figures of 80% at maximum load.
- By implementing the permeability of the Magnetics F grade μi 3000 and P grade μi 2500, the measured results indicate that there is a 1% difference in the conversion efficiency and power loss when operated in the continuous mode.
- The centre-tap push pull converter with peak-current mode control and slope compensation offers the choice to operate either in the continuous or discontinuous conduction modes. The LT1683 slope compensation reduces sub harmonic instability in the current mode control at high duty cycles.

The disadvantage is that both MOSFET Q3 and MOSFET Q4 will have more than twice the input votage when in the off state hence a higher MOSFET drain voltage is required.

The Impact of Voltage Slew Rate on the Device Losses

3.1 Introduction

This chapter investigates the impact that voltage slew-rate has on the primary MOSFET device losses. Voltage slew-rate is defined here as the time V_{ds} takes to rise from its saturated value to its off-state (for turn-off) and vice-versa for turn-on. A slew rate control technique, originated by Brewster and Nelson [19], in a custom designed CMOS controller, was identified [7] as a promising route for assessing voltage slew rate limiting and has been implemented as described in Chapter 2. The voltage slew-rate can be controlled on the DC-DC control board and is configured to provide an adjustable slew-rate setting of between 400ns and 900ns.

The continuous conduction mode of operation is used in the prototype DC-DC converter as this achieves high primary conversion efficiency as the peak output inductor current (hence MOSFET turn-off current) is lower than that required with discontinuous current.

The impact of slew rate was assessed under the following test conditions related to the primary current waveform. The duty cycle, δ , with a dc source voltage of 28V (nominal) is :-

$$\frac{ton}{T} = \frac{5.7 \ us}{26.5 \ us} = 21.5\% \quad \text{at full load.}$$
(3.1)

3.2 Experimental method

The switch drain-source voltage, V_{ds} , and the switch drain current, i_d , are sampled over one switching cycle using a 500MHz digital oscilloscope. The sampled data is then imported into a spreadsheet and processed offline in order to calculate the turn-on (E_{on}), turn-off (E_{off}) and conduction (E_{con}) energy loss in the switch during a primary switching cycle. Typically, a few hundred sample points are taken for the three periods of the cycle (turn-on, turn-off, and conduction) as the oscilloscope is capable of sampling with 4ns resolution. The samples have 8-bit accuracy so care is exercised in order to maximise the dynamic range of the captured signal in order to reduce quantisation error.

The energy dissipated in the MOSFET during a turn-off transition is

$$E_{off} = \int_{toff} V_{ds}(t) I_d(t) dt$$
(3.2)

The turn-on energy losses in the MOSFET is

$$E_{on} = \int_{ton} V_{ds}(t) I_d(t) dt \tag{3.3}$$

And the conduction energy losses

$$E_{con} = \int_{con} I_d^2 R_{dS} \quad (t) dt \tag{3.4}$$

Each energy loss component is readily calculated from the captured data using a spreadsheet application (EXCEL). In each case, the start and end of each transient period is determined by examining the waveform and its associated numerical values in the spreadsheet. The MOSFET (Q3) is an IRF640 device with an R_{dson} of 150m Ω (nominal).

From the captured data, the power loss associated with turn-on (P_{on}) , turn-off (P_{off}) and conduction (P_{con}) can be determined by multiplying each energy loss component by the switching frequency. This off-line processing is performed for the three transformers at six different slew-rate settings: 400ns to 900ns in 100ns steps. The total switch loss can then be determined by summing the three loss components.

The turn-on period starts as V_{ds} begins to fall and ends when it has reached the onstate value. The conduction period of the MOSFET is defined to start when V_{ds} has collapsed to its on-state value and i_d begins to rise in the primary of the transformer, as shown in Figure 3.1, and ends when the primary current collapses coincident with the rise time of V_{ds} . The turn-off period starts as V_{ds} starts to rise and ends when i_d has reached zero.



Fig 3.1 The illustration of when the V_{ds} saturation voltage collapses and the on state conduction current starts to rise as measured on circuit reference MOSFET Q3 only.

The two figures below represent turn-on and turn-off waveforms with a slew-rate setting of 600ns using the Aerostanrew (mod 1) transformer. It is clear that both turn-on and turn-off transients take 600 ns.

In figure 3.1 the plateau waveform of *id* at the start of turn on and end of turn off is caused by the voltage slew. Since the *Vds* is ramping smoothly, the current in the MOSFET Q3 switch is roughly C^*dV/dt where *C* is the capacitance on the switch node. Note: *C* is used on both push pull switches and is called *Cva* and *Cvb*.

During slew the MOSFET is in a linear mode and is part of a control loop so the gate voltage is just above threshold roughly Vt+Id/gm. The current slew rate is set to be very fast based on di/dt of current waveform in figure 3.1.



Fig 3.2 Example of (a) turn on (V_{ds} 20V/div, i_d 100mA/div), and (b) turn off (V_{ds} 20V/div, i_d 100mA/div), both with a slew rate setting of 600ns.

The conduction loss measurement is facilitated by measuring the primary current i_d , using a Hall-effect probe calibrated to 100mA per division on channel 1. The probe is a Tektronix TCP 202 current probe. For each value slew-rate setting the current probe was degaussed and calibrated before measurements were made. For measurements made on channel two, the probe was calibrated and compensated using the internal squarewave reference of the oscilloscope. V_{ds} is measured using the calibrated, compensated, x10 500MHz probe (P6139A) on channel 2.

It should be noted the losses measured and recorded are evaluated for one MOSFET (Q3) only. It would be incorrect to assume that when the additive losses are calculated for conduction, turn on and turn off for Q3 will be the same for MOSFET Q4. There will often be slight differences of R_{dson} and gate charge due to MOSFET process spread. However, the measurements made on MOSFET Q3 are indicative of the changes in losses that occur with the slew-rate setting.

To calculate the turn on and turn off losses from the measured voltage and current waveforms, the process is similar. Table 3.1 shows an excerpt from one of the spreadsheets and illustrates how the energy loss components are determined from the oscilloscope-captured voltage and current transients. The product of the voltage and current is calculated 'v*i' and this is numerically integrated over each sample time in the 'int(v*i)' column using the rectangular integration approximation. The 'Energy' column then sums these integral contributions over the period of the transient.

Time	Current	Voltage	v*i	int(v*i)	Energy
5.73E-08	0.238	2	0.476	9.36E-10	2.57E-08
5.93E-08	0.23	2	0.46	9.12E-10	2.66E-08
6.13E-08	0.226	2	0.452	8.96E-10	2.75E-08
6.33E-08	0.222	2	0.444	1.05E-09	2.85E-08
6.53E-08	0.218	2.8	0.6104	1.04E-09	2.96E-08
6.73E-08	0.214	2	0.428	1.02E-09	3.06E-08
6.93E-08	0.21	2.8	0.588	1.16E-09	3.17E-08
7.13E-08	0.206	2.8	0.5768	9.89E-10	3.27E-08
7.33E-08	0.206	2	0.412	8.16E-10	3.35E-08
7.53E-08	0.202	2	0.404	9.47E-10	3.45E-08
7.73E-08	0.194	2.8	0.5432	9.15E-10	3.54E-08
7.93E-08	0.186	2	0.372	7.36E-10	3.61E-08

Table 3.1. Excerpt of the Excel spread sheet that calculates the energy loss component.

Comparisons of inductive load switching losses are investigated using the three types of transformer-rectifier boards. All primary and secondary windings are composed of single-strand copper wire. Only one toroid transformer has a different permeability to the other two. The Etal-B toroid has an initial permeability of μ_i =2500 and Al = 1805. The Aerostanrew [mod 1] and Etal-A have initial permeabilities of μ_i =3000 and Al = 2166.

The system using the Aerostanrew (mod1) transformer has Microsemi Schottky rectifiers which have a lower forward voltage drop and faster reverse recovery time than the Schottky diodes used on the Etal-A and Etal- B transformers. The Microsemi Schottky diode increases the conversion efficiency and lowers the power dissipation.

3.3 MOSFET losses with the Aerostanrew transformer

Table 3.2 details the loss components measured on the system utilising the Aerostanrew transformer for each of the 6 slew-rate settings. From Table 3.2 it is clear that the turn-on and turn-off losses increase as the slew-rate setting is increased. In this system the turn-off loss component is dominant at the longer slew rate settings, but is approximately the same magnitude at 400ns.

The turn-on loss component does not vary as much as the turn-off loss as the slew rate setting is changed. The conduction loss component is approximately a factor of 2 lower than the turn-on loss. Figure 3.3 graphs these results and shows the rate of change of loss component with slew rate setting.

Table 3.2. Variation of loss components E_{on} , E_{off} and E_{con} with slew rate setting for the system with the Aerostanrew (mod1) transformer.

Slew rate setting	Conduction		
(ns)	loss (nJ)	Turn-on loss (nJ)	Turn off loss (nJ)
400	95	217	236
500	103	228	472
600	105	283	709
700	108	291	1010
800	124	320	1230
900	125	350	1330

Table 3.3 The linear gradient of increased Δ energy turn-off losses versus an increase of the slew- rate setting

slew-rate setting increment (ns)	Turn-off energy Δ losses (nJ)
400-500	236
500-600	237
600-700	301
700-800	220
800-900	100



(c)

Fig 3.3 (a) Variation of the conduction loss component E_{con} and (b) turn on loss component E_{on} and (c) Variation of loss component for turn off E_{off} versus the slew rate setting with the Aerostanrew transformer in the system.

The Aerostanrew transformer (mod1) results in Table 3.2 are plotted in figure 3.3 (a), (b) and (c). The turn-off losses vary linearly with the slew-rate as the slew-rate is increased from 400ns to 900ns. During turn-off, i_d is held at a constant value, Figure 3.2(b), whilst V_{ds} is linearly ramped back to its off value. The total turn-off loss is determined by the area under the graph of the instantaneous power, and, as the time to slew between on and off states increases, there is a linear

increase in the turn-off energy loss. This is clearly shown in the results shown in Table 3.2. A similar process occurs at turn-on and the loss component increases with a linear slope as the slew-rate setting is increased from 400ns to 900ns.

Table 3.3 details the change in turn-off energy loss with slew-rate setting between 400ns and 900ns in steps of 100ns. This clearly shows the trend of turn-off loss with slew-rate setting and indicates an average of 219nJ change for each 100ns increase in slew-rate. The change from 800ns to 900ns produces a lower change in turn-off loss.

Table 3.4 Measured loss components E_{on} , E_{off} and E_{con} for voltage slew-rate settings of 400ns and 900ns. Power loss is derived by dividing energy with the primary switching period T = 26.5us.

Loss Component	Peak energy losses	Power loss	slew-rate setting
	(nJ)	(mW)	(ns)
Eoff	236	9	400
Eon	217	8.2	400
Econ	95	3.6	400
Total energy loss	548	21	
Eoff	1330	50	900
Eon	350	13	900
Econ	125	4.7	900
Total energy loss	1805	67.7	

Table 3.4 compares the sum of three switching component energy and power losses for slew rate settings of 400ns and 900ns. This demonstrates the significant impact that the slew rate setting has on the total switching loss in the primary MOSFET device. The major contributor is E_{off} . The total MOSFET losses increase by a factor of 3.3 when the slew rate setting is changed from 400ns to 900ns.



Fig 3.4 The histogram illustrates the distribution of energy loss as a function of different slew-rate setting for the Aerostanrew (mod 1) transformer.

Figure 3.4 shows pictorially the distribution of switch loss as a percentage of the total switching loss component for each slew-rate setting and illustrates the effect of varying the slew rate setting. The turn-off energy loss contribution gradually increases from 45% at 400ns to over 70% at 900ns.

One of the main reasons why the turn-off energy loss is higher than turn-on energy loss is because the drain current plateaus at a larger current value at turn-off than at turn on. For evidence of this effect see figure 3.2(a) turn-on and 3.2(b) turn-off current and voltage characteristics: the current plateaus at 118mA at turn-off but only 40 mA at turn-on. Turn-on energy losses are between 217nJ and 350nJ for slew rate settings between 400ns to 900ns compared with 236nJ and 1330nJ for turn-off.

There is another power loss that has is no direct correlation with changes to the slew rate setting but does add a small power loss. This is due to the *Cds* of Q3 MOSFET which also affects the turn-on losses because *Cds* charges up during turn-off and during turn-on the stored energy is dissipated in the MOSFET. The power loss associated with C_{ds} is

$$P_{loss,Cds} = \frac{1}{2} * C_{ds} * V_{in} {}^{2} * f_{sw}$$
(3.5)

This results in a fixed turn-on loss component. The fixed component can be observed by extrapolating the turn-on loss curve back to the y-axis in Figure 3.3(b). The fixed component is mainly due to the dissipation of stored energy in C_{ds} in the MOSFET. The variable component is determined by the slew-rate setting.

3.4 MOSFET losses with the Etal A transformer

Table 3.5 details the three energy loss components for the 'Etal_A' transformer for slew-rate settings from 400ns to 900ns. As predicted the turn on and turn-off losses follow an increasing trend as the slew-rate setting is increased. For example, this is shown in figure 3.5(b) and figure 3.5(c). When the slew-rate setting is increased from 400ns to 500ns the delta energy losses peak at 330nJ. The turn-on loss component shows an almost linear increase with increasing slew rate settings. The conduction loss component is approximately a factor of 1.7 smaller than the turn on loss at 400ns. This factor increases to 2.6 for slew rate setting of 900ns.

Table 3.5 Variation of loss components E_{on} , E_{off} and E_{con} with slew rate setting for the system with the Etal-A transformer.

Slew rate setting	Conduction losses	Turn on losses	Turn off losses
(ns)	(nJ)	(nJ)	(nJ)
400	113	194	595
500	119	241	925
600	120	255	1060
700	120	267	1210
800	125	289	1490
900	124	325	1740

Table 3.6 The change in E_{off} versus slew rate setting

slew-rate setting increment (ns)	Turn-off energy Δ losses (nJ)
400-500	330
500-600	135
600-700	150
700-800	280
800-900	250



Fig 3.5 (a)Variation of conduction loss component E_{con} , (b) turn-on loss component E_{on} , and (c) turn-off loss component E_{off} versus the slew rate setting with the Etal-A transformer in the system.

On assessment of Fig 3.5 regarding the variations of the three switching losses for the Etal-A transformer data, the total energy losses are now identified and compared with the six settings of the slew rate extracted from Table 3.5.

At the lower end of the slew rate setting the turn-off losses rise rapidly from 400ns to 500ns resulting in a energy loss 925nJ. At the other extreme, with a slew rate setting of 900ns, the loss component peak is 1740nJ. When comparing the variation of the slew rate setting for turn-off between the Aerostanrew (mod1) transformer system and the Etal-A transformer system as shown in figure 3.3(c) and figure 3.5 (c) both exhibit a similar linear variation. From Table 3.5 with a slew rate setting of 900ns the turn-on energy loss is 325 nJ when compared to 194nJ for 400ns. As expected the losses increase with slew-rate setting.

Observation of the influence of the slew-rate setting on the conduction losses illustrates a gradual but small linear increase in energy losses. However it is observed that between 600ns and 700ns slew rate setting the energy losses do not record an increase in level. Between 600ns and 700ns the energy losses remain static at 120nJ.

The measured peak conduction losses recorded the peak at 125nJ when the slew rate setting was increased to 800ns.

Table 3.7 Measured loss components E_{on} , E_{off} and E_{con} for voltage slew-rate settings of 400ns and 900ns. Power loss is derived by dividing energy with the primary switching period T = 26.5us.

Loss Component	Peak energy	Power loss	slew-rate setting
	losses (nJ)	(mW)	(ns)
Eoff	595	22	400
Eon	194	7.3	400
Econ	113	4.3	400
Total energy loss	902	33.6	
Eoff	1740	65.7	900
Eon	325	12.2	900
Econ	124	4.7	900
Total energy loss	2189	82.6	

The effect of utilising the Etal-A transformer means the total peak energy losses for the three switching components have increased by 21.3% when compared with the Aerostanrew (mod1) transformer peak energy losses at a slew rate setting of 900 ns.

The drain current plateau have the same values as that observed for the Aerostanrew (mod) for turn on and turn off.



Fig 3.6 The histogram illustrates the distribution of energy loss as a function of different slew-rate setting for the Etal-A transformer.

The histogram in figure 3.6 illustrates that with the Etal-A transformer system whilst the turn off losses increases with slew rate setting they are relatively constant compared to the Aerostanrew system.

3.5 MOSFET losses with the Etal-B transformer

The energy loss components are identified using the Etal_B transformer and the six slew rate settings. The turn on energy losses increase linearly as the slew rate setting is gradually increased from 400ns to 900ns, Fig 3.7(b), and the results
demonstrate that there is a fixed loss component of around 100nJ most probably associated with the energy stored in the drain-source capacitance at turn-on. The conduction loss component is approximately a factor of 1.6 smaller than the turn on loss at 400ns and remains approximately constant, as expected, as the slew-rate setting increases.

In Table 3.8 and Fig 3.7(c) the turn off losses vary linearly with the slew rate setting. The peak energy loss is 1740 nJ for a slew rate setting of 900ns. Correspondingly, at this slew rate setting the turn on losses peak at 325 nJ. Examining the turn off losses between 400ns and 700ns it is noticed that the Etal-B E_{off} losses are slightly less than the E_{off} Etal-A transformer.

Table 3.8 Variation of loss components E_{on} , E_{off} and E_{con} with slew rate setting for the system with the Etal-B transformer.

	Conduction	Turn on	Turn off
Slew time (ns)	(nJ)	(nJ)	(nJ)
400	120	189	551
500	121	207	889
600	128	219	971
700	130	229	1190
800	135	300	1600
900	139	325	1740

Table 3.9 Change in E_{off} versus slew rate setting.

slew-rate setting increment (ns)	Turn-off energy Δ losses (nJ)
400-500	338
500-600	82
600-700	219
700-800	410
800-900	140





(c)

Fig 3.7 (a) Variation of conduction loss component E_{con} , (b) turn on loss component E_{on} and (c) Variation of turn off loss component E_{off} versus the slew rate setting with the Etal-B transformer in the system.

Table 3.10 lists the measured results for the energy loss components for the Etal-B transformer for 400ns and 900ns. Increasing the slew rate setting increases the total switch losses by a factor of 2.6.

Chapter Three

Table 3.10 Measured loss components E_{on} , E_{off} and E_{con} for voltage slew-rate settings of 400ns and 900ns. Power loss is derived by dividing energy with the primary switching period T = 26.5us.

Loss Component	Peak energy	Power loss	slew-rate setting
	losses (nJ)	(mW)	(ns)
Eoff	551	20.8	400
Eon	189	7.13	400
E _{con}	120	4.53	400
Total energy loss	860	32.5	
Eoff	1740	65.7	900
Eon	325	12.26	900
E _{con}	139	5.25	900
Total energy loss	2204	83.2	



Fig 3.8 The histogram illustrates the distribution of energy loss as a function of different slew-rate setting for the Etal-B transformer.

The turn-off losses account for a higher proportion of energy losses when compared to the other two switching losses, Fig 3.8. Investigation of the measurement of the current plateau at a slew rate setting of 600ns yielded 118mA at turn-off and 32mA for turn on. These values are similar to the Etal-A transformer in section 3.3 and differ slightly only at turn-off by -8mA when comparing this result with the Aerostanrew (mod1) transformer as outlined in section 3.2.

3.6 Comparing the MOSFET losses for all three transformers

For each slew rate setting the Aerostanrew (mod 1) transformer yields lower turnoff energy losses than either Etal transformers (A) or (B) by a factor of 2.5 at a slew rate setting of 400ns. This factor becomes less, approximately 1.3 at a slew rate setting of 900ns.

3.7 Turn-off Loss Comparison

Table 3.11. Comparison of measured leakage inductance L_k for all three transformers.

Aerostanrew	(mod1)	L(k)	Etal-A	L(k)	(μH)	Etal-B	L(k)	(<i>µH</i>)
(µH)								
1.55			1.95			2.70		

The primary leakage inductance L(k) contributes the turn-off switching energy losses. Table 3.11 details the measured leakage inductance and demonstrates the variation in value for each of the three transformers. The variation in leakage inductance contributes to the differences in turn-off loss component measured for each of the three transformers. The leakage inductance in the Etal-A and -Btransformers is significantly higher than the Aerostanrew transformer leading to a higher value of stored energy at turn-off (this is evidenced in Fig 3.9(a)). The drain current plateau during turn-off is the same with all three transformers. Examining the coefficient of coupling (K) versus the leakage inductance it is possible for (K) be estimated using the formula:

$$M = (K) \sqrt{Lpri * L \sec}$$
(3.6)

Transposing the formula gives

$$K = \frac{M}{\sqrt{Lpri * L \sec}}$$
(3.7)

The leakage inductance calculation L(k) (3.8) is widely used and is based on the formula in [8].

$$L(k) = \frac{292 * N \, 1.065 * Ae}{I_e * 10^5} \tag{3.8}$$

where N = the number of turns

Ae = cross-section area (cm²).

 I_e = core magnetic path length (cm).

In order to effect lower switching losses it is necessary to lower the leakage inductance $L_{(k)}$. The formula for the power switching loss contributed by the leakage inductance $L_{(k)}$ is :-

$$P_{SW,L(k)} = \frac{1}{2}L(k) * I_{prim}^{2} * F_{SW}$$
(3.9)

Where $L_{(k)}$ represents the leakage inductance of the primary winding.

The increase leakage inductance also reduces the coupling factor (K) between primary and secondary winding. The coupling factor (K) is less than 0.9 for both Etal-A and Etal-B, whereas it is greater than 0.9 for the Aerostanrew (mod1) transformer.

The transformer primary current is composed of the magnetising current plus the output current. It follows that having a lower core permeability means that an increased magnetising current is required for the same number of turns.

The data presented in Figure 3.9 (a), (b) and (c), for the variation of the slew rate setting from 400ns to 900ns, is selected not only to illustrate the comparison of losses for each of the three switching components, but primarily because of the

fundamental importance of identifying the trend of switching energy loss components that it represents.



(a)

(b)



(c) Fig 3.9 (a) Comparison of turn off component E_{off} loss (b) Comparison of turn on loss component E_{on} and (c) Comparison of the variation of conduction loss, E_{con} versus the slew rate setting and for all three transformers.

The energy loss component for turn off is illustrated in figure 3.9 (a). The difference between the system using the Aerostanrew (mod1) transformer and the

system using Etal-A transformer is 359 nJ at 400ns. For a slew rate setting of 900ns on the Etal –A transformer, the turn off energy loss has increased by 410 nJ when compared with the Aerostanrew (mod1) transformer. Both Etal-A and Etal-B systems display similar turn-off losses and are higher than the Aerostanrew(mod1) system.

3.8 Turn-on Loss Comparison

Examining the turn-on energy loss component when the slew setting is at 400ns. Figure 3.9 (b) the Aerostanrew transformer exhibits a slightly higher energy loss of 217nJ when compared to the Etal A and B transformers which display energy losses of 194 nJ and 189nJ respectively. With a slew-rate setting of 900ns, the turn-on energy losses are 325nJ with both the Etal A and B transformers, compared to 350nJ for the Aerostanrew (mod1) transformer.

The reason why the turn on characteristics has similar energy loss components is that the turn on times are similar, as are the trajectories of voltage and current during turn-on. Evidence of this similarity is clearly demonstrated for the turn on transition at 400ns for all three transformers and is illustrated in figure 3.10 (a) for current and 3.10 (b) for voltage.



(a)

(b)

Fig 3.10 Comparison of the (a) current and (b) voltage transition for the three transformers during turn on at 400ns. For both Figures of 3.10 (a) and (b) the x axis is calibrated to 250ns/division.

The reason for the slight difference in current trajectory during turn-on in figure 3.10 (a) is explained by the different magnetising currents required for each transformer. The peak magnetising current is determined from the formula:

$$I(p\ m) = \frac{Vdc}{Lm} * t_{on}$$
(3.10)

 L_m is the inductance of one split primary winding. The measured primary inductance at 10 kHz is different for all three transformers as shown in Table 11. The primary inductance associated with each transformer is different yielding slightly different turn on time trajectories, hence losses.

Aerostanrew	(mod1)	Etal-A	L(m)	(μH)	Etal-B	L(m)	(<i>µH</i>)
$L_{(m)}(\mu H)$							
4.84		4.72			4.36		

Table 3.12. The primary inductance for all three transformers

Listed in Table 3.12 is the distributed capacitance C_{dis} of the primary winding for all three transformers. These are the parasitic capacitive elements distributed between the turns of the windings. The distributed capacitance results in stored energy that gives rise to current spikes during turn on and additional energy losses. There is also parasitic capacitance across the leakage inductance. This will have a smaller effect on the turn-on losses.

Table 3.13 Comparison of the measured primary distributed capacitance C_{dis} for all three transformers.

Aerostanrew	(mod1)	<i>C</i> _{dis}	Etal-A	C_{dis} (pF)	Etal-B	C_{dis} (pF)
(pF)						
19			170		21	

From table 3.13 it is noted that the Etal –A transformer has a higher C_{dis} capacitance that has increased by a factor of 8.9 when compared with the Aerostanrew (mod1) and Etal-B transformer. The reason why the Aerostanrew transformer has a lower C_{dis} and L(k), when compared with the Etal-A and Etal-B transformers, is due to the method of interleaving the primary with the secondary windings on the ferrite core. The construction methods are detailed in chapter 2 section 2.6.

3.9 Conduction Loss Comparison

The conduction losses are minimised by selecting a MOSFET with a low $R_{ds,on}$ but this tends to increase the gate charge. The conduction losses as shown in figure 10 (c) are the lowest recorded loss component when compared with turn-on and turn-off loss components.

As expected, the conduction energy loss components remain approximately the same as the slew-rate setting is increased from 400ns to 900ns. Similarly, there is no significant difference between the conduction loss components for the three transformer types.

However between the slew rate settings of 400ns to 700ns the Aerostanrew (mod1) transformer exhibits the lowest level of conduction losses for all three transformers.

At slew rate settings of 800ns and 900ns there appears to be a one to one correlation of conduction losses with the Etal A and Aerostanrew transformer results.

The conduction loss component is not frequency dependent. However it is dependent on the duty cycle which has been determined by the equation in (3.1) for all of the measurements derived in this chapter.

3.10 Summary

In this chapter the impact that the slew-rate setting has on the turn-on, conduction and turn-off losses in the primary switching devices is considered. As expected, as the slew-rate setting is increased, the turn-on and turn-off losses increase as the device takes longer to transit from the off-state to the saturated on-state, and viceversa. The turn-on and turn-off losses will increase proportionately. The purpose of assessing the switch losses are two-fold; firstly, in order to assess the compromise that is made between switching loss and output voltage noise (as decreasing the slew-rate also decreases the output voltage noise), secondly, to evaluate how the transformer winding topology affects the losses.

The Aerostanrew (mod 1) transformer exhibits the lowest total energy losses of 548nJ with a slew-rate setting of 400ns. With a slew rate setting of 900 ns, the total losses increase to 1805nJ with this transformer. The Etal -B transformer exhibits the next lowest energy losses at 860 nJ at a slew-rate setting of 400ns. This increases to 2204nJ at 900ns. It is clear that the slew rate setting has a considerable effect on the MOSFET device losses.

The effect of reduced total switch losses for the Aerostanrew transformer is mainly due to the winding technique of individual primary layers, interleaved with the secondary windings. The Skein technique used also results in a more effective flux linkage between windings. This leads to lower leakage inductance $L_{(k)}$ and lower interwinding capacitance C_{dis} both of which reduce the turn-on and turn-off losses in the primary switching device. This results in improved overall system efficiency.



Figure 3.11Illustrates the distribution of power losses for a voltage slew rate of 400ns.

Figure 3.11 Shows the distribution of the power loss for (x2) circuit when the voltage slew rate setting is at 400ns. The main loss factors are due to the forward conduction of five individual full wave rectifiers into the network of resistive and capacitive loads shown in figure 1.2, page 17. This is followed by the copper

 I^2R losses of all primary and secondary windings in the push pull transformer circuit diagram reference (T1).

Reducing the dc resistance of the output inductor with reference to circuit element L1W6 on page 89, will optimize the conversion efficiency to approximately 85%.

Chapter Four Impact of voltage slew rate setting on the ouput noise

4.1 Introduction

In this chapter the impact of changing the slew rate on the magnitude of conducted noise emissions is assessed. Filtering of common mode conducted broadband emissions is a difficult proposition, as this occurs over a wide frequency range between 150 kHz to 150MHz. It is possible to lower the conducted emissions to noise levels below -100dBm by reducing the voltage slew rate. Voltage slew rate control lowers the harmonic components of the trapezoidal waveform at the output of the transformer secondary. Simple *LC* output filters also further reduce harmonic components.

There is a need to measure the attenuation of both the odd and even harmonics. MOSFET switching action produces odd harmonic components and even harmonics are associated with the output diode rectifier. The circuit diagram is shown in appendix A page 89.

Previous work [18] used current mirror gate drive techniques to lower highfrequency conducted emissions. The voltage slew-rate technique implemented here has the advantage over the current mirror driver as it provides increased attenuation of conducted emissions.

The conducted high frequency harmonic noise data was measured using an Anritsu spectrum analyser MS2719 B from 0Hz to 1MHz. The spectrum analyser has a calibrated resolution bandwidth of measuring noise levels in the frequency domain down to -153dBm. Harmonics of the fundamental switching frequency are doubled in frequency when measured at the low pass output filter after secondary full wave rectification.

All of the Anritsu spectrum analysis data is presented in appendix B, including the calibration of the input RF cable. Laplace transforms are used to derive the attenuation characteristics of the 2^{nd} and 4^{th} order filters.

4.2 The influence of the trapezoidal waveform on the output spectrum.

Conducted narrow band emissions are the dominant EMI emissions and must meet attenuation limits from 150 kHz to 30MHz. Investigating the CISPR publication 22, of the narrow conducted emissions limits of class B provides an average limit of magnitude with frequency. This limit line corresponds to a level below $\cong 55 \text{dB/}\mu\text{V}$ (-52dBm). Between 500 kHz and 5 MHz the level drops to approximately 46dB μ V equivalent to (-61dBm). Then after 5MHz the level increases to 50dB μ V to 30MHz, equivalent to (-57dBm). This information provides the limits of class B that can be used as a guide when investigating the narrow band conducted emission limits for the Gaia EMC and EMI specification [2].

The Gaia EMI specification calls up the conducted emission according to Mil standard 461. This specification calls for a limit to the ripple currents of $60dB\mu A$ (rms) from 10kHz to 100kHz. After this, the attenuation level rolls off at 10dB μA /decade till it drops to a level of 40dB μA (rms) at a frequency of 10 MHz and maintains this low level to 50 MHz.

Fourier analysis identifies that the amplitude of the high frequency harmonics of a trapezoidal voltage waveform attenuates at a rate of 40dB/decade beyond the 2^{nd} breakpoint [5]. The fundamental switching frequency is 75.636 kHz. Within the slew rate control system, the slew rate setting can be varied from 400ns to 900ns. With a slew rate setting of 400ns the frequency spectrum envelope will produce a second breakpoint at 796 kHz. This break point is beyond the 10th harmonic.

At 900ns the second breakpoint is 353 kHz which is below the 5th harmonic. This is identified in the spectra of Figure 4.1(a) between marker 4 and 5. The attenuation for this 2^{nd} breakpoint is approximately – 127dBm. Therefore as the slew rate setting is increased it will have an impact on the higher order harmonics but have no impact on attenuation levels for the lower order harmonics from the 1^{st} to the 5th harmonics

4.3 Experimental method and THD calculation

Measurements of conducted harmonic noise data are extracted from the regulated output of three individual transformer rectifier boards then stored on a USB memory stick. These are identified as Aerostanrew(mod1), Etal-A and Etal-B.

For each transformer, the spectrum analyser was used to extract data for conducted harmonic noise. The slew rate setting was adjusted using the slew rate potentiometer to 400ns, then repeated at intervals of 100ns to 500ns, 600ns, 700ns, 800ns, 900ns. The spectrum analyser was calibrated for a start frequency of 0Hz and a stop frequency of 800 kHz. As an example, figure 4.1 illustrates the output spectrum corresponding to a slew-rate setting of 600ns with the Aerostanrew (mod 1) transformer and rectifier board in place.



Fig 4.1(a) Illustrates the 1st to the 6th harmonic conducted emission from 0Hz to 800kHz.Measured on the (X2) prototype DC-DC converter for a slew rate setting of 600ns. This measurement was made with the Aerostanrew(mod1) transformer rectifier board in place.

Chapter Four The Impact of the Voltage Slew Rate Setting on the Output Noise



Fig 4.1(b) Illustrates the 7th to the 10th harmonic conducted emission from 0Hz to 800kHz. Measured on the (X2) prototype DC-DC converter for a slew rate setting of 600ns. This measurement was made with the Aerostanrew(mod1) transformer.

The total harmonic distortion is calculated according to DIN Standard 45403 part 2.

THD =
$$\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 \dots N_n^2}{V_a}} \div [V_a]$$
 (4.1)

Where V_2 is the rms voltage of the 2nd harmonic (4.2)

Vn is the rms voltage of the n^{th} harmonic

Va The fundamental rms voltage of the overall signal

In addition to the total harmonic distortion, the n^{th} order distortion factors are also defined:

$$D_2 = \frac{V_2}{V_a}$$
, 2nd order distortion factor (4.3)

$$Dn = \frac{V_n}{V_a}$$
, n^{th} order distortion factor (4.4)

In order to process the THD numerical results for all three transformers, the data was tabulated from the longest Vslew setting of 900ns, to the shortest Vslew setting of 400ns, with the corresponding measured attenuation level in – dBm for the 1^{st} to the 10^{th} harmonic. The – dBm value is then converted to *Vrms* and these used to convert to THD using (4.1). An example of how the THD is calculated is shown in table 4.1 for a voltage slew rate setting of 900ns.

Table 4.1 The 1 st to 10 th harmonic components (in –dBm) which are used to	
calculate THD. Slew rate setting is 900ns.	

- dBm	Harmonic	Vrms	V_{rms}^2	
-92		5.7E-06		
-100	Fundamental 1st	2.2E-06	5E-12	
-110	2	6.8E-07	4.70945E-13	
-107	3	1.0E-06	1.08635E-12	
-119	4	2.5E-07	6.51583E-14	
-113	5	4.6E-07	2.19265E-13	
-119	6	2.4E-07	6.09495E-14	
-120	7	2.3E-07	5.48239E-14	
-123	8	1.5E-07	2.5175E-14	
-128	9	9.0E-08	8.14648E-15	
-119	10	2.67E-07	6.76036E-14	
		SUM	2.05842E-12	1.43472E-06
			THD	0.641625687
			THD [%]	64.16256868

4.4 Analogue measurements of the output filters

It is rudimentary to measure the peak to peak ripple and noise floor using the oscilloscope when the DC-DC converter is turned off. This provides information that can be used to compare the difference of peak to peak ouput noise when the converter is activated with different slew rates.

This measurement is performed with the 50Ω impedance rf cable of 50cm in length. It is connected to channel 4 of the Tektronix TDS 744A digital oscilloscope with the input impedance set to 50Ω To match the input impedance of the oscilloscope to the 50Ω impedance rf cable, and the ouput impedance of the high pass *CR* network located on the DC-DC converter, a 51Ω metal film resistor

was connected in series with the output of the cable. Metal film is the best choice because it has low noise characteristics. The peak to peak ripple when the DC-DC conveter is off is illustrated in Fig 4.2 and shows the measurement noise floor.



Figure 4.2 Measured noise floor level of $920\mu V$ pk-pk, when the dc/dc converter is off.

The oscilloscope noise floor measurement is $920\mu V$ pk to pk with the dc/dc converter off. This noise floor is equivalent to -48dBm. The output ripple using each transformer are measured at each slew rate.

4.5 Analogue measurements of output voltage ripple

Two second order filters are cascaded at the regulated output of the +3.3V rail. Each second order filter rolls-off at 12dB/octave. The output ripple for the Aerostanrew (mod1) transformer are shown in table 4.2 with 400ns and 900ns, using both minimum and maximum resistive loads. Metal oxide resistors were used for both minimum and maximum load.

The first rectifier board, with the Microsemi rectifier diodes installed, was measured with the Aerostanrew (mod1) transformer in place. This provided the peak to peak ripple and noise in mV from both second order filters. All

measurements taken and recorded were selected on the full band width of 500MHz of the four channel Tektronix TDS744A oscilloscope.

The measurement exercise was then repeated for the Etal-A and Etal -B transformer rectifier boards in place, with their own generic Schottky rectifier diodes. This was to assess pk to pk noise and ripple in (mV) when measured at the regulated ouput. The pk to pk ripple and noise is then converted to (-dBm).

Table 4.2 Output voltage ripple on minimum load and full load at the slew rate setting of 400ns and 900ns: Aerostanrew (mod1) transformer rectifier board.

1	· · · · · ·	Vslew (ns)	Resistive load conditions
mv(p-p)) & (-dBm)		
1.44	(-44dBm)	400	min load 69Ω
0.86	(-49dBm)	400	max load 22Ω
0.92	(-48dBm)	900	min load 69Ω
0.80	(-49dBm)	900	max load 22Ω

The results listed in table 4.2 indicate that at a minimum load for a slew rate setting of 400ns produce an output voltage ripple of 1.44mV(p-p). At maximum load, for the same slew rate setting the result is 0.86mV(p-p). Increasing the load resistance reduces the output voltage ripple by 41%. In fact the output ripple is close to the noise floor suggesting excellent performance.

At a slew rate setting of 900ns at minimum load the result is 0.92mV(p-p). When switched to maximum load, the output ripple is 0.8mV(p-p). The ratio is 1.15. However these measurements are close to the noise floor, so it is difficult to discern any large changes in output ripple. At minimum load, the improvement in output ripple when moving from 400ns to 900ns is more apparent. For this transformer rectifier board at a slew rate setting of 400ns with full load, the peak to peak ripple is slightly more compared to a slew rate setting of 900ns. Table 4.3 Output voltage ripple on minimum load and full load at the slew ratesetting of 400ns and 900ns: Etal-A transformer rectifier board.

Output	ripple voltage	Vslew (ns)	Resistive load condition
mV(p-	p) & (-dBm)		
1.04	(-47dBm)	400	min load 69Ω
0.7	(-50dBm)	400	max load 22Ω
0.8	(-48dBm)	900	min load 69Ω
0.9	(-48dBm)	900	max load 22Ω

Table 4.3 details the results for the Etal A transformer. At minimim load with a slew rate setting of 400ns the output ripple voltage is 1.04mV(p-p). When switched to maximum load for the same slew rate yields 0.7mV(p-p) The ratio between these two results demonstrates that the ripple reduces by 33%. At a slew rate setting of 900ns and at minimum load the result is 0.8mV(p-p), and 0.9mV(p-p) at full load. This yields a drop of 1.125 in output ripple voltage. From the foregoing results demonstrate that a 400ns slew rate setting provides a lower output voltage ripple than 900ns.

Table 4.4 Output voltage ripple on minimum load and full load at the slew rate setting of 400ns and 900ns: Etal-B transformer rectifier board.

Output ripple voltage	Vslew (ns)	Resistive load condition
mV(p-p) & (-dBm)		
0.92 (-48dBm)	400	min load 69Ω
1.02 (-47dBm)	400	max load 22Ω
0.96 (-47dBm)	900	min load 69Ω
0.88 (-48dBm)	900	max load 22Ω

The results tabulated in table 4.4 for the Etal-B transformer indicate that with a minimum load, for a slew rate setting of 400ns, the output voltage ripple is 0.92mV(p-p). With maximum load, the same slew rate setting yields an output voltage ripple of 1.02mV (p-p). The ratio between these two results shows that the output voltage ripple increases by 10%. The result is 0.96mV (p-p) with a 900ns slew rate setting at minimum load decreasing slightly to 0.88mV (p-p) at full load.

For this Etal-B transformer rectifier board there is a marginal difference output voltage ripple between the two slew rate settings of 400ns and 900ns for minimum and maximum load. In all cases, with a slew rate setting of 900ns, the output voltage ripple is close to the noise floor. With a slew rate setting of 400ns, the Etal-A demonstrates the best performance at full load, with the Aerostanrew (mod 1) transformer demonstrating worse performance at minimum load.

4.6 Total harmonic distortion

From figure 4.3, the slew rate setting shows the THD between 400ns and 500ns is at the lowest level of distortion corresponding to $\approx 62\%$. As the slew rate setting is increased the effect is that the THD level increases slightly to peak at 68% at 600ns,then the level gradually decreases to 64% at 900ns. The extracted THD data is for the Aerostanrew(mod1) transformer.



Figure 4.3 Total harmonic distortion as a percentage versus the voltage slew rate setting. These measurements were taken from the Aerostanrew (mod1) transformer rectifier board.

Total harmonic distortion versus the voltage slew rate setting, figure 4.4, are for the Etal-A transformer rectifier board. The analysis of the THD for the Etal-A transformer rectifier board shows decreasing harmonic distortion when the slew rate is adjusted between 600ns and 900 ns. However, the THD rises slightly between 400ns and 500ns. At a 900ns slew rate setting, the Etal–A transformer displays 7% higher THD than the Aerostanrew (mod1) transformer rectifier board.



Figure 4.4 Total harmonic distortion as a percentage versus the voltage slew rate settings for the Etal-A transformer rectifier board.

The THD data for the Etal–B transformer figure 4.5 shows a slight decrease in THD, as the slew rate setting is varied from 800ns to 600ns. The peak THD level occurs from 400ns to 500ns. At a slew rate setting of 900ns the THD increases considerably to peak at 68.6%% and is 4.6% more than the Aerostanrew (mod1) transformer rectifier board.



Figure 4.5 Total harmonic distortion as a percentage versus the voltage slew rate setting. These measurements were taken from the Etal-B transformer rectifier board.

4.7 Conducted harmonic emission data Aerostanrew (mod1) transformer

In this section the magnitude of the harmonic components in the output voltage are investigated. The fundamental switching frequency is 75.636 kHz when measured at the output (as shown in table 4.5) with the corresponding attenuation level in (dBm). Example results shown are for a slew-rate setting of 600ns. The harmonics recorded are from the 1st to the 10th harmonic.

Table 4.5 Conducted harmonic noise emission data for the Aerostanrew (mod1) transformer and rectifier board at a slew rate setting of 600ns

Frequency of harmonic	Harmonic magnitude (-dBm)	Marker
(kHz)		identification
75.636	-100.15	1
151.272	-108.99	2
226.909	-107.37	3
302.545	-118.16	4
378.181	-111.84	5
453.818	-121.09	6
^{2nd} breakpoint 528	-115.51	7
603.636	-126.3	8
679.272	-120.76	9
754.909	-121.14	10

A comparison of the magnitude of the switching frequency harmonics from table 4.5 are identified from the spectrum analyser data shown in figure 4.1(a) and (b). Based upon the first ten harmonics illustrated in figure 4.6, the magnitudes of even harmonics are higher when compared with the odd harmonics.



Figure 4.6 The Aerostanrew mod1 transformer rectifier board harmonics from the 2^{nd} harmonic through to the 10^{th} harmonic. Slew rate setting is 600ns.

This subject has been documented in [9]. The author explained that the active device, in this case the MOSFET, will produce odd harmonics whereas the Schottky rectifiers, with the two cascaded second order lowpass filters, will produce even harmonics. The magnitudes of the harmonics from the 1st to the 8th show a trend of gradual attenuation. When examined separately as odd and even harmonics, as in figure 4.6, the attenuation is linear as the frequency increases. As the slew rate setting is increased, the second break point frequency (where the slope changes from 20dB/decade to 40dB/decade) moves down the spectrum. This means that with longer slew times the 6th harmonics and above should be attenuated slightly more compared with shorter slew times.

Investigation of the graph in fig 4.7. using the Aerostanrew (mod1) transformer rectifier board reveals that by changing the slew rate setting from 400ns to 900ns makes a difference to the attenuation of the 7^{th} and 9^{th} harmonics. However, the

 1^{st} - 6th, 8th and 10th harmonics increase if the slew rate setting is increased to 900ns.



Figure 4.7 Variation of conducted harmonic noise emissions with slew-rate settings of 400ns, 800ns and 900ns. 1st to the 10th harmonic components are shown with the Aerostanrew(mod 1) transformer rectifier board in place.

4.8 Conducted harmonic emission data Etal-A transformer

As shown in table 4.6, the harmonic magnitude are recorded from the first to the tenth harmonic for a slew-rate setting of 600ns. The odd harmonics of the 7^{th} and 9^{th} have a higher magnitude than the even harmonics between 500kHz and 800kHz, figure 4.8.

Table 4.6 Conducted harmonic noise emission data for the Etal-A transformer and rectifier board at a slew rate setting of 600ns

Frequency of harmonic	Harmonic magnitude level (-dBm)	Marker
(kHz)		identification
75.636	-100.0	1
151.272	-108.18	2
226.909	-108.39	3
302.545	-112.01	4
378.181	-116.57	5
453.818	-111.98	6
^{2nd} breakpoint 529.454	-124.0	7
605.09	-117.0	8
680.727	-123.04	9
756.363	-122.48	10



Figure 4.8 The Etal–A transformer rectifier board harmonic magnitude from the 2^{nd} harmonic through to the 10^{th} harmonic, at a slew rate setting of 600ns.





The effect of voltage slew rate adjustment with the Etal -A transformer rectifier board is shown in figure 4.9. Analysis of figure 4.9 reveals that from the first to

the third harmonic the magnitude decreases. Also there is little difference in the magnitude of the harmonics when the slew rate is changed from 400ns to 900ns. Between the 4^{th} and 10^{th} harmonic the harmonic magnitudes are greater for a slew rate setting of 400ns compared to 900ns. with the exception of the 9^{th} harmonic. The slew-rate setting has a positive impact on the magnitudes of the harmonics.

4.9 Conducted harmonic emission data Etal-B transformer

The harmonic magnitudes are recorded from the 1^{st} to the 10^{th} harmonic for a slew rate setting of 600ns, Table 4.7. The magnitudes of the odd harmonics are higher than the even harmonics with the exception of the even 10^{th} harmonic, figure 4.10. The slew rate setting with the Etal -B transformer, and its effect on the output spectrum is shown in figure 4.11. Analysis of figure 4.11 using the Etal-B transformer rectifier board shows that by changing the slew rate setting from 400ns to 900ns reduces the magnitude of the 5th, 6th, 8th 9th and 10th harmonics.

Table 4.7 Conducted harmonic noise emissions for the Etal-B transformer rectifier board at a slew rate setting of 600ns.

Frequency of harmonic	Harmonic magnitude level (-dBm)	Marker
(kHz)		identification
75.636	-98.0	1
151.272	-108.12	2
228.363	-110.82	3
304.0	-109.75	4
379.636	-121.16	5
455.272	-112.2	6
^{2nd} breakpoint 532.363	-117.0	7
608.0	-115.56	8
685.09	-117.89	9
760.727	-125.6	10



Figure 4.10 Harmonic magnitude from the 2^{nd} harmonic through to the 10^{th} harmonic, at a slew rate setting of 600ns, for the Etal-B transformer rectifier board.



Figure 4.11 Variation of conducted harmonic noise emissions with slew-rate setting 1^{st} to the 10^{th} harmonic components are shown with the Etal-B transformer rectifier board.

4.10 Summary

From comparisons of the high frequency spectra with different slew-rate settings, it is found that the higher order harmonics from the 6^{th} to the 10^{th} are attenuated more as the slew rate setting is increased from 400ns to 900ns. This correlates with the expected frequency of the 2^{nd} breakpoint in the frequency spectrum that the trapezoidal switching waveform generates. Therefore, this particular voltage slew-rate limiting system has an impact on the higher order harmonics but little impact on attenuation of the 1^{st} to the 5^{th} harmonics.

The Aerostanrew transformer indicates the best low order to high order harmonic attenuation results when compared to that of both the Etal-A and Etal-B transformers. The decrease in harmonic magnitude as the slew rate setting is increased from 400ns to 900ns may well be influenced by transformer design and manufacture.

All total harmonic distortion results were extracted from full load conditions for all five DC output voltages. Throughout all these measurements the DC-DC converter was operated in the continuous mode of operation.



Figure 4.12 Comparison of THD for all three toroids versus the function of the slew rate setting.

From the figure 4.12, it can be seen that slew rate setting has a minimal effect on for the Aerostanrew transformer (mod1) THD. The Etal-B system displays the lowest THD of all of the three systems when operated between 600ns and 800ns slew rate setting.

From the experimental data, it is found that the higher order harmonics from the 5^{th} to the 10^{th} are attenuated more as the slew rate setting is increased from 400ns to 900ns. Therefore, the voltage slew-rate limiting system implemented here will have an impact on the higher order harmonics but have no impact on attenuation levels for the lower order harmonics from the 1^{st} to the 4^{th} harmonics. The majority of the attenuation is a result of the four orders of filter between the secondary full-wave rectifier and the load, but the slew rate setting does have a positive impact on the odd harmonics in particular.

Chapter Five

5.1 Conclusions and Recommendations

This research provided an opportunity to assess four candidate low voltage DC bias supplies for the CCD-based IM modules located on the optical platform of the Gaia Satellite.

The supplies considered were:

- (i) an output drive H bridge
- (ii) a quasi resonant square wave zero voltage switch
- (iii) a charge pump
- (iv) a gate drive slew control.

From the literature review of each of the four, the slew rate control mechanism was selected based on the merits of low switching loss in the MOSFET and low core losses of the transformer. A further criterion was that the dc bias supply would provide ultra low conducted harmonic emissions when switching in the steady state condition.

The essential part of the research was to then assess the compromise between conduction, turn on and turn off losses of the MOSFET and the noise at the output. A new winding technique for the multiple output transformer was assessed that would furnish low ferrite core and copper losses and lower the magnitude EMI emissions due to the properties of the Mn-Zn ferrite core. The dc bias supplies have to provide a mixture of low voltage and high voltage outputs that are accurate and stable for all conditions of capacitive loading. High density packaging into a small size for a space environment was also considered during the design.

The chosen experimental (x2) buck derived push pull circuits' variant of a voltage slew control circuit was designed and measured while examining the impact of voltage slew rate setting on the device losses.

The Aerostanrew (mod 1) transformer exhibits the lowest total energy losses with a slew-rate setting of 400ns. With a lower slew rate setting, the total losses increase with this transformer.

The Etal -B transformer exhibits the next lowest energy losses at a slew-rate setting of 400ns. This energy loss increases at a higher slew rate setting of 900ns.

It is clear that the slew rate setting has a considerable effect on the MOSFET device losses.

At the second breakpoint frequency and a slew rate at 600ns the Etal-A transformer has the lowest magnitude of conducted harmonic emissions. With the Etal-B transformer there is a slightly higher emission. For the same conditions, the Aerostanrew transformer emissions are slightly higher than the Etal-B transformer. Investigating a compromise between noise and MOSFET energy losses, it is worthwhile noting that seventeen of these DC-DC converters can be enabled to operate the complete system CCD loads. This means that the total converter energy losses become more important to reduce than the slightly different measured noise levels between all three transformers.

Simulation and practical results indicate that this DC-DC converter has very clean switching waveforms and yields impressive noise levels. It also has very good closed loop regulation over the whole input voltage range. The empirical results quoted offer 80% conversion efficiency which is reasonable for such a low power converter (3W).

5.2 Contribution of the Author

Chapter 3 discussed the impact of voltage slew-rate on the total switch losses. When compared with both Etal transformers, the Aerostanrew transformer displays lower switching losses and this is attributed to the winding technique of individual primary layers interleaved with the secondary windings. The Skein technique used also results in a more effective flux linkage between windings. This leads to lower leakage inductance $L_{(k)}$ and lower interwinding capacitance C_{dis} both of which reduce the turn-on and turn-off losses in the primary switching device. This results in improved overall system efficiency.

From the experimental data in Chapter Four, it is found that the higher order harmonics from the 5th to the 10th are attenuated more as the slew rate setting is increased from 400ns to 900ns. Therefore, the voltage slew-rate limiting system implemented here will have an impact on the higher order harmonics but have no impact on attenuation levels for the lower order harmonics from the 1st to

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the 4th harmonics. The majority of the attenuation is a result of the four orders of filter between the secondary full-wave rectifier and the load, but the slew rate setting does have a positive impact on the odd harmonics in particular.

The Aerostanrew transformer displays the lowest noise output when compared to that of both the Etal-A and Etal-B transformers at 900ns. The decrease in harmonic magnitude as the slew rate setting is increased from 400ns to 900ns may well be influenced by transformer design and manufacture.

All real time total harmonic distortion results were extracted from full load conditions for all five DC output voltages. Throughout all these measurements the DC-DC converter was operated in the continuous mode of operation.

5.3 Suggestions for further research and development into low harmonic noise waveforms

Primary switching waveforms can be described by mathematical equations [9], and each waveform has it own connection to the peak current or voltage of the generated waveform and Fourier coefficients. It may be possible to generate a hyperbolic tangent shaped as a tan H waveform in an open loop system. The formula is expressible in terms of the exponential function.

This type of hyperbolic tangent waveform can be used to provide ultra low conducted noise. An algorithm has been written and simulated in matlab to provide an insight into its theoretical performance. From a practical perspective it would require two stages (i) to provide an input waveshaping control and (ii) a gate drive that would provide the necessary output current into the load. The new concept would be to vary the slew rate of the hyperbolic tangent using a digital waveform sythesiser.

Comparing the results with the trapezoidal waveform would contribute to our understanding of the conducted noise mechanisms. Also since this thesis was Chapter Five

written two new types of advanced ferrite materials have emerged with improved ferrite core losses. These could be used to measure the losses in this experiment.

The reverse recovery charcateristics of the rectifiers also have an impact on the noise generated within the converter. A recognised method of measurement would be used to determine the di/dt effects, as this is considered a prominent source of high frequency noise when mutiple isolated full wave rectifiers are used.

Another potential research theme would investigate techniques that remove the need for 4 orders of filtering at the output. These techniques may address the main sources of noise that are generated within the primary circuit they are: (i) the power MOSFET and (ii) the primary winding of the transformer A futher prerequisite of low noise is the input energy storage capacitor, as this capacitor provides the current required by the converter when operating in the steady state. The bandwidth of the input energy storage capacitor can be less than the operating switching frequency.

It is clear that there are many potential further research themes that can be undertaken and that this work makes an important contribution to the area of lownoise power supplies for space application of CCD arrays.

Appendix A1.1

Circuit Diagram of the final revision (X3). Push Pull topology. Continuous conduction mode, illustrating the four very low drop out micropower low linear regulators. The output noise spectrum is less than $1 \mu V \sqrt{Hz}$ between 10Hz and 100kHz for each regulator.

B1.1 Spectrum Analysis Data for different settings of the Voltage Slew Rate.

B1.2 Spectrum Analysis Data

Table B1.21 of measured conducted harmonic emissions at the output of the Aerostanrew transformer (mod1) rectifier board. This is for different settings of the voltage slew rate.

	Slew rate					
Harmonics	400ns	500ns	600ns	700ns	800ns	900ns
(-dBm)						
1st	-100	-100	-100	-100	-100	-100
2	-109	-109	-109	-109	-109	-110
3	-108	-108	-107	-107	-107	-107
4	-118	-118	-118	-118	-118	-119
5	-113	-111	-112	-113	-113	-114
6	-125	-122	-121	-121	-120	-119
7	-114	-116	-116	-116	-118	-120
8	-125	-124	-126	-126	-124	-123
9	-116	-118	-121	-127	-132	-128
10th	-127	-127	-124	-122	-120	-119

B1.3 Spectrum Analysis Data

Table B1.31 of measured conducted harmonic emissions at the output of the Etal - A transformer rectifier board. This is for different settings of the voltage slew rate.

	Slew rate					
Harmonics	400ns	500ns	600ns	700ns	800ns	900ns
(-dBm)						
1st	-98	-98	-100	-100	-100	-100
2	-108	-108	-108	-108	-107	-107
3	-107	-106	-108	-108	-108	-108
4	-109	-108	-112	-112	-112	-113
5	-111	-112	-117	-117	-121	-127
6	-109	-109	-112	-113	-113	-114
7	-115	-118	-124	-133	-127	-120
8	-111	-112	-117	-119	-122	-123
9	-121	-127	-123	-118	-117	-114
10th	-114	-118	-122	-124	-128	-124

B1.4 Spectrum Analysis Data

Table B1.41 of measured conducted harmonic emissions at the output of the Etal - B transformer rectifier board. This is for different settings of the voltage slew rate.

	Slew rate					
Harmonics	400ns	500ns	600ns	700ns	800ns	900ns
(-dBm)						
1st	-98	-98	-98	-100	-100	-100
2	-109	-108	-108	-107	-106	-105
3	-109	-110	-111	-110	-112	-109
4	-107	-107	-110	-110	-110	-109
5	-116	-118	-121	-126	-127	-126
6	-110	-110	-112	-114	-115	-115
7	-114	-117	-116	-124	-120	-115
8	-113	-115	-116	-126	-127	-120
9	-117	-118	-118	-117	-118	-113
10th	-118	-130	-126	-119	-116	-115
C1. The Magnetic Design of the Multiple Output Push Pull Toroid Transformer.

In the magnetic design of the multiple output toroid transformer, the buck-derived push pull topology controls B and H in two quadrants of the BH hysteresis curve identified as (1 and 3) in Figure C.1 below.



Figure C.1 The flux density versus Idc + ΔI when operating in the continuous mode.

In graph C.1, the Y axis is the flux density and Bsat is proportional to the core area. Since the mode of operation is in the continuous mode, the inductance is made larger which results in lower peak currents at the end of the cycle. Each conduction cycle is 26.5μ Sec or 37.5 kHz of the primary switching cycle.

The flux excursion has a variation from B+ to B- which allows maximum usage of the Mh Zinc toroid transformer. The X axis represents the magnetic field intensity which is proportional to the ampere turns. The hysteresis curve for push

pull operation manifests itself to be slim in nature of operation when varying from the B+ quadrant to the B- quadrant. Also by making the area of the hysteresis curve slim in nature the core losses will be less at the lower switching frequency of 37.5 kHz. Increasing the switching frequency will increase the core losses.

A maximum value for B_{dc} and B_{ac} is chosen to prevent saturation of the core. For a more detailed explanation of these hysteresis curves operating over an extended temperature range and their corresponding effects, see the hysteresis curves, Figure C.2 and C.3 for the F grade and P grade ferrite material as outlined for this detailed research [24].



Figure C.2 The F grade material hysteresis B-H loop at 25° C and 100° C . (Sourced from McLyman).

F grade material was selected for both (mod1) and (mod 2) toroid transformers. The first step in the design process is to design the toroid transformer for a maximum duty cycle at the minimum dc input voltage +22Vdc. Measurement defined this duty cycle to be 38% for the Aerostanrew toroid transformer (mod1). The toroid transformer was designed to provide a constant volts second product because the duty cycle will decrease when the input dc voltage is incremented to the nominal voltage of +28vdc. This duty cycle then measured 22%.

The magnetics P grade material, which has a slightly higher Bsat than the F material, was used in the manufacture of the Etal-B transformer. P grade material has an initial permeability of (μ i) 2500.

The B and H hysteresis curve for the P ferite material is shown in C.3.



Figure C.3 The P grade material hysteresis B-H loop at 25°C and 100°C. (Sourced from McLyman).

Normally for symmetrical excitation of the push pull toroid, the maximum intended flux density sweep is considered twice that for asymmetrical excitation. This is shown in figure C.1. From a practical perspective provision is made for unbalance when determining the operating flux density. In principle, the primary

reason for asymmetry is unequal conduction times or saturation voltages of the primary n-channel MOSFETS. To alleviate any potential flux imbalances and core saturation a peak-current mode control is used which places a current limit on the power switches.

This implies that this topology would provide a significant reduction in size. In order to provide a 3 watt output for all five output voltages it is necessary to mount all five secondary windings plus the split primary winding on to a 16mm air gapped toroid transformer. This is a unique feature of this tranformer when using all bifilar windings, as in the Aerostanrew (mod1) toroid transformer. The isolated output voltage is then governed by the turns ratio N. For example: Np/Ns then Vout = Ivin*(N)*28 (C.1)

$$N = 0.134$$

N = Vout + Vf/[2*duty cycle]*[Vin minimum - Isw*[Ron + Rsense](C.2)

The area of the core is 15.3mm² and the peak flux density will be:

N

$$\Delta B = \frac{50}{15.3^2} = 213 \,\mathrm{mT} \tag{C.3}$$

For the steady state conditions there will be a balance of flux density between negative and positive quadrants. One source of unbalance is unequal flux linkage between two halves of the centre tapped winding.

However, since the converter has current mode operation, this solves the unbalance problem. By monitoring the current in each of the push pull n-channel MOSFETS on a pulse by pulse basis, this forces alternate current pulses to have equal amplitude .

The selection of advanced ferrite Manganese Zinc properties for the toroid transformers is based upon the nature of the material that, in principle, exhibit high permeabilities at low frequency (usually < 500kHz) then gradually roll off as the frequency is increased. This can be plotted as series reactance versus the frequency, using 4 cycle log/log scale. Consider that the higher the permeability,

the lower the frequency where this break point roll off will occur. Inherent in this type of ferrite materials is that they exhibit very high losses at frequencies from 1MHz to 50MHz and up to 100MHz. This is one of the reasons for selecting a lower switching frequency of 76kHz.

Ferrites are known for having high resitivity features that can provide low ferrite core losses and low magnetic current for the operating switching frequency. A comparison study investigated innovative and advanced ferrite material and is shown in Table C.1 through to Table C.2.

Table C.1 Flux density parameters for four grades of ferrite material that identify the initial permeability and flux density.

Material (Mn-Zn) Toroid	Symbol	Unit	Magnetics F Grade	Magnetics P grade	Ferroxcube 3C95	Ferrox cube 3C96
Initial permeability μI (T=25°C)			3000 ±20%	2500 ±25%	3000 ±20%	2000 ±20%
Flux Density B H=1200 A/m F=10Khz@ °25C H=1200A/m F=10Khz @100°C	Bm	mT	490	500	530 410	500 440
Coercivity	Нс	Oe A/m	0.2 16	0.18 14		
Typical frequency Range	k	Hz	<1200	1300	100 to 400	25 to 500
Currie temperature Density(typical Value)	-	C Kg/m ³	>250 4800	>230 4800	≥215 4800	≥240 4800

Relative	Pv	Units	Magnetics	Magnetics	Ferrox-	Ferrox-
core			F grade	P grade	cube	cube
losses					3C95	3C96
(typical		mW/cm ³	90mW/cm ³ for	120 mW/cm ³	206mW	300mW
values)			a sinusoidal	for a sinusoidal		
25kHz,			waveform	waveform		

Table C.2 provides the relative core losses for the four grades of ferrite material. The details given above represent the manufacturers' specifications for advanced ferrites. It is an indication of core losses for mostly sine wave operation. The Ferroxcube specification did not furnish data on the type of waveform used to determine their core losses.

C1.1 The general winding characteristics of the Aerostanrew (mod1) toroid transformer.

Power transfer occurs in the toroid transformer when either switch is on; the core does not store energy and conducts current from the source. Another added feature of this topology is that the maximum power capability is twice that of a forward converter. The originality of the multiple output toroid transformer design is in the interleaving of the primary and the five, isolated secondary windings. Two of the secondary windings on the Aerostanrew toroid (mod1) use the Skeining method; on winding 2 and winding 4. Winding 2 is associated with +35Vdc rail and winding 4 is associated with the +6.5Vdc winding.

The secondary windings are evenly spaced in the same winding volume, as opposed to discrete secondary windings wound on top of each other.

In a conventionally-wound toroid the maximum turns/layer is limited by the inner diameter of the core. The maximum primary switching duty cycle of each driver in relation to the complete cycle, which consist of two periods when gate drive a and b are on, is shown in figure C.4 below.



Figure C.4 Channel 1 is the primary current on 100mA/division. Channel 2 is the gate voltage on 5V/division.

The voltage that appears across the second order LC filter has a peak value of the input voltage multiplied by the turns ratio from the primary to the secondary. This continues until the FET is turned off by the fixed frequency current mode PWM controller. There then must be a mandatory "dead time" when neither FET is conducting because it takes a finite length of time for the MOSFETS to stop conducting current.

In this case multiple outputs are achieved using the principle of galvanic isolation from the primary winding to the secondary winding. Each secondary winding is therefore isolated from each output winding. The topology most suited to this type of application is the push-pull topology which has been used extensively in satellite power conversion processing when more than one ouput is required. There is the drawback of high ripple and noise, using wave forms that have had, previously, very fast turn on and turn off times in order to achieve high system conversion efficiency.

C1.2 Operational considerations for the multiple output toroid transformer

Two choices of permeability were proposed on two types of advanced manganese and zinc [MnZn] ferrite toroid material which exhibit higher permeability [μ i] and high Bsat with minimum losses at high temperature. Magnetics F grade material provided the higher Curie temperature for operational conditions. High temperatures can be expected on a satellite space platform which can cause the ferrite molecular structure to be damaged. Other advanced ferrite materials by Ferroxcube were considered to gain information on core power loss. See tables C.1 through to C.2.

High isolation breakdown voltages are difficult to achieve on small toroid transformers. The insulation of the wire is effective to 500Vdc, providing the wire is wound single filar. If the wire is wound biflar this reduces the dc isolation voltage because of finite number of twists per mm. Therefore a single filar wound wire would meet most space applications for lower power applications. Copper wire information including wire tables are carefully outlined in reference to push-pull calculations [24].

The wire used was grade 2, polyurethane, enamelled, round copper wire that is referenced to IEC317-4 class F Part 20 and part 51 [BSEN60317]. Since separate secondary windings are used, it will be possible to meet IEC 950 criteria and gain approval for this type of toroid design. Measurements of primary and secondary inductance, including the leakage, inductance and interwinding capacitance, are achieved in accordance to BS9720.

For the measurements identified in this report, the characteristic initial permeability was selected to be $[\mu i]3000 \pm 20\%$ The Curie temperature of this ferrite toroid is >250 °C and is categorised as F grade material by Magnetics and has a A ℓ 1650•10⁻⁹

Using the P grade Magnetics ferrite, the Etal-B toroid transformer initial permeability is (µi)2500 \pm 20% and has a A ℓ 1375•10⁻⁹

C1.3 Ferrite core losses and magnetic current calculations when comparing different ferrite materials.

Toroid transformer losses of approximately 3% will result when using the F grade ferrite. It should also be noted that since the P grade ferrite material has a lower permeability than F grade it is expected that a higher magnetising current and hence higher power losses will be incurred. The Curie temperature for this P grade material is $>230^{\circ}$ C. The measured power loss is determined by the volume of the ferrite and the flux in the core. By minimising the volume for a specific flux the power loss will be less.

Hence the power loss is proportional to the volume for a given flux density.

$$B = \mu \bullet H \text{ and} \tag{C.4}$$

$$\mu = \frac{B}{H} \text{ and } \mu = \frac{\Delta B}{\Delta H}$$
(C.5)

The higher permeability increases the inductance per turn.

The core loss equation for the F and P grade material is referenced to the Magnetics data in section 3.9.

Pc loss = mW/cm³
= 0.0717
$$(f(kHz))^{1.72} * (Bac)^{2.66}$$
 (C.6)

$$= 0.0717 (37.5)^{1.72} * (1.47)^{2.66}$$
(C.7)

$$= 15.27 \text{mW/cm}^3$$
 (C.8)

The core loss equation for the P grade material is :- (C.9)

Pc loss = mW/cm³
=
$$0.158 * (37.5)^{1.36} * (1.47)^{2.86}$$
 (C.10)

$$= 34 \text{ mW/cm}^3$$
 (C.11)

In conclusion using the P grade material increases the core loss by a factor of 2.2. Ferroxcube provided empirical test data on core losses for sixteen toroid samples using the advanced 3C95 ferrite material. A maximum core loss of 479mW/cm^3 at a T^{*a*} $25(^{\circ}C)$ was recorded. When measured at T^{*a*} $100(^{\circ}C)$ the core loss was less and measured 422mW/cm^3 . This was for different conditions of operation. The frequency was 100kHz with Bac = 200mT, Ae =12.29, Le = 34.97.

The toroid transformer is designed to furnish a constant volt-second peak/ Δt product. This is because the duty cycle will decrease when the input voltage increases. This can be determined using the formula:

$$V_{\Delta t} = \Delta [Bsat * N * Ae] \tag{C.12}$$

Consider $V = N d \Phi / dt = N A_e dB / dt$

The operating flux density Bsat = 0.129mT (C.13)

N= number of turns

Γ.

$$Ae = 0.153 cmsq \tag{C.14}$$

The I mag current for a push pull toroid is added on to the MOSFET peak current at turn on. This equation is defined below:-

Then the I mag current =
$$\frac{V \operatorname{Pr} \operatorname{imary peak} * \operatorname{Turn on}}{L \operatorname{Inductance of one split primary winding}}$$
(C.15)

Then for the I mag current =
$$\frac{28 * 5.7 * 10^{-6}}{5.32 \text{mH}} = 30 \text{mA}$$
 (C.16)

The mag current of 30mA represents 8% of the total primary peak current which is 386mA pk. This is for the Aerostanrew (mod1) toroid where $\mu i = 3000$ and Vin nominal is +28Vdc. It is important to compare this result with the ETAL-B toroid that has a different initial permeability $\mu i = 2500$. The current waveform using this toroid at turn on is 6.68 μ S.

Using the formula in (C.15) it is then possible to determine the Imag current for the ETAL-B toroid:

$$\frac{28*6.68*10^{-6}}{4.8\text{mH}} = 39\text{mA} \tag{C.17}$$

Then the mag current of 39 mA represents 9.75% of the total primary peak current which is 400mA pk. This measurement is for the Etal-B toroid where $\mu i = 2500$ and Vin nominal is +28Vdc.

Then
$$\Delta \text{Imag} = \frac{\Delta \text{VTon}}{\text{Lmag}}$$
 (C.18)

$$\Delta VI = Lmag \frac{\Delta i}{\Delta t}$$
(C.19)

C1.4 Full wave rectifier, worst case voltage drop.

[2x] 0.65 (for+35Vdc) [2x]0.78 (for +15Vdc) [2x]0.71 (for+6.5Vdc) [2x]0.23 (for -6.0Vdc) [2x]0.26 (for +3.3Vdc)

C1.5 Steady state operational duty cycle.

Duty cycle min δ (0.21)

Duty cycle max δ (0.38)

Initial Permeability (Ui) \pm 3000 for Aerostanrew toroid (mod1) and Etal-B toroid Ae operating Flux density Bm (129mTesla) when Vin = +28Vdc.

Wdg #	Turns mod(1)& mod(2) bifilar	Wire mod (1) od mm single	Wire mod (2) od mm bifilar	Length (mm) plus bifilar if used on (mod2)	ac resistance of wire (mod1) across each wdgs (Ω)	Notes on measurements for Aerostanrew toroid (mod 1)
1a	14 + 14	0.25	0.375	350 + 350	15.56	Measured across pins 1 and 3
2	37 + 37	0.1	0.2	760 + 760	31.53	
3	18 + 18	0.25	0.5	400 +	9.7	
4	9 + 9	0.1	0.2	225	3.62	
5	8 + 8	0.25	0.5	200	2.24	
6	5 + 5	0.315	0.63	150	0.82	
1b	13 + 13	0.25	0.375	325		

Table C.3 Wire gauge details of all primary and secondary windings.

C1.6 Primary winding copper losses

The formula used to determine the primary copper losses for the Aerostanrew

mod 1 toroid transformer is $Pc(w) = (IPeak * \sqrt{2 * \delta})^2 * R$ (C.20)

Where δ = the duty cycle which is 0.215 at Vin nominal +28Vdc.

R is the dc resistance of the winding, in this case the total primary resistance of 1a and 1b which is 15.56 ohms

By calculation
$$Pc(w) = (386 * 10^{-3} * \sqrt{2 * 0.215})^2 * R$$
 (C.21)

Therefore the primary winding loss of wdg1a and wdg1b will be 996mW. (C.22)

Appendix C The Magnetic Design of the Multiple Output Push Pull Toroid Transformer.



Figure C.5 The Aerostanrew mod1 toroid transformer rectifier board is using the space-qualified Schottky full wave rectifiers and ultra fast switching diodes. This includes all load capacitors and load resistors attached to the (X2) PCB.

C1.7 Secondary winding copper losses.

The formula used to determine the secondary winding copper losses for the Aerostanrew mod toroid is explained in Table C.4.

Power loss of secondary wdgs	Load current I ² mA	Winding ac resistance Ω	Secondary wdg power loss in (mW)
Power loss of secondary wdg (2)	10	31.53	3
Power loss of secondary wdg (3)	80	9.7	62
Power loss of secondary wdg (4)	20	3.62	1.4
Power loss of secondary wdg (5)	100	2.24	22.4
Power loss of secondary wdg (6)	150	0.82	18.45
Total power losses for all secondary wdg's			107.25

Table C.4 Secondary windings copper losses.

To obtain the total core losses of this toroid in mW, this becomes the primary winding copper losses +secondary winding copper losses which is:

996 mW + 107 mW = 1103.25 mW (C.23)

C1.8 Temperature rise of the wound toroid transformer core.

A certain percentage of input power is lost and is converted to heat because of hysteresis and eddy currents induced into the core material. The power loss also includes the copper losses. There is a linear relationship between surface dissipation in watts/cm² versus ΔT = Temperature rise in Degrees °C. This convected and radiated heat was measured on the core of the Etal-B transformer using a Fluke infra–red probe, model 80T-IR. The digital temperature reached and then stabilised at +39°C. This was for an ambient temperature of 22.4°C.

The estimated calculation for temperature rise of the Etal- B toroid is given in the following formula:

Temperature rise (°C) =
$$\left[\frac{\text{Total Power Loss (mW)}}{\text{Surface area (cm}^2)}\right]^{0.833}$$
 (C.24)

To determine the total power loss in (mW) which is equal to the copper losses + the core loss, using the result of equation (C.8), the core loss is (15.27mW/cm^3)

This equates to
$$(1103.25 \text{mW}) + [(15.27 \text{mW/cm}^3)] * 0.85$$
 (C.25)

$$(1103.25\text{mW}) + (12.98\text{mW}) = 1116.23\text{mW}$$
 (C.26)

The surface area equation A_t of the wound toroid is:

$$A_{t} = \left[\frac{\pi \text{ OD}^{2} \text{ wound.}}{2}\right] + \left[\pi \text{ OD wound } * (\text{Ht core + OD wound - OD core})\right](C.27)$$

Toroid	Transformer	Toroid wound OD (mm)	Toroid	wound	height
manufacture	r		(mm)		
Aerostanrew	(mod1)	18	6		
Etal-A		18	6.5		
Etal-B		18	6.5		

Table C.5 Dimensions of all three transformers with populated windings.

From Table C.5 surface area =
$$\left[\frac{3.14*(18)^2}{2}\right] + [3.14*18]*[6*18] - (18)$$
 (C.28)
= 508.68 + 56.52 * 90

$$A_t = [508.68 + 5087] = 5596 \text{mm}^2 \text{ or } 55.96 \text{cm}^2$$
 (C.29)

Therefore temperature rise (°C) =
$$\left[\frac{1116.23(\text{ mW})}{55.96(\text{CM})^2}\right]^{0.833}$$

= 20°C. (C.30)

C1.9 Skin Depth Calculation

The definition of skin depth δ is the distance from the outside surface of the conductor when the current density declines to 1/e or 37% of its value at the surface. Skin effect will cause an increase in the ac resistance of the conductor when compared to the dc resistance at the primary switching frequency used in this dc/dc converter.

Temperature correction factors are also applied to the copper wires of concern in order to find the dc resistance at specific temperatures from -55° C to $+125^{\circ}$ C.

The skin depth is considered to be the radius of the conductor wire where the current will flow. The primary switching frequency is 37.5kHz.

Using the equation for the skin depth, calculation is as follows:-

$$\delta = \frac{6.61}{\sqrt{37.5 * 10^3}} \qquad [cm] \tag{C.31}$$

Hence $\delta = 0.0341$ [cm] (C.32)

Consider the wire area formula:-

Wire_{*a*} =
$$\pi * (\delta)^2 [cm]^2$$
 (C.33)

Wire_{*a*} = 0.00365
$$\left[\text{cm}^2 \right]$$
 (C.35)

Selecting a preferable wire size to the result in (C.35), from Table 9.1 in reference [24].

The practical wire size in AWG = 22 (C.36)

Therefore
$$A_{W(B)} = 0.00324 \left[cm^2 \right]$$
 (C.37)

And
$$\mu\Omega/cm = 531.4$$
 (C.38)

Therefore
$$A_W = 0.00386 \left[\text{cm}^2 \right]$$
 with insulation (C.39)

C2.0 Output impedance of the regulated +3.3Vdc output

There is a need to determine the output impedance (Z), as this dc output voltage provides the Vdd voltage to the PEM cell via the 30cm 22AWG power interconnect cable.

$$Z = \frac{\text{Vnl} - \text{Vmaxl}}{\text{Imax}} \tag{C.40}$$

Vnl = Output voltage on no load.

Vmax load = Output voltage on full load.

Imax load = Full rated current.
Therefore
$$Z = \frac{3.295 - 3.286}{154 * 10^{-3}}$$
 Z = 58m Ω . (C.41)

Appendix D1. Efficiency Assessment of the Toroid Transformers

The dc/dc converter was tested in the continuous conduction mode. This uses minimum resistive load to obtain the maximum load requirement on the controlled regulated +3.3V output. The output of the +3.3 is tested with a reservoir capacitor of 300μ F that is placed across the resistive load. All other non-regulated loads at the output of the full wave rectifiers have resistive loads with parallel reservoir capacitor loading. This is to obtain the maximum current level at the output of the full wave rectifiers as identified on page 16 and figure 1.2, including page 17.

Input and ouput powers are listed in Table D.1 for the power supply with the Aerostanrew and the Etal_B transformer. It is necessary to compare the primary and secondary power levels as these two transformers have different permeabilities and A_L values.

Table D.1 Measured input and output powers and overall efficiency for the power supply with Aerostanrew (mod1) and Etal-B transformers.

Transformer	P(In) W	Sec/Pout wdg 2	Sec/Pout wdg3	Sec/Pout wdg4	Sec/Pout wdg5	Sec/Pout wdg6	P(out) total(W)	Efficiency %
Aerostanrew (mod1)	4.8	0.40	1.7	1.06	0.19	0.5	3.85	80.2
Etal -B	5.0	0.43	1.9	0.93	0.21	0.5	3.97	79.4

The power dissipation for the system with the Aerostanrew (mod1) transformer is:

$$(Pout - Pin) = (3.85 - 4.8) = 0.95$$
 watts. (D.1)

And for the system with the Etal -B transformer the power dissipation is:

$$(Pout - Pin) = (3.97 - 5.0) = 1.03$$
 watts. (D.2)

Comparing the conversion efficiency for the system with the Aerostanrew (mod1) transformer and the Etal –B toroid transformer:

$$(80.2\% - 79.4\%) = \Delta 0.8\%) \tag{D.3}$$

And the equivalent difference in power loss is:

$$(0.95 - 1.03) = \Delta 0.08$$
 Watt (D.4)

The system with the Aerostanrew (mod1) transformer has a slightly improved efficiency and lower losses when compared with the Etal-B transformer.