University of Strathclyde
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Medium-Voltage PWM Indirect Vector Controlled Induction Motor Drive with a Long Motor Feeder

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Dedication

This thesis is dedicated to my parents, who have raised me to be the person i am today. Also, to my wife Marwa and my daughter Jomana, who offered me unconditional love and support throughout my whole life. You have been with me every step of the way, through good times and bad. Thank you for everything. I love you all!

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Abstract

This thesis studies two types of medium-voltage (MV) vector controlled PWM induction motor drives for long motor feeder applications, namely voltage source and current source based drives. As rectifiers and inverters are the main elements in any drive system, both are investigated, but with more emphasis on the inverter side.

MV PWM current source rectifiers (CSR) usually use selective harmonic elimination as a modulating strategy which provides good harmonic reduction at a low switching frequency. The rectifier performance does not meet the IEEE 519 regulation concerning harmonics injected into the supply current. Two solutions are presented. First, line side passive filters for harmonic mitigation and power factor improvement. Second, shunt active power filters based on *p-q* theory, with a step-down high-frequency transformer. The presented solutions are compared to highlight their features and limitations. Several topologies can be used for PWM CSRs. A detailed study of the selection criteria for PWM CSR semiconductors is presented based on losses, physical size, and number of series devices.

Utilization of a PWM voltage source inverter (VSI) drive system in long motor feeder applications leads to motor terminal over-voltage problems. Surge filters are used to mitigate this phenomenon. Among the various types of filters, the motor terminal *RC* filter and the inverter output *RLC* filter are common. A detailed investigation is presented of the effects of these filters on the VSI drive system. PWM current source inverter (CSI) drive systems are characterised by their motor friendly voltage behaviour and controlled short circuit capabilities. Therefore, a proposed indirect vector controlled PWM CSI drive is presented for long motor feeder applications. Performance comparison between PWM VSI and CSI drive systems for long motor feeder applications is performed to clarify features and limitations of each system. Motor voltage is needed for speed estimation but measurement of voltage/speed is impractical for long motor feeder drives. A model reference adaptive system speed estimator is proposed with a novel remote motor voltage calculator that depends on the inverter voltage and feeder parameters. Offset and drift problems that occur during the flux estimation process are solved by a proposed DC-offset eliminator.

List of Symbols

C	CSI output capacitive filter	F
C_{c_a}, C_{c_b}, C_{c_c}	Feeder capacitances per phase	F
C_{c_d}, C_{c_q}	Feeder capacitances in *d-q* frame	F
C_f	Filter capacitive element	F
D_{abc}	CSI complimentary pulse distributor signals	-
$E_{off\_switching}$	Turn-off switching loss energy	J
$E_{on\_switching}$	Turn-on switching loss energy	J
$E_{rec\_switching}$	Recovery switching loss energy	J
e_{speed}	Error between actual and reference speed signals	rpm
f_h	Nearest harmonic frequency in CSR passive filter design	Hz
f_r	CSR passive filter tuned frequency	Hz
$i^e_{c\_ds}$, $i^e_{c\_qs}$	CSI capacitor current in *d-q* rotating reference frame	A
i^*_{DC}, i_{DC}	DC-link current reference and actual respectively	A
$i^e_{m\_dr}$, $i^e_{m\_qr}$	Motor rotor current in *d-q* rotating reference frame	A
$i^e_{m\_ds}$, $i^e_{m\_qs}$	Motor stator current in *d-q* rotating reference frame	A
$i^{e*}_{m\_ds}$, $i^{e*}_{m\_qs}$	Motor stator reference current in *d-q* rotating reference frame	A
$i^s_{m\_ds}$, $i^s_{m\_qs}$	Motor stator current in *d-q* stationary reference frame	A
I_{on_state}	Steady-state current after semiconductor turn-on	A
i_{ra}, i_{rb}, i_{rc}	Rectifier input three phase currents	A
$i_{r\alpha}$, $i_{r\beta}$	Rectifier input currents in stationary frame	A
$i^{e*}_{s\_ds}$, $i^{e*}_{s\_qs}$	CSI reference input current in *d-q* rotating reference frame	A
I_{turn_on}	Turn-on semiconductor transient current	A
K_{p_est}, K_{i_est}	Speed estimator PI controller constants	-

K_{p_speed}, K_{i_speed}	Motor speed PI controllers constants	-
K_{p_d}, K_{i_d}	Motor current *d*-axis PI controller constants	-
K_{p_q}, K_{i_q}	Motor current *q*-axis PI controller constants	-
l_c	Feeder length	km
L_{c_a}, L_{c_b}, L_{c_c}	Feeder inductance per phase	H
L_{c_d}, L_{c_q}	Feeder inductance in *d-q* frame	H
L_{DC}	DC-link inductance	H
L_{ds}, L_{qs}	Motor stator inductance in *d-q* frame	H
L_{dr}, L_{qr}	Motor rotor inductance in *d-q* frame	H
L_f	Filter inductance	H
L_m	Motor mutual inductance	H
L_r	Motor rotor inductance	H
L_s	Motor stator inductance	H
M_a	PWM CSR modulation index	-
m_{abc}	PWM VSI/CSI three-phase modulating signals	-
m_d^e, m_q^e	PWM VSI/CSI modulating signals d-q rotating reference frame	-
N_r^*, N_r	Motor reference and actual speed signals respectively	rpm
N_{r_est}	Motor estimated speed signal	rpm
P	Motor number of pair poles	-
$P_{conduction}$	Semiconductor conduction loss	W
$P_{off\_switching}$	Semiconductor turn-off loss	W
$P_{on\_switching}$	Semiconductor turn-on loss	W
$P_{rec\_switching}$	Semiconductor recovery loss	W
p	Differential operator	-
p_{load}, q_{load}	Load total active and reactive power	W, VAr
$\bar{p}_{load}$, $\bar{q}_{load}$	Load active and reactive power (fundamental)	W, VAr

$\tilde{p}_{load}$, $\tilde{q}_{load}$	Load active and reactive power (harmonics)	W, VAr
R_{c_a}, R_{c_b}, R_{c_c}	Feeder resistance per phase	Ω
R_{c_d}, R_{c_q}	Feeder resistance in *d-q* frame	Ω
R_f	Filter resistance	Ω
R_r	Motor rotor resistance	Ω
R_s	Motor stator resistance	Ω
S_1 - S_6	VSI/CSI PWM signals	-
s	Speed slip	-
S_d	CSI mapping circuit complimentary pulse signal	-
T	Motor developed torque	Nm
T^*	Motor torque reference from speed controller	Nm
$t_{critical}$	Critical rise time determining motor terminal over-voltage	s
V_c	CSI capacitor voltage	V
V_{DC}	DC-link voltage	V
V_{OZ}	Inverter common-mode voltage	V
V_{ZG}	Rectifier common-mode voltage	V
v_a, v_b, v_c	Three phase utility input voltage	V
v_α, v_β	Utility input voltage in stationary frame	V
v_{inv_a}, v_{inv_b}, v_{inv_c}	Inverter three phase voltage	V
$v^e_{inv\_ds}$, $v^e_{inv\_qs}$	Inverter voltage in *d-q* rotating reference frame	V
$v^s_{inv\_ds}$, $v^s_{inv\_qs}$	Inverter voltage in *d-q* stationary reference frame	V
v_{m_a}, v_{m_b}, v_{m_c}	Motor stator three phase voltage	V
$v^e_{m\_ds}$, $v^e_{m\_qs}$	Motor stator voltage in *d-q* rotating reference frame	V
$v^s_{m\_ds}$, $v^s_{m\_qs}$	Motor stator voltage in *d-q* stationary reference frame	V
$v^e_{m\_dr}$, $v^e_{m\_qr}$	Motor rotor voltage in *d-q* rotating reference frame	V

V_{on_state}	Semiconductor on-state voltage	V
X_c	Filter capacitive reactance	Ω
X_l	Filter inductive reactance	Ω
z_o	Feeder characteristic impedance	Ω
α–β	Stationary frame	-
β	CSI SHE gating instants	°
γ	CSR passive filter design constant	-
λ^e_{ds}, λ^e_{qs}	Motor stator flux linkage in *d-q* rotating reference frame	Wb
λ^e_{dr}, λ^e_{qr}	Motor rotor flux linkage in *d-q* rotating reference frame	Wb
λ^s_{dr}, λ^s_{qr}	Motor rotor flux linkage in *d-q* stationary reference frame	Wb
$\lambda^{s/}_{dr}$, $\lambda^{s/}_{qr}$	Motor rotor flux linkage in *d-q* stationary reference frame (generated from rotor model based on estimated speed)	Wb
θ_e	Vector control transformation angle	°
σ	Motor leakage coefficient	H
ω_e	Synchronous angular speed	rad/s
ω_{est}	Estimate motor angular speed	rad/s
ω_r	Motor angular speed	rad/s
ω_{slip}	Motor angular speed	rad/s
Γ_L	Load reflective coefficient	-

List of Abbreviations

AC	Alternating current
APF	Active power filter
ASD	Adjustable speed drive
CHB	Cascaded H-bridge multilevel inverter
CSI	Current source inverter
CSR	Current source rectifier
DC	Direct current
DSP	Digital signal processor
EMC	Electromagnetic compatibility
FC	Flying capacitor multilevel inverter
FFT	Fast Fourier transform
GCT	Gate commutated thyristor
GTO	Gate turn off thyristor
HVIGBT	High voltage insulated gated bipolar transistor
IEC	International electrotechnical commission
IGBT	Insulated gated bipolar transistor
LC	Inductive-capacitive rectifier input filter
LCI	Load commutated inverter
MRAS	Model reference adaptive system
MV	Medium voltage
NPC	Neutral point clamped multilevel inverter
pf	Power factor
PWM	Pulse width modulation
RC	Motor terminal resistive-capacitive surge filter
RLC	Inverter output resistive-inductive-capacitive surge filter
SCR	Silicon controlled rectifier
SGCT	Symmetrical gate commutated thyristor
SHE	Selective harmonic elimination
SPWM	Sinusoidal pulse width modulation
SVM	Space vector modulation
THD	Total harmonic distortion
THIPWM	Third harmonic injected pulse width modulation
TPWM	Trapezoidal pulse width modulation
VSI	Voltage source inverter
VSR	Voltage source rectifier

Preface

High-power medium-voltage drives are often employed in industries like steel, paper production, oil extraction, and waste water treatment. In many applications, the motor is remotely fed via a long feeder. Among such applications are fans for underground mines and electric submersible pumps. Voltage source and current source based MV drive systems are alternatives and competitors. This research compares the performance of these drive systems for long motor feeder applications. The drive configuration, rectifier/inverter, is studied, with more emphasis on the inverter side.

The thesis is presented in eight chapters:

Chapter one surveys MV drive systems, considering the main drive elements, rectifiers and inverters. Different MV rectifiers/inverters topologies are discussed with the converter topologies used in this thesis highlighted.

Chapter two starts with the theory and operation of the PWM CSR. The rectifier topology and PWM techniques are also considered. Even with harmonic minimization PWM techniques, these rectifiers do not comply with the IEEE 519 regulation. Hence, the theory, design, and performance analysis of line side passive filters for the PWM CSR are studied in detail. A similar study is presented for the active power filter alternative. Then the performance of both filter techniques, passive and active, is compared. A survey on different passive filter techniques for the PWM CSR is also presented.

Chapter three presents three different semiconductor device alternatives suitable for the PWM CSR. A comparison of losses, physical size, and number of series devices used for the three alternatives is presented with a detailed study of loss calculations. The constant-voltage switching energy characteristic curves, in practical data sheets, for voltage source based converters, are adapted to suit varying voltage applications like the CSR.

Chapter four describes the vector controlled PWM voltage source drive system. Motor terminal over-voltage problems with long motor feeders caused by VSIs are addressed. Two filter techniques are studied to overcome these problems, namely, a motor terminal *RC* filter and an inverter output *RLC* filter. The design steps and performance analysis for each filter topology are presented. Then a comparison of the effects of the two filter networks on a vector

controlled drive is undertaken. Feeder length effects on filter losses, DC-link current and voltage regulation are also investigated.

Chapter five studies a MV drive with current source based vector control. The chapter starts with a general description of the vector controlled PWM current source drive, with emphasis on the difference between this system and the voltage source system. Then direct vector control, common for this drive, is described and its performance is evaluated. Basic indirect vector control is considered with its major drawbacks highlighted. To overcome the drawbacks, a modified indirect vector control technique is proposed which is supported by two case studies, direct connection to the motor and connection via a long feeder.

Chapter six compares between the voltage and current source vector controlled PWM drives in long motor feeder applications. Effects on important electric quantities like motor voltage, motor current, and common mode voltage are clarified. Also, the effects on mains power factor and supply current are addressed. Issues related to the inverter topology, utilization factor, feeder insulation, and length capabilities are also discussed. Filter requirements, losses, and efficiency are investigated.

Chapter seven starts with the measurement requirements for a practical sensorless long motor feeder drive. The proposed MRAS technique is illustrated for speed estimation with a novel DC-offset eliminator when calculating flux components. A remote motor voltage calculator is proposed which calculates the motor terminal voltage from the inverter voltage and feeder parameters. The proposed sensorless drive is investigated at start up and loading conditions to validate its robustness.

Chapter eight presents the conclusions, the author's contribution, and possible future research.

CHAPTER ONE:

Introduction

High power drives have been extensively researched in the past few decades. Power semiconductor developments have encouraged rapid progress in the medium-voltage drives field. MV high-power converters are used in industry for speed control, torque control, and efficiency improvement issues. Heavy industries like waste water treatment, paper production, metal rolling, and in underground mines are examples of MV applications. In this chapter a survey of MV drives is presented with emphasis on the topologies used within this thesis.

1.1 MV Drives Topology

The general block diagram of a MV drive is shown in figure 1.1, where the main parts are the rectifier and inverter [1.1] - [1.6]. The following sections describe various drive topologies and applications. The optional line-side and motor-side filters depend on the rectifier/inverter topology. A DC-link filter is mandatory yet dependant on the system topology. The phase-shifting transformer can have multiple secondaries for harmonic reduction, but has been omitted in recent transformerless industrial MV drives [1.6].

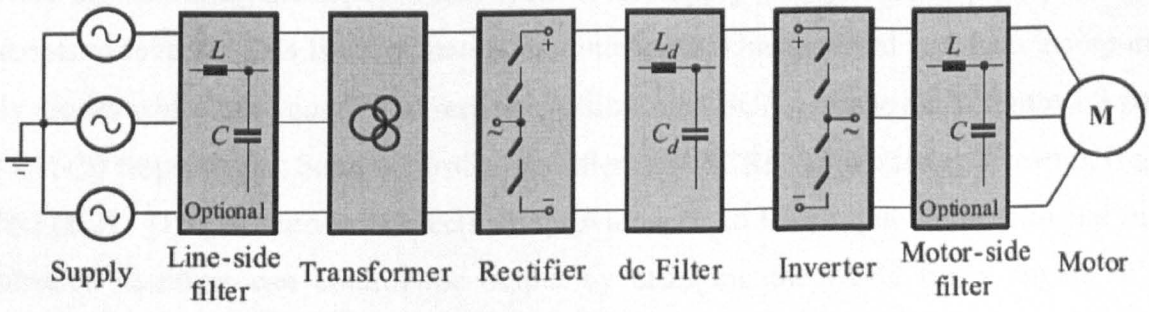

Figure 1.1: MV drive general block diagram [1.1].

1.2 Rectifier Classification

AC to DC rectification is the first stage in an induction motor drive, as indicated in figure 1.1. The rectifiers' main function is to convert the input supply from AC to DC, whether voltage or current [1.2] - [1.5]. Rectifiers can be classified according to circuit

topology as shown in figure 1.2 [1.7] where the highlighted boxes indicate the topologies used in this thesis.

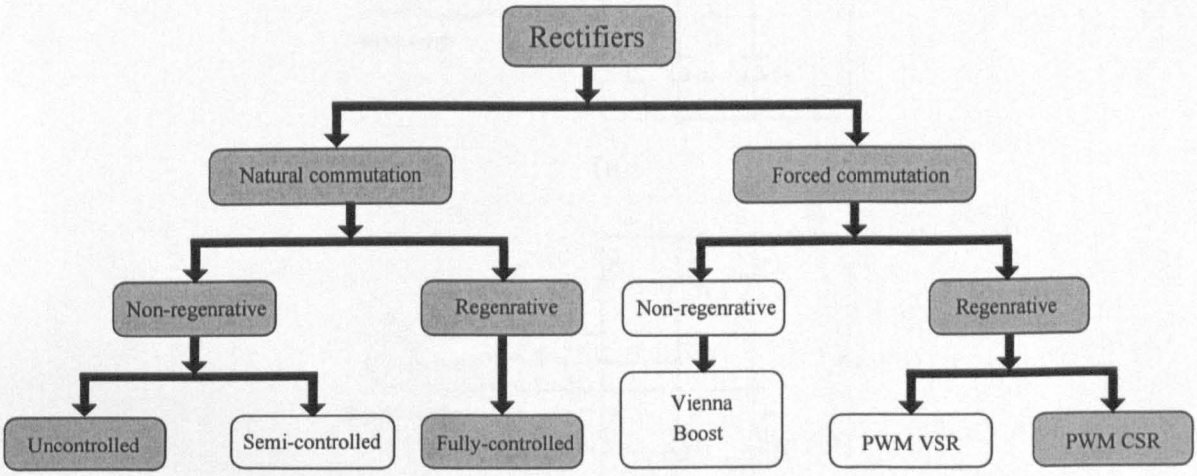

Figure 1.2: Rectifiers classification according to topology.

1.2.1 Naturally commutated rectifiers

The commutation of the rectifiers' semiconductors occurs due to the input supply voltage variation, without external intervention. The main semiconductors utilized in such rectifiers are diodes and thyristors (SCR) [1.3] - [1.5]. Diodes can not be controlled as they turn-on when forward biased by the supply voltage, while SCRs are controlled for turn-on by means of an external gating signal. Both diodes and SCRs turn-off naturally when reverse biased during the negative half cycle of the supply voltage and the principal current attempts to reverse. This is called natural commutation. Uncontrolled rectifiers incorporate only diodes while fully controlled rectifiers utilize only SCRs, as shown in figure 1.3 parts (a) and (b) respectively. Semi-controlled rectifiers use SCRs and diodes as shown in figure 1.3(c) [1.2] - [1.5]. Uncontrolled rectifiers provide a fixed DC output while semi and fully controlled rectifiers can control the output by changing the SCRs firing angle. Fully-controlled rectifiers can alternate the output voltage polarity while the output current is unidirectional, which allows power reversal. Uncontrolled and semi-controlled rectifiers are characterized by uni-polar output voltage and current, therefore no power reversal is possible [1.4], [1.5], [1.7].

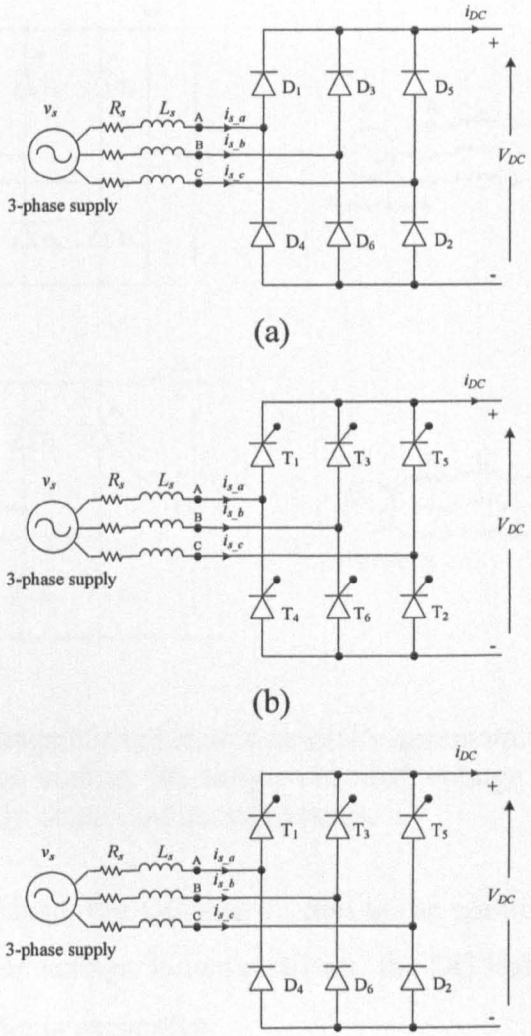

Figure 1.3: Naturally commutated rectifiers
(a) uncontrolled, (b) fully controlled, and (c) semi-controlled rectifiers.

Semi and fully controlled rectifiers can be classified as voltage source or current source naturally commutated rectifiers, as illustrated in figure 1.4. This classification is basically dependant on the controlled variable and the rectifier output filter [1.1] - [1.3], [1.7]. Voltage source rectifiers are shown in figure 1.4 parts (a) and (b) while the current source equivalents are illustrated in figure 1.4 parts (c) and (d).

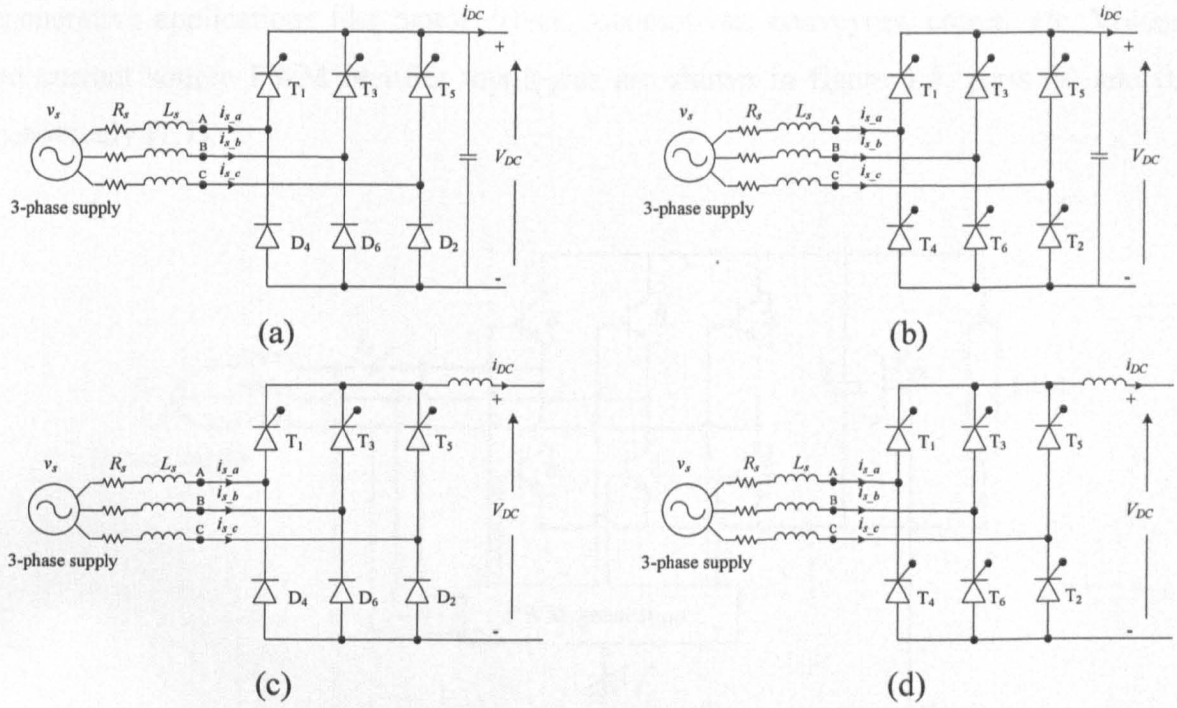

Figure 1.4: Voltage/current source naturally commutated rectifiers
(a) semi-controlled voltage source, (b) fully-controlled voltage source, (c) semi-controlled current source, and (d) fully controlled current source.

In current source rectifiers, the DC-link current is the control variable and the output filter is inductive, while for voltage source rectifiers, the DC link voltage is the controlled variable and the output filter is capacitive.

Naturally commutated rectifiers continue to be used because of their simple construction, ease of control, and possible low generation of line current harmonics. Mitigation of the harmonics involves either passive filters [1.9], [1.10] or multi-pulse rectifiers [1.11], [1.12]. Several standards have introduced stringent limits to the harmonics injected into the utility by converters [1.13].

A different rectifier concept to mitigate line current harmonics and improve the power factor uses forced-commutated rectifiers [1.1], [1.2], [1.4], [1.7].

1.2.2 Forced commutated rectifiers

The evolution of controlled power devices like the GTO and IGBT enabled relatively-high-frequency modulated forced commutated rectifiers to be developed [1.3], [1.4], [1.7], [1.8]. The ability to modulate enhances such rectifiers, which attain better performance than naturally commutated rectifiers in terms of power factor and line current harmonics

Vienna and boost rectifiers are suitable for high power applications where power reversal is not a requirement. Voltage and current source PWM rectifiers are suitable for

regenerative applications like motor drives, locomotives, conveyors, cranes, etc. Voltage and current source PWM rectifier topologies are shown in figure 1.5, parts (a) and (b) respectively [1.7].

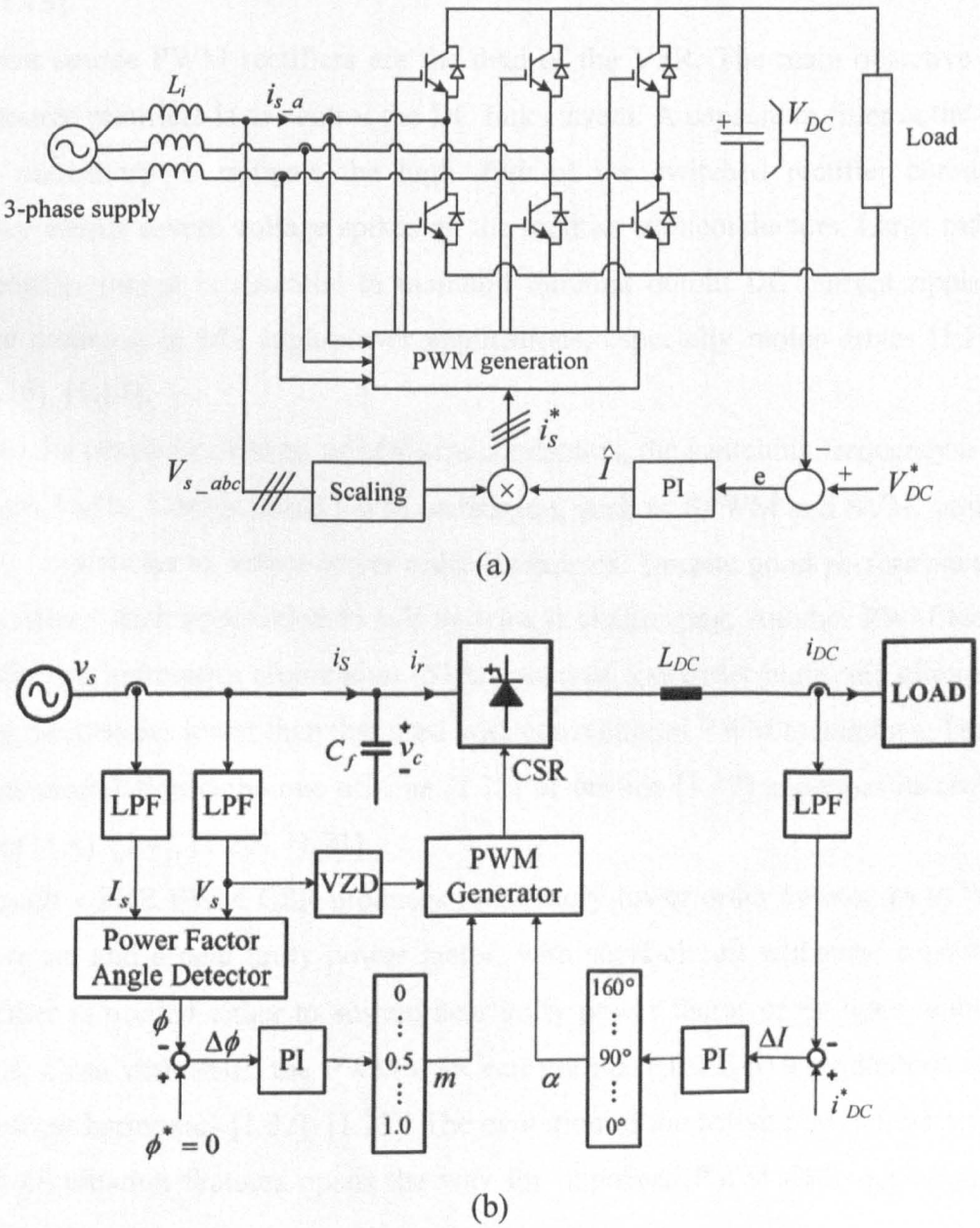

Figure 1.5: Voltage/current source PWM forced commutated rectifiers
(a) voltage source PWM rectifier and (b) current source PWM rectifier [1.1].

Voltage source PWM rectifiers are basically boost converters, where the controlled DC output voltage is greater than the peak of the input supply voltage. To achieve stability, the optimum controller is a current controller. The PWM VSR can be considered as a VSI

operating in the rectifying mode. These rectifiers allow power reversal suitable for drive applications. Proper operation of the PWM VSR relies on the capacitance at the output and inductance at the input. In addition to induction motor drives, variable-speed constant-frequency power generation is one of the main PWM VSR applications [1.1], [1.4], [1.7], [1.14], [1.15].

Current source PWM rectifiers are the dual of the VSR. The main objective of such current source rectifiers is to control the DC link current. A capacitive filter at the rectifier input is mandatory to mitigate the high *di/dt* of the switched rectifier current. Line inductance causes severe voltage spikes on the rectifier semiconductors. Large inductance at the rectifier output is essential to maintain minimal output DC current ripple. PWM CSRs are common in MV high-power applications, especially motor drives [1.1], [1.4], [1.7], [1.16], [1.17].

Due to the power limitations of MV semiconductors, the switching frequency is limited to less than 1 kHz. Conventional PWM techniques, such as SPWM and SVM, utilize high switching frequencies to reduce lower order harmonics. Despite good performance in low voltage systems, their application to MV systems is challenging. Another PWM technique, called selective harmonics elimination (SHE), ensures low order harmonic elimination at switching frequencies lower than that used with conventional PWM techniques. The ability to use this modulation technique off-line [1.18] or on-line [1.19] enhances its use in MV converters [1.1], [1.4], [1.20], [1.21].

Although a SHE PWM CSR produces satisfactory lower order harmonics in the input supply current and a near unity power factor, with short circuit withstand capabilities, a passive filter is needed either to sustain near unity power factor or mitigate higher order harmonics. Even with SHE, the PWM CSR can not meet IEEE-519 regulations for input supply current harmonics [1.22], [1.23]. The evolution of the active power filter with good harmonic elimination features opens the way for improved PWM CSR operation [1.24], [1.25].

A comparison between passive and active filter performance with the SHE PWM CSR, is presented in this study. Different semiconductors can be utilized in PWM CSR topologies, varying from the GTO and GCT to the IGBT. Optimum semiconductor selection for the PWM CSR, for different voltage levels, in terms of losses, size, and number of devices, is also investigated.

1.3 Inverter Classification

The output stage in a MV drive system is the inverter. This stage reconstructs variable-amplitude variable-frequency waveforms for motor speed control. MV inverters, classified according to topology, are shown in figure 1.6 [1.26], [1.27].

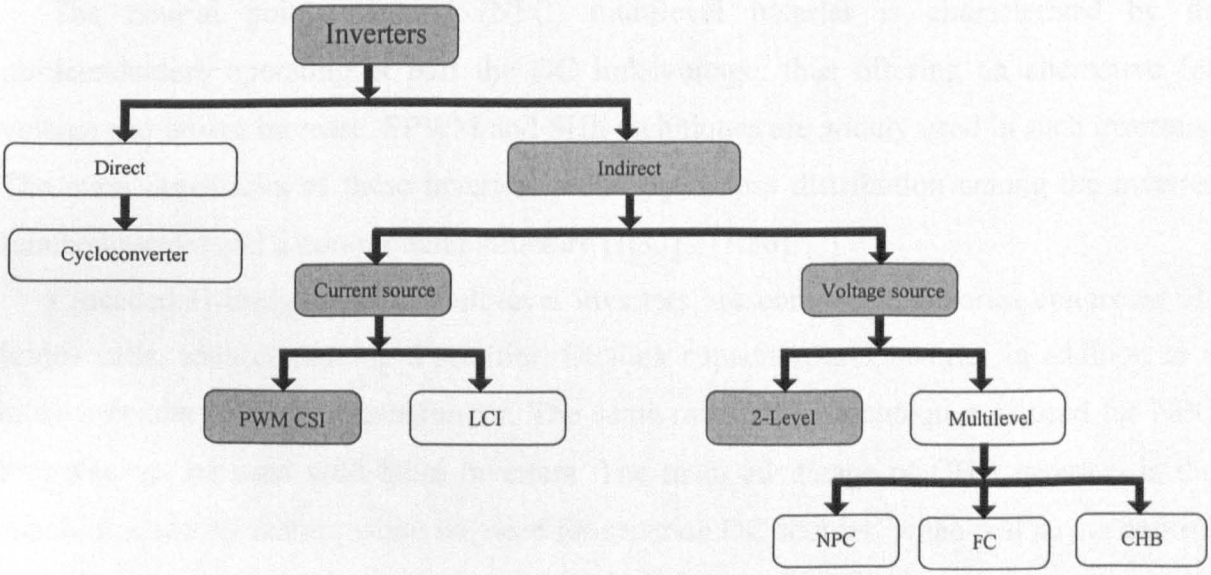

Figure 1.6: Inverters classification according to topology.

1.3.1 Direct inverters

Direct drives, using cycloconverters, perform motor control directly from the AC supply input, without a rectification stage, using an array of semiconductor switches that connect the machine to the AC supply. Cycloconverters are used in high-power drives up to 400 MW with advantages in low-speed high-torque applications like grinding mills and pump storage motor/generator sets [1.28]. Matrix converters belong to this category but are limited to applications up to 150 kW. Cycloconverters are characterized by low switching losses, high efficiency, and bi-directional power flow capabilities. Major disadvantages are limited speed range, low power factor at light load conditions, generated line harmonics, and commutation failure due to abnormal network operating conditions [1.29] - [1.32].

1.3.2 Indirect inverters

Indirect inverters can be divided into voltage and current source inverters [1.26] - [1.27].

i. Voltage source inverters

Voltage source inverters are classified as either two-level VSI or multilevel inverters. Multilevel inverters have attracted research attention, where several topologies have been introduced and commercially established. Among them, neutral point clamped, cascaded H-bridge, and flying capacitor inverters are the most common configurations [1.26].

The neutral point clamped (NPC) multilevel inverter is characterized by its semiconductors operating at half the DC link voltage, thus offering an alternative for voltage and power increase. SPWM and SHE techniques are widely used in such inverters. The main drawbacks of these inverters are unequal loss distribution among the inverter semiconductors and a non-modular structure [1.33] - [1.36].

Cascaded H-bridge (CHB) multilevel inverters are composed of series connected H-bridge cells, each containing a rectifier, DC-link capacitor, and inverter in addition to a multi-secondary isolation transformer. The same modulation techniques as used for NPC inverters can be used with these inverters. The main advantage of CHB inverters is the simple modularity feature while the need for separate DC sources, when real power control is needed, creates system complexity [1.37] - [1.39].

Flying capacitor (FC) multilevel inverters are commercially available with the disadvantages of using expensive high-voltage capacitors and a limited power range, up to 8 MW. FC multilevel converters are characterized by semi-modular features [1.40] - [1.43].

The two-level VSI is applicable to MV drives up to 6.5 kV. Extended voltage and power capabilities of the two-level VSI can be achieved by series connection of semiconductors, which is market-available technology. Two-level VSIs have the major share of the MV drives market [1.1] - [1.4], [1.26], [1.44], [1.45]. Figure 1.7 illustrates the topology of the two-level VSI.

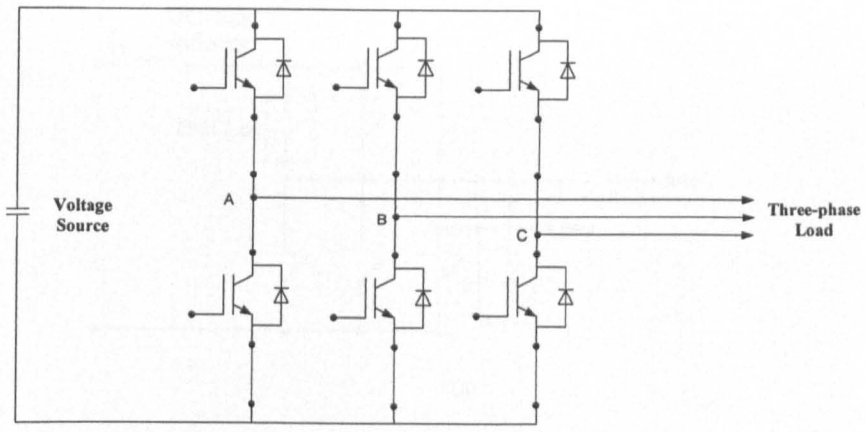

Figure 1.7: PWM VSI.

ii. Current source inverters

CSIs can be divided into two topologies, load commutated inverters (LCIs) and PWM CSIs [1.27].

LCIs are one of the earliest developed inverters, and are common in high-power synchronous motor drives of hundreds of megawatts. The SCR is the main semiconductor used in such inverters. Operation of the synchronous motor at a leading power factor facilitates SCR commutation. The rectifier stage is normally a current source fully-controlled rectifier. The main advantages of LCIs are low manufacturing cost, low semiconductor losses, and high power capability due to the use of SCRs in both rectifier and inverter stages. The disadvantages are highly distorted currents and low power factor [1.46] - [1.50].

PWM CSIs originally used GTO's and now use GCTs and high-voltage IGBTs [1.1], [1.2], [1.4], [1.8]. The PWM CSI, using different semiconductors, is shown in figure 1.8

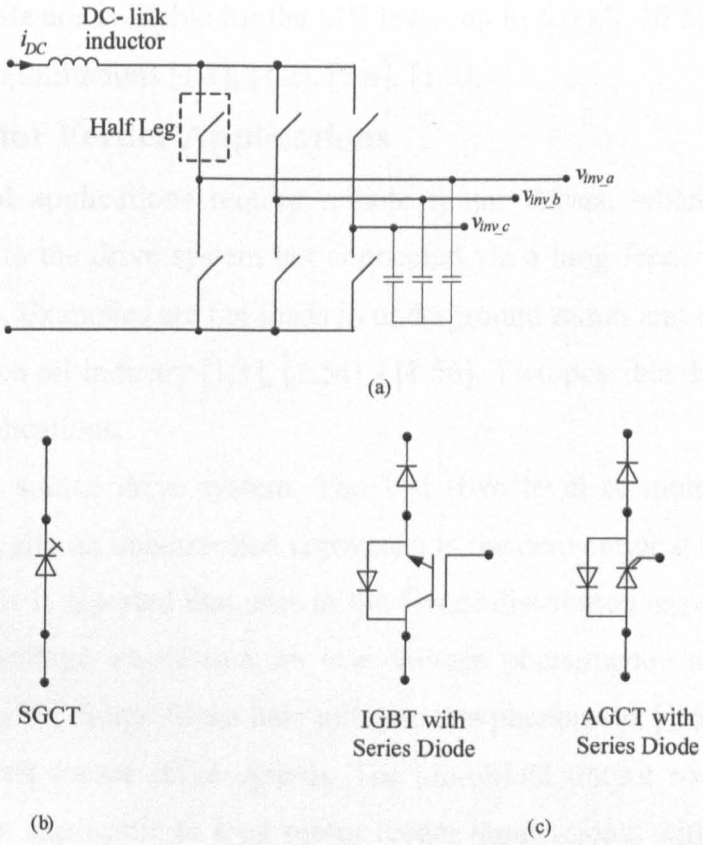

Figure 1.8: PWM CSI using different semiconductors
(a) CSI topology, (b) half leg configuration with one switch having reverse voltage capabilities, and (c) half leg configuration with one switch can not withstand reverse voltage capabilities and accompanied by series fast recovery diodes.

The CSI requires a capacitor filter at the inverter output. This filter creates near sinusoidal voltage waveforms, which are motor friendly [1.1], [1.3], [1.4]. The rectifier stage is a current source, either fully controlled SCRs or a PWM rectifier using SGCTs or HVIGBTs. Hence the input supply current can be readily harmonic mitigated with the option of near unity power factor for a wide operating range [1.51]. Due to its current source nature, the current source drive is characterized by controlled short circuit capability. The SGCTs enable a relatively high switching frequency up to 1 kHz, which allows mitigation of more lower-order harmonics [1.52]. A special DC-link inductor design enables transformerless operation, thereby reducing the size and lowering complexity [1.1]. In addition to SHE and trapezoidal pulse width modulation (TPWM) techniques, on-line switch mapping enables the use of other PWM techniques, like SVM and triple injected SPWM, which improve the harmonics mitigation process [1.53]. Drive system dynamic performance is limited due to the relatively large DC-link inductance.

Although PWM CSIs are available for the MV level, up to 6.6 kV 10 MW, semiconductors ratings are the main limitations [1.1], [1.2], [1.4], [1.5].

1.4 Long Motor Feeder Applications

Many industrial applications require remote motor drives, where the motor is not directly connected to the drive system but connected via a long feeder. The feeder length may be over 10 km. Examples are fan loads in underground mines and electric submersible pumps in the sub-sea oil industry [1.1], [1.54] - [1.56]. Two possible drive systems can be utilized in such applications.

First, a voltage source drive system. The VSI (two level or multilevel) and voltage source rectifier (usually an uncontrolled converter) is the conventional topology for such a drive systems. But it is reported that, due to the feeder distributed impedance and inverter high *dv/dt* output voltage waveforms, an over-voltage phenomenon occurs at the motor terminals [1.57] - [1.59]. Surge filters help mitigate this phenomena [1.60], [1.61].

Second, a current source drive system. The sinusoidal output nature of these drive systems, make them applicable to long motor feeder applications, with no complex filter network, like the long feeder VSI drive's surge filter, [1.1], [1.2], [1.4], [1.6], [1.62]. This study is concerned with the induction motor, with a PWM CSI accompanied by a current source fully-controlled rectifier.

A study is performed to determine which drive system is optimum for long motor feeder applications.

1.5 Thesis Objective

The main objective of the thesis is the investigation of two MV long feeder drives, namely voltage and current source systems, with emphasis on the inverter side and the long feeder. The thesis core objectives can be summarized as follows:

1.5.1 Rectifier side

- Comparison between passive and active filter performance with the SHE modulated PWM CSR.
- Loss calculation and optimum semiconductor selection for PWM CSRs.

1.5.2 Inverter side

- Performance analysis of a VSI drive for long motor feeder applications, with two surge filter networks.

- Investigation of a CSI drive, as an alternative to the VSI system, in long motor feeder applications.
- Comparison between VSI and CSI drive systems for the target application.
- Investigate a new technique for motor speed sensorless operation of long motor feeder drives.

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CHAPTER TWO:

Medium-Voltage PWM Current Source Rectifiers

In this chapter, a comparative study is undertaken of both AC side passive and active filters for MV PWM current source rectifiers, which utilize selective harmonic elimination (SHE). Modelling, design, and performance analysis of both power filters are performed in order to improve the total harmonic distortion (THD) of the input current and ensure near unity power factor operation over the full load range. The filter topologies used are the second-order passive *LC* filter with damping resistance and a shunt active power filter (APF) with control based on instantaneous active-reactive power theory (*p-q* method).

2.1 PWM CSR Filters Survey

The current Source Rectifier (CSR) is widely used in MV high-power AC drives. The basic concept types for this front end are either thyristor based rectifiers or current source rectifiers (PWM CSR) [2.1]. Thyristor based rectifiers do not meet IEEE-519 standards [2.2] hence are normally used with a group of tuned filters to improve their performance and meet the standards. The PWM CSR harmonic requirements are often accomplished by a *LC* low-pass filter, and near unity power factor operation is possible without additional circuitry [2.1], [2.3]. As the switching frequency is limited in high power applications, the preferred modulation technique is SHE. This technique enables mitigation of the low order harmonics with a low switching frequency [2.3]. A general model of the SHE technique has been presented in detail [2.4]. The design for the converter input stage filters is described in the literature [2.5] - [2.7]. A systematic approach to passive *LC* filter design for PWM current source rectifiers with consideration related to cost, power factor and parameters variation has been presented [2.8]. Filter transient response can be improved by splitting the filter into two parallel sections with the same capacitance. The purpose of the second branch is to provide a low impedance path for spike discharges due to the insertion of damping resistors [2.9]. To meet current harmonic standards [2.10], amplitude and phase variation of the modulation index for the PWM CSR to reach near unity power factor has been presented [2.11]. Practical results show acceptable performance from 30 % to 100 % loading but the performance degrades rapidly at light loads. A passive filter gives acceptable results but with some limitations:

1. Near unity power factor operation over the full loading range is not feasible.
2. Increased distortion of the rectifier input voltage.

Consequently, the active power filter has been investigated as an alternative to the passive filter. The theory of reactive power compensation has been detailed [2.12]. There are many techniques used to extract the harmonic components from the measured voltages and currents. These techniques differ in complexity, applicability to a non-ideal supply, and robustness [2.13]. The active-reactive power component method (*p-q* method) is used in this chapter, with modification to the harmonic filter order and type [2.14]. Active filters have been reviewed in many publications [2.15] - [2.17].

2.2 PWM CSR Topology and Operation

The PWM CSR circuit diagram is shown in figure 2.1. It consists of five parts, namely the utility supply, capacitor bank filter, CSR semiconductors, DC-side inductance, and the load.

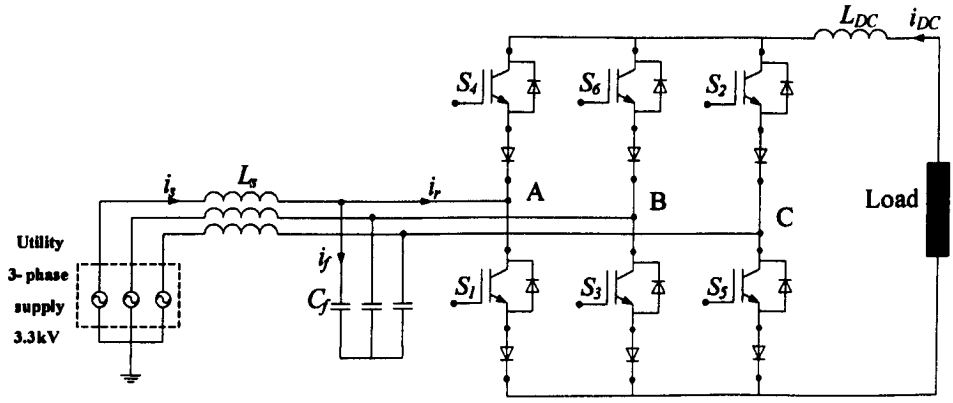


Figure 2.1: PWM CSR basic topology.

2.2.1 PWM CSR topology

The main PWM CSR parts are described in this subsection.

i. Utility supply

The CSR supply can be a single or three-phase network, depending on the construction of the rectifier. The analysis in this chapter only considers three-phase systems, hence the supply input is a three phase voltage source. Since the main application target is the MV converter, with a selected voltage level of 3.3 kV. The line inductance L_s on the rectifier AC side represents the total inductance between the utility source and the rectifier, including the equivalent inductance of the supply, leakage inductances of any isolation

transformer, and line reactor inductance for line current THD reduction. The line inductance L_s is normally in the range of 0.1 to 0.15 pu.

ii. Capacitor bank filter

The function of the PWM rectifier capacitor filter C_f is to assist rectifier semiconductor commutation and mitigate harmonic currents. The capacitance depends on the rectifier switching frequency, *LC* resonance effect, line current THD, and input power factor. It is normally in the range of 0.3 to 0.6 pu, for a switching frequency of few hundred Hertz [2.1], [2.3].

iii. CSR semiconductors

Semiconductor used in the CSR requires reverse voltage blocking capabilities, as the voltage across the devices is bi-directional. Due to semiconductors voltage limitations, series device connection is common in MV rectifiers. Therefore, symmetrical gate commutated thyristors (SGCT) or high voltage insulated gate bipolar transistors (HVIGBT) in series with a fast recovery diode are used. The selection of devices for the MV CSR, according to losses, size and number of devices, for different topologies and voltage levels, is addressed in details in chapter three.

iv. DC-side inductance

For DC current smoothing on the rectifier output, a relatively large inductance is needed, L_f. The choke is made of two mutually coupled coils on the same core to minimize the load common-mode voltage. To limit the DC-link current ripple to an acceptable level (< 15%) [2.1], the DC choke inductance is normally in the range of 0.5 to 0.8 pu.

v. Load

The PWM CSR is usually the input stage for a PWM current source inverter (CSI), which is the rectifier load. In this chapter, since the focus is on the CSR, the load is considered to be passive resistance. The PWM CSI is addressed in chapter five.

2.2.2 PWM CSR operation and control

The key to PWM CSR operation is the modulation technique used for gating the semiconductors. Since this study is concerned with MV converters, high switching frequency PWM techniques, like SVM, are not applicable because of semiconductor limitations in MV applications. The SHE technique is considered an optimum modulation technique for MV converters as it provides a superior harmonic profile with a minimum

switching frequency. Typical PWM CSR input current waveform, for a half cycle, is illustrated in figure 2.2 [2.1].

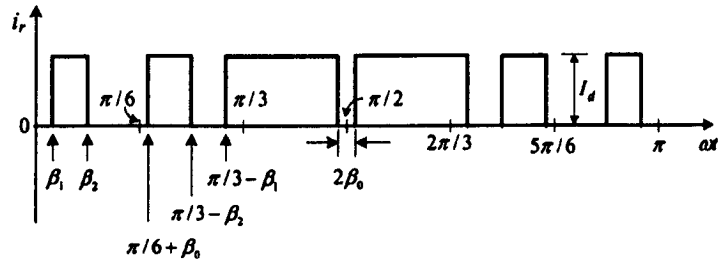


Figure 2.2: PWM CSR input current waveform for half a cycle [2.1].

There are six current pulses per half-cycle of the fundamental frequency, with only three independent switching angles, β_1, β_2, and β_0. These angles can be used to eliminate two harmonics, plus adjust the modulation index.

The PWM current waveform in figure 2.2 can be expressed as a Fourier series.

$$i_r(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t) \tag{2.1}$$

where

$$\begin{aligned} a_n &= \frac{4}{\pi}\int_0^{\pi/2} i_r \sin(n\omega t)d(\omega t) \\ &= \frac{4i_{DC}}{n\pi}\left\{\begin{array}{l}\cos(n\beta_1)-\cos(n\beta_2)+\cos(n(\frac{\pi}{6}+\beta_0))-\cos(n(\frac{\pi}{3}-\beta_2))+ \\ \cos(n(\frac{\pi}{3}-\beta_1))-\cos(n(\frac{\pi}{2}-\beta_0))\end{array}\right\} \end{aligned} \tag{2.2}$$

To eliminate the 5th and 7th harmonics, substitute $n = 5$ and 7 into (2.2) and equate to zero:

$$\left\{\begin{array}{l}\cos(5\beta_1)-\cos(5\beta_2)+\cos(5(\frac{\pi}{6}+\beta_0))-\cos(5(\frac{\pi}{3}-\beta_2))+ \\ \cos(5(\frac{\pi}{3}-\beta_1))-\cos(5(\frac{\pi}{2}-\beta_0))\end{array}\right\} = 0 \tag{2.3}$$

$$\left\{\begin{array}{l}\cos(7\beta_1)-\cos(7\beta_2)+\cos(7(\frac{\pi}{6}+\beta_0))-\cos(7(\frac{\pi}{3}-\beta_2))+\\ \cos(7(\frac{\pi}{3}-\beta_1))-\cos(7(\frac{\pi}{2}-\beta_0))\end{array}\right\}=0 \qquad (2.4)$$

By substitution into (2.2) for the fundamental frequency (n=1) where M_a is the amplitude modulation index which is the ratio of the peak fundamental rectifier input current to the DC-link output average current

$$M_a=\frac{i_{r1\_peak}}{i_{DC}} \qquad (2.5)$$

which gives

$$\frac{4}{\pi}\left\{\begin{array}{l}\cos(\beta_1)-\cos(\beta_2)+\cos(\frac{\pi}{6}+\beta_0)-\cos(\frac{\pi}{3}-\beta_2)+\\ \cos(\frac{\pi}{3}-\beta_1)-\cos(\frac{\pi}{2}-\beta_0)\end{array}\right\}-M_a=0 \qquad (2.6)$$

By solving (2.3) to (2.6) using the Newton-Raphson method, the switching angles (β_1, β_2, and β_0) as a function of the modulation index are listed in table 2.1

Table 2.1: PWM CSR switching angles for 5th and 7th harmonics elimination

M_a	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1	1.03
β_1	-13.5	-11.9	-10.3	-8.6	-6.86	-5	-3.98	-0.67	2.17	6.24	7.93
β_2	14.2	13.5	12.7	12	11.4	10.8	10.4	10.3	10.8	12.6	13.8
β_0	13.6	12.2	10.9	10.9	8	6.6	5.1	3.6	2.1	0.5	0

For a given set of switching angles β_1, β_2, and β_0, the gate signals for the CSR switching devices can be arranged. An example is shown in figure 2.3, where v_{g1} and v_{g4} are the gate signals for *S1* and *S4* in rectifier leg A, respectively. The gate signal v_{g1} is composed of six pulses, of which one is the bypass pulse, defined by θ_{11} and θ_{12}. The notch $2\beta_0$ in the centre of the i_r waveform is realized by turning on *S1* and *S4* simultaneously. The DC-link current i_{DC} is then bypassed (shorted) by the rectifier, leading to $i_r = 0$. During the bypass interval, i_{DC} is maintained constant by the large DC-link choke.

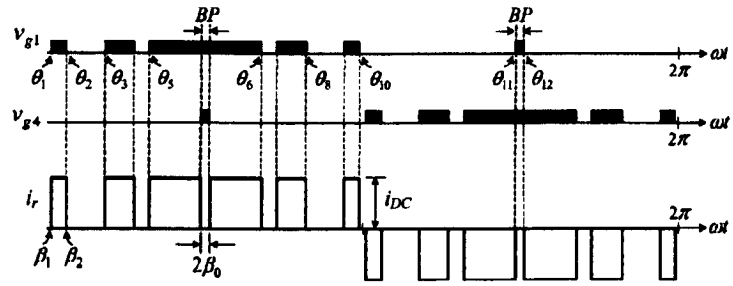


Figure 2.3: PWM CSR current and gating signals for one line [2.1].

All the gating angles, θ_1 to θ_{12}, can be calculated using table 2.1 and are plotted in figure 2.4 [2.1]. The numerical values are tabulated in Appendix A. By the same method, SHE can be extended to eliminate further harmonics by the insertion of more pulses per cycle.

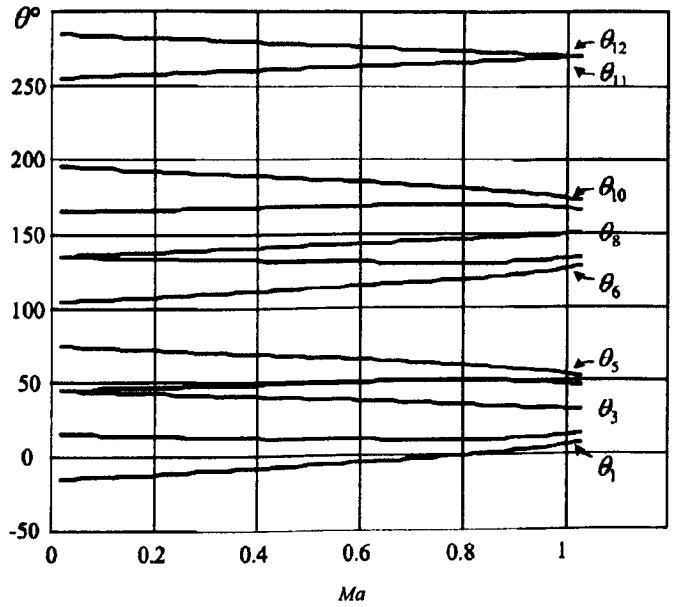


Figure 2.4: Variation of PWM CSR gating angles with modulation index for 5th and 7th harmonics elimination [2.1].

The system is simulated where the CSR is SHE modulated to mitigate the 5th, 7th, and 11th harmonics from the input line current. A 3.3 kV supply system is studied with a closed loop controlled current of 150 A. The load is a 20 Ω resistor while the DC-link inductance is 300 mH. The system block diagram is shown in figure 2.5, while figure 2.6 illustrates the input current when M_a=1 and the input current rms is 147 A, with 42.2 % THD.

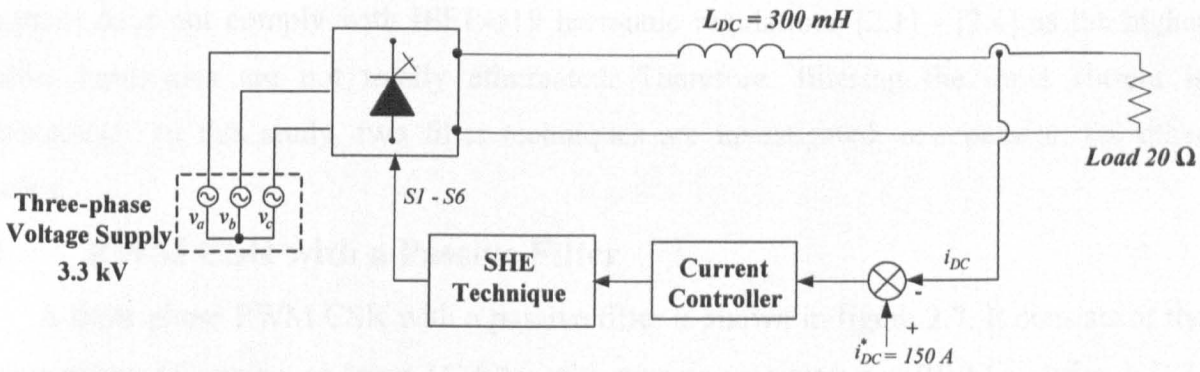
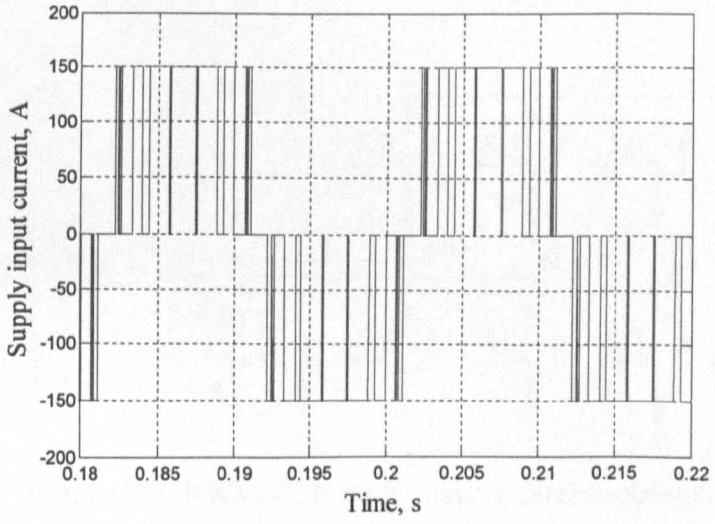
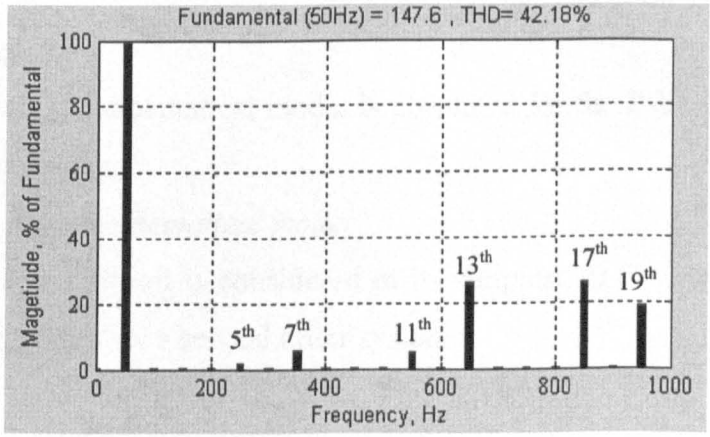


Figure 2.5: SHE CSR block diagram.



(a)



(b)

Figure 2.6: PWM CSR supply input current
(a) input current waveform and (b) input current FFT.

Although the SHE technique is used to eliminate 5th and 7th harmonics, the input current does not comply with IEEE-519 harmonic regulations [2.1] - [2.4] as the higher order harmonics are not totally eliminated. Therefore, filtering the input current is mandatory. In this study, two filter techniques are investigated, one passive, the other active.

2.3 PWM CSR with a Passive Filter

A three-phase PWM CSR with a passive filter is shown in figure 2.7. It consists of the three-phase AC mains, an input *LC* filter with damping resistance, a PWM rectifier, a DC-link inductor, and a passive load. The CSR is modulated using the SHE technique to mitigate the 5th, 7th and 11th harmonics from the input line current.

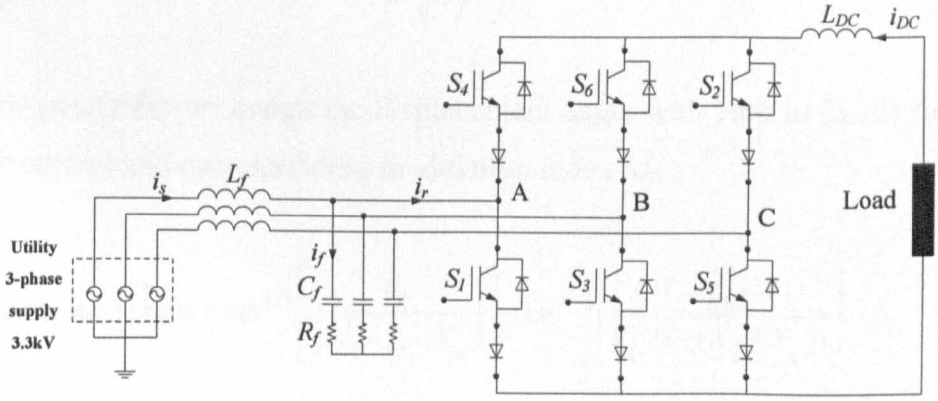


Figure 2.7: PWM CSR with passive filter topology.

2.3.1 Filter design

In this subsection, a mathematical model is presented for the PWM CSR passive filter, followed by the design steps.

i. Passive filter mathematical model

The filter equivalent circuit is considered in its simplest *RLC* form. The passive *RLC* filter transfer function (i_s/i_r) is a second order system

$$\frac{i_s}{i_r} = k\left[\frac{s+z}{s^2+2\xi\omega_r s+\omega_r{}^2}\right] \tag{2.7}$$

where

$$k=\frac{R_f}{L_f},\ z=\frac{1}{C_f R_f},\ \xi=\frac{R_f}{2\omega_r L_f},\ \text{and}\ \omega_r=\frac{1}{\sqrt{C_f L_f}}$$

The resonant angular frequency ω_r depends primarily on the C_f and L_f values, while the attenuation and damping factor ξ additionally depends on the damping resistance R_f.

ii. Passive filter design steps

(1) Select the corner frequency of the filter according to the first unwanted harmonic frequency f_h. The gain of the filter at this frequency, γ, is usually taken as 1.5 [2.8].

$$f_r \cong f_h \sqrt{\gamma} \tag{2.8}$$

(2) Substitute the selected corner frequency in (2.3)

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{2.9}$$

(3) For unity power factor, assign the displacement angle with zero in (2.10) for a certain DC-link current and corresponding modulation index M_a.

$$\text{Displacment angle} = \tan^{-1}\left[\frac{V_c}{(M_a . i_{DC} . X_c)}\right] - \tan^{-1}\left[\frac{(M_a . i_{DC} . X_l)}{V_c . (1-(X_l / X_c))}\right] \tag{2.10}$$

(4) Solve (2.9) and (2.10) to find the values of L_f and C_f.

(5) With the obtained values of L_f and C_f, find the value of damping resistor R_f by substituting into (2.11) with a gain typically 0.01 considering that the damping selection can be optimized with trade-off between filter losses and the amplification at the corner frequency [2.8].

$$\left|\frac{i_s}{i_r}\right| = \left|k\left(\frac{s+z}{s^2 + 2\xi\omega_r s + {\omega_r}^2}\right)\right| \tag{2.11}$$

2.3.2 Simulation results

The system is investigated with the same loading conditions as in the previous section but with a passive filter at the rectifier input. The performance of the passive filter is investigated with different corner frequencies to show the features of each corner

frequency selection. The results are for two different loading conditions, full load (M_a = 1) and light load (M_a = 0.1).

Table 2.2 shows the filter values at different corner frequencies while tables 2.3 and 2.4 summarize the results at the different corner frequencies for full load and light load conditions. For each filter, the tables illustrate the filter parameters (R_f, L_f and C_f), the supply current and its corresponding THD, and the peak rectifier input voltage and its corresponding THD.

Table 2.2: Filter parameters

Filter Parameter	***Units***	***350Hz***	***300Hz***	***200Hz***	***100Hz***
Filter resistance	Ω	3.7	4.03	4.7	5.9
Filter capacitance	μF	25.5	29.9	45.8	102.1
Filter inductance	mH	8.1	9.4	13.8	24.8

Table 2.3: Full load simulation results

Full Load (M_a =1)	***Units***	***350Hz***	***300Hz***	***200Hz***	***100Hz***
Supply current	A	102.8	103.4	101.6	117.3
THD of i_s	%	28.6	15.9	6.3	2.78
Rectifier input voltage V_r	V	3156	3149	3185	3808
THD of V_r	%	37.1	27.1	17.9	14.5
Power factor	-	0.903	0.926	0.963	0.994

Table 2.4: Light load simulation results

Light Load (M_a =0.1)	***Units***	***350Hz***	***300Hz***	***200Hz***	***100Hz***
Supply current	A	15.1	17.9	28.8	78.6
THD of i_s	%	6.8	4	1.1	0.1
Rectifier input voltage V_r	V	3367	3392	3515	4334
THD of V_r	%	1.32	1	0.63	0.31
Power factor	-	0.093	0.092	0.107	0.260

Figure 2.8 shows the simulated performance of the PWM CSR with the passive filter tuned at a corner frequency of 200 Hz, as an example, where the supply input current, rectifier input current, filter current, and the rectifier input line voltage are shown in figure 2.8, parts (a) to (d) respectively.

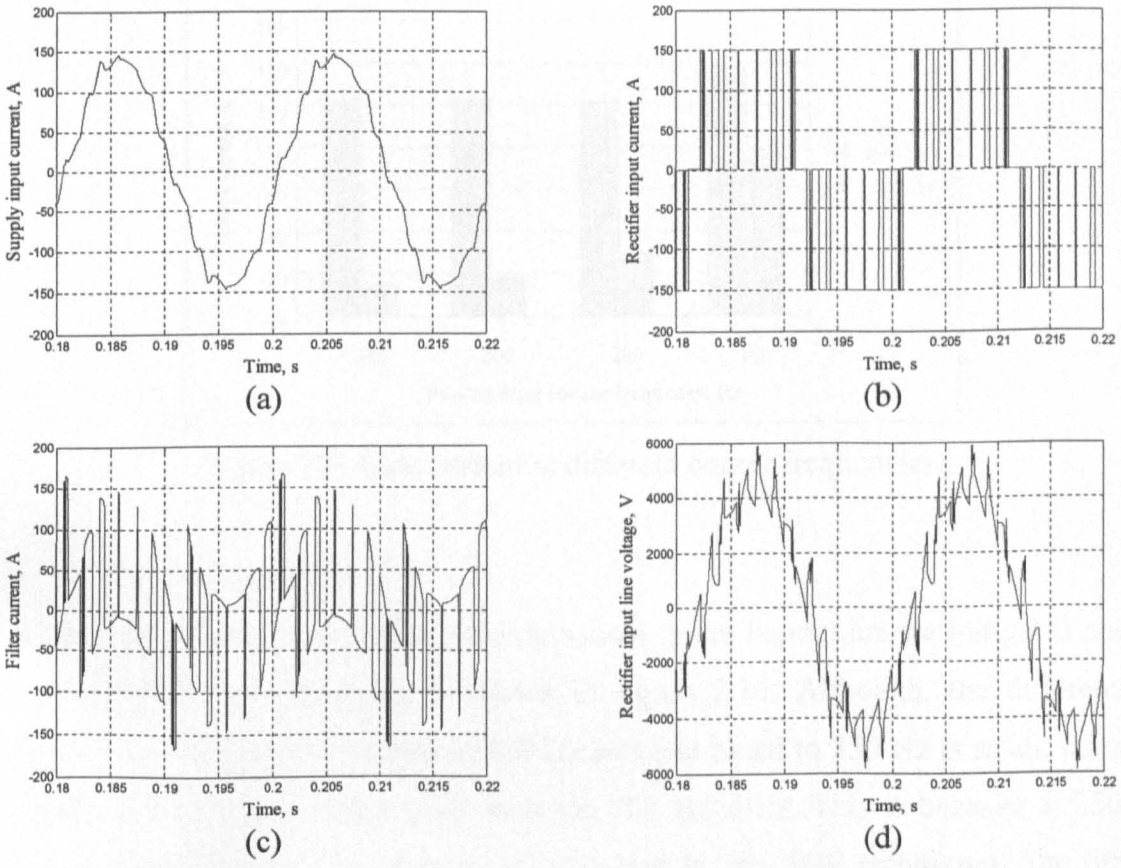


Figure 2.8: PWM CSR performance with passive filter tuned at corner frequency 200Hz at full load

(a) supply input current, (b) rectifier input current, (c) filter current, and (d) rectifier input line voltage.

The behaviour of the main parameters, (line current and its THD, filter current, power factor, and peak input line voltage of the rectifier and its THD), is investigated at different corner frequencies.

i. Line current

Figure 2.9 shows that the filters have almost the same line current when tuned at different corner frequencies, but the filter tuned at 100 Hz has increased the supply current. This is because the filter impedance is greatly decreased, (C_f is approximately doubled and L_f is halved), compared to the filter tuned to 350 Hz.

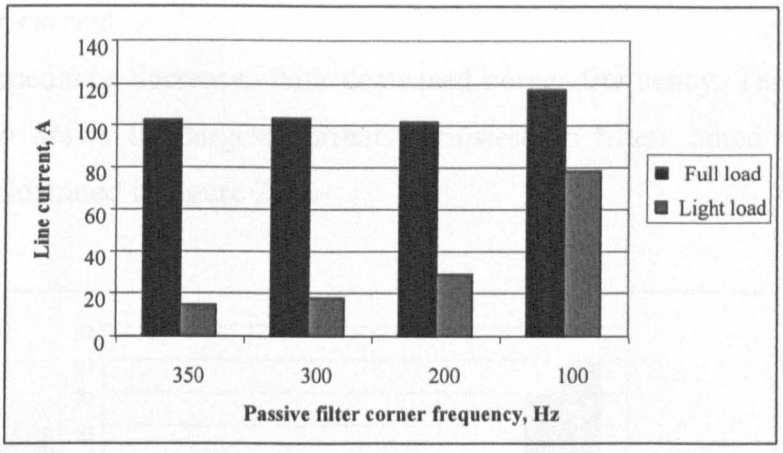


Figure 2.9: Line current at different corner frequencies.

ii. Line current THD

As the corner frequency of the filter decreases, more harmonics are mitigated and the line current THD is improved, as shown in figure 2.10. Although, the difference in impedance between the filter tuned to 300 Hz and that tuned to 350 Hz is small, there is a significant improvement in the THD with the 300 Hz filter. This is because at 350 Hz, there is a small 7^{th} harmonic component (mitigated by the SHE technique). The filter at this frequency amplifies that small harmonic component while at 300 Hz there is no harmonic. Therefore, the 300 Hz filter does not amplify any extra harmonic and produces a better THD than that tuned to 350 Hz.

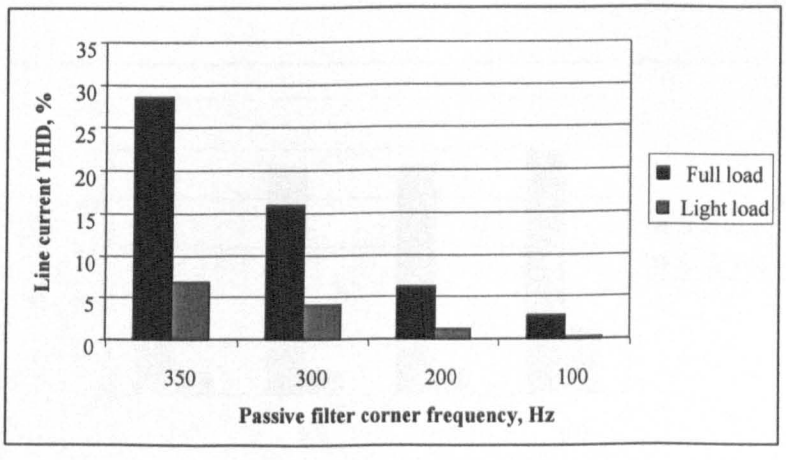


Figure 2.10: Line current THD at different corner frequencies.

iii. Filter current

The filter impedance decreases with decreased corner frequency. Therefore, the filter tuned at 100 Hz draws the largest current, compared to filters tuned at higher corner frequencies, as illustrated in figure 2.11.

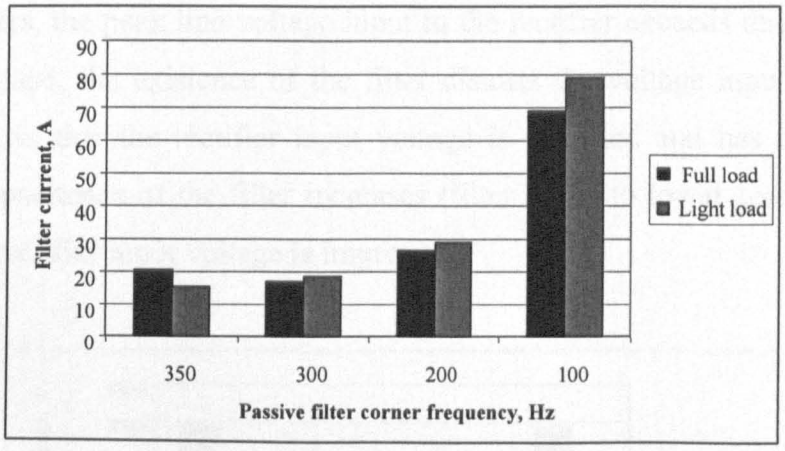


Figure 2.11: Filter current at different corner frequencies.

iv. Power factor

The design steps ensure near unity power factor operation at full load for different corner frequencies but no passive filter can achieve near unity power factor over the whole loading range. The power factor is poor, especially at light loads. Figure 2.12 shows the power factor at different corner frequencies, for both full and light loads.

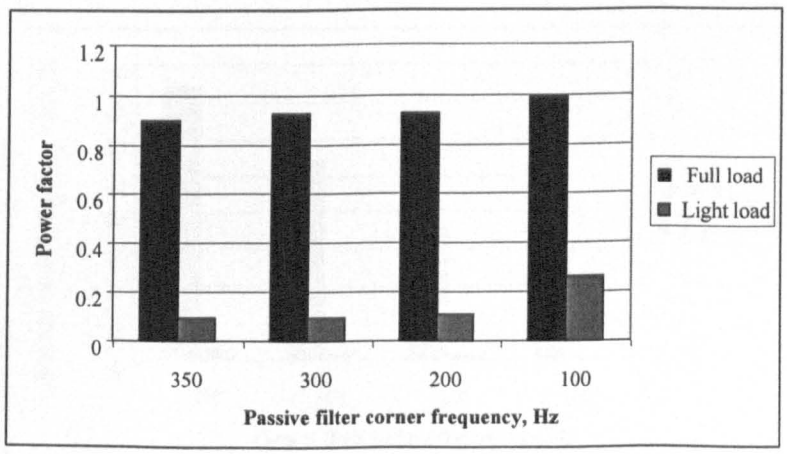


Figure 2.12: Power factor at different corner frequencies.

v. Rectifier input voltage

A passive filter affects the rectifier input voltage because of the filter inductance. The rectifier input voltage is the phasor summation of the supply voltage and the filter inductance voltage. As the filter inductance increases, the rectifier input voltage increases and becomes load dependant. The peak line voltage should be 4.66 kV, while in all the investigated filters, the peak line voltage input to the rectifier exceeds this limit, as shown in figure 2.13. Also, the existence of the filter distorts the voltage input to the rectifier. Figure 2.14 shows that the rectifier input voltage is distorted and has a relatively high THD. As the capacitance of the filter increases (filter tuned to lower corner frequencies), the THD of the rectifier input voltage is improved.

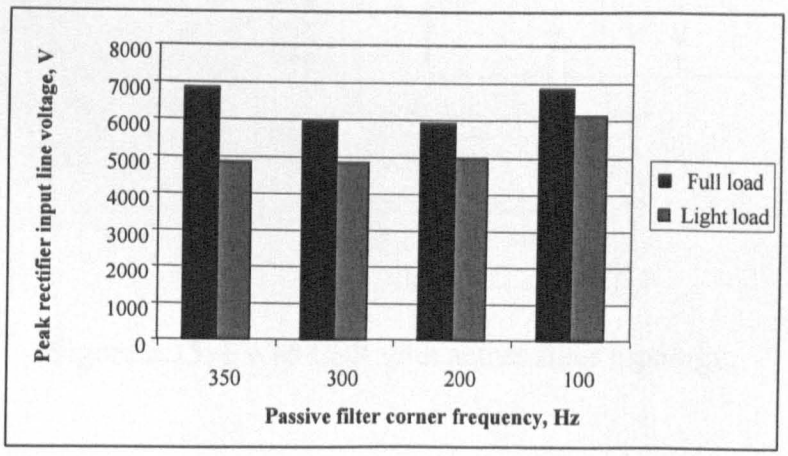


Figure 2.13: Peak rectifier input voltage.

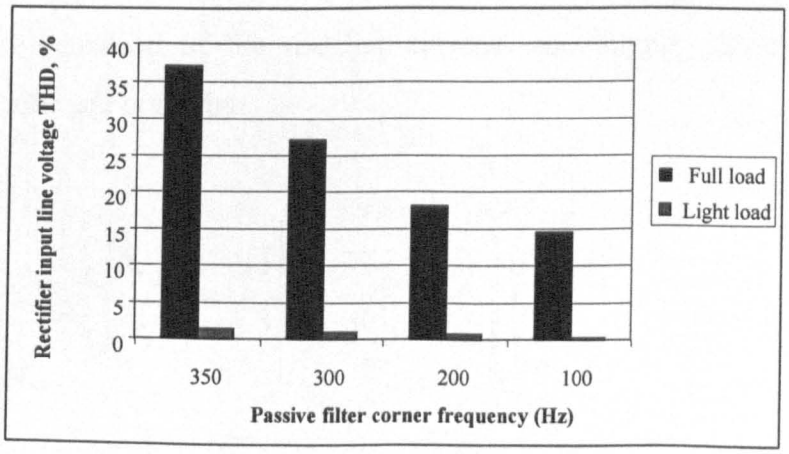


Figure 2.14: Peak rectifier input voltage THD.

2.4 PWM CSR with an Active Filter

The three-phase PWM CSR with a shunt active filter at the rectifier input is shown in figure 2.15. It consists of the three-phase AC mains, an active filter, a coupling transformer, a PWM rectifier, a DC-link inductor, and a passive load.

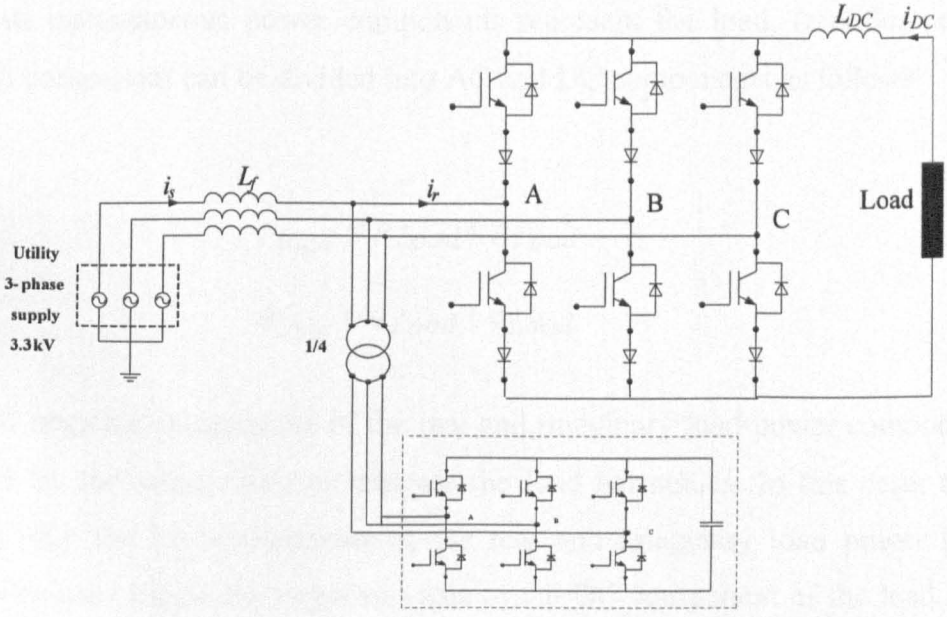


Figure 2.15: PWM CSR with active filter topology.

2.4.1 Filter design

There are various design techniques used for active filters [2.15] - [2.17]. The instantaneous active-reactive power theory is used due to its simplicity and robustness [2.16]. The transformation of the rectifier currents and supply phase voltages to the stationary α-β frame are given by

$$\begin{bmatrix} i_{r\alpha} \\ i_{r\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} \tag{2.12}$$

$$\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.13}$$

The instantaneous load real and imaginary powers can be determined by

$$\begin{bmatrix} p_{load} \\ q_{load} \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_{r\alpha} \\ i_{r\beta} \end{bmatrix} \tag{2.14}$$

The two instantaneous power components represent the load, (rectifier and passive load). Each component can be divided into AC and DC components as follows

$$p_{load} = \tilde{p}_{Load} + \bar{p}_{Load} \tag{2.15}$$

$$q_{load} = \tilde{q}_{Load} + \bar{q}_{Load} \tag{2.16}$$

The AC negative components of the real and imaginary load power components must be supplied by the active filter to mitigate the load harmonics. In this case, the supply recognizes only the DC components of the real and imaginary load power [2.14]. To improve the power factor, the negative value of the DC component of the load imaginary power must be supplied by the active filter, as given in (2.17) and (2.18). The filter draws a small amount of active power to allow for the inverter losses.

$$p_{filter} = -\tilde{p}_{load} + \bar{p}_{loss} \tag{2.17}$$

$$q_{filter} = -(\tilde{q}_{load} + \bar{q}_{load}) \tag{2.18}$$

2.4.2 Simulation results

The performance of the PWM CSR is investigated with an active filter, instead of the passive filter, under the same loading conditions. The active filter operates at a 3 kHz switching frequency, 5 mF DC-link capacitor and uses an ideal 1:4 step-down transformer to enable utilization of available low-voltage high-current IGBT modules. In the studied system, the input supply voltage is 3.3 kV and since a 1:4 transformer is used, available IGBT's rated in excess of 2.25 kV (approximately double the peak line current [2.1]) and 800 A can be used in the active filter. Higher step-down ratios result in high current demands from the active filter side while lower step-down ratios increase the voltage

stresses and leads to the need for MV semiconductors on the secondary side. Figure 2.16 shows the active filter performance at the same loading conditions as the passive filter case where the supply input current, rectifier input current, and the filter current are shown in figure 2.16 parts (a) to (c) respectively. The DC-link current is shown in part (d) while the active filter capacitor voltage and the rectifier input voltage are shown in parts (e) and (f).

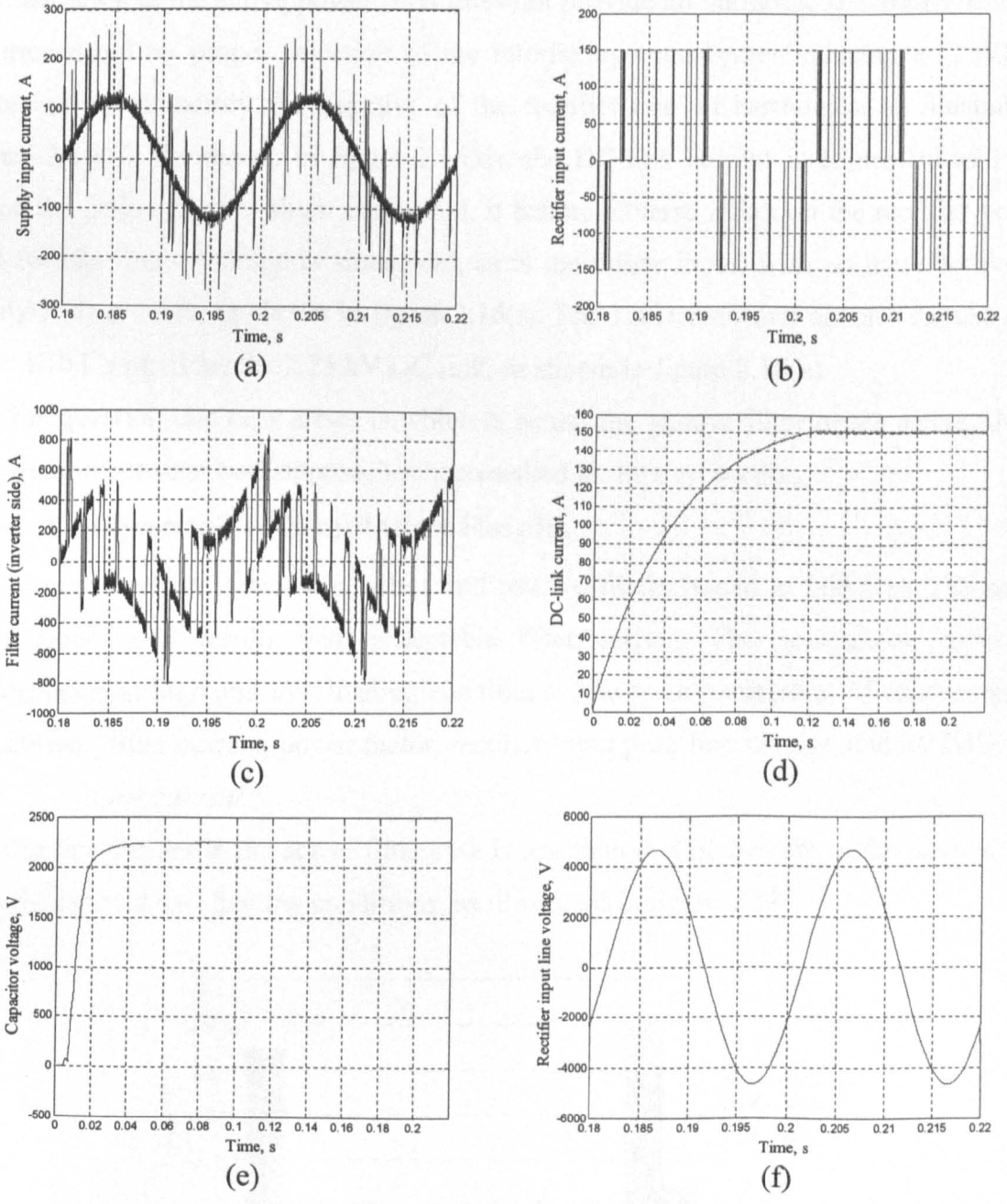


Figure 2.16: PWM CSR performance with active filter at full load
(a) supply input current, (b) rectifier input current, (c) filter current, (d) DC-link current, (e) capacitor voltage, and (f) rectifier input line voltage.

To extract the AC component from the load power, represents the harmonics, a fourth order Butterworth low pass filter with corner frequency tuned at half the supply frequency is used [2.14]. As the active filter is designed to compensate the harmonics, despite the chopped waveform of the rectifier input current shown in figure 2.16(b), the system input current is near sinusoidal with high frequency notches at the inverter switching instants, as shown in figure 2.16(a). These notches occur due to sampling delay in harmonic extraction and the fact that the active power filter does not provide all harmonic spectrums hence can be minimized by proper selection of the interfacing transformer inductance [2.17]. The filter current is mainly the negative of the rectifier current harmonics, as illustrated in figure 2.16(c). As shown in figure 2.16(d), the DC-link current is controlled to 150 A. Since the active filter is shunt connected, it has no adverse effect on the rectifier voltage. The rectifier input voltage is sinusoidal, as is the utility input, with no increase over the utility voltage level, as shown in figure 2.16(f). The 1:4 transformer enables the use active filter IGBT's rated for the 2.25 kV DC link, as shown in figure 2.16(e).

The question that now arises is which is better, the passive filter or the active filter. A comparison between both approaches is presented in the next section.

2.5 Comparison of Simulation Results

The comparison is between active and passive filters (tuned at 200 Hz). The passive filter gives good results with acceptable filter current. The comparison covers the performance at high and low loading conditions. The main parameters of concern are the line current, filter current, power factor, rectifier input peak line voltage, and its THD.

i. Line current

The line current in the active filter case is less than that in the case of the passive filter, at both high and low loading conditions, as illustrated in figure 2.17.

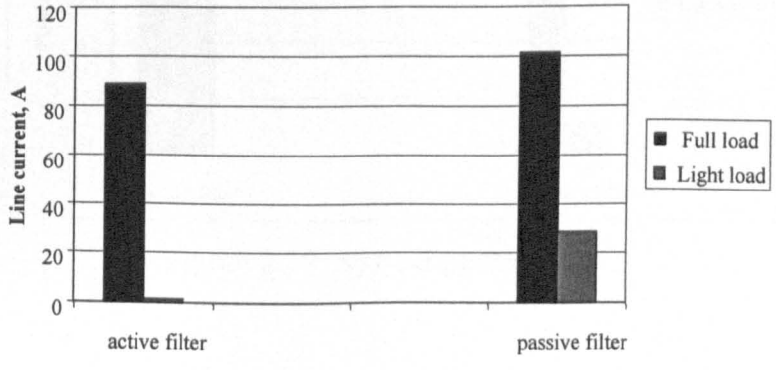


Figure 2.17: Line current for active and passive filters.

ii. Filter current

The active filter adapts to loading conditions while the passive filter draws approximately the same current over the whole loading range. This is clearly seen in figure 2.18.

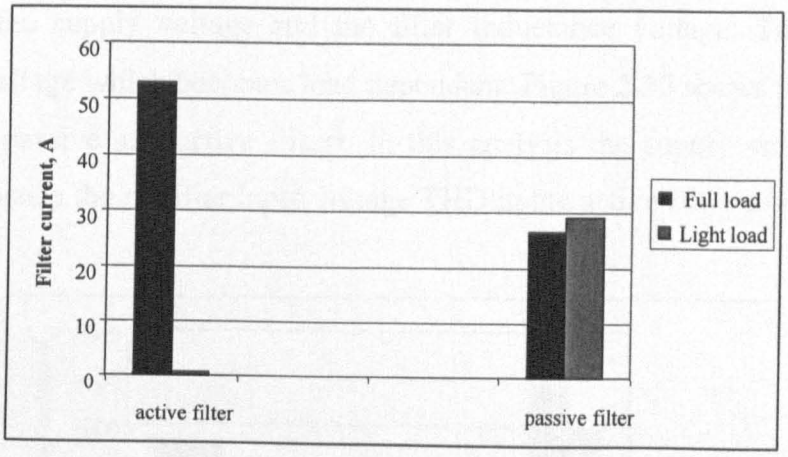


Figure 2.18: Filter current for active and passive filters.

iii. Power factor

Although the passive filter is designed to make the system operate at near unity power factor at full load, this can not be fulfilled at low loading conditions. But, the active filter can achieve near unity power factor at high and low loadings. This is illustrated in figure 2.19.

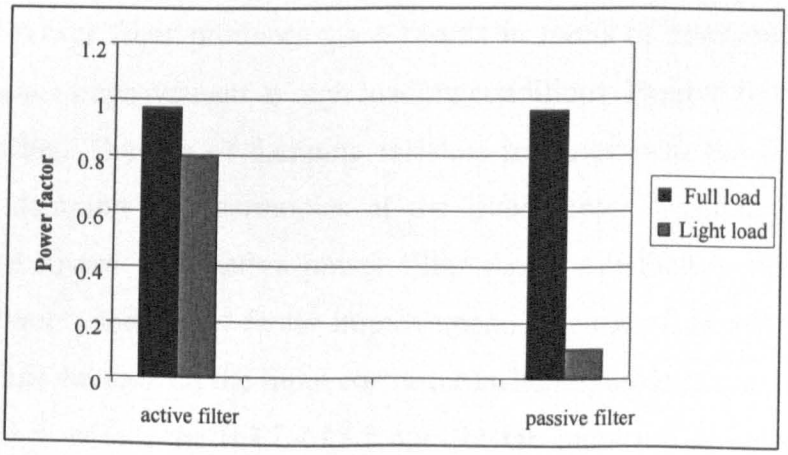


Figure 2.19: System power factor.

iv. Rectifier input voltage

An active filter does not affect the rectifier input voltage because it is connected to the system as a shunt source. The passive filter increases the rectifier input voltage because the system operates at a leading power factor due to the filter impedance (specially the shunt capacitors). Moreover, filter series inductance makes the rectifier input voltage the phasor summation of the supply voltage and the filter inductance voltage. This increases the rectifier input voltage which becomes load dependant. Figure 2.20 shows the rectifier input voltage for the passive and active filters. In this analysis the supply voltage is assumed harmonic free, hence the rectifier input voltage THD in the active filter case is almost zero

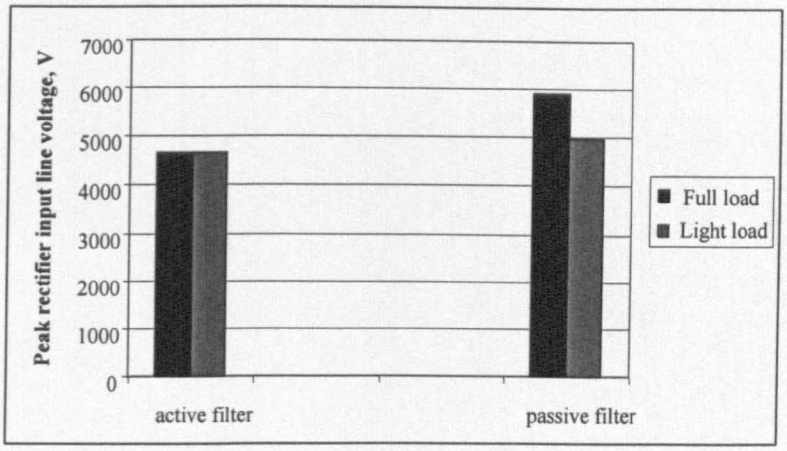


Figure 2.20: Peak line rectifier input voltage for active and passive filters.

Discussion

The passive power filter produces good results in terms of harmonic cancellation as well as power factor improvement at high loading conditions. Passive filter performance is poor at low loading. The use of damping resistors in series with the filter capacitors is mandatory (for damping any harmonics at the filter corner frequency) but contribute additional system losses. The active power filter shows satisfactory results in terms of harmonic cancellation and power factor improvement. The use of an active filter does not increase the voltage stresses on the input converter switches, as does the passive filter. The active filter THD is within the IEEE-519 range for the input utility current and voltage. The supply current is lower, for the same loading conditions in the active filter case than in the passive filter. The power factor is approximately constant over the loading range if an active filter is used. As a result, the active filter performance is superior to that of the

passive filter over the full range of loading. Small capacitance can be shunt connected in the case of active filter to decrease the active power filter current. System cost, complexity and reliability are the main drawbacks of active filters [2.18].

Summary

The construction and theory of operation of the PWM CSR were briefly explained. The SHE technique is the most suitable PWM technique for MV converters, so was presented in detail. By simulating the PWM CSR with SHE, the input current does not meet the standard harmonic regulation requirements. Hence, two types of filters were studied, passive and active filters. The mathematical model of the passive filter and its design steps were discussed, followed by a performance evaluation for different corner frequencies, to clarify optimum corner frequency selection. Then the model of the active shunt power filter was presented, guided by simulation results to illustrate system performance. Finally, a comparison between both filters was carried out showing features and limitations for both systems and their influence on the PWM CSR.

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CHAPTER THREE:

Medium-Voltage PWM Current Source Rectifiers using Different Semiconductors: Loss and Size Comparison

In this chapter, a comparison of losses and physical size is presented for three semiconductor devices when used in MV high power applications. The comparison is made for MV PWM current source rectifiers (CSR) using SHE modulation. The devices are high voltage insulated gate bipolar transistors (HVIGBT) and two types of hard-driven thyristors, namely symmetrical and asymmetrical gate commutated thyristors (SGCT, AGCT). The study is based on practical devices using semiconductor device vendor data sheets, taking into account accurate discrimination between turn-off and recovery states. The constant-voltage switching energy characteristic curves applicable to voltage source converters are adapted to suit varying voltage applications like the PWM CSR, with emphasis on how voltage is shared between series devices during each commutation. Nine configurations using different semiconductor devices are introduced for MV PWM CSRs employing SHE. The losses, (conduction, on-switching, off-switching, and recovery), associated with these configurations are investigated. A comparison from a physical size aspect is introduced. The proposed loss calculation procedure utilizes practical device data sheet curves with point by point discretization at each step. Consequently, this procedure is similar to building a discrete model with curve fitting of the semiconductor data. Moreover, the proposed procedure is generic. This chapter provides MV PWM converter designers with a systematic pre-design approach to guide in deciding which type of power semiconductor suits a particular system voltage and power requirement.

A semiconductor loss calculation survey is presented in section 3.1. Three different semiconductor arrangements suitable for the MV PWM CSR are illustrated in section 3.2, for three voltage levels, 2.4 kV, 3.3 kV and 6.6 kV. Then, in section 3.3, the loss calculation procedure, from device data sheets, is performed for each configuration at each system voltage level. Finally, a comparison between the different configurations in terms of total losses and size is presented in the section 3.4.

3.1 Semiconductors Loss Calculation Survey

Current source rectifiers are frequently used in MV, high-power AC drives. The basic front end converters are either a thyristor phase controlled rectifier or a PWM CSR that is usually SHE modulated, as the switching frequency is limited in these applications [3.1] - [3.3].

The phase-controlled rectifier is simple but requires a group of passive and/or active filters to accomplish the necessary harmonic and input power factor requirements for a wide operating range.

Alternatively, the input harmonic requirements for the PWM CSR are often accomplished with the addition of a simple LC low-pass filter, and near unity power factor operation is possible over a restricted range without additional equipment [3.1] - [3.3]. Figure 3.1 shows the basic structure of this type of active front end rectifier [3.1], [3.2].

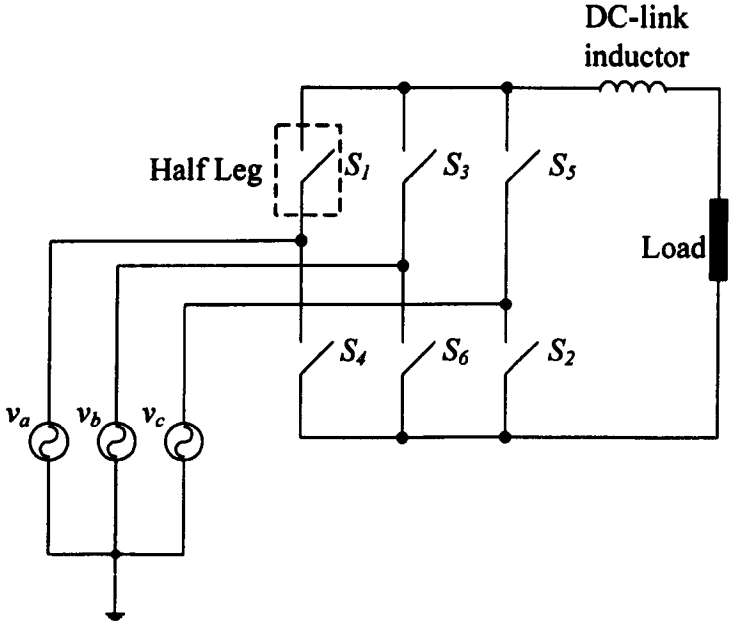


Figure 3.1: Basic structure of PWM CSR.

A SHE technique [3.1] mitigates low order harmonics, with a low switching frequency. The CSR is usually modulated to mitigate the 5th, 7th and 11th harmonics from the input line current. Therefore, the switching frequency is eleven times the supply frequency. Figure 3.2 shows the gating signals for the half-leg switch S1 in a PWM CSR operating at a modulation index (M) of 1. The shown gating signal is supposed to be quarterly and semi cycle symmetrical, like the one shown in figure 2.3 plotted at constant modulation index.

The gating signal in figure 3.2 is plotted in closed loop system hence suffers a small asymmetry due to the effect of the closed loop DC-link current control loop that continuously varies the modulation index. In order to achieve the required harmonic elimination, each rectifier switch is gated with eleven pulses per cycle.

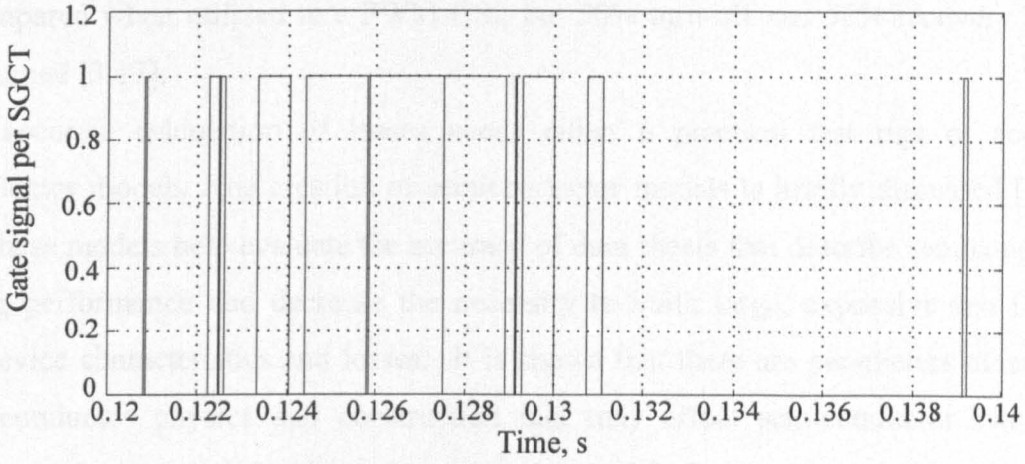


Figure 3.2: Gating signal for each half leg of PWM CSR using SHE to mitigate the 5^{th}, 7^{th} and 11^{th} harmonics in the line current.

Gate turn-off (GTO) thyristors were used in this topology until the mid 90s. GTO performance was limited by a low switching frequency and large snubber components [3.4]. The GCT, with its two variants, symmetrical (SGCT) and asymmetrical (AGCT) are an enhanced GTO. The higher operating switching frequencies and the simple *RC* snubber circuit enhance GCT utilization [3.5], [3.6]. The ability to operate with a self-powered gate driver in current source systems contributes to GCT usage [3.7]. A loss comparison between the GTO and GCT has revealed that the GCT is superior to the GTO [3.8] when a half bridge circuit with a clamping diode and inductive load are used. The GCT, series connected, has been used in a 7.2 kV inverter [3.9].

The development of robust insulated gate bipolar transistors, IGBT, capable of operating at high voltage levels complicates the decision as to which device is the best for MV high-power converters. It was shown that HVIGBT's can operate safely with a relatively high switching frequency in a snubberless mode, in inverters up to 5 MW [3.10], [3.11].

The GTO and IGBT have been compared in a voltage source inverter mode [3.12] while the IGBT and GCT have been compared using a clamp circuit and same the

operating conditions [3.13]. The GCT and IGBT were compared in a neutral point clamped inverter applications [3.14].

Other investigations have compared the IGBT, GCT and ETO (emitter turn off) thyristors using a pulse-tester circuit [3.15], [3.16]. All the mentioned comparisons were performed for constant voltage switching applications, except where the SGCT and AGCT were compared when utilized in a PWM CSI, but 50% turn-off and 50% recovery losses were assumed [3.17].

The accurate calculation of losses needs either a practical test rigs or accurate semiconductor models. The creation of semiconductor models is briefly discussed [3.18], [3.19]. These models help evaluate the accuracy of data sheets that describe semiconductor switching performance and decrease the necessity to build large, expensive test rigs to extract device characteristics and losses. It is shown that there are parameters other than the semiconductor physics and construction that may affect semiconductor switching behaviour, such as stray inductance, inverter topology, device position, and commutation loops [3.20]. Such effects are not within the scope of this study. Therefore practical data sheet utilization is sufficient to loss calculation [3.21].

3.2 Arrangement of PWM CSR Devices

Table 3.1 shows the blocking voltage requirement for each MV level [3.22].

Table 3.1: Required blocking voltage for PWM CSR per half-leg

Nominal line voltage (kV)	*Preferred repetitive blocking voltage (kV)*
2.4	6.5
3.3	9
6.6	18

In the case of current source rectifiers, each device must have reverse blocking capabilities. This is not a problem for the SGCT. But with the IGBT and AGCT, a diode in series with the switch is mandatory since such switches do not have suitable reverse blocking capabilities. Figure 3.3 shows different semiconductor combinations suitable for PWM CSR half-leg application.

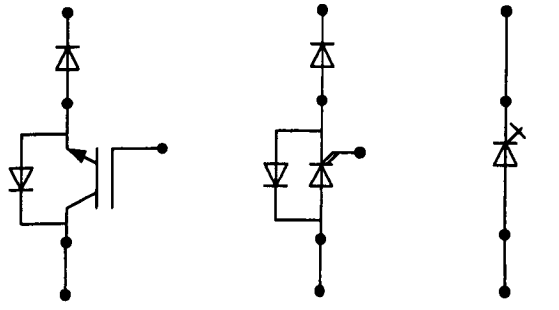


Figure 3.3: PWM CSR half leg utilizing different types of semiconductors. (Anti-parallel diodes are used to protect uni-directional switch during series diode reverse recovery)

Table 3.2 shows the different semiconductor combinations for each voltage level per half-leg of a PWM CSR, complying with the blocking voltages given in table 3.1. These combinations will be compared from a loss point of view. Note that similar devices may need series connection to achieve the required blocking voltage.

Table 3.2: Different semiconductor combinations for a half leg of a MV PWM CSR

Nominal line voltage (kV)	***HVIGBT***	***SGCT***	***AGCT***
2.4	1 x 6.5 kV HVIGBT + 2 x 4.5 kV series diodes	1 x 6.5 kV SGCT	2 x 4.5 kV AGCT + 2 x 4.5 kV series diodes
3.3	2 x 4.5 kV HVIGBT + 2 x 4.5 kV series diodes	2 x 6.5 kV SGCT	2 x 4.5 kV AGCT + 2 x 4.5 kV series diodes
6.6	3 x 6.5 kV HVIGBT + 3 x 6 kV series diodes	3 x 6.5 kV SGCT	4 x 4.5 kV AGCT + 3 x 6 kV series diodes

The series connection of semiconductors is common due to the development of voltage balancing circuits in case of the IGBT and GCT [3.1]. A universal voltage balancing circuit has been introduced [3.23]. An optimization design procedure that showed the trade-off between voltage imbalance, turn-on current, *di/dt* endurance, and losses has been presented [3.24]. The loss contribution of the voltage balancing circuits is not considered in this chapter as losses in optimal configurations can be low with traditional designs [3.25]. In the proposed loss calculation procedure, based on practical data sheets, typical switching

network parameters, like snubberless operation of the HVIGBT and recommended *RC* snubbered operation of the AGCT/SGCT, are taken into consideration. The effect on loss calculations due to deviation of these parameters is not considered, as they are case dependant and exhibit high non-linearity. A selection of applicable devices from different vendors is shown in table 3.3.

Table 3.3: Selected semiconductors

Device type	*Device voltage*	*Manufacturer*	*Part number*
HVIGBT	4.5 kV	DYNEX	DIM600NSM45F000 [3.26]
Diode	4.5 kV	DYNEX	DFM600NXM45F000 [3.27]
AGCT	4.5 kV	ABB	5SHY35L4510 [3.28]
SGCT	6.5 kV	MITSUBISHI	GCU08BA130 [3.29]
HVIGBT	6.5 kV	ABB	5SNA0600G650100 [3.30]
Diode	6.0 kV	ABB	5SDF10H6004 [3.31]

3.3 Semiconductor Losses

The main semiconductor device losses are classified into two types, namely conduction and switching losses, (turn-on and turn-off/recovery losses). Losses result in a rise in semiconductor junction temperature. The loss calculation is essential in power converter design in order to select a suitable device for each power rating and to select a suitable heat sink. Voltage and current waveforms for each half-leg configuration for a PWM CSR using SHE are shown in figure 3.4 where the switching pulses are numbered one to eleven in order to identify the switching mode at each rising/falling edge of the pulses. The PWM CSR is simulated three times, each time utilizing a different semiconductor configuration for its half legs. The simulated system has a 3.3 kV, 50 Hz input with a DC-link current ranging from 100 A to 600 A. A switching frequency of 550 Hz is used for the SHE modulation. Single, not series, devices are used in each half-leg for the following simulation to simplify the illustration. The purpose of this simulation is to show how the devices are gated and respond to the system voltages and currents. Also, conduction and switching loss periods can be illustrated, especially the difference between off-switching and recovery periods.

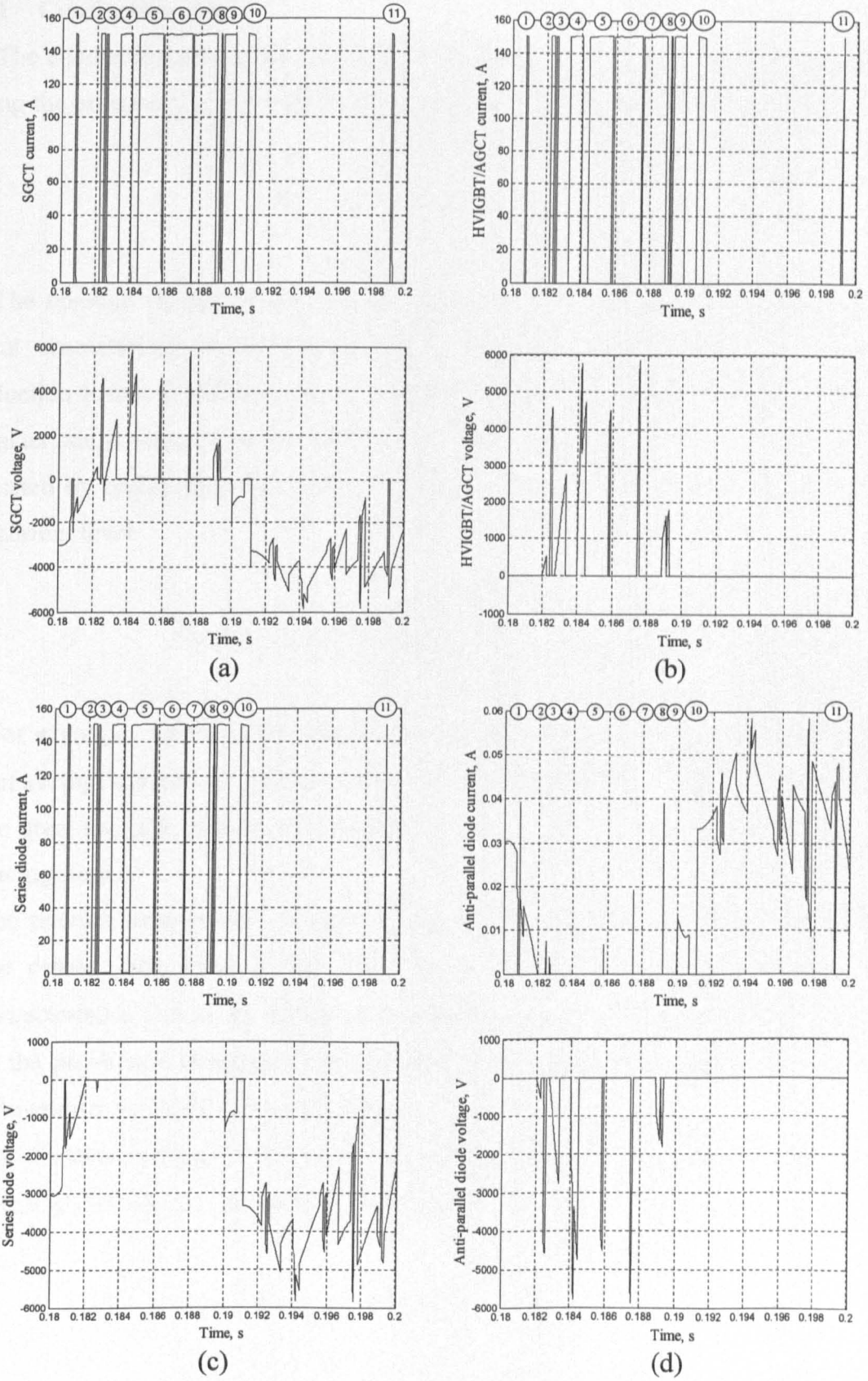


Figure 3.4: Voltage and current waveforms for half leg in a PWM CSR
(a) single SGCT is used as a half leg, (b) single AGCT/HVIGBT with anti-parallel diode and series diode are used as a half leg, (c) series diode with AGCT/HVIGBT, and (d) anti-parallel accompanying the AGCT/HVIGBT.

3.3.1 Conduction loss

The conduction power loss during device on-state is the product of the current flowing during the on-state ($I_{on\text{-}state}$) and the voltage drop at this current level ($V_{on\text{-}state}$).

$$P_{conduction} = V_{on-state} \times I_{on-state} \tag{3.1}$$

The on-state voltage depends on the current flowing through the device. The device output characteristic at maximum junction temperature can be used to calculate the conduction losses at different current levels. In order to simplify the analysis, the output characteristic is linearly interpolated [3.32]. The switch average conduction power can be evaluated by multiplying the average on-state current by the average on-state voltage at this current level.

$$P_{conduction\_average} = V_{on-state-average} \times I_{on-state-average} \tag{3.2}$$

For example, a PWM CSR with a 150 A DC-link current at a modulation index of 1, has an average current per switch of 50 A while the peak switch current is 150 A, assuming ripple free DC-link current. Calculation of the conduction loss is performed by the following steps:

1. The relation between the on-state voltage and the on-state current is determined from the device data sheet [3.26] - [3.31], as shown in figure 3.5. Selected output characteristics curves are typical characteristics at 125 °C. For HVIGBT's, in addition to the previously mentioned temperature value, output characteristics curves at 15 V gate-emitter voltage (V_{ge}) are selected.
2. The on-state relation is linearized to simplify the calculations as described in (3.3) where 'χ', '$a1$' and '$b1$' are listed in the Appendix B.

$$V_{on-state-\chi} = a1 \times I_{on-state} + b1 \tag{3.3}$$

3. The conduction loss is calculated by substituting (3.3) into (3.2) taking into account the device configuration used at each voltage level, for a DC-link current range of 100 A to 600 A. Figure 3.6 shows the conduction loss variation with DC-link current per half leg.

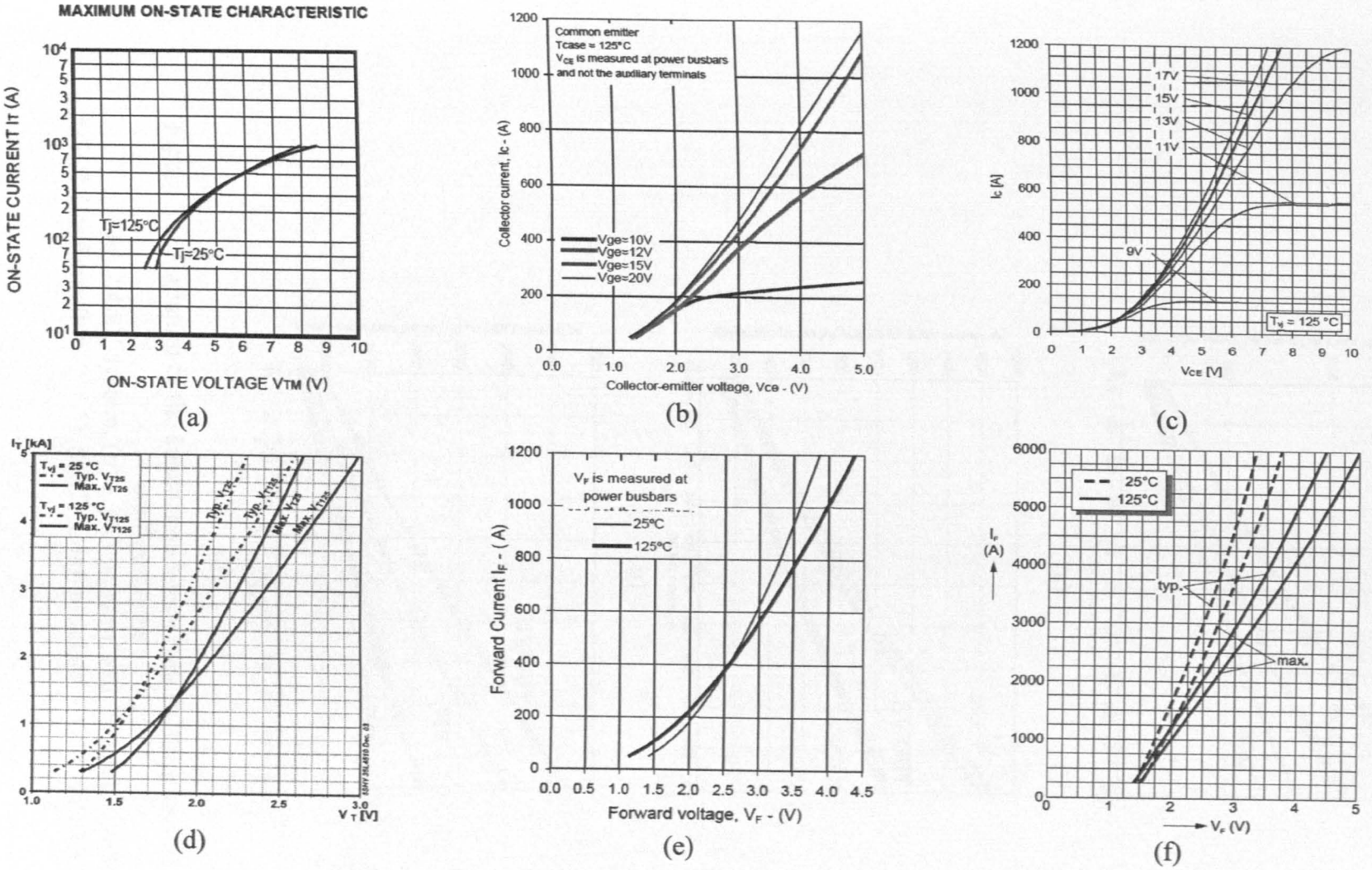
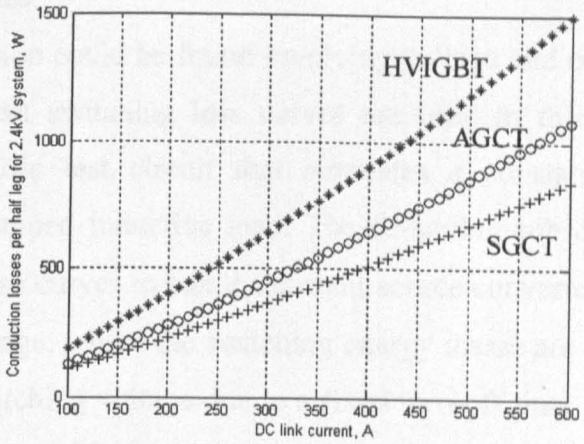
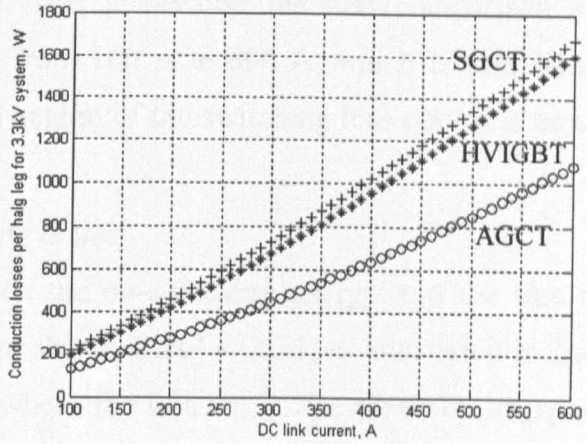


Figure 3.5: Relation between on-state voltage and on-state current for (a) 6.5 kV SGCT [3.29], (b) 4.5 kV HVIGBT [3.26], (c) 6.5 kV HVIGBT [3.30], (d) 4.5 kV AGCT [3.28], (e) 4.5 kV Fast diode [3.27], and (f) 6 kV Fast diode [3.31].



(a)



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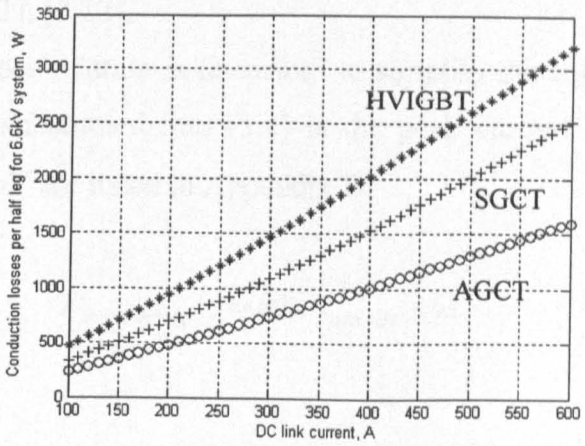


(c)

Figure 3.6: Variation of the conduction losses with DC-link current for different configurations.
(a) 2.4 kV system, (b) 3.3 kV system, and (c) 6.6 kV system
o AGCT Configuration + SGCT Configuration * HVIGBT Configuration

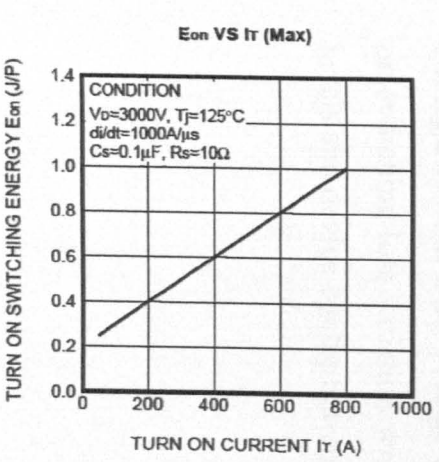
3.3.2 Switching losses

No simple expression could be found involving voltage and current during a switching transient. The datasheet switching loss curves are used in this case. These curves are referenced to a specific test circuit that simulates a constant DC-voltage switching application with a clamped inductive load. The following subsections describe how the designer can adapt these curves to suit the current source converter that is characterized by varying switching voltage, where the switching energy losses are considered to be directly proportional to the switching voltage due to a fixed turn-off time [3.32]. Switching energy curves, although exponential in the higher current range, are linearized in the proposed loss calculation procedure. This is because the loss comparison assumes operation in the normal current range, from 100 A to 600 A, which is near linear in the used data sheet curves. The non-linear region of the switching loss curves is beyond the normal operating current range.

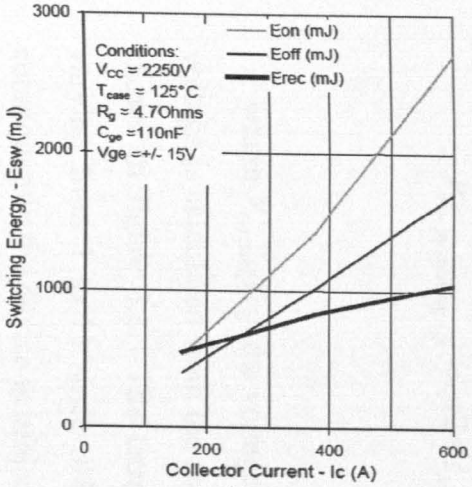
i. On-switching losses

1. The relation between the on-switching energy and the turn-on current is determined from the device data sheets [3.26] - [3.31] as illustrated in figure 3.7, specifically part (d) for the AGCT where the relation is linearized by interpolation due to the lack of curves on the data sheet. Also, the on-switching loss is neglected for the series fast recovery diodes [3.1], [3.22].
2. The on-switching loss relation is linearized to simplify the calculations as described in (3.4). The current substituted into (3.4) is the peak current at the instant of turn-on where 'χ', '$a2$' and '$b2$' are listed in Appendix B.

$$E_{on-switching-\chi} = a2 \times I_{turn-on} + b2 \tag{3.4}$$



(a)



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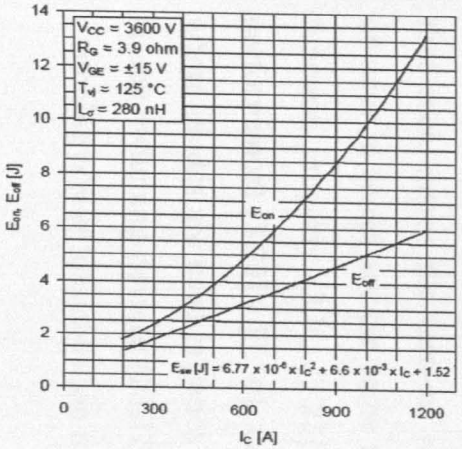


(c)

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Turn-on delay time	t_{don}	V_D = 2800 V, T_j = 125 °C			3.5	µs
Turn-on delay time status feedback	$t_{don\,SF}$	I_T = 4000 A, di/dt = V_D / L_i L_i = 5 µH C_{CL} = 10 µF, L_{CL} = 0.3 µH			7	µs
Rise time	t_r				1	µs
Turn-on energy per pulse	E_{on}				1.5	J

(d)

Figure 3.7: Relation between on-switching energy and turn-on current
(a) 6.5 kV SGCT [3.29], (b) 4.5 kV HVIGBT [3.26], (c) 6.5 kV HVIGBT [3.30], and (d) 4.5 kV AGCT [3.28].

3. All the turn-on relations are scaled by the ratio of the actual device voltage (commutation voltage) and the data sheet voltage (turn-on test voltage). When series devices are used in the half leg (to achieve the required blocking voltage), it is assumed that each shares the turn-on voltage according to its impedance. Since the utilized devices in series are the same type and the voltage sharing circuits are considered to function properly [3.1], [3.23] (active gate control can be used instead for better performance) [3.33] - [3.36], the voltage distribution is assumed uniform. In the case where diodes are used in series with IGBTs/AGCTs, the turn-on voltage appears only on the switching devices (IGBT/AGCT) as shown in figure 3.8. The compensated on-switching power loss equation for each device is given in (3.5).

$$P_{on-switching-\chi} = (a2 \times I_{turn-on} + b2) f_{fundamental} \left(\frac{\sum_{i=1}^{11} V_{switch}(i)}{V_{data\ sheet\ test}} \right) \tag{3.5}$$

where $V_{switch}(i)$ is the voltage across the switching device at the turn-on instant. This voltage is calculated from the switching curves in figure 3.4 and the voltage sharing as shown in figure 3.8. The term 'i' represents the index of the turn-on instant. It is varying from 1 to 11 since SHE is used to eliminate harmonics up to the 11^{th} and consequently the device is subjected to eleven turn-on's per cycle.

4. The on-switching loss is calculated from (3.5) taking into account the device configuration at each voltage level. For a DC-link current from 100 A to 600 A, the on-switching loss variation with the DC- link current per half leg for different voltage levels and device configurations, is shown in figure 3.9.

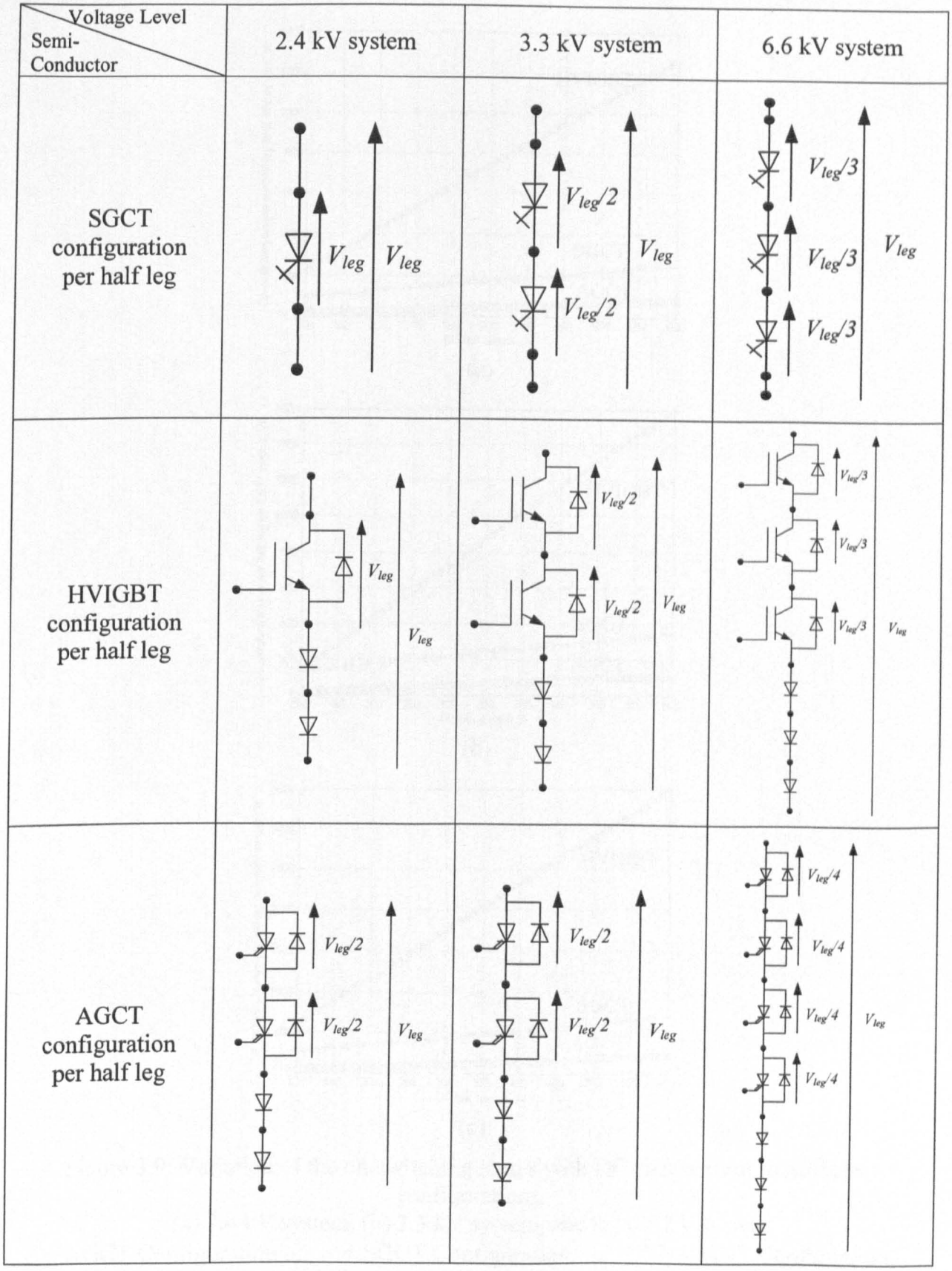
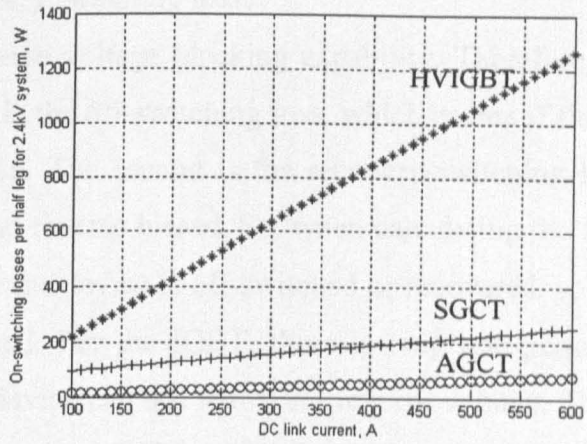
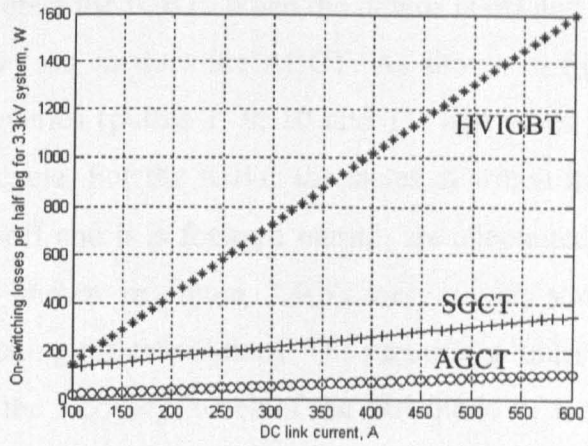


Figure 3.8: Voltage sharing per half leg in PWM CSR for different semiconductor configurations and voltage levels during turn-on/turn-off.
[Turn-on occurs at rising edges of pulses 1 to 11. Turn-off occurs at falling edges of pulses 2 to 8. Refer to figure 3.4]



(a)



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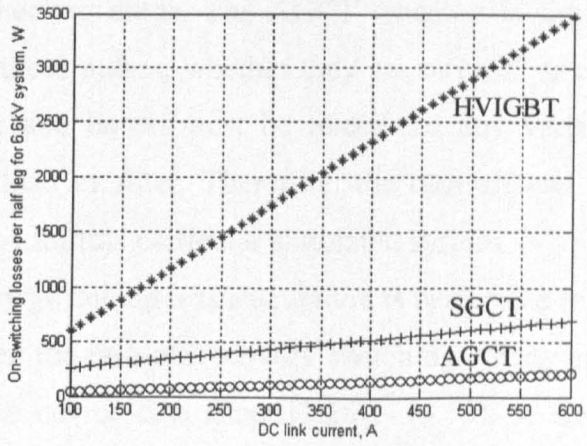


(c)

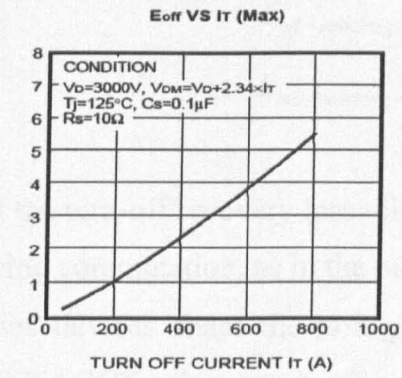
Figure 3.9: Variation of the on-switching losses with DC-link current for different configurations.
(a) 2.4 kV system, (b) 3.3 kV system, and (c) 6.6 kV system
o AGCT Configuration + SGCT Configuration * HVIGBT Configuration

ii. Off / Recovery switching losses

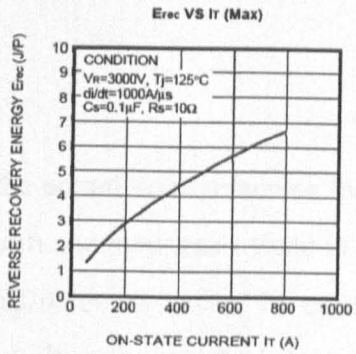
The SGCT has reverse voltage blocking capability. Therefore, it has two turn-off loss possibilities. The first is the off-switching loss, which occurs if the device is turned off and remains forward biased. The second is the recovery-switching loss, which occurs if the device is turned off and reverse biased. So, when calculating the turn-off losses, care must be taken as to whether the device is off-switched or recovered, so that the appropriate data sheet loss curve is used. For the IGBT, there is only one possibility, which is the off-switching loss as the device can not withstand reverse voltage. Therefore, for applications requiring reverse voltage capabilities like the CSR, series diodes are used to block the reverse voltage and protect the IGBT. When the device is off and reverse biased, the series diode suffers recovery loss, as does the AGCT. As shown in figure 3.4(a), the SGCT is subjected to four recoveries (pulses 1, 9, 10 and 11) and seven turn-offs (pulses 2 to 8) during one complete cycle. For the IGBT, the states at which the current is commutated due to switching turn-off and it is forward biased, are accounted for in the off-switching loss calculations. As shown in figure 3.4(b), only seven states (pulses 2 to 8) are considered in the switching off calculations. The remaining four states (pulses 1, 9, 10 and 11) are considered in the recovery losses of the fast diode in series with IGBT. At these transients, the IGBT has a small negative voltage across its terminal which is the on-state voltage of the free-wheeling diode. The AGCT situation is similar to that of the IGBT. Note that the state of these pulses, whether they are turn-off or recovery, is dependant on the load power factor and hence must be traced for any variation from the simulated system like the CSR load or filter. Therefore, the turn-off and recovery losses instants, from 1 to 11, are unique for this particular simulated system

The turn-off/recovery switching loss calculation is performed in the following steps:

1. The relation between the turn-off/recovery switching energy and the turn-off current is determined from the device data sheet [3.26] - [3.31], as shown in figure 3.10. The device data sheets in figure 3.10 parts (f) and (g) for the series diodes are linearized by interpolation due to the lack of data sheet curves.
2. The turn-off loss and the recovery loss relations are linearized to simplify the calculations as described in (3.6) and (3.7). The current substituted into (3.6) and (3.7) is the peak current at the instant of the turn-off/recovery where the constants 'χ', '$a3$', '$b3$', '$a4$' and '$b4$' are listed in Appendix B.



(a)



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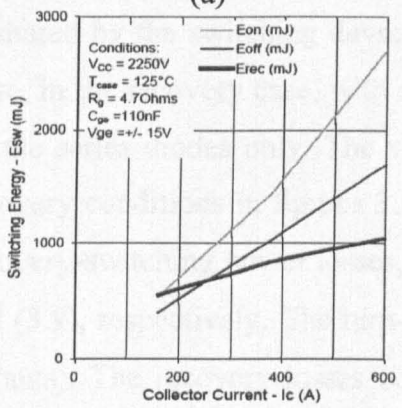
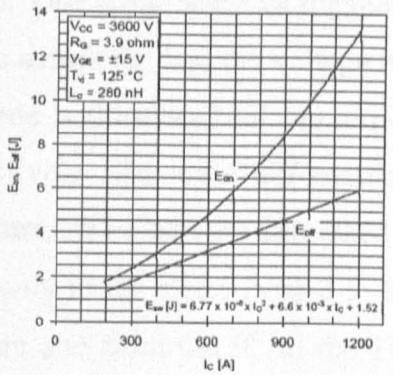
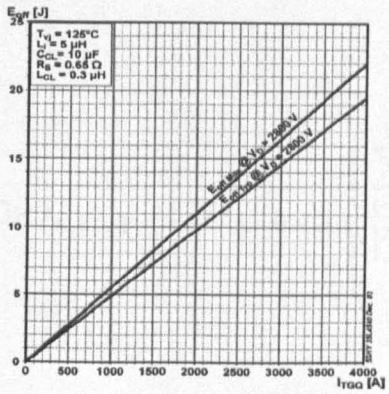


(c)



(d)



(e)

T_{case} = 125°C unless stated otherwise.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{rr}	Peak reverse recovery current	I_F = 600A,	-	820	-	A
Q_{rr}	Reverse recovery charge	dI_F/dt = 3000A/μs,	-	850	-	μC
E_{rec}	Reverse recovery energy	V_R = 2250V	-	1050	-	mJ

(f)

Turn-off

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery current	I_{RM}	di/dt = 300 A/μs, I_{TQ} = 1000 A,			1000	A
Reverse recovery charge	Q_{rr}	T_j = 125°C, V_{RM} = 2900 V,			6000	μC
Turn-off energy	E_r	C_S = 3 μF (GTO snubber circuit)			5	J

(g)

Figure 3.10: Relation between off/recovery switching energy and turn-on current (a) 6.5 kV SGCT [3.29], (b) 6.5 kV SGCT [3.29], (c) 4.5 kV HVIGBT [3.26], (d) 6.5 kV HVIGBT [3.30], (e) 4.5 kV AGCT [3.28], (f) 4.5 kV Fast diode [3.27], and (g) 6 kV Fast diode [3.31].

$$E_{off-switching-\chi} = a3 \times I_{turn-off} + b3 \tag{3.6}$$

$$E_{rec-switching-\chi} = a4 \times I_{turn-off} + b4 \tag{3.7}$$

3. All the turn-off/recovery loss relations are scaled to the actual voltage across the device during commutation, as in the on-switching loss section. An important issue is how the series devices share the voltage during the turn-off/recovery state. In case of the IGBT/AGCT, when a turn-off occurs, with a positive voltage across the leg, the voltage is shared by the switching devices (IGBT/AGCT). This is the same as for the turn-on state. In the recovery case, with a negative voltage across the leg, the voltage is shared by the series diodes only. The voltage sharing issue is illustrated for the turn-off and recovery conditions in figures 3.8 and 3.11 respectively. The scaled off-switching and recovery-switching power losses, as a function of turn-off current are expressed in (3.8) and (3.9), respectively. The turn-off losses occur only in the states from 2 to 8 (seven instants). The recovery losses occur in the 1st state and from the 9th to the 11th state (four states), as shown in figure 3.4.

$$P_{off-switching-\chi} = (a3 \times I_{turn-off} + b3) f_{fundamental} \left(\frac{\sum_{i=2}^{8} V_{switch}(i)}{V_{data\ sheet\ test}} \right) \tag{3.8}$$

$$P_{rec-switching-\chi} = (a4 \times I_{turn-off} + b4) f_{fundamental} \left(\frac{\sum_{i=1,9,10,11} V_{switch}(i)}{V_{data\ sheet\ test}} \right) \tag{3.9}$$

4. The off/recovery switching losses are calculated by substitution into (3.8) and (3.9) taking into account the device configuration used at each voltage level. For DC-link currents of 100 A to 600 A, the variation of off/recovery switching losses with DC-link current per half leg for different voltage levels and device configurations, are shown in figure 3.12.

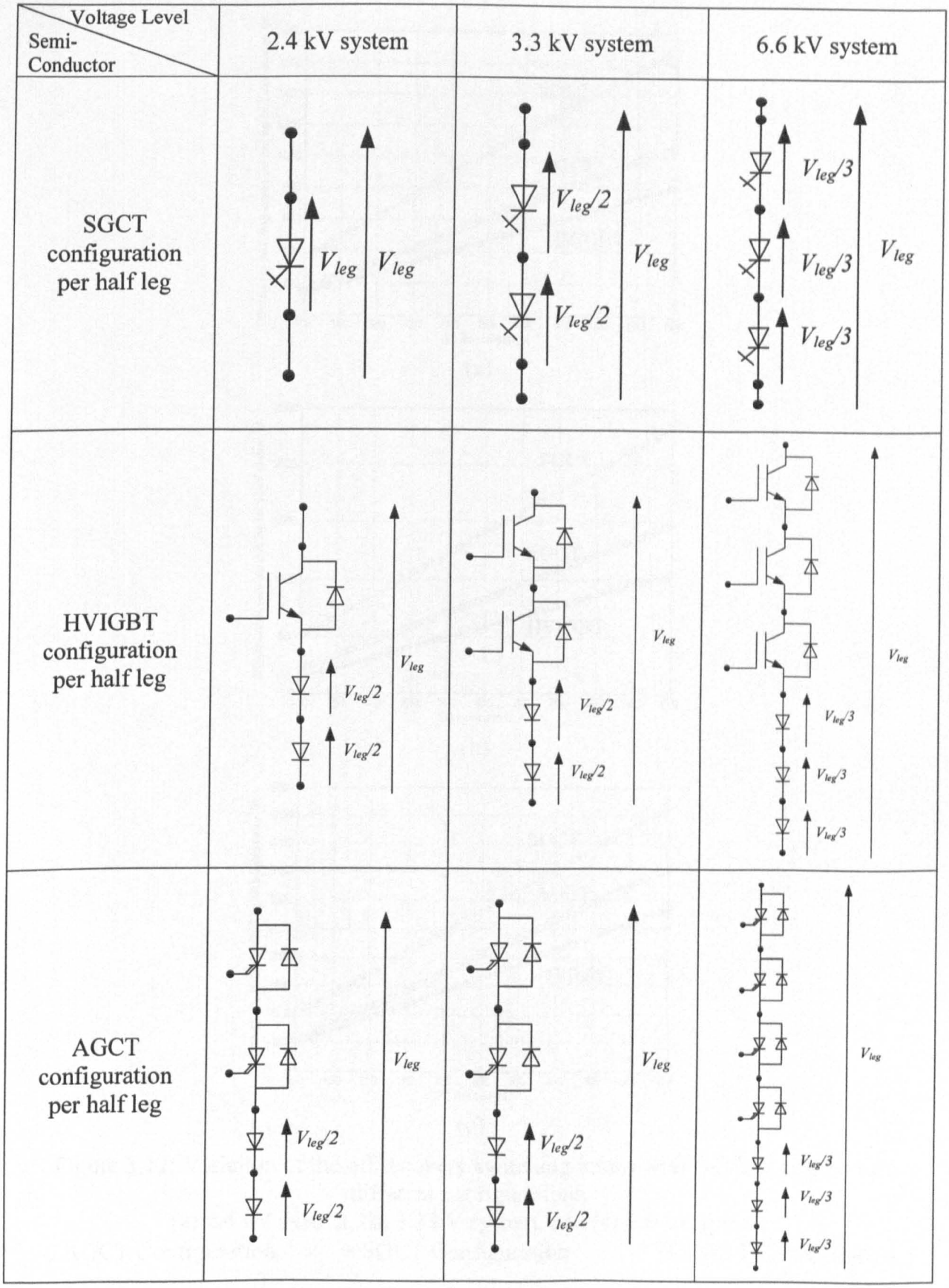
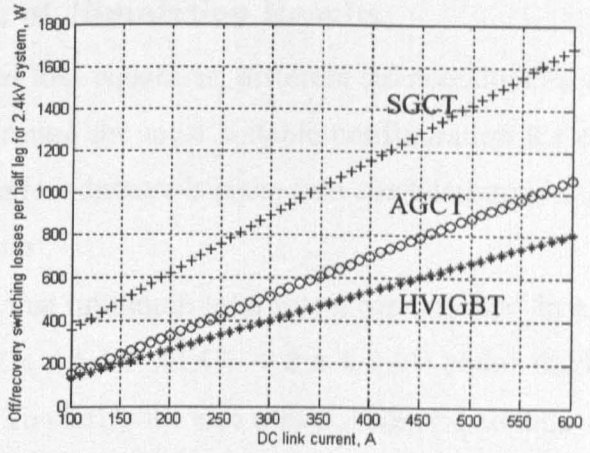
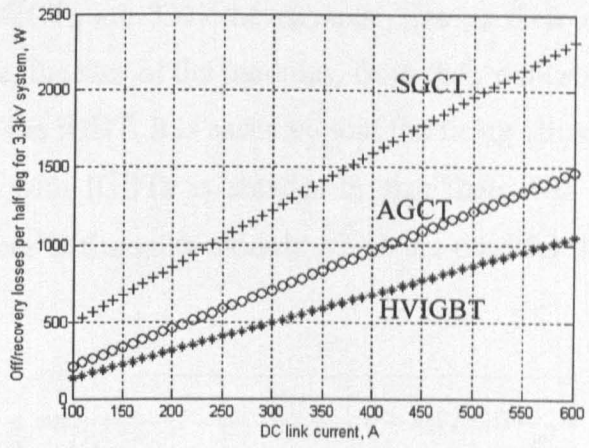


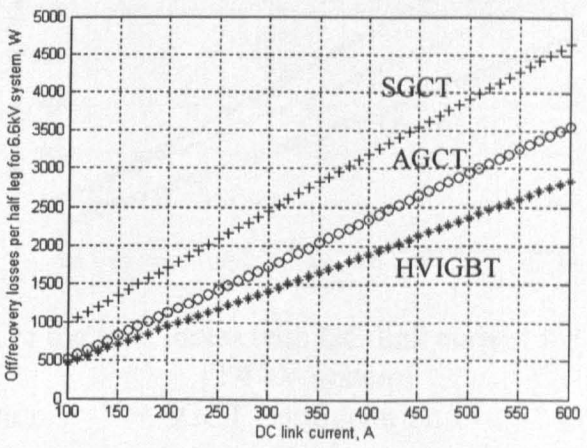
Figure 3.11: Voltage sharing per half leg in PWM CSR for different semiconductor configurations and voltage levels during recovery.
[Recovery occurs at falling edges of pulses 1,9,10, and 11. Refer to figure 3.4]



(a)



(b)



(c)

Figure 3.12: Variation of the off/recovery switching losses with DC-link current for different configurations.
(a) 2.4 kV system, (b) 3.3 kV system, and (c) 6.6 kV system
o AGCT Configuration + SGCT Configuration * HVIGBT Configuration

3.4 Comparison of Simulation Results

Using the presented loss equations, different semiconductors are compared from a loss point of view, to determine the most suitable configuration for each MV level. Also, the physical size of the semiconductors is taken into consideration in the following sections.

i. 2.4 kV system

Figure 3.13 shows that minimum total losses are acquired in a 2.4 kV system using the AGCT combination (2 x 4.5 kV AGCT + 2 x 4.5 kV series diodes) for DC-link currents from 100 A to 600 A. To clarify the size aspect, referring to data sheets [3.27] - [3.30], the size of the rectifier half leg is shown in table 3.4.

Rectifiers using SGCTs are 33% the physical size of their AGCT equivalent. In the SGCT and AGCT case, the size of the modules, from their data sheets, includes the built-in gate firing circuit. For the IGBT, it is assumed that the firing circuit is half the module size. The overall topology with IGBTs is smaller in size than with SGCTs since the IGBT module has three devices in the same module which are used for the other rectifier legs.

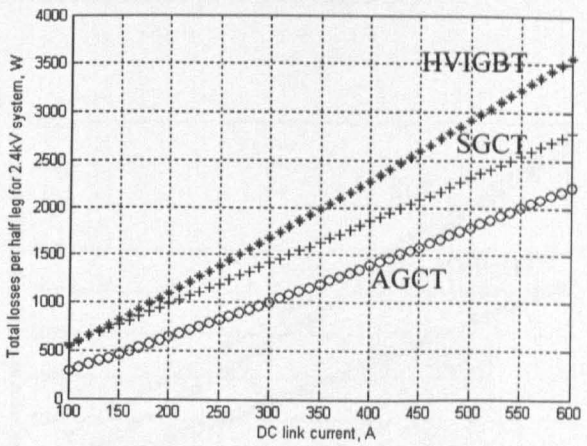


Figure 3.13: Variation of the total losses with DC-link current for different configurations. [2.4 kV system]

o AGCT Configuration + SGCT Configuration * HVIGBT Configuration

Table 3.4: Size calculation for 2.4 kV systems

Configuration	*SGCT*	*AGCT*	*HVIGBT*
Switching devices required	1	2	1
Switching devices per module	1	1	3
Module footprint (mm^2)	$52x10^3$	$76x10^3$	$26.6 x10^3$
Series diodes required	0	2	2
diodes per module	-	2	2
Module size (mm^2)	-	$16.1 x10^3$	$16.1 x10^3$
Total size (mm^2)	$52 x10^3$	$168 x10^3$	$29.4 x10^3$

ii. 3.3 kV system

Figure 3.14 shows that minimum losses occur for the AGCT combination (2 x 4.5 kV AGCT and 2 x 4.5 kV series diodes). The AGCT and IGBT configurations utilize the same type of series diodes. But the conduction losses and the on-switching losses of the AGCT are lower than those of the IGBT, as shown previously in figures 3.6(b) and 3.9(b) respectively, while off/recovery losses of the IGBT configuration is the lowest, as shown in figure 3.12(b). From a size point of view, referring to data sheets [3.28] - [3.31], the rectifier half leg size is calculated as given in table 3.5.

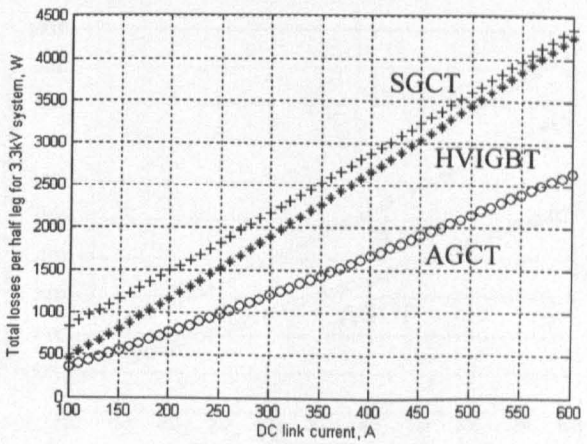


Figure 3.14: Variation of the total losses with DC-link current for different configurations. [3.3 kV system]

o AGCT Configuration + SGCT Configuration * HVIGBT Configuration

Table 3.5: Size calculation for 3.3 kV systems

Configuration	*SGCT*	*AGCT*	*HVIGBT*
Switching devices required	2	2	2
Switching devices per module	1	1	2
Module footprint (mm^2)	52 x10^3	76 x10^3	16.12 x10^3
Series diodes required	0	2	2
diodes per module	-	2	2
Module size (mm^2)	-	16.1 x10^3	16.1 x10^3

The IGBT configuration has the smallest size. It makes the overall rectifier physical size 23% that when using AGCTs. Over the current range, the AGCT is the best from the loss point of view, the IGBT is the best from a size point of view, and the SGCT is the best from the lowest number of devices aspect.

iii. 6.6 kV system

Figure 3.15 shows that minimum losses result when using the AGCT combination (4 x 4.5 kV AGCT and 3 x 6 kV series diodes) with the disadvantage of having seven devices in series per half leg. From the size point of view, the IGBT configuration is the smallest. The size of the rectifier half leg is shown in table 3.6, [3.28] - [3.31].

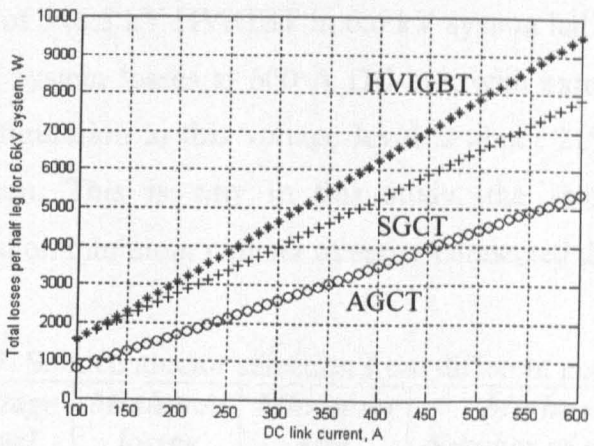


Figure 3.15: Variation of the total losses with DC-link current for different configurations. [6.6 kV system]

o AGCT Configuration + SGCT Configuration * HVIGBT Configuration

Table 3.6: Size calculation for 6.6 kV systems

Configuration	*SGCT*	*AGCT*	*HVIGBT*
Switching devices required	3	4	3
Switching devices per module	1	1	3
Module footprint (mm^2)	52×10^3	76×10^3	26.6×10^3
Series diodes required	0	3	3
diodes per module	-	1	1
Module size (mm^2)	-	7×10^3	7×10^3

Discussion

The results of the calculations and comparisons are summarized in table 3.7. As would be expected, the SGCT always yields a minimum number of devices since it has inherent reverse voltage blocking properties. Error is minimal in the proposed generic procedure since calculations are based on practical data sheets and point by point utilization of loss curves. The only source of deviation from the presented results is due to the variation of the switching conditions (temperature, values of snubber networks, gating resistance, etc.) from the selected typical conditions [3.37], [3.38]. The usage of lower voltage semiconductors with more devices in series result in lower losses but with the penalty of increasing the system size, number of devices and cost. As an example, the usage of 4x4.5 kV HVIGBT instead of 3x6.5 kV HVIGBT in 6.6 kV system half-leg results in only 11 % reduction in the total system losses at 600 A DC-link with extra six 4.5 kV HVIGBTs while the SGCT configuration in this voltage level is about 21% lower than 3x6.5 kV HVIGBT configuration. This is why in this study, the selection of the compared configurations is based on minimum number of series connected devices.

Table 3.7: Semiconductor selection from different points of view

Voltage level	*Minimum losses*	*Minimum size*	*Minimum Number of devices*
2.4 kV	AGCT	HVIGBT	SGCT
3.3 kV	AGCT	HVIGBT	SGCT
6.6 kV	AGCT	HVIGBT	SGCT

Summary

Nine configurations with different semiconductors for MV PWM CSRs have been analyzed in terms of losses and physical size. The constant voltage dependant data sheet curves are adapted to suit voltage varying applications with voltage sharing of series semiconductors in all commutation states. For each voltage level, there is a best semiconductor combination from a loss point of view. This selection may not meet other requirements, like minimum size and number of devices. The selection varies with the working voltage level and configuration.

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CHAPTER FOUR:

Vector Controlled PWM VSI Induction Motor Drive with a Long Motor Feeder

Recent developments in power electronics enable the use of adjustable speed drives (ASD's) in medium voltage applications. Such PWM drives are used in applications including pumps, compressors, fans, etc. for efficiency improvement and energy savings. The drive may be located remote from the motor, kilometres away, as in the case of electrical submersible pumps (ESP's), ventilation fans, and conveyers in underground mines [4.1] - [4.3]. Many practical problems occur in VSI long motor feeder drives. Among them, motor terminal over-voltage due to the travelling voltage waveform phenomena created by the feeder distributed impedance. To address such a problem, modelling of the feeder and the drive system should be performed. Since the over-voltage problem is related to the use of a feeder on the VSI output, filter networks are mandatory. In this chapter, the performance of a vector controlled PWM voltage source drive is investigated under the influence of a long motor feeder and filter. Emulation of the MV long motor feeder in the experimental low-voltage system is based on percentage voltage regulation. The medium-voltage drive system is scaled to a low-voltage system. Two filter topologies are compared: a motor terminal *RC* filter and an inverter output *RLC* filter. This chapter studies the effects of such filters and compares the system performance in each case. The drive performance study considers no-load/load conditions in terms of line voltage and current harmonics, effects on flux and torque current components, DC-link current harmonics, and common-mode voltage. The effects of feeder length on filter losses, DC-link current and voltage regulation are also investigated. The performance evaluation is carried out experimentally and by simulation, taking into account switching frequency limitations in MV drives.

The chapter is organized into four sections where the first section is concerned with the implemented vector control technique, the long feeder model, and the problems associated with long feeder applications. The filter techniques under study are illustrated in section two. Section three presents the effect of the two filtering techniques on drive performance [motor terminal voltage, *d*-axis motor current, *q*-axis motor current, motor line current,

speed-step response, sudden load torque response, DC-link current, and common mode voltage]. Finally the effects of feeder length on filter losses, DC-link current, and voltage regulation are studied.

4.1 Vector Control System

The system under investigation is a rotor flux based vector control induction motor drive whose block diagram is shown in figure 4.1. Currents supplied to the machine should be orientated in-phase and in-quadrature to the rotor flux vector where the rotor flux is aligned with the *d*-axis.

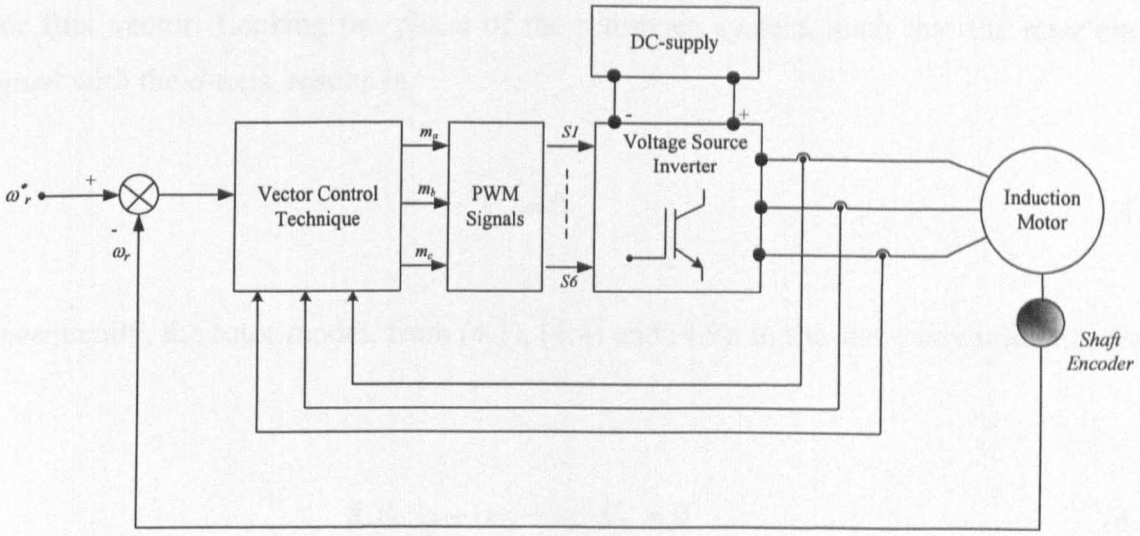


Figure 4.1: Block diagram of a voltage source PWM vector controlled induction motor drive.

Indirect vector control is based on five equations, two stator equations, two rotor equations, and the torque equation [4.2], [4.3]:

$$v^e_{m\_qs} = R_s i^e_{m\_qs} + p\lambda^e_{qs} + \omega_e \lambda^e_{ds} \tag{4.1}$$

$$v^e_{m\_ds} = R_s i^e_{m\_ds} + p\lambda^e_{ds} - \omega_e \lambda^e_{qs} \tag{4.2}$$

$$v^e_{m\_qr} = R_r i^e_{m\_qr} + p\lambda^e_{qr} + (\omega_e - \omega_r)\lambda^e_{dr} = 0 \tag{4.3}$$

$$v^e_{m\_dr} = R_r i^e_{m\_dr} + p\lambda^e_{dr} - (\omega_e - \omega_r)\lambda^e_{qr} = 0 \tag{4.4}$$

$$T = \frac{3}{2}\frac{P}{2}\frac{L_m}{L_r}(\lambda^e_{dr} i^e_{m\_qs} - \lambda^e_{qr} i^e_{m\_ds}) \tag{4.5}$$

where the stator and rotor flux linkage are described by:

$$\lambda_{ds}^{e} = L_{ds} i_{m\_ds}^{e} + L_m i_{m\_dr}^{e} \tag{4.6}$$

$$\lambda_{qs}^{e} = L_{qs} i_{m\_qs}^{e} + L_m i_{m\_qr}^{e} \tag{4.7}$$

$$\lambda_{dr}^{e} = L_{dr} i_{m\_dr}^{e} + L_m i_{m\_ds}^{e} \tag{4.8}$$

$$\lambda_{qr}^{e} = L_{qr} i_{m\_qr}^{e} + L_m i_{m\_qs}^{e} \tag{4.9}$$

Currents supplied to the machine should be orientated in-phase and in-quadrature to the rotor flux vector. Locking the phase of the reference system, such that the rotor flux is aligned with the *d*-axis, results in

$$\lambda_{qr}^{e} = 0 \tag{4.10}$$

Consequently, the rotor model, from (4.3), (4.4) and (4.9), in the stationary reference frame is:

$$R_r i_{m\_qr}^{e} + (\omega_e - \omega_r)\lambda_{dr}^{e} = 0 \tag{4.11}$$

$$R_r i_{m\_dr}^{e} + p\lambda_{dr}^{e} = 0 \tag{4.12}$$

$$\lambda_{qr}^{e} = L_{qr} i_{m\_qr}^{e} + L_m i_{m\_qs}^{e} = 0 \tag{4.13}$$

Hence $$i_{m\_qr}^{e} = -\frac{L_m}{L_r} i_{m\_qs}^{e} \tag{4.14}$$

Therefore the electromagnetic torque is expressed as

$$T = \frac{3}{2}\frac{P}{2}\frac{L_m}{L_r}(\lambda_{dr}^{e} i_{m\_qs}^{e}) \tag{4.15}$$

Equations (4.11) to (4.15) represent the dynamic response of the field orientated controlled induction machine with respect to rotor flux.

From (4.11), the slip relation can be written as

$$\omega_e - \omega_r = s\omega_e = -\frac{R_r i^e_{m\_qr}}{\lambda^e_{dr}} \tag{4.16}$$

From (4.14) and (4.16), the slip speed, as a function of the rotor flux *d*-axis component and the stator current *q*-axis component, can be expressed as

$$s\omega_e = \frac{R_r L_m i^e_{m\_qs}}{L_r \lambda^e_{dr}} \tag{4.17}$$

From (4.8), the rotor current *d*-axis component can be represented by

$$i^e_{m\_dr} = \frac{\lambda^e_{dr} - L_m i^e_{m\_ds}}{L_r} \tag{4.18}$$

Combining (4.12) and (4.18), the rotor flux *d*-axis component can be expressed as a function of the stator current *d*-axis component:

$$\lambda^e_{dr} = \frac{R_r L_m i^e_{m\_ds}}{(R_r + L_r p)} \tag{4.19}$$

In steady-state, the rotor flux *d*-axis component is a DC quantity, hence, its derivative tends to zero.

$$\lambda^e_{dr} = L_m i^e_{m\_ds} \tag{4.20}$$

From (4.20), it can be concluded that the rotor flux can be controlled by varying the stator current *d*-axis component. By substitution into (4.15), the electromagnetic torque as a function of the *d*-*q* motor components, in the synchronously rotating reference frame, is

$$T = \frac{3}{2}\frac{P}{2}\frac{L_m^2}{L_r}(i^e_{m\_ds} i^e_{m\_qs}) \tag{4.21}$$

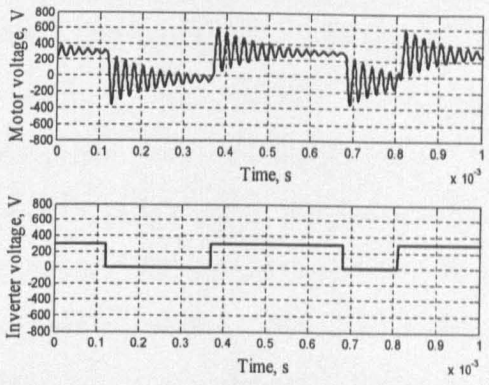
Since the machine operates with rated flux in the constant torque operating region (like the DC machine), the *d*-axis motor current component is constant. Hence, the electromagnetic torque can be controlled by varying the stator current *q*-axis component. Therefore, from (4.20) and (4.21), field orientation and decoupling are achieved as the flux and torque can be controlled by two orthogonal independent current components (*d*-axis and *q*-axis).

4.2 Problems associated with a Long Motor Feeder PWM VSI Drive

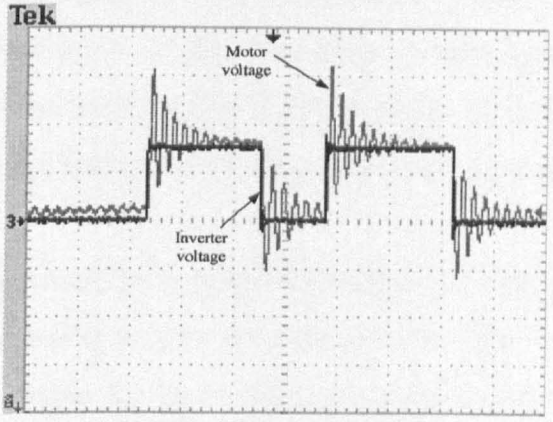
The motor and drive connection via a long feeder incurs some problems, mainly a travelling wave phenomenon that causes doubling and ringing of the motor terminal voltage. This ringing is caused by the distributed *LC* line impedance and the fast rise time of the inverter voltage [4.4], [4.5]. Moreover, the voltage drop along the feeder causes starting problems, especially with high inertia motor loads [4.6]. The high *dv/dt* of the inverter voltage has adverse effects on motor insulation and contributes to bearing currents and EMI problems [4.7]. De-rating of motors is mandatory, the extent of which is a function of feeder length and inverter switching frequency [4.8]. Another problem is the common mode voltage which contributes to the flow of a high frequency current in the motor bearings through parasitic capacitances [4.7], [4.8]. Various models predict the effect of the resultant shaft voltage [4.9]. There are many parasitic parameters that affect motor performance in the case of travelling waves and/or shaft voltages, and accurate measurement techniques are needed to obtain model values [4.10]. EMC problems are severe when low cost unshielded feeders are used [4.11]. The probability of resonance with a long feeder is common, especially when a step down transformer is used which resonantly amplifies the motor terminal voltage. So, precise on-site impedance measurements are needed to ascertain the reason for the voltage gain, namely whether it is due to travelling waves or resonance or a combination of both [4.12].

To address the over-voltage problem with long motor feeder VSI drives, a scaled low voltage drive system is tested to operate the motor via a 1 km feeder at 300 rpm with a 300 V DC-link bus and a 1 kHz switching frequency. Simulation, using MATLAB SIMULINK package and experimental results are shown in figure 4.2. The motor and feeder parameters are listed in Appendices C and D respectively. The simulation results for the inverter output and the motor terminal voltages are shown in figure 4.2(a), to clarify the over-

voltage problem and illustrate the ringing feature of the voltage waveforms. Experimental results corresponding to simulation results are shown in figure 4.2 part (b).



(a)



[200 V/div, 0.1 ms/div]

(b)

Figure 4.2: Simulation and experimental results of motor and inverter voltages for a voltage source vector controlled drive with a one kilometre feeder, without any filter network

[(a) Simulation results (b) Experimental results]

Form figure 4.2 parts (a) and (b), it can be seen that the motor terminal voltage reaches near double the inverter voltage due to the travelling wave phenomena accompany the use of a long feeders with the VSI. Moreover, the ringing nature of the motor terminal voltage is clearly seen.

Since the over-voltage problem, in VSI long motor feeder drives, is related to the feeder distributed impedance, modelling of the feeder is mandatory to study this phenomenon.

4.3 Long Feeder Model

The analysis and mitigation of the problems associated with long feeder drives needs reliable modelling of the complete drive system, especially the feeder. Although frequency domain analysis is a powerful tool in feeder modelling [4.13], lumped L and C elements can represent the feeder, even for transient analysis [4.14]. To access voltages and currents in the drive system accurately, frequency dependant models should be used [4.15]. An on-line feeder parameter estimation technique is possible [4.16], [4.17]. Also, more accurate results are obtained [4.18] when a frequency dependant lumped segment model is used. Wavelet analysis has been used to develop a precise off-line wavelet based feeder model [4.19]. Modelling of the high frequency parasitic current paths is needed to analyze the whole drive system [4.20]. Even the feeder insulation plays a role in the over-voltage problem due to the dependency of the distributed feeder inductance and capacitance parameters on the insulation structure [4.21]. Other feeder models depend on a set of time varying equations which are helpful for voltage computation at any point along the feeder [4.22].

In this chapter, a π-network with lumped elements is used to model the long motor feeder. This model is sufficient to give accurate results at the feeder terminals, even for transient analysis [4.14]. Figure 4.3 shows the long feeder π-network model. Based on this model, a prototype for the feeder model is experimentally implemented using lumped elements. The simulated feeder is a PWM special insulation reinforced three phase cable with low shunt capacitance. The feeder parameters are listed in Appendix D. Simulations and experimental results in this and subsequent chapters use and are based on this model.

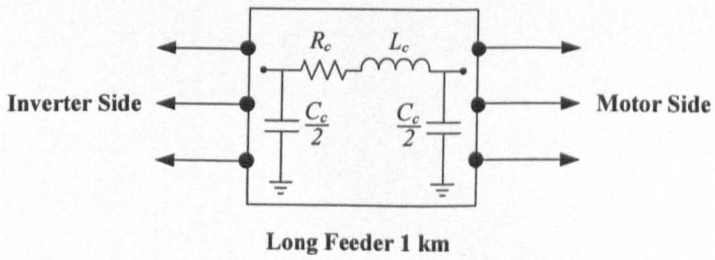


Figure 4.3: π-model for a long motor feeder representation.

4.4 Filter Techniques

Several filter topologies have been developed to improve drive power quality and decrease the long feeder effects on the motor due to fast switching inverter voltages. First and second order motor terminal filters have been compared [4.23] and an inverter output *RLC* filter has been assessed [4.24]. An input/output filter, with a DC-link interconnection, was developed to reduce the common mode voltage [4.25]. Connection of the conventional inverter output filter common point to the DC-link mid-point reduces the common mode voltage [4.26]. An *LC* resonance filter with a diode bridge may be used but is limited to low voltage drives [4.27]. A common mode transformer, with a conventional inverter output filter, mitigates common mode currents [4.28].

Although different filter topologies have been compared [4.29] and the impact of the long feeder drive system on the distribution of the stator voltage was studied [4.30], little research has been dedicated to analysing the effects of the filter networks on a vector controlled long feeder drive system.

In this chapter, two filter networks are selected to mitigate the effects of long feeders. First, an *RC* filter is used at the motor terminals [4.23] and second, an *RLC* filter is used at the inverter output [4.24], [4.29]. The following sections describe each filter topology, theory of operation, governing equations and a sample simulation and experimental result, to confirm its function.

4.4.1 Motor terminal *RC* filter

The motor terminal *RC* filter design relies on the fact that the motor terminal over-voltage can be reduced if the feeder is terminated by impedance equivalent to the feeder surge impedance. The filter topology is shown in figure 4.4.

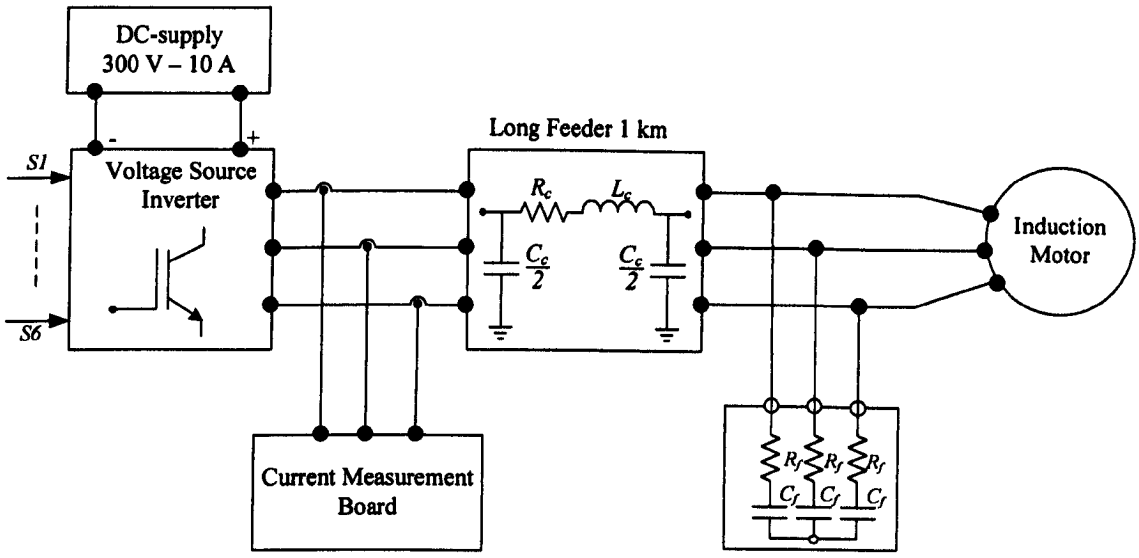


Figure 4.4: Motor terminal *RC* filter topology.

The filter impedance is designed to match the feeder surge impedance [4.23].

$$z_o = \sqrt{(R_f)^2 + \left(\frac{1}{sC_f}\right)^2} \tag{4.22}$$

$$z_o = \sqrt{\frac{L_c}{C_c}} \tag{4.23}$$

Initially, at each voltage edge (rising or falling), the filter capacitor behaves as a short circuit. Therefore the matching equation is reduced at each incident voltage wave to [4.23]:

$$z_o = R_f \tag{4.24}$$

It can be shown that for a 20% rise in the steady-state motor terminal voltage, the filter capacitance requirement is [4.23]

$$C_f = 4.484\ l_c C_c \tag{4.25}$$

From (4.24) and (4.25), filter resistance selection is only dependant on the feeder characteristics while the filter capacitance is a function of the feeder characteristics and length.

The performance of motor terminal *RC* filter networks on the motor voltage is studied by examining the drive system under the same conditions as in section 4.2. Simulation and experimental results are shown in figure 4.5. The inverter output voltage and motor terminal voltage in the case of a 1 km feeder and a motor terminal *RC* filter, is shown in figure 4.5(a) for 2 cycles of simulation, with a zoomed simulation result in figure 4.5(b). Experimental results for the simulated results are shown in figure 4.5 parts (c) and (d).

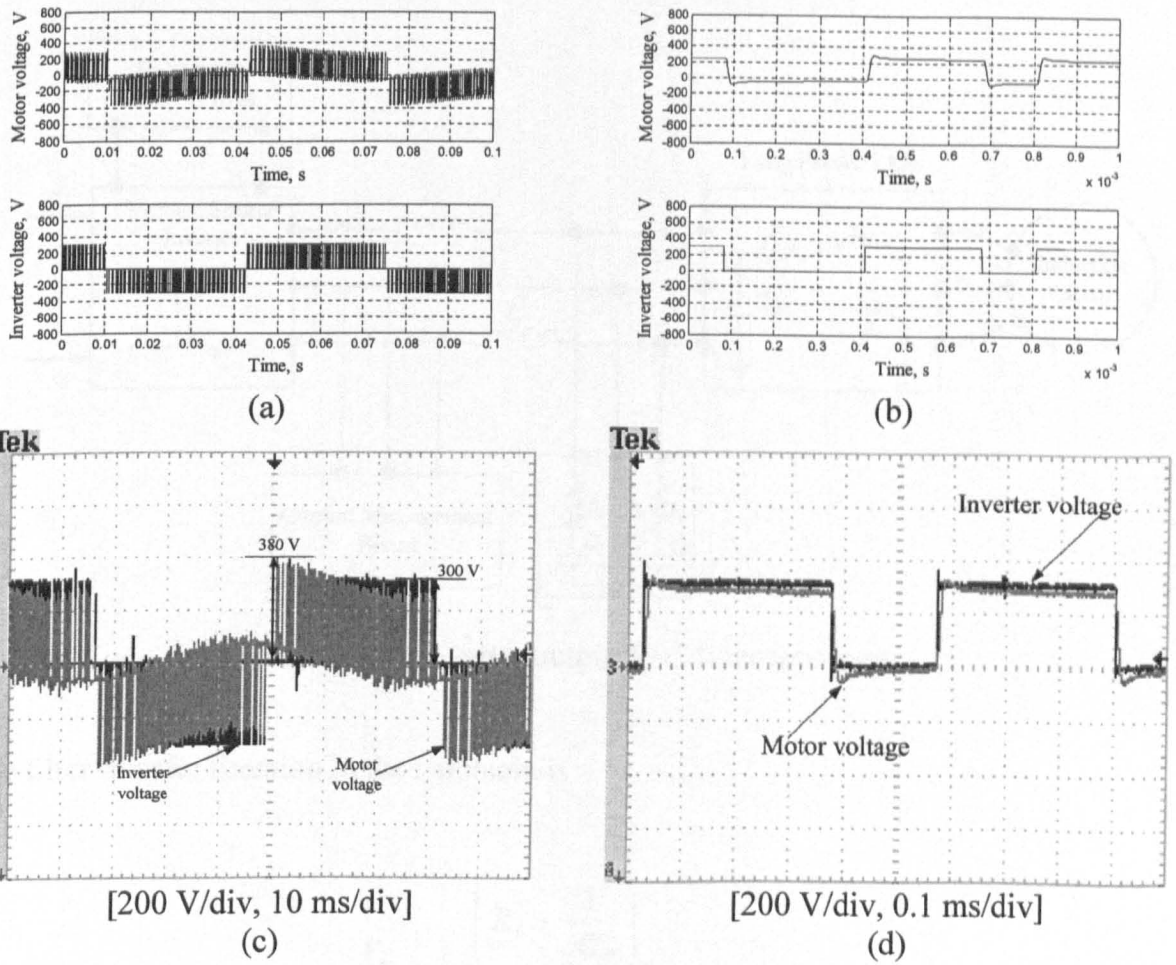


Figure 4.5: Simulation and experimental results of motor and inverter voltages with a one kilometre feeder using a motor terminal *RC* filter

[(a)-(b) Simulation results (c)-(d) Experimental results]

(a) motor/inverter voltage with long feeder and *RC* filter, (b) zoom for case (a), (c) motor/inverter voltage with long feeder and *RC* filter, and (d) zoom for case (c).

As shown in figure 4.5 parts (a) and (c), the over-voltage at the motor terminals is limited due to the insertion of the filter network. Also, the motor terminal voltage does not ringing, unlike the case without a filter, as shown in figure 4.5 parts (b) and (d).

4.4.2 Inverter output *RLC* filter

Motor terminal voltage increase is a function of the feeder type, feeder length, and the rise time of the inverter output voltage pulses. If the inverter voltage rise time is less than a critical time, which is function of the feeder type and length, the motor voltage can be doubled. The *RLC* filter increases the inverter voltage rise time to limit the motor voltage increase. The filter design is based on (4.26) to (4.30) [4.24], [4.29] and the filter topology is shown in figure 4.6.

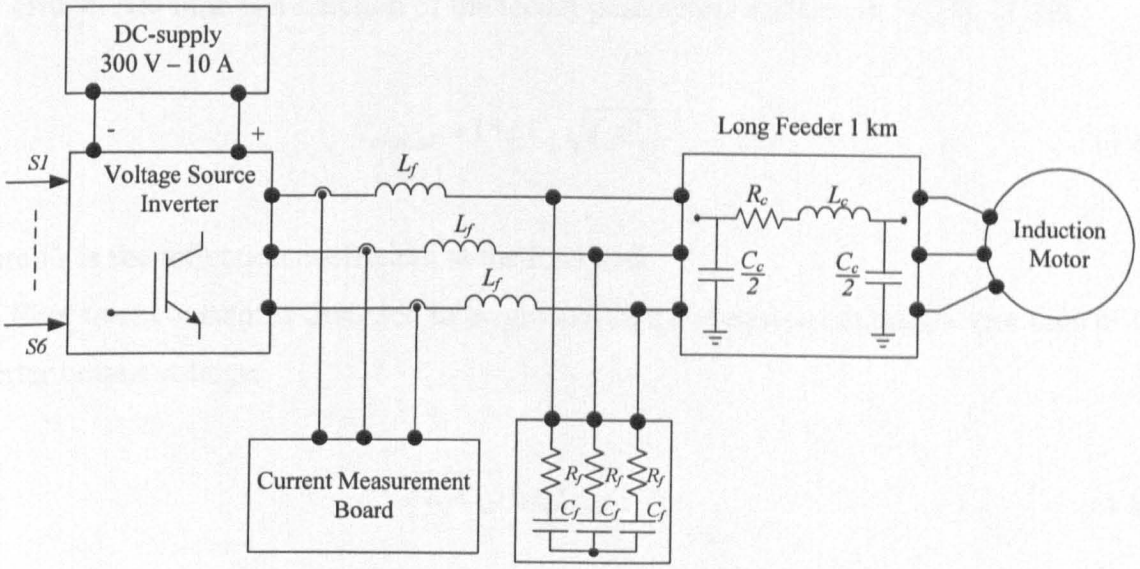


Figure 4.6: Inverter output *RLC* filter topology.

The filter transfer function in the *s*-domain is

$$\frac{V_o}{V_i} = \frac{\left(R_f + \frac{1}{sC_f}\right)}{\left(R_f + \frac{1}{sC_f} + sL_f\right)} \tag{4.26}$$

The characteristic equation of the filter transfer function is

$$s^2 + s\left(\frac{R_f}{L_f}\right) + \frac{1}{L_f C_f} = 0 \tag{4.27}$$

For an over-damped response, the roots of the characteristic equation must be real and negative when the discriminant is zero. Therefore the filter resistance is designed such that

$$R_f = 2\sqrt{\frac{L_f}{C_f}} \tag{4.28}$$

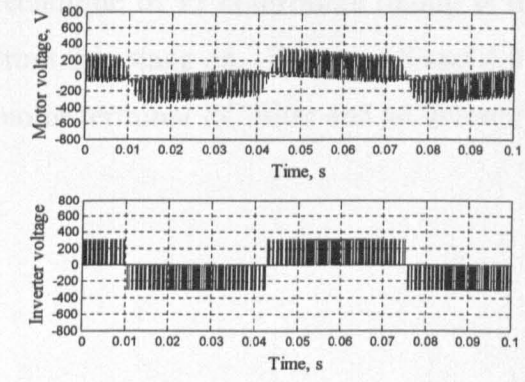
The filter resistance is selected to match the feeder surge impedance.
The critical rise time is a function of the feeder parameters and length [4.24], [4.29].

$$t_{critical} = 1.5\, l_c \Gamma_L \sqrt{L_c C_c} \tag{4.29}$$

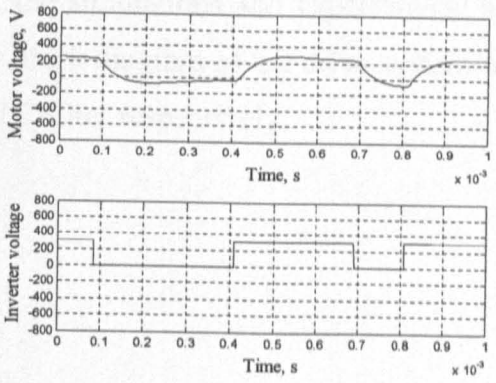
where Γ_L is the reflection coefficient at the load end.
The filter time constant is designed to be greater than or equal to the critical rise time of the inverter output voltage.

$$\sqrt{L_f C_f} \geq t_{critical} \tag{4.30}$$

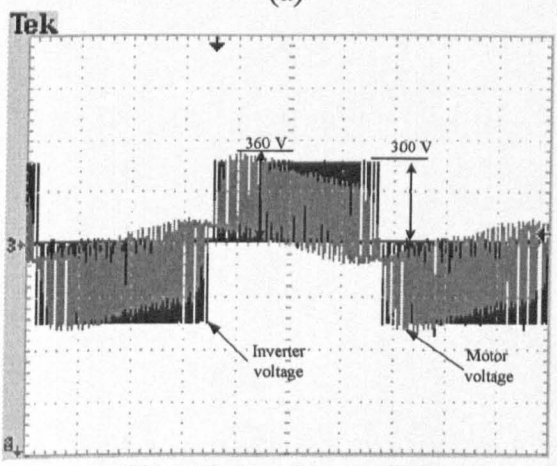
By solving (4.28) to (4.30), all the filter parameters can be evaluated. The performance of the inverter output *RLC* filter network on the motor voltage is studied by examining the drive system under the same conditions used in section 4.2. Simulation and experimental results are shown in figure 4.7. The inverter output voltage and motor terminal voltage in the case of a 1 km feeder and a motor terminal *RLC* filter is shown in figure 4.7(a) for 2 cycles of simulation. The simulation result is zoomed in figure 4.7(b). Experimental results corresponding to the simulated results are shown in figure 4.7 parts (c) and (d).



(a)

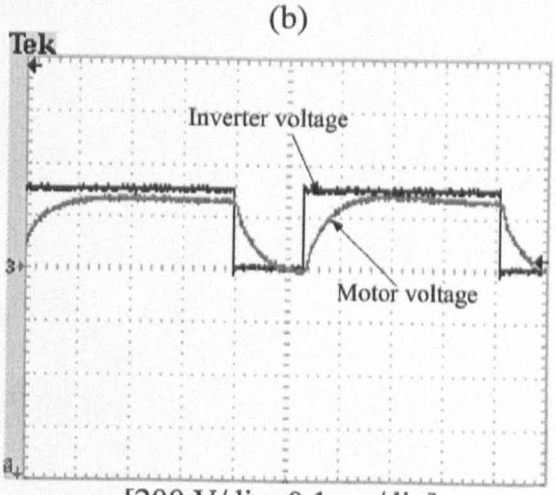


(b)



[200 V/div, 10 ms/div]

(c)



[200 V/div, 0.1 ms/div]

(d)

Figure 4.7: Simulation and experimental results of motor and inverter voltages with a one kilometre feeder using inverter output *RLC* filter
[(a)-(b) Simulation results (c)-(d) Experimental results]
(a) motor/inverter voltage with long feeder and *RLC* filter, (b) zoom for case (a),
(c) motor/inverter voltage with long feeder and *RLC* filter, and (d) zoom for case (c).

The motor terminal voltage is bounded to an acceptable level due to filter action, as shown in figure 4.7 parts (a) and (c). The motor terminal voltage is characterised by slew (rising and falling) rates due to the over-damped feature of the filter (low *dv/dt*), as shown in figure 4.7 parts (b) and (d).

4.5 Drive Performance Evaluation

The performance analysis for a vector controlled PWM VSI induction motor drive with a long motor feeder and two filter networks is investigated. Eight points are studied, [motor terminal voltage, *d*-axis motor current, *q*-axis motor current, motor line current, speed-step response, sudden load torque response, DC-link current, and common mode voltage]. For practical implementation, all PI controllers are tuned using Ziegler-Nichols Method. This

technique of PI controllers tuning is used in all the simulations and experimental setups from this stage on. Figures 4.8 and 4.9 show the block diagram of the drive system with a motor terminal *RC* filter and an inverter output *RLC* filter respectively.

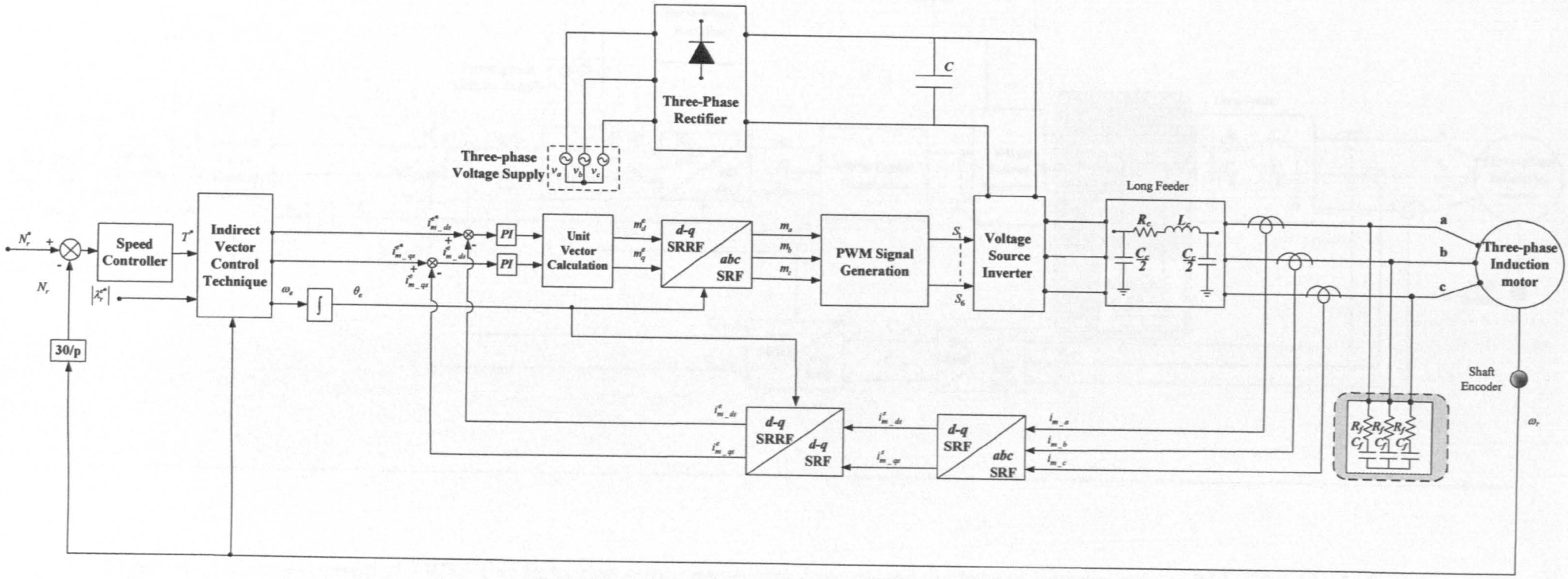


Figure 4.8: Vector controlled PWM VSI induction motor drive with long motor feeder and motor terminal *RC* filter block diagram.

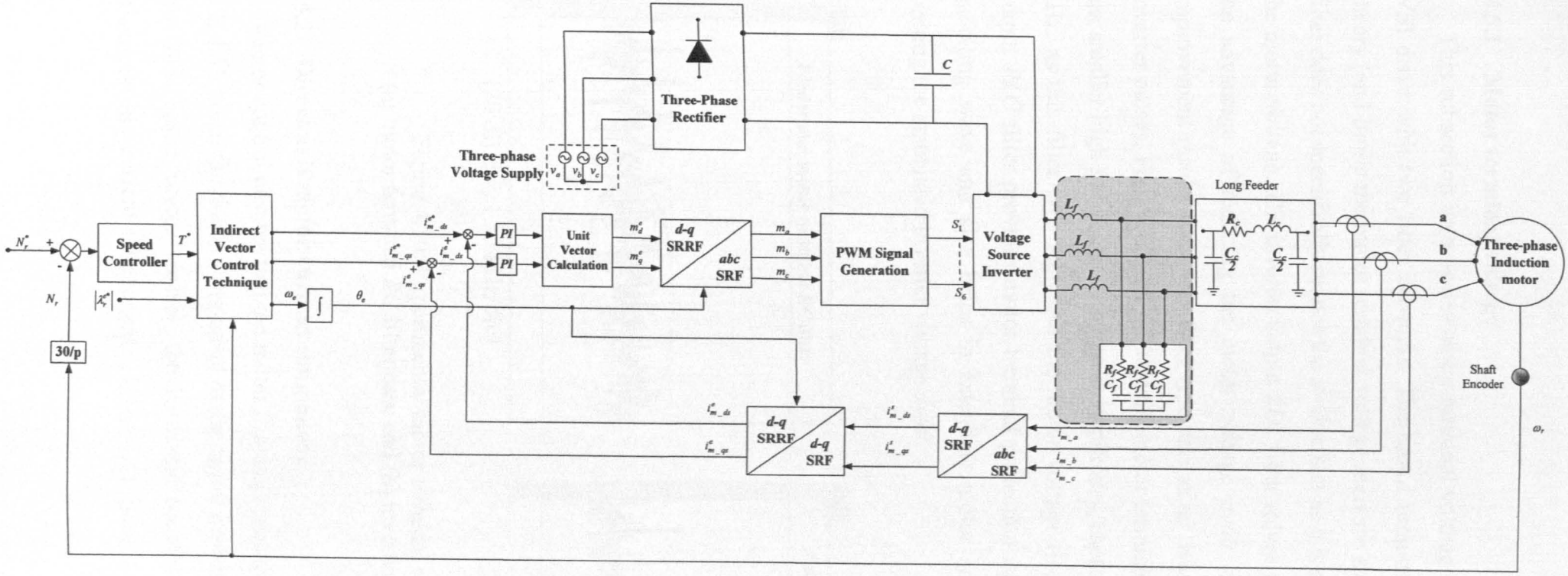
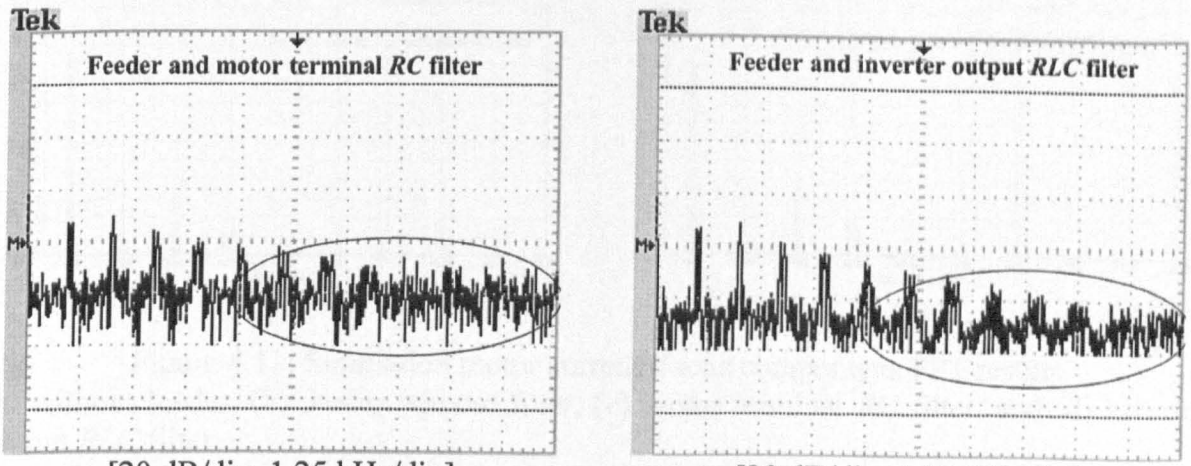


Figure 4.9: Vector controlled PWM VSI induction motor drive with long motor feeder and inverter output *RLC* filter block diagram.

4.5.1 Motor terminal voltage

This subsection investigates motor terminal voltage harmonics for a long motor feeder VSI drive with two filter networks. The motor terminal *RC* filter depends on matching theory, and limits the motor terminal voltage increase as shown in figure 4.5. This type of filter does not specifically reduce the *dv/dt* effect as it is not concerned with the rise time of the motor voltage. The inverter output *RLC* filter solves the voltage doubling problem with the advantage of reducing the motor voltage *dv/dt*, as illustrated in figure 4.7. This improvement results since this filter type acts as an over-damped circuit to the high *dv/dt* inverter pulses. Figure 4.10 shows that the motor terminal voltage FFT with the *RLC* filter, has smaller high frequency component amplitudes, especially for components exceeding 5 kHz, as this filter type increases the motor voltage rise time. Consequently, an inverter output *RLC* filter provides motor terminal protection against voltage increase due to the travelling wave and also helps in extending motor and feeder insulation life-time by limiting the associated inverter voltage *dv/dt*.



[20 dB/div, 1.25 kHz/div] (a)

[20 dB/div, 1.25 kHz/div] (b)

Figure 4.10: Experimental motor terminal voltage FFT results
(a) motor terminal *RC* filter case and (b) inverter output *RLC* filter case.

4.5.2 Direct axis motor current component

Vector control ensures that the motor flux is proportional to the motor terminal voltage [4.2, 4.3]. Since the *d*-axis component of the motor current represents the motor flux under rotor flux based vector control, the harmonic content of the motor terminal voltage influences this current component. Figure 4.11 parts (a) and (b) show that the feeder

increases the harmonic contents of the *d*-axis motor current component, which linearly affects the motor flux. Also, from figure 4.11 parts (c) and (d); the *RC* motor terminal voltage does not significantly reduce the harmonics generated by the feeder. On the other hand, figure 4.11(d) shows that the *d*-axis current component, in the case of an inverter output *RLC* filter, has the minimum amplitude of higher order harmonic contents, as the motor terminal in this case is less immune to high frequency components, as previously shown in figure 4.10. The no-feeder case represents a short feeder (i.e. lower than 10 m).

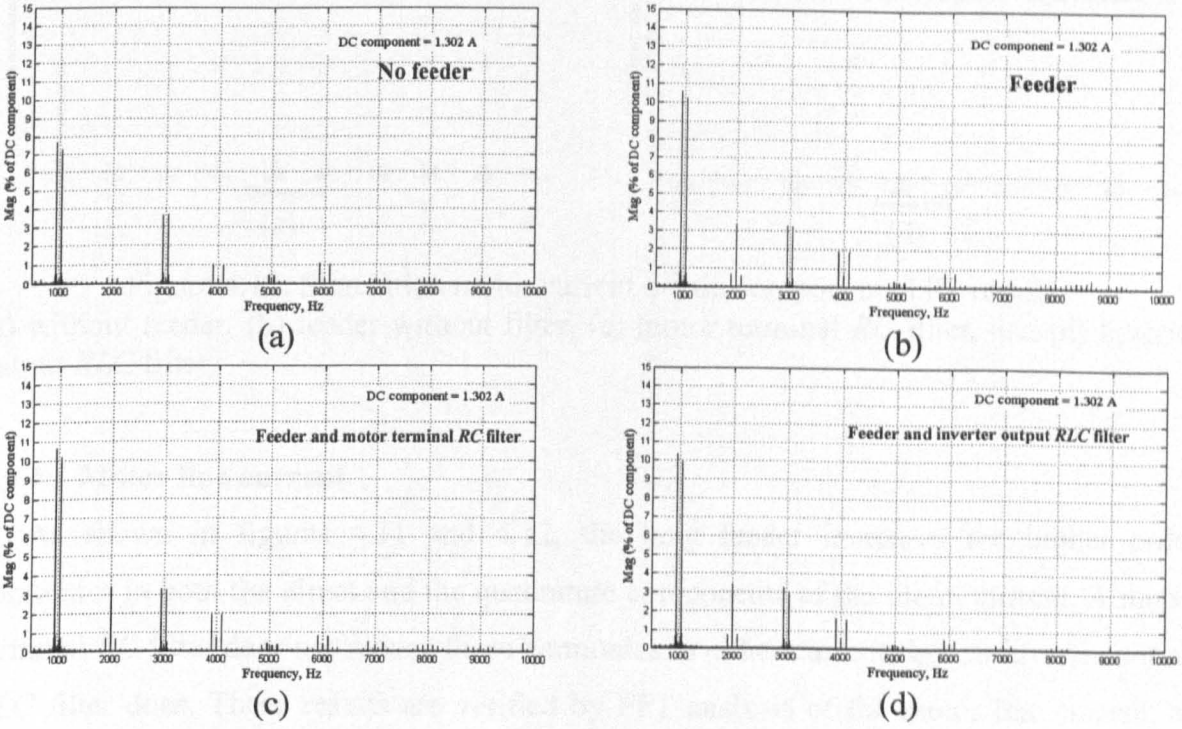


Figure 4.11: Simulation motor current *d*-axis components FFT results
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, and (d) inverter output *RLC* filter.

4.5.3 Quadrature axis motor current component

As with the *d*-axis motor current component, the feeder introduces additional harmonics into the *q*-axis motor current component which are not reduced by the motor terminal *RC* filter, as shown in figure 4.12 parts (a), (b) and (c). In figure 4.12(d) the amplitude of the higher order harmonics resulting from the inverter output *RLC* filter are less than those for the motor terminal *RC* filter case. The higher order harmonics in the *q*-axis motor current are reflected into the electromagnetic torque.

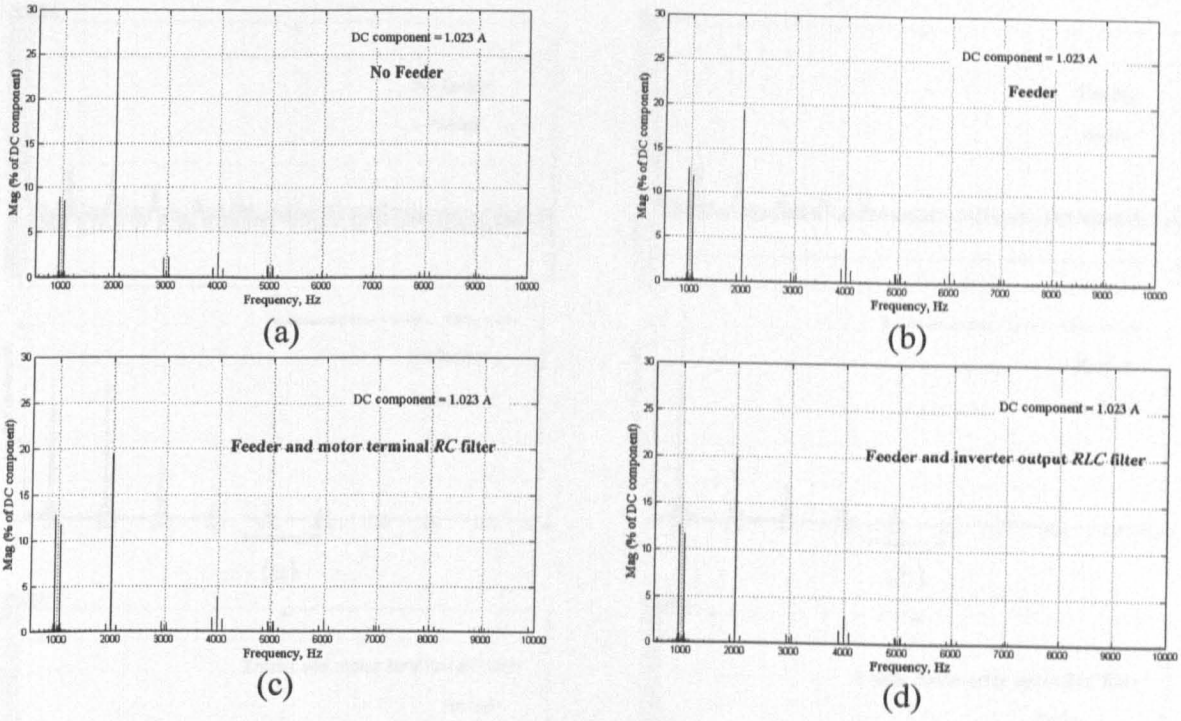


Figure 4.12: Simulation motor current q-axis components FFT results
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, and (d) inverter output *RLC* filter.

4.5.4 Motor line current

As shown in figures 4.11 and 4.12, the long feeder increases the higher order harmonics in both the direct and the quadrature components of the motor current. A motor terminal *RC* filter does not reduce these harmonics in either currents but an inverter output *RLC* filter does. These results are verified by FFT analysis of the motor line current, as shown in figure 4.13 parts (a) to (d) for the four cases under study, where the line current total harmonic distortion, (THD), has been increased in the feeder case and is similar to the motor terminal *RC* filter case. The motor line current THD is 0.26 % less in the inverter output *RLC* filter case.

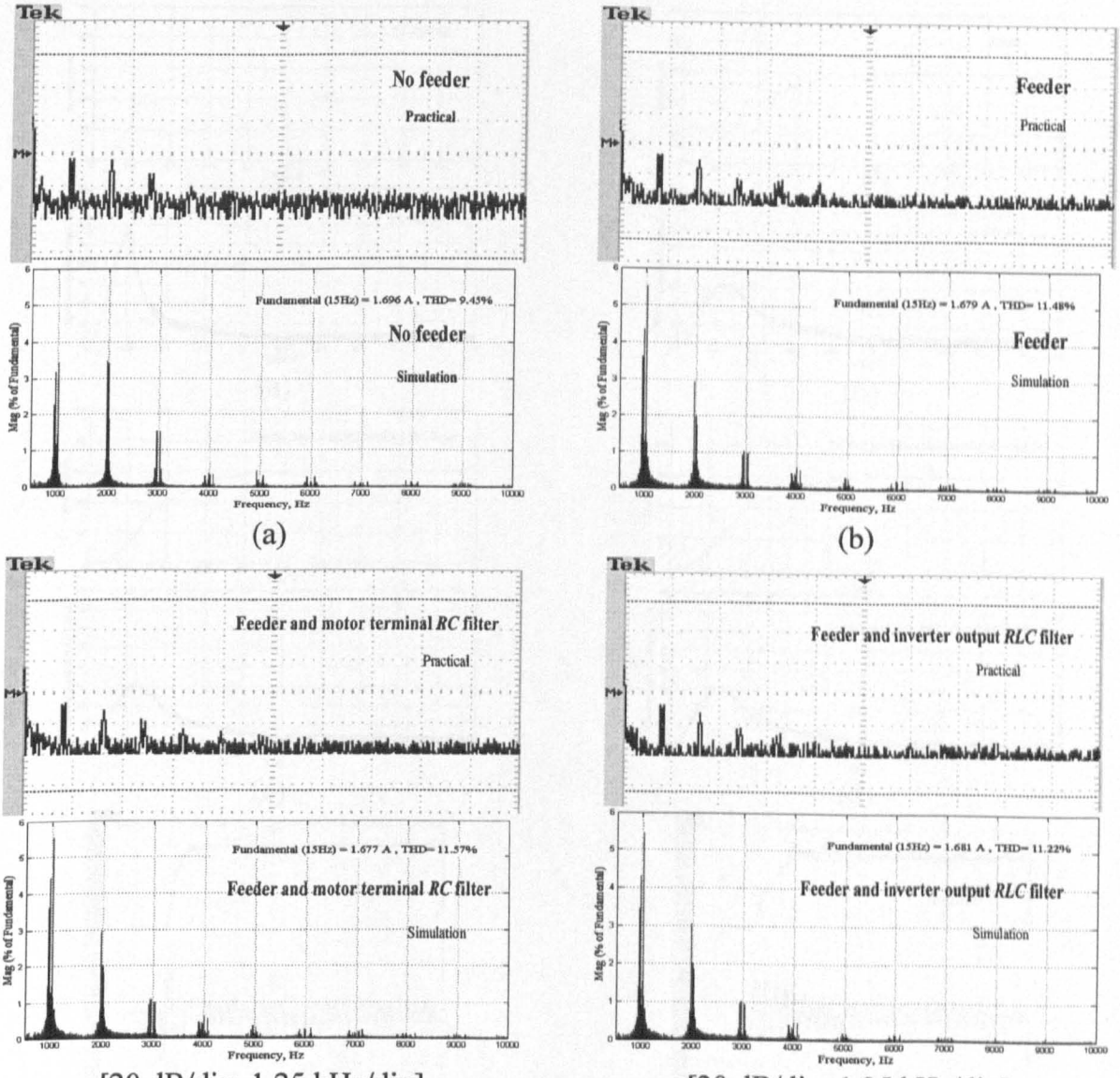
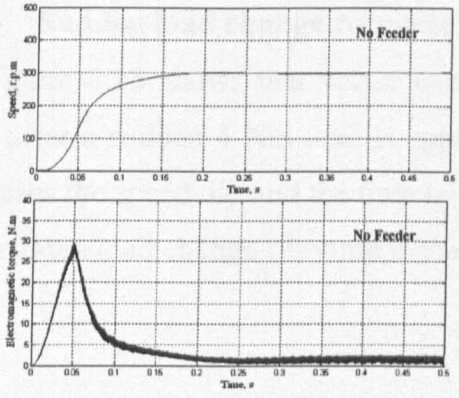


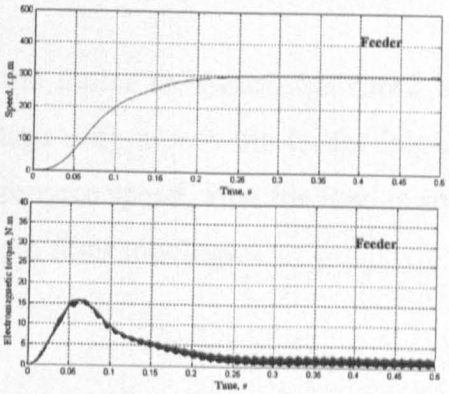
Figure 4.13: Simulation and experimental motor current FFT results
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, and (d) inverter output *RLC* filter.

4.5.5 Speed step response

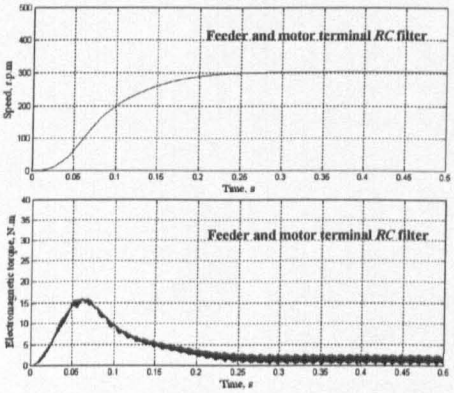
Vector control enables the motor to reach the desired speed with zero steady-state error in less than 170 ms for a speed step command, without a feeder, as shown in figure 4.14(a). The feeder introduces an extra 180 ms response delay due to the feeder impedance voltage drop which decreases the starting electromagnetic torque, and increases the rise time. This delay can not be compensated by either filter type. The simulation results in figure 4.14 show that the rise time increases due to the starting electromagnetic torque decrease with long feeders, independent of the presence of any filter.



(a)



(b)



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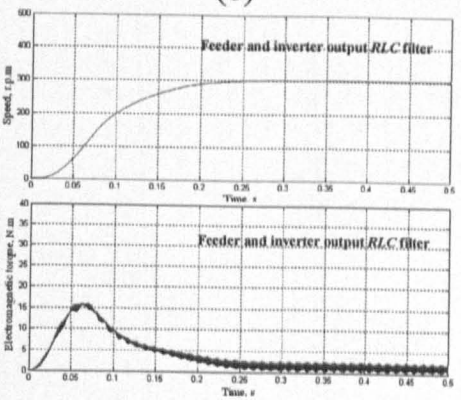

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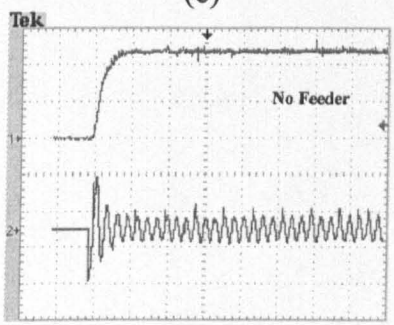
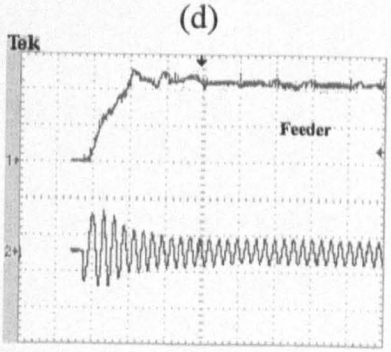


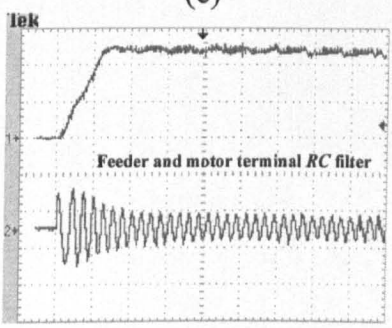
[120 rpm/div, 5 A/div, 250 ms/div]

(e)



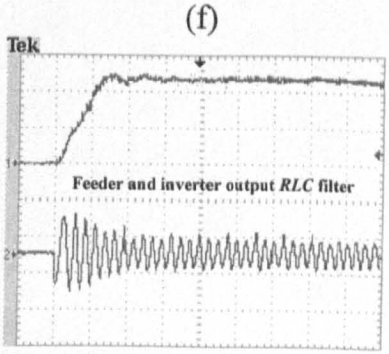
[120 rpm/div, 5 A/div, 250 ms/div]

(f)



[120 rpm/div, 5 A/div, 250 ms/div]

(g)



[120 rpm/div, 5 A/div, 250 ms/div]

(h)

Figure 4.14: Simulation and experimental no load step response results (speed step command)

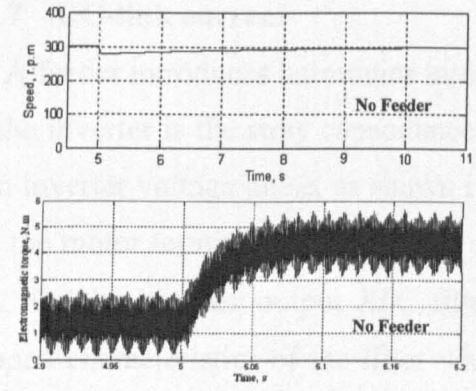
[Simulation results (a-d) for motor speed and electromagnetic torque]

[Experimental results (e-h) for motor speed and motor current]

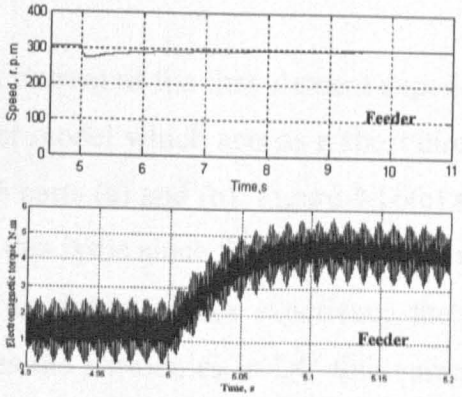
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, (d) inverter output *RLC* filter, (e) without feeder, (f) feeder without filter, (g) motor terminal *RC* filter, and (h) inverter output *RLC* filter.

4.5.6 Sudden load change response

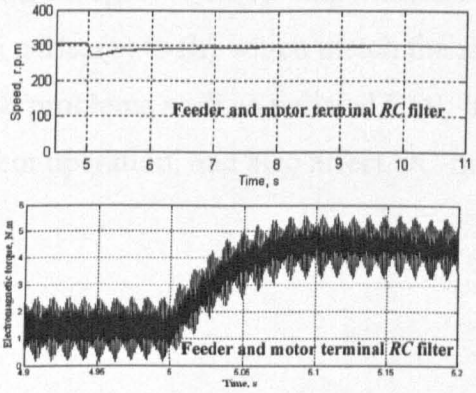
Figure 4.15 shows that vector control enables the motor to restore the speed to 300 rpm, after a sudden 4 Nm load is applied. The voltage drop across the feeder impedance increases the speed dip and the time to restore the reference speed, after the load is applied. The sudden load change response is the same with both filter topologies.



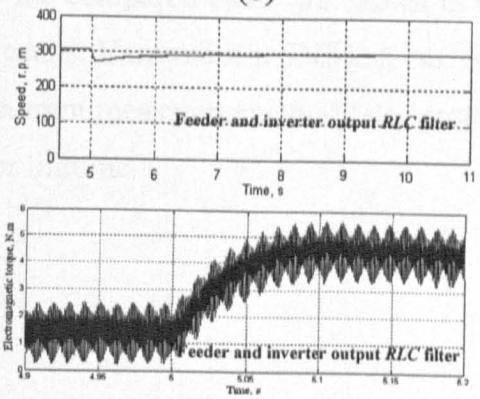
(a)



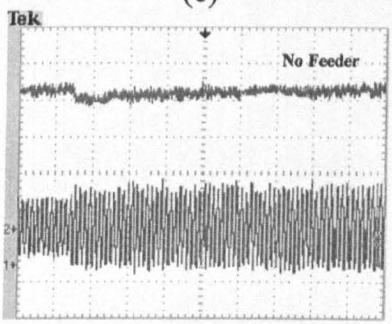
(b)



(c)

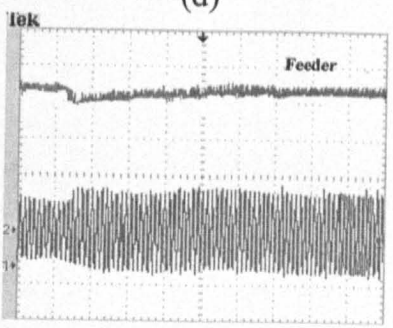


(d)



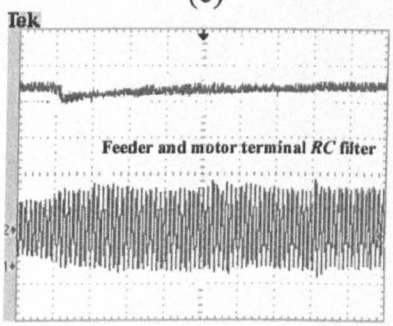
[60 rpm/div, 2 A/div, 500 ms/div]

(e)



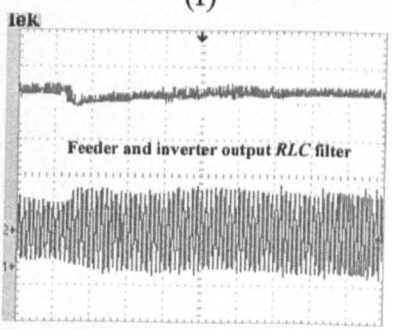
[60 rpm/div, 2 A/div, 500 ms/div]

(f)



[60 rpm/div, 2 A/div, 500 ms/div]

(g)



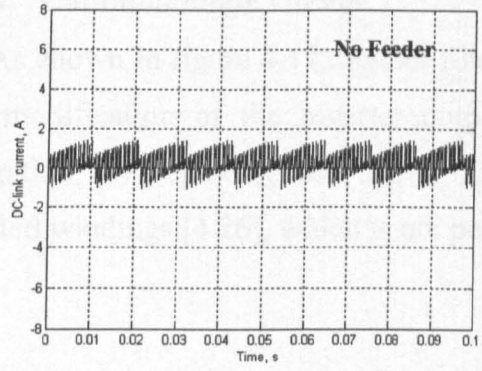
[60 rpm/div, 2 A/div, 500 ms/div]

(h)

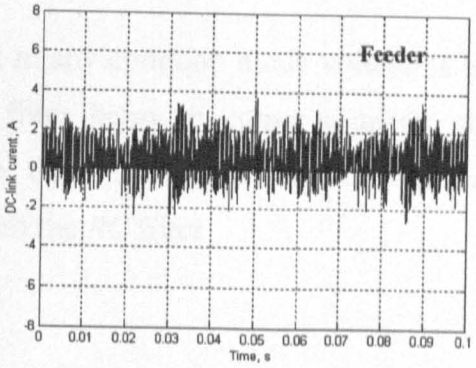
Figure 4.15: Simulation and experimental sudden load response results
[Simulation results (a-d) for motor speed and electromagnetic torque]
[Experimental results (e-h) for motor speed and motor current]
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, (d) inverter output *RLC* filter, (e) without feeder, (f) feeder without filter, (g) motor terminal *RC* filter, and (h) inverter output *RLC* filter.

4.5.7 DC-link current

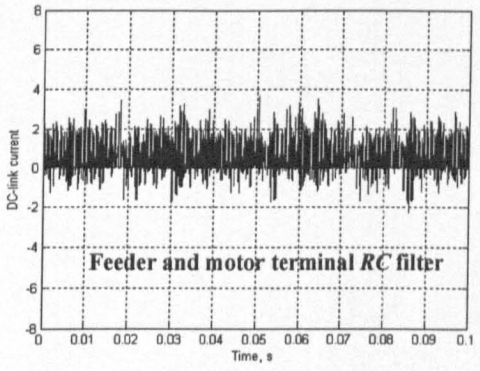
A feeder introduces harmonics into the DC-link current as the first element experienced by the inverter is the stray capacitance of the feeder model which acts as a short circuit to each inverter voltage pulse, as shown in figure 4.16 parts (a) and (b). Figure 4.16(c) shows that the motor terminal *RC* filter does not improve this issue since the filter is at the motor end. For the inverter output *RLC* filter, the inverter output pulses experience the over-damped characteristics of the filter which decreases the harmonics in DC-link current, as shown in figure 4.16(d). Experimental results for the compared cases are shown in figure 4.16 parts, (e) to (h) which match the simulation results. Harmonics in DC-link current can cause problems such as radiated EMI, inaccurate current measurement, and false protection system operation, and also affect DC-link capacitor lifetime.



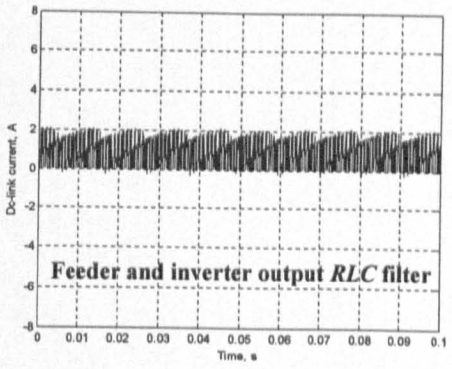
(a)



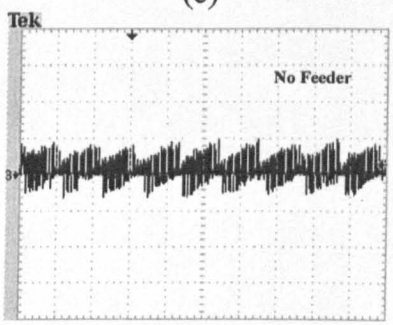
(b)



(c)

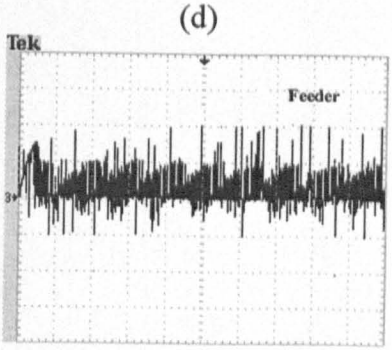


(d)



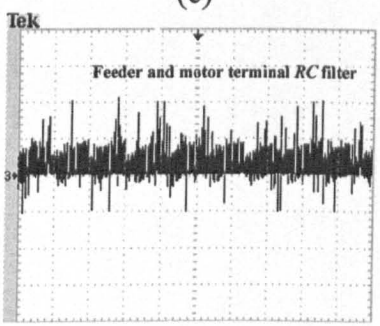
[2 A/div, 10 ms/div]

(e)



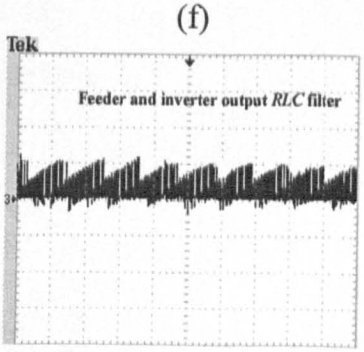
[2 A/div, 10 ms/div]

(f)



[2 A/div, 10 ms/div]

(g)



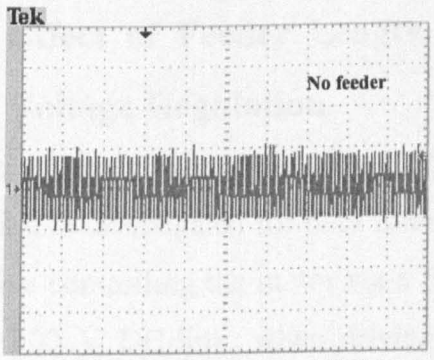
[2 A/div, 10 ms/div]

(h)

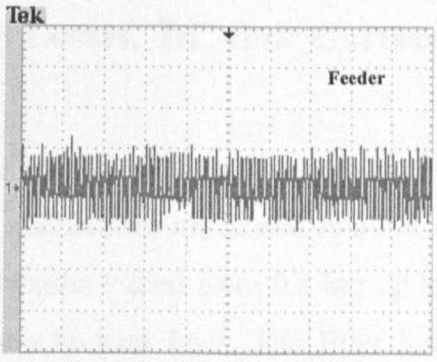
Figure 4.16: Simulation and experimental DC-link current results
[Simulation results (a-d) Experimental results (e-h)]
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, (d) inverter output *RLC* filter, (e) without feeder, (f) feeder without filter, (g) motor terminal *RC* filter, and (h) inverter output *RLC* filter.

4.5.8 Common mode voltage

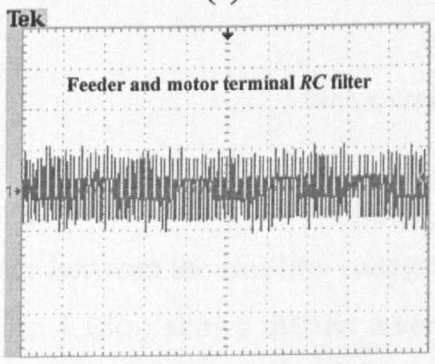
As shown in figure 4.17, neither filters result in any common mode voltage reduction. But modification of the inverter output *RLC* filter helps in common mode voltages mitigation, by replacing the series three-phase filter inductances with four mutually coupled windings [4.26], which is not possible with the *RC* filter.



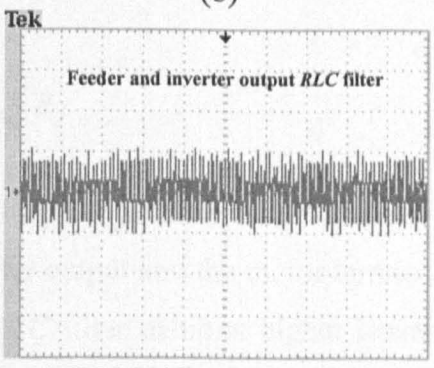
[200 V/div, 10 ms/div]
(a)



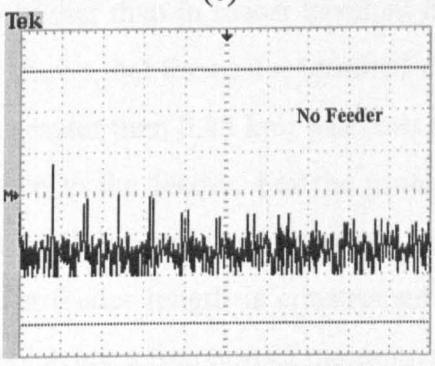
[200 V/div, 10 ms/div]
(b)



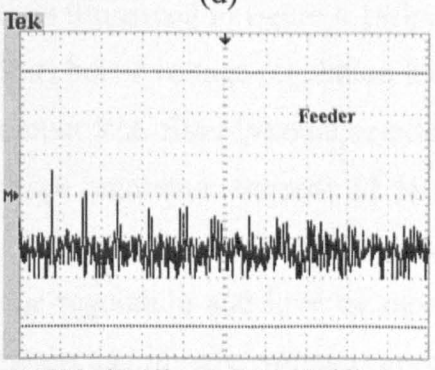
[200 V/div, 10 ms/div]
(c)



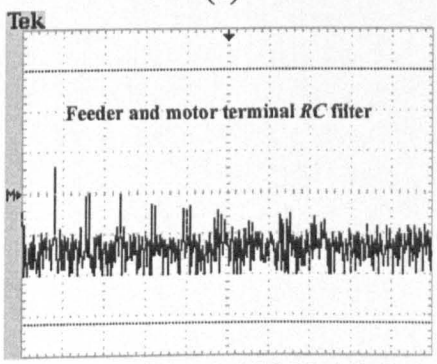
[200 V/div, 10 ms/div]
(d)



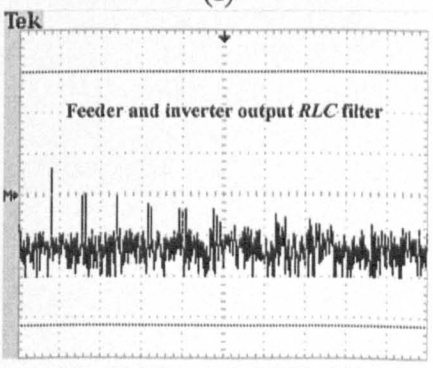
[20 dB/div, 1.25 kHz/div]
(e)



[20 dB/div, 1.25 kHz/div]
(f)



[20 dB/div, 1.25 kHz/div]
(g)



[20 dB/div, 1.25 kHz/div]
(h)

Figure 4.17: Experimental common mode voltage and its FFT results
Common mode voltage waveforms (a-d) Common mode voltage FFT (e-h)
(a) without feeder, (b) feeder without filter, (c) motor terminal *RC* filter, (d) inverter output *RLC* filter, (e) without feeder, (f) feeder without filter, (g) motor terminal *RC* filter, and (h) inverter output *RLC* filter.

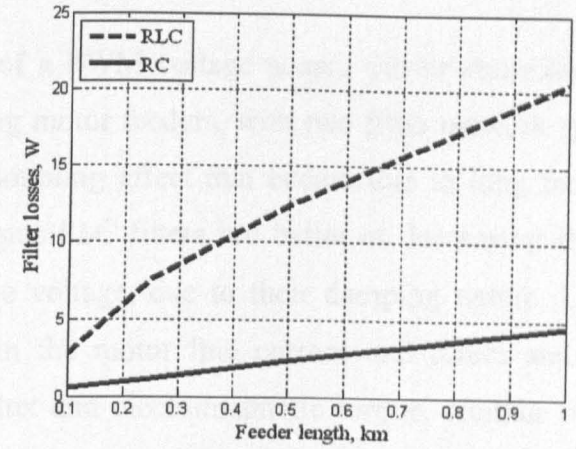
4.6 Effect of Feeder Length on Filter Losses, DC-link Current, and Voltage Regulation

The effect of feeder length on filter network losses, DC-link current, and voltage regulation is investigated for both filter types. The simulations are scaled to a low voltage VSI drive controlling the motor via a feeder with lengths varied from 0.1 km up to 1 km; with a 300 V DC-link, when driving a 4 Nm steady-state load. The filter losses are calculated using the total rms value of the filter current.

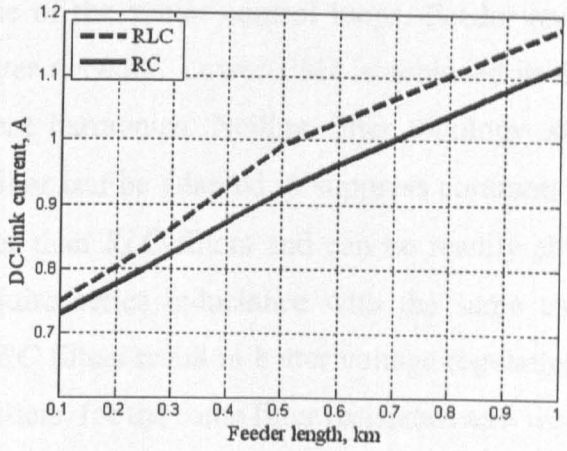
$$Filter\ losses = \left|I_{filter\_total}\right|^2 R_f \tag{4.31}$$

The DC-link current is recorded and the voltage regulation is determined by the difference between the rms line voltage of the inverter output and the motor terminal.

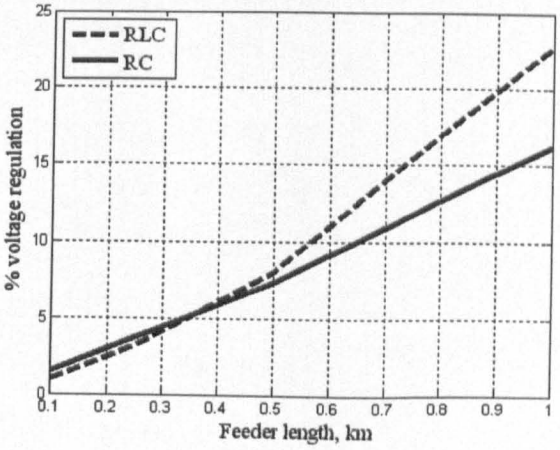
Figure 4.18(a) shows that an inverter output *RLC* filter exhibits higher losses than a motor terminal *RC* filter. The DC-link current, in the case of inverter output *RLC* filters, is slightly higher than in motor terminal *RC* filter case, as illustrated in figure 4.18(b). Figure 4.18(c) shows that the motor terminal *RC* filter exhibits better voltage regulation for feeder lengths greater than 0.45 km, where as the inverter output *RLC* filter introduces extra series impedance to the feeder. For the prototype, the voltage regulation exceeds 22 % and the inverter modulation index saturates for feeder lengths greater than 1 km. Generally, the maximum feeder length is constrained by the voltage regulation and inverter modulation index which are a function of motor and cable parameters and inverter voltage capability.



(a)



(b)



(c)

Figure 4.18: Variation of filter losses, DC-link current and voltage regulation versus varying feeder length
(a) filter losses, (b) DC-link current, and (c) voltage regulation.

Summary

The performance of a PWM voltage source vector controlled drive has been studied when utilized with long motor feeders, with two filter network types. Both filter networks mitigate the voltage doubling effect that occurs due to long feeders with voltage source inverters. Inverter output *RLC* filters are better at decreasing the higher order harmonic components in the line voltage, due to their damping nature. Consequently, *RLC* filters minimize harmonics in the motor line current and direct and quadrature components, leading to smoother flux and electromagnetic torque. Neither filter networks affects the vector control loops as they are not switching frequency filters and their time constants are long compared to those of the vector control loops. Feeder resistance decreases starting torque, independent filter network. Lower EMI is achieved in the *RLC* filter case due to reduced DC-link current harmonics. Neither filter topology affects the common mode voltage, but the *RLC* filter can be adapted to suppress common mode currents. *RC* filters are simpler and cheaper than *RLC* filters and can be readily shunt connected to existing drives. *RLC* filters require series inductance with the same current rating as the drive system output current. *RC* filters result in better voltage regulation. *RLC* filters suffer from higher losses than *RC* filters, for the same filter resistance and variable feeder length.

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CHAPTER FIVE:

Vector Controlled PWM CSI Induction Motor Drive with a Long Motor Feeder

Power inverters used in MV drives can be generally classified into voltage source inverters (VSI) and current source inverters (CSI). The voltage source inverter produces a defined three-phase PWM voltage waveform for the load while the current source inverter outputs a defined PWM current waveform. The PWM current source inverter features a simple converter topology, motor-friendly waveforms, and reliable short-circuit protection, and therefore is a widely used converter topology for MV drives [5.1] - [5.4]. This chapter addresses the vector controlled PWM CSI drive as an alternative for PWM VSI MV drives. The basic principles of the vector controlled PWM CSI drive are presented then direct vector control is discussed as it is the most common control method for these drives. Then the basics of the indirect vector controlled PWM CSI drive are given. The main drawbacks and limitations of this CSI drive leads to the proposed indirect vector controlled PWM CSI drive which can operate with acceptable performance and a simpler control algorithm than with the direct vector control method. The proposed indirect vector controlled PWM CSI drive is examined with a 1 km motor feeder. Experimental results support the simulation results.

5.1 Vector Controlled PWM CSI Drive

The general block diagram of a vector controlled PWM CSI drive, in figure 5.1, can be considered as a dual to the PWM VSI, with modifications to the control algorithm. The block diagram consists of six main parts:

- Current source inverter
- Inverter output capacitor bank
- PWM generation and mapping circuit
- Current source rectifier
- DC-link inductor
- Vector control technique

Detailed explanation of these parts is given in the following subsections.

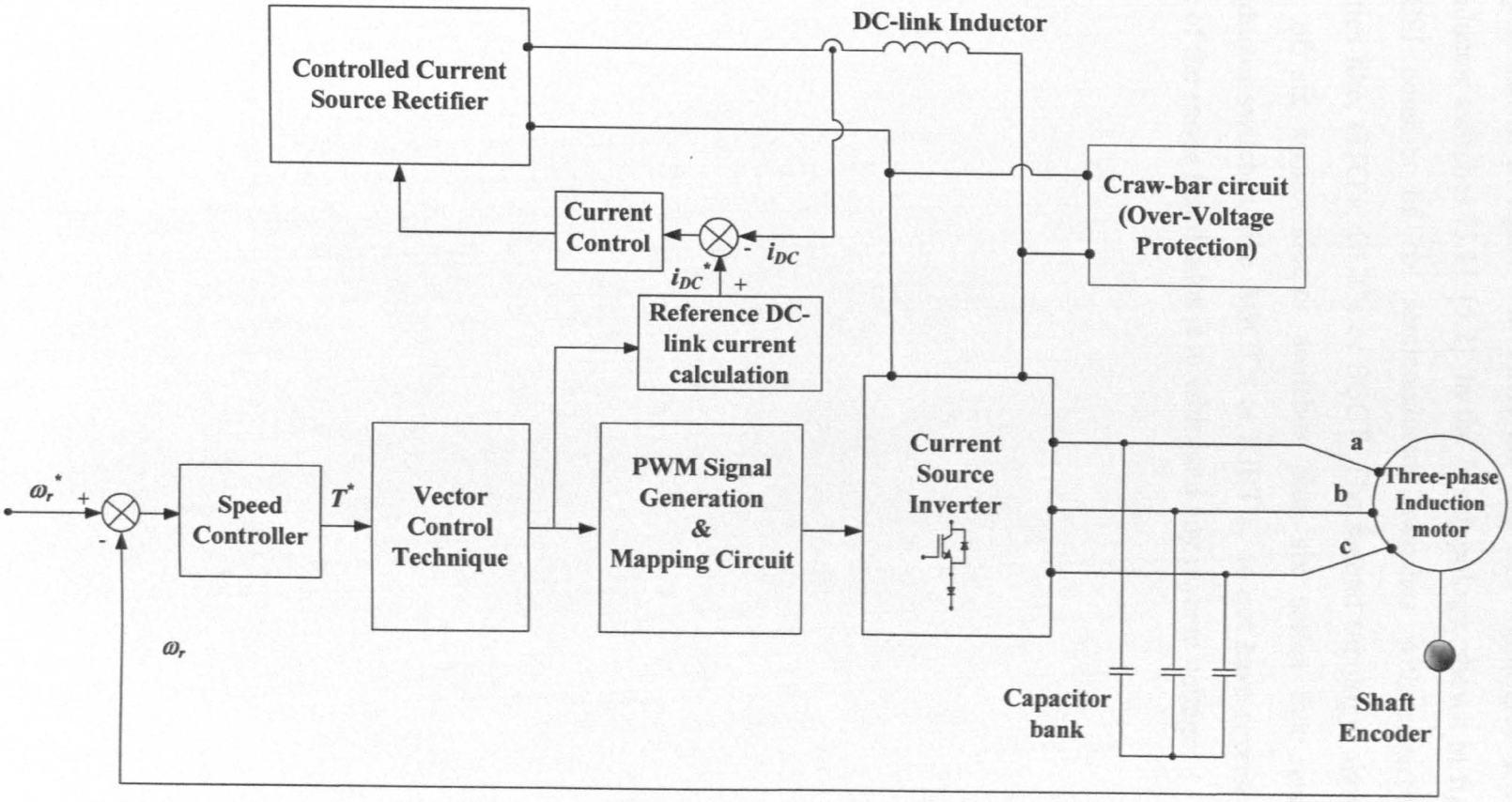


Figure 5.1: Basic vector controlled PWM CSI drive block diagram.

5.1.1 Current source inverter (CSI)

The CSI converts a DC current input into three-phase chopped AC current. The CSI topology is shown in figure 5.2. There are two CSI topologies depending on the used semiconductor switches [5.1], [5.2]. In the first topology, shown in figure 5.2(b), a three-phase CSI consists of six semiconductor switches with reverse voltage blocking capabilities like, GTO's, GCT's or SGCT. The second topology, shown in figure 5.2(c), consists of six semiconductor switches plus six series fast recovery diodes. The semiconductor switches, like AGCT's or IGBT's, do not have reverse voltage properties. The role of the series fast diodes is to withstand any reverse voltage.

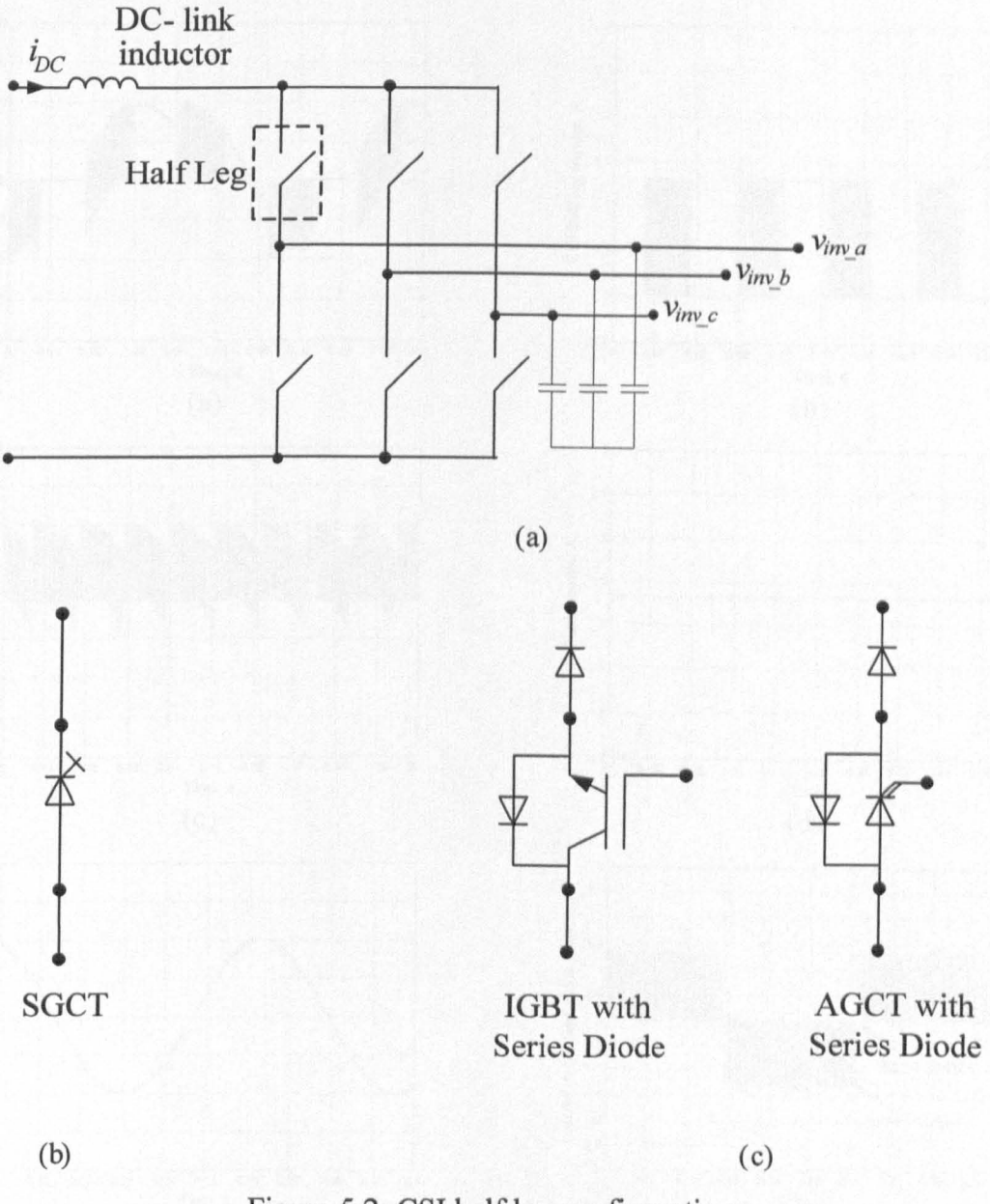


Figure 5.2: CSI half leg configurations
(a) CSI topology, (b) half leg configuration with one switch having reverse voltage capabilities, and (c) half leg configuration with one switch can not withstand reverse voltage and accompanied by series fast recovery diodes.

The output current phase and frequency are varied by the CSI. The amplitude of the output chopped AC current wave-forms is controlled from the current source rectifier side. Figure 5.3 shows typical results for the CSI input and output voltage/current waveforms and the voltage/current per half leg at a 1 kHz switching frequency and a 15 Hz fundamental output.

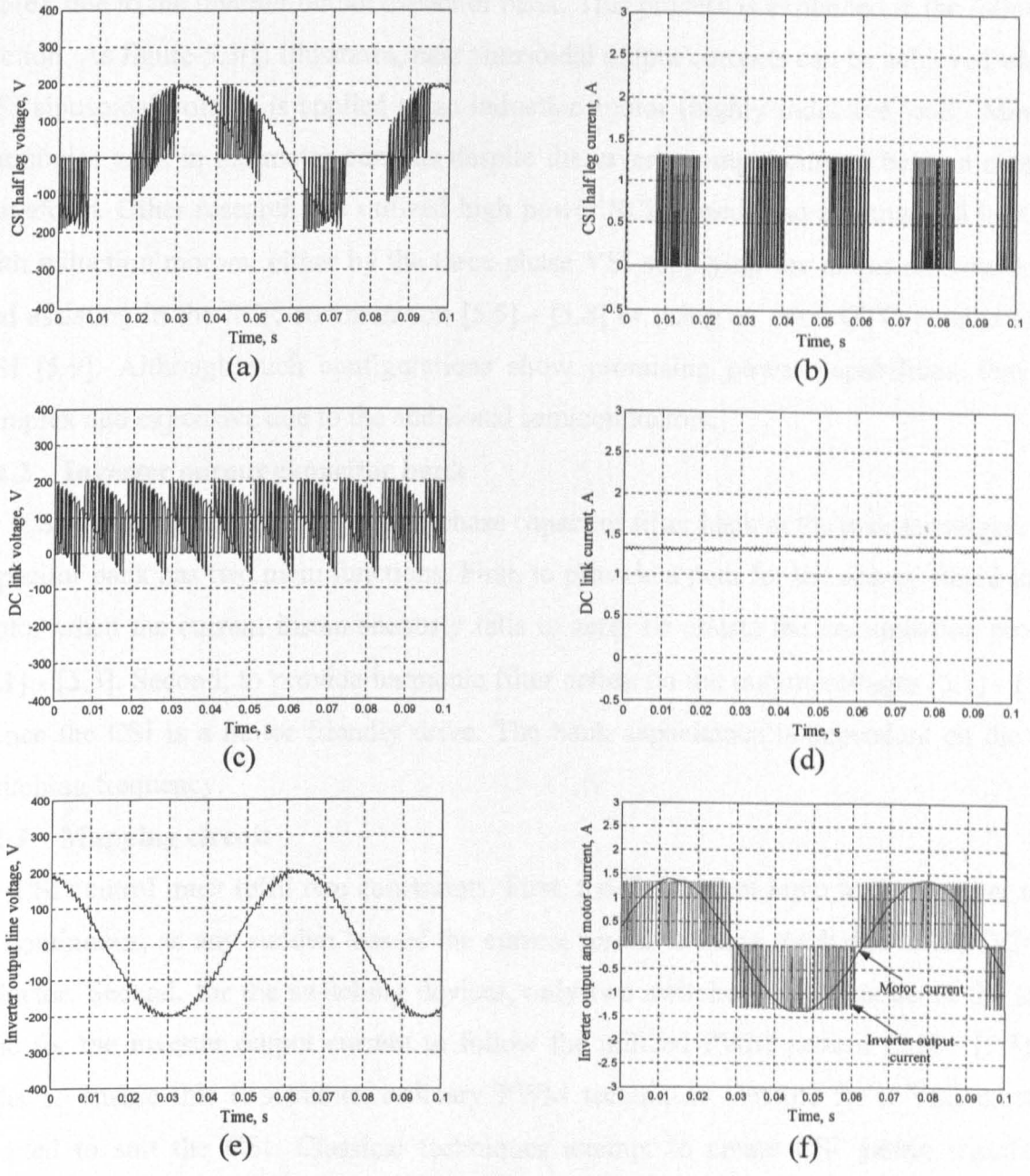


Figure 5.3: CSI voltage/current waveforms
(a) half leg voltage, (b) half leg current, (c) input DC-link voltage, (d) input DC-link current, (e) output voltage, and (f) inverter/motor current.

It can be shown from figure 5.3 parts (a) and (b) that semiconductors used in the CSI half leg must have reverse voltage blocking capabilities as the inverter half leg voltage is bidirectional while the current is unidirectional. Figure 5.3 parts (c) and (d) reflect the duality between the VSI and the CSI as the DC-link voltage in CSI case has the same pattern of the DC-link current as in the VSI, as illustrated in chapter four. Also, one of the most important merits of the CSI is the near sinusoidal output voltage, as shown in figure

5.3(e), due to the inverter output capacitor bank. This process is explained in the following section. As figure 5.3(f) illustrates, near sinusoidal output currents can be achieved when a CSI sinusoidal voltage is applied to an induction motor (highly inductive load). Minimal harmonics exist in the motor currents despite the inverter output current being a chopped waveform. Other research has utilized high power SCR based load commutated inverters with induction motors either by the three-phase VSI supplying the motor reactive power and assisting in the SCR commutation [5.5] - [5.8] or using an extra GTO parallel to the CSI [5.9]. Although such configurations show promising power capabilities, they are complex and expensive due to the additional semiconductors.

5.1.2 Inverter output capacitor bank

CSI's are characterized by a three-phase capacitor filter bank at the inverter output. The capacitor bank has two main functions. First, to provide a path for the energy stored in the motor when the current instantaneously falls to zero, i.e assists the commutation process [5.1] - [5.3]. Second, to provide harmonic filter action on the output voltages [5.1] - [5.3]. Hence the CSI is a motor friendly drive. The bank capacitance is dependant on the CSI switching frequency.

5.1.3 Mapping circuit

CSI control must fulfil two constraints. First, the DC current input to the inverter must be continuous, as any sudden loss of the current results in large *dv/dt* due to the DC-link inductor. Second, for the switching devices, only two switches must conduct at the same time for the inverter output current to follow the utilized PWM pattern [5.1] - [5.3]. In order to ensure this constraints, ordinary PWM techniques suitable for a VSI, must be adapted to suit the CSI. Classical techniques attempt to create CSI gating signals by generating off-line patterns and store them in an EPROM. This off-line technique uses fixed modulation indices and changes once per cycle which reduces the dynamic performance of the drive [5.10]. On-line PWM generation is introduced by converting bi-logic VSI PWM signals to tri-logic CSI PWM signals, using intensive matrix calculations [5.11]. For simplicity and cost/size reduction, a digital circuit, called a mapping circuit, is used to redistribute ordinary VSI PWM signals to constrained CSI signals [5.12], [5.13]. The mapping circuit could also be DSP implemented for space and hardware reduction. The mapping circuit block diagram consists of four main parts as shown in figure 5.4.

- Switching pulse generator
- Complementary pulse generator
- Complementary pulse distributor
- Pulse combinator

The mapping circuit detailed hardware construction is shown in figure 5.5.

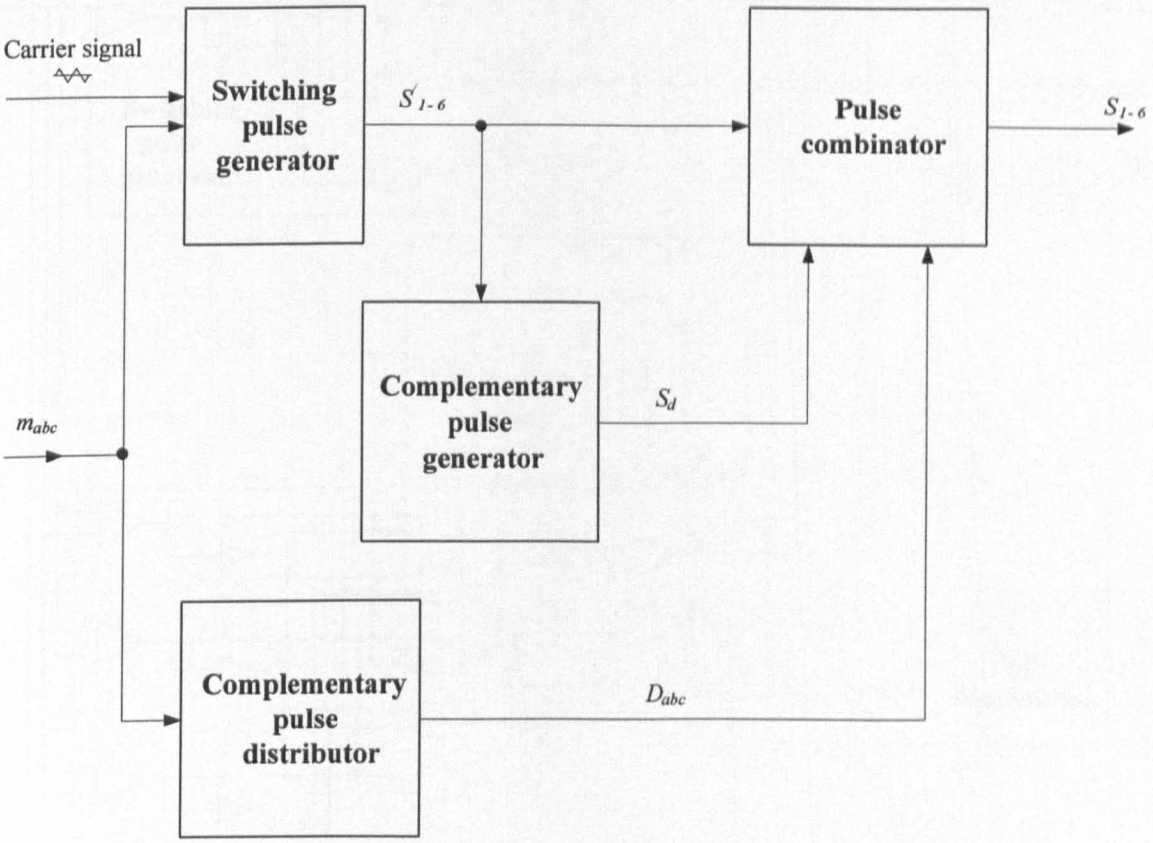


Figure 5.4: PWM generator and mapping circuit block diagram.

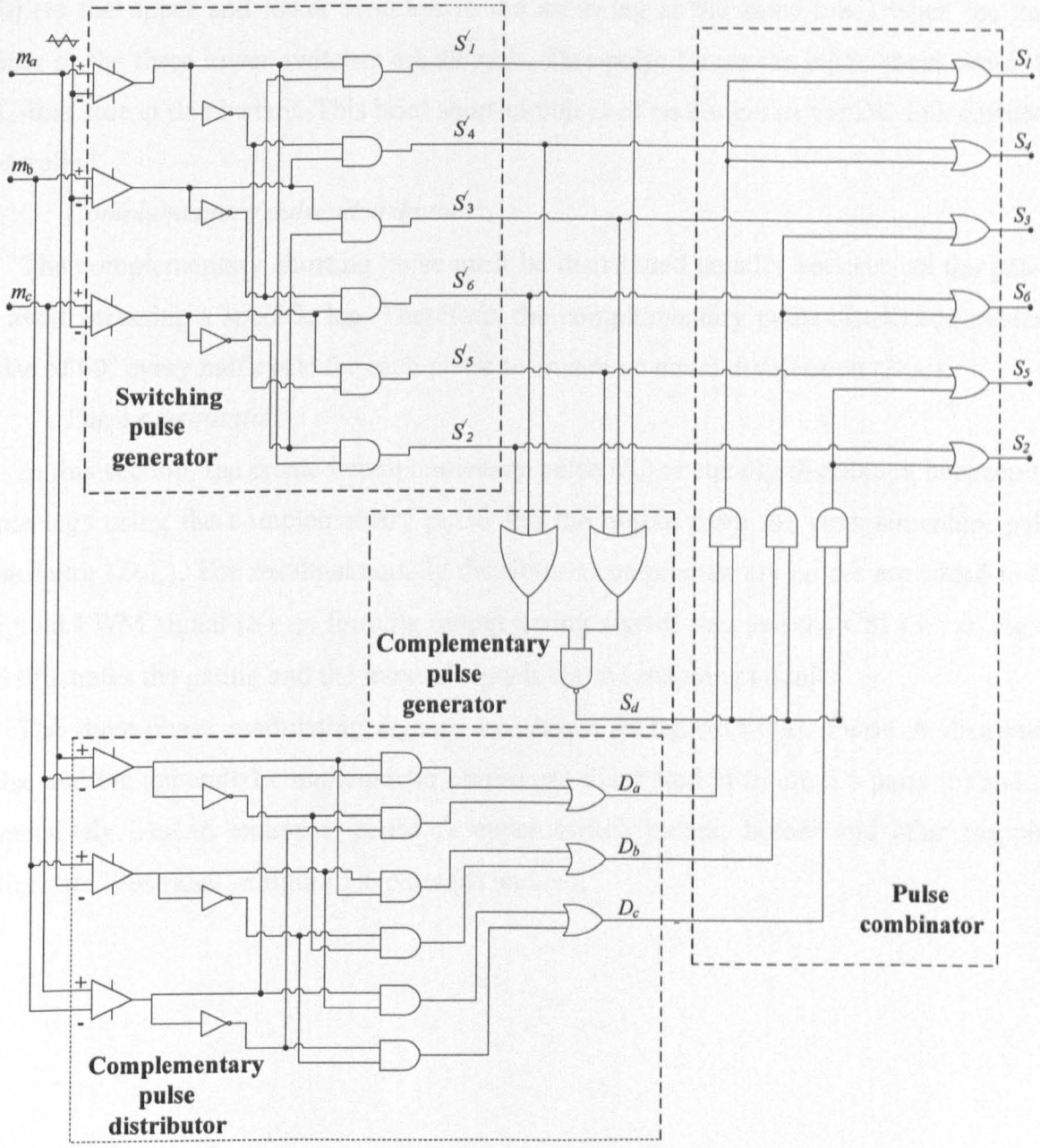


Figure 5.5: PWM generator and mapping circuit internal construction.

i. *Switching pulse generator*

Normal carrier based PWM is performed in this section. The three-phase modulating signals (m_{abc}) are compared with the carrier signal to generate pulses for the upper switches ($S'_{1,3,5}$) and their lower complements ($S'_{4,6,2}$).

ii. *Complementary pulse generator*

In order to fulfil the CSI requirement, the DC-link current should not be interrupted, so switch overlapping is added. The complementary pulse generator ensures a pulse output

(S_d) (to the upper and lower switches in the same leg at the same time) when the three upper or the three lower switches are all zero. This pulse forces the leg to short circuit the DC-link side at this instant. This brief short-circuit is of no danger as the DC-link current is controlled.

iii. Complementary pulse distributor

The complementary shorting pulse must be distributed equally between all the phases to avoid stressing a specific leg. Therefore, the complementary pulse distributor creates a pulse of 60° every half cycle for each phase to ensure an equal distribution (D_{abc}).

iv. Pulse combinator

In this section, the created complementary pulse (S_d) is equally distributed between the three legs using the complementary pulse and the output from the complementary pulse distributor (D_{abc}). The resultant equally distributed complementary pulses are added to the original PWM signal ($S'_{1..6}$) forming output gating signals that suit the CSI ($S_{1..6}$). Figure 5.6 illustrates the gating and the internal signals for the mapping circuit.

The three-phase modulating signals are shown in figure 5.6(a). Phase A distributor pulse and the generated complementary pulse are illustrated in figure 5.6 parts (b) and (c) respectively. As an example, phase A upper switch pulses, before and after mapping action, are illustrated in figure 5.6 parts (d) and (e).

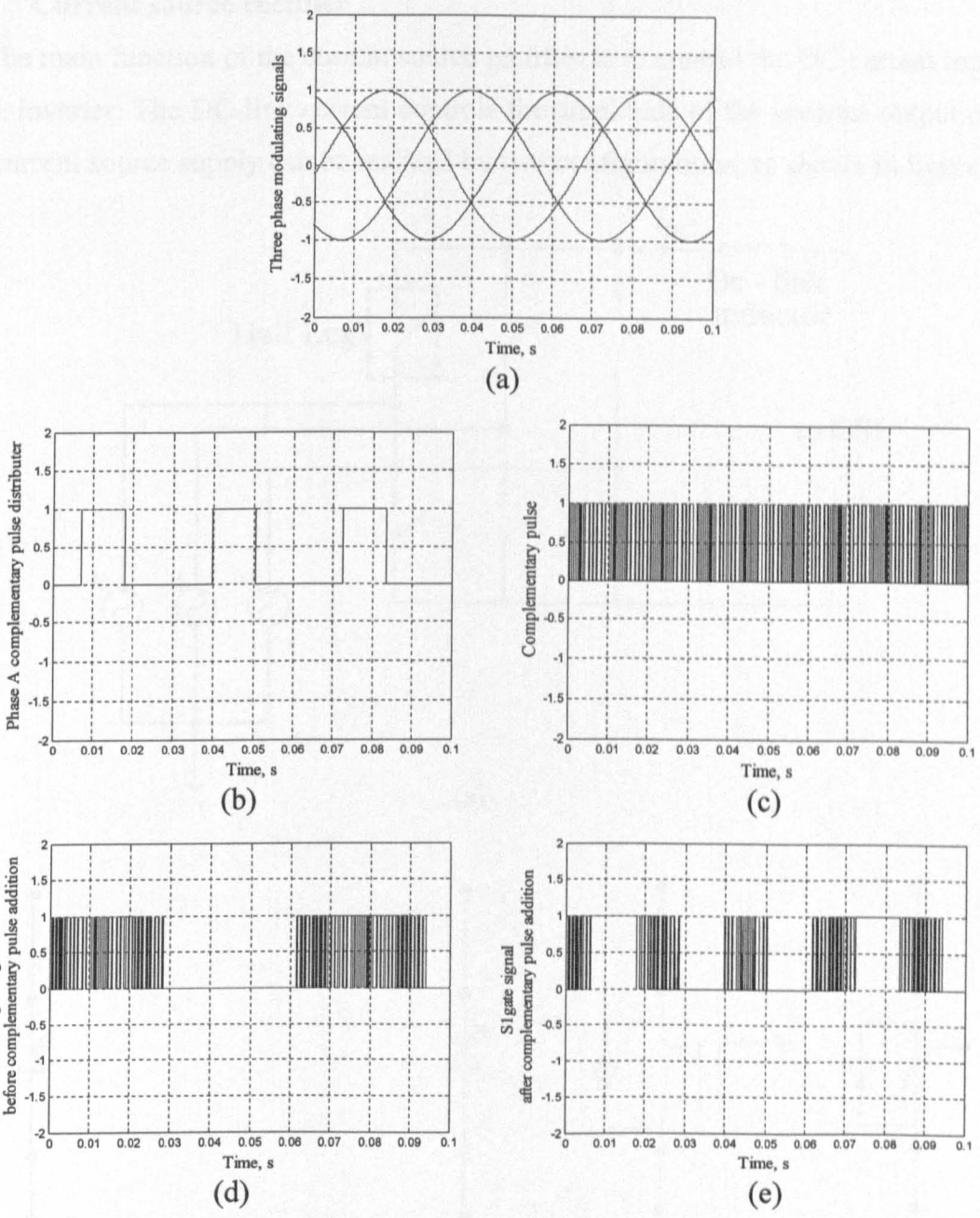


Figure 5.6: PWM generator and mapping circuit gating/control signals
(a) three phase modulating signals, (b) phase A complementary pulse distributor, (c) complementary pulse, (d) phase A upper switch original PWM signal, and (e) phase A upper switch final PWM signal.

The main advantage of mapping circuits are that they can be used with any VSI PWM technique, like SPWM or SVM, without detailed adaptation of the PWM technique [5.12], [5.13].

5.1.4 Current source rectifier

The main function of the current source rectifier is to control the DC current input level to the inverter. The DC-link current controls the amplitude of the inverter output currents. The current source supply can be realized by two configurations, as shown in figure 5.7.

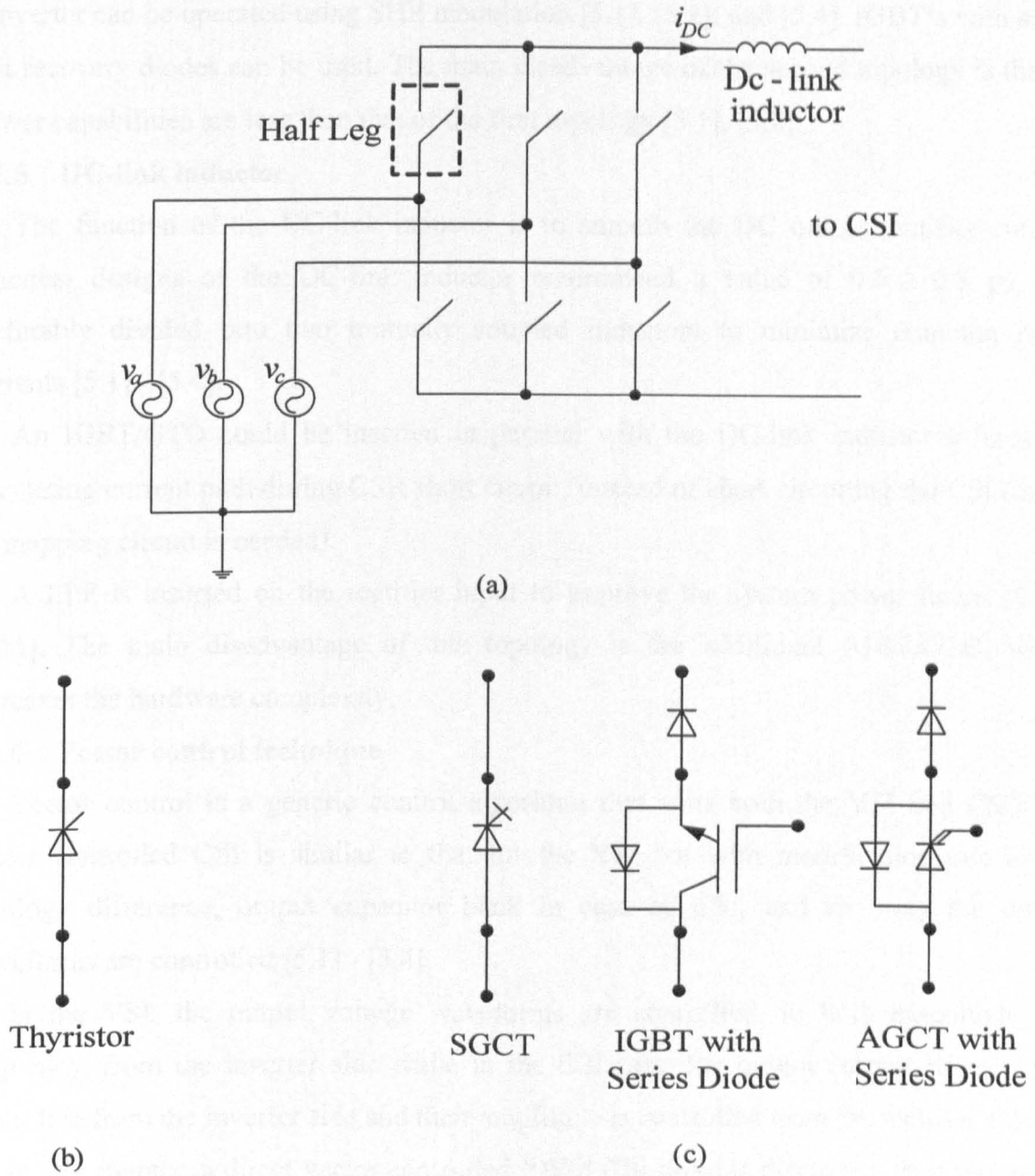


Figure 5.7: CSR semiconductors half leg configurations
(a) CSR topology, (b) half leg configuration for SCR based current controlled CSR, and (c) half leg configuration for PWM based current controlled CSR.

The first topology is a current controlled SCR converter as shown in figure 5.7(b). This topology is characterized by having simple control and high power capabilities, and is used in this chapter. The second topology is a current controlled PWM current source rectifier as shown in figure 5.7(c). It is characterized by a better input supply current THD as the converter can be operated using SHE modulation [5.1], [5.2], and [5.4]. IGBT's with series fast recovery diodes can be used. The main disadvantage of the second topology is that its power capabilities are less than that of the first topology [5.1], [5.2].

5.1.5 DC-link inductor

The function of the DC-link inductor is to smooth the DC output rectifier current. Practical designs of the DC-link inductor recommend a value of 0.5 - 0.8 pu, and preferably divided into two mutually coupled inductors to minimize common mode currents [5.1] - [5.4].

An IGBT/GTO could be inserted in parallel with the DC-link inductor to create a circulating current path during CSR short circuit, instead of short circuiting the CSI (hence no mapping circuit is needed).

A LPF is inserted on the rectifier input to improve the system power factor [5.14], [5.15]. The main disadvantage of this topology is the additional IGBT/GTO, which increases the hardware complexity.

5.1.6 Vector control technique

Vector control is a generic control algorithm that suits both the VSI and CSI. The vector controlled CSI is similar to that for the VSI but with modification due to the topology difference, output capacitor bank in case of CSI, and the way the output waveforms are controlled [5.1] - [5.4].

In the VSI, the output voltage waveforms are controlled, in both magnitude and frequency, from the inverter side while in the CSI case, the output current frequency is controlled from the inverter side and their amplitude is controlled from the rectifier side.

In this chapter, a direct vector controlled PWM CSI drive is discussed, as it represents a common method for CSI drive control. Features of this method are addressed. Then the basic indirect vector controlled PWM CSI drive is illustrated, followed by the proposed modified indirect vector controlled PWM CSI drive. The indirect vector control technique was discussed in detail in chapter 4, sections 4.1, from (4.1) to (4.21).

5.2 Direct Vector Controlled PWM CSI Drive

In this section, the principles of direct vector controlled PWM CSI drives are discussed in detail and the governing equations are presented. The drive performance is illustrated by simulation and compared with the indirect vector control technique in the following sections.

5.2.1 System description

The main objective of a direct vector controlled CSI drive is to implement decoupled control of the machine flux and torque/speed variables, using two control loops, one for the flux and the other for the speed/torque [5.16] - [5.19] as shown in figure 5.8. The motor speed is measured while the rotor flux is estimated from the stator voltage and current. The output from the speed and the flux control loops are the motor reference quadrature and direct components respectively. The capacitor *d-q* current components are calculated and added to the motor *d-q* reference currents to generate the DC-link reference current. The rectifier current controller is responsible for adjusting the DC-link current to the reference value. The CSI unit vectors, generated from the motor *d-q* reference currents and the capacitor *d-q* currents, are transformed into three-phase modulating signal for the PWM generation section. The PWM pulses suitable for the CSI are adapted using the mapping circuit. The function of the CSI is to adjust the phase and frequency of the motor input current.

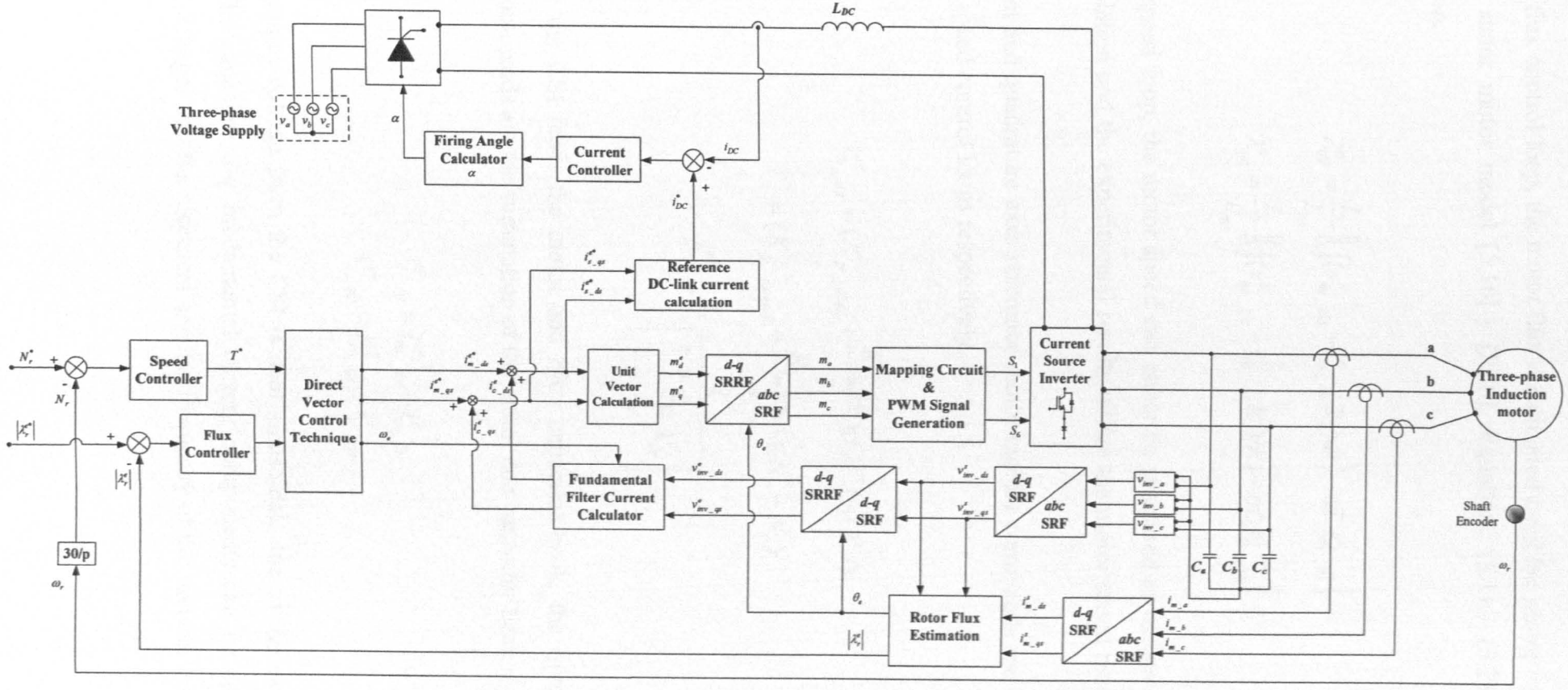


Figure 5.8: Direct vector controlled PWM CSI drive block diagram.

For the flux control loop, the motor flux is estimated from the motor voltages and currents using a stator motor model [5.16] - [5.20]. Equations (5.1) - (5.2) describe the flux estimation.

$$\lambda_{dr}^{s} = \frac{L_r}{L_m}\left[\left(\int (v_{m\_ds}^{s} - i_{m\_ds}^{s} R_s)dt\right) - \sigma L_s i_{m\_ds}^{s}\right] \tag{5.1}$$

$$\lambda_{qr}^{s} = \frac{L_r}{L_m}\left[\left(\int (v_{m\_qs}^{s} - i_{m\_qs}^{s} R_s)dt\right) - \sigma L_s i_{m\_qs}^{s}\right] \tag{5.2}$$

For the speed loop, the motor speed can either be measured or estimated. In this chapter, the simulation and the experimental results utilize the motor speed measured with a shaft encoder.

The direct and quadrature axes reference motor current commands are generated from the flux and speed control loops respectively.

$$i_{m\_ds}^{e*} = (K_{p\_flux} + \frac{K_{i\_flux}}{s})(|\lambda_r^{e*}| - |\lambda_r^{e}|) \tag{5.3}$$

$$T^{*} = (K_{p\_speed} + \frac{K_{i\_speed}}{s})(N_r^{*} - N_r) \tag{5.4}$$

$$i_{m\_qs}^{e*} = \frac{T^{*}}{\left[\frac{3}{2}\frac{P}{2}\frac{L_m}{L_r}\lambda_{dr}^{e}\right]} \tag{5.5}$$

Since the CSI feeds the motor and filter capacitor bank, the inverter *d-q* reference current commands are the summation of the motor and capacitor bank *d-q* currents.

$$i_{s\_ds}^{e*} = i_{m\_ds}^{e*} + i_{c\_ds}^{e} \tag{5.6}$$

$$i_{s\_qs}^{e*} = i_{m\_qs}^{e*} + i_{c\_qs}^{e} \tag{5.7}$$

The output voltage from the CSI is near sinusoidal, due to the capacitor bank filter action. The capacitor *d-q* fundamental current components can be calculated from the capacitor voltages and the electrical angular frequency of the inverter output currents [5.1] - [5.3].

$$i^e_{c\_ds} = -\omega_e C v^e_{inv\_qs} \tag{5.8}$$

$$i^e_{c\_qs} = \omega_e C v^e_{inv\_ds} \tag{5.9}$$

The DC-link reference current must be greater than the inverter reference current. The current source rectifier controller adjusts the DC-link current to the reference value [5.1 - 5.3].

$$i^*_{DC} = K_{DC}\sqrt{(i^{e*}_{s\_ds})^2 + (i^{e*}_{s\_qs})^2} \tag{5.10}$$

where $K_{DC} > 1$

The main concept behind direct vector control is to calculate the transformation angle θ_e from the rotor flux, estimated from the motor voltages and currents.

$$\theta_e = \tan^{-1}\left(\frac{\lambda^s_{qr}}{\lambda^s_{dr}}\right) \tag{5.11}$$

Since the CSI is used to control the frequency and phase of the ouput three phase currents, the modulating signals to the CSI must have a unity peak. A unit vector generation procedure is needed to generate the modulating signal from the reference *d-q* currents as shown in (5.12) and (5.13). The modulating signals in the rotating reference frame (m^e_{dq}) are DC quantities. After transformation from the synchronously rotating reference frame to the stationary reference frame, the resultant modulating signals in the stationary reference frame (m_{abc}) are three phase sinusoidal signals with unity peak values, ± 1. The frequency and phase of these signals can be changed by varying their components in the synchronously rotating reference frame (m^e_{dq}).

$$m^e_d = \frac{i^{e*}_{s\_ds}}{\sqrt{(i^{e*}_{s\_ds})^2 + (i^{e*}_{s\_qs})^2}} \tag{5.12}$$

$$m^e_q = \frac{i^{e*}_{s\_qs}}{\sqrt{(i^{e*}_{s\_ds})^2 + (i^{e*}_{s\_qs})^2}} \tag{5.13}$$

5.2.2 Performance analysis

The system under study is a scaled low-voltage model similar to the system used in chapter four. Direct vector controlled PWM CSI drive performance analysis is carried out by examining the drive system at start-up and during loading conditions. A reference step speed command of 300 rpm is generated and a load of 4 Nm is applied after 10 s. The switching frequency is 1 kHz, to match a practical MV drive. Tracking of the motor actual speed to the reference command at start-up and during loading conditions, are shown in figure 5.9 parts (a) and (b) respectively. The direct and quadrature rotor flux components in both loading conditions are shown in figure 5.9 parts (c) and (d) respectively. The torque response at start-up and during loading conditions is shown in figure 5.9 parts (e) and (f) respectively.

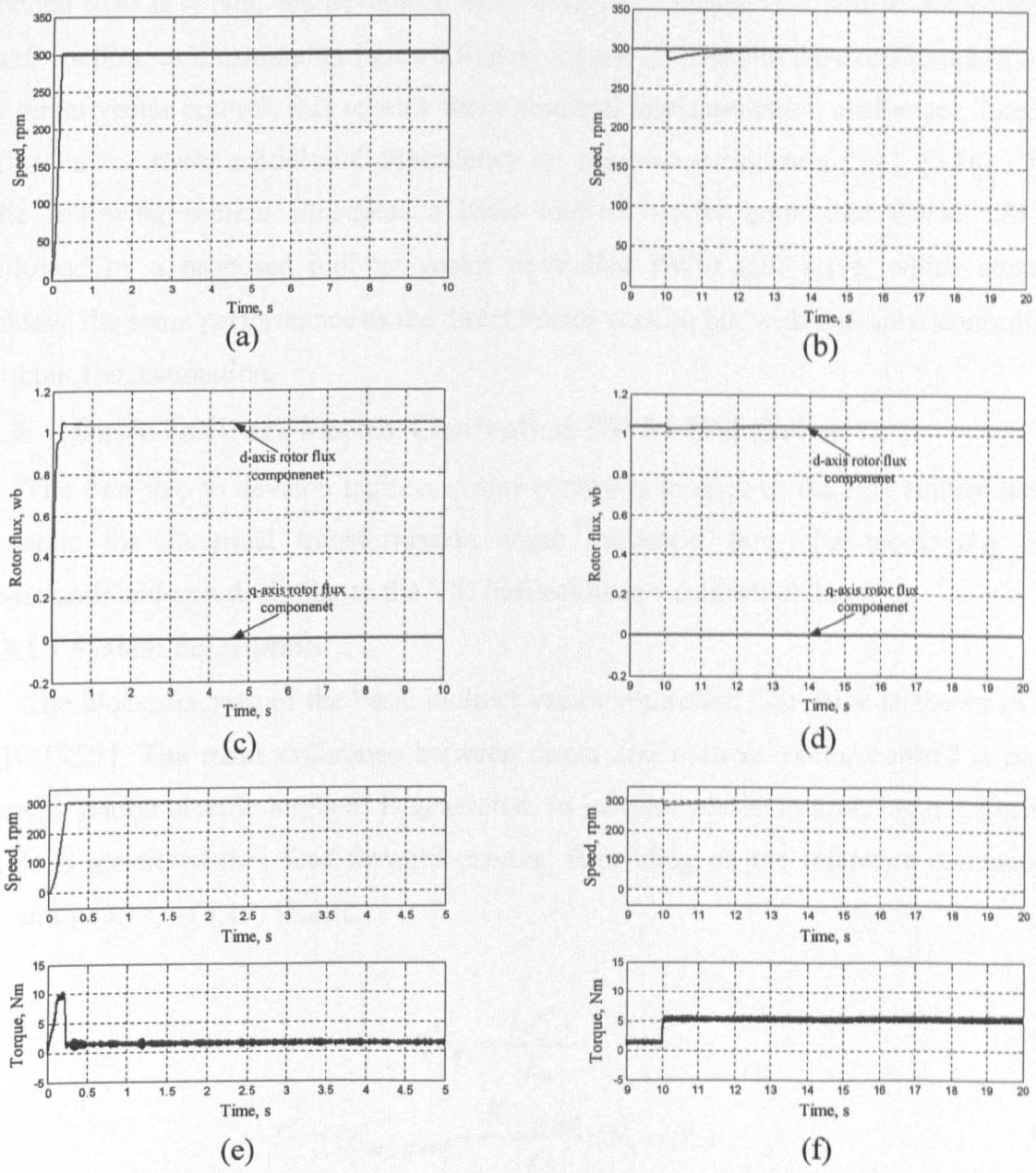


Figure 5.9: Direct vector controlled PWM CSI drive simulation results
a, c and e: Step response no-load b,d and f: Sudden load change
(a) and (b) reference and actual motor speed, (c) and (d) rotor flux *d-q* components, and (e) and (f) motor speed and developed electromagnetic torque.

The simulation results in figure 5.9 parts (a) to (f) show that the drive system can control the motor speed in conditions, start-up and a sudden load change. A step command of 300 rpm is set as a step reference, and then a load of 4 Nm is applied after 10 s. Figure 5.9 parts (a) and (b) show that the motor speed tracks the reference speed command during both conditions. The principle of field orientation is verified, forcing the quadrature component of the rotor flux to zero, as shown in figure 5.9 parts (c) and (d). Although the

applied load is 4 Nm, the developed electromagnetic torque is 5 Nm to compensate the shaft friction, as illustrated in figure 5.9 parts (e) and (f). Despite the excellent performance of direct vector control, this scheme faces practical implementation challenges, like a DC-offset in the stator model and dependency on machine parameters [5.1], [5.16] - [5.19]. The following section illustrates a basic indirect vector controlled PWM CSI drive followed by a proposed indirect vector controlled PWM CSI drive, which attempt to achieve the same performance as the direct vector version but with a simpler controller and without flux estimation.

5.3 Basic Indirect Vector Controlled PWM CSI Drive

The first step to develop indirect vector control is to remove the flux control loop and generate the electrical transformation angle indirectly from the motor *d-q* current commands and speed, similar to the VSI indirect vector controlled drive.

5.3.1 System description

The block diagram of the basic indirect vector controlled CSI drive is shown in figure 5.10 [5.21]. The main difference between direct and indirect vector control is how the transformation electric angle θ_e is generated. In indirect vector control, the transformation angle is generated in a feed forward manner, depending on the reference commands, as given by (5.14) - (5.19) [5.20].

$$i_{m\_ds}^{e*} = \frac{/\lambda_r^{e*}/}{L_m} \tag{5.14}$$

$$T^* = (K_{p\_speed} + \frac{K_{i\_speed}}{s})(N_r^* - N_r) \tag{5.15}$$

$$i_{m\_qs}^{e*} = \frac{T^*}{\left[\frac{3}{2}\frac{P}{2}\frac{L_m}{L_r}\lambda_{dr}^{e*}\right]} \tag{5.16}$$

$$\omega_{slip} = \frac{R_r}{L_r} \cdot \frac{i_{m\_qs}^{e*}}{i_{m\_ds}^{e*}} \tag{5.17}$$

$$\omega_e = \omega_{slip} + \omega_r \tag{5.18}$$

$$\theta_e = \int \omega_e \tag{5.19}$$

The process of DC current reference generation, inverter modulating signal generation, DC-link current control, and CSI control, is similar to the direct vector control case. The

main advantage of this type of vector control is that there is no flux estimation process, so the control process is simpler and less sensitive to the machine parameter variation [5.20], [5.21].

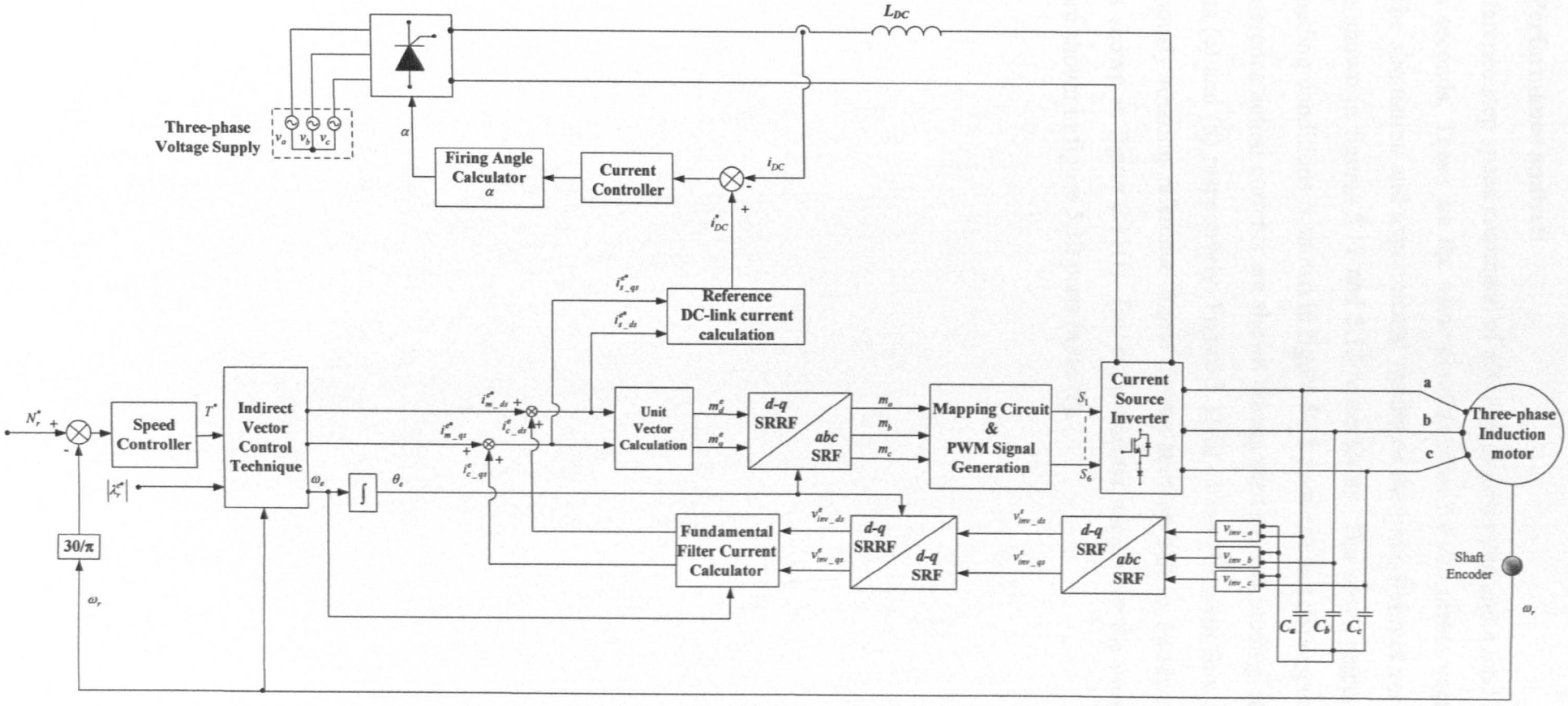


Figure 5.10: Basic indirect vector controlled CSI drive.

5.3.2 Performance analysis

A reference step speed command of 300 rpm is generated and a load of 4 Nm is applied after ten seconds. These are the same conditions as for the direct vector controlled CSI drive. The simulation and experimental results of the basic indirect vector controlled CSI drive are shown in figures 5.11 and 5.12 respectively. The speed response at start-up and during loading conditions is shown in figure 5.11 parts (a) and (b) respectively. The q-axis motor reference/actual currents are shown during start-up and loading conditions in figure 5.11 parts (c) and (d) respectively. Figure 5.11(e) shows the rotor flux components in the synchronously rotating reference frame during start-up and in steady-state. The start-up torque is shown in figure 5.11(f). The experimental results for the previously mentioned signals are shown in figure 5.12 parts (a) to (f).

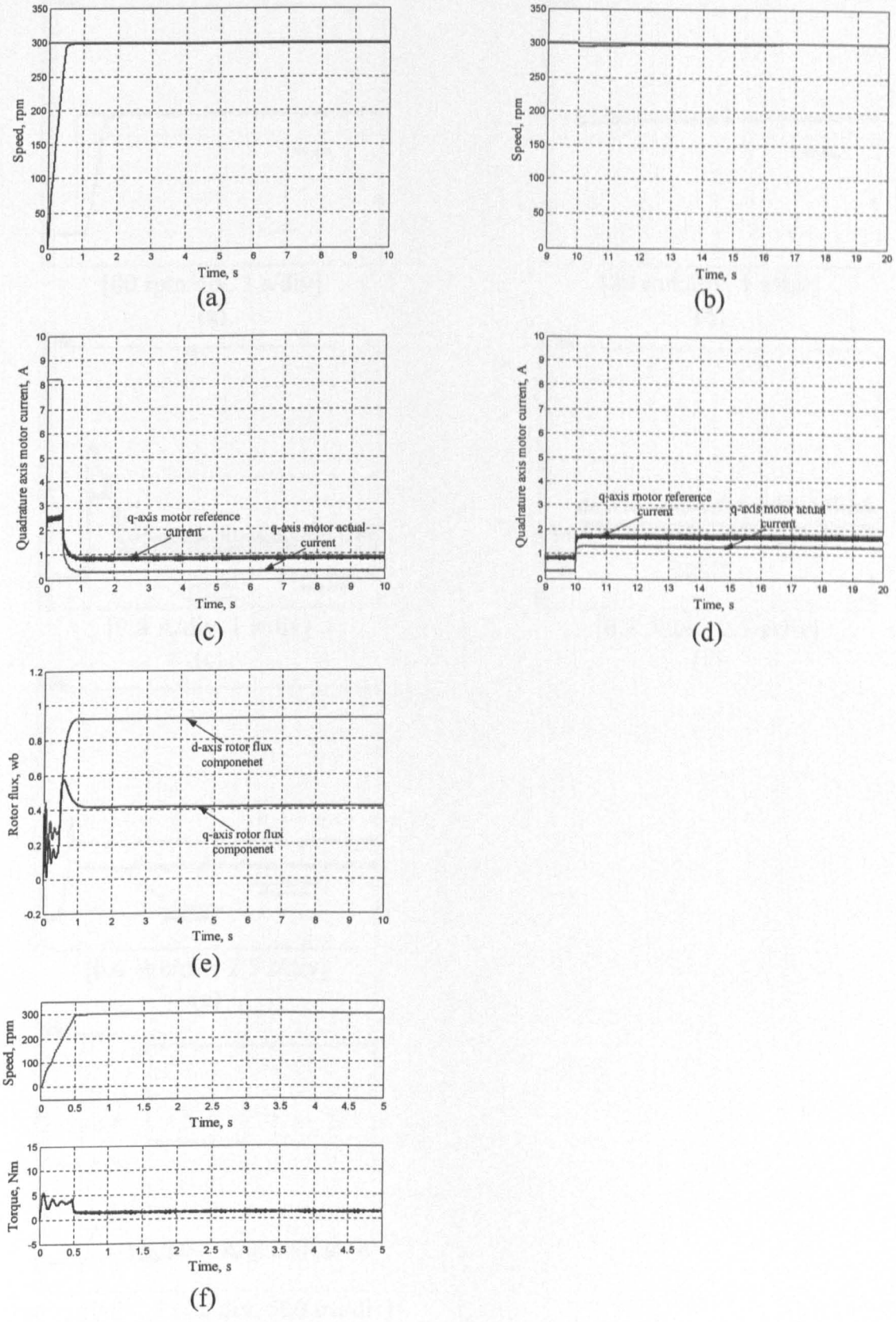
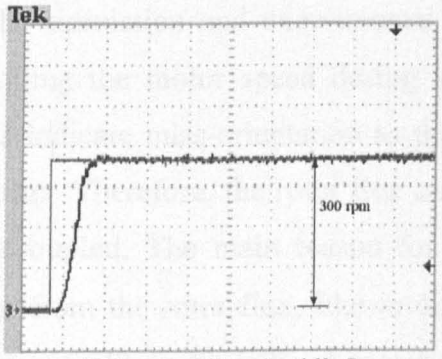
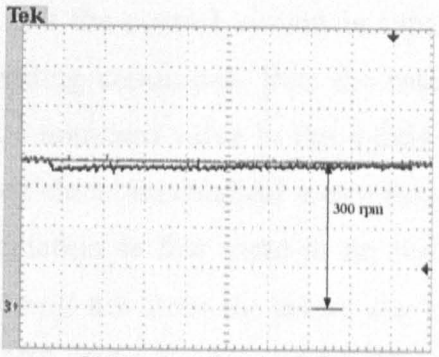


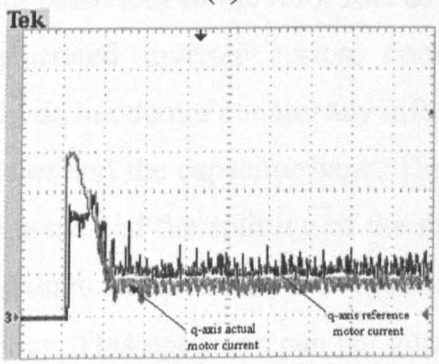
Figure 5.11: Basic indirect vector controlled PWM CSI drive simulation results
a, c, e and f: Step response no-load b and d: Sudden load change
(a) and (b) reference and actual motor speed, (c) and (d) reference and actual q-axis motor current component, (e) rotor flux d-q components, and (f) motor speed and developed electromagnetic torque.



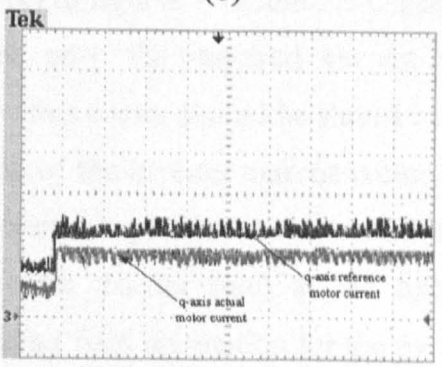
[80 rpm/div, 1 s/div]
(a)



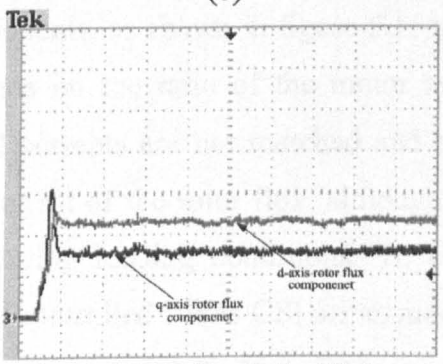
[80 rpm/div, 1 s/div]
(b)



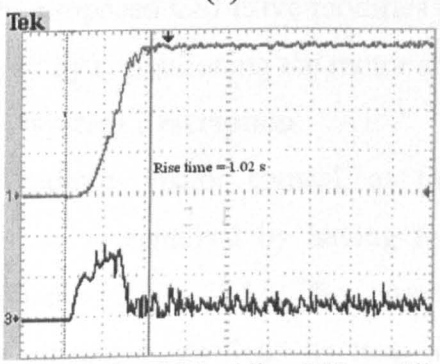
[0.8 A/div, 1 s/div]
(c)



[0.8 A/div, 2.5 s/div]
(d)



[0.4 Wb/div, 2.5 s/div]
(e)



[80 rpm/div, 3 Nm/div, 500 ms/div]
(f)

Figure 5.12: Basic indirect vector controlled PWM CSI drive experimental results
a, c, e and f: Step response no-load b and d: Sudden load change
(a) and (b) reference and actual motor speed, (c) and (d) reference and actual *q*-axis motor current component, (e) rotor flux *d-q* components, and (f) motor speed and developed electromagnetic torque.

The simulation and experimental results show that the control system is capable of controlling the motor speed during starting and loading conditions. But, the rotor flux results indicate miss-orientation as there still exists a non-zero value in the q-axis of the rotor flux. Therefore, the rotor flux and the developed electromechanical motor torque are not decoupled. The main reason for this miss-orientation is that there is no feedback, neither from the rotor flux, like in direct vector control, nor from the motor d-q current components, like with indirect vector control of the VSI. This clearly explains the random start-up behaviour of the rotor flux as shown in part (e) in figures 5.12 and 5.13. Therefore the generated inverter current commands present only the required current vector magnitude but do not contain any information on how this vector should be shared between the motor and the capacitor bank. The decomposition of the inverter current vector to d-q components and the splitting of the motor and capacitor components are determined from the capacitor and the motor impedance ratio (current divider rule) at the operating frequency. This operation can not guarantee the required field orientation for the motor, as the actual d-q current components are not compelled to match the motor reference d-q components, as shown in figure 5.11 and 5.12 parts (e) and (f). The motor injected amount depends on the ratio of the motor and capacitor impedances. The motor reference and actual currents are not matched and there still exists a non-zero value for the quadrature component of the rotor flux, although the motor fulfils the required speed at both start-up and during loading conditions. To overcome the miss-orientation in the basic indirect vector controlled PWM CSI drive, modification is mandatory.

5.4 Proposed Indirect Vector Controlled PWM CSI Drive

The proposed CSI drive modifies basic CSI indirect vector control. Field orientation is achieved by repositioning the motor and capacitor d-q current components.

5.4.1 System description

In indirect vector control, as for the VSI drive discussed in chapter four, field orientation is achieved by having two current control loops for the d-q motor current components [5.1] - [5.3]. This process is straight forward since the inverter is voltage source current controlled. As long as these control loops function correctly, matching between the reference and actual d-q motor current components ensures proper field orientation [5.20].

The problem with the CSI is that the magnitude of the inverter output current is varied from the rectifier side while the inverter changes the frequency and phase of this vector. So, implementation of straight forward *d-q* current control loops in the CSI case is not applicable.

The miss-orientation problem occurs in the basic indirect vector controlled CSI drive because of the mismatch between the motor reference and actual current (as there is no current control on the *d-q* current components). Therefore, the idea behind the proposed indirect vector control is to vary the phase of the inverter output current until the error between the reference and the actual *d-q* motor current components is minimal. At this point, field orientation is achieved similar to that of VSI indirect vector control. The inverter output current phase is compelled to change by adding two control loops for the *d-q* motor current components thus varying the *d-q* modulating signals of the CSI which are responsible for the inverter output current phase and frequency variation. The block diagram of the proposed indirect vector controlled PWM CSI drive, with the modified current control surrounded by a dotted rectangle, is shown in figure 5.13

The CSI modulating signal is not generated from the reference inverter current commands, like the basic indirect vector, but is now generated from the error between the reference and actual *d-q* motor current components.

$$m_d^{e/} = (K_{p\_d} + \frac{K_{i\_d}}{s}).(i_{m\_ds}^{e*} - i_{m\_ds}^{e}) \tag{5.20}$$

$$m_q^{e/} = (K_{p\_q} + \frac{K_{i\_q}}{s}).(i_{m\_qs}^{e*} - i_{m\_qs}^{e}) \tag{5.21}$$

$$m_d^e = \frac{m_d^e}{\sqrt{(m_d^{e/})^2 + (m_q^{e/})^2}} \tag{5.22}$$

$$m_q^e = \frac{m_q^e}{\sqrt{(m_d^{e/})^2 + (m_q^{e/})^2}} \tag{5.23}$$

Therefore the phase of the inverter current command is varied until the reference and actual *d-q* motor current components are nearly equal. Field orientation and decoupling are thus achieved.

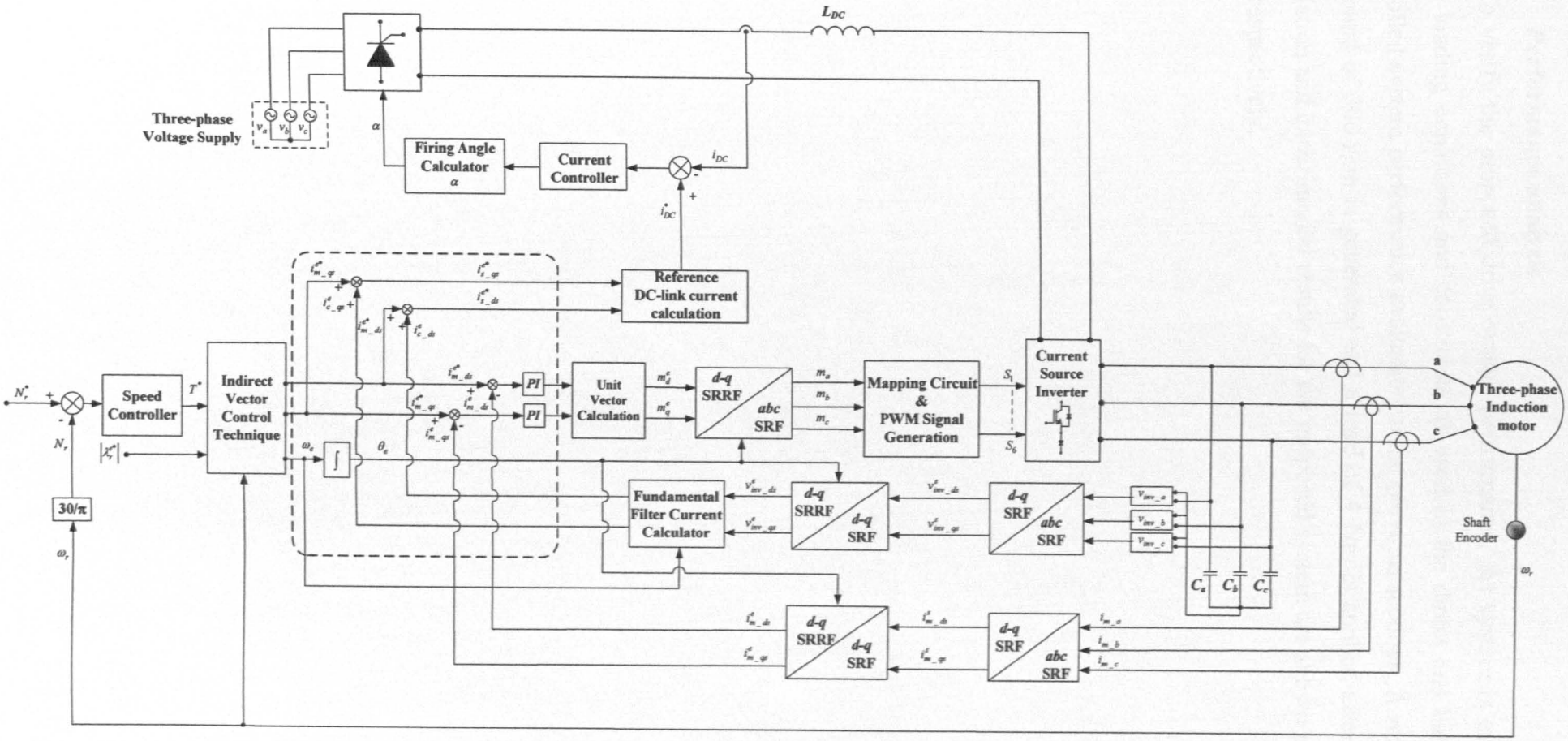
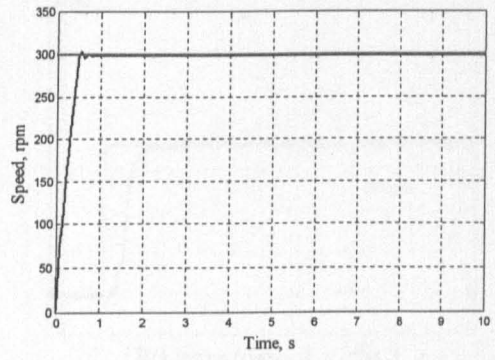


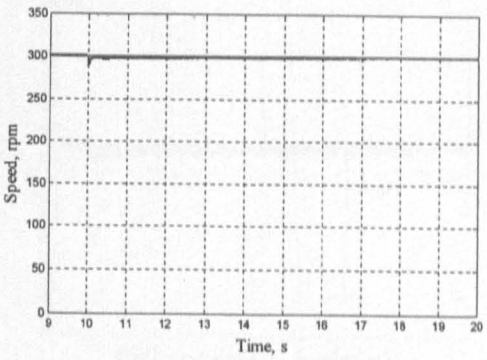
Figure 5.13: Proposed indirect vector controlled PWM CSI drive block diagram.

5.4.2 Performance analysis

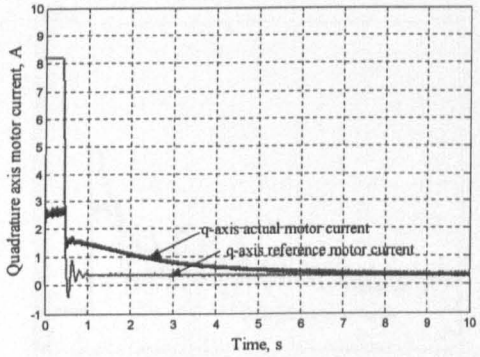
To verify the proposed drive system performance, the system is examined under the same loading conditions and constraints as used in the direct and basic indirect vector controlled system performance evaluation in the previous sections. A reference step speed command of 300 rpm is generated and a load of 4 Nm is applied after ten seconds. The simulation and experimental results for the proposed system are shown in figures 5.14 and 5.15 respectively.



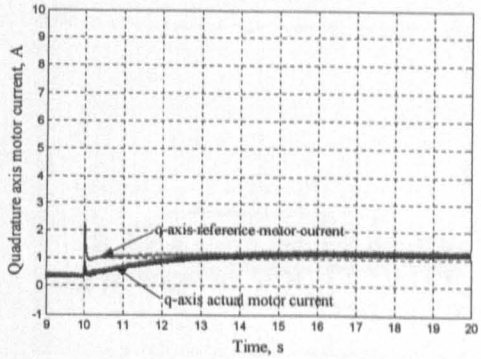
(a)



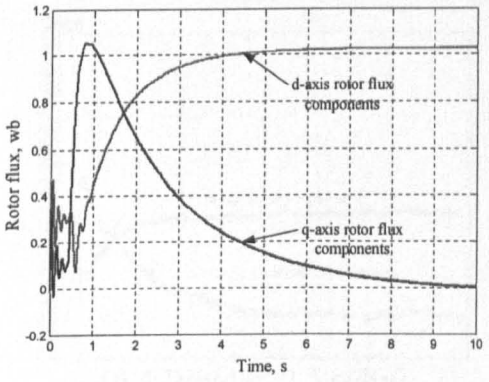
(b)



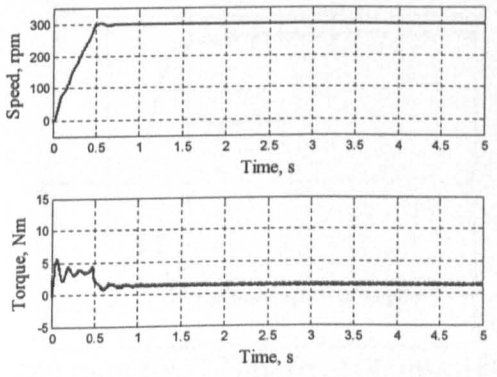
(c)



(d)

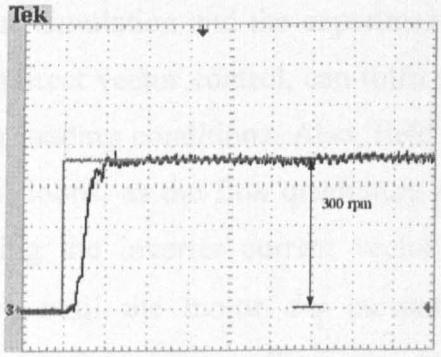


(e)

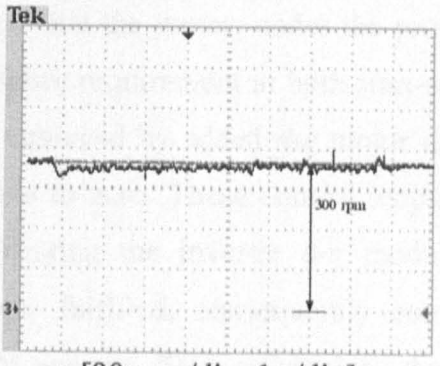


(f)

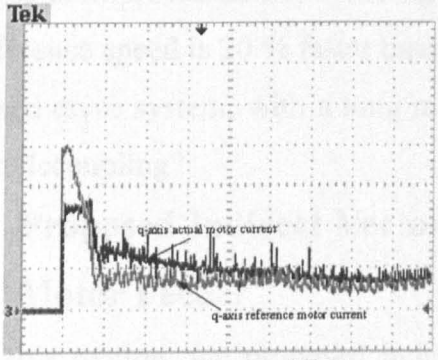
Figure 5.14: Proposed indirect vector controlled PWM CSI drive simulation results
a, c, e and f: Step response no-load b and d: Sudden load change
(a) and (b) reference and actual motor speed, (c) and (d) reference and actual q-axis motor current component, (e) rotor flux d-q components, and (f) motor speed and developed electromagnetic torque.



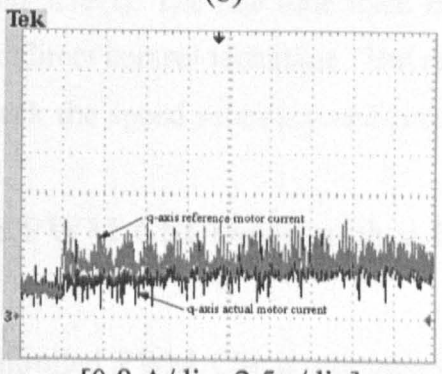
[80 rpm/div, 1 s/div]
(a)



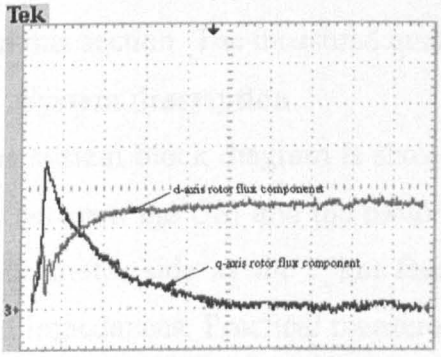
[80 rpm/div, 1 s/div]
(b)



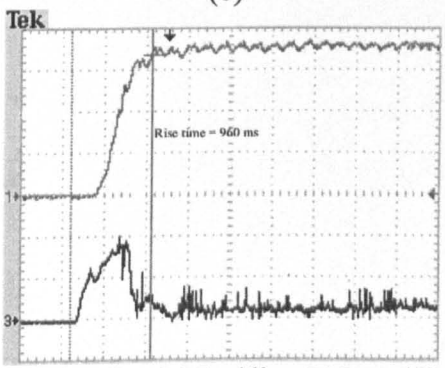
[0.8 A/div, 1 s/div]
(c)



[0.8 A/div, 2.5 s/div]
(d)



[0.4 Wb/div, 2.5 s/div]
(e)



[80 rpm/div, 3 Nm/div, 500 ms/div]
(f)

Figure 5.15: Proposed indirect vector controlled PWM CSI drive experimental results
a, c, e and f: Step response no-load b and d: Sudden load change
(a) and (b) reference and actual motor speed, (c) and (d) reference and actual q-axis motor current component, (e) rotor flux d-q components, and (f) motor speed and developed electromagnetic torque.

The simulation and the experimental results show that the motor, under the proposed CSI indirect vector control, can fulfil the speed reference requirement at both start-up and during loading conditions. Also, field orientation is achieved by added *d-q* motor current control loops, as the flux quadrature component tends to zero. These control loops keep changing the inverter current vector phase, by changing the inverter *d-q* modulating signals, until the motor *d-q* current commands are fulfilled, consequently complete orientation is achieved. Since the proposed control ensures field orientation, the step response is improved as shown in figures 5.12(f) and 5.15(f). The rise time from zero to the reference speed is 20 % faster than for the basic indirect control technique. But can the proposed drive system, with a long motor feeder, track the speed reference and preserves system decoupling?

5.5 Proposed Indirect Vector Controlled PWM CSI Drive with a Long Motor Feeder

In this section, the proposed indirect vector controlled PWM CSI is examined with long motor feeders. A π-network lumped impedance model for a one kilometre cable is used in this section. The measured quantities are the motor voltages, currents, and speed.

5.5.1 System description

The system block diagram is shown in figure 5.16 where a 1 km long feeder model is placed between the CSI and the motor. The motor voltages and currents can be measured from the motor side as the 1 km feeder does not physically exist but is represented by lumped impedances. Practical measurements problems and indirect measurement, for long feeders, are considered later in this thesis.

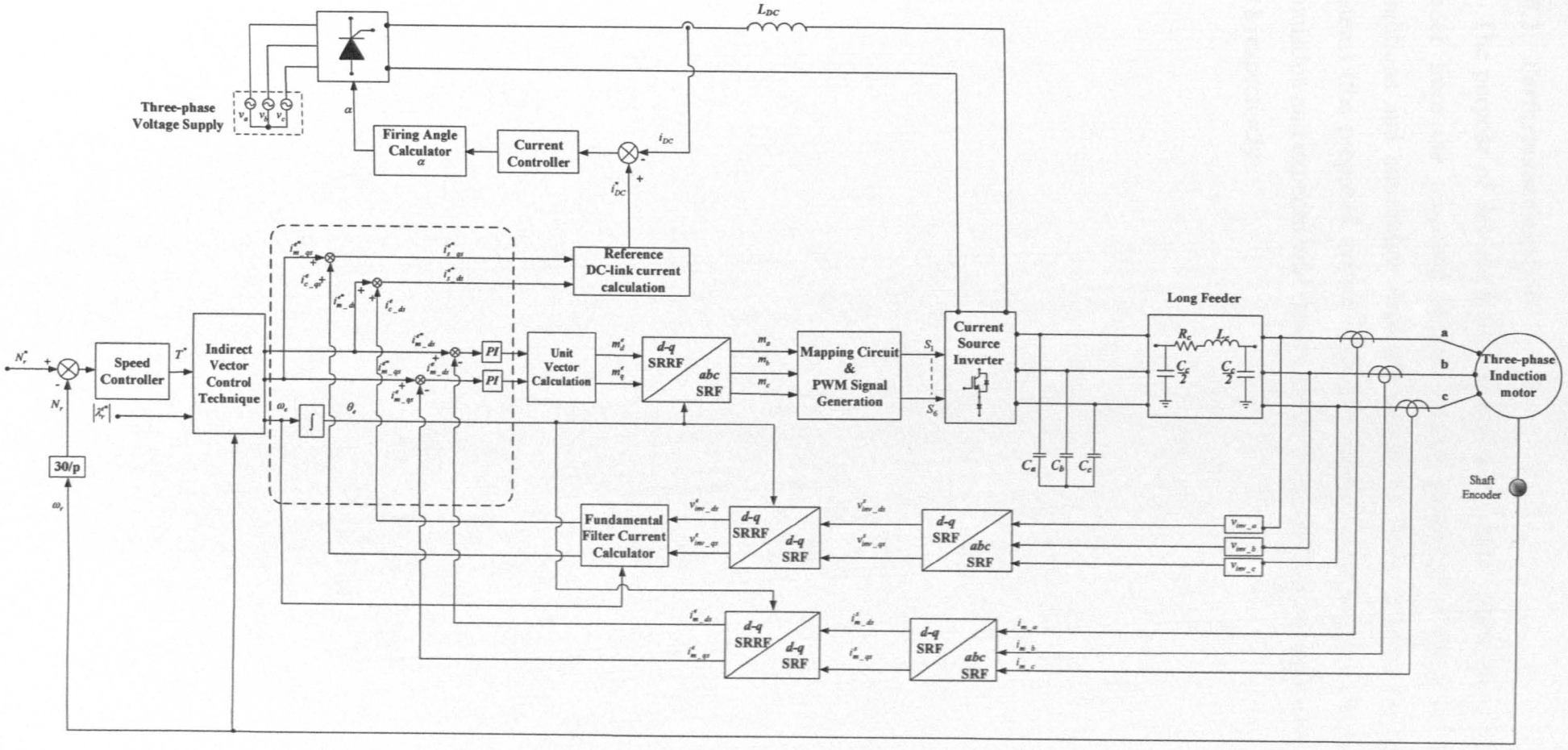
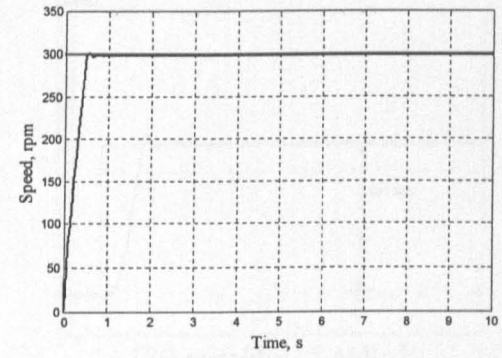


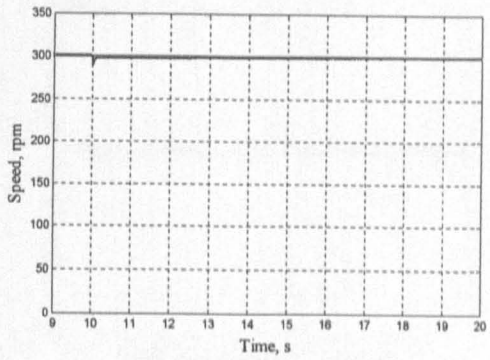
Figure 5.16: Proposed indirect vector controlled PWM CSI drive block diagram with long motor feeder.

5.5.2 Performance analysis

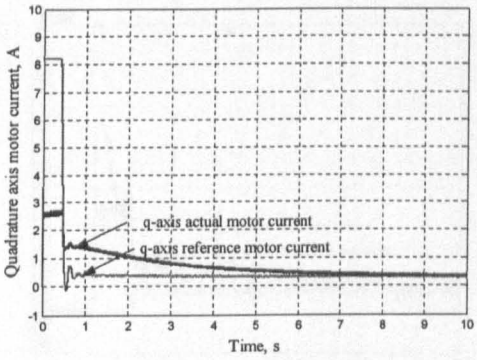
The purpose of this study is to examine the motor performance when fed via a long feeder from the proposed indirect vector controlled PWM CSI drive. The loading conditions and constraints used are similar to those used in the previously discussed systems (the proposed system without a feeder) to allow performance comparison. The simulation and experimental results for the proposed system are shown in figures 5.17 and 5.18 respectively



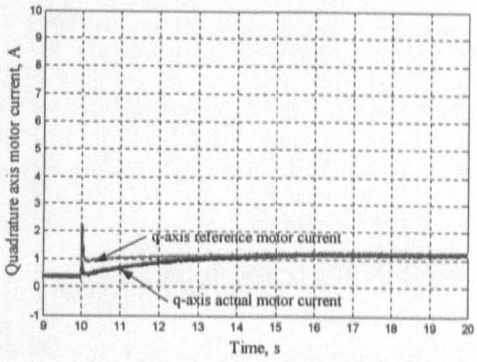
(a)



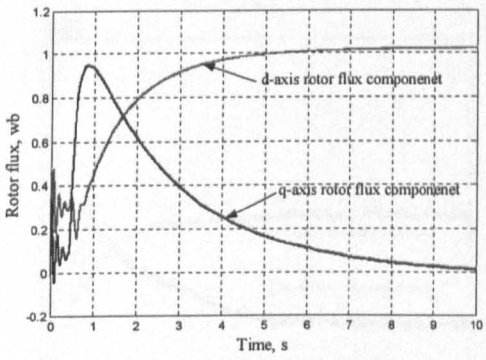
(b)



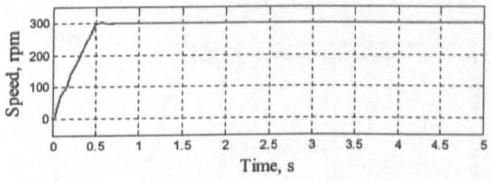
(c)

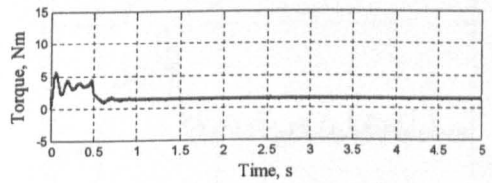


(d)



(e)



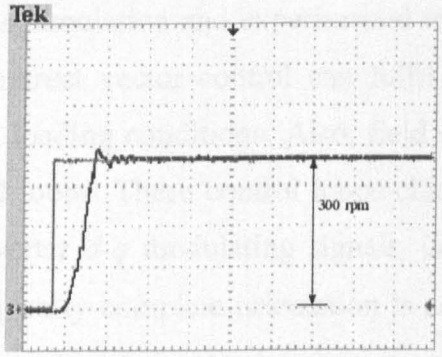


(f)

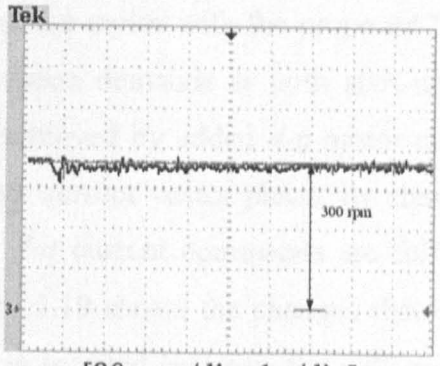
Figure 5.17: Proposed indirect vector controlled PWM CSI drive with long motor feeder simulation results

a, c, e and f: Step response no-load b and d: Sudden load change

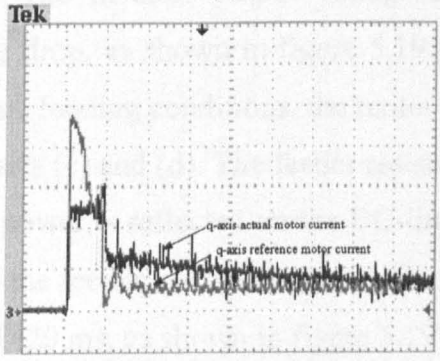
(a) and (b) reference and actual motor speed, (c) and (d) reference and actual q-axis motor current component, (e) rotor flux d-q components, and (f) motor speed and developed electromagnetic torque.



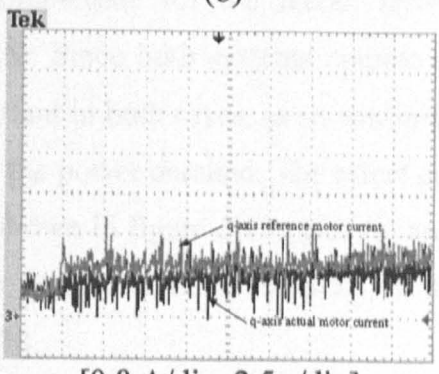
[80 rpm/div, 1 s/div]
(a)



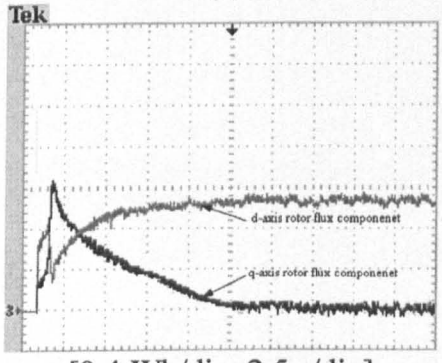
[80 rpm/div, 1 s/div]
(b)



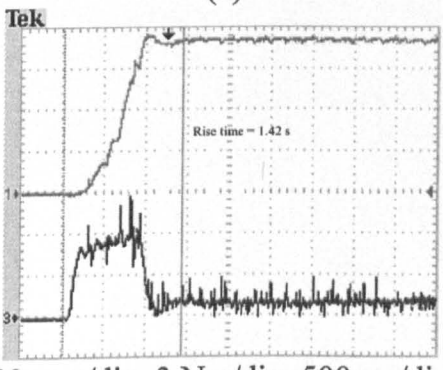
[0.8 A/div, 1 s/div]
(c)



[0.8 A/div, 2.5 s/div]
(d)



[0.4 Wb/div, 2.5 s/div]
(e)



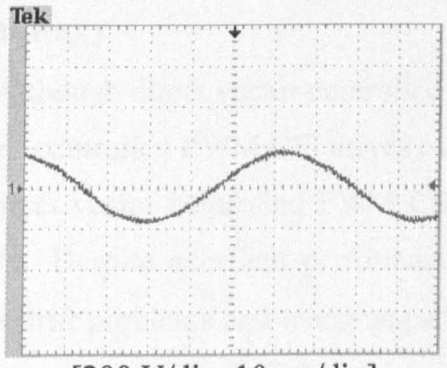
[80 rpm/div, 3 Nm/div, 500 ms/div]
(f)

Figure 5.18: Proposed indirect vector controlled PWM CSI drive with long motor feeder experimental results

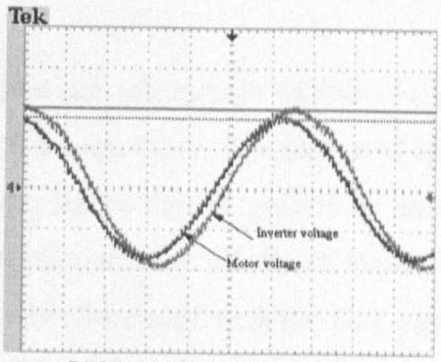
a, c, e and f: Step response no-load b and d: Sudden load change

(a) and (b) reference and actual motor speed, (c) and (d) reference and actual q-axis motor current component, (e) rotor flux d-q components, and (f) motor speed and developed electromagnetic torque.

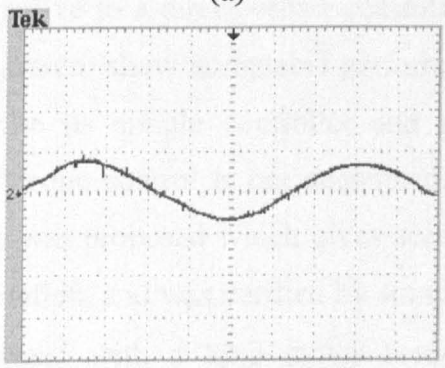
The simulation and experimental results show that the motor with the proposed PWM CSI indirect vector control can fulfil the required speed demands at both start-up and during loading conditions. Also, field orientation is achieved by added *d-q* motor current control loops. These control loops change the inverter current vector phase, by changing the inverter *d-q* modulating signals, until the motor *d-q* current commands are fulfilled, consequently complete orientation is achieved. Figure 5.19 shows the changes that occur on the system voltages and currents when a feeder is inserted between the CSI and the motor. The inverter output voltage increases to compensate for the feeder resistance voltage drop, as shown in figure 5.19 parts (a) and (b). Since both systems operate under the same loading conditions, the motor current is constant in both cases, as shown in figure 5.19 parts (c) and (d). The feeder resistance increases the power demand. The effect on this added power is reflected on the DC-link voltage, as shown in figure 5.19 parts (e) and (f). Due to the feeder voltage drop, the speed rise time for a step command increases, from 960 ms to 1420 ms, as shown in figure 5.19 parts (g) and (h).



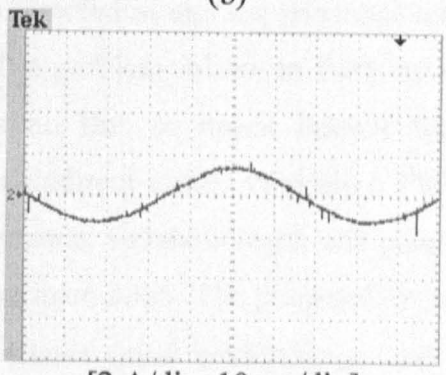
[200 V/div, 10 ms/div]
(a)



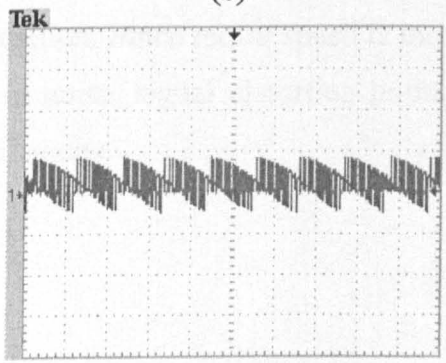
[100 V/div, 10 ms/div]
(b)



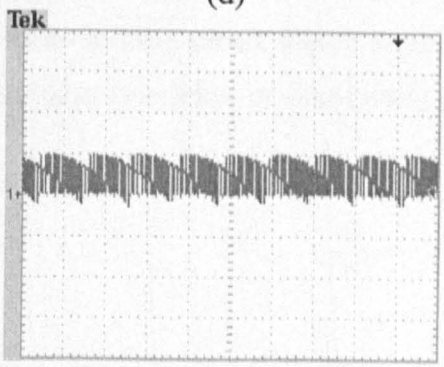
[2 A/div, 10 ms/div]
(c)



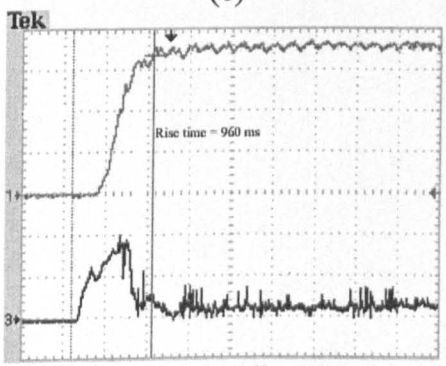
[2 A/div, 10 ms/div]
(d)



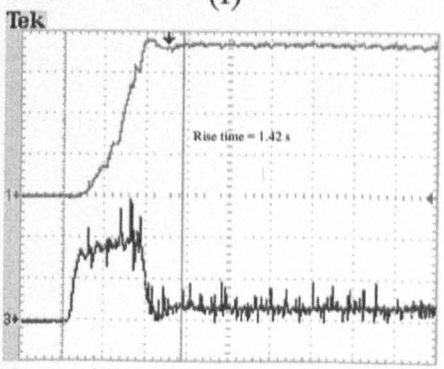
[200 V/div, 10 ms/div]
(e)



[200 V/div, 10 ms/div]
(f)



[80 rpm/div, 3 Nm/div, 500 ms/div]
(g)



[80 rpm/div, 3 Nm/div, 500 ms/div]
(h)

Figure 5.19: Proposed indirect vector controlled PWM CSI drive experimental results without/with motor feeder

a, c, e and g: No feeder b, d, f and h: 1 km feeder

(a) and (b) inverter/motor voltage, (c) and (d) motor current, (e) and (f) DC-link voltage, and (g) and (h) motor speed and developed electromagnetic torque.

Summary

Although direct vector controlled PWM VSI drives are common in MV drives, indirect vector controlled PWM CSI drives can be considered a competitor. The theory of operation of direct vector controlled PWM CSI drives was explained briefly guided by simulation results. Despite excellent performance, practical implementation of direct vector control faces drift problems and machine parameter sensitivity associated with the flux estimation process. Hence a basic indirect vector controlled PWM CSI drive was investigated as an alternative to a direct vector controlled drive. The simulation and experimental results of this system show acceptable performance, but with a problem related to field orientation. Despite its simple controller and since there is no flux or motor current feedback, flux/torque control is not decoupled. Therefore, an indirect vector controlled PWM CSI drive was proposed which gives acceptable performance, simple control, and proper field orientation, and was verified by simulation and experimentation. The proposed system was examined with a long motor feeder, where it shows good performance and robust orientation. The practical implementation of a vector controlled drive requires speed acquisition. Since motor speed is impractical to measure in long motor feeder applications, due to noise, signal distortion limitations etc., sensorless operation is mandatory in such applications.

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CHAPTER SIX:

Comparison between PWM VSI and PWM CSI Vector Controlled Drives, with Long Motor Feeder

Indirect vector controlled induction motor drives can utilize a PWM VSI or a PWM CSI. The theory of operation of conventional long motor feeder, indirect vector controlled, PWM VSI drives, with two filter networks was presented and compared in chapter four. In chapter five, an indirect vector controlled PWM CSI drive was proposed and examined with a long motor feeder, where acceptable system performance was achieved. The question that arises is which drive (VSI or CSI) provides better performance. Moreover, the drawbacks and limitations of each drive system should also be highlighted and addressed. The answer requires analysis, aided with simulation and experimentation. In this chapter, a comparison is undertaken between an indirect vector controlled PWM VSI drive, with an inverter output *RLC* filter, and the proposed indirect vector controlled PWM CSI drive. The comparison is presented in six stages.

6.1 Compared Drive Systems

In this section, VSI and CSI indirect vector controlled drives are presented with block diagrams and short descriptions. A study of and comparison between the two drive systems is presented in the following subsections.

6.1.1 Indirect vector controlled PWM VSI induction motor drive

Figure 6.1 shows the block diagram of the VSI indirect vector controlled drive. Since this study is concerned with long motor feeder issues, the inverter output *RLC* filter topology is selected [6.1]. This filter topology limits motor over-voltage when the VSI is used with a long feeder. It is concluded in chapter four that an *RLC* inverter output filter exhibits lower losses than a *RC* motor terminal filter. Also, the placement of the *RC* filter at the motor terminal may not suit many applications, like in underground mines and on submersible pumps, because of its size and weight.

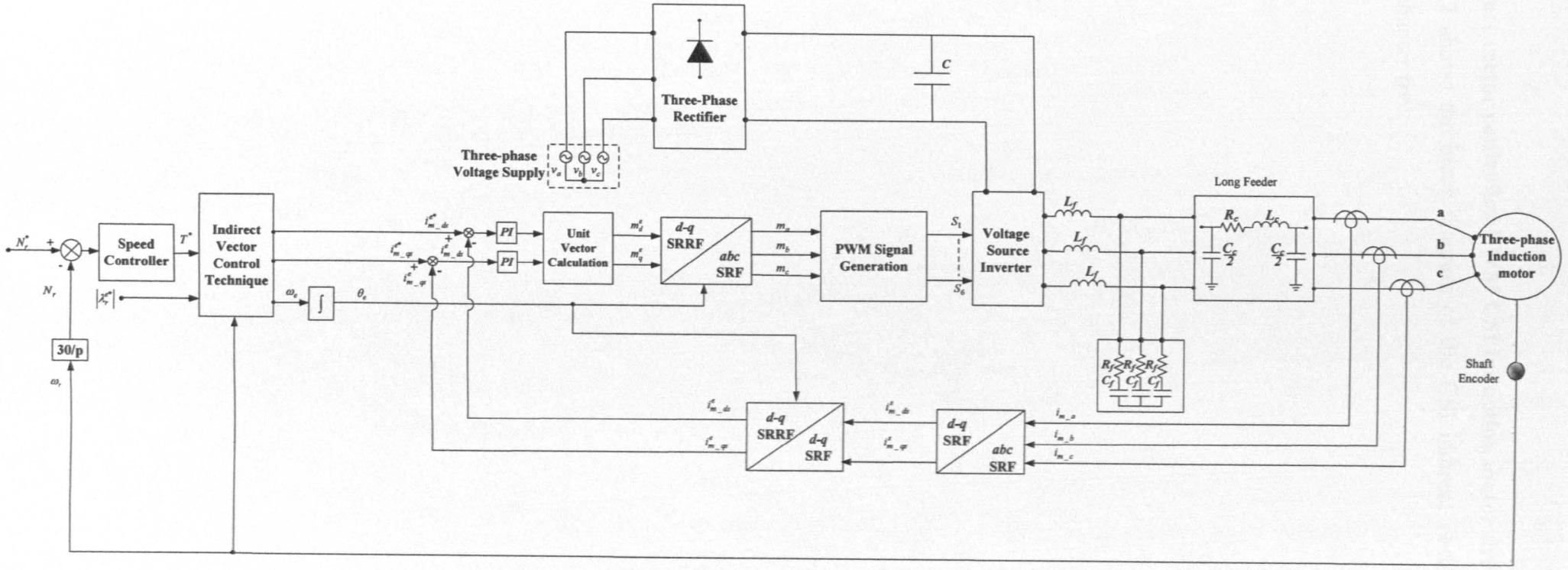


Figure 6.1: Long motor feeder indirect vector controlled PWM VSI drive.

6.1.2 Indirect vector controlled PWM CSI induction motor drive

Figure 6.2 shows the block diagram of the CSI indirect vector controlled drive, as proposed in chapter five.

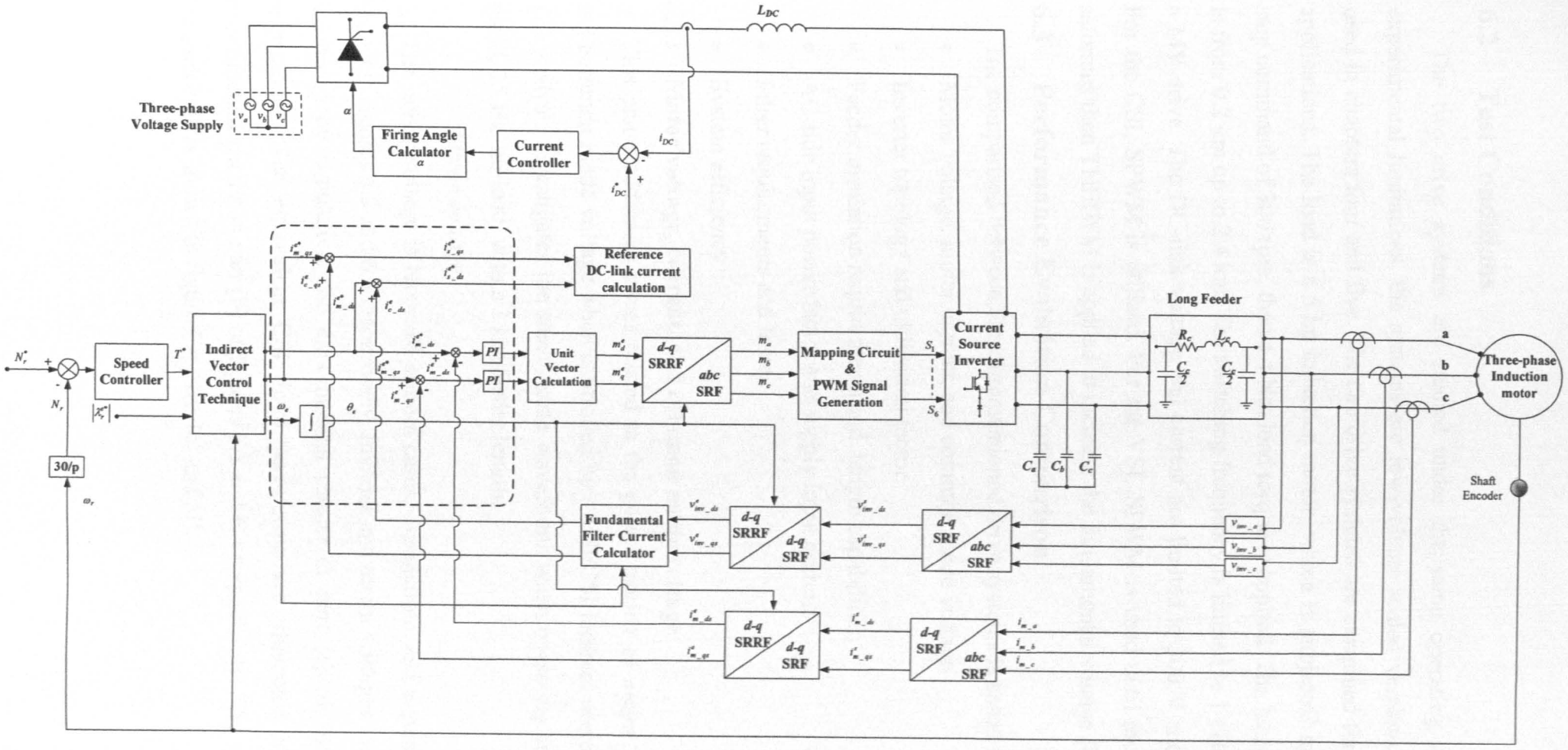


Figure 6.2: Long motor feeder proposed indirect vector controlled PWM CSI drive.

6.2 Test Conditions

The two drive systems are studied under the same operating conditions. Due to experimental limitations, the systems are low-voltage scaled versions of MV drives, as used in chapters four and five. The two drive systems are examined for long motor feeder applications. The load is a 5 hp induction motor, which is subjected to a reference speed step command of 300 rpm, then a 4 Nm load torque is applied. The feeder length test range is from 0.2 km up to 2.4 km. The switching frequency is limited to 1 kHz, similar to that of a MV drive. The DC-link voltage and current are limited to 300 V and 3 A respectively. For the CSI, SPWM is utilized. For the VSI, SPWM is used until the modulation index saturates then THIPWM is applied to increase the fundamental voltage [6.3].

6.3 Performance Evaluation Comparison

The comparison between the aforementioned drive systems is based on six aspects.

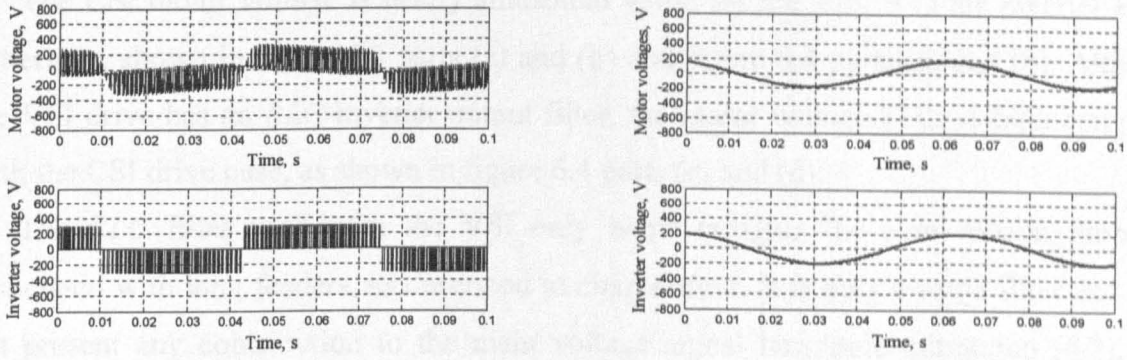
- Motor voltage, motor current, and common mode voltage
- Inverter topology and utilization factor
- Feeder insulation requirements and length capabilities
- AC side input power factor and supply input current
- Filter requirements and losses
- System efficiency

6.3.1 Motor voltage, current, and common mode voltage

This phase addresses issues related to the power quality of motor voltages, currents, and common mode voltage when controlled by a VSI/CSI indirect vector controlled drive. The analysis investigates the steady-state waveforms when operating at a 300 rpm motor speed, 15 Hz, no-load, with a 1 km feeder length.

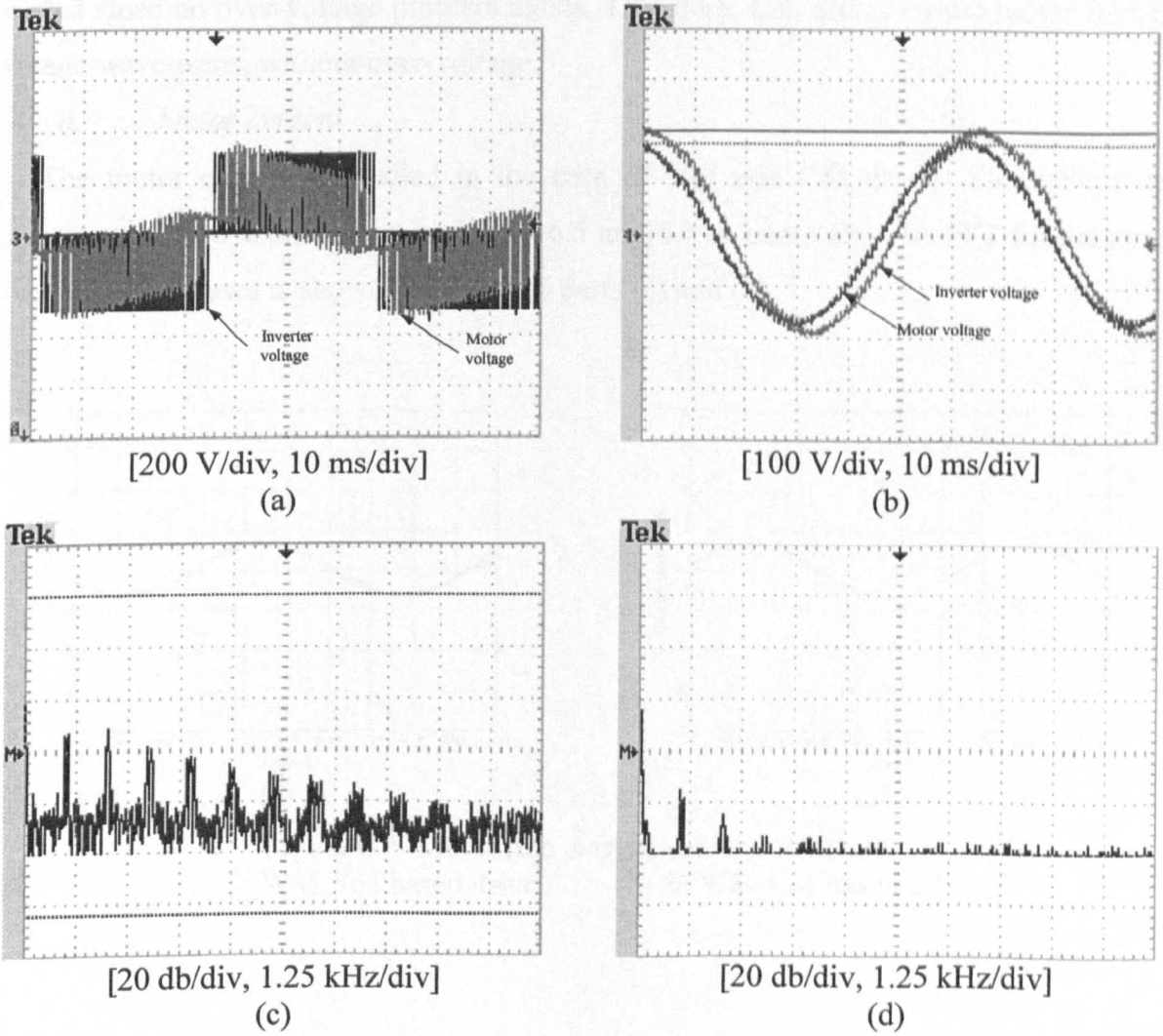
i. Motor voltage

The motor voltage is recorded in both cases. Simulations and experimental results are shown in figures 6.3 and 6.4 respectively. Inverter and motor voltages for the VSI drive are illustrated by simulation and experimental results in part (a) of figures 6.3 and 6.4 respectively. The equivalent CSI drive waveforms are illustrated by simulation and experimental results in part (b) of figures 6.3 and 6.4 respectively. The motor voltage FFT for each case is shown in figure 6.4 parts (c) and (d).



(a) (b)

Figure 6.3: Motor and inverter line voltage simulation results.
a: SPWM VSI based drive b: SPWM CSI based drive



[200 V/div, 10 ms/div] [100 V/div, 10 ms/div]
(a) (b)

[20 db/div, 1.25 kHz/div] [20 db/div, 1.25 kHz/div]
(c) (d)

Figure 6.4: Motor and inverter line voltage experimental results
a and c: SPWM VSI based drive b and d: SPWM CSI based drive
(a) and (b) motor and inverter line voltage, and (c) and (d) motor line voltage FFT.

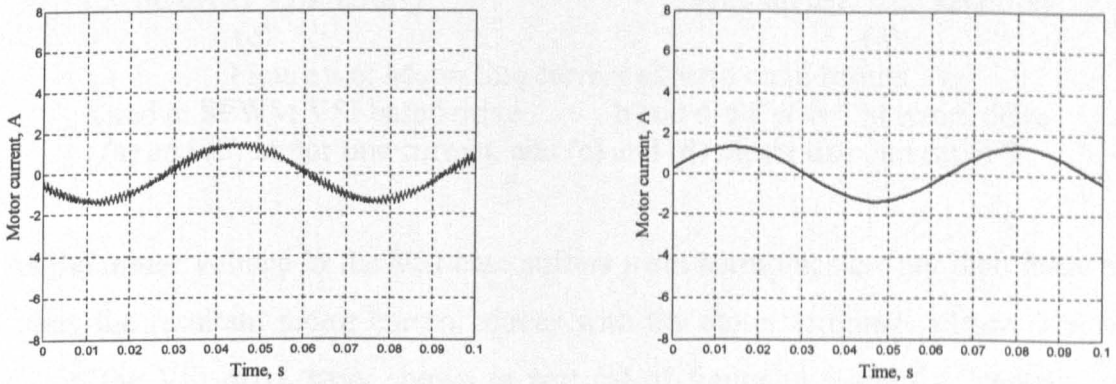
The CSI motor voltage is nearly sinusoidal while for the VSI, it is the inverter PWM pattern, as shown in figure 6.3 parts (a) and (b) and figure 6.4 parts (a) and (b). Although the VSI drive has an *RLC* inverter output filter, the motor voltage THD is high compared with the CSI drive case, as shown in figure 6.4 parts (c) and (d).

The *RLC* filter used with the VSI only helps mitigate the over-voltage problems associated with long feeders, as described in chapter four. It is only a surge filter and does not present any contribution to the main voltage signal harmonic mitigation [6.2]. The capacitor bank shunt connected to the CSI output acts as a harmonic filter to the inverter output voltage, making the voltage waveform near sinusoidal [6.3].

In the CSI case, because of the near sinusoidal output voltages, no surge filters are needed since no over-voltage problem exists. Therefore, CSI drives ensure motor friendly voltage waveforms, without over-voltage.

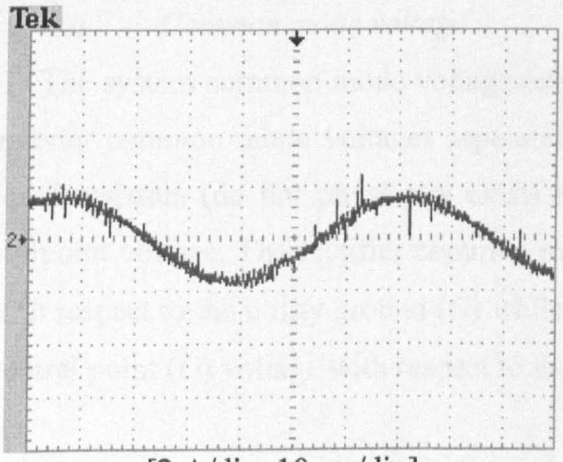
ii. Motor current

The motor current is studied in the case of VSI and CSI drives. Simulations and experimental results are shown in figures 6.5 and 6.6 respectively. The FFT for the motor current in both cases is shown in figure 6.6 parts (c) and (d).

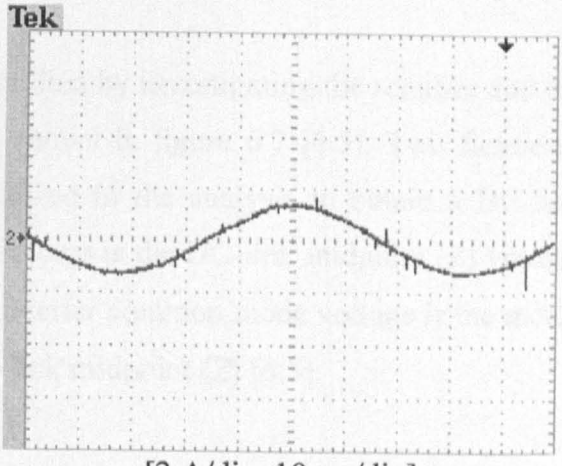


(a) (b)

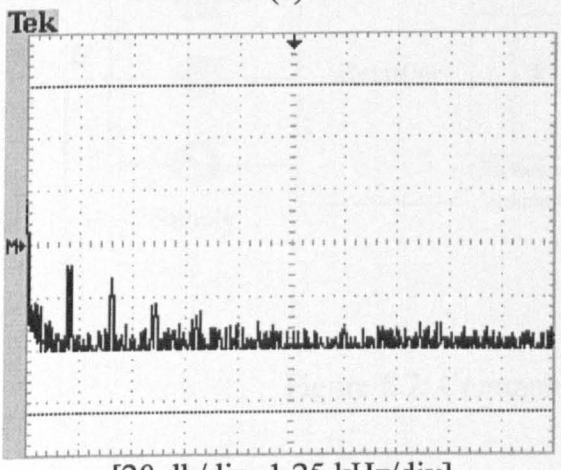
Figure 6.5: Motor line current simulation results.
a: SPWM VSI based drive b: SPWM CSI based drive



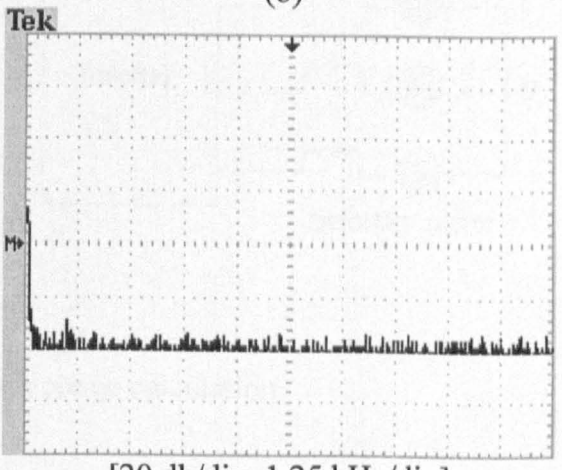
[2 A/div, 10 ms/div]
(a)



[2 A/div, 10 ms/div]
(b)



[20 db/div, 1.25 kHz/div]
(c)



[20 db/div, 1.25 kHz/div]
(d)

Figure 6.6: Motor line current experimental results
a and c: SPWM VSI based drive b and d: SPWM CSI based drive
(a) and (b) motor line current, and (c) and (d) motor line current FFT.

As the motor voltage in the VSI case suffers from harmonics greater than those of the CSI case, the resultant motor current agrees with the motor terminal voltage. The motor current in the VSI drive case, shown in part (a) of figures 6.5 and 6.6, contains larger harmonic magnitude than in the CSI drive case, as shown in part (b) of figures 6.5 and 6.6.

The motor inductance creates a current filter effect which appears clearly in the VSI drive. The motor current is sinusoidal, with higher order harmonics, although the motor voltage has a chopped PWM waveform.

In the CSI case, as a result of the near sinusoidal inverter output voltage and the motor current filter effect, the motor current harmonics are minimal as, shown in figure 6.6(d). Therefore the CSI drive provides near harmonic free motor current [6.3], [6.4].

iii. Common mode voltage

The system common mode voltage can by studied by investigating the rectifier and the inverter common mode voltages separately, as shown in figure 6.7 [6.5]. Two fictitious, equal resistors (do not physically exist) are utilized in the analysis to obtain a DC-link midpoint voltage. The rectifier common mode voltage is the DC-link midpoint (Z) voltage with respect to the utility ground (G) while the inverter common mode voltage is the motor neutral point (O) voltage with respect to the DC-link midpoint (Z) [6.5].

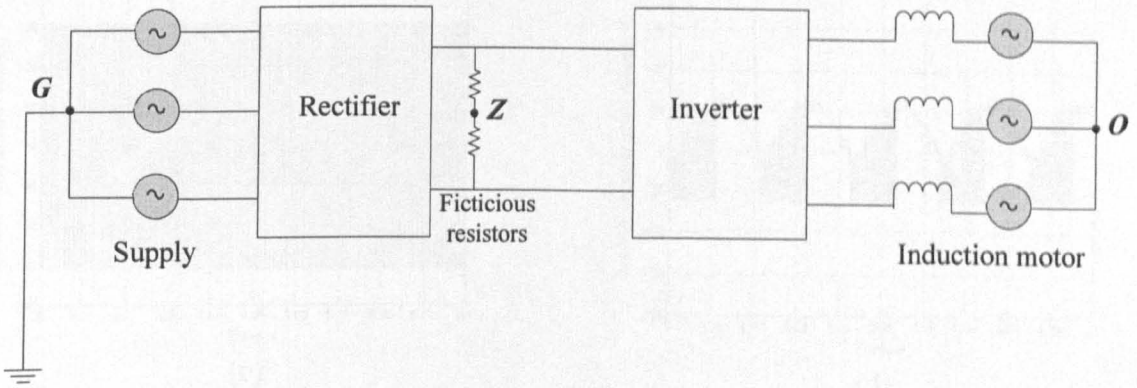


Figure 6.7: Common mode voltage calculation.

Simulation and experimental results for the system common mode voltages (rectifier common mode voltage (V_{ZG}) and inverter common mode voltage (V_{OZ})) of the VSI drive system are shown in parts (a) and (c) of figures 6.8 and 6.9 while those for the CSI drive system are shown in parts (b) and (d) in figures 6.8 and 6.9.

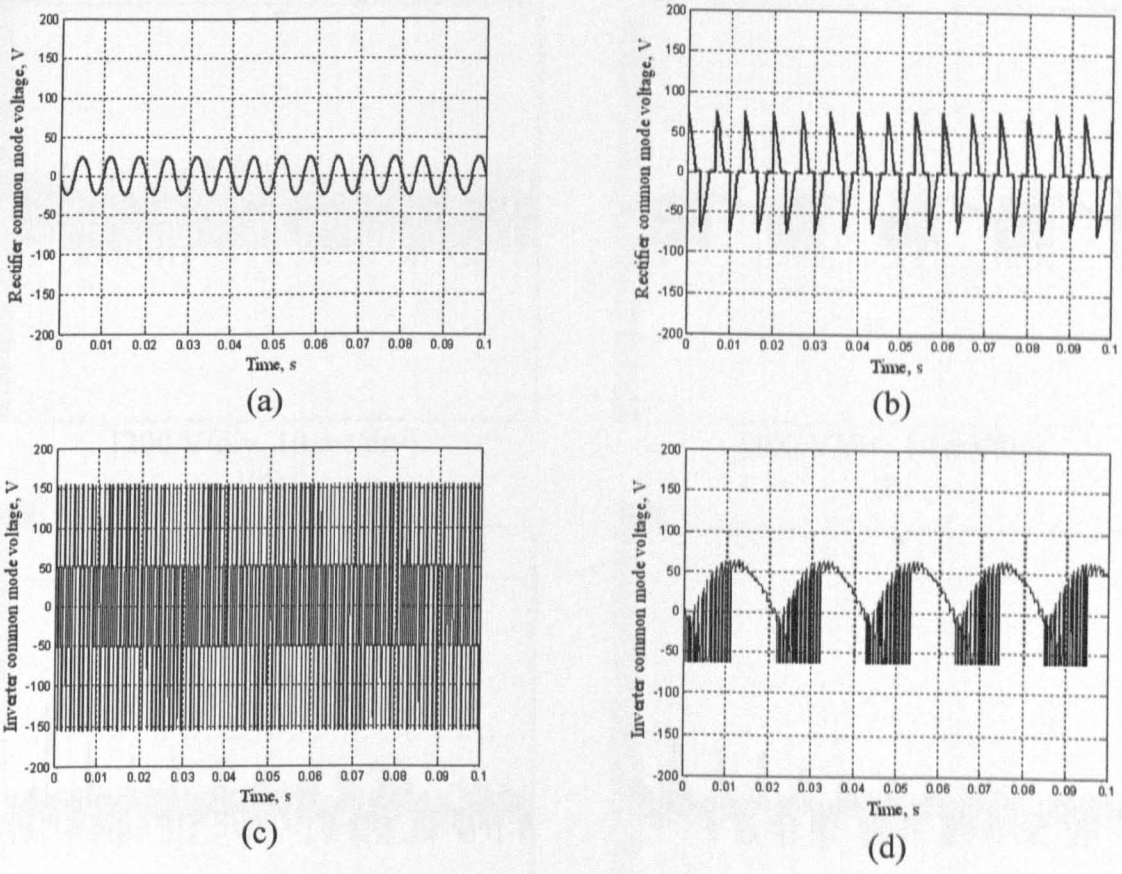
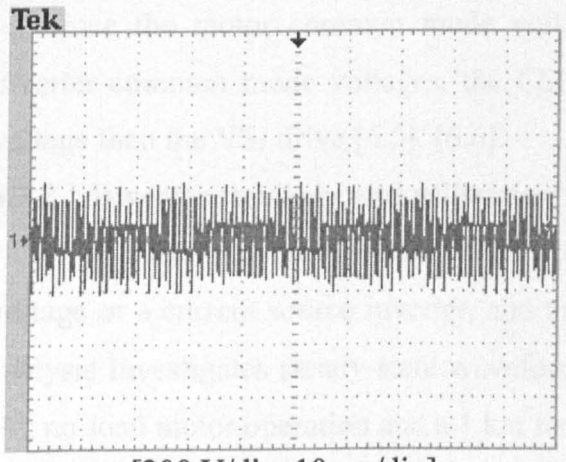
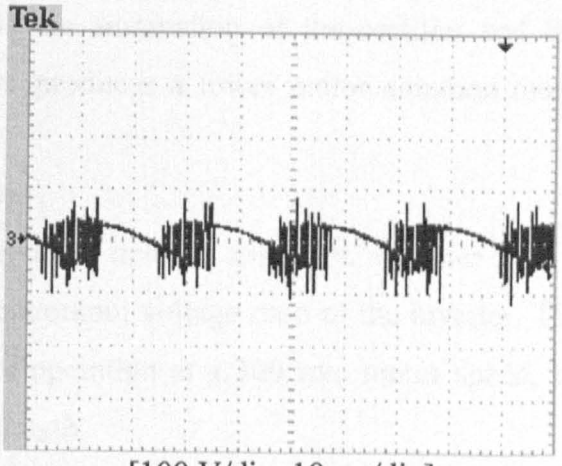


Figure 6.8: Common mode voltage simulation results.
a: SPWM VSI based drive b: SPWM CSI based drive

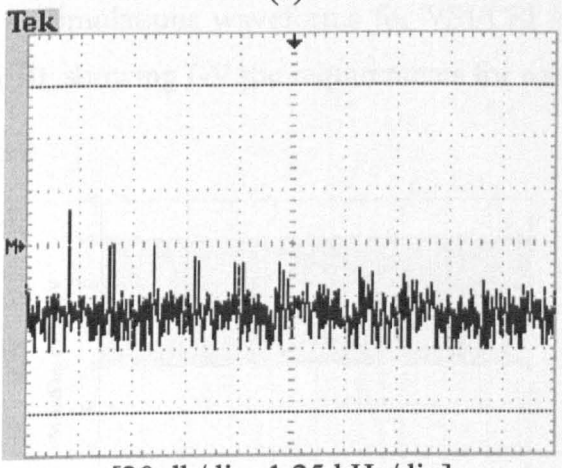
On the rectifier side, the common mode voltage in the CSI drive is greater than that for the VSI drive case. For the VSI drive, the rectifier stage is a three-phase diode bridge, where no switching occurs, while in the CSI drive the rectifier side is a three-phase SCR controller, where the output voltage from the rectifier varies with the rectifier firing angle. On the inverter side, the common mode voltage for the CSI is less than that of the VSI as the motor voltage is near sinusoidal in the CSI case due to the capacitor bank filter. The rectifier common mode voltage (V_{ZG}) in both cases is characterised by less switching action than the inverter common mode voltage (V_{OZ}).



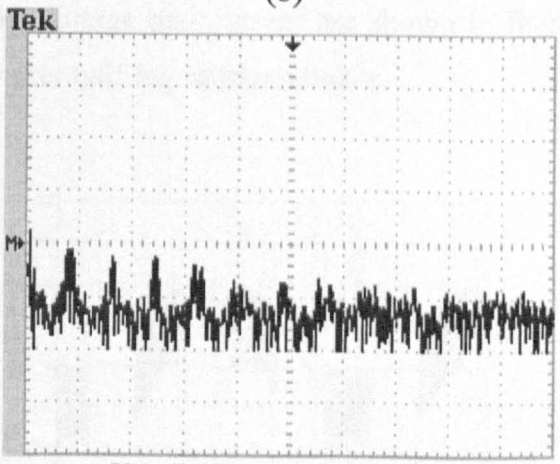
[200 V/div, 10 ms/div]
(a)



[100 V/div, 10 ms/div]
(b)



[20 db/div, 1.25 kHz/div]
(c)



[20 db/div, 1.25 kHz/div]
(d)

Figure 6.9: Inverter common mode voltage experimental results
a and c: SPWM VSI based drive b and d: SPWM CSI based drive
(a) and (b) common mode voltage, and (c) and (d) common mode voltage FFT.

The experimental results for the inverter common mode voltage (V_{OZ}) are shown in figure 6.9 parts (a) and (b) which match the simulation results shown in figure 6.8 parts (c) and (d).

The FFT analysis of the inverter common mode voltage (V_{OZ}) for both cases, shown in figure 6.9 parts (c) and (d), show that the common mode voltage in the VSI case is higher in magnitude and rich in high-order frequency components. These results match the common mode voltage pattern shown in figure 6.8 parts (a) and (b) and figure 6.9 parts (a) and (b).

Since the motor common mode voltage is the summation of the rectifier and the inverter common mode voltages, the CSI drive produces a lower motor common mode voltage than the VSI drive [6.5], [6.6].

6.3.2 Inverter topology and utilization factor

This phase addresses issues related to the drive inverter topology, whether it is a voltage or a current source inverter, and the input/output voltage ratio of the inverter. The analysis investigates steady-state waveforms for operation at a 300 rpm motor speed, 15 Hz, no-load motor operation and a 1 km feeder length.

i. Inverter topology

Simulations waveforms for VSI/CSI half leg voltage and current are shown in figure 6.10, showing I-V the requirements for each inverter half leg semiconductor.

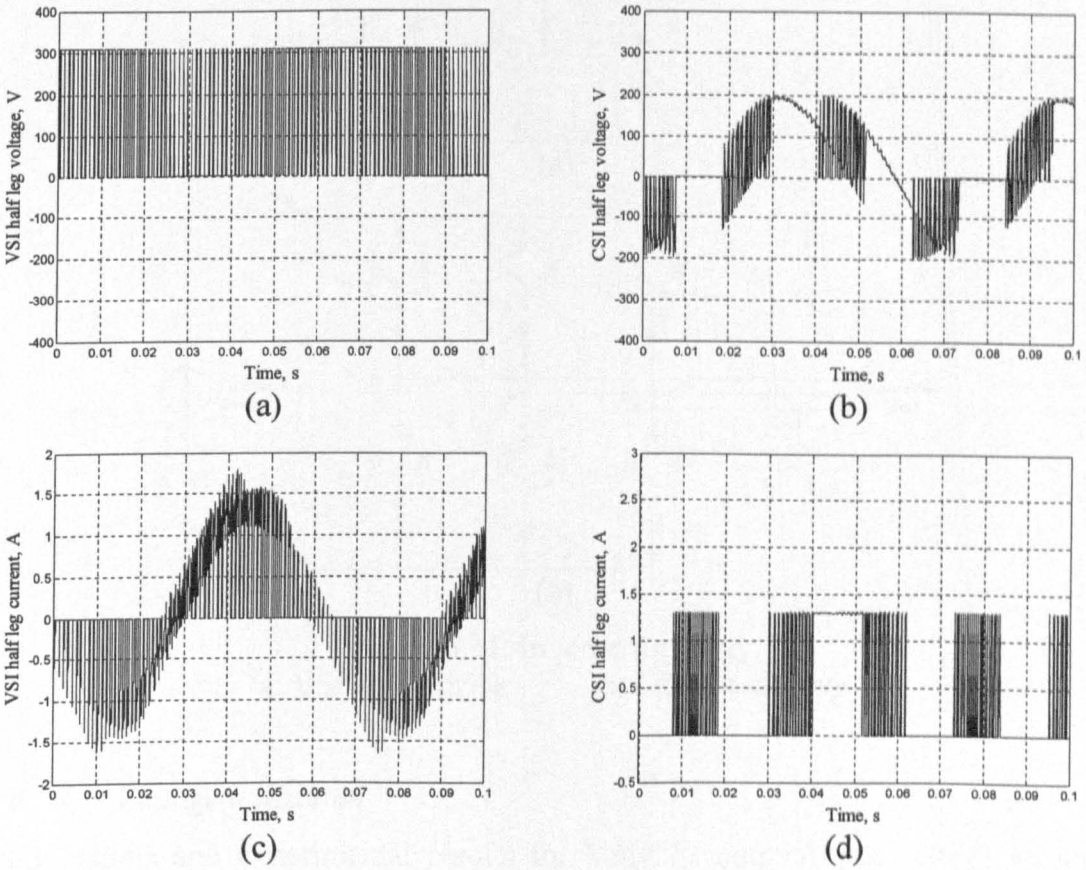


Figure 6.10: Inverter half leg voltage and current simulation results.
a and c: SPWM VSI based drive b and d: SPWM CSI based drive

The VSI voltage per half leg is unidirectional, as shown in figure 6.10(a), while the current is bidirectional as shown in figure 6.10(c). The IGBT can only withstand

unidirectional voltage and current, hence an anti-parallel diode is used to create a path for the negative (reverse) current in VSI. On the other hand, the CSI half leg semiconductor must withstand reverse voltages, as shown in figure 6.10(b). Hence, it must have a series fast recovery diode to withstand the reverse voltage in the CSI case when an IGBT is used. Consequently, the number of semiconductors in the CSI is more than that in the VSI due to the series connected fast recovery diodes as shown in figure 6.11. Therefore, the CSI topology is considered to be more complex than that of VSI, when using IGBTs.

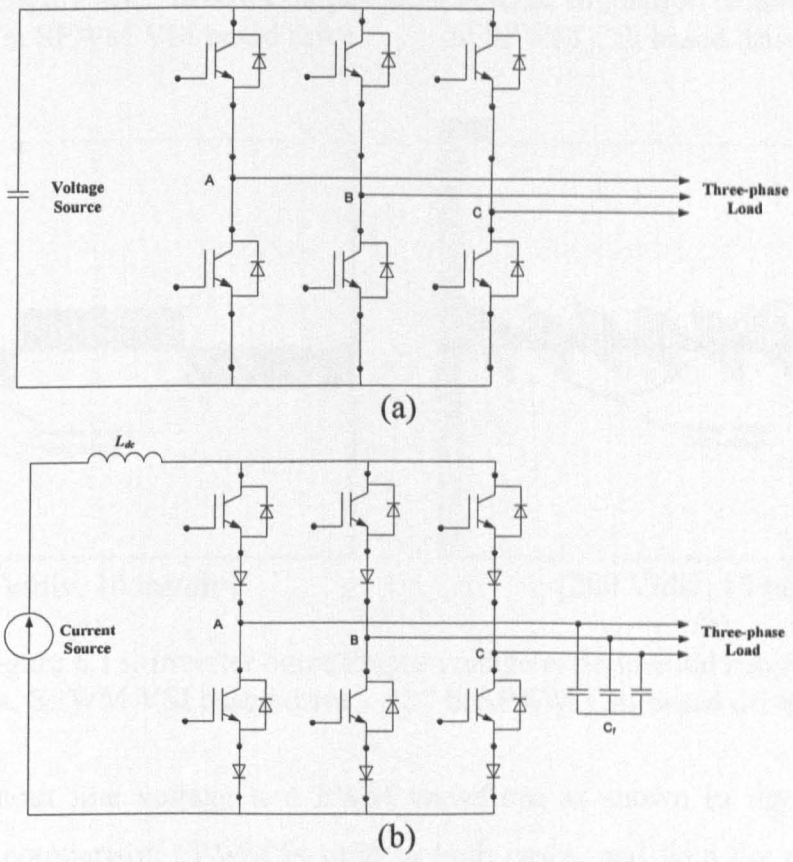
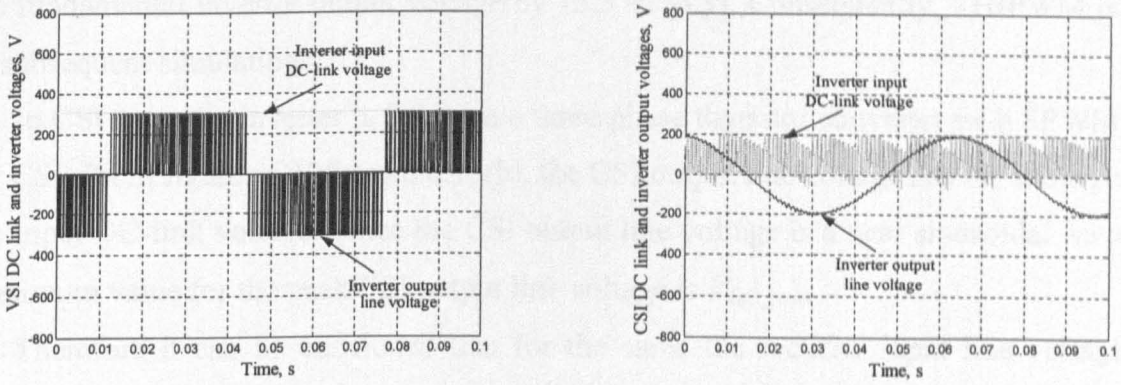


Figure 6.11: Inverter topology.
a: VSI based drive b: CSI based drive

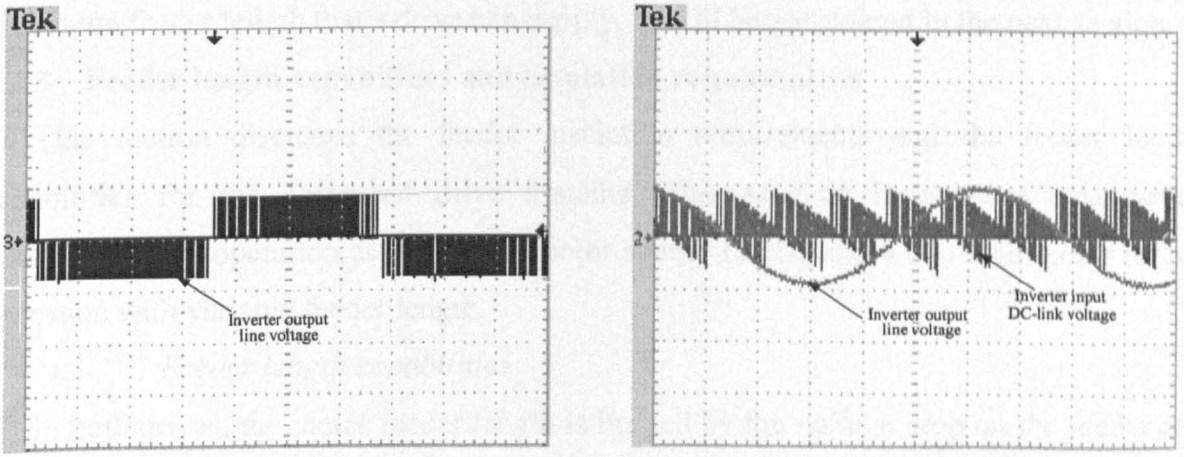
ii. Voltage utilization

Simulations and experimental results for VSI/CSI output/input voltage waveforms, hence voltage ratio, are shown in figures 6.12 and 6.13 respectively.



(a) (b)

Figure 6.12: Inverter output/input voltage simulation results.
a: SPWM VSI based drive b: SPWM CSI based drive



[400 V/div, 10 ms/div] [200 V/div, 10 ms/div]

(a) (b)

Figure 6.13: Inverter output/input voltage experimental results.
a: SPWM VSI based drive b: SPWM CSI based drive

The VSI output line voltage is a PWM waveform as shown in figures 6.12(a) and 6.13(a). In this comparison SPWM is used in both cases, and then the peak output line voltage (fundamental component) is a function of the inverter modulation index and DC-link voltage [6.3], which can be calculated as:

$$v_{inv\_abc\_peak} = \sqrt{2}(0.612 m_{abc\_peak} V_{DC}) \tag{6.1}$$

Therefore, the inverter output line voltage linearly increases with modulation index and the maximum value for the peak output fundamental line voltage in the VSI case, when SPWM is used, is $0.86V_{DC}$ which highlights the need to use THIPWM in order to increase

the fundamental inverter output voltage by 15.5 % [6.3]. Consequently, THIPWM is used in subsequent simulations.

In CSI case, the inverter is fed from a three-phase thyristor converter with SPWM used for CSI. From figures 6.12(b) and 6.13(b), the CSI output line voltage has the same peak as the input DC-link voltage. Since the CSI output line voltage is a near sinusoidal wave, the maximum value for the peak CSI output line voltage is V_{DC_peak}

Therefore it can be concluded that for the same the rectifier input line voltage, the maximum for inverter output line voltage, in CSI case, is higher than that obtained in VSI case when using the same PWM technique. Hence, the CSI voltage utilization is better than that of the VSI. The inverter voltage utilization is an important tool since it determines the maximum feeder length that a drive can supply, as will be considered in the next section.

6.3.3 Feeder length capabilities and insulation requirements

This section discusses the feeder insulation requirements and the feeder length capabilities for the compared drive systems. This analysis investigates steady-state performance for operation at a 300 rpm motor speed, 15 Hz, and 4 Nm load motor torque operation with variable feeder length.

i. Feeder length capabilities

In both drives, the motor feeder length is limited by the voltage drop on the feeder and the voltage capabilities of the inverter. The question is: For the same supply input line voltage, motor, and load, which drive can sustain a longer feeder length?

The two vector controlled drive systems (VSI/CSI based) are examined with the same motor loading conditions for different feeder lengths starting from a short feeder (0.2 km), to investigate the maximum feeder capabilities for each system. The variation of the motor voltage, inverter voltage and inverter input DC-link voltage for both drive systems are shown in figure 6.14 parts (a) and (b) respectively. The CSR firing angle decreases and VSI modulation index increases with the feeder length, as shown in figure 6.14 parts (c) and (d) respectively. For both cases, the vector controller attempt to fix the motor voltage (to hold its reference speed command and fulfil load demand), for all the feeder lengths. In figure 6.14 parts (a) and (b) the motor voltage is almost constant with the feeder length increase for both inverter topologies. But for the VSI, the input DC-link voltage is constant. Hence to attain the fixed motor voltage while the feeder increases, the VSI modulation index increases in order to increase the inverter output voltage (as shown in

figure 6.14 (c)) to overcome the feeder voltage drop up to 1.4 km. At this length, the modulation index saturates and over-modulation, causing harmonic generation, is to be avoided. Hence, the feeder length could not be further increased using SPWM. Therefore, THIPWM is used in the VSI case to increase the fundamental inverter output voltage in order to acquire longer feeder length capability. Since THIPWM increases the fundamental inverter output voltage by only 15.5 %, only 0.4 km more feeder length is gained. So, even with THIPWM, the maximum feeder length reached using the VSI drive is 1.8 km. THIPWM is used in all subsequent simulations for the VSI drive when the feeder length exceeds 1.4 km. It can be shown from figure 6.14 parts (a) and (c) that the same output inverter voltage is achieved in both cases at the same feeder length but for lower modulation index in THIPWM than SPWM. After 1.8 km feeder length, the modulation index saturates in the THIPWM VSI case.

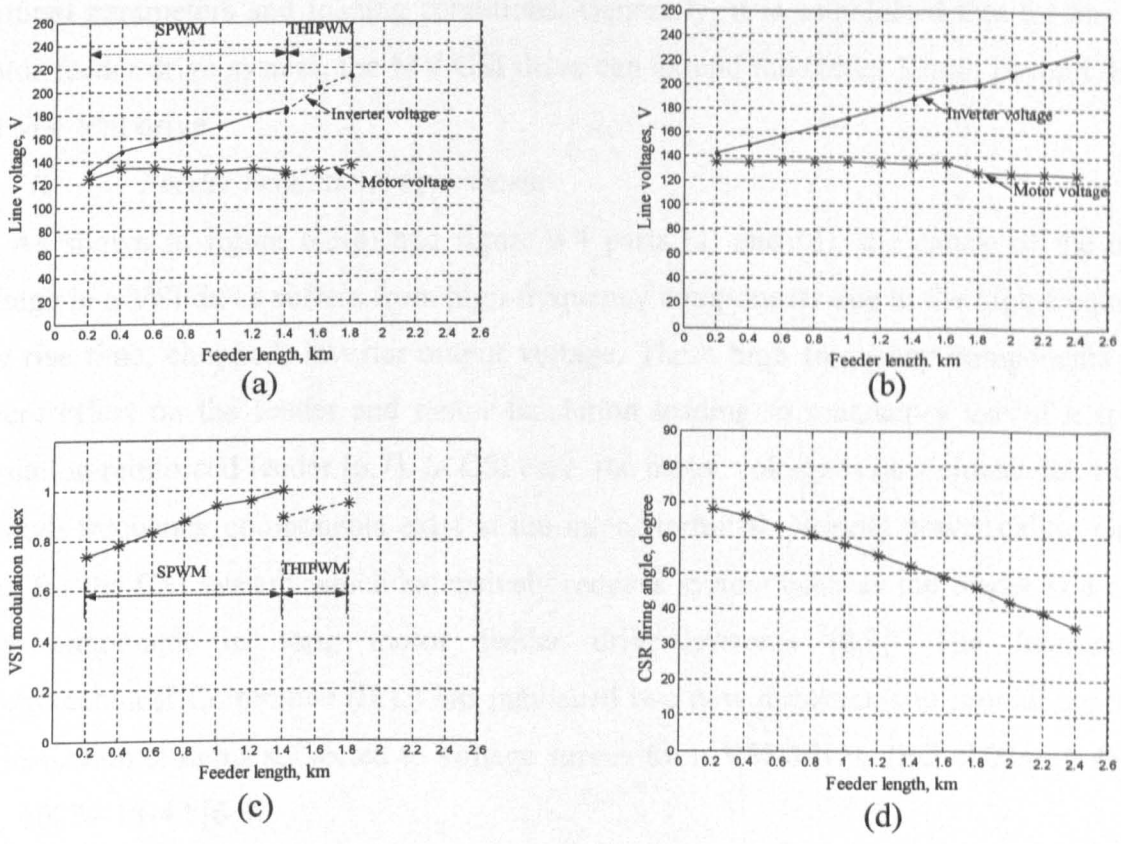


Figure 6.14: Variation of DC-link, inverter and motor line voltages with feeder length simulation results

a and c: VSI based drive b and d: CSI based drive

(a) and (b) DC-link, inverter output and motor line voltages, and (c) VSI modulation index and, (d) CSI rectifier side firing angle.

Note that the inverter output voltage is the output voltage from VSI including any filter (equals to the voltage input to the feeder).

But in the CSI case, the inverter input DC-link voltage increases by decreasing the CSR firing angle, as shown in figure 6.14(d). Hence, due to higher voltage utilization than VSI, the feeder length can be extended up to 2.4 km. At this length, the CSR firing angle reaches 30° and since the rectifier output voltage is directly proportional to a cosine the firing angle, a further feeder length increase can not be compensated by the rectifier as the voltage gain from *cos(30)* to *cos(0)* is small, less than 14 %. The utilization factor of the CSI is higher than that of the VSI as shown in the previous section. Therefore, for the same supply input voltage, motor and load, the CSI drive can extend the motor feeder beyond that of the VSI drive. The feeder extension is a function of feeder parameters, motor load, and supply input voltage. The given results and feeder lengths can only act as a guide to prove the theory. For a different case study, the previous steps should be repeated with the required parameters and loading conditions. Generally, it is established that for any long motor feeder drive system, the MV CSI drive can extend the feeder length beyond that of the MV VSI drive.

ii. Feeder insulation requirement

As shown in figure 6.3(a) and figure 6.4 parts (a) and (d), the nature of the motor voltage in a VSI drive suffers from high-frequency components due to the high-frequency, low rise time, chopped, inverter output voltage. These high frequency components have severe effect on the feeder and motor insulation leading to mandatory use of a special insulation reinforced feeder [6.7]. In CSI case, the motor voltage is near sinusoidal. Hence, no high frequency components exist at the motor terminal. Normal power cables can be used for the CSI system which extensively reduces system cost, as the feeder is a major cost component in long motor feeder drive systems [6.3]. The International Electrotechnical Committee (IEC) has published two new documents to provide guidance on insulation systems subjected to voltage surges from VSI drives, IEC 60034-18-41 and IEC 60034-18-42 [6.8].

6.3.4 AC side input power factor and supply input current

This section investigates the rectifier AC side input power factor and input current for both drive systems. The analysis investigates steady-state waveforms for the same operating conditions with a variable feeder length.

i. AC side input power factor

Although both drive systems supply an identical motor under similar loading conditions and the same feeder length, the rectifier side topology differences lead to supply input power factor differences, as shown in figure 6.15

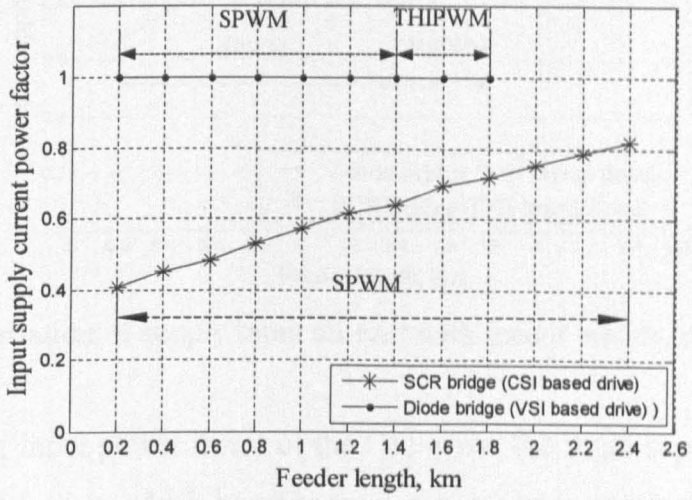


Figure 6.15: Variation of supply input power factor with feeder length, simulation results.

Since in the VSI drive, the input stage is three-phase diode-bridge (uncontrolled rectifier), the input supply power factor is constant and near unity. In the CSI drive, the input stage must be phase controlled. The simplest configuration is a three-phase six-pulse SCR-bridge, controlled rectifier, which is characterized by poor power factor at low loading conditions. This is a major disadvantage of this topology [6.3], [6.4].

ii. Supply input current

Both systems supply the same load (motor and feeder) and have same input supply line voltage, but with a different input power factor, as shown previously in figure 6.15. The resultant effect on the input supply current is shown in figure 6.16.

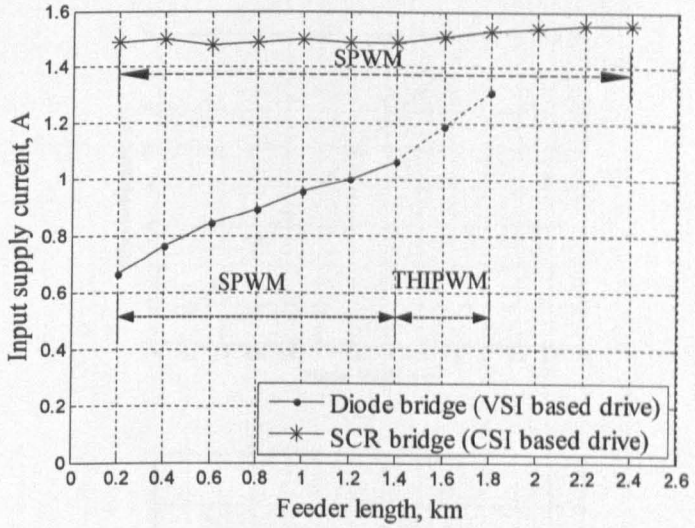


Figure 6.16: Variation of supply input current with feeder length, simulation results.

Due to the poor input power factor of the CSI drive, the input supply current is greater than that for the VSI drive, which benefits from near unity power factor. The input supply current and input power factor results will be used in the following efficiency investigation, section 6.3.6.

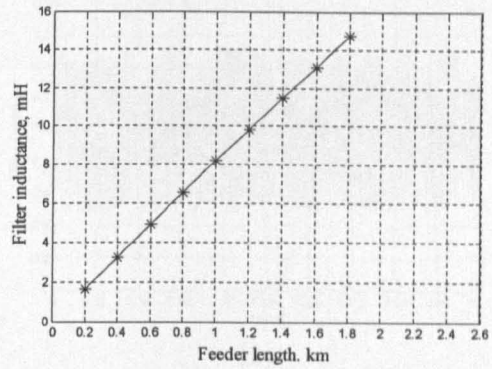
6.3.5 Filter requirements and losses

As previously mentioned, both compared systems are accompanied with filters. This section investigates the filter requirements and losses for the compared drive systems.

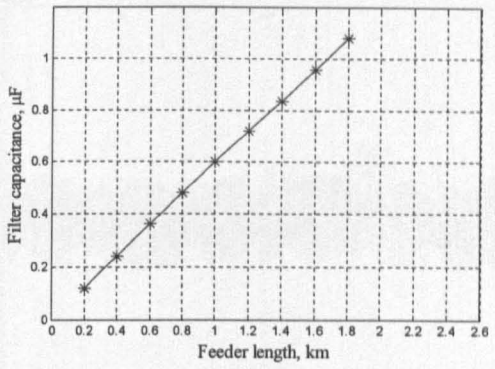
i. Filter requirement

An output line filter network is mandatory for the VSI drive to prevent over-voltage on the motor terminals when using a long motor feeder. The filter parameters are a function of cable length and switching frequency [6.2]. From the inverter output *RLC* filter discussion in chapter four, the filter component values, for varying feeder length, are shown in figure 6.17. The filter resistance is constant for all lengths, as the feeder type is constant. Filter resistance equals the characteristic impedance of the feeder, which does not depend on the feeder length, and is 234.5 Ω in the studied case.

For the CSI drive system, the filter capacitance, 25 μF in this study, is dependant on the inverter switching frequency and the load [6.3].



(a)



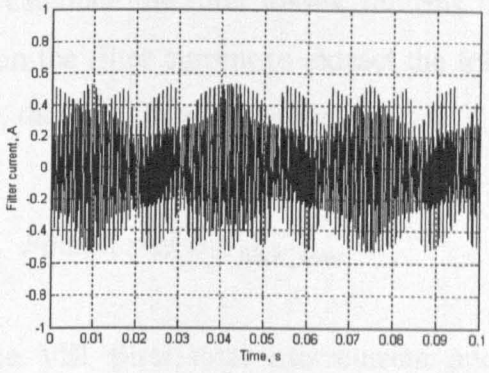
(b)

Figure 6.17: Variation of VSI inverter output *RLC* filter parameters with feeder length. (a) filter inductance and (b) filter capacitance.

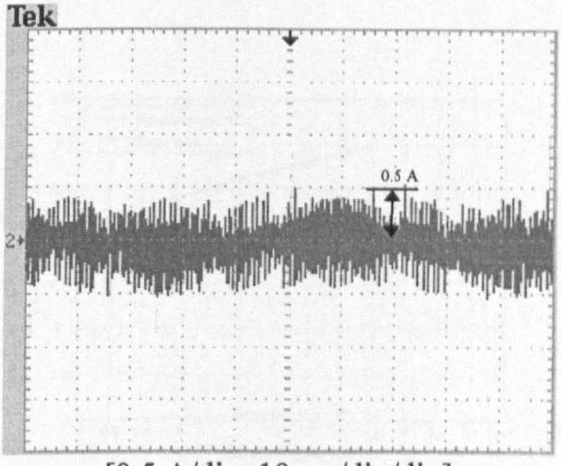
ii. Filter losses

Since the CSI filter is a three-phase capacitor bank, it is considered lossless. This is an advantage of the CSI drive. Also, the filter component values are fixed, 25 µF, for the tested feeder length variations.

As the feeder length increases, the inverter output voltage increases, creating more losses in the VSI filter resistance. This filter is not tuned to a specific frequency and the filter current has a relatively small fundamental component compared to the higher order harmonics, as shown in figure 6.18. Consequently, the filter loss calculation must consider the effect of the higher order current harmonics.

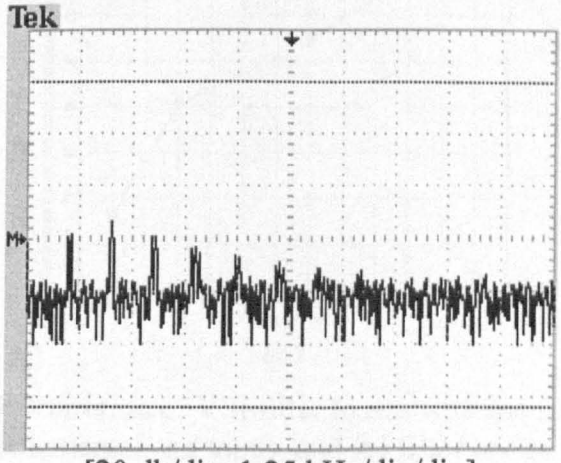


(a)



[0.5 A/div, 10 ms/div/div]

(b)



[20 db/div, 1.25 kHz/div/div]

(c)

Figure 6.18: SPWM VSI filter current
(a) simulation results, (b) experimental results, and (c) experimental results FFT.

Therefore, in order to calculate the filter losses, the rms filter current is calculated by performing FFT analysis on the filter current to extract the total rms current (fundamental plus harmonics rms value), then the filter losses are

$$Filter\,losses = \left|I_{filter\_total}\right|^2 R_f \tag{6.4}$$

Figure 6.19 shows the VSI filter total rms current and the accurate filter losses variation with feeder length.

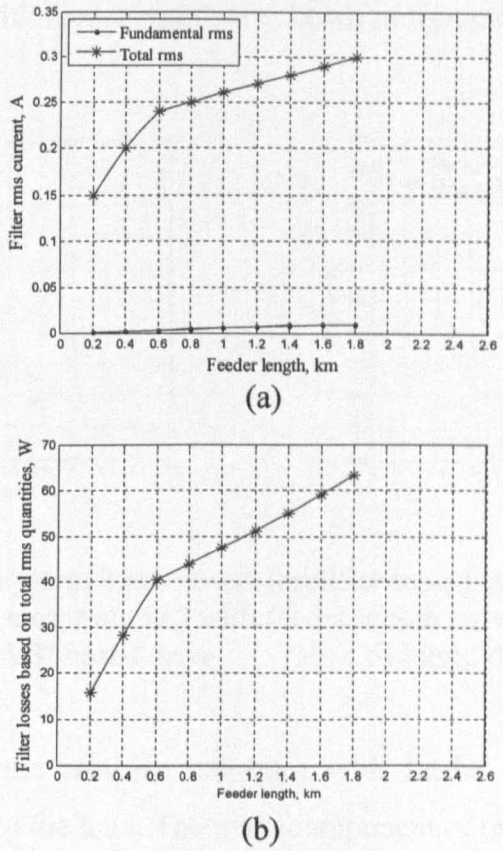


Figure 6.19: Variation of VSI filter losses with the feeder length
(a) filter rms currents (fundamental and total) and (b) filter losses based on total rms value.

Using the total rms filter current gives a more accurate and higher loss than only using the filter fundamental rms value. Although using total rms current in the losses calculation is more complex, it better reflects the total power losses in the filter resistance, as losses are mainly due to higher order harmonic components.

6.3.6 System efficiency

The efficiencies of the two drive systems are investigated under the same operating conditions, and a 220 V supply input and a variable feeder length. The overall system efficiency is

$$\eta_{overall}(\%) = \frac{T_{load}(\frac{2\pi N_r}{60})}{\sqrt{3}|V_s||I_s|pf} \times 100 \tag{6.5}$$

The system input power (rectifier input), and the system output power (mechanical motor output) variation with feeder length are shown in figure 6.20.

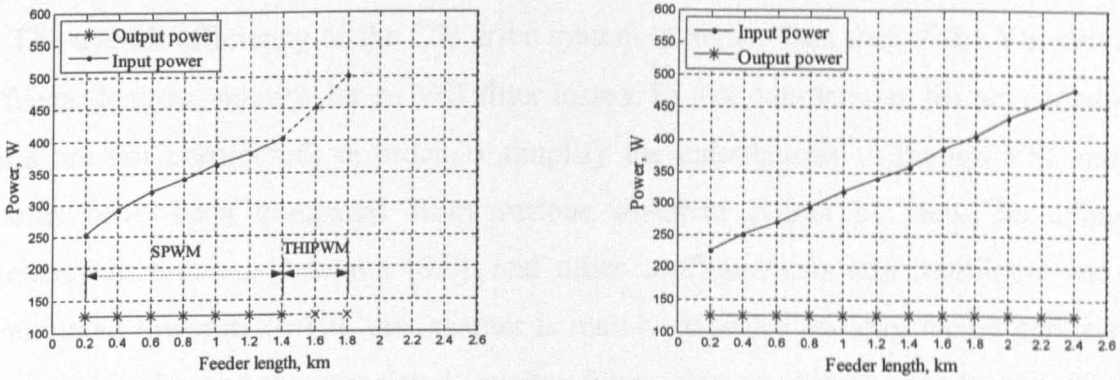


Figure 6.20: Variation of system input power (rectifier input), and the system output power (mechanical motor output) with feeder length simulation results.
a: VSI based drive b: CSI based drive

The input power to the rectifier increases with feeder length increase, to ensure constant power delivered to the load. The main component of the input power increase is to overcome the voltage drop whilst extending the feeder. Although the same motor loading conditions and same feeder parameters are used in both drive system simulations, it can be noticed that the power input for the VSI drive is higher than that for the CSI system. This is mainly due to the additional filter losses which increases the load demand from the input side in VSI case. The CSI drive filter is considered lossless as it comprises only capacitive elements. The addition of filter losses is reflected on the overall efficiency, as shown in figure 6.21.

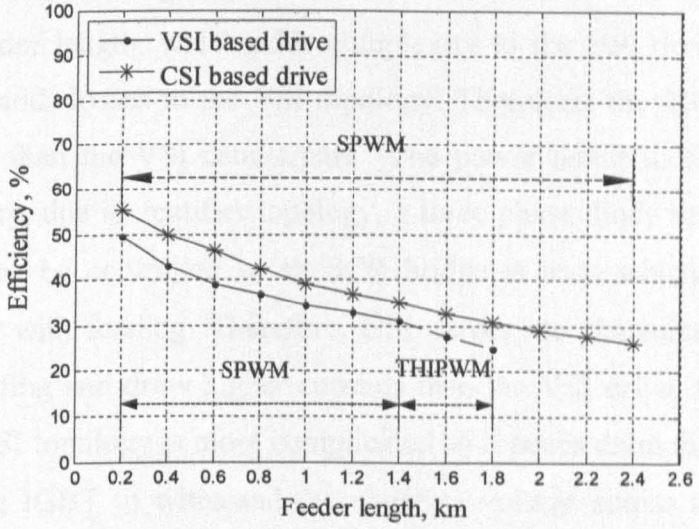


Figure 6.21: Variation of system efficiency with feeder length, simulation results.

The overall efficiency of the CSI drive system is higher than that of the VSI drive, for all feeder lengths, mainly due to VSI filter losses. In this comparison, the semiconductors losses are not considered, in order to simplify the calculations. Although VSI and CSI systems have been compared from various different points of view, including the efficiency in previous research [6.9], and other configurations like multilevel and load commutated inverters [6.10], this chapter is mainly focussed on long feeder applications, where the feeder and the associated inverter filters play important roles in the efficiency calculations.

Discussion

From the simulation and experimental results, the CSI drive delivers better quality voltage waveforms because of its capacitor filter, while the VSI drive output voltage is characterized by high *dv/dt* and fast rise-time voltage waveforms. Therefore, the motor current in the CSI case has lower distortion. Also, the motor common mode voltage in the CSI case is lower. As the voltage utilization of the CSI is better than that of the VSI, even when THIPWM is used in VSI case, the CSI drive can supply a given load to longer feeder lengths. Special insulation for the feeder and the motor are needed in the VSI drive to withstand the high *dv/dt* inverter output voltage waveforms. For CSI case, relatively cheaper common power feeder, available for power network distribution for example, can be used due to the near sinusoidal nature of the inverter output voltage waveform. The CSI main filter is a three-phase capacitor bank at the inverter output terminals. The capacitance

is fixed for the examined range (up to 2.4 km) while for the VSI, the *RLC* filter must be tuned at each feeder length, which adds complexity to the VSI drive system. The filter resistive element adds losses to the VSI topology. Therefore, the CSI drive attains better system efficiency than the VSI counterpart. The power factor in the VSI drive case is constant, near unity, due its rectifier topology, a three phase diode bridge. The rectifier in the CSI drive must be controlled so an SCR bridge is used which has a power factor linearly decreases with loading. Therefore, CSI drives are characterised by poor power factor at light loading and draw higher currents than the VSI drive, for the same loading conditions. The CSI topology is more complicated as it needs extra diode series connected with each half leg IGBT to withstand the negative voltage across the inverter half leg. From the thesis objective, the CSI drive is the better since motor power quality (voltage, current and common mode voltage) and the extended feeder length are the main objective.

Summary

VSI and CSI drives are competitors as MV drives. The decision which is better for long motor feeder applications is difficult to answer unless intensively studied. This chapter presented a detailed comparison of both drive systems with long motor feeders. Various points related to power quality of the motor waveforms (voltage and current) are addressed. Common mode voltage in both cases is studied in detail. Inverter topology, filter needs and filter losses have been considered. Finally, an assessment of efficiency and length capabilities of both systems was performed. It is established by simulation, experimentation, and analyses that CSI drives ensure minimal harmonics in the motor voltage, current and common mode due to the associated capacitive filter. Yet, its hardware is more complex than that of the VSI drive. This may not be the case with MV drives where SGCT can be used The main advantage of using a CSI drive in long motor feeder applications is that its length capabilities is longer than that of the VSI drive.

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CHAPTER SEVEN:

Proposed Sensorless Indirect Vector Controlled PWM CSI Induction Motor Drive with a Long Motor Feeder

The proposed drive system, introduced in chapter five, was shown to be suitable for short feeder lengths, up to a length where a speed sensor, tachometer or shaft encoder could be used. In many industrial applications, such as submersible pumps, conveyers and underground mine fan drives, a long feeder is required which makes a speed-sensor based drive impractical, and a sensorless drive is the only alternative. Most speed estimation techniques require feedback of the motor voltages and currents which is difficult to acquire in long motor feeder applications. Direct motor voltage measurement is to be avoided in long motor feeder drives. This chapter proposes a sensorless drive system with a remote motor voltage calculator suitable for long motor feeder applications. Additionally, a modified stator model, that avoids DC-offset and drift problems during rotor flux estimation, is proposed.

7.1 Speed Estimation using Model Reference Adaptive System (MRAS)

There are many closed loop techniques used for induction motor speed estimation, such as the model reference adaptive system (MRAS) based on: rotor flux [7.1], rotor flux derivative [7.2], [7.3], stator voltages [7.4], modified stator model [7.5], full order observers [7.6], [7.7], reduced order non-linear observers [7.8], [7.9], Kalman filter observers [7.10], [7.11] or sliding mode observers [7.12], [7.13]. Also, there are other techniques for speed estimation which do not rely on voltage/current measurement. Instead, artificial intelligence is used, such as neural networks [7.14], [7.15], harmonic rotor slotting [7.16], [7.17] or high frequency signal injection [7.18], [7.19]. MRAS based on a rotor flux technique is simple, stable and robust against machine parameter variation. This method is selected for use with the proposed modifications. The application of MRAS in speed estimation can be achieved by constructing two models (observers) to estimate the rotor flux *d-q* components in the stationary reference frame. The first observer, reference model, calculates the rotor flux *d-q* components in the stationary reference frame utilizing the motor voltages and currents as inputs. The second observer, adapted/adjusted model, calculates the rotor flux *d-q* components in the stationary reference frame utilizing the

motor current and the estimated speed as inputs. The error from the cross multiplication of the stator and rotor model outputs is used to generate the estimated speed using a *PI*-controller. The estimated speed is used as the adaptation signal for the rotor model.

The system equations are:

- Stator model (reference model) equations

$$\lambda_{dr}^{s} = \frac{L_r}{L_m}\left[\left(\int(v_{m\_ds}^{s} - i_{m\_ds}^{s} R_s)dt\right) - \sigma L_s i_{m\_ds}^{s}\right] \tag{7.1}$$

$$\lambda_{qr}^{s} = \frac{L_r}{L_m}\left[\left(\int(v_{m\_qs}^{s} - i_{m\_qs}^{s} R_s)dt\right) - \sigma L_s i_{m\_qs}^{s}\right] \tag{7.2}$$

- Rotor model (adapted/adjusted model)

$$\lambda_{dr}^{s/} = \int(-\lambda_{dr}^{s/}\frac{R_r}{L_r} - \omega_{r\_est}\lambda_{qr}^{s/} + L_m\frac{R_r}{L_r}i_{m\_ds}^{s})dt \tag{7.3}$$

$$\lambda_{qr}^{s/} = \int(\lambda_{dr}^{s/}\omega_{r\_est} - \lambda_{qr}^{s/}\frac{R_r}{L_r} + L_m\frac{R_r}{L_r}i_{m\_qs}^{s})dt \tag{7.4}$$

- Error generation

$$e_{speed} = \lambda_{qr}^{s}\lambda_{dr}^{s/} - \lambda_{dr}^{s}\lambda_{qr}^{s/} \tag{7.5}$$

- Estimated speed calculation

$$\omega_{r\_est} = (K_{p\_est} + \frac{K_{i\_est}}{s})e_{speed} \tag{7.6}$$

Figure 7.1 shows the block diagram for speed estimation using MRAS where the estimated motor speed N_{r_est} is calculated from the estimated rotor angular frequency ω_{r_est} and the machine number of poles P. The estimated motor speed is used in the vector control closed loop controller as shown in the following sections.

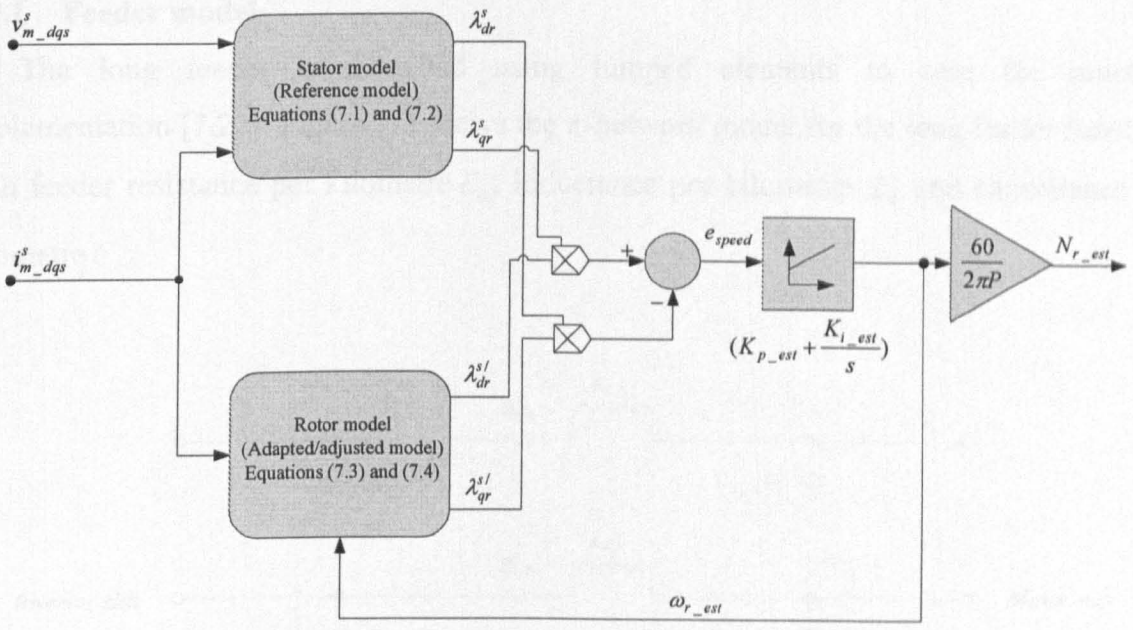


Figure 7.1: Speed estimation using MRAS block diagram.

7.2 Drive System Requirements

The MRAS speed estimator requires motor voltages and currents as inputs. Direct measurement of the motor voltages and currents is impractical for long motor feeder drives due to feeder length or safety/environmental precautions. Hence, the motor voltage and current must be calculated from the inverter end.

Another point should be considered in the practical implementation, DC-shift occurs in the stator model. This offset occurs due to two reasons. First, DC-shift occurs in the motor measurements due to dissimilar temperature coefficients of the measurement transducers in the three-phase motor lines [7.20], [7.21]. Second, flux estimation using open loop integrators, as indicated in (7.1) and (7.2), causes DC-drift due to the uncertainty in the integration initial condition and absence of integration limiters [7.21]. DC-offset problems results in flux estimation error which reflects on the accuracy of the speed estimation. Hence, DC-offset problems should be mitigated to enhance speed estimation accuracy.

7.3 Remote Motor Voltage Calculation

The calculation of the motor terminal voltages from the inverter side requires modelling of the feeder with accurate knowledge of its parameters. Then the motor voltage can be calculated from the inverter end using Kirchhoff's voltage law. In order to calculate the motor voltage from the inverter end, the feeder model is presented.

7.3.1 Feeder model

The long feeder is modelled using lumped elements to ease the practical implementation [7.22]. Figure 7.2 shows the π-network model for the long feeder function, with feeder resistance per kilometre R_c, inductance per kilometre L_c and capacitance per kilometre C_c.

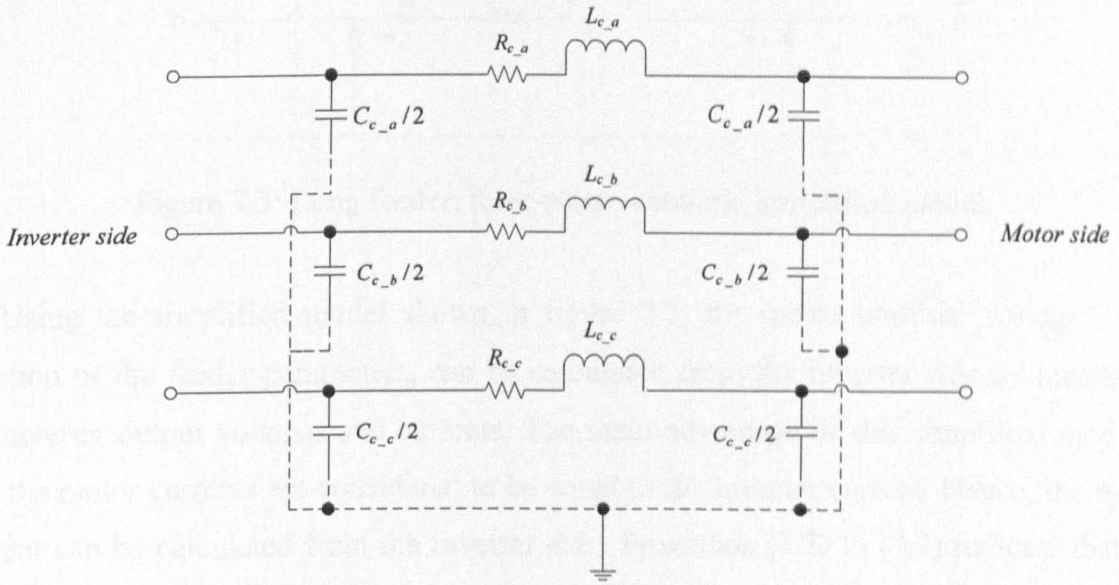


Figure 7.2: Long feeder, three-phase, π-network model.

Since the shunt capacitance reactance is low compared to the feeder resistance and inductance reactance (specially for the selected PWM feeder with low capacitance), the feeder parasitic capacitance can be neglected, making the shunt capacitive impedance at the feeder's ends act as open circuits [7.22]. Hence, neglecting the parasitic capacitance, the feeder model can be simplified to a series *RL* network as shown in figure 7.3. Consequently, the inverter output current is equal to the motor line current, which is required in the speed estimation procedure.

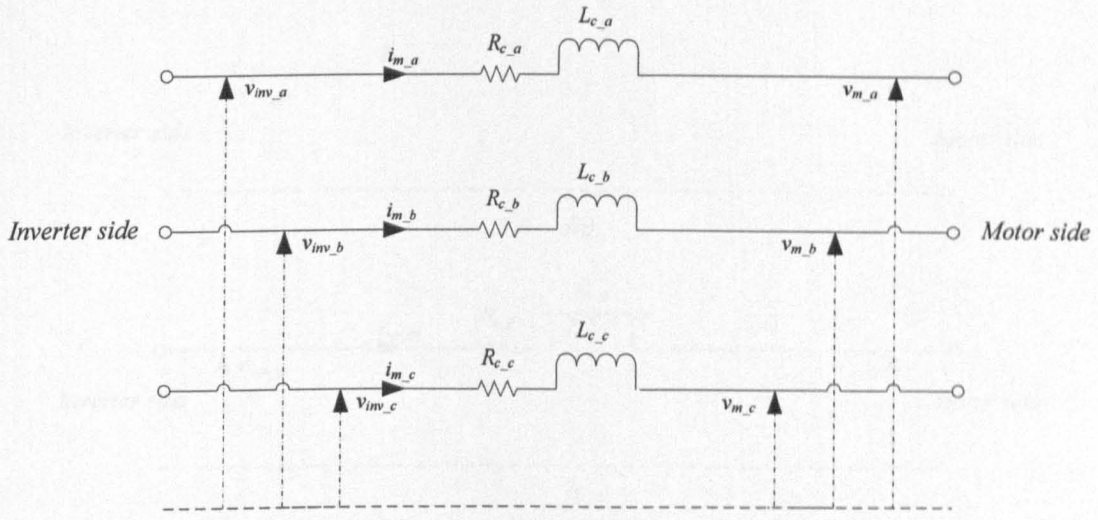


Figure 7.3: Long feeder, three-phase network, simplified model.

Using the simplified model shown in figure 7.3, the motor terminal voltages, as a function of the feeder parameters, can be calculated from the inverter side by measuring the inverter output voltages and currents. The main advantage of this simplified model is that the motor currents are considered to be equal to the inverter current. Hence, the motor current can be calculated from the inverter side. Equations (7.7) to (7.9) indicate that the motor voltage can be calculated from the inverter side but with the penalty of calculating the feeder voltage drop using the derivative process on the feeder current. The calculation of these derivatives creates several practical problems.

$$v_{m\_a} = v_{inv\_a} - i_{m\_a}R_{c\_a} - L_{c\_a}\frac{d}{dt}i_{m\_a} \tag{7.7}$$

$$v_{m\_b} = v_{inv\_b} - i_{m\_b}R_{c\_b} - L_{c\_b}\frac{d}{dt}i_{m\_b} \tag{7.8}$$

$$v_{m\_c} = v_{inv\_c} - i_{m\_c}R_{c\_c} - L_{c\_c}\frac{d}{dt}i_{m\_c} \tag{7.9}$$

7.3.2 Proposed motor voltage calculator

Practical implementation of the derivatives in (7.7) to (7.9) can be replaced by high-pass filters, but a high-pass filter introduces delay and inaccuracy in the estimation process [7.21]. The feeder model is transformed to the *d-q* stationary reference frame, since it is a balanced three-phase network [7.23], as shown in figure 7.4.

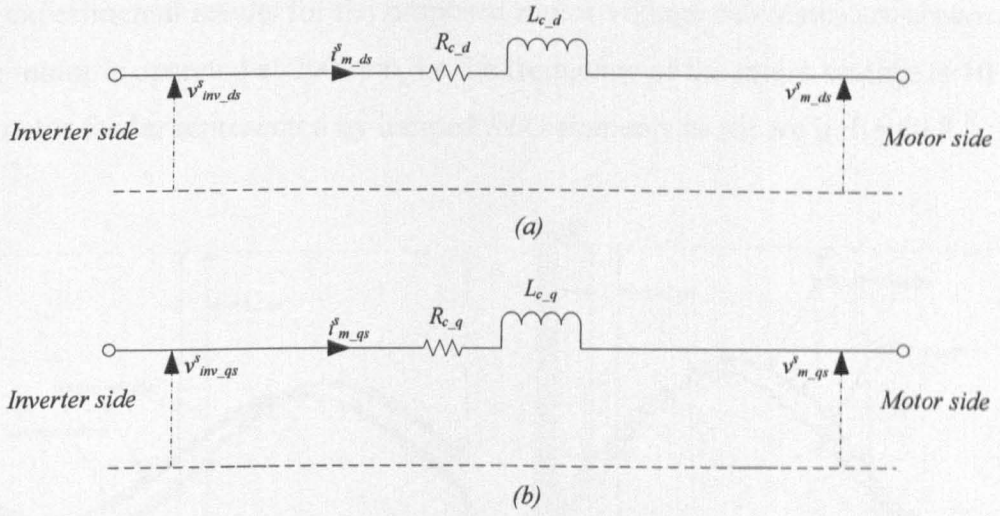


Figure 7.4: Long feeder simplified *d-q* model
(a) *d*-axis network and (b) *q*-axis network.

Due to the capacitor bank at the inverter output, motor voltages and currents are nearly sinusoidal. Consequently, the feeder impedance at the fundamental operating frequency can be represented in matrix form [7.23] that avoids the need to perform derivative to calculate the feeder inductance voltage drop.

$$Z^s_{feeder\_dq} = \begin{bmatrix} R_{c\_d} + \omega_e L_{c\_d} & 0 \\ 0 & R_{c\_q} + \omega_e L_{c\_q} \end{bmatrix} \tag{7.10}$$

The motor voltages in the *d-q* stationary reference frame are calculated from the inverter output voltages and motor currents with linear equations, without the derivative process. The motor voltage equations can be presented in matrix form.

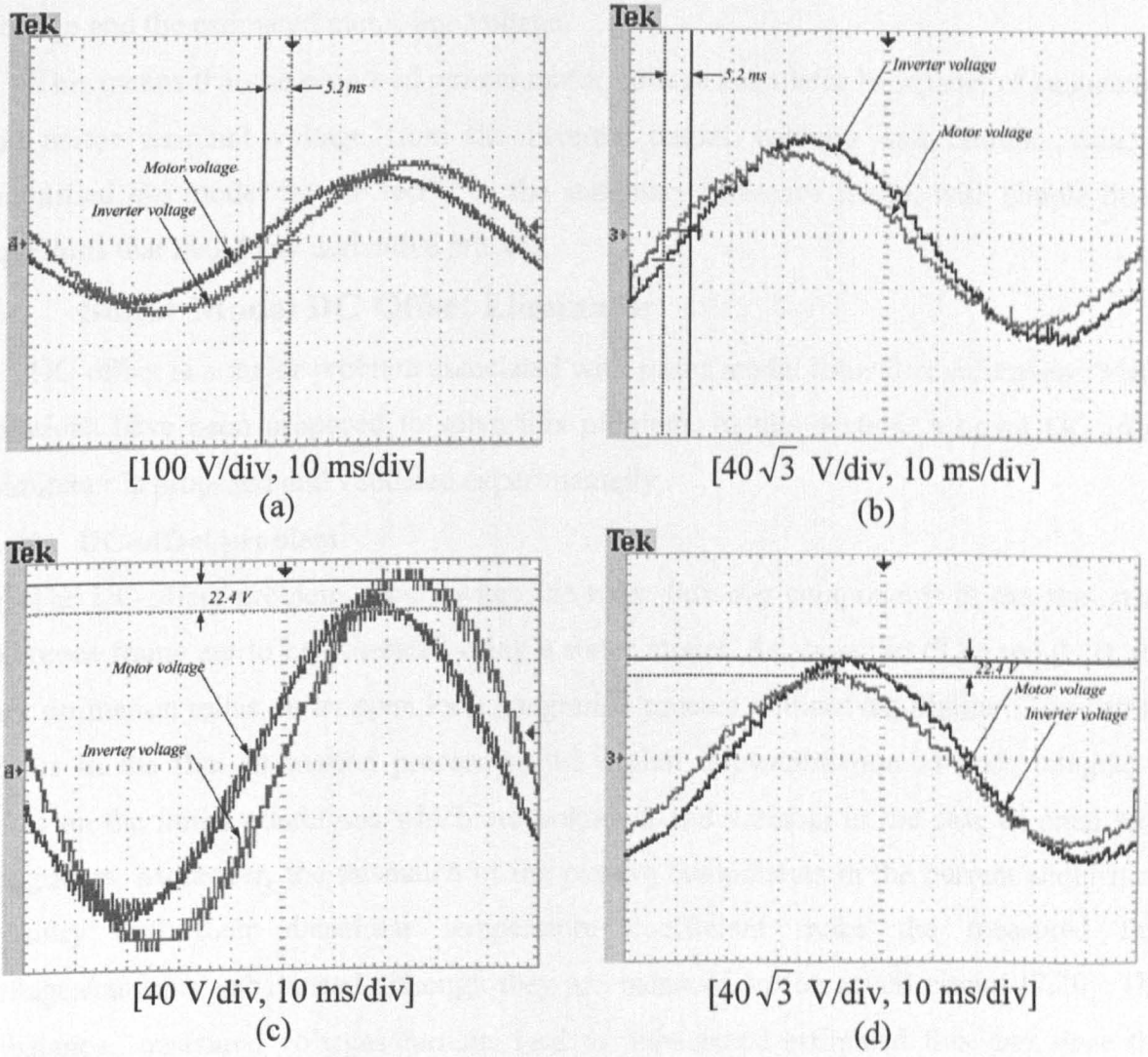
$$V^s_{m\_dqs} = V^s_{inv\_dqs} - Z^s_{feeder\_dq} * I^s_{m\_dqs} \tag{7.11}$$

$$\begin{bmatrix} v^s_{m\_ds} \\ v^s_{m\_qs} \end{bmatrix} = \begin{bmatrix} v^s_{inv\_ds} \\ v^s_{inv\_qs} \end{bmatrix} - \begin{bmatrix} R_{c\_d} + \omega_e L_{c\_d} & 0 \\ 0 & R_{c\_q} + \omega_e L_{c\_q} \end{bmatrix} \begin{bmatrix} i^s_{m\_ds} \\ i^s_{m\_qs} \end{bmatrix} \tag{7.12}$$

where

$$R_{c\_d} = R_{c\_q} = R_{c\_a} = R_{c\_b} = R_{c\_c}$$
$$L_{c\_d} = L_{c\_q} = L_{c\_a} = L_{c\_b} = L_{c\_c}$$

The experimental results for the proposed motor voltage calculator are shown in figure 7.5. The motor is operated at 200 rpm, i.e the frequency of the motor voltage is 10 Hz, with a 1 km motor feeder represented by lumped *RLC* elements as shown in figure 7.2.



[100 V/div, 10 ms/div]
(a)

[40 $\sqrt{3}$ V/div, 10 ms/div]
(b)

[40 V/div, 10 ms/div]
(c)

[40 $\sqrt{3}$ V/div, 10 ms/div]
(d)

Figure 7.5: Motor voltage estimation experimental results
(a) and (c) measured motor and inverter line voltages, (b) and (d) calculated motor voltage and measured inverter voltage.

In figure 7.5 parts (a) and (c), the inverter output line voltage and the motor line voltage are measured with high-voltage differential probes. In figure 7.5 parts (b) and (d), the inverter output line voltage (input to the DSP using voltage transducers) and the motor line voltage (calculated inside the DSP using the proposed calculator) are displayed in their analogue form by means of an external digital to analogue converter.

In figure 7.5(c), it is seen that the difference between the measured motor line voltage and the measured inverter line voltage is 22.4 V. The measured motor line voltage leads the measured inverter line voltage by 5.2 ms at 10 Hz as shown in figure 7.5(a). The same values obtained from figure 7.5 parts (b) and (d), which are the measured inverter line voltage and the estimated motor line voltage.

This means that the proposed remote motor voltage calculator is capable of calculating the motor terminal voltage from the inverter output voltages and currents using a simplified *d-q* model for the feeder in the stationary reference frame, with simple linear equations that avoid any derivative process.

7.4 Stator Model DC-Offset Eliminator

DC-offset is a major problem associated with stator model rotor flux estimation. Many solutions have been proposed to solve this problem. In this section, a novel DC-offset eliminator is proposed and validated experimentally.

7.4.1 DC-offset problem

The DC-offset problem occurs when the rotor flux *d-q* components in the stationary reference frame are to be estimated using a stator model. As shown in (7.1) and (7.2), the flux estimation relies on an open loop integration process without any limiter. Thus offset occurs in the flux estimation process as the digital implementation of such integrators relies on the initial conditions which are unknown and variable in the case of open loop integrators. Moreover, the mismatch of the passive components in the current acquisition circuitry and their dissimilar temperature coefficient make the measured line voltages/currents unbalanced although they are balanced in the actual circuit [7.20]. The unbalanced measured voltages/currents lead to unbalanced estimated flux and since the integration initial condition and the passive components mismatched temperature coefficients are variable in time, the resultant estimated rotor flux *d-q* components in the stationary reference frame are associated with a time-variable DC-offset. This degrades the accuracy of the speed estimation when using MRAS. The DC-offset problem occurs only on experimental implementation of the stator model. In simulation, the solver selects the zero crossing to start the integration, so the initial condition is always zero. Moreover, the effect of temperature coefficients or mismatch in voltages/currents measurement is not considered in simulation.

Many approaches have been proposed to overcome the problem of DC-drift in the stator model. The idea of replacing the integrator in the stator model with a low-pass filter is dominant [7.1]. This replacement introduces more delay and inaccuracy in the rotor flux phase angle estimation thus the use of the rotor flux derivative in MRAS instead of the rotor flux is introduced [7.2], [7.3]. The main problem with using the rotor flux derivative is the appearance of high frequency components in the motor stator current that creates computational problems. Improved MRAS based on the rotor flux compensates the phase angle and amplitude errors of the low-pass filter, using a load dependant flux observer [7.5] but the second order filter in this method adds extra error to the estimated flux. Another attempt to improve the performance of rotor flux based MRAS uses low-pass filters with corner frequencies that vary with the fundamental motor voltage frequency and compensates for the phase and amplitude error using their steady-state values [7.24]. The speed reversal problem associated with this technique is eliminated by performing the compensation before the low-pass filter [7.25]. Another method to improve the integration method, forces the flux trajectory to be circle by using an extra *PI*-controller, thus eliminating DC-offset [7.26]. This technique shows good performance in steady-state but exhibits start-up problems. Also, in case of DC-drifted measured motor currents, keeping the flux in a circular trajectory does not preserve oscillations in the estimated speed as this method only affects the total flux vector but does not solve the shift created in the flux *d-q* components resultant from DC-drift in the current measurement. High performance operation, even near zero speed, is achieved by constructing three compensators [7.27]. First, feedforward compensation for the large time constant drift, due to dissimilar temperature coefficients in current measurement boards, by tracking the time variable DC-offset voltage using a parallel stator model. Second, feedback compensation for the high frequency components in flux *d-q* components using a *PI*-controller and the error between the reference and the estimated flux vectors. Third, compensation for the inverter non-linear behaviour and on-line resistance estimation for the motor. Moreover, this method uses open loop integration, thus benefits from a wide estimation bandwidth. Despite these advantages, the method is complex as it uses three compensation techniques.

The DC-offset eliminator prposed in this chapter is simple in construction as only one compensation scheme is used, involving open loop integration, therefore a wide estimation bandwidth is achieved. The proposed DC-offset eliminator uses open loop integrators and

tracks the resultant shift in the estimated *d-q* flux components by calculating the average of the DC-shift then subtracts it from the original estimated flux components. The time delay in the average calculation process creates parasitic oscillations on the estimated *d-q* flux components. This delay is compensated in the synchronously rotating reference frame by means of low-pass filters to avoid any extra added phase/amplitude error. Since the proposed DC-offset eliminator deals directly with *d-q* flux components (not their resultant vector), elimination of fast/slow varying shifts are achieved with one compensator.

7.4.2 Proposed DC-offset eliminator

Figure 7.6 shows the block diagram of the proposed DC-offset eliminator which consists of six stages. The output from each stage is labelled *xj* where *j*=1, 2....12. The first stage is pure open loop integration where the output represents the rotor flux in the stationary reference frame with undetermined DC-offset, *x1* and *x2*. In the second stage, a procedure of calculating the maximum and minimum of the rotor flux with the DC-offset, then the average calculation is performed. The second stage is restarted every cycle. The calculated average from the second stage, *x3* and *x4*, is used in the next cycle to eliminate the DC-offset from the original rotor flux components in the third stage. Hence, a cycle delay is created. This is a relatively long time delay especially in the low speed range. Consequently, the resultant flux components from the third stage, *x5* and *x6*, suffer from a small time-varying DC-offset. So, stages four to six are utilized to compensate for this delay and to eliminate the small time-varying offset. Transformation from the *d-q* stationary to the *d-q* synchronously rotating reference frame is performed in the fourth stage on the flux components resulting from the third stage. Then, the transformed rotor flux components in the *d-q* synchronously rotating reference frame, *x7* and *x8*, are treated by low-pass filtering which eliminates high frequency distortion. The low-pass filtering process is performed in the synchronously rotating reference frame to eliminate the delay which occurs if performed in the stationary reference frame. In the sixth stage, the inverse transformation from the *d-q* synchronously rotating reference frame to the *d-q* stationary reference frame is performed on the *d-q* synchronously rotating reference frame filtered flux components, *x9* and *x10*. The resultant flux components in the *d-q* stationary reference frame, *x11* and *x12*, have no DC-offset, without any time delay with respect to the original DC-shifted flux components.

The proposed DC-offset eliminator is examined by running the motor at 200 rpm with a step speed input at no-load and then a 4 Nm load is applied while estimating the rotor flux for these cases. The experimental results for the proposed modified stator model produce DC-offset-free rotor flux *d-q* components estimations as shown in figures 7.7 and 7.8 respectively. These results are from the DSP internal memory, stored in matrix form. The DSP storage memory enables plotting of many signals, ensuring synchronization as they are all stored simultaneously at the end of the execution cycle. Figures 7.7 and 7.8 part (a) show the estimated rotor flux components after the calculated offset is subtracted from them. Since the process of average calculation, shown in figures 7.7 and 7.8 part (b), takes one cycle, the resultant estimated flux components suffer from small-value time-varying DC-offset which needs to be totally eliminated. With the aid of the electrical transformation angle, calculated from the estimated speed and the slip speed, the estimated flux components are transformed to synchronously rotating reference frame as shown in figures 7.7 and 7.8 part (d). The high frequency oscillations of the flux components in the synchronously rotating reference frame represent the time-varying offset. By using low pass filtering, these high frequency oscillations on the flux components are eliminated as shown in figures 7.7 and 7.8 part (e). A final stage of retransformation to the stationary reference frame results in pure sinusoidal DC-offset free flux components as shown in figures 7.7 and 7.8 part (f)

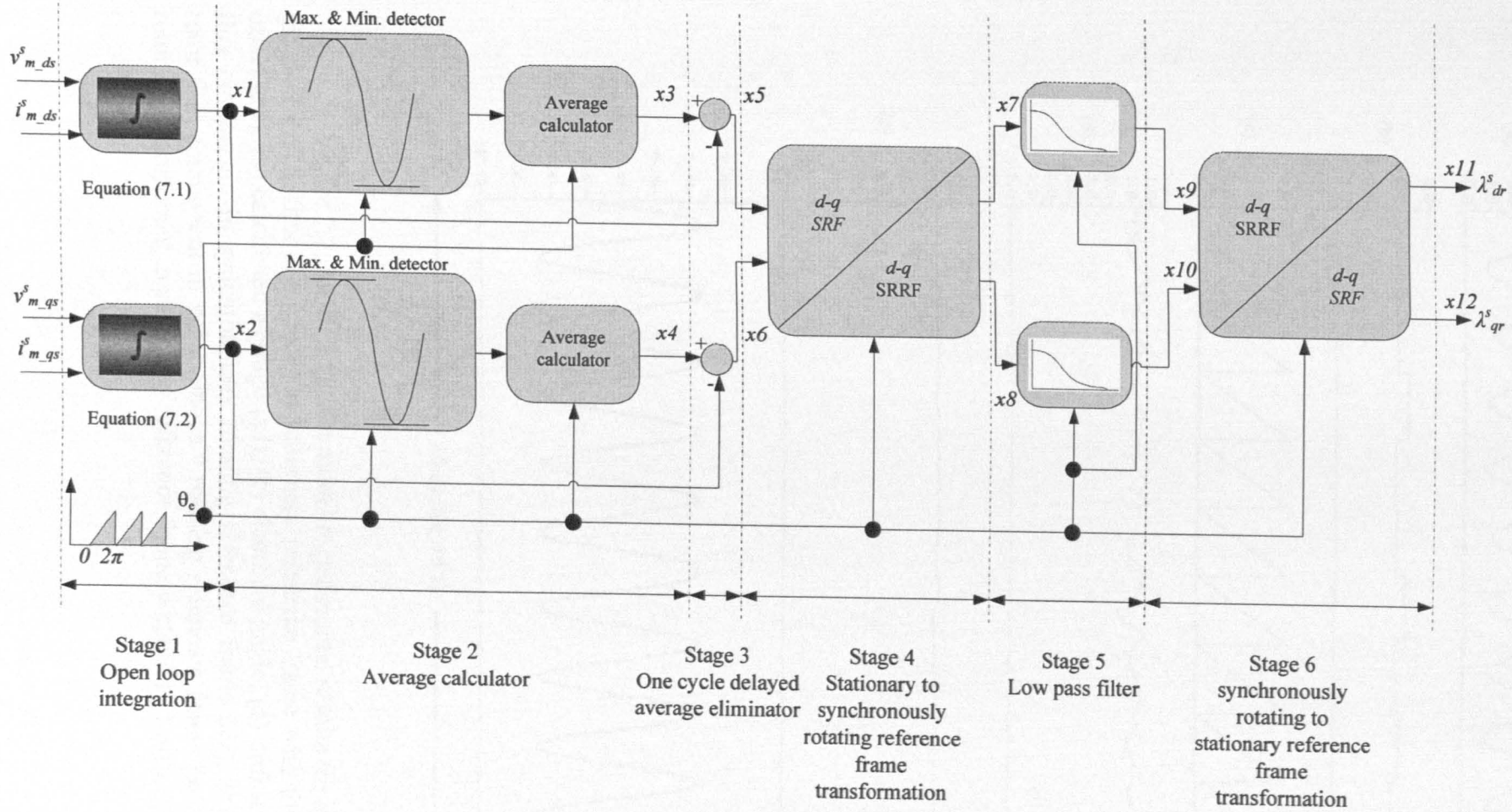


Figure 7.6: Proposed stator model DC-offset eliminator.

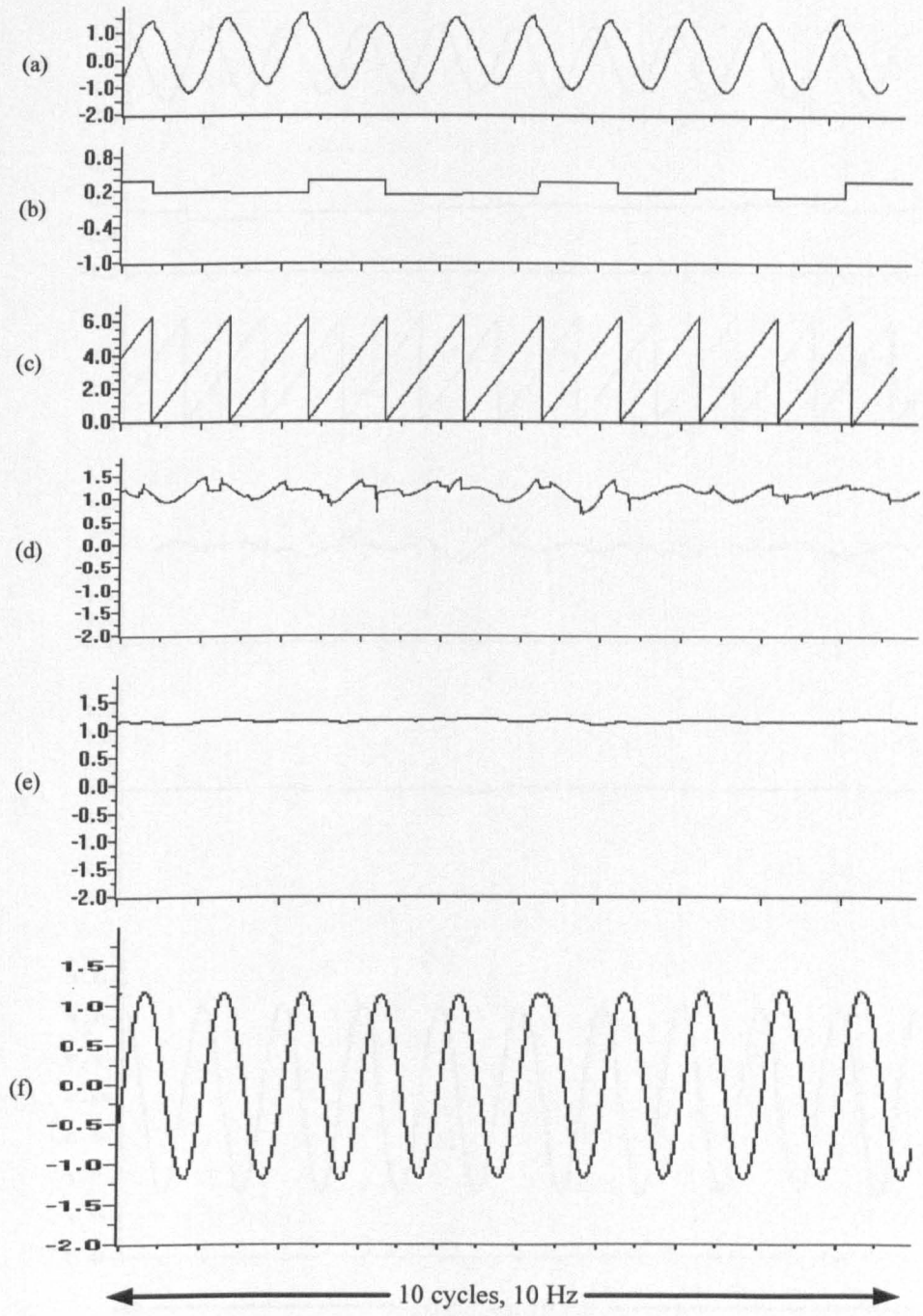


Figure 7.7: Modified stator model experimental results for *d*-axis
(a) *d*-axis rotor flux component in stationary reference frame with time varying DC-offset (*x5*), (b) calculated average (*x3*), (c) electrical angle, (d) unfiltered *d*-axis rotor flux component in synchronously rotating reference frame (*x7*), (e) filtered *d*-axis rotor flux component in synchronously rotating reference frame (*x9*), and (f) *d*-axis rotor flux component in stationary reference frame without DC-offset (*x11*).

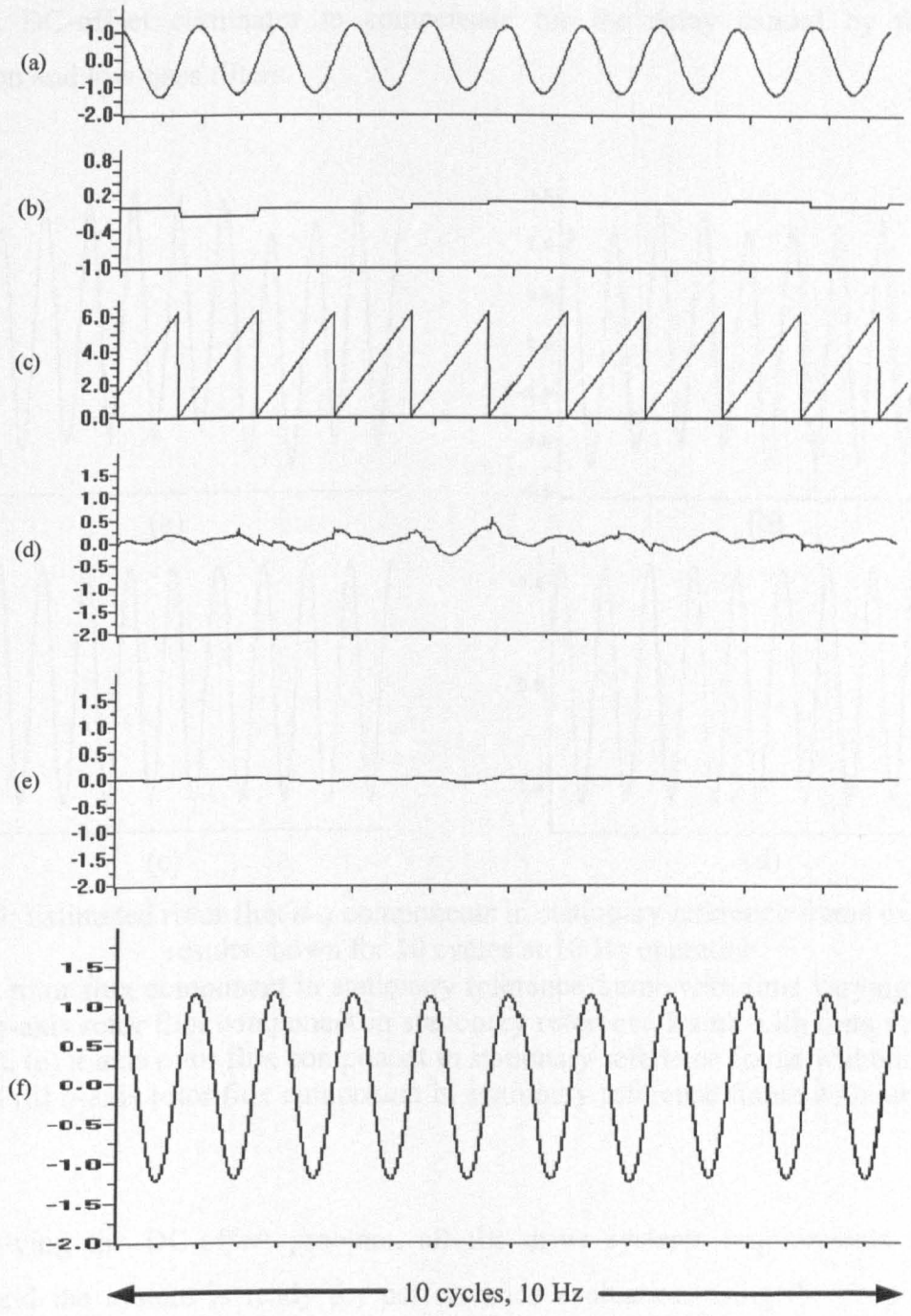


Figure 7.8: Modified stator model experimental results for q-axis
(a) q-axis rotor flux component in stationary reference frame with time varying DC-offset (*x6*), (b) calculated average (*x4*), (c) electrical angle, (d) unfiltered q-axis rotor flux component in synchronously rotating reference frame (*x8*), (e) filtered q-axis rotor flux component in synchronously rotating reference frame (*x10*), and (f) q-axis rotor flux component in stationary reference frame without DC-offset (*x12*).

Figure 7.9 shows that there is no delay between the estimated flux components in the d-q axis and the original components with DC-offset. This validates the efficiency of the

proposed DC-offset eliminator to compensate for the delay caused by the average calculation and low-pass filters.

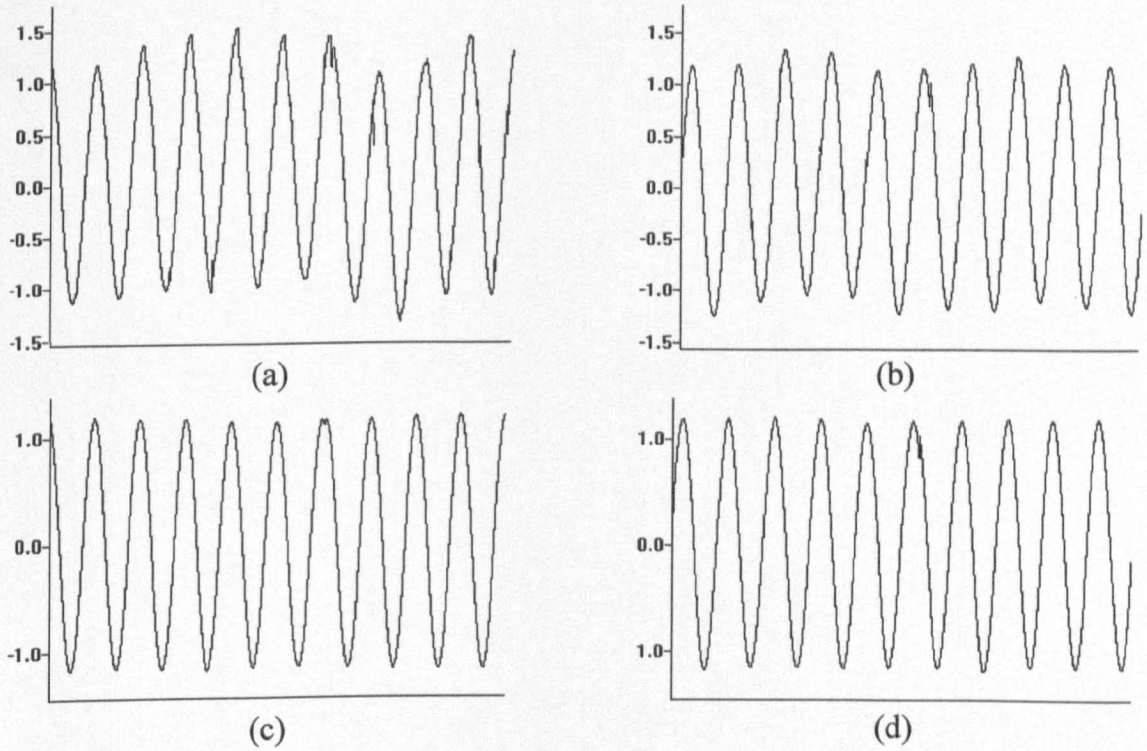


Figure 7.9: Estimated rotor flux *d-q* components in stationary reference frame experimental results shown for 10 cycles at 10 Hz operation
(a) *d*-axis rotor flux component in stationary reference frame with time varying DC-offset (*x5*), (b) *q*-axis rotor flux component in stationary reference frame with time varying DC-offset (*x6*), (c) *d*-axis rotor flux component in stationary reference frame without DC-offset (*x11*), and (d) *q*-axis rotor flux component in stationary reference frame without DC-offset (*x12*).

By solving the DC-offset problem, all the drive systems requirements have been fulfilled and the system is ready for performance evaluation using the proposed speed estimation technique.

7.5 Drive Performance Evaluation

In sections 7.3 and 7.4, the motor voltage was calculated from the inverter side by the proposed motor voltage calculator and the DC-offset occuring in the rotor flux estimation has been solved by the proposed DC-offset eliminator. The sensorless operation of the CSI vector controlled, long motor feeder drive can be considered. The block diagram of the proposed sensorless indirect vector controlled drive is shown in figure 7.10. The proposed system is tested at 200 rpm with a sudden load change of 4 Nm. The feeder length is 1 km

and the operating switching frequency is 1 kHz. The low-voltage scaled prototype that emulates MV drive, as used in chapters' four to six, is used in this experimental setup.

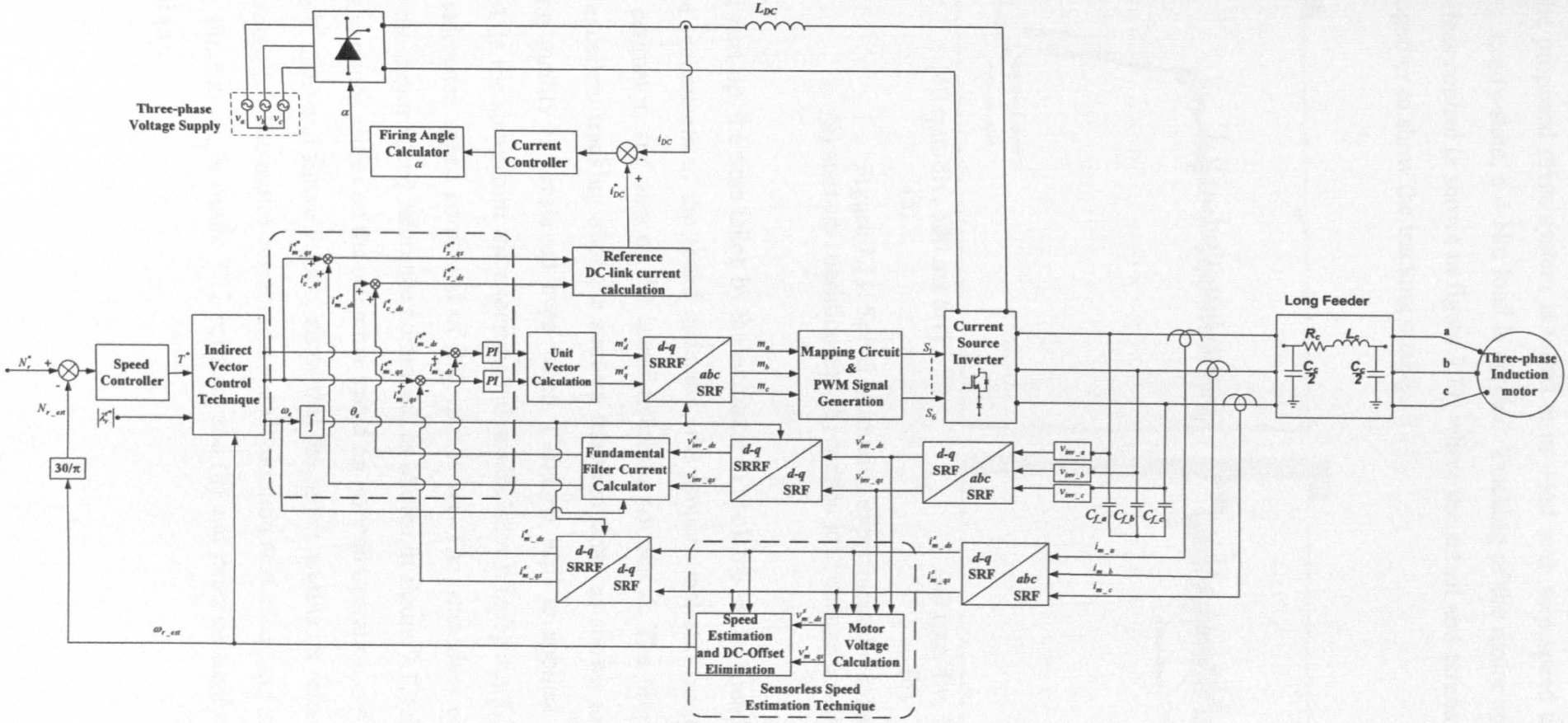
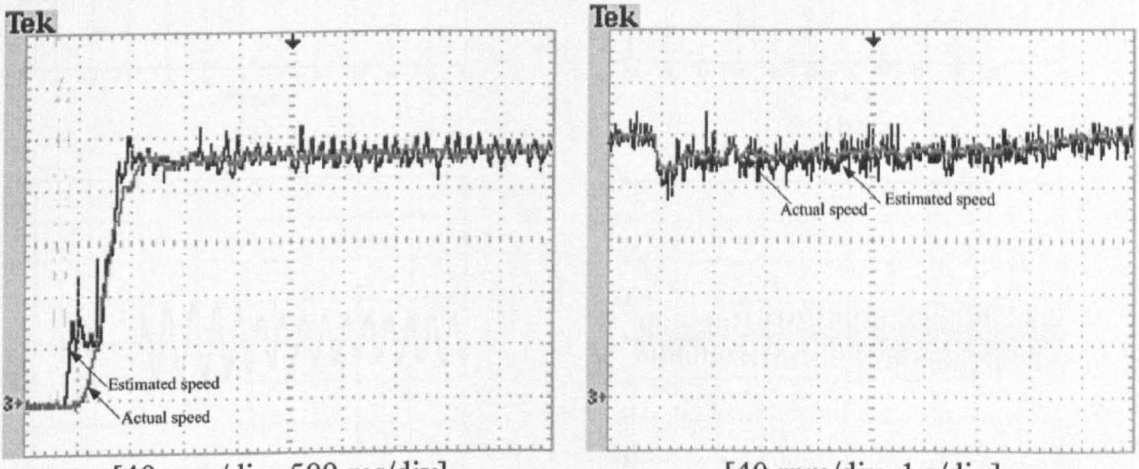


Figure 7.10: Proposed sensorless indirect vector controlled CSI induction motor drive.

The proposed drive system is tested at no-load with step speed command at start-up. During steady-state, a 4 Nm load is applied. Tracking of the motor speed by the proposed sensorless control is shown in figure 7.11, where the actual and estimated motor speeds are plot together to show the tracking quality.



[40 rpm/div, 500 ms/div] (a)

[40 rpm/div, 1 s/div] (b)

Figure 7.11: Speed estimation experimental results
(a) start-up condition and (b) sudden load change condition.

At start-up, the time taken by the estimator to track the actual speed is dependant on the control parameters of the speed estimator, the proportional and integral constants of the speed estimator, and also on the speed reference command. The proposed system results show excellent tracking after the start-up transient time, as shown in figure 7.11(a). The tracking quality is preserved even when a sudden load is applied as shown in figure 7.11(b). In the simulation and experimental results, shown in figures 7.12 and 7.13, at start-up, a reference speed command of 200 rpm is set. The sensorless estimation accurately tracks the motor speed reference command, as shown in figure 7.12(a) and figure 7.13(a). After the motor settles on the reference speed on no-load operation, a 4 Nm load is applied. Figure 7.12(b) and figure 7.13(b) show that the motor retains its reference speed after the load is applied. The motor current and speed variation at start-up and on loading are shown by the simulations in figure 7.12 parts (c) and (d) and experimentally in figure 7.13 parts (c) and (d).

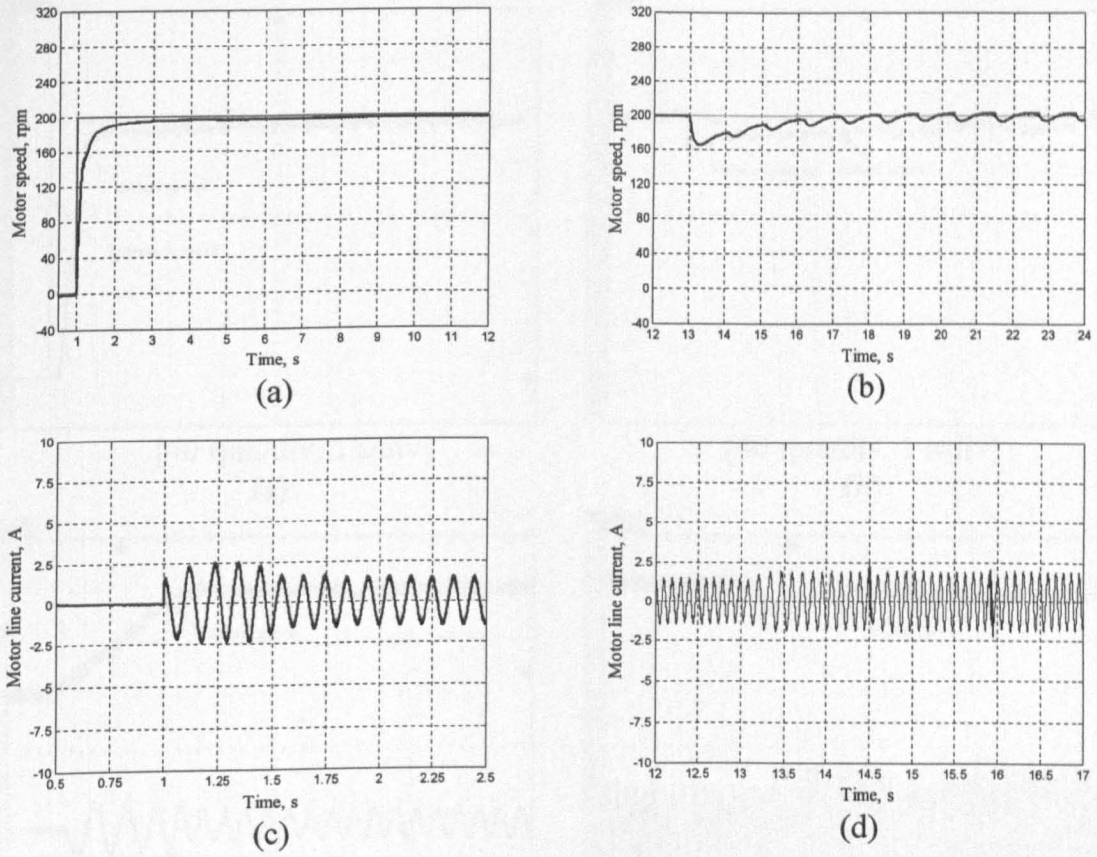
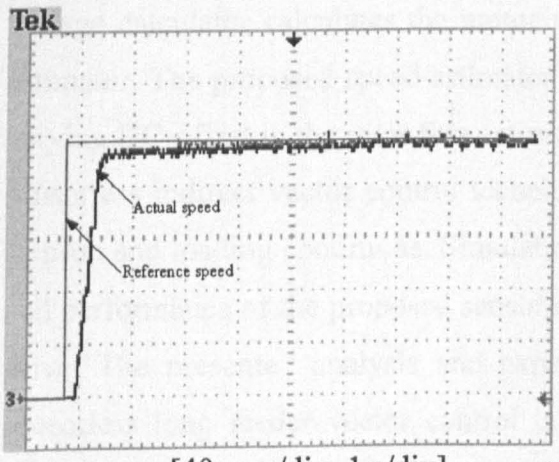
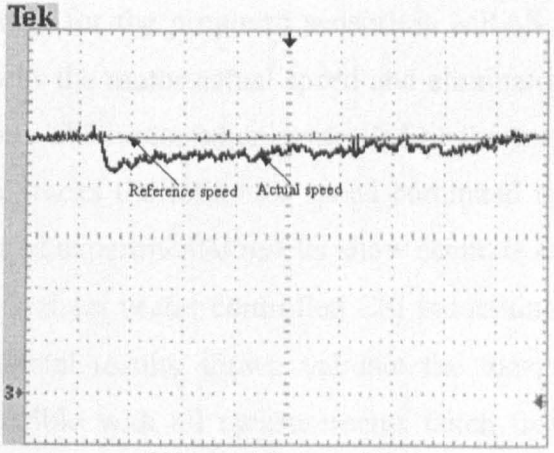


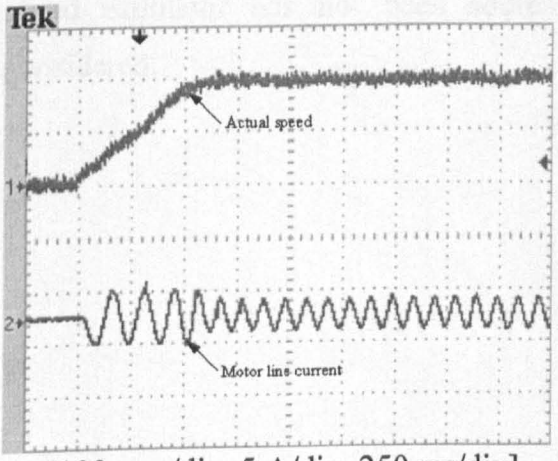
Figure 7.12: Drive performance simulation results
a, c: Start-up b, d: Sudden load change
(a, b) actual and reference motor speed, (c, d) motor line current.



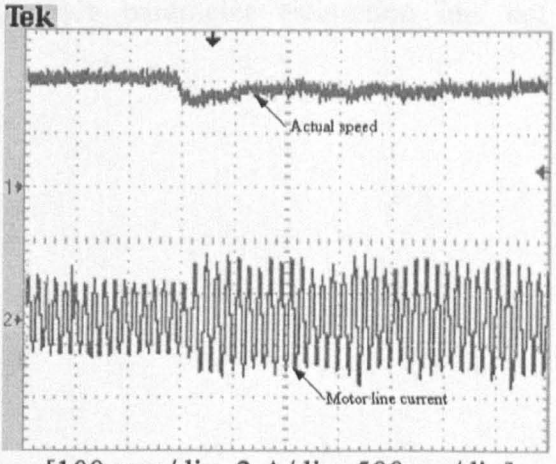
[40 rpm/div, 1 s/div]
(a)



[40 rpm/div, 1 s/div]
(b)



[100 rpm/div, 5 A/div, 250 ms/div]
(c)



[100 rpm/div, 2 A/div, 500 ms/div]
(d)

Figure 7.13: Drive performance experimental results
a, c: Start-up b, d: Sudden load change
(a, b) actual and reference motor speed, (c, d) motor actual speed and line current.

Simulations and experimental results show the good dynamic performance of the drive system with the proposed motor voltage calculator and speed estimator.

Summary

Induction motor drives with long motor feeders require speed estimation as the feeder length makes direct speed measurements impractical. The MRAS technique is a reliable and stable method for speed estimation and has been used in this chapter. Two major problems occur when applying MRAS to long motor feeder drives. First, the motor voltage must be estimated. Second, DC-drift occurs in the rotor flux estimation due to using open loop integrators in the stator model. A remote motor voltage calculator and a novel DC-offset eliminator for the stator model have been presented. The proposed remote motor

voltage calculator calculates the motor voltage for the proposed sensorless MRAS speed estimator. The proposed speed estimator tracks the motor actual speed and eliminates time varying DC-offset in the rotor flux estimation. The motor when controlled by the proposed sensorless indirect vector control technique, tracks the reference speed command in both step-up and loading conditions. Simulation and experimental results show accurate control and performance of the proposed sensorless indirect vector controlled CSI induction motor drive. The presented analysis and experimental results shown validate the theory that sensorless long feeder vector control is possible with all measurements taken from the inverter side. Zero and near zero speed sensorless drive operation using the proposed speed estimator has not been addressed, since parameter estimation has not been considered.

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CHAPTER EIGHT:

Conclusion

8.1 General Conclusion

PWM CSRs usually utilize SHE modulation as the switching frequency is limited in MV high-power drives. Although SHE provides low order harmonic elimination with a low switching frequency, PWM CSRs using this technique do not meet the IEEE 519 regulation. Two AC side filter techniques are commonly used, a passive filter or a shunt APF. The evolution of the GCT, and operating voltage/power extension of other devices, like the IGBT, has enabled more PWM CSR semiconductor configurations. Optimum device selection depends on the main criteria of the comparison, like losses, size or number of devices.

PWM 2-level VSI indirect vector controlled drives are common in MV applications. The utilization of these drives with a long motor feeder leads to motor terminal over-voltage and ringing problems. Surge filter techniques have been proposed to solve these problems, namely a motor terminal *RC* filter and an inverter output *RLC* filter both of which are simple, efficient, and robust. The PWM CSI direct vector controlled drive is an alternative to the VSI drive. A CSI provides motor friendly voltage waveforms and short circuit protection. Consequently, no surge filters are needed for long motor feeder applications. For CSI drives, direct vector control is superior to conventional indirect vector control which suffers from field orientation loss. Due to the feeder length, operation as a speed sensorless drive is mandatory. Among various speed sensorless techniques, MRAS proved to be reliable and robust to parameter variations. DC-offset in the flux estimation, is the main problem in MRAS speed estimators. Most speed sensorless techniques require feedback of motor voltage and current, but direct measurement of these quantities is impractical for long feeder lengths.

The thesis outcomes can be enumerated as follows:

- For PWM CSR power quality improvement, AC side passive filters and shunt APFs have been compared. It is concluded that the APF requires less fundamental line current. The passive filter draws a fixed current independent of the rectifier loading condition while the APF adapts its current according to the compensated

rectifier load. The APF ensures near unity power factor over the full load range, while the power factor degrades at light loading condition in the passive filter case. Rectifier semiconductor over-voltage stressing occurs with passive filters due to rectifier voltage distortion and leading power factor operation. Passive filter damping resistance adds losses to the system. The APF requires a three-phase inverter bridge and a high-frequency step-down transformer for shunt connection, to give low-voltage high-current inverter operation. Passive filter construction is simpler.

- A modified loss calculation methodology, based on device data sheets, has been presented for the PWM CSR. Three PWM CSR semiconductor configurations were compared, SGCT, AGCT, and HVIGBT, from three different aspects: losses, size and number of devices, for three MV levels, 2.4 kV, 3.3 kV and 6.6 kV. The comparison results, for the studied voltage ranges, showed that the AGCT is the optimum selection for minimum losses. The SGCT provides the minimum number of devices, while the HVIGBT gives minimum converter size.
- Surge filters, motor terminal *RC* and inverter output *RLC*, effects on a PWM VSI indirect vector controlled drive have been compared in the long motor feeder case. An inverter output *RLC* filter provides motor terminal over-voltage protection with lower high-order harmonics in the motor line current, its *d-q* components, and DC-link current. Neither filter contributes to the speed rise time at start-up and loading or the common-mode voltage. For variable feeder lengths, the inverter output *RLC* filter exhibits higher losses and higher DC-link current but gives better system voltage regulation than a motor terminal *RC* filter.
- Since indirect vector control is simpler and less sensitive to parameter variations than direct vector control, an indirect vector controlled PWM CSI with modified field orientation was assessed. The proposed indirect controller achieves complete field orientation during steady-state similar to a direct controller, in addition to a speed rise time improvement that is better than with conventional indirect control.
- An indirect vector controlled VSI drive was compared with the proposed indirect vector controlled CSI, with a long motor feeder. The CSI drive provides a near sinusoidal motor voltage, with less harmonic contents in both the motor current and inverter common mode voltage. The CSI topology is more complex than the VSI if

IGBTs or AGCTs are used due to the extra series fast recovery diode in each inverter half leg. From the voltage utilization aspect, the CSI ensures a higher fundamental inverter output voltage than the VSI, even when THIPWM is used in the VSI case, thus is capable of driving longer feeder lengths. The CSI capacitive output filter is fixed for the examined feeder lengths, up to 2.4 km, and provides near sinusoidal output voltage. Therefore, no surge filters are needed and off-the-shelf power feeders can be used. For the VSI case, *RLC* inverter output elements must be designed for each specific feeder length and since it is only a surge filter, the inverter output voltage still exhibits a high *dv/dt*. Thus, special insulation-reinforced feeders should be used for the VSI long motor feeder drive. The filter resistive element adds losses to the VSI drive. The CSI drive efficiency is higher than that of the VSI drive for the investigated range.

- A MRAS speed estimation technique is presented. The problem of direct measurement of motor voltage and current is solved by the proposed remote calculator, capable of calculating the motor voltage/current, from the inverter side and feeder parameters, using linear equations. Speed estimation errors due to drift and shift in flux estimation, occurring in the stator model, are eliminated by a proposed DC-offset eliminator. A complete sensorless indirect vector controlled PWM CSI drive was presented and examined with a long motor feeder.

8.2 Author's Contribution

- Two filter techniques, passive and active, for MV PWM CSRs were compared with highlights on the MV PWM CSR semiconductors over-voltage stress dues to passive filters.
- Systematic method, dependant on simulation and device practical data sheets, for assessing semiconductor losses, size and number of series devices for MV PWM CSRs, was presented.
- Investigation of two types of surge filter effects on long motor feeder VSI indirect vector controlled drive, were carried out.
- Modified indirect vector controller for CSI drives capable of achieving complete field orientation was proposed.
- VSI and the proposed CSI drive systems for long motor feeder application were compared.

- MRAS speed estimator with novel DC-offset estimator for the stator model was proposed.
- Remote motor voltage/current calculator for long motor feeder MRAS-based sensorless drives was proposed.

8.3 Future Research

- Study the operation of the PWM CSR with a passive filter under active damping control, without a damping resistor, incorporating dual power factor control.
- Adaptation of the proposed loss calculation method to the PWM CSI.
- Investigation of VSI drive output *RLC* filter modification for common mode voltage reduction.
- Performance analysis of the proposed indirect vector controlled CSI drive with adaptive controllers instead of conventional PI controllers.
- Comparison between the proposed CSI drive and multilevel inverter drives for long motor feeder applications.
- Investigation of the proposed MRAS speed estimator at speeds near and around zero.
- Online parameter estimator for the proposed speed estimator.

Appendix A: CSR SHE tabulated switching angles

Table A: Gating angles for PWM CSR with 5th and 7th harmonic elimination

m_a	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.03
	Degrees										
θ_1	–13.5	–11.9	–10.3	–8.60	–6.86	–5.00	–3.98	–0.67	2.17	6.24	7.93
θ_2	14.2	13.5	12.7	12.0	11.4	10.8	10.4	10.3	10.8	12.6	13.8
θ_3	43.6	42.2	40.9	39.5	38.0	36.6	35.1	33.6	32.1	30.5	30.0
θ_4	45.8	46.5	47.3	48.0	48.6	49.2	49.6	49.7	49.2	47.3	46.2
θ_5	73.5	71.9	70.3	68.6	66.9	65.0	63.0	60.7	57.8	53.8	52.1
θ_6	106.5	108.1	109.7	111.4	113.1	115.0	117.0	119.3	122.2	126.2	127.9
θ_7	134.2	133.5	132.7	132.0	131.4	130.8	130.4	130.3	130.8	132.6	133.8
θ_8	136.4	137.8	139.1	140.5	142.0	143.4	144.9	146.4	147.9	149.5	150.0
θ_9	165.8	166.5	167.3	168.0	168.6	169.2	169.6	169.7	169.2	167.3	166.2
θ_{10}	193.5	191.9	190.3	188.6	186.9	185.0	183.0	180.7	177.8	173.7	172.1
θ_{11}	256.4	257.8	259.1	260.5	262.0	263.4	264.9	266.4	267.9	269.5	270.0
θ_{12}	283.6	282.2	280.9	279.5	278.0	276.6	275.1	273.6	272.1	270.5	270.0

Appendix B: Losses equations' coefficients

Table B: Equations (3.3) - (3.9) coefficients

Coefficient \ χ	SGCT (6.5 kV)	IGBT (4.5 kV)	IGBT (6.5 kV)	AGCT (4.5 kV)	Series Diode (4.5 kV)	Series Diode (6 kV)
$a1$	5.5×10^{-3}	2.8×10^{-3}	3.75×10^{-3}	1.0×10^{-3}	3.5×10^{-3}	0.67×10^{-3}
$b1$	3.1	1.65	3.625	0.7	1.1	1.34
$a2$	1.0×10^{-3}	5.0×10^{-3}	7.9×10^{-3}	0.375×10^{-3}	-	-
$b2$	0.2	-0.25	0.036	0.0	-	-
$a3$	7.0×10^{-3}	3.12×10^{-3}	5.0×10^{-3}	5.75×10^{-3}	-	-
$b3$	-0.4	-0.125	0.0	-0.12	-	-
$a4$	7.0×10^{-3}	-	-	-	1.8×10^{-3}	5.0×10^{-3}
$b4$	1.4	-	-	-	0.0	0.0

Appendix C: Motor parameters (low voltage scaled system)

Table C: Motor parameters

Motor type	Induction	-
Number of phases	3	-
Number of poles	6	-
Rated power	5	HP
Rated line voltage	380	V
Rated line current	8	A
Stator resistance	4.1	Ω
Rotor resistance	6	Ω
Stator leakage inductance	30.7	mH
Rotor leakage inductance	30.7	mH
Magnetizing inductance	758	mH
Inertia	0.045	$Kg.m^2$
Friction	0.045	N.m.s

Appendix D: Feeder parameters (low voltage scaled system)

Table D: Feeder parameters

Quantity	*Value*	*Unit*
Cable type	Three core shielded 440 V	-
Manufacturer part number	THEN-THWN 14AWG, 600 V	-
Resistance	0.0225	Ω/m
Inductance	1.1	μH/m
Capacitance	0.02	nF/m
Length used in experiment	1	Km

Appendix E: *RC* motor terminal and *RLC* inverter output surge filters' parameters

Table E: Surge filters' parameters

	RLC inverter output filter	***RC motor terminal filter***
Resistance	234.5 Ω	234.5 Ω
Capacitance	0.47 μF	100 nF
Inductance	10 mH	-

Appendix F: Experimental test rig, hardware and software

In this thesis, a scaled low-voltage practical test rig is constructed to emulate the studied MV drive. The experimental implementation target is to verify the simulation results. Details on the hardware construction, software code and photos are presented in this appendix. Two main drive systems are practically investigated in this thesis. First, a VSI based drive system with long motor feeder. Second, a CSI based drive system with long motor feeder. Figures F.1 and F.2 show the examined systems block diagrams.

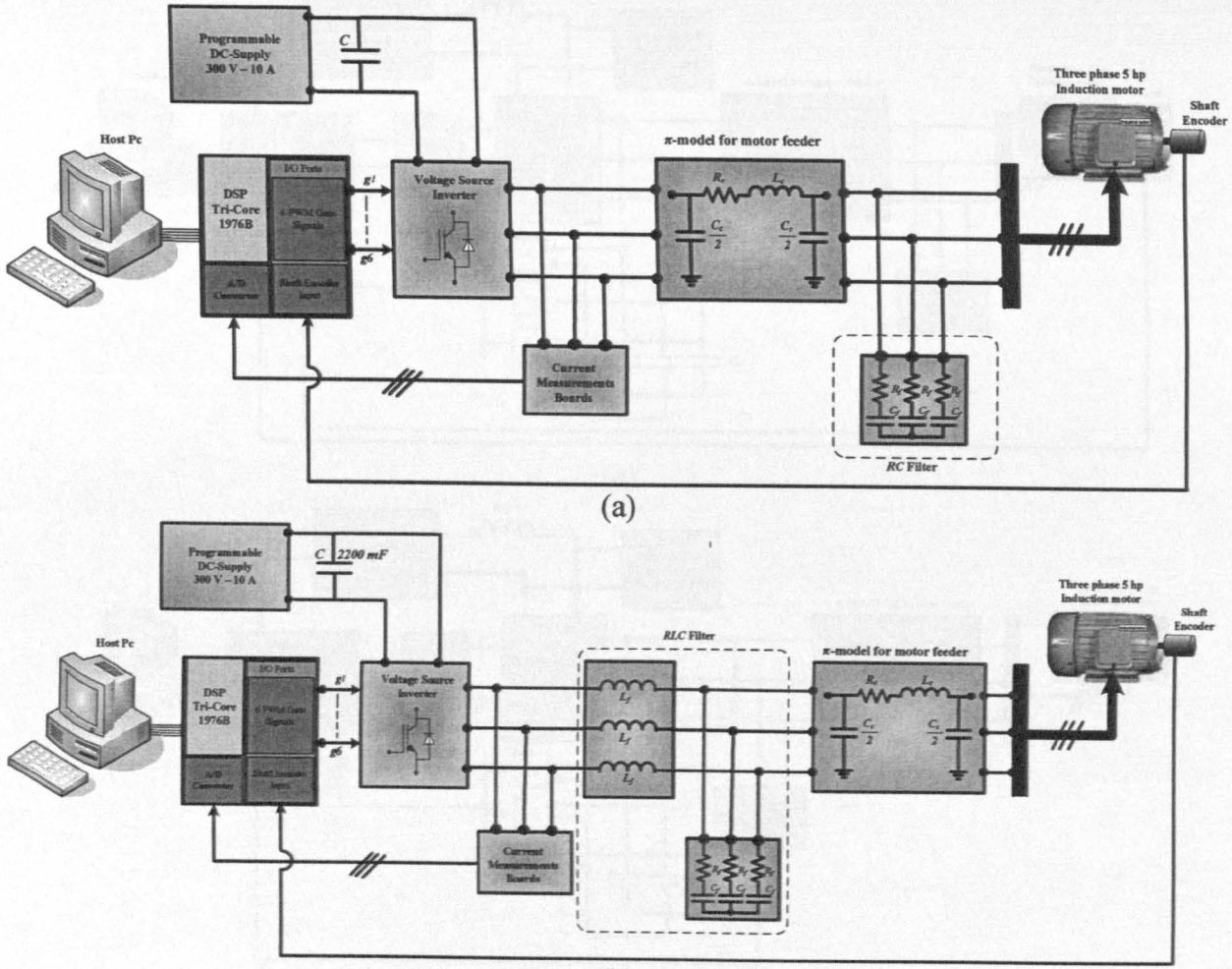


Figure F.1: VSI based drive test rigs block diagram
(a) motor terminal *RC* filter and (b) inverter output *RLC* filter.

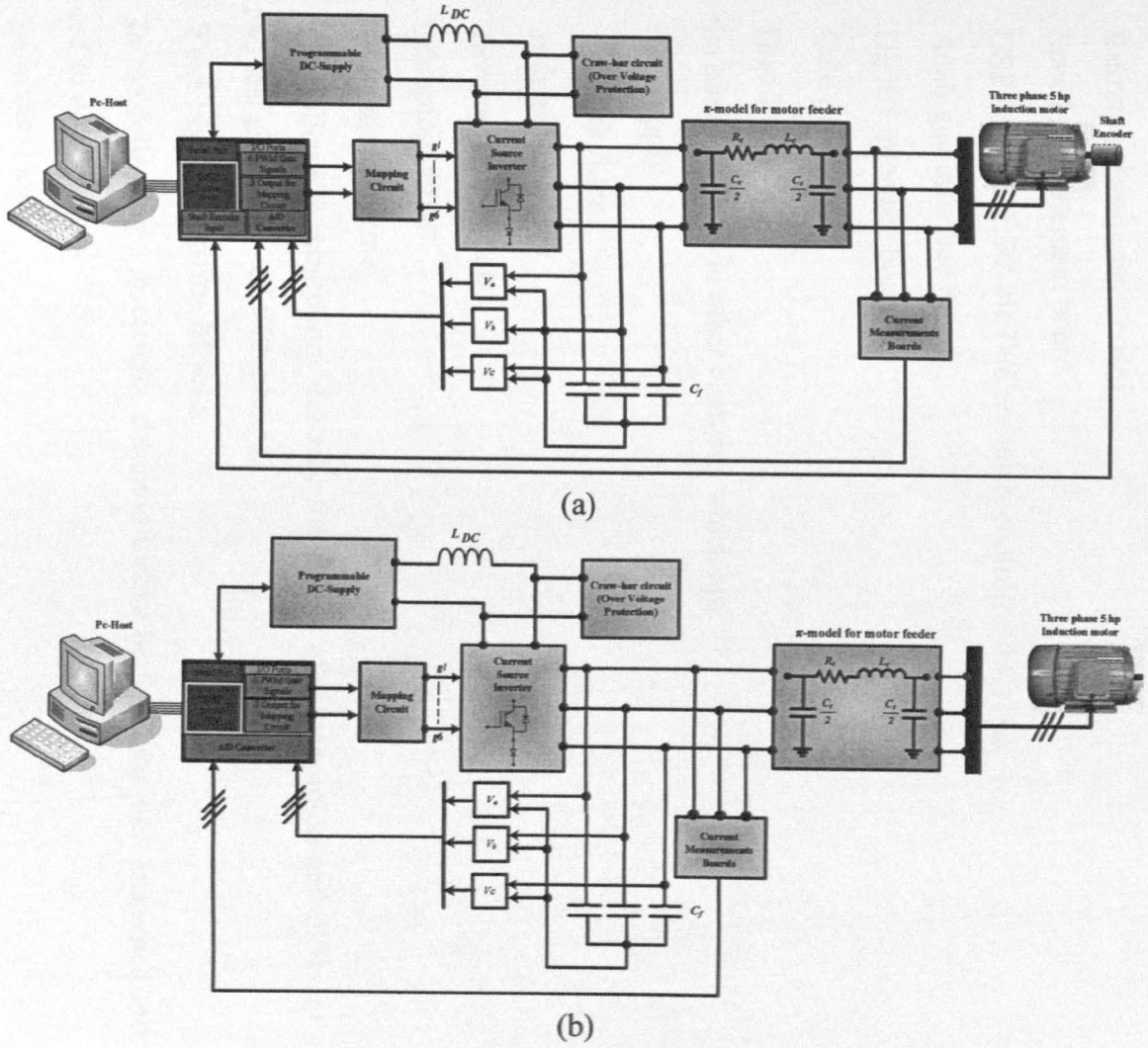


Figure F.2: CSI based drive test rigs block diagram.
(a) Speed sensored control and (b) speed sensorless control with motor voltage estimator.

As shown in figures F.1 and F.2, the two test rigs have common blocks which are:

- Induction motor
- Motor load
- Feeder
- Voltage measurement board
- Current measurement board
- Speed measurement board
- DSP controller: 32-bit *TriCore* microcontroller TC1796
- Analogue interface board
- Digital interface board
- Gate drive board
- Host PC

While the two rigs differ in other elements which are:

- DC supply
- DC-link filter
- Inverter topology
- Inverter output filter
- Mapping circuit
- Protection scheme

The following subsections describe the details of the common and different elements of the two test rigs enhanced with photos.

F.1 Test rigs common blocks

In the following subsections, common blocks between the two examined test rigs are illustrated in details.

i. Induction motor

The induction motor is the main controlled element for the drive systems under study. A laboratory low voltage scaled motor is selected to be speed controlled. The motor parameters are listed in Appendix C. The motor photo is illustrated in figure F.3

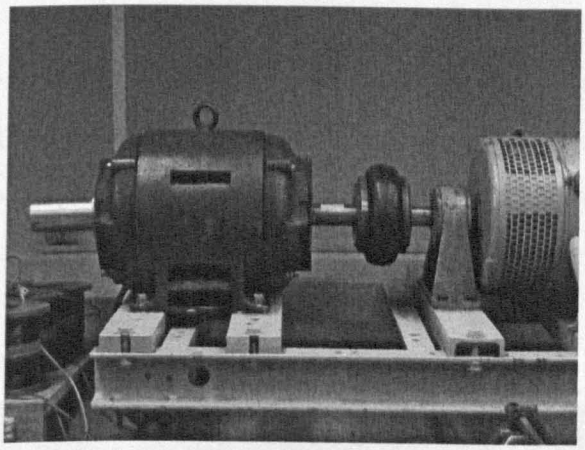


Figure F.3: Controlled induction motor.

ii. Motor load

In order to test the drive systems under different loading conditions, the induction motor must be loaded with a controllable load. A DC generator with a resistive load is mechanically coupled to the induction motor acting as a variable mechanical load when the generator resistive load varies. Figure F.4 shows the DC generator, resistive load and the mechanical coupling with the induction motor.

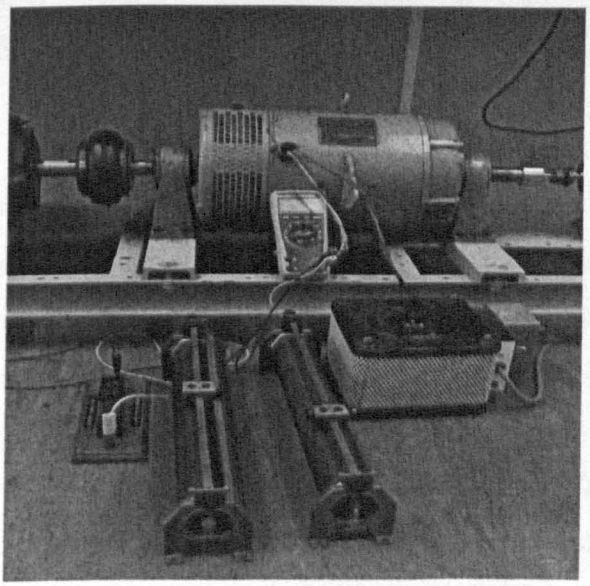


Figure F.4: Induction motor load.(DC generator with resistive load)

iii. Feeder model

As the main thesis target is the study of long motor feeder applications, a feeder suitable to the investigated low-voltage scaled system is selected. The feeder parameters are listed in Appendix D. For experimental realisation of a 1 km length, the feeder parameters for this specific length are calculated and implemented using the lumped impedance π-network as shown in figure F.5

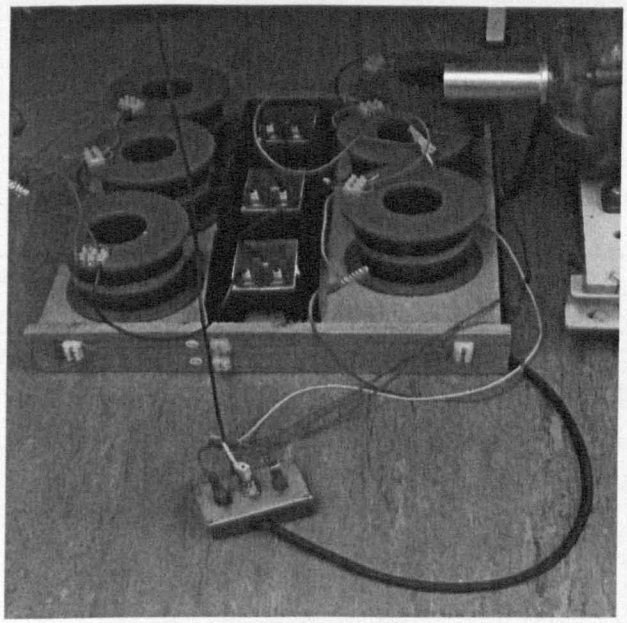


Figure F.5: Feeder model for 1 km length.

iv. Voltage measurement board

The voltage sensing circuits are implemented to measure the motor terminal voltage and/or inverter output voltage. The voltage measurement board is shown in figure F.6. The LEM voltage transducer LV 25-P uses the Hall-effect to measure AC and DC signals with galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit). Table F.1 shows the nominal parameters of the transducer used. This sensor can sense a range up to 500 V and a high frequency bandwidth, but dependent on the series connected external resistor in the primary circuit of the transducer. The transducer output is amplified through a signal conditioning circuit and fed to the control circuit. The voltage transducer circuit diagram is shown in figure F.7.

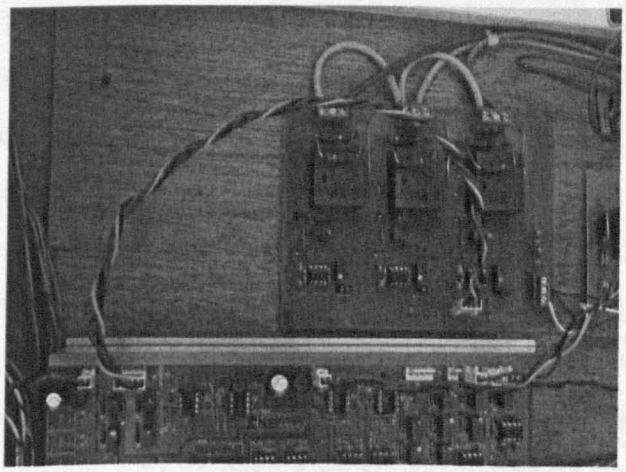


Figure F.6: Voltage measurement board.

Table F.1: The voltage transducer data sheet

Primary nominal current	10 (rms) mA
Primary current (measuring range)	0... ± 14 mA
Primary nominal voltage	10... 500 V
Bandwidth	Drop resistor dependent (max. 20 kHz)
Accuracy	± 0.8 %

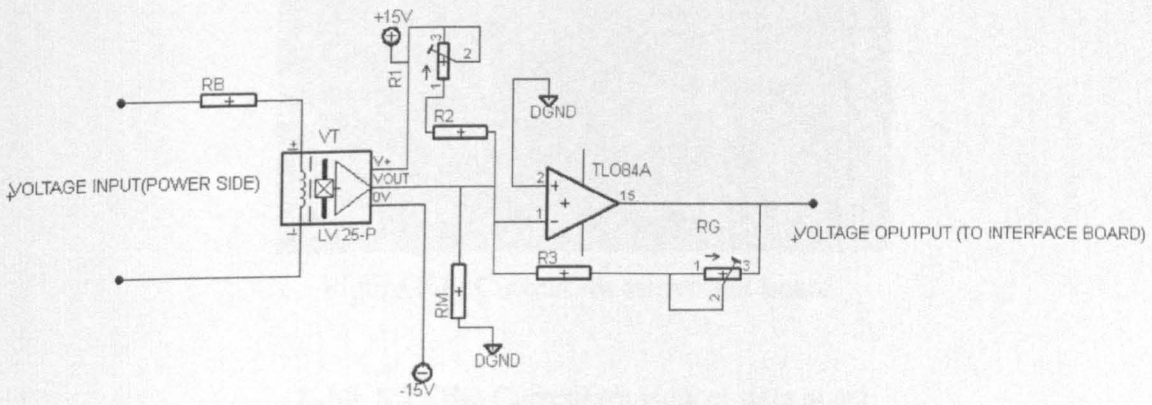


Figure F.7: Voltage measurement circuit diagram.

Note that the resistor *RB* is used to adjust the input primary current while the resistor *RM* is used to adjust the value of the secondary voltage. The op-amp following the sensor is used to tune the gain of the output voltage signal. A capacitor *C* can be shunt connected on the op-amp input-output circuit for filtering action. Care must be taken not to exceed its value to

avoid parasitic delay for the measured. In addition to the amplification, the op-amp is used to add a DC signal to shift the measured signal to be all positive value in order to match the DSP A/D input characteristics.

v. Current measurement board

The current sensing circuits are implemented to measure the motor current. The current transducer board is shown in figure F.8. The Hall-effect current sensing devices LEM (LA 55-P) were used. Table F.2 shows the nominal parameters of the transducer used. This type of sensors has the advantage of complete isolation from sensed signal beside the ease of implementation. These current sensors have a sensing range of 0A to 50A, adjustable and a frequency range from DC to 200 kHz. For proper operation, the output of the transducer is amplified through a signal conditioning circuit and fed to the control circuit. The current transducer circuit diagram is shown in figure F.9.

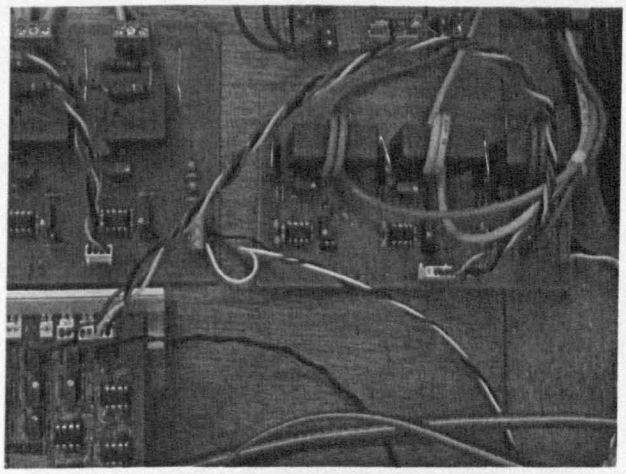


Figure F.8: Current measurement board.

Table F.2: The Current transducer data sheet

Nominal current	50 (rms) A
Current output	1 mA/A
Frequency range	DC to 200 kHz
di/dt	> 50 A/μs

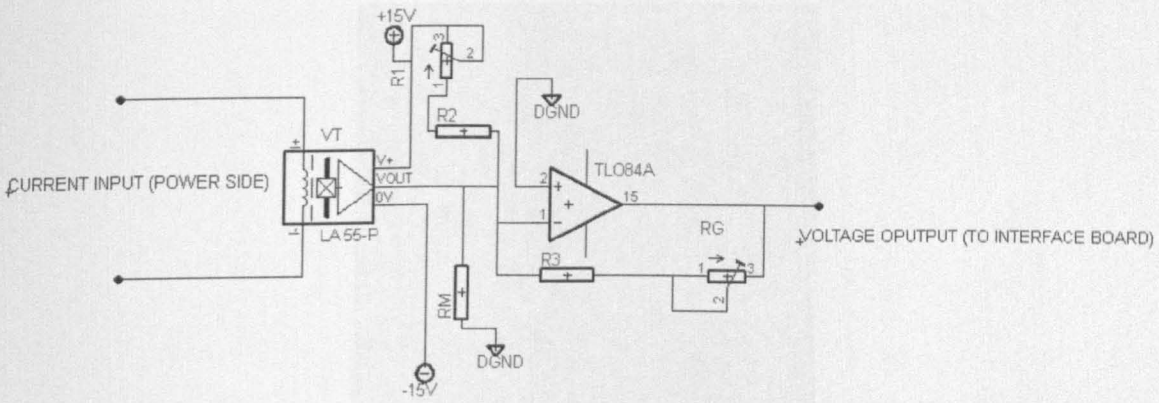


Figure F.9: Current measurement circuit diagram.

vi. Speed measurement board

For speed sensored operations, a shaft encoder is used to measure the motor speed. The encoder is connected to the motor via flexible coupling. Figure F.10 shows the encoder and the flexible coupling. An isolation board is used to minimize the noise and increase the isolation between the encoder and the DSP digital input. Note that the encoder pulses output are +5 V peak while the maximum DC input to the DSP is 3.3 V so the isolation IC ADUM1400 also provides level shifting. The speed measurement board and circuit schematics are shown in figures F.11 and F.12 respectively.

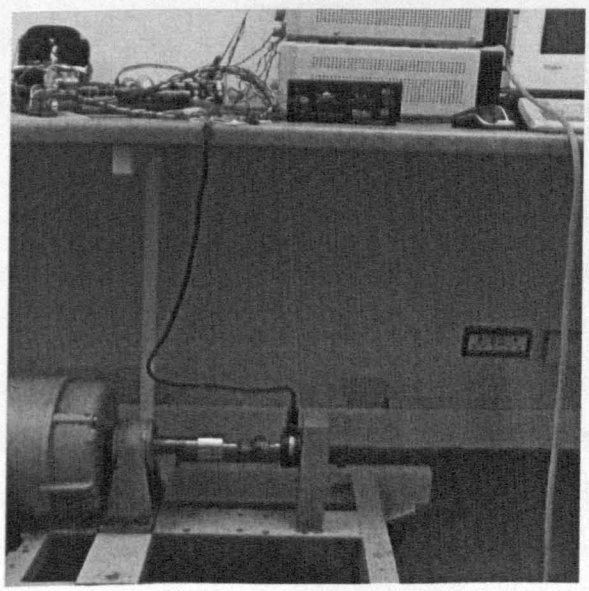


Figure F.10: Shaft encoder and flexible coupling.

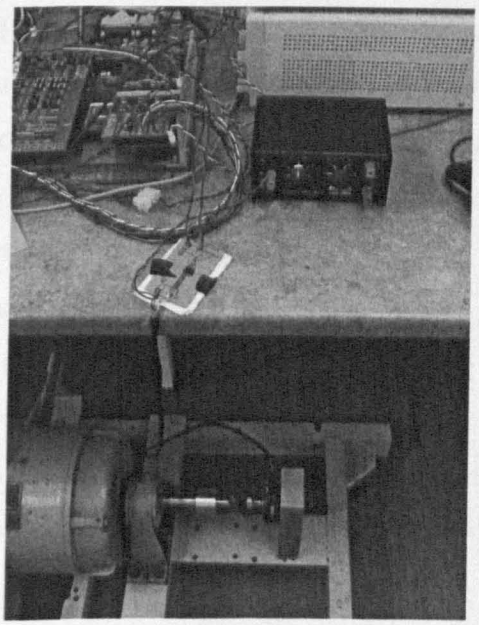


Figure F.11: Speed measurement board.

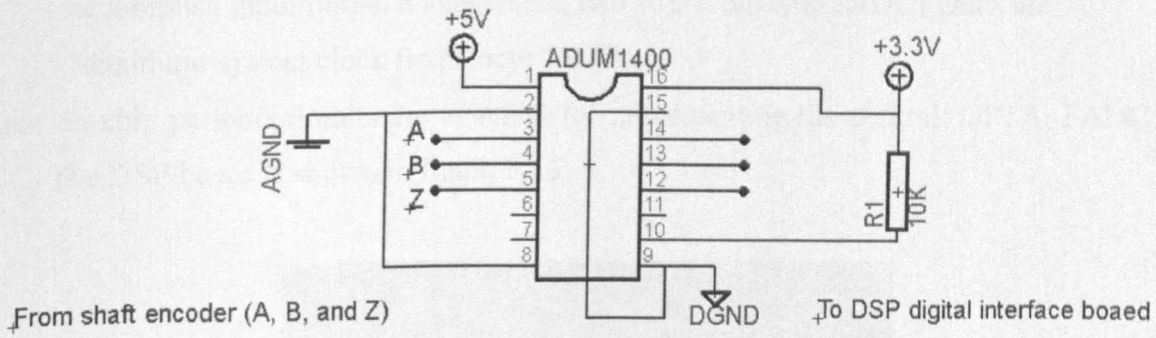


Figure F.12: Speed measurement circuit diagram.

vii. DSP board

The DSP unit is considered as the core of the control system. It is an embedded controller used in changing the control strategy during the practical evaluation. It should have some features as flexibility, processor speed, available storage memory, easy for programming and interface ability. The control scheme in the test rig is implemented using DSP type TriCore ™ TC1796 from Infineon. The DSP generates the switching pattern driving the switches of the inverter according to the software algorithm of the proposed system. The

Infineon TriCore ™ TC1796 has 32-Bit floating point microcontroller which can operate with a maximum CPU clock frequency of 150MHz. The main features of this DSP are:

- 32-Bit CPU with floating point unit and 4 Gbyte unified data, program, and I/O address space
- 16/32-bit high-efficiency instruction set
- Programmable external bus interface
- Integrated on-chip memories (programs in this work are run in the 48Kbyte Scratch-Pad RAM, which provides high accessibility.)
- Interrupt system with 181 service request node and 256 interrupt priority levels
- Peripheral control processor
- DMA controller with 16 independent DMA channels
- Parallel I/O ports with 127 digital General-Purpose I/O port lines
- On-chip peripheral units such as two General Purpose Timer Arrays (GPTA) to accomplish input/output management, two A/D Converter (ADC) units, etc
- Maximum system clock frequency: 75MHz

Three on-chip peripheral units are essential for implementing the control: GPTA, FADC and ASC. The DSP board is shown in figure F.13

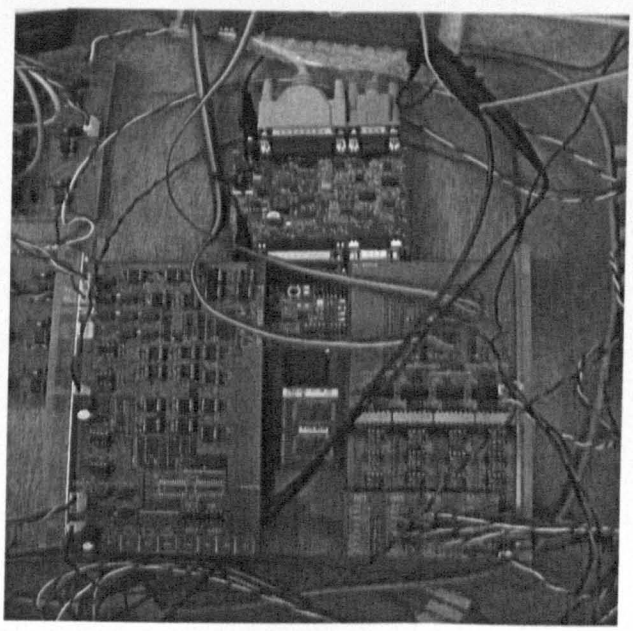


Figure F.13: DSP board.

viii. Analogue interface board

The main task of this board is to isolate the DSP from all the input analogue signals, from the voltage and current transducer boards. Also, the analogue interface board provides more amplitude tuning and protection to the A/D channels of the DSP to the 3.3 V limit. The analogue interface board and its schematic diagram are shown in figures F.14 and F.15 respectively.

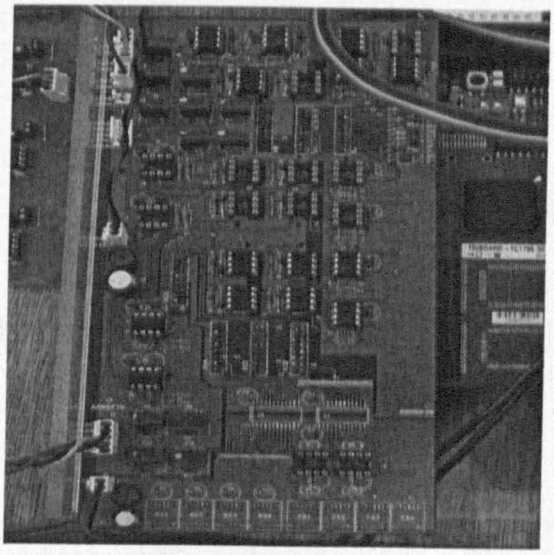


Figure F.14: Analogue interface board.

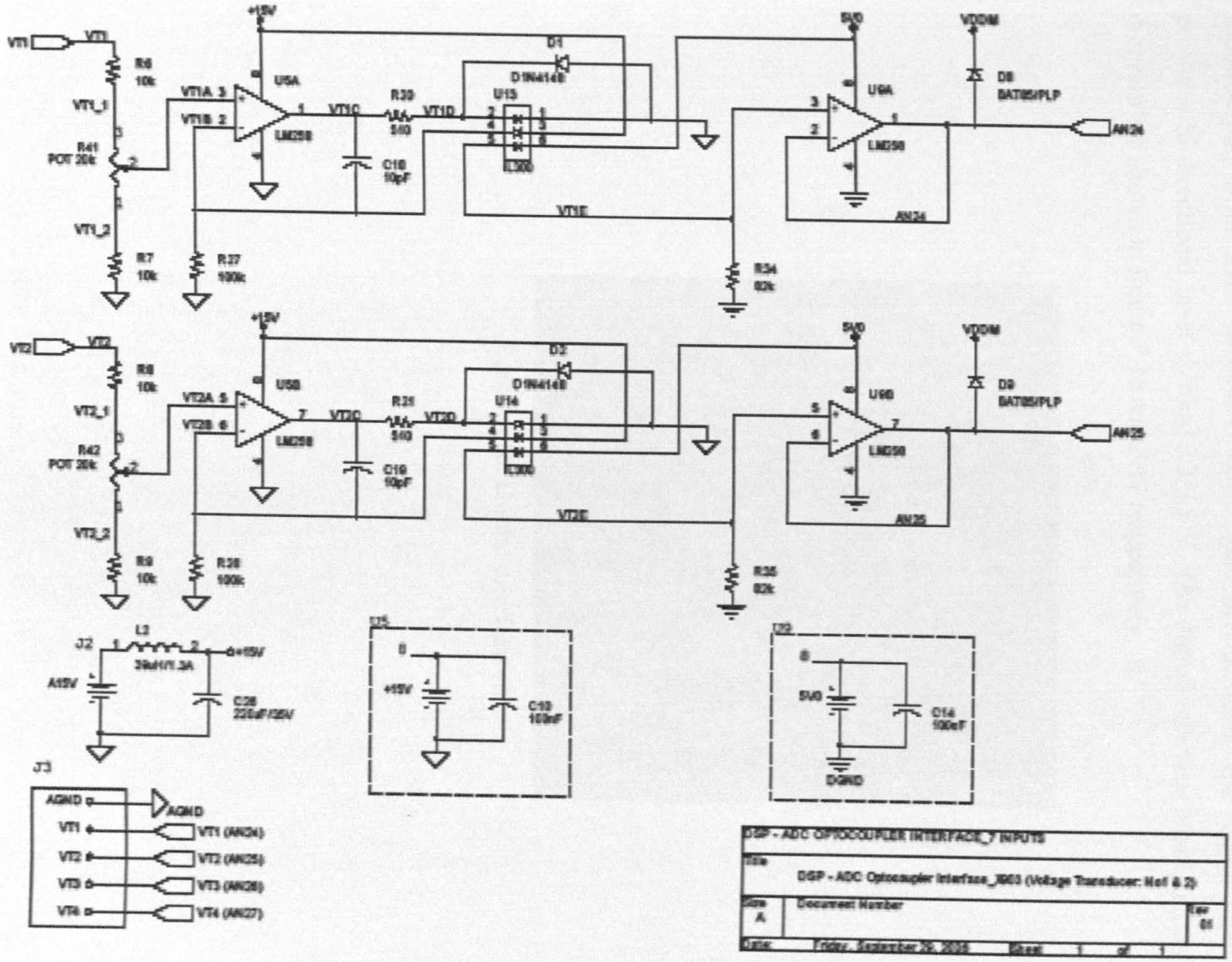


Figure F.15: Analogue interface circuit diagram.
[sample: 2 channel]

x. Digital interface board

The main task of this board is to isolate the DSP from all the digital signals input/output, from shaft encoder/to IGBT gate drives. Also, the digital interface board provides bi-directional level shifting 3.3/5.5 V. The digital interface board and its schematic diagram are shown in figure F.16 and F.17 respectively.

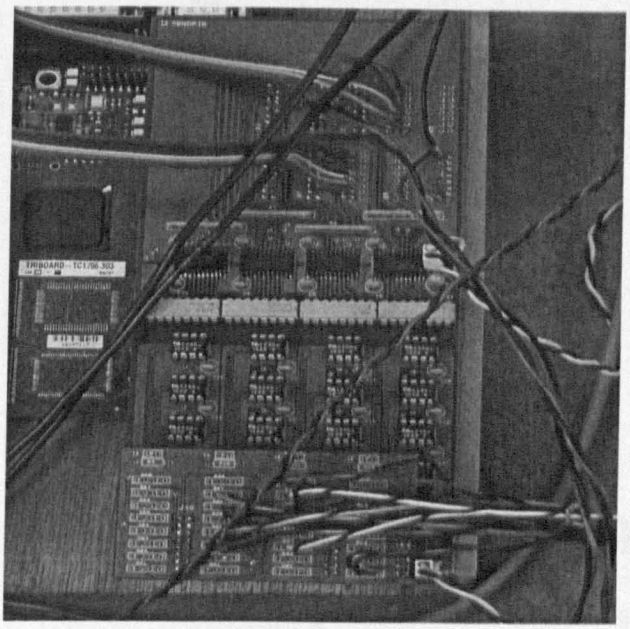


Figure F.16: Digital interface board.

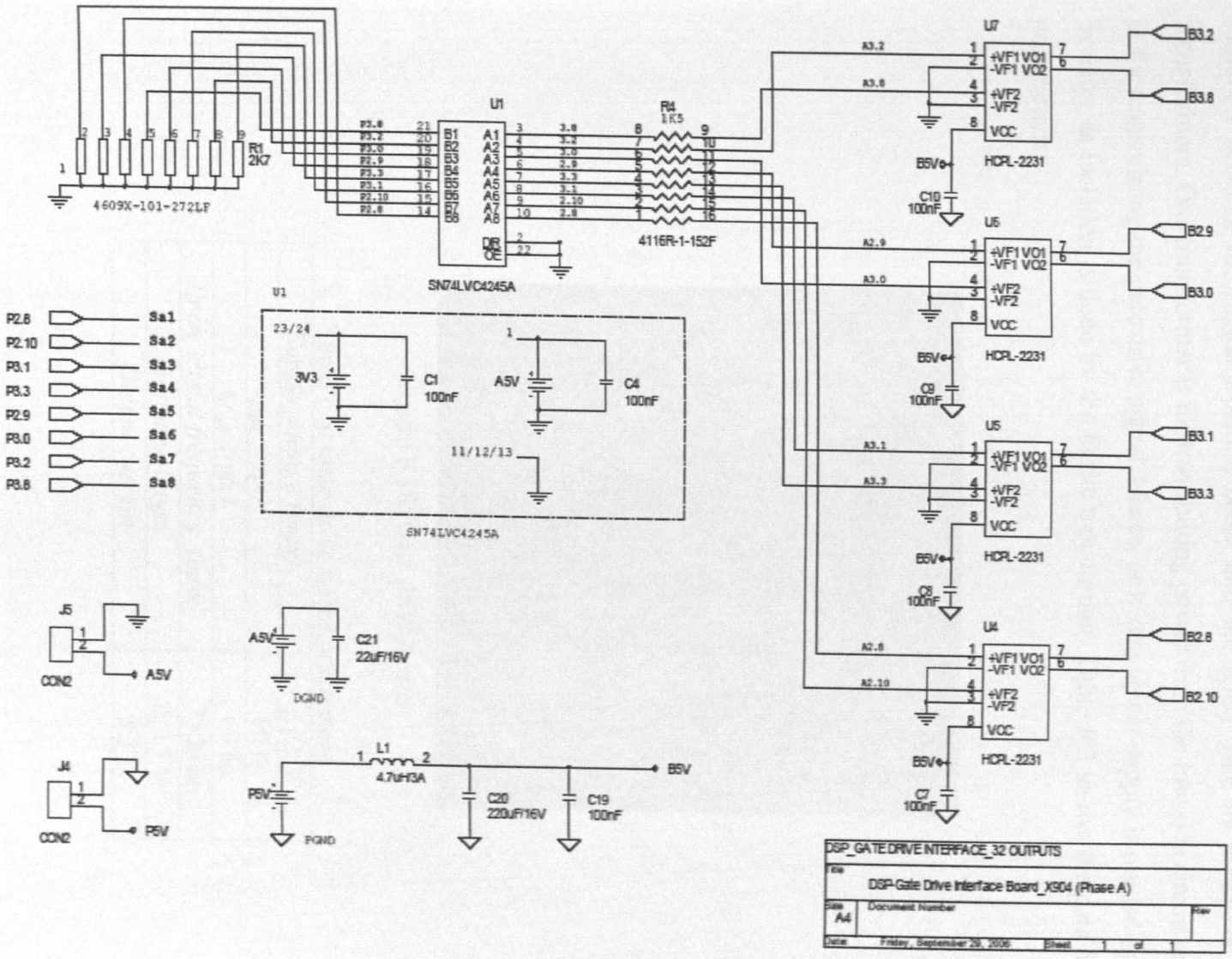


Figure F.17: Digital interface circuit diagram.
[sample: 2 channel]

xi. Gate drive board

The gate drive circuit used in the test rig is shown in figure F.18. It provides extra isolation between the digital isolation board and the IGBT gate by means of two ferrite transformers. One transformer is for transmitting power from the low side circuit and the other is for transmitting the gate drive signal. Hence, only one power supply is needed for the whole inverter as isolation is done by the ferrite transformer. Table F.3 shows the gate drive circuit parameters.

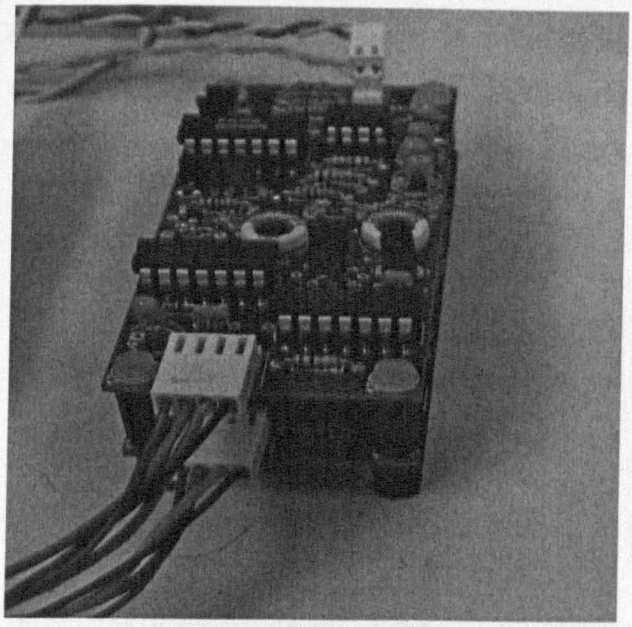


Figure F.18: Gate drive board.

Table F.3: Gate drive board parameters

Supply voltage (max)	5.25 V
$t_{d\,on}$ *(typ.)*	60 ns
$t_{d\,off}$ *(typ.)*	60 ns
Drive signal frequency (max)	75 kHz
Output voltages	0, 15 V
Output current	±3 A

F.2 Test rigs non-common blocks

In these subsections, the non-common blocks of the two test rigs are illustrated in details.

i. DC supply

The nature of the DC link source is different in the two test rigs. In the VSI based drive system, the DC supply is a constant voltage DC source, tuned at 300 V in the used experiments, as shown in figure F.19. In CSI based drive system, the DC source is a controlled current source. In the second, the same DC source used in the first test rig is reused with mode changing. The used DC supply can work in modes, voltage or current source. The DSP calculates the DC-link current command and send it as an ASCI code to the DC source using asynchronous serial communication protocol. As shown in figure F.20.

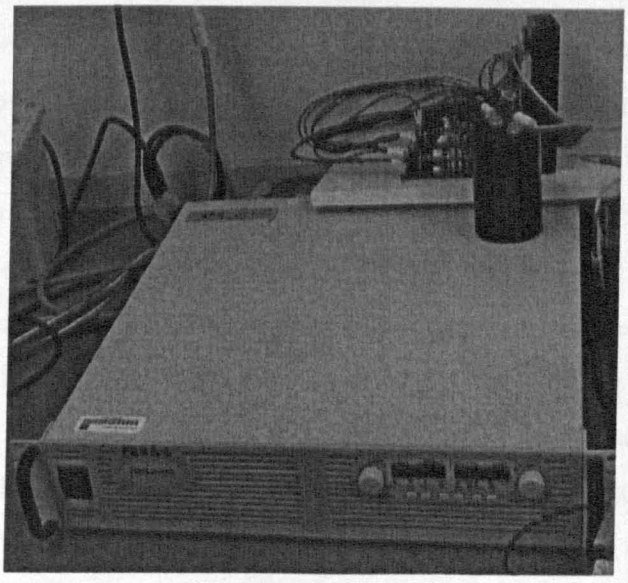


Figure F.19: DC supply for VSI based drive system (constant voltage source).

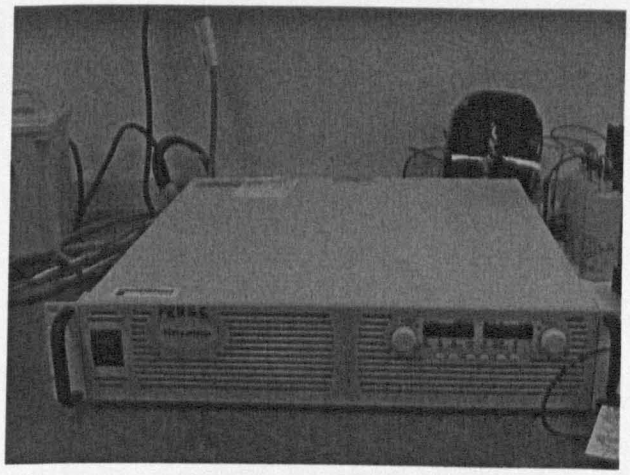


Figure F.20: DC supply for CSI based drive system (controlled current source).

ii. DC-link filter

As the nature of the DC supply is different between the two test rigs, the DC-link filter is also different. For the VSI drive system, the filter is a 2200 μF capacitor to hold the DC-link voltage constant as shown in figure F.21 while for the CSI drive, an inductance of 100 mH is used to achieve the required smoothing of the DC-link current as shown on figure F.22. Note that the DC-link inductance is designed to avoid saturation. Two methods can be used. First, utilization of an air core with the disadvantage of a large size. Second, use two C-cores with a preserved air gap between them to increase the saturation level. The second method is used in this thesis. The air gap is preserved using two paper sheets between the two cores. Note that as the air gap increases, the saturation level increases and the inductance decreases so a compromise is neede. The used inductance has a constant value of 100 mH up to a 3 A DC-link current.

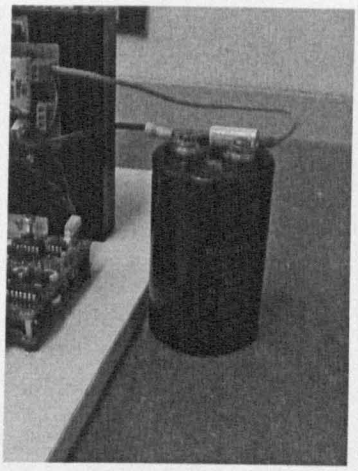


Figure F.21: DC-link filter for VSI based drive system.

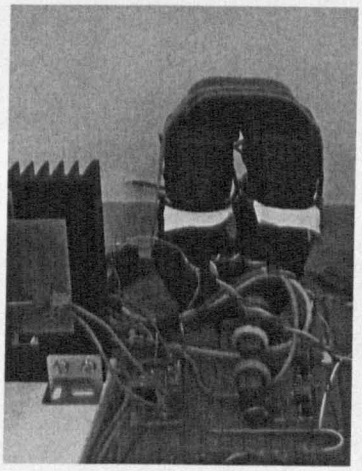


Figure F.22: DC-link filter for CSI based drive system.

iii. Inverter topology

The VSI inverter consists of six IGBTs with anti-parallel diodes mounted on a heat sink as shown in figure F.23. The CSI based inverter has an extra six series fast recovery diodes. CSI is shown in figure F.24. Table F.4 states the semiconductor types used in each inverter.

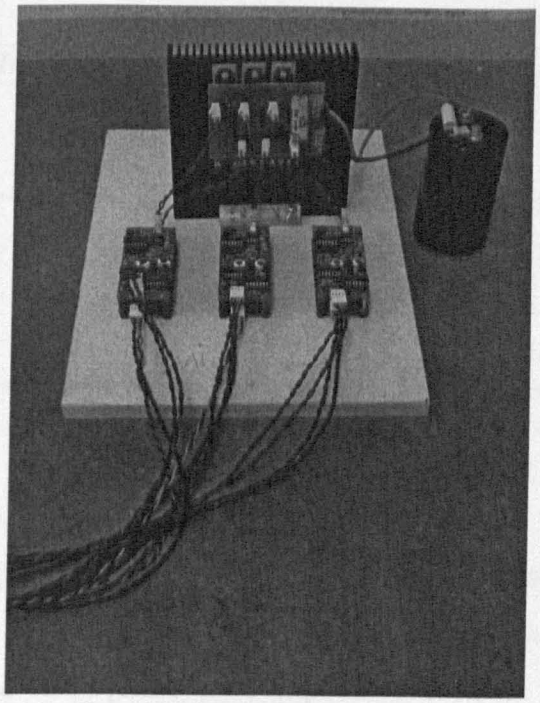


Figure F.23: VSI bridge.

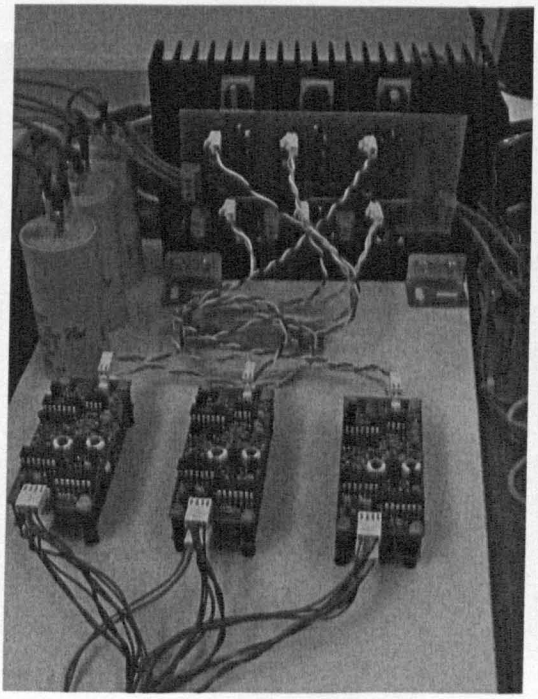


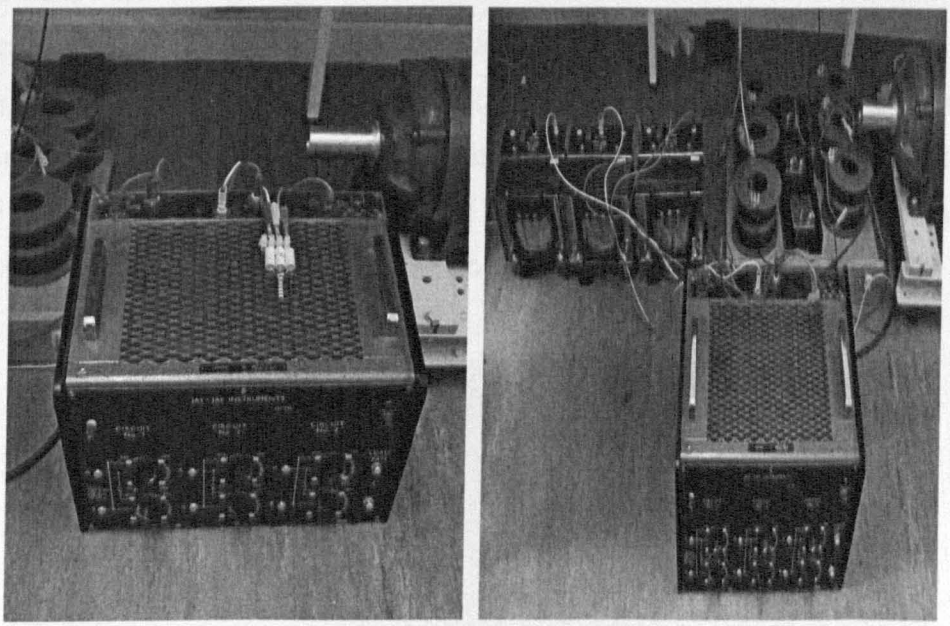
Figure F.24: CSI bridge.

Table F.4: VSI/CSI semiconductors

Inverter	*Semiconductor*	*Part Number*
VSI	IGBT plus anti-parallel diode	FGA15N120
CSI	IGBT plus anti-parallel diode	FGA15N120
	Series fast recovery diode	DSEI130-10A

iv. Output filter

For the VSI based, two surge filter networks are studies. First, motor terminal *RC* filter. Second, inverter output *RLC* filter. The two filters' parameters are listed in Appendix E. Figure F.25 shows the two filter networks. For the CSI drive system, sinusoidal voltage output is created by means of a three-phase pure capacitive filter at the inverter output. The capacitance used for this filter is 25 μF. Figure F.26 shows the CSI capacitive filter.



(a) (b)

Figure F.25: VSI filter networks.
(a) motor terminal *RC* filter and (b) inverter output *RLC* filter.

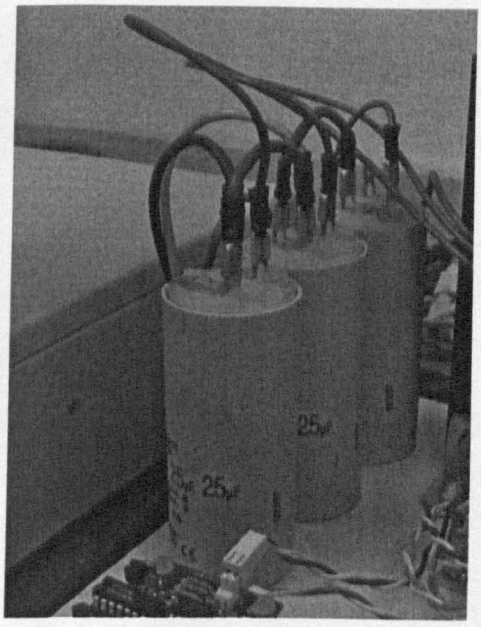


Figure F.26: CSI capacitive filter.

iv. Mapping circuit

In order to adapt the CSI gating signals on-line from the VSI PWM technique, a mapping circuit is utilized. For circuit reduction, part of the mapping circuit is converted to software code while the rest is implemented using digital ICs. As shown in figure F.27, the hardware realised part of the mapping circuit receives nine signals from the DSP and output six signals to the gate drive circuits. Figures F.28 and F.29 show the schematic of the mapping circuit with grey shading, representing the software implemented parts.

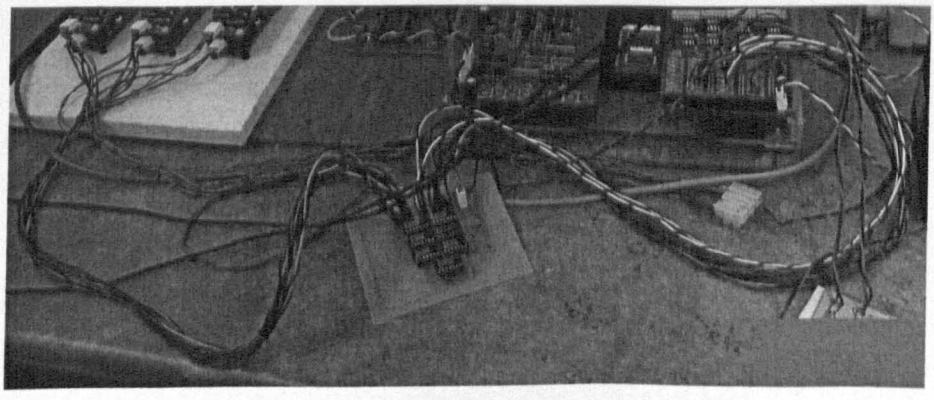


Figure F.27: Mapping circuit board.

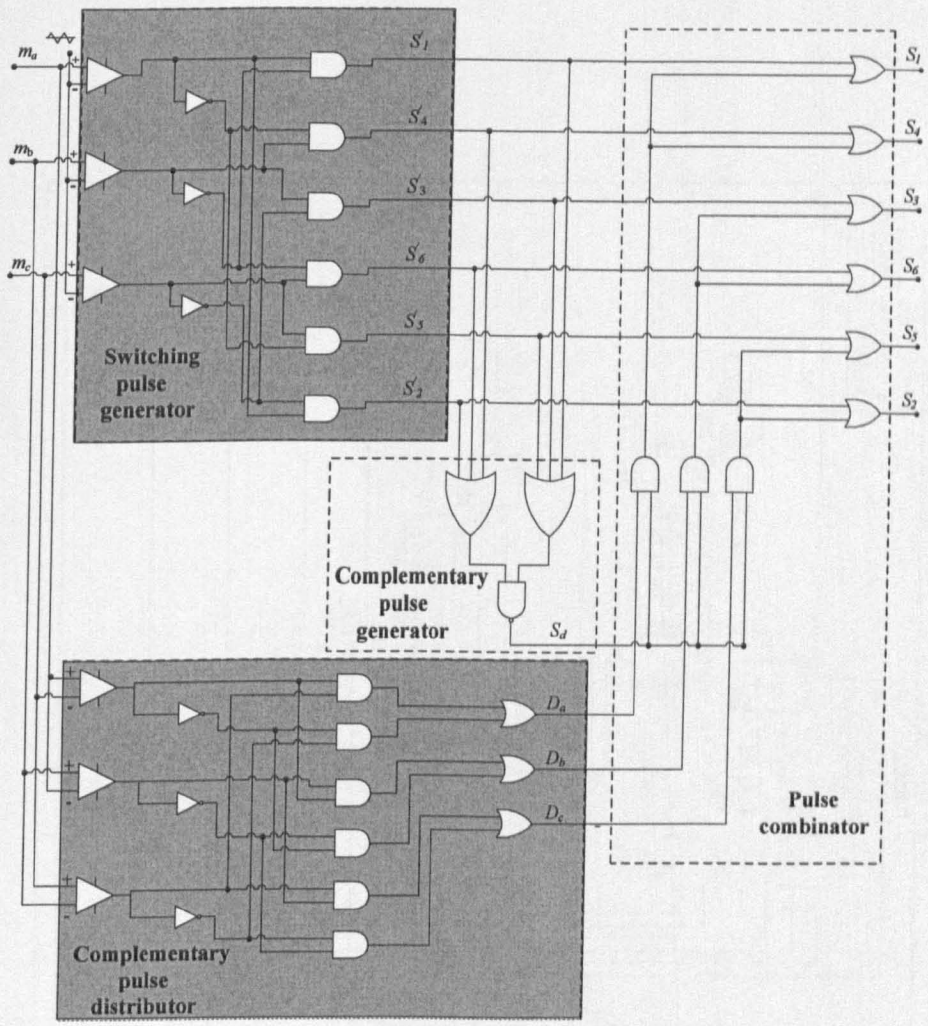


Figure F.28: Mapping circuit schematics with grey shaded parts are software implemented.

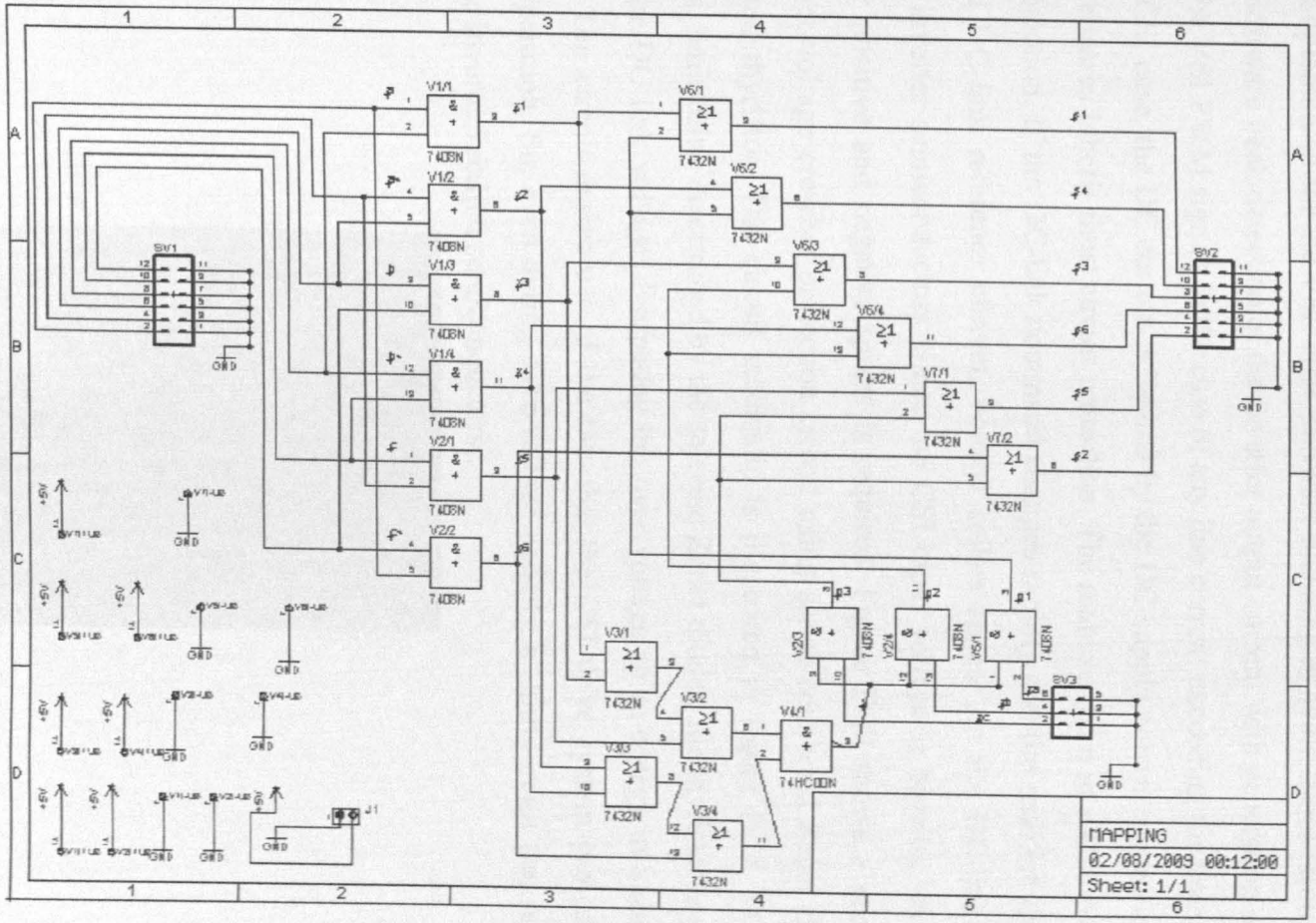


Figure F.29: Mapping circuit hardware schematics.

v. Protection scheme

For the VSI, since the voltage is constant and determined by the DC link source, VSI protection is mainly for the inverter current. In the implemented test rig, two protection schemes are implemented for the VSI. First, software blanking to avoid shoot-through on each leg. Second, software peak detection of the inverter output current with generation of a disable signal to all the VSI PWM signals in the case of any line current exceeding the threshold limit. While in the CSI case, the DC current is limited by the DC supply current controller as a CSI drive system ensures inherit short circuit protection. The main concern in a CSI drive system is voltage protection. If the DC-link command changes rapidly and the rectifier side follows the command DC-link reference current, voltage spikes appear on the DC-link side thus affecting the inverter semiconductors. Since the CSI input voltage is bi-polar, over-voltage protection for positive and negative spikes is required. Figure F.30 shows a proposed bi-directional over-voltage crowbar protection circuit using series connected Zener diodes and shunt connected thyristor. The circuit schematic is illustrated in figure F.31. When over-voltage occurs, limit being determined by the selected Zener diodes, the thyristor is gated thus short circuit the DC link voltage, dissipating the over-voltage spike energy in a short circuit current form. The circuit makes use of the fact that the CSI drive system provides output short-circuit operation. So, even during over-voltage periods, a short-circuit that occurs will not damage the inverter/rectifier semiconductors.

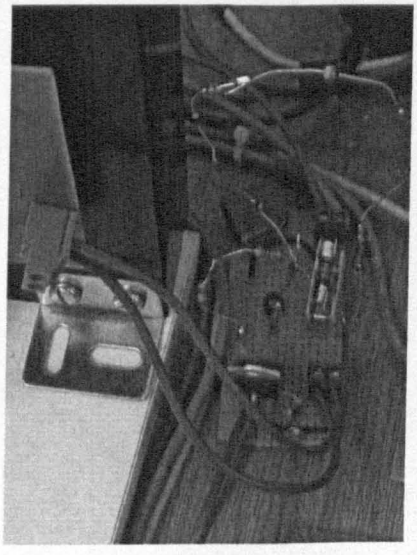


Figure F.30: CSI crow-bar circuit.

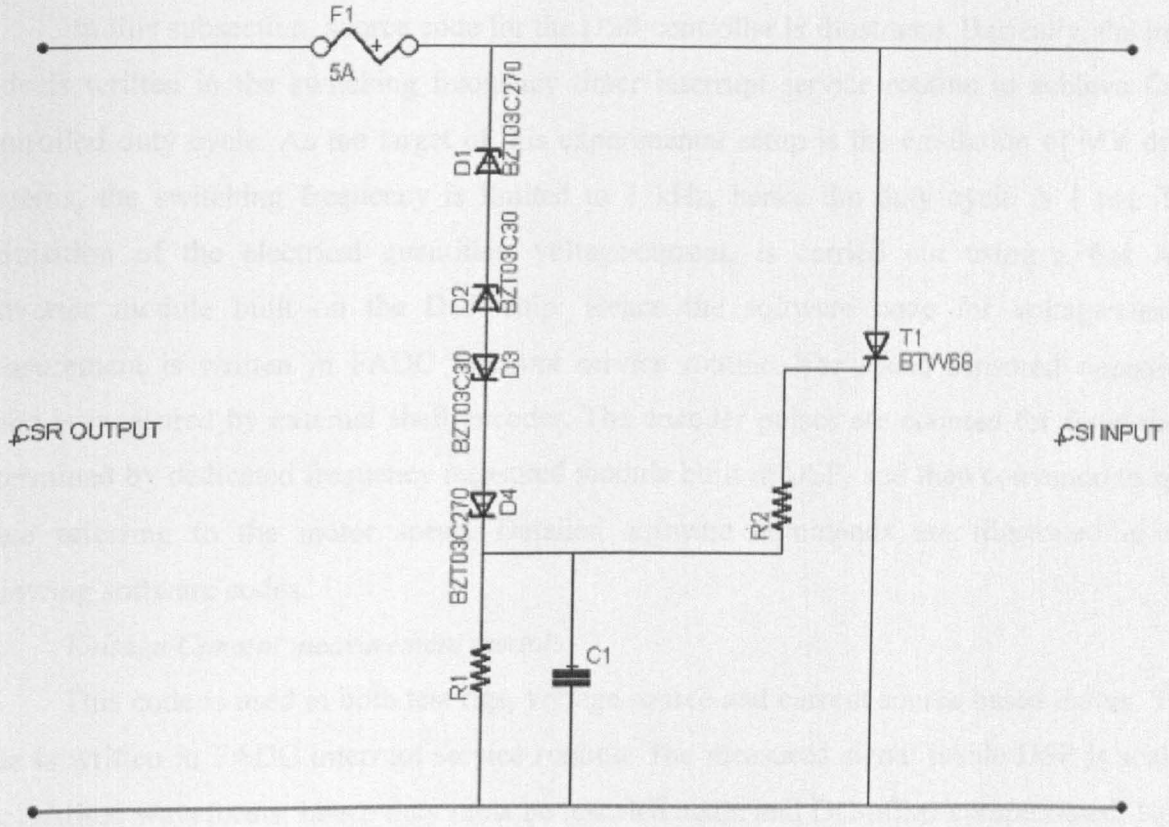


Figure F.31: CSI crow-bar circuit schematic.

F.3 Software code

In this subsection, source code for the DSP controller is illustrated. Basically, the main code is written in the switching frequency timer interrupt service routine to achieve fixed controlled duty cycle. As the target of this experimental setup is the emulation of MV drive systems, the switching frequency is limited to 1 kHz, hence the duty cycle is 1 ms. The acquisition of the electrical quantities, voltage/current, is carried out using a fast A/D converter module built on the DSP chip. Hence the software code for voltage/current measurement is written in FADC interrupt service routine. For speed sensored operation, speed is measured by external shaft encoder. The encoder pulses are counted for fixed time, determined by dedicated frequency measured module built in DSP, and then converted to rpm value referring to the motor speed. Detailed software commands are illustrated in the following software codes.

i. Voltage/Current measurement module

This code is used in both test rigs, voltage source and current source based drives. The code is written in FADC interrupt service routine. The measured signal inside DSP is scaled level shifted waveforms, hence they must be rescaled again and DC-offset compensated. Note that the DC-offset of A/D channels are not the same and must be determined separately.

```
//******************** voltage/current measurement ********************

//general formula for A/D signal acquisition:
//measured signal=
//(overall gain)*((3.3/1023)*(FADC_vGetChannelConversionResult(x))-
channel offset)


// USER CODE BEGIN (SRN0,0)

// USER CODE END

void INTERRUPT (FADC_SRN0INT) FADC_viSRN0(void)
{
  // USER CODE BEGIN (SRN0,1)

  // USER CODE END

  if(FADC_CRSR & FADC_CRSR_IRQ0)
  {
    // USER CODE BEGIN (SRN0,2)
```

```
va=(-1)*211.6*((3.3/1023)*(FADC_vGetChannelConversionResult(0))-
1.464);

    // USER CODE END

    FADC_FMR |= FADC_FMR_RIRQ0;  // reset request flag
  }

  if(FADC_CRSR & FADC_CRSR_IRQ1)
  {
    // USER CODE BEGIN (SRN0,3)

vc=(-1)*(-211.6)*((3.3/1023)*(FADC_vGetChannelConversionResult(1))-
1.787);

    // USER CODE END

    FADC_FMR |= FADC_FMR_RIRQ1;  // reset request flag
  }

  if(FADC_CRSR & FADC_CRSR_IRQ2)
  {
    // USER CODE BEGIN (SRN0,4)

ia=(2*1.4)*((6.53*sqrt(2))/3)*(((3.3/1023)*(FADC_vGetChannelConversio
nResult(2)))-1.49);

    // USER CODE END

    FADC_FMR |= FADC_FMR_RIRQ2;  // reset request flag
  }

  if(FADC_CRSR & FADC_CRSR_IRQ3)
  {
    // USER CODE BEGIN (SRN0,5)

ic=(2*1.4)*((6.53*sqrt(2))/3)*(((3.3/1023)*(FADC_vGetChannelConversio
nResult(3)))-1.5);

    // USER CODE END

    FADC_FMR |= FADC_FMR_RIRQ3;  // reset request flag
  }

  // USER CODE BEGIN (SRN0,8)
  // USER CODE END

} //  End of function FADC_viSRN0
```

ii. Speed measurement module

This code is used in both test rigs, voltage source and current source based drives. The code is written in GPTA interrupt service routine. A frequency measurement module built in DSP, DCM capture unit, is used to count the number of pulses, from shaft encoder, for a fixed period. Hence, with the knowledge of the shaft encoder number of pulses per revolution, the motor rpm can be calculated. The shaft encoder pulses are connected to pin P3.4. The shaft encoder pulses may have jitters which cause DCM unit to calculate unexpected number of pulses results in high incorrect motor speed. In order to avoid this, low pass filtering of the calculated motor speed limits on its peak value.

```
//****************************** speed measurement ******************************

void INTERRUPT (GPTA0_SRN0INT) GPTA0_viSRN0(void)
{
  // USER CODE BEGIN (SRN0,2)
  // USER CODE END

  GPTA0_SRSC0 = 0x00000001;  //  reset DCM0 rising edge service request bit

  //  DCM0 event (= rising edge of P3.4)

  // USER CODE BEGIN (SRN0,3)

//read DCM capture register to calculate counted pulse and calculate motor
//speed,
speed_rpm=(60*DCM_FREQUENCY_HZ)/(Encoder_pulses_per_rev*DCM_counted_pulses)


       speed_count=GPTA0_uwGetDCMCapture(GPTA0_DCM,0);
       speed_unf= 2341487.5/speed_count;

//speed calculation limiter


       if(speed_unf>1000)
       {
       speed_unf=speed_old;
       }
//low pass filter for measured speed to avoid unexpected values due to
//jitter effect of the measured pulses
      speed_new=(0.995*speed_old)+(0.005*speed_unf);
      speed_old=speed_new;

  // USER CODE END
} //  End of function GPTA0_viSRN0
```

iii. Vector control VSI based drive

This code is used in VSI test rig. The code is written in GPTA interrupt service routine. This code relies on the measured values of the motor currents and rotor speed from the previously mentioned software modules and generate six PWM signals for VSI. This code is used for VSI based drive and 1 km feeder with currents and speed measured from the motor side.

```
//***************************** VSI BASED DRIVE ******************************

void INTERRUPT (GPTA0_SRN22INT) GPTA0_viSRN22(void)
{
  // USER CODE BEGIN (SRN22,2)

  // USER CODE END

  if(GPTA0_SRSS2_LTC01)        //  LTC1 event (= compare with last timer)
  {
    GPTA0_SRSC2 = 0x00000002; //  reset LTC1 service request bit

    // USER CODE BEGIN (SRN22,4)

//speed error calculator

       speed_error_new=n_ref-speed_new;

//speed PI controller

      torque_ref_new=torque_ref_old+(kp_speed*(speed_error_new-
      speed_error_old))+(ki_speed*t_sample*speed_error_new);
      torque_ref_old=torque_ref_new;
      speed_error_old=speed_error_new;
      torque_ref=torque_ref_new;

//torque limiter

      if (torque_ref>torque_max)
      {
      torque_ref=torque_max;
      }
      if (torque_ref<torque_min)
      {
      torque_ref=torque_min;
      }

// vector control block

      lamda_dr=lm*i_ds_ref;
      i_qs_ref=(2.0*lr*torque_ref)/(3.0*p*lm*lamda_dr);
```

```
w_slip=(rr*lm*i_qs_ref)/(lr*lamda_dr);
w_m=p*speed_new*pi/30.0;
w_e=w_m+w_slip;
```

//calculate new theta

```
theta_e_new+=(w_e*t_sample);
```

//check overflow of theta

```
if (theta_e_new>=6.28)
{
theta_e_new=0;
}
```

//abc to dq_e transformation for motor currents

```
ib=(-1)*(ia+ic);
i_ds_unf=(2.0/3.0)*(((ia)*sin(theta_e_new))+((ib)*sin(theta_e_new-
(2*pi/3)))+((ic)*sin(theta_e_new+(2*pi/3))));
i_qs_unf=(2.0/3.0)*(((ia)*cos(theta_e_new))+((ib)*cos(theta_e_new-
(2*pi/3)))+((ic)*cos(theta_e_new+(2*pi/3))));
```

//low pass filter for motor dq_e currents

```
i_ds_act=(0.83*i_ds_old)+(0.16*i_ds_unf);
i_qs_act=(0.83*i_qs_old)+(0.16*i_qs_unf);
i_ds_old=i_ds_act;
i_qs_old=i_qs_act;
```

//ds_e and qs_e motor current error calculators

```
ds_error_new=i_ds_ref-i_ds_act;
qs_error_new=i_qs_ref-i_qs_act;
```

//md PI controller

```
md_ref_new=md_ref_old+
(kp_md*(ds_error_new-ds_error_old))+(ki_md*t_sample*ds_error_new);
md_ref_old=md_ref_new;
ds_error_old=ds_error_new;
```

//mq PI controller

```
mq_ref_new=mq_ref_old+
(kp_mq*(qs_error_new-qs_error_old))+(ki_mq*t_sample*qs_error_new);
mq_ref_old=mq_ref_new;
qs_error_old=qs_error_new;
```

//ma mb mc calculator dq_e-abc transformation

```
ma=((md_ref_new*(sin(theta_e_new)))+(mq_ref_new*(cos(theta_e_new))));
mb=((md_ref_new*(sin(theta_e_new-(2*pi/3))))+
(mq_ref_new*(cos(theta_e_new-(2*pi/3)))));
```

```
mc=((md_ref_new*(sin(theta_e_new+(2*pi/3))))+
(mq_ref_new*(cos(theta_e_new+(2*pi/3)))));
```

```
//ma limiter

                    if (ma>0.99)
                    {
                    ma=0.99;
                    }
                    if (ma<-0.99)
                    {
                    ma=-0.99;
                    }

//mb limiter

                    if (mb>0.99)
                    {
                    mb=0.99;
                    }
                    if (mb<-0.99)
                    {
                    mb=-0.99;
                    }
//mc limiter

                    if (mc>0.99)
                    {
                    mc=0.99;
                    }
                    if (mc<-0.99)
                    {
                    mc=-0.99;
                    }

//timer reload values calculation phase a

      t3 = 4998-(0.5*(ma+1)*(4998));
      t4 = 4998+(0.5*(ma+1)*(4998));
      t5 = t3-dead_time_count;//-dead_time_count;
      t6 = t4+dead_time_count;//+dead_time_count;

//timer reload values calculation phase b

      t7 = 4998-(0.5*(mb+1)*(4998));
      t8 = 4998+(0.5*(mb+1)*(4998));
      t9 = t7-dead_time_count;//-dead_time_count;
      t10 = t8+dead_time_count;//+dead_time_count;

//timer reload values calculation phase c
      t11 = 4998-(0.5*(mc+1)*(4998));
      t12 = 4998+(0.5*(mc+1)*(4998));
      t13 = t11-dead_time_count;//-dead_time_count;
      t14 = t12+dead_time_count;//+dead_time_count;
```

```
//update phase a at mid

       GPTA0_LTCXR04=t4;
       GPTA0_LTCXR06=t6;

//update phase b at mid

       GPTA0_LTCXR08=t8;
       GPTA0_LTCXR10=t10;

//update phase c at mid

       GPTA0_LTCXR12=t12;
       GPTA0_LTCXR14=t14;

     // USER CODE END

   }
   if(GPTA0_SRSS2_LTC02)        //  LTC2 event (= compare with last timer)
   {
     GPTA0_SRSC2 = 0x00000004; //  reset LTC2 service request bit

     // USER CODE BEGIN (SRN22,5)

//update phase a at end

      GPTA0_LTCXR03=t3;
      GPTA0_LTCXR05=t5;

//update phase b at end

      GPTA0_LTCXR07=t7;
      GPTA0_LTCXR09=t9;

//update phase c at end

      GPTA0_LTCXR11=t11;
      GPTA0_LTCXR13=t13;

     // USER CODE END

   }
   // USER CODE BEGIN (SRN22,8)

   // USER CODE END


} //  End of function GPTA0_viSRN22
```

iv. Vector control CSI based drive

This code is used in CSI test rig. The code is written in GPTA interrupt service routine. This code relies on the measured values of the motor currents and rotor speed from the previously mention software modules and generate six PWM signals, three signals for CSI mapping circuit, and DC-link reference (in the form of serial data command to the current source DC-link supply). This code is used for CSI based drive and 1 km feeder with currents and speed measured from the motor side. The code presented in this subsection refers to the proposed indirect vector controlled PWM CSI based drive.

```
//****************************** CSI BASED DRIVE ******************************

void INTERRUPT (GPTA0_SRN22INT) GPTA0_viSRN22(void)
{

  // USER CODE BEGIN (SRN22,2)

  // USER CODE END

  if(GPTA0_SRSS2_LTC01)        //  LTC1 event (= compare with last timer)
  {
    GPTA0_SRSC2 = 0x00000002; //  reset LTC1 service request bit

    // USER CODE BEGIN (SRN22,4)

//speed error calculator

       speed_error_new=n_ref-speed_new;

//speed PI controller

      torque_ref_new=torque_ref_old+(kp_speed*(speed_error_new-
      speed_error_old))+(ki_speed*t_sample*speed_error_new);
      torque_ref_old=torque_ref_new;
      speed_error_old=speed_error_new;
      torque_ref=torque_ref_new;

//torque limiter

      if (torque_ref>torque_max)
      {
      torque_ref=torque_max;
      }
      if (torque_ref<torque_min)
      {
      torque_ref=torque_min;
      }
```

```
// vector control block

        lamda_dr=lm*i_ds_ref;
        i_qs_ref=(2.0*lr*torque_ref)/(3.0*p*lm*lamda_dr);
        w_slip=(rr*lm*i_qs_ref)/(lr*lamda_dr);
        w_m=p*speed_new*pi/30.0;
        w_e=w_m+w_slip;

//calculate new theta

        theta_e_new+=(w_e*t_sample);

//check overflow of theta

                    if (theta_e_new>=6.28)
                    {
                    theta_e_new=0;
                    }

//abc to dq_e transformation for motor currents

        ib=(-1)*(ia+ic);
        i_ds_unf=(2.0/3.0)*(((ia)*sin(theta_e_new))+((ib)*sin(theta_e_new-
        (2*pi/3)))+((ic)*sin(theta_e_new+(2*pi/3))));
        i_qs_unf=(2.0/3.0)*(((ia)*cos(theta_e_new))+((ib)*cos(theta_e_new-
        (2*pi/3)))+((ic)*cos(theta_e_new+(2*pi/3))));

//low pass filter for motor dq_e currents

        i_ds_act=(0.83*i_ds_old)+(0.16*i_ds_unf);
        i_qs_act=(0.83*i_qs_old)+(0.16*i_qs_unf);
        i_ds_old=i_ds_act;
        i_qs_old=i_qs_act;

//md PI controller

        ds_error_new=1.3-i_ds_act;
        md_ref_new=md_ref_old+(kp_md*(ds_error_new-
        ds_error_old))+(ki_md*t_sample*ds_error_new);
        md_ref_old=md_ref_new;
        ds_error_old=ds_error_new;

//mq PI controller

        qs_error_new=(2.0*lr*torque_ref)/(3.0*p*lm*lamda_dr)-i_qs_act;
        mq_ref_new=mq_ref_old+(kp_mq*(qs_error_new-
        qs_error_old))+(ki_mq*t_sample*qs_error_new);
        mq_ref_old=mq_ref_new;
        qs_error_old=qs_error_new;

//mdq limiter

        if(md_ref_new>=1)
        {
```

```
md_ref_new=1;
md_ref_old=1;
}
if(md_ref_new<=-1)
{
md_ref_new=-1;
md_ref_old=-1;
}

if(mq_ref_new>=1)
{
mq_ref_new=1;
mq_ref_old=1;
}
if(mq_ref_new<=-1)
{
mq_ref_new=-1;
mq_ref_old=-1;
}
```

//unit vectors generated

```
md_ref_new=
(md_ref_old)/(sqrt((md_ref_old*md_ref_old)+(mq_ref_old*mq_ref_old)));
mq_ref_new=
(mq_ref_old)/(sqrt((md_ref_old*md_ref_old)+(mq_ref_old*mq_ref_old)));
```

//ma mb mc calculator dq_e-abc transformation

```
ma=0.99*((md_ref_new*(sin(theta_e_new)))
   +(mq_ref_new*(cos(theta_e_new))));
mb=0.99*((md_ref_new*(sin(theta_e_new-(2*pi/3))))+
   (mq_ref_new*(cos(theta_e_new-(2*pi/3)))));
mc=0.99*((md_ref_new*(sin(theta_e_new+(2*pi/3))))+
   (mq_ref_new*(cos(theta_e_new+(2*pi/3)))));
```

//ma limiter

```
if (ma>0.99)
{
ma=0.99;
}
if (ma<-0.99)
{
ma=-0.99;
}
```

//mb limiter

```
if (mb>0.99)
{
mb=0.99;
}
if (mb<-0.99)
```

```
                    {
                    mb=-0.99;
                    }
```

//mc limiter

```
                    if (mc>0.99)
                    {
                    mc=0.99;
                    }
                    if (mc<-0.99)
                    {
                    mc=-0.99;
                    }
```

//mapping circuit

```
        if(ma>=mc)
        {
         fya=1;
        }
        if(ma<mc)
        {
         fya=0;
        }


        if(mb>=ma)
        {
         fyb=1;
        }
        if(mb<ma)
        {
         fyb=0;
        }


        if(mc>=mb)
        {
         fyc=1;
        }
        if(mc<mb)
        {
         fyc=0;
        }


        za=!(fya^fyc);
        zb=!(fyb^fya);
        zc=!(fyc^fyb);
```

```
        if(za==1)
        {
        IO_vSetPin(IO_P4_0);
        }
        if(za==0)
        {
        IO_vResetPin(IO_P4_0);
        }


        if(zb==1)
        {
        IO_vSetPin(IO_P4_1);
        }
        if(zb==0)
        {
        IO_vResetPin(IO_P4_1);
        }


        if(zc==1)
        {
        IO_vSetPin(IO_P4_2);
        }
        if(zc==0)
        {
        IO_vResetPin(IO_P4_2);
        }

//timer reload values calculation phase a

       t3 = 4998-(0.5*(ma+1)*(4998));
       t4 = 4998+(0.5*(ma+1)*(4998));
       t5 = t3-dead_time_count;//-dead_time_count;
       t6 = t4+dead_time_count;//+dead_time_count;

//timer reload values calculation phase b

       t7 = 4998-(0.5*(mb+1)*(4998));
       t8 = 4998+(0.5*(mb+1)*(4998));
       t9 = t7-dead_time_count;//-dead_time_count;
       t10 = t8+dead_time_count;//+dead_time_count;

//timer reload values calculation phase c

      t11 = 4998-(0.5*(mc+1)*(4998));
      t12 = 4998+(0.5*(mc+1)*(4998));
      t13 = t11-dead_time_count;//-dead_time_count;
      t14 = t12+dead_time_count;//+dead_time_count;
```

```
//update phase a at mid

      GPTA0_LTCXR04=t4;
      GPTA0_LTCXR06=t6;

//update phase b at mid

      GPTA0_LTCXR08=t8;
      GPTA0_LTCXR10=t10;

//update phase c at mid

      GPTA0_LTCXR12=t12;
      GPTA0_LTCXR14=t14;

//update dq_e total current reference based on ic (c= 25 µF) correction

       i_ds_ref=1.3-(w_e*0.000025*v_qs_act);
       i_qs_ref=(2.0*lr*torque_ref)/(3.0*p*lm*lamda_dr)+(w_e*0.000025*v_ds_act);

//DC link curent calculator (DC-link constant = 1.2)

     i_dc_ref=1.2*(sqrt((i_ds_ref*i_ds_ref)+(i_qs_ref*i_qs_ref)));

//DC link current limiter (Current is limited to 3 A)

                if (i_dc_ref >=3)
                {
                i_dc_ref =3;
                }

//send dc link current reference command to power supply over serial link

       ii=sprintf(str,"%f", i_dc_ref);
          switch (flag4)
          {
          case 1: ASC0_vSendData('P');
                        break;
          case 2: ASC0_vSendData('C');
                        break;
          case 3: ASC0_vSendData(' ');
                        break;
          case 4: ASC0_vSendData(str[0]);
                        break;
          case 5: ASC0_vSendData(str[1]);
                        break;
          case 6: ASC0_vSendData(str[2]);
                        break;
          case 7: ASC0_vSendData(str[3]);
                        break;
          case 8: ASC0_vSendData(13);
                        break;
          case 12:      flag4=1;
```

```
                        break;
        }

    // USER CODE END

  }
  if(GPTA0_SRSS2_LTC02)        //  LTC2 event (= compare with last timer)
  {
    GPTA0_SRSC2 = 0x00000004; //  reset LTC2 service request bit

    // USER CODE BEGIN (SRN22,5)

//update phase a at end

     GPTA0_LTCXR03=t3;
     GPTA0_LTCXR05=t5;

//update phase b at end

     GPTA0_LTCXR07=t7;
     GPTA0_LTCXR09=t9;

//update phase c at end

     GPTA0_LTCXR11=t11;
     GPTA0_LTCXR13=t13;

    // USER CODE END

  }
  // USER CODE BEGIN (SRN22,8)

  // USER CODE END


} //  End of function GPTA0_viSRN22
```

v. Speed estimation for 1 km feeder drive

This code can be used in the VSI or CSI test rig. The code is written in the GPTA interrupt service routine. This code relies on the measured values of the inverter voltages and currents from the previously mention software modules. The code first calculates the motor terminal voltage from the inverter output voltage and current as described in chapter seven, then the calculated motor voltage is used in the MRAS algorithm to estimate the motor speed. The speed estimation algorithm also performs the novel DC-offset eliminator, illustrated in chapter seven.

```
//***************************** Speed estimation ****************************

//***************************** Motor voltage calculator*********************


//abc to dq_s transformation for inverter voltages

vds_s_new=(2.0/3.0)*(((va)*sin(0))+((vb)*sin(0-(2*pi/3)))+((vc)*sin(0+(2*pi/3))));
vqs_s_new=(2.0/3.0)*(((va)*cos(0))+((vb)*cos(0-(2*pi/3)))+((vc)*cos(0+(2*pi/3))));

//abc to dq_s transformation for motor currents

ids_s_new=(2.0/3.0)*(((ia)*sin(0))+((ib)*sin(0-(2*pi/3)))+((ic)*sin(0+(2*pi/3))));
iqs_s_new=(2.0/3.0)*(((ia)*cos(0))+((ib)*cos(0-(2*pi/3)))+((ic)*cos(0+(2*pi/3))));

//estimation of fundamental motor voltage based on cable parameters and w_e

vds_s_motor=vds_s_new-(ids_s_new*22)-(ids_s_new*w_e*1.1e-3);
vqs_s_motor=vqs_s_new-(iqs_s_new*w_e*1.1e-3)-(iqs_s_new*22);

//dq_e to abc transformation of calculated motor terminal voltage

v_a_motor=((vds_s_motor*(sin(0)))+(vqs_s_motor*(cos(0))));
v_b_motor=((vds_s_motor*(sin(0-(2*pi/3))))+(vqs_s_motor*(cos(0-(2*pi/3)))));
v_c_motor=((vds_s_motor*(sin(0+(2*pi/3))))+(vqs_s_motor*(cos(0+(2*pi/3)))));

//***************************** MRAS speed estimation*********************

//stator model

//open loop integration for stator flux

lamda_ds_s_old+=((vds_s_motor-(ids_s_new*4.1))*t_sample);
lamda_qs_s_old+=((vqs_s_motor-(iqs_s_new*4.1))*t_sample);
```

```
//max min calculation of stator flux d component

if(lamda_ds_s_old>lamda_ds_s_max)
{
lamda_ds_s_max=lamda_ds_s_old;
}
if(lamda_ds_s_old<lamda_ds_s_min)
{
lamda_ds_s_min=lamda_ds_s_old;
}

//average calculation and offset elimination of stator flux d component every pi/2

if((theta_e_new==0)|(theta_e_new==3.14))
{
fake_d_new=(lamda_ds_s_min+lamda_ds_s_max)/2.0;
lamda_ds_s_old=lamda_ds_s_old-fake_d_new;
lamda_ds_s_max=-20;
lamda_ds_s_min=20;
}
lamda_ds_s_new=lamda_ds_s_old;

//max min calculation of stator flux q component

if(lamda_qs_s_old>lamda_qs_s_max)
{
lamda_qs_s_max=lamda_qs_s_old;
}
if(lamda_qs_s_old<lamda_qs_s_min)
{
lamda_qs_s_min=lamda_qs_s_old;
}

//average calculation and offset elimination of stator flux d component every pi/2

if((theta_e_new==0)|(theta_e_new==3.14))
{
fake_q_new=(lamda_qs_s_min+lamda_qs_s_max)/2.0;
lamda_qs_s_old=lamda_qs_s_old-fake_q_new;
lamda_qs_s_max=-20;
lamda_qs_s_min=20;
}
lamda_qs_s_new=lamda_qs_s_old;

//calculation of rotor flux dq components in s frame

lamda_dr_s=(lr/lm)*(lamda_ds_s_new-((lr*lr-lm*lm)*ids_s_new/lr));
lamda_qr_s=(lr/lm)*(lamda_qs_s_new-((lr*lr-lm*lm)*iqs_s_new/lr));

//dq_s to abc transformation of rotor flux

lamda_ar=((lamda_dr_s*(sin(0)))+(lamda_qr_s*(cos(0))));
lamda_br=((lamda_dr_s*(sin(0-(2*pi/3))))+(lamda_qr_s*(cos(0-(2*pi/3)))));
lamda_cr=((lamda_dr_s*(sin(0+(2*pi/3))))+(lamda_qr_s*(cos(0+(2*pi/3)))));
```

```
//abc-dq_e transformation for rotor flux

lamda_dr_e=(2.0/3.0)*(((lamda_ar)*sin(theta_e_new))+((lamda_br)*sin(theta_e_new-
(2*pi/3)))+((lamda_cr)*sin(theta_e_new+(2*pi/3))));
lamda_qr_e=(2.0/3.0)*(((lamda_ar)*cos(theta_e_new))+((lamda_br)*cos(theta_e_new-
(2*pi/3)))+((lamda_cr)*cos(theta_e_new+(2*pi/3))));

//low pass filter for rotor flux dq_e components

lamda_dr_e_new=(0.99*lamda_dr_e_old)+(0.01*lamda_dr_e);
lamda_qr_e_new=(0.99*lamda_qr_e_old)+(0.01*lamda_qr_e);
lamda_dr_e_old=lamda_dr_e_new;
lamda_qr_e_old=lamda_qr_e_new;

//dq_e to abc transformation of filtered rotor flux

lamda_ar_fil=((lamda_dr_e_new*(sin(theta_e_new)))+
(lamda_qr_e_new*(cos(theta_e_new))));
lamda_br_fil=((lamda_dr_e_new*(sin(theta_e_new-(2*pi/3))))+
(lamda_qr_e_new*(cos(theta_e_new-(2*pi/3)))));
lamda_cr_fil=((lamda_dr_e_new*(sin(theta_e_new+(2*pi/3))))+
(lamda_qr_e_new*(cos(theta_e_new+(2*pi/3)))));

//abc to dq_s transformation of filtered rotor flux

lamda_dr_s_fil=(2.0/3.0)*(((lamda_ar_fil)*sin(0))+
((lamda_br_fil)*sin(0-(2*pi/3)))+((lamda_cr_fil)*sin(0+(2*pi/3))));
lamda_qr_s_fil=(2.0/3.0)*(((lamda_ar_fil)*cos(0))+
((lamda_br_fil)*cos(0-(2*pi/3)))+((lamda_cr_fil)*cos(0+(2*pi/3))));

//rotor model

lamda_dr_s_r+=(((ids_s_new*rr*lm/lr)-(lamda_dr_s_r_old*rr/lr)-
(lamda_qr_s_r_old*w_m_est_unf))*0.001);
lamda_qr_s_r+=(((lamda_dr_s_r_old*w_m_est_unf)-(lamda_qr_s_r_old*rr/lr)+
(iqs_s_new*rr*lm/lr))*0.001);
lamda_dr_s_r_old=lamda_dr_s_r;
lamda_qr_s_r_old=lamda_qr_s_r;

//speed estimator

e_estimator_new=(lamda_dr_s_r*lamda_qr_s_fil)-(lamda_qr_s_r*lamda_dr_s_fil);
w_m_est_unf=w_m_est_old_unf+(kp_est*(e_estimator_new-e_estimator_old))+
(ki_est*t_sample*e_estimator_new);
w_m_est_old_unf=w_m_est_unf;
e_estimator_old=e_estimator_new;

//low pass filter for estimated speed

      w_m_est=(0.9*w_m_est_old)+(0.1*w_m_est_unf);
      w_m_est_old=w_m_est;
```

Appendix G: Author's Publications

1. Abdelsalam, A.K., Masoud, M.I., Finney, S.J., and Williams, B.W.

'Comparative Study of AC Side Passive and Active Filters for Medium Voltage PWM Current Source Rectifiers'

IET 4th Power Electronics, Machines and Drives Conference, PEMD 08, York, UK, April 2008, pp. 578 - 582.

Abstract– In this paper, a comparative study for both AC side passive and active filters for medium voltage PWM current source rectifiers which utilize selective harmonic elimination technique is introduced. Modeling, design and performance analysis of both power filters are given to improve the total harmonic distortion (THD) of the input current and ensure near unity power factor operation for the whole loading range. The topologies used are second order passive LC filter with damping resistor and shunt active power filter based on instantaneous active-reactive power theory (p-q method).

2. Abdelsalam, A.K., Masoud, M.I., Finney, S.J., and Williams, B.W.

'Losses Calculation for Medium Voltage PWM Current Source Rectifiers using Different Semiconductor Devices'

International Symposium on Power electronics, Electrical Drives, Automation and Motion, SPEEDAM 08, Ischia, Italy, June 2008, pp. 1356 - 1362.

Abstract-- In this paper, a comparison of losses and size for three semiconductor devices suitable for medium voltage (2.4 kV, 3.3 kV and 6.6 kV) high power applications is presented. The comparison is made for medium voltage PWM current source rectifiers using a selective harmonic elimination technique. The devices compared are High Voltage Insulated Gate Bipolar Transistor (HVIGBT) and two types of hard-driven thyristors, namely, the Symmetrical Gate Commutated Thyristor (SGCT) and the Asymmetrical Gate Commutated Thyristor (AGCT). The study depends on practical devices, data sheets from well known semiconductor vendors, taking into account accurate discrimination between turn-off and recovery states.

3. Abdelsalam, A.K., Masoud, M.I., Finney, S.J., and Williams, B.W.

'Medium Voltage PWM Current Source Rectifiers using Different Semiconductors: Loss and Size Comparison'

IET Proc. Power Electronics, Accepted for future publication.

Abstract-- In this paper, a comparison of losses and physical size is presented for three semiconductor devices suitable for medium voltage high power applications. The comparison is made for medium voltage PWM current source rectifiers (CSR) using a selective harmonic elimination technique. The devices are High Voltage Insulated Gate Bipolar Transistors and two types of hard-driven thyristors, namely the Symmetrical Gate Commutated Thyristor and the Asymmetrical Gate Commutated Thyristor. The study is based on practical devices using data sheets from semiconductor device vendors, taking into account accurate discrimination between turn-off and recovery states. The constant-voltage switching energy data sheet curves for voltage source converters are adapted to suit varying voltage applications like the PWM-CSR, with emphasis on how voltage is shared between series devices during each commutation instant.

Appendix H: List of figures and tables

H.1 List of figures

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H.2 List of tables

Chapter 2:

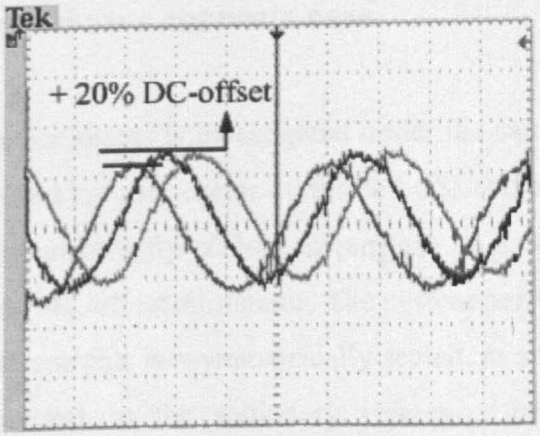
Chapter 3:

Appendix I: Proposed DC-offset eliminator experimental verification

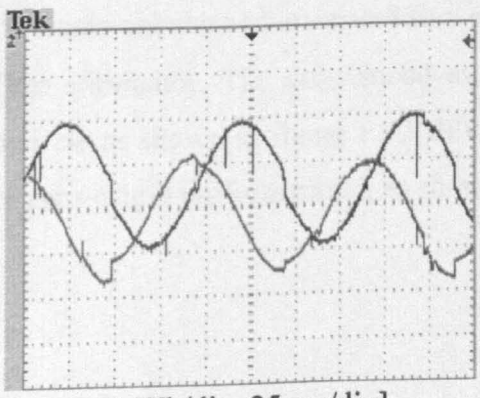
In this section, the proposed DC-offset eliminator, for the flux estimation from the stator model, is investigated with distorted input currents. This distortion is basically created due to limitations of measuring circuit board. The mismatch in the current measurement board resistors, as in their values and temperature coefficients, also the human error in tuning the measuring board variable resistors gains and transducers non-linearities can cause distortions even for undistorted motor input current signals. The distortion for the measured signals occurs in two forms, DC-offset and asymmetric gain. The performance of the proposed DC-offset eliminator is examined in the following subsections under such distortion to validate the efficiency and robustness of the proposed eliminator.

I.1 Motor currents with DC-offset case

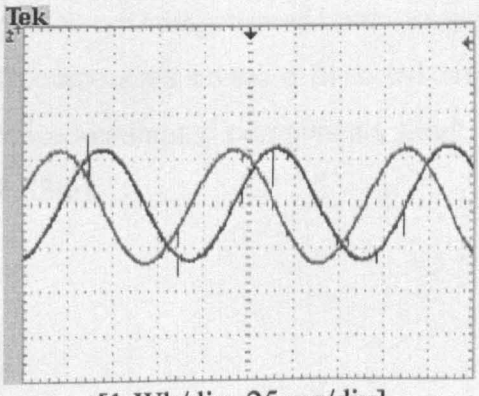
In this subsection, the motor is controlled using the proposed indirect vector controlled CSI drive in a sensorless mode, via 1 km feeder. The switching frequency is 1 kHz and a step reference speed of 200 rpm is commanded. A DC-offset is created, on purpose, onto one of the measured line currents to validate the efficiency of the proposed DC-offset eliminator. The system performance is shown in figure F.32. One of the three phase currents suffers from an on purpose DC-offset as shown in figure F.32(a). The estimated flux *d-q* components in the stationary reference, before and after DC-offset elimination, are illustrated in figure F.32 parts (b) and (c). As seen, the offset in one of the measured motor currents creates unbalanced estimated flux components which are compensated after being treated by the proposed DC-offset eliminator. The unbalanced estimated flux components create a distorted origin-shifted circle as shown in figure F.32(d) while the balanced estimated components create a definite zero-origin uniform circle, as shown in figure F.32(e). This reflects the balancing and orthogonality of the final estimated flux components, validating the excellence of the DC-offset eliminator.



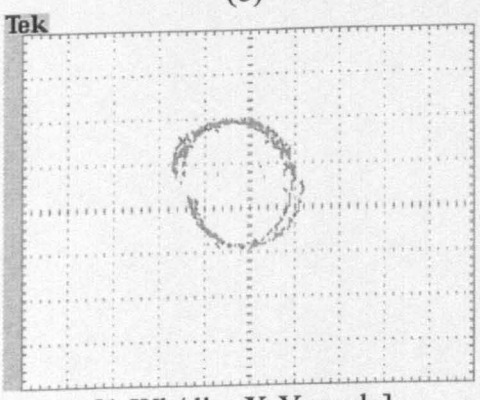
[1 A/div, 25 ms/div]
(a)



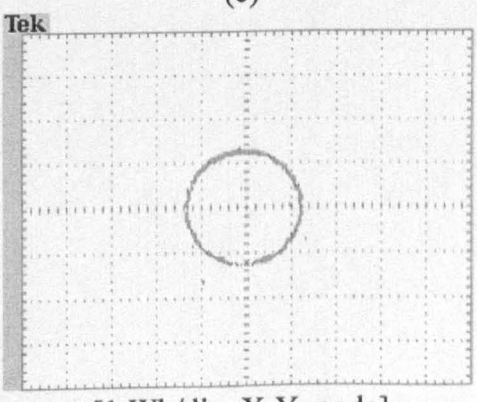
[1 Wb/div, 25 ms/div]
(b)



[1 Wb/div, 25 ms/div]
(c)



[1 Wb/div, X-Y mode]
(d)

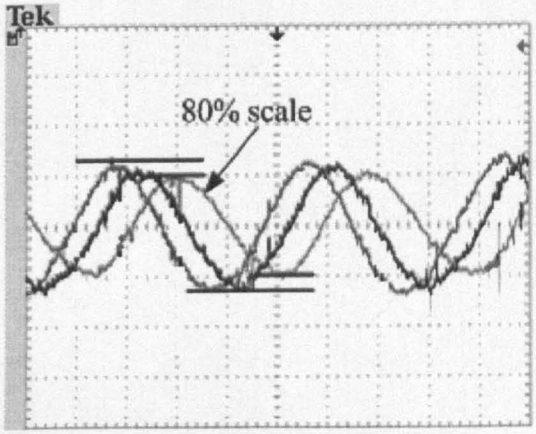


[1 Wb/div, X-Y mode]
(e)

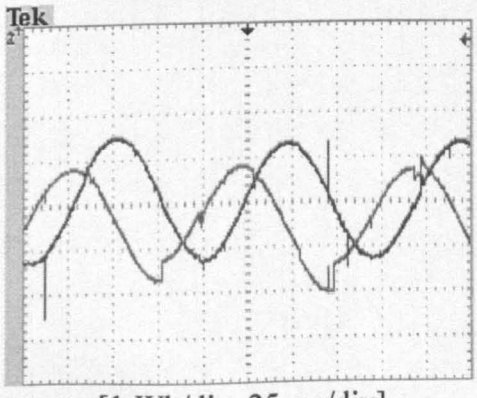
Figure F.32: Performance evaluation of the proposed DC-offset eliminator under % DC-offset of one measured current signal:
(a) measured motor current signals, (b) estimated rotor flux *d-q* component before DC-offset elimination, (c) estimated rotor flux *d-q* component after DC-offset elimination, (d) X-Y mode for estimated rotor flux *d-q* component before DC-offset elimination, and (e) X-Y mode for estimated rotor flux *d-q* component after DC-offset elimination.

I.2 Unbalanced motor currents case

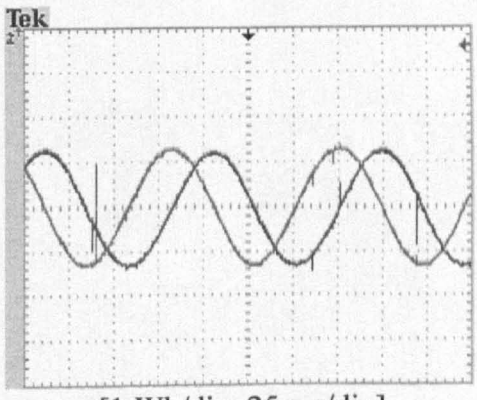
The proposed DC-offset estimator is investigated under the same loading condition as the previous case for the proposed indirect vector controlled CSI drive with 1 km feeder. One of the measure currents is asymmetrically scaled on purpose so as to study the consequential performance of the proposed DC-offset eliminator. The system performance is shown in figure F.33. One of the three phase currents is asymmetrically scaled, as shown in figure F.33(a). The estimated flux *d-q* components in the stationary reference, before and after DC-offset elimination, are illustrated in figure F.33 parts (b) and (c). The unbalanced measured motor currents create unbalanced estimated flux components which are compensated by the proposed DC-offset eliminator. The unbalanced estimated flux components create a distorted origin-shifted circle as shown in figure F.33(d) while the balanced estimated components result in a definite zero-origin uniform circle, as shown in figure F.33(e).



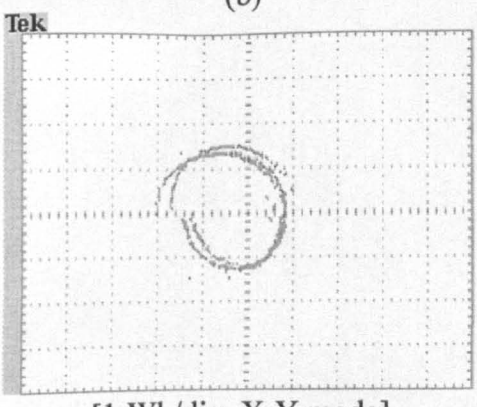
[1 A/div, 25 ms/div]
(a)



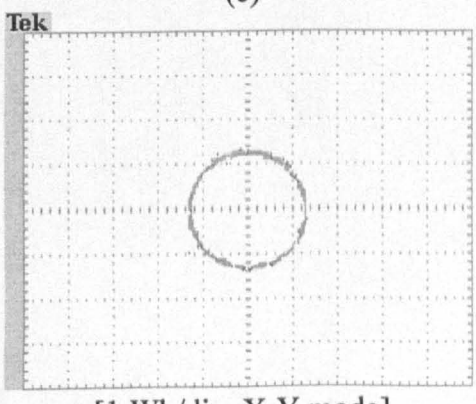
[1 Wb/div, 25 ms/div]
(b)



[1 Wb/div, 25 ms/div]
(c)



[1 Wb/div, X-Y mode]
(d)



[1 Wb/div, X-Y mode]
(e)

Figure F.33: Performance evaluation of the proposed DC-offset eliminator under % scale of one measured current signal:
(a) measured motor current signals, (b) estimated rotor flux *d-q* component before DC-offset elimination, (c) estimated rotor flux *d-q* component after DC-offset elimination, (d) X-Y mode for estimated rotor flux *d-q* component before DC-offset elimination, and (e) X-Y mode for estimated rotor flux *d-q* component after DC-offset elimination.