University of Strathclyde
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Supercapacitor based Energy Storage System

by

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Dedicated to my family

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Abstract

The supercapacitor, as a recently developed electrochemical energy storage device, offers extremely high capacitance per unit volume. Due to its unique double-layer structure and electrostatic charge mechanism, the supercapacitor has a much higher power density than the battery, and a much higher energy density than the conventional capacitor. It also benefits from a long cycle life, and wide temperature range. However, limited by a low cell voltage of 2.7V and high equivalent series resistance, the supercapacitor may be inefficient for high power grid level applications. Characteristic analysis of the supercapacitor shows that the efficiency reduces to 54.7% at peak current conditions.

Based on supercapacitor modelling studies, two parameter identification methods are proposed, which are realised by a simple experiment, with an acceptable accuracy.

A parallel combined supercapacitor and electrolytic capacitor energy storage system is proposed to improve high power application performance, which offers efficiency improvements in excess of 10%. A detailed description of such parallel capacitor systems are included in this thesis, where a design guide is developed to achieve an optimal design in terms of system efficiency, power capability, and volume. The capacitor based energy storage technique is suited to distributed generation applications where low-voltage ride through and grid code compliance are important considerations.

A supercapacitor based static synchronous compensator is proposed, which is able to manipulate both active and reactive power exchange with the power system. Steady-state and transient responses are studied based on simulation of a test power system. A system frequency based control algorithm is used for active power control, which has a better stabilised system frequency than with conventional voltage control. The parallel hybrid capacitor technique is employed, which greatly improves the system performance in terms of efficiency, thermally, costs, and volume, compared with a system that only uses supercapacitors.

List of Symbols

C_0 C_2 C_3	First, second or third branch capacitance (F)
C_{EC}	Electrolytic capacitor capacitance (F)
C_i	Initial capacitance in variable capacitance model (F)
C_{SC}	Supercapacitor capacitance (F)
C_{th}	Thermal capacitance (J/ ℃)
C_V	Variable capacitance in variable capacitance model (F)
E_{ECloss}	Energy loss of electrolytic capacitor (J)
$E_{falling}$	Energy loss during falling time (s)
E_{loss}	Overall energy loss on R_{dc} (J)
$E_{loss50\%}$	Overall energy loss on R_{dc} with 50% discharge(J)
$E_{residual}$	Residual energy in supercapacitor (J)
$E_{residual50\%}$	Residual energy in supercapacitor with 50% discharge (J)
E_{rising}	Energy loss during rise time (s)
$E_{SCECloss}$	Energy loss of SCEC system (J)
$E_{SCECout}$	Output energy of SCEC system (J)
E_{SCloss}	Energy loss of supercapacitor (J)
E_{total}	Total energy stored in capacitor (J)
E_{trans}	Transferred energy (J)
f	Frequency (Hz)
f_0	Fundamental frequency (Hz)
$f_{cutoffEC}$	Cutoff frequency of $Gain_{EC}$ (Hz)
$f_{resonantEC}$	Resonant frequency of the EC (Hz)
$f_{resonantPPC}$	Resonant frequency of the PPC (Hz)
$Gain_{EC}$	Current magnitude gain of I_{EC} normalised by I_{SC}
$Gain_{ECMAX}$	Maximum current gain of I_{EC} normalised by I_{SC}
$Gain_{ECSC}(f)$	Current gain of I_{EC} normalised by I_{SC}
$Gain_{ECSCMAX}(f)$	Maximum Current gain of I_{EC} normalised by I_{SC}
$Gain_{PPCSC}(f)$	Current gain of I_{PPC} normalised by I_{SC}
$Gain_{PPCSCMAX}(f)$	Maximum Current gain of I_{PPC} normalised by I_{SC}
I_{PPC}	PPC current (A)
I_{revA}	Half-period reversed current (A)
$I_{SCA/B/C}$	Input current of VSC for phase A/B/C (A)

I_{SCout}/I_{SC}	Output current of supercapacitor (A)
I_{SCrms}	Supercapacitor rms current (A)
$I_{STATCOM}$	STATCOM current (A)
I_{tri}	Triangle wave current (A)
$I_{VSCA/B/V}$	Output current of VSC for phase A/B/C (A)
K_C	Ratio of SC and EC parallel number
K_{I}	Integral gain
K_{P}	Proportional gain
k_v	Variable capacitance coefficient (F/V)
$L_0\ L_2\ L_3$	First, second or third branch inductance (H)
m_{VSC}	Modulation index of VSC
N_P	Parallel number
N_S	Series number
N_{SC}	Total supercapacitor number
N_{SCp}	Total supercapacitor parallel number
N_{SCs}	Total supercapacitor series number
P	Instantaneous power (W)
P_{loss}	Power loss on R_{dc} (W)
P_{max}	Theoretical maximum power (W)
P_{out}	Defined output power (W)
$\breve{P}$	Minimum instantaneous power (W)
$R_0\ R_2\ R_3$	First, second or thirdf branch resistance (Ω)
$R_{circuit}$	Circuit resistance (Ω)
R_{dc}/R_{SC}	Equivalent series resistance of supercapacitor (Ω)
R_{EC}	Equivalent series resistance of electrolytic capacitor (Ω)
R_{EPR}	Equivalent parallel resistor (Ω)
R_{ESR}	Equivalent series resistor (Ω)
R_{load}	Load resistance (Ω)
R_{th}	Thermal resistance (℃/W)
T/T_0	Fundamental period (s)
T_{ccdis}	Allowed constant current discharge time (s)
$T_{ccdis50\%}$	Allowed constant current discharge time with 50% discharge (s)
t_{con}	Continuous time for discontinuous triangle wave current (s)
T_{cpdis}	Allowed constant power discharge time (s)
$T_{cpdis50\%}$	Allowed constant power discharge time with 50% discharge (s)

$T_{dis\text{-}tridis}$	Allowed discontinuous triangle wave current discharge time (s)
t_r	Rise time of triangle wave current (s)
T_{tridis}	Allowed triangle wave current discharge time (s)
V_a	SPWM voltage control reference (V)
V_C	Capacitor voltage (V)
V_{C0} V_{C2} V_{C3}	First second or third branch capacitor voltage (V)
V_{cmin}	Minimum capacitor voltage for constant power condition(V)
V_{dc}	dc link voltage (V)
V_{Grid}	Grid voltage (V)
V_{rated}	Rated maximum voltage of supercapacitor (V)
VR_{bus}	dc bus voltage regulation
$V_{residual}$	Residual voltage (V)
V_{SCout}/V_{SC}	Output voltage of supercapacitor (V)
$V_{STATCOM}$	STATCOM voltage (V)
Δi	Ripple current (A)
ΔT	Temperature change (℃)
ΔT_{max}	Maximum temperature change (℃)
η	Instantaneous efficiency (p.u.)
η_{loss}	Energy loss percentage (p.u.)
η_{SCEC}	SCEC system efficiency (p.u.)
$\eta_{transfer}$	Energy transfer efficiency (p.u.)
$\eta_{transfer50\%}$	Energy transfer efficiency with 50% discharge (p.u.)
θ_{ps}	Phase shift (*rad*)
θ_{VI}	Phase difference between voltage and current (*rad*)
$\tau_{temperature}$	Temperature change time constant (s)

List of Abbreviations

ac	alternative current
CSC	Current-Sourced Converter
dc	direct current
DG	Distributed Generation
EC	Electrolytic Capacitor
EDLC	Electric Double Layer Capacitor
EIS	Electrochemical Impedance Spectroscopy
EPR	Equivalent Parallel Resistor
ESR	Equivalent Series Resistor
FACTS	Flexible Ac Transmission Systems
FC	Film Capacitor
FFT	Fast Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LVRT	Low-Voltage Ride Through
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PI	Proportional Plus Integral
PPC	Polypropylene Capacitor
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
rms	root mean square
SC	Supercapacitor
SCEC	Supercapacitor And Electrolytic Capacitor
SCFC	Supercapacitor And Film Capacitor
SESS	SC Based Energy Storage System
SMPS	Switched-Mode Power Supply
STATCOM	Static Synchronous Compensator
THI	Third Harmonic Injection
UPS	Uninterrupted Power Supply
VSC	Voltage-Sourced Converter

Chapter 1

1 Introduction

Due to the nature of electrical energy, it is better to consume energy as it is generated. However, for most practical conditions, energy consumption and generation are not balanced. Rather than waste energy excess, electrical energy storage technology has been used for decades. The battery and capacitor are the most common electrical energy storage devices.

The battery is able to store considerable energy within a small volume and weight. However, as an electrochemical device, the energy release, that is, the power of the battery is limited by its chemical reaction. With increased power requirements in today's electrical applications, the battery has become less effective in fulfilling the excess demand, where it has to sacrifice energy density and life time to achieve the required high power rating [1.1, 2]. Furthermore, for most battery types, its shortcomings in shelf life and cycle number results in frequent maintenance of the energy storage system, which is undesirable in many applications [1.1, 3, 4].

In contrast, the capacitor provides high power capability within a small volume and weight. However, due to its limited energy storage capability, the power only last for less than seconds. Thus capacitors are normally applied in high frequency or transient voltage stabilisation rather than energy storage [1.5, 6]. Applications, which require high power energy storage, have to tolerate large size capacitors or short life time batteries.

The supercapacitor (SC) provides a solution to the void between energy storage and power capability. This is shown in the Ragone plot (the indicated areas are rough guide lines) in Figure 1.1. Due to its extremely high capacitance, of the order of F, compared to the conventional capacitor of the order of μF, the SC is able to store much more energy. Also, since the SC operates on a similar principle as the conventional capacitor, its power capability is much higher than that of batteries. Furthermore, the SC has a better cycle life expectation than the battery.

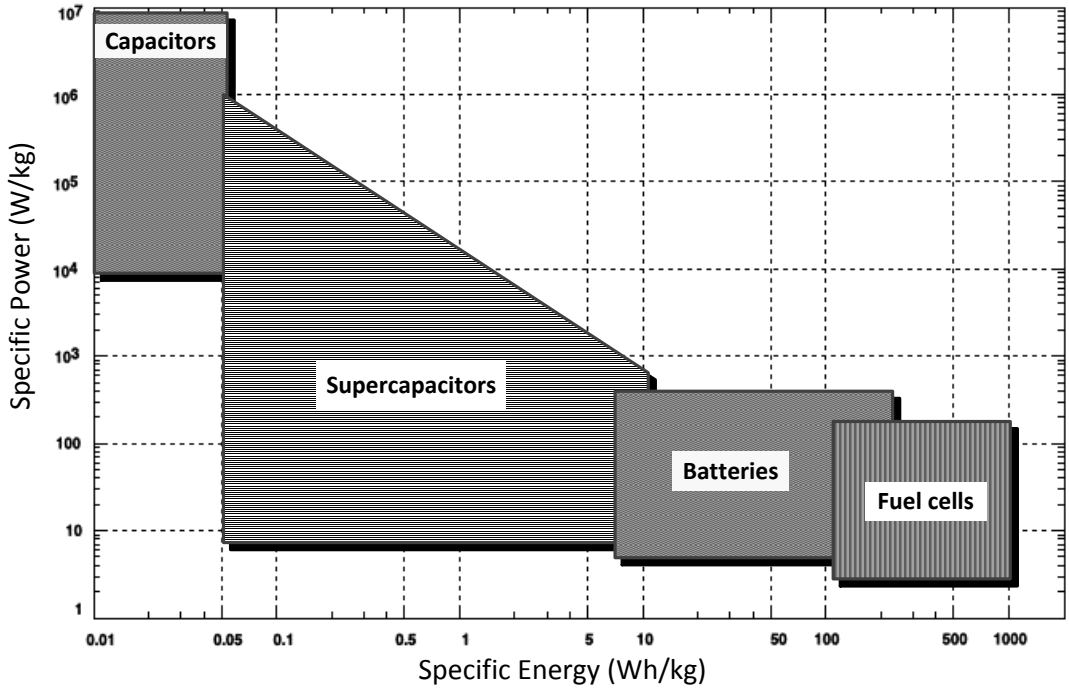

Figure 1.1 Ragone Plot for Various Energy Storage Devices [1.7].

In this chapter, the basic structure and operational principle of the SC is introduced. Advantages and disadvantages are highlighted to assess suitable conditions for applying the SC, while practical applications at different power levels are included. The problems of applying the SC as an electrical energy storage device are stressed; this being the motivation in this research to exploring better SC utilisation methods.

1.1 What is a Supercapacitor?

The word supercapacitor was originally used for the class of capacitive devices with extremely high capacitance, which generally refers to the family of electrochemical capacitors. The Nippon Electric Company (NEC) trademarked the name supercapacitor in 1975, while ultracapacitor starts to be used for the same meaning [1.8]. Based on its different charge storage mechanism, SCs can be divided into three classes: electric double-layer capacitors, pseudocapacitors, and hybrid capacitors, as shown in Figure 1.2 [1.9].

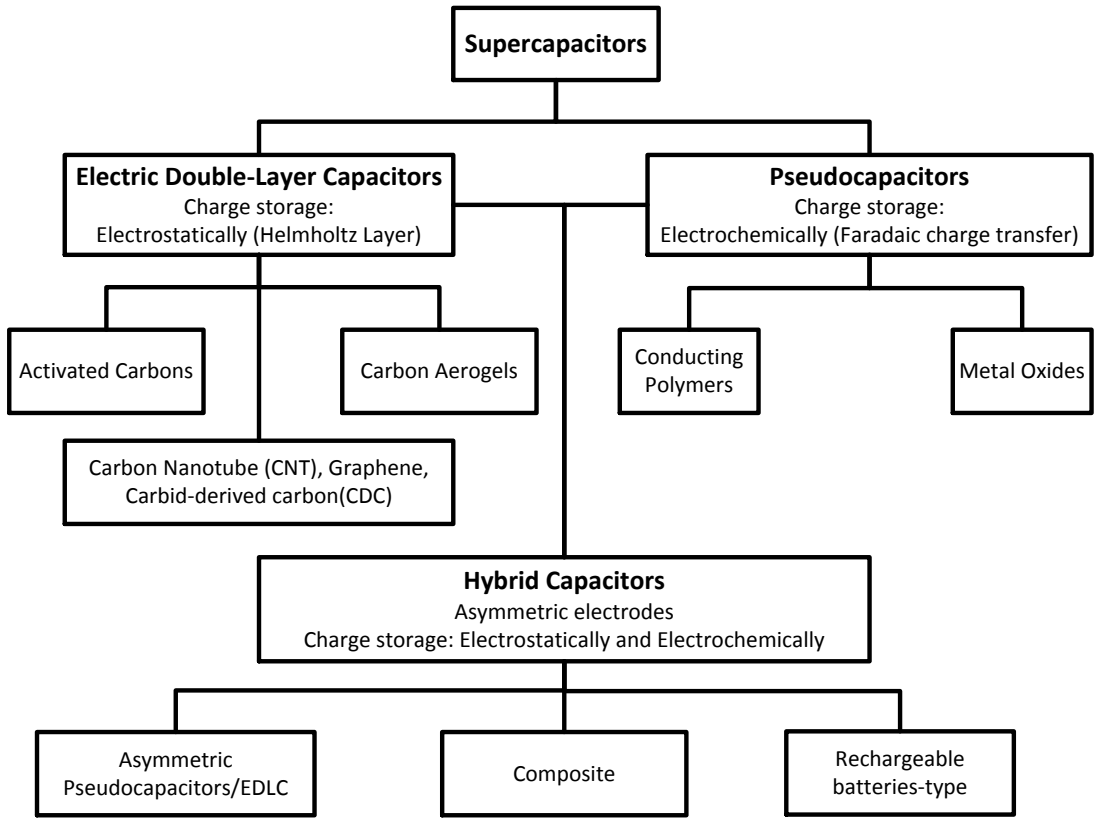

Figure 1.2 Taxonomy of Supercapacitors [1.9].

The electric double layer capacitor (EDLC) type SC has four parts, which are the current collecting plate, two carbon-based electrodes, electrolyte, and separator as shown in Figure 1.3. The EDLC charge storage principle is based on the electric double layer phenomenon, which is electrostatical without transferring of charge between the electrode and electrolyte. With a voltage applied, charge accumulates on the surface of electrode, while within the electrolyte solution, ions with opposite charge to the electrode charge, diffuse across the separator into the electrode pores. Within the specified voltage range, a double-layer of charge is formed on each electrode as shown in Figure 1.3 [1.9, 10]. Due to the large surface area and decreased distance between double layers, the EDLC can achieve much higher capacitance than conventional capacitors [1.1, 7]. The EDLC charge/discharge is a non-Faradaic process, where no or few chemical reaction, such as reduction-oxidation reactions, is involved [1.13, 14]. In such case, the energy can be stored or released as quickly as conventional capacitors, which enables high power density

realisation. Also a further benefit of the electrostatic process is that energy storage is highly reversible, with a greatly increased cycle life.

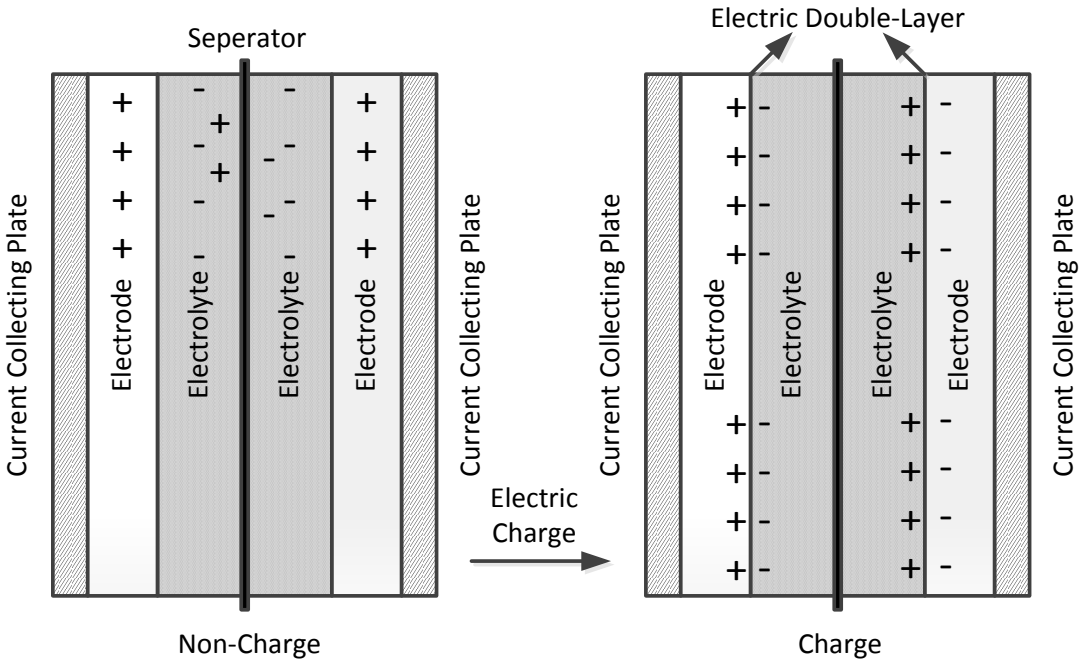

Figure 1.3 EDLC Structure and Charge Process.

Pseudocapacitors store charges by the transferring of charge between electrode and electrolyte, which accomplish through electrosorption, reduction-oxidation reactions, and intercalation processes [1.11, 12]. Due to the faradaic process, pseudocapacitors achieve greater capacitances and energy densities than EDLCs. Also a reduced cycle life is also introduced [1.13, 14].

Hybrid capacitors, which are developed by combining EDLCs, pseudocapacitors and even batteries together, aim to provide better energy storage performance [1.2, 9]. Both Faradaic and non-Faradaic processes are involved in the charge/discharge processes of hybrid capacitor, which increases the energy and power densities with less cycling stability sacrifice [1.15].

Due to the large capacitance and high power capability, SCs have been used as energy storage devices in various applications, especially in high power short duration situations. The research resented analyses SC characteristics for different

operating conditions. Because of SC limitations, a better method of using SCs is proposed, to improve its performance in efficiency, power capability, thermal, and life expectance. In addition, as the research of this thesis focuses on the EDLC, unless stated, the word 'supercapacitor' within the following chapters refers to the EDLC type SC.

1.2 Advantages and Disadvantages of the Supercapacitor

Due to the SCs unique physical structure, high power density is achieved by the electrostatic charge storage mechanism, while the high energy density is achieved by the high surface area and narrow distance of the double-layer. As a result, the advantages when applying SCs as the energy storage devices are summarised as follows:

1) 'High' energy and power density

The SC fills the gap between the conventional capacitor and battery, but has a higher energy density than the conventional capacitor, and a higher power density than the battery. In such conditions, it is ideal for operating as an energy storage system in high power pulse applications.

2) 'Unlimited' cycle life

As an energy storage device, the SC has to charge and discharge to realise energy exchange. Compare to battery, SC has a much better cycle life, which is 1000 times that of the battery, as shown in Table 1.1. This excellent feature enables its applications at non-user serviceable locations, such as deep sea or mountainous locations [1.1, 7].

3) Rapid charging

The SC can be fully charged in the order of seconds due to its high power capability. As no chemical reaction is involved, fast SC charging has no or little affects on its performance. For the battery, a high power charge results in decreased life time. The rapid SC charging feature ideally fits public transportation requirement, where

the SC can be charged at each stop. In such conditions, the required energy is reduced due to the short distance between two stops of public vehicle.

4) Simple charge methods

Since the SC has similar electric characteristics as the conventional capacitor, the voltage directly reflects its state of charge. Unlike a battery, no full-charge detection is required. In addition, the SC does not have specific current requirement during the charge process, provided it is below the maximum current limit. In practical applications, the most common charge method is constant current or power charge, which can be easily achieved with dc/dc converter [1.16-18].

Table 1.1 Energy Storage Technology Comparison [1.19]

STORAGE TECHNOLOGY	Charge/ Discharge Time (s)	Cycle Life (80% Depth of Discharge)	Specific Energy (Wh/kg)	Cost ($/kWh)
Electrostatic Capacitor	10^{-9}	$>10^{15}$	0.001	2,000,000
Electrolytic Capacitor	10^{-4}	$>10^{10}$	0.05	1,000,000
Supercapacitor	1	$>10^{6}$	5	20,000
Li-ion Battery	10^{2}	$>10^{3}$	100	1,000
Lead Acid Battery	10^{4}	$>10^{2}$	30	100

5) Cost reduction

In the past decade, SC costs have greatly reduced, by 99%. The cost of the Maxwell BCAP3000 with 3000F 2.7V, was $5,000 10 years ago, while today, it only costs $50 [1.20]. During the same period, battery costs have reduced by only 30% to 40%. A reduction of 30% to 50% is predicted for the SC in the near future [1.19].

6) Wide temperature range

The SC is able to operate within a temperature range of -40 ℃ to 65 ℃, and stored within a -40 ℃ to 70 ℃. Such thermal performance enables applications in some extreme environment. However, SC operation outwith these temperatures and voltages could expect a reduced life. As shown in Figure 1.4, component life at 55 ℃ doubles for every 10 ℃ decrease in temperature, while 0.1V decrease in voltage also doubles the life time. In order to achieve a better life expectation, the SC should operate at a low temperature, while the operation voltage is normally 0.1V to 0.2V lower than its maximum voltage rating.

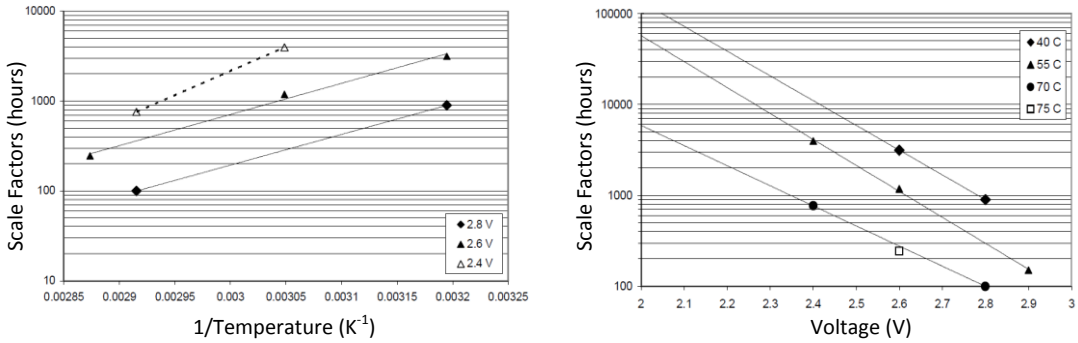

Figure 1.4 Capacitor Life versus Temperature and Voltage for Panasonic "Gold Cap" [1.19]

Based on these excellent features, the SC has been incorporated into different application areas. However, the following SC application limitations have to be noted:

1) Linear discharge voltage

SC voltage decreases linearly as the energy discharges, where external control circuit is required to regulate the output current and power. Also, full energy spectrum usage is difficult to realise due to the low voltage at the end of discharge process. In practice, an SC is normally charged and discharged between its maximum and half of the rated value, which stores 75% of the total SC energy.

2) Low energy density

Although the SC has a much higher energy density than the conventional capacitor, it is still not able to achieve that of the battery. For applications requiring high Wh/kg, such as electric vehicles, the SC can only be used as a secondary energy source.

3) Low cells voltage

The equivalent plate separation distance of the SC is determined by the thickness of the formed double layer, which is the electrolyte molecules thickness (0.4nm). In such case, strong electric field strength is generated. For available electrolyte material, it can only withstand low voltage to resist such strong electric field strength, and thus the single cell voltage of the SC is limited to a low value, only 2.7V for Maxwell products [1.2]. As a result, series connection is required for most applications. For high voltage conditions, a large number of SC in series is challenging for the voltage balancing circuitry. A small difference in resistance and capacitance can result in considerably heavy stress on a single cell.

4) High self-discharge

Almost all energy storage devices, including capacitors and batteries exhibit electrical leakage, which causes a gradual loss of stored charge. The SC self-discharge rate is considerably higher than that of an electrochemical battery [1.9]. For certain applications, such as uninterrupted power supply (UPS), the energy storage device may be stored for a long period. In such cases, the SC requires an external source to compensate for the self-discharged energy.

5) Equivalent series resistance

SC has a higher equivalent series resistance than in conventional capacitors. The internal resistor, which is the power loss source, results in SC temperature rise. Furthermore, being limited by a low cell voltage, the SC has to be discharged at a high current level to achieve a high power requirement. In such conditions, the higher the output power, the more power loss in the internal resistor and the higher the temperature rise. The equivalent series resistance can be considered as one key factor limiting SC performance.

6) Low operating frequency

SC has an RC time constant of about 1s, which means operating at high frequency becomes inefficient. Also as shown in Table 1.1, a conventional capacitor in a high frequency ac system has a much better cycle life than a SC. Thus the SC is normally used for energy storage in dc system.

1.3 Applications of Supercapacitor

Compare to the battery and conventional capacitor, the SC is a relatively new device which has not been used widespread in practical applications, especially at the grid level. Initially, due to its high cost with limited power and energy capabilities, SC was only used in low-power, low energy applications, such as telecommunications and portable devices for energy back up [1.21, 22]. Recently, however, manufacturing technology and the costs of SCs have experienced a rapid improvement, which enables its applications at medium and high power levels [1.23]. At medium power levels, SC based energy storage systems have drawn attention, especially in electrical vehicles and for public transportation. Much research has been presented on energy storage based on either the SC only or in combination with batteries or fuel cells [1.2, 9, 22, 24]. Also due to its good performance in high power pulse applications, the SC has been proposed for grid level applications. For conditions, such as low voltage ride through, power mismatch, and system frequency oscillation, an SC based energy storage system is able to provide active power compensation to improve system performance [1.25, 26]. Examples of applying SC based energy storage at different power levels follow.

1.3.1 Small Electronic Device Application

For small electronic device applications involving real-time clocks and memory buffers, the SC is usually used as the backup power to ensure the device functions for a short period during sudden lost of the primary energy supply. Compare to conventional backup power sources, such as the battery, the SC has a virtually unlimited life cycle, which results in less frequent or even non-maintenance of the device. Nowadays, flash memory in applications such as network computer servers,

telecommunications, hospitals and factories, relies on uninterrupted and a high quality energy supply to ensure its operation. In such cases, a brief power interruption can cause loss of critical data. The SC is used to provide protection during sudden power loss, where the SC enables storage of important data within a short period of time. Several solid-state disk drive producers have integrated Maxwell's ultracapacitors to realise a 'power loss protection' function in their devices [1.27].

1.3.2 Transportation Application

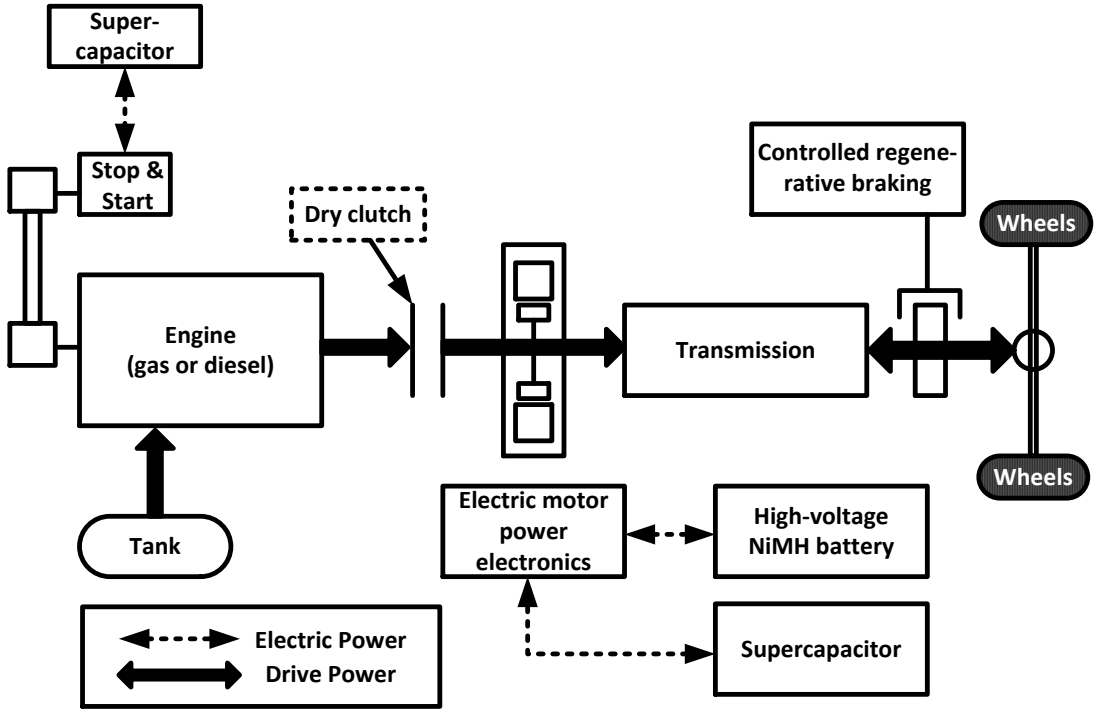

Figure 1.5 Mid-Scale and Full Hybrid Electrical Vehicle Structure [1.2].

Due to its high power capability, the supercapacitor is able to capture a large amount of energy during a short period, which is ideally for regenerative braking. Regenerative braking, which is normally applied in electrical vehicles or hybrid electrical vehicles, is used to recovery energy during vehicle deceleration. Unlike a conventional braking system, a regenerative breaking system converts some of its kinetic energy into a storable form of energy rather than dissipating it as heat. As

deceleration has to be finished within seconds, the primary energy source, such as battery or fuel cell, can only recover small amount of energy due to its limited power capability. SC features match the regenerative brake condition, where the stored energy can be discharge from the SC at higher power to achieve better performance during acceleration.

Figure 1.5 shows the structure of a medium-scale hybrid electrical vehicle incorporating a SC based energy storage system. Battery and gas operate as the primary energy source, where the battery operates at low speed and the gas fed part starts operation as the battery exceeds its capability or the battery energy is depleted. The SC as the secondary energy source provides regenerative braking functionality to improve vehicle performance during deceleration and acceleration [1.2]. In addition, a start-stop technology is realised by the SC as shown in Figure 1.5. Such technology enables energy savings by shutting down the engine at stops, such as red lights or heavy traffic. By benefiting from its low life cycle cost and high reliability at temperatures from -25 ℃ to 45 ℃, the SC is able to help a vehicle to achieve better energy efficiency [1.28].

SC Bus Station Overhead Charging Line

Figure 1.6 SC Bus at a Bus Stop in Shanghai [1.29].

The SC also has potential in public transportation systems. In an urban area, a bus has a preset route with a regularly distance of 4.8km between stops [1.29]. Due to its fast charging characteristic, a SC based bus is able recharge via the charging station at each stop. As shown in Figure 1.6, an overhead charging line is installed at the bus stop, where a collector on the top of the bus rises to connect and charge the SC.

Compared to an electric trolley bus, a SC bus is able to save 40% energy due to its lighter weight and recovered energy from regenerative braking. Compared to a conventional diesel bus, a SC bus is able to achieve a lifetime fuel savings of $200,000, estimated by Sinuate [1.29].

1.3.3 Grid Level Application

In order to satisfy the peak power requirement of grid level applications, over sized primary energy storage devices, such as batteries or fuel cells, have to be designed in to tolerate the rarely peak power conditions. As a result, the over sized energy storage system is based on peak power needs, rather than continuous power requirements, so is costly and inefficient. The high power short duration characteristic of the SC fits well with such conditions. Applications, such as large-scale UPS, low-voltage ride through (LVRT) conditions for wind generation and STATCOMs with active power capability, have been investigated to combine with SC based energy storage systems [1.25, 30].

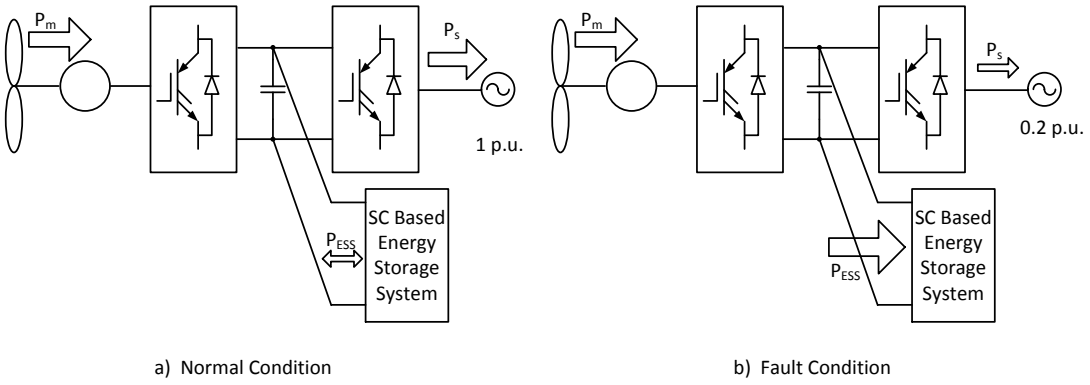

Figure 1.7 SC based Energy Storage System for Wind Generation during LVRT [1.25]

LVRT, (also known as fault/transient ride through), refers to the ability of handling a temporally grid voltage decrease caused by a fault or load change. During fault conditions, the whole power system may become unstable. Conventionally, generators may be disconnected from the grid to avoid system instability. In such cases, the system recovery time is lengthy due to the complicated generator reconnection procedure. At present, distributed generation (DG), such as wind and

solar energy, provides a relatively small percentage of the whole power generation, so has limited impact on power system stability. However, with increased DG, LVRT is essential for power system stability. It is required that generators withstand a fault or load change induced voltage dip for a certain period of time, for example, E.ON and UK grid codes are 150ms, 140ms respectively [1.31, 32].

As shown in Figure 1.7, a SC based energy storage system (SESS) is connected in parallel with the dc link capacitor to enhance LVRT capability and improve output power quality of wind power system. The basic idea for using SESS in wind power generation is similar to regenerative braking. Under normal conditions in Figure 1.7a, SESS can be used to maintain the generator output power at a certain level, or smooth the power oscillation. Under fault conditions in Figure 1.7b, the generator is able to continuously provide power as during normal conditions, where the energy is delivered to the SESS. After the fault is cleared, the system can recovery fast and the SESS stored energy can be redelivered to the grid.

1.4 Statement of the Problem

As stated in the SC limitations section, the relatively high equivalent series resistance limits SC power capability during sub one second durations. For grid level applications, the SC can be inefficient as the discharge/charge time less than 1s. Based on the SC constant current discharge characteristic, efficiency can decrease to 58.3% at SC peak current rating. Furthermore, the high voltage level of the grid requires a large number of SCs in series connection, which introduces increased capacitor size and voltage balancing problems. Under such circumstances, applying a SC based energy storage system in grid level applications is challenging.

1.5 Thesis Organization

This thesis aims to develop an improved method of using the SC in energy storage systems. As stated, the SC is inefficient during short duration (<1s) grid level (high voltage and current) applications. A parallel capacitor technique is proposed to support transient conditions, where a SC based STATCOM is developed to

demonstrate the SC in grid level applications. The main topics of each chapter are as follows.

Chapter 2 analyses the characteristics of a SC operating under different conditions, including constant current, constant power, and triangle wave discharge. Mathematical models are developed for the characteristic analysis, and are verified by simulation and experimentation. A SC based energy storage system with a bidirectional buck/boost converter is presented as an example of SC application for voltage stabilisation. A thermal SC model is developed for its operation at different current and power levels.

Chapter 3 reviews different electrical SC models, where the model topology, parameter identification method, and suitable applying conditions, are included. Two new parameter identification methods are proposed to demonstrate a simplified experimental test for SC modelling.

Chapter 4 proposes the parallel capacitor technique to improve transient energy supply efficiency for SC based energy storage systems. A parallel connected supercapacitor and electrolytic capacitor system is developed along with its mathematical model, where simulation and experimental results are presented to validate the concept. The characteristics of the combined system are summarised and verified experimentally. A design guide for the combined energy storage system is introduced which aims to achieve an optimal solution for efficiency, output power, and capacitor size. A three branch model, as an extension of the two capacitor (SC plus electrolytic) parallel system, is developed with the third branch of a lower time constant being a metallised polyethylene capacitor. Frequency analysis based on the mathematical model of the two and three branch models is included.

Chapter 5. A supercapacitor based STATCOM aims to provide reactive power during normal conditions, which normalise the grid voltage at the required level. During transient conditions, such as a fault or sudden load change, it is able to provide active power to stabilise the power system frequency. Further energy storage system analysis, based on supercapacitors paralleled with other types of capacitors, is introduced to improve SC efficiency, volume, thermal performance,

and lifetime. The supercapacitor based STATCOM is developed, where the STATCOM topology and control system are introduced. Simulations under different conditions are analysed to evaluate the performance of applying supercapacitors in a STATCOM during both steady-state and transient conditions. The current, voltage, efficiency, and thermal characteristics of a single cell supercapacitor are scaled to a fullscale energy storage system to analyse the feasibility of combining supercapacitors and the STATCOM.

Chapter 6 summarises the thesis and highlights the contributions. Future research is suggested for the SC based energy storage system.

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Chapter 2

2 Supercapacitor Characteristic Analysis

Due to its ultra high capacitance, the supercapacitor (SC) has a much higher energy density than a conventional capacitor, and higher power density than a battery. As a result, it is ideal for energy storage applications which involve high power within relevant short duration. As an energy storage device, efficiency is a significant parameter when evaluating its performance. In a supercapacitor, the internal resistance accounts for most of the energy loss, causing heat during charge/discharge processes. Similar to the conventional capacitor, the temperature raise caused by the internal resistance limits SC operation range. The characteristic analysis of a SC aims to provide a general view of the performance in terms of efficiency, discharge time, power, current and voltage variation trend, for the SC operating at different conditions.

Several SC models have been proposed and can be categorized as a classic model, a variable capacitance capacitor model, a multi-branch model or a transmission line model. In general, better supercapacitor behaviour accuracy requires a more complex model, and applying a complex model in developing an analytical model is inefficient [2.1-4]. As in this chapter, the SC characteristic analysis focuses on mathematical modelling of the SC at different discharge conditions, where a more convenient and straightforward model is required for better understanding of SC characteristics. Therefore, the simplified supercapacitor classic model is chosen to yield efficient analysis [2.5]. Complex models for better SC behaviour description are discussed in Chapter 3.

The characteristic analysis includes different SC operating conditions. Constant current and constant power discharge are typical application methods for the supercapacitor, where the analytical model is developed to show the efficiency characteristics of the SC. A triangle wave discharge relates to the supercapacitor in practical applications. The bidirectional buck/boost converter introduces a classic example for applying the supercapacitor as an energy storage system with its energy

flow control algorithm. A thermal model is developed to illustrate and examine the thermal characterises of the supercapacitor.

2.1 Constant Current Discharge

Similarly to the conventional capacitor, the SC voltage varies during its charging/discharging, and the change rate is related to its charging/discharging current. Due to convenience and accuracy, the constant current charging/discharging method is a typical method for applying the SC in practical applications and is accurate in practice [2.6-10]. Although the boundary conditions for discharge and charge processes are different, the mathematical expression for the basic circuit is valid for both processes. The characteristic analysis is developed based on discharging the SC at given constant current level to a certain voltage. The mathematical model is developed for the characteristic research, while simulation and experimentation verify the mathematical model.

2.1.1 Constant Current Discharge Mathematical Modelling

The SC mathematical model is developed on the same electrical characteristics as the conventional capacitor, which can be described by two equations: Capacitor voltage:

$$V_c(t) = V_c(0) - \int_0^t \frac{I \cdot t}{C} dt \quad \textbf{(2.1)}$$

where I is the current through the capacitor, and $V_c(0)$ is the initial voltage of the capacitor

Energy stored in capacitor:

$$E_{total} = \frac{1}{2} C \cdot {V_c}^2 \quad \textbf{(2.2)}$$

where V_c is the voltage across the capacitor

According to the classic SC model [2.5], the SC is modelled as a capacitor C in series with internal resistor R_{dc}. Under constant current conditions, it is connected to a constant current source as shown in Figure 2.1.

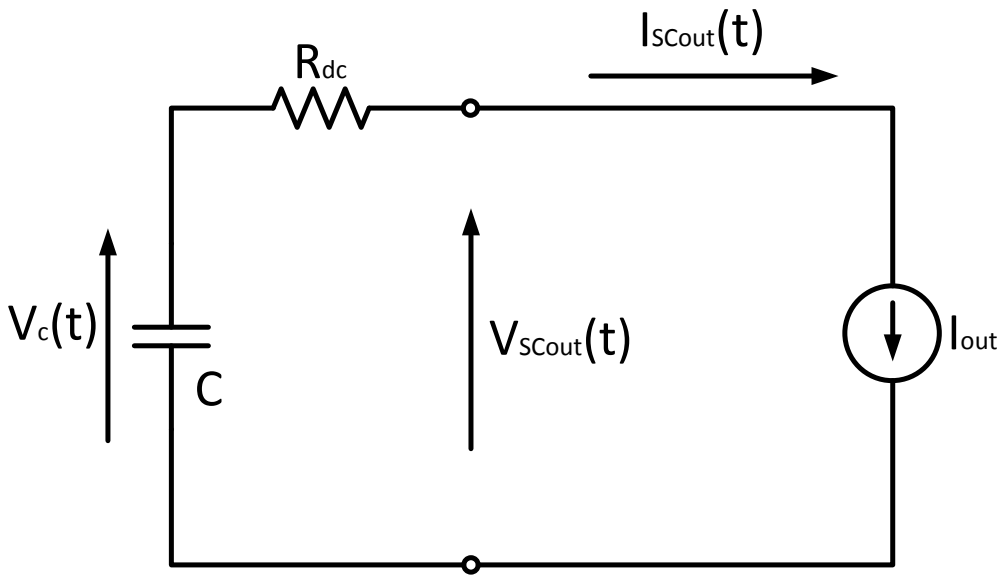

Figure 2.1 Constant Current Discharge Mathematical Model.

From the circuit diagram, the following mathematical equations can be developed to build the mathematical model:

The output current of SC is defined as a constant:

$$I_{SCout}(t) = I_{out} \tag{2.3}$$

The output voltage of SC:

$$\begin{aligned} V_{SCout}(t) &= V_c(t) - I_{SCout}(t) \cdot R_{dc} \\ &= V_c(0) - \frac{I_{out} \cdot t}{C} - I_{out} \cdot R_{dc} \ (t \in [0, T_{ccdis}]) \end{aligned} \tag{2.4}$$

Equation (2.4) is valid as t is within the allowed constant current discharge time T_{ccdis}. T_{ccdis} is defined by the boundary of the constant current discharge condition, where the current $I_{SCout}(t)$ cannot remain constant because the capacitor voltage $V_C(t)$ equals the voltage across R_{dc}. This capacitor voltage $V_C(T_{ccdis})$ is defined as the residual voltage $V_{residual}$.

$$V_{residual} = V_c(T_{ccdis}) = I_{out} \cdot R_{dc} \tag{2.5}$$

Also from Equation (2.1), the residual voltage can be expressed as:

$$V_{residual} = V_c(T_{ccdis}) = V_c(0) - \frac{I_{out} \cdot T_{ccdis}}{C} \quad \textbf{(2.6)}$$

Combining equations (2.5) and (2.6), the allowed constant current discharge time T_{ccdis} for an SC in terms of discharge current I_{out} is:

$$T_{ccdis}(I_{out}) = \frac{C}{I_{out}} \cdot (V_c(0) - I_{out} \cdot R_{dc}) = \frac{Q(0)}{I_{out}} - \tau$$

where $Q(0)$ *is the initial electric charge, and* τ *is the time constant of SC.* **(2.7)**

Conversely, the discharge current I_{out} in terms of T_{ccdis} is:

$$I(T_{ccdis}) = \frac{C \cdot V_c(0)}{T_{ccdis} + C \cdot R_{dc}} \quad \textbf{(2.8)}$$

The residual voltage in terms of T_{ccdis} is:

$$V_{residual}(T_{ccdis}) = I(T_{ccdis}) \cdot R_{dc} = \frac{C \cdot V_c(0) \cdot R_{dc}}{T_{ccdis} + C \cdot R_{dc}} = \frac{V_c(0) \cdot \tau}{T_{ccdis} + \tau} \quad \textbf{(2.9)}$$

A similar boundary occurs for the charging process. As the SC voltage $V_{SCout}(t)$ charges to the rated voltage during a constant current condition, the charging process has to stop to prevent capacitor over voltage. However, due to the internal resistance, the SC voltage $V_{Scout}(t)$ drops once the current ceases. For fully charging the SC to its rated voltage, the current has to reduce to zero gradually at the end of charging process.

Based on the basic equations presented, the following useful parameters for the characteristic analysis can be developed:

1. Instantaneous Power:

$$P(t) = V_{SCout}(t) \cdot I_{out} = (V_c(0) - \frac{I_{out} \cdot t}{C} - I_{out} \cdot R_{dc}) \cdot I_{out} \quad \textbf{(2.10)}$$

Minimum Instantaneous Power:

$$\check{P} = \left(V_c(0) - \frac{I_{out} \cdot t}{C} - I_{out} \cdot R_{dc}\right) \cdot I_{out} = 0, when\ t = \frac{Q(0)}{I_{out}} - \tau \quad \textbf{(2.11)}$$

2. Instantaneous Efficiency:

$$\eta(t) = \frac{P(t)}{P(t) + P_{loss}} = \frac{V_{SCout}(t) \cdot I_{out}}{V_{SCout}(t) \cdot I_{out} + {I_{out}}^2 \cdot R_{dc}} = \frac{V_c(0) - \frac{I_{out} \cdot t}{C} - I_{out} \cdot R_{dc}}{V_c(0) - \frac{I_{out} \cdot t}{C}} \quad \textbf{(2.12)}$$

3. Energy Transfer Efficiency:

$$\eta_{transfer} = \frac{E_{total} - E_{loss} - E_{residual}}{E_{total}} \quad \textbf{(2.13)}$$

Overall energy loss on R_{dc}:

$$E_{loss} = \int_0^{T_{ccdis}} {I_{out}}^2 \cdot R_{dc}\, dt = I_{out} \cdot R_{dc} \cdot C \cdot (V_c(0) - I_{out} \cdot R_{dc}) \quad \textbf{(2.14)}$$

Residual energy in SC:

$$E_{residual}(I_{out}) = \frac{1}{2} C \cdot {V_{residual}}^2 = \frac{1}{2} C \cdot {I_{out}}^2 \cdot {R_{dc}}^2 \quad \textbf{(2.15)}$$

Total energy stored in SC at initial voltage $V_C(0)$:

$$E_{total} = \frac{1}{2} C \cdot V_c(0)^2 \quad \textbf{(2.16)}$$

The Energy Transfer Efficiency is:

$$\eta_{transfer}(I_{out}) = 1 - \frac{2I_{out} \cdot R_{dc}}{V_c(0)} + \frac{{I_{out}}^2 \cdot {R_{dc}}^2}{V_c(0)^2} \quad \textbf{(2.17)}$$

Equation (2.17) describes the useable energy as a percentage of the whole energy stored in the SC at a defined discharge current level I_{out}.

4. Energy Loss Percentage:

$$\eta_{loss}(I_{out}) = \frac{E_{loss}}{E_{total}} = \frac{2I_{out} \cdot R_{dc}}{V_c(0)} - \frac{2{I_{out}}^2 \cdot {R_{dc}}^2}{V_c(0)^2} \quad \textbf{(2.18)}$$

Differentiate $\eta_{loss}(I_{out})$ with respect to I_{out} :

$$\frac{d\eta_{loss}(I_{out})}{dI} = \frac{2R_{dc}}{V_c(0)} - \frac{4I_{out} \cdot {R_{dc}}^2}{V_c(0)^2} \xrightarrow{Let\ \frac{d\eta_{loss}(I_{out})}{dI} = 0} I_{out} = \frac{V_c(0)}{2R_{dc}} = \frac{I_{S/C}}{2}$$

The Maximum Energy Loss occurs when $I_{out} = \frac{V_c(0)}{2R_{dc}} = \frac{I_{S/C}}{2}$, which is the half the short circuit current, and the Energy Loss Percentage is 50%.

$$\eta_{loss}\left(\frac{I_{S/C}}{2}\right) = \frac{2\frac{V_c(0)}{2R_{dc}} \cdot R_{dc}}{V_c(0)} - \frac{2(\frac{V_c(0)}{2R_{dc}})^2 \cdot {R_{dc}}^2}{V_c(0)^2} = 1 - \frac{1}{2} = 50\%$$

5. Transfer Efficiency for 50% Discharging:

In practical applications, the SC is normally charged and discharged between its maximum and half of the rated value which stores 75% of the total energy in the SC. Assuming the initial SC voltage $V_C(0)$ is charged at its rated maximum voltage V_{rated}, the discharge time for the SC voltage $V_{Scout}(t)$ discharge to 50% of V_{rated} is

$$T_{ccdis50\%}(I_{out}) = \frac{C}{I_{out}} \cdot (0.5V_{rated} - I_{out} \cdot R_{dc}) \quad \textbf{(2.19)}$$

The energy loss on R_{dc} is:

$$\begin{aligned} E_{loss50\%} &= \int_0^{T_{ccdis50\%}} {I_{out}}^2 \cdot R_{dc}\, dt \\ &= I_{out} \cdot R_{dc} \cdot C \cdot (0.5V_{rated} - I_{out} \cdot R_{dc}) \end{aligned} \quad \textbf{(2.20)}$$

Residual energy in SC:

$$E_{residual50\%}(I_{out}) = \frac{1}{2}C \cdot (0.5V_{rated})^2 \quad \textbf{(2.21)}$$

Total energy stored in SC at an initial voltage of V_{rated} is:

$$E_{total} = \frac{1}{2}C \cdot {V_{rated}}^2 \quad \textbf{(2.22)}$$

The Energy Transfer Efficiency is:

$$\eta_{transfer50\%}(I_{out}) = \frac{E_{total} - E_{loss50\%} - E_{residual50\%}}{E_{total}} \quad \textbf{(2.23)}$$

Based on the Maxwell BCAP3000 model, the Four-Quarter characteristic plot is shown in Figure 2.2, while Table 2.1 listed the four important current levels in the datasheet with the discharge time, transfer efficiency and loss percentage.

Table 2.1 Discharge Results of BCAP3000.

	Test Condition	I_{out}	T_{ccdis}	$\eta_{transfer}$	η_{loss}
a	Maximum Continuous Current ($\Delta T = 15℃$)	130A	61.44s	97.2%	2.8%
b	Maximum Peak Current, 1s (no repetitive)	2200A	2.81s	58.3%	36.1%
c	Maximum Energy Loss	4655A	0.87s	25%	50%
d	Short Circuit Current	9130A	0s	0%	0%

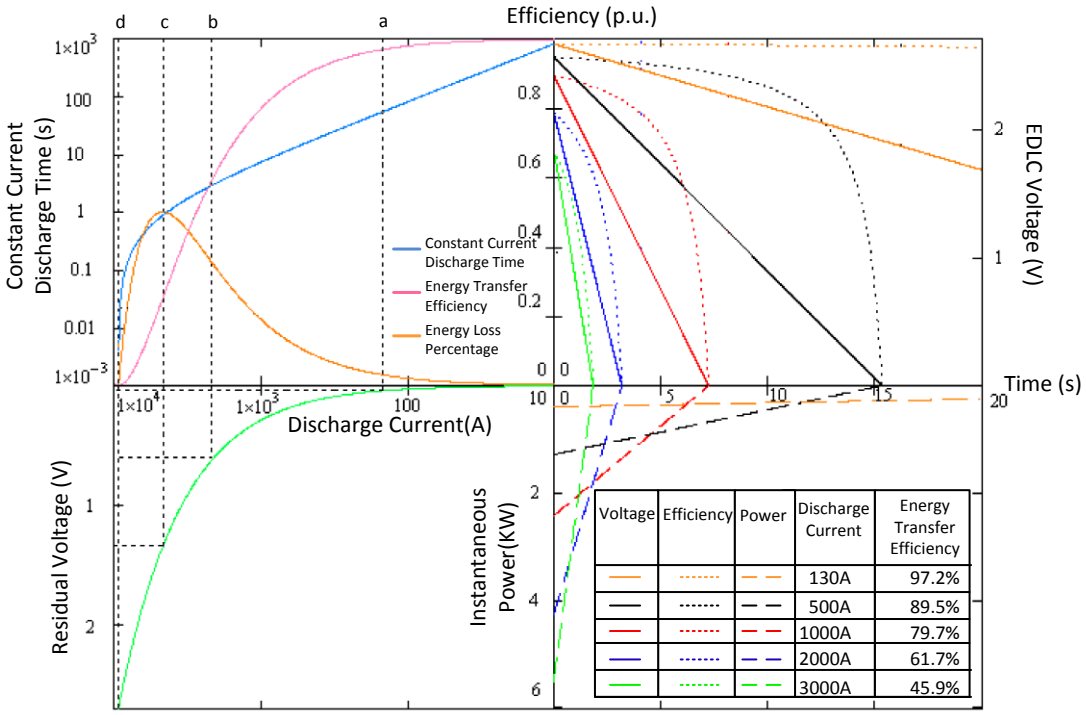

Figure 2.2 Four-Quadrant Constant Current Discharge Characteristic Plot for BCAP3000.

Figure 2.2 is divided into four quadrants, which incorporates the different parameters during constant current discharge. The general SC characteristics, based on mathematical model, are summarised as follows:

1. First quadrant: The SC Voltage decreases linearly for constant current discharge (equation (2.4)). Instantaneous efficiency decreases non-linearly (equation (2.12)), where a higher discharge current level results in lower efficiency and shorter discharge time.
2. Second quadrant: Constant Current Discharge Time (equation (2.7)) and Energy Transfer Efficiency (equation (2.17)) decreases as the reference current increases. Energy loss percentage (equation (2.18)) has a maximum value of 50% at half the short circuit current, after which the loss percentage decreased as more energy is stored in the capacitor as residual energy.
3. Third quadrant: The Residual Voltage increases as the reference current increase, equation (2.6).
4. Fourth quadrant: Instantaneous Power varies linearly with time under a constant current discharge condition (equation (2.10)).

The developed mathematical model for SC constant current discharge is suitable for general SC efficiency analysis. For a general commercial SC product data sheet which only provides capacitance and internal resistance, the mathematical model is convenient for estimating the efficiency of the designed SC energy storage system. The model can be extended for analysing different capacitors which have the similar series resistor and capacitor topology.

2.1.2 Constant Current Discharge Simulation Verification

The simulation model, developed in Matlab/Simulink, is based on a boost converter with a 40kHz switching frequency, where the inductor current is controlled to achieve the constant current discharge condition, with minimal ripple current. The SC simulation model is same as the mathematical model: a capacitor with an initial voltage in series with its internal resistance. By sensing the inductor current, the output current of the SC is regulated using a proportional plus integral (PI) controller, with proportional gain $K_P = 0.01$ and integral gain $K_I = 5$, chosen to give a slightly overdamped control characteristic. The PI controller generates the pulse width modulation (PWM) duty cycle, which provide the switch control signal for the ideal switch, as shown in Figure 2.3. The SC model is based on the Maxwell

BCAP3000 SC with capacitance of 3000F and internal resistance of 0.29mΩ, at 2.7V. The instantaneous efficiency is calculated from equation (2.12).

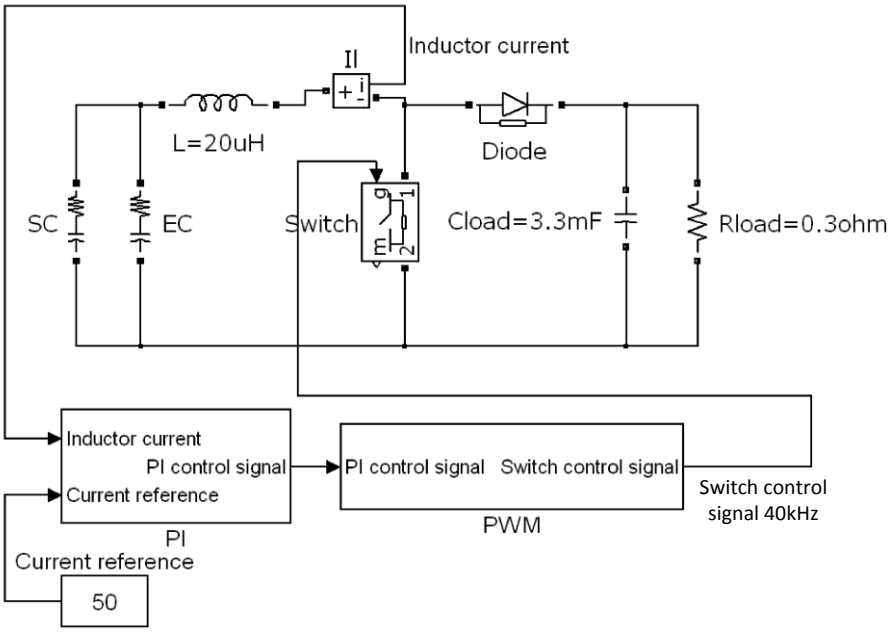

Figure 2.3 Constant Current Simulation Model.

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Simulation is based on different current levels, which are selected between the maximum continuous current and the maximum peak current.

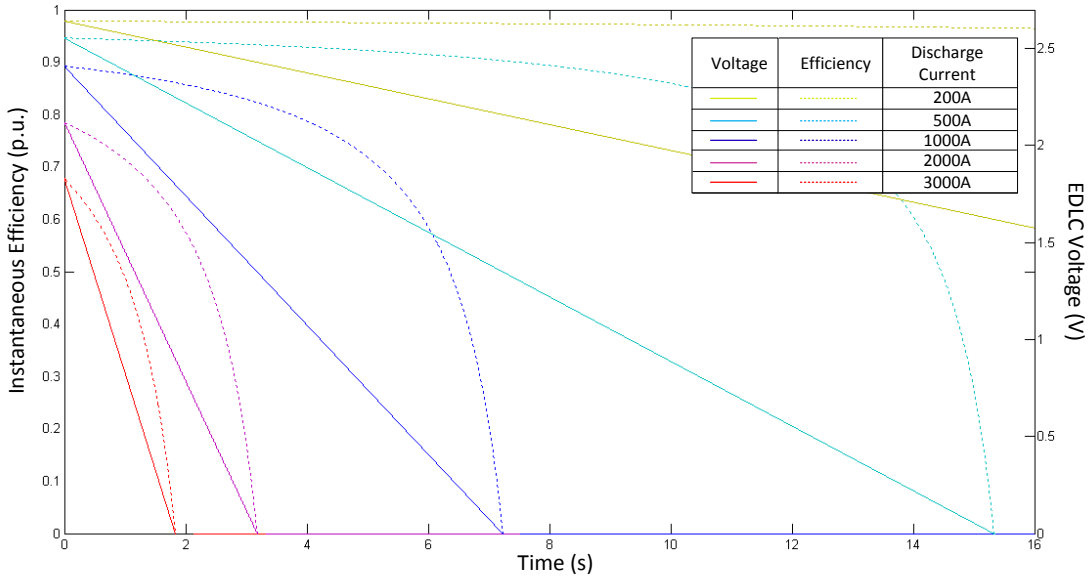

Figure 2.4 SC Constant Current Discharge Simulation Results.

Based on the simulation results, similar SC characteristics are obtained from the mathematical model. As shown in Figure 2.4, the simulation results match well with mathematical results, and the SC voltage decreases linearly under constant current conditions. The instantaneous efficiency decreases non-linearly, and the decrease rate increases as the SC voltage decreases. The discharge time and efficiency decrease as the reference current increases.

2.1.3 Constant Current Discharge Experiment Verification

The constant current discharge experiment is based on the boost converter shown in Figure 2.5, where an IGBT is used as S1. Similar to the simulation model, a PI controller is realised by the PIC micro controller which produces the gate signal for S1. By adjusting the on-state duty cycle of S1, the SC output current is maintained at the reference level. Four BCAP650s, each with 650F capacitance and 0.8mΩ internal resistance, are series connected to form one effective SC.

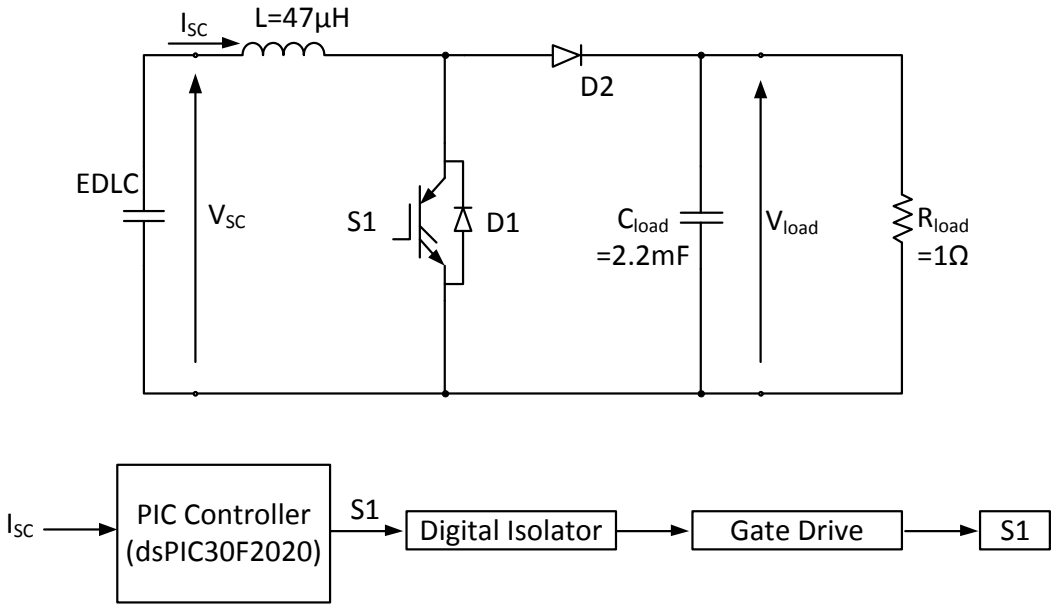

Figure 2.5 Constant Current Discharge Experiment Boost Converter.

Experiment verification is based on low current level, used to verify that the SC voltage decreases linearly under a constant current discharge condition. The SC is pre-charged to 8.5V, and the current reference is set to 8A. More detailed

experimental results on characteristic verification are shown in Chapter 4 with higher current level at rated voltage.

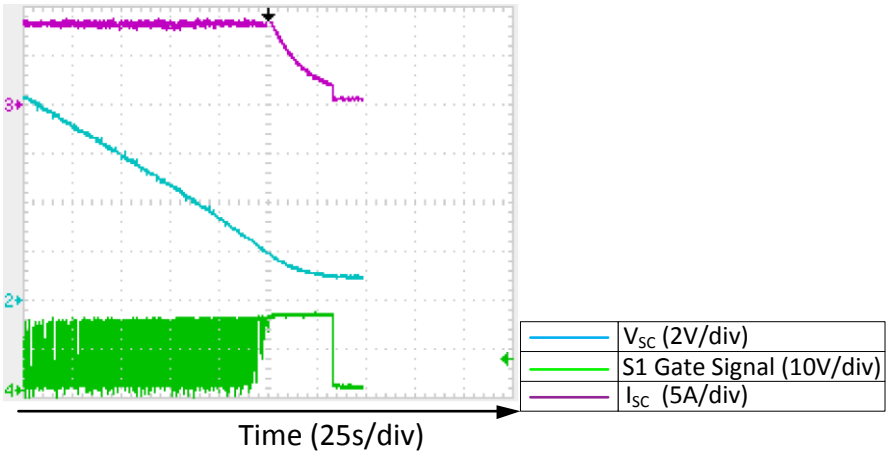

Figure 2.6 SC Constant Current Discharge Low Level Test.

The experiment result in Figure 2.6, shows the output current is maintained at the reference level 8A, and the SC voltage decreases linearly from 8V. When the SC voltage discharges to certain level, in this case about 1.7V, the current cannot be maintained constant. However, this voltage is much higher than the residual voltage as previously above, mainly due to the conduction voltage drop of the IGBT. For the constant current discharge process, the experiment result confirms the simulation and mathematical model results.

For applications where the charge/discharge process is within the SC maximum continuous current range, the SC efficiency is over 95%. However, the efficiency drops exponentially as the current level increases. For short-term applications, such as fault-ride-through where the discharge process is less than 1s, the efficiency drops down to 58% (at 2200A for BCAP3000). For such transient high current applications, the energy system needs more SCs in parallel to satisfy the current requirement. However, due to the single cell voltage limit, the SC voltage balance problem during transient conditions is challenging for system design. Different types of capacitors are investigated to parallel connect to the SC. With different capacitor characteristics, a combined energy storage system can be developed for different applications, as introduced in subsequent chapters.

2.2 Constant Power Discharge

Constant power discharge is another typical use for the SC in industry [2.11-13]. The output power of the SC is controlled to be constant during discharge until the SC voltage reaches a certain level [2.1]. A mathematical model for constant power discharge is developed based on the classic model, while simulation and experimentation are used for verification.

2.2.1 Constant Power Discharge Mathematical Modelling

Instead of using the constant current source, a voltage controlled current source is connected to the SC model as shown in Figure 2.7. As the SC discharges, the output voltage decreases and the output current increases to maintain constant output power.

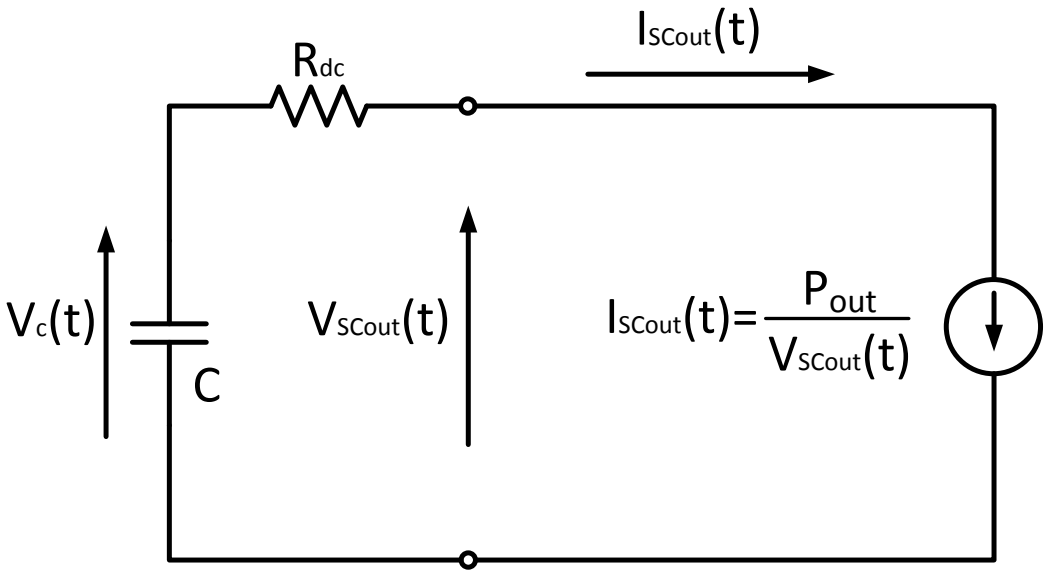

Figure 2.7 Constant Power Discharge Model.

From the electrical circuit, the following equations are developed to build the mathematical model:

Output Power of SC:

$$P_{out} = V_{SCout}(t) \cdot I_{SCout}(t) \quad \textbf{(2.24)}$$

Basic equation for the circuit is:

$$V_{SCout}(t) = V_c(t) - I_{SCout}(t) \cdot R_{dc}$$

Multiply $I_{SCout}(t)$ on both sides,

$$V_{SCout}(t) \cdot I_{SCout}(t) = V_c(t) \cdot I_{SCout}(t) - I_{SCout}(t)^2 \cdot R_{dc}$$

As defined in equation (2.24):

$$P_{out} - V_c(t) \cdot I_{SCout}(t) + I_{SCout}(t)^2 \cdot R_{dc} = 0 \quad \textbf{(2.25)}$$

Solving Equation (2.25), $I_{SCout}(t)$ in terms of $V_C(t)$ is:

$$I_{SCout}(t) = \frac{V_c(t)}{2 \cdot R_{dc}} \pm \frac{1}{2 \cdot R_{dc}} \sqrt{V_c(t)^2 - 4 \cdot P_{out} \cdot R_{dc}}$$

Since $I_{SCout}(t)$ increases as P_{out} increases, the derivative of P_{out} in terms of $I_{SCout}(t)$ should be greater than 0,

$$\frac{dP_{out}}{dI_{SCout}(t)} > 0$$

$$\frac{d}{dI_{SCout}(t)} [V_c(t) \cdot I_{SCout}(t) - I_{SCout}(t)^2 \cdot R_{dc}] > 0$$

$$I_{SCout}(t) < \frac{V_c(t)}{2 \cdot R_{dc}}$$

The SC output current $I_{SCout}(t)$ is:

$$I_{SCout}(t) = \frac{V_c(t)}{2 \cdot R_{dc}} - \frac{1}{2 \cdot R_{dc}} \sqrt{V_c(t)^2 - 4 \cdot P_{out} \cdot R_{dc}} \quad \textbf{(2.26)}$$

As $I_{SCout}(t)$ should be real

$$\therefore \Delta = V_c(t)^2 - 4 \cdot P_{out} \cdot R_{dc} > 0$$

$$\therefore V_c(t) \geq \sqrt{4 \cdot P_{out} \cdot R_{dc}}$$

The minimum capacitor voltage is:

$$V_{cmin} = 2 \cdot \sqrt{P_{out} \cdot R_{dc}} \quad \textbf{(2.27)}$$

The minimum SC voltage is:

$$V_{SCoutmin} = \frac{1}{2} \cdot V_{cmin} + \frac{1}{2} \sqrt{{V_{cmin}}^2 - 4 \cdot P_{out} \cdot R_{dc}} = \sqrt{P_{out} \cdot R_{dc}} \quad \textbf{(2.28)}$$

and the theoretical maximum power is:

$$P_{max} = \frac{{V_{rated}}^2}{4 \cdot R_{dc}} \tag{2.29}$$

where V_{rated} is the rated maximum voltage for SC

The output voltage of SC:

$$V_{SCout}(t) = V_c(t) - I_{SCout}(t) \cdot R_{dc}$$

By substituting Equation (2.26),

$$V_{SCout}(t) = \frac{1}{2} \cdot V_c(t) + \frac{1}{2}\sqrt{V_c(t)^2 - 4 \cdot P_{out} \cdot R_{dc}} \tag{2.30}$$

Transferred energy in time t is defined as:

$$E_{trans}(t) = P_{out} \cdot t \tag{2.31}$$

Transferred energy E_{trans} can also been expressed in terms of output voltage and current:

$$E_{trans}(t) = \int_0^t V_{SCout}(t) \cdot I_{SCout}(t)\, dt \tag{2.32}$$

From Equation (2.24), the capacitor voltage is:

$$V_c(t) = V_{SCout}(t) + I_{SCout}(t) \cdot R_{dc} = \frac{V_{SCout}(t)^2 + P_{out} \cdot R_{dc}}{V_{SCout}(t)} \tag{2.33}$$

By definition, equation (2.1), the SC output current $I_{SCout}(t)$ can be expressed as:

$$I_{SCout}(t) = C \cdot \frac{d\, V_c(t)}{dt}$$

By substituting equation (2.33),

$$I_{SCout}(t) = C \cdot \frac{(P_{out} \cdot R_{dc} - V_{SCout}(t)^2)}{V_{SCout}(t)^2} \cdot \frac{d\, V_{SCout}(t)}{dt} \tag{2.34}$$

Substitute equation (2.34) into equation (2.32):

$$E_{trans}(t) = \int_0^t \left[\frac{C \cdot (P_{out} \cdot R_{dc} - V_{SCout}(t)^2)}{V_{SCout}(t)}\right] d\,V_{SCout}(t)$$
$$= \frac{1}{2} C \cdot \left(2P_{out} \cdot R_{dc} \cdot ln\frac{V_{SCout}(t)}{V_{SCout}(0)} - V_{SCout}(t)^2 + V_{SCout}(0)^2\right)$$
$$where \quad \begin{cases} V_{SCout}(0) = \frac{V_c(0)}{2} + \frac{1}{2}\sqrt{V_c(0)^2 - 4 \cdot P_{out} \cdot R_{dc}} \\ V_{SCout}(t) = \frac{V_c(t)}{2} + \frac{1}{2}\sqrt{V_c(t)^2 - 4 \cdot P_{out} \cdot R_{dc}} \end{cases} \quad \textbf{(2.35)}$$

Based on equation (2.31), the expression for time *t* in terms of the SC output voltage is:

$$t = \frac{C}{2P_{out}} \cdot \left(2P_{out} \cdot R_{dc} \cdot ln\frac{V_{SCout}(t)}{V_{SCout}(0)} - V_{SCout}(t)^2 + V_{SCout}(0)^2\right)$$
$$where \quad \begin{cases} V_{SCout}(0) = \frac{V_c(0)}{2} + \frac{1}{2}\sqrt{V_c(0)^2 - 4 \cdot P_{out} \cdot R_{dc}} \\ V_{SCout}(t) = \frac{V_c(t)}{2} + \frac{1}{2}\sqrt{V_c(t)^2 - 4 \cdot P_{out} \cdot R_{dc}} \end{cases} \quad \textbf{(2.36)}$$

Since $0 < \frac{V_{SCout(t=t)}}{V_{SCout(t=0)}} < 1$, the equation (2.36) can be expended by using Maclaurin series expansion:

$$t = \frac{C}{2P_{out}} \cdot \left[2P_{out} \cdot R_{dc} \cdot \sum_{n=1}^{\infty}\left(-\frac{\left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right)^n}{n}\right) - V_{SCout}(t)^2 + V_{SCout}(0)^2\right] \quad \textbf{(2.37)}$$

For *n*=1, the first-order estimation equation is:

$$t = \frac{C}{2P_{out}} \cdot \left[-2P_{out} \cdot R_{dc} \cdot \left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right) - V_{SCout}(t)^2 + V_{SCout}(0)^2\right]$$
$$\frac{C}{2P_{out}} \cdot V_{SCout}(t)^2 - \frac{C \cdot R_{dc}}{V_{SCout}(0)} \cdot V_{SCout}(t) + \left(C \cdot R_{dc} - \frac{C}{2P_{out}} \cdot V_{SCout}(0)^2 + t\right) = 0$$

To solve output voltage $V_{SCout}(t)$, let

$$A_1 = \frac{C}{2P_{out}},\ B_1 = -\frac{C \cdot R_{dc}}{V_{SCout}(0)}\ and\ C_1 = C \cdot R_{dc} - \frac{C}{2P_{out}} \cdot V_{SCout}(0)^2 + t$$

So the first-order estimation for $V_{SCout}(t)$ is

$$V_{SCout1}(t) = \frac{-B_1 - \sqrt{{B_1}^2 - 4\,A_1 \cdot C_1}}{2\,A_1} \quad \textbf{(2.38)}$$

For n = 2, the second-order estimation equation is:

$$t = \frac{C}{2P_{out}} \cdot \left[-2P_{out} \cdot R_{dc} \cdot \left[\left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right) + \frac{1}{2}\left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right)^2 \right] - V_{SCout}(t)^2 + V_{SCout}(0)^2 \right]$$

The second-order estimation for $V_{SCout}(t)$ is:

$$V_{SCout2}(t) = \frac{-B_2 - \sqrt{{B_2}^2 - 4\,A_2 \cdot C_2}}{2\,A_2}$$

where

$$A_2 = -\left(\frac{C \cdot R_{dc}}{2{V_{(t=0)}}^2} + \frac{C}{2P_{out}}\right),\ B_2 = \frac{2C \cdot R_{dc}}{V_{(t=0)}} \quad \textbf{(2.39)}$$

$$and\ C_2 = -\frac{3}{2}C \cdot R_{dc} + \frac{C}{2P_{out}} \cdot {V_{(t=0)}}^2 - t$$

For n = 3, the third-order estimation equation is:

$$t = \frac{C}{2P_{out}} \cdot \left[V_{SCout}(0)^2 - V_{SCout}(t)^2 - 2P_{out} \cdot R_{dc} \cdot \left[\left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right) + \frac{1}{2}\left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right)^2 + \frac{1}{3}\left(1 - \frac{V_{SCout}(t)}{V_{SCout}(0)}\right)^3 \right] \right]$$

Expanding and

$$\frac{C \cdot R_{dc}}{3V_{SCout}(0)^3} \cdot V_{SCout}(t)^3 - \left(\frac{3C \cdot R_{dc}}{2V_{SCout}(0)^2} + \frac{C}{2P_{out}}\right) \cdot V_{SCout}(t)^2 + \frac{3C \cdot R_{dc}}{V_{SCout}(0)} \cdot V_{SCout}(t) + \left(-\frac{11}{6}C \cdot R_{dc} + \frac{C}{2P_{out}} \cdot V_{SCout}(0)^2 - t\right) = 0$$

Let

$$A_3 = \frac{C \cdot R_{dc}}{3V_{SCout}(0)^3},\ B_3 = -\left(\frac{3C \cdot R_{dc}}{2V_{SCout}(0)^2} + \frac{C}{2P_{out}}\right), C_3 = \frac{3C \cdot R_{dc}}{V_{SCout}(0)},$$

$$D_3 = -\frac{11}{6}C \cdot R_{dc} + \frac{C}{2P_{out}} \cdot V_{SCout}(0)^2 - t;$$

$$a_0 = \frac{D_3}{A_3},\ a_1 = \frac{C_3}{A_3},\ a_2 = \frac{B_3}{A_3};$$

$$q = \frac{1}{3}\ a_1 - \frac{1}{9}\ {a_2}^2, r = \frac{1}{6}\ a_1 \cdot\ a_2 - 3\ a_0 - \frac{1}{27}\ {a_2}^3;$$

$$S_1 = \sqrt[3]{r + \sqrt{q^3 + r^2}}\ and\ S_2 = \sqrt[3]{r - \sqrt{q^3 + r^2}}$$

The third-order estimation for $V_{SCout}(t)$ is:

$$V_{SCout3}(t) = -\frac{1}{2}(S_1 + S_2) - \frac{a_2}{3} - \frac{i\sqrt{3}}{2} \cdot (S_1 - S_2) \quad \textbf{(2.40)}$$

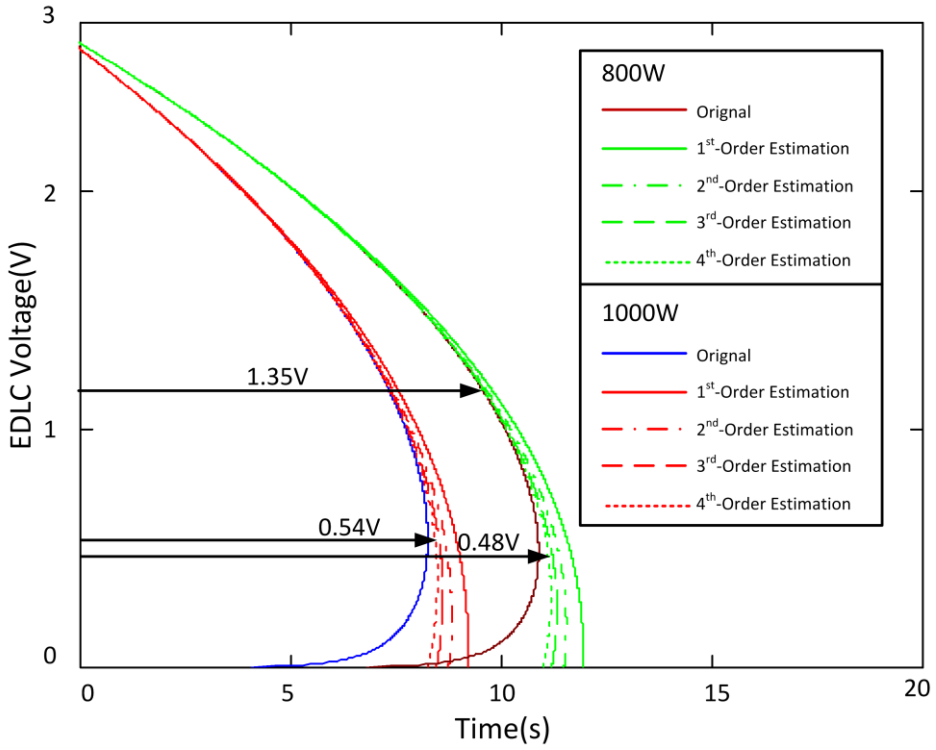

Figure 2.8 Original and Estimated Equation Plot for SC Constant Power Discharge.

Figure 2.8 compares plots based on the original equation and the estimated equations under 800W and 1000W constant power discharge conditions. The higher order estimated equation has the higher accuracy.

Based on equations (2.28) and (2.27), there is a minimum voltage for a constant power discharge condition. According to Figure 2.8, the estimated equation plot fits well with the original plot within the first half of the discharge range, where the SC is usually applied in practice. Considering model complexity, the second-order estimation equation (2.39) is selected, which has valid real solutions covering the whole constant power discharge range.

Based on the previous equations, the following characteristic analysis is developed using the second-order SC output voltage estimation shown in equation (2.39):

1. Instantaneous Output Current

$$I_{SCout}(t) = \frac{P_{out}}{V_{SCout}(t)} \quad \textbf{(2.41)}$$

where $V_{SCout}(t)$ *is defined by the estimation equation (2.39)*

2. Instantaneous Efficiency

$$\eta(t) = \frac{P_{out}}{P_{out} + P_{loss}} \quad \textbf{(2.42)}$$

where

$$P_{loss} = I_{SCout}(t)^2 \cdot R_{dc} = \left(\frac{P_{out}}{V_{SCout}(t)}\right)^2 \cdot R_{dc}$$

3. Constant Power Discharge Time, which is defined as the time for capacitor constant power discharge to reach its minimal value. By substituting equation (2.28) into equation (2.36), the Constant Power Discharge Time can be expressed as:

$$T_{cpdis} = \frac{C}{2P_{out}} \cdot \left(2P_{out} \cdot R_{dc} \cdot ln\frac{V_{SCoutmin}}{V_{SCout}(0)} - {V_{SCoutmin}}^2 + V_{SCout}(0)^2\right) \quad \textbf{(2.43)}$$

4. Energy Transfer Efficiency

$$\eta_{transfer}(P_{out}) = \frac{E_{trans}}{E_{total}} = \frac{P_{out} \cdot T_{cpdis}}{\frac{1}{2} C \cdot V_{SCout}(0)^2} \quad \textbf{(2.44)}$$

5. Energy Loss Percentage

$$\eta_{loss}(P_{out}) = \frac{E_{loss}}{E_{total}} = \frac{\frac{1}{2} C \cdot V_{SCout}(0)^2 - P_{out} \cdot T_{cpdis} - \frac{1}{2} C \cdot {V_{cmin}}^2}{\frac{1}{2} C \cdot V_{SCout}(0)^2} \quad \textbf{(2.45)}$$

6. Residual Voltage

$$V_{residual} = V_{cmin} = 2 \cdot \sqrt{P_{out} \cdot R_{dc}} \quad \textbf{(2.46)}$$

7. Transfer Efficiency for 50% Discharging:

Assuming the initial SC voltage $V_C(0)$ is its rated maximum voltage V_{rated}, the discharge time for the SC voltage $V_{SCout}(t)$ discharge to 50% of V_{rated} is

$$T_{cpdis50\%} = R_{dc} \cdot C \cdot ln\frac{1}{2} + 0.75{V_{rated}}^2 \cdot \frac{C}{2P_{out}} \quad \textbf{(2.47)}$$

Transferred energy in time $T_{cpdis50\%}$ is:

$$E_{trans50\%} = P_{out} \cdot T_{cpdis50\%} \quad \textbf{(2.48)}$$

Total energy stored in SC at an initial voltage of V_{rated}:

$$E_{total} = \frac{1}{2} C \cdot {V_{rated}}^2 \quad \textbf{(2.49)}$$

The Energy Transfer Efficiency is:

$$\eta_{transfer50\%}(I_{out}) = \frac{E_{trans50\%}}{E_{total}} \quad \textbf{(2.50)}$$

Based on the BCAP3000 datasheet, similar to Figure 2.2, Four-Quarter characteristics plotted under constant power discharge are shown in Figure 2.9.

Based on the four quadrants in Figure 2.9, the constant power discharge characteristics are summarised as follows:

1. First quadrant: the decrease rate of the SC voltage increases with time (equation (2.39)). The Instantaneous Efficiency decreases smoothly as the SC discharging from rated voltage to half, and then deceases exponentially (equation (2.42)).
2. Second quadrant: Constant Power Discharge Time (equation (2.43)) and Energy Transfer Efficiency (equation (2.44)) decrease as the reference power increases. Energy Loss Percentage (equation (2.45)) increases as the reference power increases in the low power range, while in high power range it decreases due to more residual energy stored in the SC.
3. Third quadrant: The Residual Voltage increases as the reference power increases (equation (2.46)).
4. Fourth quadrant: Instantaneous current decreases smoothly as the SC discharges from rated voltage to half, and then deceases exponentially (equation (2.41)).

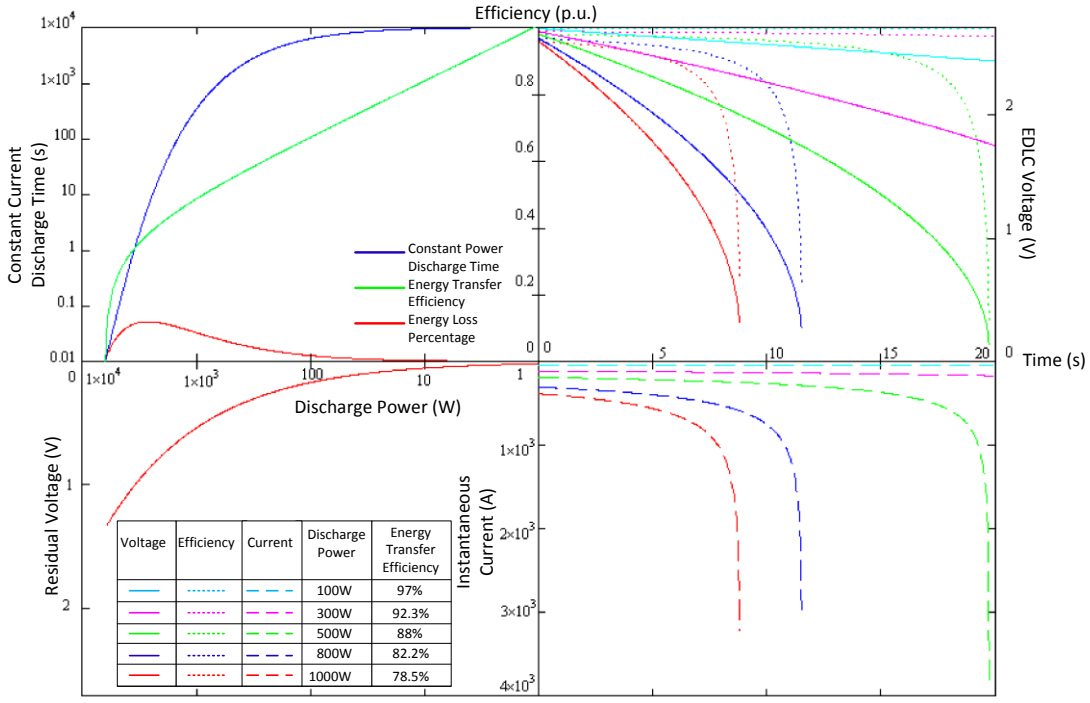

Figure 2.9 Four-Quadrant Constant Power Discharge Characteristic Plot for BCAP3000.

The developed mathematical model for SC constant power discharge indicates the SC output current increases exponentially as the SC discharges. As the SC requires an external converter for energy flow control, the increased current level

during constant power discharge is an important issue for device selection. Furthermore, the increased current leads to higher energy loss, while at the SC energy storage system design stage, choosing a proper voltage discharge range for constant power discharge is critical for system efficiency. The model can be extended for analysing different types of capacitors which have a similar series resistor and capacitor topology.

2.2.2 Constant Power Discharge Simulation Verification

The Matlab/Simulink simulation model for constant power discharge is similar to the constant current model, where a boost converter with a switching frequency of 40kHz is adopted. By sensing the inductor current and the SC output voltage, the output power of the capacitor can be calculated and regulated by the PI controller. The PI controller generates the PWM duty cycle, which provide the switch control signal to drive the ideal switch as shown in Figure 2.10. The model is based on the Maxwell BCAP3000 SC with a capacitance of 3000F and internal resistance of 0.29mΩ, at 2.7V. The instantaneous efficiency is calculated from equation (2.42).

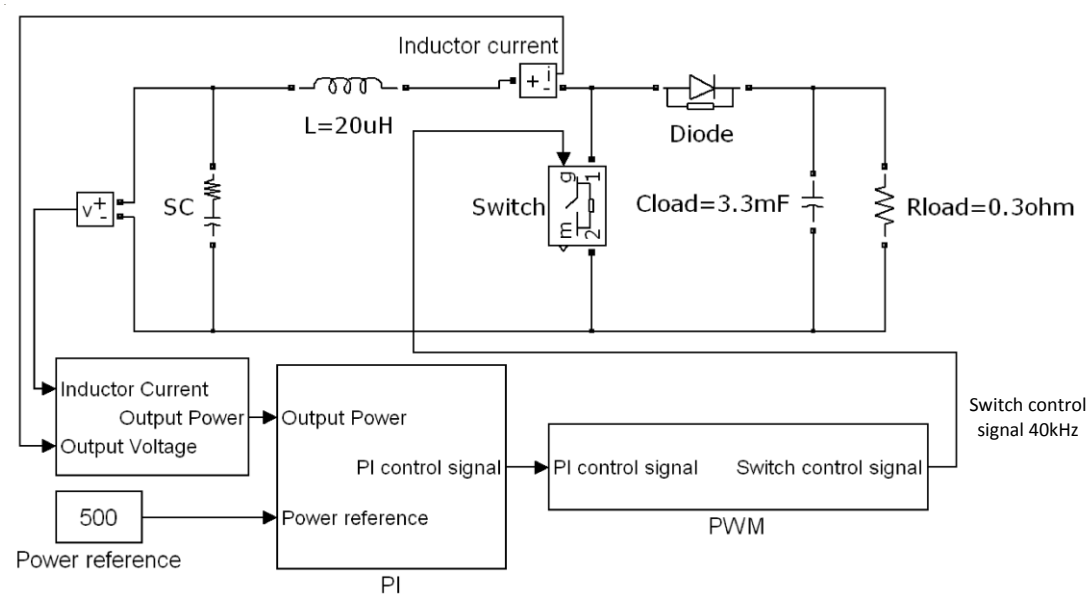

Figure 2.10 Constant Power Simulation Model.

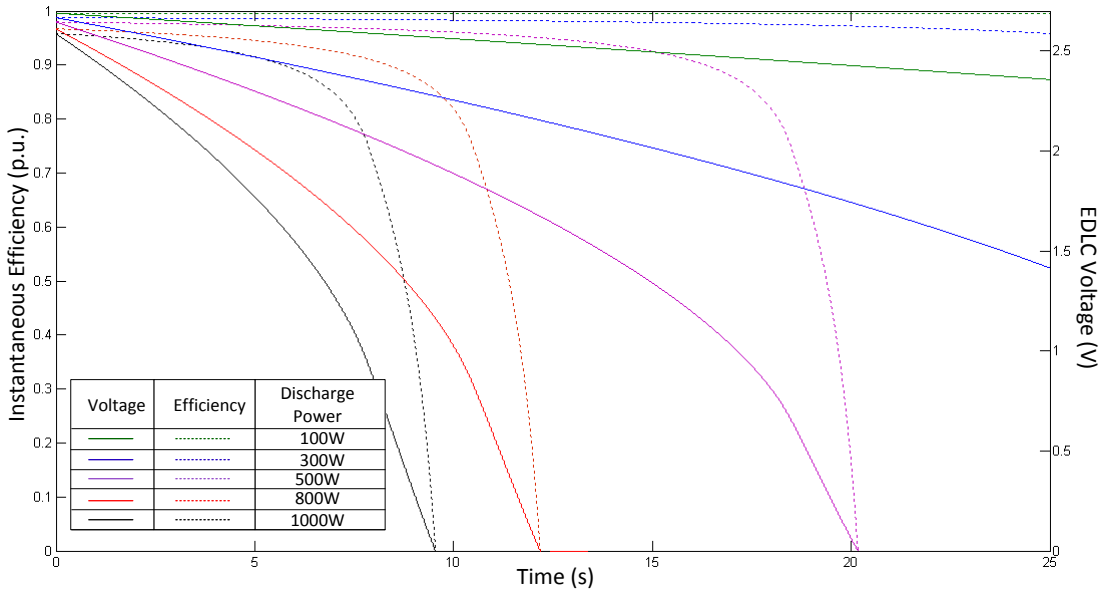

Figure 2.11 SC Constant Power Discharge Simulation Results.

The simulation results based on different reference power levels are shown in Figure 2.11. These simulation results match well with the results from the mathematical model shown in Figure 2.9, where the decrease rate of the SC voltage and instantaneous efficiency increases with time.

2.2.3 Constant Power Discharge Experiment Verification

The constant power discharge experiment is based the same circuit as in Figure 2.5. The SC output voltage and current are monitored to calculate the instant output power. Based on the PI control algorithm, the PIC micro controller produces the gate signal for S1 at the required duty cycle.

The experimental verification is based on a low power level, and verifies the SC voltage and current variation characteristic under the constant power discharge condition. The SC is pre-charged to 6V, and the power reference is set to 40W.

The experimental result in Figure 2.12 shows the output power is maintained at 40W, which is the reference power set by the control algorithm. The SC voltage decreases non-linearly, and the decrease rate increased as the voltage decreases. Due to the increased current level, the residual voltage is about ½V higher than the constant

current condition. The experimental result confirms the simulation and mathematical model results.

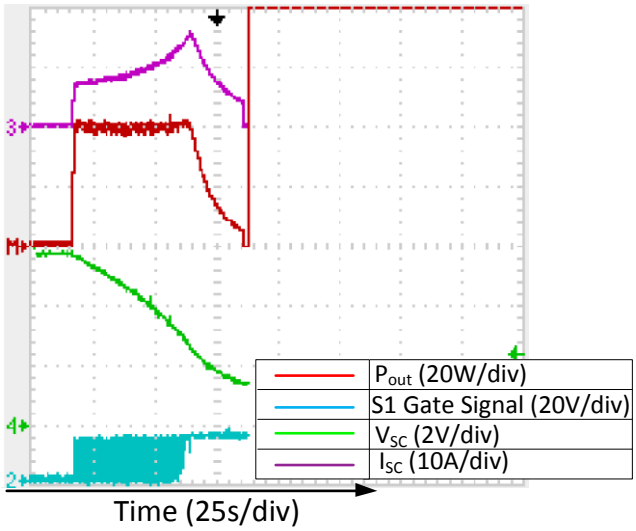

Figure 2.12 SC Constant Current Discharge Low Level Test.

For SC constant power discharge, due to the nonlinear variation of the current and voltage, the mathematical model and control strategy are more complicated than that for a constant current condition. As mentioned, the exponentially increasing current at low voltage can cause problems for the external converter devices and lowers the efficiency which needs to be stressed during the overall energy system design.

2.3 Triangle Wave Current Discharge

For typical SC applications, especially medium to high power energy storage systems, a dc/dc converter is required for controlling SC charging and discharging. In practice, most dc/dc converters are unable to produce the ideal constant current assumed previously. The boost converter, which is normally used for SC discharging [2.14-16], is selected to analyse the effects of non-ideal current on SC efficiency characteristics. The SC output current, when connected to a boost converter, can be considered as a triangle wave. Depending on the current level and inductor size, the converter works in an inductor current continuous or discontinuous mode. The mathematical models for these two different modes are developed for SC efficiency analysis.

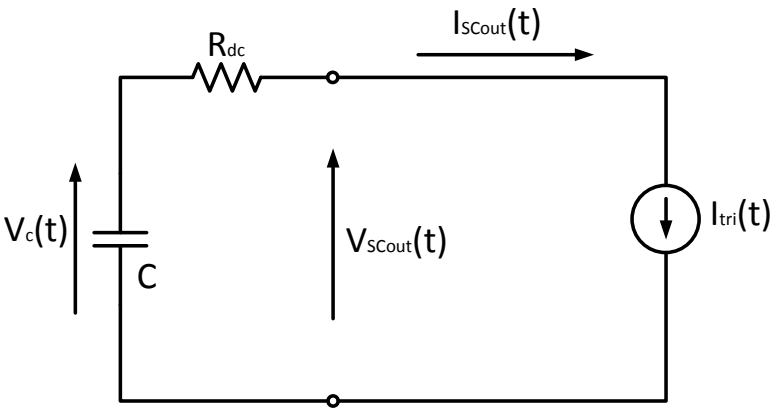

Figure 2.13 Triangle Wave Current Discharge Model.

The Triangle Wave Current Discharge Mathematical Model is similar to the constant current discharge model, where the constant current source is replaced by a triangle wave current source. A single resistor and capacitor (RC) branch model is used to represent the SC, where the circuit model is shown in Figure 2.13.

2.3.1 Continuous Conduction Mode

In a continuous triangle wave current discharge mode, the SC discharges with the current waveform defined in Figure 2.14. The current is based on an offset current with the ripple current at a specified frequency and magnitude.

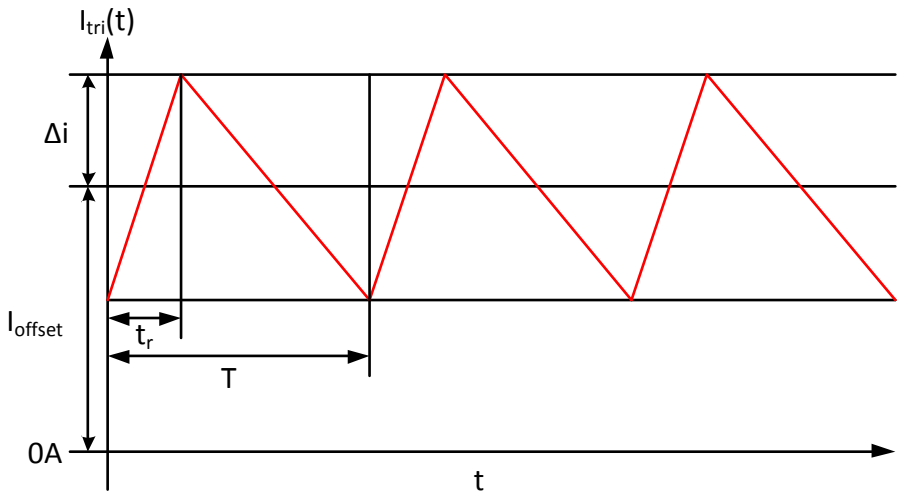

Figure 2.14 Continuous Triangle Wave Current.

The triangle current in continuous conduction mode can be expressed as:

$$I_{tri}(t) = \begin{cases} 2\Delta i \dfrac{t - T \cdot INT\left(\frac{t}{T}\right)}{t_r} + I_{offset} - \Delta i, 0 \le t - T \cdot INT\left(\frac{t}{T}\right) \le \\ 2\Delta i \dfrac{t - T \cdot INT\left(\frac{t}{T}\right) - t_r}{t_r - T} + I_{offset} + \Delta i, t_r < t - T \cdot INT\left(\frac{t}{T}\right) < \end{cases} \quad \textbf{(2.51)}$$

where $INT\left(\frac{t}{T}\right)$ *refers to the number of whole period* T *within time* t

In equation (2.51), Δi is the ripple current, I_{offset} is the offset current, t_r is the rise time and T is the fundamental period. For a boost converter, the duty cycle is defined as:

$$Duty = \frac{t_r}{T}$$

From Figure 2.13, the following equations are used to build the mathematical model:

The SC output voltage:

$$V_{SCout}(t) = V_c(t) - I_{tri}(t) \cdot R_{dc} = V_{co} - \int_0^t \frac{I_{tri}(t)}{C} dt - I_{tri}(t) \cdot R_{dc} \quad \textbf{(2.52)}$$

where $t \in [0, T_{tridis}]$

With the triangle wave current definition, a similar discharge characteristic as the constant current discharge is obtained. To simplify the model, the boundary condition for the triangle wave current is calculated based on a constant current discharge model with a reference current of I_{offset}.

The residual voltage is:

$$V_{residual} = V_c(T_{tridis}) = I_{offset} \cdot R_{dc} \quad \textbf{(2.53)}$$

The allowed discharge time T_{tridis} for an SC in terms of discharge current is:

$$T_{tridis}(I_{offset}) = \frac{C}{I_{offset}} \cdot \left(V_c(0) - I_{offset} \cdot R_{dc}\right) = \frac{Q(0)}{I_{offset}} - \tau \quad \textbf{(2.54)}$$

where $Q(0)$ *is the initial electric charge, and* τ *is the SC time constant.*

Inversely, the offset current reference I_{offset} in terms of T_{tridis} is:

$$I_{offset}(T_{tridis}) = \frac{C \cdot V_c(0)}{T_{tridis} + C \cdot R_{dc}} \quad \textbf{(2.55)}$$

The residual voltage in terms of T_{tridis} is:

$$V_{residual}(T_{tridis}) = I_{offset}(T_{tridis}) \cdot R_{dc} = \frac{C \cdot V_c(0) \cdot R_{dc}}{T_{tridis} + C \cdot R_{dc}} = \frac{V_c(0) \cdot \tau}{T_{tridis} + \tau} \quad \textbf{(2.56)}$$

Based on this basic equation, the following useful parameters for characteristic analysis can be derived:

1. Instantaneous Power:

$$P(t) = V_{SCout}(t) \cdot I_{tri}(t) = (V_{co} - \int_0^t \frac{I_{tri}(t)}{C} dt - I_{tri}(t) \cdot R_{dc}) \cdot I_{tri}(t) \quad \textbf{(2.57)}$$

2. Instantaneous Efficiency:

$$\eta(t) = \frac{P_{tri}(t)}{P_{tri}(t) + P_{loss}} = \frac{V_{SCout}(t)}{V_{SCout}(t) + I_{tri}(t) \cdot R_{dc}} \quad \textbf{(2.58)}$$

3. Energy Transfer Efficiency:

$$\eta_{transfer} = \frac{E_{total} - E_{loss} - E_{residual}}{E_{total}}$$

Energy loss on R_{dc}:

$$E_{loss} = \int_0^{T_{tridis}} I_{tri}(t)^2 \cdot R_{dc}\, dt$$

Calculating E_{loss} can be divided into two parts, which are Rising Current integration and Falling Current integration:

$$\begin{cases} E_{Rising}(t) = \int_0^t \left[\frac{2 \cdot \Delta i}{t_r} \cdot t + \left(I_{offset} - \Delta i\right)\right]^2 \cdot R_{dc} dt\,, & 0 \le t \le t_r \\ E_{Falling}(t) = \int_0^t \left[-\frac{2 \cdot \Delta i}{T - t_r} \cdot t + \left(I_{offset} + \Delta i\right)\right]^2 \cdot R_{dc} dt\,, & t_r < t < T \end{cases}$$

The energy loss for one period *T* can be calculated as:

$$E_{loss}(T) = E_{Rising}(t) + E_{Falling}(T - t_r) = \left(\frac{1}{3} \cdot \Delta i^2 \cdot T + {I_{offset}}^2 \cdot T\right) \cdot R_{dc} \quad \textbf{(2.59)}$$

Equation (2.59) indicates that the energy loss in one period is independent of t_r, specifically duty cycle.

The overall energy loss in R_{dc} can be calculated as a piecewise function:

$$E_{loss}(T_{tridis}) = \begin{cases} N \cdot E_{loss}(T) + E_{Rising}(T_{tridis} - N \cdot T) \\ \quad for\ 0 \leq T_{tridis} - N \cdot T \leq t_r \\ N \cdot E_{loss}(T) + E_{Rising}(t_1) + E_{Falling}(T_{tridis} - t_r - N \cdot T) \\ \quad for\ t_r \leq T_{tridis} - N \cdot T \leq T \end{cases} \quad \textbf{(2.60)}$$

where N is the number of whole cycles during T_{tridis}

Residual energy in SC:

$$E_{residual} = \frac{1}{2} C \cdot V_{residual}(T_{tridis})^2 = \frac{1}{2} C \cdot {I_{offset}}^2 \cdot {R_{dc}}^2 \quad \textbf{(2.61)}$$

The Energy Transfer Efficiency is:

$$\eta_{transfer} = 1 - \frac{E_{loss}(T_{tridis})}{\frac{1}{2} C \cdot V_c(0)^2} + \frac{{I_{offset}}^2 \cdot {R_{dc}}^2}{V_c(0)^2} \quad \textbf{(2.62)}$$

4. Energy Loss Percentage:

$$\eta_{loss} = \frac{E_{loss}}{E_{total}} = \frac{E_{loss}(T_{tridis})}{\frac{1}{2} C \cdot V_c(0)^2} \quad \textbf{(2.63)}$$

According to the mathematical model, the following discharge characteristics can be summarised:

1. Increasing offset current results in lower transfer efficiency, equation 2.62.
2. Increasing ripple current level results in lower transfer efficiency, equation 2.62.

For the boost converter, one factor that determines the ripple current is the input inductance, where a correctly designed inductor can slightly increase the transfer efficiency.

Based on the BCAP3000 P270 SC datasheet, the energy transfer efficiency plots with different ripple current level, are shown in Figure 2.15.

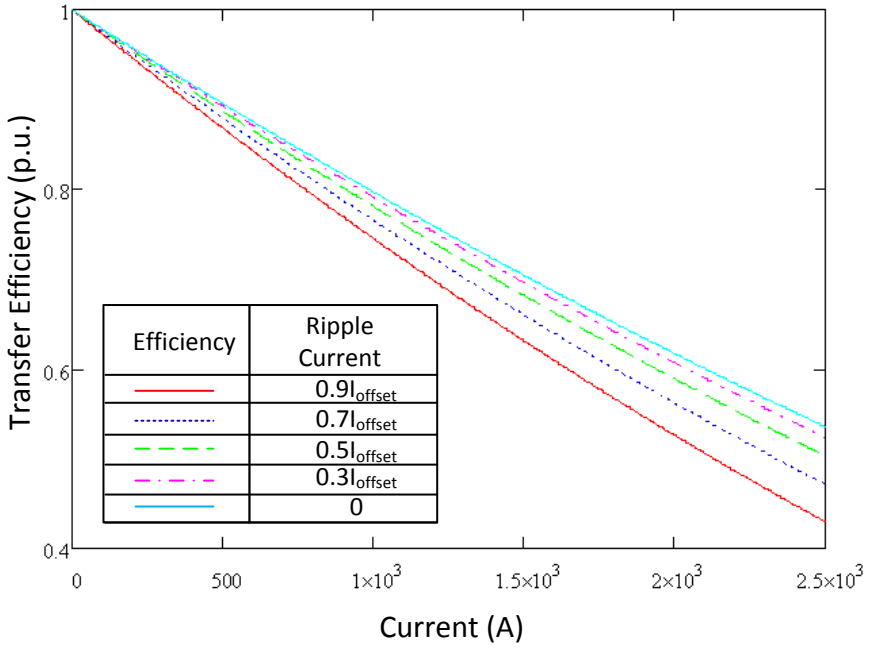

Figure 2.15 Triangle Wave Continuous Current Discharge with Different Ripple Current Level at 40kHz Half Duty.

As the efficiency plots in Figure 2.15 show, the transfer efficiency difference between the ideal constant current and other triangle wave continuous conduction currents with different ripple level, is less than 1% of the offset current, when less than the SC maximum continuous current (210A for BCAP3000). As a result, the general efficiency estimation for the triangle wave continuous conduction current within the SC maximum continuous current range can be simplified as the constant current discharge. For high-level triangle-wave continuous conduction current discharge, the transfer efficiency can be estimated using a correction coefficient. The correction coefficient is defined as the ratio of the efficiency at different ripple level with the efficiency of the ideal constant current discharge at specified offset current. For given offset current I_{offset} and ripple current values, the efficiency can be calculated by multiplying the correction coefficient and the efficiency at constant discharging current of I_{offset}.

2.3.2 Discontinuous Conduction Mode

The discontinuous triangle wave current discharge model is based on the circuit shown in Figure 2.13, where the triangle wave current source is defined by the waveform shown in Figure 2.16.

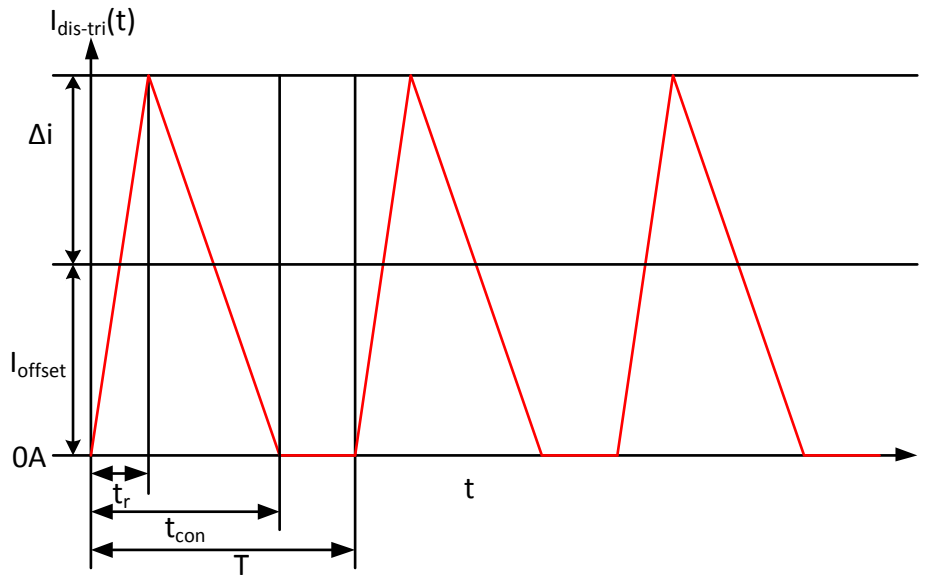

Figure 2.16 Discontinuous Triangle Wave Current.

As shown in Figure 2.16, the offset current I_{offset} equals to the ripple current Δi, and there is a discontinuous period where the SC current is 0A. The discontinuous period:

$$T_{dis} = T - t_{con} \tag{2.64}$$

The discontinuous triangle wave current is expressed as:

$$I_{dis-tri}(t) = \begin{cases} 2I_{offset}\dfrac{t - T \cdot INT\left(\frac{t}{T}\right)}{t_r}, & 0 \le t - T \cdot INT\left(\frac{t}{T}\right) \le t_r \\ 2I_{offset}\dfrac{t - T \cdot INT\left(\frac{t}{T}\right) - t_{con}}{t_r - t_{con}}, & t_r < t - T \cdot INT\left(\frac{t}{T}\right) \le t_{con} \\ 0, & t_{con} < t - T \cdot INT\left(\frac{t}{T}\right) < T \end{cases} \tag{2.65}$$

where $INT\left(\frac{t}{T}\right)$ *refers to the number of whole period* T *within time* t

Again, the duty cycle is defined as:

$$Duty = \frac{t_r}{t_{con}}$$

From the circuit in Figure 2.13, the following equations are used to develop the mathematical model:

The SC output voltage:

$$\begin{aligned} V_{SCout}(t) &= V_c(t) - I_{dis-tri}(t) \cdot R_{dc} \\ &= V_{co} - \int_0^t \frac{I_{dis-tri}(t)}{C} dt - I_{dis-tri}(t) \cdot R_{dc} \end{aligned} \quad \textbf{(2.66)}$$

$$where\ t \in [0, T_{dis-tridis}]$$

Similar to the continuous conduction mode, the boundary for discharge occurs when the voltage across the internal resistor equals the capacitor voltage. The residual voltage is defined as:

$$V_{residual} = V_c(T_{dis-tridis}) = \ I_{offset} \cdot R_{dc} \quad \textbf{(2.67)}$$

The allowed discharge time $T_{dis\text{-}tridis}$ for an SC in terms of discharge current is:

$$\begin{aligned} T_{dis-tridis}(\ I_{offset}) &= \frac{C}{\frac{t_{con}}{T} \cdot I_{offset}} \cdot \left(V_c(0) - I_{offset} \cdot R_{dc}\right) \\ &= \frac{T}{t_{con}} \cdot \left(\frac{Q_0}{I_{offset}} - \tau\right) \end{aligned} \quad \textbf{(2.68)}$$

Inversely, the offset current reference I_{offset} in terms of $T_{dis\text{-}tridis}$ is:

$$I_{offset}(\ T_{dis-tridis}) = \frac{C \cdot V_c(0)}{\frac{t_{con}}{T} \cdot T_{dis-tridis} + C \cdot R_{dc}} \quad \textbf{(2.69)}$$

The residual voltage in terms of $T_{dis\text{-}tridis}$ is:

$$\begin{aligned} V_{residual}(\ T_{dis-tridis}) &= \frac{C \cdot V_c(0) \cdot R_{dc}}{\frac{t_{con}}{T} \cdot T_{dis-tridis} + C \cdot R_{dc}} \\ &= \frac{V_c(0) \cdot \tau}{\frac{t_{con}}{T} \cdot T_{dis-tridis} + \tau} \end{aligned} \quad \textbf{(2.70)}$$

Based on this basic equation, the following useful parameters for characteristic analysis can be developed:

1. Instantaneous Power:

$$P_{dis-tri}(t) = V_{SCout}(t) \cdot I_{dis-tri}(t)$$
$$= \left(V_c(0) - \int_0^t \frac{I_{dis-tri}(t)}{C} dt - I_{dis-tri}(t) \cdot R_{dc}\right) \cdot I_{dis-tri}(t) \quad \textbf{(2.71)}$$

2. Instantaneous Efficiency:

$$\eta(t) = \frac{P_{dis-tri}(t)}{P_{dis-tri}(t) + P_{loss}} = \frac{V_{SCout}(t)}{V_{SCout}(t) + I_{dis-tri}(t) \cdot R_{dc}} \quad \textbf{(2.72)}$$

3. Energy Transfer Efficiency:

$$\eta_{transfer} = \frac{E_{total} - E_{loss} - E_{residual}}{E_{total}}$$

Energy loss on R_{dc}:

$$E_{loss} = \int_0^{T_{dis-tridis}} I_{dis-tri}(t)^2 \cdot R_{dc}\, dt$$

Calculating E_{loss} can be divided into three parts, which are Rising Current integration, Falling Current integration and 0 for the discontinuous duration:

$$\begin{cases} E_{Rising}(t) = \int_0^t \left[\frac{2I_{offset}}{t_r} \cdot t\right]^2 \cdot R_{dc} dt\,, & 0 \le t \le t_r \\ E_{Falling}(t) = \int_0^t \left[-\frac{2I_{offset}}{t_{con} - t_r} \cdot t + 2I_{offset}\right]^2 \cdot R_{dc} dt, & t_r < t < t_{con} \\ 0, & t_{con} < t < T \end{cases}$$

The energy loss for one period T can be calculated as:

$$E_{loss}(T) = E_{Rising}(t_r) + E_{Falling}(t_{con} - t_r) + 0 = \left(\frac{4}{3} {I_{offset}}^2 \cdot t_{con}\right) \cdot R_{dc} \quad \textbf{(2.73)}$$

Equation (2.73) indicates that the energy loss in one period depends on t_2, which is the current conduction duration.

The overall energy loss on R_{dc} can be calculated as a piecewise function:

$$E_{loss}(T_{dis-tridis}) =$$

$$\begin{cases} N \cdot E_{loss}(T) + E_{Rising}(T_{dis-tridis} - N \cdot T), \\ for\ 0 \leq T_{dis-tridis} - N \cdot T \leq t_r \\ N \cdot E_{loss}(T) + E_{Rising}(t_r) + E_{Falling}(T_{dis-tridis} - t_r - N \cdot T), \\ for\ t_r \leq T_{dis-tridis} - N \cdot T \leq t_{con} \\ N \cdot E_{loss}(T), \\ for\ t_{con} \leq T_{dis-tridis} - N \cdot T \leq T \end{cases} \quad \textbf{(2.74)}$$

where N is the number of whole cycles during $T_{dis-tridis}$

SC Residual energy:

$$V_{residual}(T_{dis-tridis}) = \frac{1}{2} C \cdot {V_{residual}}^2 = \frac{1}{2} C \cdot {I_{offset}}^2 \cdot {R_{dc}}^2 \quad \textbf{(2.75)}$$

The Energy Transfer Efficiency is:

$$\eta_{transfer} = 1 - \frac{E_{loss}(T_{dis-tridis})}{\frac{1}{2} C \cdot V_c(0)^2} - \frac{{I_{offset}}^2 \cdot {R_{dc}}^2}{V_c(0)^2} \quad \textbf{(2.76)}$$

4. Energy Loss Percentage:

$$\eta_{loss} = \frac{E_{loss}}{E_{total}} = \frac{E_{loss}(T_{dis-tridis})}{\frac{1}{2} C \cdot V_c(0)^2} \quad \textbf{(2.77)}$$

Based on the mathematical model, the following discharge characteristics can be summarised:

1. Increasing offset current results in lower transfer efficiency, equation (2.76).
2. The allowed discharge time increases as the discontinuous duration increases.
3. Transfer efficiency is independent of discontinuous duration and duty cycle.

Based on BCAP3000 P270 SC datasheet, the energy transfer efficiency plots with different discontinuous time are shown in Figure 2.17.

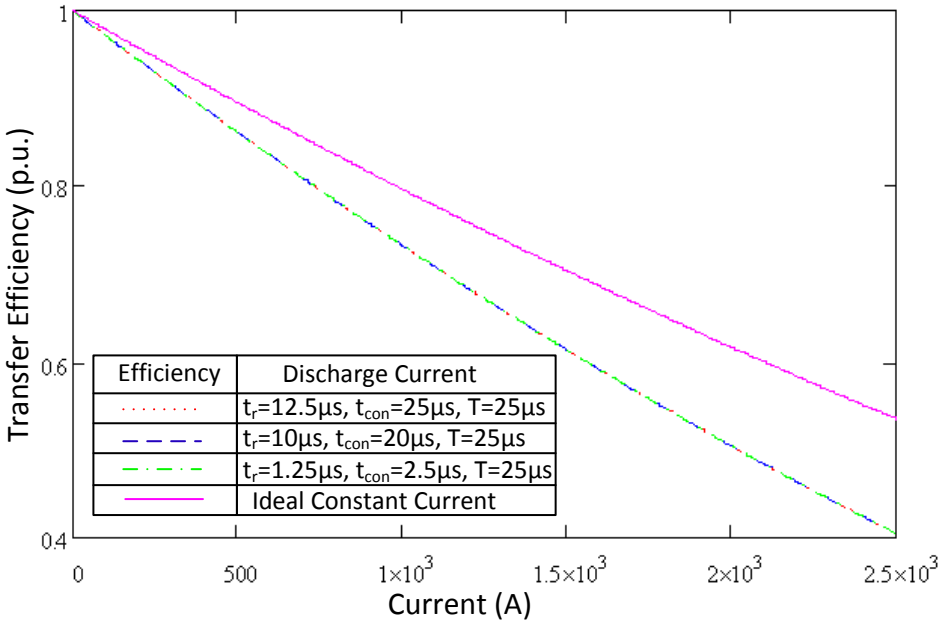

Figure 2.17 Discontinuous Triangle Wave Current Discharge with Different Discontinuous Duration at a Switching Frequency of 40kHz and 50% Duty.

As the efficiency plot in Figure 2.17 shows, the transfer efficiency difference between the ideal constant current and the discontinuous triangle wave currents is larger than the difference for the continuous condition with low ripple level. The efficiency for the discontinuous condition is independent of the discontinuous duration, which is identical to the continuous condition with the ripple current equal to the offset current. Again a correction coefficient approach can be applied for high level current transfer efficiency estimation.

According to the mathematical analysis, the efficiency estimation for triangle wave current discharge condition can be divided into two approaches based on the offset current and ripple level. For low offset current, which is normally within the maximum continuous current, as defined in the SC datasheet, the efficiency can be simplified to be based on an ideal constant current condition. For higher offset current with a high ripple level, the efficiency can be estimated by the correction coefficient approach as introduced in continuous conduction Mode.

2.4 Bidirectional Buck/Boost Converter Charge and Discharge

Bidirectional dc/dc converters which have fewer devices, lower cost and higher efficiency are widely applied in bidirectional energy transfer systems [2.16]. In many applications, such as uninterruptible power supplies, hybrid electric vehicles, fuel cell power systems, and solar cell power systems, the bidirectional converter is used as the key part for controlling the energy flow between the energy storage system and the dc link [2.15]. Due to its simplicity and robustness, the bidirectional buck/boost converter is often selected in combination with the supercapacitor for the energy storage system demonstration [2.14, 17]. The basic topology and operation principle of the bidirectional buck/boost converter will be explained, and an experiment to verify bidirectional energy flow control ability is included.

2.4.1 Bidirectional Buck/Boost Converter

The basic topology for bidirectional buck/boost converter is shown in Figure 2.18 and is developed based on Switched-Mode Power Supply (SMPS) technology. By switching S1 and S2, the converter can work either as a boost converter to discharge the SC, or a buck converter to charge the SC. The control objective is to maintain the voltage of the dc bus constant.

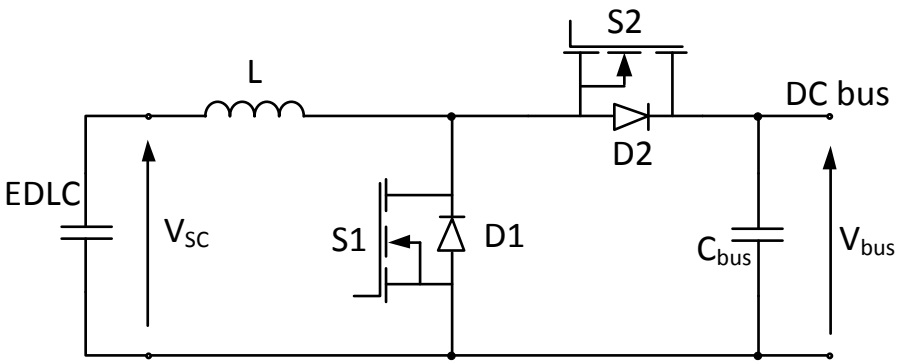

Figure 2.18 Bidirectional Buck-Boost Converter.

As V_{bus} lower than the reference value, the converter works at boost mode, where energy is transferred from the SC to the dc bus. S2 is disabled, and S1 is switched on and off at required duty cycle. When S1 is on, energy is transferred from SC to

inductor; when S1 is off, energy stored in both SC and inductor is transferred to dc bus through D2.

When V_{bus} is higher than the reference, the converter operates in the buck mode, where energy is transferred from the dc bus to the SC. S1 is disabled, and S2 is switched on and off with required duty cycle. When S2 is on, energy is transferred from dc bus to the inductor and the SC; when S2 is off, energy stored in inductor is transferred to the SC through D1.

2.4.2 Bidirectional Buck/Boost Converter Constant Output Voltage Experiment Verification

To verify the bidirectional buck/boost converter topology, the converter is connected to a variable load with a current source. By controlling the energy flow between the SC and the current source, the converter is used to maintain the load voltage at 12V. As shown in Figure 2.19, the paralleled resistors R_1 and R_2, of 1Ω each, is used as the variable load. By switching on S3, the load resistance is varied from 1Ω to 0.5Ω. The parallel connected diode is freewheel diode.

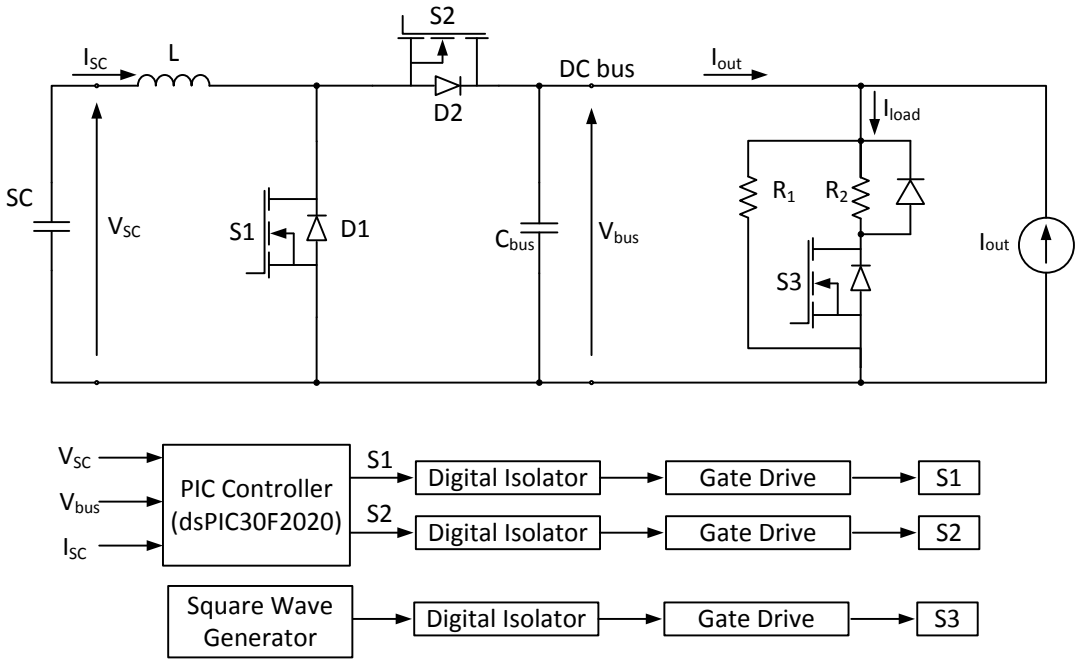

Figure 2.19 Bidirectional Buck-Boost Converter with Variable Load Experiment.

By comparing the dc bus voltage V_{bus} with the reference voltage, the converter operates in either a boost or buck mode. However, there is maximum and minimum voltage limit for the SC. In the buck mode, when the SC charges to its maximum rated value, the converter enters a hold mode where both S1 and S2 are disabled to prevent overvolting of the SC. In the boost mode, when the SC discharges to its minimum value and the converter cannot boost the voltage to required value, the converter enters a buck charge mode to charge the SC under a constant current condition. With V_{SC} within the maximum and minimum voltage limits, the converter operates in a normal mode, which maintains the dc bus voltage at reference value. The control flow chart for the bidirectional converter is shown in Figure 2.20.

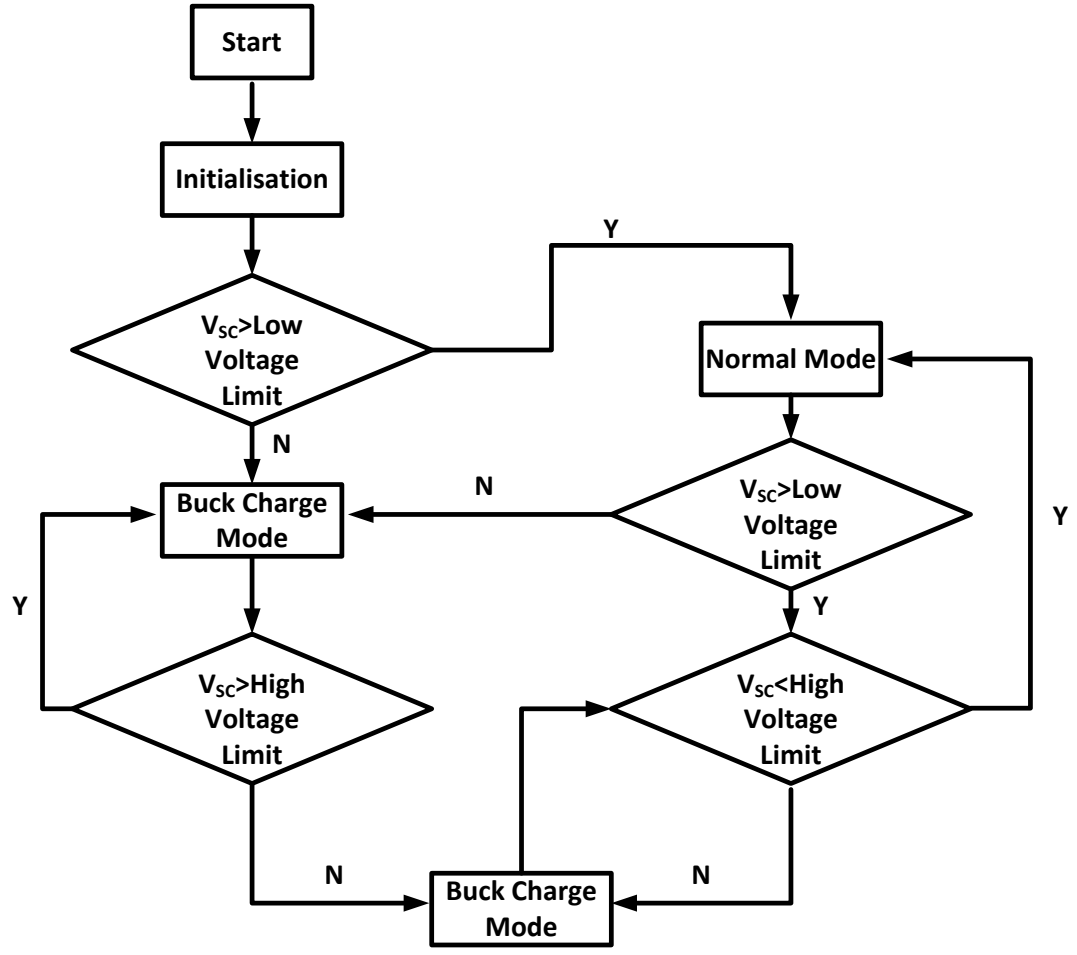

Figure 2.20 Control Flow Chart for Bidirectional Buck/Boost Converter.

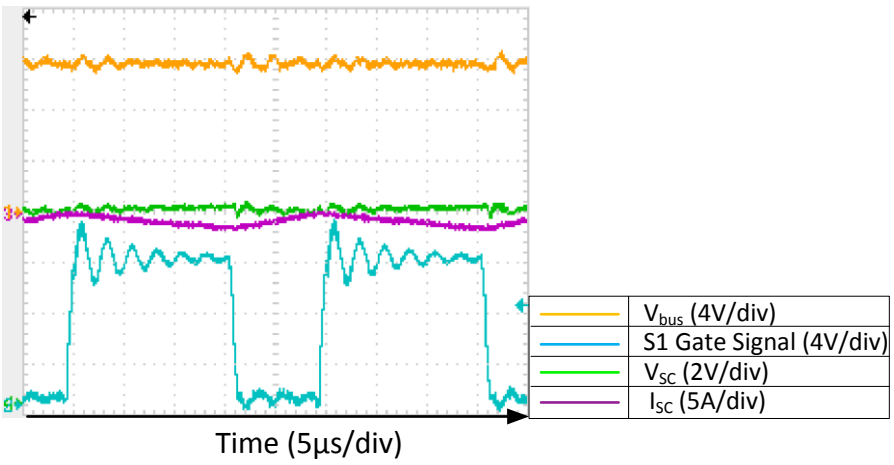

Figure 2.21 Bidirectional Buck/Boost Converter under Normal Mode without Load Switching.

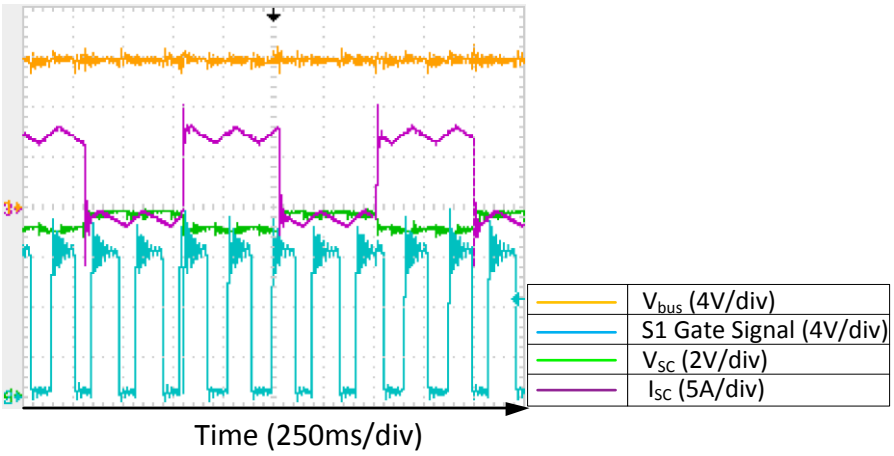

Figure 2.22 Bidirectional Buck/Boost Converter under Normal Mode with Load Switching.

During the experimentation, low and high voltage limit are 5V and 10V, while the dc bus reference voltage is 12V. Figure 2.21 shows that the converter operates in a normal mode with S3 turned off, and dc bus voltage is supported by the current source. The current is negative which means the converter is operating in the buck mode during, where the excess energy from the current source is transferred to the SC. Figure 2.22 shows the result that the converter works under normal mode with S3 turned on and off. With S3 turned on, the current source cannot maintain the dc bus voltage at 12V. The converter operates in the boost mode, where the SC

discharges to supply energy to maintain the dc bus voltage. When S3 is off, the converter operates in the condition shown in Figure 2.21.

Figure 2.23 shows the step response for the converter during load switching, the response time is 5.2ms. The dc bus voltage regulation, which is defined in equation (2.78), is 7.6%.

$$VR_{bus} = \frac{|V_{bus-normal} - V_{bus-min}|}{V_{bus-normal}} \times 100\% \quad \textbf{(2.78)}$$

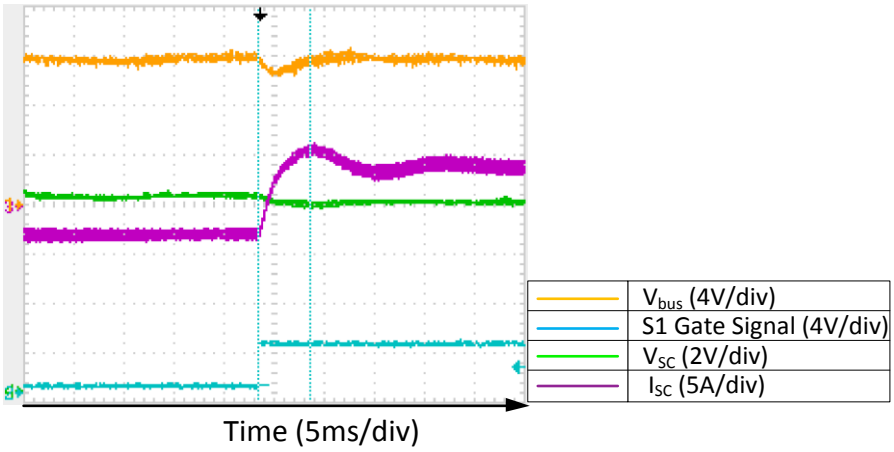

Figure 2.23 Step Response for Bidirectional Buck/Boost Converter during Load Switching.

The experiment shows the proposed bidirectional buck/boost converter is capable of both charging and discharging the SC to maintain the dc bus voltage, with a suitable response time. A hold mode protects the SC from over voltage, while the buck charge mode maintains the SC within its rated operating range.

2.5 Thermal Model

The SC is normally used as an energy storage device, which is ideal for high power transient state applications. In such applications, SC operates at high current level to store huge amount of energy in a small volume. Due to its internal resistance, high

energy loss can be generated and transferred into heat at high current level [2.18, 19]. Temperature is one of the significant parameter for SC operation, which affect its series resistance, capacitance and lifetime. For SC which made with activated carbon and an organic electrolyte technology, the operating temperature range is limited between -40 ℃ and 60 ℃. The temperature can result in reversible effect on the SC properties, where as the temperature increase, the equivalent series resistance decreases, while the capacitance and the self-discharge increases [2.20-25]. Higher temperature can also cause irreversible effect on the reducing lifetime expectancy of SC, where the heat generated by the losses from the internal resistance including carbon and conductor electronic resistance and the electrolyte ionic resistance [2.18, 26, 27].

As SC behaviour (internal resistance) is sensitive to temperature, it is necessary to develop a thermal model to analyse temperature variations under different charging/discharging conditions. SC heating can be evaluated by the imbalance between the energy loss in the internal resistance and the thermal dissipation capability. A simplified thermal circuit model with SC case to ambient thermal resistance R_{th} and thermal capacitance C_{th} is developed based on Figure 2.24.

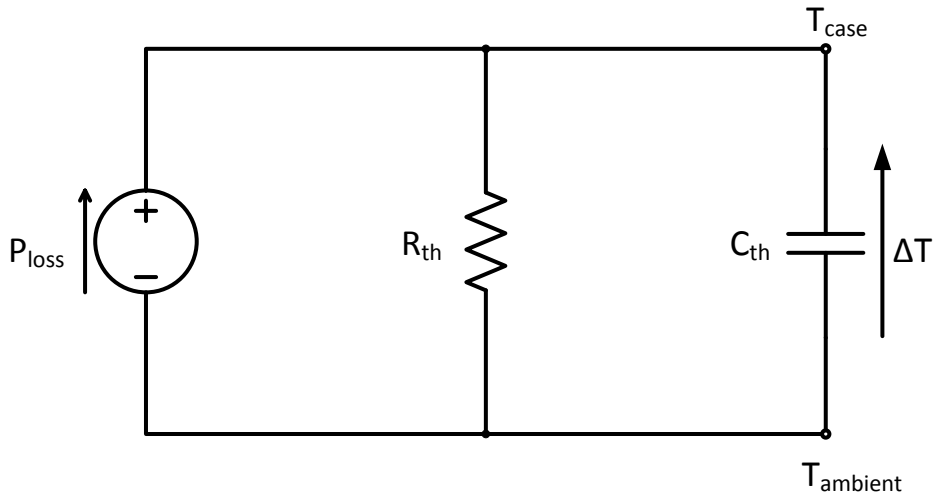

Figure 2.24 Thermal Circuit for SC.

As shown in the equivalent thermal circuit, the current source represents the power loss in the internal resistance. The temperature change can be expressed as:

$$\Delta T = P_{loss} \cdot R_{th}\left(1 - e^{-\frac{t}{R_{th} \cdot C_{th}}}\right)$$
$$where\ P_{loss} = {I_{SCrms}}^2 \cdot R_{dc} \quad \textbf{(2.79)}$$

According to equation (2.79), following parameters can be calculated:

Maximum temperature change:

$$\Delta T_{max} = P_{loss} \cdot R_{th} = {I_{SCrms}}^2 \cdot R_{dc} \cdot R_{th} \quad \textbf{(2.80)}$$

Temperature change time constant:

$$\tau_{temperature} = R_{th} \cdot C_{th} \quad \textbf{(2.81)}$$

Based on BCAP3000 P270 SC datasheet, the temperature change with time, at different rms current levels, is shown in Figure 2.25.

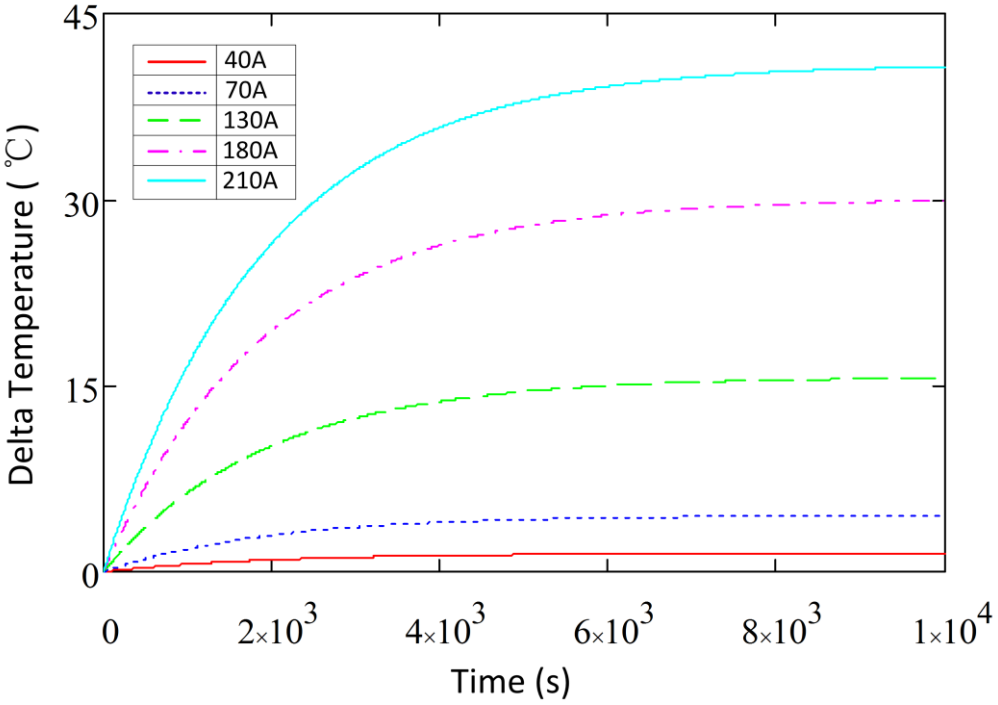

Figure 2.25 Temperature Change at Different rms Current Levels, for BCAP3000.

Based on the temperature change plot in Figure 2.25, higher current results in higher temperature raise. Due to the large thermal capacitance of the BCAP3000, the temperature change time constant is 1920s, which implies the time for the

BCAP3000 to reach its maximum temperature change is more than 2 hours. For certain low duty applications, such as 140ms grid fault-ride-through, the temperature change is relative small because of the short discharge time, so a high discharge current level can be selected during system design for a better volume/price solution.

2.6 Summary

The characteristic analysis of the supercapacitor presented in this chapter, has introduced its electrical behaviour and performance under different operating condition. Under constant current and constant power discharge, which are typical application cases for the supercapacitor, the characteristics of the current, voltage, power, discharge time and efficiency have been demonstrated based on a mathematical model and verified by simulation and experimentation. A triangle wave current effects capacitor efficiency, which commonly occurs in the input of the boost converter, are analysed in both continuous and discontinuous conduction modes. A control algorithm example of using the supercapacitor as an energy storage system has been introduced, based on a bidirectional buck/boost converter, which is able to control energy flow to both charge or discharge the supercapacitor in order to maintain the load voltage. The thermal model of the supercapacitor has been introduced for thermal analysis, which seriously affects supercapacitor lifetime expectancy.

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Chapter 3

3 Supercapacitor Modelling

With rapidly developing manufacturing technology and cost reductions, a supercapacitor (SC) based energy storage system for different power level applications is an industrial reality [3.1]. In low level power system, the supercapacitor is applied in telecommunication and portable devices for energy back up [3.2, 3]. In medium power system, the supercapacitor is used either solely or in combination with other energy storage devices, such as the battery and fuel cells, in the electrical vehicle, heavy transportation, and elevators [3.3, 4]. In high power systems, the supercapacitor is proposed as an energy storage system to improve the low voltage ride through capability and power quality in distributed renewable energy applications [3.5, 6]. For all such supercapacitor applications, an accurate model of supercapacitor is essential for analysing its behaviour under various operating conditions.

The SC can be modelled either by an electrochemical model or an equivalent circuit model. The electrochemical model, with a large number of parameters, is developed to describe the physical behaviour of the supercapacitor. However, for electrical applications, the electrochemical model is difficult to integrate into an electrical circuit model. The equivalent circuit model, developed with existing electrical component, is readily manipulated within practical circuit applications.

The equivalent circuit model is useful in electrical application as it allows insertion into the circuit for system modelling. Based on the physical behaviour, the SC has two electrical parts, namely the energy storage being the capacitive part and the energy loss being the resistive part [3.7]. As a result, the supercapacitor is modelled as a capacitor in series with a resistor, which is known as the classic model.

However, due to the complex physical structure, the classic model may not satisfactorily describe SC behaviour, especially the charge redistribution phenomena. Many different electrical models have been proposed to improve accuracy under different conditions, such as the three branch model, ladder model, and transmission

line model [3.8-10]. The associated parameter identification methods are also important in improving model accuracy. Different models are reviewed in this chapter, and the applicable conditions for each model are discussed. Two new parameter identification methods are proposed to demonstrate a simplified experimental test to identify the SC model parameters.

3.1 Supercapacitor Model Review

The supercapacitor, which technically known as the electric double layer capacitor, is developed on the double layer structure discovered by Helmholtz since the late 1800s [3.11]. At the same time, the double layer is described as a simple parallel plate capacitor by the Helmholtz-Perrin model [3.11]. Considering the typical expression for a parallel plate capacitor, the capacitance can be expressed as

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d} \tag{3.1}$$

ε_0 is the permittivity of free space,

ε_r is the relative permittivity of the dielectric,

A the plate surface area, and

d the plate separation.

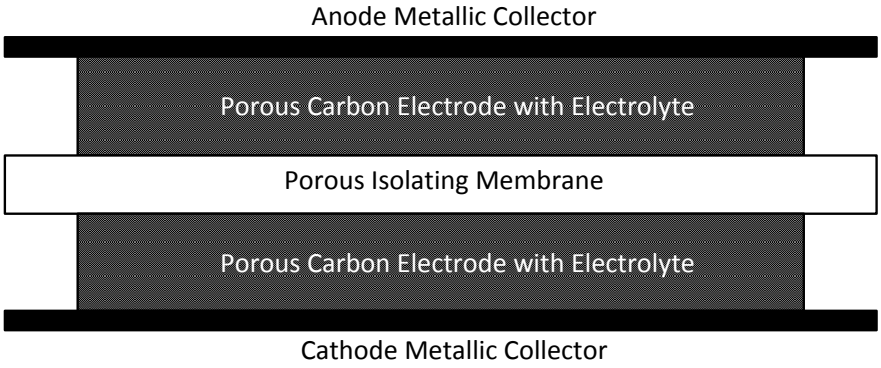


Figure 3.1 SC Physical Construction.

The relative permittivity of the dielectric for SC refers to the one or several layers of electrolyte molecules and depends on the electrolyte material. For SC with organic electrolyte solvent of acetonitrile, the relative permittivity is 37.5 [3.12]. The ultra

high capacitance of the SC is achieved by its large surface area and small equivalent plate separation compared to conventional capacitors. Equation (3.1) defines the SC capacitance in terms of its physical structure; however, the electric behaviour of SC model is more important when analysing the SC in practical applications.

Due to a similar electric behaviour as the conventional capacitor, the SC model is based on a capacitor and resistor combination structure. For charge/discharge processes, the voltage and current of the SC can be described by a single RC branch, where for higher accuracy variable capacitance can be used. For medium and long term SC characteristics, a charge redistribution, multi branch model, and impedance model, are adopted for SC modelling.

3.1.1 Theoretical Model of Supercapacitor

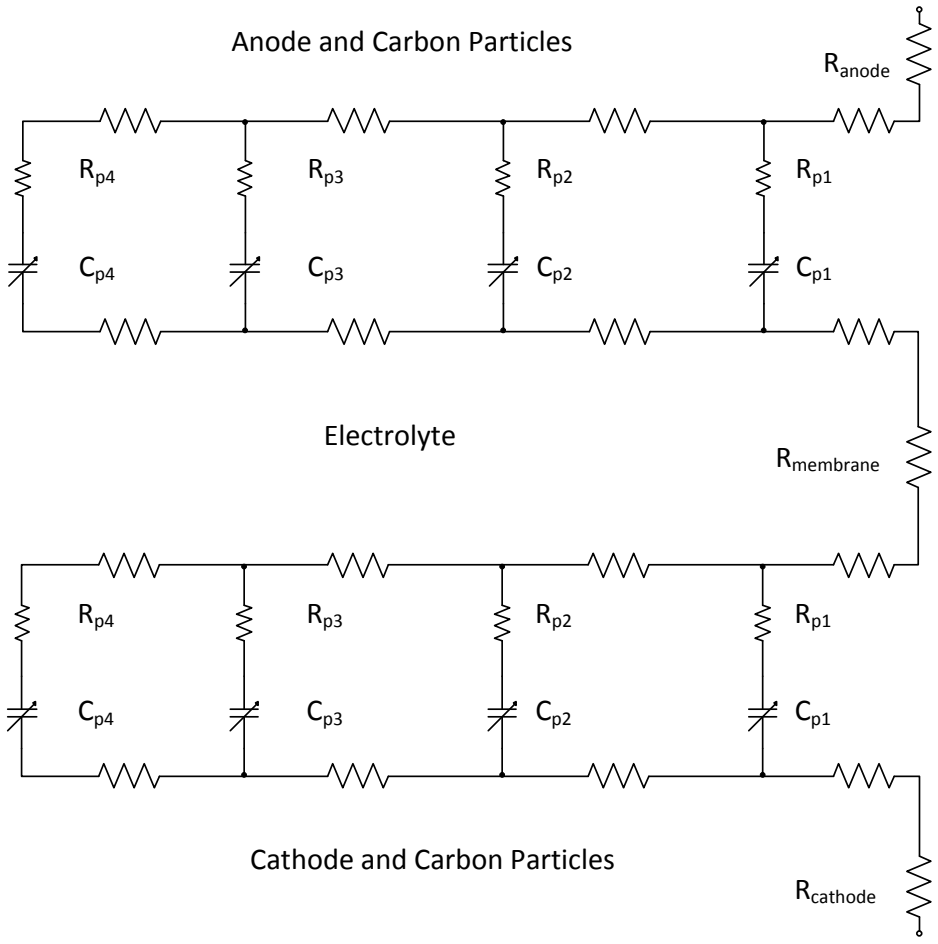


Figure 3.2 Theoretical Model of a SC.

The extremely high SC capacitance is achieved by using porous electrode materials with high surface area, which is normally activated carbon. The two porous carbon electrodes are impregnated with electrolyte and separated by a porous insulating membrane which allows ionic conduction but prevents short circuits between the electrodes. The anode and cathode metallic collectors are attached at the end of the two porous carbon electrodes. The physical construction representation for the SC is shown in Figure 3.1 [3.8, 13, 14].

The theoretical SC model is composed of billions resistor and capacitor (RC) branches in parallel as shown in Figure 3.2, where C_p and R_p represents the pore capacitor and resistor [3.13, 14]. The pore capacitance is a voltage dependent parameter. The resistance of each pore resistor is different, which depends on electrode materials resistivity and electrolyte resistivity. The external anode and cathode resistance R_{anode} and $R_{cathode}$ is associated with leads and connections. The porous membrane can be represented by a resistor $R_{membrane}$ which connects the two halves of the SC [3.8, 14]. Due to the difference in capacitance and resistance, a charge redistribute phenomenal is observed in practice, where the SC voltage varies briefly after been disconnected [3.8].

The theoretical model parameters are difficult to identify in practice, and applying the theoretical model in energy storage system simulation and analysis is inefficient. However, the basic topology for most SC models are developed based the theoretical model with a decreased number of RC branches.

3.1.2 Classical model

The classical model [3.15] for the SC shown in Figure 3.3 is the basic model to represents SC behaviour and is widely presented in SC manufactures datasheets. The model includes a capacitor, an equivalent series resistor (R_{ESR}) representing the internal resistance and an equivalent parallel resistor (R_{EPR}) modelling leakage current [3.11].

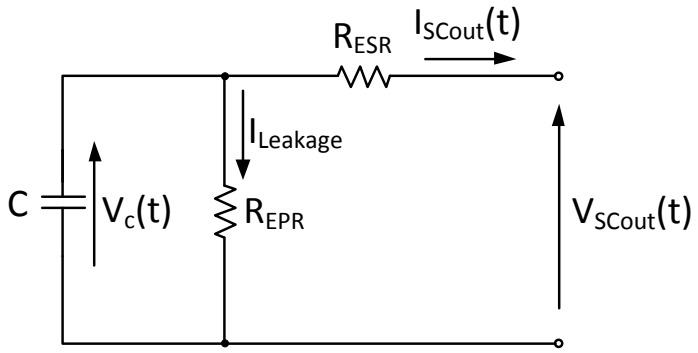


Figure 3.3 Classical Model for a SC.

Capacitor behaviour can be described as a mathematical function:

$$V_c(t) = V_c(0) - \int_0^t \frac{\left(I_{SCout}(t) + I_{Leakage}\right) \cdot t}{C} dt \quad \textbf{(3.2)}$$

where $V_c(0)$ *is the initial voltage of the capacitor*

The SC output voltage is:

$$V_{SCout}(t) = V_c(t) - I_{SCout}(t) \cdot R_{ESR} \quad \textbf{(3.3)}$$

Usually a SC datasheet provides capacitance, internal resistance and the leakage current for general design. Due to the low leakage current compared to the SC operational current, the R_{EPR} is usually neglected in analytical modelling and system simulation [3.11, 16]. The R_{EPR} is used to predict the voltage variance of a long-term stored SC. It is essential for certain application designs, such as back-up energy storage systems, where the energy storage system is not frequently used, but needs to be charged at a required voltage level [3.17, 18]. Based on the classic model, the series and parallel number of SCs can be estimated for energy storage system design. The total capacitance and resistance can be expressed by the series and parallel number of individual capacitors:

$$C_{total} = \frac{N_P}{N_S} \cdot C \quad \textbf{(3.4)}$$

$$R_{total} = \frac{N_S}{N_P} \cdot R_{ESR} \quad \textbf{(3.5)}$$

where N_S *is the series number and* N_P *is the parallel number*

Normally, the design estimation is based on the rated SC parameters in the datasheet. However, in simulation and practical efficiency calculation, experimentally based SC parameters are required to increase accuracy. According to [3.11], a detailed parameter identification method is now introduced:

1. Parallel Resistance R_{EPR}

The SC is slowly charged to a set voltage V_1, then the SC voltage V_2 is measured and recorded after the SC been stored open circuit for three hours. As shown in Figure 3.3, the SC experiences an RC discharge. By using the rated capacitance, the resistance of the R_{EPR} is calculated as:

$$R_{EPR} = \frac{-10800}{ln\left(\frac{V_1}{V_2}\right) \cdot C} \tag{3.6}$$

Due to the large value of R_{EPR}, which is in the range of 500Ω to 2000Ω, the typical leakage current of SC is in the order of a few milliampere. In such case, it is removed from the model to simplify the R_{ESR} and capacitance identification method.

2. Series Resistance R_{ESR}

The SC is connected with a resistive load via a switch. Then the SC is pre-charged to a set value and the SC voltage and current difference are measured as ΔV and ΔI, after the switch is turned on. The R_{ESR} is calculated as:

$$R_{ESR} = \frac{\Delta V}{\Delta I} \tag{3.7}$$

In [3.11], some variance in the calculated ESR values are observed; however, the variance is small enough to be ignored in the capacitance calculations. As a result, during the capacitance calculation, the ESR is considered a constant.

3. Capacitance

A similar discharge process as the ESR identification method is used, where the output current and voltage are measured. According to the circuit in Figure 3.3, the capacitance is calculated based on the change in stored energy, where the stored energy is:

$$\Delta E = \frac{1}{2} C \cdot (V_c(t_1)^2 - V_c(t_2)^2) = \int_{t_1}^{t_2} V_c(t) \cdot I_{SCout}(t)\, dt$$

The capacitance can be calculated from the change in stored energy:

$$C = \frac{2 \int_{t_1}^{t_2} V_c(t) \cdot I_{SCout}(t)}{V_c(t_1)^2 - V_c(t_2)^2} \quad \textbf{(3.8)}$$

The capacitor voltage is determined with the calculated ESR:

$$V_c(t) = V_{SCout}(t) + R_{ESR} \cdot I_{SCout}(t) \quad \textbf{(3.9)}$$

By choosing a proper time interval [t_1, t_2], the average capacitance is calculated based on moving the interval from the start to the end of discharge process.

Due to the simplicity of analytical model, efficiency, power loss and thermal calculation, can be easily analysed compared to more complicated models. However, the accuracy for the classic model may be poor. In [3.9, 11], about 10% capacitance change occurs experimentally. As the SC capacitance and resistance are nonlinear, the classic model cannot accurately describe SC behaviour, especially the charge redistribution phenomena and frequency response.

3.1.3 Three Branch Model

The Three Branch Model introduced in [3.9], includes three series RC branches in parallel. The model is developed based on the physical model, however due to practical reasons the RC branch number is limited to three. The three RC branches are termed the immediate branch, delayed branch, and long-term branch, along with a leakage resistor, as shown in Figure 3.4.

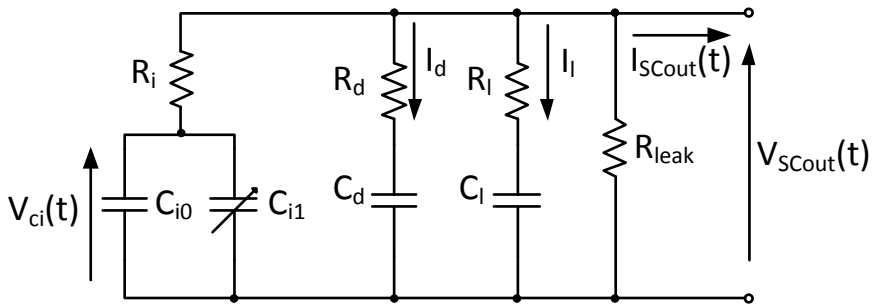


Figure 3.4 Three Branch Model.

The immediate branch, which includes R_i, C_{i0} and a voltage-dependent capacitor C_{i1}, is used to describe the immediate frequency behaviour of the SC in the time range of seconds. The voltage-dependent capacitor is expressed as:

$$C_{i1}(V_{ci}) = k_v \cdot V_{ci}$$
$$\textit{where } k_v \textit{ is the capacitance/voltage coefficient} \qquad \textbf{(3.10)}$$

The voltage-dependent capacitor models SC nonlinear characteristics. The delayed branch with R_d and C_d is used to describe the SC behaviour in the long term range, in minutes. The long-term branch of R_l and C_l, determines the behaviour for times longer than 10 minutes. The leakage resistor R_{leak} is employed to describe the SC self-discharge in time range of hours.

The approach to determine the different model parameters is based on charging the SC under high constant current condition until it reaches the rated value, which is maintained for several tens of seconds. Due to the largely differing time constants, the three RC branches are treated independently to simplify the parameter identification process. A high current level, 5% of the specified SC short circuit current, is selected to desensitise the other two branches [3.9]. The whole parameter identification process is divided into 9 events with 8 time intervals:

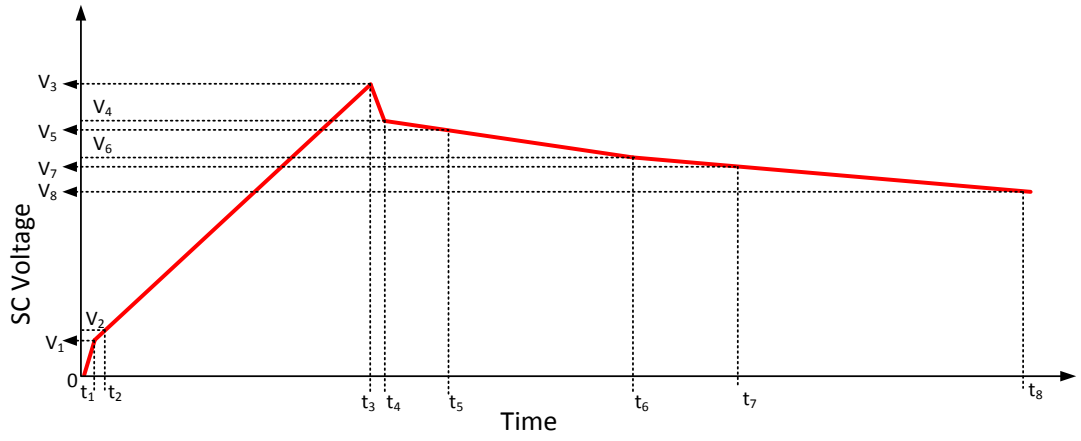


Figure 3.5 Parameter Identification Process for the Three Branch Model.

Event=0

At time 0, the SC is charged from 0V with the constant current I_{out}.

Event=1

It is assumed that the voltage change in 20ms is mainly due to the resistor rather than charge in the capacitor. The SC voltage is measured as V_1 at t_1 = 20ms, and the immediate branch resistance is:

$$R_i = \frac{V_1}{I_{out}} \tag{3.11}$$

Event=2

The time t_2 is recorded as the SC voltage increased by $\Delta V = 50mV$ from V_1 to V_2. The variable capacitor C_{i1} is ignored as the capacitor voltage V_{ci} is low. The initial capacitance of the immediate branch is:

$$C_{i0} = I_{out} \cdot \frac{t_2 - t_1}{\Delta V} \tag{3.12}$$

Event=3

The SC is charged to rated voltage V_3 at t_3, and the constant current charge stops.

Event=4

A 20ms interval is selected to ensure the SC output current falls to 0. The SC voltage V_4 at $t_4 = t_3 + 20\text{ms}$ is recorded, and the variable capacitance coefficient can be calculated based on the total capacitor charge:

$$k_v = \frac{2}{V_4} \cdot \left(\frac{Q_{tot}}{V_4} - C_{i0}\right)$$
$$where\ Q_{tot} = I_{out} \cdot (t_4 - t_1) \tag{3.13}$$

Event=5

The time t_5 is recorded as the SC voltage decreases to $V_5 = V_4 - \Delta V$, where ΔV is 50mV. The delayed branch is assumed to be charged by the immediate branch with a constant current I_d, which can be expressed as:

$$I_d = \frac{V_4 - \frac{\Delta V}{2}}{R_d}$$

The constant current also can be expressed in terms of the change in the charge of the immediate branch capacitor:

$$I_d = \left(C_{i0} + k_v \cdot \left(V_4 - \frac{\Delta V}{2}\right)\right) \cdot \frac{\Delta V}{t_5 - t_4}$$

The delayed branch resistor can be calculated from:

$$R_d = \frac{\left(V_4 - \frac{\Delta V}{2}\right) \cdot (t_5 - t_4)}{\left(C_{i0} + k_v \cdot \left(V_4 - \frac{\Delta V}{2}\right)\right) \cdot \Delta V} \quad \textbf{(3.14)}$$

Event=6

At time $t_6 = t_5 + 3(R_d \cdot C_d)$, where $R_d \cdot C_d$ is normally 100s, the SC voltage is recorded as V_6. It is assumed that the voltage of delayed branch capacitor equals the voltage of the immediate branch capacitor, and the redistributed total charge of the SC can be expressed as:

$$Q_{tot} = C_d \cdot V_6 + \left(C_{i0} + k_v \cdot \frac{V_6}{2}\right) \cdot V_6$$

The capacitance of the delayed branch is:

$$C_d = \frac{Q_{tot}}{V_6} - \left(C_{i0} + k_v \cdot \frac{V_6}{2}\right) \quad \textbf{(3.15)}$$

Event=7

The time t_7 is recorded as the SC voltage decreases to $V_7 = V_6 - \Delta V$, where ΔV is 50mV. The long-term branch starts to be charged by the other two branches, the current from the delayed branch is ignored due to the resistance difference. The long-term branch resistance is:

$$R_l = \frac{\left(V_6 - \frac{\Delta V}{2}\right) \cdot (t_7 - t_6)}{\left(C_{i0} + k_v \cdot \left(V_6 - \frac{\Delta V}{2}\right)\right) \cdot \Delta V} \tag{3.16}$$

Event=8

The time $t_8 = 30\text{mins}$ is selected, which assumes the charge redistribution within the SC has ceased. The long-term branch capacitance is:

$$C_l = \frac{Q_{tot}}{V_8} - \left(C_{i0} + k_v \cdot \frac{V_8}{2}\right) - C_d \tag{3.17}$$

The model adequately represents the SC internal charge redistribution characteristic, and the current and voltage are accurate for voltages above 40% of the rated terminal voltage. However, due to assumptions made in simplifying the model and the parameters identification process, the error at low voltages may over 10% of the rated voltage [3.9].

3.1.4 Transmission line model

The SC theoretical model can be represented by a transmission line model with voltage dependent distributed capacitance [3.8]. The transmission line model indicates that the capacitance increases as the voltage increases and a time dependent apparent capacitance is introduced due to the space distribution of electrical charge and electrostatic energy. The transmission line model under a step current with magnitude of I is shown in Figure 3.6, where x represents the distance. A mathematical model based on it in time domain is developed as follows:

$$C_{app}(t) = \frac{1}{Z_{imp}(t)}$$

$$Z_{imp}(t) = \frac{1}{C} \cdot \sqrt{\frac{\tau}{\pi \cdot t}} \cdot \left(1 + 2\sum_{n=1}^{+\infty} e^{-n^2 \cdot \frac{\tau}{t}}\right)$$

$$V(0,t) = Z_{ind}(t) \cdot I$$

$$Z_{ind}(t) = \frac{2}{C} \cdot \sqrt{\frac{\tau \cdot t}{\pi}} \cdot \left(1 + 2\sqrt{\pi}\sum_{n=1}^{+\infty} ierfc\left(n \cdot \sqrt{\frac{\tau}{t}}\right)\right) \quad \textbf{(3.18)}$$

$$\tau = R \cdot C$$

where the function ierfc() is defined as the integral error function for each element of a_0:

$$ierfc(a_0) = \frac{e^{-{a_0}^2}}{\sqrt{\pi} \cdot} - \frac{2a_0}{\sqrt{\pi}} \cdot \int_{a_0}^{\infty} e^{-t^2}\, dt$$

In equation (3.18), the apparent capacitance C_{app} is defined by the line pulse impedance Z_{imp}, while the line voltage $V(0,t)$ is defined by the step impedance Z_{ind}. Both pulse impedance and step impedance are determined by the total line capacitance C and resistance R of the transmission line.

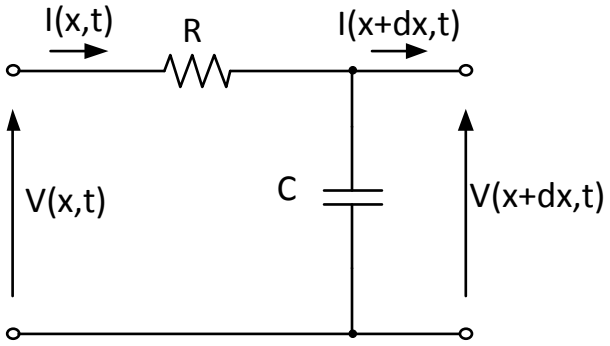


Figure 3.6 Transmission Line Mathematical Model.

In [3.8], a combined transmission line model with the three branch model [3.9] is introduced to improve SC accuracy. The short time SC behaviour is determined by the nonlinear transmission line model, while the parallel RC branches are used to

indicate the charge redistribution phenomena for long term behaviour. A finite number of parallel RC branches are required for simulation.

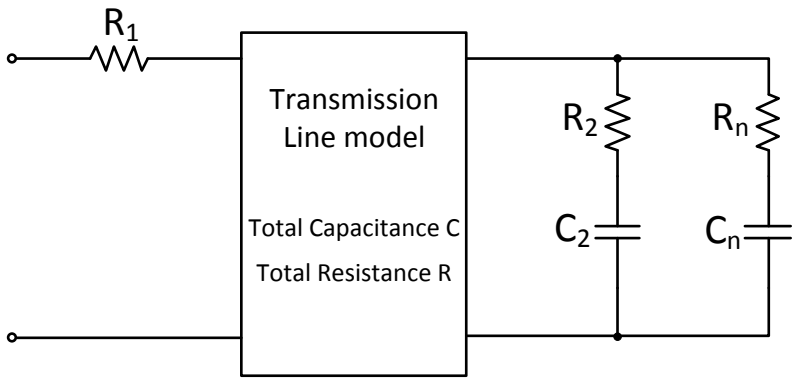


Figure 3.7 Transmission Line Model.

The parameter of the transmission line model is identified based on voltage response of SC short duration constant current charging at different initial voltage level. Similar to the identification process of the three branch model, the long-term RC branches are ignored for short-term parameter identification.

The resistance R_1 is calculated by the initial voltage drop. The line total capacitance C is determined by experimental SC partial charge, which defines the capacitance as a voltage dependant parameter. The line total resistance R is extracted from the step impedance equation (3.18) in very short period, which is simplified to:

$$Z_{ind}(t) \approx R_1 + \sqrt{\frac{4R}{\pi \cdot C} \cdot t} \qquad \textbf{(3.19)}$$

The long-term RC branch parameters are identified using the same approach introduced in the three branch model.

The transmission line model results in a difference in store or delivered charge of the SC compared to the three branch model. The charge variation in the transmission line model depends on the current level for a certain voltage variation. The transmission line model indicates less deliverable charge and deliverable energy storage, where the difference is over 18% [3.8]. Although the model provides SC higher accuracy, the identification procedure and development of the analytical

model based on the transmission line model is complex, thus the transmission line model is not widely used in SC simulation.

3.1.5 The SC Ladder Model

The SC multi-stage ladder model is based on impedance spectroscopic measurement [3.19]. In [3.19], Miller introduced the five-stage ladder model shown in Figure 3.8. The topology is selected based on the impedance plot shown in Figure 3.9. The five-stage ladder model has sufficient accuracy for frequency analysis up to 10 kHz [3.10].

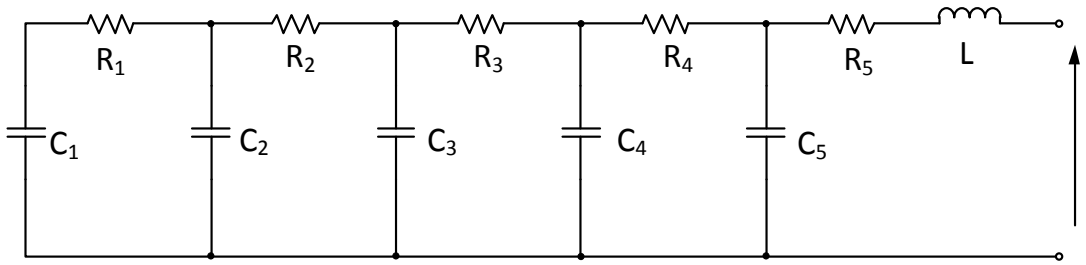


Figure 3.8 Five-Stage Ladder Model of SC.

However, the ladder model is inefficient in simulation due to the limitation of high-order step times. An automatic order selection method has been developed based on the five-stage ladder model for simulation at different frequency bands [3.10]. As shown in Figure 3.9, a different order model represents the different frequency ranges of the five-stage ladder model. According to the simulation time step, the automatic order selection model justifies the correct order of the ladder network to achieve an optimal solution for minimising calculation error and saving computational time. The parameter value of the reduced order model is developed based on the five-stage ladder model which is calculated as shown in Figure 3.10.

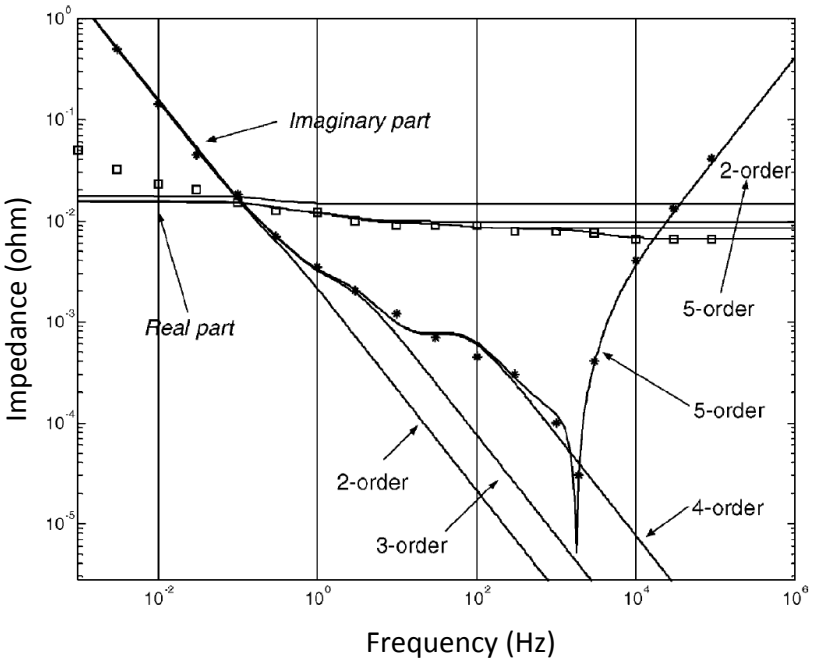


Figure 3.9 Impedance Plot for Maxwell PC100[3.10].

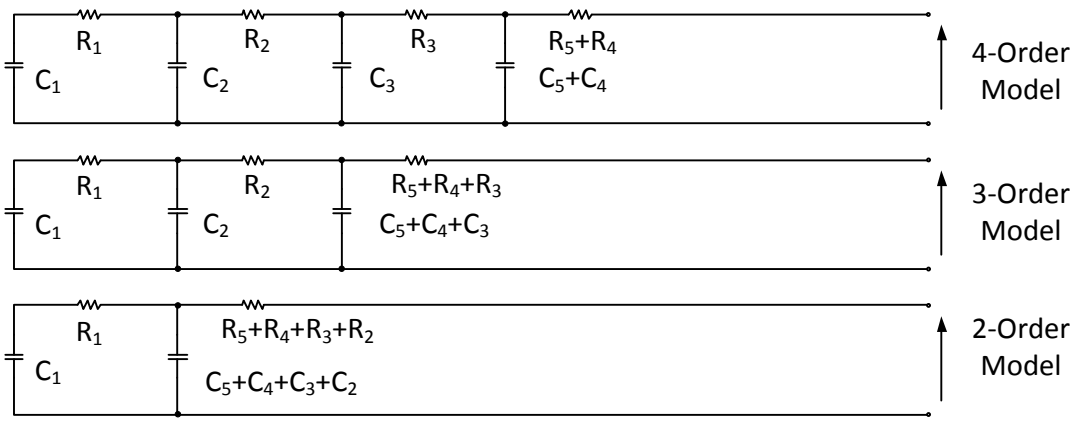


Figure 3.10 Automatic Order Selection Model.

Although the automatic order selection multi-stage ladder model shows good accuracy for SC practical behaviour, with improved simulation performance, the parameters are based on the five-stage ladder model which requires a complex identification process. Electrochemical impedance spectroscopy (EIS) method, based on an EIS meter, is used to produce the impedance response. Furthermore, the

impedance response varies for different types of SC at different operating conditions, which potentially changes the model order number to fit the full frequency range.

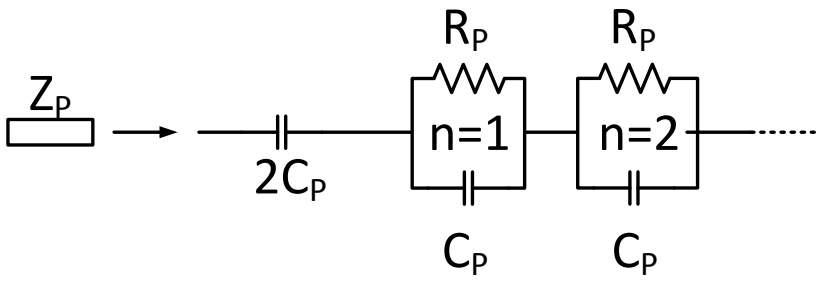
Similar SC model based on the EIS method, developed based on the impedance response, is introduced in [3.20-22]. As shown in Figure 3.11 (a), the model includes an inductor L, a series resistor R_i and complex pore impedance Z_P, which is used to fit the impedance characteristic. The pore impedance in the frequency domain is defined as:

$$Z_P(j\omega) = \frac{\tau \cdot coth(\sqrt{\tau \cdot j\omega})}{C_P \cdot \sqrt{\tau \cdot j\omega}} \quad \textbf{(3.20)}$$

In time domain, the pore impedance can be approximated by the circuit shown in Figure 3.11 (b), where the pore resistance is

$$R_P = \frac{\tau}{\pi^2} \cdot \frac{2}{n^2 \cdot C_P}$$

a) Advanced Equivalent Circuit



b) Time Domain Expansion of Z_P

Figure 3.11 Advanced Equivalent Circuit for SC.

Four parameters, R_i, L, C_P and τ, need to be extracted from the impedance plot, which is fewer than for the ladder model. However, the pore capacitance and time constant are voltage and temperature dependent, which results in a large number of impedance measurements for different operating conditions.

Both models are based on the EIS, and improve SC accuracy over the full frequency response range. However, a large number of experiments for identifying the impedance characteristics is inefficient for general SC modelling. The analysis and simulation are more complex than for the classic model.

3.1.6 N Branch Model

An extended *n* branch model based on the three branch model is introduced in [3.23]. The model includes an equivalent series inductor and an increased number of RC braches to expand the effective frequency range, as shown in Figure 3.12. Each RC branch is defined by its branch time constant, which is:

$$\tau_1 = k \cdot \tau_2 = \cdots = k^{n-1} \cdot \tau_n$$
$$where\ \tau_n = R_n C_n \quad \textbf{(3.21)}$$

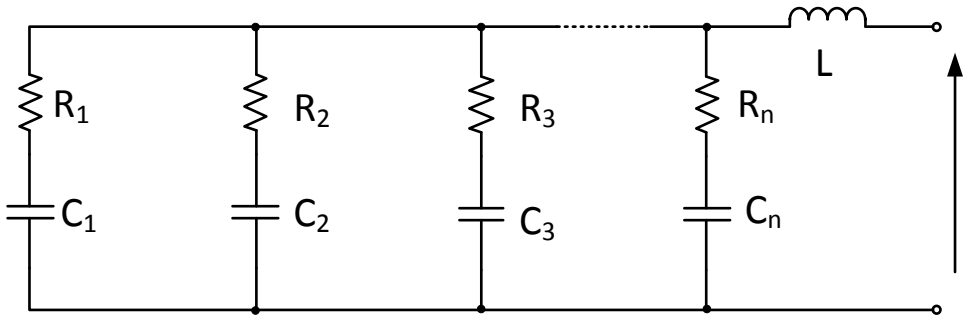


Figure 3.12 N Branch SC Model.

The parameter is identified based on the impedance plot, which is similar to the SC ladder model. According to the frequency domain expression of the model, the values of RC in each branch are identified by a nonlinear least-square fitting algorithm.

The structure of the *n* branch model is easy to understand, since all the RC branches are paralleled. The frequency domain expression can be readily obtained. However, as the branch number increases, parameter identification by using nonlinear lease-squares fitting becomes more complex, presenting similar problems as the ladder model.

3.2 Novel SC Parameter Identification Methods

As stated previously, SC model accuracy increases as complexity increases. Increasing the number of paralleled RC branches and using voltage dependant capacitors, typically increase SC modelling accuracy. The two branch model and the variable capacitance model are selected for analysing SC discharge behaviour. The parameter identification of the multi branch model and variable capacitor model are based on either EIS or the constant current method, which requires external control circuit and special equipment. The proposed parameter identification method is based on a simple RC discharge, which only requires charging the SC to a set value and discharge through a resistor.

3.2.1 Two Branch Model Parameter Identification Method Based On RC Discharge

The RC discharge parameter identification method is developed for the two branch mathematical model, where the two parallel RC branches are connected a load resistor as shown in Figure 3.13. The SC output voltage and current are measured during the RC discharge process, and the four parameters of the model can be calculated based on a nonlinear least-square curve fitting method.

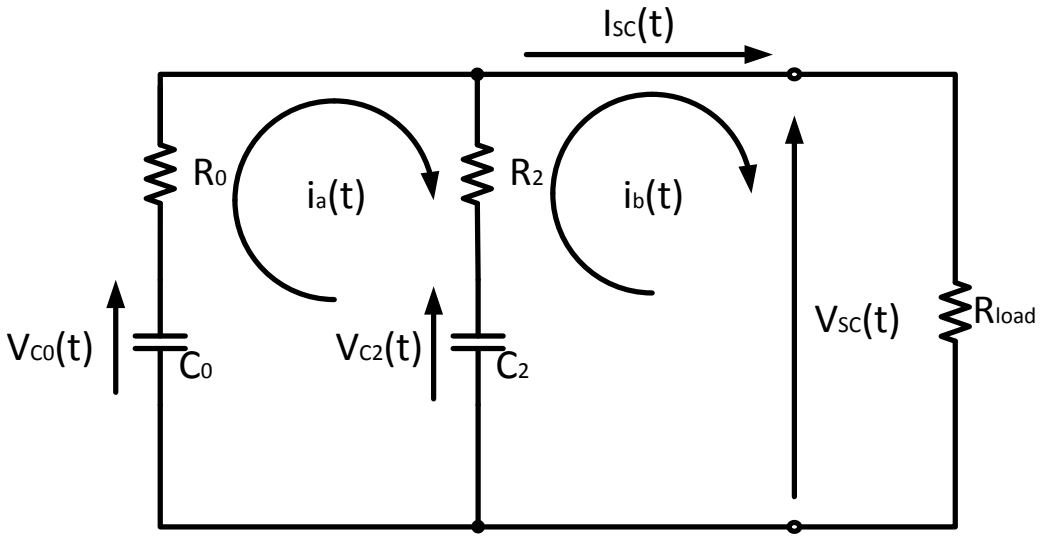


Figure 3.13 Two Branch RC Discharge Mathematical Model.

Based on the mathematical model, the SC output current can be expressed as:

$$I_{SC}(t) = K_{b1} \cdot e^{p_{b1} \cdot t} + K_{b2} \cdot e^{p_{b2} \cdot t}$$

where

$$p_{b1} = \frac{-D_b + \sqrt{{D_b}^2 - 4C_b}}{2C_b}, p_{b2} = \frac{-D_b - \sqrt{{D_b}^2 - 4C_b}}{2C_b}$$

$$K_{b1} = \frac{N(S)}{D^*(S)}\bigg|_{S=p_{b1}} = \frac{A_b \cdot p_{b1} + B_b}{2C_b \cdot p_{a1} + D_b},$$

$$K_{b2} = \frac{N(S)}{D^*(S)}\bigg|_{S=p_{b2}} = \frac{A_b \cdot p_{b2} + B_b}{2C_b \cdot p_{b2} + D_b} \quad \textbf{(3.22)}$$

with

$$A_b = C_0 \cdot V_{C0}(0) \cdot R_2 \cdot C_2 + R_0 \cdot C_0 \cdot C_2 \cdot V_{C2}(0),$$

$$B_b = C_0 \cdot V_{C0}(0) + C_2 \cdot V_{C2}(0),$$

$$C_b = R_0 \cdot C_0 \cdot C_2 \cdot R_{load} + R_0 \cdot C_0 \cdot C_2 \cdot R_2 + R_2 \cdot C_0 \cdot C_2 \cdot R_{load},$$

$$D_b = R_0 \cdot C_0 + R_2 \cdot C_2 + R_{load} \cdot C_2 + C_0 \cdot R_{load}$$

The experimental circuit is shown in Figure 3.14, where a dc power supply is used for charging the SC, and a switch activates the RC discharge process.

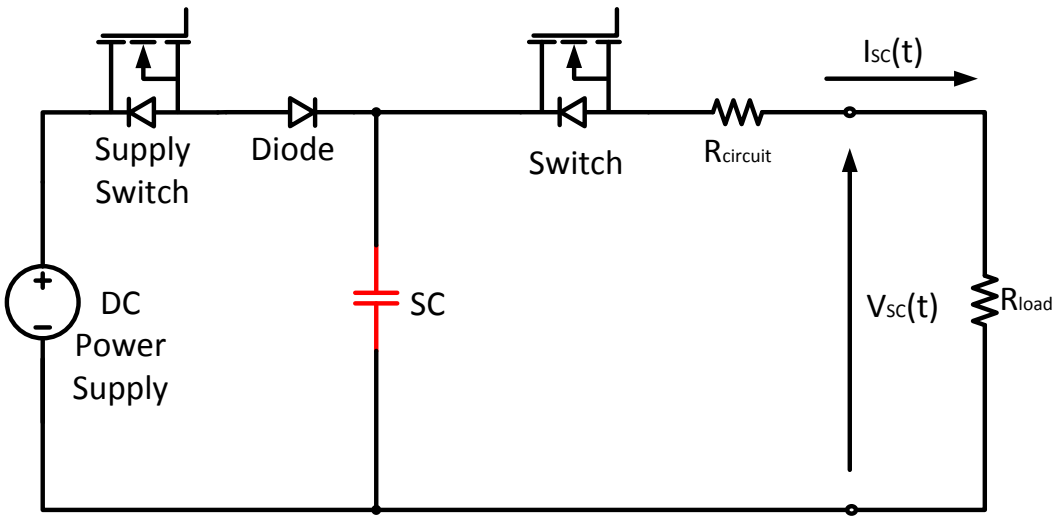


Figure 3.14 Experiment Circuit for RC Discharge of SC Parameter Identification.

The parameter identification procedure is as follows:

1. Turn on the supply switch to charge the SC to the set voltage level, by the DC power supply;
2. Turn off the supply switch and leave the SC for 5 minutes to avoid any charge redistribution effects.
3. Turn on the switch to start the RC discharge and record the SC output current and voltage;
4. Based on the experimental results, the parameters p_{b1}, p_{b2}, K_{b1} and K_{b2} in equation (3.22) can be identified by a nonlinear least-square fitting method.
5. Parameters A_b, B_b, C_b and D_b can be solved by equation (3.22).
6. The initial voltage of the two capacitor $V_{C0}(0)$ and $V_{C2}(0)$ are the initial SC discharge voltage.
7. Using A_b, B_b, C_b, D_b, $V_{C0}(0)$ and $V_{C2}(0)$, the SC model parameters C_0, R_0, C_2 and R_2 can be calculated by solving the inverse of equation (3.22).

An example of the identification procedure for a SC bank, which includes four BCAP0350 in series, follows. The SC bank is charged to its rated voltage, an initial discharge voltage of 10V, and discharged through a load resistance of 0.28Ω with the equivalent circuit resistance of 0.004Ω including the MOSFET on-stated resistance. As the load resistor and equivalent circuit resistor are series connected, the resistance can be added together as R_{load} in equation (3.22). The SC output voltage and current are recorded in Figure 3.15.

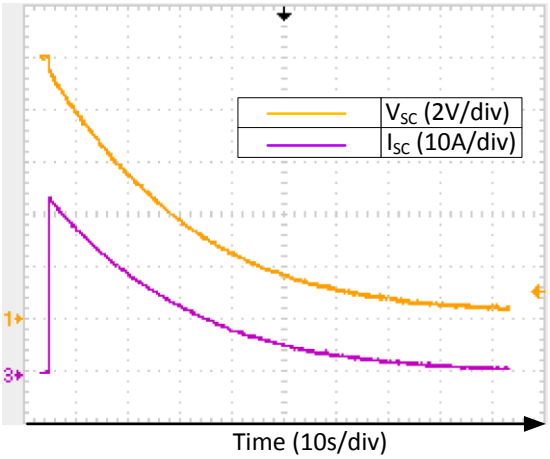


Figure 3.15 Experiment Results for Discharge SC Bank with 0.28ohm Load.

Table 3.1 Two Branch Model Parameters for SC Bank

Parameter	Value	Parameter	Value
$V_{C0}(0)$	10 V	$V_{C2}(0)$	10 V
C_0	88.167 F	R_2	$1.804 \times 10^{15}\ \Omega$
R_0	0.011 Ω	C_2	1.42×10^{-14} F

The calculated parameters for the proposed model are shown in Table 3.1. The first branch parameters are realistic and related to the practical datasheet. The parameters for the second branch are calculated to fit the experimental result, but without any physical meaning.

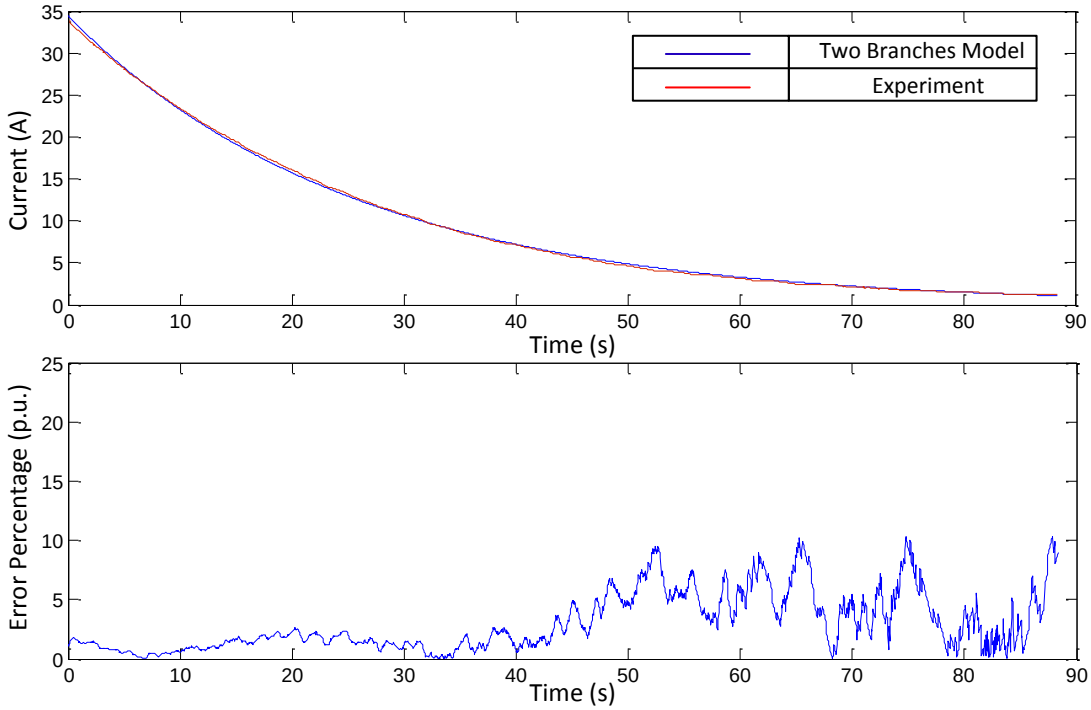


Figure 3.16 Comparison of the Two Branch Model and Original Experiment Result and Error Percentage Plot.

Figure 3.16 is a comparison plot of the proposed model and the original experiment, where error percentage is defined as:

$$Error\ Percentage = \frac{\left|I_{Model} - I_{Exp}\right|}{I_{Exp}} \times 100$$

As the result show in Figure 3.16, the proposed two branch model fits well with the experiment result when the current is greater than 5A. The error percentage increases over 10% when the current falls below 5A, which is mainly due to definition of the error percentage. Although the absolute current error is near constant over the full range, the decreased base value increases the error percentage.

Similar RC discharge experiments on a single BCAP350 at different voltage levels are performed to investigate the voltage dependence of the model parameters. The SC is charged to different initial voltage levels, specifically 10 levels from 2.5V to 0.5V. The SC is discharged through a 0.021Ω load resistor, and same parameter identification method is applied. The calculated parameters follow:

As the result show in Table 3.2, the first branch parameters are stable, while the second branch values are random as shown in the 10V experiment. The capacitance of the first branch C_0 increases linearly with voltage as shown in Figure 3.17 (a). The resistance R_0 remains about 5mΩ, as shown in Figure 3.17 (b). The second branch values are random, but the RC time constant is stable at voltages above 1.25V, as shown in Figure 3.17 (c).

Table 3.2 Parameter Value of Two Branch Model for BCAP350 at Different Voltages

$V_{C0}(0)$ (V)	K_1	P_1	K_2	P_2	C_0 (F)	R_0 (mΩ)	C_2 (F)	R_2 (Ω)
0.272	3.872	-0.1608	5.044	-0.09338	256.955	6.036	30.16	0.276
0.512	16.39	-0.1225	0.8504	-0.04717	281.44	5.117	15.091	1.367
0.780	26.03	-0.1140	0.1509	-0.0010	295.535	5.198	190.661	5.22
1.04	34.82	-0.1112	0.2064	-32.56	300.89	5.274	0.202	0.148
1.29	44.54	-0.1013	0.0010	-0.1002	340.918	4.356	1.259×10^{-5}	7.928×10^{5}
1.54	52.62	-0.09699	0.0010	-0.1031	352.355	4.661	3.622×10^{-4}	2.678×10^{4}
1.82	57.68	-0.09560	3.617	-0.09558	352.302	5.092	1.247×10^{-6}	8.387×10^{6}
2.08	69.87	-0.09347	0.1470	-0.09340	360.138	5.107	6.174×10^{-7}	1.734×10^{7}
2.32	78.67	-0.09162	0.0010	-0.1151	370.144	4.887	3.922×10^{-3}	2.215×10^{3}
2.56	86.43	-0.08944	0.0100	-0.1670	377.465	5.016	0.038	159.251

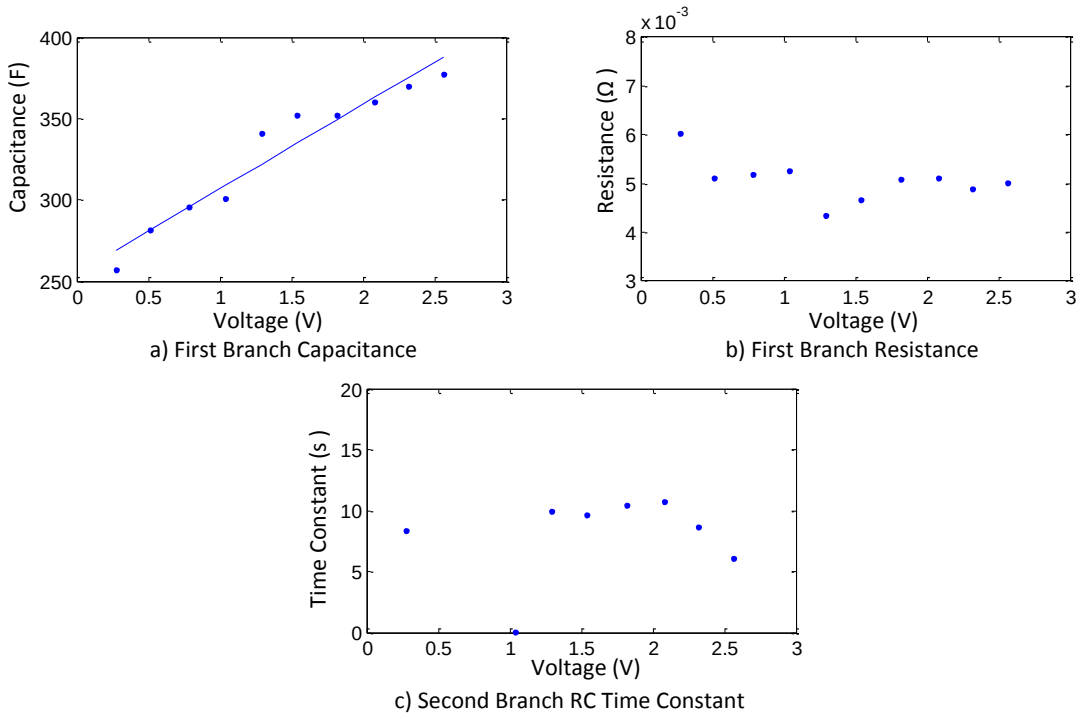


Figure 3.17 Parameter Variance Trend of the Two Branch Model using a BCAP350.

The proposed two branch model provides good agreement for SC discharge behaviour. The first branch RC values are stable, while the second branch RC values vary randomly though its effect on the accuracy is quite small as the current and voltage behaviours are mainly depended on the first branch values. Furthermore, the parameter values vary as the voltage changes. For better accuracy, the parameters need to be identified at the SC practical working voltage.

3.2.2 Variable Capacitance Model Parameter Identification Method Based on RC Discharge

The variable capacitance model, which employs a voltage dependent capacitor to represent the variable capacitance characteristic, provides a more accurate description of SC discharge behaviour. The parameter identification method is developed based on a mathematical model of the variable capacitor. The SC output

voltage and current are measured during the RC discharge process, and the model parameters are calculated based on the mathematical expression.

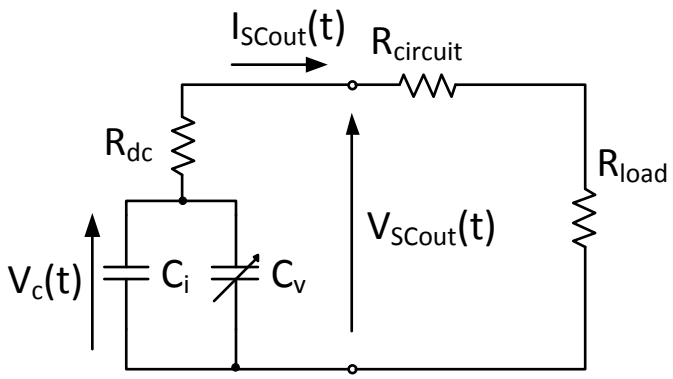


Figure 3.18 Variable Capacitance RC Discharge Model.

The circuit shown in Figure 3.18, the SC capacitor is represented by a fixed initial capacitor C_i in parallel with a voltage dependent capacitor C_V. It is assumed that the capacitance of the voltage dependent capacitor varies linearly with the coefficient k_v as defined in the three branch model, previously. The capacitance is defined as:

$$C_{SC}(V_{SCout}) = C_i + C_V = C_i + k_v \cdot V_{SCout} \tag{3.23}$$

The SC is connected to a resistive load R_{load}, and the circuit resistance, which is the wiring and switch resistance in the circuit. The SC output voltage is:

$$V_{SCout}(t) = V_c(0) \cdot \frac{R_{circuit} + R_{dc}}{R_{load} + R_{circuit} + R_{dc}} \cdot e^{-\frac{t}{(R_{load}+R_{circuit}+R_0)\cdot(C_0+K_V\cdot V_{SCout}(t))}} \tag{3.24}$$

The load resistance R_{load}, circuit resistance $R_{circuit}$ and internal resistance R_{dc} can be calculated directly from the measured SC output voltage and current. The fixed capacitance C_i and the variable capacitance coefficient k_v can be extracted by choosing two points on the SC output voltage plot during the RC discharge. By substituting the two points into equation (3.24), the parameters can be solved. In

order to increase model accuracy, the two points are chosen at $^1/_3$ and $^2/_3$ of the initial SC voltage, to cater for the whole discharge process.

The experiment is based on the circuit in Figure 3.14, and the parameter identification procedure is as follows:

1. Charge the SC to the set level by the external power supply;
2. Turn off the power supply 5 minutes to avoid the charge redistribution effects.
3. Turn on the switch to start the RC discharge and record the SC output current and voltage;
4. Based on the experimental result, the internal resistance R_{dc} is calculated from equation (3.25) with initial voltage drop ΔV at current I_{SCini};

$$R_{dc} = \frac{\Delta V}{I_{SCini}} \tag{3.25}$$

5. Choose two point from the SC output voltage plot $P_1(V_1, t_1)$ and $P_2(V_2, t_2)$, then the initial capacitance and voltage dependent coefficient are:

$$\begin{cases} C_0 = \dfrac{t_1 \cdot V_2 \cdot ln(V_2 \cdot A_0) - t_2 \cdot V_1 \cdot ln(V_1 \cdot A_0)}{R_{total} \cdot (V_1 - V_2) \cdot ln(V_1 \cdot A_0) \cdot ln(V_2 \cdot A_0)} \\ k_v = \dfrac{t_1 \cdot ln(V_2 \cdot A_0) - t_2 \cdot ln(V_1 \cdot A_0)}{R_{total} \cdot (V_1 - V_2) \cdot ln(V_1 \cdot A_0) \cdot ln(V_2 \cdot A_0)} \end{cases} \tag{3.26}$$

$$where\ A_0 = \frac{R_{total}}{V_c(0) \cdot (R_{circuit} + R_{load})}\ and\ R_{total} = R_{dc} + R_{circuit} + R_{load}$$

Based on the same experiment results shown in Figure 3.15, the variable capacitance model parameters are shown in Table 3.3.

Table 3.3 Variable Capacitance Model Parameters for SC Bank

Parameter	Value	Parameter	Value
$V_c(0)$	10V	R_{Load}	0.28 Ω
ΔV	0.4V	R_{circuit}	0.004 Ω
I_{SCini}	34A	R_{dc}	0.012 Ω
$P_1(V_1, t_1)$	$P_1(7V, 8.64s)$	C_0	88.382 F
$P_2(V_2, t_2)$	$P_2(3.5V, 26.84s)$	k_v	0.805

A comparison plot of the proposed variable capacitance model and original experiment results are shown in Figure 3.19.

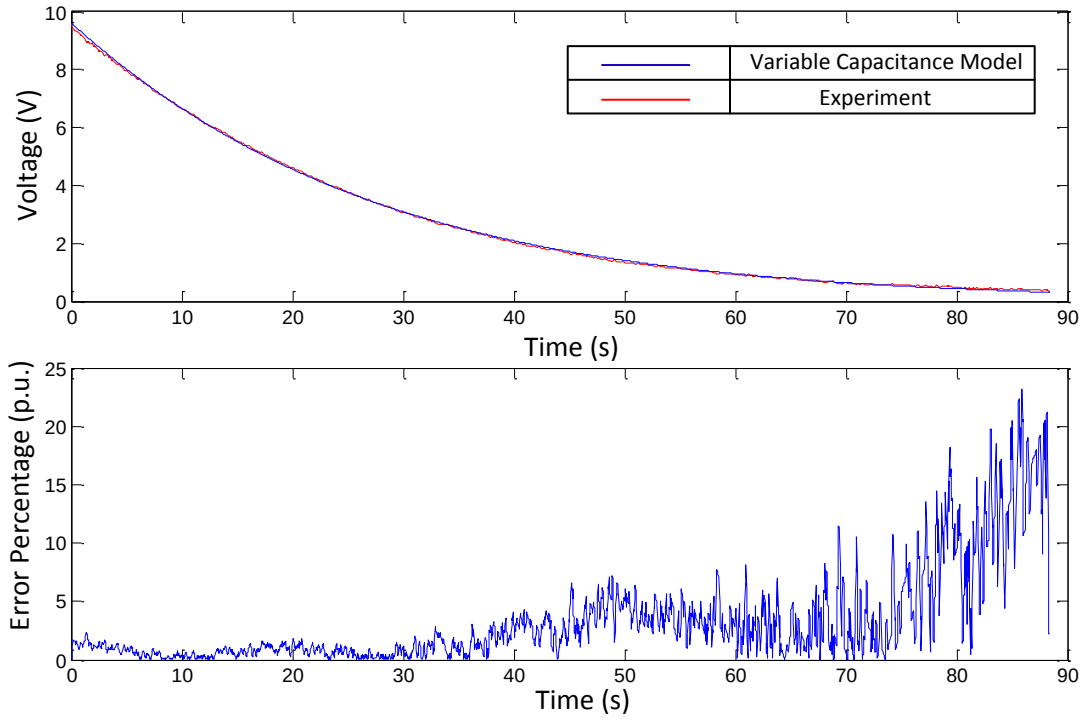


Figure 3.19 Comparison of the Variable Capacitance Model and Original Experiment Result & Error Percentage Plot.

As the result in Figure 3.19 show, the variable capacitance results are similar to the two branch model results, where high accuracy is shown for voltage above 2V (0.5V per SC). The error percentage is higher than the two branch model, which rises above 20%, as the voltage decreases. The reason for increased error is the decreased base value, but the absolute error is near constant.

Similarly, the parameters based on the 10 different voltage level experimentation are calculated to investigate the impact of the voltage on model parameters. The parameters are calculated based on the average value of R_{dc}, which is 4.46mΩ, and a circuit resistance of 4mΩ. The parameters values follow:

Table 3.4 Parameter Value of Variable Capacitance Model for BCAP350 at Different Voltage

$V_c(0)$ (V)	$P_1(V_1, t_1)$	$P_2(V_2, t_2)$	R_{dc} (mΩ)	C_i (F)	k_v
0.272	$P_1(0.18V, 2.33\text{s})$	$P_2(0.091V, 8.4\text{s})$	4.44	294.377	131.408
0.512	$P_1(0.34V, 2.29\text{s})$	$P_2(0.17V, 8.55\text{s})$	4.14	301.582	45.314
0.780	$P_1(0.52V, 2.47\text{s})$	$P_2(0.26V, 8.99\text{s})$	4.23	305.678	80.333
1.04	$P_1(0.69V, 2.42\text{s})$	$P_2(0.34V, 9.12\text{s})$	4.60	315.596	26.312
1.29	$P_1(0.86V, 2.44\text{s})$	$P_2(0.43V, 9.29\text{s})$	4.32	331.693	13.416
1.54	$P_1(1.03V, 2.49\text{s})$	$P_2(0.51V, 9.73\text{s})$	4.53	347.04	7.760
1.82	$P_1(1.21V, 2.62\text{s})$	$P_2(0.61V, 9.88\text{s})$	4.59	357.568	5.643
2.08	$P_1(1.39V, 2.64\text{s})$	$P_2(0.69V, 10.14\text{s})$	4.57	357.924	12.354
2.32	$P_1(1.55V, 2.75\text{s})$	$P_2(0.77V, 10.39\text{s})$	4.56	361.233	18.766
2.56	$P_1(1.71V, 2.88\text{s})$	$P_2(0.85V, 10.66\text{s})$	4.59	363.063	26.529

As the results in Table 3.4 show, parameter variance shows a similar trend as the two branch model, where the SC capacitance increases as the voltage increases. In

Figure 3.20 (a), the initial fixed capacitance increases as the voltage increases, while in Figure 3.20 (b), the internal resistance remains about 4.46mΩ. In Figure 3.20 (c), the voltage dependent coefficient decreases as the voltage decreases for the SC voltages above 1.5V, and then varies randomly as the voltage decreases.

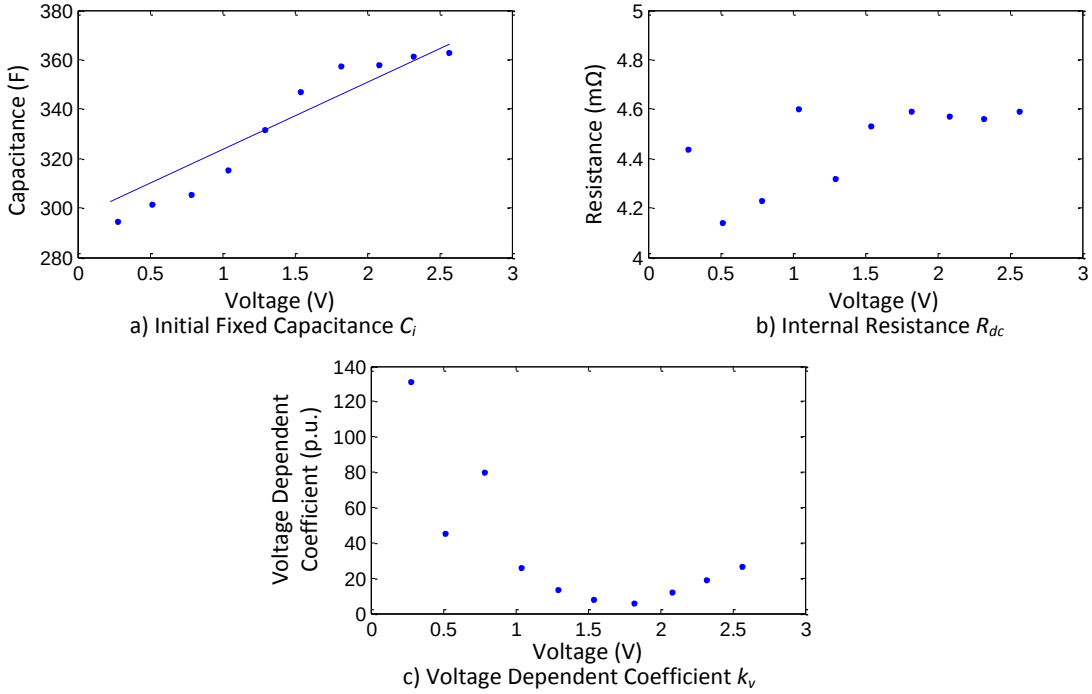


Figure 3.20 Parameter Value Variance Trend of Variable Capacitance Model for the BCAP350.

As the experimental results show, the accuracy of variable capacitance model is similar to the two branch model for the SC voltages above half of the initial value. The accuracy decreases as the SC discharges. Furthermore, the parameter values vary as the SC voltage changes. For better accuracy, each parameter needs to be identified at the voltage level of the SC practical working condition. Parameter values of the variable capacitance model mainly depend on the chosen calculation points, where a small reading error can result in a large difference in the calculated value. As a result, precise measurement and reading of the chosen points is essential for parameter identification.

3.2.3 Comparison of the Proposed Methods with the Classic Model

The proposed model parameter identification methods, which are based on the two branch model and variable capacitance model, accurately model SC discharge behavior. The error percentage is within 5% for the SC operating above half its initial voltage, which is the typical SC working range. However, the parameters of second branch in the two branch model vary randomly, which improves the agreement between the model and experimentation. The classic model, which contains a single RC branch, is more convenient in efficiency analysis. Based on the RC discharge of the BCAP350, the three models are compared when discharging from 2.5V.

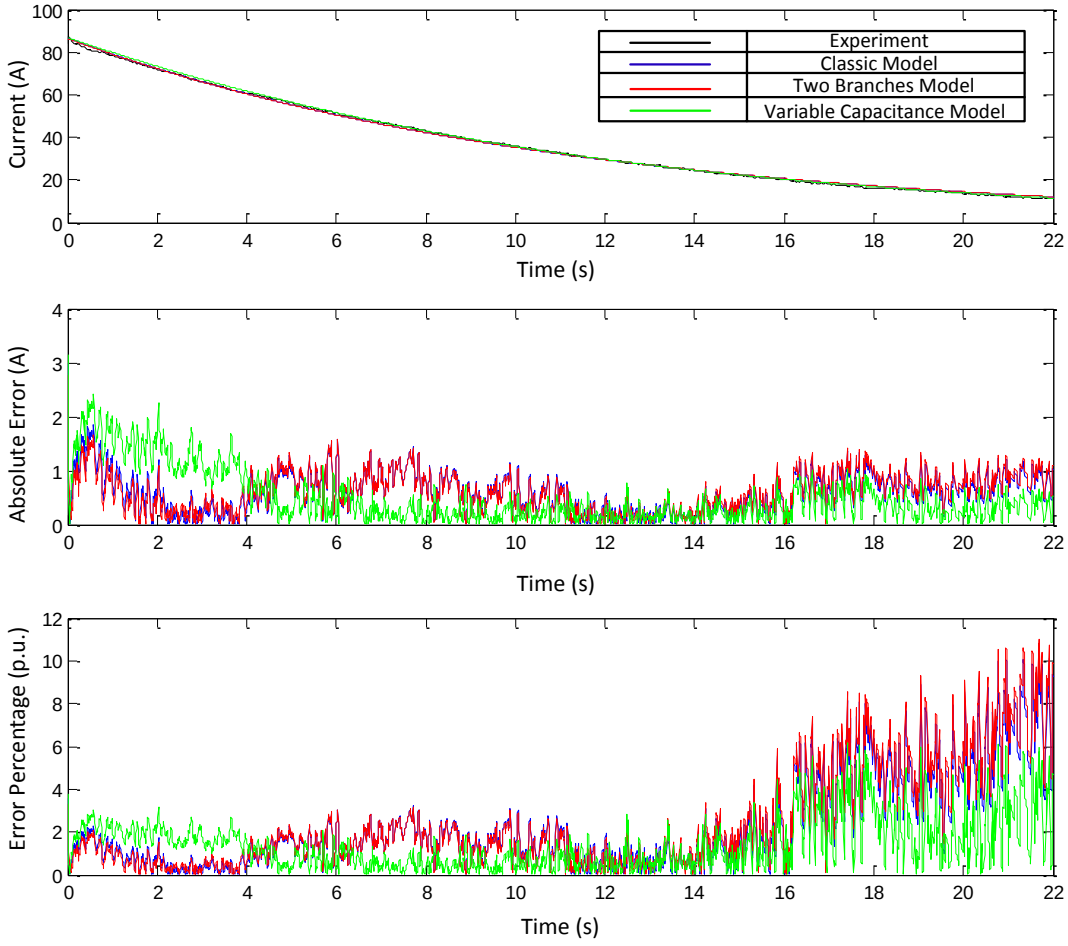


Figure 3.21 Comparison of the Classic Model, Two Branch Model and Variable Capacitance Model.

As the comparison result in Figure 3.21 show, all three models provide good accuracy in describing SC discharge characteristics. The accuracy of the classic model is almost identical to those of the two branch model. The variable capacitance model has a higher error at start of SC discharge, and the error falls below the other two models after $^1/_3$a third of the discharge process. As the difference in the three models is less than 1%, the classic model, due to its simplicity, is more efficient and convenient in simulation and efficiency analysis of the SC discharge process.

3.3 Critical Discussion

Based on the SC model review, different topologies have been developed to illustrate SC characteristics. Different models better suit different operating conditions. The parameter identification method depends on the model topology, where identification method difficulty increases as model complexity increases. The merits and limitations of the different model topologies and parameter identification methods are discussed in terms of operating conditions.

3.3.1 SC Model Discussion

The SC is normally represented by a capacitor in series with an internal resistor, plus a parallel shunting resistor to cater for the self-discharge phenomena. However, due to the complex physical construction, the single RC branch model may not accurately describe the SC, especially the nonlinear capacitance variance with the voltage and charge redistribution phenomena. The SC models are mainly divided into four topology types, namely the single RC branch model, multi RC-branch model, variable capacitance model, and the complex impedance and transmission line models.

The single RC branch model, known as the classic model, is widely used in SC analysis. The model only describes the short-term SC charge/discharge process, while long-term behaviour, such as charge redistribution phenomena, is ignored. Based on the experimental results, the single RC branch model shows the same accuracy as the two branch model and variable capacitance model in terms of the SC discharge process. Although model accuracy is lower than with the other models in

the full range analysis, its simplicity enables a more convenient and efficient method for developing analytical models.

The multi-branch model is developed based on the physical construction of the SC, where the large number of parallel RC branches represents the infinite number of the pore capacitors and resistors. The RC branches represent different characteristics of the SC. For example, in the three branch model the branches are divided based on the charge redistribution phenomena, while in the ladder model the branches refer to the SC frequency response. In most multi-branch models, the number of the parallel RC branches is limited. As the branch number increases, the identification process becomes more complicated and analysis based on such models can be inefficient. The automatic order selection method based on the ladder model, attempts to achieve optimal usage of the multi-branch model, but the complex parameter identification process is the key model weakness.

The variable capacitance model, which employs a voltage dependent capacitor to describe the nonlinear capacitance characteristic, gives high accuracy for the SC charge/discharge process. However, as the experiment shows, even with a variable capacitance model, the parameter values vary as the voltage changes. It is important for improving model accuracy that the parameter is identified based on the practical operation voltage range.

The complex impedance and transmission line models are an extension of the multi-branch model, which employ different expressions to reduce the number of parameters used with the multi-branch model. Although the number of parameters is reduced, identification requires a large number of experiments. The complex impedance and transmission line models provide high SC behaviour accuracy, and are suitable for both time domain and frequency domain analysis. However, the associated simulation and necessary analysis is difficult to develop for such models.

In general, the more complex the model, the higher the accuracy, but the more difficult to identify the parameters and apply in practical simulation and analysis. The SC model is developed based on one or a combination of topologies, such as the three branch model which combines the variable capacitance model and the multi-branch model. The choice of the model depends on the SC practical operation

conditions. According to the experimental results, the accuracy of the single branch model, two branch model, and variable capacitance model is the same when describing the SC discharge process.

3.3.2 SC Model Parameter Identification Discussion

A variety of SC model topologies have been developed to describe SC electrical and thermal characteristics. Depending on the operation conditions, a specific model is selected to fit the practical situation. Although a complex topology improves model accuracy, the model parameters play a key role in developing the model. Parameter identification is paramount in SC modelling, where most of the parameters are identified based on practical experiment to improve the accuracy. Although the parameter identification method varies for the different SC model topologies, the identification methods can be grouped in two main categories, namely time or frequency domain identification methods.

Time domain identification methods, which applied to the classic model, three branch model, and transmission line model, focus on the time domain response of the SC during charge, discharge, and standby. The main RC branch parameters which represent the short-term response are identified by the charging or discharging processes, generally based on a constant current condition. The disadvantage of the constant current method is that the experimental circuit requires complex control to achieve the constant current condition. Additionally, it is difficult to ensure ideal constant current in a practical experiment, where reading error is introduced by small current oscillations. Because the SC internal resistance is at the milliohm level, a small error results in a large variation in parameter value.

The two proposed identification methods are based on discharge the SC with a resistor, which simplifies the experiment circuit and overcomes the error from the non-ideal constant current. According to the experiment results, the capacitance, of which the first branch capacitor in two branch model and the initial capacitor in variable capacitance model, is affected by the SC voltage. To achieve a better accuracy of the model, the parameters need to be identified within its practical working voltage range. For the mid-term and long-term RC branches, the parameters

are identified by disconnecting the SC for certain time, which is inefficient compared to the frequency domain identification method.

The frequency domain identification method, which is applicable to the ladder model and complex impedance model, is based on the EIS meter. The model parameters are identified from the SC impedance plot. The advantage of the frequency domain method is the high accuracy of the model resistive parameter, and a good agreement of the medium and long term behaviour [3.7]. However, an accurate impedance plot requires a large number of experiments, and the impedance response varies as the test conditions change. The frequency domain identification method is suitable for identification of the medium and long term parameters, which tends to the stand by behaviour.

The application of the two parameter identification methods depends on the SC model. For SC charge/discharge analysis, a time domain method is more convenient, while the frequency domain method gives better fit for the medium and long term analysis. The identification methods can also be combined, such as in the on-line method introduced in [3.7]. In [3.7], the frequency response is used for resistive parameter identification, while the time domain response is used for capacitance identification.

3.4 Summary

Table 3.5 Supercapacitor Model Compare

Model	Topology Complexity	Model Accuracy	Parameter Identification Complexity
Classical RC	Low	Medium	Low
Variable Capacitance	Medium	Medium	Medium
Multi Branches	High	High	High
Transmission Line	High	High	High

Supercapacitor modelling involves two aspects, namely the model topology and the parameter identification method. In general, higher topology complexity results in a more complex parameter identification method. Different models are suitable for different application conditions. Several different models with their parameter identification method have been reviewed in this chapter, and applicable application conditions for each model were discussed. A comparison of topology complexity, accuracy, and parameter identification method complexity, for the supercapacitor models, is presented in Table 3.5. The classic RC model has a good accuracy in representing SC charge/discharge behaviour with a simple topology and easy parameter identification method. For the variable capacitance model, although the topology complexity is increased, it shows a similar the accuracy as the classic model. The multi-branch model and transmission line models have an improved accuracy especially for the full frequency spectrum responses. However, the complexity of the models and parameter identification methods limit their applications.

Two novel parameter identification methods, based on the two branch and variable capacitance topologies, were demonstrated. These two methods use a simple experimental method to extract model parameters with an acceptable accuracy.

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Chapter 4

4 Combined Supercapacitor and Electrolytic Capacitor Energy Storage System

With the rapid development of renewable energy technology, distributed generation has been identified as a major contributor to future power systems. Connection of increasing amounts of distributed generation to the network poses significant challenges in terms of grid code compliance. In particular, low-voltage ride through requirements, where a generator must remain connected to the grid for a specified duration (E.ON grid code: 150ms, UK grid code: 140ms [4.1, 2]) during a fault or load change induced voltage dip to a predefined percentage of the nominal value (0% in some cases), are a major consideration in the design of distributed generation systems. Energy storage systems that are able to supply transient energy efficiently to the network can assist with low-voltage ride through compliance requirements.

Supercapacitors (SC) are a storage technology that has been proposed as a means of supplying short-duration transient energy [4.3]. The inherent long time constant (~1s) associated with the supercapacitor means that this short-term energy transfer is inefficient. It is proposed here, that the overall efficiency of the supercapacitor based transient energy supply system can be significantly improved by combining the supercapacitor with parallel connected capacitor having a lower time constant. In this case the parallel capacitor is an electrolytic type, due to the relatively high capacitance per unit volume compared to other capacitor types. The supercapacitor can therefore provide energy efficiently to cater for the lower bandwidth component of the transient whilst the parallel connected electrolytic capacitor, with its relatively short time constant (~1ms), demonstrates better efficiency and faster response during high-current short-duration transients [4.4, 5].

The proposed parallel capacitor technique improves the efficiency of transient energy supply by over 10% when compared to a system based only on the supercapacitor. Mathematical models, simulation and experimental results are presented to validate the concept. The characteristics of the combined supercapacitor and electrolytic

capacitor system are verified experimentally. A design guide for the combined energy storage system is introduced to achieve an optimal solution for efficiency, output power, and capacitor size. A three branch model, where a third branch with a lower time constant such as that of a polyethylene capacitor, is developed as an extension of the two capacitor (SC plus electrolytic) parallel system. The frequency analysis of the two and three branch models are analysed.

4.1 Supercapacitor and Electrolytic Capacitor Energy Storage System

The supercapacitor, which offers higher energy density than conventional electrolytic capacitors, is a suitable energy storage device in high power pulse applications [4.6]. However, due to its high internal resistance [4.7, 8], the power capability and efficiency of a supercapacitor are lower than those of a conventional capacitor. Charge and discharge times for supercapacitors typically lie in the range 0.36s to 360s with an average efficiency of 86% [4.9]. Based on the SC characteristics analysis in Chapter 2, parameters for the BCAP0350 SC were incorporated into the model used to investigate discharge time, energy transfer efficiency, and percentage energy loss for constant current discharge, at different constant current levels.

Table 4.1 Corresponding Performance of BCAP350 at Different Current Level

	Test Condition	I_{out}	T_{ccdis} (s)	$\eta_{transfer}$	η_{loss}
a	Maximum Continuous Current	34A	26.67s	92.1%	7.7%
b	Maximum Peak Current	220A	3.18s	54.7%	38.6%
c	Maximum Energy Loss	420A	1.13s	25.2%	50%
d	Short Circuit Current	840A	0s	0%	0%

Figure 4.1 presents the results of the modelling exercise, whilst Table 4.1 highlights the corresponding performance indicators. Discharge time T_{ccdis} defines the time for the supercapacitor to discharge at a specified current level from its maximum voltage to its residual voltage. Energy transfer efficiency $\eta_{transfer}$ is defined as the ratio of the transferred energy to the total energy stored in the supercapacitor, where energy loss in the internal resistor and residual energy are included. The energy loss percentage

η_{loss} is defined as the ratio of energy loss in the internal resistor to the total stored energy.

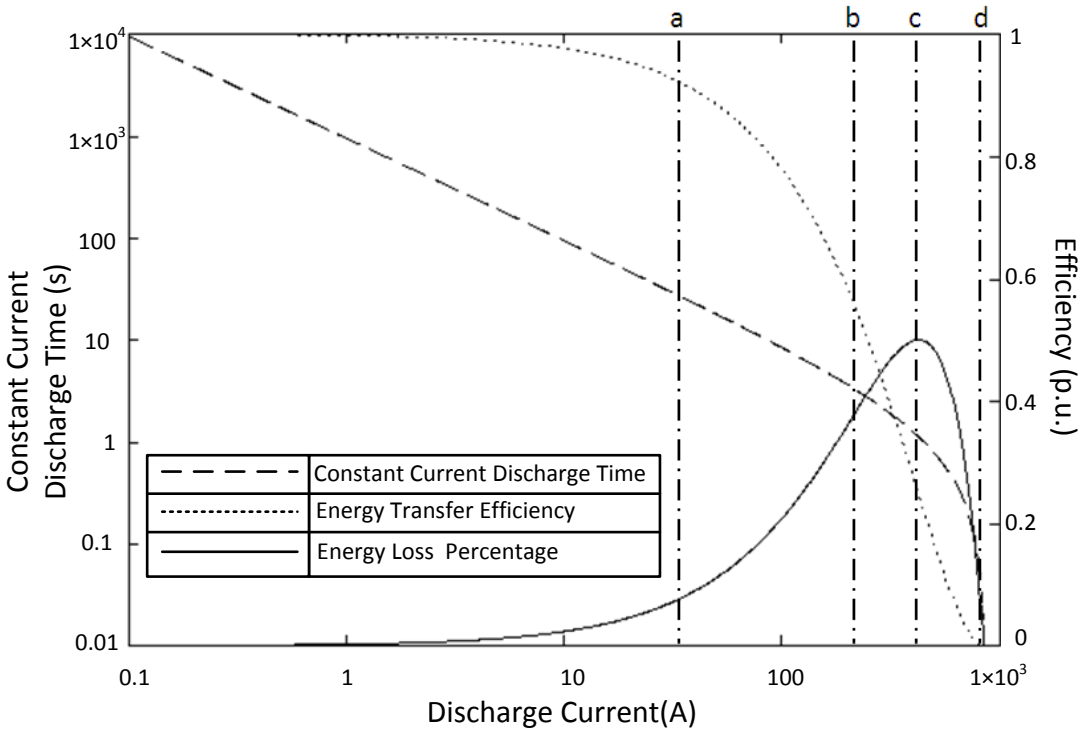

Figure 4.1 Discharge Characteristics for BCAP350 at Constant Current.

From the 'energy transfer efficiency' characteristic, at 54.7%, the efficiency of maximum peak current discharge is 30% lower than the average value. Specifically, Figure 4.1 highlights the low efficiency associated with short-duration, high-current discharge.

It is proposed that significant improvement in the efficiency of high-current (a discharge current in the range between the SC's maximum continuous current and its maximum peak current, which for the BCAP0350 are 34A and 220A respectively [4.8]), short-duration (<1s) energy transfer can be achieved by connecting a suitably sized and rated electrolytic capacitor EC in parallel with the supercapacitor (SCEC). The electrolytic capacitor has better power capability, lower internal resistance, and faster response time than the supercapacitor. The SC is therefore able to meet the

steady-state and slow transient current requirements whilst the electrolytic capacitor meets the fast transient requirement, resulting in increased overall system efficiency.

4.1.1 Introduction of Electrolytic Capacitor

The electrolytic capacitor (EC), (unlike the thin metallic film layer structure of a standard capacitor), has one electrode, usually the cathode, that is a semi-liquid electrolyte along with a metallic film anode [4.10, 11]. Depending on the anode electrode material, the EC is categorised as either an aluminium or a tantalum electrolytic capacitor. The EC dielectric is a thin oxide layer which is electro-chemically formed on the anode metallic material with a thickness of less than ten microns. Due to this thin dielectric, the EC achieves a large capacitance within a small physical volume [4.11]. An example of the aluminium electrolytic capacitor structure is shown in Figure 4.2. Most electrolytic capacitors are polarised, where the capacitor terminals must connect in the correct polarity to a dc voltage. Reverse polarity connection can break down the dielectric oxide layer, resulting in permanent damage.

Although EC capacitance is less than that of the SC, its cell voltage is much higher than the SC. Typically, the aluminium electrolytic capacitor has a higher capacitance and voltage rating than the tantalum electrolytic capacitor, however, the tantalum capacitor is more stable and has a lower leakage current [4.10, 12]. In a combined SCEC system used as an energy storage device in a power system, the aluminium electrolytic capacitor (as opposed to a tantalum capacitor) is more suitable for the energy storage purposes because of the availability of higher capacitances.

The aluminium electrolytic capacitor uses either a plain foil or an etched foil. The etched foil type, which the anode and cathode are chemically etched to increase the surface area, produces higher capacitance than the plain foil type, for a giving volume. However, the capacitance tolerance range is much higher and can exceed ±20%, while the resistance and leakage of the etched foil type is higher than that of the plain foil type [4.5, 11].

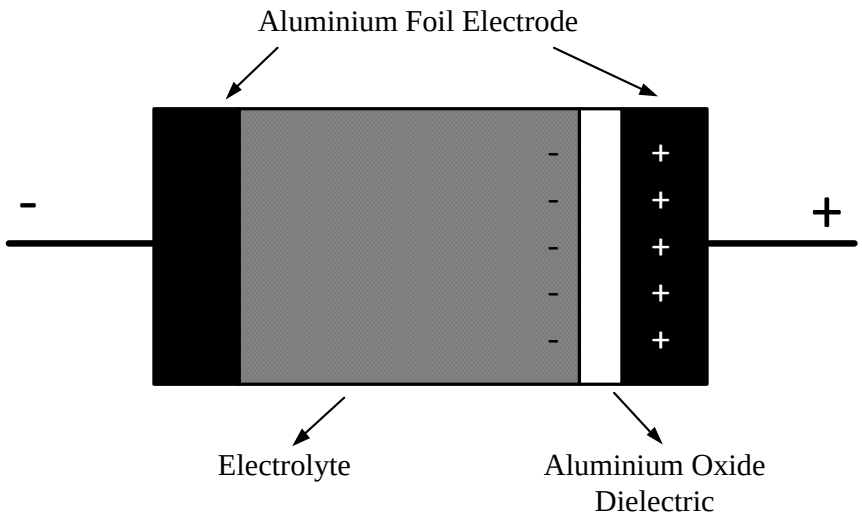

Figure 4.2 Electrolytic Capacitor Structure.

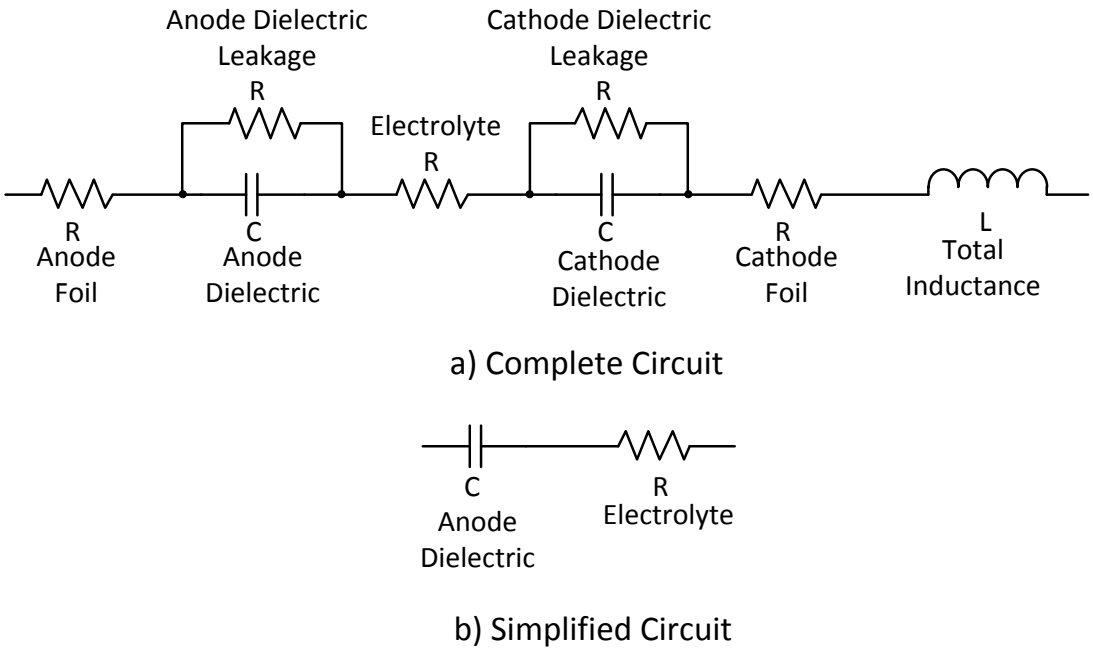

Figure 4.3 Equivalent Circuit of Aluminium Electrolytic Capacitor.

Based on its physical structure, the equivalent circuit of an aluminium electrolytic capacitor contains elements as shown in Figure 4.3 (a). Since the capacitance of the cathode is usually much greater than that of the anode, and the anode and cathode

foil resistances are small enough to ignore, the EC equivalent circuit can be simplified to a single RC branch as shown in Figure 4.3 (b), for analysis of low frequency applications [4.11].

The electrolytic capacitor, which has a higher capacitance to volume ratio and lower cost performance than other conventional capacitor types, is applicable to filtering and energy storage power systems [4.13]. Due to its key function of dc bus voltage stabilisation and transient energy storage in power systems, EC performance can directly affect system stability [4.14]. However, the major EC drawback is its low reliability. It is reported that the electrolytic capacitor has the highest failure possibility, compared to other power electronic devices, such as IGBT, power MOSFET, and power diode [4.15]. In electronic equipment, about 30% of breakdowns are caused by static converters, of which half of faults are due to electrolytic capacitors [4.16].

For aluminium electrolytic capacitors, vaporisation of electrolyte and its loss through the end seal is the primary wear-out mechanism [4.17]. Electrolyte vaporisation leads to an increase in the equivalent series resistance and a capacitance decrease, so that these parameters drift out of specified range, whence the EC is considered to have failed. Additionally, the EC operates at a high current level, so that any increase on resistance accelerates the wear-out process due to the increased internal heating [4.13]. The typical operation temperature for aluminium electrolytic capacitor is 85℃ and for special constructed high temperature capacitor, the limit can rise to 105℃ and 125℃. For an EC operating at high temperature, the vaporisation process is accelerated which greatly decreases capacitor life time [4.11]. Generally, a 10℃ operating temperature decrease doubles EC lifetime. As a result, it is important to identify the operating ripple current level and temperature during the design process.

4.1.2 SCEC Energy Storage System Mathematical Modelling

From the SC models in Chapter 3, the supercapacitor theoretical model consists of a number of parallel connected resistor-capacitor branches, where the capacitance terms are voltage dependent and the resistance terms depend on several physical

parameters [4.18]. Such a model is complex and of minimal practical use. Several less complicated SC models have been developed and are categorized as a classical model, a variable capacitance capacitor model, a multi-branch model or a transmission line model [4.19-21]. Of these, the more complex models, such as the multi-branch and transmission line model, provide better accuracy when modelling medium or long term discharge characteristics, or the charge redistribution phenomena. However, the parameter identification process for these models requires detailed analysis of the operating characteristics or complex experimental procedures [4.21-23].

Since the application here focuses on short-term (<1s) discharge, the SC model is simplified as shown in Figure 4.4. Based on the classical approach, the model has a single branch consisting of an ideal capacitance *C* in series with an internal resistance R_{dc}. A constant current source I_{out} is used to define the capacitor discharge characteristics.

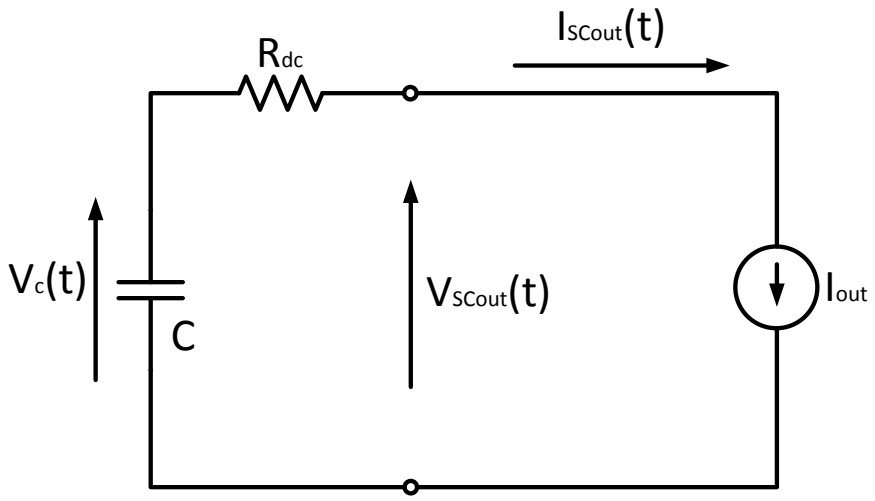

Figure 4.4 SC Constant Current Discharge Model.

The SC constant current discharge mathematical model for Figure 4.4 is developed in Chapter 2, where the following quantities were defined for efficiency analysis:

SC output energy:

$$E_{SCout} = \int_0^t V_{SCout}(t) \cdot I_{SCout}(t)\, dt \quad \textbf{(4.1)}$$

SC energy loss:

$$E_{SCloss} = \int_0^t I_{SCout}(t)^2 \cdot R_{dc}\, dt \quad \textbf{(4.2)}$$

SC output energy efficiency:

$$\eta_{SC}(t) = \frac{E_{SCout}}{E_{SCout} + E_{SCloss}} \quad \textbf{(4.3)}$$

Figure 4.5 extends the model in Figure 4.4 to represent the proposed combined supercapacitor and electrolytic capacitor system, under constant current discharge. In Figure 4.5, C_{SC} and R_{SC} represent the SC elements, and C_{EC} and R_{EC} represent the EC elements.

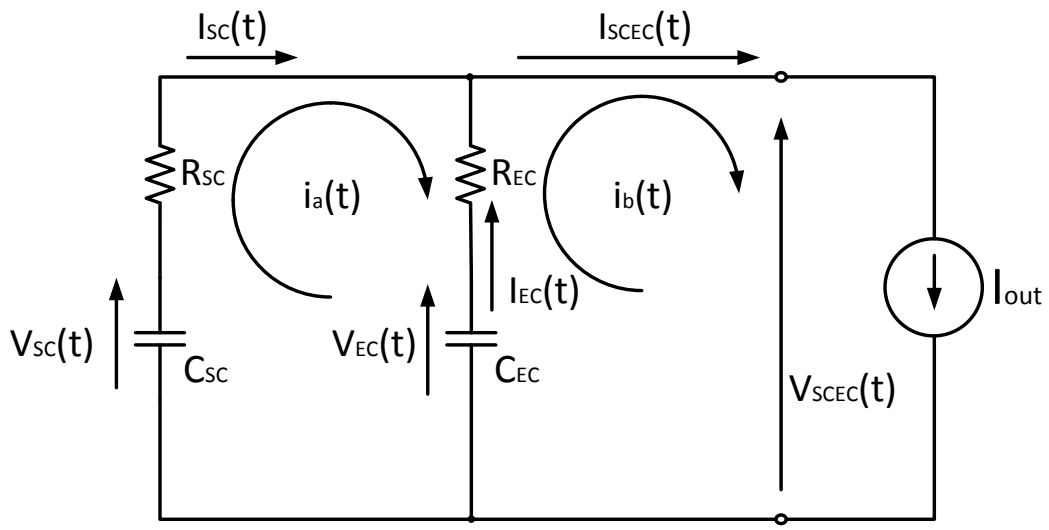

Figure 4.5 SCEC Constant Current Discharge Model.

Similarly, efficiency analysis equations based on Figure 4.5 for the combined SCEC system are developed as follows:

Supercapacitor current:

$$I_{SC}(t) = i_a(t) = \frac{B}{D} + \left(\frac{A}{C} - \frac{B}{D}\right) e^{-\frac{D}{C} \cdot t}$$

$$where$$

$$A = V_{SC}(0) - V_{EC}(0) + I_{out} \cdot R_{EC}, B = \frac{I_{out}}{C_{EC}}, C = R_{SC} + R_{EC} \quad \textbf{(4.4)}$$

$$and\ D = \frac{1}{C_{SC}} + \frac{1}{C_{EC}}$$

Electrolytic capacitor current:

$$I_{EC}(t) = i_b(t) - i_a(t) = I_{out} - I_{SC}(t) \quad \textbf{(4.5)}$$

Output energy of SCEC system:

$$E_{SCECout} = \int_0^t V_{SCECout}(t) \cdot I_{out}\, dt \quad \textbf{(4.6)}$$

SCEC system energy loss:

$$E_{SCECloss} = E_{SCloss} + E_{ECloss} = \int_0^t I_{SC}(t)^2 \cdot R_{SC}\, dt + \int_0^t I_{EC}(t)^2 \cdot R_{EC}\, dt \quad \textbf{(4.7)}$$

SCEC system output energy efficiency:

$$\eta_{SCEC}(t) = \frac{E_{SCECout}}{E_{SCECout} + E_{SCECloss}} \quad \textbf{(4.8)}$$

Equations (4.4) to (4.8) facilitate detailed analysis of the system proposed in Figure 4.5. With fixed SC parameters and variable electrolytic parameters, equations (4.4) and (4.5) can be used to analyse the current sharing relationship between the parallel connected capacitors under constant current discharge conditions, thereby enabling the effect of the electrolytic capacitor on system performance to be determined. Based on this analysis:

1. The initial current from electrolytic capacitor depends upon its internal resistance R_{EC}. Lower R_{EC} results in greater initial current from the electrolytic capacitor.
2. The steady-state electrolytic capacitor current depends upon capacitance C_{EC}. Increasing C_{EC} results in greater electrolytic capacitor current in the steady-state.

Based on these observations and analysis using equations (4.6) to (4.8), it can be concluded that a parallel connected electrolytic capacitor with high capacitance and low internal resistance results in improved system efficiency. Additionally, based on (4.3) and (4.8), efficiency is mainly dependent upon discharge current and discharge time if the capacitor parameters are fixed.

4.2 SC and SCEC Energy storage System

Based on the mathematical models, the SCEC system provides better performance in both transient and steady-state than the SC system. In order to verify the proposed SCEC system, both simulation and experimentation are developed based on the practical SCs and ECs. Parameters of the SC are identified according to the test constant current condition. The efficiency improvement, which is determined by the discharge time and current level, are compared under different test conditions, by simulation and experimentation. Simulation and experiment results are compared with the mathematical calculation results. Potential improvement in transient power capability and response time are discussed for boost converter applications.

4.2.1 Series SC Bank Parameters Identification

The supercapacitor bank used in the SCEC experiment is four series connected Maxwell BCAP0350 SCs. Based on the datasheet [4.8], each cell of the supercapacitor bank has 3.2mΩ resistance and 350F capacitance. Theoretically, the series supercapacitor bank has a resistance of 12.8mohm and capacitance of 87.5F. However, the experimental results differ from the theoretical values, mainly due to product tolerance and connection topology. As introduced in Chapter 3, SC model parameters based on the practical operating conditions provide better accuracy. As

the experimental verification is based on a constant current discharge, the identification for the series SC bank parameters is based on the following profile:

1. Charge the SC bank to a certain value, chosen as 10V and 8V in these experiments.
2. Discharge the supercapacitor bank under a constant current condition, where the current levels are 106A, 70A, and 50A.

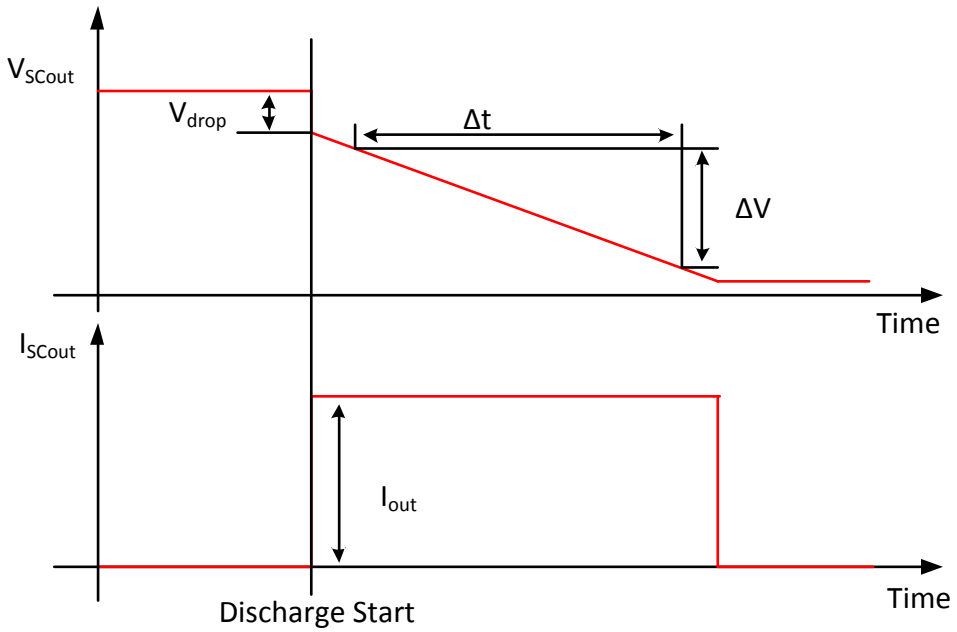

Figure 4.6 Typical Constant Current Discharge Plot of the SC Bank.

3. Record the SC output voltage and current, as in the typical constant current discharge plot shown in Figure 4.6. By identifying the initial voltage drop V_{drop}, constant current I_{out}, and voltage change ΔV within a certain period Δt, the capacitance and resistance of the single RC branch model is calculated as:

$$C_{SC} = \frac{I_{out} \cdot \Delta t}{\Delta V} \quad \textbf{(4.9)}$$

$$R_{dc} = \frac{V_{drop}}{I_{Out}} \quad \textbf{(4.10)}$$

Table 4.2 Resistance and Capacitance of SC Bank at Different Test Condition

Test Condition		Parameters Value	
Voltage (V)	**Current (A)**	R_{dc}**(Ω)**	C_{SC}**(F)**
10	106	0.0213	96.09
	70	0.0224	94.35
	50	0.0288	94.7
8	106	0.0276	94.86
	70	0.0308	98.64
	50	0.0319	94.22

The parameters are identified based on the proposed method at different initial voltage and current levels. The calculated resistance and capacitance of the classic model is shown in Table 4.2. According to the experimental results, the SC capacitance and resistance for further efficiency analysis and simulation, are 95F and 25mΩ.

4.2.2 Simulation and Experimental Verification

Figure 4.7 shows the Matlab Simulink simulation model for the combined supercapacitor and electrolytic capacitor energy storage system. Constant current discharge is realised using a boost converter with a 40kHz switching frequency. Current is regulated using a PI controller, with proportional gain $K_P = 0.01$ and integral gain $K_I = 5$ chosen to give a slightly overdamped control characteristic.

In both the simulation and experimental systems, the supercapacitor bank is comprised of 4 series connected BCAP0350 SCs having a total capacitance of 95F and a total internal resistance of 25mΩ, giving an associated time constant of τ = 2.38s. The 16V electrolytic capacitor, can be readily connected and disconnected to enable the performance of both energy storage systems (SC only and SCEC) to be investigated, has capacitance of 0.47F and internal resistance of 6mΩ, giving an associated time constant of τ = 2.82ms. The capacitors are connected to a MOSFET based dc-dc boost converter, where a Hall-effect current transducer (100kHz bandwidth) and a dsPIC30F2020 controller are used to regulate the discharge current.

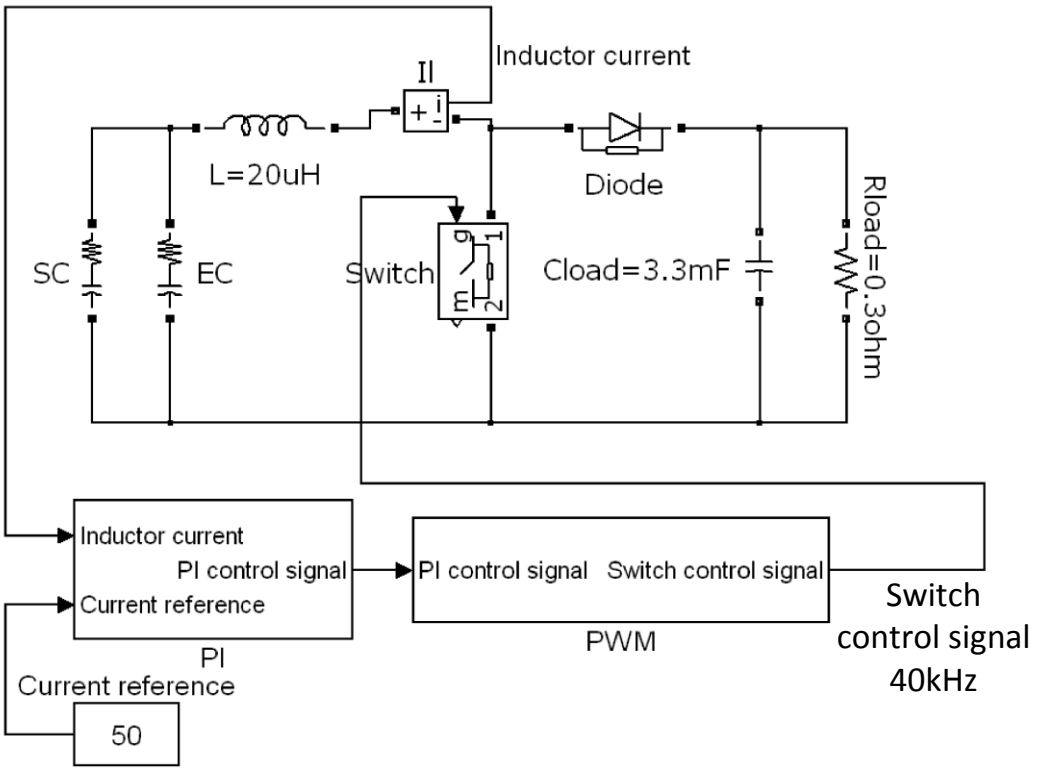

Figure 4.7 Matlab Simulink simulation model for the SCEC Energy Storage System.

The experimental procedure involves using a dc power supply to charge the capacitors to a predefined voltage. The power supply is removed and the capacitors are discharged into the resistive load at a defined reference current level, regulated by the PI-controlled boost converter. In the experiment circuit in Figure 4.8, S1 and S2 are controlled to enable the constant SCEC output current, while S3 is used to prevent unwanted discharge via D2 before the boost converter operation and is closed when the constant current discharge process starts. Currents and voltages for both the supercapacitor and electrolytic capacitor are recorded and are processed off-line using Matlab.

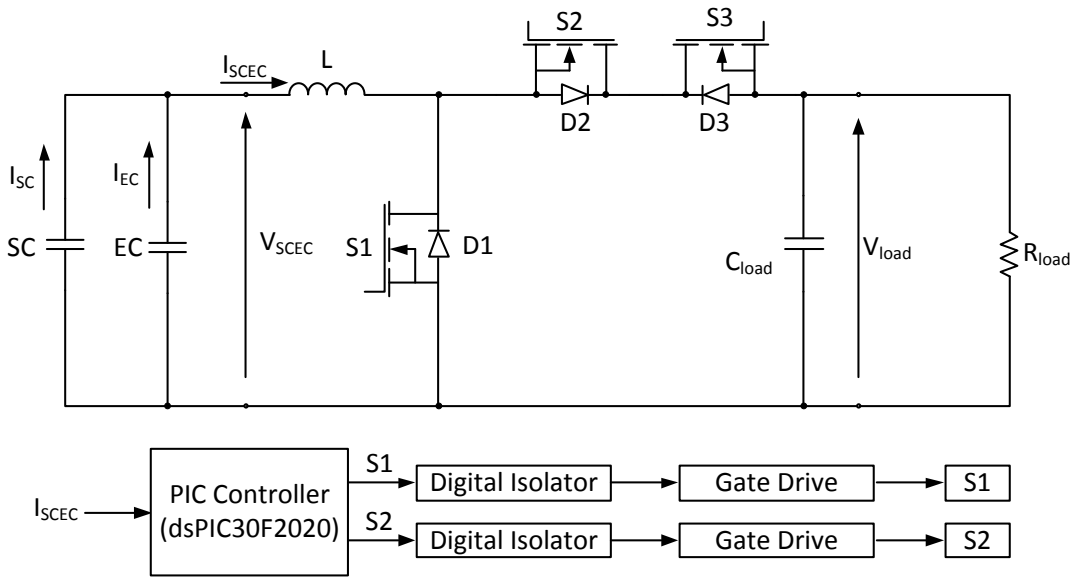

Figure 4.8 Experiment Circuit for SCEC System Constant Current Discharge.

Simulations and experiments focus on discharge time and current, since these are the two main factors affecting system efficiency. The relationship between efficiency and discharge time is investigated based on an initial total capacitor voltage of 10V and 106A discharge current. The relationship between efficiency and discharge current is investigated based on a 10V initial total capacitor voltage and a 20ms discharge time. Discharge current references are chosen in the range between the supercapacitor's rated maximum continuous current and its rated peak current [8].

4.2.3 Simulation and Experiment Result

The results for the mathematical model, simulation, and the experiment, with common parameter values and test conditions, are recorded and processed using Matlab. Figure 4.9 shows the mathematical, simulated, and experimental efficiencies as a function of discharge time t_d for both the SC and combined SCEC energy storage systems. The combined supercapacitor and electrolytic capacitor system shows improved efficiency across the entire discharge duration: the greatest improvement in the period shortly after discharge commences and reduces as the discharge progresses.

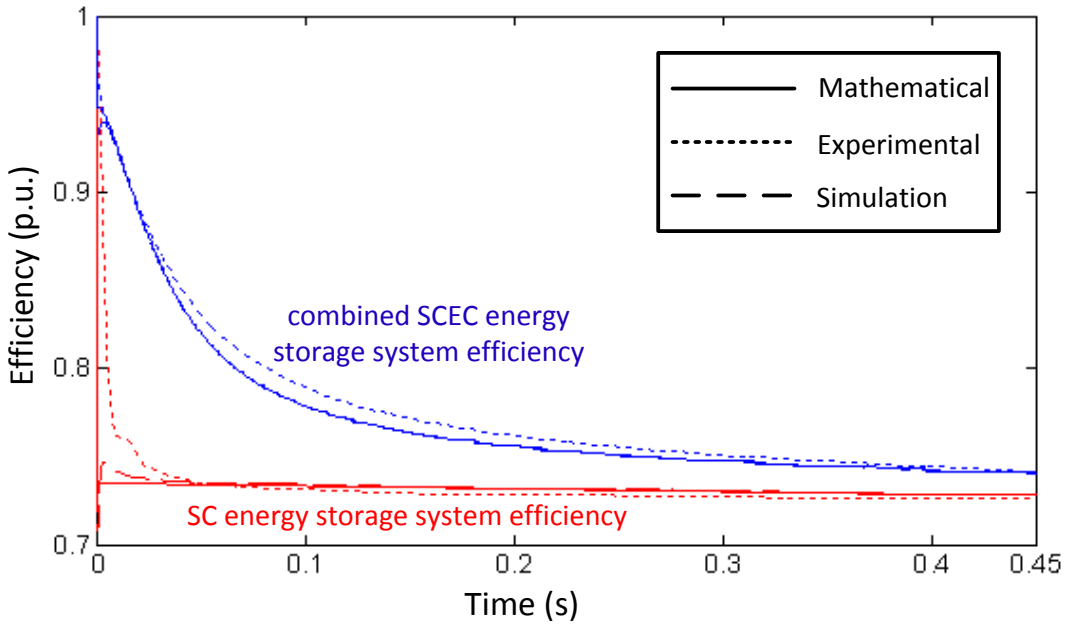

Figure 4.9 Efficiency versus Discharge Time at 106A.

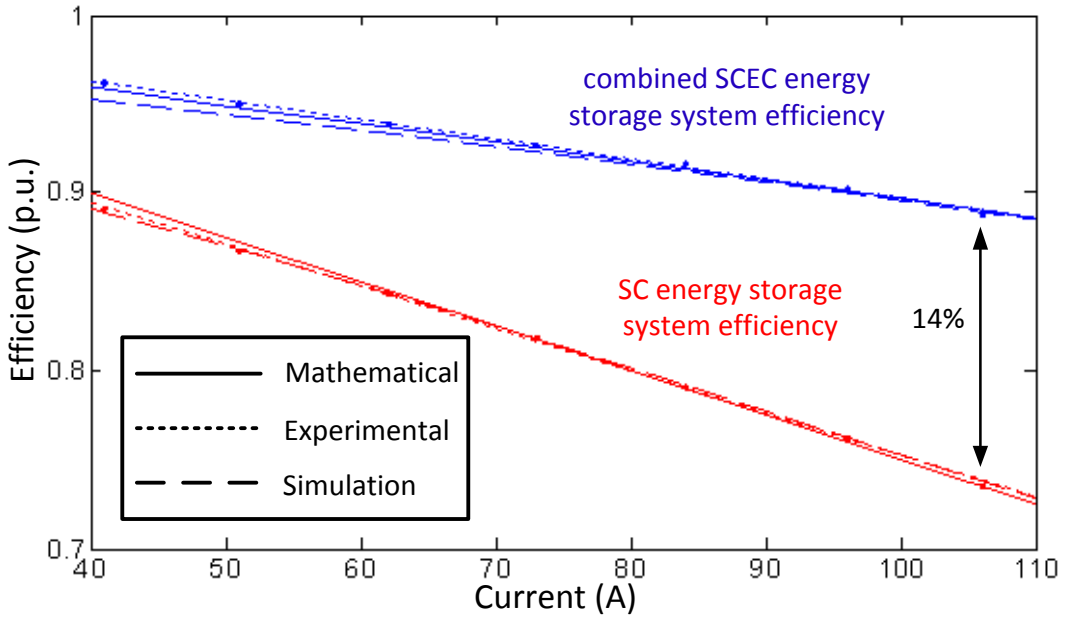

Figure 4.10 Efficiency versus Discharge Current t_d=20ms.

Figure 4.10 compares the systems during a fixed duration discharge of 20ms over the current range 41A ≤ i ≤ 106A, and shows that the efficiency improvement increases as the discharge current increases: here the greatest efficiency improvement is approximately 14% at 106A. Generally, both the SC, and combined SCEC system efficiencies decrease as the discharge current increases.

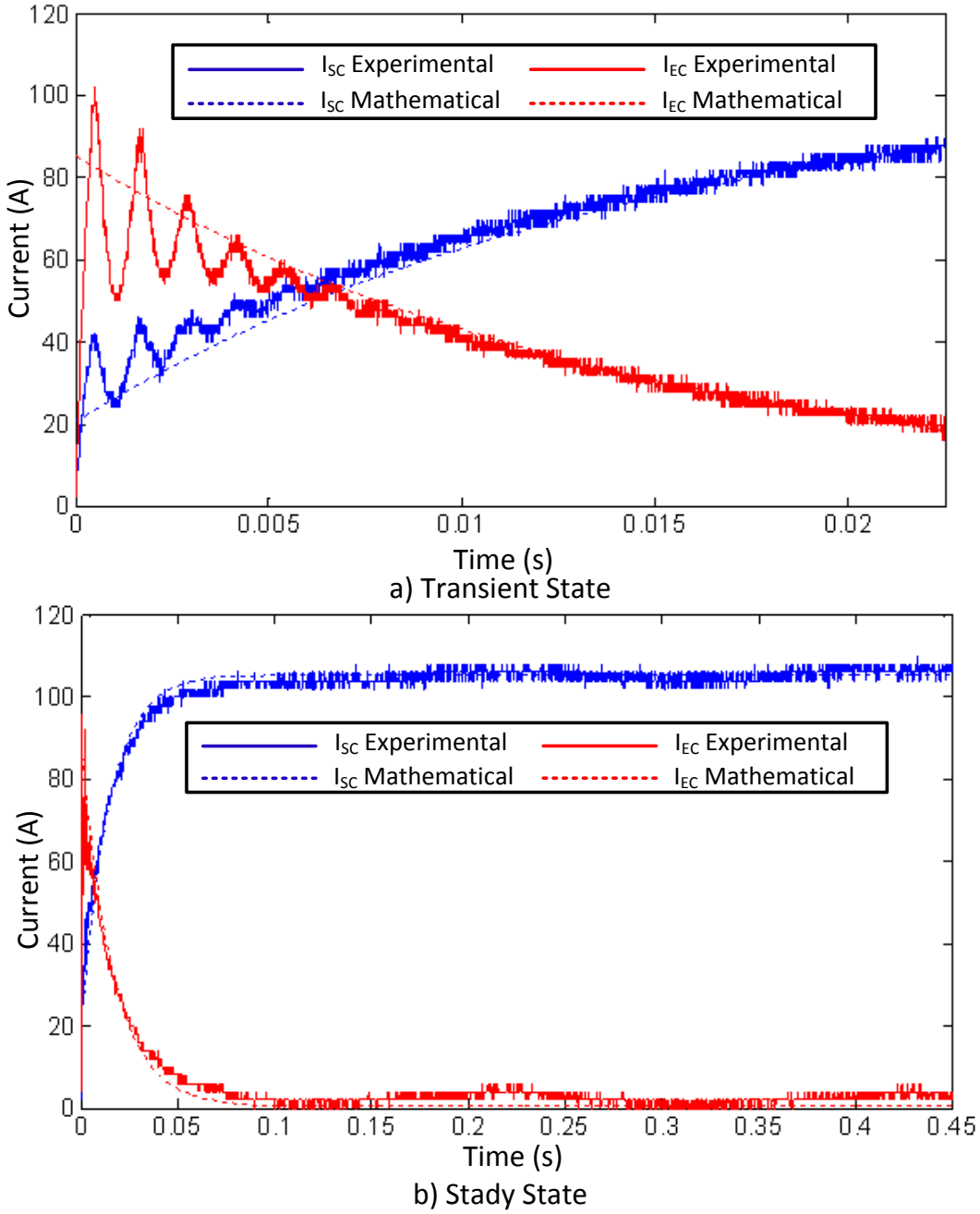

Figure 4.11 The SC and EC Current Sharing Relation at 106A.

Figure 4.11 verifies the current sharing relationship between the output of the SC and the EC. The SCEC system discharges from 10V at 106A, and both the initial and steady-state current data are recorded. At the beginning of the discharge process shown in Figure 4.11 (a), due to its low internal resistance, the majority of the current is drawn from the EC. As the discharge process continuous, the SCEC system reaches steady state as shown in Figure 4.11 (b), where the current is dominated by the SC.

As shown in Figure 4.12, the SCEC system smoothes the initial voltage drop phenomenon seen in the SC system. As both of the systems are discharged at same current level, the SCEC system delivers more power than the SC system, especially for a transient condition. The higher power capability of the SCEC system can potentially improve the response time, compared to the SC system, for applications which require transient peak power. Furthermore, the higher the reference current level, the better the gains from the SCEC energy system.

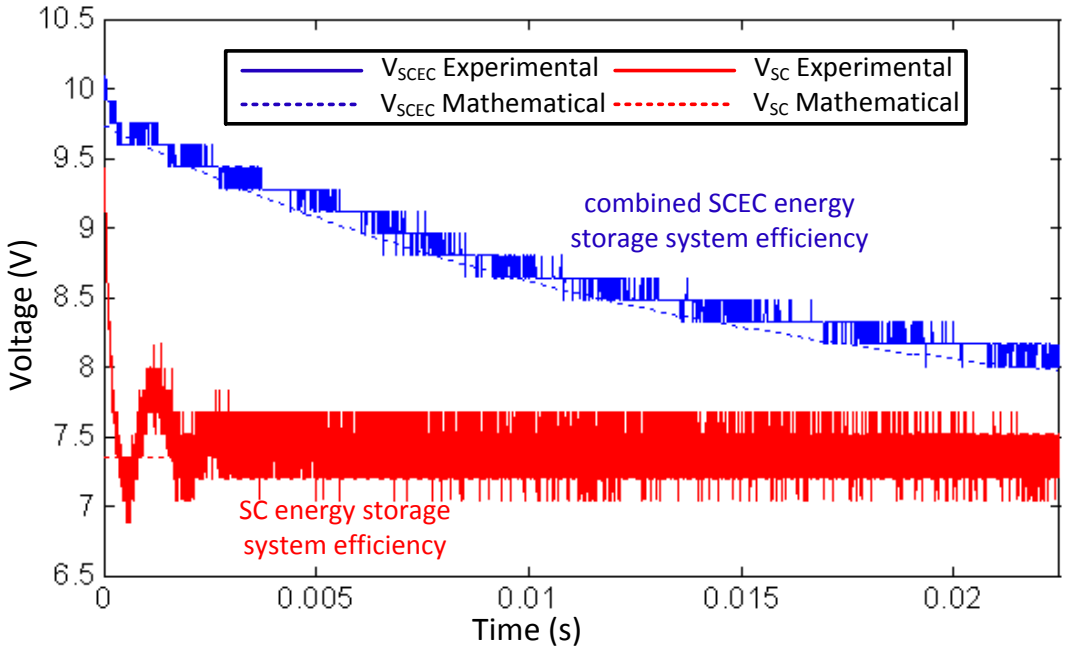

Figure 4.12 Voltage Compare for Discharge from 10V at 106A.

When comparing the simulation and experimental results, when using the simplified capacitor models of Figure 4.4 and Figure 4.5, the error is less than 1.5%. This can

be attributed to the difference between the inrush current and the reference current during experiment start-up, to delays introduced by the PI controller, and to parameter setting errors.

4.2.4 SC and SCEC Energy Storage System Comparison

The study results show that an energy storage system consisting a supercapacitor and an electrolytic capacitor connected in parallel (95.47F) operates more efficiently under conditions of short-duration, high-current discharge, compared to a system incorporating only a supercapacitor (95F).

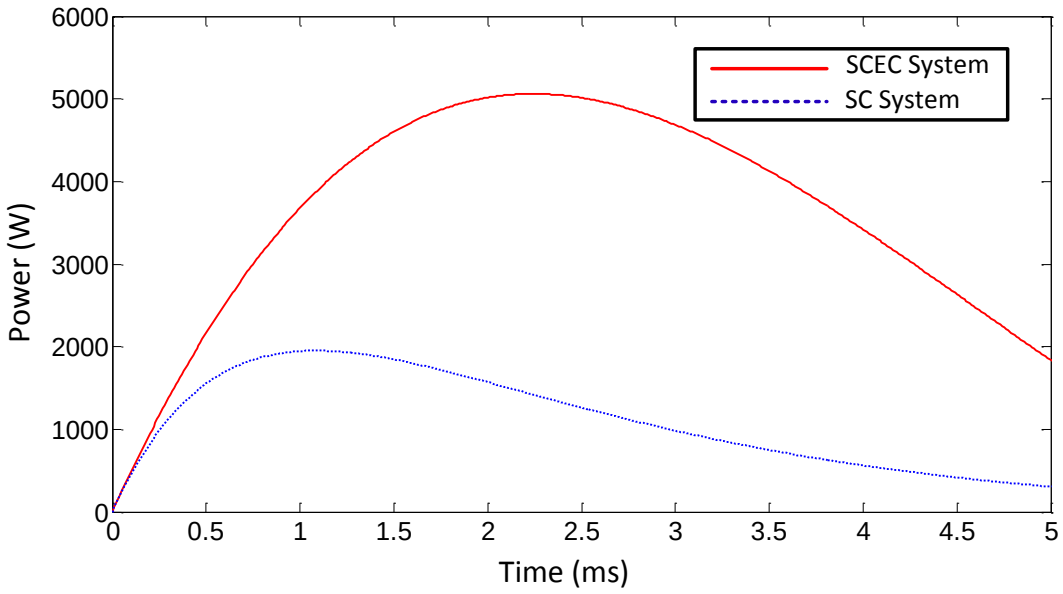

Figure 4.13 Power Capability Comparison.

Also, the combined SCEC energy storage system not only improves efficiency, but also improves peak power capability, compared to the SC based system. The electrolytic capacitor has a lower internal resistance than the supercapacitor which means that, for the same current level, the combined SCEC energy storage system voltage is greater than that of the SC based system, and therefore has higher power ability. For example, when the boost converter switch S1 is on (0.08mΩ), the primary source is discharged by the on-state resistance of the switch via the inductor. The inductance is 20μH with 0.08mΩ switch resistance. Based on the mathematical model, the output power of both energy storage systems are plotted in Figure 4.13. The SCEC provides almost twice the power of the SC system under the same

conditions. As a result, the SCEC system has a faster response time in achieving the required power level, compared to the SC system.

Figure 4.14 shows a three-dimensional plot based on the simplified model for the combined supercapacitor and electrolytic capacitor system, which can be used as an energy storage system design tool. In this example, the plot is based on a 95F supercapacitor with 25mΩ internal resistance, discharged at 100A from 10.8V. The full voltage capability of the supercapacitors (4×2.7V) is exploited. By choosing the desired discharge time and target efficiency, the required electrolytic capacitance can be obtained from Figure 4.14.

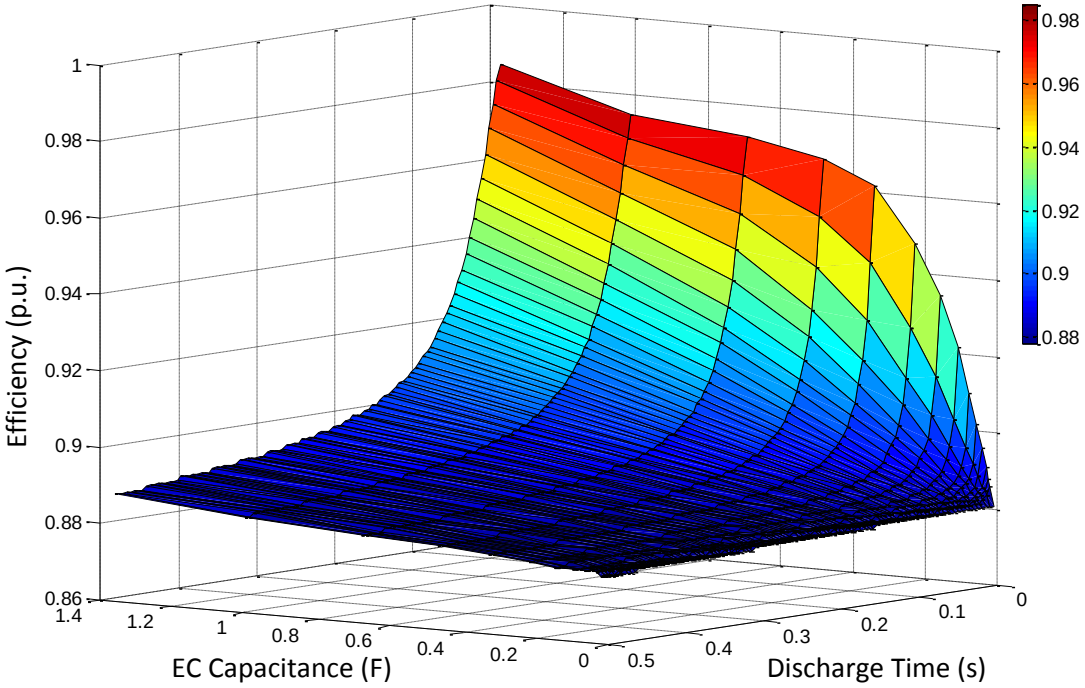

Figure 4.14 Efficiency of the Hybrid System with Variation of the Electrolytic Capacitance and Discharge Time (Supercapacitor: 95F / 25mΩ, Discharge Current: 100A, Initial Capacitor Voltage: 10.8V).

4.3 SCEC Energy Storage System Characteristics

The proposed supercapacitor and electrolytic capacitor energy storage system is an improvement to the supercapacitor based energy storage system, which is more efficient and has a faster response time. Although the SCEC system structure is

simple, with two parallel capacitors, its performance relates to several parameters. The SCEC characteristic analysis is based on the constant current discharge mathematical model and experimental verification is included.

From equations (4.4) to (4.8), the SCEC energy storage system efficiency mathematically depends on several parameters, which are discharge current level, discharge time, initial discharge voltage, and supercapacitor capacitance and resistance, as well as electrolytic capacitor capacitance and resistance. The discharge current, voltage and time are external controllable, while the resistance and capacitance values are determined by the capacitors. The characteristics of the controllable parameters are experimentally verified, the resistance effects are explained mathematically, and capacitance verification is achieved by using a different number of SCs and ECs.

Experimental verification is based on the circuit in Figure 4.8, where the SCEC system current is maintained at a level set by the boost converter. The 4 series BCAP350 with capacitance of 95F and resistance of 25mΩ form the SC part, while the EC is a 0.47F 16V, capacitor with 6mΩ resistance.

According to the system comparison analysis, increased current level and decreased discharge time results in decreased efficiency. As the results shown in Figure 4.9, the greatest difference between the two systems occurs at the beginning of the discharge, and then decreases as the discharge process continuous. The results in Figure 4.10 verify that the difference increases as the current level increases. The following research focuses on the other parameters that affect SCEC system efficiency.

4.3.1 Initial Discharge Voltage

The SCEC system voltage, which refers to the amount of energy in the system, determines its output power. Under constant current condition, the loss on the internal resistor is fixed, while the increased initial discharge voltage results in a higher output power. In such case, the efficiency of the SCEC system can be improved by increasing the initial discharge voltage.

The constant current discharge experiments based on different initial voltage verify the initial discharge voltage effects. The voltage range is between 5.4V, half of the maximum voltage, and 10.8V, the maximum voltage, representing ¾ of the stored energy range. The efficiency is identified at constant discharge currents of 50A for 20ms, where the initial discharge voltage is 5.4V, 6V, 7V, 8V, 9V and 10V.

The experiment results in Figure 4.15 verify the efficiency increase as the initial discharge voltage increases. Compare to the mathematical model, the error percentage is less than 2%. The efficiency decrease rate increases as the initial discharge voltage decreases, while the maximum efficiency occurs at the maximum rated voltage of the SC. Restrained to the 2.7V voltage limit of the SC cell and the voltage dependent energy storage characteristics, best SCEC system efficiency is achieved by operating at a high initial voltage. However, the life time reduces as SC operating voltage increases, which potentially affects system design.

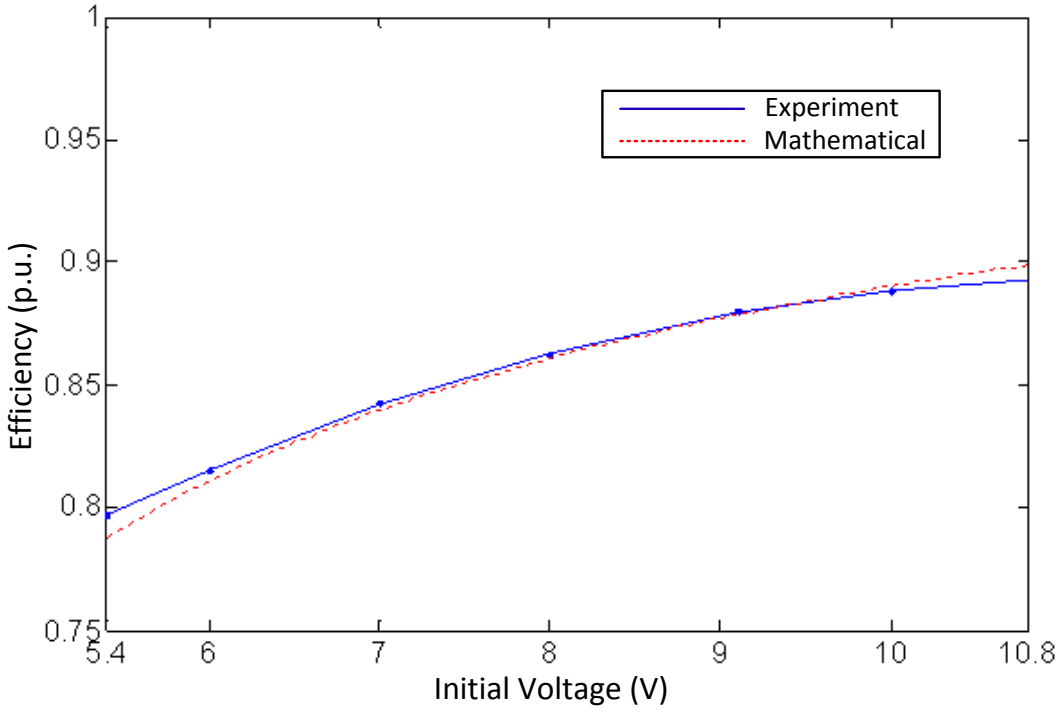

Figure 4.15 Efficiency versus Initial Discharge Voltage.

4.3.2 Supercapacitor Resistance

The SC resistance is the key source of energy loss in the electrical system. According to the mathematical model, minimising the resistance of both the SC and EC can improve the efficiency. However, due to the physical structure, resistance is unavoidable. For commercial products, the resistance is a fixed value. As a result, it is difficult to verify the efficiency increases as resistance decreases. A prediction based on the mathematical model is developed to show the resistance effect on SCEC system efficiency.

The efficiency is calculated based on the six series BCAP350s rated at 15V for the SC part, which has the capacitance of 58.3F and resistance of 19.2mΩ based on the datasheet [4.8]. For the EC part, the maximum resistance is 3mΩ with a capacitance of 0.47F, rated at 16V according to [4.24]. The SCEC system is discharged from 15V, with a 100A constant current. The efficiency is plotted for a percentage of the original resistance, which is 19.2mΩ for the SC and 3mΩ for the EC. Efficiency plots based on different discharge times, 5ms, 10ms and 20ms, are compared to show the effects of the SC and EC resistances.

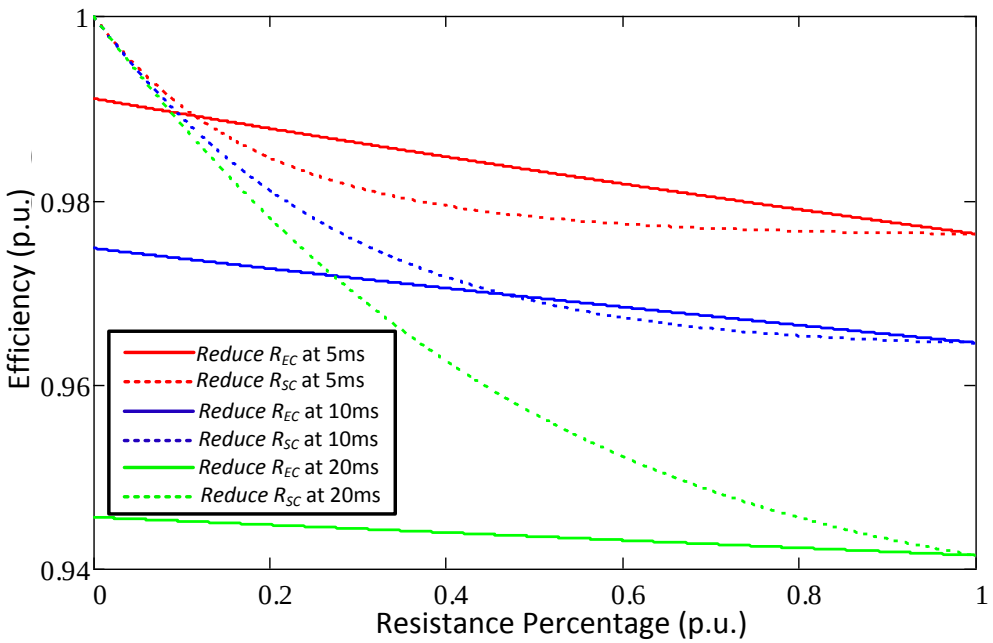

Figure 4.16 SCEC Efficiency versus Reduction of SC or EC Resistance and Different Discharge Time.

From Figure 4.16, the efficiency increases when resistance decreases for both SC and EC. At different discharge times, the resistance effects of the SC and EC are different. For the SC resistance, as it decreases below certain percentage of its original value, a system efficiency better than that of the EC resistance results, with the efficiency tending to 1 as the SC resistance decreases to 0. However, for a transient discharge condition, EC resistance reduction gives a more obvious improvement above a certain value.

It is assumed that in the future SC and EC resistance values can be reduced, but minimally. According to mathematical prediction, it is more efficient to decrease the EC resistance for transient applications. However, for long-duration applications, reduction of SC resistance is more significant.

4.3.3 Parallel Effects

Parallel connection of capacitors results in higher capacitance and lower resistance. For SC commercial products, the capacitor rated voltage is fixed at 2.7V, while the capacitance, resistance, and current limits are variables. Table 4.3 summarises parameters of the Maxwell K2 series ultracapacitor, where the value in the bracket is the per unit value based on the parameters of the BCAP3000.

Table 4.3 Summary of Maxwell K2 Series Product Parameters

	Capacitance (F)	ESR (mΩ)	Maximum Continuous Current (A)	Time Constant (s)	Volume ($\times 10^6 mm^3$)
BCAP3000	3000 (1p.u.)	0.29 (1p.u.)	210 (1p.u.)	0.87 (1p.u.)	0.403 (1p.u.)
BCAP2000	2000 (0.667p.u.)	0.35 (1.21p.u.)	170 (0.810p.u.)	0.7 (0.805p.u.)	0.298 (0.739p.u.)
BCAP1500	1500 (0.5p.u.)	0.47 (1.62p.u.)	140 (0.667p.u.)	0.705 (0.81p.u.)	0.248 (0.615p.u.)
BCAP1200	1200 (0.4p.u.)	0.58 (2p.u.)	110 (0.524p.u.)	0.696 (0.8p.u.)	0.216 (0.536p.u.)
BCAP0650	650 (0.217p.u.)	0.8 (2.76p.u.)	88 (0.419p.u.)	0.52 (0.598p.u.)	0.150 (0.372p.u.)

In order to show paralleling effects, low capacitance SCs are paralleled to achieve the capacitance of 3000F. Due to capacitance difference, parallel integral numbers of SCs cannot achieve 3000F, so a parallel factor is assumed to mathematically compare the paralleling.

Table 4.4 Capacitance Scale Parallel Effects

	Parallel Factor	p.u. Capacitance (F)	ESR (mΩ)	Maximum Continuous Current (A)	Time Constant (s)	Volume ($\times 10^6 mm^3$)
BCAP 3000	1	3000	0.29 (1p.u.)	210 (1p.u.)	0.87 (1p.u.)	0.403 (1p.u.)
BCAP 2000	1.5	3000	0.233 (0.803p.u.)	255 (1.214p.u.)	0.7 (0.805p.u.)	0.447 (1.109p.u.)
BCAP 1500	2	3000	0.235 (0.810p.u.)	280 (1.330p.u.)	0.705 (0.81p.u.)	0.496 (1.231p.u.)
BCAP 1200	2.5	3000	0.232 (0.8p.u.)	275 (1.310p.u.)	0.696 (0.8p.u.)	0.54 (1.340p.u.)
BCAP 0650	4.62	3000	0.173 (0.597p.u.)	406.56 (1.936p.u.)	0.52 (0.598p.u.)	0.693 (1.720p.u.)

The results in Table 4.4 show that paralleling of low capacitance SCs has no effect on the time constant. The ESR and maximum continuous current are improved, which is mainly due to the increased volume. Comparison of parallel connected SCs based on the same volume is shown in Table 4.5.

Table 4.5 shows capacitance of parallel SCs does not achieve 3000F for the same volume, while the ESR and maximum continuous current are about the same at same volume condition. It can be concluded that, for a specified volume, parallel connection of high capacitance SCs provides higher capacitance than that of the low capacitance SCs with a similar resistance and current level.

Table 4.5 Volume Scale Parallel Effects

	Parallel Factor	Capacitance (F)	ESR (mΩ)	Maximum Continuous Current (A)	Time Constant (s)	p.u. Volume ($\times 10^6 mm^3$)
BCAP 3000	1	3000 (1p.u.)	0.29 (1p.u.)	210 (1p.u.)	0.87 (1p.u.)	0.403
BCAP 2000	1.352	2704.7 (0.902p.u.)	0.259 (0.893p.u.)	229.84 (1.094p.u.)	0.7 (0.805p.u.)	0.403
BCAP 1500	1.625	2437.5 (0.813p.u.)	0.289 (0.997p.u.)	227.5 (1.083p.u.)	0.705 (0.81p.u.)	0.403
BCAP 1200	1.866	2239.2 (0.746p.u.)	0.311 (1.072p.u.)	205.26 (0.977p.u.)	0.696 (0.8p.u.)	0.403
BCAP 0650	2.687	1746.55 (0.582p.u.)	0.2977 (1.027p.u.)	236.456 (1.126p.u.)	0.52 (0.598p.u.)	0.403

4.3.4 Capacitance Effects

According to the mathematical model, capacitance mainly affects the steady state current sharing relationship between the SC and EC, where the higher capacitance draws more current from the SCEC system. Similar to resistance effects, the capacitance is fixed for a given commercial product. The analysis of capacitance effects focuses on the effects of employing a different number of SCs and ECs in the SCEC energy storage system.

The ratio of SC and EC, denoted as K_C, is defined as the SC capacitance divided by EC capacitance. The experimental validation is based on four BCAP350s and two ECs with 0.47F, which allows three SCEC combinations.

$K_C = 101$, four series SCs in parallel with 2 parallel ECs;

$K_C = 202$, four series SCs in parallel with one EC; and

$K_C = 404$, two series SCs in parallel with one EC.

The SCEC system is discharged at a constant 50A, and the initial voltage depends on the maximum rated voltage of the SC part, which is 2.5V per cell in parallel. The efficiency is recorded at the discharge time of 20ms.

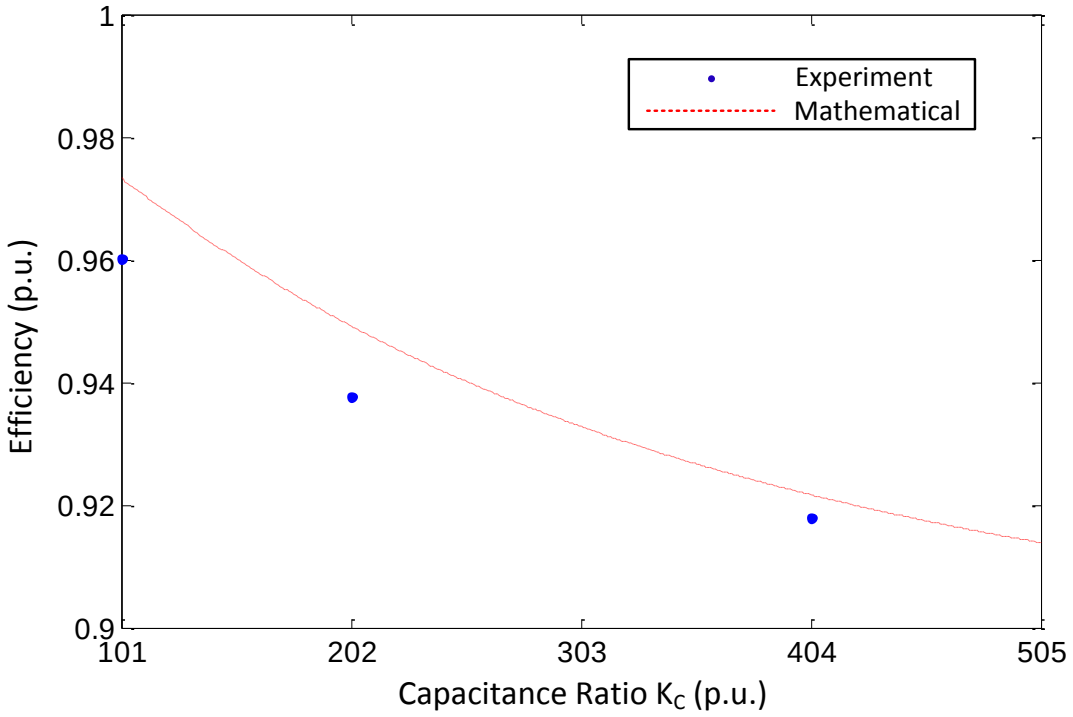

Figure 4.17 Efficiency versus Capacitance Ratio K_C.

The result in Figure 4.17 shows that the system efficiency decreases as the capacitance ratio K_C increases, which means lower SC capacitance or higher EC capacitance improves the efficiency. Also at a given capacitance ratio, the efficiencies of the different SCEC combinations are identical, according to the mathematical model. An efficiency prediction of the SCEC system, where the SC part is the four series BCAP350s while the EC parallel number is incrementally increased, is developed based on the mathematical model. The system is discharged from 10V with a 100A constant current, and the efficiency is recorded at 20ms.

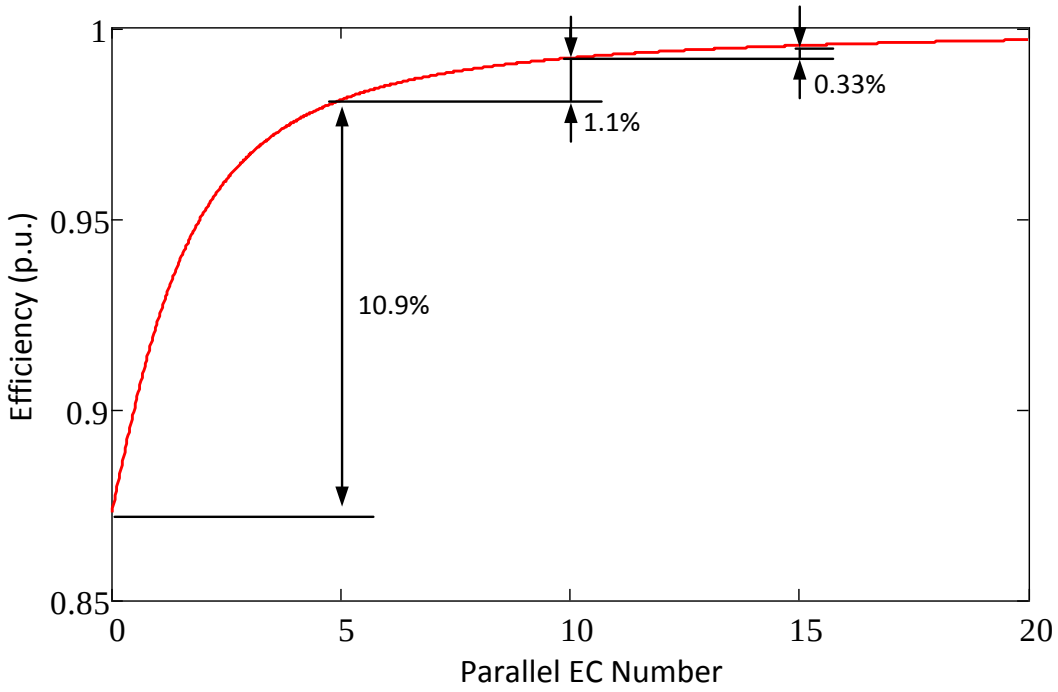

Figure 4.18 Efficiency versus Parallel EC Number

Figure 4.18 shows that efficiency increases as the parallel EC number increases, however the increase rate decreases dramatically as the number increases. For the first five ECs in parallel, the efficiency is increased by 10.9%, while adding a second five ECs, the improvement is only 1.1%. When the EC number increases to fifteen, the efficiency is only increased by 0.33%, compared to ten ECs. Considering costs, it is necessary to assess the parallel EC number and its improvement in the system efficiency, to achieve an optimal solution.

Although the characteristic analysis of the SCEC system is developed based on the discharging process, similar characteristics hold during the charging process, as the developed mathematical model is valid for both processes. As introduced in Chapter 2, the difference between the charging and discharging process is the boundary condition, which is described by the mathematical model. During the charging process, the SC efficiency (with the addition of paralleled connected EC) can be improved in the same way as it is for the discharging process.

Theoretically, higher capacitance and lower internal resistance provides better efficiency, which is a general rule for choosing a capacitor. The SCEC system efficiency can be improved by the following method: decrease discharge current, decrease discharge time, decrease SC and EC resistance, increase initial discharge voltage, and decrease the capacitance ratio. As a result, it is important to consider these multiple effects on the system efficiency and develop a design process for a practical SCEC system.

4.4 SCEC Energy Storage System Design

According to the characteristic analysis, SCEC system efficiency depends on several parameters, which can be divided into internal structure parameters and external controllable parameters. The internal structure parameters, including capacitance, resistance and rated voltage, are fixed for given SC and EC single cells. The external controllable parameters, including discharge current, time and voltage range, are controllable, but have to be within the SC and EC product electrical and thermal limits. As a result, series and parallel connections are required to satisfy practical application requirements.

4.4.1 General Design Guide for SCEC System

This design guide aims to develop a general method for determining the necessary number of series and parallel connected SCs and ECs. For an energy storage system, especially for applications requires transient high power capability, the combined SCEC system provides better performance in efficiency, volume and cost than a purely SC system. Based on the application requirement, a 3D plot allows determination of a suitable number of SC, based on the efficiency with a different number of EC, at different discharge currents and times.

The design guide is developed based on practical applications that employ the SCEC system as an energy storage device. The detailed design process is as follows:

1. Specify application requirement.

As the SCEC system operates as an energy storage device, the requirement of the practical application is essential to design process. The required energy E_{req}, which

defines the total energy required for the system under normal conditions, is used for identifying the SC capacitance part. The rated voltage and current at the normal working condition V_{rated} and I_{rated}, are identified for the converter design, while the transient peak current I_{peak} and transient peak duration t_{peak} are used for the EC part component identification.

2. Specify the dc-dc converter requirement.

Since the capacitor voltage decreased as the energy stored in the capacitor decreases, a dc-dc converter is required to control the energy flow and output voltage of the system. Based on the application requirement, the converter output needs to satisfy the normal working condition requirement and be able to tolerate the transient peak condition. The converter maximum and minimum input voltages $V_{convertermax}$ and $V_{convertermin}$ are required to determine the SC number.

3. Specify discharge ratio of SC under normal working condition.

As the higher discharge voltage improves the system efficiency, it is better to discharge the SCEC system at its upper voltage range. The discharge ratio d_{SC} defines the minimum voltage of the SCEC system, and is determined by the converter input.

$$d_{SC} = \frac{V_{convertermin}}{V_{convertermax}} \tag{4.11}$$

As the SC is normally discharged to 50% of its rated voltage, the converter is developed to meet the minimum input voltage requirement.

4. Specify SC number.

Based on the discharge ratio, the usable energy for a SC single cell is:

$$E_{SCcell} = \frac{1}{2} \cdot C_{SCcell} \cdot {V_{SCcell}}^2 \cdot \left(1 - {d_{SC}}^2\right)$$

where E_{SCcell}, C_{SCcell} *and* V_{SCcell} *are useable energy, capacitance and rated voltage for single cell of SC* **(4.12)**

According to the application required energy, the total required SC number can be approximated as:

$$N_{SC} = \frac{E_{req}}{E_{SCcell}} \tag{4.13}$$

5. Determine series and parallel number of supercapacitors.

The number of series SCs determines the maximum voltage of the SCEC system, where the series SC number is determined by the maximum converter input voltage as:

$$N_{SCs} = \frac{V_{convertermax}}{V_{C0}} \tag{4.14}$$

The parallel number of the series SC strings is identified by comparing the series SC number and the total required SC number and the rated current at normal conditions. Two assumed parallel numbers are calculated based on the energy and current requirement, which are:

$$N_{SCp1} = \frac{N_{SC}}{N_{SCs}} \tag{4.15}$$

$$N_{SCp2} = \frac{I_{rated}}{I_{SCcell}} \tag{4.16}$$

The larger of N_{SCp1} and N_{SCp2} is selected as the parallel number $N_{SCp}$to satisfy both energy and current requirements. The series and parallel number decision flow chart is shown in Figure 4.19.

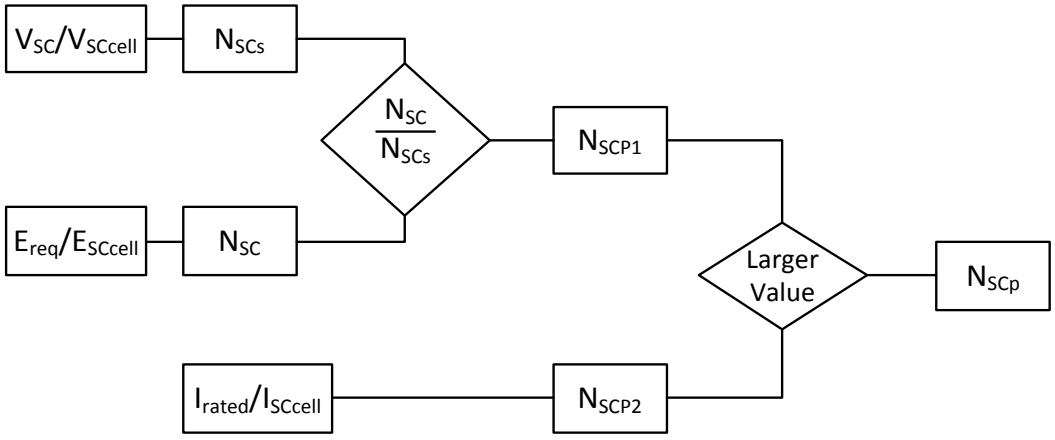

Figure 4.19 Series and Parallel Number Decision Flow Chart.

6. Define total supercapacitor capacitance and resistance.

The total SC capacitance is

$$C_{SC} = \frac{N_{SCp}}{N_{SCs}} \cdot C_{SCcell} \quad \textbf{(4.17)}$$

The total SC resistance is

$$R_{SC} = \frac{N_{SCs}}{N_{SCp}} \cdot R_{SCcell} \quad \textbf{(4.18)}$$

7. Determine EC number based on efficiency plot at transient peak current conditions.

Typically, the single cell electrolytic capacitor is selected based on larger capacitance and lower resistance at a rated voltage $V_{convertermax}$. Based on the single cell parameter, the efficiency improvement is shown on the plot with respect to the number of parallel electrolytic capacitors. The EC number is determined by the application type, which requires a specified efficiency or better volume and cost performance.

As introduced in the design guide, the series number is determined by the load maximum voltage, where parallel of series SC strings is required to satisfy the energy or current requirement of the application. However, due to the low SC single cell voltage limitation, the series number is quite large. Thus, for transient conditions, which require high power or current in a short duration (<1s), it is inefficient in volume and cost to parallel extra SC strings. The EC, which is able to provide higher power and efficiency in the short duration range with much better volume and cost performance, is selected to improve the SC energy storage system. Followed by the design process, the SC number is identified based on normal condition requirements, while the EC number is determined by the transient condition requirements.

4.4.2 500V SCEC System Design

Based on the general design guide, an example of SCEC system design is developed for an energy storage device in wind generation, which is connected to the dc link for smoothing dc ripple and enhancing transient low voltage ride through capability.

The dc link voltage is 500V, while during normal conditions, the energy storage system is used to smooth the power flow, which is able to sink or source 50kW for 20s, that is, 1MJ of energy exchange. During the fault ride through condition, the system supplies 3000A for 20ms.

1. Specify application requirement.

For the operating conditions introduced, the application requirements are summarised in Table 4.6.

Table 4.6 Summary of Application Requirement

E_{req}	1MJ	P_{rated}	50kW
V_{rated}	500V	I_{peak}	3000A
I_{rated}	180A	t_{peak}	20ms

2. Specify the dc-dc converter requirement.

As the dc link voltage is 500V, for a Boost converter, the maximum and minimum converter input voltage $V_{convertermax}$ and $V_{convertermin}$ are 500V and 250V, which gives the SCEC system charge and discharge within the converter range. According to the transient requirement, the converter has to be able to tolerate the peak current.

3. Specify discharge ratio of the SC under normal working conditions.

From the converter specification, the discharge ratio d_{SC} is calculated based on equation (4.11), which is ½.

4. Specify SC number.

The BCAP3000 is selected as the single SC cell, and has rated cell voltage V_{SCcell} of 2.5V, cell capacitance C_{SCcell} of 3000F, and cell resistance R_{SCcell} of 0.29mΩ. The usable cell energy E_{SCcell} is 7031J according to equation (4.12). Based on equation (4.13), the total SC number N_{SC} is calculated as 143.

5. Determine series and parallel numbers of supercapacitors.

The series number of SC N_{SCs} is determined by the 500V maximum converter input voltage, which is 200 for a single cell rated voltage of 2.5V. According to equations (4.15) and (4.16), a single SC strings is able to satisfy the energy and current requirement. Thus the parallel number N_{SCp} is 1.

6. Define total supercapacitor capacitance and resistance.

The total capacitance and resistance of the SC part is calculated based on equations (4.17) and (4.18), giving 15F and 58mΩ. For the SC part, constant power discharge at rated conditions, 50kW for 20s, the voltage drops from 500V to 329V, and the maximum current is 152A. Based on theoretical estimation, the developed SC part is capable of supporting the defined normal conditions.

7. Determine EC number based on the efficiency plot at transient peak current conditions.

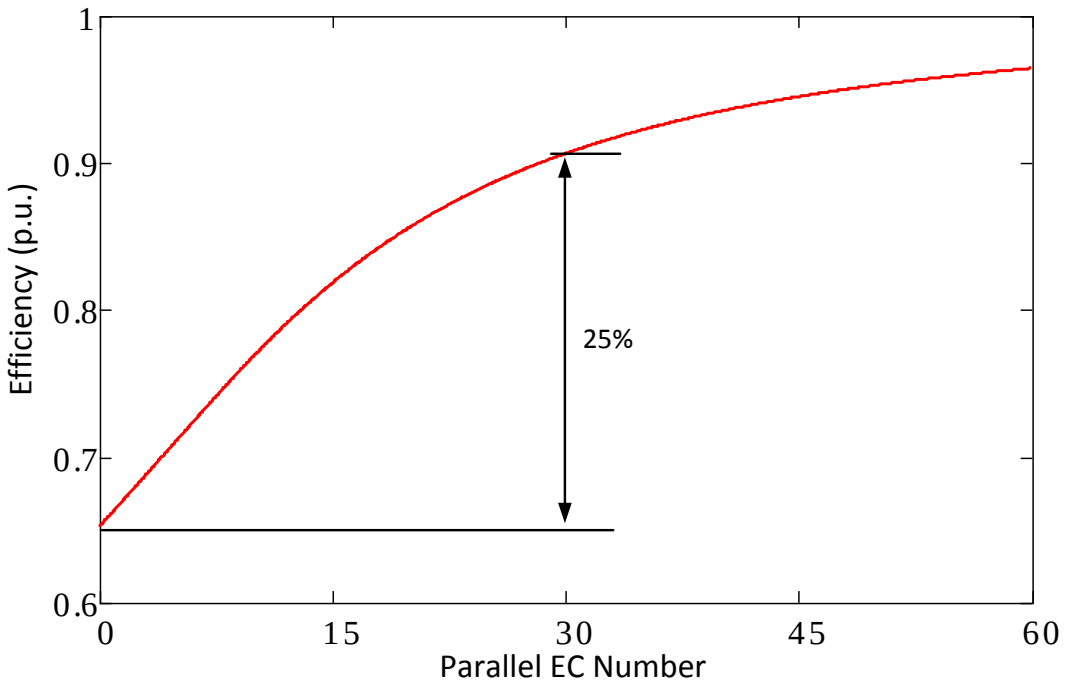

Figure 4.20 Efficiency versus Parallel EC Number for 500V SCEC System Design.

Based on the developed SC part, an electrolytic capacitor, rated at 500V with 8400μF capacitance and 14.3mΩ, is chosen as the parallel EC element. Considering the volume of the system, the developed SC part is $80.6\times10^{6}mm^{3}$, while the EC cell volume is $1.36\times10^{6}mm^{3}$. For same volume of SCs and ECs, the EC parallel number can theoretically be sixty. The efficiency plot for the SCEC system at 3000A for 20ms, with respect to the parallel EC number is shown in Figure 4.20. The efficiency increases by 25% for thirty parallel EC, which has half the volume of the SC part.

With a 2200A BCAP3000 peak current limit, if the energy storage system is based solely on the SC, due to the 3kA transient current requirement, an extra SC string of two hundred BCAP3000s has to be connected in parallel. In such a case, the volume is increased to $160.12\times10^{6}mm^{3}$, and the extra energy provided from the parallel SC string exceeds twice the normal condition requirement, which is inefficient in terms of volume and cost. For the thirty parallel EC with the SC bank, under peak conditions, the average currents from the EC and SC banks are 1640A and 1360A, which the system can tolerant. In addition, the SCEC system power is 14% higher than that of the SC system, at the transient peak current condition. As established, the developed EC part is capable of fulfilling the peak requirement with a better volume and cost performance, which optimises the energy storage system for the required power application.

4.5 SCEC Energy Storage System Frequency Analysis

The SCEC system frequency analysis aims to provide a mathematical model for analysing the current relationship between the SC and EC part, under ac conditions. The SC is ideal for energy storage in dc applications. For ac applications, the cycle life of the SC limits its applications at medium and high frequency. Based on the frequency analysis, the developed SCEC system is able to separate the ac and dc components, where the SC part supports the dc current, while the ac component is filtered by the EC part.

4.5.1 Two Branch Frequency Analysis

From the time domain mathematical model in Figure 4.5, the associated complex domain model is developed by taking the Laplace transform for frequency analysis. As shown in Figure 4.21, the constant current source is replaced by a general current source $I_{out}(s)$.

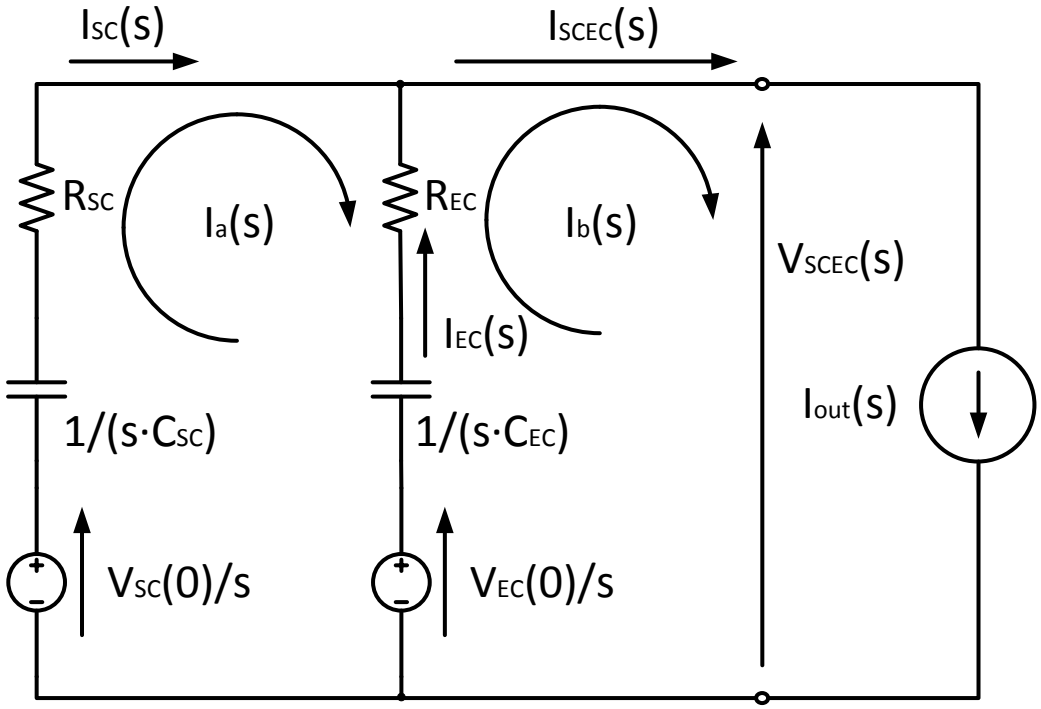

Figure 4.21 SCEC Constant Current Discharge Equivalent Circuits in s Domain.

By KVL, the following equations solve the SC and EC currents:

$$\begin{cases} \left(R_{SC}+\dfrac{1}{s\cdot C_{SC}}+R_{SC}+\dfrac{1}{s\cdot C_{EC}}\right)\cdot I_a(s)-\left(R_2+\dfrac{1}{s\cdot C_{EC}}\right)\cdot I_b(s)=\dfrac{V_{SC}(0)-V_{EC}(0)}{s} \\ -\left(R_{EC}+\dfrac{1}{s\cdot C_{EC}}\right)\cdot I_a(s)+\left(R_{EC}+\dfrac{1}{s\cdot C_{EC}}\right)\cdot I_b(s)=\dfrac{V_{EC}(0)}{s}-V_{SCEC}(s) \\ I_b(s)=I_{out}(s) \end{cases}$$

Assuming the initial voltages of SC and EC parts are equal, the first branch $I_a(s)$ is calculated as:

$$I_a(s) = \frac{\left(R_{EC} \cdot s + \frac{1}{C_{EC}}\right)}{(R_{SC} + R_{EC}) \cdot s + \left(\frac{1}{C_{SC}} + \frac{1}{C_{EC}}\right)} \cdot I_{out}(s) \quad \textbf{(4.19)}$$

By replacing s with $2\pi \cdot f \cdot i$, the frequency response of SC output current is:

$$I_{SC}(f) = I_a(f) = \frac{2\pi \cdot f \cdot i \cdot R_{EC} + \frac{1}{C_{EC}}}{(R_{SC} + R_{EC}) \cdot (2\pi \cdot f \cdot i) + \left(\frac{1}{C_{SC}} + \frac{1}{C_{EC}}\right)} \cdot I_{out}(2\pi \cdot f \cdot i) \quad \textbf{(4.20)}$$

The frequency response of EC output current is:

$$I_{EC}(f) = \left[1 - \frac{2\pi \cdot f \cdot i \cdot R_{EC} + \frac{1}{C_{EC}}}{(R_{SC} + R_{EC}) \cdot (2\pi \cdot f \cdot i) + \left(\frac{1}{C_{SC}} + \frac{1}{C_{EC}}\right)}\right] \cdot I_{out}(2\pi \cdot f \cdot i) \quad \textbf{(4.21)}$$

The current magnitude gain of I_{EC} normalised by I_{SC}:

$$Gain_{EC}(f) = \frac{|I_{EC}(f)|}{|I_{SC}(f)|} = \frac{\sqrt{(C_{EC})^2 + (2\pi \cdot C_{SC} \cdot C_{EC} \cdot R_{SC} \cdot f)^2}}{\sqrt{(C_{SC})^2 + (2\pi \cdot C_{SC} \cdot C_{EC} \cdot R_{EC} \cdot f)^2}} \quad \textbf{(4.22)}$$

The maximum current gain of I_{EC} normalised by I_{SC} is:

$$Gain_{ECMAX}(f) = \lim_{f \to \infty} Gain_{EC}(f) = \frac{R_{SC}}{R_{EC}} \quad \textbf{(4.23)}$$

The cutoff frequency of $Gain_{EC}$, which is defined as the frequency when $Gain_{EC}(f) = \frac{1}{\sqrt{2}} Gain_{ECMAX}(f)$:

$$f_{cutoffEC} = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{(C_{EC} \cdot R_{EC})^2} - \frac{2}{(C_{SC} \cdot R_{SC})^2}} = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{(\tau_{EC})^2} - \frac{2}{(\tau_{SC})^2}} \quad \textbf{(4.24)}$$

As equation (4.22) established, the current sharing relationship in frequency domain of the SCEC system is independent of the current wave type. The maximum magnitude gain is determined by the resistance of the EC and SC. Figure 4.22 shows the EC current gain frequency response with SC parameter values of 95F and 25mΩ and EC parameter values of 0.47F and 6mΩ.

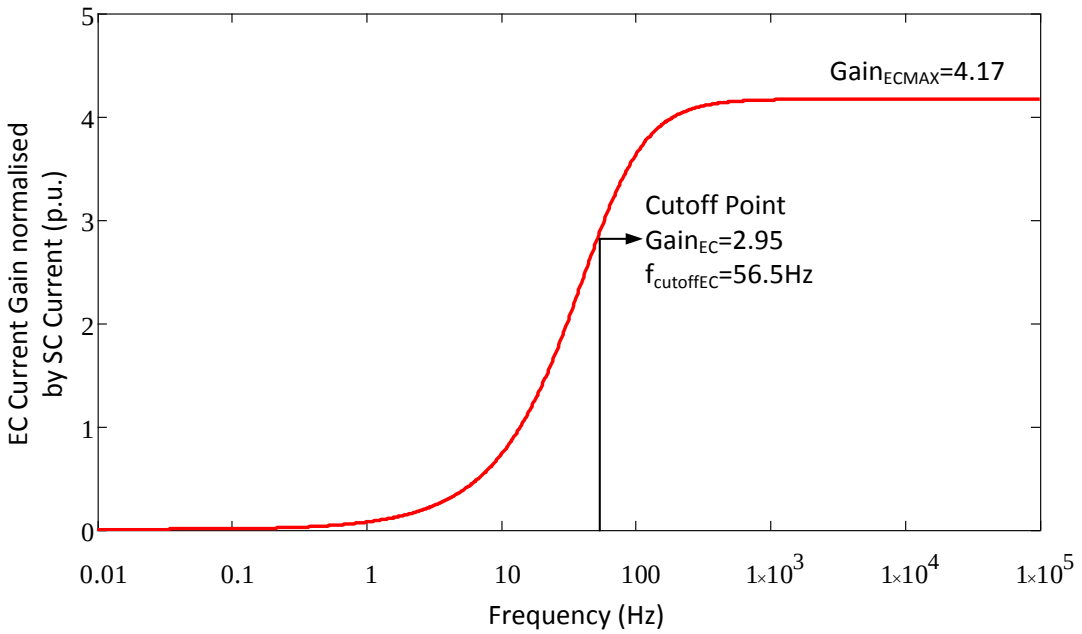

Figure 4.22 EC Current Gain Frequency Response.

An SCEC system ac current discharge model, based on the SC and EC parameter values associated with Figure 4.22, is developed in simulation to verify the mathematical model of the EC current gain frequency response. The SCEC system is discharged by a sine wave current source, I_{SCEC}, which has an offset current of 60A with a 30A ripple. Two frequencies, 2.1kHz and 56.5Hz, are selected to verify the ac current sharing relationship.

The results in Figure 4.23 show the EC gain of the ac component confirms the mathematical model calculation results. In Figure 4.23 (a), with a discharge current frequency of 2.1kHz, the SC carries 59.7A offset current with a ripple of 5.8A, while the EC has an offset current of 0.3A with 24.19A ripple at steady state. The EC current magnitude gain is calculated as 4.17, which is identical to the result shown in

Figure 4.22. In Figure 4.23 (b), the discharge current operates at the 56.5Hz cutoff frequency. At steady state, the SC carries 59.7A offset current with 8.05A ripple, while the EC has an offset 0.3A with the ripple is 23.73A, which gives an EC gain of 2.94.

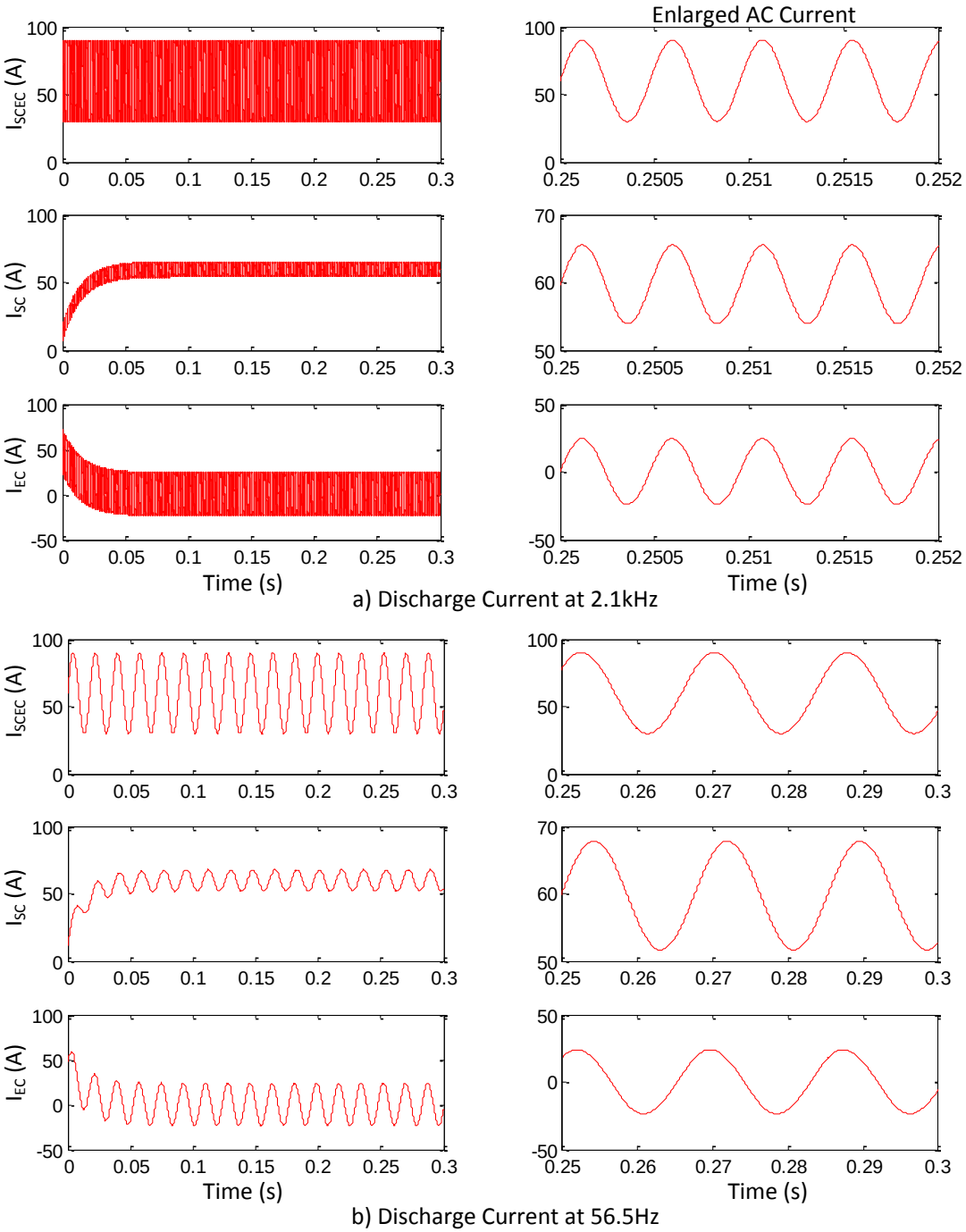

Figure 4.23 SCEC AC Discharge Current Relation Simulation Results.

Based on both the time and frequency domain analyses of the SCEC system, analysis is able to mathematically predict the current share relationship between the SC and the EC. During the design process, the developed model helps determine the number of SC and EC to meet either the dc or ac requirements.

4.5.2 Extended Three Branch Frequency Analysis

The two branch RC s-domain circuit previously introduced is suitable for medium and low frequency analysis. For high frequency analysis, the model lacks inductive effects. The extended three branch model, which has three different types of capacitors in parallel, is developed with series inductive components to provide full frequency range analysis. The third RC branch represents a polypropylene capacitor (PPC), which can have a time constant of less than a microsecond. Normally, the polypropylene capacitor is connected in parallel with the electrolytic capacitor to protect the EC from high ripple current. As the capacitance of the PPC is much smaller than that of the EC and the SC, the current fall time of the PPC in transient condition is extremely short, while the shared dc current in steady-state is small enough to be ignored. As a result, the effect of the PPC is insignificant in the dc time domain analysis. However, due to its low series resistance, its current gain is much larger than the EC at high frequency. The developed three branch model aims to analyse the effect of the parallel PPC in ac current conditions.

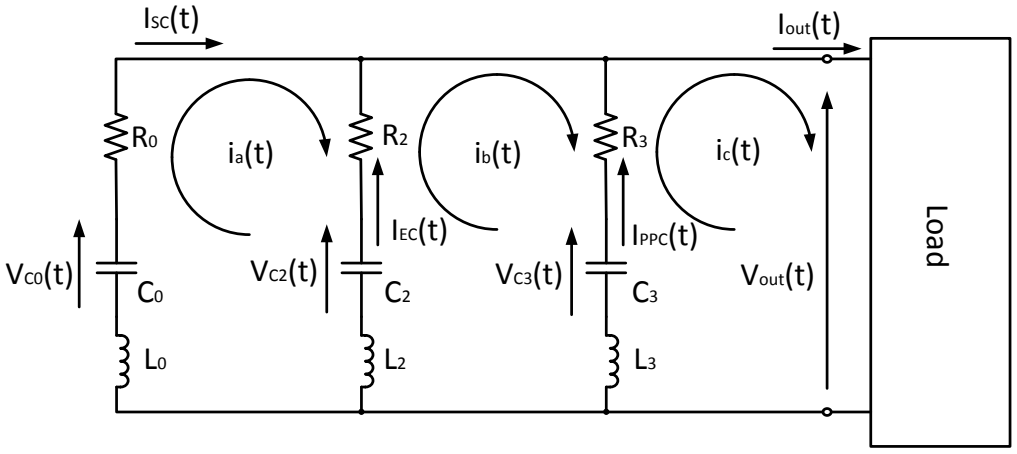

Figure 4.24 Three RC Branches Time Domain Circuit.

The time domain three branch circuit is modelled as three RC branches parallel connected to a general load with output voltage V_{out}(t) and current I_{out}(t) , where C_0 and R_0 represents the SC, C_2 and R_2 represents the EC and C_3 and R_3 represents the PPC, while each branch has a series inductor L for high frequency analysis.

The following assumptions are made when developing the mathematical model, where the initial current of each branch is assumed zero, and the initial voltage of all capacitors is equal. An approach similar to that use with Figure 4.21 is applied to identify the frequency response, where the operational circuit is developed by taking the Laplace transform for Figure 4.24.

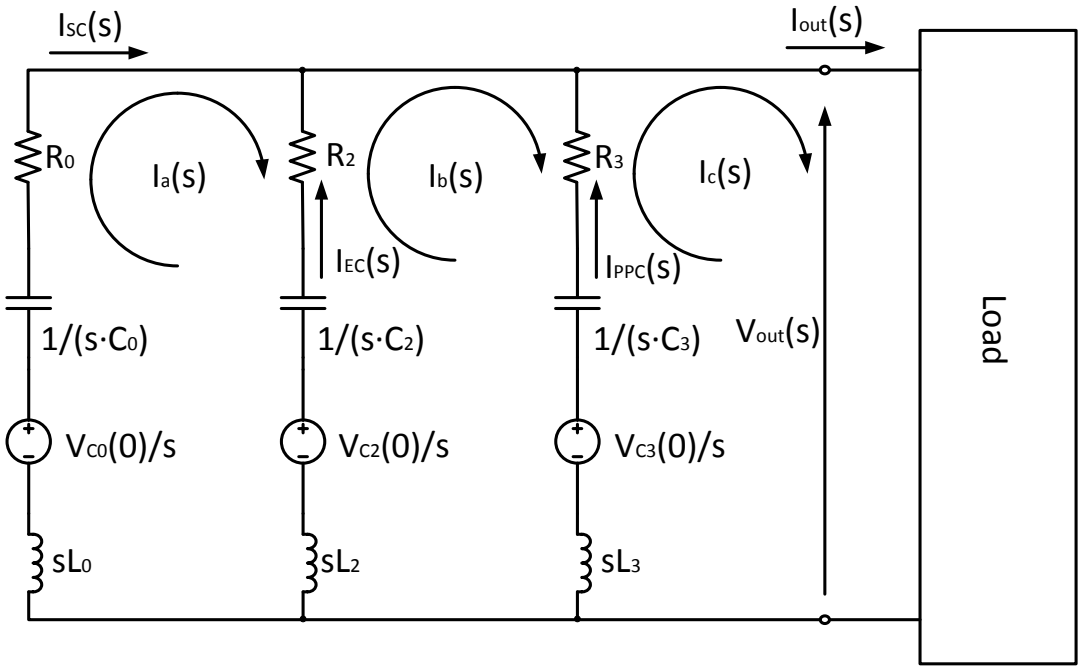

Figure 4.25 Three Branch Constant s domain Circuit.

Assuming $Z_0(s) = R_0 + \frac{1}{s \cdot C_0} + s \cdot L_0$, $Z_2(s) = R_2 + \frac{1}{s \cdot C_2} + s \cdot L_2$ and $Z_3(s) = R_3 + \frac{1}{s \cdot C_3} + s \cdot L_3$, the following equations are developed based on KVL:

$$\begin{cases} (Z_0(s) + Z_2(s)) \cdot I_a(s) - Z_2(s) \cdot I_b(s) = \dfrac{V_{c0}(0) - V_{c2}(0)}{s} \\ -Z_2(s) \cdot I_a(s) + (Z_2(S) + Z_3(s)) \cdot I_b(s) - Z_3(s) \cdot I_c(s) = \dfrac{V_{c2}(0) - V_{c3}(0)}{s} \\ -Z_3(s) \cdot I_b(s) + Z_3(s) \cdot I_c(s) = \dfrac{V_{c3}}{s} - V_{out}(s) \\ I_c(s) = I_{out}(s) \end{cases}$$

By solving the previous equations, the current $I_a(s)$ can be expressed as:

$$I_a(s) = \frac{A1 \cdot s^4 + B1 \cdot s^3 + C1 \cdot s^2 + D1 \cdot s + E1}{F1 \cdot s^5 + G1 \cdot s^4 + H1 \cdot s^3 + I1 \cdot s^2 + J1 \cdot s} \quad \textbf{(4.25)}$$

where

$$A1 = s \cdot I_{out}(s) \cdot C_0 \cdot L_2 \cdot L_3 \cdot C_3$$

$$B1 = s \cdot I_{out}(s) \cdot C_0 \cdot (L_2 \cdot C_2 \cdot R_3 \cdot C_3 + R_2 \cdot C_2 \cdot L_3 \cdot C_3)$$

$$C1 = s \cdot I_{out}(s) \cdot C_0 \cdot (L_3 \cdot C_3 + C_0 \cdot L_2 \cdot C_2 + R_2 \cdot C_2 \cdot R_3 \cdot C_3)$$

$$D1 = s \cdot I_{out}(s) \cdot C_0 \cdot (R_3 \cdot C_3 + R_2 \cdot C_2)$$

$$E1 = s \cdot I_{out}(s) \cdot C_0$$

$$F1 = C_0 \cdot (L_2 \cdot C_2 \cdot L_3 \cdot C_3 + L_0 \cdot C_2 \cdot L_3 \cdot C_3 + L_0 \cdot C_2 \cdot L_2 \cdot C_3)$$

$$G1 = C_0 \cdot (R_0 \cdot C_2 \cdot L_2 \cdot C_3 + L_2 \cdot C_2 \cdot R_3 \cdot C_3 + R_0 \cdot C_2 \cdot L_3 \cdot C_3 + L_0 \cdot C_2 \cdot R_2 \cdot C_3 + R_2 \cdot C_2 \cdot L_3 \cdot C_3)$$

$$H1 = C_0 \cdot R_0 \cdot C_2 \cdot R_2 \cdot C_3 + C_0 \cdot L_2 \cdot C_2 + C_2 \cdot L_3 \cdot C_3 + C_0 \cdot L_0 \cdot C_2 + C_0 \cdot L_3 \cdot C_3 + C_0 \cdot R_0 \cdot C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_2 \cdot C_2 \cdot R_3 \cdot C_3 + C_2 \cdot L_2 \cdot C_3 + C_0 \cdot L_0 \cdot C_3$$

$$I1 = C_2 \cdot R_2 \cdot C_3 + C_0 \cdot R_0 \cdot C_2 + C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_0 \cdot C_3 + C_0 \cdot R_2 \cdot C_2 + C_0 \cdot R_3 \cdot C_3$$

$$J1 = C_0 + C_2 + C_3$$

The current $I_b(s)$ can be expressed as:

$$I_b(S) = \frac{A2 \cdot S^4 + B2 \cdot S^3 + C2 \cdot S^2 + D2 \cdot S + E2}{F2 \cdot S^5 + G2 \cdot S^4 + H2 \cdot S^3 + I2 \cdot S^2 + J2 \cdot S} \quad \textbf{(4.26)}$$

where

$$A2 = s \cdot I_{out}(s) \cdot C_0 \cdot (L_0 \cdot C_2 \cdot L_3 \cdot C_3 + L_2 \cdot C_0 \cdot L_3 \cdot C_3)$$

$$B2 = s \cdot I_{out}(s) \cdot C_0 \cdot (L_2 \cdot C_2 \cdot R_3 \cdot C_3 + R_0 \cdot C_2 \cdot L_3 \cdot C_3 + L_0 \cdot C_2 \cdot R_3 \cdot C_3 + R_2 \cdot C_2 \cdot L_3 \cdot C_3)$$

$$C2 = s \cdot I_{out}(s) \cdot (C_2 \cdot L_3 \cdot C_3 + C_0 \cdot L_0 \cdot C_2 + C_0 \cdot L_3 \cdot C_3 + C_0 \cdot L_2 \cdot C_2 + C_0 \cdot R_0 \cdot C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_2 \cdot C_2 \cdot R_3 \cdot C_3)$$

$$D2 = s \cdot I_{out}(s) \cdot (C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_0 \cdot C_2 + C_0 \cdot R_3 \cdot C_3 + C_0 \cdot R_2 \cdot C_2)$$

$$E2 = s \cdot I_{out}(s) \cdot (C_0 + C_2)$$

$$F2 = C_0 \cdot (L_0 \cdot C_2 \cdot L_3 \cdot C_3 + L_0 \cdot C_2 \cdot L_2 \cdot C_3 + L_2 \cdot C_2 \cdot L_3 \cdot C_3)$$

$$G2 = C_0 \cdot (R_0 \cdot C_2 \cdot L_2 \cdot C_3 + R_0 \cdot C_2 \cdot L_3 \cdot C_3 + R_2 \cdot C_2 \cdot L_3 \cdot C_3 + L_0 \cdot C_2 \cdot R_3 \cdot C_3 + L_0 \cdot C_2 \cdot R_2 \cdot C_3 + L_2 \cdot C_2 \cdot R_3 \cdot C_3)$$

$$H2 = C_2 \cdot L_3 \cdot C_3 + C_2 \cdot L_2 \cdot C_3 + C_0 \cdot L_2 \cdot C_2 + C_0 \cdot L_0 \cdot C_2 + C_0 \cdot L_0 \cdot C_3 + C_0 \cdot L_3 \cdot C_3 + C_0 \cdot R_0 \cdot C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_2 \cdot C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_0 \cdot C_2 \cdot R_2 \cdot C_3$$

$$I2 = C_2 \cdot R_2 \cdot C_3 + C_0 \cdot R_0 \cdot C_2 + C_2 \cdot R_3 \cdot C_3 + C_0 \cdot R_0 \cdot C_3 + C_0 \cdot R_2 \cdot C_2 + C_0 \cdot R_3 \cdot C_3$$

$$J2 = C_0 + C_2 + C_3$$

By replacing *s* with $2\pi \cdot f \cdot i$, the frequency response of SC output current is:

$$I_{SC}(f) = I_a(f) \quad \textbf{(4.27)}$$

The frequency response of EC output current:

$$I_{EC}(f) = I_b(f) - I_{SC}(f) \tag{4.28}$$

The frequency response of Polypropylene capacitor output current:

$$I_{PPC}(f) = I_{out}(f) - I_{EC}(f) \tag{4.29}$$

The current gain of I_{EC} normalised by I_{SC} is:

$$Gain_{ECSC}(f) = \frac{|I_{EC}(f)|}{|I_{SC}(f)|} = \frac{\sqrt{(2\pi \cdot C_2 \cdot C_0 \cdot R_0 \cdot f)^2 + (4\pi^2 \cdot C_2 \cdot C_0 \cdot L_0 \cdot f^2 - C_2)^2}}{\sqrt{(2\pi \cdot C_2 \cdot C_0 \cdot R_2 \cdot f)^2 + (4\pi^2 \cdot C_2 \cdot C_0 \cdot L_2 \cdot f^2 - C_0)^2}} \tag{4.30}$$

At resonant frequency of the EC:

$$f_{resonantEC} = \frac{1}{2\pi\sqrt{L_2 \cdot C_2}} \tag{4.31}$$

The maximum current gain of I_{EC} normalised by I_{SC} is:

$$Gain_{ECSCMAX}(f) = \sqrt{\frac{(C_0 \cdot L_0 - C_2 \cdot L_2)^2 + C_2 \cdot {C_0}^2 \cdot L_2 \cdot {R_0}^2}{C_2 \cdot {C_0}^2 \cdot L_2 \cdot {R_2}^2}} \tag{4.32}$$

The current gain of I_{PPC} normalised by I_{SC} is:

$$Gain_{PPCSC}(f) = \frac{\sqrt{(2\pi \cdot C_3 \cdot C_0 \cdot R_0 \cdot f)^2 + (4\pi^2 \cdot C_3 \cdot C_0 \cdot L_0 \cdot f^2 - C_3)^2}}{\sqrt{(2\pi \cdot C_3 \cdot C_0 \cdot R_3 \cdot f)^2 + (4\pi^2 \cdot C_3 \cdot C_0 \cdot L_3 \cdot f^2 - C_0)^2}} \tag{4.33}$$

At resonant frequency of the PPC:

$$f_{resonantPPC} = \frac{1}{2\pi\sqrt{L_3 \cdot C_3}} \tag{4.34}$$

The maximum current gain of I_{PPC} normalised by I_{SC}:

$$Gain_{PPCSCMAX}(f) = \sqrt{\frac{(C_0 \cdot L_0 - C_3 \cdot L_3)^2 + C_3 \cdot {C_0}^2 \cdot L_3 \cdot {R_0}^2}{C_3 \cdot {C_0}^2 \cdot L_3 \cdot {R_3}^2}} \tag{4.35}$$

For both equations (4.30) and (4.33), the final current gain of the EC or PPC as the frequency increases to infinity, tends to:

$$Gain_{Final}(f) = \lim_{f\to\infty} Gain_{PPC/ECSC}(f) = \frac{L_0}{L_{3/2}} \quad \textbf{(4.36)}$$

Based on the developed mathematical model, the frequency response of a parallel SC, EC and PPC system is shown in Figure 4.26. The SC and EC parameters are the same as applicable to Figure 4.22, and the PPC has a capacitance of 2μF and resistance of 2.3mΩ, while the inductances of the three capacitors are all assumed as 20nH.

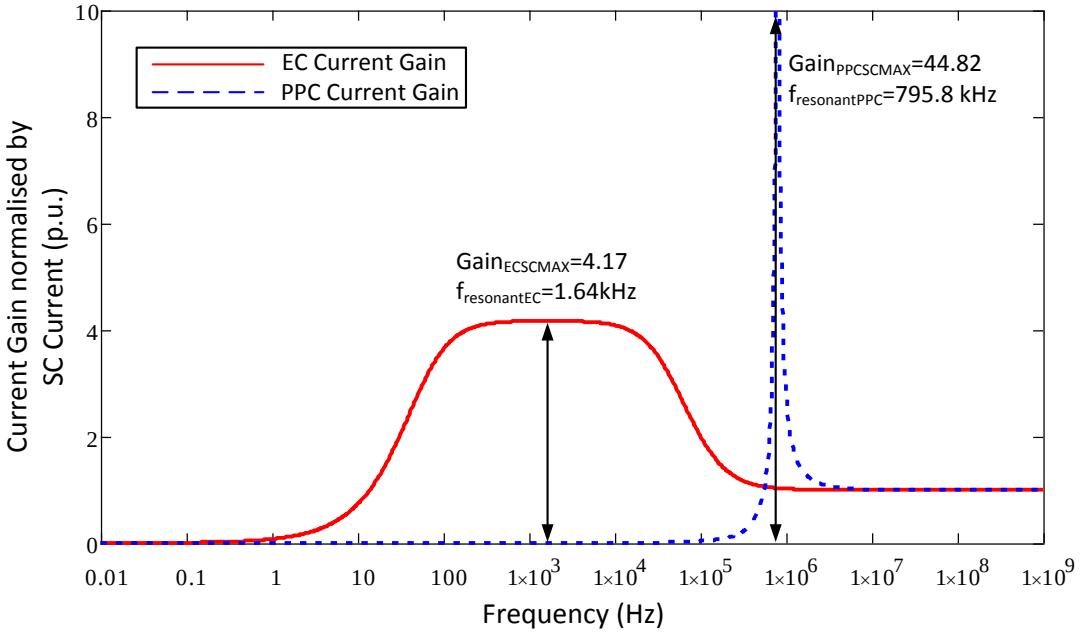

Figure 4.26 Frequency Response of the Parallel Three Capacitors System.

The frequency response in Figure 4.26 shows the PPC current gain is only effective at frequencies above 100kHz, which is relative high for an energy storage system. For the EC current gain, in low frequency range, the response is the same as it shown in Figure 4.22, while at high frequency, due to the inductive component, the response drops to 1 according to equation (4.36). For the PPC current gain, the maximum occurs at the PPC resonant frequency of 795.8kHz, and is 44.82.

Based on the above mathematical model, it can be concluded that the current gain of a specified capacitor depends on the capacitors involved in the normalisation. The

maximum current gain occurs at the resonant frequency, while the final current gain depends on the inductance.

4.6 Summary

Due to its ultra high capacitance, the supercapacitor is ideal for high power pulse applications. However, for short duration (<1s) applications, the efficiency of the supercapacitor can be lower than 55% when discharged at its peak current. The electrolytic capacitor, which has a higher power capability and efficiency, is introduced in parallel with the supercapacitor to improve energy storage system performance. The proposed SCEC system improves the efficiency in transient conditions by over 10%. Mathematical modelling, simulation and experimentation have been developed to verify the higher efficiency of the SCEC system, compared to a SC system. The efficiency characteristics are discussed based on the mathematical model, and experimentally verified. Theoretically, the SCEC system has better power capability and response time. A design guide with a practical application design example was presented for the SCEC system. Frequency analysis either in time domain or frequency domain completes the SCEC system performance assessment. The mathematical model for three branches, which included series inductance, was developed for analysing a general parallel capacitor system in the frequency domain.

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Chapter 5

5 Feasibility Analysis for Supercapacitor Based STATCOM

A static synchronous compensator (STATCOM) is a common device in flexible ac transmission systems (FACTS), which has been widely used over the past decade [5.1, 2]. A STATCOM is typically applied in a power system to support the voltage, increase transmission capability, enhance voltage stability, and improve transient stability, which are realised by controlling the reactive power exchanged with the power system [5.3-5]. As the STATCOM has a faster dynamic response, better voltage quality, and higher accuracy in reactive power control than conventional synchronous generators or thyristor based static compensators, it has an increasing potential in power system applications [5.6, 7].

However, due to its restricted capability to deliver active power, the STATCOM is ineffective in situations which require active power compensation. Active power control can provide better performance by damping power swings and improving the transient stability [5.3, 8]. To extend system stability margins, energy storage devices are used with the STATCOM to enable active power exchange capability with the grid [5.8, 9]. With significant developments in energy storage technologies, including battery technologies, fuel cells, flywheel energy storage and superconducting magnetic energy storage, it is realised that a combined energy storage system with the STATCOM can inject/absorb active power to balance power system mismatch [5.3, 8, 10-13]. However, these technologies have limitations in power capability, response time, and life time.

The supercapacitor, SC, due to its good performance when supplying a high power pulse condition, is suitable as an energy storage system for the STATCOM [5.14-17]. In this chapter, the supercapacitor based STATCOM is proposed, which is able to provide both active and reactive power control functions. The SC based STATCOM aims to provide reactive power during normal conditions, which normalise the grid voltage to the required level. During transient conditions, such as faults or sudden load changes, it is able to provide active power to stabilise the power system frequency. Further analysis of the energy storage system, based on supercapacitors

in parallel with other capacitor types, is introduced to improve the efficiency, volume, thermal performance, cost, and lifetime. The developed supercapacitor based STATCOM topology and control system are introduced. Simulations under different conditions are analysed to evaluate the performance of using supercapacitors in a STATCOM during both steady-state and transient conditions. The current, voltage, efficiency, and thermal characteristics of a single cell supercapacitor are scaled up in the energy storage system to analyse the feasibility of applying supercapacitors within a STATCOM.

5.1 Supercapacitor Based STATCOM

The proposed supercapacitor based STATCOM is developed to control both reactive and active power exchange with the power system. The control objective is to maintain the voltage and frequency of the common coupling point at the grid load side. The ac voltage is realised by reactive power control during normal conditions. Frequency control is achieved by varying the dc link voltage within the STATCOM, which can either sink or source active power to stabilise the system frequency oscillations during transient conditions. The SC is directly attached to the dc link of the STATCOM. Due to its ultra high capacitance, the SC is able to provide active control by varying the dc link voltage within a suitable range. The basic STATCOM operating principle is introduced, and the associated SC based energy storage system is developed to provide transient active power control. The STATCOM topology is based on a three-level H-Bridge voltage source converter, while the control system is developed with a *dq* frame control algorithm.

5.1.1 Introduction of STATCOM

Theoretically, all types of dc/ac and ac/ac converters have the ability to control reactive power. However, compared to the dc/ac converter, the ac/ac converter is more costly and complicated in high power applications [5.1]. In FACTS controllers, most devices are developed using dc/ac converters. As the converters input and output are connected by a number of solid switches, no energy can be stored within the converter, which implies the instantaneous input power has to be equal to the instantaneous output power. The input and output terminals has to be

complimentary as well, which means if the input is a voltage source, the output has to be a current source and vice versa. In dc/ac converters, the dc side is normally considered the input, where the converters are distinguished as voltage-sourced and current-sourced converters by connecting the dc side with a voltage source (capacitor) or a current source (inductor).

Most present FACTS devices, including the STATCOM, are developed based on the voltage-sourced converter (VSC) rather than the current-sourced converter (CSC). The following summarise the reasons which limits the application of current-sourced converter in FACTS devices:

1. Power semiconductors used in the CSC have to be able to block voltage bi-directionally. For available high power semiconductors, such as the IGCT and IGBT, it either does not have reverse voltage block capability (specifically the IGBT) or has a slow switching speed (specifically the symmetrical IGCT). In practice, CSC losses are higher than those of the equivalent VSC.
2. The CSC requires a voltage source at the ac side, which is usually a capacitive filter. However, the ac side current source for the VSC is inherently provided by the leakage inductance of the ac transformer, whence no further filtering is required.
3. The VSC can provide protection of the power semiconductors during a transient fault on transmission line voltage, while overvoltage protection or higher semiconductors ratings are required by the current-sourced converter.

Due to the advantages of the VSC, the STATCOM employed in this chapter is based on the VSC. As a regulating device used in an ac transmission system, the basic topology in single-line diagram form is shown in Figure 5.1. With dc capacitor C_{dc}, which operates as the input voltage source, the converter generates a set of controllable three-phase output voltages $V_{STATCOM}$ at the ac power system frequency. Each phase voltage is coupled to the corresponding ac system voltage V_{Grid} via the per phase leakage inductor of the coupling transformer with a relatively small inductance of 0.1-0.15 p.u. [5.1]. By controlling the amplitude of $V_{STATCOM}$, the STATCOM can be controlled to generate or absorb reactive power. That is, if the

amplitude of $V_{STATCOM}$ is increased above that of V_{Grid}, the converter generates reactive power for the ac system. If the amplitude of $V_{STATCOM}$ is lower than that of the V_{Grid}, the converter absorbs reactive power.

The voltage source dc to ac converter produces a pulse-width modulated output voltage waveform. By phase-shifting the voltage waveform, a three-phase voltage is produced as the final output voltage of the complete converter. With proper design, the output voltage can approximate a sine wave with no (or minimal) filtering. A filter is used in the simulation model to improve the output waveform, which means the waveform is considered a pure sine wave to simplify the analysis.

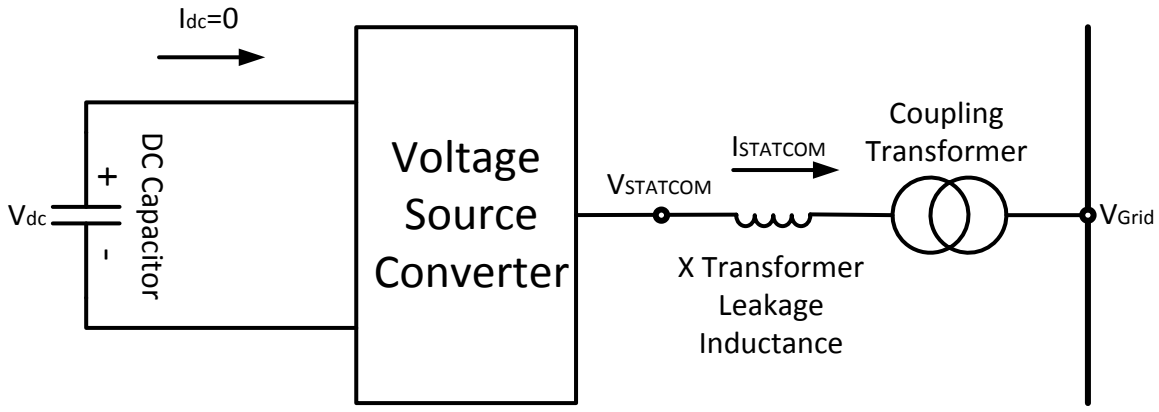


Figure 5.1 Basic Topology of STATCOM.

Since the converter only generates/absorbs reactive power, the dc capacitor at zero frequency contributes no reactive power by definition. In other words, the converter interconnects the three ac terminals such that the reactive output currents flow freely between them [5.1]. The storage dc capacitor is theoretically used to compensate the fluctuating component within the net instantaneous output power (VA). During the switching of the power electronic devices in a VSC, the dc capacitor has to absorb the switching ripple current even in perfect sine conditions on the ac output.

In a practical converter, the semiconductor switches suffer losses, which tend to discharge the dc capacitor. To avoid such a condition, the converter is controlled to absorb a small amount of real power from the ac system by making $V_{STATCOM}$ lag

V_{Grid} by a small angle. The phase angle adjustment control can also be used to control the reactive power flow. By charging or discharging the dc link capacitor voltage, the converter output voltage amplitude is regulated to generate/absorb reactive power [5.1]. Similar idea is applied for the proposed supercapacitor based STATCOM, which charging/discharging the SC can control active power exchange with the ac power system.

As mentioned, it is possible to use an energy storage device on the dc link, such as a supercapacitor or battery. In this case, both reactive and real power exchange can be controlled by the converter, thus it can function as a static synchronous generator. The SC based STATCOM introduced in this chapter, replaces the dc capacitor with a supercapacitor, which can provide much more energy when discharging the dc link voltage, that is, higher real power capability. The capability of controlling active and reactive power exchange enables the STATCOM to be applied in smoothing power oscillation, levelling peak power demand, and providing uninterrupted power for critical loads [5.1].

5.1.2 Supercapacitor Based STATCOM Modelling

The SC based STATCOM can be modelled with five parts, which are the supercapacitor based energy storage system at the dc link, the voltage source converter, the three-phase filter, the three-phase transformer, and the measurement device. The Simulink topology is shown in Figure 5.2. The SC based energy storage system is connected to the dc link at a voltage of 500V. The voltage source converter with a maximum power limit of 1MVA is connected to the coupling transformer via the filter. The LC filter, including a series LC (34mH and 0.3mF) and parallel LC (17mH and 0.6mF), resonates at the fundamental frequency of 50Hz. The series LC blocks high order voltage harmonics and the parallel LC bypass the high order current harmonics to improve the output waveforms. The three-phase transformer, which is 280V/3.3kV rated at 1MVA, connects the STATCOM to the ac grid. The STATCOM measurement records the three-phase voltage, current and frequency signals for the VSC control system for regulating the converter output.

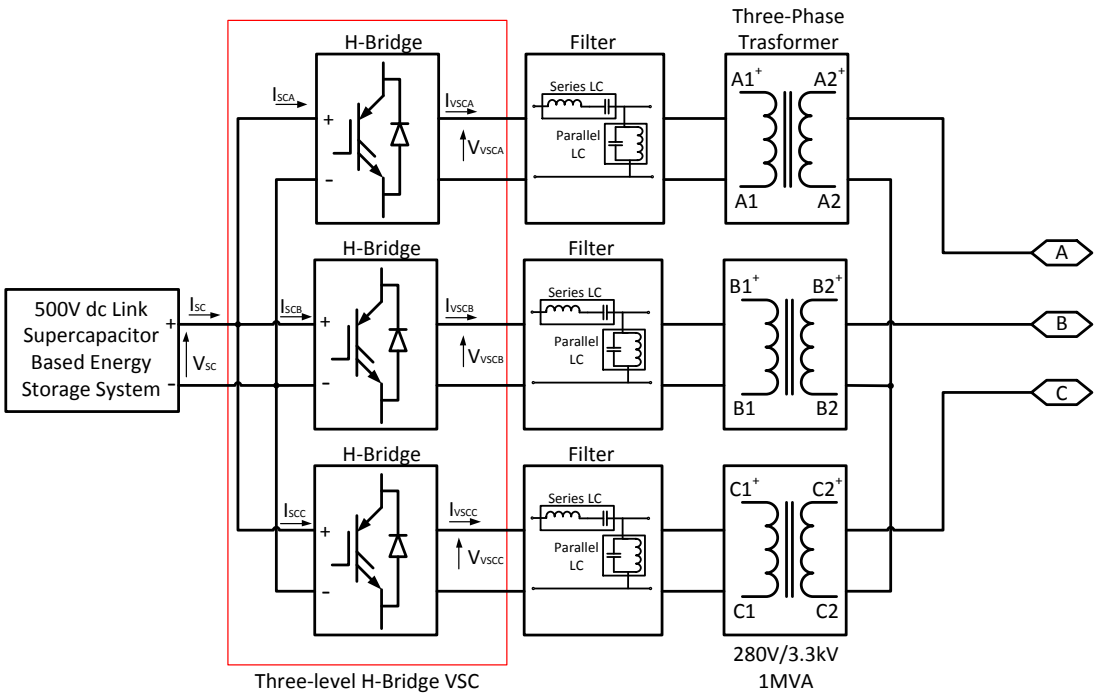


Figure 5.2 STATCOM topology in Simulink.

Based on the measured ac side signals, the control system calculates the required VSC output voltage, and generates the gate signal by using sinusoidal pulse-width modulation (SPWM). By proper control, the SC based STATCOM can generate/absorb both active and reactive power to maintain the voltage at the measurement point at the required level, and damp any frequency oscillations.

As the analysis here focuses on the effects of replacing the dc capacitor with a SC based energy system, the output current I_{SC} and voltage V_{SC} of the SC are monitored during normal and transient conditions. The energy loss, rms ripple current, efficiency during active power compensation, and thermal variation are analysed for different load conditions. Additionally, different energy storage systems, based on different combinations of capacitor types, are compared to improve the storage volume and efficiency performance.

5.1.3 Supercapacitor Energy Storage System Description

Due to the low operating voltage limitation of 2.7V, supercapacitors need to be connected in series and parallel for grid level application. The BCAP3000, which

has the highest capacitance in the Maxwell's product range, is used in the simulations and its key data is summarised in Table 5.1.

Table 5.1 Single SC Cell Data for BCAP3000

Capacitance (F)	Resistance (mΩ)	Voltage (V)	Max Continuous Current (ΔT = 40℃)	Thermal Resistance (℃/W)	Thermal capacitance (J/℃)	Weight (kg)
3000	0.29	2.7	$210A_{RMS}$	3.2	600	0.51

The dc link voltage for the STATCOM is 500V, which means 200 BCAP3000s need to be connected in series to achieve the 500V requirement. The voltage source converter has a maximum power limit of 1MVA, where four strings of series supercapacitor banks are parallel connected to meet the ripple current limit when the STATCOM operates at rated conditions. The SC based energy storage system specification is shown in Table 5.2.

Table 5.2 SC Energy Storage System

DC link Voltage	$V_{SC} = 500V$	Total Capacitance	60F
Series SC No.	$N_{series} = 200$	Total Energy at 500V in SC	7.5MJ
Parallel SC No.	$N_{parallel} = 4$	Useable Energy (DC link Discharge to 350V)	3.825MJ
Total Resistance	14.5mΩ	RMS Current(ΔT = 40℃)	$840A_{RMS}$

However, the parallel capacitor SCEC system in Chapter 4 can be used as an energy storage system. As shown, the four SC strings are parallel to satisfy the rms ripple current requirement. The electrolytic capacitor (EC) and film capacitor (FC) are parallel connected to the SC. Compared to EC, FC can supply a much higher current at high frequency and has a higher reliability and better thermal performance at high ripple current condition though its energy density is much lower. In such case, two combined energy systems are developed and compared with the purely SC storage system.

To avoid balancing problem, EC and FC are selected to be capable of withstanding peak voltages in excess 500V. The capacitance, resistance, rms current rating, and volume are considered for the capacitor selection, where the EC and FC cell data are summarised in Table 5.3.

Table 5.3 Single EC and FC Cell Data

	Capacitance (μF)	Resistance (mΩ)	Voltage (V)	RMS Current (A)	Volume ($\times 10^6 mm^3$)	Weight (kg)
EC[5.18]	8400	14.3	500	31	1.36	1.658
FC[5.19]	900	1.1	700	80	1.00	1.13

Since the EC or FC carries the high frequency components, while under normal conditions, their dc component is small enough to be ignored, most of the ripple current is at high frequency. For such conditions, capacitors have to be paralleled to achieve the rms current requirement of 830A at rated load condition. The proposed EC and FC systems are compared with a single SC string in Table 5.4.

As Table 5.4 shown, the EC and FC systems can handle the same rms current with a much smaller volume and less cost than the SC system. The resistances are also much less which effectively improves the energy storage system efficiency. As the high frequency ripple current is carried by the EC or FC, the parallel number for the SC system can be reduced based on the active power requirement during transient

conditions. In addition, the SC in the parallel capacitor system only supports the dc component of the dc link current, that is, transient active power exchange, thus its thermal performance and life expectation are improved.

Table 5.4 EC, FC and Single SC String Compare

	EC System	FC System	SC Single String
Parallel Number	28	11	1
Cost ($)	6440	1870	12000
Capacitance (F)	0.2352	9.9×10^{-3}	15
Resistance (mΩ)	0.511	0.1	58
Voltage (V)	500	700	500
RMS Current (A)	868	880	210
Weight (kg)	46.424	12.43	102
Volume ($\times10^6 mm^3$)	38.1	11	80.6

5.1.4 VSC Control System

The VSC control system is based on a *dq* control algorithm. In a balanced three-phase system, by ignoring the zero-sequence components, the three-phase system *abc* to rotating frame *dq* transformation can be expressed as [5.20, 21]:

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos(\omega \cdot t) & cos(\omega \cdot t - 120°) & cos(\omega \cdot t + 120°) \\ -sin(\omega \cdot t) & -sin(\omega \cdot t - 120°) & -sin(\omega \cdot t + 120°) \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad \textbf{(5.1)}$$

Based on equation (5.1), the three-phase system voltages and currents are processed in the *dq* frame. The control objective is to maintain the ac voltage and frequency stable through controlling the active and reactive power exchange between the STATCOM and the ac network. The control algorithm development is as follows:

The control algorithm is based on [5.22, 23], where the mathematical model describing the VSC in the *dq* frame is:

$$\frac{di_{sd}}{dt} = -\frac{R_T}{L_T} + \frac{(V_{sd} + \omega \cdot L_T \cdot i_{sq} - V_{gd})}{L_T} \quad \textbf{(5.2)}$$

$$\frac{di_{sq}}{dt} = -\frac{R_T}{L_T} + \frac{(V_{sq} - \omega \cdot L_T \cdot i_{sd} - V_{gq})}{L_T} \quad \textbf{(5.3)}$$

where R_T and L_T are the total resistance and inductance of the coupling transformer. The cross-coupling terms U_d and U_q are defined as:

$$U_d = V_{sd} + \omega \cdot L_T \cdot i_{sq} - V_{gd} \quad \textbf{(5.4)}$$

$$U_q = V_{sq} - \omega \cdot L_T \cdot i_{sd} - V_{gq} \quad \textbf{(5.5)}$$

By substituting U_d and U_q into equations (5.2) and (5.3), the basic control equation is:

$$\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} -\frac{R_T}{L_T} & 0 \\ 0 & -\frac{R_T}{L_T} \end{bmatrix} \cdot \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_T} & 0 \\ 0 & \frac{1}{L_T} \end{bmatrix} \cdot \begin{bmatrix} U_d \\ U_q \end{bmatrix} \quad \textbf{(5.6)}$$

Based on equation (2.3), the inner current controller which regulates the *dq* currents can by expressed in a PI controller form:

$$U_d = K_{pi} \cdot (i_{sd}^* - i_{sd}) + K_{ii} \cdot \int (i_{sd}^* - i_{sd})\, dt \quad \textbf{(5.7)}$$

$$U_q = K_{pi} \cdot (i_{sq}^* - i_{sq}) + K_{ii} \cdot \int (i_{sq}^* - i_{sq})\, dt \quad \textbf{(5.8)}$$

where K_{pi} and K_{ii} are the proportional and integral gains of the inner current controller, and the superscript * denotes a reference value.

In the STATCOM, ac voltage V_g is used to control the reactive power exchange with the ac network, while the dc link voltage V_{dc} is used to control the active power. These two control signals provide the inner current controller references:

$$i_{sd}^* = K_{pdc} \cdot (V_{dc} - V_{dc}^*) + K_{idc} \cdot \int (V_{dc} - V_{dc}^*)\, dt \quad \textbf{(5.9)}$$

$$i_{sq}^* = K_{pac} \cdot (V_g - V_g^*) + K_{iac} \cdot \int (V_g - V_g^*)\, dt \quad \textbf{(5.10)}$$

The references for the ac and dc voltages are 1 p.u. in the conventional STATCOM, which focuses on the reactive power control. In the proposed STATCOM, the ac network frequency, which can reflect active power mismatch in the network, is used as a control signal to generate the dc link voltage reference V_{dc}^{*}. The PI controller is expressed as follows:

$$V_{dc}^{*} = K_{pf} \cdot (f - f^{*}) + K_{if} \cdot \int (f - f^{*})\, dt \qquad \textbf{(5.11)}$$

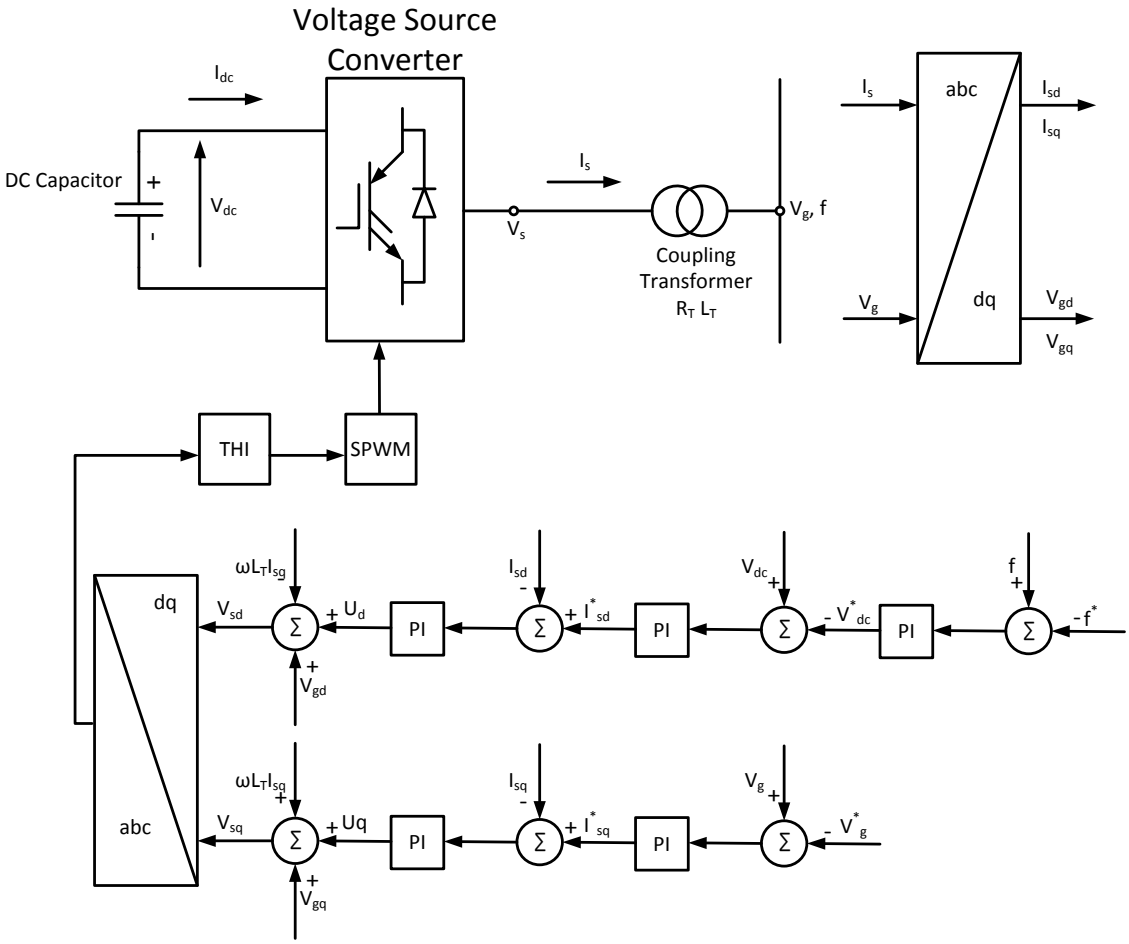


Figure 5.3 VSC control system.

The complete control system is shown in Figure 5.3. The measured parameters are grid side ac voltage V_g and current I_s which are transformed into the *dq* frame, grid side frequency f and dc link voltage V_{dc}. The system calculates the required VSC

output voltage V_s, where third harmonic injection (THI) is used to achieve a better dc link voltage utilisation and reduce harmonic ratios [5.24, 25]. Based on this three-phase signal, SPWM generates the gate signals to drive the converter.

5.1.5 VSC Topology and SPWM

The VSC in the STATCOM produces the three-phase sine-wave output voltage. In practice, VSCs are constructed based on several basic converter topologies, including single-phase H-bridges, three-phase, two-level, six-pulse bridges, or three-level, 12-pulse bridges [5.1]. The converters valves are compromised of series and parallel connected power semiconductors, such as IGBTs with reverse-parallel diodes. The output voltage waveforms of the converters are in the form of square, quasi-square or pulse-width modulated waveforms. The final output voltage is produced by phase-shifting the three-phase voltage and using a filter to reduce the harmonics.

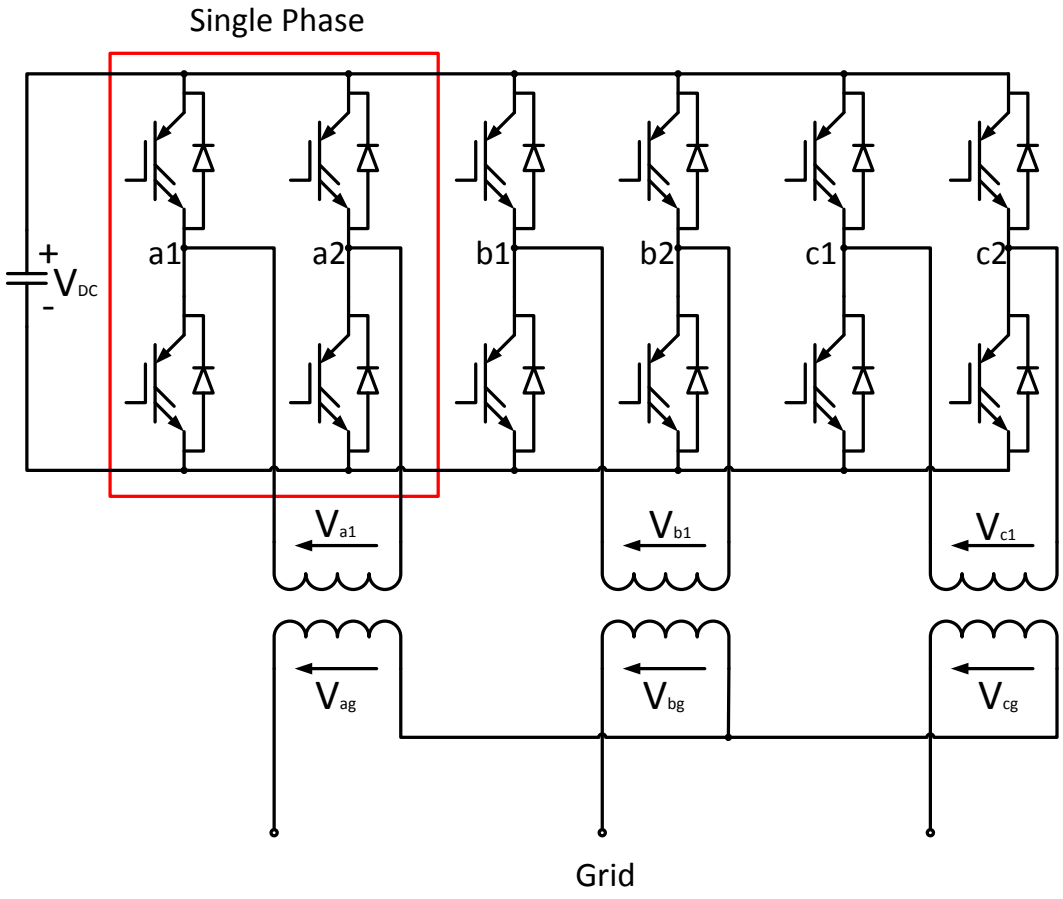


Figure 5.4 3L-HB-VSC Topology.

The three-level H-Bridge voltage source converter in Figure 5.4 is selected where each phase is controlled by an H-bridge converter. Based on such topology, the three phases of the VSC can be controlled separately, and the H-bridge topology enables unipolar SPWM, which reduces the high frequency harmonics and produces better VSC output waveform. As the IGBTs of each phase operate use the same control principle but phase-shifted, the switching operation is introduced based on the single phase H-Bridge topology shown in Figure 5.5. IGBTs are switching at 2.1 kHz. Three output levels are achieved by different switch combination. For positive output, IGBT1 and IGBT4 are closed while IGBT2 and IGBT3 are open, the output V_{AC} equals to V_{DC}. For negative output, IGBT1 and IGBT4 are open while IGBT2 and IGBT3 are closed, and the output V_{AC} equals $-V_{DC}$. For zero output, IGBT1 and IGBT3 are closed while IGBT2 and IGBT4 are open, the output V_{AC} equals to zero. To balance switch losses, alternating zero voltage loops are used, where the next zero voltage output involves IGBT2 and IGBT4 are closed while IGBT1 and IGBT3 are open. By maintaining a $120°$ phase-shift from each other phase, the three-phase voltage is connected to the filter to eliminate harmonic components.

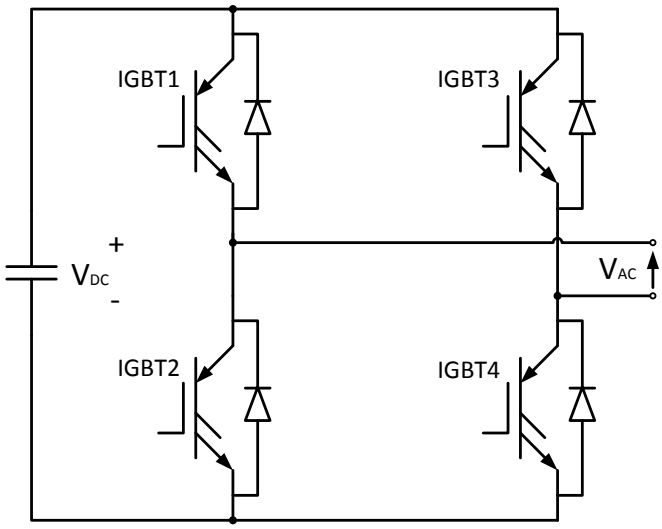
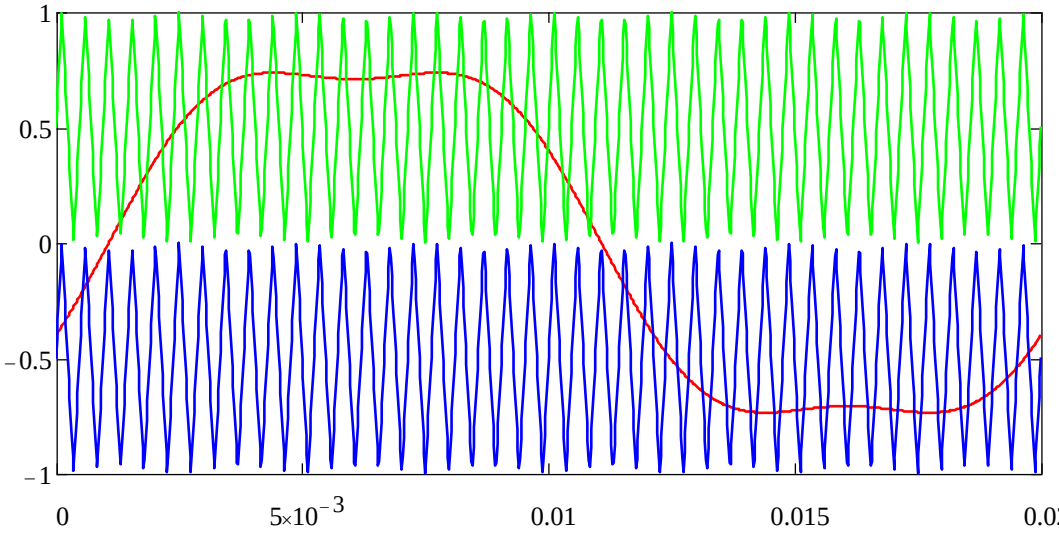


Figure 5.5 Single Phase Topology.

Sinusoidal pulse width modulation is employed for IGBT gate signal generation. The on and off signals are determined by comparing a modulating sine-wave with the carrier triangle wave. The output voltage magnitude is determined by the peak

amplitude of modulating wave, while the output voltage frequency is determined by the modulating wave frequency. The IGBT switching frequency is determined by the carrier frequency. As mentioned, THI is applied to the modulating sine-wave to produce a higher amplitude modulated output waveform.

Based on the control system calculation results, the required output voltage signal V_a is compared with two triangle carrier waveforms V_{C1} and V_{C2}, as shown in Figure 5.6. If $V_a > V_{c1}$, a positive output condition is activated. If $V_a < V_{c2}$, a negative output condition is activated. If $V_{c2} \leq V_a \leq V_{c1}$, a zero output condition is activated.



	IGBT1	IGBT2	IGBT3	IGBT4	V_{AC}
Va>Vc1	1	0	0	1	V_{DC}
Vc2≤Va≤Vc1	1	0	1	0	0
	0	1	0	1	0
Va<Vc2	0	1	1	0	$-V_{DC}$

Carrier Wave Vc1
Carrier Wave Vc2
Phase Voltage
Reference Va
1 Represents on
0 Represents off

Figure 5.6 SPWM Operating Principle.

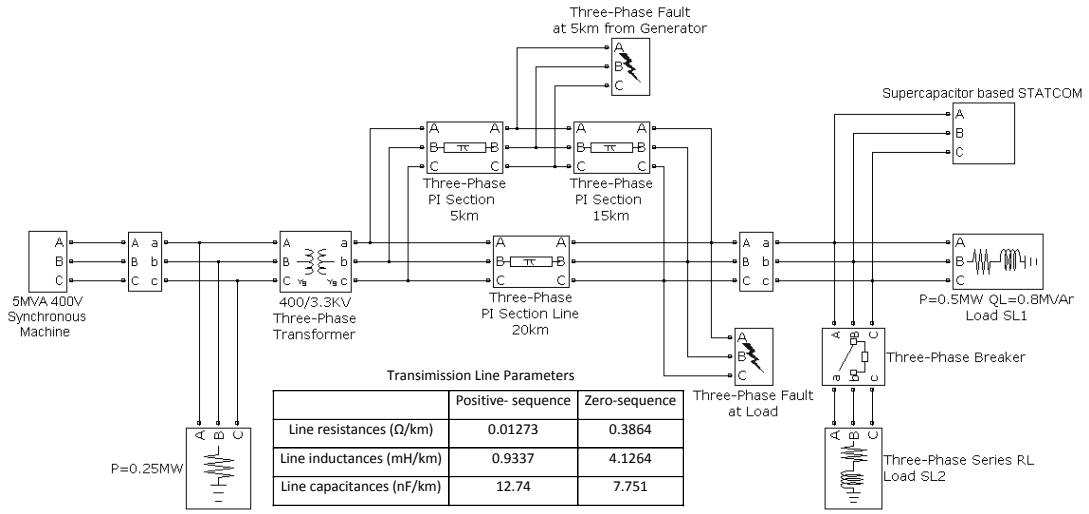
An example of single phase gate signal generation process is shown in Figure 5.6. By comparing the single phase voltages V_a with V_{C1} and V_{C2}, the gate signal is generated based on the switch combination table. Based on the output voltage

reference of each phase, the gate signals are generated to produce the required three-phase output voltage.

5.2 Supercapacitor Based STATCOM Normal Condition Analysis

The proposed SC based STATCOM system is developed in Matlab/Simulink for simulation. Normal condition analysis focuses on the steady-state response of the supercapacitor based energy storage system at different load conditions. By analysing the output current of the SC, that is, the input current of the VSC, the ripple current rms value, power loss of the energy storage system, and thermal effects are presented. Two current waveform analysis methods are used, which are the Fast Fourier Transform (FFT) method and a mathematical method. According to the analysis results, an energy storage system based on parallel EC or FC with the SC is developed to improve the efficiency and capacitor volume. The performance of the different parallel capacitor energy storage systems are compared and discussed for suitable application suitability.

5.2.1 Power System Simulation Description



Transimission Line Parameters

	Positive- sequence	Zero-sequence
Line resistances (Ω/km)	0.01273	0.3864
Line inductances (mH/km)	0.9337	4.1264
Line capacitances (nF/km)	12.74	7.751

Figure 5.7 Test Power System Configuration.

The power system shown in Figure 5.7 is the test system for the proposed SC based STATCOM. A synchronous machine, rated at 400V, 5MVA, is used as the system

power source. The load S_{L1} is connected to the 3.3kV transmission line through a 400V/3.3kV step-up transformer. The transmission line model is based on two 20km parallel connected three-phase PI section lines where the line parameters are shown in Figure 5.7. The switching load S_{L2} is used to verify the transient response of STATCOM under a sudden load change condition. The STATCOM is connected at the load side to maintain the ac voltage and provide active power when required.

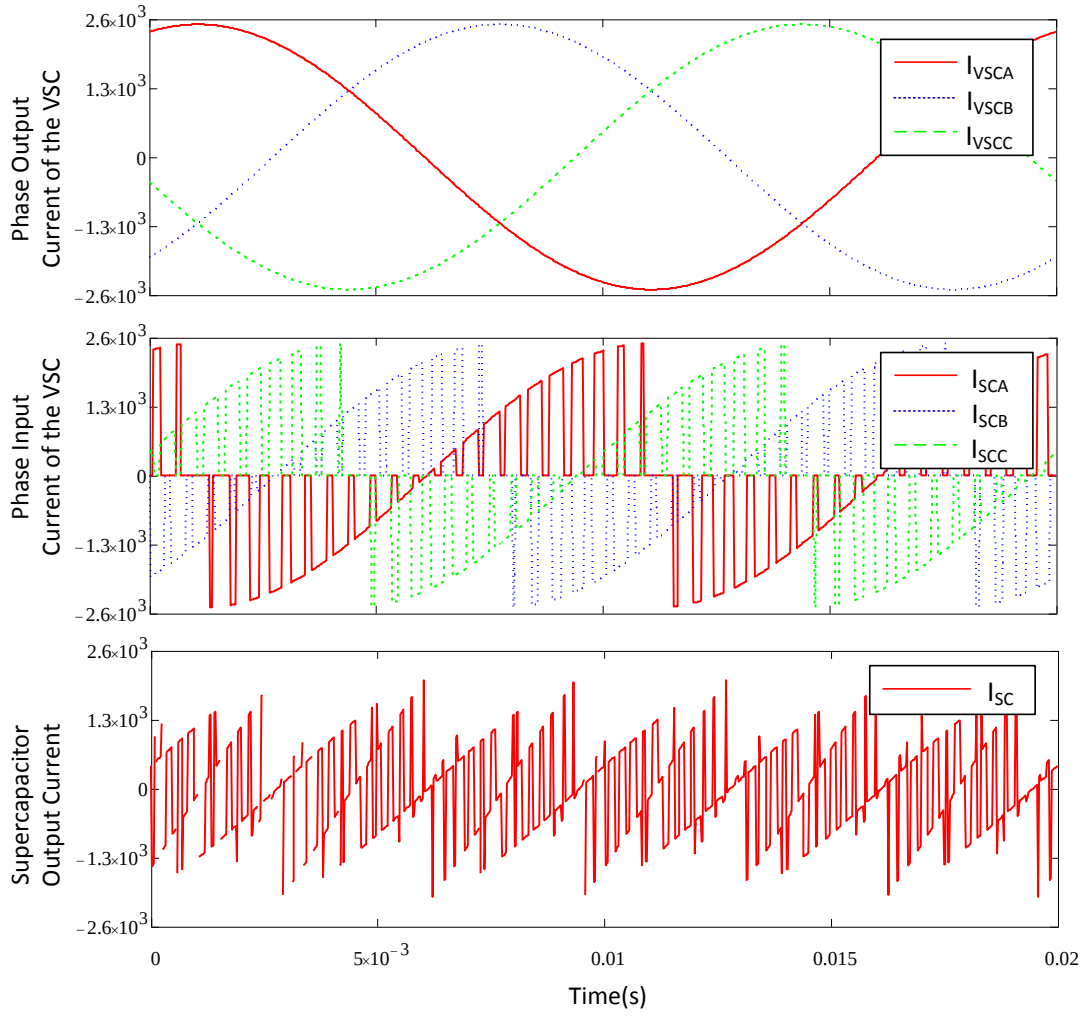


Figure 5.8 Current Waveform at Normal Condition.

Under normal conditions, the STATCOM only provides reactive power to support the load voltage. With a load S_{L1} = (0.5+j0.8)MVA, the STATCOM generates 0.85MVAr, which is 85% of its maximum rating. To analyse the feasibility of using supercapacitors in the STATCOM, the simulation initially focuses on the behaviour of the supercapacitor based energy storage system. The main analysis target is the

SC output current I_{SC}, which is related to the power loss and thermal limit for the proposed supercapacitors. The output dc current I_{SC} can be considered as the sum of the VSC dc input currents I_{SCA}, I_{SCB} and I_{SCC}, as shown in Figure 5.2.

The current waveform under normal conditions in one fundamental period (0.02s) is shown in Figure 5.8. As stated, the VSC output current is purely sinusoidal. However, the output current of the SC is a complex waveform which is difficult to describe in a simple equation form. Two different analysis methods are used, where the FFT method focuses on the harmonic analysis, while the mathematical model is more flexible for power loss calculation.

5.2.2 DC Link Current Analysis Based on FFT

The FFT method is based on the actual SC output current waveform. The FFT analysis tool is built into the Powergui in Simulink, which can be calculated the magnitude and phase of each harmonic order of the waveform. By choosing the large amplitude harmonics, the waveform can be described as a sum of several sinusoidal waves. An analysis example based on a light load condition S_{L1} = (0.3+j0.2)MVA is shown in Figure 5.9.

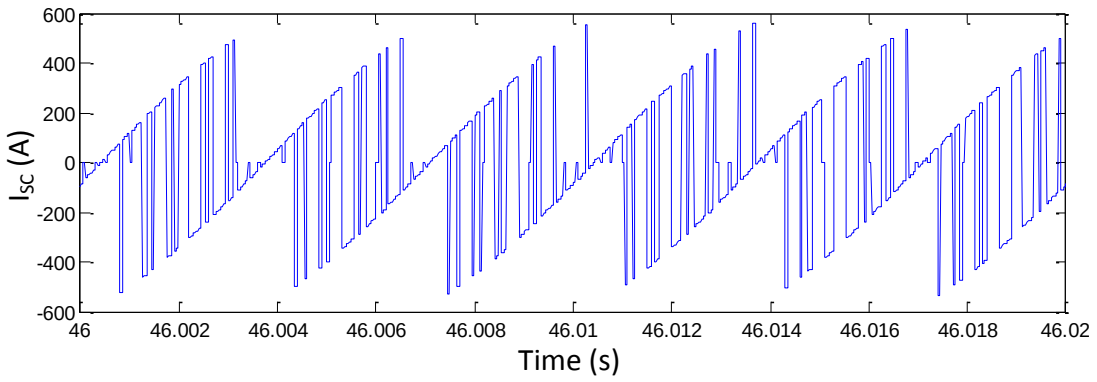


Figure 5.9 I_{SC} at S_{L1} = (0.3+j0.2)MVA.

Based on the I_{SC} simulation result shown in Figure 5.9, the Powergui FFT Analysis tool generates a harmonic report with the fundamental frequency f_0 = 50Hz. The harmonic plot is shown in Figure 5.10, and the large amplitude harmonics are

summarised in Table 5.5, where the amplitude percentage is defined as the ratio of the amplitude of the specified harmonic and the SC output current magnitude.

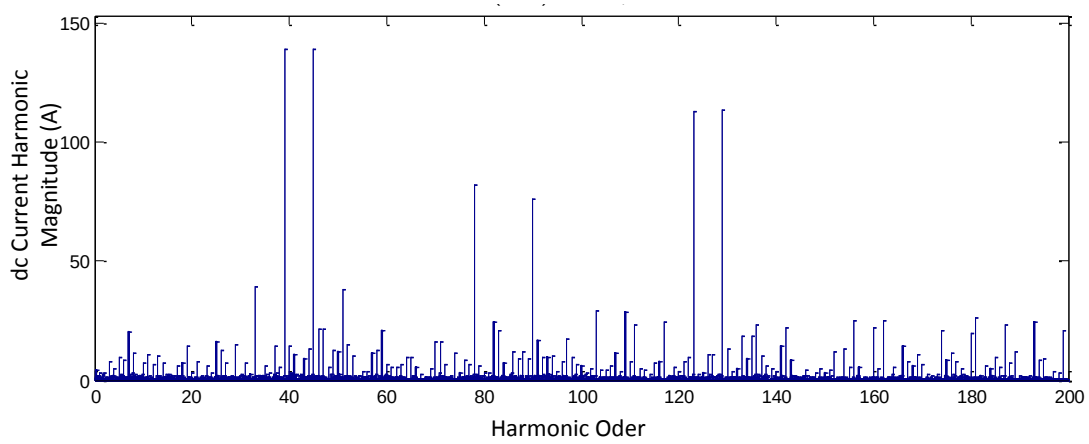


Figure 5.10 Harmonic Plot for S_{L1} = (0.3+j0.2)MVA.

As shown in Figure 5.10, the large harmonics are distributed within the bandwidth and symmetrical to the integral multiple of the switching frequency f_c = 2.1kHz. By using the magnitude and phase of the large amplitude harmonics, the I_{SC} can be approximated in a sinusoidal Fourier mathematical model. The I_{SC} comparison plot between the FFT method I_{SCfft} and the simulation result $I_{SCsimulation}$ is shown in Figure 5.11. The FFT plot fits well with the simulation result at the middle period part, but the maximum positive and negative end excursions of the period are suppressed.

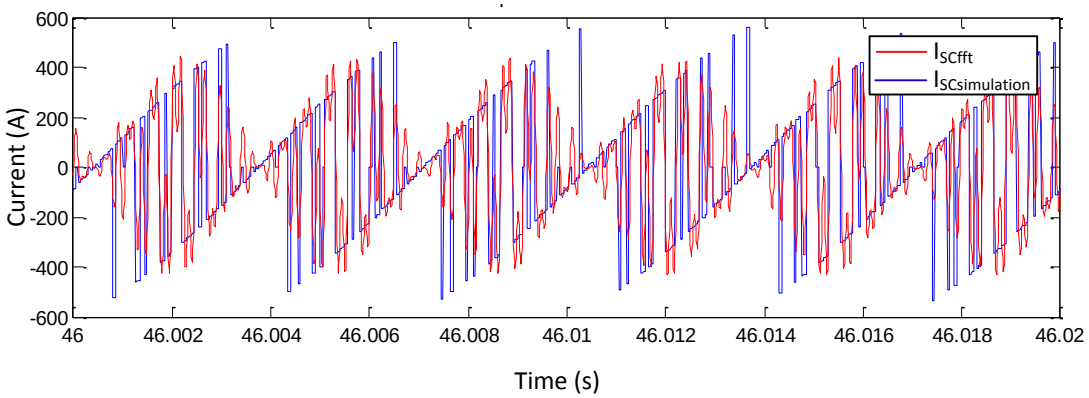


Figure 5.11 I_{SC} Compare Plot for FFT Method.

The large amplitude harmonic distribution varies as the load condition changes. Table 5.5 lists harmonics distribution of the SC output current normalised by the peak dc current I_{SCpeak} under different load conditions. For light and medium load conditions, the load requires the same active power of 0.3MW and reactive powers of 0.2MVAr and 0.8MVAr respectively. As the reactive power is supported by the STATCOM, the modulating waveforms are different in order to produce the required reactive power, which results in a different harmonic distribution, as shown in Table 5.5. For medium and large load conditions, the load requires same reactive power of 0.8MVAr and active power of 0.3MVAr and 0.5MVAr respectively. The harmonic distributions of the SC output current are similar due to the same reactive power required by the load. It can be concluded that, under different load conditions, especially large difference in reactive power, the STATCOM has to operate at different conditions to support the grid voltage. As a result, the SPWM generates different current waveforms to satisfy the required load condition. The single FFT analysis result is only valid for analysing the same load condition, and cannot be used to predict the SC output current under variable load conditions.

According to the harmonic distribution shown in Table 5.5, the large amplitude harmonics are in the high frequency range, above 1.5kHz. The dc and fundamental frequency are relatively small compared to the high frequency components in the dc link. As the frequency analysis showed in Chapter 4, the high frequency components are sourced by the EC or FC in parallel with the SC. In such conditions, the SC-only provides the dc component, while the EC and FC, especially the FC which has higher ripple current capability, can carry the high frequency component.

Based on frequency analysis of the parallel capacitor system, the current gain of the SCEC and SCFC system are plotted to verify the current sharing relationship of the high frequency components. The EC and FC system data are based on Table 5.4, which are paralleled with one SC string. As the large amplitude harmonics are above 1.5kHz, inductance effects are included. The inductance for each SC, EC and FC single cell are all in the order of nanohenries (nH) [5.26-28]. As the SCs are series connected, while the ECs and FCs are parallel connected, the SC string has a higher inductance than the EC and FC banks, in theory. In the mathematical model, the

inductance of the SC, EC and FC banks are assumed to be 50nH. The current gain of the EC and FC normalised by the SC current are plotted with and without inductor in Figure 5.12.

Table 5.5 Large Amplitude dc Current Harmonics Distribution Comparison

Harmonic Order	Harmonic Distribution	Large Amplitude Harmonics Amplitude Percentage		
		Light Load S_{L1}=(0.3+j0.2)MVA	Mid Load S_{L1}=(0.3+j0.8)MVA	Large Load S_{L1}=(0.5+j0.8)MVA
STATCOM Reactive Power		j0.2274 MVA	j0.8316 MVA	j0.8705 MVA
dc Current Harmonic Base Value (I_{SCpeak})		500A	2000A	2000A
DC	0	0.215%	0.2%	0.019%
H1	fo	0.614%	3.55%	0.984%
H33	fc-9fo	7.91%	9.21%	9.64%
H39	fc-3fo	27.8%	10.1%	9.74%
H45	fc+3fo	27.8%	9.67%	10.4%
H51	fc+9fo	7.71%	9.36%	11.8%
H78	2fc-6fo	16.4%	24.1%	23.9%
H90	2fc+6fo	15.3%	22.8%	23.4%
H117	3fc-9fo	4.94%	2.88%	5.4%
H123	3fc-3fo	22.5%	0.89%	0.47%
H129	3fc+3fo	22.7%	0.72%	1.56%
H135	3fc+9fo	3.79%	3.52%	4.34%
H156	4fc-12fo	5.03%	7.95%	7.85%
H162	4fc-6fo	5%	5.28%	4.87%
H174	4fc-6fo	4.23%	4.61%	4.71%
H180	4fc+12fo	4.03%	6.76%	6.04%
H187	4fc+19fo	4.67%	6.27%	7.9%
H193	5fc-17f0	4.87%	6.01%	6.38%

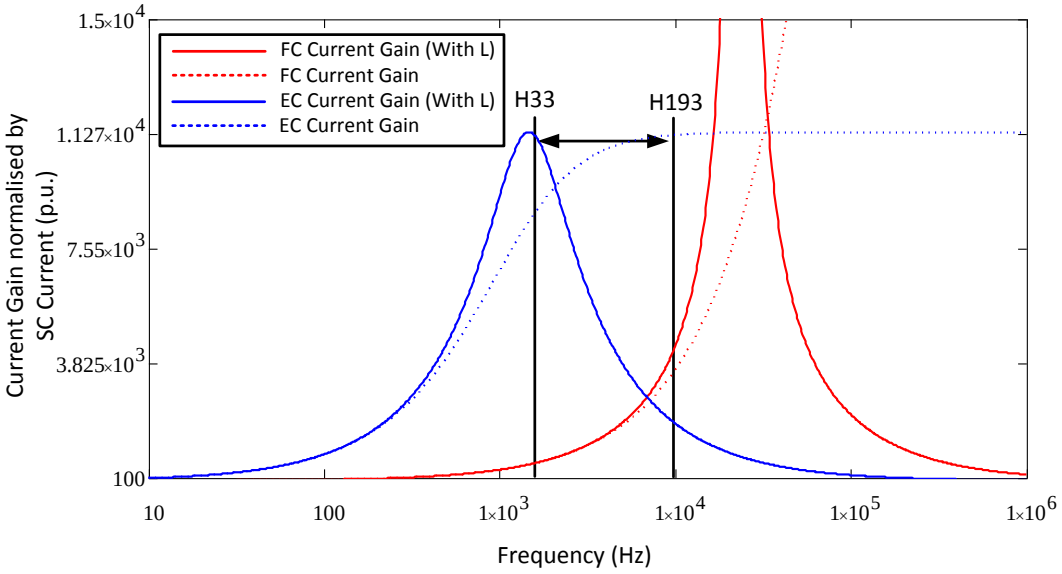


Figure 5.12 EC and FC Current Gain Normalised by SC Current.

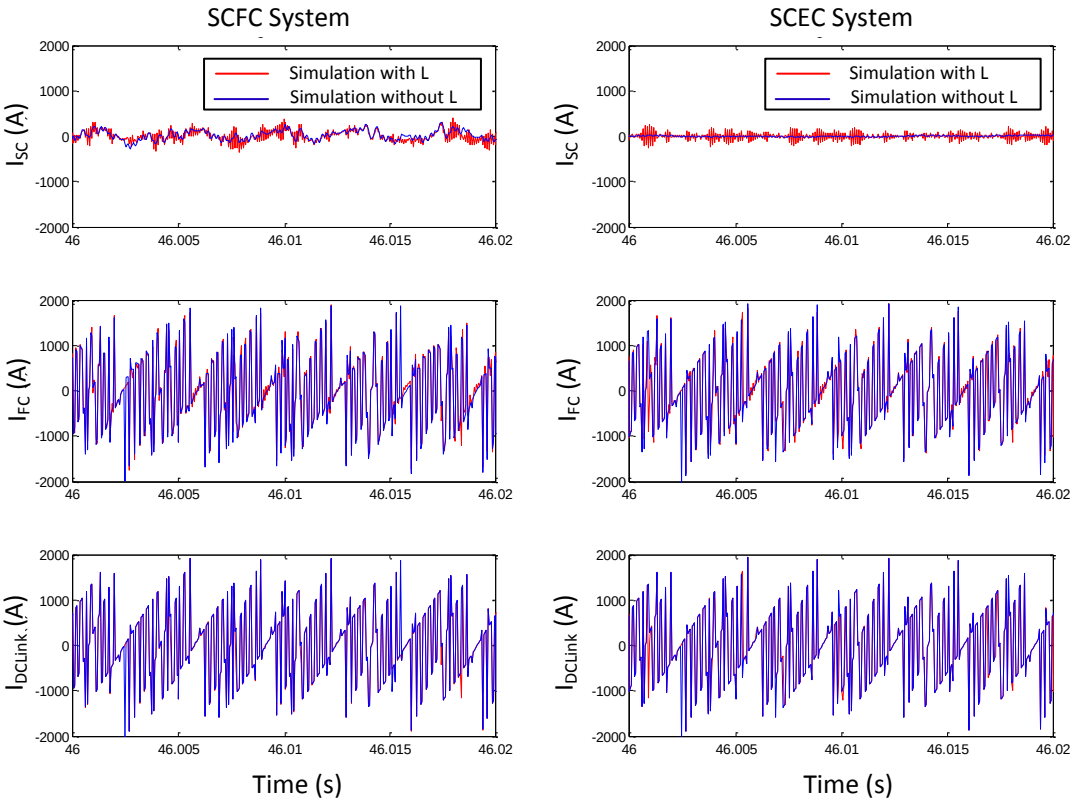


Figure 5.13 Current Simulation Compare for SCEC and SCFC System with and without Series Inductor at S_{L1} = (0.5+j0.8)MVA.

The current gain of EC and FC banks with and without series inductor are all above 100. Within the large amplitude harmonic range, which is H33 (1650Hz) to H193 (9650Hz), the EC and FC current magnitudes are much greater than the SC current. The SCEC and SCFC system with and without series inductor are simulated at rated load conditions, where the SC, EC and FC currents within the energy storage system are recorded.

Although the series inductor affects current gain values, due to the extremely high gain, the difference in currents shown in Figure 5.13 is small. As a result, the inductors are eliminated from the capacitor models to simplify the simulation. Based on the simulation results, the parallel EC or FC is able to carry the high frequency component, while the SC current is the dc component. It can be concluded that the parallel capacitor energy storage system improves life expectation, efficiency and volume, when compared to a SC-only system when operating under normal conditions.

5.2.3 DC Link Current Analysis Based on Mathematical Mode

The discontinuous three-phase input currents of the VSC are generated based on SPWM, and can be described by a mathematical model. The VSC output current is assumed a pure sinusoidal waveform. As shown in Figure 5.14, the single phase input current can be generated by the sinusoidal waveform from a mathematical transformation, and the SC output current is generated by combining the three-phase current.

The VSC single phase input current of the generation process is derived as follows:

1. Identify the SPWM voltage control reference V_a. Based on simulation, the modulation index m_{VSC} and the initial phase shift θ_{ps} can be obtained. The third-harmonic component is added, and the expression for V_a is:

$$V_a = m_{VSC} sin\left(2\pi \cdot f_0 \cdot t - \theta_{ps}\right) + \frac{1}{6} \cdot m_{VSC} sin(6\pi \cdot f_0 \cdot t - \theta_{ps}) \qquad \textbf{(5.12)}$$

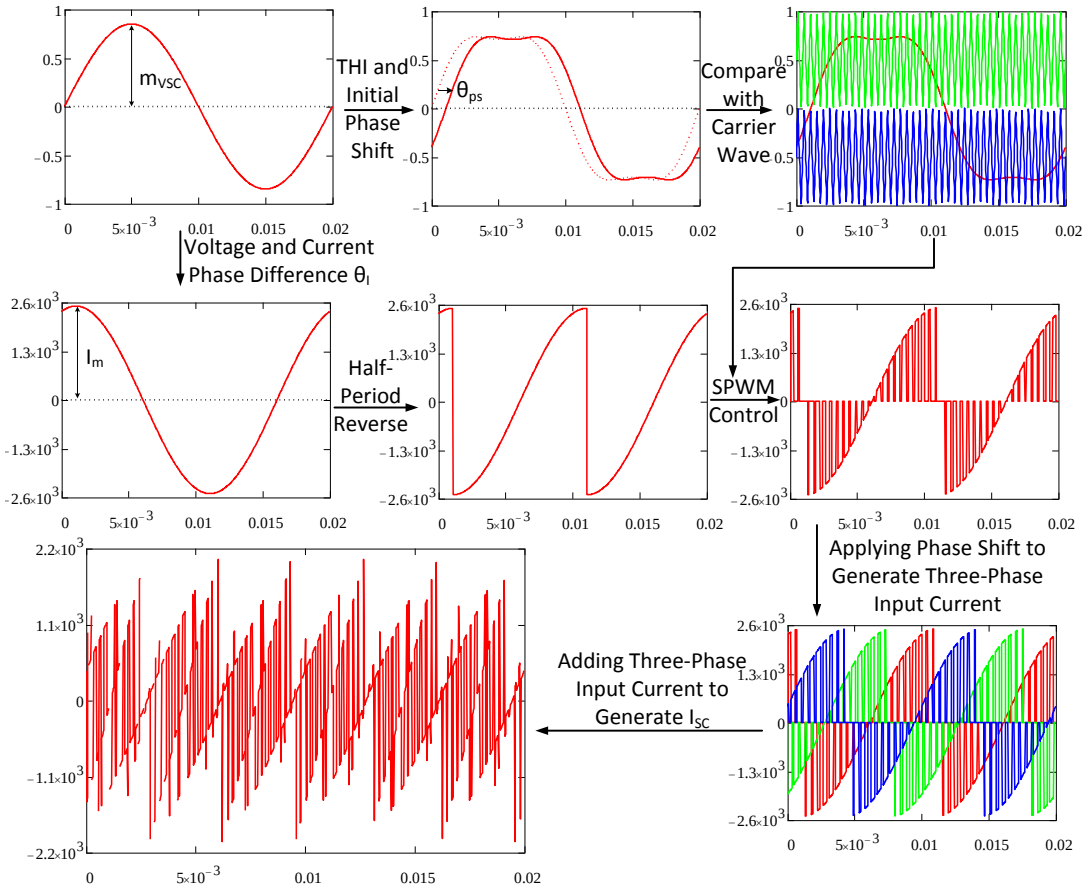


Figure 5.14 DC Link Current Generation Mathematical Model.

2. Identify the parameters for VSC single phase output current I_{VSCA}. The amplitude Im, and phase difference between the output voltage and current θ_{VI} can be obtained from the simulation, and the output current can be described as follows:

$$\begin{aligned} I_{VSCA}(t) &= Im \cdot sin\left(2\pi \cdot f_0 \cdot t - \theta_{ps} - \theta_{VI}\right) \\ &= Im \cdot sin(2\pi \cdot f_0 \cdot t - \theta_I) \end{aligned} \qquad \textbf{(5.13)}$$

where $\theta_I = \theta_{ps} + \theta_{VI}$

3. Half-period reverse the output current waveform $I_{VSCA}(t)$, and current base $I_{revA}(t)$ which is used for generating the discontinuous VSC input current is:

$$I_{revA}(t) = \begin{cases} Im \cdot sin(2\pi \cdot f_0 \cdot t - \theta_I), if\ \frac{T_0}{4} - \theta_I + n \cdot T_0 < t < \frac{3 \cdot T_0}{4} - \theta_I + n \cdot T_0 \\ -Im \cdot sin(2\pi \cdot f_0 \cdot t - \theta_I), otherwise \end{cases} \quad \textbf{(5.14)}$$

where n is the cycle number

4. Based on the SPWM control strategy, the discontinuous VSC input current I_{SCA} is:

$$I_{SCA}(t) = \begin{cases} 0, if\ \ V_{C2} < V_a < V_{C1} \\ I_{revA}(t), otherwise \end{cases}$$

V_{C1} and V_{C2} are the carrier wave, where

$$\begin{cases} V_{C1} = 0.5 \cdot (1 + \frac{\pi}{2} asin\ (sin\ (2\pi \cdot f_c \cdot t))) \\ V_{C2} = 0.5 \cdot (-1 + \frac{\pi}{2} asin\ (sin\ (2\pi \cdot f_c \cdot t))) \end{cases} \quad \textbf{(5.15)}$$

5. Based on the single phase current $I_{SCA}(t)$, the other two phase currents can be expressed by introducing $\frac{\pi}{3}$ and $\frac{2\pi}{3}$ phase shifts:

$$\begin{cases} I_{SCB}(t) = I_{SCA}(t - \frac{1}{3}T_0) \\ I_{SCC}(t) = I_{SCA}(t - \frac{2}{3}T_0) \end{cases} \quad \textbf{(5.16)}$$

By adding all three-phase currents, the SC output current is:

$$I_{SC}(t) = I_{SCA}(t) + I_{SCB}(t) + I_{SCC}(t) \quad \textbf{(5.17)}$$

Based on the mathematical model, the rms current rate, which defined as the ratio of the SC output current rms and the single phase current amplitude, varies as the modulation index changes. As shown in Figure 5.15, a maximum rms rate of 0.4 occurs at a modulation index of 0.59, while at high modulation indices (0.6~1.05), a minimum rms rate of 0.328 occurs at modulation index 0.91.

Based on the developed mathematical model, the SC rms output current can be estimated under different conditions. The simulated rms SC output currents at the light, medium and heavy load conditions shown in Table 5.5 are 256A, 794A and 830A, while the calculated rms values based on the mathematical model are 259A, 800A and 826A. As shown, the mathematical model and simulation results are

similar. Based on the current analysis, the associated power loss and thermal characteristics of the SC can be developed.

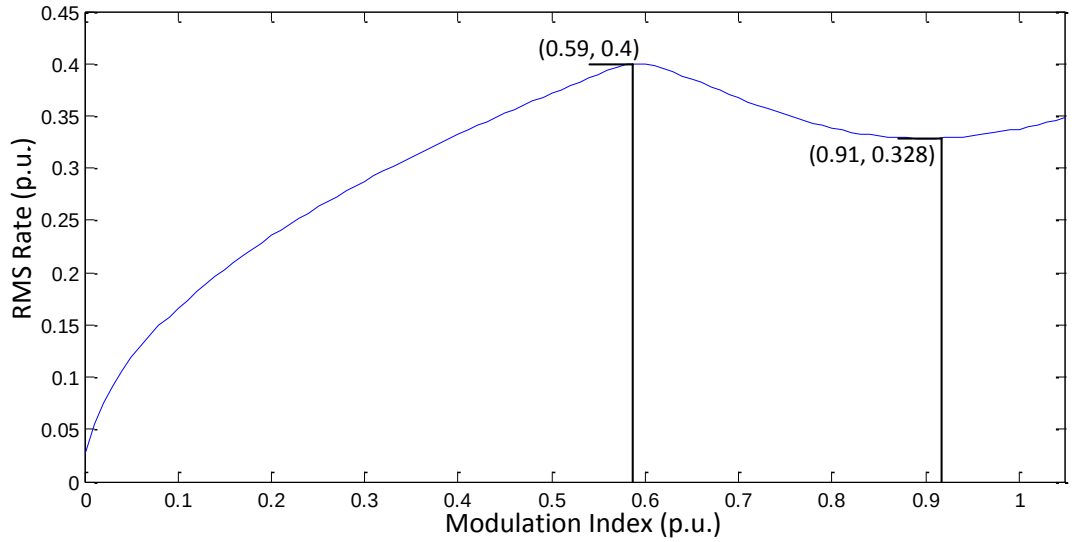


Figure 5.15 RMS Rate versus Modulation Index.

5.2.4 Power Loss Analysis

As the research focuses on the supercapacitor, the loss analysis refers to the energy loss within the SC energy storage system. For the SC based energy storage system, loss is generated by the SC internal resistance. Under normal conditions, the STATCOM generates reactive power to support the grid voltage, while in order to maintain the dc link voltage, a small amount of active power is absorbed to compensate the energy loss in the VSC and the energy storage system. Based on the SC rms output current, the loss power is:

$$P_{LosssC} = {I_{SCRMS}}^2 \cdot R_{SC} \quad \textbf{(5.18)}$$

Obviously, a higher rms current results in higher power loss in the SC energy storage system. For the parallel capacitor system, the power loss combines the EC or FC and SC losses. Under normal conditions, the parallel EC and FC banks carry the high frequency dc link current components and the SC rms current is much lower than for the purely SC system. As the EC and FC have a much lower resistance, the total power loss of the parallel system can be effectively reduced.

Table 5.6 Parallel Capacitor Energy Storage System Compare

	SC only System	SCFC System	SCEC System
total SC number	800	200	200
parallel SC string number	4	1	1
parallel FC number	0	11	0
parallel EC number	0	0	28
capacitance (F) (SC capacitance + parallel capacitance)	60 + 0	$15 + 9.9 \times 10^{-3}$	15 + 0.2352
resistance (mΩ) (SC resistance / parallel resistance)	14.5 / 0	58 / 0.1	58 / 0.511
rated voltage (V) (SC / parallel capacitor)	500 / 0	500 / 700	500 / 500
SC rms current (A)	830	109	13
parallel capacitor rms current (A)	0	826	828
dc link rms current (A)	830	835	835
SC power loss (W)	9989	700	10
parallel power loss (W)	0	68	350
total power loss (W)	9989	768	360
active power exchange (MW)	0.0322	0.0211	0.0207
reactive power exchange (MVAr)	0.87	0.868	0.868
energy storage system efficiency	69.0%	96.4%	98.3%
system capacitor volume ($\times 10^6 mm^3$)	322.4	91.6	118.7
Weight (kg)	408	114.43	148.424
per unit cost (p.u.)	2.60	0.752	1

The power loss analysis is based on rated conditions with the load S_{L1} = (0.5+j0.8)MVA. The power loss of the purely SC system is 9989W, while the absorbed active power and generated reactive power are 0.0322MW and 0.87MVAr. Assuming the efficiency of the energy storage system is defined as:

$$\eta_{SC} = \frac{P_{active} - P_{LossSC}}{P_{active}}$$

where P_{active} *is the active power exchange between the STATCOM and Grid* **(5.19)**

The SC energy storage system efficiency under rated conditions is 69.0%. Under same load conditions, the SCFC and SCEC systems, which are based on the system data shown in Table 5.4, are simulated and compared with the SC-only system.

According to the results in Table 5.6, the SC rms current is effectively reduced by using a parallel capacitor system, especially the EC system where the SC rms current is only 13A. Due to the decreased power loss within the energy storage system, the required active power, which is used to compensate the energy loss within the STATCOM for maintaining the dc link voltage, is reduced. The defined energy storage system efficiency is increased from 69% for the SC-only system to 98.3% for the SCEC system.

In order to link the SC characteristics in previous chapters, the SC current is scaled down to the SC single cell level. Assuming the capacitance and resistance of each SC cell within the SC bank are identical, the single cell SC current is:

$$I_{SCcell} = \frac{I_{SC}}{N_{SCp}}$$

where N_{SC} *is the number of parallel SC strings* **(5.20)**

Based on equation (5.20), the single cell SC rms current of the SC-only, SCEC and SCFC are 207.5A, 109A and 13A. The current stress on the single cell SC of the parallel capacitor systems is less than the SC-only system. In such cases, the efficiency, thermal performance (which is related to rms current squared), cost and life expectation of the supercapacitor are greatly improved.

5.2.5 Thermal Analysis

The thermal analysis is based on the thermal model introduced in Chapter 2. Using the thermal parameters in Table 5.1, the thermal characteristics are analysed for a single cell supercapacitor, with thermal resistance and capacitance of 3.2 ℃/W and 600J/ ℃. Under rated load conditions, the dc link current rms is 830A. For the SC-only system, different parallel number of the SC strings results in different currents in a single cell of supercapacitor bank. Based on equation (5.20) and the thermal model, the temperature change of the SC-only system with different parallel string number can be plotted in terms of time. Assuming the operating ambient temperature is 25 ℃, and the SC maximum operating temperature is 65 ℃, the allowed maximum temperature rise is 40 ℃.

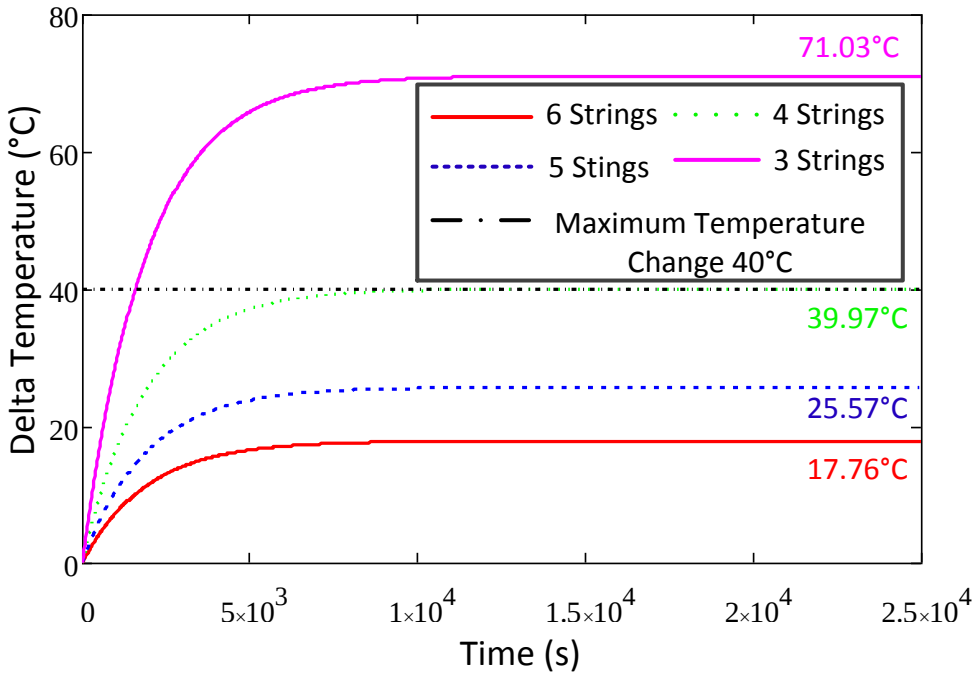


Figure 5.16 Temperature Change for SC only System with Different Number of Parallel Strings.

As the results show in Figure 5.16, the temperature rise of a single cell SC is reduced as the parallel number of the SC strings increases. The temperature rise of the SC-only system with four parallel strings is 39.97 ℃ which practically is the 40 ℃ cell limit, while the three string system exceeds the 40 ℃ limit by 31 ℃. Although the

four parallel strings SC system is within the SC operating range, the SC lifetime will be reduced as it operates at the maximum operating temperature.

According to this research on the parallel capacitor system, the SC rms current is significantly reduced as the high ripple component is carried by the parallel EC and FC banks. The reduced power loss results in a smaller temperature rise in the SCEC and SCFC systems. As the results show in Figure 5.17, the temperature rises for the SCEC and SCFC systems are 0.157 ℃ and 11.03 ℃, which has only one string of series supercapacitors. Compared to the four strings SC system, even though the parallel number is reduced, the temperature rise is much less. For such conditions, the lifetime of the SC string in the parallel capacitor system, is increased.

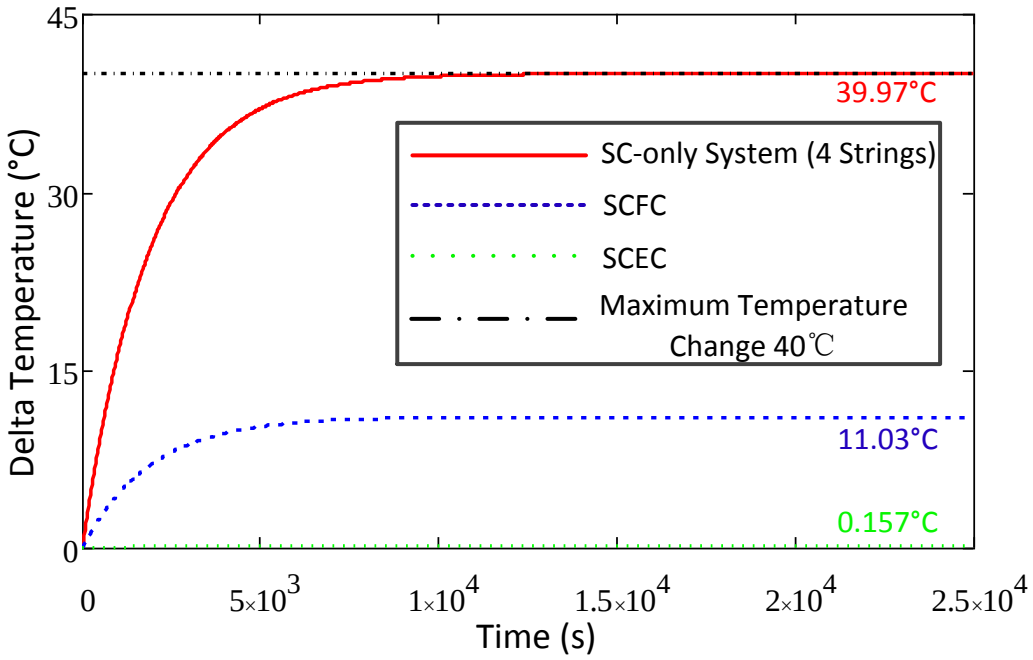


Figure 5.17 Temperature Change for Parallel Capacitor System.

As the EC is also sensitive to temperature, the temperature rise for a single EC cell under rated conditions is calculated. According to the EC data sheet, it is able to withstand an rms current of 31A at 85 ℃. As the maximum temperature is 105 ℃, the thermal resistance is estimated as 1.46 ℃/W. The power loss in the EC system under rated condition is 350W, which for a single EC cell is 12.5W. For such losses, the temperature rise of single cell EC can be estimated as 20.4 ℃, which is half that

of the SC-only system. Such a low core temperature rise affords an accept EC lifetime. Similarly, the temperature raise of the FC is 16.07 ℃, as its thermal resistance of 2.6 ℃/W with the cell power loss of 6.18W.

5.3 Supercapacitor Based STATCOM Transient Condition Analysis

The transient condition analysis for the STATCOM is simulated based on the same power system shown in Figure 5.7. Different transient conditions, including transient voltage (reactive power) support, transient active power support and fault ride-though capability, are simulated. The energy storage system based on SC only, SCEC and SCFC are compared in simulation to exam the ability of the STATCOM under different transient condition.

5.3.1 Transient Reactive Power Injection

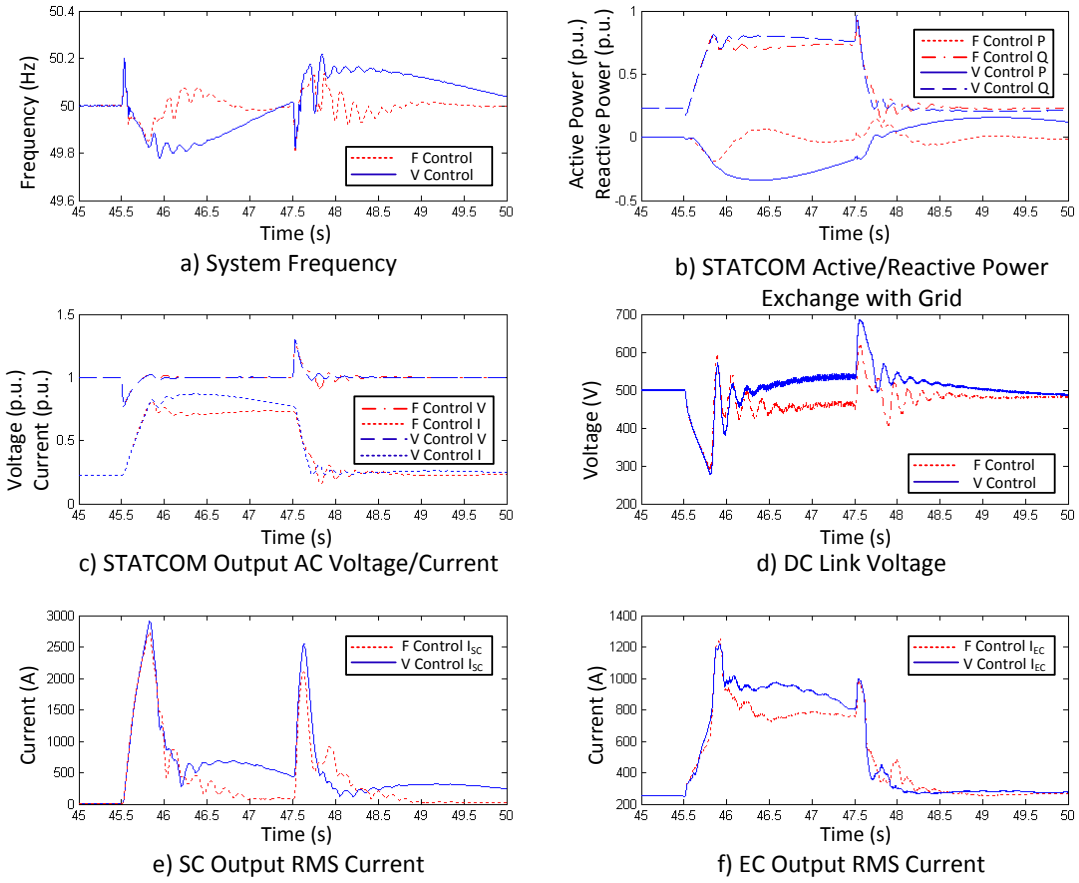


Figure 5.18 SCEC based STATCOM Transient Reactive Power Injection Performance.

The basic function of the STATCOM is to generate or absorb reactive power to maintain the load voltage. The transient voltage support capability is examined by switching in and out a reactive load, which is S_{L2} in Figure 5.7. Initially, the power system is at steady-state with load S_{L1} = (0.3 + j0.2)MVA, the load S_{L2} = (0 + j0.5)MVA is switched in and out at t = 45.5s and t = 47.5s respectively. Two control systems, namely conventional voltage control (V control) and the proposed frequency control (f control), are compared in simulation to evaluate the STATCOMs performance.

Figure 5.18 shows the transient performance of the SCEC based STATCOM during sudden reactive load change conditions. For both frequency and voltage control, the STATCOM has increased the reactive power generation as shown in Figure 5.18(b), while the voltage is maintained at 1.0 p.u. at the ac grid side, shown in Figure 5.18(c). Compare to voltage control, frequency control provides better frequency performance, with a response time 1s faster, as shown in Figure 5.18(a). The dc link voltage shown in Figure 5.18(d) has a large voltage spike at load change, which is mainly due to the resistor in the energy storage system model, while the large transient current can introduce large SC voltage changes. For the steady-state dc link voltage in Figure 5.18(d), the frequency control algorithm slightly adjusts the voltage reference to stabilise the system frequency, while the voltage control algorithm maintains the 500V reference. The high transient current from SC and EC during load switching shown in Figure 5.18(e) and (f), which may cause damage to the power switching devices.

For the same control strategy, the ac voltage responses for the STATCOM based on different energy storage systems are similar to the result in Figure 5.18(c). However, the system frequency response and current/voltage within the energy storage system with different capacitor combinations behave differently.

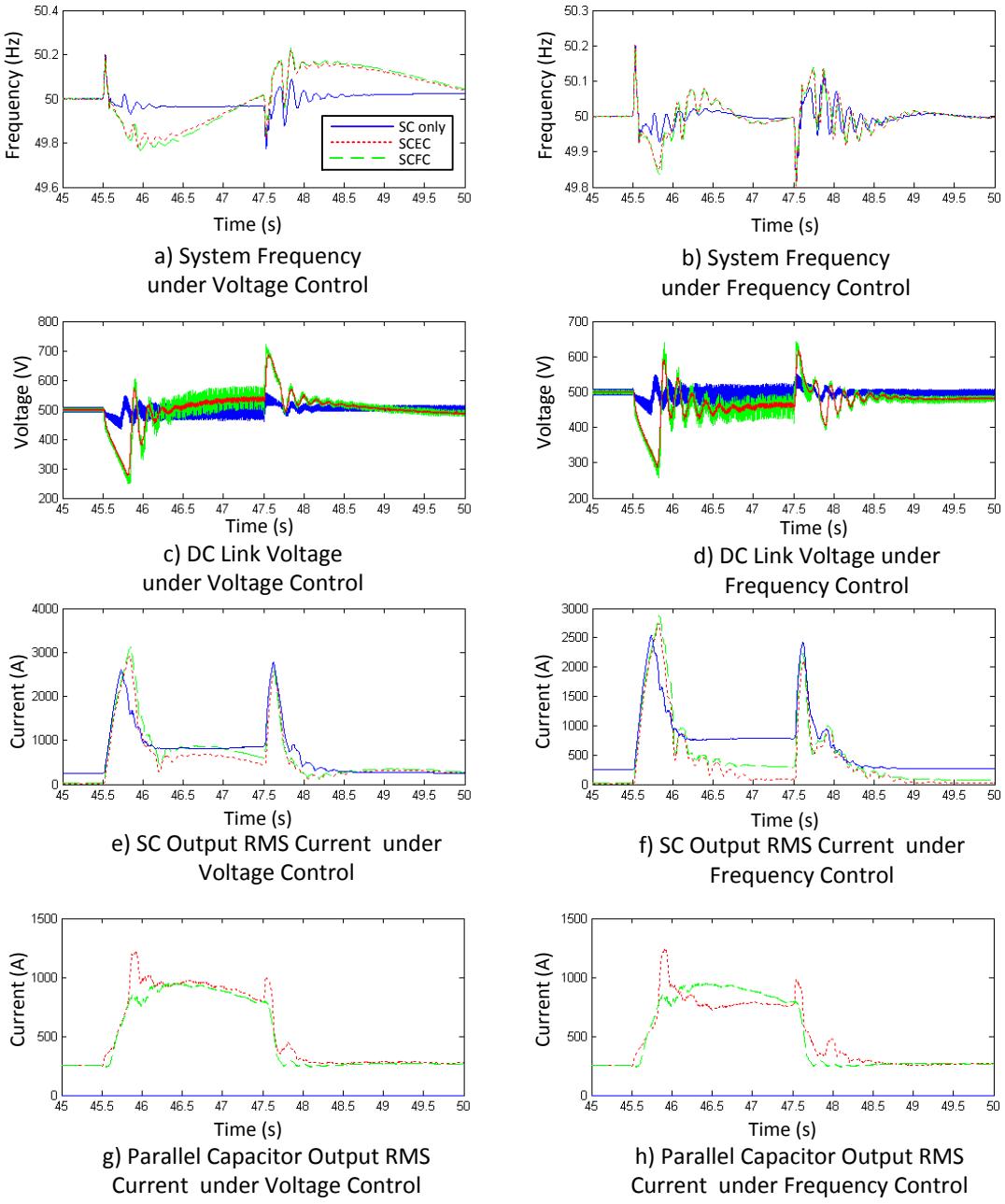


Figure 5.19 Energy Storage System Performance Compare for Transient Reactive Power Injection.

Figure 5.19 compares the SC-only, SCEC and SCFC energy storage systems, where the system frequency, capacitor voltage, SC current, and parallel capacitor current are shown. The dc link voltage in Figure 5.19(c) and (d), the SC-only system with four SC strings in parallel, is more stable due to the low internal resistance in the SC part, compared to the SCEC and SCFC system with one SC string. As a result, the

system frequency for the SC-only system is more stable under voltage control as shown in Figure 5.19(a), while the SCEC and SCFC systems can reach similar performance under frequency control, as shown in Figure 5.19(b). The transient SC output current of the SCEC system is smaller than that of the SCFC system, as shown in Figure 5.19(e) and (f), where the EC high capacitance is able to share the transient current to reduce the current SC stress. The SCFC system, which has a higher operating frequency range than the SCEC system, can only reduce the high frequency ripple current as shown in Figure 5.19(g) and (h).

As shown in the simulations, the SC based STATCOM is capable of supporting reactive power to maintain the ac grid voltage during transient conditions. The ac voltage response for both voltage and frequency control are similar, while frequency control has better performance when stabilising the system frequency. For the energy storage system, the SC-only system has a more stable dc link voltage due to the increased parallel bank number. Both the SCEC and SCFC systems can filter the high frequency ripple current. However, due to the higher capacitance of EC bank, the SCEC system is able to reduce the current stress on the SC during transient conditions.

5.3.2 Transient Active Power Injection

As the SC based STATCOM aims to provide transient active power support, an active load is switched in for a short period, and the SC energy storage system provides active power to stabilise the system frequency. As the active load is switched in or out, the system frequency changes due to the power mismatch, and the STATCOM adjusts the dc link voltage to sink or source active power to support the frequency, which has a faster response than the generator. Similarly to reactive power injection, the power system is at steady state with load S_{L1} = (0.3 + j0.2)MVA initially, while the switch load is S_{L2} = (0.5 + j0.2)MVA**,** switched in and out at t = 45.5s and t = 46.5s respectively. The voltage and frequency control algorithms are compared in simulation to evaluate the performance of the SC-only, SCEC and SCFC based STATCOMs.

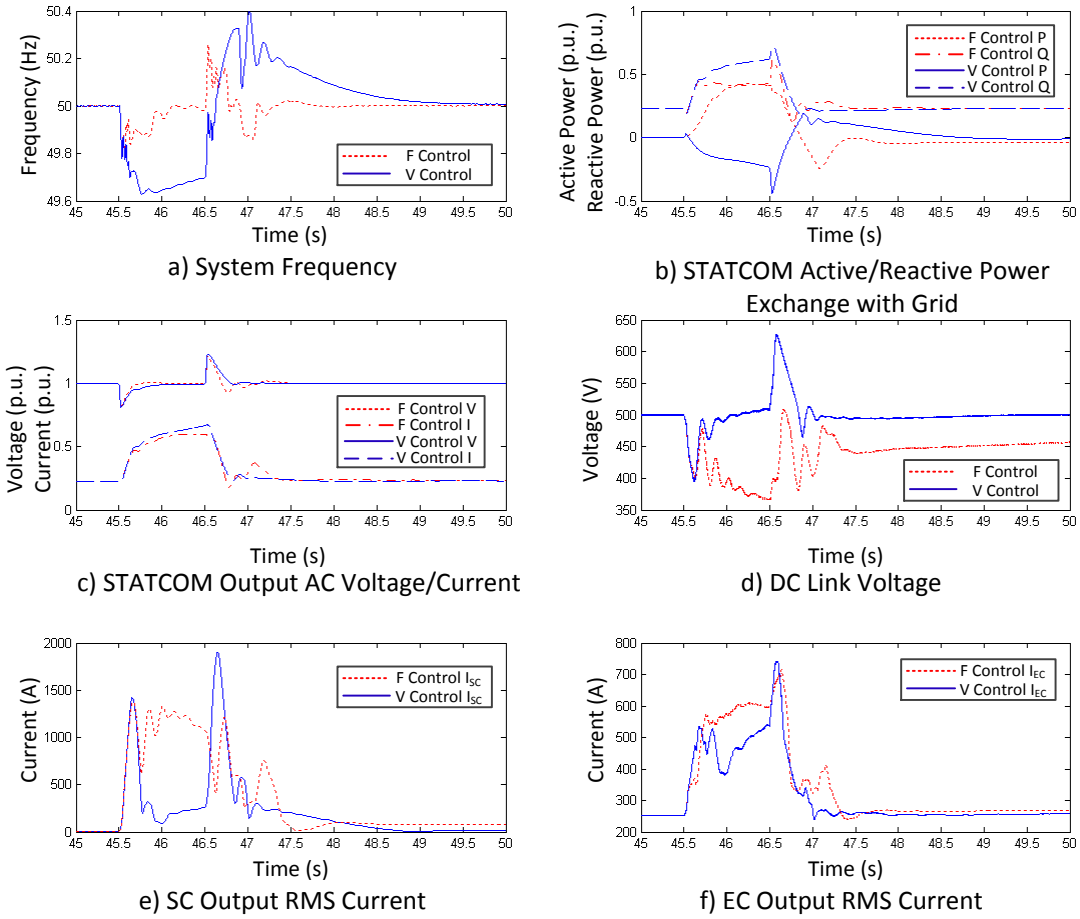


Figure 5.20 SCEC based STATCOM Transient Active Power Injection Performance.

Figure 5.20 shows the transient performance of the SCEC based STATCOM during active load switching. Compare to voltage control, frequency control can manipulate the active power, with the system frequency recovering to 50Hz within 0.5s, while the voltage control operates under frequency during the whole period load of the load switched in. As shown in Figure 5.20(b), frequency control generates active power to support the frequency, while voltage control absorbs active power to maintain the DC link voltage. In Figure 5.20(c), both frequency and voltage control can recover the ac grid voltage during load change. However, since the frequency control algorithm provides active power support, it also improves the ac voltage response time. Similarly, the dc link voltage still has the large voltage spike during load switching as shown in Figure 5.20(d). For steady-state dc link voltage, the frequency control discharges to near the low dc link voltage limit (350V) to generate active

power, while the voltage control algorithm maintains the 500V reference. The high transient current from the SC and EC during load switching shown in Figure 5.20(e) and (f) causes the large voltage spike across the internal resistor of the SC model, where more SCs may be connected in series or parallel to reduce the voltage variation.

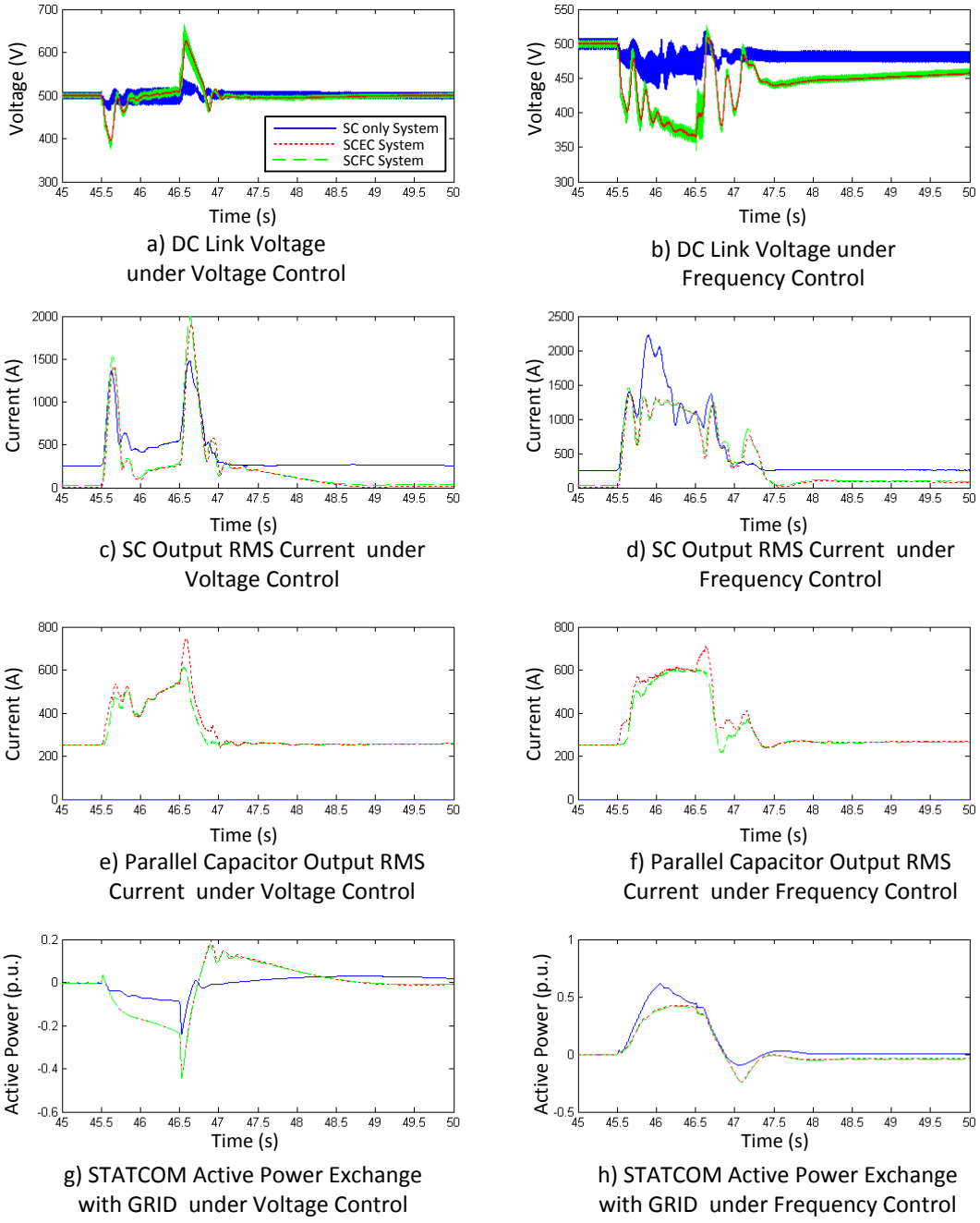


Figure 5.21 Energy Storage System Performance Compare for Transient Active Power Injection.

Performance of the different energy storage system is shown in Figure 5.21. For the dc link voltage in Figure 5.21(a) and (b), the large voltage spike only appears in the SCEC and SCFC systems, which have only one SC string. Due to the four parallel SC strings, the SC-only system has a much smaller equivalent internal resistance and less energy loss, which effectively reduces the voltage spike during the transient condition. The increased SC parallel number of the SC-only system stores more energy within same voltage range than the other systems, where the SC-only system only discharges 40V to achieve the same performance as the SCEC and SCFC systems which discharge by 150V. With voltage control, the SCEC and SCFC systems absorb more energy to recover the dc link voltage as shown in Figure 5.21(g), and for frequency control, the SC-only system provides more active power to stabilise the system frequency, as shown in Figure 5.21(h). The parallel EC and FC currents behave similar to the reactive load switch condition in Figure 5.21(e) and (f).

As the simulations show, the SC based STATCOM is able to generate and absorb active power to stabilise the system frequency for sudden active load changes. Frequency control provides better performance for frequency stabilisation and ac voltage response time, compared to the voltage control. The energy storage systems based on the different capacitors show similar characteristic as the switched reactive load cases.

5.3.3 Transient Performance during Fault Condition

STATCOM transient performance during fault conditions is examined by applying a three-phase fault 5km from the generator, as shown in Figure 5.7. The fault occurs at t = 45.5s and cleared at t = 45.64s (140ms fault). STATCOMs based on the SC-only, SCEC and SCFC are simulated with both voltage and frequency control algorithms.

Figure 5.22 shows the simulation results of the SCEC based STATCOM during the fault condition. The STATCOM using both control algorithms can recover the ac grid voltage as the fault is cleared, as shown in Figure 5.22(c). The frequency responses are similar, and recover quickly due the small active power variation, as shown in Figure 5.22(a). The dc link voltage for frequency control slightly increases

to adjust the system frequency, while the voltage with voltage control recovers to its previous steady-state within 1.5s, as shown in Figure 5.22(d). The SC and EC current with both controllers shows similar behaviour during the transient condition, while the SC current for frequency control charges the dc link voltage to the reference as shown in Figure 5.22(e) and (f).

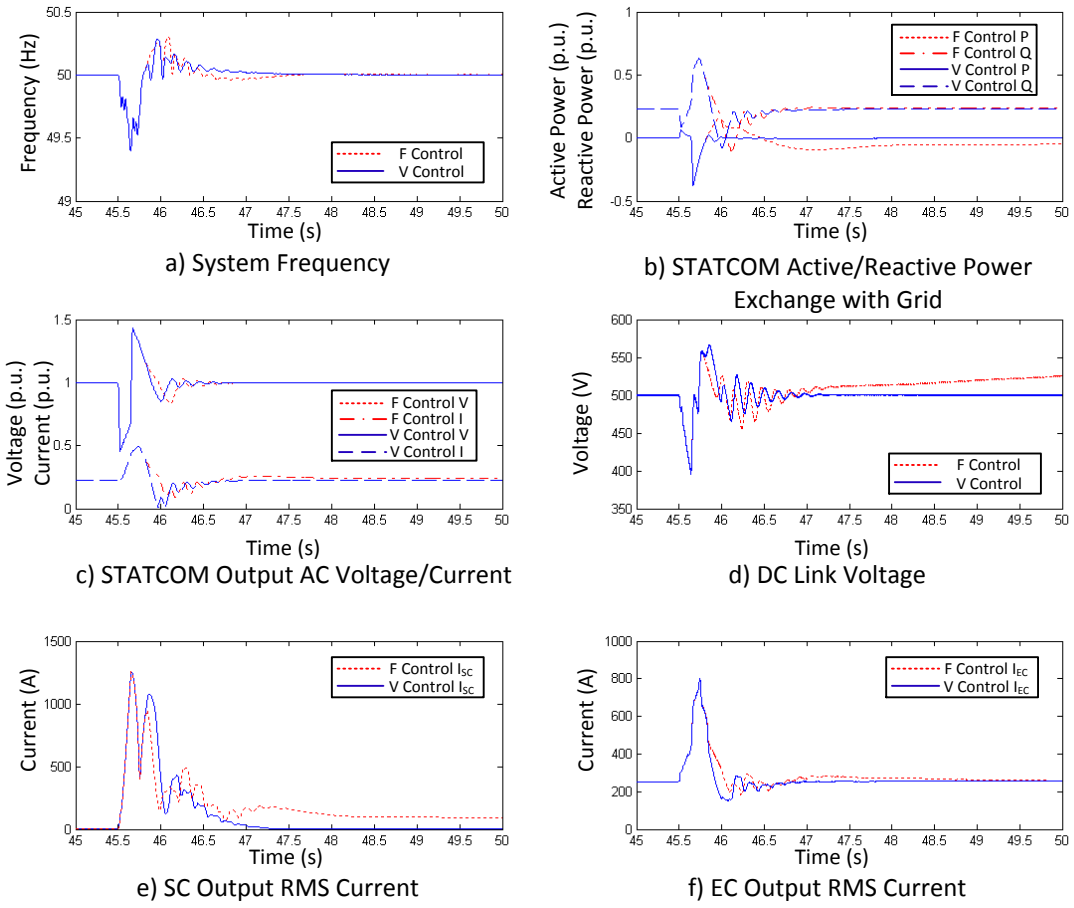


Figure 5.22 SCEC based STATCOM Transient AC Fault Ride-Though Performance.

Figure 5.23 compares the behaviour of the different energy storage systems. Similarly, the SC-only system has a more stabilised dc link voltage, as shown in Figure 5.23(a) and (b). The transient SC output current of the SCEC system is smaller than the other two systems, as shown in Figure 5.23(c) and (d), since the EC bank takes more transient current, as shown in Figure 5.23(e) and (f).

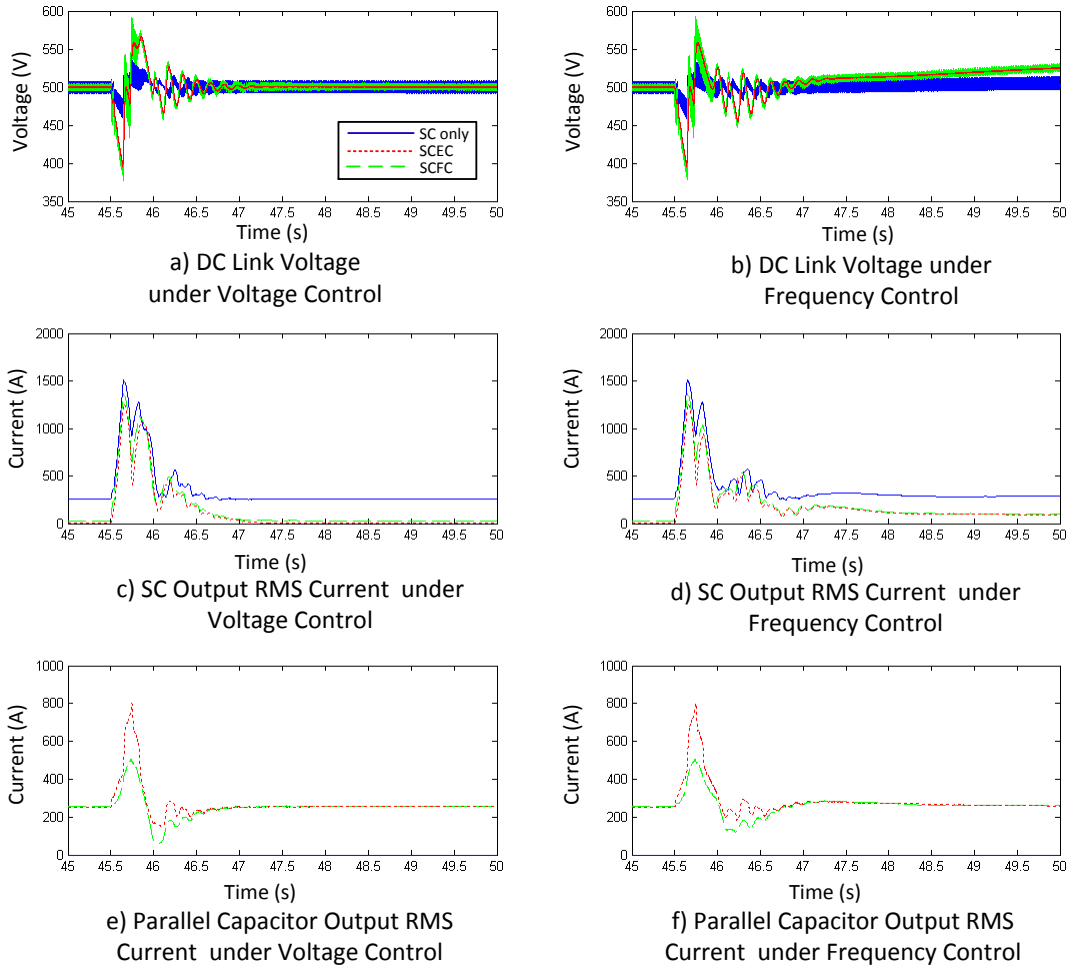


Figure 5.23 Energy Storage System Performance Compare for Transient AC Fault Ride-Though.

The simulations show that the SC based STATCOM is able to tolerate the three-phase fault, and recover the ac grid voltage. Both control algorithms provide similar performance during the fault ride-through condition. The increased SC parallel number is able to provide a better stabilised dc link voltage. Similar parallel capacitor current characteristics are observed during transient and steady-state conditions.

5.4 Feasibility Analysis

The SC based STATCOM has been developed and verified in simulation. It is not only able to provide basic STATCOM functionality in generating/absorbing reactive power to support ac grid voltage, but also has active power capability to stabilise system frequency. The feasibility analysis of applying a SC based STATCOM is discussed in both normal and transient conditions. Different SC based energy storage systems, including SC-only, SCEC and SCFC, were connected to the STATCOM to compare system performance.

Under normal conditions, the STATCOM generates rated reactive power to maintain grid voltage. The simulation results shows that, even at steady-state, the dc link has a high ripple current, 830A rms. For available SCs, the maximum current rating is 210A, so SC parallel connection is required. However, due to the SC low single cell voltage limit of 2.7V, at least 200 SCs have to be connected in series to achieve the 500V dc link requirement. As a result, the SC-only system requires a large number of SCs, operating at maximum current ratings. Based on FFT analysis, the large amplitude harmonics in the ripple current are at high frequency. The SCEC and SCFC systems, where the EC and FC operate at a higher frequency range than the SC, filter the high frequency component to reduce SC stresses. According to the simulation results, the SC rms current of the two hybrid capacitor systems has been effectively reduced, with only one SC string sufficient to withstand the ripple current. As a result, system volume, power loss, efficiency, temperature performance, cost and life expectation can be improved by using the hybrid parallel capacitor system.

For transient conditions, reactive/active power injection and fault conditions were simulated to exam the performance of STATCOM with SC-only, SCEC and SCFC energy storage systems. Two control algorithms, conventional voltage control and proposed frequency control, are compared. Based on the simulation results, a STATCOM based on the different energy storage systems can recover ac grid voltage under both control algorithms. Frequency control provides a better performance in stabilising the system frequency than the voltage control, especially during active load switching. The SC-only system has a more stable dc link voltage

due to its large capacitance of four parallel SC strings. For the parallel hybrid capacitor systems, due to capacitor different operation frequency ranges, the EC shares the transient dc current variation to reduce the SC output current, while the FC can only filter the high frequency component of the ripple current. A large voltage spike is observed for the parallel capacitor systems which have one SC string. Due to the large equivalent resistance of the SC bank, the current change during the transient condition results in a large voltage variation. In such conditions, more SCs may be required to better control the voltage spike.

The feasibility analysis shows a positive bias for using the SC as the energy storage system for a STATCOM to provide active power. The proposed SC based STATCOM has a similar topology as the conventional STATCOM, with the capacitor bank replaced by the SC based energy storage system. As shown in the simulations, the proposed SC based STATCOM holds the same reactive power capability as the conventional system, and also is able to generate or absorb active power to stabilise the system frequency. The SCEC and SCFC hybrid systems can filter the high frequency, large amplitude ripple current to improve the energy storage system performance during normal conditions, while the SCEC system also shares the transient dc current between the SC and EC, to improve the transient performance. However, due to the voltage limitations of the SC, SCs have to be connected in series, where voltage balancing problems could limit its extension to high voltage.

5.5 Summary

The proposed SC based STATCOM aims to provide both active and reactive power control functionality. The topology and control algorithms of the STATCOM were introduced. The energy storage system with different parallel capacitor systems, including SCEC and SCFC configurations, were developed and performance compared with the SC-only storage system. The STATCOM has been developed in simulation with a test power system to exam its performance in both steady-state and transient conditions. For steady-state condition, two analysis methods, FFT and mathematical model, were introduced for analysing the dc link current, which then allows power loss, efficiency and thermal analysis. For the transient condition, a

sudden active/reactive load change and three-phase fault condition were simulated based on both voltage and frequency control algorithms for three SC based energy storage systems. With the aid of the simulation results, the feasibility analysis shows that the SC based STATCOM is suitable for medium and low voltage applications.

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Chapter 6

6 Conclusion

Due to its unique double-layer structure and electrostatic charge mechanism, the supercapacitor (SC) is able to fill the gap between conventional batteries and capacitors in respect to specific energy and power capability. Its advantages in energy density, power density, cycle life, and temperature range enable a wide application range at different power levels. However, its low cell voltage and high series resistance limit application at the grid level. Motivated by these SC limitations, this thesis proposed a solution for applying the SC as the energy storage system for high voltage and power applications, which improves system performance in terms of efficiency, power capability, temperature, and volume. In this chapter, the general conclusion, contributions and future research suggestions are presented.

6.1 General Conclusion

The thesis provides a general view of SCs in Chapter 1. By comparison with the conventional battery and capacitor, SC advantages and limitations are stressed for applications at different power level. Internal resistance resultant limitations, mathematical models for SC operating at different conditions, including constant current, constant power and triangle wave current, are developed and verified by simulation and experiment in Chapter 2. The result shows that the SC can be inefficient under high current/power conditions, where a higher temperature rise is observed, based on the developed SC thermal model at higher current/power conditions.

Chapter 3 reviews different SC models in terms of model topology and parameter identification method. A complex model topology normally requires development of a complex parameter identification method, while the accuracy varies for the SC operating at different conditions. Based on the two branch and variable capacitance topologies, two novel parameter identification methods were proposed, both realised with a simple experimental method with an acceptable accuracy.

In order to improve SC based energy system performance in high-power short-duration (<1s) applications, a parallel capacitor system (termed SCEC) with an electrolytic capacitor (EC) connected in parallel with the SC is proposed in Chapter 4. As established, the SCEC system improves the efficiency in transient conditions by over 10% when compared to SC-only system. Mathematical modelling, simulation and experimentation verify the improvement in efficiency, power capability and response time gained with the SCEC approach. Parameters, which affect SCEC system efficiency, were analysed based on the mathematical model, and experimentally verified, while the efficiency is increased by decreased discharge current, decreased discharge time, decreased SC and EC resistance, increased initial discharge voltage, and increased capacitance ratio. The SCEC system design guide was presented with a practical design example. Frequency analysis, based on a mathematical model, was presented to complete SCEC system performance assessment, and extended to three branches with inductance effects included.

Chapter 5 demonstrated a SC energy storage system for grid level application. A SC based STATCOM was proposed to provide both active and reactive power control functionality, where the topology and control algorithms were introduced. Three SC based energy storage systems, including SC-only, SCEC and SCFC configurations, were developed to replace the conventional dc capacitor on the STATCOM dc link. A test power system was developed in simulation to exam STATCOM performance with different SC energy storage systems under both steady-state and transient conditions.

For steady-state conditions, FFT and mathematical methods were adopted to analyse the dc link current. The SCEC and SCFC systems were able to effectively reduce SC rms current stress, with only one SC string being sufficient to withstand the dc link ripple current. As a result, system volume, power loss, efficiency, temperature performance, cost and life expectation can be improved by using the proposed hybrid parallel capacitor system.

For the transient conditions, a STATCOM based on both voltage and frequency control algorithms was simulated under sudden active/reactive load change and three-phase fault conditions. For all three SC energy storage systems, both control

algorithms can recover the ac grid voltage, while better performance in stabilising the system frequency was achieved by frequency control, especially during active load switching. Due to its large capacitance, the SC-only system has a more stable dc link voltage. For the parallel hybrid capacitor systems, EC shared the transient dc current to reduce the SC current stress, while FC only filtered the high frequency ripple current component. The feasibility analysis shows that a SC based STATCOM is suitable for medium and low voltage applications.

6.2 Author's Contribution

This thesis is concerned with applying SC based energy storage systems in high power applications. The thesis contributions can be summarised as follows:

- Development of SC mathematical models under different conditions, including constant current, constant power and triangle wave current, enables fast performance estimation of SC based energy storage systems.
- Based on the SC model reviews, two novel parameter identification methods were developed for the two branch and variable capacitance topologies. With a simple SC RC discharge experiment, the two methods yield parameter values, with acceptable accuracy.
- The proposed SCEC system enables improvement in efficiency, power capability, system volume, cost, and thermal performance compared to the SC-only system.
- The mathematical model of the SCEC system was developed for characteristic analysis. SCEC system efficiency characteristics were concluded, while methods for increasing system efficiency were stressed. The model can be extended to other parallel connected capacitor systems using the two branch topology.
- A general design guide for the SCEC system was presented, which aims to achieve optimal system design in terms of efficiency, power capability, cost, and volume.

- Mathematical model for frequency analysis of a three branch system was developed with consideration of inductance effects, which can be applied for systems with three RC branches in parallel.
- A SC based STATCOM was developed on conventional topology by replacing the dc link capacitor with various SC based energy storage systems. Compared with conventional voltage control, frequency control was employed to provide active power functionality for system frequency stabilisation.
- DC link current analysis, mathematical model, and FFT methods were demonstrated and these enable fast STATCOM performance estimation under normal conditions, including power losses, efficiency, and thermal effects.
- During normal conditions, the proposed parallel capacitor systems, SCEC and SCFC, both provided better performance in efficiency, thermal, system volume, and life expectation than the SC-only system.
- STATCOM transient performance comparison with both control algorithms based on different SC based energy storage systems were presented.
- Feasibility analysis of applying SCs in energy storage STATCOM systems was discussed in terms of both steady-state and transient performance.

6.3 Suggestions for Future Research

The research undertaken in this thesis stressed the limitations of using the SC in high power applications, while viable solutions were presented to improve the SC based energy storage system performance. Several suggestions for future research are proposed.

- SC balancing problems. As large number of SCs are connected either in series or/and parallel in high power applications, unbalanced voltage, current and temperature on single cell or multiple cells can cause damage to the system.
- Integration of the parallel capacitor system with a primary energy storage system, such as a battery and/or fuel cell.

- A dc/dc converter can be applied together with the SC to provide active power support for a STATCOM. Comparison of such a topology when directly supplying the dc link SC capacitor in this thesis, can be useful for STATCOM system design.

Appendix A

Model Derivation

In this section, derivations of two branch supercapacitor (SC) mathematical models under RC discharge and constant current conditions are presented.

A.1 Two Branch RC Discharge Model

The SC two branch model is employed, using the novel parameter identification method in Chapter 3, where the mathematical model derivation is as follows.

As the SC is discharged by a resistor, the circuit diagram is shown in Figure A. 1.

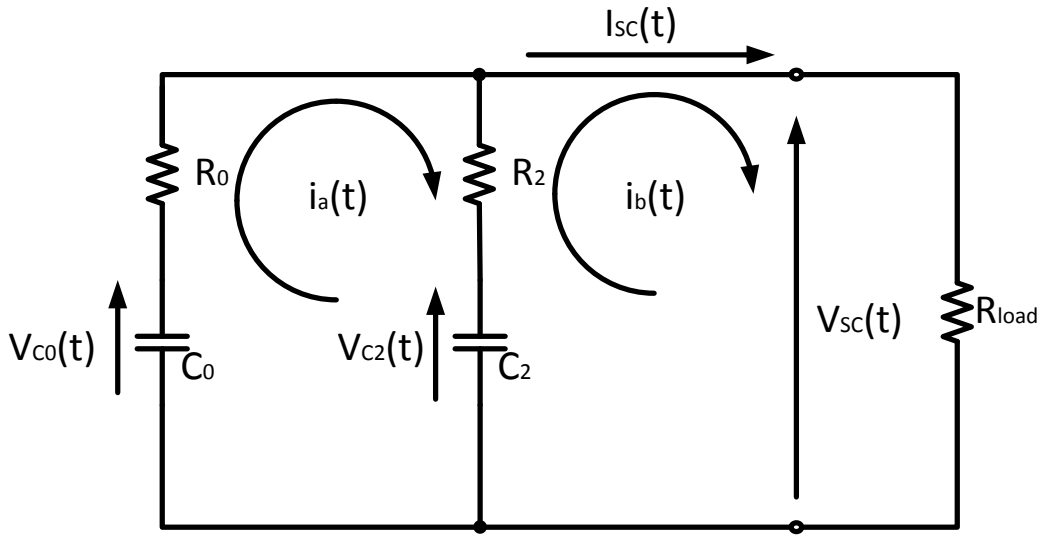

Figure A. 1 Two Branch RC Discharge Mathematical Model.

By taking Laplace transforms, the original circuit is transferred to the complex domain to obtain the SC output current expression.

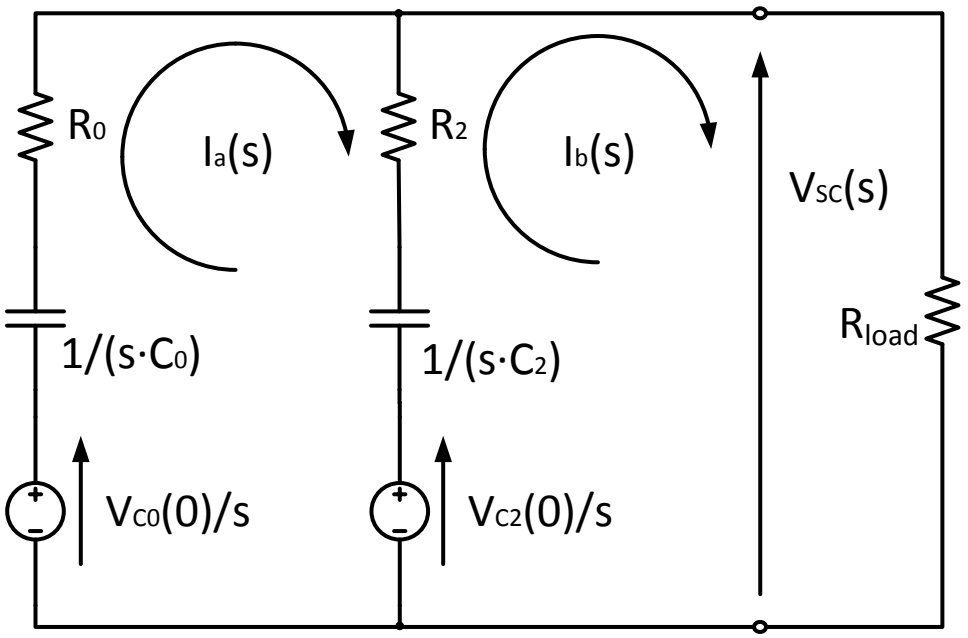

Figure A. 2 Two Branch RC Discharge Complex Domain.

By KVL, the following equations are developed:

$$\begin{cases} \left(R_0 + \frac{1}{s \cdot C_0} + R_2 + \frac{1}{s \cdot C_2}\right) \cdot I_a(s) - \left(R_2 + \frac{1}{s \cdot C_2}\right) \cdot I_b(s) = \frac{V_{c0}(0) - V_{c2}(0)}{s} \\ -\left(R_2 + \frac{1}{s \cdot C_2}\right) \cdot I_a(s) + \left(R_2 + \frac{1}{s \cdot C_2} + R_{load}\right) \cdot I_b(s) = \frac{V_{c2}(0)}{s} \end{cases}$$

By solving above equations, $I_a(s)$ is solved as:

$$I_a(s) = \frac{N(s)}{D(s)} = \frac{A \cdot s + B}{C \cdot s^2 + D \cdot s + E}$$

where

$$\begin{aligned} A_a &= C_0 \cdot (V_{c0} \cdot R_2 \cdot C_2 + V_{c0} \cdot R_{Load} \cdot C_2 - V_{c2} \cdot R_{Load} \cdot C_2) \\ B_a &= C_0 \cdot V_{c0} \\ C_a &= R_0 \cdot C_0 \cdot R_2 \cdot R_{Load} + R_0 \cdot C_0 \cdot C_2 \cdot R_2 + R_2 \cdot C_0 \cdot C_2 \cdot R_{Load} \\ D_a &= R_0 \cdot C_0 + R_2 \cdot C_2 + R_{Load} \cdot C_2 + C_0 \cdot R_{Load} \\ E_a &= 1 \end{aligned} \quad \textbf{(A. 1)}$$

Taking inverse Laplace transform for (A. 1), let $D(s) = C_a \cdot s^2 + D_a \cdot s + E_a = 0$, two roots of *D(s)* can be calculated as:

$$p_{a1} = \frac{-D_a + \sqrt{{D_a}^2 - 4C_a \cdot E_a}}{2C_a}$$

$$p_{a2} = \frac{-D_a - \sqrt{{D_a}^2 - 4C_a \cdot E_a}}{2C_a}$$

Time domain coefficient Ka_1 and Ka_2 are

$$K_{a1} = \frac{N(S)}{D^*(S)}\Big|_{S=p_{a1}} = \frac{A_a \cdot p_{a1} + B_a}{2C_a \cdot p_{a1} + D_a}$$

$$K_{a2} = \frac{N(S)}{D^*(S)}\Big|_{S=p_{a2}} = \frac{A_a \cdot p_{a2} + B_a}{2C_a \cdot p_{a2} + D_a}$$

By taking inverse Laplace transform for $I_a(s)$, the time domain expression is

$$i_a(t) = K_{a1} \cdot e^{p_{a1} \cdot t} + K_{a2} \cdot e^{p_{a2} \cdot t} \quad \textbf{(A. 2)}$$

Similarly, the time domain expression for $I_b(t)$ is

$$I_b(t) = K_{b1} \cdot e^{p_{b1} \cdot t} + K_{b2} \cdot e^{p_{b2} \cdot t}$$

where

$$p_{b1} = \frac{-D_b + \sqrt{{D_b}^2 - 4C_b}}{2C_b}, p_{b2} = \frac{-D_b - \sqrt{{D_b}^2 - 4C_b}}{2C_b}$$

$$K_{b1} = \frac{N(S)}{D^*(S)}\Big|_{S=p_{b1}} = \frac{A_b \cdot p_{b1} + B_b}{2C_b \cdot p_{a1} + D_b},$$

$$K_{b2} = \frac{N(S)}{D^*(S)}\Big|_{S=p_{b2}} = \frac{A_b \cdot p_{b2} + B_b}{2C_b \cdot p_{b2} + D_b} \quad \textbf{(A. 3)}$$

with

$$A_b = C_0 \cdot V_{C0}(0) \cdot R_2 \cdot C_2 + R_0 \cdot C_0 \cdot C_2 \cdot V_{C2}(0),$$

$$B_b = C_0 \cdot V_{C0}(0) + C_2 \cdot V_{C2}(0),$$

$$C_b = R_0 \cdot C_0 \cdot C_2 \cdot R_{load} + R_0 \cdot C_0 \cdot C_2 \cdot R_2 + R_2 \cdot C_0 \cdot C_2 \cdot R_{load},$$

$$D_b = R_0 \cdot C_0 + R_2 \cdot C_2 + R_{load} \cdot C_2 + C_0 \cdot R_{load}$$

A.2 Two Branch Constant Current Discharge Model

The SCEC system mathematical model is developed on the two branch model discharged by a constant current source in Chapter 4.

As the circuit diagram shown in Figure A. 1, similar method as the RC discharge model is applied.

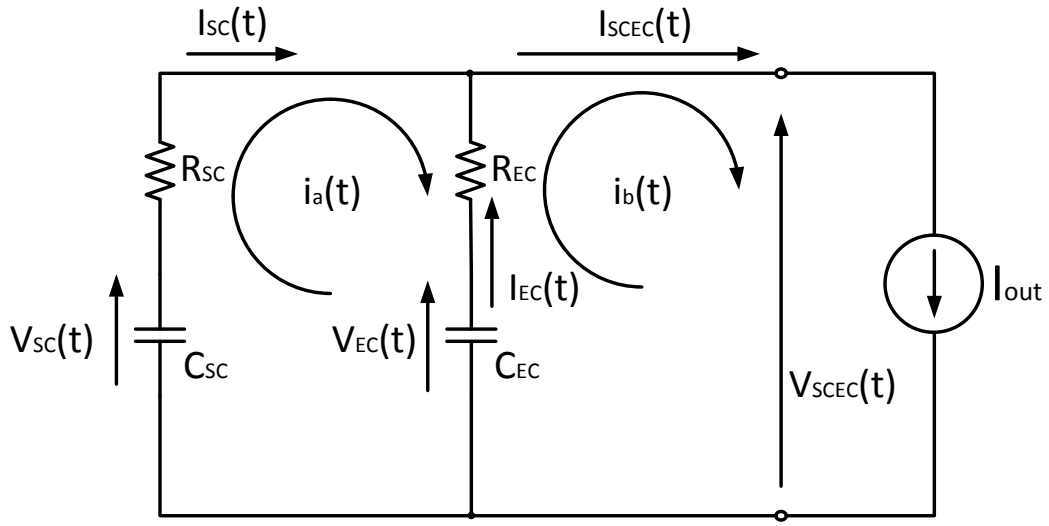

Figure A. 3 SCEC Constant Current Discharge Model.

By taking Laplace transform, the original circuit is transferred to complex domain to obtain the SC output current expression.

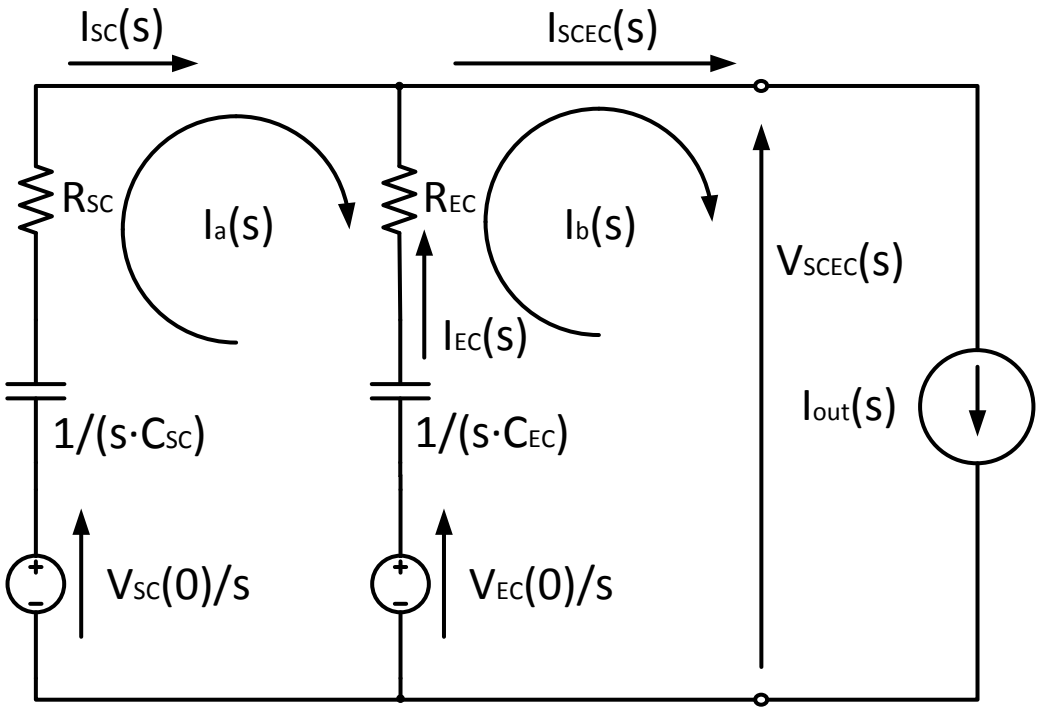

Figure A. 4 SCEC Constant Current Discharge Model (s Domain).

By KVL, the following equations are developed:

$$\begin{cases} \left(R_{SC} + \dfrac{1}{s \cdot C_{SC}} + R_{SC} + \dfrac{1}{s \cdot C_{EC}}\right) \cdot I_a(s) - \left(R_2 + \dfrac{1}{s \cdot C_{EC}}\right) \cdot I_b(s) = \dfrac{V_{SC}(0) - V_{EC}(0)}{s} \\ -\left(R_{EC} + \dfrac{1}{s \cdot C_{EC}}\right) \cdot I_a(s) + \left(R_{EC} + \dfrac{1}{s \cdot C_{EC}}\right) \cdot I_b(s) = \dfrac{V_{EC}(0)}{s} - V_{SCEC}(s) \\ I_b(s) = \dfrac{I_{out}}{s} \end{cases}$$

The first branch current $I_a(s)$ is calculated as:

$$I_a(s) = \frac{(V_{SC}(0) - V_{EC}(0) + I_{out} \cdot R_{EC}) \cdot S + \dfrac{I_{out}}{C_{EC}}}{(R_{SC} + R_{EC}) \cdot S^2 + \left(\dfrac{1}{C_{SC}} + \dfrac{1}{C_{EC}}\right) \cdot S} \qquad \textbf{(A. 4)}$$

Taking inverse Laplace transform, supercapacitor current:

$$I_{SC}(t) = i_a(t) = \frac{B}{D} + \left(\frac{A}{C} - \frac{B}{D}\right) e^{-\frac{D}{C} \cdot t}$$

$$where$$

$$A = V_{SC}(0) - V_{EC}(0) + I_{out} \cdot R_{EC}, B = \frac{I_{out}}{C_{EC}}, C = R_{SC} + R_{EC} \quad \textbf{(A. 5)}$$

$$and\ D = \frac{1}{C_{SC}} + \frac{1}{C_{EC}}$$

Electrolytic capacitor current:

$$I_{EC}(t) = i_b(t) - i_a(t) = I_{SCECout} - I_{SC}(t) \quad \textbf{(A. 6)}$$

Appendix B

Experimental Setup

B.1 Test Rig Structure

As the thesis has covered different conditions of SC discharging/charging, three different test rigs have been practically implemented.

B.1.1 Constant Current/Power Discharge for Characteristic Analysis

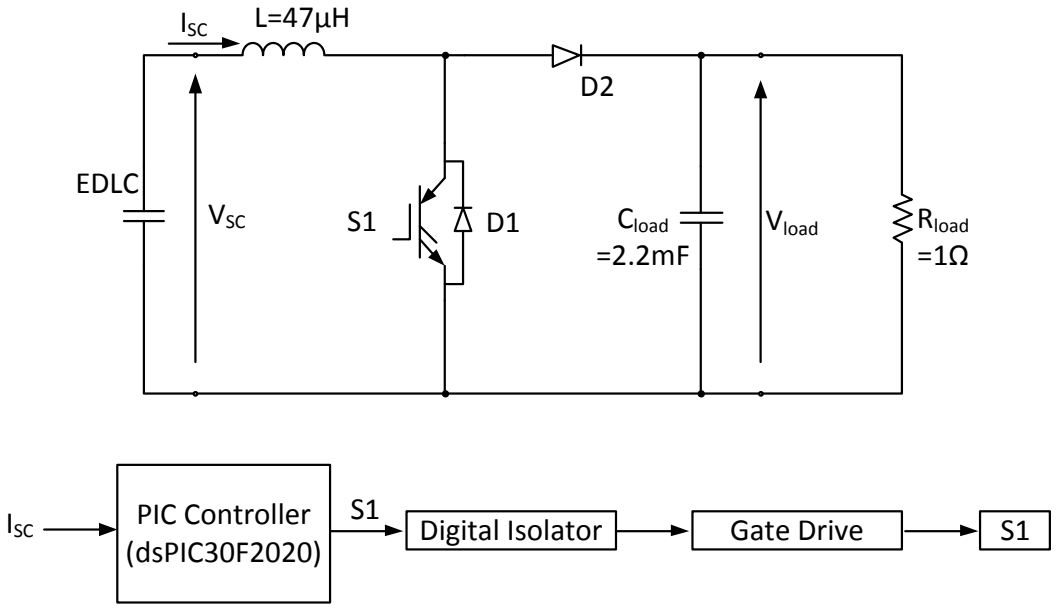

Figure A. 5 Constant Current Discharge Experiment Boost Converter.

The constant current/power characteristic analysis introduced in Chapter 2 is based on a boost converter, which includes the following components:

- 4 series connected supercapacitor BCAP0650.
- Inductor 47 µH.
- IGBT with diode.
- PIC controller and digital isolator.
- Gate drive.
- Voltage and current transducer.

- Load resistor and capacitor.

The electrical circuit diagram is shown in Figure A. 5, while the practical system photo is in Figure A. 6.

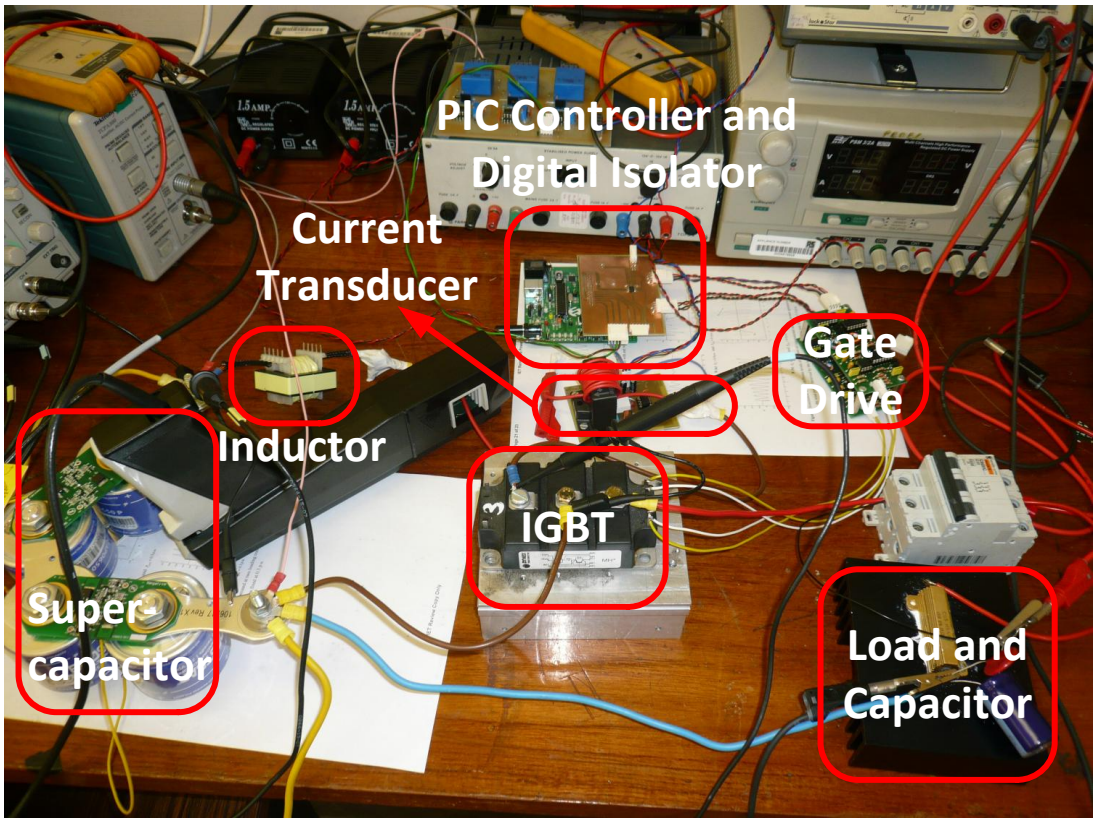

Figure A. 6 **System Photo of Boost Converter for Constant Current/Power Discharge.**

B.1.2 Bidirectional Buck-Boost Converter

The bidirectional buck-boost converter is introduced in Chapter 2, where a variable load is used to verify that power can be flowed bidirectional with the converter maintaining the load voltage. It includes the following components:

- 4 series connected supercapacitor BCAP0650.
- Inductor 47 µH.
- MOSFET based buck-boost converter.

- PIC controller and digital isolator.
- Gate drive.
- Voltage and current transducer.
- Variable ½ load resistor and capacitor.
- External current source.

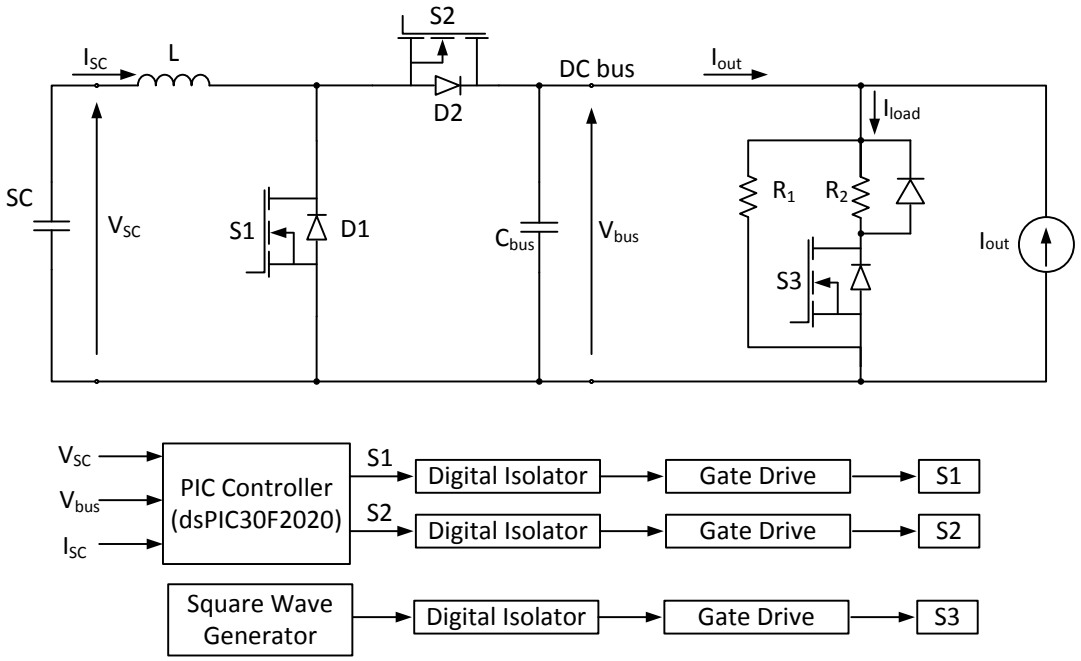

Figure A. 7 Bidirectional Buck-Boost Converter Variable Load Experiment.

The electrical circuit diagram is shown in Figure A. 7, while the practical system photo is in Figure A. 8.

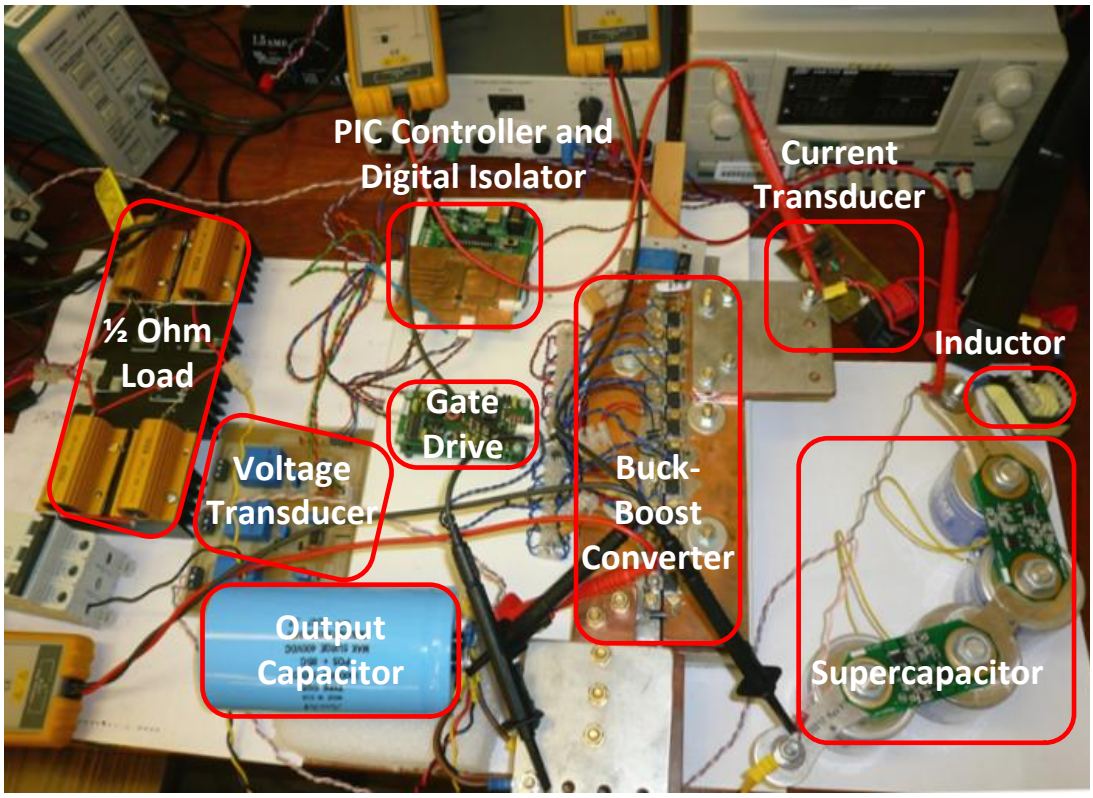

Figure A. 8 System Photo of Bidirectional Buck-Boost Converter Variable Load Experiment

B.1.3 SCEC System Constant Current Discharge

The SCEC system characteristics introduced in Chapter 4 are verified by constant current discharging of the system with a boost converter. It includes the following components:

- 4 series connected supercapacitor BCAP350.
- Inductor 47 µH.
- MOSFET based buck-boost converter.
- PIC controller and digital isolator.
- Gate drive.
- Current transducer.
- High power low resistance load.

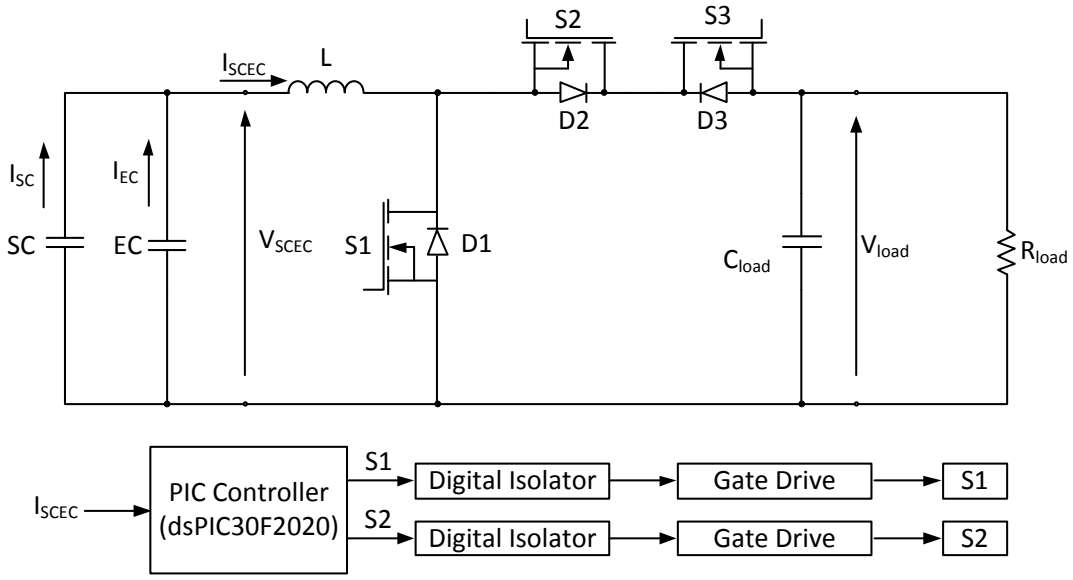

Figure A. 9 Experiment Circuit for SCEC System Constant Current Discharge.

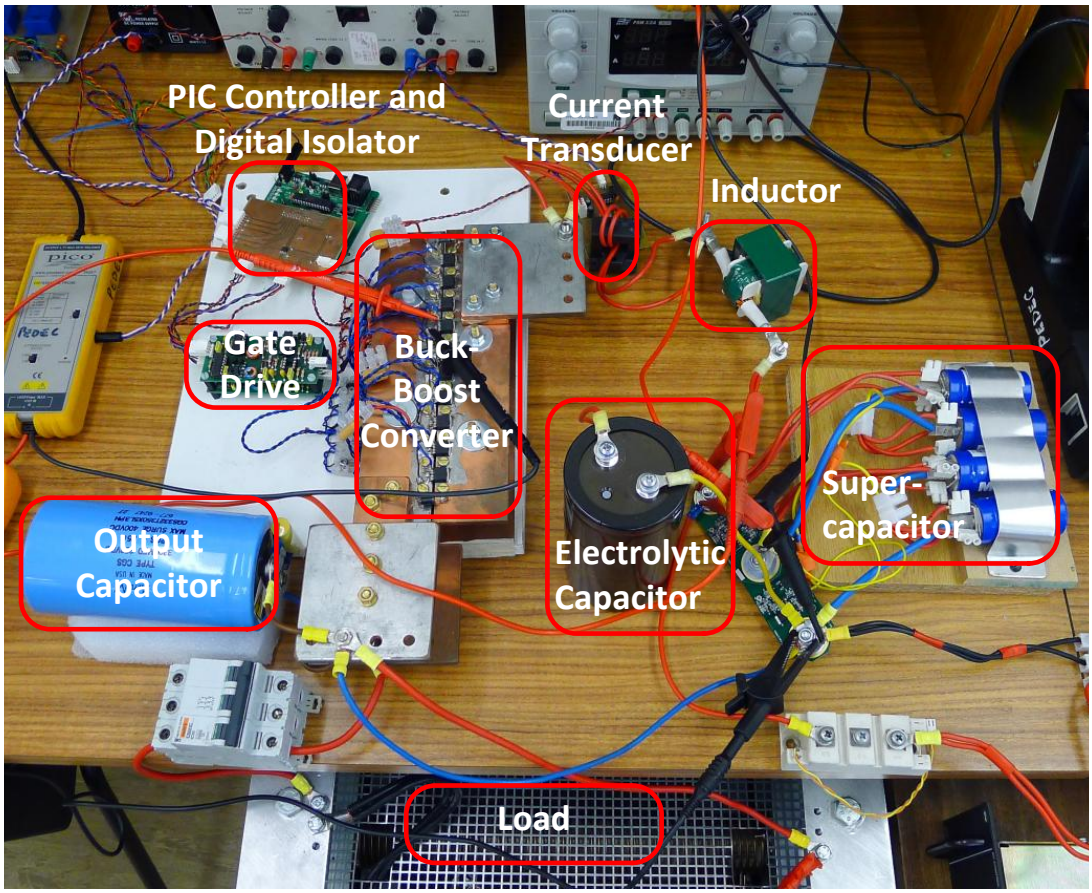

Figure A. 10 System Photo of SCEC System Constant Current Discharge.

The electrical circuit diagram is shown in Figure A. 9, while the practical system photo is in Figure A. 10.

B.2 Test Rig Components

The main components used in the practical implementations are introduced in this section.

B.2.1 PIC Controller

The main task of the PIC Controller is to sense the circuit analogue signals and to generate the required switch driving signals for power electronic devices according to the implemented software algorithm. The dsPIC30F2020 shown in Figure A. 11 is employed as the controller for all practical implementations.

Figure A. 11 dsPIC30F2020.

The main features of the DSP related to the practical implementation are:

- Modified Harvard architecture
- C compiler optimized instruction set architecture
- 24-bit wide instructions, 16-bit wide data path
- 12 Kbytes on-chip Flash program space
- 512 bytes on-chip data RAM
- 16 x 16-bit working register array
- Up to 30 MIPS operation:
    - Dual Internal RC

    - 9.7 and 14.55 MHz (±1%) Industrial Temp
    - 6.4 and 9.7 MHz (±1%) Extended Temp
    - 32X PLL with 480 MHz VCO
    - PLL inputs ±3%
    - External EC clock 6.0 to 14.55 MHz
    - HS Crystal mode 6.0 to 14.55 MHz
- 32 interrupt sources
- 8 user-selectable priority levels for each interrupt
- 4 processor exceptions and software traps

Power Supply PWM Module Features:

- Four PWM generators with 8 outputs
- Duty cycle resolution of 1.1 ns at 30 MIPS
- Individual dead time for each PWM generator:
- Dead-time resolution 4.2 ns at 30 MIPS
- Dead time for rising and falling edges
- Frequency resolution of 8.4 ns @ 30 MIPS
- PWM modes supported:
- Complementary
- Independent Current-Limit and Fault Inputs
- PWM generated ADC Trigger

ADC:

- 10-bit resolution
- 2000 Ksps conversion rate
- Up to 12 input channels
- PWM control loop:
    - Up to six conversion pairs available
    - Each conversion pair has up to four PWM and seven other selectable trigger sources
- Interrupt hardware supports up to 1M interrupts per second

B.2.2 PIC Controller Interface Circuits

An interface board is used to connect analogue input signals and output PWM gate drive signals which are isolated using optocoupler. The photo of the interface board is shown in Figure A. 12, with the circuit schematics shown in Figure A. 13.

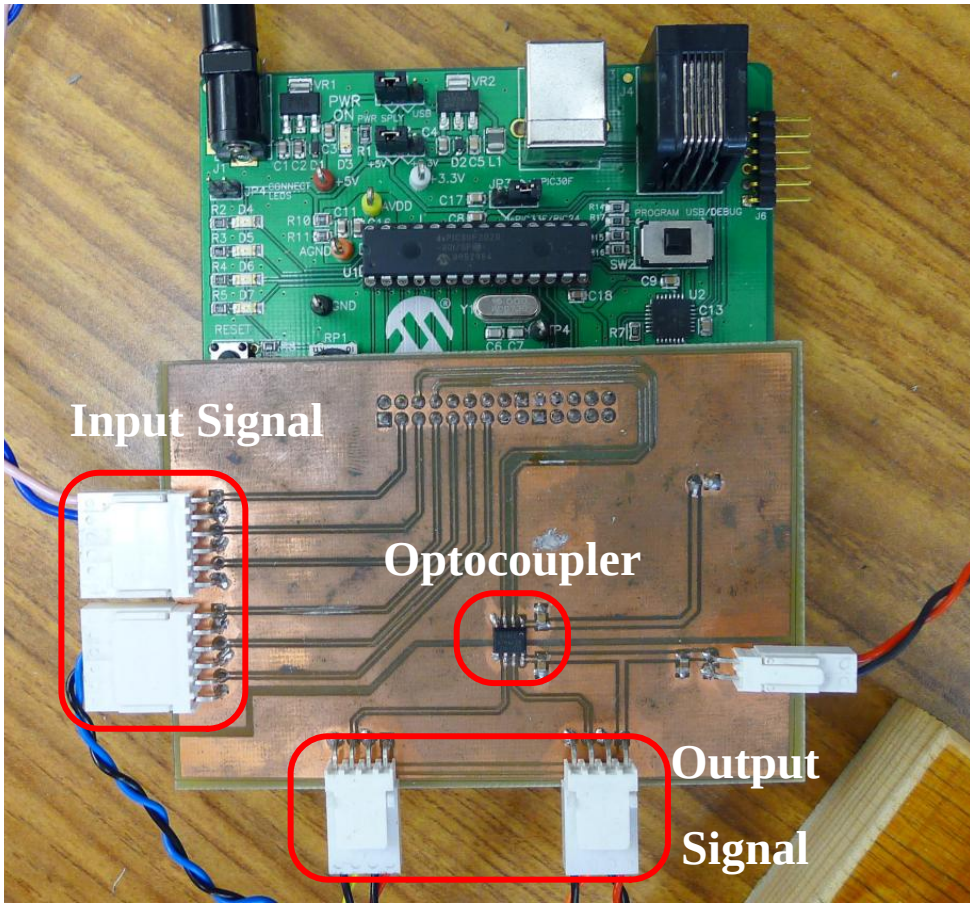

Figure A. 12 Photo of Interface Board

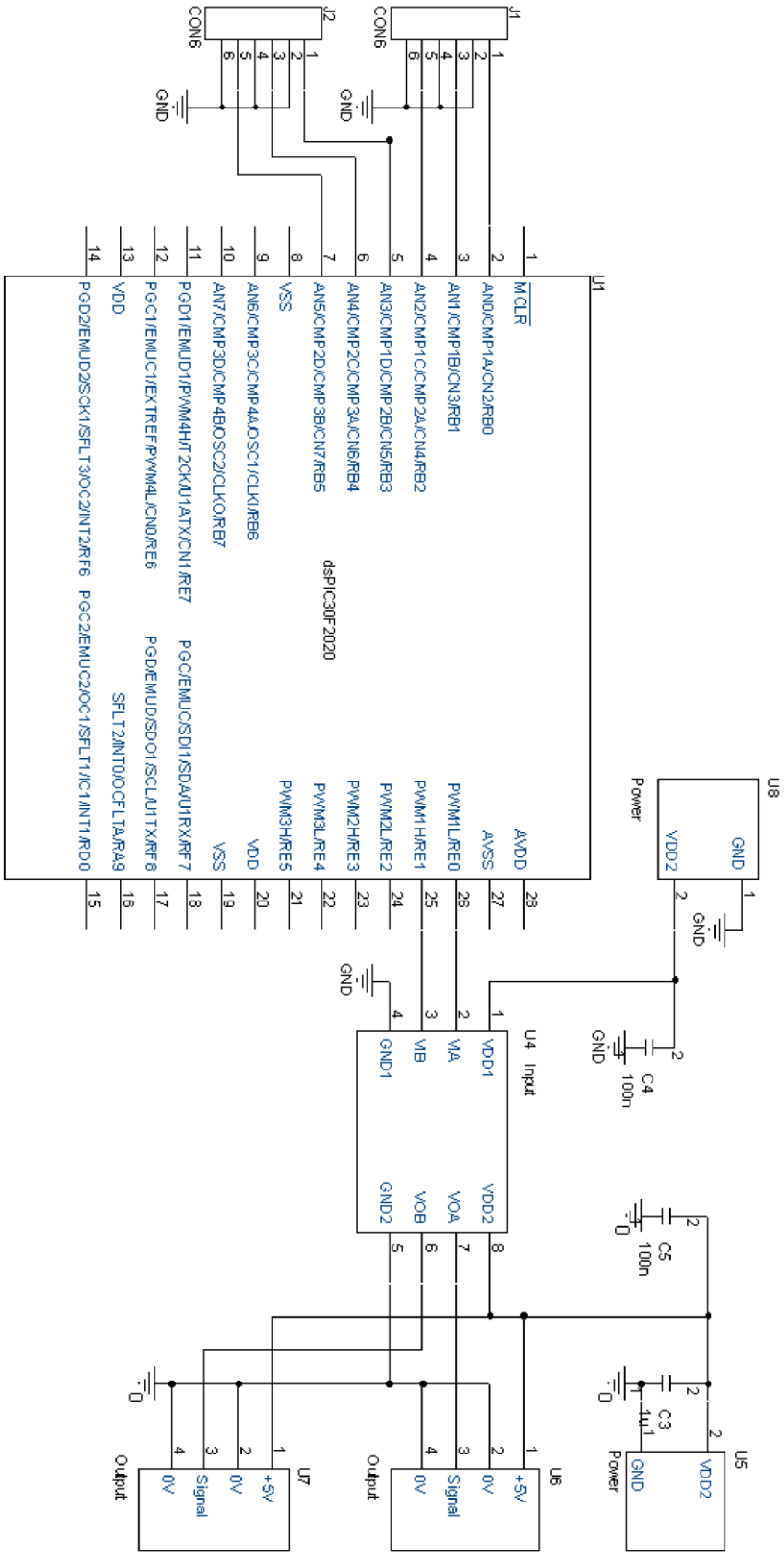

Figure A. 13 Electrical Circuit of Interface Board.

B.2.3 Voltage and Current Transducers

Voltage and current transducers are the key measurement devices to provide accurate data for the controller. The HAL 600-S current transducer, which is a Hall effect current sensing device, is employed with a extension board to interface the controller input signal requirement. The circuit schematic is shown in Figure A. 14, while the photo of transducers is in Figure A. 15.

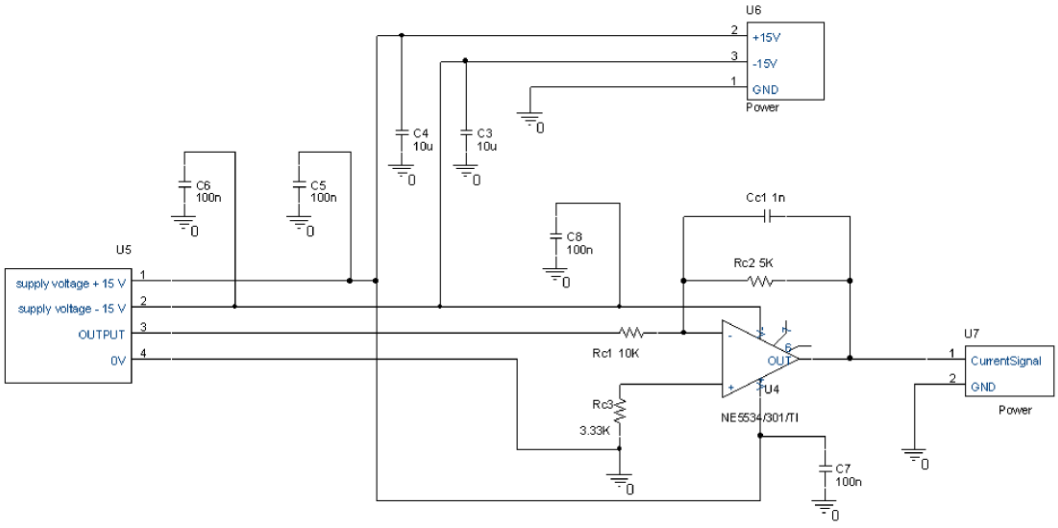

Figure A. 14 Circuit Schematic of the Current Transducer.

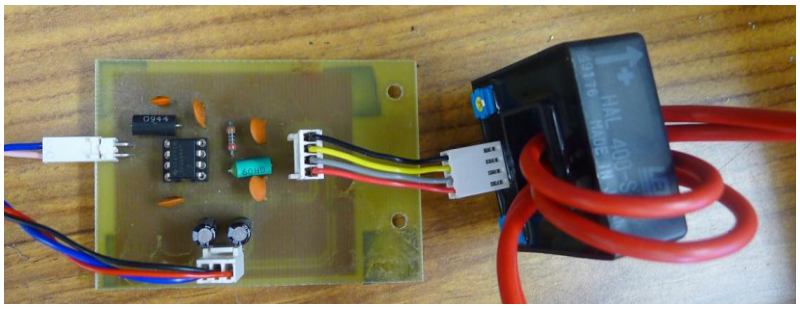

Figure A. 15 Photo of Current Transducer.

The voltage transducer, LV25P, is employed in the same way. The circuit schematic is shown in Figure A. 16, while the photo of transducers is in Figure A. 17.

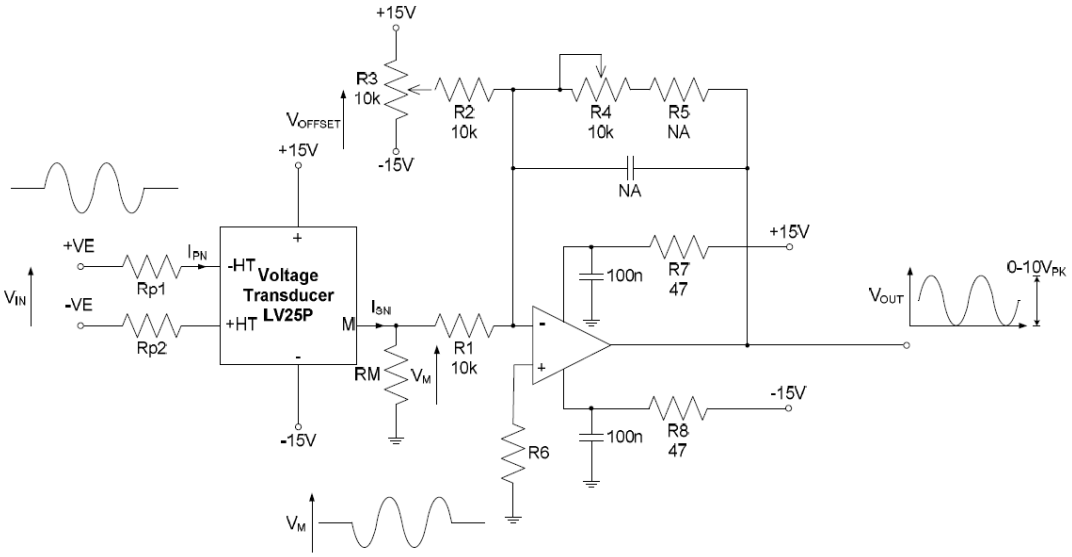

Figure A. 16 Circuit Schematic of the Voltage Transducer.

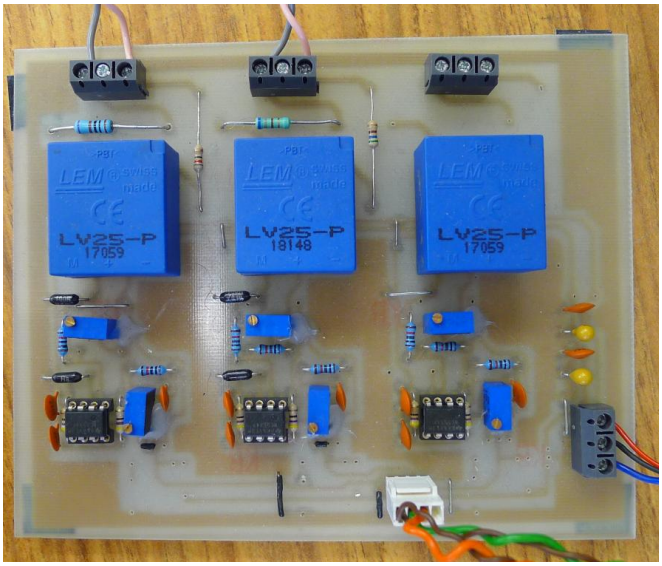

Figure A. 17 Photo of Voltage Transducer.

Appendix C

Program Code

C.1 Constant Current Discharge

```
#include "p30f2020.h"
#include "timer.h"
#include "smpsadc.h"
#include "dsp.h"
#include "smpspwm.h"

_FOSC(CSW_ON_FSCM_OFF & OSC2_CLKO & HS);
_FPOR(PWRT_OFF)
_FOSCSEL(PRIOSC_PLL)
_FGS(CODE_PROT_OFF)
_FBS(BSS_NO_FLASH)

int Current,PIref,Diff,DiffA,Kp,Ki;
unsigned  int Duty,Dutylimithigh,Dutylimitlow;
float Voltage;
void init_PWM1()
{
PTCONbits.SEVTPS=0;
PTCONbits.SYNCSRC=0;
PTCONbits.SYNCEN=1;
PTCONbits.SYNCOEN=0;
PTCONbits.SYNCPOL=0;
PTCONbits.EIPU=1;
PTCONbits.SEIEN=0;
PTCONbits.SESTAT=0;
PTCONbits.PTSIDL=0;
PTCONbits.PTEN=1;
PTPER=0x3E80;
PWMCON1bits.IUE=0;
PWMCON1bits.XPRES=0;
PWMCON1bits.DTC=1;
PWMCON1bits.MDCS=0;
PWMCON1bits.ITB=0;
PWMCON1bits.TRGIEN=1;
PWMCON1bits.CLIEN=0;
PWMCON1bits.FLTIEN=0;
PWMCON1bits.TRGSTAT=1;
PWMCON1bits.CLSTAT=0;
PWMCON1bits.FLTSTAT=0;
DTR1=160;
ALTDTR1=160;
```

```
PHASE1=0x8000;
TRGCON1=0;
PDC1=0x00;
TRIG1=0x1F40;
IOCON1bits.OSYNC=0;
IOCON1bits.CLDAT=0;
IOCON1bits.FLTDAT=0;
IOCON1bits.OVRDAT=0;
IOCON1bits.OVRENL=0;
IOCON1bits.OVRENH=0;
IOCON1bits.PMOD=0x0;
IOCON1bits.POLL=1;
IOCON1bits.POLH=1;
IOCON1bits.PENL=1;
IOCON1bits.PENH=1;
}

void init_ADC()
{
OpenSmpsADC(ADC_MOD_EN|ADC_IDLE_CONT|ADC_DATA_INT);
ConfigSmpsADCPort(ADC_PORT_PIN0_AN|ADC_PORT_PIN1_AN);
ConfigSmpsADCTrigSource0(ADC_AN1_0_TRIG_PWM1);
}

void __attribute__((__interrupt__))_PWM1Interrupt(void)
{
  IFS1bits.PWM1IF=0;
  Current=ReadSmpsADC(0);
  Diff=PIref-Current;
  DiffA=DiffA+Diff;
  Duty=Kp*Diff+Ki*DiffA;
if(Duty>Dutylimithigh)
  {
  Duty=Dutylimithigh;
    DiffA=Dutylimithigh;
  }
else if(Duty<Dutylimitlow)
{
  Duty=Dutylimitlow;
    DiffA=Dutylimitlow;
  }
else
  {
  Duty=Duty;
  }
PDC1=Duty;
}
```

```
void main()
{
init_ADC();
Current=ReadSmpsADC(0);
IEC1bits.PWM1IE=1;
init_PWM1();
Duty=8000;
Current=0;
PIref=605;
Kp=2;
Ki=5;
Dutylimithigh=14800;
Dutylimitlow=850;
TRISBbits.TRISB4=0;
PORTBbits.RB4=1;
while(1)
 {
 }
}
```

C.2 Constant Power Discharge

```
#include "p30f2020.h"
#include "timer.h"
#include "smpsadc.h"
#include "dsp.h"
#include "smpspwm.h"

_FOSC(CSW_ON_FSCM_OFF & OSC2_CLKO & HS);
_FPOR(PWRT_OFF)
_FOSCSEL(PRIOSC_PLL)
_FGS(CODE_PROT_OFF)
_FBS(BSS_NO_FLASH)

unsigned int Current,Voltage,Kp,Ki;
unsigned int Power;
int PIref,Diff,DiffA;
int Duty;

void init_PWM1()
{
PTCONbits.SEVTPS=0;
PTCONbits.SYNCSRC=0;
PTCONbits.SYNCEN=1;
PTCONbits.SYNCOEN=0;
PTCONbits.SYNCPOL=0;
PTCONbits.EIPU=1;
```

```
PTCONbits.SEIEN=0;
PTCONbits.SESTAT=0;
PTCONbits.PTSIDL=0;
PTCONbits.PTEN=1;
PTPER=0x3E80;
PWMCON1bits.IUE=0;
PWMCON1bits.XPRES=0;
PWMCON1bits.DTC=1;
PWMCON1bits.MDCS=0;
PWMCON1bits.ITB=0;
PWMCON1bits.TRGIEN=1;
PWMCON1bits.CLIEN=0;
PWMCON1bits.FLTIEN=0;
PWMCON1bits.TRGSTAT=1;
PWMCON1bits.CLSTAT=0;
PWMCON1bits.FLTSTAT=0;
DTR1=0x0064;
ALTDTR1=0x0064;
PHASE1=0x8000;
TRGCON1=0;
PDC1=0;
TRIG1=0x1F40;
IOCON1bits.OSYNC=0;
IOCON1bits.CLDAT=0;
IOCON1bits.FLTDAT=0;
IOCON1bits.OVRDAT=0;
IOCON1bits.OVRENL=0;
IOCON1bits.OVRENH=0;
IOCON1bits.PMOD=0x0;
IOCON1bits.POLL=1;
IOCON1bits.POLH=1;
IOCON1bits.PENL=1;
IOCON1bits.PENH=1;
}

void init_ADC()
{
OpenSmpsADC(ADC_MOD_EN|ADC_IDLE_CONT|ADC_DATA_INT);
ConfigSmpsADCPort(ADC_PORT_PIN0_AN|ADC_PORT_PIN1_AN);
ConfigSmpsADCTrigSource0(ADC_AN1_0_TRIG_PWM1);
}

void __attribute__((__interrupt__))_PWM1Interrupt(void)
{
  IFS1bits.PWM1IF=0;
  Current=ReadSmpsADC(0);
  Voltage=ReadSmpsADC(1);
  Power=(Current*Voltage)/100;
```

```
  Diff=PIref-Power;
  DiffA=DiffA+Diff;
  Duty=Kp*Diff+Ki*DiffA;

if(Duty>0x3E80)
  {
  Duty=0x3E80;

  DiffA=0x3E80;
  }
else if(Duty<0x0010)
  {
  Duty=0x0010;

  DiffA=0;
  }
else
  {
  Duty=Duty;
  }
PDC1=Duty;
}

void main()
{
init_ADC();
Current=ReadSmpsADC(0);
Voltage=ReadSmpsADC(1);
IEC1bits.PWM1IE=1;
init_PWM1();
Duty=0;
Current=0;
PIref=600;
Kp=1;
Ki=1;
while(1)
 {
 }
}
```

C.3 Constant Load Voltage with Bidirectional Buck/Boost Converter

```
#include "p30f2020.h"
#include "timer.h"
#include "smpsadc.h"
#include "dsp.h"
#include "smpspwm.h"
```

```
_FOSC(CSW_ON_FSCM_OFF & OSC2_CLKO & HS);
_FPOR(PWRT_OFF)
_FOSCSEL(PRIOSC_PLL)
_FGS(CODE_PROT_OFF)
_FBS(BSS_NO_FLASH)

Unsigned int
mode,SCVoltage,OutVoltage,Current,LowVoltageLimit,HighVoltageLimit;
float Kp,Ki;
float CurrentPIref,VoltagePIref,Diff,DiffA;
float Duty;

void init_PWM1()
{
PTCONbits.SEVTPS=0;
PTCONbits.SYNCSRC=0;
PTCONbits.SYNCEN=1;
PTCONbits.SYNCOEN=0;
PTCONbits.SYNCPOL=0;
PTCONbits.EIPU=1;
PTCONbits.SEIEN=0;
PTCONbits.SESTAT=0;
PTCONbits.PTSIDL=0;
PTCONbits.PTEN=1;
PTPER=0x3E80;
PWMCON1bits.IUE=0;
PWMCON1bits.XPRES=0;
PWMCON1bits.DTC=1;
PWMCON1bits.MDCS=0;
PWMCON1bits.ITB=0;
PWMCON1bits.TRGIEN=1;
PWMCON1bits.CLIEN=0;
PWMCON1bits.FLTIEN=0;
PWMCON1bits.TRGSTAT=1;
PWMCON1bits.CLSTAT=0;
PWMCON1bits.FLTSTAT=0;
DTR1=640;
ALTDTR1=640;
PHASE1=0x8000;
TRGCON1=0;
PDC1=0x00;
TRIG1=0x1F40;
IOCON1bits.OSYNC=0;
IOCON1bits.CLDAT=0;
IOCON1bits.FLTDAT=0;
IOCON1bits.OVRDAT=0;
IOCON1bits.OVRENL=0;
IOCON1bits.OVRENH=0;
```

```
IOCON1bits.PMOD=0x0;
IOCON1bits.POLL=1;
IOCON1bits.POLH=1;
IOCON1bits.PENL=1;
IOCON1bits.PENH=1;
}

void init_ADC()
{
OpenSmpsADC(ADC_MOD_EN|ADC_IDLE_CONT|ADC_DATA_INT);
ConfigSmpsADCPort(ADC_PORT_PIN0_AN|ADC_PORT_PIN5_AN|ADC_PORT
_PIN4_AN);
ConfigSmpsADCTrigSource0(ADC_AN1_0_TRIG_PWM1);
ConfigSmpsADCTrigSource2(ADC_AN5_4_TRIG_PWM1);
}

void buckcharge()
{
if(SCVoltage<HighVoltageLimit)
 {
   HighVoltageLimit=800;
   IOCON1bits.PENL=1;
   Diff=CurrentPIref-Current;
   DiffA=DiffA+Diff;
 if(DiffA>288000)
   {
     DiffA=288000;
   }
 else
   {
   DiffA=DiffA;
   }
   Duty=0.8*Diff+0.5*DiffA;

  if(Duty>14400)
   {
    Duty=14400;
   }
  else if(Duty<1600)
   {
    Duty=1600;
   }
  else
   {
    Duty=Duty;
   }
}
else
```

```
{
 IOCON1bits.PENL=0;
 Duty=15990;
 HighVoltageLimit=800;
 mode=0;
}
PDC1=16000-Duty;
}

void normal()
{
   Diff=VoltagePIref-OutVoltage;
   DiffA=DiffA+Diff;
if(SCVoltage<=LowVoltageLimit)
 {mode=1;}
else if(SCVoltage<HighVoltageLimit)
 {
  IOCON1bits.PENL=1;
  HighVoltageLimit=800;
  if(DiffA>280000)
   {
   DiffA=280000;
   }
   Duty=Kp*Diff+Ki*DiffA;

  if(Duty>13500)
   {
   Duty=13500;
   }
  else if(Duty<0x0010)
   {
   Duty=0x0010;

   DiffA=0;
   }
  else
   {
   Duty=Duty;
   }
 }
else
 {
  IOCON1bits.PENL=0;
  HighVoltageLimit=780;
  Duty=10;
 }
PDC1=Duty;
}
```

```
void __attribute__((__interrupt__))_PWM1Interrupt(void)
{
 IFS1bits.PWM1IF=0;
 Current=ReadSmpsADC(0);
 SCVoltage=ReadSmpsADC(5);
 OutVoltage=ReadSmpsADC(4);
 if(mode==1)
 {
 buckcharge();
 }
 else
 {
 normal();
 }
}
void main()
{
init_ADC();
Current=ReadSmpsADC(0);
SCVoltage=ReadSmpsADC(5);
OutVoltage=ReadSmpsADC(4);
IEC1bits.PWM1IE=1;
init_PWM1();
Duty=10;
VoltagePIref=700;
CurrentPIref=580;
Kp=0.1;
Ki=0.5;
HighVoltageLimit=800;
LowVoltageLimit=20;
while(1)
 {
  if(SCVoltage<LowVoltageLimit)
  {
   mode=1;
   while(mode==1)
   {}
  }
  else
  {
   mode=0;
   while(mode==0)
   {}
  }
 }
}
```

Appendix D

List of Tables and Figures

D.1 List of Figures

D.2 List of Tables

Appendix E

List of Author's Publications

Xiao Chang; Holliday, D.; Williams, B.W., "Efficiency improved supercapacitor based energy storage system for short duration, large amplitude current pulse applications," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE* , vol., no., pp.3112,3116, 17-21 March 2013.

Abstract: A combined supercapacitor and electrolytic capacitor energy storage system offers efficiency improvements in excess of 10% when compared to a supercapacitor-only storage system used in short-duration (<1s), high-current discharge applications. The technique is suited to distributed generation applications where low-voltage ride through and grid code compliance are important considerations. A simplified mathematical model of the system compares well with more complex, established modelling approaches, and simulation and experimental results verify the proposed technique.