DC Fault Protection in HVDC System and the Impact on AC Frequency Response

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Date:

Dedicated to my family

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Abstract

The integration of renewable energy generations requires the transmission of bulky power over long distance and in many applications, HVDC transmission systems become a more preferable choice compared to conventional HVAC systems. Thus, the reduction of conventional synchronous generators in the system coupled with the increase of DC connections reduces system inertia and weakens the effect of primary frequency regulation leading to larger frequency derivation in the event of large transients. This thesis investigates frequency support strategies utilizing the flexible power flow controllability of MMC-HVDC. Different control strategies for providing frequency support in a 2-terminal and 3-terminal HVDC systems are studied in detail.

For HVDC systems, DC protection strategy can significantly impact on the duration of power outage in the event of a DC fault. The current definition of maximum loss-of-infeed for an AC network does not consider the duration of the power outage, and the impacts of DC fault protection arrangements which result in different speed of power restoration, on the system frequency of connected AC network, have not been properly understood. Different DC protection arrangements using DC switches, fast and slow DC circuit breakers on frequency response of the connected AC networks are investigated. A 3-terminal meshed HVDC system is studied to demonstrate system behaviour during DC faults. It is found that both the amount of power loss and outage duration affect system frequency response, and thus the two need to be considered simultaneously when determining the maximum “loss-of-infeed” for future AC-DC hybrid power grids.

The full-bridge submodule based MMCs have DC fault blocking and active fault current control capability. An energy based virtual damping control for FB-MMC is proposed to rapidly de-energise large meshed DC network in the event of a DC fault by quickly absorbing energy from the DC network through the FB-MMCs. The proposed method regulates the DC terminal current of the FB-MMC to follow the DC voltage to behave as a virtual damping resistor to quickly suppress the potential circulating DC fault currents. This enables fast fault isolation using DC switches and thereby fast fault recovery after fault isolation. The fault isolation time is significantly reduced from around

50ms with the existing FB-MMC fault control method to around 15 ms. The validity of the proposed control is verified in a three-terminal meshed DC network.

List of Abbreviations

HVDC	High Voltage Direct Current
LCC	Line Commutated Converter
IGBT	Insulated-Gate Bipolar Transistor
VSC	Voltage Source Converter
MMC	Modular Multilevel Converter
MTDC	Multi-Terminal Direct Current
DG	Distributed Generation
DCCB	Direct Current Circuit Breaker
ROCOF	Rate Of Change Of Frequency
DCSW	Direct Current Switch
PWM	Pulse Width Modulation
SM	Sub-Model
HB	Half-Bridge
FB	Full-Bridge
INEC	Inertial Emulation Control
SCR	Silicon-Controlled Rectifier
ITOP	Inverse Time Overcurrent Protection
FFT	Fast Fourier Transformation
CWT	Continuous Wavelet Transformation
GPS	Global Positioning System
NLM	Nearest Level Modulation
PLL	Phase Locked Loop
PSS	Power System Stabilizer
ACCB	Alternating Current Circuit Breaker

List of Symbols

MMC model symbols:

I_{dc}	Nominal DC current
U_{dc}	Nominal DC voltage
P	Power rating
N	Number of SM per arm
V_{sm}	SM DC voltage
C_{sm}	SM capacitance
L_{arm}	Arm inductance
L_t	Station DC terminal inductance
i_{pj}	Upper arm current
i_{nj}	Lower arm current
u_{pj}	Upper arm voltage
u_{nj}	Lower arm voltage
i_{cj}	Converter terminal AC phase current
u_{cj}	Converter terminal AC phase voltage
u_{commj}	Common mode voltage
i_{comj}	Common mode current
u_{diffj}	Difference mode voltage
i_{cirj}	Circulating current
Subscript j	j=a,b,c
R_0	Arm resistance
L_0	Arm inductance
I_{r2m}	2nd order harmonic of nominal DC current
U_s	AC network voltage
$\tilde{u}_{commj}$	2nd harmonic of common mode voltage
i_{cd}	d-axis current
i_{cq}	q-axis current

Subscript *	Reference value

AC system model symbols:

J_{sys}	System inertia
ω	Electrical angular frequency
P_g	System power generated
P_d	System power consumed
H_{gen}	Generator inertia time constant
H_{sys}	System inertia time constant
S_{gen}	Generator nominal power rating
S_{sys}	System nominal power rating
ω_0	Nominal angular frequency
J_{gen}	Generator inertia
Subscript *	Per unit values
Pf	Generator power factor
T_e	Generator electromagnetic torque
ω_m	Generator rotor speed
P_m	Generator mechanical power input
P_{eo}	Generator electrical power output
pp	Generator pole pairs
X_{trm}	Transformer reactance
R_{trm}	Transformer resistance
L	Length of Cable
R_{cable}, L_{cable}, C_{cable}	R, L and C per unit length of cable
N_{pi}	Number of pi section

Control of MMC in Chapter 4:

f_i	AC system frequency
Δf_i	Frequency deviation
Subscript i	Number of terminal (i=1,2,3)

v_{dc}	DC voltage
Δv	DC voltage deviation
${\Delta P_{dc}}^{ref}$	Active DC power deviation reference
${\Delta V_{dc}}^{ref}$	DC voltage deviation reference
k	Gain of frequency support control

Control of MMC in Chapter 6:

P	Converter station DC terminal active power
E	Energy absorbed by converter station
v, i	Converter station DC terminal voltage and current
Subscript *ref*	Reference of the value
R_v	Control parameter of virtual DC damping resistor
k	Gain of the MMC virtual damping control

List of Figures

List of Tables

Table of Contents

Chapter 1 Introduction

1.1 HVDC development

In the early twentieth century, the development of the mercury arc valves technology led the born of the high voltage direct current (HVDC) power transmission technology [1], and the world's first commercial HVDC project was installed from the mainland of Sweden to the island of Gotland in 1954 using a 96 km undersea cable at 100 kV and 20 MW [2]. From then on, more and more HVDC transmission projects have been put into operation all around the world.

With the rapid development of semiconductors and power electronics technologies, thyristor based line commutated converter (LCC) HVDC technology became the dominated technology for the HVDC power transmission in the 1970s. Further development work in the related area has made HVDC power transmission more advantages over the traditional AC power transmission such as large capacity power transmission over a long distance, power transmission through underground and undersea cables and interconnections of non-synchronous AC networks [3].

Since 1990s, due to the development of Insulated-Gate Bipolar Transistor (IGBT) HVDC transmission technology based on voltage source converters (VSC) has been proposed [4, 5]. In order to distinguish from the thyristor based HVDC power transmission technology, it was defined by CIGRE and IEEE as voltage source converter based high voltage direct current (VSC-HVDC) power transmission technology.

In the early 2000s the modular multilevel converter (MMC) was developed which has revolutionised VSC-HVDC transmission. Due to the use of fully-controlled switching devices and modular structure, MMC-HVDC systems have many advantages over the traditional LCC-HVDC [6], including decoupling control of real and reactive powers, near sinusoidal converter voltage/current, no need for reactive power compensation, power supply for passive networks, compact design etc.

1.2 Challenges for future AC/DC hybrid power network

However, with the HVDC power transmission technology showing advantages over AC power transmission technology, problems emerge at the same time. Large number of infeed integrated through converters significantly decrease the entire system inertia leading to frequency problems. Meanwhile, comparing to the point-to-point HVDC system at the beginning of the HVDC technology development, the multi-terminal HVDC (MTDC) power transmission system is required in order to meet the future power network requirement [7]. However, MTDC power transmission system increases the system operation flexibility and power transmission capacity on one hand, it also increases the complexity of system structure on the other hand. A fault occurring on the part of a MTDC system will affect all the other DC converters connected to the same DC network and potentially causing significant disruption to the wide AC networks connected to the DC system. This can potentially threat the safe and stable operation of the entire AC/DC integrated system. In addition, the interactions between the AC and DC systems, between different DC systems connected to the same AC network, make the control and protection strategies for the whole system more complex.

1.2.1 System inertia reduction and frequency stability

In order to deal with the climate change problem, green energies such as wind and solar power generation is getting more and more attention. For example, as outlined in the 'Gone Green' generation mix for the future shown in Fig. 1.1 which is represented in the UK National Grid Ten Year Statement 2014, the traditional fossil fuel fired generation will be significantly replaced by the wind farm and gas generation [8]. Because the existing large power grid is radial or interconnected traditional network with a single 'lumped' source at each end, those new green energy generations will be connected into the current power grid as remote infeeds and distributed generations (DGs).

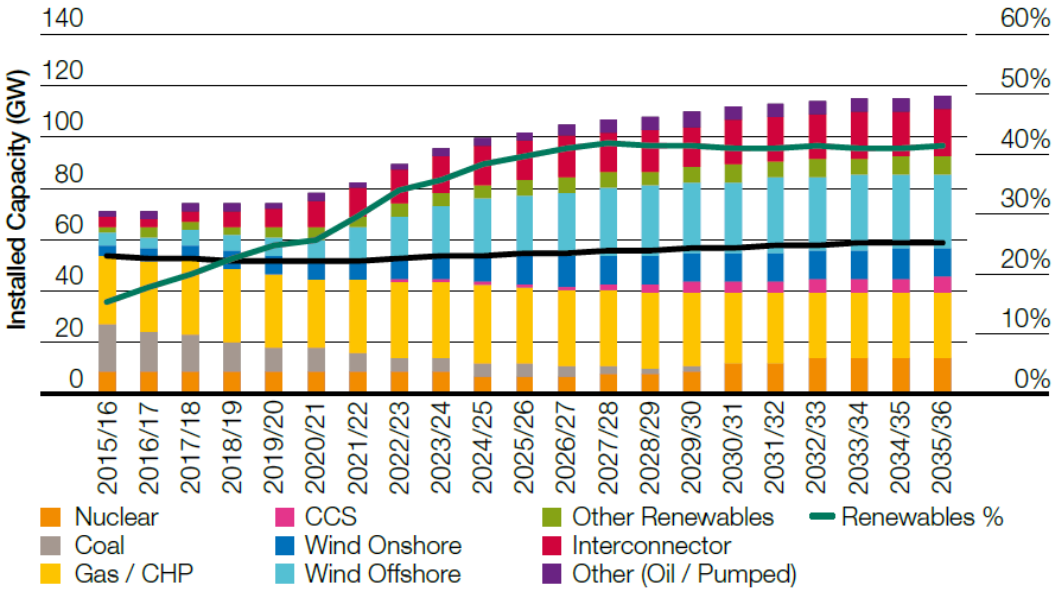


Fig. 1. 1 'Gone Green' generation mix for the future [8].

There are many advantages of the network connecting with more remote infeed compared to connecting with single source such as flexible generator locations, shorter distances between source and generators, and more emergency backup units connections etc. However, different types of energy generations connected to the grid give different effects to the power system operation and result in some system operation challenges. The main challenge that attracted attention is the reduction in system inertia.

Wind turbines are connected to the network through power electronics equipment like VSC, which de-coupled the rotation component of the wind turbine from the network [9]. For other kinds of renewable sourced generations such as solar PVs, they do not have any rotating components due to its design. In this way, such renewable generations cannot contribute inertia to the system. This also applies to HVDC interconnections as the connected AC networks are decoupled and system inertias on the individual networks do not influence the others. Consequently, the overall inertia of future power systems will decline significantly resulting in significant frequency deviations under transients and potentially system instability.

For the power grid standard frequency regulation procedure during the frequency even, the primary frequency regulation will be initialled firstly. It is an automatic procedure provided by the generators' governor to regulate their output within their capacities to balance the difference between load and generation thus stopping the grid frequency drop/increase. The primary frequency regulation can only stabilize the frequency at the new balance point with difference from the normal value remained. The secondary frequency regulation generators, such as large power plants and power storage units, will be dispatched by the system operators to provide secondary frequency regulation in order to make the frequency back to its normal value. The frequency regulation procedure is an important method to keep the power grid stable facing system disturbances. The inertia reduction will significantly weaken the system frequency regulation leading to potentially system instability such as serious frequency deviation under transients.

1.2.2 DC network protection and impact on connected AC network

HVDC transmission systems based on modular multilevel converters (MMCs) have developed rapidly due to their significant advantages. However, the behaviours and characteristics of large DC network during DC faults are major issues to be considered in future applications. In the event of a DC short circuit, there potentially leads to high AC and DC current and rapid collapse of the complete DC network [10-12]. For large scale HVDC systems connecting offshore wind farms and AC networks, e.g. the proposed North Sea Super Grid, disturbances in the DC network especially during DC faults, can cause severe disruption to power transmission and the operation of the connected AC networks. However, the detailed study on how DC protection affecting the connected AC system operation, e.g. frequency transient, is still insufficient.

On the other hand, the development of future large DC networks which are likely to use different types of converter configurations and protection arrangements, requires improved coordination between converter control and protection devices. For example, the full-bridge (FB) based MMCs is able to control the fault current during DC faults and thus enables the use of low cost DC switches instead of the more expensive DC circuit breakers (DCCBs). However, such capabilities of FB-MMC have not been made best use

for DC fault protection strategies for large-scale meshed DC networks and further research and development are required.

1.3 Scope of the thesis

1.3.1 Research motivation and objective

Research motivations are raised based on the two aspects of challenges for the future power network with large scale HVDC systems penetration, i.e.:

i. Frequency problem caused by reduction of system inertia

In the event of loss of infeed and load change in a AC network, it has been indicated in [13-16] that the rate of change of frequency (ROCOF) will increase significantly for an AC-DC hybrid system with low inertia, compared to systems with high inertia. In [17], a comparison of frequency response after generator outage in hybrid systems with different levels of wind penetration was carried out and the results showed that the ROCOF and frequency nadir became larger with the decrease of system inertia. Meanwhile, the reduction of system inertia weakens the effect of primary frequency regulation provided by conventional synchronous generators which will make the system frequency performance even worse after such AC network disturbances [18, 19]. Therefore, frequency support utilizing the flexible power flow controllability of MMC-HVDC is increasingly important and thus will be investigated in this thesis.

DC faults can cause significant disruption to the whole DC network and consequently affecting the connected AC systems. Most of the researches on DC fault in an AC-DC hybrid system have been focused on fault transient analysis, e.g. fault currents [20], fault detection, locating and isolation [21-23], and fault ride-through capabilities [24, 25]. There is limited research on the impacts of DC fault and DC protection strategies on frequency response of the connected AC system in a low inertia system environment. In both point-to-point and MTDC systems, the severity of DC fault impact is affected by the magnitude and duration of the power outage, which is highly dependent on the employed

protection strategy and recovery method after fault isolation. Therefore, a better understood of the impact of DC protection and control strategies on frequency response of connected AC network is essential for improving system stability and DC protection technology, and will be investigated in this thesis.

ii. FB-MMC fault current control capability for large meshed DC networks protection.

Due to the DC fault blocking capability and high controllability during DC faults, the use of FB-MMCs can significantly simplify DC protection requirement and strategy. By simply blocking the MMC during the fault to reduce the fault current injection from AC side thereby reduce the requirements for the DC current breaking devices, or actively controlling the DC fault current for its suppression, have shown good performance in point-to-point HVDC systems or radial MTDC systems[26, 27]. However, the application of such concepts in large meshed MTDC systems remains unclear due to existence of the various DC fault current loops. Therefore, the fault current control ability of FB-MMC during DC faults should be further investigated in large meshed MTDC systems which are the trend of DC power network development with increased size and structure complexity.

1.3.2 Thesis contributions

The main contributions of this thesis are:

- An active power sharing strategy is proposed for frequency support which enables the power shortage to be shared proportionally by the frequency-support providing terminals during a frequency transient at one of the AC terminals, thus to achieve optimised overall frequency response across large AC networks.

- A full-scale protection system is developed for a 3-terminal meshed MMC-HVDC system where impact of different protection equipment employed (e.g. DCSWs, slow DCCBs and fast DCCBs) on frequency response of the connected AC system is studied. Studies on the impact of the amount of loss-of-infeed and power loss duration on frequency response are provided to better

understand the system design requirement related the maximum loss-of-infeed of HVDC connected AC systems.

- An energy based virtual damping control of FB-MMCs for meshed HVDC using DCSWs is proposed for fast DC cable fault current interruption. The DC fault current interruption time is reduced from around 50ms to 15ms, comparing to other control methods, thus enables using DCSWs for fault fast isolation. The effectiveness of proposed control is investigated in detail including the influences of different control parameters and different fault locations.

1.4 Thesis organization

This thesis is organised as follows:

Chapter 2 provides a general literature review of related contents in this thesis including HVDC technology, frequency support strategies in HVDC system, DCCB technology, DC fault detection and location, and DC fault protection strategies for HVDC systems.

Chapter 3 presents the modelling of MMC system that is used in simulations including converter modelling and controller design. Meanwhile, the modelling of simplified AC systems for frequency studies is also provided. Typical simulation results are presented to illustrate the behaviour of the SG models for AC system frequency dynamics study.

Chapter 4 studies the frequency dynamics during load increase in an ac network connected to a 2-terminal and 3-terminal HVDC systems, respectively. The use of HVDC system for power system frequency support is studied. Detailed simulations are carried out to investigate and validate various system frequency support strategies. The effectiveness of such strategies using different control parameters are also illustrated. An active power sharing strategy is proposed and investigated for a 3-terminal system that

enables power shortage to be shared proportionally to the AC grid capacities of the frequency-support providing terminals.

Chapter 5 develops a full-scale DC protection system for a 3-terminal meshed HVDC system to study the impact of different protection strategies on frequency response of the connected AC system Different protection systems using DCSWs, slow DCCBs and fast DCCBs are studied. Using the developed model, the impact of the amount and duration of power loss during a DC fault on the AC frequency of the connected network is carried out.

Chapter 6 discusses the problems associated with the conventional active fault current control methods of FB-MMC in meshed DC systems. An energy based virtual damping control of FB-MMC for HVDC grids is proposed to achieve fast fault current interruption and DC network de-energisation. The effectiveness of the proposed control strategy is studied including the impact of different aspects including control parameters, controller dynamics such as control delay and fault location.

Chapter 7 delivers the conclusion and suggests for future work.

Chapter 2 Literature Review

This chapter provides an overview of HVDC systems, the issues and proposed solutions related to AC power network with significant converter presence, and the different DC fault protection and management methods. A general overview of HVDC transmission system solutions are introduced first, including the LCC-HVDC, VSC-HVDC, hybrid-HVDC systems etc. Problem related to AC system frequency under low inertia system environment and various frequency support strategies are reviewed. Different DC fault current interrupters, i.e., DC circuit breakers are reviewed. Finally, a general overview of DC fault protection strategies for HVDC system including fault detection, location and protection strategies are presented.

2.1 HVDC Power Transmission Systems

Depending on the used converter technology, HVDC transmission systems can be largely classified as LCC-HVDC and VSC-HVDC systems. This section will introduce individual technology and their advantages and drawbacks are then summarised and compared with in Table 2.1.

2.1.1 LCC-HVDC

LCC-HVDC is a mature technology operating around world since 1950s [28]. It is based on thyristors, which can only be controlled to switch on, whilst its switch off has to rely on external AC grid to provide the commutation voltage. The advantages of large transmission capacity with highest device current and voltage rating of 6250A and 10kV [29, 30], low cost and mature technology make it widely used for the AC-DC hybrid power grid at this stage. The basic structure of LCC is a 6-pulse bridge composed by six thyristor valves. However, due to the harmonic currents generated by the 6-pulse bridge arrangement, the most widely used is the 12-pulse bridge arrangement shown in Fig. 2.1, to reduce the AC and DC harmonics.

However, with lack of abilities such as black start, flexible power flow reversal, power delivery to passive network, LCC-HVDC cannot fulfil the requirements for future large-scale DC power systems.

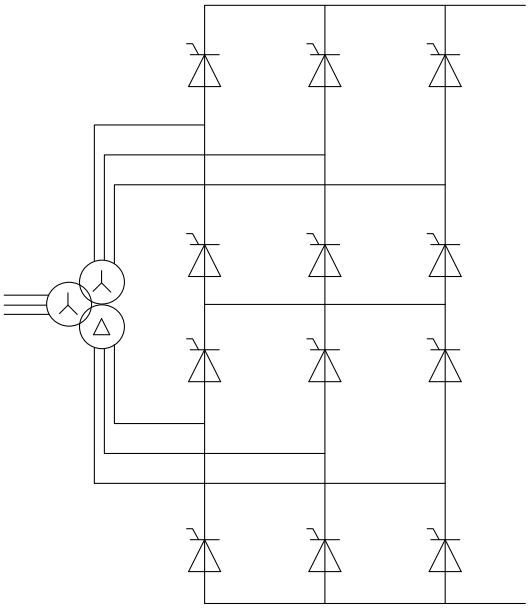


Fig. 2. 1 Twelve-pulse bridge LCC.

2.1.2 VSC-HVDC

VSC-HVDC systems use insulated gate bipolar transistors (IGBTs) as the main switching devices, which can be fully controlled for turn on and off independently of the external AC voltage. The significant advantages provided by VSC-HVDC comparing with LCC-HVDC for the future AC-DC hybrid power networks are described as [31-34]:

i. Ability to deliver power for passive network.

ii. No reactive power compensation requirement.

iii. Flexible power reversal control without polarity change of DC voltage.

The early stage VSC-HVDC system used 2-level VSC topology as illustrated in Fig. 2.2. High frequency switching using pulse width modulation (PWM) technique was used for the VSC-HVDC to generate AC voltage output with reduced harmonic distortion comparing to the LCC-HVDC [32].

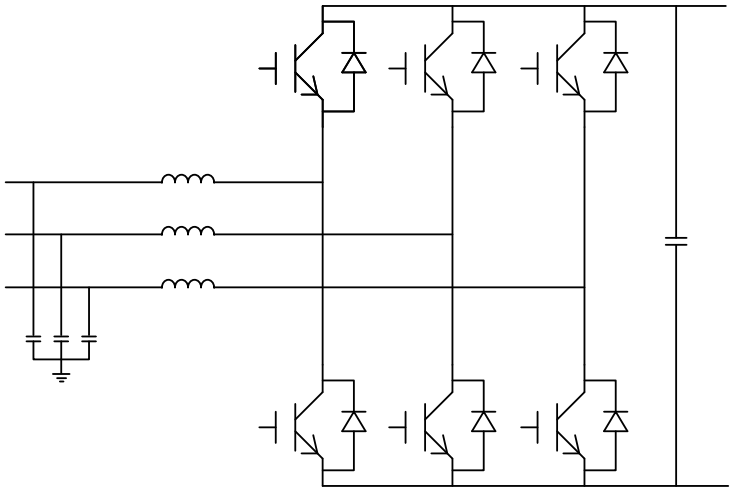


Fig. 2. 2 Two-level VSC.

However, with high switching frequency, earlier VSC-HDC has high power loss comparing to LCC-HVDC. Moreover, the severe electromagnetic interference generated by switching 2-level VSC limits its feasibility for implementation in systems with very high voltage level [35].

HVDC systems using the modular multilevel converters (MMC-HVDC) in which large numbers of sub-models (SMs) are connected in series, as shown in Fig. 2.3 (a), was first proposed in [36] in 2003 and has attracted wide interests in recent years. It provides following advantages comparing with 2-level VSC-HVDC [35-38]:

i. Reduced switching frequency leads to lower power loss

ii. Great improvement on the harmonic contents

iii. No requirement for the large DC-link capacitors

iv. Improved electromagnetic interference

v. Flexibility for different voltage levels

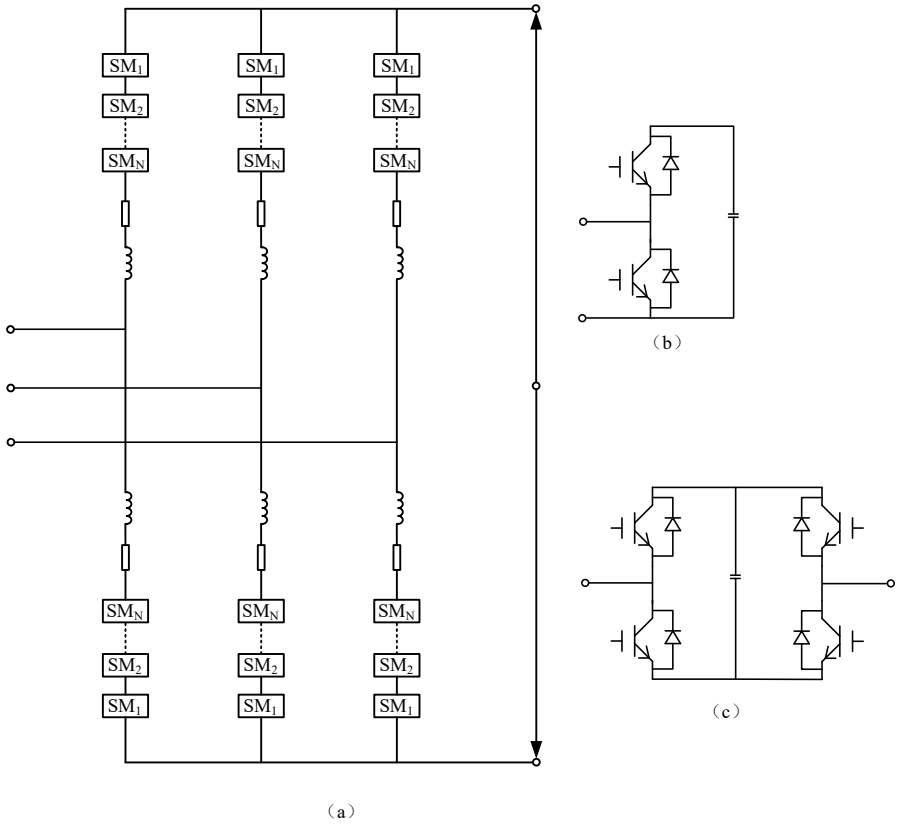


Fig. 2. 3 MMC and two submodule topologies.

The most commonly implemented SMs are the half-bridge (HB) SM and full-bridge (FB) SM, as shown in Fig. 2.3 (b) and (c), respectively. Comparing with MMC based on HBSM, the MMC based on FBSM can provide more control flexibility with ability to output negative DC voltage. Therefore, it has ability to block fault current in the event of DC faults, while HB-MMC will operate under freewheeling state providing path for fault current injection from AC side to the DC fault [39, 40]. Although FB-MMC increases

SM losses due to the increased number of SMs, the DC fault block capacity may still make it attractive for some applications as fast and reliable commercial manufacture of DCCB is not mature yet and their cost is likely to be high.

Table 2. 1 Comparison between LCC-HVDC and VSC-HVDC

	Advantages	Disadvantages
LCC-HVDC	• Large transmission capacity • Low cost with high reliability • Low power loss and high efficiency • Mature technology	• Requires AC source for commutation • Needs reactive power compensation • Change of voltage polarity during power reversal • Needs large AC filters leading to large converter footprints
2-level VSC-HVDC	• Ability to deliver power to passive network • Ability to provide reactive power compensation • Power reversal without polarity change of DC voltage	• High switching frequency leading to high loss • Severe electromagnetic interference • Difficulty for DC fault protection
MMC-HVDC	• Reduced switching frequency leading to high efficiency • Good AC waveform quality and no AC filter required • No requirement for the large DC-link capacitors • Modular design and high flexibility for different voltage levels	• Large volume of SMs leads to complex control system • Large converter valve hall • High capital cost

2.2 Frequency support

The system ability of frequency regulation is mostly depending on two aspects which are system inertia and frequency regulation capacity of generations [41]. In order to deal with the problem of nowadays energy crisis and worsening environment pollution, green energy such as wind farm and solar power generation is expanding rapidly with limited frequency regulation capacity and reduce the overall power system inertia with their increased penetration [42-44]. Therefore, the power system frequency stability becomes a problem for the future power grid. The frequency support strategies are reviewed from two aspects as frequency support based on renewable power generations and frequency support based on HVDC system.

2.2.1 Frequency support based on wind turbine control

Because most wind farms are connected to the power grid through power converters which de-coupled them from each other, frequency support from wind power generation is achieved by emulating inertia and ancillary frequency response control through regulating the wind turbine rotor speed, output power etc. [45] .

In [46], the overproduction and underproduction ability of the variable speed wind turbine control is utilized to provide the initial frequency support. The results show that 5% additional output power can be achieved for 10s. The same method is used in [47] and the overproduction is improved to 20% for 10s. However, in both cases, the results are highly limited by the overproduction or underproduction level and the wind condition. In another researches [45, 48], a method of controlling the conversion system of the variable wind speed turbine generator is introduced and tested which is able to make the turbine working at the de-loading status to provide 20% additional output power. It is achieved by regulating the generator speed during the frequency event to release the kinetic energy stored in the rotating mass. The regulating of generator speed is determined by frequency deviation through droop control loops. However, the rotation speed has to be recovered after the frequency support.

2.2.2 Frequency support based on HVDC system control

A VSC-HVDC link integrating large AC grids also has its own potential frequency support capability with its advantage of highly controllable and flexible power flow. However, as frequencies of the two AC networks connected by a HVDC link are decoupled, frequency transition at one AC network does not appear naturally on the other AC network. In addition, for potential frequency support using VSC, it is necessary that additional energy can be available for VSC active power modulation according to the variation of the frequency of its connected grid. Two different concepts, one uses the VSC to artificially couple the remote infeed with AC grid such as virtual synchronous techniques [49, 50] and the other uses the energy stored in the VSC DC capacitors, have been proposed to provide inertia response and virtual power generator using droop control based on local frequency [51, 52].

i. Frequency support based on coupling remote network with main grid

One of the ways to couple both sides of a HVDC link is to express the frequency change at the AC grid of the remote side (e.g. offshore wind farm or another AC grid) through the variation of the DC voltage and converter control. The basic control concept [53-55] is illustrated in Fig. 2.4.

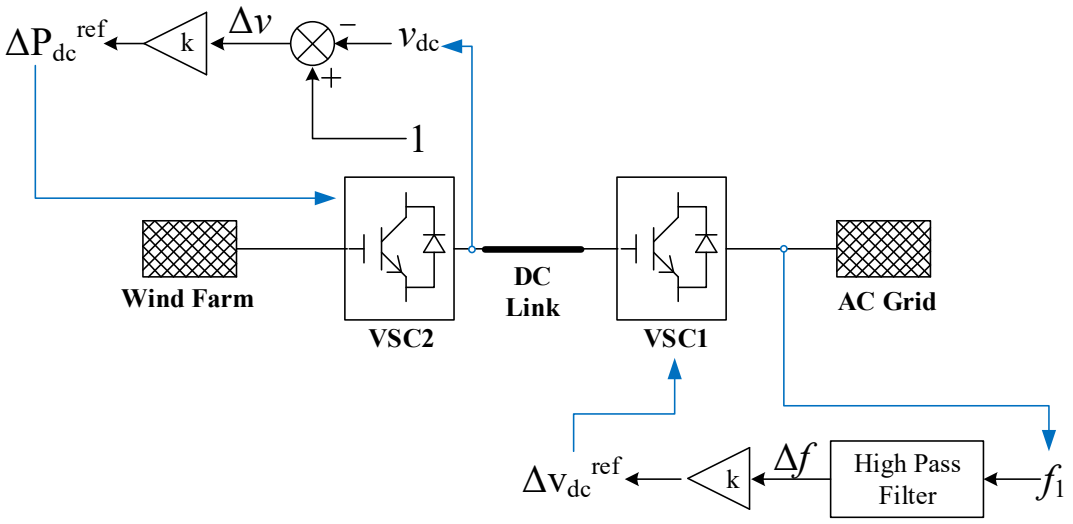


Fig. 2. 4 The basic control concept of systems coupling through HVDC link.

From Fig. 2.4, VSC1 controls the DC voltage while VSC2 controls the active power from the wind farm. Frequency of the AC Grid side is monitored and the frequency deviation during frequency events is used to regulate the DC voltage control reference at VSC1 in a small range of, e.g. 0.05pu, which is proportional to the frequency deviation. On the VSC2 side, the deviation of the DC voltage variation is measured, and the active power control reference is modified accordingly. In this way, the power output from remote infeed side can be regulated according to the frequency at AC grid side with all variables measured locally. For instance, a frequency drop makes a small drop on DC voltage through VSC1 and then the voltage drop increases the active power output from remote infeed side through VSC2 to provide frequency support. Obviously, in order to provide additional active power, the network connected to VSC2 has to have the capability to supply additional power/energy when required. Therefore, if VSC2 connects to an offshore wind farm, methods outlined in Section 2.2.1 have to be implemented at the wind farm level.

In [16], the flexibility of power control of VSC is used to re-dispatch active power in a MTDC system, in order to share the power shortage between different terminals to provide improved overall frequency behavior during frequency event on one terminal. However, the power sharing strategies between the different supporting terminals are not considered during frequency event at one AC terminal. For example, more power should be shared by the terminals with higher grid capacity than others connected to AC networks with smaller capacity.

ii. Frequency support based on the VSC DC capacitors

Instead of using the VSC-HVDC to achieve the coupling between the remote infeed and the main AC power grid, some researches focus on using the energy stored in the shunt capacitors of the VSC-HCDC link to provide potential system frequency support. In [56] and [57], an approach called inertial emulation control (INEC) strategy for VSC-HVDC transmission system is presented. The primary frequency control and the inertial support capabilities for the VSC-HVDC system are achieved by using the energy stored in the shunt DC capacitors of the HVDC systems to offset the frequency fluctuations from the AC grid side after disturbances. By means of INEC, the VSC-HVDC system is

enabled to provide frequency and inertia support just in an emulated way refer to the conventional synchronous generators. In order to set up the relationship between the system frequency deviation and the shunt capacitors stored energy deviation, a virtual inertia time constant of VSC system H_{VSC} was presented as [57]:

$$\frac{NCV_{DC}}{S_{VSC}} \cdot \frac{dV_{DC}}{dt} = \frac{2H_{VSC}}{f_0} \cdot \frac{df}{dt} \tag{2.1}$$

where N is number of VSC DC capacitor employed, C is the capacitance of VSC DC capacitor, V_{DC} is the DC voltage, S_{VSC} is the VSC normal capacity, f and f_0 are the system frequency and the rated system frequency respectively.

Thus, the frequency deviation on the AC side is coupled with the power deviation of the VSC DC shunt capacitors which can be controlled by regulating the DC voltage. By this mean, if the shunt capacitance is sufficiently large enough, it can contribute additional active power/energy by varying DC voltages. However, the main constraint is that the frequency support capacity of such control is limited by the size of DC link capacitor. An equivalent DC capacitor of 7.5mF at ±300 kV (for a 300 MW HVDC link) was used in the simulations which is relatively large comparing with practical systems.

Further work has been presented in [58], which combines the DC capacitor energy and additional energy from the connected wind farm to further improve the overall system behavior during the frequency events. The frequency support from wind farm is provided through communication with the onshore AC grid. For a case of load increase at the onshore AC grid, the DC voltage is reduced to release the energy stored in the VSC DC capacitors to give fast primary frequency support until the wind farm initiated respond. However, the same issues of limited energy storage on the DC capacitors and difficulties in initiating active power response from wind farms exist.

2.3 DC Fault Characteristics

Due to the low impedance nature of DC networks, in the event of a fault on DC lines, there can be very rapid increase of DC fault current coupled with reduction of DC voltage. The typical characteristics are discussed below for systems employing HB-MMCs [20, 59-62].

Taking a permanent DC pole-to-pole fault for instance, in the first stage, the DC voltage at the fault location drops rapidly although the converter can still remain controlled by providing nominal AC voltage [63]. The reduction of MMC terminal DC voltage leads to the discharging of SM capacitors, and the converter starts to loss control on the AC voltage and current. Thus, AC fault current starts to flow from the AC grid [64, 65]. Once converter detects the fault and is quickly blocked, the SM capacitors are bypassed, and the converter is working as an uncontrolled diode rectifier. The fault current is continuously fed by the AC grid through the diodes of the SMs [66] leading to high AC and DC fault current.

Typical waveforms are shown in Fig. 2.5 to illustrate the DC fault current characteristics with a pole-to-pole DC fault happened at t=8s and the converter blocked at t=8.005s. As shown in Fig. 2.5 (a), the DC terminal voltage drops to under half of its nominal value rapidly after fault occurrence. Meanwhile, the AC voltage and current maintain largely un-disturbed in the initial stage as shown in Fig. 2.5 (c) and (d) before converter blocked after 5ms. After converter blocking, the AC voltage is uncontrolled and the AC current increases to contribute to the DC fault current through the SM diodes. The DC fault current shown in Fig. 2.5 (b), rapidly increases to over 5pu before converter blocking, and continues rising to almost 10pu due to the fault current contributed by the AC grid.

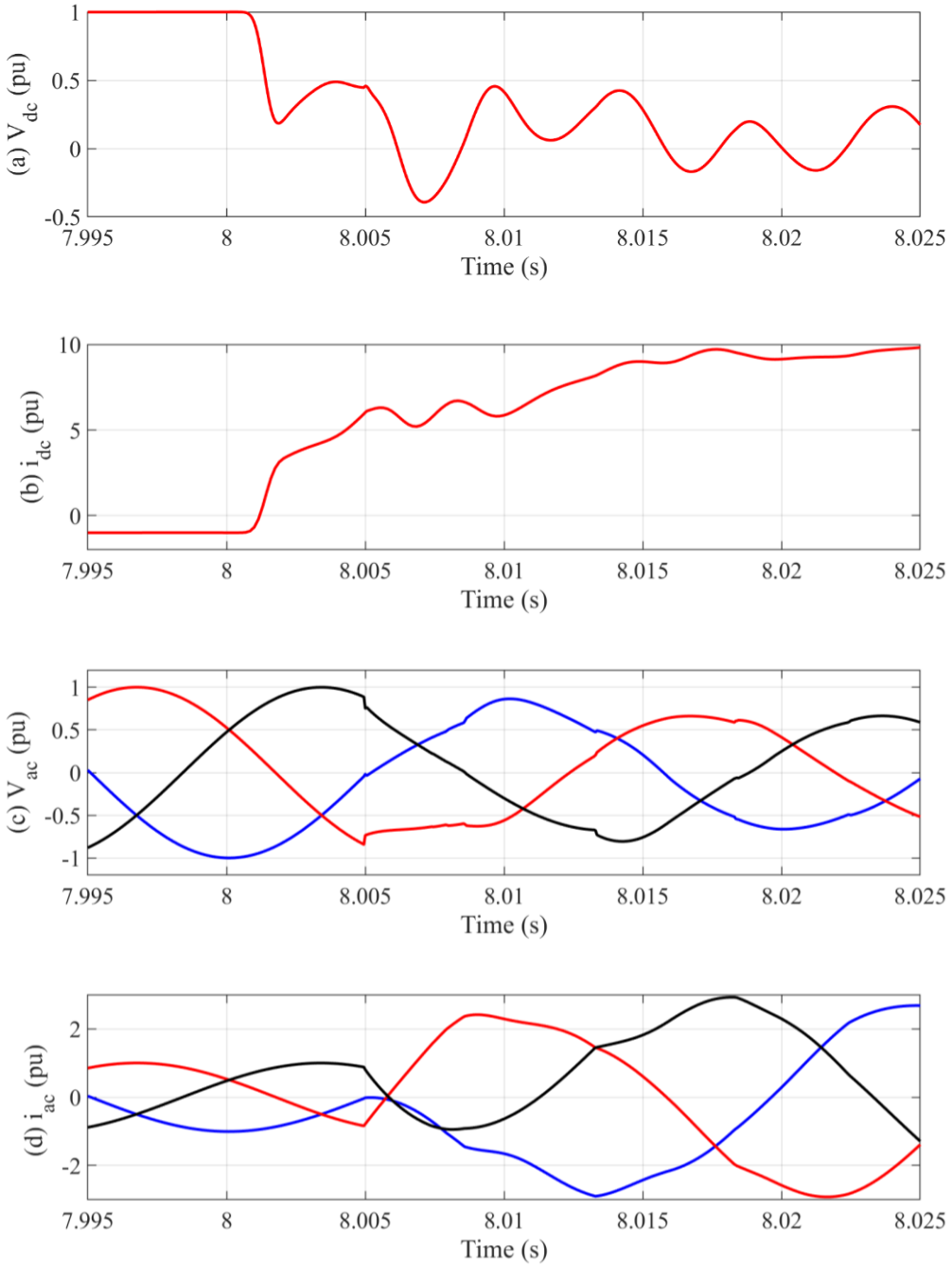


Fig. 2. 5 Waveforms at AC and DC terminal of VSC for typical DC fault current characteristics: (a) DC voltage, (b) DC current, (c) AC voltage and (d) AC current.

2.4 DC Circuit Breaker Technology

Interrupting DC current is more difficult than that of AC current due to inherent absence of current zero crossing, and thus the mature technique of arc extinguishing is not applicable to DC fault current interruption. Meanwhile, the huge energy stored in the conductive components on the DC network increase the difficulty of DC current interruption. As described earlier, low DC impedance makes the rate of rise of fault current very high, and thus it requires high speed fault current interruption. Therefore, the two focuses when investigating DCCBs are on the interruption of DC fault current and arc extinguishment, and absorption of the residual energy stored in the DC network.

2.4.1 Main Requirements of DCCBs

Considering the application environment of DCCBs, their requirements are significantly different to those of ACCBs.

i. High voltage and current capacity. Due to the fast rise of fault current, and continuous increase of the voltage and power ratings of DC system, DCCBs are required to break current up to tens of kilo-amperes.

   High operation speed. Due to the fast rise of fault current and large fault current, the operation speed of DCCB large determines the requirements of tolerance of fault current for other components in the DC network. Thus, typically DCCBs are required to operate within a few milliseconds.

ii. High reliability and economic

   It is different from AC fault current interruption, delayed DC fault current interruption can significantly raise the fault current peak causing serious consequences to the equipment in the whole DC network. Therefore, high reliability of DCCBs is critical.

   Low power loss. During normal operation, the power loss of DCCBs should be low.

Economic design. As large scale MTDC network requires large amount of DCCBs, the costs of BCCBs are thus significant for their adoption in future high voltage and high capacity MTDC systems.

The current technologies of DCCBs can be largely classified as mechanical DCCB, Solid-state DCCB and hybrid DCCB.

2.4.2 Mechanical DCCB

Mechanical DCCBs use ACCBs as the current interruption unit and it is implemented with different assistance branches to extinguish the electrical arc to achieve fault current interruption. It has the advantages of low loss under normal operation and high capacity of large current interruption. However, the operation time is long.

Since there is no inherent zero-cross point in DC fault current, the generation of current zero-cross point for mechanical DCCB interruption unit is required. Depending on the method to generate the current zero crossing, mechanical DCCBs can be classified by the ways of artificial zero-cross point generation as self-excited oscillation, pre-charge oscillation and coupled-inductor circuit.

i. Self-excited oscillation

The circuit diagram of DCCB based on self-excited oscillation is shown in Fig. 2.6 comprising a mechanical circuit breaker (CB), an opposite current generation branch (capacitor C and inductor L connected in series) and an energy absorption branch (ZnO surge arrestor) [67, 68].

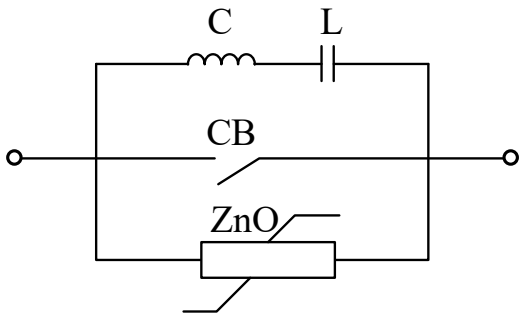


Fig. 2. 6 Circuit diagram of DCCB based on self-excited oscillation.

During normal operation, the current flows through the mechanical circuit breaker branch. When the current interruption initiated, the CB starts to open and generates an electrical arc. The negative resistance characteristic of electrical arc makes the opposite current generation branch to generate oscillation current with increasing amplitude flowing to the CB branch thereby generating the current zero-cross point. With the zero-cross point generated by the oscillation current, the electrical arc is extinguished, and CB is able to fully open. Then the residual energy in the DC network is consumed by the surge arrestors in the energy absorption branch.

The mechanical DCCBs based on self-excited oscillation have advantages of simple topology, low loss and cost, relatively small footprint and easy to be controlled and implemented. However, the generation of zero-cross point normally takes tens of milliseconds and thus the operation speed is low. Moreover, weakening of the negative resistance characteristic of arc with the increasing arc current makes the amplitude of the oscillation current insufficient to generate the zero-cross point on the CB branch. This indicates that the current interruption capacity of this kind of DCCBs is limited.

In 1980s, a 500kV/2kA mechanical DCCB based on self-excited oscillation is produced by Brown Boveri Corporation (BBC), and was field tested at the CELILO converter station on the Pacific Northwest-Southwest HVdc Intertie [69, 70].

ii. Pre-charge oscillation

The circuit diagram of DCCBs based pre-charge oscillation is shown in Fig. 2.7 comprising a mechanical CB, an opposite current generation branch (capacitor C pre-charged with revers voltage, inductor L and switch K connected in series) and an energy absorption branch.

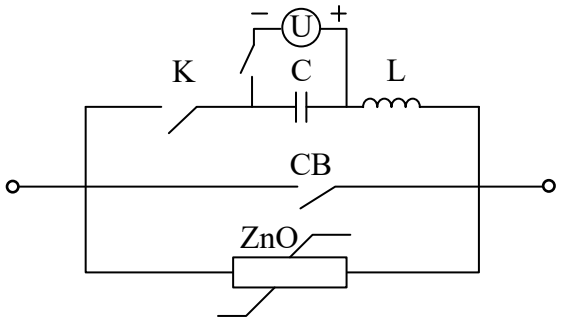


Fig. 2. 7 Circuit diagram of DCCB based on pre-charge oscillation.

When the current interruption is initiated, the CB starts to open and generates an electrical arc. Then the switch K is closed, the pre-charged LC circuit generates reverse current flowing to the CB branch. With the zero-cross point generated by the revers current adding to the CB branch, the electrical arc is extinguished, and the CB is able to fully open. The residual energy in the DC network is also consumed by the energy absorption branch.

The mechanical DCCB based on pre-charge oscillation circuit is suitable for the high current interruption compared with that based on self-excited oscillation. In 1972, a 80kV/30kA DCCB based on pre-charge oscillation and vacuum CB was produced by GE company [71], and a 250kV/1.2kA DCCB based on pre-charge oscillation and SF_6 CB was produced by Toshiba Corporation in 1984 [72]. In the next year, a DCCB base on same principle with higher current interruption capacity of 250kV/8kA, was introduced and lab-tested by Hitachi, Ltd. [73]. Most recently, Mitsubishi Electric Corporation announced on October of 2019 the development of an 160kV mechanical DCCB prototype which is able to interrupt a peak current of 16kA within 7ms [74].

Faster operation speed can be achieved by the DCCB based on pre-charge oscillation compared to that on self-excited oscillation. However, the additional units of power supply for pre-charging the capacitor and the switch K increase the overall cost and control difficulty. In addition, the typical operating speed of mechanical DCCBs is in the order of tens milliseconds.

iii. Coupled-inductor circuit

The key to generating zero-crossing point is to inject reverse current into the main CB branch. A coupled-inductor circuit is proposed rather than oscillation circuit as shown in Fig. 2.8. [75-78]

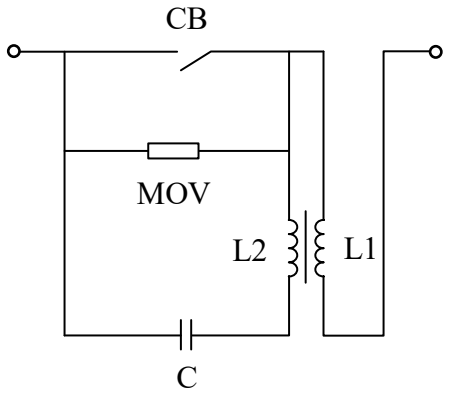


Fig. 2. 8 Circuit diagram of DCCB based on coupled-inductor circuit.

As shown, the reverse current generation branch is composed by a coupled-inductor L_2 and a capacitor C. When current interruption initiated, the fast-increasing fault current flowing through coupled-inductor L_1 generates current on L_2 with opposite direction of the fault current. Thereby, the superposition of those two currents with opposite directions generates the current zero-cross point on the CB branch. Therefore, the arc can be extinguished, and the CB can be fully opened to finalize the fault current separation. The current research on this type of DCCB is focused on fast operation time and low total cost. However, how to increase its voltage capacity becomes a challenge and further researches are required.

2.4.3 Solid-state DCCB

In 1970s, with the development of power electronics technology, the silicon-controlled rectifier (SCR) started to be used as the separation units in DCCBs. With the

birth of full control semiconductor device in the 1980s, solid-state DCCBs have developed rapidly [79-81].

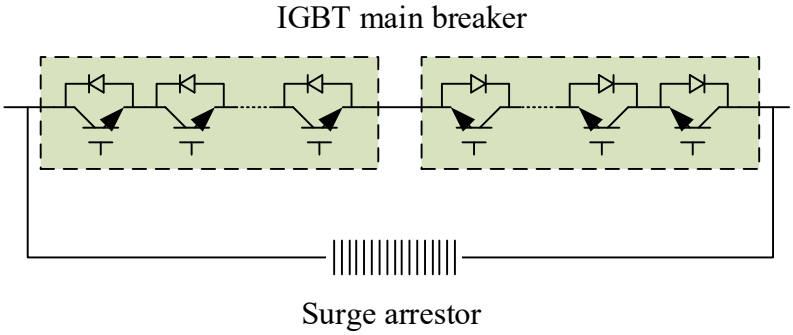


Fig. 2. 9 Simplified basic structure of pure solid-state DCCB [59].

The basic simplified structure of a solid-state DCCB is illustrated in Fig. 2.9 comprising a solid-state power electronic switch (IGBTs and IGCTs) branch (main breaker) and an energy absorption branch (surge arrestor). Under normal system operation, the current flows through the solid-state power electronic switch branch. When fault current interruption initiated after fault detection, the power electronic devices on the switch branch switch off to rapidly separate the circuit. Then the residual energy in the DC network is absorbed by the energy absorption branch to finalize fault current interruption. Thus, super-fast switching speed can be achieved by solid-state DCCBs.

However, due to the low voltage and current capacity of a single power electronic switch, large number of switches are connected in series in order to fulfil the requirement of high voltage and current capacity. This may lead to large footprint of DCCB stations, complex structure and control with increased cost. Meanwhile, the large on-state loss of the solid-state DCCB limits it implement in the HVDC system with high voltage and capacity.

The optimization of pure solid-state DCCB is still on-going. A freewheeling diode is used to reduce the surge voltage in order to optimize the power loss in [82]. In [83], the

energy absorption and overvoltage protection are separated and connected with a large and small varistor, respectively, in order to prevent from uncontrolled overvoltage.

2.4.4 Hybrid DCCB

Since the 1990s, hybrid DCCBs comprising power electronic devices and mechanical CBs have become a hot research spot. This type of DCCB makes full use of the current-carrying and insulating capacity of the mechanical switch and the fault current interruption capacity of the solid-state switch to achieve DC current interruption [84-87].

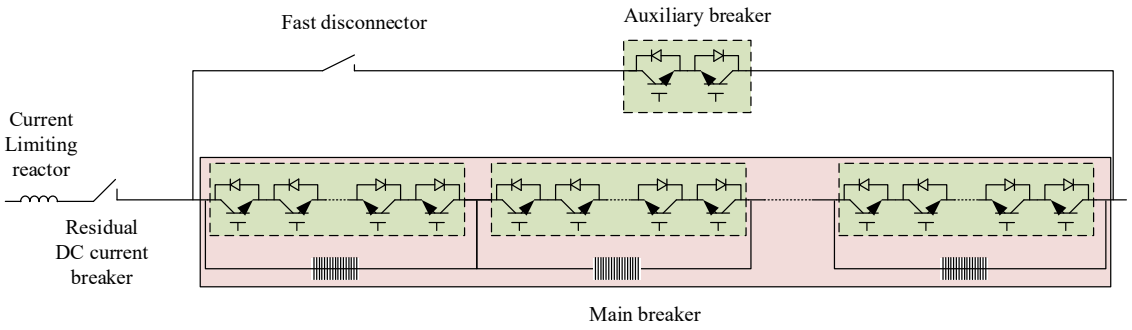


Fig. 2. 10 Simplified basic diagram of the hybrid DCCB based on forced current commutation [88-90].

The simplified basic diagram of a hybrid DCCB is shown in Fig. 2.10, which comprises a current commutation branch, a high voltage solid-state power electronic switch (IGBTs and IGCTs) branch and an energy absorption branch (main breaker). The current commutation branch contains a mechanical CB (fast disconnector) and low voltage solid-state current commutation switch (auxiliary breaker). Under normal operation, both the current commutation branch and the high voltage power electronic switch branch are closed, though the system current is carried by the current commutation branch due to its lower impedance than the other. When DC fault current interruption initiated, the solid-state switch on the current commutation branch switches off and thus the fault current is commutated to the solid-state switch branch. The mechanical CB can

then be opened at zero current. After the specific separation distance at the mechanical CB is achieved, the solid-state high voltage switches open and the fault current flows to the energy absorption branch to finalize the fault current interruption.

This type of DC circuit breaker makes full use of the current-carrying and insulating capacity of the mechanical switch and the fault current interruption capacity of the solid-state switch to deliver high speed fault current commutation and interruption. As the high voltage solid-state switches do not carry current during normal operation, the power loss of the hybrid DCCBs is very low when compared to that of the solid-state DCCBs. Similar to pure solid-state DCCBs, large numbers of power electronic devices are required leading to high complexity of control and high cost, which limit its implantation in practical systems.

A 10kA hybrid DCCB prototype using IGCTs and mechanical CB was tested and reported in [91]. In 2012, a 320kV/2.6kA hybrid DCCB using IGCTs was proposed by ABB with current interruption capacity of 9kA in 5ms [92-94]. A 200kV/2kA hybrid DCCB, which is able to interrupt fault current of 15kA in 3ms, has been developed by China State Grid and implemented in Zhoushan 5-terminal ±200kV MMC-HVDC project [95]. The same DCCB technology has been further developed and implemented at Zhangbei 4-terminal ±500kV MMC-HVDC project [96].

2.4 DC Fault Detection and Location

Unlike the AC systems, many traditional AC protection techniques, especially impedance-based methods, are unable to be used to protect DC systems due to its near-zero reactance and low resistance. Meanwhile, this characteristic makes DC fault protection a more severe challenge because of insufficient ability of limiting high rate-of-rise of DC fault current when a DC fault happens. Meanwhile, in the large HVDC network, the fault is expected to be detected and isolated quickly so the healthy part can continually operate. Therefore, DC protections including fault detection and location need to be very fast, e.g., within a few milliseconds [97-100]. If fast DC protection cannot be realised, the HVDC systems (especially converters) have to be designed to withstand the fault (with

high fault current) for a considerable time and the interruption of power transmission during such events has to be manageable for the connected AC networks. This is the approach adopted in most point-to-point HVDC systems where conventional AC protection techniques have been used for DC fault protection. However, such protection arrangement is insufficient in operation speed and selectivity for protecting large MTDC grid. Various methods, such as signal-processing based, traveling wave based, wavelet based and artificial neural network based methods have been developed to improve the DC system protection more specifically.

2.4.1 Overcurrent/Current Differential Protection

Overcurrent protection is widely used in both AC and DC systems due to its simple equipment and control. It is a straightforward method using local measurements without the necessity for fast communication among relays. However, the drawback of low accuracy in fault location discrimination makes overcurrent protection unsuitable as a main protection for a DC grid [101]. In DC protection, the thresholds of overcurrent protection are always set at a high value in order to prevent from mis-tripping circuit breakers of healthy zones, which delays protection operation and leads to higher fault currents. Therefore, overcurrent protection is normally employed as backup protection and to protect converter components in HVDC systems [59]. The inverse time overcurrent protection (ITOP) is implemented in a 3-terminal HVDC network proposed in [102]. The DC terminal inductors are added to reduce the DC fault current rising rate in order to imitate the AC environment for the ITOP. However, the relay on the cable terminal closing to the fault respond faster than the other side one and their cooperation is not clear. Meanwhile, the performance of such protection highly relies on the size of the integrated inductors.

Similar to overcurrent protection, current differential protection is well developed and often employed in AC system. However, in DC systems, since communication among relays is required and due to fault current traveling speed in DC lines, communication delay becomes a significant issue. Meanwhile, due to capacitive current and low inductance of DC cables, the reliability and selectivity of current differential protection using in DC system is not sufficient [103, 104].

2.4.2 Derivative/Transient Based Protection

To use voltage derivative protection in DC systems, due to the low inductance of DC cables, additional inductance is required at each end of the DC lines in order to discriminate internal and external faults [105]. When a DC fault happens in a MTDC grid, the voltage derivative of terminals that are close to fault location will be higher than those that are far away. Therefore, voltage derivative can be used as a fault indicator to discriminate internal and external faults with advantages of communication-less and only requiring local measurements.

Other fault indicators such as transient DC voltage, DC current and current derivative are tested and compared with voltage derivative together in [105], considering the dependability, speed, security and selectivity under different fault scenarios. Simulation results show that derivative based protection gives better and faster response with higher reliability when indicating fault locations than the others. However, the size of the added DC inductors has significant effects on protection sensitivity and security and needs to be carefully designed. Meanwhile, faults with high resistance to the ground will deteriorate detection performance.

In [106-108], similar idea of a communication-less protection scheme based on transient DC fault current, using single end local measurement is proposed. With a DC filter and a smoothing reactor at both ends of each DC line, the component of transient DC fault current with specific frequency is extracted and can be considered as the fault indicator to discriminate internal and external faults. However, the reliability and selectivity highly depend on the system configuration and parameters especially the sizes of the smoothing reactors and DC filters. Meanwhile, fault resistance has also significant influence on the selectivity of this protection scheme. Methods using transient DC voltage during fault with specific frequency as fault indicator are proposed in [109, 110]. Similar protection effectiveness is got as acting to fault in several milliseconds. Another similar communication-less protection scheme based on transient voltage, is presented in [111]. It uses the ratios of the voltages across the inductors at both ends of each DC line to indicate internal or external DC line faults. This method is very simple as it uses local measurements with no need of communications, though it requires sizeable DC inductor

for good selectivity whereas large inductors add extra cost and power loss in addition to reducing system dynamics. Meanwhile, the performance in meshed MTDC system is untested as all the studies were carried out in redial multi-terminal DC systems.

2.4.3 Traveling-Wave Based Protection

The main drawback of voltage based protection for DC transmission lines is the reliability of protection is very sensitive to fault impedance [112]. Traveling-Wave based protection technologies have shown significant advantages over voltage-based protection technologies. When a fault occurs on a DC line, abrupt changes in electrical quantities introduce electromagnetic waves traveling along the line in both directions from the fault point. Relays at the ends of DC line detect and record the arrival times of these travelling waves and analysis them in order to extract the information of fault location. The traveling-wave based protection methods contain technologies of traveling wave detection, wave front acquisition and different signal processing methods such as Fast Fourier Transformation (FFT), Discrete Wavelet Transformation (DWT) and Continuous Wavelet Transformation (CWT) [113-116]. The basic principle of traveling wave based protection is illustrated in Fig. 2.11

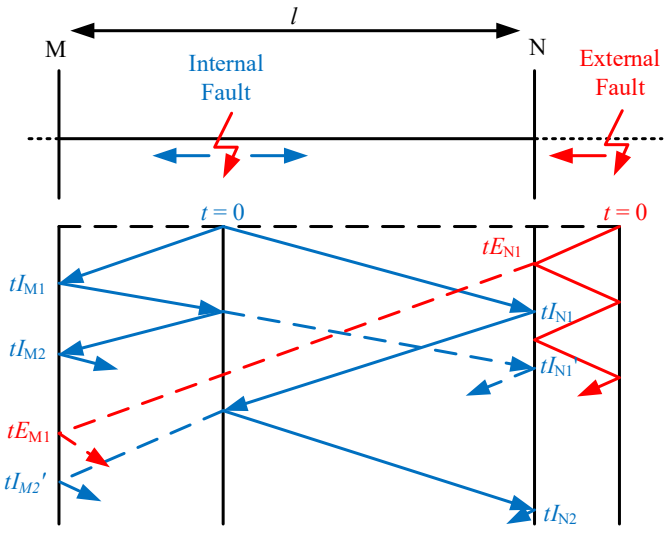


Fig. 2. 11 Basic principle of traveling wave based protection [117].

The traveling wave based protection methods can be categorized as one- and two-terminal methods [118-120]. One-terminal methods uses difference of arrival times between the first-arrived-wave and its reflection wave (e.g. tI_{M1} and tI_{M2} shown in Fig. 2.11) from the fault point to calculate the distance from the fault point to the relay. It can provide fault location very quickly in terms of milliseconds with no need of communications between relays [121, 122]. However, it requires complex signal processing methods and detection equipment to distinguish and receive the damped reflection waves from fault points, local terminal and remote terminal. In this case, these schemes inherently have a problem of locating faults that are on or close to the line terminals.

Two-terminal method is relatively simple and direct as relays at both terminals of DC line use the difference of arrival times of their first received waves to calculate the fault location (e.g. tI_{M1} and tI_{N1} shown in Fig. 2.11). The traveling wave can be recognised by relays as high frequency components of terminal voltage [117]. This time difference is used with wave propagation velocity (c) to calculate the difference of travel distance of two first-arrived-waves. If the travel distance difference is shorter (e.g. $| c * tI_{M1} - c * tI_{N1} | < l$) or longer (e.g. $| c * tE_{M1} - c * tE_{N1} | \geqslant l$) than the entire protected line length, the fault will be considered as internal fault or external fault respectively [123]. However, because of the high speed travelling wave propagation, high speed communication between relays at two terminals is required to reduce the error of arrival time difference. This problem is improved by using global positioning system (GPS) to provide a unified time reference for both relays. Another shortfall limiting the implementation of traveling wave based protection schemes is the requirement of high frequency data sampling (up to several MHz) and storage, as its reliability and accuracy are highly depending on the data sampling frequency [124]. In fact, the fault location accuracy can be tripled by increasing the sampling frequency from 500 kHz to 1 MHz. Meanwhile, fault location based on traveling wave is more challenging as it requires complicated data analysis algorisms [125].

2.5 DC Fault Protection Strategies for VSC-HVDC System

Based on the protection concept and equipment used, DC fault protection can be considered into two different categories. The first one is based on the use of protection equipment (i.e. circuit breakers) to break the fault current whereas the second uses fault blocking MMC converters to extinguish the fault current.

2.5.1 DC Fault Protection Based on Circuit Breaker Technologies

For the existing two-terminal VSC-HVDC systems, system protection replies on the opening of ACCBs in the event of a DC fault while the converter is blocked. Thereby, power source on the AC side is isolated from the DC fault upon the opening of the ACCBs, and the DC fault current drops gradually. After the residual energy on the DC network is consumed by the components on the DC network, if the fault is temporary, the ACCBs can be re-closed and the system recover (converters de-block, DC voltage re-build and power flow recover) can be initialled. Alternatively, DC disconnectors/switches installed at the converter DC terminals can be opened (at zero DC current) to isolate the faulty branch. Such strategy can be achieved easily with simple equipment and control, providing good reliability. However, the blocked converter acts as a diode rectifier and the diodes inside the converters have to be designed to withstand high fault current for a considerable time (e.g., tens of millisecond). This necessitates the use of additional protection devices in the SMs of the MMC such as thyristors or fast vacuum switches [126].

A handshaking protection method based on the use of ACCBs and DC switches (DCSWs) is proposed for a meshed MTDC network in [23], which is the method that employed in Chapter 5 to identify and isolate the faulty branch in the proposed system. The basic idea of the handshaking protection method is illustrated in Fig. 2.12.

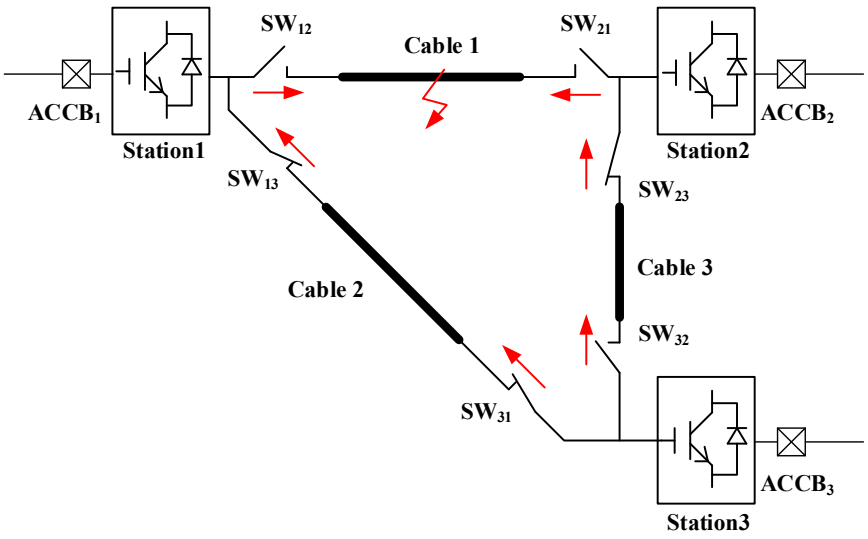


Fig. 2. 12 Diagram of 'Handshaking' approach [23].

With the 'Handshaking' approach, when a DC fault happens, the DC fault current flowing through SWs are labelled depending on their directions. For example, the fault current is regarded as positive when flowing into the cable, and negative when flowing out of the cable. The selected SWs whose detected fault current are positive are considered connecting to potential faulty lines, and are opened to isolate the faulty area. However, if multiple positive cable current is detected by one station, only the SW with the largest positive current is selected to open. For example, when a fault happens on Cable 1 with fault currents (red arrows) shown in Fig. 2.12, the DC fault current will be labelled as positive at SW_{12}, SW_{21}, SW_{31} and SW_{32}, and thereby SW_{12}, SW_{21} and SW_{32} (with higher fault current than that of SW_{31}) are respectively selected by Station 1, 2 and 3 to be opened. Meanwhile Cable 1 and Cable 3 are considered as potential faulty lines. In order to restore power transmission after fault isolation, the opened SWs connecting to the healthy cables will need to be reclosed when reclose conditions are fulfilled. This is achieved by detecting the SWs whose voltage on both sides recovers during restoring process to be reclosed. In the restoring process, SW_{32} will be reclosed when the voltage on both sides are recovered (as voltage only appears on one side of SW_{12} and SW_{21} so they are Cable 1 is determined as the faulty cable).

However, the low resistance on the DC network leads to slow DC fault current reduction after the ACCBs are opened. Thus, fault isolation and system recovery are slow resulting in a prolonged down time of the whole DC system which could severely affect the connected AC networks (e.g. AC frequency) [127-130].

In order to solve such problems, DC fault protection based on fast acting DCCB technologies have been developed and installed. The fast acting DCCBs (e.g. solid-state DCCB and hybrid DCCB) are able to interrupt DC fault current and isolate faulty line very quickly, without the need to open ACCBs. Hence, faulty lines can be isolated quickly and the current stress in the converters are significantly reduced compared to the previous ACCB based protection. Consequently, the healthy system (e.g. in a large MTDC setup) can quickly recover. However, the technologies of DCCBs, as reviewed in Section 2.4, are not fully mature with limited experience. Therefore, DC fault protection for large DC system with high capacity and voltage level relying on the DCCB is still a challenge [131].

2.5.2 DC Fault Protection Based on FB-MMC Converters

Due to the DC fault blocking capability, full-bridge (FB) SM based MMCs (FB-MMCs) have attracted much attention. By blocking all the semiconductor switches T_1 to T_4 in the FB SM shown in Fig. 2.13, the SM capacitor C_{SM} is inserted into the conduction path in negative polarity to the AC fault current pth so as to block the fault current flowing though the freewheeling diodes fed by the AC grid voltage [26, 27].

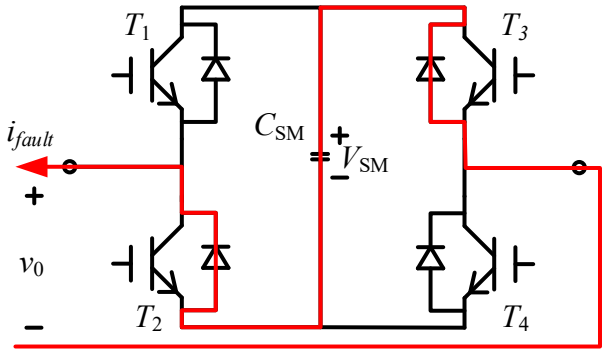


Fig. 2. 13 Fault current path when FB SM blocked [60].

FB-MMC has been proposed for HVDC link with overhead lines, e.g. the ULTRANET direct current project (±380 kV, 2 GW, Germany), where DC faults could occur relatively frequently compared to schemes using cables. FB-MMC stations can quickly extinguish fault current and deionize the arc, and provide fast restart after clearance of temporary faults to minimize power transmission interruption [132]. By simply blocking the FB-MMCs, the fault currents can be quickly suppressed to zero in point-to-point HVDC links [26, 27]. This method is also applied in the three-terminal radial DC network in [133]. After DC fault currents are suppressed to around zero by blocking all the FB-MMC stations, the DCSWs at the DC terminals of the faulty line can be opened for isolation.

Active control of DC fault current is proposed in [134] to regulate the common-mode voltages by adjusting the output of the FB-MMC circulating current controller. The proposed control is disabled during normal operation but is activated after DC fault occurrence to effectively suppress the DC fault current to zero. The basic idea of such control is shown in Fig. 2.14

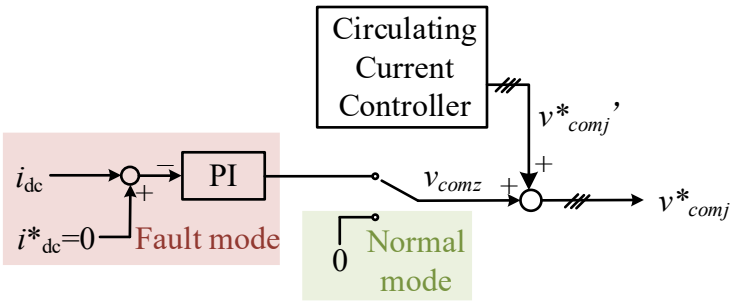


Fig. 2. 14 Control diagram of active control of DC fault current [134].

Similarly in [40, 135], the common-mode components of arm currents (i.e. half the sum of the upper and lower arm currents) are regulated by the SM capacitor voltage controller which also controls the DC current of the FB-MMC around zero during DC faults. An enhanced control is proposed in [136], to provide independent control of the

positive and negative poles of a symmetrical monopole FB-MMC during asymmetrical DC faults, to suppress the DC terminal current at zero during pole-to-pole DC faults. However, these active DC fault current control schemes have only been tested in simple point-to-point HVDC links and their validity in meshed DC grids remains unclear.

Reference [137] proposes a voltage polarity reversal control of a 2-terminal symmetrical bi-pole HVDC systems based on FB-MMCs. During pole-to-pole DC faults, the voltage of the negative pole is reversed from $-1/2V_{dc}$ to $1/2V_{dc}$, so as to become the same with the positive pole, while the neutral pole voltage remains 0. In this way, the rated DC power transmission can be maintained through the neutral wire during DC faults. However, in reality, it is likely that a pole-to-pole fault also shorten the ground so the proposed scheme becomes un-valid.

In [138], a low-energy protection system based on FB-MMC is proposed and tested in a 4-converter segment of the CIGRE B4.57/58 DC grid system, which contains a meshed section and a radial section [139]. Mechanical DCCBs are employed as fault interrupters. In such a large system, the fault current through the DCCBs on the faulty line will be large as fault current contributed by all four converters. The research focused on delaying the operation of DCCBs until the DC terminal current of all converters are controlled under 0.1pu, in order to reduce the energy dissipated in the energy absorb branch of DCCBs on the faulty line while operating. Therefore, the cost and the size of such DCCBs can be limited. However, as the current of the DC network is controlled to 0.1pu before DCCBs are opened, it takes extra 30ms, which reduces the benefit of using fast acting DCCBs (e.g. in several milliseconds) and leads to slow post-fault system recover. Meanwhile, controlling DC fault current to 0.1 pu (150A in the simulation cases) is almost equivalent to totally de-energize the DC network. Thus, the use of low cost DCSWs may become more beneficial.

The possibility of using DCSWs as fault interrupter is discussed in [140, 141], FB-MMC is used to control the DC fault current of the faulty line in a 4-terminal meshed DC network, which is then isolated using DCSWs. The general protection strategy is illustrated in Fig. 2.15. All FB-MMCs are initially switched to control the DC terminal current and once the fault line is located (e.g. using the various fault locating methods

introduced earlier), the FB-MMCs on both terminals of the faulty line are then switched to regulate the DC current on the faulty cable to zero.

This control can be well implemented in a radial multi-terminal HVDC (MTDC) system. However, in a meshed MTDC system, the voltage change on the healthy cables caused by the current control of the faulty line will weaken the control performance leading to slow DC fault current interruption. This problem will be further discussed in chapter 6.

Other than the FB-MMC, some other MMC topologies based on FB and HB SMs are introduced for providing fault current blocking whilst reducing the required switching devices and power losses, such as MMC based on double-clamp SM, unipolar FB SM, single-thyristor switch scheme, double-thyristor switch scheme, grid thyristor switch scheme and etc. [32, 35, 38, 142-145]

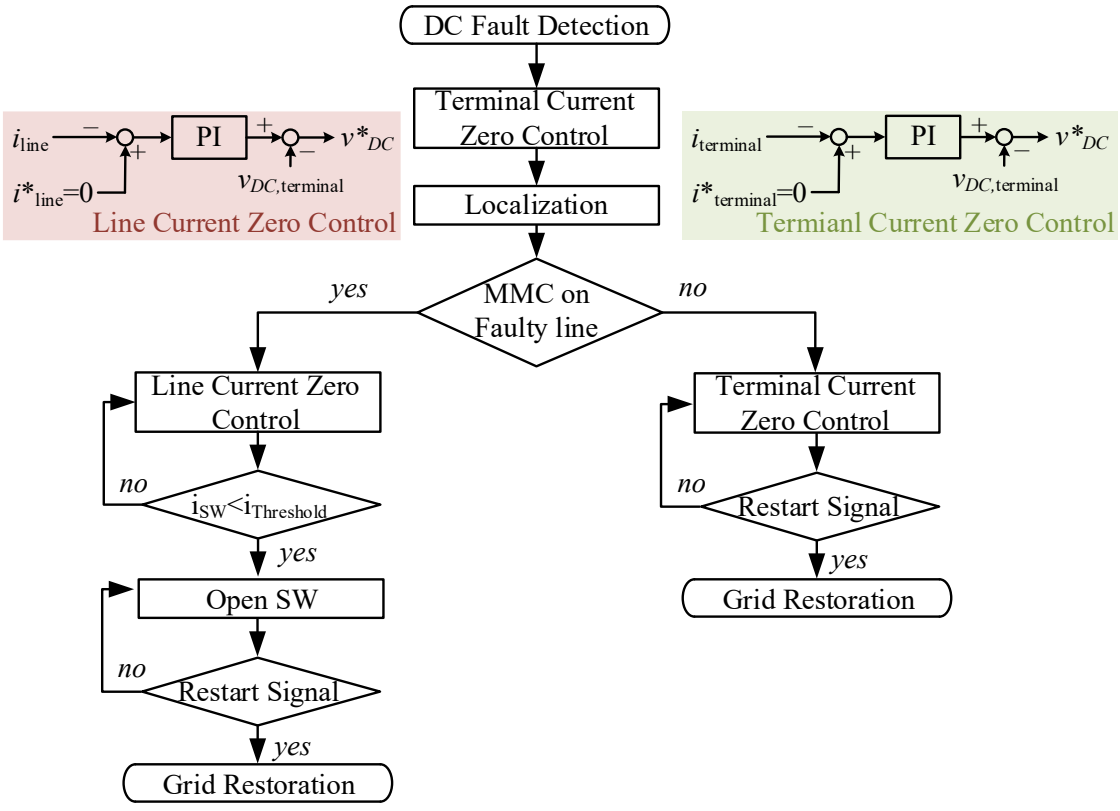


Fig. 2. 15 General protection strategy proposed in [141].

Chapter 3 Modelling of MMC and AC System

As one of the most important feature of power system operation and stability, system frequency is always required to maintain in an acceptable safety range. Sudden change of demand or generation may cause system frequency fluctuation and potentially make the system unstable. Furthermore, facing the global energy crisis, the reduced system inertia increases the risk of system frequency problems. Besides the frequency regulating capacity of the grid itself, MMC-HVDC system can be controlled to provide frequency support. In this chapter, a three-terminal power grid interconnected by HB-MMC system is simulated using MATLAB/SIMULINK. A power grid frequency support control is proposed and discussed.

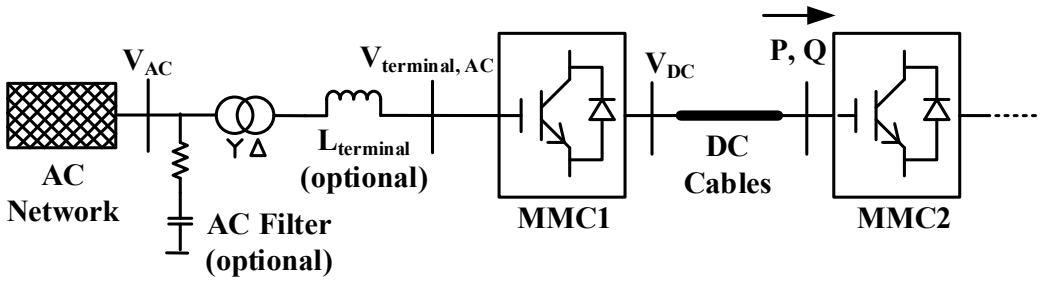


Fig. 3. 1 Typical single line MMC-HVDC system.

3.1 Control and Operation of MMC-HVDC System

Fig. 3.1 shows the single line diagram of a typical MMC-HVDC system with detailed illustration of one converter terminal. Each side comprises a converter, a converter transformer, one optional converter terminal reactor and an optional AC filter.

The converter transformer is used to provide voltage matching and galvanic isolation, and to block zero-sequence components. It also provides certain inductance between the converter terminal and connected AC network for power flow control, fault

current limiting etc. Depending on specific applications, an optional terminal reactor ($L_{terminal}$) may be added to further increase the inductance between the converter terminal and AC grid.

As MMC with large numbers of submodules nearest level modulation (NLM) [146] technique generates very low harmonics in the output voltage and current, there potentially requires no AC filtering. Nevertheless, depending on system design and operation requirement, small AC filter could be added if necessary, to provide additional harmonic filtering and reactive power compensation.

Typical operation for the system shown in Fig. 3.1 requires one MMC to control the DC voltage whereas the other MMC can control the active power transmission across the DC network.

3.1.1 Synchronous dq Reference Frame

The basic concept used for modelling and control of MMC is implemented in the synchronous rotating dq frame, which transfers a 3-phase AC system to a DC system to decouple the control of active power and reactive power. So, a brief description on the dq reference farm and transformations among the different frames is provided here. For a balanced three-phase system without zero sequence component, there is:

$$X_a + X_b + X_c = 0 \tag{3.1}$$

where X_{abc} can be either the phase abc voltage or current.

Fig. 3.2 shows the spatial relationships among the stationary abc and αβ frames, and the rotating synchronous dq frame, where X represents the voltage/current vector.

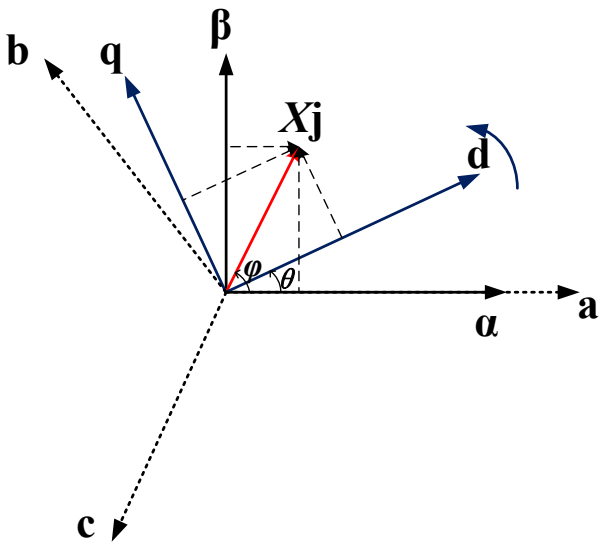


Fig. 3. 2 Stationary αβ reference frame to rotating dq reference frame.

The transformation from stationary abc to αβ frames is given by Clark Transformation as:

$$X_{\alpha\beta} = X_\alpha + jX_\beta = k[X_a + X_b e^{j\frac{2\pi}{3}} + X_c e^{j\frac{4\pi}{3}}] \tag{3.2}$$

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = k \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.3}$$

where k is a constant number and its value is set as $\sqrt{\frac{2}{3}}$ for power invariant transformation and $\frac{2}{3}$ for voltage invariant transformation.

Park Transformation transforms from αβ to dq reference frame as

$$X_{dq} = X_{\alpha\beta} e^{-j\theta} \tag{3.4}$$

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = k \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.5}$$

where θ is the angle shift between the α and d axis.

Thereby, the direct transformation from abc frame to dq frame is given as

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = k \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.6}$$

The inverse transformation from dq frame to abc frame is given as

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = k \begin{bmatrix} \cos\theta & -\sin\theta \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_d \\ X_q \end{bmatrix} \tag{3.7}$$

3.1.2 Modelling of MMC

The circuit configuration of an MMC is shown in Fig 3.3, and its equivalent circuit is shown in Fig. 3.4 in which each arm is represented by an equivalent voltage source. In Fig. 3.3 and 3.4, I_{dc} and U_{dc} are the respective nominal DC current and voltage. i_{pj} and i_{nj} (j=a,b,c) are the respective upper and lower arm current. u_{pj} and u_{nj} are the equivalent voltage generated by the upper and lower arms respectively. R_0 and L_0 are the respective arm resistance and inductance. u_{cj} and i_{cj} are the respective converter terminal AC phase voltage and current. $L_{terminal}$ is the overall equivalent converter terminal inductance and transformer leakage inductance. U_{sj} represents the AC source voltage.

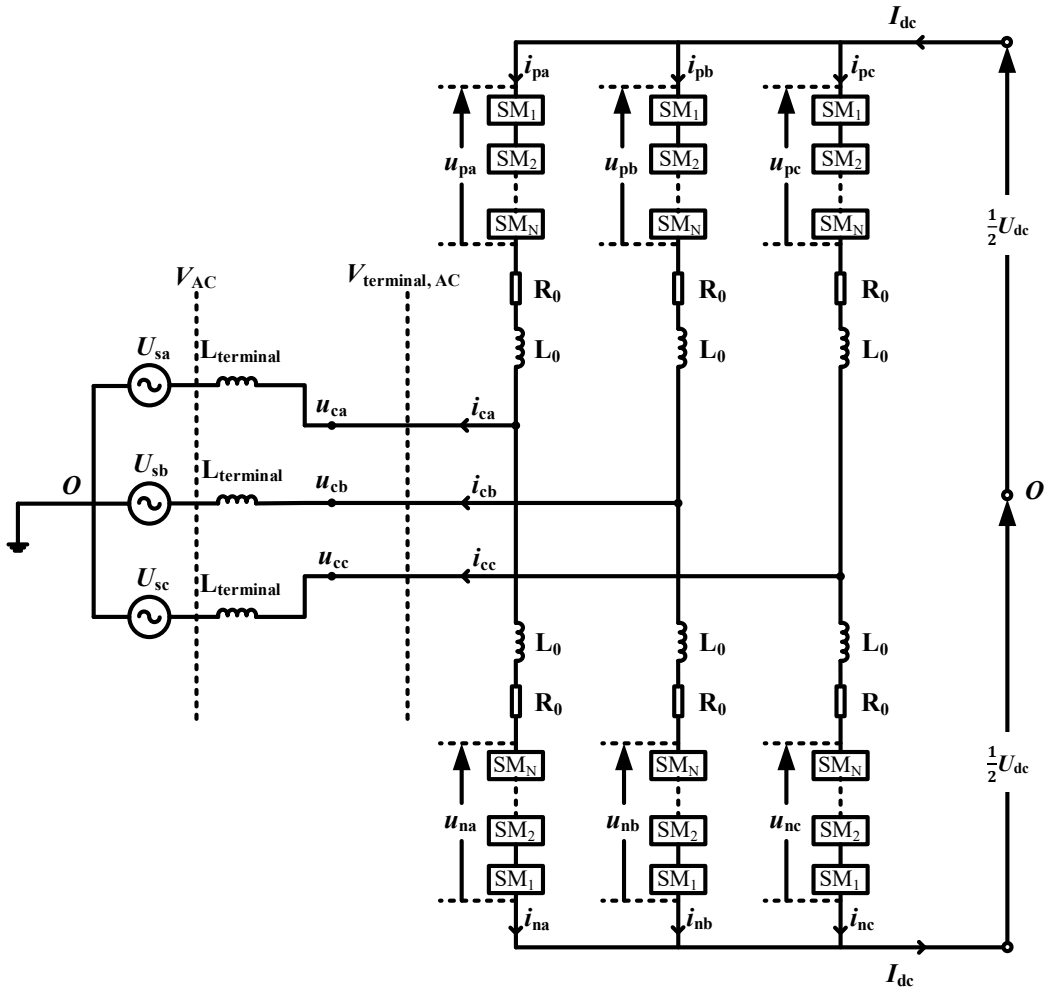


Fig. 3. 3 Topology of MMC.

Taking phase a as an example and according to the KVL principle, the MMC system can be expressed as:

$$U_{sa} + L_{terminal}\frac{di_{ca}}{dt} + u_{pa} + R_0 i_{pa} + L_0\frac{di_{pa}}{dt} = \frac{1}{2}U_{dc} \tag{3.8}$$

$$U_{sa} + L_{terminal}\frac{di_{ca}}{dt} - u_{na} - R_0 i_{na} - L_0\frac{di_{pa}}{dt} = -\frac{1}{2}U_{dc} \tag{3.9}$$

The common mode voltage u_{comma}, difference model voltage u_{diffa} of the upper and lower arms, common mode current i_{coma} and AC phase current i_{ca} are defined as:

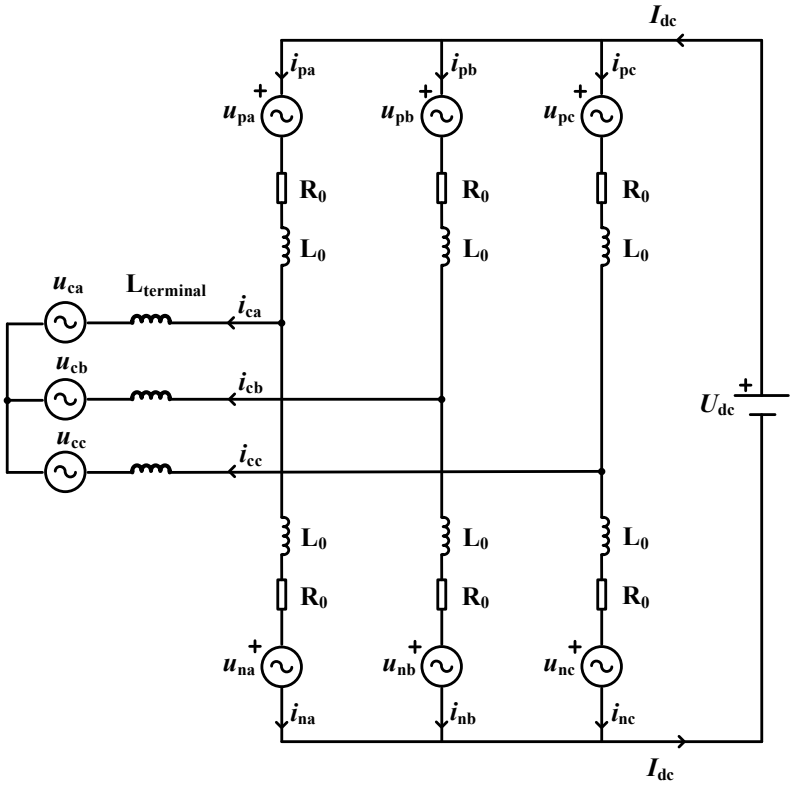


Fig. 3. 4 Equivalent circuit of an MMC.

$$u_{comma} = \frac{1}{2}(u_{na} + u_{pa}) \tag{3.10}$$

$$u_{diffa} = \frac{1}{2}(u_{na} - u_{pa}) \tag{3.11}$$

$$i_{coma} = \frac{1}{2}(i_{na} + i_{pa}) \tag{3.12}$$

$$i_{ca} = \frac{1}{2}(i_{pa} - i_{na}) \tag{3.13}$$

Substituting (3.10), (3.11) and (3.12) into (3.8) and (3.9), there are:

$$-U_{sa} + u_{diffa} = \left(L_{terminal} + \frac{1}{2}L_0\right)\frac{di_{ca}}{dt} + \frac{1}{2}R_0 i_{ca} \tag{3.14}$$

$$\frac{1}{2}U_{dc} - u_{comma} = L_0\frac{di_{coma}}{dt} + R_0 i_{coma} \tag{3.15}$$

It can be seen from (3.14) and (3.15) that, when AC and DC voltage are stable, the output AC phase current and common mode current can be controlled by manipulating the difference voltage and common voltage of the upper and lower arm respectively.

Equation (3.14) can be derived in 3-phase form in time domain as:

$$\begin{cases} L\dfrac{di_{ca}(t)}{dt} + Ri_{ca}(t) = -U_{sa}(t) + u_{diffa}(t) \\ L\dfrac{di_{cb}(t)}{dt} + Ri_{cb}(t) = -U_{sb}(t) + u_{diffb}(t) \\ L\dfrac{di_{cc}(t)}{dt} + Ri_{cc}(t) = -U_{sc}(t) + u_{diffc}(t) \end{cases} \tag{3.16}$$

where $L = L_{terminal} + \frac{1}{2}L_0$ and $R = \frac{1}{2}R_0$.

Applying the constant voltage Park Transformation shown in (3.6) with k=2/3 yields:

$$\begin{cases} L\dfrac{di_{cd}(t)}{dt} + Ri_{cd}(t) = -U_{sd}(t) + u_{diffd}(t) + \omega Li_{cq}(t) \\ L\dfrac{di_{cq}(t)}{dt} + Ri_{cq}(t) = -U_{sq}(t) + u_{diffq}(t) - \omega Li_{cd}(t) \end{cases} \tag{3.17}$$

Equation (3.17) can be expressed in frequency domain using Laplace transform as:

$$\begin{cases} (R + sL)i_{cd}(s) = -U_{sd}(s) + u_{diffd}(s) + \omega Li_{cq}(s) \\ (R + sL)i_{cq}(s) = -U_{sq}(t) + u_{diffq}(t) - \omega Li_{cd}(t) \end{cases} \tag{3.18}$$

Therefore, the MMC AC side mathematical frequency domain model in dq-frame is obtained, and can be illustrated as diagram shown in Fig. 3.5.

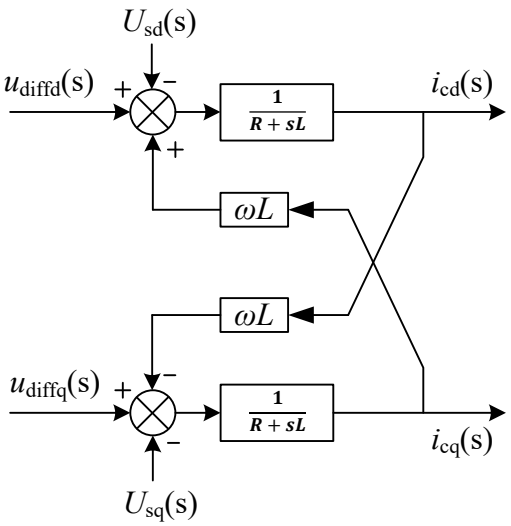


Fig. 3. 5 MMC mathematical frequency domain model in dq-frame.

From Fig. 3.5 and (3.18), it can be known that the output AC current can be controlled by controlling the difference mode voltage.

If the d-axis is aligned to the AC network voltage U_s, the active and reactive power injected into the AC system by the MMC can be expressed as

$$\begin{cases} p_s = \frac{3}{2} U_s i_{cd} \\ p_s = -\frac{3}{2} U_s i_{cq} \end{cases} \tag{3.19}$$

Therefore, the real and reactive power injected into the AC system can be regulated by controlling the current in the dq frame, respectively.

3.1.3 Circulating Current Control

The main cause for the circulating current between arms is the output arm voltage variation due to the voltage ripples from the submodules. Due to the periodic charge and discharge of the submodules' capacitors, their voltage contains significant fundamental and second order harmonic variation. Such submodule capacitor voltage variation leads

to harmonic voltages (mainly 2nd harmonics) being generated by the arms and consequently circulating current among the three-phase arms. The circulating current appears as common mode component shown in (3.12) as it flows through both upper and lower arms in each phase. Considering the common mode current also contains a DC component which defines the AC and DC power transfer, the circulating current i_{cira}, taking phase A as example, and can be expressed as (where harmonic components of 3rd order and above are neglected):

$$i_{coma} = \frac{1}{3} I_{dc} + i_{cira}, \qquad i_{cira} = I_{r2m} \cos(2\omega t - \theta) \tag{3.20}$$

where I_{r2m} is the 2nd order harmonic component.

The circulating currents for phase b and c are:

$$\begin{aligned} i_{comb} &= \frac{1}{3} I_{dc} + i_{cirb}, \qquad i_{cirb} = I_{r2m} \cos\left(2\omega t - \theta + \frac{2}{3}\pi\right) \\ i_{comc} &= \frac{1}{3} I_{dc} + i_{circ}, \qquad i_{circ} = I_{r2m} \cos\left(2\omega t - \theta - \frac{2}{3}\pi\right) \end{aligned} \tag{3.21}$$

It can be seen that the 2nd order harmonic component is negative sequence component. The abc-dq transformation can also be applied based on the negative sequence 2nd order harmonic component as:

$$\boldsymbol{T}(\theta) = \frac{2}{3} \begin{bmatrix} \cos 2\theta & \cos(2\theta + \frac{2\pi}{3}) & \cos(2\theta - \frac{2\pi}{3}) \\ \sin 2\theta & \sin(2\theta + \frac{2\pi}{3}) & \sin(2\theta - \frac{2\pi}{3}) \end{bmatrix} \tag{3.22}$$

The MMC differential equation (3.15) can be written in three phases as

$$-\begin{bmatrix} \tilde{u}_{comma}(t) \\ \tilde{u}_{commb}(t) \\ \tilde{u}_{commc}(t) \end{bmatrix} = L \frac{d}{dt} \begin{bmatrix} i_{cira}(t) \\ i_{cirb}(t) \\ i_{circ}(t) \end{bmatrix} + R \begin{bmatrix} i_{cira}(t) \\ i_{cirb}(t) \\ i_{circ}(t) \end{bmatrix} \tag{3.23}$$

where $\tilde{u}_{commj}$ is the AC component (2nd harmonic) of the common mode voltage u_{commj}.

Combine equations (3.22) and (3.23) getting

$$\begin{bmatrix} 0 & -2\omega L \\ 2\omega L & 0 \end{bmatrix} \begin{bmatrix} i_{cird}(t) \\ i_{cirq}(t) \end{bmatrix} - \begin{bmatrix} \tilde{u}_{commd}(t) \\ \tilde{u}_{commq}(t) \end{bmatrix} = L\frac{d}{d_t}\begin{bmatrix} i_{cird}(t) \\ i_{cirq}(t) \end{bmatrix} + R\begin{bmatrix} i_{cird}(t) \\ i_{cirq}(t) \end{bmatrix} \quad (3.24)$$

Then the frequency domain model can be obtained through Laplace transform and expressed as

$$\begin{cases} (R + sL)i_{cird}(s) = -\tilde{u}_{commd}(s) - 2\omega L i_{cirq}(s) \\ (R + sL)i_{cirq}(s) = -\tilde{u}_{commq}(t) + 2\omega L i_{cird}(t) \end{cases} \quad (3.25)$$

It can be seen that the circulating current can be regulated by controlling the AC component (2nd harmonic) of the common mode voltage, as shown in Fig. 3.6.

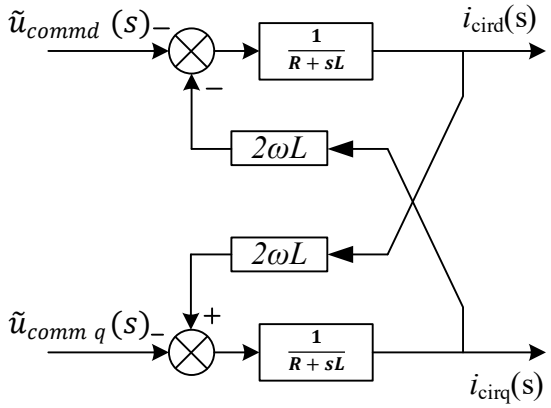


Fig. 3. 6 MMC mathematical model of circulating current in dq-frame.

As the system is transferred to DC using dq-frame synchronized to the 2nd harmonics. It can be controlled using traditional feedback control.

3.1.4 Capacitor Voltage balancing and NLM

The MMC arms are composed by large number of SMs, and they are subject to periodic charging and discharging leading to voltage variations of the SM capacitors during normal operation. The voltage balancing of all SM capacitors is one of the requirements for the MMC to output good quality waveforms and to ensure the SMs are within their safe voltage range. The most widely used capacitor voltage balancing method is the capacitor voltage sorting algorithm with nearest level modulation (NLM) technique [147]. The voltage of all capacitors is measured and sorted from high to low. The capacitors with the highest voltage are switched in during the discharging cycle whilst capacitors with the lowest voltage are switched in during the charging cycle according to the sorted sequence.

The sorting algorithm of capacitor voltage advise the preferential sequence for the SMs to be switched in, when, which and how many SMs should be switched in is determined by the modulator. The modulation method adopted is NLM which is suitable for applications with large number of SMs [146, 148]. NLM aims to control the voltage difference between modulated wave (reference voltage) and MMC stair wave within $\pm 0.5U_c$, where U_c is the voltage of one SM capacitor. Therefore, with more voltage levels, the output waveform is formed more precise to a sin wave. Combining NLM with the SM capacitor voltage sorting algorithm, the fire signals are generated for the IGBTs in the SMs.

3.1.5 Control Design of MMC

The basic control system of MMC-HVDC consists of inner current control layer, outer power control layer, circulating current control, coordinate transformation, phase locked loop (PLL) and submodule capacitor voltage balancing and switching pulse generation (NLM) as shown in Fig 3.7.

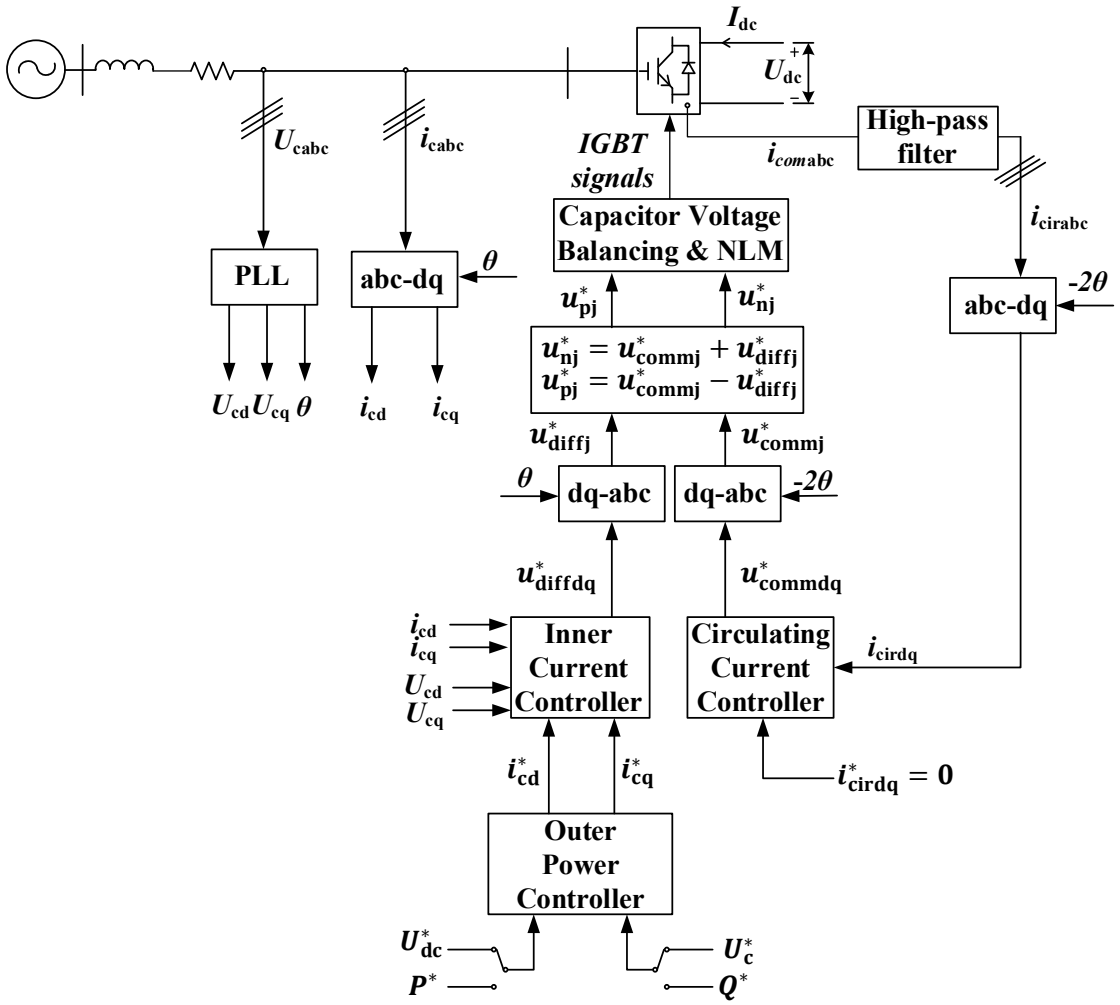


Fig. 3. 7 Diagram of control system of MMC converter.

As shown in Fig. 3.7, the θ for the coordinate transmission between abc and dq frames is generated by the PLL. For a point-to-point HVDC system, normally DC voltage control is implemented at one end and active power control at the other end, and they will generate the active current d-axis current reference i^*_{cd} for each of the terminals. Reactive power and AC voltage can be independently controlled at each terminal which generates the q-axis current reference i^*_{cq}. The differential mode voltage reference is generated by the inner current controller based on the i^*_{cd} and i^*_{cq}. The circulating current i_{cirabc} (2nd order AC component) is measured through a high-pass filter from the common mode

current i_{comabc}, and is then controlled at zero by the circulating current controller through the common mode voltage.

3.2 AC System Modelling and Frequency Dynamics

The AC system used for the Chapter 4 and 5 is modelled to ensure the feature of system frequency response, and detailed synchronous generator model is thus used.

3.2.1 AC system frequency dynamics

Stability of frequency is generally defined as the ability of a power system to maintain or regain a steady frequency after a system disturbance, which depends on the ability of restoring the balance between system demand and generation [149]. Severe system disturbances such as large generation loss and transmission line faults, will lead to significant excursions of system frequency whereas frequency excursion always causes large deviations of voltage, rotor angle and other system variables. Therefore, as one of the most important variable of power system operation and stability, system frequency is always required to maintain at a certain safety range.

The rotor speeds of conventional synchronous generators with rotating mass determine system frequency and they are strictly coupled with the dynamic equilibrium of active power demand and generation. Events of unbalance between load and generation such as unexpected load change and system structure change due to the isolation of faulted elements, will cause frequency excursions. Due to the mechanical nature of system inertia provided by generator rotating mass, frequency excursion dynamic performances are relatively slow which is in the order of hundreds of milliseconds to seconds, compared to other power system transients. The relationship between active power balance and system frequency excursion is given as

$$\frac{1}{2}J_{sys}\frac{d\omega^2}{dt} = P_g - P_d \tag{3.26}$$

where J_{sys} is the system inertia, ω is the electrical angular frequency, P_g and P_d are system power generated and consumed respectively.

For a single generator, the inertia is preferred to be expressed in per unit term as inertia time constant H_{gen} as

$$H_{gen} = \frac{\frac{1}{2}J_{gen}{\omega_0}^2}{S_{gen}} \tag{3.27}$$

where S_{gen} is the nominal power rating of the generator, ω_0 is the nominal angular frequency, J_{gen} is the generator inertia.

Since system inertia can be simply expressed by the sum of inertias of all generators within the system, therefore the inertia time constant of system can be determined as

$$H_{sys} = \frac{\sum H_{gen} \cdot S_{gen}}{S_{sys}} \tag{3.28}$$

where S_{sys} is the nominal power rating of the whole system.

Since H_{sys} represents the inertia time constant of the whole system, (3.26) can be rewritten as

$$2H_{sys} \cdot \frac{d\omega^*}{dt} = {P_g}^* - {P_d}^* \tag{3.29}$$

where superscript * represents per unit values.

It can be seen from (3.29) that the frequency deviation is determined by system inertia and active power imbalance. The system total inertia is determined by all the generators contained in the system. Thus, for a given system, the inertia is defined, and the system frequency is influenced by the system dynamic power balance.

3.2.2 Modelling and Control of Synchronous Generators

The Synchronous Generator (SG) now is still the most widely used power generation worldwide, and the inertia feature of SG determines power system dynamics. Therefore, proper SG models are required for simulation studies and the lower order SG models may not provide accurate performance of the generators. Thus, the conventional seventh order model, of SG is modelled and used for simulation in this study, as shown in Fig. 3.8.

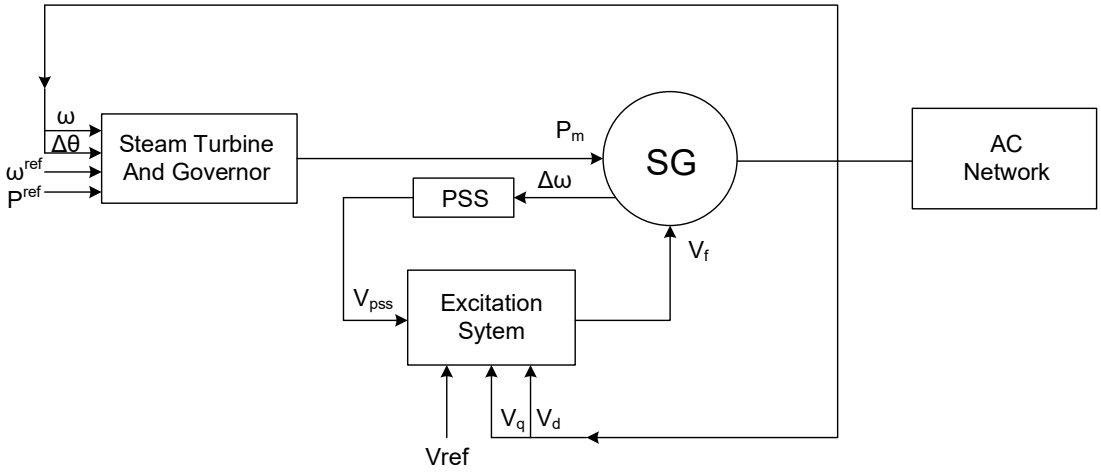


Fig. 3. 8 The SG model and control system.

It is shown in Fig. 3.8 that the excitation system controls the generator terminal voltage by controlling the filed current. As seen, the real-time terminal voltage is compared with the reference value to achieve the dynamic output voltage control. The problem of rotor oscillations in case of disturbances is restricted by the power system stabilizer (PSS) which generates a voltage stabilizing signal to the input voltage reference. The input of the PSS is the torque balance related signals such as rotor speed and frequency.

The mechanical feature of the generator is modelled and provided by the steam turbine and governor, which produce the prime mechanical power to the generator. Since one of the most important objectives of Chapter 4 and 5 is to investigate system frequency related problems, the prime turbine is necessary to be modelled in the generator model to provide the mechanical features. On the other hand, if the time period of the investigated objective is relatively short, e.g. in a few seconds or less, the generator prime turbine may not have time to change the mechanical input because of slow response of the turbine governor. Therefore, the mechanical input power can be modelled as a constant to simplify the modelling. However, if system frequency related events are studied which requires longer simulation period of the tens of seconds, the turbine governor is necessary to be included in the generator model.

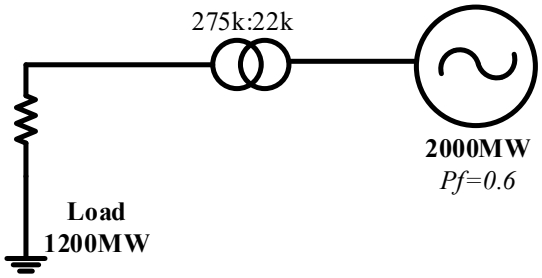
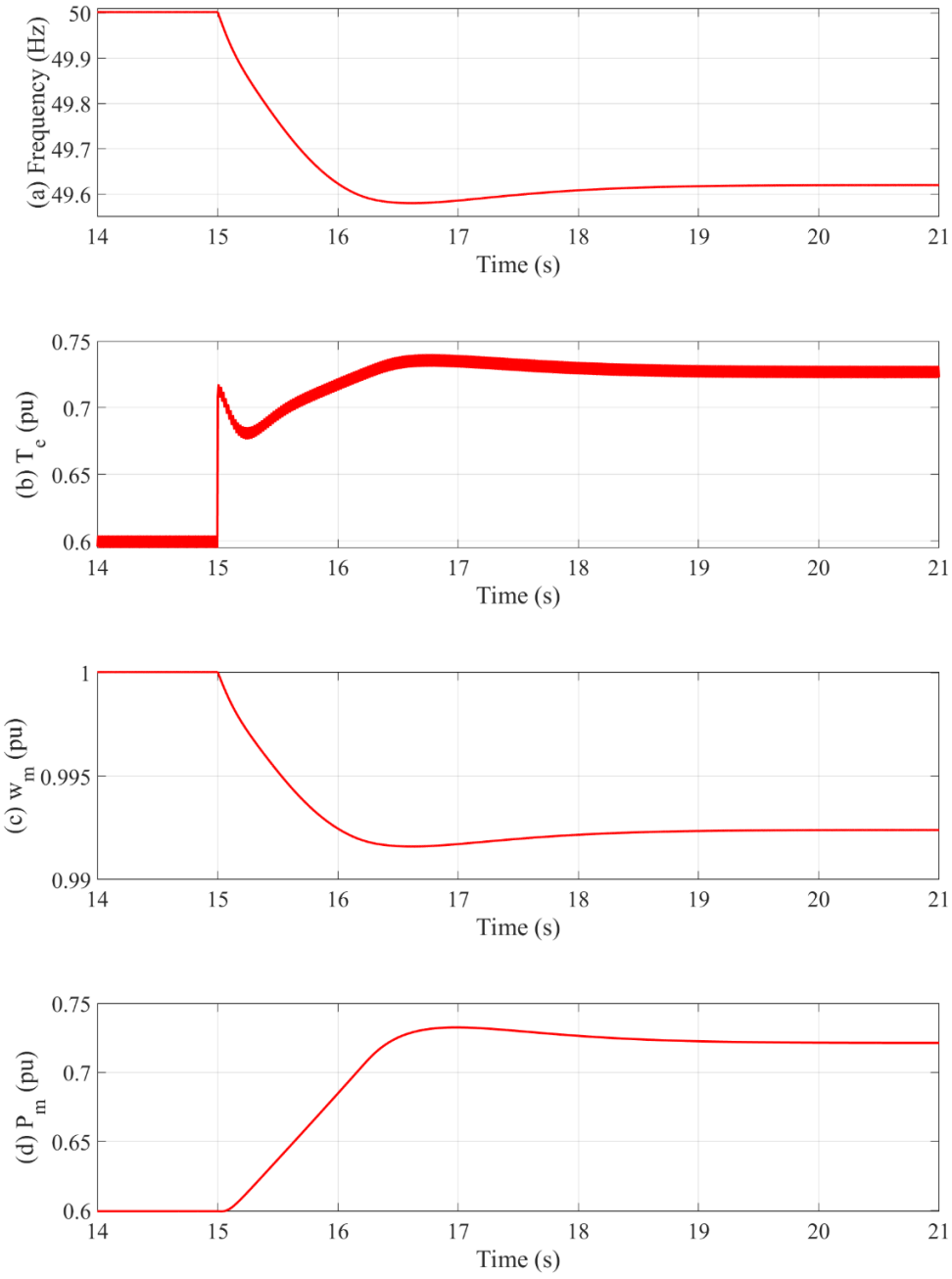


Fig. 3. 9 A simple system used to show SG response under load increase.

For a simple system which contains a SG, a transformer and a pure resistive load shown in Fig. 3.9, Fig. 3.10 shows the frequency response of the system in case of 10% load increase at the time of 15s. It can be seen from Fig. 3.10 (a) that the system frequency drops from 50 Hz rapidly and stabilises at a new stable value around 49.6 Hz at the time of 20s. The rapid decrease of frequency is because when the load suddenly increased, the increased electromagnetic torque T_e (shown in Fig. 3.10 (b)) of the generator on the stator exceeds the mechanical torque of the prime turbine and consequently, the rotor speed ω_m of the generator slows down shown in Fig. 3.10 (c). The turbine governor then increases the mechanical power input P_m (shown in Fig. 3.10 (d)) to the generator to increase the

output electrical power P_{eo} (shown in Fig. 3.10 (e)) to fulfil the power shortage and the difference between the mechanical torque and electromagnetic torque decreases and the rotor speed and system frequency gradually recover to a new stable point. The simulation results show that the model provide enough mechanical features for the studies in the following chapters. Due to the use of frequency-active power droop in the turbine governor, the frequency does not recover to the rated value of 50Hz in the simulation.



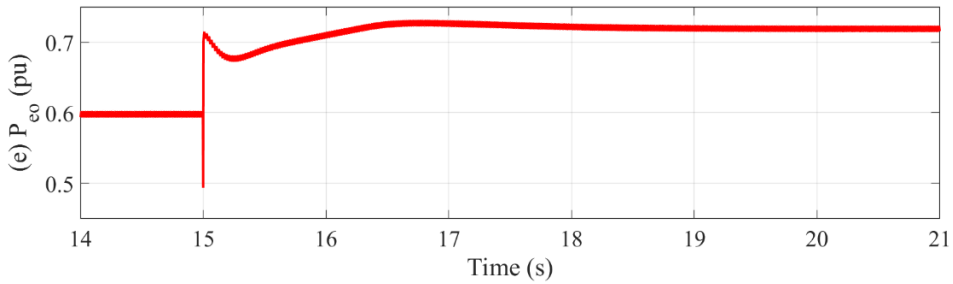


Fig. 3. 10 Waveforms of SG during the 10% load increase: (a) frequency, (b) electromagnetic torque, (c) rotor speed, (d) mechanical power input and (e) output electrical power.

Chapter 4 Dynamic Power Sharing and Frequency Support in HVDC system

This chapter investigates the use of HVDC connections to provide frequency support to the connected AC networks. The focus is on the design of the outer control layers for the HVDC systems. In this chapter, both point-to-point HVDC connection and three-terminal HVDC system are studied to investigate different frequency support strategies.

4.1 Network Configuration

The power system is modelled in MATLAB/Simulink as a two-terminal VSC-HVDC system shown in Fig. 4.1. Both converters (MMC1 and MMC2) are rated at 2500 MW. As shown, AC terminal 1 contains a synchronous generator rated at 2.7 GW and 3.2 GW load while, AC terminal 2 contains a synchronous generator rated at 5.5 GW and 1.7 GW load. MMC2 controls the DC voltage and MMC1 controls active power. In the study below, MMC1 transfers 1600 MW from DC to AC Terminal 1.

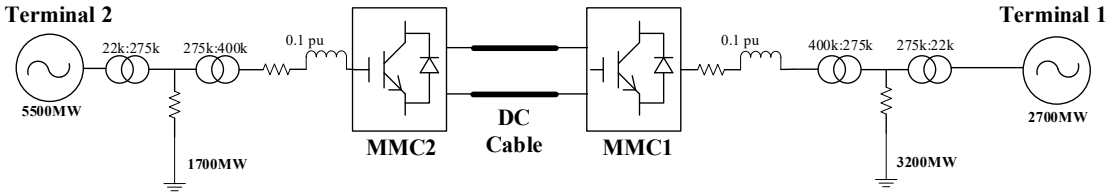


Fig. 4. 1 The diagram of the 2-terminal HVDC simulation network.

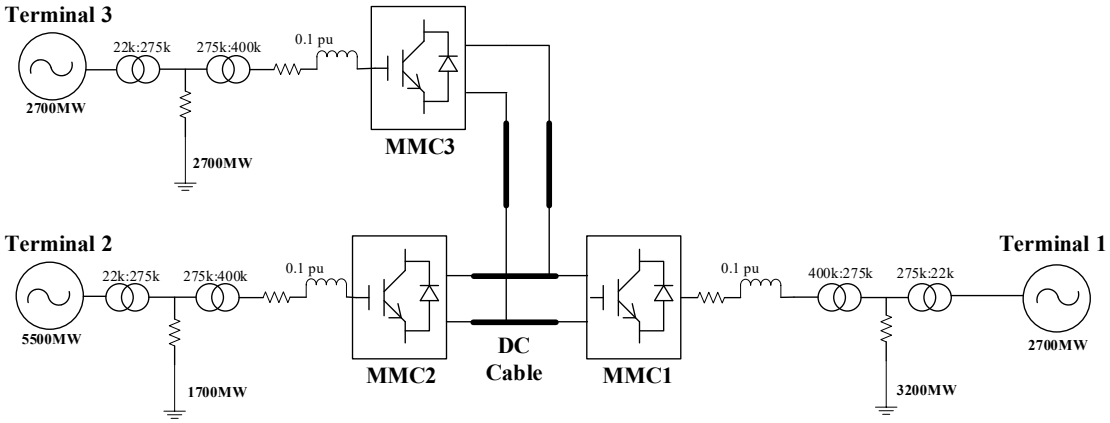


Fig. 4. 2 The diagram of three-terminal simulation network.

For the second stage study, simulation model of a radial three-terminal MMC-HVDC system shown in the figure 4.2 is developed, with rated power of 3500 MW for MMC2 and 2500MW for MMC1 and MMC3. Under nominal operation, Terminal 2 delivers 1600 MW and 1100 MW to Terminal 1 and 3, respectively. As the same with two-terminal system simulation, MMC2 controls the DC voltage, whilst MMC1 and MMC3 control active power.

4.2 Frequency Support Strategies

The key content of the frequency support strategy is to dispatch real power from other terminals to fill the power shortage when load increases suddenly at one terminal, in order to reduce the frequency drop while the local generators adjusting their output to balance the power change. Although this re-dispatch of real power can influence the system frequency at other terminals, it can improve the overall system frequency performance in case of disturbances. Moreover, when the power unbalance happens at a terminal with relatively low capacity, the other terminals with higher capacity can provide significant support with much less influence on their own frequencies. In another word, power shortage happens at one terminal is shared by all the terminals connected by the HVDC network. However, it is important to consider the different capacities of AC

networks at different terminals to ensure reasonable power sharing proportion so as to improve the overall system frequency performance.

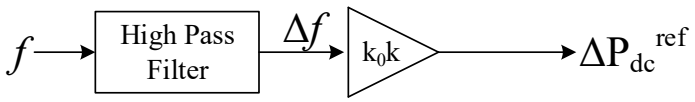


Fig. 4. 3 frequency support control diagram implemented at Terminal 1.

Fig. 4.3 shows the basic control diagram of the outer control layer for the frequency support control loop at power controlling terminal MMC1. When the frequency varies as the result of sudden active power imbalance in AC terminal 1, a frequency deviation Δf (in Hz) is generated by the high-pass filter output (in pu). The controller is switched in when Δf exceeds the threshold of 2% (0.1 Hz), and then it passes to a gain of k_0k to generate the active DC power deviation of $\Delta P_{dc}{}^{ref}$ (in pu), which is added to the initial active power reference to modulated the converter's active power exchange between the DC and AC terminal 1. Value of k_0 is set as 50 in all cases in this chapter. In this study, the converter only provides transient frequency support and all the steady-state power shortage is supplied by the local generator itself with secondary frequency modulation. Thus, when the output of local generator has fulfilled the power shortage, the additional active power dispatched from other terminals drops back to zero.

An event of 20% load increase at Terminal 1 is simulated and selected waveforms are shown in Fig. 4.4 to give a general overview of the frequency support control. As described, MMC2 at Terminal 2 controls the DC voltage while MMC1 at Terminal 1 controls the active power flow. Under the normal operation, 1.6 GW active power is transferred from Terminal 2 to 1, and the gain of frequency support unit k is 0.01.

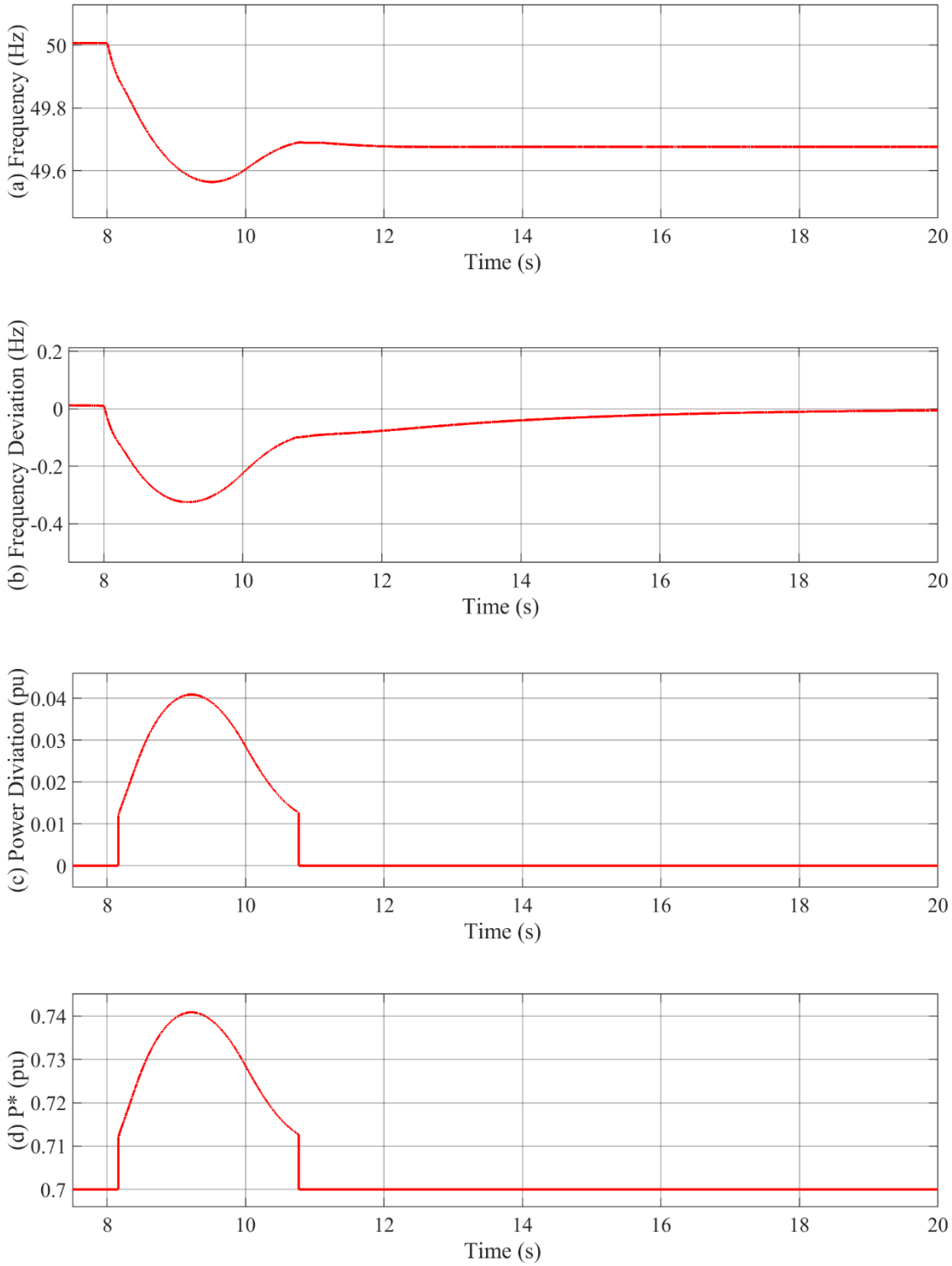


Fig. 4. 4 Waveforms at Station 1 with 20% load increase of (a) frequency, (b) frequency deviation, (c) power deviation, and (d) overall active power reference for the current control loop.

It can be seen from Fig. 4.4 that when a 20% load increase happens at Terminal 1 at time of 8s the system frequency f drops as shown in Fig 4.4 (a). A frequency deviation Δf signal is generated as shown in Fig 4.4 (b). When the frequency deviation exceeds 2% (0.1 Hz) at time of 8.16s, the frequency support unit is switched and as seen in Fig 4.4 (c), a power deviation order is generated accordingly. This additional active power reference is added to the original active power order as shown in Fig 4.4 (d). The increase of power output from the local generator reduces the local power shortage thereby the deviation of frequency drops. When the frequency deviation is lower than 0.1 Hz (at time around 10.77s) the additional active power reference drops to zero.

Fig. 4.5 compares the frequencies at Terminal 1 with and without frequency support. The final stable frequencies are the same as all the power shortage is eventually fulfilled by the local generator (with frequency/active power drop control). The Lowest frequencies are 49.58 Hz and 49.4Hz with and without frequency support, respectively. Therefore, the frequency support can increase the frequency nadir effectively.

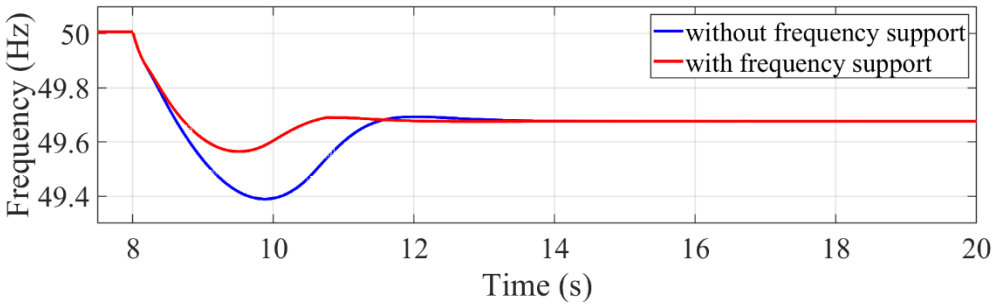


Fig. 4. 5 Frequency at Terminal 1 in case of with and without frequency support.

4.3 Two-terminal network cases studies

4.3.1 Frequency support with different regulation gain (k)

An event of 20% load increase at Terminal 1 is simulated in the same system shown in Fig. 4.6. When the load increase happens at Terminal 1 at time of 8s and the frequency deviation exceeds 0.1 Hz at time of 8.16s, the frequency support unit with different k is switched in to dispatch additional active power from Terminal 2 to 1 in order to support the frequency at Terminal 1. The frequency support is not switched out while frequency deviation is lower than 0.1 Hz in this case (Case 4.3.1).

Fig. 4.6 shows the waveforms at Terminal 1 when different k values are used. With higher value of k, the frequency support provides faster reaction to frequency drop by outputting higher additional active power to AC terminal 1. With k=0 (no additional support), the frequency (blue curve) shown in Fig. 4.6 (a) drops to 49.4 Hz and with frequency support, the frequency nadirs are improved. Meanwhile, it can also be seen that higher value of k makes frequency support controller more sensitive to the frequency drop and slower the drop of the power dispatched from Terminal 2, e.g. k=0.05, 0.5 and 1 shown in Fig. 4.6 (a). In Fig. 4.6 (b), it shows the frequency deviation generated with different value of k and the corresponding additional active power on the frequency deviation is shown in Fig. 4.6 (c). However, with higher value of k, e.g. k=0.5 and 1, the power order is too high for the converter to deliver the corresponding additional power due to the converter's capacity limit. In the study, the active power is limited in the range of -0.95 pu to 0.95 pu, shown in Fig. 4.6 (d). This also indicates the reason why the frequency support performance is not improved when k is increased from 0.5 to 1. However, as mentioned, higher value of k delivers faster frequency support, meanwhile, slower the process of fulfilling the power shortage by local generator, leading to higher amount of power dispatched from Terminal 2 for longer time. Consequently, this could affect the frequency at Terminal 2. Therefore, the design of the value of k should be carefully considered to balance the frequency performance at both terminals in this case.

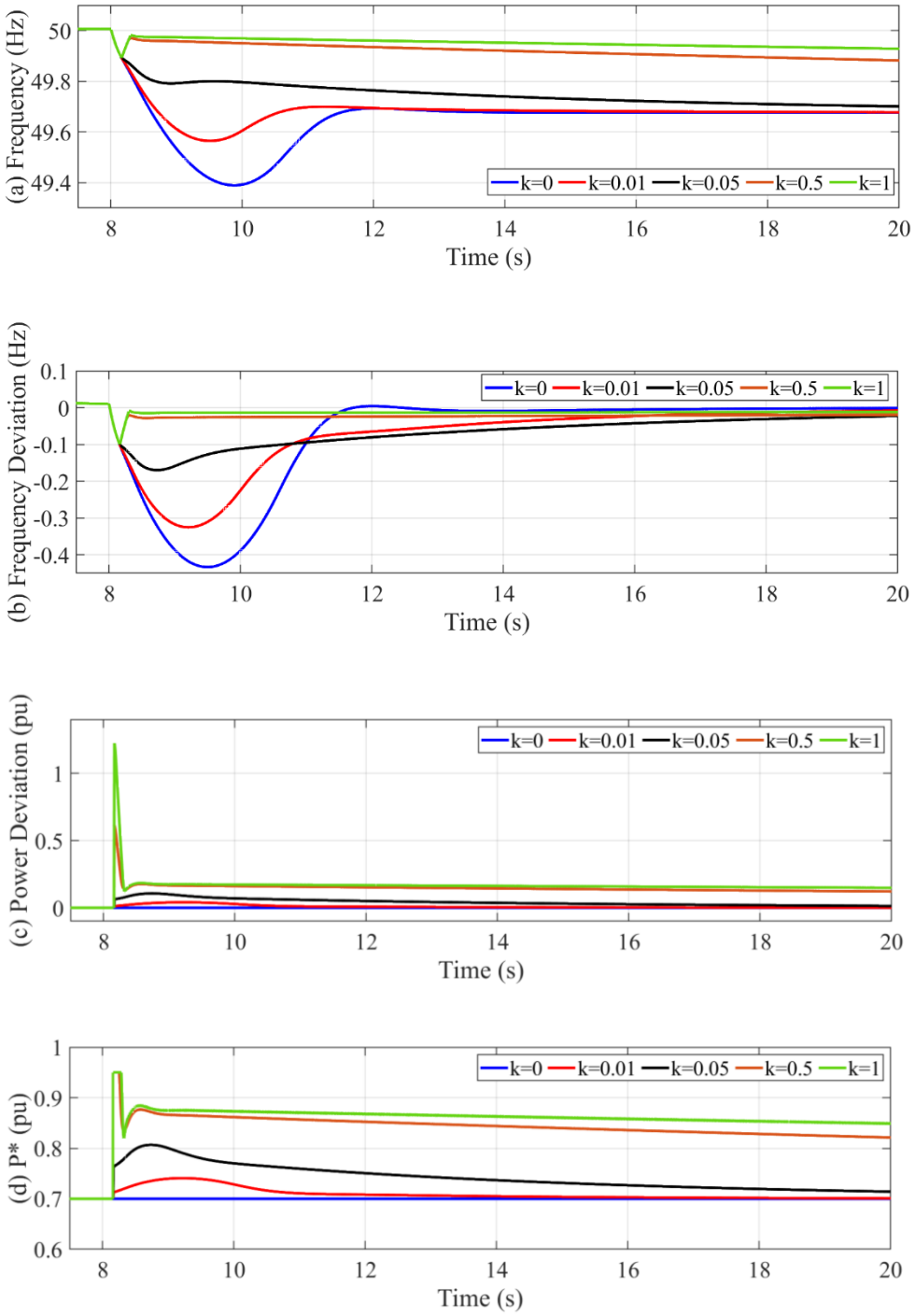


Fig. 4. 6 Waveforms at Station 1 in Case 4.3.1: (a) frequency, (b) frequency deviation, (c) power deviation, and (d) active power reference.

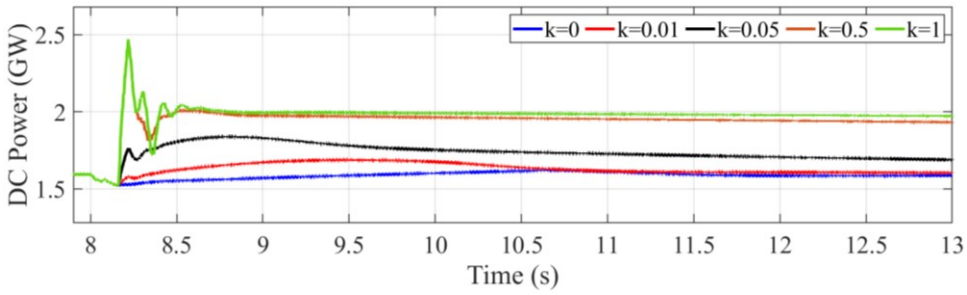


Fig. 4. 7 DC power of Terminal 1.

Fig. 4.7 compares the DC power of Terminal 1 with different k values. Again, with higher value of k, the higher DC power is dispatched from Terminal 2 to 1 leading to faster frequency support response.

Fig. 4.8 shows the DC voltage at Terminal 1 in this case. When the frequency support switched in at time of 8.16s, larger disturbances happens with higher value of k. Therefore, this also indicates that the design of k should be careful to balance the frequency performance on AC side of Terminal 1 and the control and stability of DC voltage.

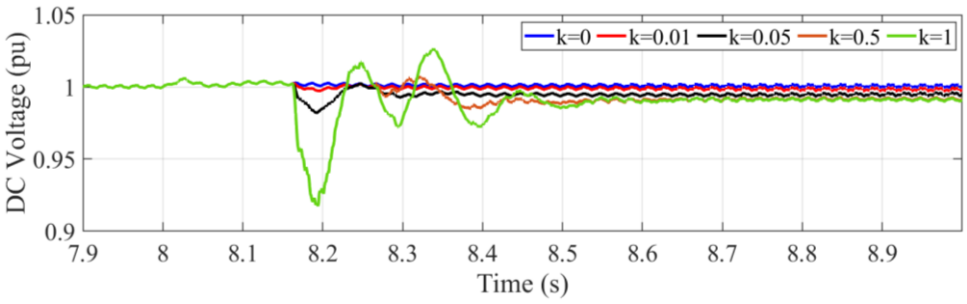
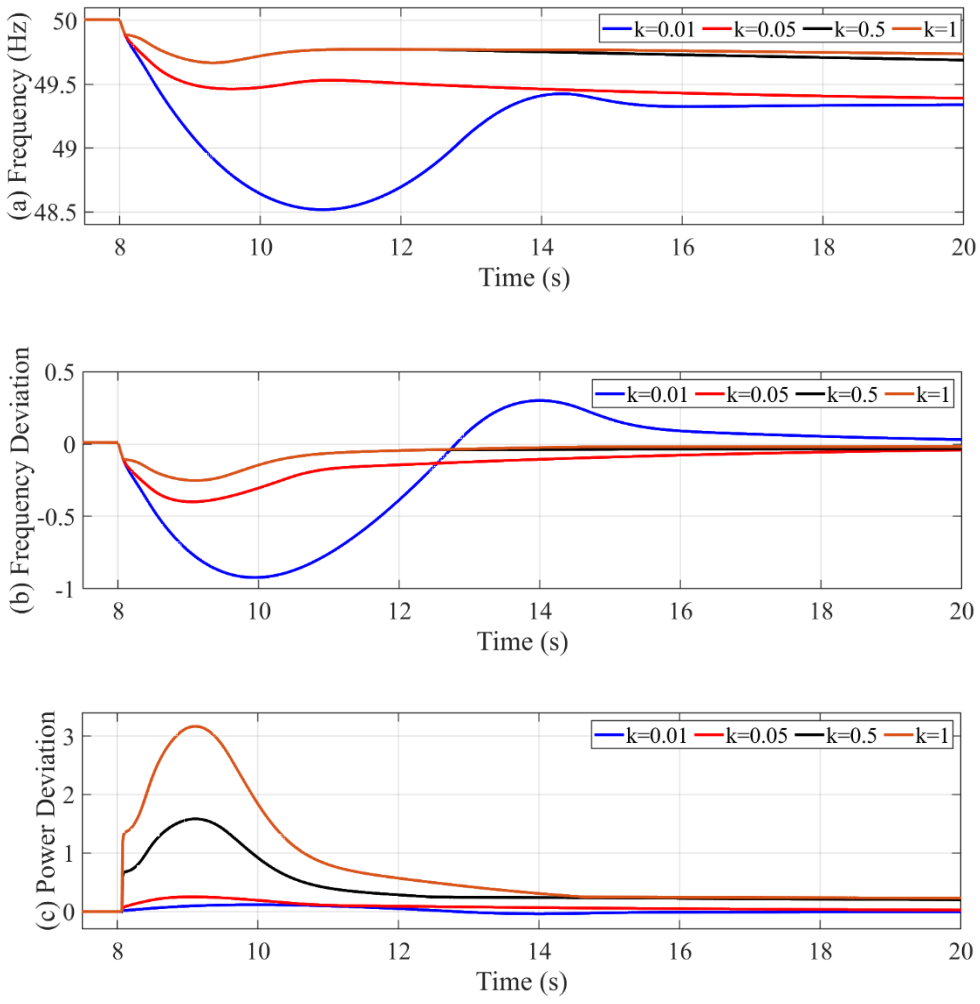


Fig. 4. 8 DC voltage of Terminal 1.

4.3.2 Frequency support with large load increase

A more sever imbalance between load demand and generation caused by 40% load increase is simulated. During nominal operation, the power transmission to Terminal 1 is again 0.7 pu. The load increase happens at time of 8s and with such a larger power shortage, the frequency drops fast and exceeds 0.1 Hz at time of 8.07s, when the frequency support is switched in.

Since the load increase (40%) placed in Case 4.3.2 is too large, the system can only remain stable if sufficient frequency support is used. Therefore, the simulations of k=0 is not considered in this case.



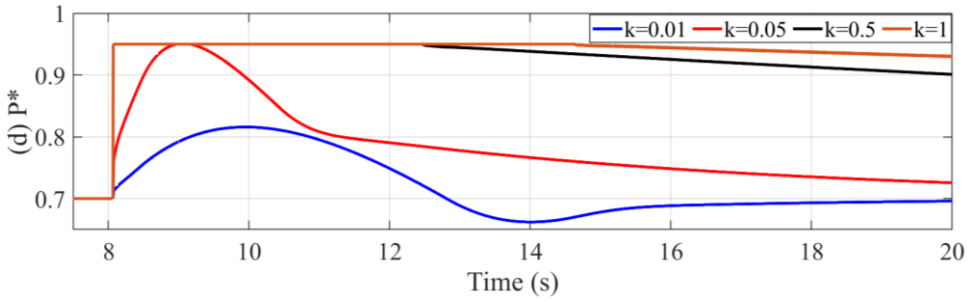


Fig. 4. 9 Waveforms at Station 1: (a) frequency, (b) frequency deviation, (c) power deviation, and (d) active power reference.

Fig. 4.9 shows the system performance at Terminal 1. As can be seen, similar results as with previous case are obtained. However, from Fig. 4.9 (a), it can be seen that the frequencies are almost the same with k=0.5 and 1, due to the limitation of the capacity of MMC1. This can also be observed from Fig. 4.9 (d). With k=0.01, the frequency fluctuation is serious and takes long time to get to a stable state, whereas it is found the system will lose stability if value of k is smaller than 0.01. Therefore, sufficient frequency support is required to maintain system stability in case of sever power imbalance. From the results in this case, k=0.05 can be considered as adequate since k=0.5 and 1 lead to large DC voltage oscillation and sever frequency drop at Terminal 2.

Further simulation with opposition initial power flow direct is simulated, i.e., active power is not being transmitted from Terminal 1 to Terminal 2 (-0.3 pu) prior to the 40% load increases at Terminal 1. As seen from Fig. 4.10 (a), the lowest frequency is now higher than the 49.85 Hz which is improved much compared with previous simulation, which is around 4.97 Hz when k=1 shown in Fig. 4.9 (a). The overall results of this simulation indicate that the negative power transmission at Terminal 1 during nominal operation allows significant additional net active power to be provided to Terminal 1 for frequency support.

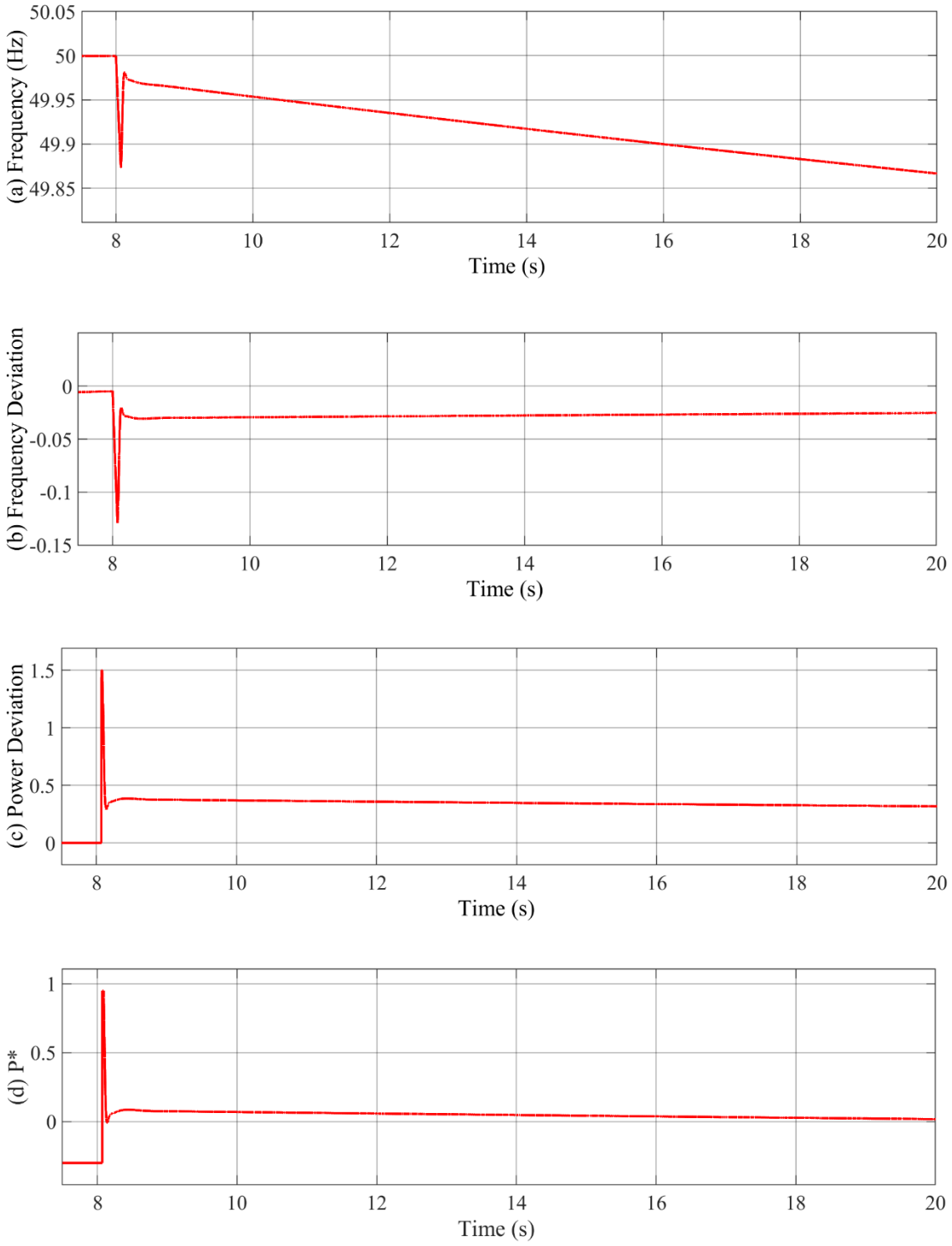


Fig. 4. 10 Waveforms at Station 1 with reversed power transmission: (a) frequency, (b) frequency deviation, (c) power deviation, and (d) active power reference.

4.3.3 Frequency support with load increase at voltage control terminal

With load increase happens at power control terminal (e.g. Terminal 1 in Case 4.3.1), the frequency can be monitored locally, and active power can be dispatched from Terminal 2 without the need for communication. However, when load increase occurs at voltage control terminal, communication with power control terminal may be a problem after local frequency deviation is detected. Therefore, a different frequency support system is studied dealing with load increase at the voltage control terminal.

In Case 4.3.3, the same system shown in Fig. 4.1 is implemented but now Terminal 1 controls the DC voltage and Terminal 2 controls active power. Active power is transferred from Terminal 2 to 1 under nominal operation. A 20% load increase is placed at Terminal 1 at time of 8s. After frequency deviation exceeds 0.1 Hz (at time of 8.16s), the control shown in Fig. 4.11 is switched in to reduce the terminal DC voltage of Terminal 1.

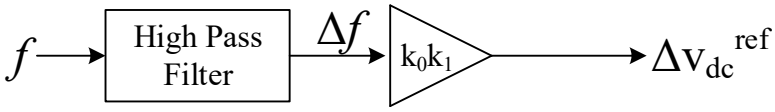


Fig. 4. 11 frequency support control diagram implemented at Terminal 1.

Similar as the control used in previous cases, a DC voltage deviation (in pu) is generated by a gain of k_0k_1 (k_0=50) from the frequency deviation (in pu). Then it is added to the nominal DC voltage to regulate its terminal DC voltage, e.g. a negative frequency deviation (load increase) will generate a negative DC voltage reference to reduce the DC voltage until the power deviation is zero.

At Terminal 2, the control shown in Fig. 4.12 is implemented to dispatch active power depending on the DC voltage, in order to deliver frequency support for Terminal 1.

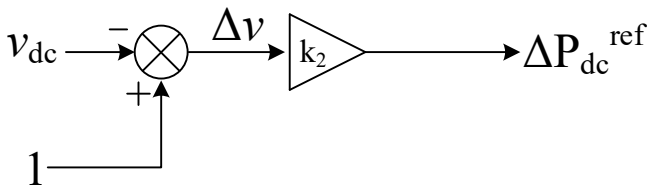


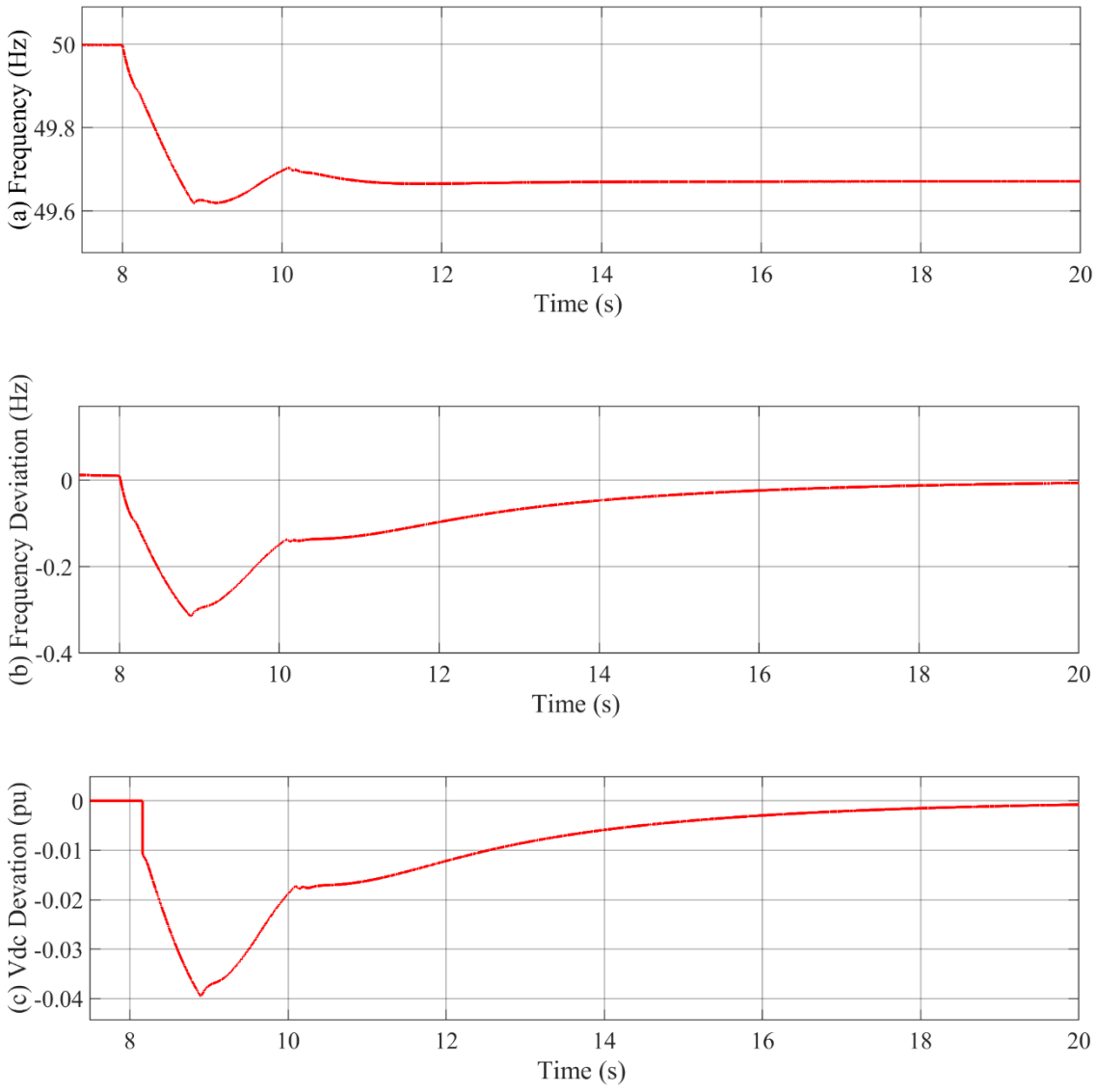
Fig. 4. 12 frequency support control diagram implemented at Terminal 2.

When a DC voltage change Δv beyond 0.02 pu is detected at Terminal 2, the control shown in Fig. 3.23 is switched in to generate a active power deviation (in pu) adding to the original active power reference at Terminal 2, e.g. when a negative voltage deviation is detected, a negative active power reference will be generated to increase power output to Terminal 1 to achieve the frequency support.

Fig. 4.13 shows waveforms at Terminal 1 and 2 to show the general process of the frequency support used in Case 4.3.3 with k_1=0.01 and k_2=2. For the results at Terminal 1, shown in Fig. 4.13 (a), the frequency nadir is higher than 49.6 Hz, which is improved comparing with the same case without frequency support (49.4 Hz) shown in Fig. 4.5. In Fig. 4.13 (a) and (b), when the load increases at time of 8s, the frequency at Terminal 1 starts to drop. When the frequency deviation exceeds 0.1 Hz at time of 8.16s, the controller at Terminal 1 is switched in to reduce the DC voltage reference from 1pu as shown in Fig. 4.13 (d).

At Terminal 2, the DC voltage can be seen from Fig. 4.13 (e) and a low-pass filter is used here to obtain the DC voltage deviation (shown in Fig. 4.13 (f)) in order to prevent the repetitive switching in/out due to the DC voltage transient oscillation. After DC voltage deviation exceeds 0.02pu, the active power reference is increased, shown in Fig. 4.13 (g), to output more power to Terminal 1. While more power is transmitted to Terminal 1, the frequency at Terminal 1 starts to recover, and the DC voltage gradually increases back to 1pu. With the increased DC voltage, the additional power output from

Terminal 2 also reduces gradually until the DC voltage deviation is lower than 0.02pu. The frequency improvement in Case 4.3.3 is similar (lowest frequency improved from 49.4 Hz to around 49.6 Hz) comparing to that in Case 4.3.2 with k=0.01 shown in Fig. 4.13 (a).



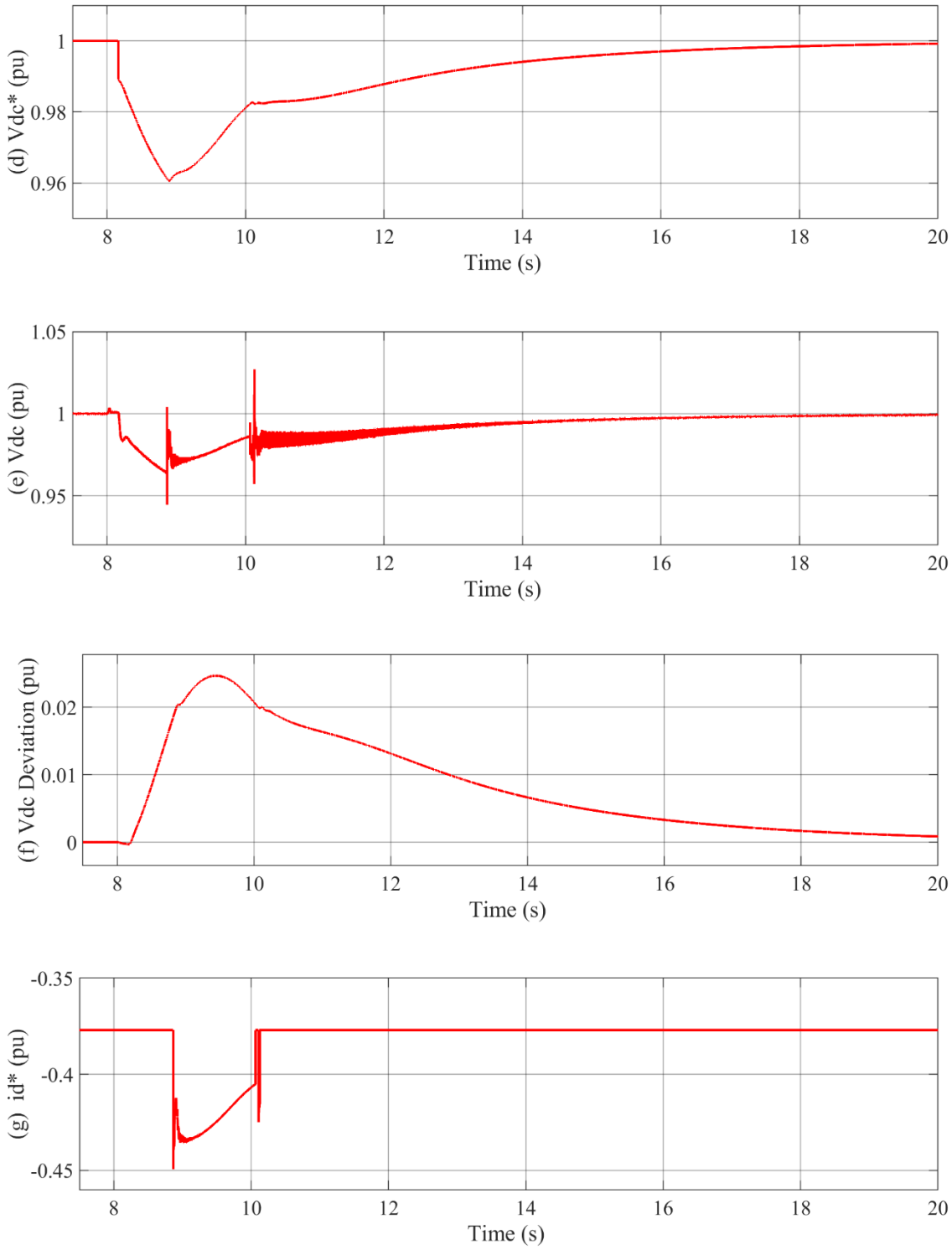


Fig. 4. 13 Waveforms in Case 4.3.3 at Terminal 1: (a) frequency, (b) frequency deviation, (c) power deviation, (d) DC voltage reference, and at Terminal 2: (e) DC voltage, (f) DC voltage deviation detected and (g) active power reference.

4.3.4 Frequency support with load increase at voltage control terminal with different k_1

The same system and load increase event from Case 4.3.3 is used in this case with fixed k_2=2 and various k_1=0.008, 0.01 and 0.012, respectively, in order to study the influence of different values of k_1 on the frequency support performance.

The frequency dynamics at Terminal 1 under frequency support in Case 4.3.4 with difference values of k_1 are shown in Fig. 4.14 (a). Lowest frequency increases from 49.55 Hz to 49.67Hz with k_1 increases from 0.008 to 0.012. With k_1=0.014, the frequency is improved further to 49.69 Hz before the control at Terminal 2 is switched out. However, it drops slightly back to 49.67 Hz since the local generation at Terminal 1 takes some time to fulfil the power shortage. Fig. 4.14 (b) shows the DC voltage reference for the controller at Terminal 1 indicating that big DC voltage reduction with higher value of k_1 in order to make the controller at Terminal 2 switch in earlier and produce higher additional power transferred to Terminal 1.

At Terminal 2, the DC voltage deviation is detected and generated through a low-pass filter shown in Fig. 4.14 (c), which switches in the controller at Terminal 2 when it exceeds 0.02pu and switches out when it is smaller than 0.01pu. It can be seen that the voltage deviation exceeds 0.02 earlier as well as delivers higher gain for the power reference with higher value of k_1 as shown in Fig. 4.14 (d). As more power is transferred to Terminal 1 during frequency support with higher value of k_1, it gives better frequency performance at Terminal 1.

Although better frequency support performance can be achieved by higher value of k_1, design of k_1 should be carefully considered to include its impact at Terminal 2.

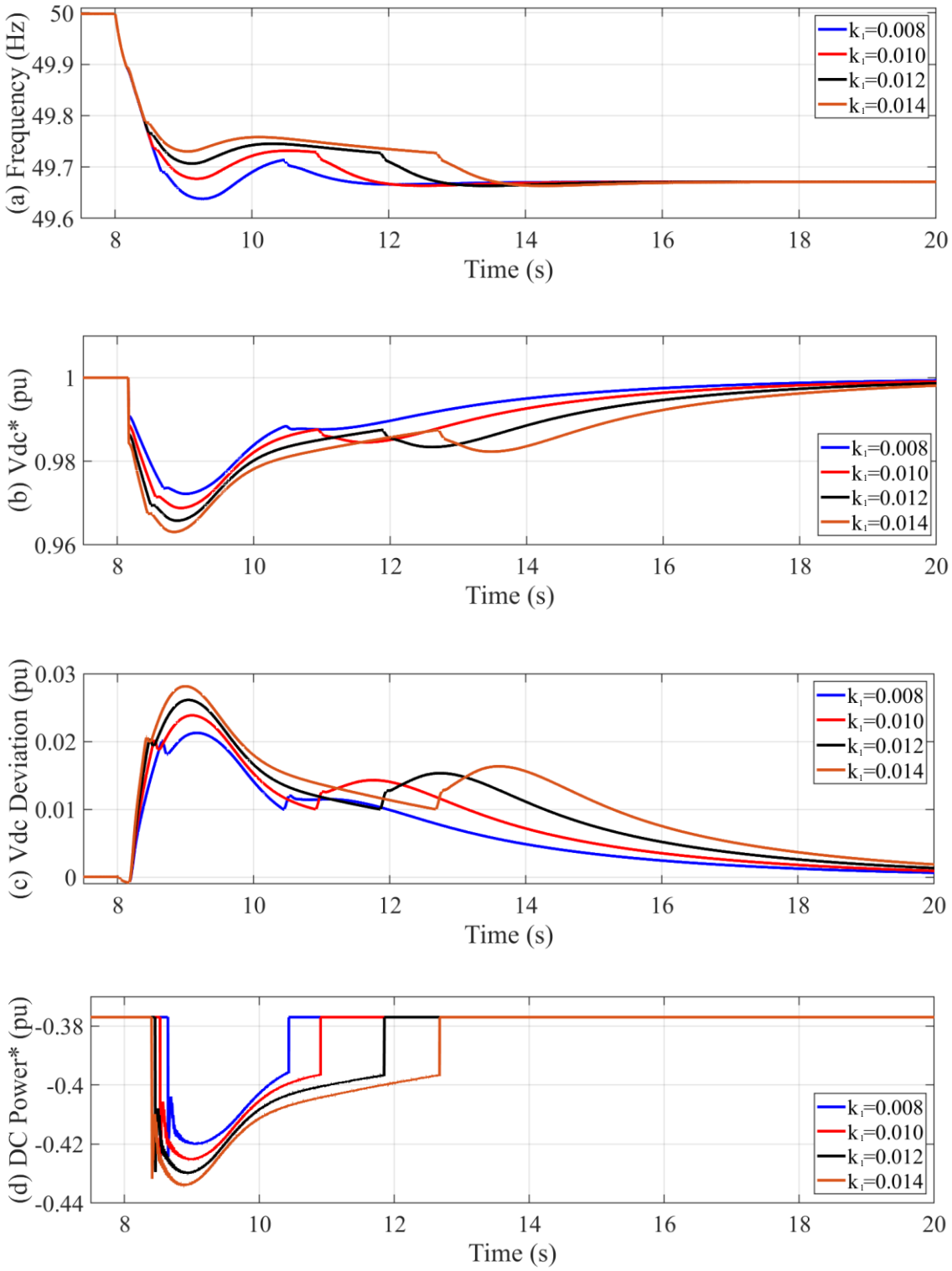
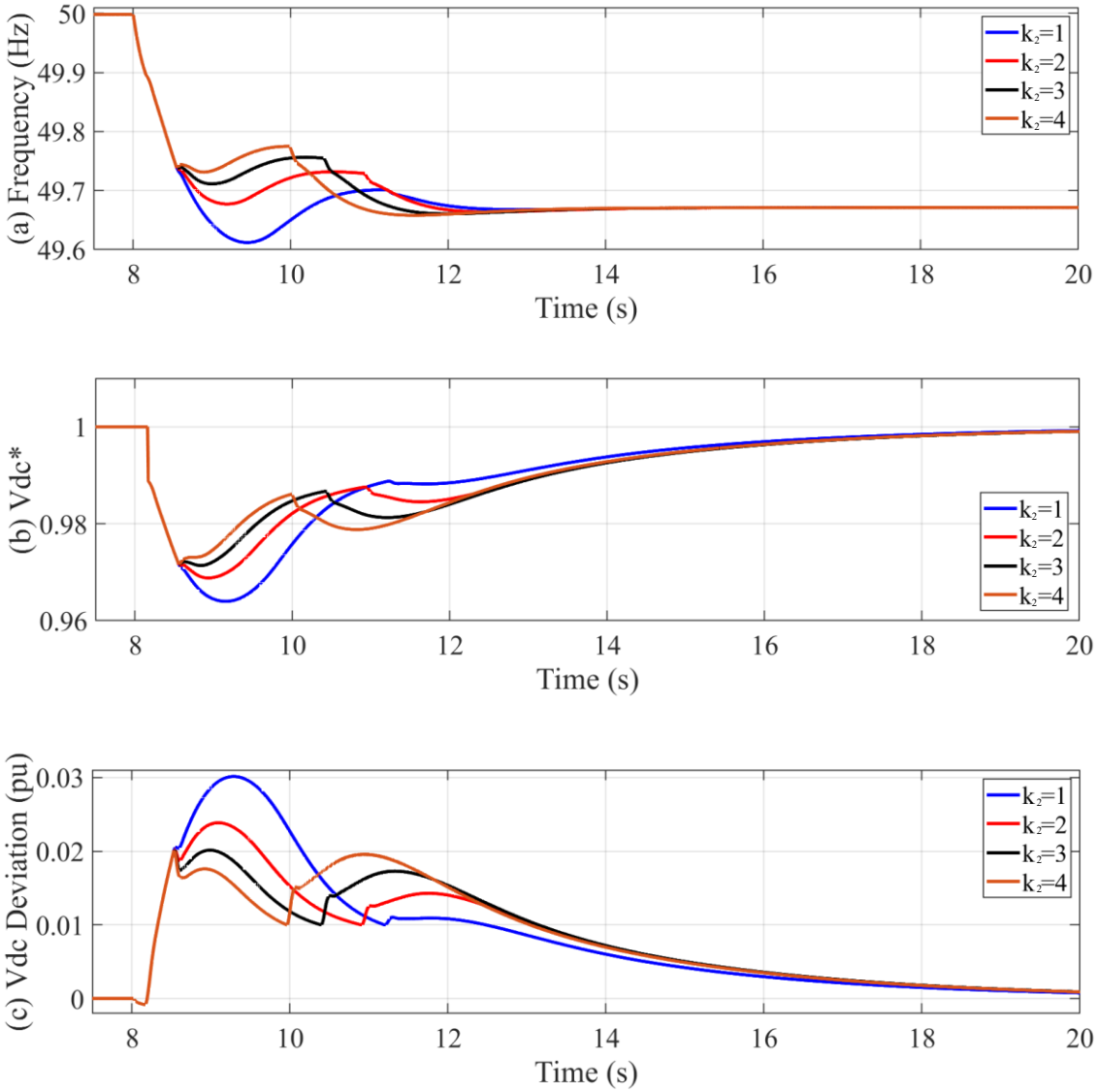


Fig. 4. 14 waveforms in Case 4.3.4 at Terminal 1: (a) frequency, (b) DC voltage reference for the current control loop, and at Terminal 2: (c) DC voltage deviation, (d) overall active power reference for the current control loop.

4.3.5 Frequency support with load increase at voltage control terminal with different k_2

The same system and load increase event from Case 4.3.4 is used in this case with k_1=0.01 and k_2=1, 2, 3 and 4, respectively, in order to study the influence of different values of k_2 on the frequency support performance.



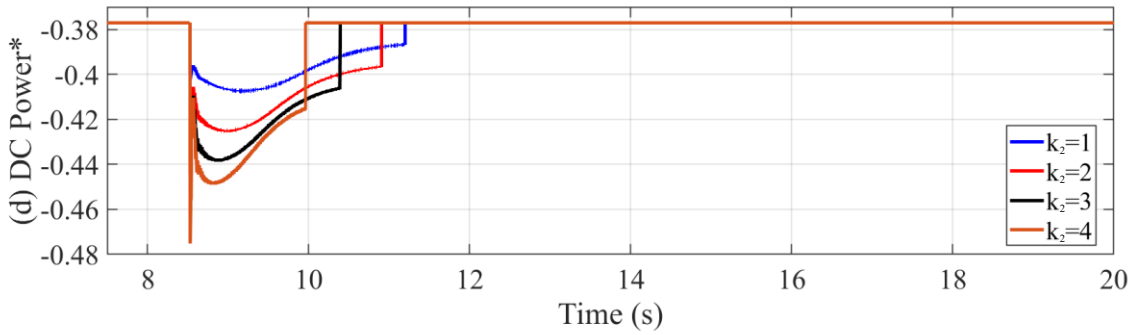


Fig. 4. 15 waveforms in Case 4.3.5 at Terminal 1: (a) frequency, (b) DC voltage reference, and at Terminal 2: (c) DC voltage deviation, (d) active power reference.

The frequency dynamics at Terminal 1 with difference values of k_2 are shown in Fig. 4.15 (a). It can be seen that the lowest frequency is improved with higher k_2, and the frequency support time period is also shorter. This can also be verified from Fig. 4.15 (b) that the voltage recovers back to 1pu faster after controller at Terminal 2 is switched in, indicating the frequency drop at Terminal 1 is restrained faster with higher value of k_2.

At Terminal 2, the DC voltage deviation detected after the low-pass filter is shown in Fig. 4.15 (c). With higher value of k_2, more power is transmitted to Terminal 1 from Terminal 2 as shown in Fig. 4.15 (d), leading to faster recovery of AC frequency and DC voltage, and shorter period of frequency support. However, with high k_2, the frequency support is withdrawn quicker, potentially leading to further shortage of active power in Terminal 1 and further frequency drop as can be seen in Fig. 4.25 (d), especially for k_2=4.

4.4 Three-terminal network cases studies

The system studied in this section has been introduced in Section 4.1 and shown in Fig. 4.2. MMC 1 and MMC3 control active power whilst MMC2 controls the DC voltage. To better support the frequency during active power imbalance in one of the three AC terminals, the other two terminals should share the power shortage.

4.4.1 Terminal 1 frequency used as reference with different k_3

The control shown in Fig. 4.3 is equipped at MMC1 and MMC3 with parameter k represented as k_1 and k_3 respectively in this case. The power shortage is shared between Terminal 2 and 3 during an event at Terminal 1. However, in order to enable Terminal 3 to participate into frequency support, communication between Terminal 1 and 3 is required. Thus, frequency at Terminal 1 is taken as the reference for frequency support control at Terminal 3 (with 50ms communication delay) to deliver additional power to Terminal 1.

As Terminal 2 control DC voltage, it will automatically balance the power on the DC network during the frequency support. For the same k_1 value at Terminal 1, the additional power will be identical to the previous cases resulting in same frequency response. As way of example, frequency improvement at Terminal 1 with fixed k_1=0.05 is shown in Fig. 4.16. Therefore, the study in this case is focused on the frequency performance at Terminal 2 and 3 during the frequency support period.

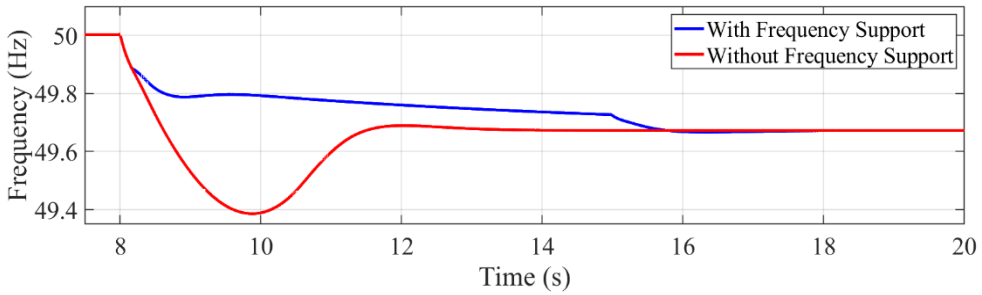
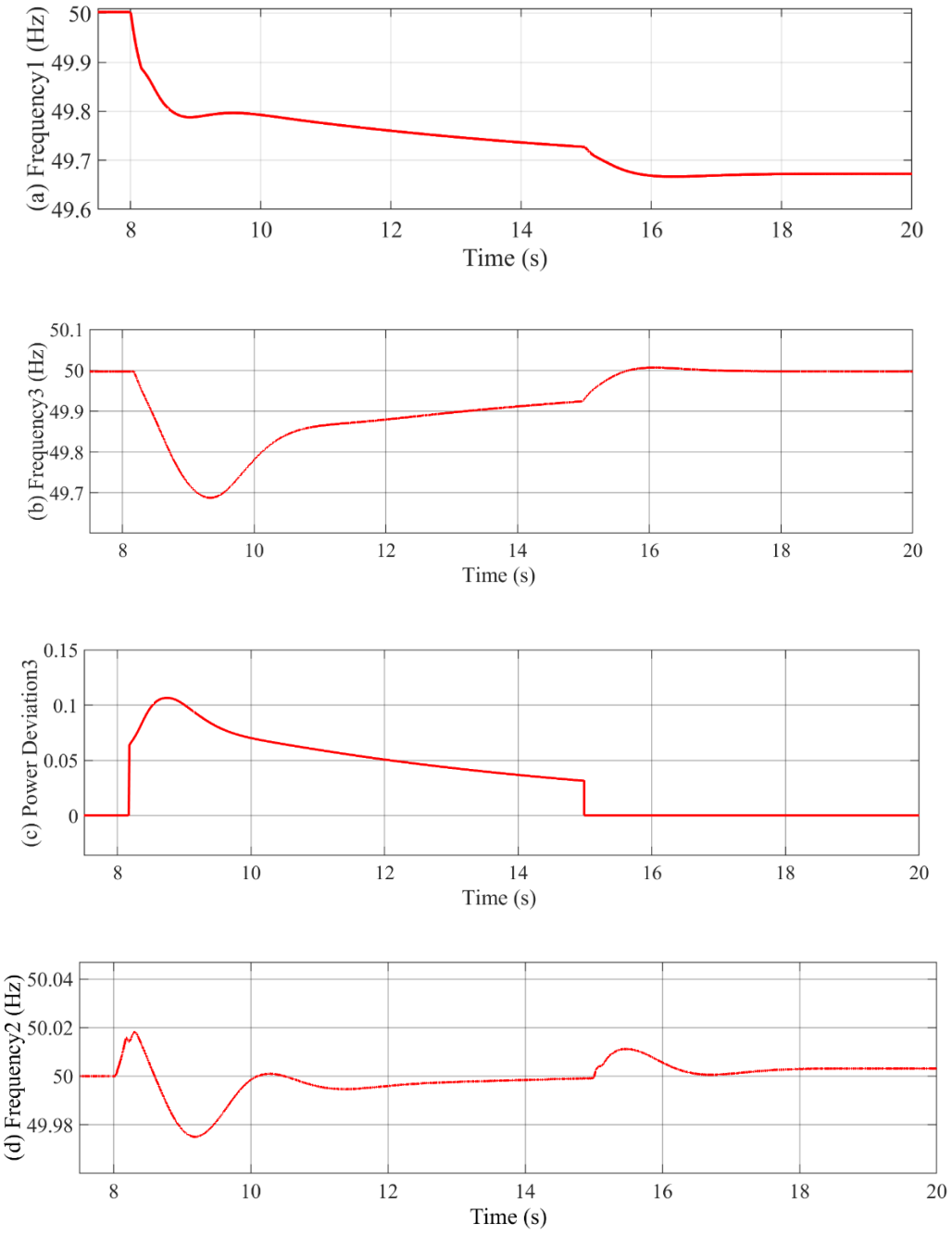


Fig. 4. 16 Frequency at Terminal 1 with and without frequency support

Fig. 4.17 shows waveforms with k_1=0.05 and k_3=0.05. In Fig. 4.17 (c), a power deviation is generated based on the frequency at Terminal 1 shown in Fig. 4.17 (a). the frequency support control at Terminal 1 is switched in and out when frequency deviation at Terminal 1 is higher than 0.1 Hz and lower than 0.01 Hz, respectively. The control implemented at Terminal 3 is switched in and out 50ms (communication delay) later than

that at Terminal 1. The additional power transferred from Terminal 3 to 1 during the frequency support period can be seen from the active power reference at Terminal 3 shown in Fig. 4.17 (c). The power surplus transmitted to Terminal 1 from the voltage control terminal (Terminal 2) is shown in Fig. 4.17 (e). From Fig. 4.17 (b) and (d), the frequency at Terminal 3 and 2 drops to 49.69 Hz and 49.97 Hz respectively, in order to support the frequency at Terminal 1.



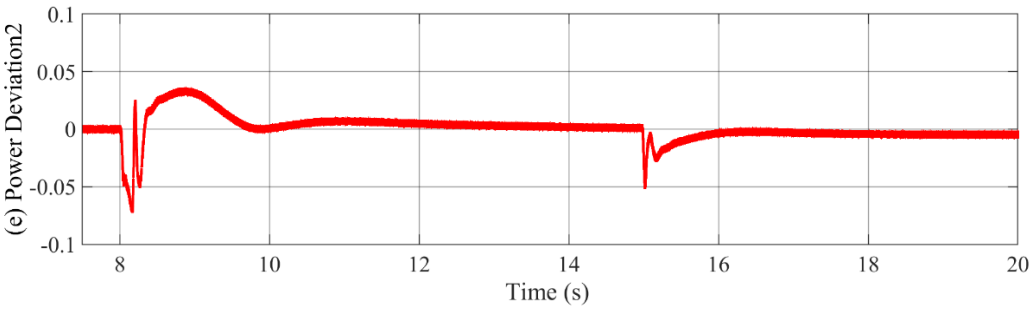


Fig. 4. 17 Simulated waveforms: (a) frequency at Terminal 1, (b) frequency at Terminal 3, (c) power deviation generated at Terminal 3, (d) frequency at Terminal 2 and (e) power deviation at Terminal 2.

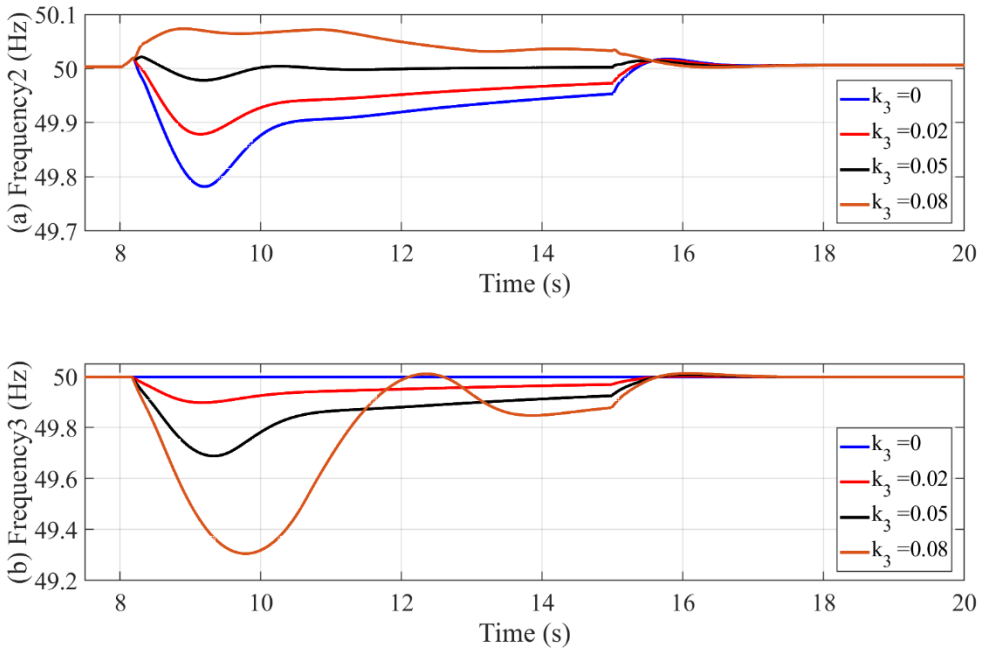


Fig. 4. 18 Frequency in Case 4.4.1 at (a) Terminal 2 and (b) Terminal 3 with different values of k_3.

Since Terminal 2 is controlling the DC voltage, it will balance the generation and demand on the DC network when additional active power is required by Terminal 1 during the frequency support period. This means the additional power required from

Terminal 2 is the difference between Terminal 1 and 3. As can be seen from Fig. 4.18, the total power shortage at Terminal 1 is thus shared by Terminal 2 and 3. With higher value of k_3, Terminal 3 shares more power than Terminal 2, leading to larger frequency drop at Terminal 3 than at Terminal 2. In the case when k_3=0.08, Terminal 3 produces more power than that required at Terminal 1 (as k_1=0.05) and thus Terminal 2 actually results in power surplus. Consequently, this leads to severe frequency drop at Terminal 3 (minimum frequency of 49.3 Hz shown in Fig. 4.18 (b)) and frequency increase at Terminal 2 (shown in Fig. 4.18 (a)). Therefore, the value of k_3 should be designed to be less than k_1 and carefully considering the capacities of Terminal 2 and 3 (3000 MW and 2000MW generator for Terminal 2 and 3 in the study, respectively), e.g. more power shortage should be shared by Terminal 2 as it has higher capacity than Terminal 3.

As to achieve minimum frequency drop at both terminals while fulfil the frequency support for Terminal 1, another improved method for power shortage sharing between Terminal 2 and 3 is discussed in Case 4.4.2.

4.4.2 Terminal 2 and 3 frequencies used as references

The control implemented at Terminal 3 is shown in Fig. 4.19. As to achieve minimum frequency drop at both Terminal 2 and 3 (more power is shared by the terminal with higher capacity) during the frequency support, the additional power provided by Terminal 3 is controlled such that its frequency deviation follows that at Terminal 2. After additional power is required by Terminal 1, being the active power controlling terminal, Terminal 2 increases its power output to Terminal 1 causing its AC frequency to drop. Such frequency drop is communicated to Terminal 3 so its output power is also increased accordingly. The power shortage is shared between Terminal 2 and 3 automatically to ensure they have similar frequency variation. Consequently, more power is shared by the AC network with higher capacity (Terminal 2 in this case).

With the same control used at Terminal 1 as in Case 4.4.1, same frequency improvement of Terminal 1 can be shown by Fig. 4.16. On the other two terminals, it can be seen from Fig. 4.20 (a) and (b) that the frequency at Terminal 3 is controlled to be similar to that at Terminal 2. The power share can be calculated from Fig. 4.20 (c) and (d)

that maximum power output increase of 150 MW and 100MW at Terminal 2 and 3 respectively, indicating that both terminals share the total power shortage largely according to the ratio of their capacities (3000 MW and 2000MW generators for Terminal 2 and 3 respectively). Thus, the frequency support is achieved with the minimum overall frequency drop on Terminal 2 and 3 automatically.

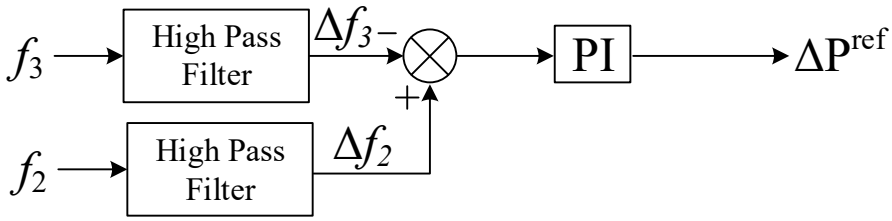
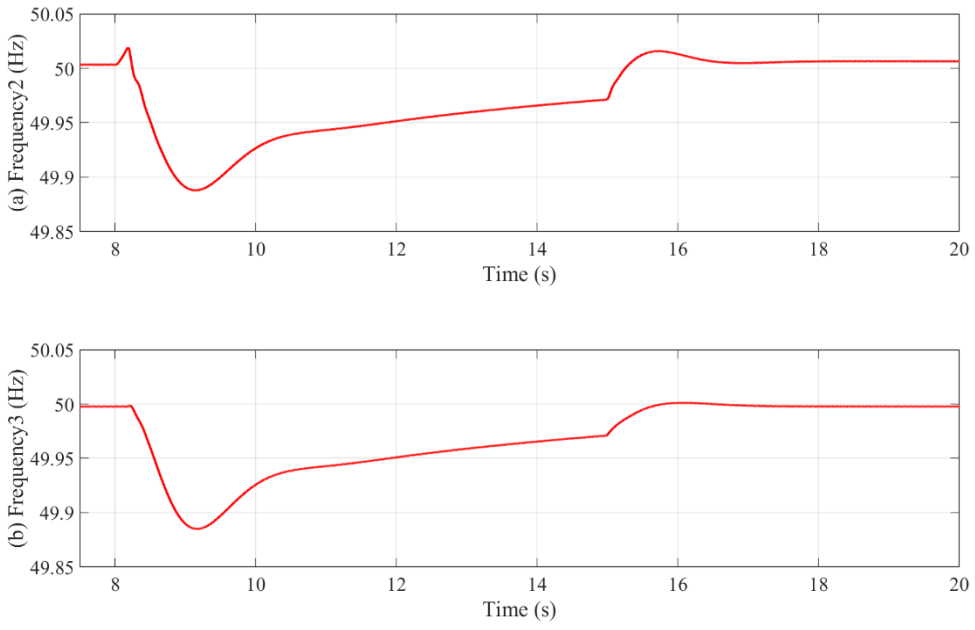


Fig. 4. 19 Diagram of frequency support control implemented at Terminal 3.



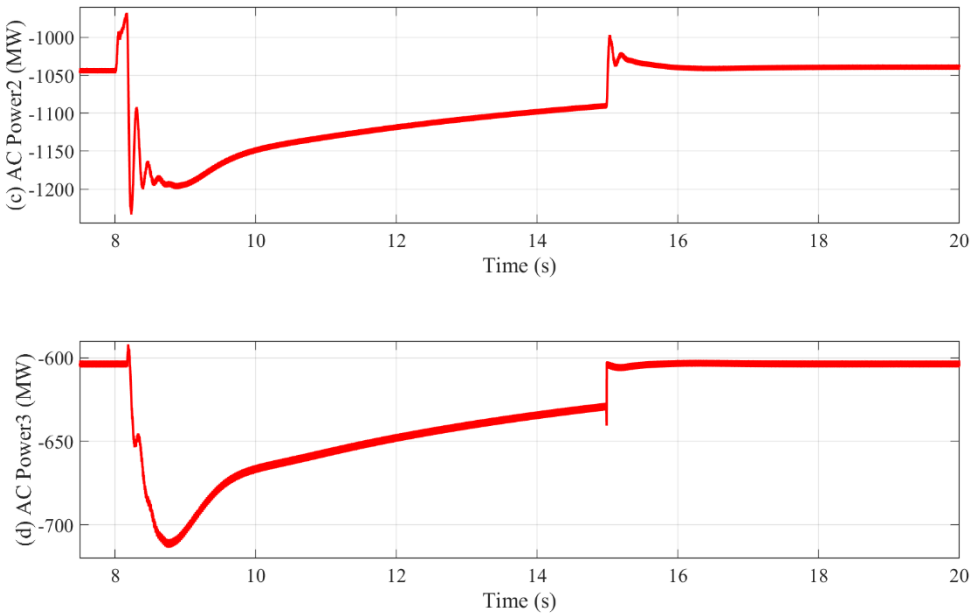


Fig. 4. 20 Waveforms of frequency at (a) Terminal 2, (b) Terminal 3, and DC power at (c) Terminal 2, (d) Terminal 3.

4.4.3 Three-terminal system frequency support with load increase at DC voltage control terminal

In this section, the load increase happens at voltage control terminal, similar to the Case 4.3.3 in Section 4.3.3. In this case, the same system shown in Fig. 4.2 is implemented but Terminal 1 now controls DC voltage and Terminal 2 and 3 control active power. The power is transferring from Terminal 2 and 3 to 1 under nominal operation. A 20% load increase is placed at Terminal 1 at time of 8s. After frequency deviation exceeds 0.1 Hz (at time of 8.16s), the control shown in Fig. 4.11 is switched in to reduce the DC voltage.

With decreased DC voltage lower than 0.98pu is detected at Terminals 2 and 3, the same control shown in Fig. 4.12 (k_2 and k_3 at Terminal 2 and 3 respectively) is switched in at both terminals. With decreased DC voltage, additional active power is output from both terminals leading to frequency recovery at Terminal 1. Thus, frequency support can be achieved without communication between the terminals. The amount of power shared

between Terminal 2 and 3 during frequency support period is dependent on the ratio of value of k_2 and k_3.

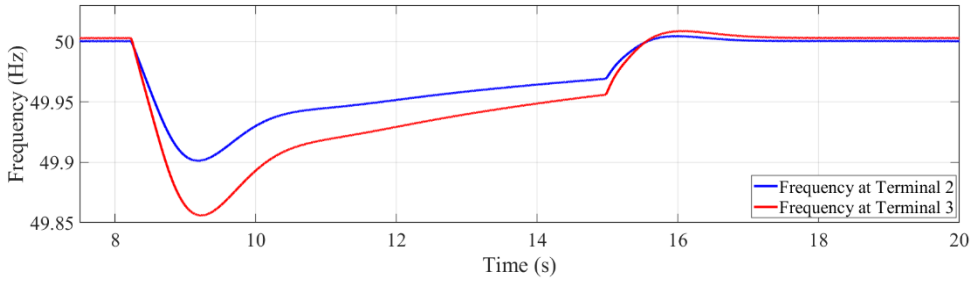


Fig. 4. 21 Frequency of Terminal 2 and 3 in Case 4.4.3 when k_2=k_3=2.

It can be seen from Fig. 4.21 that with same values of k_2 and k_3 (same amount of additional power is output from Terminal 2 and 3 during the frequency support period), the frequency drop of Terminal 3 is 50% more than that of Terminal 2, largely according to the ratio of the capacities of Terminal 2 and 3.

Similar results can be observed in Section 4.3.3 where higher values of k_2 and k_3 leads to faster and shorter period of frequency support as well as larger frequency drop at Terminal 2 and 3. The study in this case is thus focused on the power sharing between Terminal 2 and 3, and the results with variations of k_2 and fixed k_3=2 are shown in Fig. 4.22.

As seen from Fig. 4.22 (c) and (d), more power is shared by Terminal 2 with higher value of k_2. From the frequencies at Terminal 2 and 3 shown in Fig. 4.22 (a) and (b), the best overall frequency of Terminal 2 and 3 (minimum frequency at around 49.87 Hz at both terminals) can be achieved when k_2=3, which matches the ratio of k_2 and k_3 to that of the capacities of Terminal 2 and 3. This also verifies the results from Case 4.3.2 in this section.

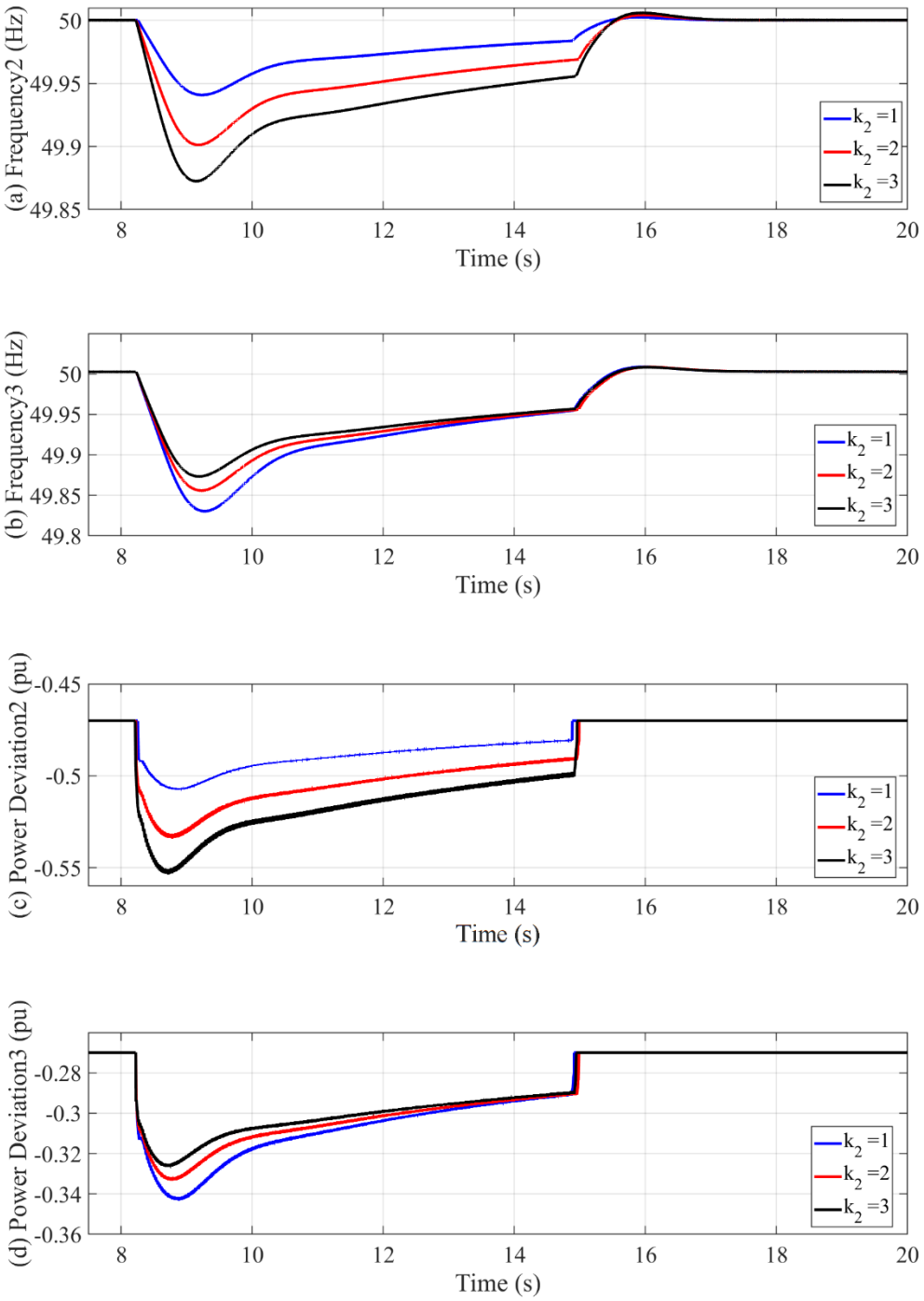


Fig. 4. 22 Waveforms of frequency with variations of k_2 and fixed k_3=2: (a) Terminal 2, (b) Terminal 3, and DC power reference at (c) Terminal 2, (d) Terminal 3.

4.5 Conclusion

Modelling and control of MMC-HVDC system, the use of HVDC system for power system frequency support have been studied in this chapter. Detailed simulations have been carried out to investigate and validate various system frequency support strategies.

In a two-terminal system, in a frequency event at the power controlling terminal, the active power output from the converter can be directly modulated to provide frequency support to the affected AC network. In contrast, for a frequency event at the DC voltage controlling terminal, through active DC voltage manipulation by the converter controlling the DC voltage, and active power modulation by the power controlling terminal upon the detection of DC voltage derivation can also provide fast and effective frequency support to the affected AC network. Different parameter designs have also been discussed and their impact on frequency response studied.

For a multi-terminal HVDC system connecting different AC networks, power shortage sharing among the supporting terminals needs to be optimized. AC networks with higher capacities should likely to share more power than those with lower capacities, so as to improve the overall system frequency. Different design options considering frequency events at both power controlling and Dc voltage controlling terminals have been discussed. In a frequency event at one of the power controlling terminals, the active power output from the other converters can be better shared by modulating the active power according to the resultant frequency derivation during the frequency support process. In contrast, for a frequency event at the DC voltage controlling terminal, power sharing from the remaining power controlling terminal can be controlled by properly setting up their droop constants, e.g. according to the network capacitor, so as to provide similar frequency performance at the healthy AC networks.

Chapter 5 Impact of DC Protection Strategy on Frequency Response of the Connected AC System

For a future large multi-terminal HVDC network, such as the proposed North Sea Super Grid [150, 151], the power transfer capability can be in the order of tens of gigawatts. Thus, in the event of a fault on the DC network, it potentially can disrupt the whole power transmission for a considerable time. Therefore, one of the most important concerns is how the DC protection strategy can impact on the connected AC system performance, e.g. system frequency. The maximum loss-of-infeed for an AC network is highly dependent on the duration of the power outage, and the impacts of DC fault protection arrangements which result in different speed of power restoration on the connected AC system, on the system frequency, have not been properly understood. Different DC protection arrangements using DC disconnectors, fast and slow DC circuit breakers on frequency response of the connected AC networks are thus investigated in this chapter. A 3-terminal meshed HVDC system based on HF-MMC is studied to demonstrate system behaviour during DC faults.

5.1 System Layout and Control Requirements

The proposed 3-terminal MTDC network is shown in Fig. 5.1 where Station 1, 2 and 3 are rated at 3GW, 2GW and 1GW respectively. The rated DC voltage is ±400kV. Station 1 acts as the mater DC voltage controller whereas Station 2 regulates active power flowing into the AC Network 2 which contains two synchronous generators SG1 and SG2 with capacity of 2GVA and 1GVA, respectively. Station 3 controls its power export from DC to AC Network 3. Both AC network 1 and 3 are modelled as voltage sources behind certain impedances with SCRs being 4.2 and 12.5, respectively. The loads on AC Network 2 are modelled as constant power load with unit power factor. More specific parameters are shown in Table 5.1 and 5.2.

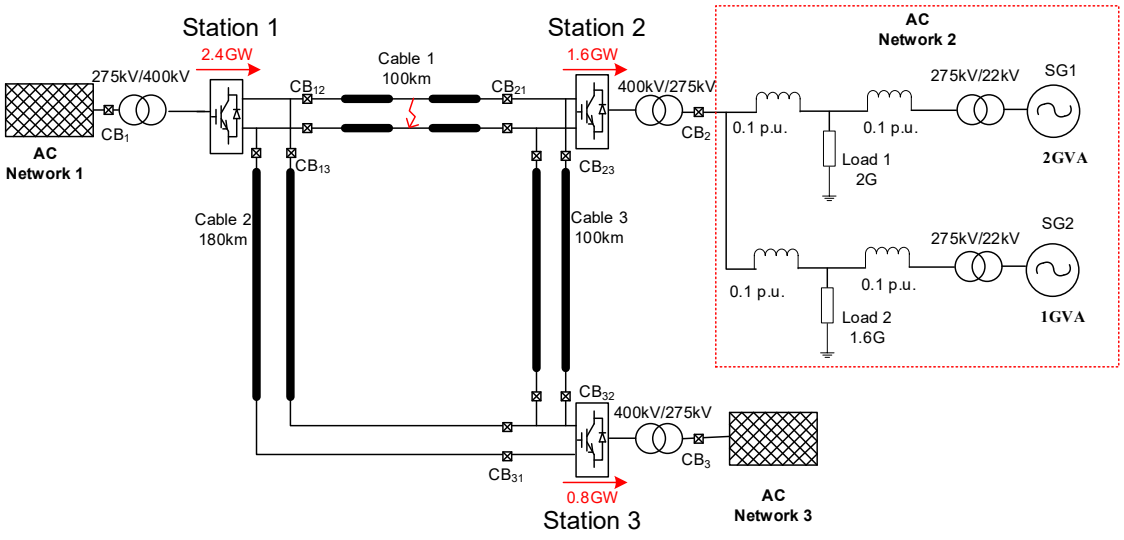


Fig. 5. 1 Block diagram of a three terminal MMC based MTDC network.

Table 5. 1 Converter and cable parameters

Parameters	**Symbol**	**Nominal Value**
Rated DC voltage	V_{dc}	$\pm$400 kV
Power rating of Station 1	P_1	3000 MW
Power rating of Station 2	P_2	2000 MW
Power rating of Station 3	P_3	1000 MW
Transformer reactance and resistance (400/275 kV)	X_{trm}, R_{trm},	0.2 p.u. 0.0045 p.u.
Number of SM per arm	N	320
SM DC voltage	V_{sm}	2.5 kV
SM capacitance	C_{sm}	7.9 mF
Arm inductance	L_{arm}	30 mH
Station DC terminal inductance	L_t	100 mH

Length of Cable 1, 2, and 3	L_1, L_2, L_2	100, 180, 100 km
R, L and C per unit length of cable	R_{cable}, L_{cable}, C_{cable}	9 mΩ/km, 1.4 mH/km, 0.23μF/km
Number of pi section	N_{pi}	10

Table 5. 2 Synchronous generators parameters

Parameters	**Symbol**	**Nominal Value**	
		SG1	**SG2**
Rated voltage	V_s	22kV	22kV
Nominal power	S	2GVA	1GVA
Power factor	pf	0.6	0.8
Nominal frequency	f	50Hz	50Hz
Pole pairs	pp	1	1
Nominal speed of SG		3000rpm	

In this study, the converters are modelled as HB-MMC average models in all the three stations [152], and π section models are used for DC cables with the lengths indicated in Fig. 5.1. The average HB-MMC model (taking the upper arm of phase a as an example) is shown in Fig. 5.2 [153].

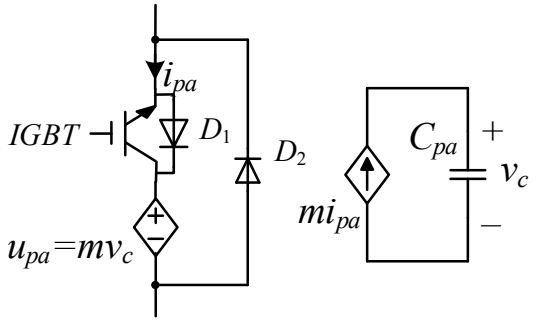


Fig. 5. 2 Block diagram of HB-MMC model of the upper arm of phase a.

The arm capacitor C_{pa} is charged by a controlled current source and the arm output voltage is represented by a controlled voltage source. The capacitor charge current and the arm voltage output voltage is determined by the modulation function *m*. Since only one capacitor is used per arm shown in Fig. 5.2, the SM capacitor voltage balancing is not considered. The whole average HB-MMC model uses 6 arm models as in Fig. 5.2 to simulate MMC behaviour under different operating conditions. During normal operation, the IGBT is always on and as $m>0$ for HB-MMC, D_2 is reverse biased and u_{pa} appears at the arm terminals. In MMC blocking state, the IGBT is switched off and *m* is set to 1, the arm current flows through either D_1 or D_2 depending on its direction, so as to emulate the behaviour of the HB-MMC. The basic controls of the HB-MMCs are the same as those introduced in Chapter 3.

The SGs in AC Network 2 is modelled in the same way as in Chapter 3. The loads in the AC Network 2 are modelled as pure resistance load, whereas AC Network 1 and 3 are modelled as AC voltage source in order to accelerate simulation speed.

5.2 Protection Strategies

Three different DC fault protection arrangements based on the use of different equipment are considered in the proposed 3-terminal MTDC network including:

- DC switches/disconnectors (DCSWs, which can only open when the current becomes zero) together with AC circuit breakers (ACCBs),
- fast DC circuit breakers (DCCBs) with operation speed of 5ms,
- slow DCCBs with operation speed of 20ms

All three protection arrangements use the same fault detecting and locating principle which is introduced in the following sections.

5.2.1 Fault detection and locating

Since DC faults cause severe voltage drop, converters at all three stations are equipped with overcurrent protection as the main protection with the under voltage protection as backup systems which is trigged when the measured DC current is over $2\ p.u.$ When the fault happens, the main protection system should operate as design requirement. The backup protection is used for the fault isolation when the main protection or the circuit interrupters are failed to operate.

Many DC fault locating methods have been studied [20, 22, 23, 154]. A 'Handshaking' approach was proposed in [23], which is the method that employed in this paper to identify and isolate the faulty branch in the proposed system. The basic idea of fault locating is illustrated in Fig. 5.3.

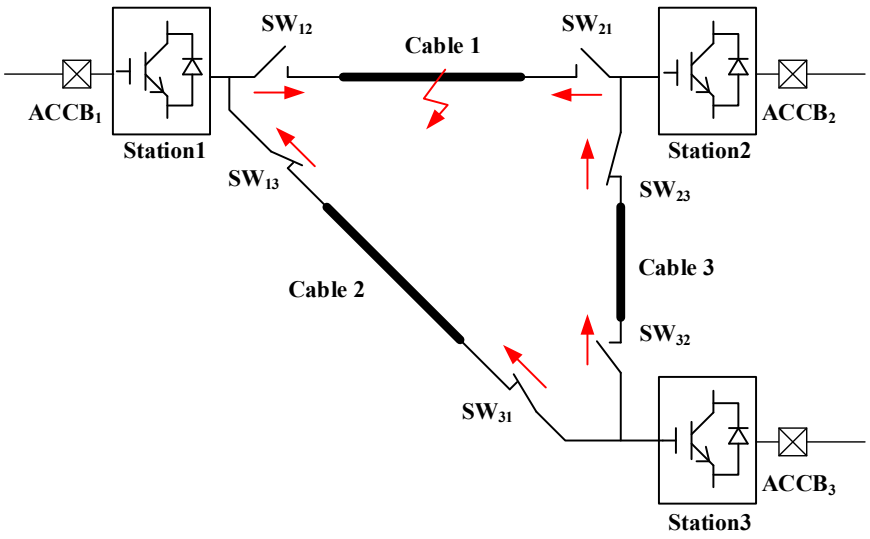


Fig. 5. 3 Diagram of 'Handshaking' approach.

With the 'Handshaking' approach, when a DC fault happens, the DC fault current ($I_{dc} > 2\ p.u.$) flowing through SWs are labelled depending on its direction by the converter stations shown in Fig. 5.3. The fault current is positive when flowing into the cable, and negative when flowing out of the cable. If multiple positive cable current are detected by one station, only the SW with the largest positive current is selected. The selected SWs are considered connecting to potential faulty lines, and they are opened to isolate the faulty area. In order to restore power transmission after fault isolation, the opened SWs connecting to the healthy cables will need to be reclosed when reclose conditions are fulfilled (SWs with voltage on both sides are recovered to nominal value during restoring process). For an example, when a fault happens on Cable 1 with fault currents (red arrows) shown in Fig. 5.3, the DC fault current will be labelled as positive at SW_{12}, SW_{21}, SW_{31} and SW_{32}, and thereby SW_{12}, SW_{21} and SW_{32} (with higher fault current than that of SW_{31}) are respectively selected by Station 1, 2 and 3 to be opened. Meanwhile Cable 1 and Cable 3 are considered as potential faulty lines. In the restoring process, the SW_{32} will be reclosed when the voltage on both sides are recovered (as voltage only on one side of SW_{12} and SW_{21} is recovered with fault on Cable 1).

5.2.2 Sequence of protection based on DCSWs

Under the protection arrangement using DCSWs shown in Fig. 5.3, ACCBs are used to break the fault current, i.e., CB_1, CB_2 and CB_3 on the AC side of stations. Taking a DC pole-to-pole short circuit fault happens at the middle of Cable 1 as example, SW_{12}, SW_{21} and SW_{32} label the local fault current as positive. Then, all the converters are blocked and the ACCBs, i.e. CB_1, CB_2, and CB_3 are opened, to protect the converters and extinguish the fault current flowing into the DC network. When the DC fault current reduced to near-zero, SW_{12}, SW_{21}, and SW_{32} are opened to isolate the potential faulty cables. Upon isolation of the faulty cables, all the three ACCBs are then re-closed and converters are enabled in DC voltage control mode to recharge the DC network. Because SW_{23} remains closed, the voltage on Cable 3 is rebuilt by Station 2 and detected by SW_{32}. Therefore, SW_{32} will be subsequently reclosed after the recharge of Cable 3 and brought back online as the healthy branch. However, since the DCSWs can only be opened when the DC current falls to near zero, this protection strategy is relatively slow with the typical recovery time in the order of hundreds of milliseconds. The overall protection sequence can be seen from Fig. 5.4.

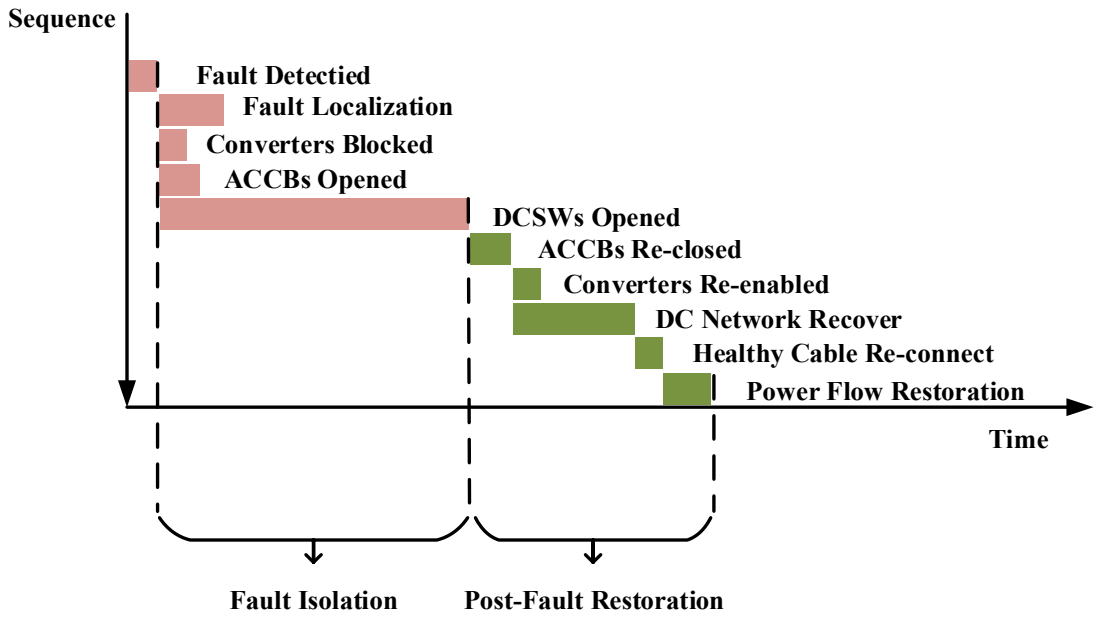


Fig. 5. 4 Diagram of sequence of protection based on DCSWs.

5.2.3 Sequence of protection based on DCCBs

In order to quickly isolate the fault and restore the healthy branches, the 'Handshaking' method can also be adopted when using DCCBs instead of DCSWs. With the same fault locating method, SWs on each end of DC cables shown in Fig. 5.3 are replaced by DCCBs (labelled as CB_{12}, CB_{21}, CB_{13}, CB_{31}, CB_{23} and CB_{32}). Under this protection arrangement, different DCCB technologies are considered late in the chapter, one based on hybrid type (fast acting DCCB) [78] with a typical opening time of 5ms and the other on mechanical type (slow acting DCCB) [155] with a typical opening time of 20ms. The short duration of such protection process leads to less impact on system frequency of the connected AC networks though the impact of the system recovery speed on acceptable maximum temporary "loss-of-infeed" is largely unknown.

The other difference from protection based on DCSWs is that since the fault is able to be isolated fast, ACCBs on the AC side are not required to act. Again, taking fault at the middle of Cable 1 as an example, all converters blocked, and CB_{12}, CB_{21} and CB_{32} label the local fault current as positive and thus opened, thereby the fault Cable 1 is isolated. Upon isolation of the faulty cables, all three converters are enabled in DC voltage control mode to recharge the DC network and then CB_{32} is reclosed for power flow restoration. Fig. 5.5 illustrates the overall protection process based on DCCBs.

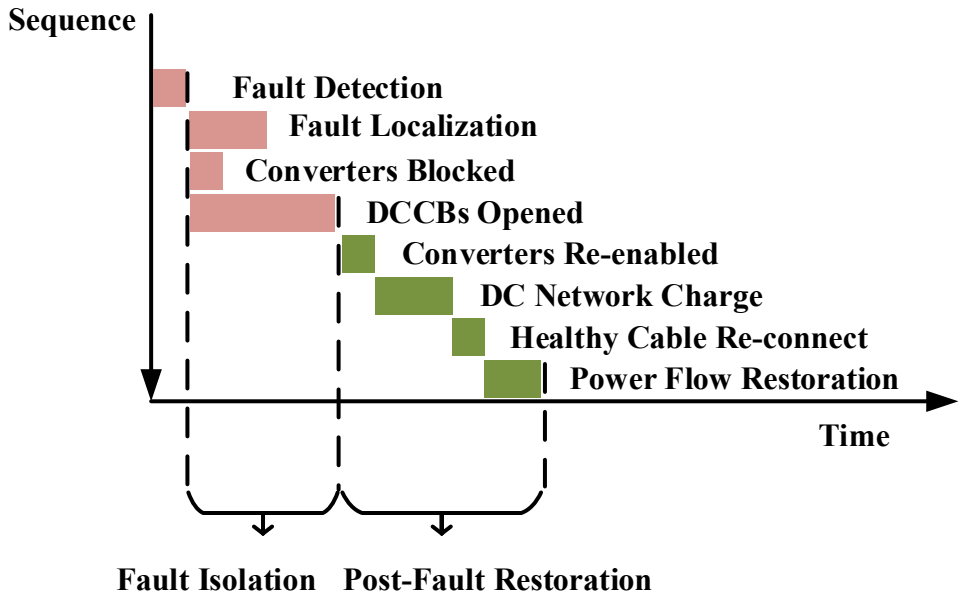
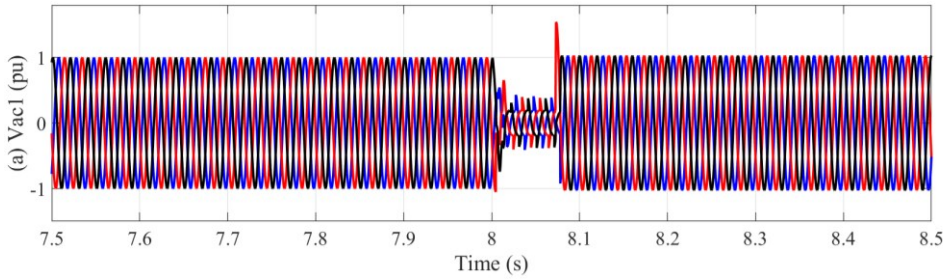


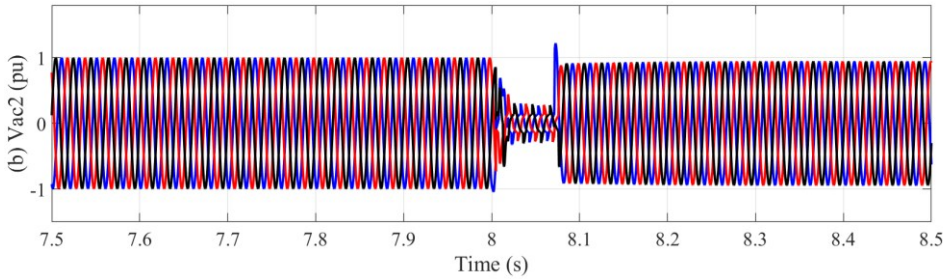
Fig. 5. 5 Diagram of sequence of protection based on DCCBs.

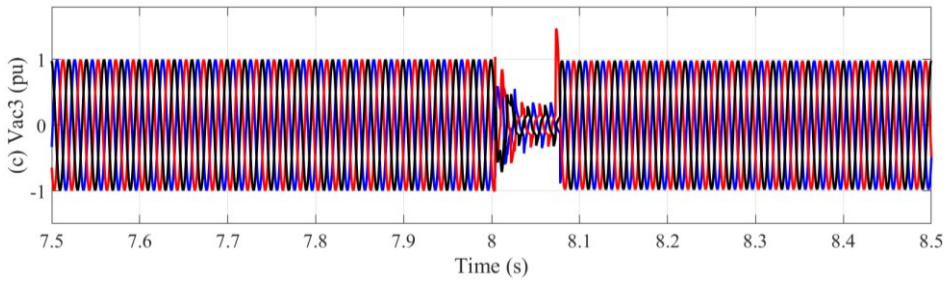
The frequency responses of AC Network 2 showing in Fig. 5.1 with the aforementioned three protection arrangements using DCSWs, slow DCCBs and fast DCCBs are studied and discussed late in the chapter.

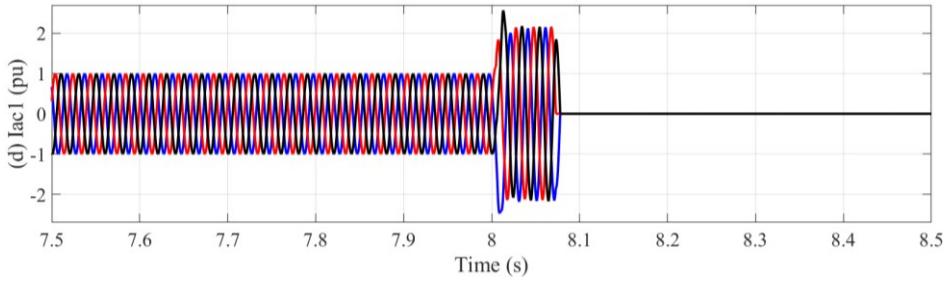
5.3 Fault characteristics

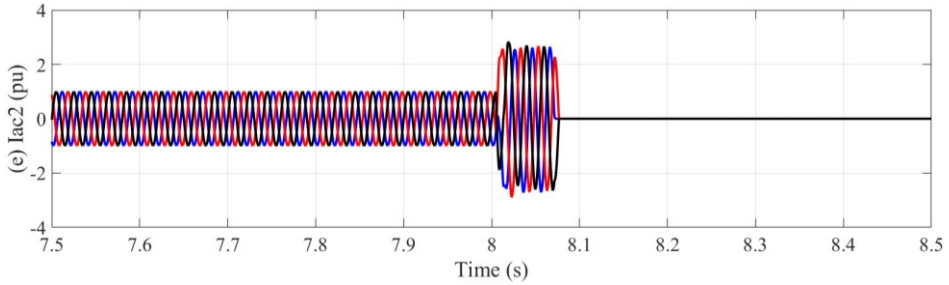
The typical system behaviour during a DC fault is illustrated here. A permanent DC pole-to-pole fault is applied in the middle of Cable 1 at 8s in the proposed MTDC system showing in Fig. 5.1. The converters are blocked within 5ms, 5ms and 4ms after fault initiation (when over current is detected) at Station 1, 2 and 3, respectively. All ACCBs are opened at time of 8.068s. No further protection actions are taken to observe the system fault behaviour.


(a) Vac1 (pu)
1
0
-1
7.5
7.6
7.7
7.8
7.9
8
8.1
8.2
8.3
8.4
8.5
Time (s)


(b) Vac2 (pu)
1
0
-1
7.5
7.6
7.7
7.8
7.9
8
8.1
8.2
8.3
8.4
8.5
Time (s)


(c) Vac3 (pu)
1
0
-1
7.5
7.6
7.7
7.8
7.9
8
8.1
8.2
8.3
8.4
8.5
Time (s)


(d) Iac1 (pu)
2
1
0
-1
-2
7.5
7.6
7.7
7.8
7.9
8
8.1
8.2
8.3
8.4
8.5
Time (s)


(e) Iac2 (pu)
4
2
0
-2
-4
7.5
7.6
7.7
7.8
7.9
8
8.1
8.2
8.3
8.4
8.5
Time (s)

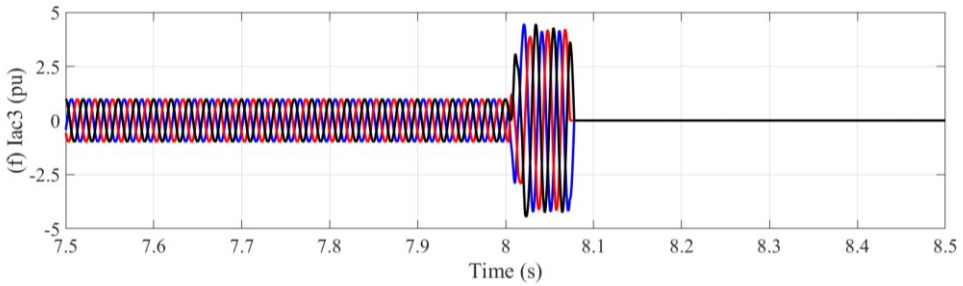
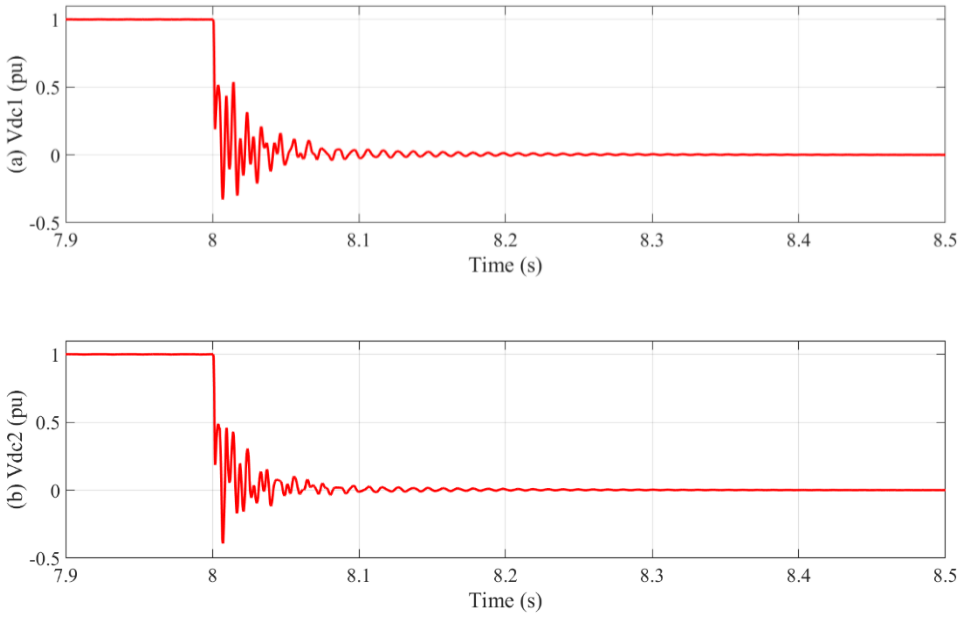


Fig. 5. 6 Voltage at AC side of (a) Station 1, (b) Station 2, (c) Station 3, and current at AC side of (d) Station 1, (e) Station 2 and (f) Station 3.

Fig. 5.6 shows the voltages and currents at AC sides of the three stations. From the voltage waveforms ((a), (b) and (c)) it can be seen that the AC voltage drops to around half of its normal value as the AC side is short circuited through the transformer by the faulty DC cable after fault initiation, and recovered back after ACCBs are opened From the AC current waveforms ((d), (e) and (f)), 2.1pu, 3pu and 3.5pu overcurrent are observed at Station 1, 2 and 3, respectively, during the fault, until they are interrupted by the ACCBs. The lower fault current in Network 1 is due to its relatively lower network strength (SCR) than the other two.



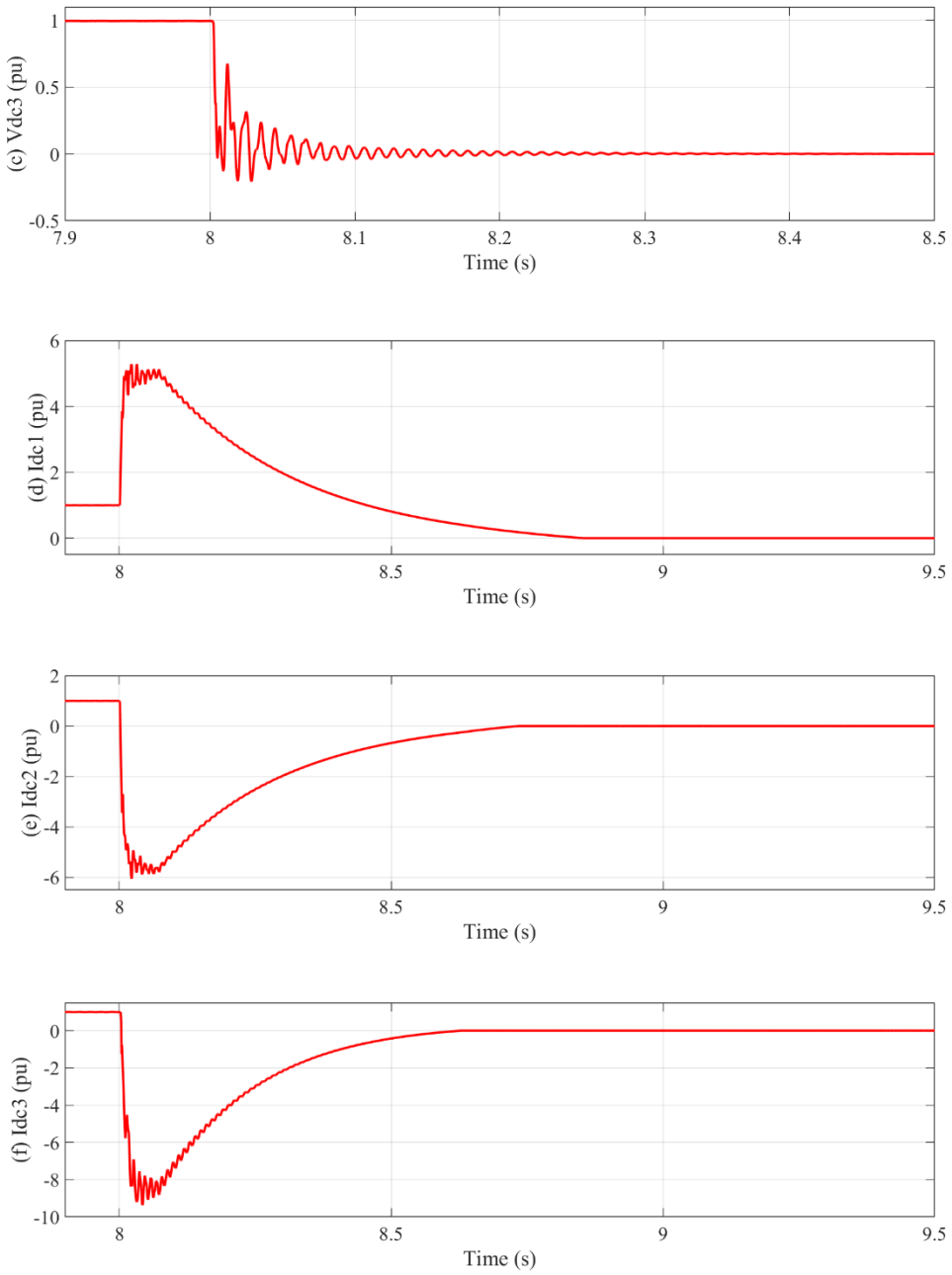
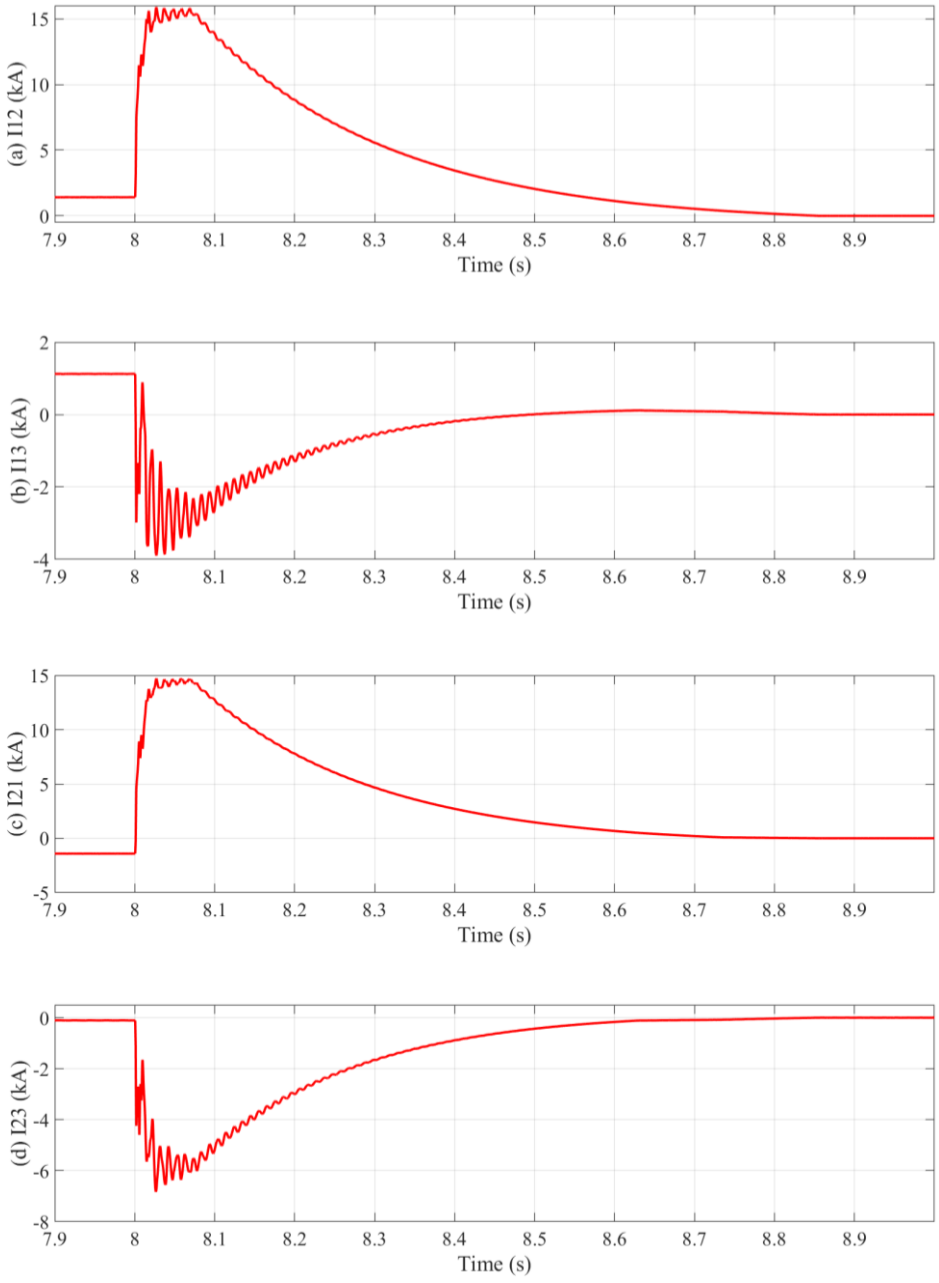


Fig. 5. 7 Voltage on DC side of (a) Terminal 1, (b) Terminal 2, (c) Terminal 3, and Current on DC side of (d) Terminal 1, (e) Terminal 2 and (f) Terminal 3.

Fig. 5.7 illustrates the voltage and current on the DC sides of the three stations. As seen from Fig. 5.7 (a), (b) and (c), all the DC voltage drop immediately after the fault and oscillate toward t zero. The DC terminal current shown in Fig. 5.7 (d), (e) and (f) increase

rapidly to around 5pu, 6pu and 9pu at Terminal 1, 2 and 3 respectively, contributed by the converter capacitor discharge (in the initial stage before converter blocking) and fault current injection from AC side. Since fault current injection is interrupted by ACCBs, the DC terminal current start to drop to zero gradually after about 600ms for all the three stations.



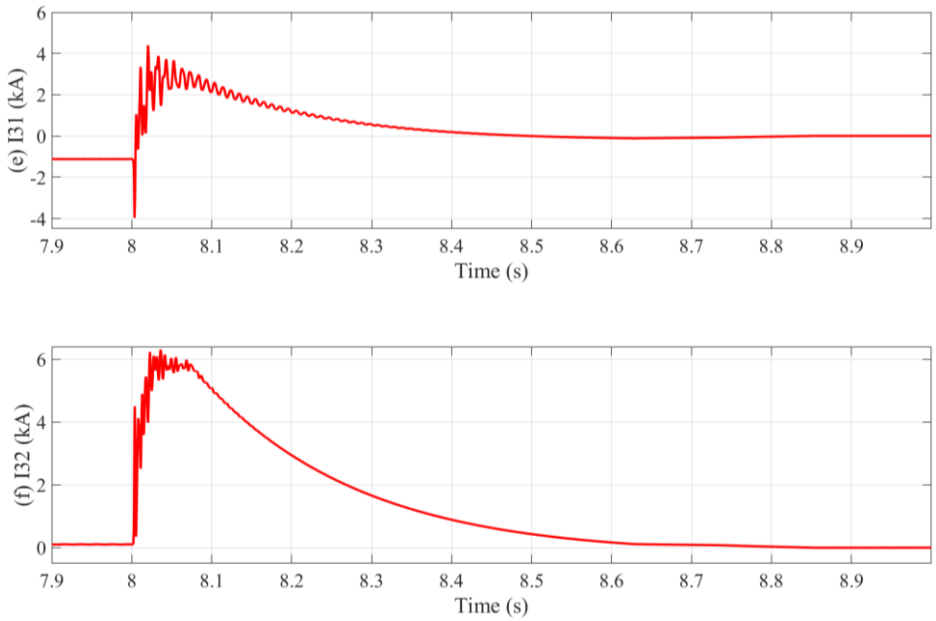


Fig. 5. 8 DC current flowing through (a) SW_{12}, (b) SW_{13}, (c) SW_{21}, (d) SW_{23}, (e) SW_{31} and (f) SW_{32}.

The DC current flow through the DC SWs are shown in Fig. 5.8. It can be seen that the DC current at SW_{12}, SW_{21}, SW_{31} and SW_{32} are positive shown in Fig. 5.8 (a), (c), (e) and (f), respectively. However, from Fig. 5.8 (e) and (f), it can be verified that the peak current at SW_{32} (6kA) is higher than that at SW_{31} (3.9kA). Thus, SW_{12}, SW_{21} and SW_{32} (not SW_{31}) are considered to be connected to potential faulty lines and can be selected to open when the 'Handshaking' approach is used. The current slowly drop to zero when the DC network is fully do-energized after the opening of the ACCBs, due to the low resistance on the DC network.

5.4 Simulation results

Three case studies of the impact of DC fault protection arrangements using DCSWs (Case 1), slow DCCBs (Case 2) and fast DCCBs (Case 3) on frequency response of connected AC Network 2 are carried out in this section. Prior to the DC fault, Station 2

and 3 transmit 1.6 GW and 0.8 GW to AC Network 2 and 3, respectively, as indicated in Fig. 5.1.

5.4.1 Protection arrangements using DCSWs

In Case 1, the proposed 3-terminal MTDC system is protected using ACCBs and DCSWs. A permanent DC pole-to-pole fault is applied at the middle of Cable 1 at 8s. Converters at Station 1, 2 and 3 detect the overcurrent flowing through the converter arms ($I_{arm} \geq 2\ p.u.$) and are then blocked at 8.005s, 8.005s and 8.004s respectively, to protect converter components. Meanwhile, Cable 1 and 3 are considered as potential faulty lines by CB_{12}, CB_{21} and CB_{32} from the measured DC fault current polarity under the 'Handshaking' principle. The ACCBs, i.e. CB_1, CB_2 and CB_3 are opened with 60ms delay after respective AC overcurrent detection ($|I_{ac}| \geq 2\ p.u.$) at time of 8.008s. Upon the isolation of the AC terminals, the DC network start to discharge, and CB_{12}, CB_{21} and CB_{32} are opened at 8.845s, 8.850s and 8.840s respectively as the DC currents on Cable 1, 2 and 3 took considerable time to drop to 20 A due to low resistance of the DC cables. Once the faulty branch is isolated, all ACCBs are reclosed with 20ms communication delay at time of 8.870s. Converters at the three stations are de-blocked at 8.192s and start to re-recharge Cable 2 through CB_{13} and CB_{31}, and Cable 3 through CB_{23}. CB_{32} is re-closed at 9.210s when the magnitude of the DC voltage on Cable 3 is recover to the proper range. The time sequence of the protection actions is summarised in Table 5.3.

Table 5. 3 Protection sequence in Case 1

Time	**Events**
8s	A permanent DC fault initiated at Cable 1.
8.005s	Station 1 blocked
8.005s	Station 2 blocked
8.004s	Station 3 blocked
8.068s	ACCBs CB_1, CB_2 and CB_3 opened

8.845s	DCSWs CB_{32} opened
8.850s	DCSWs CB_{12} opened
8.840s	DCSWs CB_{21} opened, faulty line isolated
8.870s	ACCBs CB_1, CB_2 and CB_3 re-closed, AC networks reconnected
8.890s	Station1, 2 and 3 de-blocked, DC cables recovery initialled
9.210s	CB_{32} re-closed, power flow restoration initiated
9.215s	Power delivery restored

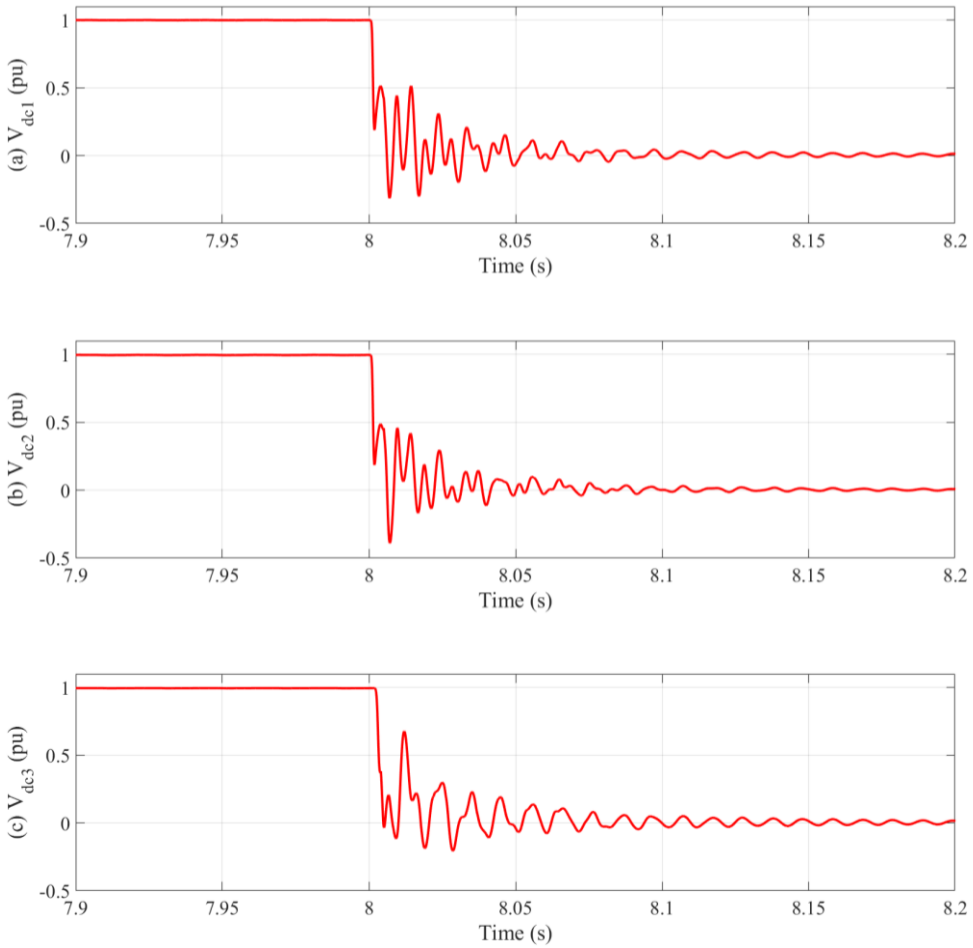


Fig. 5. 9 DC voltage at terminal of (a) Station 1, (b) Station 2 and (c) Station 3 when fault happens in Case 1.

Fig. 5.9 shows the terminal DC voltages at the three converter stations. The voltages drop rapid when the fault occurs but oscillate around zero for considerable time due to the cable impedances. Fig. 5.10 shows the upper arm currents of all three stations when the fault happens. The fault currents on arms increase fast leading to quick converter blocking in 5ms after fault initiation for Station 1 and 3, and 4ms for Station 2 (due to its closer distance to the fault comparing to Station 3 and lower converter capacity comparing to Station 1). Since the HB-MMC has no ability of fault current blocking, fault currents are fed from the AC sides as shown in Fig. 5.11. The AC fault currents lead to the ACCBs opened to interrupt the fault current injection from AC side at 8.068 s. The fault current injection from AC side is thus terminated.

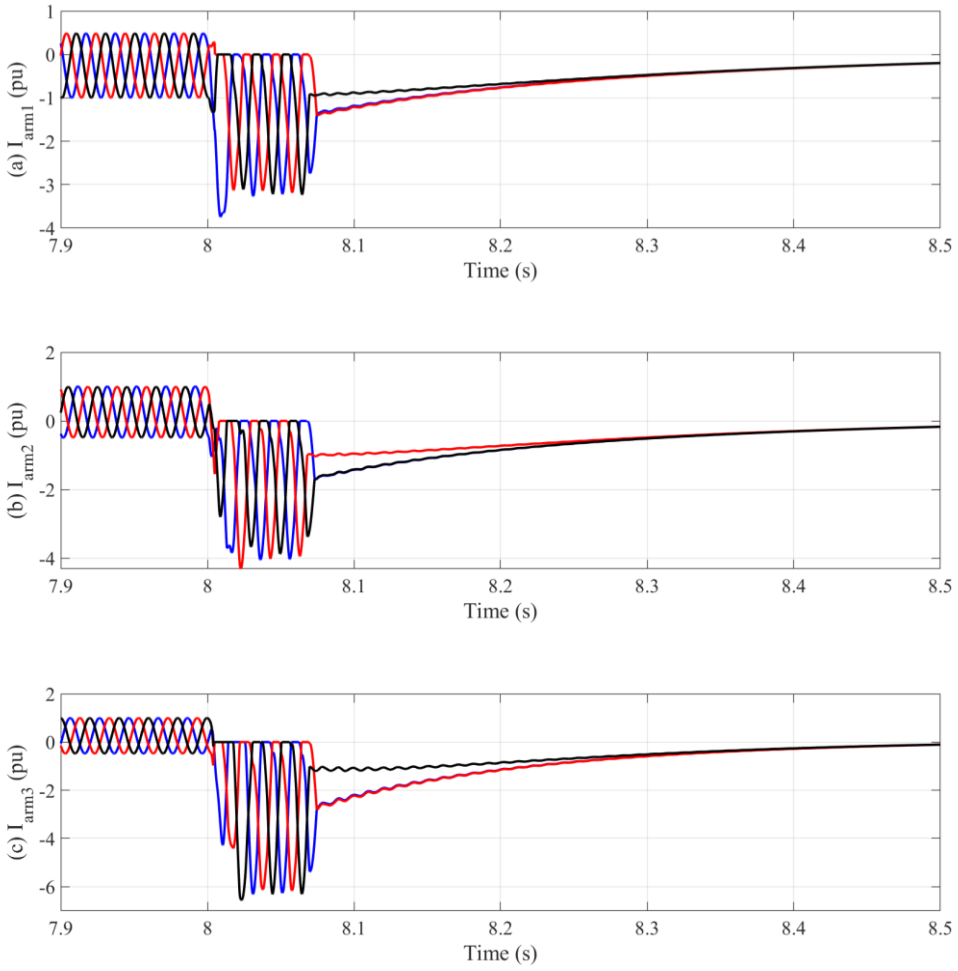


Fig. 5. 10 Upper arm currents of (a): Station 1, (b): Station 2 and (c): Station 3.

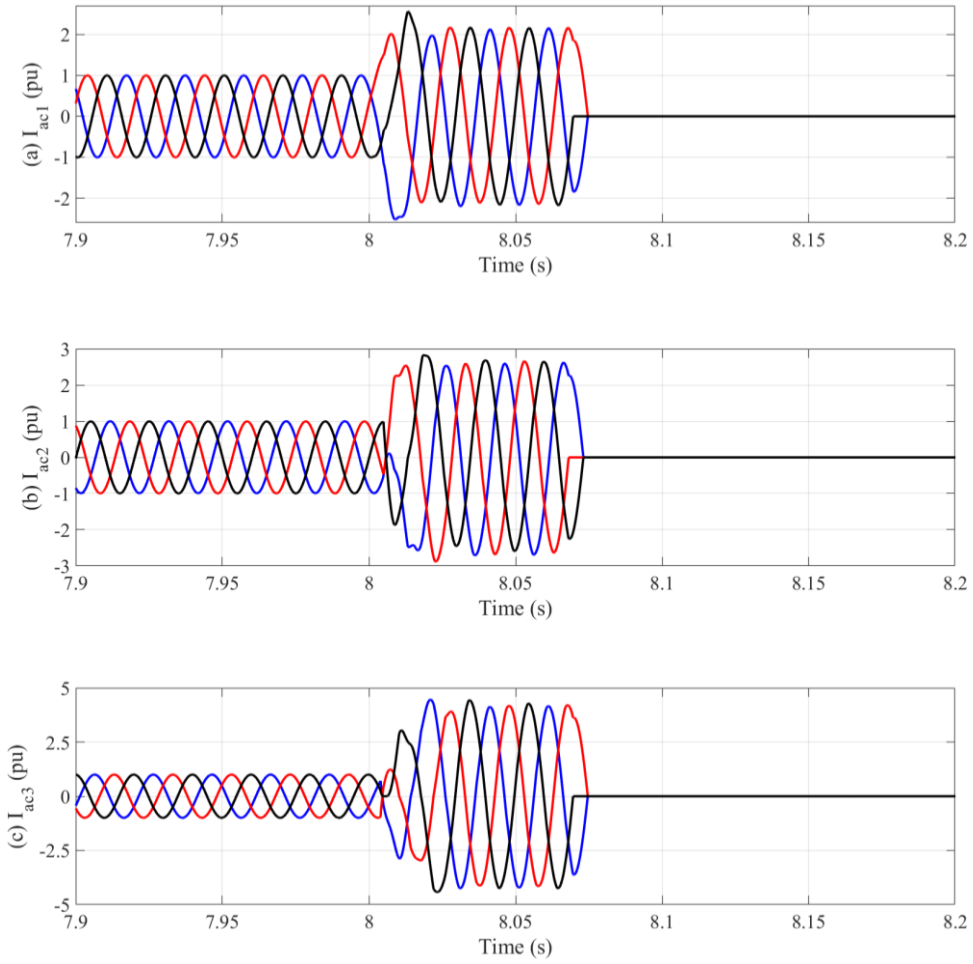
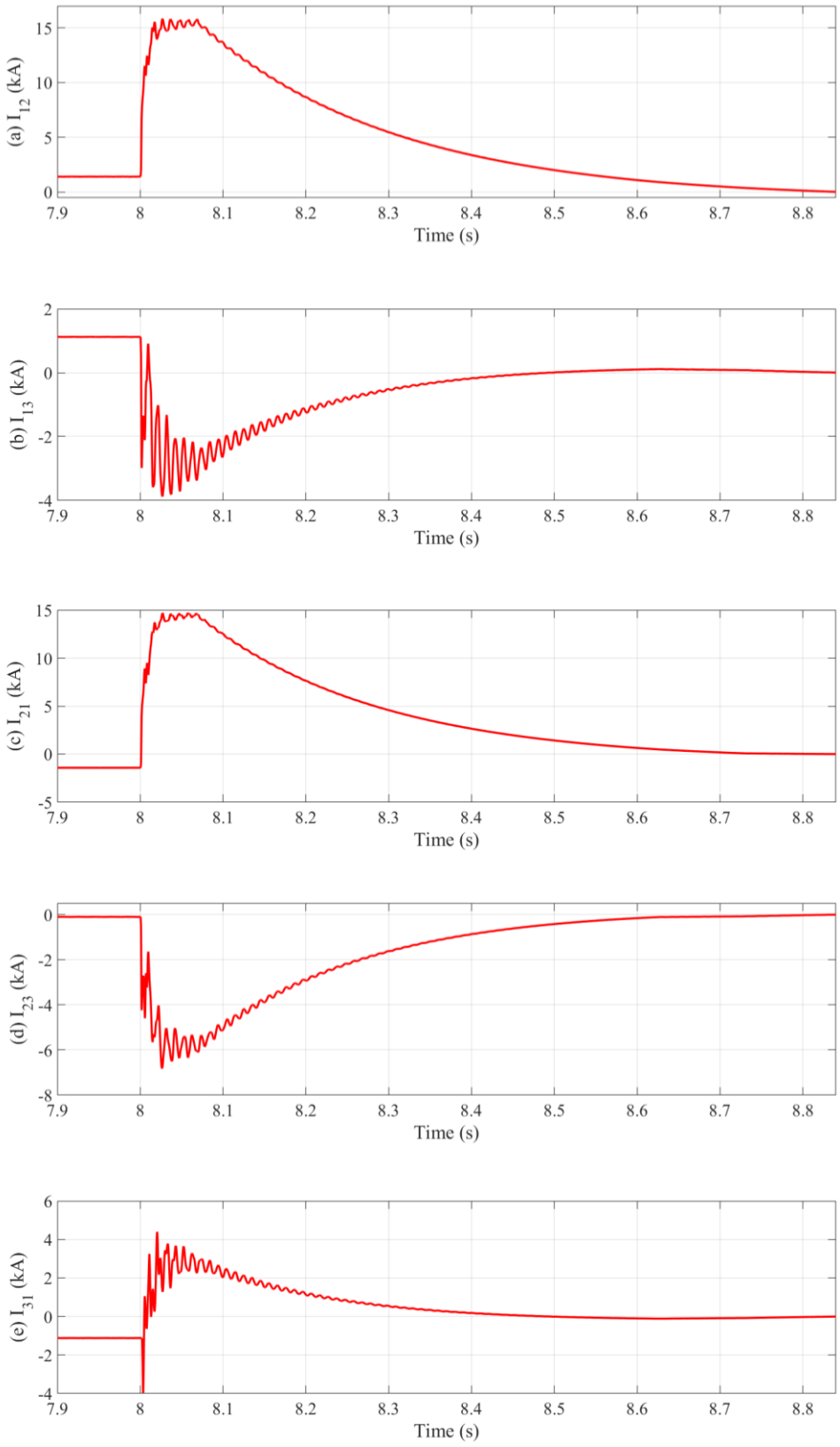


Fig. 5. 11 AC currents of (a): Station 1, (b): Station 2 and (c): Station 3 when fault happens in Case 1.


(a) I12 (kA)
15
10
5
0
7.9
8
8.1
8.2
8.3
8.4
8.5
8.6
8.7
8.8
Time (s)
(b) I13 (kA)
2
0
-2
-4
Time (s)
(c) I21 (kA)
15
10
5
0
-5
Time (s)
(d) I23 (kA)
0
-2
-4
-6
-8
Time (s)
(e) I31 (kA)
6
4
2
0
-2
-4
Time (s)

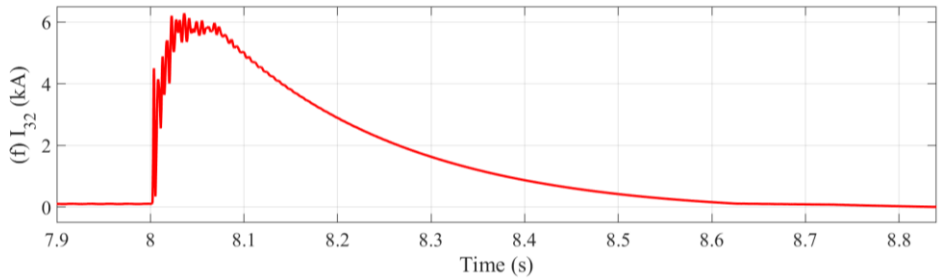


Fig. 5. 12 DC currents at DCSWs (a) 12, (b) 13, (c) 21, (d) 23, (e) 31 and (f) 32 when fault happens in Case 1.

Due to the low resistance on the DC network, the DC fault currents increase fast as shown in Fig. 5.12. It exceeds over 5 pu in 2 ms at all the DCSWs. After ACCBs are opened, the DC network starts to discharge, and DC fault currents drop. Due to the low impedance of the DC cables, the fault current drop takes considerable time while the residual energy is consuming on the DC network. As can be seen from Fig. 5.12, the DC currents at DCSWs 12, 21, 31 and 32 flow into the cables (positive current) while the DC currents flow out from the cable at DCSWs 13 and 23. And the peak fault current at DCSW 32 (6kA) is higher than that at 31 (3.9kA). Thus, based on the handshaking principles, DCSWs 12, 21 and 32 are set to open. Since the DC switches used in this study only can be opened when the DC current is around zero (in the range of ±20 A in this study), the DCSWs 12, 21 and 32 are opened at time of 8.850s, 8.840s, and 8.845s respectively.

After DCSWs 12, 21 and 32 are opened, the faulty line is isolated, and system can initiate recovery procedure. ACCBs at all the three terminals are reclosed with 20 ms communication delay at time of 8.870s to reconnect the AC networks to the DC system, and then all the converters are de-blocked at time of 8.890s allowing 20ms for system stability. All the de-blocked converters are switched to control the terminal voltages in order to recover the DC voltage on Cable 2 and 3 before DCSW 32 can be reclosed to restart power delivery along Cable 3.

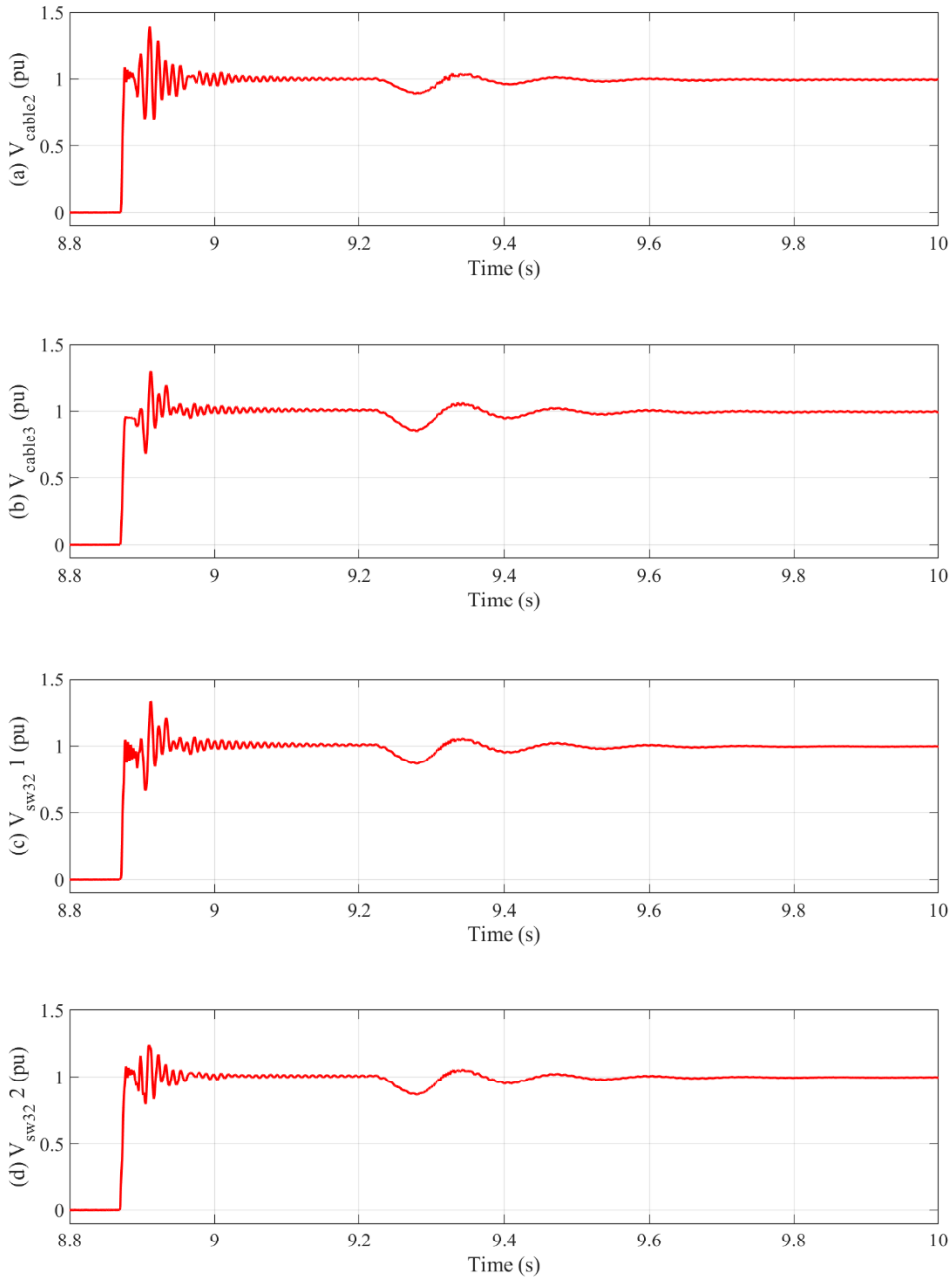


Fig. 5. 13 DC voltage during the system recovery after fault clearance: (a) Cable 2, (b) Cable 3, (c) up-side of SW_{32} and (d) down-side of SW_{32}.

During the system recovery after fault clearance, the converter at Station 2 switched to control the terminal voltage to re-build the DC voltage on Cable 3, and converters at Station 1 and 3 control the terminal DC voltage to re-build the voltage on Cable 2. From

Fig. 5.13 (a) and (b), the cable voltages start to rise after ACCBs are re-closed at 8.870s and reach its nominal value after converters are re-enabled at 8.890s. The voltage on Cable 2, shown in Fig. 5.13 (a), takes longer time to eliminate the oscillation and remain stable in the range of ±5% of its nominal value at time of 9.210s. Then the DC SW_{32} is re-closed at the same time when voltages on both sides are recovered to 1pu as shown in Fig. 5.13 (c) and (d). Thereby, power delivery path between Station 2 to Station 3 is re-established. Station 2 and 3 are switched to control the active power. The voltage drop seen on Fig 5.12 around time of 9.2s is due to the power and DC current increase at Station 2 and 3.

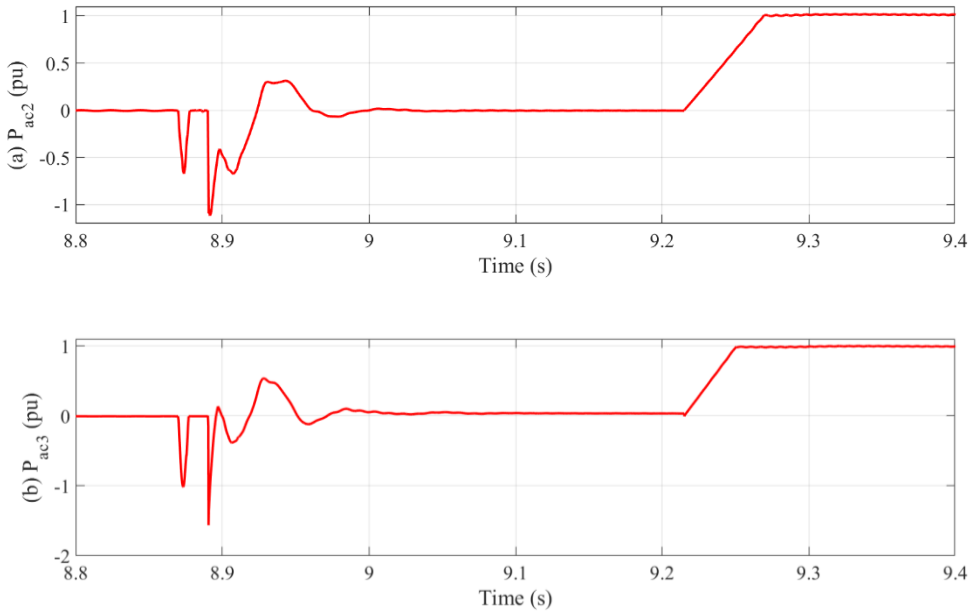
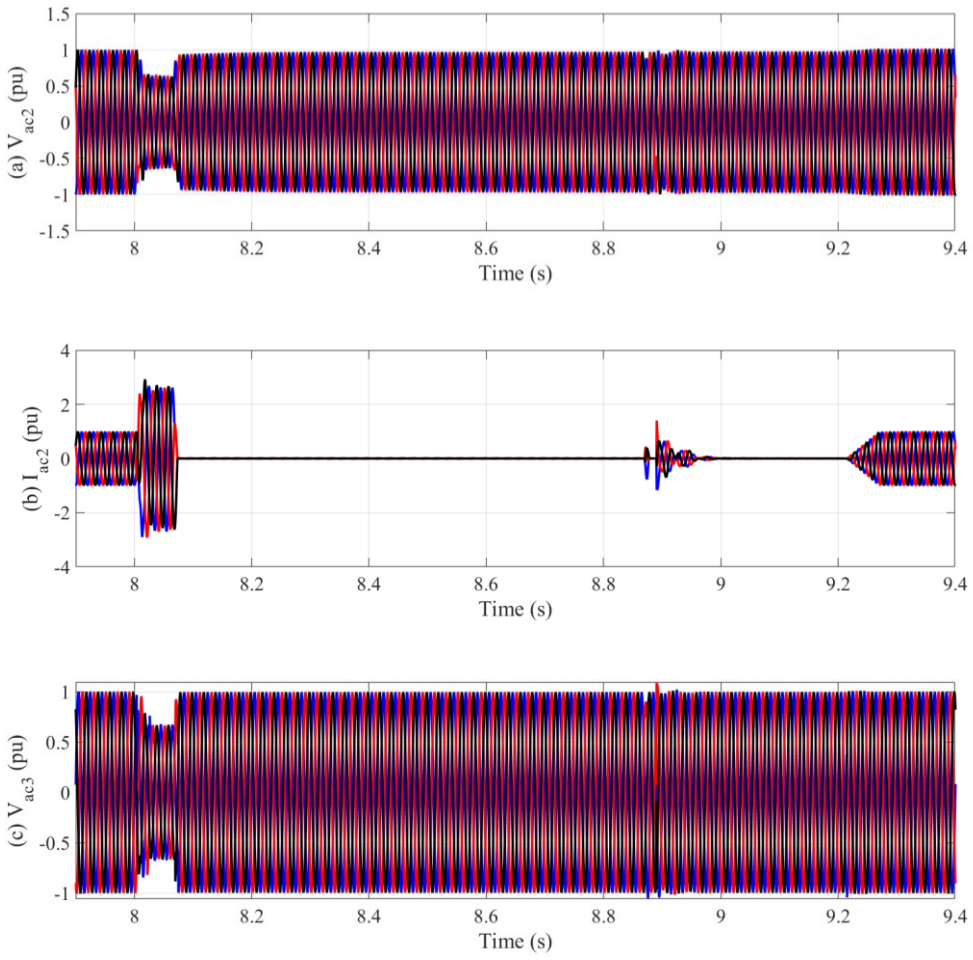


Fig. 5. 14 AC power at terminal of (a) Station 2 and (b) Station 3 during the system recovery.

Fig. 5.14 shows the active power Station 2 and 3 during system recovery. The negative AC power pulses around 8.85-8.9s are due to the charging of DC network from the AC sides. The power deliver starts to recover after converters switched to active power control at time of 9.215s and take 60 ms ramping to its nominal value and finalized the system recovery.

Fig. 5.15 shows the voltages and currents at the AC sides of Station 2 and 3. The AC voltages drop after fault initiation until the ACCB is opened. In the meantime, there is high fault currents flowing from the AC to the DC fault until 8.068s when the ACCBs are opened. After the isolation of Cable 2 and the reclosing of ACCBs, at 8.870s, the smaller incensement of AC current indicates that AC Network 2 charges the DC network through Station 2 (MMC diodes) as shown in Fig. 5.15 (b). The more significant increase at time of 8.890s indicates that energy is injected from AC Network 2 to charge cables furtherly. The similar results can be observed at Station 3 shown in Fig. 5.15 (c) and (d). From this AC charge current, it can be found that the charge is finalized around 9.2s and then the active power restore is initiated and converter station 2 and 3 are switched to control the active power at 9.215s.



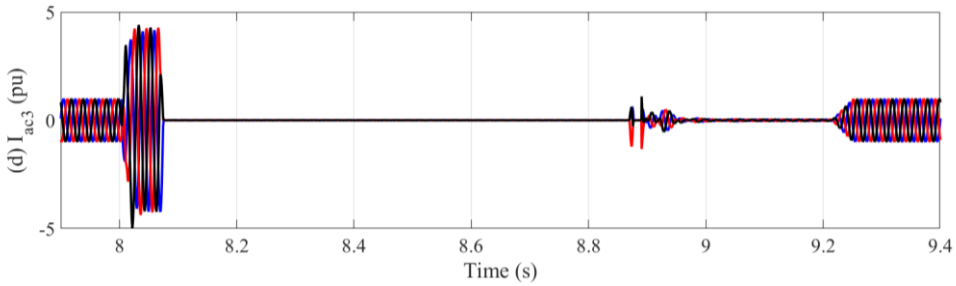


Fig. 5. 15 AC (a) voltage and (b) current at AC side of Station 2, (c) voltage and (d) current at AC side of Station 3 in Case 1.

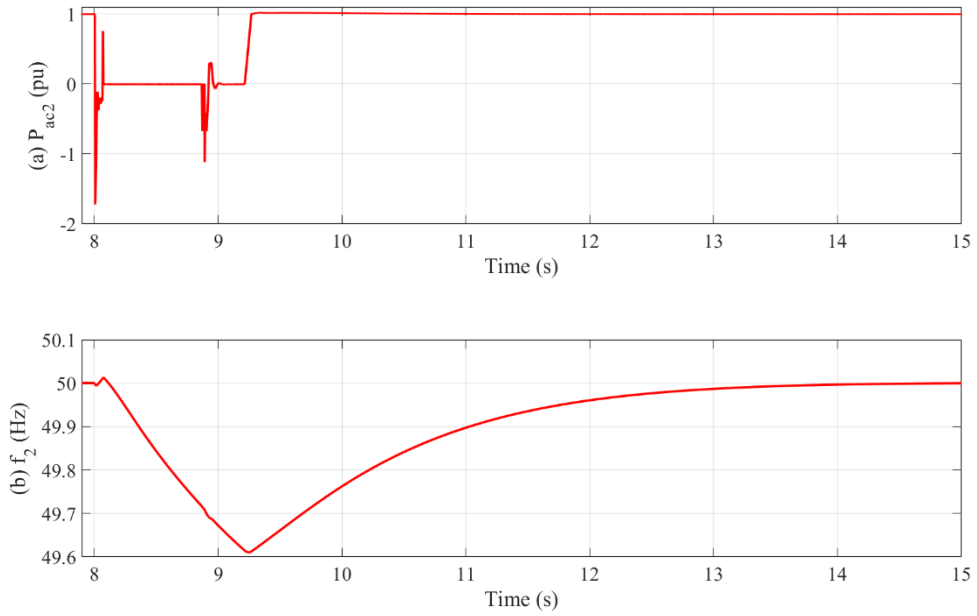


Fig. 5. 16 System response of AC Network 2 in Case 1: (a) Active power transmitted to AC Network 2 (b) frequency.

The system response of AC Network 2 during fault isolation and restoration process under protection strategies based on DCSWs is shown in Fig 5.16. As can be seen, after the DC fault, the transmitted active power from the DC to AC Network 2 is quickly drops to zero. Thus, this leads to a net loss of 1.6 GW to AC Network 2, and consequently, the frequency at AC Network 2 drops (nadir 49.6 Hz shown in Fig. 5.15 (b)). When Cable 1 is isolated and the system recovers, the negative active power pules in Fig. 5.16 (a) around time 9s relates to the re-charge of Cable 3 through Station 2. After the reclosing of CB_{32}

power transmission restarts. The power infeed to AC Network 2 is now through Cable 2 and 3 instead of Cable 1 and system frequency starts to recover to its normal value in around 5.5 seconds. The duration of loss of infeed and frequency nadir in Case 1 observed are severe due to the relatively limited synchronous generation in AC Network 2 and large HVDC converter, which is likely to trig load shedding on AC Network 2 according to the current power system operation setting. For such a system, a faster protection strategy is required to reduce the duration of loss of infeed and increase the frequency nadir.

5.4.2 Protection arrangements using DCCBs

In Case 2 and 3, DCCBs are used with operation times of 20ms and 5ms respectively to emulate the response times of typical mechanical and hybrid DCCBs, respectively. In the simulation the DCCB is modelled as shown in Fig. 5.17.

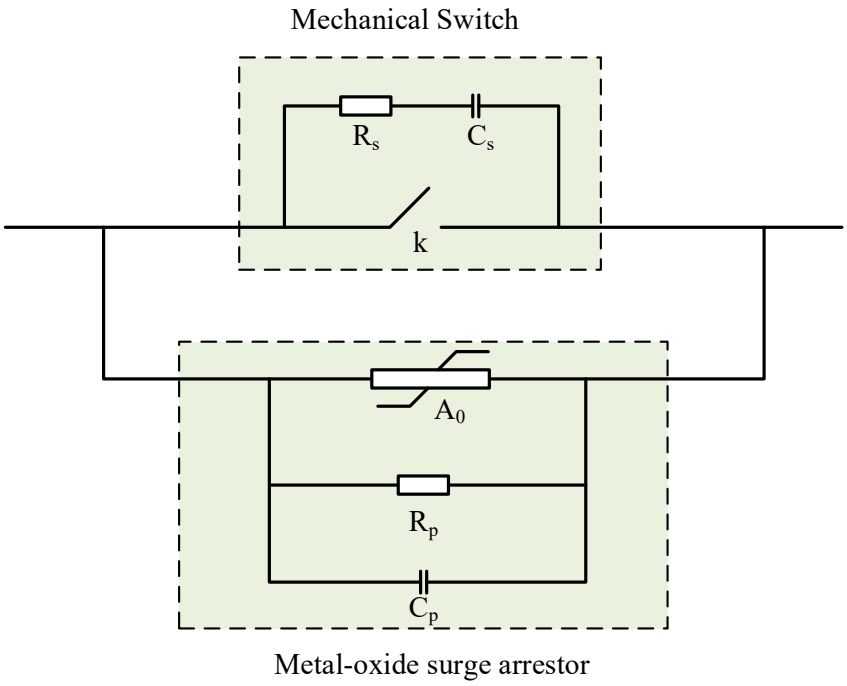


Fig. 5. 17 Diagram of DCCB used in simulation [156].

The mechanical switch is modelled as an ideal switch k connected with a RC snubber circuit in parallel. The metal-oxide surge arrestor is composed by a non-liner resistance A_0 connected with the leakage resistance R_p and parasitic capacitance C_p in parallel [156]. The model is used to simulate slow and fast DCCB in this section with 20ms and 5ms time delay implemented at switch k.

A permanent DC pole-to-pole fault is applied at the middle of Cable 1 at 8s and Station 1, 2 and 3 are blocked at 8.005s, 8.005s and 8.004s respectively, after overcurrent on converters arms ($I_{arm} \geq 2\ p.u.$) is detected. DC overcurrent ($I_{dc} \geq 2\ p.u.$) is detected at time of 8.002s at CB_{12} and CB_{21} are opened after 20ms and 5ms delays for Case 2 and 3, respectively. Similar to Case 1, CB_{32} is also opened and the alternative power transmitting path from Station 1 to Station 2 through Cables 2 and 3 is thus disrupted. Upon the isolation of Cable 1, Station 1, 2 and 3 are de-blocked at 8.037s and 8.022s for Case 2 and 3, respectively, to re-energise Cable 3. Once the DC voltage on Cable 3 is stabled in the range of 95% ~ 115% of its nominal voltage, the CB_{32} is re-closed at 8.355s in Case 2 and 8.24s in Case 3. The power transmitting from Station 1 to Station 2 can then be resumed. The time sequences of the protection actions in Case 2 and 3 are summarised in Table 5.4.

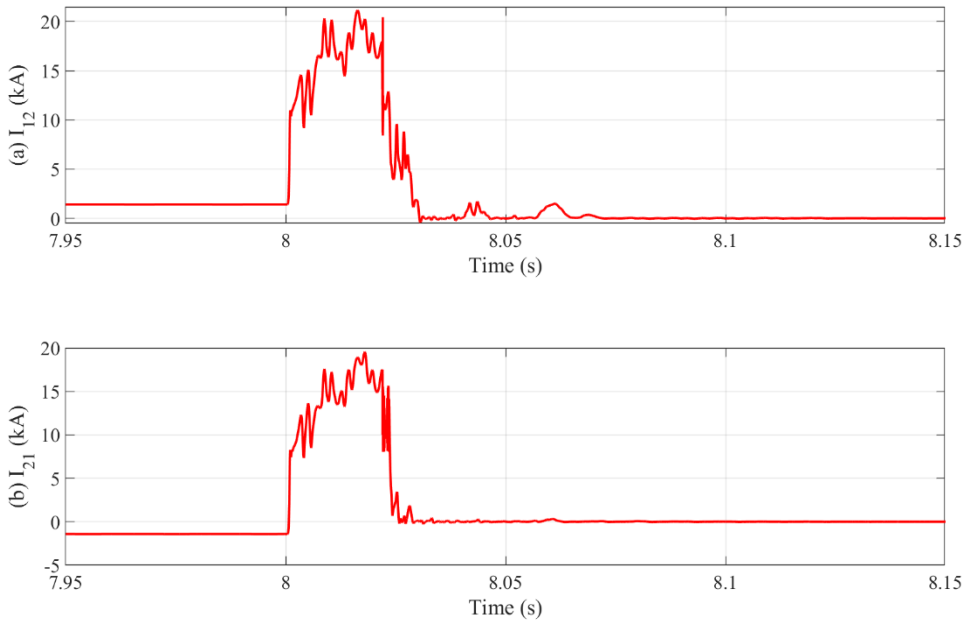
Table 5. 4 Protection sequence in Case 2 and 3

Time		**Events**
Case 2	**Case 3**	
8s	8s	A permanent DC pole-to-pole fault at Cable 1.
8.004s	8.004s	Station 3 blocked
8.005s	8.005s	Station 2 blocked
8.005s	8.005s	Station 1 blocked
8.022s	8.006s	DCCBs CB_{12}, CB_{21} are opened
8.023s	8.007s	DCCB CB_{32} is opened, fault isolation finalized

8.037s	8.022s	Station1, 2 and 3 de-blocked
8.355s	8.240s	CB_{32} re-closed, power flow restoration initiated.
8.360s	8.245s	Power delivery restore

Unlike the DCSWs employed in Case 1, DCCBs are implemented in Case 2 and 3 and they can be opened directly after the current exceeds the pre-set value with a delay. The DC overcurrent thresholds are set to 2 p.u. for every DCCBs based on their local nominal DC currents. Once the local DC current increases beyond 2 p.u., the local DCCB starts the open operation.

Fig. 5.18 shows the DC currents at $DCCB_{12}$, $DCCB_{21}$ and $DCCB_{32}$ in Case 2 ((a), (b) and (c)) and 3 ((d), (e) and (f)), respectively. It can be seen that the DC fault current increases rapid after the DC fault initiation due to the low resistance of the DC network and exceeds 2 p.u. at time of 8.001s at $DCCB_{12}$ and $DCCB_{21}$, and 8.002s at $DCCB_{32}$. Then, with a 20ms open operation time delay of the slow DCCBs implemented in Case 2, $DCCB_{12}$, $DCCB_{21}$ and $DCCB_{32}$ fully opened at time 8.021s, 8.021s and 8.022s, respectively. For Case 3 with a 5ms open delay of the fast DCCBs, $DCCB_{12}$, $DCCB_{21}$ and $DCCB_{32}$ are fully opened at time 8.006s, 8.006s and 8.007s, respectively.



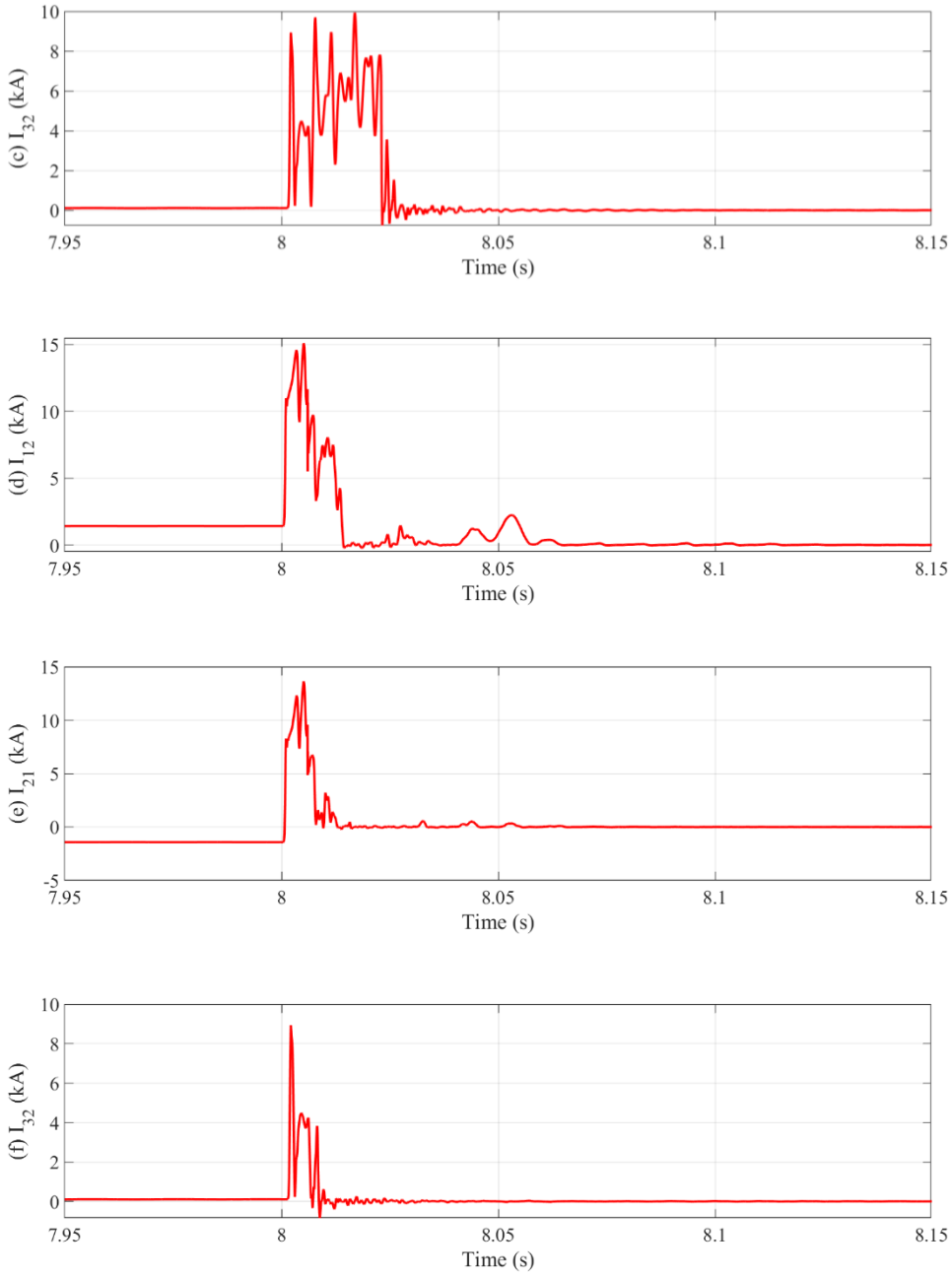


Fig. 5. 18 DC current at $DCCB_{12}$, $DCCB_{21}$ and $DCCB_{32}$ when fault occurs in Case 2 (a), (b), (c) and 3 (d), (e), (f) respectively.

After faulty line is isolated, the DC current starts to drop and the converters can be de-blocked to recover the voltage on the healthy cables. A 15ms communication delay is considered between DCCBs and converter stations after DCCBs are opened. Converters

are de-blocked at time of 8.037s and 8.022s for Case 2 and 3 respectively and are switched to control the terminal voltage.

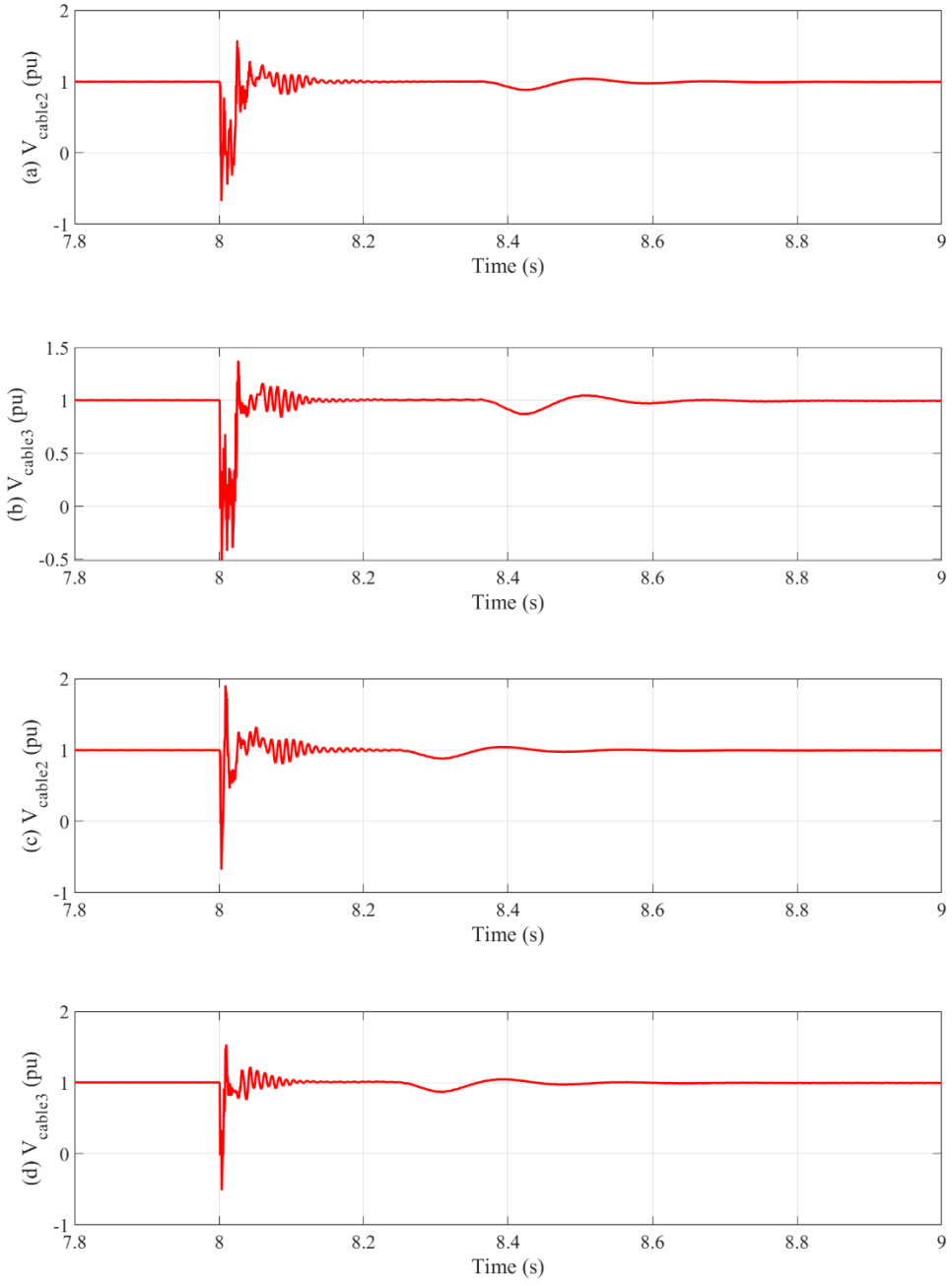


Fig. 5. 19 DC voltage of Cable (a) 2 and (b) 3 in Case 2, (c) 2 and (d) 3 in Case 3.

Fig. 5.19 shows the DC voltages on Cable 2 and 3 in Case 2 ((a) and (b)), in Case 3 ((c) and (d)). It can be seen from the figure that voltages drop to zero when fault initiated and increase back to around 0.8 p.u. after the fault is isolated (DCCBs opened). This is because the Cable 3 is still connected to AC Network 2 through the free diode rectifier circuit even while the converters are blocked. Then, after the 15ms communication delay between DCCBs and converter stations, the converters are de-blocked. The converter at Station 2 is switched from active power control mode to DC voltage control mode to help to rebuild the voltage on the Cable 3, since it is the only converter connect with Cable 3 before $DCCB_{32}$ is re-closed. From Fig. 5.19, the voltage is rebuilt to 1pu and oscillate for a short period, and then $DCCB_{32}$ can be re-closed and converter at Station 2 switches back to active power control mode at time of 8.360s and 8.250s for Case 2 and 3 respectively. Then the fault isolation and system restoration are finalized. The time between the moment when $DCCB_{32}$ detects the voltage on Cable 3 is over 800 kV (so Cables 3 is not in fault and $DCCB_{32}$ can be reclosed) and the time it recloses is set to 320ms and 220ms in the study, in Case 2 and 3, respectively. This affects the speed of recovery and maybe be shortened in practical cases for faster system recovery.

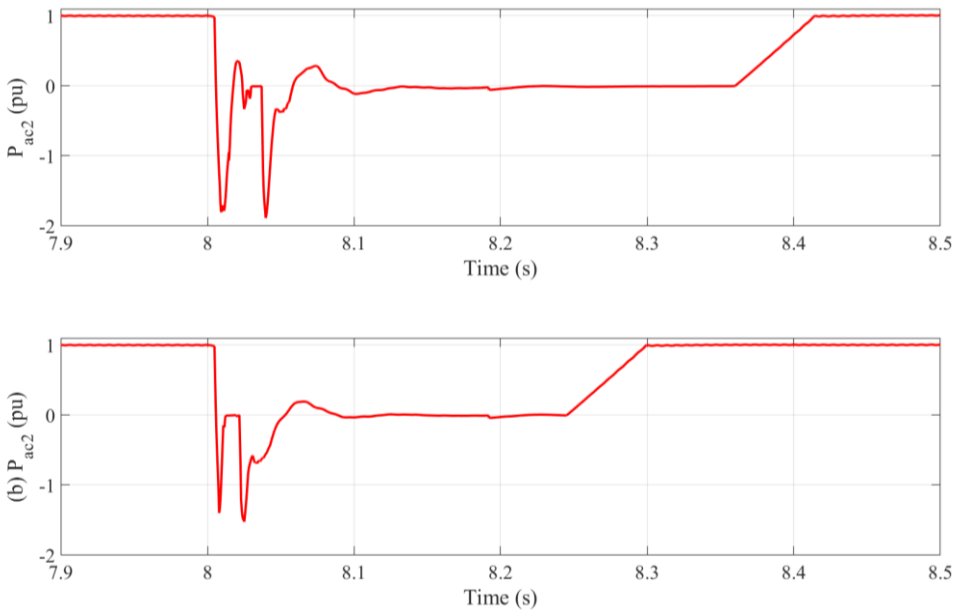


Fig. 5. 20 DC power at terminal of Station 2 in (a) Case 2 and (b) Case 3.

Fig. 5.20 (a) and (b) show the respective AC power at Station 2 in Case 2 and Case 3 during the power delivery restoration. In both cases, active power ramps to 1 pu in 60 ms. The active power in Station 3 is similar to those of Station 2 and thus not shown here. The overall active power outages for Network 2 are 360ms and 245ms in Case 2 and 3, respectively.

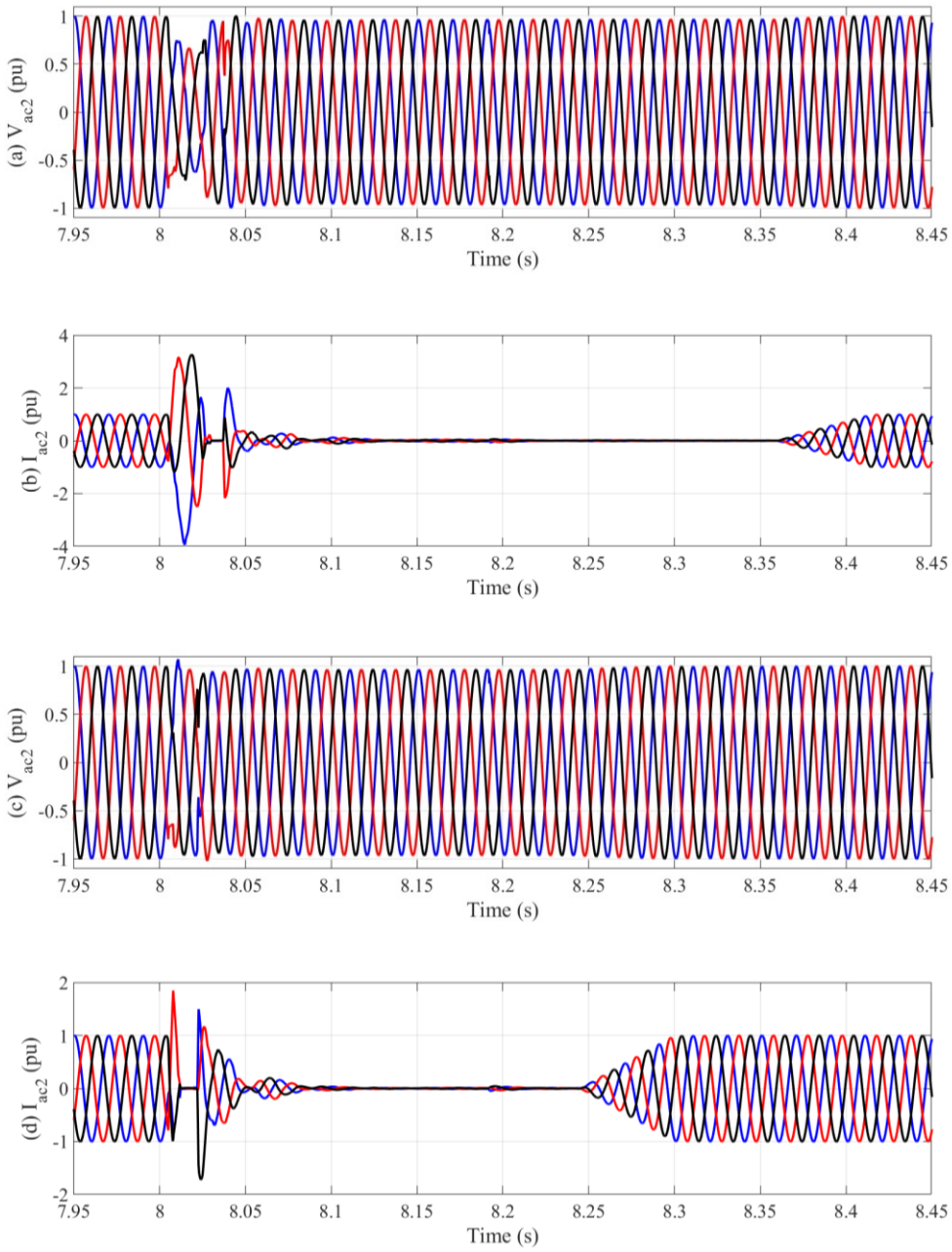


Fig. 5. 21 AC waveforms of Station 2 in Case 2: (a) voltage and (b) current, and in Case 3: (c) voltage and (d) current.

Fig. 5.21 shows the AC voltage and current at the AC side of Station 2 in Case 2 ((a) and (b)) and Case 3 ((c) and (d)). The voltage drops after fault initialled and it does not stop to drop until the DCCBs are opened (fault is isolated from the AC system) due to the connection to the DC network through the free diode branches even when the converter is blocked. After fault is isolated, voltage increase back to near nominal value and stay stable. For the AC current, it can be seen that huge fault current is keeping delivered to the DC network until time of 8.022s when DC fault is fully isolated in Case 2 and 8.007s in Case 3. The incenses of AC current from 8.037s and 8.022s shown in Fig. 5.21 (b) and (d) for Case 2 and 3 respectively, indicate that AC Network 2 charges Cable 3. Taking Case 2 as an example, the voltage rebuilt time for $DCCB_{32}$ is set to 320ms, though it can be seen from the current shown in Fig. 5.21 (b) that the charge (AC current injection to DC network) is largely finished around time of 8.15s instead of 8.36s. This also indicates the voltage rebuilt time could be set much shorter, which has been discussed before.

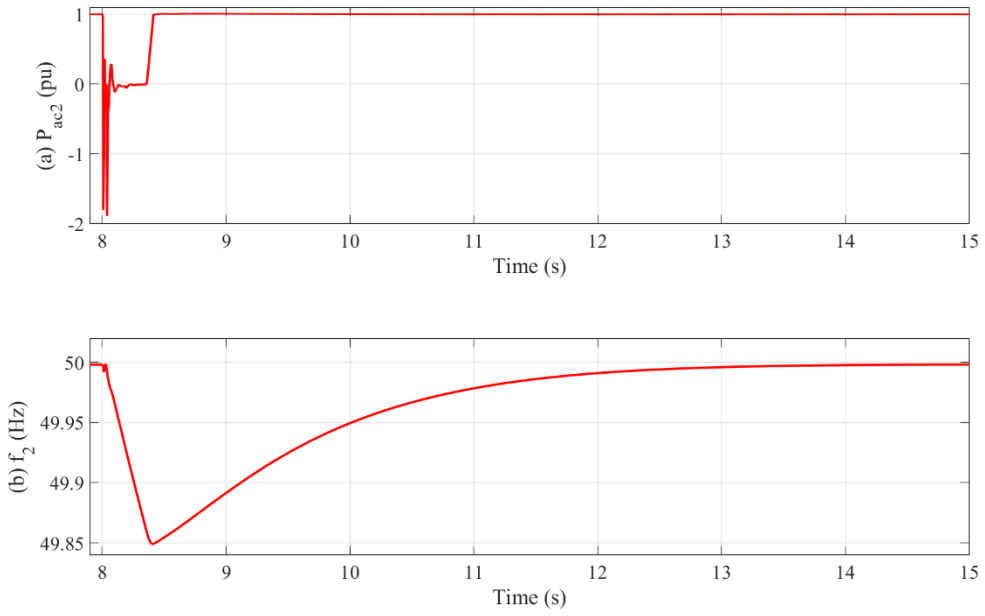


Fig. 5. 22 System response of AC Network 2 in Case 2: (a) Active power transmitted to AC Network 2 (b) frequency.

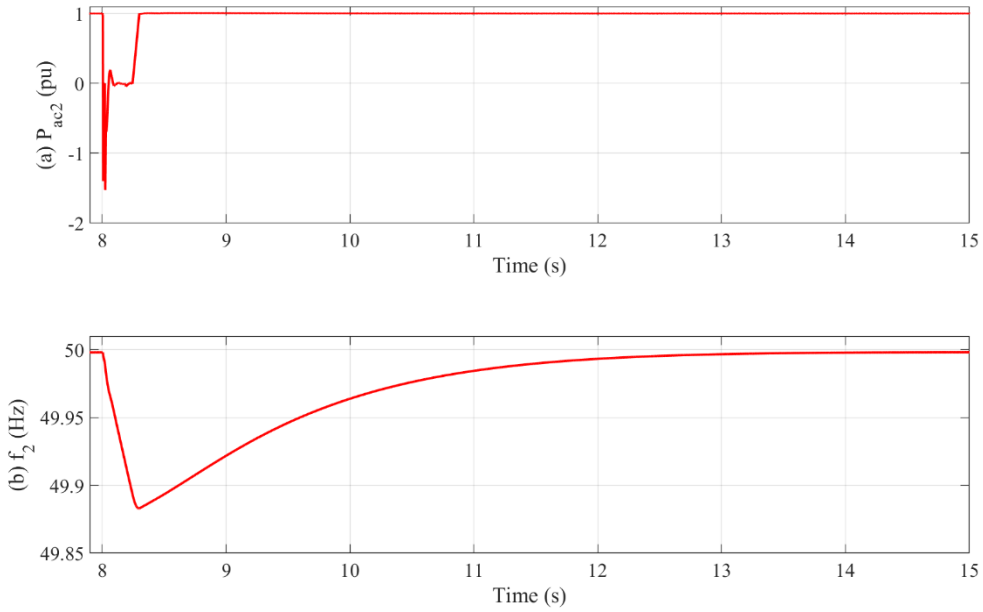


Fig. 5. 23 System response of AC Network 2 in Case 3: (a) Active power transmitted to AC Network 2 (b) frequency.

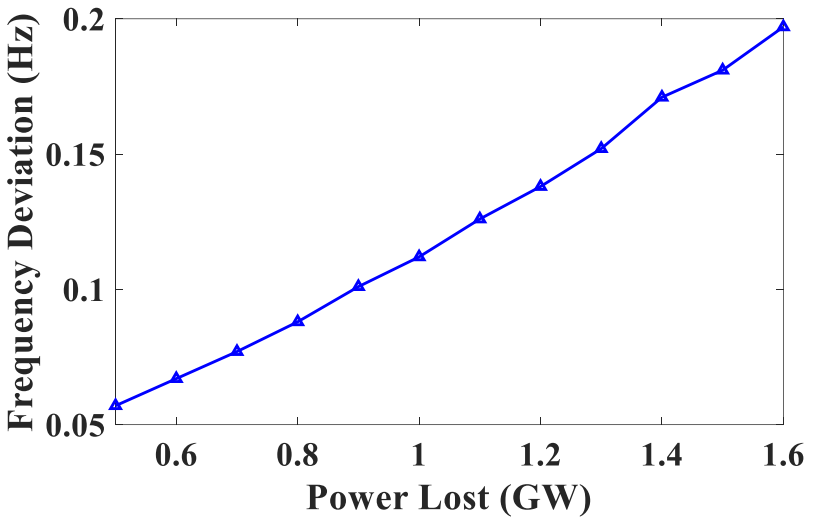
Fig 5.22 and Fig 5.23 compare the frequencies and active power infeed of AC Network 2 in Case 2 and 3, respectively. In both cases, the frequencies start to drop as the result of the DC faults interrupting DC transmission from DC to AC Network 2. As shown in Fig. 5.22 (b), the AC Network 2 frequencies drop to around 49.85 Hz in Case 2, and 49.87 Hz in Case 3 (shown in Fig. 5.23 (b)), respectively. The oscillation of active power at 8.037s and 8.022s shown in Fig. 5.22 (a) and Fig. 5.23 (a) are due to the re-charging of Cable 3 after Station 2 is enabled. The faster acting DCCBs equipped in Case 3 isolates the faulty Cable 1 sooner than that of the slow DCCBs in Case 2. Consequently, power transmission can be recovered earlier in Case 3 than in 2, power loss in case 2 is from 8.022s to 8.360s whereas from 8.007s to 8.250s for Case 3 As a result, the nadir of frequency drop in Case 3 (49.87Hz) is higher than that in Case 2 (49.85Hz). Compare to Case 1 in Section 5.4.1 where the AC frequency is dropped to 49.6Hz, the system frequency performances in Case 2 and 3 are much improved and the frequency nadir during DC fault events is increased by the faster fault isolation and system restoration.

However, from the results, it is evident that the difference in DCCB opening time does not lead to significant difference in frequency nadir. This is largely due to the fact that once DCCBs are opened (takes 23ms and 7ms in Case 2 and 3, respectively), the recovery process also takes considerable time before power restoration. Another issue is that the handshaking protection method is used here which leads to the opening of CB_{32} which has to be re-closed before power transmission can be restored. Many protection methods can lead to fast fault detection and full selective fault location and thus, only CB_{12} and CB_{21} need to be opened. However, no significant difference is observed on frequency nadir as the process of CB_{32} reclose takes 20ms less only. Therefore, from the results in this chapter, the restoration process of the protection strategies influences more on the frequency of connected AC system than the fault isolation speed.

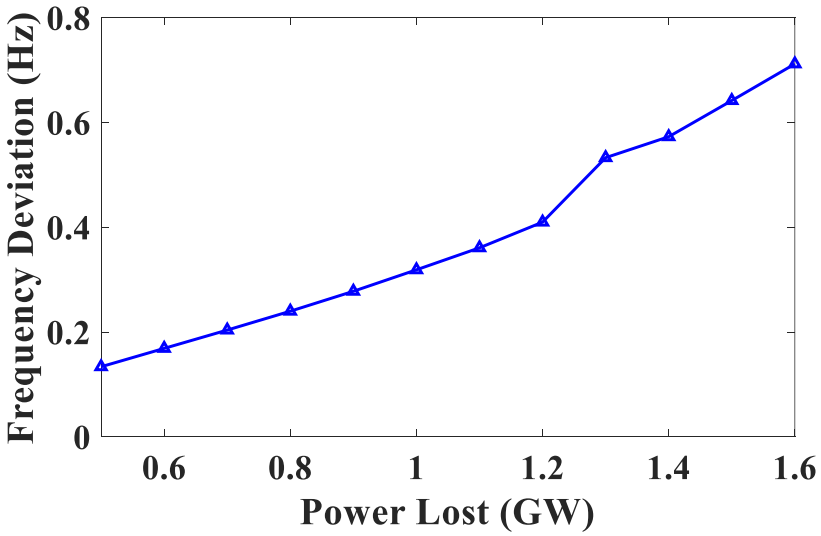
5.4.3 Impact of the amount of loss-of-infeed and power loss duration on frequency response

Further studies have been carried out to investigate impact of the amount of loss-of-infeed on frequency response during DC fault protection process. This is achieved by setting different initial power infeed from the DC network to AC Network 2 prior to the DC fault. Fig 5.24 (a) and (b) show the variation of frequency deviation for different amounts of infeed loss of AC Network 2 during DC fault protection process based on fast DCCBs (with 5ms operation time) and DCSWs respectively.

As can be seen in Fig. 5.24, the frequency deviation of AC Network 2 increases with the increased loss-of-infeed. On the other hand, it can be observed that for the same frequency deviation, the allowed power loss in Fig. 5.24 (a) with fast DCCB is much larger than that in Fig. 5.24 (b) with slow DCSW, e.g. for 0.2 Hz deviation, the allowed power losses are around 1.6 GW in (a) and 0.7 GW in (b), respectively. This indicates that higher power loss can be allowed with faster DC fault isolation and system restoration for the same minimum frequency. Thus, the current maximum 'loss-of-infeed', which is determined based on the amount of permanent power loss, may not be suitable for future AC-DC hybrid power grid. Instead, both the amount of loss-of-infeed and outage duration have to be considered.



(a)



(b)

Fig. 5. 24 Frequency response to different amounts of power shortage during DC fault protection processes with alternative protection arrangements: (a) fast DCCBs; (b) DCSWs.

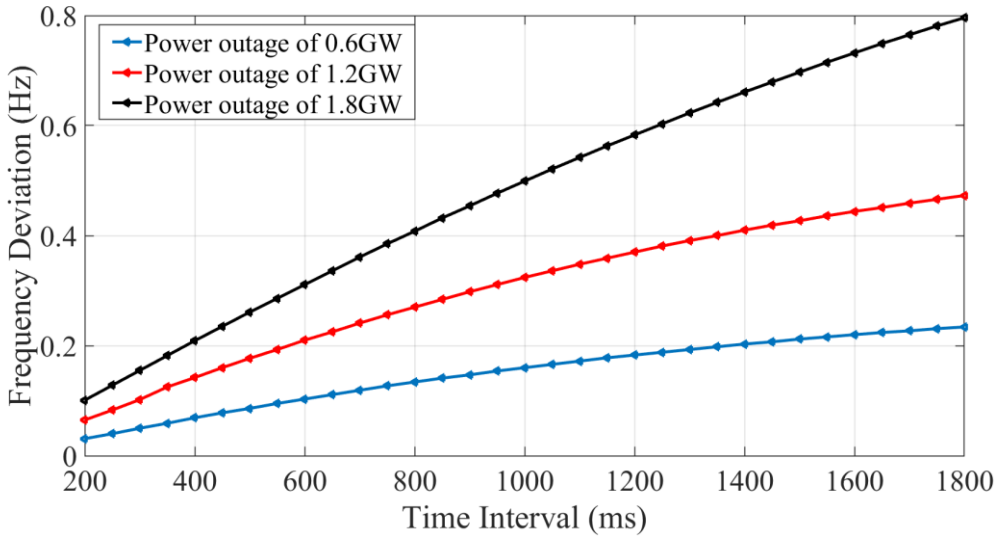


Fig. 5. 25 Frequency response for different power loss duration and loss-of-infeed.

Impact of power loss duration on frequency response is carried out and the simulation results are shown in Fig. 5.25 when different loss-of-infeed are also considered. Under the same power loss, frequency deviation increases with higher power outage duration. For example, at power loss of 1.8 GW, the frequency deviation increases from 0.1Hz to 0.4Hz and to 0.8Hz when the outage duration increases from 200ms to 800ms and to 1.8s. Also as previously described, for the same outage duration, increased power loss amount increases frequency deviation. Therefore, when determining the maximum loss-of-infeed for a particular network, the potential outage duration must be considered. From the study, it can be seen that a larger loss-of-infeed could be allowed if the period of power loss is relatively short.

5.5 Conclusion

This chapter investigates the impacts of different DC fault protection arrangements on frequency response of connected AC systems. A three-terminal meshed MTDC network has been modelled and used for case studies. The frequency responses of

connected AC network to different DC fault protection arrangements based on DCSWs, slow DCCBs and fast DCCBs have been carried out in case studies. It has shown that the frequency performance and frequency nadir are improved with faster DC fault isolation and system restoration. Both the amount of power loss and outage duration affect system frequency response and thus the two need to be considered simultaneously when determining the maximum "loss-of-infeed" for future AC-DC hybrid power grids. A large loss-of-infeed could be allowed if the period of power loss is relatively short when fast DC fault protection is implemented.

Chapter 6 Energy Based Virtual Damping Control of FB-MMCs for Meshed HVDC Grids

Full-bridge submodule based modular multilevel converters (FB-MMCs) have attracted wide attention due to their DC fault blocking capability. However, blocking FB-MMCs only prevents AC current from feeding to the DC faults through the converter whilst the fault currents in the DC network may still circulate for a considerable time especially for large meshed DC networks. To address this issue, an energy based virtual damping control is proposed, where the DC terminal current of the FB-MMC is regulated to follow the DC voltage in the event of a DC fault. The FB-MMC is thus controlled as a virtual damping resistor to actively absorb the residual energy in the DC network and quickly suppress the potential circulating DC fault currents. This enables fast fault isolation using DC switches and thereby fast fault recovery after fault isolation. The fault isolation time is significantly reduced from around 120 ms with the FB-MMC simply being blocked and 50ms with the conventional FB-MMC fault control method [140, 141] to around 15 ms. The validity of the proposed control is verified in a three-terminal meshed DC network.

6.1 System Layout

The investigated three-terminal hybrid DC network is illustrated in Fig. 6.1, where the HB-MMC is adopted for Station 1 while the FB-MMC is used for Station 2 and 3. The mixed MMC configuration arrangement is adopted in order to include varieties of DC protection design using DCCBs and DCSs, though the proposed fault current control method can be used for DC networks with FB-MMC only. As shown in Fig. 6.1, DCCBs are equipped at the DC terminals of the HB-MMC station for DC fault isolation, shown as DCCB 12 and 13. Considering the fault current controllability of the FB-MMC and to reduce the capital cost of protection equipment, DCSs are connected at the DC terminals of the FB-MMCs, shown as DCS 21, 23, 31, and 32. Under normal operation, Station 1

controls the DC voltage of the DC network while Station 2 and 3 operate on active power control mode. All the three stations are modelled as average-value MMC models [153] with 320 HB SMs (Station 1 as have been described in Chapter 3) and 320 FB SMs (Stations 2 and 3, to be described below) submodules per arm, respectively. The DCCB is represented as hybrid DCCB with fault current breaking time of 5 ms [78], as have been described in Chapter 4. The DCS is modelled as SF6 puffer circuit disconnector and can only open when its current is less than 100 A [140, 141, 157]. Each DC transmission cable is represented by 10 π-section transmission line models. The detailed parameters of the considered hybrid DC system are listed in Table 6.1.

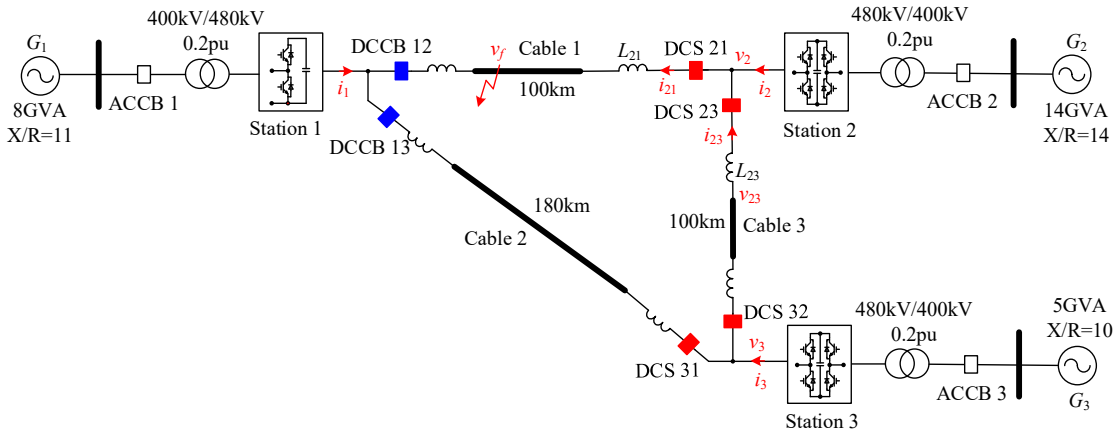


Fig. 6. 1 Meshed hybrid DC network.

Fig. 6.2 shows the implemented average FB-MMC model (taking upper arm of phase a as example) [158]. Similar to the HB-MMC model introduced in Chapter 5 that the arm capacitor C_{arm} is charged by the current generated by a controlled current source based on the arm current i_{pa} and the modulation function m. the output arm voltage is generated by a controlled voltage source based on the arm capacitor voltage v_c and the modulation function m. When the FB-MMC is in control mode, IGBT 1 and 4 on, 2 and 3 off, so the arm voltage equals u_{pa}. During normal operation, 0<m<1 and the arm voltage is positive, whereas under fault control mode -1<m<0 and the arm voltage is negative.

The absence of anti-parallel diodes at $IGBT_2$ and $IGBT_3$ is to simulate the behaviour of the FB-MMC during converter blocking mode when the IGBTs in all the SMs are turned off. During the converter blocking state, IGBT 1 and 4 are off, whilst IGBT 2 and 3 turned on with m=1, so the capacitor voltages in all the FB SMs are inserted to the circuit [6].

Table 6. 1 Converter and Cable Parameters

Parameters	**Nominal Value**
Rated DC voltage	±400 kV
Power rating of Station 1, 2 & 3	2600 MW, 1300 MW, 1300 MW
Number of SM per arm / SM voltage	320 / 2.5 kV
SM capacitance for Station 1, 2 & 3	3.8 mF, 1.9mF &1.9mF
Arm inductance	0.05 pu
DC terminal inductance of Station 1	100 mH
DC terminal inductance of Station 2 & 3	30 mH
R, L and C per unit length of cable	3 mΩ/km, 0.5 mH/km, 0.2 μF/km
Number of pi section	10
Nominal p.u. AC voltage and power	400 kV / 2200 MW

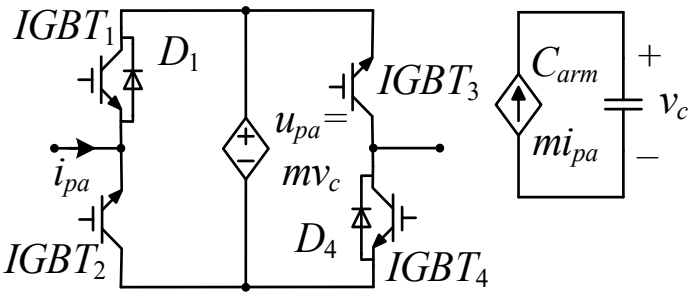


Fig. 6. 2 Average FB-MMC model implementation.

6.2 Fault Characteristics of the Hybrid DC Network

The fault characteristics of the investigated hybrid DC network are presented in this section, considering the situations when the FB-MMCs are blocked and actively controlled, respectively.

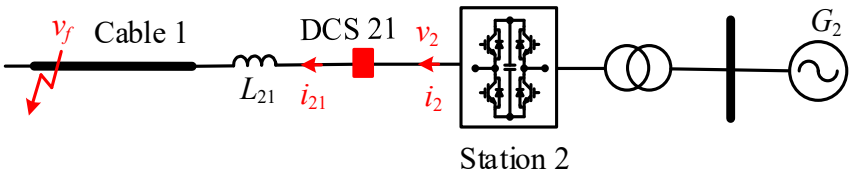
6.2.1 Fault Characteristics When FB-MMCs Are Blocked

FB-MMCs have DC fault blocking capability and thus, DCSs may be used at their DC terminals for the protection of the DC network to reduce the cost of protection equipment. To isolate the fault, the currents flowing through DCSs need to be quickly suppressed to around zero, before opening the DCSs. For radial DC network where only one DC cable is connected at the terminal of the station as illustrated in Fig. 6.3 (a), the DC fault currents i_2 and i_{21} can be quickly suppressed to zero following the blocking of the FB-MMC and thus, DCS 21 can be quickly opened at around zero current. However, for the considered meshed DC network, the fault currents exhibit different behaviours, as will be discussed in this subsection.

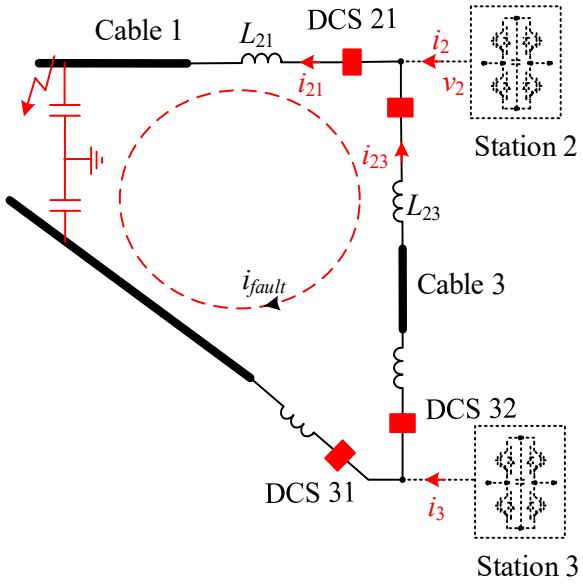
Considering a permanent pole-to-pole DC fault at the middle of Cable 1 as illustrated in Fig. 6.1 and Fig. 6.3 (b), all the three stations are immediately blocked once the DC fault is detected by the respective station based on local measurements [159]. DCCB 12 and 13 are then opened to protect the HB-MMC based Station 1 from overcurrent.

In addition to DCCB 12, DCS 21 also needs to open when its current is reduced to around zero to completely isolate the faulty Cable 1. Following the blocking of the FB-MMCs (Station 2 and 3), their DC terminal currents, i.e. i_2 and i_3 are quickly suppressed to zero, as shown in Fig. 6.4 (a) for i_2 during the DC fault at Cable 1 at 0.7 s. However, even though DCCB 12 and 13 have opened, and i_2 and i_3 have dropped to zero, significant currents still flow through the DCSs and cables, as the distributed capacitors of the DC cables provide circulating paths for the fault current, as illustrated in Fig. 6.3(b). Taking the current i_{21} flowing through DCS 21 as an example, it decays slowly as shown in Fig. 6.4 (b), due to the resonance and low resistance of the fault current circulating path in Fig.

6.3 (b). As seen, it takes over 130 ms for the currents i_{21} to decrease to the range of ±100 A, leading to significant delay for the fault isolation (by opening DCS 21) and the restoration of the healthy part of the system.



(a) In a radial DC network.



(b) Fault current circulating path through distributed capacitors of DC cables in a meshed DC network.

Fig. 6. 3 DC fault protection based on FB-MMCs and DCSs.

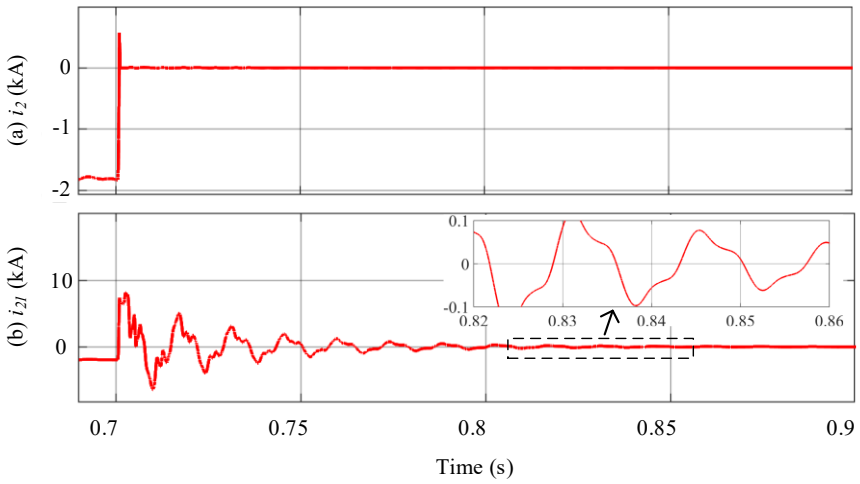


Fig. 6. 4 DC fault currents during the pole-to-pole DC fault applied at Cable 1 in the meshed DC network at t=0.7 s: (a) DC current of Station 2 and (b) DC current flowing through DCS 21.

6.2.2 FB-MMC Active Fault Current Control

Instead of blocking the FB-MMCs during DC faults, active control of the fault current can be adopted [141], where the FB-MMC directly controls the fault current flowing through the DCS by regulating the DC voltage output of the FB-MMC, as shown in Fig. 6.5. As shown, V_{dcref} is the DC offset voltage reference for each of the arms and during normal operation, it equals half of the DC voltage. When the fault is detected, all the converters are switched to control their terminal DC current to zero, until the faulty line is located. Then the converters directly connected to the faulty line is switched to control the DC current flowing through the DSC on the faulty line. As shown in Fig. 6.5, V_{dcref} is switched to the fault control scheme where the DCS current i_{21} is regulated by a PI controller to adjust the DC voltage v_2 of the FB-MMC output. As shown in Fig. 6.3(a), by regulating the voltage difference between v_2 and the fault voltage v_f which is around zero during a low resistance fault, the current i_{21} flowing through the DCS can be quickly suppressed to zero when only one DC cable is connected with the FB-MMC.

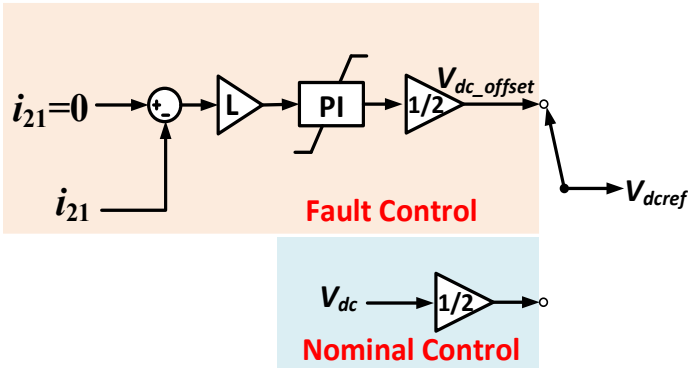


Fig. 6. 5 Control diagram of DC line fault current control.

When multiple cables are connected at the DC terminal of the FB-MMC, the interaction between the adjacent cables pose a challenge for such control approach. Again, considered Station 2 of the meshed DC network in Fig. 6.1 and Fig. 6.3(b) as an example, where both Cable 12 and 23 are connected at the DC terminal of Station 2, the Station 2 FB-MMC tries to suppress the DCS current i_{21} to zero, after Cable 1 is detected as the faulty line, by regulating the output voltage v_2. However, the regulation of v_2 also affects the current flowing through Cable 3

From the simulated waveforms shown in Fig. 6.6, when the current i_{21} flows to the fault as shown in Fig. 6.6 (a), the FB-MMC at Station 2 switches to fault control and tries to generate a negative voltage v_2 to suppress i_{21} to 0. However, the voltage v_2 shown in Fig. 6.6 (d) also affects the current i_{23} at Cable 3 as shown in Fig. 6.6 (c), which could potentially flow through DCS 21 and feed the fault, leading to significant oscillations of the DCS current i_{21}.

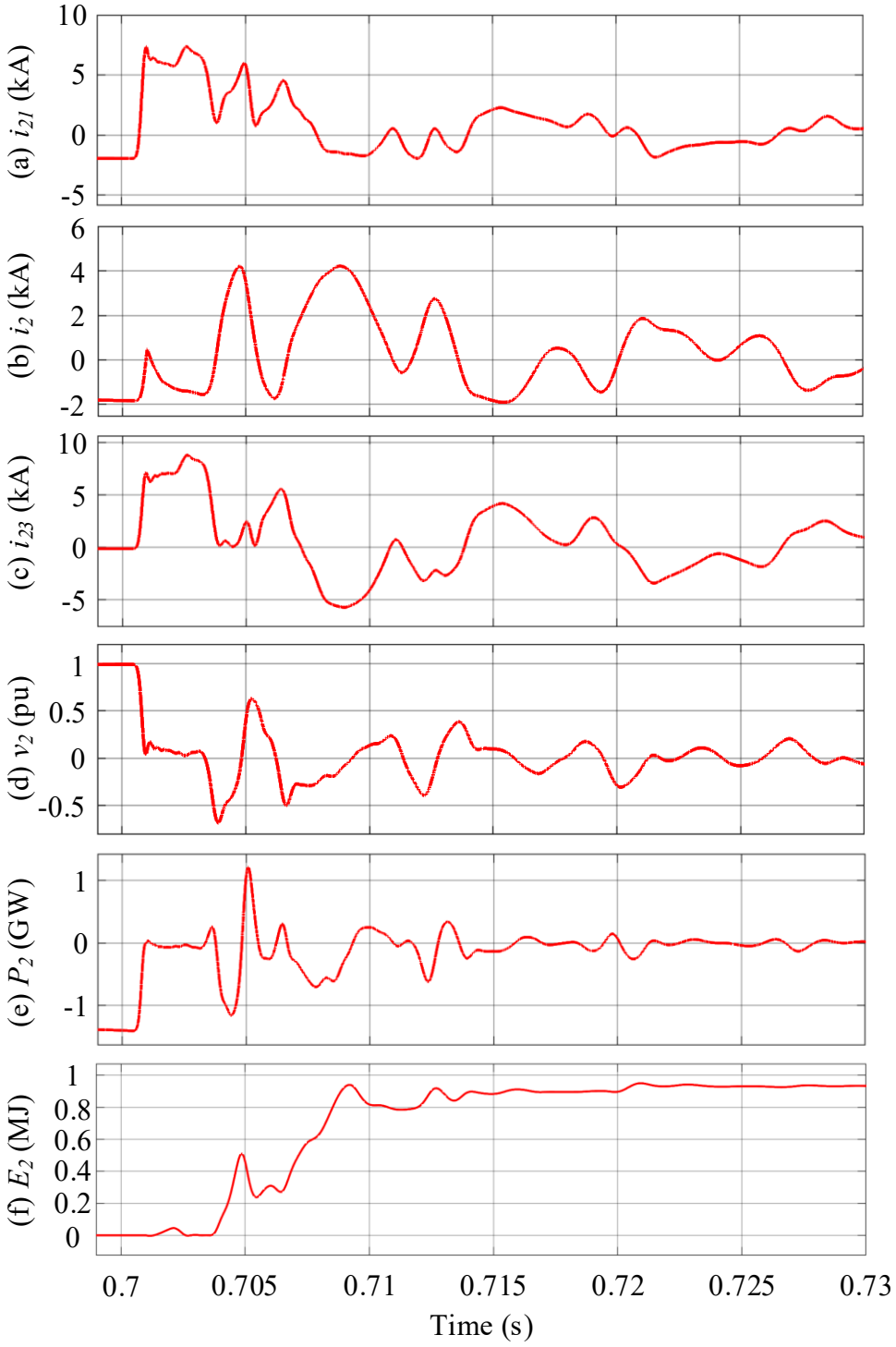


Fig. 6. 6 Waveforms of the hybrid DC network with conventional control, where the DC fault is applied at t=0.7 s and fault current control switched in at t=0.701 s: (a) DC line current i_{21}, (b) DC terminal current i_2, (c) DC line current i_{23}, (d) DC voltage v_2, (e) active power P_2 of Station 2 and (f) energy absorbed by Station 2.

The issues related to the above described control interaction can be further explained from the perspective of energy. The DC active power P_2 of Station 2 is

$$P_2 = v_2 i_2 \tag{6.1}$$

which oscillates as shown in Fig. 6.6 (e). When P_2 is negative, Station 2 absorbs energy from the DC network, contributing to the de-energisation of the DC network and suppression of the DCS current i_{21}. However, when P_2 is positive, Station 2 actually injects energy from the AC gird to the DC side, leading to the increase of the overall fault currents/energy that circulate in the DC grid. This is also demonstrated by the absorbed energy E_2 of Station 2 from the DC network, as shown in Fig. 6.6 (f), which is obtained by integrating the active power P_2 from 0.7 s onwards. At the initial stage after the fault occurrence, E_2 increases and Station 2 absorbs energy from the DC grid but during some periods, it decreases, indicating that Station 2 injects energy back to the DC grid. Consequently, this delays the suppression of the DCS current i_{21}, as shown in Fig. 6.6 (a).

6.3 Proposed Energy Based Virtual Damping Control

6.3.1 Control Strategy

The DC switches can only be opened at around zero current when the DC network is totally de-energized. Thus, from the perspective of energy, the fault isolation speed is heavily determined by the speed of de-energization of the DC network by the FB-MMCs. In the aforementioned conventional control, the FB-MMCs try to directly control the current at the faulty cables to zero. However, due to the interactions of the cables in a mashed DC grid, the performance is poor and the converters potentially inject energy to the DC network, leading to slow de-energisation and decrease of the fault currents flowing through the DCSs. To tackle this issue, an energy based virtual damping control is thus proposed in this section.

The basic concept of the propose control is that the FB-MMCs are actively controlled during DC faults to absorb energy from the DC network as quickly as possible

without trying to directly control the cable current. This avoids injecting energy into the DC network as previously observed and thus indirectly suppresses the DCS current to zero quickly. As shown in Fig. 6.7, the proposed control regulates the DC terminal current of the FB-MMC i_2 based on the measured DC terminal voltage v_2 instead of trying to directly control the DCS current i_{21} to zero as used in the other methods. This effectively operates the FB-MMC as a virtual DC damping resistor R_v as the DC current reference is given as:

$$i_{2ref} = \frac{1}{R_v} v_2 \tag{6.2}$$

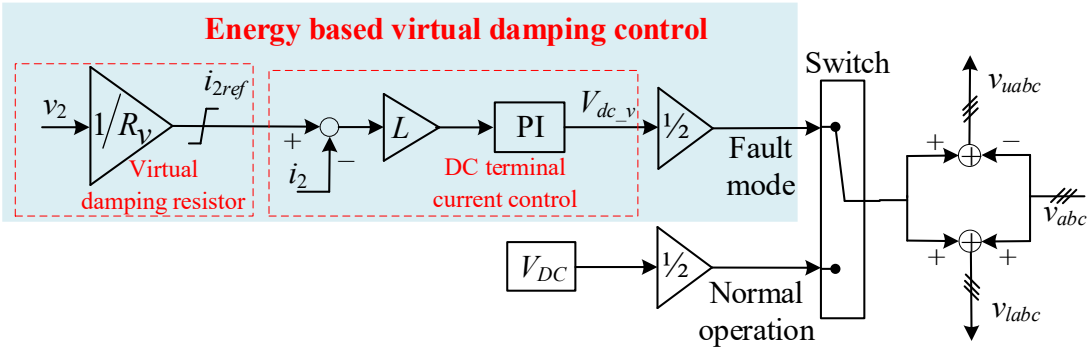


Fig. 6. 7 Proposed energy based virtual damping control.

The FB-MMC is then only required to control its DC terminal current to follow the reference value which removes the issue related to the control of cable current due to interactions between adjacent cables as identified in the previous section. Even though the DC terminal voltage v_2 oscillates around zero during faults, the FB-MMC is controlled to absorb DC current from the meshed DC network when v_2 is positive, and inject current to the DC grid when v_2 is negative. Thus, the FB-MMC always absorbs energy from the DC network so as to accelerate the de-energization, leading to fast decrease of the DC

fault currents circulating in the meshed DC network. Assuming i_2=i_{2ref} and from (6.2), the absorbed energy of the FB-MMC is

$$P_2 = v_2 i_2 = \frac{1}{R_v} {v_2}^2 \tag{6.3}$$

Once the DC grid is de-energized by the FB-MMC, the DCS can be opened at zero current to isolate the fault.

As shown in Fig. 6.7, the DC offset of the arm voltages v_{uabc} and v_{labc} is set at $0.5V_{dc}$ during normal operation. In the event of a DC fault, the proposed energy based virtual damping control is activated after fault detection to regulate the DC terminal current i_2 by manipulating the DC offset in the arm voltage, as illustrated in Fig. 6.7, where V_{dc_v} is the output of the proposed virtual damping controller.

In addition, the conventional method [140] tries to control the DCS current directly which requires accurate fault location to decide which DCS current should be suppressed to zero. This introduces significant delay for the initiation of the fault current control and further leads to slower fault isolation. Also, it is likely that only the FB-MMC connected directly to the faulty cable contributes to the suppression of the fault current flowing through the DCS. In contrast, the proposed virtual damping control does not rely on the information of fault location and can be immediately initiated once the DC fault is detected by the FB-MMC based on local measurements. In addition, all the FB-MMCs can adopt the proposed strategy to automatically absorb residual energy from the DC network with the proposed control, yielding faster de-energization and fault isolation.

The FB-MMC with the proposed control is equivalent to a virtual resistor R_v connected to a voltage source v_2 and its absorbed power is depicted by (6.3). Thus, with lower virtual resistance R_v, the FB-MMC could absorb the residual power of the DC grid quicker, yielding faster fault current suppression. However, the maximum DC current of the converter is limited and the response of the FB-MMC's current control also needs to be considered when selecting the R_v value.

In addition to FB-MMCs, the proposed control is also applicable for other alternatives with negative voltage generating capability, e.g. hybrid MMCs [160], cross-connected SM based MMCs [6, 161], etc.

6.4 Simulation Results

To assess the effectiveness of the proposed virtual damping control, a permanent pole-to-pole DC short circuit fault is applied at the middle of Cable 1 at t=0.7 s, as illustrated in Fig. 6.1. The faulty DC line is isolated using a combination of DCCB 12 and DCS 21 with the assistance of FB-MMC Stations 2 and 3 as described in Section 6.3. It can be known from the control diagram shown in Fig. 6.7, with smaller value of R_v, larger terminal current reference can be generated thus absorb more energy wither higher power, delivering better control results. However, with the terminal current limited at 1.4 pu, the R_v smaller than 50 Ω cannot make the control performance better anymore. Therefore, the virtual damping resistance R_v is set at 50 Ω for both Station 2 and 3.

After isolation of the faulty Cable 1, the system resumes power transmission through Cable 2 and 3. The system performances during fault clearance and recovery are addressed in the following subsections A and B, respectively.

6.4.1 System Performance with the Proposed Virtual Damping Control

(A) Both FB-MMC adopt the proposed control

In the first test, the proposed damping control is applied to both Station 2 and 3, and the simulated waveforms are shown in Fig. 6.8 and 6.9 for Station 2 and 3, respectively. The waveforms for Station 1 and the current flowing through the fault cable i_{21} are shown in Fig. 6.10. After the DC fault occurrence at t=0.7 s, the DC grid voltages collapse within 1 and 2 ms, as shown in Fig. 6.8 (a) and Fig. 6.9 (a) for Station 2 and 3, respectively. Station 1 detects the fault at t=0.702s and is blocked immediately. Fault currents flow through the antiparallel diodes of Station 1 to the fault, as indicated by the high arm current in Fig. 6.10 (b). DCCB 12 and 13 at the DC terminal of Station 1 open

at t=0.704 s to break the fault current from Station 1, as displayed in Fig. 6.10 (a) and (b) for the DC current and arm currents of Station 1.

The FB-MMC based Station 2 and 3 detect the fault at t=0.701 s and 0.702 s respectively and switch to the proposed virtual damping control mode. The DC terminal currents i_2 and i_3 are controlled to follow the DC terminal voltages v_2 and v_3, as can be seen in Fig. 6.8 (a) (b) and Fig. 6.9 (a) (b), where i_2 and i_3 exhibit similar shape (the DC current is limited to 1.4 pu of the respective rated converter current as previously described) to those of v_2 and v_3 in the virtual damping control mode. Thus, the power P_2 and P_3 of Station 2 and 3 are always negative and the FB-MMC stations only absorb energy from DC grid as displayed in Fig. 6.8 (c) and Fig. 6.9 (c). The issue of potentially re-injecting power from AC gird to the DC network shown in Fig. 6.6 is effectively avoided. This is also demonstrated by the energies absorbed by the two FB-MMC stations as shown Fig. 6.8 (d) and Fig. 6.9 (d), which keep increasing until the system is completely de-energized.

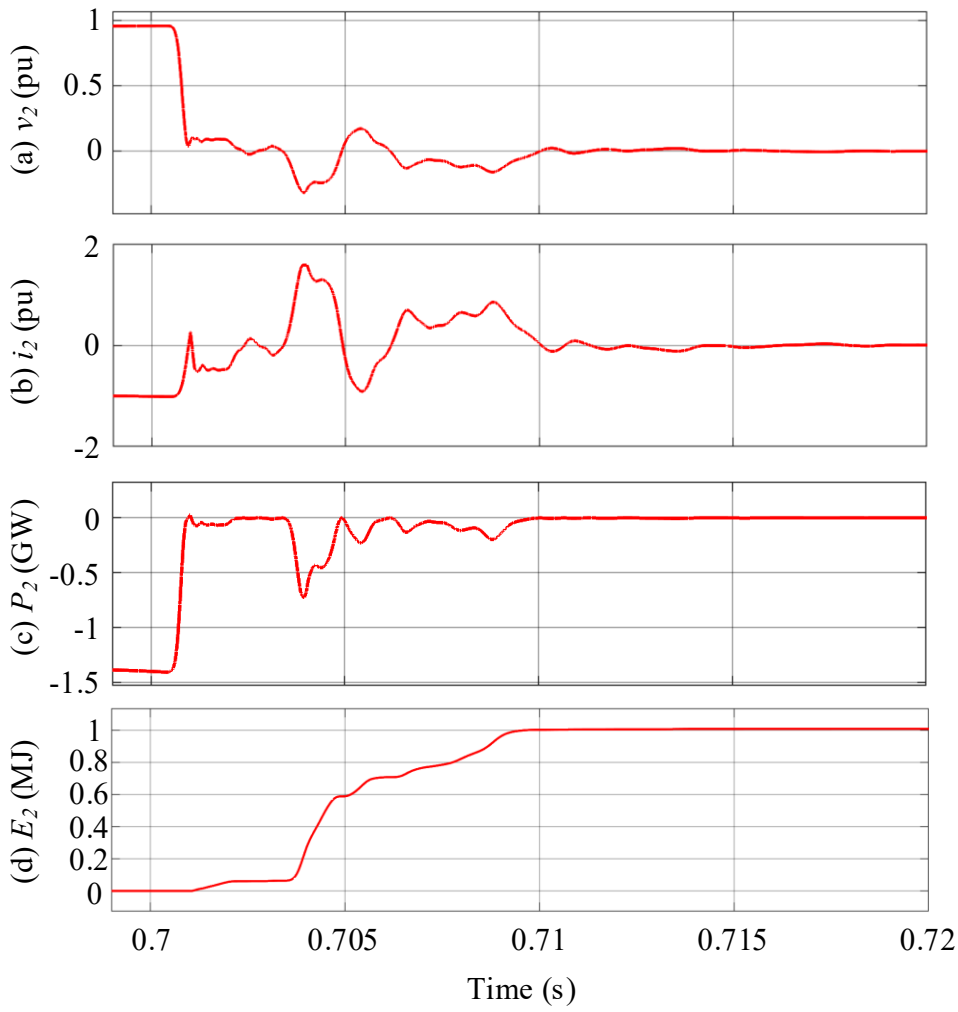


Fig. 6. 8 Simulated waveforms of Station 2 during fault clearance: (a) DC voltage, (b) DC current, (c) DC power and (d) energy absorbed by FB-MMC.

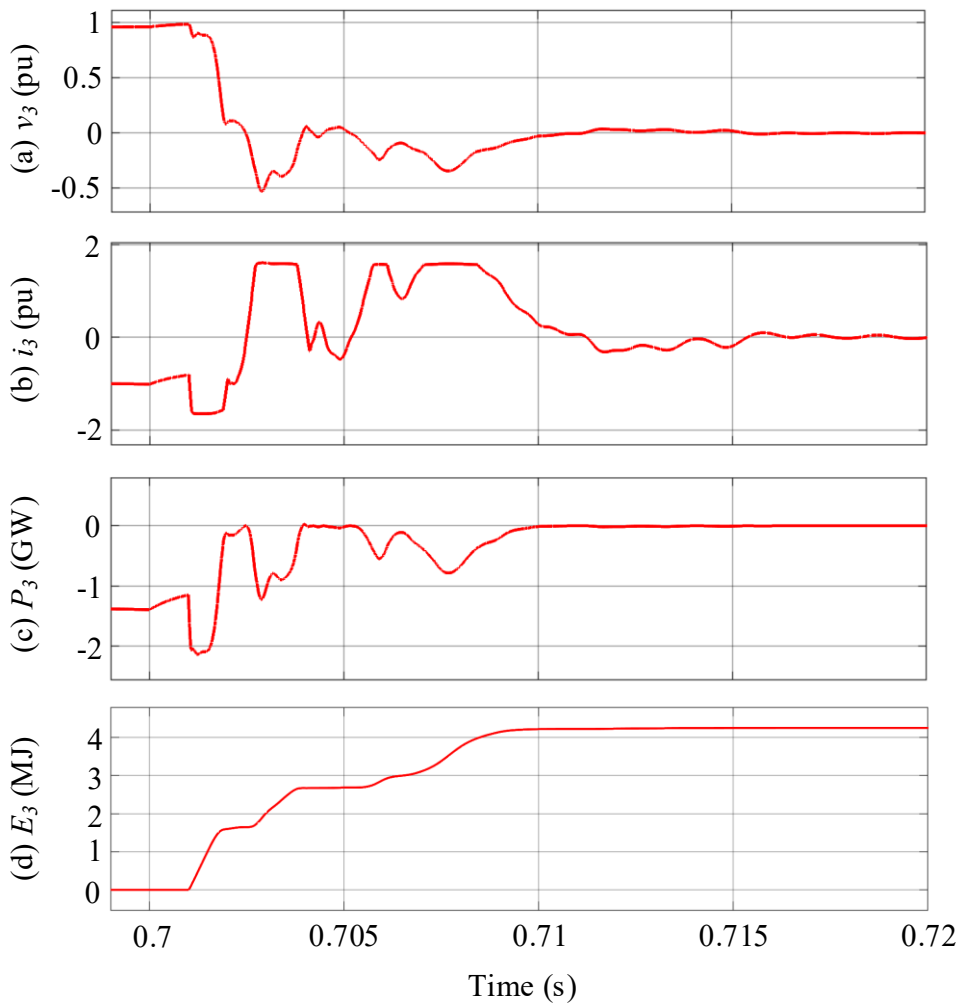


Fig. 6. 9 Simulated waveforms of Station 3 during fault clearance: (a) DC voltage, (b) DC current, (c) DC power and (d) energy absorbed by FB-MMC.

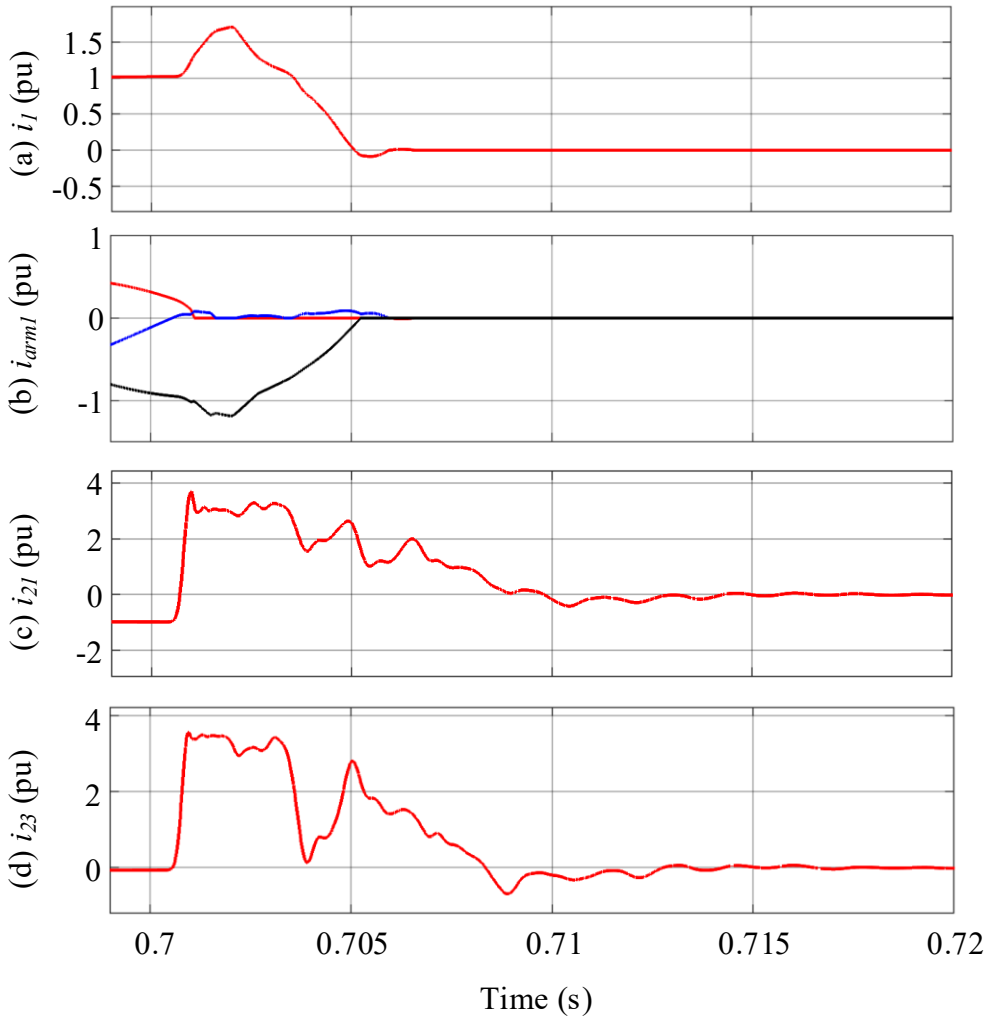


Fig. 6. 10 Waveforms of Station 1 and DCSs during fault clearance: (a) DC current of Station 1, (b) arm currents of Station 1, (c) DC current of DCS 21 and (d) DC current of DCS 23.

The circulating DC fault currents that flow through the DCSs, DC cables and their distributed capacitors are quickly suppressed to zero, as shown in Fig. 6.10 (c) and (d). Then DCS 21 is opened at around zero currents at t=0.715 s for fault isolation after the fault is located at Cable 1.

As Station 3 is adjacent to the longest Cable 2 and is further away from the DC fault at Cable 1, its DC voltage during the fault remains higher than that of Station2, as shown

in Fig. 6.8 (a) and Fig. 6.9 (a). Consequently, it can absorb more power and energy than those of Station 2, as seen in Fig. 6.8 (c)(d) and Fig. 6.9 (c)(d). The DC currents of both Station 2 and 3 are limited within 1.4 pu assuming a short term 40% overcurrent capability, as observed in Fig. 6.8 (b) and Fig. 6.9 (b).

(B) Compared to the conventional method

Fig. 6.11 compares the DC current i_{21} flowing through DCS 21 with the conventional direct cable current control and the proposed virtual damping control. In the conventional control, both Station 2 and 3 are switched to control their terminal DC current to zero until the faulty Cable 1 is located. Then Station 2 is switched to control the current at DCS 21 to zero while station 3 still controls its terminal DC current providing no contribution to the DC network de-energization as respect of energy. The time when i_{21} is controlled into the range of ±100 A is significantly reduced from over 50 ms to less than 15 ms by the proposed control, as shown in Fig. 6.11. Thus, DCS 21 can be opened earlier after fault initiation, leading to fast fault isolation.

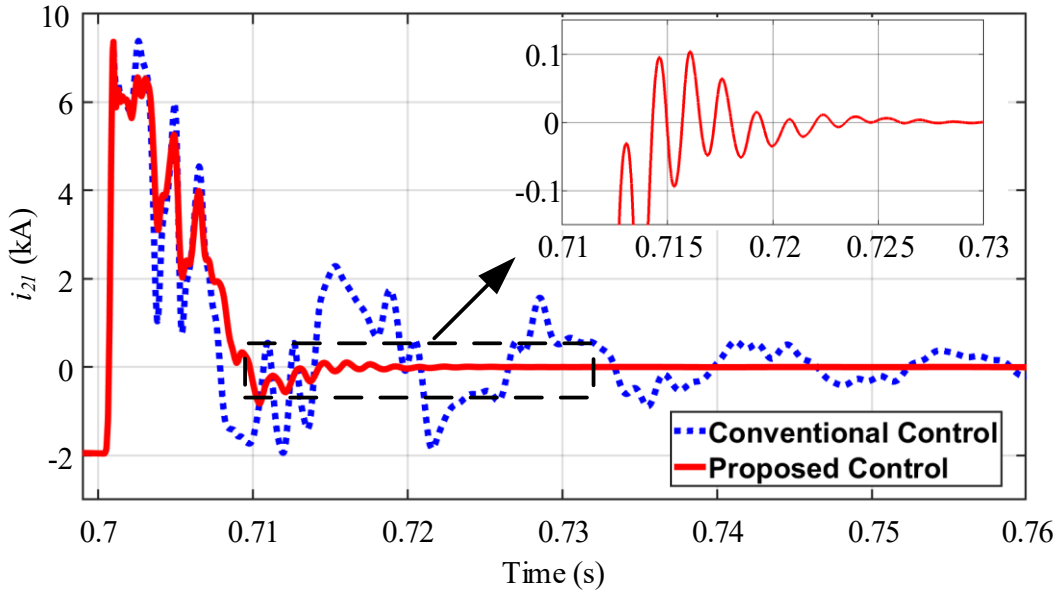


Fig. 6. 11 Comparison of the DCS 21 currents i_{21} with conventional control and proposed control.

6.4.2 Influence of the Virtual Damping Resistance R_v

Further studies with different virtual damping resistance are carried out and the results are compared in Fig. 6.12. As demonstrated in Fig. 6.12 (a), lower R_v results in faster network de-energization, though with larger DC current i_2 and i_3 as depicted by (6.2) and shown in Fig. 6.12 (b) and (d) which has to be handled by the FB-MMC. Therefore, the trade-off between performance and converter current stress must be considered carefully when tuning the virtual resistance. To avoid overcurrent, a saturation block is used to limit the maximum DC terminal current reference i_{2ref} and i_{3ref} at 1.4 pu as shown in Fig. 6.7. As seen in Fig. 6.12 (b) and (d), the maximum DC current is limited to 2.7 kA (1.4 pu). Compared to Terminal 2, severer saturation of DC current is observed at Terminal 3 due to its higher remaining DC voltage during the fault control period due to it being further away from the fault than Terminal 2.

Fig. 6.12 (c) displays the energy absorbed by Station 2 with different virtual damping resistance R_v. The absorbed energy of Station 3 shown in Fig. 6.12 (e) exhibits similar behaviour to that of Station 2 but with higher absorption due to its higher remaining DC terminal voltage. With lower virtual resistance R_v, the FB-MMC absorbs the residual energy from the DC grid quicker for fast de-energization, which is in agreement with Fig. 6.12 (a). When higher R_v is used, it takes longer to suppress the circulating DC current through the DC network and thus, more energy is dissipated by the DC cable resistors and less needs to be absorbed by the FB-MMCs. Consequently, as observed in Fig. 6.12 (c), the energy absorbed by the FB-MMCs with R_v=800 Ω is slightly lower than that with R_v=50 Ω, considering constant residual energy of the DC network that needs to be dissipated by either the DC cables or the FB-MMCs.

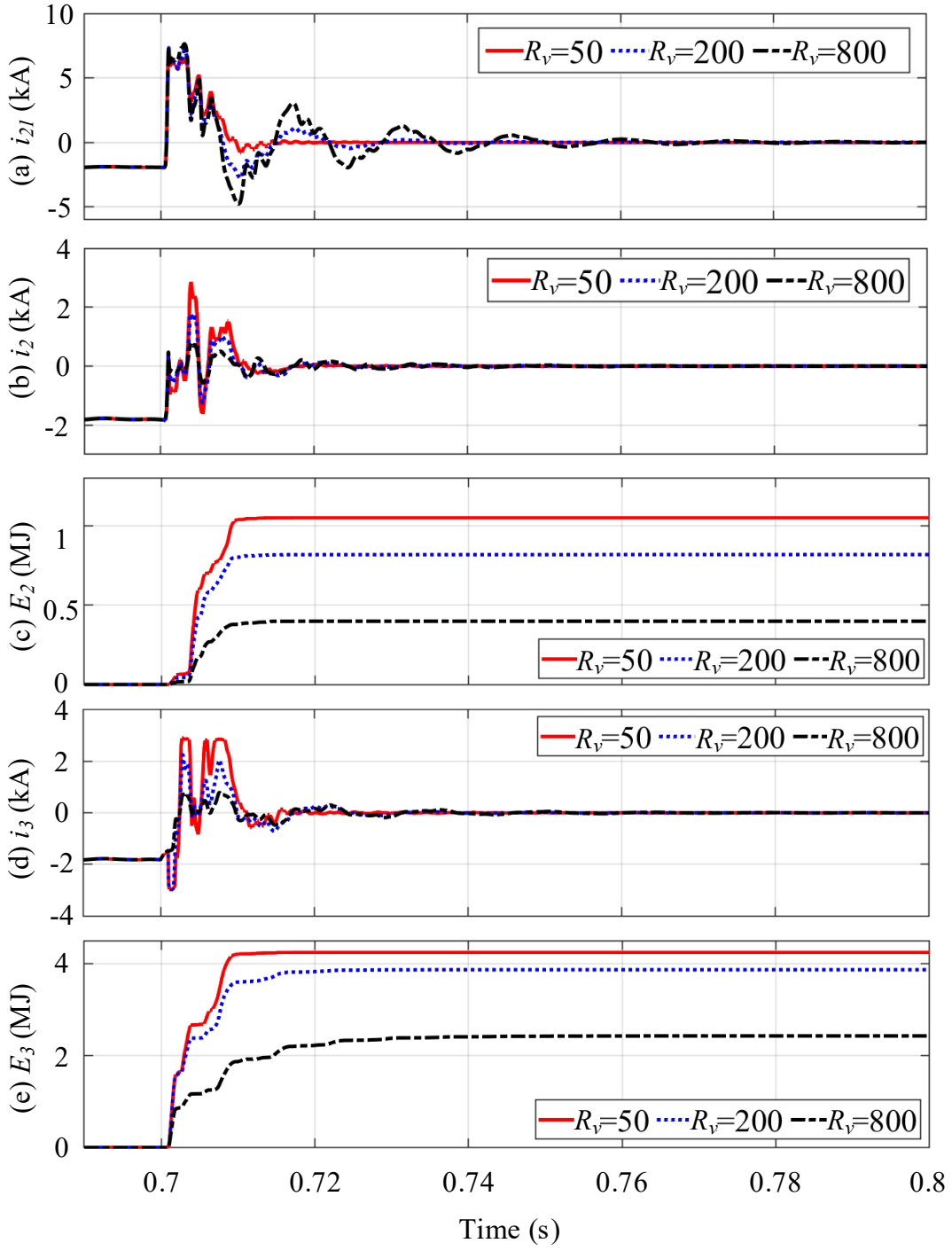


Fig. 6. 12 Influence of the virtual damping resistance R_v on the proposed control: (a) current flowing through DCS 21, (b) DC terminal current of Station 2, (c) energy absorbed by Station 2, (d) DC terminal current of Station 3 and (e) energy absorbed by Station 3.

6.4.3 Influence of DC current control dynamics

The emulation of the virtual damping resistance by the FB-MMCs is dependent on controlling the DC terminal current according to the value of the corresponding DC terminal voltage. As the DC terminal voltages can oscillate at relatively high frequency, the response of the DC current controller which ensures the active DC terminal current follows the reference is critically important. The impact of DC fault current control dynamics on the effect of energy absorption is studied by varying the gain used in the PI controller shown in Fig. 6.7. The gain in this section is timed by an additional k_0 with value of 1, 0.05 and 0.025, respectively Fig. 6.13 compares the waveforms with k_0=1 (value used for previous studies), 0.05, and 0.025 in the DC current control loop.

The waveforms of i_2 and i_{2ref} with k_0=1, 0.05 and 0.025 are shown in Fig. 6.13 (d), (e) and (f), respectively. It can be seen that with lower value of k_0, which effectively reduces the DC current control dynamics, the tracking of current i_2 to its reference deteriorates. Consequently, the DC power of Terminal 2 shows positive values (injecting power into the DC network) during part of the fault control, shown in Fig. 6.13 (b). The power injection can also be observed from the energy absorbed by Terminal 2 shown in Fig. 6.13 (c) around t=0.705s, indicating slower power absorption leading to the longer waiting time for the current i_{21} to drop. From Fig. 6.13 (a), it can be seen that with k_0=0.05 and 0.025, i_{21} still have considerable values at time of 0.705s than that of case with k_0=1 which is in the range of ±100A. The open time of DCS 21 is postponed for about 15ms and 20ms for the cases with k_0=0.05 and 0.025, respectively.

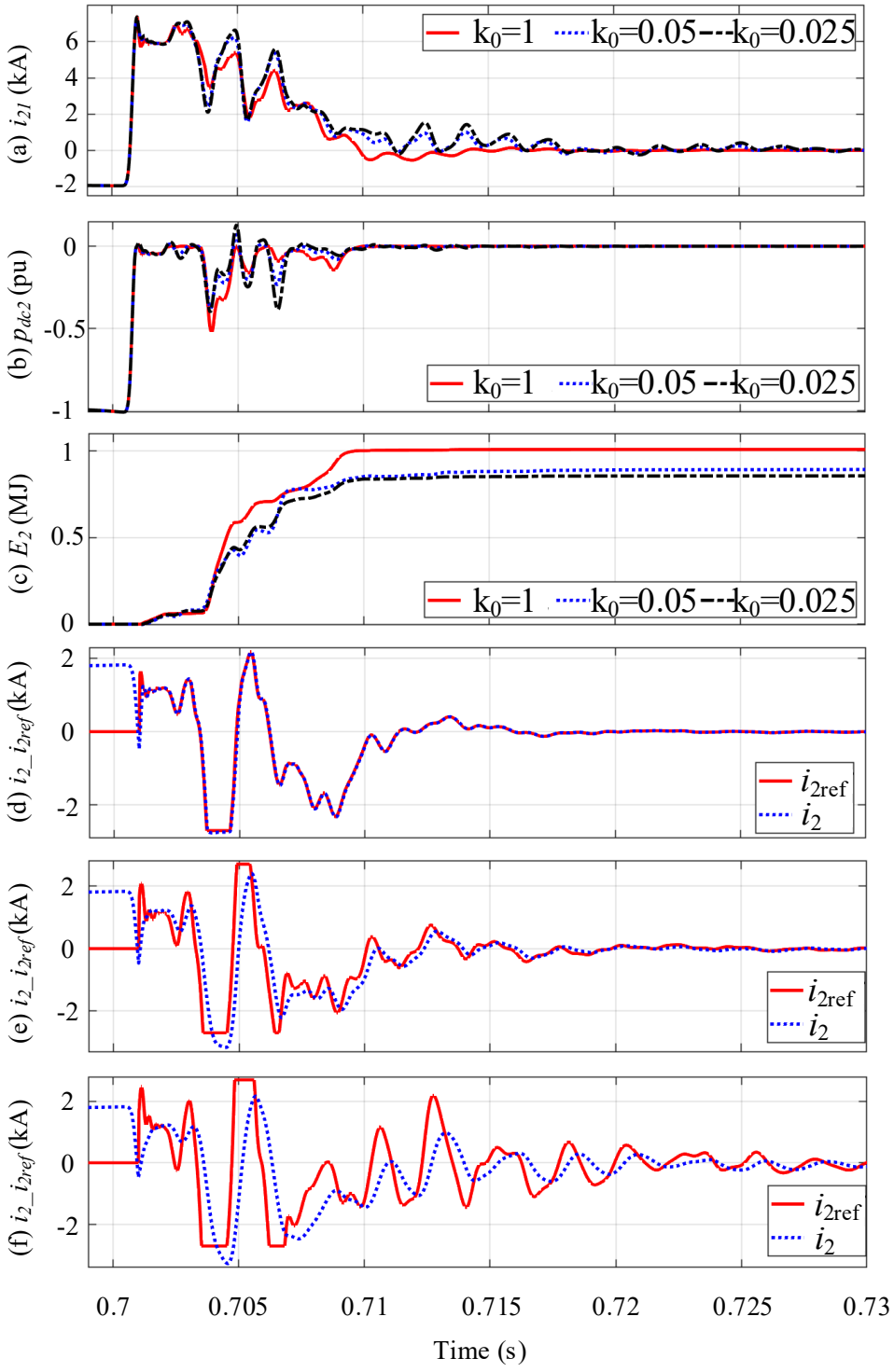


Fig. 6. 13 Influence of the control delay on the proposed control: (a) current flowing through DCS 21, (b) DC power of Station 2, (c) energy absorbed by Station 2, (d) i_2 and i_2 reference when k_0=1, (e) i_2 and i_2 reference when k_0=0.05 and (f) i_2 and i_2 reference when k_0=0.025.

6.4.4 Influence of fault location

The influence of different fault locations on the proposed fault control is studied in this section. Three cases with fault locations shown in Fig. 6.14 are carried out with Fault 1 at the middle of Cable 1, Fault 2 at 5km to Station 2 and Fault 3 at 5km to Station 1.

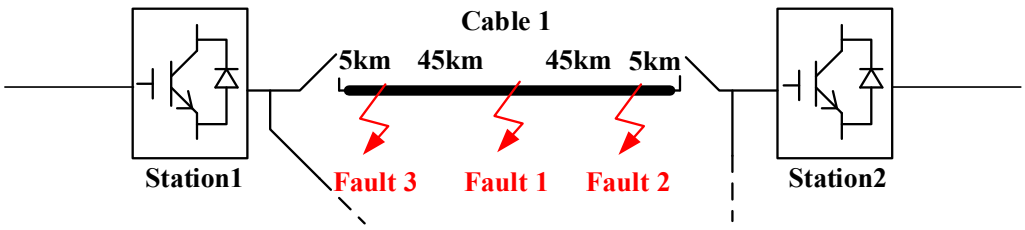


Fig. 6. 14 Locations of different fault cases.

The results are compared in Fig. 6.15. In the Fault 2 case, the fault control is switched in earlier than that in other two cases. However, the fault being close to Station 2 makes the DC voltage drops fast and maintains a very low amplitude, and consequently leading to low energy absorption by Station 2 during the fault control as shown in Fig. 6.15 (b). In contrast, in the Fault 3 case, as the fault is further away from Station 2 and though the fault control is switched in later than that in Fault 1 and 2 case, with higher DC voltage on the Terminal 2, the DC power absorption is higher than the other two fault cases as shown in Fig.6.15 (b) and (c). For the DC power and energy absorbed during the fault control by Station 3 shown in Fig. 6.15 (d) and (e), not much differences are observed as the faults in three cases are all relatively 'far' from Station 3. Slightly drop on the energy absorbed by Station 3 in Fault 3 case due to the significant power absorption increase at Station 2. From Fig. 6.15 (a), the control results of the current of DSC 21 are similar in case of Fault 1 and 3 while i_{21} is largely affected in the case of Fault 2 leading to around 20ms delay for DCS 21 to open. Therefore, from the results, the fault location affects the effectiveness of the proposed control especially when the fault is close to the stations.

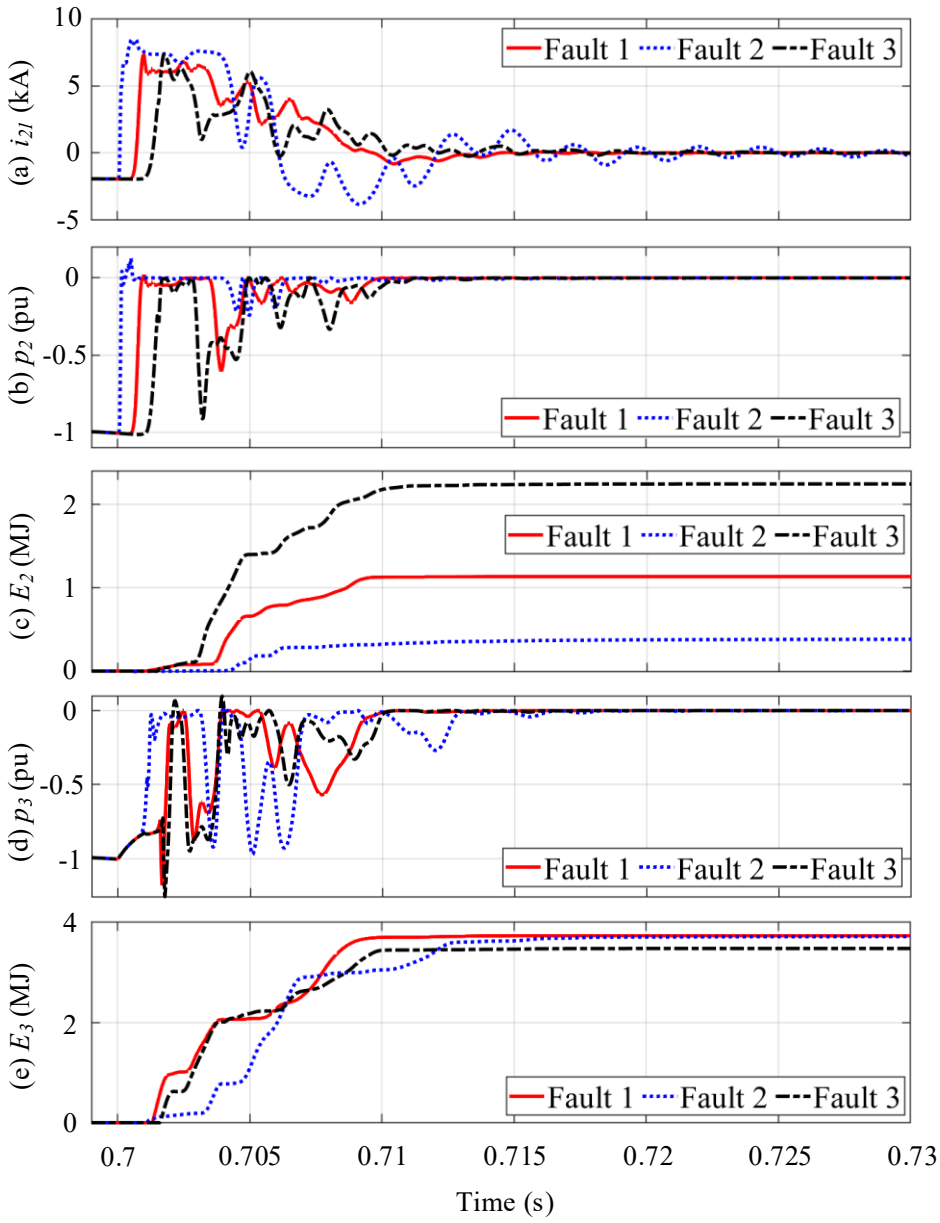


Fig. 6. 15 Influence of the fault location on the proposed control: (a) current flowing through DCS 21, (b) DC power of Station 2, (c) energy absorbed by Station 2, (d) DC power of Station 3 and (e) energy absorbed by Station 3.

6.4.5 System Recovery

The complete protection and recovery process using the proposed virtual damping control is shown in Fig. 6.16 to Fig. 6.18. After isolation of the faulty Cable 1 from the

DC network as described in the above subsection, the FB-MMC based Station 2 and 3 switch to DC voltage control mode at t=0.72 s to charge Cable 2 and 3 and ramp the DC voltage to the rated value in 20 ms, as seen in Fig. 6.16 (a) and Fig. 6.17(a). The HB-MMC at Station 1 is de-blocked at t=0.725 s to restore its terminal voltage to the nominal value, as shown in Fig. 6.18 (a). When the DC voltage across DCCB 2 is close to 1, it is reclosed at t=0.74 s, reconnecting Station 1 to the DC grid. During the DCCB 2 reclosing process, the DC grid voltages and currents do not see disturbance as shown in Fig. 6.16 (a) (b) and Fig. 6.17 (a) (b). Station 1 then takes control of the DC voltage of the DC grid, and Station 2 and 3 subsequently switch back to active power control mode and ramp up (down to negative value) the active power to the rated value in 60 ms, as shown in Fig. 6.16 (c) and Fig. 6.17 (c).

During the DC fault and DC grid restoration, the AC and arm currents of the stations 2 and 3 remain well-regulated without significant overshoots, as demonstrated in Fig. 6.16 (d)(e) and Fig. 6.17 (d)(e). As previously described, 40% over-current capability is considered for all the MMCs. The fault isolation time that the proposed DC fault ride-through scheme offers in this illustration is around 15 ms, much shorter than that with FB-MMC blocking (around 120 ms) and that with conventional control (around 50 ms), which enables a faster system recovery.

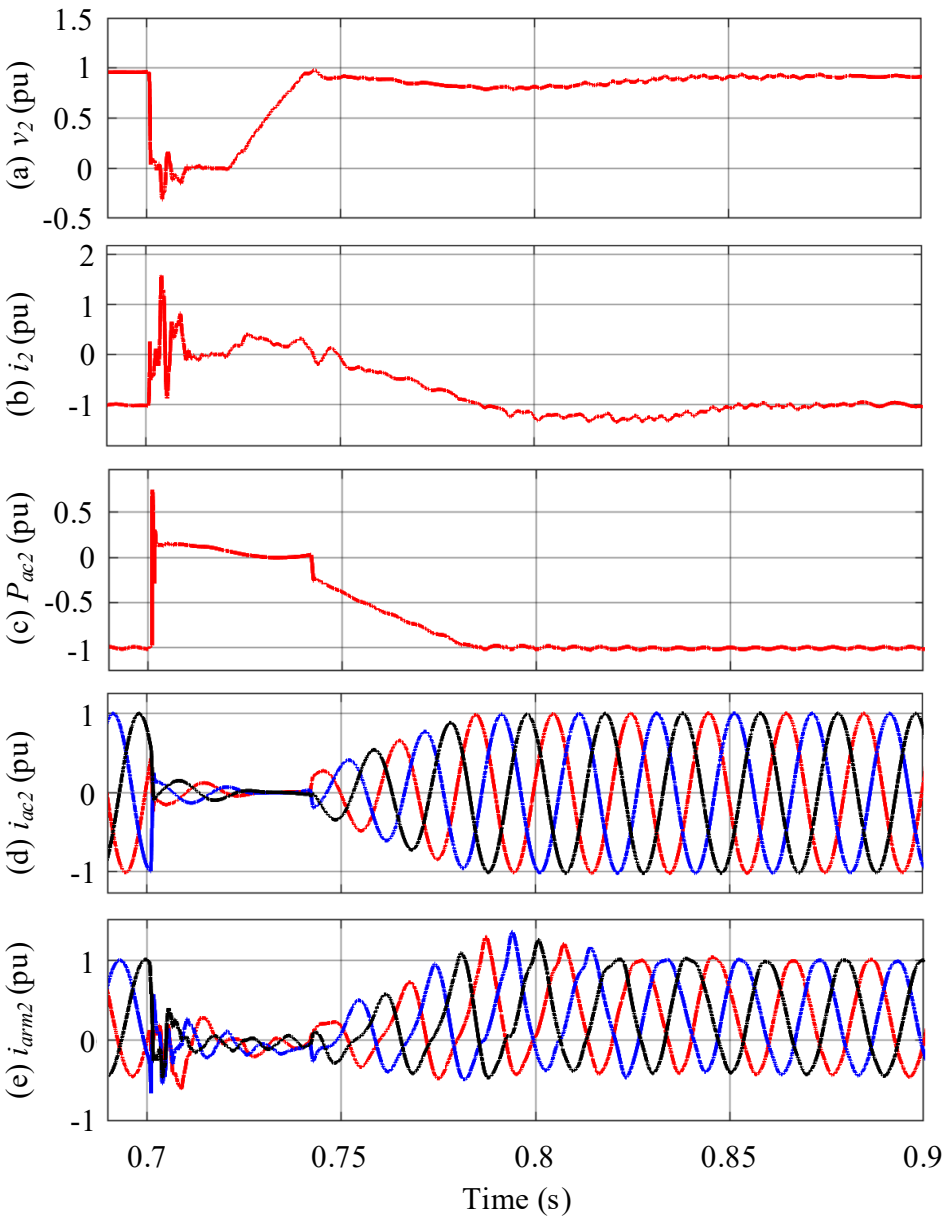


Fig. 6. 16 Waveforms of Station 2 during system recovery: (a) DC voltage, (b) DC current, (c) AC active power, (d) AC currents and (e) arm currents.

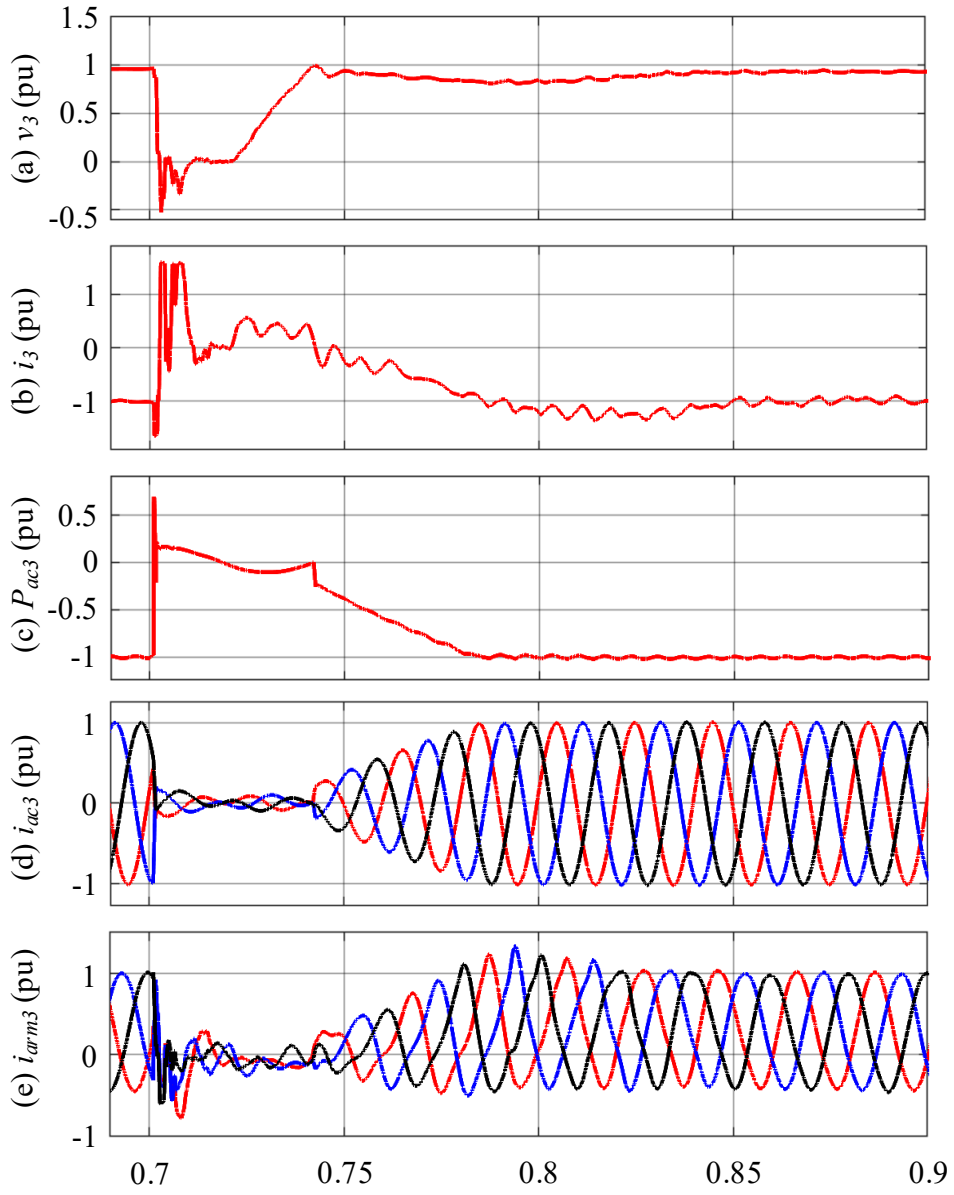


Fig. 6. 17 Waveforms of Station 3 during system recovery: (a) DC voltage, (b) DC current, (c) AC active power, (d) AC currents and (e) arm currents.

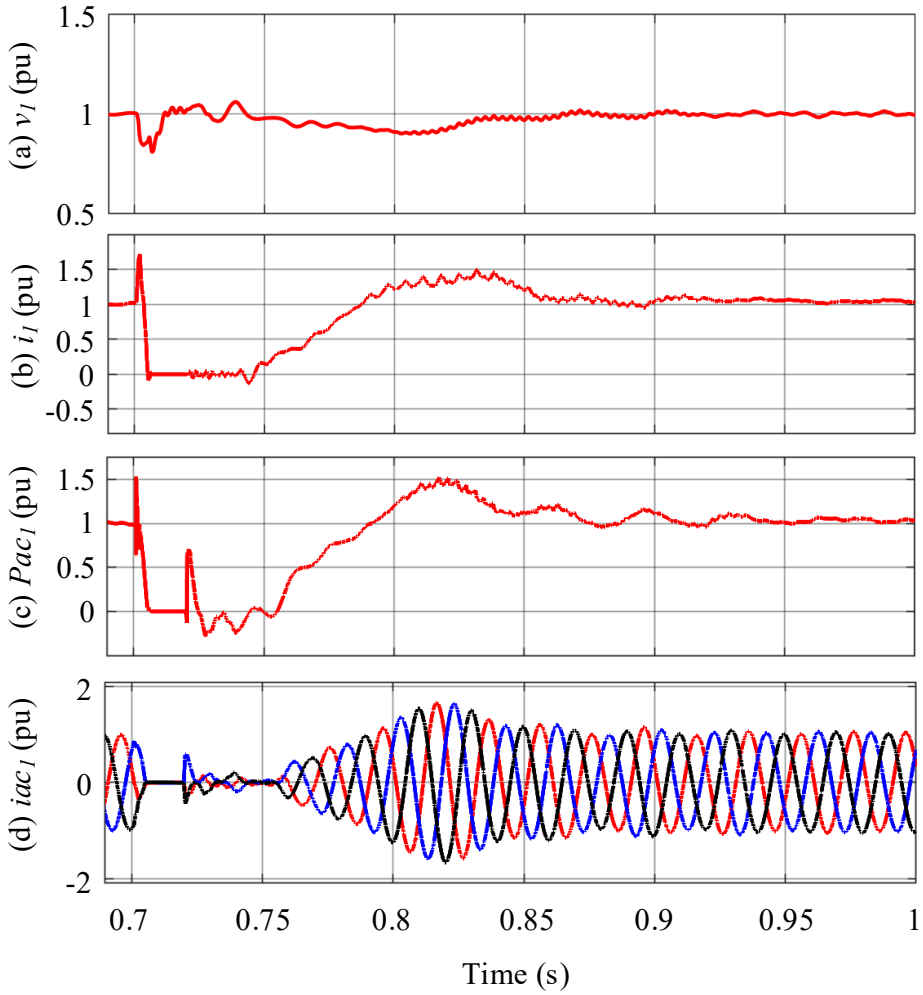


Fig. 6. 18 Waveforms of Station 1 during system recovery: (a) DC voltage, (b) DC current, (c) AC active power and (d) AC currents.

6.5 Conclusion

Conventional active fault current control of FB-MMC during DC faults aims to directly suppress the DC current in the faulty cable for fast fault isolation using DC switches. However, for meshed DC grid, due to the coupling and interconnection of the DC cables, such method may mistakenly lead to energy injection by the FB-MMC to the DC network which deteriorates the fault current suppression during DC faults. A new energy based virtual damping control for FB-MMC is proposed in this chapter to fast suppress the fault current that circulates within the meshed MTDC system. In the

proposed control, the terminal current of the FB-MMC is controlled to follow the terminal voltage during DC faults such that the FB-MMC acts as a virtual resistor to quickly absorb the residual energy from the DC network. Thus, the issue related to the conventional active fault current control is effectively avoided. The operating mechanism of the proposed control is revealed from the energy perspective and the design principle of the virtual resistance is discussed. The simulation results in a three-terminal meshed DC system demonstrate that the fault isolation time is significantly reduced from around 50 ms to 15 ms compared to conventional active fault current control, alleviating interruption of power transmission during DC faults. The impact of the variations of the damping resistance and DC current control delay on the effect of network de-energisation have also been investigated. The influences of DC current control dynamics and fault locations on the effectiveness of the proposed method are carried out. Slower DC current control dynamics can weaken the effectiveness of the proposed control. In addition, if the fault is close to the controlling station, the low DC remaining voltage results in less energy absorption and increases the time required to reenergise the DC network.

Regarding to the influence of the proposed fault current damping control on frequency of the connected AC network, further simulation could be done in the future work. For an initial view for this, the total shut down time of the power delivery is around 80ms shown in Fig. 6.16 and Fig. 6.17 from fault initialled at time of 0.7s to power delivery recovery finalised at time of 0.78s, which is much shorter than that (245ms) in the case using fast DCCBs in Section 5.4.2. This is because the fault isolation speed is fast using the proposed control and no need to reconnect the healthy cables to enable the power delivery path. This will increase the frequency nadir and improve the frequency behaviour significantly where neglectable frequency drop (around 0.05Hz), in view of system operators, can be expected. This also is consistent with the conclusion made in Chapter 5 that once fault is isolated, the recovery process also takes considerable time before power restoration, therefore, the restoration process of the protection strategies (e.g. full selected protection) influences more on the frequency of connected AC system than the fault isolation speed.

Chapter 7 Conclusion and future work

7.1 General conclusions

This thesis focuses on addressing some of the challenges brought by increased renewable power generation and HVDC connection in power networks using improved HVDC system control and protection. The specific challenges addressed in the thesis include the power network inertia reduction leading to deteriorated frequency dynamic in DC/AC hybrid systems under AC disturbances (e.g. load and generation changes) and DC disturbances (e.g. DC faults), and DC fault protection of large scale multi-terminal DC systems.

For improved frequency response in a DC/AC hybrid system, the use of HVDC system for power system frequency support has been studied first. Detailed simulations have been carried out to investigate and validate various system frequency support strategies. In a two-terminal system, in a frequency event at the power controlling terminal, the active power output from the converter can be directly modulated to provide frequency support to the affected AC network. In contrast, for a frequency event at the DC voltage controlling terminal, through active DC voltage manipulation by the converter controlling the DC voltage, and active power modulation by the power controlling terminal upon the detection of DC voltage derivation can also provide fast and effective frequency support to the affected AC network. Different parameter designs have been discussed and their impact on frequency response studied. For a multi-terminal HVDC system connecting different AC networks, power shortage sharing among the supporting terminals needs to be optimized. AC networks with higher capacities are designed to share more power than those with lower capacities, so as to improve the overall system frequency. Different design options considering frequency events at both power controlling and DC voltage controlling terminals have been discussed. In a frequency event at one of the power controlling terminals, the active power output from the other converters can be better shared by modulating the active power according to the resultant frequency derivation during the frequency support process. In contrast, for a

frequency event at the DC voltage controlling terminal, power sharing from the remaining power controlling terminal can be controlled by properly setting up their droop constants, e.g. according to the network capacity, so as to provide similar frequency performance at the healthy AC networks.

DC faults cause the interruption of transmitted power through the DC network and affect the connected AC network operation, e.g., causing frequency transient event. The impact of different DC fault protection arrangements on frequency response of connected AC systems has been investigated. A representative three-terminal meshed MTDC network was modelled and used for case studies. The frequency responses of connected AC network with different DC fault protection arrangements based on DC switches, slow DCCBs and fast DCCBs have been carried out. It has shown that the frequency performance and frequency nadir are improved with faster DC fault isolation and system restoration. Both the amount of power loss and outage duration affect system frequency response, and thus the two need to be considered simultaneously when determining the maximum "loss-of-infeed" for future AC-DC hybrid power grids. The studies also reveal that the speed of the adopted DCCBs does not significantly affect the power outage duration since once converter blocking is initiated, the recovery process which involves recharging DC cables and re-starting converters usually require considerably longer time to establish.

The protection of a meshed DC network using both FB-MMC and HB-MMC is investigated focusing on the fast DC grid de-energisation using the FB-MMC. Conventional active fault current control of FB-MMC during DC faults aims to directly suppress the DC current in the faulty cable for fast fault isolation using DC switches. However, for meshed DC grid, due to the coupling and interconnection of the DC cables, such method becomes less effective and may even lead to energy injection by the FB-MMC to the DC network which deteriorates the fault current suppression during DC faults. A new energy based virtual damping control for FB-MMC is proposed in this thesis to fast suppress the fault current that circulates within the meshed MTDC system in the event of DC faults. In the proposed control, the terminal current of the FB-MMC is controlled to follow the terminal voltage during DC faults such that the FB-MMC acts as

a virtual resistor to quickly absorb the residual energy from the DC network. Thus, the issue related to the conventional active fault current control is effectively avoided. The operating mechanism of the proposed control is revealed from the energy perspective and the design principle of the virtual resistance is discussed. The impact of the variations of the damping resistance, DC current control dynamics and fault locations on the effectiveness of network de-energisation have also been investigated. The simulation results in a three-terminal meshed DC system demonstrated that the fault isolation time is significantly reduced from around 50 ms to 15 ms compared to conventional active fault current control, alleviating interruption of power transmission during DC faults.

7.2 Suggestions for future research

Potential areas of future research include:

- In MTDC systems, the power shortage sharing strategy between frequency-support-providing terminals need to be further investigated, including the possibility of absence of communications between sharing terminals and the potential possibility of passive network participation in the power shortage sharing considering it's secondary frequency regulation.

- Further study on the network code of frequency response to different AC and DC system disturbances can be carried out in order to raise the detailed requirements for the DC protection systems, considering the increase penetration of power electronic systems in the future power network.

- The frequency response to the protection strategy proposed in Chapter 6 can be further investigated comparing with other protection strategies.

- The investigation of the protection strategy can be carried out in larger MTDC systems with many different types of converters and protection devices considering different operating speed and constraints.

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Author's Publications

[1] Zhou, D., Rahman, M. H., Xu, L., & Wang, Y., "Impact *of DC protection strategy of large HVDC network on frequency response of the connected AC system*. 1-6. Paper presented" at The 9th International Conference on Power Electronics, Machines and Drives, 2018, Liverpool, United Kingdom.

Abstract: Integration of renewable energy generations requires the transmission of bulky power over long distance and HVDC transmission systems become a more preferable choice compared to conventional HVAC systems. For HVDC systems, one of the important concerns is the DC protection strategy which can significantly impact on the connected AC system performance, e.g. system frequency. The maximum loss-of-infeed for a AC network is highly dependent on the duration of the power outage, and the impacts of DC fault protection arrangements which result in different speed of power restoration on the connected AC system, on the system frequency, have not been properly understood. Different DC protection arrangements using DC disconnectors, fast and slow DC circuit breakers on frequency response of the connected AC networks are investigated. A 3-terminal meshed HVDC system is studied to demonstrate system behaviour during DC faults.

[2] Zhou, D., Rui. L, Xu, L., & Wang, Y., "Energy *Based Virtual Damping Control of FB-MMCs for HVDC Grid*", IEEE Journal of Emerging and Selected Topics in Power Electronic. (under first-round review)

Abstract: Full-bridge submodule based modular multilevel converters (FB-MMCs) have attracted wide attention due to the DC fault blocking capability. However, the blocking of the FB-MMC can only suppress its DC terminal current while the fault currents may still circulate along the meshed DC network. To address this issue, an energy based virtual damping control is proposed, where the DC terminal current of the FB-MMC is regulated to follow the DC voltage in the event of a DC fault. The FB-MMC is thus controlled as a virtual damping resistor to actively absorb the residual energy in the DC network and quickly suppress the potential circulating DC fault currents. This enables fast fault isolation using DC switches and thereby fast fault recovery after fault isolation. The fault

isolation time is significantly reduced from around 120 ms with the FB-MMC simply being blocked and 50ms with the conventional FB-MMC fault control method to around 15 ms. The validity of the proposed control is verified in a three-terminal meshed DC network.