Low-Voltage Organic Transistors with High Transconductance

By

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This thesis is the result of the author's original research. It has been accomplished by the author and has not been previously submitted for examination which has led to the award of a degree.

Afra Salim Mohamed Al Ruzaiqi

Date: January 2020

Dedicated to my supervisor,

parents

and

sisters

for their endless support

and encouragement

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In the name of Allah, the Most Gracious and the Most Merciful Alhamdulillah, all praises to Allah for giving me the strength and patience to complete this PhD journey.

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Author’s declaration

I declare that all work presented in this thesis has been carried out by me, unless otherwise acknowledged.

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2020

Abstract

This thesis presents the development of low-voltage organic thin-film transistors with high transconductance. This was achieved by employing ultra-thin bi-layer gate dielectric consisting of aluminium oxide (AlO_x) and a self-assembled monolayer of octadecyl phosphonic acid ($C_{18}PA$) and by increasing the channel width of the transistors through the implementation of the multi-finger source/drain contacts. The transistors based on dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) exhibited low turn-on voltage and a.c. transconductance around 30 to 60 μS. Transistor amplifiers based on such transistors exhibited voltage gain approaching 10 V/V and a gain of about 2 V/V when the supply voltage was limited to 5 V. Next, a series of [n]phenacenes ([n] = 5, 6, or 7) was used for the first time in combination with the thin $AlO_x/C_{18}PA$ dielectric bi-layer. Regardless of the substrate and the source-drain contact geometry, the field-effect mobility of such transistors was found to increase with increasing length of the conjugated [n]phenacene core, leading to the best performance for [7]phenacene with the largest average field-effect mobility of 0.27 $cm^2/V{\cdot}s$ for transistors on glass and 0.092 $cm^2/V{\cdot}s$ for transistors on flexible PEN. The highest transconductance of 12.2 μS was achieved for [7]phenacene transistors on glass, which was lower than that achieved for DNTT transistors. In addition, nearly hysteresis-free behaviour, improved charge carrier injection/extraction properties, and reduced threshold voltage were achieved. Finally, a semi-empirical transistor model was developed in Matlab. The model was validated using d.c. and a.c. measurements obtained on DNTT transistors with high transconductance. Four fitting parameters were extracted by optimising a fitting function using genetic algorithm. The model reproduces the d.c. transistor measurements with high accuracy. The error between the measured and simulated peak-to-peak a.c. transconductance values ranged from 1.7% to 11.6%.

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List of Abbreviations and Symbols

$\frac{\Delta L}{L}$	The channel length modulation interpolation
λ	Channel length modulation factor
μ	Field-effect mobility
γ	Mobility enhancement factor
ε_0	Permittivity of the vacuum
μ_0	Low-field mobility
ε_r	Relative permittivity or dielectric constant
δ_{VT}	Threshold voltage bias sensitivity
ADC	Ammonium dichromate
Ag	Sliver
Al	Aluminium
AlO_x	Aluminium oxide
AMOLED	Active Matrix OLED
ATO	Al_2O_y/TiO_x
Au	Gold
$Ba_xSr_{1-x}TiO_3$	Barium Strontium Titanate
BBL	Poly(benzimidazobenzophenanthroline)
BTBT	[1]benzothieno[3,2-b][1]benzothiophene
C	The gate dielectric capacitance.
C_{10}-DNTT	2,9-didecyldi- naphtho[2,3-b:2^0,3^0-f]thieno[3,2-b]thiophene
C_{18}PA	Octadecyl phosphonic acid
C_8-BTBT	2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene
C_{diel}	Dielectric capacitance
CeO_2	Ceric oxide
CMOS	Complementary metal-oxide-semiconductor
COC	Cyclic olefin copolymer
Cr	Chromium
CuPc	Copper phthalocyanine
D	Drain
d	Thickness of the dielectric layer
DNTT	Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene
DPh-DNTT	2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b] thiophene
DPP	Diketopyrrolopyrrole
dq	Charge at a segment of the dielectric layer
dx	A segment of the channel length
$Eu(tta)_3L$	Lanthanide complex of tta=2-thenoyltrifluoroacetonate, L=4,5-pinene bipyridine)
E_x	Electric field
f	Frequency

F_4TCNQ	2,3,5,6-tetrafluoro-7,7,8,8- tetracyanoquinodimethane
F8BT	Poly(9,9-din-octylfluorene-alt-benzothiadiazole)
G	Gate
g_d	The drain conductance of the transistor
G_m	Transconductance
HfO_2	Hafnium oxide
HOMO	Highest occupied molecular orbital
I_D	Drain current
i_d	Modulation in the drain current
I_G	Gate leakage current
I_{OFF}	Off-state current
I_{ON}	On-state current
I_{ON}/I_{OFF}	On/off ratio
k	Relative permittivity or dielectric constant
L	Channel length
La_2O_3	Lanthanum oxide
LED	Light emitting diodes
LUMO	Lowest unoccupied molecular orbital
MIM	Metal-insulator-metal
MRT	Multi-trapping and release
MSE	Mean square error
Nd_2O_3	Neodymium oxide
Novaled NDP-9	Novaled dopant p-type, number 9
O_3	Ozone
ODPA	Octadecylphosphonic acid
OECT	Organic electrochemical transistor
OFET	Organic field effect transistor
OLED	Organic light emitting diode
OSC	Organic solar cell
OTFT	Organic thin-film transistor
OTS	Octadecyltrichlorosilane
PANI	Polyaniline
pBTTT	Poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3, 2-b]thiophene
PEN	Poly (ethylene 2,6-naphthalate)
PET	Polyethylene terephthalate
PFBT	Pentafluorobenzenethiol
PI	Polyimide
PMMA	Polymethyl methacrylate
PNBS	Selenophene containing polymer
PQT-12	Poly(3,3‴-didode-cylquaterthiophene)
Pr_2O_3	Praseodymium oxide
PTAA	Polytriarylamines
PVA	Polyvinyl alcohol

PVP	Polyvinyl phenol
Q	Charge
R_d	Drain resistor
RFID	Radio frequency identification tags
S	Source
S	Subthreshold slope
SAM	Self-assembled monolayer
SB-OTFTs	Schottky barrier organic thin-film transistor
SiO_2	Silicon dioxide
SRAM	Static random access memory
Ta_2O_5	Tantalum pentoxide
TFT	Thin-film transistor
TiO_2	Titanium dioxide
TIPS-pentacene	6,13-bis(triisopropylsilylethynyl)pentacene
v	Velocity of the charge carriers
V	Voltage
$V_{(x)}$	Voltage potential at point x of the channel
V_D	Drain voltage
V_{DD}	Supply voltages
VD_{EODR}	Effective voltage overdrive on the drain side
V_{DS}	Drain-to-source voltage
V_G	Gate voltage
v_g	Gate bias sinusoidal voltage
V_{GS}	Gate-to-source voltage
v_{out}	Output voltage
V_{pp}	Peak-to-peak voltage
VRH	Variable range hopping
VS_{EODR}	Effective voltage overdrive on the source side
V_{SS}	Subthreshold slope voltage
V_T	Threshold voltage
W	Channel width
Y_2O_3	Yttrium oxide
ZrO_2	Zirconium dioxide

List of Publications

Journal papers

1. A. Al Ruzaiqi, H. Okamoto, Y. Kubozono, U. Zschieschang, H. Klauk, P. Baran, H. Gleskova, "Low-voltage organic thin-film transistors based on [n]phenacenes", *Organic Electronics*, vol. 73, pp. 286-291, 2019.
2. A. Al Ruzaiqi, A. Ishaku, H. Gleskova, "Organic thin film transistors with multi-finger contacts as voltage amplifiers", *IEEE Access*, vol. 6, pp. 43770-43775, 2018.
3. S. Hannah, J. Cardona, D. Lamprou, P. Sutta, P. Baran, A. Ruzaiqi, K. Johnston, H. Gleskova, "Interplay between vacuum-grown monolayers of alkylphosphonic acids and the performance of organic transistors based on dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene", *ACS Applied Materials & Interfaces*, vol. 8, no. 38, pp. 25405-25414, 2016.

Conference papers

1. A. Al Ruzaiqi, B. Nikolov, L. Chen, H. Gleskova, "Compact modeling of organic transistors with multi-finger contacts", in *IEEE International Conference on Flexible and Printable Sensors and Systems*, 8th – 10th July, Glasgow, United Kingdom, 2019.
2. A. A. Ishaku, A. Al Ruzaiqi, H. Gleskova, "Low-voltage high-transconductance dinaphtho-[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT) transistors on polyethylene naphthalate (PEN) foils". *IEEE International Conference on Flexible and Printable Sensors and Systems*, 8th – 10th July, Glasgow, United Kingdom.

Chapter 1

Introduction

1.1. Organic electronics

Organic electronics refers to electronic devices such as transistors, light-emitting diodes (OLEDs), organic solar cells (OSCs), organic field-effect transistors (OFETs) and sensors [1], etc., that are based on organic materials. They have drawn much attention for several novel applications because of their unique advantages such as light weight, low-cost production and low fabrication temperature, enabling them to be fabricated on flexible substrates such as plastic [2]. Research into organic electronic devices covers various aspects ranging from synthesising new materials to the design of new devices, studies of mechanical flexibility, and development of new manufacturing techniques [3]. Furthermore, device modelling complements various experimental device optimisation efforts.

OLED is fabricated by placing a number of thin organic films between two electrodes. Their advantages over the conventional/inorganic LED include mechanical flexibility, low-power consumption and superior light emission. Flexible displays with sharper images were achieved by using OLEDs [4]. Active Matrix OLED (AMOLED) are used in the current high-end smart phone displays and TVs [5]. Organic solar cells are fabricated using organic semiconductors that convert the absorbed light to electricity [6]. Figure 1.1(a) shows a flexible OLED screen and organic flexible solar cell is depicted in Figure 1.1(b). Figure 1.2 shows AMOLED display implemented in a foldable smartphone.

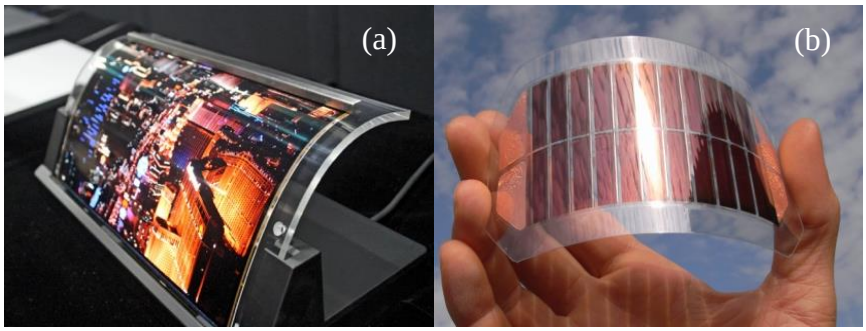

Figure 1.1: OLED [7] (a) and organic solar cell [8] (b).

Figure 1.2: Smartphone with AMOLED display [9].

1.2. Motivation for research

Optimising the electrical performance of the organic transistor is an ongoing process to produce a reliable building block for the future organic circuits and sensors. There are numerous papers addressing the transistor development; references [10-17] represent a few.

The transistor optimisation aims to achieve high field-effect mobility, hysteresis-free characteristics, high transconductance, low-voltage operation, mechanical flexibly, etc. The recent progress in the organic transistors have made them compelling candidates for upcoming flexible and wearable applications such as biosensors [18-20], sensors for biomedical applications [21-24] and tactile sensors [25].

This thesis focuses on furthering the development of low-voltage organic thin-film transistors (OTFTs) by increasing the transistor on-current and its transconductance. By redesigning the transistor's source/drain contacts and selecting appropriate combination of organic semiconductor and gate dielectric, low-voltage OTFTs suitable for low-cost wearable/flexible analogue sensor circuits can be developed. The modification of the source/drain contacts aims to increase the on-state drain current and the transistor transconductance, whereas the low-voltage operation was achieved through the use of an ultra-thin bi-layer gate dielectric that exhibits high capacitance and low leakage current.

For flexible or wearable analogue sensors, it may be desirable to pre-process the signal produced by the stimulus at the collection site. This pre-processing typically consists of converting the signal into voltage with subsequent amplification. Consequently, technologies that offer such attributes, i.e. transistors with high transconductance, are needed. Another important demand for flexible/wearable sensors is the low-voltage operation; hence, it is of interest to investigate methods and techniques for producing low-voltage organic transistors with high transconductance.

1.3. Thesis objectives

This thesis presents low-voltage, high-transconductance OTFTs that employ ultra-thin bi-layer gate dielectric and multi-finger source and drain contacts. The former grants low-voltage operation because such dielectric layer exhibits high capacitance, whereas the latter provides a high channel width-to-length ratio (*W/L*) which results in high on-state current and high transconductance. The ultra-thin gate dielectric bi-layer consists of aluminium oxide (AlO_x) prepared by UV/ozone oxidation and a self-assembled monolayer of octadecyl phosphonic acid ($C_{18}PA$) prepared by vacuum evaporation. The aim was to develop and optimise the transistors based on dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) because such transistors have already shown low-voltage operation [26]. To advance such transistors, multi-finger source/drain contacts were introduced and the performance of the fabricated transistors was investigated under d.c. and a.c. conditions.

Next, building on the success of the low-voltage DNTT transistors with multi-finger source/drain contacts, new organic semiconductors based on [n]phenacenes were implemented into OTFTs and the fabricated transistors were tested. To our knowledge, it was the first attempt to combine the ultra-thin bi-layer gate dielectric and multi-finger contact structure with [n]phenacenes to produce low-voltage OTFTs.

Finally, a semi-empirical model to reproduce the transistor behaviour was built and tested in Matlab. Matlab has been chosen because it is widely used in science and engineering. The model simulates the measured transfer characteristics of a transistor to predict its behaviour under other circuit condition.

1.4. Thesis outline

A summary of this thesis is as follows: Background information on OTFTs is given in Chapter 2. This includes transistor operation and transistor materials, structures, and

parameters. Chapter 3 describes the methodology, namely the fabrication process of metal-insulator-metal (MIM) structures and OTFTs along with the measurements and parameter extraction protocols. The performance of DNTT OTFTs with multi-finger source/drain contacts is discussed in Chapter 4. The chapter summarizes the d.c. and a.c. transistor measurements as well as results of a simple transistor amplifier. Chapter 5 demonstrates the use of [n]phenacene organic semiconductors (where n ranges from 5 to 7) in low-voltage OTFTs on two different substrates (glass and poly (ethylene 2,6-naphthalate) (PEN)) accompanied by an in-depth analysis of the transistor performance. A semi-empirical compact model built in Matlab is presented in Chapter 6. The measurements presented in Chapter 4 serve as a base for the model verification. Finally, Chapter 7 concludes the thesis and provides a summary of the obtained results and suggestions for the future work.

1.5. Thesis contribution

This research represents a considerable advancement of low-voltage OTFTs either on rigid (glass) or flexible (PEN) substrates. The main contributions are summarised below.

The use of multi-finger source/drain contacts in DNTT-based OTFTs provided high *W/L* ratio while keeping overall device area small. The *W/L* ratio was increased by a factor of about ~11 compared to the previous standard structure. Yet, the transistors exhibited low turn-on voltage and one of the highest transconductances reported to date. In addition, a voltage amplifier based on such transistors provided voltage gain even when the supply voltage was limited to −5 V. Finally, such transistors are suitable for working with a.c. frequencies up to at least 1 kHz.

P-channel OTFTs based on [5]phenacene, [6]phenacene, and [7]phenacene and a bi-layer gate dielectric consisting of aluminium oxide and octadecyl phosphonic acid self-sampled monolayer uncovered the potential of these organic semiconductors for the

fabrication of low-voltage OTFTs. To our knowledge, this material combination has been demonstrated for the first time. The OTFTs exhibited good electrical performance with mobility of up to 0.27 $cm^2/V \cdot s$ and threshold voltage of −3.4 V.

The developed semi-empirical OTFT model builds on the model developed previously [27]. However, it reduces the number of fitting parameters and introduces the use of genetic algorithm to compute these parameters. The model represents the first step towards PSpice-like simulations involving low-voltage transistors with multi-finger source/drain contacts.

Chapter 2

Organic thin-film transistors

This chapter elaborates some of the important aspects of the organic thin-film transistor with the focus on low-voltage operation. It provides the fundamental transistor figures of merit and discusses the transistor structures and operation. The chapter outline is as follows. Firstly, an overview of metal-insulator-metal structure is presented in Section 2.1 while introduction of OTFTs and their applications are given in Section 2.2. Additionally, the established transistor structures and their advantages are explained in Section 2.3. Section 2.4 shows the materials available for the different parts/layers of the transistors. The transistor operation and its various operation regimes are presented in Sections 2.5 and 2.6 respectively. Furthermore, the main transistor parameters are outlined in Section 2.7. Section 2.8 gives a brief summary of the charge carrier transport models. Finally, the state-of-the-art of low-voltage OTFTs are presented in Section 2.9

2.1. Metal-insulator-metal structure (MIM)

The MIM structure is a parallel plate capacitor, as shown in Figure 2.1, consisting of two metal electrodes (of the same type or different) separated by a dielectric material. When voltage is applied across the electrodes, positive and negative charges accumulate on the electrodes of the capacitor, i.e. the positive charge accumulates on the electrode connected to the positive side of the voltage source and the negative charge on the electrode connected to the negative side; hence, an electric filed is produced. This electric field causes the polarisation of the dielectric material, i.e. formation of the electric dipoles. The relative permittivity ε_r (or dielectric constant k) is a term used to describe the ability of the dielectric material to polarize (easier polarisation leads to a larger k/ε_r value). High-k material will exhibit higher capacitance and lead to higher charge on its electrodes for the given applied voltage. Consequently, the capacitance of MIM structure is given by:

$$C = {}^{Q}/_{V} \tag{2.1}$$

where, Q is the charge in coulomb and V is the applied voltage in volts. The capacitance per unit area in F/cm2 for a parallel-plate capacitor is given by:

$$C = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{2.2}$$

where ε_0 is the permittivity of the vacuum of 8.854 10^{-12} F/m, ε_r is the relative permittivity of the given dielectric and d is the separation between the metal electrodes, i.e. the thickness of the dielectric.

The MIM structure plays an important role in assessing the properties of gate dielectric used in OTFTs. It is usually fabricated alongside the OTFTs [28-29].

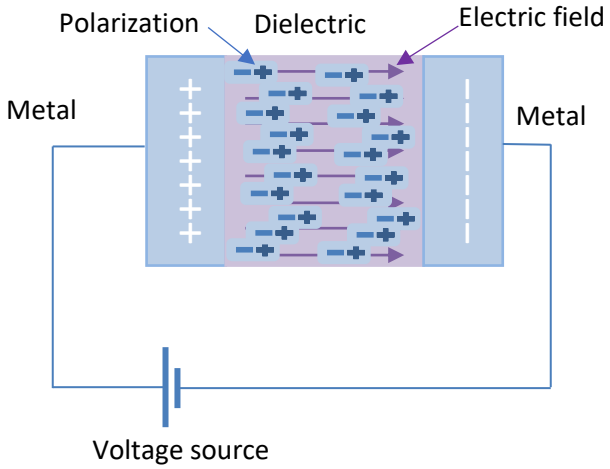

Figure 2.1: Parallel plate capacitor.

2.2. Application of low-voltage organic thin-film transistors

Organic transistors are envisioned to be used in many large-area applications such as wireless power transmission sheet, communication sheet, active-matrix, flexible and rollable flat-panel displays, radio frequency identification tags (RFID) (Figure 2.2(a)), sensors, banknotes, price/inventory tags, bio-electronics (e.g. sensing stamps), disposable and wearable electronics and cloths, e-skin [30], e-book, e-paper (Figure 2.2(b)), storage devices e.g. static random access memory (SRAM), flexible smart cards, touch screen mobile phones, e-textile in textile electronic circuit, flexible integrated circuits, and optoelectronic devices [31-38].

Owing to the organic transistor advantages such as environmentally-friendly materials, low-cost and large-area production, flexibility (they can be fabricated on low-cost flexible substrate such as paper [39] and plastic), light-weight, large throughput, low fabrication temperature, and the ability to implement manufacturing techniques such as printing [38], spin-coating, and drop casting [32,33,35,38,40], they have become very attractive for many new applications.

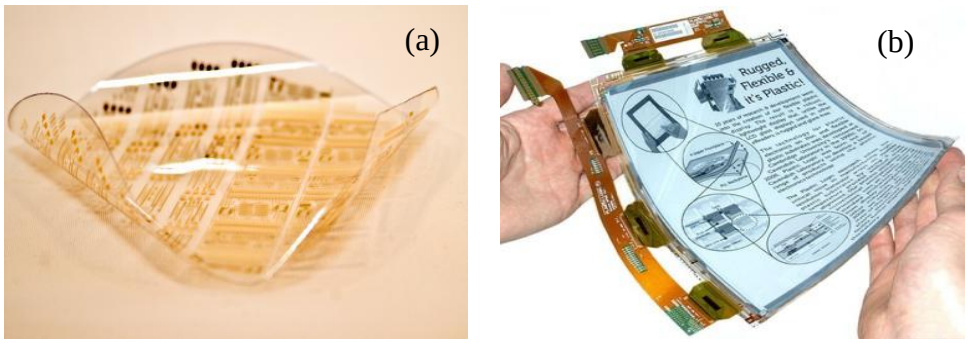

Figure 2.2: Organic RFID [41] (a) and E-paper [42] (b).

2.3. OTFT structures

Depending on the position of the transistor electrodes (gate, source and drain) and the organic semiconductor layer, there are four possible OTFT structures: (i) top-contact top-gate, (ii) top-contact bottom-gate, (iii) bottom-contact top-gate, and (iv) bottom-contact bottom-gate, as shown in Figure 2.3. Also, there is always a dielectric layer, i.e. gate dielectric, that isolates the gate electrode from the semiconductor layer. The top-gate structure with either bottom- or top-contact requires more intricate fabrication procedure because the formation of the gate dielectric on top of the semiconductor layer may lead to a 'contamination' of the organic semiconductor. In addition, the bottom-gate top-contact OTFT structure often exhibits lower source/drain contact resistance compared to bottom-gate bottom-contact OTFT. In the latter the charge carrier injection effective area is smaller and, therefore, higher field-effect mobility values are observed from the bottom-gate top-contact OTFT. Finally, bottom-gate bottom-contact OTFT has two main advantages: (i) the gate dielectric is deposited before the semiconductor layer and therefore causing no harm to it and (ii) the use of standard lithographic techniques for source/drain contacts allows OTFTs with short channel lengths [35].

Using high-quality monolayer of pentafluorobenzenethiol (PFBT) between the source/drain contacts and DPh-DNTT organic semiconductor resulted in improved charge carrier transport because the carrier injection barrier was reduced as a result of large interface dipole and the improved morphology of the organic semiconductor near the contacts. Such treatment resulted in reduction of contact resistance of the bottom-gate bottom-contact structure compared to similar structure of bottom-gate top-contact (for top-contact 56 Ωcm, bottom-contact 29 Ωcm) even when the channel length was aggressively reduced to 0.6 μm, thus high frequency device with mobility of 2 $cm^2/V \cdot s$ was obtained based on DPh-DNTT [43].

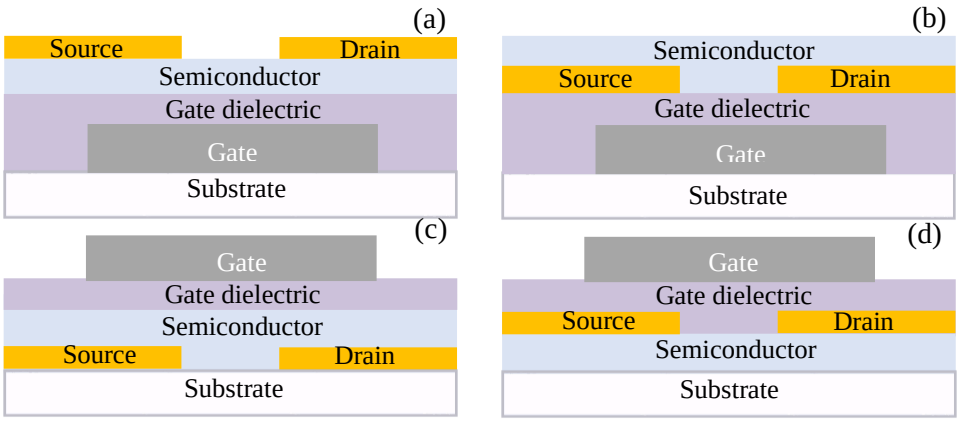

Figure 2.3: OTFT structures: top-contact bottom-gate (a), bottom-contact bottom-gate (b), bottom-contact top-gate (c), and top-contact top-gate (d).

2.4. OTFT materials

2.4.1 Gate electrode and source/drain contacts

For the gate electrode, metals exhibiting high adhesion on substrate such as glass and plastic are used, e.g. aluminium (Al) and chromium (Cr). On the other hand, the source/drain contacts are usually made of metals such as gold (Au). Gold is widely used owing to its high work function, air stability and conductivity [44]. Polyaniline (PANI) conducting polymer is

also an optional material to make gate electrodes and the source and drain contacts. To achieve good charge carrier transport, the material used for source/drain contacts should provide a low interface barrier with the organic semiconductor [35].

2.4.2 Organic semiconductors

The organic semiconductors can be divided into polymers and small molecules. Generally, the small molecules are better in forming polycrystalline films and several researchers reported higher field-effect mobility values when compared to polymer semiconductors [45-46]. Recently OTFTs based on diketopyrrolopyrrole (DPP) polymers showed mobilities similar to those of small molecules, as a result of careful side-chain engineering [47].

2.4.2.1 Organic polymers

One of the commonly used organic semiconducting polymers is poly(3-hexylthiophene) (P3HT). An engineered polythiophene with molecules able to self-organize into crystalline lamella and extended π-conjugation called regio-regular P3HT produced higher mobility values than the regio-random P3HT. Nevertheless, several studies indicated that interconnection between the individual lamellar domains, the degree of regio-regularity and the molecular weight could be other factors to account for such mobility in regio-regular P3HT. Due to the reduction in the ionization potential caused by the large extent of the π-conjugation, the un-encapsulated P3HT showed poor oxidation resistance and instable behaviour. Therefore, more stable polythiophene derivatives such as poly(3,3‴-didode-cylquaterthiophene), PQT-12 and poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3, 2-b]thiophene pBTTT were developed with the latter exhibiting excellent stability and high mobility [45,47]. Other polymer options for OTFTs are: polytriarylamines (PTAA), regio-regular PQTs and poly(9,9-din-octylfluorene-alt-benzothiadiazole) (F8BT) [48]. For n-type transport

in OTFTs, some examples are poly(benzimidazobenzophenanthroline) (BBL) and selenophene containing polymer (PNBS) [47].

2.4.2.2 Small-molecule organic semiconductors

Small-molecule organic semiconductors can self-organise into well-ordered polycrystalline films. Some of the widely used and studied small-molecule organic semiconductors are: rubrene, pentacene, [1]benzothieno[3,2-b][1]benzothiophene (BTBT), dinaphtho[2,3-b:2′,3″-f]thieno[3,2-b]thiophene (DNTT) and their derivatives [47-48], and phenacenes. Although pentacene (consists of five linearly-arranged benzene rings) exhibits good mobility resulting from its crystalline structure and the insignificant impediment caused by the grain boundaries, it suffers from environmental degradation (oxidation) due to its weak air stability. On the other hand, in DNTT the middle benzene ring is replaced by two thiophene rings, leading to p-type transistor with better air stability and strong intrinsic resistance against oxidation [49], while maintaining carrier mobility similar to that of pentacene [45]. Additionally, DNTT is more stable because it has low-lying HOMO level and larger HOMO-LUMO energy gap (i.e. larger ionisation potential) [47,50]. Nevertheless, encapsulation of pentacene has shown to improve the mobility degradation induced from air [49]. A comparison between OTFTs based on DNTT and its alkyl (C_{10}-DNTT) and phenyl (DPh-DNTT) derivatives and pentacene was also presented [26]. The results showed that OTFTs based on DNTT and its derivatives exhibit higher mobility values and lower contact resistance compared to pentacene. For low-voltage operation the field-effect mobility was found to be 0.68 cm^2/Vs for DPh-DNTT and 0.24 cm^2/Vs for pentacene. Such high DPh-DNTT mobility resulted from the very low contact resistance (0.24 kΩcm) compared to the contact resistance (1.4 kΩcm) in pentacene transistors. In addition, the transistors based on

DNTT-derivatives showed higher filed-effect mobilities compared to DNTT transistors due to the enhancement of the charge transport properties that these derivatives provide [26].

2.4.3 Gate dielectric materials

To obtain low-voltage operation and thus low power consumption, materials with high relative permittivity (i.e. dielectric constant) can be used [51] because the capacitance of such dielectric materials is large. The capacitance of the gate dielectric determines the operating voltage of the transistor, which in turn depends on the thickness and dielectric constant of the gate dielectric material. The fact that the transistor channel formation is located near the gate dielectric interface, the properties of the gate dielectric layer, whether electrical, mechanical or chemical, influence the channel [52]. The two main categories of gate dielectrics are: single layer or multi-layer, as shown in Figure 2.4.

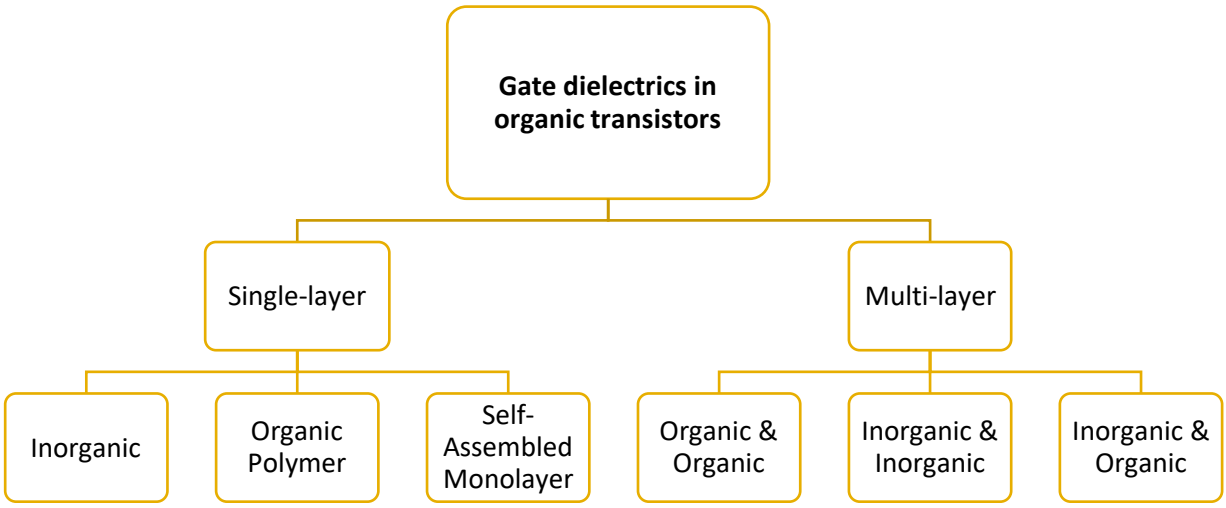

Figure 2.4: Gate dielectrics in OTFTs.

2.4.3.1 Single-layer gate dielectrics

Inorganic dielectrics:

Metal oxides are commonly used as inorganic gate dielectric layers, while many of them offer high relative permittivity. Examples are silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), La_2O_3, CeO_2, Pr_2O_3, Nd_2O_3[53], TiO_2, HfO_2, ZrO_2 [54] and Ta_2O_5 [55].

However, these high-permittivity metal-oxides usually exhibit a smaller band gap that results in larger leakage currents through the dielectric layer. Some other metal oxidises such as HfO_2 and ZrO_2 form polycrystalline structures at relatively low temperature, leading to the formation of grain boundaries and degradation of their dielectric performance. Al_2O_3 has a moderate-*k* value, but it is a good candidate because of its excellent thermal stability and a large band gap [54]. In addition, good film quality means that a thin layer of aluminium oxide is sufficient to minimise the gate leakage current, while being prepared using low-cost deposition methods such as anodization [52].

Organic polymers:

One of the advantages of using single-layer organic polymers as dielectrics is that they can be prepared by low-cost fabrication techniques such as solution deposition. However, low gate-dielectric capacitance offered by polymer dielectrics limits the device performance and typically leads to higher operation voltage and higher leakage current [44]. Commonly used polymer dielectrics are polyimide (PI), polyvinyl phenol (PVP), polyvinyl alcohol (PVA), and polymethyl methacrylate (PMMA) [53].

Self-assembled monolayers:

Self-assembled monolayers (SAMs) can provide high quality, insulating, ultra-thin layer that can lead to OTFTs with low operating voltages. Examples include carboxyl-terminated monolayer, alkyl phosphonic acids and fluoroalkylphosphonic acids [52].

2.4.3.2 Multi-layer gate dielectrics

To develop the gate dielectric layer, several approaches have been attempted including combining two types of gate dielectrics, often called bi-layer or multi-layer. Possible combinations are two inorganic dielectrics, two organic dielectrics (e.g. SAM and PVP), and finally inorganic with organic dielectrics. When inorganic metal oxide is treated with organic self-assembled monolayer, low-surface energy dielectric is obtained leading to an improved growth of the organic semiconductor and improved field-effect mobility of the organic transistor. A three-dimensional growth is obtained when small-molecule organic semiconductor is grown on a low-energy (bi-layer dielectric) surface. Three-dimensional growth leads to denser films where the gaps between the large grains are filled with smaller grains. Consequently, transistors with high mobility are produced. Otherwise, two-dimensional growth typically occurs when small-molecule organic semiconductor is deposited on high-energy (bare inorganic dielectric) surface. Two-dimensional growth leads to large grain formation with the gaps between the grains and thus transistors with lower field-effect mobility are seen [45].

2.5. OTFT operation

The unipolar organic transistor has three electrodes called gate (G) source (S) and drain (D). It operates in accumulation mode as a result of the organic semiconductors (carbon-

based conjugated organic molecules) being ‘intrinsic semiconductors’ in their nature [45]. For p-type OTFTs, negative voltages are applied at the transistor terminals to produce the accumulation of positive charges, i.e. holes.

The gate voltage V_G modulates the channel conductivity and thus controls the drain current. In p-type OTFTs, a negative voltage on the gate will attract positive charges (holes) to the interface between the organic semiconductor and the gate dielectric, thus forming a p-type conductive channel at the interface. To cause the accumulated charge carriers to flow between the source and drain, a negative drain voltage V_D should be applied because holes conventionally flow in the direction of the applied electric field. Therefore, applying a negative voltage at the drain electrode V_D will cause the flow of holes, i.e. drain current I_D. If V_D is increased, I_D will increase linearly (linear regime). When $|V_D|$ reaches $|V_G| - |V_T|$, where V_T is the threshold voltage, a channel pinch-off occurs near the drain and the drain current remains constant for higher V_D (saturation regime). Figure 2.5 summaries these transistor states [47].

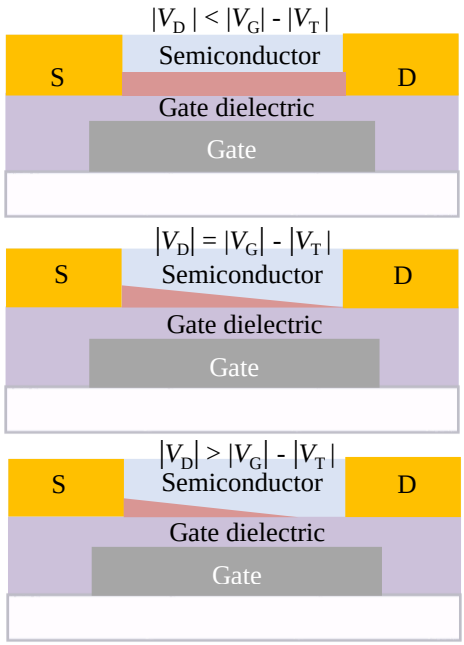

Figure 2.5: Transistor channel formation with changing V_D.

Similarly, in n-type organic OTFTs, positive voltage is applied at the gate electrode thus negative charges (electrons) accumulate at the interface of the semiconductor and the gate dielectric, i.e. n-channel is formed at the interface. A positive voltage V_D should be applied at the drain because electrons flow against the applied electric field and this causes current to flow from the drain to the source.

Semiconductor materials in comparison to metals have an energy gap between the valence and conduction bands. In organic semiconductor they are referred to as the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) respectively. The existence and the size of the bandgap determines the conducting properties of the material.

The type of channel formed in OTFT depends on the organic semiconductor, more precisely on the position of its LUMO and HOMO with respect to the Fermi level of the material (metal) used for the source and drain contacts. P-channel is formed when the HOMO is 'aligned' with the Fermi level as holes are more easily injected and accumulate near the semiconductor/dielectric interface when the gate voltage is negative. In contrast, n-channel is formed when the LUMO is 'aligned' with the Fermi level as electros are more easily injected and accumulated at the interface when the applied gate voltage is positive. Figure 2.6 shows the energy scheme of p-type and n-type organic transistors.

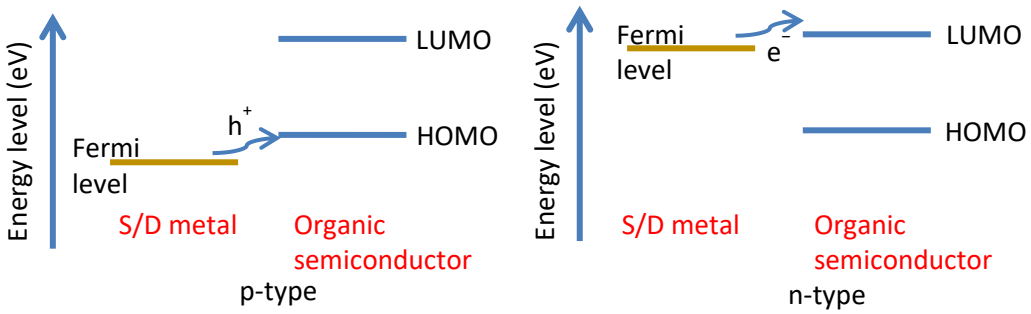

Figure 2.6: Energy scheme of p-type and n-type organic transistor.

However, due to external factors such as the formation of dipoles at the interface of the semiconductor and the contacts and the charge transfer [45], this prediction of the type of the OTFT might not be fully accurate.

2.6. OTFT operation regimes

2.6.1 Linear regime

To obtain the current-voltage relationships in OTFT, the first step is to define the charge density $\frac{dq}{dA} = \frac{dq}{Wdx}$ at a strip/segment of the dielectric layer of the OTFT which can be given as [56]:

$$dq = C_{diel}[V_{GS} - V_T - V(x)]Wdx \tag{2.3}$$

where C_{diel} is the dielectric capacitance, V_{GS} is the gate-to-source voltage, V_T is the threshold voltage, $V(x)$ is the voltage potential at point x of the channel, W and dx are the channel width and a segment of the channel length respectively. Also, by definition the current is the flow of charge, i.e.:

$$I_D = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt} \tag{2.4}$$

where the expression $\frac{dx}{dt}$ is simply the mean speed (change of distance over time) and in this case it is assumed that the velocity of the charge carriers is uniform (constant mobility) which can also be expressed as:

$$v = \frac{dx}{dt} = \mu E_x \tag{2.5}$$

where μ is the charge carrier mobility and E_x is the electric-field. Furthermore, E_x is given by:

$$E_x = \frac{dV}{dx} \tag{2.6}$$

where V is the electrode voltage.

Substituting (2.3) and (2.5) into (2.4) yields the following expression for I_D:

$$I_D = C_{diel}[V_{GS} - V_T - V(x)]W\mu\frac{dV}{dx} \tag{2.7}$$

Integrating equation (2.7) over the channel length (L) on the left hand side and over the potential variation (V_{DS}) along the channel on the right hand side, i.e. integrating from source to drain (x from 0 to L and $V_{(x)}$ from $V(0) = 0$ and $V(L) = V_{DS}$), gives:

$$\int_0^L I_D dx = \int_0^{V_{DS}} C_{diel}[V_{GS} - V_T - V(x)]W\mu\, dV$$

$$I_D L = W\mu C_{diel}\left[(V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

$$I_D = \frac{W}{L}\mu C_{diel}\left[(V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right] \tag{2.8}$$

The above equation represents the drain current in the linear regime at which the drain-to-source voltage is less than the difference between the gate-to-source voltage and the threshold voltage, namely $|V_{DS}| < |V_{GS}| - |V_T|$. At low values of V_{DS} the term $\frac{{V_{DS}}^2}{2}$ is usually very small and can be neglected. Thus equation (2.8) becomes:

$$I_D = \frac{W}{L}\mu C_{diel}(V_{GS} - V_T)V_{DS} \tag{2.9}$$

Rearranging the equation (2.9) gives the field-effect mobility in the linear regime [56], μ_{lin} as:

$$\mu_{lin} = \frac{L}{WC_{diel}V_{DS}}\frac{\partial I_D}{\partial V_{GS}} \tag{2.10}$$

2.6.2 Saturation regime

The saturation operation of the transistor occurs when the drain-to-source voltage is greater than the difference between the gate-to-source voltage and the threshold voltage, namely $|V_{DS}| > |V_{GS}| - |V_T|$. To find the drain current in saturation regime V_{DS} is substituted by $V_{GS} - V_T$ in equation (2.8), leading to:

$$I_D = \frac{W}{2L}\mu C_{diel}(V_{GS} - V_T)^2 \tag{2.11}$$

Similarly, by rearranging (2.11) for field-effect mobility in saturation regime [56], μ_{sat} is:

$$\mu_{sat} = \frac{2L}{WC_{diel}}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \tag{2.12}$$

2.6.3 Subthreshold regime

This regime is defined as the region where gate-to-source V_{GS} is less than threshold voltage V_T (i.e. $|V_{GS}| < |V_T|$). The drain current in this region is increasing exponentially with V_{GS}. The subthreshold slope S is used to assess the transistor's ability to transit quickly from off-state to on-state and vice versa. The steeper the subthreshold slope, the faster the transition to the on-state which is particularly important for digital applications.

The transistor characteristics and figures describing the above regimes are available in the next chapter (Chapter 3).

2.7. Transistor parameters

Transistor performance is evaluated by several parameters such as field-effect mobility, on/off current ratio, threshold voltage, subthreshold slope, and transconductance. Their extraction method will be described in Chapter 3 Section 3.5.

The carrier mobility μ is defined as "the average charge carrier drift velocity per unit electric filed" [51]. It represents how easily charge carriers move from one molecule to adjacent molecule under the effect of electric filed. High mobility values are preferable for achieving better transistor performance and faster switching. The mobility of the transistor is mainly controlled by the choice of the organic semiconductor material but also by the gate voltage, channel length, the interface between the semiconductor and the gate dielectric, the microstructure of the organic semiconductor, and the morphology of the films. Simply put, the on-state current I_{ON} (on-current) is the maximum drain current value in the on-state of the transistor and the off-state current I_{OFF} (off-current) is the minimum drain current value in the off-state of the transistor. On/off current ratio I_{ON}/I_{OFF} is the ratio between the on- and the off-currents and for digital application it is required to be of a large value. It is inversely proportional to the length of the channel and the semiconductor thickness.

Threshold voltage, V_T, is the minimum gate voltage needed to achieve considerable drain current. For good transistor performance it is desirable to have low threshold voltage value because this means that the device is able to switch more rapidly [45, 51]. In addition, a low V_T value results in low-voltage operation, thus useful for low-power consumption applications. The subthreshold slope or the subthreshold swing, *S*, is a quantity used to evaluate the transition of the transistor from the off- to the on-state and it is usually given in mV/decade. Ideally, for faster transition the *S* value should be low (i.e. steep transition). Finally, transconductance is an important figure of merit to assess the transistor a.c. performance and higher value is required for high frequency applications.

2.8. Charge transport theories

Although many studies have been dedicated to understanding the charge carrier transport in organic materials, it is yet to be fully understood because many factors, such as

surface roughness, dipole formation, film disorder, chemical impurity and structural defects [37] affect the charge transport. In addition, depending on the OTFT structure and the organic semiconductor used, the carrier mobility ranges from ~10^{-3} up to 6 $cm^2/V \cdot s$ [45] and this cannot be explained with a single model. Nevertheless, several models were proposed to elaborate the charge carrier transport. Among them there are two models that address two cases of molecular ordering and they are applicable to the highly ordered molecular crystals (polycrystalline films) and the disordered (amorphous films) organic semiconductors [38]. The multi-trapping and release (MRT) model is used to address the former case while variable range hopping (VRH) is for the latter. They are both are briefly explained next [45, 57-58].

2.8.1 Multiple trapping and release

MRT is usually applied to small-molecule organic semiconductors which tend to readily form a polycrystalline film when deposited by vacuum evaporation. Here, effective charge-carrier transfer is facilitated due to the delocalised orbitals that are partially overlapping as a result of the regular molecular arrangement. The extended state band where the charge transport occurs and localized states/traps where most of the charge carriers are trapped are the main assumptions in this model. Simply put, the charge carriers (the trapped ones) are temporarily released to the extended state band for transport and they do not move directly from one trapped state to another. This trapping and release occurs multiple times for each carrier. Localized states/traps are associated with the presence of structural/chemical defects, grain boundaries and impurities in the channel. On the other hand, temperature, the gate-voltage bias and energy between the localized states/traps and the extended state band are factors that control the number of the carriers available for transport as well as the distribution of the carriers between the transport and trapping levels [45, 57-58].

2.8.2 Variable-range hopping

Since the inter-molecular bonding between the organic molecules is accomplished through relatively weak van der Waals interactions, the electronic wave functions are localized to a finite number of molecules rather than extending over the whole volume of the organic solid. For amorphous semiconductors that exhibit disordered molecular arrangement, the charge carriers are trapped in the localized states called hopping sites. When the charge carriers are thermally activated, they jump/hop between these sites, either with high activation energy over smaller distance or with low activation energy over longer distance. Hopping distance and energy distribution of the hopping sites determine how frequently a hopping event can occur. The tunnelling of the charge carriers through hopping sites depends on the overlap of the wave functions of the localized states. The ease with which charge carriers transport (mobility) also increases with increasing temperature, gate-voltage and good molecular arrangement [45, 57-58].

2.9. State-of-the-art low-voltage OTFTs

The increasing interest in organic transistors over the last decades has led to manufacture of higher performance transistors and encouraged the search for new materials to improve the device performance. Different approaches were taken to realise this. Depending on the application though, stability, high mobility and high speed were often desired. For instance, the field-effect mobility was increased by synthesising new organic semiconducting materials. Furthermore, the stability of the OTFT is an important aspect for fully developing OTFTs suitable for commercial use, hence numerous studies are addressing the environmental (e.g. oxidization and moisture [59]), operational and thermal stabilities of the OTFT. The operational stability is in term of the effect of the bias voltage stress on the

device, as it was reported that the gate voltage would have significant effect on the device degradation with a partial degradation recovery after the bias voltage is removed [60].

One of the proposed solutions to improve the OTFT environmental/thermal stability is the use of organic semiconductors with modified side chains [61]. For example, the use of phenyl groups on DNTT (DPh-DNTT) [62] led to a good transistor thermal stability and only a very small change in the transistor mobility up to 250 °C [63]. Similarly, the use of pentacene derivative 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) enhanced the thermal stability of the transistor, although the material is still prone to photochemical degradation [64].

The DNTT which was used in this research as organic semiconductor layer was reported to be of high environment stability. A study has reported that OTFTs based on DNTT survived different environmental condition including storage under normal laboratory air [64], while another suggested that they exhibit a thermally stable behaviour suitable for medical sterilization conditions. Finally, DNTT is commercially available [65].

In addition, great effort was directed to study and investigate the gate dielectric layer, especially to obtain low-voltage transistor operation. Here, some of the previously reported low-voltage OTFTs and the different techniques used to achieve them will be presented.

Low-voltage operation is an essential requirement for flexible/wearable applications. The capacitance of the gate dielectric controls the voltage operation. As shown in equation (2.1) for low-voltage operation the capacitance should be high. Also, according to equation (2.2) materials with high-dielectric constant (k or ε_r) and/or small thickness of the dielectric layer will result in high capacitance value. However, issues may arise, e.g. reducing the thickness may cause a high leakage current and therefore poor transistor performance.

In fact, it might not be as straightforward as already explained. The number of accumulated charge carriers at the interface of the dielectric and the semiconductor increases

with the use of high-*k* dielectric which may lead to increase in the mobility (known as bulk effect). On the other hand, the highly polar high-*k* metal oxide (inorganic dielectric) may affect the charge transfer and reduce the mobility of the OTFTs. Hence, a trade-off exists [66].

To address this trade-off, a possible solution is the use of hybrid dielectrics consisting of high-k material coated with a low-k material [66]. In [66] it was demonstrated that OTFT based on C_8-BTBT with metal oxide gate dielectric treated by low-*k* polymers, exhibited improved transistor performance. The Y_2O_3/polymethyl methacrylate (PMMA) bi-layer had the best low-voltage operation improvement with $V_T = -1.4$ V which was reduced from $V_T = -3.8$ V for bare-Y_2O_3 due to the reduced dipolar disorder and removal of the defects at the interface.

The addition of SAM layer to the gate dielectric layer enhances the performance of the OTFT because this leads to improvement in the semiconductor morphology and thus lowering the injection barrier at the interface of the source/drain metal and the semiconductor and/or reduction in trap densities and charge scattering at the interface [34]. Since the threshold voltage depends on the quality of the interface between the dielectric and the semiconductor, low threshold voltage can be achieved with smoother (low surface roughness) surface of the gate dielectric as the probability of trapped charges at such interface will be reduced [53]. It was reported that the use of extra organic layer provides a smother surface to the dielectric layer [53] and reduces trapping at the interface [67], thus leading to better transistor performance.

In [53], pentacene based OTFT with a bi-layer consisting of neodymium oxide (Nd_2O_3) and crosslinked polyvinyl alcohol (PVA) with ammonium dichromate (ADC) was implemented. ADC was used to reduce the hydrophilicity of PVA which otherwise would lead to degradation resultant from the moisture absorption. This provided low-voltage

operation with V_T = –2.8 V. The surface roughness of such a bi-layer was also improved when compared to bare Nd_2O_3.

Similarly in [44], pentacene-based OTFTs with octadecylphosphonic acid (ODPA) self-assembled monolayer and Al_2O_y/TiO_x (also known as ATO) dielectric achieved excellent low-voltage operation with V_T = –0.4 V and mobility of 1.5 $cm^2/V{\cdot}s$. Such dielectric exhibited low-surface energy due to its high hydrophobicity, low leakage current, and high capacitance, thus low-voltage transistor operation was obtained.

It was reported in [55] that to improve the morphology of the interface between the organic semiconductor and the gate dielectric, hafnium oxide (HfO_x) (high-*k* metal-oxide) was passivated with cyclic olefin copolymer COC which is a hydroxyl-free polymer. Overall, the device performance was improved in terms of low-leakage current, higher mobility and less hysteresis in the transistor characteristics, since the trap density was reduced after the COC passivation.

A combination of two inorganic dielectrics into a bi-layer can also provide low-voltage transistor operation by increasing the gate dielectric capacitance. This was demonstrated in [54] where low-voltage operation of –1.5 V with V_T = –0.5 V was reported for copper phthalocyanine (CuPc) OTFTs with gate dielectric bi-layer of Al_2O_y and TiO_x. The dielectric layer exhibited smooth surface and high capacitance of 250 nF/cm^2; when compared to similar transistors with 300 nm of SiO_2, significant improvement in the threshold voltage was realised.

In [68] a novel approach was presented using triple-laminated thin film of $Eu(tta)_3L$/PVA/OTS (high-*k* lanthanide complex of $Eu(tta)_3L$ (tta=2-thenoyltrifluoro-acetonate, L=4,5-pinene bipyridine), polyvinyl alcohol (PVA), octadecyltrichlorosilane (OTS)) as gate dielectric. The OTFT was based on pentacene and achieved good electrical performance with V_T = –0.9 V and mobility of 0.17 $cm^2/V{\cdot}s$.

The transistor in this study follows similar approach to the ones reported above, i.e. the use of an ultra-thin bi-layer consisting of an inorganic, medium-*k* AlO_x and SAM of octadecyl phosphonic acid ($C_{18}PA$) with total thickness of about 11 to 15 nm, resulting in high capacitance value of ~0.4 to 0.3 μF/cm^2 and leakage current of ~ 10^{-8} A/cm^2 [69].

In addition to low-voltage operation the transistor transconductance is also important parameter for wearable/portable application. It is defined by the modulation of the drain current that results from the gate-source voltage modulation:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.13}$$

Consequently, the derivation of equations (2.9 and 2.11) with respect to V_{GS} gives the transconductance in linear and saturation regimes respectively:

$$g_{m\,lin} = \frac{W}{L}\mu C_{diel} V_{DS} \tag{2.14}$$

$$g_{m\,sat} = \frac{W}{2L}\mu C_{diel}(2V_{GS} - 2V_T) = \frac{W}{L}\mu C_{diel}(V_{GS} - V_T) \tag{2.15}$$

where W is the channel width, L is the channel length, μ is the field-effect mobility, C_{diel} is the gate dielectric capacitance per unit area, V_{GS} is the gate-to-source voltage, and V_T is the threshold voltage.

As seen from the equations (2.14 and 2.15), the transconductance is directly proportional to the increase of one and/or all (taking *W/L* ratio as whole) variables on the right-hand side of the equations. Since the goal is to keep the low-voltage transistor operation, i.e. near-zero V_T, the ($V_{GS} - V_T$) term is automatically optimised. Techniques on increasing C_{diel} were explained at the beginning of this section (Section 2.9). Optimising the mobility as mentioned previously, depends on the organic semiconductor material primarily and so the morphology and type of the grown thin film, in addition to quality of the interface

between the dielectric and the semiconductor for optimised charge carrier transport. If C_{diel} and μ have been maximised, increasing *W/L* ratio remains as the last option for increasing g_m.

This, in fact, is one of the studied approaches to achieve high transconductance. More precisely, the focus has been on reducing *L* and fabricating short-channel OTFTs. The decrease of *L* to below 1 μm is challenging because the source/drain contact resistance has to be carefully addressed in the short-channel OTFTs [47]. Nevertheless, solutions were proposed to reduce the contact resistance in OTFTs with nanoscale channel length [70].

Increasing the *W* can also be employed to increase the transistor transconductance. Without increasing the overall area of the transistor, the multi-finger contact structure is a promising solution to provide high *W/L* ratio, as will be discussed in Chapter 4.

Chapter 3

Methodology

This chapter describes the fabrication of organic thin-film transistors and metal-insulator-metal (MIM) structures in addition to the measurements performed on the transistors to evaluate their electrical performance. The fabrication procedure is explained in Section 3.1. The execution of different measurements on the transistor is described in Section 3.2, whereas the related measurements preformed on MIM structures are shown in Section 3.3. Section 3.4 outlines the setup for a.c. measurements used to assess the a.c. performance of the transistors. Finally, in Section 3.5 the extraction of the essential transistor electrical parameters is illustrated.

3.1. Fabrication of OTFTs and MIM structures

Figure 3.1 shows the standard steps applied during the fabrication of organic thin-film transistors by thermal evaporation in vacuum. Similar procedure is described in [71-72], where the $C_{18}PA$ monolayer has been optimised in terms of evaporation rate, deposition temperature and the post-evaporation desorption/annealing time.

The fabrication process is as follows: firstly, the substrate – glass (Ossila, U.K.) or flexible PEN (Optfine PQA1, DuPont Teijin) – was cleaned in boiling deionized water bath placed in ultrasonic cleaner for 60 minutes and then dried by nitrogen gun. Alternatively, acetone and isopropanol were used to clean the substrates.

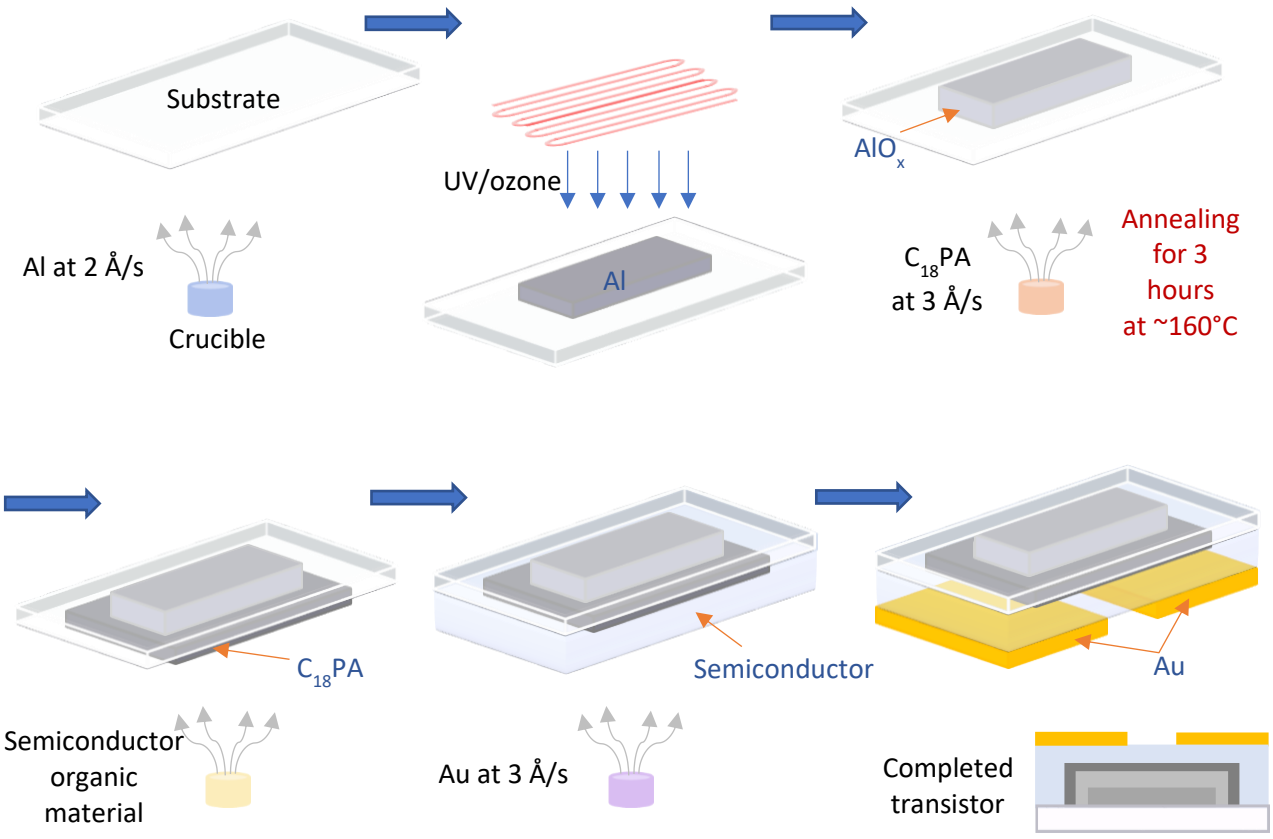

Figure 3.1: Summary of the fabrication steps for OTFT.

Next, a substrate holder was used to load the glass/PEN substrates together with shadow masks for the gate electrode evaporation. All evaporations were performed in the Mini-SPECTROS (K. J. Lesker, U.K.) evaporation chamber placed inside a glove box filled with nitrogen (Jacomex, France) to provide an oxygen-free and humidity-free environment. The chamber base pressure was around 10^{-7} mBar before each thermal evaporation. The source material (powder or pellet) to be deposited by thermal evaporation was loaded in a designated crucible.

For the gate electrode, a 30-nm-thick aluminium was deposited onto the substrate at a rate of about 2 Å/s at room temperature. Such evaporation rate was previously shown to result in a lower surface roughness compared to lower evaporation rate of Al [71]. Afterwards, a 40-nm-thick gold (Au) was evaporated on the top segment of the gate contacts at a rate of 3 Å/s to prevent the oxidation of the gate electrodes in the next step. The exposed/uncoated part of the aluminium gates was oxidised on the surface to form thin AlO_x layer, the first part of the gate dielectric.

Next, the gate dielectric layer preparation consisted of AlO_x and SAM ($C_{18}PA$, 97% purity Strem Chemicals, USA) formation. The thin layer of AlO_x was prepared using UV/ozone cleaner (UVOCS, USA) where an ultraviolet light with two dominant wavelengths was emitted by low-pressure mercury lamp. A 184.9 nm wavelength decomposes oxygen present in the air to create ozone (O_3) and a 253.7 nm wavelength can decompose ozone, thus creating a highly-reactive atomic oxygen (normal oxygen is stable in the form of O_2) needed for the surface oxidation of the Al gates [73]. Consequently, the Al gates exposed to UV/ozone have thin AlO_x layer formed on their surface. The UV/ozone cleaner was enclosed under a Hepa filter to prevent the contamination of the oxidizing surface and the UV/ozone oxidation takes 1 hour. If thicker AlO_x layer is required, the Al evaporation and UV/ozone

exposure are repeated. In this case, however, a very thin layer of aluminium is used (15 or 12 Å) requiring slower evaporation rate of about 0.3 Å/s.

Another shadow mask for SAM layer was used. After reaching the base pressure ~20 nm of $C_{18}PA$ was deposited at room temperature at the rate of about 3 Å/s. This rate has previously led to low-voltage, hysteresis-free transistors based on DNTT [72]. Afterwards, the substrate temperature was raised to ~160°C and the samples were annealed for 3 hours to remove all physisorbed $C_{18}PA$ molecules. After the annealing only the first layer of $C_{18}PA$ molecules that are chemically bonded to AlO_x remains, leading to the monolayer formation [69]. The next transistor layer was the organic semiconductor and in this study either DNTT or [n]phenacene were used. Different shadow masks were used for the deposition of the organic semiconductor. In the case of DNTT, ~ 20 nm of DNTT was deposited at room temperature at a rate of 0.5 Å/s. Similar evaporation rate, yet thicker layers, were used for [n]phenacenes. Finally, the last shadow mask for the source/drain contacts was used to evaporate a 50-nm-thick Au layer at a rate of ~3 Å/s to complete the transistor. Altogether five different shadow masks were used and care was taken to ensure a proper alignment of each mask to the previous layer.

For the MIM structures, i.e. the capacitors, the fabrication was done alongside the OTFTs. Exactly the same procedure was applied; however, the capacitors were completely shielded during the deposition of the semiconductor layer.

3.2. OTFT measurements

Agilent B1500A semiconductor device analyser was used to conduct various measurements on the OTFTs. The measurements of the transistors and corresponding metal-insulator-metal structures were performed under dark ambient conditions. All measurements were for p-type OTFTs, therefore negative voltages were applied to the transistor terminals to

bring the transistor to its on-state (to turn the transistor on). The transfer and output characteristics of the OTFTs were measured in a sweep mode.

3.2.1 Output characteristics (I_D-V_{DS})

The output characteristic is a plot of I_D against V_{DS} for several fixed values of V_{GS}. An example of such measurement for a low-voltage DNTT transistor is shown in Figure 3.2 where I_D is measured for V_{DS} ranging from 0 to –2 V and V_{GS} is stepped from –0.5 to –2 V with a step of –0.25 V. The output characteristics capture the transistor performance in both linear (i.e. $|V_{DS}| < |V_{GS}| - |V_T|$) and saturation regimes ($|V_{DS}| > |V_{GS}| - |V_T|$). For small values of V_{DS} a linear raise in I_D is observed, whereas for larger V_{DS} the drain current I_D saturates.

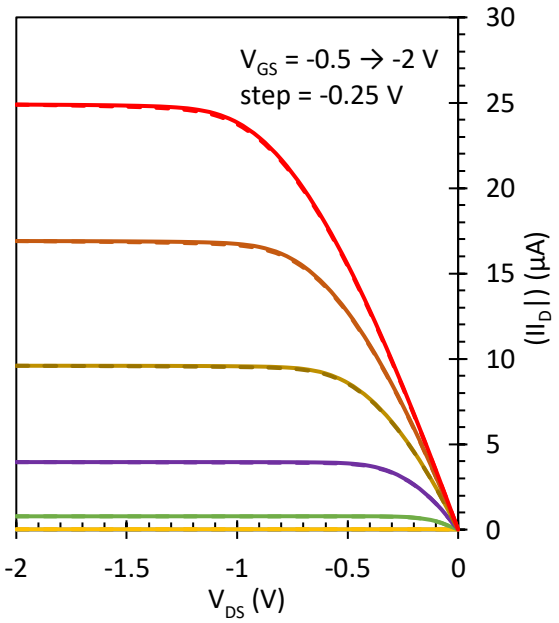

Figure 3.2: Transistor output characteristics; hysteresis measurements from 0 to -2 V and back.

3.2.2 Transfer characteristics (I_D-V_{GS})

Transfer characteristic of the transistor is the plot of measured drain current (I_D) as a function of gate-to-source voltage (V_{GS}) for a fixed value of drain-to-source voltage (V_{DS}). For low-voltage transistors, small values of V_{GS}/V_{DS} are sufficient to turn the OTFT on,

therefore V_{GS} is varied from 0 to −2 V for DNTT OTFTs and up to −6 V for [n]phenacene OTFTs (see Chapter 5). To achieve linear regime operation, V_{DS} was set to −0.1 V, while it was set to −2 V to place the DNTT transistor into saturation operation. Figure 3.3 shows an example of transfer characteristics of a p-type low-voltage OTFT based on DNTT.

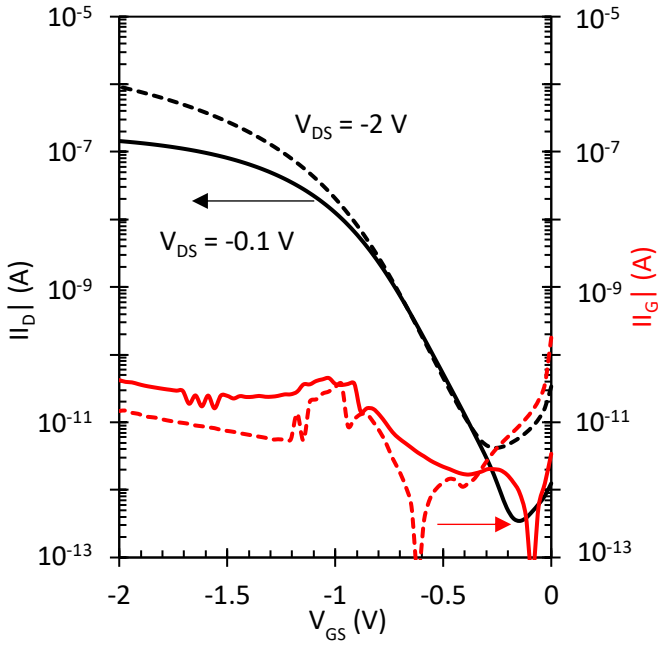

Figure 3.3: Transistor transfer characteristics; the solid line corresponds to linear regime, the dashed line to the saturation regime.

The measurement of the transistor transfer characteristics is important for assessing the transistor performance, as most of the d.c. electrical parameters such as filed-effect mobility, threshold voltage, subthreshold slope, on-state current, off-state current, on/off current ratio, d.c. transconductance and gate leakage current are extracted from it. In addition, observing the changes in the transfer characteristics after prolonged and/or high voltage application on the transistor terminals will give an insight into the transistor stability. Any recovery of the transistor may also be assessed by measuring and analysing the transfer characteristics before and after a period of time. More details on how to extract the transistor parameters are explained in Section 3.5.

3.2.3 Hysteresis measurements

Hysteresis measurements are achieved by sweeping V_{GS} (transfer characteristics) or V_{DS} (output characteristics) in both directions, i.e. measuring from 0 to −2 V and back, for example. A hysteresis-free behaviour is reported when both measurements are the same regardless of the voltage sweeping direction. Figure 3.2 shows an example of hysteresis measurement for output characteristics. Ideally, hysteresis-free behaviour is desired.

3.3. MIM structure: measurements

Measurements of the metal-insulator-metal structures were also performed with Agilent B1500A semiconductor analyser equipped with a capacitance module. These measurements are: capacitance as a function of frequency (*C-f*) and current as a function of voltage (*I-V*). The former measurement provides information about the gate dielectric capacitance. Since the gate dielectric used here consists of C_{18}PA and AlO_x, the thickness of the C_{18}PA can be estimated also by knowing the total gate dielectric capacitance. The latter measurement is used to assess the leakage current density of the gate dielectric layer [72].

3.3.1 Capacitance measurement (*C-f*)

The capacitance of the MIM structure as a function of frequency from 1 kHz to 1 MHz was measured using Agilent B1500A semiconductor device analyser equipped with a capacitance module. In this thesis the capacitance value is extracted at 10 kHz. Figure 3.4 shows an example of this measurement.

The gate dielectric capacitance is expressed in F/cm$_2$, i.e. capacitance per unit area. The overlap area of the capacitor electrodes determines the capacitor area. This area is measured to allow the calculation of the capacitance per unit area. For each transistor set several MIM structures were measured and the mean capacitance value was calculated.

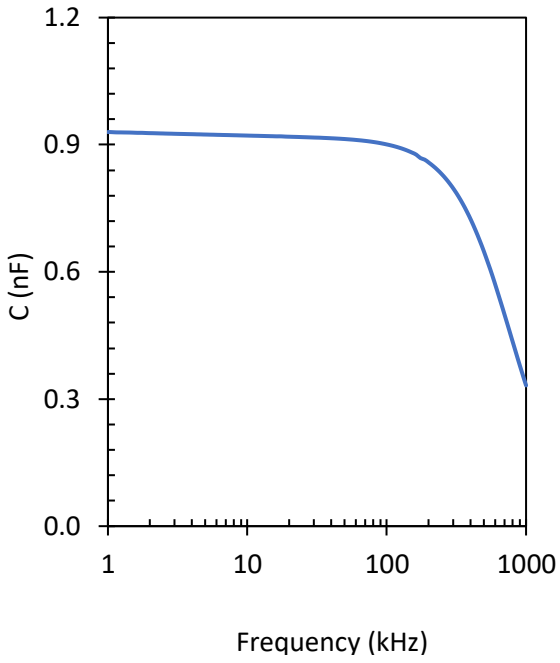

Figure 3.4: MIM capacitance as a function of frequency.

The thickness of octadecyl phosphonic acid monolayer ($C_{18}PA$) which is part of the bi-layer gate dielectric can be estimated as follows. For example, for the MIM structure in Chapter 4, the measured capacitance of bare AlO_x (without phosphonic acid monolayer) is 7.78×10^{-7} F/cm^2. From there the AlO_x thickness can be calculated as:

$$d = \frac{\varepsilon_r \varepsilon_o}{C} \tag{3.1}$$

where d is the thickness, ε_r the AlO_x relative permittivity of ~7 [74] and ε_o is the vacuum permittivity of 8.85×10^{-14} F·cm^{-1}. Substituting these values results in $d = 7.96\times10^{-7}$ cm $\cong$ 8 nm. The total bi-layer capacitance is given by:

$$1/C_{total} = 1/C_{AlO_x} + 1/C_{C_{18}PA} \tag{3.2}$$

where $C_{total} = 4.23\times10^{-7}$ F/cm^2 is the capacitance of the $AlO_x/C_{18}PA$ bi-layer, C_{AlO_x} is the capacitance of the aluminium oxide and C_{C18PA} is the capacitance of octadecyl phosphonic

acid monolayer. Rearranging (3.2) and substituting the values results in $C_{18}PA$ capacitance of 9.27×10^{-7} F/cm^2. Finally, using (3.1) and ε_r = 2.1 for $C_{18}PA$ [74], the thickness d of the octadecyl phosphonic acid was calculated to be 2 nm, i.e. a monolayer. This calculation and the capacitance measurements (decrease of the capacitance value after the deposition of $C_{18}PA$) proves the formation of the octadecyl phosphonic acid on the AlO_x surface with a thickness corresponding to a about a monolayer [69].

3.3.2 Leakage current density

Figure 3.5 shows a current-voltage (*I-V*) measurement on MIM structure of $AlO_x/C_{18}PA$, where the current is expressed as current density in A/cm^2. This measurement can be used to evaluate the leakage current density of the dielectric layer. As shown, the voltage is swept from 0 to 2 V and again from 0 to -2 V.

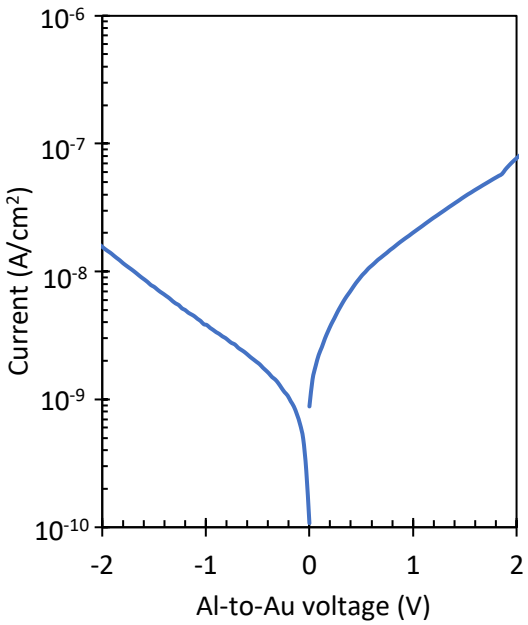

Figure 3.5: Current density as a function of voltage for MIM structure.

3.4. OTFT a.c. measurements

The a.c. measurements performed on some OTFTs used in this study (shown in Chapter 4) include a.c. transconductance, cut-off frequency, and voltage gain of a common-source transistor amplifier based on the OTFT.

The a.c. transconductance was determined by measuring the modulated drain current when a sinusoidal voltage of 0.2 peak-to-peak and an offset of –2 V was applied on the gate electrode, while –2 V d.c. voltage was applied on the drain electrode and the source electrode was grounded. The a.c. transconductance was calculated as a ratio of the measured peak-to-peak modulation in the drain current divided by the gate bias modulation, such as:

$$g_m = \frac{i_d}{v_g} \tag{3.3}$$

The maximum operation frequency (cut-off) was investigated by measuring the transconductance as a function of a.c. frequency, as shown in Figure 3.6. This was achieved by applying similar sinusoidal gate voltage as before, however the frequency of the input signal was varied from 0.5 Hz to 50 kHz. Agilent B1500A semiconductor device analyser is equipped with an arbitrary waveform generator; however, an external digital oscilloscope (Agilent DSO7052A, 500MHz) was used to capture the high frequency signals.

The final a.c. measurement conducted in this study is a voltage gain of a simple common-source voltage amplifier based on the OTFT, as shown in Figure 3.7. A resistor is added on the drain side of the transistor while the source electrode is grounded. In these measurements a sinusoidal voltage of 1 Hz was applied to the transistor gate and the modulated output voltage was measured below the resistor. The drain current and the output voltage were measured simultaneously for a range of supply voltages to allow a deeper

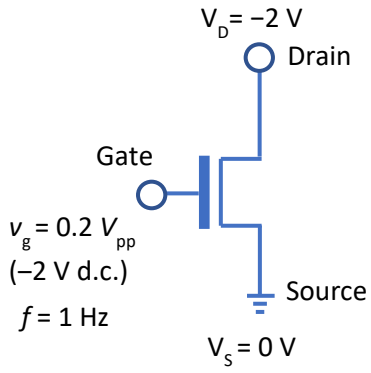

Figure 3.6: Transconductance measurement setup.

analysis of the transistor amplifier. The a.c. voltage gain was calculated by dividing the measured peak-to-peak modulation in the output voltage and the gate bias modulation of 0.2 V_{pp}, such as:

$$g_v = \frac{v_{out}}{v_g} \tag{3.4}$$

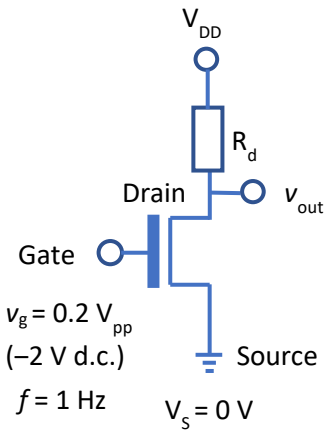

Figure 3.7: Voltage amplifier circuit.

3.5. Extraction of transistor parameters

The transistor performance is evaluated by several parameters such as mobility μ, threshold voltage V_T, subthreshold slope S, leakage current I_G, on-state current I_{ON}, off-state

current I_{OFF}, on/off current ratio I_{ON}/I_{OFF}, and transconductance G_m. These parameters were extracted from the transistor transfer characteristics in linear and saturation regime. In this section, the procedure on how to find the OTFT parameters is illustrated.

The threshold voltage V_T is extracted from the transistor transfer characteristics measurement and both linear and saturation regimes can be used. The method for extracting V_T from each regime is as follows. In the linear regime ($|V_{DS}| < |V_{GS}| - |V_T|$), the threshold voltage is extracted from the plot of I_D versus V_{GS}. The linear portion of that curve is fitted with a straight line and its intercept with the x-axis (V_{GS}) gives the threshold voltage V_T, as shown in Figure 3.8(a). This can be inferred from the transistor equation in linear regime (see equation 2.10). Similar method is used to find V_T in the saturation regime ($|V_{DS}| > |V_{GS}| - |V_T|$); however, square root of I_D against V_{GS} is plotted, as depicted in Figure 3.8(b) and dictated by the transistor equation (2.12).

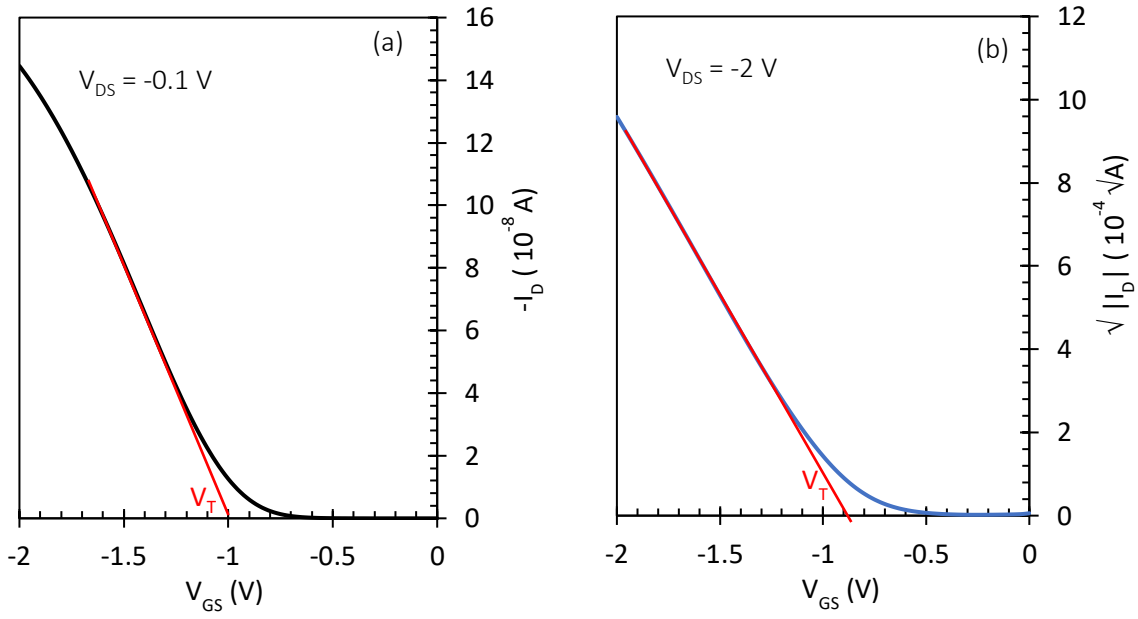

Figure 3.8: Extraction of the threshold voltage in the linear regime (a) and saturation regime (b).

The plot of I_D as a function of V_{GS} shown in Figure 3.8(a) was also used to calculate the mobility (in $cm^2/V{\cdot}s$) in the linear regime using equation (2.10), namely:

$$\mu_{lin} = \frac{L}{C_{diel} W V_{DS}} \frac{\partial I_D}{\partial V_{GS}}$$

where L is the channel length, W the channel width, C_{diel} the dielectric capacitance per unit area in F/cm^2, V_{DS} is voltage applied on the drain electrode and $\frac{\partial I_D}{\partial V_{GS}}$ is the slope of steepest segment in I_D against V_{GS} (shown in red). For mobility in the saturation regime equation (2.12) is used, namely:

$$\mu_{sat} = \frac{2L}{C_{diel} W} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2$$

where $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$ is the slope of steepest segment in the plot of the square root of I_D as a function of V_{GS} as shown in Figure 3.8(b). The steepest segment in the curve is shown in red.

The subthreshold slope S is given by equation (3.5) and can be extracted by plotting log I_D against V_{GS} as depicted in Figure 3.9. The transistor data in the saturation regime were used to extract S that captures the exponential rise in the drain current before the transistor is turned on. The red line in Figure 3.9 shows this region. Since the subthreshold slope is expressed in mV/decade, the reciprocal value of the slope was taken.

$$S = \frac{\partial V_{GS}}{\partial (\log I_D)} \tag{3.5}$$

The on-state and off-state currents are defined as the highest and the lowest drain current values respectively, when the transistor operates in saturation. They are shown in Figure 3.9. Therefore, I_D at V_{GS} = –2 V (or at the highest V_{GS} bias) is the on-state current

value indicated by a red-circle and the lowest point on the curve is the off-state current indicated by a blue-circle. Lastly, the on/off current ratio is calculated as I_{ON}/I_{OFF}.

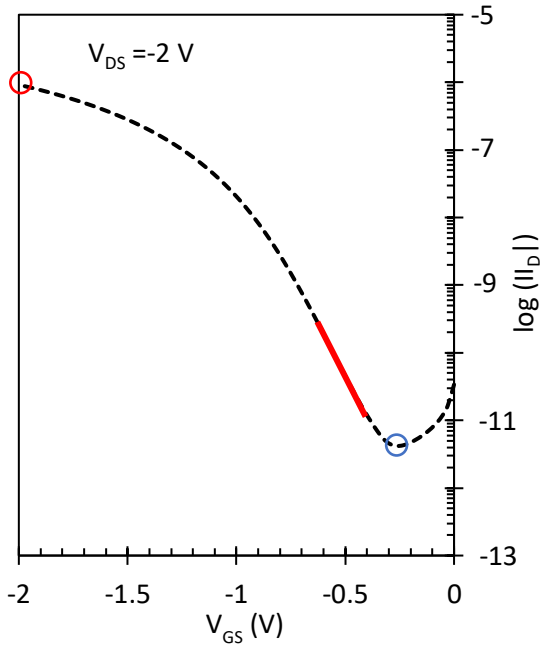

Figure 3.9: Log_{10} drain current as a function of gate-to-source voltage in saturation regime.

In addition, in this thesis (unless otherwise stated) the transconductance G_m is found from the derivative of the measured I_D versus V_{GS} in the saturation regime and taken its value at V_{GS} = –2 V and V_{DS} = –2 V. The gate leakage current I_G is taken at V_{GS} = –2 V and V_{DS} = –2 V (the maximum voltages applied during the measurement). Finally, the values of the channel width W and the channel length L of the fabricated transistors were measured using stage micrometre and microscope camera (depending on the proximity of the mask and the substrate during the evaporation, they may deviate from the mask dimensions).

Coded functions were built in Matlab to manage the extraction of transistor parameters. Equations given in this section were used. This enabled faster execution of the calculations.

Chapter 4

OTFTs with multi-finger contacts

This chapter presents multi-finger organic thin-film transistors with high transconductance based on DNTT. OTFTs with two different structures were fabricated on glass with the aim to increase the *W/L* ratio, and therefore the transconductance of the transistor, while the operation voltage was kept low. The chapter provides the measurements and results for the OTFTs under d.c. and some a.c. circuit conditions.

The chapter outline is as follows. Firstly, an introduction of the multi-finger approach is given in Section 4.1. The details of the multi-finger contact structure and transistor fabrication are summarised in Section 4.2. The results obtained from various measurements on the transistors are provided in Section 4.3. Finally, the discussion is given in Section 4.4 and a brief summary is provided in Section 4.5.

4.1. Introduction

The consumer uptake of wearable electronics [75] has been propelled by technology-savvy and health-aware consumers around the world. The calculator watch was the first wearable technology reported in the 1980s [76]. Today, fitness bands and smart watches that monitor physical activity and record vital signs are becoming smaller and more aesthetically pleasing while incorporating a whole spectrum of technologies [77]. Although they represent a commercially-successful first generation of wearable electronics, the future wearable electronics is envisioned to be highly flexible/conformal and even embedded in textiles [78]. Here, technologies that provide such mechanical attributes, in addition to desired electronic performance, are needed.

The low cost, ease of manufacturing, and ability to fabricate organic thin film transistors (OTFTs) on a variety of substrates [79], including textiles [80], make such technology suitable for wearable sensors. Some applications reported to date include highly flexible organic thin film transistors (OTFTs) used as mechanical strain sensors on PET substrate [81], pH detection devices [82], and multi-functional sensors for detecting temperature changes, light intensity, pressure and nitrogen flow [83]. Being an integral part of an analogue sensor, the OTFT can provide two functions. It can act as a signal transducer by converting the physical stimulus to voltage [84] and a signal amplifier. The transconductance and geometry of the transistor play an important role for the latter.

The OTFT transconductance can be increased by several means. If the gate dielectric capacitance and the field-effect mobility of the OTFT are fixed (the latter being mostly controlled by the choice of the semiconductor material), one way to increase the drain current is by increasing the ratio of the channel width to channel length (W/L), i.e. to increase W and/or reduce L [85]. To date the main focus was on the reduction in L and the

demonstration of digital circuits with high operation frequency [86-87]. When OTFTs with *L* = 1 μm and *W* = 10 μm were achieved by using high-resolution silicon stencil masks, the transconductance of 12 μS was achieved and ring oscillators based on such transistors exhibited megahertz operation [86]. In such a case the *W/L* ratio of 10 was used to minimize the transistor parasitic capacitances and thus realize high switching speed. Recently, bottom-contact OTFTs based on Dph-DNTT have successfully achieved high operating frequency due to their small contact resistance. Although typically the top-contact configuration will result in a smaller contact resistance, this was accomplished by employing a sufficiently thin gate dielectric and a treatment to the surface of the source/drain contacts [88].

Wearable analogue sensors are not likely to be required to work in megahertz frequency range and OTFTs operating at ~1 kHz would satisfy many applications. For example, in [89] the complementary (CMOS) D-flip flop logic circuits based on OTFT with operating frequency of 75 Hz was proposed for wearable/flexible sensors because it exhibits low-voltage operation. Nevertheless, the ability of the transistors to amplify signals remains essential.

If the demand on the transistor operation frequency is relaxed, increasing the channel width *W* becomes an option. One of the little explored pathways for increasing *W* is the use of multi-finger source/drain contacts [90]. Such transistors offer high *W/L* ratio and therefore high drain current while keeping the overall transistor area reasonably small.

This chapter represents a significant advancement of such transistor structures by achieving low-voltage operation and, to our knowledge, one of the highest transconductance values reported to date. Simple voltage amplifier based on such transistors is also shown for the first time. Finally, the chosen transistor dimensions are compatible with the minimum line features achievable by printing [91-92], making the transistors with multi-finger source/drain contacts viable for large-scale printed electronics.

4.2. Experimental details

Low-voltage bottom-gate, top-contact p-type transistors based on dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) were fabricated according to the procedure described in Chapter 3 on glass (Ossila, U.K.). The ultra-thin gate dielectric bi-layer consisted of aluminium oxide (AlO_x) prepared by UV/ozone oxidation [74] and an octadecyl phosphonic acid ($C_{18}PA$) monolayer prepared in vacuum [69]. The thickness of the gate dielectric was 10 nm [93]. The thickness of the DNTT layer was 20 nm. The thickness of the gold source/drain contacts was 50 nm. Figure 4.1 shows a cross section of the transistor along with the layer thicknesses. Two different source-drain masks (Ossila, U.K.) were used:

(a) Wide-gate structure with L = 50 μm and W = 18.23 mm leading to W/L ratio of ~365

(b) Narrow-gate structure with L = 20 μm and W = 4.03 mm leading to W/L ratio of ~202

In addition, four different gate widths were used to allow the additional control of W. Figure 4.2 depicts a schematic and top-view of the narrow- and wide-gate structure respectively, featuring a schematic of the four different gate widths in the wide-gate structure.

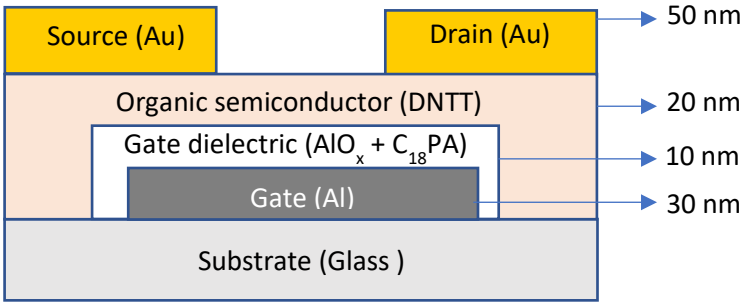

Figure 4.1: Cross-section of an organic transistor.

The transfer and output characteristics of the OTFTs were measured in a sweep mode. The gate-to-source voltage V_{GS} (or drain-to-source voltage V_{DS}) was swept from 0 to −2 V.

The threshold voltage and field-effect mobility were extracted from the transfer characteristics measured in saturation using equations descripted in Chapter 3. Subthreshold slope, on-state current, off-state current and on/off current ratio were also extracted from the saturation curve. The transistor a.c. performance was investigated in terms of the a.c. transconductance, cut-off frequency, and voltage gain obtained from a simple common-source amplifier based on such transistors.

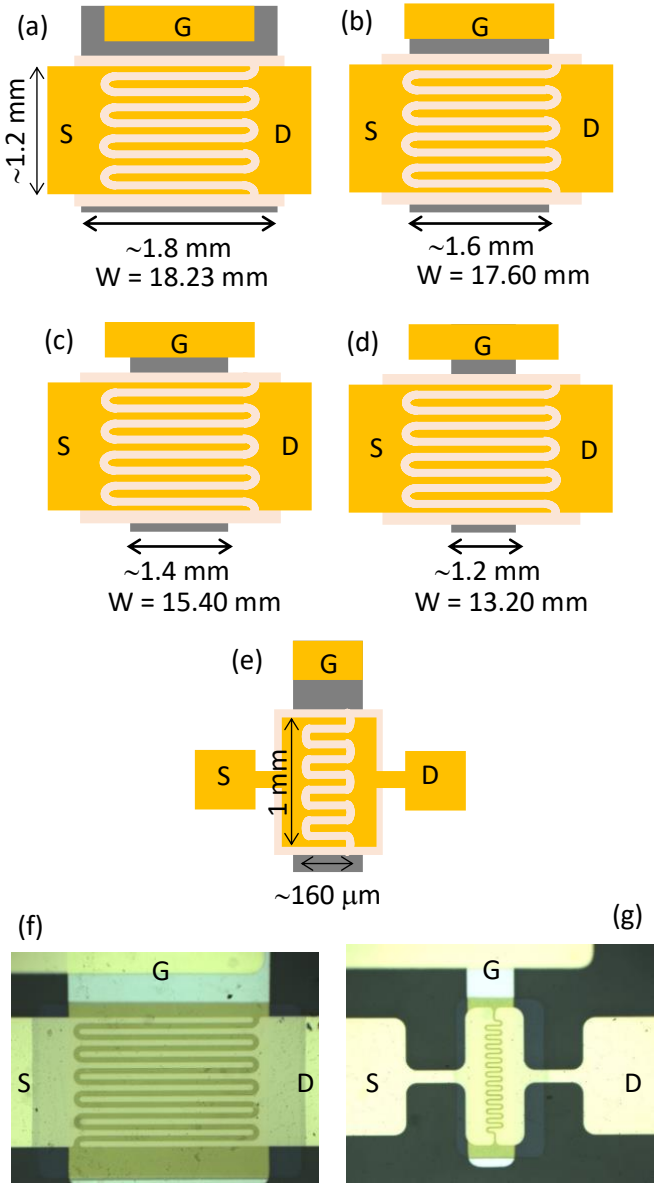

Figure 4.2: Schematic of wide-gate transistor with different gate width (a-d), schematic of narrow-gate transistor (e) and top-view of wide-gate and narrow-gate transistors (f,g).

4.3. Results

4.3.1 Transistor electrical characteristics

Figure 4.3 shows the transfer and output characteristics of a narrow-gate transistor on glass substrate. In the saturation regime its threshold voltage V_T is −0.57 V, the field-effect mobility μ is 0.23 cm2/V·s and the transconductance G_m, calculated by the derivation of the transfer characteristic and taken the value at $V_{GS} = V_{DS} = -2$ V, is 33 µS. The gate dielectric capacitance C_{diel} = 0.423 µF/cm2. Both transistor structures provide the on-state current (measured at $V_{GS} = V_{DS} = -2$ V) in the 10^{-5} A range, off-state current of ~10^{-8}–10^{-11} A, gate leakage current (measured at $V_{GS} = V_{DS} = -2$ V) less than 10^{-9} A, subthreshold slope of ~100 to ~330 mV/decade, and transconductance G_m of ~30 to 60 µS.

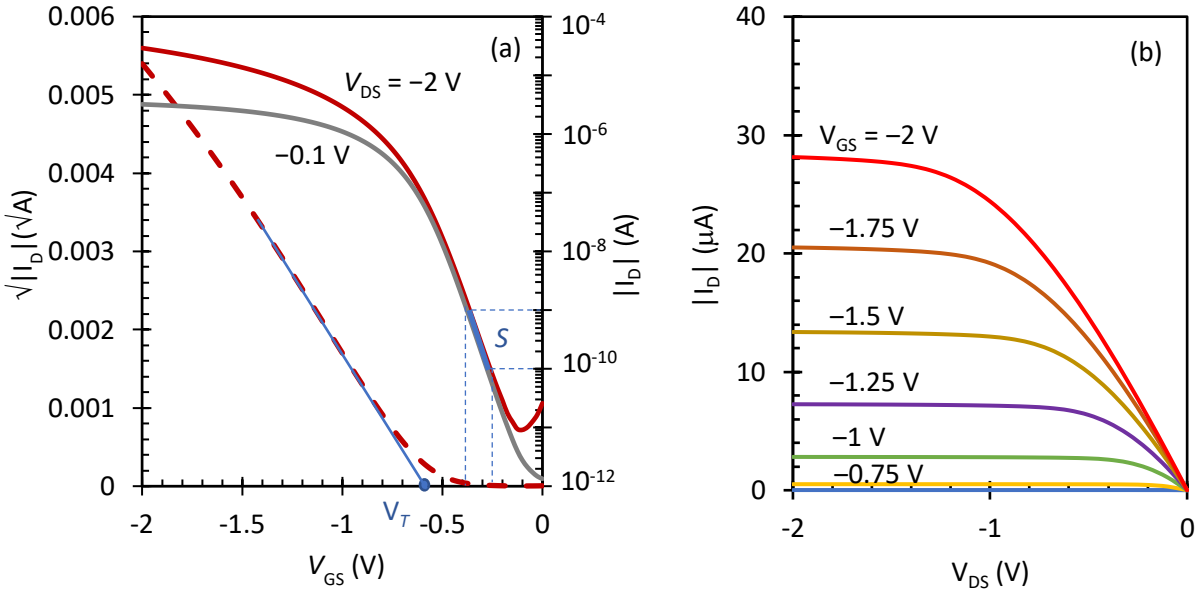

Figure 4.3: Transfer (a) and output (b) characteristics of a narrow-gate organic transistor on glass.

Figure 4.4 shows the mobility, the threshold voltage and subthreshold slope plotted as a function of *W/L* for both wide- and narrow-gate transistors. The variation in *W/L* ratio is a

result of different gate widths (see Figure 4.2) and a variation in *L* resulting from the proximity of the mask and substrate during the evaporation.

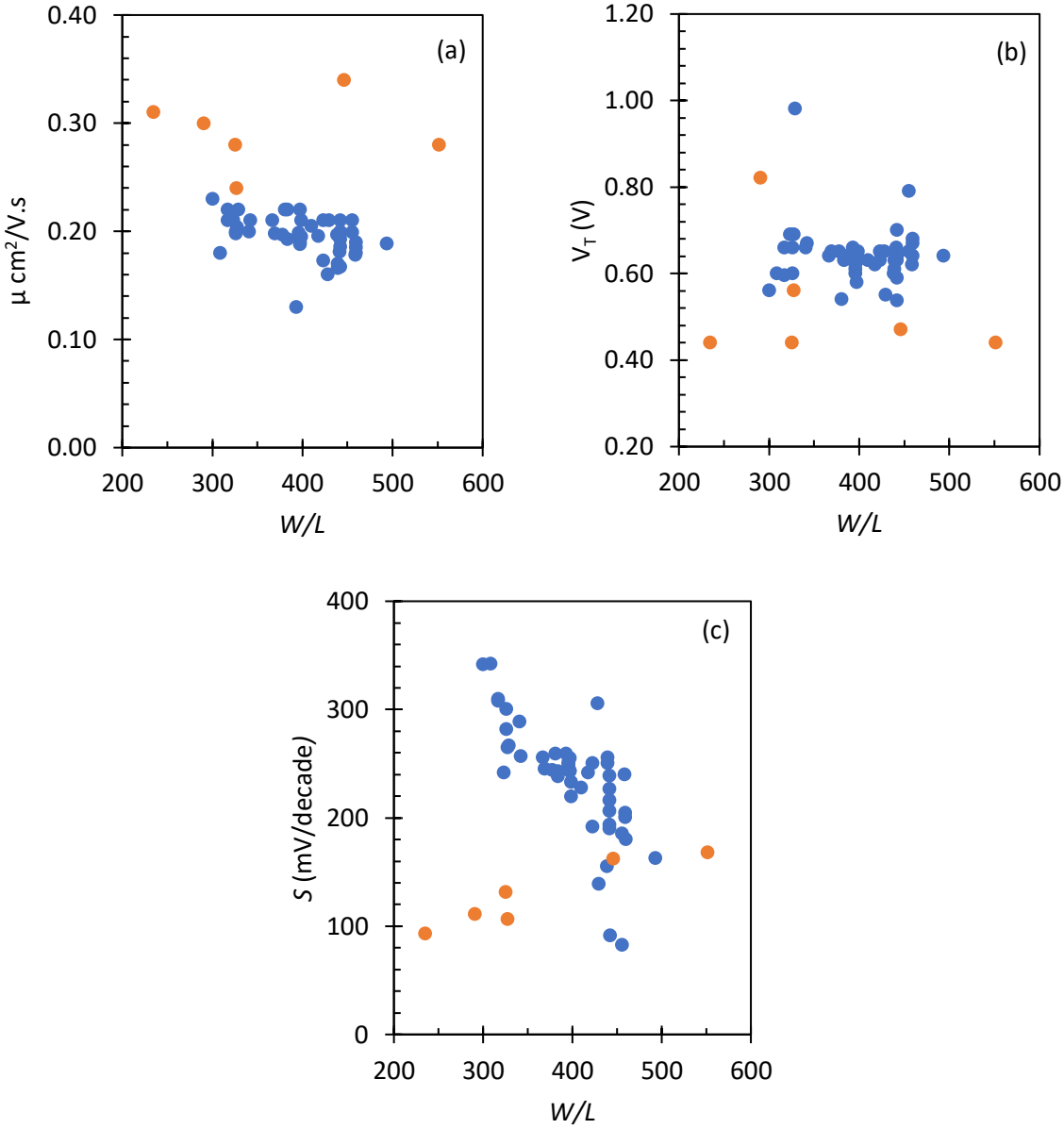

Figure 4.4: Mobility (a), threshold voltage (b) and subthreshold slope (c) of wide- (blue points) and narrow-gate (orange points) transistors plotted against *W/L*.

The wide-gate transistors exhibit similar mobility and threshold voltage regardless of the *W/L*. The same is true for the narrow-gate transistors. Overall, the narrow-gate transistors exhibit slightly higher mobility and lower threshold voltage when compared to the wide-gate transistors.

The subthreshold slope of wide-gate transistors showed larger change with the increase of *W/L* (difference of ~251 mV/decade) compared to the narrow-gate transistors (difference of ~75 mV/decade). At the same time, the subthreshold slope of wide-gate transistors decreased with increasing *W/L* ratio, while the subthreshold slope of narrow-gate transistors decreased. In addition, narrow-gate transistors exhibited lower subthreshold slope compared to wide-gate transistors.

Previously the geometry of multi-finger source/drain contacts was studied in OTFTs based on 6,13-bis(triisopropylsilylethynyl) pentacene [90]. These transistors required high driving voltages of 40 V and the hysteresis in their transfer characteristics increased to ~15 V as the number of fingers increased from 1 to 4. Here, the turn-on voltage of the transistors is close to zero, leading to very low threshold and operation voltages.

4.3.2 A.c. performance of the transistor

Next, the a.c. transconductance was measured by applying a sinusoidal voltage of 1 Hz. The circuit configuration for this measurement is shown in Figure 3.6 (see Chapter 3). The transconductance was calculated using equation (3.3), namely:

$$g_{\mathrm{m}} = \frac{i_{\mathrm{d}}}{v_{\mathrm{g}}}$$

where i_{d} is the measured peak-to-peak modulation in the drain current and v_{g} is the gate bias sinusoidal voltage of 0.2 V peak-to-peak (V_{pp}). The d.c. offset of the gate voltage and the drain voltage were held at −2 V, to allow the transistors to operate in the saturation regime. In the saturation regime, the transconductance depends on the gate voltage V_{GS} and is independent of the drain voltage V_{DS}. Examples of a.c. transconductance measurements are shown in Figure 4.5. The Figure depicts the measured drain current for transistors with different gate widths against time. Both the transistors with wide and narrow gates are shown.

The transconductance g_m calculated according to (3.3) increased from ~31 to ~62 μS as the *W/L* increased. These values are similar to those obtained by differentiating the transfer characteristic for $V_{GS} = V_{DS} = -2$ V (d.c. transconductance), as expressed by equation (2.15). They also surpass the highest reported values to date [86] by a factor of 2 to 5.

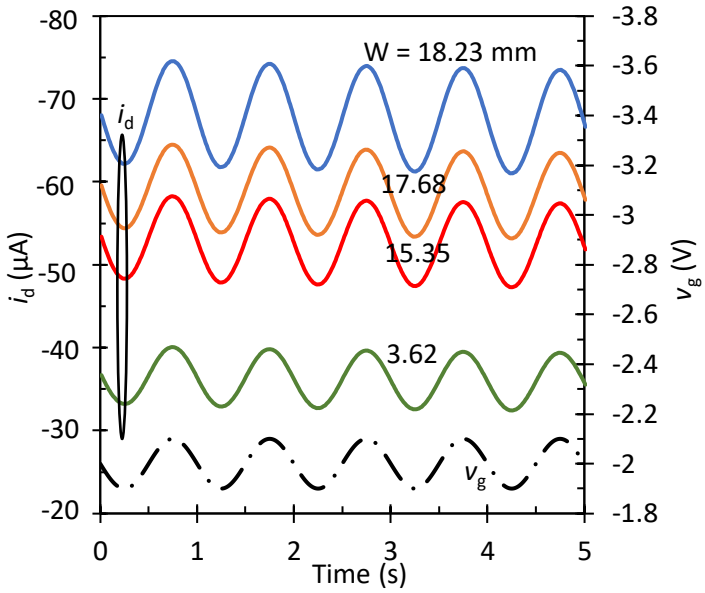

Figure 4.5: Drain current versus time for transistors with different gate widths, given in mm. W of 3.62 mm corresponds to narrow-gate transistor. Solid and dashed curves depict i_d and input voltage v_g, respectively.

As seen in Figure 4.5, the measured i_d and its modulation is higher for wide-gate transistors compared to narrow-gate ones because the wide-gate transistors possess larger *W/L* ratio. In addition, as the *W/L* of the wide-gate transistors increases, so does the transconductance. This behaviour is in agreement with equation (2.15).

To investigate the maximum operation frequency (cut-off) of both transistor structures, the transconductance was measured as a function of a.c. frequency. Figure 4.6 shows the transconductance of wide- and narrow-gate transistors. The transconductance of the narrow-gate transistor is ~ 32 μS up to ~ 10 kHz and its cut-off frequency is 13.4 kHz. However, the wide-gate transistor shows a slightly different behaviour. The transconductance

at low frequencies is ~ 60 μS and remains approximately constant up to ~ 2 kHz. For higher frequencies g_m initially increases and then decreases, reaching the maximum value of ~ 105 μS around 9 kHz. Although this anomaly requires further investigation, both types of transistors are suitable for working with frequencies up to 1 kHz.

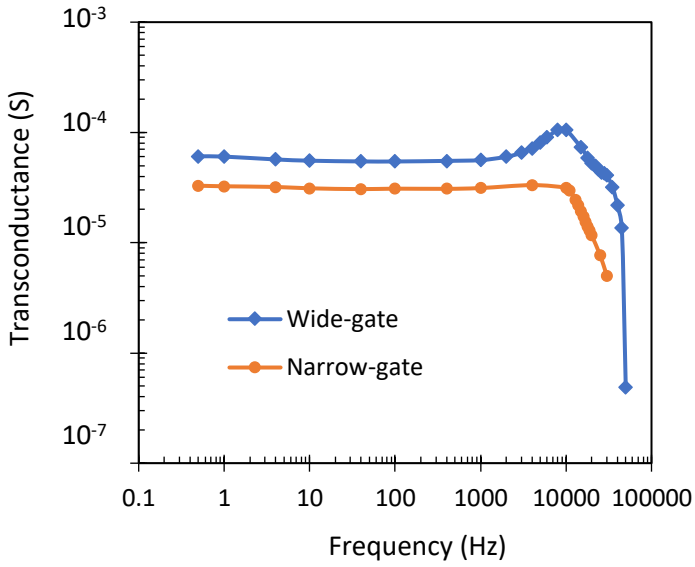

Figure 4.6: Transconductance as a function of a.c. frequency.

Finally, a simple voltage amplifier was built according to Figure 3.7 (see Chapter 3). Again, sinusoidal voltage of 1 Hz was applied to the transistor gate with a peak-to-peak voltage of 0.2 V and the modulated output voltage was measured below resistor R_d. Three different resistor values were used; 5.6 kΩ, 47 kΩ and 220 kΩ. For each transistor and resistor combination, a range of supply voltages V_{DD} was used and the drain current i_d and the output voltage v_{out} were measured. The a.c. voltage gain was calculated using equation (3.4), namely:

$$g_v = \frac{v_{out}}{v_g}$$

where v_{out} is the measured peak-to-peak modulation in the output voltage and v_g is the gate bias modulation of 0.2 V_{pp}. An example of the measured output voltage is shown in Figures 4.7 to 4.9 for different values R_d and V_{DD} voltages.

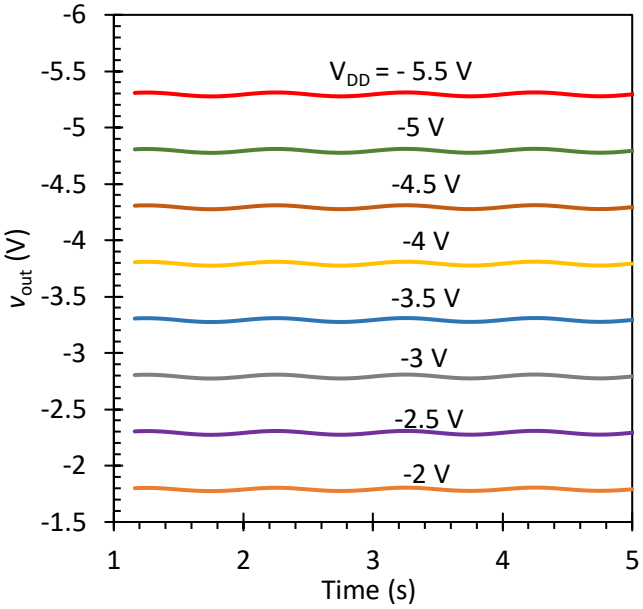

Figure 4.7: Output voltages v_{out} of the transistor amplifier for R_d = 5.6 kΩ and different V_{DD}. v_{in} was identical to v_g of Figure 4.5.

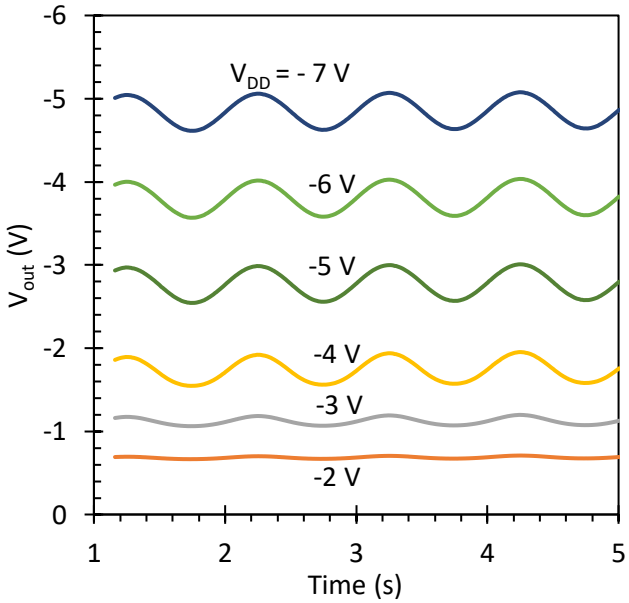

Figure 4.8: Output voltages v_{out} of the transistor amplifier for R_d = 47 kΩ and different V_{DD}, v_{in} was identical to v_g of Figure 4.5.

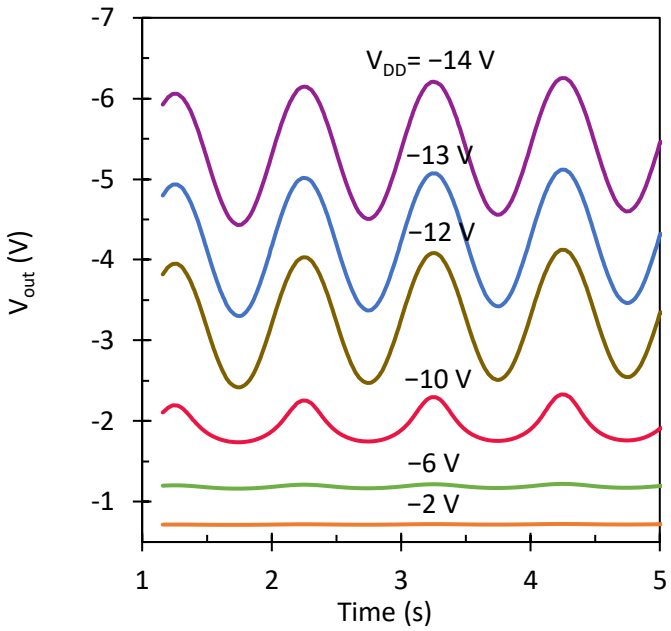

Figure 4.9: Output voltages v_{out} of the transistor amplifier for R_d = 220 kΩ and different V_{DD}, v_{in} was identical to v_g of Figure 4.5.

The transistor operation point V_{DS} and a.c. voltage gain g_V, calculated using equation (3.4), are plotted against V_{DD} in Figure 4.10, for the three different R_d values. For R_d = 5.6 kΩ, peak-to-peak v_{out} increases with increasing V_{DD} until V_{DD} reaches ~ –2.5 V; for R_d = 47 kΩ it is also increasing until it reaches ~ –5 V. Finally, for R_d = 220 kΩ the peak-to-peak v_{out} increases with increasing V_{DD} until V_{DD} reaches ~ –12 V. Further increase in $|V_{DD}|$ does not affect the output voltage v_{out}.

The a.c. voltage gain increases with increasing R_d, reaching ~ 8.4 V/V for R_d = 220 kΩ. The gain saturates when the transistor reaches saturation operation. The data of Figures (4.7) to (4.9) suggests that regardless of the value of R_d, V_{DS} operation point of at least −2.5 V is needed to reach the maximum voltage gain when v_g oscillates around −2 V. One can also infer that the resistance between source and drain is ~100 kΩ, a factor of ~10 smaller when compared to DNTT transistors with standard source/drain contacts with L = 30 μm and W = 1 mm [84]. This decrease is important for the reduction in both V_{DD} and R_d.

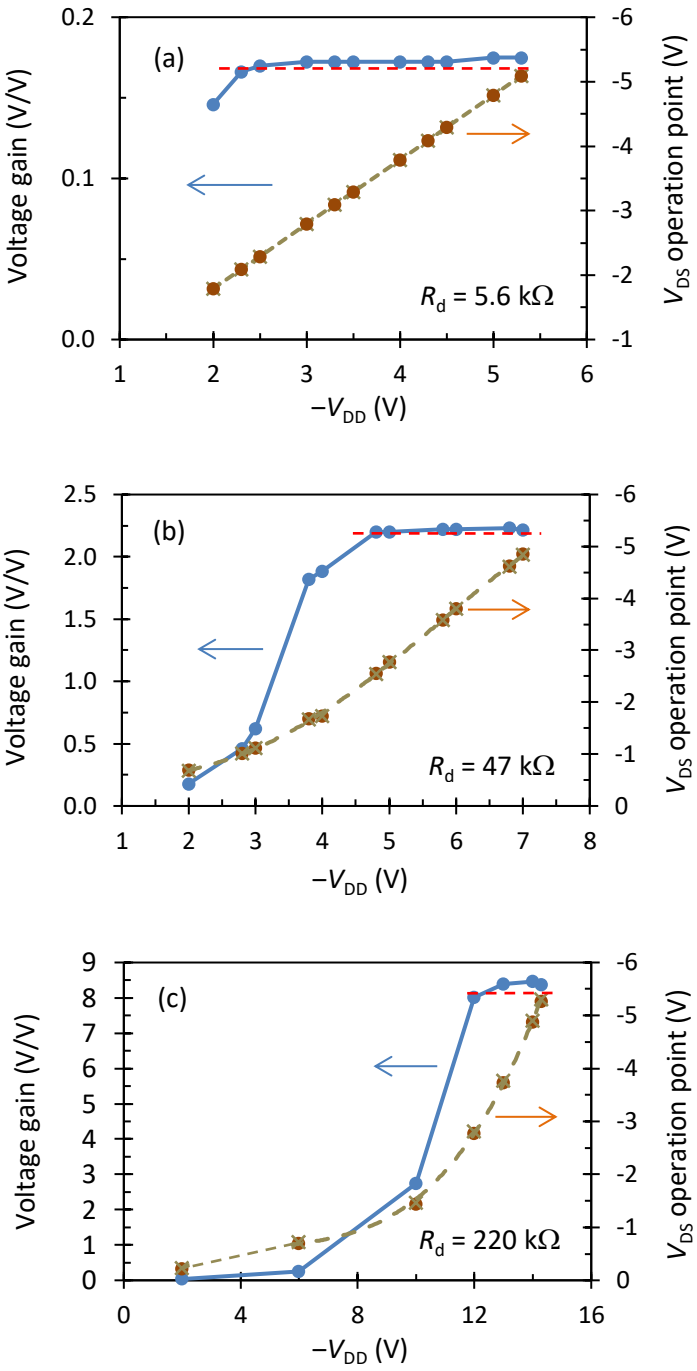

Figure 4.10: Voltage gain of the transistor amplifier of Figure 3.7 for three values of R_d. v_g was identical to that of Figure 4.5. The a.c. voltage gain was calculated using Eq. (3.4). The solid dots show the measured data. The ×-symbols correspond to calculations using Eq. (4.1). The red dashed lines correspond to calculations using Eq. (4.5).

4.4. Discussion

To date, some of the largest reported OTFT transconductances are: 0.76 μS for low-voltage OTFT based on DNTT with *W/L*= 1μm/1μm and silver source/drain contacts fabricated using subfemtoliter inkjet printing [94]; and 4 μS and 3 μS for OTFTs based on pentacene and di(phenylvinyl)anthracene (DPVAnt) respectively, with the latter being more stable alternative compared to the former [95]. The largest reported width-normalized transconductance for organic transistors employing similar materials as those used in this work is 0.4 S/m. These were nanoscale OTFTs with W = 500 nm and L= 90 nm (i.e. G_m = 0.2 μS) [70]. However, one may note that submicron L leads to adverse effects such as high contact resistance [90] and less defined saturation behaviour of the transistor. Area-selective doping technique can be used to reduce the contact resistance [70], while reducing the gate dielectric thickness [91] along with the reduced channel length can eliminate the latter effect [96]. Finally, the largest reported value so far for similar type of OTFTs is 12 μS for C_{10}-DNTT OTFTs exhibiting low-voltage operation [86,97]. In this current work, the achieved transconductance ranges from ~30 μS to ~60 μS and appears to be one of the highest reported for OTFTs. This high transconductance results from the low-voltage transistor operation combined with the multi-finger source-drain contacts.

Based on the circuit of Figure 3.7 V_{out} can be expressed as:

$$V_{out} = V_{DD} - R_d \cdot I_D \tag{4.1}$$

where the drain current I_D is a function of V_{GS} and V_{DS}. If the a.c. modulation of the gate voltage is turned off, V_{out} becomes the operation point V_{DS} of the transistor. Equation (4.1) was used to calculate V_{DS} from the known values of V_{DD}, Rd and the measured I_D. The calculated values are shown as ×-symbols in Figure 4.10. The agreement between the

measured and calculated values confirms the validity of (4.1). In analogy to [98] the differentiation of (4.1) leads to:

$$dV_{\mathrm{out}} = -R_{\mathrm{d}} \cdot dI_{\mathrm{d}} \,, \tag{4.2}$$

where

$$dI_{\mathrm{d}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}}\bigg|_{V_{\mathrm{ds}}} dV_{\mathrm{gs}} + \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{ds}}}\bigg|_{V_{\mathrm{gs}}} dV_{\mathrm{ds}} = g_{\mathrm{m}} dV_{\mathrm{gs}} + g_{\mathrm{d}} dV_{\mathrm{ds}} = g_{\mathrm{m}} dV_{\mathrm{gs}} + g_{\mathrm{d}} dV_{\mathrm{out}} \tag{4.3}$$

where g_{m} is the transconductance and g_{d} the drain conductance of the transistor. The minus sign in (4.2) means that the phase of the sinusoidal drain current and the output voltage are shifted by 180°. Since the drain current follows the changes in the gate voltage (see Figure 4.5), i.e. they are in phase, a phase shift of 180° between the output and gate voltages exists (see Figures 4.7 to 4.9).

Combining (4.2) and (4.3) leads to the voltage gain:

$$g_{\mathrm{v}} = -\frac{g_{\mathrm{m}}}{g_{\mathrm{d}} + \frac{1}{R_{\mathrm{d}}}} \,, \tag{4.4}$$

When the transistor operates in the saturation regime, the drain conductance becomes zero, namely $g_{\mathrm{d}} = 0$. Consequently, the voltage gain can be expressed as:

$$|g_{\mathrm{v}}| = g_{\mathrm{m}} R_{\mathrm{d}} \tag{4.5}$$

The voltage gain becomes constant and proportional to the transconductance of the transistor and the resistor R_{d}.

The saturation of the voltage gain is observed in Figure 4.10 for all values of R_{d}. In addition, based on equation (4.5) the voltage gain of the transistor shown in Figure 4.10(a)

should be 30 μS × 5.6 k = 0.168, whereas the measured value is 0.173 V/V. The calculated voltage gain of the transistor of Figure 4.10(b) is 46 μS × 47 k = 2.16 whereas the measured value is 2.20 V/V. Finally, the calculated voltage gain of the transistor shown in Figure 4.10(c) is 37 μS × 220 kΩ = 8.14, whereas the measured value is ~ 8.40 V/V. The achieved agreement confirms the validity of the above model for the voltage amplifier of Figure 3.7 based on the organic transistor. This behaviour resembles the one observed for similar voltage amplifiers based on organic electrochemical transistors (OECT) [98], even though OTFT and OECT operate very differently. While OECT is a 'normally-on' transistor that requires diffusion of ions into the transistor active area to curtail the drain current, OTFT is a 'normally-off' transistor where the field-effect controls the drain current.

For practical applications one would prefer high voltage gain of the transistor while keeping the supply voltage V_{DD} as low as possible. Figures 4.7 to 4.9 show that V_{DD} must be high enough to allow the transistor to operate in saturation. In such a case the output voltage is sinusoidal. To achieve the voltage gain higher than one, a suitable resistor R_d must be selected. As the R_d increases, the voltage gain in saturation increases, but so does the required V_{DD}. When R_d = 47 kΩ, a −5 V supply voltage provides voltage gain of 2.2 V/V. Increase of R_d to 220 kΩ leads to a gain of ~8.4 V/V but V_{DD} off at least −12 V is required. This is because a larger voltage drop occurs across the resistor R_d. Ultimately there is a trade-off between the gain and the supply voltage.

4.5. Summary

Low-voltage, p-type DNTT transistors with two multi-finger source/drain contacts were studied. They exhibited threshold voltage between ~ −0.4 and ~ −0.8 V and field-effect

mobility between 0.13 and 0.34 cm^2/Vs. Owing to high W/L ratio their a.c. transconductance varies from ~30 to ~60 μS and scales with the transistor dimensions.

The multi-finger contact configuration is promising for large-scale printed electronics as it is compatible with the printing techniques available. The approach of increasing W/L ratio presented in this chapter led to OTFTs with high transconductance, surpassing any previously published data. Both transistor types operate beyond 1 kHz while the transistors with the shorter channel length (L = 20 μm, W = 4.03 mm) exhibited a cut-off frequency of 13.4 kHz. In addition, the transistors were used to build simple voltage amplifiers by adding a resistor R_d on the drain side of the transistor. Higher R_d required higher supply voltage V_{DD} but resulted in increased voltage gain. A voltage gain in excess of 8 V/V was obtained for V_{DD} of −12 V and R_d of 220 kΩ when transistor with medium value of transconductance of 37 μS was used. Consequently, these transistor structures are capable of providing voltage gain higher than 10 V/V.

Chapter 5

OTFTs based on [n]phenacenes

Previously in Chapter 4, the performance of various transistor structures based on DNTT was investigated. In this chapter similar transistors, yet using other organic semiconductors, are presented. OTFTs based on [n]phenacenes with different number of benzene rings (n) were fabricated with the aim to lower the threshold voltage and increase the field-effect mobility of the transistors and thus raise the transconductance even further. [n] was varied from 5 to 7 and for the first time these high-mobility organic semiconductors were paired with ultra-thin bi-layer gate dielectric.

The chapter outline is as follows. Section 5.1 introduces [n]phenacenes as semiconductors for OTFTs. The experimental details including the transistor fabrication and layer structure are summarised in Section 5.2. The results obtained from a comprehensive

evaluation of various [n]phenacene transistors are provided in Section 5.3. Finally, the discussion and the chapter summary are given in Section 5.4 and Section 5.5, respectively.

5.1. Introduction

[n]Phenacenes are conjugated organic semiconductors formed from benzene rings fused in a zigzag pattern where [n] indicates the number of benzene rings. They exhibit promising electrical properties suitable for p-channel organic thin-film transistors. These properties result from their molecular structure that distinguishes them from their isomeric [n]acene counterparts such as tetracene and pentacene. [n]Acenes are formed by linearly-fused benzene rings and although OTFTs based on them can exhibit reasonably high field-effect mobility, a major downside is their sensitivity to light and ambient oxygen and moisture [99]. Phenacenes compared to acenes possess larger bandgap and deeper highest occupied molecule orbital (HOMO) i.e. higher ionisation potential, resulting in better environmental stability and lower reactivity. Consequently, increasing attention is directed towards these materials for organic transistors and their applications [100-106].

Previously reported OTFTs based on single crystals of [n]phenacene showed outstanding filed-effect mobility. However, the threshold voltage for such transistors was relatively high (more than –30 V) since they were fabricated on oxidized silicon wafer. The achieved mobility ranges from 1 to about 11 $cm^2/V{\cdot}s$ for [5]phenacene and [9]phenacene respectively [106]. A low desired threshold voltage of around –6 V was obtained by decreasing the thickness of SiO_2 gate dielectric and the use of high-permittivity gate dielectrics, but this also resulted in substantial reduction in the field-effect mobility because the semiconductor in these OTFTs was a vacuum-deposited thin film rather than a single-crystal which routinely shows higher mobility compared to the thin film [103,107]. Furthermore, in these studies it was observed that the growth of [n]phenacene on the gate

dielectric with smaller surface energy showed more preferable molecular arrangement of the [n]phenacene molecules in the vacuum-deposited thin films.

The capacitance of the gate dielectric controls the operating voltage of a field-effect transistor. That is, the realisation of low-operating voltage can be achieved by reducing the thickness of the gate dielectric and/or by using dielectric materials with larger permittivity, as both will lead to higher gate dielectric capacitance and lower operating voltage of the OTFTs. The use of ultra-thin bi-layer gate dielectric involving organic (self-assembled monolayer) and inorganic (aluminium oxide) materials is a well-established method to achieve this. The former provides low surface energy and the latter large relative permittivity [15,69,108-111].

Previously, such ultra-thin bi-layer gate dielectrics with a thickness of 5 to 12 nm were employed in OTFTs based on DNTT and such transistors successfully achieved operating voltages compatible with the state-of-art silicon microelectronics. They exhibit low threshold voltage of about −0.5 V, small leakage current density, and large capacitance of 0.3 to 0.7 μF/ cm^2 [15,69].

In this chapter, OTFTs based on [n]phenacenes (n = 5, n = 6 and n = 7) were fabricated and their electrical performance was investigated. Since the aim was to reduce the threshold voltage of the transistors, i.e. realize low-voltage operation, while taking advantage of the higher mobility of [n]phenacenes, the bi-layer gate dielectric previously employed in DNTT OTFTs was used (see Chapter 4). As previously described, this bi-layer consists of AlO_x coated with $C_{18}PA$. Two batches of OTFTs were fabricated, one on PEN foils and the other on glass. On PEN two different transistor structures, wide- and narrow-gate, (see Chapter 4) were fabricated to allow investigation of different channel width-to-length ratios. In addition, modification of the interface between the source/drain contacts and [n]phenacene was introduced in some OTFTs by adding an [m]phenacene layer of a different chain length than that used for the semiconductor (i.e. $m \neq n$). This might alter the injection of carriers at

the contact/semiconductor interface, as phenacenes with higher number of benzene rings have a smaller bandgap and/or deeper HOMO level. Finally, another round of fabrication was executed to assess the effect of the substrate and/or the geometry of the transistor channel. Here, OTFTs were fabricated on glass substrate with standard source/drain contacts structure. Moreover, the interfacial layer between the source/drain contacts and the organic semiconductor layer was omitted but the bi-layer gate dielectric was prepared using two different methods [15,69].

5.2. Experimental procedures

Many OTFT samples with [n]phenacenes (where [n] = 5, 6 or 7) as the semiconductor layers were fabricated. Overall, three different transistor geometries (standard, narrow-gate and wide-gate), two substrates (glass or PEN) and two different $AlO_x/C_{18}PA$ dielectrics were tested for various [n]phenacenes, with or without the contact/semiconductor interfacial layers. The aim of such a large sample set was to apply the state-of-the-art know-how from low-voltage DNTT transistors to [n]phenacenes and identify the best fabrication approach for achieving the desired electrical performance for [n]phenacene OTFTs. Furthermore, the reference DNTT transistors were fabricated alongside phenacene OTFTs to gain comparison between these transistors and the previously studied DNTT OTFTs (see Chapter 4).

Mallory homologation protocol was employed [112] to synthesise [5]phenacene, [6]phenacene and [7]phenacene used in the transistors, following the procedure published by H. Okamoto [113]. For the first fabricated batch, bottom-gate, top-contact p-channel thin film transistors based on [n]phenacenes were fabricated and investigated with two different multi-finger source/drain contact OTFT geometries on flexible PEN (Optfine PQA1, DuPont Teijin) substrates. Wide-gate transistors with L = 50 μm and W = 18.23 mm and narrow-gate transistors with L = 20 μm and W = 4.03 mm were used. Figures 5.1 and 5.2 show a cross-

section of the OTFTs fabricated on PEN along with layer thicknesses, and the phenacene molecules, respectively. The aluminium gate layer was prepared by thermal evaporation in vacuum. The gate dielectric bi-layer consists of self-assembled monolayer of octadecyl-phosphonic acid ($C_{18}PA$) (Strem Chemicals, USA) thermally evaporated in vacuum [69] and UV/ozone oxidised aluminum oxide AlO_x [93]. A 50-nm-thick [n]phenacene semiconductor

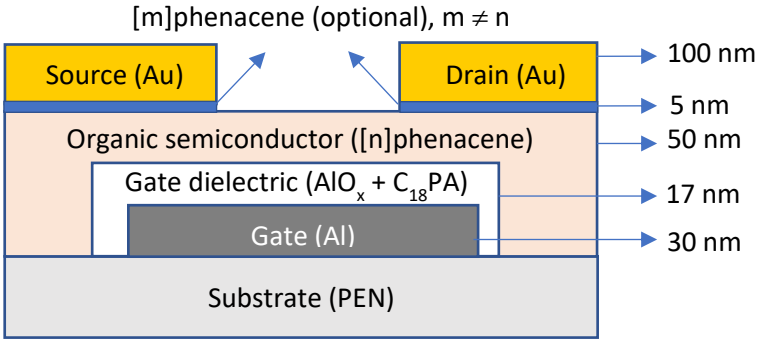

Figure 5.1: Cross-section of a transistor based on [n]phenacene fabricated on PEN.

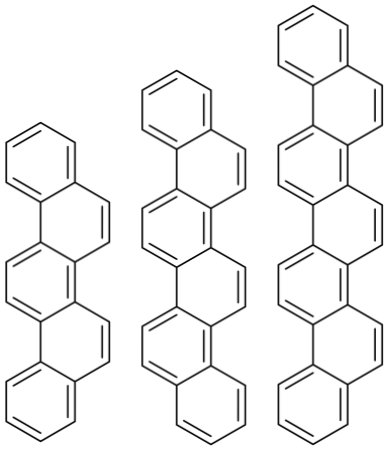

Figure 5.2: The [n]phenacene molecules. From left to right: [5], [6] and [7]phenacene.

layer was prepared by vacuum deposition at room temperature while the source/drain contacts were made of thermally-evaporated gold. Furthermore, the interface between the source/drain contacts and the organic semiconductor was modified by the insertion of an

extra layer of phenacene in some transistors. The interfacial layer consisted of [m]phenacene (m ≠ n) with a different length than the [n]phenacene used for the transistor semiconductor layer. Due to the change in the bandgap and/or the HOMO level position for phenacenes with different length, the insertion of a thin layer of longer or shorter phenacene between the source/drain contacts and the semiconductor could modify the injection of charge carriers at this interface.

To investigate the effect of the substrate and/or the transistor geometry, in the second fabrication round the transistors were fabricated on glass substrates (Ossila, U.K.) and a standard transistor structure with W = 1 mm and L = 30 μm was used to provide a direct comparison to our pervious OTFTs based on DNTT [69]. The layer structure was similar to that shown in Figure 5.1; however, the extra interfacial layer was not used and the [n]phenacene semiconductor layer was at least 100 nm thick. Additionally, the AlO_x/C_{18}PA gate dielectric bi-layer was prepared in two different ways. These two methods will be refed to as 'vacuum-prepared' and 'solution-prepared' to differentiate between the transistor gate dielectrics accordingly. For the former preparation method, the AlO_x layer of about 15 nm was prepared by UV/ozone oxidation of the surface of the gate electrodes and C_{18}PA SAM was vacuum evaporated [69]. For the latter, the AlO_x layer of about 3.6 nm was prepared by plasma oxidation of the surface of the gate electrodes and the C_{18}PA SAM was prepared in solution [108]. Finally, the transistor characteristics were measured in a dark ambient environment using Agilent B1500A Semiconductor Parameter Analyser.

5.3. Results

5.3.1 Transistor characteristics

Figure 5.3 shows the measured transfer characteristics of a [7]phenacene narrow-gate OTFT on PEN. The voltage V_{GS} was swept from 0 to −6 V and back to investigate the

hysteresis, while the voltage V_{DS} was fixed at −6 V. The OTFT exhibits a threshold voltage of −3.28 V, a field-effect mobility of 0.027 $cm^2/V{\cdot}s$ and a subthreshold slope of 110 mV/decade. The on-off current ratio is about 5×10^5. The gate dielectric capacitance was 0.24 μF/cm2.

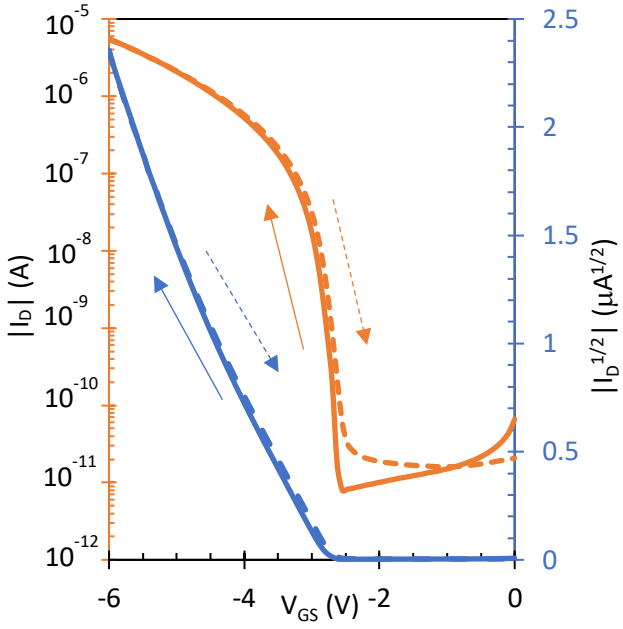

Figure 5.3: Transfer characteristics of a [7]phenacene narrow-gate OTFT on PEN substrate.

A set of the output characteristics of the same OTFT is shown in Figure 5.4. The voltage on the drain electrode was swept from 0 to −6 V and back to capture the hysteresis, if any, and V_{GS} was gradually increased. The OTFT exhibits good performance for V_{GS} up to about −4.5 V.

5.3.2 Parameters of [n]phenacene transistor on PEN substrate

The mean and standard deviations of various transistor parameters for the narrow-gate and wide-gate OTFTs fabricated on PEN were calculated and plotted as a function of the

length of the [n]phenacene molecule, as shown in Figure 5.5. The transistor parameters that were investigated are: field-effect mobility μ, threshold voltage V_T, the on-state drain current I_{ON}, the off-state current I_{OFF} and the subthreshold slope S.

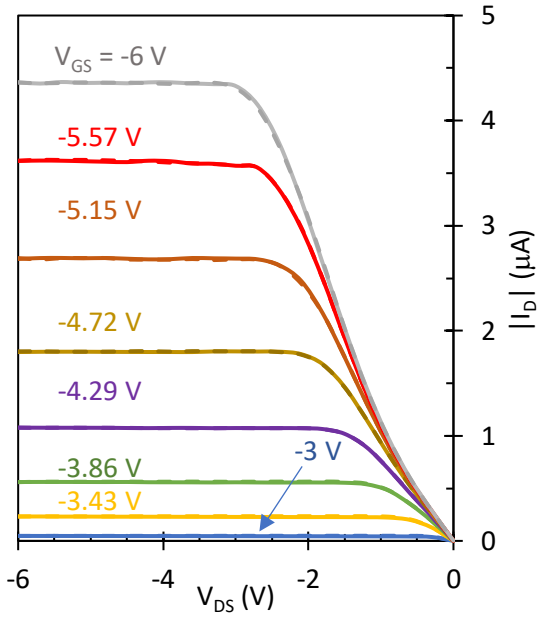

Figure 5.4: Output characteristics of [7]phenacene OTFT of Figure 5.3.

As seen in Figure 5.5(a), for both the narrow-gate and wide-gate OTFTs the mean value of the field-effect mobility increases with the increasing length of the phenacene molecule. The narrow-gate OTFTs show lower mean filed-effect mobility when compared to the wide-gate OTFTs. This is true for all [n]phenacenes. Furthermore, the difference between the mobility of the narrow-gate and the wide-gate OTFTs increases as the phenacene molecule length increases. Thus, [7]phenacene wide-gate OTFTs achieved the highest mean mobility of 0.092 $cm^2/V \cdot s$.

A different behaviour was observed for the mean threshold voltage with respect to the length of the [n]phenacene molecules for both OTFT geometries. Excluding the narrow-gate OTFTs based on [6]phenacene, the threshold voltage is not affected by the selection of

phenacene, though narrow-gate OTFTs exhibit lower threshold voltage of about −3.6 V when compared to the wide-gate OTFTs with threshold voltage of about −4.3 V.

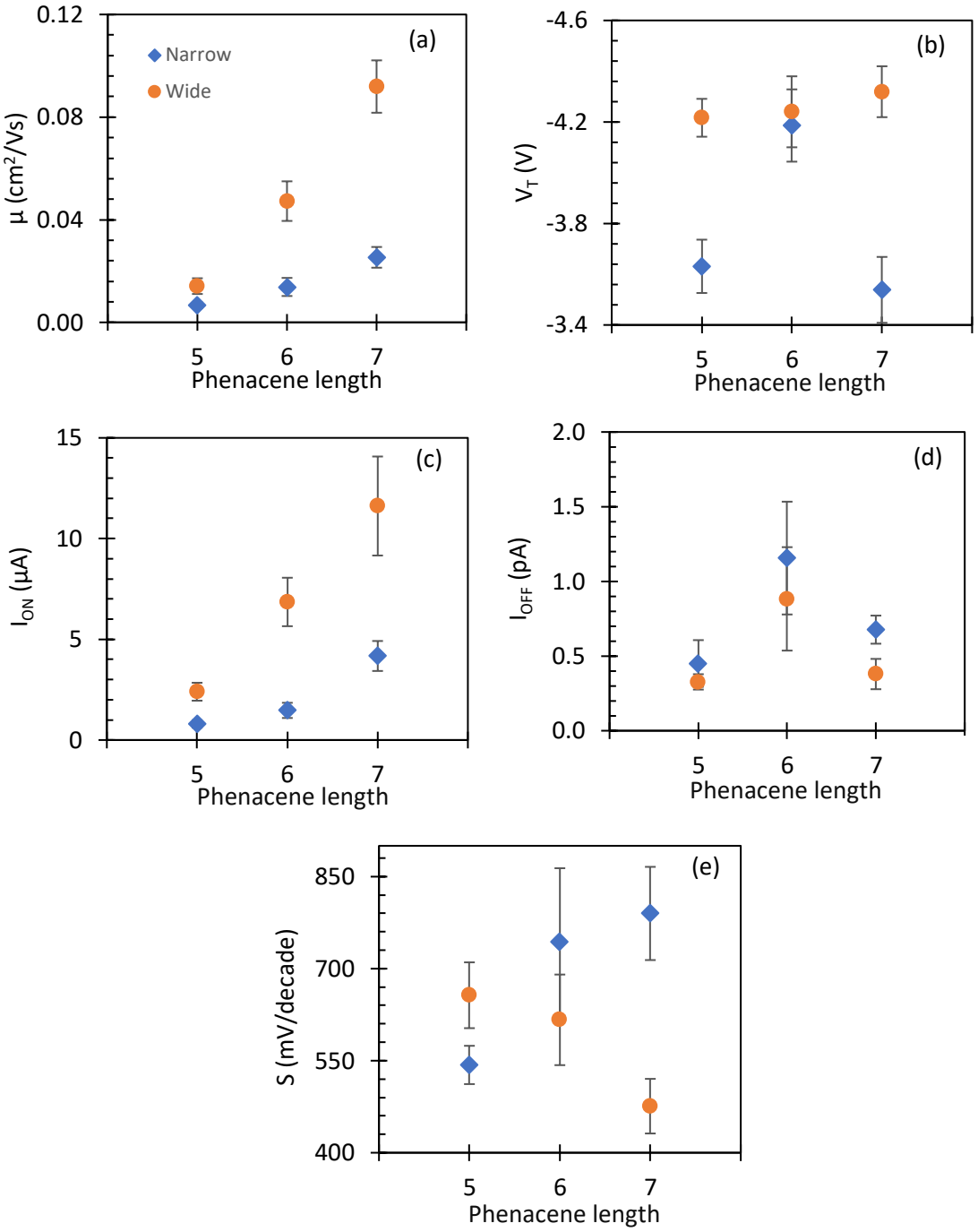

Figure 5.5: Field-effect mobility (a), threshold voltage (b), on-state drain current (c), off-state drain current (d) and subthreshold slope (e) as functions of the length of the [n]phenacene molecule for narrow- and wide-gate OTFTs on PEN substrates. The on-state drain current was extracted at $V_D = V_G = -6$V.

A qualitatively similar behaviour to that of the field-effect mobility was observed for the on-state drain current. For both the wide-gate and the narrow-gate OTFTs the on-state drain current increases as the length of the [n]phenacene molecules increases. Consequently, wide-gate [7]phenacene OTFTs have the highest on-state current of about 12 μA.

No relationship was observed for the off-state current for both the narrow-gate and the wide-gate OTFTs and the lowest mean off-state current value was 0.327 pA for wide-gate [5]phenacene OTFTs. Generally, wide-gate transistors had lower off-state current compared to narrow-gate OTFTs with the same [n]phenacene. Normalising the mean off-state current by L/W (not shown) did not have any effect apart from slightly changing the difference between the off-state currents of the narrow-gate and the wide-gate transistors, suggesting that the OTFT geometry does not play significant role.

Finally, a contrasting behaviour of the subthreshold values of the narrow-gate and wide-gate OTFTs was noted. The mean value of subthreshold slope increases with increasing phenacene length for narrow-gate OTFTs but it decreases for wide-gate OTFTs. It can be noted that as the length of the phenacene molecule increases the difference in the subthreshold slope between the wide- and narrow-gate transistors increases. The lowest subthreshold slope was obtained for wide-gate [7]phenacene OTFTs.

5.3.3 [n]Phenacene transistors on PEN with and without the source/drain interfacial layer

Figure 5.6 summarises the mean values of the field-effect mobility, threshold voltage, on-state drain current (extracted at $V_{DS} = V_{GS} = -6$ V), off-state current and subthreshold slope when [m]phenacene interfacial layer is inserted between the [n]phenacene semiconductor (m ≠ n) and the source/drain contacts. Diamonds represent the mean values of the narrow-gate OTFTs and the circles represent the parameters of the wide-gate OTFTs. The

values of the reference OTFTs without interfacial layer are shown by empty symbols. Additionally, purple symbols are used for [5]phenacene, red for [6]phenacene and yellow for [7]phenacene interfacial layer.

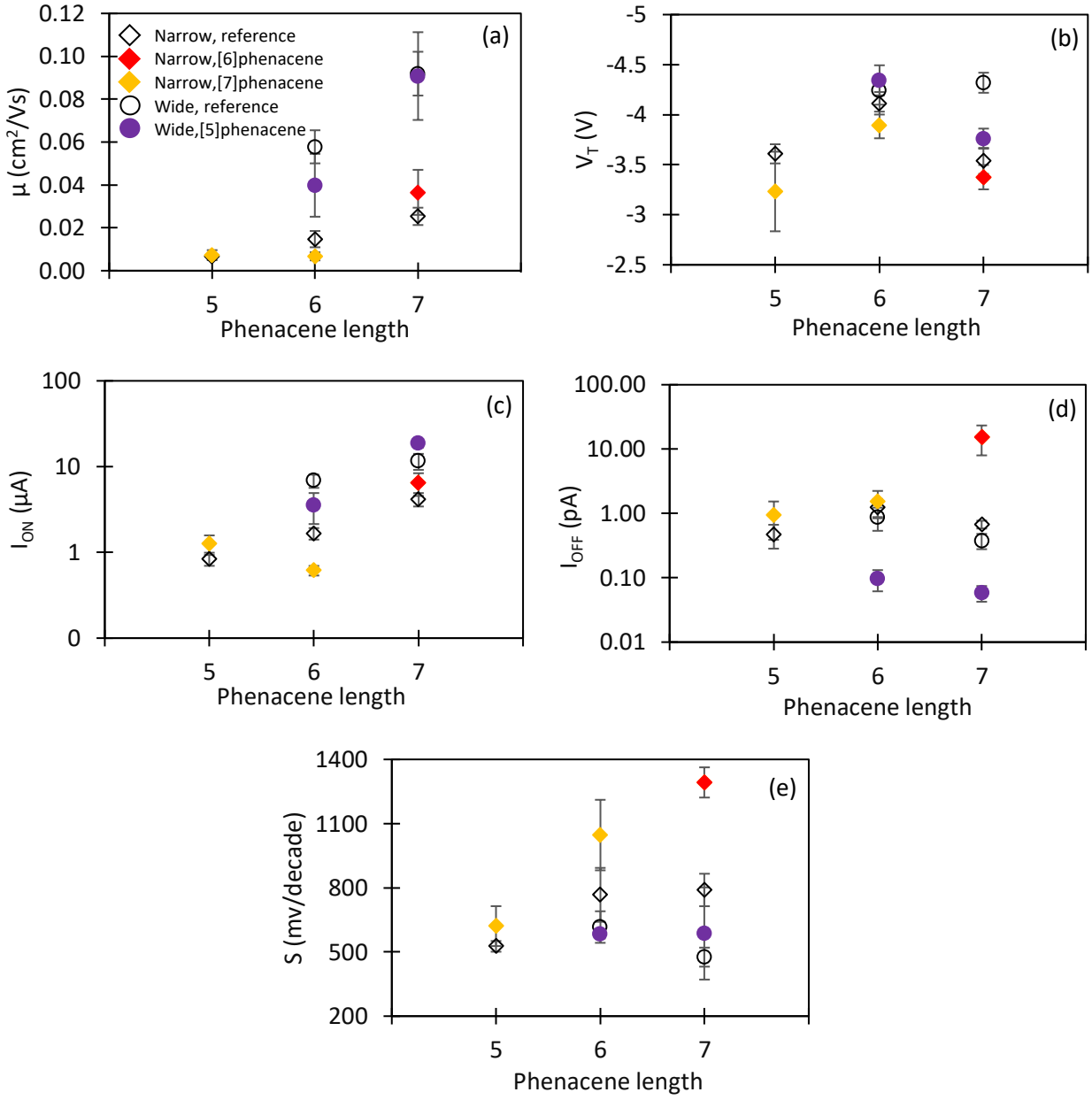

Figure 5.6: Field-effect mobility (a), threshold voltage (b), on-state drain current (c), off-state drain current (d) and subthreshold slope (e) as functions of the length of the [n]phenacene semiconductor for narrow- and wide-gate OTFTs on PEN.

The field-effect mobility was not affected by the insertion of [7]phenacene interfacial layer in [5]phenacene OTFTs. For the [6]phenacene OTFTs, the addition of [5]phenacene or [7]phenacene interfacial layer resulted in a slight reduction in the field-effect mobility. The insertion of a [5]phenacene interfacial layer to the [7]phenacene OTFTs showed no effect, whereas in [7]phenacene OTFTs adding [6]phenacene interfacial layer led to a slight increase in the field-effect mobility.

Almost all combinations of the semiconductor and interfacial material showed a reduction in the threshold voltage compared to OTFTs with no interfacial layer. The greatest reduction in threshold-voltage value is detected in the combination of [5]phenacene and [7]phenacene. The threshold voltage decreased by about 0.4 V in OTFTs with [5]phenacene semiconductor and [7]phenacene interfacial layer. Also a reduction of the threshold voltage by about 0.55 V was obtained by combining [7]phenacene semiconductor and [5]phenacene interface material.

OTFTs with [6]phenacene semiconductor in combination with [5]phenacene or [7]phenacene interfacial layer exhibit a decrease in the on-state drain current values. However, [5]phenacene or [7]phenacene OTFTs with the interfacial layer between the source/drain contacts and the semiconductor had a slight increase in the on-state drain current.

The off-state current is slightly increased upon the insertion of [7]phenacene or [6]phenacene as interfacial layer, with the highest increase observed for the [7]phenacene semiconductor and [6]phenacene interfacial layer in narrow-gate OTFTs. The addition of [5]phenacene interfacial layer to [6]phenacene or [7]phenacene OTFTs decreased the value of the mean off-state current. Employing [6]phenacene as the semiconductor layer and [5]phenacene as the interface material resulted in higher change (reduction of about one order of magnitude) compared to when [7]phenacene is used as the interface material with the same

semiconductor, i.e. [6]phenacene. This resulted in a slight increase in the mean off-state current by about 3×10^{-10} A.

Finally, an increase in the subthreshold slope was observed for all combinations of semiconductor and interfacial material with the exception of [6]phenacene semiconductor combined with [5]phenacene interfacial layer which resulted in a slight reduction in the subthreshold slope from 616 to 581 mV/decade. The highest increase was observed when [7]phenacene semiconductor was combined with [6]phenacene interfacial material.

To summarise, it can be concluded that the addition of the interfacial layer does not lead to a measurable improvement of the transistor parameters with the exception of the threshold voltage.

Table 5.1 summarizes the results of the measurements of the output characteristics for various phenacene transistors, with and without the source/drain interfacial layer. The measurements from DNTT OTFTs fabricated alongside the phenacene OTFTs are also shown for comparison. The source/drain contacts are called 'Ohmic' when the drain current increased linearly for small V_{DS}, for V_{GS} up to −6 V as shown in Figure 5.7 (data in red). Otherwise, the term 'Non-ohmic' was used for the source/drain contacts when the drain current increased non-linearly (a diode-like behaviour) for small V_{DS}, as shown in Figure 5.7 (data in green).

Table 5.1: Properties of the source/drain contacts for various OTFTs.

		Interfacial layer			
		None	**[5]phenacene**	**[6]phenacene**	**[7]phenacene**
Semiconductor	**[5]phenacene**	Ohmic	×	not available	Ohmic
	[6]phenacene	Non-ohmic	Non-ohmic	×	Non-ohmic
	[7]phenacene	Non-ohmic	Non-ohmic	Non-ohmic	×
	DNTT	Ohmic	Ohmic	not available	Ohmic

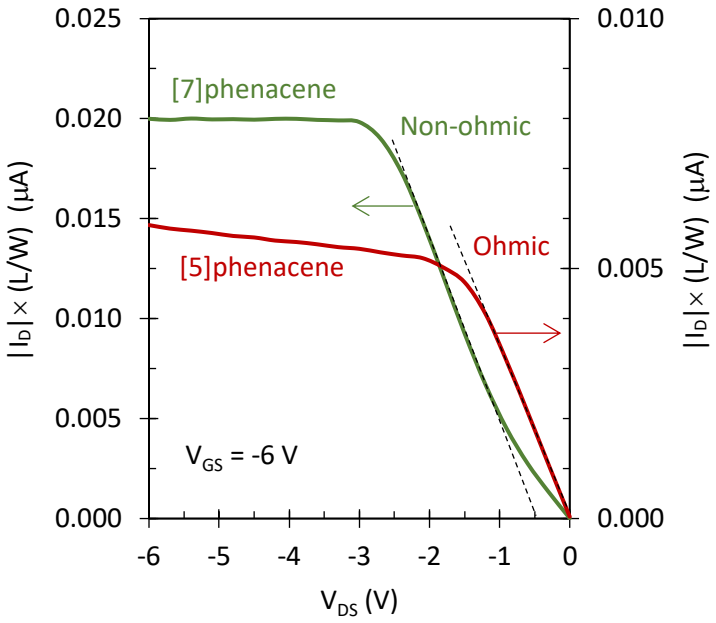

Figure 5.7: 'Ohmic' (red) and 'Non-ohmic' (green) behaviour in transistor output characteristics.

As shown in Table 5.1, Ohmic source/drain contacts were observed for transistors based on DNTT and [5]phenacene, regardless of whether the interfacial layer was applied. On the other hand, non-ohmic behaviour of the source/drain contacts was displayed by OTFTs based on [6]phenacene and [7]phenacene. No fundamental change to this behaviour was observed for any [n]phenacene after the insertion of the thin interfacial layer between the source/drain contacts and the organic semiconductor.

5.3.4 [n]Phenacene transistors on glass with 'vacuum-prepared' and 'solution-prepared' gate dielectric

The parameters of the 'standard' OTFTs fabricated on glass substrate are summarized in Table 5.2. Here, two types of gate dielectrics, either solution- or vacuum-prepared were used. Additionally, a larger thickness of the semiconductor layer compared to OTFTs

fabricated on PEN was employed. The OTFTs were fabricated side by side with the exception of the gate dielectric layer. The table shows the transistor parameters, namely the field-effect mobility μ and the threshold voltage V_T in the saturation regime, the on-state drain current I_{ON} (at $V_{GS} = V_T - 1$ V and $V_{DS} = -5$ V), the off-state drain current I_{OFF} (the smallest drain current at $V_{DS} = -5$ V), leakage current I_G (at $V_{GS} = -5$ V), and the d.c. transconductance. The gate-dielectric capacitance per unit area C_{diel}, for solution- and vacuum-prepared dielectric was 0.70 and 0.30 μF/cm2 respectively.

Table 5.2: Parameters of OTFTs on glass.

Dielectric	**Semiconductor**	**μ (cm2/V·s)**	**V_T (V)**	**$\lvert I_{ON}\rvert$ (A) @ $V_T - 1$ V**	**$\lvert I_{OFF}\rvert$ (A)**	**$\lvert I_G\rvert$ (A)**	**G_m (μS)**
Solution-prepared	[5]phenacene	0.0015	–3.96	2.36×10^{-8}	1.94×10^{-13}	1.77×10^{-11}	0.05
	[6]phenacene	0.025	–3.89	4.34×10^{-7}	7.91×10^{-13}	2.26×10^{-10}	1.06
	[7]phenacene	0.27	–3.40	4.17×10^{-6}	1.88×10^{-12}	7.83×10^{-11}	12.2
Vacuum-prepared	[5]phenacene	0.0093	–5.49	6.40×10^{-8}	5.76×10^{-14}	1.98×10^{-7}	0.01
	[6]phenacene	0.010	–4.95	9.26×10^{-8}	1.09×10^{-13}	2.15×10^{-10}	0.05
	[7]phenacene	0.031	–4.53	1.95×10^{-7}	3.36×10^{-13}	3.38×10^{-10}	0.12

As seen with the OTFTs fabricated on PEN, the best electrical performance, i.e. the highest field-effect mobility and the smallest threshold voltage, was achieved for [7]phenacene transistors. With the length of the phenacene molecule increasing, the field-effect mobility increases, the threshold voltage decreases, the on-state drain current increases, and the off-state drain current also increases for both gate dielectrics. Moreover, OTFTs with solution-prepared gate dielectric showed a bigger change in the field-effect mobility, rising from 0.0015 cm2/V·s for [5]phenacene to 0.27 cm2/ V·s for [7]phenacene, compared to the transistors with vacuum-prepared dielectric where μ increased from 0.0093 cm2/V·s for [5]phenacene to 0.031 cm2/V·s for [7]phenacene. Furthermore, OTFTs with solution-

prepared gate dielectric exhibit smaller threshold voltages for all [n]phenacenes. On the other hand, OTFTs with vacuum-prepared gate dielectric resulted in lower off-state drain currents for all [n] phenacenes. Regarding the gate leakage current, with the exception of the vacuum-prepared OTFTs with [5]phenacene, all other transistors exhibit the gate leakage current below or around 0.1 nA. Overall, the gate leakage current shows a slight reduction with the increasing length of the phenacene molecule. Finally, the transconductance increases as the length of phenacene increases for both the solution- and vacuum-prepared OTFTs, although the former exhibits higher values of G_m compared to the latter. Regardless of the dielectric preparation [7]phenacene transistors exhibit the highest G_m. Overall, the solution-prepared [7]phenacene OTFTs have the highest G_m of 12.2 μS.

Comparing the standard OTFTs on glass to those fabricated on PEN (all with the vacuum-prepared dielectric), one observes that the former exhibit field-effect mobilities similar to those of the narrow-gate OTFTs on PEN. At the same time, the standard OTFTs on glass have larger threshold voltages than the narrow-gate OTFTs on PEN.

5.4. Discussion

For OTFTs fabricated on flexible PEN substrates, the wide-gate Au/[7]phenacene/C_{18}PA/AlO_x/Al devices exhibited the best performance, with an average field-effect mobility of 0.092 $cm^2/V{\cdot}s$ and a threshold voltage of –4.32 V. On glass substrates, the transistors that combined [7]phenacene with C_{18}PA prepared from solution exhibited the highest mobility of 0.27 $cm^2/V{\cdot}s$ and a threshold voltage of –3.40 V. These field-effect mobilities are similar to those realized in previous studies of low-voltage [n]phenacene OTFTs [103,107]. However, the threshold voltages achieved here are smaller and the OTFTs exhibit improved contact properties. Previously, [5]phenacene OTFTs with a ZrO_2 gate dielectric showed a field-effect mobility of 0.036 $cm^2/V{\cdot}s$ and a threshold voltage

of –6.7 V, [5]phenacene OTFTs with a HfO_2 gate dielectric exhibited a mobility of 0.015 $cm^2/V{\cdot}s$ and a threshold voltage of –6.9 V, [5]phenacene OTFTs with a $Ba_xSr_{1-x}TiO_3$ gate dielectric had a mobility of 0.0019 $cm^2/V{\cdot}s$ and a threshold voltage of –4.0 V, [5]phenacene OTFTs with a parylene/Ta_2O_5 gate dielectric showed a mobility of 0.54 $cm^2/V{\cdot}s$ and a threshold voltage of –6.2 V [107], and [6]phenacene OTFTs with a parylene/Ta_2O_5 gate dielectric exhibited a mobility of 0.09 $cm^2/V{\cdot}s$ and a threshold voltage of –5.4 V [103]. However, in most of the previously reported low-voltage [n]phenacene OTFTs, the output characteristics exhibited a strong diode-like behaviour for drain-source voltages of up to a few volts. The comparison of our low-voltage transistors and those published previously is summarised in Table 5.3.

Table 5.3: Field-effect mobility and threshold voltage of low-voltage thin-film transistors based on [5], [6], and [7]phenacene.

Semiconductor	Gate dielectric	Mobility ($cm^2/V{\cdot}s$)	Threshold voltage (V)	Reference
[5]phenacene	$C_{18}PA/AlO_x$	0.0015	−3.96	this work
[6]phenacene	$C_{18}PA/AlO_x$	0.025	−3.89	this work
[7]phenacene	$C_{18}PA/AlO_x$	0.27	−3.40	this work
[5]phenacene	ZrO_2	0.036	−6.7	[107]
[5]phenacene	HfO_2	0.015	−6.9	[107]
[5]phenacene	$Ba_xSr_{1-x}TiO_3$	0.0019	−4.0	[107]
[5]phenacene	Parylene/Ta_2O_5	0.54	−6.2	[107]
[6]phenacene	Parylene/Ta_2O_5	0.09	−5.4	[103]

Modifying the interface between the source/drain contacts and the semiconductor layer did not improve the transistor performance and only a slight reduction in threshold voltage was observed. The field-effect mobility is about the same, regardless of the presence of the interfacial layer, indicating that this property is controlled mainly by the molecular arrangement of the [n]phenacene molecules within the semiconductor layer. In fact, in all cases the mobility increases with increasing length of the [n]phenacene molecules, most

likely as a result of stronger intermolecular interactions in the case of the longer [n]phenacenes. Previously it was shown that the mobility in single-crystal transistors based on [n]phenacene increases as [n] rises from 5 to 9, due to the stronger π-π interaction between the molecules for larger [n] [114-115]. The maximum mobility reported for single-crystal transistors with SiO_2 gate dielectric and [9]phenacene was 10.5 $cm^2/V \cdot s$ [115]. On the other hand, such trend was previously not apparent in [n]phenacene thin-film transistors. This was ascribed to the formation and quality of the thin film and the presence of defects that may affect the mobility in OTFTs [115-116]. Our current results show a correlation between the mobility and the length of the phenacene molecule even in the case of thin-film phenacenes. This may result from the fact that the surface energy of the phosphonic acid is very low and, consequently, the interaction between the phenacene molecules plays role during the deposition of the phenacene layer.

Generally, higher field-effect mobility should be possible when larger transfer integral and lower reorganization energy between the neighbouring orbitals exist, which results from increased intermolecular overlap of the orbitals as the π-conjugated dimension increases, i.e. with the rising number of the benzene rings [99,117-118]. This was also reported in [119] where different computational methods were used to assess the charge transport properties of [n]phenacenes (n = 6 to 10), concluding that upon the insertion/addition of an extra benzene ring, the charge-transfer mobility increases and thus the synthesis of longer phenacene molecules is encouraged. As stated in the previous paragraph, the thin-film transistors presented in this chapter have shown an increase in the mobility with increased length on phenacene, although other factors may have played a role because the mobility did not reach the value reported for single-crystal phenacenes.

One can also observe that the preparation method of the phosphonic acid monolayer affects the field-effect mobility of the OTFTs. Even though the solution- and vacuum-

prepared C_{18}PA SAMs have similar water contact angles (macroscopic properties) [69,120], they are likely to differ on the microscopic scale. One would predict that the density of vacuum-prepared SAMs is lower than that of their solution-prepared counterparts as a result of the laws that govern physical vapour deposition. The microscopic changes in the morphology of the vacuum-prepared SAMs have profound effect on the field-effect mobility of the OTFTs based on DNTT, even though these SAMs have similar water contact angles and surface energies [69]. Consequently, it is not surprising that the solution- and vacuum-prepared SAMs lead to [n]phenacene OTFTs with different field-effect mobilities.

The non-linear response of the drain current for small source-drain voltages suggests the presence of carrier injection/extraction barriers. Schottky barrier may be formed at the interface between metal and semiconductor if their work functions are different and the interface is free of carrier traps (the presence of such traps will help the carriers to move/tunnel across the energy barrier, giving rise to Ohmic-like contact behaviour). For Ohmic contacts, the Fermi level of the source/drain metal should be aligned with the HOMO level of the organic semiconductor in p-type transistors and LUMO level in case of n-type transistors [121], otherwise a non-linear (non-Ohmic or Schottky) behaviour may occur for small V_{DS}, leading to diode-like observation in the transistor output characteristics.

Different combination of metals and semiconductors will establish different level of energy barrier heights at their interface due to their different energy levels. Recently in [122], C_8-BTBT with HOMO level of 5.7 eV and source/drain contacts made of silver (Ag) with a work function modified from 4.3 to 5.3 eV were employed to fabricate Schottky barrier organic thin-film transistor (SB-OTFTs). Similarly, the observation of the non-ohmic contacts in several [n]phenacene OTFTs presented in this chapter can results from a larger difference between the work function of Au (~5.1 eV [103]) and the HOMO of [n]phenacene (ranging from 5.5 to 5.7 eV as [n] increased from 5 to 7 [100,104]). Consequently, it is not

surprising to observe non-linear behaviour for OTFTs with longer phenacene molecules, while such behaviour is absent in DNTT transistors (HOMO of ~5.3 eV [123]). In fact, as the length of the phenacene molecule increases (the number of benzene rings increases), the band gap decreases and the HOMO level deepens. Consequently the difference between the Fermi level of Au and HOMO level of the [n]phenacene increases, providing an opportunity for the Schottky barrier formation. Nevertheless, such non-linear behaviour was absent in the extremely extended [10]phenacene and [11]phenacene OTFTs with Au source/drain contacts [116], possibly because the contact resistance was reduced by the insertion of F_4TCNQ between the Au and [n]phenacene.

Finally, the combination of [n]phenacene with thin bi-layer of $AlO_x/C_{18}PA$ as the gate dielectric resulted in low-voltage operation of the OTFTs. In short, high capacitance was yielded through the use of such gate dielectric, leading to the low-voltage operation. Further optimization of the source/drain contacts and/or the use of [n]phenacenes with n > 7 hold promise for future low-voltage OTFTs based on such organic semiconductors.

5.5. Summary

In this chapter, for the first time, the use of the $AlO_x/C_{18}PA$ bi-layer for low-voltage OTFTs with [5], [6] and [7]phenacene was investigated. These transistors were fabricated on two different substrates – glass and flexible PEN. Three transistor structures were fabricated and tested, a 'standard' structure on glass substrates with a channel length of 30 μm and a channel width of 1 mm (W/L ~ 33), a 'wide-gate' multi-finger structure on PEN substrates with a channel length of 50 μm and a channel width of 18.23 mm (W/L ~ 365), and a 'narrow-gate' multi-finger structure also on PEN substrates with a channel length of 20 μm and a channel width of 4.03 mm (W/L ~ 202). In addition, in some cases, the preparation of the bi-layer gate dielectric was executed in two different ways – solution-prepared and

vacuum-prepared – and a modification of the interface between the source/drain contacts and the semiconductor was implemented by inserting a thin layer of [n]phenacene that had a different length than that used for the semiconductor layer. The field-effect mobility is found to increase with increasing length of the conjugated [n]phenacene core with no regard to the substrate and the transistor structure, leading to the best performance for [7]phenacene. For OTFTs fabricated on PEN substrates, Al/AlO_x/C_{18}PA/[7]phenacene/Au with wide-gate multi-finger structure exhibited the best performance with an average filed-effect mobility of 0.092 cm^2/V·s and a threshold voltage of −4.32 V. For OTFTs fabricated on glass substrates, the [7]phenacene OTFTs with standard structure and solution-prepared gate dielectric delivered the best performance in terms of the highest mobility of 0.27 cm^2/V·s, the lowest threshold voltage of −3.40 V, and the highest transconductance of 12.2 μS. Although the field-effect mobilities are similar to those reported in the past for low-voltage [n]phenacene OTFTs, other improvements were achieved. These include a nearly hysteresis-free transfer characteristics, a decrease in the threshold voltage, and substantially improved source/drain charge carrier injection properties. Only a slight decrease in the threshold voltage was observed with the introduction of the interfacial contact layer and no other significant improvements in the OTFT performance were observed. Further use of [n]phenacenes with n > 7 holds promise for future high performance low-voltage OTFTs based on such organic semiconductors with a consideration to optimise the source/drain contacts.

Chapter 6

Compact model for OTFTs with multi-finger source/drain contacts

This chapter introduces a compact model developed for the multi-finger organic thin-film transistors with high transconductance. The chapter provides the mathematical description of the model together with the steps taken to validate this model and test its accuracy under different d.c. and low-frequency a.c. circuit conditions. The chapter outline is as follows. Firstly, an introduction and details of the model and its implementation are elaborated in Sections 6.1 and 6.2 respectively. Section 6.3 presents the results obtained for d.c. and a.c. transistor measurements. Finally, the discussion is given in Section 6.4 and a brief summary is provided in Section 6.5.

6.1. Introduction

The commercial success of thin-film transistors based on polycrystalline and hydrogenated amorphous silicon [124] was accompanied by an extensive effort devoted to the development of thin-film transistor models that were needed for the subsequent circuit design. Such models were later extended to and adopted for other thin-film transistor technologies including OTFTs. The rapid growth of OTFT applications initiated the need for circuit-level integration of these transistors rather than the narrow transistor-level investigation; hence, rising the importance of OTFT compact model development [125-126].

To accurately capture the physical performance of the device, physical transistor models are needed; however, they tend to be fairly complex and require depth of knowledge of the transistor physical behaviour. Here, the challenge for OTFTs is even greater because many device architectures and a large combination of gate dielectric materials and organic semiconductors can be used. In addition, the variety of the deposition techniques enabled by the organic materials and low-temperature fabrication leads to even greater variability. Consequently, a simpler approach is to use semi-empirical mathematical equations which can accurately describe the transistor drain current based on the voltages applied to the transistor terminals. Such models result in shorter computation time, while predicting, with high precision, the operating characteristics of the transistors via computed empirical/fitting parameters.

Different OTFT compact models were developed focusing on particular features and principles of the OTFTs and/or to adopt simplifications for providing an accessible analysis [126-129]. Capacitance modelling of OTFT [128], a d.c. model considering Schottky barrier limitation on carrier injection in short channel transistors and a small signal a.c. non-quasi-static model addressing parasitic capacitances in printed devices which exhibit large process tolerances are examples of such models [130].

To help with the design of flexible sensors and circuits implementing low-voltage OTFTs with multi-finger contacts, a semi-empirical model was developed and tested on DNTT OTFTs. For this model, the measured transistor transfer characteristics are used to produce the mathematical expression for the OTFT drain current as a function of the voltages applied on OTFT terminals. The fitting procedure of the drain current covers all transistor operating regimes, i.e below and above-threshold operation and the off-state. Once the drain current is obtained, it can be used to model the d.c. and low-frequency a.c. transistor drain current as well as the output voltage of a common-source amplifier based on such a transistor.

A compact model, tested on the transistors discussed in Chapter 4, was implemented in Matlab Simulink environment. The semi-empirical model requires four fitting parameters that are extracted by fitting the measured transistor transfer characteristics (I_D-V_{GS}) in both linear and saturation regimes of the transistor. This method is valid even if only transfer characteristic in saturation regime is available; however, slightly higher accuracy is obtained if two transfer characteristics, one corresponding to the linear regime and the other to the saturation regime, are used.

The model was validated on OTFTs with different geometries. In addition, the validation was executed in the following three ways:

a) Transistor output characteristics (I_D-V_{DS}) were calculated and compared to the measured data.
b) The transistor drain current was calculated for 1 Hz sinusoidal gate voltage and compared to the measured drain current.
c) Output voltages of a common-source transistor amplifier were calculated and compared to the experimental data.

As part of the validation procedure the numerical errors, i.e. the difference between the calculated/modelled and measured values, were calculated to assess the accuracy of the model.

6.2. Details of the model and its implementation

A compact model proposed in [27] served as a foundation for the model presented in this chapter. The model is based on the well-established and accepted thin-film transistor charge drift theory, as explained in [27]. This model is semi-empirical and involves the use of five 'fitting' parameters determined from the experimental data. Our modified version of the model reduces the number of fitting parameters from five to four. In addition, the source/drain contact resistance was neglected, to allow for shorter computation time. The model was implemented in Matlab Simulink environment since it is commonly used numerical and mathematical software in the engineering and science fields.

The developed compact model computes the OTFT drain current based on a set of measured transfer characteristics in linear and saturation regimes or saturation regime only. Equation (6.1) defines the modelled drain current I_D as follows:

$$I_D = \frac{W}{L\left(1-\frac{\Delta L}{L}\right)} \cdot \frac{\mu_o}{\left(\frac{V_{SS}}{2+\gamma}\right)^{\gamma}} \cdot C \cdot \left[\frac{(VS_{EODR})^{(\gamma+2)}}{\gamma+2} - \frac{(VD_{EODR})^{(\gamma+2)}}{\gamma+2}\right] \tag{6.1}$$

where VS_{EODR} and VD_{EODR} are the effective voltage overdrive on source and drain side respectively. The voltage overdrive represents the incorporation of the subthreshold regime in the model and $\frac{\Delta L}{L}$ represents the channel length modulation interpolation. They are defined as:

$$VS_{EODR} = V_{SS} \ln\left\{1 + \exp\left[\frac{V_G - V_T - V_S - (V_G - V_S)\delta_{VT}}{V_{SS}}\right]\right\} \tag{6.2}$$

$$VD_{EODR} = V_{SS}\ln\left\{1+\exp\left[\frac{V_G-V_T-V_D-(V_G-V_D)\delta_{VT}}{V_{SS}}\right]\right\} \tag{6.3}$$

$$\frac{\Delta L}{L} = \lambda(V_D - V_S)\cdot\frac{(V_D-V_S)+V_{GT\Delta L}}{2(V_D-V_S)+V_{GT\Delta L}} \geq 0 \tag{6.4}$$

Here V_G, V_D, and V_S are voltages on the gate, drain and source terminals respectively, W is the channel width, L the channel length, C the gate dielectric capacitance and V_T the threshold voltage of the transistor. The specific transistor determines W, L, C and V_T, as well as the transistor off-current. Furthermore, $V_{GT\Delta L} = \max(V_G - V_T,\ 0.01\,V)$ and λ is the channel length modulation. The four empirical/fitting parameters are the subthreshold slope V_{SS}, mobility enhancement factor γ, low-field mobility μ_o, and the threshold voltage bias sensitivity δ_{VT}.

The values of the above mentioned fitting parameters are found by employing an objective function defined as a mean square error (MSE) of the measured and fitted data. A genetic algorithm with a hybrid option (a second optimization function) is used to minimise this function. The second optimisation function is a derivative-free method [131] and it starts with the final solutions found by the genetic algorithm as initial points. This technique was used to speed up calculation and optimise the solution-finding process, i.e. to determine the four fitting parameters. The genetic algorithm works by generating a population of possible individual solutions to an optimization problem, then repeatedly altering the population to progress toward an optimal solution. This is an iterative process producing a population per iteration known as generation and through several successive generations, an optimal solution is reached. Initially, the first population is generated randomly, then the algorithm improves it by creating the next generation 'child' using individuals from the current 'parents' population. This is executed by using three methods which are: selection, crossover and

mutation at each step of the next generation production process. Selection is retaining individual solutions of the best performance to contribute to the population of the next generation. Crossover is combining and selecting common similarities of individual solutions from two parents (existing population) to produce the child for the next generation. Finally, mutation is taking a few individual solutions from parents and altering it to take on a random value to form the child generation; this helps keeping diversity with each new created generation and increases the likelihood that individuals with better fitness values are produced. The objective function is the fitness function that is being optimized by the genetic algorithm. The value of the objective function is evaluated for each generation. Eventually, the termination of the algorithm occurs when a specified maximum number of generations or high fitness level has been reached [132-134].

There are two main ways in which the genetic algorithm varies from a classical optimization algorithm (derivative-based). Firstly, it produces a population of points for each iteration, while the classical algorithm only produces a single point. Consequently, in genetic algorithm the best point in the population evolves towards an optimal solution whereas in the latter it is a sequence of points to reach optimal solution. Secondly, in the genetic algorithm the random number generators are used to compute and select the next population, as described previously, however, in the classical algorithm the selection of the next point in the sequence is through deterministic computation [132,135].

In this chapter, the objective function was defined to minimise the mean square error between the fitted data and the measured experimental data. Hence, the genetic algorithm finds variables (fitting parameters) that satisfy this condition.

The main steps of the developed Matlab code are as follows:

1. Uploading the experimental data and physical parameters from Excel spreadsheet, for a specific transistor. The programme reads and sorts this data accordingly.

2. Fitting the data to determine the four fitting parameters for this transistor.
3. Using the obtained fitting parameters to model the drain current of the transistor for different bias conditions of V_G and V_D in d.c. or a.c.
4. Finally, the accuracy of the model is tested by replicating a variety of experimental data including transistors with wide-gate and narrow-gate structures on PEN or glass and under different circuit condition. More details are given in the next section.

6.3. Results

The OTFT data used to develop and test the model were taken from the prior experiments performed with the multi-finger OTFTs (see Chapter 4). The obtained modelled data was compared to the measured data for three different tests described next.

6.3.1 Modelling of d.c. transistor characteristics

Figure 6.1 shows the measured and simulated transfer characteristics of a wide-gate transistor with W = 18.23 mm and L = 40 μm and a narrow-gate transistor with W = 4.03 mm and L = 12.30 μm in linear and saturation regimes. The corresponding fitting parameters shown in Table 6.1 were used to simulate the output characteristics of these transistors. Their comparison to the measured data is shown in Figure 6.2. The results show that this compact model is able to reproduce the electrical d.c. performance of the transistors with high precision.

Table 6.1: Parameters for wide-gate and narrow-gate transistors of Figures 6.1 and 6.2.

		Wide-gate transistor	Narrow-gate transistor
Transistor parameters extracted from measurement	W (mm)	18.23	4.03
	L (μm)	40	12.3
	C (F/cm2)	4.23×10^{-7}	4.23×10^{-7}
	V_T (V)	0.460	0.597
	λ	0.0001	0.06
Below threshold fitting parameters	V_{SS}	0.113	0.043
	γ	0.0002	-1.127
	μ_o	0.104	0.190
	δ_{VT}	0.390	0.065
Above threshold fitting parameters	V_{SS}	0.087	0.095
	γ	-0.313	-0.314
	μ_o	0.531	0.609
	δ_{VT}	-0.062	-0.101

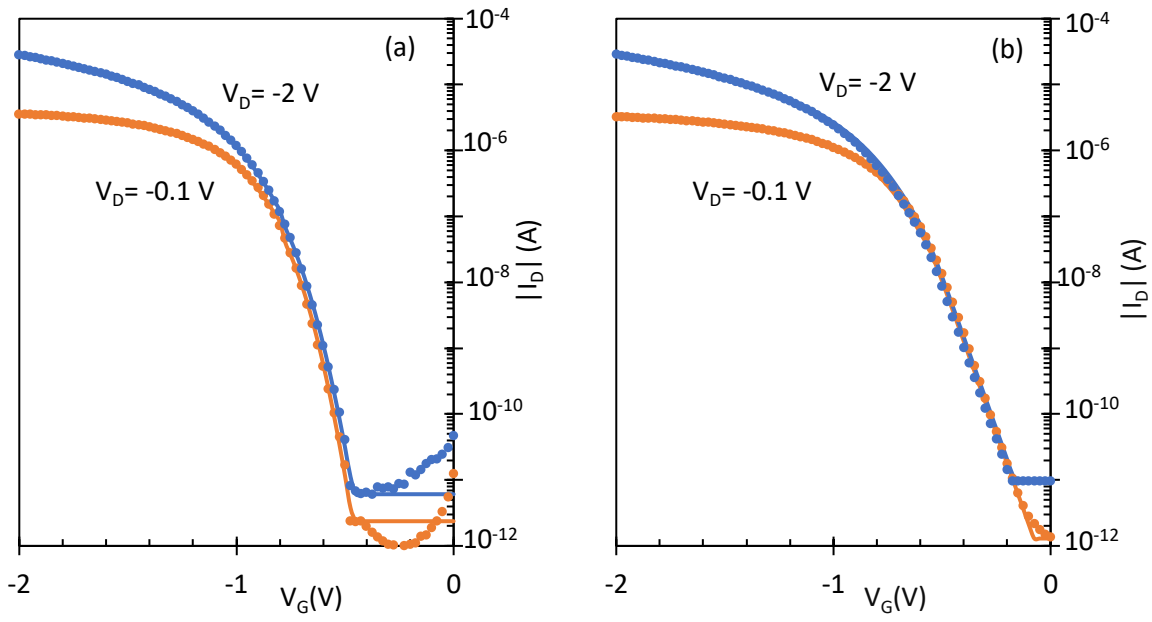

Figure 6.1: Transfer characteristics of wide- (a) and narrow-gate (b) transistors. The solid lines represent the model and the points the measured data.

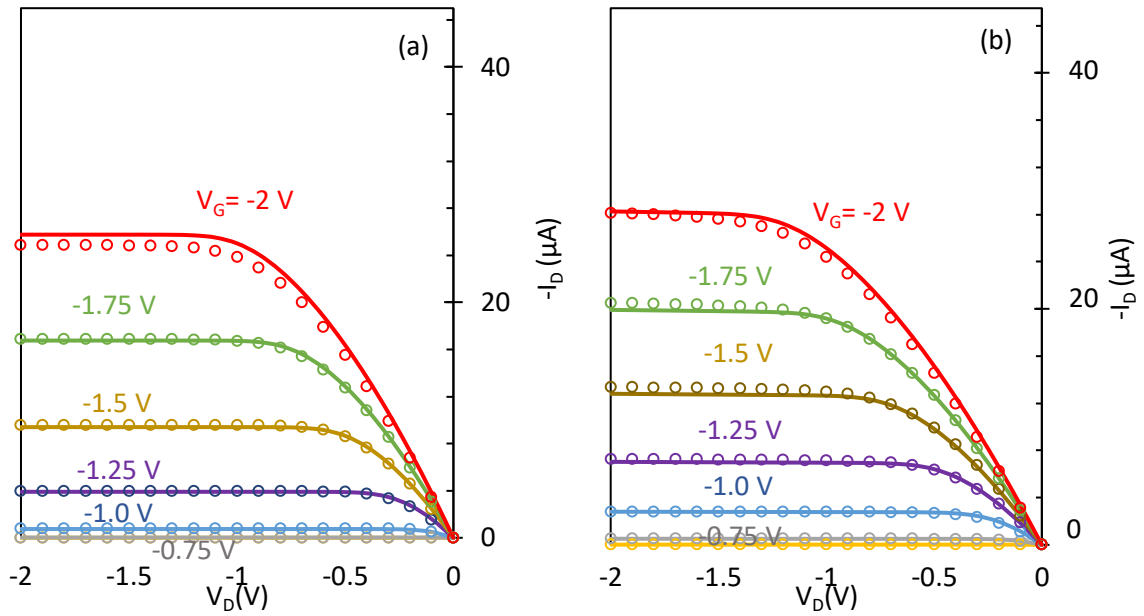

Figure 6.2: Output characteristics of wide- (a) and narrow-gate (b) transistors. The solid lines represent the model and the points the measured data.

6.3.2 Modelling of low-frequency a.c. transistor outputs

6.3.2.1 Transistor a.c. drain current

In the next step, the transistor transconductance measurements (refer to Chapter 3 for the circuit configuration) were simulated. In the corresponding experiment the gate voltage was a 1 Hz sine wave of 0.2 V peak-to-peak and an off-set of –2 V, while the drain voltage was kept constant at –2 V and the source electrode was grounded. The measured and simulated a.c. drain current of six transistors with different *W* and *L* are shown in Figure 6.3.

The peak-to-peak values of the measured and simulated drain current of these transistors are summarized in Table 6.2. The results show that all simulated peak-to-peak values were slightly greater than the experimental values for a.c. drain current, the errors were found to range from 1.7% to 11.6%.

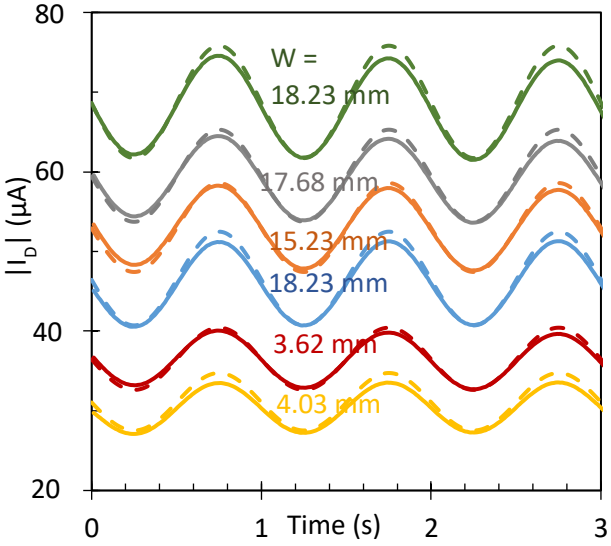

Figure 6.3: A.c. drain current for transistors with various *W*. The solid lines correspond to the measured data and dashed lines to the model.

Table 6.2: Peak-to-peak values and errors for measured and simulated data of Figure 6.3.

W (mm)	**18.23**	**17.68**	**15.35**	**18.23**	**3.62**	**4.03**
I_{Dpp} meas (μA)	13.5	11.3	11.0	10.7	7.7	6.5
I_{Dpp} model (μA)	14.1	11.6	11.2	11.8	7.8	7.2
Error (%)	4.3	2.3	1.7	9.5	2.0	11.6

6.3.2.2 Output voltage of a common source transistor amplifier

The output from the common-source amplifier (see Chapter 3 and Figure 3.7) was simulated for different values of V_{DD} and R_d. The results are shown in Figures 6.4 and 6.5. Furthermore, the comparison of the peak-to-peak output voltages for the various V_{DD} and R_d combinations of this transistor amplifier are shown Table 6.3 and Table 6.4 respectively.

It can be noted that the error in the peak-to-peak voltage increased with decreasing V_{DD} for R_d = 47 kΩ, which resulted in the highest percentage error for V_{DD} = –2 V. However for R_d = 5.6 kΩ, the highest percentage error is found for V_{DD} = –3.5 V and no direct relation

is observed between V_{DD} and the peak-to-peak error. Generally, the measured peak-to-peak output voltages were slightly lower when compared to the simulated ones. The high accuracy

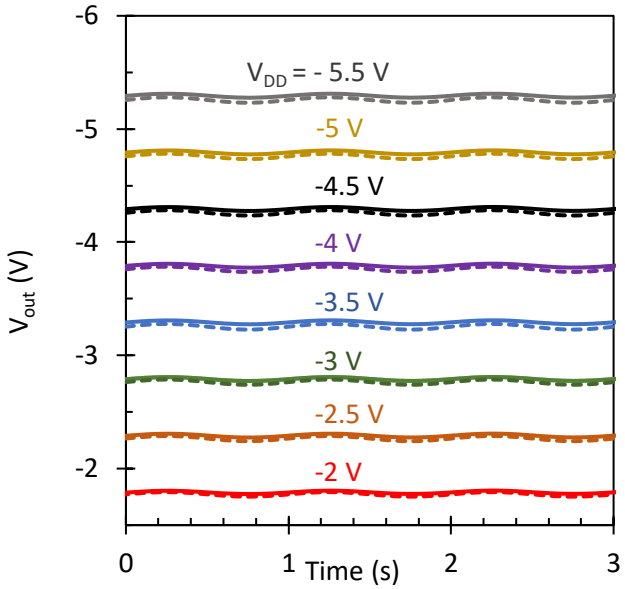

Figure 6.4: Output voltage of the transistor amplifier for various V_{DD} and R_d = 5.6 kΩ. The solid lines correspond to the measured data and dashed lines to the model.

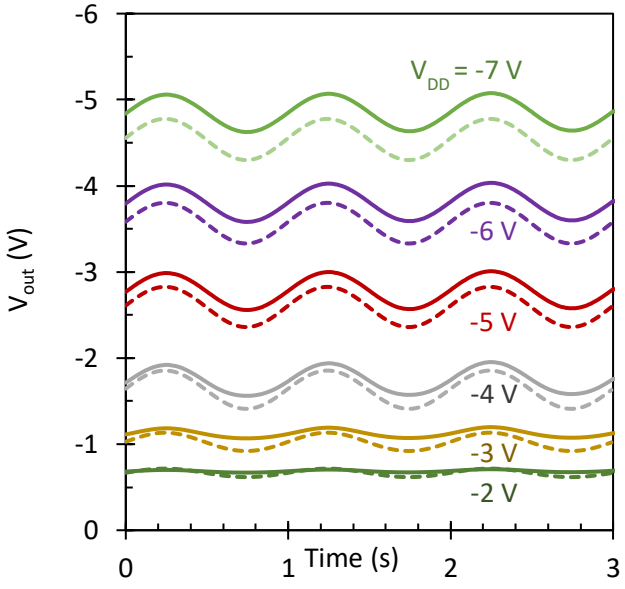

Figure 6.5: Output voltage of the transistor amplifier for various V_{DD} and R_d = 47 kΩ. The solid lines correspond to the measured data and dashed lines to the model.

Table 6.3: Peak-to-peak values and errors for measured and simulated data of Figure 6.4.

V_{DD} (V)	-2	-2.5	-3	-3.5	-4	-4.5	-5	-5.5
V_{OUTpp} meas (V)	0.0312	0.0350	0.0355	0.0350	0.0365	0.0360	0.0360	0.0360
V_{OUTpp} model (V)	0.0398	0.0451	0.0458	0.0496	0.0461	0.0463	0.0469	0.0475
Error (%)	27.5	29.0	29.1	41.8	26.3	28.7	30.3	32.0

Table 6.4: Peak-to-peak values and errors for measured and simulated data of Figure 6.5.

V_{DD} (V)	-2	-3	-4	-5	-6	-7
V_{OUTpp} meas (V)	0.040	0.130	0.392	0.450	0.454	0.453
V_{OUTpp} model (V)	0.099	0.213	0.444	0.466	0.472	0.477
Error (%)	148.8	63.0	13.4	3.7	4.1	5.5

achieved for d.c. output characteristics could be due to the fact that both the linear and saturation regimes were available for the simulations in Figures 6.1 and 6.2. However, only the transfer characteristics in saturation regime were available for the a.c. results shown in Figures 6.3, 6.4 and 6.5. Consequently, the error is increased when the transistor operates in the linear regime. Finally, one should note that while the error seems high for the low peak-to-peak voltages, the actual differences between the measured and simulated values are less than 15 mV for the data of Figure 6.4 and less than 85 mV for the data of Figure 6.5.

6.4. Discussion

The model was built in Matlab to take advantage of a widely-used platform that provides easy debugging of the code and assessing of the obtained results and allows further development of the model. The future development is especially important because this current model serves as a first step toward simulating flexible sensors and circuits implementing organic transistors. Since Matlab is widely used in the engineering field, adding on other features and further development of the model will be possible. It is worth to remind the reader that this model is meant to use the available measured transfer

characteristics of a particular transistor along with its physical parameters to further predict/model this transistor's behaviour at different circuit conditions, i.e. what would be the transistor output (I_D) with different voltages applied on its terminals.

To model any transistor, i.e. represent its drain current mathematically, a set of eight fitting parameters is determined by fitting the transfer characteristics of that transistor. Out of these eight parameters four represent the below-threshold region and the other four the above-threshold operation (see Table 6.1). This separation into two regions dramatically improves the accuracy of the fit when the transistor operates below the threshold voltage. While this is not essential for the d.c. and a.c. simulations performed in this work, the accurate mathematical description of the transistor operation for low V_G (below the threshold) may become important in the future.

To measure the output characteristics the transistor must be turned on ($V_G > V_T$) and, consequently, only the four parameters describing the transistor behaviour above the threshold are needed to reproduce the curves. Similarly, all transistors were turned on during the a.c. transconductance measurement and were operating in the saturation. Therefore, the modelling of the a.c. transconductance and most of the output voltages of the transistor amplifier relied on the four fitting parameters describing the above-threshold region.

By implementing this approach of eight fitting parameters, the model is able to capture the transistor behaviour in all regimes of operation, as best demonstrated by Figure 6.1. The simulation of the d.c. transistor transfer and output characteristics showed high agreement between the measured and fitted data. The fitting of the a.c. transconductance and the output voltage of the common-source amplifier showed somewhat larger discrepancy between the measured values and the simulated data. Namely, the error in the peak-to-peak output voltages was higher compared to the error in the peak-to-peak transconductance. The former is likely caused by the circuit amplifying the error in the drain current I_D.

Considering the error of up to 148.8% for V_{DD} = –2 V and R_d = 47 kΩ in the transistor amplifier circuit, the future modifications of the existing model should focus on producing higher-accuracy fits to such measurements. One approach is to investigate and address the transistor contacts resistance as it was neglected in the current model. Furthermore, using transistor measurements that capture both the linear and saturation regimes provides more accurate fits (e.g., d.c. modelling) compared to cases when only the transfer characteristic in saturation was available (e.g., a.c. modelling). Therefore, one may consider measuring transfer characteristics in both linear and saturation regimes prior to modelling any a.c. transistor operation. Here, the measurements of the transfer characteristics in saturation regime, in comparison to the ones in linear regime, carry more weight in determining the fitting parameters as most of the parameters can be extracted from the saturation measurements.

The OTFT model adopted here is based on [27] that focuses on covering all transistor operation regimes using 5 fitting parameters. Our model reduced the number of the fitting parameters to four. The fifth parameter V_γ was omitted by expressing it via V_{SS} as $V_{SS}/(2+\gamma)$. The modelling results for the d.c. transistor characteristics suggest that this reduction in the number of the parameters did not affect the outcome of the fitting, as both procedures reproduce the transfer and output characteristics with high accuracy. The OTFT variety resulting from materials, structures, fabrication procedures, geometry, etc., led to the development of other models as well. However, these address different issues of the organic transistors and as such are not relevant for this work.

In this semi-empirical transistor model the extraction of the fitting parameters was enabled through the use of genetic algorithm built in Matlab. This comes with the advantage of fast computation time. To perform the computation/fitting, the physical parameters of the transistor (L, W, C, …) along with the measured transfer characteristics are imported to

Matlab. Currently, the physical parameters are obtained separately and entered by hand into Excel containing the data for the transfer characteristics. In the future, an approach to merge both processes may be investigated.

Sensitivity analysis was executed to assess the impact of the four fitting parameters on the drain current. To do that, the ranked correlation coefficient also known as Spearman's rank analysis which tests the strength and direction of monotonic association between two variables [136-137] was calculated. In addition, partial correlation method that finds the impact of a particular parameter on the output while removing the effect of the other parameters was executed. The current model accounts for all transistor operating regimes and a set of 8 parameters for below- and above-threshold regions is produced for a transistor. Thus, the analysis was performed for each region to test if the parameters will have different impact in different regions.

The obtained results can be summarised as follows: in the below-threshold region all parameters have negative correlation associated with the drain current, i.e. as the parameter increases the output (I_D) decreases. This can be inferred from equation (6.1); however the performed analysis provided statistical analysis for this relationship. The low-field mobility μ_o has the strongest impact on the drain current as a small change in μ_o will result in a bigger change in I_D with the ranked correlation coefficient r_s of –0.92. γ and δ_{VT} have a week association with I_D and V_{SS} has the least significant impact with r_s = –0.092. Furthermore, the partial correlation test resulted in the same order for the impact of the parameters on I_D that going from the strongest to the weakest is μ_o, γ, δ_{VT} and V_{SS}. The corresponding correlation coefficients for these parameters are r_s = –0.99, –0.92, –0.895, –0.68 respectively.

Similarly, for the above-threshold region the fitting parameters have negative correlation to I_D, indicated by the negative values of r_s. Contrary to the below-threshold regime, γ has the strongest effect on the drain current in the above-threshold region with the

correlation coefficient of –0.702, followed by μ_o, V_{SS}, and δ_{VT}. The last two have weak impact and their r_s values were less than –0.3 therefore can be regarded as insignificant. For the partial correlation test, the same order was observed, i.e. γ, μ_o, V_{SS}, and δ_{VT}, with r_s = –0.97, –0.96, –0.79 and –0.69 respectively.

6.5. Summary

This chapter presents compact model applied to multi-finger OTFTs based on DNTT presented in this thesis. Measurements of the transfer characteristics along with the transistor physical parameters form the input data for the compact model that computes the 'missing' fitting parameters. The data used to verify the model have been presented in previous chapters. To assess the ability of the model to reproduce variety of the experimental data, three validation procedures involving d.c. and a.c. measurements were used. For the d.c. measurements, the model was able to reproduce the measured transfer and output characteristics with high accuracy. The a.c. measurements included the transistor a.c. transconductance and the output voltage from the common-source transistor amplifier. The error between the measured and simulated peak-to-peak values ranged from 1.7% to 11.6% for the former and from 3.6% to 148.8% for the latter. While the model reproduces the OTFT d.c. characteristics well, additional work is needed to improve the accuracy of the low-frequency a.c. measurements in the future.

Chapter 7

Conclusion

In this chapter, Section 7.1 concludes the experiments conducted in the thesis and Section 7.2 presents suggestions for future work.

7.1. Conclusion

This thesis presented development and optimisation of low-voltage organic thin-film transistors with high transconductance. This involved the fabrication of low-voltage high-transconductance OTFTs based on DNTT and multi-finger source-drain contacts, the fabrication and investigation of similar transistor structures based on [n]phenacenes with

conjugated core length ranging from 5 to 7 and the development and implementation of semi-empirical transistor model in Matlab.

In the attempt to increase the transistor on-state current and transconductance, multi-finger source/drain contacts were used to provide high *W/L* ratio. Two different structures were used and called a wide- and narrow-gate OTFT with *W/L* of ~365 and ~202 respectively. Low-voltage p-type DNTT transistors and MIM structure were fabricated using such source/drain masks. The d.c. and a.c. electrical performance of the produced OTFTs was investigated. In addition, common-source transistor amplifiers based on such transistors were constructed by adding a resistor R_d with various values on the drain side of the transistor. The voltage gain of such amplifiers was measured.

The results indicate that these DNTT transistors exhibited threshold voltage between −0.4 and −0.8 V and field-effect mobility between 0.13 and 0.34 $cm^2/V{\cdot}s$. Owing to high *W/L* ratio their a.c. transconductance varied from ∼30 to ∼60 μS and scaled with the transistor dimensions. The multi-finger contacts structure offered a promising potential for high transconductance OTFTs without inducing high contact resistance typically associated with extremely reduced channel length. Both transistor types operate beyond 1 kHz and are suitable for analogue sensors applications. The transistor amplifier delivered a voltage gain in excess of 8 V/V for supply voltage V_{DD} of −12 V and R_d of 220 kΩ when transistor with medium value of transconductance of 37 μS was used. When the supply voltage was limited to −5 V, a gain of 2.2 V/V was achieved with R_d of 47 kΩ . Higher R_d required higher supply voltage V_{DD} but resulted in increased voltage gain.

Similar OTFTs, yet with different organic semiconductor layer were also investigated and studied. Namely, [5], [6] and [7]phenacene were used to fabricate OTFTs on two different substrates – glass and flexible PEN. Furthermore, three different source-drain contacts were tested (i.e. standard, wide- and narrow-gate OTFTs). In some cases, on the

glass substrate, the preparation of the bi-layer gate dielectric was executed in two different ways. The 'solution-prepared' dielectric refers to AlO_x prepared by plasma oxidation and $C_{18}PA$ assembled in solution, while the 'vacuum-prepared' dielectric refers to AlO_x prepared by UV/ozone oxidation and $C_{18}PA$ deposited in vacuum. In some OTFTs fabricated on PEN the interface between the source/drain contacts and the semiconductor was modified by inserting a thin layer of [n]phenacene that had a different length than that used for the semiconductor layer.

Regardless of the substrate and the transistor structure, the field-effect mobility was found to increase with increasing length of the conjugated [n]phenacene core, leading to the best performance for [7]phenacene transistors. The largest average field-effect mobility was 0.27 $cm^2/V{\cdot}s$ for transistors on glass and 0.092 $cm^2/V{\cdot}s$ for transistors on flexible PEN. Other improvements with respect to the previously reported low-voltage [n]phenacene OTFTs were: (a) nearly hysteresis-free transfer characteristics, (b) a decrease in the threshold voltage, and (c) improved source/drain charge carrier injection properties. The insertion of the interfacial contact layer only resulted in slight reduction in the threshold voltage. The highest transconductance of 12.2 μS was achieved for the [7]phenacene transistors with solution-prepared dielectric. This value is lower than the one achieved for DNTT transistors.

A compact model capable of replicating the transistor drain current was developed in Matlab and applied to the multi-finger OTFTs based on DNTT presented in this thesis. The transistor transfer characteristics along with the transistor physical parameters form the input data for the model that computes four fitting parameters to mathematically express the drain current as a function of the voltages applied on the OTFT terminals. The accuracy of the model was validated using our experimental data. Verification process involved three procedures including d.c. and a.c. transistor measurements.

The model was able to reproduce the measured d.c. data with high accuracy. However, the error between the measured and simulated peak-to-peak values ranged from 1.7% to 11.6% for the a.c. transconductance measurements and from 3.6% to 148.8% for the a.c. output voltage from the common-source transistor amplifier.

7.2. Future work

This thesis has summarised the development of low-voltage, high-transconductance OTFTs through the use of transistor structures with high *W/L* while building on the previous in-house DNTT OTFT know-how. In addition, similar OTFTs with [n]phenacene organic semiconductors of different length were also designed and fabricated.

The analysis of the results showed that further improvement would be desirable, especially for the [n]phenacene OTFTs. For instance, prior to this research the growth of DNTT was studied with respect to the deposition rate and temperature [72]. Therefore, it would be of interest to preform similar investigation for [n]phenacenes.

Several [n]phenacene OTFTs showed non-linear behaviour in I_D–V_{DS} at low values of V_{DS} (see Chapter 5) that is an indication of non-Ohmic source-drain contacts. This high 'contact resistance' has been previously studied in transistors with very short channel length. In [70], p-type contact doping was used in DNTT transistors with short channel length *L* to reduce the contact resistance and achieve more linear I_D–V_{DS} behaviour. The goal was to create excess holes in DNTT through the use of a dopant whose LUMO level falls near/below the HOMO level of the organic semiconductor. The authors have doped the source/drain contacts with Novaled NDP-9 (LUMO level of –5.3 eV) in DNTT (HOMO level of –5.33 ± 0.1 eV) based transistors. Consequently, it would be interesting to investigate the use of such p-type dopant in [n]phenacene transistors (HOMO level of –5.5 eV for [5]phenacene and [6]phenacene and –5.7 eV for [7]phenacene [100]) to improve the injection/extraction of the

charge carriers. Other dopants of interest include 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F_4-TCNQ) with LUMO level around –5.2 eV [70] which was employed previously in [6]phenacene transistors on Si and PET substrates and led to improved mobility and the linearity of the output curve at low V_{DS} [105]. Similarly in [100], improved transistor performance (lower V_T) of [7]phenacene single-crystal FET was achieved by the insertion of F_4-TCNQ between the source/drain contacts and the semiconductor.

Furthermore, since these transistors are to be used in flexible application, it is of interest to preform force and bending experiments once the device performance is thoroughly optimised. The bias stability measurements would also be essential as well as any age-degradation studies.

Finally, the developed compact model has provided significant effort towards achieving fully functional OTFT model built in Matlab. As mentioned previously, further work is needed to accomplish more comprehensive model to improve the accuracy of the a.c. data simulation. Since some simplifications were applied in the present model, the addition of the contact resistance and the parasitic capacitance might lead to improved results.

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