Enhanced Protection and Location Techniques for Enabling Wider Implementation of LVDC Distribution Networks

PhD Thesis

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

With the increasing penetration of renewable generation in power systems and the electrification of heat and transport, LV distribution networks are under pressure to host a growing number of low carbon technologies. Alternative Low Voltage Direct Current (LVDC) distribution networks have been considered as an effective approach to release the pressure on existing LV distribution networks. Meanwhile, the fast development of power electronics and increasing LVDC applications facilitate the transition to LVDC distribution networks. However, DC fault protection and location have been identified as key technical challenges by a number of research works and industrial groups.

This thesis works toward the development of a fast and selective protection scheme and a reliable and accurate fault location technique that are to ensure secure and reliable LVDC operations, thereby facilitating the transition towards the widespread implementation of LVDC distribution networks. As LVDC protection solutions are influenced by AC/DC interface converters, existing protection solutions are mainly based on conventional two-level voltage source converters. Recently, new converter technologies such as solid-state transformers (SST) have been implemented, their unique fault characteristics introducing new requirements in understanding the impact of new converters. This is presenting the need for new recommendations and guidelines, and for developing new protection solutions.

Therefore, this thesis presents an approach for fault characterisation and protection evaluation of future LVDC distribution networks. The SST is selected in this thesis to conduct case studies due to its unique fault characteristics, enhanced fault current control capabilities, great potential to replace existing LV transformers, and additional

ancillary services. The derived understanding of the impact of SST on DC fault response and the effectiveness of existing protection solutions gives recommendations for future LVDC protection design. These help the development of a novel voltage-based protection scheme that uses the combination of sign of current derivative, voltage magnitude, and voltage concavity. The proposed protection scheme only relies on local measurements without any communications. The enhanced protection selectivity and the fast protection speed have been proven by simulation studies. The improved performance of the proposed protection scheme compared to existing methods allows LVDC distribution networks to have faster power restoration during fault events thus enabling resilient LVDC operations. In addition, a fault let-through energy (FLTE) based fault location technique is developed that uses FLTE in conjunction with a 'critical point' concept that is based on the capacitor ratio of local and remote converters. This achieves improved accuracy and reliability over the most of the proposed fault distance estimation techniques during the fault transient period. The enhanced performance of the proposed fault location technique has been verified based on simulation studies. This improved accuracy and reliability allows DC faults to be accurately located and facilitates rapid network reconfiguration and post fault cable maintenance.

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Glossary of Abbreviations

AC	Alternating Current
AIE	Active Impedance Estimation
AMR	Anisotropic MagnetroResistance
ANN	Artificial Neural Network
BESS	Battery Energy Storage System
CDCCB	Capacitor DC Circuit Breaker
DAB	Dual Active Bridge
DC	Direct Current
EMS	Energy Management System
ETO	Emitter Turn Off
EV	Electric Vehicle
FB	Full-Bridge
FLTE	Fault Let-through Energy
GMR	Giant MagnetroResistance
GTO	Gate Turned Off
GUI	Graphical User Interface
HB	Half-Bridge

HVDC	High Voltage Direct Current
IED	Intelligent Electronic Device
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IT	Isolé-Terre
LED	Light-Emitting Diode
LV	Low Voltage
LVAC	Low Voltage Alternating Current
LVDC	Low Voltage Direct Current
MMC	Modular Multilevel Converter
MCCB	Molded-Case Circuit Breaker
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MRA	Multi-Resolution Analysis
MV	Medium Voltage
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped
PCC	Point of Common Coupling
PET	Power Electronic Transformer
PLL	Phase Lock Loop
PoE	Power over Ethernet
PV	Photovoltaic
PWM	Pulse Width Modulation

RB-IGCT	Reverse Blocking Integrated Gate-Commutated Thyristor
RLC	Resistance-Inductance-Capacitance
RMS	Root Main Square
RMU	Ring Main Unit
SCADA	Supervisory Control and Data Acquisition
SM	Sub-Module
SSCB	Solid State Circuit Breaker
SST	Solid State Transformer
THD	Total Harmonic Distortion
TRL	Technology Readiness Level
USB	Universal Serial Bus
VSC	Voltage Source Converter
WT	Wavelet Transform

Chapter 1

Introduction

1.1 Research Context

Existing Low Voltage (LV) distribution networks are already under pressure to host growing numbers of low carbon technologies such as electric vehicles, heat pumps, energy storage systems, and solar generation. Due to developments in power electronic converters (e.g. achieving increased power density and reduced footprint [1]) and the increasing applications inherently powered by DC systems, Low Voltage Direct Current (LVDC) distribution has been recognised by a number of industrial and research groups as one of the preferred solutions to alleviate the stress and provide the required increased capacity. Further benefits such as energy-saving and enhanced controllability have also already been demonstrated via trials across the world [2]. In order to pave the way for a wider LVDC uptake, this effort has been recently supported by technical guidance and standards developed by the International Electrotechnical Commission (IEC) [3]. One of the key challenging areas identified by various research efforts and the IEC is the need for selective DC protection solutions as well as reliable and accurate DC fault location techniques in order to ensure the security and reliability of LVDC operation [4].

In general, the design and performance of LVDC protection schemes are highly influenced by the way the main grid and the LVDC distribution network are interfaced. Two-level Voltage Source Converters (VSCs) have been commonly used for connecting LVDC systems to the AC grid due to their simplicity and low cost. However, they do

not provide any fault control capabilities and hence require higher equipment ratings and fast protection due to the high fault current infeed from the AC grid. There are already a number of DC protection solutions available in the literature to meet such requirements [5]. Very recently, new innovative interface technologies such as solid-state transformers (SSTs) have been proposed to ultimately replace conventional transformers at medium voltage (MV) to provide both LVAC and LVDC supplies, since they are capable of providing more effective and flexible voltage control and independent real and reactive power control [6]. From a protection perspective, the SST will provide reduced prospective fault current and will potentially enable the use of equipment with lower current ratings. However, deployment of an SST at distribution substations will fundamentally change the fault profiles of any associated LVDC distribution networks and introduce additional protection challenges and requirements only by understanding the impact and developing recommendations and guidelines, will be required new protection solution emerge. From these issues, the main challenges to be addressed in this thesis are briefly described below:

- There is a need to understand fault characteristics of an SST interfaced LVDC distribution network. This will prove the benefits of SST implementation in reducing the fault current stress of LVDC power electronics. However, the reduced fault currents have the potential to present challenges regarding the effectiveness of existing protection solutions. Consequently, there is a need to understand the impact of an SST on existing protection solutions, especially in terms of their protection speed and DC fault discrimination capability.

- To protect SST interfaced LVDC distribution networks, voltage-based protection solutions pose potentially better credentials compared to existing current-based protection solutions. However, conventional voltage-based protection solutions lack selectivity in terms of distinguishing upstream and downstream faults, and they are very sensitive to resistive faults that can easily lose fault discrimination of internal and external faults. These issues present challenges to threshold settings which are required to provide a good level of protection selectivity.

- There is a requirement to establish more accurate and reliable LVDC fault location estimation when converters are integrated within LVDC systems, in order to facilitate improved post-fault network maintenance. Existing LVDC fault distance estimation methods are primarily based on the current derivative which is very sensitive to noise and, in order to achieve high levels of accuracy, also requires complicated filter designs to process the measured signals. Meanwhile, existing fault location techniques do not effectively determine the remote end converters' fault current contributions, thus compromising the accuracy of their local measurement-based methods.

Therefore, the existing understanding of fault characteristics and protection solutions will no longer be suitable to guarantee the security of future LVDC distribution networks when more advanced converters are used. In light of this, there are new opportunities to extend existing understanding and develop new protection solutions to fill the identified gap in protection solutions and implementations that has arisen from the aforementioned recent trends in LVDC systems. To this end, the main work reported in this thesis is focused on developing effective LVDC fault protection and location techniques. This is underpinned by investigating, analysing, and identifying the limitations of existing protection solutions. Subsequently, novel methods for a voltage-based protection solution and fault let-through energy-based fault location technique are proposed to ensure the secure operation of future LVDC distribution networks.

1.2 Research Contributions

This thesis provides the following distinctive contributions to existing knowledge:

- Development of a comprehensive approach for future LVDC fault characterisation and protection evaluation. This is used to facilitate better understanding of the impact of advanced converters on DC fault characteristics and effectiveness of existing DC protection solutions.
- Detailed fault characterisation of an SST interfaced LVDC distribution network. A comparison of the difference in each fault stage to a two-level VSC interfaced

LVDC distribution network is drawn as well as quantification of the impact of an SST on the fault profile.

- Detailed modelling and evaluation of existing LVDC protection solutions on an SST interfaced LVDC distribution network. Quantification of the impact of the SST on the effectiveness of existing protection performance in terms of protection speed and fault discrimination capabilities is presented. As a consequence, an outline of recommendations for future protection solution design is developed, based on the outcomes of the associated investigations.

- Design, analysis and software realisation of a novel voltage-based protection solution with enhanced protection selectivity by using the combination of the sign of current derivative dI/dt, voltage magnitude V, and voltage concavity d^2V/dt^2 in cooperation with assistive inductors. The solution is communication-less, relying only on local measurements. The enhanced protection selectivity is verified on an LVDC network model using PSCAD/EMTDC.

- Design, analysis, and software realisation of a novel fault let-through energy-based fault location technique. The method subsequently proposes a new DC fault location strategy which uses the 'critical point' as a reference to direct post-fault network maintenance teams. The proposed method does not require data synchronization to establish the critical point, and this is regardless of the size of the converters connected to the LVDC feeder. The accuracy and reliability of the proposed fault location strategy are also validated against a number of faults on an LVDC network model using PSCAD/EMTDC.

1.3 Thesis Overview

Chapter 2: This chapter presents the transition to LVDC distribution networks and addresses the four key drivers governing the paradigm shift: the pressure of existing LV networks, developments of power electronics, increasing applications operating with LVDC, and the claimed benefits of LVDC technologies. Following on from this, the

chapter reviews the developments of various worldwide LVDC trial projects, technical standards, and existing LVDC technologies, with special emphasis placed on LVDC converters and protection solutions. The chapter concludes by outlining the remaining technical and economic challenges for the increased use of LVDC distribution networks. Based on the discussion, the main research areas for this work have been identified.

Chapter 3: Having identified the research questions and thesis objectives, this chapter focuses on the development of an approach for fault characterisation and protection evaluation of future LVDC distribution networks integrated with advanced converter topologies. An SST interfaced LVDC distribution network is developed as a test network model to facilitate fault characterisation and protection evaluation research.

Chapter 4: This chapter investigates and quantifies the impacts of an SST and a commonly-used two-level VSC on the fault characterisation of LVDC distribution networks by comparing the respective fault responses in each fault stage. After that, modelling of existing LVDC protection solutions is presented and the effectiveness of these methods to protect an SST interfaced LVDC distribution network evaluated. Key limitations are highlighted. Following on from these discussions, recommendations for protecting SST interfaced LVDC distribution networks are provided.

Chapter 5: Subsequently, this chapter focuses on the development of a novel voltage-based protection scheme for protecting an SST interfaced LVDC distribution network. The chapter initially highlights the selectivity challenge of conventional LV voltage-based protection solutions, and based on the discussions, a novel voltage-based protection scheme is developed. This uses a combination of the sign of current derivative, voltage magnitude, and voltage concavity to provide enhanced protection selectivity. Finally, the effectiveness of the proposed method is validated by application to the SST interfaced LVDC test network using PSCAD/EMTDC.

Chapter 6: This chapter presents the development of a novel fault location technique that can provide more accurate and reliable fault distance estimation to facilitate

post-fault maintenance of LVDC distribution networks. The chapter first presents the limitations of existing fault location techniques when LVDC feeders are interconnected with renewables through remote end converters. Following on from these discussions, a novel fault let-through energy-based fault location technique is proposed in conjunction with a 'critical point'. The improved accuracy and enhanced reliability of the proposed method is then validated in the LVDC test network model using PSCAD/EMTDC.

Chapter 7: This chapter summarizes the contributions of the research and identifies the remaining potential issues worthy of future work. Specific advances towards a higher Technology Readiness Levels (TRL) of the proposed protection scheme and fault location estimation technique are also discussed. In addition, the potential challenge of troublesome interactions between fast DC protection and control systems is identified, and the required further investigation is outlined to ensure the secure operation of future LVDC systems.

1.4 Publications

The following section will introduce the publications result from research works.

1.4.1 Published Journal Articles

- **D. Wang**, V. Psaras, A. Emhemed, G. Burt, "A Novel Fault Let-through Energy based Fault Location for LVDC Distribution Networks," *IEEE Trans. Power Deliv*, *Early Access*, 2020.

- **D. Wang**, A. Emhemed, and G. Burt, "Improved voltage-based protection scheme for an LVDC distribution network interfaced by a solid state smart transformer," *IET Gener. Transm. Distrib.*, vol. 13, no. 21, pp. 4821–4829, 2019.

- K. Smith, **D. Wang**, A. Emhemed, S. Galloway, and G. Burt, "Overview Paper on: Low Voltage Direct Current Distribution System Standards," *Int. J. Power Electron.*, vol. 9, no. 3, pp. 1–24, 2017.

1.4.2 Published Conference Papers

- K. Smith, **D. Wang**, R. Peña-Alzola, G. Burt, A. Kazerooni, and M. Eves, "An Approach to Assessing the Effective Integration of Solid State Transformers in LV Networks," in *CIRED 2020*, 2020.
- **D. Wang**, A. Emhemed, G. Burt, J. Zafer, A. Kazerooni, A. Donoghue, "Quantification of Transient Fault Let-through Energy within a Faulted LVDC Distribution Network," in *IET ACDC 2019*, Feb 2019.
- A. Emhemed, **D. Wang**, G. Burt, J. Zafar, A. Kazerooni, and A. Donoghue, "Multi-zone LVDC Distribution Systems Architecture for Facilitating Low Carbon Technologies Uptake," in *IET ACDC 2019*, Feb 2019.
- A. Smith, **D. Wang**, A. Emhemed, and G. Burt, "An Investigation into the Limitations of the Combined dv/dt and di/dt Protection Technique for Compact d.c. Distribution Systems," in *UPEC 2018*, Sep 2018.
- A. Makkieh, A. Emhemed, **D. Wang**, G. Burt, A. Junyent-Ferre, "Fault Characterisation of a DC Microgrid with Multiple Earthing under Grid Connected and Islanded Operations," in *UPEC 2018*, Sep 2018.
- A. Makkieh, A. Emhemed, **D. Wang**, A. Junyent-Ferre, G. Burt, "Investigation of Different System Earthing Schemes for Protection of Low Voltage DC Microgrids," in *IET RPG 2018*, Jun 2018.
- **D. Wang**, A. Emhemed, and G. Burt, "A Novel Protection Scheme for an LVDC Distribution Network with Reduced Fault Levels," in *ICDCM 2017*, 2017.
- **D. Wang**, A. Emhemed, P. Norman, and G. Burt, "Evaluation of Existing DC Protection Solutions on an Active LVDC Distribution Network under Different Fault Conditions," in *CIRED 2017*, 2017.
- **D. Wang**, A. Emhemed, G. Burt, and P. Norman, "Fault Analysis of an Active LVDC Distribution Network for Utility Applications," in *UPEC 2016*, 2016.

Chapter 2

Transition to LVDC Distribution Networks and Key Challenges

2.1 Drivers Toward LVDC Distribution Networks

There are four main drivers for the transition of existing LV networks to LVDC distribution networks such as the pressure on existing LV networks, the development of power electronics, increasing numbers of devices operating with LVDC, and the quantified benefits of using LVDC.

2.1.1 The Pressure on Existing LV Networks

More recently, the increased understanding and concern with the pollution to the environment that traditional power generations bring, has initiated a clean power revolution that is challenging the current 100 year old power system paradigm. Existing LV distribution networks are under pressure to host growing numbers of low carbon technologies such as electric vehicles (EVs), heat pumps, energy storage, and solar generation. This is set to continue, with legislation setting at ambitions targets. For example, the sale of petrol and diesel vehicles will be banned and replaced by EVs in many countries such as in Norway by 2025, Germany by 2030, and the UK by 2040 [7]. Such a radical change in the transport sector, in addition to the electrification of heat (e.g. heat pumps), will

add a significant demand to existing LV networks. Considering the UK as an example, under a future low carbon scenario, the high penetration of electric vehicles is expected by 2050 to result in an annual demand up to 90TWh [8]. This represents an increase in demand by 30% from 2017. Heat pumps are also expected to become dominant in the UK by 2050, with the expectation that the use of gas boilers will fall as a result, by 70% of the present volume [8]. These will require a large investment, estimated to be £30-45 billion for the UK grid and as such, radical solutions in LV networks are needed to meet these expected increases in demand [9]. Significant works are going to help systems to alleviate pressure, but that levels of power demand growth will still fundamentally challenge capacity of existing LV networks. LVDC distribution has recently been recognised by a number of industrial and research groups as one of the preferred solutions to alleviate the strain and increase the capacity of existing LV networks in order to meet this anticipated growth in transport and heat demand [10].

2.1.2 Development of Power Electronics

The significant development of power electronic technologies also represent a key driver for the serious consideration of enabling a transition to LVDC. The Insulated Gate Bipolar Transistor (IGBT) for example has in recent years, been applied in most power electronic applications, especially with medium and high power equipment (e.g. Uninterruptable Power Supply, wind and solar generation). In the last quarter of a century, due to the development of IGBT chip and package technologies, it still plays the leading role in controlling the power electronics [1]. For example, a 1200V IGBT has seen a 70% reduction in footprint size (as shown in Figure 2.1) and 200% power density increase from the year 1990 to 2015 [1]. With the developments of power electronics, LVDC distribution networks are more likely to have more compact and smaller size converters than conventional AC transformers in LVAC distribution networks. The advancements in power electronics also contribute to better power converter topologies, achieving more efficient and advanced AC/DC and DC/DC conversions, and solid-state transformer (SST) with high-frequency galvanic isolation being one particular emerging example. The typical size of an SST is much smaller than a conventional 50Hz

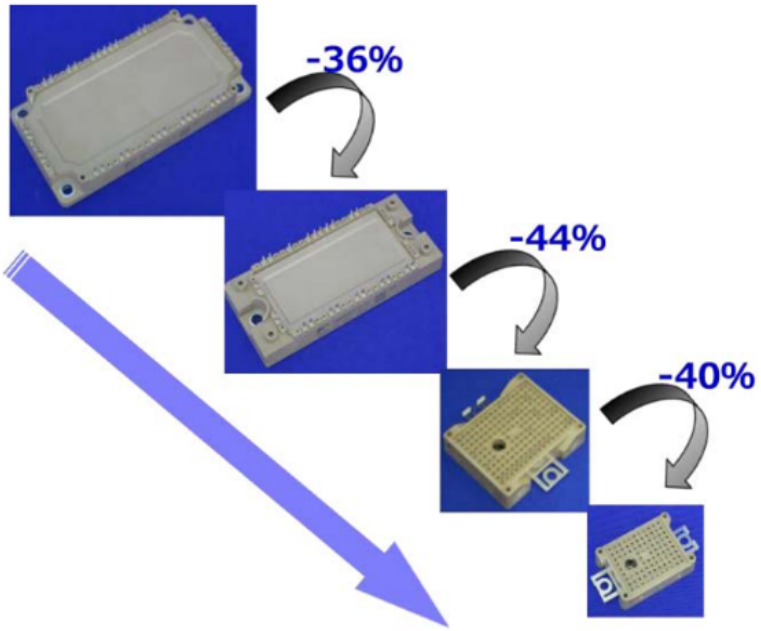

Figure 2.1: Footprint reduction of IGBT Module rating 35A/1200V over four typical IGBT generations during the years 1990-2015 [1]

AC transformer and can provide more efficient and flexible voltage and power control capabilities for MVDC, LVDC, and LVAC supplies [6]. The development of power converters facilitates the transition from purely LVAC systems, to hybrid AC/DC or purely LVDC distribution networks.

2.1.3 Increasing Applications Operate with LVDC

Apart from the development of power electronics and converters, an increasing number of applications operating primarily with DC is also an important motivating factor for adopting LVDC infrastructure, with a number of applications, both industrial and on the consumer side, using DC. DC ready applications have served the market for a long time in the form of, telecommunications [11], data centres [12], marine applications [13], and rail transport [14]. Renewable generations such as solar Photovoltaic (PV) have also been widely implemented as a competitive renewable energy source, with the generated DC power available for direct storage in a complementary Battery Energy Storage System (BESS) or exported to AC feeders [15].

On the consumer side, there are a number of DC-ready end-user applications such as cooling and heating (e.g. radiant heating [16] and air conditioners [17]), refrigeration [18], and lighting systems [19]. There have also been a rapid adoption of Light-Emitting Diode (LED) lights due to their high energy efficiency and quick payback period [20] with most LED bulbs to date operated on AC power with an internal converter. However, DC LEDs can operate on a dedicated DC network and have been proven to be more efficient, providing higher lighting quality with greater resilience to voltage fluctuations [21]. As well as this, an increasing number of companies are now offering Power over Ethernet (PoE) lighting solutions for commercial and residential buildings. In terms of transport, electric vehicles are gaining more attention as it becomes an important factor in facilitating the decarburization of society [22]. A significant number of car manufacturers have developed electric vehicles that can be directly charged by DC power such as Porsche, BMW, Volkswagen, and Nissan [23]. The development of advanced DC rapid chargers is also easing the apprehension over milage range, charging accessibility and time to charge [24].

In addition, there is an ever increasing number of end-user appliances requiring DC such as mobile phones and computers as society becomes largely technology focused. The Universal Serial Bus (USB) is one example of a widely used DC system that is common in almost all personal computers, desktops and mobile phones, which requires rectifier that converts AC power to DC. Existing DC applications can be generally categorised into their respective different voltage levels as shown in Figure 2.2. It can be seen that there are a number of existing DC applications available that have been widely used. However, most of these applications are still powered by AC distribution networks through a number of AC/DC converters. The shift to an LVDC paradigm is a more efficient way to interconnect with DC ready applications and the proceeding section will introduce the quantified benefits of adopting LVDC infrastructure.

2.1.4 Quantified Energy Savings and Cost Reductions of Using LVDC

In some developing countries, the medium of DC provides electricity access for 1.2 billion people, drastically improving their living experience [4, 26]. This is largely at-

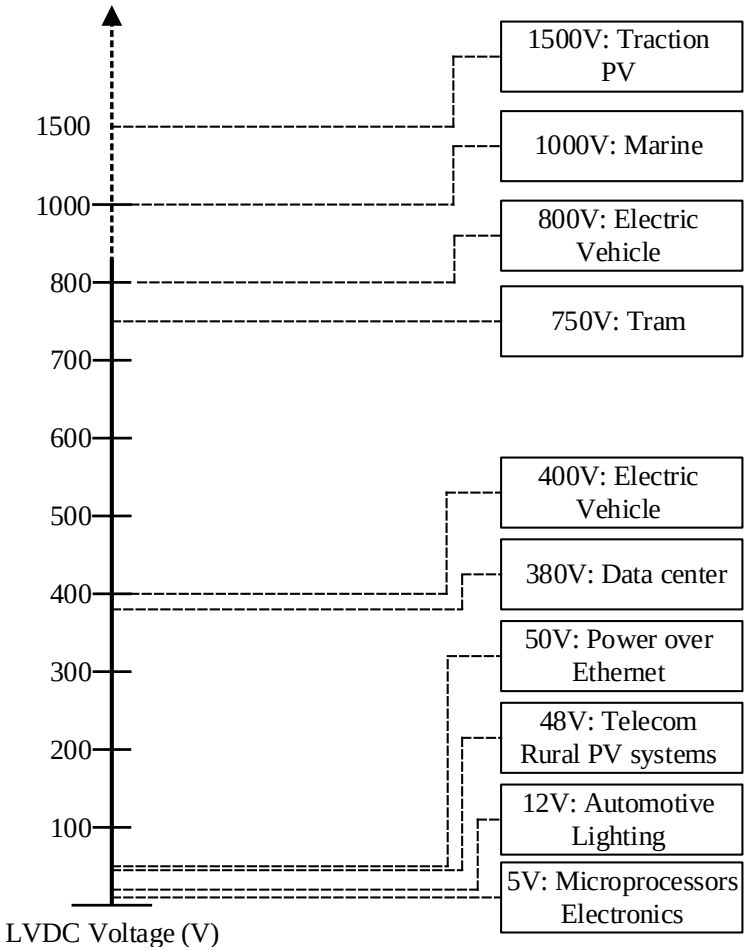

Figure 2.2: Typical existing DC applications based on different DC voltages [25]

tributed to the reduced cost of PV and high-performance batteries. Meanwhile, the development of LED lighting allows for the rapid development of local power supply installations that do not require a connection to the main grid which, in the case of many developing countries, is often more problematic to achieve. With LVDC infrastructure, there is also no synchronisation required for connecting DC power generation (such as PV) and, unlike with AC transmission, there is no skin effect to consider in the cables. With regards to the cabling, DC provides more efficient and higher power transfer compared with AC as the current density is evenly distributed across the entire cable cross-section. As well as these general outstanding advantages of DC, there are several more benefits specific to LVDC applications that have been reported through

simulation estimations, experimental verifications, and pilot projects.

There are many devices that operate internally on DC that are more efficient compared to their AC counterparts. For example, advanced brushless DC (permanent magnet) motors can save 5%-15% energy when compared to a traditional AC induction motor and 30%-50% in variable-speed applications such as pumping and space cooling [27]. Also, a DC motor driven heat pump for space heating is reported to save 50% or more energy [27]. For LED lighting systems, work presented in [28] has reported LED lighting systems supplied with DC power from PV can have 5% saving on the annual cost when compared to LED lighting systems supplied with AC power from PV.

The use of LVDC infrastructure has been proven as a more efficient solution in marine systems, rural and urban areas distribution networks. ABB has developed a marine DC microgrid and demonstrated a reduction in the electrical equipment footprint as well as weight reductions of up to 30%, which in turn yields fuel and emission savings of up to 20% [13]. In rural areas, LVDC has been proven as an effective approach for replacing ageing MV lines which currently supply light loads, saving up to 10-25% in life cycle costs and 5% in operational costs when compared to conventional upgrade approaches [29]. The saving in operational costs is attributed to the minimise of rural networks maintenance costs by improving the automation offered by the inherent features of LVDC systems and converter control capabilities. In urban areas, the increased power capacity to supply more loads and minimising the capital expenditure required for LV network reinforcement, as well as the need for better energy management, are reported as some of the key drivers for LVDC solutions. For example, DC-powered street lighting with a smart management system have demonstrated up to 70% energy savings in LVDC trials conducted in the Netherlands [2].

The aforementioned key drivers continue to raise awareness of the potential a transition to LVDC paradigm can possess by releasing the pressure of hosting an ever increasing quantity of renewable generation installations and the electrified heat and transportation loads. The development of power electronics and the increasing number of applications based on DC are facilitating a transition to LVDC infrastructure. The

quantified benefits of existing DC powered applications and DC pilot projects have proven that LVDC has the potential to be the more efficient power distribution approach at LV and the subsequent sections will briefly introduce the development of LVDC standards, pilot projects, and technologies.

2.2 Developments in LVDC Distribution Networks

2.2.1 Concept of LVDC Distribution Networks

An LVDC distribution system is primarily comprised of power electronic converters and DC links to deliver electrical power, the nominal voltage of which ($\leq$1500V DC) has been specified in the standard IEC 60038 [30]. LVDC technology has been used in several applications, however, large scale DC distribution networks have not yet been widely explored. In terms of network configurations, radial and ring LVDC distribution networks have been proposed and implemented in existing pilot projects [2].

Existing LVAC distribution networks operate in a unified regime with regulated voltage, cables, and protection solutions but despite this, future implementations of LVDC are more likely to take on a multi regime approach, utilising a variety of operating voltages, earthing arrangements, and protection schemes, as shown in Figure 2.3. Such a regime can be classified by different operating zones, for example, zone 1 includes the highest DC voltage range from $\pm$400V to $\pm$750V and provides high power (e.g. 50kW-350kW) with a longer power distribution distance. In zone 1, the voltage level has exceeded the safety limits identified by IEC60479 and thus, Isolé-Terre (IT) earthing is applied to convert this zone into a floating system [2]. The other zones have different operating voltages and earthing configurations that can facilitate the interconnection of different applications. One of the potential benefits of implementing a multi regime is minimising the standards modifications of installing existing DC ready applications in LVDC distribution networks. However, LVDC distribution still requires standards developments to facilitate connections with existing end users. The following section will briefly introduce developments in standards and guidelines.

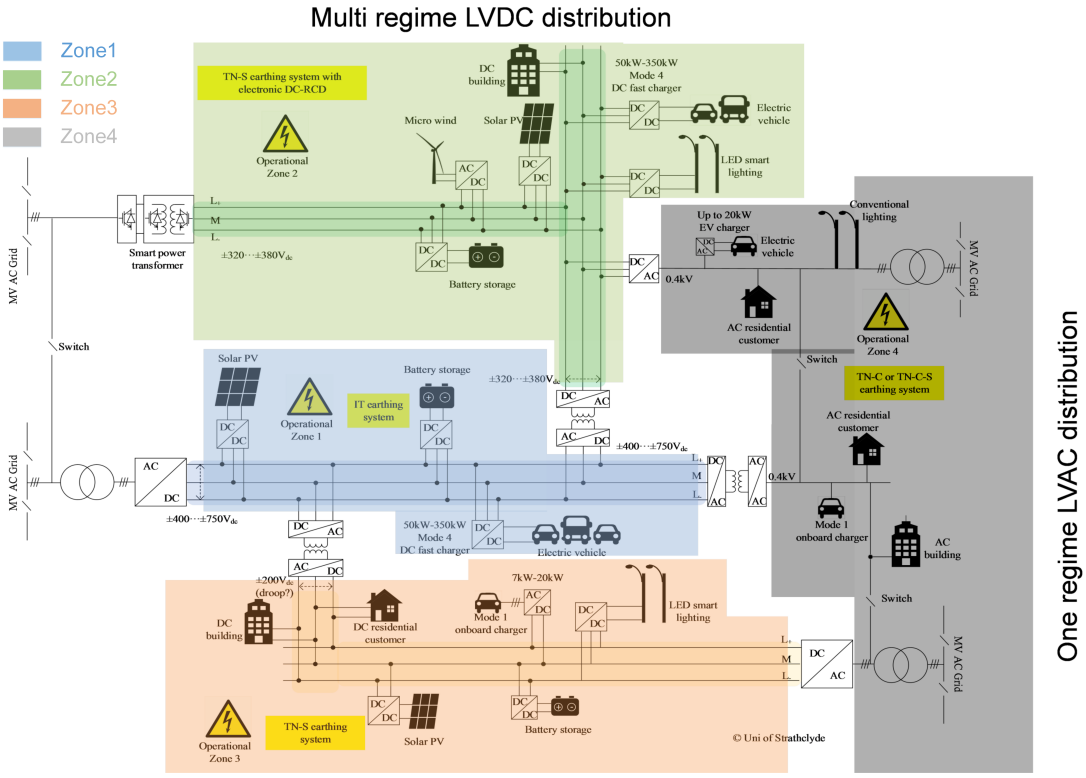

Figure 2.3: An example of a multi regime LVDC distribution network [2]

2.2.2 Developments in LVDC Standards and Guidelines

Several international standards organisations are developing guidelines and requirements for the design and safe operation of LVDC applications (e.g. traction systems, PV generations, marine systems, and data centres). This includes the International Electrotechnical Committee (IEC), Emerge Alliance, the Institute of Engineering Technology (IET), the European Telecommunications Standards Institute (ETSI), and the Institute of Electrical and Electronic Engineering (IEEE). The IEC SyC LVDC is working on the evaluation of the status of standardization in LVDC applications, while the Emerge Alliance is focusing on promoting the use of DC systems and facilitating the development of LVDC standards. The IET has published a code of practice for low and extra-low voltage DC power distribution in buildings, while ETSI establishes standards for telecom systems with 48V DC and 400V DC power systems. In addition, the IEEE working group, Distribution Resources Integrated Working Group/remote DC Micro-

grids, is currently drafting standards for DC microgrids for rural and remote electricity access applications. In terms of different DC applications, Table 2.1 summarises some of the applicable standards for existing LVDC applications.

Table 2.1: Applicable standards for existing LVDC applications [3]

Applications	**Protection**	**Safety**	**Power Quality**	**Earthing & Bonding**
USB	USB-IF	USB-IF	USB-IF	USB-IF
LED	BS EN 61347 2-13	IEC 60598-1	BS EN 62384	IEC 61347-1
Lighting	BS EN 61347-1	IEC 61347-1	-	-
PoE	NEC. 725	-	IEEE 802. 3at	-
Telecom	ETSI 300 132-3-1	ITU-TL. 12 (00-05)	ETSI 300 132-3-1	ETSI EN 301 605
EV charging	BS EN 61851-23:2014	BS EN 61851-23:2014	BS EN 61851-23:2014	-
Data Centre	BS EN 50600-2-2:2014	BS EN 50600-2-2:2014	BS EN 50600-2-2:2014	ETSI EN 301 605
Traction	BS EN 50123-7-1	BS EN 50328	BS EN 50328	IEC 62128
Public Network	-	P2030.10	-	NEC .250
Marine	IEC 60092-507	IEC 60092-507	IEC 60092-101	-
Solar PV	BS EN 60269-6	BS EN 62129-1	BS EN 62109-1	IEC 60364-7-712

At present, there are no international standards to guide the construction of large scale DC distribution systems such as islanded DC microgrids, hybrid AC/DC microgrids, or last-mile DC distribution networks but there is potential to extract and use experience from existing DC applications such as DC traction systems to inform future standards developments. However, traction systems possess a large power quality tolerance due to the special electric loads' requirements. On the other hand, LVDC distribution networks have various low carbon technologies that may require a much tighter power quality tolerance and more selective protection solutions.

It is clear stand-alone LVDC applications have well-developed standards, but public LVDC distribution networks are still found to be lacking standards relating to voltage

harmonics, safety, and protection requirements [3]. In order to have a better understanding of cost benefits and challenges of LVDC distribution, a number of trial projects have been implemented.

2.2.3 Examples of LVDC Pilot Projects

LVDC pilot projects have been available in different countries, such as Finland, Netherlands, South Korea, and China. This section briefly introduces features of examples of LVDC pilot projects and their main purposes.

Finland

In Finland, LVDC distribution systems have been recognised by a number of distribution system operators (DSOs) as a more efficient solution to increase the overall security and reliability of the power supply [31]. Currently, there are three active LVDC utility-scale projects that include a utility LVDC research site [32], point to point embedded LVDC link [33], and LVDC RULES [34].

The LVDC research site has been installed in a live utility distribution network, supplying a normal daily demand of four residential customers and is shown in Figure 2.4 [32].

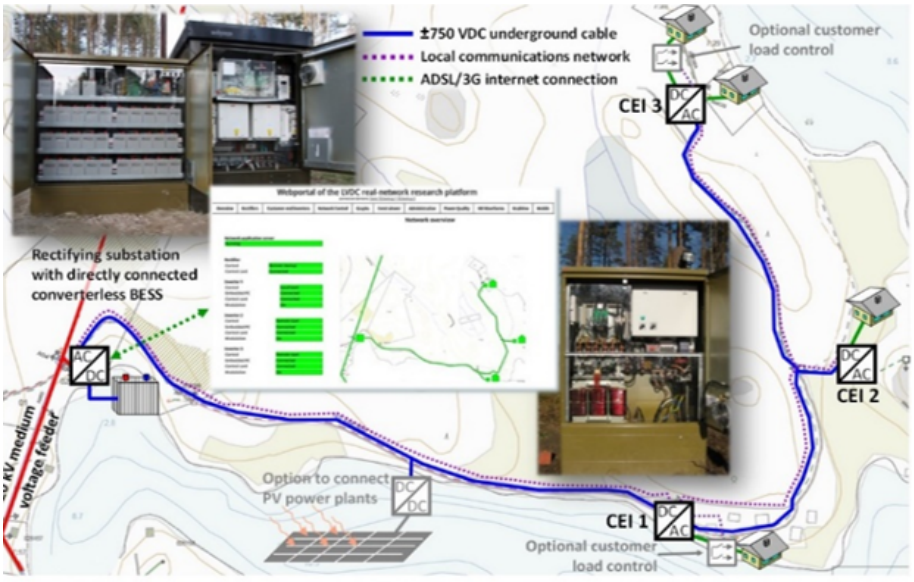

Figure 2.4: LVDC research site in Finland [32]

The research site has been used as a platform to understand the operation of an LVDC distribution network and is led by Lappeenranta University of Technology (LUT). The LVDC network interfaces to a 20kV medium voltage (MV) network through a 100kVA transformer and two parallel-connected fully controlled AC/DC converters and is configured as a bipolar (±750V) system and feeding AC customers through 16kVA DC/AC converters [35]. This trial site has been in continuous operation since 2012 with temperature conditions experienced between +30°C to -30°C [32].

There is also a Finnish point-to-point LVDC pilot project installed in the DSO Elenia Oy distribution network in collaboration with ABB Oy drives [33] and is comprised a 0.5km point-to-point LVDC link to feed LVAC customers, as shown in Figure 2.5 and has been in operation since 2014. This LVDC project is configured as a unipolar system, operating at 750V. The point-to-point converters are integrated with 3G Phoenix modem and wireless communications to the service portal, which can measure data and monitor events and faults [33]. Additionally, converter control is supplied by a 24V lithium-ion battery as a backup power supply helping the power converter control to withstand power outages up to 15minutes, to ensure the reliability of the system. The main purpose of this pilot project is to collect long term user experiences of LVDC operations and maintenance as well as specifying the cycle cost of the embedded LVDC system.

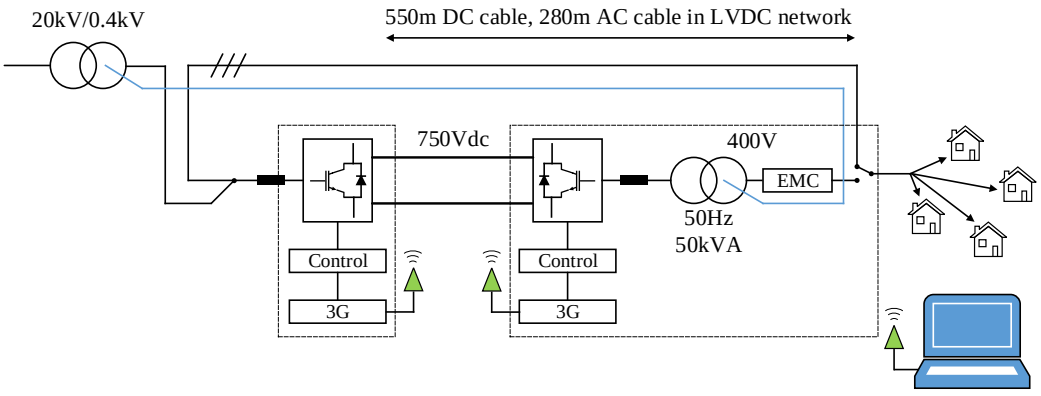

Figure 2.5: Structure of the Finland point to point LVDC pilot project [33]

As well as this, the LVDC RULES project was launched in 2015 based on the existing LVDC research site platform with some improvements, the principle structure of which is shown as Figure 2.6. The construction was undertaken through a collaboration between LUT, Elenia Oy, and Ensto Finland Oy. Currently, LVDC network short-circuit protection is overcurrent protection which is implemented using DC-rated circuit breakers, while the AC side of the converter is protected by fuses [34]. The key objectives of this project are to transfer the LVDC research knowledge into an industrial-scale application and commercially feasible solutions [33]. The project contains four themes including functionalities and technology solutions, impact on distribution networks and business, active resources and renewables, as well as recommended standards practices and professional training [36].

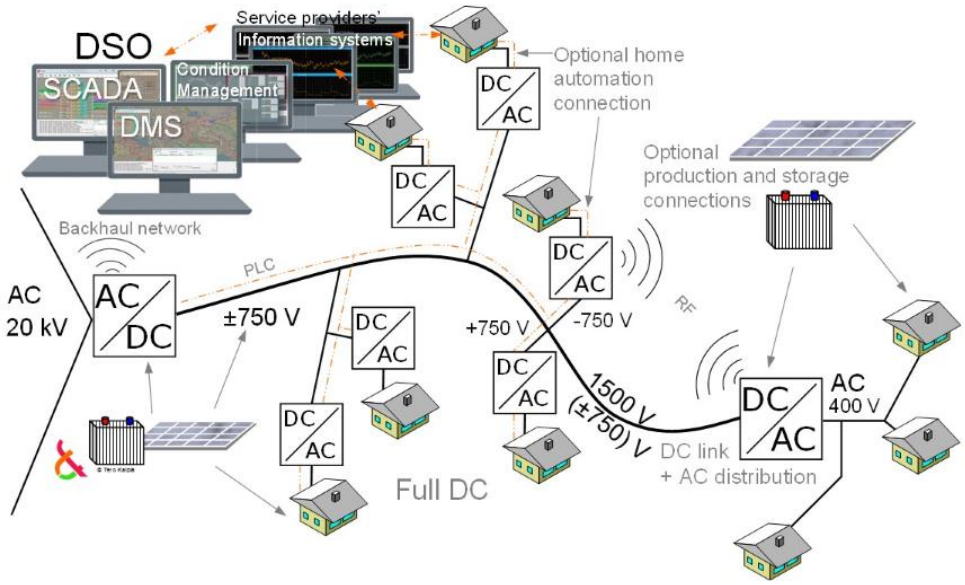

Figure 2.6: Principled structure of LVDC RULES [31]

Netherlands

In the Netherlands, LVDC distribution system development is primarily focused on urban areas. Referring to the Netherlands Energy Agenda 2016, the current AC energy networks are not capable of handling the pressure of the desired energy transition including high penetration of renewables and electric transport [37]. It was also claimed that LVDC infrastructure is the more efficient technology to facilitate such an energy

transition, thus, several LVDC projects have been trialed and implemented. Most of these LVDC projects are led by the company Direct Current BV. For example, the Port of Amsterdam DC lighting project installed 350V public light LED drivers and DC lamps and the schematic of the street lighting system is shown as Figure 2.7. Also, there are a further 12 LVDC projects being undertaken [37].

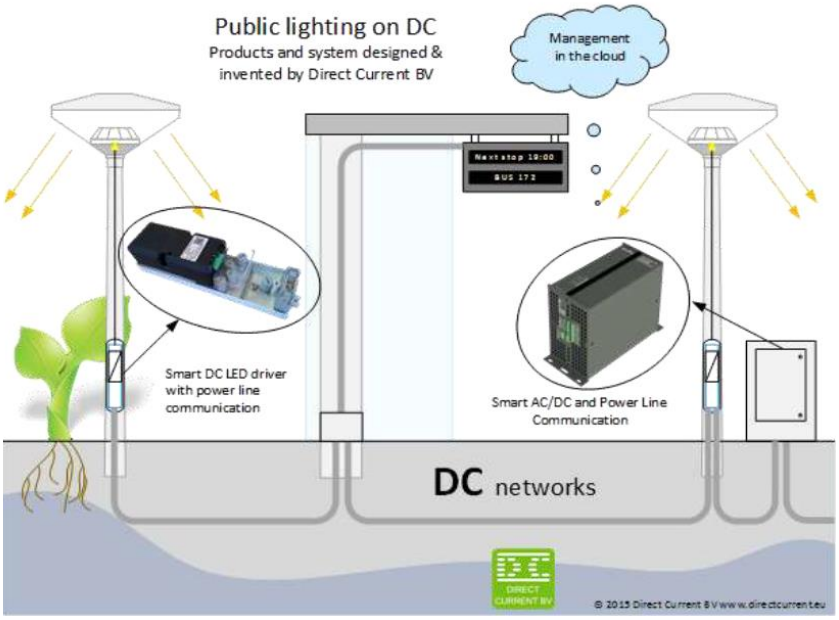

Figure 2.7: Schematic structure of DC street lighting system [37]

South Korea

The implementation of several LVDC pilot projects in South Korea is mainly led by the Korea Electric Power Corporation (KEPCO), with three main projects constructed and reported in the literature. Similar to Finland, a point-to-point LVDC link has been implemented in a mountainous area in Korea with the motivation being the required updating of existing MV rural networks, as shown in Figure 2.8. This LVDC link is designed as a $750V_{DC}$ IT system to supply 27kW loads including a communications repeater (10kW), street lighting (1kW), agricultural (10kW), and domestic loads (6kW) [38]. Power converter is protected by over-voltage protection and over-current protection [38]. The site is also remotely controlled through the graphical user interface (GUI) in a control centre 8km away from the main site.

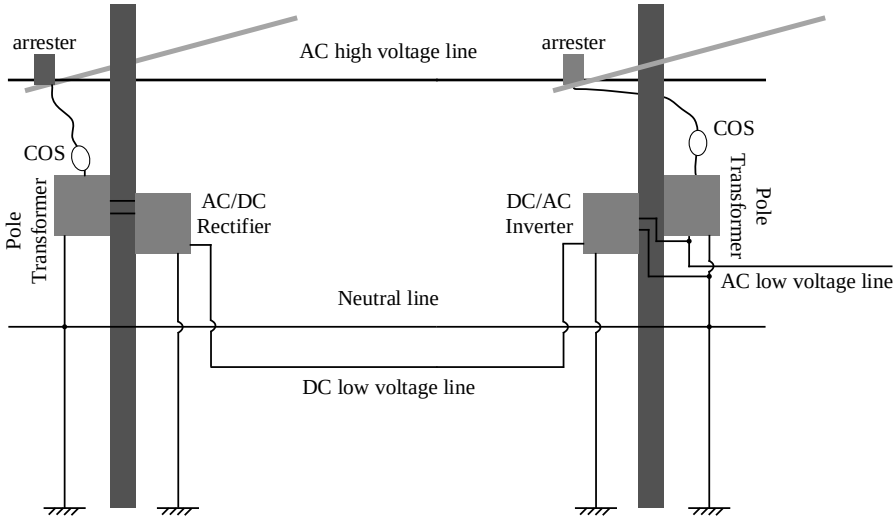

Figure 2.8: Schematic of the Korea pole to pole LVDC distribution link [38]

KEPCO has also constructed an LVDC site in Gochang, South Korea [39] and the configuration is shown in Figure 2.9. It comprises a 100kVA two-level VSC on the secondary side of a 150kVA MV/LV transformer, converting $380V_{AC}$ to $\pm 750V_{DC}$.

Figure 2.9: Schematic of the Korea pole to pole LVDC distribution link [39]

The load side is comprised of 15kW DC/DC converters to step down $750V_{DC}$ to $380V_{DC}$, 15kVA DC/AC inverters to supply AC customers, 10kW DC and 10kVA AC load simulators, 200W LED lighting and a 2.2kW AC motor [39]. The purpose of

building this demonstration site is to understand the stability of LVDC distribution networks especially with regards to output voltage maintenance, voltage ripples, and total harmonic distortion (THD) of power conversion units. In the future, it is planned to provide DC power directly to the customer.

KEPCO has also installed an LVDC network on Geochado Island, South Korea, with the main objective to reduce the reliance on traditional diesel generators as the main source of power through the implementation of an LVDC microgrid with renewables, energy storage, and smart energy management systems. The LVDC system is interfaced to an AC microgrid through a 200kW AC/DC converter with several interconnected renewables such as 200kW PV, as shown in Figure 2.10 [40].

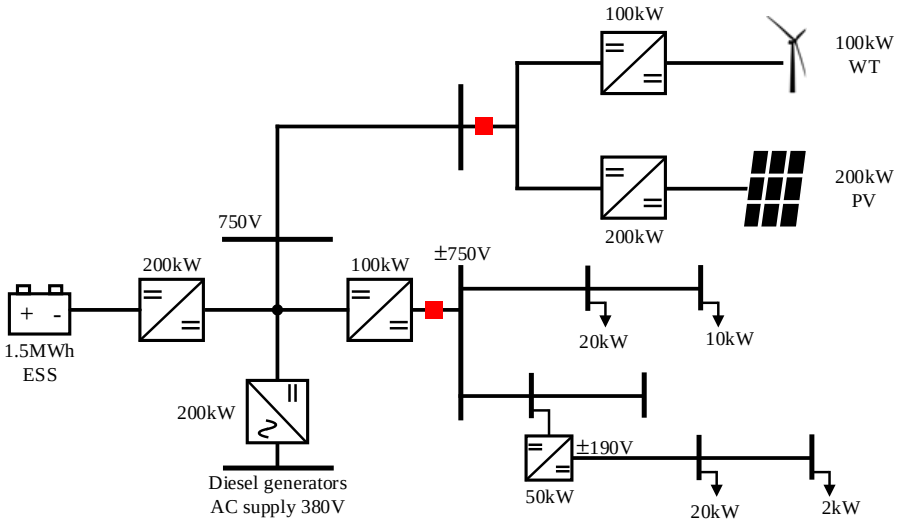

Figure 2.10: Design of LVDC demonstration island [40]

There are also ten existing residential loads and two commercial loads supplied directly by the LVDC system through DC/DC and DC/AC converters. This trial is monitored and controlled by a smart energy management system (EMS) based on centralised supervisory control and data acquisition (SCADA) [40] and is used to verify high-efficiency DC networks compared with existing AC networks. The project will also help the development of DC components in LVDC such as converters and monitoring devices, while, the business model of LVDC systems based on this project will be developed to be fit for domestic and overseas power systems.

China

LVDC distribution projects also have been constructed in China. For example, China State Grid has constructed a Suzhou Tongli LVDC distribution network which provides $\pm 750V_{DC}$ and $\pm 375V_{DC}$. This project has been introduced at the 81st IEC General Meeting in October 2017 [41]. The configuration of this network is shown in Figure 2.11. The network hosts a number of distributed renewable energy sources (total 3MW, 2.91MW PV, 25kW solar thermal, 20kW wind generation) and DC loads (total 1.2MW, 600kW EV chargers, 3kW DC loads, 300kW DC air condition, and 200kW data centre) as well as a Power Electronic Transformer (PET) providing connections between MVAC, MVDC, LVDC, and LVAC. There are other LVDC trial projects installed in China, however, the information available is limited in the literature.

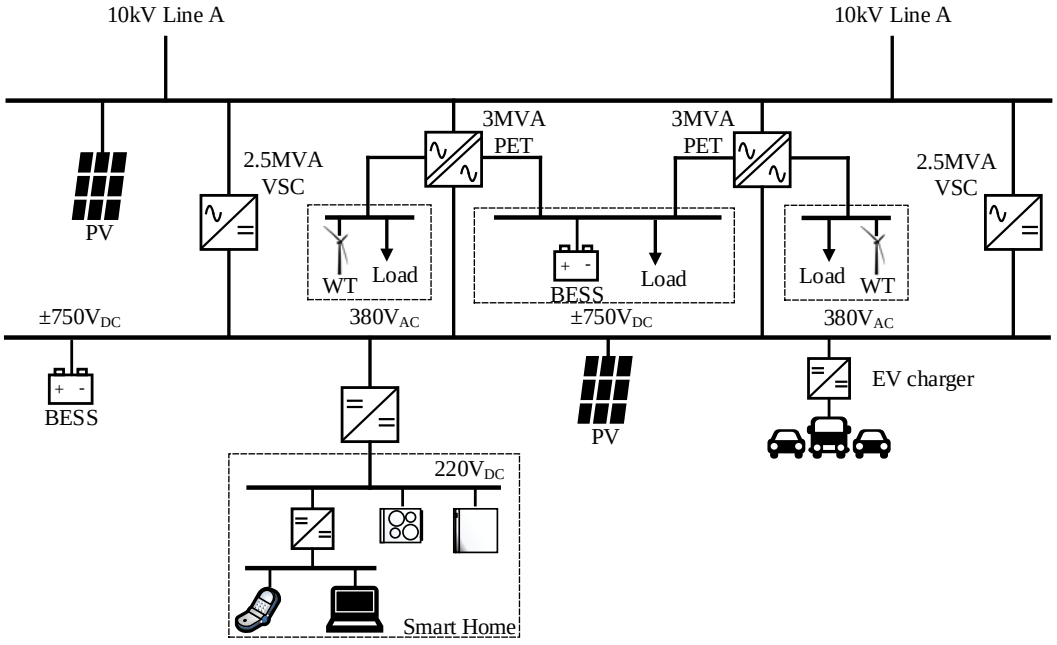

Figure 2.11: Configuration of Suzhou Tongli LVDC site in China [42]

The aforementioned global LVDC trials are just a few examples of existing pilot projects that have been published in the literature. There remain a number of other projects across the world but with limited public information available. The implementations of these pilot projects all have the common goal of quantifying the benefits of using LVDC compared to LVAC for both short term and long term operations. However,

as discussed in section 2.2.2, public LVDC distribution networks still lack standards in some aspects, especially with regards to regulating power quality and protection solutions. One of the other remaining key challenging areas highlighted by various research efforts and the IEC LVDC technology report is the need for reliable DC protection solutions that can provide adequate protection with a good level of safety, selectivity, supporting resilient operation.

In general, the design and performance of LVDC protection solutions are highly influenced by the LVDC interface between the main grid and the LVDC distribution network. Thus, the following section will review the developments of LVDC interfaces.

2.2.4 Developments in LVDC Interfaces

Several different converter types have been used in the various LVDC projects such as two-level VSC, Neutral Point Clamped (NPC) converter, buck-boost DC/DC converter, Dual Active Bridge (DAB) converter with high-frequency transformer, and Solid-State Transformers (SST). Also, the more advanced converters such as Modular Multilevel Converters (MMC) are widely discussed for implementation in LVDC distribution networks [43]. The following sections will first review a number of standard converter topologies and highlight their potential impacts on fault response.

Two-level Voltage Source Converter (VSC)

The two-level VSC consists of IGBTs, diodes, choke inductors, and filter capacitors as shown in Figure 2.12. An IGBT can be replaced by any self-commutated power electronic switch such as a Gate Turned Off (GTO) thyristor or Insulated Gate Commutated Thyristor (IGCT). With Pulse Width Modulation (PWM) based control, a high-quality output voltage can be generated and active power and reactive power can be independently controlled [44]. The two-level VSC has already been utilised in different LVDC projects such as the Finnish LVDC distribution network research site (35kVA) [32], Korea LVDC distribution site [39], Chinese-Danish DC microgrid cooperation project [45], and hybrid microgrid testbed (750kVA) [46]. It should be noted that as a DC link capacitor (i.e. *2C* shown in 2.12) is connected to the end of the converter, significant fault current can be generated under DC fault conditions.

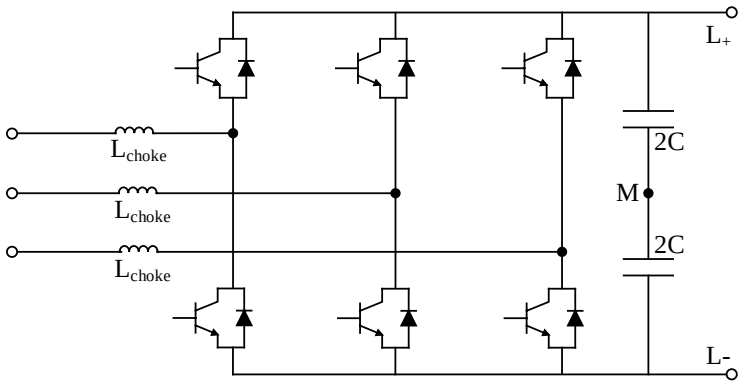

Figure 2.12: Configuration of a two-level voltage source converter

Three-level Neutral Point Clamped (NPC) Converter

The NPC converter is also a suitable solution for LVDC with a typical structure shown in Figure 2.13. Compared to the two-level VSC, three-level NPC converters possess higher grid power quality, reduced total harmonic distortion (THD), and lower switching frequency [47]. It has also been proposed for use in EV charging stations [48] and used in the LVDC test lab [49]. As the DC link capacitor (i.e. *2C* shown in Figure 2.13) is connected at the end of the converter, the fault response is similar to the two-level VSC [50].

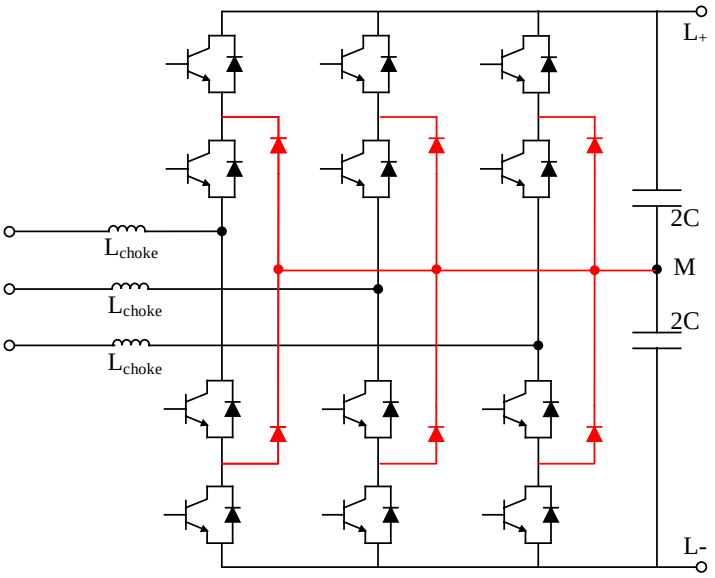

Figure 2.13: Three-level neutral point clamped converter

Modular Multilevel Converter (MMC)

In general, MMCs are classified into three types: half-bridge MMC, full-bridge MMC, and hybrid (combined half and full bridge) MMC. The main MMC topologies are depicted in Figure 2.14, where arm units can be comprised either Half-Bridge (HB) or Full-Bridge (FB) sub-modules and the filter capacitor is distributed in each sub-module. The HB MMC can bypass the sub-module capacitor, but the grid can still contribute fault currents that result in similar fault responses to the two-level VSC. In comparison, as electronic switches are located in the current path of FB Sub-Modules (SM), the FB MMCs and hybrid MMCs are capable of limiting fault currents [51].

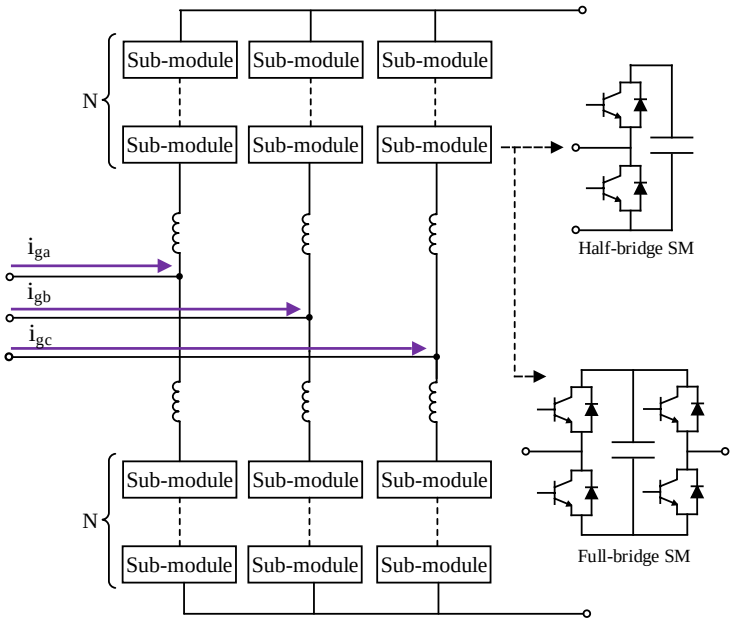

Figure 2.14: Structure of MMC

In comparison to two-level and three-level VSCs however, MMCs are still at a relatively early stage of development for deployment in LVDC distribution networks, non having been deployed in a pilot project. But there are numbers of research articles proposing MMCs with different topologies for specific LVDC distribution applications. For example, MOSFET-based MMCs have been developed to increase the efficiency of MMCs in LVDC applications [43]. Also, using an MMC with fault current limiting capabilities in DC buildings to enhance the interface control capability and fault current

management has been proposed in [52]. In addition, the real prototype of an LV HB MMC has been tested in [43].

DC/DC Converter

DC/DC converters are well developed and have been used in several DC applications such as EVs [53] and solar PV systems [54]. They can be classified into non-isolated converter and isolated converter topologies [55]. A typical non-isolated DC/DC buck-boost converter is shown in Figure 2.15 [56]. The IGBT-diode units are used to modulate the output voltage and the filter capacitors are required to eliminate the harmonics and maintain the DC voltage. Also, this topology will have a similar fault transient as the two-level VSC.

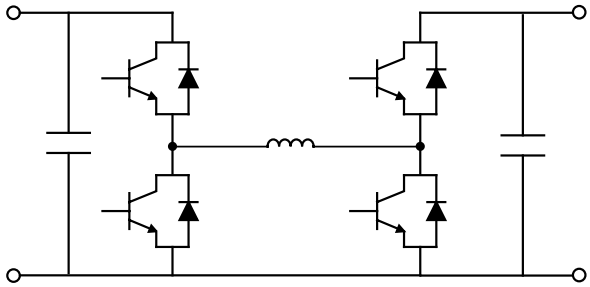

Figure 2.15: Configuration of a typical non-isolated DC/DC buck-boost converter

The isolated DC/DC converter can be seen in Figure 2.16 showing an isolated DC/DC dual active bridge (DAB) which has been proposed for interfacing with a DC distribution grid [57] and also used for connecting PVs [58] and energy storages [59]. Compared to the non-isolated DC/DC converter, the DAB converter has a high-frequency transformer interlink between the primary and secondary bridges. With this transformer, the DAB converter is more flexible with various grounding configurations [60] and the interruption of upstream and downstream fault current feedings [61]. More details of its fault current management capabilities will be discussed in Chapter 4.

Solid State Transformer (SST)

Recently, new innovative interface technologies such as Solid-State Transformers (SSTs) have been proposed to replace conventional transformers at medium to low voltage (MV/LV) secondary substations, with the additional capability to provide both LVAC

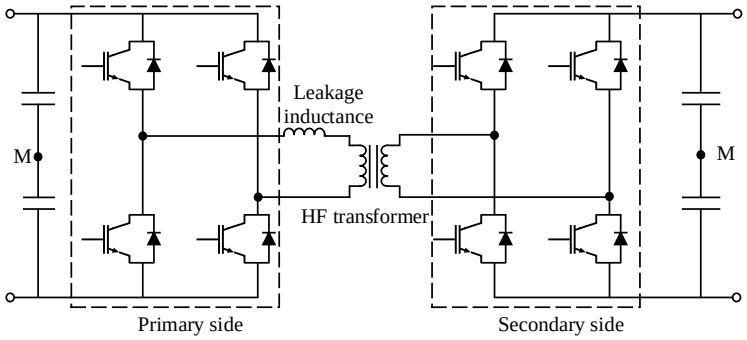

Figure 2.16: Configuration of DAB converter with a high-frequency isolation transformer

and LVDC supplies. Also, compared to existing low frequency transformer, SST can provide reactive power compensation, voltage regulation, power flow control, voltage sag compensation, bi-directional power flow, fault current limiting, harmonic block, and galvanic isolation [62]. It has been trialed in existing LVDC pilot projects where for example, a 3MVA SST has been implemented to convert 10kV_{AC} to $\pm 750\text{V}_{\text{DC}}$ and 380V_{AC} as shown in Figure 2.11 [42]. The SST deployment has also been considered for real utility-owned MV/LV distribution systems to provide more effective voltage control, independent real and reactive power controls, and bidirectional real power control [63, 64]. There are four basic topology configurations, as shown in Figure 2.17. Type A is the direct AC to AC conversion with galvanic isolation to step down from MVAC to LVAC. Type B, an isolated AC to DC conversion stage provides the LVDC followed by DC to AC conversion to supply LVAC power. Type C has the galvanic isolation in DC to AC conversion, LVDC is not available in this type. Type D is a three stage conversion with high frequency isolation in the DC to DC stage [65]. The SST is considered as a compact component to reduce the footprint of future substations [63]. The typical more specific configuration of an three stage SST is shown in Figure 2.18. It consists of a two level voltage source converter, a DAB DC/DC converter, and a two-level DC/AC inverter. Compared to the other DC/DC converters, DAB topology is commonly used in solid state transformer which has zero-voltage switching, bidirectional power flow, and lower component stresses. Also, its associated high frequency transformer with high frequency switching devices can reduce the weight and volume

of passive magnetic devices. In addition, the leakage inductance of the high frequency transformer helps soft switching that limit current and voltage derivative across the switches to reduce switching losses and achieve higher power efficiency [66]. The DAB converter based SST is the mainly focused AC/DC interface for further research.

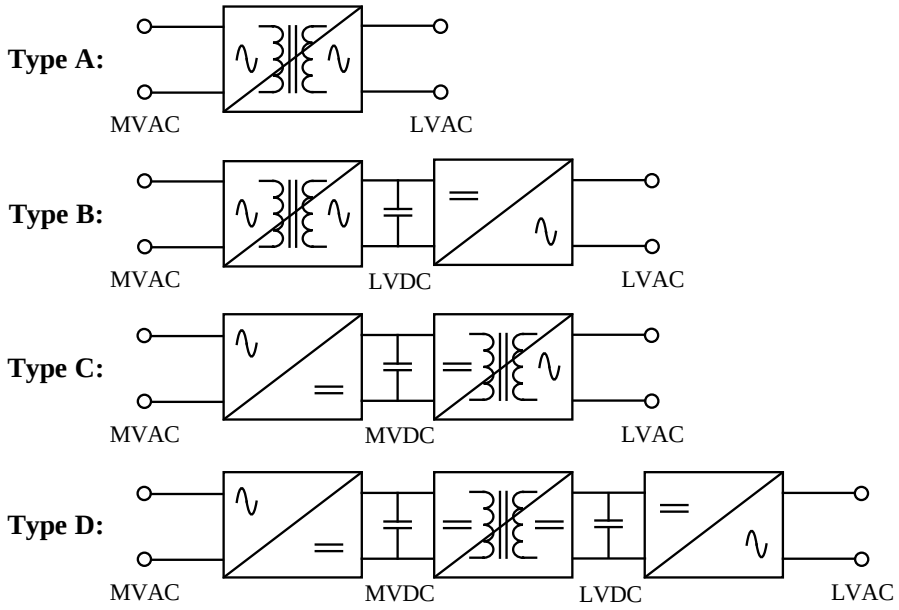

Figure 2.17: Topology classification of SST [65]

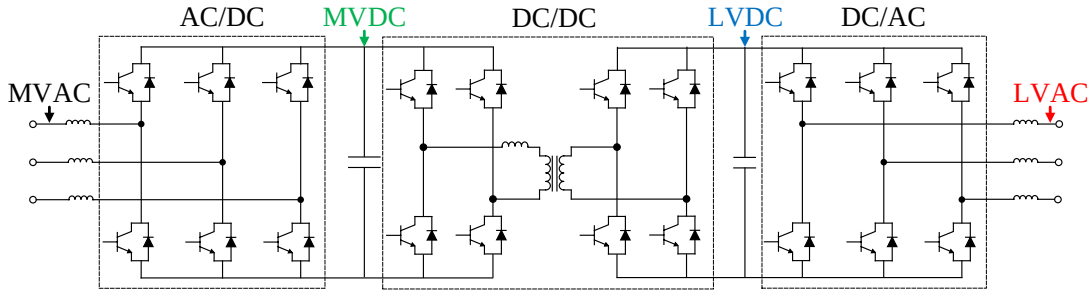

Figure 2.18: Configuration of a typical SST [64]

Implementing SST, the LVDC link is directly feeding the LVAC power supply. In existing LVDC protection solutions for a two-level VSC based LVDC distribution network, the main AC/DC converter can be protected with additional circuit breakers and without concerns about further network influence propagation. Regarding an SST interfaced LVDC distribution network, if the LVDC power supply is isolated directly by

blocking the SST, power outages will be experienced on the other power supplies. In addition, compared to existing two-level VSC, SST only provides low fault current which potentially make existing current based protection solutions less effective in terms of protection speed and fault discrimination capability. These require more effective protection solutions to coordinate SST and LVDC downstream protection relays to avoid unnecessary trips of SST. Especially for distinguishing internal fault, terminal fault, and feeder fault as shown in Figure 2.19 which have quite similar voltage and current characteristics. More details will be discussed in Chapter 4 and Chapter 5.

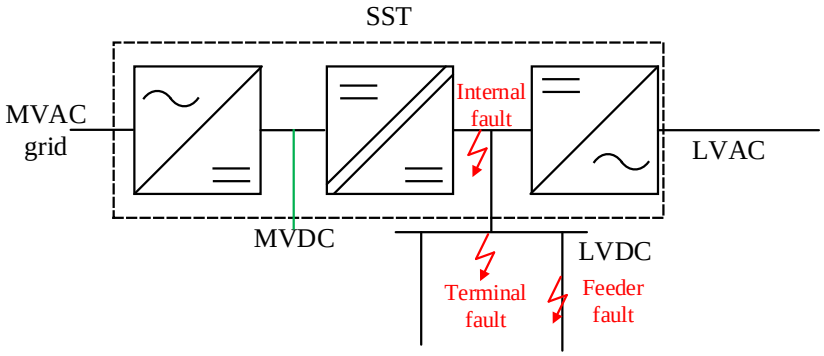

Figure 2.19: An exmaple of a SST single line diagram

2.2.5 The State of the Art of LVDC Protection and Fault Location Techniques

The development of LVDC interfaces creates different fault characteristics compared to existing understandings that is mainly based on two-level voltage source converters, which has the potential to bring challenges to existing LVDC protection solutions. Therefore, it is necessary to understand the state of the art of LVDC protection techniques. Existing LVDC applications can be effectively protected by a mix of simple overcurrent devices, over-rating of converters, and insulation monitoring devices [32]. However, these techniques are limited to wide usage, for example, oversizing a converter is expensive when multiple generators and loads are connected. Most of the existing research works are focused on developing fast numerical protection solutions to protect LVDC systems. Generally, numerical protection architecture consists of measurement

transducer, analog-to-digital conversion, signal processor, and circuit breaker as shown in Figure 2.20 [67].

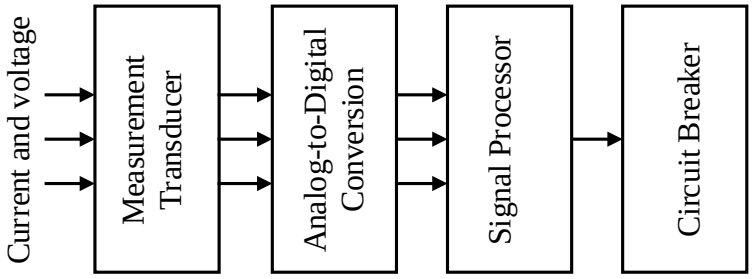

Figure 2.20: General architecture of numerical protection [67]

This section will review existing DC protection and fault location techniques in addition to the available DC protection devices that including measurement transducers and circuit breaking devices. While, the suitability of these techniques for protecting an LVDC distribution network is also discussed.

Non-unit Protection

Non-unit protection solutions do not provide an exact protection boundary and will operate whenever a threshold is exceeded. At present, current and voltage magnitude, current and voltage derivatives, and impedance-based protection solutions have been proposed. The following section will briefly introduce their protection philosophies and discuss the effectiveness of protecting public LVDC distribution networks.

Overcurrent Protection has been widely implemented in existing AC systems. Fault discrimination is performed by time, current, or combined time and current but due to the limitations of individual time and individual current, the characteristic of combined time and current is more commonly used in LV systems such as with fuses [67]. The fault discrimination of the fuse is based on its thermal operation point, which is related to the integral of the square of current over time t (i.e. $\int I^2 t$, defined as fault let-through energy [68]).

Fuse protection has been used in data centres [69] and practical LVDC distribution applications [32], while inverse-time based overcurrent protection has been involved in BS EN standards for protecting traction systems [70], solar PV [71], and marine systems

[72]. Additionally, an improved overcurrent protection system has been proposed for protecting multi-terminal DC (MTDC) systems [73]. This uses the Emitter Turn-Off thyristor (ETO) based Capacitor DC Circuit Breaker (CDCCB), as shown in Figure 2.21, to isolate the filter capacitor, while downstream feeders and loads are protected by fuses and circuit breaker-based overcurrent protection. However, putting a circuit breaker in series with a filter capacitor could cause significant losses as the capacitor is dynamically holding the DC link voltage. When LVDC distribution networks are interfaced with the fault tolerant converters introduced in Section 2.2.4 which only provide limited fault current, longer time is required to clear faults and relays may be unable to detect and discriminate faults. The impact of fault-tolerant converters such as the SST on the effectiveness of overcurrent protection will be investigated and evaluated in Chapter 4.

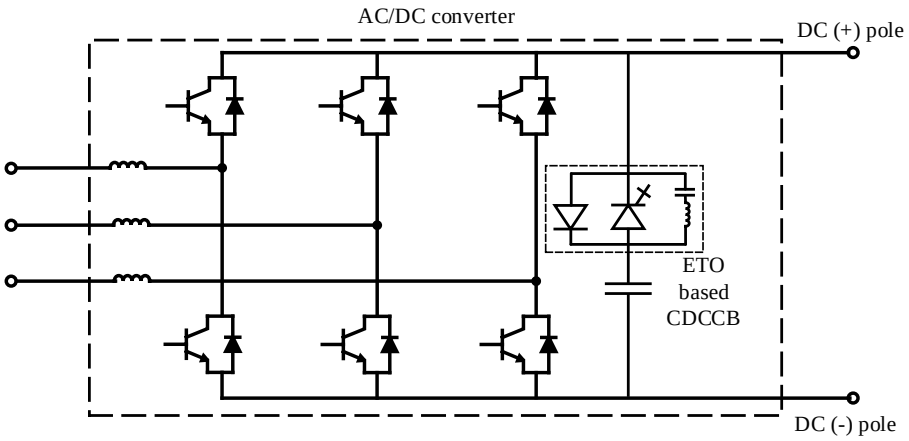

Figure 2.21: ETO based CDCCB

Current Derivative-based Protection relies on the current derivative in the early stages of the DC fault. Compared to overcurrent, current derivative-based protection is much faster and faults can be detected and located in the early stage of the fault transient. It has also been developed to rely on the first point of fault current when the fault is initialised. Under fault conditions, the maximum current derivative is related to the impedance of the fault path [74] and the minimum current derivative can be defined with the maximum inductance (i.e. entire cable impedance) as shown in Figure 2.22 which is selected as a threshold. Such a method has been proposed for protect-

ing a ring bus DC microgrid where DC faults can be detected and distinguished within 200μs [75]. In this protection scheme, the impact of fault-tolerant converters on current derivative-based protection is much less than conventional overcurrent protection but data acquisition is the most challenging issue. As the current derivative is high, any measurement errors (e.g. noise and data loss) can result in weak reliability of the protection. The data optimisation techniques such as least-squares have been implemented to improve the reliability of current derivative-based protection solutions [76]. More details of the effectiveness of this method for protecting LVDC distribution networks will be evaluated and discussed in Chapters 4 and 6.

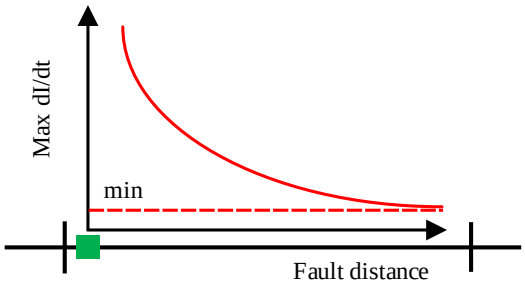

Figure 2.22: Typical current derivative performance against different fault distance

Voltage and Voltage Derivative-based Protection have been proposed for High Voltage Direct Current (HVDC) wind farm collection systems [77]. Such schemes use a voltage divider and time grading to achieve protection selectivity that is similar to fixed time grading-based overcurrent protection. A more efficient voltage-based protection has been proposed which uses voltage magnitude and voltage derivatives in conjunction with DC reactors and MMCs [78]. The voltage derivative allows for discrimination between different fault locations which can be used to distinguish between internal and external faults. However, implementations of large size DC reactors is less likely to happen in LVDC distribution networks as more complicated and frequently power flow changes will result in significant losses on such large size DC reactors. Compared to current based protection, voltage-based protection solutions may be more efficient when fault-tolerant converters are implemented. However, voltage and voltage derivative-based protection have limited protection selectivity in terms of distinguish-

ing between upstream and downstream faults. Chapter 5 of this thesis proposes an improved voltage-based protection scheme to improve the selectivity of voltage and voltage derivative-based protection solutions.

Distance Protection relies on the impedance of the fault path to detect and discriminate between faults. During the fault transient period, due to the rapid changing of voltage and current characteristics, the division of voltage by current can cause estimation errors and result in false fault protection decisions. Some improved DC distance protection solutions have been proposed, for example, the method proposed in [79] coordinates downstream relays with fault current management capabilities of converters. It directly estimates the impedance within the DC fault path using the ratio between the steady-state voltage and current, using the estimated fault impedance to identify the fault location in a DC ring-type microgrid. However, the resistive fault is a significant issue as its resistance will be accounted as part of the cable impedance.

Some other distance protection solutions have better resistive fault protection capability such as active impedance estimation (AIE). This method uses a pre-designed unit as shown Figure 2.23 to inject a 'spike' current, with the Fast Fourier Transform (FFT) used to analyse the relative current and voltage responses to estimate the fault impedance [80].

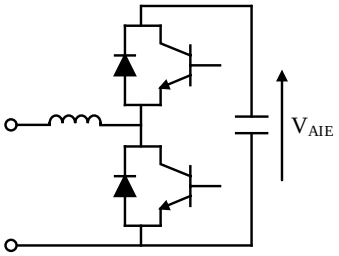

Figure 2.23: Schematic circuit diagram of AIE unit [80]

However, this method is more likely to be implemented for fault location in post-fault conditions, since the AIE unit will have interaction with DC link capacitors that could lead to errors in fault distance estimation.

Wavelet Analysis-based Protection is based on the wavelet analysis of current and voltage signals to extract information to detect and discriminate faults such as the method proposed in [81]. This uses a Wavelet Transform (WT) to monitor the specific frequency component, generated by the predesigned inductor-capacitor circuit shown in Figure 2.24, which can effectively detect and discriminate faults. However, it requires high-speed data processing and communication techniques and additional components could increase the cost.

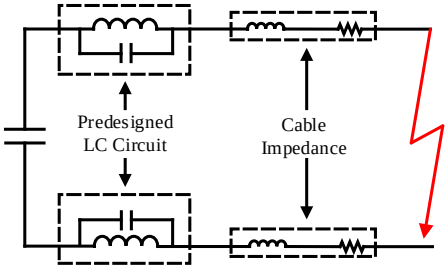

Figure 2.24: Simplified circuit during pole to pole fault using predesigned LC circuit

Apart from using WT in tandem with the predesigned circuit, WT also has been used directly to detect and discriminate faults [81–83]. For example, the WT based Multi-Resolution Analysis (MRA) method in [81], the sampled current signal is processed with the high and low-pass filters and uses the half sampling frequency to compute the scaling and wavelet coefficients, as explained in Figure 2.25.

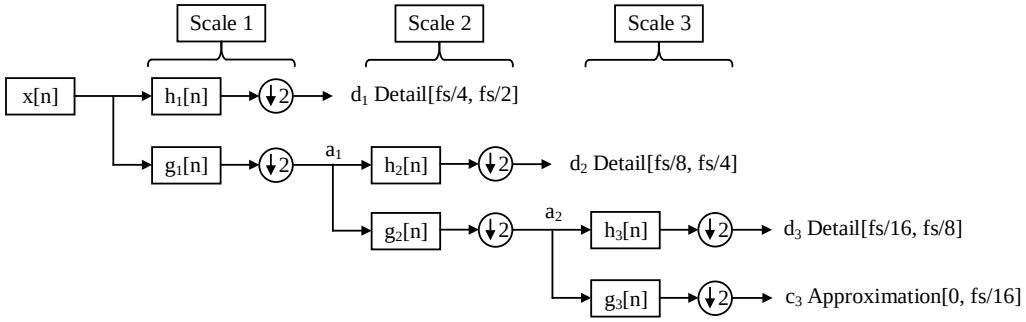

Figure 2.25: Typical decomposition of WT-based MRA [82]

The scaling coefficients, c_x, indicate the low-frequency components which give the approximation description of the fault current. Meanwhile, wavelet coefficients, d_x,

manifest the high-frequency components that give the detailed characteristics of fault current [82]. By using an Artificial Neural Network (ANN) to process the feature vectors, the faults can be classified as illustrated in Figure 2.26.

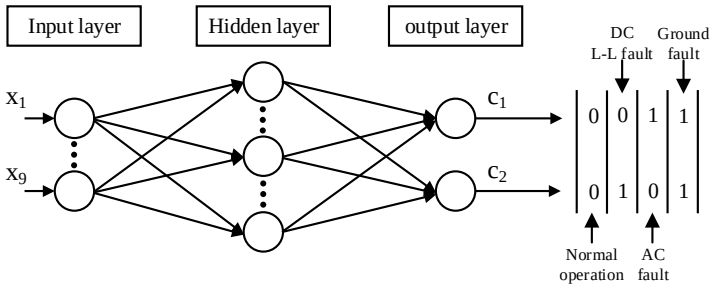

Figure 2.26: Typical 3 layers ANN diagram [82]

Unit Protection

Unit protection techniques have exact protection boundaries and should not operate for external faults. In DC systems, unit protection is normally integrated with high speed and high fidelity communication links and Intelligent Electronic Devices (IED) [84, 85].

Differential Protection is a common form of unit protection. The IED compares the magnitudes of current in (e.g. I_1 shown in Figure 2.27) and current out (e.g. I_2 shown in Figure 2.27) of the protected zone. If the current difference exceeds the pre-set threshold (e.g. $I_{threshold}$ shown in Figure 2.27), the fault is detected and located as an internal fault, and trip signals are generated by the IED and sent to associated breakers located at the boundary of the protected zone. The schematic diagram of differential protection is shown in Figure 2.27. Such a technique has been proposed for LVDC microgrids and with a 20% current difference, the fault can be detected and isolated within 250μs with Solid-State Circuit Breakers (SSCBs) [86].

Directional Protection is another unit protection technique that uses current direction but without a threshold selection. As future LVDC systems will have a number of integrated renewable generations and electrical transportation, all of the downstream and upstream interconnected converters and sources contribute current during fault conditions as depicted in Figure 2.27, and the current direction will be different from normal operation. Comparing current directions in the protected zone, faults can be

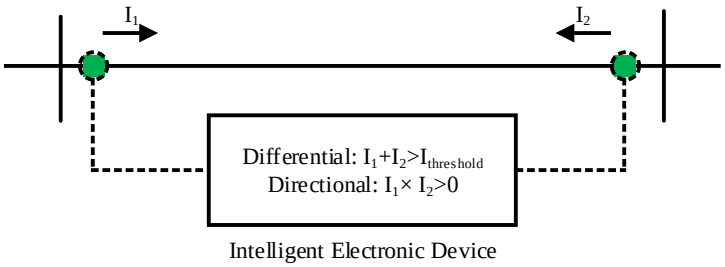

Figure 2.27: Schematic diagram of differential protection

detected and discriminated. An LVDC last-mile distribution network protection scheme has been proposed in [87] that using communications and SSCBs can clear faults in 30μs with a 1ms communication delay. However, due to the high rate of change of current, differential protection is extremely sensitive to communication delay and it is a challenge for IEDs to establish efficient measurement synchronization under DC fault conditions. More details for the effectiveness of these unit protection solutions will be evaluated and discussed in Chapter 4.

DC Fault Location Techniques

Fault location techniques are used to extract the fault distance to facilitate rapid post fault maintenance such as cable replacement and network reconfigurations. Existing fault location methods can be classified into offline and online techniques. There are some fault location techniques that have been proposed. For example, research in [88] proposed the use of a probe unit to locate faults for DC traction power systems. A more accurate non-iterative algorithm, which considers the damping frequency and attenuation constant of the probe currents has been proposed in [89] to improve the accuracy of the original algorithm. The probe unit has also been used in DC marine systems [80] using Fast Fourier Transforms (FFT) to derive an active impedance estimation (AIE), and the impedance of the faulted path is used to estimate the fault distance. The limitations for these offline techniques require additional discharge devices that bring extra cost and the faulted section to be isolated first to avoid the interaction between these additional devices and grid supply. That leads to the requirements of the extra operating time. Besides offline fault location techniques, numbers of online fault

location techniques have been proposed. For example, research in [76] has proposed an online method that relies on the transient RLC response using the local voltage, current, and current derivative (i.e. dI/dt) measurements to estimate the impedance within the faulted path. However, this method only focuses on DC systems without fault current contributions from the remote end of the feeder. This is less likely to happen in LVDC distribution networks as widely integrated low carbon technology. Also, different smoothing capacitors of remote end converters have different impact on fault location estimation. The most straightforward method to eliminate this impact is to use a communication link to synchronize the measurement from both sides of the cable as illustrated in [90]. However, the reliance on communication links potentially leads to additional cost and reliability issues. Recently, methods based exclusively on local measurements have been proposed in order to provide accurate fault location estimation, even in LVDC distribution networks with remote fault current contributions. For example, the method presented in [91] uses the 'Prony' method to extract the attenuation factor and resonance angular frequency to determine the impedance of the faulted path. Also, the method in [92] introduces an improved mathematical model that considers remote end fault current contributions and improves the accuracy of fault distance estimation when the fault is located within 50% of the entire cable length. However, both of these two methods assume that the remote end converter has the same filter capacitor size as the main terminal converter. In LVDC distribution networks, the power ratings of the converter at the customer end are expected to vary depending on the local demand and power sources. Thus, the assumption made in [92] is not sufficient for representing the impact of the remote end fault current contributions. The limitations of existing fault location estimation methods are not only related to the insufficient determination of the impacts of the remote end fault current contribution, but also to the original current derivative-based mathematical model. Several existing fault location methods rely on the current derivative [89–93]. As the current derivative is very sensitive to noise (e.g. transducer noise), using current derivative to estimate the fault distance could lead to significant reliability (i.e. anti-noise capability) issues and consequently misrepresent action of the dI/dt. More details of the effectiveness of

current derivative based fault location techniques will be discussed in Chapter 4 and Chapter 6.

DC Measurement Transducers

The following part briefly reviews the available DC transducers that ensuring accurate current and voltage measurement.

Hall Effect Sensor is a commonly used DC transducer. There are open loop and closed loop types. The open loop sensor is the simplest application of the hall effect and the structure can be shown in Figure 2.28 [94]. A conductor that is flowing from current produces a magnetic field in a magnetic core. In the linear area function of material, the magnetic flux density is proportional to the primary current if and the hall voltage, V_h, is proportional to the magnetic flux density. The output signal of the hall device V_h is then further amplified to provide an instantaneous output voltage proportional to the primary current.

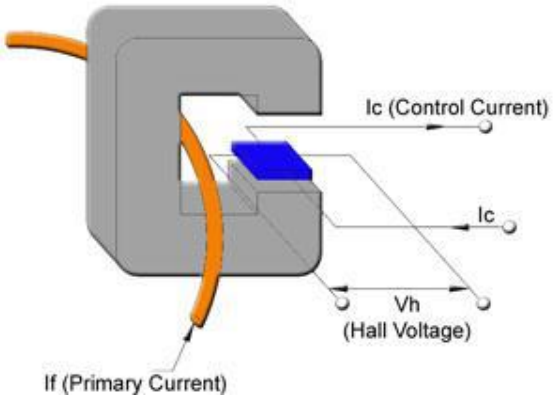

Figure 2.28: An example of an open loop hall effect sensor [94]

The close loop hall effect sensor has a similar circuit with the open loop, the difference being that there is an addition compensation circuit winding on the magnetic core which increases the performance of operation as shown in Figure 2.29. This design provides a good accuracy and linearity due to the winding compensation. In addition, the secondary winding will act as a current transformer at higher frequencies, which significantly increases the bandwidth [95].

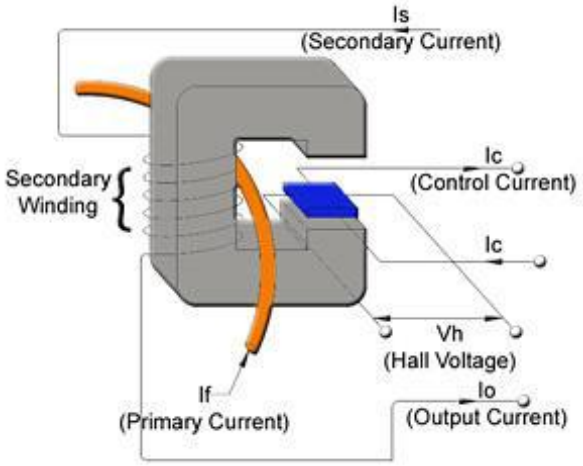

Figure 2.29: An example of a close loop hall effect sensor [94]

Fluxgate Current Sensor is similar to the closed loop hall effect transducer, using the same magnetic circuit with the difference in construction that replaces the hall plate with a probe coil (saturable inductor) comprising the secondary winding, as shown in Figure 2.30. It has high accuracy, linearity and sensitivity, wide range and fast response. This type sensors are very expensive while the design is complicated [96].

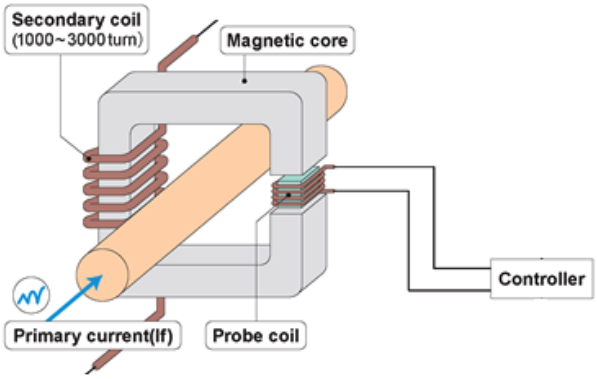

Figure 2.30: An example of a fluxgate current sensor [94]

Magnetoresistance Sensor is the property of a conducting material to change the value of its electrical resistance when an external magnetic field is applied to it. Depending on the material used, there are two types of magnetoresistive sensors: anisotropic magnetoresistance (AMR) sensors and giant magnetoresistance (GMR) sensors [97].

AMR sensors use ferromagnetic materials in which a magnetic field influences the electrical resistance [97]. GMR sensors rely on a significantly higher impact of the magnetic field on the resistance of a structure built of alternating ferromagnetic and nonmagnetic layers [97]. Figure 2.31 shows an example of a magnetoresistance sensor. Four magnetoresistance resistors are connected in a Wheatstone bridge to form a complete AMR sensor. The resistors are placed to represent a differential field sensor. With this way decreases a temperature drift and the interference fields eliminated. Magnetoresitance sensors have inherently low hysteresis and high linearity in the measurement accuracy. They have the extremely high bandwidth and can to detect magnetic fields with frequencies in the MHz region [97]. The comparison of the above typical DC transducers have listed in Table 2.2.

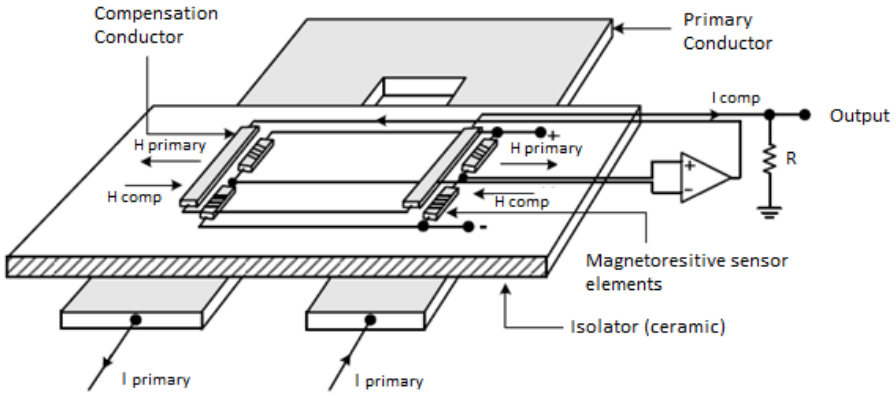

Figure 2.31: An exmaple of a magnetoresistance sensor [98]

Table 2.2: Comparison of typical DC sensors [94–98]

Details/Sensors	*Hall Effect Sensor*		*Fluxgate Sensor*	*Magnetoresistive Sensor*	
Core	Yes/No		Yes	No	
Current Sensor Type	Open loop	Close loop	Close loop	AMR	GMR
Accuracy	Low	Medium	High	Medium	High
Bandwidth	20kHz-800kHz		<1MHz	>2MHz	
Cost	Cheap	Normal	Expensive	Normal	

DC Circuit Breaking Devices

The development of LVDC protection solutions is not just in algorithms, but also in circuit breaking devices. As DC fault current does not have a zero-crossing point, as shown in Figure 2.32, arc extinguishing is more difficult than with AC faults [99].

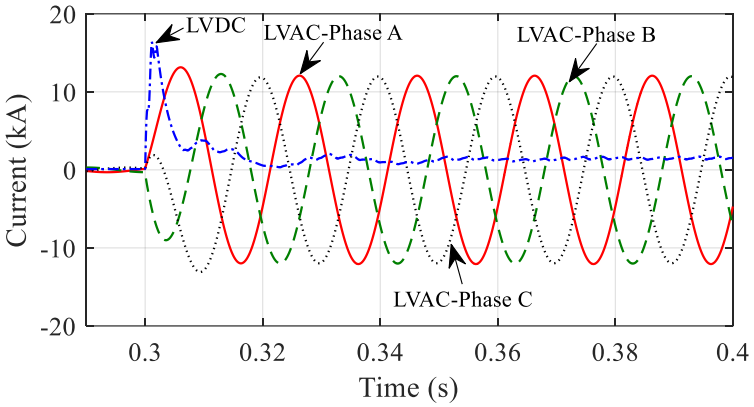

Figure 2.32: Fault current examples of AC three-phase short circuit fault and DC pole-to-pole fault at 0.3s

Several fault isolation devices have been proposed for LVDC systems such as DC fuses, Molded-Case Circuit Breakers (MCCB), SSCB, and hybrid circuit breakers.

Fuses are installed in series with power lines. Under fault conditions, the generated heat of the fault current melts the fuse, and the circuit is opened. Normally, fuses are divided into fast-acting and time-delay types [100]. Fast-acting fuses are mainly used to protect power electronic converters while delay fuses are used to protect high inrush current and surge current applications [100]. In DC systems where faults should be isolated within a few milliseconds, a conventional fuse is not a sufficient primary protection for LVDC distribution networks. Improved fuses have been proposed for DC systems [101] while DC fuses have been commercially available for protecting 1500V DC PV applications such as the ABB E90 series [102] and the Eaton Bussmann series [103].

Molded-Case Circuit Breaker (MCCB) consists of a quenching chamber, contacts, and a tripping device and have been commercially available for solar PV, electric traction, and other auxiliary services [104]. The Eaton series G-JG [105] and ABB Tmax T4 [104], are current examples and their technical specifications are listed in Table 2.3.

Table 2.3: Technical specification of two typical MCCB examples

	Eaton	**ABB**
Model	Series G-JG [105]	Tmax, T4 [104]
Operational DC Voltage	250V	125V, 500V, 750V
Trip Unit	Fix/Adjustable thermal/magnetic	Thermal/Magnetic, Electronic
Standards	IEC 60947-2	IEC 60947-2
Breaking Capacity	Up to 50kA at 250V DC	Up to 150kA at 250V DC

Solid-State Circuit Breaker (SSCB) makes use of semiconductor valves such as Metal Oxide Semiconductor Field Effect Transistors (MOSFET), Insulated Gate Bipolar Transistors (IGBT), Integrated Gate-Commutated Thyristors (IGCT), and Emitter Turn Off (ETO). High-speed MOSFET-based SSCBs have been developed [106], but due to the high on-state resistance of MOSFET, high loss under fault conditions is experienced [100]. Comparatively, IGBT-based SSCBs have shown improved performance but cannot provide bidirectional fault interruption. The lower loss IGCT-based SSCBs have been proposed, where using a reverse blocking IGCT (RB-IGCT), allows for bidirectional fault interruption. Also, RB-IGCT-based SSCBs developed by ABB, as shown in Figure 2.33, are commercially available and are efficient for protecting DC systems operating at voltages up to 1000V and nominal currents from 1000A to 5000A [107]. Faults can be isolated by activating IGCTs, and the Metal Oxide Varistor (MOV) absorbs the residual electromagnetic energy of the closed loop.

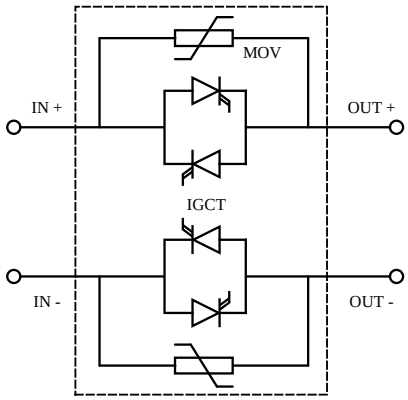

Figure 2.33: Schematic diagram of ABB RB-IGCT based SSCB [107]

Although fully SSCBs are effective and fast to protect LVDC systems, they are still relatively costly and have on-state losses, which slows their wide implementation. Several hybrid SSCBs have been proposed that combine a fast electromechanical CB with a solid-state commutation bypass, which provides an acceptable protection speed while also being cheaper with lower conduction losses than standard SSCBs [108].

2.3 Remaining Technical and Economic Challenges for the Increasing Use of LVDC Distribution Networks

The majority of LVDC distribution networks are still at the conceptual or prototype stage only and a limited number of practical examples have been deployed. To pave the way for wide implementation of LVDC distribution networks, there still remains some technical and economic challenges.

In terms of technical challenges, although there are a lot of DC application standards available, public LVDC distribution networks still lack standards for regulating and guiding technical aspects such as power quality, voltage levels, protection solutions, and grounding systems. Currently, there is still no definitive consensus on the voltage levels of the DC distribution networks, where Finland (750V/±750V), Netherlands (700V/±350V), Korea (±750V/380V/±190V) and China (±750V/220V) all adopt different approaches as mentioned in section 2.2.3.

LVDC protection is the main issue within the technical challenges that dominates the restricted implementation of DC distribution networks. As discussed before, existing trial projects are mainly based on using conventional overcurrent protection, with an overrated converter to withstand fault conditions. However, DC fault response depends on interface converters. As introduced in section 2.2.4, different converters have different fault current contributions. Conventional protection solutions (e.g. overcurrent protection) rely on significant fault currents of two-level VSCs, which are more likely to be influenced by integrating with new power conversion technologies (e.g. DAB converters and SSTs). The fault current contributions of converters and their protection functionalities need to be regulated with guidelines to ensure the reliability, selectivity,

and speed of LVDC protection solutions. Meanwhile, protection algorithms need to be considered with different converter topologies within different network configurations. Future LVDC distribution networks are less likely to have the same power conversion interfaces and standardization groups have to cover these scenarios in order to guide engineers to ensure reliable and secure LVDC distribution networks.

The need for guidelines is not just related to the impacts of converters on protection solutions and coordination between converters and protection solutions, but also in protection devices. There are several DC protection devices (such as fuses and MCCB) available in the market, but they are just for individual DC applications. When they are used to protect complex public distribution networks, standards should provide regulations for their performance within the networks. Also, emerging technologies such as fault current limiters and SSCBs still lack standards and regulations to guide their installations in future LVDC distribution networks. These two technologies need to be considered with interface converters and protection algorithms as they could significantly influence DC fault behaviours and protection requirements. Although there are some pilot projects installed across the world, the guidelines they follow are based on existing AC or DC applications. More technical justifications are required when constructing a public LVDC distribution network. Besides, other technical challenges such as earthing systems, wiring, post-fault maintenance, and communications still lack guidelines and standardization.

Apart from the technical issues, critical economic challenges still exist such as lack of market maturity for appliances that have a DC input and can readily operate on DC. This is also caused by the limited numbers of products that use DC input directly and most of the existing DC devices are connected with rectifier stages. Only a few manufacturers pay attention to DC products which consequently slows the development of the DC market. The manufacturers are essential to forming the new DC market that could provide competition to facilitate the expansion of DC distribution networks. The DC market is currently restricted by the relatively high capital investment costs required where, the initial investment is higher than the AC option, for example, the high protection cost. Even though DC protection technologies are developing, pro-

tection devices are still more expensive than AC solutions [109]. Several pilot LVDC projects with expensive approaches maybe appropriate for industrial applications but is not appropriate for the standardised studies that are essential to establishing low cost and widely used utility applications.

2.4 Area Identified for Research

From the above literature review, it can be concluded that economic challenges are partially led by technical challenges that slow the progression of wide scale implementation of LVDC distribution networks, especially significant being effective and reliable DC protection solutions. In order to bring greater clarity to how these protection issues should be tackled three clear opportunities for research contributions have been identified.

Firstly, there is an opportunity to investigate the impacts of SST and a commonly-used two-level VSC on the fault characterisation of LVDC distribution networks. In this thesis, SST is selected for the further research work since SST is regarded as an emerging technology with high potential to be implemented in practical areas and it has unique fault characteristics [63]. This investigation is mainly focused on the quantification of the difference in fault behaviour in terms of voltage, current, and fault let-through energy. Based on this, an evaluation of the impacts of these differences on the performance of existing protection solutions to define design requirements for future LVDC distribution networks is considered.

Secondly, an opportunity exists to better coordinate protection solutions and converter protection functionalities (i.e. limiting and blocking). In particular, to develop a higher speed, more selective, and reliable LVDC protection scheme for an SST interfaced LVDC distribution network. Based on the literature review, most of the existing protection solutions are based on the two-level VSC that can generate high fault currents, the reasons for using two-level VSCs being their simplicity and low cost. However, the SST has been considered as an inter-link between MVAC, MVDC, LVDC, and LVAC, and it can allow for more compact substations by reducing their footprint and adding more

control functionalities, but with limited fault current. Protection solutions for LVDC distribution networks interfaced by an SST are quite limited, creating an opportunity for research contribution.

Thirdly, there is an opportunity to develop a more reliable and accurate fault location technique to facilitate LVDC post-fault maintenance. Most of the existing fault location solutions are based on current derivatives which are easily influenced by transducer noise. Meanwhile, the impact of remote end converters have not been sufficiently examined. These factors deeply influence the accuracy of fault distance estimation, which provides an opportunity for research contribution.

Each of these opportunities have been pursued in the work reported in this thesis.

2.5 Chapter 2 Summary

This chapter briefly introduces the key drivers towards the use of LVDC, identifying how the pressure on LV networks, developments in power electronics, increasing applications operating with DC, and the claimed benefits of using LVDC, are enabling the transition to LVDC distribution networks. Following this, the development of LVDC distribution networks in terms of concept, updates on standards, and updates on pilot projects are examined. Also, LVDC technologies, especially for LVDC interfaces and LVDC protection solutions are introduced on the basis of the available literature. Based on this literature review, existing technical and economic challenges for increasing the use of LVDC have been outlined. This justifies the selection of DC protection as the main topic for this research study.

From the review of relevant literature, several key findings were drawn. First of all, most of the existing protection solutions are designed based on the two-level VSC interfaced LVDC. However, more advanced converters such as SSTs are going to be installed in existing networks as they can provide hybrid AC and DC power supplies with more flexible controls. The limited fault currents of SSTs will influence the performance of existing protection solutions and as such, the remainder of this thesis will focus on the development of protection solutions for this converter type.

Secondly, it was concluded that in order to accurately define the requirements of network protection, a detailed approach for characterisation and protection evaluation of future LVDC distribution networks driven by new converters is required. This will in turn facilitate the understanding of how significantly the SST will influence the performance of available protection solutions.

Additionally, it was concluded that in order to better coordinate the fault current management capabilities of SST and downstream converters, a method capable of providing effective fault detection and discrimination without relying on the current magnitude is required.

Finally, it was concluded that to facilitate post-fault maintenance, a more accurate and reliable fault location technique to estimate fault distance is required which does not rely on current derivatives but accurately considers the impact of remote converter fault current contributions.

Chapter 3

An Approach for Fault Characterisation and Protection Evaluation of Future LVDC Distribution Networks

Chapter 2 has identified the key research objectives that will be addressed in the subsequent chapters of this thesis. Before thinking about the novel fault protection and location solutions however, it is necessary to characterise DC faults while sufficiently evaluating the effectiveness of existing protection solutions. This is especially important because new converter topologies will be implemented in future LVDC distribution networks, which have great potential to influence DC fault characteristics and thus the effectiveness of protection solutions. The proposed approach analyses the DC fault characteristics of the new converter based on numerical calculations and software-base simulation validations, quantifies the difference between the new converter and traditional two-level VSC, and highlight the fault-let through energy reduction beneficial of implementing the new converter. This helps improve the understanding in the reduction of thermal ratings of power electronic components when the new converter is implemented. While the proposed approach evaluates and quantifies the effectiveness of

existing protection solutions in terms of protection speed and fault discrimination capabilities. This improves understanding on the weakness of existing protection solutions and the impacts of using new converters, which facilitates the development of advanced protection solutions that provide enhanced protection performance which also applies to the newly implemented converter. The first section of this chapter will present an overview and the main framework of the proposed approach for fault characterisation and protection evaluation.

3.1 Fault Characterisation and Protection Evaluation: Designing a suitable approach

3.1.1 A Suitable Fault Characterisation Approach

In general, fault characterisation is conducting fault analysis using numerical calculations or simulation tools to describe fault profiles (e.g. current and voltage) that helps health and safety considerations, design, operation and protection of power systems, and design of power system equipment [110]. Original DC fault characteristics have been summarised by IEC61660 [111]. Also, the work in [112] has characterised the performances of a passive LVDC distribution system under different fault conditions and outlined the requirements for the improvements of IEC 61660. In [113], the fault characteristics of individual solar photovoltaic and battery energy storage systems are investigated. However, LVDC distribution networks expect to host high penetration of renewables, which bring different types of converters. These makes LVDC distribution networks fault characteristics more complex due to different fault limiting and blocking capabilities of converters. Existing fault characterisation approaches have not considered the fault current managements capabilities of converters (e.g. fault current limiting and blocking) and have not determined the reductions of fault let-through energy by implementing new converters with these fault current management capabilities. Therefore, the new fault characterisation approach is proposed in this section that derives the fault profiles with considerations of fault current management capabilities of converters and quantifies the difference between the new converter and existing two-level VSC,

which provides more precise understandings of fault behaviours that facilitates design of protection and power system equipment. The proposed approach is summarised in Figure 3.1, and the following section describes the steps.

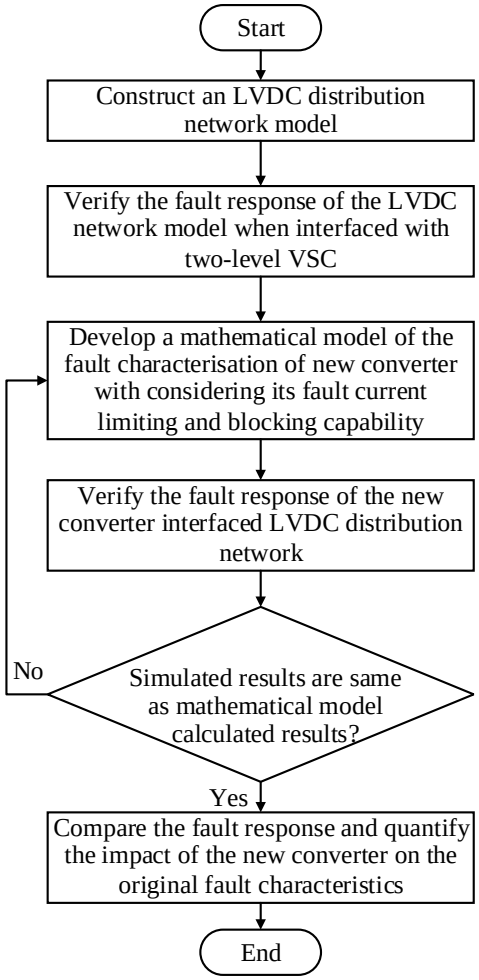

Figure 3.1: An approach for fault characterisation of future LVDC distribution networks

1) Construct an LVDC distribution network model. The model should be suitable for implementing new converter and the basic two-level VSC while remaining within the acceptable normal operation conditions. Using the parameters such as voltage ripples, system response speed to step changes, and voltage drops from existing LVDC trial projects is a potential way to make sure the model is working properly;

2) Verify the fault response of the LVDC network model when interfaced with two-level VSC. After building an LVDC distribution network model, the fault characteristics of basic two-level VSC must be verified to ensure the model is working properly under faulted conditions, with verification focused on short circuit faults. More specifically, solid fault scenarios are used for the initial simulation study. In order to ensure the accuracy of the two-level VSC model interfaced with an LVDC network, relative parameters such as nominal voltage and fault impedance are input into the existing mathematical model [77] of two-level converter. This is done to compare the mathematical model calculated values of the selected parameters such as peak fault current, time to peak fault current, transient current derivative, and transient voltage derivative with what have been presented in the simulation result. In addition, quantification of the fault let-through energy of a two-level VSC based LVDC distribution network is used as a reference for understanding the significance of the fault current stress on the existing two-level VSC and further identification of the impact of using the new converter on releasing the fault stress.

3) Develop a mathematical model of the fault current characteristics of the new converter. The DC fault characteristic based on the two-level VSC is defined through the three fault stages capacitor discharge, diode free-wheeling, and grid contribution. In this step, the topology of the new converter is compared with the basic two-level VSC. Identify the difference in each fault stage of the new converter and basic two-level VSC and, derive the mathematical model of the new converter based on the existing model of two-level VSC;

4) Verify the fault response of the new converter. This step verifies the simulation results with the developed mathematical model. Similar to step 2, short circuit fault simulation studies are performed. The relative parameters such as nominal voltage and fault impedance are input into the developed mathematical model and to compare the mathematical model calculated values of the selected parameters (e.g. peak fault current, time to peak fault current, transient current derivative, and transient voltage derivative) with what have been presented in the simulation results. This is done to ensure the mathematical model achieves a good level of accuracy.

5) Compare the fault response and quantify the impact of the new converter on the original fault characteristics. Once the fault characteristic of the new converter interfaced LVDC distribution network is verified, compare the fault response (current peak, time to peak, transient current derivative, transient voltage derivative, and fault let-through energy) to the LVDC distribution network interfaced by the two-level VSC and quantify the difference between the new converter and two-level VSC. This step gives an understanding of the impact of the new converter on the fault characteristics.

3.1.2 Protection Evaluation Approach Design

After conducting the fault characterisation of the new converter interfaced LVDC distribution network, it is necessary to understand its impact on the effectiveness of existing protection solutions. Existing evaluation methodologies [114–116] are mainly focused on protection philosophies but not consider the impacts of converter topologies on the effectiveness of protection solutions. Therefore, a new protection evaluation method is proposed to facilitate the understanding of the impact of different converter architecture and controls. This is important to help provide recommendations for future protection solutions when new converters are applied. The approach for the evaluation of existing protection solutions on an LVDC distribution network interfaced by a new converter is shown in Figure 3.2, and described in more details as follows:

1) Identify typical LVDC protection solutions. These typical LVDC protection solutions are mainly implemented in existing LVDC trial projects, LVDC applications, and proposed in highly cited research articles;

2) Collect technical specifications of the selected protection solutions. This step specifically focuses on collecting protection threshold settings from practical use cases (e.g. real LVDC implementations and trials), existing LVDC application standards, and highly cited research articles;

3) Model the selected protection solutions in the LVDC distribution network by simulation tools. The LVDC test network model that is used for fault characterisation is also used for protection evaluation. Model the selected protection

solutions in the selected LVDC test network with the collected technical specifications.

4) Define and select the evaluation scenarios. Choose appropriate evaluation parameters that are sufficient to reflect the effectiveness of the selected protection solutions. The current approach considers protection speed, fault discrimination capability, protection sensitivity and high resistive fault detection capability, protection reliability (i.e. considering the impact of measurement errors and communication delay):

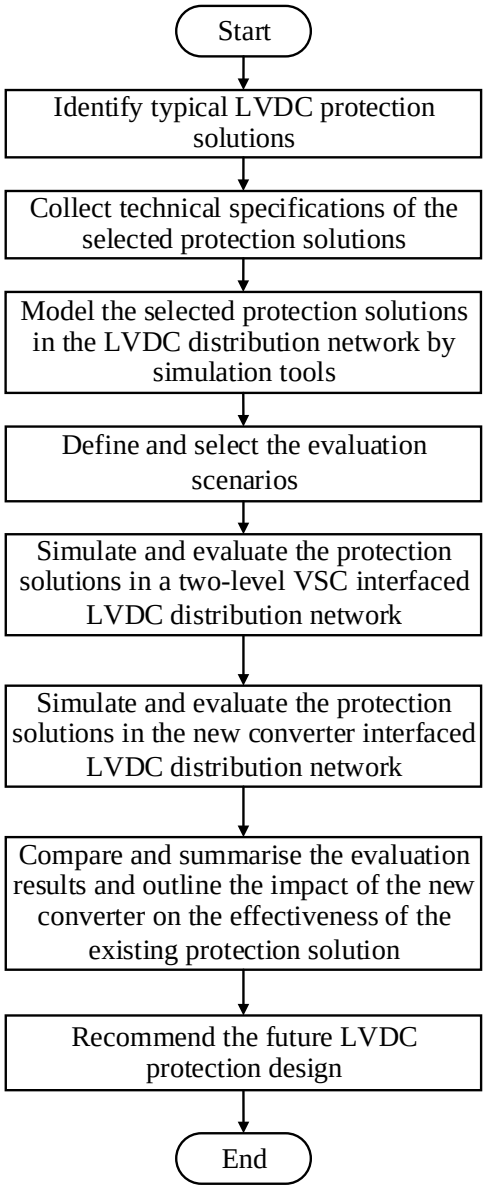

Figure 3.2: An approach for protection evaluation of future LVDC distribution networks

(i) **Protection speed**: to determine if the protection speed is within the required time window or not;

(ii) **Fault discrimination capability**: determine if the protection solution is effective at discrimination between downstream and upstream faults at different locations (i.e. internal and external faults). Investigate the reasons for discrimination failure of the selected protection solutions if requires;

(iii) **Protection sensitivity**: to identify the maximum high resistive fault detection capability of the selected protection solutions;

(iv) **Protection reliability**: to determine the impact of measurement errors and communication delays and investigate their capabilities to withstand these factors;

5) Simulate and evaluate the protection solutions in a two-level VSC interfaced LVDC distribution network. An evaluation of existing protection solutions through quantitative assessments is considered in this step. Simulate the selected protection solutions in a basic two-level VSC interfaced LVDC distribution network with the defined scenarios to set up a reference of protection performance. This reference is used to determine the impact of the new converter on the effectiveness of existing protection solutions;

6) Simulate and evaluate the protection solutions in a new converter interfaced LVDC distribution network. The protection solutions are simulated and evaluated against the same fault scenarios and compared to the protection performance of the basic two-level VSC interfaced LVDC distribution network to quantify the difference in the defined evaluation scenarios.

7) Compare and summarise the evaluation results and outline the impact of the new converter on the effectiveness of the existing protection solution. This step aims to identify the limitations of existing protection solutions when these are deployed in new converter interfaced future LVDC distribution networks.

8) Recommend the future LVDC protection design. Based on evaluation and discussions, recommendations for future LVDC protection design are outlined to over-

come the limitations of existing protection solutions. The recommendations serve as guidelines for changing converter controls and architecture and developing novel protection solutions and techniques.

The above section has introduced the framework for conducting fault characterisation and protection evaluation for future LVDC distribution networks driven by new converter topologies. The remainder of this chapter will introduce the details of the LVDC test model that will be used with the above approach. The SST is selected as the new converter topology due to great potential for replacing existing LV transformers and its unique fault characteristics, as reported in Chapter 2, and more detail of the relevant studies will be presented in the next chapter.

3.2 Modelling of an LVDC Distribution Network with different converter interfaces

This section introduces the development of an LVDC distribution network model with different converter interfaces. The detailed two-level VSC and two-stage SST are modelled in order to conduct further comparison studies in the following Chapter.

There are mainly two types of LVDC systems (i.e. single-bus and multiple-bus) that have been proposed by research and industrial groups, which consider different requirements and applications [85]. For example, single-bus LVDC systems have been widely used in automotive and telecommunication industries at 12V and 48V [25]. Multiple-bus configurations have been used to provide the interconnections within systems, demonstrating the higher reliability and flexibility, especially under fault conditions and during post-fault maintenance [116]. Since the main focus for the following research work is characterising LVDC last mile distribution networks, an LVDC test network based on multiple-bus configurations is introduced and modelled in PSCAD/EMTDC. The parameters of the LVDC test network are based on practical LV distribution networks and LVDC trial projects. The structure of the network is shown in Figure 3.3, which is developed from the LVDC network model presented in [117]. Compared to the model presented in [117], this LVDC network model contains a two-level VSC and an

SST as main interface converters and downstream dual active bridge (DAB) DC/DC converters that can provide fault current limiting and blocking capabilities, which is capable of emulating LVDC distribution networks with reduced fault levels under short circuit fault conditions.

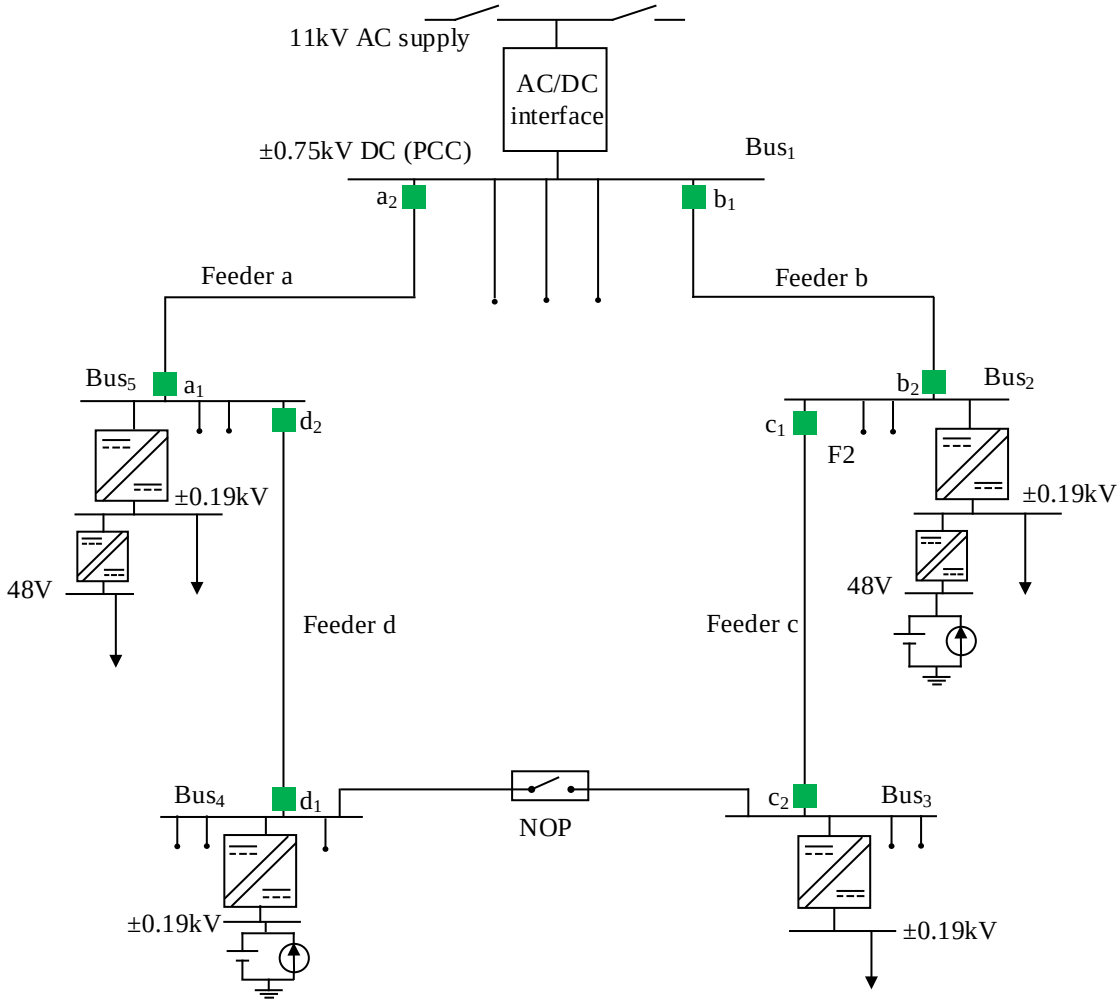

Figure 3.3: An LVDC test network with different converter interfaces

The entire network is supplied by 11kV AC (modelled with a 174MVA fault level and an X/R of 8.6 [118]). The LVDC network is connected to the 11kV AC grid through an 11kV/0.4kV conventional 50Hz transformer and a two-level VSC or an SST. A two-level VSC is built for comparing the performance of the two converter topologies. In this LVDC test network, AC/DC interfaces provide 1.5kV (±0.75kV) DC, and midpoint

grounding is used for facilitating the detection of pole to ground faults [119]. The two main feeders are modelled as a resistor (R=0.164Ω/km) connected in series with an inductor (L=0.24mH/km) [117]. Cable capacitance has been neglected due to its small value and its small influence when compared to the smoothing capacitors of converters in the test network [111]. The length of each cable is selected as 0.25km. This choice is based on a trade-off between the maximum transfer power of DC cables and the acceptable voltage level for the remote end AC inverter for powering AC customers [120]. The LVDC network supplies AC and DC loads through two-level VSCs and DAB DC/DC converters with galvanic isolation, since these two types of converters are widely used for grid interconnections [32]. The DC customers are supplied by ±0.19kV. The battery storage systems at the DC customer side are aggregated and are assumed to be ideal DC voltage sources that are used to emulate fault current contribution of battery storage under DC fault conditions [113]. The selection of ±0.19kV for the DC customers side is based on existing DC trial projects and the DC safety consideration [2]. The model details of each component are developed as follows.

3.2.1 AC Grid Supply

The MV Grid Supply Point (GSP) is developed as an ideal 11kV three-phase voltage source connected in series with an equivalent impedance to provide a fault level of a real distribution network based on a SP Energy Networks urban example [118]. Port Dundas GSP and Charles Street secondary substation in Glasgow, UK are selected to be modelled as the AC grid supply. Table 3.1 lists the fault level data used in the developed network model. Figure 3.4 illustrates the simulated three-phase 11kV RMS and instantaneous voltages under a three-phase short circuit fault at 0.3s. The simulated fault current is given in Figure 3.5 which is similar to the actual value given in Table 3.1.

Table 3.1: Fault level parameters used for the test network [118]

Voltage	**R**	**X**	**X/R ratio**	**Fault Current**
11kV	0.0766Ω	0.6587Ω	8.6	9.14kA

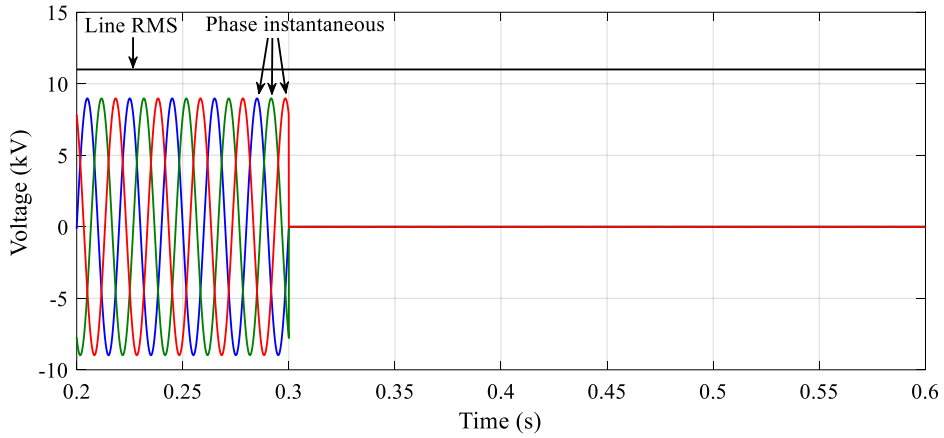

Figure 3.4: Three-phase voltages under a three phase short circuit at 0.3s

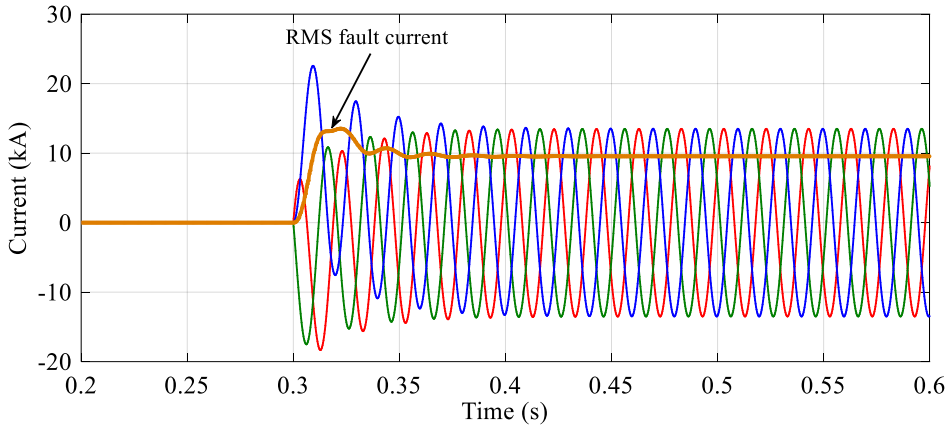

Figure 3.5: under a three phase short circuit at 0.3s

3.2.2 Performance Requirements of Converter Interfaces

In the test network, two-level VSC and SST are considered as two-level VSCs have already been implemented [32] while SSTs are expected to be implemented in the near future [63]. An LVDC voltage of ±0.75kV is considered as the output of the converters and is used to test the fault transient behaviour of the system at the highest possible voltage which can be classified as LV systems as identified by IEC60038 [30]. Currently, there are no UK standards that define the acceptable DC voltage ripple and response time for power flow and voltage control of converter interfaces in public LVDC distribution networks. However, some regulations from existing DC applications have been reported, such as a maximum 10% voltage ripple in DC marine systems [121].

Moreover, based on an existing pilot project in an LVDC research site in Korea, a ±0.7% voltage ripple is acceptable for the AC/DC converter [39]. In terms of response time requirement of power flow and voltage control, an technical specifications document of SST performance has outlined the response time for power flow control should be less than 2s [122]. Therefore, based on the above information, the modelling requirements of acceptable performance are listed below:

- Voltage ripple is less than ±0.7%
- Control error is less ±0.7%
- Voltage and power control response time are less than 2s

To validate the performance of the modelled converter that can follow the above roles, ±10% step changes in voltage and power control are used to make sure the simulated step change results are acceptable.

3.3 Model of a Two-level Voltage Source Converter

The two-level VSC detailed model is designed to have 1MW power capacity based on an existing example [64]. The circuit diagram is illustrated in Figure 2.12. The selection of the choke inductor is designed based on equation (3.1) [123], where, the switching frequency, *fs*, 2kHz, the peak-to-peak ripple current $I_{p\text{-}p}$, is 5% of the line peak current, and the maximum current rating, *a*, is 120% of the nominal current [123, 124]. The size of selected choke inductance has been listed in Table 3.2 together with other key parameters.

$$L_f = \frac{\sqrt{3}}{2} \cdot \frac{m_a \cdot V_{DC}}{6 \cdot a \cdot f_s \cdot I_{p-p}} \tag{3.1}$$

The main controller is modelled as shown in Figure 3.6, where a phase lock loop (PLL) is used to rack the angle, θ, of the grid voltage that is used in the Clark and Park transformations [125]. By using the PLL and Clark and Park transformations, the AC voltage and current are decoupled in the synchronous d-q reference frame.

Table 3.2: Parameters of two-level voltage source converter [123]

Choke inductance	Filter capacitor	Switching frequency	DC voltage	Reactive power	Signal modulation
0.88mH	10mF	2kHz	±750V	0Var	PWM

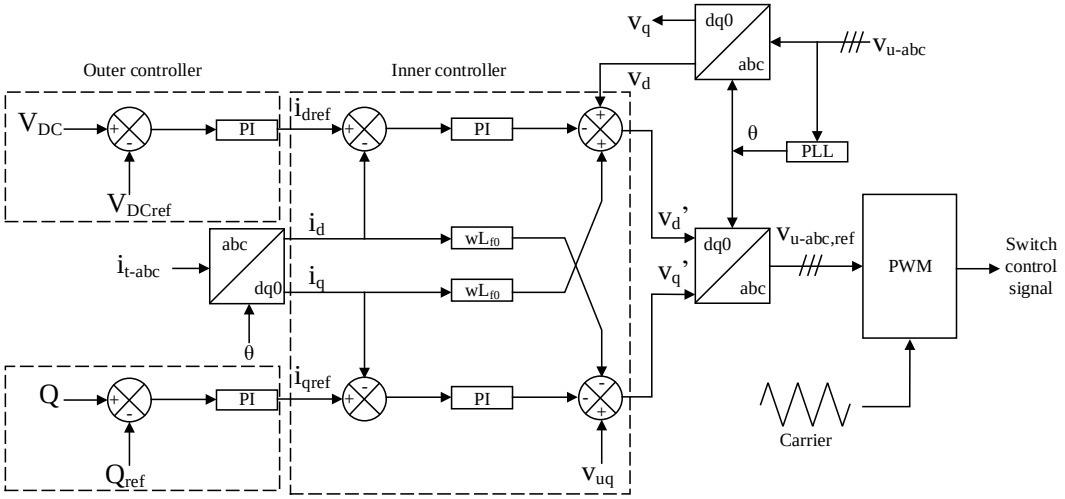

Figure 3.6: Vector control diagram of two-level voltage source converter

The relative current reference in the d-q frame, i_{dref}, is determined by the desired DC voltage or active power, while i_{qref} is obtained from the set-point reference of the reactive power or AC voltage. Each of these current references is controlled by the outer controller. For example, AC/DC converters are mainly used to regulate DC link voltage (i.e. V_{DC}) and reactive power (i.e. Q) injection or absorption from the AC grid. The outer control commonly uses Proportional-Integral (PI) controllers to act on V_{DC} and Q differences from the set-points, in order to generate the current references, i_{dref} and i_{qref}, respectively. These are in turn used by the inner current controller to generate the new d-q voltage references as illustrated in equations (3.2) and (3.3) [124] where L_{f0} is the choke inductance, ω is the grid frequency, and V_d' and V_q' are the generated voltage references that are transferred back to the phase equivalent AC voltage waveforms. The generated voltage references are used for the Pulse Width Modulation (PWM) generation for switching the power electronic devices of the converter to synthesize the desired AC voltage waveforms.

$$V_d' = -L \cdot \frac{di_d}{dt} + \omega \cdot L_{f0} \cdot i_q + V_d \tag{3.2}$$

$$V_q' = -L \cdot \frac{di_q}{dt} - \omega \cdot L_{f0} \cdot i_d + V_q \tag{3.3}$$

In the test network, the AC/DC converter regulates the DC voltage and reactive power flow of the AC grid. Figure 3.7 and Figure 3.8 show the step change response of DC voltage and reactive power of the two-level VSC with ±10% reference changes.

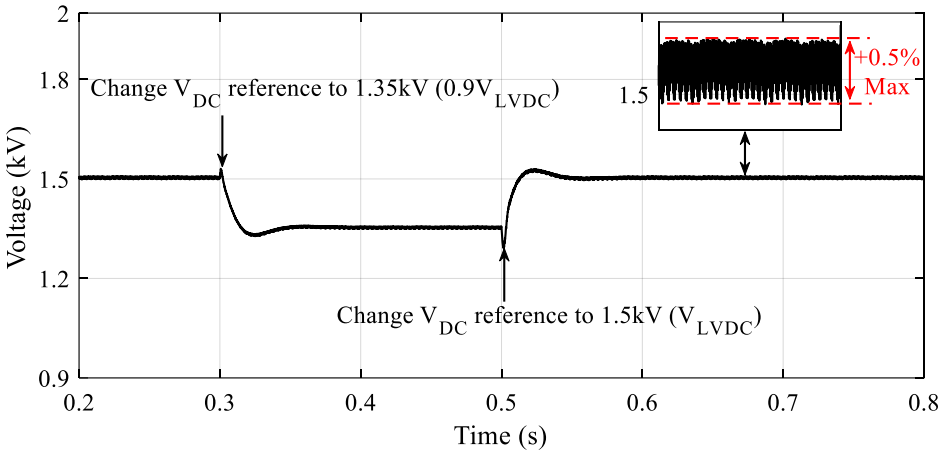

Figure 3.7: DC voltage step response of two-level VSC

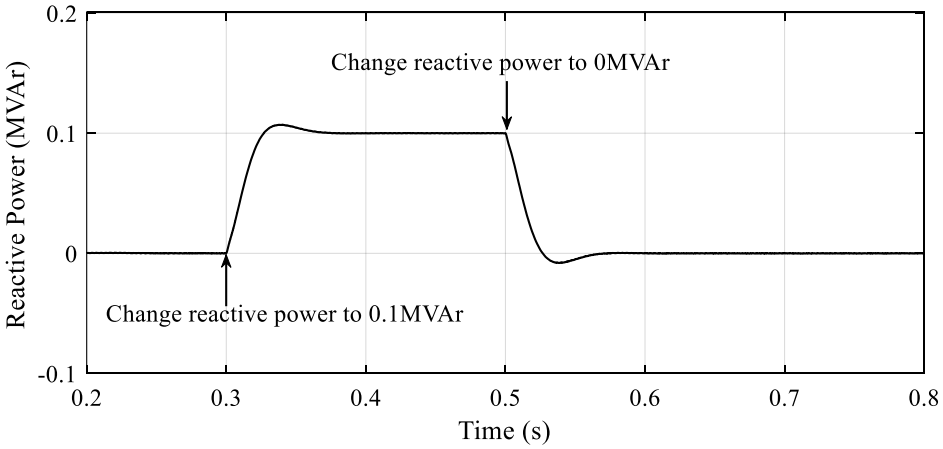

Figure 3.8: Reactive power response of the modelled two-level VSC

The modelled two-level VSC shows a 0.5% voltage ripple that is within the performance requirement range listed in Section 3.2.2, while the fast and accurate response shows the effectiveness of the reactive power control of the modelled two-level VSC. Thus the suitability of the steady state operation of the model is validated.

3.4 Model of a Two-stage Solid-state Transformer

The topology of the modelled SST is similar to the topology shown in Figure 2.17 [126]. The two-stage SST is modelled as a combination of a basic two-level VSC and a DAB DC/DC converter with galvanic isolation. The output voltage of the SST is MVDC (±10kV)/LVDC (±750V). The voltage selection of the MVDC side has been selected based on a demonstration project [127]. The first stage is an MVAC/MVDC stage that is conducted by a two-level VSC. The controller of the first stage is similar to the controller presented in Figure 3.6. This two-level VSC controls the DC link voltage (20kV) on the MVDC side and the reactive power (0MVAr) on the MVAC side. Figure 3.9 and Figure 3.10 show the DC voltage and reactive power response with ±10% step changes at 0.3s and 0.5s, respectively. The dynamic response of voltage only has ±0.12% voltage ripple. While, fast and accurate voltage and power response indicate that the first stage of SST works properly under steady-state conditions.

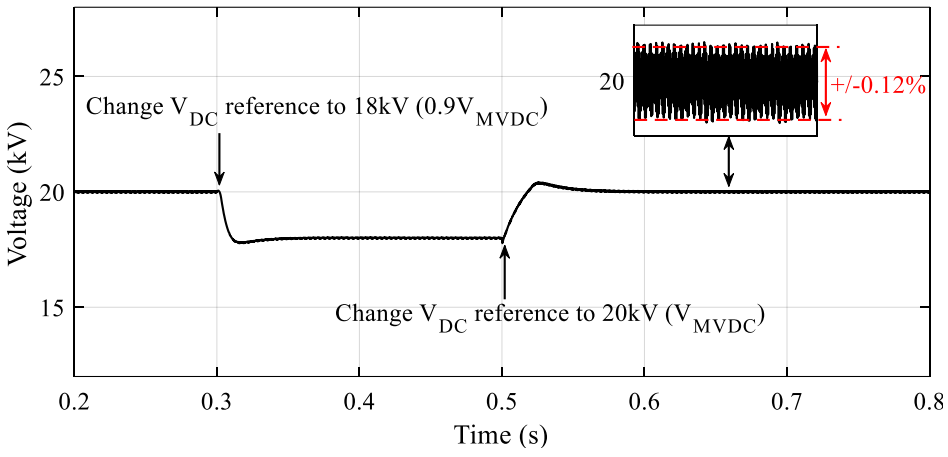

Figure 3.9: MVDC voltage step response of SST

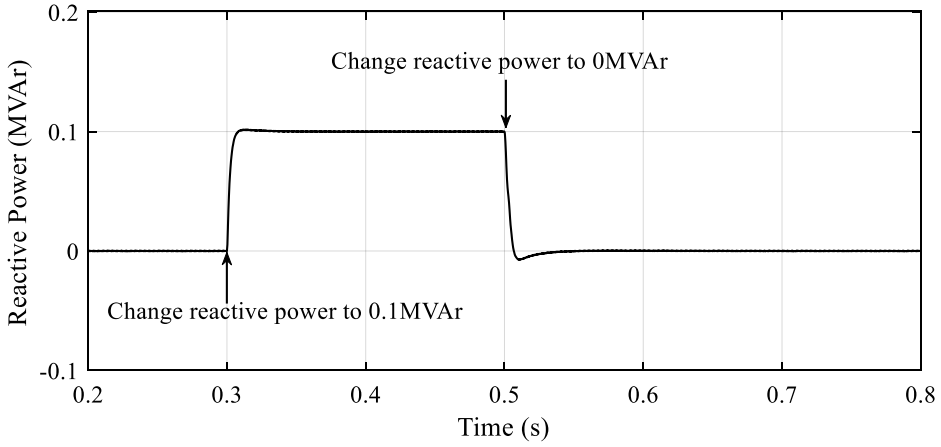

Figure 3.10: Reactive power response of the AC/DC stage of SST

The second stage conversion (i.e. MVDC/LVDC) is comprised of a DAB DC/DC converter with galvanic isolation (i.e. high-frequency transformer). The DAB converter is modelled as a DC voltage regulator to maintain the DC voltage (i.e. ±750V) on the LVDC side while phase-shift based voltage and current controllers are used [59]. The power exchange between the primary bridge and the secondary bridge of DAB DC/DC converter is based on the phase shift between the voltages on the primary bridge and the secondary bridge. As expressed in equation (3.4) [59], V_{MV} and V_{LV} are the voltages on the primary and secondary sides of DAB, φ is the phase shift between these two voltages, n_T is the transformer turn ratio of the galvanic isolation transformer, f_s is the switching frequency and L is the auxiliary inductance. In order to reduce the circulating current and to increase the efficiency, the transformer turns ratio, n_T, should match the voltage conversion ratio of DAB, that is, n_T=V_{MV}/V_{LV} [128].

$$P = \frac{n_T \cdot V_{MV} \cdot V_{LV}}{2 \cdot \pi \cdot f_s \cdot L} \cdot \varphi \cdot (\pi - \varphi) \tag{3.4}$$

Also, the selections of auxiliary inductance, L, and switching frequency f_s must ensure the smooth power transfer of the DAB converter to serve the nominal load. Thus, the theoretical maximum power should be larger than the rated power of load as illustrated in (3.5) [129] where P_N is the rated power, λ is the margin coefficient (e.g. 4/3 [129]), and $V_{MV\text{-}min}$ and $V_{LV\text{-}min}$ are the minimum voltages on the MVDC

and LVDC sides respectively that are set to 90% of the nominal voltage. The switching frequency f_s is determined by the characteristics of the electronic switches, which is usually below 20kHz [128]. The parameters of the modelled DAB converter are listed in Table 3.3.

$$\frac{n_T \cdot V_{MV-min} \cdot V_{LV-min}}{8 \cdot f_s \cdot L} \geq \lambda \cdot P_N \tag{3.5}$$

Table 3.3: Parameters of DAB converter

Primary voltage	**Secondary voltage**	**Switching frequency**	**Auxiliary inductor**	**Filter capacitor**	**Signal modulation**
±10kV	±0.75kV	20kHz	1.52mH	10mF	PWM

The purpose of the controller is mainly to control the phase-shift between the primary bridge and the secondary bridge, which is dependent on the difference between the reference (i.e. current or voltage) and dynamic voltage and current signals [130]. In normal operation, the DC/DC stage is mainly used to maintain the DC link voltage in the LVDC side that is controlled by the phase-shift-based voltage control as shown in Figure 3.11 [130]. Figure 3.12 shows the LVDC voltage of SST can effectively follow the reference step changes with only ±0.3% voltage ripples that is within the converter requirement listed in Section 3.2.2.

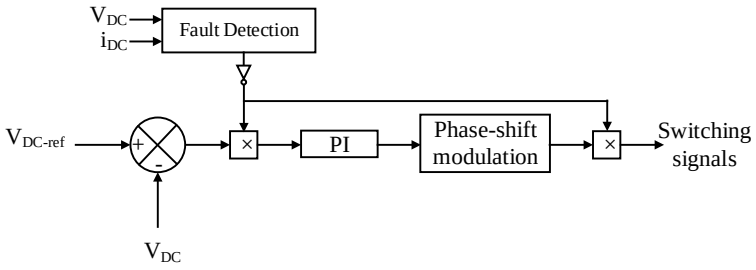

Figure 3.11: Voltage controller of DAB converter [130]

Under fault conditions on the LVDC side, the SST is controlled by current control as shown in Figure 3.13 [131]. This control is used to limit the output fault current from the upstream side. With the implemented current control, the fault current can be limited to help the two-stage SST ride through the LVDC fault conditions. For example,

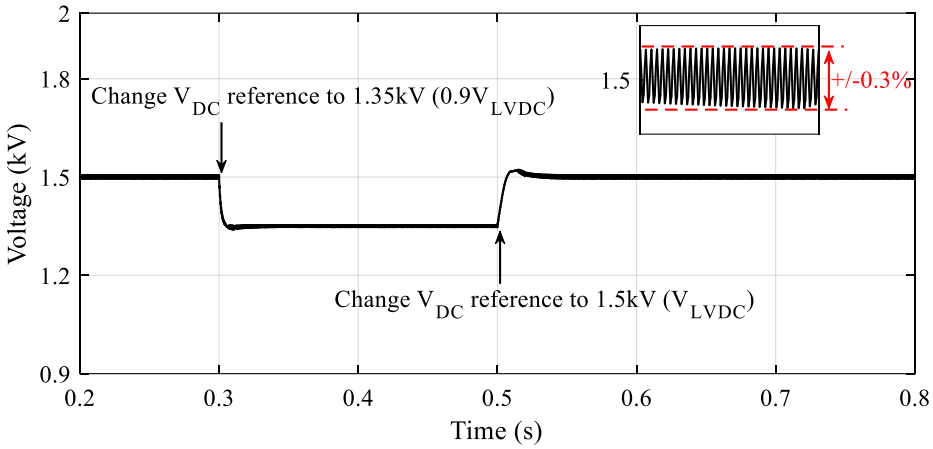

Figure 3.12: Voltage step response of DAB converter (LVDC side)

Figure 3.14 shows the DC current limiting capabilities of SST with the different current references (e.g. $0.9 \cdot i_{nor}$ and $0.8 \cdot i_{nor}$, where i_{nor} is the nominal current).

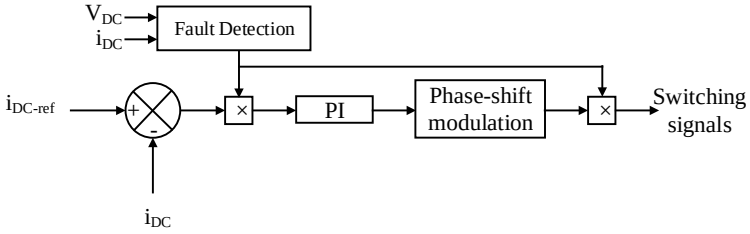

Figure 3.13: Current controller of DAB converter

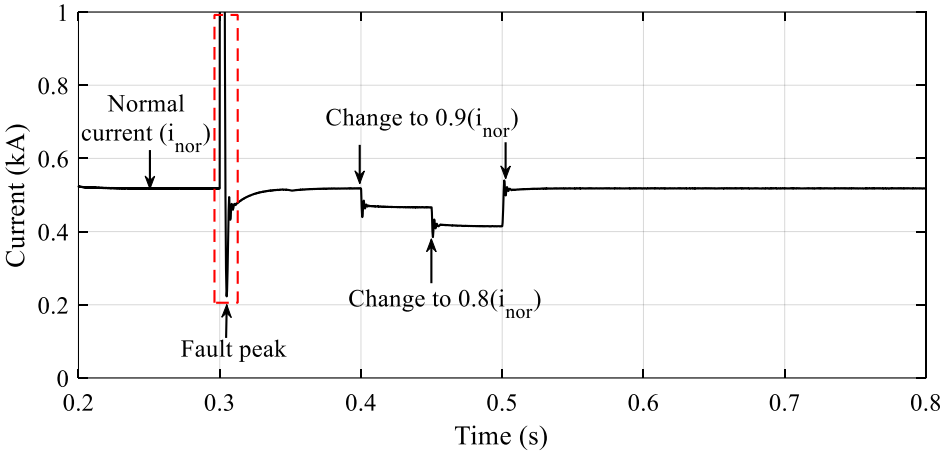

Figure 3.14: An example of LVDC fault current response of DAB converter

3.5 Model of a Dual Active Bridge DC/DC Converter

In the test network, every DC customer is interfaced by a DAB converter with galvanic isolation. The converter topology is similar to that described in Section 2.2.4. The converter provides ±0.19kV DC voltage. The principle of the power transfer between the primary and secondary bridges of DAB converter that was introduced in Section 3.3 also serves as the basis of the control of the customer side DAB converter [132]. In addition, the phase shift based voltage controller has been applied to control the local customer DC link voltage (±0.19kV). The converter operates at 20kHz frequency. Based on the power capacity (i.e. 200kW), the auxiliary inductor is calculated via (3.5). The parameters of the customer DAB converter are listed in Table 3.4.

Table 3.4: Parameters of DC/DC DAB converters in DC customer side [133]

Primary voltage	**Secondary voltage**	**Switching frequency**	**Auxiliary inductor**	**Filter capacitor**	**Signal modulation**
±0.75kV	±0.19kV	20kHz	0.052mH	5mF	PWM

Figure 3.15 shows the voltage step response of the customer side DAB converter. It is evident that the converter can react effectively when the voltage reference has ±10% step changes and the voltage variations are significantly small (i.e. less than 0.2%). The accurate and fast voltage control performance of DAB converter are within the requirements listed in Section 3.2.2. Thus, the model of DAB converter is validated.

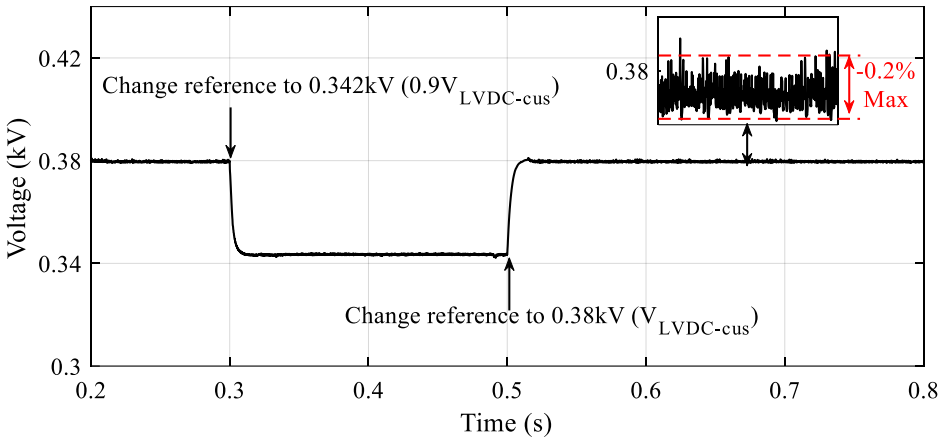

Figure 3.15: Voltage step response of customer side local DAB

3.6 Chapter 3 Summary

This chapter has presented an approach for fault characterisation and protection evaluation for future LVDC distribution networks driven by new converters. The details of the proposed approach have been introduced step-by-step, which facilitates the fault characterisation and protection evaluation of future LVDC distribution networks. The proposed fault characterisation approach helps improve the understanding in the reduction of thermal stress of power electronic components when the new converter is implemented. While the proposed protection evaluation approach improves understanding on the weakness of existing protection solutions and the impacts of using new converters. The more detailed simulation-based studies will be presented in the subsequent chapters.

Following the introduction of the proposed fault characterisation and protection evaluation approach, the rest of the chapter presents the modelling of an LVDC distribution network with different converter interfaces that is used as a test model with the proposed fault characterising and protection evaluation approach. The modelled LVDC network model contains a two-level VSC and an SST as main interface converters and downstream DAB DC/DC converters that can provide fault current limiting and blocking capabilities, which is capable of emulating the LVDC distribution networks with reduced fault levels under short circuit fault conditions. Currently, there are no UK standards to regulate the performance of public LVDC distribution networks. However, the presented converter models have been tested in the case of significant step changes to DC voltage and AC side reactive power, to validate their performance and to ensure that the DC voltage remains within the limits suggested by existing LVDC pilot projects.

Chapter 4

Evaluation of the Impact of SST on DC Fault Characteristics and Protection Effectiveness

4.1 Investigation of the Impact of SST on DC Fault Response

This section investigates and identifies the DC fault response of two-level VSCs and SSTs. Existing DC fault characterisations have been summarised in literature [111–113]. However, these DC fault characterisations have not considered fault current management capabilities (i.e. fault current limiting and blocking) of converters, which are not feasible to understand the fault characteristics of SSTs. Thus, it is necessary to accurately identify the impacts of SST on DC fault characteristics and the effectiveness and limitations of existing protection solutions to facilitate the design of more robust and effective protection solutions. Key factors such as current magnitude, current derivative (i.e., rate change of current), voltage magnitude, voltage derivative (i.e., rate change of voltage), and fault let-through energy are analysed. Also, the discussions on these parameters are followed with simulation results that are conducted in the LVDC test network presented in Chapter 3.

4.2 Fault Response Verification of an LVDC distribution network with a Two-level VSC

It is necessary to verify the fault response of the modelled LVDC test network interfaced with a two-level VSC to ensure the model is working properly during DC fault transient period. This verification is based on the methodology that has introduced in Chapter 3. The main parameters of a fault characterisation study include voltage and current magnitudes, voltage and current derivatives, and fault let-through energy. Under DC pole-to-pole faults, DC fault current can be defined by three stages, the fault current path for each stage is shown in Figure 4.1 [134],

- **Stage I**: capacitor discharge. Smoothing capacitor (i.e. *2C* shown in Figure 4.1) of two-level VSC will discharge and supply a high transient current in the fault path shown with the red dashed line in Figure 4.1.
- **Stage II**: diode free-wheeling. This is the most dangerous stage for converters [120]. After the capacitor is completely discharged, the antiparallel diodes will be forward biased with the green line shown in Figure 4.1. The current through the diode is commutated from Stage I, and diodes experience the highest overcurrent of the three stages.
- **Stage III**: grid supply fault contribution. After diodes commutate the Stage I fault current, grid supply starts to contribute fault current though converter diodes that follow the blue path shown in Figure 4.1 [50].

Stage I: capacitor discharge

When pole-to-pole short circuit fault happens, a resistance-inductance-capacitance (RLC) circuit is established which is excited by the energy initially stored in the capacitor and inductor. Depending on the parameters of the faulted path, the capacitor discharge of a two-level VSC can be defined as overdamped, critical damped, and underdamped [135]. Table 4.1 lists a summary of the mathematical models for the overdamped and underdamped fault conditions based on literature [135–137].

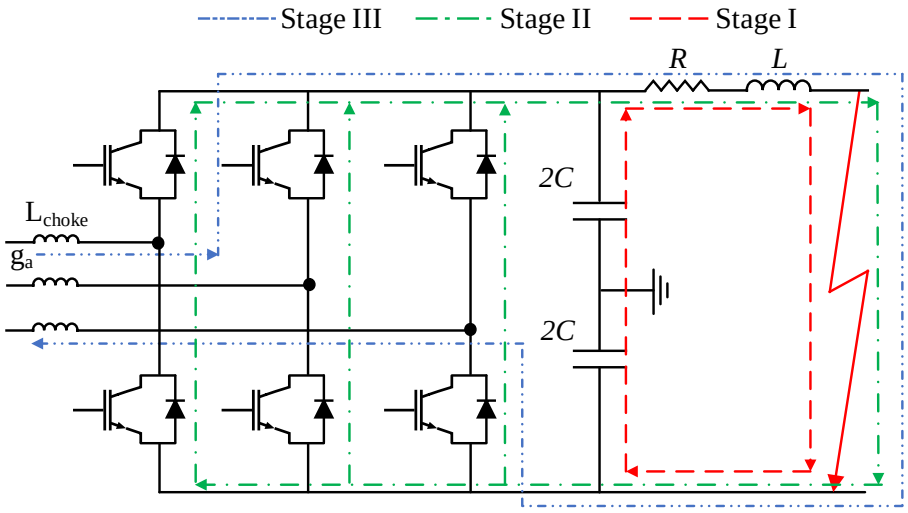

Figure 4.1: Fault current path of a simplified two-level voltage source converter

Table 4.1: Summary of the overdamped and underdamped response in the capacitor discharge [135–137]

	Overdamped	**Underdamped**
Current	$\frac{V_0}{L\cdot(s_1-s_2)}\cdot(e^{s_1t}-e^{s_2t})$ $+\frac{I_0}{s_1-s_2}\left[(s_1+\frac{R}{L})\cdot e^{s_2t}-(s_2+\frac{R}{L})\cdot e^{s_1t}\right]$	$\frac{V_0}{L\cdot\omega_d}\cdot e^{-\alpha t}\cdot\sin(\omega_d\cdot t)$ $+I_0\cdot e^{-\alpha t}[\cos(\omega_d\cdot t)-\frac{\alpha}{\omega_d}\sin(\omega_d\cdot t)]$
Current derivative	$\frac{V_0}{L\cdot(s_1-s_2)}\cdot(s_1\cdot e^{s_1t}-s_2\cdot e^{s_2t})$	$\frac{V_0\cdot e^{-\alpha\cdot t}}{L}\cdot[\cos(\omega_d\cdot t)-\frac{\alpha}{\omega_d}\cdot\sin(\omega_d\cdot t)]$
Time to max current	$\frac{\ln(s_2/s_1)}{s_1-s_2}$	$\frac{1}{\omega_d}\cdot\arctan(\frac{\omega_d}{\alpha})$
Voltage	$\frac{V_0}{L\cdot C\cdot(s_1-s_2)}\cdot(\frac{e^{s_2t}}{s_2}-\frac{e^{s_1t}}{s_1})$	$V_0\cdot e^{-\alpha\cdot t}\cdot\cos(\omega_d\cdot t)+\frac{V_0\cdot\alpha}{\omega_d}\cdot e^{-\alpha\cdot t}\cdot\sin(\omega_d\cdot t)$
Voltage derivative	$\frac{V_0}{L\cdot C\cdot(s_1-s_2)}\cdot(e^{s_2t}-e^{s_1t})$	$-V_0\cdot e^{-\alpha\cdot t}\cdot\omega_d\cdot\sin(\omega_d\cdot t)-\frac{V_0}{\omega_d}\cdot\alpha^2\cdot e^{-\alpha\cdot t}\cdot\sin(\omega_d\cdot t)$
where, R, L, C are the resistor, inductor, and capacitor within the fault path. V_0 is the initial voltage across the capacitor and I_0 is the initial current flow through the inductor, $s_1\,\&\,s_2=-\alpha\pm\sqrt{\alpha^2-\omega_0{}^2}$, $\alpha=\frac{R}{2L}$, $\omega_0=\frac{1}{\sqrt{LC}}$, and $\omega_d=\sqrt{\omega_0^2-\alpha^2}$		

Stage II: diodes freewheeling

After the voltage of the capacitor drops to 0, the inductance within the fault path starts to drive the fault current. The converter diodes are directly conducting to commutate the fault current from capacitor discharge. This significantly high commutating current can damage the diodes of converters by thermal effect, which makes this stage the most dangerous for two-level VSC [135]. In this stage, the short circuit loop is an RL circuit, and the initial current (I_0') is the current value when the capacitor voltage drops to 0. The mathematical model for Stage II fault current in the cable is shown in (4.1) [135]. Where, I_0' is the initial current (right after Stage I), R and L are the resistance and inductance of the fault loop as shown in Figure 4.1.

$$I_{StageII}(t) = I_0' \cdot e^{-(R/L)\cdot t} \tag{4.1}$$

Stage III: grid contribution

After the diodes, freewheeling, the grid starts to feed fault current. With the two-level VSC, in Stage III, a DC short circuit fault can be regarded as a three-phase AC fault, and the output fault current of the converter is the sum of the currents from phase A, phase B, and phase C that flow through the converter diodes. It can be described in (4.2). Taking phase A as an example, the phase current can be expressed as in (4.3). Where, φ=$arctan[\omega_s \cdot (L_{choke}+L)/R]$, τ=$(L_{choke}+L)/R$, I_{g0} and φ_0 are the initial grid current amplitude and phase angle, L_{choke} is the grid side choke inductance [136].

$$I_{StageIII}(t) = I_{ga} + I_{gb} + I_{gc} \tag{4.2}$$

$$I_{ga}(t) = I_g \cdot sin(\omega_s t + \alpha - \varphi) + [I_{g0} \cdot sin(\alpha - \varphi_0)] \cdot e^{-t/\tau} \tag{4.3}$$

The above mathematical models are used to verify the fault characteristics of the LVDC test network with the theoretical two-level VSC fault behaviour to verify that the model is working as expected during DC fault conditions. The simulation results shown in Figure 4.2 are conducted in the LVDC network model with an example fault (i.e. a 100m distant solid fault) and the simplified circuit diagram (i.e. R=$32.8m\Omega$,

L=0.048mH, C=10mF) similar to that shown in Figure 4.1.

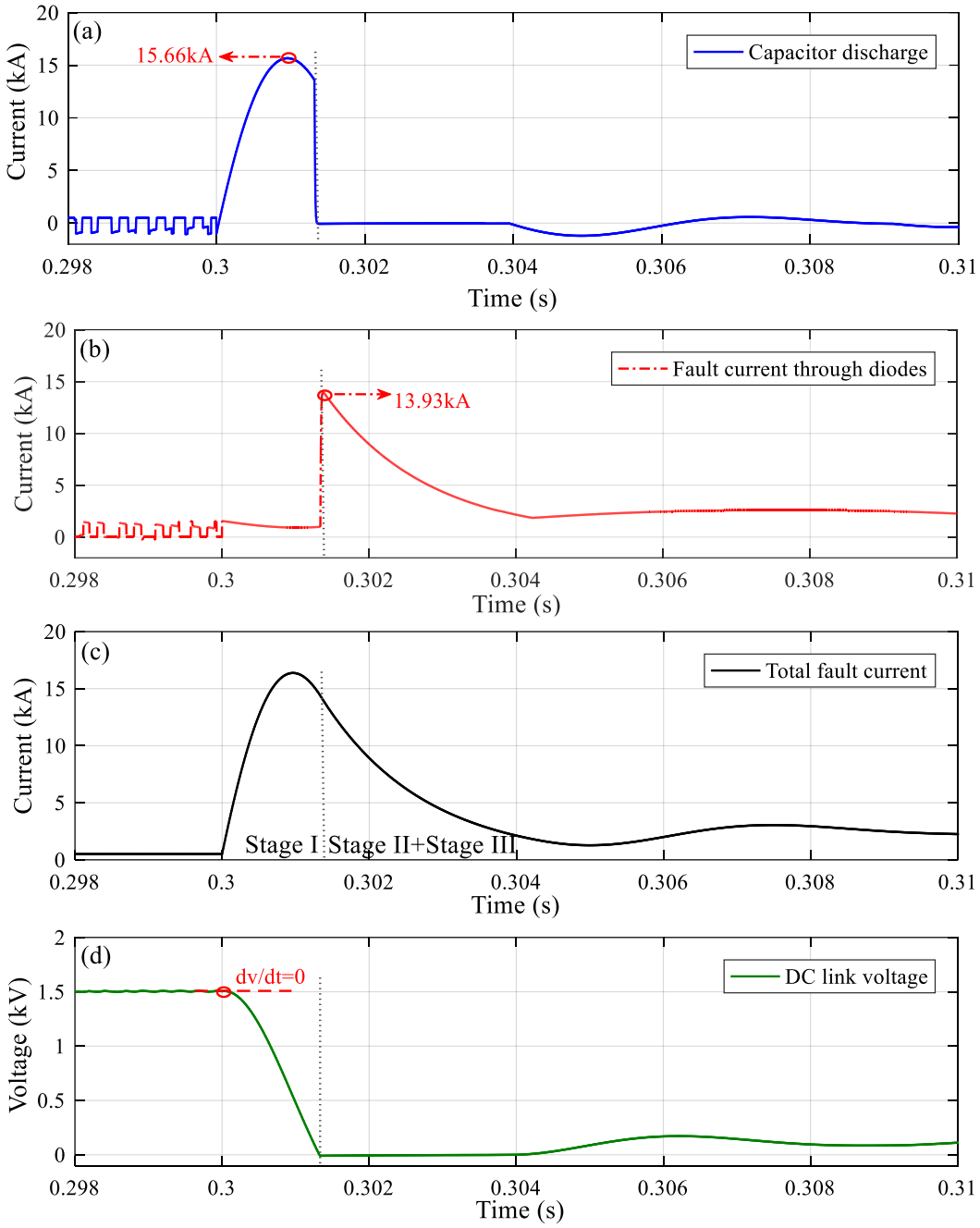

Figure 4.2: Voltage and current profiles of two-level VSC under a DC short circuit, (a) capacitor discharge, (b) fault current through diodes, (c) total fault current, (d) DC-link voltage

The non-constant currents of capacitor and diode during normal operation are caused by the switching of power electronics of converters. In this case, 2kHz is selected as the switching frequency which is a typical value for high power voltage source converters [138]. Lower switching frequency requires a larger filter for effective elimination of switching harmonics and meeting the power quality requirements [138].

In Stage I, when the fault initiates, based on the underdamped equations listed in Table 4.1 with $t=0$, the transient dI/dt is mainly determined by the relationship between initial voltage and inductance within the faulted circuit loop, and it can be calculated by (4.4). The mathematical calculation of current derivative is based on backward finite difference approximation that has been used in LVDC current derivative based protection solutions, which uses the present sampled line current minus the previous sampled line current and divided by the sampling time [139]. In practical, optimization techniques such as properly design filters could potentially increase the quality of this technique to against noise impact [140]. The modelling diagram of this technique is shown in Figure B.2. In this case, the mathematically calculated value is closed to the simulation result as shown in Figure 4.3 with 1.4% error.

$$\frac{dI}{dt} \approx \frac{V_0}{dt} = \frac{1500V}{0.048 \times 10^{-3}H} = 3.125 \times 10^4 (kA/s) \tag{4.4}$$

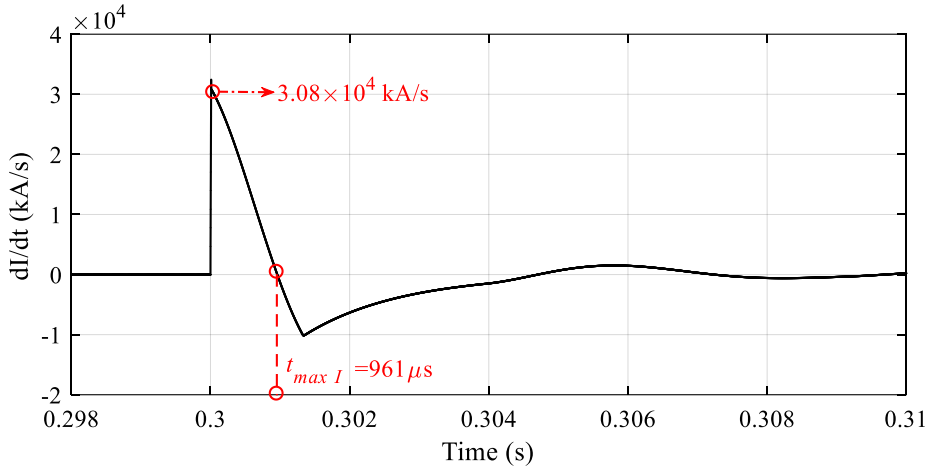

Figure 4.3: Current derivative of a two-level VSC based LVDC under short circuit fault condition

In terms of the maximum fault current, based on the faulted current response shown in Figure 4.2, when the fault current reaches the maximum value, the dI/dt is 0, and the time to reach the maximum fault current can be calculated by the underdamped equations listed in Table 4.1 that is 949μs, which is closed to the simulated value as shown in Figure 4.3 with 1.2% error. Using this time feed into the underdamped current equation listed in Table 4.1, the maximum fault current is calculated as 15.649kA, which is close to the simulated 15.66kA as shown in Figure 4.2 with 0.07% error. Thus, the fault current performance of the model is verified with the mathematical model.

Also, voltage response is verified by simulation results. For example, when the fault initiates, using the underdamped voltage derivative equation listed in Table 4.1 with $t=0$, dV/dt is 0, which is same as the response shown in Figure 4.2 (d). Compared to the rapid current response, voltage changes gradually, and the associated voltage derivatives show a small value at the beginning of the fault as shown in Figure 4.4.

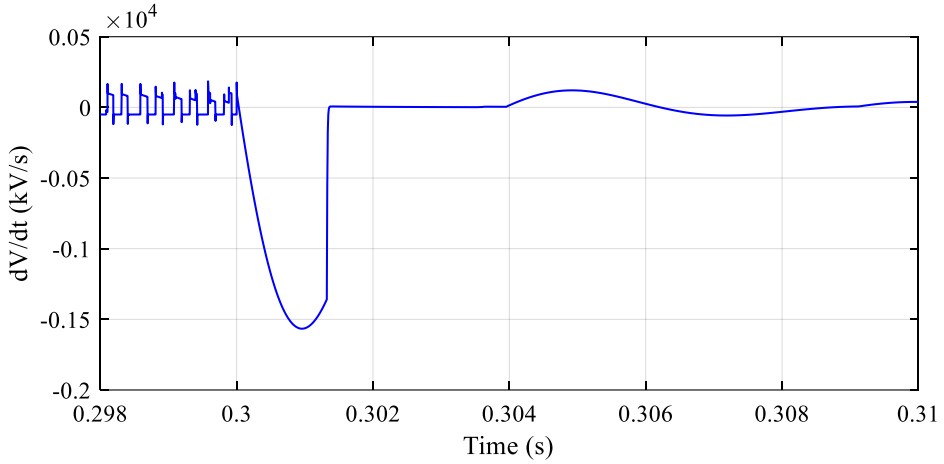

Figure 4.4: Voltage derivative of a two-level VSC based LVDC system under short circuit fault condition

Semiconductors within power converters have much lower fault current withstand capability than other power equipment such as generators, transformers and cables. As discussed before, the inductance within the fault path leads to a surge current through the diodes of converters within fractions of milliseconds to several milliseconds [141]. The transient peak and steady-state fault currents can be beyond the nominal currents. The generated fault energy directly reflects the condition of power electronics during

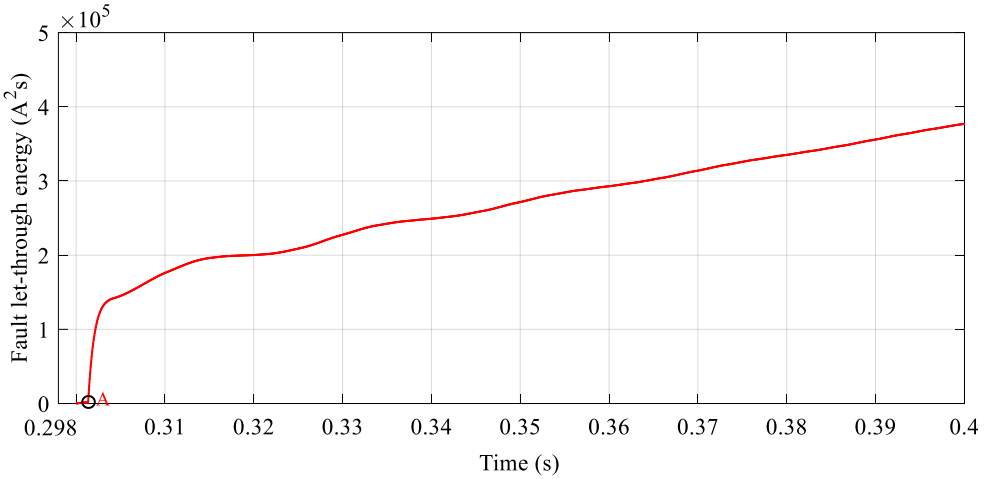

Figure 4.5: An example of FLTE of a two-level VSC under a short circuit fault condition

DC fault conditions. Based on IEC 60747, fault let-through energy (FLTE) is defined as the surge current integral I^2t as (4.5) [141, 142], where *I(t)* is the current flowing through diodes and t is the integration time.

$$\int_0^t I^2(t) \cdot dt \tag{4.5}$$

FLTE also can be used to define the thermal stress of diodes, as exceeding this limit will lead to over-heating of the device [143]. Figure 4.5 shows the FLTE of a two-level VSC under a 100m distant short circuit fault as shown in Figure 4.2. By inspecting the current through diode shown in Figure 4.2, there is very small FLTE generated in the diode before they commutate the capacitor discharge fault current (i.e. before point 'A' in Figure 4.5). After the diode commutates the capacitor discharge fault current (i.e. 1.3ms in this case), the generated FLTE increases dramatically that has potential to damage diodes. This profile of the FLTE of a two-level VSC is used for further comparison with SST to understand its impact on the thermal stress.

Regarding to SST, the active fault current management capabilities offered by SST will reduce the requirements of higher current ratings for the associated assets [144]. However, the challenges with SST-based LVDC systems is the changes in the LV fault current profiles that will influence the performance of existing protection solutions.

Thus, it is necessary to understand the changes of fault behaviours when SSTs are integrated in LVDC systems. The following section of this chapter will identify and quantify the variation of the current, voltage, and FLTE when an SST is implemented in an LVDC distribution network.

4.3 Impact of SST on LVDC Fault Response

Normally, SST consists of AC/DC converters followed by isolated DC/DC DAB converters, and finally DC/AC converters, which provide MVDC, LVDC, and LVAC links, respectively. In LVDC distribution networks, the two-stage SST is considered to provide an LVDC link [145]. The fault characteristic of the LVDC side is in effect the fault response of an isolated DC/DC DAB converter. Thus, in this section, the impact of SST will be conducted based on the fault characterisation of a DAB converter. Figure 4.6 shows the fault current path of a typical DC/DC DAB converter. During the DC pole-to-pole fault transient period (i.e. capacitor discharge), the fault path of an LVDC with a DAB converter is similar to that of a two-level VSC as shown in Figure 4.1, which includes capacitor discharge stage (i.e. Stage I) and diode freewheeling stage (i.e. Stage II) in the secondary side of DAB as shown in Figure 4.6.

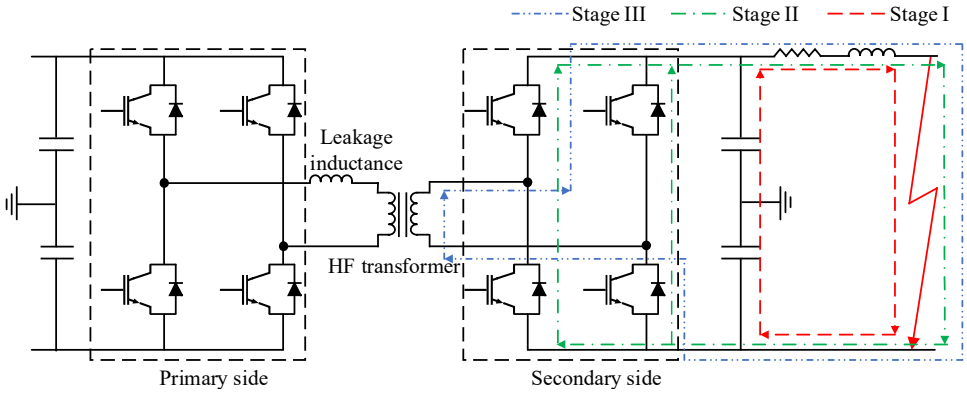

Figure 4.6: Fault path of DC/DC DAB converter

Figure 4.7 shows the relative current and voltage response of an LVDC distribution network with a two-stage SST under an example fault (i.e. a 100m solid DC fault). Compared to the simulation results presented in Figure 4.2 and Figure 4.7, Stage I and

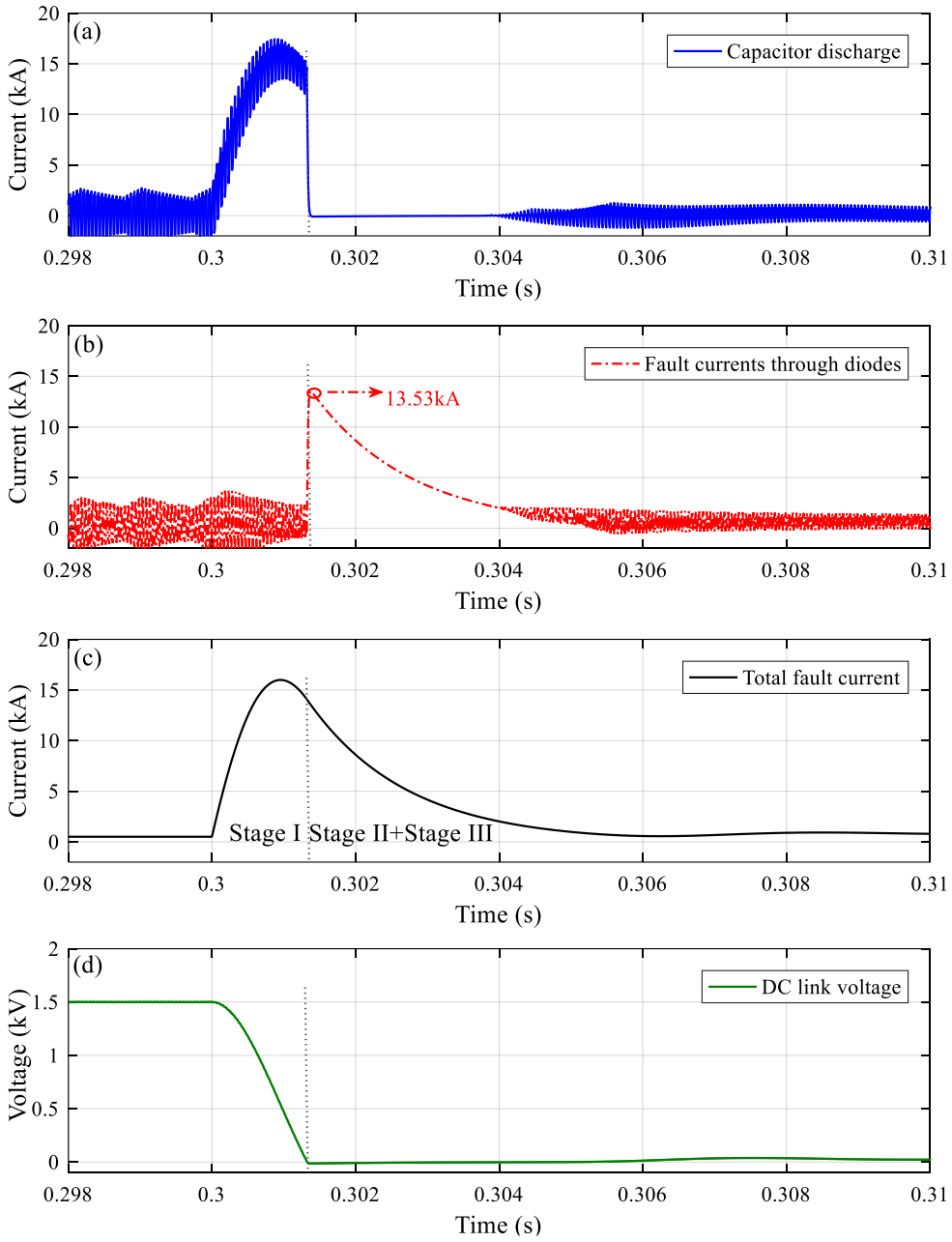

Figure 4.7: Current and voltage profiles of two-stage solid-state transformer under a short circuit fault condition, (a) capacitor discharge, (b) total fault current through diodes, (c) total fault current, (d) DC-link voltage

Stage II from SST and two-level VSC are similar. For example, fault current peak through diode of an SST interfaced LVDC (i.e. 13.53kA) is close to a two-level VSC interfaced LVDC (i.e. 13.93kA). Regarding the steady-state (i.e. Stage III) fault cur-

rent, since a DAB converter has a high-frequency isolation transformer interlink and a fully controllable primary bridge, the fault current feeding to the secondary side is limited [146]. Based on the power transfer relationship described in (3.4), the secondary current ($I_{secondary}$) can be expressed as in (4.6).

$$I_{secondary} = \frac{n_T \cdot V_{MV}}{2 \cdot \pi \cdot f_s \cdot L} \cdot \varphi \cdot (\pi - \varphi) \tag{4.6}$$

The secondary side current is related to the turns ratio of the galvanic isolation transformer (i.e. n_T, 20kV/1.5kV), the voltage of the primary bridge of a DAB (i.e. V_{MV}, 20kV), the switching frequency (i.e. f_s, 20kHz), the auxiliary inductance (i.e. L, 1.875mH) and φ, which is the phase shift between the voltages of the primary bridge and secondary bridge. With the predesigned parameters, the secondary current is directly influenced by the phase shift.

In normal operation, the DAB converter of the SST is controlled by voltage-based phase-shift control as described in Chapter 3. Under fault conditions, as the voltage of the secondary side of the DAB collapses due to the small impedance within the fault path, voltage-based phase shift controller will try to force the DAB to inject more power to the secondary side to maintain the voltage at the normal level. Thus, the steady-state fault current without fault current limiting control will reach the current ratings at the nominal voltage [147]. When fault current limiting and blocking controllers are activated, the fault response is significantly changed.

- **Fault current limiting operation mode:** the controller controls the phase shift between the primary bridge and secondary bridge. With the selected current reference, the DAB converter limits the fault current feeding from the primary side to the secondary side which is less than 50% of the fault current from the two level VSC, and the voltage at the secondary side drops to a very small value due to the small fault resistance in the faulted path as shown in Figure 4.8. Furthermore, the relative FLTE in the diode of DAB is much smaller than the two-level VSC as shown in Figure 4.9 which has 19.2% reduction in 10ms and 41.9% reduction in 100ms.

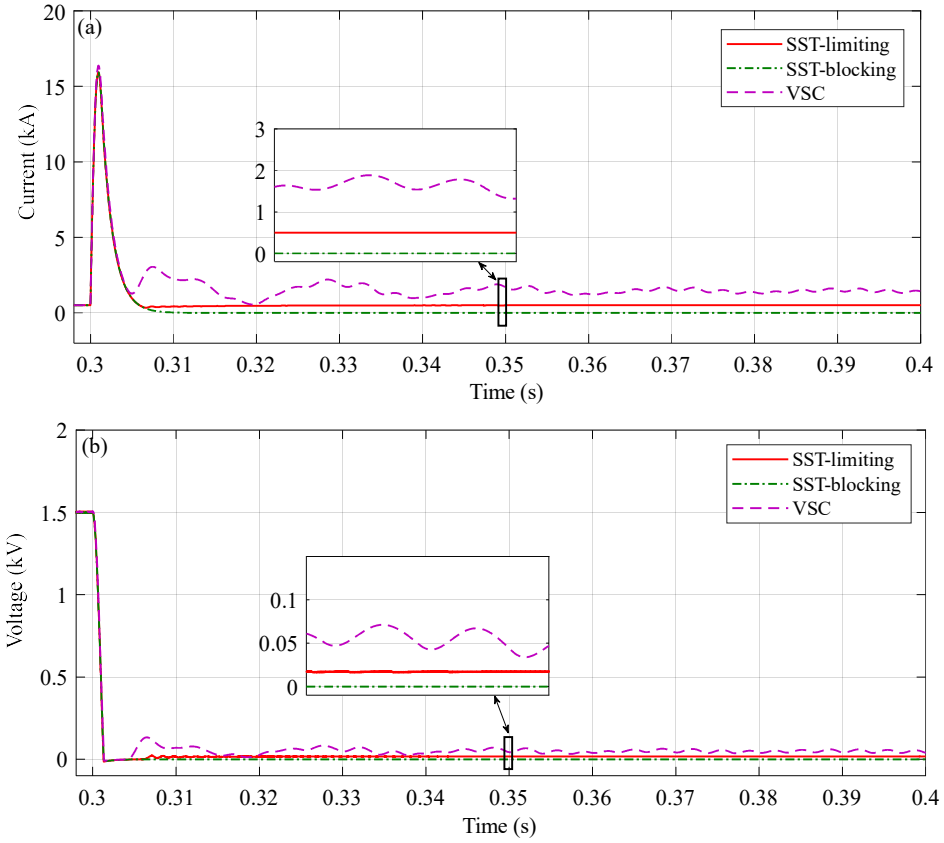

Figure 4.8: Current and voltage comparison between VSC and SST under a DC short circuit condition in simulation study, (a) Current, (b) Voltage

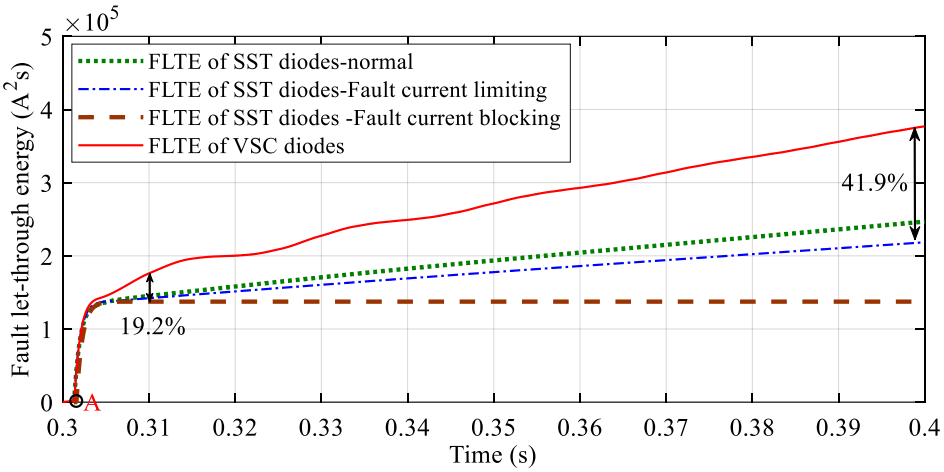

Figure 4.9: Comparison of FLTE through diodes in VSC and the DAB of SST in simulation study

- **Fault blocking operation mode:** the converter stops feeding the fault current and voltage drop to 0 as shown in Figure 4.8. The FLTE generated in diodes is much smaller than the two-level VSC which has 22.5% reduction in 10ms and 63.3% reduction in 100ms.The fault current blocking capability of SST has the potential to eliminate the use of breakers in future SST interfaced LVDC distribution networks. This could reduce the footprint of power substations.

The inherently lower fault currents from the DAB converter of SST provide extra benefits for the design of converters, e.g. lower rating elements can be used to ride through fault conditions. From the above discussion, the SST can eliminate the steady-state DC fault current, but the diodes within the converter still need to withstand the transient fault current that is commutated from capacitor discharge.

There are some more advanced technologies that have been proposed in research work and have the potential to be used in the future LVDC distribution networks to provide stronger fault withstand capability, which can fully eliminate the DC fault current transient period. These are MMCs [148, 149] and fault current limiters (FCL) [150]. In principle, the fault current limiting functionality of MMCs and FCLs is accomplished by introducing additional switches and adjustable impedance in the fault path. When DC faults occur, these elements are activated to limit the fault current. However, to fully realise fault current control and high fault withstand capability of future LVDC distribution networks, not only the main AC/DC interface converters but also the downstream DC/AC and DC/DC converters need to adopt full-bridge based technologies [151] or to be equipped with advanced fault current limiters. To date, the cost of a wider implementation of these technologies is significantly high. Comparatively, SSTs have been proposed and will be trialed in the UK urban area as they can provide more power supply flexibility than conventional 50Hz transformers [63]. The fault response of SST based LVDC distribution networks is more likely to be considered as the main consideration for the design of the near future LVDC protection solutions. Therefore, the following work is focused on using the protection evaluation approach presented in Chapter 3 to evaluate the existing protection performance on an SST interfaced LVDC distribution network.

4.4 Evaluation of Existing Protection Solutions

Most of existing DC protection solutions have been developed for specific applications such as solar photovoltaic (PV) systems [152], electric ships [153], and DC traction systems [154]. However, their suitability for providing a good level of selectivity, reliability, and sensitivity for LVDC distribution networks is still not fully understood especially when SSTs are integrated. Therefore, this section conducts a software-based evaluation of a number of typical DC protection methods that have been used in existing LVDC trials and proposed in the literature, which mainly focuses on current based protection solutions in this chapter, such as the inverse-time based overcurrent protection, current derivative based protection, differential and directional protection. Considerations of voltage based protection solutions will be discussed in Chapter 5. Each protection solution is evaluated in the LVDC test network interfaced by a two-level VSC and a two-stage SST that has presented in Chapter 3 with the following criteria:

- **Protection speed:** time used for fault detection, location, and interruption. The fault interruption process is really dependent on the employed breaker topologies and the materials used in the breakers [155]. As this section mainly determines the speed of fault detection and discrimination, the fault interruption is simplified with a fixed time delay (i.e. representing a typical time delay 0.5ms for a solid-state circuit breaker [153], which has been reported by ABB [107]).

- **Fault discrimination and coordination capabilities:** capability of distinguishing faults that are located within or outwith the protected region, and coordinating relays to select the most suitable relay to trip its associated breaker to clear the faults. This selective tripping is also called discrimination [156].

- **High resistive fault impact:** most of existing LVDC protection solutions only consider short circuit fault as their main protection target. However, high-resistive fault protection capability of protection solutions is also important for the security of future LVDC distribution networks.

- **Communication delay and measurement error effects:** communication delay is mainly used to determine its impact on high-speed differential protection and directional based protection solutions. The measurement errors are mainly used to determine its impact on current derivative based protection solutions.

This evaluation is conducted in the test network as shown in Figure 4.10, which is based on the network presented in Chapter 3 and integrated with protection units (i.e. relays and breakers) that are named as a_1-a_2, b_1-b_2, c_1-c_2, and d_1-d_2. The breaker is considered as an ideal switch with a 0.5ms time delay that is based on a practical solid state circuit breaker [107].

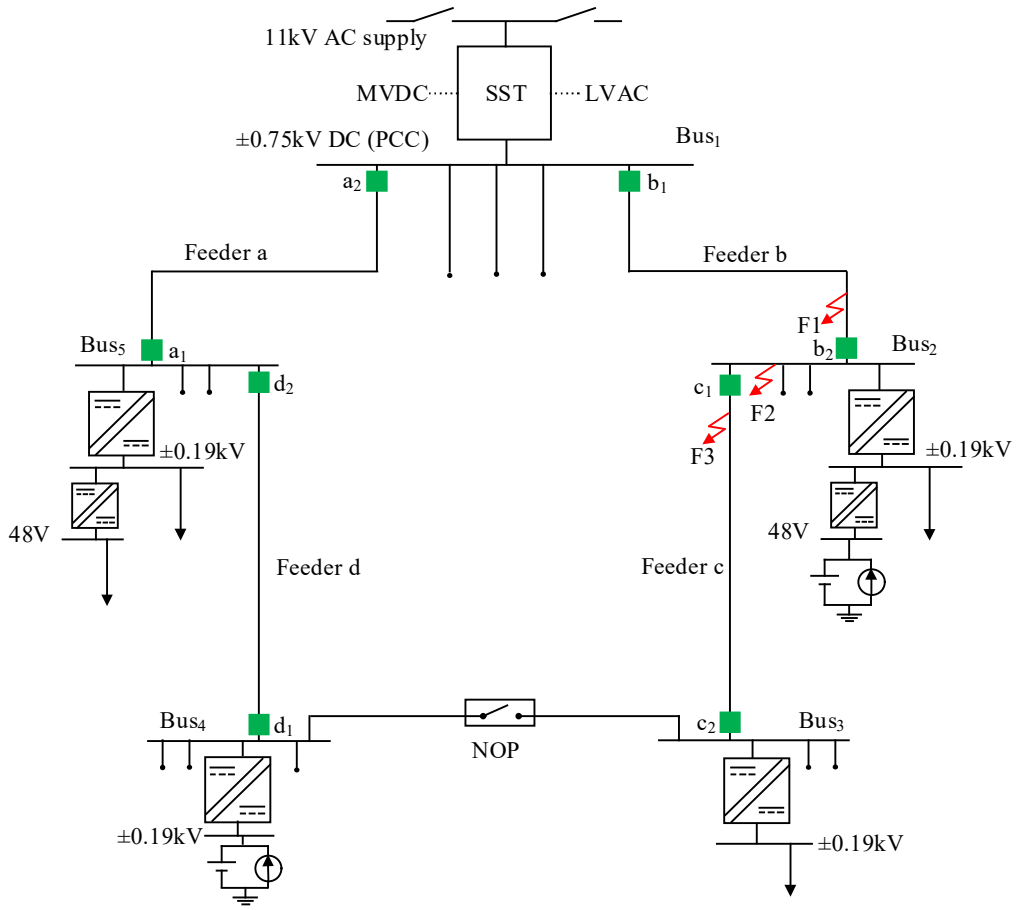

Figure 4.10: An SST interfaced LVDC distribution network model used for protection evaluation

In this test network, DC customers are interfaced by DAB converters with galvanic isolation. The leakage inductance within DAB converters can eliminate the impact of load changes on protection security. Also, the evaluation of the impact of other transients on protection security will be included in future work with simulation studies and experimental tests. This evaluation is based on the methodology that has been presented in Chapter 3. The test network is protected with alternative protection solutions that are commonly used in existing DC applications and proposed in literature, such as overcurrent protection, differential protection, directional protection, and current derivative based protection solution. Performance of protection devices b_1, b_2, and c_1 are mainly selected to evaluate the effectiveness of the selected protection solutions. In the test network, faults in location F1, F2, and F3 are mainly considered. Fault F1 is used to evaluate the protection speed of each protection method. Fault F2 is used to evaluate the protection discrimination capability when faults are located in busbars. Fault F3 is an external fault of device b_1. All the faults are applied at 0.3s.

4.4.1 Modelling of Typical DC Protection Solutions

This section introduces the modelling of the selected protection solutions such as overcurrent protection, differential protection, directional protection, and current derivative based protection that are going to be evaluated for protection studies.

Set Up of Inverse-time based Overcurrent Protection Scheme

In [157,158], overcurrent protection is evaluated for protecting LVDC systems. In [157], the protection devices are integrated with IEEE Std. C37. 112 extremely inverse time overcurrent characteristics [159], which has a threshold setting with twice of the full load current. In the test network shown in Figure 4.10, the same overcurrent tripping profile is equipped in the protection devices (devices 'b_1' and 'c_1' are selected as an example). In order to provide fast protection, the extremely inverse standard characteristic is selected, and the pickup current for the test network is set to 1.2 times of the full load current in each feeder. In this case, the thresholds for device 'b_1' and 'c_1' are *320A* and *160A* since the full load currents of Feeder b and Feeder c are *266.6A* and *133.3A*. The entire model of the tripping logic of device 'b_1' is built as depicted in Figure 4.11.

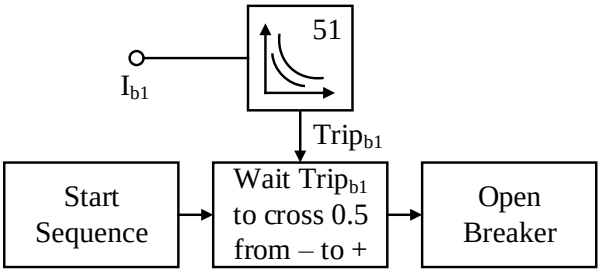

Figure 4.11: Model of overcurrent protection in PSCAD/EMTDC [157]

Set Up of Differential and Directional based Protection

Differential protection and directional protection solutions have been widely implemented in AC systems and have been investigated to be used in LVDC systems [152]. As discussed in [86], DC differential protection only requires the current difference between the current measurements. The differential current calculation is based on using the center processing unit with communication links. The measured currents from each side of the protected boundary are summed up and passed to a relay and compared against a trip threshold. Based on this comparison, a protection decision (i.e. trip or non-trip) is sent to the associated breakers. In terms of the threshold setting of differential protection, 20% of full load current has been used as an example for protecting DC microgrids [160]. This threshold is applied for the differential protection set up in the LVDC test network. For device 'b_1' and 'b_2', the threshold is *64A* since the full load current for Feeder b is *320A*. The model of differential protection in PSCAD/EMTDC is shown as Figure 4.12.

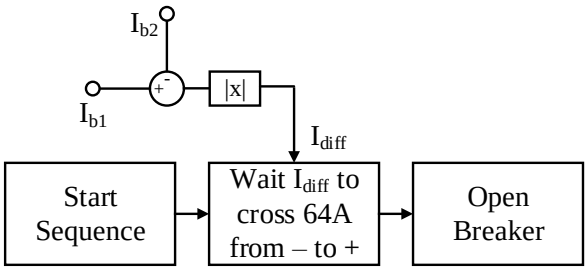

Figure 4.12: Model of differential protection in PSCAD/EMTDC [160]

Compared to DC differential protection, DC directional based protection directly compares the direction information of relays through communication. The setting for directional based protection is more straightforward than DC differential protection. For implementing this protection scheme, all the protection devices are equipped with communication links to realise the comparison of the local fault current direction with the remote end's current direction. The model of directional protection in PSCAD/EMTDC is shown in Figure 4.13. Where, using the multiplier to identify the direction difference between device 'b_1' and device 'b_2'. If the current direction is the same as the current direction measured at the end of the protection zone, the fault is an external fault and no trip signal is generated for this zone. Otherwise, the fault is an internal fault and trip signals are sent to the associated breakers to isolate the faulted zone [117]. This algorithm is also suitable for bus protection when a bus is regarded as a protection zone. For this communication-based DC directional protection, no threshold is required, only the current direction is used for fault detection and location.

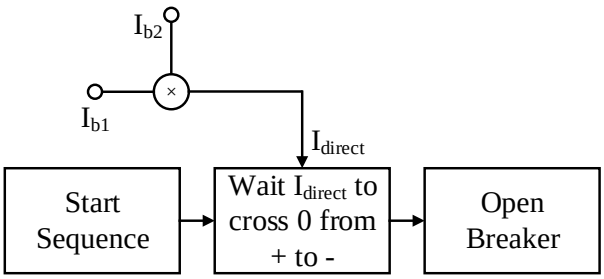

Figure 4.13: Model of directional protection in PSCAD/EMTDC [117]

Set Up of Current Derivative-based Protection

Current derivative-based protection has been proposed for protecting DC microgrids that relies only on local measurements without using communication links [75]. The threshold setting is based on the fault distance from the fault location to the protection device. As discussed in section 4.1.1 and based on the mathematical expressions listed in Table 4.1, when a fault happens, the current derivative is equal to the voltage of the converter capacitor divided by the inductance within the fault path, while neglecting the pre-fault current contribution (i.e. due to the relatively small value of the prod-

uct of initial current and line impedance, the current derivative is dominated by the voltage divided with the inductance within the fault path). This means the protection discrimination can be achieved by setting the threshold based on different inductances of different protection zones as shown in (4.7), where V_0 is the initial voltage on the capacitor, dI/dt is the current derivative measured at the converter capacitor terminal, and L is the inductance within the fault path.

$$L = \frac{V_0}{\frac{dI}{dt}} \tag{4.7}$$

In the LVDC network shown in Figure 4.10, the distance between each downstream converter is 250m (i.e. L=0.12mH) as presented in Chapter 3. Based on (4.7), the threshold for the protection device is $1.25\times10^4 kA/s$ with 1.5kV initial voltage for the converter capacitor. If the transient current derivative is higher than this threshold, the fault is detected and located within the protected zone, and the trip signal is sent to the associated breaker. Otherwise, the fault is located outside the protected zone. The model of current derivative based protection in PSCAD/EMTDC is shown in Figure 4.14. In this model, $\Delta I/\Delta t$ is used to represent dI/dt, where function e^{-sT} is used to capture the previous measurement. The sampling time of the simulation is selected as 1MHz [161], the threshold (i.e. $1.25\times10^4 kA/s$) is divided by the sampling frequency to obtain the corresponding setting (i.e. $0.0125kA$) used in the PSCAD model.

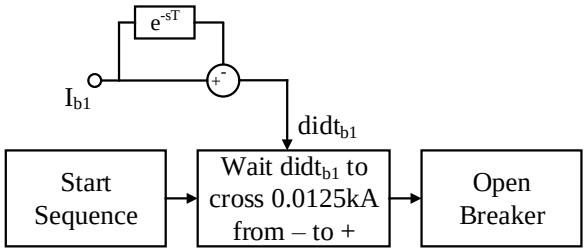

Figure 4.14: Model of current derivative based protection in PSCAD/EMTDC

4.4.2 Performance of the Modelled Protection Solutions

In this section, refer to the protection criteria mentioned before, such as protection speed, fault discrimination and coordination capabilities, high resistive fault impact, and communication delay and measurement error effects. The following part will discuss the performance of the modelled protection solutions related to each protection criteria.

Protection Speed

To evaluate protection speed, a solid fault F1 is selected. Each selected protection method is protecting the LVDC distribution network aginast this fault in this evaluation criteria. Figure 4.15 and Figure 4.16 show the voltage and current response of a two-level VSC interfaced LVDC test network protected by overcurrent, differential, directional, and current derivative based protection solutions.

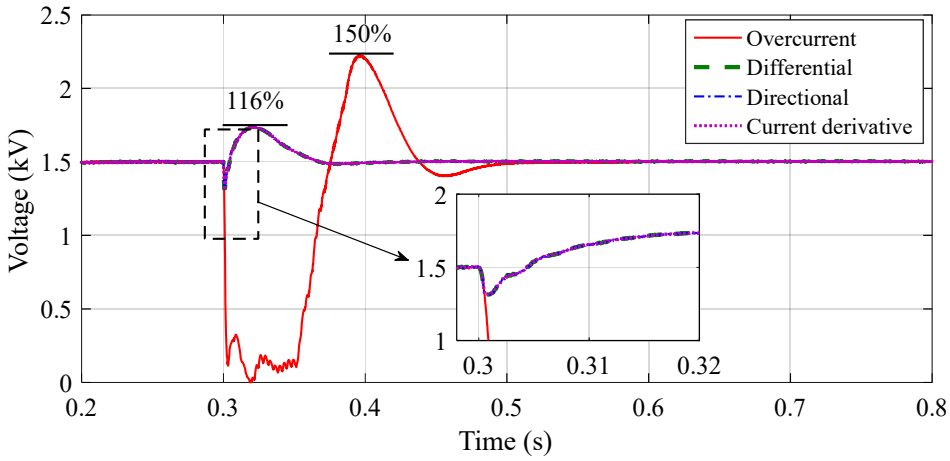

Figure 4.15: Voltage response following tripping by different protection methods under F1 fault condition when two-level VSC is used

In the two-level VSC interfaced LVDC test network, inverse-time overcurrent protection has the slowest protection speed (i.e. 52.5ms). Due to its slow performance, the two-level VSC experiences a significantly high fault current and a dramatic voltage drop (i.e. almost to 0). Also, as a result of this long-time fault clearance, after the fault is cleared, voltage shows 150% overshoot and the two-level VSC converter takes 200ms to recover. In this case, converter diodes would need to have a high thermal rating to withstand fault currents.

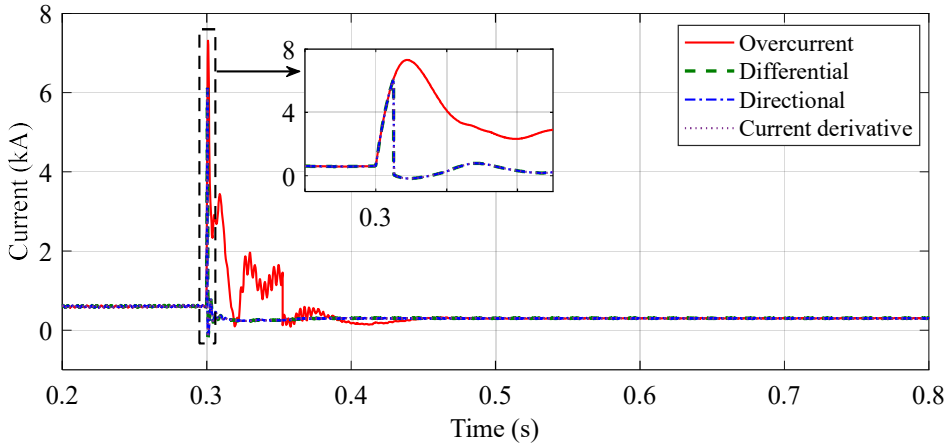

Figure 4.16: Current response following tripping by different protection methods under F1 fault condition when two-level VSC is used

The speed of overcurrent protection is get slower when the LVDC test network is interfaced with an SST. Due to its limited fault current, steady-state fault current of SST is only about 50% of the fault current generated by a two-level VSC as shown in Figure 4.17. However, the reduced fault current slows down inverse-time based overcurrent protection. It can be seen that F1 fault is cleared in 206ms, which is almost 4 times longer than the time it takes for the two-level VSC interfaced LVDC test network. This slow protection speed is caused by the limited fault currents generated by power electronic converters.

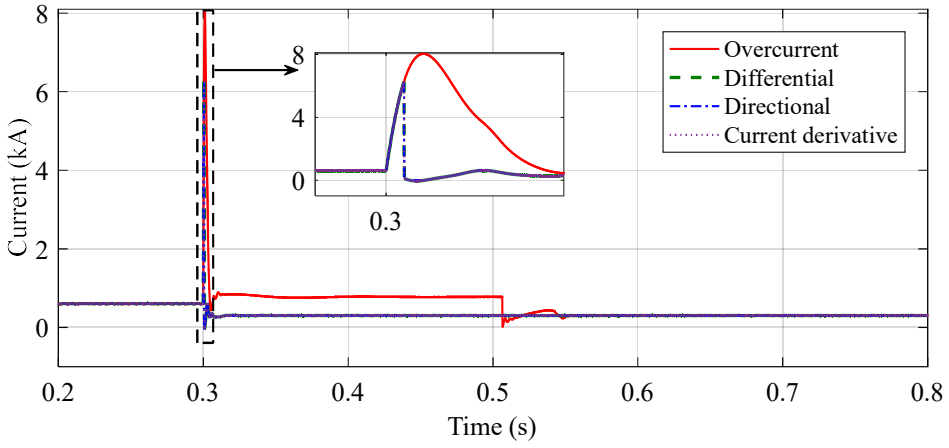

Figure 4.17: Current response of different protection methods under F1 fault condition when SST is connected

Conventional inverse-time overcurrent protection is designed for AC systems that are interlinked with conventional low-frequency transformers. Compared to power converters, transformers can survive a much higher fault level that allows the downstream protection devices to be coordinated by inverse-time characteristics with an acceptable protection speed [67]. However, in LVDC systems, due to fragile power electronic converters, only 1-2p.u. fault current is acceptable [162] within a constrained time window (e.g. 2ms). This level of fault current or the even smaller fault current can significantly delay the operation speed of overcurrent protection. Thus, if conventional overcurrent protection is implemented in future SST interfaced LVDC distribution networks, the downstream protection using overcurrent protection will be adversely affected, which has potential to create further impact on the overall power quality of LVDC systems.

Compared to the slow protection speed of conventional inverse-time overcurrent protection, more advanced current derivative based protection and communication link based differential and directional protection solutions demonstrate much faster protection speed (i.e. Fault F1 can be cleared in 0.5ms). This fast fault clearance isolates the F1 fault at the beginning of the capacitor discharge stage of the F1 fault, and no freewheeling and steady-state fault currents flow through converter diodes. Also, the reduction in total fault period leads to lower system voltage drop (i.e. 12.6% of nominal voltage), and faster post-fault recovery (i.e. 75ms) as shown in Figure 4.15. In addition, as these fast protection methods only rely on the very early stage of the capacitor discharge current, the limited fault current of SST has an insignificant impact on the protection speed of these fast protection methods. Hence, these methods will benefit the design of converters, permitting the lower thermal rating devices to be used. Also, the faster power recovery of advanced protection solutions leads to higher power quality than the overcurrent protection implemented LVDC systems. After protection speed, fault discrimination and protection coordination capability is considered.

Fault Discrimination and Protection Coordination Capability

To evaluate fault discrimination and protection coordination capability, fault F2 and F3 are implemented that are external faults of device 'b_1'. While, identify whether there are mal-operations of device 'b_1'. With the typical setting of overcurrent protection,

slow protection speed is achieved, and converter diodes have to withstand the freewheeling and high steady-state fault current. To protect the power electronic devices, converter protection should operate before diode freewheeling stage (i.e. normally less than 2ms). To achieve this high speed, the time dial setting of overcurrent protection is revised from a typical value of 0.05 to 0.01. In this way, Fault F3 can be cleared in 2ms that is during capacitor discharge stage as shown in Figure 4.18.

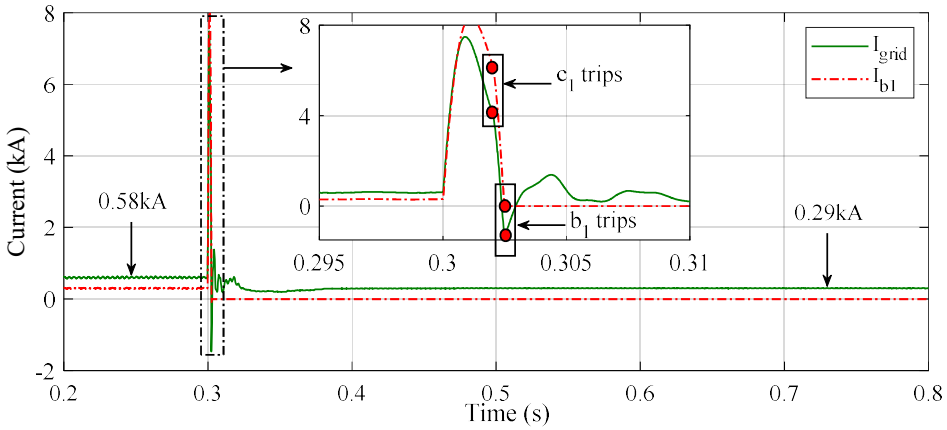

Figure 4.18: Currents of a two-level VSC interfaced LVDC distribution network with overcurrent protection with time dial setting 0.01 under F1 fault condition

However, this high-speed setting required for protecting power electronic devices bring challenges for protection coordination. After device 'c_1' trips, device 'b_1' trips as well as shown in Figure 4.18. Hence, mal-operation of overcurrent protection implemented in device 'b_1' happens, and the LVDC distribution networks only feed half of the system (i.e. current from *0.58kA* to *0.29kA* as shown in Figure 4.18). The reason for this mal-operation is because the reduced operation time for each protection zone reduces the coordination margin. Another potential reason that may cause mal-operation is the operation speed of the circuit breaker. Since inverse-time current protection is based on time grading, trip signals are possible to be generated by upstream relays when the downstream relay already sends a trip signal to the downstream breaker (i.e. during breaker operation time period). This is because, during this period, current will continue to flow through upstream devices and make upstream devices operate.

When SST is integrated in the LVDC test network, the same situation is experienced

when the time dial setting is reduced to 0.01. Due to the reduced fault current of SST that has been discussed in Section 4.1.2, achieving protection coordination within the same time window as for the two-level VSC, will be more difficult. Compared to two-level VSC, SST might have a longer time to withstand fault current, but it complicates protection coordination and has the potential to cause power quality issues.

Compared to inverse-time overcurrent protection, current derivative based protection is another non-unit protection. Its protection coordination is based on fault distance. As illustrated in (4.7), the transient current derivative is only related to the inductance within the fault path. Using this phenomenon to discriminate faults is much faster than using time-grading. For example, Figure 4.19 shows the maximum current derivative with different fault distance in a two-level VSC interfaced LVDC distribution network. The current derivative is reducing when fault distance is increasing, which can provide a good level of fault discrimination.

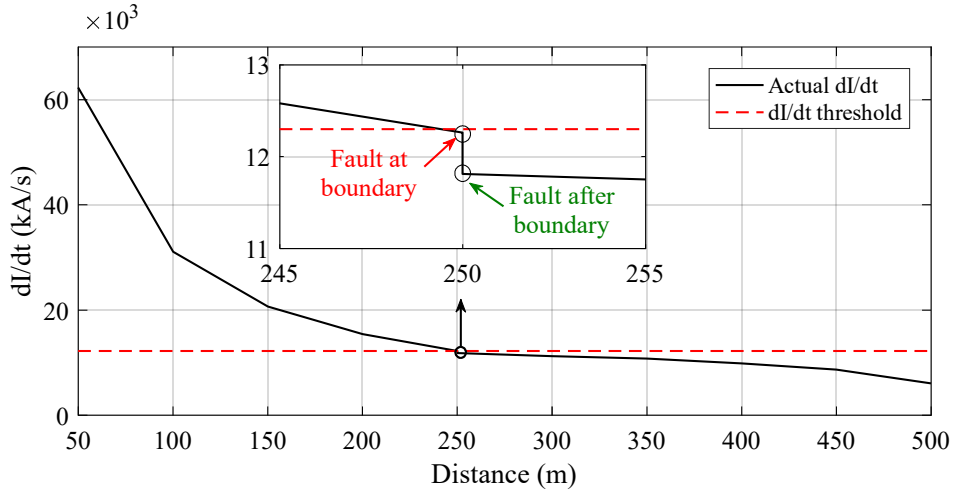

Figure 4.19: Current derivative of 'b_1' with different fault distance in a two-level VSC interfaced LVDC

However, for the fault close to the boundary, it might cause confusions to current derivative based protection methods. As shown in Figure 4.19, for faults (fault F2 and F3 right after the boundary (i.e. after device 'c_1', the neglectable impedance between the fault and boundary), the current derivative is close to the threshold. The same problem may occur for faults located before and after device 'b_2' as there is no

inductance within the protection device 'b$_2$'. Regarding the SST impact, as the limited fault current affects only in the steady-state, the influence of SST can be neglected.

Compared to non-unit protection, unit protection solutions such as differential protection and directional protection are more effective in discriminating DC faults. Using communication links, the comparison between the currents flowing from the upstream and downstream side of the protected zone can be performed, and the faults can be quickly discriminated. For example, Figure 4.20 and Figure 4.21 show the currents measured by device 'b$_1$' and device 'b$_2$' under F1 fault condition.

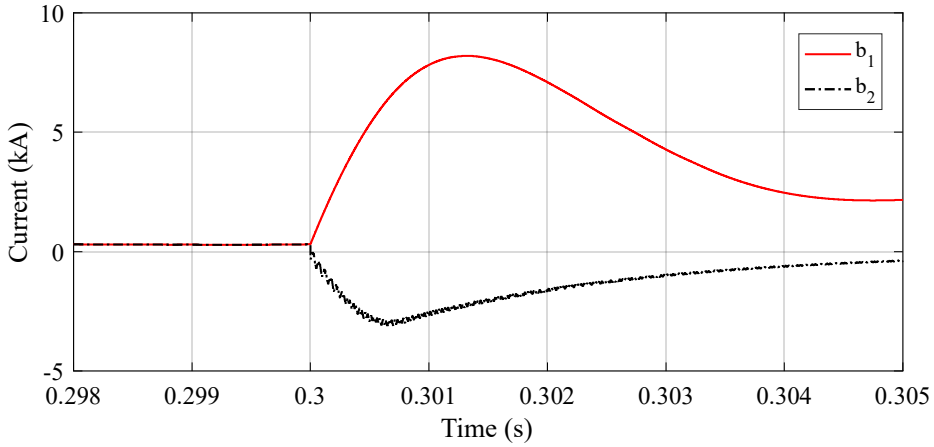

Figure 4.20: Current measured by device 'b$_1$' and device 'b$_2$' under F1 fault conditions in a two-level VSC interfaced LVDC distribution network

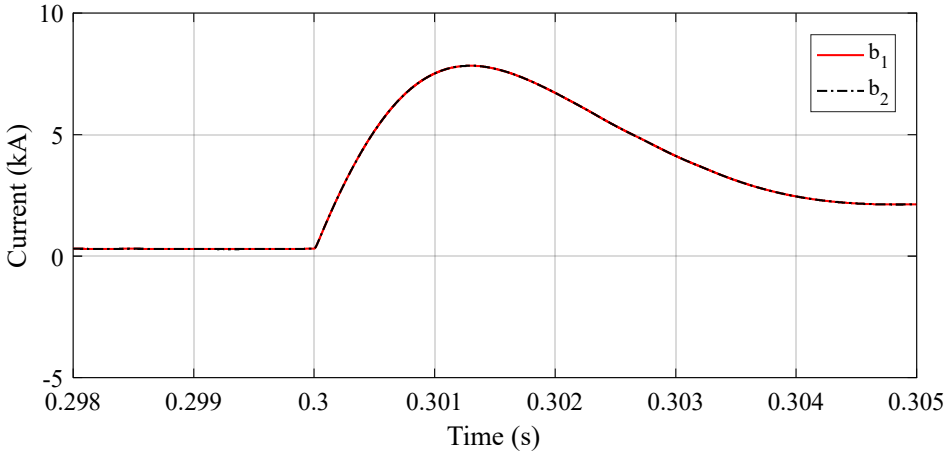

Figure 4.21: Current measured by device 'b$_1$' and device 'b$_2$' under F3 fault conditions in a two-level VSC interfaced LVDC distribution network

When fault F1 happens, fault currents that flow from the upstream and downstream side to the fault point result in significant fault current difference (i.e. I_{b1}-I_{b2}), which exceeds the threshold in 1μs. Comparatively, when the external fault F3 happens, device 'b_1' and device 'b_2' have similar current measurements with a negligible current difference, and the fault is regarded as an external fault. It can be seen that in differential protection based on communication links, fault discrimination of solid faults can be achieved at an ultra-fast speed. Also, directional protection is based on the similar concept that is comparing the current directions between the current in and current out of the protection zone. In contrast to the current differential, it only relies on the current direction measurements. Based on the current measurements shown in Figure 4.20 and Figure 4.21, faults can be quickly distinguished (i.e. 1μs) by using current direction. As both these two methods act during the capacitor discharge stage, the impact of the lower fault current in the case of the SST on the effectiveness of these two methods is neglectable. After evaluating the fault discrimination capability of the selected protection solutions, the impact of fault resistance is considered.

Fault Resistance Impacts

The impact of fault resistance on the performance of existing protection solutions is used to determine their sensitivity. In this section, pole to pole resistive faults are selected to evaluate. The typical value of fault impedance is from solid to 10Ω [92,114,163], where a 1Ω fault has been considered as a high resistance fault and a 10Ω fault is regarded as a very high resistance fault [163]. As inverse-time overcurrent protection is based on current magnitude, the higher the fault resistance, the smaller the fault current magnitude. This directly slows down the protection speed. For example, Figure 4.22 shows the currents measured by device 'b_1' when highly resistive faults occur. It can be seen that the protection speed is dramatically reduced from 2ms to 120ms (with 0.01 time dial setting) when fault resistance increases from solid to 5Ω.

Compared to conventional overcurrent protection, current derivative based protection demonstrates faster and more effective fault discrimination for resistive faults. Figure 4.23 shows the current derivative for resistive faults. It can be seen that the transient current derivatives are almost the same (i.e. red circle in Figure 4.23) as

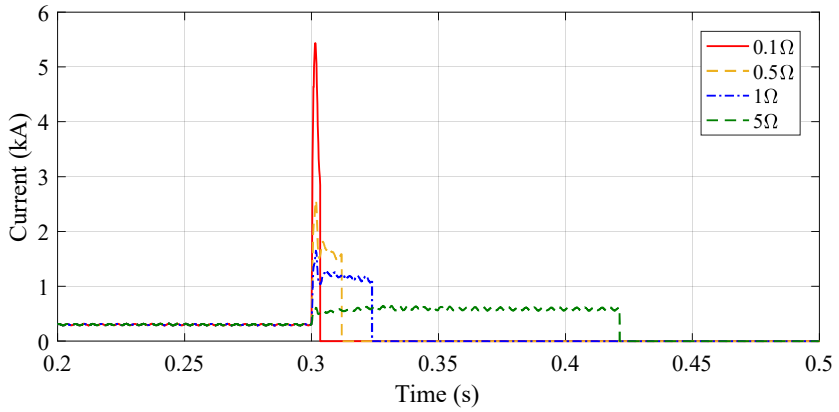

Figure 4.22: Fault currents of a two-level VSC interfaced LVDC distribution network under F1 fault conditions with increased fault resistance

the threshold calculated in Section 4.2.1 when fault resistance changes from 0.1Ω to 5Ω. Thus, if protection measurement is fast enough to capture the first point of fault current as soon as the fault initiates, resistive faults within the range of 0.1Ω-5Ω have a negligible impact on the performance of current derivative based protection methods.

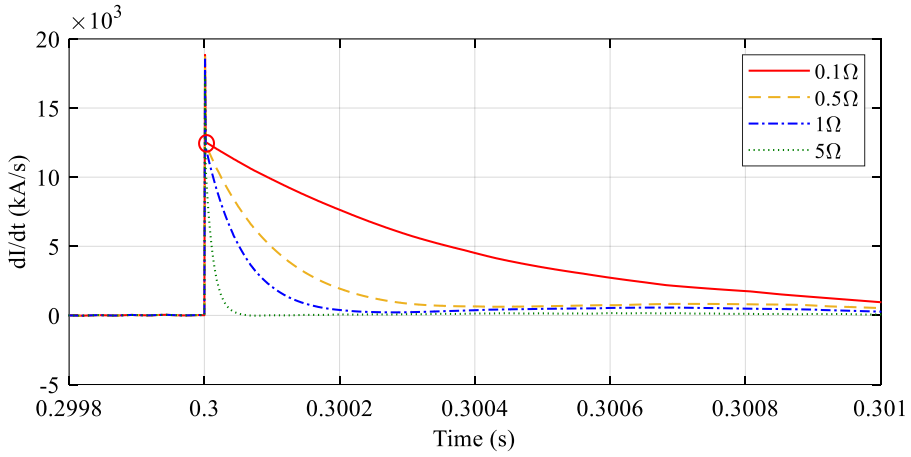

Figure 4.23: Current derivatives (kA/s) of a two-level VSC interfaced LVDC distribution network under F1 fault conditions with increased fault resistance

Communication-based differential protection and directional protection are effective for solid faults. However, when resistive faults happen, their performance is going to be less effective. For example, Figure 4.24 shows the current difference (i.e. I_{b1}-I_{b2}) between device 'b$_1$' and device 'b$_2$' when fault resistance increases from 0.1Ω to 5Ω. It

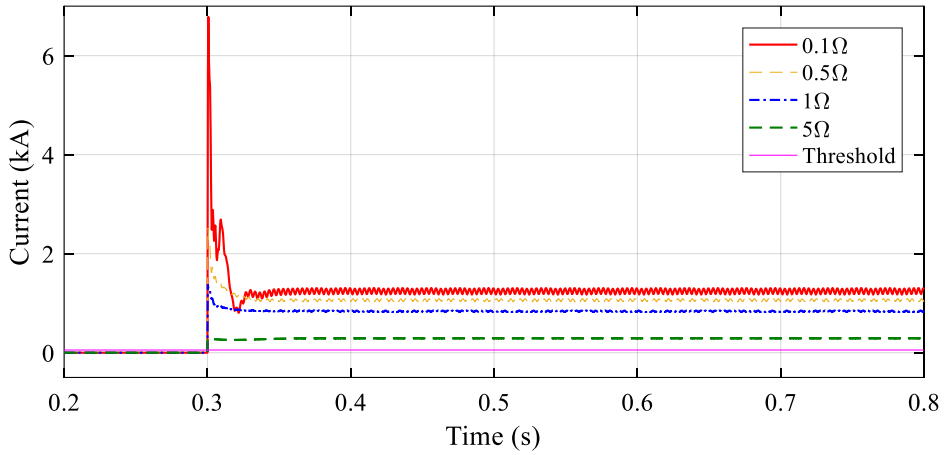

Figure 4.24: Current difference between device 'b_1' and device 'b_2' under F1 fault condition with increased fault resistance

can be seen that the current difference is approaching the set threshold. Although it still can provide fault resistance tolerance up to 5Ω, higher values of fault resistance have the potential to impact the effectiveness of the method.

Compared to the differential protection, directional protection is less effective in protecting high resistive faults. For example, as shown in Figure 4.25, the remote side converter stops to feed the reverse fault current when fault resistance is bigger than 2.5Ω, both devices 'b_1' and 'b_2' have the same fault current direction. This makes directional based protection unable to detect and discriminate highly resistive faults.

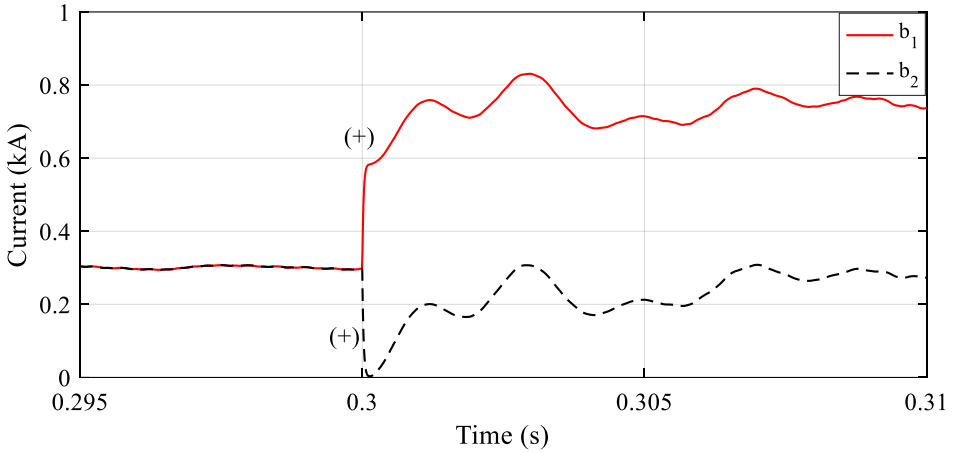

Figure 4.25: Current measurements of device 'b_1' and device 'b_2' under F1 fault conditions with 2.5Ω

Communication Delay and Measurement Error Impacts

Communication links help DC unit protection solutions (e.g. differential and direction protection) to provide high-speed fault detection and fault discrimination. However, communication delays can influence protection coordination of directional and differential protection. For example, Figure 4.26 shows the current measurements with 10μs communication delay in the remote end device 'b_2'. It can be seen that device 'b_2' with 10μs delay initiates the trip signal under F2 fault condition which is an external fault.

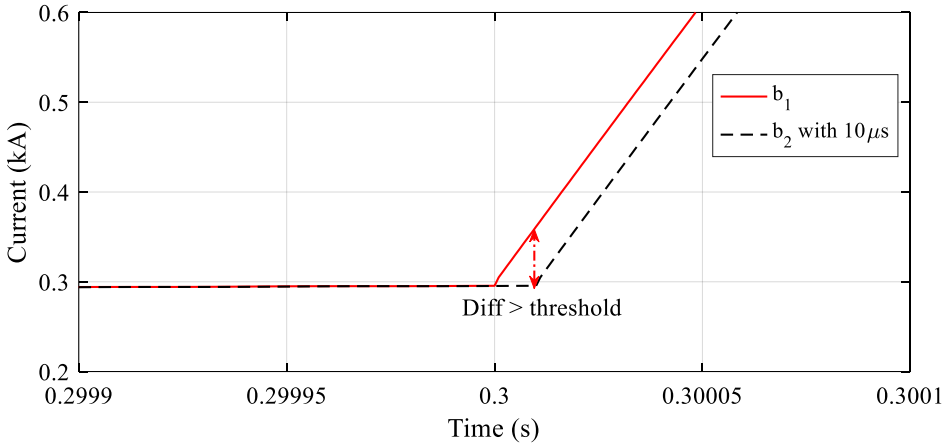

Figure 4.26: Current measurements of 'b_1' and 'b_2' with 10μs time delay under F2 solid fault condition

The same phenomenon is observed in the case of directional-based protection. The delay makes direction comparison among currents unrealistic and mal-operation happens. Moreover, measurement errors, such as transducer noise, can significantly influence the performance of high-speed protection solutions. Transducer noise not only affects communication-based unit protection solutions but also for advanced non-unit protection such as current derivative based. In the presence of noise, using the mathematical relationship to estimate fault distance could lead to significant reliability issues and consequently, to misrepresent current derivative. For example, Figure 4.27 demonstrates the significant impact of noise on the current derivative. Even though the noise magnitude is only ±0.3% of the original current signal (captured from an LVDC testbed [84]), the calculated current derivative significantly deviates from the actual current derivative signal (e.g. ±85% as shown in Figure 4.27).

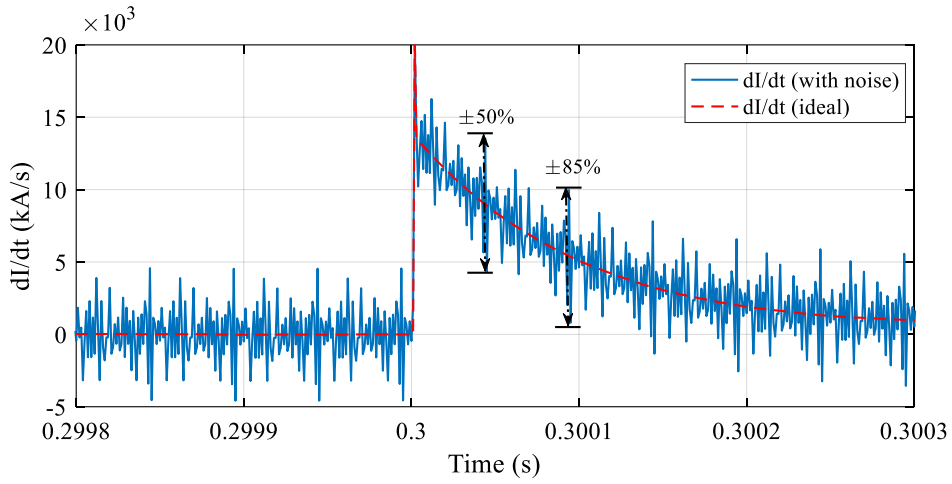

Figure 4.27: Noise impacts on the current derivative of device 'b_1' under F1 solid fault condition

This section has evaluated the effectiveness of typical LVDC protection solutions for a two level and an SST interfaced LVDC distribution networks. The simulation results offered a comprehensive understanding that helps to provide recommendations for designing more effective LVDC protection solutions, which are summarised in the following section.

4.4.3 Recommendations for Future LVDC Protection Solutions

Based on the above protection evaluation, there are some recommendations that need to be considered for future LVDC protection solutions design:

- Fast speed and efficient fault discrimination. Fast speed is still required for two-level and SST interfaced LVDC distribution networks. These two types of converters still have capacitor discharge stage of DC faults and their diodes will experience significant fault current. This phenomenon highlights the challenge of conventional overcurrent protection to achieve coordination between relays (i.e. fault discrimination) within such a short time period (i.e. 2ms). Also, the speed requirement of using overcurrent protection is less likely to be achieved when fault-tolerant converters such as SST are employed due to their limited fault current. Consequently, conventional overcurrent protection has to be improved with

dependencies (e.g. combined with voltage) in order to rely less on the current magnitude;

- Future protection solutions need to be effectively coordinated with the fault management capabilities (i.e. fault current limiting and blocking) of converters. SST is one kind of fault-tolerant converters that can limit steady-state fault current. More advanced converters such as modular multilevel converter (MMC) have more enhanced fault current limiting capabilities that not only limit the steady-state fault current but also limit the capacitor discharge current. This will make current based protection less effective if these fault management capabilities are activated before the required time window needed for fault protection schemes. In these situations, voltage-based protection and other combination-based protection solutions need to be developed. This will be the focus of Chapter 5;

- Implementing protection solutions that only rely on local measurements requires exact protection boundary to be defined. For example, for conventional overcurrent protection and advanced current derivative based protection, their fault discrimination is based on time grading and distance. However, current and current derivative differences for faults located around the edge of the protected zone are quite similar, which are difficult to be distinguished. Therefore, external elements are required to help non-communication-based protection solutions to have more discriminative protection capability. Additional inductance within the protection zone can be a potential option to define the protection boundary;

- Communication-based protection solutions need to effectively deal with the impact of time delay such as 10μs in the selected test cases. These errors are likely to cause maloperations of communication-based protection solutions due to the fast rising of fault currents in LVDC. Using GPS synchronisation is not a cost-effective technique for large LVDC distribution networks. Threshold optimization could be a potential option to improve their reliability, but more fault scenarios need to be undertaken to validate it.

- High impedance fault protection is still a remaining significant challenge that

needs to be considered, which is easy to make protection confused. From the evaluated protection solutions, only current derivative based protection solution can protect against highly resistive fault (i.e. fault resistance detection capability up to 5Ω). The other methods need to be improved to provide higher sensitivity. For example, differential protection can increase its protection sensitivity with a smaller threshold but it will be more sensitive to communication delay and noise.

- High fidelity measurement techniques are required. As LVDC systems experience much faster rise of fault currents than AC systems, measurement errors may confuse communication based and current derivative based protection methods such as ±0.3% noise results in up to 85% errors in current derivative in the selected test case. Also, for some of the existing fault location techniques that are based on current derivative, the unpredictable noise could create significant errors for fault distance estimation, which raises challenges for post-fault maintenance such as cable section replacement and network reconfiguration. To eliminate the noise impact and facilitate the implementation of fast fault detection, fault discrimination, and fault distance estimation, more reliable techniques should be developed. This will be discussed in Chapter 6.

4.5 Chapter 4 Summary

This chapter firstly investigates and quantifies how SST can influence DC fault characteristics. On this basis, the fault characterisation of an SST interfaced LVDC distribution that was developed in Chapter 3 has been established. In addition, this chapter has conducted the evaluation of existing protection solutions to identify and quantify the impacts of SST on the effectiveness of existing LVDC protection solutions.

The development of an effective protection solution is a critical step towards the realisation of future LVDC distribution networks. LVDC protection design is to a great degree dependent on the fault characteristic of the interfaced converters. Therefore, the SST, which is an emerging power electronic device, exhibits unique fault characteristics that influence the performance of conventional protection solutions. Based on

the demonstration and analysis of the limitations of non-unit protection solutions and unit protection methods to achieve effective and reliable fault discrimination, recommendations have been proposed to guide future LVDC protection design to achieve better performance in terms of fault detection, fault discrimination, and fault distance estimation even in the case of limited fault currents.

The work represented in this chapter is an extended version of the author's publications, the details of which are described in [5, 50]

Chapter 5

A Novel Voltage-based Protection Scheme with Enhanced Selectivity

From the previous chapter, it has been established that the reduction in magnitude of the prospective fault current caused by the utilization of SST makes conventional overcurrent-based protection solutions less effective in terms of reliability and selectivity. There are a few methods that have been proposed in the literature which use the changes in voltage profiles as an alternative way to detect DC short circuit faults with limited fault current. However, due to the relatively small value of DC cable impedance, the DC voltage disturbance propagates very rapidly, leading to protection coordination and selectivity challenges.

Therefore, this chapter presents a novel DC voltage-based protection scheme to rapidly detect and precisely locate DC faults in a faulted SST-interfaced LVDC distribution network. The developed scheme does not require communication links while the protection actions of the relays are all driven by local measurements of a combination of parameters including DC voltage magnitude, DC voltage concavity (sign of d^2V/dt^2, extracted from the increasing and decreasing trends of DC voltage derivative (dV/dt)), and the sign of current derivative (dI/dt) regardless of the current magnitudes.

5.1 Protecting an SST Interfaced LVDC Distribution Network

The deployment of SSTs as an innovative technology to improve the controllability and flexibility of secondary substations has recently attracted the interest of a number of utilities and researchers [164]. With regards to LVDC, the SST can either be configured as a two-stage conversion (shown in Figure 5.1 (a)) [165] to provide dedicated LVDC outputs or as a three-stage (shown in Figure 5.1 (b)) [166] to provide both DC and AC outputs. The following section will introduce the main challenges of protecting an SST interfaced LVDC distribution network.

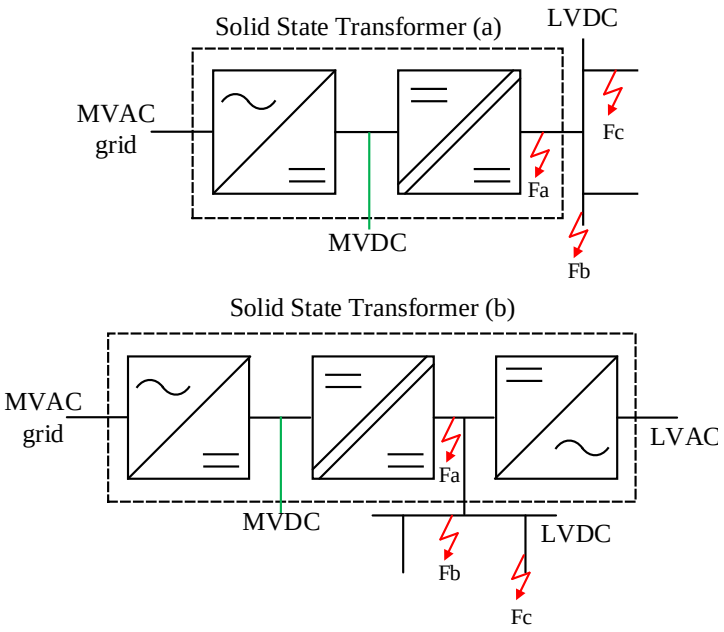

Figure 5.1: A typical SST layout: (a) two-stage SST with DC outputs, and (b) three-stage SST with DC and AC outputs

5.1.1 Protection Challenges

Limited Fault Current

As analysed and discussed in the previous chapter, the implementation of the SST will introduce new forms of DC fault characteristics that can impact existing protection solutions. For example, its active fault current limiting and blocking capabilities can

reduce the thermal stress on diodes by about 19.2% in 10ms and 41.9% in 100ms. This allows the converter to be designed with lower ratings to withstand fault currents. However, the fault current limiting capability (i.e. limit fault current to 1p.u.) leads to almost four times longer fault detection and discrimination time of conventional overcurrent protection than in a common two-level VSC interfaced LVDC system. This has the potential to create a further impact on the whole network protection coordination using overcurrent protection and cause power quality issues [167, 168]

Coordination with Downstream Protection Relays

Challenges of protecting an SST interfaced LVDC distribution network are not just in the limited fault current but also the coordination between downstream protection relays. In contrast to two-level VSCs, SSTs offer multiple power supplies such as MVDC, LVDC, and LVAC. The LVDC link is directly feeding the LVAC power supply. In existing protection solutions for a two-level VSC interfaced LVDC distribution network, the main two-level AC/DC converter can be isolated with additional circuit breakers [73] and without concerns about further network influence propagation. Regarding an SST interfaced LVDC distribution network, if the LVDC power supply is isolated by blocking the SST, power outages will be experienced on the other power supplies. Thus, LVDC downstream protection relays need to be effectively coordinated with the active fault current limiting and blocking functions of SST to avoid any unnecessary outages.

Currently, LVDC protection solutions are still mainly targeted on two-level VSC based LVDC distribution networks. The development of protection solutions based on SST are still not mature due to the attractive simplicity of two-level VSC. However, the increasing interest and the recent implementations of SST form new requirements for developing protection solutions with enhanced performance.

5.1.2 Limitations of Existing Voltage-based Protection Solutions

As discussed in the previous chapter, rather than using current magnitude, voltage-based protection is one of the potential options to overcome the limitation of current-based protection against the limited fault currents of SST. In response to this, currently, a number of voltage-based protection methods have been proposed and developed by

different researchers for protecting DC systems. The research developed in [78] has proposed the usage of under-voltage to detect DC faults and voltage derivative (dV/dt) for fault discrimination. Another method proposed in [169] involves estimating the impedance within the DC fault path using the ratio between the DC steady-state voltages and fault currents in order to identify the fault location in a DC ring microgrid. In addition to these, a new protection method called "Prony's method" is developed in [91] to estimate DC fault locations using attenuation factors and angular frequencies extracted from the voltage resonance when the fault is initiated.

The aforementioned voltage-based protection methods may be sufficient for protecting against faults on LVDC downstream feeders, but may not guarantee adequate protection with a good level of selectivity for upstream faults. The upstream faults are referred to as DC pole-to-pole SST internal faults (e.g. fault 'Fa' in Figure 5.1), faults on the main DC bus (e.g. fault 'Fb' in Figure 5.1) and faults at the beginning of the outgoing DC feeders (e.g. 'Fc' as shown in Figure 5.1). In this case, the SST will experience the same current and voltage response for the internal fault at 'Fa', the fault at the main bus at 'Fb' and at the beginning of the LVDC feeders at 'Fc'. This could potentially lead to the unnecessary tripping of the SST for faults at the main bus or at the main feeders because the same fault distance. The limitations of existing voltage-based protection will be discussed in detail as follows.

Voltage and voltage derivative-based protection solutions have been proposed in DC microgrids [170–172]. Undervoltage-based protection is mainly used for protecting converters. During fault conditions, the simplified circuit diagram of a two-level VSC based LVDC distribution network for the section around the main converter is shown in Figure 5.2. Where, the converter is simplified as a capacitor in the fault transient, R and L are the cable impedance within the fault path, C is the capacitor of the converter, and 'Dt' is the protection relay which measures current and voltage.

In this circuit, the voltage measured by the device 'Dt' can be expressed in (5.1), and the voltage derivative is expressed in (5.2).

$$V = L \cdot \frac{dI}{dt} + I \cdot R + V_f \tag{5.1}$$

$$\frac{dV}{dt} = L \cdot \frac{d^2I}{dt^2} + \frac{dI}{dt} \cdot R + \frac{dV_f}{dt} \tag{5.2}$$

Where V and I are the measured voltage and current of device 'Dt', V_f is the voltage at the respective fault locations. It can be seen that voltage magnitude and voltage derivative are changing and really dependent on the current derivative and impedance of the fault path which is unknown under fault conditions. Thus, it is difficult to establish effective fault discrimination by using voltage and voltage derivative with fixed thresholds.

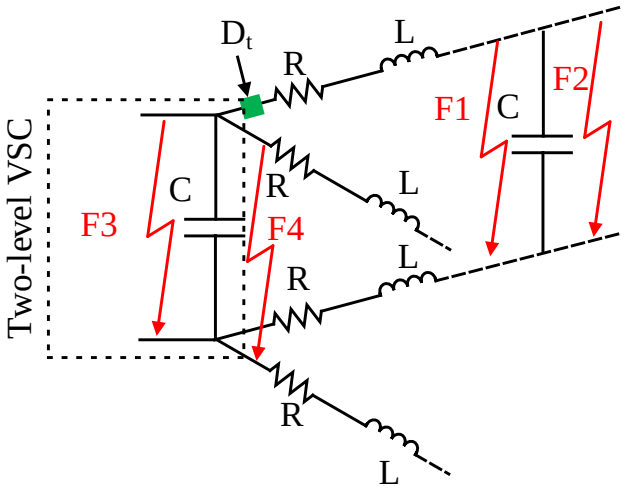

Figure 5.2: Simplified circuit diagram of the LVDC system section around the main converter of a two-level VSC interfaced LVDC systems

For example, there is no significant difference in voltage and voltage derivative under fault F1 condition (internal fault for device 'Dt', at the end of its protection boundary) and fault F2 condition (external fault for device 'Dt', close up to its protection boundary). Similarly, weak fault discrimination is observed for fault F3 and F4 due to the same fault impedance of their fault paths. Also, in this network configuration, voltage and voltage derivative are quite sensitive against the variation of the fault resistance [173]. Figure 5.3 shows an example of voltage response of a two-level VSC interfaced LVDC under F1 fault condition (test model in this section is built as shown in Figure 5.2, the distance from fault F1 to device 'Dt' is 250m, the cable parameters

have been listed in Chapter 3). From this figure, the voltage drop is getting slower when fault resistance is increasing. This brings challenges to threshold selection in terms of protection selectivity. For example, the internal fault with the higher fault impedance will be regarded as an external fault.

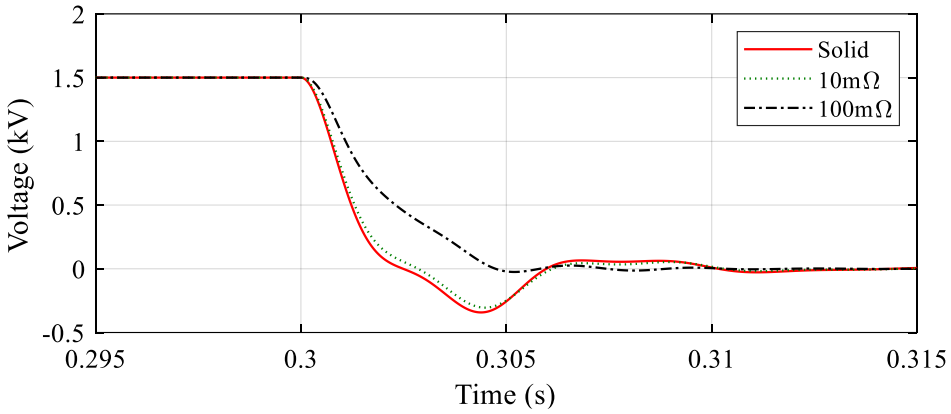

Figure 5.3: Voltage response of a two-level VSC interfaced LVDC distribution network with increasing fault resistance

This weak fault discrimination of voltage-based protection is similar to conventional overcurrent protection that has been evaluated in Chapter 4. Adding an additional inductor to establish a protection boundary could be one of the potential solutions to address this problem, especially if the protection scheme must rely only on local measurements. In HVDC systems, DC reactors [174] and inductors in series with the breakers [78] have been proposed to establish effective fault discrimination. Considering an MMC topology, which is commonly used in HVDC systems that incorporates an arm inductor, the simplified circuit diagram around the converter in an HVDC system is shown in Figure 5.4. In this case, due to the considerable significance of cable capacitance in HVDC systems, voltage and voltage derivative measured by device 'Dt' are buffered, and their theoretical equations are more complex than (5.1) and (5.2). That results in voltage and voltage derivative being more unpredictable than in LVDC systems.

DC reactors and inductors usually come at a large size as their main function is to limit the fault current and slow down the fast rise of the fault current in order to facilitate fault current interruption in HVDC applications [78, 174]. Using the DC

reactor and inductor termination also increases their fault discrimination capability against resistive faults. For example, with 100mH termination inductors, the voltage measured by the device 'Dt' under fault F1 and fault F2 conditions are shown in Figure 5.5, which is conducted in the same system model presented in [175]. It can be seen that the additional inductor creates a voltage difference between fault F1 and F2 fault conditions, which facilitate the threshold setting to distinguish faults F1 and F2 even with significant fault resistance (e.g. 10Ω as shown in Figure 5.5).

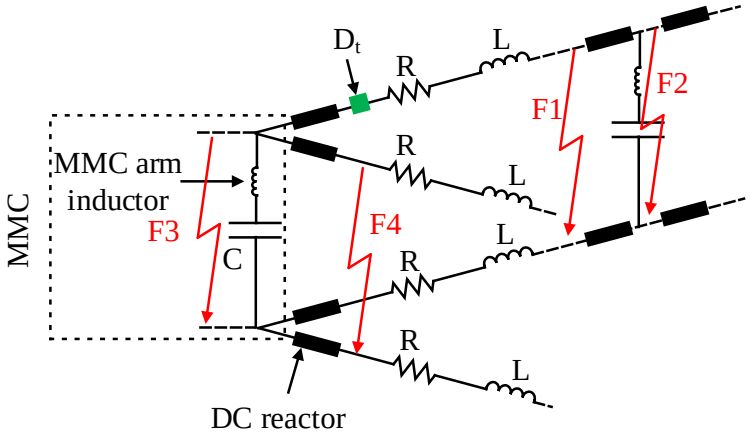

Figure 5.4: Simplified circuit diagram of the section around the main terminal of MMCs based HVDC systems

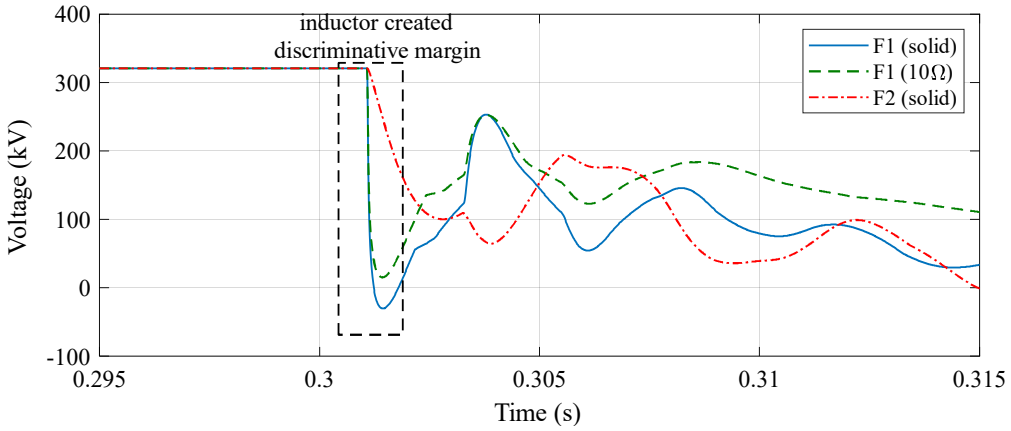

Figure 5.5: Voltage response measured by device 'Dt' under F1 and F2 fault conditions

However, protection schemes based on relatively large inductors at each feeder are less likely to be implemented in LVDC distribution networks. This is because,

- Placement of large inductors at each feeder (e.g. 100mH [78]) could create significant losses and influence system stability [176] as there are lots of power-sharing variations with widely distributed renewable generators [177];
- DC cable capacitance is significant in HVDC systems but it is negligible in LVDC systems [76, 79, 116, 178–182]. Thus, the buffer impact of cable capacitance on voltage and voltage derivative in LVDC becomes much less than in HVDC. This makes voltage drop in LVDC and consequently, more straightforward and fast protection solutions are required.
- Currently, MMCs are not mature in LVDC due to their complexity and high cost. The existing HVDC voltage based method is targeted on MMC based multi-terminal HVDC grids. The arm inductor within MMC helps the protection device not only to distinguish the downstream faults (e.g. F1 and F2 in Figure 5.4 with regard to device 'Dt') but also distinguish the upstream faults (e.g. F3 and F4 in Figure 5.4 with regard to device 'Dt') [174]. In LVDC systems, two-level VSC is a mature technology and SST has a great potential to be widely implemented. When SSTs are implemented, the DC terminal is similar to the 'Two-level VSC' terminal shown in Figure 5.2 without arm inductor in it.

The following will give more detailed explanation about the unique voltage response of an SST interfaced LVDC distribution network with assistive inductors. A simplified circuit diagram is shown in Figure 5.6. In this circuit diagram, the additional inductor as shown in Figure 5.6 is mainly used to distinguish faults to help non-unit protection schemes to provide effective fault discrimination. For example, with the additional inductor that is 10% of the entire cable section, voltages measured by device 'Dt' are shown in Figure 5.7 with different fault conditions, i.e. fault after device 'Dt', fault at the 50% of the cable, fault at the end (100%) of the cable (i.e. F1 shown in Figure 5.6), fault at the 110% of the cable (i.e. F2 shown in Figure 5.6), and fault at the 120% of the cable (i.e. after F2 with an additional inductor). It can be seen that transient voltages derivatives of faults F1 and F2 are quite similar, which could make existing voltage based protection solutions less effective.

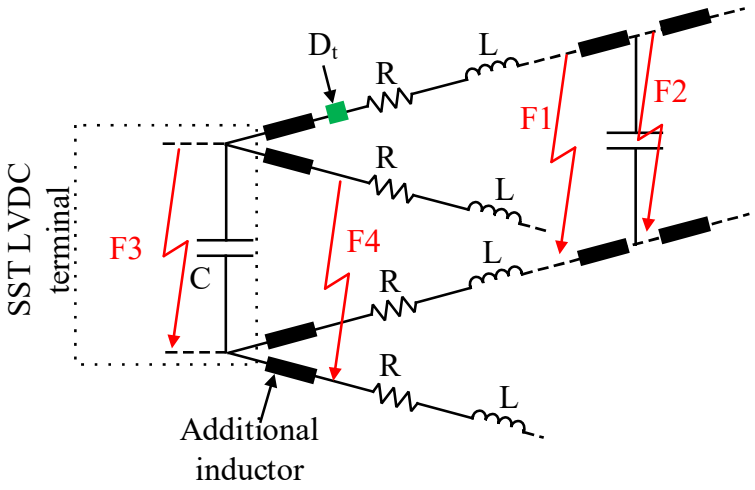

Figure 5.6: A simplified diagram of the part around the main terminal of an SST based LVDC systems

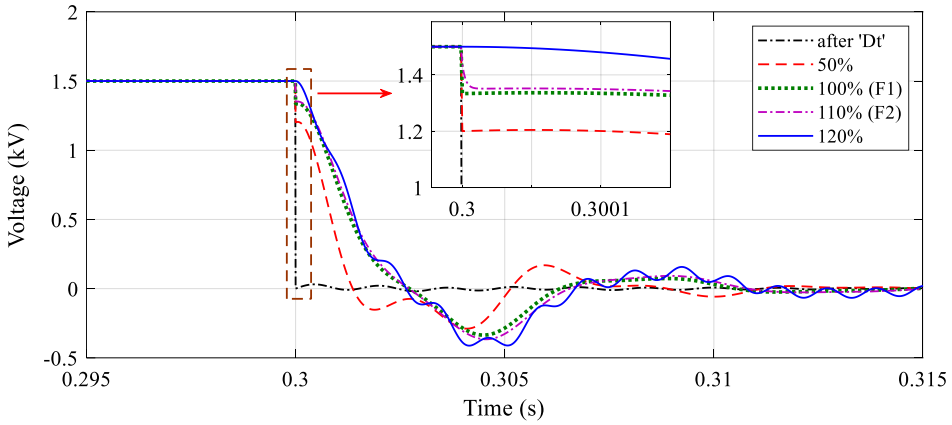

Figure 5.7: Voltage measured by device 'Dt' in an SST interfaced LVDC systems with additional inductors under different fault conditions along the feeder

The limitation of existing voltage-based protection is not only the unique voltage behaviour of downstream faults but also the weakness in distinguishing upstream faults. Regarding the configuration presented in Figure 5.2, with the voltage-based protection (e.g. undervoltage and voltage derivative-based protection solutions), the healthy feeders will be tripped with poor selectivity. For other applications in HVDC systems (with a configuration similar to that presented in Figure 5.4), the research in [78] has proposed the addition of inductance at the start of the DC line to create a voltage drop (ΔV) which can be used to distinguish between faults on the main DC bus and faults

at the beginning of the line by using different dV/dt thresholds. The issue with this method is that resistive faults on the main bus are likely to be seen as a remote fault on the DC lines. For example, Figure 5.8 shows the voltage measured by the device 'Dt' under F3 and F4 fault conditions. It can be seen that for fault F3 voltage drop gets slower than the external solid fault (i.e. F4) when fault resistance is increasing. As the SST LVDC terminals lack arm inductors, the theory presented for protecting MMC based HVDC systems in [174] cannot be applied. Also, Fgiure 5.9 shows the corresponding voltage derivatives under F3 and F4 fault conditions.

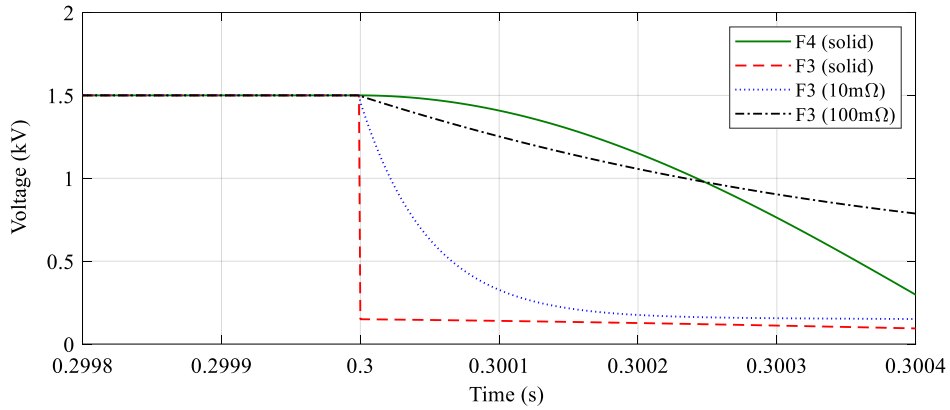

Figure 5.8: Voltage measured by device 'Dt' under fault F4 and F3 conditions with different fault resistance

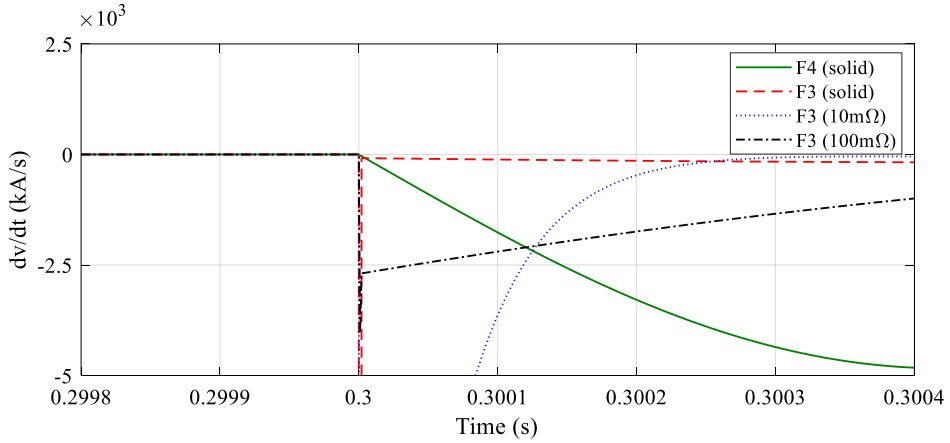

Figure 5.9: dV/dt calculated by device 'Dt' under fault F4 and F3 conditions with different fault resistance

It illustrates that voltage derivative is overlapped which further challenges existing voltage derivative-based protection solutions to discriminate LVDC upstream faults. For example, the resistive upstream internal fault can be regarded as an external fault that makes protection blind. Moreover, the different voltage response (as shown in Figure 5.7 and Figure 5.8) for upstream faults and downstream faults in an SST interfaced LVDC distribution network requires different voltage settings against different fault directions, which has not been considered by existing voltage and voltage derivative-based protection schemes.

Considering the voltage profile difference between internal and external faults, it can be seen that the internal fault shows the concave shape and the external fault shows the convex profile. The concavity of the voltage profile can be represented by the sign of the secondary voltage derivative as shown in Figure 5.10. The external fault has a negative value while the internal faults have positive values. It shows the more discriminative characteristic than voltage derivative which has the potential to be used to establish a more selective protection scheme. Therefore, the following section will present a novel DC voltage based protection that uses voltage concavity to improve the performance of the existing voltage-based protection method to provide a good level of selectivity and discrimination between upstream and downstream faults in an SST interfaced LVDC distribution network.

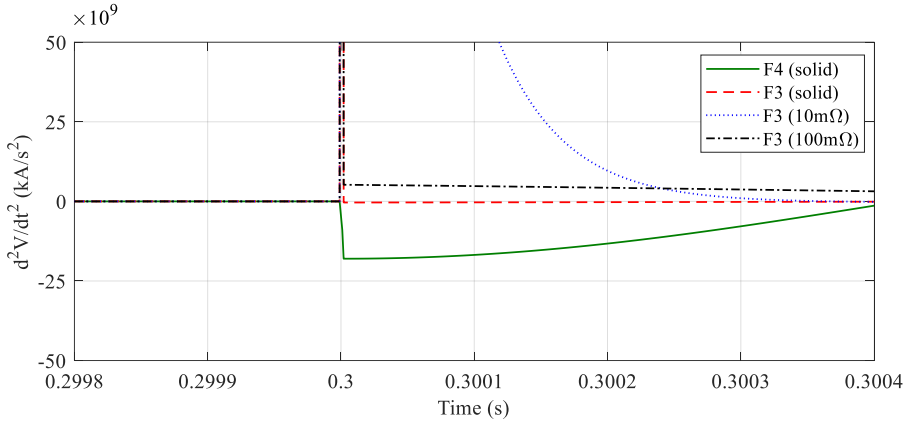

Figure 5.10: d^2V/dt^2 calculated by device 'Dt' under fault F4 and F3 conditions with different fault resistance

5.2 Concept of the Proposed Protection Scheme

The developed protection scheme uses the sign of current derivative (dI/dt) as an indicator of fault direction (i.e. whether the direction is upstream or downstream) in combination with voltage magnitude and voltage concavity (sign of d^2V/dt^2, extracted from voltage derivatives during the fault). The flow chart of the proposed protection scheme is shown in Figure 5.11. The proposed protection scheme is also coordinated with the active fault current limiting and blocking capabilities of an SST. More details of the proposed protection scheme are discussed in the following sections.

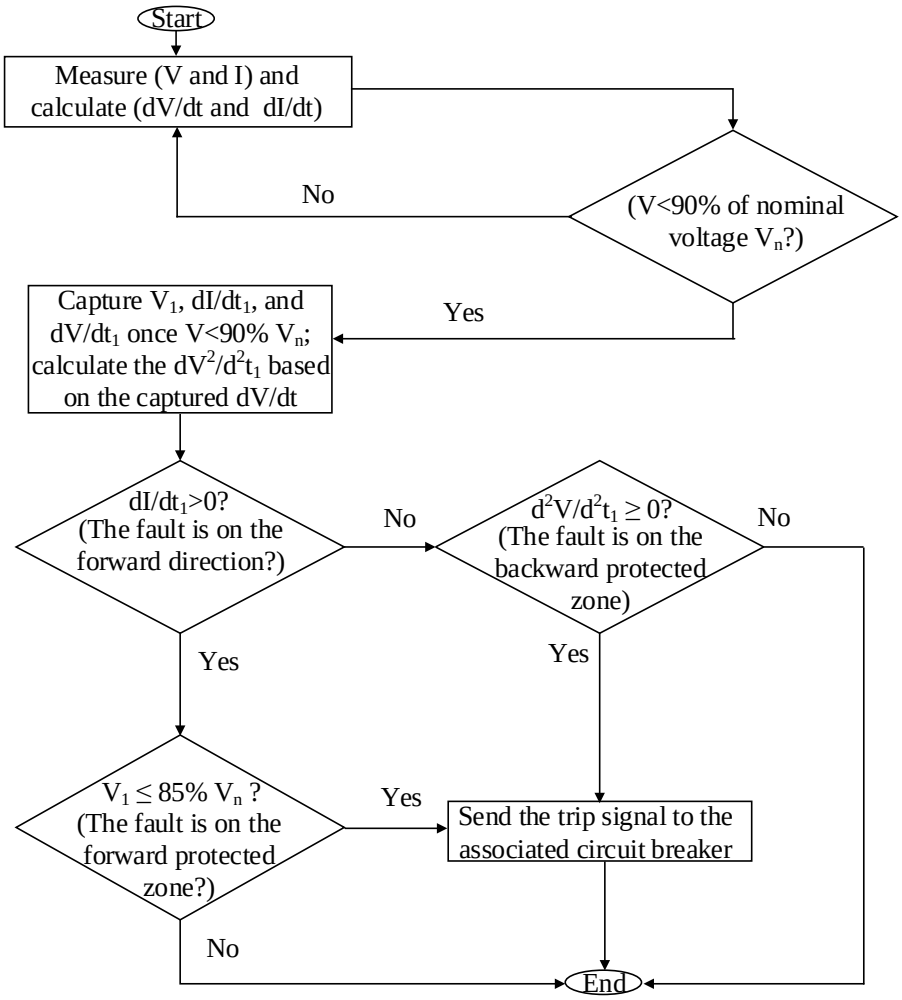

Figure 5.11: Flow chart of the proposed voltage based protection scheme

5.2.1 Key Parameters for the Protection Scheme

The key parameters measured by the local relays within the protection algorithm as shown in Figure 5.11 are the DC voltages and voltage derivatives (dV/dt) along with the signs of current derivatives (dI/dt). In this protection scheme, voltage concavity is indicated by the sign of the secondary voltage derivative that is obtained by comparing the present voltage derivative with the previous voltage derivative under fault conditions. An assistive inductance is also used at the beginning of each DC feeder to create additional boundaries to enhance the discrimination of the voltage responses under different short circuit faults. In general, these parameters are exposed to different levels of noise which can be introduced by measurement devices. Thus, a moving-average low pass filter is used to minimise the noise of all dI/dt and dV/dt profiles.

5.2.2 Voltage-based LVDC Fault Detection

The LVDC distribution network is considered to be under faulted conditions if the DC voltage decreases to <90% of the nominal operating voltage (V_n) (90%V_n defined as δ_1). As reviewed in Chapter 2, currently, no standard exists regarding the acceptable DC voltage variations in LVDC public distribution networks and thus this value is chosen from the IEC60092-101 for marine-based DC distribution systems. During fault conditions, voltage, voltage derivative and current derivative will continue to change until they reach their steady-state. Therefore, the calculated transient current derivative and voltage derivative values (immediately after the fault is detected) are recorded and used for fault discrimination and selective tripping.

5.2.3 Combination of Current and Voltage based Fault Discrimination

A simplified single line diagram of LVDC feeders is presented in Figure 5.12 and is used to explain how the developed protection scheme can distinguish between different DC faults at different locations. A capacitor is added to each bus to emulate the smoothing capacitors typically used in converters. The relays at the beginning of the feeders 'a_1' and 'b_1' are defined to consider the current flow from upstream to downstream (i.e. left

to right) as the forward direction with respect to their locations. The relays at the end of the feeders 'a_2' and 'b_2' are defined to consider the current flow from downstream to upstream (i.e. right to left) as their forward direction. If the calculated dI/dt is positive, the fault lies in the forward direction, otherwise, the fault is located in the backward direction with respect to the relay location.

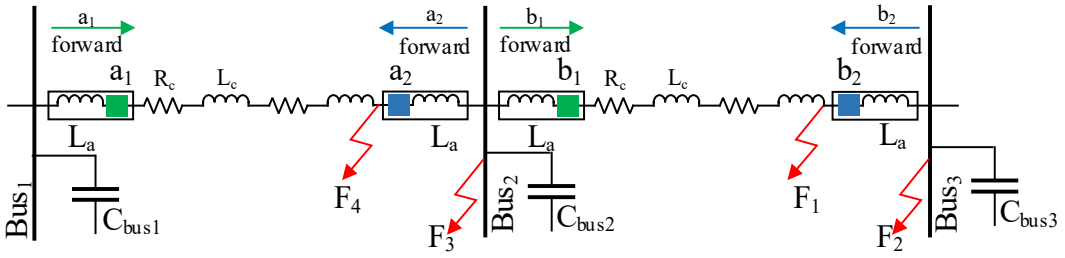

Figure 5.12: A simplified single line diagram of LVDC feeders

Each protection device has its own protected region and it will operate as soon as any fault is located within this region. Taking as an example the protection relay 'b_1', it should operate when faults are located within the cable region between relays 'b_1' and 'b_2' and at the backward bus (Bus_2). As briefly discussed in section 5.1.2, the voltage response of downstream and upstream faults is different, thus, different algorithms to distinguish internal faults and external faults in the downstream and upstream side are required. These algorithms are driven by the sign of the current derivative. Followed with the monitoring of the sign of current derivative, fault direction (i.e. forward or backward) can be identified, and fault discrimination to distinguish if the fault is an internal fault or an external fault is defined in the next paragraphs.

Forward Fault Discrimination of Relay

A DC pole-to-pole fault located at F1 (see Figure 5.12) is selected as an example to illustrate the voltage response of the relay 'b_1' under a forward fault condition. Before the fault happens, the voltage of relay 'b_1' is equal to the DC nominal voltage (V_n). After the fault is initiated, the transient voltage change at relay 'b_1' can be defined as (5.3), where $V_{Bus2}(0^+)$ is the voltage the instant before the fault happens and $V_{Bus2}(0^-)$ is the voltage the instant after the fault happens.

$$V_{Bus2}(0^-) = V_{Bus2}(0^+) = V_n \tag{5.3}$$

Also, the voltage measured at Bus_2 can be written as in (5.4).

$$V_{Bus2} - V_{fault} = L \cdot \frac{dI}{dt} + I \cdot R \tag{5.4}$$

Where V_{Bus2} is the voltage at Bus_2, V_{fault} is the voltage at the fault point (F1), L and R are the inductance and resistance of the cable from Bus_2 to the fault point (F1) and I is the current that flows in the cable section from Bus_2 to the fault point (F1). At the instant before the fault happens (i.e. time (0^+)), the transient voltage, V_{fault}, at the fault point is almost zero due to the relatively small impact of the cable capacitor. Therefore, at time (0^+), the initial current magnitude is relatively small. As a result, the term $(I{\cdot}R)$ is relatively small and can be neglected, allowing the formula presented in (5.4) to be simplified as in (5.5).

$$V_{Bus2} = V_n \approx L \cdot \frac{dI}{dt} \tag{5.5}$$

The voltage difference between the voltage at the relay measured point and the voltage at the fault point is directly influenced by the equivalent inductance between these two points. For example, as shown in Figure 5.12 and at the time (0^+) immediately after fault F1 happens, the transient voltage at relay 'b_1' ($V_{b1\text{-}F1}(0^+)$, where the relay 'b_1' is connected through assistive inductance (L_a) and L' is the inductance between relay point and fault point) can be expressed in (5.6).

$$V_{b1-F1}(0^+) = \frac{V_{Bus}(0^+)}{L} \cdot L' = \frac{V_n}{L_{cable} + L_a} \cdot L_{cable} \tag{5.6}$$

The size of the assistive inductance (L_a) can be easily calculated from (5.6) in accordance with the transient voltage drop settings. In this work, 85% of V_n ($85\%\,V_n$ defined as δ_2) is selected as a transient voltage drop setting to restrict the size of the assistive inductance (L_a) to 10% of the total cable inductance. In practical, the voltage drop may have some delays to reach this pre-set value (i.e. $85\%\,V_n$) due to

capacitive components (e.g. cable capacitance). To solve this issue, an additional time delay is required to eliminate the impact of system capacitive components on the voltage drop. After the fault is detected, if the captured transient voltage (i.e. immediately after the fault is initiated) is below 85% of the nominal voltage (V_n), and the dI/dt slope is positive, then the fault is located within the forward protected region of the associated relay. Also, as the transient voltage after the fault initiates only relates to the inductance of the faulted path as illustrated in(5.6)), the transient voltage based forward fault discrimination can provide a good level of selectivity even against highly resistive faults. For example, Figure 5.13 shows the voltage response of an SST interfaced LVDC distribution network (e.g. voltage measurement of device 'Dt' in the circuit as shown in Figure 5.12 with a 10% assistive inductor and 1.5kV DC link). It can be seen that the transient voltage drop is not influenced by fault resistance.

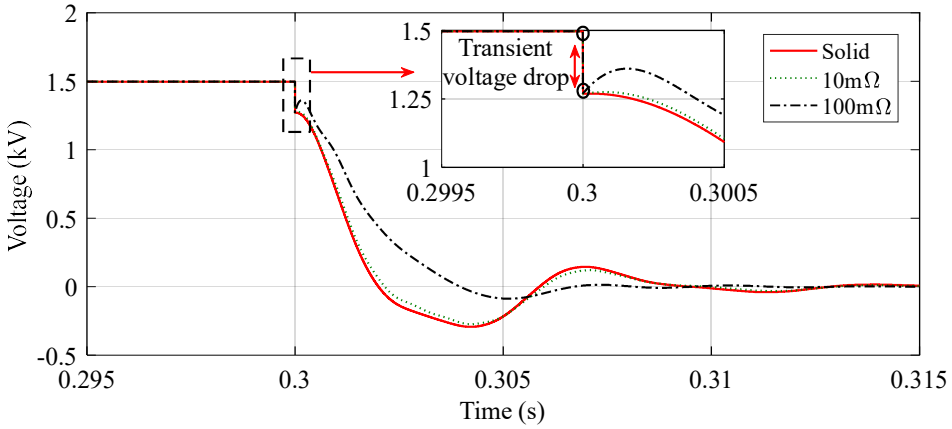

Figure 5.13: Voltage response of an SST interfaced LVDC distribution network integrated with assistive inductor under fault conditions with varying fault resistance

Backward Fault Discrimination of Relay

For the backward faults (e.g. fault F3 in Figure 5.12 with respect to relays 'b_1' and 'a_2') and as discussed in section 5.1.2, it is very important to ensure that resistive faults do not impact the accuracy of detecting and locating DC faults. Taking relay 'b_1' in Figure 5.12 as an example, the resistive fault at location F3 as a backward internal fault can potentially lead to the smaller dV/dt that could be regarded as a backward external fault. To explain this further, Figure 5.14 shows the trace of the resultant

dV/dt of a pole-to-pole fault at the location F3 for varying resistance. It can be clearly seen from Figure 5.14 that for any faults with a resistance $\geq 0.05\Omega$, the dV/dt will overlap with solid faults at location F4. This means the relays 'b_1' and 'a_2' will both see any faults at Bus_2 with a resistance $\geq 0.05\Omega$ as out of their protected backward regions and hence none of them will operate if the protection relies solely on dV/dt with a fixed threshold as proposed in the literature [78].

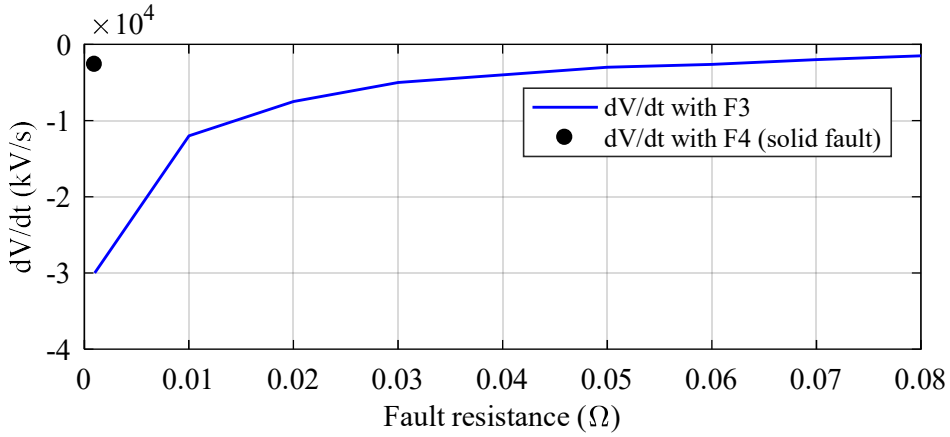

Figure 5.14: dV/dt measured at Bus_2 under fault F3 with different fault resistance

To overcome this issue, the developed algorithm in this chapter utilises multiple points of dV/dt to identify the concavity of the voltage behaviour. The voltage concavity under faulted conditions is derived as follows.

When a resistive fault occurs at location F4 (see Figure 5.12), a resistance-inductance -capacitance (RLC) circuit consists of the fault resistance (R_f), the assistive inductance (L_a) and the Bus_2 smoothing capacitor (C_{Bus2}) within the fault path. The current leaving Bus_2 (I_{Bus2}) can be expressed as in (5.7),

$$I_{Bus2} = -C_{Bus2} \cdot \frac{dV_{Bus2}}{dt} \tag{5.7}$$

The derivative of (5.7) yields equation (5.8).

$$\frac{dI_{Bus2}}{dt} = -C_{Bus2} \cdot \frac{d^2V_{Bus2}}{dt^2} \tag{5.8}$$

Since the dI/dt of the Bus_2 smoothing capacitor is positive during fault transient,

the secondary voltage derivative has to be negative. This means during the transient period of the fault at location F4, the magnitude of the dV/dt is increasing with a negative slope and the voltage drops with a convex trend.

On the other hand, when a backward fault occurs at location F3 (see Figure 5.12), a resistor-capacitor (RC) circuit is formed. In this case, the dI/dt is negative and the sign of the second derivative of voltage (d^2V/dt^2) is positive. This means that during the transient period of the fault F3, the magnitude of the dV/dt is decreasing with a negative slope and the voltage drops with a concave trend. The voltage concavities calculated at Bus_2 and relay 'b_1' are similar due to the small assistive inductor. Consequently, with the discriminative voltage characteristics for forward and backward faults, the protection selectivity of the developed protection algorithm is defined as follows,

- If ($dI/dt>0$) $\cap$ ($V_1 \leq 85\% V_n$), the fault is located within the relay forward protected region.
- If ($dI/dt<0$) $\cap$ ($d^2V/dt^2>0$), the fault is located within the relay backward protected zone.

Converters Fault Discrimination and Coordination with Downstream Relays
Voltage concavity-based fault discrimination can be integrated within the SST to distinguish between faults on the main SST terminals (i.e. PCC) and the fault at the beginning of outgoing feeders. If the sign of d^2V/dt^2 as seen by the SST is positive, then the fault is located at the PCC. Whilst, if the sign of d^2V/dt^2 is negative, the fault is located at the beginning of the feeder (i.e. after the assistive inductance of the faulted feeder). Based on the fault location, the SST can provide two protection functionalities. For faults at the PCC, the SST will interrupt the fault infeed from the grid side, while when faults happen at the beginning of the LV feeders, the SST limits the fault current first to facilitate interruption of the current by the circuit breakers.

5.3 Validation of the Proposed Protection Scheme

In this section, the proposed method is validated in an LVDC test network that is developed from the LVDC model presented in Chapter 3. The proposed voltage based protection scheme is implemented in the LVDC test network.

Different fault scenarios are considered to validate the effectiveness of the proposed protection scheme. Internal faults and external faults that are closed to the downstream and upstream boundaries are selected to test the fault discrimination capabilities of the proposed protection scheme. Also, the results are compared to the performance of the existing voltage derivate based protection solution. The following section will first introduce the developed model that is going to be used in validation, modelling of the developed protection scheme, and detailed simulation studies.

5.3.1 Development of the LVDC Test Network Model

The developed LVDC test network as depicted in Figure 5.15 is developed and used for the validation studies. The LVDC network is interfaced to an AC grid through a two-stage SST. The SST provides ±750V DC at the point of common coupling (PCC). The MVAC grid is modelled as a voltage source with an equivalent impedance to provide a practical fault level representative of an urban MV/LV network [117]. The LVDC feeders are modelled as an equivalent resistance in series with an inductance with each feeder assumed to be 250m long. For the selection of assistive inductors, different cable lengths will require different size of assistive inductor to ensure the threshold setting is effective and secure. A summary of the parameters of the developed test network are given in Table 5.1. The LVDC network supplies four loads, each modelled as a lumped (200kW) load and interfaced to the LVDC network through dual active bridge (DAB) DC/DC converters with galvanic isolation transformers. The local sources are modelled as ideal DC voltage sources. Each feeder is protected by the proposed protection scheme that is modelled as described in the following section.

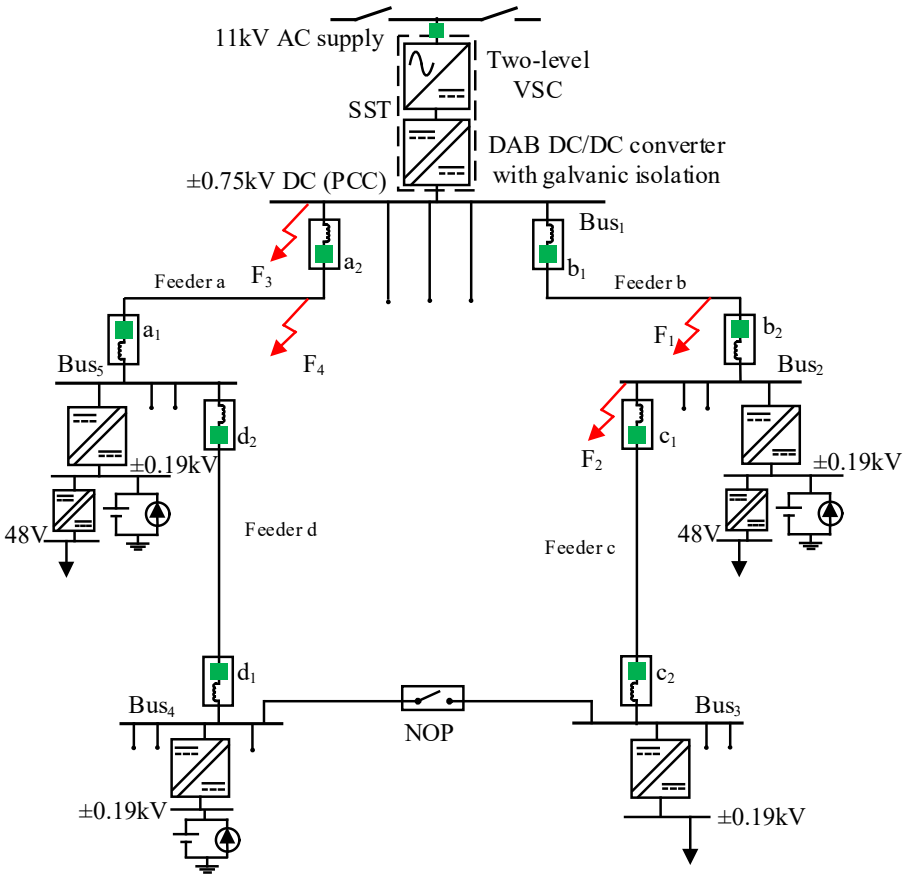

Figure 5.15: A test model of an LVDC distribution network protected with the proposed voltage-based protection scheme

Table 5.1: Parameters of the LVDC test network

Parameter	**Value**
AC supply	11kV
Fault level	174MVA
SST capacity	1MVA
SST DAB parameter	20kV DC/±750V DC, switching frequency 20kHz, LV smoothing capacitor 10mF, choke inductor 1.52mH [183]
MVDC voltage	20kV (pole-to-pole)
LVDC voltage	±750V (pole-to-pole)
LVDC cables	0.164Ω/km, 0.00024 H/km, 250m each section
DC customers	200kW each
Local DC source	380V
Assistive inductors	0.011mH for each pole

5.3.2 Modelling of the Developed Protection Scheme

Related to the above protection algorithm, the threshold settings can be summarised in Table 5.2, and a model of the protection algorithm as shown in Figure 5.16 is developed and implemented in each protection device model of the test network. The relay measures and calculates locally the key parameters (e.g. voltage, current, dI/dt, and dV/dt) and processes them by fault detection and fault location circuits for providing the required tripping signals to the associated breakers if a fault is detected and located. A simplified DC solid-state circuit breaker (SSCB) with 0.5ms operation time is modelled and used for fault interruption [107]. A 0.011mH assistive inductor is added to each breaker. The size of the inductor is calculated using the developed formula (5.6) in section 5.2.3, and is designed as 10% of the total inductance of each cable section.

Table 5.2: Protection Relay Threshold Settings

	Fault Detection	**Fault Discrimination**	
		Forward	**Backward**
Protection Relay (a1, a2, b1, b2, c1, c2...)	$90\%\,V_n$	$dI/dt>0$, $85\%\,V_n$	$dI/dt<0$, $d^2V/dt^2>0$

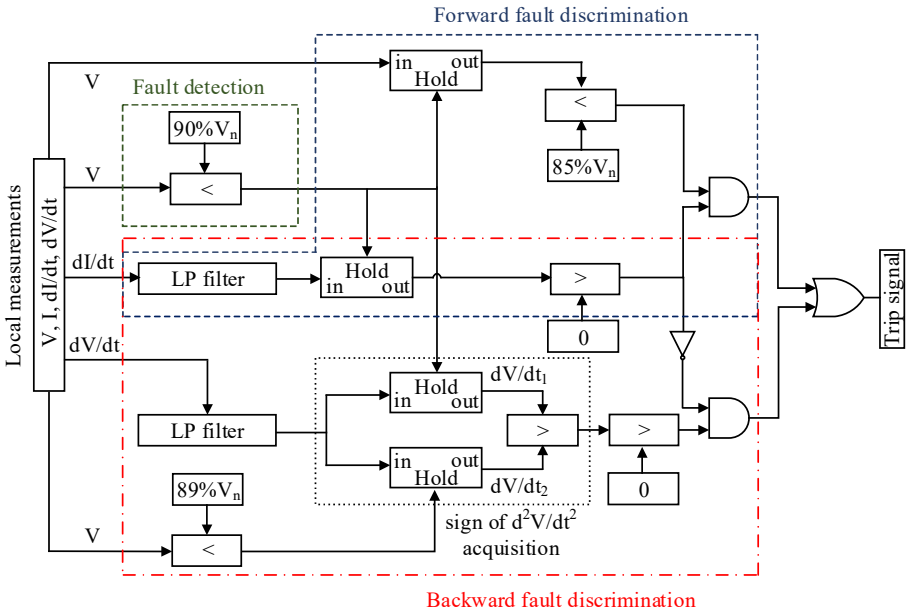

Figure 5.16: Model of the developed protection scheme

To improve the reliability of the developed protection scheme, the impact of noise on dI/dt and dV/dt is considered within the protection model. Since the protection algorithm depends on the direction of dI/dt as one input parameter to locate the fault, the measurement noise can potentially increase the error in the dI/dt direction assessment. Therefore, an actual noise signal captured from a DC current transducer in a laboratory environment is added to the measured currents in the simulation studies [87]. Figure 5.17 shows an example of a dI/dt profile of a DC current with added practical noise. A moving average low pass filter with 100μs window size is selected to eliminate such noise from the calculated dI/dt and dV/dt signals. In addition, 1MHz sampling frequency is applied for the simulation studies to ensure that the protection scheme can obtain the derivative signals within high-resolution windows [140].

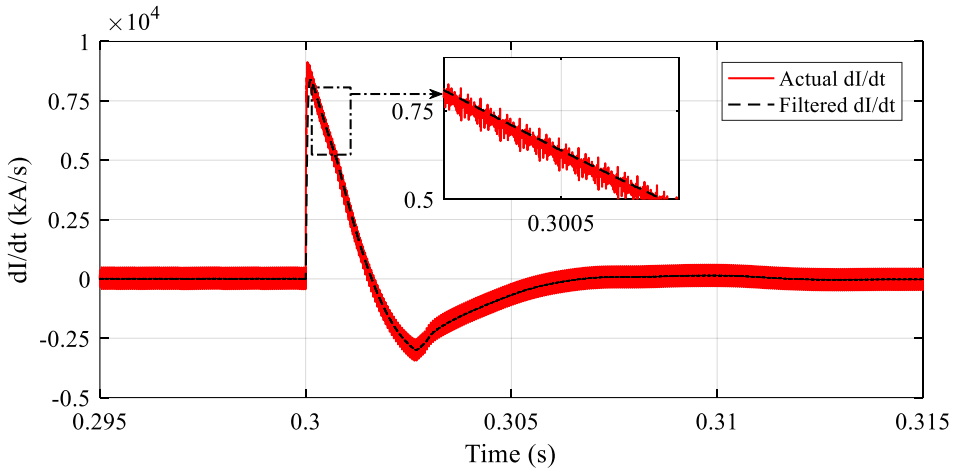

Figure 5.17: A dI/dt signal profile example with and without filtering

5.3.3 Simulation Studies

In this section, protection device 'b_1' is selected as an example, while mainly two downstream fault cases (i.e. F1 and F2) and two upstream fault cases (i.e. F3 and F4) are considered to validate the effectiveness of fault detection and discrimination capabilities of downstream and upstream faults related to device 'b_1'. All the scenarios happen at 0.3s during the simulation in PSCAD/EMTDC. The simulation results demonstrate the improved performance over previous techniques that are presented as follows.

Test case 1: downstream fault discrimination

Under this fault scenario, two downstream pole-to-pole solid faults labelled as F1 and F2 in Figure 5.15 are applied at the end of feeder 'b' and on Bus_2 respectively. Fault F1 should be cleared by protection devices 'b_1' and 'b_2' and fault F2 should be cleared by protection devices 'b_2' and 'c_1'. When fault, F1, is applied on feeder 'b', the voltage responses captured by relay 'b_1' and relay 'b_2' are shown in Figure 5.18. For the detection of the fault, it can be clearly seen from Figure 5.18 that the DC voltages measured by relays 'b_1' and 'b_2' are smaller than the fault detection threshold (δ_1=90% of the V_n). For the fault location, the signs of the dI/dt slopes as calculated by relays 'b_1' and 'b_2' (shown in Figure 5.19) are positive. These indicate that the fault is located in the forward direction of relays 'b_1' and 'b_2'.

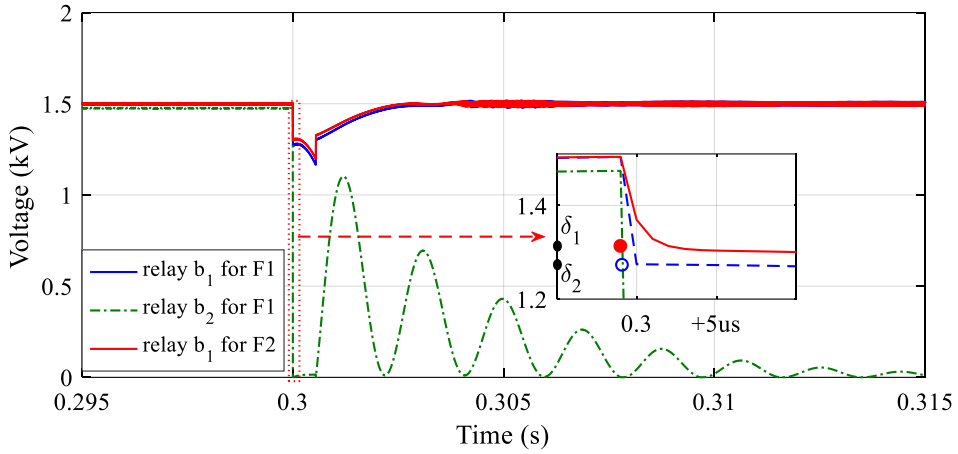

Figure 5.18: Voltage of relay 'b_1' and 'b_2' for solid faults at location F1 and F2

Following the fault detection using the threshold δ_1 and the fault location in the downstream direction using the sign of dI/dt, relays 'b_1' and 'b_2' then identify whether the fault is located within their downstream protected regions or not via a discrimination threshold δ_2=85% of the V_n. From Figure 5.18, it can be seen that for both relays ('b_1' and 'b_2') the transient voltages following the fault are smaller than δ_2=85% of the V_n. Therefore, the fault is located within the downstream protected regions and the relays 'b_1' and 'b_2' will send trip signals to their associated breakers to trip the feeder 'b' to clear the fault, and LVDC supply is restored as shown in Figure 5.20.

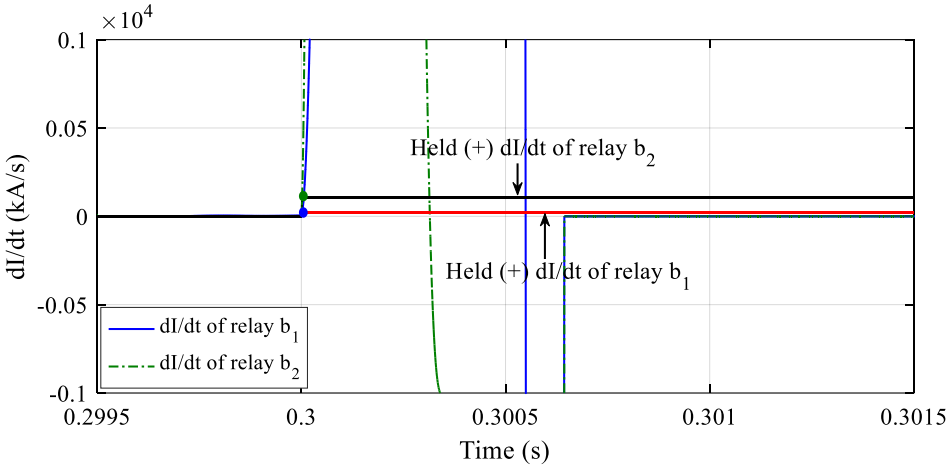

Figure 5.19: Filtered *dI/dt* of relay 'b_1' and relay 'b_2' for a solid fault at location F1

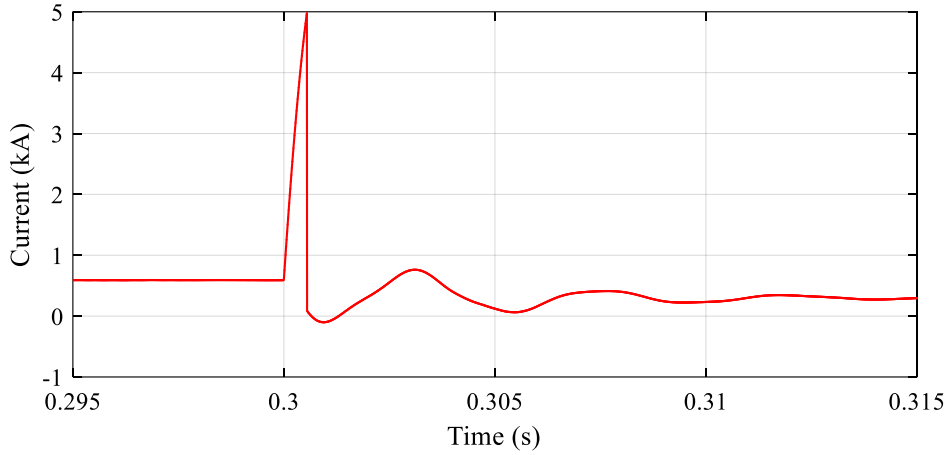

Figure 5.20: Grid current of a solid fault at location F1

For the downstream fault applied at location F2 on Bus_2 (see Figure 5.15) and as demonstrated in Figure 5.18, the relay 'b_1' still detects this fault and sees it as a downstream fault. Since the transient voltage measured by the relay 'b_1' following the initiation of the fault F2 is not smaller than the discrimination threshold δ_2 (85% V_n), the fault then is located outside of its downstream protected region, and no trip signals generated for relay 'b_1' associated breaker.

The above studies have proven the proposed scheme can effectively distinguish downstream internal and external faults. Figure 5.21 shows the timing diagram of the proposed protection scheme.

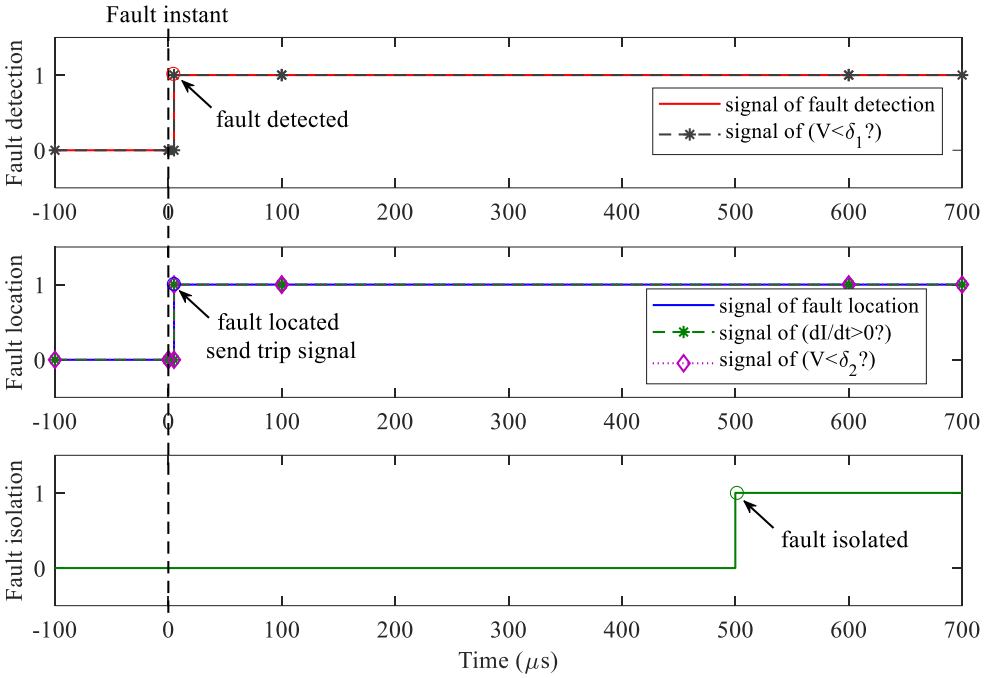

Figure 5.21: Timing diagram of the proposed protection scheme against downstream faults

As the proposed protection relies on the initial fault voltage and current responses, fault detection and location are very fast. The developed scheme requires only 5μs to detect and locate the faults within the relay's downstream protected regions and 500μs to interrupt the fault current using SSCBs (see the fault current in Figure 5.20). This also helps quick recovery of the grid voltage as shown in Figure 5.18.

Test case 2: upstream fault discrimination

In this case, two upstream pole-to-pole solid faults of relay 'b_1', F3 and F4 in Figure 5.15, are applied at the main DC bus (PCC) and at the beginning of feeder 'a' respectively. Fault F3 should be cleared by protection devices 'b_1' and 'a_2' and fault F4 should be cleared by protection devices 'a_1' and 'a_2'. The responses of both relays 'b_1' and 'a_2' when protecting outgoing feeders 'a' and 'b' in addition to the SST protection functionality are studied. When fault F3 is applied, the DC voltages sensed by relays 'b_1' and 'a_2' exceed the fault detection threshold (δ_1=90% V_n) (see Figure 5.22).

In this case, the signs of the dI/dt slopes as shown in Figure 5.23 are negative. Consequently, the fault is located in the backward direction of relays 'b_1' and 'a_2'. Also, using voltage derivative calculated at 90% of V_n (dV/dt_1) and voltage derivative calculated at 89% of V_n (dV/dt_2) to derive voltage concavity to make sure the fault can be discriminated as soon as the fault is detected.

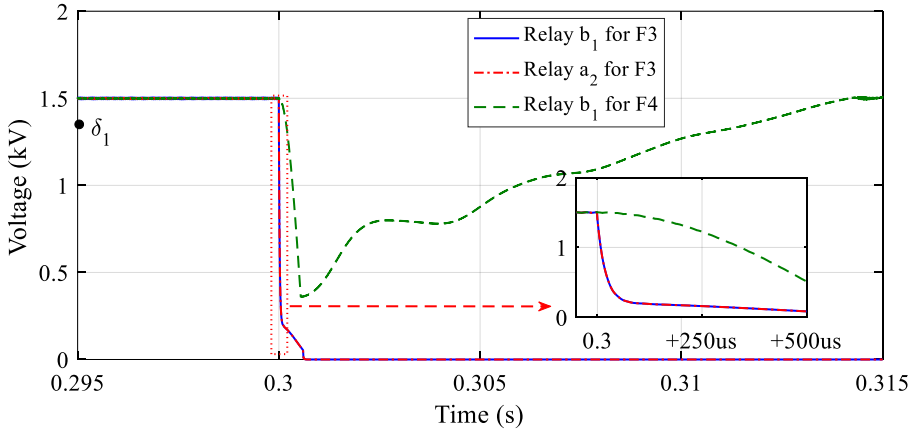

Figure 5.22: Voltage of relay 'b_1' and relay 'a_2' for solid faults at location F3 and F4

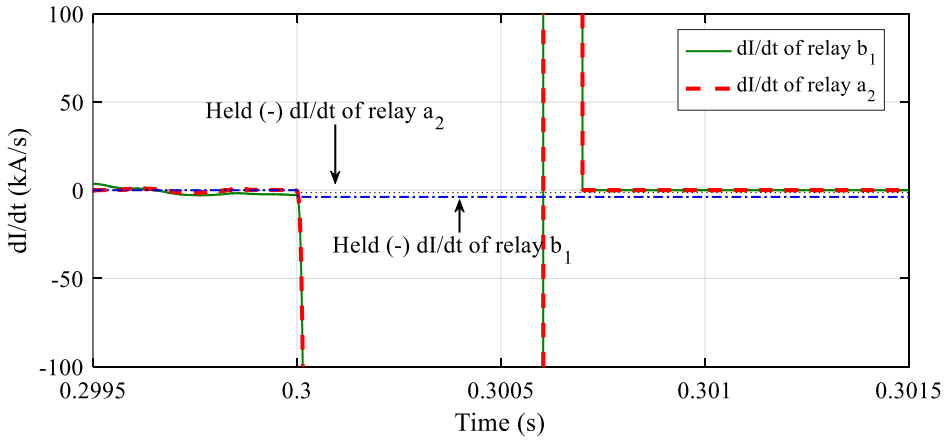

Figure 5.23: Filtered dI/dt of relay 'b_1' and relay 'a_2' for a solid fault at location F3

By capturing two dV/dt values during fault transient shown as dV/dt_1 and dV/dt_2 in Figure 5.24, it can be clearly noticed that dV/dt of relay 'b_1' has a decreasing trend with a negative slope after the fault is detected. The dV/dt of relay 'a_2' has the similar profile as relay 'b_1' under F3 fault condition since they have the similar voltage response as shown in Figure 5.22.

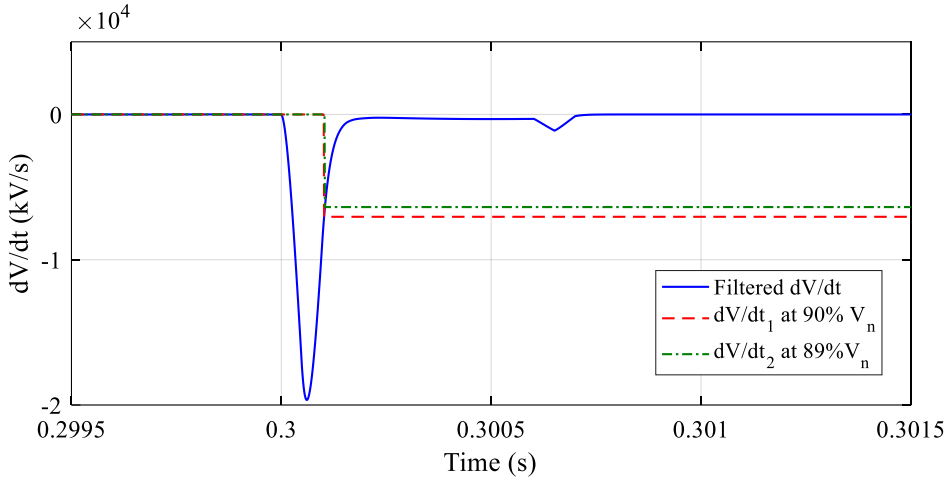

Figure 5.24: dV/dt of relay 'b_1' captured at $90\%\,V_n$ and $89\%\,V_n$ for a solid fault at location F3

This indicates a positive sign of d^2V/dt^2, which implies that the fault is located within the upstream protected regions of relays 'b_1' and 'a_2'. Accordingly, trip signals will be sent by these relays to interrupt any reverse fault currents supplied by local sources (e.g. battery sources). The fault is also interrupted from the AC grid side by blocking the SST as shown in Figure 5.25. The SST, through the voltage concavity-based fault discrimination functionality (implemented in its control), easily detects and locates the fault at the main bus (PCC).

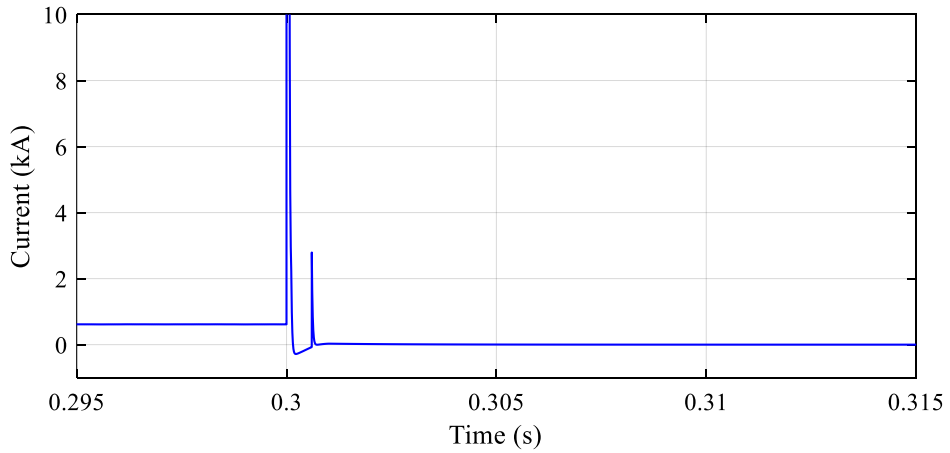

Figure 5.25: Grid current measured at PCC of a solid fault at location F3

For the upstream fault applied at location F4 on feeder 'a' (see Figure 5.15) and as illustrated in Figure 5.22 and Figure 5.26, the fault detection threshold of relay 'b_1' protecting the healthy feeder is passed and therefore, relay 'b_1' detects this fault. However, the calculated transient dV/dt following the fault shows an increasing trend with a negative slope, implying a d^2V/dt^2 with a negative sign and thus the fault seen by the relay is located outside of its backward protected region. Thus, no protection action will be taken by relay 'b_1' and the fault will be cleared by relays 'a_2' and 'a_1' by tripping feeder 'a'.

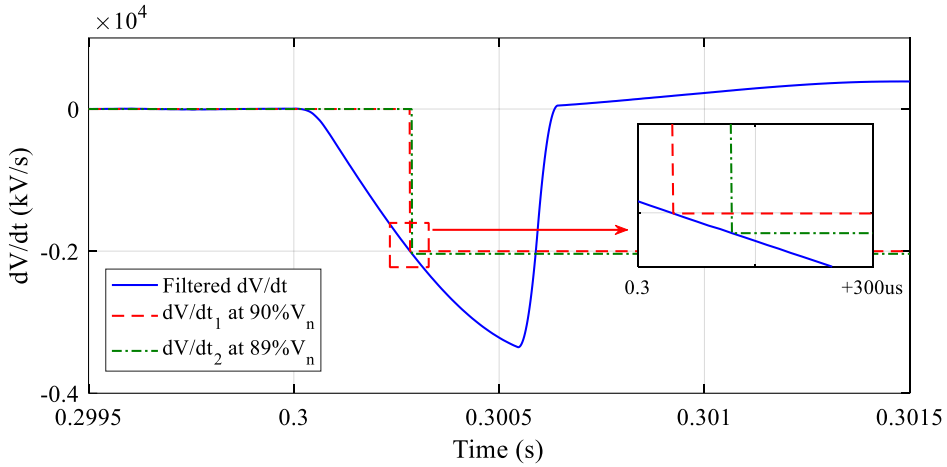

Figure 5.26: dV/dt of relay 'b_1' captured at $90\%V_n$ and $89\%V_n$ for a solid fault at location F4

Figure 5.27 shows the timing diagram of the proposed protection scheme. As the proposed protection relies on the initial fault responses, fault detection is very fast. The main time-consuming part of the protection algorithm is fault discrimination because of the delay of using filters to process the current and voltage derivative signals. For the entire protection scheme, fault isolation consumes most of the time due to the difficulties of DC fault current breaking of available technology.

The protection relay actions under simulated fault scenarios are listed in Table 5.3. The fast and selective performance of the proposed protection scheme can detect, locate, and isolate DC short circuit fault in the early stage of converter capacitor discharge, which improves system stability to ensure resilient operations of LVDC distribution networks.

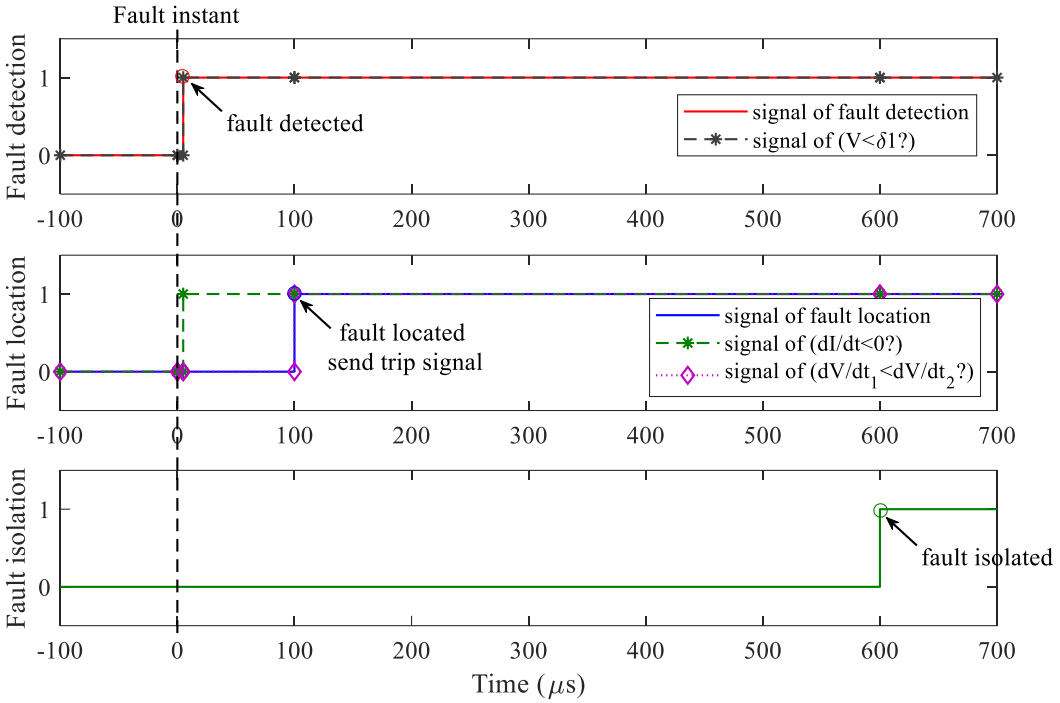

Figure 5.27: Timing diagram of the proposed protection scheme against upstream faults

Table 5.3: Summary of Protection Relay Actions under Simulated Fault Scenarios

	F1	**F2**	**F3**	**F4**
$\mathbf{a_1}$	×	×	×	✓(500us)
$\mathbf{a_2}$	×	×	✓(600μs)	✓(500μs)
$\mathbf{b_1}$	✓(500μs)	×	✓(600μs)	×
$\mathbf{b_2}$	✓(500μs)	✓(600μs)	×	×
$\mathbf{c_1}$	×	✓(600μs)	×	×
$\mathbf{c_2}$	×	×	×	×
✓: trip; ×: non-trip				

Test case 3: protection against resistive faults

As discussed and explained in Section 5.1.2, conventional voltage-based protection schemes are in general vulnerable to resistive faults. Therefore, this test scenario investigates the resilience level of the developed protection algorithm as an improved voltage-based protection solution to DC resistive faults. As discussed in section 5.2.3, based on (5.6), downstream voltage performance is less likely to be influenced by resistive fault compared to the upstream fault. Thus, this section is mainly validating

protection capability against upstream resistive fault. An upstream DC pole-to-pole resistive fault (selected as an example) is applied at location F4 as shown in Figure 5.15. The selection of the fault at F4 to validate protection capability against upstream resistive faults is mainly because it is the most closed to the upstream internal fault at F3, which is highly likely to confuse existing voltage based protection as demonstrated in Figure 5.14. The fault is applied with different resistance and in each case, the increasing and decreasing trends of dV/dt (which are used to identify the sign of the d^2V/dt^2 concavity for accurate fault location) are tested.

Based on simulations, it has been found that the developed voltage concavity-based fault discrimination method becomes less effective when the fault resistance reaches 0.17Ω (that is almost 3 times of resistive fault discrimination capability of the existing voltage-based protection solutions as illustrated in Figure 5.14), as shown in Figure 5.28. When the fault resistance exceeds this value, the dV/dt as presented in Figure 5.28 crosses the maximum point of $|dV/dt|$ in the negative slope. This will cause relay 'b$_1$' for example (see Figure 5.15) of the healthy feeder to see a positive d^2V/dt^2 concavity and hence trip for fault F4 on the adjacent feeder. This limitation can potentially be addressed by relatively increasing the size of the assistive inductor (L_a) per DC pole to widen the range of d^2V/dt^2 concavity fault location.

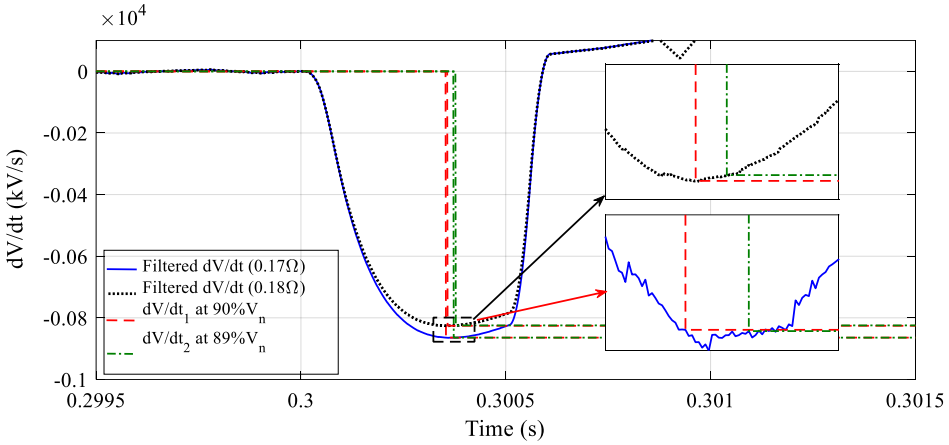

Figure 5.28: dV/dt of relay b1 captured at 90% V_n and 89% V_n for a resistive fault (0.17Ω) and (0.18Ω) at location F4

Figure 5.29 shows that by increasing the L_a from 0.011mH (equivalent to 10% of the total cable inductance) to 0.018mH (equivalent to 15% of the total cable inductance), the capability of the developed protection algorithm to accurately locate resistive DC faults is improved from faults with fault resistance equal to 0.17Ω, to faults with fault resistance up to 0.25Ω.

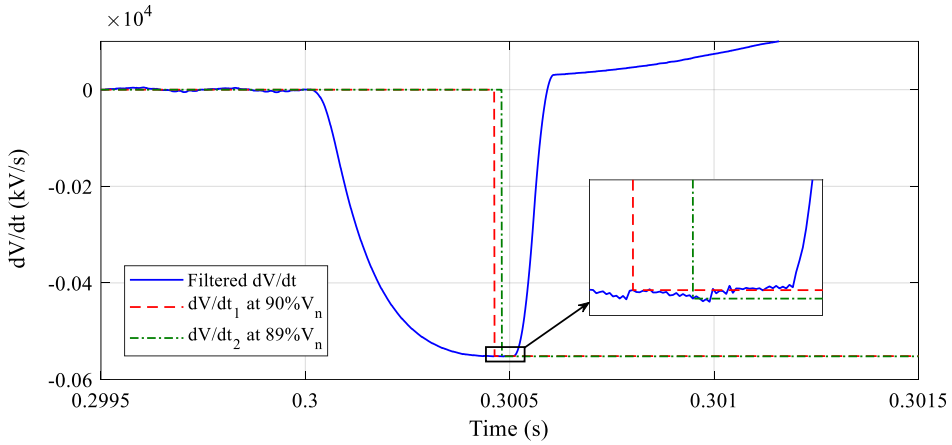

Figure 5.29: dV/dt of relay 'b$_1$' captured at 90% V_n and 89% V_n for a resistive fault (0.25Ω) at location F4 with 15% of total cable section inductance

From the above simulation studies, the key findings can be summarised as follows:

- Existing DC protection methods based on under voltage and voltage derivative have clear limitations for distinguishing between faults at the main DC bus (i.e. PCC) and faults at the beginning of outgoing DC feeders. The advanced protection algorithm presented in this chapter using DC voltage concavity (d^2V/dt^2 by sensing the increasing and decreasing trends of dV/dt) has demonstrated its credibility to overcome such limitations.

- The developed protection solution has proven, through detailed simulation, its fidelity to detect and locate solid DC faults and send trip signals within 100μs. With the fast breakers such as electronic DC breakers, the faults can be detected, located and completely interrupted within <0.6ms. Such fast-acting protection can significantly reduce the stress on the LVDC system during the fault and improve the post-fault system response. Examples include improved SST fault ride-

through capability and power quality by reducing the impact of voltage swells, sags and resonances which can be caused by faults with relatively slow protection.

- The developed protection scheme utilises only local measurements and no communications are required. This can potentially play an important factor for reducing the cost and avoiding any delays or reliability issues that may arise when utilising communication links.

- In comparison to existing dV/dt based protection methods, the developed protection algorithm has demonstrated a considerable improvement in detecting and locating DC resistive faults. As proven by the results, faults with a resistance of up to 0.17Ω can be accurately located that is about three times if conventional dV/dt is used. The limitation in using DC voltage concavity for locating relatively high resistive faults (e.g. up 0.25Ω) can be improved by increasing the size of the assistive inductors (L_a) (added in series with the DC breakers) as shown in Figure 5.30 (e.g. size increased from 10% to 15% of total cable impedance). Also, with the increased assistive inductor, the proposed voltage concavity based protection method has the greater upstream fault resistance tolerance compared to the existing dV/dt based solutions.

- The proposed protection scheme only relies on the transient DC voltage and current characteristics that are mainly dependent on the capacitor discharge of

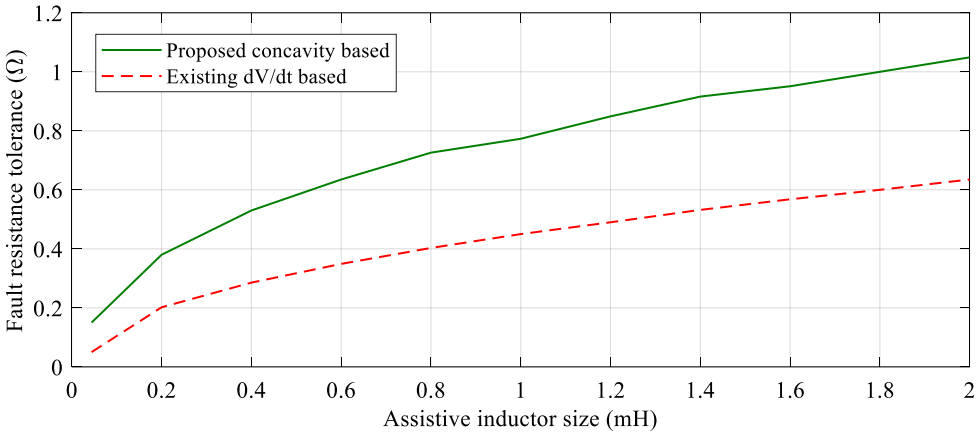

Figure 5.30: Fault resistance tolerance comparison

the converter, which makes the proposed protection scheme applicable for both radial and meshed systems even with different converter interfaces such as two-level VSCs.

5.4 Chapter 5 Summary

This chapter has identified the specific protection challenges of an SST interfaced LVDC distribution network especially implementing existing voltage based protection solutions against the limited fault current of SST. The suitability and limitations of using existing voltage based protection solutions into discriminating LVDC downstream and upstream faults and in providing a good level of protection coordination between relays and converters have been highlighted. Meanwhile, the weakness against resistive fault has been recognized.

On this basis, this chapter has presented a novel communication-less protection scheme that can effectively detect and locate DC faults even with reduced fault levels. The developed protection scheme overcomes the selectivity limitations in LVDC voltage-based protection solutions by applying assistive inductors and using a combination of DC voltage magnitude, voltage concavity (sign of d^2V/dt^2) and the sign of current derivative regardless of the current magnitude.

The credibility and enhanced protection selectivity of the developed protection algorithm have been tested and validated against different fault scenarios applied on an active LVDC distribution network built in PSCAD/EMTDC. Noise signals have been included in the simulation to appraise the resilience of the developed scheme. Based on the simulation results, the proposed protection scheme can detect, locate, and isolate faults within 600μs. Also, it can provide up to 3 times fault resistance tolerance to ensure effective fault discrimination compared to the existing voltage derivative based protection solutions. The enhanced performance of the proposed protection scheme enables wider implementations of LVDC distribution networks.

The work presented in this chapter is extended from the basis of a journal publication, the details of which are described in [184].

Chapter 6

A Novel Fault Let-through Energy based Fault Location with Enhanced Accuracy and Reliability

From Chapter 4, it has been proven that conventional overcurrent-based protection solutions are less effective in terms of reliability and selectivity when SST is utilized in an LVDC system. The above chapter has proposed a new voltage-based protection to provide enhanced selectivity. However, as opposed to DC fault detection requirements for fast and selective performance, DC fault location requires high accuracy and reliability in order to facilitate post-fault maintenance, especially for timely cable replacement and network reconfiguration. Most of the existing fault location techniques are based on external discharge devices that are connected offline (i.e. after protection operates [89]). However, these methods require the faulted section to be isolated first to avoid interaction between the external discharging device and the grid power supply, which are time-consuming [116]. Besides offline fault location methods, a few online (i.e. the method operates during the fault period) fault location techniques have been proposed in [91, 92]. However, these techniques assume the remote end converter is

identical to the main converter. This is less likely to happen in LVDC distribution networks as varying quantities of renewables and end-user devices (e.g. electric vehicle chargers) are connected. Also, the majority of DC fault location methods rely on the relationship between transient voltage, current, and current derivative. However, the magnitude of the current derivative is difficult to capture and very sensitive to noise, while high fidelity data acquisition is challenging [185]. Fault let-through energy (FLTE) is based on the integration of instantaneous current that has been widely used in traditional LV overcurrent protection as discussed in Chapter 4. Although the limited fault current of SST makes FLTE less effective to achieve high protection speed and a good level of fault discrimination, it has the potential to be used as a more reliable fault location indicator to provide fault distance estimation and mitigate significantly the noise effect during integration period.

Therefore, this chapter develops a mathematical model to describe the fault energy during the transient period of DC faults and analyses the impact of remote converters on fault location accuracy. Based on this analysis, a novel FLTE-based fault location strategy is proposed. Also, the estimation error is optimized using a critical point concept (i.e. based on the ratio of local and remote end converter capacity) to locate the fault. The proposed fault location method does not require data synchronization.

6.1 Locating Faults in LVDC Distribution Networks

Existing fault location methods can be classified into offline and online techniques. The former requires an additional external device (e.g. probe unit [186,187]) to inject current into the isolated faulted cable. By analysing the dynamic response of the injected current and the related voltage signals, the fault distance can be estimated. Generally with the probe unit, the main component used for fault location is the predesigned resistor-inductor-capacitor (RLC) circuit which generates predetermined voltage and current waves [80]. Compared to this predesigned circuit, the faulted DC circuit is also an RLC circuit, thus providing opportunities for online fault distance estimation based on the transient RLC fault response during fault period.

6.1.1 LVDC Fault Location Challenges

Offline techniques are more straightforward than online methods. As offline methods usually operate when the faulted cable section is isolated, there is no fault current contribution and influence in offline fault distance estimation. However, it requires extra working time to conduct network maintenance and cable reconfigurations. Compared to offline methods, online fault location estimation techniques provide faster fault location estimation normally during DC fault transient period. However, fault response is deeply influenced by remote converters [90]. Meanwhile, the remote fault current contributions are dependent on the fault resistance and fault distance that are difficult to predict [182]. This raises the challenge for online fault distance estimation techniques of considering the impact of remote converter fault contributions. Also, online techniques mainly rely on fault response during the transient period. Due to the fast changes in DC fault response, noise could create great impacts on the accuracy of online fault distance estimation [186]. This brings challenges for DC metrology and online estimation algorithms to provide a reliable fault distance estimation.

6.1.2 Limitations of Existing Fault Location Techniques

To tackle the aforementioned challenges, some fault location techniques have been proposed. Their applicabilities and limitations have been discussed in Chapter 2 such as the reliability issues of using current derivative to estimate fault distance and un-sufficient determination of the impact of remote end converter on fault location accuracy. Emphasising the reliability issue of using current derivative based techniques to locate a fault, referring the example in Chapter 4, with a noise magnitude of only ±0.3% in the original current signal, the calculated current derivative significantly deviates from the actual current derivative signal (e.g. ±85% as shown in Figure 4.27). This would significantly impact the accuracy of a fault location method based on it. Filters have been introduced in [185] in an effort to eliminate the noise impacts, but the filter design can be complex.

Fault let-through energy (FLTE), defined as $\int I^2 \cdot t$ [188], is the integration of the square of instantaneous current that is a more reliable parameter than the current

derivative, and has been used in conventional overcurrent protection for AC fault detection and discrimination. However, it has not been used for locating DC feeder faults. In contrast to current derivative, FLTE offers the capability to eliminate noise impact and reduce any requirements for additional filters. For example, in the original current signal of Figure 4.27, the variation of FLTE in a 100μs window is only 0.03% when there is $\pm$0.3% noise in the current signals. Therefore, the proceeding section develops a FLTE based fault location method for LVDC distribution networks, using local voltage and current measurements along with the calculated transient FLTE.

6.2 Concept of the Proposed Fault Location Technique

6.2.1 Description of a Mathematical Model based on FLTE

During the capacitor discharge, an equivalent RLC circuit can be established as shown in Figure 6.1, where, C_l and C_r are the capacitors within the local and the remote converters which are considered as the dominant capacitive elements in the fault circuit. This assumption is justified by the fact that the equivalent capacitance of LVDC cables (e.g. 0.1μF/km [152]) is much smaller than the converter capacitor (e.g. 12mF [32]), and therefore can be neglected without significantly affecting the accuracy of the equivalent circuit. R_l and L_l are the upstream impedance up to the local converter, R_r and L_r are the downstream impedance down to the remote end converter.

The relationship between voltage and current on the upstream side (i.e. left side in Figure 6.1 can be described in (6.1),

$$V_l - V_f = V_l - (I_l + I_r) \cdot R_f = L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l \tag{6.1}$$

where, (V_l, I_l) and (V_r, I_r) are the upstream and downstream (i.e. with respect to the fault) voltages and currents respectively, V_f is the voltage at the fault point, L_l and R_l are the total inductance and resistance between the capacitor C_l to the fault point.

To obtain the energy expression, both sides of (6.1) are multiplied by $I_l \cdot \Delta t$ and subsequently integrated for the time period t_1-t_2 (i.e. t_1-t_2 is the first fixed time window

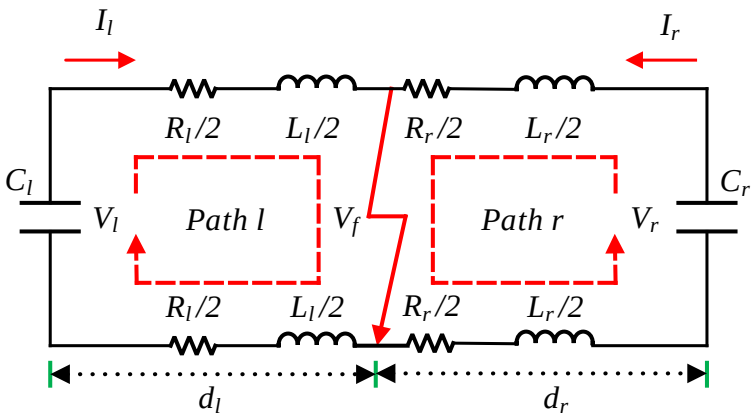

Figure 6.1: Simplified faulted circuit during converter capacitor discharge stage under pole to pole fault conditions

for calculating the energy, t_1 is selected based on overcurrent detection). The resulting energy equation is illustrated in (6.2).

$$\begin{aligned} V_l - V_f = V_l - (I_l + I_r) \cdot R_f &= L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l \\ \rightarrow V_l &= L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l + (I_l + I_r) \cdot R_f \\ \rightarrow V_l \cdot I_l \cdot \Delta t &= L_l \cdot \frac{dI_l}{dt} \cdot I_l \cdot \Delta t + I_l \cdot R_l \cdot I_l \cdot \Delta t + (I_l + I_r) \cdot R_f \cdot I_l \cdot \Delta t \\ \rightarrow \int_{t_1}^{t_2} V_l \cdot I_l \cdot dt &= (R_l + R_f) \cdot \int_{t_1}^{t_2} I_l^2 \cdot dt + L_l \cdot \frac{1}{2} \cdot (I_{l-t2}^2 - I_{l-t1}^2) + R_f \cdot \int_{t_1}^{t_2} I_l \cdot I_r \cdot dt \end{aligned} \tag{6.2}$$

In the right side of (6.2), the first term indicates the FLTE in the resistance within the Path l as shown in Figure 6.1, the second term illustrates the energy in the inductance within the Path l, where $I_{l\text{-}t1}$ and $I_{l\text{-}t2}$ are the currents recorded at time t_1 and t_2, while the final term is the energy in the fault resistance contributed by both upstream (i.e. I_l) and downstream (i.e. I_r) currents. To determine the impedance of the fault path, the energy balance equation is also applied for the time period t_1-t_3 (i.e. t_1-t_3 is the second fixed time window for calculating the energy, t_1 is selected based on overcurrent detection). By combining the two energy balance equations, the inductance of the fault path can be derived by (6.3).

$$L_l = \frac{C_1 - C_2 \cdot \frac{A_1}{A_2}}{B_1 - B_2 \cdot \frac{A_1}{A_2}} - R_f \cdot \frac{D_1 - D_2 \cdot \frac{A_1}{A_2}}{B_1 - B_2 \cdot \frac{A_1}{A_2}} \tag{6.3}$$

While, each term in (6.3) is defined in (6.4).

$$\begin{cases} A_1 = \int_{t_1}^{t_2} I_l^2 \cdot dt \\ B_1 = \int_{t_1}^{t_2} I_l \cdot \frac{dI_l}{dt} \approx \frac{1}{2} \cdot (I_{l-t2}^2 - I_{l-t1}^2) \\ C_1 = \int_{t_1}^{t_2} V_l \cdot I_l \cdot dt \\ D_1 = \int_{t_1}^{t_2} I_l \cdot I_r \cdot dt \\ A_2 = \int_{t_1}^{t_3} I_l^2 \cdot dt \\ B_2 = \int_{t_1}^{t_3} I_l \cdot \frac{dI_l}{dt} \approx \frac{1}{2} \cdot (I_{l-t3}^2 - I_{l-t1}^2) \\ C_2 = \int_{t_1}^{t_3} V_l \cdot I_l \cdot dt \\ D_2 = \int_{t_1}^{t_3} I_l \cdot I_r \cdot dt \end{cases} \tag{6.4}$$

Where, $I_{l\text{-}t3}$ is the current recorded at time t_3. Also, in (6.3), A_1 is the FLTE during t_1-t_2, B_1 is the energy contribution to the cable inductance, C_1 is the energy dissipated in the upstream side during t_1-t_2, and D_1 is the fault energy in the fault resistance contributed from upstream and downstream fault currents. Similarly, A_2, B_2, C_2, and D_2 are the corresponding parameters during time t_1-t_3. Regarding the right side of (6.3), only the first part can be calculated based on local measurements, while the second part is dependent on the remote end fault current (I_r) and fault resistance (R_f).

6.2.2 Optimizing Location Accuracy using the Critical Point

If the fault location relies only on the local measurement of one side, the latter part of (6.3) is recognized as the estimation error that can be written as (6.5).

$$error = R_f \cdot \frac{\frac{D_1}{A_1} - \frac{D_2}{A_2}}{\frac{B_1}{A_1} - \frac{B_2}{A_2}} \tag{6.5}$$

If the ratio of the fault currents (i.e. I_l/I_r) is a constant, the error is theoretically zero due to D_1/A_1 is equal to D_2/A_2. Thus, this fault distance is regarded as the critical

fault location and is defined as the location where the fault current ratio of upstream and downstream is fixed.

It is necessary to know the critical point before a DC fault happens. Using (6.1) and the similar equation based on V_r, the relationship between the voltage and the ratio between upstream to downstream current can be illustrated in (6.6).

$$V_l - V_r = L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l - (L_r \cdot \frac{dI_r}{dt} + I_r \cdot R_r) \tag{6.6}$$

Equation (6.6) can also be expressed as in (6.7).

$$\frac{V_l - V_r}{L_r \cdot \frac{dV_r}{dt} + I_r \cdot R_r} = \frac{L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l}{L_r \cdot \frac{dI_r}{dt} + I_r \cdot R_r} - 1 \tag{6.7}$$

If the voltages on the upstream and downstream sides are equal during the transient fault period, the current ratio is equal to the ratio of the fault distance as seen from the upstream side (i.e. d_l, as shown in Figure 6.1) to that seen from the downstream side (i.e. d_r, as shown in Figure 6.1) and is shown in (6.8).

$$\frac{d_l}{d_r} \approx \frac{I_r}{I_l} \tag{6.8}$$

Assuming the fault current from the capacitor dominates the fault current within the fault path during the transient period, there is a relationship between the voltage and current of upstream and downstream converters as shown in (6.9).

$$\begin{cases} I_l = -C_l \cdot \frac{dV_l}{dt} \\ I_r = -C_r \cdot \frac{dV_r}{dt} \end{cases} \tag{6.9}$$

Combining (6.8) and (6.9), and assuming the voltages from upstream and downstream sides are equal, the critical distance can be derived as the capacitor ratio shown in (6.10). This means that, theoretically, the critical distance is dominated by the size of capacitors connected at both sides of the faulted feeder.

$$\frac{d_l}{d_r} = \frac{C_r}{C_l} \tag{6.10}$$

The following analysis is based on the aforementioned critical distance and focuses on the remote end fault current contributions when capacitors at both ends are the same and local measurements at the upstream side as shown in Figure 6.1 are considered. Moreover, the time period t_1-t_2 and t_2-t_3 are assumed equal to the sampling time Δt. If the fault distance is less than the critical fault location, current I_l is always bigger than current I_r during the capacitor discharge stage. The numerator of (6.5), defined as $error_{num}$ can be evaluated based on Riemann sums left rule [189] as shown in (6.11).

$$\begin{aligned} error_{num} &= \frac{\int_{t_1}^{t_2} I_l \cdot I_r \cdot dt}{\int_{t_1}^{t_2} I_l \cdot I_l \cdot dt} - \frac{\int_{t_1}^{t_3} I_l \cdot I_r \cdot dt}{\int_{t_1}^{t_3} I_l \cdot I_l \cdot dt} \\ &\approx \frac{I_r(t_1)}{I_l(t_1)} - \frac{I_l(t_1) \cdot I_r(t_1) + I_l(t_2) \cdot I_r(t_2)}{I_l(t_1) \cdot I_l(t_1) + I_l(t_2) \cdot I_l(t_2)} \end{aligned} \tag{6.11}$$

During the DC fault transient period (i.e. capacitor discharge phase), the fault current derivative decreases. As the fault path impedance in the upstream side (i.e. Path l as shown in Figure 6.1) is smaller than the downstream side (i.e. Path r as shown in Figure 6.1), the current derivative of the upstream side reduces faster than the downstream side. Thus, from time t_1 to t_2, the ratio I_r/I_l is increasing as illustrated in (6.12).

$$\frac{I_r(t_2)}{I_l(t_2)} > \frac{I_r(t_1)}{I_l(t_1)} \tag{6.12}$$

As a result, the second term in (6.11) becomes increasingly greater than the first term, causing (6.11) to be negative when the fault distance is less than the critical point. In contrast, when the fault distance is beyond the critical point, the sign of (6.11) is positive. Meanwhile, when the fault is located close to the local converter, the current derivative of the upstream side has the highest transient peak compared to the other fault locations. That results in the biggest value of $error_{num}$ with a negative sign. Similarly, when the fault is located close to the remote end converter, the $error_{num}$ has the highest value with a positive sign. Thus, the $error_{num}$ is a monotonic increasing function that is zero at the critical point.

The denominator of the later term of (6.5), is also given by (6.13).

$$\begin{aligned} error_{den} &= \frac{\int_{t_1}^{t_2} I_l \cdot \frac{dI_l}{dt} \cdot dt}{\int_{t_1}^{t_2} I_l \cdot I_l \cdot dt} - \frac{\int_{t_1}^{t_3} I_l \cdot \frac{dI_l}{dt} \cdot dt}{\int_{t_1}^{t_3} I_l \cdot I_l \cdot dt} \\ &\approx \frac{\frac{dI_l}{dt}(t_1)}{I_l(t_1)} - \frac{I_l(t_1) \cdot \frac{dI_l}{dt}(t_1) + I_l(t_2) \cdot \frac{dI_l}{dt}(t_2)}{I_l(t_1) \cdot I_l(t_1) + I_l(t_2) \cdot I_l(t_2)} \end{aligned} \tag{6.13}$$

In the time domain, from time t_1 to t_2, as the current derivative is reducing and current is increasing during the fault transient period, the ratio of current derivative to the current (i.e. *(dI/dt)/I)* is decreasing as illustrated in (6.14).

$$\frac{\frac{dI_l}{dt}(t_1)}{I_l(t_1)} > \frac{\frac{dI_l}{dt}(t_2)}{I_l(t_2)} \tag{6.14}$$

As a result, the sign of $error_{den}$ is positive. Considering the distance to the fault and the fact that the current derivative is directly influenced by the fault distance, the ratio between current derivative and current magnitude reduces for increasing distance. This in turn causes the $error_{den}$ to decrease and behaves as a monotonic decreasing function as fault distance increases far away from local converters.

Table 6.1 summarizes the above qualitative analysis. As the fault moves along the feeder length, if the fault distance is less than the critical point, the estimated fault distance is less than the actual fault distance. Otherwise, the estimated fault location is greater than the actual fault location.

Table 6.1: Summary of fault location errors as fault distance is increasing

Fault distance	**Sign of error**	**Magnitude of error**
<critical point	-	decreasing
>critical point	+	increasing

Figure 6.2 shows an example of estimation errors for different faults (fault distance is assumed with respect to C_l) on the simplified circuit shown in Figure 6.1, when a 500m cable is connected with same capacitors at both ends. In this case, the mid-point is the critical fault location as the Path l and Path r are symmetrical as shown in Figure 6.1. For the fixed time windows t_1-t_2 and t_1-t_3, during which the fault current increases rapidly for any fault along the feeder, the absolute values of $error_{num}$ are symmetrical around the critical location calculated from the local side and the remote

side. Moreover, since the $error_{den}$ is a positive monotonic decreasing function, the value of $error_{den}$ for faults before the critical distance is averagely higher than the one for faults after critical distance. The above characteristics of $error_{num}$ and $error_{den}$ make the estimation error for faults happening at the upstream side of the critical distance relatively smaller than for faults on the downstream side. The validation is shown in Figure 6.2, where the average error of the fault location estimation is significantly smaller for faults before the critical point.

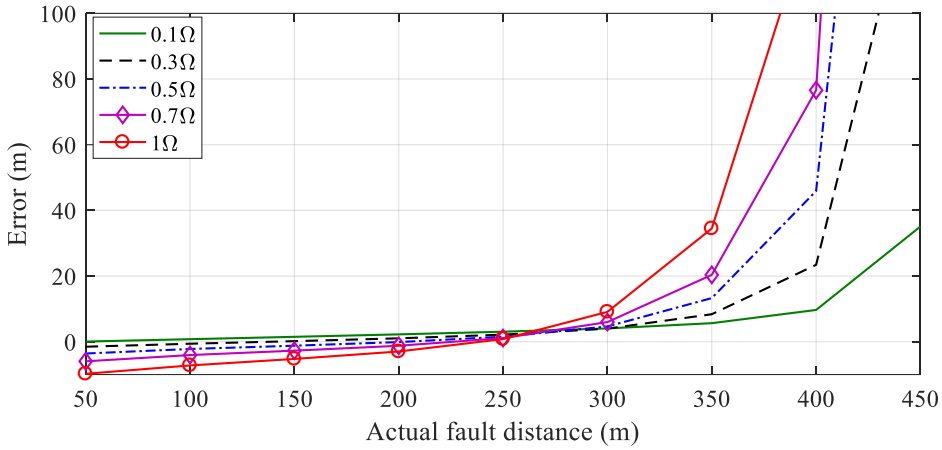

Figure 6.2: An example of fault location errors for faults on an ideal circuit with the same capacitors connected at both ends

Thus, by combining the fault location estimations of both local and remote side based on the critical point, a more accurate result is possible. In detail, the critical distance based fault location working strategy is as follows:

- If the local estimated fault distance is less than critical distance, then this side's estimation is selected.
- Otherwise, the remote side's distance estimation is selected.

6.2.3 Description of a FLTE based Fault Location Algorithm

Based on the previous analysis, a novel fault location technique based on FLTE is proposed. The distance estimation is optimized by the critical distance based fault location working strategy. The proposed method does not require any data synchro-

nization and relies only on local measurements. The flow chart of the proposed fault location algorithm is shown in Figure 6.3.

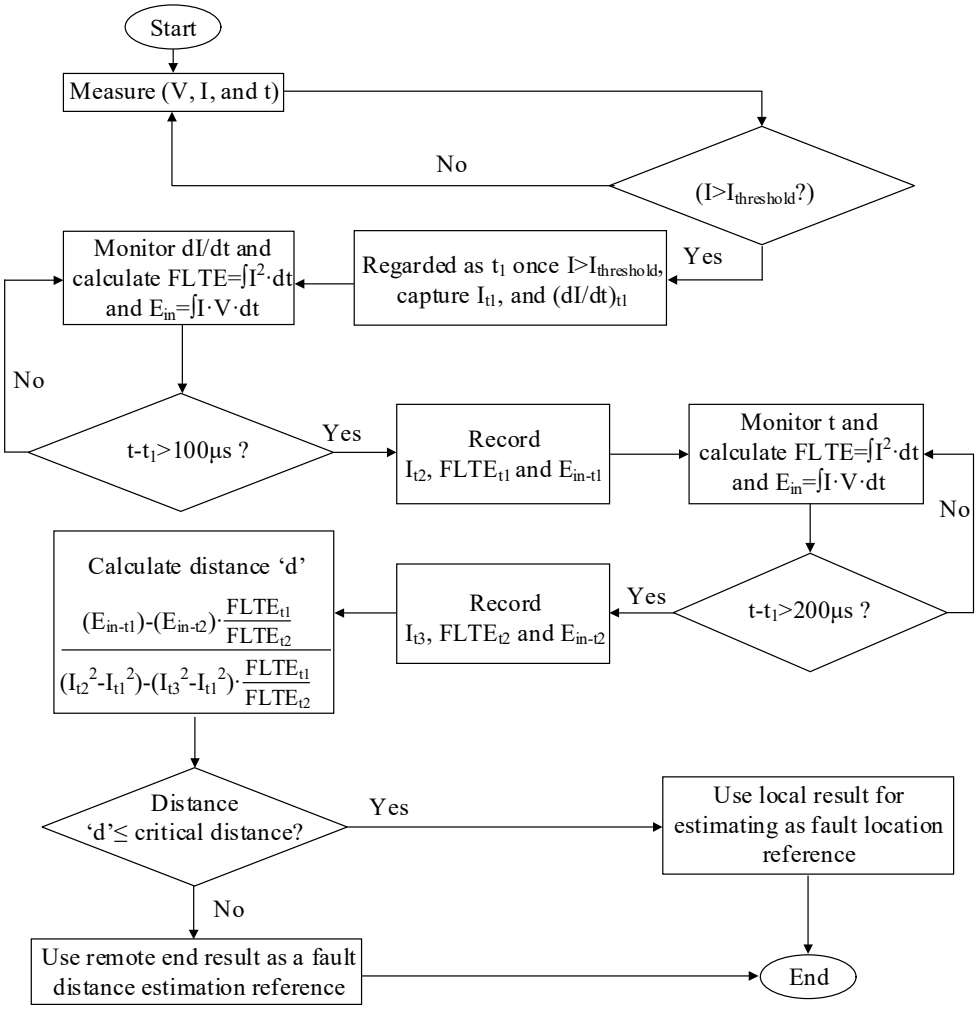

Figure 6.3: Flow chart of the proposed online fault location strategy

The key parameters used by the local fault location devices are the DC voltages, currents, and the calculated FLTEs. The calculation of the injected energy into the fault path is based on the integration of the voltage-current product (i.e. $E_{in}=\int V \cdot I \cdot dt$). As discussed in the previous section, the proposed fault location technique is dependent on the capacitor discharge stage. It is necessary to set criteria for initialising the fault location algorithm when it is required and for selecting an appropriate window to calculate the FLTE. For this purpose, a combination of overcurrent and a fixed time

period is used. Time t_1 is considered as the time instant where the fault current first exceeds the threshold set (i.e. $I_{threshold}$, *1.2p.u.* in this case). The time that after 100μs of time t_1 is recorded as time t_2, while the time that after 200μs of time t_1, is recorded as time t_3. The window selection is mainly described to ensure that the captured data for fault location is within the initial stage of the DC fault transient period.

6.3 Validation of the Proposed Fault Location Technique

The proposed method is validated in an LVDC test network that is developed from the LVDC model presented in Chapter 3. The proposed voltage based protection scheme is also implemented in the LVDC test network. Different fault scenarios are considered to validate the effectiveness of the proposed fault location technique.

Firstly, test the fault location estimation accuracy. Applying faults with different fault resistances (i.e. 0.1Ω, 0.3Ω, 0.5Ω, 0.7Ω, and 1Ω) along a 500m feeder with local and remote converters connected with capacity ratio 2:1 and 4:1. The faults are applied with 50m intervals. Then, test the proposed fault location technique on a 1000m feeder (local and remote converter connected with capacity ratio 4:1 and the faults are applied with 100m intervals). These two steps are testing the impact of different cable lengths and different connected local and remote converter capacity ratios on the accuracy of the proposed fault location technique. At the same time, compared to the results with the existing current derivative based fault location technique under the same conditions in terms of cable length and local and remote converter capacity ratio, to present the fault location accuracy improvements of the proposed method.

Secondly, conduct stability and reliability analysis. This stage is investigating the impact of different noise levels on the accuracy of the proposed method to validate its anti-noise capability. Meanwhile, compared to the results with the existing current derivative based method to highlight the stability and reliability improvements of the proposed fault location technique. The following sections present more details.

6.3.1 Test Network Modelling

An LVDC test network is developed as shown in Figure 6.4. The LVDC is interfaced to an AC grid through a two-level VSC. The VSC provides ±0.75kV DC pole-to-pole voltage at the point of common coupling (PCC). The LVDC feeders are modelled as an equivalent R-L circuit with 500m long. The LVDC network supplies four aggregated end users (200kW each) that are interfaced through a dual active bridge (DAB) converter. The parameters of the network are given in Table 6.2.

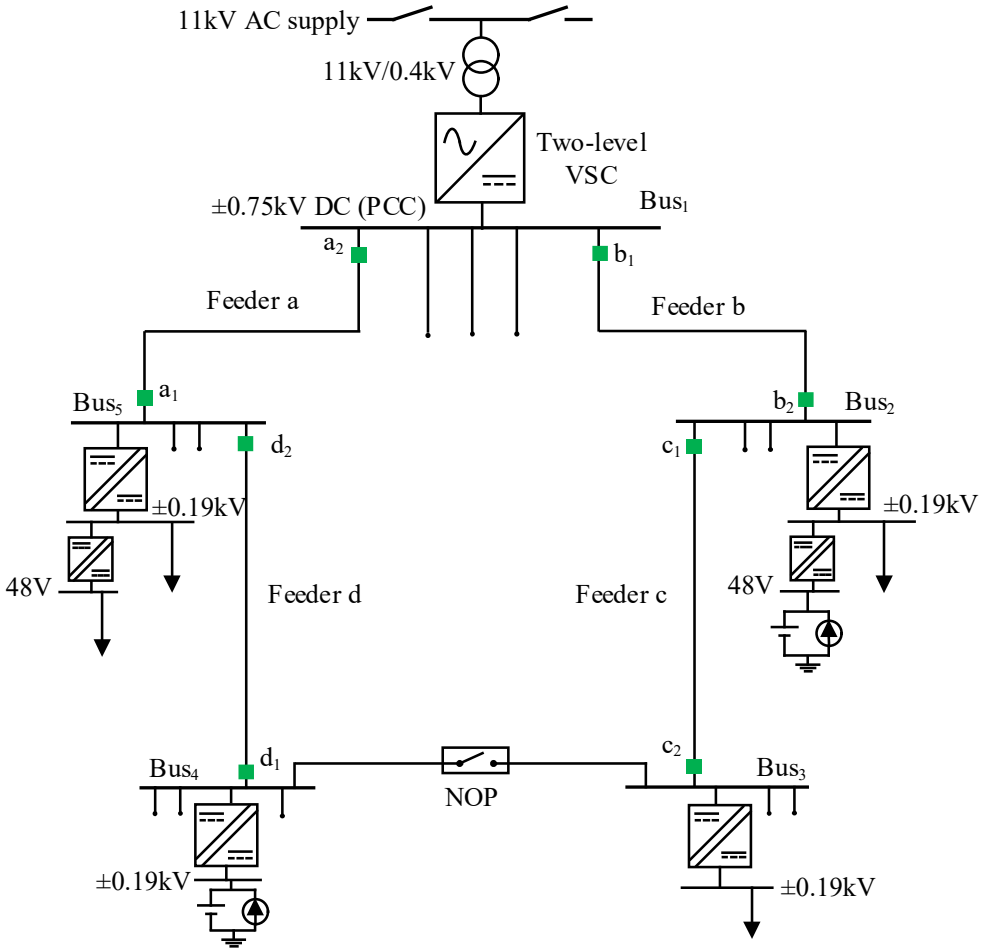

Figure 6.4: A test model of an LVDC distribution network used for validating the proposed fault location technique

Table 6.2: Parameters of the LVDC test network

Parameter	Value
Transformer	11kV/0.4kV
VSC	1MVA, 5mF
LVDC distribution voltage	±0.75kV (pole-to-pole)
LVDC feeder	0.164 Ω/km, 0.00024 H/km, 500m
DAB converter	±0.75kV/±0.19kV, 200kW, 2.5mF

6.3.2 Model of FLTE based Fault Location

The model developed for the implementation of the proposed fault location algorithm is illustrated in Figure 6.5. Devices 'b_1', and 'b_2' shown in Figure 6.4 are fault location devices. For each fault location device, only voltage, current, and time are monitored with 1MHz sampling frequency [185]. Each device is updated with the associated critical point (i.e. 'b_1' is 167m, 'b_2' is 333m). To add credibility to the simulation based validation, voltage and current measurements are contaminated with noise signal (±0.3% variations) captured from an experimental LVDC test bed [87].

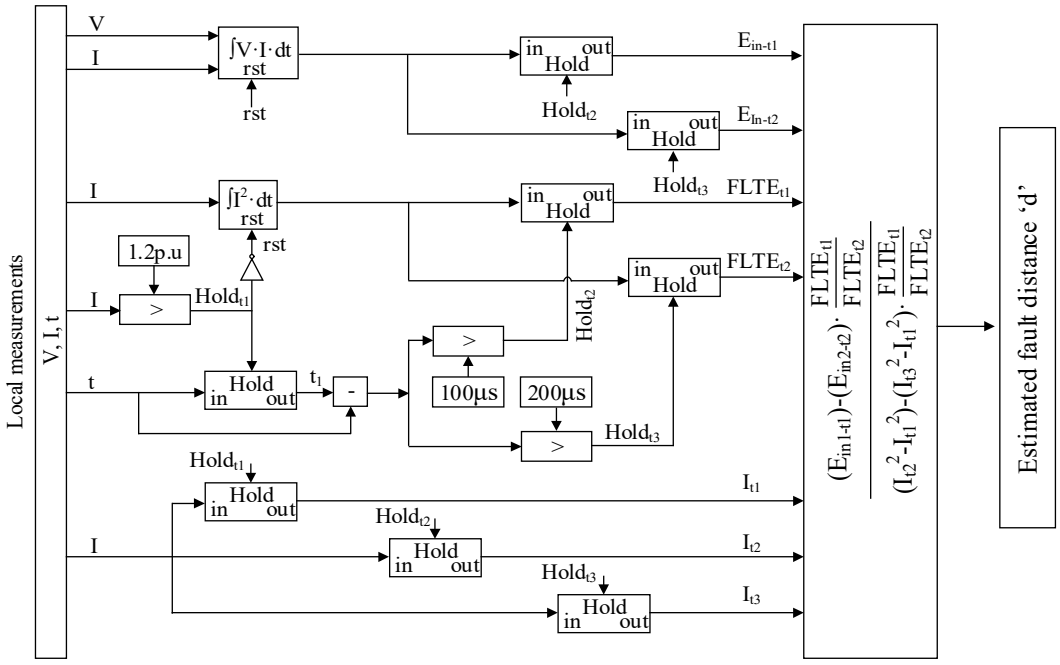

Figure 6.5: Model of fault let-through energy based fault location

6.3.3 Simulation Validation

In the simulation studies, DC pole-to-pole faults are applied along the 0.5km cables with 0.1Ω fault resistance intervals in the range from 0.1Ω to 1Ω. Faults are applied on feeder 'b' to test the case where the feeder has converters of different size connected to its ends.

A. Fault Location Estimation Accuracy

Figure 6.6 shows the fault location errors of device 'b_1' for faults on feeder 'b' for different fault distances and fault resistances. Within 167m, the fault location estimation of device 'b_1' has a relatively small error (1.7m, 3%, the fault at 50m away device 'b_1'). When the fault moves beyond 167m, the fault location error increases significantly (up to 393m, 87%, the fault at 450m away device 'b_1').

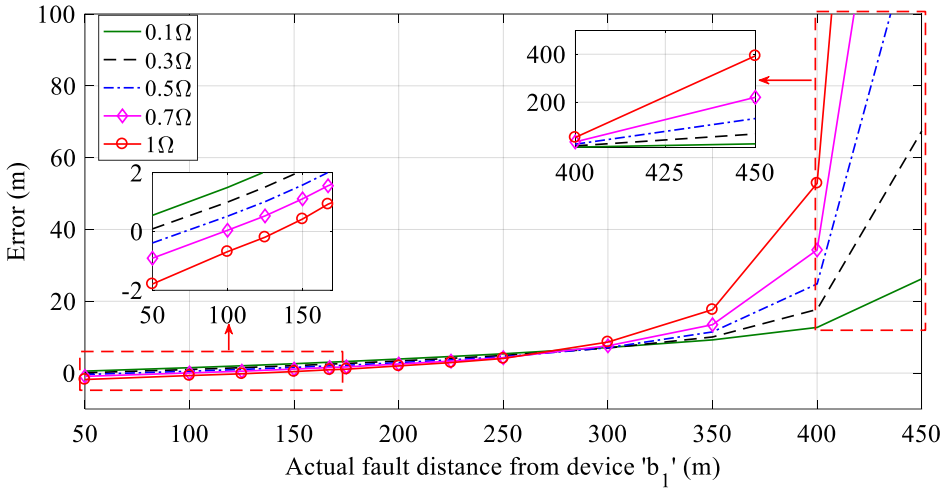

Figure 6.6: Fault location errors of device 'b_1' when faults located on feeder 'b'

For device 'b_2', the fault location error is relatively small (up to 3.5m, i.e. 0.7%, for a fault at 450m away device 'b_1') for faults that occur within the critical distance (333m away from device 'b_2') as shown in Figure 6.7. When the fault occurs beyond the critical point, the estimation error can reach up to 213m, representing 426% distance error for the fault 50m away from device 'b_1'. It is evident that the fault location estimation from both sides of the cable are significantly different when the LVDC feeder is connected with different converters at each end. It is therefore necessary for a workable estimation

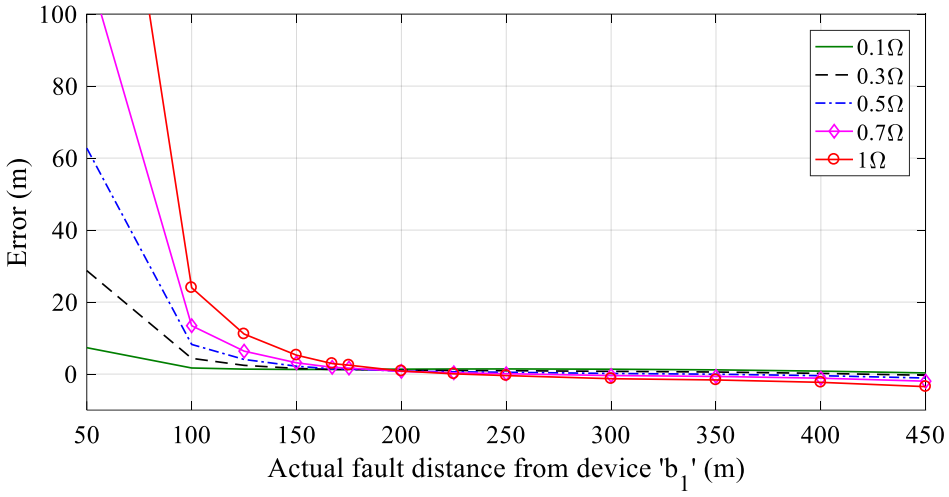

Figure 6.7: Fault location errors of device 'b_2' when fault located on feeder 'b'

algorithm to select the appropriate device ('b_1' or 'b_2') to be used for locating the DC fault. The existing strategy for locating DC faults as proposed in [170], namely the 50% rule, relies on each protective relay being responsible for locating DC faults in the first half of the feeder. Nevertheless, if this strategy is used in this particular example greater errors will arise because device 'b_1' can provide more accurate fault location estimation for the first 33.3% of the feeder rather than the remaining 66.7% of the feeder.

For example, Figure 6.8 shows the errors of the critical point based estimation method for a 500m cable connected with converters (local to remote capacitor ratio is 2:1). Its estimation errors are within the range of (-2.5m to 3.5m, average 0.6%). In terms of the improvements of the fault location working algorithm, compared to the existing 50% fault location strategy, the proposed critical point based strategy has smaller estimation errors and provides more accurate fault location estimation especially for the faults located in the range of 167m to 250m away from device 'b_1'. For example, when fault resistance is 0.1Ω, using capacitor ratio based fault location strategy, fault estimation error can be reduced up from 2.1% (i.e. 5.4m) to 0.5% (i.e. 1.4m). The simulation results of this basic case illustrate the effectiveness of the proposed method that is using FLTE and critical distance based fault location working algorithm.

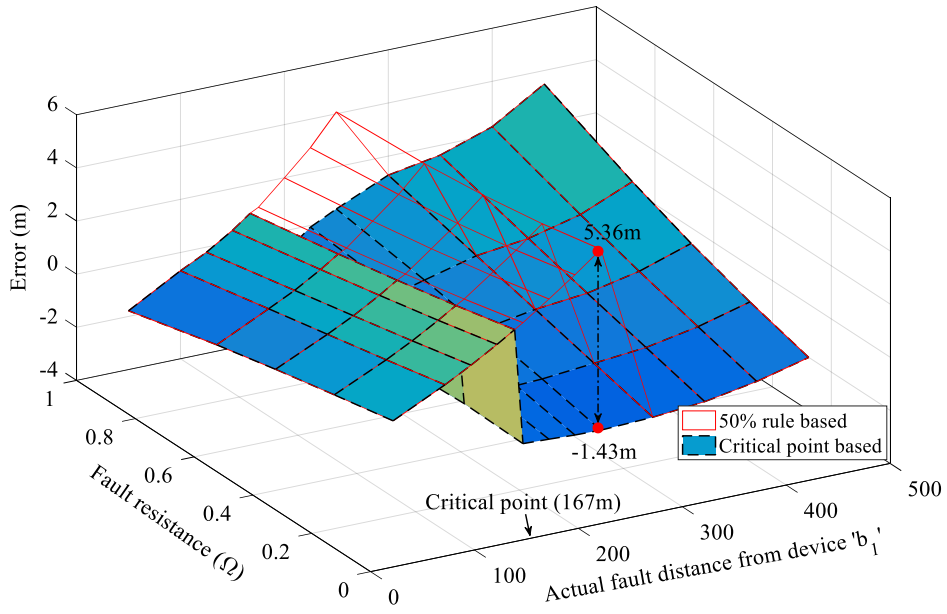

Figure 6.8: Fault location errors based on 50% rule and critical point for a 500m feeder with converter capacitor ratio 2:1

B. Stability and Reliability Analysis

The following section will validate its stability and reliability against different converter capacitor ratios, different length of cable, and noises. To investigate the stability of the proposed fault location strategy, the ratio of capacitor size of local and remote converters is increased to 4:1. Figure 6.9 shows the errors of the proposed estimation method for a 500m connected with converters (local to remote capacitor ratio is 4:1). Its estimation errors are within the range of (-0.9m to 10.3m, average 1.6%). In terms of the improvements of the proposed critical point based fault location working algorithm, compared to the existing 50% fault location strategy, when the fault resistance is relatively small ($\leq$0.2Ω), the proposed critical point based strategy provides more accurate fault location estimation in this case. For example, when fault resistance is 0.1Ω, using the critical point based fault location working strategy, fault estimation error can be reduced from 2.4% (i.e. 6m) to 0.3% (i.e. 0.9m). However, as fault resistance increases, fault resistance dominates the estimation error more than the remote fault current contribution (see (6.5)), and the errors of the distance estimation are getting negatively affected leading to increased errors when local and remote estimations are

combined based on the critical point based working strategy.

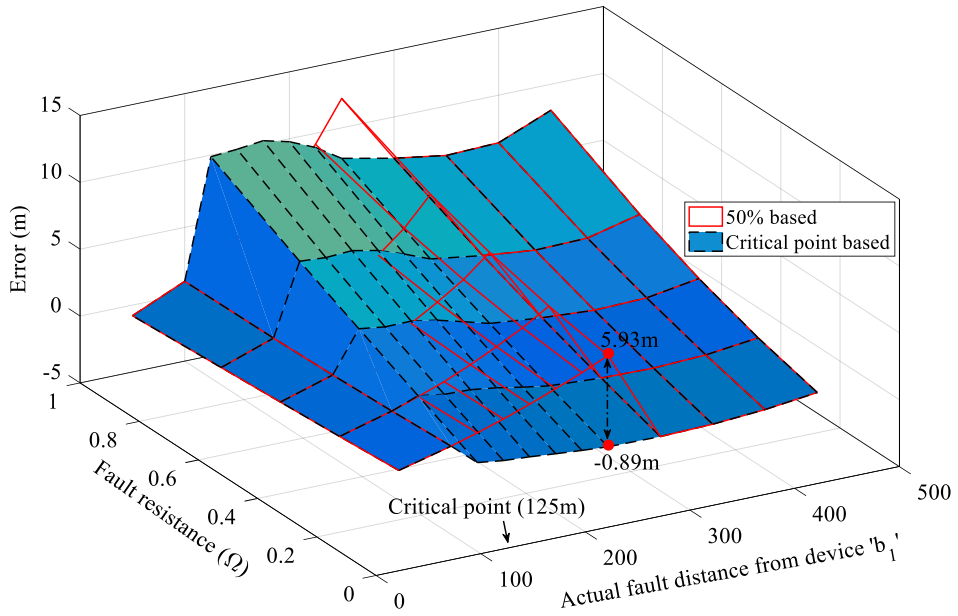

Figure 6.9: Fault location errors based on 50% rule and critical point for a 500m feeder with converter capacitor ratio 4:1

The increasing estimation errors for highly resistive faults becomes less when locating faults for a 1000m feeder connected with different converters (local to remote capacitor ratio is 4:1). In this case, the critical distance is 200m away from device 'b_1'. Figure 6.10 shows that the errors of using the proposed fault location strategy in this case are within the range of (-1.4m to 4.6m, average 0.4%). The estimation errors are smaller than the ones from the existing 50% based fault location working algorithm. For example, for a 0.1Ω fault, the estimation error can be reduced from 3% (i.e. 15m) to 0.12% (i.e. 0.6m). Compared to the results in the 500m feeder case shown in Figure 6.9, the reduced fault estimation errors are mainly caused by the increased cable impedance. The impact of the increasing fault resistance in the fault estimation error (as illustrated in (6.5)) is less significant than the remote fault current contributions.

From the above analysis, it can be summarised that the ratio of capacitor size and cable length will influence the performance of the proposed fault location algorithm compared to the existing 50% rule. However, for a relatively small fault resistance (e.g. 0.1Ω), the proposed algorithm is always more accurate (e.g. error reduction up to

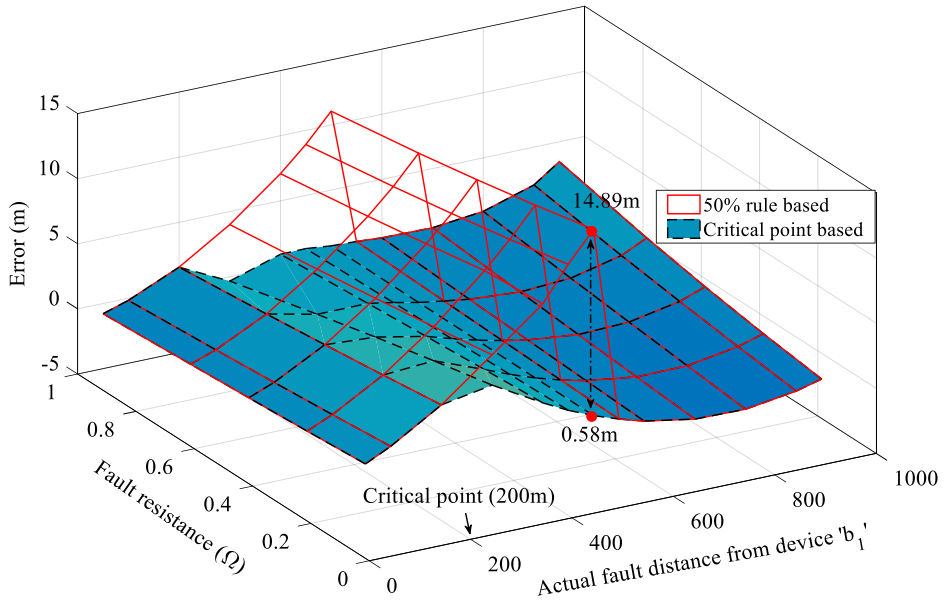

Figure 6.10: Fault location errors based on 50% rule and critical point for a 1000m feeder with converter capacitor ratio 4:1

15m, 3%) among the studies. Apart from the improved accuracy, enhanced reliability against noise impact is another key improvement. For example, Figure 6.11 shows the behaviours of current, current derivative, and FLTE with white Gaussian noise (signal-to-noise ratio (SNR) 40dB and 20dB) under a 250m 0.1Ω fault (at 0.2s) on a 500m feeder. It can be seen that current derivative signals are almost destroyed with SNR 40dB and 20dB noise signals. Comparatively, the SNR 40dB white noise has negligible impacts on the FLTE as shown in Figure 6.11 (c). Even for the significant SNR 20dB white noise, it only creates a small range of FLTE variations ($\leq$0.23%). The high immunity of FLTE allows the proposed FLTE based fault location technique to provide reliable fault distance estimation with a good level of accuracy under significant noise conditions.

Table 6.3 illustrates the average estimation errors for estimating faults ($\leq$1Ω) on 500m and 1000m feeders with white Gaussian noise signals (SNR 60dB, 40dB, and 20dB). The estimation error of the proposed method is within 5% for a 500m feeder and 2.5% for a 1000m feeder which is less likely to be achieved by the existing current derivative based fault location techniques without using additional complicated filters.

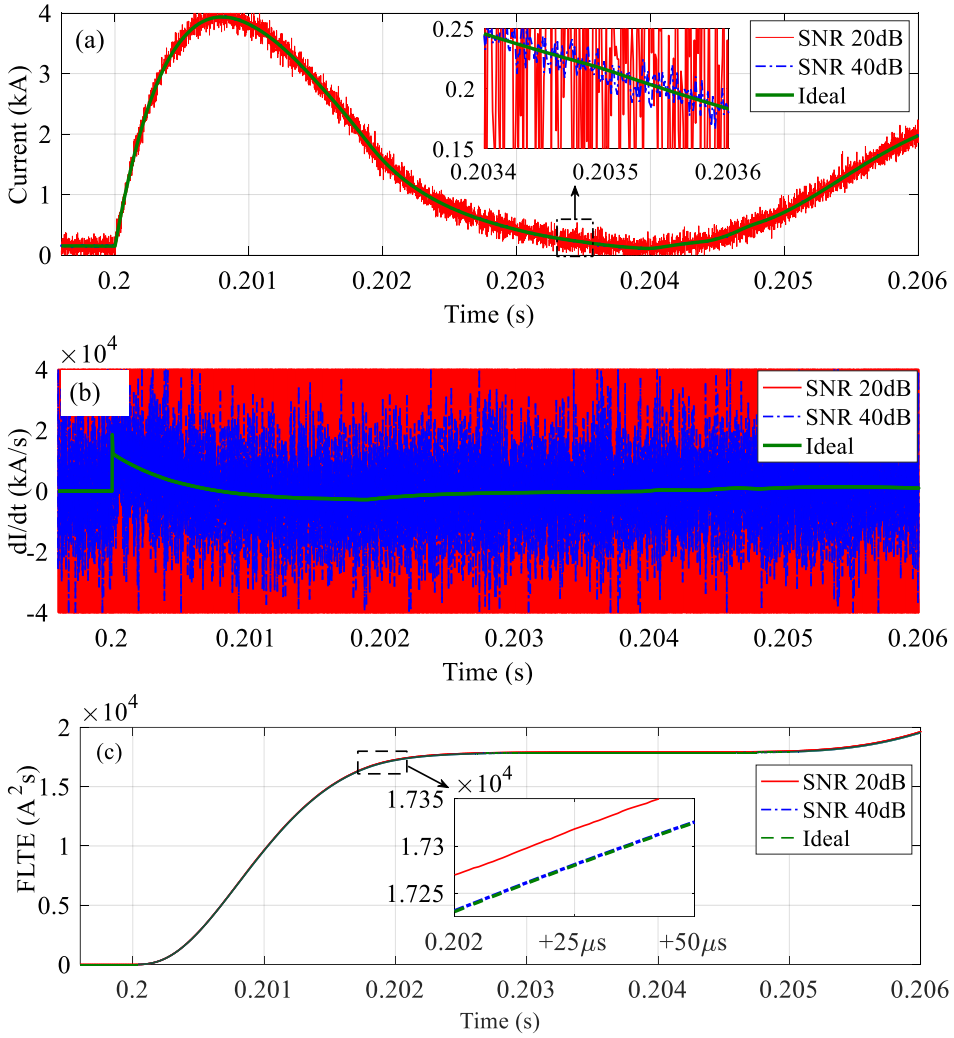

Figure 6.11: Response of current (a), current derivative (b), and FLTE (c) with noise signals under a 250m 0.1Ω fault on a 500m LVDC feeder

In particular, the current derivative based method with filtering discussed in [92] has been included in the comparative results shown in Table 6.3. The results of the existing current derivative based method are obtained by simulation studies conducted in PSCAD following the illustrations in [92]. While, both local and remote end location devices are used to locate DC faults in the first half of the feeder. It can be seen that even with properly designed filters that have been presented in [185], the estimation errors of the current derivative based fault location technique can be up to 18.85% for a 500m feeder and 24.88% for a 1000m feeder with 20dB noise signals. These errors are

Table 6.3: Average estimation errors of the proposed methods under different noise levels

SNR (dB)	Average Estimation Error (≤1Ω)			
	500m feeder		1000m feeder	
	Proposed (FLTE)	Existing (dI/dt) [92]	Proposed (FLTE)	Existing (dI/dt) [92]
60	0.58%	1.1%	0.65%	3.42%
40	2.5%	7.6%	0.94%	11.80%
20	4.7%	18.85%	2.54%	24.88%

mainly originating from the distortion of current and voltage signals caused by the use of filters. The comparison between the two methods highlights the significantly greater reliability and accuracy of the proposed FLTE based method at different noise levels. In addition, as the proposed fault location technique only relies on DC fault transient, it will also be applicable for the SST interfaced LVDC distribution networks.

6.4 Chapter 6 Summary

This chapter has developed a fault let-through energy based fault location technique that can be applied successfully for LVDC fault location estimation. An analytical method has been presented for assessing the fault location estimation errors and the critical distance beyond which the error increases significantly. Based on the critical distance, the device of the more suitable end for the feeder is selected in order to minimize the estimation errors. Its high accuracy has been verified against different cable lengths with fault resistance less than 1Ω. For instance, studies have demonstrated an average error 0.6%, with a maximum 3.5m for a 500m feeder and 0.4% average error, 4.6m maximum error for a 1000m. The proposed critical point based working algorithm can reduce estimation errors up to 15m (3%) for a 1000m feeder compared to the existing 50% rule. The improved accuracy allows DC faults to be accurately located and facilitates rapid post-fault cable maintenance even where different converters are installed at each end of a feeder. The high reliability of using fault let-through energy to estimate LVDC fault distance has been validated and it has been found that it provides a good level of accuracy. For instance, average error 4.7% for a 500m feeder

and 2.54% for a 1000m feeder under a significantly noisy environment with SNR up to 20dB. This reduces the requirements of using complicated and expensive filters to achieve an acceptable level of fault location accuracy compared to the existing current derivative based technique. The enhanced accuracy and reliability of the proposed fault location technique enables wider implementations of LVDC distribution networks.

The work presented in this chapter is extended from a journal publication [190].

Chapter 7

Conclusions and Future Work

7.1 Summary

LV distribution networks are currently under pressure to host growing numbers of low carbon technologies. With the developments in power electronic technologies, increasing appliances inherently using DC, and the quantified energy saving and cost reduction of using LVDC, LVDC distribution has been proposed as an effective approach to release this pressure on hosting increasing numbers of low carbon technologies. However, selective fault protection and reliable and accurate fault location are the key outstanding LVDC technical challenges that have been reported by a number of research works and industrial groups. The work presented within this thesis covers a number of key issues related to fault protection and location of LVDC distribution networks.

In particular, the work considers the protection of an LVDC distribution network interfaced with advanced fault-tolerant converters such as solid-state transformers (SST). These are regarded as an emerging technology that is expected to ultimately replace conventional LV transformers. The unique fault behaviours of SST make the understandings of existing fault characteristics and protection solutions no longer suitable to guarantee the security of future LVDC networks especially for existing LV overcurrent protection solutions.

In addition, the integrations of renewables in future LVDC distribution networks will challenge the accuracy of fault distance estimations, while existing fault location

techniques are dramatically influenced by noise. These issues significantly compromise post-fault recovery such as network reconfiguration and cable section replacement.

To this end, this thesis presents a novel protection scheme and a novel fault location technique that enable wider implementations of LVDC distribution networks: (i) a voltage-based protection scheme that enhances the protection selectivity to effectively distinguish downstream and upstream internal and external faults, and (ii) a fault let-through energy based fault location technique that enhances accuracy and provides increased noise-tolerance. The performance of the proposed protection scheme and fault location technique have been verified by PSCAD/EMTDC simulations. The following sections outline the major conclusions of this research and identify areas of research worth being taken forward in future work.

7.2 Conclusions

The contributions from the work undertaken throughout this thesis can be attributed to the following distinct knowledge streams. The following three sub-sections present the contributions to each stream in detail.

7.2.1 Approach for Fault Characterisation and Protection Evaluation of Future LVDC Distribution Networks

Acknowledging the recently identified emerging transition to LVDC distribution in addition to the development of more advanced converter topologies, this thesis proposes a new approach for fault characterisation and protection evaluation of future LVDC distribution networks. The proposed approach is effective in understanding and quantifying the fault characteristic differences between LVDC distribution networks interfaced with new converters or with existing commonly-used two-level VSCs, as well as their impact on the performance of existing protection solutions.

The SST is selected in this thesis due to its unique fault characteristics, enhanced fault current control capabilities, great potential to replace existing LV transformer, and additional ancillary services (e.g. voltage and power control). Based on the proposed

approach, the impact of SST on the DC fault characteristics and existing protection performance has highlighted the following as reported in Chapter 4:

- The impact of an SST on DC fault response is in the steady state stage to the extent that it inherently limits the fault current which is less than 50% of the fault current of a two-level VSC;
- The DC fault current reduction of the SST can reduce the FLTE by up to 20% in 10ms and 40% in 100ms. This amount of reduction in the fault energy results in the overcurrent protection operation taking up to four times longer, increasing the challenge in using this method to coordinate the downstream protection within the required time window;
- Fast protection solutions (e.g. current derivative-based, voltage derivative-based, differential, and directional-based) that rely on DC fault transient period (i.e. capacitor discharge stage) will not significantly be influenced by the SST and can clear fault within 0.5ms;
- Communication-based protection solutions that require data synchronisation can lose protection discrimination when there is a communication time delay greater than 10μs;
- Current derivative based protection solutions are the most effective within the tested protection solutions to protect against high resistive fault up to 5Ω while ensuring high speed within 0.5ms;
- The test showed that noise levels of $\pm$0.3% in the current resulted errors of 85% in its derivatives. This shows that derivative-based protection solutions can easily lose fault protection and location capabilities in noisy environment;

7.2.2 A Voltage-based LVDC Protection Scheme with Enhanced Selectivity

To overcome the limitations of overcurrent protection for future SST interfaced LVDC distribution networks and follow the recommendations of future protection design, as

highlighted in Chapter 4, voltage-based protection solutions demonstrate a greater potential. This is because their performance is not affected by the limited fault currents provided by SST. However, based on the evaluations of existing voltage-based protection solutions, it was found that:

- Existing voltage-based protection solutions lack effective fault discrimination to distinguish downstream and upstream faults;
- It is difficult to select a protection setting that ensures a good level of selectivity especially against highly resistive faults;

To overcome these issues, a novel voltage based protection scheme that exhibits enhanced protection selectivity and stability especially for distinguishing resistive DC faults is proposed for LVDC distribution networks. The proposed protection scheme is communication-less, fast acting, fully discriminative, and incorporates a combination of the sign of current derivative, DC voltage magnitude, and DC voltage concavity (sign of d^2V/dt^2). In comparison to existing voltage-based protection, the proposed scheme has been shown to successfully discriminate faults up to three times higher fault resistance.

The performance of the proposed protection scheme is verified by simulations in PSCAD/EMTDC. To improve realism, the measurement signals were then superimposed with noise captured from a transducer in a laboratory setting. The simulation results have proven the viability of the developed protection scheme for reliably detecting and locating DC faults within a faulted LVDC network interfaced by an SST. The effective coordination between the SST and LVDC system protection is realised within 100μs. Such fast DC protection scheme performance allows DC faults to be interrupted at an early stage, leading to reduced short circuit stress on the system and fast DC power supply restoration in 2.5ms that improves the post-fault power quality and resilient LVDC network operation.

7.2.3 A Fault Let-through Energy-based LVDC Fault Location Technique with Enhanced Accuracy and Reliability

Besides the requirement for a protection scheme with improved selectivity, further practical challenges arise from the need for a more accurate and reliable DC fault location method for future LVDC distribution networks. The challenges identified were related to:

- Lack of sufficient understanding of the impact of different ratings of remote end converters on the accuracy of fault distance estimation;
- Low reliability against noise when using the current derivative to establish fault distance estimation.

Fault Let-Through Energy (FLTE) has been used as a parameter for LVAC protection especially in support of protection coordination. Due to the limited fault current in LVDC, the use of FLTE for protection coordination is less effective as reported in Chapter 4. However, it has been identified that it has the potential to be used as a more reliable fault location indicator that provides more accurate fault distance estimation and significantly mitigates the noise effect. To address the above issues, a novel FLTE-based fault location technique has been developed for LVDC distribution networks. The proposed fault location technique is successfully applied for LVDC fault location estimation. Meanwhile, an analytical method has been established for assessing the fault location estimation errors and the critical distance beyond which the error increases significantly. This allows for the selection of the most suitable location device for a given feeder based on the critical distance.

The high accuracy of the proposed fault location technique has been verified in simulations involving different cable lengths with fault resistance less than 1Ω. For instance, the study has demonstrated an average error 0.6%, with a maximum 3.5m for a 500m feeder and 0.4% average error, 4.6m maximum error for a 1000m. The proposed critical point based working algorithm can reduce estimation errors up to 15m (3%) for a 1000m feeder compared to the most of the proposed fault location strategies

(i.e. using local side device to estimate the first half of the feeder, and remote side device to estimate the remaining half of the feeder). The improved accuracy allows DC faults to be accurately located and facilitates rapid post-fault cable maintenance even where different converters are installed at each end of a feeder. The high immunity and reliability of using fault let-through energy to estimate LVDC fault distance has been verified in simulations where a good level of accuracy was achieved even in a noisy environment. For instance, 4.7% for a 500m feeder and 2.54% for a 1000m feeder have been achieved in fault distance estimations in a significant noisy environment with SNR up to 20dB. The highlighted noise-tolerant capabilities of FLTE-based fault location technique reduces the requirements of using complicated and expensive filters to achieve an acceptable level of fault location accuracy compared with the existing current derivative-based technique.

7.3 Future Work

Based on the findings and conclusions of the accomplished work, potential areas of future work have been identified and are presented in the following sub-sections, which can further enhance the security and reliability of LVDC operations.

7.3.1 Improving Technology Readiness Levels of the Proposed Techniques

The effectiveness of the proposed fault protection scheme and fault location technique has been proven in PSCAD/EMTDC simulations. However, it is worth validating these techniques in a laboratory environment to test their performance and help overcome potential issues that may adversely impact their deployment in practical LVDC distribution networks. The key objective of the laboratory-based validation experiments of the proposed protection scheme and fault location technique is to identify the effectiveness and accuracy of the hardware-based data acquisition in terms of the measurements of current derivative, voltage, voltage concavity, and fault let-through energy during the fast DC fault transient period.

7.3.2 Developing a Coordinated Control and Protection Scheme for Hybrid AC and DC Distribution Networks Interfacing SSTs

SST is an emerging converter technology that can provide MVDC, LVDC, and LVAC power supplies. Hence, it is worth investigating the interaction between LVDC and LVAC. The interaction between the control and protection of the SST interfaced LVAC distribution network maybe not be significant as the available time window in LVAC is longer than in LVDC. However, for LVDC systems, faults that happen on the LVAC side may cause problems with respect to the coordination between protection and control systems. The miscoordination of protection and control may lead to cascading events that could significantly influence SST interfaced networks.

7.3.3 Validating and Improving the Proposed Techniques in the Other Converters Interfaced LVDC Distribution Networks

SST is an emerging technology that has great potential to be implemented in the future LV distribution networks. However, other advanced converters such as modular multi-level converters (MMC) have been proposed in the literature. As reported in Chapter 2, MMCs have lower fault energy and a smaller time window for protection to operate than SSTs. It is necessary to investigate the effectiveness of the proposed methods in the other modern converter topologies that interface with LVDC distribution networks to test and improve their compatibilities.

Appendix A

PSCAD model of the LVDC test network

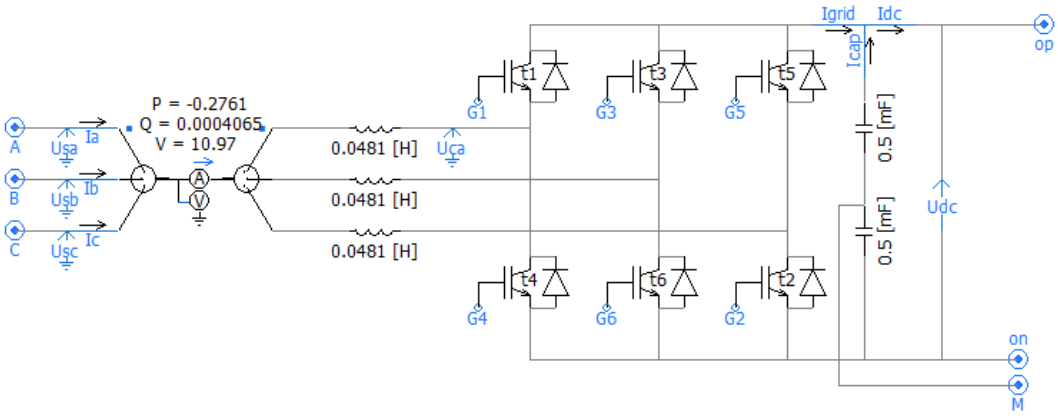

Figure A.1: Layout of the AC/DC converter of the two-stage SST

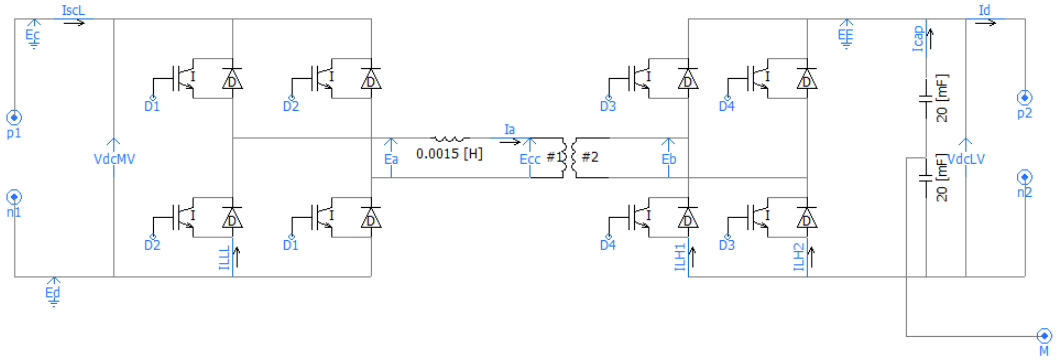

Figure A.2: Layout of the DAB converter of the two-stage SST

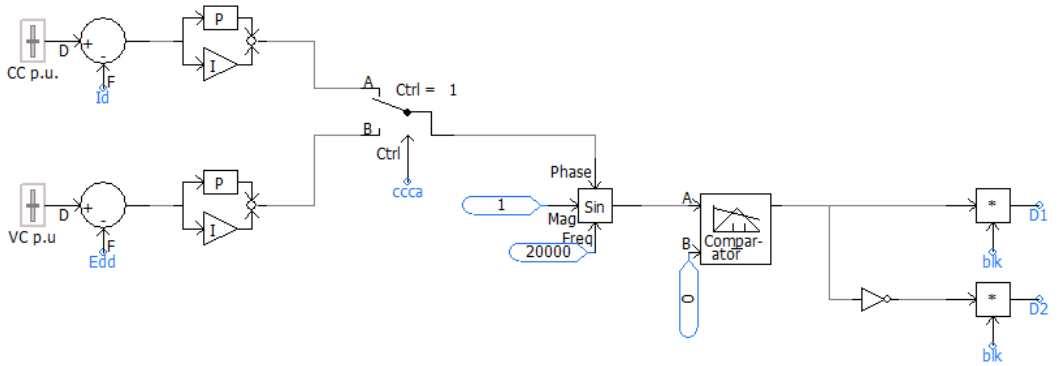

Figure A.3: Layout of the primary bridge control of DAB converter

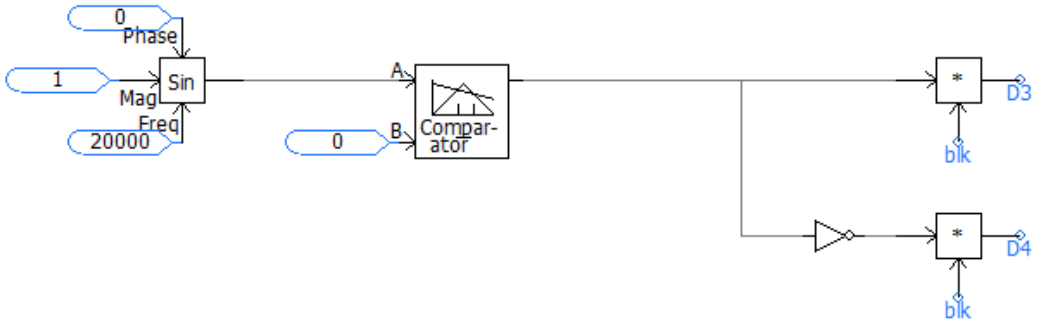

Figure A.4: Layout of the secondary bridge control of DAB converter

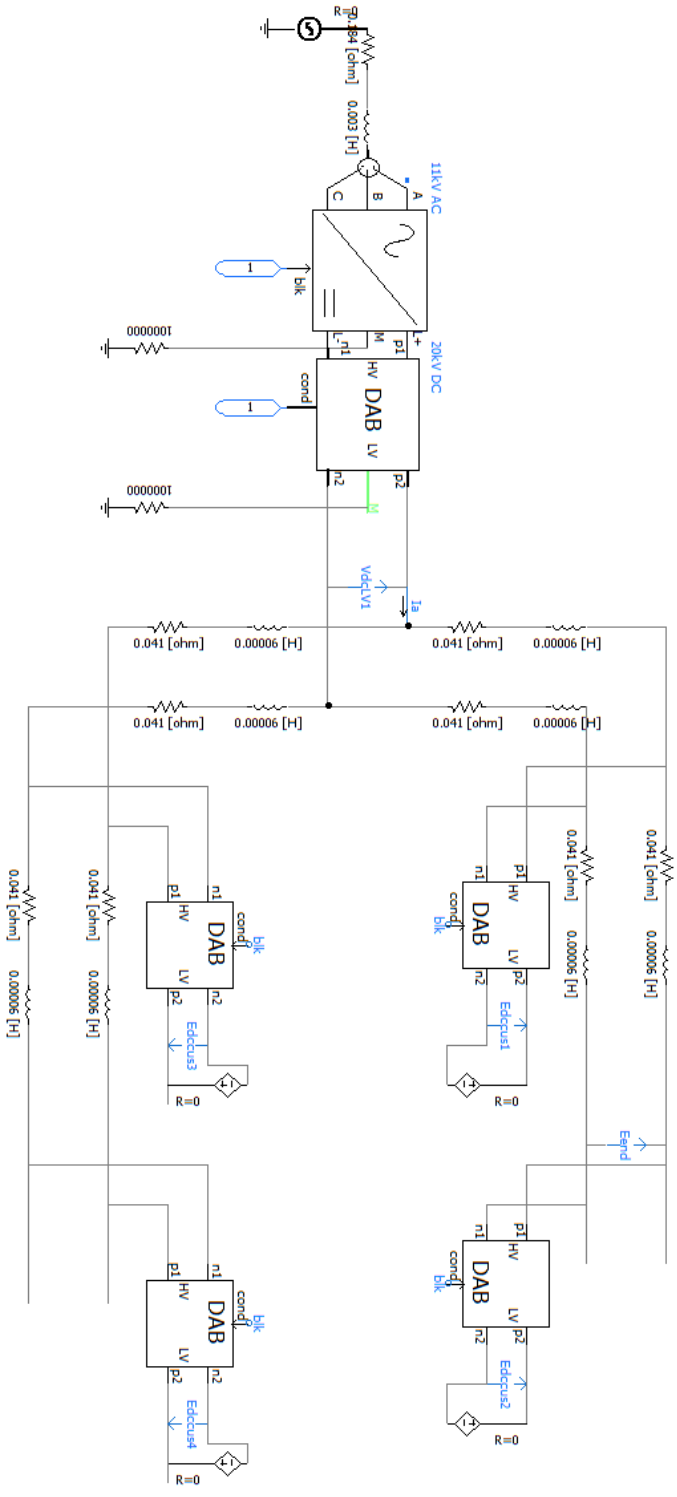

Figure A.5: Layout of an SST interfaced LVDC test network

Table A.1: Parameters of the used test network models

Parameter	**Value**
AC supply	11kV
Fault level	174MVA
SST capacity	1MVA
SST DAB	20kV DC/±750V DC, switching frequency 20kHz, LV smoothing capacitor 10mF, choke inductor 1.52mH
MVDC voltage	20kV (pole-to-pole)
LVDC voltage	±750V (pole-to-pole)
LVDC cables	0.164ohm/km, 0.00024H.km, 250 each section
DC customers	200kW each
Local DC source	380V
Assistive inductors	0.011mH for each pole
Two-level VSC	Choke inductor 0.88mH, filter capacitor 10mF, switching frequency 2kHz, DC voltage +/-750V
Local DAB converter	±750V DC/±190V, switching frequency 20kHz, auxiliary inductor 0.052mH, filter capacitor 5mF

Appendix B

PSCAD model of the proposed fault protection scheme

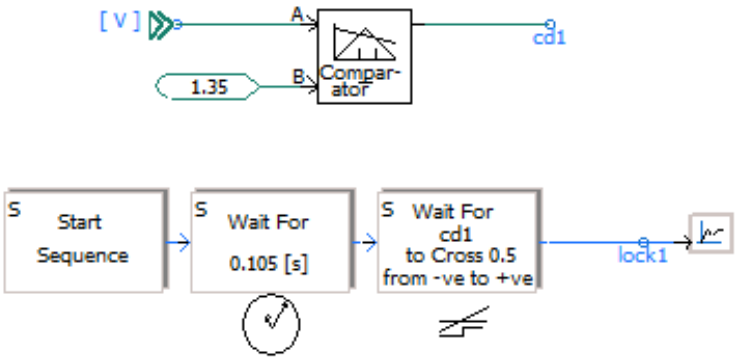

Figure B.1: Layout of fault detection of the proposed protection scheme

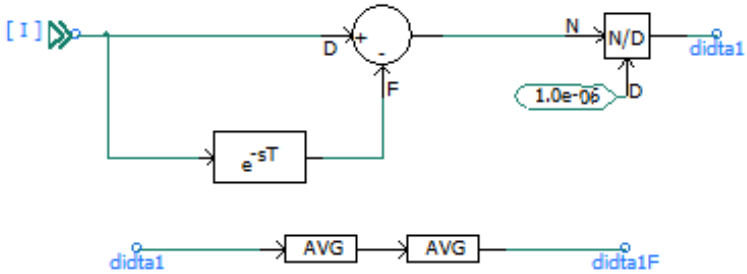

Figure B.2: Layout of fault discrimination of the proposed protection scheme-Part.1

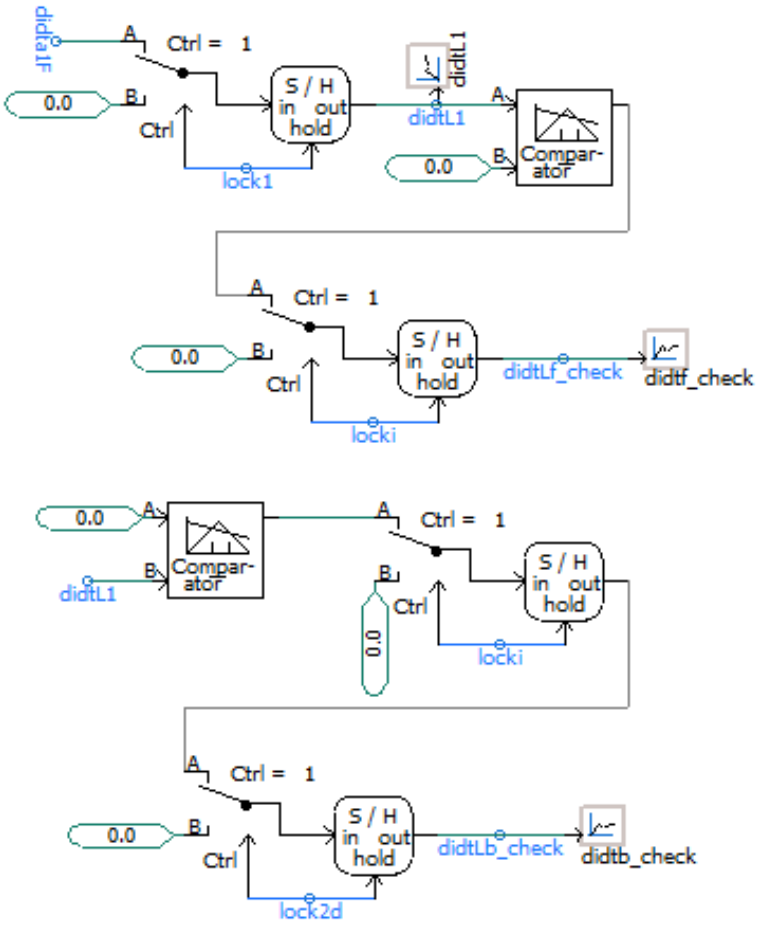

Figure B.3: Layout of fault discrimination of the proposed protection scheme-Part.2

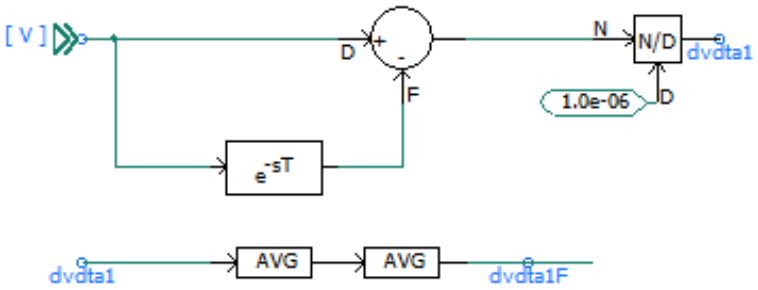

Figure B.4: Layout of fault discrimination of the proposed protection scheme-Part.3

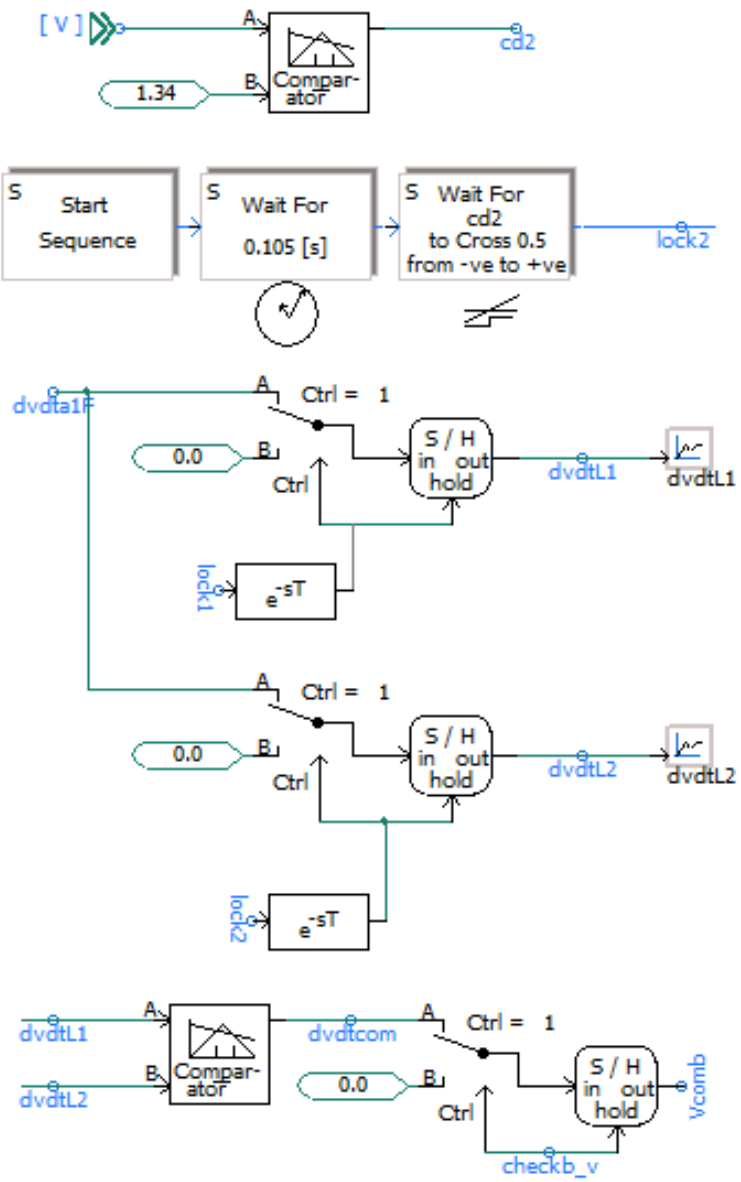

Figure B.5: Layout of fault discrimination of the proposed protection scheme-Part.4

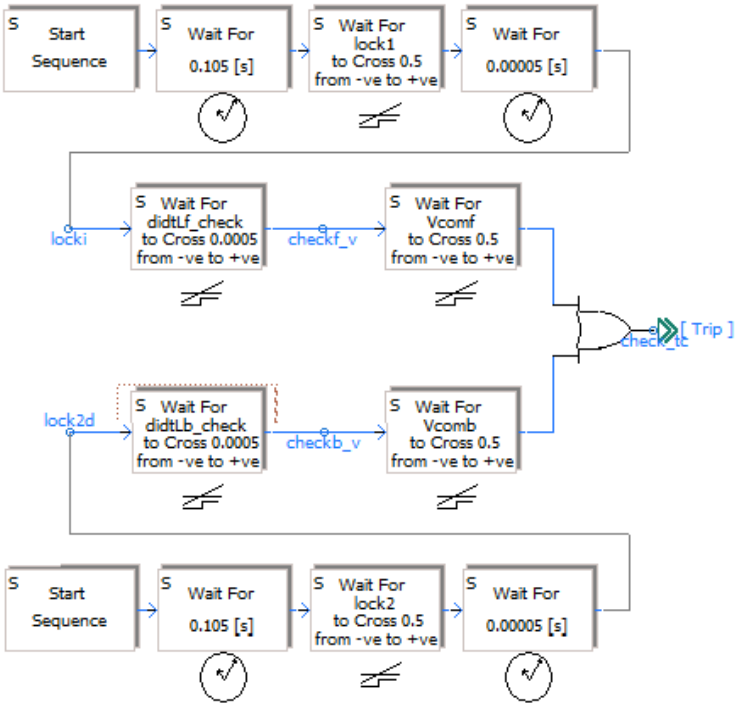

Figure B.6: Layout of fault discrimination of the proposed protection scheme-Part.5

Appendix C

PSCAD model of the proposed fault location technique

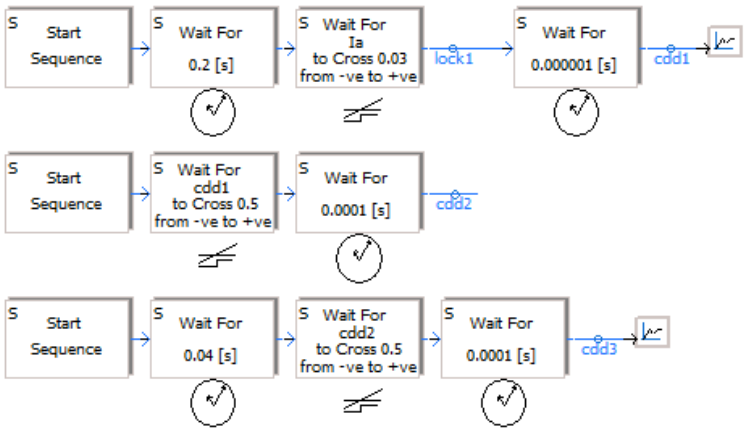

Figure C.1: Layout of time window selection of the proposed fault location technique

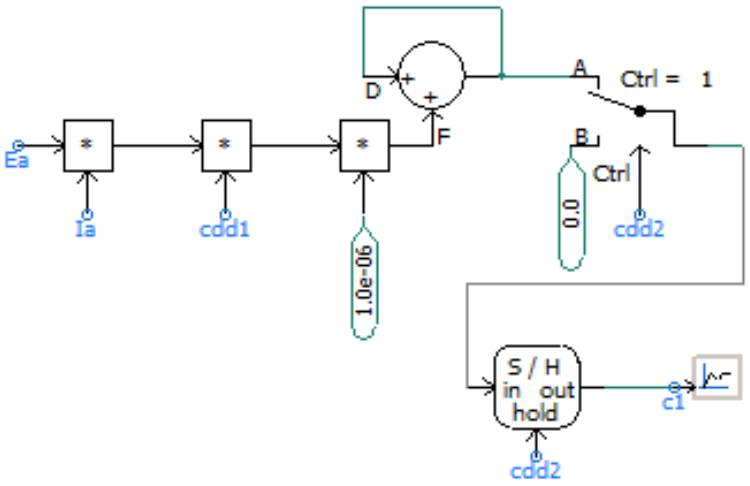

Figure C.2: Layout of parameter calculation of the proposed fault location technique-Part.1

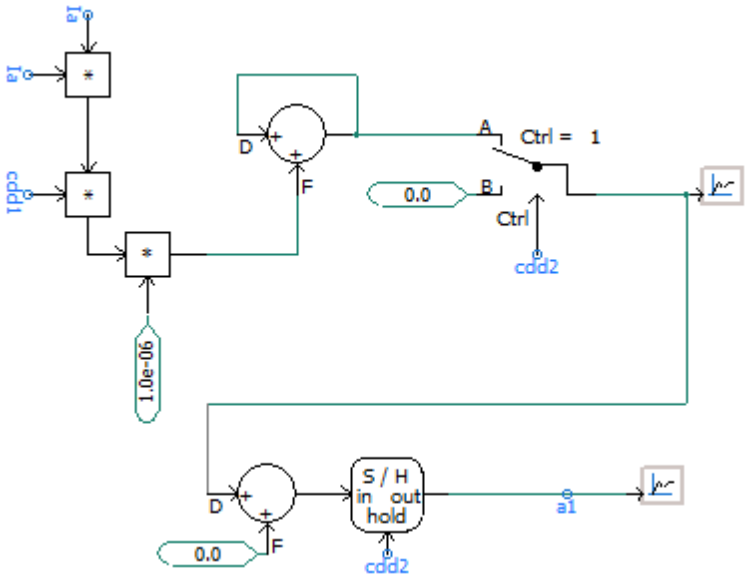

Figure C.3: Layout of parameter calculation of the proposed fault location technique-Part.2

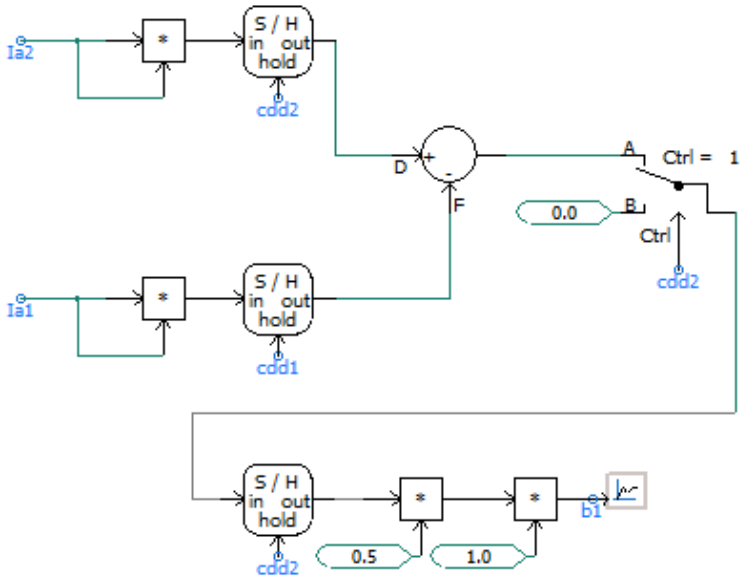

Figure C.4: Layout of parameter calculation of the proposed fault location technique-Part.3

Bibliography

[1] N. Iwamuro and T. Laska, "IGBT History, State-of-the-Art, and Future Prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 741–752, 2017.

[2] A. Emhemed, D Wang, G. Burt, J. Zafar, A. Kazerooni, and A. Donoghue, "Multi-zone LVDC Distribution Systems Architecture for Facilitating Low Carbon Technologies Uptake," in *15th IET ACDC*, 2019.

[3] K. Smith, D. Wang, A. Emhemed, S. Galloway, and G. Burt, "Overview Paper on: Low Voltage Direct Current Distribution System Standards," *Int. J. Power Electron.*, vol. 9, no. 3, pp. 1–24, 2017.

[4] IEC, "LVDC: electricity for the 21st century," 2017. [Online]. Available: https://www.iec.ch/technologyreport/lvdc/. [Accessed: 20-Nov-2019].

[5] D. Wang, A. Emhemed, P. Norman, and G. Burt, "Evaluation of Existing DC Protection Solutions on the Performance of an Active LVDC Distribution Network under Different Fault Conditions," in *CIRED - Open Access Proceedings Journal 2017*, 2017.

[6] SP Energy Networks, "2017 Network Innovation Competition Proposal," 2017. [Online]. Available: https://www.spenergynetworks.co.uk.

[7] C. Kumar and B. Klein, "How the UK can lead the electric vehicle revolution," Green Alliance, 2018. [Online]. Available: http://www.green-alliance.org.uk. [Accessed: 03-Dec-2019].

[8] National Grid, "Future Energy Scenarios 2019," 2019.

[9] C. Cluzel and H.-M. Alastair, "Transport Energy Infrastructure Roadmap to 2050," 2015.

[10] V. Vossos, K. Johnson, M. Kloss, M. Khattar, D. Gerber, and R. Brown, "Review of DC Power Distribution in Buildings: A Technology and Market Assessment," 2017.

[11] LAMARCHE, "Telecom DC Power Systems." [Online]. Available: https://www.lamarchemfg.com/. [Accessed: 08-Dec-2019].

[12] G. Allee and W. Tschudi, "Edison Redux: 380 Vdc Brings Reliability and Efficiency to Sustainable Data Centers," *IEEE Power Energy Mag.*, vol. 10, no. 6, pp. 50–59, 2012.

[13] ABB, "The Step Forward Onboard DC Grid," 2014. [Online]. Available: new.abb.com. [Accessed: 08-Dec-2019].

[14] TOSHIBA, "Traction and Auxiliary Power Systems," 2014. [Online]. Available: https://www.toshiba.co.jp/. [Accessed: 08-Dec-2019].

[15] ABB, "ABB Solar Coupled with Energy Storage-A Wide Variety of Choices." [Online]. Available: https://library.abb.com/en. [Accessed: 04-Dec-2019].

[16] Warmfloor, "A Unique Heating System," 2016. [Online]. Available: http://www.warmfloor.com. [Accessed: 08-Dec-2019].

[17] Hotspot Energy, "Solar / DC Air Conditioner," 2016. [Online]. Available: www.hotspotenergy.com. [Accessed: 08-Dec-2019].

[18] Phocos, "DC Chest Refrigerator/Freezer," 2019. [Online]. Available: http://www.phocos.com. [Accessed: 08-Dec-2019].

[19] Nuleds, "SPICEbox- NuLEDs - Intelligent LED Lighting." [Online]. Available: https://www.nuleds.com/. [Accessed: 19-Nov-2019].

[20] Navigant, "Adoption of Light-Emitting Diodes in Common Lighting Applications," 2017. [Online]. Available: https://www.energy.gov/. [Accessed: 08-Dec-2019].

[21] IET, "Code of Practice for the Application of LED Lighting Systems," 2014.

[22] A. Genovese, F. Ortenzi, and C. Villante, "On the Energy Efficiency of Quick DC Vehicle Battery Charging," *World Electr. Veh. J.*, vol. 7, no. 4, pp. 570–576, 2015.

[23] "Compare Hybrid and Electric Vehicles - EV Database UK." [Online]. Available: https://ev-database.uk/. [Accessed: 19-Nov-2019].

[24] "Pulse QC50." [Online]. Available: www.rapidonline.com. [Accessed: 19-Nov-2019].

[25] E. Rodriguez-Diaz, F. Chen, J. C. Vasquez, J. M. Guerrero, R. Burgos, and D. Boroyevich, "Voltage-Level Selection of Future Two-Level LVdc Distribution Grids: A Compromise between Grid Compatibility, Safety, and Efficiency," *IEEE Electrif. Mag.*, vol. 4, no. 2, pp. 20–28, 2016.

[26] T. Kaipia et al., "Survey of Market Prospects and Standardisation Development needs of LVDC Technology," *CIRED - Open Access Proc. J.*, 2017

[27] V. Vossos, K. Garbesi, and H. Shen, "Energy Savings from Direct-DC in U.S. Residential Buildings," *Energy Build.*, vol. 68, pp. 223–231, 2014.

[28] B. A. Thomas, I. L. Azevedo, and G. Morgan, "Edison Revisited: Should we use DC circuits for lighting in commercial buildings?," *Energy Policy*, vol. 45, pp. 399–411, 2012.

[29] J. Karppanen, T. Kaipia, P. Nuutinen, A. Mattsson, A. Lana, A. Pinomaa, P. Peltoniemi, J. Partanen, T. Hakala, and T. Lähdeaho, "Comparison of Lvdc Distribution Network Alternatives: Full-Dc Vs. Link-Type Solutions," in *CIRED 2017*, 2017.

[30] IEC, "IEC 60038: IEC standard voltages," 2009.

[31] T. Hakala, P. Virtanen, and T. Kasteenpohja, "LVDC RULES – Towards Industrial-Scale Application of Low-Voltage Direct Current in Public Power Distribution," in *CIRED Workshop*, 2016.

[32] P. Nuutinen, T. Kaipia, P. Peltoniemi, A. Lana, A. Pinomaa, A. Mattsson, P. Silventoinen, J. Partanen, J. Lohjala, and M. Matikainen, "Research Site for Low-Voltage Direct Current Distribution in a Utility Network-Structure, Functions, and Operation," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2574–2582, 2014.

[33] T. Hakala, T. Lähdeaho, and R. Komsi, "LVDC Pilot Implementation in Public Distribution Network," in *CIRED 2015*, 2015.

[34] P. Nuutinen, T. Kaipia, J. Karppanen, A. Mattsson, A. Lana, A. Pinomaa, P. Peltoniemi, J. Partanen, M. Luukkanen, and T. Hakala, "LVDC Rules-Technical Specifications for Public LVDC Distribution Network," *CIRED - Open Access Proc. J.*, 2017.

[35] P. Nuutinen, "Power Electronic Converters in Low Voltage Direct Current Distribution-Analysis and Implementation," *thesis*, Lappeenranta University of Technology, 2015.

[36] "LVDC Rules-LVDC Projects-LUT." [Online]. Available: https://www.lut.fi. [Accessed: 21-Nov-2019].

[37] "DC Systems-Innovative Smart DC Systems for Utility Buildings, Offices, Public and Commercial Areas." [Online]. Available: https://dc.systems/index.php. [Accessed: 22-Nov-2019].

[38] Y. Cho, H. J. Kim, J. Kim, J. Cho, and J. Kim, "Construction of Actual LVDC Distribution Line," *CIRED - Open Access Proc. J.*, 2017.

[39] Y. Cho, J. Kim, J. Cho, and J. Kim, "Design and Construction of LVDC Distribution Site," in *CIRED Workshop*, 2016.

[40] H. Kim, Y. Cho, J. Kim, J. Cho, and J. Kim, "Demonstration of LVDC Distribution System in Island," in *CIRED 2017*, 2017.

[41] "Assessment of Standard Voltages and Power Quality Requirement for LVDC Electricity Supply Systems," 2018. [Online]. Available: https://www.nen.nl/web/file?uuid=9cca4c12-3ab9-4fa7-bfaa-cbbbe5a13d48&owner=f7d5c30e-931f-476e-bb88-d8a47e8b308a. [Accessed: 25-Nov-2019].

[42] "Developments of DC Transmission & Distribution Technology in China." [Online]. Available: https://www.nedo.go.jp/content/100893755.pdf. [Accessed: 25-Nov-2019].

[43] Y. Zhong, N. Roscoe, D. Holliday, T. C. Lim, and S. J. Finney, "High-Efficiency mosfet-Based MMC Design for LVDC Distribution Systems," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 321–334, 2018.

[44] G. Adam, *Voltage Source Converter: modulation, control and applications in power systems*, https://www.createspace.com, 2013.

[45] E. R. Diaz, X. Su, M. Savaghebi, J. C. Vasquez, M. Han, and J. M. Guerrero, "Intelligent DC Microgrid Living Laboratories - A Chinese-Danish Cooperation Project," in *ICDCM 2015*, 2015.

[46] H. A. Mantooth, Y. Liu, C. Farnell, F. Zhang, Q. Li, and J. Di, "Securing DC and Hybrid Microgrids," in *ICDCM 2015*, 2015.

[47] S. Rivera, B. Wu, S. Kouro, V. Yaramasu, and J. Wang, "Electric Vehicle Charging Station Using a Neutral Point Clamped Converter with Bipolar DC Bus," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 1999–2009, 2015.

[48] L. Tan, B. Wu, S. Rivera, and V. Yaramasu, "Comprehensive DC Power Balance Management in High-Power Three-Level DC-DC Converter for Electric Vehicle Fast Charging," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 89–100, 2016.

[49] J. Cho, J. Kim, H. Lee, and J. Kim, "Design and Construction of Korean LVDC Distribution System for Supplying DC Power to Customer," in *CIRED 2015*, 2015.

[50] D. Wang, A. Emhemed, G. Burt, and P. Norman, "Fault Analysis of an Active LVDC Distribution Network for Utility Applications," in *UPEC 2016*, 2016.

[51] M. M. Steurer, S. Member, K. Schoder, O. Faruque, S. Member, D. Soto, M. Bosworth, M. Sloderbeck, F. Bogdan, J. Hauer, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional Megawatt-Scale Medium Voltage DC Test Bed Based on Modular Multilevel Converter Technology," *IEEE Trans. Transp. Electrif.*, vol. 2, no. 4, pp. 597–606, 2016.

[52] A. Ghazanfari and Y. A. R. I. Mohamed, "A Decentralized Control Strategy with dc Fault Handling Capability for Smart dc Buildings," in *APEC*, 2017.

[53] M. A. Khan, A. Ahmed, I. Husain, Y. Sozer, and M. Badawy, "Performance Analysis of Bidirectional DC-DC Converters for Electric Vehicles," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3442–3452, 2015.

[54] B. Sri Revathi and M. Prabhakar, "Non Isolated High Gain DC-DC Converter Topologies for PV Applications – A Comprehensive Review," *Renew. Sustain. Energy Rev.*, vol. 66, pp. 920–933, 2016.

[55] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-Up DC-DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, 2017.

[56] Z. Zhou, H. Li, and X. Wu, "A Constant Frequency ZVS Control System for the Four-Switch Buck-Boost DC-DC Converter with Reduced Inductor Current," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 5996–6003, 2019.

[57] R. W. De Doncker, "Power Electronic Technologies for Flexible DC Distribution Grids," in *IPEC*, 2014.

[58] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized Operation of Current-Fed Dual Active Bridge DC-DC Converter for PV Applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, 2015.

[59] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, 2014.

[60] A. Mattsson, V. Vaisanen, P. Nuutinen, P. Peltoniemi, T. Kaipia, P. Silventoinen, and J. Partanen, "Evaluation of Isolated Converter Topologies for Low voltage DC Distribution," in *IECON 2015*, 2015.

[61] M. I. Rahman, K. H. Ahmed, and D. Jovcic, "Analysis of DC Fault for Dual-Active Bridge DC/DC Converter Including Prototype Verification," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 2, pp. 1107–1115, 2019.

[62] M. A. Hannan, P. J. Ker, M. S. H. LIPU, and *et al.*, "State of the Art of Solid-State Transformers: Advanced Topologies, Implementation Issues, Recent Progress and Improvements," *IEEE Access*, vol. 8, pp. 19113–19132, 2020.

[63] SP Energy Networks, "LV Engine-A Smarter Electricity Network," 2018. [Online]. Available: https://www.spenergynetworks.co.uk/.

[64] A. Emhemed, *et al.*, "Protection and Earthing Requirements of LV AC and DC Distribution Networks Interfaced by Smart Transformers," in *CIRED 2019*, 2019.

[65] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 1, no. 3, pp. 186–198, 2013.

[66] H. Qin, "Dual active bridge converters in solid state transformers," *thesis*, Missouri University Of Science and Technology, 2012.

[67] Alstom Grid, *Network Protection & Automation Guide*, 2011.

[68] IEEE Std C37.112-2018, "IEEE Standard for Inverse- Time Characteristics Equations for Overcurrent Relays," 2018.

[69] P. Hu, "Design and Specification for Safe and Reliable Battery Systems for Large UPS." [Online]. Available: https://it-resource.schneider-electric.com/. [Accessed: 28-Nov-2019].

[70] BS EN 50123-7-1:2003, "Railway Applications — Fixed Installations —D.C. Switchgear — Part 7-1: Measurement, Control and Proteciton Devices for Specific Use in d.c. Traction Systems — Application Guide," 2003.

[71] BS IEC 62548:2016, "Photovoltaic (PV) Arrays — Design Requirements," 2016.

[72] BS IEC 60092-201:2019, "Electrical Installations in Ships Part 201: System Design-General," 2019.

[73] M. E. Baran and N. R. Mahajan, "Overcurrent Protection on Voltage-Source-Converter-based Multiterminal DC Distribution Systems," *IEEE Trans. Power Deliv.*, vol. 22, no. 1, pp. 406–412, 2007.

[74] S. Fletcher, P. Norman, and G. Burt, "Fault Detection and Location in DC Systems from Initial di/dt Measurement," in *Euro Tech Con Conference*, 2012.

[75] A. Meghwani, S. C. Srivastava, and S. Chakrabarti, "A Non-unit Protection Scheme for DC Microgrid Based on Local Measurements," *IEEE Trans. Power Deliv.*, vol. 32, no. 1, pp. 172–181, 2017.

[76] X. Feng, L. Qi, and J. Pan, "A Novel Fault Location Method and Algorithm for DC Distribution Protection," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 1834–1840, 2017.

[77] J. Yang, J. E. Fletcher, and J. O'Reilly, "Multiterminal DC Wind Farm Collection Grid Internal Fault Analysis and Protection Design," *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 2308–2318, 2010.

[78] W. Leterme, J. Beerten, and D. Hertem, "Nonunit Protection of HVDC Grids with Inductive DC Cable Termination," *IEEE Trans. Power Deliv.*, vol. 31, no. 2, pp. 820–828, 2016.

[79] P. Cairoli, I. Kondratiev, and R. A. Dougal, "Coordinated Control of the Bus Tie Switches and Power Supply Converters for Fault Protection in DC Microgrids," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2037–2047, 2013.

[80] K. Jia, T. Bi, B. Liu, E. Christopher, D. W. P. Thomas, and M. Sumner, "Marine Power Distribution System Fault Location Using a Portable Injection Unit," *IEEE Trans. Power Deliv.*, vol. 30, no. 2, pp. 818–826, 2015.

[81] K. A. Saleh, A. Hooshyar, and E. F. El-Saadany, "Hybrid Passive-Overcurrent Relay for Detection of Faults in Low-Voltage DC Grids," *IEEE Trans. Smart Grid*, vol. 8, no. 3, pp. 1129–1138, 2017.

[82] W. Li, A. Monti, and F. Ponci, "Fault Detection and Classification in Medium Voltage dc Shipboard Power Systems with Wavelets and Artificial Neural Networks," *IEEE Trans. Instrum. Meas.*, vol. 63, no. 11, pp. 2651–2665, 2014.

[83] D. K. J. S. Jayamaha, N. W. A. Lidula, and A. D. Rajapakse, "Wavelet-Multi Resolution Analysis Based ANN Architecture for Fault Detection and Localization in DC Microgrids," *IEEE Access*, vol. 7, pp. 145371–145384, 2019.

[84] S. Som and S. R. Samantaray, "Efficient Protection Scheme for Low-Voltage DC Micro-Grid," *IET Gener. Transm. Distrib.*, vol. 12, no. 13, pp. 3322–3329, 2018.

[85] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids - Part II: A Review of Power Architectures, Applications, and Standardization Issues," *IEEE Transactions on Power Electronics*, vol. 31, no. 5. pp. 3528–3549, 2016.

[86] S. Fletcher, P. Norman, K. Fong, S. Galloway, and G. Burt, "High-Speed Differential Protection for Smart DC Distribution Systems," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2610–2617, 2014.

[87] A. Emhemed, K. Fong, S. Fletcher, and G. Burt, "Validation of Fast and Selective Protection Scheme for an LVDC Distribution Network," *IEEE Trans. Power Deliv.*, vol. 32, no. 3, pp. 1432–1440, 2017.

[88] J. Do Park, "Ground Fault Detection and Location for Ungrounded DC Traction Power Systems," *IEEE Trans. Veh. Technol.*, vol. 64, no. 12, pp. 5667–5676, 2015.

[89] R. Mohanty, U. S. M. Balaji, and A. K. Pradhan, "An Accurate Noniterative Fault-Location Technique for Low-Voltage DC Microgrid," *IEEE Trans. Power Deliv.*, vol. 31, no. 2, pp. 475–481, 2016.

[90] L. Zhang, N. Tai, W. Huang, and Y. Wang, "Fault Distance Estimation-based Protection Scheme for DC Microgrids," *J. Eng.*, vol. 2019, no. 16, pp. 1199-1203, 2018.

[91] K. Jia, M. Li, T. Bi, and Q. Yang, "A Voltage Resonance-based Single-Ended Online Fault Location Algorithm for DC Distribution Networks," *Sci. China Technol. Sci.*, vol. 59, no. 5, pp. 721–729, 2016.

[92] A. Meghwani, S. C. Srivastava, and S. Chakrabarti, "Local Measurement-based Technique for Estimating Fault Location in Multi-Source DC Microgrids," *IET Gener. Transm. Distrib.*, vol. 12, no. 13, pp. 3305–3313, 2018.

[93] X. Feng, Q. Xiong, D. Wardell, A. Gattozzi, S. Strank, and R. Hebner, "Converter-based DC Distribution System Protection," in *2018 IEEE Industry Applications Society Annual Meeting (IAS)*, 2018.

[94] Tamura-Europe LTD, "Current Sensors." [Online]. Available: http://www.tamura-europe.co.uk. [Accessed: 23-Nov-2020].

[95] Honeywell, "Closed Loop Current Sensors." [Online]. Available: https://sensing.honeywell.com/. [Accessed: 23-Nov-2020].

[96] Powerguru, "Transducers Based on Fluxgate Technologies." [Online]. Available: http://www.powerguru.org/transducers-based-on-fluxgate-technologies/. [Accessed: 23-Nov-2020].

[97] P. Ripka, "Electric current sensors: a review," *Meas. Sci. Technol.*, vol. 21, no. 11, 2010.

[98] Sensitec GmbH, "MR sensor technology." [Online]. Available: http://www.sensitec.com. [Accessed: 23-Nov-2020].

[99] K. Dinesh, F. Zare, and G. Arindam, "DC Microgrid Technology: System Architectures, AC Grid Interfaces, Grounding Schemes, Power Quality, Communication Networks, Applications, and Standardizations Aspects," *IEEE Access*, vol. 5, pp. 12230–12256, 2017.

[100] N. Bayati, A. Hajizadeh, and M. Soltani, "Protection in DC Microgrids: A Comparative Review," *IET Smart Grid*, vol. 1, no. 3, pp. 66–75, 2018.

[101] R. Ouaida, J. F. De Palma, and G. Gonthier, "Hybrid Protection based on Pyroswitch and Fuse Technologies for DC Applications," in *Symposium de Genie Electrique*, 2016.

[102] ABB, "E90 Range of Fuse Disconnectors and Fuseholders." [Online]. Available: https://new.abb.com/. [Accessed: 02-Dec-2019].

[103] EATON, "Fuseology-Overcurrent Protection Fundamentals," 2017. [Online]. Available: http://www.cooperindustries.com/content/public/en/bussmann.html. [Accessed: 02-Dec-2019].

[104] ABB, "Technical Application Papers No.5 ABB Circuit-Breakers for Direct Current Applications," 2011. [Online]. Available: https://new.abb.com/. [Accessed: 02-Dec-2019].

[105] EATON, "Molded Case Circuit Breakers," 2017. [Online]. Available: https://www.eaton.com/. [Accessed: 09-Dec-2019].

[106] D. P. Urciuoli, D. Ibitayo, G. Koebke, G. Ovrebo, and R. Green, "A Compact 100-A, 850-V, Silicon Carbide Solid-State DC Circuit Breaker," in *ECCE 2016*, 2016.

[107] ABB, "Ultra-Fast High Current DC Breaker Innovates Marine Applications and Beyond," 2019. [Online]. Available: https://new.abb.com/news/detail/26578/ultra-fast-high-current-dc-breaker-innovates-marine-applications-and-beyond. [Accessed: 03-Dec-2019].

[108] Z. J. Shen, Z. Miao, and A. M. Roshandeh, "Solid State Circuit Breakers for DC Micrgrids: Current Status and Future Trends," in *ICDCM 2015*, 2015.

[109] L. Mackay, N. Blij, L. Ramirez-Elizondo, and P. Bauer, "Toward the Universal DC Distribution System," *Electr. Power Components Syst.*, vol. 45, no. 10, pp. 1032–1042, 2017.

[110] N. Tleis, Power Systems Modelling and Fault Analysis: Theory and Practice, *Elsevier*, 2007.

[111] BS EN 61660-1, "Short-Circuit Currents in d.c Auxiliary Installations in Power Plants and Substations - Part 1: Calculation of Short-Circuit Currents," 2000.

[112] A. Emhemed and G. Burt, "The Effectiveness of Using IEC61660 for Characterising Short-Circuit Currents of Future Low Voltage DC Distribution Networks," in *CIRED 2013*, 2013.

[113] ABB, "Technical Application Papers No.14 Faults in LVDC Microgrids with Front-End Converters," 2015. [Online]. Available: https://library.e.abb.com. [Accessed: 14-Dec-2019].

[114] S. Fletcher, P. Norman, S. Galloway, and G. Burt, "Analysis of the Effectiveness of Non-Unit Protection Methods within DC Microgrids," in *IET Conference on Renewable Power Generation 2011*, 2011.

[115] S. Fletcher, P. Norman, S. Galloway, P. Crolla, and G. Burt, "Optimizing the Roles of Unit and Non-Unit Protection Methods within DC Microgrids," *IEEE Trans. Smart Grid*, vol. 3, no. 4, pp. 2079–2087, 2012.

[116] W. Javed, D. Chen, M. E. Farrag, and Y. Xu, "System Configuration, Fault Detection, Location, Isolation and Restoration: A Review on LVDC Microgrid Protections," *Energies*, vol. 12, no. 6, p. 1001, 2019.

[117] A. Emhemed and G. Burt, "An Advanced Protection Scheme for Enabling an LVDC Last Mile Distribution Network," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2602–2609, 2014.

[118] SP Energy Networks, "Distribution Long Term Development Statement for the years 2017/2018 to 2021/22," 2017.

[119] J. Karppanen, T. Kaipia, P. Nuutinen, A. Lana, P. Peltoniemi, A. Pinomaa, A. Mattsson, J. Partanen, A. Pinomaa, C. Jintae, and K. Jaehan, "Effect of Voltage Level Selection on Earthing and Protection of LVDC Distribution Systems," in *11^{th} IET ACDC*, 2015.

[120] T. Hakala, T. Lahdeaho, and P. Jarventausta, "Low-Voltage DC Distribution-Utilization Potential in a Large Distribution Network Company," *IEEE Trans. Power Deliv.*, vol. 30, no. 4, pp. 1694–1701, 2015.

[121] BS IEC 60092-101:2018, "Electrical Installations in Ships, Part 101: Definitions and General Requirements," 2018.

[122] SP Energy Networks, "Smart Transformer Technical Specifications," 2018 [Internal project document].

[123] P. K. Goel, B. Singh, S. S. Murthy, and N. Kishore, "Isolated Wind-Hydro Hybrid System Using Cage Generators and Battery Storage," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1141–1153, 2011.

[124] M. Liserre, F. Blaabjerg, and A. Dell'aquila, "Step-by-Step Design Procedure for a Grid-Connected Three-Phase PWM Voltage Source Converter," *Int. J. Electron.*, vol. 91, no. 8, pp. 445–460, 2004.

[125] A. Sangwongwanich, A. Abdelhakim, Y. Yang, and K. Zhou, *Control of Single-Phase and Three-Phase DC/AC Converters*, *Academic Press*, 2018.

[126] J. E. Huber, D. Rothmund, and J. W. Kolar, "Comparative Evaluation of Isolated Front End and Isolated Back End Multi-Cell SSTs," in *IPEMC-ECCE Asia 2016*, 2016.

[127] L. Qu, Z. Yu, Q. Song, Z. Yuan, B. Zhao, D. Yao, J. Chen, Y. Liu, and R. Zeng, "Planning and Analysis of the Demonstration Project of the MVDC Distribution Network in Zhuhai," *Front. Energy*, vol. 13, no. 1, pp. 120–130, 2019.

[128] B. Zhao, Q. Song, J. Li, Q. Sun, and W. Liu, "Full-Process Operation, Control, and Experiments of Modular High-Frequency-Link DC Transformer Based on Dual Active Bridge for Flexible MVDC Distribution: A Practical Tutorial," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6751–6766, 2017.

[129] B. Zhao, Q. Song, W. Liu, and Y. Sun, "A Synthetic Discrete Design Methodology of High-Frequency Isolated Bidirectional DC/DC Converter for Grid-Connected Battery Energy Storage System using Advanced Components," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5402–5410, 2014.

[130] H. Qin and J. W. Kimball, "Closed-Loop Control of DC-DC Dual-Active-Bridge Converters Driving Single-Phase Inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 1006–1017, 2014.

[131] Y. Shi and H. Li, "Isolated Modular Multilevel DC-DC Converter With DC Fault Current Control Capability Based on Current-Fed Dual Active Bridge for MVDC Application," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2145–2161, 2018.

[132] M. Ryu, H. Kim, J. Baek, H. Kim, and J. Jung, "Effective Test Bed of 380-V DC Distribution System Using Isolated Power Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4525–4536, 2015.

[133] M. R. Banaei and R. Alizadeh, "Simulation-Based Modeling and Power Management of All-Electric Ships Based on Renewable Energy Generation Using Model Predictive Control Strategy," *IEEE Intell. Transp. Syst. Mag.*, vol. 8, no. 2, pp. 90–103, 2016.

[134] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-Circuit and Ground Fault Analyses and Location in VSC-based DC Network Cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, 2012.

[135] Z. Shuai, D. He, Z. Xiong, Z. Lei, and Z. John Shen, "Comparative Study of Short-Circuit Fault Characteristics for VSC-Based DC Distribution Networks with Different Distributed Generators," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 528–540, 2019.

[136] S. Fletcher, P. Norman, S. Galloway, and G. Burt, "Determination of Protection System Requirements for DC Unmanned Aerial Vehicle Electrical Power Networks for Enhanced Capability and Survivability," *IET Electr. Syst. Transp.*, vol. 1, no. 4, pp. 137-147, 2011.

[137] S. Fletcher, P. Norman, S. Galloway, P. Crolla, and G. Burt, "Optimizing the Roles of Unit and Non-Unit Protection Methods within DC Microgrids," *IEEE Trans. Smart Grid*, vol. 3, no. 4, pp. 2079–2087, 2012.

[138] K. Alawasa, Y. Mohamed, and W. Xu, "Active Mitigation of Subsynchronous Interactions Between PWM Voltage-Source Converters and Power Networks," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 121–134, 2014.

[139] A. Meghwani, S. C. Srivastava, and S. Chakrabarti, "A Non-unit Protection Scheme for DC Microgrid Based on Local Measurements," *IEEE Trans. Power Deliv.*, vol. 32, no. 1, pp. 172–181, 2017.

[140] C. Li, P. Rakhra, P. Norman, P. Niewczas, G. Burt, and P. Clarkson, "Practical Computation of di/dt for High-Speed Protection of DC Microgrids," in *ICDCM 2017*, 2017.

[141] ABB, "Surge Currents for IGBT Diodes," 2014. [Online]. Available: https://library.abb.com/. [Accessed: 14-Dec-2019].

[142] BS IEC 60747, "Semiconductor Devices," 2016.

[143] ABB, "IGBT Diode Safe Operating Area (SOA)," 2016. [Online]. Available: https://library.abb.com/. [Accessed: 14-Dec-2019].

[144] S. Kim, D. Dujić, and S. N. Kim, "Protection Schemes in Low-Voltage dc Shipboard Power Systems," in *PCIM Europe*, 2018.

[145] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z. X. Zou, "The Smart Transformer: Impact on the Electric Grid and Technology Challenges," *IEEE Ind. Electron. Mag.*, vol. 10, no. 2, pp. 46–58, 2016.

[146] M. I. Rahman, K. H. Ahmed, and D. Jovcic, "Analysis of DC Fault for Dual-Active Bridge DC/DC Converter Including Prototype Verification," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 2, pp. 1107–1115, 2019.

[147] A. Virdag, T. Hager, J. Hu, and R. W. D. Doncker, "Short circuit behavior of Dual Active Bridge DCDC converter with low resistance DC side fault," in *PEDG 2017*, 2017.

[148] A. Ghazanfari and Y. A. I. Mohamed, "Decentralized Cooperative Control for Smart DC Home With DC Fault Handling Capability," *IEEE Trans. Smart Grid*, vol. 9, no. 5, pp. 5249–5259, 2018.

[149] F. Chang, O. Ilina, M. Lienkamp, and L. Voss, "Improving the Overall Efficiency of Automotive Inverters Using a Multilevel Converter Composed of Low Voltage Si mosfets," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3586–3602, 2019.

[150] D. Philpott and L. Qi, "Solid-State Fault Current Limiters for Residential Houses and Commercial Buildings," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 3431–3436, 2019.

[151] G. P. Adam, I. Abdelsalam, J. E. Fletcher, L. Xu, G. M. Burt, D. Holliday, and S. J. Finney, "Improved Two-Level Voltage Source Converter for High-Voltage Direct Current Transmission Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 4, pp. 1670–1686, 2017.

[152] S. Dhar, R. K. Patnaik, and P. K. Dash, "Fault Detection and Location of Photovoltaic Based DC Microgrid Using Differential Protection Strategy," *IEEE Trans. Smart Grid*, vol. 9, no. 5, pp. 4303-4312, 2018.

[153] L. L. Qi, A. Antoniazzi, L. Raciti, and D. Leoni, "Design of Solid-State Circuit Breaker-Based Protection for DC Shipboard Power Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 260–268, 2017.

[154] J. Do Park, "Ground Fault Detection and Location for Ungrounded DC Traction Power Systems," *IEEE Trans. Veh. Technol.*, vol. 64, no. 12, pp. 5667–5676, 2015.

[155] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC Microgrid Protection: A Comprehensive Review," *IEEE J. Emerg. Sel. Top. Power Electron.*, (Early Access), 2019.

[156] ALSTOM, *Network Protection & Automation Guide*. 2011.

[157] A. Emhemed and G. Burt, "Protection Analysis for Plant Rating and Power Quality Issues in LVDC Distribution Power Systems," in *IEEE Power and Energy Society General Meeting*, 2015.

[158] J. Kim, H. Kim, Y. Cho, H. Kim, and J. Cho, "Application of a DC Distribution System in Korea: A Case Study of the LVDC Project," *Appl. Sci.*, vol. 9, no. 6, 2019.

[159] IEEE, "IEEE Standard for Inverse-Time Characteristics Equations for Overcurrent Relays," 2018.

[160] J. Do Park and J. Candelaria, "Fault Detection and Isolation in Low-Voltage dc-Bus Microgrid System," *IEEE Trans. Power Deliv.*, vol. 28, no. 2, pp. 779–787, 2013.

[161] C. Stefanovic, M. Angjelichinoski, P. Danzi, and P. Popovski, "Resilient and Secure Low-Rate Connectivity for Smart Energy Applications through Power Talk in DC Microgrids," *IEEE Commun. Mag.*, vol. 55, no. 10, pp. 83–89, 2017.

[162] J. Keller and B. Kroposki, "Understanding Fault Characteristics of Inverter-based Distributed Energy Sources," National Renewable Energy Laboratory, Golden, CO, NREL/TP-550-46698, 2010.

[163] K. K. Mehmood, M. Mehdi, C. Noh, and C. Kim, "A High-Speed Fault Detection, Identification, and Isolation Method for a Last Mile Radial LVDC Distribution Network," Energies, vol. 11, no. 11, 2018

[164] J. E. Huber and J. W. Kolar, "Solid-State Transformers: On the Origins and Evolution of Key Concepts," *Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19–28, 2016.

[165] J. Y. Lee, Y. Cho, H. S. Kim, J. T. Cho, and J. Y. Kim, "A Study on the Bipolar DC-DC Converter of SST for LVDC Distribution," in *ICPE 2019 - ECCE Asia*, 2019.

[166] A. Agrawal, C. S. Nalamati, and R. Gupta, "Hybrid DC-AC Zonal Microgrid Enabled by Solid-State Transformer and Centralized ESD Integration," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 9097–9107, 2019.

[167] T. Guillod, F. Krismer, and J. W. Kolar, "Protection of MV Converters in the Grid: The Case of MV/LV Solid-State Transformers," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 393–408, 2017.

[168] H. Hooshyar, M. E. Baran, S. R. Firouzi, and L. Vanfretti, "PMU-Assisted Overcurrent Protection for Distribution Feeders Employing Solid State Transformers," *Sustain. Energy, Grids Networks*, vol. 10, pp. 26–34, 2017.

[169] P. Cairoli and R. A. Dougal, "Fault Detection and Isolation in Medium-Voltage DC Microgrids: Coordination between Supply Power Converters and Bus Contactors," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4535–4546, 2018.

[170] L. Zhang, N. Tai, W. Huang, J. Liu, and Y. Wang, "A Review on Protection of DC Microgrids," *J. Mod. Power Syst. Clean Energy*, vol. 6, no. 6, pp. 1113–1127, 2018.

[171] D. M. Bui, S. L. Chen, C. H. Wu, K. Y. Lien, C. H. Huang, and K. K. Jen, "Review on Protection Coordination Strategies and Development of An Effective Protection Coordination System for DC Microgrid," in *APPEEC*, 2014.

[172] D. Wang, A. Emhemed, and G. Burt, "A Novel Protection Scheme for an LVDC Distribution Network With Reduced Fault Levels," in *ICDCM 2017*, 2017.

[173] A. Smith, D. Wang, A. Emhemed, and G. Burt, "An Investigation into the Limitations of the Combined dv/dt and di/dt Protection Technique for Compact d.c. Distribution Systems," in *UPEC 2018*, 2018.

[174] R. Li, L. Xu, and L. Yao, "DC Fault Detection and Location in Meshed Multiterminal HVDC Systems based on DC Reactor Voltage Change Rate," *IEEE Trans. Power Deliv.*, vol. 32, no. 3, pp. 1516–1526, 2017.

[175] V. Psaras, A. Emhemed, G. Adam, and G. Burt, "Review and Evaluation of the State of the Art of DC Fault Detection for HVDC Grids," in *UPEC 2018*, 2018.

[176] D. Chen, L. Xu, and J. Yu, "Adaptive DC Stabilizer with Reduced DC Fault Current for Active Distribution Power System Application," *IEEE Trans. Power Syst.*, vol. 32, no. 2, pp. 1430–1439, 2017.

[177] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC Microgrids - Part I: A Review of Control Strategies and Stabilization Techniques," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4876–4891, 2016.

[178] M. K. Bucher and C. M. Franck, "Analytic Approximation of Fault Current Contributions from Capacitive Components in HVDC Cable Networks," *IEEE Trans. Power Deliv.*, vol. 30, no. 1, pp. 74–81, 2015.

[179] M. Farhadi and O. A. Mohammed, "Event-Based Protection Scheme for a Multiterminal Hybrid DC Power System," *IEEE Trans. Smart Grid*, vol. 6, no. 4, pp. 1658–1669, 2015.

[180] A. Shabani and K. Mazlumi, "Evaluation of a Communication-Assisted Overcurrent Protection Scheme for Photovoltaic Based DC Microgrid," *IEEE Trans. Smart Grid*, vol. PP, no. c, pp. 1–1, 2019.

[181] X. Feng, Q. Xiong, D. Wardell, A. L. Gattozzi, S. M. Strank, and R. E. Hebner, "Extra-Fast DC Distribution System Protection for Future Energy Systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 3421–3430, 2019.

[182] A. Meghwani, R. Gokaraju, S. C. Srivastava, and S. Chakrabarti, "Local Measurements-Based Backup Protection for DC Microgrids Using Sequential Analyzing Technique," *IEEE Syst. J.*, (Early Access), 2019.

[183] F. Wang and Z. Zhang, "Overview of Silicon Carbide Technology: Device, Converter, System, and Application," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, 2016.

[184] D. Wang, A. A. S. Emhemed, and G. M. Burt, "Improved Voltage-based Protection Scheme for An LVDC Distribution Network Interfaced by A Solid State Smart Transformer," *IET Gener. Transm. Distrib.*, vol. 13, no. 21, pp. 4821–4829, 2019.

[185] C. Li, P. Rakhra, P. Norman, G. Burt, and P. Clarkson, "Metrology Requirements of State-of-the-Art Protection Schemes for DC Microgrids," *J. Eng.*, vol. 2018, no. 15, pp. 987–992, 2018.

[186] S. Jiang, C. Fan, and N. Huang, "Fault Location in Low-Voltage Direct Current Network based on Auxiliary Injection Unit," *IET Gener. Transm. Distrib.*, vol. 13, no. 19, pp. 4347–4354, 2019.

[187] K. Jia, M. Sumner, E. Christopher, T. Bi, and D. Thomas, "Advanced DC Zonal Marine Power System Protection," *IET Gener. Transm. Distrib.*, vol. 8, no. 2, pp. 301–309, 2014.

[188] BS7671, "Requirements for Electrical Installations," 2018.

[189] S. Stewart, *How to Integrate It: A Practical Guide to Finding Elementary Integrals*. Cambridge University Press, 2017.

[190] D. Wang, V. Psaras, A. Emhemed, and G. Burt, "A Novel Fault Let-through Energy based Fault Location for LVDC Distribution Networks," *IEEE Trans. Power Deliv.*, *Early Access*, 2020.