University of Strathclyde

Department of Electronic and Electrical Engineering

New Types of Voltage Source Converters Applied in Flexible AC Transmission System Devices

Peng Li

A thesis presented in fulfilment of the requirements for the Degree of Doctor of Philosophy

June 2015

Dedicated to my family

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: **Peng Li**

Date: 18/06/2015

Acknowledgement

Sincere gratitude belongs to my family for their unconditional support and great love; and I want to extend the best wishes for their health and happiness.

I would like to express my high tribute to my supervisors Prof. Barry Williams and Dr. Derrick Holliday for their constructive supervision and continuous support. Special thanks to Dr. Grain Philip Adam for his invaluable suggestions based on his profound knowledge and Mr. Charles Croser, who helped me in the building of the test rigs.

In retrospect, I have spent such pleasant time in the PEDEC research group with so many caring colleagues. This will always be a fortune of my life.

I would also like to acknowledge China Scholarship Council (CSC) for their financial support during my Ph.D. study.

All in all, thanks to everyone who helped me to get through the memorable journey and finally reach this stage.

Abstract

The uses of flexible alternating current transmission system (FACTS) controllers in next generation smart grids are encouraged by the increased uses of decentralized and highly meshed grid structures that may affect the stability of power systems. Voltage source converter (VSC) based FACTS devices have reduced footprint and offer increased control flexibility, extended range and faster reaction time than line commutated thyristor based equivalent solutions.

The performance of commonly used FACTS devices that employ a two-level converter is summarized. Then, multilevel converters and direct AC-AC converters which are viable for FACTS applications are reviewed. The outcomes of the literature surveys are refined to identify new features that may be critical for future centralised and decentralized smart grids such as: control range extension, improved efficiency and power density at reduced hardware cost. To pursue these features, three novel VSC topologies are proposed and analysed:

An AC voltage-doubled (ACVD) topology with an internal inverting buck-boost cell in each phase-leg, is able to synthesize twice the output voltage of a conventional two-level VSC for the same dc link voltage, is proposed. A number of new modulation and control strategies that aim to further increase DC utilization of the ACVD converter and to manage its internal dynamic interaction to prevent the appearance of low-order harmonics in the output currents, are presented. With its high DC-rail utilization and sophisticated control strategies, the ACVD converter offers an extended power control range, which is increasingly important for shunt and series type FACTS devices.

The controlled transition full-bridge hybrid multilevel converter (CTFB-HMC) with chain-links of full-bridge cells is proposed to combine the advantages of improved wave-shaping ability, reduced footprint and high efficiency, which promote its applications in medium and high voltage FACTS devices.

An AC hexagonal chopper using heterodyne modulation to decouple the control of AC voltage amplitude from that of the phase-angle is proposed. For scalability to medium and high voltage, a modular multilevel AC hexagonal chopper (M2AHC) is developed. With adoption of a quasi-two-level transitional mode for reduced cell number and minimized footprint, dv/dt is limited and reliability is improved.

Simulation and experimentation are used to validate the modulation, control and FACTS implementation of the three proposed converters.

Abbreviation

FACTS	flexible alternating current system
HVDC	high voltage direct current
VSC	voltage source converter
DG	distributed generation
SVC	static var compensator
TCSC	thyristor controlled series compensator
DPFC	dynamic power flow controller
PST	phase-shift transformer
IGBT	insulated gate bipolar transistor
IGCT	integrated gate commutated thyristor
STATCOM	static synchronous compensator
SSSC	static synchronous series compensator
DVR	dynamic voltage restorer
UPFC	unified power flow controller
PCC	point of common coupling
PI	proportional integral
PR	proportional resonance
SRF	synchronous reference frame
ADC	analog-digital conversion
ACVD	AC voltage-doubled
HB-MMC	half-bridge modular multilevel converter
FB-MMC	full-bridge modular multilevel converter
HMC	hybrid multilevel converter
CTFB	controlled transition full-bridge
M2AHC	modular multilevel AC hexagonal chopper
SST	solid-state transformer
GMPFC	general multi-bus power flow controller

Nomenclature

V_g	grid nodal voltage
V_c	VSC output voltage
i_{sh}	shunt compensator injected current
Q_{sh}	exchanged shunt compensator reactive power
V_{se}	injected series compensator voltage
Q_{se}	exchanged series compensator reactive power exchange
V_{dc}	DC-link voltage
C_d	DC-link capacitance of VSC
C_f	filtering capacitance of VSC
L_f	filtering inductance of VSC
M	voltage transfer ratio of ACVD converter
f_0	grid nominal fundamental frequency
f_{sw}	switching frequency of power electronics converter
f_r	resonance frequency for second-order system
G_i	transfer function of control to output current
G_v	transfer function of control to output voltage
G_{vdc}	transfer function of control to DC voltage
ω_B	window width of proportional integral controller
v_{cell}	cell capacitor voltage
N	total number of full-bridge cells in CTFB-HMC
N_{on}	cell number for voltage synthesis in the CTFB-HMC
N_p	positive-state cell number in the CTFB-HMC
N_n	negative-state cell number in the CTFB-HMC
N_0	zero-state cell number in the CTFB-HMC
L_{dc}	DC side inductance of CTFB-HMC
T_s	sampling period of power electronics converter
P_{IGBT}	power losses of IGBT
P_D	power losses of diode
F_{con}	power switching device number in the conduction path

	of multilevel converters
A	amplitude of output voltage for the hexagonal chopper system without heterodyne modulation
Δ	phase-shift of output voltage for the hexagonal chopper system without heterodyne modulation
n_u	number of cell capacitors in conduction path of M2AHC upper arm
n_l	number of cell capacitors in conduction path of M2AHC lower arm
δt	time step for quasi-2-level mode operation of M2AHC
τ	duty cycle loss for quasi-2-level operation in M2AHC
C_{eh}	effective capacitance in upper arm of M2AHC
C_{el}	effective capacitance in lower arm of M2AHC
i_h	upper arm current in the hexagonal AC chopper
i_l	lower arm current in the hexagonal AC chopper
i_o	output current in the hexagonal AC chopper
i_{cir}	circulating current in the hexagonal AC chopper
A_H	Amplitude of output voltage for the hexagonal chopper system with heterodyne modulation
Δ_H	Phase-shift of output voltage for the hexagonal chopper system with heterodyne modulation

Table of Contents

CHAPTER 1

Introduction

With the increased demand of reform to the traditional centralized power system, the deep penetration of distributed generation (DG) and liberalisation process have increased stresses on current electric power network facilities in terms of capacity, stability and other technical limits. Grid integration of large scale renewable energy sources with an intermittent nature is growing rapidly in order to cut the carbon emission level of traditional fossil fuels. These factors all contribute to the trend of decentralized and a meshed grid structure; and call for fast, accurate power flow control ability to manage the electric power dispatch task. The flexible alternating current transmission system (FACTS) offers attractive features for voltage, current, impedance, and power regulation by using power electronics switching devices, and has drawn attention and effort in academic research and industry practise.

1.1 Background

The traditional alternating current (AC) power network was initially established for its convenience and low cost. However, increasing power delivery capacity and distance, along with the various grid connected objects and methods in generation and distribution, all make the old power system inefficient and inflexible, thereby constraining the sustainable development of the electric power industry [1-3].

Power electronics is a subject that employs power semiconductor devices to manipulate energy flow to achieve several desired control objectives at the system level. It can facilitate an efficient interface between the micro-control system and the bulky power solution components. After surmounting several bottlenecks, such as safe operation and reliable control of high voltage high power converters, power electronics continues to penetrate the area of power systems [4-7].

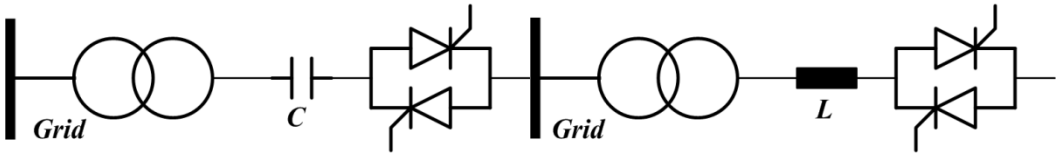
The flexible alternating current transmission system (FACTS) covers a wide range of techniques dedicated to enhance power system controllability including power quality, dynamic performance, operational stability, and transmission capacity by means of static switched devices based on power semiconductors [1, 8]. As shown in Table 1-1, conventional compensation devices are based on fixed or mechanical switched inductors, capacitors, resistors and transformers; while FACTS devices employ power electronics converters to switch these passive elements with fast speed and a flexible pattern, thus, they are usually described as static and dynamic controllers. Currently, the thyristor-valve and the voltage source converter (VSC) that uses the insulated gate bipolar transistor (IGBT) or integrated gate commutated thyristor (IGCT), are the two major FACTS device components [9, 10]. Impedance based FACTS devices can be divided according to their connection types, viz., shunt, series, and shunt-series. Examples of these categories are series mechanical switched capacitors (MSC); series and shunt thyristor switched capacitor (TSC) and shunt thyristor controlled reactor (TCR); and phase shift transformer (PST). Also, current and voltage source converter based FACTS devices can be divided into series and shunt types. Besides of the manipulation of reactive power to control power flow, some current and voltage source converter based FACTS devices can be used to transmit power over long distance and decouple the AC grids, such as line-commutated and self-commutated high voltage direct current (HVDC) transmission systems, including back-to-back (B2B) architectures [8, 11-14].

Table 1-1. Classification of power system compensators (mechanical switched devices, FACTS)

	Conventional Mechanical Switch	FACTS Devices	
		Thyristor Valve	Voltage Source Converter (VSC)
Shunt Type	Switched Shunt LC Compensator	Static VAr Compensator (SVC)	Static Synchronous Compensator (STATCOM)
Series Type	Switched Series LC Compensator	Thyristor Controlled Series Compensator (TCSC)	Static Synchronous Series Compensator (SSSC)
Shunt and Series Types	Phase Shift Transformer (PST)	Dynamic Power Flow Controller (DPFC)	Unified Power Flow Controller (UPFC)

1.1.1. Shunt Type FACTS Devices

Shunt connected compensators are predominantly used for the reactive power compensation and voltage control. Static VAr compensator (SVC) with thyristors is an example of the shunt type line-commutated FACTS devices; while the static synchronous compensator (STATCOM) is a self-commutated FACTS device based on current or voltage source converters, where the voltage source type is preferred for its suitability in high voltage conditions over current source types. Compared to mechanical switched LC devices, SVC and STATCOM offer fast and accurate response due to the use of static switches and flexible modulation techniques.



(a) (b)

Fig. 1-1. The typical SVC components with thyristor-valves: (a) TSC and (b) TSR/TCR.

A typical SVC installation with inductive and capacitive reactive power generation capability consists of back-to-back thyristor-valves, air-core reactors, high-voltage AC capacitors and an interfacing transformer to facilitate the controllable LC network loaded on the grid [15]. Generally, as in Fig. 1-1, this network can be combinations of a thyristor switched capacitor (TSC) and a thyristor controlled reactor (TCR) [16, 17]. Proper operation and coordination of these controllable passive elements can contribute to fast and precise reactive power compensation

suitable for mitigation of the impact of random load variations on grid voltage fluctuation; thereby, improving the overall power system stability [18, 19].

Since the SVC can be recognized as a controllable impedance network, its shunt current characteristics are influenced by the grid nodal voltage at the point of common coupling (PCC), thus, the reactive power. In contrast, the VSC based STATCOM supplies (absorbs) reactive power to (from) the grid by varying the magnitude of the synthesized voltage behind phase interfacing reactors or transformer relative to the grid at the PCC, as shown by Fig. 1-2. It contains the DC bus capacitor bank, IGBT/IGCT stack, and interfacing reactors or transformer. The use of self-commutated power switching devices allows the VSC to smoothly turn-on and turn-off the LC energizing path at high frequency, which reduces the hardware volume. Also, flexible modulation techniques and independent active reactive power control are available. Since it can generate an arbitrary and independent voltage vector in the shunt branch to regulate the quadrature current, the VSC based STATCOM decouples the relationship between the shunt current and grid voltage. Therefore, it is expected that full capability can be guaranteed, even under voltage droop conditions [20-23].

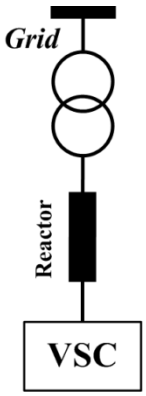


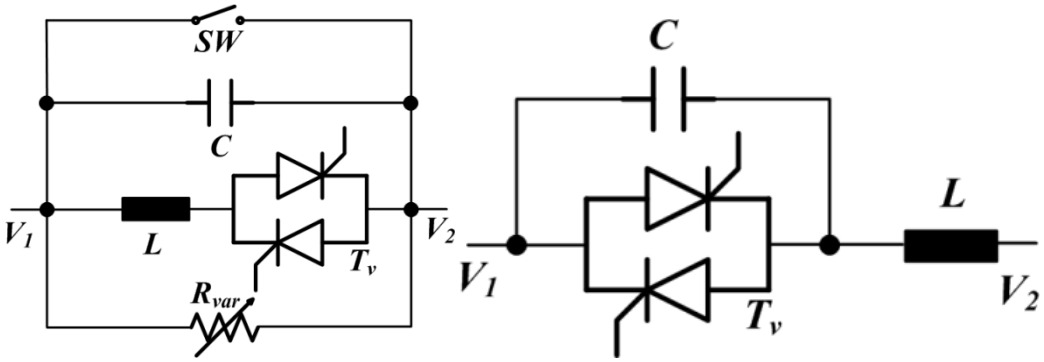
Fig. 1-2. STATCOM configuration using a VSC.

1.1.2. Series Type FACTS Devices

Series compensation devices are series connected into the power line, thus can adjust the line effective impedance to change the power flow and improve stability. Practically, this kind of device is vulnerable during fault conditions; therefore, it should be installed in parallel with thyristors switched protector for bypassing under fault conditions. Thyristor-valve and VSC (using self-commutated IGBT/IGCT) based series FACTS devices are usually named as a thyristor controlled series compensator (TCSC) and static synchronous series compensator (SSSC) respectively.

TCSC is mainly used as a damping device such as for the inter-area oscillation or sub-synchronous resonance (SSR) problems, to stabilize the overall system [24]; and naturally, the power flow can be regulated by smooth adjustment of the line impedance. Its typical configuration is shown in Fig. 1-3(a), where *SW* represents the bypass protection valve and T_v is fired to supply compensation. By tuning the output characteristic of the thyristor controlled block, the impedance of the fixed main capacitor bank becomes variable, thereby is able to suppress potential unstable factors and track the power flow command to respond to load transitions [25, 26].

Short-circuit current limiter (SCCL) is another kind of widely used thyristor series device, as shown in Fig. 1-3(b), where a thyristor protected series capacitor (TPSC) is included. During normal operation, the SCCL behaves like as TCSC by tuning the composite network impedance. When a short-circuit occurs, the capacitor is shorted rapidly by the thyristor and the series reactor will effectively increase the output impedance to limit any sharp rise of the line current [27].



(a) (b)

Fig. 1-3. Typical series FACTS devices with thyristor-valves protection: (a) TCSC and (b) SCCL.

The VSC based series compensation device of Fig. 1-4 at the transmission level is called a SSSC. It contains a DC-link capacitor bank, IGBT/IGCT stack, local filter and a series injected transformer. By inserting a quadrature voltage source that is always perpendicular to the line current, the effective line impedance can be adjusted, thus, the power flow and stability are influenced. The SSSC also requires a thyristor valve as a protection switch because of the low overload capability of power semiconductors. Due to high installation costs and the fact that a TCSC can meet most of the grid requirements currently, the SSSC has not achieved practical penetration, although it is superior in terms of control range and flexibility. Alternatively, a VSC based series device in a voltage control mode, called dynamic

voltage restorer (DVR), has gained wide application as a voltage maintainer at the distribution level or grid area with large scale intermittent renewable energy incorporation, providing sag/swell restoration, flicker mitigation, and unbalanced compensation [28-30].

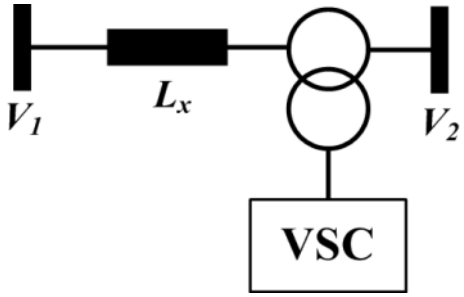


Fig. 1-4. SSSC configuration using VSC.

1.1.3. Shunt-Series Type Devices

With the increasing diversity of load conditions and grid structure complexity, power flow dispatch becomes more important to better utilize transmission capacity and balance regional power supply-demand.

A shunt-series FACTS device using thyristor-valves is called the dynamic power flow controller (DPFC), and is used for power flow controllability improvement. It employs a fractional PST that provides a phase-variable voltage source in series with a chain of TSC and TCR devices which are employed to respond to fast load transitions, as in Fig. 1-5. This facility is able to augment power line transmission capacity utilization and fulfil current power flow control requirements. The PST maximum tap-changer ratio, the maximum capacitance, and maximum reactance, together define the power flow control range of the DPFC [31, 32].

The VSC based shunt-series device is called unified power flow controller (UPFC), which consists of a shunt connected VSC and a series-connected VSC sharing a common DC-link. The UPFC is usually viewed as a combination of STATCOM and SSSC, as in Fig. 1-6; therefore, it supplies independent power flow controllability as well as a free degree for voltage regulation. Since the DC-link is shared by the two VSCs, an additional active power flow path is offered by the UPFC, meaning an independent voltage vector relative to the line current can be injected into the grid, extending the power flow control range. Like the SSSC, the series VSC of the UPFC installation also requires a thyristor bypass switch in case of overload [33, 34].

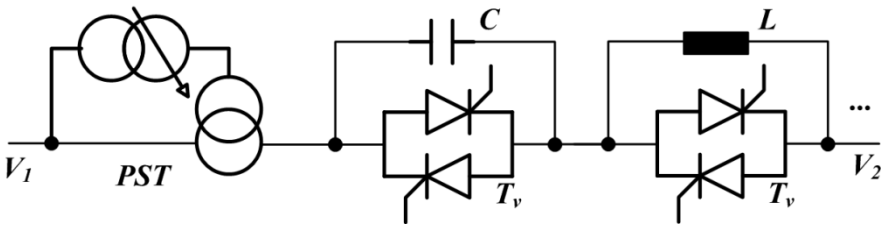


Fig. 1-5. DPFC using PST and thyristor controlled impedance.

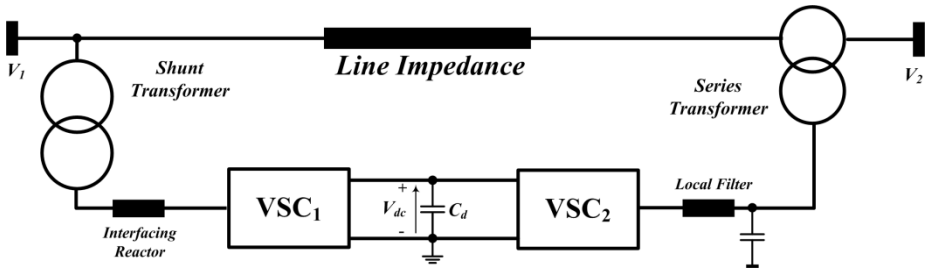
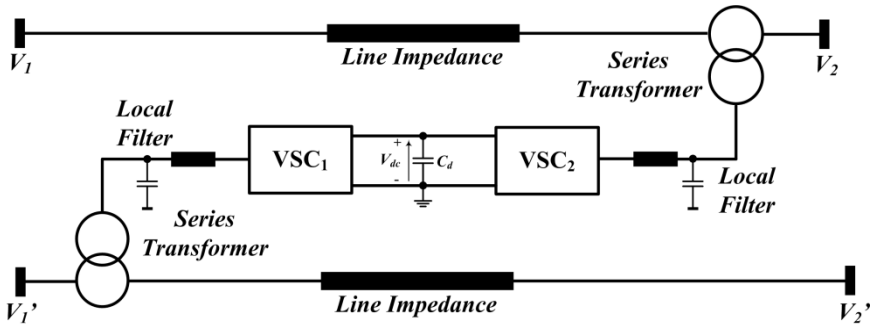
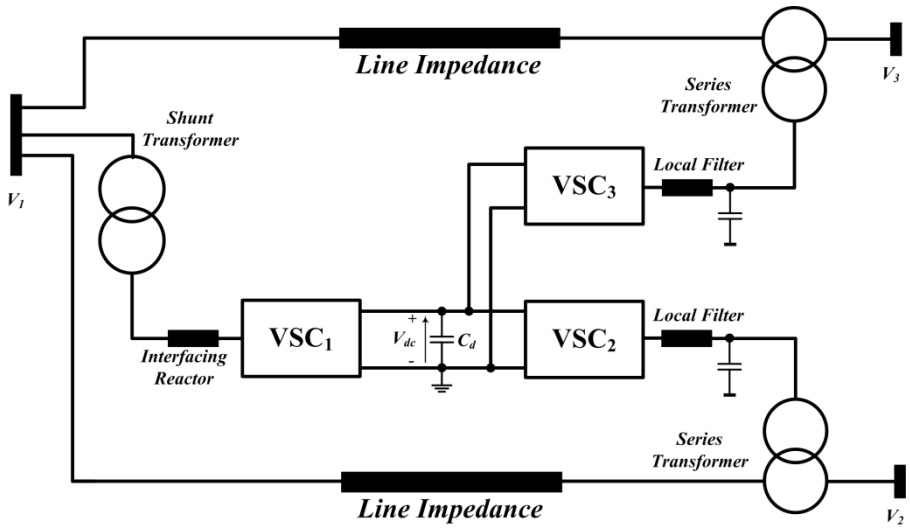


Fig. 1-6. Diagram of the UPFC configuration using VSC.

Several multi-bus power flow controllers can be derived from the UPFC configuration such as the interline power flow controller (IPFC) and the generalized power flow controller (GUPFC). The IPFC structure is shown in Fig. 1-7(a). It employs two series connected VSC via a common DC-link, where the active power is able to circulate through this path. Then the power flow on the two lines can be regulated rapidly. Compared with the IPFC, the more complex GUPFC device incorporates an extra shunt connected VSC; and a scalable number of series VSCs are coupled to the same DC-link, as in Fig. 1-7(b). Therefore, a group of buses can be integrated and regulated through a GUPFC acting as a hub, which significantly improves the flexibility and capacity of the power transmission [35-38]. Many of the considered multifunction FACT devices may suffer from the long distance between the various optimally located shunt and series connected devices, as illustrated in Fig. 1-7(a), for example.



(a)



(b)

Fig. 1-7. VSC based multi-bus power flow controller: (a) IPFC and (b) GUPFC.

1.1.4. Back-to-Back Devices

Back-to-back (B2B) configured devices are usually used to supply full-range power flow control. Typically, a HVDC system as in Fig. 1-8 offers side-by-side decoupling and provides the ability to integrate AC grids with different frequencies (asynchronous connection), avoiding synchronization problems in pure synchronous AC systems.

Conventional HVDC using thyristor based line-commutated-converter (LCC) can only control the active power, not reactive power. This lack of independence on power control largely constrains the operation range of the LCC-HVDC station. It also requires large sized passive devices for filtering due to the low order harmonic distortion introduced by an LCC. Given the high power capacity of the thyristor, the LCC-HVDC station is competitive at high power levels [11, 12].

VSC-HVDC is called light HVDC (by ABB), and offers more flexible control, higher response speed, and more operational convenience in power flow control. A VSC-HVDC system offers four-quadrant operational ability at both terminals and provides independent active/reactive power control. Reactive power control can significantly improve the utilization and transmission capacity of the power cable. The VSC self-commutated power switches allows voltage synthesizes with only high frequency harmonics, the filtering element size is smaller, relative to a LCC converter [14, 39]. B2B devices with fragmental power rating can be viewed as a DC-link coupled STATCOM, which can also exchange active power with the grid.

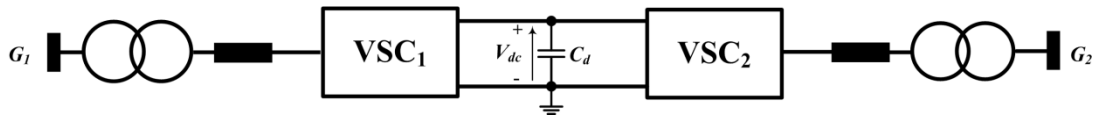


Fig. 1-8. B2B HVDC transmission system with two grid terminals.

1.2 Motivation

VSC based FACTS devices have advantages in terms of independent control of active and reactive power, reduced footprint, and better dynamic response than conventional thyristor based solutions. In modern power system, VSC topologies for FACTS devices should meet the requirements of high power density, low power losses, low harmonic components, small footprint, etc.

The conventional two-level converter is able to synthesize better quality output voltage than the LCC by the use of self-commutated power switches and various high frequency pulse width modulation (PWM) methods. However, it suffers from DC rail low utilization (thus, large DC capacitor size and footprint), high switching losses, and high *dv*/*dt* (electromagnetic interference, EMI and stray capacitor currents) seen by the AC side.

The multilevel converter was introduced to reduce the voltage stress per switch and extend the power rating without using direct series connection of power switches. Compared to a two-level converter, it can improve the AC voltage waveform quality by stepping through multiple intermediate voltage levels at the converter output terminal. As a result, the *dv*/*dt* (EMI) and switching losses are decreased.

To improve the power density of a two-level converter, modulation techniques that directly or indirectly utilize the zero sequence components were developed, such as the triplen injection sinusoidal PWM (TSPWM), space vector modulation (SVM) and selective harmonic elimination (SHE). However, these improvements are minor due to the hardware constraints. The incorporation of voltage-lift cells into each phase-leg of a two-level converter is suggested in this thesis as an effective way to extend the output voltage range (thus, achieving high power density). Several modelling and control challenge problems that arise from the existence of numerous energy conversion stages from the input to output, have been solved to ensure proper operation.

Direct AC-AC converter is an alternative solution for AC voltage control without using bulky DC-link capacitors; so it is able to reduce the footprint, improve the power density, and increase the service life. The decoupled regulation of the AC

voltage amplitude and phase-angle (active and reactive power) are required in this kind of converter; especially when acting as power flow and power quality controllers.

The research in this thesis explores new VSC topologies that are advantageous in medium and high voltage applications, particularly in FACTS devices. High DC-rail utilization topologies, multilevel converters, and direct AC-AC converters are the focus.

1.3 Objectives

In this thesis, two-level, multilevel and direct AC-AC converters are reviewed to identify their main attributes and limitations from the point of view of FACTS devices. Then novel converter topologies within these categories are to be exploited in this thesis to achieve the following system improvements:

- Improved power density and DC-link voltage utilization are preferred to extend the power control range of STATCOM and SSSC by overcoming the DC voltage limit for reactive power generation compared to the two-level converter (for the same dc link).
- High efficiency and high power density multilevel converter topologies for medium and high voltage applications are investigated to facilitate scalability, high reliability and better steady-state performance.
- Direct AC-AC converter with independent active and reactive power control, modularity and small energy storage can save the DC-link stage, making the overall system light and economical without discount in the performance as typical FACTS devices.

1.4 Thesis Organization

This thesis is organized into ten chapters. The arrangement is elaborately interpreted as follows:

Chapter 1 (Introduction of FACTS):

This chapter presents the background and evolution of the FACTS devices. The functions of different FACTS controllers are interpreted. Then, the motivation and objectives of this research are outlined, where three main categories of converters including the two-level converter, multilevel converter and direct AC-AC converter are to be investigated for FACTS applications.

Chapter 2-4 (Two-level converter):

In chapter 2, the brief review of two-level and full-bridge converters as well as different modulation techniques is carried out. Also, system level behaviour and control strategies for key FACTS devices are analysed and derived based on the two-level converter.

Chapter 3 proposes an ACVD-VSC topology which uses a voltage-lift cell in each phase to improve output voltage range and power density. Modelling and control schemes are presented to achieve high quality AC voltage and current. Simulation and experimentation substantiate the effectiveness of the converter.

Chapter 4 develops the ACVD converter to be applied as a FACTS device. The *d-q* frame control schemes for an ACVD-STATCOM and SSSC are described; and their extended power control ranges are compared to two-level VSC solutions, and verified through simulation.

Chapter 5-6 (Multilevel converter):

Chapter 5 presents a detailed literature survey of multilevel converter topologies. The main contributions and limitations of these converters are analysed and compared

Chapter 6 proposes a novel multilevel converter with the CTFB topology, which offers low power losses and high power density. Converter dimensioning and modulation strategy for cell energy balancing are investigated. Simulation and experimental results confirm the validity of the proposed converter. The CTFB converter used as a STATCOM is demonstrated.

Chapter 7-9 (Direct AC-AC converter):

Chapter 7 summarizes the different kinds of AC-AC converters that are viable for FACTS devices, where the advantages and disadvantages are highlighted.

Chapter 8 considers the operational principles of a three-phase delta-connected AC chopper system and its scalable version - the M2AHC. Using heterodyne modulation, output AC voltage amplitude and phase control can be decoupled, allowing independent regulation of active and reactive power. The feasibility of this approach is verified with simulation and experimentation.

Chapter 9 employs the M2AHC to generate a new breed of FACTS devices based on direct AC-AC conversion. The configuration, modelling, and control algorithms are interpreted and verified by simulation.

Chapter 10 (Research Conclusion):

This chapter highlights the main achievements of this research; and the expectations for the future research are also presented.

Reference

[1] N. G. Hingorani, L., *Understanding FACTS:Concepts and Technology of Flexible AC Transmission Systems*: Wiley-IEEE Press, 2000.

[2] V. K. Sood, *HVDC and FACTS controllers: applications of static converters in power systems*: Springer Science & Business Media, 2004.

[3] M. H. Bollen, *Understanding power quality problems* vol. 3: IEEE press New York, 2000.

[4] N. G. Hingorani, "High power electronics and flexible AC transmission system," in *Proceedings of the American Power Conference;(USA)*, 1988.

[5] N. G. Hingorani, "Power electronics in electric utilities: role of power electronics in future power systems," *Proceedings of the IEEE*, pp. 481-482, 1988.

[6] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*: Springer Science & Business Media, 2001.

[7] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *Power Electronics, IEEE Transactions on*, vol. 19, pp. 1184-1194, 2004.

[8] X.-P. Zhang, C. Rehtanz, and B. Pal, *Flexible AC Transmission Systems: Modelling and Control*: Springer Science & Business Media, 2012.

[9] R. M. Mathur and R. K. Varma, *Thyristor-based FACTS controllers for electrical transmission systems*: John Wiley & Sons, 2002.

[10] G. Reed, R. Pape, and M. Takeda, "Advantages of voltage sourced converter (VSC) based design concepts for FACTS and HVDC-link applications," in *Power Engineering Society General Meeting, 2003, IEEE*, 2003.

[11] G. Chunyi, Z. Yi, A. Gole, and Z. Chengyong, "Analysis of dual-infeed HVDC with LCC-HVDC and VSC-HVDC," in *Power and Energy Society General Meeting (PES), 2013 IEEE*, 2013, pp. 1-1.

[12] Y. Haiping, F. Lingling, and M. Zhixin, "Coordination between DFIG-based wind farm and LCC-HVDC transmission considering limiting factors," in *Energytech, 2011 IEEE*, 2011, pp. 1-6.

[13] W. Song, L. Gengyin, Z. Ming, and Z. Zhe, "Research on VSC-HVDC system to mitigate power output fluctuation caused by wind farms," in *Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on*, 2011, pp. 314-319.

[14] K. Eriksson, "Operational experience of HVDC Light," in *AC-DC Power Transmission, 2001. Seventh International Conference on (Conf. Publ. No. 485)*, 2001, pp. 205-210.

[15] R. Grunbaum, M. Halonen, and G. Stromberg, "SVC for 69 kV direct grid connection," in *Transmission and Distribution Conference and Exposition, 2008. T&D. IEEE/PES*, 2008, pp. 1-7.

[16] K. M. Son, K. S. Moon, S. K. Lee, and J. K. Park, "Coordination of an SVC with a ULTC reserving compensation margin for emergency control," in *Power Industry Computer Applications, 1999. PICA '99. Proceedings of the 21st 1999 IEEE International Conference*, 1999, pp. 343-348.

[17] C. Peiyuan, C. Zhe, and B. Bak-Jensen, "Comparison of steady-state SVC models in load flow calculations," in *Universities Power Engineering Conference, 2008. UPEC 2008. 43rd International*, 2008, pp. 1-5.

[18] C. Ya-Chin, "Multi-Objective Optimal SVC Installation for Power System Loading Margin Improvement," *Power Systems, IEEE Transactions on,* vol. 27, pp. 984-992, 2012.

[19] H. Ambriz-Perez, E. Acha, and C. R. Fuerte-Esquivel, "Advanced SVC models for Newton-Raphson load flow and Newton optimal power flow studies," *Power Systems, IEEE Transactions on,* vol. 15, pp. 129-136, 2000.

[20] Q. Wei, R. G. Harley, and G. K. Venayagamoorthy, "Coordinated Reactive Power Control of a Large Wind Farm and a STATCOM Using Heuristic Dynamic Programming," *Energy Conversion, IEEE Transactions on,* vol. 24, pp. 493-503, 2009.

[21] Y. Del Valle, J. C. Hernandez, G. K. Venayagamoorthy, and R. G. Harley, "Multiple STATCOM Allocation and Sizing Using Particle Swarm Optimization," in *Power Systems Conference and Exposition, 2006. PSCE '06. 2006 IEEE PES*, 2006, pp. 1884-1891.

[22] C. Yiqiang and O. Boon-Teck, "STATCOM based on multimodules of multilevel converters under multiple regulation feedback control," *Power Electronics, IEEE Transactions on,* vol. 14, pp. 959-965, 1999.

[23] B. T. Ooi, H. Xiaogang, and G. Joos, "Operating principles of shunt STATCOM based on 3-level diode-clamped converters," in *Power Engineering Society 1999 Winter Meeting, IEEE*, 1999, p. 1333 vol.2.

[24] H. Hosseini and B. Tousi, "Mitigating SSR in hybrid system with steam and wind turbine by TCSC," in *Electrical Power Distribution Networks (EPDC), 2012 Proceedings of 17th Conference on*, 2012, pp. 1-6.

[25] S. Meikandasivam, R. K. Nema, and S. K. Jain, "Selection of TCSC parameters: Capacitor and inductor," in *Power Electronics (IICPE), 2010 India International Conference on*, 2011, pp. 1-5.

[26] P. K. Tiwari and Y. R. Sood, "An Efficient Approach for Optimal Allocation and Parameters Determination of TCSC With Investment Cost Recovery Under Competitive Power Market," *Power Systems, IEEE Transactions on,* vol. 28, pp. 2475-2484, 2013.

[27] H. Song, M. Xue-yan, and C. Yong, "A study on modeling of high-voltage short circuit current limiter in electromechanical transient simulation," in *Power System Technology (POWERCON), 2010 International Conference on*, 2010, pp. 1-6.

[28] Q. Liu, Z. Wang, and Z. Zheng, "Study and Simulation of SSSC and TCSC Transient Control Performance," in *Power System Technology and IEEE Power India Conference, 2008. POWERCON 2008. Joint International Conference on*, 2008, pp. 1-6.

[29] S. Kamel, M. Abdel-Akher, and M. K. El-Nemr, "Implementation of SSSC model in the Newton-Raphson power flow formulation using current injections," in *Universities Power Engineering Conference (UPEC), 2010 45th International*, 2010, pp. 1-5.

[30] Y. Prakash and S. Sankar, "Power quality improvement using DVR in power system," in *Power and Energy Systems Conference: Towards Sustainable Energy, 2014*, 2014, pp. 1-6.

[31] U. Hager, K. Gorner, and C. Rehtanz, "Hardware model of a Dynamic Power Flow Controller," in *PowerTech, 2011 IEEE Trondheim*, 2011, pp. 1-6.

[32] A. Sheykholeslami, A. R. Ahmadi, S. A. N. Niaki, and H. Ghaffari, "Power flow modeling/calculation for power systems with Dynamic Flow Controller," in *Vehicle Power and Propulsion Conference, 2008. VPPC '08. IEEE*, 2008, pp. 1-5.

[33] S.-j. Yao, X.-y. Song, Y. Wang, Y.-x. Yan, and Z. Yan, "Research on dynamic characteristics of Unified Power Flow Controller (UPFC)," in *Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on*, 2011, pp. 490-493.

[34] A. Seungwon, J. Condren, and T. W. Gedra, "An Ideal Transformer UPFC Model, OPF First-Order Sensitivities, and Application to Screening for Optimal UPFC Locations," *Power Systems, IEEE Transactions on*, vol. 22, pp. 68-75, 2007.

[35] S. Sankar and S. Ramareddy, "Simulation of series and shunt compensated IPFC system," in *Information and Communication Technology in Electrical Sciences (ICTES 2007), 2007. ICTES. IET-UK International Conference on*, 2007, pp. 485-488.

[36] A. V. N. Babu and S. Sivanagaraju, "Mathematical modelling, analysis and effects of interline power flow controller (IPFC) parameters in power flow studies," in *Power Electronics (IICPE), 2010 India International Conference on*, 2011, pp. 1-7.

[37] R. S. Lubis, "Modeling and simulation of generalized unified power flow controller (GUPFC)," in *Instrumentation, Communications, Information Technology, and Biomedical Engineering (ICICI-BME), 2011 2nd International Conference on*, 2011, pp. 207-213.

[38] Z. Xiao-Ping, E. Handschin, and M. Yao, "Modeling of the generalized unified power flow controller (GUPFC) in a nonlinear interior point OPF," *Power Systems, IEEE Transactions on*, vol. 16, pp. 367-373, 2001.

[39] D. Das, J. Pan, and S. Bala, "HVDC Light for large offshore wind farm integration," in *Power Electronics and Machines in Wind Applications (PEMWA), 2012 IEEE*, 2012, pp. 1-7.

CHAPTER 2

Operational Principles of FACTS Devices Using Two-level VSC

This chapter presents a detailed literature survey of the two-level and full-bridge voltage source converters (VSCs). The survey focuses on power electronic systems and other converter issues, including modulation techniques and application to FACTS devices, such as the STATCOM, SSSC, UPFC, IPFC/GUPFC, and back-to-back solutions. Operating principles of selected FACTS devices are explained and supported by simulations. Some of the control strategies established and observations drawn in this chapter are used in the subsequent chapters.

2.1 Background

The conventional AC power system has dominated electric energy transmission and distribution by its effectiveness and continence on the voltage amplitude adjustment, isolation and fault protection (with wide use of transformers and circuit breakers) [1]. But during long distance power transmission, the voltage may drop if reactive power is in short, which means the capacity of the transmission power line will be significantly discounted with length increase [2-7]. The fast developing power system decentralization and increasing consumer load diversity, forces the grid topology to be highly meshed [8-12]. These all necessitate the incorporation of power flow and power quality control which is implemented by FACTS controllers [13, 14]. VSC-FACTS devices such as the STATCOM, SSSC and UPFC are theoretically superior and promising in terms of power decoupling, power flow control range, response speed and accuracy [15-20]. They significantly improve power transmission line capacity utilization.

The two-level converter is the basic VSC topology for AC-DC and DC-AC power conversion, and employs self-commutated IGBT/IGCTs as power switches. With appropriate modulation, four-quadrant operation can be fulfilled and a low harmonic distorted voltage waveform with decoupled amplitude and phase angle can be generated. Then the full range control of active and reactive power can be implemented and decoupled; with lighter and smaller filtering passive elements than with the line-commutated-converter (LCC), which in turn improves system dynamic response [21, 22].

2.2 Two-level VSC Topology and Modulation

The three-phase two-level VSC topology is shown in Fig. 2-1, where, in each phase, the two switches conduct complementarily. Then relative to the mid-point of the DC-link, three-phase bipolar output voltage waveforms can be synthesized.

Two-level VSC modulation techniques have been intensively researched. In principle, all modulation methods aim to lower harmonic distortion in the output voltage and current, improve dc link utilization, and minimize switching losses, among which there should be a trade-off to achieve balanced converter performance under all operating conditions.

Generally, sinusoidal pulse width modulation (SPWM) generates a train of pulses with a voltage-second area the same as that of the reference signal over one

switching or fundamental period. Its downside is that the maximum linear modulation index is limited to 1pu, and the switching devices experience the carrier frequency. Third harmonic (triplen) injection SPWM (TSPWM) extends the maximum modulation index to 1.155pu, but inherent are all the other features of SPWM, and the introduced zero-sequence components in the phase voltage do not contribute to the three-phase load currents. Space vector modulation (SVM) is developed from the space vector representation of the inverter output voltage in the α-β plane. The dc voltage utilization is 1.155pu, and it offers additional flexibilities in terms of pulse placement and switching patterns selection, hence switching losses can be optimized. SVM is suitable for real-time and digital implementation. But it assumes a perfect three phase grid/load in terms of phase and magnitude. Selective harmonic elimination (SHE) controls the fundamental voltage and eliminates specific harmonics by directly calculating the switching instances. In this manner, it generates high quality output voltage at a lower switching frequency than other modulation methods, and a relatively high modulation index (exceeding 1.155pu) is achievable in three-phase systems [23-29].

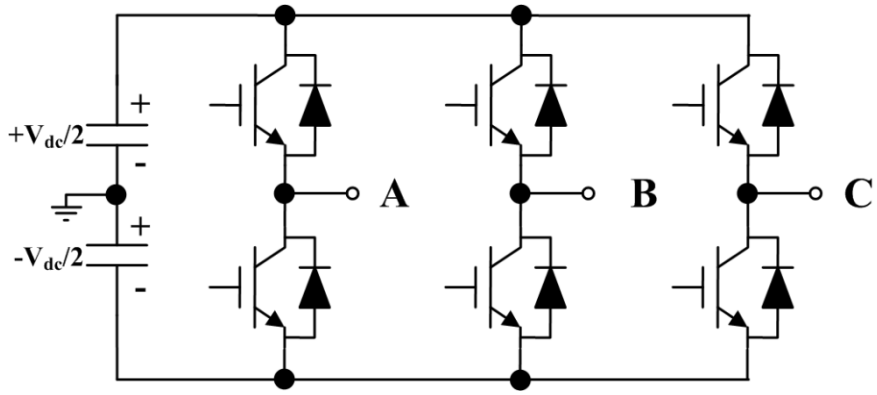


Fig. 2-1. Three-phase two-level VSC topology.

As a comparative study of the modulation techniques, the two-level VSC in Fig. 2-1 is employed in the inverter mode with the specifications listed in Table 2-1. Four modulation techniques including SPWM, TSPWM, SVM and SHE are analysed, where m_f represents the ratio of the switching frequency to fundamental frequency, and m_a is the modulation index [30-32].

If V_{1p} is the peak value of the line-to-line fundamental output voltage, the DC-link voltage utilization index λ, defined by (2.1), reflects the voltage transfer limit and is restricted to 1.1 for a square wave mode.

$$\lambda = \frac{V_{1p}}{V_{dc}} \tag{2.1}$$

The harmonic performance is usually evaluated by the total harmonic distortion (THD). However, low order harmonics contribute the most significant current component to the load in practise. So the weighted THD (WTHD) is employed in this section to indicate the effective quantity of harmonic contents in the output voltage waveform. (2.2) is the WTHD definition and an upper limit of the 75th order harmonic is used in this comparative study.

$$WTHD = \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{np}}{n}\right)^2} / V_{1p} \tag{2.2}$$

Table 2-1. Simulation results for different modulation methods of two-level VSC.

Three-Phase Two-level VSC, Vdc=100V, fo=50Hz										
ITEMS	*SPWM(mf=30, ma=1)*		*TSPWM(mf=30, ma=1.1547)*		*SVM(mf=30, ma=1, Pattern 2 sequence)*		*SHE(ma=1.16, 9 switching angles)*		*Square-Wave Inversion*	
fsw (kHz)	1.5		1.5		1.5		0.95		0.05	
λ(V 1p/V dc)	0.866		0.9977		0.9977		1.0046		1.1026	
THD (%)	68.62		52.62		52.55		56.66		31.09	
First 8 Significant Harmonics on base of V 1p	*Order*	*Vp (%)*	*Order*	*Vp (%)*	*Order*	*Vp (%)*	*Order*	*Vp (%)*	*Order*	*Vp (%)*
	26	1.8	26	10.43	17	1.4	29	4.61	5	20
	28	31.79	28	25.94	19	1.95	31	2.01	7	14.28
	32	31.79	32	25.94	23	5.44	35	30.01	11	9.09
	34	1.83	34	10.41	25	11.92	37	29.55	13	7.69
	55	3.35	53	3.54	29	23.37	41	9.11	17	5.88
	59	18.15	55	10.27	31	23.38	43	4.53	19	5.26
	61	18.13	59	7.55	35	11.89	47	1.19	23	4.35
	65	3.3	61	7.57	37	5.38	61	3.6	25	4
WTHD (%)	1.57		1.36		1.35		1.24		4.64	

The VSC specification with its four modulation strategies and the detailed quantitative results including the DC voltage utilization, for the first 8 significant harmonics percentages with respect to the fundamental, and the WTHD, are shown in Table 2-1. For the modulation techniques at maximum linear output, the various positions and widths of the rectangular trains in the synthesized voltage waveforms contribute to the different maximum fundamental voltage and harmonic spectra, as indicated in Fig. 2-2 and Fig. 2-3, respectively. In Fig. 2-3, the DC bus voltage is the base used to normalize the spectral component magnitudes, thereby allowing performance comparison between each modulation method.

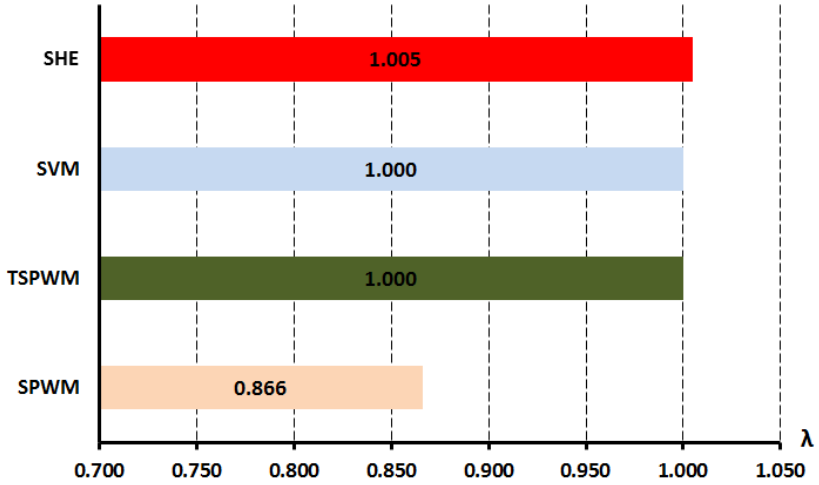


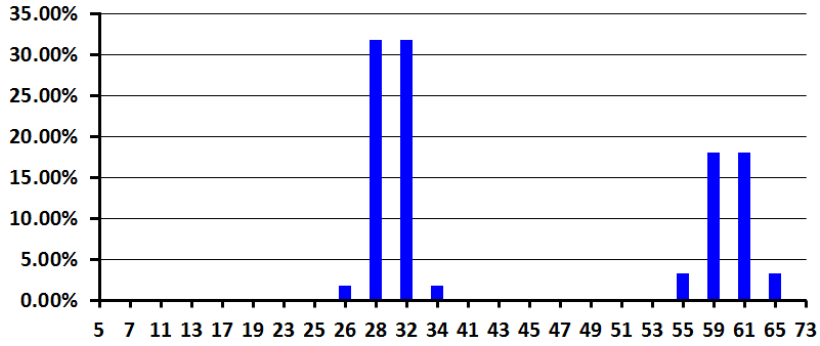
Fig. 2-2. Maximum peak value of the output line-to-line voltage for 4 different modulation methods.

i) SPWM: From Fig. 2-2, the DC voltage utilization of basic SPWM is 0.866, and Fig. 2-3(a) shows the corresponding spectrum of output line-to-line voltage. According to Table 2-1, the WTHD of SPWM is 1.57%, and all the significant harmonics are concentrated around the sidebands of the switching frequency components.

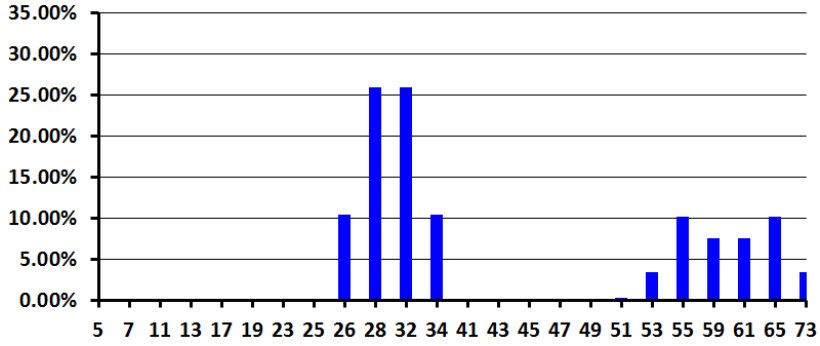
ii) TSPWM: In Fig. 2-2 and Table 2-1, optimal injection of the 3rd harmonic into the modulating wave extends the linear modulation index to 1.155 that of SPWM and the output 3rd harmonics in each phase cancel on the line-to-line output voltage in a three-phase system. The WTHD is decreased to 1.36% due to the increased fundamental voltage. Harmonic distribution is shown in Fig. 2-3(b).

iii) SVM: SVM can generate waveforms with a same maximum fundamental output as TSPWM, as shown in Fig. 2-2 and Table 2-1. The corresponding WTHD is 1.35%. However, there will be deviation from the ideal situation as the sidebands around the first switching frequency manifest as low order harmonics in Fig. 2-3(c).

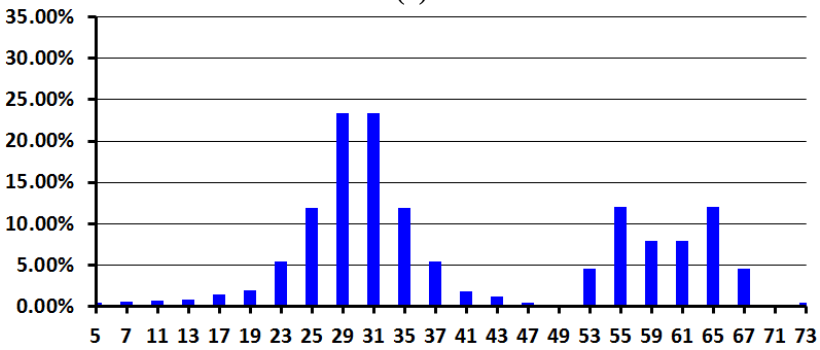
iv) SHE: The WTHD under SHE modulation with an equivalent frequency of 19 times the fundamental (which is lower than for the other methods) is 1.24% and the first significant harmonics are the 29th and 31st, as shown in Table 2-1 and Fig. 2-3(d). In SHE, by defining the maximum linear modulation index to 1.16, which is slightly higher than that of SVM and TSPWM, nine controllable switching angles eliminate up to the 25th order harmonic.



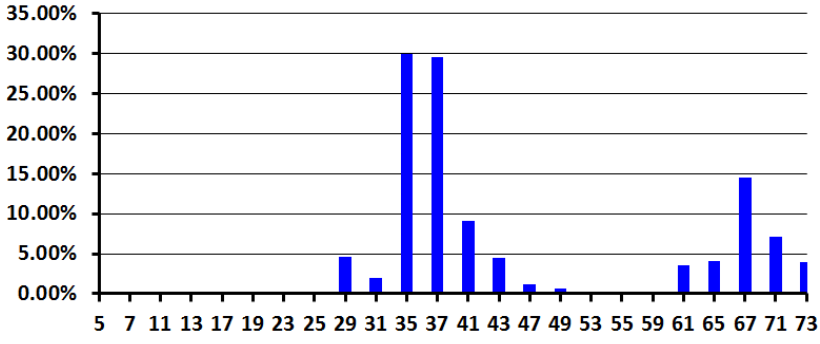
(a)



(b)



(c)



(d)

Fig. 2-3. Line-to-line voltage spectra for different modulation methods (peak value normalized by V_{dc}) versus Harmonic order: (a) SPWM (mf=30, ma=1); (b) TSPWM (mf=30, ma=1.1547); (c) SVM (mf=30, ma=1.1547); and (d) SHE (9 angles, ma=1.16).

Fig. 2-4 shows output line-to-line voltage THD varying with the modulation index for SPWM, TSPWM, SVM and SHE. The switching frequency for SPWM, TSPWM

and SVM are the same; while SHE employs a lower switching frequency (dependant on the number of switching angles). As is shown, the THD decreases with increasing modulation index.

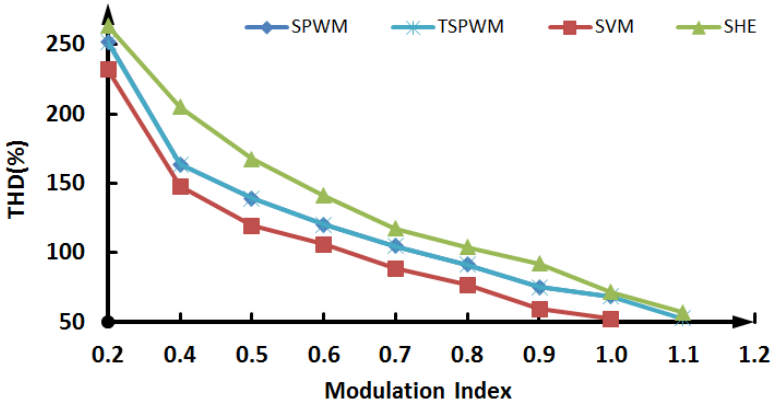


Fig. 2-4. Total Harmonic Distortion (THD) versus Modulation index.

The total number of commutations per cycle directly influences device switching losses. The multiple ways to achieve fixed composite space vector output offers opportunity to optimize the switching sequence in SVM, hence switching losses can be minimize. SHE offers the lowest switching frequency, while the harmonic performance is better than that of the other modulation methods. However, generally, switching losses are determined by not only the switching frequency but also the switching location distribution and the load current at each switching instance.

Realization of each modulation technique can be either in real-time or through a pre-calculated look-up table. The real-time or on-line running mode can be supplied by directly observed variables, allowing a flexible control strategy to correct deviations. However, significant real-time calculation increases processor requirements and any deviation from the real value can introduce output distortion, involving low order harmonics. A look-up table or an off-line mode employs several pre-computed local-data tables to avoid the on-line calculations, making the control decisions instantaneous. However, reduced control flexibility becomes the penalty and a large quantity of data has to be downloaded into the read-only memory before the converter activation.

When incorporating feedback to control the converter, the running mode of each modulation method influences the practicality and realization complexity due to the principle of modulating itself. Generally, algorithm complexity and commercial processor speeds are considered.

For SPWM, TSPWM and SVM, the output voltage amplitude is linearly dependent on modulation index over a wide range, making control calculation simple and efficient. Given available processor speeds, an on-line operational mode is viable and able to monitor all status parameter and variables. However, for SHE, significant arithmetic processing is needed to implement the algorithm, so an off-line mode with look-up tables and interpolation, is preferred. The switching instances for different modulation indices are stored as local data so that a specific output voltage can be obtained by an interpolation method.

2.3 Full-bridge VSC Topology and Modulation

For high voltage, the three-phase two-level converter in Fig. 2-1 has several disadvantages, among which the low DC-link voltage utilization becomes a constraint. It requires either a high DC-link voltage or a bulky step-up transformer for voltage adaption.

The full-bridge topology in Fig. 2-5, consisting of two legs per phase, is able to generate a maximum of twice the output voltage of the conventional two-level converter, by reversing the output voltage polarity. Also, this converter is able to generate '+1', '0' and '-1' voltage levels, reducing the THD. The disadvantage of the full-bridge topology, other than more semiconductors, is the need of independent transformer windings for the multi-phase system in Fig. 2-5.

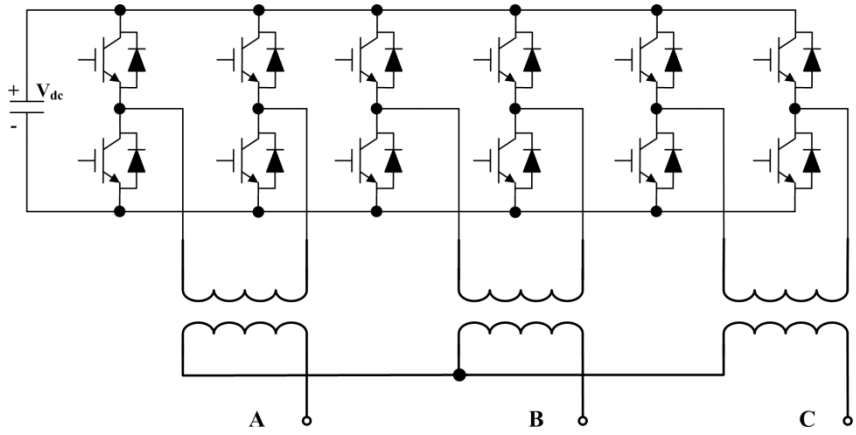


Fig. 2-5. Three-phase full-bridge VSC with transformer.

For the full-bridge, since the output voltage polarity can be reversed, both unipolar and bipolar modulation can be implemented. The single-phase full-bridge converter is simulated under various modulation methods to evaluate its performance [33].

i. Bipolar SPWM with mf=30 and ma=1

The bipolar SPWM (Bi-SPWM) modulates two legs at same switching frequency and both positive and negative voltage levels are synthesized in one switching period. From Fig. 2-6, the calculated *WTHD* is 2.59% and the maximum fundamental output is equal to *Vdc* for a Bi-SPWM modulated singe-phase full-bridge converter.

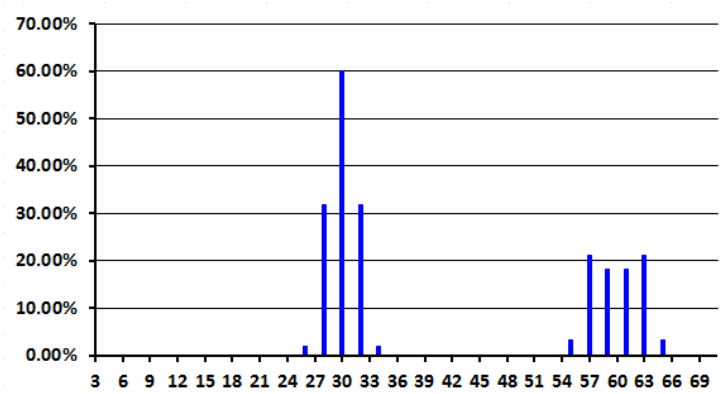


Fig. 2-6. Harmonics distribution normalized by fundamental *vs* Harmonic order for Bi-SPWM.

ii. Unipolar SPWM with mf=30 and ma=1

The maximum fundamental output voltage using the unipolar SPWM (Un-SPWM) still equals *Vdc*. The simulated harmonic result is displayed in Fig. 2-7, from which the *WTHD* is calculated to be 1.21%.

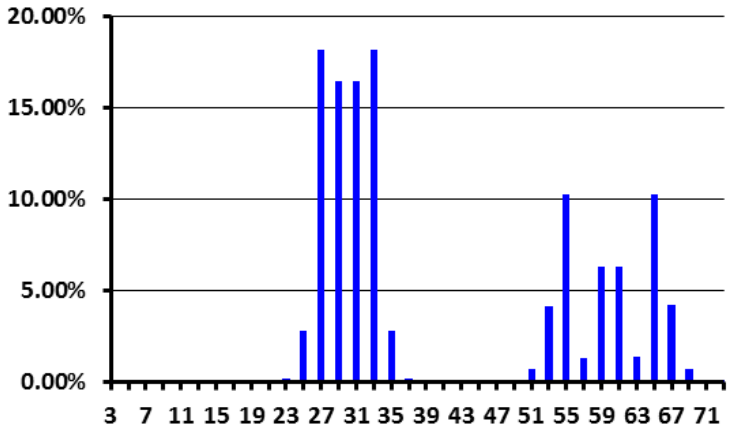


Fig. 2-7. Harmonics distribution normalized by fundamental *vs* Harmonic order for Un-SPWM.

The distribution of the switching frequency harmonics and its sidebands in Un-SPWM is different from that in Bi-SPWM. For the latter, both positive and negative voltages are generated in each switching period, but for the former, one leg is operated at fundamental frequency, while the other leg is switched at the switching frequency to obtain {‘+1’, ‘0’} in positive half-cycle and {‘-1’, ‘0’} in negative half-cycle. Hence, lower THD and lower switching losses are achieved with Un-SPWM than with Bi-SPWM.

iii. Unipolar SPWM with Frequency Doubling – SPWM-FD (mf=15, ma=1)

Traditional bipolar SPWM supplies an output voltage with bipolar rectangular trains in one leg. Here, frequency doubling, employing a pair of phase-inverting modulating waveforms or carriers to control each leg separately, achieves a unipolar voltage waveform with similar output quality as common unipolar SPWM but with half the switching frequency.

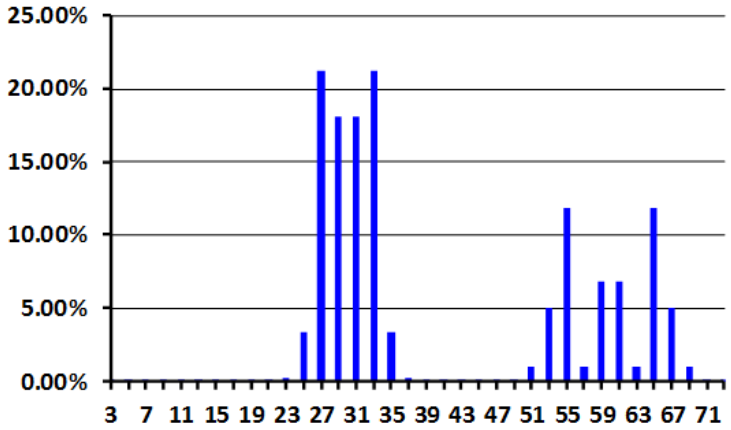


Fig. 2-8. Harmonics distribution normalized by fundamental *vs* Harmonic order for SPWM-FD.

Simulation at a modulation index of 1 achieve a maximum output voltage equal to *Vdc*. Fig. 2-8 shows each voltage harmonic percentage normalized by the fundamental voltage. These values can be used directly in the calculation of *WTHD*, and the result is 1.38%. With frequency doubling, the high order harmonic distribution is similar to that in traditional Un-SPWM.

iv. Bipolar SHE with 9 Controllable Switching Angles

The bipolar pattern of SHE (Bi-SHE) is employed to control the low order harmonics to be zero and achieve a higher fundamental voltage output in this simulation. Fig. 2-9 gives a *WTHD* of 3.28% when up to 75th order harmonics are considered, however, since Bi-SHE with 9 switching angles is able to control the fundamental voltage plus the first 8 harmonics components, it is expected the WTHD within this range will be lower than SPWM methods. In the single-phase full-bridge system with Bi-SHE, the fundamental component is marginally improved due to the necessity of 3rd harmonic elimination; while in a three-phase system as shown by Fig. 2-5, the DC voltage utilization can be improved because 3rd order harmonics cancel in the line-to-line output voltage.

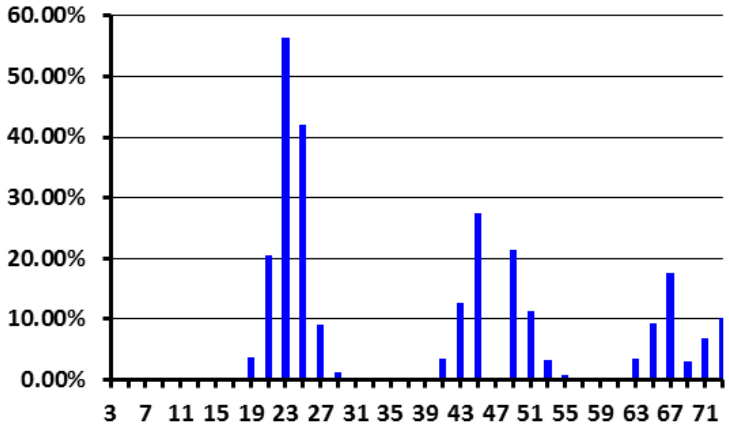


Fig. 2-9. Harmonics distribution normalized by fundamental *vs* Harmonic order for Bi-SHE.

v. Unipolar SHE with 9 Controllable Switching Angles

Compared to Bi-SHE, unipolar SHE modulation (Un-SHE) generates a lower *WTHD* of 1.68% with a similar fundamental output voltage peak value, which agrees with the theoretical analysis.

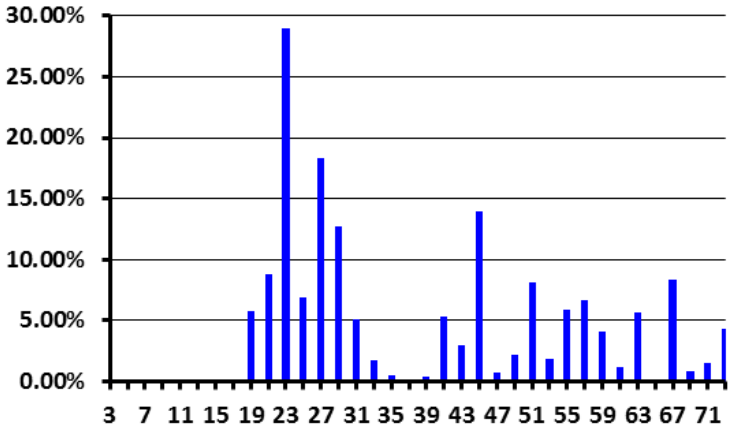


Fig. 2-10. Harmonics distribution normalized by fundamental *vs* Harmonic order for Uni-SHE.

As is explained, in a three-phase full-bridge system, SHE has the capability to extend the fundamental voltage component and suppress the selected lower order harmonics. Both TSPWM, (bipolar or unipolar), and SVM with two-level or three-level vector space are expected to be viable and superior in improving DC voltage utilization.

2.4 Operating Principle of Typical FACTS Devices

In this section, system level operational principles for typical FACTS devices including STATCOM, SSSC, DVR, UPFC, IPFC, GUPFC and HVDC system, are analysed based on a three-phase two-level VSC in Fig. 2-1. VSC-based FACTS devices can solve many grid problems, such as reactive power compensation, voltage

control, and power flow control, which are verified in this section by illustrative examples.

2.4.1 Static Synchronous Compensator (STATCOM)

A STATCOM using a three-phase two-level VSC is shown in Fig. 2-11(a), and its equivalent circuit is interpreted by Fig. 2-11(b), where L is the interfacing reactor leakage inductance, $\boldsymbol{V_{pcc}}$ is the grid voltage at the point of common coupling (PCC) (referred to the converter side before transformer is $\boldsymbol{V_g}$), and the vector $\boldsymbol{V_c}$ represents the VSC output voltage with controllable phase angle and amplitude.

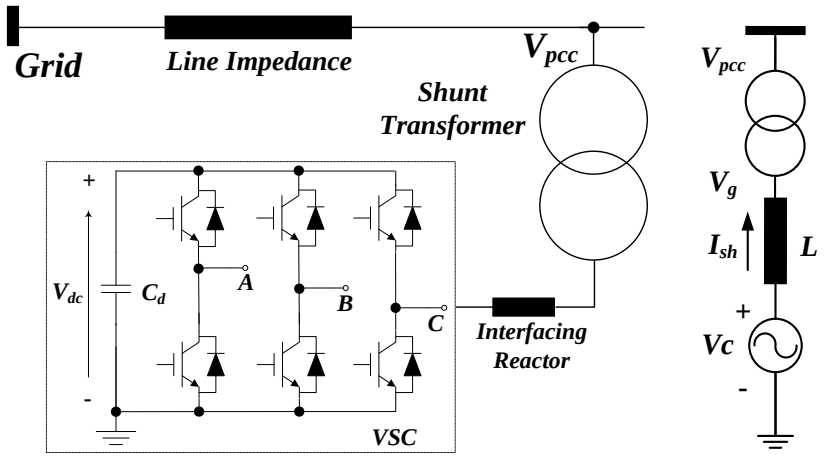


Fig. 2-11. STATCOM diagram: (a) device level model using two-level VSC and (b) system level equivalent circuit.

The STATCOM is mainly used as a reactive power and voltage amplitude controller and the isolated DC capacitor is employed to support the DC link voltage. The DC voltage is stable, since there is no active power exchange between STATCOM and the grid, if all losses are neglected. Assuming $\boldsymbol{V_g}$ is the input of the phase-locked-loop (PLL); its quadrature component and the shunt current $\boldsymbol{i_{sh}}$ projection onto the direct axes are always equal to zero; therefore, the shunt current and reactive power exchange can be expressed by (2.3), where ω is the angular frequency of grid voltage; P_{sh} and Q_{sh} are the active and reactive power exchange respectively [34-36].

$$\begin{cases} I_{sh,d}=0;\ I_{sh,q}=\dfrac{V_{cd}-V_{gd}}{\omega L} \\ P_{sh}=0;\ Q_{sh}=\dfrac{V_{gd}\cdot(V_{cd}-V_{gd})}{\omega L} \end{cases} \tag{2.3}$$

The STATCOM injects positive shunt current, thus capacitive reactive power, to the grid when $V_{cd}>V_{gd}$; while negative shunt current, that is, inductive reactive power

will be absorbed by STATCOM when $V_{cd}<V_{gd}$. The phasor diagrams for the two cases are clarified by Fig. 2-12.

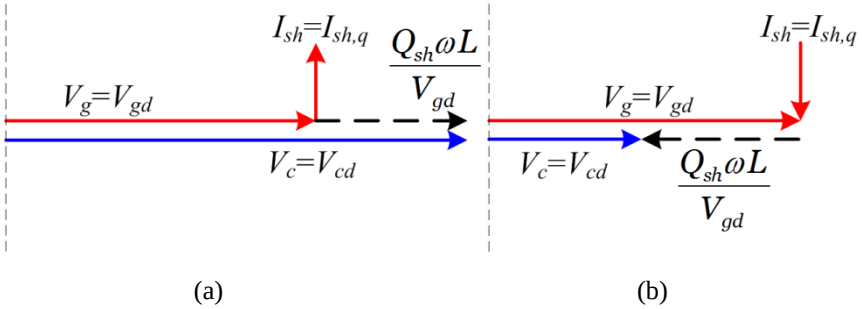


Fig. 2-12. Phasor diagram of STATCOM vectors when: (a) STATCOM generates capacitive reactive power to the grid and (b) STATCOM absorbs inductive reactive power from the grid.

For STATCOM inductive reactive power absorption, the control range boundary is usually defined by the current limit of the power semiconductor devices since the VSC output voltage vector can be far lower than the grid voltage; however, for capacitive reactive power generation, typically, the limited voltage amplitude synthesized by the VSC will contribute to determine the maximum injected reactive power before the switches reach their current limits. Therefore, the reactive power control range of the STATCOM is usually asymmetrical. In some situations, the DC bus of the VSC can be connected to active sources such as a battery bank. Then the STATCOM can also influence grid active power. The overall power control range, considering practical limitations, are shown in Fig. 2-13.

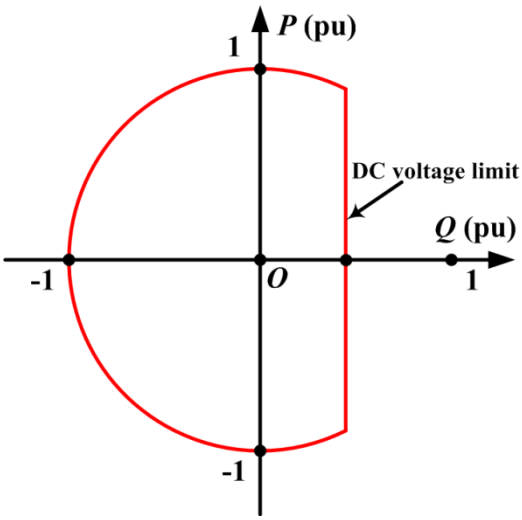


Fig. 2-13. The overall power flow control range of STATCOM considering both the VSC device current and synthesized voltage amplitude limits.

The two-layer control strategy for the STATCOM in synchronous reference frame (SRF) is summarized in Fig. 2-14, where the PCC voltage is the PLL input to get the reference angle θ. Using Park transformation, the direct-quadrature components of the shunt current can be achieved as i_{dq} and their reference values in the d-q frame are generated by the outer layer DC voltage controller and reactive power (or PCC voltage amplitude) controller respectively[15, 37].

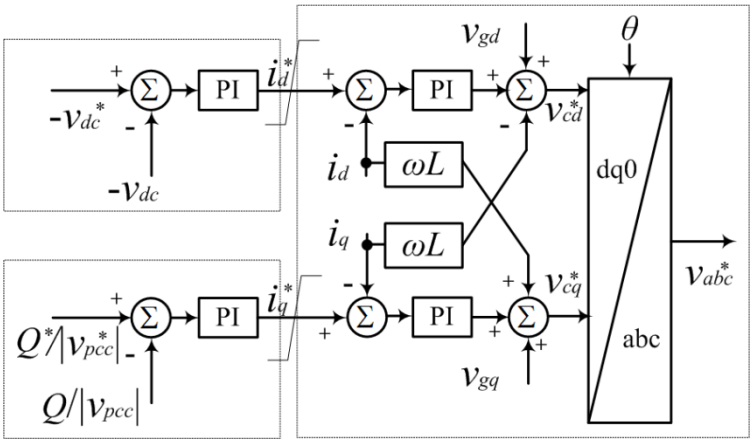


Fig. 2-14. Control diagram of two-level VSC based STATCOM in SRF.

If δ is the duty cycle of the upper switches in the two-level VSC, by manipulation of time domain state space equations with Park transformation, the d-q frame differential equations for the ac side are obtained in (2.4), in a time-invariant form. The coupling terms $i_{d,q}$ and disturbance terms $v_{gd,q}$ will influence the dynamic performance of the VSC system, thus, a feed-forward method as in (2.5) is introduced into the control block to decouple the d-q components and improve the response speed. $\gamma_{d,q}$ represents the output value of the $i_{d,q}$ compensator (such as a proportional and integral, PI controller).

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = -\frac{r}{L}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega\begin{bmatrix} i_q \\ -i_d \end{bmatrix} + \frac{v_{dc}}{L}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{2.4}$$

$$\begin{cases} v_{cd}^* = \gamma_d + v_{gd} - \omega L i_q \\ v_{cq}^* = \gamma_q + v_{gq} + \omega L i_d \end{cases} \tag{2.5}$$

In order to design the DC voltage controller outer layer, the converter active power consumption should be considered. From the law of energy conservation, the active power should be balanced between the DC and AC sides as interpreted by (2.6). Since the converter output voltage has a small phase shift relative to PCC voltage, $v_{cq} \approx 0$ is reasonably assumed. Then the DC voltage differential equation is expressed

as in (2.7). From this analysis, the direct shunt current reference can be produced by the outer layer DC voltage controller as in (2.8), where the PI method is used with parameters of $\{k_{dcp}, k_{dci}\}$.

$$-v_{dc}C_d\frac{dv_{dc}}{dt} = v_{cd}i_d + v_{cq}i_q \tag{2.6}$$

$$\frac{dv_{dc}}{dt} = -\frac{v_{cd}i_d + v_{cq}i_q}{v_{dc}C_d} \approx -\frac{d_d i_d}{C_d} \tag{2.7}$$

$$i_d^* = -[k_{dcp}(v_{dc}^* - v_{dc}) + k_{dci}\int(v_{dc}^* - v_{dc})dt] \tag{2.8}$$

According to (2.3), the quadrature current reference can be obtained by the outer layer PCC voltage amplitude controller or the reactive power controller as shown in (2.9) and Fig. 2-14. $\{k_{acp}, k_{aci}\}$ and $\{k_{Qp}, k_{Qi}\}$ represent the corresponding pairs of controller PI gains.

$$\begin{aligned} & i_q^* = k_{acp}(\left|v_{pcc}^*\right| - \left|v_{pcc}\right|) + k_{aci}\int(\left|v_{pcc}^*\right| - \left|v_{pcc}\right|)dt \\ or \quad & i_q^* = k_{Qp}(Q^* - Q) + k_{Qi}\int(Q^* - Q)dt \end{aligned} \tag{2.9}$$

As an illustration, a two-level VSC based STATCOM shown in Fig. 2-11(a), with specifications in Table 2-2, is simulated in SIMULINK/MATLAB. The interfacing transformer and AC transmission grid parameters are shown in Table 2-3 and Table 2-4 respectively.

Table 2-2. Specifications of VSC model in STATCOM.

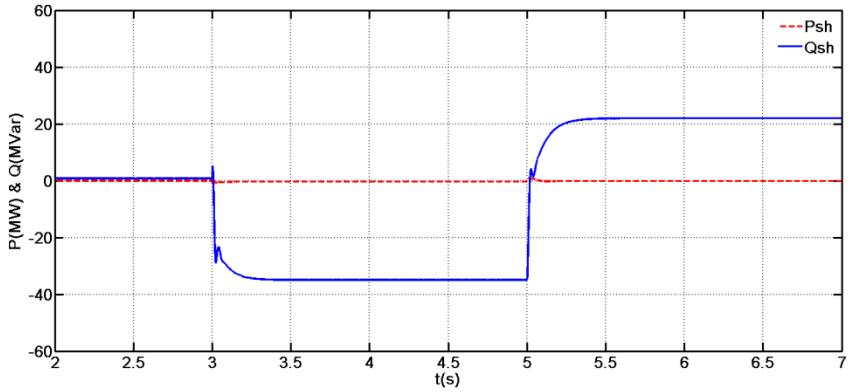
Two-level VSC	
Apparent power rating S_{con}	40MVA
DC link voltage V_{dc}	41kV
DC link capacitor C_d	2200μF
Shunt inductor L_{sh}	12mH
Converter switching frequency	2.5kHz

Table 2-3. Specifications of transformer installation.

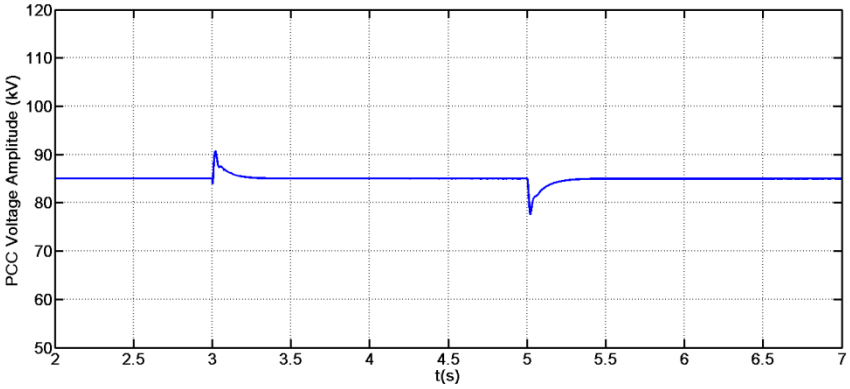
Shunt transformer	
Power capacity	40MVA
Voltage ratio	110kV/17.32kV
Per unit impedance	(0.0005+j0.08)

Table 2-4. AC transmission system parameters.

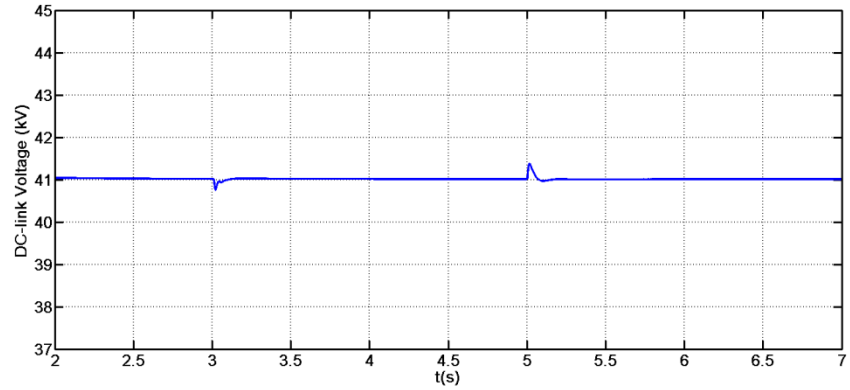
Grid parameters for shunt compensation	
Nominal line voltage	110kV(RMS)
Line impedance	(0.466+j9.322)


Psh
Qsh
P(MW) & Q(MVar)
t(s)

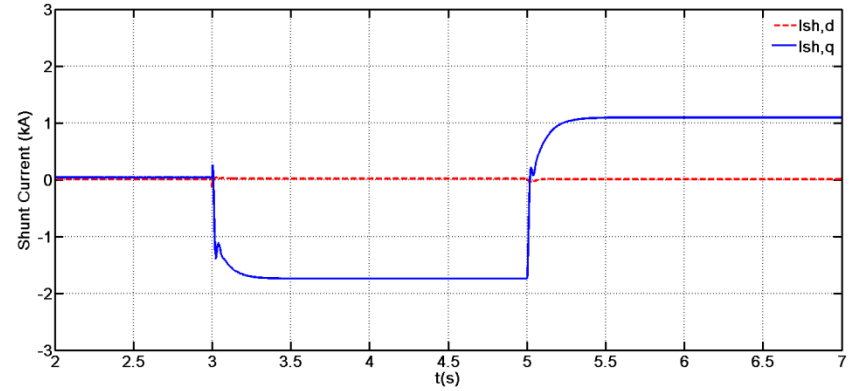
(a)


PCC Voltage Amplitude (kV)
t(s)

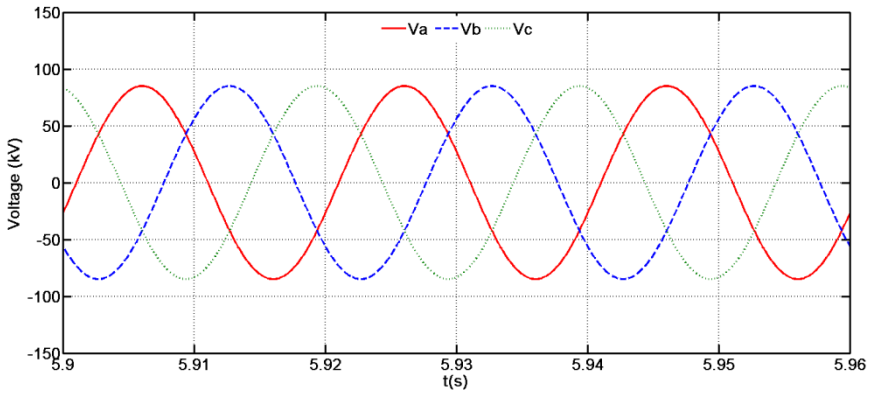
(b)


DC-link Voltage (kV)
t(s)

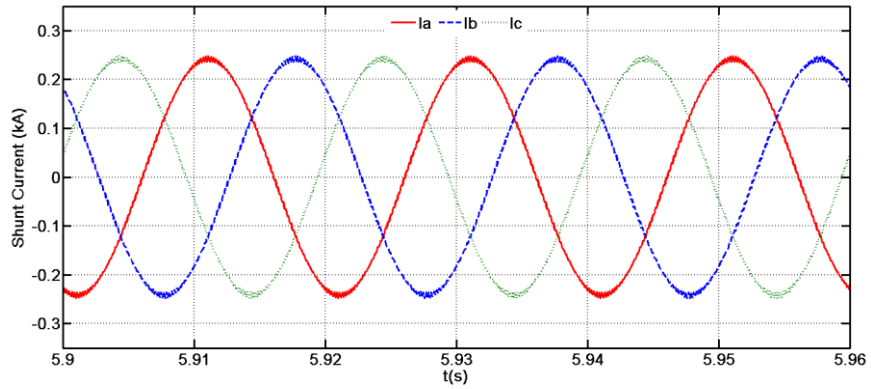
(c)


Ish,d
Ish,q
Shunt Current (kA)
t(s)

(d)



(e)



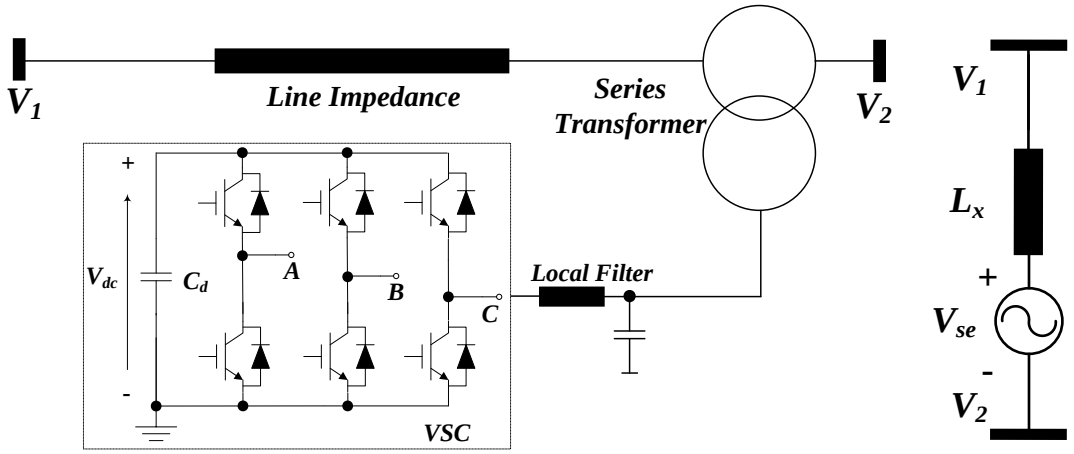
(f)

Fig. 2-15. Simulation for STATCOM in voltage supporting mode: (a) active and reactive power exchange between STATCOM and grid; (b) PCC voltage amplitude during load transitions; (c) DC-link voltage of STATCOM; (d) shunt current in *d-q* frame; (e) time domain waveform of PCC voltage; and (e) time domain waveform of shunt current.

In this simulation, the STATCOM operates in a voltage supporting mode and the shunt current positive direction is from the converter to the grid as defined in Fig. 2-11(b). The PCC load power flow is set to increase by 20MW-*j*40MVAr at *t*=3s and 10MW+*j*60MVAr at *t*=5s. From Fig. 2-15(a), the STATCOM absorbs reactive power during 3-5s; while it generates positive reactive power into the grid during 5-7s to support the PCC voltage. Thus, the PCC voltage amplitude can be maintained constant during load transitions as shown in Fig. 2-15(b). Fig. 2-15(c) is the voltage of the STATCOM DC-link capacitor that is maintained constant during disturbances and the *d-q* components of the shunt current transit, shown in Fig. 2-15(d), regulate the injected reactive power. Time domain waveforms of the PCC voltage and shunt branch current are displayed in Fig. 2-15(e) and Fig. 2-15(f) respectively.

2.4.2 Static Synchronous Series Compensator (SSSC) & Dynamic Voltage Restorer (DVR)

The two-level VSC based SSSC installation is shown in Fig. 2-16(a) and Fig. 2-16(b) is the equivalent circuit. $\boldsymbol{V_{se}}$ represents the series injected voltage vector and L_x is the power line reactance. During ideal conditions, the SSSC exchanges zero active power with the grid, which means the series injected voltage vector should always be orthogonal to the line current. If line current is used as the PLL system input, the injected voltage and line current can be achieved as in (2.10). The line current is expressed by (2.11), where the SSSC functions as variable reactance. This means the injected current introduced by SSSC is always aligned with the grid line current, either positive or negative. Therefore, the incremental active power and reactive power are in proportion that is depended on the bus voltage *d-q* axes values. Accordingly, the active power flow is chosen as the control target during typical SSSC operation, and its increment can be calculated by (2.12). The power exchange between the grid and SSSC device in steady state is shown in (2.13).



(a) (b)

Fig. 2-16. SSSC diagrams: (a) device level model using two-level VSC and (b) system level equivalent circuit.

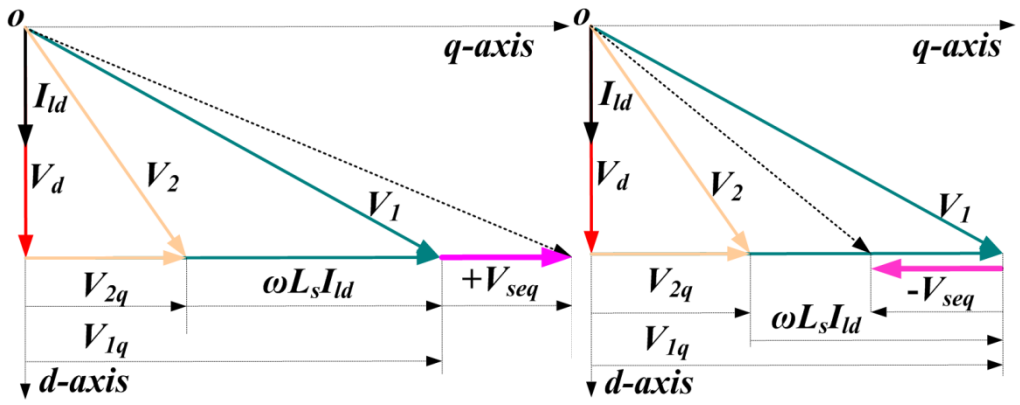
$$\begin{cases} V_{sed} = 0;\ I_{lq} = 0; V_{1d} = V_{2d} = V_d \\ I_{ld} = \dfrac{V_{1q} - V_{2q} - V_{seq}}{\omega L_s};\ I_{lq} = 0 \end{cases} \tag{2.10}$$

$$\begin{cases} I_{ld} = \dfrac{V_{1q} - V_{2q}}{\omega L_s + Z_s} \\ Z_s = \dfrac{V_{seq}}{I_{ld}} \end{cases} \tag{2.11}$$

$$\Delta P = -\frac{V_d \cdot V_{seq}}{\omega L_s} \tag{2.12}$$

$$\begin{cases} P_{se} = 0 \\ Q_{se} = i_{ld} \cdot V_{seq} \end{cases} \tag{2.13}$$

The SSSC phasor diagram is interpreted by Fig. 2-17. When the series inserted voltage increases the net value of the voltage vectors quadrature components, SSSC can augment the power flow transmission ability of the power line, see Fig. 2-17(a); while if the SSSC contributes a negative value to the grid voltage to improve the effective line reactance, the power flow will be decreased as in Fig. 2-17(b).



(a) (b)

Fig. 2-17. Phasor diagram of SSSC vectors when: (a) SSSC increase the power flow and (b) SSSC decreases the power flow.

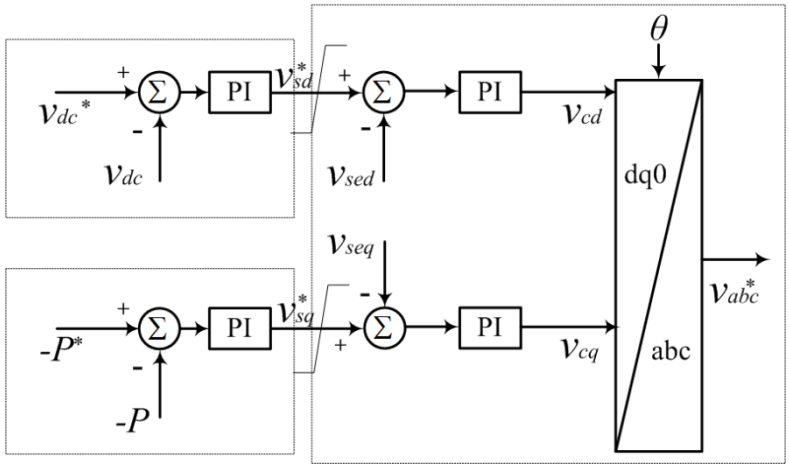


Fig. 2-18. Control diagram of two-level VSC based SSSC in SRF.

In practise, a small amount of active power is absorbed by SSSC from the grid to because of internal losses and to maintain the DC-link voltage. The dynamic relationship can be written as (2.14) based on the energy conservation law. Also,

from (2.12), the grid active power flow is directly regulated by the quadrature component of the series injected voltage. Now the SSSC control strategy is clarified by Fig. 2-18. The *d*-*q* components references of the SSSC series injected voltage can be obtained by (2.15), where $\{m_{dcp}, m_{dci}\}$ and $\{m_{Pp}, m_{Pi}\}$ are the corresponding controller pairs [38, 39].

$$\frac{dv_{dc}}{dt} = \frac{v_{sd}i_{ld} + v_{sq}i_{lq}}{v_{dc}C_d} = \frac{v_{sd}i_{ld}}{C_d} \tag{2.14}$$

$$\begin{cases} v_{sed}^{*} = m_{dcp}(v_{dc}^{*} - v_{dc}) + m_{dci}\int(v_{dc}^{*} - v_{dc})dt \\ v_{seq}^{*} = -[m_{Pp}(P^{*} - P) + m_{Pi}\int(P^{*} - P)dt] \end{cases} \tag{2.15}$$

To verify this analysis, the SSSC based power flow control is simulated with the specifications in Table 2-5 to Table 2-7. The active power flow command is set to 300MW initially, and stepped up 40MW at *t*=3. Then, the reference is progressively increased by 20MW at *t*=4s and *t*=5s.

Table 2-5. Specifications of VSC model in SSSC.

Two-level VSC	
Apparent power rating S_{con}	20MVA
DC link voltage V_{dc}	41kV
DC link capacitor C_d	2200μF
Filtering inductor L_f	12mH
Filtering capacitor C_f	80μF
Converter switching frequency	2.5kHz

Table 2-6. Specifications of transformer installations.

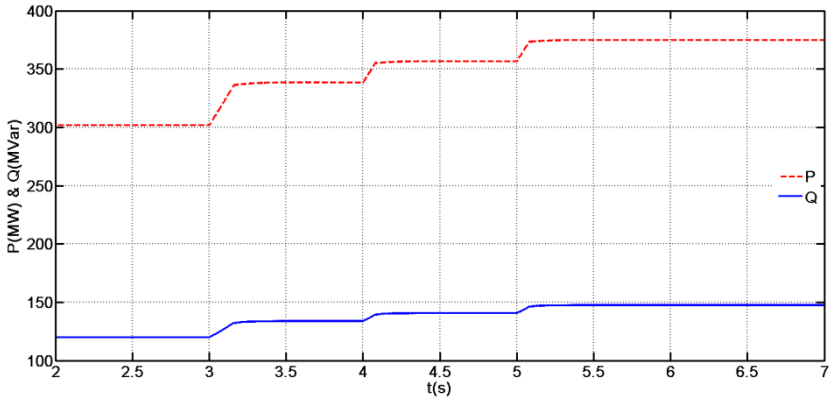
Series transformer	
Power capacity	20MVA
Voltage ratio	20kV/3.9kV
Per unit impedance	(0.0002+j0.05)

Table 2-7. AC transmission system parameters.

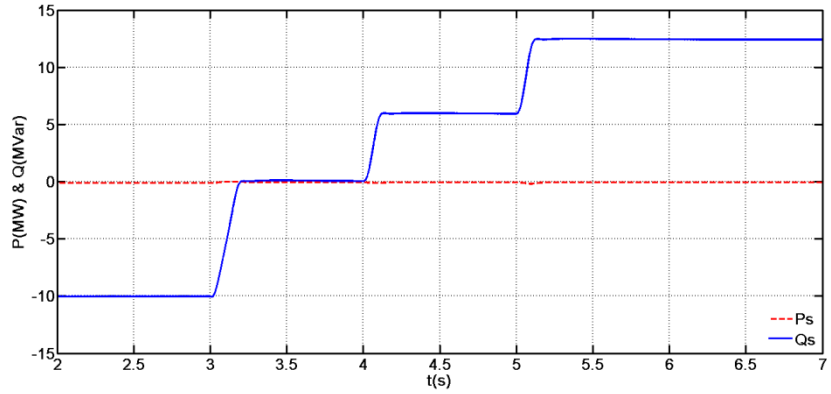
Grid parameters for series compensation	
Nominal line voltage	347kV(RMS)
Line impedance	(0.466+j9.322)

The simulated results are displayed in Fig. 2-19. The actual active power controlled by the SSSC tracks the reference smoothly, from Fig. 2-19(a). Fig. 2-19(b) and (c) show the corresponding power exchange from the SSSC to the grid and the series injected voltage in the *d*-*q* frame, respectively. In Fig. 2-19(d), the time domain waveforms of the SSSC injected voltage and the line current for phase *a* are nearly perpendicular since zero active power is exchanged between the SSSC and the grid if

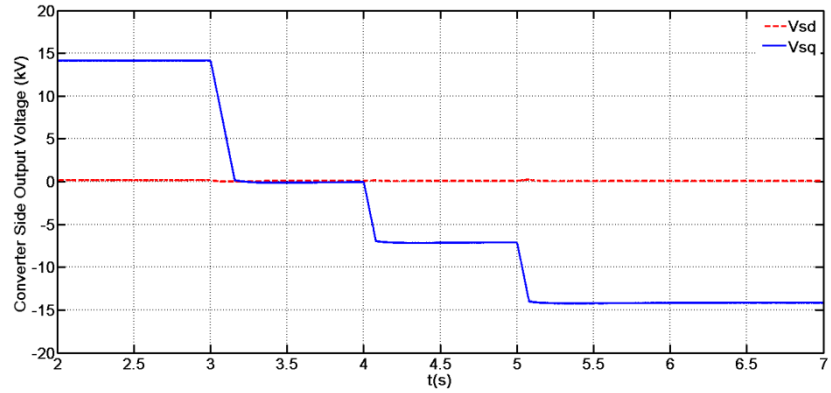
the internal losses are neglected. The SSSC capacitor bank DC-link voltage is maintained constant during the step transitions, from Fig. 2-19(e).



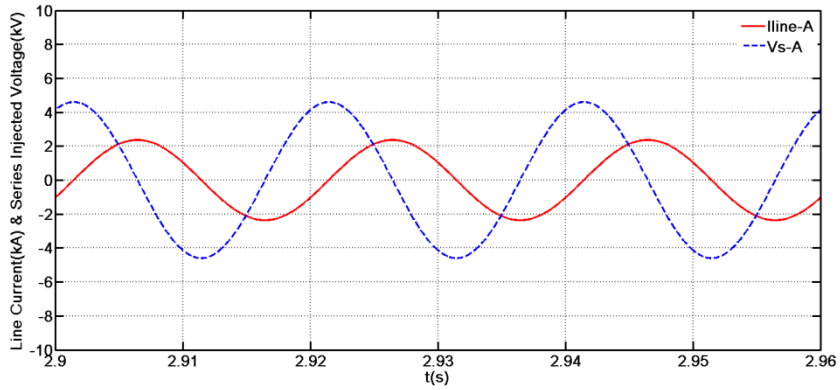
(a)



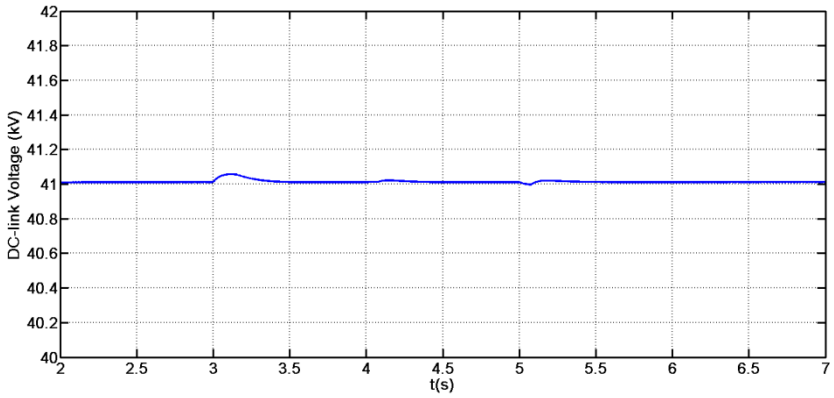
(b)



(c)



(d)



(e)

Fig. 2-19. SSSC simulation for active power flow control: (a) active and reactive power transition in the power line; (b) active and reactive power exchange between SSSC and grid; (c) converter output voltage in *d-q* frame; (d) time domain waveforms of the series injected voltage and grid line current; and (e) DC-link voltage of SSSC during step changes.

At the distribution level, the VSC based series compensation device is termed a DVR. It functions in a voltage control mode and the DC-link is connected to active sources as in Fig. 2-20 to generate an independent voltage output, used for voltage compensation during local in feed problems such as the power flow flicker, load unbalance or voltage amplitude sag/swell, etc [40, 41].

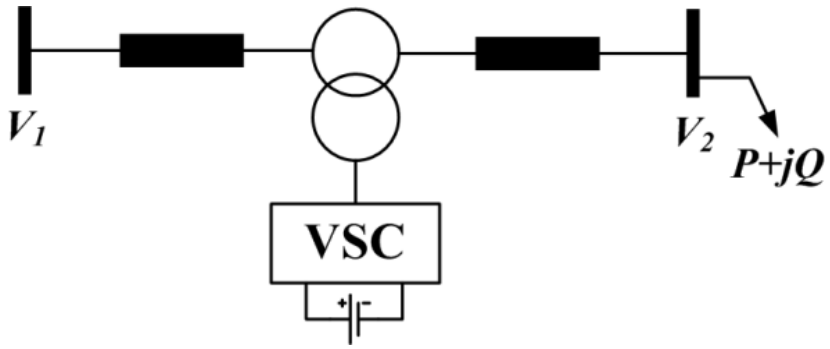


Fig. 2-20. Diagram of the DVR installed for voltage compensation.

The phasor diagram of the vectors is drawn in Fig. 2-21. The DVR output voltage can have an arbitrary angle relative to the grid current, thus is able to contribute both active and reactive power to restore the voltage quality on a critical bus.

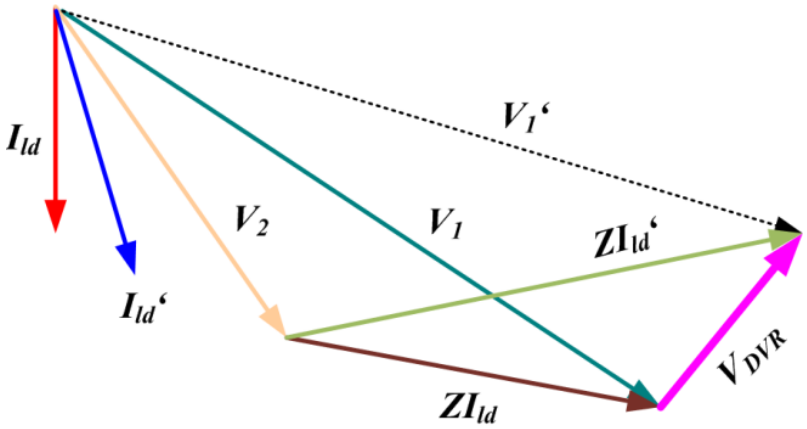


Fig. 2-21. Phasor diagram of vectors in a DVR.

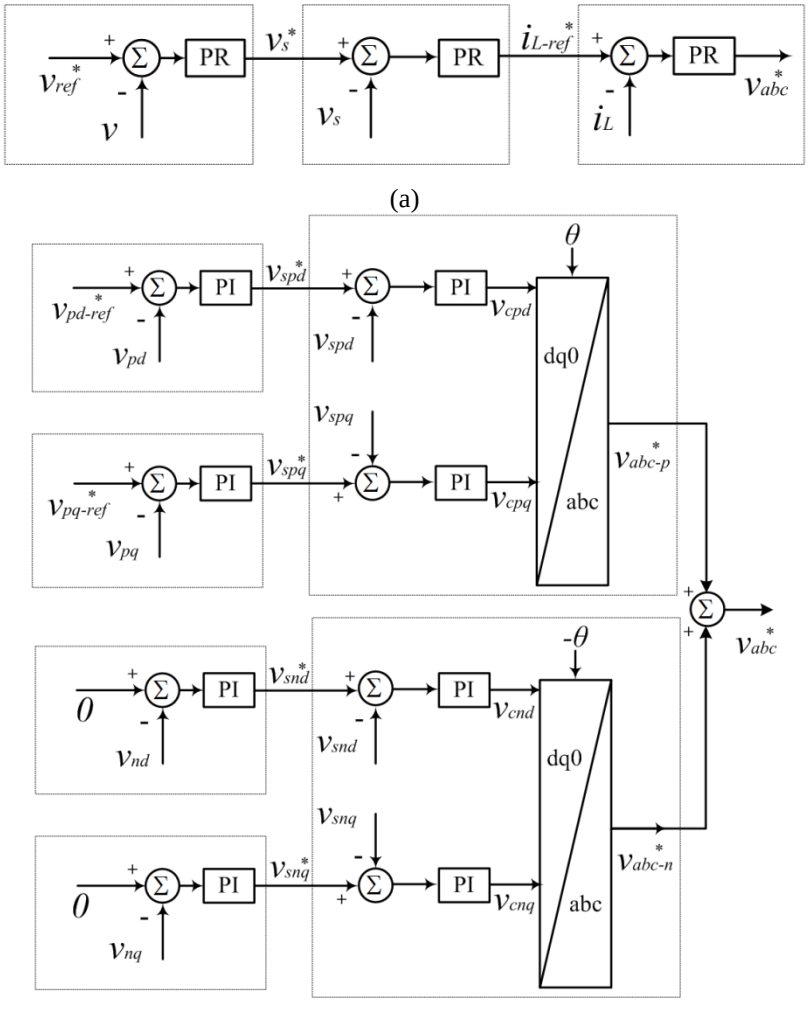


Fig. 2-22. Control blocks of a two-level VSC based DVR: (a) PR controller in time domain and (b) Park transformation and PI controller in SRF.

The time domain DVR control strategy offers independent regulation of each phase voltage, making the control structure simple in response to unbalanced disturbances. However, the time variant system with a PI controller will create steady-state-error; whence the proportional resonance (PR) control method provides an alternative implementation that reduces the steady-state-error, shown in Fig. 2-22(a). To achieve better accuracy results, symmetrical components analysis can be employed to resolve critical voltage and current into positive and negative sequences, where the variables become DC components, thus are suitable to obtain zero steady-state-error using the PI method. In Fig. 2-22(b), the variables projected into positive and negative sequence SRFs are controlled independently to handle unbalanced compensation, and their output signals are summed to form the reference signal for VSC voltage synthesis. This method requires a complicated control structure and large amount of calculation for mathematical transformation.

The converter level DVR model, with specifications as in Table 2-8 to Table 2-10, is assessed. A single-phase 30Ω load is connected between phase *a* and phase *b* at *t*=2s; then removed at *t*=4s. During these transitions, the DVR is employed to maintain the load bus voltage.

Table 2-8. Specifications of VSC model in DVR.

Two-level VSC	
Apparent power rating S_{con}	20MVA
DC link voltage V_{dc}	41kV
DC link capacitor C_d	2200μF
Filtering inductor L_f	12mH
Filtering capacitor C_f	80μF
Converter switching frequency	2.5kHz

Table 2-9. Specifications of transformer installations.

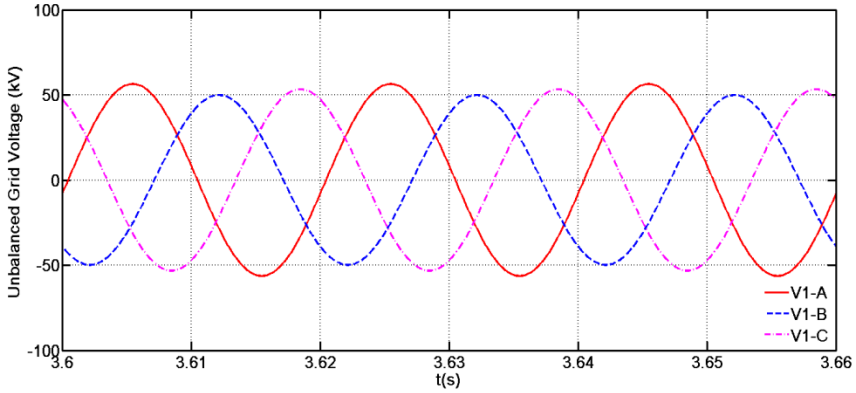
Series transformer	
Power capacity	20MVA
Voltage ratio	20kV/10kV
Per unit impedance	(0.0002+j0.05)

Table 2-10. AC distribution grid parameters.

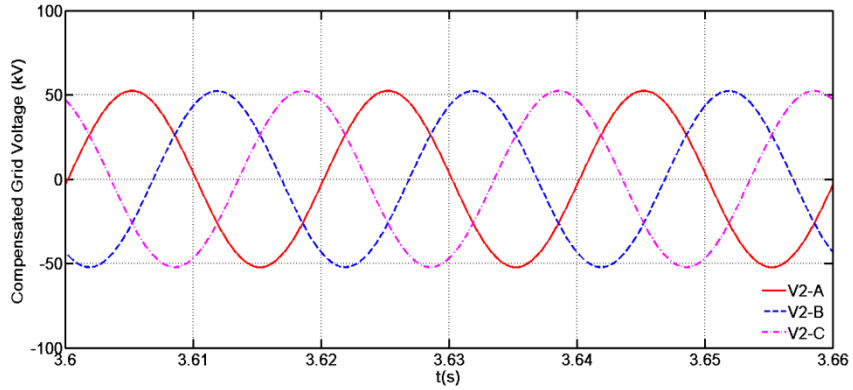
Grid parameters for series compensation	
Nominal line voltage	66kV(RMS)
Short circuit level	2GMVA
X/R ratio	20

The disturbed unbalanced voltage waveform is shown in Fig. 2-23(a); and the corrected critical bus with the DVR installed is as in Fig. 2-23(b). The series injected

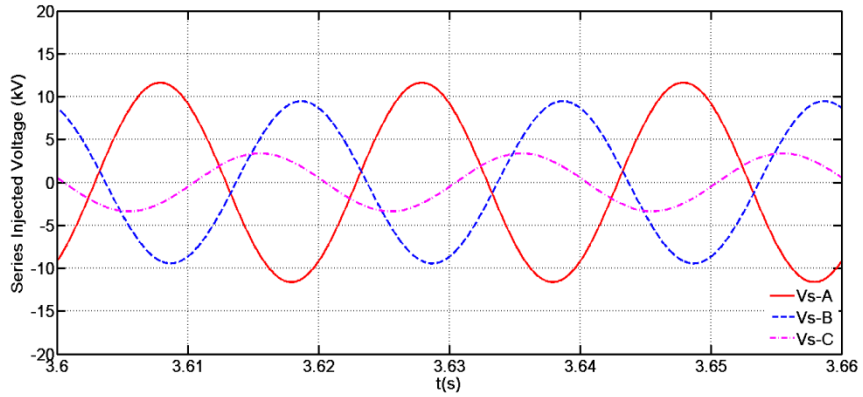
voltage and total load current waveforms are shown by Fig. 2-23(c) and (d), respectively. The angle between the series injected voltage and line current in Fig. 2-23(e) verifies that both active and reactive power can be exchanged between the DVR and the grid. Fig. 2-23(f) shows that the load bus voltage amplitude for each phase are controlled to maintain the reference during transitions, and correspondingly, the injected phase voltage amplitudes are displayed in Fig. 2-23(g). In the *d*-*q* frame, the positive and negative sequence components of the DVR injected voltage are seen in Fig. 2-23(h).



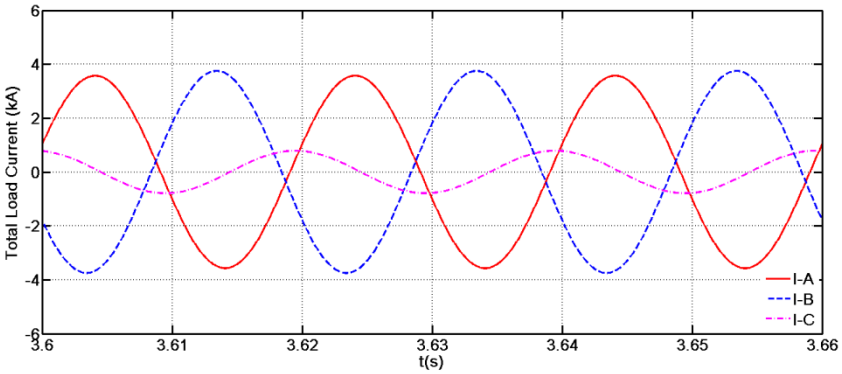
(a)



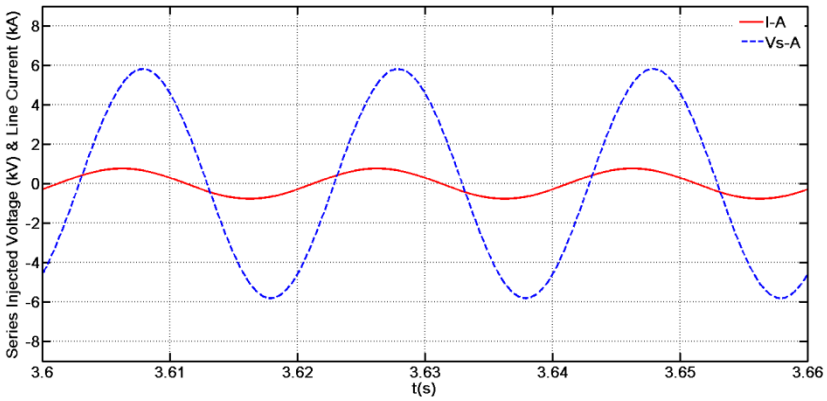
(b)



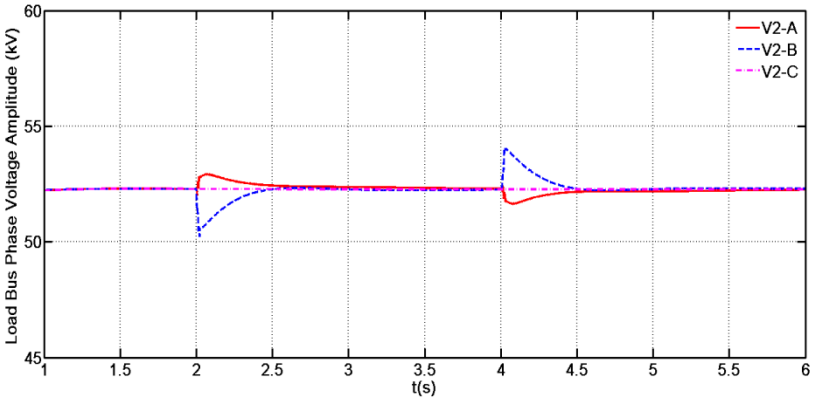
(c)


Total Load Current (kA)
t(s)
I-A
I-B
I-C

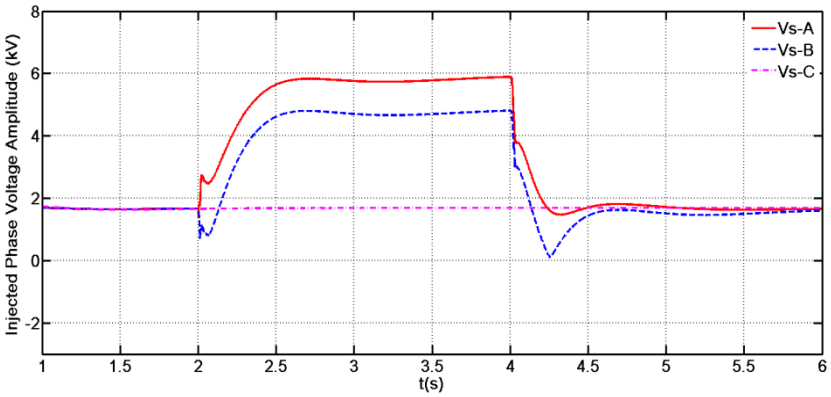
(d)


Series Injected Voltage (kV) & Line Current (kA)
t(s)
I-A
Vs-A

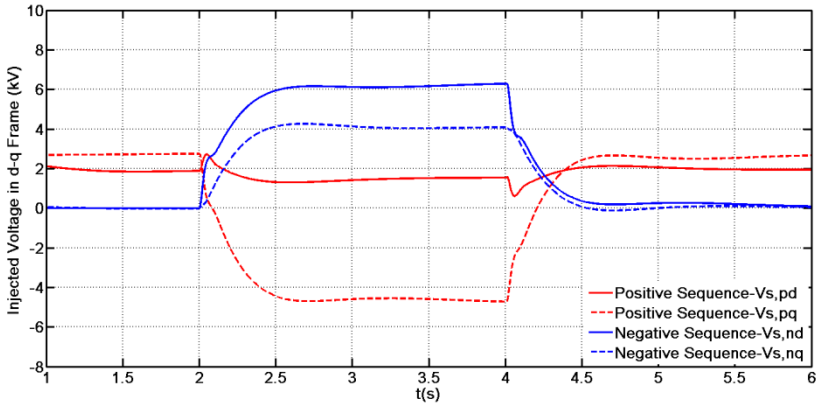
(e)


Load Bus Phase Voltage Amplitude (kV)
t(s)
V2-A
V2-B
V2-C

(f)


Injected Phase Voltage Amplitude (kV)
t(s)
Vs-A
Vs-B
Vs-C

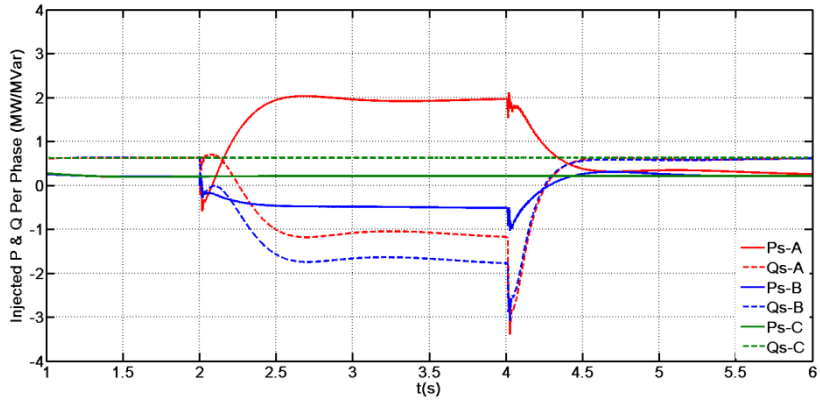
(g)



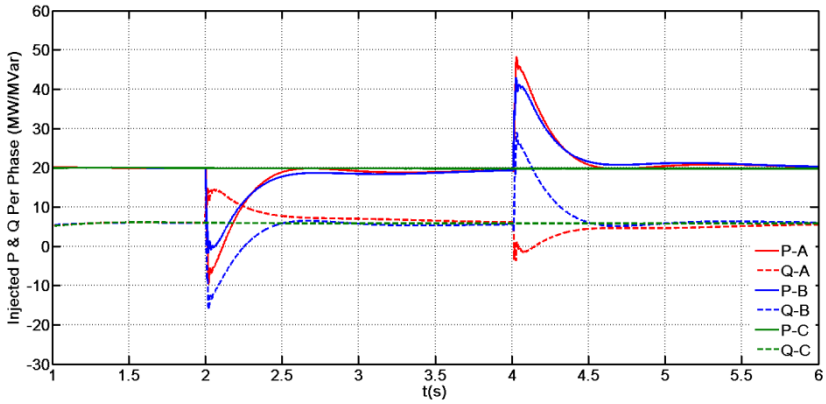
(h)

Fig. 2-23. DVR for unbalanced load compensation: (a) disturbed voltage by unbalanced load; (b) compensated voltage using DVR; (c) three-phase injected voltage by DVR; (d) total load current during unbalanced condition; (e) series injected voltage and grid line current in phase A; (f) critical bus voltage amplitude during disturbances; (g) DVR injected voltage amplitude variation; and (h) DVR injected voltage in *d-q* frame.

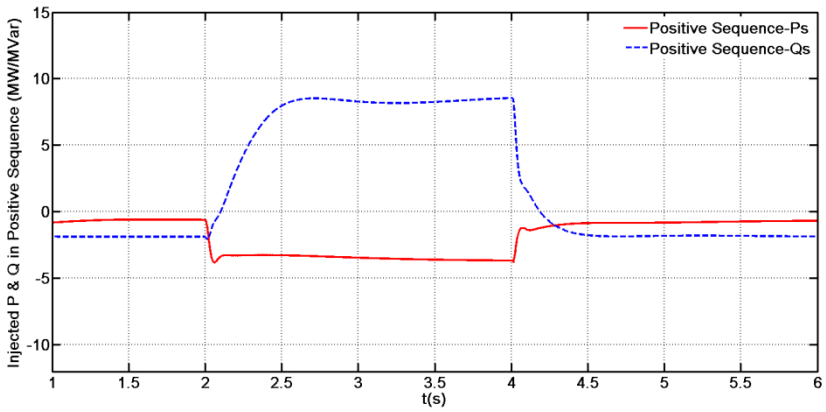
Power flow influences caused by DVR action are shown by Fig. 2-24. The active and reactive power at the load bus for each phase can be observed in Fig. 2-24(a). As expected, the DVR contributes a different power flow for each phase to restore the bus voltage as in Fig. 2-24(b); and its *d-q* frame interpretation in both the positive and negative sequences are shown in Fig. 2-24(c) and Fig. 2-24(d).



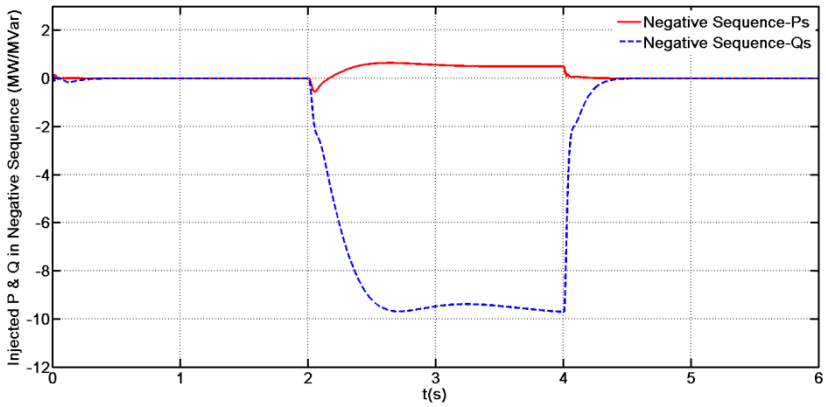
(a)



(b)



(c)



(d)

Fig. 2-24. DVR power flow influence: (a) DVR injected active and reactive power for each phase; (b) critical bus power flow for each phase; (c) DVR injected active and reactive power in positive sequence; and (d) DVR injected active and reactive power in negative sequence.

A DVR is also potentially able to compensate the harmonic distortion caused by nonlinear loads. However, this function will is not considered in this thesis because its implementation requires high switching frequency to fully respond to the reference which is practically not desirable at the distribution level of a utility.

2.4.3 United Power Flow Controller (UPFC)

A UPFC configuration is shown in Fig. 2-25, which can be viewed as a typical STATCOM and SSSC coupled via a common DC-link. Thus, the shunt connected VSC controls the voltage amplitude or reactive power at the shunt transformer PCC and maintains the DC-link voltage; while the series type VSC manages the power flow on the grid line [42-48].

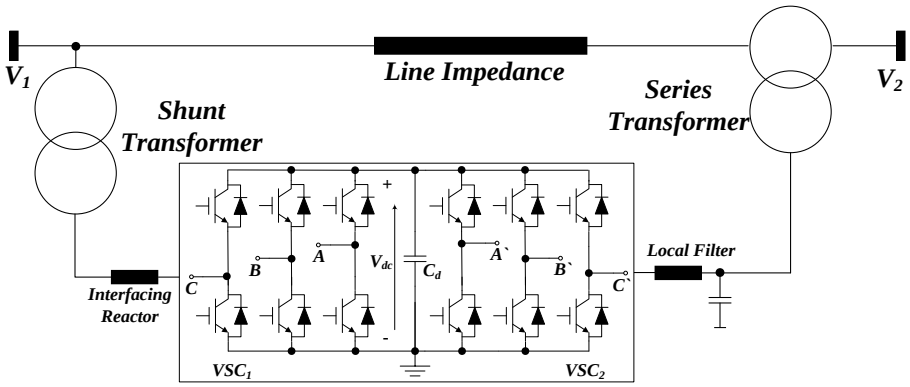


Fig. 2-25. UPFC diagram using two-level VSC.

Since the DC-link voltage can be regulated by the shunt VSC, the series VSC output voltage can be an arbitrary angle to the line current, which means the possibility of active power exchanged between the UPFC and the grid. In this sense, the shunt type converter of the UPFC operates in a typical STATCOM mode where the control strategy in Fig. 2-14 is inherited; and for the series VSC, the two control degrees of freedom can be assigned to realize various control targets such as active/reactive power, active power/apparent impedance, active power/voltage amplitude, etc.

The upper level supervisory control and data acquisition (SCADA) system resolves the voltage reference for the local controller of the series type VSC in a UPFC as in Fig. 2-26. For example, if the direct axes voltage is fixed at zero and the quadrature voltage reference comes from the active power flow manipulation, the series converter operates in a typical SSSC mode. Since the VSC DC-link voltage is maintained constant by the controller, if all internal losses are neglected, the total active power exchange between the DC-link and the two VSCs (grid) should be zero as in (2.16), by considering the energy conservation law.

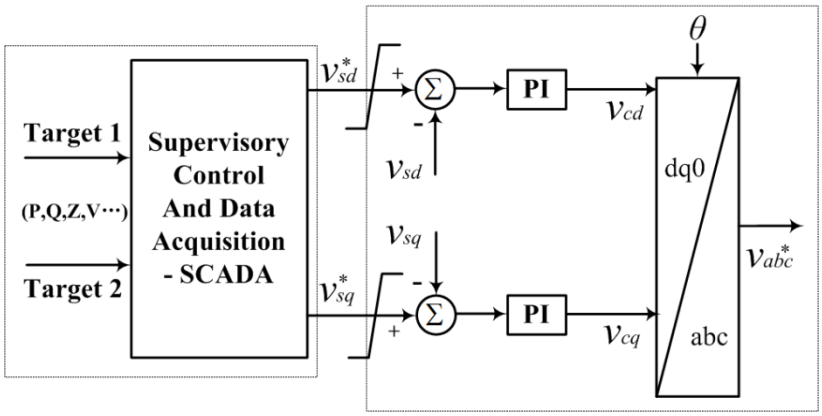
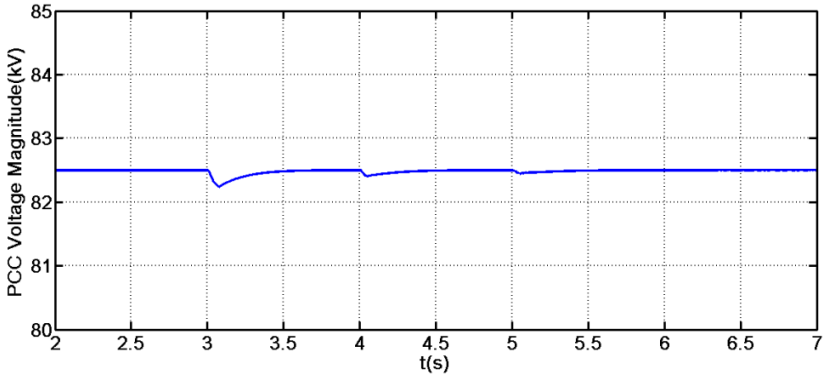


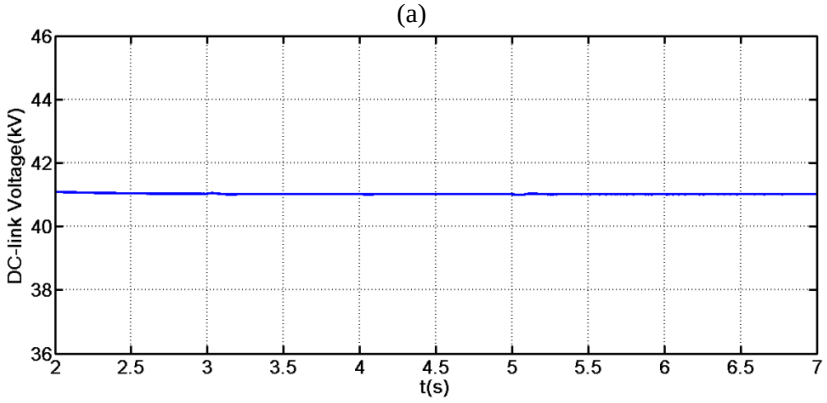
Fig. 2-26. Control block of series VSC in a UPFC.

$$P_{sh} + P_s = \mathrm{Re}(\mathbf{V_{sh}} \times \mathbf{I_{sh}}^*) + \mathrm{Re}(\mathbf{V_s} \times \mathbf{I_l}^*) = 0 \qquad (2.16)$$

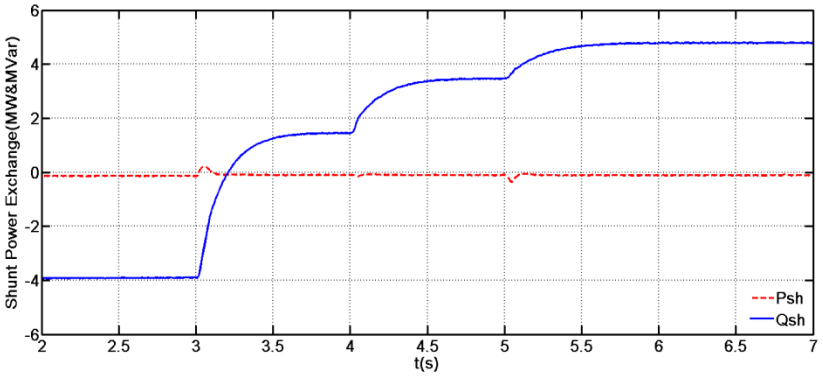
If the active power flow is the control target and the UPFC exchanges zero active power with the grid; simulation is based on following specifications: converter DC-link voltage: 41kV; grid line-to-line RMS voltage: 110kV; shunt transformer: 110kV/16.78kV with the leakage impedance of 0.0005pu+j0.08pu; series transformer: 20kV/10kV with the leakage impedance of 0.0002pu+j0.05pu. Fig. 2-27(a) and (b) confirm that the UPFC is able to stabilize the voltage magnitude at the shunt connection terminal and maintain the DC link voltage. Fig. 2-27(c) shows the reactive power generated by the UPFC shunt VSC for terminal voltage regulation. Fig. 2-27(d) is the power exchange between series converter and the grid. Then, the power flow between two buses is manipulated to track reference, from Fig. 2-27(e).



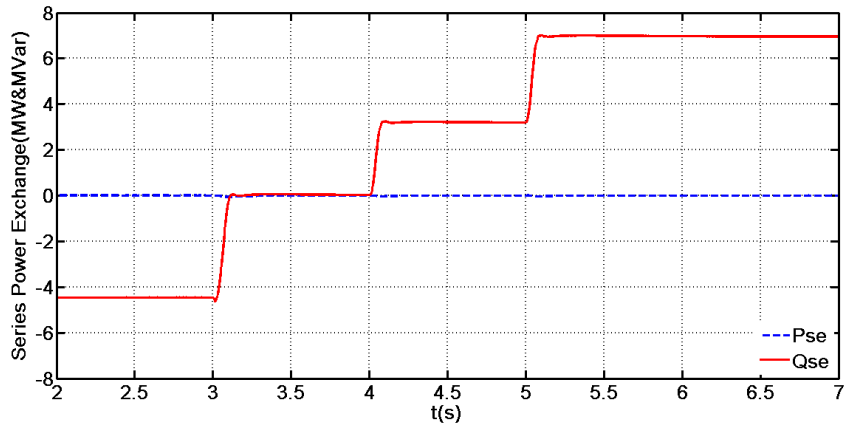
(a)



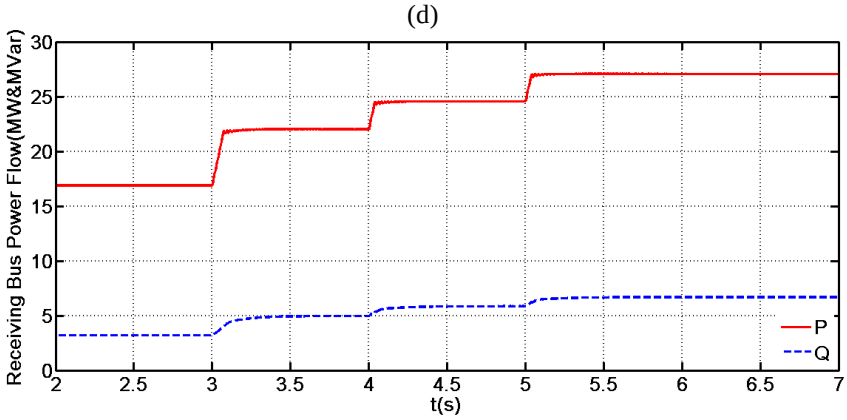
(b)



(c)



(d)



(e)

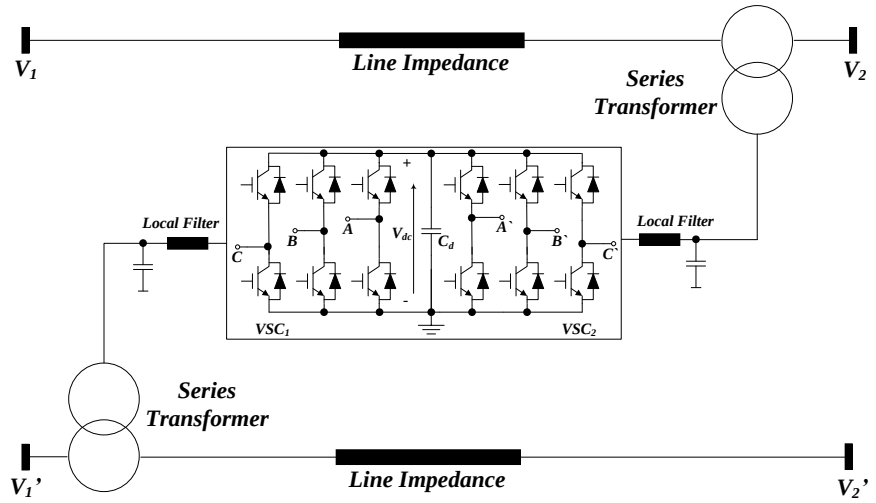
Fig. 2-27. UPFC power flow influence: (a) voltage amplitude at the PCC for shunt type converter; (b) DC-link voltage of UPFC; (c) power exchange between shunt converter and grid; (d) power exchange between series converter and grid; (e) power flow of the grid line.

2.4.4 Interline Power Flow Controller (IPFC) & Generalized Unified Power Flow Controller (GUPFC)

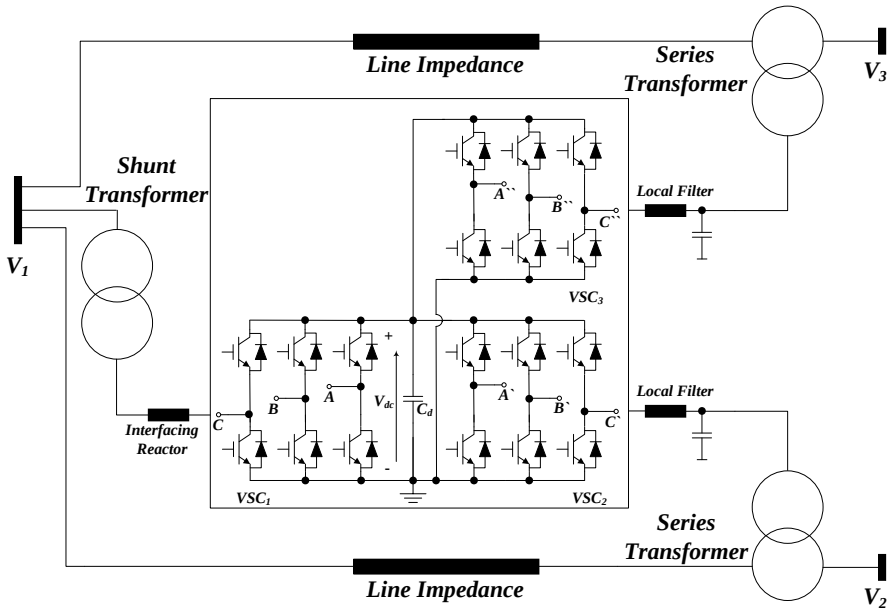
Based on a DC-link common coupling configuration, complicated multi-bus power flow controllers based on the VSC can be derived [49-52].

The IPFC integrates multiple series converters via one DC-link, to regulate the power flows on a group of power line branches from the same substation. It is able to enhance the utilization of the power line transfer capacity in existing grid facilities. The basic case of an IPFC installation with two VSC units is shown in Fig. 2-28(a). For an IPFC system with m_k buses (VSCs), there are $2m_k$-1 controllable power system quantities due to the law of active power conservation. This constraint can be interpreted by (2.17) if the DC-link voltage is maintained constant by a VSC using the typical SSSC control strategy in Fig. 2-18. Then, the other VSCs will each have two control degrees of freedom for grid variables with the control diagram inherited from Fig. 2-26.

$$\sum P_s = \sum \mathrm{Re}(\mathbf{V_s} \times \mathbf{I_l}^*) = 0 \qquad (2.17)$$



(a)



(b)

Fig. 2-28. Configurations of typical multi-bus power flow controllers based on two-level VSC: (a) IPFC and (b) GUPFC.

As a UPFC expansion, the GUPFC incorporates more than one series type VSC onto the common DC-link. It is appropriate for explicit control of the grid nodal voltage and managing the power flow over multiple power lines. A basic case that has three VSCs (one shunt and two series) is displayed in Fig. 2-28(b). The operation constraint of a GUPFC based on energy conservation is shown in (2.18) and the control strategies for each VSC unit can be inherited from the UPFC, see Fig. 2-14 and Fig. 2-26.

$$P_{sh} + \sum P_s = \mathrm{Re}(\mathbf{V_{sh}} \times \mathbf{I_{sh}}^*) + \sum \mathrm{Re}(\mathbf{V_s} \times \mathbf{I_l}^*) = 0 \qquad (2.18)$$

2.4.5 Back-To-Back (B2B) VSC Devices

B2B VSC devices offer four-quadrant operation ability to realize full range control of active and reactive power flow in both terminals. In fractional power flow control devices, they can be viewed as a B2B STATCOM to supply an auxiliary power transmission path for the existing grid. In a full power rated power flow control system, the VSC-HVDC solution is formed [53-59].

The VSC-HVDC system configuration using the two-level converter topology is shown in Fig. 2-29. Similar to the STATCOM derivation process from (2.4) to (2.9), the local control strategy for the VSC based converter station in the HVDC transmission system can be described by Fig. 2-30. The direct axes current reference is set by the active power or DC-link voltage controller in the outer-layer, while the grid voltage amplitude or reactive power regulator is responsible for determining the command current in quadrature axis. A HVDC system is able to realize a wide range of power system control targets such as power flow control, voltage control, frequency support, asynchronous integration, etc.

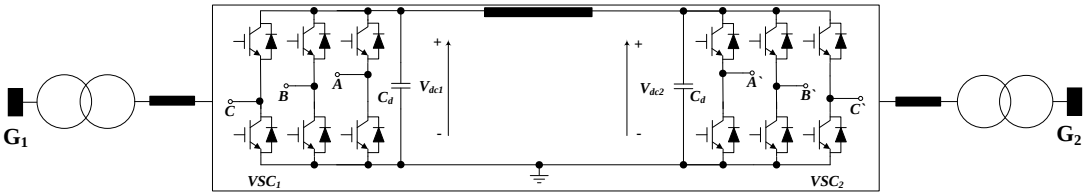


Fig. 2-29. Configurations of HVDC system using two-level VSC.

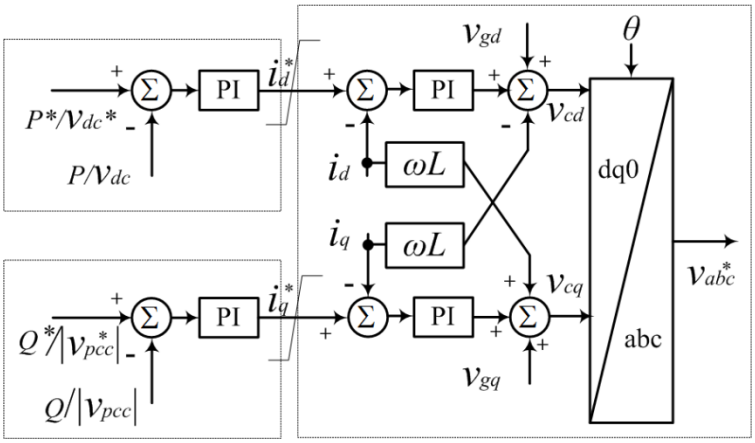


Fig. 2-30. Control block for two-level VSC based HVDC system.

2.5 Summary

The first part of this chapter reviewed the conventional three-phase two-level converter and the full-bridge converter, including their modulation schemes. Established modulation techniques such as SPWM, TSPWM, SVM and SHE were analysed and compared quantitatively using simulations. The second part of this chapter used the two-level converter to illustrate the operational principles of key FACTS devices such as STATCOM, SSSC, DVR, UPFC, IPFC, GUPFC, and B2B VSC. A number of illustrative simulations for typical cases confirmed the effectiveness of FACTS devices. Key observations are:

- The two-level converter has a maximum DC utilization of 0.5 within the linear modulation range; while a full-bridge converter using SPWM can generate twice the AC voltage magnitude relative to the two-level converter;
- Compared to basic SPWM, the TSPWM, SVM and SHE improve the DC voltage utilization for three-phase VSC systems by the introduction of 3^{rd} order harmonics into the converter phase voltage;
- In two-level and full bridge converters, the power switches sustain full DC-link voltage; thus, high switching losses and high *dv*/*dt* promote the use of multilevel converters in FACTS applications, which can also reduce the output voltage THD and filter size. This will be discussed in later chapters;
- To reduce VSC footprint and cost in medium and high voltage conditions, new topologies with improved DC voltage utilization (power density) and direct AC-AC converter without a DC-link will also be researched in this thesis;
- Operation principles of typical FACTS devices were demonstrated using the two-level converter; and these system level control strategies are applicable to other VSC topologies.

Reference

[1] X. Zhang, "Restructured Electric Power Systems: Analysis of Electricity Markets with Equilibrium Models," ed: Wiley-IEEE Press, 2010, pp. 12-13.

[2] C. Hong, "Practices of reactive power management and compensation," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, 2008, pp. 1-4.

[3] G. Blanchon, N. Girard, Y. Logeay, and F. Meslier, "New Developments in Planning of Reactive Power Compensation Devices," *Power Systems, IEEE Transactions on*, vol. 2, pp. 764-771, 1987.

[4] M. Yehia, R. Ramadan, Z. El-Tawail, and K. Tarhini, "An integrated technico-economical methodology for solving reactive power compensation problem," *Power Systems, IEEE Transactions on,* vol. 13, pp. 54-59, 1998.

[5] L. Furong, J. D. Pilgrim, C. Dabeedin, A. Chebbo, and R. K. Aggarwal, "Genetic algorithms for optimal reactive power compensation on the national grid system," *Power Systems, IEEE Transactions on,* vol. 20, pp. 493-500, 2005.

[6] G. Joksimovic, "Transformer Reactive Power Compensation 2013; Fixed Capacitor Bank Calculation," *Power Delivery, IEEE Transactions on,* vol. PP, pp. 1-1, 2014.

[7] S. Ganguly, "Multi-Objective Planning for Reactive Power Compensation of Radial Distribution Networks With Unified Power Quality Conditioner Allocation Using Particle Swarm Optimization," *Power Systems, IEEE Transactions on,* vol. 29, pp. 1801-1810, 2014.

[8] F. Kreikebaum, D. Das, J. Hernandez, and D. Divan, "Ubiquitous power flow control in meshed grids," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE,* 2009, pp. 3907-3914.

[9] P. F. Keebler, "Meshing power quality and electromagnetic compatibility for tomorrow's smart grid," *Electromagnetic Compatibility Magazine, IEEE,* vol. 1, pp. 100-103, 2012.

[10] A. K. Marten and D. Westermann, "Schedule for converters of a meshed HVDC grid and a contingency schedule for adaption to unscheduled power flow changes," in *Power and Energy Society General Meeting (PES), 2013 IEEE,* 2013, pp. 1-5.

[11] T. M. Haileselassie and K. Uhlen, "Power System Security in a Meshed North Sea HVDC Grid," *Proceedings of the IEEE,* vol. 101, pp. 978-990, 2013.

[12] Z. Jiahui, Q. Ming, L. Xiaokang, C. Xiaoyu, and Y. Weijia, "Modeling and analysis of the power transmission with an 110kV/3kA HTS cable in a meshed grid," in *PES General Meeting | Conference & Exposition, 2014 IEEE,* 2014, pp. 1-5.

[13] X.-P. Zhang, C. Rehtanz, and B. Pal, *Flexible AC Transmission Systems: Modelling and Control* Springer Science & Business Media, 2012.

[14] N. G. Hingorani, L., *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*: Wiley-IEEE Press, 2000.

[15] H. Akagi, S. Inoue, and T. Yoshii, "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration," *Industry Applications, IEEE Transactions on,* vol. 43, pp. 1041-1049, 2007.

[16] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV Transformerless STATCOM Based on a Five-Level Diode-Clamped PWM Converter: System Design and Experimentation of a 200-V 10-kVA Laboratory Model," *Industry Applications, IEEE Transactions on,* vol. 44, pp. 672-680, 2008.

[17] L. Chia-Tse, W. Bo-siang, C. Sheng-wan, C. Shih-feng, H. Jun-lin, C. Po-Tai, *et al.*, "Average Power Balancing Control of a STATCOM Based on the Cascaded H-Bridge PWM Converter With Star Configuration," *Industry Applications, IEEE Transactions on,* vol. 50, pp. 3893-3901, 2014.

[18] D. Rai, S. O. Faried, G. Ramakrishna, and A. Edris, "An SSSC-Based Hybrid Series Compensation Scheme Capable of Damping Subsynchronous

Resonance," *Power Delivery, IEEE Transactions on,* vol. 27, pp. 531-540, 2012.

[19] A. Griffo and D. Lauria, "Two-Leg Three-Phase Inverter Control for STATCOM and SSSC Applications," *Power Delivery, IEEE Transactions on,* vol. 23, pp. 361-370, 2008.

[20] F. M. Albatsh, S. Ahmad, S. Mekhilef, H. Mokhlis, and M. A. Hassan, "D - Q model of fuzzy based UPFC to control power flow in transmission network," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on,* 2014, pp. 1-6.

[21] A. L. P. de Oliveira, C. E. Tiburcio, M. N. Lemes, and D. Retzmann, "Prospects of Voltage-Sourced Converters (VSC) applications in power transmission systems," in *ANDESCON, 2010 IEEE,* 2010, pp. 1-4.

[22] R. L. Sellick, x030A, and M. Kerberg, "Comparison of HVDC Light (VSC) and HVDC Classic (LCC) site aspects, for a 500MW 400kV HVDC transmission scheme," in *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on,* 2012, pp. 1-6.

[23] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice* vol. 18: John Wiley & Sons, 2003.

[24] J. Do-Hyun and Y. Duck-Yong, "Space-vector PWM technique for two-phase inverter-fed two-phase induction motors," *Industry Applications, IEEE Transactions on,* vol. 39, pp. 542-549, 2003.

[25] J. Do-Hyun, "PWM methods for two-phase inverters," *Industry Applications Magazine, IEEE,* vol. 13, pp. 50-61, 2007.

[26] E. R. C. da Silva, E. C. dos Santos, and C. B. Jacobina, "Pulsewidth Modulation Strategies," *Industrial Electronics Magazine, IEEE,* vol. 5, pp. 37-45, 2011.

[27] D. G. Holmes, "A general analytical method for determining the theoretical harmonic components of carrier based PWM strategies," in *Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE,* 1998, pp. 1207-1214 vol.2.

[28] L. G. Franquelo, J. Napoles, R. C. P. Guisado, J. I. Leon, and M. A. Aguirre, "A Flexible Selective Harmonic Mitigation Technique to Meet Grid Codes in Three-Level PWM Converters," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 3022-3029, 2007.

[29] S. R. Bowes and D. Holliday, "Comparison of pulse-width-modulation control strategies for three-phase inverter systems," *Electric Power Applications, IEE Proceedings -,* vol. 153, pp. 575-584, 2006.

[30] A. Tatu, P. N. Kapil, V. Patel, and J. Patel, "Review of modulation schemes for loss analysis in inverters," in *Engineering (NUiCONE), 2012 Nirma University International Conference on,* 2012, pp. 1-5.

[31] N. Flourentzou and V. G. Agelidis, "Harmonic performance of multiple sets of solutions of SHE-PWM for a 2-level VSC topology with fluctuating DC-link voltage," in *Power Engineering Conference, 2007. AUPEC 2007. Australasian Universities,* 2007, pp. 1-8.

[32] P. G. Handley and J. T. Boys, "Space vector modulation: an engineering review," in *Power Electronics and Variable-Speed Drives, 1991., Fourth International Conference on,* 1990, pp. 87-91.

[33] H. Dehbonei, L. Borle, and C. V. Nayar, "A review and a proposal for optimal harmonic mitigation in single-phase pulse width modulation," in

Power Electronics and Drive Systems, 2001. Proceedings., 2001 4th IEEE International Conference on, 2001, pp. 408-414 vol.1.

[34] O. Anaya-Lara and E. Acha, "Modeling and analysis of custom power systems by PSCAD/EMTDC," *Power Delivery, IEEE Transactions on*, vol. 17, pp. 266-272, 2002.

[35] A. B. Arsoy, Y. Liu, P. F. Ribeiro, and F. Wang, "StatCom-SMES," *Industry Applications Magazine, IEEE*, vol. 9, pp. 21-28, 2003.

[36] F. A. Albasri, T. S. Sidhu, and R. K. Varma, "Performance Comparison of Distance Protection Schemes for Shunt-FACTS Compensated Transmission Lines," *Power Delivery, IEEE Transactions on*, vol. 22, pp. 2116-2125, 2007.

[37] S. Anand, B. G. Fernandes, and K. Chatterjee, "DC Voltage Controller for Asymmetric-Twin-Converter-Topology-Based High-Power STATCOM," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 11-19, 2013.

[38] F. A. R. A. Jowder and O. Boon-Teck, "Series compensation of radial power system by a combination of SSSC and dielectric capacitors," *Power Delivery, IEEE Transactions on*, vol. 20, pp. 458-465, 2005.

[39] M. S. El-Moursi and A. M. Sharaf, "Novel controllers for the 48-pulse VSC STATCOM and SSSC for voltage regulation and reactive power compensation," *Power Systems, IEEE Transactions on*, vol. 20, pp. 1985-1997, 2005.

[40] Z. Changjiang, V. K. Ramachandaramurthy, A. Arulampalam, C. Fitzer, S. Kromlidis, M. Barnes, *et al.*, "Dynamic voltage restorer based on voltage space vector PWM control," in *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, 2001, pp. 1301-1307 vol.2.

[41] I. R. Filho, J. L. S. Neto, L. G. Rolim, and M. Aredes, "Design and Implementation of a Low Cost Series Compensator for Voltage Sags," in *Industrial Electronics, 2006 IEEE International Symposium on*, 2006, pp. 1353-1357.

[42] H. Ambriz-Perez, E. Acha, C. R. Fuerte-Esquivel, and A. De la Torre, "Incorporation of a UPFC model in an optimal power flow using Newton's method," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 145, pp. 336-344, 1998.

[43] F. Aminifar, M. F. Firuzabad, and R. Billinton, "Extended reliability model of a unified power flow controller," *Generation, Transmission & Distribution, IET*, vol. 1, pp. 896-903, 2007.

[44] S. Arabi, P. Kundur, and R. Adapa, "Innovative techniques in modeling UPFC for power system analysis," *Power Systems, IEEE Transactions on*, vol. 15, pp. 336-341, 2000.

[45] S. Bruno, E. De Tuglie, M. La Scala, and P. Scarpellini, "Dynamic security corrective control by UPFCs," in *Power Industry Computer Applications, 2001. PICA 2001. Innovative Computing for Power - Electric Energy Meets the Market. 22nd IEEE Power Engineering Society International Conference on*, 2001, pp. 241-245.

[46] J. Z. Bebic, P. W. Lehn, and M. R. Iravani, "P-δ characteristics for the unified power flow controller-analysis inclusive of equipment ratings and line limits," *Power Delivery, IEEE Transactions on*, vol. 18, pp. 1066-1072, 2003.

[47] X. Bei and A. Abur, "State estimation of systems with UPFCs using the interior point method," *Power Systems, IEEE Transactions on*, vol. 19, pp. 1635-1641, 2004.
[48] S. Bhowmick, B. Das, and N. Kumar, "An Indirect UPFC Model to Enhance Reusability of Newton Power-Flow Codes," *Power Delivery, IEEE Transactions on*, vol. 23, pp. 2079-2088, 2008.
[49] S. Arabi, H. Hamadanizadeh, and B. B. Fardanesh, "Convertible static compensator performance studies on the NY state transmission system," *Power Systems, IEEE Transactions on*, vol. 17, pp. 701-706, 2002.
[50] B. Fardanesh, "Optimal utilization, sizing, and steady-state performance comparison of multiconverter VSC-based FACTS controllers," *Power Delivery, IEEE Transactions on*, vol. 19, pp. 1321-1327, Jul 2004.
[51] J. Sun, L. Hopkins, B. Shperling, B. Fardanesh, M. Graham, M. Parisi, *et al.*, "Operating characteristics of the convertible static compensator on the 345 kV network," in *Power Systems Conference and Exposition, 2004. IEEE PES*, 2004, pp. 732-738 vol.2.
[52] B. Shperling, J. Sun, and S. Bhattacharya, "Power flow control on 345 kV lines with the 200 MVA convertible static compensator," in *Power Tech, 2005 IEEE Russia*, 2005, pp. 1-7.
[53] G. P. Adam, K. H. Ahmed, S. J. Finney, and B. W. Williams, "AC fault ride-through capability of a VSC-HVDC transmission systems," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, 2010, pp. 3739-3745.
[54] X. Jianzhong, Z. Chengyong, and Z. Baoshun, "Control design and operational characteristics comparation for VSC-HVDC supplying active/passive networks," in *Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on*, 2011, pp. 1381-1386.
[55] H. Liu and Z. Chen, "Contribution of VSC-HVDC to Frequency Regulation of Power Systems With Offshore Wind Generation," *Energy Conversion, IEEE Transactions on*, vol. PP, pp. 1-9, 2015.
[56] J. Yang, J. E. Fletcher, J. O'Reilly, G. P. Adam, and S. Fan, "Protection scheme design for meshed VSC-HVDC transmission systems of large-scale wind farms," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.
[57] W. Song, L. Gengyin, Z. Ming, and Z. Zhe, "Research on VSC-HVDC system to mitigate power output fluctuation caused by wind farms," in *Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on*, 2011, pp. 314-319.
[58] T. M. Haileselassie, R. E. Torres-Olguin, T. K. Vrana, K. Uhlen, and T. Undeland, "Main grid frequency support strategy for VSC-HVDC connected wind farms with variable speed wind turbines," in *PowerTech, 2011 IEEE Trondheim*, 2011, pp. 1-6.
[59] T. D. Vrionis, X. I. Koutiva, N. A. Vovos, and G. B. Giannakopoulos, "Control of an HVdc Link Connecting a Wind Farm to the Grid for Fault Ride-Through Enhancement," *Power Systems, IEEE Transactions on*, vol. 22, pp. 2039-2047, 2007.

CHAPTER 3

AC Side Voltage-Doubled High Power-Density VSC with Intrinsic Buck-Boost Cells and Common-Mode Voltage Suppression

In this chapter, a three-phase AC side voltage-doubled VSC topology with intrinsic buck-boost cells is presented and analysed. The AC side voltage is doubled with the phase peak value equal to the DC-link voltage. The proposed converter uses its buck-boost cell as virtual voltage source to synthesize the negative part of the output voltage by modulating its output AC phase voltage around the negative bus (which is the real zero when grounded). This permits the average CM voltage to be suppressed to zero, and loads connected to the converter AC side do not withstand any DC voltage stress (reducing the insulation requirement). Modelling and control design for both the rectifier and inverter modes of this converter in the synchronous reference frame (SRF) are investigated to ensure four-quadrant back-to-back system operation. Experimental results are shown to verify the feasibility and effectiveness of the proposed configuration and the designed control strategies.

3.1 Background

Power electronics based energy conversion systems have penetrated low, medium and high voltage applications such as power transmission and reactive power compensation, grid interfacing of renewable energy, machine drives, etc. Since traditional AC grids still dominate power systems, AC power conversion involving amplitude regulation, phase and frequency control, active power and reactive power management for utility/micro-grid applications draw the attention of both academia and industry.

The back-to-back (B2B) VSC based configuration is widely used in AC conversion due to its control simplicity and better dynamic performance over current source converter based solutions [1, 2]. This is because it offers four-quadrant operational ability, decoupling of the two connected AC sides, and independent control of active/reactive power. The VSC together with its B2B configuration have taken over the traditional power traction area and spread into utility applications, such as PV (photovoltaic) grid connection, wind energy interfacing, flexible AC and high voltage DC transmission systems (FACTS and HVDC), etc. [3-9].

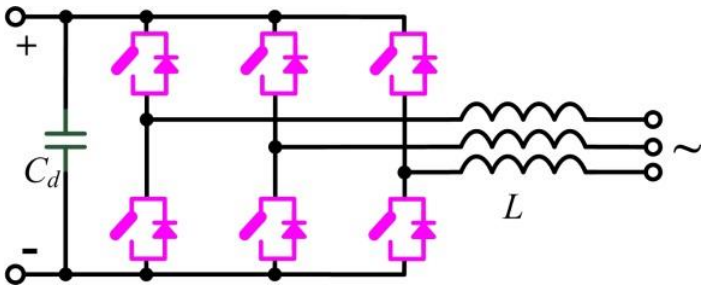


Fig. 3-1 Three-phase two-level voltage source converter.

The three-phase two-level converter depicted in Fig. 3-1 is widely used for AC-DC and DC-AC power conversion systems, in research and industry. However, in this topology, the peak value of AC side voltage per phase cannot exceed half the DC link voltage with traditional sinusoidal pulse width modulation (SPWM). Although triplen sinusoidal pulse width modulation (TSPWM), space vector modulation (SVM), and selective harmonic elimination (SHE) methods have been developed to extend the fundamental voltage output range on the AC side, the increase is limited (15.5% for TSPWM/SVM, and slightly higher for optimized SHE) [10]. Generally, three-phase balanced conditions should be guaranteed to insure this voltage utilization extension; otherwise, low order harmonics are observed in the line-to-line

voltages and line currents. This is because zero sequence components emerge in the phase voltage when it goes beyond the envelope of the positive and negative DC-link, and they can only be neutralized under three-phase balanced situations. Therefore, operation in medium and high voltage applications requires a high DC-link voltage (minimum twice of the peak fundamental voltage) or a bulky step-up transformer for voltage matching, which in turn increases system cost, size and weight.

The three-phase two-level VSC in Fig. 3-1 may impose DC voltage stress on the AC side loads depending on the adopted grounding arrangement [11, 12]. When the negative terminal is grounded, the output phase voltage relative to real ground varies around half the DC-link voltage, and this requires AC loads to be able to withstand DC voltage stress [13]. Furthermore, the voltage fluctuation around half the DC-link on the load neutral point may exacerbate bearing voltage problems in machine drives such as in wind turbine interfacing. The split DC-link capacitor with parallel balancing resistors can be employed to address the problem of DC voltage stress and reduce the impact of the CM voltage. However, this solution is less attractive as it introduces additional loss and cost.

A specific case under the spotlight recently is the transformerless PV integration area where effort is made to suppress the CM current through the parasitic capacitor between the PV arrays and ground. By introducing extra auxiliary switches, the H5, H6 and HERIC schemes are candidates to suppress the CM leakage current [14]. However, the CM voltage component still exists and remains constant in these situations. The virtual DC bus concept [15] and HA4S converter [16] have been promoted to eliminate the CM voltage by direct connection between ground terminals. Unfortunately, all these solutions are in single-phase applications and originate from the full-bridge topology. Thus, it is difficult to transfer these derived converters directly into three-phase applications.

In this chapter, a three-phase AC side voltage-doubled (ACVD) converter with intrinsic buck-boost cells (IBBCs) is proposed, which can generate an AC phase voltage with a maximum peak value equal to full DC-link voltage, doubled the output range of the traditional three-phase two-level VSC. Alternatively, the DC-link can be halved when a given output voltage is demanded. Therefore, either the line transformer or the DC capacitor bank can be reduced to form a compact, cost-efficient system. In addition, the power density of the proposed converter can be

increased. Since the proposed topology inherits a real ground fixed at the negative bus, its output phase voltage is modulated around this ground. As a result, DC voltage stress exerted on AC loads is minimized to zero, which will suppress the CM voltage magnitude to an average of zero, as seen by the load neutral point. Hence, reduced bearing voltage/current can be expected. Further a composite hardware configuration or an optimized modulation strategy can eliminate the CM voltage high frequency components, which is not considered in this chapter [17-19]. The ACVD converter is capable of being employed in PV integration, wind energy interfacing, and distributed FACTS areas. The remainder of this chapter is organized as follows: the operational principle of the proposed converter is described in 3.2. 3.3 analyses the voltage and current stresses on the power switches and presents some design issues for the passive components. In 3.4, the modelling process of three-phase ACVD-VSC for inverter and rectifier modes in a synchronous reference frame (SRF) is established. Then, 3.5 presents the control strategies design; with experimental verification presented in 3.6 to validate the proposed converter. Finally conclusions drawn and major findings are summarised in 3.7.

3.2 Operational Principle of the ACVD Converter

The proposed three-phase ACVD-VSC is shown in Fig. 3-2(a), where an IBBC is inserted into each phase of a two-level converter to achieve an extended AC output voltage range. The single-phase circuit under inverter mode depicted in Fig. 3-2(b) clarifies the topology structure. The IBBC consists of L_1 and C_1, while L_2 and C_2 make up the output stage filter. The power switches S_1 and S_2 conduct complementarily. V_{dc} is the input voltage, and i_1, v_1, i_2 and v_2 represent the four state variables of the passive components L_1, C_1, L_2 and C_2 respectively. v_1 is reversed relative to the input voltage to ensure magnetic reset of the flux linked in L_1. Similarly, i_1 and i_2 are in opposite directions to maintain voltage balance on C_1.

Operation of the proposed converter can be described in two modes as follows:

Mode 1: S_1 is turned on. Output voltage v_2 fed from V_{dc} is generated relative to ground. Also, this mode creates a zero voltage loop for inductor L_1 and capacitor C_1 for charging the buck-boost capacitor with a reversed polarity as V_{dc}.

Mode 2: When S_2 is on, the IBBC capacitor is employed as a virtual voltage source to generate the negative voltage at the output. The inner inductor L_1 is charged to store energy, ready for energy transfer in the subsequent switching cycle.

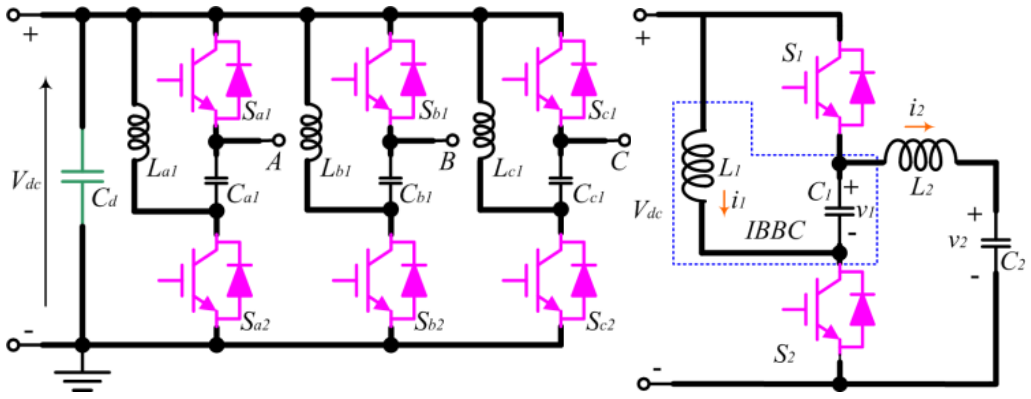


Fig. 3-2. Proposed ACVD converter: (a) three-phase configuration (without output filter) and (b) single-phase unit operated in the inverter mode.

Fig. 3-3 shows the steady state waveforms of the proposed converter at a fixed operating point, where v_2, i_2 are positive and i_1 is negative. The output voltage v_2 is always within the envelope created by the input voltage and the IBBC voltage, which guarantees inductor energy balance. Similarly, the inductor currents i_1 and i_2 charge and discharge the capacitors in each switching cycle to give the composed voltage output.

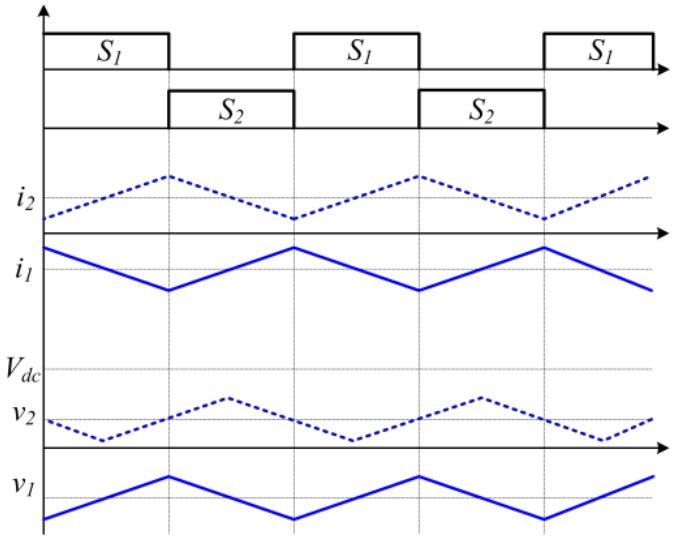


Fig. 3-3. Steady state waveforms of the proposed converter at a stationary operating point when v_2, i_2 are positive and i_1 is negative

Four-quadrant operation of the ACVD-VSC is shown in Fig. 3-4. In Fig. 3-4(a) and Fig. 3-4(b), i_2 flows out of the converter to the load; accordingly i_1 should either discharge C_1 or feed its stored energy back to the DC-link. The alternative situation is where i_2 flows into the converter from the load and i_1 draws energy from the DC side, delivering it to C_1 as in Fig. 3-4(c) and Fig. 3-4(d). Thus, it is concluded that the proposed converter qualifies for four-quadrant operational VSC applications.

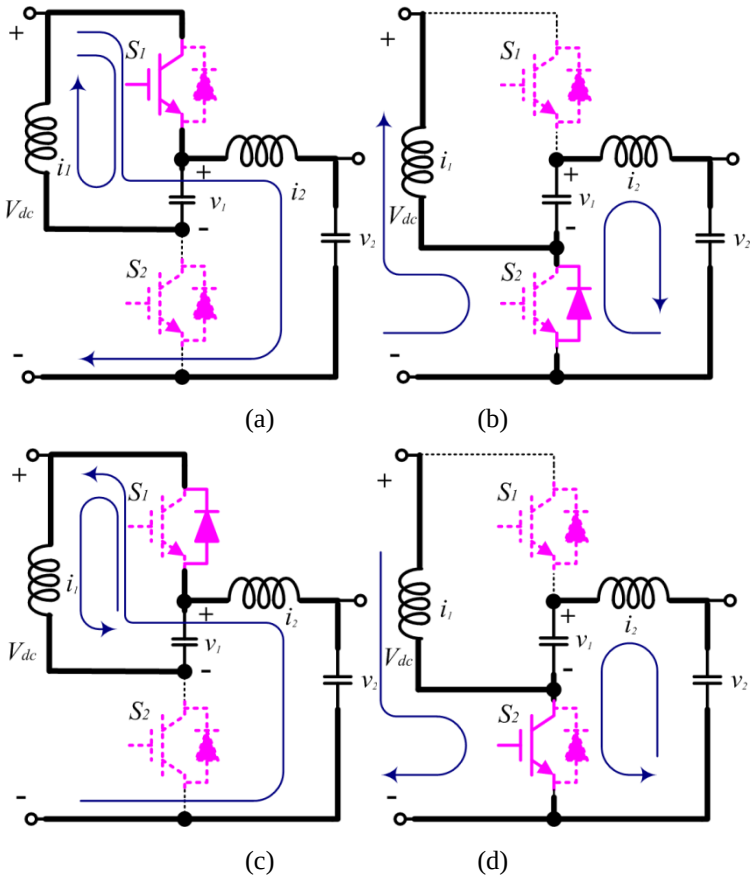


Fig. 3-4. Switching modes of the proposed converter when implementing four-quadrant operation: (a) S_1 turns on with outflow load current; (b) S_2 turns on with outflow load current; (c) S_1 turns on with inflow load current; and (d) S_2 turns on with inflow load current.

Based on this analysis, the differential equations that describe the dynamics of the proposed converter are interpreted in (3.1),

$$\begin{cases} L_1 \dfrac{di_1}{dt} = u(v_1 - V_{dc}) + V_{dc} \\ C_1 \dfrac{dv_1}{dt} = u(i_2 - i_1) - i_2 \\ L_2 \dfrac{di_2}{dt} = u(V_{dc} - v_1) + (v_1 - v_2) \\ C_2 \dfrac{dv_2}{dt} = i_2 - i_o \end{cases} \tag{3.1}$$

where u is the switching function defined as (3.2),

$$u = \begin{cases} 1, & S_1 \, turns \, on \\ 0, & S_2 \, turns \, on \end{cases} \tag{3.2}$$

When the switching frequency f_{sw} is sufficiently high compared to fundamental frequency of the AC voltage being synthesized, the assumption that the state variables can be viewed as constant is valid. Therefore, the derivative terms in (3.1)

can be set to zero, and the average value of the switching function u over one switching period is equal to the duty cycle D. Then equation (3.1) is reduced to:

$$\begin{cases} D(V_1 - V_{dc}) + V_{dc} = 0 \\ D(I_2 - I_1) - I_2 = 0 \\ D(V_{dc} - V_1) + (V_1 - V_2) = 0 \\ I_2 - I_o = 0 \end{cases} \tag{3.3}$$

After algebraic manipulation of the first and third equations in (3.3), the voltage transfer ratio of proposed converter is obtained as:

$$M = \frac{V_2}{V_{dc}} = 2 - \frac{1}{D} \tag{3.4}$$

Fig. 3-5(a) shows the plot of M versus D, where a bipolar voltage output is achieved when the duty cycle varies around 0.5 (⅓<D<1).

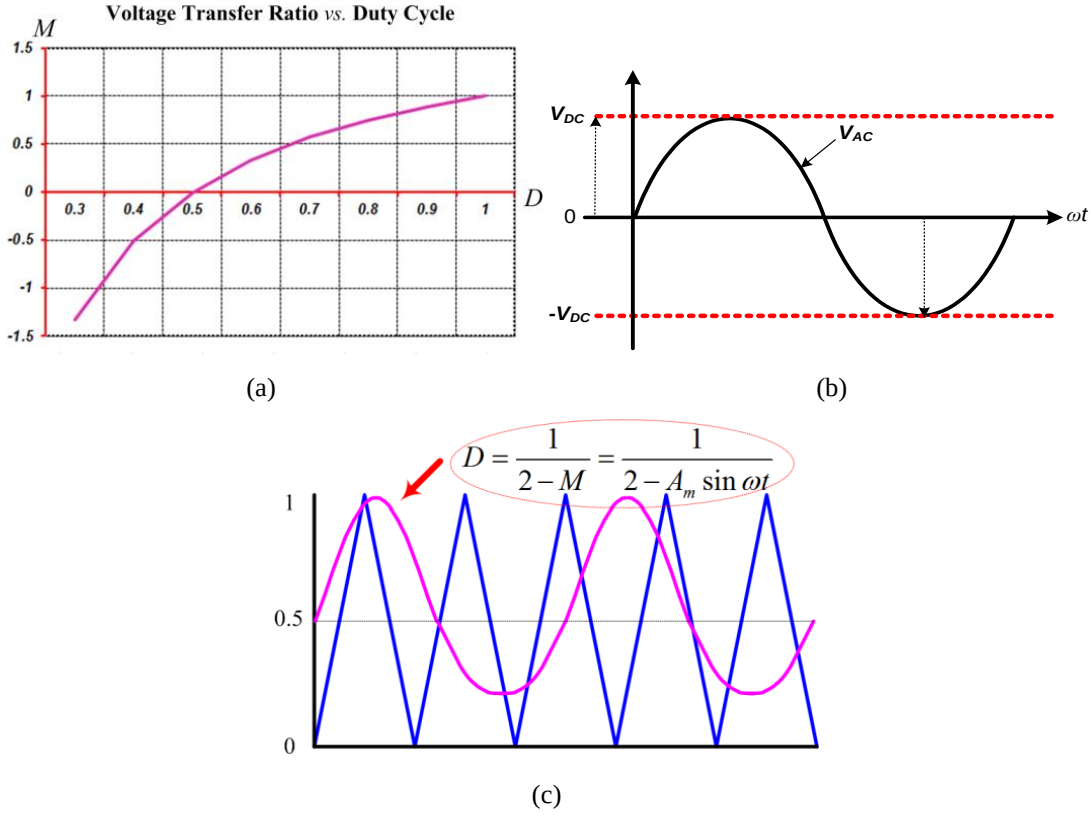
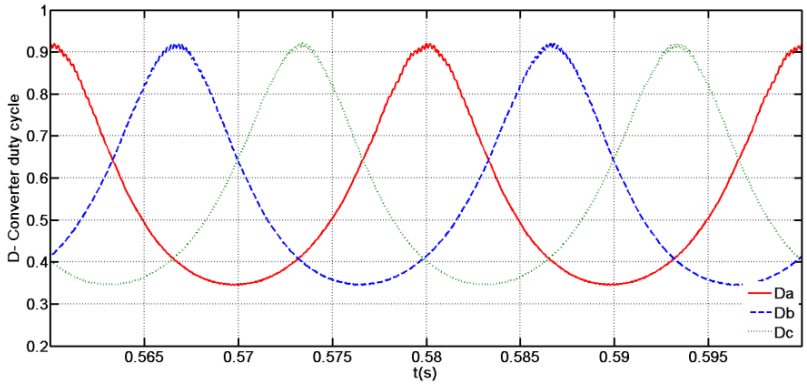


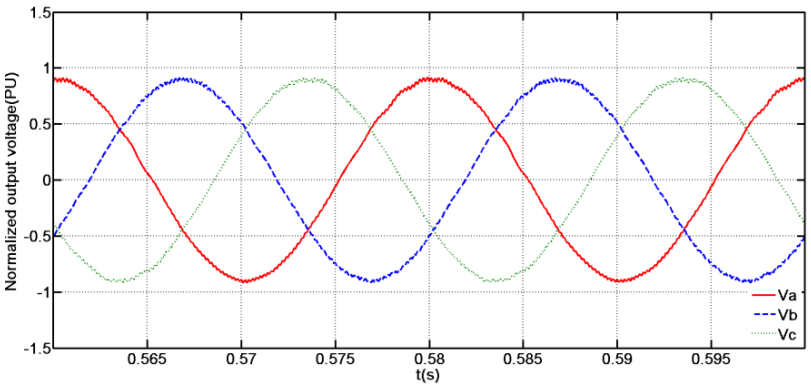
Fig. 3-5. Voltage output range and modulation for the proposed converter: (a) voltage transfer ratio versus duty cycle; (b) AC side output voltage range; and (c) open loop modulation strategy based on transfer ratio.

From Fig. 3-5(b), the maximum modulation index is 1pu for the peak value of phase voltage (V_{dc}), which is twice that in the two-level converter (½V_{dc}). Due to this large extension in the DC rail utilization, reduced DC-link voltage and dv/dt can be achieved. With the specifications of: f_{sw}=5kHz; V_{dc}=200V; L_1=2mH; C_1=10μF;

L_2=5mH; C_2=10μF, the proposed converter has been accessed with single-phase configuration in several cases. The simulated output voltage and modulating signal are shown in Fig. 3-6 with predefined duty cycle range of 0.33 to 1.



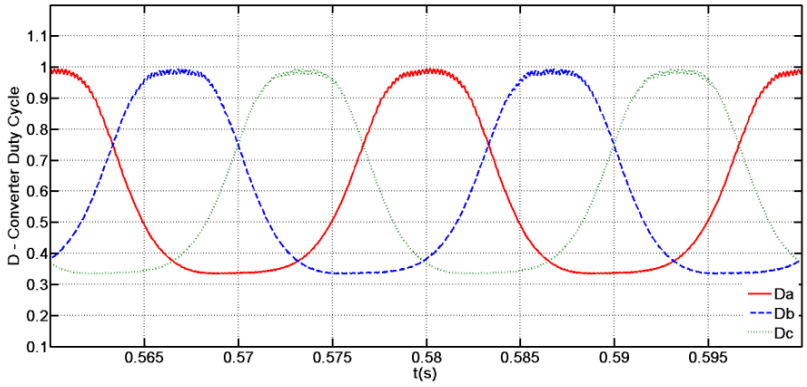
(a)



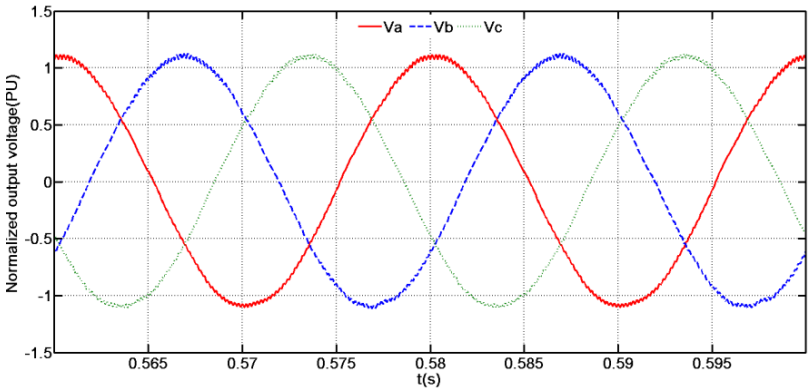
(b)

Fig. 3-6. Simulated output voltage and modulating signal for ACVD converter: (a) duty cycle and (b) normalized three-phase output voltage.

As in a conventional two-level converter, triplen injection can further improve the DC-link voltage utilization of ACVD converter by 15.5%. The modulating signals and output voltages for this case are shown in Fig. 3-7, where the fundamental output voltage can exceed 1pu. This conclusion can be generalized to all modulation methods that indirectly utilize the 3rd harmonic or other forms of zero sequence components to increase fundamental output voltage, such as SVM, switching frequency optimal (SFO) and SHE. However, the main drawback of the methods that exploit zero sequence harmonics is the appearance of the low order harmonics in the output voltage according to (3.4), predominantly the 2nd and 4th. These low order harmonics can be actively controlled with small modulation index sacrifice, especially when the load current is high.



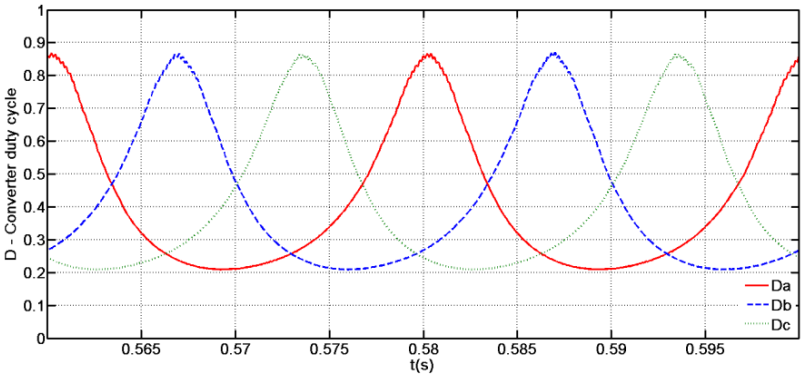
(a)



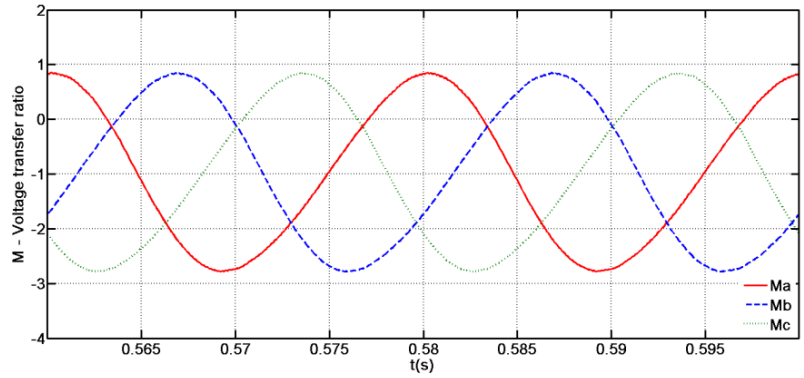
(b)

Fig. 3-7. Simulated output voltage and modulating signal for ACVD converter with triplen component injection: (a) duty cycle and (b) normalized three-phase output voltage.

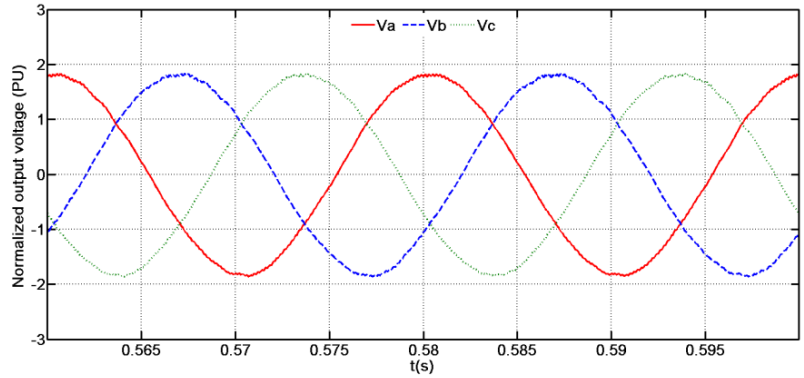
Additional improvement of DC link utilization improvement can be achieved when a negative DC bias is injected into modulating signal. Based on (3.4), the duty cycle range from 0.2 to 1 corresponding to the output phase voltage (relative to negative bus) from $-3V_{dc}$ to V_{dc}. By cancellation of the DC bias in line-to-line voltage of the three-phase system, the DC utilization of the ACVD converter can be doubled to 2pu, but increasing the power switch voltage stresses. This is verified by simulation in Fig. 3-8. Due to practical semiconductor voltage rating limits and a requirement for zero average CM voltage, the remainder of this chapter does not utilize the zero sequence component or negative DC bias injection.



(a)



(b)



(c)

Fig. 3-8. Voltage output range and modulation for ACVD converter using DC bias cancellation: (a) duty cycle and (b) converter voltage transfer ratio; and (c) normalized output voltage.

The inner capacitance is significantly less than that of the DC-link because of its fluctuating voltage. The asymmetry between the two voltage polarities synthesized during modes 1 and 2 potentially distorts the output voltage by even order harmonics when the modulation strategy in Fig. 3-5(c) is adopted. As a result, proper converter operation with sinusoidal AC side voltage and current requires modulation strategy counter-measures to neutralize the negative impact of such distortion, which is investigated in later sections.

From this discussion of single-phase ACVD-VSC, it is seen that the DC-link and AC side share the common ground. Consequently, in the three-phase three-wire system, the average CM voltage between the DC-link ground and AC neutral point is zero for balanced conditions.

3.3 Performance Evaluation of Voltage/Current Stresses and the Integrated Magnetic Design

In this section, analysis of the voltage/current stresses of power switches and some design issues of the passive components, are considered. Since the IBBC exerts extra voltage/current stresses on the devices, it is important to explore the quantitative relationship between switch electrical stresses and output power. An integrated magnetic technique can be employed to integrate the two inductors into one magnetic core, compacting the installation and reducing the magnetic cost.

A. Voltage Stress Analysis

According to (3.3), the voltage on C_1 and C_2 are given by (3.5) and (3.6) respectively. The opposite polarity of V_{dc} and V_1 offers the possibility to generate the bipolar voltage on C_2.

$$V_1 = (1-1/D)V_{dc} \tag{3.5}$$

$$V_2 = (2-1/D)V_{dc} \tag{3.6}$$

Consequently, the reverse blocked voltage of the power switches S_1 and S_2 can be calculated from:

$$V_{RB} = V_{dc} - V_1 = V_{dc}/D \tag{3.7}$$

Since the maximum output-input voltage ratio is A_m, the voltage stress is then given by (3.8).

$$V_{RB} = (2-M)V_{dc} = (2-A_m \sin \omega t)V_{dc} \tag{3.8}$$

In Fig. 3-5(a), the duty cycle D varies from 0.33-1.0 at the maximum output condition ($\pm V_{dc}$) when A_m is 1. The maximum voltage stress on the power switches is twice the DC voltage plus the peak of the output phase voltage. Compared with the two-level topology, the voltage stresses are increased by 50% during extreme conditions, but the AC output voltage is twice of that in two-level topology. This attribute is achieved by the incorporation of IBBCs. The fluctuating voltage across C_1 makes small value AC capacitance viable but this is traded for increased power switch ratings [20].

B. Current Stress Analysis

Manipulation of (3.3) for the current state variables, gives equations (3.9) and (3.10), where currents i_1 and i_2 are in opposite directions, which is necessary for the energy balance of C_1.

$$I_1 = (1-1/D)I_2 \tag{3.9}$$

$$I_2 = V_2 / R = I_o \tag{3.10}$$

The current of the IBBC inductor i_1 passes through either S_1 or S_2 to alternatively store and release energy. From Fig. 3-4, the total power switch current is the sum of the absolute value of the two current state variables. Since I_1 and I_2 are in opposite directions, the total current stress of each switch is expressed as (3.11).

$$I_c = |I_1| + |I_2| = |I_1 - I_2| \tag{3.11}$$

In general, the power switch current is (3.12), where φ is the power factor angle, ω is the angular frequency of the output voltage, and I_{om} is the maximum load current.

$$I_c = |I_1 - I_2| = (I_{om} / D) \cdot \sin(\omega t + \varphi) \tag{3.12}$$

Considering (3.4), equation (3.12) can be developed as in (3.13):

$$I_c = (2 - A_m \sin \omega t) I_{om} \sin(\omega t + \varphi) \tag{3.13}$$

Second order harmonic current is introduced by the IBBC. The peak power switch current occurs when (3.13) reaches the maximum. An approximate margin of three times the load current should be considered in a practical ACVD converter design. The output current of this converter is approximately half that of two-level topology under for the same DC-link and same power rating, since its output voltage is doubled, which reduces the current stress levels.

C. Passive Device Selection

(a) (b)

Fig. 3-9. Equivalent model of the power path for the inner capacitor C_1 of the ACVD converter: (a) S_2 is on, S_1 is off and (b) S_1 is on, S_2 is off.

Since L_2 and C_2 form the output filter, L_2 and C_2 can be selected based on the filter design methods of the conventional two-level VSC, as presented in [21]. L_1 and C_1 are selected based on the switching model from an AC point of view since all the

state variables are AC. The equivalent power paths for the inner capacitor C_1 are shown in Fig. 3-9. When S_2 is on and S_1 is off, inner capacitor C_1 is in series with output filter inductor L_2 as in Fig. 3-9(a). In order to make the AC component of the voltage across C_1 follow the output voltage and avoid a large high frequency oscillation on C_1, the resonant frequency of C_1 and L_2 is placed between the fundamental and switching frequencies (f_0 and f_{sw}). With L_2, C_2 and f_{sw} known; the geometrical mean in (3.14) is used to calculate C_1.

$$f_r = 1/(2\pi \cdot \sqrt{C_1 L_2}) = \sqrt{f_0 f_{sw}} \tag{3.14}$$

In the proposed ACVD converter, the inner inductor L_1 is employed as a buffer for energy transfer from the DC-link to C_1 in the periods where the upper switch of each phase leg is on. It has similar function as MMC arm inductance in limiting inrush current from capacitor C_1 when the upper switch of each phase leg is on [22]. In Fig. 3-9(b), L_1 and C_1 are in series. Large L_1 causes a large fundamental voltage drop and limits the magnitude of the high frequency current ripple. In this sense, the characteristic impedance of L_1 and C_1 in (3.15) should be used as a compromise between the output power range and ripple current demand.

$$z_0 = \sqrt{L_1 / C_1} \tag{3.15}$$

D. Potential Magnetic Integration

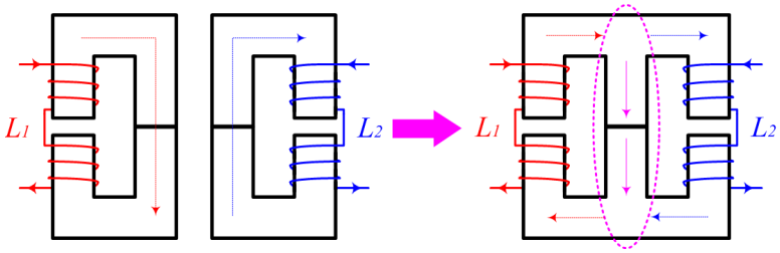


Fig. 3-10. Principles of the integrated magnetic solution.

In order to improve the power density, magnetic integration of L_1 and L_2 into one core is viable for the IBBC inductor and output filtering inductor [23-25]. Fig. 3-10 interprets the solution for the magnetic integration, where a three-leg EE type magnetic core is employed per phase. Air gaps are inserted into the two outer legs while no air gap exists in the center leg (thereby presenting low reluctance to fluxes from the legs). The IBBC inductor L_1 is wound around one outer leg and the filtering inductor L_2 is inversely wound around the other outer leg. In this way, the magneto-motive force will be distributed mostly on the outer legs due to the high reluctance

produced by the air gaps and the two inductors can be decoupled effectively (low reluctance in the center leg). Fig. 3-10 shows that the flux linkages of the two inductors oppose, so the average flux component in the center leg is reduced; thus, a smaller cross section area center leg can be used. The power density and the efficiency can be enhanced with the proposed magnetic integration method. However, this approach is restricted to low and medium power stages due to the limited window area of commercial high magneto-conductivity cores.

3.4 Three-phase ACVD-VSC Modelling and Analysis in the Synchronous Reference Frame

The Park transformation based decoupling model for the three-phase two-level VSC is generally used to implement independent control of active and reactive power. Since the references become DC values in the SRF, zero steady state errors are expected with a proportional-integral (PI) controller. In this section, the proposed ACVD-VSC is modelled in the SRF to give insight into the control design. Resistive load conditions are assumed and in the following control design section for simplicity. In other load conditions, the load current can be treated as a new state variable, which increases the order of state space equations and transfer functions. However, the general design procedure remains the same.

The ACVD converter can form a three-phase four-wire system, when the DC and AC grounds are connected. Thus, each phase can be controlled independently. This configuration can be employed in UPS and aero-space applications. However, the following analysis is based on a three-phase three-wire system.

A. The Inverter Mode

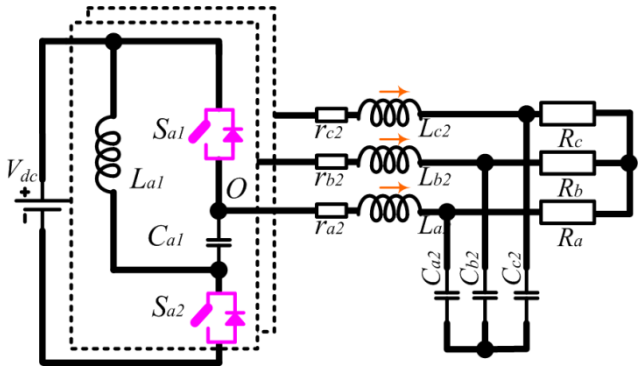


Fig. 3-11. Rearrangement for the proposed three-phase inverter.

Rearrangement of the three-phase ACVD-VSC as a standalone inverter is depicted in Fig. 3-11. From the instantaneous state space equations in (3.1) and the assumptions in (3.16), the three-phase AC side equations can be expressed as in (3.17).

$$\begin{cases} L_2 = L_{a2} = L_{b2} = L_{c2} \\ C_2 = C_{a2} = C_{b2} = C_{c2} \\ R = R_a = R_b = R_c \\ r_2 = r_{a2} = r_{b2} = r_{c2} \end{cases} \tag{3.16}$$

$$\begin{cases} L_2 \dfrac{d}{dt}\begin{bmatrix} i_{a2}-i_{b2} \\ i_{b2}-i_{c2} \\ i_{c2}-i_{a2} \end{bmatrix} = \begin{bmatrix} v_a - v_b \\ v_b - v_c \\ v_c - v_a \end{bmatrix} - r_2 \begin{bmatrix} i_{a2}-i_{b2} \\ i_{b2}-i_{c2} \\ i_{c2}-i_{a2} \end{bmatrix} - \begin{bmatrix} v_{a2}-v_{b2} \\ v_{b2}-v_{c2} \\ v_{c2}-v_{a2} \end{bmatrix} \\ RC_2 \dfrac{d}{dt}\begin{bmatrix} v_{a2}-v_{b2} \\ v_{b2}-v_{c2} \\ v_{c2}-v_{a2} \end{bmatrix} = R\begin{bmatrix} i_{a2}-i_{b2} \\ i_{b2}-i_{c2} \\ i_{c2}-i_{a2} \end{bmatrix} - \begin{bmatrix} v_{a2}-v_{b2} \\ v_{b2}-v_{c2} \\ v_{c2}-v_{a2} \end{bmatrix} \end{cases} \tag{3.17}$$

$$\triangleq \begin{cases} L_2 \dfrac{d}{dt}\begin{bmatrix} i_{ab2} \\ i_{bc2} \\ i_{ca2} \end{bmatrix} = \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} - r_2 \begin{bmatrix} i_{ab2} \\ i_{bc2} \\ i_{ca2} \end{bmatrix} - \begin{bmatrix} v_{ab2} \\ v_{bc2} \\ v_{ca2} \end{bmatrix} \\ RC_2 \dfrac{d}{dt}\begin{bmatrix} v_{ab2} \\ v_{bc2} \\ v_{ca2} \end{bmatrix} = R\begin{bmatrix} i_{ab2} \\ i_{bc2} \\ i_{ca2} \end{bmatrix} - \begin{bmatrix} v_{ab2} \\ v_{bc2} \\ v_{ca2} \end{bmatrix} \end{cases}$$

where $\{v_a, v_b, v_c\}$ represents converter output phase voltage (measured from poles $O=\{O_1,O_2,O_3\}$ relative to ground), and V_{dc} is the DC side input voltage. R and r_2 are the load and filter reactor L_2 resistances respectively.

With the definition of u in (3.2), the extended three-phase switching function can be denoted as in (3.18). The converter output voltage is then defined in (3.19). The proposed converter exhibits some time-variant behaviour that makes the decoupled large signal modelling infeasible. Thus, approximations are made to facilitate the development of the fundamental average model which is necessary for control design and analysis simplicity.

$$u_i = \begin{cases} 1, & S_{i1} \quad turns\ on \\ 0, & S_{i2} \quad turns\ on \end{cases} \quad (i = a,b,c) \tag{3.18}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} V_{dc} + \begin{bmatrix} 1-u_a & 0 & 0 \\ 0 & 1-u_b & 0 \\ 0 & 0 & 1-u_c \end{bmatrix} \begin{bmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \end{bmatrix} \tag{3.19}$$

To synthesize sinusoidal output voltages based on (3.5), the IBBC voltage can be expected to contain both DC and AC components. According to (3.13), second order harmonic current emerge in the IBBC inductor. Therefore, the IBBC capacitor AC voltage contains both fundamental and second order harmonics. When neglecting the second order harmonics, (3.20) is obtained. After application of the classical average method to the switching function, equation (3.19) is rearranged into (3.21), which can be simplified to (3.22),

$$\begin{bmatrix} v_{a1} \\ v_{b1} \\ v_{c1} \end{bmatrix} \approx -\begin{bmatrix} V_{dc} \\ V_{dc} \\ V_{dc} \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.20}$$

$$\begin{bmatrix} \overline{v_a} \\ \overline{v_b} \\ \overline{v_c} \end{bmatrix} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} V_{dc} + \begin{bmatrix} d_a - 1 & 0 & 0 \\ 0 & d_b - 1 & 0 \\ 0 & 0 & d_c - 1 \end{bmatrix} \begin{bmatrix} V_{dc} - \overline{v_a} \\ V_{dc} - \overline{v_b} \\ V_{dc} - \overline{v_c} \end{bmatrix} \tag{3.21}$$

$$\begin{bmatrix} \overline{v_a} \\ \overline{v_b} \\ \overline{v_c} \end{bmatrix} = \begin{bmatrix} 2 - 1/d_a \\ 2 - 1/d_b \\ 2 - 1/d_c \end{bmatrix} V_{dc} \triangleq \begin{bmatrix} m_a \\ m_b \\ m_c \end{bmatrix} V_{dc} \tag{3.22}$$

where $\{d_a, d_b, d_c\}$ is the duty ratio for each phase, $\{m_a, m_b, m_c\}$ is the equivalent transfer ratio and '—' is the averaging operator over one switching cycle.

By defining $\{m_{ab}, m_{bc}, m_{ca}\}=\{m_a-m_b, m_b-m_c, m_c-m_a\}$, the switching averaged AC side equations can be derived as in (3.23). Park transformation of the form in (3.24) is then applied to obtain the equivalent time-invariant system. The decoupling model of the proposed ACVD inverter in the SRF becomes (3.25).

$$\begin{cases} L_2 \dfrac{d}{dt} \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} = \begin{bmatrix} m_{ab} \\ m_{bc} \\ m_{ca} \end{bmatrix} V_{dc} - r_2 \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \begin{bmatrix} \overline{v_{ab2}} \\ \overline{v_{bc2}} \\ \overline{v_{ca2}} \end{bmatrix} \\ C_2 \dfrac{d}{dt} \begin{bmatrix} \overline{v_{ab2}} \\ \overline{v_{bc2}} \\ \overline{v_{ca2}} \end{bmatrix} = \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \dfrac{1}{R} \begin{bmatrix} \overline{v_{ab2}} \\ \overline{v_{bc2}} \\ \overline{v_{ca2}} \end{bmatrix} \end{cases} \tag{3.23}$$

$$T = \frac{2}{3} \begin{bmatrix} \cos \omega t & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ -\sin \omega t & -\sin(\omega t - 2\pi/3) & -\sin(\omega t + 2\pi/3) \\ ½ & ½ & ½ \end{bmatrix} \tag{3.24}$$

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix}\overline{i_{2d}}\\ \overline{i_{2q}}\end{bmatrix} = -\dfrac{1}{L_2}\begin{bmatrix}\overline{v_{2d}}\\ \overline{v_{2q}}\end{bmatrix} - \begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\overline{i_{2d}}\\ \overline{i_{2q}}\end{bmatrix} - \dfrac{r_2}{L_2}\begin{bmatrix}\overline{i_{2d}}\\ \overline{i_{2q}}\end{bmatrix} + \dfrac{V_{dc}}{L_2}\begin{bmatrix}m_d\\ m_q\end{bmatrix} \\ \dfrac{d}{dt}\begin{bmatrix}\overline{v_{2d}}\\ \overline{v_{2q}}\end{bmatrix} = \dfrac{1}{C_2}\begin{bmatrix}\overline{i_{2d}}\\ \overline{i_{2q}}\end{bmatrix} - \begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\cdot\begin{bmatrix}\overline{v_{2d}}\\ \overline{v_{2q}}\end{bmatrix} - \dfrac{1}{RC_2}\begin{bmatrix}\overline{v_{2d}}\\ \overline{v_{2q}}\end{bmatrix} \end{cases} \tag{3.25}$$

The mentioned second order harmonic distortion problem must be treated separately with additional control loops to ensure pure sinusoidal output voltage and current, and will be covered in later part of this chapter.

B. The Rectifier Mode

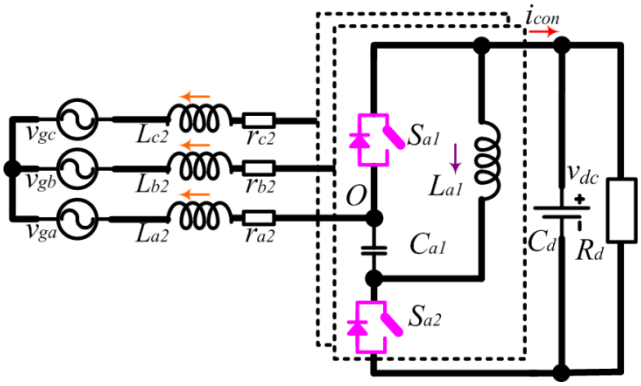


Fig. 3-12. Rearrangement for the proposed three-phase rectifier.

Fig. 3-12 shows the proposed ACVD-VSC when configured as a rectifier. The AC side and DC side equations are shown in (3.26), in which $\{v_{gab}, v_{gbc}, v_{gca}\}=\{v_{ga}-v_{gb}, v_{gb}-v_{gc}, v_{gc}-v_{ga}\}$ represents the AC input voltage, v_{dc} is the output voltage, and i_{con} in (3.27) is the total current from the converter to the DC side.

The second order current component in the IBBC inductor is neglected temporarily. From (3.9) and by utilizing the switching average operator, (3.27) develops into (3.28). After substituting (3.22) and (3.28) into (3.26), the standard form of the proposed rectifier model is given as in (3.29).

$$\begin{cases} L_2\dfrac{d}{dt}\begin{bmatrix}i_{ab2}\\ i_{bc2}\\ i_{ca2}\end{bmatrix} = \begin{bmatrix}v_{ab}\\ v_{bc}\\ v_{ca}\end{bmatrix} - r_2\begin{bmatrix}i_{ab2}\\ i_{bc2}\\ i_{ca2}\end{bmatrix} - \begin{bmatrix}v_{gab}\\ v_{gbc}\\ v_{gca}\end{bmatrix} \\ C_d\dfrac{dv_{dc}}{dt} = i_{con} - \dfrac{v_{dc}}{R_d} \end{cases} \tag{3.26}$$

$$i_{con} = -\begin{bmatrix}u_a & u_b & u_c\end{bmatrix}\cdot\begin{bmatrix}i_{a2}\\ i_{b2}\\ i_{c2}\end{bmatrix} - \begin{bmatrix}1-u_a & 1-u_b & 1-u_c\end{bmatrix}\cdot\begin{bmatrix}i_{a1}\\ i_{b1}\\ i_{c1}\end{bmatrix} \tag{3.27}$$

$$\overline{i_{con}} = -\begin{bmatrix} m_a & m_b & m_c \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{a2}} \\ \overline{i_{b2}} \\ \overline{i_{c2}} \end{bmatrix} = -\begin{bmatrix} m_{ab} & m_{bc} & m_{ca} \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} \tag{3.28}$$

$$\begin{cases} L_2 \dfrac{d}{dt} \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} = \begin{bmatrix} m_{ab} \\ m_{bc} \\ m_{ca} \end{bmatrix} \overline{v_{dc}} - r_2 \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \begin{bmatrix} \overline{v_{gab}} \\ \overline{v_{gbc}} \\ \overline{v_{gca}} \end{bmatrix} \\ C_d \dfrac{d\overline{v_{dc}}}{dt} = -\begin{bmatrix} m_{ab} & m_{bc} & m_{ca} \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{ab2}} \\ \overline{i_{bc2}} \\ \overline{i_{ca2}} \end{bmatrix} - \dfrac{\overline{v_{dc}}}{R_d} \end{cases} \tag{3.29}$$

Using Park transformation to achieve (3.30), which clarifies the model of the proposed ACVD rectifier in the SRF.

$$\begin{cases} \dfrac{d}{dt} \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} = -\dfrac{1}{L_2} \begin{bmatrix} \overline{v_{gd}} \\ \overline{v_{gq}} \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} - \dfrac{r_2}{L_2} \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} + \dfrac{\overline{v_{dc}}}{L_2} \begin{bmatrix} m_d \\ m_q \end{bmatrix} \\ \dfrac{d\overline{v_{dc}}}{dt} = -\dfrac{1}{C_d} \begin{bmatrix} m_d & m_q \end{bmatrix} \cdot \begin{bmatrix} \overline{i_{2d}} \\ \overline{i_{2q}} \end{bmatrix} - \dfrac{\overline{v_{dc}}}{R_d C_d} \end{cases} \tag{3.30}$$

Similar as the inverter mode analysis, the *o* axis is omitted in (3.30) for three-phase three-wire rectifier system. Second order harmonic distortion occurs in the line current if no suppression is applied. Thus, an extra control loop is necessary to calibrate the modulating signal to obtain line current with low total harmonic distortion (THD).

C. The Second Order Distortion

The second order distortion can be explained by using the classical transfer function method. The quasi-static analysis is employed to reveal the system gain scheduling at different operational points.

Using the single-phase inverter in Fig. 3-2(b) with resistive load R_o as an example, the switching average large signal model is shown in (3.31). The Taylor series based linearization method is employed for a fixed operation point to obtained state space equations and the transfer function for perturbations near the selected state. Then, (3.31) can be linearized into (3.32). Using Laplace transformation yields the transfer function G_{v2d}, which is shown in (3.33).

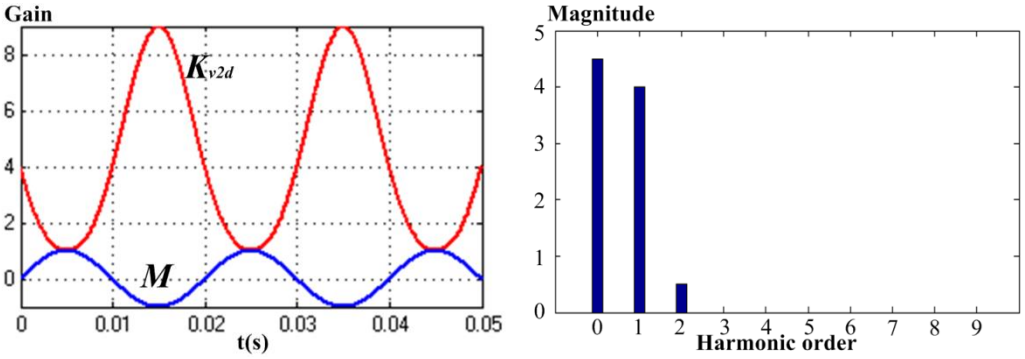
$$\begin{cases} L_1 \dfrac{d\overline{i_1}}{dt} = d(\overline{v_1} - V_{dc}) + V_{dc} \\ C_1 \dfrac{d\overline{v_1}}{dt} = d(\overline{i_2} - \overline{i_1}) - \overline{i_2} \\ L_2 \dfrac{d\overline{i_2}}{dt} = d(V_{dc} - \overline{v_1}) + (\overline{v_1} - \overline{v_2}) \\ C_2 \dfrac{d\overline{v_2}}{dt} = \overline{i_2} - \dfrac{\overline{v_2}}{R_o} \end{cases} \tag{3.31}$$

$$\begin{cases} L_1 \dfrac{d\Delta i_1}{dt} = D_0 \Delta v_1 + (V_1 - V_{dc})\Delta d \\ C_1 \dfrac{d\Delta v_1}{dt} = -(1-D_0)\Delta i_2 - D_0 \Delta i_1 + (I_2 - I_1)\Delta d \\ L_2 \dfrac{d\Delta i_2}{dt} = (1-D_0)\Delta v_1 - (V_1 - V_{dc})\Delta d - \Delta v_2 \\ C_2 \dfrac{d\Delta v_2}{dt} = \Delta i_2 - \dfrac{\Delta v_2}{R_o} \end{cases} \tag{3.32}$$

$$\begin{aligned} G_{v2d} &= \frac{\Delta v_2(s)}{\Delta d(s)} = \frac{V_{dc} + A_1 s + A_2 s^2}{D^2 + B_1 s + B_2 s^2 + B_3 s^3 + B_4 s^4} \\ A_1 &= L_1(1-D_0)(I_2 - I_1) \\ A_2 &= L_1 C_1 \frac{V_{dc}}{D_0} \\ B_1 &= \frac{(1-D_0)^2 L_1 + D_0{}^2 L_2}{R_o} \\ B_2 &= L_1 C_1 + D_0{}^2 L_2 C_2 + (1-D_0)^2 L_1 C_2 \\ B_3 &= \frac{L_1 C_1 L_2}{R_o} \\ B_4 &= L_1 C_1 L_2 C_2 \end{aligned} \tag{3.33}$$

Assuming the DC input voltage is 1pu and the modulation index is 1, when the operation point varies sinusoidally, the loop gain K_{v2d} is not constant as it is for a two-level converter. Periodical oscillation occurs mainly focused on fundamental and second order components as shown in Fig. 3-13. Both the zeroes and poles drift due to the duty cycle variation. The proposed converter exhibit second order distortion and a minimal third order component as by-products when operated in open loop. With a normal time-domain PI controller, the output voltage will be distorted due to the non-uniform loop gain distribution and the floating poles/zeroes. As a result, zero

steady state error is difficult to be obtained by instantaneous value control, especially under heavy load situations.



(a) (b)

Fig. 3-13. Loop gain scheduling along sinusoidal operation points: (a) loop gain versus transfer ratio and (b) FFT analysis of the loop gain oscillation.

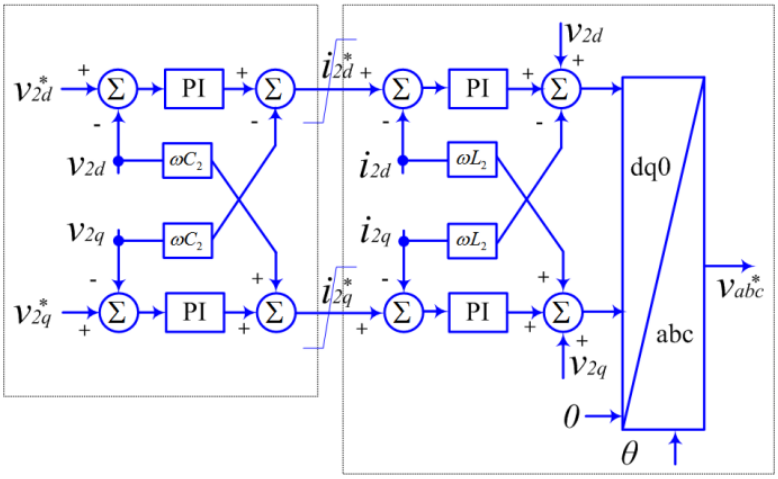
The reason for this phenomenon is that the proposed converter exhibits internal inertia, thus cannot be viewed as an ideal amplifier to the modulating signal due to its time variant features. The same applies when investigating the transfer function G_{i2d} for the single-phase ACVD rectifier. Although passive components sizing can alleviate this problem to some extent, the design degree of freedom will be constrained and the passive devices will be large. So a software solution is preferred, which is considered in the next section.

3.5 ACVD-VSC Control Strategies for Inverter and Rectifier Modes

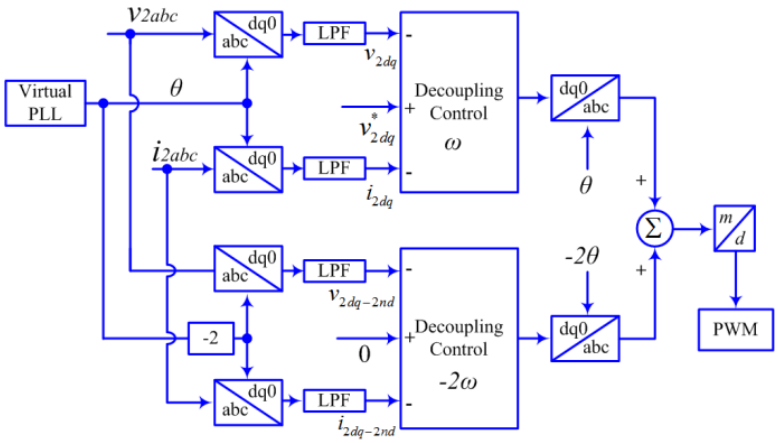
In this section, the controller designs for both the inverter and rectifier modes are facilitated in state space. Based on the converter decoupling model in the SRF, the PI controller is sufficient to achieve zero steady state error. The transfer functions can be investigated by using root locus analysis to determine the proportional gain and integral rate for the closed loop in each control layer.

3.5.1 Control Design for Standalone Inverter Mode

The ACVD converter operates as a standalone inverter in the voltage control mode, where the main objective is to establish a stiff AC voltage bus across the load with a pre-fined frequency. Based on the SRF model in (3.25) where the voltage vector is aligned with the *d*-axis, the decoupling control scheme summarized in Fig. 3-14(a) is developed. The detailed transfer function is derived as follows.



(a)



(b)

Fig. 3-14. Control structure in standalone inverter mode: (a) two layers decoupling control and (b) overview of the control diagram including the second order harmonic eliminating loop.

Rewriting (3.25) into (3.34) for simplification, the terms $\{\chi_d, \chi_q\}$ and $\{\lambda_d, \lambda_q\}$ can be obtained from the PI controllers in the closed loop system.

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = \dfrac{1}{L_2}\begin{bmatrix} \chi_d \\ \chi_q \end{bmatrix} - \dfrac{r_2}{L_2}\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} \\ \dfrac{d}{dt}\begin{bmatrix} v_{2d} \\ v_{2q} \end{bmatrix} = \dfrac{1}{C_2}\begin{bmatrix} \lambda_d \\ \lambda_q \end{bmatrix} - \dfrac{1}{RC_2}\begin{bmatrix} v_{2d} \\ v_{2q} \end{bmatrix} \end{cases} \tag{3.34}$$

$$\begin{aligned} \chi_d &= V_{dc}m_d - v_{2d} + \omega L_2 i_{2q} = K_{ip}(i_{2d}^* - i_{2d}) + K_{ii}\int (i_{2d}^* - i_{2d})dt \\ \chi_q &= V_{dc}m_q - v_{2q} - \omega L_2 i_{2d} = K_{ip}(i_{2q}^* - i_{2q}) + K_{ii}\int (i_{2q}^* - i_{2q})dt \\ \lambda_d &= i_{2d} + \omega C_2 v_{2q} = K_{vp}(v_{2d}^* - v_{2d}) + K_{vi}\int (v_{2d}^* - v_{2d})dt \\ \lambda_q &= i_{2q} - \omega C_2 v_{2d} = K_{vp}(v_{2q}^* - v_{2q}) + K_{vi}\int (v_{2q}^* - v_{2q})dt \end{aligned} \tag{3.35}$$

From (3.34), (3.35) and the definition in (3.36), the state space equations for the direct axis current and voltage loop can be derived as in (3.37).

$$\begin{cases} F_{i2d} = \int (i_{2d}^{*} - i_{2d})dt \\ F_{v2d} = \int (v_{2d}^{*} - v_{2d})dt \end{cases} \tag{3.36}$$

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} = \begin{bmatrix} -\dfrac{K_{ip}+r_2}{L_2} & \dfrac{K_{ii}}{L_2} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} + \begin{bmatrix} \dfrac{K_{ip}}{L_2} \\ 1 \end{bmatrix} i_{2d}^{*} \\ \dfrac{d}{dt}\begin{bmatrix} v_{2d} \\ F_{v2d} \end{bmatrix} = \begin{bmatrix} -\dfrac{K_{vp}R+1}{RC_2} & \dfrac{K_{vi}}{C_2} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{2d} \\ F_{v2d} \end{bmatrix} + \begin{bmatrix} \dfrac{K_{vp}}{C_2} \\ 1 \end{bmatrix} v_{2d}^{*} \end{cases} \tag{3.37}$$

In (3.34), since the quadrature axis has the same structure as the direct axis, the transfer functions can be similarly derived as in (3.38).

$$\begin{cases} G_{i2} = \dfrac{i_{2d}}{i_{2d}^{*}} = \dfrac{i_{2q}}{i_{2q}^{*}} = \dfrac{K_{ii} + sK_{ip}}{K_{ii} + s(r_2 + K_{ip}) + s^2 L_2} \\ G_{v2} = \dfrac{v_{2d}}{v_{2d}^{*}} = \dfrac{v_{2q}}{v_{2q}^{*}} = \dfrac{K_{vi} + sK_{vp}}{K_{vi} + s(1/R + K_{vp}) + s^2 C_2} \end{cases} \tag{3.38}$$

Consequently, the current controller reference and the modulating signal into the PWM module can be derived as (3.39), which is in accordance with Fig. 3-14(a).

$$\begin{aligned} U_{2d}^{*} &= \chi_d + v_{2d} - \omega L_2 i_{2q} \\ U_{2q}^{*} &= \chi_q + v_{2q} + \omega L_2 i_{2d} \\ i_{2d}^{*} &= \lambda_d - \omega C_2 v_{2q} \\ i_{2q}^{*} &= \lambda_q + \omega C_2 v_{2d} \end{aligned} \tag{3.39}$$

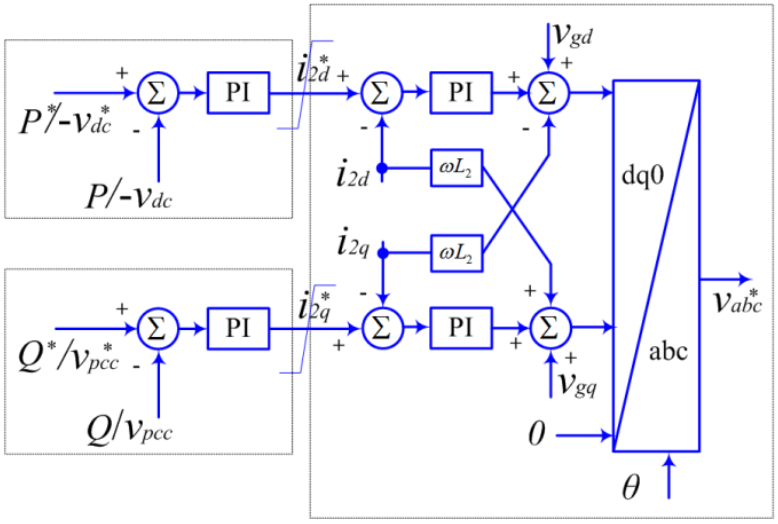
The outer loop of the control structure in Fig. 3-14(a) regulates the AC voltage at the load and sets the reference currents (i_{2d}* and i_{2q}*) to the inner current loop. The inner current loop regulates the load current and prevents converter over-loading, and also generates the first version of the modulating signals {m_{ab}, m_{bc}, m_{ca}}, which will be modified to {m_a, m_b, m_c} and then {d_a, d_b, d_c} for the modulator to generate the gating signals for the switching devices.

The ACVD converter has the same structure in the SRF for all frequencies where $n\omega$ (where n=±1, ±2, ±3…) is the rotational rate under balanced conditions. Thus, the second order distortion problem can be solved by adding an eliminating loop in the -2ω SRF that forces its d-q components to zero as shown in Fig. 3-14(b). The decoupling control block for the harmonic eliminating loop is the same as that for the fundamental voltage and current in Fig. 3-14(a). Low pass filters (LPFs) produce the

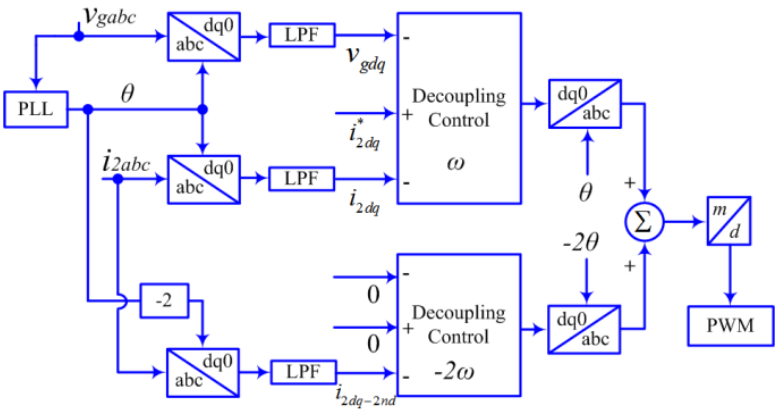
d-q components for each frequency. The supplementary loop output that suppresses the second harmonic is added to the fundamental voltage and current loop that is responsible for power transfer between the converter AC and DC sides.

3.5.2 Control Design for Rectifier and Grid-connected Inverter Modes

For completeness, the control diagram for the proposed converter in a rectifier/grid-connected inverter mode is shown in Fig. 3-15(a), where the outer control layers that generate the reference currents for the inner current controllers are determined by the operational circumstances and control targets. In the rectifier mode, unity power factor is of concerned, thus the quadrature current command is set to zero, while the direct current is decided by the DC voltage controller. In distributed energy resource (DER) applications where energy management is necessary, the active power (DC side voltage) and reactive power control layers generate the references for *d*-axis and *q*-axis currents respectively. If the DER interfacing inverter is connected to a local microgrid, then a voltage support function may be needed, where the point of common coupling (PCC) AC voltage is controlled in the outer layer [26, 27].



(a)



(b)

Fig. 3-15. Control structure in rectifier/grid-connected inverter mode: (a) two layers decoupling control and (b) overview of the control diagram including the second order elimination loop.

Taking the rectifier mode as an example, the transfer functions for the two-layer controller can be derived as follows. Rearranging (3.30) into (3.40), where the terms $\{\gamma_d, \gamma_q\}$ and η are obtained from the PI controllers in closed loop.

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = \dfrac{1}{L_2}\begin{bmatrix} \gamma_d \\ \gamma_q \end{bmatrix} - \dfrac{r_2}{L_2}\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} \\ \dfrac{dv_{dc}}{dt} = \dfrac{1}{C_d}\eta - \dfrac{v_{dc}}{R_d C_d} \end{cases} \tag{3.40}$$

$$\begin{aligned} \gamma_d &= v_{dc}m_d - v_{gd} + \omega L_2 i_{2q} = K_{ip}^{'}(i_{2d}^{*} - i_{2d}) + K_{ii}^{'}\int (i_{2d}^{*} - i_{2d})dt \\ \gamma_q &= v_{dc}m_q - v_{gq} - \omega L_2 i_{2d} = K_{ip}^{'}(i_{2q}^{*} - i_{2q}) + K_{ii}^{'}\int (i_{2q}^{*} - i_{2q})dt \\ \eta &= -\begin{bmatrix} m_d & m_q \end{bmatrix}\cdot\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} = K_{vp}^{'}(v_{dc}^{*} - v_{dc}) + K_{vi}^{'}\int (v_{dc}^{*} - v_{dc})dt \end{aligned} \tag{3.41}$$

From (3.40), (3.41) and the definition in (3.42), the state space equations for the direct current control loop and DC voltage regulation loop can be derived as in (3.43).

$$\begin{cases} F_{i2d} = \int (i_{2d}^{*} - i_{2d})dt \\ F_{vdc} = \int (v_{dc}^{*} - v_{dc})dt \end{cases} \tag{3.42}$$

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} = \begin{bmatrix} -\dfrac{K_{ip}^{'} + r_2}{L_2} & \dfrac{K_{ii}^{'}}{L_2} \\ -1 & 0 \end{bmatrix}\cdot\begin{bmatrix} i_{2d} \\ F_{i2d} \end{bmatrix} + \begin{bmatrix} \dfrac{K_{ip}^{'}}{L_2} \\ 1 \end{bmatrix} i_{2d}^{*} \\ \dfrac{d}{dt}\begin{bmatrix} v_{dc} \\ F_{vdc} \end{bmatrix} = \begin{bmatrix} -\dfrac{K_{vp}^{'}R_d + 1}{R_d C_d} & \dfrac{K_{vi}^{'}}{C_d} \\ -1 & 0 \end{bmatrix}\cdot\begin{bmatrix} v_{dc} \\ F_{vdc} \end{bmatrix} + \begin{bmatrix} \dfrac{K_{vp}^{'}}{C_d} \\ 1 \end{bmatrix} v_{dc}^{*} \end{cases} \tag{3.43}$$

In (3.40), since the quadrant axis has the same structure as the direct axis, the transfer functions can be achieved as in (3.44).

$$\begin{cases} G_{i2}^{'} = \dfrac{i_{2d}}{i_{2d}^{*}} = \dfrac{i_{2q}}{i_{2q}^{*}} = \dfrac{K_{ii}^{'} + sK_{ip}^{'}}{K_{ii}^{'} + s(r_2 + K_{ip}^{'}) + s^2 L_2} \\ G_{vdc} = \dfrac{v_{dc}}{v_{dc}^{*}} = \dfrac{K_{vi}^{'} + sK_{vp}^{'}}{K_{vi}^{'} + s(1/R_d + K_{vp}^{'}) + s^2 C_d} \end{cases} \tag{3.44}$$

Since the *q*-axis reference is zero, the actual quadrature current is small. Based on this approximation, the direct current reference and the modulating signal into the PWM module are shown in (3.45), which is in accordance with Fig. 3-15(a).

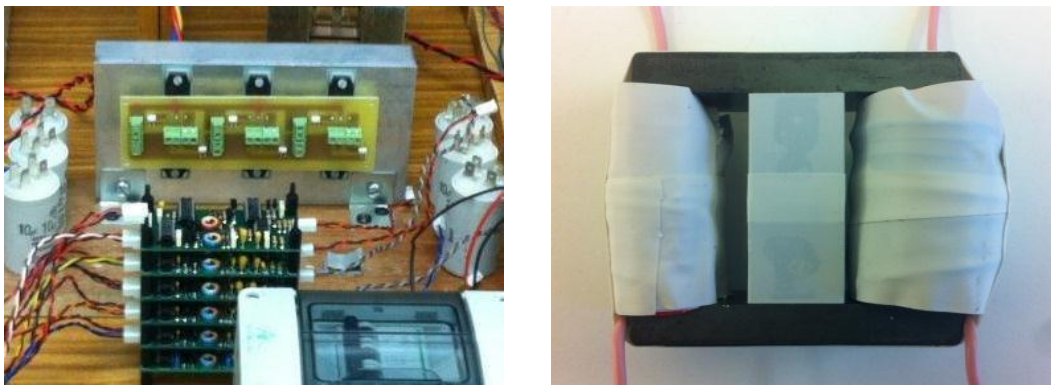
$$\begin{aligned} U_{2d}^{*} &= \gamma_d + v_{gd} - \omega L_2 i_{2q} \\ U_{2q}^{*} &= \gamma_q + v_{gq} + \omega L_2 i_{2d} \\ i_{2d}^{*} &= -\eta \end{aligned} \tag{3.45}$$

The outer layer with the active power controller, reactive power controller or DER DC voltage controller situations can be similarly solved by the proposed state space approach. The overall control scheme, including second order current elimination, is demonstrated in Fig. 3-15(b).

3.6 Experimental Verification

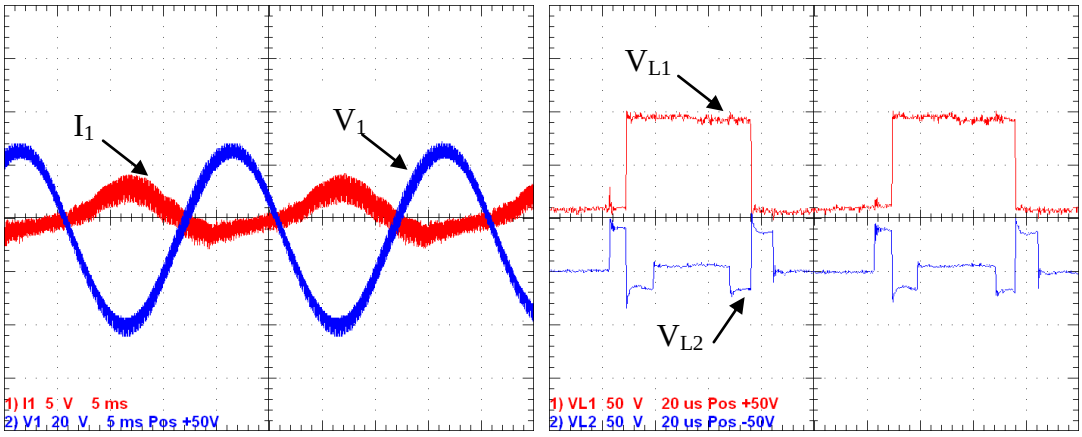
To substantiate the discussion and analysis in previous sections, a 2.5kVA three-phase ACVD converter based on Fig. 3-2(a) is experimentally accessed with the following specifications: 200V DC-link voltage; AC side phase voltage is 170V (peak value); 10kHz switching frequency (f_s); 470μF DC capacitance (C_d); 2mH IBBC inductance (L_1); 10μF IBBC capacitance (C_1); 5mH AC side inductance (L_2); and 10μF AC side capacitance C_2. The maximum AC output phase voltage is 200V. Compared with the 400V voltage stress for a conventional VSC, the IGBT voltage stresses in ACVD converter fluctuates around 400V with an AC component equal to the AC output voltage (this fluctuating voltage reduces the capacitor size). The AC side capacitor voltage and inductor current are equal to the output voltage and current respectively. In this demonstration, a Texas Instrument DSP TMS320F28335 is employed for digital implementation of the modulation and control systems.

Initially, the prototype is operated in an inverter mode to show its ability to cope with different power factors (unity, leading and lagging).



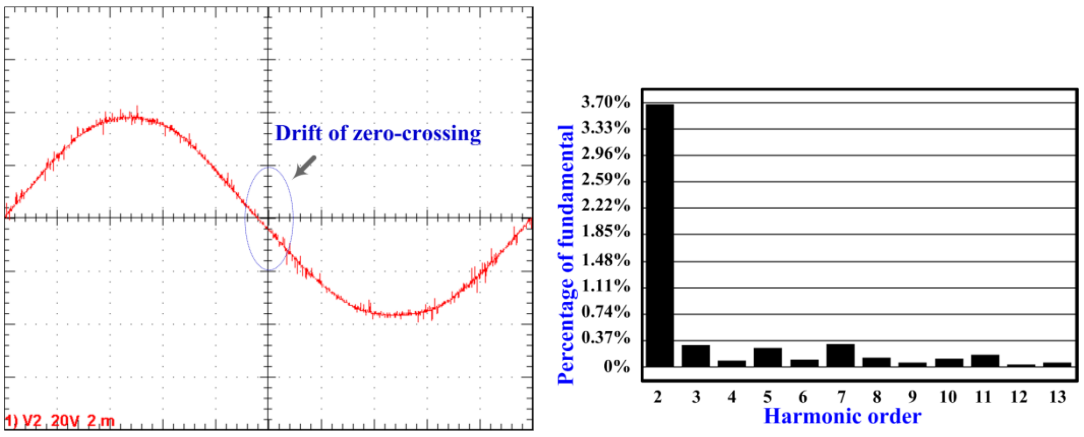
(a) (b)

Fig. 3-16. Photographs of (a) prototype for the power circuit of the proposed (three-phase) and its drivers and (b) integrated design of magnetic parts (L_1 and L_2).



(a) (b)

Fig. 3-17. Voltage and current waveforms of the state variables (5ms/div): (a) IBBC inductor current (5A/div) and IBBC capacitor voltage (20V/div) and (b) voltage across the two windings in the integrated magnetic component (50V/div).



(a) (b)

Fig. 3-18. Open loop output voltage with second order harmonic distortion: (a) output voltage waveform (20V/div, 2ms/div) and (b) distribution of the base band harmonics.

The footprint of the prototype is shown in Fig. 3-16(a). To demonstrate the effectiveness of the integrated design of L_1 and L_2 discussed in 3.3, such an inductor,

shown in Fig. 3-16(b), is tested when the inverter is operated as a single-phase standalone inverter from a 50V DC-link without second harmonic compensation. The IBBC voltage and current waveforms are displayed in Fig. 3-17(a), where the results in Fig. 3-17(b) show that the integrated design L_1 and L_2 can function independently in one core without noticeable interaction. (The fluxes do not interaction, having been shunted by the low reluctance center limb.) Therefore, the magnetic integration technique is an effective solution in confined space applications where a compact hardware design is required. The open loop output voltage and its spectrum in Fig. 3-18 exhibit a second order harmonic, which is in line with the presented analysis. In Fig. 3-18(a), the zero-crossing point drifts by 0.4ms and 3.7% second harmonic is observed in Fig. 3-18(b). This distortion is expected to be aggravated as the power increases, necessitating a second order harmonic mitigation mechanism within the converter controller.

To eliminate the second harmonic from the output voltage (thus, the output current), the control strategy depicted in Fig. 3-14(a) and (b) involving both fundamental regulation and harmonic elimination, is adopted for three-phase operation of the ACVD converter.

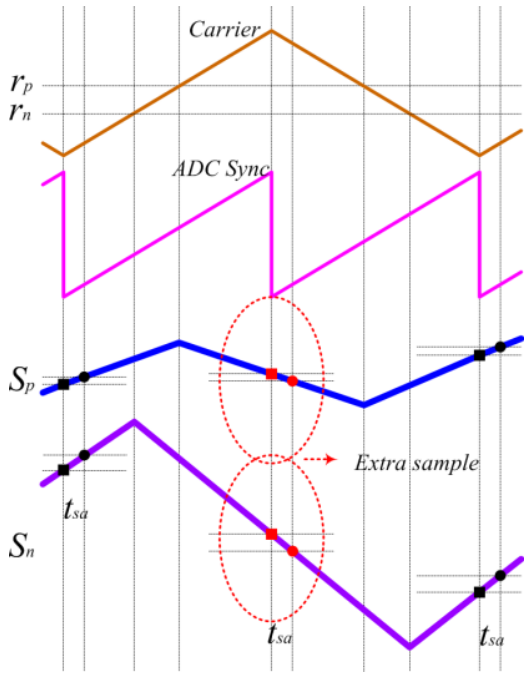
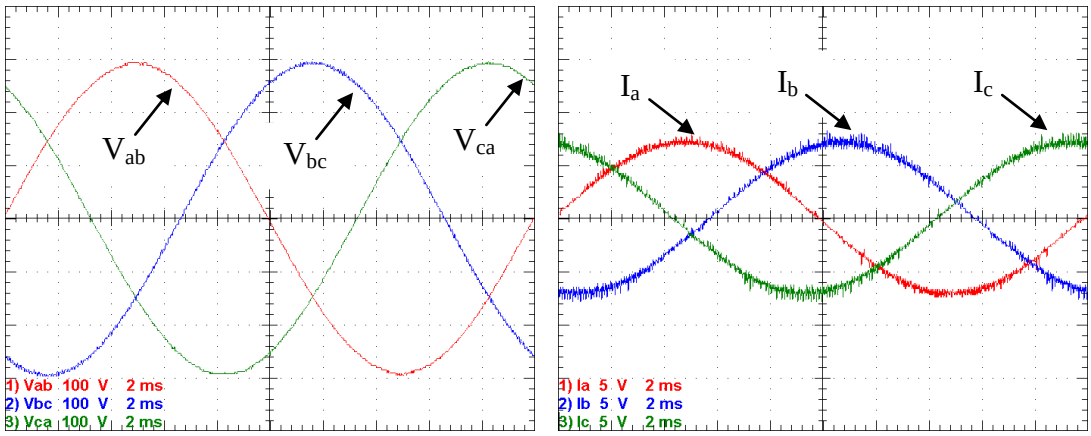


Fig. 3-19. ADC synchronization for asymmetric ripple compensation.

Fig. 3-19 shows the ADC synchronization scheme employed to compensate the asymmetric deviation from the average value during positive and negative half cycles.

r_p and r_n are the reference values 180 °apart, while S_p and S_n are the corresponding state variables. The ADC time t_{sa} causes some drift from the mid-point. Since the voltage/current slopes in the positive and negative half cycles are asymmetric for the ACVD converter, some DC bias will appear when the micro-controller samples one point (multi-times) per switching cycle. That is, the sampling process must strictly obey the Shannon principle, which demands the sampling speed be at least twice the switching frequency. So the ADC module is synchronized at double the frequency of the PWM generator. In this way, the extra samples can compensate the asymmetrical deviation from the actual value and eliminate the DC bias.



(a) (b)

Fig. 3-20. Output waveforms for standalone inverter mode (2ms/div): (a) line-to-line voltage (100V/div) and (b) line current with 22Ω resistive load (5A/div).

Fig. 3-20 shows the line-to-line voltage and three-phase currents during standalone operation of the proposed converter operating as an inverter. The THD for the voltage and current waveforms in Fig. 3-20, from FFT analysis up to 13 order harmonics, are both lower than 1% and meet IEEE and IEC harmonic standards. The peak line-to-line voltage of 295V is achieved from a 200V DC-link, which is beyond the DC utilization of 0.866pu for a conventional two-level VSC. This confirms the extended output voltage range of the proposed converter.

Fig. 3-21(a)-(c) demonstrate the operability of the proposed ACVD converter as an islanded inverter with resistive, capacitive and inductive loads. These plots establish that this converter is able to operate under such operating conditions, without any performance deterioration.

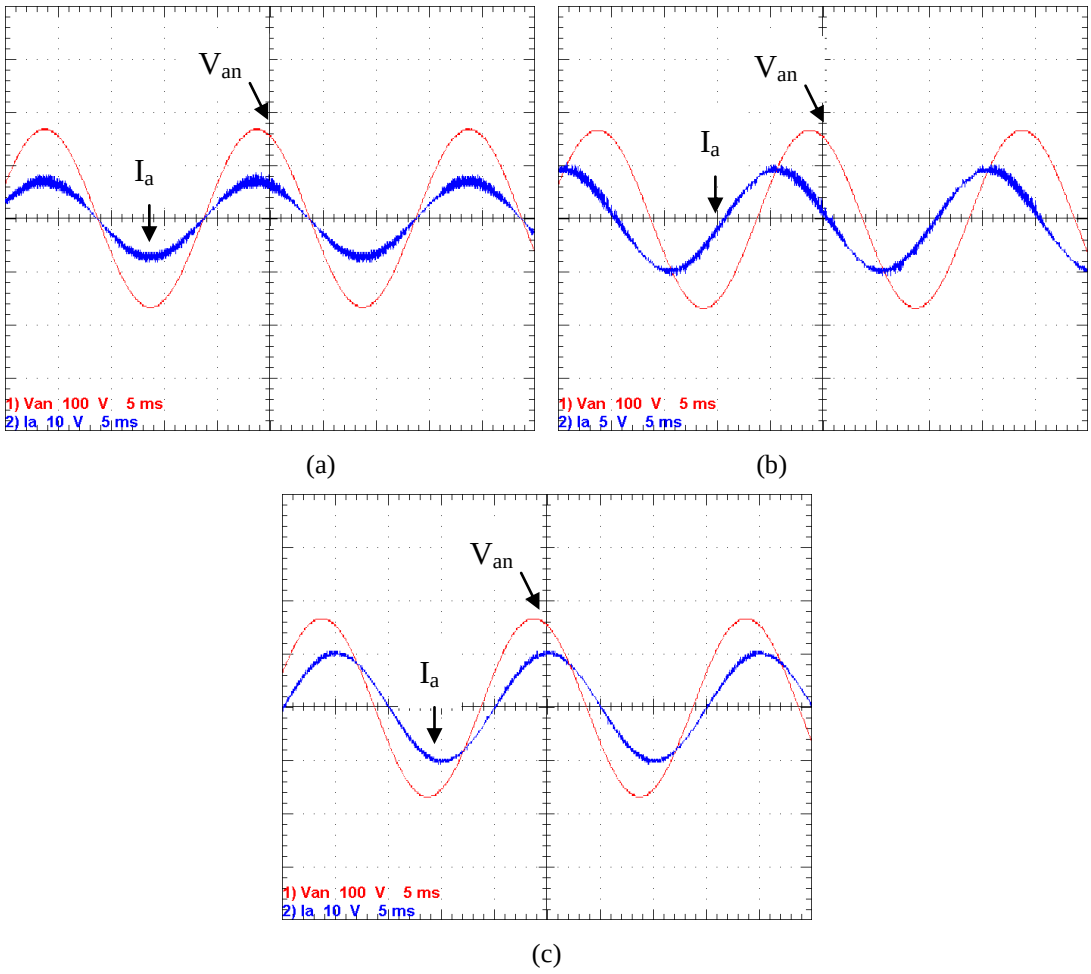
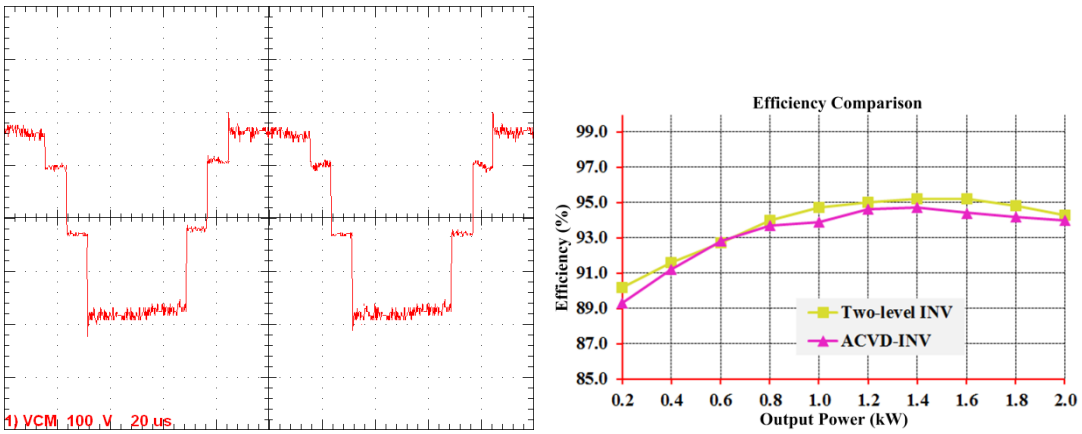


Fig. 3-21. Phase voltage/current waveforms of the ACVD-VSC under different load conditions (5ms/div): (a) phase voltage (100V/div) and phase current (10A/div) with 22Ω resistive load; (b) phase voltage (100V/div) and phase current (5A/div) with 22Ω +100μF capacitive load; and (c) phase voltage (100V/div) and phase current (10A/div) with 15Ω +30mH inductive load.

Fig. 3-22(a) show a snapshot of the load neutral point voltage relative to ground, which is fixed at the negative DC bus. The CM voltage has no DC component and has a switching bipolar nature around zero (real ground). This reduces the isolation requirement on the load connected to the AC side. The energy conversion efficiency as a standalone inverter with resistive load is compared with a two-level inverter with the same DC-link voltage, modulation index and power rating. In Fig. 3-22(b), the ACVD inverter overall efficiency is marginally lower than that of the two-level inverter. This is because the current stresses are nearly the same for the two converters in this application.



(a) (b)

Fig. 3-22. CM voltage and efficiency examination for proposed converter: (a) CM voltage between DC ground and AC neutral (100V/div, 20μs/div) and (b) efficiency performance for standalone inverter mode.

The feasibility of proposed converter for unity power factor rectifier application is also assessed using the prototype in Fig. 3-16(a). The AC input phase voltage is 150V (peak), and the DC output voltage is regulated at 200V with load resistance of 47Ω. The control system for rectifier operation shown in Fig. 3-15 is used. The DC output voltage, input phase current, and grid voltage waveforms are displayed in Fig. 3-23, where the input AC current is in phase with the grid voltage.

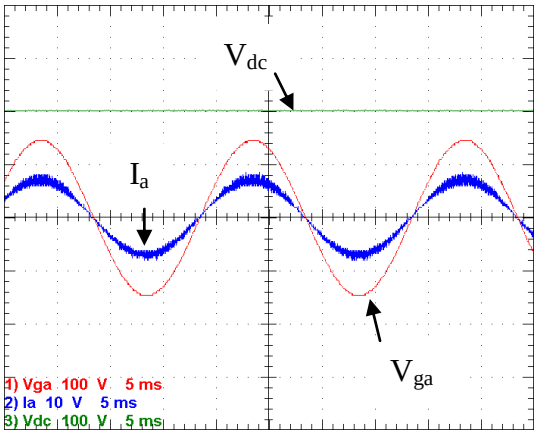


Fig. 3-23. Grid voltage (100V/div), phase current (5A/div) and DC output voltage (100V/div) for ACVD rectifier with 47Ω load (5ms/div).

Based on the inverter and rectifier operation results demonstrated in this section, the bidirectional operational capability of the proposed ACVD converter is confirmed.

It is concluded that the ACVD converter qualifies as a four-quadrant VSC with an extended AC voltage output range, high power density (twice the output voltage of the two-level converter with the same DC-link voltage), and high conversion efficiency. Additionally, the CM voltage has no DC component. Although higher

current stress is generated by the IBBC, the output power can be twice that of the two-level converter since the AC output voltage can be doubled. This means there is no appreciable degradation on efficiency performance with the ACVD-VSC.

3.7 Summary

In this chapter, a three-phase voltage source converter with doubled AC side voltage and suppressed DC common mode voltage was proposed. Due to the introduced IBBC, the DC-link utilization is extended to 1pu for the phase voltage (twice that of the two-level converter). Thus, the DC-link capacitor and interfacing transformer sizes are reduced. Due to the inherent ground of the negative terminal of DC-link, no CM voltage DC component is seen on the AC side neutral. Since the IBBC synthesizes the negative half of the output voltage, second order harmonics are introduced into the AC side voltage and current when operated in open loop. The *d-q* SRF models of the proposed converter in islanding or grid connected modes were presented, which are used to design the necessary control loops for fundamental power transfer and elimination of the second order harmonic distortion. This chapter also considered the voltage/current stresses on the semiconductor switches. Experimental results substantiated the claimed attributes of the ACVD-VSC, including its four-quadrant operational capability.

Reference

[1] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative Evaluation of Three-Phase AC-AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 4487-4510, 2012.

[2] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of Three-Phase PWM AC-AC Converter Topologies," *Industrial Electronics, IEEE Transactions on,* vol. 58, pp. 4988-5006, 2011.

[3] X. Changliang, Z. Faqiang, W. Zhiqiang, and H. Xiangning, "Equivalent Switch Circuit Model and Proportional Resonant Control for Triple Line-Voltage Cascaded Voltage-Source Converter," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2389-2401, 2013.

[4] S. Rodrigues, R. T. Pinto, P. Bauer, and J. Pierik, "Optimal Power Flow Control of VSC-Based Multiterminal DC Network for Offshore Wind Integration in the North Sea," *Emerging and Selected Topics in Power Electronics, IEEE Journal of,* vol. 1, pp. 260-268, 2013.

[5] Z. Changzheng, D. Shaowu, and C. Qiaofu, "A Novel Scheme Suitable for High-Voltage and Large-Capacity Photovoltaic Power Stations," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 3775-3783, 2013.

[6] J. Chivite-Zabalza, Rodri, x, M. A. guez Vidal, P. Izurza-Moreno, G. Calvo, *et al.*, "A Large Power, Low-Switching-Frequency Voltage Source Converter for FACTS Applications With Low Effects on the Transmission Line," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 4868-4879, 2012.
[7] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on,* vol. 28, pp. 335-346, 2013.
[8] J. Beerten, S. Cole, and R. Belmans, "Modeling of Multi-Terminal VSC HVDC Systems With Distributed DC Voltage Control," *Power Systems, IEEE Transactions on,* vol. 29, pp. 34-42, 2014.
[9] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, "Power Capability Investigation Based on Electrothermal Models of Press-Pack IGBT Three-Level NPC and ANPC VSCs for Multimegawatt Wind Turbines," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3195-3206, 2012.
[10] F. Wanmin, R. Xinbo, and W. Bin, "A Generalized Formulation of Quarter-Wave Symmetry SHE-PWM Problems for Multilevel Inverters," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 1758-1766, 2009.
[11] U. T. Shami and H. Akagi, "Identification and Discussion of the Origin of a Shaft End-to-End Voltage in an Inverter-Driven Motor," *Power Electronics, IEEE Transactions on,* vol. 25, pp. 1615-1625, 2010.
[12] U. T. Shami and H. Akagi, "Experimental Discussions on a Shaft End-to-End Voltage Appearing in an Inverter-Driven Motor," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 1532-1540, 2009.
[13] T. Maetani, S. Morimoto, K. Yamamoto, Y. Isomura, A. Watanabe, and K. Nakano, "Shaft voltage comparison between grounded and ungrounded brushless DC motors with insulated rotor driven by PWM inverter," in *Electrical Machines and Systems (ICEMS), 2012 15th International Conference on*, 2012, pp. 1-6.
[14] Y. Bo, L. Wuhua, G. Yunjie, C. Wenfeng, and H. Xiangning, "Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 752-762, 2012.
[15] G. Yunjie, L. Wuhua, Z. Yi, Y. Bo, L. Chushan, and H. Xiangning, "Transformerless Inverter With Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 793-805, 2013.
[16] J. W. Shin, H. Shin, G. S. Seo, J. I. Ha, and B. H. Cho, "Low-Common Mode Voltage H-Bridge Converter with Additional Switch Legs," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 1773-1782, 2013.
[17] H. Akagi and T. Doumoto, "An approach to eliminating high-frequency shaft voltage and ground leakage current from an inverter-driven motor," *Industry Applications, IEEE Transactions on,* vol. 40, pp. 1162-1169, 2004.
[18] Dura, x, M. J. n, J. Prieto, and F. Barrero, "Space Vector PWM With Reduced Common-Mode Voltage for Five-Phase Induction Motor Drives Operating in Overmodulation Zone," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 4030-4040, 2013.
[19] C. C. Hou, C. C. Shih, P. T. Cheng, and A. M. Hava, "Common-Mode Voltage Reduction Pulsewidth Modulation Techniques for Three-Phase Grid-Connected Converters," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 1971-1979, 2013.

[20] Y. Otani, T. Isobe, and R. Shimada, "Control and design principle of a soft-switching boost dc to ac converter without smoothing capacitor using a MERS pulse link concept," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2102-2108.
[21] W. Weimin, H. Yuanbin, and F. Blaabjerg, "An LLCL Power Filter for Single-Phase Grid-Tied Inverter," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 782-789, 2012.
[22] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 57-68, 2012.
[23] J. D. Van Wyk, F. C. Lee, L. Zhenxian, R. Chen, W. Shuo, and L. Bing, "Integrating active, passive and EMI-filter functions in power electronics systems:a case study of some technologies," *Power Electronics, IEEE Transactions on,* vol. 20, pp. 523-536, 2005.
[24] Z. Yi, L. Wuhua, D. Yan, and H. Xiangning, "Analysis, Design, and Experimentation of an Isolated ZVT Boost Converter With Coupled Inductors," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 541-550, 2011.
[25] L. Wuhua, L. Peng, Y. Huan, and H. Xiangning, "Three-Level Forward-Flyback Phase-Shift ZVS Converter With Integrated Series-Connected Coupled Inductors," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 2846-2856, 2012.
[26] Q. Shafiee, J. M. Guerrero, and J. C. Vasquez, "Distributed Secondary Control for Islanded Microgrids - A Novel Approach," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1018-1031, 2014.
[27] Y. A. R. I. Mohamed, H. H. Zeineldin, M. M. A. Salama, and R. Seethapathy, "Seamless Formation and Robust Control of Distributed Generation Microgrids via Direct Voltage Control and Optimized Dynamic Power Sharing," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 1283-1294, 2012.

CHAPTER 4

ACVD-VSC Based High Power Density FACTS Devices with Extended Control Range

This chapter proposes a new family of flexible AC transmission system (FACTS) devices based on the AC side voltage doubled voltage source converter (ACVD-VSC) in Chapter 3, which has twice the DC-link utilization of a two-level VSC, hence improved power density per unit DC-link voltage. This means its DC voltage limit for reactive power generation is higher than that for the conventional static synchronous compensator (STATCOM) and static synchronous series compensator (SSSC). Therefore, extended control ranges result for all members in the proposed family of FACTS devices. Also the ACVD converter has zero DC common mode voltage between the AC side neutral point and the DC-link negative terminal, reducing the insulation level for the interfacing transformer when the negative DC bus is grounded. The basic ACVD-VSC operation principles are reviewed. Then, it is used in FACTS devices to perform voltage or power flow control as shunt or series compensators. The STATCOM and SSSC using the ACVD-VSC are analyzed and tested under different control modes including transients. Simulation results are presented to verify the feasibility of the proposed schemes.

4.1 Background

The rising interest in developing smart grids encourages the decentralization of traditional power systems; thus, making the grid structure more flexible, reliable but increasingly complex. Consequently, the networking of distributed generation and regional power transmission require fast and reliable power flow controllers to achieve flexible power management targets [1-8].

The voltage source converter (VSC) based flexible AC transmission system (FACTS) uses self-commutated devices to realize various functions such as voltage magnitude regulation, reactive power compensation, and power flow control [9, 10].

The static synchronous compensator (STATCOM) and the static synchronous series compensator (SSSC) are two FACTS devices used to achieve these targets by shunt and series compensation respectively. Based on these devices, a group of multi-bus FACTS devices such as the unified power flow controller (UPFC), interline power flow controller (IPFC), and generalized unified power flow controller (GUPFC) can be created by sharing a common DC-link capacitor [11, 12]. This chapter mainly focuses on the STATCOM and SSSC.

Basically the STATCOM reactive power absorption limit is defined by the current limit of the power devices, while its reactive power generation limit is constraint by the available DC link voltage to synthesize the maximum ac side voltage behind the phase interfacing reactor or transformer. The low DC voltage utilization of all half-bridge (two series devices across a DC link) based topologies, such as the two-level VSC, constrains their ability to generate the necessary AC voltage necessary to inject sufficient reactive power to the grid without raising the DC-link voltage. Consequently, the STATCOM reactive power rating tends to be asymmetrical [13].

An SSSC injects a series voltage that is seen as a variable reactor by the power line to regulate the active power flow in a given branch. Its control range is determined by the maximum AC voltage inserted in series with the transmission line [14].

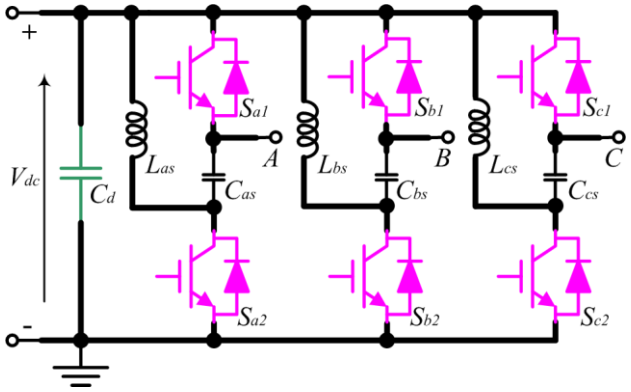
Consequently, the control range of conventional VSC based FACTS devices is largely constraint by the DC link utilization. The use of space vector modulation (SVM) improves the DC utilization by about 15%, offering a limited extension of the power control range [15]. This limit is imposed by the hardware constraint that the instantaneous value of AC side voltage cannot extend beyond half the DC-link voltage. In Chapter 3, the AC side voltage doubled (ACVD) converter topology is

presented to circumvent this hardware constraint and has twice the DC utilization of a two-level converter.

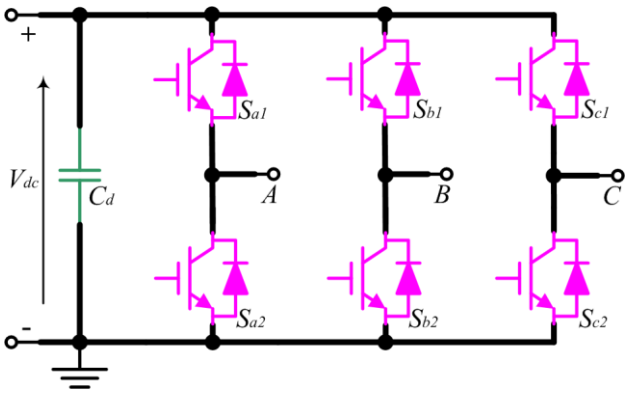
This chapter assesses the suitability of the ACVD-VSC in two representative FACTS devices, namely, the STATCOM and SSSC. By analyzing their performance, it will be shown that the ACVD-VSC based STATCOM is able to synthesize higher AC voltage from a given DC-link voltage, surpassing the DC voltage limit and approaches the current limit for reactive power generation, in contrast to the conventional two-level VSC counterpart. Thus, the STATCOM with a symmetrically extended reactive power control range can be achieved with the ACVD-VSC. The ACVD-SSSC offers a larger control range than its equivalent two-level-SSSC due to its ability to insert higher series voltage into the tie line for a given DC voltage. Also, in all ACVD solutions, the negative DC bus can be grounded without introducing any DC voltage stress to the transformer neutral (the internal *LC* cell acts as a temporary source to generate negative voltage relative to the negative DC bus).

4.2 ACVD-VSC with Doubled DC Utilization and AC Side Common Mode Voltage Suppression

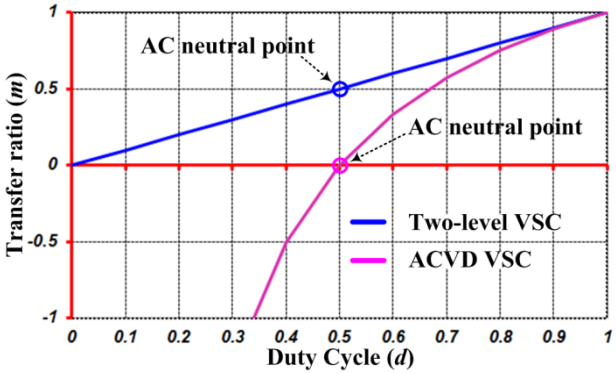
The schematic of the ACVD-VSC is shown in Fig. 4-1(a), and its operational principle will be discussed. The detailed ACVD-VSC converter level analysis can be found in Chapter 3.



(a)



(b)



(c)

Fig. 4-1. Comparison between the ACVD-VSC and the conventional two-level VSC: (a) ACVD-VSC topology; (b) two-level VSC; and (c) voltage transfer ratio versus duty cycle.

Compared with the conventional two-level VSC in Fig. 4-1(b), an *LC* cell is inserted into each phase of the ACVD converter to achieve an advanced voltage transfer characteristic. Taking phase '*a*' for example, ACVD-VSC operation can be described in two modes as follows [16]:

Mode 1: when S_{a1} is on and S_{a2} is off, output voltage is generated at pole '*A*' relative to ground. This mode creates a zero voltage loop that comprises inductor L_{as} and capacitor C_{as} for charging the capacitor with reversed polarity relative to V_{dc}.

Mode 2: when S_{a2} is on and S_{a1} is off, C_{as} is employed as a virtual voltage source to generate the negative voltage at the output. This mode creates another loop to energise the inner inductor L_{as}; and this stored energy can be subsequently transferred to the capacitor, as per mode 1.

Assuming *d* is the duty cycle of an upper switch in both VSCs (two-level and ACVD VSCs with upper and lower switches in each phase operating complementarily), V_m is the peak value of the AC side phase voltage and V_{dc} is the DC-link voltage, the voltage transfer ratio *m* can be defined by (4.1). For the two-level VSC, *m*=*d*; while

m=2-1/d for the ACVD-VSC. The relations between m and d for the two VSCs are displayed in Fig. 4-1(c). The ACVD-VSC has an output voltage range $\pm V_{dc}$, and the average voltage at the AC side neutral point of the ACVD-VSC is equal to the real ground (zero) of the DC-link; while the two-level converter output voltage ranges from 0 to V_{dc}, and AC neutral point voltage is $\frac{1}{2}V_{dc}$. Consequently, in the two-level VSC, the DC-link is usually split into two with the mid-point grounded to suppress the DC common mode voltage.

$$m = V_m / V_{dc} \tag{4.1}$$

In summary, the proposed ACVD-VSC has double the output voltage range of the conventional two-level VSC, and its AC side neutral point has zero DC common mode voltage relative to the negative terminal of the DC-link, which, practically, can decrease the insulation level of any associated transformer compared with the two-level VSC when the negative DC bus is grounded.

As a four-quadrant operational converter, when the ACVD-VSC acts as a FACTS device, several advantages are expected:

- STATCOM: Due to the improved power density of the ACVD-VSC, the shunt current (voltage, reactive power) control range is extended for the same DC-link voltage as the conventional solution.
- SSSC: The series voltage control range for a given DC-link voltage is increased for the proposed converter. Conversely, for the same control range, the required DC-link voltage is virtually halved.
- UPFC: If taking a UPFC as comprising a STATCOM and a SSSC, both the previous attributes are inherited.

Analysis of the ACVD-VSC in FACTS applications is addressed in following sections.

4.3 Performance Analysis and Control Design for FACTS Applications

This section presents discussion of two ACVD-VSC based FACTS devices, specifically the STATCOM and the SSSC.

4.3.1 STATCOM Performance and Control Design

Fig. 4-2 shows the system diagram of the ACVD-VSC configured as a STATCOM, where B_0 is the slack sending bus, and B_1 is the PQ (load) bus. The STATCOM being

studied is connected to the point of common coupling (PCC) through its phase interfacing reactor X_{sh} and a shunt interfacing transformer T_{sh} with a turns ratio N.

If the PCC voltage v_g is used as the input to a phase-locked-loop (PLL) and aligned with the d-axis, no active power is exchanged between the grid and the STATCOM DC side capacitor, except for negligible internal losses. Neglecting the transformer and phase interfacing resistance and assume the transformer leakage reactance are combined with the phase interfacing reactors X_{sh}, the converter voltage $v_{cd,q}$, shunt current i_{dq}, and injected power $P_{sh}+jQ_{sh}$ are (4.2) and (4.3).

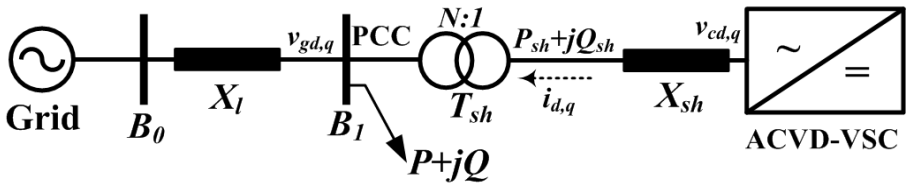


Fig. 4-2. The ACVD-VSC configured as a STATCOM.

$$v_{gq} = 0,\ v_{cq} = 0,\ i_d = 0,\ P_{sh} = 0 \tag{4.2}$$

$$i_q = \frac{v_{cd} - v_{gd} / N}{X_{sh}},\ Q_{sh} = \frac{v_{gd}(v_{cd} - v_{gd} / N)}{N X_{sh}} \tag{4.3}$$

The STATCOM generates capacitive reactive power to the grid when v_{cd} is larger than v_{gd}/N. Assuming a fixed DC side voltage V_{dc} and m is the modulation index, the output voltage of the ACVD-VSC is mV_{dc} compared to $½mV_{dc}$ for a two-level VSC in SPWM mode. Therefore, for grid connection, a shunt transformer with turns-ratio of $2N$ is needed for a two-level converter.

If an active source or energy storage device is connected to the DC-link capacitor, the STATCOM is able to exchange active power with the grid, and the bidirectional d-axis current and active power flow in the shunt branch is determined by (4.4). Practically, the power control range of an active sourced STATCOM is constrained by the current limit of the power switches (the under excitation region) and the maximum synthesized voltage on the converter side for reactive power generation (the over excitation region).

$$i_d = \frac{v_{cq}}{X_{sh}},\ P_{sh} = \frac{v_{gd}\ v_{cq}}{N X_{sh}} \tag{4.4}$$

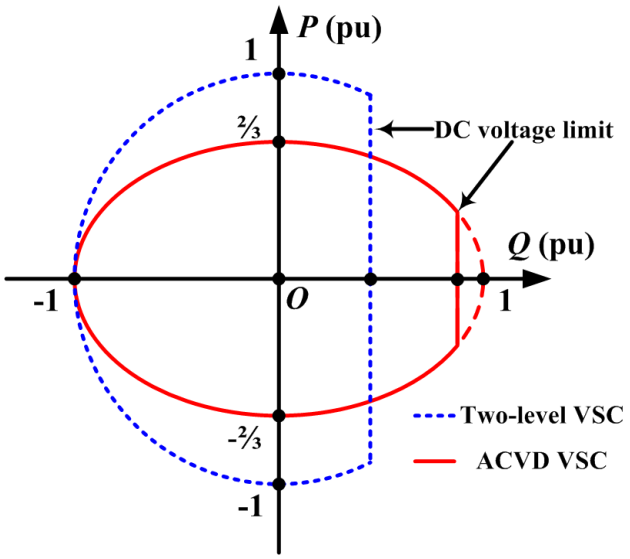


Fig. 4-3. Power control range comparison between ACVD-VSC and two-level VSC STATCOMs.

To compare the power control range of the two versions of STATCOM (ACVD-VSC and two-level VSC based), the same DC-link voltage and the same current rated power switches (IGBT or IGCT) are assumed. Since the AC side maximum voltage is doubled with the ACVD-VSC, considering the power switch capacity, the rated output current should be reduced in the ACVD-VSC; and according to Chapter 3, its maximum output current is ⅓ to ½ of that in the two-level VSC, depending on the power factor (½ for zero power factor and ⅓ for unity power factor). As stated, due to the doubled AC side voltage range, the shunt transformer T_{sh} has half the turns-ratio of the conventional two-level VSC solution. From (4.3) and (4.4), the maximum shunt current of ACVD-VSC based STATCOM injected to the grid is ⅔ to 1. Therefore, the control range of the two STATCOM versions is clarified by Fig. 4-3, where the arc of the circle and ellipse are the power switch current limit of the two-level and ACVD solutions respectively. However, in the right half plane where STATCOM capacitive reactive power is generated, the voltage amplitude is the main limitation for the conventional two-level VSC, because its AC side voltage is constraint to $½V_{dc}$, such that at maximum reactive power generation the current limit is not reached. But for the ACVD scheme, the converter terminal ac voltage is doubled. From (4.3), the reactive power generation range of the ACVD STATCOM is significantly extended and has a higher possibility to reach the pre-defined power device current limit ellipse that leads to a symmetrical control range.

The STATCOM is mainly employed as a reactive power control device (without an active DC side source). From Fig. 4-3, the increased horizontal length for the ACVD

solution shows its extension of the reactive power control range. This advantage is because the ACVD converter uses higher voltage and lower current (compared to two-level VSC) to transfer a given power.

Fig. 4-3 is drawn for the same DC-link voltage and the same current rated power devices. Another perspective is, since the proposed converter has an improved power density, at most four times power can be generated from the same DC-link voltage to the same load condition, compared with two-level VSC, provided higher capacity power devices are used.

The control diagram of the proposed STATCOM scheme is summarized in Fig. 4-4, where the PCC voltage v_{gabc} is the PLL input to produce the reference angle θ and i_{abc} is the shunt current. In the *dq* frame, the outer layer DC voltage controller and reactive power (PCC voltage amplitude) controller are used to generate the direct and quadrature current references respectively. The inner layer current controllers generate the *dq* commands of the converter output voltage. Also, in this layer, a proportional-resonant (PR) controller is used to eliminate the 2nd order component generated by each *LC* cell.

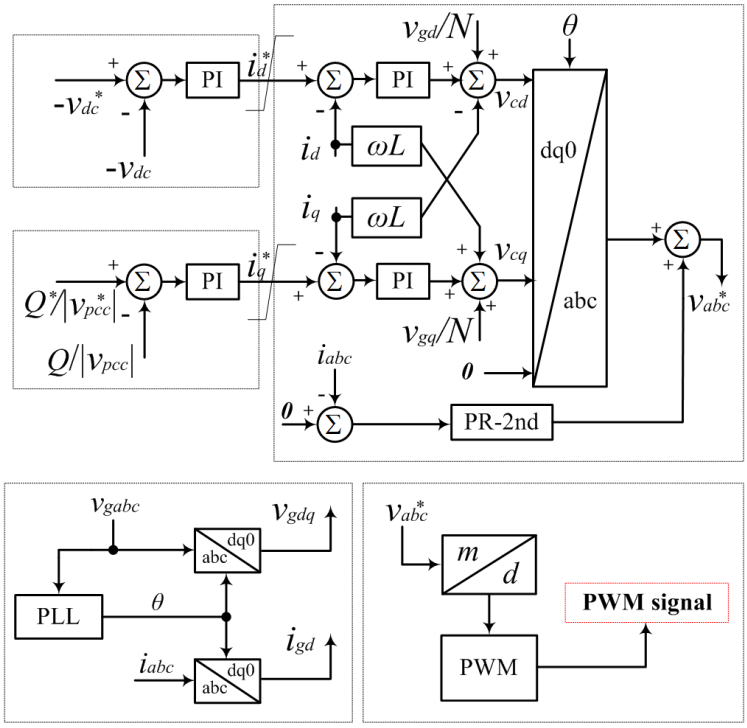


Fig. 4-4. ACVD-VSC based STATCOM control diagram.

a) Inner Layer Fundamental Current Controller

The ACVD-VSC voltage transfer ratio is defined as m=2-1/d, and d is the duty cycle of the upper switches. Then, the differential equations describing the ac side performance are show in (4.5) and (4.6), where k_{ip} and k_{ii} are the current controller proportional and integral (PI) parameters.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{L}\begin{bmatrix} \gamma_d \\ \gamma_q \end{bmatrix} - \frac{r}{L}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{4.5}$$

$$\begin{cases} \gamma_d = v_{dc}m_d - v_{gd} + \omega L i_q = k_{ip}(i_d^* - i_d) + k_{ii}\int (i_d^* - i_d)dt \\ \gamma_q = v_{dc}m_q - v_{gq} - \omega L i_d = k_{ip}(i_q^* - i_q) + k_{ii}\int (i_q^* - i_q)dt \end{cases} \tag{4.6}$$

To facilitate control design in state space, the PI controller integral terms are defined in (4.7). Substituting (4.6) and (4.7) into (4.5), the same full state space equations for direct and quadrature axes are achieved, in (4.8). With Laplace manipulation, the *dq* current loop transfer functions are also identical and are clarified by (4.9), which is employed to tune the control parameters. From Fig. 4-4 and (4.6), the voltage command v_{cdq}* for the ACVD-VSC can be obtained from the PI output and feed-forward terms, expressed in (4.10).

$$\begin{cases} F_{id} = \int (i_d^* - i_d)dt \\ F_{iq} = \int (i_q^* - i_q)dt \end{cases} \tag{4.7}$$

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_d \\ F_{id} \end{bmatrix} = \begin{bmatrix} -\dfrac{k_{ip}+r}{L} & \dfrac{k_{ii}}{L} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_d \\ F_{id} \end{bmatrix} + \begin{bmatrix} \dfrac{k_{ip}}{L} \\ 1 \end{bmatrix} i_d^* \\ \dfrac{d}{dt}\begin{bmatrix} i_q \\ F_{iq} \end{bmatrix} = \begin{bmatrix} -\dfrac{k_{ip}+r}{L} & \dfrac{k_{ii}}{L} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_q \\ F_{iq} \end{bmatrix} + \begin{bmatrix} \dfrac{k_{ip}}{L} \\ 1 \end{bmatrix} i_q^* \end{cases} \tag{4.8}$$

$$G_i = \frac{i_d}{i_d^*} = \frac{i_q}{i_q^*} = \frac{k_{ii} + sk_{ip}}{k_{ii} + s(r + k_{ip}) + s^2 L} \tag{4.9}$$

$$\begin{cases} v_{cd}^* = \gamma_d + v_{gd} - \omega L i_q \\ v_{cq}^* = \gamma_q + v_{gq} + \omega L i_d \end{cases} \tag{4.10}$$

b) Inner Layer 2nd Order Current Eliminating Controller

In Chapter 3, it was shown that the ACVD converter inner cell introduces 2nd order harmonic distortion into the AC side, which can be eliminated by adding a parallel

decoupling control loop with the same structure as the fundamental loop but counter-rotating at twice the fundamental angular frequency.

In this chapter, a PR controller is employed in the inner layer to suppress the 2nd order harmonic current. Compared with the method in Chapter 3, a PR controller can simplify the overall control design and enhance the dynamic performance since it does not require large bandwidth, phase and gain margins, as with the proportional-integral method, to ensure stability [17, 18] .

The modified PR controller in (4.11) is adopted, where k_{2p} is the proportional coefficient, k_{2r} is the resonant gain, ω_2 is the angular frequency of the 2nd order harmonic (the quantity to be controlled), and ω_B is the band-pass window width used to avoid potential system instability caused by frequency quantization drifting and round-off error.

$$T_r = k_{2p} + \frac{k_{2r}\omega_B s}{\omega_2^{\,2} + 2\omega_B s + s^2} \tag{4.11}$$

c) Outer Layer DC Voltage Maintaining Controller

Assume P_a is the internal losses that may cause a DC voltage drop. Since the converter voltage has a small phase shift relative to the PCC voltage, $v_{cq}\approx 0$ and $m_q\approx 0$ (the modulation index quadrature component). Thus the state space equations describing the dc side are as in (4.12). The active power (internal losses) P_a through an isolated STATCOM is small; therefore v_{dc} and m_d can be considered constant. From the third equation of (4.12), η can be generated by the outer layer DC voltage controller as in (4.13) where the integral term is denoted as F_{dc}. Then, the state space equations of the DC voltage closed loop is expressed in (4.14), and by Laplace manipulation, the DC voltage transfer function is (4.15). (4.16) produces the direct current reference.

$$\begin{cases} \dfrac{dv_{dc}}{dt} = -\dfrac{P_a}{v_{dc}C_d} = \dfrac{1}{C_d}\eta \\ P_a = v_{cd}i_d + v_{cq}i_q \approx v_{cd}i_d \\ \eta = -\begin{bmatrix} m_d & m_q \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \approx -m_d i_d \end{cases} \tag{4.12}$$

$$\begin{cases} \eta = k_{dcp}(v_{dc}^* - v_{dc}) + k_{dci}\int (v_{dc}^* - v_{dc})dt \\ F_{dc} = \int (v_{dc}^* - v_{dc})dt \end{cases} \tag{4.13}$$

$$\frac{d}{dt}\begin{bmatrix} v_{dc} \\ F_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{k_{dcp}}{C_d} & \frac{k_{dci}}{C_d} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{dc} \\ F_{dc} \end{bmatrix} + \begin{bmatrix} \frac{k_{dcp}}{C_d} \\ 1 \end{bmatrix} v_{dc}^* \tag{4.14}$$

$$G_{vdc} = \frac{v_{dc}}{v_{dc}^*} = \frac{k_{dci} + sk_{dcp}}{k_{dci} + sk_{dcp} + s^2 C_d} \tag{4.15}$$

$$i_d^* = -[k_{dcp}(v_{dc}^* - v_{dc}) + k_{dci}\int (v_{dc}^* - v_{dc})dt] \tag{4.16}$$

d) Outer Layer AC Voltage/Reactive Power Controller

From (4.3) and Fig. 4-4, the quadrature current reference is set by the outer layer PCC voltage amplitude controller or the reactive power controller as shown in (4.17). The gains for these controllers are determined using a trial-and-error searching method to realize the optimal time domain performance for the overall system.

$$\begin{aligned} & i_q^* = k_{acp}(|v_{pcc}^*| - |v_{pcc}|) + k_{aci}\int (|v_{pcc}^*| - |v_{pcc}|)dt \\ or \quad & i_q^* = k_{Qp}(Q^* - Q) + k_{Qi}\int (Q^* - Q)dt \end{aligned} \tag{4.17}$$

4.3.2 SSSC Performance and Control Design

Fig. 4-5 shows the ACVD-VSC configured as a SSSC, where the reference bus B_0 exchanges power flow of $P+jQ$ where B_1, X_{l1} and X_{l2} are the line impedances, and T_{se} is the series transformer with a turns-ratio N:1.

The grid current i_l is the PLL reference, and no active power is exchanged between the SSSC and the grid if internal losses are neglected. Also, the line impedances are assumed to be purely inductive. Therefore, the injected voltage v_{se} is perpendicular to the line current. $v_{0d,q}$ and $v_{1d,q}$ are the bus voltages and the SSSC voltage $v_{sed,q}$ equals $1/N$ the converter output voltage $v_{cd,q}$. Then (4.18) and (4.19) are obtained.

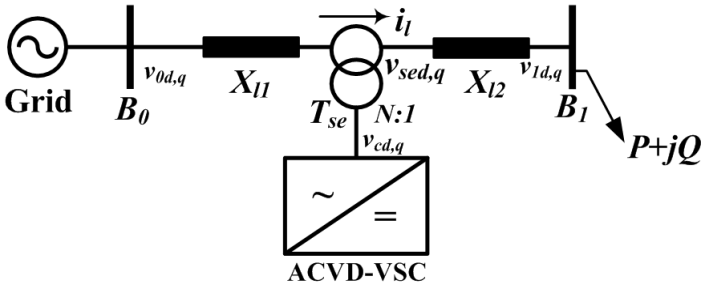


Fig. 4-5. Diagram of the ACVD-VSC configured as an SSSC.

$$\boldsymbol{v_{sed}} = 0, \boldsymbol{i_{lq}} = 0, \boldsymbol{v_{0d}} = \boldsymbol{v_{1d}} = \boldsymbol{v_{gd}} \tag{4.18}$$

$$i_{ld}=\frac{v_{0q}-v_{1q}-v_{seq}}{X_{l1}+X_{l2}},\quad P=\frac{v_{gd}\left(v_{0q}-v_{1q}-v_{seq}\right)}{X_{l1}+X_{l2}} \tag{4.19}$$

Equation (4.19) indicates that v_{seq} is the only control variable that can be manipulated to regulate the power flow in the line being considered. Thus, the active power control range is determined by the variation range of v_{seq}. Different to a shunt connection, there is no voltage adaption requirement for series compensation; so the fixed DC-link voltage and the same series transformer are assumed to compare the power flow control range of the ACVD and two-level SSSC versions.

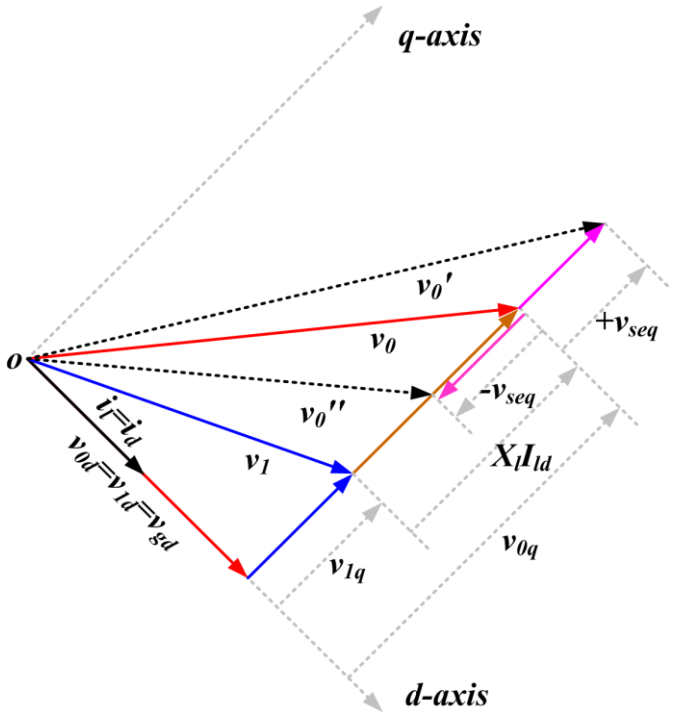


Fig. 4-6. Phasor diagram of an SSSC based on the ACVD-VSC.

The SSSC phasor diagram is shown by Fig. 4-6, where X_l is the total line reactance at the power frequency and I_l is the line current before compensation. The net voltage vector across the line is v_0-v_1 before SSSC injection; and by the series voltage $\pm v_{seq}$, the excitation voltage is controllable to either v_0' or v_0'', which means the net voltage vector in the q-axis can be increased or decreased to regulate active power flow.

If the DC-link voltage is V_{dc}, the voltage control range in Fig. 4-6 is doubled by using an ACVD-VSC, compared to a conventional two-level converter. From (4.19), the incremental active power flow is given by (4.20), and is linearly dependent on the series injected voltage amplitude. This means the power flow control range is doubled by using the proposed SSSC scheme. Thus reactive power exchange

between the VSC and the grid is also doubled according to (4.21), at the expense of using twice current rated power switches.

$$\Delta P = -\frac{v_{gd} \cdot v_{seq}}{Z_l} \tag{4.20}$$

$$Q_{sssc} = i_{ld} \cdot v_{seq} \tag{4.21}$$

Fig. 4-7 is the control scheme of ACVD-SSSC, where the line current i_{labc} is the PLL input to get the reference angle θ and $v_{se.abc}$ represents the injected voltage. In the *dq* frame, an outer layer DC voltage controller and power flow controller are used to generate the direct and quadrature series voltage references respectively. The inner layer controllers set the *dq* commands of the converter output voltage. Also, in this layer, the PR controller in (4.11) eliminates the 2nd order component caused by the *LC* cells.

Since the grid line current i_l is the PLL reference, and SSSC active power exchange with the grid (internal losses) is small, i_{lq}=0 and v_{dc} is assumed constant. Then, the state space equations for dc side performance is given by (4.22). ρ can be obtained by the outer layer DC voltage controller as described in (4.23), denoting the integral term as W_{dc} to facilitate the state space derivation. Similar to (4.14) and (4.15), the DC voltage transfer function for the SSSC mode is as in (4.24), and the injected direct and quadrature voltage references are given by (4.25) and (4.26) respectively.

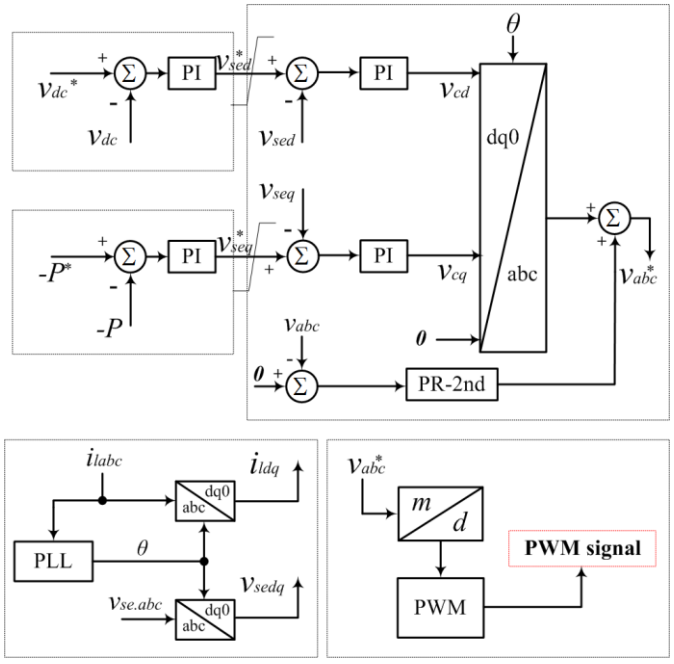


Fig. 4-7. ACVD-VSC based SSSC control diagram.

$$\begin{cases} \dfrac{dv_{dc}}{dt} = \dfrac{P_a}{v_{dc}C_d} = \dfrac{1}{C_d}\rho \\ P_a = v_{sed}i_{ld} + v_{seq}i_{lq} = v_{sed}i_{ld} \\ \rho = \dfrac{i_{ld}}{v_{dc}} \quad v_{sed} \end{cases} \tag{4.22}$$

$$\begin{cases} \rho = m_{dcp}(v_{dc}^{*} - v_{dc}) + m_{dci}\int (v_{dc}^{*} - v_{dc})dt \\ W_{dc} = \int (v_{dc}^{*} - v_{dc})dt \end{cases} \tag{4.23}$$

$$T'_{vdc} = \frac{v_{dc}}{v_{dc}^{*}} = \frac{m_{dci} + sm_{dcp}}{m_{dci} + sm_{dcp} + s^2 C_d} \tag{4.24}$$

$$v_{sed}^{*} = m_{dcp}(v_{dc}^{*} - v_{dc}) + m_{dci}\int (v_{dc}^{*} - v_{dc})dt \tag{4.25}$$

$$v_{seq}^{*} = -[m_{Pp}(P^{*} - P) + m_{Pi}\int (P^{*} - P)dt] \tag{4.26}$$

In summary, the improved power density of the ACVD-VSC allows more power from a given DC-link, compared with a two-level VSC. Generally, ACVD based STATCOM, SSSC and UPFC can all double (pure reactive power) or quadruple (both active and reactive power) the control range, with higher capacity power switches. For the case of the ACVD-STATCOM, from Fig. 4-3, even when the same current rated power devices are used as a conventional converter (reactive power absorption ability is also the same), its capacitive reactive power generation ability is significantly improved due to better DC voltage utilization.

4.4 Performance Assessment and Extended Control Range Verification

Simulation results for the ACVD-VSC based STATCOM and SSSC can verify the effectiveness of the proposed ACVD-VSC and its control strategies in FACTS applications.

Table 4-1. ACVD converter specification for simulation

ACVD-VSC	
Apparent power rating S_{con}	40MVA
DC link voltage V_{dc}	40kV
DC link capacitor C_d	2200μF
Shunt or filtering inductor L_{sh}/L_f	12mH
Filtering capacitor C_f	80μF
Internal cell capacitor C_s	8μF
Internal cell inductor L_s	8mH
Converter switching frequency	2.5kHz

Table 4-2. Converter transformer parameters

Shunt transformer	
Power capacity	40MVA
Voltage ratio	110kV/34.64kV
Per unit impedance	(0.0005+j0.08)
Series transformer	
Power capacity	40MVA
Voltage ratio	20kV/3.9kV
Per unit impedance	(0.0002+j0.05)

Table 4-3. AC transmission system parameters

Grid parameters for shunt/series compensation	
Power rating	367MVA
Nominal line voltage	110kV(RMS)
Line impedance	(0.466+j9.322)

The ACVD-VSC specification is listed in Table 4-1, while the parameters for the shunt/series interfacing transformer and the AC power grid are shown in Table 4-2 and Table 4-3 respectively.

4.4.1 STATCOM Simulation Results

This section presents simulation waveforms when the ACVD-STATCOM injects variable reactive power into the grid, when:

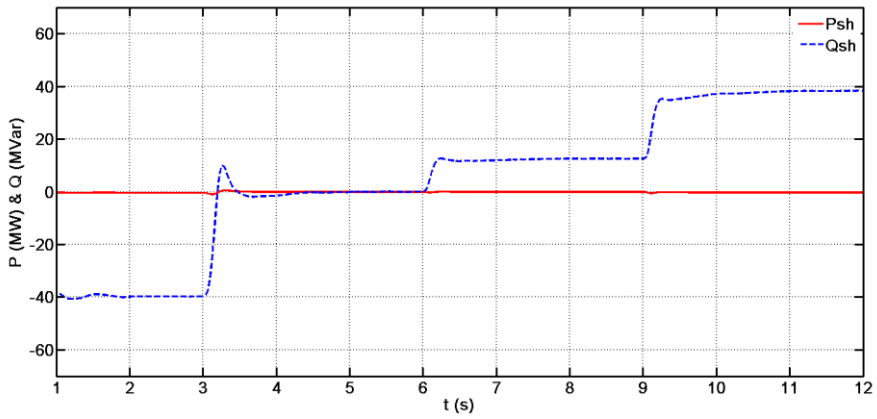
- t: 0~3s, Q_{sh}^{*} = -40MVAr, STATCOM absorbs Q;
- t: 3~6s, Q_{sh}^{*} = 0, no Q exchange in the shunt branch;
- t: 6~9s, Q_{sh}^{*} = 12MVAr, STATCOM generates Q;
- t: 9~12s, Q_{sh}^{*} = 36MVAr, STATCOM generates Q.

The simulation results when the STATCOM reactive power command varies according to these conditions are displayed in Fig. 4-8. Fig. 4-8(a) shows that the STATCOM reactive power output tracks the reference and almost zero active power is exchanged with the grid. The voltage amplitude at the PCC varies with STATCOM reactive power injection into the grid, and correspondingly, also the shunt current; see Fig. 4-8(b) and (c). Fig. 4-8(d) and (e) present the expanded waveforms of the PCC voltage and shunt current. DC-link voltage and internal cell capacitor voltage waveforms are shown in Fig. 4-8(f) and (g).

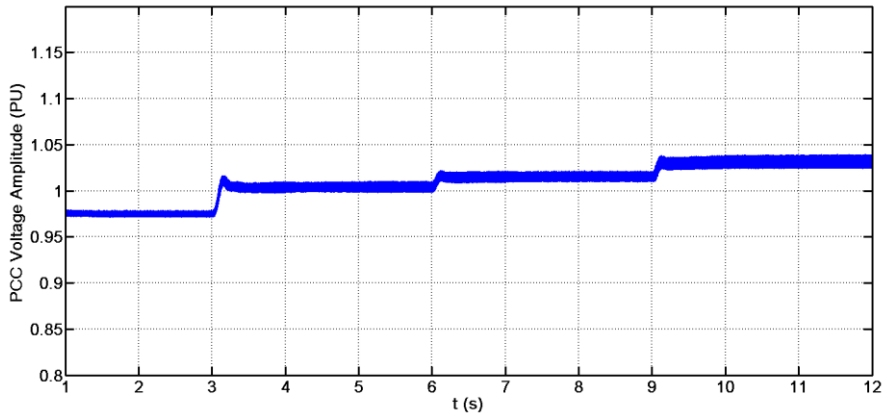
In this simulation, zero reactive power exchange between the STATCOM and the grid is achieved at 0.7 modulation index (modulation index is defined based on the full dc link voltage). Also, the STATCOM maximum reactive current limit is set to ±1kA (equivalent to ±315A referred to the grid side), which is implemented as

saturation at the output of the reactive power controller that defines the reference shunt current within the control block.

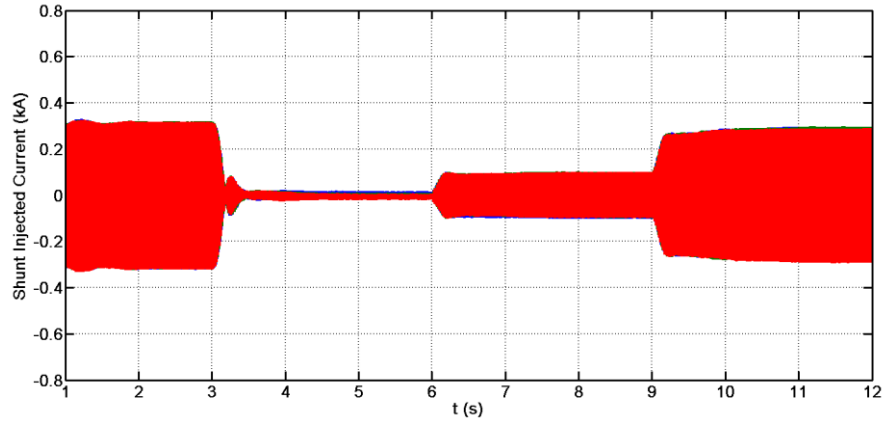
To verify the extended reactive power control range of the proposed STATCOM shown in Fig. 4-3, the results in Fig. 4-8(a) and (c) are re-examined. The preset control range of -40MVAr to 36MVAr is reached before modulation index saturation. As a comparison, in the conventional two-level VSC case, the zero power injection point should be equivalently kept at a modulation index of 0.7. Since modulation index is defined based on ½ dc-link voltage for two-level VSC, as in Fig. 4-1(c), its converter side ac voltage becomes half that of the ACVD converter. This means the shunt transformer voltage ratio of the two-level STATCOM has to be double the value specified in Table 4-2 to adapt the grid voltage. Fig. 4-9 summarizes the reactive power control range for the two-level STATCOM superimposed on that of the ACVD-STATCOM. The two-level solution exhausts its full modulation linear range (reaching its reactive power generation limit) before the ACVD-VSC based STATCOM, and the injected shunt reactive power range of the proposed ACVD-STATCOM is much wider and nearly symmetrical compared to the two-level case, see Fig. 4-9(a) and (b). These results are achieved with the equivalent parameters for the two VSCs, so that the zero power injection points of both STATCOMs occur at 70% of their linear modulation range. The ACVD converter has a wider voltage variation range around its zero power point than the two-level converter due to its doubled DC link utilization. Therefore, the extended reactive power envelope of the ACVD-STATCOM in the over-excitation region where it generates capacitive reactive power to the grid, is verified as indicated in Fig. 4-3.



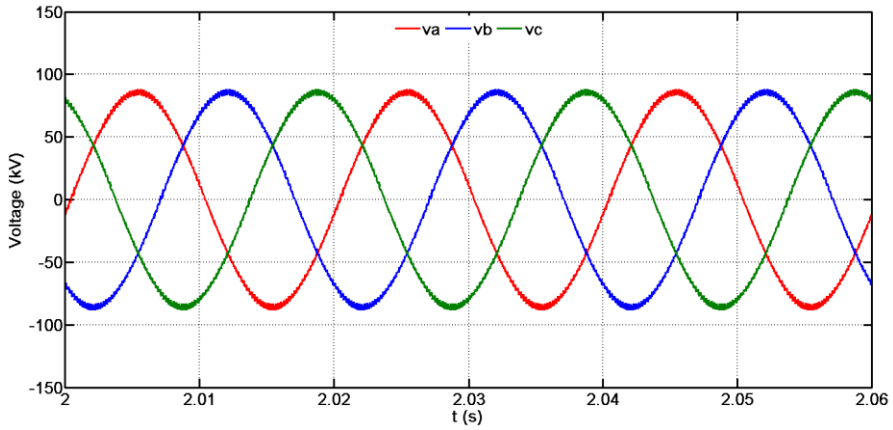
(a)


PCC Voltage Amplitude (PU)
1.15
1.1
1.05
1
0.95
0.9
0.85
0.8
1
2
3
4
5
6
7
8
9
10
11
12
t (s)

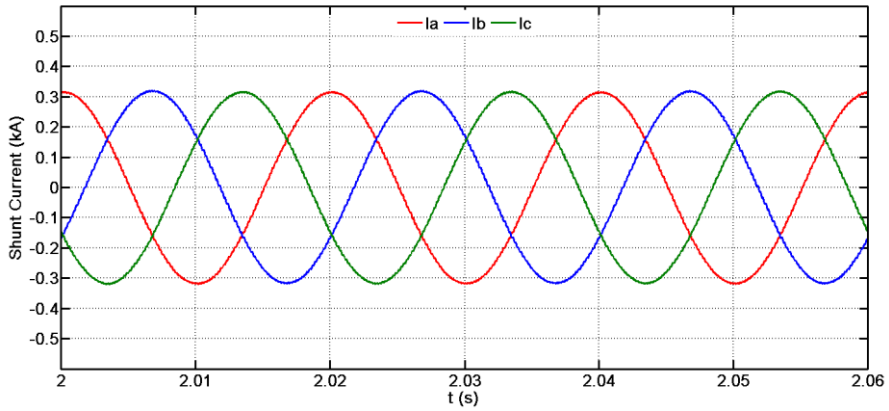
(b)


Shunt Injected Current (kA)
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
1
2
3
4
5
6
7
8
9
10
11
12
t (s)

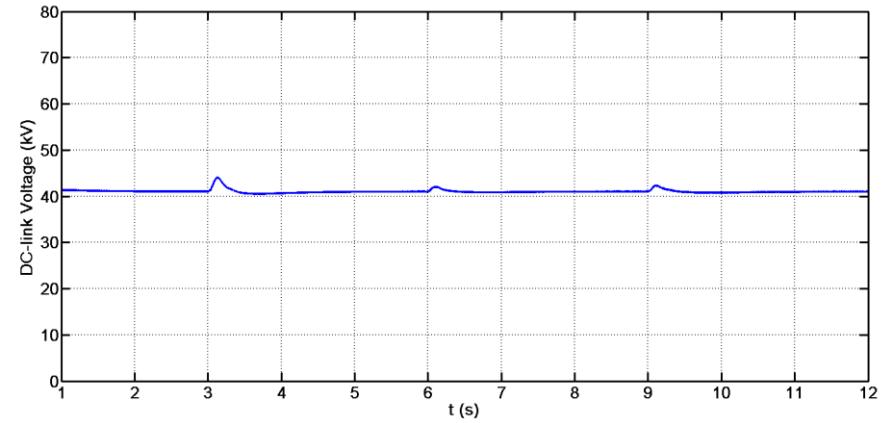
(c)


va
vb
vc
Voltage (kV)
150
100
50
0
-50
-100
-150
2
2.01
2.02
2.03
2.04
2.05
2.06
t (s)

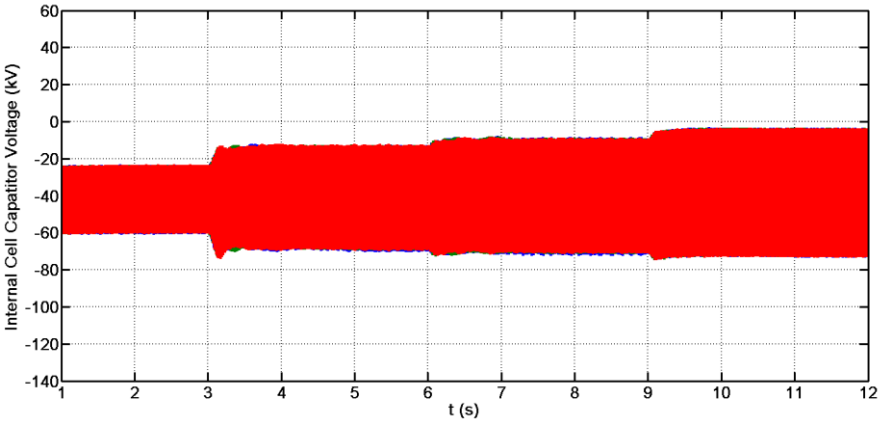
(d)



(e)

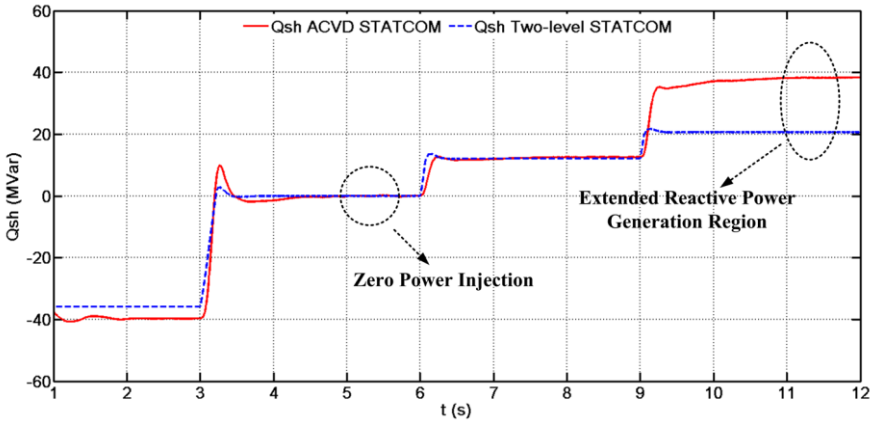


(f)

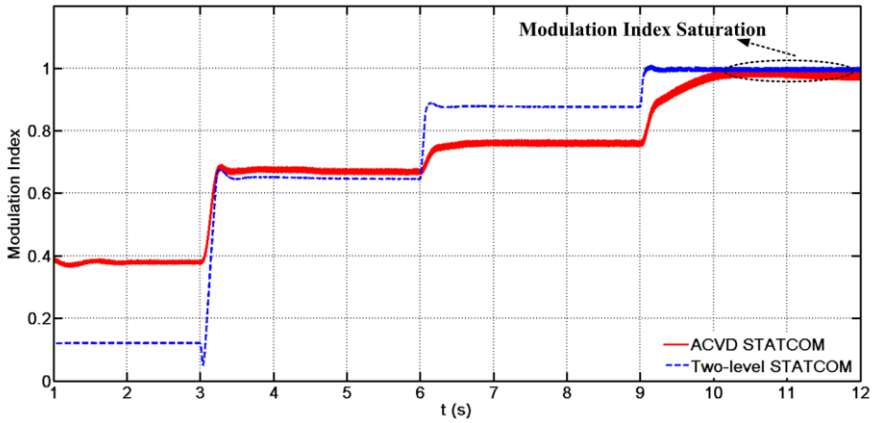


(g)

Fig. 4-8. ACVD-STATCOM simulations: (a) power exchange between the STATCOM and the grid; (b) PCC voltage amplitude; (c) shunt current step changes; (d) expanded PCC voltage; (e) expanded shunt current; (f) DC-link voltage; and (g) internal cell capacitor voltage.



(a)



(b)

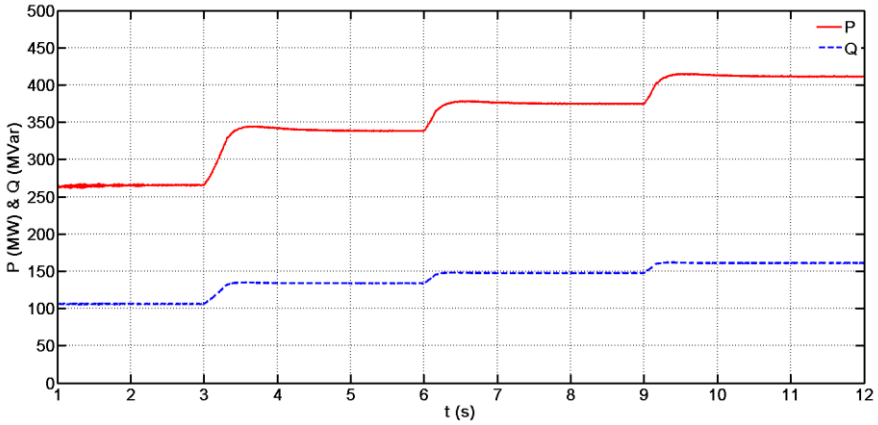
Fig. 4-9. Verification of the control range extension of the ACVD-STATCOM: (a) reactive power generation comparison and (b) modulation index.

4.4.2 SSSC Simulation Results

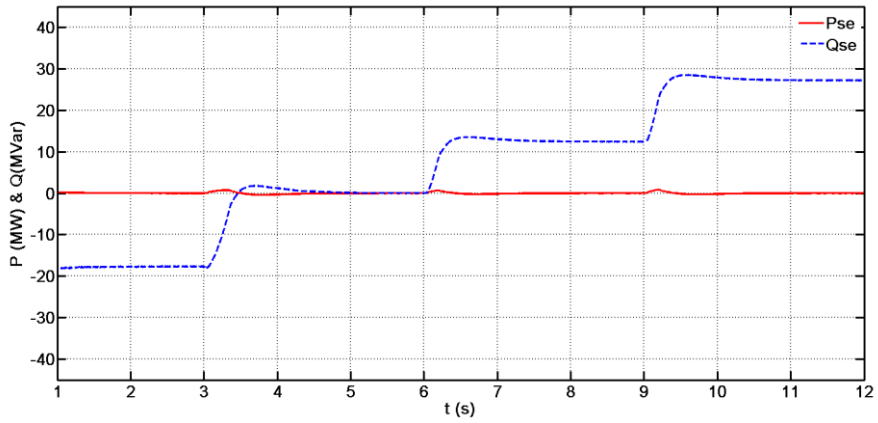
Fig. 4-10 presents simulation results when the ACVD-SSSC varies the per phase power flow command as follows.

- t: 0~3s, P^* = 265MW, SSSC decreases net voltage;
- t: 3s~6s, P^* = 340MW, SSSC gives zero voltage;
- t: 6s~9s, P^* = 375MW, SSSC increases net voltage;
- t: 9s~12s, P^* = 415MW, SSSC increases net voltage.

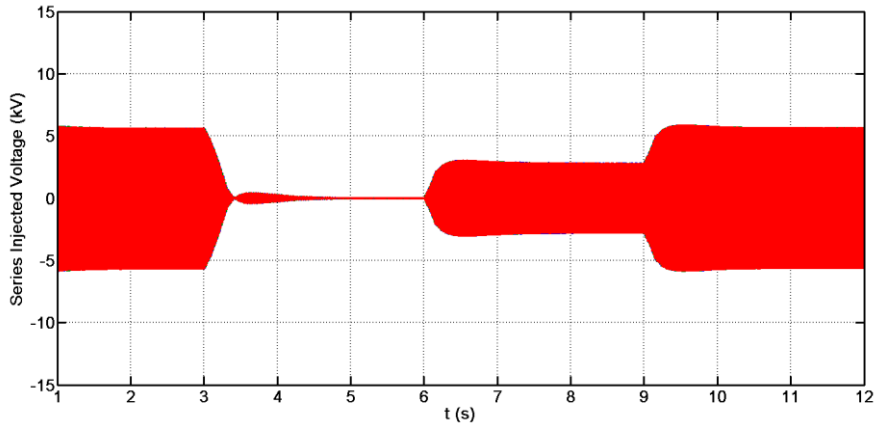
In Fig. 4-10(a) and (b), the grid active power flow control and the reactive power exchange between the SSSC and the grid are displayed, respectively. The transient processes of the series injected voltage are given in Fig. 4-10(c). From Fig. 4-10(d), the injected voltage is perpendicular to the line current as discussed; with nearly zero active power exchange with the grid (the small active power drawn from the grid is to maintain the SSSC dc link voltage and feed losses).


P
Q
P (MW) & Q (MVar)
t (s)

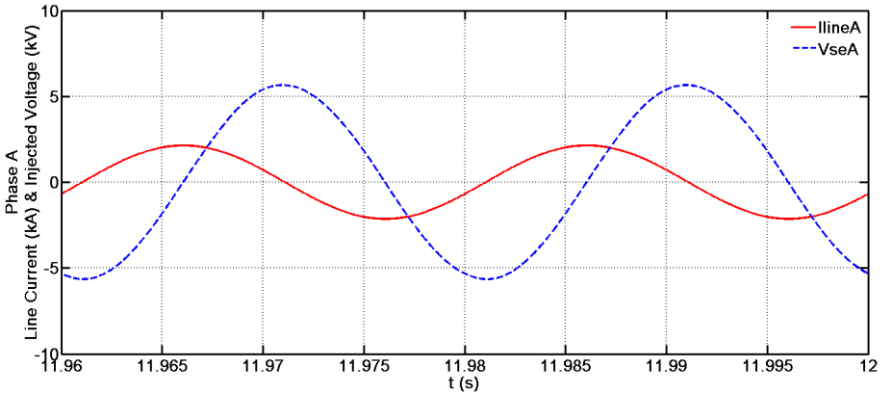
(a)


Pse
Qse
P (MW) & Q(MVar)
t (s)

(b)


Series Injected Voltage (kV)
t (s)

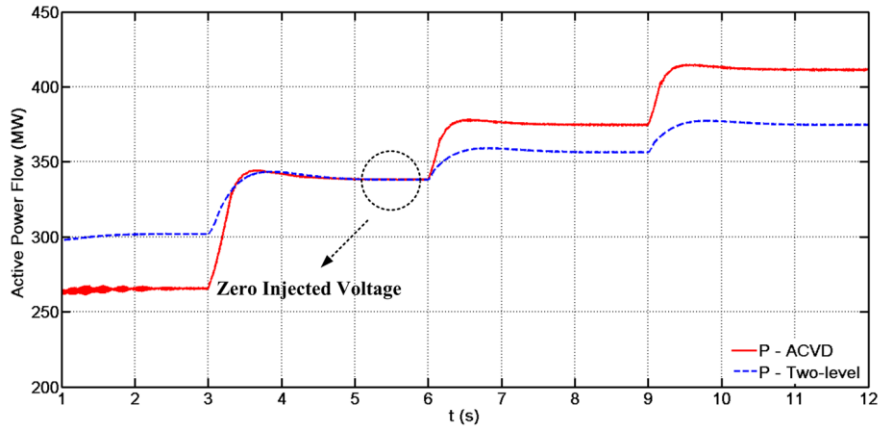
(c)



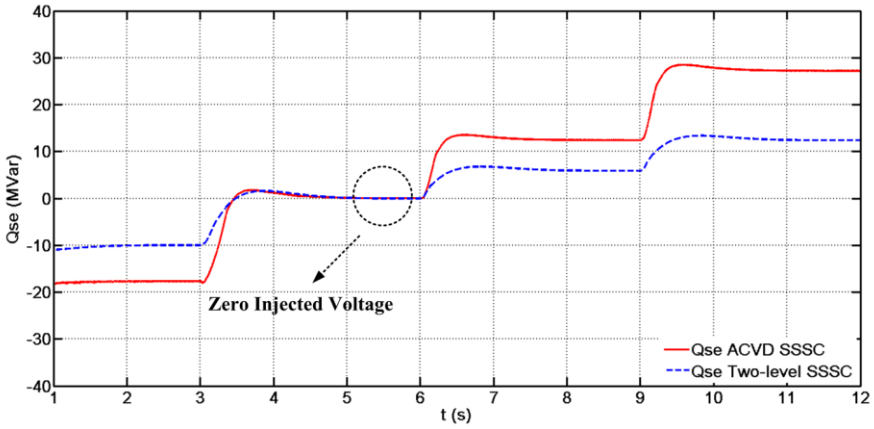
(d)

Fig. 4-10. ACVD-SSSC simulation: (a) power flow changes in the grid; (b) power exchanges between the SSSC and the grid; (c) series injected voltage step changes; and (d) expanded line current and injected voltage.

The interfacing transformer is the same for the comparison between two-level and ACVD converter SSSCs. In order to make a valid comparison, the modulation ranges for the two converters are both set to ±70% of their full range. Fig. 4-11 summarizes the comparison results of active power flow control range and reactive power exchange for the two cases. Within the same linear modulation range, the ACVD-SSSC is able to realize an extended power flow control range compared to convention solution, as described in 4.3.



(a)



(b)

Fig. 4-11. Verification of the control range extension of the ACVD-SSSC: (a) active power flow control range comparison and (b) reactive power exchange.

4.5 Summary

This chapter presented new FACTS device topologies that use an AC side voltage doubled (ACVD) converter with higher power density than existing topologies. It has been shown that the proposed FACT devices are able to operate as shunt and series compensators, typically as STATCOM and SSSC, and offer the following advantages:

- STATCOM DC voltage limit for reactive power generation is increased, extending (nearly symmetrically) the reactive power compensation range without recourse to increasing the dc link voltage, as needed with half-bridge solutions.
- The control range, when the SSSC injects voltage to regulate the power flow, is increased, benefiting from the doubled DC utilization in the ACVD converter.
- The power density is significantly improved with the ACVD converter, which means more power from a given DC link voltage.
- ACVD FACTS devices do not expose their interfacing transformers to DC stress even if the negative terminal of DC link is grounded.

Based on the discussions in this chapter, it can be deduced that the back to back configuration of ACVD-VSCs can act as a UPFC, with all the ACVD advantages inherent.

Reference

[1] E. Ghahremani and I. Kamwa, "Analysing the effects of different types of FACTS devices on the steady-state performance of the Hydro-Quebec network," *Generation, Transmission & Distribution, IET,* vol. 8, pp. 233-249, 2014.

[2] J. Verveckken, F. Silva, D. Barros, and J. Driesen, "Direct Power Control of Series Converter of Unified Power-Flow Controller With Three-Level Neutral Point Clamped Converter," *Power Delivery, IEEE Transactions on,* vol. 27, pp. 1772-1782, 2012.

[3] D. M. Divan, W. E. Brumsickle, R. S. Schneider, B. Kranz, R. W. Gascoigne, D. T. Bradshaw, *et al.*, "A Distributed Static Series Compensator System for Realizing Active Power Flow Control on Existing Power Lines," *Power Delivery, IEEE Transactions on,* vol. 22, pp. 642-649, 2007.

[4] N. M. R. Santos, J. F. Silva, J. Verveckken, V. M. F. Pires, and R. M. G. Castro, "Enhancing the Ride-Through Capability of DC-Link Voltage in NPC Multilevel Unified Power-Flow Controllers," *Power Delivery, IEEE Transactions on,* vol. 29, pp. 1542-1550, Aug 2014.

[5] M. Aredes and R. Dias, "FACTS for Tapping and Power Flow Control in Half-Wavelength Transmission Lines," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 3669-3679, 2012.

[6] L. Bin and B. T. Ooi, "Nonlinear control of FACTS and HVDC belonging to the voltage-source converter family," in *Control Applications, 2005. CCA 2005. Proceedings of 2005 IEEE Conference on*, 2005, pp. 617-623.

[7] T. Aziz, M. J. Hossain, T. K. Saha, and N. Mithulananthan, "VAR Planning With Tuning of STATCOM in a DG Integrated Industrial System," *Power Delivery, IEEE Transactions on,* vol. 28, pp. 875-885, 2013.

[8] A. Cetin and M. Ermis, "VSC-Based D-STATCOM With Selective Harmonic Elimination," *Industry Applications, IEEE Transactions on,* vol. 45, pp. 1000-1015, 2009.

[9] J. Segundo-Ramirez and A. Medina, "Modeling of FACTS Devices Based on SPWM VSCs," *Power Delivery, IEEE Transactions on,* vol. 24, pp. 1815-1823, Oct 2009.

[10] Y. H. Liu, N. R. Watson, K. L. Zhou, and B. F. Yang, "Converter System Nonlinear Modeling and Control for Transmission Applications - Part I: VSC System," *Power Delivery, IEEE Transactions on,* vol. 28, pp. 1381-1390, Jul 2013.

[11] M. Noroozian, L. Angquist, M. Ghandhari, and G. Andersson, "Use of UPFC for optimal power flow control," *Power Delivery, IEEE Transactions on,* vol. 12, pp. 1629-1634, 1997.

[12] J. Pourhossein, G. B. Gharehpetian, and S. H. Fathi, "Unified Interphase Power Controller (UIPC) Modeling and Its Comparison With IPC and UPFC," *Power Delivery, IEEE Transactions on,* vol. 27, pp. 1956-1963, 2012.

[13] A. de la Villa Jaen, E. Acha, and A. G. Exposito, "Voltage Source Converter Modeling for Power System State Estimation: STATCOM and VSC-HVDC," *Power Systems, IEEE Transactions on,* vol. 23, pp. 1552-1559, 2008.

[14] F. A. R. Jowder and B. T. Ooi, "VSC-HVDC station with SSSC characteristics," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 1053-1059, 2004.

[15] D. Ahmadi, Z. Ke, L. Cong, H. Yi, and W. Jin, "A Universal Selective Harmonic Elimination Method for High-Power Inverters," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 2743-2752, 2011.

[16] P. Li, G. P. Adam, Y. Hu, D. Holliday, and B. W. Williams, "Three-Phase AC-Side Voltage-Doubling High Power Density Voltage Source Converter With Intrinsic Buck-Boost Cell and Common-Mode Voltage Suppression," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 5284-5298, 2015.

[17] X. Changliang, W. Zhiqiang, S. Tingna, and H. Xiangning, "An Improved Control Strategy of Triple Line-Voltage Cascaded Voltage Source Converter Based on Proportional-Resonant Controller," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 2894-2908, 2013.

[18] A. Hasanzadeh, O. C. Onar, H. Mokhtari, and A. Khaligh, "A Proportional-Resonant Controller-Based Wireless Control Strategy With a Reduced Number of Sensors for Parallel-Operated UPSs," *Power Delivery, IEEE Transactions on*, vol. 25, pp. 468-478, 2010.

CHAPTER 5

Literature Review for Multilevel Converter Topologies

To reduce the voltage stress on power switching devices, limit the EMI caused by high *dv*/*dt*, and minimize the harmonic distortion of the two-level VSC, the multilevel converter is introduced. This chapter reviews the evolution of multilevel converter topologies by investigation of conventional clamping technique based solutions, cascaded full-bridge converter, and the modular multilevel converter (MMC). The unique features of these state-of-art candidates are discussed and compared.

5.1 Background

Multilevel converters are widely accepted for their attractive features such as lower device voltage stress, reduced *dv/dt*, and low output voltage THD. One of the important groups of multilevel topologies is based on the clamping technique, such as the diode clamped multilevel converter (DCMC) and the flying capacitor multilevel converter [1].

The three-level DCMC, also called the neutral point clamped (NPC) converter, was proposed by Nabae *et al*. in 1980 [2] and later extended to general multilevel cases in 1983 [3]. Then, the flying capacitor multilevel converter was introduced [4]. Derived from these two original prototypes, many new topologies developed, such as the active neutral point clamped (ANPC) converter, hybrid clamped multilevel converter (HCMC), and multilevel clamped multilevel converter (MLC2) [5-7].

However, these topologies suffer from a rapid increase in complexity of power circuit (device installation) and modulation when the voltage level number is high. Also the power switching device losses of these topologies are not evenly distributed between the switches in each arm, which challenges losses analysis and thermal design. Alternatively, motivated by pursuing modularity, the cascaded full-bridge converter was put forward, which offers straightforwardness and simplicity for the topology derivation and control design under high voltage level conditions. However, it requires separate DC source such as photovoltaic (PV) panels or batteries for each module, which is not desirable when a common DC-link is necessary or multiple DC sources are unavailable [8, 9].

Using a common DC-link, the modular multilevel converter (MMC) with half-bridge (HB) cells was proposed and has several advantages including reduced power switch losses, modularity for voltage level number extension, minimized voltage harmonics, cell capacitor voltage balancing ability, and system redundancy [10].

Motivated by HVDC application demand, DC fault reverse-blocking capability that can avoid the use of DC circuit breakers became of interest. As a result, the full-bridge (FB) cell MMC was developed to offer ride-through ability during DC-link voltage collapse but with twice the power switches and doubled the conduction losses. The mixed cell MMC contains both HB and FB cells in its arm; thus, it is able to block any AC side inrush current but with compromised power switch losses. The FB cells can also generate voltage with reversed polarity to the DC-link to boost the

AC side voltage and supply power to the grid when the DC voltage drops, but at the expense of challenging the cell capacitor voltage balancing implementation and increase the voltage stress on the power switches [11-14].

To reduce the footprint and cost of the conventional HB and FB MMCs, new topologies, termed hybrid multilevel converters (HMC), has been proposed. For example, the alternate arm multilevel converter (AAMC) and the AC side FB cell cascaded multilevel converter, etc. [15]. Since the arm current in these HMCs may be discontinuous due to the use of two-level chopped switches, voltage balancing implementation becomes critical.

5.2 Diode Clamped Multilevel Converter

The single-phase three-level DCMC topology is displayed in Fig. 5-1, where D_{c1} and D_{c2} are clamping diodes utilized for zero-voltage-level synthesis relative to the DC capacitor mid-point. The four self-commutated switching devices (S_1, S_2, S_3 and S_4) with freewheel diodes sustain half the DC-link voltage stress. During zero output voltage status, the positive and negative half DC-link capacitors are charged or discharged by the load current flowing through the relevant clamping diode and main switching device into or out of the neutral point.

The output voltage v_{Ao} has three voltage levels $\{+½V_{dc}, 0, -½V_{dc}\}$. The rail-to-rail $\pm½V_{dc}$ states are realized when the two switches in either the upper or lower arm are synchronously turned on; while the zero-state is achieved if the gate signals for S_2 and S_3 are triggered and the clamping diodes D_{c1} and D_{c2} are activated to exchange current between the DC-link mid-point and the AC side. These switch combinations for single-phase three-level DCMC are summarized in Table 5-1.

In the general N-level case, for each phase of the diode clamped converter, (N-1) capacitors are required to divide the voltage levels by their series connection across the common DC-link; and the total number of power semiconductor devices is 2×(N-1) self-commutated power switches plus (N-1)×(N-2) clamping diodes.

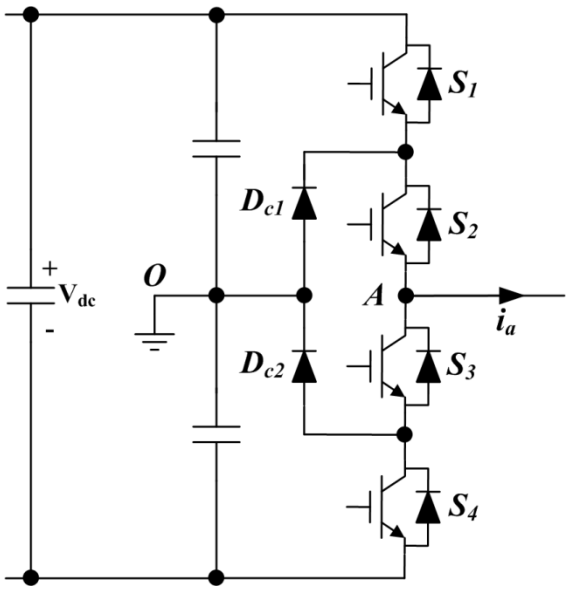


Fig. 5-1. Single-phase three-level DCMC topology.

Table 5-1. Operational states of single-phase three-level DCMC.

S_1	S_2	S_3	S_4	Output voltage v_{Ao}
on	on	off	off	$½V_{dc}$
off	on	on	off	0
off	off	on	on	$-½V_{dc}$

The DC-link mid-point voltage can be distorted by the charging and discharging processes during a zero-voltage-state if the mid-point current integration is not zero during every fundamental period. Although, theoretically, this integration should be zero in a three-level DCMC, the non-ideal hardware and controller parameters cause deviation; also in five or more level situations, the net current throughput of the mid-point is not equal, which causes operation malfunction and the topology degenerates to a three-level converter. Therefore, mid-point voltage balancing in a DCMC is challenging [16].

This can be solved by using independent DC sources or voltage balancing resistors at the expenses of increased total cost or losses. Alternatively, voltage balancing algorithms for DCMC are required to maintain normal operation. Due to unidirectional clamping of the diodes, the redundancy of the single-phase DCMC topology is limited and voltage balance is achieved by adjusting the dead-time in [16]; while in a three-phase system, the implementation of capacitor voltage

balancing can be realized by the rearrangement of the redundant vectors in SVM and the zero-sequence component injection method [17-23].

Taking the three-level DCMC in Fig. 5-1 as an example, although the anode (cathode) of the upper (lower) clamping diode D_{c1} (D_{c2}) is solidly connected to the DC-link mid-point; the other terminals of the diodes are floating between the series-connected power switches. Because of the unidirectional conductivity of the diodes, the stray inductance voltage drop cannot be released after commutation and this may cause further unbalance voltage stresses between the loosely clamped power switches. In order to overcome this practical problem, an auxiliary balancing resistor across the two clamping diodes is installed but introduces additional cost and losses [24]. To solve the uneven distribution of switching losses between the power devices in the NPC converter, the ANPC topology using active switches for clamping was developed [25].

The rapidly increasing device number and control complexity is the main DCMC topology constraint when applied in more than a five-level case. The complicated hardware installation makes water cooling system unreliable, thus limiting its maximum power capacity beyond 10MVA. The large number of devices and the severe DC capacitor voltage imbalance problem necessitate the use of external circuitry and time-consuming on-line algorithms to ensure normal operation, which devalue its practical viability.

5.3 Flying capacitor multilevel converter

The flying capacitor topology is another basic multilevel converter. Different from the DCMC, the flying capacitor multilevel converter employs capacitors with floating connection to clamp the output voltage to different levels. In a general N-level flying capacitor multilevel converter, (N-1) DC-link capacitors and ½(N-1)(N-2) flying capacitors in total are required for each phase. The nominal voltage stress on each power switch is equal to V_{dc}/(N-1). As an example, the single phase three-level flying capacitor multilevel converter is shown in Fig. 5-2, and all the switching combinations and possible output voltage levels are outlined by Table 5-2.

Similar to the DCMC topology, the flying capacitor multilevel converter is not appropriate for high voltage level applications due to reduced reliability and increased cost. Also, the modulation complexity and severe capacitor voltage

imbalance also limit its application is medium and high voltage power conversion [26].

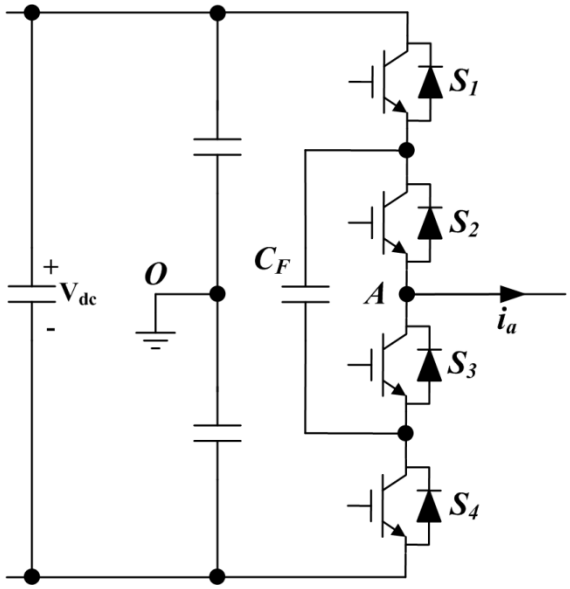


Fig. 5-2. Single-phase three-level flying capacitor multilevel converter.

Table 5-2. Output states of single-phase three-level flying capacitor multilevel converter

S_1	S_2	S_3	S_4	Output voltage v_{Ao}
on	on	off	off	$½V_{dc}$
on	off	on	off	0
off	on	off	on	0
off	off	on	on	$-½V_{dc}$

5.4 Other Multilevel Converter Clamping Techniques

Capacitor balancing regimes for diode and flying capacitor clamped converters are limited by power factor and other non-ideal factors due to the lack of converter redundancy. In an attempt to incorporate extra degrees of freedom for capacitor voltage balancing by using more clamping devices, the hybrid clamped multilevel converter in [7, 27, 28] was developed, where diodes, active switches and capacitors are utilized to insure the full range of voltage balance. However, these schemes all require a large number of devices and are not cost-effective.

The multilevel-Clamped multilevel converter (MLC2) was proposed in [6, 29], where the multilevel clamp concept is introduced to increase the voltage level

number and improve the modularity. The MLC2 power losses are analysed in [30] and the SVM using virtual vectors is implemented for voltage synthesis in [31]. However, the high voltage application of MLC2 is hindered due to the complex modulation algorithm and hardware configuration. Also, the capacitor voltage balancing strategy needs investigation.

5.5 Cascaded Full-bridge Multilevel Converter

The cascaded full-bridge multilevel converter in Fig. 5-3 was developed to achieve true modularity which benefits manufacturing and maintenance by reducing the topological complexity under high voltage conditions and introducing tolerance for modular-block failures. As a result, the overall reliability and efficiency of the control algorithm are optimized compared to those for clamping technique based multilevel converters. The main limitation of the cascaded full-bridge converter is the requirement of an independent DC source for each module, which is not appreciable if a common DC-link is necessary or multiple DC sources are unavailable. Thus, it is usually employed in the application involving photovoltaic (PV) integration, electric or hybrid vehicles DC transformers, AC static VAr compensation, etc. [32, 33].

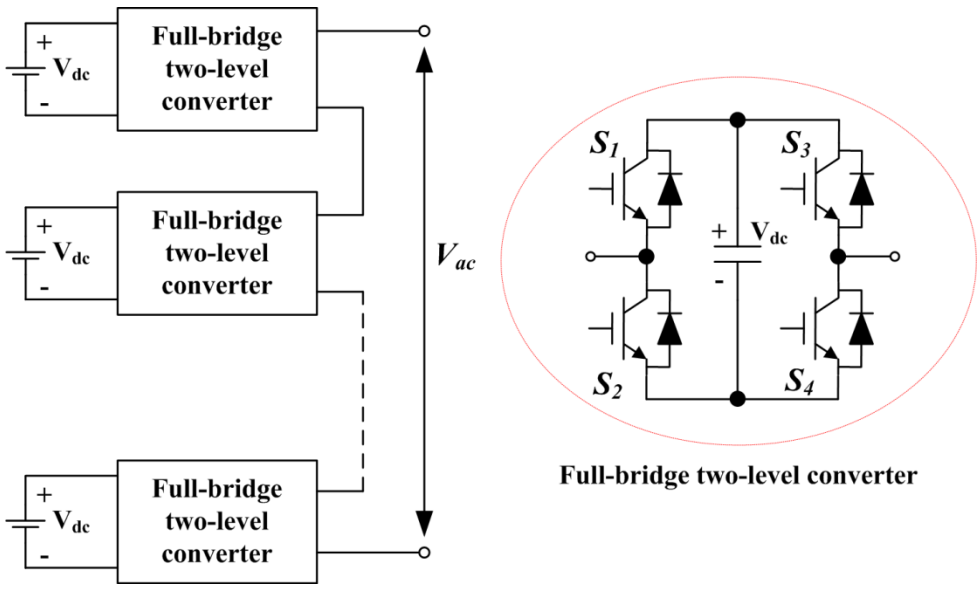


Fig. 5-3. Cascaded full-bridge multilevel converter.

5.6 Modular Multilevel Converter

The modular multilevel converter (MMC) was developed to achieve modularity and energy balance without using independent DC sources. Therefore, its application area is extended compared to the cascaded full-bridge converter. With different

functionality considerations, various MMC cell structures and different control strategies for cell capacitor voltage balancing, DC voltage ripple suppression, and inner current cancellation, have been investigated [13, 34-39].

5.6.1 MMC Based on Half-bridge Cells

The MMC is first proposed with basic half-bridge (HB) cells, and is capable of lowering switching losses and reducing the output voltage harmonics, based on a common DC-link.

The single-phase HB-MMC diagram is displayed in Fig. 5-4. If N cells are adopted in each arm, N+1 voltage levels can be synthesized on the AC side voltage with a power switch voltage stress of V_{dc}/N. In order to limit the inrush current in the loop of DC-link and cell stacks, an inductor is used in each arm. The arm inductance can also limit the harmonic components in the arm current as well as the current rising slope during short-circuit. Due to the fluctuating voltage on each cell capacitor, the arm current and output voltage will contain certain low order harmonics, predominantly the 2nd order [40, 41].

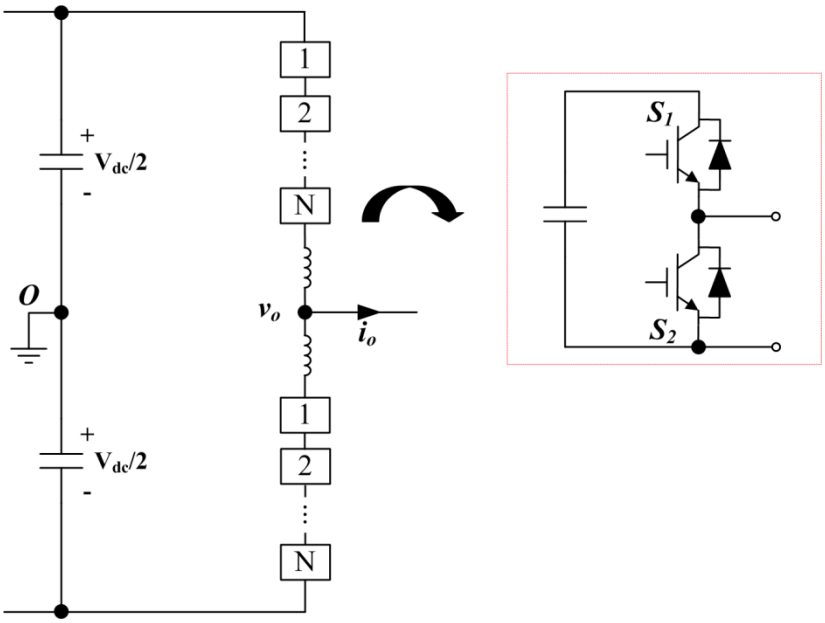


Fig. 5-4. Single-phase HB-MMC topology.

MMC energy balancing issues are solved by consideration of the arm current polarity and cell capacitor voltage sorting results. Due to system redundancy, the proper switching combinations can be selected to compensate the cell voltage errors in the intermediate voltage level region [10]. If the cell number is few, carried based pulse width modulation (CB-PWM) is used to generate a multilevel voltage with low THD;

while when the cell number is high and the cell voltage resolution is high enough relative to the AC side voltage, staircase modulation with direct reference tracking can be adopted, reducing the switching instances and losses.

The main HB-MMC advantages include derated voltage stress per switching device, reduced total switching instances, and average number of devices in conduction path (switching and conduction losses), as well as minimized size of AC side filters due to its improved voltage wave shaping ability [42]. However, the HB-MMC cannot operate if the DC-link voltage drops to below the AC side peak voltage (the rectification level) because the HB cells do not have the reverse-blocking ability for the AC side current. Therefore, in a HVDC transmission system, the HB-MMC is not able to ride-through a DC short-circuit fault. In medium or high voltage applications without long distance DC cables, such as renewable energy networking and FACTS devices, the converter should be bypassed and blocked when the DC voltage drops [43].

5.6.2 MMC with Reverse-blocking Cells

The MMC with full-bridge (FB) cells can block AC side reverse current due to the opposite series-connected diodes and boost the output voltage by utilizing the bipolar voltage generation ability of FB cells. Therefore, the FB-MMC is capable of maintaining power control ability during a DC voltage drop in renewable energy or in HVDC transmission applications [44].

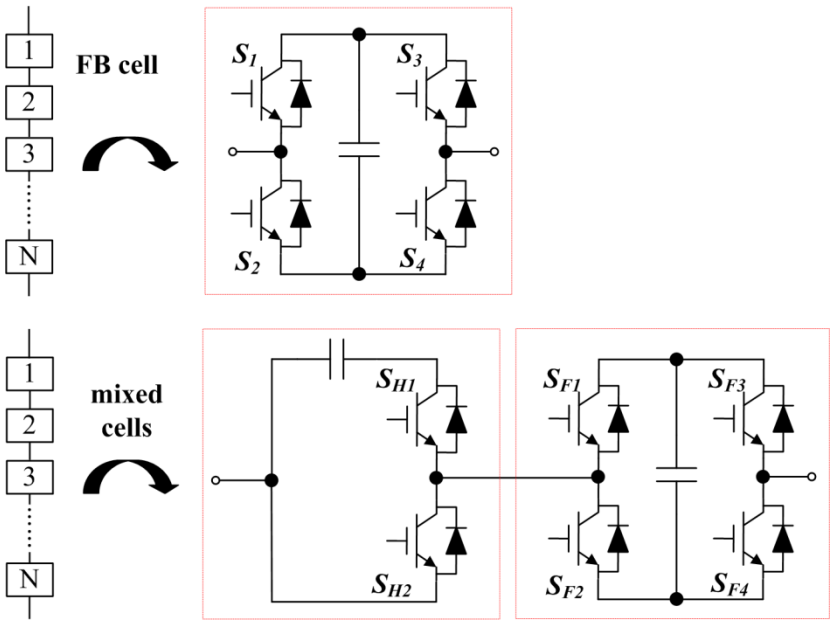


Fig. 5-5. MMC reverse-blocking cell structures.

However, for the same power rating, the FB-MMC conduction losses are almost twice those of the HB-MMC due to the doubled number of power devices in the conduction path. As a result, the overall FB-MMC power conversion efficiency is low [39]. As a compromise, the mixed cell MMC, using both HB and FB cells in each arm, was proposed, which is DC fault proof, with moderate power conversion losses [45].

In these DC fault tolerant MMC topologies with reverse-blocking cell structures as in Fig. 5-5, the use of FB voltage reverse ability improves the AC output voltage range but increases the power device voltage stresses and challenges cell capacitor voltage balancing implementation.

5.6.3 Multilevel Cell Structures

The three-level and extended multilevel cells for the MMC are also reported to block DC fault inrush current with lower conduction losses than the FB-MMC [14, 46, 47]. The multilevel cell based converter provides a higher voltage level number than conventional MMCs with the same number of cells in each arm; however, it uses more power switching devices and capacitors for each cell. The use of different cells can achieve a trade-off between power semiconductor losses and reverse blocking range. The main drawback of the multilevel cell based MMC is increased modulation complexity for cell energy balancing and voltage synthesis, which limits its practical use.

5.7 Hybrid Multilevel Converter

The MMC is competitive in medium and high voltage applications due to its modularity which reduces power conversion losses, has low dv/dt and high quality AC voltage. However, as the voltage and power rating increases, the footprint of MMC becomes large since a large number of cells are needed to sustain the full DC-link voltage and to generate a high number voltage levels. This array of many cell capacitors may also shorten converter service life due to the repeating charging and discharging processes of the DC capacitors.

The two-level VSC contains no cell capacitors but only stacks of power switches, thus converter size is smaller than the MMC. The hybrid multilevel converter (HMC) employs a two-level conversion stage as a phase director to change the voltage polarity; while the chain-links of the modular cells are responsible for optimize the

voltage waveform quality by superposition of cell capacitors and DC-link voltages. This combination can reduce the cell number required to generate a given voltage level and power rating, as a conventional MMC, which is expected to contribute a smaller footprint [48].

In these HMC topologies, since the arm current may be discontinuous due to the use of chopped switches, voltage balancing implementation for each cell becomes critical. The general laws for fulfilling energy balance can be summarised as follows:

- In a converter topology, there is a set consisting of a DC-link and modular cells whose net energy exchange is zero during one fundamental period; and
- Each member of this set must have opportunity to periodically exchange (increase or decrease) power with other members.

5.7.1 Alternate Arm Multilevel Converter

The alternate arm multilevel converter (AAMC) in Fig. 5-6 employs S_P and S_N as a pair of directing switches in each phase to synthesize the positive and negative half cycle voltage respectively. The chain-links of the modular cells tolerate half the DC-link voltage; thus, half the number of cells is required per phase to generate a given voltage level number. The directing switches are implemented by series connected power switches sustaining a maximum voltage stress equal to half the DC-link voltage. In the AAMC topology, the total number of devices in a conduction path is reduced compared to the FB-MMC [49].

In normal AAMC operation, the directing switches operate at the line frequency, while the chain-link cells are used to control the output voltage. Therefore, to realize cell voltage balance, energy exchange path between the DC-link and the chain-links should be facilitated. The first way is to use the zero output voltage periods to conduct both directing switches; and in this period, the cells in the upper and lower arms are modulated to exchange energy with the DC-link and compensate any voltage errors [49]. A zero-sequence current injection method is presented in [50] to decouple output voltage control and cell energy balancing.

In summary, the main AAMC contribution is a smaller footprint than the FB-MMC. It has moderate efficiency performance compared to the HB and FB MMCs. A scheme is necessary to maintain AAMC cell voltage balance.

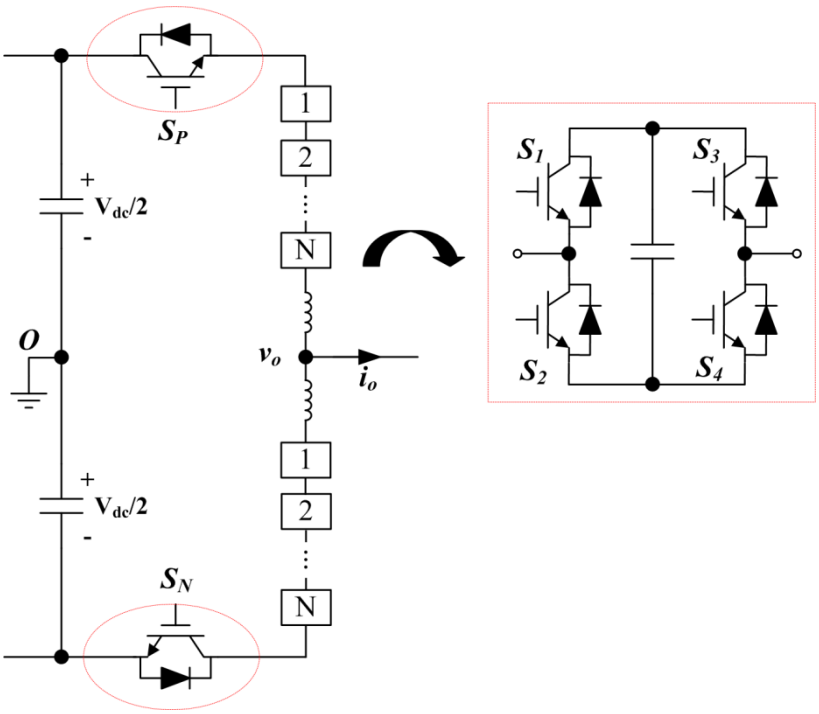


Fig. 5-6. Single-phase AAMC configuration.

5.7.2 Hybrid AC Side FB Cascaded Multilevel Converter

The HMC with AC side cascaded FB cells is shown in Fig. 5-7, which consists of a two-level conversion stage for output voltage generation and a cascaded chain-link of FB cells that acts as an active power filter to suppress associated low order voltage harmonics from the two-level converter. The two-level converter stage is usually modulated by selective harmonic elimination (SHE) at a low frequency (50-200Hz) to offer fundamental voltage control ability, with a modest increase in switching losses [51, 52].

Due to the cascaded structure of the AC side, no additional arm inductance is needed; but its AC side chain-link is restricted to sustain zero fundamental voltage in order to guarantee cell energy balance over the full power factor range.

For low power factor applications, the chain-link of FB cells of the cascaded HMC has been reported to be utilized to boost the output voltage [53]. In this way, twice the voltage level number is achieved and an even smaller footprint is expected.

Since full load current flows through the two-level converter series-connected power devices and the FB cells chain-link, the total conduction losses are expected to be higher than the AAMC.

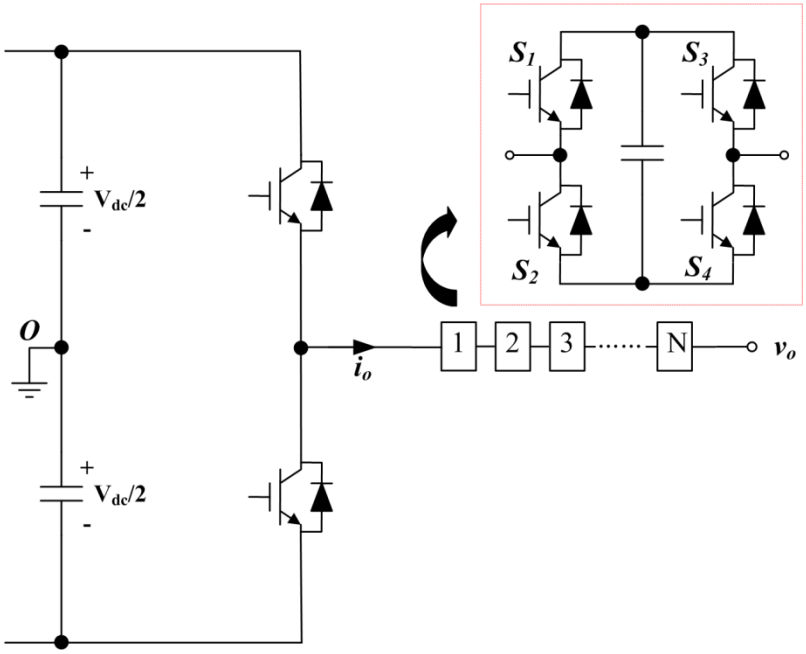


Fig. 5-7. Single-phase AC Side FB cascaded HMC.

5.7.3 Other Hybrid Multilevel Converters

The parallel HMC topology using a wave-shaping circuit and phase directing switches in parallel is proposed in [54, 55], where the three-phase chain-links are series connected across the full DC-link. However, this converter fails to maintain the cell voltage balance during low power factor conditions; in addition, the voltage stress on the power devices depends on modulation index, which reduces reliability. In [54], triplen component injection is employed to ease this difficulty.

The HMC with DC side cascaded FB cells was analysed in [56] with doubled power density and DC voltage utilization. However, the total conduction losses are still high due to its series connection of power devices.

5.8 Summary

This chapter summarized the evolution of multilevel converter topologies. The clamping technique based multilevel converters; cascaded full-bridge converter; state-of-art MMC and HMC were reviewed and compared. Among these candidates, the MMC and HMC outperforms the clamped multilevel converters in terms of modularity and scalability; and compared to cascaded full-bridge converter, the independent DC input for each module can be avoided.

MMC requires a large number of cells per arm to synthesize the desired high quality output voltage waveform. As motivation to reduce the MMC footprint, various HMC

topologies have been introduced but are associated with increased power conversion losses, compared to the HB-MMC.

Reference

[1] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on,* vol. 49, pp. 724-738, 2002.

[2] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *Industry Applications, IEEE Transactions on,* vol. IA-17, pp. 518-523, 1981.

[3] P. M. Bhagwat and V. R. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *Industry Applications, IEEE Transactions on,* vol. IA-19, pp. 1057-1069, 1983.

[4] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, 1992, pp. 397-403 vol.1.

[5] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, "Active-neutral-point-clamped (ANPC) multilevel converter technology," in *Power Electronics and Applications, 2005 European Conference on*, 2005, pp. 10 pp.-P.10.

[6] P. Rodriguez, M. D. Bellar, R. S. Munoz-Aguilar, S. Busquets-Monge, and F. Blaabjerg, "Multilevel-Clamped Multilevel Converters (MLC2)," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 1055-1060, 2012.

[7] C. Alian and H. Xiangning, "Research on Hybrid-Clamped Multilevel-Inverter Topologies," *Industrial Electronics, IEEE Transactions on,* vol. 53, pp. 1898-1907, 2006.

[8] H. Iman-Eini, J. L. Schanen, S. Farhangi, and J. Roudet, "A Modular Strategy for Control and Voltage Balancing of Cascaded H-Bridge Rectifiers," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 2428-2442, 2008.

[9] H. Keivani, M. R. Askari, F. Kavehnia, M. G. HosseiniAghdam, and A. Mohammadi, "Novel Multi-Carrier PWM Method for a Three-Phase Cascaded H-Bridge Multi-Level Inverter," in *Universities Power Engineering Conference, 2006.UPEC '06. Proceedings of the 41st International*, 2006, pp. 593-597.

[10] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *Power Electronics, IET,* vol. 3, pp. 702-715, Sep 2010.

[11] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 4-17, 2015.

[12] D. Fujin and C. Zhe, "A Control Method for Voltage Balancing in Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 66-76, 2014.

[13] S. Debnath, Q. Jiangchao, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter:

A Review," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 37-53, 2015.

[14] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 18-36, 2015.

[15] G. P. Adam, S. J. Finney, and B. W. Williams, "Hybrid converter with ac side cascaded H-bridge cells against H-bridge alternative arm modular multilevel converter: steady-state and dynamic performance," *Generation, Transmission & Distribution, IET,* vol. 7, pp. 318-328, 2013.

[16] I. Staudt and M. Sprenger, "Development of a New 1000 V / 1 MVA IGBT 3L-NPC-VSC PEBB Type 2 with Independent Modulation, DC-Link Balancing and Short-Circuit Protection," in *Integrated Power Systems (CIPS), 2014 8th International Conference on*, 2014, pp. 1-5.

[17] S. Wenxiang, C. Guocheng, D. Xiaoyu, and S. Mantang, "Research on Neutral-point Balancing Control for Three-level NPC Inverter Based on Correlation between Carrier-based PWM and SVPWM," in *Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International*, 2006, pp. 1-6.

[18] C. Newton and M. Sumner, "Novel technique for maintaining balanced internal DC link voltages in diode clamped five-level inverters," *Electric Power Applications, IEE Proceedings* -, vol. 146, pp. 341-349, 1999.

[19] C. Newton and M. Sumner, "A novel arrangement for balancing the capacitor voltages of a five level diode clamped inverter," in *Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (Conf. Publ. No. 456)*, 1998, pp. 465-470.

[20] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Limits of the neutral-point balance in back-to-back-connected three-level converters," *Power Electronics, IEEE Transactions on,* vol. 19, pp. 722-731, 2004.

[21] J. Pou, R. Pindado, D. Boroyevich, P. Rodriguez, and J. Vicente, "Voltage-balancing strategies for diode-clamped multilevel converters," in *Power Electronics Specialists Conference, 2004. PESC 04.2004 IEEE 35th Annual*, 2004, pp. 3988-3993 Vol.5.

[22] A. Laka, J. AndoniBarrena, J. Chivite-Zabalza, and M. A. Rodriguez, "Passive balancing of the DC bus midpoint for Neutral Point Clamped (NPC) based Voltage Source Converters," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, 2013, pp. 1148-1153.

[23] Z. Huibin, S. J. Finney, A. Massoud, and B. W. Williams, "An SVM Algorithm to Balance the Capacitor Voltages of the Three-Level NPC Active Power Filter," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 2694-2702, 2008.

[24] W. Jun, Y. Binjian, Z. Jing, D. Yan, H. Xiangning, and Z. Xu, "Development of a compact 750KVA three-phase NPC three-level universal inverter module with specifically designed busbar," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 1266-1271.

[25] D. Floricau, C. L. Popescu, M. O. Popescu, E. Floricau, and L. Spataru, "A comparison of efficiency for three-level NPC and Active NPC voltage source

converters," in *Compatibility and Power Electronics, 2009. CPE '09.*, 2009, pp. 331-336.

[26] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 58-62.

[27] K. Young-Seok, S. Beom-Seok, and H. Dong-seok, "A new N-level high voltage inversion system," in *Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on*, 1993, pp. 1252-1257 vol.2.

[28] P. Fang Zheng, "A generalized multilevel inverter topology with self voltage balancing," *Industry Applications, IEEE Transactions on,* vol. 37, pp. 611-618, 2001.

[29] P. Rodriguez, M. D. Bellar, R. S. Munoz-Aguilar, J. Rocabert, and A. Luna, "Multilevel-clamped multilevel converters (MLC2) - an alternative approach for multilevel power conversion," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 4433-4438.

[30] M. Ke, R. S. Munoz-Aguilar, P. Rodriguez, and F. Blaabjerg, "Thermal and Efficiency Analysis of Five-Level Multilevel-Clamped Multilevel Converter Considering Grid Codes," *Industry Applications, IEEE Transactions on,* vol. 50, pp. 415-423, 2014.

[31] P. Rodriguez, Mu, x00F, R. S. oz-Aguilar, S. Busquets-Monge, M. D. Bellar, *et al.*, "Virtual-vector-based space vector pulse width modulation of the DC-AC multilevel-clamped multilevel converter (MLC²)," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 170-176.

[32] X. Liang, R. Li, and X. Cai, "Control of a battery-energy-storage system based on a cascaded H-Bridge converter under fault condition," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, 2012, pp. 952-957.

[33] J. Rodriguez, S. Bernet, W. Bin, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 2930-2945, 2007.

[34] M. Ji-Woo, K. Chun-Sung, P. Jung-Woo, K. Dea-Wook, and K. Jang-Mok, "Circulating Current Control in MMC Under the Unbalanced Voltage," *Power Delivery, IEEE Transactions on,* vol. 28, pp. 1952-1959, 2013.

[35] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzande, J. C. Vannier, *et al.*, "An Energy-Based Controller for HVDC Modular Multilevel Converter in Decoupled Double Synchronous Reference Frame for Voltage Oscillation Reduction," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 2360-2371, 2013.

[36] J. Bocker, B. Freudenberg, A.The, and S. Dieckerhoff, "Experimental Comparison of Model Predictive Control and Cascaded Control of the Modular Multilevel Converter," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 422-430, 2015.

[37] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac, "Modular Multilevel Converter With Different Submodule Concepts - Part I:

Capacitor Voltage Balancing Method," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 4525-4535, 2013.

[38] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 349-357, 2015.

[39] C. Shenghui, K. Sungmin, J. Jae-jung, and S. Seung-Ki, "Principle, control and comparison of modular multilevel converters (MMCs) with DC short circuit fault ride-through capability," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 610-616.

[40] A. Rasic, U. Krebs, H. Leu, and G. Herold, "Optimization of the modular multilevel converters performance using the second harmonic of the module current," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.

[41] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 57-68, 2012.

[42] M. Wu Cong, Y. Avenas, M. Miscevic, M. X. Wang, R. Mitova, J. P. Lavieville, *et al.*, "Thermal analysis of a submodule for modular multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, 2014, pp. 2675-2681.

[43] G. P. Adam and B. W. Williams, "Half- and Full-Bridge Modular Multilevel Converter Models for Simulations of Full-Scale HVDC Links and Multiterminal DC Grids," *Emerging and Selected Topics in Power Electronics, IEEE Journal of,* vol. 2, pp. 1089-1108, 2014.

[44] L. Younggi, C. Shenghui, K. Sungmin, and S. Seung-Ki, "Control of hybrid HVDC transmission system with LCC and FB-MMC," in *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, 2014, pp. 475-482.

[45] G. P. Adam, K. H. Ahmed, and B. W. Williams, "Mixed cells modular multilevel converter," in *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on*, 2014, pp. 1390-1395.

[46] R. Marquardt, "Modular Multilevel Converter topologies with DC-Short circuit current limitation," in *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, 2011, pp. 1425-1431.

[47] R. Li, J. E. Fletcher, L. Xu, D. Holliday, and B. W. Williams, "A Hybrid Modular Multilevel Converter with Novel Three-level Cells for DC Fault Blocking Capability," *Power Delivery, IEEE Transactions on,* vol. PP, pp. 1-1, 2015.

[48] C. C. Davidson and D. R. Trainer, "Innovative concepts for hybrid multi-level converters for HVDC power transmission," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.

[49] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, "A new hybrid multi-level Voltage-Source Converter with DC fault blocking capability," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.

[50] A. M. Cross, D. R. Trainer, and R. W. Crookes, "Chain-link based HVDC Voltage Source Converter using current injection," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.

[51] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on,* vol. 28, pp. 335-346, 2013.

[52] G. P. Adam, I. A. Abdelsalam, K. H. Ahmed, and B. W. Williams, "Hybrid Multilevel Converter With Cascaded H-bridge Cells for HVDC Applications: Operating Principle and Scalability," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 65-77, 2015.

[53] Z. Yushu, G. P. Adam, T. C. Lim, S. J. Finney, and B. W. Williams, "Hybrid Multilevel Converter: Capacitor Voltage Balancing Limits and its Extension," *Industrial Informatics, IEEE Transactions on,* vol. 9, pp. 2063-2073, 2013.

[54] R. Feldman, M. Tomasini, J. C. Clare, P. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

[55] R. Feldman, M. Tomasini, J. C. Clare, P. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A low loss modular multilevel voltage source converter for HVDC power transmission and reactive power compensation," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.

[56] G. P. Adam and B. W. Williams, "New emerging voltage source converter for high-voltage application: hybrid multilevel converter with dc side H-bridge chain links," *Generation, Transmission & Distribution, IET,* vol. 8, pp. 765-773, 2014.

CHAPTER 6

Controlled Transition Full-bridge Hybrid Multilevel Converter with Chain-links of Full-bridge Cells

This chapter proposes a controlled transition full-bridge (CTFB) hybrid multilevel converter (HMC) for medium and high voltage applications, which employs a full-bridge cell chain-link (FB-CL) between the two legs in each phase to generate multilevel bipolar output voltage. The CTFB-HMC has twice DC voltage utilization or power density of conventional converters due to the bipolar capability of its full-bridge configuration. Hence, for the same power rating and same voltage level number, its total cells per phase are quarter that in the MMC, which reduces the hardware installation volume. Also, the total device number in the conduction paths is the same as in the HB-MMC; thus, improving the efficiency performance. Also the FB-CL current of the CTFB converter has no DC component, which offers the potential to enhance the transient response. Comparative studies between the CTFB and other multilevel topologies are carried out to show its main features. Modulation strategies and parameter sizing of the proposed converter are investigated using a generic case. Simulation and experimental results are used to verify the effectiveness of the proposed approach.

6.1 Background

With increasing penetration of voltage source converter (VSC) techniques into high-voltage high-power applications such as machine drives, large scale distributed energy source integration and power system control, the multilevel converter has attracted research attention due to its reduced EMI emission and improved voltage wave shaping ability compared with the two-level converter [1-8].

Amongst the various multilevel topologies, the modular multilevel converter (MMC) contributes advantages of modularity, redundancy, hardware simplification and less modulation complexity than the cascaded full-bridge converter and clamping technique based solutions including diode and flying capacitor clamped converters [8]. The basic MMC has half-bridge (HB) cells, and when extended to a full-bridge (FB) cell MMC is able to offer ride-through ability during DC voltage collapse but with doubled the power switch losses. As a compromise, the mixed cell MMC employs both kinds of cells in the arm, facilitating reverse blocking capability with lower conduction losses than the FB-MMC [6, 9-13].

In general, conventional MMCs require a large cell number to synthesize the voltage waveform with a high number of voltage levels; thus, their footprints may be large due to the array of cell capacitors and power switching devices. To combine the advantages of the two-level VSC (low device number) and the MMC (less EMI and switching losses), several new topologies have evolved and are termed hybrid multilevel converters (HMCs).

The alternative arm multilevel converter (AAMC) presented in [14] employs a directing switch made up of series connected power switches in each arm to alternatively use the upper or lower full-bridge cell chain-link (FB-CL) for voltage synthesis. In this way, the number of cells can be halved compared with conventional MMCs. To ensure energy balancing of the cell capacitors, directing switch AC voltage zero-crossing commutation is utilized. This overlap region of the upper and lower arms allows both arms to operate as a typical MMC, thus allowing energy exchange in the inner loop. Another method is to inject a zero-sequence current component, which offers a path for power compensation between the cell stacks and the DC-link [15]. These all increase control complexity. But successful commutation between the upper and lower arms in the AAMC is not guaranteed when the AC side voltage is distorted during fault conditions.

The HMC with AC side cascaded FB cells offers an even smaller footprint with half the cell number of the AAMC by moving the chain-links to the AC side in series with the load, avoiding additional arm inductance [16]. In this topology, the two-level converter is modulated by selective harmonic elimination (SHE), facilitating fundamental voltage control and improve DC-link voltage utilization; while its AC side FB-CL behaves like an active filter that attenuates low order voltage harmonics. The energy balancing of cell capacitors can be fulfilled by modulating the cells according to the reference signal, capacitor voltage sorting and phase current polarity. Practically, the FB-CL needs a small fundamental voltage to compensate for internal losses. The main shortcoming of this converter is high power losses due to the hard-switched power devices in the two-level converter stage and the increased total device number in the conduction paths.

Another topology with a HB cell based chain-link wave-shaping circuit and phase directing switches in parallel has been reported in [17]. The three phases are in series to support the full DC-link voltage. Its main drawback is the confliction between cell voltage balancing and reactive power exchange, which will vary the voltage stress on the power devices when the AC side voltage reference is adjusted, thus losing black-start ability and hampering its practical exploitation.

A HMC with DC side cascaded FB cells is analysed in [18], where a FB two-level converter is used as a phase director and the FB-CL is located in the DC side for each phase. It is able to decouple the power flow control from the energy balancing of cell capacitors by using the zero-state to parallel connect the chain-link and DC-link, which is advantageous to that in [17]. The total required cell number for this converter is the same as the AAMC topology. However, its disadvantage of high power semiconductor losses persists, as in the AC side FB cascaded converter.

In this chapter, a novel HMC topology using the controlled transition full-bridge (CTFB) configuration is proposed for medium and high voltage applications such as flexible AC transmission system (FACTS) devices and machine drives. It has twice the DC utilization and a quarter the cells of the HB-MMC for the same power rating, thus high power density and small footprint are expected. The device number in the conduction path in the CTFB-HMC is equal to that in the HB-MMC and significantly less than other MMCs and HMCs; thus, conduction losses are minimized. It also has

zero DC current in the chain-link, which may bring advantages over the MMC in terms of dynamic performance.

6.2 Proposed Controlled Transition Full-bridge (CTFB) Hybrid Multilevel Converter (HMC)

The schematic of the single-phase CTFB-HMC is shown in Fig. 6-1, where the FB-CL is employed to dynamically clamp the voltage between two leg terminals "*x*" and "*y*" to synthesize a true multilevel output voltage waveform v_{xy} as shown in Fig. 6-2. The maximum AC side peak voltage is equal to the DC-link voltage with $2N+1$ voltage levels when the FB-CL has N cells. Therefore, to generate the same voltage levels as the conventional MMC, the cell number per phase in the CTFB-HMC is a quarter and both polarities of its FB cells are utilized; besides, the DC utilization is twice of that with MMCs, AAMC and the AC side cascaded FB topologies, which indicates a higher power density and smaller footprint for the CTFB-HMC. The power switch voltage stress V_{cell} in the CTFB-HMC is expressed as (6.1).

$$V_{cell} = V_{dc} / N \tag{6.1}$$

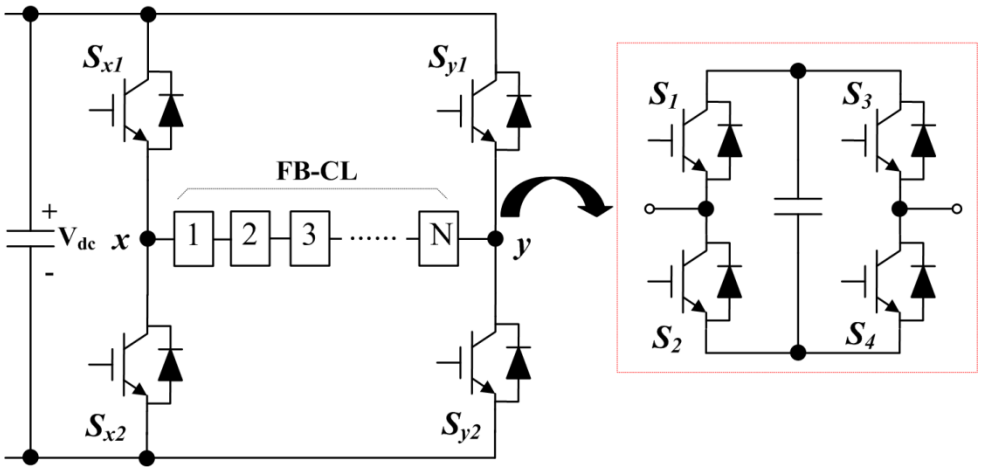


Fig. 6-1. The topology of single-phase CTFB-HMC and cell structure.

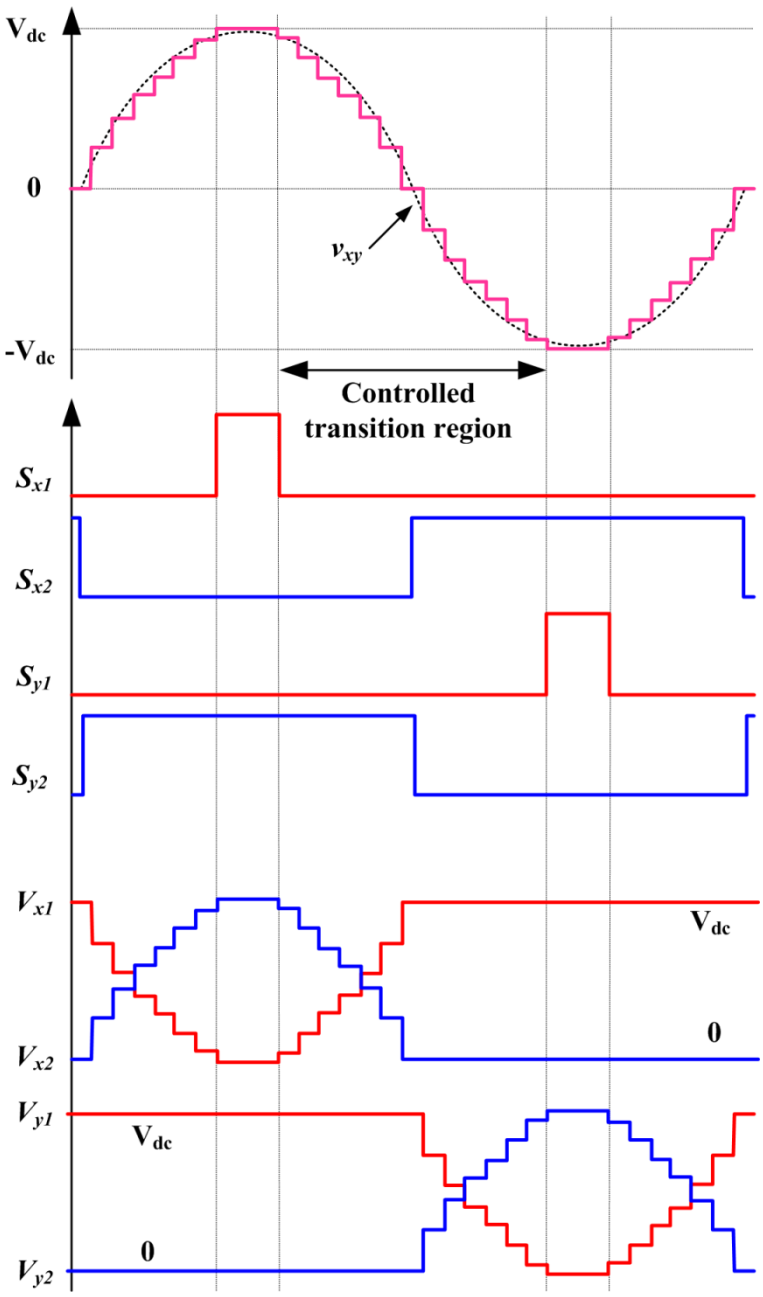


Fig. 6-2. The maximum synthesized multilevel voltage and key waveforms of the main directing switches for the single-phase CTFB-HMC.

To generate a true multilevel output from the CTFB-HMC, its FB-CL should be activated to dynamically clamp the two leg terminals "*x*" and "*y*" to track the reference, while the main directing switches {S_{x1}, S_{x2}} and {S_{y1}, S_{y2}} are operated diagonally when the output voltage is clamped to $\pm V_{dc}$; thus allowing the energy exchange between the DC-link and FB-CL. The gate signals and sustained voltage of the main directing switches are interpreted in Fig. 6-2, where the transitions of S_{x1} and S_{y1} occur when there blocked voltage is equal V_{cell} in (6.1), thus the switching losses and dv/dt can be largely reduced. The conditions for S_{x2} and S_{y2} are further

improved, since they operate at zero voltage and current condition, which means they do not create any switching losses. Also the directing switches only turn on and off at a low frequency, thus their switching losses are minimal. From Fig. 6-2, the FB-CL is responsible for voltage synthesis during the controlled transition region, while the main directing switches are activated for rail-to-rail voltage clamping.

This time-division mode of the main directing switches and FB-CL is able to reduce the device number in the conduction paths, thus minimizing the conduction losses. As an illustration, the HB-MMC can generate the same AC voltage and power rating as the proposed converter when its dc link voltage is $2V_{dc}$ and with $2N$ cells in each arm ($4N$ per phase). So the total device and conduction path device numbers for HB-MMC are $8N$ and $2N$ respectively, which are the same as for the CTFB-HMC. Alternatively, if same DC- link V_{dc} and number of cell per arm N are employed, the power rating of HB-MMC is half of that in CTFB-HMC when the same load current is assumed, and the total device and conduction path device numbers become $4N$ and N. This means the total conduction loss percentage of the CTFB-HMC is generally the same as that in the HB-MMC. Since HB-MMC offers lower losses than the FB-MMC, AAMC and FB cell cascaded HMCs, it is expected that the proposed CTFB-HMC is also superior in terms of efficiency [19]. In fact, from Fig. 6-1, the chain-link current in the CTFB converter has no DC component. This implies that dynamic response for the proposed converter is better than the HB-MMC at high power factor high modulation index conditions when the total active power increases and the DC component of the MMC arm current reaches its maximum.

In practise, the HMC with AC side cascaded FB cells in [20] can avoid additional arm inductance for current limiting due to the series connection of the chain-link with the load but at the expense of increasing the total conduction losses. For non-cascaded topologies, the inductance is necessary to limit the potential inrush current during energy exchange between DC-link and the cells. Also, the two-level configuration of the directing switches in the CTFB-HMC determines the discontinuous current waveform in the DC side. Therefore, a circulating valve with parallel combination of inductance and clamping switch is introduced into its DC path as in Fig. 6-3. The clamping switch is triggered when the energy exchange paths between the DC-link and FB-CL are cut-off. This switch could be a diode in unidirectional power flow applications such as renewable energy source integration

without storage; however, to ensure the current limit function under four-quadrant operation, a bidirectional switching device is employed. The voltage stress of this device is low, leading to the negligible switching losses. To minimize the circulating losses, an integrated gate commutated thyristor (IGCT) with a smaller forward voltage drop is suggested. Compared to conventional MMCs with a pair of inductors in each phase, the proposed converter is able to share a common DC side inductor for multiple phases to limit the inrush current, thus reducing overall size and weight.

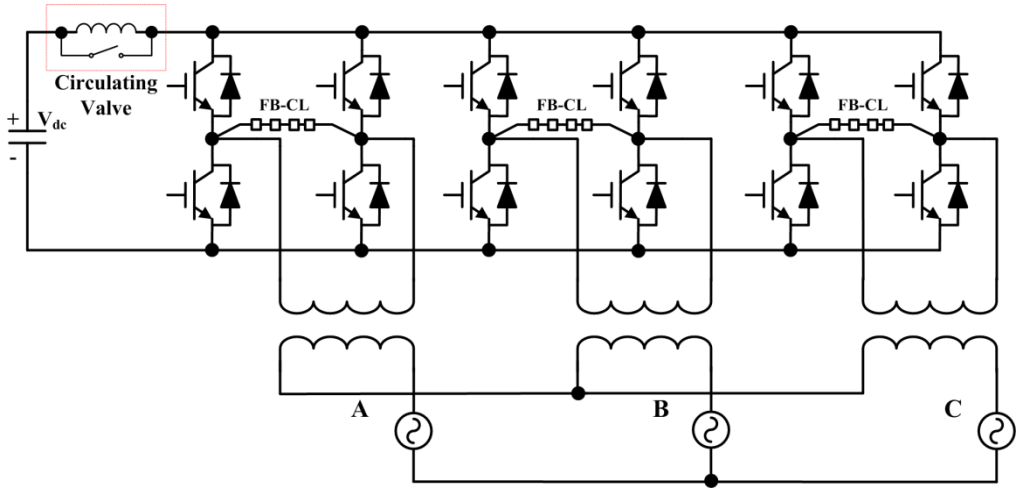


Fig. 6-3. Grid-tied three-phase CTFB-HMC with DC side circulating valve for current limiting.

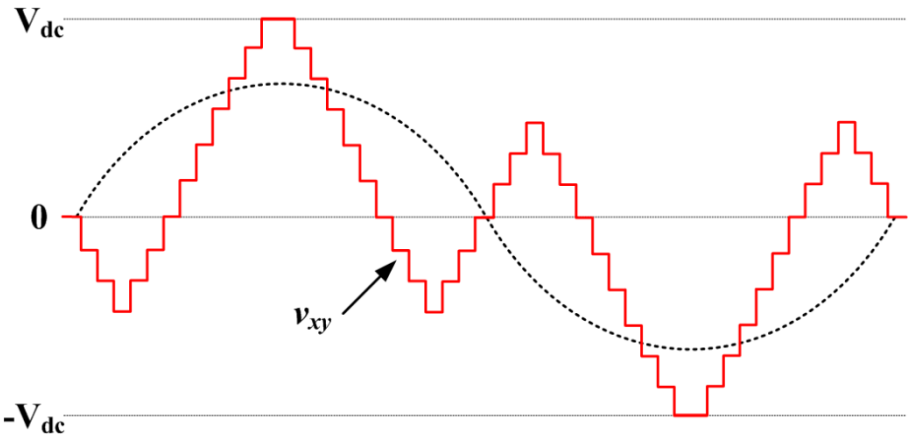


Fig. 6-4. AC side phase voltage waveform with triplen components injection.

Since the main directing switches and FB-CL operate alternatively except during short period, the energy balancing of the cell capacitors relies on the DC-link conduction path, which means the modulation index is critical for voltage balancing realization. To overcome this constraint, the triplen components are injected to guarantee enough time for the reference signal to touch the boundaries defined by $\pm V_{dc}$. These triplen components can be neutralized in a three-phase system. The

voltage reference for each phase is expressed in (6.2), where m is the required fundamental modulation index, ω is the fundamental angular frequency, θ_0 is the phase angle relative to the phase-locked-loop (PLL) reference system and $\omega t+\theta_0$ represents the real-time angle of the fundamental voltage. The waveform of output voltage in the converter AC side is shown in Fig. 6-4. For typical three-phase system in Fig. 6-3 with {0, -⅔π, ⅔π} phase differences, the triplen components cannot propagate and the secondary side line-to-line voltage between phase 'A' and 'B' is calculated by (6.3), where n_t is the turns-ratio of the adopted interfacing transformer.

$$v_{xy} = \mathrm{V_{dc}} \cdot m\cos(\omega t+\theta_0) - \mathrm{V_{dc}} \cdot (m-1)\cdot\cos[3(\omega t+\theta_0)] \tag{6.2}$$

$$v_{AB} = \sqrt{3} n_t \mathrm{V_{dc}} \cdot m\cos(\omega t+\theta_0+\tfrac{1}{6}\pi) \tag{6.3}$$

With the modulation scheme in Fig. 6-4, the injected triplen components can guarantee the energy exchange between DC-link and the chain-link cells within short duration, which is several sampling period. In low power factor applications such as grid reactive power controller, there is theoretically zero energy exchange between the chain-link capacitors and DC-link except for the internal losses. Thus, the inrush current superposed to the directing switches is minor. However, for the cases with large amount of active power transfer, the chain-link capacitors need to exchange energy with DC-link, leading to the inrush current through directing switches and chain-link when the modulation reference reaches '±1'.

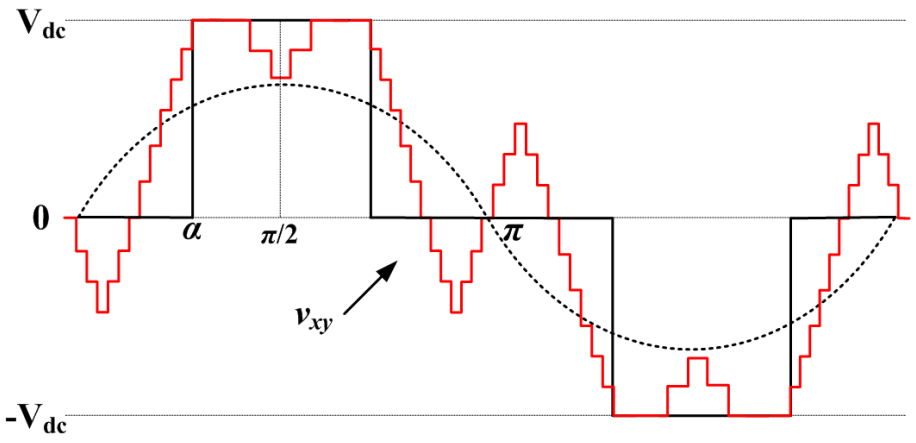


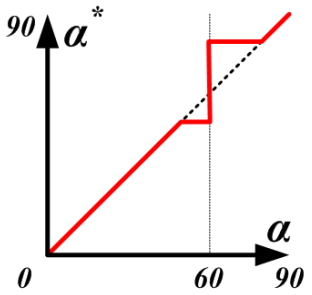
Fig. 6-5. Modified modulating waveform for high active power applications.

The inrush current can cause extra power losses. By extending the clamping duration of the chain-link voltage to '±1', more active power is transferred through the directing switches, thus reducing the voltage deviation of the cell capacitors. Also for fixed energy exchange, a longer period reduces the inrush current RMS. Therefore,

the inrush current power losses can be effectively limited by the clamping time increase. Such techniques are found in the literature such as trapezoidal modulation but with low order harmonic emergence [21, 22]. To optimize the amount of low order harmonics due to the voltage clamp (saturation), multi-slope trapezoidal modulation is presented in [21]. Although the maximum AC voltage can be increased with these methods, their modulation control range is limited due to the narrowed wave-shaping ability. To further reduce the low order harmonics and extend the modulation index control range, a new triplen component injection scheme is introduced in Fig. 6-5.

If the targeted modulation index is m (fundamental voltage is $m\mathrm{V}_{\mathrm{dc}}$), in Fig. 6-5, the width-variant rectangular wave can be employed to represent the equivalent fundamental voltage, where α is the angle of the rectangular waveform. Thus, (6.4) is obtained from its Fourier series. At $\omega t=\alpha$, the normalized fundamental voltage plus the injected triplen harmonic is set to 1pu to ensure that the equivalent modulating signal always touches 1 and -1 (which are equivalent to $+V_{dc}$ and $-V_{dc}$). As α approaches 60 °, the triplen component value (3α is around 180 °) asymptotes to zero (represents a point of discontinuity), making the desired amplitude of triplen injection high thus reducing the actual fundamental voltage in the clamped modulating signal. To overcome this, a dead-zone is inserted to calibrate the angle for triplen amplitude calculation as in Fig. 6-6.

$$m = 4/\pi \cos\alpha, \quad \alpha \in [0^\circ, 90^\circ] \tag{6.4}$$



$$\alpha^* = \begin{cases} \alpha, \alpha \in [0^\circ, 50^\circ) \cup (80^\circ, 90^\circ] \\ 80^\circ, \alpha \in [60^\circ, 80^\circ] \\ 50^\circ, \alpha \in [50^\circ, 60^\circ) \end{cases}$$

Fig. 6-6. Modified clamping angle for triplen component injection.

Then, with α^* known (in Fig. 6-6) and solving (6.5), the amplitude of triplen injection for different m can be achieved as m_t, which is used to replace the term (m -1) in (6.2).

$$m\sin\alpha + m_t \sin 3\alpha^* = 1 \tag{6.5}$$

By applying saturation to the superposed signal, the staircase voltage waveform results are shown as in Fig. 6-5, which extends the AC side peak voltage beyond V_{dc} and more precisely tracks the sinusoidal waveform on the slope and peak areas than trapezoidal methods, thus reducing the lower harmonics. Although the dead zone being adopted may introduce inaccuracies at lower modulation indices, this region is only used briefly during system start-up. Otherwise, for practical reasons associated with power loss and waveform quality, the entire P-Q and Q-V envelopes of the proposed converter, when connected to grid as FACTS devices or inverters, is usually designed to be realised with modulation index above 0.8, which is beyond the imposed dead zone.

Notice that, the modulation method in Fig. 6-5 is recommended to be used in high active power applications. In these cases, it can decrease the capacitor size and reduce the DC side current by reducing the angle α. However, since the clamping area may have overlap between phases if α is smaller than 60 °, the inrush current limiting inductance should not be centralized in the DC-link as in Fig. 6-3. On the contrary, the inductance can be distributed into each phase to limit the current exchanges between phases. In high active power condition with the modified modulation scheme, due to the extended voltage clamping period and reduced cyclical cell energy wane, the total inductance remains similar value as that of the configuration in Fig. 6-3 with low power factor and sinusoidal modulation.

In summary, all voltage clamping (saturation) methods can increase the power rating (DC voltage utilization) and reduce the power losses as illustrated. These attributes are achieved with the penalty of emerging low order harmonics in the AC side, which may require a relatively small tuned-filter in order to satisfy the grid code.

Since the focus of this converter is as a candidate for FACTS devices involving small amounts of active power (low power factor), the sinusoidal modulation scheme in Fig. 6-4 is employed here after, unless otherwise stated.

6.3 Modulation with Cell Capacitor Voltage Balancing Algorithm

The algorithm for cell capacitor voltage balancing of the CTFB-HMC is presented in this section. During intermediate voltage levels, the FB-CL uses both polarities as well as zero-state to synthesize the AC side voltage and self-adjust the charging and discharging status of each cell capacitor according to the voltage sorting and load current polarity. When the reference reaches the DC-link, energy exchange occurs

between the cell capacitors and DC-link, where the power exchange can be in either direction depending on the operational quadrant of the converter.

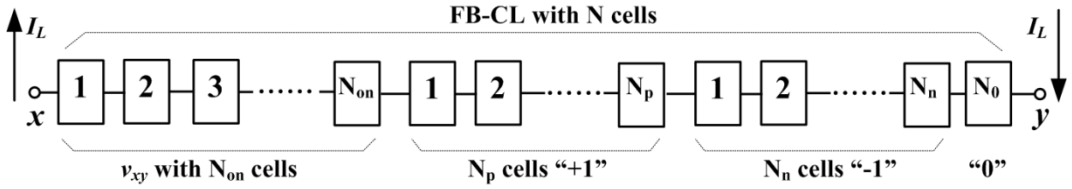


Fig. 6-7. Cell status distribution in the FB-CL during intermediate voltage levels.

Each CTFB-HMC phase with N cells in the FB-CL uses the reference in (6.2) to synthesize the multilevel voltage waveform in Fig. 6-4. Considering high voltage situations where the cell number $N \geq 10$, the resolution of the cell voltage in (6.1) to approximate a sinusoidal waveform becomes acceptable, Thus, staircase modulation using nearest voltage levels to directly track the reference can be implemented, which avoids extra switching action and saves the switching losses compared to carrier based pulse width modulation (CB-PWM). The cell number required to generate the target voltage is calculated from (6.6), where the negative N_{on} represents the negative polarity of the AC side voltage. Then, the rest of the cells should produce a net zero output voltage. To better utilize these redundant switching cells for energy balancing, the strategy in Fig. 6-7 is adopted, where the outmost pairs of positive and negative statuses are employed to facilitate maximum energy exchange between cell capacitors. The number of positive and negative pairs is obtained from (6.7), and the zero-state cell number is either zero or one as shown in (6.8). The summation of these cell numbers in difference states is equal to N, viz., (6.9).

$$N_{on} = \text{round}(v_{xy} / \text{V}_{\text{cell}}) \in \{-N, N\} \tag{6.6}$$

$$N_p = N_n = \text{floor}[\tfrac{1}{2}(N - |N_{on}|)] \tag{6.7}$$

$$N_0 = \text{mod}[\tfrac{1}{2}(N - |N_{on}|)] \tag{6.8}$$

$$|N_{on}| + N_p + N_n + N_0 = N \tag{6.9}$$

Considering the load current polarity during intermediate voltage levels, the three voltage states of each FB cell are exploited to maintain the desired output voltage and achieve energy balance by adjusting the behavioural polarities of the cells in the conduction path. With proper arrangement, the cell capacitor voltage errors can be limited to a marginal range via charging or discharging processes with the AC side. When the staircase waveform approaches the peak of $\pm \text{V}_{\text{dc}}$, energy is exchanged

between the FB cells and DC-link through the DC side inductor. In this way, the net active power exchange over one fundamental period for the FB-CL is compensated to zero. The generalized algorithm for cell capacitor voltage balancing of the CTFB-HMC is summarized as follows:

- At the beginning of each sampling period, the capacitor voltages of N cells are sorted in ascending order as in (6.10). The input data $\mathbf{V_{CN}}$ contains the sampled instantaneous cell voltage values; while $\mathbf{I_xA}$ and $\mathbf{V_cA}$ are the vectors of the index and value for each cell capacitor voltage after ascending sort.

$$[\mathbf{I_xA}, \mathbf{V_cA}] = \text{sort}(\mathbf{V_{CN}}, \text{'ascend'}) \tag{6.10}$$

- Based on the voltage reference value in each sampling period, the number of cells with different states $\{N_{on}, N_p, N_n, N_0\}$ are obtained from (6.6) to (6.8).
- Considering the load current polarity and the cell voltage sorting results, the capacitors with smaller values are assigned to be charged by the AC side current while the higher ones should be discharged. If $\mathbf{S_x}[N]$ is the array of switching states for all the FB cells and each element has possible values of {'+1', '-1', '0'} to identify the polarity, the generic code for cell voltage balancing can be interpreted in Fig. 6-8(a). An illustrative example with 11 cells per chain-link is presented in Fig. 6-8(b), where the numbers of cells inserted with different polarities (positive, negative and bypassed) are displayed.

$N_{on} \geq 0, I_L \geq 0$

for $i = 1 : N$
  if $(i \leq N_n)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "-1"$
  elseif $(i \leq N_n + N_0)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "0"$
  else
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "+1"$

$N_{on} \geq 0, I_L < 0$

for $i = 1 : N$
  if $(i \leq N_{on} + N_p)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "+1"$
  elseif $(i \leq N_{on} + N_p + N_0)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "0"$
  else
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "-1"$

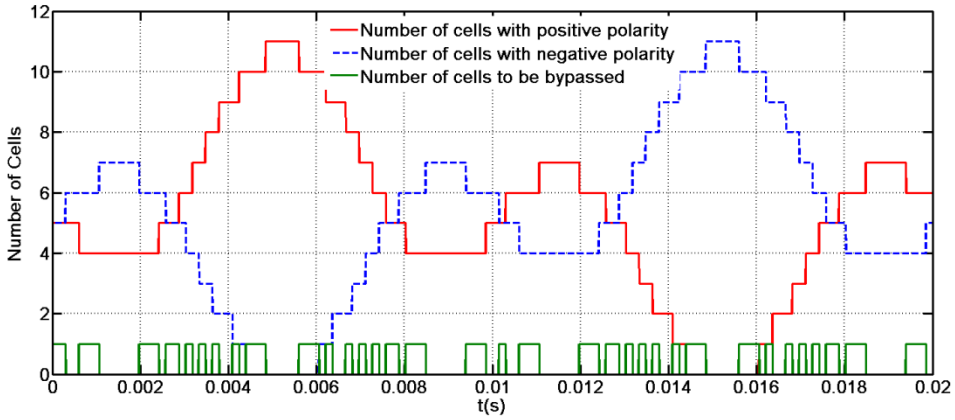
$N_{on} < 0, I_L \geq 0$

for $i = 1 : N$
  if $(i \leq -N_{on} + N_n)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "-1"$
  elseif $(i \leq -N_{on} + N_n + N_0)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "0"$
  else
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "+1"$

$N_{on} < 0, I_L < 0$

for $i = 1 : N$
  if $(i \leq N_p)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "+1"$
  elseif $(i \leq N_p + N_0)$
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "0"$
  else
    $\mathbf{S}_x[\mathrm{I}_x\mathrm{A}[i]] = "-1"$

(a)



(b)

Fig. 6-8. The energy balancing scheme: (a) generic code for CTFB converter cell voltage balancing and (b) number of cells in each state over a fundamental period (11 cells).

6.4 Converter Hardware Dimensioning

The FB-CL inserts a variable number of cell capacitors into the power path according to the predefined modulating signal. This modulating signal is derived from the voltage reference in (6.2). In order to simplify the analysis and estimation processes for the chain-link component interaction and passive device sizing, the following prioritized assumptions are made:

- Sufficient FB cells are located in the chain-link to ensure enough resolution for each cell voltage over the full AC side voltage so that a direct reference tracking method can be used for voltage synthesis.
- Sufficiently high sampling frequency is used by the controller so that the each cell status can be recognized and changed effectively; also, the reference signal in (6.2) is proportional to the effective duty cycle for the FB-CL.
- All internal losses due to the non-ideal parameters are neglected to establish a lossless system model.

With these assumptions and based on (6.2), the equivalent duty ratio of the duration when FB-CL cell capacitors are inserted into the conduction path linearly changes with the voltage reference and is calculated by (6.11).

$$d_{eq} = m\cos(\omega t + \theta_0) + (1-m)\cdot\cos[3(\omega t + \theta_0)] \tag{6.11}$$

Since in a typical three-phase system, the triplen components do not contribute to the current, the AC side line current is pure fundamental and expressed in (6.12), where I_m is the line current amplitude and θ_1 is the phase-shift angle relative to the PLL reference. The effective current for cell capacitor charging or discharging can be achieved by (6.13).

$$i_L = I_m\cos(\omega t + \theta_1) \tag{6.12}$$

$$\begin{aligned} i_c &= d_{eq}\cdot i_L = I_m\cdot\{m\cos(\omega t+\theta_0)+(1-m)\cos[3(\omega t+\theta_0)]\}\cdot\cos(\omega t+\theta_1) \\ &= \frac{I_m}{2}\cdot[m\cos(\theta_0-\theta_1)+m\cos(2\omega t+\theta_0+\theta_1)+(1-m)\cos(2\omega t+3\theta_0-\theta_1) \\ &\quad +(1-m)\cos(4\omega t+3\theta_0+\theta_1)] \end{aligned} \tag{6.13}$$

Consequently, the averaged voltage fluctuation of each cell capacitor is obtained by manipulation of (6.14), since the cell capacitors are assumed to be balanced.

$$v_c = -\frac{1}{C_{ce}/N}\int i_c dt\cdot\frac{1}{N} = -\frac{1}{C_{ce}}\int i_c dt \tag{6.14}$$

From (6.11) to (6.14), the expanded expression for cell capacitor voltage is shown in (6.15) with a constant term T_c. The function of cell capacitor voltage v_c of (6.15) should be discontinuous in the time-domain due to step changes of the equivalent topology at conduction instances of the main directing switches. From (6.11), when d_{eq}=1 or d_{eq}=-1, the instantaneous value of the FB-CL voltage v_{xy} reaches $\pm V_{dc}$ and the main switches start to conduct and transfer energy between the DC-link and FB-

CL. Thus, the cell capacitor voltage values at these points are both clamped to V_{dc}/N, then, substituting these relations into (6.15), (6.16) is obtained.

$$\begin{aligned} v_c = &-\frac{I_m}{2C_{ce}}[\frac{1-m}{4\omega}\sin(4\omega t+3\theta_0+\theta_1)+\frac{1-m}{2\omega}\sin(2\omega t+3\theta_0-\theta_1) \\ &+\frac{m}{2\omega}\sin(2\omega t+\theta_0+\theta_1)+m\cos(\theta_0-\theta_1)t]+T_c \end{aligned} \tag{6.15}$$

$$\begin{cases} \dfrac{V_{dc}}{N} = -\dfrac{I_m}{2C_{ce}}[\dfrac{1-3m}{4\omega}\sin(\theta_0-\theta_1)+\dfrac{2k\pi-\theta_0}{\omega}m\cos(\theta_0-\theta_1)]+T_c^+ \\ \dfrac{V_{dc}}{N} = -\dfrac{I_m}{2C_{ce}}[\dfrac{1-3m}{4\omega}\sin(\theta_0-\theta_1)+\dfrac{(2k+1)\pi-\theta_0}{\omega}m\cos(\theta_0-\theta_1)]+T_c^- \end{cases} \tag{6.16}$$

By solving for $\{T_c^+, T_c^-\}$ from (6.16), the final equation for v_c can be derived as (6.17) with definitions in (6.18). Expression (6.17) becomes continuous only at the case of $\theta_0=\theta_1$ when the AC power factor is zero and the converter exchanges zero active power with both the AC and DC sides, which is in accordance with the energy conservation law for converter operation.

$$v_c = \begin{cases} \dfrac{V_{dc}}{N}-\dfrac{I_m}{2C_{ce}}[A_W(t)+B_W(t)+C_W+\dfrac{\pi}{2\omega}m\cos(\theta_0-\theta_1)] \\ \qquad (\omega t+\theta_0\in[2k\pi,(2k+1)\pi],k\in\mathbb{Z}) \\ \dfrac{V_{dc}}{N}-\dfrac{I_m}{2C_{ce}}[A_W(t)+B_W(t)+C_W-\dfrac{\pi}{2\omega}m\cos(\theta_0-\theta_1)] \\ \qquad (\omega t+\theta_0\in[(2k+1)\pi,(2k+2)\pi],k\in\mathbb{Z}) \end{cases} \tag{6.17}$$

$$\begin{cases} A_W(t) = \dfrac{1-m}{4\omega}\sin(4\omega t+3\theta_0+\theta_1)+\dfrac{1-m}{2\omega}\sin(2\omega t+3\theta_0-\theta_1) \\ B_W(t) = \dfrac{m}{2\omega}\sin(2\omega t+\theta_0+\theta_1)+m\cos(\theta_0-\theta_1)t \\ C_W = -\dfrac{1-3m}{4\omega}\sin(\theta_0-\theta_1)-\dfrac{(4k+1)\pi-2\theta_0}{2\omega}m\cos(\theta_0-\theta_1) \end{cases} \tag{6.18}$$

Based on (6.17), the magnitude percentage of the cell capacitor voltage ripple over its nominal DC value (V_{dc}/N) is generally determined by the DC-link voltage level (V_{dc}), number of cells in the FB-CL (N), AC side current amplitude (I_m) and the cell capacitance (C_{ce}). For CTFB converter design with known V_{dc} and I_m, N is selected according to the rated voltage of the power switching devices and the value of the C_{ce} is calculated to fulfil the demanded voltage ripple percentage. In (6.17), the cell capacitor voltage of CTFB converter oscillates around the nominal DC value without a fundamental frequency component for any power factor in contrast to HB-MMC.

Recall (6.17) and (6.18), the total chain-link cell capacitor voltage deviation from V_{dc} before turn-on of directing switches (at the discontinuous points) is given by (6.19), where τ is the radian duration in one fundamental period that the directing switches are enabled. V_{err} can be either positive or negative depending on the sign of the term $\cos(\theta_0-\theta_1)$ (the direction of active power flow); and its absolute value is mainly determined by the power factor and directing switch conduction period (τ, radian). In low power factor conditions, the voltage error is almost zero and minimal current is exchanged between the DC-link and cell capacitors; while at high power factors, the longer the directing switches are enabled, the smaller the voltage deviation and charging/discharging current. Besides, the magnitude of V_{err} determines the rising slope of inrush current when the directing switches are turned on, and the incremental current during charging time can be estimated by (6.20), where L_{dc} denotes the current limiting DC side inductance. Based on this equation and the rated pulse current for the selected power semiconductor devices, an optimized value of DC side inductance can be obtained.

$$V_{err} = \frac{(\pi-\tau)NI_m}{2\omega C_{ce}} m\cos(\theta_0-\theta_1) \tag{6.19}$$

$$\Delta I_{dc} = \frac{\tau\,|V_{err}|}{\omega L_{dc}} = \frac{m\tau(\pi-\tau)NI_m}{2\omega^2 L_{dc}C_{ce}}\,|\cos(\theta_0-\theta_1)| \tag{6.20}$$

The net energy exchange from the FB-CL in the time-domain is derived and shown in (6.21). Based on (6.17), due to the incorporation of the energy exchange with DC side at certain instances, E_{CL} over one fundamental period is zero as in (6.22). In further, the root-mean-square (RMS) value of E_{CL} can be calculated by (6.23), which represents the total energy exchange between the chain-link capacitors and the AC side when directing switches are disabled.

$$E_{CL}(t) = \int i_L \cdot v_{xy}\,dt = V_{dc}\int i_L \cdot d_{eq}\,dt = V_{dc}\int i_c\,dt = C_{ce}V_{dc}v_c \tag{6.21}$$

$$E_{CL}(t)\Big|_0^T = 0 \tag{6.22}$$

$$RMS[E_{CL}(t)]\Big|_0^T = 2C_{ce}V_{dc}v_c\Big|_0^{T/2} = \frac{(\pi-\tau)mV_{dc}I_m\,|\cos(\theta_0-\theta_1)|}{\omega} \tag{6.23}$$

6.5 Comparison with Typical MMC and HMC Topologies

The operating principle, energy balancing algorithm and main element sizing of the CTFB-HMC have been discussed in previous sections. To reveal certain aspects of its behaviour, a comparative study which involves the CTFB-HMC as well as typical MMC and HMC topologies is presented in this section.

On the assumption of fixed apparent power, fixed AC side voltage (thus, same line current) and same type of power switching devices (voltage and current ratings) for each candidate, the converters including CTFB-HMC, HB-MMC, FB-MMC, AAMC are investigated in Table 6-1, where the number of devices in the conduction path in this case (fixed line current) reflects the percentage of conduction losses. Based on Table 6-1, following summary can be made:

- Compared to HB-MMC, the proposed CTFB topology requires half DC-link voltage per unit power (thus, doubled power density); also, it uses a quarter number of cell capacitors (smaller footprint) to synthesize same number of voltage levels on AC side without discount in efficiency.
- Similar conclusions hold between the CTFB-HMC and FB-MMC except that the latter employs twice the number of total device for reverse-blocking ability but at the expense of doubled conduction losses.
- The proposed CTFB-HMC also contributes lower conduction losses, doubled power density and fewer cell number than the AAMC.
- The main limitation of the CTFB-HMC (as with the HB-MMC) is the lack of reverse-blocking capability compared with other converters such as FB-MMC and AAMC. However, this is not critical for the applications where there is no long distance DC cable such as FACTS devices.

Table 6-1. Comparisons between CTFB-HMC and other typical multilevel converters.

The same power, AC side voltage/current and same type power switches for each candidate						
Converter type	DC-link required	Cell number per phase	Voltage level number	Total devices per phase	Conduction path devices per phase	Efficiency
CTFB-HMC	V_{dc}	N	$2N+1$	$8N$	$2N$	High
HB-MMC	$2V_{dc}$	$4N$	$2N+1$	$8N$	$2N$	High
FB-MMC	$2V_{dc}$	$4N$	$2N+1$	$16N$	$4N$	Low
AAMC	$2V_{dc}$	$2N$	$2N+1$	$10N$	$3N$	Moderate

To quantitatively show the efficiency performance for all these topologies, the loss calculation for each converter is exploited. Since the HMC directing switches usually operate at low frequency with multi-step voltage transitions, the switching losses for multilevel converters are much smaller than conduction losses [23, 24]. Therefore, to simplify the derivation, conduction losses are adopted for efficiency comparison and harmonic components in the arm current are neglected.

Assuming the insulated gate bipolar transistor (IGBT) modules are used to build each converter, the total on-state losses are the summation of IGBT and diode losses as in (6.24). The forward voltage drop of IGBT and its anti-parallel diode are calculated from (6.25), where $\{V_{CE}, V_D\}$ are the voltage drop in conduction mode; $\{I_C, I_D\}$ are the instantaneous value of the device current; $\{V_{CEO}, V_{DO}\}$ represent the device threshold voltages; $\{R_V, R_D\}$ define the equivalent resistances for IGBT and diode respectively, and can be further obtained by (6.26) according to the nominal device operation points $\{V_{CEN}, I_{CN}\}$ and $\{V_{DN}, I_{DN}\}$ from the manufacturer datasheet.

$$P_{Loss} = P_{IGBT} + P_D \tag{6.24}$$

$$\begin{cases} V_{CE} = R_V \cdot I_C + V_{CEO} \\ V_D = R_D \cdot I_D + V_{DO} \end{cases} \tag{6.25}$$

$$\begin{cases} R_V = \dfrac{V_{CEN} - V_{CEO}}{I_{CN}} \\ R_D = \dfrac{V_{DN} - V_{DO}}{I_{DN}} \end{cases} \tag{6.26}$$

The conduction loss calculation processes for HB-MMC and FB-MMC are the same since only unipolar cell voltage state is utilized in the latter. The upper and lower arm currents $\{i^+, i^-\}$ in MMC are continuous and can be expressed by (6.27), where I_d is the DC side current per phase from the DC-link to the AC side.

$$\begin{cases} i^+ = I_d + \frac{1}{2} i_L = I_d + \frac{1}{2} I_m \cos(\omega t + \theta_1) \\ i^- = I_d - \frac{1}{2} i_L = I_d - \frac{1}{2} I_m \cos(\omega t + \theta_1) \end{cases} \tag{6.27}$$

Based on this definition, the positive duration of each arm current flows through its IGBTs, while the negative arm current passes the diodes. Based on the law of energy conservation, (6.28) can be obtained, where φ is the power factor angle.

$$I_d = \frac{1}{4} m I_m \cos\varphi \tag{6.28}$$

If the conduction angles for IGBTs and diodes are denoted in (6.29), due to the symmetrical operation of upper and lower arms, the total IGBT and diode losses per phase in the MMC converters can be expressed by (6.30), where F_{con} is the device number in the conduction path. From Table 6-1, for HB-MMC, F_{con} equals to $2N$; and F_{con} is $4N$ in FB-MMC.

$$\begin{cases} \alpha = \cos^{-1}(\dfrac{-2I_d}{I_m}) = \cos^{-1}(-\tfrac{1}{2} m\cos\varphi) \\ \beta = \cos^{-1}(\dfrac{2I_d}{I_m}) = \cos^{-1}(\tfrac{1}{2} m\cos\varphi) \end{cases} \tag{6.29}$$

$$\begin{cases} P_{IGBT} = 2\times\dfrac{1}{2\pi}\displaystyle\int_{-\theta_1-\alpha}^{-\theta_1+\alpha}(R_V\cdot i^{+}+V_{CEO})i^{+}F_{con}d\omega t \\ P_D = 2\times\dfrac{1}{2\pi}\displaystyle\int_{-\theta_1-\beta}^{-\theta_1+\beta}(-R_D\cdot i^{-}+V_{DO})(-i^{-})F_{con}d\omega t \end{cases} \tag{6.30}$$

Substituting (6.28) into (6.30), the final equations for device losses per phase of MMC type topologies are shown in (6.31).

$$\begin{cases} P_{IGBT} = \dfrac{I_m F_{con}}{16\pi}[(2R_V I_m m^2\cos\varphi^2 + 4R_V I_m + 8m\cos\varphi V_{CEO})\alpha \\ \qquad\qquad + (3R_V m I_m\cos\varphi + 8V_{CEO})\sqrt{4-m^2\cos\varphi^2}\,] \\ P_D = \dfrac{I_m F_{con}}{16\pi}[(2R_D I_m m^2\cos\varphi^2 + 4R_D I_m - 8m\cos\varphi V_{DO})\beta \\ \qquad\qquad - (3R_D m I_m\cos\varphi - 8V_{DO})\sqrt{4-m^2\cos\varphi^2}\,] \end{cases} \tag{6.31}$$

In the AAMC topology, the FB cells still operate in unipolar mode and the AC side current alternatively flows through the upper and lower arms. Thus, the total conduction losses for IGBT and diode in each phase of the AAMC can be derived from (6.32), and simplified to be (6.33). Recalled Table 6-1, the total number of devices in the conduction path per phase for AAMC is F_{con}=3N.

$$\begin{cases} P_{IGBT} = 2\times\dfrac{1}{2\pi}\displaystyle\int_{-\theta_1-\pi/2}^{-\theta_1+\pi/2-\varphi}(R_V\cdot i_L+V_{CEO})i_L F_{con}d\omega t \\ P_D = 2\times\dfrac{1}{2\pi}\displaystyle\int_{-\theta_1+\pi/2-\varphi}^{-\theta_1+\pi/2}(R_D\cdot i_L+V_{DO})i_L F_{con}d\omega t \end{cases} \tag{6.32}$$

$$\begin{cases} P_{IGBT} = \dfrac{I_m F_{con}}{2\pi}[R_V\cdot I_m(\pi-\varphi+\sin\varphi\cos\varphi)+2V_{CEO}(1+\cos\varphi)] \\ P_D = \dfrac{I_m F_{con}}{2\pi}[R_D\cdot I_m(\varphi-\sin\varphi\cos\varphi)+2V_{DO}(1-\cos\varphi)] \end{cases} \tag{6.33}$$

For the proposed CTFB-HMC, the FB cells are utilized to generate bipolar voltage. Thus, although the total amount of device in conduction path is constant, the number of IGBTs or diodes that are used to carry current becomes continuously time-variant according to the modulation reference. Since the line current is pure fundamental in the three-phase CTFB-HMC, the injected 3rd order modulating signal has marginal influence on the conduction losses. Therefore, with the AC side current defined in (6.12), (6.34) represents the effective fundamental reference signal for the proposed CTFB-HMC. Recall its voltage balancing strategy in Fig. 6-8, during the half cycle with positive chain-link current, the numbers of on-state IGBT and diode are calculated by the first and second equations in (6.35) respectively, where the total number of devices in conduction path per phase is $F_{con}=2N$ in Table 6-1. Considering the symmetrical operation between the two half cycles with different current polarities, the conduction losses of IGBT and diode created by the energy exchange between DC and AC sides in one phase of the CTFB topology can be achieved by (6.36), and in further to be (6.37).

$$M_{eq} = m\cos(\omega t + \theta_0) \tag{6.34}$$

$$\begin{cases} n_T = \tfrac{1}{2}(1+M_{eq})\cdot F_{con} \\ n_D = \tfrac{1}{2}(1-M_{eq})\cdot F_{con} \end{cases} \tag{6.35}$$

$$\begin{cases} P_{IGBT} = 2\times\dfrac{1}{2\pi}\displaystyle\int_{-\theta_1-\pi/2}^{-\theta_1+\pi/2}(R_V\cdot i_L + V_{CEO})i_L n_T d\omega t \\ P_D = 2\times\dfrac{1}{2\pi}\displaystyle\int_{-\theta_1-\pi/2}^{-\theta_1+\pi/2}(R_D\cdot i_L + V_{DO})i_L n_D d\omega t \end{cases} \tag{6.36}$$

$$\begin{cases} P_{IGBT} = \dfrac{I_m F_{con}}{12\pi}[3\pi R_V\cdot I_m + 12V_{CEO} + (8R_V\cdot I_m + 3\pi V_{CEO})m\cos\varphi] \\ P_D = \dfrac{I_m F_{con}}{12\pi}[3\pi R_D\cdot I_m + 12V_{DO} - (8R_D\cdot I_m + 3\pi V_{DO})m\cos\varphi] \end{cases} \tag{6.37}$$

Provided the power factor is not zero, the cell voltage will deviate from the rated value, causing energy exchange between the DC-link and the chain-link capacitors. Due to the use of the DC side inductor, the current from the DC-link can be assumed constant during the directing switch enabled period ($T_\Delta=\tau/\omega$). For energy balance, (6.38) is fulfilled; and from (6.19), is simplified to (6.39). Then, the power path conduction losses for energy exchange between the DC-link and the chain-link in one phase can be estimated by (6.40), where it is concluded that:

- In low power factor conditions, P_{ch} is small due to the marginal voltage errors between the DC-link and the chain-link capacitors.
- In high power factor conditions, the directing switch increased enable-time (through the modulation method in Fig. 6-5) reduces power losses due to the reduced voltage error and RMS current.

$$\frac{1}{2}\frac{C_{ce}}{N}[\mathrm{V_{dc}}^2-(\mathrm{V_{dc}}-\mathrm{V_{err}})^2]\approx I_{dc}(\mathrm{V_{dc}}-\tfrac{1}{2}\mathrm{V_{err}})T_{\Delta} \tag{6.38}$$

$$\begin{cases} I_{dc}T_{\Delta}=\dfrac{\mathrm{V_{err}}C_{ce}}{N}=\dfrac{(\pi-\tau)I_m}{2\omega}m\cos(\theta_0-\theta_1) \\ I_{dc}=\dfrac{(\pi-\tau)I_m}{2\tau}m\cos(\theta_0-\theta_1) \end{cases} \tag{6.39}$$

$$P_{ch}=\frac{\omega}{\pi}F_{con}\left|I_{dc}\right|T_{\Delta}[(R_V\cdot\left|I_{dc}\right|+V_{CEO})+(R_D\cdot\left|I_{dc}\right|+V_{DO})] \tag{6.40}$$

Therefore, the unified expression for the CTFB-HMC per phase conduction losses under arbitrary power factor and modulation scheme is obtained using (6.41).

$$P_{con}=P_{IGBT}+P_D+P_{ch} \tag{6.41}$$

As explained previously, the proposed CTFB-HMC topology has better efficiency performance than FB-MMC and AAMC; and in further, it should be virtually the same as HB-MMC for low power factor applications such as the reactive power controllers and machine drives by evaluation the number of devices in conduction path. In the proposed converter, the chain-link current is pure AC component, which differs from that in HB-MMC.

Table 6-2. Total conduction losses comparison between CTFB-HMC and other typical multilevel converter topologies.

Three-phase apparent power rating 687MVA and AC voltage 300kV (line-to-line RMS), N=135, V_{dc}=300kV.			
Converter type	Three-phase total conduction losses		
	P=600MW, Q=0	P=0, Q=600MVar	P=600MW, Q=300MVar (lagging)
CTFB-HMC	4.52MW (0.75%)*	2.72MW (0.45%)	4.93MW (0.82%)*
HB-MMC	2.69MW (0.45%)	2.34MW (0.39%)	2.84MW (0.47%)
FB-MMC	5.38MW (0.90%)	4.68MW (0.78%)	5.69MW (0.95%)
AAMC	4.43MW (0.74%)	4.43MW (0.74%)	4.78MW (0.80%)

* Data is achieved with modified triplen injection modulation in Fig. 6-5 for active power transfer.

Based on the 4.5kV IGBT T1800GB45A parameters, the calculated conduction losses for HB-MMC, FB-MMC and AAMC as well as the simulated result for CTFB-HMC are summarized in Table 6-2. These results assume a 687MVA three-phase power rating and a line-to-line RMS 300kV AC side for all the converters; plus the DC link voltage of the proposed CTFB converter V_{dc} is set to 300kV and N equals 135, for a maximum voltage stress of 2.25kV (50% of full rating) for the employed IGBT. This means the other converters must use a 600kV DC-link voltage and 270 cells in each arm (540 per phase) to transfer the same power, as explained in Table 6-1. From Table 6-2, for low power factor conditions, the proposed converter has a similar efficiency performance as the HB-MMC with sinusoidal modulation. But for high power factor applications, with the modified modulation scheme in Fig. 6-5, the efficiency of the CTFB-HMC is virtually the same as the AAMC. Thus, the CTFB is more competitive for low power factor applications, such as FACTS devices and power drives. The FB-MMC has the highest on-state losses due to a higher number of power devices in the conduction paths.

6.6 Control System Design

The *d-q* frame control diagram of the proposed three-phase CTFB-HMC under grid-tied mode is summarized in Fig. 6-9. With this synchronous-reference-frame (SRF) method, the critical variables become time-invariant. Thus, the proportional-integral (PI) controller is sufficient for zero-steady-state reference tracking.

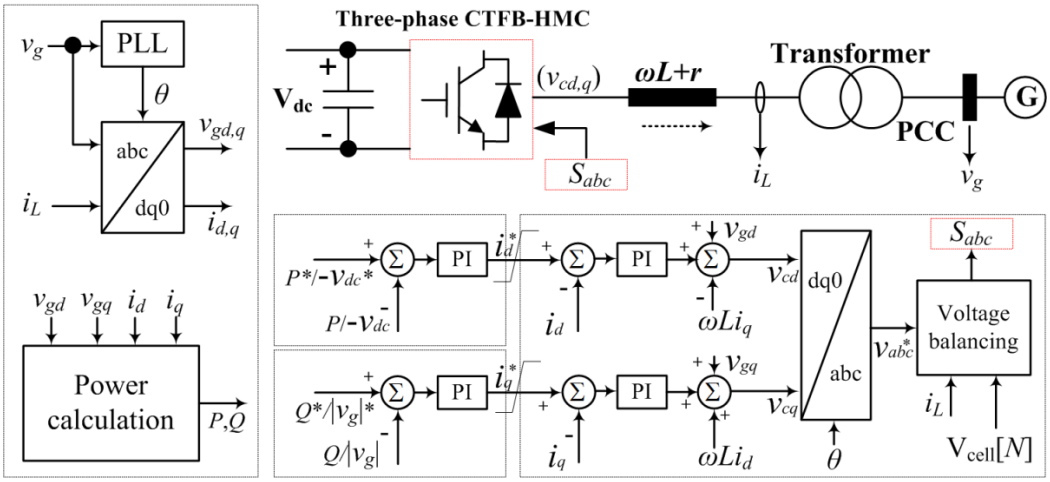


Fig. 6-9. The control strategy for grid-connected three-phase CTFB-HMC in *d-q* frame.

If $v_{cd,q}$ represents the output pole voltage of the CTFB converter, its *d-q* frame AC side differential equations are obtained in (6.42), where i_{dq} is the AC side line current;

$v_{gd,q}$ is the voltage at the point-of-common-coupling (PCC); L and r represent the parameters of interfacing reactor.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = -\frac{r}{L}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega\begin{bmatrix} i_q \\ -i_d \end{bmatrix} + \frac{1}{L}\begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_{gd} \\ v_{gq} \end{bmatrix} \tag{6.42}$$

The reference signal for converter output voltage is set according to (6.43), where $\gamma_{d,q}$ is the output of the inner layer current PI controller. With the voltage and current polarity defined in Fig. 6-9, the outer layer controllers that are used to generate the reference signals for i_d and i_q can be expressed by (6.44) and (6.45) respectively.

$$\begin{cases} v_{cd}^* = \gamma_d + v_{gd} - \omega L i_q \\ v_{cq}^* = \gamma_q + v_{gq} + \omega L i_d \end{cases} \tag{6.43}$$

$$\begin{aligned} & i_d^* = -[k_{dcp}(v_{dc}^* - v_{dc}) + k_{dci}\int (v_{dc}^* - v_{dc})dt] \\ or \quad & i_d^* = k_{Pp}(P^* - P) + k_{Pi}\int (P^* - P)dt \end{aligned} \tag{6.44}$$

$$\begin{aligned} & i_q^* = k_{acp}(|v_g^*| - |v_g|) + k_{aci}\int (|v_g^*| - |v_g|)dt \\ or \quad & i_q^* = k_{Qp}(Q^* - Q) + k_{Qi}\int (Q^* - Q)dt \end{aligned} \tag{6.45}$$

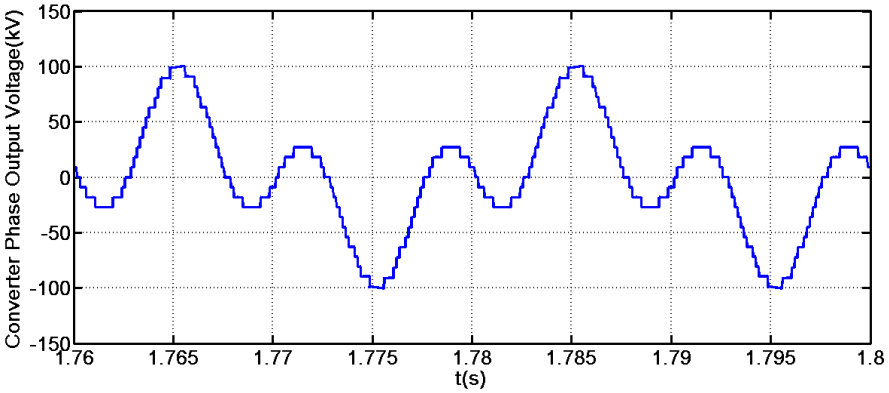
For the current controller, DC voltage controller and active power controller designs, the PI parameters can be arranged by state space analysis that incorporates the local converter feedback and feedforward as presented in [25]. In reality, due to the uncertainty and randomness of some grid parameters, the tuning of reactive power and PCC voltage PI controllers are usually achieved by a trial-and-error indexing method to find the proper gain combinations for the best time domain response.

6.7 Simulation Analysis

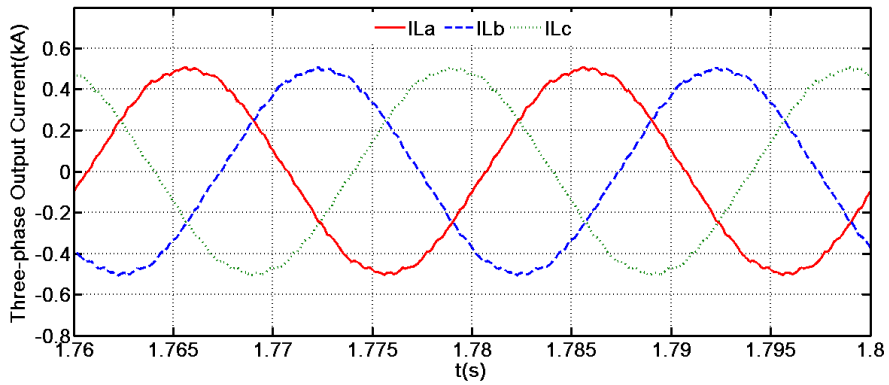
6.7.1 Three-phase CTFB-HMC with 11 Cells in Staircase Mode

A three-phase CTFB-HMC with 11 cells in the chain-link and staircase modulation is tested in Matlab/Simulink with following specifications: DC-link voltage: 100kV; power rating: 150MVA, cell capacitance: 2.2mF; current limiting inductance: 5mH. Using the modulation scheme of Fig. 6-4 and energy balancing algorithm in Fig. 6-8, the performance under unity power factor condition is evaluated. In Fig. 6-10(a), the phase "*a*" output voltage waveform that contains triplen component is displayed. Since these triplen components will be cancelled in line-to-line voltage, three-phase output current waveform in dominant fundamental frequency is obtained as in Fig. 6-10(b). Fig. 6-10(c) shows the chain-link current of phase "*a*", where the inrush

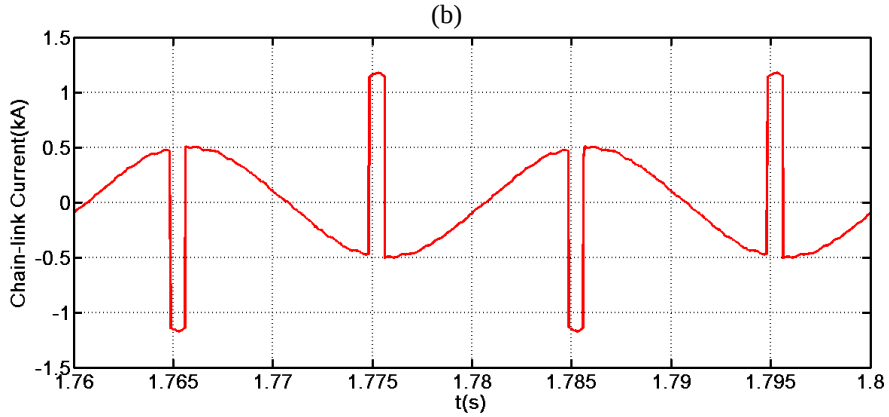
current for energy exchange between DC-link and cell capacitors is limited to an acceptable range. The cell capacitor voltage balancing results are demonstrated in Fig. 6-10(d).



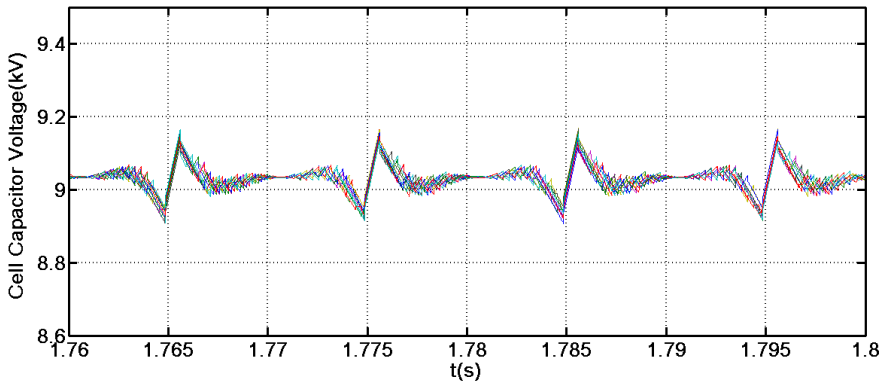
(a)



(b)



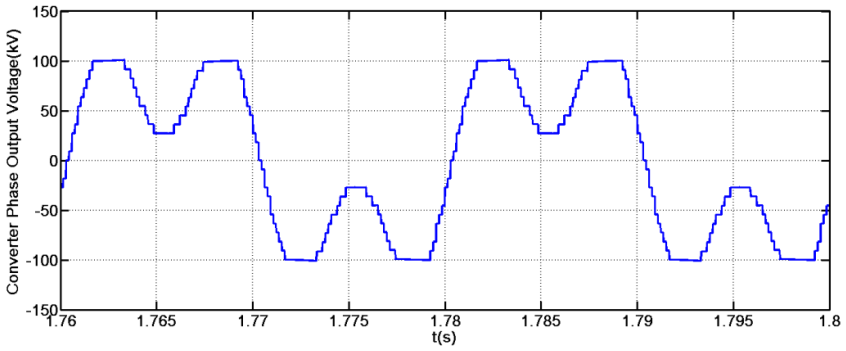
(c)



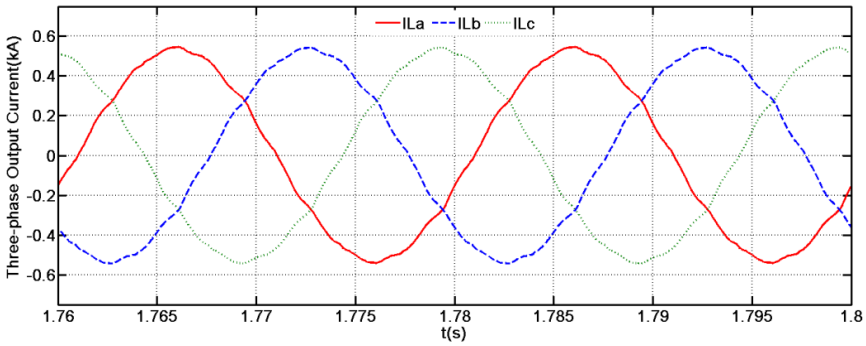
(d)

Fig. 6-10. Waveforms for unity power factor condition with sinusoidal modulation: (a) converter phase '*a*' output voltage with triplen component; (b) three-phase line current in fundamental frequency; (c) chain-link current of phase '*a*'; and (d) cell capacitor voltages.

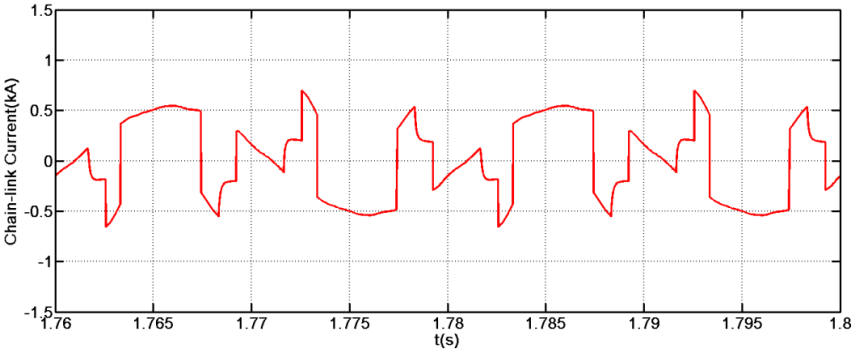
In Fig. 6-10, for high power factor conditions, the energy exchange time between the chain-link and the DC-link is short and is concentrated in the voltage peak area if the modulation scheme of Fig. 6-4 is employed. This effect increases the power losses and requires large DC side inductance to limit any inrush current. As seen in Fig. 6-5, the modified triplen injection modulation is assessed in another simulation. By extending the voltage level clamping duration, the cell capacitor voltage deviation and inrush current can both be reduced as in Fig. 6-11(c) and (d) compared to the results of Fig. 6-10(c) and (d). With the modified triplen injection modulation, a small amount of low order harmonics emerge in the phase voltage waveform of Fig. 6-11(a) [22]. In this simulation, a tuned-filter for the 7^{th} order harmonic is used to limit the current distortion, where the total harmonic distortion (THD) of line current in Fig. 6-11(b) is 2.1%. To further improve the power quality, a double-tuned filter with minimal reactive power consumption can be investigated [26, 27]. Also, with the modulation scheme in Fig. 6-5, the DC side current waveforms, such as the inductor current and the circulating current for high power factor condition, are displayed in Fig. 6-11(e) and (f) respectively.



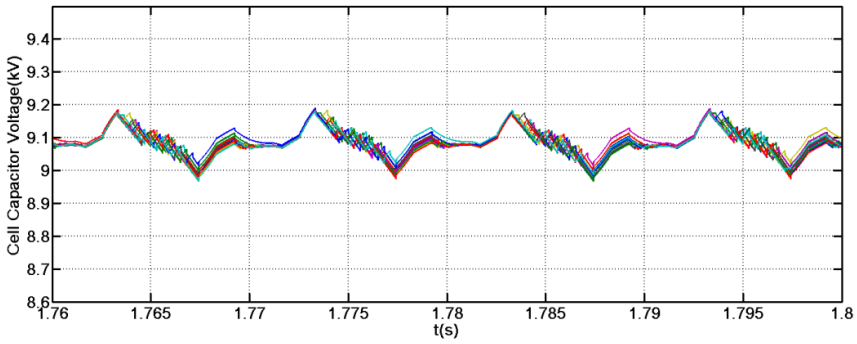
(a)


ILa
ILb
ILc
Three-phase Output Current(kA)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

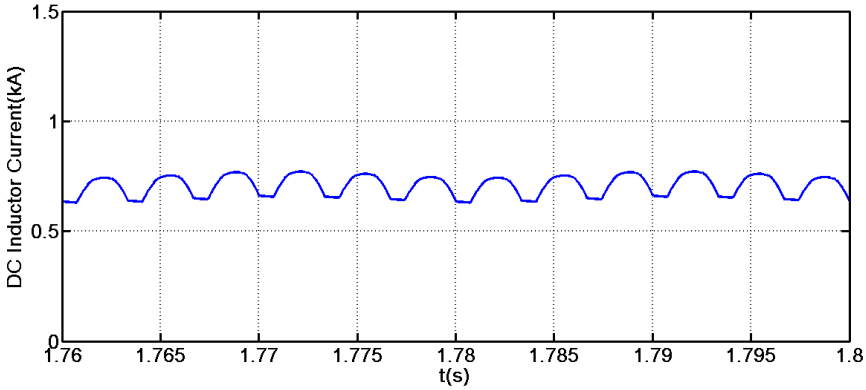
(b)


Chain-link Current(kA)
1.5
1
0.5
0
-0.5
-1
-1.5
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

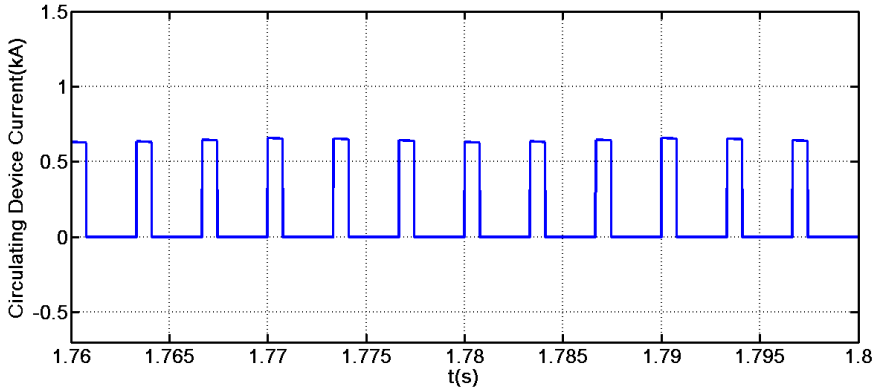
(c)


Cell Capacitor Voltage(kV)
9.4
9.3
9.2
9.1
9
8.9
8.8
8.7
8.6
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

(d)


DC Inductor Current(kA)
1.5
1
0.5
0
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

(e)

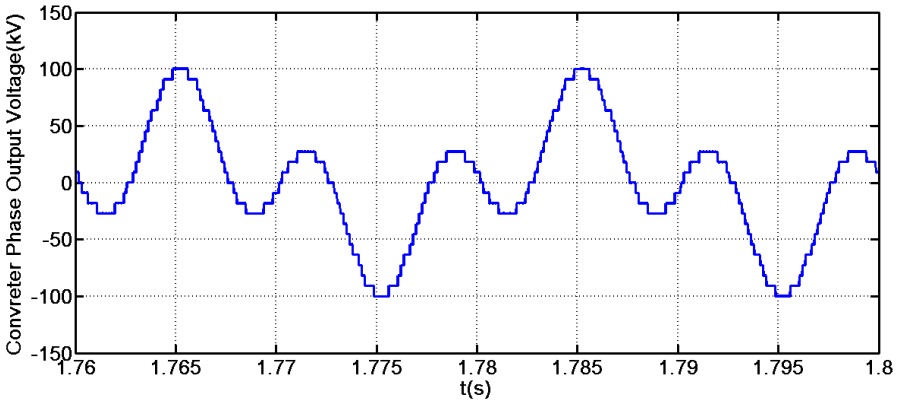


(f)

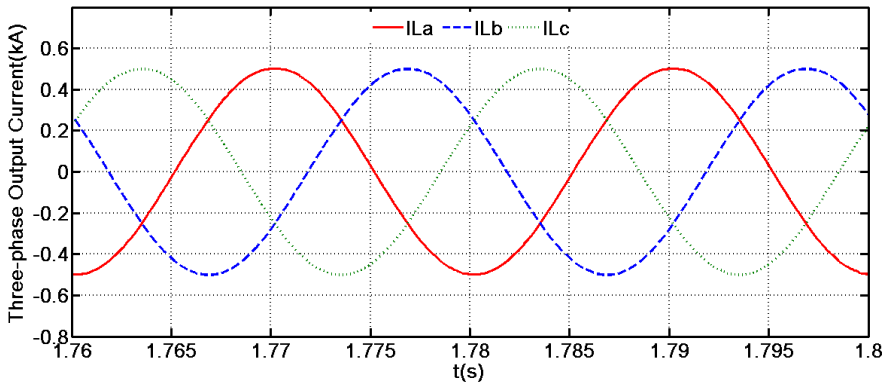
Fig. 6-11. Waveforms for unity power factor with modified triplen injection modulation: (a) converter phase '*a*' output voltage with triplen component; (b) three-phase line current in fundamental frequency; (c) chain-link current of phase '*a*'; (d) cell capacitor voltage; (e) DC side inductance currents; and (f) circulating valve device current.

If the power factor is set to about zero and the sinusoidal modulation in Fig. 6-4 is employed, the phase output voltage and line current quality are shown in Fig. 6-12(a) and (b). The inrush current in this condition is near zero since the active power exchange is minimal, see Fig. 6-12(c). Thus, from Fig. 6-12(d), the cell capacitor voltage ripple is also decreased. In low power factor conditions, the DC side current is insignificant relative to the AC side current as shown in Fig. 6-12(e) and (f). In the proposed CTFB topology, the DC inductor is located in the DC side and shared by multiple phases, which reduces the total weight and cost compared to conventional MMCs.

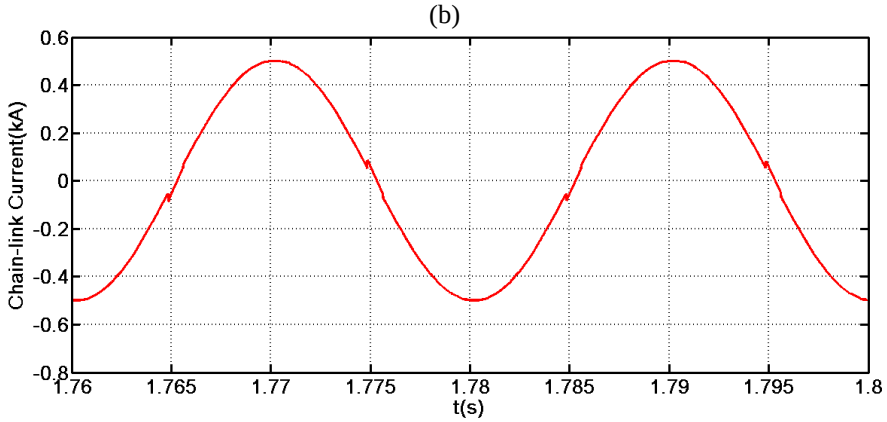
From these two cases that cover the full power factor variation range, it is concluded that, with proper modulation schemes, the proposed CTFB-HMC is able to maintain energy balance of its cell capacitors, while synthesizing the desired voltage under various operational conditions.



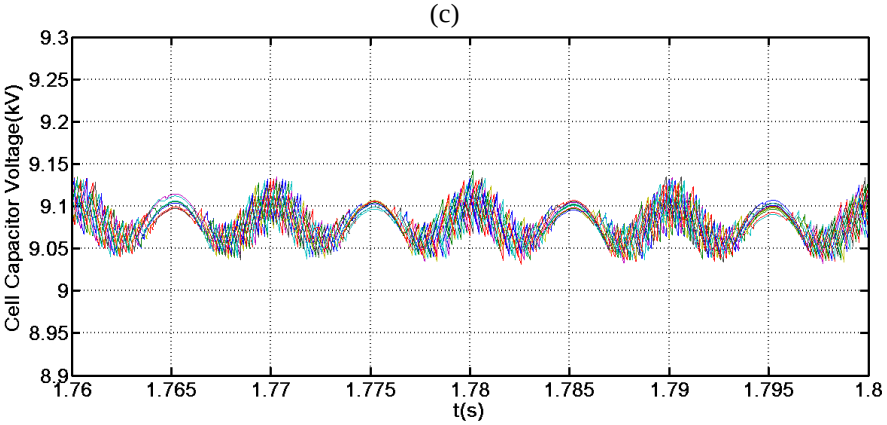
(a)


ILa
ILb
ILc
Three-phase Output Current(kA)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

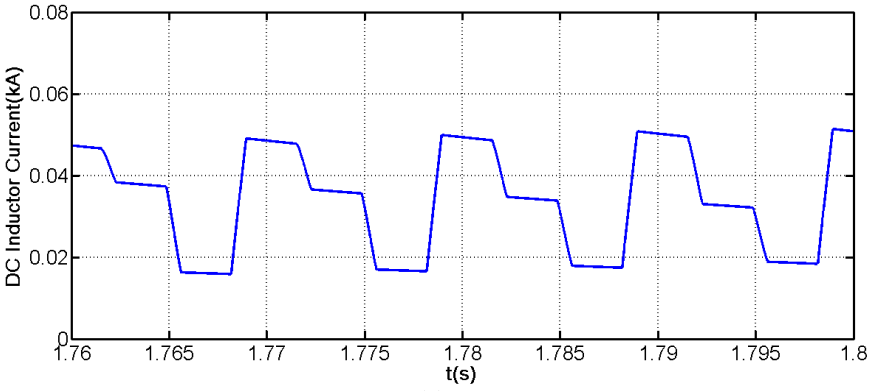
(b)


Chain-link Current(kA)
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

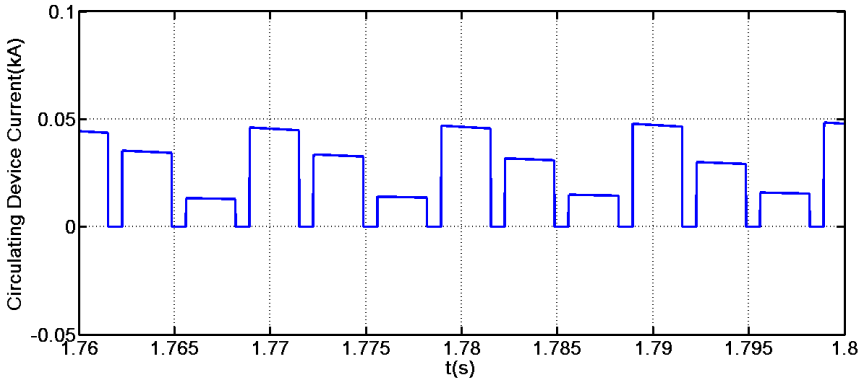
(c)


Cell Capacitor Voltage(kV)
9.3
9.25
9.2
9.15
9.1
9.05
9
8.95
8.9
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

(d)


DC Inductor Current(kA)
0.08
0.06
0.04
0.02
0
1.76
1.765
1.77
1.775
1.78
1.785
1.79
1.795
1.8
t(s)

(e)



(f)

Fig. 6-12. Waveforms under zero power factor: (a) converter phase '*a*' output voltage with triplen component; (b) three-phase line current in fundamental frequency; (c) chain-link current of phase '*a*'; (d) cell capacitor voltage balancing results; (e) DC side inductance currents; and (f) circulating valve device current.

6.7.2 Operation of Three-phase CTFB-HMC based STATCOM

The grid-connected CTFB-HMC model with 3 FB cells using PWM method is built and tested in Matlab/Simulink to demonstrate two aspects:

- For a small number of cells per chain-link, operation in PWM mode is able to achieve high quality output voltage with a modest increase on the average switching frequency for each device.
- The proposed converter is suitable for FACTS devices and its control strategy in Fig. 6-9 is verified with typical STATCOM operation.

Table 6-3. Specifications of CTFB-HMC model as STATCOM.

CTFB-HMC with 3 cells per phase	
Apparent power rating S_{con}	60MVA
DC link voltage V_{dc}	40kV
DC link capacitor C_d	470μF
Cell capacitor C_{cell}	2200 μF
Shunt inductor L_{sh}	12mH
Converter switching frequency	2.5kHz

Table 6-4. Specifications of transformer installation.

Three-phase independent shunt transformer	
Power capacity	60MVA
Voltage ratio	63.5kV/21.2kV
Per unit impedance	(0.0003+j0.05)

Table 6-5. AC transmission system parameters.

Grid parameters for shunt compensation	
Nominal line voltage	110kV(RMS)
Short-circuit power rating	2GVA
X/R ratio	20

The parameters for CTFB converter, interfacing transformer and the grid are listed in Table 6-3, Table 6-4 and Table 6-5 respectively.

Waveforms of the CTFB-HMC with PWM mode are presented in Fig. 6-13, where the converter phase synthesized voltage with triplen components and chain-link current are shown by Fig. 6-13(a) and (b) respectively. The inrush current in the chain-link is minor due to the low power factor in typical STATCOM. Fig. 6-13(c) is the cell capacitor voltage balancing results under PWM operation.

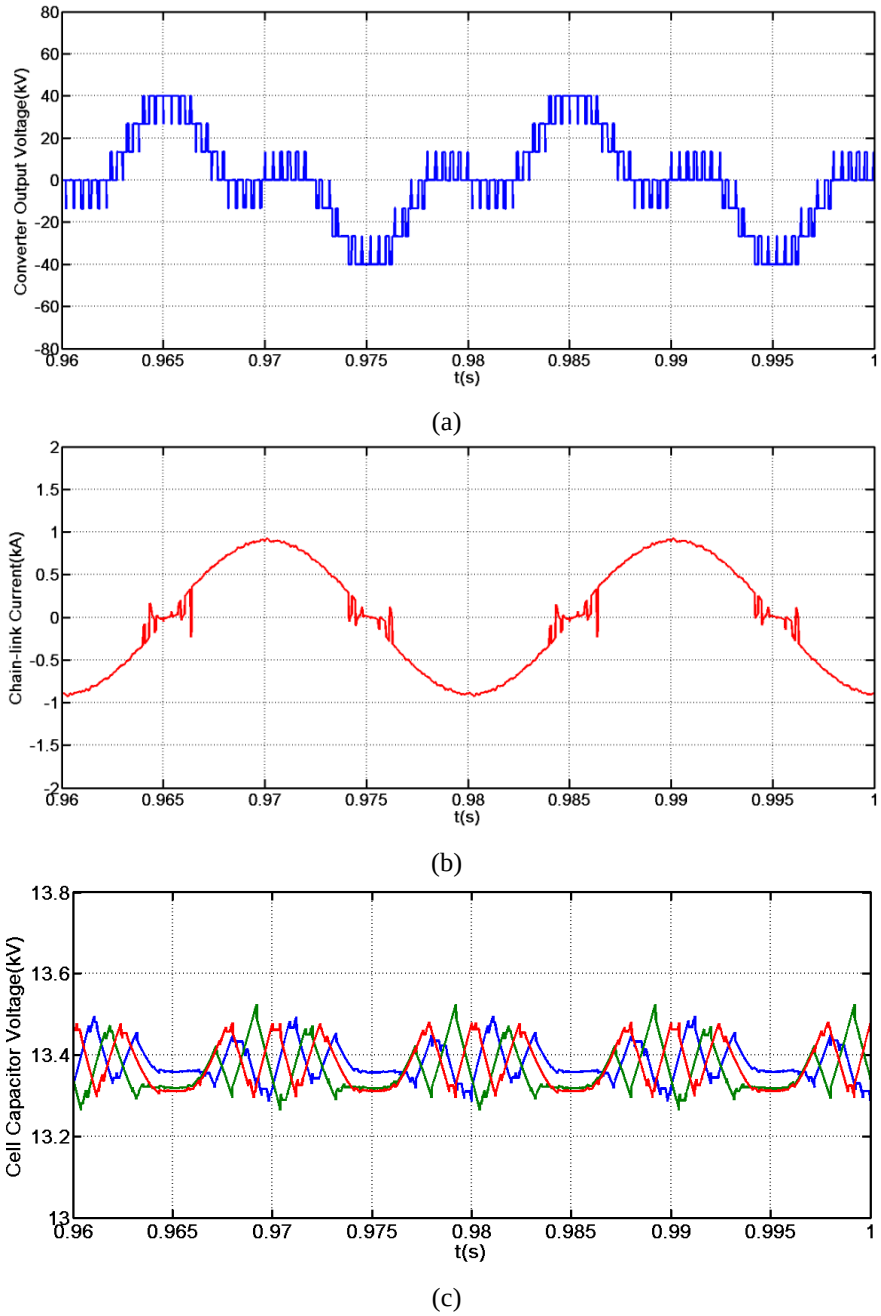
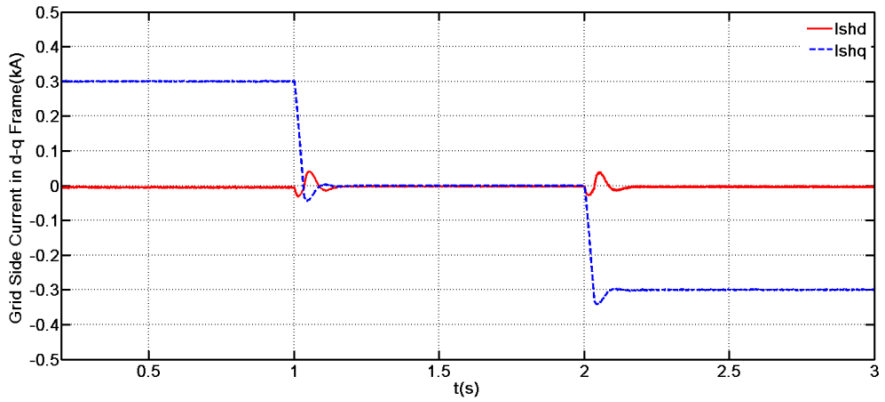
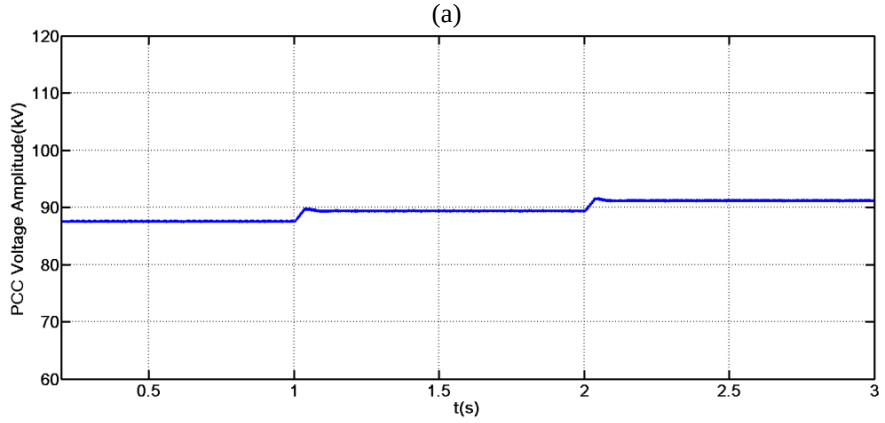


Fig. 6-13. Waveforms of the PWM mode CTFB converter: (a) converter phase voltage with triplen component; (b) converter chain-link current; and (c) cell capacitor voltage.

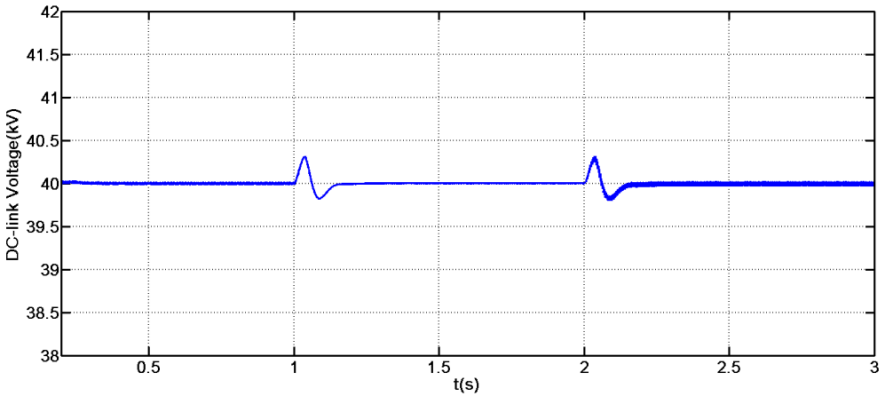
As illustrated in Fig. 6-9, the direct axes controller is employed to maintain the DC-link voltage in this illustration, while the quadrature controller regulates the reactive power exchange with the grid. With the reference command shift, in Fig. 6-14(a), the quadrature current i_q is controlled to step from +300A to 0 at t=1s and then to -300A at t=2s. Correspondingly, the reactive power exchanged with the grid will increase, leading to a noticeable change in the PCC voltage magnitude as shown in Fig. 6-14(b). Then, Fig. 6-14(c) and (d) manifest the DC-link voltage response and modulation index self-adjustment for the CTFB converter. In further, the zoomed-in PCC voltage and shunt current waveforms are displayed in Fig. 6-14(e) and (f).



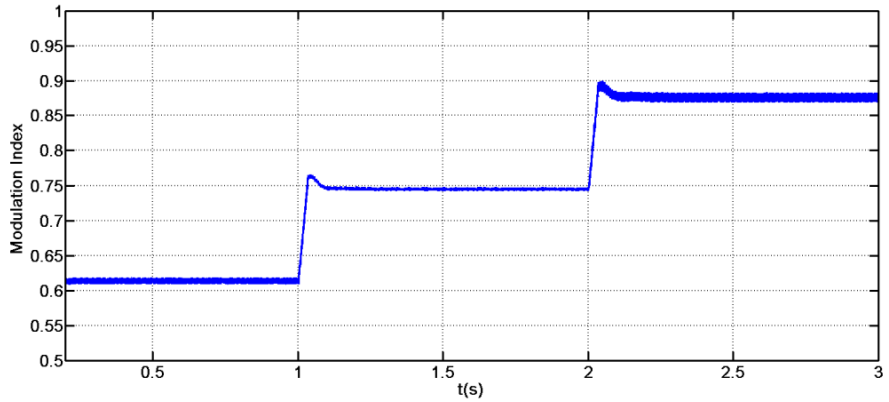
(a)



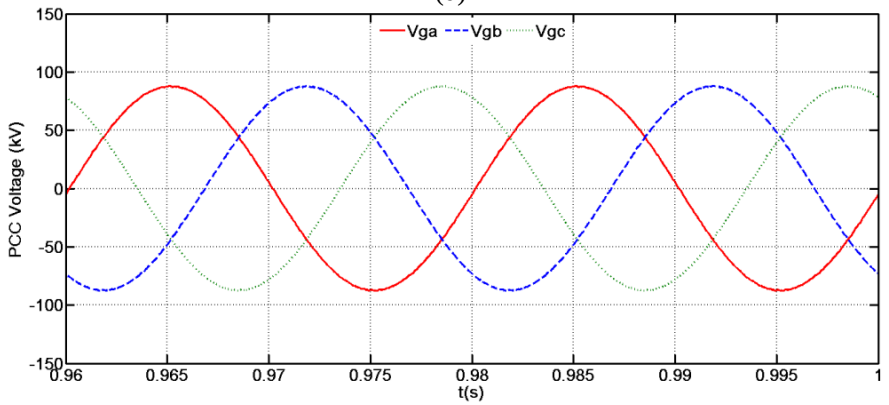
(b)



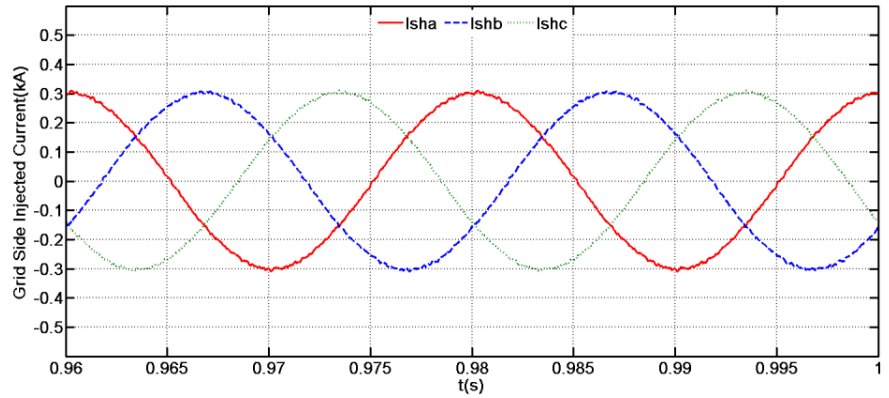
(c)



(d)



(e)



(f)

Fig. 6-14. Transient processes for three-phase CTFB-HMC based STATCOM: (a) grid side shunt current in *d*-*q* frame; (b) PCC voltage amplitude; (c) DC-link voltage response; (d) modulation index self-adjustment of the CTFB converter; (e) PCC voltage; and (f) shunt current.

6.8 Experimental Verification

The single-phase CTFB-HMC converter with three cells in the chain-link is tested under standalone operation as in Fig. 6-15. Since the number of cells is limited, conventional CB-PWM method is used for voltage synthesis in this experiment. Due to the unidirectional DC side current, the circulating valve for chain-link current limit is implemented by the parallel combination of an inductor and diode. Also, in order

to imitate the three-phase CTFB converter from a single-phase bridge operation, a third order harmonic trap is installed in the AC side to remove the triplen current component from load current. The harmonic trap consists of an inductor in parallel with a capacitor, and the overall impedance seen by the 3rd harmonic voltage component is infinite with proper tuning of the passive element parameters [28]. In this way, the line current will contain no 3rd order harmonic current as in the typical three-phase system case.

The detailed converter specifications for this prototype are as follows: nominal power rating: 1kVA; DC-link voltage: 200*V*; DC-link capacitance: 470μF; FB cell capacitance: 2200μF; power switches: IGBT G4PC40FD; DC side circulating valve: 3.3*mH* inductor and anti-parallel diode in IGBT G4PC40FD; AC side *L*-*C* filter: 10*mH* inductor and 33μF capacitance; third order harmonic trap: 10*mH* inductance and 110μF capacitance. To realize the modulation scheme in Fig. 6-4 as well as the cell capacitor voltage balancing algorithm in Fig. 6-8, the Infineon DSP Tricore TC1796 is employed as the controller in Fig. 6-15 to generate the IGBT switching signals.

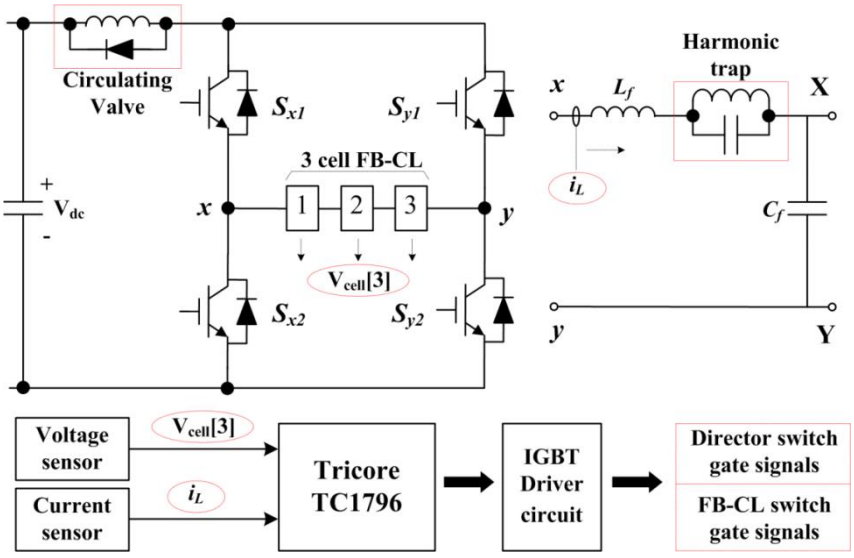
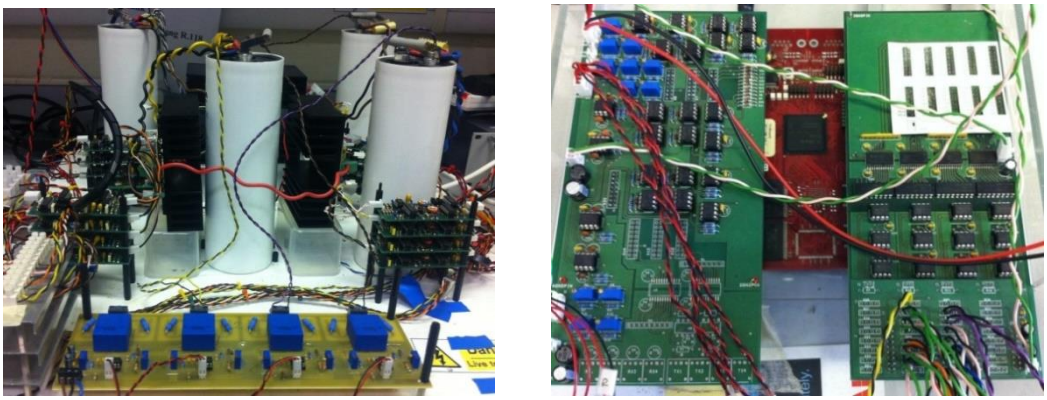


Fig. 6-15. The experiment setup of single-phase 3 cells CTFB-HMC with harmonic trap.

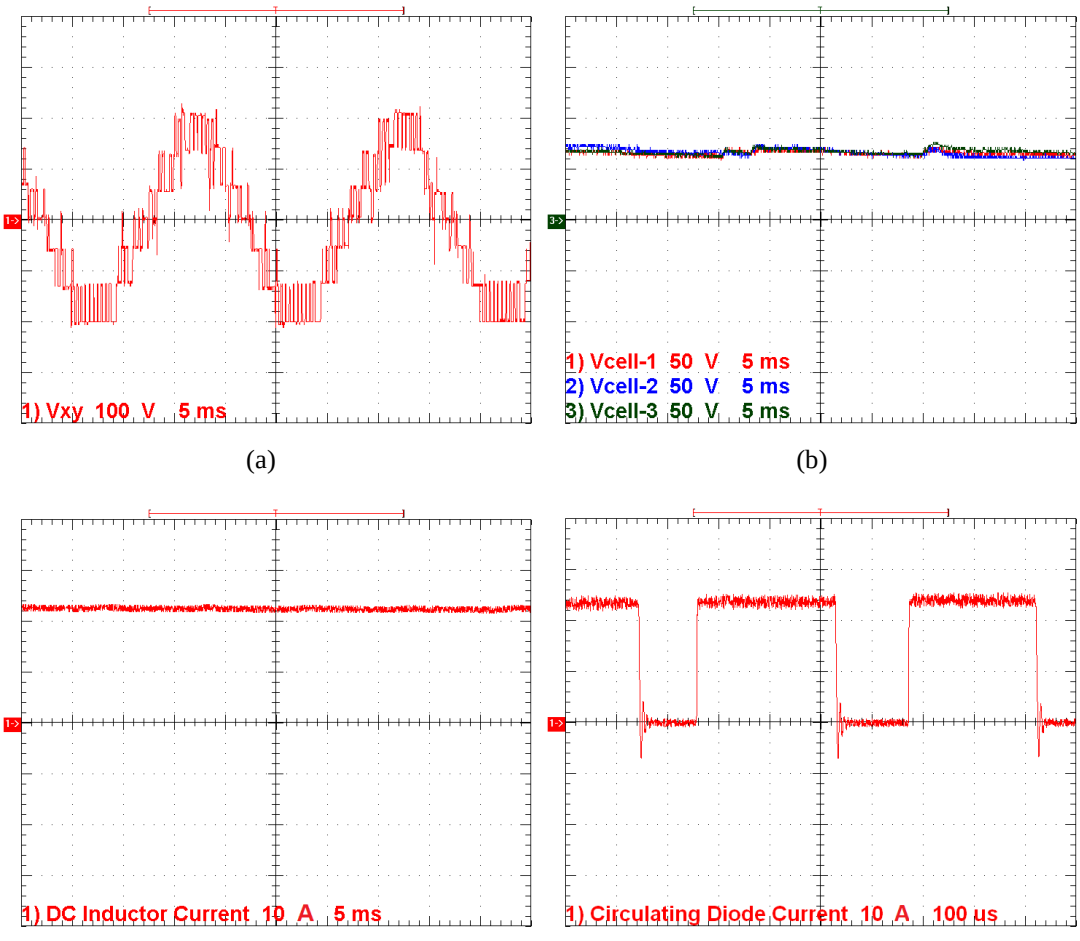
The hardware installation photograph is in Fig. 6-16. Initially, the modulation index is set to be 0.8 without triplen signal injection and the load resistance is 33Ω. By the CB-PWM operation, the output multilevel voltage in Fig. 6-17(a) can touch the full DC-link voltage; thus, energy balancing for cell capacitors is fulfilled but with a noticeable ripple near the AC side peak voltage area as shown in Fig. 6-17(b). This is caused by the short time duration for energy exchange between DC-link and the cell

capacitors. Accordingly, the DC side inductor current shown in Fig. 6-17(c) is high in order to balance the energy within the directing switch enabled time. The zoomed-in version of the high frequency current waveform of the circulating diode in the DC side is displayed in Fig. 6-17(d).



(a) (b)

Fig. 6-16. The picture of experimental installation: (a) CTFB converter and (b) DSP controller.

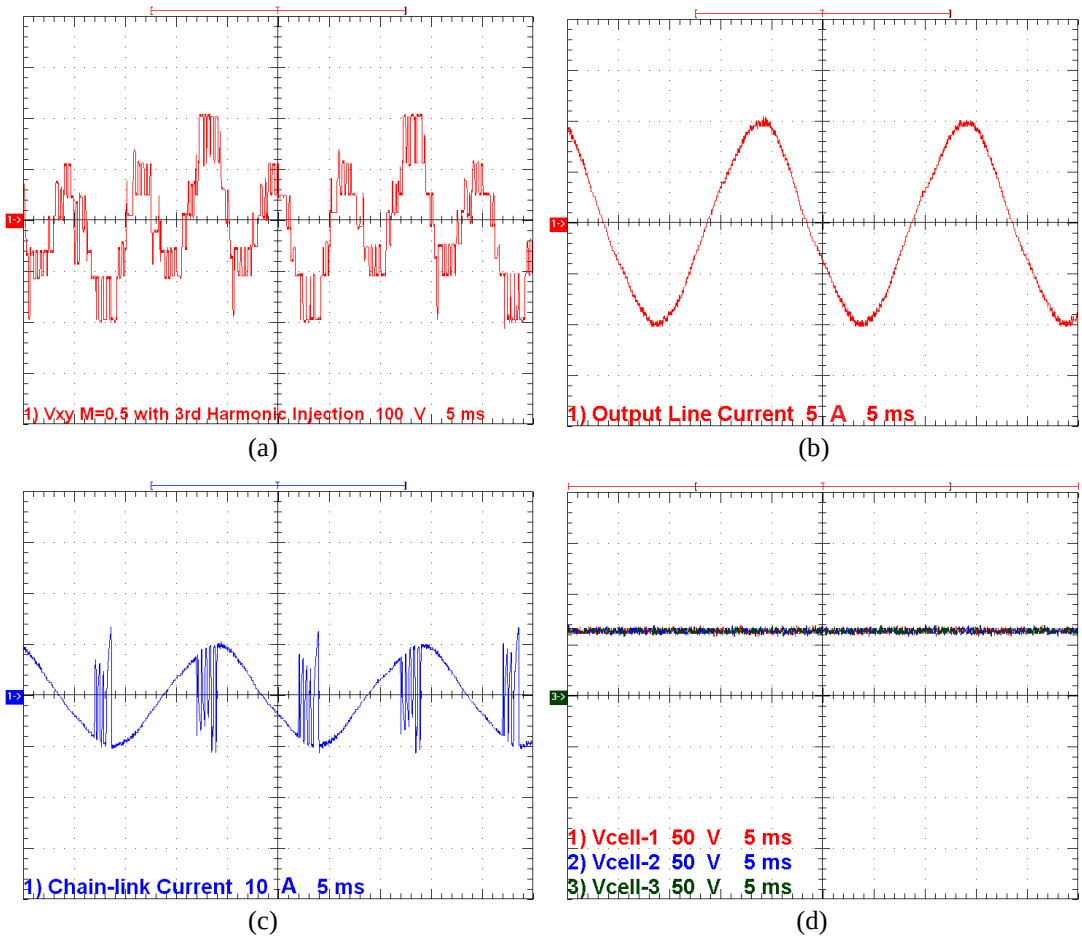


(a) (b)

(c) (d)

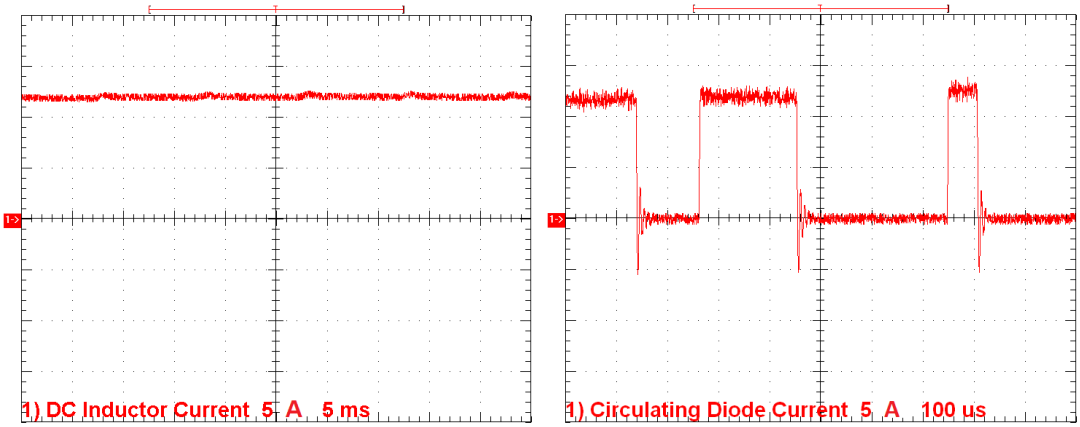
Fig. 6-17. The CTFB converter with 0.8 modulation index and no triplen component injection: (a) chain-link output voltage waveform; (b) cell capacitor voltage balancing results; (c) DC inductor current; and (d) zoomed-in circulating valve current.

In order to overcome the energy balancing constraint for the CTFB-HMC with low modulation index, the triplen component signal is inserted as illustrated in (6.11). If the required modulation index is set to be 0.5, the multilevel output voltage across the FB-CL in this case is shown in Fig. 6-18(a), and the corresponding line current is presented in Fig. 6-18(b). The current contains predominantly fundamental frequency due to the use of the 3rd order harmonic trap. In further, the current waveform of the FB-CL is displayed by Fig. 6-18(c), where the current direction is reversed to charge the cell capacitors during the effective conduction time of directing switches. With the injection of triplen component in reference signal, the chain-link output voltage is able to maintain the peak phase voltage value as $\pm V_{dc}$; thus, the energy balancing for cell capacitors in the FB-CL can be implemented for low modulation index condition as presented in Fig. 6-18(d), where the voltage ripple are removed due to the extension of the voltage clamping time by the triplen component injection. Also, from Fig. 6-18(e) and (f), the DC side inductor current and the circulating diode current are both reduced to the load current level.



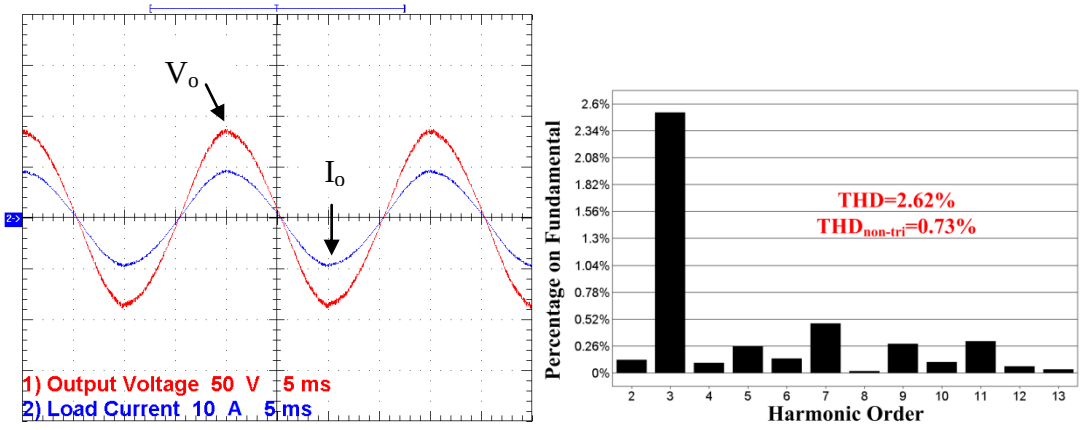
(a) (b)

(c) (d)



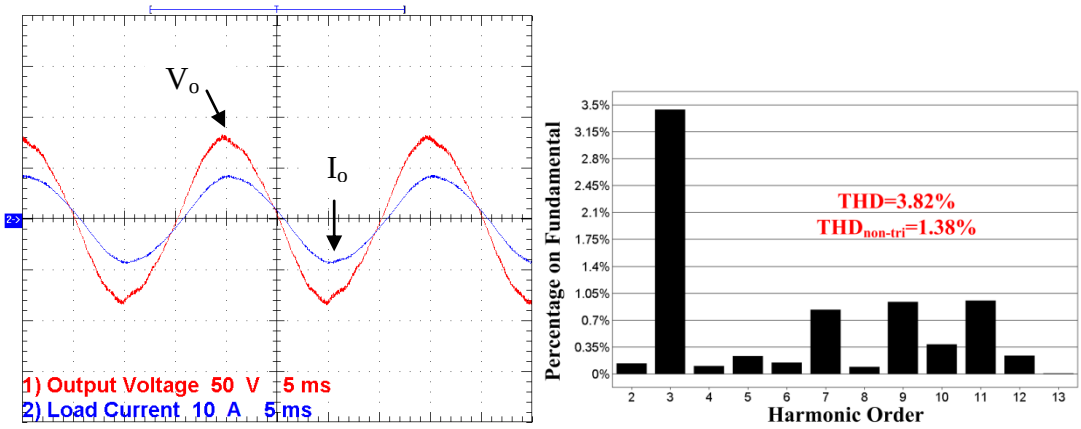
(e) (f)

Fig. 6-18. Waveforms of the CTFB-HMC with 0.5 modulation index and triplen component injection: (a) voltage waveform on the converter output pole; (b) AC side current with 3rd order harmonic trap; (c) the FB-CL current; (d) cell voltage balancing results; (e) DC inductor current; and (f) zoomed-in circulating valve current.



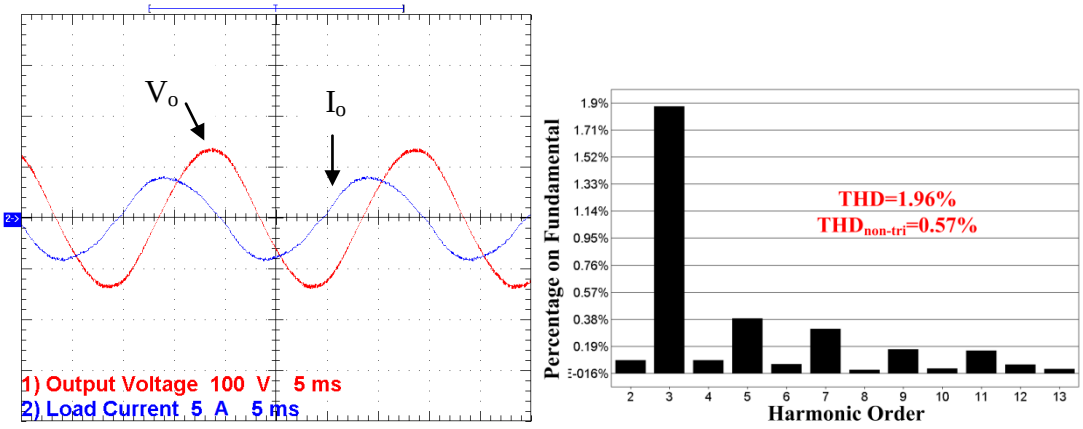
(a) (b)

Fig. 6-19. The post-filter voltage and current with resistive load: (a) time-domain waveforms and (b) base-band voltage harmonic distribution.



(a) (b)

Fig. 6-20. The post-filter voltage and current with inductive load: (a) time-domain waveforms and (b) base-band voltage harmonic distribution.



(a) (b)

Fig. 6-21. The post-filter voltage and current with capacitive load: (a) time-domain waveforms and (b) base-band voltage harmonic distribution.

Keeping the pre-set 0.5 modulation index and triplen component reference signal, the post-filter output voltage and current feeding a 9.2Ω resistive load are demonstrated by Fig. 6-19(a), where the CTFB converter can generate the desired fundamental voltage with the modulation method in (6.11) provided the triplen component is eliminated. Particularly in this experiment, a certain amount of residual 3rd order harmonics is observed in the base-band spectrum in Fig. 6-19(b) due to the non-ideal parameters in the harmonic trap design. It is expected that in a real three-phase CTFB-HMC, these harmonics can be fully cancelled in line-to-line voltage. On this basis, the THD values with or without triplen harmonics are calculated as in Fig. 6-19(b). Similar conclusions for inductive load (9.2Ω, 5mH) and capacitive load (9.2Ω, 100μF) conditions can be concluded from Fig. 6-20 and Fig. 6-21, respectively. Therefore, the proposed CTFB-HMC topology is verified to be able to operate under various power factor conditions with the proposed modulation schemes.

6.9 Summary

The controlled transition full-bridge hybrid multilevel converter (CTFB-HMC) has been proposed in this paper. The main features are summarized as follows:

- The CTFB-HMC uses a full-bridge (FB) cell chain-link that dynamically clamps the output poles to synthesize multilevel voltage. Thus, the transformer avoids high dv/dt, which reduces the insulation design demand.
- Due to the two-leg configuration per phase in the proposed topology, its DC voltage utilization and power density are doubled the conventional MMC and

hybrid multilevel converters (HMC). Therefore, the number of cell capacitors (footprint) can be minimized when transferring the same power.

- The conduction path device number of the CTFB-HMC is minimized to be same as the half-bridge (HB) cell MMC for per unit power, which leads to better efficiency performance over other topologies including the mixed cell MMC, the FB-MMC and the alternative arm multilevel converter (AAMC).
- The proposed CTFB topology has no DC current in its chain-link, which makes the cell capacitor voltage fluctuate without fundamental frequency and benefits the converter dynamic performance.
- In the proposed CTFB-HMC, a common DC side inductor can be shared by multiple phases, while the conventional MMC has a pair of inductors in each phase for inrush current limiting. A single inductor will reduce converter volume and weight.
- Energy balancing for the cell capacitors in the proposed CTFB converter is implemented utilizing the bipolar voltage output ability of FB cells. To ensure the net energy exchange on the chain-link is zero during a fundamental period, a triplen component signal is injected to realize full range adjustment of the modulation index, which can be neutralized in three-phase systems.
- Comparison between the CTFB-HMC and other multilevel converters shows CTFB-HMC superiorities including doubled power density, improved efficiency and reduced total costs.
- The control strategy is illustrated in the *d-q* frame. Then, simulation and experimentation showed the feasibility of the proposed approaches.
- The main limitation of the proposed converter is the lack of reverse-blocking capability as with the typical HB-MMC. Therefore, in this paper, the CTFB-HMC is suggested for applications without long distance DC cables, such as fractionally connected FACTS devices and machine drives.

Reference

[1] J. Rodriguez, S. Bernet, W. Bin, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *Industrial Electronics, IEEE Transactions on,* vol. 54, pp. 2930-2945, 2007.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, W. Bin, *et al.*, "Recent Advances and Industrial Applications of Multilevel Converters," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 2553-2580, 2010.

[3] Z. Yuebin, J. Daozhuo, H. Pengfei, G. Jie, L. Yiqiao, and L. Zhiyong, "A Prototype of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 3267-3278, 2014.

[4] S. Rivera, S. Kouro, W. Bin, S. Alepuz, M. Malinowski, P. Cortes, *et al.*, "Multilevel Direct Power Control - A Generalized Approach for Grid-Tied Multilevel Converter Applications," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 5592-5604, 2014.

[5] B. S. Riar and U. K. Madawala, "Decoupled Control of Modular Multilevel Converters Using Voltage Correcting Modules," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 690-698, 2015.

[6] S. Debnath, Q. Jiangchao, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 37-53, 2015.

[7] G. Feng, N. Decun, T. Hao, J. Chunjuan, L. Nan, and Z. Yong, "Control of Parallel-Connected Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 372-386, 2015.

[8] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 4-17, 2015.

[9] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 18-36, 2015.

[10] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 57-68, 2012.

[11] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 349-357, 2015.

[12] H. Saad, T. Ould-Bachir, J. Mahseredjian, C. Dufour, S. Dennetiere, and S. Nguefeu, "Real-Time Simulation of MMCs Using CPU and FPGA," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 259-267, 2015.

[13] D. Siemaszko, "Fast Sorting Method for Balancing Capacitor Voltages in Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 463-470, 2015.

[14] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, D. R. Critchley, and R. W. Crookes, "A new hybrid multi-level Voltage-Source Converter with DC fault blocking capability," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.

[15] A. M. Cross, D. R. Trainer, and R. W. Crookes, "Chain-link based HVDC Voltage Source Converter using current injection," in *AC and DC Power*

Transmission, 2010. ACDC. 9th IET International Conference on, 2010, pp. 1-5.

[16] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell, and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *Power Systems, IEEE Transactions on,* vol. 28, pp. 335-346, 2013.

[17] R. Feldman, M. Tomasini, J. C. Clare, P. Wheeler, D. R. Trainer, and R. S. Whitehouse, "A hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, 2010, pp. 1-6.

[18] G. P. Adam and B. W. Williams, "New emerging voltage source converter for high-voltage application: hybrid multilevel converter with dc side H-bridge chain links," *Generation, Transmission & Distribution, IET,* vol. 8, pp. 765-773, 2014.

[19] P. Ladoux, N. Serbia, P. Marino, and L. Rubino, "Comparative study of variant topologies for MMC," in *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2014 International Symposium on*, 2014, pp. 659-664.

[20] G. P. Adam, I. A. Abdelsalam, K. H. Ahmed, and B. W. Williams, "Hybrid Multilevel Converter With Cascaded H-bridge Cells for HVDC Applications: Operating Principle and Scalability," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 65-77, 2015.

[21] C. Oates, K. Dyke, and D. Trainer, "The use of trapezoid waveforms within converters for HVDC," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[22] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday, and B. W. Williams, "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 5439-5457, 2015.

[23] M. Zygmanowski, B. Grzesik, M. Fulczyk, and R. Nalepa, "Analytical and numerical power loss analysis in Modular Multilevel Converter," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE,* 2013, pp. 465-470.

[24] P. L. T. Jonsson;, S. Maiti; and Y. Jiang-Häfner, , "Converter Technologies and Functional Requirements for Reliable andEconomical HVDC Grid Design," in *CIGRÉ Canada Conference, 2013*, The Westin Calgary,Alberta.

[25] S. Angkititrakul and R. W. Erickson, "Control and implementation of a new modular matrix converter," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE,* 2004, pp. 813-819 vol.2.

[26] B. N. Alajmi, K. H. Ahmed, G. P. Adam, and B. W. Williams, "Single-Phase Single-Stage Transformer less Grid-Connected PV System," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2664-2676, 2013.

[27] O. C. Onar, O. H. A. Shirazi, and A. Khaligh, "Grid Interaction Operation of a Telecommunications Power System With a Novel Topology for Multiple-Input Buck-Boost Converter," *Power Delivery, IEEE Transactions on,* vol. 25, pp. 2633-2645, 2010.

[28] Z. Youjun and R. Xinbo, "AC-AC Converter With Controllable Phase and Amplitude," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 6235-6244, Nov 2014.

CHAPTER 7

Literature Review for Direct AC-AC Converter Topologies

This chapter discusses single-stage direct AC-AC converters that are suitable for FACTS applications. The main advantage of this type of solution is the absence of any bulky DC-link capacitor; thus, reduced footprint and extended service life for the overall system can be expected. Among the various AC-AC topologies, the matrix converter, vector switching converter, AC chopper, high frequency link AC-AC converter, and full-bridge cell chain-links AC-AC converter, are review.

7.1 Background

In many applications at distribution and transmission levels, such as AC power control, power quality enhancement, grid interfacing of renewable energy and machine drives, the back-to-back (B2B) AC-DC-AC configuration is widely adopted [1-4]. Due to its side-to-side decoupling, full control over frequency, amplitude and phase-angle of the AC voltage/current can be implemented, and fault ride-through ability is also facilitated [5, 6]. However, the energy storage element in the DC-link is sizable, uneconomical, has low reliability and a short service life. Considering these advantages and disadvantages due to the DC-link capacitor, when the power converter application requires fault ride-through, the AC-DC-AC solution is preferred. But if the operational environment is marginally volatile (relative to the full rating of the system) and fault conditions can be handled by circuit breakers or other converters, direct AC-AC conversion without a DC-link is viable. Thus a trade-off centred on the DC-link capacitor should be made according to the specific demand [7]. The single stage direct AC-AC converter has been developed as an alternative to avoid the DC-link capacitance and its problems.

The matrix converter employs arrays of bidirectional power switches to synthesize the target voltage waveform with variable frequency, phase-angle and amplitude in multi-phase input system [8]. A large number of power switches, low commutation reliability and complex modulation schemes are the main disadvantages of the matrix converter, among AC-AC converters.

The vector switching converter (VeSC) incorporates multi-throw input voltage sources from multiplexed transformers, which leads to a flexible system design but a low power density (MVA/m^3) [9].

The AC chopper and high frequency link (HFL) AC-AC converter are derived from the DC chopper and isolated DC-DC converters respectively. Thus, they are basically used as a voltage amplitude regulator or restorer [10], where the input and output frequencies are the same.

A full-bridge cell is able to generate bipolar voltage, thus, chain links of full-bridge cells are able to withstand AC voltage [11]. However, to generate the phase-amplitude independent voltage output, more than one branch should be used to ride through the zero-crossing region of the input voltage. With this logic, the full-bridge modular multilevel AC-AC converter, full-bridge modular multilevel matrix

converter (M3C) and hexverter have been presented [12-16]. Compared to conventional B2B MMC configurations, the intermediate DC-link stage is absent in these topologies. However, the full-bridge cells still use DC capacitors to ensure voltage synthesis ability, which discounts the compactness and service-life.

7.2 The Matrix Converter

AC voltage amplitude regulation is straightforward; however, to change the output voltage frequency and phase-angle, the zero-crossing area of input AC voltage is the main constraint for phase-to-phase conversion. Therefore, the cross connection of a multi-phase input system is necessary to realize full AC voltage control.

The direct matrix converter (DMC) uses bidirectional switches to select the appropriate power path for each phase to feed the load, thus, independent control of voltage magnitude, frequency, phase angle and power factor can be achieved [8]. The three-phase input, three-phase output 3×3 DMC is shown in Fig. 7-1. All the bidirectional switches in this thesis are implemented by anti-series connected IGBTs, as in Fig. 7-1. Although other possible combinations, such as the reverse blocking IGBT (RB-IGBT) are possible, they are not considered or discussed in this thesis.

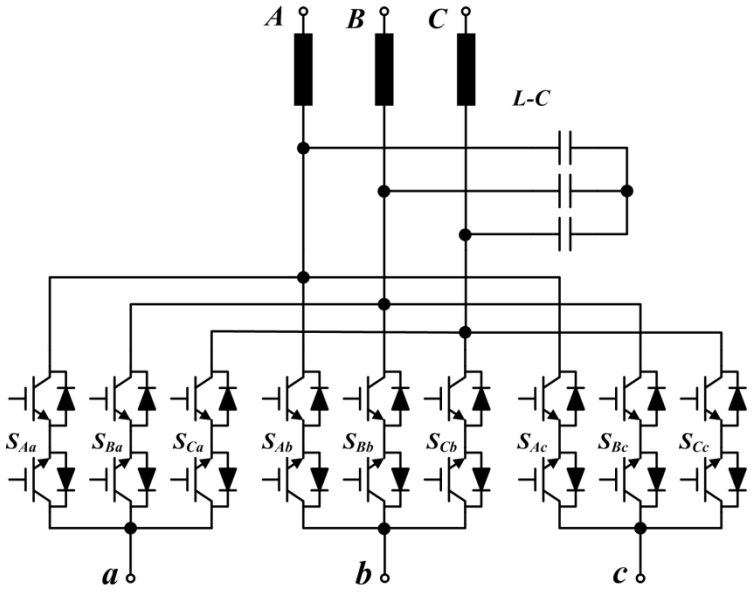


Fig. 7-1. Three-phase input three-phase output 3×3 DMC topology.

The modulation and control schemes of the DMC can be divided into several groups, including scalar methods, pulse width modulation (PWM), direct torque control, predictive control, etc. The scalar methods represent the direct transfer function (Venturini) approach and Roy composition strategy using instantaneous voltage ratio.

PWM techniques developed for DC-AC applications are also transplanted into matrix converter, such as the carrier based PWM and SVM. In the machine drive area, direct torque or flux control is developed to fulfil speed control. Mature hardware support and advanced modern control theory such as predictive method, have been presented recently [17].

From Fig. 7-1, in each power path, only one bidirectional switch participates to define the output voltage; so either a dead band time or overlap will produce commutation problems, such as a line-to-line short-circuit or output open-circuit due to the lack of clamping. To ease this challenge, multiple-step commutation schemes are developed as in [18].

In an attempt to reduce the risk of commutation failure, the indirect matrix converter (IMC) is presented and shown in Fig. 7-2. It offers extra clamping for power path transitions by choosing a proper modulation method. The total number of active switches in the IMC is equal to that in the DMC. The implementation of PWM and predictive control for the IMC are presented in [19] and [20]. The main drawbacks of the IMC topology are the increased power losses in the conduction paths and deteriorated output voltage linearity owing to the fluctuant intermediate link voltage.

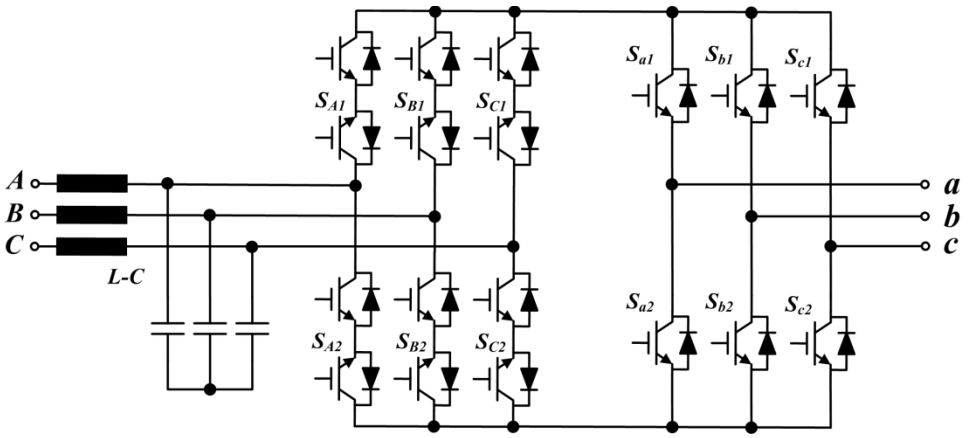


Fig. 7-2. Indirect 3×3 matrix converter topology.

Based on the matrix converters in Fig. 7-1 and Fig. 7-2, various topologies can be derived, such as the sparse matrix converter (SMC), very-sparse matrix converter (VSMC), ultra-sparse matrix converter (USMC), full-bridge matrix converter, hybrid matrix converter, and indirect three-level matrix converter [21].

For all matrix converters, the numerous power switches as well as the complicated modulation and commutation schemes are the main disadvantages.

7.3 Vector Switching Converter

Compared with the DMC, an alternative way of cross connecting the output phase with various voltage inputs is to use multiplex phase-shift-transformers (PSTs) that offer phase-shifted multiple input sources. This combination is named the vector switching converter (VeSC) [9]. For a PST system with *N*-throw inputs, a three-phase output voltage requires $3\times N$ bidirectional switches to control the feeding source for each output terminal. A two-throw input three-phase output VeSC is shown in Fig. 7-3.

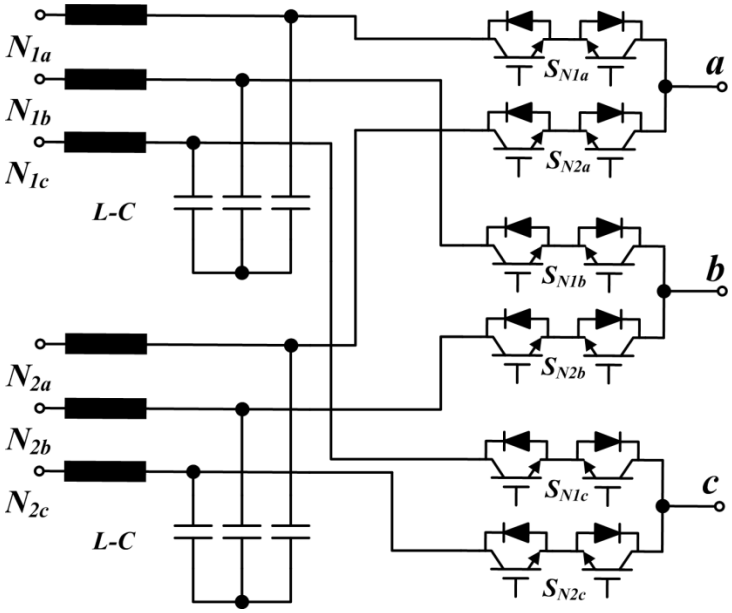


Fig. 7-3. Two-throw input three phase output VeSC configuration.

The VeSC is employed as FACTS controllers in [22] and [23]. Compared with matrix converters, the VeSC may reduce the number of switching devices only when the input source branches are not more than the input phase number. The main constraint is the strongly dependent relationship between the output voltage range and the complexity of input PST system. More input source throws can supply more degrees of freedom for voltage synthesis but increase system size and cost dramatically.

7.4 The AC chopper

Based on the DC chopper topology, various AC choppers exist for voltage amplitude control in the soft-start of induction motors and distributed voltage conditioning applications [16].

In Fig. 7-4(a), the three-phase AC chopper using three pairs of unidirectional power switches is shown. Both switches in the phase connected to lowest input voltage should be switched on in order to ensure a safe commutation; while the other four switches are modulated with predefined duty cycle signals. In this way, an output voltage with variable magnitude can be generated [16].

The use of bidirectional switches facilitates full blocking ability of voltage or current in both polarities. Fig. 7-4(b) shows an alternative topology of the three-phase AC chopper, mainly used for unbalanced voltage compensation. The two pairs of bidirectional switches are employed to control their output voltages, while the other phase input and output is directly feed through [16].

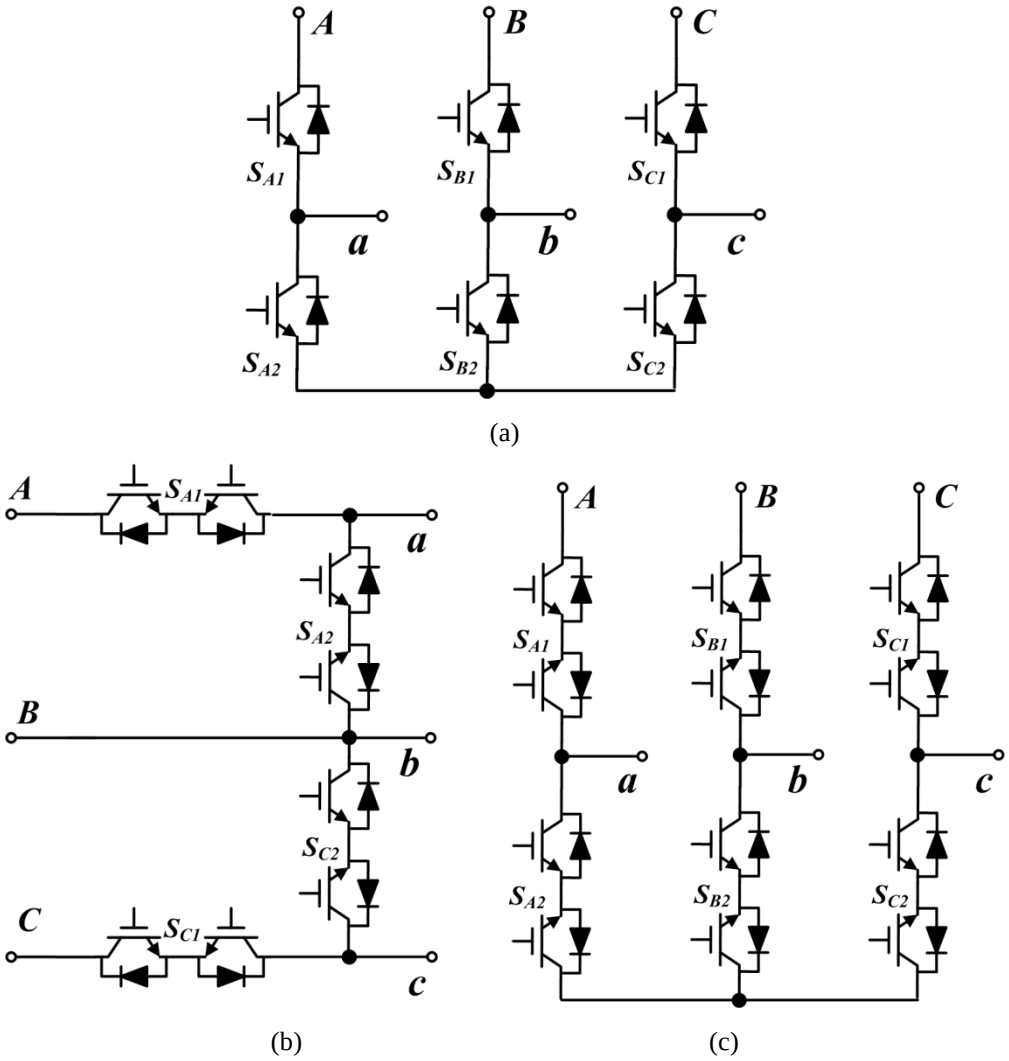


Fig. 7-4. Three-phase AC choppers topologies: (a) using unidirectional switches; (b) using bidirectional switches for two phases; and (c) using all bidirectional switches.

When pairs of bidirectional switches are used in each phases as shown in Fig. 7-4(c), independent phase voltage regulation and maximum control degree of freedom can

be achieved. By appropriate defined modulating signals for each phase, the AC chopper in Fig. 7-4(c) is able to shift the phase angle as presented in [24], which is a transplanted idea of the heterodyne method in communications.

7.5 High frequency link AC-AC converter

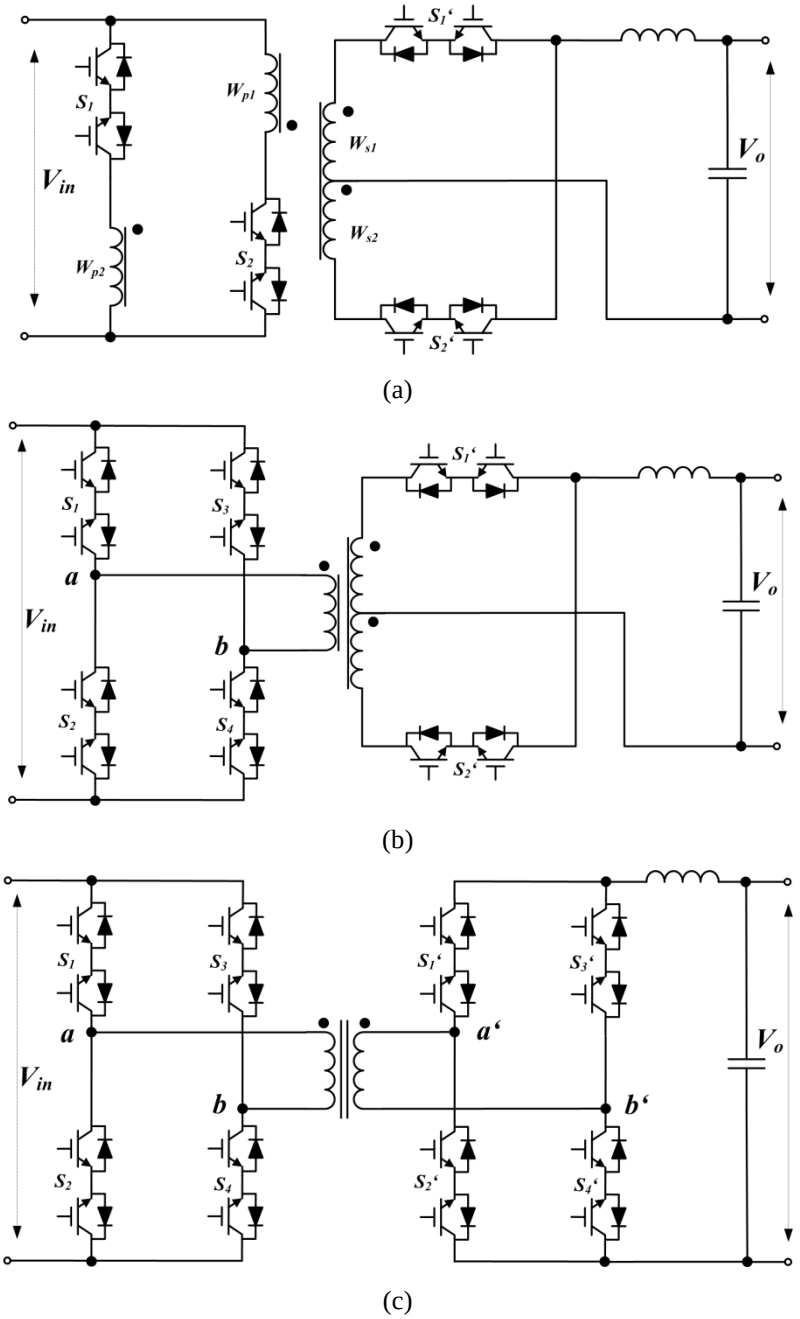


Fig. 7-5. Single-phase HFL AC-AC topologies: (a) push-pull forward converter; (b) full bridge converter; and (c) dual-active-bridge converter.

To build in AC-AC converter galvanic isolation between the input and output sides, without using line frequency transformers, high frequency link (HFL) techniques can be employed [25].

Several isolated DC-DC topologies such as the push-pull forward converter, full bridge converter and dual-active-bridge converter can be transplanted to HFL AC-AC versions with bidirectional switches as in Fig. 7-5, which are capable of savings on size, weight and cost of the overall system due to the use of high frequency transformers. The heterodyne principle is also applicable to the HFL AC-AC converter, where [26] presents its application as a low-speed drive and active power filter.

The switching averaged flux in the HFL AC-AC converter transformer is zero since the core can be reset within one switching period. However, the total losses are increased due to the extra power switches for wave shaping and the leakage inductance circulating processes. Currently, a switching frequency higher than 3kHz is not viable in large scale power applications, which makes HFL techniques less competitive. The absence of scalability in HFL AC-AC converter is also a constraint on power capacity extension.

7.6 Full-bridge cell based modular multilevel AC-AC converters

The modular multilevel converter (MMC) is widely researched in HVDC systems as a part of an AC-DC-AC configuration. Compared with conventional half-bridge cell topology, the full-bridge cell based MMC offers reverse blocking capability under the DC fault conditions due to the bipolar voltage synthesis ability of each arm. Thus, by using chain-links of full-bridge cells, several single-stage AC-AC converters with modular scalability have been presented [12-16].

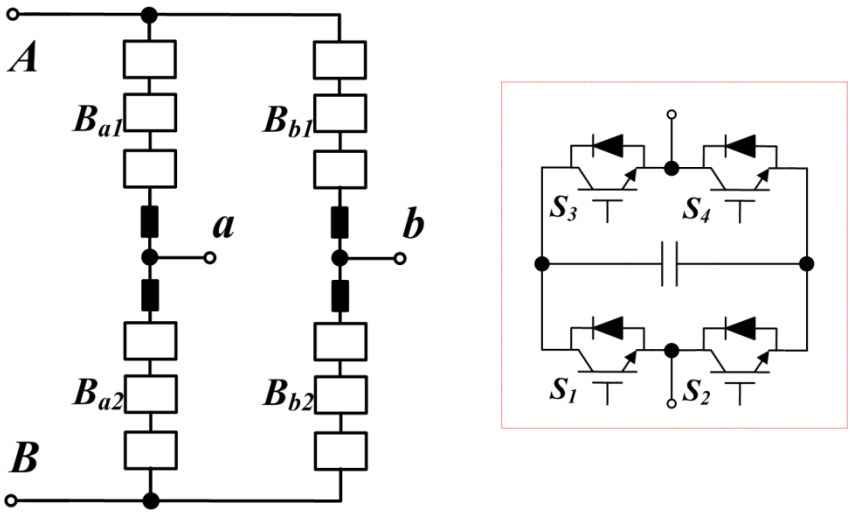


Fig. 7-6. Single-phase topology of full-bridge AC-AC MMC.

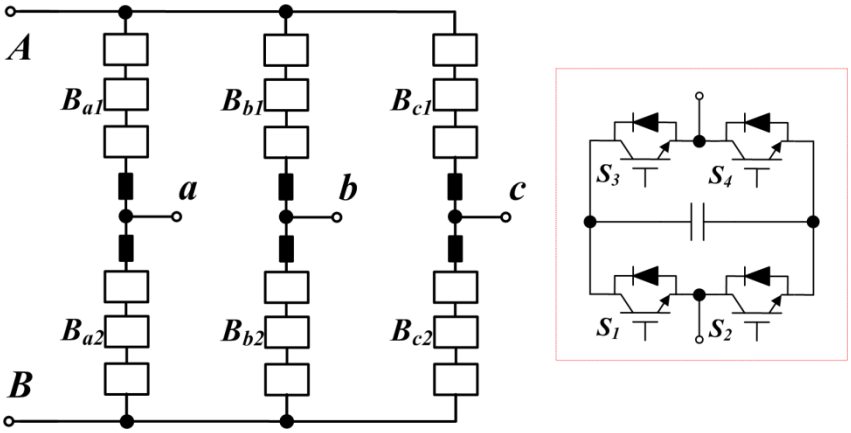


Fig. 7-7. Single-phase to three-phase AC-AC MMC with full-bridge cells.

A single-phase full-bridge cell based AC-AC MMC topology is shown by Fig. 7-6, which consists of four arms; and each sustains a bipolar voltage that is determined by the input and output voltage waveforms on the corresponding phase. This topology is developed into three-phase output system as in Fig. 7-7 [27]. For these direct AC-AC MMCs, the arm current may have various frequency components; whence nonlinear converter performance, where conventional feedback plus a time-domain PI controller scheme are difficult to be implemented. To overcome this problem, the control strategy of three-phase grid-connected AC-AC MMC in *d-q* frame is investigated in [27, 28]; and [14] presents a predictive control scheme applied to a single-phase AC-AC MMC, which can also be generalized to other similar converters.

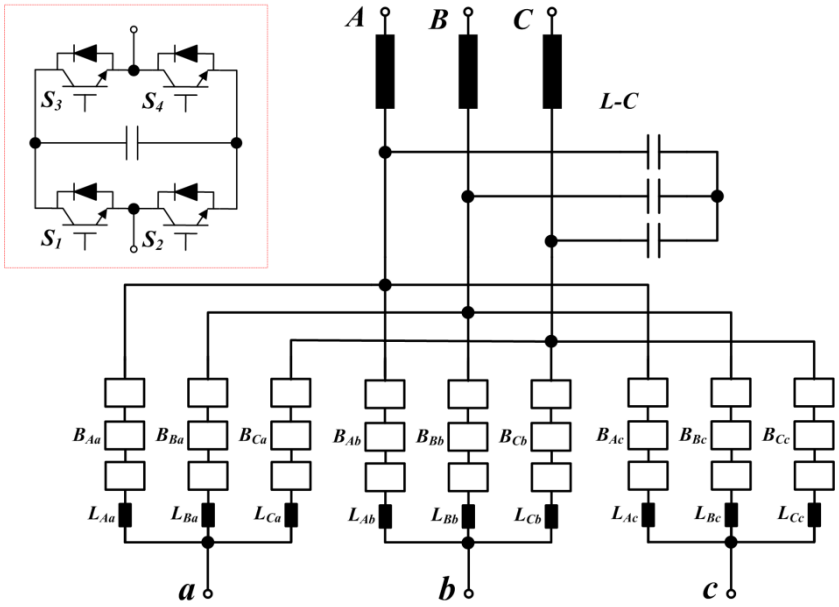


Fig. 7-8. Modular multilevel matrix converter (M3C) with full-bridge cells.

The full-bridge modular multilevel matrix converter (M3C) is proposed in [15] and shown in Fig. 7-8. The M3C replaces the bidirectional switch array in the original matrix converter with chain-links of full-bridge cells composed of four unidirectional switches and a DC capacitor. Therefore, each arm is able to generate bipolar voltage to realize the interconnection of two AC voltage sources.

The SVM method including the cell capacitor voltage balancing strategy for an M3C with one cell per arm has been presented in [29] and [30]. However, with higher cell numbers, the total number of available space vectors increases dramatically, making realization difficult. By transferring the AC input and output line inductances into the chain-links, each predefined voltage source mode full-bridge chain-link can be viewed as a controlled current source branch [31]. Then, the feed-forward control and DC cell capacitor voltage balancing algorithm are implemented as in [31] and [32] respectively. [33] describes a hierarchical feedback control scheme involving the inner arm current loop and the outer layer voltage loop. M3C power balancing analysis and its control design under unbalanced grid or load conditions are discussed for a low-speed drive in [34]. An independent M3C current control method is considered in [35]; and [36] presents an M3C variable-speed machine drive application with four cells per chain-link.

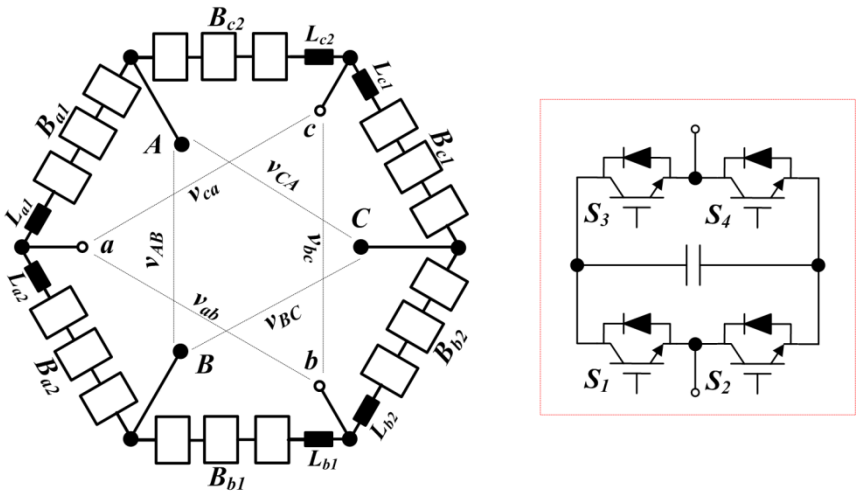


Fig. 7-9. Hexverter based on full-bridge cells configuration.

An alternative full-bridge chain-links based AC-AC converter configuration is shown in Fig. 7-9, which is named the hexverter in [16]. Compared with the M3C, it reduces the number of cells and power switching devices. Power balancing and adjacent power analysis for hexverter are researched in [37], where dimensioned experimental

verification for steady state operation is carried out. Its closed loop control strategy with cell voltage balancing is presented in [38].

Modularity is the main advantage of the full-bridge cell based topologies over traditional AC-AC converters, which makes them competitive in high-voltage high-power applications. However, although the intermediate full DC-link stage is eliminated, the full-bridge cell chain-links AC converters are actually not purely direct AC-AC conversions, because DC capacitors are translated into each cell and a voltage balancing scheme is necessary to maintain uniformly distributed DC voltage across them. This means energy storage elements are still required to support the voltage synthesis of this type of converters, under different load conditions.

7.7 Summary

In an attempt to remove the bulky DC-link in conventional AC-DC-AC converters, the main types of direct AC-AC converters were reviewed in this chapter. Attributes and limitations of each topology were discussed and can be summarized as follows:

- The matrix converter and the vector switching converter are able to independently control the voltage magnitude and phase angle by using the cross connection of different input phases. However, these converters require either numerous bidirectional power switches or complex multi-throw phase-shift-transformers as input sources, which are not cost-effective. Also, the lack of modularity makes them less competitive in high voltage applications, considering the converter fault tolerance.
- The AC chopper and high-frequency-link AC-AC converter originated from DC-DC equivalents; thus, they are usually employed to regulate the AC voltage amplitude against voltage sag/swell problems in the local infeed. The series connected power switches and high switching frequency (high power losses) confine them to small scale power conversion.
- Full-bridge chain-link based AC-AC converters facilitate scalability to medium and high voltage applications such as the interconnection of the wind turbine and grid. However, DC capacitors are required for each cell to give weak decoupling of both sides.

To combine the advantages of existing direct AC-AC converters, such as zero DC component, modularity and independent active/reactive power control ability, a new converter topology is to be investigated in chapters 8 and 9 of this thesis.

Reference

[1] A. de la Villa Jaen, E. Acha, and A. G. Exposito, "Voltage Source Converter Modeling for Power System State Estimation: STATCOM and VSC-HVDC," *Power Systems, IEEE Transactions on,* vol. 23, pp. 1552-1559, 2008.

[2] A. Cetin and M. Ermis, "VSC-Based D-STATCOM With Selective Harmonic Elimination," *Industry Applications, IEEE Transactions on,* vol. 45, pp. 1000-1015, 2009.

[3] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, "Power Capability Investigation Based on Electrothermal Models of Press-Pack IGBT Three-Level NPC and ANPC VSCs for Multimegawatt Wind Turbines," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 3195-3206, 2012.

[4] A. Gomez-Exposito, J. M. Mauricio, and J. M. Maza-Ortega, "VSC-Based MVDC Railway Electrification System," *Power Delivery, IEEE Transactions on,* vol. 29, pp. 422-431, 2014.

[5] N. Thanh Hai and L. Dong-Choon, "Advanced Fault Ride-Through Technique for PMSG Wind Turbine Systems Using Line-Side Converter as STATCOM," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 2842-2850, 2013.

[6] M. A. Parker, R. Li, and S. J. Finney, "Distributed Control of a Fault-Tolerant Modular Multilevel Inverter for Direct-Drive Wind Turbine Grid Interfacing," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 509-522, 2013.

[7] T. Friedli, J. W. Kolar, J. Rodriguez, and P. W. Wheeler, "Comparative Evaluation of Three-Phase AC-AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 4487-4510, Dec 2012.

[8] L. Meng Yeong, P. Wheeler, and C. Klumpner, "Space-Vector Modulated Multilevel Matrix Converter," *Industrial Electronics, IEEE Transactions on,* vol. 57, pp. 3385-3394, 2010.

[9] F. Mancilla-David, "AC link Vector Switching Converters for power flow control and power quality: A review," in *North American Power Symposium (NAPS),* 2009, pp. 1-7.

[10] J. Kaniewski, Z. Fedyczak, and G. Benysek, "AC Voltage Sag/Swell Compensator Based on Three-Phase Hybrid Transformer With Buck-Boost Matrix-Reactance Chopper," *Industrial Electronics, IEEE Transactions on,* vol. 61, pp. 3835-3846, Aug 2014.

[11] K. Sungmin, C. Shenghui, and S. Seung-Ki, "Modular multilevel converter based on full bridge cells for Multi-Terminal DC transmission," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[12] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *Industrial Electronics, IEEE Transactions on,* vol. 52, pp. 662-669, 2005.

[13] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 508-515.
[14] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive Control of AC-AC Modular Multilevel Converters," *Industrial Electronics, IEEE Transactions on*, vol. 59, pp. 2832-2839, Jul 2012.
[15] R. W. Erickson and O. A. Al-Naseem, "A new family of matrix converters," in *Industrial Electronics Society, 2001. IECON '01. The 27th Annual Conference of the IEEE*, 2001, pp. 1515-1520 vol.2.
[16] L. Baruschka and A. Mertens, "A new 3-phase direct modular multilevel converter," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-10.
[17] J. Rodriguez, M. Rivera, J. W. Kolar, and P. W. Wheeler, "A Review of Control and Modulation Methods for Matrix Converters," *Industrial Electronics, IEEE Transactions on*, vol. 59, pp. 58-70, 2012.
[18] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *Industrial Electronics, IEEE Transactions on*, vol. 49, pp. 276-288, 2002.
[19] M. Jussila and H. Tuusa, "Comparison of Direct and Indirect Matrix Converters in Induction Motor Drive," in *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, 2006, pp. 1621-1626.
[20] P. Correa, J. Rodriguez, M. Rivera, J. R. Espinoza, and J. W. Kolar, "Predictive Control of an Indirect Matrix Converter," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 1847-1853, 2009.
[21] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of Three-Phase PWM AC-AC Converter Topologies," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 4988-5006, Nov 2011.
[22] J. M. Ramirez, J. M. Gonzales, and M. L. Crow, "Steady state formulation of FACTS devices based on ac/ac converters," *Generation, Transmission & Distribution, IET*, vol. 1, pp. 619-631, Jul 2007.
[23] G. Venkataramanan, "Three-phase vector switching converters for power flow control," *Electric Power Applications, IEE Proceedings* -, vol. 151, pp. 321-333, 2004.
[24] D. M. Divan, D. M. Divan, and J. Sastry, "Voltage Synthesis Using Dual Virtual Quadrature Sources - A New Concept in AC Power Conversion," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 3004-3013, Nov 2008.
[25] C. Daolian and L. Jian, "The uni-polarity phase-shifted controlled voltage mode AC-AC converters with high frequency AC link," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 899-905, 2006.
[26] L. Chushan, D. Yan, L. Zibo, L. Wuhua, H. Xiangning, and W. Yousheng, "Virtual Quadrature Source-Based Sinusoidal Modulation Applied to High-Frequency Link Converter Enabling Arbitrary Direct AC-AC Power Conversion," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4195-4208, 2014.
[27] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, "A single-phase to three-phase direct AC/AC modular multilevel cascade converter based on double-star bridge-cells (MMCC-DSBC)," in *Future Energy Electronics Conference (IFEEC), 2013 1st International*, 2013, pp. 476-481.

[28] M. Hagiwara, R. Maeda, and H. Akagi, "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," *Industry Applications, IEEE Transactions on*, vol. 48, pp. 720-729, 2012.

[29] S. Angkititrakul and R. W. Erickson, "Control and implementation of a new modular matrix converter," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, 2004, pp. 813-819 vol.2.

[30] S. Angkititrakul and R. W. Erickson, "Capacitor voltage balancing control for a modular matrix converter," in *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, 2006, p. 7 pp.

[31] C. Oates, "A methodology for developing Chainlink converters," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.

[32] C. Oates and G. Mondal, "DC circulating current for capacitor voltage balancing in modular multilevel matrix converter," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-7.

[33] D. C. Ludois, J. K. Reed, and G. Venkataramanan, "Hierarchical Control of Bridge-of-Bridge Multilevel Power Converters," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 2679-2690, 2010.

[34] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Direct modular multi-level converter for gearless low-speed drives," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-7.

[35] F. Kammerer, J. Kolb, and M. Braun, "A novel cascaded vector control scheme for the Modular Multilevel Matrix Converter," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, 2011, pp. 1097-1102.

[36] W. Kawamura, M. Hagiwara, and H. Akagi, "A broad range of frequency control for the modular multilevel cascade converter based on triple-star bridge-cells (MMCC-TSBC)," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 4014-4021.

[37] L. Baruschka and A. Mertens, "A New Three-Phase AC/AC Modular Multilevel Converter With Six Branches in Hexagonal Configuration," *Industry Applications, IEEE Transactions on*, vol. 49, pp. 1400-1410, May-Jun 2013.

[38] S. I. Hamasaki, K. Okamura, and M. Tsuji, "Control of Modular Multilevel Converter based on bridge cells for 3-phase AC/AC converter," in *Electrical Machines and Systems (ICEMS), 2013 International Conference on*, 2013, pp. 1532-1537.

CHAPTER 8

Three-Phase AC-AC Hexagonal Chopper System with Heterodyne Modulation for Power Flow Control Enhancement

This chapter proposes a three-phase AC chopper system for the interconnection of various distributed generation (DG) farms or main utilities, to enhance active and reactive power flow control. The absence of an energy storage component in direct AC-AC converters makes the system footprint small and reliable. As an interface for different AC sources, the presented converter can be configured as star or delta. However, delta connection is preferred as it traps the potential zero-sequence current and reduces the current rating of the switching devices. In this way, the proposed converter resembles the hexagonal chopper, and it offers an inherent degree of freedom for output voltage phase-shifting. Considering scalability in high voltage applications, a new version of the hexagonal chopper with a half-bridge cell modular multilevel structure is developed. The modular multilevel AC hexagonal chopper (M2AHC) is operated in a quasi-2-level mode to suppress electro-magnetic interference (EMI) caused by high voltage switching. Quasi-2-level operation divides the voltage level transition into multi-steps, reducing voltage rise and fall rates (dv/dt) in high voltage applications. Then, heterodyne modulation is adopted for the presented chopper system, supplying a new degree of freedom to decouple phase and amplitude regulation. Based on this concept, a system control strategy is developed in the synchronous reference frame (SRF). Simulation and experimentation confirm the validity of the proposed approaches.

8.1 Background

Recently, distributed generation (DG) penetration into traditional power system has accelerated, and has been encouraged by increasing popularity and development of the smart grid. DG resources are operated as part of large grids as well as in islanding mode, called the microgrid. Although the microgrid concept is recent, it has received significant attention from academia and industry [1-5]. Solar and wind energy are being extensively integrated into grids via power electronic converters, where a DC-AC or a back-to-back voltage source converter (VSC) is preferred due to the energy storage buffer that offers side-to-side decoupling. Unlike the intermittent nature of renewable energy, conventional DGs such as synchronous generator arrays provide stable power output with full control over frequency and voltage amplitude. Therefore, these DG resources are widely employed to stabilize the AC grid or microgrid with considerable amounts of renewable energy incorporated. In AC power networks, active and reactive power flow control is facilitated by using the droop method which slightly refines the voltage amplitude and phase [6-8]. However, the control range is limited by line impedance, especially in long distance and meshed interconnections, where neither the synchronous generator nor the VSC is able to force the power flow in any specific branch beyond its terminals. In order to enhance power flow control ability at reduced cost, direct AC-AC conversion can be employed as the interfacing converter between critical DG or utility buses.

In direct AC-AC conversion, the matrix converter (MC) has attracted significant interest for its ability to regulate the frequency and phase without a DC-link. MC application in motor drives, power flow control and wind turbine interfacing are investigated in [9-11]. However, numerous switching devices, a complex modulation scheme combined with high switching and conduction losses, constrain the spread of the MC. Additionally, MC control and modulation depend on direct coupling of the input and output, leading to the increased possibility of system failure in fault conditions. Besides, the wide range frequency control function of MC is not needed in 50/60Hz grid devices.

The vector switching converter (VeSC) has a reduced number of switches and simplified modulation compared to the MC, at the expense of incorporating multi-throw input voltages generated from a bulky phase shift transformer, which in turn increases the size and cost of the overall system [12].

An AC chopper using bidirectional switches is a particular VeSC case with only a one throw input voltage [13]. Generally, the AC chopper can only change the voltage amplitude with a one throw input source and DC duty cycle modulation. In order to provide an additional degree of freedom for voltage synthesis, the widely used heterodyne principle in communication can be transposed to power converters. The heterodyne idea is based on trigonometric identities, where by inserting new frequency components into the modulating signal, new sinusoidal components and the relevant byproducts can be generated from the AC source. References [14] and [15, 16] are special cases that use the heterodyne principle for the VeSC and AC chopper respectively. However, 3rd order harmonic current is drawn from the input source in these schemes.

For high and medium power wind turbine interfacing applications, the hexverter originated from the back-to-back modular multilevel converter (MMC) by omitting the DC-link, as presented in [17]. However, weak decoupling exists since large DC cell capacitance and full-bridge cells are employed for voltage synthesis and reverse blocking. Consequently, the branch current comprises a large DC component to facilitate power transfer between the two AC sides and the AC components associated with frequencies of both AC sides and their interactions. The hexverter is suitable for interfacing future multi-megawatt variable speed wind-turbine generators due to the decoupling feature inherent from the use of DC capacitors. However, the incorporation of large DC capacitors makes it less competitive as a power flow controller between two synchronous AC grids.

This chapter presents a three-phase hexagonal AC chopper as an interfacing converter for interconnection between DG farms or utilities, and specifically, it can be used as an AC grid voltage regulator, flexible AC transmission system (FACTS) device, off-line programmable AC voltage source, etc. The hexagonal configuration of the AC chopper forms a delta connection of three phases, where zero-sequence current can be trapped. To increase the voltage and power rating, the basic hexagonal chopper is extended into a modular multilevel AC hexagonal chopper (M2AHC). Since the overall system is direct AC-AC conversion, the cell capacitors of the M2AHC are an AC type with low capacitance. Accordingly, the necessary arm inductance is small and may merge into just stray inductance. Quasi-2-level operation of the M2AHC is investigated to offer further cell capacitance reduction,

small voltage transient steps (less EMI), and consistent system control with a two level chopper. The heterodyne principle is employed to synthesize a phase-shifted output voltage from the input by cancellation of the byproducts between phases. Based on this idea, a multi-layer multi-loop system control scheme is developed in the SRF for the hexagonal chopper. The hexagonal chopper can be arranged as a back-to-back system if each AC network has this chopper at each terminal, doubling the control flexibility and adapting the voltage amplitude (the AC chopper is a step-down converter). However, a common step-up transformer is assumed at the converter output in this chapter to allow concentration on a single converter unit.

8.2 Proposed Three-phase Hexagonal Chopper System

In this section, the operational principles of the proposed hexagonal chopper and its extension - the M2AHC, are analysed. The two chopper system versions are equivalent from a system point of view, with a similar relationship as the 2-level VSC and the MMC in DC-AC applications.

8.2.1 Performance Analysis of the Hexagonal Chopper

The schematic of proposed three-phase hexagonal chopper is shown in Fig. 8-1. Six groups of series-connected insulated gate bipolar transistors (IGBT) as bidirectional switches are used to form a hexagonal ring. The switches are denoted as S_{xy} where x=*a*, *b*, *c* are the chopper phases; and *y*=1, 2 are the upper and lower switches respectively as in Fig. 8-1. The two IGBTs in each bidirectional switch are driven by the same signal, while the upper and lower switches of one phase are complementarily triggered from a pulse width modulation (PWM) scheme. {*A*, *B*, *C*} and {A_o, B_o, C_o} are three input and output terminals respectively. The risk of resonance between the line filters when zero-sequence current is drawn is avoided by the solid connection of terminal capacitors, in contrast to a three-wire star connection.

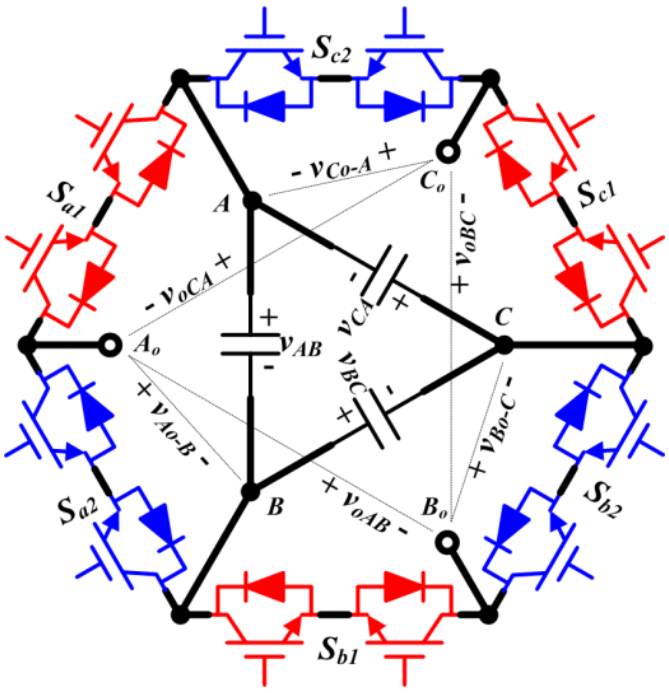


Fig. 8-1. Proposed three-phase hexagonal chopper (without filter).

In Fig. 8-1, each phase functions as a buck-type AC chopper, and the directly generated voltages are denoted as $\{v_{Ao\text{-}B}, v_{Bo\text{-}C}, v_{Co\text{-}A}\}$. $\{d_a, d_b, d_c\}$ are the duty cycles of the upper switches. $\{v_{AB}, v_{BC}, v_{CA}\}$ are the input line voltages. The output voltages $\{v_{Ao\text{-}B}, v_{Bo\text{-}C}, v_{Co\text{-}A}\}$ are related to input voltages $\{v_{AB}, v_{BC}, v_{CA}\}$ by the duty cycles of the upper switches as: $v_{Ao\text{-}B}=d_a v_{AB}$, $v_{Bo\text{-}C}=d_b v_{BC}$ and $v_{Co\text{-}A}=d_c v_{CA}$. Accordingly, the output line voltages $\{v_{oAB}, v_{oBC}, v_{oCA}\}$ are given by (8.1).

$$\begin{cases} v_{oAB} = v_{Ao-B} - v_{Bo-C} + v_{BC} = v_{AB} \cdot d_a + v_{BC} \cdot (1-d_b) \\ v_{oBC} = v_{Bo-C} - v_{Co-A} + v_{CA} = v_{BC} \cdot d_b + v_{CA} \cdot (1-d_c) \\ v_{oCA} = v_{Co-A} - v_{Ao-B} + v_{AB} = v_{CA} \cdot d_c + v_{AB} \cdot (1-d_a) \end{cases} \tag{8.1}$$

In normal operation, the duty cycles of the three phases are equal with the pure DC component denoted as D. Considering the sinusoidal input voltages in (8.2), where v_m and ω are the amplitude and angular frequency of the input voltage respectively, (8.1) can be consolidated into (8.3), with the definitions in (8.4).

$$\begin{cases} v_{AB} = v_m \cdot \cos \omega t \\ v_{BC} = v_m \cdot \cos(\omega t - \tfrac{2}{3}\pi) \\ v_{CA} = v_m \cdot \cos(\omega t + \tfrac{2}{3}\pi) \end{cases} \tag{8.2}$$

$$\begin{cases} v_{oAB} = A \cdot v_m \cdot \cos(\omega t + \Delta) \\ v_{oBC} = A \cdot v_m \cdot \cos(\omega t + \Delta - \tfrac{2}{3}\pi) \\ v_{oCA} = A \cdot v_m \cdot \cos(\omega t + \Delta + \tfrac{2}{3}\pi) \end{cases} \tag{8.3}$$

$$\begin{cases} A = \sqrt{3D^2 - 3D + 1} \\ \Delta = -\cos^{-1}\left(\dfrac{3D-1}{2A}\right) \end{cases} \tag{8.4}$$

Fig. 8-2 shows the plot of A and Δ (in degrees) varying with D. The hexagonal chopper operates similarly to a zig-zag transformer as it offers output voltage phase-shifting, that is, the flexibility for power flow control, which is an additional feature of the proposed configuration over the star connection which has only amplitude adjustment.

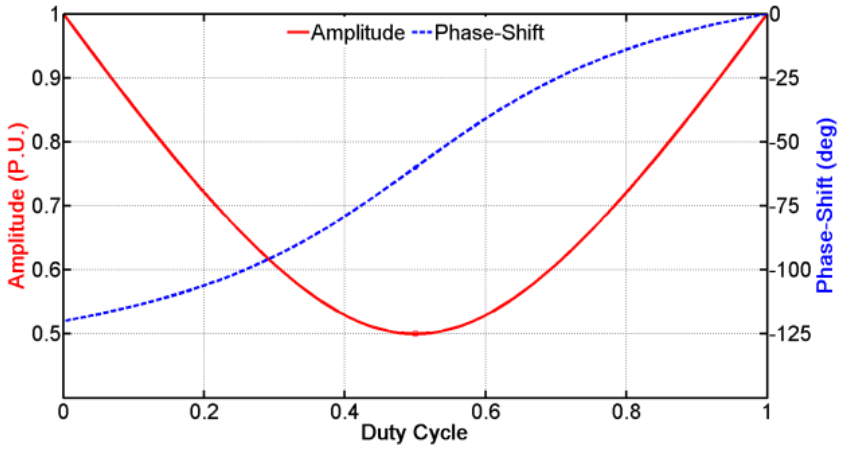


Fig. 8-2. Hexagonal chopper amplitude and phase of output line voltage *versus* DC duty cycle.

From Fig. 8-2, when D=0.5 is the initial operating point, the phase-shift range can be a maximum and bidirectional. However, phase regulation will also change the amplitude (minimum 0.5) due to the input voltage envelope in the constant duty cycle mode and the coupling between amplitude and phase control. This issue is investigated in a later section, to avoid the use of an on-load tap changer (OLTC) or an extra converter for voltage amplitude recovery (decoupling).

8.2.2 M2AHC with a Quasi-2-Level Operational Mode

In high and medium voltage applications, the presented hexagonal chopper requires series connection of bidirectional switches to operate in a typical two-level mode. In order to reduce the EMI generated from high frequency switching of high voltage levels and avoid uneven dynamic voltage sharing amongst series connected semiconductor devices (low reliability), M2AHC operation in a quasi-2-level mode has been developed, as depicted in Fig. 8-3, where the switches of Fig. 8-1 are replaced by a chain link of half-bridge cells and inductors in each arm to enable scalability to high power and high voltage applications. The cell capacitors in the

proposed M2AHC only sustain a pure AC voltage, allowing the use of small AC capacitors instead of large DC counterparts, as presented in the hexverter in [17]. The arm inductors, which limit the inrush current of the inner hexagonal ring during transient voltage mismatch between input voltage and the sum of the non-bypassed cell capacitor voltages, can be significantly reduced, compared with the MMC or hexverter. The quasi-2-level operation mode interpreted in Fig. 8-4 is adopted to minimize *dv*/*dt* stresses on output connected equipment. The proposed quasi-2-level operation divides voltage level transitions into multiple steps without significant compromise on duty cycle information. It facilitates orderly output voltage transitions from level '0' to level '1' (and vice versa) through artificially created intermediate voltage levels. These intermediate voltage levels enable sequential switching of the MMC cells of the upper and lower arms in and out of the power path. In this way, the voltage gradient (*dv*/*dt*) during switching transitions is greatly reduced; enhancing system reliability [18].

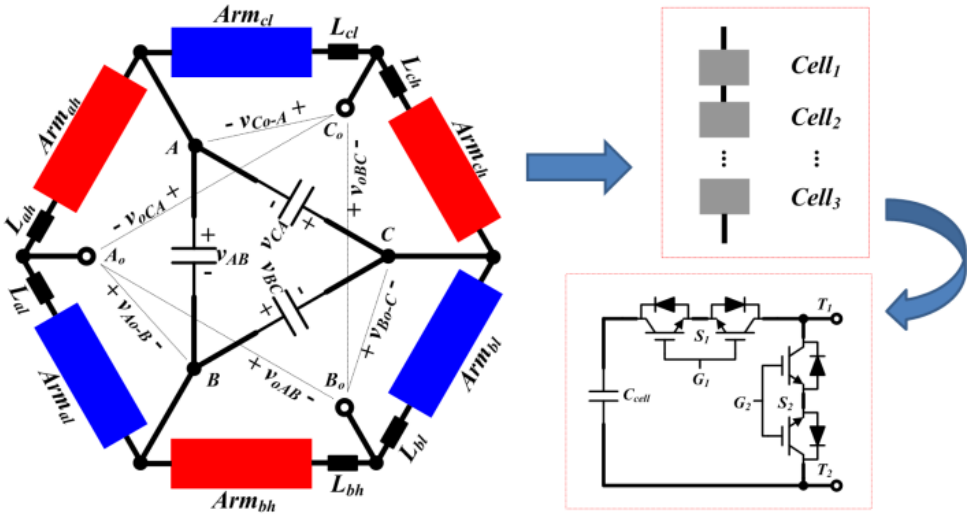
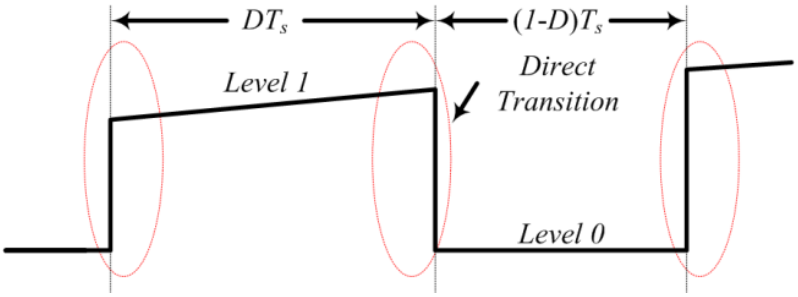
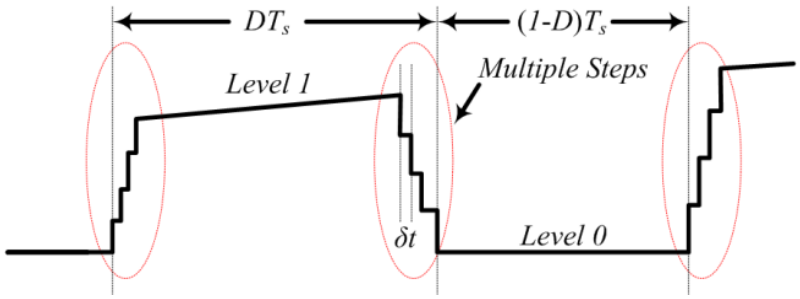


Fig. 8-3. Proposed M2AHC with its arm and cell structures.



(a)



(b)

Fig. 8-4. Comparison of (a) real-2-level and (b) quasi-2-level modes for AC chopper systems.

This discussion has shown that the proposed M2AHC is different from the hexverter [17], although topologically they look similar. The main differences are summarized as follows:

a) The M2AHC with half-bridge cells (with bidirectional switches) contains no large energy storage component; because the cell capacitor voltages are pure AC. Arm inductances are also small and may merge into stray inductance in a compact design. However, the hexverter uses full-bridge cells (with unidirectional switches) and incorporates a large DC capacitor in each cell [19].

b) The presented converter operates in a quasi-2-level mode, while the hexverter functions in a typical multilevel mode.

c) The proposed converter acts as an AC chopper from the system point of view, where duty cycle is the control input. But the hexverter is derived from the back-to-back MMC and can be viewed as an indirect AC-AC system.

d) The arm current in the M2AHC is discontinuous and transits between zero and the load current by multi-steps (di/dt is limited), while the hexverter (also MMC) maintains continuous arm current. Lower conduction losses are expected in the M2AHC.

e) Normally, only fundamental and high frequency currents flow in the M2AHC arm. However, circulating currents of the MMC or hexverter contain DC and 2^{nd} order components.

The use of bidirectional switches in the chopper system facilities reverse blocking capability for the half-bridge cell configuration under fault conditions.

Investigation of design issues for the M2AHC using quasi-2-level operation follows.

1) Parameter Selection

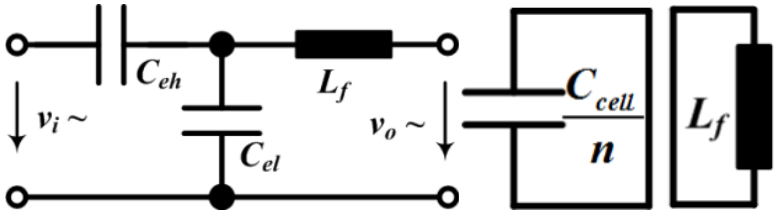
The input *C*-filter and output *LC*-filter are designed according to established approaches as discussed in [20], so are not repeated.

Similar to the conventional MMC, each M2AHC arm must be able to block the input voltage peak. This means each M2AHC phase must have *2n* cells (*n* cells per arm). During normal operation, the total number of series cells in the power path from the upper and lower arms at any instant must equal *n*. This means $n_u+n_l=n$, where n_u and n_l are the instantaneous number of cells selected from the upper and lower arms. When $n_u=0$ ($n_l=n$) and $n_l=0$ ($n_u=n$), the output poles (A_o, B_o and C_o) of the M2AHC are connected to level '1' and level '0' of their individual phases respectively. Thus, the maximum voltage stress per cell is limited to V_m/n, where V_m is input voltage peak and *n* is cell number per arm.

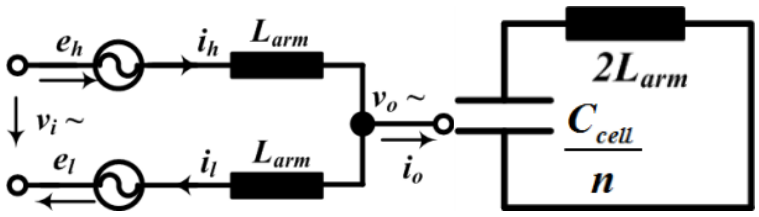
Fig. 8-4(b) shows that M2AC quasi-2-level operation is achieved by the modifications introduced to the typical two-level duty cycle in Fig. 8-4(a), hence, the total time at intermediate voltage levels, limits the maximum fundamental output voltage. This drawback can be minimized by making the dwell time at each intermediate voltage level sufficiently small to ensure smooth transition of the output voltage between levels '0' and '1'. Then system level consistency between the M2AHC and the 2-level hexagonal chopper is maintained. From Fig. 8-4(b), the duty cycle loss can be calculated by (8.5), where T_s is the switching period and δt is the step duration.

$$\tau = (n-1)\cdot \delta t / T_s \tag{8.5}$$

The step number is constrained by the duty cycle loss. Considering one typical application, with a $1kHz$ switching frequency and IGBT modules with a switching delay of about $5\mu s$ (Infineon FZ1500R33HL3); the step duration δt can be about $10\mu s$. In this case, if maximum tolerated duty cycle loss is 8%, at most 9 cells per arm (10-level waveform in the transition) is allowed according to (8.5). Such a limit is reasonable because the purpose of the M2AHC is not to track references as with the conventional MMC.



(a) (b)



(c) (d)

Fig. 8-5. Equivalent M2AHC model: (a) quasi-2-level transient model; (b) power loop in steady-state; (c) arm current model; and (d) inner branch model.

For the M2AHC design, another difference to the MMC is in the hexverter or quasi-2-level DC-AC converter [18], the weak decoupling of the DC-link affects calculation of cell capacitance and arm inductance.

In conventional converters, the DC cell capacitor is chosen based on switching ripple demand, while the M2AHC is a pure AC system, with AC capacitors. Considering the simplified M2AHC transient model in Fig. 8-5(a), C_{eh} and C_{el} are the equivalent capacitors of the non-bypassed cells in the upper and lower arms during quasi-2-level transitions. All n cell capacitors in each arm are either clamped to the input voltage or bypassed after a transition as in Fig. 8-5(b). C_{cell} and L_f are cell capacitance and output filter inductance. State equations can be established as in (8.6), from which the equivalent resonant frequency f_r between $C_{eh}//C_{el}$ and L_f must be between the fundamental frequency f_o and switching frequency f_{sw}, as in (8.7). If f_r is smaller than f_o (large C_{cell}), cell capacitor voltages cannot follow an increasing output voltage; while if f_r is larger than f_{sw} (small C_{cell}), high frequency oscillation will disturb the step voltage during transitions. Practically, a geometrical mean of the normalized frequencies is suggested, of the resonant frequency f_{r0} of C_{cell} and L_f as shown in (8.8). The M2AHC cell capacitor voltage is pure AC, while quasi-2-level operation of a conventional MMC uses DC cell capacitors to maintain a constant voltage. Thus the presented M2AHC is able to use smaller cell capacitors than in [18], under the same operating conditions.

$$\begin{cases} L_f(C_{eh}//C_{el})\cdot\dfrac{d^2v_c}{dt^2}+k\cdot v_c=v_i-v_o \\ \dfrac{n}{n-1}\geq\dfrac{C_{eh}//C_{el}}{C_{cell}}\geq\left[\dfrac{1}{floor(\frac{1}{2}n)}+\dfrac{1}{ceil(\frac{1}{2}n)}\right] \end{cases} \tag{8.6}$$

$$\begin{cases} 1/(2\pi\sqrt{\dfrac{n}{n-1}C_{cell}L_f}) > f_o \\ 1/(2\pi\sqrt{[\dfrac{1}{floor(½n)}+\dfrac{1}{ceil(½n)}]C_{cell}L_f}) < f_{sw} \end{cases} \tag{8.7}$$

$$\begin{cases} f_{r0} = 1/(2\pi\sqrt{L_f C_{cell}}) = \sqrt{N \cdot f_o \cdot f_{sw}} \\ N = \sqrt{\dfrac{n}{n-1}[\dfrac{1}{floor(½n)}+\dfrac{1}{ceil(½n)}]} \end{cases} \tag{8.8}$$

In a typical 2-level hexagonal chopper, the load current alternatively flows out of (into) one switch and its complement according to the duty cycle. Hence, pure fundamental current (in phase with load current) is carried by each arm. In the M2AHC, neglecting the quasi-2-level process, considering Fig. 8-5(c) and constant duty cycle *D*, the arm currents are expressed as in (8.9), which is in accordance with a 2-level chopper. Practically, a small phase-shift is introduced to upper and lower arm currents by the quasi-2-level transition delay. However, this will have no influence on the system performance since (8.10) (Kirchhoff's law) always holds (i_{cir} is the circulating current in the hexagonal ring).

$$\begin{cases} i_h = D \cdot i_o \\ i_l = -(1-D) \cdot i_o \end{cases} \tag{8.9}$$

$$\begin{cases} i_o = i_h - i_l \\ i_{cir} = ½(i_h + i_l) \end{cases} \tag{8.10}$$

The arm inductance is evaluated from Fig. 8-5(d). As analyzed, the arm current of M2AHC contains only a fundamental component. Since *n* cell capacitors are series connected at any instant, the inner branch characteristic impedance ζ can be obtained as in (8.11). In order to damp the high frequency inrush current (due to cell capacitor voltage summation error) and reduce the fundamental voltage drop on the arm inductance, trade-off is made based on the output power level and inner ripple current demand (current ratings for power devices) when selecting the characteristic impedance ζ, and L_{arm} can be specified according to:

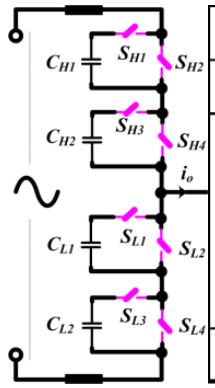
$$\zeta = \sqrt{2nL_{arm}/C_{cell}} \tag{8.11}$$

2) Voltage Balancing Strategy

The cell capacitor voltage balancing strategy can be explained using the illustrative example with two cells per arm in Fig. 8-6(a). By detecting the load current direction

and voltage differences between the relevant cell capacitors, the appropriate redundant switching states can be assigned to compensate the voltage errors [21]. Similar with the conventional MMC, the M2AHC output voltage with two cells per arm contains one intermediate voltage level which can be synthesized by multiple switch combinations (redundant switch states). The modulation strategy for the three-level M2AHC is interpreted as follows:

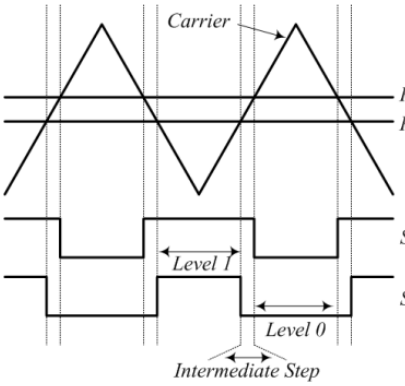
(1). The duty cycle command is transferred to the converter, denoted as Ref_1 in Fig. 8-6(c). The reference signal Ref_2 is calculated from Ref_1 and their subtraction determines the duration of the intermediate step, which is smaller than the original duty cycle.



(a)

V_o	S_{H1}	S_{H2}	S_{H3}	S_{H4}	S_{L1}	S_{L2}	S_{L3}	S_{L4}
Level 1	0	1	0	1	1	0	1	0
Intermed-iate Step	1	0	0	1	0	1	1	0
	1	0	0	1	1	0	0	1
	0	1	1	0	1	0	0	1
	0	1	1	0	0	1	1	0
Level 0	1	0	1	0	0	1	0	1

(b)



(c)

V_{H1}-V_{H2}	V_{L1}-V_{L2}	i_o	Switching States
+	+	+	01101001
+	-	+	01100110
-	+	+	10011001
-	-	+	10010110
+	+	-	10010110
+	-	-	10011001
-	+	-	01100110
-	-	-	01101001

(d)

Fig. 8-6. Interpretation of the modulation for three-level MMC based hexagonal chopper: (a) configuration for one phase; (b) output voltage level and relevant switch states; (c) modulating signal to define the voltage output states; and (d) voltage balancing strategy.

(2). According to the difference between Ref_1 and Ref_2. The pulse signals ST_1 and ST_2 are obtained. In Fig. 8-6(b), if ST_1 & ST_2 = 1, the two upper cells both generate 'zero' and output voltage is 'Level 1'; while if ST_1 || ST_2 =0, the two upper cells both give 'one', and output voltage is 'Level 0'. All remaining states belong to the intermediate

voltage level used for voltage balancing by taking into account the arm or output current direction.

(3). The redundant switch states for the intermediate output voltage level are assigned according to the output current direction and cell capacitor voltage difference in Fig. 8-6(d). For example, assuming the load current flows from the converter, if the voltage on C_{H1} is larger than that on C_{H2}, the upper arm switch state is '0110'; while if V_{L1} is smaller than V_{L2}, the lower arm should have a switch state of '1001'. In this analogy, the remaining states can be deduced.

An M2AHC (using quasi-2-level) with a larger number of cells can be modulated similarly to the illustrative example but with a more sophisticated software overhead for cell capacitor voltage sorting and switch state selection.

Since the quasi-2-level mode only introduces minor modifications to the duty cycle of the two-level AC chopper in Fig. 8-1, to generate intermediate voltage states, system level equivalence between them can be concluded. Therefore, the hexagonal chopper and M2AHC share the same control scheme at the system level, similar to the 2-level VSC and the MMC in DC-AC applications.

8.3 Heterodyne Modulation and System Control

The hexagonal chopper system has a problem, exposed in Fig. 8-2, where phase regulation simultaneously causes amplitude changes if the duty cycles are constrained to equal a DC value (as previously assumed). This is the same as with the zig-zag transformer, where OLTC is employed to adjust the amplitude. Also the minimum amplitude is 0.5, which means the voltage control range is limited. In order to overcome these drawbacks and improve system flexibility, a new degree of freedom for voltage synthesis is developed by exploiting the heterodyne principle, which is clarified by the trigonometric identity in (8.12).

$$\cos\alpha\cdot\cos\beta=\tfrac{1}{2}[\cos(\alpha-\beta)+\cos(\alpha+\beta)] \tag{8.12}$$

$$\begin{cases}\cos\omega t\cdot\cos(-2\omega t+\varphi)=\tfrac{1}{2}[\cos(\omega t-\varphi)+\cos(3\omega t-\varphi)]\\ \cos(\omega t-\tfrac{2}{3}\pi)\cdot\cos(-2\omega t+\varphi-\tfrac{2}{3}\pi)=\tfrac{1}{2}[\cos(\omega t-\varphi-\tfrac{2}{3}\pi)+\cos(3\omega t-\varphi)]\\ \cos(\omega t+\tfrac{2}{3}\pi)\cdot\cos(-2\omega t+\varphi+\tfrac{2}{3}\pi)=\tfrac{1}{2}[\cos(\omega t-\varphi+\tfrac{2}{3}\pi)+\cos(3\omega t-\varphi)]\end{cases} \tag{8.13}$$

Considering the fundamental input line voltage (positive sequence), the 2nd order harmonic component in the negative sequence is inserted into the modulating signal to generate a phase-shifted positive sequence fundamental together with a 3rd order

harmonic component (zero sequence) by-product that cannot propagate in a three-phase system. The derivation in (8.13) is equivalent to the even harmonic modulation (EHM) presented in [15], which is a special case of the heterodyne method.

Practically, the three-phase modulating signals are chosen as (8.14) with a range between 0 and 1. From (8.1), (8.2), (8.3), (8.13) and (8.14), by the cancellation of the zero-sequence components, the output phase voltage denoted as $\{v_{opA}, v_{opB}, v_{opC}\}$ can be calculated from (8.15) and (8.16).

$$\begin{cases} d_a = k_0 + k_2 \cos(-2\omega t + \varphi) \\ d_b = k_0 + k_2 \cos(-2\omega t + \varphi - \tfrac{2}{3}\pi), \\ d_c = k_0 + k_2 \cos(-2\omega t + \varphi + \tfrac{2}{3}\pi) \end{cases} \quad \text{with} \begin{cases} |k_0| + |k_2| \le 1 \\ 0 \le k_0 \le 1 \end{cases} \tag{8.14}$$

$$\begin{cases} v_{opA} = v_m [A_d \cos \omega t - A_q \sin \omega t] \\ v_{opB} = v_m [A_d \cos(\omega t - \tfrac{2}{3}\pi) - A_q \sin(\omega t - \tfrac{2}{3}\pi)] \\ v_{opC} = v_m [A_d \cos(\omega t + \tfrac{2}{3}\pi) - A_q \sin(\omega t + \tfrac{2}{3}\pi)] \end{cases} \tag{8.15}$$

$$\begin{cases} A_d = \tfrac{1}{2}(2k_0 - 1 + k_2 \cos\varphi) \\ A_q = -\dfrac{1}{2\sqrt{3}}(1 + \sqrt{3} k_2 \sin\varphi) \end{cases} \tag{8.16}$$

From this analysis, the introduced degree of freedom can regulate the input voltage direct component and generate a new controllable quadrature component, by which phase control can be achieved independent of amplitude regulation. k_0 is practically suggested to be around 0.5 to guarantee a maximum range for the 2nd order modulating signals.

From Fig. 8-2, the maximum and bidirectional power flow control range can be achieved around the initial point (zero power flow point) at half duty cycle. This point has an inherent -60 °phase shift and 0.5 amplitude gain compared with the input AC voltage due to the delta connection of the three phases. This voltage adaption issue can be overcome by a back-to-back configuration if each AC network is equipped with the presented chopper system. However, a 1:2 interfacing transformer with 60 °leading phase shift is assumed in the following parts to adapt the converter output voltage to the grid. This simplification allows the focus to be on the performance analysis of a single converter unit.

8.3.1 Arm Current under Heterodyne Modulation

With the presented heterodyne method, the arm currents for the hexagonal chopper and M2AHC are re-evaluated. From (8.9) and (8.14), the arm current (phase A) is

shown in (8.17), where I_m is load current peak value and β is the power factor angle. The circulating current is calculated in (8.18).

$$\begin{cases} i_{ah} = [k_0 + k_2 \cos(-2\omega t + \varphi)] \cdot I_m \cos(\omega t + \beta) \\ i_{al} = [k_0 - 1 + k_2 \cos(-2\omega t + \varphi)] \cdot I_m \cos(\omega t + \beta) \end{cases} \tag{8.17}$$

$$i_{cir} = (k_0 - ½) I_m \cos(\omega t + \beta) + ½ k_2 I_m [\cos(\omega t - \varphi - \beta) + \cos(3\omega t - \varphi + \beta)] \tag{8.18}$$

In (8.18), the circulating current of the presented hexagonal chopper and M2AHC contain fundamental and 3rd order zero-sequence components when heterodyne modulation is employed. Thus the line currents in the input and output terminals are only the fundamental (high frequency ripple can be readily filtered). However, if the chopper system is configured as a star, the neutral line must be used as a power path for the 3rd order current which will be drawn from the input current [15], otherwise, resonance on the input filter occurs. This is another advantage of using a delta connected hexagonal chopper. For the M2AHC, the arm current is still discontinuous and with a width-variant chopped shape after the insertion of AC components in the modulating signals. Since in the M2AHC, *n* cell capacitors are always activated, cell capacitor voltage is not influenced by heterodyne modulation.

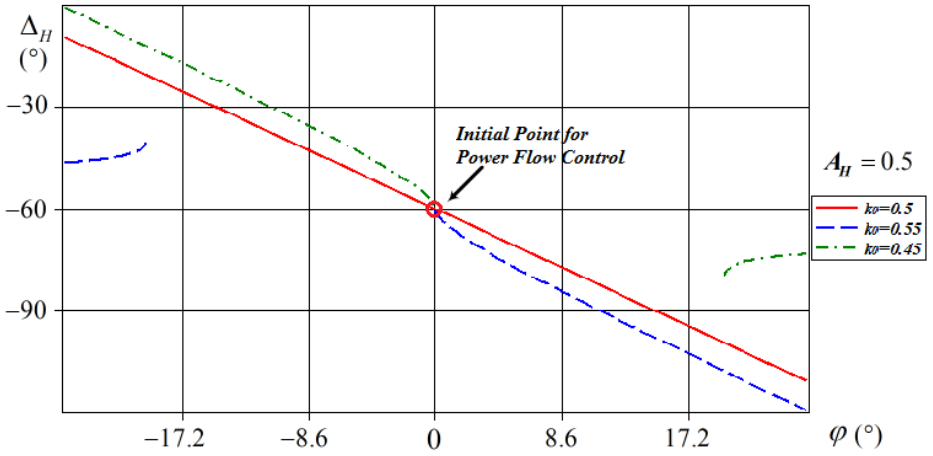
8.3.2 Power Flow Control Range with the Heterodyne Method

From (8.16), the output line voltage magnitude and angle can be expressed as in (8.19), after using the heterodyne method. Compared with (8.4) and Fig. 8-2, a new degree of freedom for voltage synthesis and power flow control is created by heterodyne modulation. Practically, the voltage variation range of the interfacing converter (hexagonal chopper in this chapter) is small in order to maintain the stability of the parallel AC system. This narrow range is sufficient for power flow control, which is different from a series compensation device with a fractional power rating, where the converter operational point varies significantly [22, 23]). Therefore, the output voltage amplitude gain for the presented hexagonal chopper is considered to be controlled constantly, as a first step. Then, with fixed k_0, the relationship between k_2 and φ is also fixed. Thus, the relevant phase-shift range can be obtained by evaluating (8.19). However, since it is difficult to derive an analytic solution for the transcendental equations, some graphical results are investigated, considering the range of k_0, k_2 in (8.14).

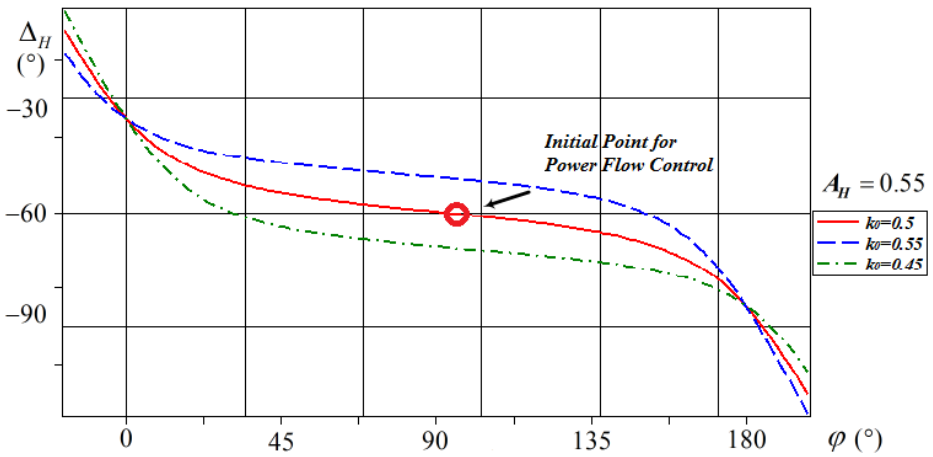
In Fig. 8-7(a), the voltage amplitude is controlled to be 0.5, and the output voltage phase-shift ranges of three typical cases (k_0=0.55, k_0=0.5, k_0=0.45) are plotted. The

inserted 2nd order modulating signal is capable of decoupling amplitude regulation and phase control. When the amplitude is fixed, sufficient phase-shift range around the initial point (-60°) is achieved for power flow control. A similar conclusion is drawn from Fig. 8-7(b) when the amplitude gain is set to 0.55. In Fig. 8-7(c), the amplitude can be maintained at 0.45 which is lower than the minimum of 0.5 without heterodyne modulation (Fig. 8-2), and output voltage phase-shift can also be implemented.

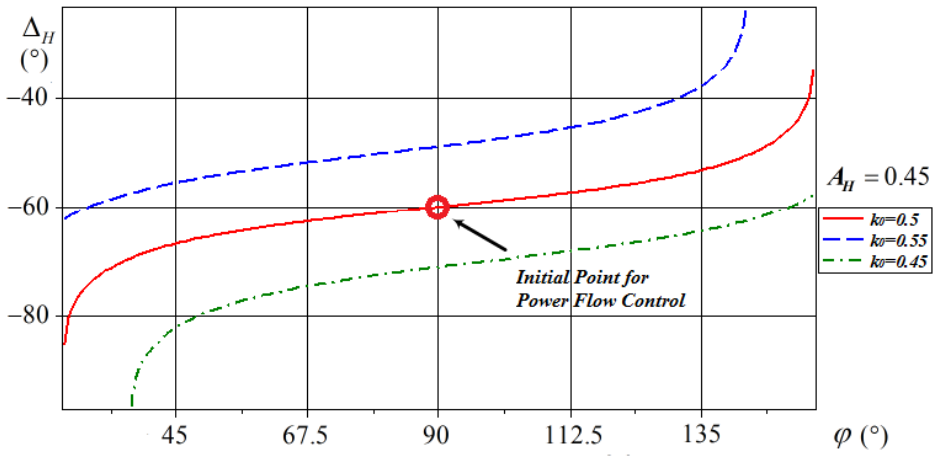
$$\begin{cases} A_H = \sqrt{\dfrac{1+3(2k_0-1)^2+3k_2^{\,2}}{4}+\dfrac{3(2k_0-1)k_2\cos\varphi+\sqrt{3}k_2\sin\varphi}{2}} \\ \Delta_H = -\cos^{-1}\left[\dfrac{\sqrt{3}(2k_0-1)+\sqrt{3}k_2\cos\varphi}{2A_H}\right]+30^\circ \end{cases} \tag{8.19}$$



(a)



(b)



(c)

Fig. 8-7. Phase-shift range with heterodyne modulation: (a) A_H=0.5; (b) A_H=0.55; and (c) A_H=0.45.

Typically, if $k_0 \approx 0.5$ ($0 \le k_2 \le 0.5$), the output bus voltage $v_b \approx v_i$ (v_i is the grid voltage) by using a 1:2 transformer, 60 ºleading, for voltage adaption, and a bus phase difference δ=2 º, the power flow output of proposed hexagonal chopper system can be obtained by (8.20), if inductive impedance dominates [1]. (The adaption transformer can be avoided with a back-to-back structure but is not considered in this chapter as previously mentioned.) Accordingly, Fig. 8-8 shows the theoretical power flow control range when using heterodyne modulation and normalized by (8.21).

$$\begin{cases} P = \dfrac{2A_H v_i v_b \sin(\delta + \Delta_H + \frac{1}{3}\pi)}{X} \\ Q = \dfrac{2A_H v_i [2A_H v_i - v_b \cos(\delta + \Delta_H + \frac{1}{3}\pi)]}{X} \end{cases} \tag{8.20}$$

$$\begin{cases} P_N = \dfrac{v_i v_b \sin\delta}{X} \\ Q_N = \dfrac{v_i (v_i - v_b \cos\delta)}{X} \end{cases} \tag{8.21}$$

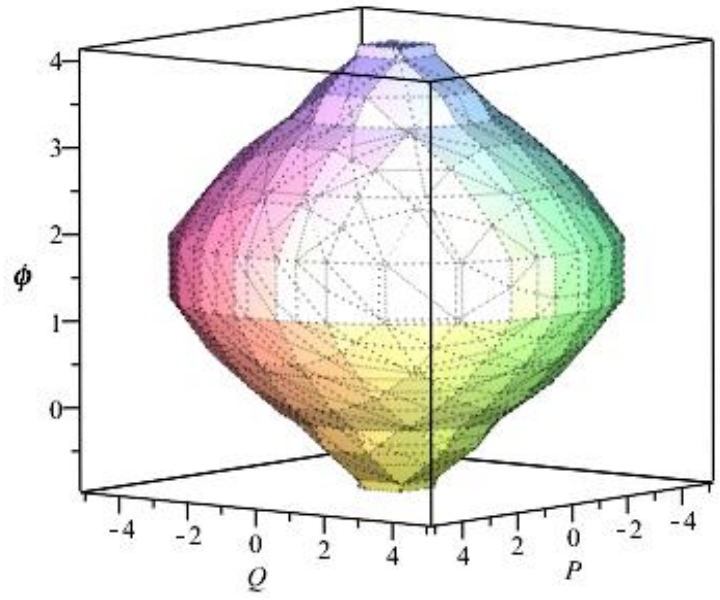


Fig. 8-8. Power control range (pu) with single-end hexagonal chopper (no back-to-back configuration) when k_0 and k_2 equal 0.5.

8.3.3 Control Scheme for the Hexagonal Chopper in the SRF

Fig. 8-9 summarizes the generic control systems that can be used for both versions of the presented AC choppers (2-level hexagonal chopper and quasi-2-level mode M2AHC) when used to connect two AC networks (DG to utility or utility to utility). After generating the voltage reference from the central power flow controller, the hexagonal chopper acts as an AC-AC VSC and is dominated by the voltage supporting controller (intermediate layer and inner current control layer). From (8.14), (8.15) and (8.16), the direct axis output voltage can be controlled by the DC component and direct component of the 2nd order signal in the modulating reference, while the quadrature axis voltage is only determined by the 2nd order quadrature signal.

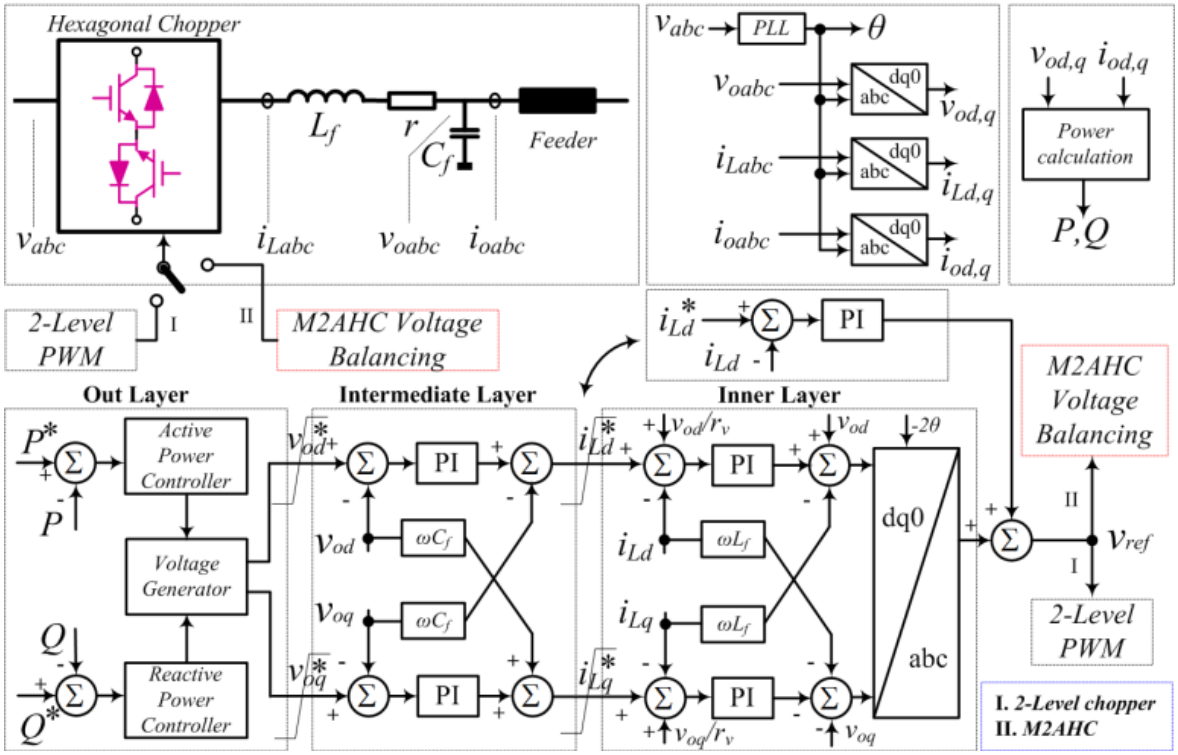


Fig. 8-9. Diagram of local controller for the hexagonal chopper.

The *d-q* equations describing the output voltage are shown in (8.22), from which the intermediate voltage control layer is designed. The terms $\{\lambda_d, \lambda_q\}$ defined in (8.23), can be obtained from the proportional-integral (PI) controller, as in (8.24). If $\{\rho_p, \rho_i\}$ are the PI parameters for the *d-q* axes, the current reference for the inner layer can be derived from (8.25), as in Fig. 8-9. The active damping factor $1/r_v$ is employed for load adaption and oscillation suppression. From (8.22) to (8.25), the close loop voltage transfer function G_{vo} is as in (8.26).

$$\begin{cases} \dfrac{dv_{od}}{dt} = \dfrac{i_{Ld} + \omega C_f v_{oq} - i_{od}}{C_f} \\ \dfrac{dv_{oq}}{dt} = \dfrac{i_{Lq} - \omega C_f v_{od} - i_{oq}}{C_f} \end{cases} \tag{8.22}$$

$$\begin{cases} \lambda_d = i_{Ld} + \omega C_f v_{oq} - i_{od} \\ \lambda_q = i_{Lq} - \omega C_f v_{od} - i_{oq} \end{cases} \tag{8.23}$$

$$\begin{cases} \lambda_d = \rho_p \cdot (v_{od}^* - v_{od}) + \rho_i \cdot \int (v_{od}^* - v_{od}) dt \\ \lambda_q = \rho_p \cdot (v_{oq}^* - v_{oq}) + \rho_i \cdot \int (v_{oq}^* - v_{oq}) dt \end{cases} \tag{8.24}$$

$$\begin{cases} i_{Ld}^{*} = \lambda_d - \omega C_f v_{oq} + v_{od} / r_v \\ i_{Lq}^{*} = \lambda_q + \omega C_f v_{od} + v_{oq} / r_v \end{cases} \tag{8.25}$$

$$G_{vo} = \frac{v_{od}}{v_{od}^{*}} = \frac{v_{oq}}{v_{oq}^{*}} = \frac{\rho_i + s\rho_p}{\rho_i + s(1/r_v + \rho_p) + s^2 C_f} \tag{8.26}$$

Similarly, the inner layer current controller is derived from (8.27), where r is the filter inductor resistance and $\{v_{cond}, v_{conq}\}$ is the converter output voltage before filtering. By the same derivation as for the intermediate control layer, the hexagonal chopper reference signal $\{v^{*}_{con.d}, v^{*}_{con.q}\}$ and close loop inductor current transfer function G_{iL} can be interpreted from (8.28) and (8.29) respectively, where $\{\sigma_p, \sigma_i\}$ are the PI parameters for the current controller and $\{\chi_d, \chi_q\}$ are the PI controller output.

$$\begin{cases} \dfrac{di_{Ld}}{dt} = -\dfrac{r}{L_f} i_{Ld} + \dfrac{v_{con.d} - v_{od} + \omega L_f i_{Lq}}{L_f} \\ \dfrac{di_{Lq}}{dt} = -\dfrac{r}{L_f} i_{Lq} + \dfrac{v_{con.q} - v_{oq} - \omega L_f i_{Ld}}{L_f} \end{cases} \tag{8.27}$$

$$\begin{cases} v_{con.d}^{*} = \chi_d - \omega L_f i_{Lq} + v_{od} \\ v_{con.q}^{*} = \chi_q + \omega L_f i_{Ld} + v_{oq} \end{cases} \tag{8.28}$$

$$G_{iL} = \frac{i_{Ld}}{i_{Ld}^{*}} = \frac{i_{Lq}}{i_{Lq}^{*}} = \frac{\sigma_i + s\sigma_p}{\sigma_i + s(r + \sigma_p) + s^2 L_f} \tag{8.29}$$

According to (8.14) and (8.16), $\{v^{*}_{con.d}, v^{*}_{con.q}\}$ are transformed to $\{v^{*}_{con.d}, -v^{*}_{con.q}\}$ and inverse Park transformed with -2θ (θ is from the fundamental phase locked loop, PLL from the input voltage) rotational speed. The resultant modulating signal is in the 2nd order negative sequence.

Since the direct axis voltage can also be regulated by the DC component of the duty cycle, an additional parallel loop using a PI controller is inserted to further compensate the direct voltage output. It is located in the inner control layer and shares the current reference with the previous current controller. This controller actually determines the DC modulating signal. Practically, this loop is set to be much slower than the 2nd order harmonic modulation loops. The sum of the DC component and 2nd order signal gives the final reference for the chopper system.

Based on this system control strategy, the final reference signal v_{ref} for the typical 2-level hexagonal chopper, is directly transferred to a PWM module to generate the

gate signals; while for the M2AHC, v_{ref} is used as the reference for the cell capacitor voltage balancing scheme (Fig. 8-6).

8.4 Discrete Drive to Remove Dead-Band Effect

In previous sections, an integrated drive scheme (two IGBTs are triggered by the same signal) for bidirectional switches is assumed to make the system more readily acceptable. Practically, dead-band time will cause voltage spikes in both the 2-level hexagonal chopper and the M2AHC with integrated drive, when both switches are turned off. Generally, in all direct AC-AC applications with integrated controlled bidirectional switches, any dead-band time will cut off all paths for current flow, leading to IGBT high voltage stresses. This issue has not been fully addressed in previous papers on direct AC-AC conversion using bidirectional switches [15, 16].

To overcome this issue without adding any snubbers, the integrated drive scheme should be modified but without influencing the considered performance. In Fig. 8-10, different operational modes of the bidirectional switch are displayed, when separate gate signals are employed. Fig. 8-10(a) shows the integrated drive situation where bidirectional reverse voltage blocking is addressed; Fig. 8-10(b) represents the reverse current blocked state when G_1 is always off; while in Fig. 8-10(c), the bidirectional switch reverts to a single IGBT if G_1 is turned on constantly.

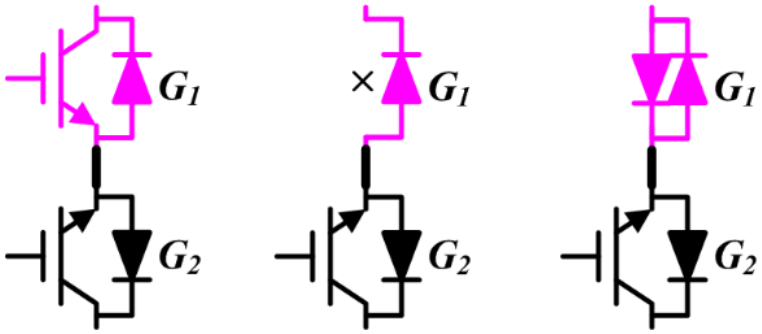


Fig. 8-10. Bidirectional switch with two series IGBTs: (a) integrated drive; (b) reverse-blocking state; and (c) reverse conduction state.

A discrete drive scheme without reverse blocking ability should be considered to avoid the dead-band effect. The two IGBTs sustain the reverse voltage alternatively due to the input voltage polarity. Thus, each IGBT can be maintain in conduction depending on the input polarity as in Fig. 8-10(c), to provide an extra current path during the dead-band time, thus eliminating any voltage spikes. With this approach,

the presented converter can be decoupled into two chopper units with unidirectional switches as shown in Fig. 8-11.

This discrete drive scheme does not change AC chopper system performance. For a 2-level converter, an input voltage transducer should be added. However, since M2AHC cell capacitor voltages are necessarily for their voltage balancing, voltage polarity can be derived by the average cell capacitor voltage. Thus a dedicated voltage transducer is not needed. Additionally, the total switching of the power switches is nearly halved by the discrete drive scheme (switching losses are reduced because the unblocked IGBT in the integrated drive always experiences zero voltage switching – ZVS).

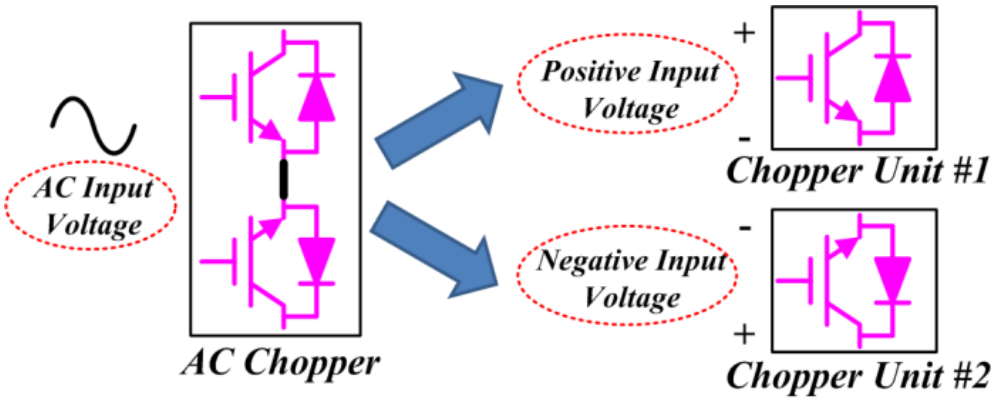


Fig. 8-11. Decoupling principle of the AC chopper by using discrete drive scheme for the bidirectional switches.

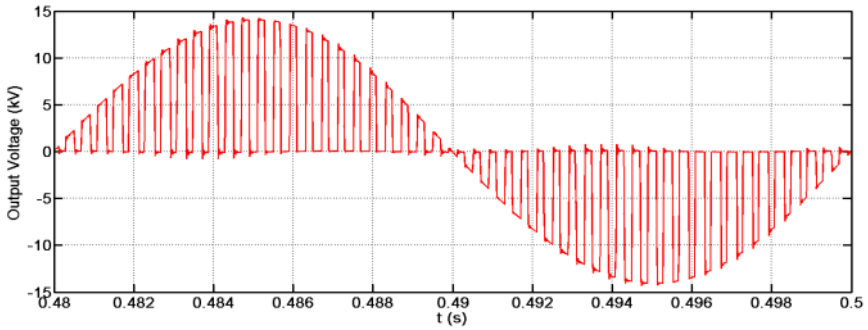
8.5 Simulation and Experimental Results

To verify the operational principle and voltage balancing scheme for the M2AHC, simulation on a three-phase 5-level (four cells per arm) model and experimentation on a single-phase 3-level test rig, have been carried out.

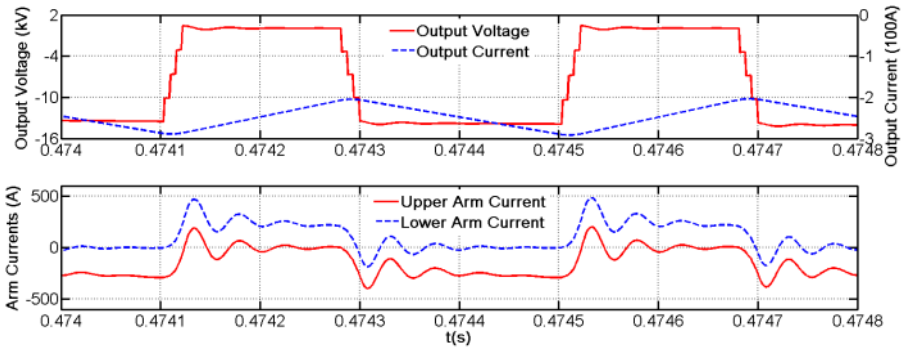
The heterodyne control scheme (system level) for the proposed hexagonal chopper system is verified experimentally on a three-phase 2-level mode prototype.

8.5.1 Simulation Tests

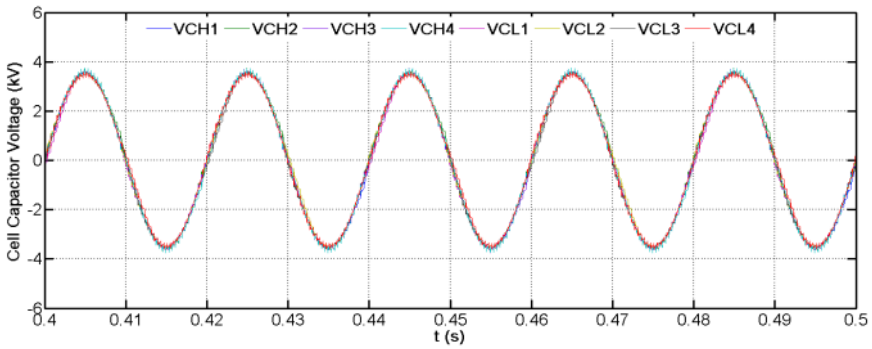
An illustrative four-cell version (five-level transitions) of the presented M2AHC has been simulated in Matlab/Simulink with following specifications: input line voltage: $10kV$ (RMS); input C-filter: $10\mu F$, cell capacitor: $10\mu F$, arm inductor: $10\mu H$, switching frequency: $2.5kHz$, output filter inductor: $15mH$, output filter capacitor: $100\mu F$, active power load: $5.4MW$, reactive power load: $2.1MVAr$. A composite modulating signal with k_0=0.5, k_2=0.12, φ=25 °and a $10\mu s$ step duration for the quasi-2-level mode is used in this model.


Output Voltage (kV)
t (s)

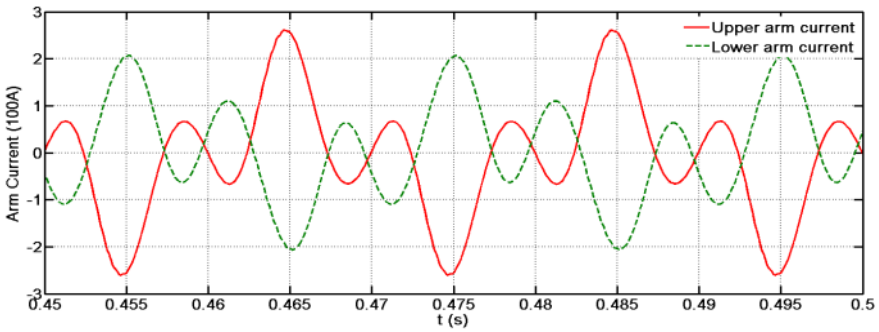
(a)


Output Voltage
Output Current
Output Voltage (kV)
Output Current (100A)
Upper Arm Current
Lower Arm Current
Arm Currents (A)
t(s)

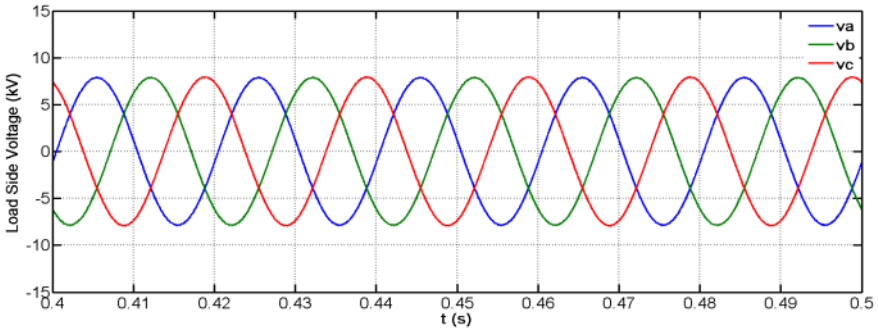
(b)


VCH1
VCH2
VCH3
VCH4
VCL1
VCL2
VCL3
VCL4
Cell Capacitor Voltage (kV)
t (s)

(c)


Upper arm current
Lower arm current
Arm Current (100A)
t (s)

(d)



(e)

Fig. 8-12. Simulation results: (a) chopped output voltage for one phase; (b) quasi-2-level mode with 5-step voltage transition and output/arm currents; (c) voltage balancing results; (d) upper and lower arm currents after moving average filter; and (e) three-phase output voltage.

The output voltage waveform in Fig. 8-12(a) shows that the presented M2AHC operates in a chopper mode with duty cycle as the control input. Zoomed versions of the output voltage together with the output and arm currents are displayed in Fig. 8-12(b). The use of quasi-two-level operation introduces intermediate voltage steps to avoid high voltage level switching. Thus, reduced *dv/dt* is impressed on the output connected load. Also, Fig. 8-12(b) shows that the M2AHC in a quasi-2-level mode simultaneously conducts load current through the upper and lower arms only during transitions of the output phase, via the artificially induced intermediate voltage levels; otherwise, the entire load current is conducted either through an upper or lower arm. In Fig. 8-12(c), the input voltage is equally shared by the eight cell capacitors, verifying the proposed voltage balancing scheme. Small AC capacitors based on (8.8) are sufficient for the proposed ratings (10*kV* and 6 *MVA*). Fig. 8-12(d) displays the moving averaged upper and lower arm currents which contain fundamental and 3rd order harmonics as in section III. From (8.17) the fundamental currents of the two arms are not necessarily equal. High quality post-filter three-phase output voltage from the M2AHC is demonstrated in Fig. 8-12(e).

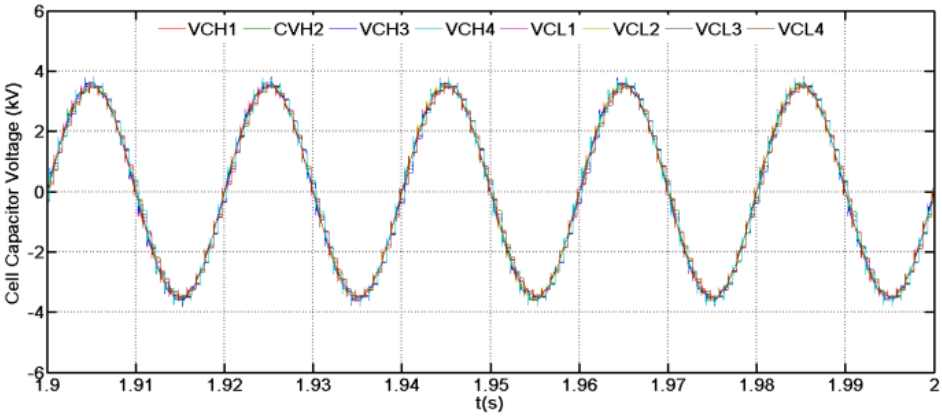
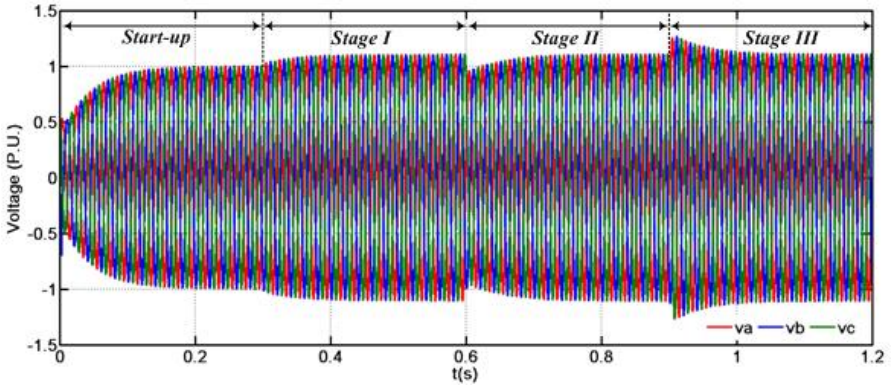
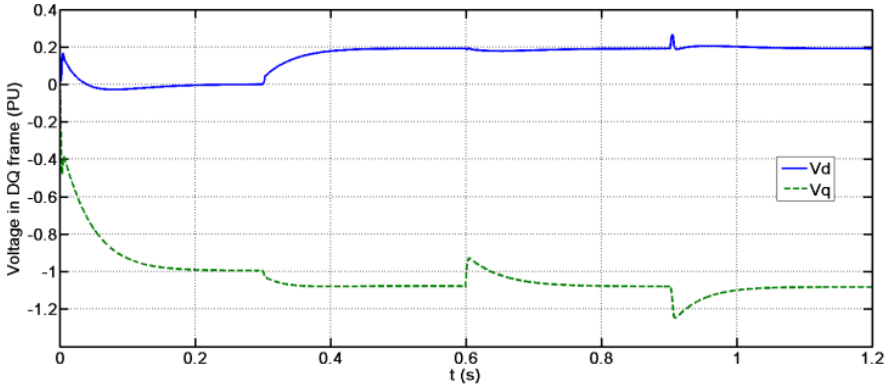


Fig. 8-13. Voltage balancing for a zero power factor condition.

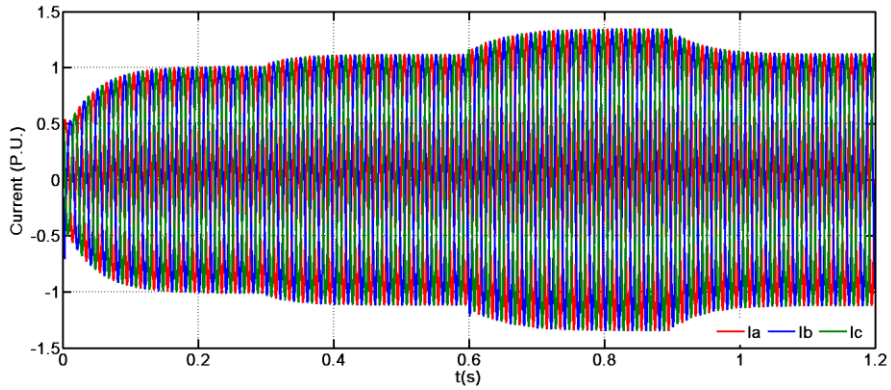
The voltage balancing results can be further examined in Fig. 8-13 under a zero power factor condition, which is the most challenging situation for modular multilevel based converters (such as the conventional MMC). The cell capacitor voltages remain stable and balance. This verifies that the proposed M2AHC is able to survive any arbitrary power factor condition, given Fig. 8-12(d) and Fig. 8-13 represent the two extreme conditions (nearly unity and zero power factors).



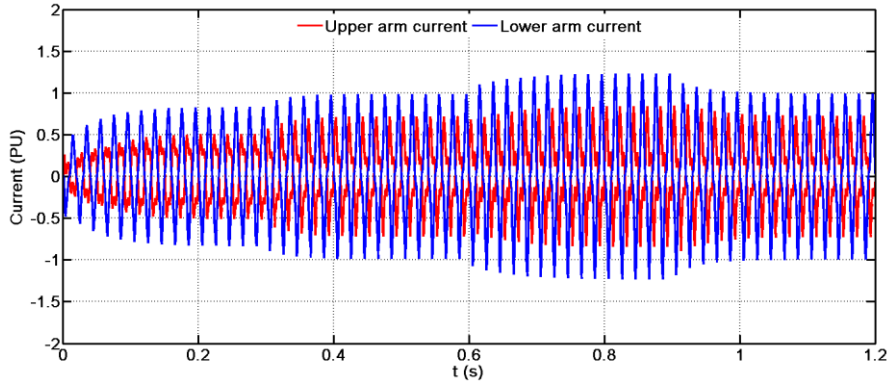
(a)



(b)



(c)



(d)

Fig. 8-14. Voltage command and power load transient processes for the proposed hexagonal chopper during a voltage supporting mode: (a) output voltage in the time domain; (b) output voltage in the SRF; (c) load current; and (d) moving-averaged arm current for one phase.

In order to evaluate the transient process, the post-filter voltage of the model is examined under step output voltage changes. In Fig. 8-14, during 0 to 0.3s, 1pu voltage is established; then the voltage control command is stepped to 1.1pu with a positive 10^{o} phase shift at 0.3s; the load power is step increased to 1.2pu and recovered to 1pu at 0.6s and 0.9s respectively. Fig. 8-14(a) and (b) show the output voltage waveforms in time domain and the SRF during the transient. Fig. 8-14(c) and (d) show the load current and moving-averaged arm current (the two arm currents are not necessarily equal, according to (8.17)). The effectiveness of the control strategy in Fig. 8-9 is confirmed by these results. The cell capacitor voltage remains as in Fig. 8-12(d) (or Fig. 8-13) during the transient processes because the cell capacitor voltage sum for one arm is always equal to the input voltage and each cell capacitor voltage is uniformly distributed due to the voltage balancing strategy.

Based on the theoretical discussion in section II and these results, it is concluded that the M2AHC performs like a typical two-level AC chopper, except for the employed

half-bridge cells which enable the generation of a step voltage transition between zero and the instantaneous peak (positive or negative). The adopted voltage balancing strategy ensures the uniform distribution of the input voltage across the cell capacitors, thus avoiding the need for series device connection in medium and high voltage applications.

8.5.2 Experimental Results

1) Modulation and Voltage Balancing for the M2AHC

Based on the previous simulation, the voltage balancing scheme and open loop performance of the M2AHC are further verified on a single-phase prototype with two cells per arm, as in Fig. 8-15. The Infineon TriCore 1796B DSP is employed as the controller. The specifications are as follows: input voltage: 240V (RMS), IGBT: FGA20S120M (1.2kV, 20A), switching frequency: 2.5kHz, power rating: 1.2kVA, input C-filter: 10μF, cell capacitor: 10μF, output filter inductor: 10mH, output filter capacitor: 100μF, and load: series 10mH and 10Ω.

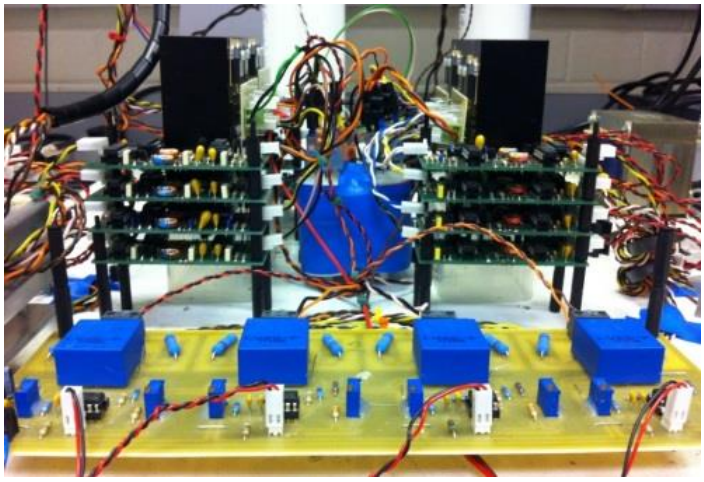


Fig. 8-15. Experiment setup photograph of the single-phase M2AHC with two cells per arm.

Fig. 8-16(a) shows the effective gate signals for the lower switches in each cell. The upper and lower arms operate complementarily (chopper) and the small edge durations are the quasi-2-level mode transition. The generated output voltage with an intermediate step and the arm currents are displayed in Fig. 8-16(b), where the arm currents are discontinuous for the proposed M2AHC, and the quasi-2-level operation slows the voltage rise and fall rate of the chopped edge. Fig. 8-16(c) and (d) are the fundamental period time based waveforms of the output voltage and arm currents respectively. The voltage balancing strategy developed in 8.2.2 for the M2AHC is

verified by Fig. 8-16(e) since the four cell capacitor voltage waveforms all coincide with each other.

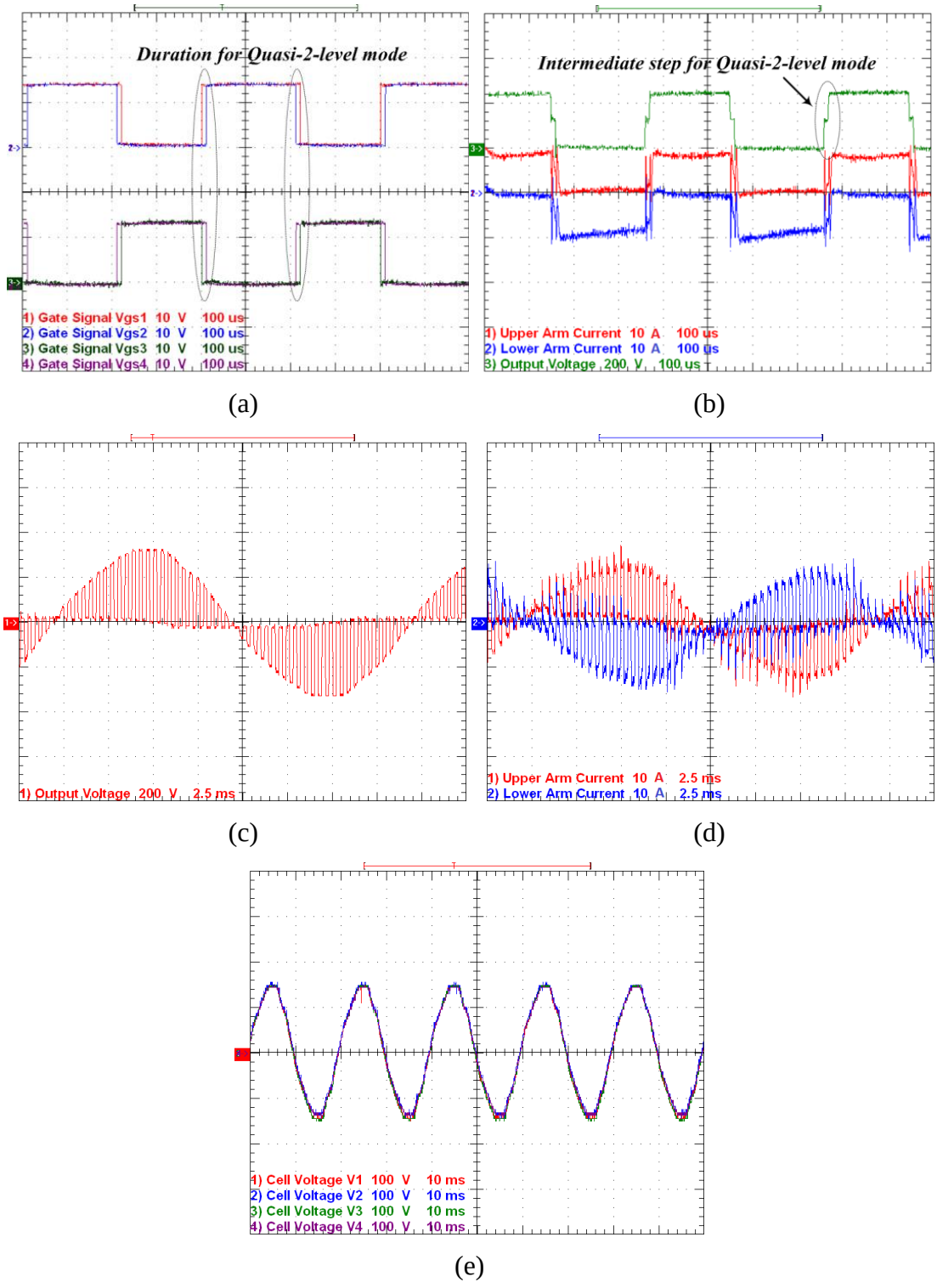


Fig. 8-16. Test results for a single-phase M2AHC with 2 cells per arm: (a) effective gate signals for lower switches in 4 cells; (b) interaction between output voltage (with intermediate step) and arm currents at switching period time base; (c) output voltage under fundamental period time base; (d) arm currents under fundamental period time base; and (e) cell capacitor voltage balancing results.

2) System Control with the Heterodyne Method

To verify the system control scheme developed in section 8.3 part C, a 2-level hexagonal chopper is assessed, where the experiment setup photograph is seen in Fig. 8-17. The input and output buses are interfaced by two three-phase transformers with all reference terminals accessible for voltage adaption. The TI DSP TMS320F28335 is employed as the controller. Specification of the prototype are: grid voltage: 110V (line-to-line RMS, three-phase), IGBT: FGA20S120M (1.2kV, 20A), switching frequency: 2.5kHz, power rating: 1.2kVA, input filter capacitor: 10μF, output filtering inductor: 10mH, and output filter capacitor: 100μF.

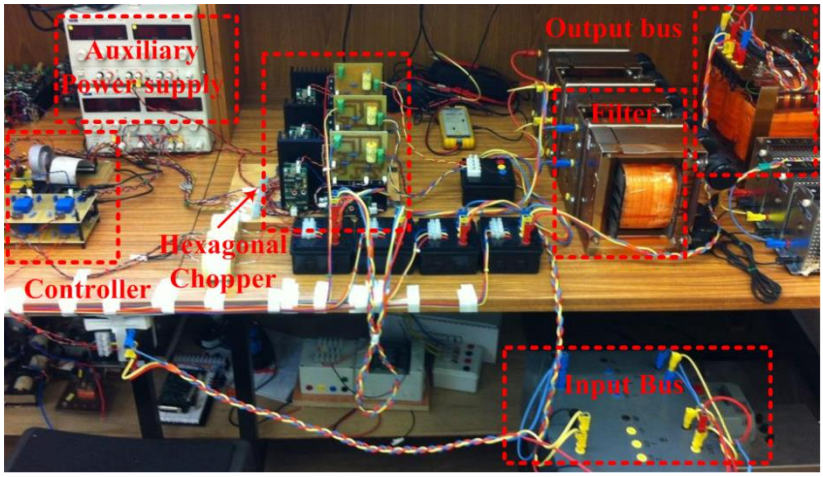
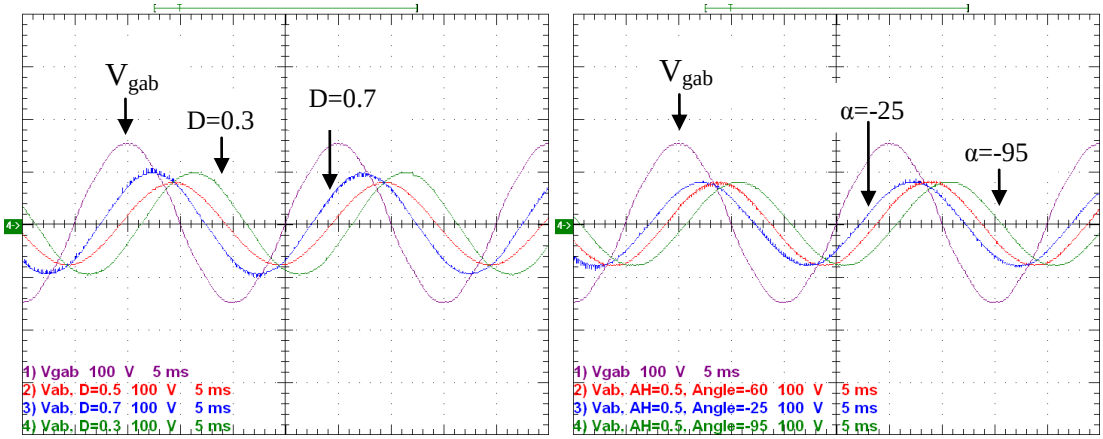


Fig. 8-17. Photo of the experiment setup for the hexagonal chopper system.



(a) (b)

Fig. 8-18. Comparison of voltage synthesis ability of the hexagonal chopper: (a) constant duty cycle and (b) heterodyne method.

Initially, the voltage synthesis ability of the hexagonal chopper is demonstrated by a standalone mode test, where heterodyne modulation and conventional constant duty cycle methods are employed. In Fig. 8-18(a), output voltage phase-shift causes

amplitude changes simultaneously when the duty cycle is constant. This is because the output voltage always falls within the envelope formed by three-phase input voltage. In Fig. 8-18(b), with heterodyne modulation, the amplitude can be controlled constantly independent of phase-shift as described mathematically by (8.15), (8.16) and (8.19). When the heterodyne method is used, 3rd order current circulates in the hexagonal ring as discussed, which can be verified by Fig. 8-19 (the waveform is not discontinuous because the delta connected input *C*-filter current is also included). From (8.17) and (8.18), the fundamental currents in the upper and lower arms are in opposite direction with different amplitudes; while the 3rd order components are equal, allowing trapping of the zero-sequence current.

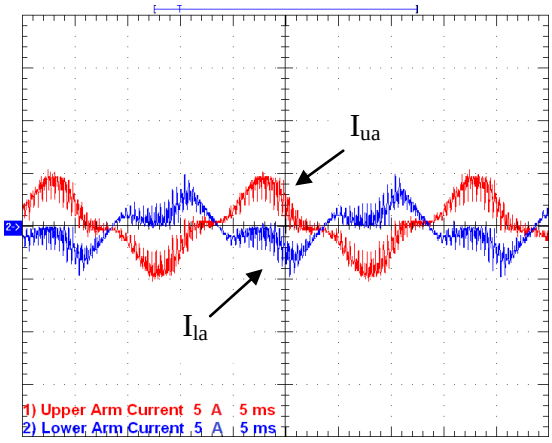


Fig. 8-19. Arm currents (plus input C-filter) under heterodyne modulation (A_H=0.5, Δ_H=-25°).

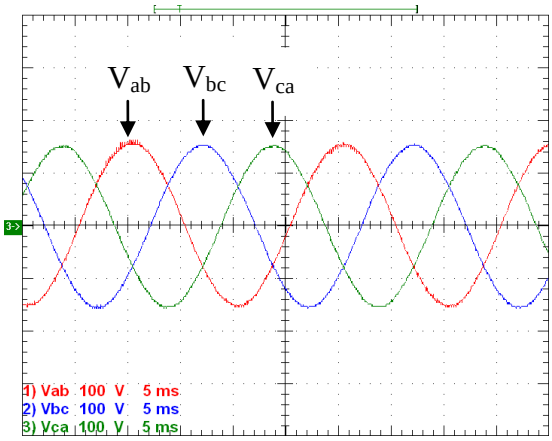
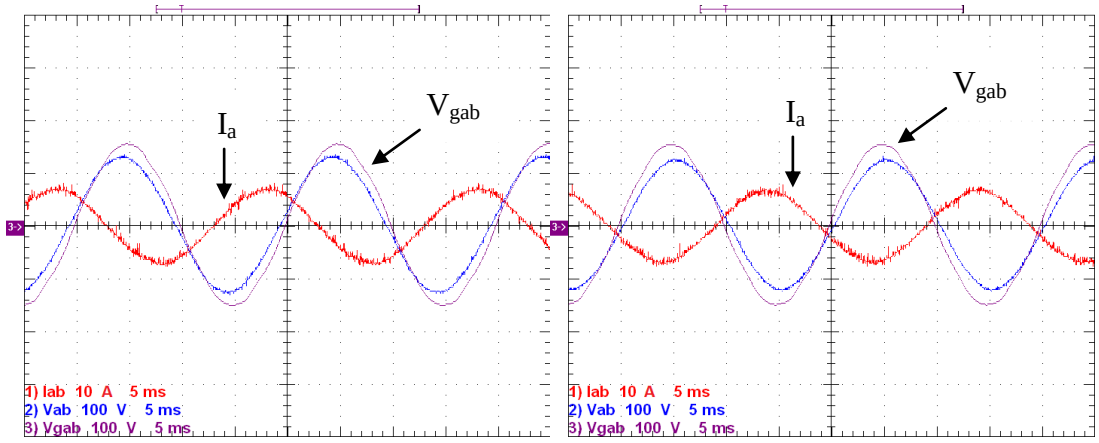


Fig. 8-20. Three-phase output voltage at transformer terminals, with zero power flow.

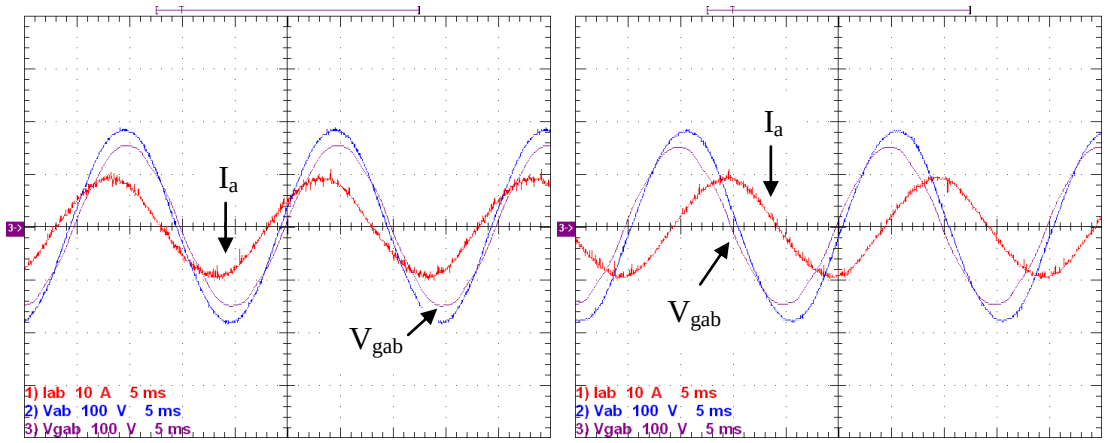
To further verify the heterodyne control strategy, the chopper is feed from the grid and its output is connected back to the grid through a 1:2 transformer with a 60° phase shift, leading. Since the power controller that can slightly refine the voltage reference is not considered in this chapter, a 3Ω resistor and $3mH$ inductor are

inserted as the line impedance when the voltage reference is manually changed (with large amplitude and phase errors). Fig. 8-20 shows the zero power flow situation, where the three-phase output bus voltage is the same as the grid voltage. In Fig. 8-21, A_H is set to 0.4. Power flow control, when the output bus voltage phase is 10 ºleading and 10 º lagging to the grid, are demonstrated, respectively. Similarly, if the output voltage gain is controlled as 0.6, ±10 º phase error can still be regulated by the proposed hexagonal chopper system, and the corresponding power flow control results are illustrated by Fig. 8-22. These results verified the decoupling and the extended voltage synthesis range (on both phase-shift and amplitude) of the heterodyne modulation in Fig. 8-7.



(a) (b)

Fig. 8-21. Power flow control with hexagonal chopper: (a) A_H=0.4, δ=10 ºand (b) A_H=0.4, δ=-10 º.



(a) (b)

Fig. 8-22. Power flow control with hexagonal chopper: (a) A_H=0.6, δ=10 ºand (b) A_H=0.6, δ=-10 º.

8.6 Summary

This chapter has proposed two versions of a three-phase hexagonal chopper system dedicated to the enhancement of power flow control in AC power networks. The first hexagonal chopper version consists of six bidirectional switches connected end to end without energy storage components. For scalability to high voltage applications, the second version, called the modular multilevel AC hexagonal chopper (M2AHC), was developed, based on the MMC switch voltage sharing concept. The operational principle, modulation and control of both versions were described and substantiated using simulations and experimentation. The contributions of this chapter are summarized as follows:

- The hexagonal chopper achieves direct AC-AC conversion with a small footprint, reduced switch count and control complexity compared to the matrix converter, which makes it attractive as power flow controller between AC networks. However, direct AC-AC converters are not proposed for interfacing wind turbines due to the lack of side-to-side decoupling.
- The proposed M2AHC employs significant smaller AC cell capacitance and arm inductance than the hexverter, where large DC capacitance and arm inductance are used.
- In high voltage applications, quasi-2-level operation of the M2AHC divides the voltage transition into multi-steps without significantly compromising maximum output voltage, slowing the voltage transition rate (dv/dt). Redundant switching states are assigned for voltage balancing.
- Heterodyne modulation with an inserted 2^{nd} order negative sequence component, decouples phase and amplitude regulation. It also extends the power flow control range.
- Heterodyne modulation requires 3^{rd} order zero sequence current to flow in the power path. Since the proposed converters are delta connected, this current can be trapped in the inner hexagonal ring, so will not influence the line current. If the star configuration is employed, the neutral line is used to provide a path to circulate the 3^{rd} order current. Otherwise, the input filter will resonate.

A back-to-back configuration with the hexagonal chopper or M2AHC can be formed at the PCC (point of common coupling) to adapt the voltage and double the control flexibility when each AC grid terminal is equipped with the proposed converter.

References

[1] R. Majumder, A. Ghosh, G. Ledwich, and F. Zare, "Power Management and Power Flow Control With Back-to-Back Converters in a Utility Connected Microgrid," *Power Systems, IEEE Transactions on,* vol. 25, pp. 821-834, May 2010.

[2] C. Changhee, J. Jin-Hong, K. Jong-Yul, K. Soonman, P. Kyongyop, and K. Sungshin, "Active Synchronizing Control of a Microgrid," *Power Electronics, IEEE Transactions on,* vol. 26, pp. 3707-3719, Dec 2011.

[3] Y. Xunwei, S. Xu, N. Xijun, and A. Q. Huang, "System Integration and Hierarchical Power Management Strategy for a Solid-State Transformer Interfaced Microgrid System," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 4414-4425, Aug 2014.

[4] M. A. Zamani, T. S. Sidhu, and A. Yazdani, "Investigations Into the Control and Protection of an Existing Distribution Network to Operate as a Microgrid: A Case Study," *Industrial Electronics, IEEE Transactions on,* vol. 61, pp. 1904-1915, Apr 2014.

[5] P. C. Loh, L. Ding, C. Yi Kang, and F. Blaabjerg, "Autonomous Operation of Hybrid Microgrid With AC and DC Subgrids," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2214-2223, May 2013.

[6] C. N. Rowe, T. J. Summers, R. E. Betz, D. J. Cornforth, and T. G. Moore, "Arctan Power - Frequency Droop for Improved Microgrid Stability," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 3747-3759, Aug 2013.

[7] I. U. Nutkani, L. Poh Chiang, and F. Blaabjerg, "Droop Scheme With Consideration of Operating Costs," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1047-1052, Mar 2014.

[8] C. T. Lee, C. C. Chu, and P. T. Cheng, "A New Droop Control Method for the Autonomous Operation of Distributed Energy Resource Interface Converters," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 1980-1993, Apr 2013.

[9] A. Ecklebe, A. Lindemann, and S. Schulz, "Bidirectional Switch Commutation for a Matrix Converter Supplying a Series Resonant Load," *Power Electronics, IEEE Transactions on,* vol. 24, pp. 1173-1181, May 2009.

[10] B. Metidji, N. Taib, L. Baghli, T. Rekioua, and S. Bacha, "Novel Single Current Sensor Topology for Venturini Controlled Direct Matrix Converters," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 3509-3516, Jul 2013.

[11] S. Yao, S. Mei, L. Xing, W. Hui, and G. Weihua, "A General Constructive Approach to Matrix Converter Stabilization," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 418-431, Jan 2013.

[12] F. Mancilla-David, "AC link Vector Switching Converters for power flow control and power quality: A review," in *North American Power Symposium (NAPS),* 2009, pp. 1-7.

[13] J. Kaniewski, Z. Fedyczak, and G. Benysek, "AC Voltage Sag/Swell Compensator Based on Three-Phase Hybrid Transformer With Buck-Boost

Matrix-Reactance Chopper," *Industrial Electronics, IEEE Transactions on,* vol. 61, pp. 3835-3846, Aug 2014.

[14] L. A. C. Lopes, G. Joos, and O. Boon-Teck, "A high power PWM quadrature booster phase-shifter based on a multi-module converter," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE,* 1995, pp. 375-380 vol.1.

[15] D. M. Divan, D. M. Divan, and J. Sastry, "Voltage Synthesis Using Dual Virtual Quadrature Sources - A New Concept in AC Power Conversion," *Power Electronics, IEEE Transactions on,* vol. 23, pp. 3004-3013, Nov 2008.

[16] Z. Youjun and R. Xinbo, "AC-AC Converter With Controllable Phase and Amplitude," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 6235-6244, Nov 2014.

[17] L. Baruschka and A. Mertens, "A New Three-Phase AC/AC Modular Multilevel Converter With Six Branches in Hexagonal Configuration," *Industry Applications, IEEE Transactions on,* vol. 49, pp. 1400-1410, May-Jun 2013.

[18] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 108-123, Jan 2015.

[19] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive Control of AC-AC Modular Multilevel Converters," *Industrial Electronics, IEEE Transactions on,* vol. 59, pp. 2832-2839, Jul 2012.

[20] W. Weimin, H. Yuanbin, and F. Blaabjerg, "An LLCL Power Filter for Single-Phase Grid-Tied Inverter," *Power Electronics, IEEE Transactions on,* vol. 27, pp. 782-789, Feb 2012.

[21] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *Power Electronics, IET,* vol. 3, pp. 702-715, Sep 2010.

[22] V. S. P. Cheung, H. S. H. Chung, W. Ke-Wei, and A. W. L. Lo, "Paralleling Multiple Static Synchronous Series Compensators Using Daisy-Chained Transformers," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 2764-2773, Jun 2014.

[23] W. Huai, H. S. H. Chung, and L. Wenchao, "Use of a Series Voltage Compensator for Reduction of the DC-Link Capacitance in a Capacitor-Supported System," *Power Electronics, IEEE Transactions on,* vol. 29, pp. 1163-1175, Mar 2014.

CHAPTER 9

A New Range of FACTS Devices using a Modular Multilevel AC Hexagonal Chopper

This chapter proposes a new range of FACTS device based on direct AC-AC conversion, where the modular multilevel AC hexagonal chopper (M2AHC) is employed. The M2AHC is operated in a quasi-2-level mode; and heterodyne modulation is used to decouple voltage amplitude regulation from the phase shift; thus, achieving independent control of active and reactive power. Then, a family of FACTS devices based on the M2AHC that offer voltage, active power and reactive power flow control as both shunt and series compensators, is analysed. The use of AC cell capacitors, instead of DC capacitors, in the M2AHC make its footprint smaller and lighter than conventional AC-DC or DC-AC voltage source converter (VSC) based FACTS devices; hence, high reliability and extended service life can be expected. System modelling and controller design of the proposed FACTS devices, are illustrated in a unified reference frame, considering different control modes, transient and unbalanced conditions. Simulation results are used to verify the feasibility of the proposed M2AHC based FACTS devices.

9.1 Background

Penetration of flexible AC transmission system (FACTS) devices into power systems has been fostered by increasing decentralization and meshed grids that bring more complexity to the power dispatch task in electric power networks [1-3].

Voltage source converter (VSC) based FACTS devices such as the static synchronous compensator (STATCOM), static synchronous series compensator (SSSC), and unified power flow controller (UPFC) have proven effective for autonomous voltage and reactive power control, manipulation of shunt reactive current for attenuation of low-order harmonic currents, active power flow control, and voltage unbalance correction through line impedance manipulation. Thus, any attempt to reduce passive component cost, size, weight, reliability; and enhancing the control range compared with thyristor based solutions is advantageous [4, 5].

The two-level VSC is the basic topology for FACTS devices. To reduce power switch voltage stresses and dv/dt on coupling transformers in high voltage applications, various multilevel converters have been introduced and applied. The neutral point clamped (NPC) converter, cascaded full-bridge converter, and modular multilevel converter (MMC) have been presented as FACTS devices in [6-8].

For these DC-AC converters, power flow control theory and grid compensation plus ride-through ability for transient and unbalanced conditions have been developed. However, the high cost and short service life of the large DC-link capacitor bank is currently one constraint hampering the spread of FACTS devices.

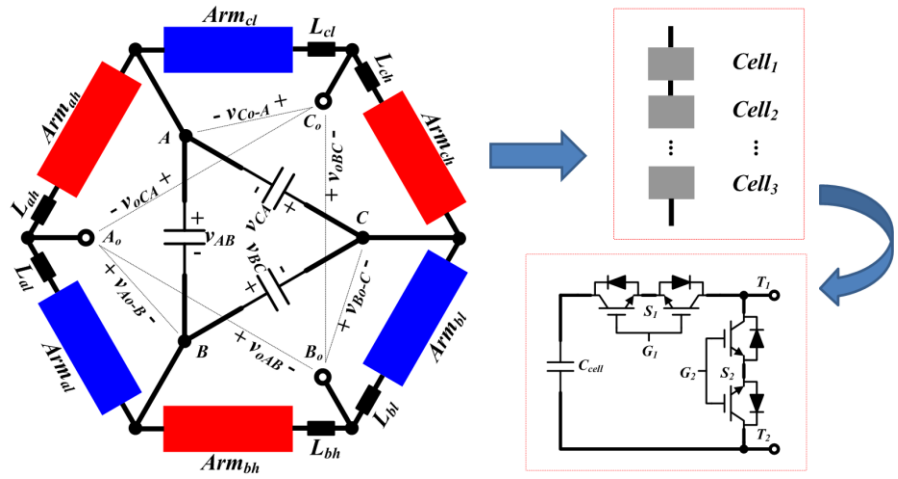
Thus researchers have started investigating direct AC-AC solutions, without a DC-link, for voltage compensators and power flow controllers. The matrix converter is employed as UPFC in [9], where the steady state model and control are analyzed. However, the matrix converter requires numerous bidirectional power switches and complex modulation schemes. The vector switching converter may reduce the number of switches but necessitates the use of a multi-throw input transformer as a power source [10]. The AC chopper is conventionally viewed as voltage amplitude regulator without phase shift ability. By cross connection of different phases in a multi-phase chopper system, both voltage amplitude regulation and phase control are achieved, but are coupled. With the heterodyne based techniques in [11-13] decoupled power control for the vector switching converter, AC chopper and high frequency link AC converter have been developed. However, the necessary high

switching frequency and lack of modularity hamper their extension beyond low and medium voltage applications. Also 3rd order harmonic current is drawn from the grid in these solutions.

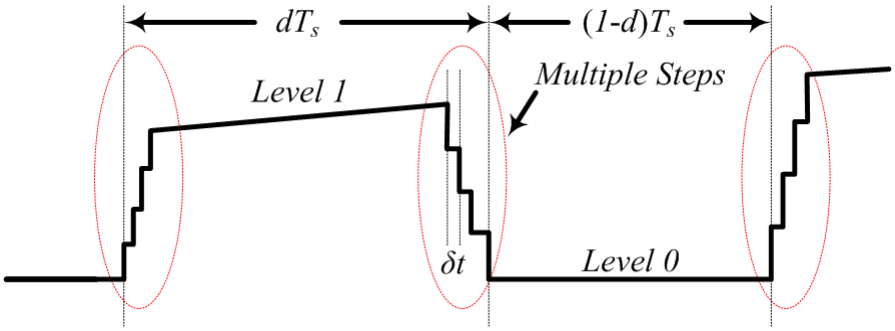
The modular multilevel AC hexagonal chopper (M2AHC) is proposed in Chapter 8, where its configuration and operational principle are discussed. It offers scalability for high-voltage high-power applications by introducing pure AC modular switching cells. Using heterodyne modulation, independent control of voltage amplitude and phase angle is achieved, thus, facilitating the decoupled control of active and reactive power without a DC decoupling stage. Also, its hexagonal structure can circulate zero sequence by-products within the converter, avoiding additional filtering devices. This chapter employs the M2AHC to create a new range of FACTS devices. System configuration and control design are investigated to handle the steady state operation, transient, and unbalanced conditions. The remainder of this chapter is organized as follows: section II reviews converter performance briefly. In section II, potential members of the new range of M2AHC based FACTS devices are introduced and discussed. Then, the modelling of the M2AHC configured as a representative FACTS device with its controller design is explored in section IV. Section V addresses some typical cases to verify the feasibility and effectiveness of the proposed approach. Finally, major findings are highlighted in section VI.

9.2 M2AHC in a Quasi-2-Level Mode with Decoupled Voltage Amplitude and Phase Control

The M2AHC is shown in Fig. 9-1(a), where its six arms are chain links of the half-bridge AC switching cells and AC arm inductors connected end-to-end to form a hexagonal ring. Three-phase output voltages are synthesized by modulating the two arms of each phase according to pre-defined patterns. The use of modular AC switching cells in combination with quasi-2-level operation in Fig. 9-1(b) that divides the voltage level transition into multiple small steps makes the M2AHC scalable to high voltage situations with low electromagnetic interference (EMI). An effective AC cell capacitor voltage balancing strategy is implemented to ensure static and dynamic voltage sharing between power switches [14].



(a)



(b)

Fig. 9-1. M2AHC summary: (a) converter configuration with its arm and cell structures and (b) quasi-2-level operation mode.

In Fig. 9-1, the input line voltages are denoted as $\{v_{AB}, v_{BC}, v_{CA}\}$, $\{d_a, d_b, d_c\}$ are the duty cycles, N is the number of cells in each arm, δt is the time duration for each step in quasi-2-level operation, and T_s is the switching period ($\delta t << T_s$). Then, the duty cycle loss τ by quasi-2-level operation in Fig. 9-1(b) can be calculated by (9.1), and the M2AHC output line voltage can be expressed as in (9.2) when duty cycle loss is neglected.

$$\tau = (N-1)\,\delta t / T_s \tag{9.1}$$

$$\begin{cases} v_{oAB} = v_{AB}\,d_a + v_{BC}\,(1-d_b) \\ v_{oBC} = v_{BC}\,d_b + v_{CA}\,(1-d_c) \\ v_{oCA} = v_{CA}\,d_c + v_{AB}\,(1-d_a) \end{cases} \tag{9.2}$$

If the duty cycle of the M2AHC contains only a DC constant component, the output voltage amplitude and phase regulation cannot be decoupled for lacking of a control degree of freedom. Heterodyne modulation uses harmonic band signals to give a new input degree of freedom for voltage synthesis. As in Chapter 8, a 2nd order negative

sequence modulation signal is employed for decoupling fundamental amplitude and phase angle control of the M2AHC during normal operation. Zero sequence by-products are circulated in the hexagonal ring and are cancelled in the output line-to-line voltage. For unbalanced conditions, the voltage and current waveforms can be resolved into positive and negative sequence components and both should be synthesized from the M2AHC by the heterodyne method separately. In [13], a generalized form of the heterodyne modulation technique is presented for a wide range frequency spectrum. However, this chapter focuses on the transmission level, where the power rating is high, voltage unbalanced between phases is sufficiently small, switching frequency is low, and no high order harmonic distortion exists. Then signals with differential mode DC values plus 2nd order negative sequence components are inserted into the original DC constant duty cycle as shown in (9.3). If the input line voltage is expressed as in (9.4), from (9.2) and (9.3), the synthesized voltage can be derived from (9.5) and (9.6), where $\{v_{pd}, v_{pq}\}$ and $\{v_{nd}, v_{nq}\}$ are *d-q* components of the positive and negative sequences in the M2AHC output phase voltage.

$$\begin{cases} d_a = k_{dc} + k_0 \cos\varphi_0 + k_2 \cos(-2\omega t + \varphi_2) \\ d_b = k_{dc} + k_0 \cos(\varphi_0 - \tfrac{2}{3}\pi) + k_2 \cos(-2\omega t + \varphi_2 - \tfrac{2}{3}\pi) \\ d_c = k_{dc} + k_0 \cos(\varphi_0 + \tfrac{2}{3}\pi) + k_2 \cos(-2\omega t + \varphi_2 + \tfrac{2}{3}\pi) \end{cases} \tag{9.3}$$

$$\begin{cases} v_{AB} = v_m \cos\omega t \\ v_{BC} = v_m \cos(\omega t - \tfrac{2}{3}\pi) \\ v_{CA} = v_m \cos(\omega t + \tfrac{2}{3}\pi) \end{cases} \tag{9.4}$$

$$\begin{cases} v_{pd} = \tfrac{1}{2} v_m (2k_{dc} - 1 + k_2 \cos\varphi_2) \\ v_{pq} = -\tfrac{1}{2} v_m (1/\sqrt{3} + k_2 \sin\varphi_2) \end{cases} \tag{9.5}$$

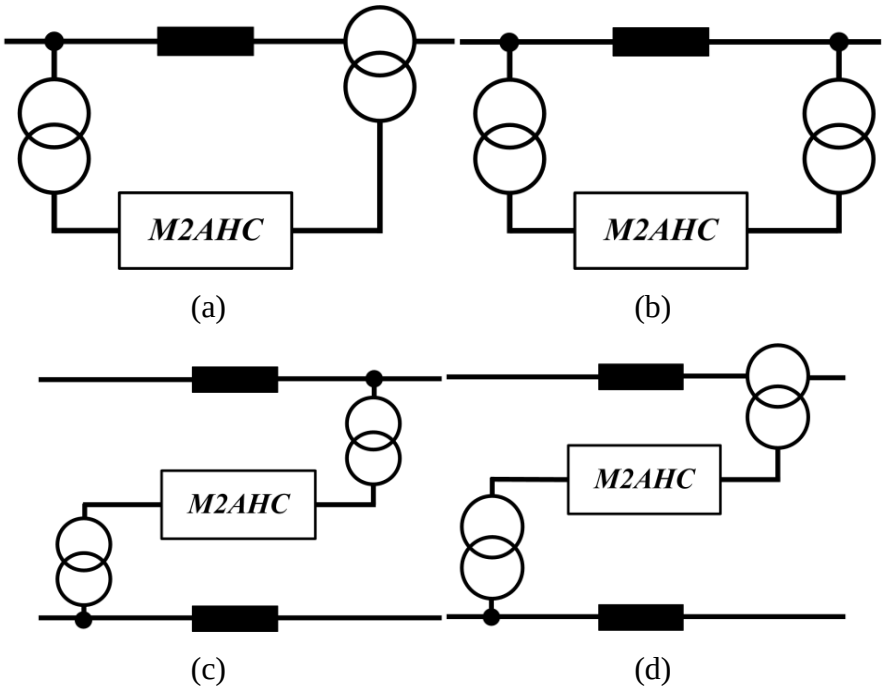
$$\begin{cases} v_{nd} = \tfrac{1}{2} v_m k_0 \cos\varphi_0 \\ v_{nq} = -\tfrac{1}{2} v_m k_0 \sin\varphi_0 \end{cases} \tag{9.6}$$

From (9.5) and (9.6), it is concluded that the M2AHC with heterodyne modulation is able to generate independent voltage vectors, thus, fully decouple the active and reactive power flow control and offers voltage imbalanced mitigation when applied as a FACTS device.

9.3 New Range of FACTS Devices Based on the M2AHC

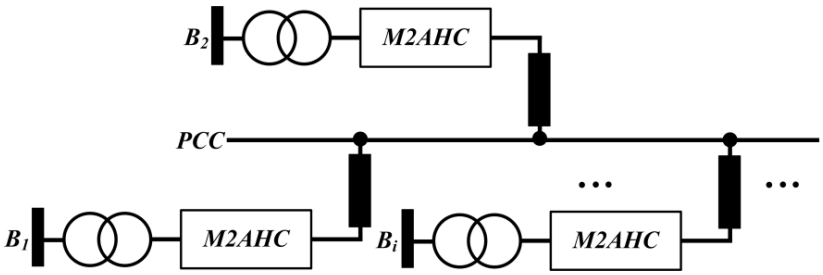
The M2AHC can be configured to form a family of FACTS devices. If the input side is series connected in the power line, the M2AHC operates in current source mode; while if the input terminal is shunt connected to the reference bus, it functions in a voltage source mode. For duality, this chapter focuses on the voltage source mode. Due to the direct AC-AC conversion ability of the M2AHC and different output terminal connection types, a variety of multi-bus FACTS devices can be formed as shown in Fig. 9-2.

When the M2AHC output voltage is inserted in series with the power line, it resembles a basic series compensation device as in Fig. 9-2(a), which is analogous to a conventional UPFC based on AC-DC-AC stages. Similarly, the device in Fig. 9-2(b) is shunt connected to the power line at both terminals and is equivalent to the active source (energy storage) triggered DC-AC VSC STATCOM, which can exchange active power with the grid. Fig. 9-2(c) and (d) show two versions of the dual-power-line configuration, substituting for the interline power flow controller (IPFC). If multiple M2AHC units are adopted to integrate the power buses at the point of common coupling (PCC), a general multi-bus power flow controller which is similar to the multi-terminal AC-DC-AC back-to-back (B2B) device results as in Fig. 9-2(e).



(a) (b)

(c) (d)



(e)

Fig. 9-2. Potential M2AHC configurations according to the output connection types: (a) series compensator; (b) shunt compensator; (c) shunt type interline compensator; (d) series type interline compensator; and (e) general multi-bus power flow controller.

A M2AHC based FACTS device synthesizes amplitude-phase independent AC voltage from the input, thus, it behaves as an AC-AC VSC based solid state transformer (SST). Compared to the magnetic and mechanical phase shift transformer (PST), zig-zag windings plus tap changers can be avoided, thus, the size is significantly reduced and higher flexibility is achieved. Also, due to the absence of a DC link capacitor and M2AHC modularity, the cost and service-life of the proposed FACTS devices are better optimized.

9.4 Generic Modelling and Control Design of an M2AHC Based FACTS Device

As a VSC, the M2AHC is able to either directly determine the injected voltage as a series compensator or regulate the injected current by changing the net voltage vector across the branch as a shunt compensator. In this section, the single power line series compensator of Fig. 9-2(a) is selected as a representative candidate for modelling and control analysis. Then, the general multi-bus power flow controller in Fig. 9-2(e) which involves the B2B configuration of M2AHCs is investigated to offer extended power flow control range and integrated regulation for multiple power grid buses.

9.4.1 M2AHC Based Series Compensator

The detailed configuration of Fig. 9-2(a) is shown in Fig. 9-3, where $\boldsymbol{v_i}=v_i\angle\theta_i$ and $\boldsymbol{v_j}=v_j\angle\theta_j$ are the two bus voltages; X_s represents the power line reactance carrying a current of $\boldsymbol{i_g}$; $n_i\angle\alpha$ is the input shunt transformer voltage ratio; $\boldsymbol{v_{se}}=v_{se}\angle\gamma$ is the series injected voltage by the series interfacing transformer T_{se} with fixed phase shift angle β and turns ratio n_s; and X_f, X_L and B_f are impedances and susceptance of the interfacing passive network as in Fig. 9-3. Active power losses are neglected in the following discussion.

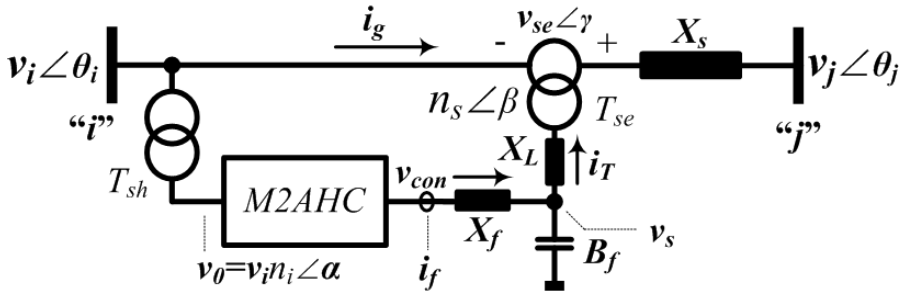


Fig. 9-3. The equivalent circuit of the M2AHC series compensator.

For simplicity, the modelling process focuses on normal operation without any unbalanced disturbance. Bus voltage $\boldsymbol{v_i}$ is employed to feed the input transformer of the M2AHC. From (9.5), its output voltage $\boldsymbol{v_{con}}$ is expressed by (9.7) and (9.8) [14].

$$\boldsymbol{v_{con}} = \boldsymbol{v_o} \cdot A_H\angle\Delta_H = \boldsymbol{v_i} \cdot n_i\angle\alpha \cdot A_H\angle\Delta_H \tag{9.7}$$

$$\begin{cases} A_H = \sqrt{\dfrac{1+3(2k_{dc}-1)^2+3k_2{}^2}{4} + \dfrac{(6k_{dc}-3)k_2\cos\varphi_2 + \sqrt{3}k_2\sin\varphi_2}{2}} \\ \Delta_H = -\cos^{-1}\left[\dfrac{\sqrt{3}(2k_{dc}-1)+\sqrt{3}k_2\cos\varphi_2}{2A_H}\right] + \frac{1}{6}\pi \end{cases} \tag{9.8}$$

Based on the previous analysis, the current vectors and nodal power flow equations of the series compensator are derived as in (9.9)-(9.11), where $\boldsymbol{S_{con}}$ and $\boldsymbol{S_{se}}$ are the power flows of the M2AHC output terminal and power injection point respectively. The expressions of active and reactive power at these two nodes are determined from (9.12) to (9.14) after algebraic manipulation. Parameters n_i, n_s, α, β, W_e, X_f, X_L and B_f are known, fixed parameters.

$$\begin{pmatrix} \boldsymbol{i_f} \\ \boldsymbol{i_g} \end{pmatrix} = \begin{pmatrix} \dfrac{X_L B_f - 1}{jW_e} & \dfrac{\angle-\beta}{jn_s W_e} \\ \dfrac{-\angle\beta}{jn_s W_e} & \dfrac{1-X_f B_f}{jn_s{}^2 W_e} \end{pmatrix} \times \begin{pmatrix} \boldsymbol{v_{con}} \\ \boldsymbol{v_{se}} \end{pmatrix} \tag{9.9}$$

$$W_e = X_L X_f B_f - X_f - X_L \tag{9.10}$$

$$\begin{aligned} \begin{pmatrix} \boldsymbol{S_{con}} \\ \boldsymbol{S_{se}} \end{pmatrix} &= \begin{pmatrix} \boldsymbol{v_{con}} & \\ & \boldsymbol{v_{se}} \end{pmatrix} \times \begin{pmatrix} \boldsymbol{i_f}^* \\ \boldsymbol{i_g}^* \end{pmatrix} \\ &= \begin{pmatrix} \boldsymbol{v_{con}} & \\ & \boldsymbol{v_{se}} \end{pmatrix} \times \begin{pmatrix} \dfrac{1-X_L B_f}{jW_e}\boldsymbol{v_{con}}^* + \dfrac{-\angle\beta}{jn_s W_e}\boldsymbol{v_{se}}^* \\ \dfrac{\angle-\beta}{jn_s W_e}\boldsymbol{v_{con}}^* + \dfrac{X_f B_f - 1}{jn_s{}^2 W_e}\boldsymbol{v_{se}}^* \end{pmatrix} \end{aligned} \tag{9.11}$$

$$P_{con} = P_{se} = -\frac{n_i A_H v_i v_{se}}{n_s W_e} \sin(\Delta_H + \theta_i + \alpha + \beta - \gamma) \tag{9.12}$$

$$Q_{con} = \frac{(X_L B_f - 1) n_i^2 A_H^2 v_i^2}{W_e} + \frac{n_i A_H v_i v_{se}}{n_s W_e} \cos(\Delta_H + \theta_i + \alpha + \beta - \gamma) \tag{9.13}$$

$$Q_{se} = \frac{(1 - X_f B_f) v_{se}^2}{n_s^2 W_e} - \frac{n_i A_H v_i v_{se}}{n_s W_e} \cos(\Delta_H + \theta_i + \alpha + \beta - \gamma) \tag{9.14}$$

From the grid model, the power flow at the series injection point $\boldsymbol{S_{se}}$ is expressed in (9.15) if the grid line current equation is obtained from the grid voltage vectors.

$$\begin{cases} \boldsymbol{S_{se}} = \boldsymbol{v_{se}} \cdot (\dfrac{\boldsymbol{v_i} + \boldsymbol{v_{se}} - \boldsymbol{v_j}}{jX_s})^* \\ P_{se} = \dfrac{v_j v_{se} \sin(\gamma - \theta_j) - v_i v_{se} \sin(\gamma - \theta_i)}{X_s} \\ Q_{se} = \dfrac{v_i v_{se} \cos(\gamma - \theta_i) + v_{se}^2 - v_j v_{se} \cos(\gamma - \theta_j)}{X_s} \end{cases} \tag{9.15}$$

The injected voltage $\boldsymbol{v_{se}}$ is able to independently control the active and reactive power flow between $\boldsymbol{v_i}$ and $\boldsymbol{v_j}$. Based on the power injection model in [15], the incremental power flow at nodes '*i*' and '*j*' are calculated by (9.16). Then, the active and reactive power injection are given by (9.17) and (9.18).

$$\begin{cases} \delta \boldsymbol{S_i} = \boldsymbol{v_i} (\dfrac{\boldsymbol{v_{se}}}{jX_s})^* + P_{con} + jQ_{con} \\ \delta \boldsymbol{S_j} = \boldsymbol{v_j} (\dfrac{\boldsymbol{v_{se}}}{jX_s})^* \end{cases} \tag{9.16}$$

$$\begin{cases} \delta P_i = \dfrac{v_i v_{se} \sin(\gamma - \theta_i)}{X_s} + P_{se} \\ \delta Q_i = \dfrac{v_i v_{se} \cos(\gamma - \theta_i)}{X_s} + Q_{con} \end{cases} \tag{9.17}$$

$$\begin{cases} \delta P_j = \dfrac{v_j v_{se} \sin(\gamma - \theta_j)}{X_s} \\ \delta Q_j = \dfrac{v_j v_{se} \cos(\gamma - \theta_j)}{X_s} \end{cases} \tag{9.18}$$

Thus, the set of mismatch power equations to achieve the equilibrium operating point of the network is arrived at:

$$\begin{pmatrix} \Delta P_i \\ \Delta P_j \\ \Delta Q_i \\ \Delta Q_j \end{pmatrix} = -\begin{pmatrix} J_{p\theta} & J_{pv} \\ J_{q\theta} & J_{qv} \end{pmatrix} \times \begin{pmatrix} \Delta \theta_i \\ \Delta \theta_j \\ \Delta v_i \\ \Delta v_j \end{pmatrix} \tag{9.19}$$

where the modified Jacobian matrix after injection of the M2AHC compensator is detailed in (9.20) to (9.23):

$$J_{p\theta} = \begin{pmatrix} \frac{\partial \Delta P_i}{\partial \theta_i} + \frac{\partial \delta P_i}{\partial \theta_i} & \frac{\partial \Delta P_i}{\partial \theta_j} + \frac{\partial P_{se}}{\partial \theta_j} \\ \frac{\partial \Delta P_j}{\partial \theta_i} & \frac{\partial \Delta P_j}{\partial \theta_j} + \frac{\partial \delta P_j}{\partial \theta_j} \end{pmatrix} \tag{9.20}$$

$$J_{pv} = \begin{pmatrix} \frac{\partial \Delta P_i}{\partial v_i} + \frac{\partial \delta P_i}{\partial v_i} & \frac{\partial \Delta P_i}{\partial v_j} + \frac{\partial P_{se}}{\partial v_j} \\ \frac{\partial \Delta P_j}{\partial v_i} & \frac{\partial \Delta P_j}{\partial v_j} + \frac{\partial \delta P_j}{\partial v_j} \end{pmatrix} \tag{9.21}$$

$$J_{q\theta} = \begin{pmatrix} \frac{\partial \Delta Q_i}{\partial \theta_i} + \frac{\partial \delta Q_i}{\partial \theta_i} & \frac{\partial \Delta Q_i}{\partial \theta_j} \\ \frac{\partial \Delta Q_j}{\partial \theta_i} & \frac{\partial \Delta Q_j}{\partial \theta_j} + \frac{\partial \delta Q_j}{\partial \theta_j} \end{pmatrix} \tag{9.22}$$

$$J_{qv} = \begin{pmatrix} \frac{\partial \Delta Q_i}{\partial v_i} + \frac{\partial \delta Q_i}{\partial v_i} & \frac{\partial \Delta Q_i}{\partial v_j} \\ \frac{\partial \Delta Q_j}{\partial v_i} & \frac{\partial \Delta Q_j}{\partial v_j} + \frac{\partial \delta Q_j}{\partial v_j} \end{pmatrix} \tag{9.23}$$

By solving the power flow mismatch equations in (9.19), the compensator solutions for v_{se}, γ, A_H, Δ_H and the reference bus voltage status, can be determined.

As is explained in Chapter 8, the M2AHC output voltage contains an initial bias voltage of half the input voltage, caused when the converter operates with 0.5 duty cycle. This issue does not limit shunt type devices but makes the reactive power control range of series M2AHC devices asymmetrical (the full active power control range can always be guaranteed). To overcome this, the input transformer secondary winding can be centrally tapped to supply the reference terminal for the output winding in Fig. 9-4.

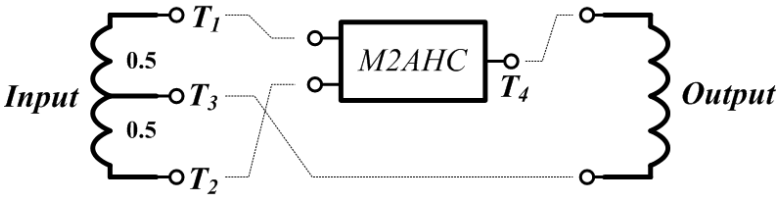


Fig. 9-4. Tapped winding connection for bias voltage blocking in M2AHC series compensator.

9.4.2 System Control Design

In Chapter 8, the M2AHC controller design with an *LCL* filter is discussed, and is divided into three layers and implemented in the *d-q* frame. As a series type compensator, the incremental active and reactive powers of receiving node '*j*' are set as control targets, with the reference voltage $\boldsymbol{v_i}$ as input to the phase-locked-loop (PLL).

$$\begin{cases} |\delta S_j| = \sqrt{\delta P_j^{\,2} + \delta Q_j^{\,2}} = \dfrac{v_j v_{se}}{X_s} \\ \delta P_j / \delta Q_j = \tan(\gamma - \theta_j) \end{cases} \tag{9.24}$$

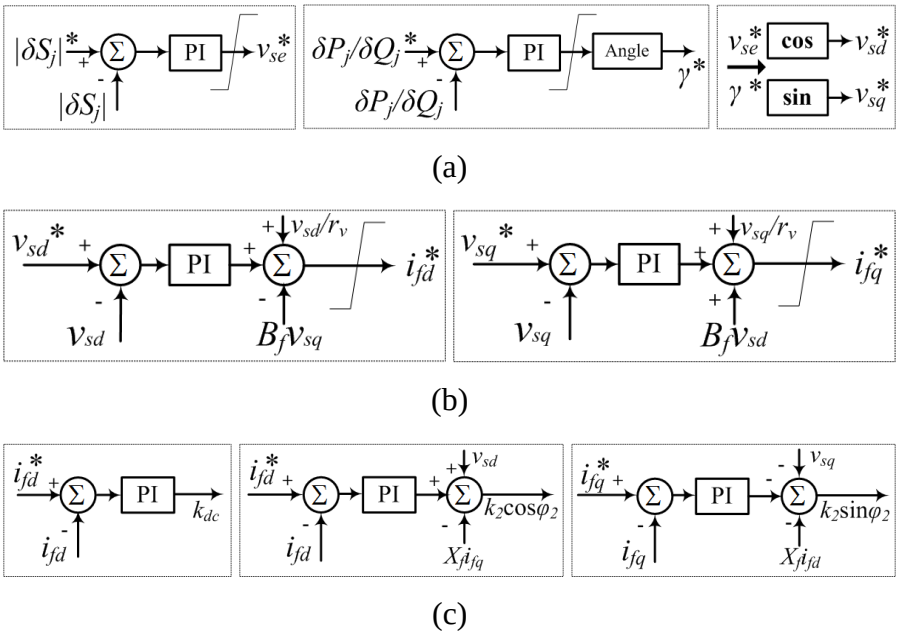


Fig. 9-5. Diagrams of dynamic control blocks for the M2AHC series compensator: (a) power flow control layer; (b) local voltage control layer; and (c) converter output current controller.

Based on (9.18), independent control of active and reactive power flow is obtained by manipulation of the voltage amplitude and phase, as in (9.24). Thus, the power control layer is clarified by Fig. 9-5(a), where the obtained reference signals v_{se} and γ are used to generate the *d-q* frame references $\{v_{sd}^*, v_{sq}^*\}$ for the next levels. Then, Fig. 9-5(b) and (c) show the intermediate and inner control layers respectively [14].

k_{dc} and $k_2\cos\varphi_2$ are responsible for regulating the direct component of the M2AHC output voltage, while $k_2\sin\varphi_2$ determines its quadrature part. The proportional-integral (PI) method is adopted in the control block of Fig. 9-5 to stabilize the global system, where r_v is the active damping coefficient. Detailed transfer function derivation is presented in Chapter 8.

9.4.3 Ride-Through Ability for Unbalanced Conditions

During voltage unbalanced operation, the series type M2AHC can act as a DVR to mitigate voltage unbalance, based on (9.6). By differentiating the DC component of the heterodyne modulating signal in each phase with $k_0\cos\varphi_0$, $k_0\cos(\varphi_0-\frac{2}{3}\pi)$ and $k_0\cos(\varphi_0+\frac{2}{3}\pi)$, an independent negative sequence component of the fundamental is generated. This component can be exploited to manipulate the M2AHC to correct the disturbed load bus voltage when it suffers from unbalanced voltage or power flow.

If v_{jnd} and v_{jnq} are the direct and quadrature components of the negative sequence disturbance in the load bus voltage v_j, to suppress them to zero, and from Fig. 9-3, the M2AHC unit should contribute a specific amount of negative sequence output voltage locally to counter that in the system. Fig. 9-6 clarifies the control block diagrams for load bus unbalanced voltage cancellation, where $v_{snd,q}$ and $i_{fnd,q}$ are the corresponding output state variables of the M2AHC in the negative sequence. The obtained pair of control outputs, $\{k_0\cos\varphi_0, k_0\sin\varphi_0\}$ is employed to synthesize the required DC differential signals for the voltage compensation mode (unbalanced power flow ride-through).

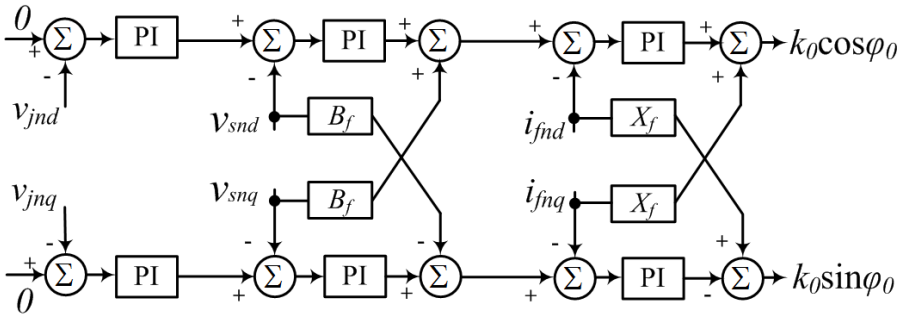


Fig. 9-6. Control blocks for negative sequence voltage elimination.

9.4.4 Generalized Multi-bus Power Flow Controller

As in Fig. 9-2(e), multiple AC grid buses can be integrated into a single PCC by M2AHC units, where the two converters resemble a B2B arrangement, and is called a generalized multi-bus power flow controller (GMPFC). With this configuration, the active and reactive power flow of each grid can be controlled autonomously or can

achieve desired operational objectives set by a high-level supervisory controller, such as SCADA (supervisory control and data acquisition). The connection of two M2AHCs in a B2B arrangement in Fig. 9-7 offers independent control of active and reactive power over the full range in a pure AC system, which is similar to that in multi-terminal high voltage direct current (HVDC) systems. For illustration simplicity, this chapter uses voltage droop to realize active and reactive control at the PCC hub.

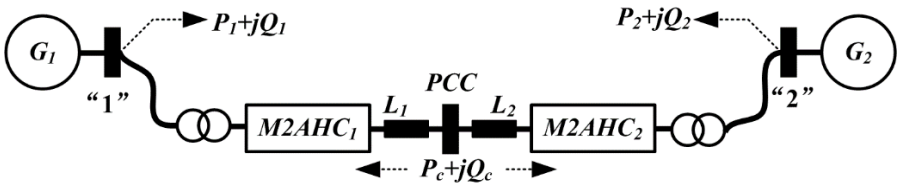


Fig. 9-7. Connection of the GMPFC using two M2AHC B2B units.

The bias voltages caused by the DC component of the modulating signals, to cancel between the two M2AHC units; thus, symmetrical and a doubled power flow control range are achieved when using basic shunt interfacing transformers, thereby avoiding the tapped winding structures in Fig. 9-4 for the single M2AHC series compensator. For an *m*-buses power network, there are *m*-1 control degrees of freedom for the proposed GMPFC, considering the law of energy conservation.

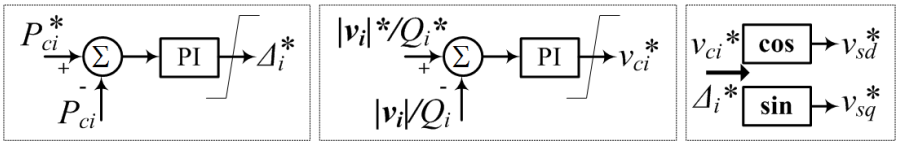


Fig. 9-8. Power control blocks for a GMPFC based on B2B M2AHC devices.

The GMPFC control block is shown in Fig. 9-8, where bus *i* is assumed for general cases. Neglecting M2AHC losses, the bus active power mismatch equals that through the PCC port, and is denoted by P_{ci}. Thus, in Fig. 9-8, P_{ci} is controlled to generate the reference for the converter output voltage phase-shift Δ_i while the bus reactive power Q_i can be regulated by the converter output voltage amplitude v_{ci}. The generated signals Δ_i* and v_{ci}* are transferred as voltage references for the inner control layer, then the local control strategy shown in Fig. 9-6 is compatible for each M2AHC unit. The GMPFC potentially affords voltage support if one grid bus voltage drops. In this case, the converter connected to the fault bus functions in a boost mode with pure DC modulating signals to offer step-up ability for bus voltage build up.

9.5 Performance Evaluation

To confirm the effectiveness of the proposed approach, the performance of the M2AHC based FACTS device as series compensator, as in Fig. 9-3, is investigated using an 11-level converter model (with ten AC switching cells per arm) in the Matlab/Simulink software environment. Then, the general multi-bus power flow controller, with two converter units, is simulated to show power regulation functionality for a meshed grid.

Table 9-1. M2AHC specification for simulation

11-level M2AHC	
Apparent power rating S_{con}	60MVA
AC input phase voltage v_0	15.88kV(RMS)
AC cell capacitor C_{cell}	10μF
Arm inductor L_{arm}	10μH
Filtering capacitor C_f	100μF
filtering inductor L_f	10mH
Quasi-two-level time duration	5μs
Converter switching frequency	1.8kHz

Table 9-2. Interfacing transformer parameters

Shunt transformer	
Power capacity	60MVA
Winding type	Δ/Y
Voltage ratio	110kV/27.5kV
Per unit impedance	(0.0005+j0.08)
Series transformer	
Power capacity	60MVA
Winding type	Δ/Independent
Voltage ratio	17kV/17kV
Per unit impedance	(0.0002+j0.05)

Table 9-3. AC power system parameters

Grid parameters for series compensation	
Three-phase short circuit level	1.91GVA
Nominal line voltage	110kV(RMS)
X/R	18

The M2AHC specification is given in Table 9-1; while the parameters for the transformers and AC grid are shown in Table 9-2 and Table 9-3 respectively.

The device level results of M2AHC converter operation are briefly summarized in Fig. 9-9. Fig. 9-9(a) is the chopped AC voltage on an M2AHC output terminal and Fig. 9-9(b) shows voltage balancing of the 20 AC cell capacitors. The zoomed version of the output voltage with multilevel steps is displayed by Fig. 9-10(a); while the corresponding upper and lower arm currents are shown in Fig. 9-10(b).

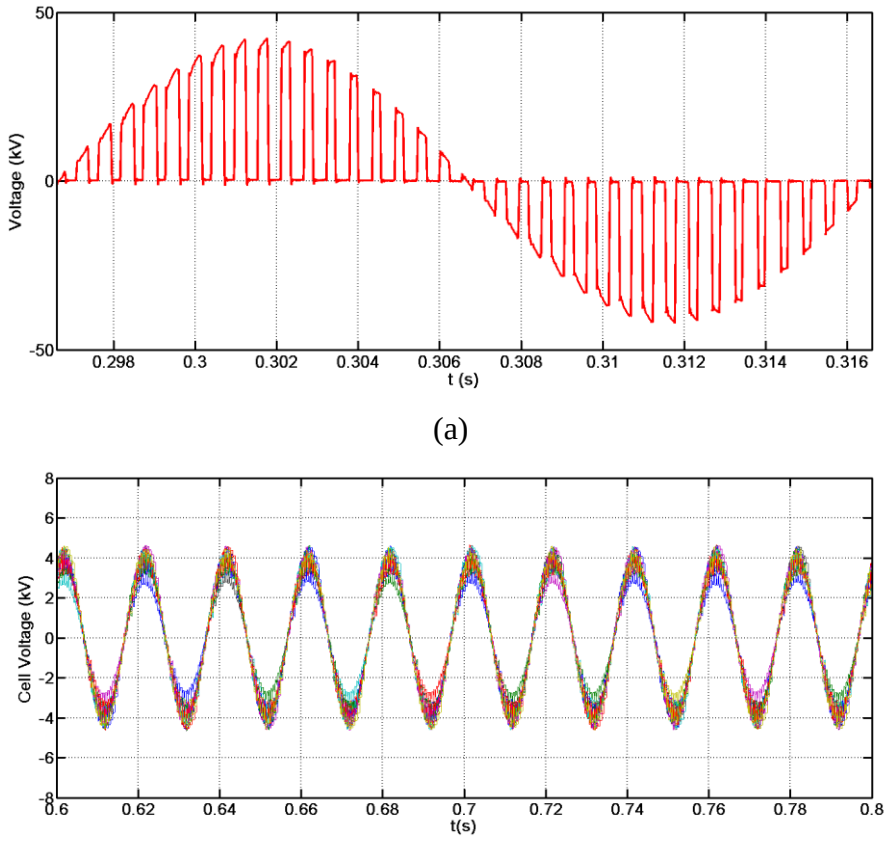


Fig. 9-9. Waveforms of the M2AHC operated in a quasi-two-level mode: (a) chopped output voltage and (b) AC cell capacitor voltage balancing result.

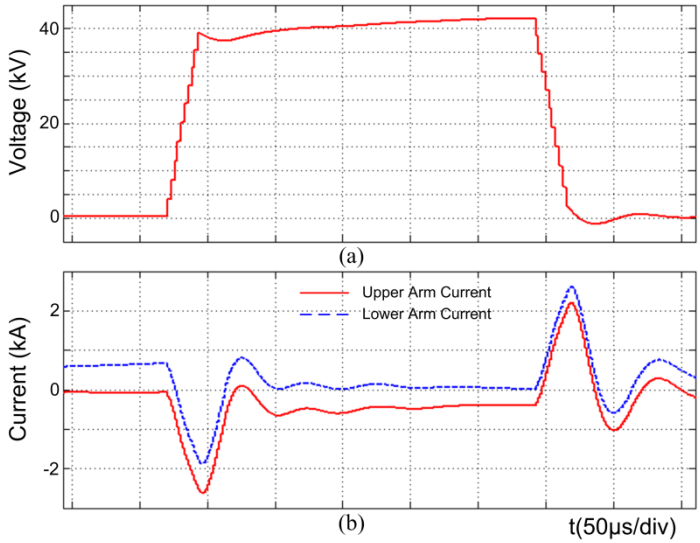
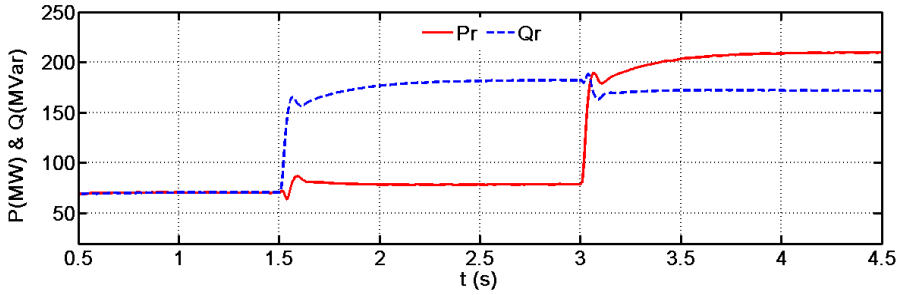


Fig. 9-10. Quasi-two-level mode operation of the M2AHC: (a) multilevel steps on the voltage chopping edge and (b) the corresponding arm currents.

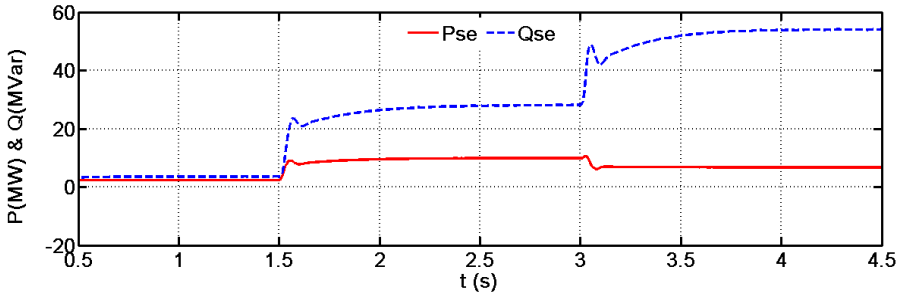
Firstly, the M2AHC based series compensator is tested in a power flow control mode. The control targets are the receiving bus active and reactive power. Initially, the grid line carries a power flow of 70MW+*j*70MVAr. At t=1.5*s*, the reactive power

command is stepped to 180MVAr; then, at t=3s, the active power command is increased to 210MW.

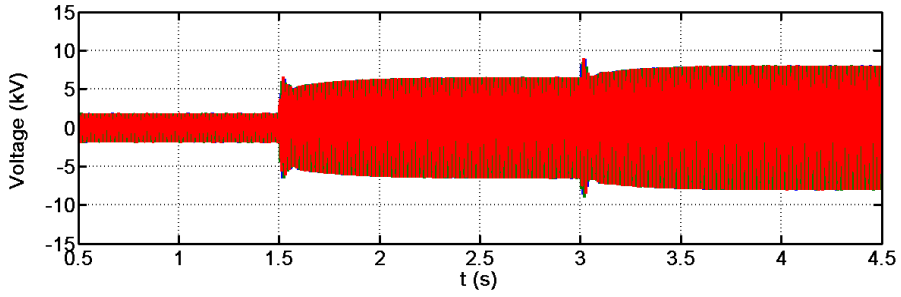
Fig. 9-11(a) and (b) show the active and reactive power at the power line, where the power flow references are smoothly tracked. During the power flow transitions, the M2AHC compensator contributes small active power and significant reactive power as it controls the power flow in the main line as in Fig. 9-11(b). Correspondingly, Fig. 9-11(c) and (d) display the series injected voltage in the time domain and its *d-q* version when the M2AHC operates in a power flow control mode. The *d-q* components of the inserted voltage are widely manipulated as they control the grid power flow, which is contrary to that in a conventional SSSC. This indicates that the M2AHC based series compensator in Fig. 9-3 can perform the functions of both a conventional SSSC and a UPFC.



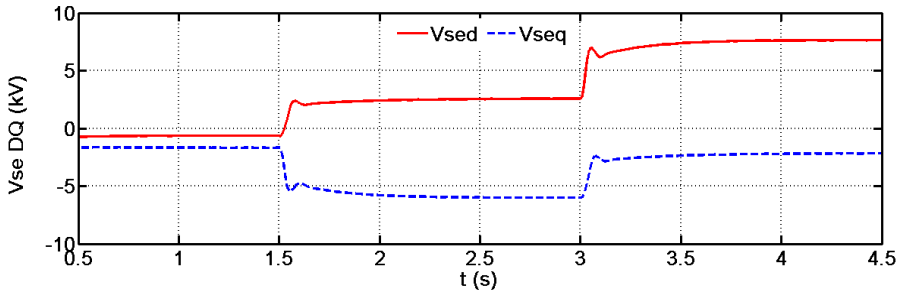
(a)



(b)



(c)

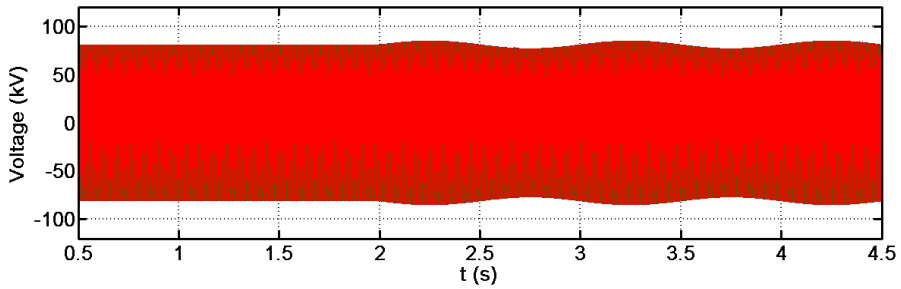


(d)

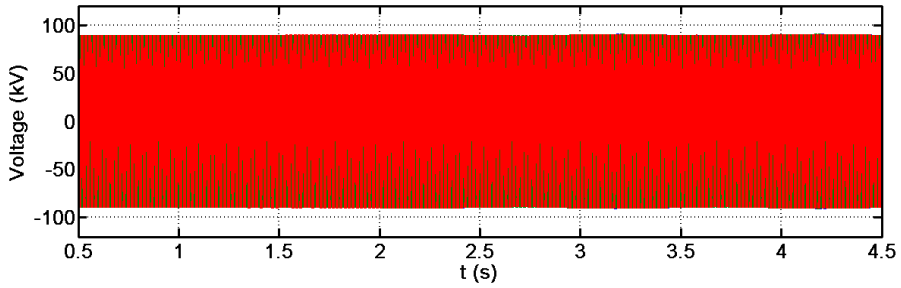
Fig. 9-11. Power flow regulation using the M2AHC series compensator: (a) active and reactive power flow in grid line; (b) power exchange between compensator and grid; (c) series injected voltage in the time domain; and (d) series injected voltage in *d-q* frame.

With continuing decentralization of the power system, operation under unbalanced voltage conditions in medium-voltage distribution systems is becoming increasingly challenging due to a large number of single-phase loads and DGs connected at lower distribution voltages. Assuming the bus terminal B_r in Fig. 9-3 is weak and disturbed by uneven power flow in the line, two cases are examined: flicker phenomenon and unbalanced load.

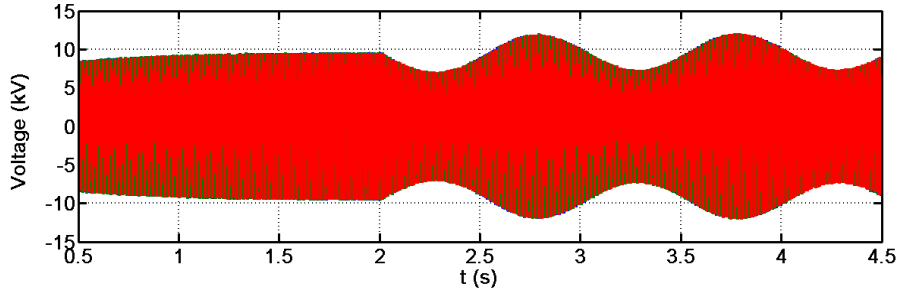
To illustrate flicker mitigation, a dynamic load that mimics a typical flicker with a 1Hz oscillation frequency is connected at the weak receiving bus B_r at t= 2s. Such a flicker risk is expected to be a common problem with increased penetration of medium-scale wind farms on the distribution systems. Fig. 9-12(a) shows that the voltage waveform at B_r has heavy flicker at 1Hz frequency, without compensation. This bus voltage can be controlled near flicker free (constant) after enabling the M2AHC series compensator operating in a voltage control mode (similar to the dynamic voltage restorer, DVR), as in Fig. 9-12(b). Fig. 9-12(c) and (d) show the series voltage waveform injected by the M2AHC (in time domain) and the *d-q* frame, respectively.



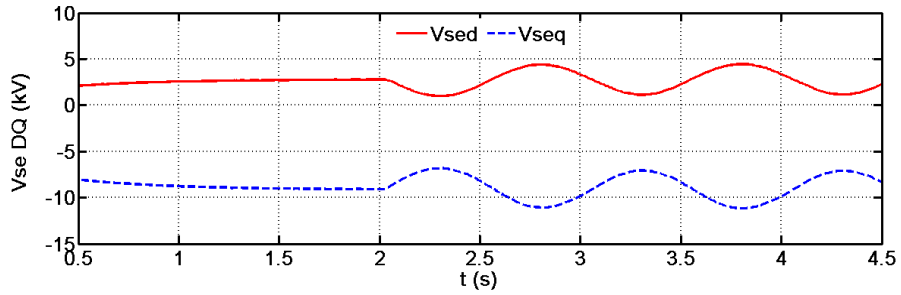
(a)



(b)



(c)

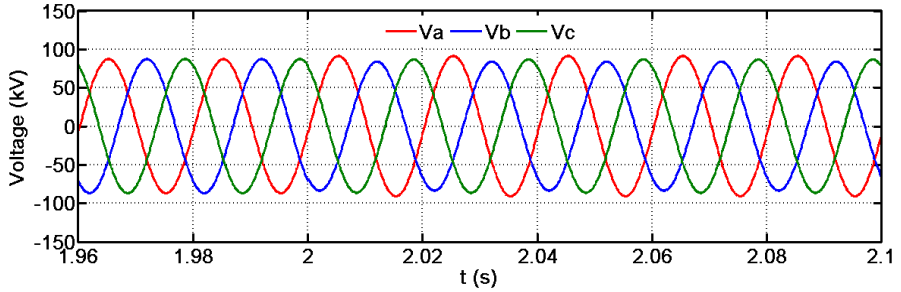


(d)

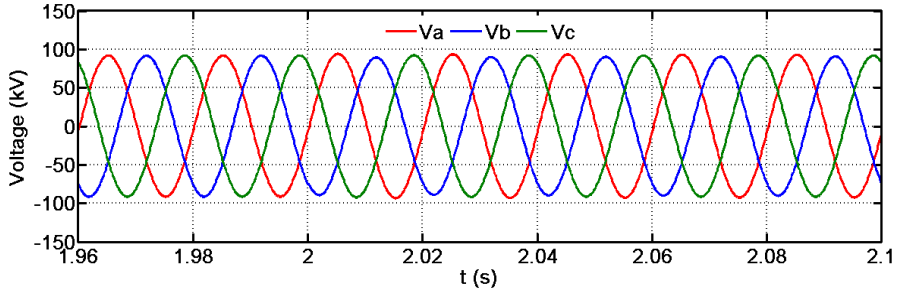
Fig. 9-12. Voltage flicker immunization using an M2AHC series compensator: (a) flicker without compensation; (b) flicker-free bus voltage with the proposed compensator; (c) injected voltage in the time domain; and (e) injected voltage in the *d-q* frame.

The unbalanced load condition influences the weak bus voltage. In Fig. 9-3, an unbalanced fault occurs at t=2s, and the load bus voltage without compensation is displayed in Fig. 9-13(a). The control block in Fig. 9-6 for the M2AHC series compensator is activated, and the unbalanced negative sequence component is eliminated as in Fig. 9-13(b) and the bus voltage is maintained balanced. Fig. 9-13(c) is the series unbalanced voltage injected by the M2AHC FACTS device. The positive and negative sequence *d-q* compensator voltage components are shown in Fig. 9-13(d). The proposed M2AHC series compensator adjusts the *d-q* components of the negative sequence in order to mitigate voltage balanced at B_r.

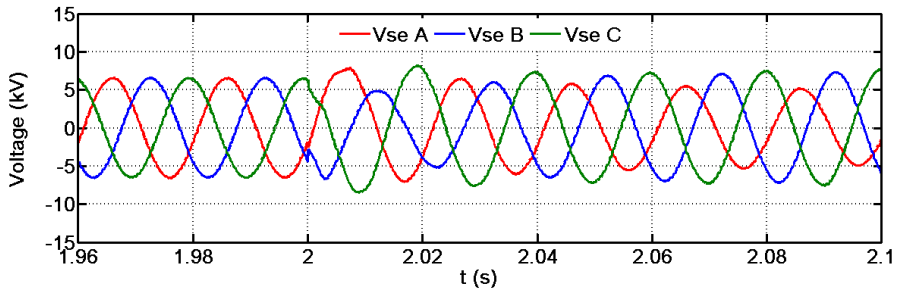
These results verified that the proposed M2AHC series compensator is capable of acting as a unified power controller and implements a voltage compensation function during disturbances. Thus the conventional SSSC, UPFC and DVR can be replaced by the proposed M2AHC based solutions, under certain conditions.



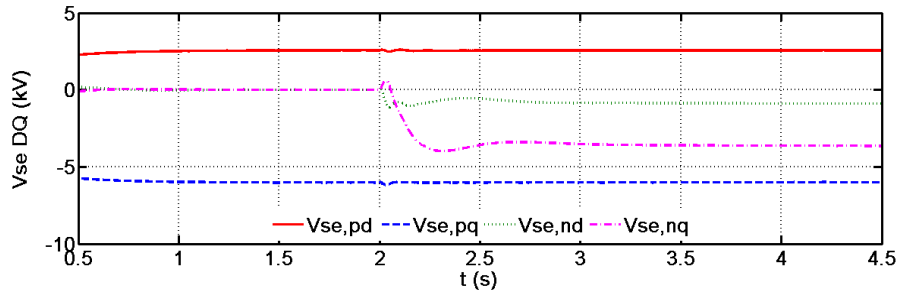
(a)



(b)



(c)



(d)

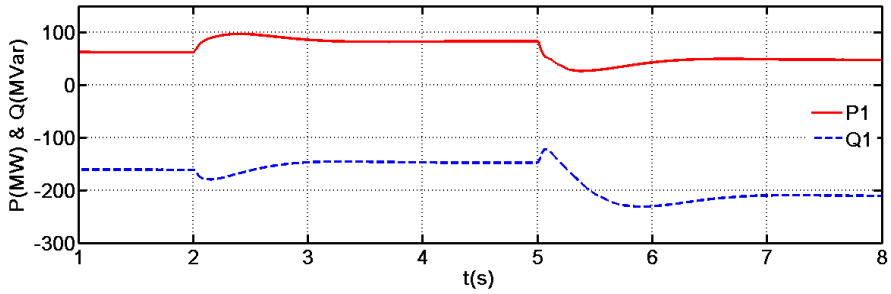
Fig. 9-13. Voltage unbalance compensation using the M2AHC series compensator: (a) unbalanced disturbance without compensation; (b) balanced voltage with the proposed compensator; (c) injected voltage in the time domain; and (e) injected voltage in the *d-q* frame.

For the GMPFC case with two M2AHC units as in Fig. 9-7, with a two bus network, there is one degree of freedom for power control and bus '1' is concerned as the control target.

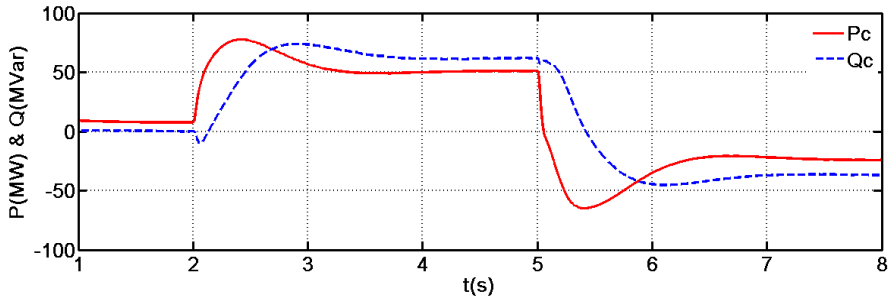
Initially the nodal active and reactive power is controlled via M2AHC output voltage droop. The initial power flow for bus '1' is 60MW-*j*170MVAr, and the commands for active and reactive power are increased by 30MW/MVAr at *t*=2*s* and decreased by 50MW/MVAr at 5*s*. In Fig. 9-14(a), the M2AHC voltage droop forces the nodal power flow to track their references. The power exchange between the GMPFC and grid in Fig. 9-14(b) shows that a bidirectional power injection range is obtained and the bias voltage problem of a single M2AHC unit when configured as series type device, is avoided in a B2B configuration.

Then, the controller is set to maintain voltage amplitude at node '1' and regulate the active power flow between AC grids '1' and '2'. Initially, the B2B supplies 30MW active power and zero reactive power to node '1'. The active power flow command is stepped to 60MW at *t*=2*s*, and an additional 60MW+*j*80MVAr load is applied on bus '1' at 4s and removed at 6*s*. During these transitions, the GMPFC maintains the voltage amplitude by regulating the shunt injected reactive power and tracks the active power flow command, as shown in Fig. 9-14(c) and (d).

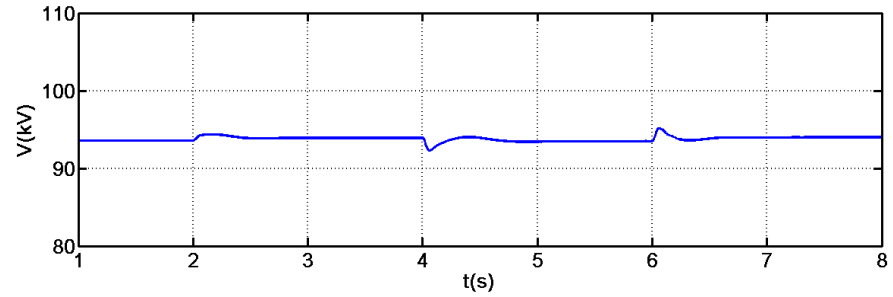
The proposed M2AHC based B2B arrangement performs functionally as an AC-DC-AC system (HVDC). It offers independent active and reactive power control for power flow optimization in highly meshed grids as well as voltage support during disturbances.



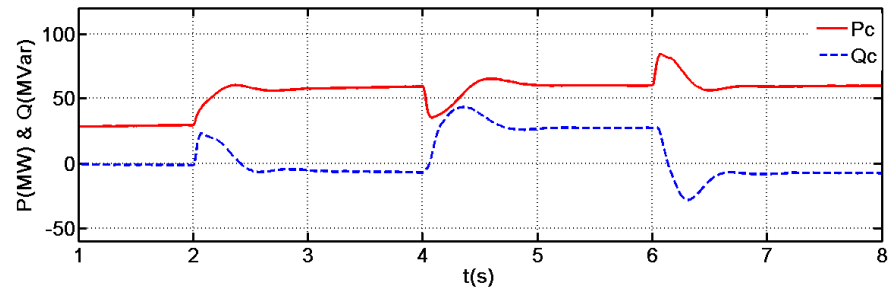
(a)



(b)



(c)



(d)

Fig. 9-14. Power and voltage control using the B2B M2AHC device: (a) nodal power flow response in power control mode; (b) power exchange between device and grid; (c) bus voltage amplitude response; and (e) power exchange between device and grid in voltage control mode.

9.6 Summary

This chapter has proposed a new range of FACTS devices using the modular multilevel AC hexagonal chopper (M2AHC). The main contributions of this research are:

- By adopting the direct AC-AC scheme, the footprint of a M2AHC based power flow controller is reduced due to the absence of sizable DC link and DC cell capacitors.
- The M2AHC with heterodyne modulation act like a typical VSC with independent control of voltage amplitude and phase (active and reactive

power). The modularity and reduced switch number per unit voltage rating, make the M2AHC competitive with the matrix converter.

- Potential uses of the M2AHC for different FACTS devices were discussed, and offered different grid control functions.
- The modelling and power flow equations of the M2AHC series compensation device were presented, showing the interaction between the power controller and the grid.
- The M2AHC local controllers have been interpreted to arrive at a flexible power control strategy, adaptable to different control targets.
- Power flow control and mitigation of voltage flicker and unbalance by the series M2AHC compensator were verified.
- The B2B configuration with the proposed M2AHC was shown to offer an extended control range and for integrate multiple AC grids in a hub, better utilized transmission capacity.

Reference

[1] X. Ying, Y. H. Song, L. Chen-Ching, and Y. Z. Sun, "Available transfer capability enhancement using FACTS devices," *Power Systems, IEEE Transactions on,* vol. 18, pp. 305-312, Feb 2003.

[2] R. S. Wibowo, N. Yorino, M. Eghbal, Y. Zoka, and Y. Sasaki, "FACTS Devices Allocation With Control Coordination Considering Congestion Relief and Voltage Stability," *Power Systems, IEEE Transactions on,* vol. 26, pp. 2302-2310, Nov 2011.

[3] J. Mutale and G. Strbac, "Transmission network reinforcement versus FACTS: an economic assessment," *Power Systems, IEEE Transactions on,* vol. 15, pp. 961-967, Aug 2000.

[4] G. Cao, Z. Y. Dong, Y. Wang, and P. Zhang, "VSC based series FACTS controllers for damping local mode oscillations," in *Power Engineering Society General Meeting, 2007. IEEE*, 2007, pp. 1-7.

[5] Y. Liangzhong, P. Cartwright, L. Schmitt, and Z. Xiao-Ping, "Congestion Management of Transmission Systems Using FACTS," in *Transmission and Distribution Conference and Exhibition: Asia and Pacific, 2005 IEEE/PES*, 2005, pp. 1-5.

[6] N. M. R. Santos, J. F. Silva, J. Verveckken, V. M. F. Pires, and R. M. G. Castro, "Enhancing the Ride-Through Capability of DC-Link Voltage in NPC Multilevel Unified Power-Flow Controllers," *Power Delivery, IEEE Transactions on,* vol. 29, pp. 1542-1550, Aug 2014.

[7] A. Marzoughi, Y. Neyshabouri, and H. Imaneini, "Control scheme for cascaded H-bridge converter-based distribution network static compensator," *Power Electronics, IET,* vol. 7, pp. 2837-2845, Nov 2014.

[8] D. Sixing and L. Jinjun, "A Study on DC Voltage Control for Chopper-Cell-Based Modular Multilevel Converters in D-STATCOM Application," *Power Delivery, IEEE Transactions on*, vol. 28, pp. 2030-2038, 2013.

[9] O. Boon-Teck and M. Kazerani, "Unified power flow controller based on matrix converter," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 502-507 vol.1.

[10] J. M. Ramirez, J. M. Gonzales, and M. L. Crow, "Steady state formulation of FACTS devices based on ac/ac converters," *Generation, Transmission & Distribution, IET*, vol. 1, pp. 619-631, Jul 2007.

[11] L. A. C. Lopes, G. Joos, and O. Boon-Teck, "A high power PWM quadrature booster phase-shifter based on a multi-module converter," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, 1995, pp. 375-380 vol.1.

[12] D. M. Divan, D. M. Divan, and J. Sastry, "Voltage Synthesis Using Dual Virtual Quadrature Sources - A New Concept in AC Power Conversion," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 3004-3013, Nov 2008.

[13] L. Chushan, D. Yan, L. Zibo, L. Wuhua, H. Xiangning, and W. Yousheng, "Virtual Quadrature Source-Based Sinusoidal Modulation Applied to High-Frequency Link Converter Enabling Arbitrary Direct AC-AC Power Conversion," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4195-4208, 2014.

[14] P. Li, Y. Wang, G. Philip Adam, D. Holliday, and B. W. Williams, "Three-Phase AC-AC Hexagonal Chopper System With Heterodyne Modulation for Power Flow Control Enhancement," *IEEE Transactions on Power Electronics*, vol. 30, pp. 5508-5521, 2015.

[15] M. Noroozian, L. Angquist, M. Ghandhari, and G. Andersson, "Use of UPFC for optimal power flow control," *Power Delivery, IEEE Transactions on*, vol. 12, pp. 1629-1634, 1997.

CHAPTER 10

Conclusion

10.1 Author's Contribution

Chapter one presented a review of the FACTS devices and their uses to optimize and extend dynamic ratings of aging power systems and future smart grids. Discussion of the operating principles, control strategies, attributes and limitations of the main types of current and voltage source converter (CSC, VSC) based FACTS devices, was presented. It is concluded that existing voltage source converter based FACTS devices offer significant advantages over current source converter and impedance based line commutated counterparts. However, the circuit topologies of existing VSC based FACTS devices that employ two-level, neutral-point clamped and modular converters, do not allow full exploitation of their DC link voltages to maximize the control range. In addressing this weakness, a number of novel DC/AC and direct AC/AC converters were introduced. These converters present a new set of features suitable for modern power systems, such as high DC utilization, small footprint (light weight and small size), high efficiency, and low cost.

Chapter two used two-level and full-bridge voltage source converters to illustrate the fundamental concepts and control strategies of series and shunt types FACTS devices. This chapter forms the basis for the new FACTS devices presented in the subsequent chapters, including those based on direct AC/AC converters.

Chapters three and four analysed the AC side voltage-doubled (ACVD) converter and its performance as FACTS devices, by considering a static synchronous compensator (STATCOM) and a static series synchronous compensator (SSSC), as examples. The use of ACVD converter improves the power density per unit DC-link; thus, extends the control range in grid-connected inverters and series and shunt type FACTS devices.

Chapters five discussed multilevel converters with the emphasis on the device and system aspects which are relevant to FACTS devices for medium and high voltage applications.

In chapter six, a new controlled transition full-bridge hybrid multilevel converter (CTFB-HMC), with full-bridge (FB) cells chain-links, was proposed. The proposed converter offers the following features: modularity and scalable to medium and high-voltage applications, high efficiency, and high power density. Its modulation and cell energy balancing method and control strategy for grid and islanding modes were analysed, and its feasibility as a FACTS device was assessed using the STATCOM as a bench mark.

Chapter seven reviewed the viable direct AC –AC converter topologies such as matrix converter, vector switching converter, AC chopper, high-frequency-link AC-AC converter and full-bridge cell cascaded AC-AC converters. The attributes and limitations are all highlighted.

Two-level and multilevel versions of the three-phase AC chopper were proposed in chapter eight, where the necessary modulation strategy that exploits the heterodyne concept is utilized to decouple the active and reactive power control, as in the conventional DC-AC VSC.

Chapter nine used the modular multilevel AC hexagonal chopper (M2AHC) developed in chapter eight to generate new array of series and shunt FACTS devices, demonstrated by simulation. The hexagonal AC choppers offer a cost effective solution for FACTS devices since the functions of several conventional FACTS devices, such as STATCOM, SSC, DVR and UPFC, can be combined in a single configuration, with a minimum number of conversion stages.

The main contribution and significance of this thesis can be summarised as:

- A new ACVD converter, which increases DC link voltage utilization to twice that of the two-level converter, has been proposed.
- Insertion of a DC bias into modulating signal of the ACVD converter facilitates better exploitation of the DC bias across the internal buck-boost cell capacitor, increasing the maximum peak of the AC voltage to twice the DC rail voltage. This is achieved at the expense of increased voltage stresses on the converter switching devices.

- The theoretical analysis of the ACVD converter showed that, to generate sinusoidal output voltage and current, a dedicated control strategy is needed to suppress the low-order harmonic distortion caused by its internal cell dynamics, which is predominantly 2^{nd} order for a sinusoidal reference.
- The application of the ACVD-VSC in shunt and series type FACTS devices such as STATCOM and SSSC was investigated and compared to two-level converter equivalents. It was demonstrated that the FACTS devices based on ACVD converters have larger control range than two-level converter based FACTS devices; due to its doubled DC-link voltage utilization.
- A controlled transition full-bridge hybrid multilevel converter (CTFB-HMC) was proposed, which is scalable to medium and high-voltage applications. Its operating principle, modulation scheme for voltage synthesis and cell voltage balancing were illustrated.
- The hardware design guidelines and power loss analysis for CTFB-HMC were presented. The proposed converter offers high power density due to the doubled DC utilization, and its power conversion efficiency is comparable to the half-bridge cell MMC.
- The control scheme for CTFB-HMC and its operation as a grid-connected VSC and FACTS devices was demonstrated using simulation.
- A direct AC-AC two-level hexagonal AC chopper for micro-grids and FACTS device was proposed. Its modulation strategy exploits a 2^{nd} harmonic to decouple the control of voltage magnitude from the phase angle; thus, independent control of active and reactive powers is achieved.
- The modular multilevel AC hexagonal chopper (M2AHC) with quasi-2-level operation was proposed to achieve true scalability and lower dv/dt on the interfacing transformer. The proposed solution offers a saving compared to the hexverter, as DC cell capacitors are replaced by small AC capacitors.
- The proposed M2AHC was adopted to generate a new family of FACTS devices based on direct AC-AC conversion, involving a minimum number of conversion stages.
- The representative single-line series controller and the general multi-bus power flow controller (GMPFC) using M2AHC were assessed. The series controller is able to implement the functions of SSSC and DVR devices;

while the GMPFC can serve as a hub to integrate and distribute the power flow between multiple AC grids.

10.2 Future Research Expectation

The thesis has proposed three types of voltage source converters that are suitable for medium and high voltage FACTS devices. Some recommendations for future research are:

- Nonlinear modelling and control strategies are suggested for the ACVD converter to improve its dynamic response and control accuracy.
- To optimize the cell capacitor size and further improve the output voltage quality of the proposed CTFB-HMC, and additional control loop for elimination of the low order harmonic cell voltage ripple can be investigated.
- Detailed analysis is required for the power system with multiple installations of M2AHC based FACTS controllers, such as their influence on grid stability.

Appendices

Appendix A. Park Transformation and Phase-Locked-Loop System

The definition of Park transformation used in this thesis is described as follows:

The Clark transformation matrix $T_{abc/\alpha\beta\gamma}$ is expressed in (A.1), which is employed to transform the balanced three-phase vectors $\mathbf{X_{abc}}$ into $\alpha\beta\gamma$ axes with the γ component equal to zero.

$$T_{abc/\alpha\beta\gamma} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.1}$$

Since the obtained $\mathbf{X_{\alpha\beta\gamma}}$ is time-variant, a new axes system with relative rotational displacement of θ is introduced as shown in Fig.A-1. As a result, the projection of α-β components on d-q axes can be calculated by (A.2). So the transformation matrix $\alpha\beta\gamma$-dqo is expressed in (A.3).

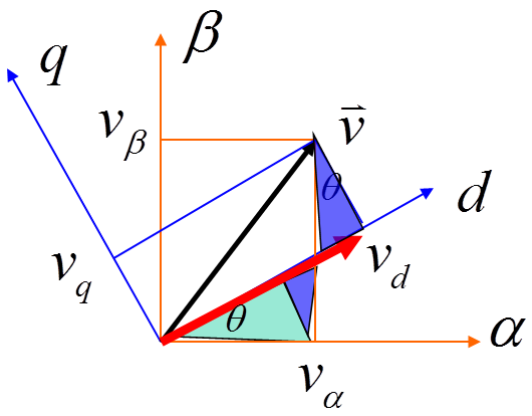


Fig.A-1. The location of *d*-*q* axes and *α*-*β* axes.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{A.2}$$

$$\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} \tag{A.3}$$

The overall transformation matrix from *abc* to *dqo* is therefore achieved in (A.4), and the transformation and its inverse process can be summarized by (A.5). If the *d-q* components of the voltage and current at the same node are known as $v_{d,q}$ and $i_{d,q}$, the nodal power flow can be calculated from (A.6).

$$T = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - \tfrac{2}{3}\pi) & \cos(\theta + \tfrac{2}{3}\pi) \\ -\sin\theta & -\sin(\theta - \tfrac{2}{3}\pi) & -\sin(\theta + \tfrac{2}{3}\pi) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.4}$$

$$\begin{cases} X_{dqo} = T \cdot X_{abc} \\ X_{abc} = T^{-1} \cdot X_{dqo} \end{cases} \tag{A.5}$$

$$\begin{cases} P = v_d \cdot i_d + v_q \cdot i_q \\ Q = v_q \cdot i_d - v_d \cdot i_q \end{cases} \tag{A.6}$$

In order to ride through the unbalanced disturbance of the grid, the phase-locked-loop and the *d-q* transformation should be reformed. In three-phase unbalanced conditions, the time-variant variables can be resolved into positive and negative sequences using the symmetrical component. To enhance the dynamic response of the PLL system and controller, the dual-decoupled synchronous reference frame (DDSRF) is utilized.

$$\begin{bmatrix} x_{Pd} \\ x_{Pq} \end{bmatrix} = \begin{bmatrix} X_{Pd} \\ X_{Pq} \end{bmatrix} + X_{Nq} \begin{bmatrix} \sin 2\theta \\ \cos 2\theta \end{bmatrix} + X_{Nd} \begin{bmatrix} \cos 2\theta \\ \sin(-2\theta) \end{bmatrix} \tag{A.7}$$

$$\begin{bmatrix} x_{Nd} \\ x_{Nq} \end{bmatrix} = \begin{bmatrix} X_{Nd} \\ X_{Nq} \end{bmatrix} + X_{Pq} \begin{bmatrix} \sin(-2\theta) \\ \cos 2\theta \end{bmatrix} + X_{Pd} \begin{bmatrix} \cos 2\theta \\ \sin 2\theta \end{bmatrix} \tag{A.8}$$

When the unbalanced signals are input into the positive and negative sequence *d-q* transformations, the time-variant coupling terms with 2nd order emerge according to (A.7) and (A.8). Therefore, as in Fig.A-2, the multiple cross feedforward can be used to simultaneously compensate the 2nd order harmonics in both transformations.

In a PLL system, by forcing the positive sequence *q*-component of the DDSRF to be zero using the PI controller, the effective phase-angle of the fundamental variable in positive sequence can be precisely tracked.

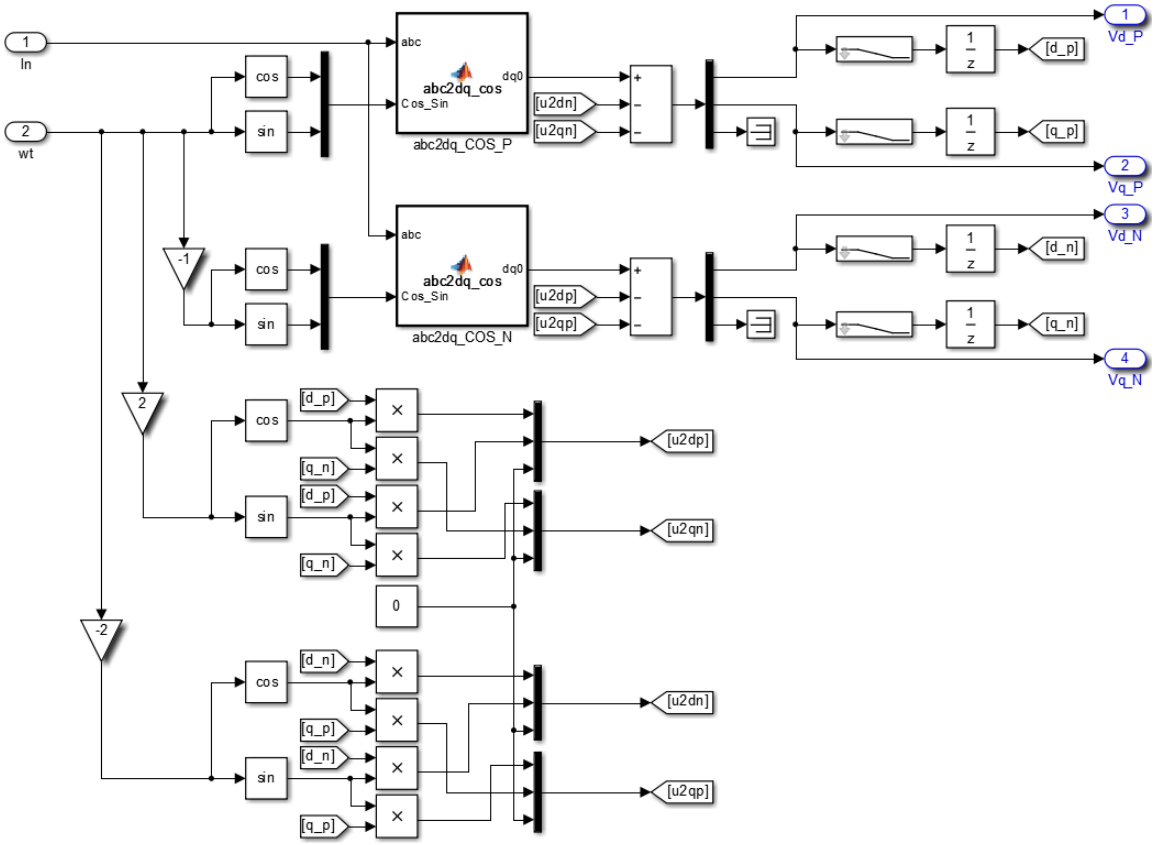


Fig.A-2. The dual-decoupled synchronous reference frame (DDSRF) for PLL and *d-q* transformation under unbalanced conditions.

Appendix B. Power Filter Design Routine

I. The L filter design

The L filter in Fig.A-3 uses a single inductor to attenuate the current harmonics, limiting the ripple; and it also direct influence the power exchange range between the grid and the converter. The first-order L type filter has only one design degree of freedom. The inductance value L directly determines the power injection range and current harmonics level when other conditions are fixed.

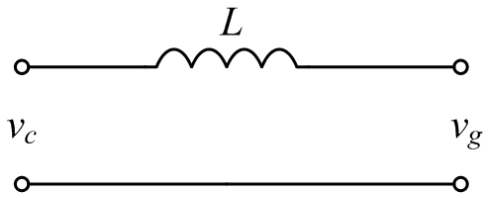


Fig.A-3. Representation of L filter.

Assume V_g is the grid voltage amplitude, V_c is the converter voltage amplitude, S_N is the rated power in each phase that is injected by the converter and ω is the grid fundamental angular frequency, the maximum power can be calculated by (A.9).

$$S_N = \frac{V_g}{\omega L}\sqrt{V_c^2 - V_g^2} \tag{A.9}$$

Then, for harmonic consideration, if the *n*th order voltage harmonic amplitude is V_n and η_n represents the required maximum percentage of *n*th order current harmonic among the total rated current (according to IEEE or IEC standards), (A.10) can be arrived.

$$\frac{|V_n|}{\omega L}\cdot\frac{V_g}{S_N} \le \eta_n \tag{A.10}$$

Based on above analysis and by the compromise evaluation of (A.9) and (A.10), the proper L filter value can be selected. Then, by calculating the current ripple flowing through the power switches with the selected value, L can be further optimized.

II. The LC filter design

The LC filter in Fig.A-4 has an extra high impedance shunt capacitor compared to L filter; therefore, the harmonic can be further attenuated. In grid-connected mode with insufficient line impedance, the shunt capacitor of LC filter is bypassed for the high

frequency component since the grid can be viewed as short circuit for high frequency harmonics.

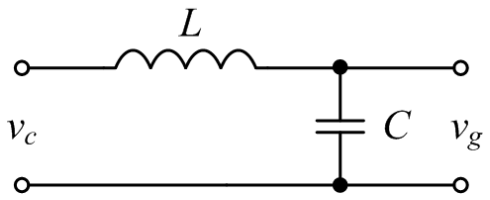


Fig.A-4. Representation of LC filter.

In standalone mode, the LC filter design procedure can be summarized as follows:

- The cut-off frequency of the LC filter expressed by (A.11) is chosen to meet the voltage harmonic requirement. For example, if the lowest order switching frequency side band harmonic should be attenuated to sufficient low level, as shown in (A.12), where $G(s)$ is the voltage transfer function of LC filter, ω_h is the angular frequency of the dominant harmonic, and correspondingly, η_h is its maximum allowed percentage.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{A.11}$$

$$\left|G(s)\right|_{s=j\omega_h} \le V_c \cdot \eta_h \tag{A.12}$$

- The inductance value L can influence the current ripple and the voltage drop across itself. The voltage drop amplitude of L is denoted as V_L, and it is able to reflect the total absorbed reactive power as well as the voltage amplitude difference between the converter and the grid. Usually, it is suggested VL is below certain percentage (λ) of grid voltage as in (A.13). For example, if λ is chosen to be 25%, the converter voltage amplitude V_c is nearly same as V_g.

$$V_L \le \lambda V_g \tag{A.13}$$

- Verify the reactive power rating of the shunt capacitor and usually make it below certain percentage (λ_c) of the total power rating of the system as is shown in (A.14). Then, the system can work well in rated condition.

$$\omega C V_g^2 \le S_N \cdot \lambda_c \tag{A.14}$$

With the above method, the LC filter can achieve sufficient harmonic attenuation, minimum reactive power storage and guarantee enough bandwidth to ensure the overall dynamic response.

III. The LCL filter design

As pointed above, in gird connected condition, the LC filter can achieve sufficient attenuation only when the interfacing line impedance is large enough. With this idea, the LCL filter in Fig.A-5 is used to obtain better steady state results for the grid-tied converters.

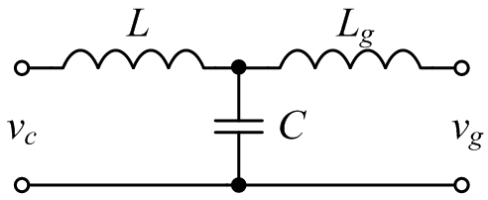


Fig.A-5. Representation of LCL filter.

The design method of the parameters L, C and L_g are summarized as follows:

- Based on the tolerable current ripple percentage (γ) for the power converter, the inner inductance L is evaluated by (A.15).

$$\frac{\Delta I_L}{I_m} = \frac{V_{in}}{4Lf_{sw}I_m} \le \gamma \tag{A.15}$$

- The capacitor rated reactive power rating should be limited, which can be referred to (A.14).
- The grid side inductor L_g is mainly used to attenuate the high order harmonics that are located within the sideband of the switching frequency f_{sw}. Also, to avoid significant voltage drop across the two inductors, the total inductance $L+L_g$ should be limited, such as to be 0.1pu of the normalized impedance that is defined by the rated voltage and power.
- The resonant frequency of the LCL filter expressed in (A.16) should be located in a reasonable range such as between 10 times of line frequency and half of switching frequency.

$$f_r = \frac{1}{2\pi} \cdot \sqrt{\frac{L+L_g}{LL_gC}} \tag{A.16}$$

- By manipulating the impedance of the LCL network in Fig.A-5, the current harmonic transfer function for each frequency can be obtained. Using the parameters evaluated above to check the attenuation level. If the result is not

qualified, try to change the limit of the inductance voltage drop V_L or the resonant frequency location; then, reset the procedure.

- Using the passive damping or active damping methods can reduce the quality factor of the LCL network, avoiding oscillation and instability.

Appendix C. Controller Design Using State-Space in SRF

In this thesis, the converters are all controlled using cascaded control diagram, which has a compensator for each passive device state variable (first-order). In this way, the open-loop transfer function for describing each stage is a first-order inertial element and belongs to type-0 system. With this knowledge, to present the general controller parameter design method adopted in this thesis, the current controller of the grid-tied VSC in Fig.A-6 is considered as an example and all variables are expressed in *d-q* frame, where $v_{c,dq}$ is the converter terminal voltage, $v_{g,dq}$ is the grid voltage, i_{dq} is the current flowing from the VSC to the grid and $\omega L+r$ represents the impedance of the line reactor.

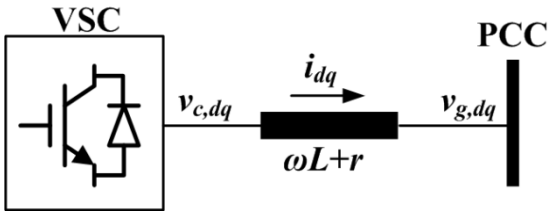


Fig.A-6. Representation of VSC connected to the grid.

The type-0 system theoretically has steady-state error when responding to the input signal. If the input signal is a step function, by compensating the system to type-I, zero steady state error can be achieved, which means the normal PI controller is sufficient to implement precise reference tracking. This benefit is brought by using the SRF analysis method.

The differential equations that describe the ac side dynamic performance of the grid-tied VSC in SRF are summarized by (A.17).

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{L}\begin{bmatrix} v_{cd} - v_{gd} + \omega L i_q \\ v_{cq} - v_{gq} - \omega L i_d \end{bmatrix} - \frac{r}{L}\begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{A.17}$$

In SRF, with the cross feedforward decoupling, the output of the PI controller can be expressed by (A.18) in a closed loop system. Then, using $\{F_d, F_q\}$ to represent the integral terms of the PI controller, the state space equations for the direct current and quadrature current closed loop system are obtained as (A.19) and (A.20).

$$\begin{cases} \gamma_d = v_{cd} - v_{gd} + \omega L i_q = k_p(i_d^* - i_d) + k_i \int (i_d^* - i_d)dt \\ \gamma_q = v_{cq} - v_{gq} - \omega L i_d = k_p(i_q^* - i_q) + k_i \int (i_q^* - i_q)dt \end{cases} \tag{A.18}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ F_d \end{bmatrix} = \begin{bmatrix} -\dfrac{k_p + r}{L} & \dfrac{k_i}{L} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_d \\ F_d \end{bmatrix} + \begin{bmatrix} \dfrac{k_p}{L} \\ 1 \end{bmatrix} i_d^* \tag{A.19}$$

$$\frac{d}{dt}\begin{bmatrix} i_q \\ F_q \end{bmatrix} = \begin{bmatrix} -\dfrac{k_p + r}{L} & \dfrac{k_i}{L} \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_q \\ F_q \end{bmatrix} + \begin{bmatrix} \dfrac{k_p}{L} \\ 1 \end{bmatrix} i_q^* \tag{A.20}$$

Combining (A.19) and (A.20), the current control system can be optimized by proper placement of the poles and zeros. Alternatively, from the state space equations, the open loop *d-q* current transfer function with PI compensation can be expressed as in (A.21).

$$G_i = \frac{k_i(1 + s \cdot k_p / k_i)}{r \cdot s \cdot (1 + s \cdot L / r)} \tag{A.21}$$

With the predefined switching frequency f_{sw} (selected based on switching losses and ripple requirement), the crossover frequency of the compensated system is set to be 0.2 f_{sw} to ensure dynamics and stability, that is expressed by (A.22).

$$\begin{cases} f_c = f_{sw} / 5 \\ \left| G_i(j\omega) \right|_{\omega = 2\pi f_c} = 1 \end{cases} \tag{A.22}$$

Usually, the cut-off frequency of the PI compensator f_L is selected to be lower than the cut-off frequency of the open loop transfer function without compensation, which is noted as f_o. In this way, adequate phase margin can be maintained.

Appendix D. Test Rig Description

I. The DSP control system

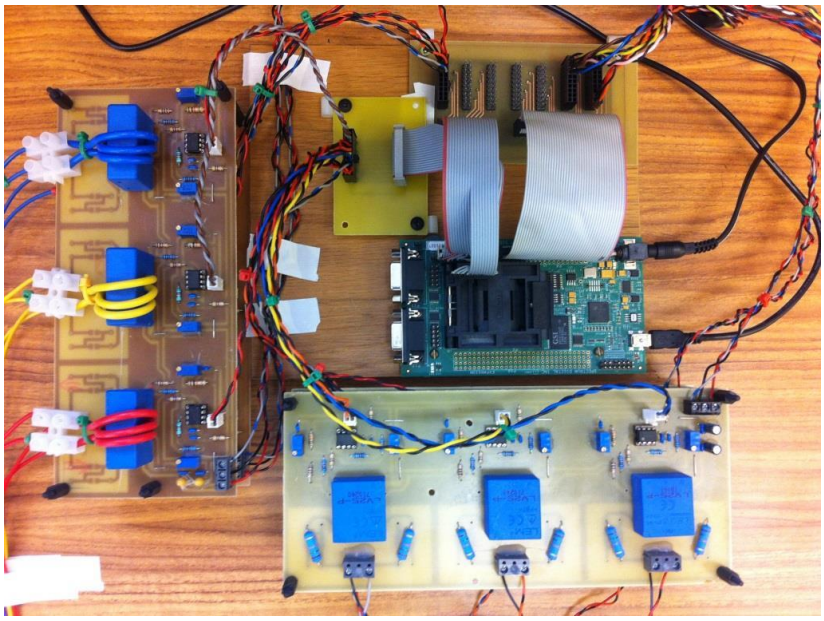


Fig.A-7. The TMS320F28335 DSP platform.

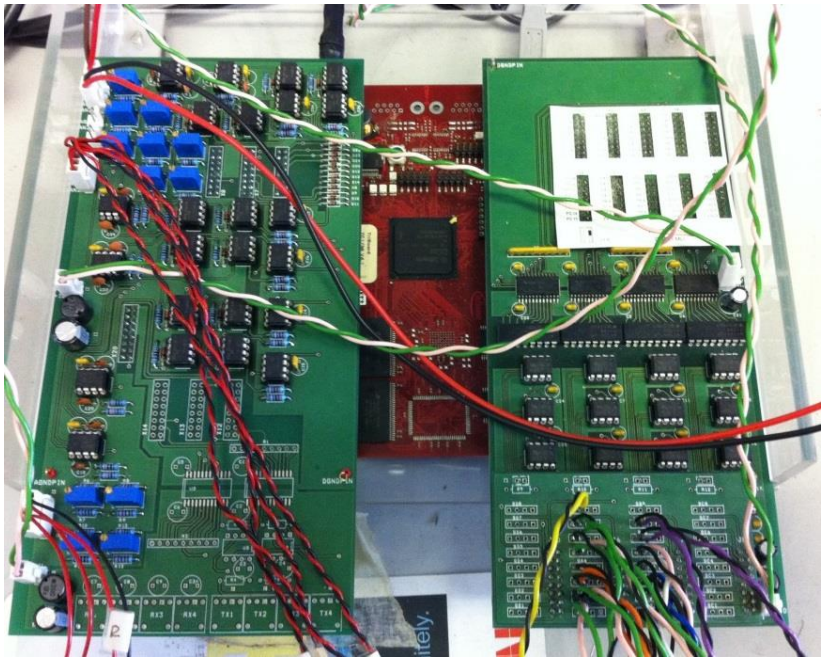


Fig.A-8. The TC1796 DSP and the extension boards.

Two kinds DSP controllers are utilized in this research. As in Fig.A-7, the Texas Instrument (TI) TMS320F28335 is responsible for the generation of three pairs of PWM outputs; while in multilevel converter experiments with more than six PWM

channels required, the Infineon TC1796 in Fig.A-8 is employed to avoid the use of an FPGA/CPLD for I/O extension.

II. The ACVD converter test rig

The test rig for ACVD converter in Chapter 3 is shown in Fig.A-9. It consists of:

- TMS320F28335 DSP controller
- Voltage and current transducer board
- Gate drivers
- DC-link capacitor
- Buck-boost cell capacitor and inductor
- DC power supply and auxiliary voltage source
- Output LC filter

Fig.A-9. The photo of the test rig for ACVD converter.

III. The two-level AC hexagonal chopper test rig

The test rig for two-level hexagonal AC chopper in Chapter 8 is shown in Fig.A-10. It consists of:

- TMS320F28335 DSP controller
- Auxiliary voltage source
- Gate drivers
- Three-phase two-level AC hexagonal chopper
- Voltage and current transducer boards
- Three-phase input transformer

- Input and output filters
- Grid interfacing transformer

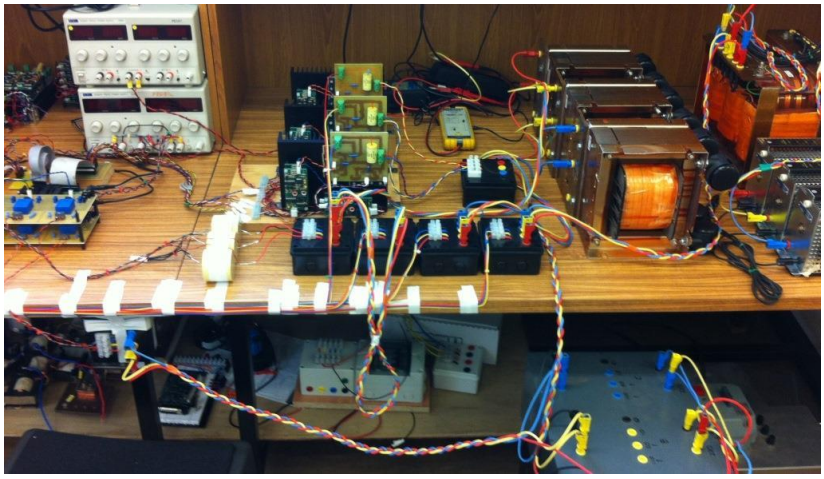


Fig.A-10. The photo of the test rig for two-level AC hexagonal chopper.

IV. The M2AHC test rig

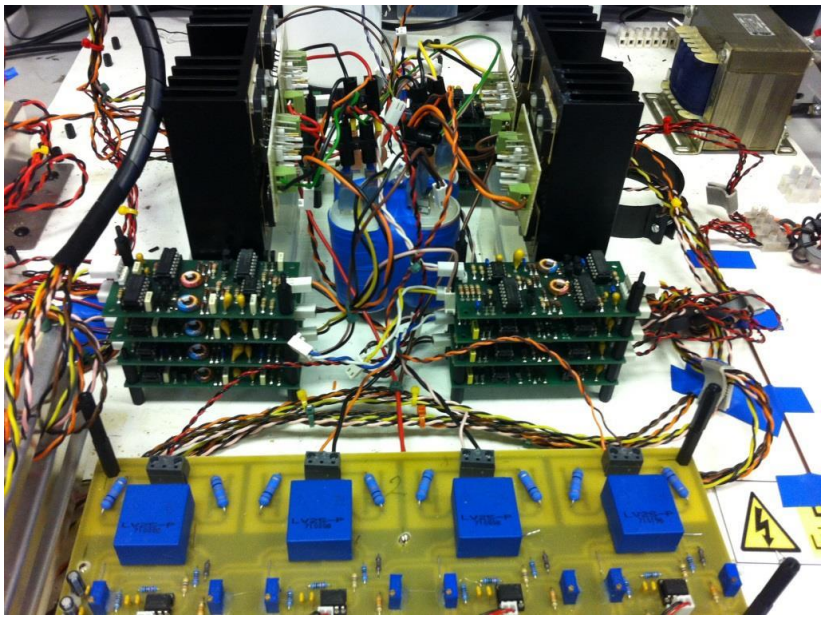


Fig.A-11. The photo of the test rig for single-phase M2AHC with two cells per arm.

The test rig for M2AHC with two cells per arm in Chapter 8 is shown in Fig.A-11. It consists of:

- TC1796 DSP controller
- AC cell capacitors
- AC chopper switching cells
- Gate drivers

- Voltage and current transducer
- AC input transformer and voltage regulator
- Auxiliary voltage source
- Input and output filters
- Arm inductors

V. The CTFB-HMC test rig

The test rig for single-phase CTFB-HMC with three cells in the chain-link in Chapter 6 is shown in Fig.A-12. It consists of:

- TC1796 DSP controller
- DC cell capacitors and DC-link capacitor
- Full-bridge switching cells
- Gate drivers
- Voltage and current transducer
- DC power supply and auxiliary voltage source
- Output filters and harmonic trap
- DC side inductors and circulating diode

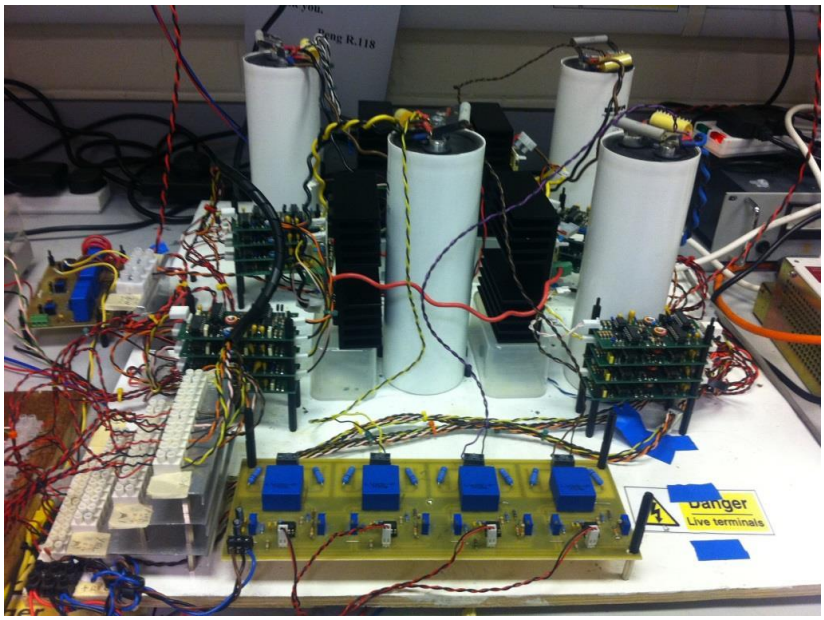


Fig.A-12. The photo of the test rig for singe-phase CTFB-HMC.

Appendix E. Sample Code for Verifications

I. The generalized modulation algorithm for N cells CTFB converter

```
function Outputs(block)
 global Nc;
 Vcell_Ascend = block.InputPort(1).Data;
 Iarm = block.InputPort(2).Data;
 Ref = block.InputPort(3).Data;
 Sx=zeros(1,4*(Nc+1));
 Non=round(Ref*Nc);
 Npn=floor((Nc-abs(Non))/2);
 N0=Nc-abs(Non)-2*Npn;
 if Non==Nc
        Sx(1)=1;
        Sx(2)=0;
        Sx(3)=0;
        Sx(4)=1;
        for jj=1:Nc
        Sx(4*jj+1)=1;
        Sx(4*jj+2)=0;
        Sx(4*jj+3)=0;
        Sx(4*jj+4)=1;
        end
 elseif Non==-Nc
        Sx(1)=0;
        Sx(2)=1;
        Sx(3)=1;
        Sx(4)=0;
        for jj=1:Nc
        Sx(4*jj+1)=0;
        Sx(4*jj+2)=1;
        Sx(4*jj+3)=1;
        Sx(4*jj+4)=0;
        end
 else % intermediate levels
        Sx(1)=0;
        Sx(2)=0;
        Sx(3)=0;
        Sx(4)=0;
        if(Iarm>=0)
           if Ref>=0
             for jj=1:Nc
               if jj<=Npn
                  Sx(4*Vcell_Ascend(jj)+1)=0;
                  Sx(4*Vcell_Ascend(jj)+2)=1;
                  Sx(4*Vcell_Ascend(jj)+3)=1;
                  Sx(4*Vcell_Ascend(jj)+4)=0;
               elseif jj<=Npn+N0
                  Sx(4*Vcell_Ascend(jj)+1)=1;
                  Sx(4*Vcell_Ascend(jj)+2)=0;
                  Sx(4*Vcell_Ascend(jj)+3)=1;
                  Sx(4*Vcell_Ascend(jj)+4)=0;
               else
                  Sx(4*Vcell_Ascend(jj)+1)=1;
                  Sx(4*Vcell_Ascend(jj)+2)=0;
                  Sx(4*Vcell_Ascend(jj)+3)=0;
                  Sx(4*Vcell_Ascend(jj)+4)=1;
```

```
        end
      end
    else % Ref<0
      for jj=1:Nc
       if jj<=abs(Non)+Npn
         Sx(4*Vcell_Ascend(jj)+1)=0;
         Sx(4*Vcell_Ascend(jj)+2)=1;
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
       elseif jj<=abs(Non)+Npn+N0
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=0;
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
       else
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=0;
         Sx(4*Vcell_Ascend(jj)+3)=0;
         Sx(4*Vcell_Ascend(jj)+4)=1;
       end
      end
    end
  else  %Iarm<0
    if Ref>=0
      for jj=1:Nc
       if jj<=abs(Non)+Npn
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=0;
         Sx(4*Vcell_Ascend(jj)+3)=0;
         Sx(4*Vcell_Ascend(jj)+4)=1;
       elseif jj<=abs(Non)+Npn+N0
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=0;
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
       else
         Sx(4*Vcell_Ascend(jj)+1)=0;
         Sx(4*Vcell_Ascend(jj)+2)=1;
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
       end
      end
    else % Ref<0
      for jj=1:Nc
       if jj<=Npn
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=0;
         Sx(4*Vcell_Ascend(jj)+3)=0;
         Sx(4*Vcell_Ascend(jj)+4)=1;
       elseif jj<=Npn+N0
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=0;
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
       else
         Sx(4*Vcell_Ascend(jj)+1)=0;
         Sx(4*Vcell_Ascend(jj)+2)=1;
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
```

```
            end
          end
        end
      end
    end
block.OutputPort(1).Data = Sx';
%endfunction
```

II. The PWM modulation algorithm for 3 cells CTFB converter

```
function Outputs(block)
 global Nc;
 global Ts;
 delta=Ts*0.0; % dead-babd
 Vcell_Ascend = block.InputPort(1).Data;
 Iarm = block.InputPort(2).Data;
 Ref = block.InputPort(3).Data;
 Sx=zeros(1,4*(1+Nc));
  if(Iarm>=0)
    if abs(Ref)>(Nc-1)/Nc&&abs(Ref)<=1 % +/-1, 1-2/3
     if Ref>=0
        Sx(1)=1-Nc*(1-Ref);%Nc*(Ref-(Nc-1)/Nc)
        Sx(2)=1;%means always turn-off because of the complementry comparison
        Sx(3)=0;
        Sx(4)=1;
        %bypass or positive   1,4--->2,4
        Sx(4*Vcell_Ascend(1)+1)=1-Nc*(1-Ref)-delta;%same as S1
        Sx(4*Vcell_Ascend(1)+2)=1-Nc*(1-Ref)+delta;% complementray as Sx(4*Vcell_Ascend(1)+1)
        Sx(4*Vcell_Ascend(1)+3)=0;
        Sx(4*Vcell_Ascend(1)+4)=1;
       if Nc>=2
        for jj=2:Nc   %positive
        Sx(4*Vcell_Ascend(jj)+1)=1;
        Sx(4*Vcell_Ascend(jj)+2)=1;%1 means turn off
        Sx(4*Vcell_Ascend(jj)+3)=0;
        Sx(4*Vcell_Ascend(jj)+4)=1;
        end
       end
     else %Ref<0
        Sx(1)=0;
        Sx(2)=Nc*(1+Ref);% complementray relation positive comparison means turn off
        Sx(3)=1;
        Sx(4)=0;
        %bypass or negative 1,3--->2,3
        Sx(4*Vcell_Ascend(Nc)+1)=Nc*(1+Ref)-delta;%Nc*(Ref+1)
        Sx(4*Vcell_Ascend(Nc)+2)=Nc*(1+Ref)+delta;%same as S2;complementray as above
        Sx(4*Vcell_Ascend(Nc)+3)=1;
        Sx(4*Vcell_Ascend(Nc)+4)=0;
       if Nc>=2
        for jj=1:Nc-1  %negative
        Sx(4*Vcell_Ascend(jj)+1)=0;
        Sx(4*Vcell_Ascend(jj)+2)=0;%0 means turn on
        Sx(4*Vcell_Ascend(jj)+3)=1;
        Sx(4*Vcell_Ascend(jj)+4)=0;
        end
       end
     end
    elseif abs(Ref)>(Nc-2)/Nc&&abs(Ref)<=(Nc-1)/Nc % +/-(Nc-1)/Nc, 2/3-1/3
     if Ref>=0
        Sx(1)=0;
```

```
    Sx(2)=1;%1 means turn off
    Sx(3)=0;
    Sx(4)=0;
    %smallest bypass or negative(be charged) 1,3-->2,3
    Sx(4*Vcell_Ascend(1)+1)=2-Nc*(1-Ref)-delta;%Nc*(Ref-(Nc-2)/Nc)
    Sx(4*Vcell_Ascend(1)+2)=2-Nc*(1-Ref)+delta;%complementray relationship as above
    Sx(4*Vcell_Ascend(1)+3)=1;
    Sx(4*Vcell_Ascend(1)+4)=0;
   if Nc>=2 %positive
    for jj=2:Nc
    Sx(4*Vcell_Ascend(jj)+1)=1;
    Sx(4*Vcell_Ascend(jj)+2)=1;%1 means turn off
    Sx(4*Vcell_Ascend(jj)+3)=0;
    Sx(4*Vcell_Ascend(jj)+4)=1;
    end
   end
 else %Ref<0
    Sx(1)=0;
    Sx(2)=1;%1 means turn off
    Sx(3)=0;
    Sx(4)=0;
    %largest bypass or positive(be discharged) 2,4-->1,4
    Sx(4*Vcell_Ascend(Nc)+1)=Nc*(1+Ref)-1-delta;%Nc*(Ref+(Nc-1)/Nc)
    Sx(4*Vcell_Ascend(Nc)+2)=Nc*(1+Ref)-1+delta;%complementray relationship as above
    Sx(4*Vcell_Ascend(Nc)+3)=0;
    Sx(4*Vcell_Ascend(Nc)+4)=1;
   if Nc>=2
    for jj=1:Nc-1  %negative
    Sx(4*Vcell_Ascend(jj)+1)=0;
    Sx(4*Vcell_Ascend(jj)+2)=0;%0 means turn on
    Sx(4*Vcell_Ascend(jj)+3)=1;
    Sx(4*Vcell_Ascend(jj)+4)=0;
    end
   end
 end
elseif abs(Ref)>=(Nc-3)/Nc&&abs(Ref)<=(Nc-2)/Nc % +/-(Nc-2)/Nc, 1/3-0
 if Ref>=0
    Sx(1)=0;
    Sx(2)=1; % 1 means turn off
    Sx(3)=0;
    Sx(4)=0;
    % positive and discharged
    Sx(4*Vcell_Ascend(Nc)+1)=1;
    Sx(4*Vcell_Ascend(Nc)+2)=1;% 1 means turn off
    Sx(4*Vcell_Ascend(Nc)+3)=0;
    Sx(4*Vcell_Ascend(Nc)+4)=1;
    % negative and charged
    Sx(4*Vcell_Ascend(1)+1)=0;
    Sx(4*Vcell_Ascend(1)+2)=0;% 0 means turn on
    Sx(4*Vcell_Ascend(1)+3)=1;
    Sx(4*Vcell_Ascend(1)+4)=0;
    if Nc>=3 %positive or bypass +1 or 0, 1,4--->2,4
    for jj=2:Nc-1
    Sx(4*Vcell_Ascend(jj)+1)=3-Nc*(1-Ref)-delta;%Nc*(Ref-(Nc-3)/Nc)
    Sx(4*Vcell_Ascend(jj)+2)=3-Nc*(1-Ref)-delta;%complementry comparison action as above
    Sx(4*Vcell_Ascend(jj)+3)=0;
    Sx(4*Vcell_Ascend(jj)+4)=1;
    end
   end
```

```
      else %Ref<0
         Sx(1)=0;
         Sx(2)=1;% 1 means turn off
         Sx(3)=0;
         Sx(4)=0;
         % positive and discharged
         Sx(4*Vcell_Ascend(Nc)+1)=1;
         Sx(4*Vcell_Ascend(Nc)+2)=1;% 1 means turn off
         Sx(4*Vcell_Ascend(Nc)+3)=0;
         Sx(4*Vcell_Ascend(Nc)+4)=1;
         % negative and charged
         Sx(4*Vcell_Ascend(1)+1)=0;
         Sx(4*Vcell_Ascend(1)+2)=0;% 0 means turn on
         Sx(4*Vcell_Ascend(1)+3)=1;
         Sx(4*Vcell_Ascend(1)+4)=0;
         if Nc>=3 %negative or bypass -1 or 0, 2,3--->1,3
         for jj=2:Nc-1
         Sx(4*Vcell_Ascend(jj)+1)=Nc*(1+Ref)-2-delta;%1-Nc*(Ref-(Nc-3)/Nc)
         Sx(4*Vcell_Ascend(jj)+2)=Nc*(1+Ref)-2-delta;%complementry comparison action as above
         Sx(4*Vcell_Ascend(jj)+3)=1;
         Sx(4*Vcell_Ascend(jj)+4)=0;
         end
        end
      end
    end
  else
    %Iarm<0
   if abs(Ref)>(Nc-1)/Nc&&abs(Ref)<=1 % +/-1, 1-2/3
     if Ref>=0
         Sx(1)=1-Nc*(1-Ref);%Nc*(Ref-(Nc-1)/Nc)
         Sx(2)=1;% 1 means turn off
         Sx(3)=0;
         Sx(4)=1;
         %bypass or positive   1,4--->2,4
         Sx(4*Vcell_Ascend(Nc)+1)=1-Nc*(1-Ref)-delta;%same as S1
         Sx(4*Vcell_Ascend(Nc)+2)=1-Nc*(1-Ref)+delta;% complementray as
Sx(4*Vcell_Ascend(1)+1)
         Sx(4*Vcell_Ascend(Nc)+3)=0;
         Sx(4*Vcell_Ascend(Nc)+4)=1;
        if Nc>=2
         for jj=1:Nc-1   %positive
         Sx(4*Vcell_Ascend(jj)+1)=1;
         Sx(4*Vcell_Ascend(jj)+2)=1;% 1 means turn off
         Sx(4*Vcell_Ascend(jj)+3)=0;
         Sx(4*Vcell_Ascend(jj)+4)=1;
         end
        end
      else %Ref<0
         Sx(1)=0;
         Sx(2)=Nc*(1+Ref);% complementray relation positive comparison means turn off
         Sx(3)=1;
         Sx(4)=0;
         %bypass or negative 1,3--->2,3
         Sx(4*Vcell_Ascend(1)+1)=Nc*(1+Ref)-delta;%
         Sx(4*Vcell_Ascend(1)+2)=Nc*(1+Ref)+delta;%same as S2;complementray as above
         Sx(4*Vcell_Ascend(1)+3)=1;
         Sx(4*Vcell_Ascend(1)+4)=0;
        if Nc>=2
         for jj=2:Nc  %negative
```

```
    Sx(4*Vcell_Ascend(jj)+1)=0;
    Sx(4*Vcell_Ascend(jj)+2)=0;% 0 means turn on
    Sx(4*Vcell_Ascend(jj)+3)=1;
    Sx(4*Vcell_Ascend(jj)+4)=0;
    end
   end
  end
elseif abs(Ref)>(Nc-2)/Nc&&abs(Ref)<=(Nc-1)/Nc % +/-(Nc-1)/Nc, 2/3-1/3
  if Ref>=0
    Sx(1)=0;
    Sx(2)=1;% 1 means turn off
    Sx(3)=0;
    Sx(4)=0;
    %largest bypass or negative(be discharged) 1,3-->2,3
    Sx(4*Vcell_Ascend(Nc)+1)=2-Nc*(1-Ref)-delta;%Nc*(Ref-(Nc-2)/Nc)
    Sx(4*Vcell_Ascend(Nc)+2)=2-Nc*(1-Ref)+delta;%complementray relationship as above
    Sx(4*Vcell_Ascend(Nc)+3)=1;
    Sx(4*Vcell_Ascend(Nc)+4)=0;
   if Nc>=2 %positive
    for jj=1:Nc-1
    Sx(4*Vcell_Ascend(jj)+1)=1;
    Sx(4*Vcell_Ascend(jj)+2)=1;% 1 means turn off
    Sx(4*Vcell_Ascend(jj)+3)=0;
    Sx(4*Vcell_Ascend(jj)+4)=1;
    end
   end
  else %Ref<0
    Sx(1)=0;
    Sx(2)=1;% 1 means turn off
    Sx(3)=0;
    Sx(4)=0;
    %smallest bypass or positive(be charged) 2,4-->1,4
    Sx(4*Vcell_Ascend(1)+1)=Nc*(1+Ref)-1-delta;%Nc*(Ref+(Nc-1)/Nc)
    Sx(4*Vcell_Ascend(1)+2)=Nc*(1+Ref)-1+delta;%complementray relationship as above
    Sx(4*Vcell_Ascend(1)+3)=0;
    Sx(4*Vcell_Ascend(1)+4)=1;
   if Nc>=2
    for jj=2:Nc  %negative
    Sx(4*Vcell_Ascend(jj)+1)=0;
    Sx(4*Vcell_Ascend(jj)+2)=0;% 0 means turn on
    Sx(4*Vcell_Ascend(jj)+3)=1;
    Sx(4*Vcell_Ascend(jj)+4)=0;
    end
   end
  end
elseif abs(Ref)>=(Nc-3)/Nc&&abs(Ref)<=(Nc-2)/Nc % +/-(Nc-2)/Nc, 1/3-0
  if Ref>=0
    Sx(1)=0;
    Sx(2)=1;% 1 means turn off
    Sx(3)=0;
    Sx(4)=0;
    % positive and charged
    Sx(4*Vcell_Ascend(1)+1)=1;
    Sx(4*Vcell_Ascend(1)+2)=1;% 1 means turn off
    Sx(4*Vcell_Ascend(1)+3)=0;
    Sx(4*Vcell_Ascend(1)+4)=1;
    % negative and discharged
    Sx(4*Vcell_Ascend(Nc)+1)=0;
    Sx(4*Vcell_Ascend(Nc)+2)=0;% 0 means turn on
```

```
        Sx(4*Vcell_Ascend(Nc)+3)=1;
        Sx(4*Vcell_Ascend(Nc)+4)=0;
        if Nc>=3 %positive or bypass +1 or 0, 1,4--->2,4
        for jj=2:Nc-1
        Sx(4*Vcell_Ascend(jj)+1)=3-Nc*(1-Ref)-delta;%Nc*(Ref-(Nc-3)/Nc)
        Sx(4*Vcell_Ascend(jj)+2)=3-Nc*(1-Ref)-delta;%complementry comparison action as above
        Sx(4*Vcell_Ascend(jj)+3)=0;
        Sx(4*Vcell_Ascend(jj)+4)=1;
        end
       end
     else %Ref<0
        Sx(1)=0;
        Sx(2)=1;% 1 means turn off
        Sx(3)=0;
        Sx(4)=0;
        % positive and charged
        Sx(4*Vcell_Ascend(1)+1)=1;
        Sx(4*Vcell_Ascend(1)+2)=1;% 1 means turn off
        Sx(4*Vcell_Ascend(1)+3)=0;
        Sx(4*Vcell_Ascend(1)+4)=1;
        % negative and discharged
        Sx(4*Vcell_Ascend(Nc)+1)=0;
        Sx(4*Vcell_Ascend(Nc)+2)=0;% 0 means turn on
        Sx(4*Vcell_Ascend(Nc)+3)=1;
        Sx(4*Vcell_Ascend(Nc)+4)=0;
        if Nc>=3 %negative or bypass -1 or 0, 2,3--->1,3
        for jj=2:Nc-1
        Sx(4*Vcell_Ascend(jj)+1)=Nc*(1+Ref)-2-delta;%1-Nc*(Ref-(Nc-3)/Nc)
        Sx(4*Vcell_Ascend(jj)+2)=Nc*(1+Ref)-2-delta;%complementry comparison action as above
        Sx(4*Vcell_Ascend(jj)+3)=1;
        Sx(4*Vcell_Ascend(jj)+4)=0;
        end
       end
     end
   end
 end
 block.OutputPort(1).Data = Sx';
%endfunction
```

III. The PWM modulation algorithm for 2 cells M2AHC

```
function [ra11,ra12,ra21,ra22,rb11,rb12,rb21,rb22,rc11,rc12,rc21,rc22,rd11,rd12,rd21,rd22] =
MMC(eab,ecd,il,ref,deadband,delta,Ts)
%#codegen
   ra11=0;
   ra12=0;
   ra21=0;
   ra22=0;
   rb11=0;
   rb12=0;
   rb21=0;
   rb22=0;
   rc11=0;
   rc12=0;
   rc21=0;
   rc22=0;
   rd11=0;
   rd12=0;
   rd21=0;
   rd22=0;
```

```
% Initialization
if il>=0
if eab>=0&&ecd>=0 %2 3
   ra11=0.5+0.5*ref;
   ra12=0.5-0.5*ref;
   ra21=0.5-0.5*ref+deadband/Ts;
   ra22=0.5+0.5*ref-deadband/Ts;
   rb11=0.5+0.5*ref-delta/Ts;
   rb12=0.5-0.5*ref+delta/Ts;
   rb21=0.5-0.5*ref+deadband/Ts+delta/Ts;
   rb22=0.5+0.5*ref-deadband/Ts-delta/Ts;
   rc11=0.5-0.5*ref;
   rc12=0.5+0.5*ref;
   rc21=0.5+0.5*ref+deadband/Ts;
   rc22=0.5-0.5*ref-deadband/Ts;
   rd11=0.5-0.5*ref+delta/Ts;
   rd12=0.5+0.5*ref-delta/Ts;
   rd21=0.5+0.5*ref+deadband/Ts-delta/Ts;
   rd22=0.5-0.5*ref-deadband/Ts+delta/Ts;
elseif eab>=0&&ecd<0 %2 4
   ra11=0.5+0.5*ref;
   ra12=0.5-0.5*ref;
   ra21=0.5-0.5*ref+deadband/Ts;
   ra22=0.5+0.5*ref-deadband/Ts;
   rb11=0.5+0.5*ref-delta/Ts;
   rb12=0.5-0.5*ref+delta/Ts;
   rb21=0.5-0.5*ref+deadband/Ts+delta/Ts;
   rb22=0.5+0.5*ref-deadband/Ts-delta/Ts;
   rd11=0.5-0.5*ref;
   rd12=0.5+0.5*ref;
   rd21=0.5+0.5*ref+deadband/Ts;
   rd22=0.5-0.5*ref-deadband/Ts;
   rc11=0.5-0.5*ref+delta/Ts;
   rc12=0.5+0.5*ref-delta/Ts;
   rc21=0.5+0.5*ref+deadband/Ts-delta/Ts;
   rc22=0.5-0.5*ref-deadband/Ts+delta/Ts;
elseif eab<0&&ecd>=0 %1 3
   rb11=0.5+0.5*ref;
   rb12=0.5-0.5*ref;
   rb21=0.5-0.5*ref+deadband/Ts;
   rb22=0.5+0.5*ref-deadband/Ts;
   ra11=0.5+0.5*ref-delta/Ts;
   ra12=0.5-0.5*ref+delta/Ts;
   ra21=0.5-0.5*ref+deadband/Ts+delta/Ts;
   ra22=0.5+0.5*ref-deadband/Ts-delta/Ts;
   rc11=0.5-0.5*ref;
   rc12=0.5+0.5*ref;
   rc21=0.5+0.5*ref+deadband/Ts;
   rc22=0.5-0.5*ref-deadband/Ts;
   rd11=0.5-0.5*ref+delta/Ts;
   rd12=0.5+0.5*ref-delta/Ts;
   rd21=0.5+0.5*ref+deadband/Ts-delta/Ts;
   rd22=0.5-0.5*ref-deadband/Ts+delta/Ts;
elseif eab<0&&ecd<0 %1 4
   rb11=0.5+0.5*ref;
   rb12=0.5-0.5*ref;
   rb21=0.5-0.5*ref+deadband/Ts;
   rb22=0.5+0.5*ref-deadband/Ts;
   ra11=0.5+0.5*ref-delta/Ts;
```

```
    ra12=0.5-0.5*ref+delta/Ts;
    ra21=0.5-0.5*ref+deadband/Ts+delta/Ts;
    ra22=0.5+0.5*ref-deadband/Ts-delta/Ts;
    rd11=0.5-0.5*ref;
    rd12=0.5+0.5*ref;
    rd21=0.5+0.5*ref+deadband/Ts;
    rd22=0.5-0.5*ref-deadband/Ts;
    rc11=0.5-0.5*ref+delta/Ts;
    rc12=0.5+0.5*ref-delta/Ts;
    rc21=0.5+0.5*ref+deadband/Ts-delta/Ts;
    rc22=0.5-0.5*ref-deadband/Ts+delta/Ts;
  end
  elseif il<0
   if eab>=0&&ecd>=0 %1 4
    rb11=0.5+0.5*ref;
    rb12=0.5-0.5*ref;
    rb21=0.5-0.5*ref+deadband/Ts;
    rb22=0.5+0.5*ref-deadband/Ts;
    ra11=0.5+0.5*ref-delta/Ts;
    ra12=0.5-0.5*ref+delta/Ts;
    ra21=0.5-0.5*ref+deadband/Ts+delta/Ts;
    ra22=0.5+0.5*ref-deadband/Ts-delta/Ts;
    rd11=0.5-0.5*ref;
    rd12=0.5+0.5*ref;
    rd21=0.5+0.5*ref+deadband/Ts;
    rd22=0.5-0.5*ref-deadband/Ts;
    rc11=0.5-0.5*ref+delta/Ts;
    rc12=0.5+0.5*ref-delta/Ts;
    rc21=0.5+0.5*ref+deadband/Ts-delta/Ts;
    rc22=0.5-0.5*ref-deadband/Ts+delta/Ts;
  elseif eab>=0&&ecd<0 %1 3
    rb11=0.5+0.5*ref;
    rb12=0.5-0.5*ref;
    rb21=0.5-0.5*ref+deadband/Ts;
    rb22=0.5+0.5*ref-deadband/Ts;
    ra11=0.5+0.5*ref-delta/Ts;
    ra12=0.5-0.5*ref+delta/Ts;
    ra21=0.5-0.5*ref+deadband/Ts+delta/Ts;
    ra22=0.5+0.5*ref-deadband/Ts-delta/Ts;
    rc11=0.5-0.5*ref;
    rc12=0.5+0.5*ref;
    rc21=0.5+0.5*ref+deadband/Ts;
    rc22=0.5-0.5*ref-deadband/Ts;
    rd11=0.5-0.5*ref+delta/Ts;
    rd12=0.5+0.5*ref-delta/Ts;
    rd21=0.5+0.5*ref+deadband/Ts-delta/Ts;
    rd22=0.5-0.5*ref-deadband/Ts+delta/Ts;
  elseif eab<0&&ecd>=0 %2 4
    ra11=0.5+0.5*ref;
    ra12=0.5-0.5*ref;
    ra21=0.5-0.5*ref+deadband/Ts;
    ra22=0.5+0.5*ref-deadband/Ts;
    rb11=0.5+0.5*ref-delta/Ts;
    rb12=0.5-0.5*ref+delta/Ts;
    rb21=0.5-0.5*ref+deadband/Ts+delta/Ts;
    rb22=0.5+0.5*ref-deadband/Ts-delta/Ts;
    rd11=0.5-0.5*ref;
    rd12=0.5+0.5*ref;
    rd21=0.5+0.5*ref+deadband/Ts;
```

```
    rd22=0.5-0.5*ref-deadband/Ts;
    rc11=0.5-0.5*ref+delta/Ts;
    rc12=0.5+0.5*ref-delta/Ts;
    rc21=0.5+0.5*ref+deadband/Ts-delta/Ts;
    rc22=0.5-0.5*ref-deadband/Ts+delta/Ts;
elseif eab<0&&ecd<0 %2 3
    ra11=0.5+0.5*ref;
    ra12=0.5-0.5*ref;
    ra21=0.5-0.5*ref+deadband/Ts;
    ra22=0.5+0.5*ref-deadband/Ts;
    rb11=0.5+0.5*ref-delta/Ts;
    rb12=0.5-0.5*ref+delta/Ts;
    rb21=0.5-0.5*ref+deadband/Ts+delta/Ts;
    rb22=0.5+0.5*ref-deadband/Ts-delta/Ts;
    rc11=0.5-0.5*ref;
    rc12=0.5+0.5*ref;
    rc21=0.5+0.5*ref+deadband/Ts;
    rc22=0.5-0.5*ref-deadband/Ts;
    rd11=0.5-0.5*ref+delta/Ts;
    rd12=0.5+0.5*ref-delta/Ts;
    rd21=0.5+0.5*ref+deadband/Ts-delta/Ts;
    rd22=0.5-0.5*ref-deadband/Ts+delta/Ts;
end
end
end
```

IV. The modulation algorithm for N cells M2AHC

Upper arm:

```
function Outputs(block)
 global Nc;
 global Ts;
 delta=Ts*0.08/(Nc-1);
 Vcell_Ascend = block.InputPort(1).Data;
 Iarm = block.InputPort(2).Data;
 Ref = block.InputPort(3).Data;
 Sx=zeros(1,Nc);
  if(Iarm>=0)
     for jj=1:Nc
        Sx(Vcell_Ascend(jj))=Ref-(Nc-jj)*delta/Ts;
     end
  else
     %Iarm<0
     for jj=1:Nc
        Sx(Vcell_Ascend(Nc-jj+1))=Ref-(Nc-jj)*delta/Ts;
     end
  end
 block.OutputPort(1).Data = Sx';
%endfunction
```

Lower arm:

```
function Outputs(block)
 global Nc;
 global Ts;
 delta=Ts*0.08/(Nc-1);
 Vcell_Ascend = block.InputPort(1).Data;
```

```
 Iarm = block.InputPort(2).Data;
 Ref = block.InputPort(3).Data;
 Sx=zeros(1,Nc);
  if(Iarm>=0)
     for jj=1:Nc
        Sx(Vcell_Ascend(jj))=Ref-(jj-1)*delta/Ts;
     end
  else
     %Iarm<0
     for jj=1:Nc
        Sx(Vcell_Ascend(Nc-jj+1))=Ref-(jj-1)*delta/Ts;
     end
  end
 block.OutputPort(1).Data = Sx';
%endfunction
```

Appendix F. List of Figures

Appendix G. List of Tables

Appendix H. Publication Output

Journal Publications

1. **Peng Li**, Y. Wang, G. Adam, D. Holliday, and B. Williams, "Three-Phase AC-AC Hexagonal Chopper System with Heterodyne Modulation for Power Flow Control Enhancement," *Power Electronics, IEEE Transactions on*, vol. 30, no. 10, pp. 5508-5521, Oct. 2015.

   Abstract: This paper proposes a three-phase AC chopper system for the interconnection of various distributed generation (DG) farms or main utilities to enhance the active and reactive power flow control. The absence of large energy storage component in direct AC-AC converter makes the system footprint small and reliable. As the interface for different AC sources, the presented converter can be configured as star or delta. However, delta connection is preferred as it can trap the potential zero-sequence current and reduce the current rating of the switching devices. In this way, the proposed converter resembles the hexagonal chopper, and it offers an inherent degree of freedom for output voltage phase-shifting. Considering the scalability in high voltage applications, a new version of the hexagonal chopper with half-bridge cell modular multilevel structure is developed. The modular multilevel AC hexagonal chopper (M2AHC) is operated in quasi-2-level mode to suppress the electro-magnetic interference (EMI) caused by high voltage switching. Quasi-2-level operation divides the voltage level transition into multi-steps, diminishing the voltage rising and falling rates (dv/dt) in high voltage condition. Then, heterodyne modulation is adopted for the presented chopper system, supplying a new degree of freedom to decouple the phase and amplitude regulation. Based on this idea, system control strategy is developed in synchronous reference frame (SRF). Simulations and experimentations have confirmed the validity of the proposed approaches

2. **Peng Li**, G. Adam, Y. Hu, D. Holliday, and B. W. Williams, "Three-Phase AC-Side Voltage-Doubling High Power Density Voltage Source Converter With Intrinsic Buck-Boost Cell and Common-Mode Voltage Suppression," *Power Electronics, IEEE Transactions on*, vol. 30, no. 9, pp. 5284-5298, Sep. 2015.

Abstract: The three-phase two-level voltage source converter (VSC) is widely employed in power conversions between AC and DC for its four-quadrant operation and control flexibility. However, it suffers from the low output voltage range with a peak value of half DC-link per phase, which necessitates the use of either high DC-link voltage or bulky step-up transformer to enable the medium voltage operation. Additionally, the high common mode (CM) voltage between AC loads neutral points and ground may reduce the service life and reliability of electric machinery. In this paper, a three-phase AC side voltage-doubling VSC topology with intrinsic Buck-Boost cell is analyzed. By this configuration, the AC side voltage is doubled with the phase peak value equal to DC-link. That is, only half of the DC side capacitor bank is needed to generate the same output voltage. The proposed converter uses its buck-boost cell as a virtual voltage source to synthesize negative half of the output voltage by modulating its output AC phase voltage around the negative bus (which is the real zero when grounded). This permits the average CM voltage to be suppressed to zero, and loads connected to converter AC side not to withstand any DC voltage stress (reducing the insulation requirement). Modeling and control design for both rectifier and inverter modes of this converter in synchronous reference frame have been investigated to ensure a four-quadrant three-phase back-to-back system. Experimental results have verified the feasibility and the effectiveness of the proposed configuration and the designed control strategies.

Submitted Journal Papers

3. **Peng Li**, G. Adam, Y. Wang, D. Holliday, and B. Williams, "Controlled Transition Full-bridge Hybrid Multilevel Converter with Chain-links of Full-bridge Cells," *Power Electronics, IEEE Transactions on*, (submitted).

   Abstract: This paper proposes the controlled transition full-bridge (CTFB) hybrid multilevel converter (HMC) for medium and high voltage applications, which employs a full-bridge cell chain-link (FB-CL) between the two legs in each phase to generate multilevel bipolar output voltage. The CTFB-HMC has twice DC voltage utilization or power density of conventional converters due to the bipolar capability of its full-bridge configuration. Hence, for the same power

rating and same voltage level number, its total cells per phase are quarter of that in MMC, reducing the hardware installation volume. Also, the total device number in the conduction paths is the same as in HB-MMC; thus, improving the efficiency performance. Besides, for the CTFB converter, its FB-CL current has no DC component, which offers the potential to enhance the transient response. Comparative studies between the CTFB and other multilevel topologies are carried out to show its main features. Modulation strategies and parameter sizing of the proposed converter are investigated using a generic case. Simulation and experimental results are used to verify the effectiveness of the proposed approach.

4. **Peng Li**, Y. Wang, G. Adam, D. Holliday, and B. Williams, "New Breed of FACTS Devices Using a Modular Multilevel AC Hexagonal Chopper," *Power Delivery, IEEE Transactions on*, (submitted).

   Abstract: This paper proposes a new breed of FACTS device based on direct AC-AC conversion, where modular multilevel AC hexagonal chopper (M2AHC) is employed. The M2AHC is operated in quasi-two-level mode; and the heterodyne modulation is used to decouple voltage amplitude regulation from that of the phase shift; thus, independent control of active and reactive power is achieved. Then, a family of FACTS devices based on M2AHC that offers voltage, active power and reactive power flow control in both shunt and series compensations is analysed. The use of AC cell capacitors instead of DC capacitors in M2AHC makes its footprint much smaller and lighter than conventional AC-DC or DC-AC voltage source converter (VSC) based FACTS devices; hence, high reliability and extended service life could be expected. The modelling and controller design of the proposed FACTS devices are illustrated in a unified reference frame, considering different control modes, transient and unbalanced conditions. Simulation results are used to verify the feasibility of the proposed M2AHC based FACTS device.

5. **Peng Li**, G. Adam, D. Holliday, and B. Williams, "ACVD-VSC Based High Power Density FACTS Devices with Extended Control Range," *Power Delivery, IEEE Transactions on*, (submitted).

Abstract: This paper proposes a new family of flexible AC transmission system (FACTS) devices based on the ac-side voltage doubling voltage source converter (ACVD-VSC), which has twice of the DC-link utilization as a two-level VSC, hence improved power density per unit DC-link voltage. This means its DC voltage limit for reactive power generation is higher than that for the conventional static synchronous compensator (STATCOM) and the static synchronous series compensator (SSSC). Therefore, extended control ranges result for all members in the proposed family of FACTS devices. Also the ACVD converter has zero DC common mode voltage between the AC side neutral point and the DC-link negative terminal, reducing the insulation level for the interfacing transformer when the negative DC bus is grounded. The basic operation principles of ACVD-VSC are reviewed. Then, it is used in FACTS devices to perform voltage or power flow control as shunt or series compensators. The STATCOM and SSSC using the ACVD-VSC are analyzed and tested under different control modes including transients. The practical results presented to verify the feasibility of the proposed schemes, are discussed.

Conference Papers

6. G. Adam, **Peng. Li**, I. Gowaid, and B. Williams "Generalized switching function model of modular multilevel converter", *Industrial Technology (ICIT), 2015 IEEE International Conference on*, pp. 2702-2707, 17-19 March 2015.

   Abstract: this paper presents a generalized switching function model of the modular multilevel converter (MMC) that can be used instead of MMC electromagnetic transient simulation model for full-scale simulations of high-voltage DC (HVDC) and flexible AC transmission systems (FACTS). The proposed method is computationally more efficient and numerically stable than its electromagnetic transient simulation counterpart, and it is applicable for wide range of studies, including ac and dc network faults. The proposed switching function model is packaged in a graphical form to suit various simulation platforms such as Simulink and PSCAD. The validity of the presented model is confirmed using simulation and its scalability has been demonstrated on MMC with 301 cells per arm, considering power reversal during normal operation and DC short circuit fault.