DC/DC Converter for Offshore DC Collection Network

Yiqing Lian

A thesis presented in fulfilment of the requirements for the degree of Doctor of Philosophy

March 2016

Institute of Energy and Environment
Department of Electronic and Electrical Engineering
University of Strathclyde
Glasgow
UK

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Date:

Dedicated to my family

Abstract

Large wind farms, especially large offshore wind farms, present a challenge for the electrical networks that will provide interconnection of turbines and onward transmission to the onshore power network. High wind farm capacity combined with a move to larger wind turbines will result in a large geographical footprint requiring a substantial sub-sea power network to provide internal interconnection. While advanced HVDC transmission has addressed the issue of long-distance transmission, internal wind farm power networks have seen relatively little innovation. Recent studies have highlighted the potential benefits of DC collection networks. First with appropriate selection of DC voltage, reduced losses can be expected. In addition, the size and weight of the electrical plant may also be reduced through the use of medium- or high-frequency transformers to step up the generator output voltage for connection to a medium-voltage network suitable for wide-area interconnection. However, achieving DC/DC conversion at the required voltage and power levels presents a significant challenge for wind-turbine power electronics.

This thesis first proposes a modular DC/DC converter with input-parallel output-series connection, consisting of full-bridge DC/DC modules. A new master-slave control scheme is developed to ensure power sharing under all operating conditions, including during failure of a master module by allowing the status of master module to be reallocated to another healthy module. Secondly, a novel modular DC/DC converter with input-series-input-parallel output-series connection is presented. In addition, a robust control scheme is developed to ensure power sharing between practical modules even where modules have mismatched parameters or when there is a faulted module. Further, the control strategy is able to isolate faulted modules to ensure fault ride-through during internal module faults, whilst maintaining good transient performance. The ISIPOS connection is then applied to a converter with bidirectional power flow capability, realised using dual-active bridge modules.

The small- and large-signal analyses of the proposed converters are performed in order to deduce the control structure for the converter input and output stages. Simulation and experimental results demonstrate and validate the proposed converters and associated control schemes.

Acknowledgement

First and foremost I would like to thank Prof. Stephen Finney and Dr. Derrick Holliday for their constructive supervision and invaluable guidance throughout the duration of my Ph.D study and also Professor Bill Leithead, who gave me the opportunity to conduct this work. My Ph.D journey would not have been possible without their continuous support. Special cordial thanks to all colleagues in PEDEC research group and CDT research group and particular thanks are due to Dr. Grain Philip Adam for his valuable suggestions to my work and Mr Charles Croser, Dr. Tee Lim for the guidance whilst building the laboratory test rig. Also I am very grateful for the help of Mr Drew Smith without whom the CDT would not be so successful.

The work is supported by EPSRC Centre for Doctoral Training in Wind Energy System and the Underpinning Power Electronics 2012: Converter Theme research programme and I would like to acknowledge them for their financial support. A gracious acknowledgement is also made to Electronic and Electrical department of University of Strathclyde, thanks to everyone who helped me to get through this memorable Ph.D journey.

Last, but not least, I would like to thank my family, my beloved husband, my beloved mother, my beloved father and my beloved mother-in-law, for their unconditional support and continued love.

List of Symbols

The following are the symbols and abbreviations used throughout this thesis.

Δd_1	Duty cycle perturbation
Δi_{lf}	Inductor current perturbation
Δv_{in}	Input voltage perturbation
Δv_o	Capacitor voltage perturbation
Br	Residual magnetic flux density
Bs	Saturation magnetic flux density
C_d	Input capacitance
C_f	Filter capacitance
C_n	*n*th module output capacitance
D_e	Effective duty cycle
D_{max}	Maximum duty cycle
E_c	Energy
f_s	Switching frequency
I_{in}	Input current
I_{inn}	*n*th module input current
I_o	Load current
I_{out}	Output current
J	Current density
k	Transformer turn-ratio
k_d	Derivative gain
k_p	Proportion gain
K_u	Window utilisation factor
L_f	Filter inductance
L_n	*n*th module output inductance
L_r	Transformer leakage inductance
n_{ideal}	Ideal urn-ratio
P_{in}	Input power
P_{out}	Output power
R_{ESR}	Equivalent series resistance

R_o	Load
$v(x)$	Lyapunov function
V_c	Capacitor voltage
V_{dc}	DC side voltage
V_{in}	Input voltage
v_o*	Output voltage reference signal
V_{on}	*n*th module output voltage
V_{out}	Output voltage
V_{pri}	Transformer primary voltage
v_{re}	Rectifier output average voltage
V_{sec}	Transformer secondary voltage
W_{iv}	Weighting factor
μ_{iv}	Distribution factor
Φ	Phase shift angle
η_t	Transformer efficiency

List of Abbreviations

CHB	Cascaded H-bridge
DAB	Dual-active-bridge
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
HVAC	High-voltage AC
HVDC	High-voltage DC
ICS	Input current sharing
IPOP	Input-parallel output-parallel
IPOS	Input-parallel output-series
ISIPOS	Input-series-input-parallel output-parallel
ISOP	Input-series output-parallel
ISOS	Input-series output-series
IVS	Input voltage sharing
M2C	Modular multilevel converter
MVAC	Medium-voltage AC
NPC	Neutral-point-clamped
OCS	Output current sharing
OVS	Output voltage sharing
PRC	Parallel resonant converter
PSMC	Parallel-series modular converter
PSM	Phase shift modulation
PWM	Pulse width modulation
SPRC	Series-parallel resonant converter
STATCOM	Static synchronous compensator
VSC	Voltage source converter
ZCS	Zero current switching
ZVS	Zero voltage switching

Table of Contents

Chapter 1: Introduction

The environmental benefits and cost-competitiveness of wind power have driven its rapid expansion in recent decades, particularly onshore wind farms. Difficulties of obtained planning permission for onshore wind farms in recent years have forced the power industry to pay attention to the possible exploitation of the vast wind resources available offshore to generate large amounts of power. Consequently, research on collection networks and high-power converters are driven by the predicted growth of offshore wind deployment. In this chapter, the advantages of DC collection networks and possible DC/DC converters are outlined. In addition, the objectives of this thesis are identified and thesis organization delivers a view of the following chapters.

1.1 Renewable Energy Development

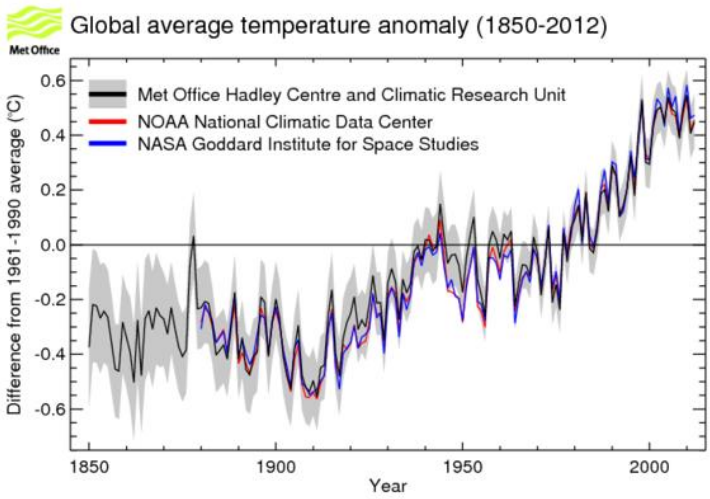


Fig.1.1: Global average temperature anomaly [1]

Since the early 20th century, the global average temperature has significantly increased as shown in Fig.1.1. A surge in temperature increase can be observed during recent decades due to the rapid increase in fossil energy consumption. Climate change has also caused the sea level to rise, for example the sea level around the UK has risen 10 cm since 1900 [2]. These environmental problems, such as climate change, sea level rise and air pollution, have become a major global problem. In order to reduce the emission of greenhouse gases (carbon dioxide) and reduce air pollutants, the development of clean energy has been encouraged. Additionally, the diverse energy plan helps to reduce dependence on diminishing fossil energy and provide a more reliable on-going energy supply.

Renewable energy, which is repeatable and occurs naturally, encompasses many different types of technology, such as solar energy, wind energy, hydro, tidal, and so on. Compared to conventional fossil fuel sources, major advantages with the use of renewable energy are the reduced impact of climate change with their environmentally friendly nature, sustainability of the energy sources and economic benefits. Due to rising fossil fuel prices and the falling costs of renewables, renewable energy has cemented its position as an indispensable part of the global energy mix, based on the report by the international energy agency in 2013 [3].

In March 2007, the EU endorsed an energy technology plan which sets a target that 20 % of energy must come from renewable sources by 2020 to increase the share of the renewable energy sectors [4]. Included in the plan, the UK has embarked upon a strategy aimed at providing 15 % of energy consumed via renewable sources and 20 % of electricity via renewable by 2020 [5].

1.2 The Role of Wind Energy

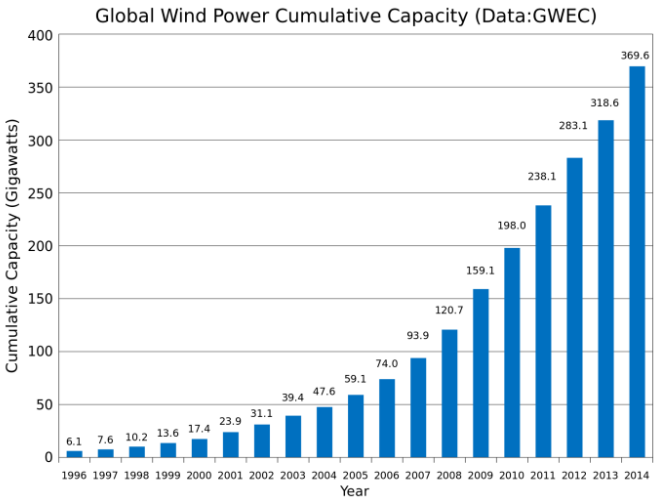


Fig.1.2: Worldwide growth of wind capacity [6]

Amongst all the renewable energy sources, the environmental benefits and cost-competitiveness of wind power have driven its rapid expansion in recent decades. As shown in Fig.1.2, worldwide installed capacity of wind power grew to 369 GW in 2014. Starting from a near zero share in 2004, China has followed an aggressive plan of wind power development and, by far, has led the world, installing 20.7 GW in 2014 to bring the total so far to 114.76 GW installed, and leading to 200 GW capacity by 2020 [7]. The United States is second with 65.8 GW wind energy capacity and their strategy plan aims at providing a 20 % share of the electricity via wind power by 2030 [8]. As reported by the Global Wind Energy Council (GWEC), wind power has expanded by almost 16 % in 2014 across the world to reach a new peak of 368.8 GW of total installed capacity [9]. Moreover, there is expected to be substantial growth in wind energy capacity around the world in the coming years.

1.3 Motivation

The predicted growth in UK wind deployment, particularly large-scale offshore wind farms, drives the industry and academia to search for cost effective network architectures that can facilitate large power harvesting offshore and transmit it to the onshore mainland AC grid. The offshore DC collection network is one of the promising possibilities being investigated at present, including development of DC/DC converter topologies to realise such a DC collection network, without overstressing these DC/DC converters and other network components. In the search for suitable DC/DC converters for offshore DC collection networks, this thesis will investigate a number of DC/DC converters that can be used offshore, including the necessary control architecture to facilitate their fault tolerant operation.

1.3.1 Offshore Wind Generation in the UK

Today, onshore wind farms have proven to be a commercially viable technology, and are widely used to reduce climate change effects and meet national renewable energy targets in Europe and around the world. However, in recent years there have been attempts to increase outputs of wind generation by exploiting offshore wind energy. The first reason that offshore wind energy is preferable to onshore is the low occupation of land space. Additionally, the higher wind speed and lower turbulence levels offshore contribute to a more stable and plentiful energy supply than the onshore solution. It is known that doubling the wind speed leads to an eightfold increase in the output power. This cubic relationship between power output and wind speed makes offshore wind energy highly attractive. In addition, without the noise and visual restrictions, larger wind turbines can be built to operate at higher rotor rotational speed which decreases the loading on the turbine as well.

The UK offshore wind industry has experienced a rapid growth since the ‘Round 1’ project started in 2000. There are 18 offshore wind farms involved in Round 1 with potential capacity of 1.5 GW, and now 13 projects are fully operational with a generating capacity of 1.2 GW. Round 2 projects provide 7 GW capacity and are now almost complete. The much larger Round 3 project can provide 32.2 GW potential capacity and all the projects involved are all in the pre-planning or planning

stages. The London Array, shown in Fig.1.3, is now the world's largest offshore wind farm located 20 km of the Kent coast in the UK. Within the European sector there is currently in excess of 8 GW of installed capacity with potential for 40 GW by 2020, of which 24 GW is allocated for the UK sector [10, 11]. Today, the UK has become the undisputed leader of offshore power with half of the world's installed capacity. With Round 1, 2, 3 and Scottish Territorial Waters projects, the cumulative offshore wind power installation is expected to reach 153 GW by 2030 worldwide and this trend will surely continue [6].

Fig.1.3: London array offshore wind farm [12]

1.3.2 Electrical System for Offshore Wind Farms

The ambitious plans for offshore energy require the creation of remote, high-capacity wind farms with ratings significantly in excess of 1 GW. Although, a lot of technical problems have been solved during the past decade to improve the reliability and reduce the cost of offshore wind energy, the electrical system is still one of the major research issues [13-15].

Fig.1.4, using data collected from two large surveys (LWK represents Landwirtschaftskammer dataset and WMEP represents wind turbine measurement and evaluation programmer) of European wind turbines over 13 years, summarises the failure rates for different turbine components and the corresponding downtime per failure. It can be seen from this figure that the electrical and control systems play a severe problematic role in terms of failure rate and downtime. Consequently, a high percentage of electricity production may be lost due to failure of the electrical aspect.

Furthermore, large offshore wind farms with higher power levels present a more severe challenge for the electrical networks that will provide interconnection of turbines and onward transmission to the onshore power network.

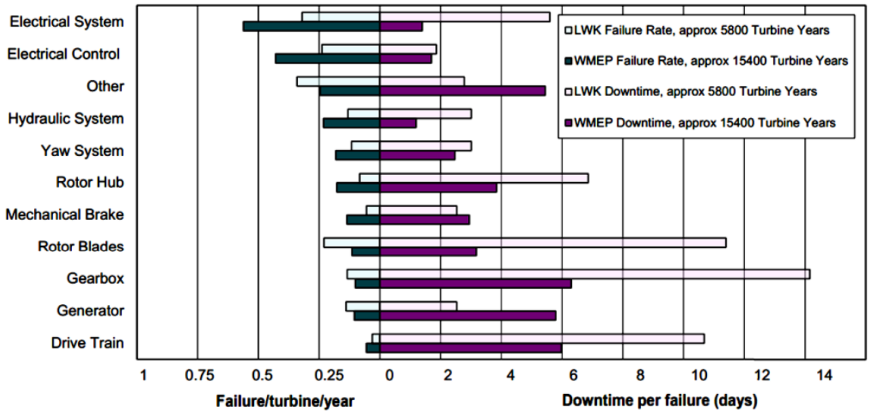


Fig.1.4: Failure rates and downtime survey [16]

The electrical system for offshore wind farm consists of two networks: a collection system and a transmission system. The collection network gathers the outputs from each individual wind turbine and brings them to a central collection point which is typically rated in the region of 30 kV. At the offshore converter substation, this voltage is increased using a transformer to high-voltage transmission level and eventually the generated power is brought onshore through this transmission system.

The traditional electrical system for offshore wind farms is a pure AC system, as shown in Fig.1.5, with a voltage step-up in two stages. Transformers at each wind turbine step up the generator voltage to medium-voltage, and at the medium-voltage AC (MVAC) collection network the voltage is stepped up to high-voltage AC (HVAC) transmission level.

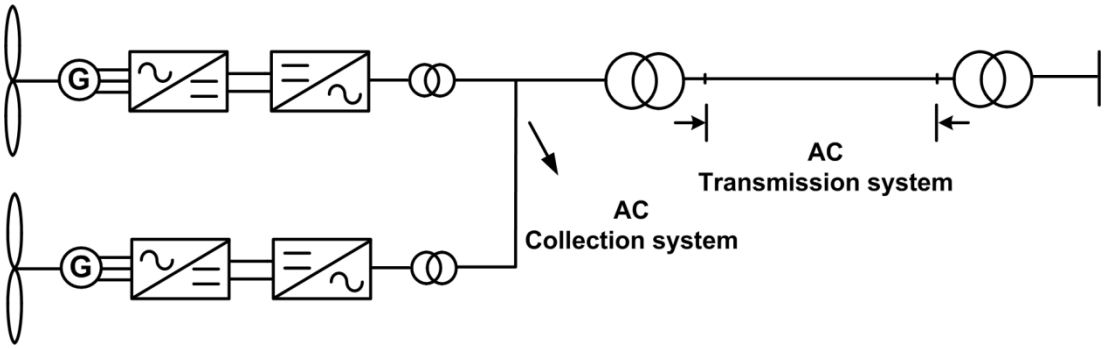


Fig.1.5: Pure AC electrical system for offshore wind farm

Recently, high-voltage DC (HVDC), recognised as a technically advantageous and cost-effective solution over long-distance cable transmission, is preferred over the AC solution for offshore transmission systems due to the dramatically increased reactive power production incurred in long AC transmission lines [17]. Therefore, a new type of AC/DC electrical system is proposed, as shown in Fig.1.6, where the MVAC output needs to be stepped up to high-voltage through a line-frequency transformer and then rectified by an AC/DC converter to conduct HVDC transmission system.

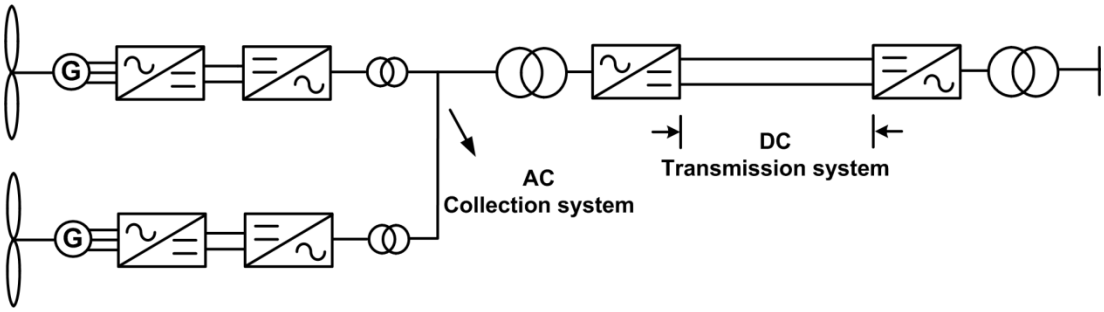


Fig.1.6: AC collector network and HVDC transmission link for offshore wind farm

Whilst the advanced HVDC transmission has addressed the issue of long-distance transmission, internal power networks for offshore wind farms have seen relatively little innovation. High wind farm capacity combined with a move to larger wind turbines will result in a large geographical footprint, requiring a substantial sub-sea power network to provide internal interconnection. Additionally, the larger wind turbines require large separation to decrease turbulent effects on adjacent turbines. Consequently, the internal power connections have an important impact on the annual produced power, the operation, and the footprint design of the wind farm.

Present solutions for collection networks are based around conventional MVAC architectures. However, the cascade of multiple AC/DC and DC/AC conversion stages can lead to a poor system efficiency. One of the promising options to address the internal power network is to use a pure DC system, as shown in Fig.1.7, where each individual wind turbine outputs DC from a fully rated wind turbine DC/DC converter. Afterwards, outputs of multiple wind turbines are collected and stepped up to HVDC transmission level through an offshore DC/DC converter. With such a configuration, the number of conversion stages is reduced, and better energy storage system integration can also be achieved [15, 18-23].

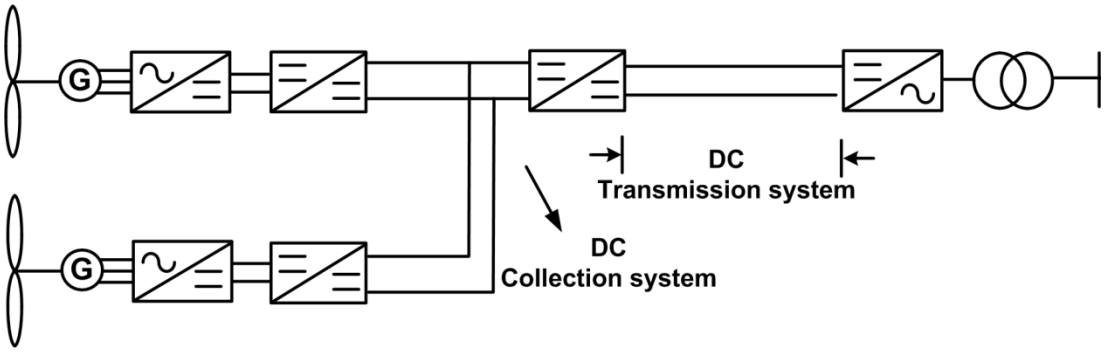


Fig.1.7: Pure DC electrical system for offshore wind farm

There are two ways to deliver DC collection grid within the wind farms: one utilising a diode rectifier for AC/DC rectifier and a DC/DC converter and the other employing an IGBT rectifier and a DC/DC converter. The DC/DC converter consists of an inverter, a coupling transformer and a rectifier-either passive or active. The rectifier based on the IGBTs are more expensive and lossy than rectifier based on diodes, however, it keeps the input voltage to the DC/DC converter constant, allowing easier control the MPPT of the variable-speed wind turbine.

1.3.3 MVDC Collection Network

Recent studies have highlighted the potential benefits of MVDC collection networks, which will become increasingly attractive given the growing offshore wind farm capacities [15, 18-23].

Since the effective power that can be transmitted through the AC cable is only 0.7 times the peak value, DC cable has 1.4 times higher power transport ability compared to AC cable with the same cable characteristic [24]. In addition, DC transmission does not suffer from reactive power losses which are present in AC systems. If the capacity of offshore wind farms increases as is projected, more cables are needed for the internal collection network. For example, the site area of the London Array project with 1000 MW total capacity is in excess of 200 km^2 and requires a 200 km MVAC array connection cable [12]. Therefore, the use of DC has better utilisation of the cable voltage rating and eliminates the charging current issue associated with AC cables.

With appropriate design, MVDC collection networks have the potential to reduce losses through better optimisation of conversion stages, and substantial research

effort has concluded that the power losses associated with MVDC are expected to be significantly lower compared to its AC equivalent [15, 25, 26]. A DC collection grid can also lower the life-cycle cost [19]. Additionally, higher dynamic control can be achieved over the power flow of the collection network compared to an AC system. In particular, it has been shown in many publications that the voltage and current during fault conditions are manageable [27].

A DC collection grid presents an opportunity to significantly reduce the size and weight of the required plant and power units [28]. Present offshore wind farms connect to conventional 50 or 60 Hz AC systems by employing line-frequency transformers to step up the generator output voltage to collection network voltage levels. However, the bulky, heavy and noisy line-frequency transformer imposes limitations on the power density of the system [29]. Advances in power electronic DC/DC conversion systems allow the replacement of line-frequency transformers by medium- or high-frequency technologies, leading to significant weight and size savings when interfacing turbine generators to the MVDC network [15, 30]. In addition, the DC/DC converter with a medium- or high-frequency transformer is considered as a developing trend in power conversion systems, as it avoids voltage and current waveform distortion caused by the core saturation of lower frequency transformers. For offshore wind farms, the greater the power produced per installed wind turbine, the more cost-effective the solution and consequently a higher power DC/DC converter for each turbine is needed [31]. As a result, there is growing interest both in industry and academia to investigate the technical and economic viability of MVDC collection networks for offshore application based around high-power DC/DC converters [15, 32-36].

1.3.4 DC/DC Converter for Collection Networks

Viability of MVDC collection networks requires efficient and reliable high-power DC/DC converters to step up the wind generator output voltage (e.g. 5 kV DC) to a level compatible with an efficient wide area network connection (e.g. 50 kV DC) and provide galvanic isolation. Although a DC network can offer improved power quality, a smaller size and the potential to reduce cost and losses compared to an AC grid, the advantages greatly depend on the efficiency of the DC/DC converters [37]. To meet

system requirements, megawatt (MW) DC/DC converters must operate at voltages and currents in excess of individual semiconductor device ratings, requiring complex circuit topologies that can achieve power sharing between multiple devices. In addition, galvanic isolation is required to meet the safety standards, therefore voltage stresses presented at the primary and secondary windings of the transformer must be fully controlled. Additionally, high switching frequency is necessary for high power density, and leads to the reduction in size and weight of the interfacing transformer.

Some of the existing high-efficiency step-up DC/DC converters face the challenge of transferring these technologies to the required network voltages, since both the input and output of the DC/DC converter must operate above the voltage capability of existing power semiconductors [38, 39]. To solve this issue, a range of circuit topologies have been proposed to deliver high-power, high- or medium-voltage DC/DC converters. One way is to connect the semiconductor devices in series and to operate in a conventional two-level manner [40, 41]. Some researchers have opted for a multilevel approach, e.g. diode-clamped converter, flying capacitor (FC) clamped converter, series connected H-bridge voltage source converter (SCHB VSC), bridge of bridge converter (BoBc), etc., due to its advantages of low *dv*/*dt*, low harmonic content and low distortion [42-44]. It is known that the modular multilevel converter (M2C) has been deemed as a feasible candidate for high-power medium-voltage conversion systems. An isolated bidirectional M2C-transformer-M2C configuration has been introduced [45, 46] that can be deployed to interconnect HVDC and MVDC networks of different or similar voltage levels. Parallel-series connection of low-power rated modules is another excellent solution for scalability of DC/DC converters for a high-power DC grid, with improved robustness, reliability and fault-tolerant ability due to its inherent modular feature [47-49].

1.4 Objectives

Considering the subject of ‘DC/DC converter for offshore DC collection network’, this thesis focuses on the study and implementation of the high-power medium-voltage DC/DC converters for an offshore DC collection network. In particular the following aspects are addressed in this thesis:

- Analyse and compare the properties and advantages of the DC collection network to the existing AC collection network.
- Analyse potential candidate topologies for a high-power medium-voltage DC/DC converter to achieve voltage matching with and galvanic isolation from the DC grid. Here, particular attention is paid to parallel-series modular techniques that are applicable to the offshore DC collection network.
- Propose three kinds of parallel-series modular DC/DC converters, with an emphasis on the necessary control architecture to facilitate power sharing and fault ride-through ability. Simulation and experimental performances of the converters and control techniques under different conditions are compared and discussed.

1.5 Thesis Organization

The 7 chapters in this thesis are organised as follows:

This chapter briefly introduces the background to this study and is dedicated to the advantages of the DC collection network and challenges of current high-power medium-voltage DC/DC converters. Chapter 2 reviews potential high-power DC/DC converters that can be employed in this application, and identifies the requirements for DC/DC converters that can realise such DC collection networks. In Chapter 3, earlier work relating to parallel-series modular DC/DC converters is described, followed by the introduction of the full-bridge and the dual-active bridge (DAB) DC/DC converters as the module topology of the proposed converter. Chapter 4 proposes the first DC/DC converter topology with input-parallel output-series (IPOS) connection of full-bridge modules and a novel control strategy based on a 'master-slave' scheme that provides power sharing and fault-tolerant ability. The proposed topology and control strategy has been applied to a system-level simulation and a scaled-down experimental system to validate its viability. Chapter 5 focuses on a novel configuration consisting of *n* isolated full-bridge modules, whose inputs are input-series-input-parallel (ISIP) connected, whilst the outputs are series connected. The power sharing issue, control topology and both simulation and experimental results for this new proposed converter are presented and the performance of this converter under different control schemes is compared and discussed in terms of

power distribution issues. Chapter 6 extends the input-series-input-parallel output-series (ISIPOS) configuration described in Chapter 5 to a DAB circuit, and a higher power rating rig aimed at 15 kW power is built to demonstrate a more realistic module for the proposed application. The rig design process, and experimental and simulation results with a multi-module ISIPOS connected DC/DC converter are presented. Finally, Chapter 7 presents the main conclusions, contributions and potential for future study of the technologies developed in this thesis. In addition, a number of appendices are attached that include details of the experimental rig, experimental DSP code and the author's publication information.

1.6 Chapter Reference

[1] "http://www.metoffice.gov.uk/climate-guide/science/temp-records."

[2] P. T. Gaynor, R. Y. Webb and C. C. Lloyd, "A Low Temperature Differential Stirling Engine for Power Generation," in 2008 IEEE International Conference on Sustainable Energy Technologies, pp. 492-495, 2008.

[3] I. E. Agency, "World Energy Outlook 2012," November 2012, 2012.

[4] Renewable_Energy_Technology_Roadmap 20% by 2020, European Renewable Energy Council (EREC), Brussels.

[5] UK Renewable Energy Roadmap Update 2012, Department of Energy & Climate Change, 2012.

[6] G. W. E. Council, Global Wind Energy Outlook 2014, 2014.

[7] R. S. Semken, M. Polikarpova, Ro, x, ytta, P., J. Alexandrova, Pyrho, J. nen, J. Nerg, A. Mikkola and J. Backman, "Direct-drive permanent magnet generators for high-power wind turbines: benefits and limiting factors," Renewable Power Generation, IET, vol. 6, no. 1, pp. 1-8, 2012.

[8] M. Robinson, Veers, P., Butterfield, S., Greene, J., Thresher, W.M.R., U. DOE, 20% wind energy by 2030: increasing wind energy's contribution to U.S. electricity supply, National Renewable Energy Laboratory (NREL), US. DOE, 2008.

[9] Global Wind Statistics 2012, Global Wind Energy Council (GWEC), Brussels, Belgium, 2013.

[10] E. W. E. Association. "The European offshore wind industry - key trends and statistics 1st half 2015," http://www.ewea.org/statistics/offshore/, Online available.

[11] E. W. E. Association. "Offshore wind policy issues," http://www.ewea.org/policy-issues/offshore/, Online available.

[12] http://www.londonarray.com/.

[13] Y. Zhou, D. E. Macpherson, W. Blewitt and D. Jovcic, "Comparison of DC-DC converter topologies for offshore wind-farm application," in Power Electronics, Machines and Drives (PEMD 2012), 6th IET International Conference on, Bristol, pp. 1-6, 2012.

[14] L. Max, T. Thiringer and O. Carlson, “Control of a wind farm with an internal direct current collection grid,” Wind Energy, vol. 15, no. 4, pp. 547-561, 2012.
[15] L. Yiqing and S. J. Finney, “DC collection networks for offshore generation,” in Renewable Power Generation Conference (RPG 2013), 2nd IET, Beijing, pp. 1-4, 2013.
[16] P. Tchakoua, R. Wamkeue, M. Ouhrouche, F. Slaoui-Hasnaoui, T. Tameghe and G. Ekemb, “Wind Turbine Condition Monitoring: State-of-the-Art Review, New Trends, and Future Challenges,” Energies, vol. 7, no. 4, pp. 2595, 2014.
[17] S. B. Jiuping Pan, Magnus Callavik, Peter Sandeberg, “DC Connection of Offshore Wind Power Plants without Platform,” in 13th Wind Integration Workshop, Berlin, 2014.
[18] F. Deng and C. Zhe, “Operation and Control of a DC-Grid Offshore Wind Farm Under DC Transmission System Faults,” Power Delivery, IEEE Transactions on, vol. 28, no. 3, pp. 1356-1363, 2013.
[19] M. Stieneker, J. Riedel, N. Soltau, H. Stagge and R. W. De Doncker, “Design of series-connected dual-active bridges for integration of wind park cluster into MVDC grids,” in Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on, Lappeenranta, pp. 1-10, 2014.
[20] S. P. Engel, N. Soltau, H. Stagge and R. W. De Doncker, “Dynamic and Balanced Control of Three-Phase High-Power Dual-Active Bridge DC-DC Converters in DC-Grid Applications,” Power Electronics, IEEE Transactions on, vol. 28, no. 4, pp. 1880-1889, 2013.
[21] C. Meyer, M. Hoing, A. Peterson and R. W. De Doncker, “Control and Design of DC Grids for Offshore Wind Farms,” Industry Applications, IEEE Transactions on, vol. 43, no. 6, pp. 1475-1482, 2007.
[22] J. Robinson, D. Jovcic and G. Joos, “Analysis and Design of an Offshore Wind Farm Using a MV DC Grid,” Power Delivery, IEEE Transactions on, vol. 25, no. 4, pp. 2164-2173, 2010.
[23] P. Bresesti, W. L. Kling, R. L. Hendriks and R. Vailati, “HVDC Connection of Offshore Wind Farms to the Transmission System,” Energy Conversion, IEEE Transactions on, vol. 22, no. 1, pp. 37-43, 2007.
[24] S. Kenzelmann, “Modular DC/DC Converter for DC Distribution and Collection Networks,” Ecole Polytechnique Federale De Lausanne, Suisse, 2012.
[25] L. Max, “Design and Control of a DC Collection Grid for a Wind Farm,” Department of Energy and Environment, Chalmers University of Technology, Sweden, 2009.
[26] N. R. Chaudhuri and A. Yazdani, “An aggregation scheme for offshore wind farms with VSC-based HVDC collection system,” in Power and Energy Society General Meeting, 2011 IEEE, pp. 1-8, 2011.
[27] G. Ortiz, J. Biela, D. Bortis and J. W. Kolar, “1 Megawatt, 20 kHz, isolated, bidirectional 12kV to 1.2kV DC-DC converter for renewable energy applications,” in Power Electronics Conference (IPEC), 2010 International, pp. 3212-3219, 2010.
[28] D. M. Valcan, P. C. Kjar, L. Helle, S. Sahukari, M. Haj-Maharsi and S. Singh, “Cost of energy assessment methodology for offshore AC and DC wind

power plants," in Optimization of Electrical and Electronic Equipment (OPTIM), 2012 13th International Conference on, Brasov, pp. 919-928, 2012.
[29] Z. Biao, S. Qiang, L. Wenhua and S. Yandong, "Overview of Dual-Active-Bridge Isolated Bidirectional DC&DC Converter for High-Frequency-Link Power-Conversion System," Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4091-4106, 2014.
[30] P. Monjean, J. Delanoe, D. Marin, J. Auguste, C. Saudemont and B. Robyns, "Control strategies of DC-based offshore wind farm," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1-9, 2011.
[31] E. Veilleux and P. W. Lehn, "Interconnection of Direct-Drive Wind Turbines Using a Series-Connected DC Grid," Sustainable Energy, IEEE Transactions on, vol. 5, no. 1, pp. 139-147, 2014.
[32] Y. Jin, J. E. Fletcher and J. O'Reilly, "Multiterminal DC Wind Farm Collection Grid Internal Fault Analysis and Protection Design," Power Delivery, IEEE Transactions on, vol. 25, no. 4, pp. 2308-2318, 2010.
[33] W. Chen, A. Q. Huang, C. Li, G. Wang and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," Power Electronics, IEEE Transactions on, vol. 28, no. 4, pp. 2014-2023, 2013.
[34] Y. Jin, J. E. Fletcher and J. O'Reilly, "Multi-terminal DC wind farm collection and transmission system internal fault analysis," in Industrial Electronics (ISIE), 2010 IEEE International Symposium on, pp. 2437-2442, 2010.
[35] A. B. Morton, S. Cowdroy, J. R. A. Hill, M. Halliday and G. D. Nicholson, "AC or DC? economics of grid connection design for offshore wind farms," in AC and DC Power Transmission, 2006. ACDC 2006. The 8th IEE International Conference on, pp. 236-240, 2006.
[36] D. Fujin and C. Zhe, "An offshore wind farm with DC grid connection and its performance under power system transients," in Power and Energy Society General Meeting, 2011 IEEE, pp. 1-8, 2011.
[37] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge and R. W. De Doncker, "Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids," Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 124-137, 2015.
[38] C. Wu, A. Huang, S. Lukic, J. Svensson, L. Jun and W. Zhenyuan, "A comparison of medium voltage high power DC/DC converters with high step-up conversion ratio for offshore wind energy systems," in Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, Phoenix, AZ, pp. 584-589, 2011.
[39] Y. Lian, G. P. Adam, D. Holliday and S. J. Finney, "Active power sharing in input-series-input-parallel output-series connected DC/DC converters," in Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE, Charlotte, NC, pp. 2790-2797, 2015.
[40] M. P. N. van Wesenbeeck, J. B. Klaasens, U. von Stockhausen, A. Munoz de Morales Anciola and S. S. Valtchev, "A multiple-switch high-voltage DC-DC

converter," Industrial Electronics, IEEE Transactions on, vol. 44, no. 6, pp. 780-787, 1997.

[41] K. Vechalapu, A. K. Kadavelugu and S. Bhattacharya, "High voltage dual active bridge with series connected high voltage silicon carbide (SiC) devices," in Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, Pittsburgh, PA, pp. 2057-2064, 2014.

[42] N. Soltau, H. Stagge, R. W. De Doncker and O. Apeldoorn, "Development and demonstration of a medium-voltage high-power DC-DC converter for DC distribution systems," in Power Electronics for Distributed Generation Systems (PEDG), 2014 IEEE 5th International Symposium on, pp. 1-8, 2014.

[43] R. W. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," Industry Applications, IEEE Transactions on, vol. 27, no. 1, pp. 63-73, 1991.

[44] S. Inoue and H. Akagi, "A Bidirectional Isolated DC/DC Converter as a Core Circuit of the Next-Generation Medium-Voltage Power Conversion System," Power Electronics, IEEE Transactions on, vol. 22, no. 2, pp. 535-542, 2007.

[45] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F. Canales and Y. R. De Novaes, "A versatile DC-DC converter for energy collection and distribution using the Modular Multilevel Converter," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1-10, 2011.

[46] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales and Y. R. De Novaes, "Isolated DC/DC Structure Based on Modular Multilevel Converter," Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 89-98, 2015.

[47] A. Mohammadpour, L. Parsa, M. H. Todorovic, L. Rixin and R. Datta, "Interleaved multi-phase ZCS isolated DC-DC converter for sub-sea power distribution," in Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE, pp. 924-929, 2013.

[48] A. Mohammadpour, L. Parsa, M. Harfman Todorovic, R. Lai, R. Datta and L. Garces, "Series-Input Parallel-Output Modular-Phase DC-DC Converter with Soft Switching and High Frequency Isolation," Power Electronics, IEEE Transactions on, vol. PP, no. 99, pp. 1-1, 2015.

[49] J. Ji, C. Qianhong, M. Yundong and G. Chunying, "Non-grid-connected wind power system and its high power DC-DC converter," in World Non-Grid-Connected Wind Power and Energy Conference, 2009. WNWEC 2009, pp. 1-5, 2009.

Chapter 2: High Power DC/DC Converter

The high-power DC/DC converter is perceived as one of the key-enabling components of the offshore DC collection network and it is vital that it is designed for high reliability and efficiency. This chapter reviews several DC/DC converter topologies, which are considered as potential candidates for high-power applications, with emphasis on DC collection networks for large-scale offshore wind farms. The first part of this review considers solutions that connect the power devices in series in order to make conventional two-level topologies applicable to high-power systems. This category also includes multilevel topologies that use series-connected semiconductor switches along with several active or passive DC voltage sources to synthesise a two-level output voltage with staircase voltage transitions to reduce *dv*/*dt* and AC harmonics in the AC voltage that will be presented to the isolation transformers of the DC/DC converter, and to improve efficiency and power density. Presently, modular type converters are popular due to their inherent redundancies, which are critical for continued operation under active or passive devices failures. In this chapter, the main features of these converters are discussed, with basic analysis of their fundamental operational principles. Following that, the requirements of DC/DC converters to be applied to the offshore collection network are outlined.

2.1 Review on High-Power DC/DC Converter

Nowadays, power electronic system integration is an important trend in the power industry [1]. In offshore wind farm collection networks, the numerous advantages of power electronics and DC cables outweigh those of the conventional AC counterpart, for example full control over energy flow, improved power quality, and potentially lower cost can be achieved [2]. Additionally, transformers in DC/DC converters are operated at elevated frequency, allowing dramatic weight and size savings as compared to systems using 50 or 60 Hz transformers, leading to higher power density as well as lower loading on the wind turbine [3].

MVDC system is a feasible solution for offshore wind collection grid. However, realising the benefits of MVDC will require the use of high-power DC/DC converters with the capability of operating at the required network voltages, e.g. a 5 MW rated wind turbine with 5 kV DC link voltage, stepped up to a level (e.g. 50 kV DC) compatible with an efficient wide area network connection. The development of HVDC transmission and DC collection grids for renewable energies spurs the need for DC/DC converters at megawatt levels for voltage matching and galvanic isolation of the DC grid. Over the past few decades, great efforts have been made to develop high-power medium-voltage DC/DC converters that are capable of processing energy effectively due to the following reasons:

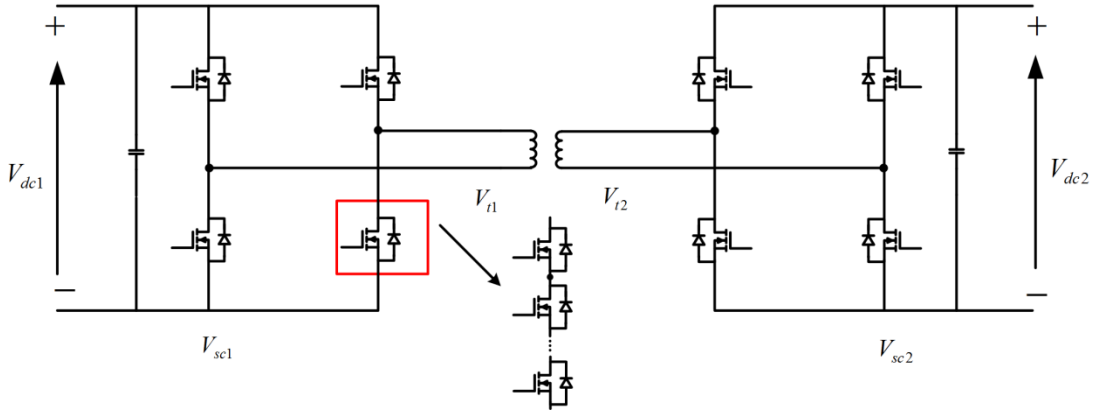
- Most of the widely-used converters encountered in low-power applications cannot be applied directly in high-power application.
- The choice of a single semiconductor switching device that can withstand high DC voltage stresses is limited. Currently, the voltage rating of a single IGBT is limited at 6.5 kV with a maximum nominal current of 750 A, and the cost is very high. Therefore, the operating voltage level in many studies challenges most of the existing technologies since both the input and output of the DC/DC converter must operate above the voltage capability of existing power semiconductors.
- In most high-power applications, galvanic isolation is mandatory to meet safety standards, especially at high conversion ratios as the isolation transformer can limit the circulating power and the resulting losses. Therefore, only DC/DC converters with isolation transformer are considered in this study.

- High switching frequency is necessary for high power density as it leads to the reduction in size and weight of the interfacing transformer. However, the switching frequency is limited by the level of the switching losses and by electromagnetic interference (due to high *di*/*dt* and *dv*/*dt*). Attention must be paid to the trade-off between switching frequency and power losses.
- Most DC/DC conversion presents major challenges due to the combination of high-power, medium-voltage and medium-frequency.

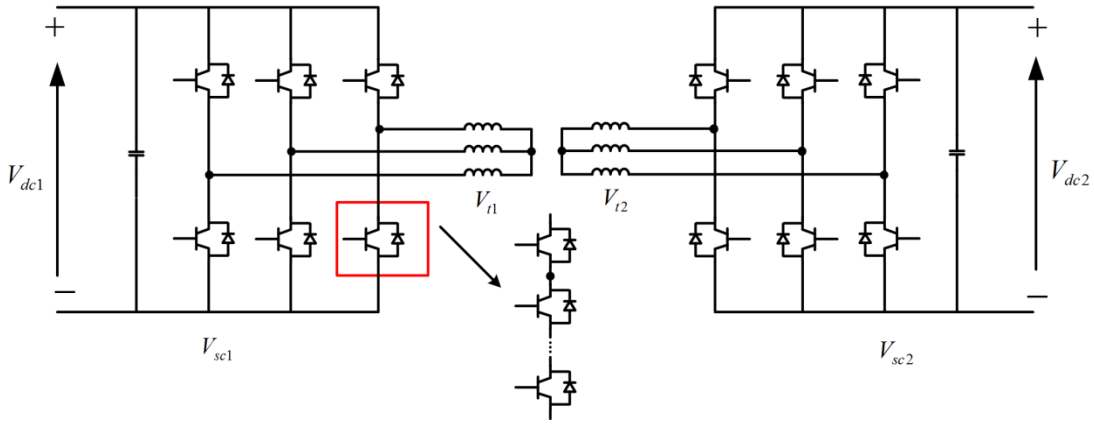
Since the currently available devices cannot withstand such high voltage stresses, there are three possible ways to deliver high-power medium-voltage DC/DC converters. Direct series connection of power switching devices is an effective way of approaching high-voltage and high-power conversion with well-known two-level circuit structures. The second way is to use a multilevel converter to address high power with low-rating devices. In addition, series connection can be integrated into the multilevel methodology to further expand the operating level and enhance system performance. The third solution is to change the converter topology to a modular one, which has a number of smaller modules and where each module only contributes a small fraction of overall converter power. All approaches will be reviewed and discussed in the following sections, with particular attention to the context of high-power application.

2.1.1 Converter with Series Connected Devices

In order to overcome device limitations, realisation of high-power semiconductor switches by connecting devices in series has been utilised in medium- and high-voltage applications [4]. As a result of series connection techniques, higher operating voltage can be reached, and at the same time low-voltage rating devices with higher performance can be used to obtain better switching performance in the series connected configuration [5, 6].



(a)



(b)

Fig.2.1: Two-level dual active bridge converter topology (a) single phase with MOSFET devices and (b) three-phase with IGBT devices

In 1980s, series connection of gate turn-off (GTO) thyristors was proposed. Since the 1990s, series connection of integrated gate commutated thyristors (IGCTs) and insulated gate bipolar transistors (IGBTs) has evolved into mature techniques used in medium- or high-voltage systems [7-9]. Fig.2.1 shows the MOSFET and IGBT based two-level DC/DC converter in single-phase and three-phase configurations respectively. This circuit can operate in a soft-switched manner where the semiconductor devices tend to turn on and off under conditions of zero current and zero voltage, thus making it possible to achieve lower switching losses and an increase in switching frequency [10]. The switching device consists of several series-connected switching devices as shown in the figure to enable operation at high voltage levels, and a medium- or high-frequency transformer is employed to provide isolation and voltage matching [11]. The inverter side converts the DC voltage into

an AC signal, and the frequency of the square waveform at the transformer is significantly higher than 50 Hz (with frequency ranging from 250 Hz to 1 kHz), which leads to a reduced transformer size. The stepped-up or stepped-down voltage after the transformer is then rectified at the output.

The topology with series-connected devices inherits the benefits of well-known circuit structures, control methods and dynamic response. However, one problem of series connection is the unequal voltage distribution between the semiconductor devices under steady-state and transient conditions due to gate drive delays, physical differences in the structure of the devices and snubber circuitry [12, 13]. It is essential to connect series-connected switching devices in a reliable manner. However, the induced uneven distribution of voltage across the series-connected power switches could result in overvoltage of individual device and failure of the entire series string of devices. Special attention also should be paid to the issue of instant voltage balancing during start-up and turn-off transience, otherwise the switch that switches off first (or switches on last) needs to sustain the whole voltage.

For safe operation, various active balancing methods have been proposed to equalise static and dynamic voltage balancing. Passive control methods, termed as load side control, involve snubber circuitry, with or without auxiliary circuits [4]. Most of the snubber circuits minimise voltage unbalance by limiting the device voltage rise rate, but suffer from incurred power losses [8, 14, 15]. As an effective method for suppressing overvoltage and balancing the voltage across series-connected IGBTs, active clamping techniques have been widely applied [15, 16]. However, during conduction by the active clamping circuit, the IGBTs operate in the active region, which results in high switching loss, particularly in high-voltage converter applications [17]. The use of active gate control topologies, in which the gate charge is controlled to increase or decrease the rate of change of collector-emitter voltage has been reported [18, 19]. Although there may be a small increase in switching losses since the active gate control must operate at the speed of the slowest device, the feedback control that requires high-speed devices and added components degrades the reliability of the control method. The complicated control also restricts the switching speed. Additionally, perfect balancing is hard to accomplish during the switching transients. Once all the switches are commutated at the same time, high

dv/dt stress will be generated which may induce tremendous electromagnetic interference (EMI) problems, and may cause insulation failure and restrict the maximum voltage level that can be achieved. Due to this, the voltage level of the previous voltage source converter (VSC) with series connection technology, namely 'HVDC Light' developed by ABB, is limited to ±200 kV [20, 21]. Moreover, the achievable frequency for this topology is also impeded by the central transformer, as the high frequency is not viable for a high power level transformer [22].

It can be seen that conventional two-level voltage source converters with series connection of devices suffers from certain significant disadvantages, such as high *dv*/*dt* stresses on devices and low achievable switching frequency leading to high current ripple or large volume passive component [23, 24]. In addition, series connection of devices leads to additional snubber components. To overcome such issues, series-connected devices are applied in a multilevel topology to allow operating at high voltage level. The primary aim of the multilevel topology is to generate an output voltage which is much higher than the voltage rating of the individual switching devices, to meet the requirements of medium- and high-voltage applications. This multilevel concept has become increasingly attractive to industry and academia in recent years due to its ability to synthesise waveforms with better harmonic performance and lower *dv*/*dt* stresses. The next section will introduce several types of multilevel converter.

2.1.2 Multilevel Converter

The multilevel converter concept was firstly introduced in 1975 [25], and several multilevel converter topologies have subsequently been proposed for high-power and high-voltage applications. The principle of the multilevel converter is to use a series of semiconductor switches and several DC voltage sources to generate a staircase voltage waveform. The multilevel converter can outperform the conventional two-level converter in high-voltage power conversion due to the following advantages [26-29]:

- Low harmonic distortion at the converter output and low electromagnetic compatibility (EMC) that contributes to the reduction in both AC side filter requirements and the likelihood of insulation breakdown.

- Low *dv*/*dt* stress on the insulation of the AC loads.
- Low distortion input current.
- For sinusoidal AC fundamental, multilevel converters can operate at a lower switching frequency compared to that of a conventional two-level converter, leading to lower switching loss and higher efficiency.
- Multilevel converters can provide ride-through capability under emergency conditions if batteries or capacitors were used as DC sources.

However, their main disadvantages are that these features are achieved at greater complexity of the power circuit and control. The following section reviews three major multilevel inverter topologies with their fundamental multilevel structures, and advantages and disadvantages of each topology.

A. Conventional Cascaded H-Bridge

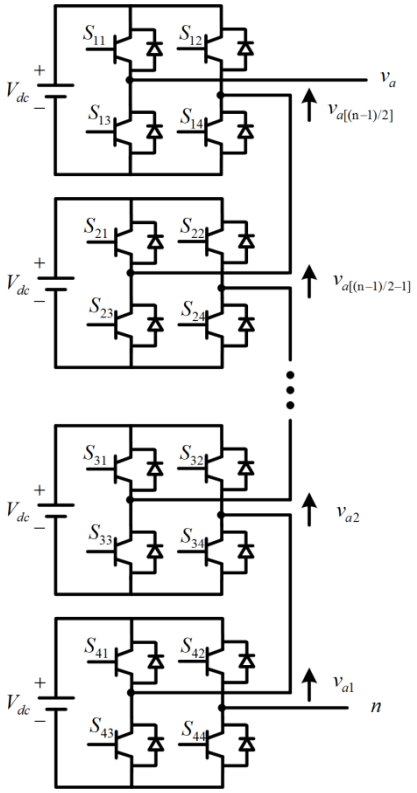


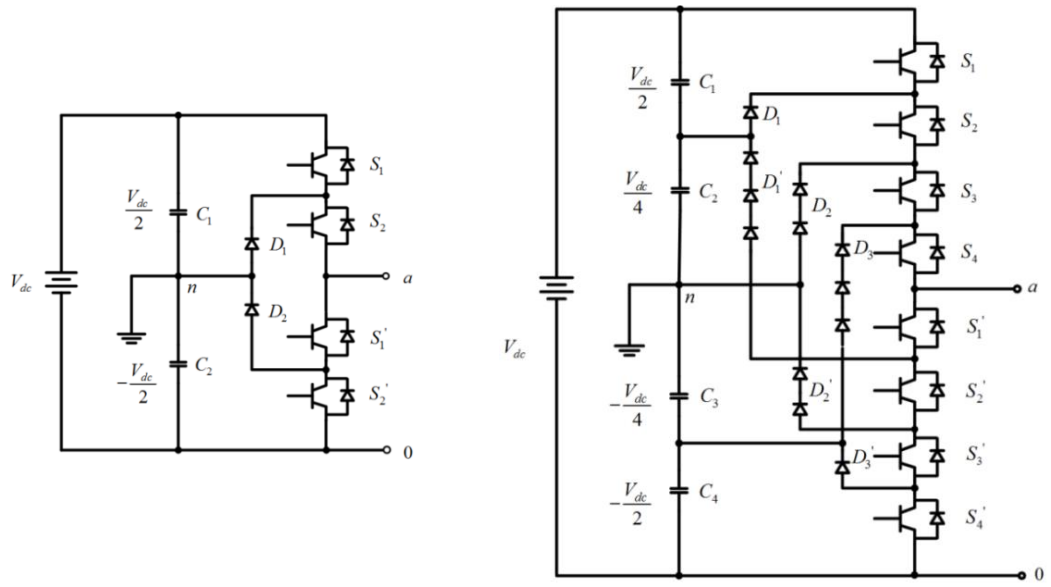
Fig.2.2: Single phase cascaded H-bridge multilevel inverter topology

The cascaded H-bridge (CHB) multilevel inverter was first introduced in 1975, and is based on series-connected H-bridge cells with independent DC sources to produce a

sinusoidal voltage output. It has gained more attention since the 1990s and has been generally applied to static synchronous compensator (STATCOM) and medium-voltage drives applications [30].

Fig.2.2 shows the power circuit for a single phase leg of an *n*-level inverter with full-bridge cells. The resulting phase voltage is synthesised by the addition of the voltages generated by the different cells. The cascaded multilevel converter is suited to applications where no real power is transferred from the cell capacitors to the AC output. The absence of the common DC link limits its application for DC/DC conversion, as the provision of real power calls for the cell capacitors to be replaced with isolated DC sources [31, 32].

B. Diode-Clamped Multilevel Inverter



(a) (b)

Fig.2.3: Diode-clamped multilevel inverter topologies (a) single phase three-level and (b) single phase five-level

The first diode-clamped multilevel topology was proposed in 1981 [33]. It was a three-level diode-clamped converter, also known as neutral-point clamped (NPC), in which the clamping diodes are used to clamp the DC bus voltage so as to achieve steps in the output voltage. Since the introduction of NPC, it has been widely used in different types of industrial applications, including interfacing for wind generators.

Single phase three-level and five-level diode-clamped multilevel converters are shown in Fig.2.3 (a) and (b) respectively. The three-level inverter consists of four switches (S_1, S_2, S_1' and S_2') with their freewheeling diodes, two series-connected bulky capacitor (C_1 and C_2) with their mid-point n as the neutral point to generate an additional voltage level, and two diodes (D_1 and D_1') to clamp the switch voltage to half the level of the DC bus voltage. With the ground reference, the three possible voltage outputs V_{an} are $½V_{dc}$, $-½V_{dc}$ and 0 with the switching scheme shown in Table 2.1, where '1' represents the ON state and '0' represents the OFF state. In each switching state, D_1 and D_2 are utilised to clamp the voltage stress to $½V_{DC}$ on each switch that is turned off.

Table 2.1: Switching scheme for three-level NPC

S_1	S_2	S_1'	S_2'	V_{an}
1	1	0	0	$½V_{dc}$
0	1	1	0	0
0	0	1	1	$-½V_{dc}$

Similarly, the five-level diode-clamped inverter has five voltage levels V_{an}: $½V_{dc}$ with all upper switches turned on, $-½V_{dc}$ with all lower switches turned on, $¼V_{dc}$ with S_2, S_3, S_4 and S_1' turned on, $-¼V_{dc}$ with S_4, S_1', S_2' and S_3' turned on, and 0 voltage with S_3, S_4, S_1' and S_2' turned on.

It can be concluded that an n-level diode-clamped multilevel converter needs (n-1) capacitors connected in series across the DC bus, 2×(n-1) switching devices and (n-1)×(n-2) clamped diodes to produce an n-level output voltage. With diode-clamped multilevel technology, each device voltage stress will be limited to one capacitor voltage level V_{dc}/n through the clamping diode. As the number of voltage levels increases, the output voltage waveform becomes closer to a sinusoidal waveform, with improved harmonic performance [34].

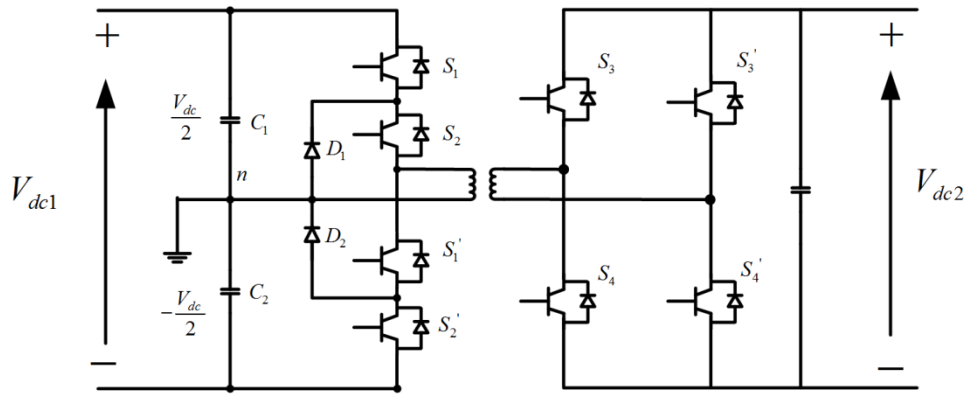
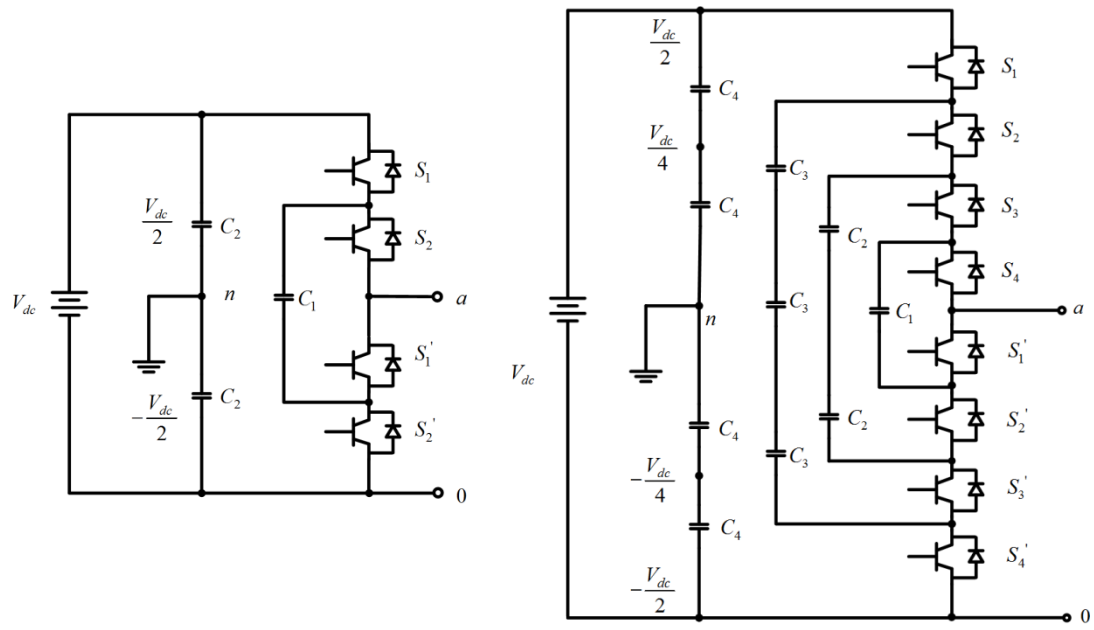


Fig.2.4: NPC based DC/DC converter

A high-power DC/DC converter, shown in Fig.2.4, comprises an NPC on the MV side and a full-bridge on the LV side [35]. Also, a new DC/DC multi-output boost converter is proposed for high-power application [36], where the variable output voltage is boosted and regulated by a diode-clamped converter. However, in both cases some additional clamping diodes are required, which limits their practical use in high-power applications. Moreover, the voltage stresses across the diodes are non-uniform, which further complicates the design. Another major problem associated with the converter is the unbalancing of the DC-link capacitor voltages when the number of voltage levels exceeds three, requiring external circuitry and balancing methods to balance the DC link capacitor voltages [37]. The use of the controlled DC voltage sources will also introduce extra complexity as well as cost penalties. Additionally, the reverse recovery of the clamping diodes challenges its utilisation in high-power application [37, 38].

C. Flying-Capacitor Multilevel Inverter

The flying-capacitor (FC) multilevel converter was introduced in 1992 [39]. After its introduction, both industry and academia have shown great interest in it. Fig.2.5 (a) and (b) illustrate single phase capacitor clamped multilevel inverter for three-level and five-level operation respectively, where the structure is similar to that of the diode-clamped converter except that instead of using clamping diodes, the inverter uses capacitors in their place.



(a) (b)

Fig.2.5: Flying-capacitor multilevel inverter topologies (a) single phase three-level and (b) single phase five-level

The three-level FC inverter shown in Fig.2.5 (a) consists of one flying capacitor C_1, two DC bus capacitor C_2, and four switches (S_1, S_2, S_1' and S_2'). The switching schemes are listed in Table 2.2 that can synthesise three output voltage levels: $V_{dc}/2$, $-V_{dc}/2$ and 0 with the corresponding states of the flying capacitor for a positive half-cycle only. The switches are operated in such a way to regulate the flying capacitor voltage to $V_{dc}/2$. Similar to the NPC converter, the voltage stress on each switching device is equivalent to the voltage rating of each capacitor, which is $V_{dc}/2$ in this case. Moreover, more levels at the converter output can be achieved by adding or subtracting the flying capacitor voltage from the DC link voltage.

Voltage output V_{an} in five-level FC converter shown in Fig.2.5 (b) can be synthesised by five levels: $½V_{dc}$ with all upper switches turned on, $-½V_{dc}$ with all lower switches turned on, $¼V_{dc}$ with three possible combinations, $-¼V_{dc}$ with three possible combinations and 0 voltage with six possible combinations. With proper switching scheme, the capacitor charge states can be balanced. Therefore, it can be concluded that the n-level FC converter requires (n-1) DC bus capacitors as well as (n-1)×(n-2)/2 clamped flying capacitors and (n-1) pairs of power semiconductor devices.

Table 2.2: Switching scheme for three-level FC inverter

S_1	S_2	S_1'	S_2'	V_{an}	C_1
1	1	0	0	$½V_{dc}$	No change
1	0	1	0	0	Charging
0	1	0	1	0	Discharging
0	0	1	1	$-½V_{dc}$	No change

Compared to the NPC converter, the FC clamping converter has redundant switching combinations for voltage synthesis which provide more flexibility in controlling the output voltage. Therefore, unlike the NPC converter, it does not suffer from the problem of DC link capacitor voltage imbalance. More importantly, the redundant switching schemes can easily control the charge states of the flying capacitors, making it a very competitive candidate for high-voltage conversion. Furthermore, the FC clamping converter does not suffer from the diode reverse recovery problem, and the structure is simpler [37, 38].

An isolated ZVS PWM DC/DC converter based on the flying capacitor cell is proposed for 600 V input voltage application, where the voltages across the switches are lower than the input voltage [40]. Another isolated flying-capacitor DC/DC converter is proposed, where the full-bridge converter and three-level flying capacitor circuit are integrated for a high step-down and high-power DC-based system [41]. Besides the difficulty of balancing voltage in real power conversion, the capacitor clamping converter requires an excessive number of bulky and costly capacitors to clamp the voltage which limits its implementation for high-voltage operation. Capacitor pre-charging and start-up processes are more complex as the number of levels increases [42].

Besides the three common multilevel converter topologies previously discussed, several generalised or emerging multilevel converter topologies have been proposed, such as the mixed-level hybrid multilevel converter, the asymmetric hybrid multilevel converter, and the soft-switched multilevel converter, which are theoretical hybrid circuits that are combinations of the common multilevel topologies or slight variations to them [26]. Although the total harmonic distortion of multilevel

converters is lower when compared to that of the two-level converter with series connected devices, one particular disadvantage is the large quantity of diodes or flying capacitors required, causing the overall system to be more complex and expensive [43]. The multilevel converter also suffers from a voltage balancing problem due to capacitors which act as DC voltage sources. In addition, for converters having greater than three-levels, system reliability is degraded due to the large quantity of diodes or flying capacitors [2], and reliability is one of the most important concerns for converters in offshore wind applications due to the lack of turbine access at sea [44].

Considering the aforementioned issues associated with multilevel converters, the tendency is towards modular converters, where a single high-power converter is replaced with a set of low-power rating converter modules and each module only needs to contribute small fraction of overall converter power, to overcome the limitations imposed by semiconductor voltage ratings and to provide redundancy. Two types of modular converter are described in the following section.

2.1.3 Modular Multilevel Converter

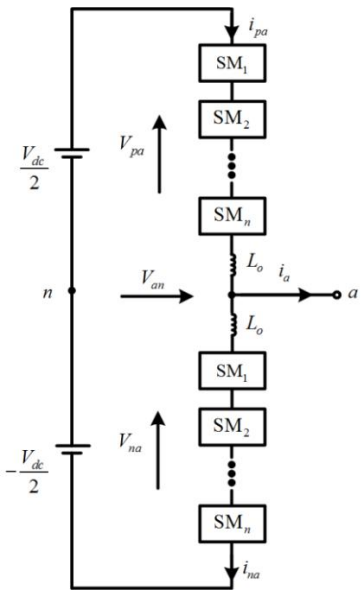


Fig.2.6: Single phase M2C converter topology

In 2002, Marquardt and Lesnicar firstly proposed the modular multilevel converter (M2C) [45]. Since then, the M2C has had an increasingly essential role in medium- and high-voltage power conversion systems due to its inherent advantages, such as

modularity, multilevel waveform with low harmonic distortion, low voltage stresses on each switching device as the voltage level increases, high efficiency with relatively low switching frequency, safe operation following device failures and low investment cost [46]. In particular, voltage source converter (VSC) HVDC has become increasingly popular and, as a result, this emerging M2C topology is of growing interest as a very suitable converter candidate for HVDC grids.

A single-phase M2C structure is shown in Fig.2.6. The converter has one upper arm and one lower arm, where each arm contains *n* basic sub-module (SM) blocks (*n* is chosen according to operational requirements), V_{dc} is the DC-link voltage, i_a is the AC output current, two arm inductors used to limit circulating current due to voltage imbalance between the upper and lower converter arms and to limit fault current during DC faults, V_{pa} and V_{na} are termed as the voltages generated by all the SMs in the upper and lower arms, and i_{pa} and i_{na} are the currents in the upper and lower arm respectively.

There are three main SM topologies: the half-bridge SM (HB-SM) shown in Fig.2.7 (a), the full-bridge SM (FB-SM) shown in Fig.2.7 (b), and the clamp double half-bridge SM (CD-SM) shown in Fig.2.7 (c).

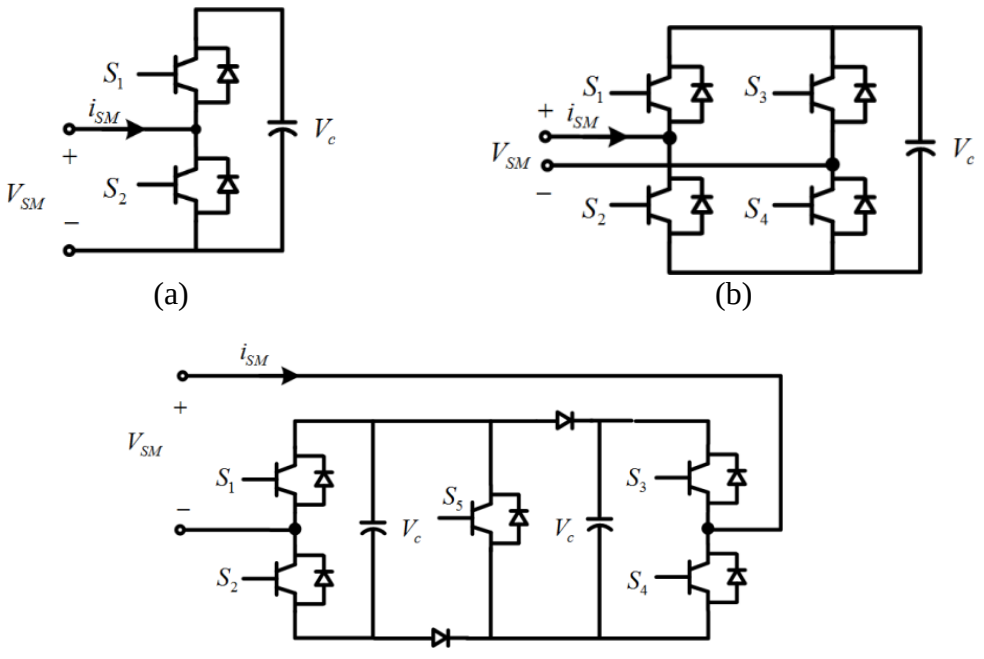


Fig.2.7: Module topologies (a) HB-SM (b) FB-SM and (c) CD-SM

Table 2.3: Switching scheme for a half-bridge SM

S_1	S_2	V_{SM}	V_c (i_{SM}>0)
1	0	V_c	Charging
0	1	0	No change

In Fig.2.7 (a), each sub-module is a half-bridge connected to a capacitor, which can be individually switched on and off. With the switching scheme illustrated in Table 2.3 where '1' represents the ON state and '0' represents the OFF state, each HB-SM can generate two voltage states, V_c and 0, across its output terminals. The most commonly used type of VSC for MVDC and HVDC today is the M2C with HB-SM, which can generate lower power losses compared with other M2C variants due to the reduced number of conducting devices.

Table 2.4: Switching scheme for a full-bridge SM

S_1	S_2	S_3	S_4	V_{SM}	V_c
1	0	0	1	V_c	Charging
0	1	0	1	0	No change
1	0	1	0	0	No change
0	1	1	0	$-V_c$	Discharging
0	0	0	0	-	-

The M2C with FB-SM shown in Fig.2.7 (b), which uses four semiconductor switches instead of two in each sub-module, was proposed to address the aforementioned DC fault issues with its inherent capability of DC fault blocking. In the case of an FB-SM, the capacitor voltage can additionally be connected with negative polarity, and as a result each FB-SM can generate three states: V_c, 0 and $-V_c$ based on the switching scheme shown in Table 2.4. This type of M2C is capable of suppressing a DC fault, but incurs the penalty of double the number of power devices compared to that of an M2C with HB-SM, which not only increases the cost but also results in higher power losses.

Table 2.5: Switching scheme for a clamp double half-bridge SM

S_1	S_2	S_3	S_4	S_5	V_{SM}	V_c
1	0	0	1	1	$2V_c$	Charging
0	1	1	0	1	0	No change
1	0	1	0	0	V_c	Charging
0	1	0	0	1	V_c	Charging
0	0	0	0	0	-	-

The switching scheme of an M2C with CD-SM, shown in Fig.2.7 (c), is given in Table 2.5 and is highlighted to achieve DC fault handling capability with fewer semiconductor devices when compared to an M2C with FB-SM, and slightly increased conduction losses compared to those of an M2C with HB-SM.

Other emerging types of modular multilevel converter are those based on aforementioned module structures, such as the hybrid modular multilevel converter [47], the crossed-connected SM modular multilevel converter [48] and the diode-clamped SM multilevel converter [49], etc. In respect to other topologies in the medium-voltage and high-voltage field, the M2C has the advantages of modularity, scalability, reliability, low semiconductor voltage ratings, low harmonic current content, and high efficiency with low actual switching frequency. Consequently, the M2C has become a preferred candidate for DC/AC conversion in various applications.

Apart from DC/AC conversion, the M2C can also be integrated efficiently as a DC converter for DC/DC applications. Direct-connected M2C based DC/DC conversion is not considered here, as the lack of galvanic isolation may cause a safety problem. A single phase bidirectional M2C-transformer-M2C configuration (M2C-T-M2C) shown in Fig.2.8 is introduced [50, 51], where two M2Cs are connected back-to-back through a low- or medium-frequency transformer to enable operation as an isolated bidirectional interface between the two DC grids. If bidirectional power flow is not required, one M2C can be replaced with a diode rectifier circuit. This topology can manage short-circuits at the input and output without the need for additional circuit breakers. Fundamental frequency switching is utilised in order to reduce passive

component requirements. The transformer provides galvanic isolation as well as voltage step-up/down. A similar topology has been presented [52], where each module contributes to voltage stepping in addition to the transformer step-up. This M2C-M2C DC/DC topology can be operated in full multilevel or quasi two-level mode [53], where quasi two-level mode allows the circuit to operate with lower capacitance values and the cells operate as an active clamp network.

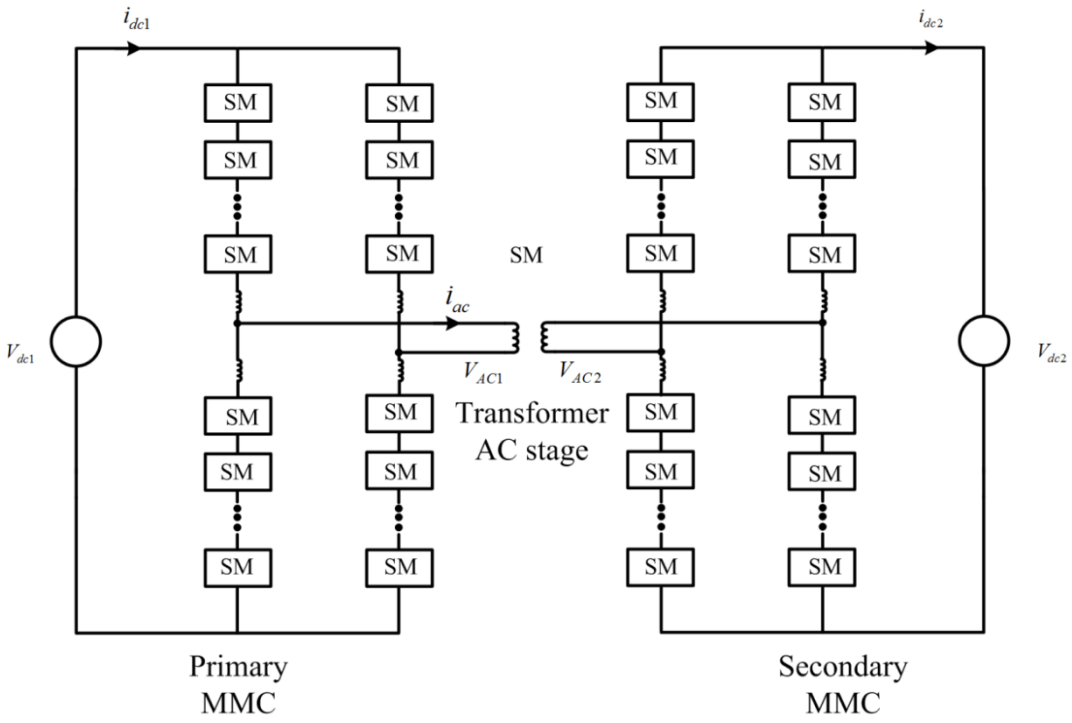


Fig.2.8: Single phase M2C-T-M2C DC/DC converter topology

Although the M2C-T-M2C DC/DC approach is attractive for DC voltage matching between DC collection network and transmission levels, the reduction that can be achieved in its size and weight due to the use of high frequency in the AC link will be limited by the high-voltage insulation and isolation requirements, i.e. a minimum clearance must be observed between phases, and transformer bushings must be mechanically strong to withstand forces that may be generated during normal transient operation. More importantly, as the transformer required for the AC stage is rated for full input power, high switching frequency operation is not viable for this transformer due to the construction difficulties and potential losses, resulting in low overall conversion efficiency [54]. The large number of capacitors also introduces higher cost and more difficult power stage dimensioning and the M2C module

capacitors require complex voltage balancing control. In addition, the voltage drop across the arm inductance can be significant in high-current applications, leading to significant reactive power losses [55-57].

The M2C has proven to be a feasible candidate in DC/AC power conversion at grid power frequency because of the reduced switching losses. However, the advantages are not so great when used for DC/DC conversion where a raised fundamental frequency is desired and the effectiveness of such M2C-T-M2C converters in DC/DC conversion is limited by the aforementioned disadvantages [56, 58, 59]. Therefore, a parallel-series modular structure is introduced in this study to address medium-voltage high-power DC/DC conversion. More discussion regarding this topology will be given in the following section.

2.1.4 Parallel-Series Modular Converter

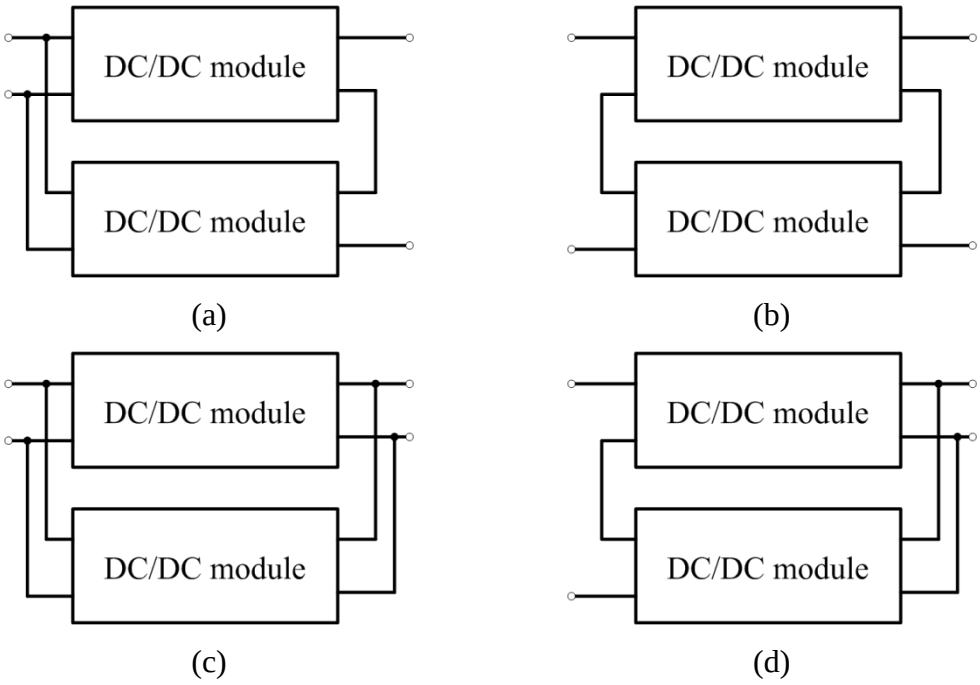


Fig.2.9: Four different common connections at the input and output for parallel-series modular converter (a) IPOS, (b) ISOS, (c) IPOP and (d) ISOP

Compared to the M2C modular converter, a more compact and lighter design that uses a few modules arranged in a parallel-series topology could provide an excellent solution for scalable DC/DC converters to facilitate operation at the required level [56]. These standardised modules, which are characterised by low-power rating, can

be grouped together in combinations of parallel or series connection, both at the output as well as at the input sides, to realise many input-output specifications and extend their application with robust and inexpensive low-rating modules [60]. Normally, parallel-series connected architectures can be classified into four categories: input-parallel output-series (IPOS), input-series output-series (ISOS), input-parallel output-parallel (IPOP), and input-series output-parallel (ISOP), as shown in Fig.2.9 [61].

Various types of parallel-series modular converters (PSMC) have been proposed for high-power application where the required voltage and power levels exceed those of individual devices or a single module. With parallel-series modular converters, higher switching frequency can be achieved without significant design challenges as the rating of each module is very low. Additionally, interleaved control of the multi-module converter can further reduce EMI filter size compared to other topologies [62]. Such a modular structure allows distribution of power amongst modules, thereby reducing thermal and electrical stresses on the switching devices and passive components of individual modules, as the parallel connection can reduce the current stresses whilst the voltage stresses can be reduced with series connection. It is also known that the parallel connections can increase output power and light-load efficiency by shutting down unnecessary modules, and that series connections can increase voltage handling capability, as collapsing one or more module input voltage enables more efficient low-voltage operation [63]. More importantly, the modular structure with redundancy provides great system reliability since single module failure does not cause a system failure. Moreover, the use of power electronic building blocks reduces production and deployment costs [43, 64]. Hence, this topology is currently of great interest.

Fig.2.10 shows an IPOS connected modular DC/DC converter with unidirectional power flow capability, which is a suggested candidate for a medium-voltage high-power offshore wind collection grid where bi-directional power flow capability is not needed. Connection of multiple low-power rated modules as in the IPOS DC/DC converter provides an excellent solution for the proposed application, as it improves robustness and the possibility of the fault-tolerant operation that is critical for an offshore application as a result of (n+k) designed redundancy. The use of a medium-

or high-frequency transformer results in a significant reduction in its volume and weight. However, special attention must be paid to the level of transformer isolation, since each module transformer must withstand the full MVDC voltage. Apart from the converter shown in Fig.2.10, converters with dual-active-bridge (DAB) modules, which enable bi-directional power flow in a DC distribution network, are receiving increased attention. The series resonant full-bridge DC/DC converter is another potential candidate in respect of soft-switching. More discussion regarding the choices of module topology will be given in Chapter 3.

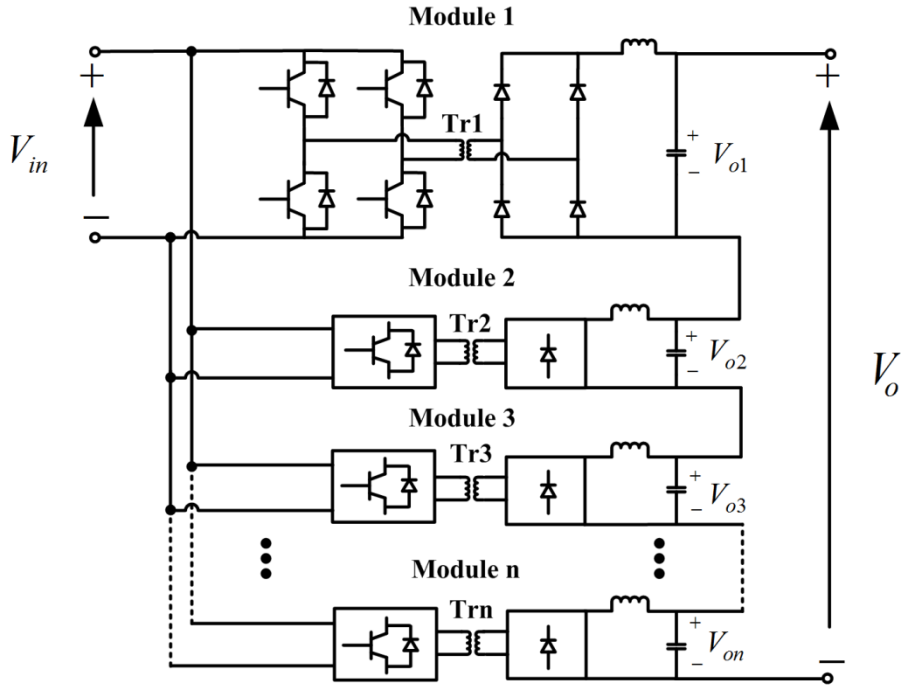


Fig.2.10: IPOS converter with full-bridge modules

In contrast to the topology where a single converter manages all of the power, the power of the parallel-series modular converter needs to be equally shared by all modules. Consequently, reliable operation of this modular DC/DC converter requires a control mechanism that ensures equal power sharing amongst the individual modules during steady-state as well as transient conditions, with ability to compensate for any mismatch in the passive components and other noticeable mismatches. Otherwise, it is possible that some modules deliver an excessive share of the power, leading to degradation of whole-system reliability due to excessive

thermal stresses [65]. Further discussion of the control aspects is provided in Chapter 3.

2.1.5 Review Summary

All types of converter mentioned earlier can be used to address high-power applications, but all present design compromises. A converter with series-connected devices is less competitive because it suffers high *dv*/*dt* which may cause component damage and restrict the achievable voltage level. In contrast, multilevel converters offer controllable thermal and electrical stresses on the power devices. However, for early-stage multilevel converters, system reliability may be degraded by the large quantity of diodes or flying capacitors, thereby limiting the possible benefits in high-power applications. The third option, i.e. a converter with a modular structure, shows considerable promise in addressing improvements in reliability by introducing a desired level of redundancy.

- Although the M2C is an attractive practical modular multilevel topology for DC/AC conversion in medium- or high-voltage applications, the implementation of M2C-T-M2C in the proposed offshore DC collection grid is limited by the ability to realise a reduced size and weight converter are a result of limitations imposed by the transformer as stated previously. In addition, the required capacitors and semiconductors occupy a large fraction of the overall volume, leading to high volume and cost. Another limitation of the M2C for the proposed application with high voltage ratios is due to the circulating current [56].
- Considering transformer design, PSMC can realise higher switching frequency and higher input-to-output ratio with low module transformer turns-ratio instead of one single full-scale high turns-ratio transformer which may become problematic [2]. Additionally, interleaved control of the module switches can decrease the output ripple considerably, which corresponds to further smaller size [66].

Hence, PSMC is the most promising candidate to address DC/DC conversion in offshore DC collection grids because it offers best overall performance.

2.2 DC/DC Converter Requirements

As interest in offshore DC collection networks increases, highly controllable and flexible power electronic based DC/DC converters are the most important elements required to realise the offshore DC collection network, and are currently of great interest.

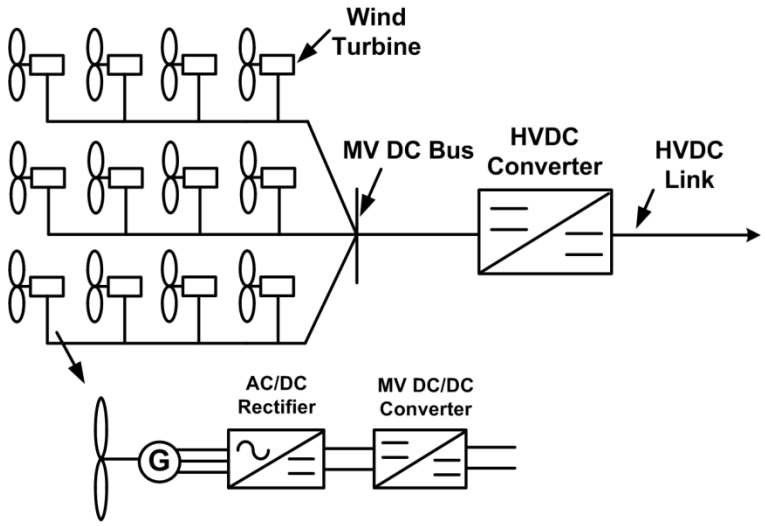


Fig.2.11: Proposed DC collection network for offshore generation

The MV DC/DC converter shown in Fig.2.11, consisting of a DC/AC inverter at the input, an AC link transformer and an AC/DC inverter at the output, is responsible for stepping up the voltage and providing galvanic isolation between low-voltage and medium-voltage. Thus, it represents a key component within the DC collection network. Nowadays, offshore wind turbines process powers in the MW range. Therefore, rating requirements for a full-scale DC/DC converter can be 1-10 MW to interface a DC wind turbine and boost its output voltage to the collection grid level. Whilst the previous section evaluated potential DC/DC converter solutions, another major objective is to investigate the essential operating requirements for the MV DC/DC converter, considering the input and output voltages, and the operating frequency.

2.2.1 Input Voltage

According to ETH Zurich's Institute of Environmental Engineering report, the top 10 available wind turbines are listed in Table 2.6. It can be seen from Table 2.6 that

most wind turbine generators normally operate at 690 V and possibly even lower. However, a high-voltage generator becomes more and more attractive for large wind turbines under the growing trends of wind turbine development, as it can reduce the current and thereby reduce the losses and the amount of heat generated [67]. Input voltage for a DC/DC converter is 6 kV [68], whilst the voltage is assumed to vary from 2 kV to 5 kV DC for a diode rectifier and is constant at 5 kV for an IGBT rectifier [69, 70]. Considering the future trend of higher generator output voltage, the input voltage of the medium-voltage high-power DC/DC converter is set to 2-6 kV.

Table 2.6: Top 10 biggest offshore wind turbines

Supply	***Power rating***	***Generator voltage***	***Generator type***
Sea Titan	10 MW	690 V	High-temperature superconductor generotor
Sway Turbine	10 MW	3.5 kV	Permanent magnet generator
Areva	8 MW	690 V	Permanent magnet generator
Vestas V164	8 MW	6.6 kV	Permanent magnet generator
Enercon E126	7.5 MW	690 V	Annular synchronous generator
Samsung S7.0 171	7 MW	3.3 kV	Permanent magnet generator
MHI Sea Angel	7 MW	6.6 kV	Brushless synchronous generator
Repower	6 MW	6.6 kV	Double Fed Asynchronous generator
Siemens SWT-6.0 150	6 MW	690 V	Permanent magnet generator
Alstom Haliade 150	6 MW	900 V	Permanent magnet generator

2.2.2 Output Voltage

The most common AC collection system for offshore wind farms is a 33 kV system, where the collection grid is a 33 kV AC voltage connected to the onshore grid through a 150 kV submarine cable. Since higher voltage levels can increase power transfer and reduce losses, moving from the presently favoured 33 kV voltage level to a higher voltage constitutes on-going research. In a DC configuration, the choice of collection grid voltage level has an influence on the efficiency and component size of the MV DC/DC converter, as well as the downstream HV DC/DC converter [71].

In addition, the output voltage defines the manner in which the modules of the proposed converter are stacked allowing the converter to achieve the required conversion ratio. In general, an isolation transformer with unity turns ratio is preferred since it results in simple construction and minimum leakage inductance. An MVDC grid has been designed for a 40 kV, 300 MW rated wind farm [72], and a 30 kV DC collection grid is proposed for an offshore wind farm with 150 MW power rating [11]. Hence, a DC voltage of 30-60 kV is considered as the nominal voltage for the collection grid.

2.2.3 Operation Frequency

Since the voltage at the terminals of the transformer does not need to be sinusoidal or at 50 or 60 Hz, a medium- or high-frequency transformer is selected in order to reach a high power density in the isolated DC/DC converter design. The use of a medium- or high-frequency isolation transformer in the AC link leads to a drastic reduction in the size and weight of the transformer, resulting in a compact DC/DC converter. It is stated that the estimated weight of a 1200 Hz transformer is 8 % of that of a 50 Hz transformer for a 3 MW wind turbine [69]. However, the switching frequency is a trade-off between power losses and power density. A 5 MW rated DAB 3-phase DC/DC converter with 1 kHz switching frequency has been proposed [10], as has a 166 kW rated DC/DC converter operating at 20 kHz [73]. In order to keep the size of the transformer as small as possible without significant sacrifice to its efficiency, a medium-frequency (1 kHz<f<20 kHz) transformer is preferred in this application. However, the combination of medium frequency and high power results in strong parasitic effects in the transformer core material, decreasing its efficiency and reliability. Transformer core material is discussed further in Chapter 3.

2.3 Summary

This chapter presents a brief review of various high-power converter topologies and focuses on possible candidates for DC/DC converters suitable for offshore wind farm collection networks. A range of circuit topologies have been examined, primarily considering the viability and reliability in high-power and medium-voltage applications. The capabilities and limitations of the presented converters have also

been appraised. Amongst the DC/DC converters discussed, the parallel-series modular converter has been evaluated to be the most promising and appropriate solution for offshore collection applications, offering features such as scalability, high efficiency, low production cost, small footprint, high reliability, and controlled *dv*/*dt*. Particularly, its modular architecture offers many advantages in terms of internal fault management, reconfiguration ability, and reduced filter size resulting from interleaved control. Additionally, the general operating requirements of the DC/DC converter for offshore collection grid have been defined.

2.4 Chapter Reference

[1] Z. Kai and R. Xinbo, "Control strategy to achieve input voltage sharing and output current sharing for input-series-output-parallel inverter," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, Rhodes, pp. 3655-3658, 2008.

[2] F. Haifeng and L. Hui, "High-Frequency Transformer Isolated Bidirectional DC&DC Converter Modules With High Efficiency Over Wide Load Range for 20 kVA Solid-State Transformer," Power Electronics, IEEE Transactions on, vol. 26, no. 12, pp. 3599-3608, 2011.

[3] Z. Biao, S. Qiang, L. Wenhua and S. Yandong, "Overview of Dual-Active-Bridge Isolated Bidirectional DC&DC Converter for High-Frequency-Link Power-Conversion System," Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4091-4106, 2014.

[4] T. C. Lim, B. W. Williams and S. J. Finney, "Active Snubber Energy Recovery Circuit for Series-Connected IGBTs," Power Electronics, IEEE Transactions on, vol. 26, no. 7, pp. 1879-1889, 2011.

[5] C. Abbate, G. Busatto and F. Iannuzzo, "High-Voltage, High-Performance Switch Using Series-Connected IGBTs," Power Electronics, IEEE Transactions on, vol. 25, no. 9, pp. 2450-2459, 2010.

[6] H. Soonwook, C. Venkatesh and D. A. Torrey, "Series connection of IGBT's with active voltage balancing," Industry Applications, IEEE Transactions on, vol. 35, no. 4, pp. 917-923, 1999.

[7] Z. Chunpeng, W. Yingdong, J. Qirong and T. Luyuan, "Dynamic voltage balancing of series connected IGBTs using slope regulating and voltage clamping," in Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, Atlanta, GA, pp. 4336-4340, 2010.

[8] J. W. Baek, D. W. Yoo and H. G. Kim, "High voltage switch using series-connected IGBTs with simple auxiliary circuit," in Industry Applications Conference, 2000. Conference Record of the 2000 IEEE, pp. 2237-2242 vol.4, 2000.

[9] C. Gerster, "Fast high-power/high-voltage switch using series-connected IGBTs with active gate-controlled voltage-balancing," in Applied Power Electronics Conference and Exposition, 1994. APEC '94. Conference Proceedings 1994., Ninth Annual, pp. 469-472 vol.1, 1994.

[10] N. Soltau, H. Stagge, R. W. De Doncker and O. Apeldoorn, “Development and demonstration of a medium-voltage high-power DC-DC converter for DC distribution systems,” in Power Electronics for Distributed Generation Systems (PEDG), 2014 IEEE 5th International Symposium on, pp. 1-8, 2014.
[11] C. Meyer, M. Hoing, A. Peterson and R. W. De Doncker, “Control and Design of DC Grids for Offshore Wind Farms,” Industry Applications, IEEE Transactions on, vol. 43, no. 6, pp. 1475-1482, 2007.
[12] R. Withanage and N. Shammas, “Series Connection of Insulated Gate Bipolar Transistors (IGBTs),” Power Electronics, IEEE Transactions on, vol. 27, no. 4, pp. 2204-2212, 2012.
[13] P. R. Palmer, H. S. Rajamani and N. Dutton, “Experimental comparison of methods of employing IGBTs connected in series,” Electric Power Applications, IEE Proceedings -, vol. 151, no. 5, pp. 576-582, 2004.
[14] C. Jiann-Fuh, L. Jiunn-Nan and A. Tsu-Hua, “The techniques of the serial and paralleled IGBTs,” in Industrial Electronics, Control, and Instrumentation, 1996., Proceedings of the 1996 IEEE IECON 22nd International Conference on, pp. 999-1004 vol.2, 1996.
[15] G. Busatto, B. Cascone, L. Fratelli and A. Luciano, “Series connection of IGBTs in hard-switching applications,” in Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE, pp. 825-830 vol.2, 1998.
[16] F. V. Robinson and V. Hamidi, “Series connecting devices for high-voltage power conversion,” in Universities Power Engineering Conference, 2007. UPEC 2007. 42nd International, Year, pp. 1134-1139.
[17] L. Ting, Z. Zhengming, J. Shiqi, Y. Hualong and Y. Liqiang, “Active Clamping Circuit With Status Feedback for Series-Connected HV-IGBTs,” Industry Applications, IEEE Transactions on, vol. 50, no. 5, pp. 3579-3590, 2014.
[18] J. Shiqi, L. Ting, Z. Zhengming, Y. Hualong and Y. Liqiang, “Series-Connected HV-IGBTs Using Active Voltage Balancing Control With Status Feedback Circuit,” Power Electronics, IEEE Transactions on, vol. 30, no. 8, pp. 4165-4174, 2015.
[19] F. Zhang, Y. Ren, M. Tian and X. Yang, “Active gate charge control strategy for series-connected IGBTs,” in Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on, Year, pp. 1840-1845.
[20] J. HÄFNER; and B. JACOBSON, “Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids,” in Cigre 2011, The Electric Power System of the Future-Integrating Supergrids and Microgrids International Symposium, BOLOGNA, 2011.
[21] B. Jacobson;, P. Karlsson;, G.Asplund;, L.Harnnart; and a. T. Jonsson, “VSC-HVDC Transmission with Cascaded Two-level Converters,” in CIGRE 2010, 2010.
[22] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday and B. W. Williams, “Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers,” Power Electronics, IEEE Transactions on, vol. 30, no. 10, pp. 5439-5457, 2015.
[23] R. Feldman, M. Tomasini, E. Amankwah, J. C. Clare, P. W. Wheeler, D. R. Trainer and R. S. Whitehouse, “A Hybrid Modular Multilevel Voltage Source

Converter for HVDC Power Transmission," Industry Applications, IEEE Transactions on, vol. 49, no. 4, pp. 1577-1588, 2013.
[24] S. Allebrod, R. Hamerski and R. Marquardt, "New transformerless, scalable Modular Multilevel Converters for HVDC-transmission," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, Year, pp. 174-179.
[25] R. H. Baker, Electric Power Converter, U.S. Patent, Feb. 1975.
[26] J. Rodriguez, L. Jih-Sheng and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," Industrial Electronics, IEEE Transactions on, vol. 49, no. 4, pp. 724-738, 2002.
[27] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," Industrial Electronics, IEEE Transactions on, vol. 57, no. 7, pp. 2219-2230, 2010.
[28] A. Das, K. Sivakumar, R. Ramchand, C. Patel and K. Gopakumar, "A Pulsewidth Modulated Control of Induction Motor Drive Using Multilevel 12-Sided Polygonal Voltage Space Vectors," Industrial Electronics, IEEE Transactions on, vol. 56, no. 7, pp. 2441-2449, 2009.
[29] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos and D. Boroyevich, "Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point," Industrial Electronics, IEEE Transactions on, vol. 54, no. 4, pp. 2288-2294, 2007.
[30] M. Zygmanowski, B. Grzesik and J. Michalak, "Power conditioning system with cascaded H-bridge multilevel converter DC-link voltage balancing method," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, Year, pp. 1-10.
[31] E. Villanueva, P. Correa, J. Rodriguez and M. Pacas, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems," Industrial Electronics, IEEE Transactions on, vol. 56, no. 11, pp. 4399-4406, 2009.
[32] J. Rodriguez, S. Bernet, W. Bin, J. O. Pontt and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," Industrial Electronics, IEEE Transactions on, vol. 54, no. 6, pp. 2930-2945, 2007.
[33] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," Industry Applications, IEEE Transactions on, vol. IA-17, no. 5, pp. 518-523, 1981.
[34] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," in Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE, Year, pp. 1336-1343 vol.2.
[35] G. Ortiz, "High-Power DC-DC Converter Technologies for Smart Grid and Traction Applications," Department of Information Technology and Electrical Engineering, ETH, Zurich, 2014.
[36] A. Nami, F. Zare, A. Ghosh and F. Blaabjerg, "Multi-output DC-DC converters based on diode-clamped converters configuration: topology and control strategy," Power Electronics, IET, vol. 3, no. 2, pp. 197-208, 2010.

[37] G. P. Adam, S. J. Finney, A. M. Massoud and B. W. Williams, “Capacitor Balance Issues of the Diode-Clamped Multilevel Inverter Operated in a Quasi Two-State Mode,” Industrial Electronics, IEEE Transactions on, vol. 55, no. 8, pp. 3088-3099, 2008.

[38] G. P. Adam, K. H. Ahmed, S. J. Finney and B. W. Williams, “Modular multilevel converter for medium-voltage applications,” in Electric Machines & Drives Conference (IEMDC), 2011 IEEE International, Year, pp. 1013-1018.

[39] T. A. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” in Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE, Year, pp. 397-403 vol.1.

[40] E. Deschamps, A. R. Borges and A. S. G. da Silva, “The influence of gate signals differences on the voltage across the switches in a flying-capacitor DC-to-DC multilevel converter,” in Industrial Electronics, 2003. ISIE '03. 2003 IEEE International Symposium on, pp. 656-661 vol. 1, 2003.

[41] L. Wuhua, J. Qun, M. Ye, L. Chushan, D. Yan and H. Xiangning, “Modular Multilevel DC/DC Converters With Phase-Shift Control Scheme for High-Voltage DC-Based Systems,” Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 99-107, 2015.

[42] M. Khazraei, H. Sepahvand, K. A. Corzine and M. Ferdowsi, “Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters,” Industrial Electronics, IEEE Transactions on, vol. 59, no. 2, pp. 769-778, 2012.

[43] R. Xinbo, C. Wu, C. Lulu, C. K. Tse, Y. Hong and Z. Tao, “Control Strategy for Input-Series&Output-Parallel Converters,” Industrial Electronics, IEEE Transactions on, vol. 56, no. 4, pp. 1174-1185, 2009.

[44] A. Parastar, K. Yong Cheol and S. Jul-Ki, “Multilevel Modular DC/DC Power Converter for High-Voltage DC-Connected Offshore Wind Energy Applications,” Industrial Electronics, IEEE Transactions on, vol. 62, no. 5, pp. 2879-2890, 2015.

[45] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range,” in Power Tech Conference Proceedings, 2003 IEEE Bologna, pp. 6 pp. Vol.3, 2003.

[46] R. Marquardt, “Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications,” in Power Electronics Conference (IPEC), 2010 International, pp. 502-507, 2010.

[47] Z. Rong, X. Lie and Y. Liangzhong, “An improved modular multilevel converter with DC fault blocking capability,” in PES General Meeting | Conference & Exposition, 2014 IEEE, pp. 1-5, 2014.

[48] Q. Jiangchao, M. Saeedifard, A. Rockhill and Z. Rui, “Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits,” Power Delivery, IEEE Transactions on, vol. 30, no. 1, pp. 385-394, 2015.

[49] L. Xiaoqian, L. Wenhua, S. Qiang, R. Hong and X. Shukai, “An enhanced MMC topology with DC fault ride-through capability,” in Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE, pp. 6182-6188, 2013.

[50] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F. Canales and Y. R. De Novaes, “A versatile DC-DC converter for energy collection and distribution using the Modular Multilevel Converter,” in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1-10, 2011.

[51] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales and Y. R. De Novaes, “Isolated DC/DC Structure Based on Modular Multilevel Converter,” Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 89-98, 2015.

[52] T. Luth, M. M. C. Merlin, T. C. Green, F. Hassan and C. D. Barker, “High-Frequency Operation of a DC/AC/DC System for HVDC Applications,” Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4107-4115, 2014.

[53] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, “Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability,” Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 108-123, 2015.

[54] G. J. Kish, M. Ranjram and P. W. Lehn, “A Modular Multilevel DC/DC Converter With Fault Blocking Capability for HVDC Interconnects,” Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 148-162, 2015.

[55] V. Staudt, R. Bartelt and C. Heising, “Fault Scenarios in DC Ship Grids: The advantages and disadvantages of modular multilevel converters,” Electrification Magazine, IEEE, vol. 3, no. 2, pp. 40-48, 2015.

[56] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge and R. W. De Doncker, “Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids,” Power Electronics, IEEE Transactions on, vol. 30, no. 1, pp. 124-137, 2015.

[57] R. Lizana, M. Perez, J. Rodriguez and W. Bin, “Modular multilevel converter based on current source H-bridge cells implemented with low cost reversing conducting IGCT,” in Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, pp. 3363-3367, 2013.

[58] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, “Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer with DC Fault Isolation Capability,” Power Electronics, IEEE Transactions on, vol. PP, no. 99, pp. 1-1, 2014.

[59] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano and A. Rufer, “Design and Control of a Modular Multilevel DC/DC Converter for Regenerative Applications,” Power Electronics, IEEE Transactions on, vol. 28, no. 8, pp. 3970-3979, 2013.

[60] S. Chunwei, R. Zhao, L. Wangqing and Z. Zheng, “A novel control strategy for input-parallel-output-series inverter system,” in Electrical Machines and Systems (ICEMS), 2011 International Conference on, Beijing, pp. 1-5, 2011.

[61] R. Ayyanar, R. Giri and N. Mohan, “Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme,” Power Electronics, IEEE Transactions on, vol. 19, no. 6, pp. 1462-1473, 2004.

[62] Y. Lian, G. P. Adam, D. Holliday and S. J. Finney, “Active power sharing in input-series-input-parallel output-series connected DC/DC converters,” in

Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE, Charlotte, NC, pp. 2790-2797, 2015.

[63] S. Effler, M. Halton and K. Rinne, “Efficiency-Based Current Distribution Scheme for Scalable Digital Power Converters,” Power Electronics, IEEE Transactions on, vol. 26, no. 4, pp. 1261-1269, 2011.

[64] C. Wu, R. Xinbo, Y. Hong and C. K. Tse, “DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications,” Power Electronics, IEEE Transactions on, vol. 24, no. 6, pp. 1463-1474, 2009.

[65] J. S. Glaser and A. F. Witulski, “Output plane analysis of load-sharing in multiple-module converter systems,” Power Electronics, IEEE Transactions on, vol. 9, no. 1, pp. 43-50, 1994.

[66] P. S. Shenoy and P. T. Krein, “Local control of multiple module dc-dc converters,” in Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on, Boulder, CO, pp. 1-6, 2010.

[67] L. Söder and T. Ackermann, "Wind Power in Power Systems: An Introduction," Wind Power in Power Systems, pp. 47-72: John Wiley & Sons, Ltd, 2012.

[68] O. Martander, “DC grid for wind farms,” Dept. of EPE, Chalmers University of Technology, Landala,Sweden, 2002.

[69] L. Max, “Design and Control of a DC Collection Grid for a Wind Farm,” Department of Energy and Environment, Chalmers University of Technology, Sweden, 2009.

[70] L. Max and T. Thiringer, “Control method and snubber selection for a 5 MW wind turbine single active bridge DC/DC converter,” in Power Electronics and Applications, 2007 European Conference on, pp. 1-10, 2007.

[71] C. Wu, A. Huang, S. Lukic, J. Svensson, L. Jun and W. Zhenyuan, “A comparison of medium voltage high power DC/DC converters with high step-up conversion ratio for offshore wind energy systems,” in Energy Conversion Congress and Exposition (ECCE), 2011 IEEE, Phoenix, AZ, pp. 584-589, 2011.

[72] J. Robinson, D. Jovcic, Joo, x and G. s, “Analysis and Design of an Offshore Wind Farm Using a MV DC Grid,” Power Delivery, IEEE Transactions on, vol. 25, no. 4, pp. 2164-2173, 2010.

[73] G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar and O. Apeldoorn, “Modeling of Soft-Switching Losses of IGBTs in High-Power High-Efficiency Dual-Active-Bridge DC/DC Converters,” Electron Devices, IEEE Transactions on, vol. 60, no. 2, pp. 587-597, 2013.

Chapter 3: Parallel-Series Modular DC/DC Converter and Module Selection

Chapter 2 has presented the main motivations for suggesting parallel-series modular converters for realisation of offshore wind farm DC collection networks. However, many design aspects need to be investigated to determine their feasibility for the proposed application. In this chapter, four types of parallel or series connected modular DC/DC converters will be explored, namely, input-series output-series (ISOS), input-series output-parallel (ISOP), input-parallel output-parallel (IPOP), and input-parallel output-series (IPOS). Moreover, the power sharing control strategies for each type are investigated, since the viability of these converters for the aforesaid application is dependent on the power sharing stability. In Section 2, three choices for possible module topologies are evaluated, including discussion and assessment of merits and limitations. Finally, the design of the converter is evaluated further in the context of the transformer core material.

3.1 Parallel-Series Connection

The parallel-series modular converter, which consists of multiple modules connected in series or parallel both at the input and output sides, has drawn attention due to its distinct features, including the possibility of usage of low-power rating devices for a high-power application, increased system reliability due to the reduced stresses on the devices, increased power density with interleaved control amongst the modules, and ease of reconfiguration of the power stage to meet different input and output voltage specifications [1-3]. In addition, the significant benefits regarding cost and time due to the standardised modular approach is discernible, and more importantly, fault-tolerant redundancy can be easily implemented with such a modular structure.

Amongst the four possible connections presented in Chapter 2, the structure should be chosen depending on the particular types of applications being considered. Generally, parallel connection is an approach that is widely used in applications involving high current at the input or output sides. For applications involving high input or output voltage, series connection is suitable.

Despite the claimed modularity, practical modules are usually not identical due to the different tolerance and nonlinearities of the active and passive components used in the power stage. It is therefore important to consider issues resulting from mismatches between the modules [2]. Normally, the module that contributes more power may experience thermal overstress, and this may degrade the system performance and result in premature system failure. Consequently, it is essential to develop a dedicated power sharing control scheme to distribute the total power equally amongst the modules during steady-state and transient operations [4]. Generally, power sharing methods are classified into two categories from a control mechanism viewpoint. These are the droop method and the active sharing method. Although droop control does not need any wire interconnections, only active sharing methods are considered in this study due to the limited regulation of droop control.

Previous research has explored the common duty-cycle scheme [5], the master-slave approach [6], the average sharing scheme [7], and other active sharing control approaches. Common duty-cycle control, which simplifies control functions with a single central controller, is an extremely simple and effective technique. However,

this centralised control yields single points of failure and cannot respond to module mismatches. When the master-slave and average sharing approaches are employed to equalise power distribution between non-identical modules, each module requires its own controller to obtain each module's local information when making the control decisions [8]. In the master-slave scheme, one master module is responsible for load regulation whilst the slave is devoted to ensuring power balance. In contrast, instead of following the master module's reference, all the modules have an equalised role in the average sharing control system. For transient response, the average sharing scheme provides more stable performance than the master-slave sharing method. Considering reliability, the side effect of the master-slave sharing method is that a defective master may cause failure of the whole system. This is in contrast to an average sharing control system where a damaged module does not give rise to whole system failure [9]**.** However, fault ride-through under slave module failure may be achieved more simply using master-slave control, with power being evenly shared amongst the remaining healthy modules to avoid module overload that could lead to cascade failure of the entire system. This is because fault tracking is easier than with the average sharing scheme where all modules take the same roles [10]. More discussion regarding the control techniques will be provided in the following sections.

Table 3.1: Comparison of four parallel-series modular converters

Topology	***Suitable application***	***Required control***
ISOP	High input voltage High output current	Input voltage control Output current control
ISOS	High input voltage High output voltage	Input voltage control Output voltage control
IPOP	High input current High output current	Input current control Output current control
IPOS	High input current High output voltage	Input current control Output voltage control

Table 3.1 illustrates suitable applications for the four parallel-series connections, and the controls that have to be integrated to equalise the currents and voltages at the input and output sides of the individual modules. It can be seen that the objective of parallel connection is to share the current amongst the constituent modules, whilst

the objective of series connection is to balance the voltage amongst the constituent modules. The following section will focus on the features and control methods for the four connections presented in Table 3.1.

3.1.1 Input-Series Output-Parallel Connection

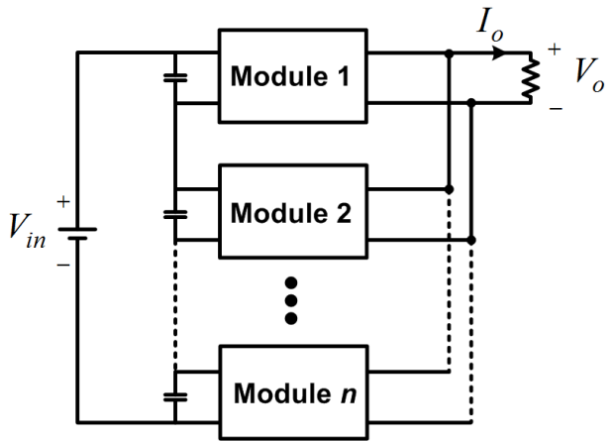


Fig.3.1: Schematic of an *n*-module ISOP DC/DC converter

The ISOP system shown in Fig.3.1 is widely adopted in high-speed train power systems, industrial drives and undersea observatories [11-13]. In addition, this configuration is a promising candidate for realising high step-down voltage ratios [14] with small transformer turns-ratio, leading to small leakage inductance and, thus, low power loss [15]. Additionally, the ability to dynamically collapse the input voltage and shut down modules according to input voltage requirements can achieve a higher overall efficiency and a wider operating range [16].

In the ISOP configuration, the input voltage for each module is reduced to V_{in}/n, whilst the modular output current is reduced to I_o/n, where n is the number of the modules, and V_{in} and I_o are the input voltage and output current of the ISOP converter respectively. The main objective of the control system is to achieve power sharing balance irrespective of module mismatch, and to ensure even input voltage sharing (IVS) and output current sharing (OCS) for all constituent modules.

The common duty-cycle scheme is proposed [5, 17] which utilises a common output voltage controller with an inner load current loop without specific input voltage or output current sharing loops. This scheme ensures power sharing through the inherent self-correcting mechanism. A form of sensor-less current-mode control is

proposed [15] to achieve IVS, which has a similar control mechanism as that of common duty-cycle control. Although common duty-cycle control can achieve stable operation using a simple control scheme, component tolerances affect its power, input voltage and output current sharing performance. It ensures equal power sharing only when modules are identical [18]. Moreover, it does not facilitate reconfiguration, which is necessary to enable isolation of a failed module, whilst the system remains operational [19], and this indicates the need for a dedicated power sharing control scheme.

In order to guarantee power sharing, a three-loop control scheme, consisting of a common output voltage loop, individual inner current loops and IVS loops, is proposed [20]. However, the interaction amongst the control loops may degrade its performance. A decoupled three-loop master-slave control scheme is proposed [19] to achieve IVS, however with this control technique, the system may fail once the master module has a malfunction. In contrast to the fact that a dedicated IVS controller results in uniform OCS in the presence of substantial differences in various parameters, the OCS loop does not guarantee stable operation due to the induced runaway of the module input voltages caused by the negative input resistance property of the DC/DC converters [12, 20]. However, a cross-feedback OCS scheme [21] which eliminates the input voltage feed-forward term shows satisfactory results.

3.1.2 Input-Series Output-Series Connection

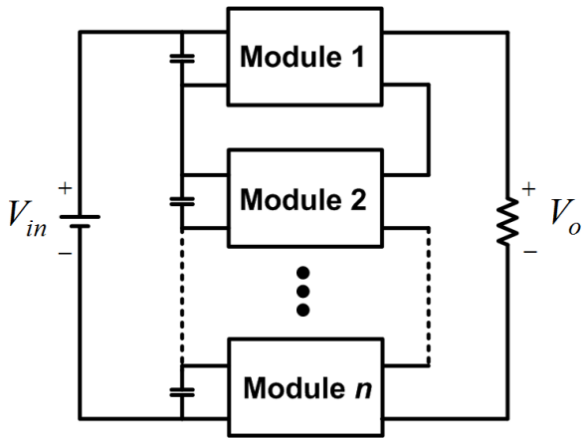


Fig.3.2: Schematic of an *n*-module ISOS DC/DC converter

Similar to the ISOP connected modular converter, the ISOS configuration shown in Fig.3.2 can facilitate high input voltage applications due to the same input-series connection. In addition, this configuration is desirable for high input and output voltage applications, such as medium-voltage power systems. The input and output voltages of each module are V_{in}/n and V_o/n respectively.

Proper operation of an ISOS system is achieved when even input and output voltage sharing is ensured amongst the modules. Unlike an ISOP system, the ISOS configuration tends to be unstable under common duty-ratio control due to its weak natural balancing ability [1]. Similar to the ISOP configuration, it requires an IVS loop for the input-series connection [12]. Hence, a dedicated input voltage control needs to be implemented for an ISOS system to achieve IVS and output voltage sharing (OVS) in the presence of mismatches between the modules.

A three-loop control scheme, including a common load voltage controller, an input voltage controller and an individual inner current controller, has been proposed [7]. A similar control scheme is adopted for an ISOS connected inverter system [22]. Although it is found that IVS and OVS cannot be realised through an OVS controller, OVS control has been successfully applied to a two-module ISOS DC/DC converter by exchanging their duty cycles [19]. However, it is only suitable for a two-module ISOS system and cannot be applied to an ISOS system consisting of three or more modules. A control scheme based on the output-voltage gradient regulation characteristics for each module and without a current loop has been presented [23]. However, individual current loops are necessary to provide overload protection and DC fault protection in the proposed application.

3.1.3 Input-Parallel Output-Parallel Connection

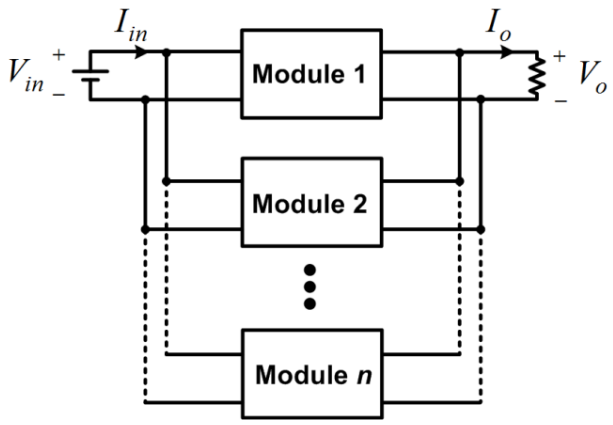


Fig.3.3: Schematic of an *n*-module IPOP DC/DC converter

Fig.3.3 shows the block diagram of an IPOP connected modular DC/DC converter. The parallel system of power modules is desirable for high-power applications, with high input and output currents. Moreover, connecting the modules in an IPOP configuration provides the advantages of increased power capacity, power density and reliability of the power electronic system [24-26]. For computer and telecommunication industries, and distributed power systems, the IPOP system is preferred [11]. The input and output currents of each module in an IPOP converter are I_{in}/n and I_o/n respectively, where I_{in} and I_o respectively are the converter input and output currents. It is known that the major concern of operating modules in parallel is the current distribution between the modules.

Several control schemes have been proposed to ensure equal input and output current sharing between non-identical modules. A common duty-cycle approach has been discussed [25], however, precise current balance cannot be obtained. Two different schemes for realising active load current sharing between these parallel modules have been proposed [9], where master-slave control and central-limit control are addressed and compared, considering dynamic performance and fault-tolerant operation. A systematic classification of all possible parallel connected structures and control configurations of load current sharing for the IPOP architecture have been presented [27], proving the presence of a current sharing loop is important for achieving good performance.

3.1.4 Input-Parallel Output-Series Connection

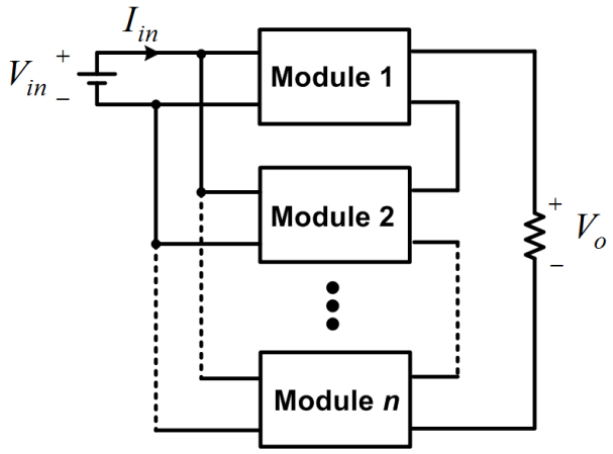


Fig.3.4: Schematic of an *n*-module IPOS DC/DC converter

In an effort to address the high-power step-up converter, an IPOS configuration that involves parallel connection at the input sides and series connection at the output sides is introduced. Fig.3.4 shows the IPOS connected DC/DC converter which can be used for reducing the input current stresses and output voltage stresses since the input current and output voltage for each module are reduced to I_{in}/n and V_o/n respectively. Apart from the benefits of input-parallel connection, an output-series connected converter enables the flexibility of expansion and transforms input voltage to a much higher output voltage. Consequently, a transformer with lower voltage ratio can be applied with the IPOS system, leading to lower leakage inductance [28, 29].

Since the modules share a common input power source and a common output load, as shown in Fig.3.4, component variations would result in non-uniformly distributed power between the modules. Hence, it is necessary to incorporate a dedicated OVS loop or input current sharing (ICS) loop [30].

One control topology [31] utilises one master's voltage loop output as the slaves' inner current control loop reference. However, equal power regulation is only achieved when it is assumed that all modules are identical. A common duty-cycle scheme [32] has been shown to be incapable of ensuring power sharing between modules without a dedicated power sharing loop. Moreover, this approach is not suitable for medium-voltage applications, as modules may be exposed to the risk of

damage from over-voltages during transients. A three-loop control system for a DC/AC inverter has been proposed [33], and consists of an outer common output voltage loop, OVS loops and inner current loops, where each modular output voltage is regulated to V_o/n to ensure power balance. However, the interaction between the multiple loops and the fault-tolerant control scheme are not considered.

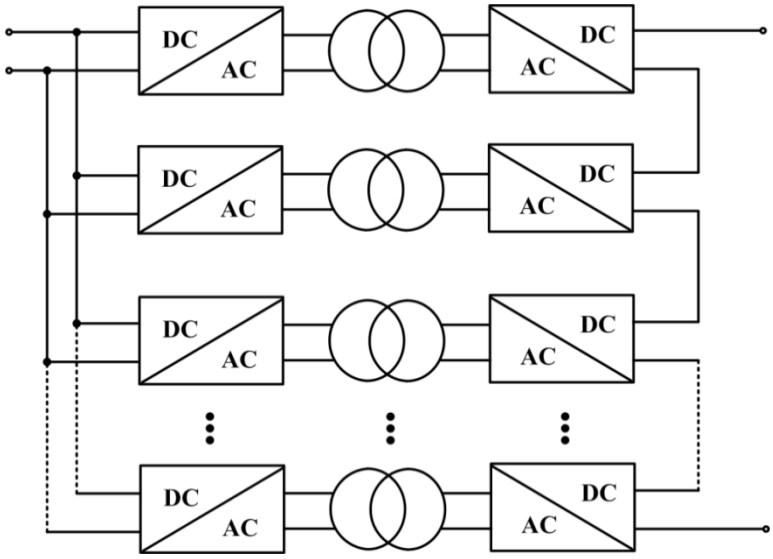


Fig.3.5: Proposed IPOS connected modular DC/DC converter configuration

It is shown that an IPOS system is well suited for renewable energy systems, particularly, when high step-up ratio is required. For example, an IPOS connected modular DC/DC converter for integration of a low-voltage renewable energy source to a medium-voltage network, such as the collection networks for airborne wind energy, offshore wind energy and photovoltaic power systems, has been employed [34-36]. A 20 MW, 250 kV DC boost conversion system for offshore HVDC transmission system, consisting of 40 DAB modules in an IPOS connection has been proposed [37]. Hence, a DC/DC converter with IPOS connection and galvanic isolation provided by a medium-frequency transformer, as shown in Fig.3.5, is selected to address the conversion system for the offshore wind farm MVDC collection network.

3.2 Design Aspects of Converter Module

In the proposed application, the DC/DC converter is required to operate at megawatt power levels with high-voltage and at medium-frequency. Currently, there is no such

DC/DC converter available in the market for scaling up to this power level. IPOS topologies previously outlined are employed to help reduce the individual module rating. Apart from the IPOS topologies, several design aspects need to be specified to address the medium-power DC/DC converter. Firstly, the choice of module topology is one of the most important aspects to achieve high-efficiency and good performance over a wide range of operating conditions. Hence, the following section firstly examines three isolated DC/DC converters as the potential choices of module topology to determine the most suitable topology. In addition, the medium-frequency transformer is another key element that provides isolation and step up of the voltage levels. Consequently, issues associated with choices of transformer core are also analysed in the following section.

3.2.1 Choices of Module Topology

Fig.3.6 shows a general classification of high-power DC/DC converters with galvanic isolation according to their operating features. The three main categories are non-resonant topologies, resonant topologies and hybrid topologies.

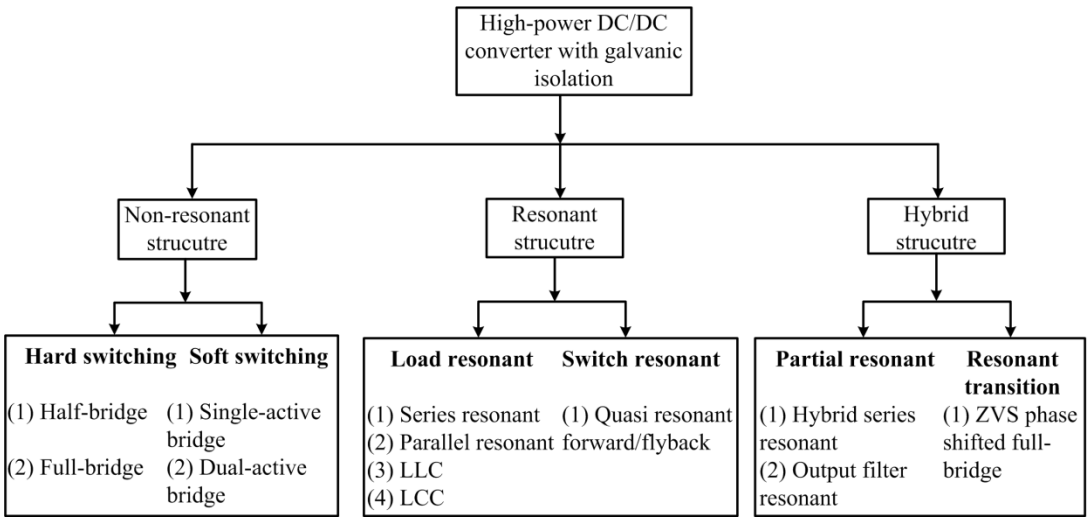


Fig.3.6: General classification of DC/DC converter with galvanic isolation

A. Phase Shifted Full-bridge Converter

For the non-resonant hard switching topologies, the switches experience significant high power losses due to the simultaneous overlap of voltage and current during the switching transients. Comparing the half-bridge and full-bridge topologies, the maximum output voltage of the full-bridge converter is twice that of the half-bridge

converter with the same DC input voltage, which offers a distinct advantage in high-power applications. Full-bridge converters can either be controlled by hard switching control or phase shift control with hybrid structure. For zero voltage switching (ZVS) phase shifted full-bridge converters, the resonant transition is enabled by the snubber capacitors across the transistors, leading to minimised switching losses and EMI signature. Moreover, a much higher switching frequency is possible with this technique when compared to a hard switching topology. Therefore, a phase shifted full-bridge topology outperforms the conventional full-bridge converter and is therefore adopted in this study. Note that it is difficult to sustain soft switching over the whole load range.

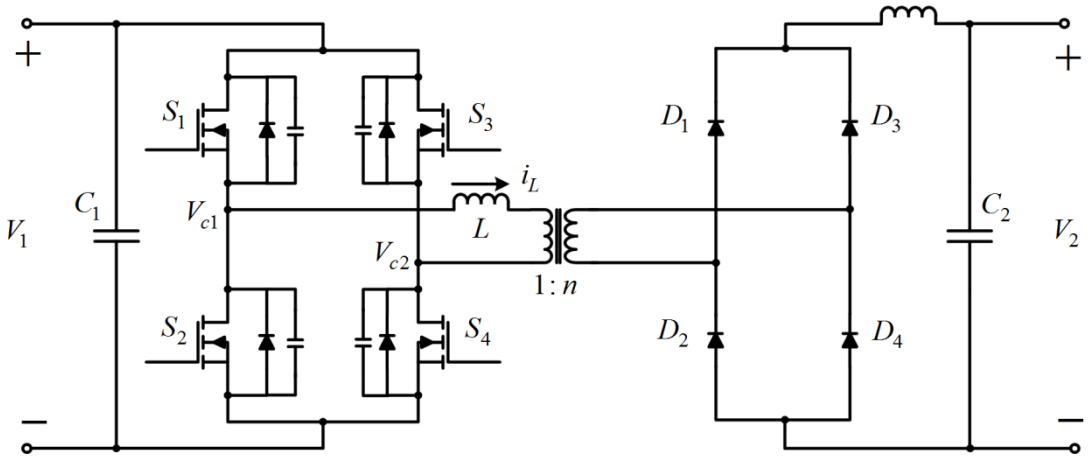


Fig.3.7: ZVS phase shifted full-bridge converter

A phase shifted full-bridge converter, shown in Fig.3.7, consists of a full-bridge inverter, a diode bridge rectifier and a transformer, and is one of the most attractive DC/DC converters due to its ability to achieve ZVS for all the active switches through phase shift modulation (PSM) and the inclusion of parasitic circuit elements.

S_1 and S_2 are switched in anti-phase with 50 % duty cycle. S_3 and S_4 are similarly switched. The switching control signals for S_1 and S_2 are phase shifted with respect to those applied to S_3 and S_4 to form a PWM output signal and V_{C1} and V_{C2} are the equivalent AC output voltages from each leg. The phase shift angle φ, shown in Fig.3.8 dictates the amount of power transferred to the load. It can be seen from Fig.3.8 that the controlled bridge presents a square waveform voltage to the high-frequency transformer in the ac link. Furthermore, EMI filter design can be simplified as a result of constant frequency control. For ZVS operation, the leakage

inductance of the transformer and the snubber capacitances across the switches are utilised as the resonant tank to reduce the turn on and turn off losses. Hence, the phase shifted full-bridge converter reduces the switching losses, thereby enabling a higher switching frequency.

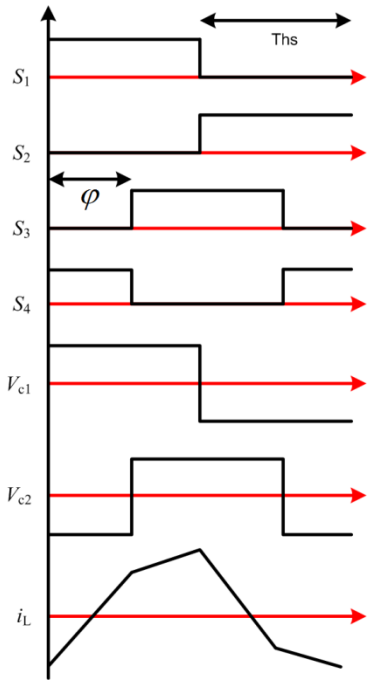


Fig.3.8: PWM and operating waveforms for phase shifted full-bridge converter

Although the presence of circulating current during off-time and the hard switching for the diode bridge limit its benefits, the phase shifted full-bridge converter is a viable choice for the proposed application due to its simplicity, low mass magnetics, constant frequency operation, high efficiency and lack of auxiliary circuits [38].

B. Full-Bridge LC Resonant Converter

In respect of ZVS or ZCS soft-switching, load resonant converters, where a resonant network comprising inductors and capacitors modifies the voltage and current in order to turn on and off at zero voltage or zero current, are also widely implemented in high-power applications [39, 40]. Although there are number of possible combinations in the resonant network, the three widely used load resonant converters are series resonant converter (SRC), parallel resonant converter (PRC) and series-parallel resonant converter (SPRC). The latter one, consisting of three reactive elements in the resonant network e.g. *LCC* or *LLC*, combines the advantages of the

SRC and PRC at the cost of more complex designs and more elements. Collectively, resonant converters help to reduce losses by switching at zero voltage or current, thus increasing power density and enabling operation at a higher switching frequency [41, 42].

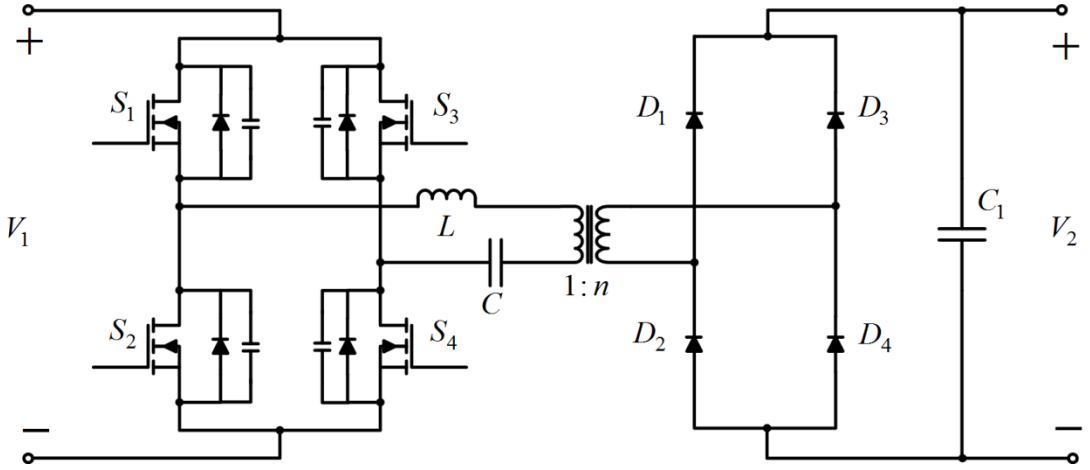


Fig.3.9: Full-bridge *LC* resonant converter

For the SRC converter shown in Fig.3.9, two reactive elements (inductance *L* and capacitance *C*) are placed in series with the load. The converter adjusts its switching frequency above but near the resonant frequency of the AC link shown in (3.1) to obtain ZVS operation.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

However, the full-bridge resonant converter requires a large frequency range under light load conditions, leading to large dimension passive components. Otherwise, soft switching is only limited to a narrow load range, and the circulating currents are increased [43]. Further, the SRC cannot be regulated in the case of no-load. In addition, the current through and voltage across the resonant tank tend to be extremely high due to resonance, thus increasing stresses and requiring a large and heavy resonant inductor and capacitor. Note that the values of the characteristic impedance of the tank and the transformer turns-ratio need to be carefully chosen to yield the lowest peak resonant tank voltage and current for a given output power [44]. In addition, the interleaved control scheme cannot apply to parallel-series connected modular converter with full-bridge LC resonant modules due to the variable frequency operations between the moduels. For the PRC configuration, the output

voltage can be regulated at no load. However, the currents through the switches and resonant tank do not decrease with decreasing load and consequently it has a higher circulating current than the SRC. Moreover, an additional output inductor is required which adds volume to the converter. Similarly, the shortcoming of the SPRC is that it has larger footprint due to the extra capacitor (within *LCC* case) or inductor (within *LLC* case) employed. Hence, load resonant converters are rendered less attractive than the phase shifted full-bridge converter, and thus they are not considered any further in this study.

C. Dual-Active Bridge Converter

Apart from resonant converters, non-resonant soft-switching topologies can also enable operation with ZVS or ZCS over a limited range, leading to a drastic reduction of the switching losses compared with hard switching topologies. The dual-active bridge (DAB) converter which is shown in Fig.3.10 utilises transformer leakage inductance as the energy transfer element, which eliminates the output inductor compared with the conventional full-bridge DC/DC converter. In addition, they achieve ZVS operation over a reasonable operating range without additional resonant circuits by incorporating the transformer leakage inductance, thus achieving high efficiency [45]. However, the lack of output filter inductance in this cases greatly increases the required ripple current carrying requirements of the output capacitance.

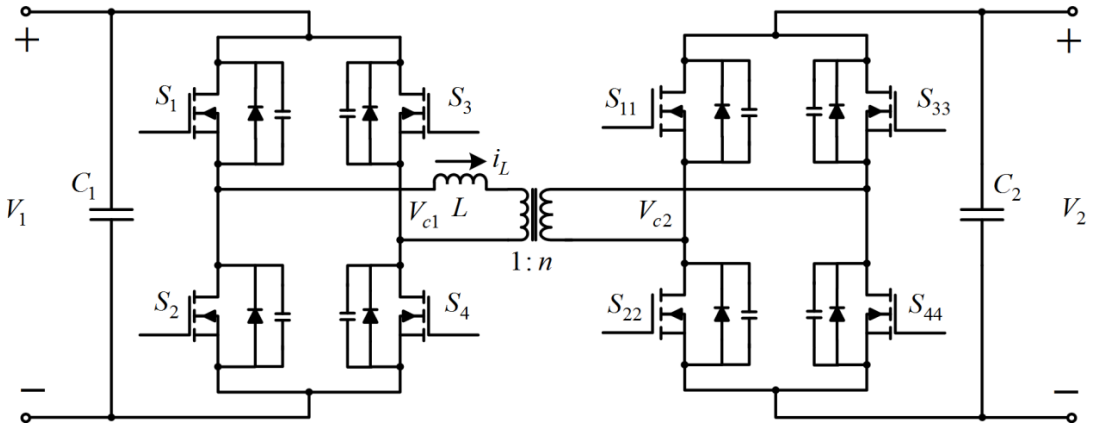


Fig.3.10: Dual-active bridge converter

To address the increasing needs of bidirectional energy transfer systems and energy storage systems, interest in this bidirectional DC/DC converter has increased. The

DAB converter consisting of two active bridges interfaced by a high-frequency isolation transformer, one operating in rectification AC/DC mode and the other operating in inversion DC/AC mode, has been introduced. Apart from the capability of buck-boost operation, the DAB converter enables bidirectional power flow by phase shifting the high-frequency resonant transition square waves from each bridge to change the direction and magnitude of the inductor current. The transmission power of the DAB converer can be derived as (3.2).

$$\begin{cases} P_{\sin e} = \dfrac{V_{rms1}V_{rms2}}{2\pi f_s L}\sin\varphi \\ P_{square} = \dfrac{V_1 V_2}{2\pi^2 f_s nL}\varphi(\pi-\varphi) \end{cases} \tag{3.2}$$

where V_{rms1} and V_{rms2} are the root mean square (RMS) of sinusoical waves, V_1 and V_2 are the primary and secondary voltages, n is the transformer turns ratio, φ is the phase shift between AC voltages which determines the direction of power flow, and L is the leakage inductance of the transformer which determines the maximum amount of transferable power for a given switching frequency.

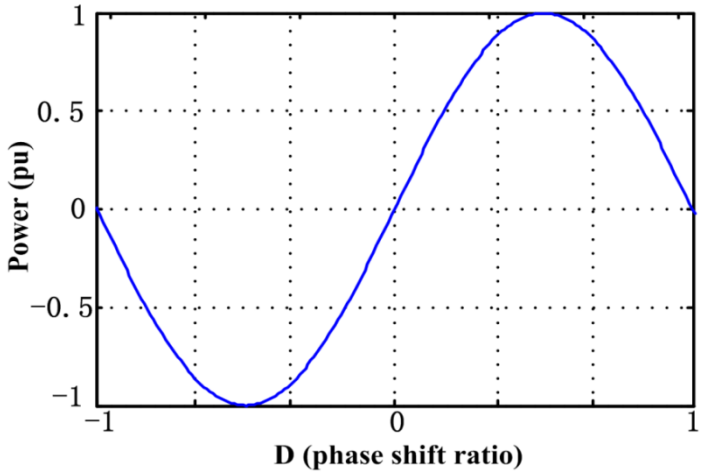


Fig.3.11: Transmission power characterisation for SPS control

In respect of the control strategy, different modulation schemes are proposed including single-phase-shift (SPS) control, extended-phase-shift (EPS) control, dual-phase-shift (DPS) control and triple-phase-shift (TPS) control, etc. [49]. SPS control is discussed here due to the fact that it is the most feasible strategy in the view of its simple implementation. The transmission power characterisation of SPS control is shown in Fig.3.11, where $D=\varphi/\pi$ is the phase shift ratio. It can be seen that

transmission power curve is symmetric, and that zero and maximum power transmission are achieved at D=0 and D=0.5 respectively. With the symmetric circuit structure, converter efficiency is independent of the actual power transfer direction.

Fig.3.12 illustrates the PWM waveforms for SPS control, where S_1-S_4 and S_{11}-S_{44} are the square-wave gate signals for the eight switches, V_{C1} and V_{C2} are the equivalent AC output voltages from two bridges, and i_L is the inductor current. Through adjusting the phase-shift angle, the power flow direction and magnitude can simply be controlled through simple-fixed frequency phase-shifting control. However, it would be problematic due to the circulating power introduced by the phase-shift modulation when the voltage amplitudes of the two sides of the transformer are not matched. In addition, the converter cannot achieve ZVS across the whole power range, particularly under light load conditions [45].

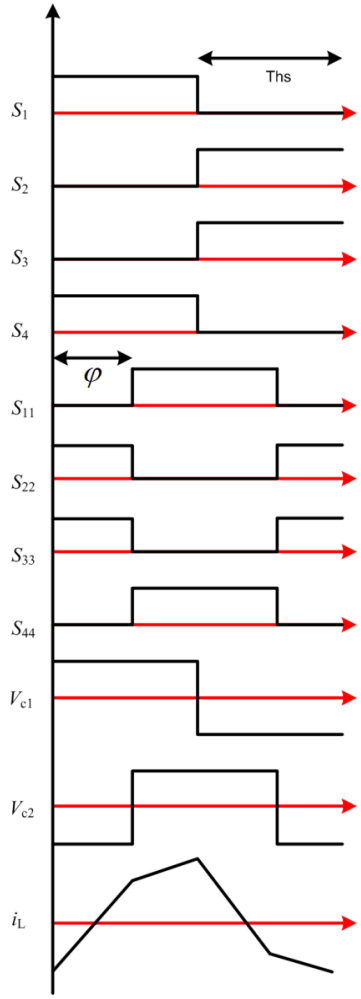


Fig.3.12: SPS control for DAB converter

Although bidirectional power flow capability is not required in the proposed application, some active switches can be replaced with diodes. In addition, concerning storage systems, distribution grids and wind turbine black-start, a DAB converter is considered as a potential candidate because of its advantages of bidirectional power transfer capability, high power density, high gain ability, and inherent soft-switching feasibility [49].

Several topologies are discussed with their benefits and shortcomings. Based on these findings, the phase shifted full-bridge converter and DAB converter are considered the most promising with respect to high input-to-output ratio, high efficiency and high power density. The phase shifted full-bridge converter is adopted as the module topology in the parallel-series connected modular converter in Chapter 4 and Chapter 5. A parallel-series connected modular DC/DC converter based on a DAB module is presented in Chapter 6. The following section will further discuss the choices of transformer core.

3.2.2 Choices of Transformer Core

In the modular DC/DC converter being studied, it is possible to replace the line-frequency transformer with a medium- or high-frequency transformer as it reduces the size and weight of the magnetics, leading to a reduced size of the whole power conversion system. Therefore, the medium- or high-frequency transformer is the key component to address the high-power DC/DC converter. Considering the whole transformer, magnetic core materials are considered one of the most critical components that affect the DC/DC converter's efficiency, size and dynamic response [50]. Therefore, high performance core material is required in order to maximise the performance of the converter.

Ferrites are usually employed in the high-frequency transformer core owing to the features of low residual flux and high resistivity. For operation frequency above 100 kHz, ferrites are normally the only choice available. However, the issues of low flux saturation, Curie temperature and magnetic permeability may result in large size, unstable operation states and poor temperature properties [49]. On the contrary, nanocrystalline starts to be commercialised as one of the most promising magnetics materials.

Table 3.2: Characteristic comparisons of nanocrystalline alloy and ferrites

Parameter	*Nanocrystalline alloy*	*Ferrite*
Saturation magnetic flux density Bs (T)	1.2	0.2-0.4
Residual magnetic flux density Br (T)	<0.2	0.2
Iron loss (20kHz/0.2T) (W/Kg)	<3.4	7.5
Magnetic permeability	>20000	2000
Coercive force Hc (A/m)	<1.6	6
Curie temperature (°C)	570	<200

A 500 kVA prototype transformer has been successfully tested with 8 kHz operating frequency [51]. The weight of the prototype is only 18 kg and the stray inductance is 2.3 μH. A high-density transformer using a nanocrystalline core developed for a 30 kW, 200 kHz resonant converter has been proposed [52]. Nanocrystalline material has been applied to a 1 MW bidirectional DC/DC converter operating at 20 kHz [53]. From the comparisons in Table 3.2, it can be seen that nanocrystalline alloy called NANOPERM with higher saturation flux density, lower loss density, and higher Curie temperature has shown promise for significantly improved efficiency and power density for high-power, high-frequency applications. Therefore, the nanocrystalline alloy core is chosen in this study.

3.3 Summary

DC/DC converters that can facilitate DC/DC conversion in offshore DC collection network are still under development. Given the proposed parallel-series connected modular DC/DC converter, this chapter firstly introduces the control strategies applicable to parallel-series connections. From these assessments, a converter with IPOS connection that is most suited to the proposed application is selected. Secondly, the phase shifted full-bridge converter and the DAB converter are selected as promising module topologies after assessing several high-power isolated DC/DC converters. Simulation and experimental results of the proposed converters are presented in the following chapters. Finally, nanocrystalline alloy and ferrite are assessed based on their suitability for medium-power and medium-frequency

transformers, and nanocrystalline alloy is chosen based on its higher saturation flux density, lower loss density, and higher Curie temperature.

3.4 Chapter Reference

[1] J. W. van der Merwe and H. du T Mouton, "An investigation of the natural balancing mechanisms of modular input-series-output-series DC-DC converters," in Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, pp. 817-822, 2010.

[2] Y. Lian, D. Holliday and S. Finney, "Modular input-parallel-output-series DC/DC converter control with fault detection and redundancy," in AC and DC Power Transmission, 11th IET International Conference on, Birmingham, pp. 1-8, 2015.

[3] L. Yiqing and S. J. Finney, "DC collection networks for offshore generation," in Renewable Power Generation Conference (RPG 2013), 2nd IET, Beijing, pp. 1-4, 2013.

[4] L. Shiguo, Y. Zhihong, L. Ray-Lee and F. C. Lee, "A classification and evaluation of paralleling methods for power supply modules," in Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE, pp. 901-908 vol.2, 1999.

[5] R. Giri, V. Choudhary, R. Ayyanar and N. Mohan, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," Industry Applications, IEEE Transactions on, vol. 42, no. 4, pp. 1101-1111, 2006.

[6] Grbovic, x and P. J., "Master/Slave Control of Input-Series- and Output-Parallel-Connected Converters: Concept for Low-Cost High-Voltage Auxiliary Power Supplies," Power Electronics, IEEE Transactions on, vol. 24, no. 2, pp. 316-328, 2009.

[7] R. Giri, R. Ayyanar and E. Ledezma, "Input-series and output-series connected modular DC-DC converters with active input voltage and output voltage sharing," in Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE, pp. 1751-1756 Vol.3, 2004.

[8] P. S. Shenoy and P. T. Krein, "Local control of multiple module dc-dc converters," in Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on, Boulder, CO, pp. 1-6, 2010.

[9] K. Siri, C. Q. Lee and T. F. Wu, "Current distribution control for parallel connected converters. I," Aerospace and Electronic Systems, IEEE Transactions on, vol. 28, no. 3, pp. 829-840, 1992.

[10] Y. Lian, G. P. Adam, D. Holliday and S. J. Finney, "Active power sharing in input-series-input-parallel output-series connected DC/DC converters," in Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE, Charlotte, NC, pp. 2790-2797, 2015.

[11] C. Wu, R. Xinbo, Y. Hong and C. K. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," Power Electronics, IEEE Transactions on, vol. 24, no. 6, pp. 1463-1474, 2009.

[12] R. Xinbo, C. Wu, C. Lulu, C. K. Tse, Y. Hong and Z. Tao, "Control Strategy for Input-Series & Output-Parallel Converters," Industrial Electronics, IEEE Transactions on, vol. 56, no. 4, pp. 1174-1185, 2009.

[13] A. A. Aboushady, "Design, Analysis and Modelling of Modular Medium-Voltage DC/DC Converter Based Systems," PhD thesis, Departement of Electronics and Electrical Engineering, University of Strathclyde, Glasgow, 2012.

[14] F. Haifeng and L. Hui, "High-Frequency Transformer Isolated Bidirectional DC&DC Converter Modules With High Efficiency Over Wide Load Range for 20 kVA Solid-State Transformer," Power Electronics, IEEE Transactions on, vol. 26, no. 12, pp. 3599-3608, 2011.

[15] J. W. Kimball, J. T. Mossoba and P. T. Krein, "A Stabilizing, High-Performance Controller for Input Series-Output Parallel Converters," Power Electronics, IEEE Transactions on, vol. 23, no. 3, pp. 1416-1427, 2008.

[16] T. Yeh, S. de Haan and J. A. Ferreira, "A modular DC-DC converter with collapsible input voltage of series connected modules without additional bypass switch," in Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, Denver, CO, pp. 2341-2346, 2013.

[17] S. Jianjiang, L. Jie and H. Xiangning, "Common-Duty-Ratio Control of Input-Series Output-Parallel Connected Phase-shift Full-Bridge DC/DC Converter Modules," Power Electronics, IEEE Transactions on, vol. 26, no. 11, pp. 3318-3329, 2011.

[18] P. J. Grbovic, "Master/Slave Control of Input-Series- and Output-Parallel-Connected Converters: Concept for Low-Cost High-Voltage Auxiliary Power Supplies," Power Electronics, IEEE Transactions on, vol. 24, no. 2, pp. 316-328, 2009.

[19] S. Deshang, D. Kai and L. Xiaozhong, "Duty Cycle Exchanging Control for Input-Series-Output-Series Connected Two PS-FB DC-DC Converters," Power Electronics, IEEE Transactions on, vol. 27, no. 3, pp. 1490-1501, 2012.

[20] R. Ayyanar, R. Giri and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," Power Electronics, IEEE Transactions on, vol. 19, no. 6, pp. 1462-1473, 2004.

[21] S. Deshang, G. Zhiqiang and L. Xiaozhong, "Cross-Feedback Output-Current-Sharing Control for Input-Series-Output-Parallel Modular DC&DC Converters," Power Electronics, IEEE Transactions on, vol. 25, no. 11, pp. 2762-2771, 2010.

[22] F. Tianzhi, R. Xinbo and C. K. Tse, "Control Strategy to Achieve Input and Output Voltage Sharing for Input-Series&Output-Series-Connected Inverter Systems," Power Electronics, IEEE Transactions on, vol. 25, no. 6, pp. 1585-1596, 2010.

[23] C. Wu and W. Guangjiang, "Decentralized Voltage-Sharing Control Strategy for Fully Modular Input-Series&Output-Series System With Improved Voltage Regulation," Industrial Electronics, IEEE Transactions on, vol. 62, no. 5, pp. 2777-2787, 2015.

[24] V. Choudhary, E. Ledezma, R. Ayyanar and R. M. Button, "Fault Tolerant Circuit Topology and Control Method for Input-Series and Output-Parallel

Modular DC-DC Converters," Power Electronics, IEEE Transactions on, vol. 23, no. 1, pp. 402-411, 2008.

[25] S. Jianjiang, Z. Lingbing and H. Xiangning, "Common-Duty-Ratio Control of Input-Parallel Output-Parallel (IPOP) Connected DC&DC Converter Modules With Automatic Sharing of Currents," Power Electronics, IEEE Transactions on, vol. 27, no. 7, pp. 3277-3291, 2012.

[26] V. J. Thottuvelil and G. C. Verghese, "Stability analysis of paralleled DC/DC converters with active current sharing," in Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE, pp. 1080-1086 vol.2, 1996.

[27] H. Yuehui and C. K. Tse, "Circuit Theoretic Classification of Parallel Connected DC–DC Converters," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 54, no. 5, pp. 1099-1108, 2007.

[28] K. Jeong-il, R. Chung-Wook, M. Gun-Woo and Y. Myung-Joong, "Phase-shifted parallel-input/series-output dual converter for high-power step-up applications," Industrial Electronics, IEEE Transactions on, vol. 49, no. 3, pp. 649-652, 2002.

[29] K. Siri, M. Willhoff and K. Conner, "Uniform Voltage Distribution Control for Series Connected DC&DC Converters," Power Electronics, IEEE Transactions on, vol. 22, no. 4, pp. 1269-1279, 2007.

[30] K. Siri, M. Willhoff and K. Conner, "Uniform Voltage Distribution Control for Series Connected DC&DC Converters," Power Electronics, IEEE Transactions on, vol. 22, no. 4, pp. 1269-1279, 2007.

[31] S. N. Manias and G. Kostakis, "Modular DC-DC convertor for high-output voltage applications," Electric Power Applications, IEE Proceedings B, vol. 140, no. 2, pp. 97-102, 1993.

[32] W. Linbing, "Input-Parallel and Output-Series Modular DC-DC Converters with One Common Filter," in EUROCON, 2007. The International Conference on "Computer as a Tool", Warsaw, pp. 1398-1402, 2007.

[33] S. Chunwei, R. Zhao, L. Wangqing and Z. Zheng, "A novel control strategy for input-parallel-output-series inverter system," in Electrical Machines and Systems (ICEMS), 2011 International Conference on, Beijing, pp. 1-5, 2011.

[34] J. W. Kolar, T. Friedli, F. Krismer, A. Looser, M. Schweizer, P. Steimer and J. Bevirt, "Conceptualization and multi-objective optimization of the electric system of an Airborne Wind Turbine," in Industrial Electronics (ISIE), 2011 IEEE International Symposium on, pp. 32-55, 2011.

[35] J. Adhikari, A. K. Rathore and S. K. Panda, "Modular interleaved ZVS current fed isolated DC-DC converter for harvesting high altitude wind power," in Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE, pp. 7187-7192, 2013.

[36] G. Ling, K. Yueping, J. Ke and S. Zhiyuan, "Input-parallel output-series isolated DC-DC converter for PV generation system," in Power Electronics for Distributed Generation Systems (PEDG), 2013 4th IEEE International Symposium on, pp. 1-8, 2013.

[37] K. Sano and M. Takasaki, "A boost conversion system consisting of multiple DC-DC converter modules for interfacing wind farms and HVDC transmission," in Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, Denver, CO, pp. 2613-2618, 2013.

[38] R. L. Steigerwald, R. W. De Doncker and M. H. Kheraluwala, "A comparison of high-power DC-DC soft-switched converter topologies," Industry Applications, IEEE Transactions on, vol. 32, no. 5, pp. 1139-1145, 1996.

[39] H. Xiucheng, W. Jianfeng, Z. Junming and Q. Zhaoming, "A hybrid driving scheme for full-bridge synchronous rectified LLC resonant DC/DC converter," in Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, pp. 579-584, 2011.

[40] J. Liu, J. Mookken and K. L. Wong, "Highly Efficient, and Compact ZVS Resonant Full Bridge Converter using 1200V SiC MOSFETs," in PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of, pp. 1-8, 2014.

[41] G. Yilei, L. Zhengyu, H. Lijun, Q. Zhaoming and H. Guisong, "Three-level LLC series resonant DC/DC converter," Power Electronics, IEEE Transactions on, vol. 20, no. 4, pp. 781-789, 2005.

[42] J. A. Ferreira, "The zero voltage switching partial series resonant converter," Industry Applications, IEEE Transactions on, vol. 31, no. 4, pp. 879-886, 1995.

[43] Y. Ting, "DC-DC Converters with a Wide Load Range and a Wide Input-Voltage Range," RWTH Aachen University, Duitsland, 2015.

[44] A. J. Gilbert, C. M. Bingham, D. A. Stone and M. P. Foster, "Normalized Analysis and Design of LCC Resonant Converters," Power Electronics, IEEE Transactions on, vol. 22, no. 6, pp. 2386-2402, 2007.

[45] K. D. Hoang and J. Wang, "Design optimization of high frequency transformer for dual active bridge DC-DC converter," in Electrical Machines (ICEM), 2012 XXth International Conference on, pp. 2311-2317, 2012.

[46] R. W. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," Industry Applications, IEEE Transactions on, vol. 27, no. 1, pp. 63-73, 1991.

[47] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," Industry Applications, IEEE Transactions on, vol. 28, no. 6, pp. 1294-1301, 1992.

[48] M. H. Kheraluwala and R. W. De Doncker, "Single phase unity power factor control for dual active bridge converter," in Industry Applications Society Annual Meeting, 1993., Conference Record of the 1993 IEEE, pp. 909-916 vol.2, 1993.

[49] Z. Biao, S. Qiang, L. Wenhua and S. Yandong, "Overview of Dual-Active-Bridge Isolated Bidirectional DC&DC Converter for High-Frequency-Link Power-Conversion System," Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4091-4106, 2014.

[50] O. A. Hassan, C. Klumpner and G. Asher, "Design considerations for core material selection and operating modes for a high frequency transformer used in an isolated DC/DC converter," in Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1-11, 2011.

[51] M. Steiner and H. Reinold, “Medium frequency topology in railway applications,” in Power Electronics and Applications, 2007 European Conference on, pp. 1-10, 2007.

[52] S. Wei, W. Fei, D. Boroyevich and C. W. Tipton, “High-Density Nanocrystalline Core Transformer for High-Power High-Frequency Resonant Converter,” Industry Applications, IEEE Transactions on, vol. 44, no. 1, pp. 213-222, 2008.

[53] G. Ortiz, J. Biela and J. W. Kolar, “Optimized design of medium frequency transformers with high isolation requirements,” in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, pp. 631-638, 2010.

Chapter 4: IPOS Connected Modular DC/DC Converter

This chapter presents a control strategy based on a ‘master-slave’ scheme that enables power sharing between modules in an input-parallel output-series (IPOS) connected modular DC/DC converter where there are mismatches between module components, and achieves fault-tolerant operation during internal module failure. First, this chapter introduces the IPOS connected modular DC/DC converter and then power sharing issues in the proposed converter are discussed. Following that, control topology design, including small-signal modelling, large-signal modelling and the proposed power sharing strategy, is addressed. Power sharing performance between modules with mismatched components, and (n+1) redundancy in the event that the master module is faulted are compared with those of a widely-used control approach. Finally, both simulation and experimental results are presented to test the viability of the proposed control scheme.

4.1 IPOS Connection Background

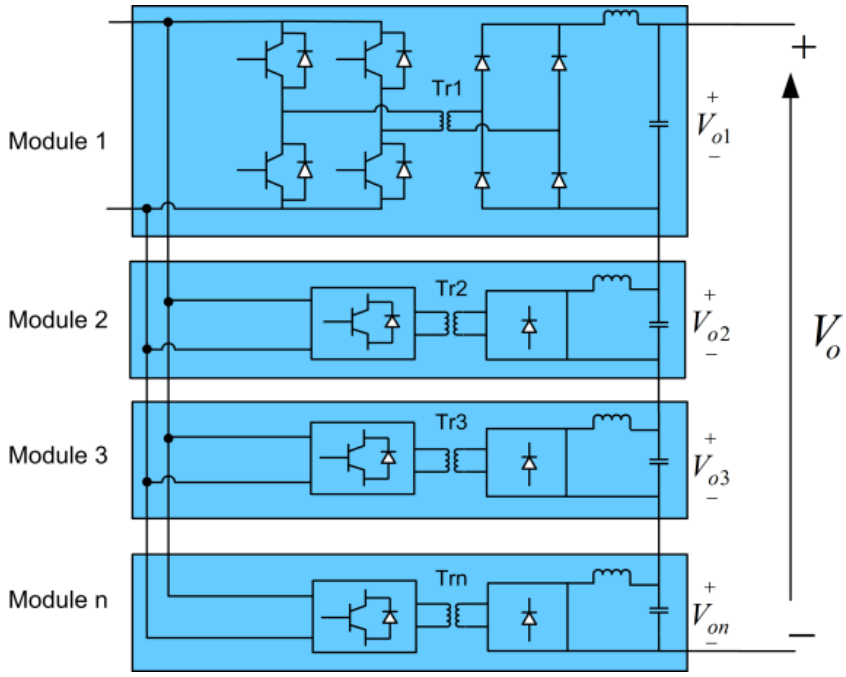


Fig.4.1: IPOS converter topology with full-bridge DC/DC modules

Parallel-series architectures can be classified into four categories based on their connection. These categories are input-parallel output-parallel (IPOP), input-parallel output-series (IPOS), input-series output-parallel (ISOP) and input-series output-series (ISOS) [1]. It has been stated in Chapter 3 that IPOS connection is most suitable for high input-to-output conversion ratios, as required for interfacing wind turbine generators to a medium-voltage DC collection network. Input-parallel connection improves power handling capability, dynamic performance and enables fault-tolerant operation [2], whilst the output-series connection of the high-voltage side has the capability of supporting the collection network voltage and reducing voltage stress per device, thus avoiding the need for high-voltage diodes with short recovery time.

Fig.4.1 represents a generic IPOS connected modular DC/DC converter with *n* phase shifted full-bridge modules. In contrast to the topology where a single converter manages all the power, the power is equally shared by all the modules in the converter, thereby reducing thermal and electrical stresses on the switching devices and passive components. In addition, connection of multiple low-power rating

modules provides an excellent solution, with improved robustness and the possibility for fault-tolerant operation as a result of (n+k) designed redundancy. Reduced filter size can be achieved due to the interleaved control. Moreover, the use of power electronic building blocks (PEBB) reduces production and deployment costs [1, 3].

4.2 Power Sharing Issue with IPOS Connected Modular DC/DC Converter

In typical applications, modules are not identical, having inherent component mismatches such as differences in transformer coupling coefficient, capacitances and semiconductor devices nonlinearities, and these may cause unequal power distribution between the modules. System reliability may suffer because the modules that contribute a greater portion of the power are thermally overstressed [4, 5]. Therefore, reliable operation of the IPOS connected DC/DC converter requires a control mechanism that ensures equal power sharing amongst the constituent modules under all conditions, including cases when module components have noticeable mismatches and internal module failure.

The efficiency of each module is assumed to be 100% and there are n modules in total. The relationship between input and output power can be obtained for each module as (4.1).

$$\begin{cases} V_{in} I_{in1} = V_{o1} I_o \\ V_{in} I_{in1} = V_{o2} I_o \\ \quad \cdot \ \cdot \ \cdot \\ V_{in} I_{inn} = V_{on} I_o \end{cases} \tag{4.1}$$

where V_{in} is the DC input voltage, I_{in1}, I_{in2},…, I_{inn} are the module input currents, V_{o1}, V_{o2},…, V_{on} are the module output voltages, and I_o is the load current. In the steady-state condition, the average filter capacitor current is zero, and therefore output filter inductor currents are identical except for a small ripple component. If output voltage sharing (OVS) is achieved, then, V_{o1}=V_{o2}=…=V_{on}. Substituting this result for OVS into (4.1) gives (4.2).

$$I_{in1} = I_{in2} = ... = I_{inn} \tag{4.2}$$

It should be noted that input current sharing (ICS) is automatically achieved as long as OVS is achieved. Alternatively, if all modules share the same input current, then output voltage sharing is also achieved.

This study proposes a 'master-slave' control scheme using OVS control to obtain power balancing between the modules. First, the response of the converter to small perturbations is introduced so that the linear small-signal model for the proposed converter can be deduced.

4.3 Small-Signal Modelling for IPOS Connected Two-module Converter

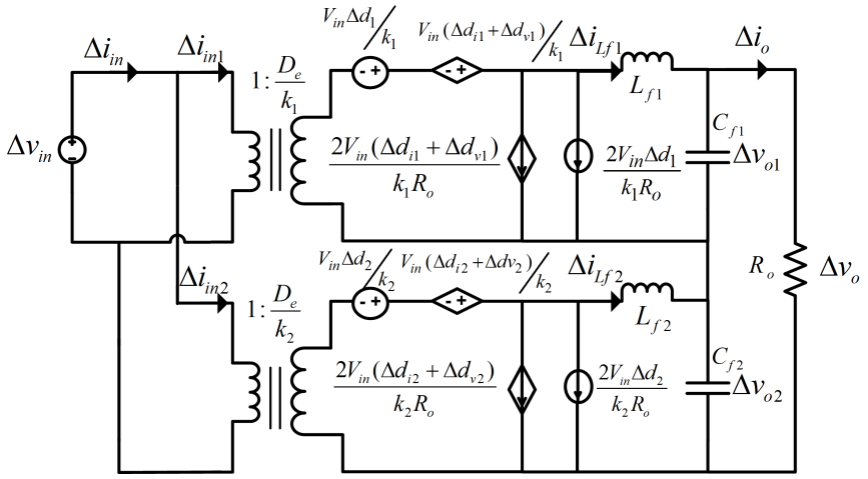


Fig.4.2: Small-signal equivalent circuit of the IPOS connected 2-module converter

The small-signal model of the proposed converter is deduced by linearising about a given steady-state operating point, and used to design the control scheme. The small-signal equivalent circuit of the IPOS connected converter with two phase-shift full-bridge modules shown in Fig.4.2 builds on a single module converter model [6], where k_1 and k_2 are the transformer turns-ratios, D_e is the effective duty cycle per module, and L_{f1}, L_{f2}, C_{f1} and C_{f2} are the filter inductances and capacitances for modules 1 and 2 respectively. Input voltage perturbation is represented by Δv_{in}, input current perturbations for the two modules are Δi_{in1} and Δi_{in2} respectively, and filter inductor current and capacitor voltage perturbations are represented by Δi_{lf1}, Δi_{lf2}, Δv_{o1} and Δv_{o2} respectively. Δd_1 and Δd_2 are duty cycle perturbations, and Δd_{v1}, Δd_{v2},

Δd_{i1} and Δd_{i2} respectively represent duty cycle perturbations due to input voltage and output current as defined in (4.3),

$$\begin{cases} \Delta d_{v1} = \Delta d_{v2} = \dfrac{8L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{in} \\ \Delta d_{i1} = -\dfrac{4L_r f_s}{kV_{in}} \Delta i_{lf1} \\ \Delta d_{i2} = -\dfrac{4L_r f_s}{kV_{in}} \Delta i_{lf2} \end{cases} \tag{4.3}$$

where L_r is the transformer leakage inductance. To reduce the complexity of the small-signal transfer functions based on the feature of modularity [7], it is assumed that two modules have the same effective duty cycle, transformer turns-ratios, and capacitor and inductor values, i.e. $k_1=k_2=k$, $L_{f1}=L_{f2}=L_f$, and $C_{f1}=C_{f2}=C_f$. From Fig.4.2, KVL and KCL equations of the converter are obtained as (4.4).

$$\begin{cases} \dfrac{D_e \Delta v_{in}}{k} + \dfrac{V_{in}}{k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) = sL_f \Delta i_{lf1} + \Delta v_{o1} \\ \dfrac{D_e \Delta v_{in}}{k} + \dfrac{V_{in}}{k}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = sL_f \Delta i_{lf2} + \Delta v_{o2} \\ \dfrac{k}{D_e}\Delta i_{in1} = \dfrac{2V_{in}}{kR_o}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) + \Delta i_{lf1} \\ \dfrac{k}{D_e}\Delta i_{in2} = \dfrac{2V_{in}}{kR_o}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) + \Delta i_{lf2} \end{cases} \tag{4.4}$$

Module voltage perturbations are given as (4.5), which highlights the interaction between modules.

$$\begin{cases} \Delta v_{o1} = \dfrac{1}{sC_f}\left(\Delta i_{lf1} - \dfrac{\Delta v_{o1} + \Delta v_{o2}}{R_o}\right) \\ \Delta v_{o2} = \dfrac{1}{sC_f}\left(\Delta i_{lf2} - \dfrac{\Delta v_{o1} + \Delta v_{o2}}{R_o}\right) \end{cases} \tag{4.5}$$

This can be rewritten as (4.6).

$$\begin{cases} \Delta v_{o1} = \dfrac{1 + sC_f R_o}{s^2 {C_f}^2 R_o + 2sC_f} \Delta i_{lf1} - \dfrac{1}{s^2 {C_f}^2 R_o + 2sC_f} \Delta i_{lf2} \\ \Delta v_{o2} = -\dfrac{1}{s^2 {C_f}^2 R_o + 2sC_f} \Delta i_{lf1} + \dfrac{1 + sC_f R_o}{s^2 {C_f}^2 R_o + 2sC_f} \Delta i_{lf2} \end{cases} \tag{4.6}$$

Rearranging (4.6), the transfer function between module output voltages and currents can be obtained in the matrix form (4.7),

$$\begin{bmatrix} \Delta v_{o1} \\ \Delta v_{o2} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} \tag{4.7}$$

where

$$\begin{cases} G_{11} = G_{22} = \dfrac{1 + sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} \\ G_{12} = G_{21} = -\dfrac{1}{s^2 C_f{}^2 R_o + 2sC_f} \end{cases} \tag{4.8}$$

Addition of the first two equations in (4.4) gives (4.9).

$$\begin{aligned} &\frac{2D_e \Delta v_{in}}{k} + \frac{V_{in}}{k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1} + \Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) \\ &= sL_f \Delta i_{lf1} + \Delta v_{o1} + sL_f \Delta i_{lf2} + \Delta v_{o2} \end{aligned} \tag{4.9}$$

Assuming that $\Delta v_{in}=0$, and $\Delta d_k=0$ (k=1,2 and $k\neq j$), the relationship between load voltage and duty cycle, derived from the (4.5) and (4.9), is used to design the system output voltage controller.

$$G_{ovd} = \frac{\Delta v_o}{\Delta d_j} = \frac{V_{in}/k}{L_f C_f s^2 + [\dfrac{2L_f}{R_o} + \dfrac{4L_r f_s}{k^2} C_f]s + \dfrac{8L_r f_s}{k^2 R_o} + 1} \tag{4.10}$$

Substituting (4.3) and (4.6) into (4.10), assuming $\Delta v_{in}=0$, yields (4.11).

$$\begin{cases} \dfrac{V_{in}}{k}\Delta d_1 = [L_f s + \dfrac{1 + C_f R_o s}{C_f{}^2 R_o s^2 + 2C_f s} + \dfrac{4L_r f_s}{k^2}]\Delta i_{lf1} - \dfrac{1}{C_f{}^2 R_o s^2 + 2C_f s}\Delta i_{lf2} \\ \dfrac{V_{in}}{k}\Delta d_2 = -\dfrac{1}{C_f{}^2 R_o s^2 + 2C_f s}\Delta i_{lf1} + [L_f s + \dfrac{1 + C_f R_o s}{C_f{}^2 R_o s^2 + 2C_f s} + \dfrac{4L_r f_s}{k^2}]\Delta i_{lf2} \end{cases} \tag{4.11}$$

Rearranging (4.11), the relationship between duty cycles and inductor currents can be represented as (4.12), highlighting that the current controllers for each module are designed independently,

$$\begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix} \tag{4.12}$$

where

$$\begin{cases} g_{11} = g_{22} = \dfrac{\mathrm{V}_{in}(sL_f + \dfrac{1+sC_fR_o}{s^2{C_f}^2R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2})}{k(sL_f + \dfrac{R_o}{s^2{C_f}^2R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}) \times (sL_f + \dfrac{2+sC_fR_o}{s^2{C_f}^2R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2})} \\ g_{12} = g_{21} = -\dfrac{\mathrm{V}_{in}(\dfrac{-1}{s^2{C_f}^2R_o + 2sC_f})}{k(sL_f + \dfrac{R_o}{s^2{C_f}^2R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}) \times (sL_f + \dfrac{2+sC_fR_o}{s^2{C_f}^2R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2})} \end{cases}$$

The transfer function between module output voltage and duty cycle is given in (4.13) and provides the basis for design of the output voltage sharing controller.

$$\begin{aligned} \begin{bmatrix} \Delta v_{o1} \\ \Delta v_{o2} \end{bmatrix} &= \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} \\ &= \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix} \\ &= \begin{bmatrix} G_{11}g_{11} + G_{12}g_{21} & G_{11}g_{12} + G_{12}g_{22} \\ G_{21}g_{11} + G_{22}g_{21} & G_{21}g_{12} + G_{22}g_{22} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix} \end{aligned} \tag{4.13}$$

The transfer functions which are obtained from the small-signal model are used to select initial gains for inner current and outer voltage controllers. These gains are further optimised using time-domain simulation to ensure acceptable performance is achieved over the full operating range (from no load to full load, including during transients and reconfiguration of modules). This is to remove the dependency of controller performance on the quiescent point, which is the main limitation of model based controller designs that use linearised system models.

A new control strategy that aims to cope with substantial parameter mismatches between modules, and which track its DC output voltage reference without exposing the converter to the risk of parameter uncertainty and exogenous disturbance, is presented in the following section.

4.4 Novel Control Strategy in Normal Operation

In the master-slave control method, the master module is responsible for load regulation whilst the slaves ensure equal current or voltage sharing amongst the modules. The proposed 'master-slave' control strategy for the IPOS DC/DC converter with n modules that facilitates power sharing amongst the modules with mismatched components in normal operation consists of three loops: the master module to produce control signal Δi (current command) to control the output voltage, (n-1) slave modules to produce the voltage balancing current reference quantities Δi_i (i=1,2,…,n-1) by OVS control, and individual inner current loops for each module. Details of the design of the proposed novel 'master-slave' control strategy are given in the following sections.

4.4.1 Output Voltage Control

The outer control loop of the IPOS DC/DC converter acts to regulate the total output voltage achieved by the constituent modules which must operate as a single composite converter. However, DC/DC converters are inherently nonlinear systems whose behaviour is set by circuit parameters which are subject to measurement uncertainty and variation due to ageing and thermal effects. Established linear control techniques, such as PI control, provide a simple implementation for the output voltage controller. However, this approach may limit converter performance. Alternatively, nonlinear techniques can be employed which have the capability of obtaining a more accurate representation of the system dynamics, and which can provide robust response to parameter variations and enhanced transient responses [8].

Most of the nonlinear control laws are complex, which makes them difficult to apply, but the large-signal linear schemes have the advantage of reducing the proposed converter model to an equivalent output filter model which significantly simplifies the control design process [9, 10]. This study uses two nonlinear control algorithms, Lyapunov control and sliding-mode control, developed around the linearised large-signal model to control the output voltage. Simulation and experimental results for the proposed nonlinear controller and the PI controller are compared to show how the

nonlinear controllers are better defined and less subject to system uncertainty and variation, whilst a detailed stability and robustness analysis are presented as follows.

A. Linearisation Large-signal Scheme for IPOS DC/DC Converter

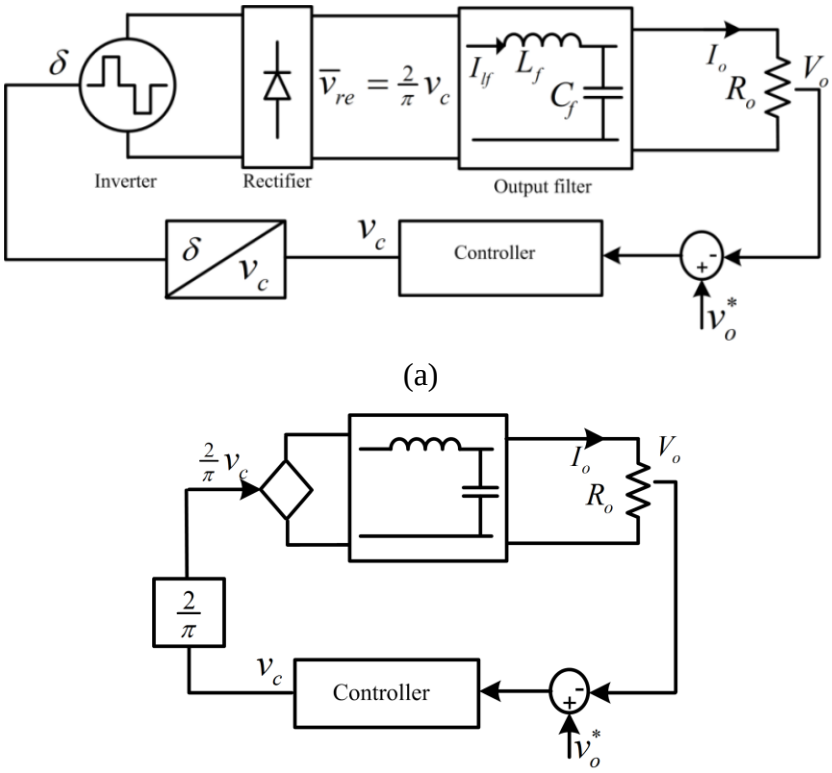


Fig.4.3: Closed-loop output voltage control configuration using the linearisation scheme (a) full structure and (b) reduced equivalent model for single unit [9]

A linearised scheme for the closed-loop output voltage control of a phase shifted full-bridge DC/DC converter is shown in Fig.4.3 (a), where L_f and C_f are the output inductance and capacitance relatively, I_{lf} denotes the inductance current, R_o represents the load, I_o is the output current, V_o is the output voltage, and v_o* is the output voltage reference, v_{re} is the rectifier output average voltage, the control input signal v_c is equal to the steady-state voltage before the rectifier, and δ is the phase shift angle for the converter phase shift PWM control [9]. The large-signal linear model is proven to be sufficient to represent the complete converter. Therefore, the reduced equivalent linearisation model which reduces a single full-bridge converter to an equivalent output filter model shown as Fig.4.3 (b) is used here to simplify the control design process.

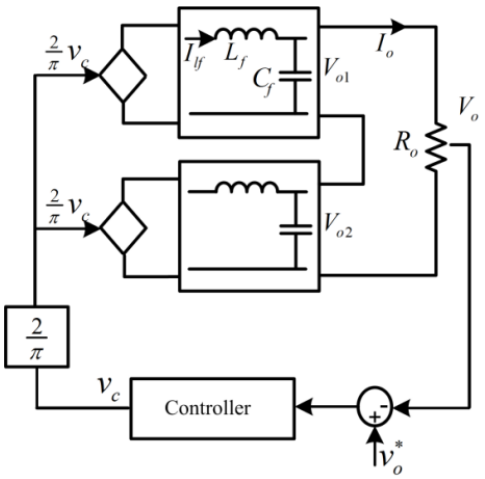


Fig.4.4: Reduced equivalent model for IPOS connected two-module system

The equivalent large-signal model for the IPOS connected 2-module system is shown in Fig.4.4, where the power stage of the proposed converter can be represented by the state equations (4.14) and (4.15) from the equivalent model. The control variable v_c is expressed in a second order transfer function of the output voltage as (4.16).

$$\frac{dI_{lf}}{dt} = \frac{1}{L_f}(\frac{2}{\pi}v_c - V_{o1}) = \frac{1}{L_f}(\frac{2}{\pi}v_c - \frac{1}{2}V_o) \tag{4.14}$$

$$\frac{dV_{o1}}{dt} = \frac{1}{2}\frac{dV_o}{dt} = \frac{1}{C_f}(I_{lf} - I_o) = \frac{1}{C_f}(I_{lf} - \frac{V_o}{R_o}) \tag{4.15}$$

$$\ddot{V}_o = \frac{2}{C_f}(-\frac{V_o}{2L_f} + \frac{2v_c}{\pi L_f} - \frac{\dot{V}_o}{R_o}) \tag{4.16}$$

From (4.17) and (4.18), it can be noted that the relative degree of the output voltage is two, due to the fact that this is the smallest number of differentiations of the variable with regards to time, so that the control input appears explicitly [11]. Hence, the desired closed-loop output voltage dynamics need to be controlled by a second order control law.

$$\frac{\partial}{\partial v_c}(\frac{dV_o}{dt}) = 0 \tag{4.17}$$

$$\frac{\partial}{\partial v_c}(\frac{d^2V_o}{dt^2}) \neq 0 \tag{4.18}$$

The control-to-output transfer function is therefore approximated by (4.19) for the IPOS converter in Fig.4.4.

$$G_{oc} = \frac{V_o(s)}{v_c(s)} \approx 2 * \frac{2}{\pi} \frac{V_o(s)}{\bar{v}_{re}(s)} = \frac{4}{\pi} \frac{1}{L_f C_f s^2 + 1} \tag{4.19}$$

The discussion regarding output voltage control that uses the Lyapunov stability law to ensure asymptotic stability of the system is presented in the following section.

B. Lyapunov Controller Design and Stability Criteria Analysis

Lyapunov stability theory has been a powerful tool in the stability analysis of nonlinear systems since its introduction in 1982 [12]. The objective is to use a control-Lyapunov candidate in the feedback loop, and to ensure that the derivative of positive definite Lyapunov function $v(x)$ is negative when choosing the control, which if satisfied means that for each state x, a control input u exists that will reduce $v(x)$. For example, considering a nonlinear system as (4.20)

$$\dot{x} = f_0(x) \tag{4.20}$$

where x is a n-dimensional state vector which belongs to the Euclidean space R^n. The system is specified by the vector field function $f_0 : D \rightarrow R^n$ which is continuous and has continuous first-order partial derivatives with respect to x on a domain $D \subset R_n$ into R_n [13]. Choose x=0 is the equilibrium point for (4.20), function $v(x)$ and its derivative can be obtained as (4.21) and (4.22) respectively.

$$v(0) = 0 \ \textit{and} \ v(D) > 0 \ \textit{in} \ D - \{0\} \tag{4.21}$$

$$\dot{v}(x) = grad(v(x)) \cdot f_0(x) \quad \textit{in} \ D \tag{4.22}$$

The stability of the system feedback can be tested by control-Lyapunov function, that is, a scalar smooth positive definite and radially unbounded function $v(x)$ for control system $\dot{x} = f(x,u)$ there exists $u(x)$ such that $\frac{\partial v(x)}{\partial x} f(x,u(x)) < 0 \ \forall x \neq 0$ [14]. Hence, Lyapunov function is stable, if

$$\dot{v}(x) = grad(v(x)) \cdot f_0(x) \leq 0 \quad \textit{in} \ D \tag{4.23}$$

Note that it should be negative definite for asymptotic stability.

For output voltage control, the objective is to minimise the output voltage error signal shown in (4.24).

$$e = v_o^* - V_o \tag{4.24}$$

A function $r = \dot{e} + ae$ is defined, where α is an arbitrary real constant, and a control-Lyapunov candidate $v(x)$ is then as (4.25), which is positive definite for all $v_o^* \neq 0$ and $V_o \neq 0$.

$$v = \frac{1}{2} r^2 \tag{4.25}$$

Taking the derivative of (4.25) with respect to time, which should be negative according to Lyapunov stability law, gives (4.26).

$$\dot{v} = r\dot{r} = (\dot{e} + ae)(\ddot{e} + a\dot{e}) < 0 \tag{4.26}$$

A negative derivative is defined as $\dot{v} = -kv$, where k is strictly a positive proportionality constant, thus, the derivative is negative definite for all system dynamics and the closed-loop system will be globally stable. Substituting this result into (4.25) and (4.26) yields (4.27).

$$\ddot{v}_o^* - \ddot{V}_o + \alpha\dot{e} = -\frac{1}{2} k(\dot{e} + \alpha e) \tag{4.27}$$

Substituting for dynamic $\ddot{V}_o$ from (4.16) into (4.27)gives (4.28).

$$(\ddot{v}_o^* + \frac{V_o}{L_f C_f} - \frac{4v_c}{\pi L_f C_f} + \frac{2\dot{V}_o}{C_f R_o} + \alpha\dot{e}) = -\frac{1}{2} k(\dot{e} + \alpha e) \tag{4.28}$$

Solving (4.28) for v_c yields the control law as (4.29).

$$v_c = \frac{L_f C_f \pi}{4} (\ddot{v}_o^* + \frac{V_o}{L_f C_f} + \frac{2\ddot{V}_o}{C_f R_o} + \alpha\dot{e} + \frac{k}{2} r) \tag{4.29}$$

Assuming v_o^* to be constant, $\dot{e} = -\dot{V}_o$ and $\dot{e} = -\ddot{V}_o$, substituting (4.16) to (4.29) yields (4.30).

$$v_c = \frac{\alpha k C_f L_f \pi}{8} (v_o^* - V_o) - \frac{C_f L_f \pi}{4} (\frac{k}{2} + \alpha - \frac{2}{C_f R_o}) \dot{V}_o + \frac{\pi}{4} V_o \tag{4.30}$$

Notice that the first and second terms of (4.30) represent a PD controller which is sufficient to ensure stability of the overall output voltage, where 'e' will decay to 0 as the system output voltage V_o converges to its reference desired set point. The term

$\pi V_o/4$ represents a feed-forward term to speed start-up and to help stabilise the controller. Therefore, (4.30) can be rewritten as (4.31),

$$v_c = k_p e + k_d \dot{e} + \frac{\pi}{4} V_o \tag{4.31}$$

where k_p is the proportion gain and k_d is the derivative gain.

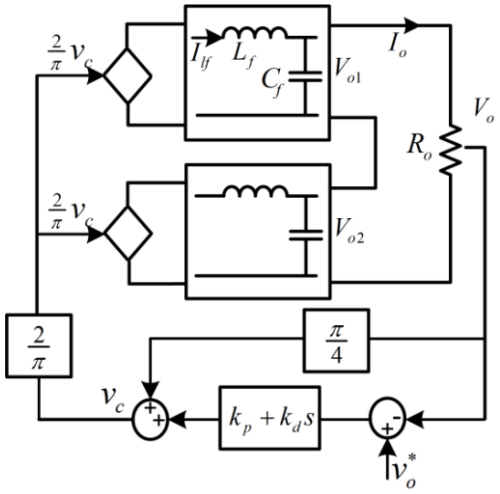


Fig.4.5: Lyapunov based PD output voltage controller

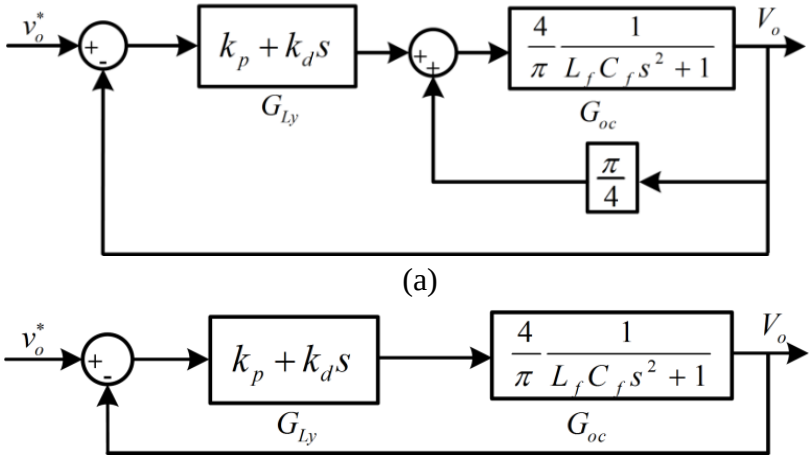


Fig.4.6: Closed-loop Lyapunov based controller (a) full structure (b) reduced equivalent control, omitting the feed-forward term

The reduced equivalent model of the closed-loop output voltage control realised by PD controller is shown in Fig.4.5. The control-to-output transfer function for the IPOS converter is given by (4.19), so the closed-loop system with a PD controller can be re-represented as Fig.4.6, where Fig.4.6 (a) illustrates the full structure of the

closed loop system and Fig.4.6 (b) shows the reduced equivalent control which excludes the feed-forward term.

However, the validity of the controller is established by its stability and robustness to parameter variations and transients. Hence, design of the controller experiences a set of design restrictions in terms of closed-loop stability and possible instability resulting from discretisation, which are presented in the following sub-sections.

- **Closed-Loop Stability**

From Fig.4.6 (b), the system open-loop, closed-loop and characteristic equations can be derived as (4.32)-(4.34) respectively.

$$G_{ol} = \frac{4}{\pi}\frac{k_p + k_d s}{L_f C_f s^2} \tag{4.32}$$

$$H_{cl} = \frac{4k_p + 4k_d s}{L_f C_f \pi s^2 + 4k_p + 4k_d s} \tag{4.33}$$

$$s^2 + \frac{4k_d}{L_f C_f \pi} s + \frac{4k_p}{L_f C_f \pi} = 0 \tag{4.34}$$

Equation (4.34) can be written in the general form (4.35),

$$s^2 + k_d a_1 s + k_p a_1 = 0 \tag{4.35}$$

where $a_1 = \frac{4}{L_f C_f \pi}$, and the coefficients of the polynomial are shown in Table 4.1.

Table 4.1: Polynomial table

Term	*Coefficient*
s^2	1
s^1	$k_d a_1$
s^0	$k_p a_1$

The Routh-Hurwitz stability criterion [15] clarifies that the system represented by the characteristic equation shown in (4.34) is stable if all its coefficients of the characteristic equation are positive. Therefore, with regard to closed-loop stability, the system is stable if proportional and derivative gains k_p and k_d are both positive as in (4.36).

$$k_p > 0,\ k_d > 0 \tag{4.36}$$

- **Discrete Time Domain Stability**

This continuous time DC/DC converter is controlled using a digital signal processing that operates in a discrete time environment. In the preceding discussion on closed-loop stability, the robustness criteria obtained are based on a continuous time system. Considering the practical implementation in DSP, system stability in the discrete time domain also limits the system criteria. Since it is impossible to obtain the exact discrete time modelling of the system, the Euler method [16] is employed to provide an approximate discrete model for the controller design. Three methods that can be used to obtain the discrete time approximation of a continuous time transfer funcation are the forward difference where Laplace operator *s* can be substituted by $s \to \frac{z-1}{T}$, the backward difference method with $s \to \frac{z-1}{Tz}$ and Tustin's approximation with $s \to \frac{2}{T}\frac{z-1}{z+1}$ [17]. However, only Tustin's method guarantees that stable controllers in the continuous mode are approximated by stable discrete controllers, and that unstable continuous controllers map to unstable discrete controllers. Thus, Tustin's approximation is applied and the resulting pulse transfer function of the system characteristic equation is given by (4.37),

$$D(z) = a_0 + a_1 z + a_2 z^2 \tag{4.37}$$

where T is the sampling time, $a_0 = \frac{4k_p T^2}{L_f C_f \pi} - \frac{8k_d T}{L_f C_f \pi} + 4$, $a_1 = \frac{8k_p T^2}{L_f C_f \pi} - 8$, and $a_2 = 4 + \frac{8k_d T}{L_f C_f \pi} + \frac{4k_p T^2}{L_f C_f \pi}$.

Table 4.2: Jury test

Rule	***Conditions***	***Results***
1	If z equals 1, the system output must be positive $\rightarrow D(1)=\frac{16k_pT^2}{L_fC_f\pi}$	$k_p>0$
2	If z equals -1, the system output must hold $\rightarrow(-1)^2D(-1)>0$	D(-1)=16>0
3	The absolute value of the constant term a_0 must be less than the highest coefficient a_2 $\rightarrow\left\lvert\frac{4k_pT^2}{L_fC_f\pi}-\frac{8k_dT}{L_fC_f\pi}+4\right\rvert<4+\frac{8k_dT}{L_fC_f\pi}+\frac{4k_pT^2}{L_fC_f\pi}$	$k_p>-\frac{L_fC_f\pi}{T^2}$ $k_d>0$
4	The Jury array must satisfies the following $\rightarrow\lvert b_0\rvert>\lvert b_1\rvert$	The Jury array is constructed as Table 4.3

The system must pass all of the Jury test shown in Table 4.2, which is an algebraic test, similar in form to Routh-Hurwitz approach, determining whether the roots of a polynomial lie within the unit circle [18] and that the system is therefore considered stable. Coefficients b_0 and b_1 are formed in Jury array as shown in Table 4.3,

Table 4.3: Jury array

Row	z^0	z^1	z^2
1	a_0	a_1	a_2
2	a_2	a_1	a_0
3	b_0	b_1	0
4	b_1	b_0	0
5	c_0	0	0

where $b_0=\left\lvert a_0^2-a_2^2\right\rvert, b_1=\left\lvert a_0a_1-a_1a_2\right\rvert, c_0=\left\lvert b_0^2-b_1^2\right\rvert$ and the 4$^{\text{th}}$ rule in Jury test leads to $\lvert b_0\rvert>\lvert b_1\rvert\rightarrow\left\lvert a_0^2-a_2^2\right\rvert>\left\lvert a_0a_1-a_1a_2\right\rvert$. It is clear that a_1>0, a_0-a_2<0 and a_0+a_2>0, thus the system meets these inequality conditions without any new condition being imposed upon k_p and k_i. Furthermore, the stability of this discrete time system can be analysed by the coefficients of its characteristic polynomial using Jury stability criterion shown in Table 4.4, which is the discrete time analogue of the Routh-

Hurwitz stability criterion. In this stability criterion, the system is considered to be stable if the coefficients of the odd-numbered rows of the first column are positive [18].

Table 4.4: Characteristic polynomial for Jury stability criterion

Row	z^2	z^1	z^0
1	a_2	a_1	a_0
2	a_0	a_1	a_2
3	$a_2 - a_0 \frac{a_0}{a_2}$	$a_1 - a_1 \frac{a_0}{a_2}$	0
4	$a_1 - a_1 \frac{a_0}{a_2}$	$a_2 - a_0 \frac{a_0}{a_2}$	0
5	$a_2 - a_0 \frac{a_0}{a_2} - \frac{(a_1 - a_1 \frac{a_0}{a_2})^2}{a_2 - a_0 \frac{a_0}{a_2}}$	0	0

The Jury stability criterion leads to (4.38)-(4.40).

$$a_2 > 0 \Rightarrow 4 + \frac{8k_d T}{L_f C_f \pi} + \frac{4k_p T^2}{L_f C_f \pi} > 0 \tag{4.38}$$

$$a_2 - a_0 \frac{a_0}{a_2} \Rightarrow a_2 > a_0 \Rightarrow \frac{16k_d T}{L_f C_f \pi} > 0 \tag{4.39}$$

$$a_2 - a_0 \frac{a_0}{a_2} - \frac{(a_1 - a_1 \frac{a_0}{a_2})^2}{a_2 - a_0 \frac{a_0}{a_2}} \Rightarrow a_2 + a_0 > a_1 \Rightarrow 8 > -8 \tag{4.40}$$

The stability condition for the discrete time domain concern can be obtained as (4.41), which is equivalent to the closed-loop stability criterion in the continuous time domain.

$$k_p > 0, \;\; k_d > 0 \tag{4.41}$$

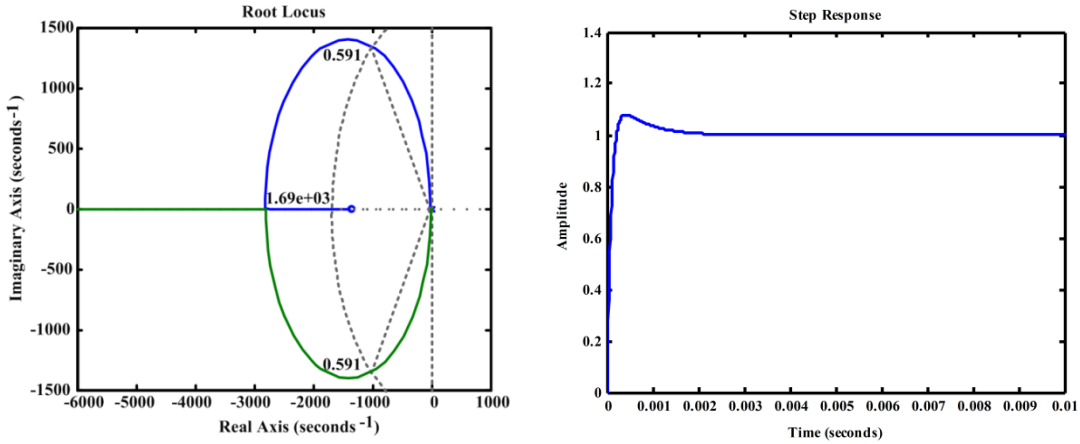
Thus, synthesising the stability criteria, k_p and k_d should be positive to satisfy the requirements to make the closed-loop stable. By designing the damping ratio and natural frequency from the system characteristic equation, the required closed-loop performance can be achieved. Given the design requirements of 10 % overshoot and

4 ms settling time, the proportional and derivative gains k_p and k_d are defined as (4.43) and (4.44) based on the parameters from the test rig. Substituing these gain values into (4.32) and (4.33), the system root locus plot and closed-loop step response respectively can be derived, as shown in Fig.4.7.

$$\varsigma = \frac{k_d}{\sqrt{k_p L_f C_f \pi}} = 0.591, \quad \omega_n = \sqrt{\frac{4k_p}{L_f C_f \pi}} = 1692 \tag{4.42}$$

$$k_p = \frac{\omega_n^{\,2} L_f C_f \pi}{4} = 2.158 \tag{4.43}$$

$$k_d = \sqrt{\varsigma^2 k_p L_f C_f \pi} = 0.00151 \tag{4.44}$$



(a) (b)

Fig.4.7: (a) Root locus performance and (b) step response for system with output voltage controller

C. Sliding Mode Controller Design and Stability Criteria Analysis

Sliding mode control, developed in the early 1950s and, by its wide utilisation in various industrial applications and research studies [19-22], has been proven to be able to provide superb system performance, including tracking system structured uncertainties (or parametric uncertainties), unstructured uncertainties (or unmodeled dynamics), and rejecting external disturbances. In addition, sliding mode control is relatively simple to implement as a result of the high degree of flexibility in its design choices. Several different kinds of sliding mode controller for single module DC/DC converters have been proposed [20, 21, 23-26]. In this study, output voltage

control is achieved using a sliding-mode controller based on the large-signal system shown in Fig.4.4.

This discontinuous controller switches at high-speed between two distinctively different structures to drive the system trajectory on the specified surface and maintain it on the surface upon interception. The surface is called sliding surface $S(x)$. With an appropriate choice of sliding surface, the controller is able to maintain the required system robustness against disturbances and become totally insensitive to a particular class of uncertainties [10, 27]. However, it is based on the assumption that control signal can be switched between the two values infinitely fast. One practical limitation, therefore, is the existing of 'chattering', as it is impossible to achieve infinitely fast switching control due to finite time delays associate with the control computation and limitations of physical switches. The resulting high-frequency oscillation near the desired equilibrium point is highly undesirable.

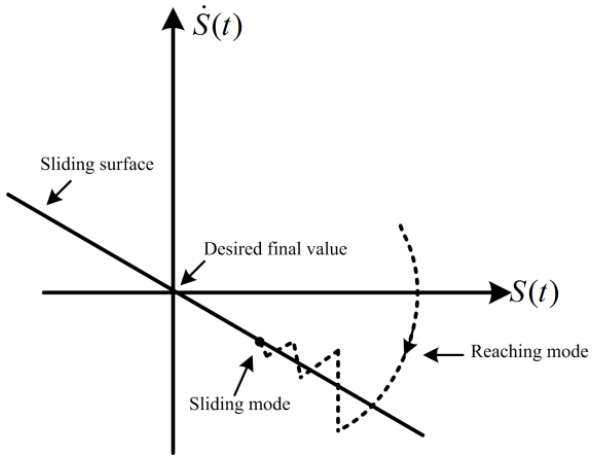


Fig.4.8: Graphical interpretation of sliding mode control

The concept of sliding mode control shown in Fig.4.8 is to force state variable (in this case is the output voltage error) to approach the sliding surface and to move along it until reaching the desired final value. There are two conditions, which if satisfied guarantee the system will converge. Firstly, existence of sliding surface, which requires that a sliding surface must be created that system is able to be directed towards it. From Utki theory, it is known that sliding mode will exist if the inequality in (4.45) is satisfied.

$$\dot{S}(x)S(x) < 0 \tag{4.45}$$

Secondly, the reachability condition consists of two aspects: hitting and stability condition. Once (4.46) is achieved, the capability of the system to hit the sliding surface is ensured. The stability condition requires that the system moves along surface $S(x)$, until a stable point is reached. The system trajectory can be described by differential equation in (4.47).

$$S(x) = 0 \tag{4.46}$$

$$\dot{S}(x) = 0 \tag{4.47}$$

The proposed sliding mode control generates the phase shift angle for PWM control using a state feedback scheme. A new variable is defined by DC input voltage and transformer turn ratio as shown in (4.48). A state space matrix of the error between the output voltage and the output votlage reference (4.49) is also defined. The control objective is to reduce this error to zero. The system state vector is shown in (4.50).

$$v_i = V_{dc} / k \tag{4.48}$$

$$e = v_o^* - V_o \tag{4.49}$$

$$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} v_o^* - V_o \\ \dfrac{d(v_o^* - V_o)}{dt} \\ \int x_1 dt \end{bmatrix} = \begin{bmatrix} v_o^* - V_o \\ -2\dfrac{I_{lf}}{C_f} + \dfrac{2V_o}{R_o C_f} \\ \int x_1 dt \end{bmatrix} = \begin{bmatrix} v_o^* - V_o \\ 2\int \dfrac{V_o - v_i u}{L_f C_f} dt + \dfrac{2V_o}{R_o C_f} \\ \int x_1 dt \end{bmatrix} \tag{4.50}$$

State space equation of (4.50) can be rewritten as (4.51),

$$\dot{x} = Ax + Bu + C \tag{4.51}$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & \dfrac{2V_o}{L_f C_f} & 0 \\ 1 & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ \dfrac{-2v_i}{L_f C_f} \\ 0 \end{bmatrix}, \quad C = \begin{bmatrix} 0 \\ \dfrac{2V_o}{R_o C_f} \\ 0 \end{bmatrix} \tag{4.52}$$

The sliding surface with proportional, integral and derivative of error is defined as (4.53) and the derivative of the sliding surface can be obtained as (4.54) [22, 28, 29].

$$S = k_1 e(t) + k_2 \frac{de(t)}{dt} + k_3 \int e(t)dt = k_1 x_1 + k_2 x_2 + k_3 x_3 = Jx \tag{4.53}$$

$$\dot{S}(x) = k_1 \dot{e}(t) + k_2 \ddot{e}(t) + k_3 e(t) = JAx + JBu + JC \tag{4.54}$$

where k_1, k_2 and k_3 are sticky positive constants which determine the trajectory of state variables, $J = \begin{bmatrix} k_1 & k_2 & k_3 \end{bmatrix}$, u=1 when S>0 and u=0 when S<0. Equation (4.54) highlights the dependence of the sliding surface existence condition on input voltage, filter capacitance, inductance, resistance and output voltage. A previous study [22] explains the need for fixed-frequency sliding mode control. Therefore, a PWM based sliding mode controller is employed instead of a hysteresis modulation based sliding mode controller. Control signal d_{eq} can be derived by solving (4.54) when set equal to 0.

$$d_{eq} = -\left[JB\right]^{-1} J\left[Ax + C\right] = \frac{L_f C_f k_3}{2k_2 v_i} x_1 + (\frac{V_o}{v_i} + \frac{L_f C_f k_1}{2k_2 v_i}) x_2 + \frac{V_o}{v_i R_o} \tag{4.55}$$

Substituting (4.49) and (4.50), (4.55) can be rewritten as (4.56),

$$d_{eq} = k_p e + k_d \dot{e} + \frac{V_o}{v_i R_o} \tag{4.56}$$

where the k_p is the proportion gain and k_d is the derivative gain.

Given the sliding surface, the sliding mode output voltage controller for IPOS connected 2-module DC/DC converter is shown in Fig.4.9. The conditions that must be satisfied by the controller include the sliding mode existence condition, reachability and stability conditions. It can be seen from Fig.4.9 that the control signal of the sliding mode controller can be represented as a PD controller, in the same way as with the Lyapunov controller. Considering the unavoidable and undesirable chattering issue associated with sliding mode control, the Lyapunov topology is the non-linear controller adopted in this study.

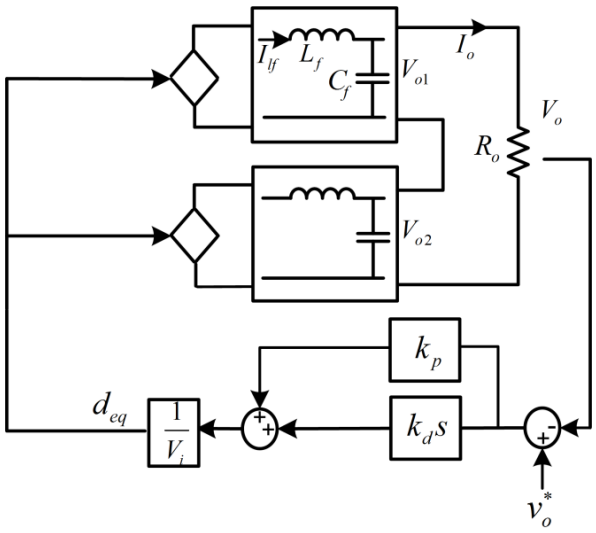


Fig.4.9: Sliding mode control based PD output voltage controller

D. Comparison between Lyapunov and PI Controllers

The closed-loop output voltage controller obtained using the Lyapunov approach is shown in Fig.4.6 (b). In contrast, the linear PI output voltage closed-loop controller shown in Fig.4.10, based on the small-signal model transfer function (4.10), is introduced to enable the comparison.

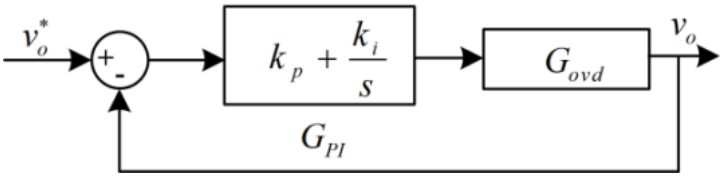
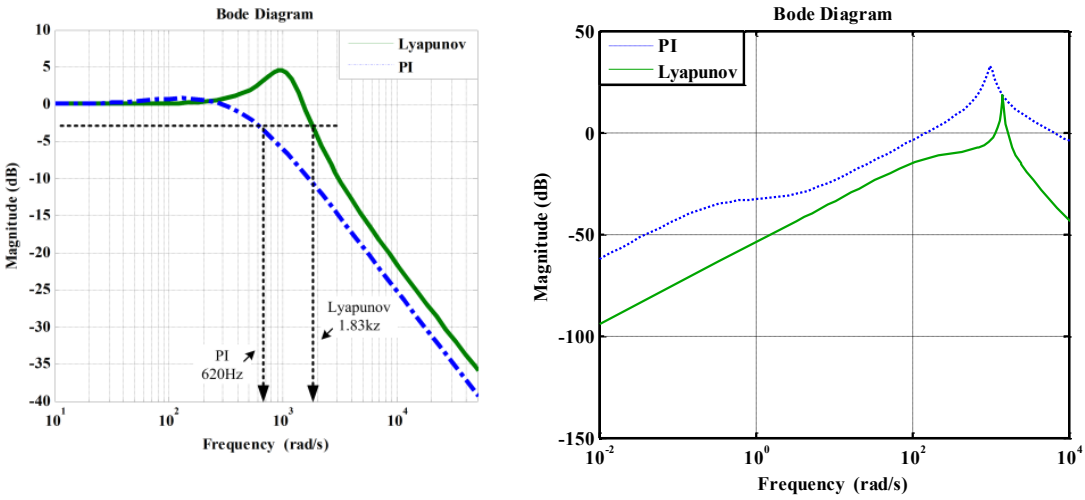


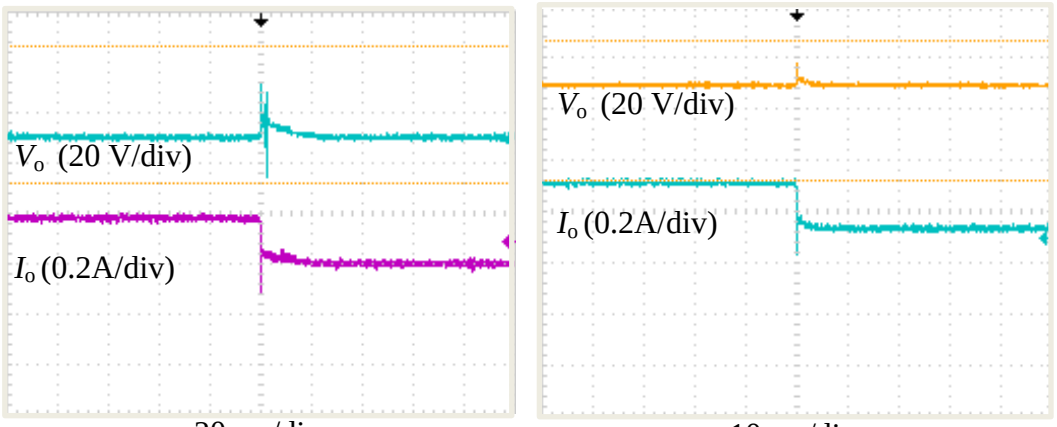
Fig.4.10: Conventional PI closed-loop controller

The robustness of the Lyapunov based controller to circuit parameter variations and its superior performance are shown by comparing the system bandwidth of the two controllers. Fig.4.11 (a) shows that the system bandwidth achieved using PI control is 620 Hz, whilst that achieved using Lyapunov control is 1.83 kHz. Fig.4.11 (b) shows the closed-loop output impedance performance of a PI controller superimposed on that of the Lyapunov counterpart. Observe that the proposed Lyapunov controller exhibits much better attenuation and disturbance rejection than the PI controller.



(a) (b)

Fig.4.11: Comparison of PI and Lyapunov controllers (a) closed-loop bandwidth and (b) closed-loop output impedance



20 ms/div 10 ms/div

(a) (b)

Fig.4.12: Output voltage and current response to a step load decrease (a) PI controller and (b) Lyapunov controller

From Fig.4.12 , it can been seen that the output voltage and current recover from the load change transient (realised by increasing load resistance from 80 Ω to 100 Ω) is less than 5 ms for the Lyapunov controller compared to nearly 15 ms for the PI controller. According to the comparison, Lyapunov control, which features the faster dynamic response at start-up and higher disturbance rejection capability, is applied to track the output voltage reference. The output voltage sharing controller that ensures the power sharing between modules with parameter mismatched is described in the following section.

4.4.2 Power Sharing Control

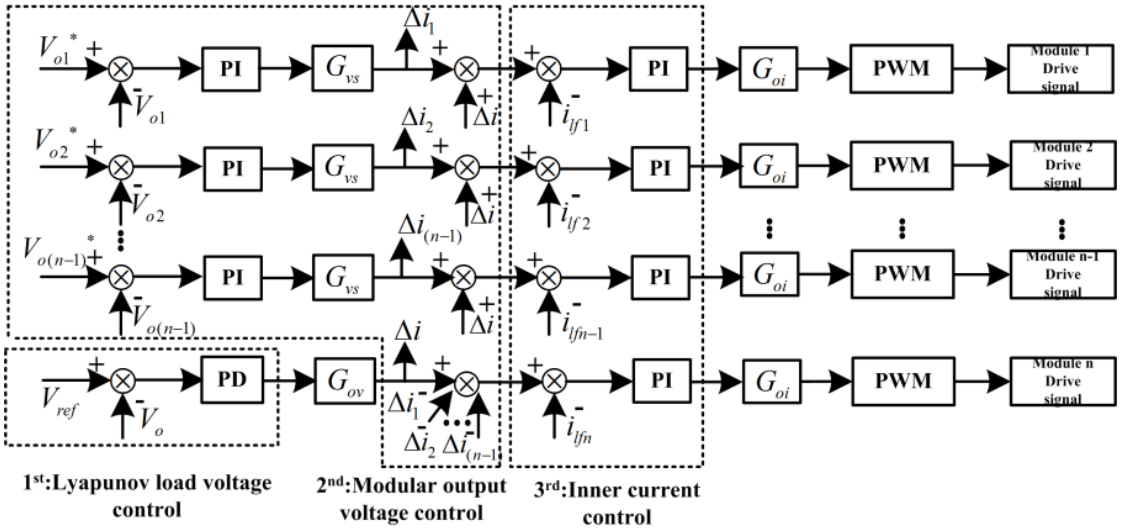


Fig.4.13: Overall control scheme

It has been stated that the Lyapunov-based voltage controller is used to establish a structure for the load voltage controller that ensures global system stability, and has resulted in a PD controller. Here, the Lyapunov controller serves as an outer control loop to produce the current reference required by the inner current control loop. The process of designing the control function is the same as in the previous section. For power sharing control, the OVS controller balances the slave module output voltages and compensates for any disturbance by minimising the differences between the slave output voltages and the voltage reference signal to generate the inductor current contributions Δi_1, Δi_2, Δi_3 and Δi_{n-1} through the PI controller. In this case, each slave module output voltage controller tracks the set-point, $V_{o1}^* = V_{o2}^* = V_{o(n-1)}^* = V_o/n$, with zero steady-state error. The sum of the current references Δi_i (i=1, 2,…, n-1) produced by all of the slave modules is subtracted from the current reference for the master module (the n^{th} module in Fig.4.1), and Δi is added to the current reference of each slave module. During steady-state operation, the integral term in the modular output voltage controller contributes the majority of the current demand to the inner current loop, however, it should be noted that the PD controller plays the most crucial role during start-up and other major transient events, especially module failure events. A third current control loop is added to increase the control freedom in order to

improve performance, and is designed according to (4.12) for each module. The resulting control structure is shown in Fig.4.13.

In order to assess the effectiveness of the proposed control scheme, a system consisting of 10 modules connected in an IPOS topology with rated output power of 10 MW is simulated and the results are given in the following section.

4.4.3 Simulation Validations of Normal Operation

Table 4.5: List of parameters for IPOS connected 10-module DC/DC converter

Parameter	***Simulation Values***	***Parameter***	***Simulation Values***
Converter Rated Power	5 MW	Transformer Turns-Ratio	T_1 =1:1.78 T_2 =1:1.74 T_3 =1:1.7 T_4 =1:1.78 T_5 =1:1.74 T_6 =1:1.7 T_7 =1:1.78 T_8 =1:1.74 T_9 =1:1.7 T_{10}=1:1.78
Number of Modules	10		
Input DC Voltage	5 kV		
Output DC Voltage	50 kV		
PWM Carrier Frequency	2.5 kHz		
Output Inductance	L_1 =50 mH L_2 =60 mH L_3 =50 mH L_4 =60 mH L_5 =50 mH L_6 =60 mH L_7 =50 mH L_8 =60 mH L_9 =50 mH L_{10}=60 mH	Output Capacitance	C_1 =80 μF C_2 =90 μF C_3 =80 μF C_4 =90 μF C_5 =80 μF C_6 =90 μF C_7 =80 μF C_8 =90 μF C_9 =80 μF C_{10}=90 μF

The converter acts as a step-up DC transformer with 5 kV/50 kV voltage ratio. Other parameters are listed in Table 4.5, where different parameters mismatches are considered to test the effectiveness of the power balancing function. In this illustration, the converter is initially commanded to regulate its output terminal voltage at 48 kV across a resistive load of 500 Ω. At time t=0.1 s, output voltage is increased to the 50 kV and is then reduced to 48 kV at time t=0.2 s. Selected waveforms are presented in Fig.4.14.

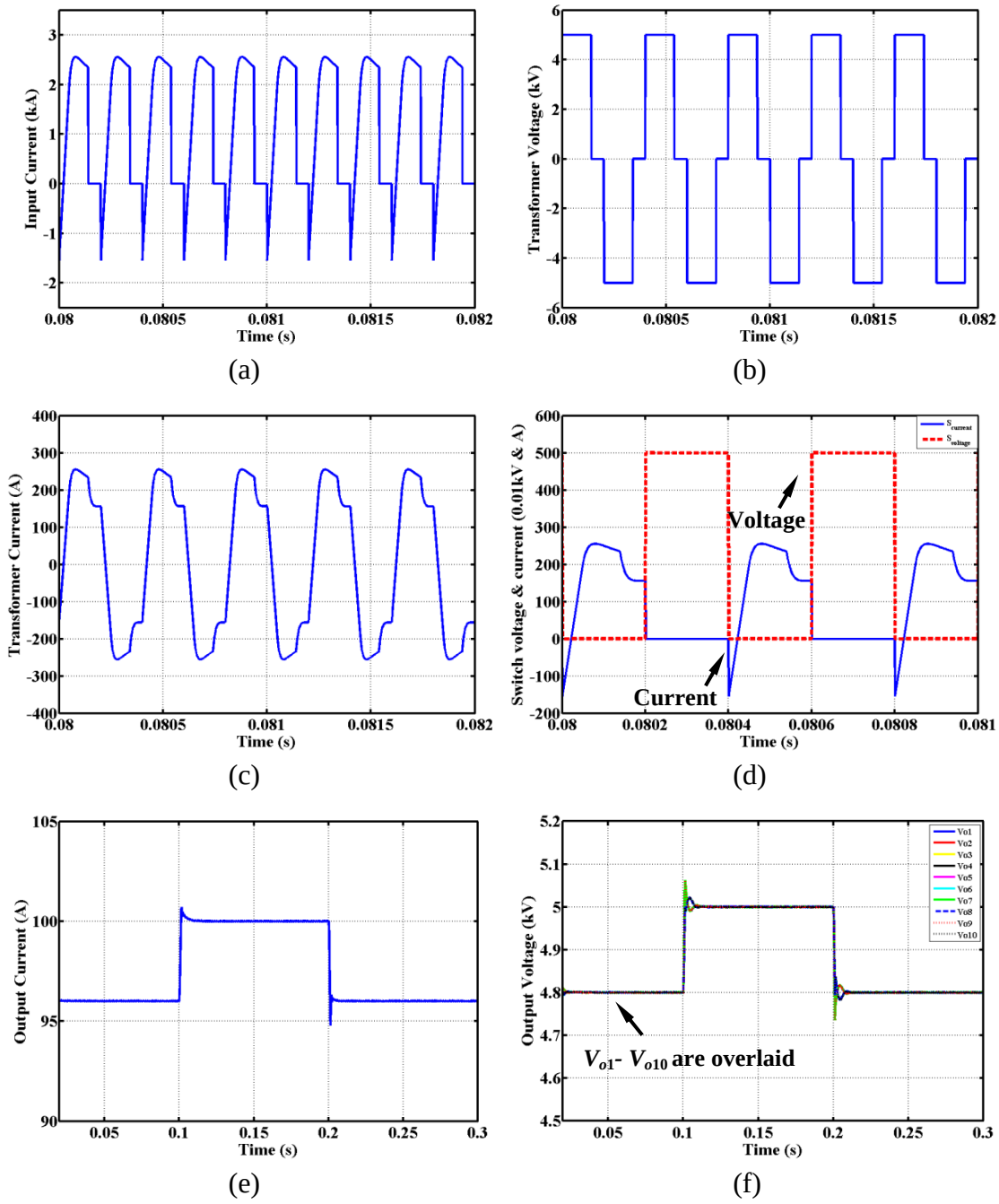
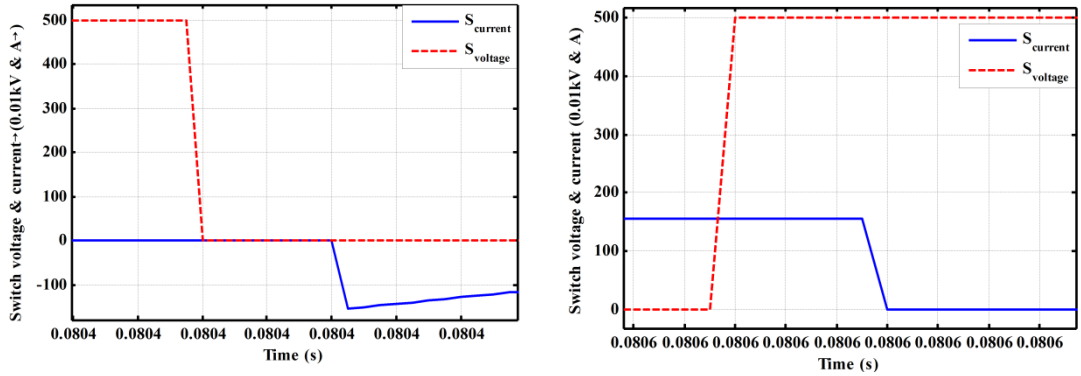


Fig.4.14: Dynamic response of the converter to a step change in DC output voltage (a) pre-filter input current per module (b) voltage waveform presented to the primary windings of the high-frequency transformer (c) current waveform in the primary windings of the high-frequency transformer (d) switch voltage and current waveforms (e) output dc current (f) output voltages of individual modules

Fig.4.14 (a), (b) and (c) show several cycles of discontinuous input current for a single module, the voltage waveform across the primary winding of the transformer, and current in the transformer primary winding respectively. Fig.4.14 (d) shows current in the switching device and its corresponding voltage normalised by a factor of 10. It can be observed from these waveforms that the full-bridge devices operate using soft switching, thus, low switching losses are expected. Fig.4.14 (e) and (f) show DC output current and modular output voltages as the output voltage reference changes as stated previously.



(a) (b)

Fig.4.15: Waveforms demonstrating the switch voltage and current waveforms

Waveforms in Fig.4.15 illusrate the soft-switching of the module active front full-bridge, where Fig.4.15 (a) shows the ZVS turn-on without switching on losses and Fig.4.15 (b) shows the ZVS turn-off without switching off losses. Additional results in Fig.4.16 demonstrate the converter ability to perform controlled recharge of medium-voltage DC network by ramping the output voltage gradually from 0 to 50 kV within 50 ms, and selected waveforms obtained are presented in Fig.4.16 (a) to (d). Fig.4.16 (a) and (b) show the gradual output current and voltage. Fig.4.16 (c) shows the modular output voltage sharing performance under ramping condition and (d) gives the transient performance.

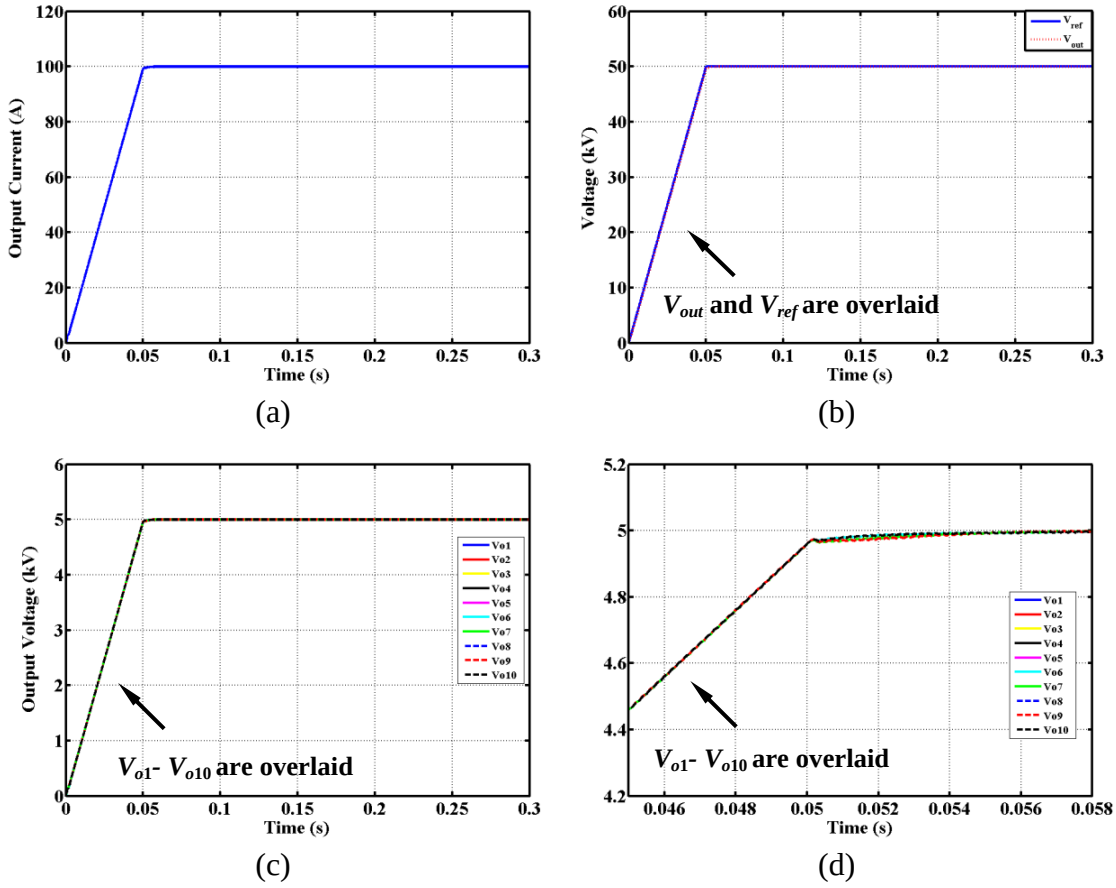


Fig.4.16: Waveforms demonstrating the gradual output build-up and output voltage sharing between modules (a) output dc currents (b) voltage reference and output voltage (c) output voltages of individual modules (d) transient performance of output voltages of individual modules

Fig.4.14 shows that the proposed control strategy for the IPOS connected modular DC/DC converter, which has a dedicated voltage balancing loop and a current loop for each module, exhibits superior performance in terms of dynamic response, requiring only a few milliseconds to follow the voltage variation, and power sharing between modules with mismatches in parameter values. These results in Fig.4.16 show that the converter has the ability to recharge a DC network, with total output voltage being evenly shared between modules. In addition, these results illustrate the possibilities of this family of DC/DC converters in medium-voltage high-power applications.

To be capable of achieving true (n+1) redundancy, a novel 'non-dedicated master' control scheme is constructed to guarantee the reliability of the converter in the event of a fault in the master module, and is presented in the next section.

4.5 Novel 'Non-Dedicated Master' Control Scheme with True (n+1) Redundancy

The multi-module DC/DC converter has internal fault management capability similar to that of an M2C converter, in that faulty modules may be bypassed in order to allow continued system operation without any performance degradation [30]. Such a feature is normally achievable by incorporating redundant modules to allow re-configuration of the power circuit and bypassing of the faulty modules. The modularity feature allows (n+k) redundancy, where n is the number of modules required to ensure that each module operates within its voltage rating, and k is the number of redundant modules that can be used to replace k faulty modules and maintain uninterrupted operation. In the following section, (n+1) redundancy is chosen to address the control scheme.

4.5.1 Fault Tolerant Control

The modular structure facilitates identification of fault location and bypassing of the faulty modules. To illustrate its fault-tolerance operation, a 4-module DC/DC converter with the toplogogy shown in Fig.4.1 redundancy level k=1 is introduced. The failure of a single or multiple modules can be detected by monitoring module output voltages and currents and comparing them with predefined limits, such as [$0.2V_o$<V_{oi}<$0.3V_o$] in this case, for i=1 to 4. The faulty modules are isolated by blocking their front-end H-bridge converters, and their corresponding output diode bridges are bypassed using a combination of bypass switches and bleed resistors to dissipate the energy E_c , shown in (4.57), stored in their DC side filter capacitors.

$$E_c = \frac{1}{2} CU^2 \tag{4.57}$$

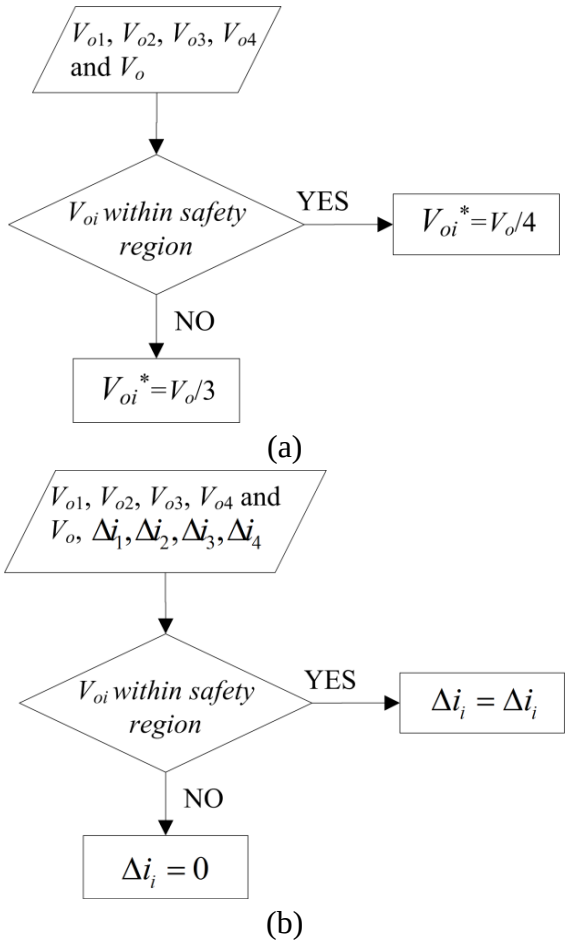


Fig.4.17: Flow chart for (a) voltage reference generation function (b) current demand correction function

Flow charts defining the voltage reference generation and current demand correction functions are shown in Fig.4.17. The modular structure facilitates location of the faulty module. Any module can be operated in either an active state or a blocked state. A current demand correction function is activated to remove the bypassed module's contribution to the master module. Moreover, each module can be equipped with an over-current protection function at its input so that, if module input current exceeds a predefined threshold for a predefined duration, a trip signal is generated to block the front-end converter and bypass its output as previously stated.

When any slave module fails, it will be identified and bypassed, whilst the system remains operational. In this case, the reference voltage to the slave modules must be changed. For an example, when k out of n modules have failed, the reference voltage for all slave modules must be changed from V_o^*/n to $V_o^*/(n-k)$. The commonly used

master-slave scheme, however, has problems associated with ensuring fault ride-through operation in the event of a fault in the master module, which is a consequence of its 'fixed master' characteristic. The operation of the slaves is, however, dependent upon the master module control signal, i.e. if the master module malfunctions the overall system may fail [31]. To date, the widely-used master-slave scheme, where a specific module is designated as 'master' under all conditions, has a decreased reliability and modularity, and using such a control scheme for the modular DC/DC converter being studied is less attractive from the system reliability point of view. To solve the issue, this study proposes a novel control strategy for enabling power sharing in the IPOS connected modular DC/DC converter, when there is mismatch between module components, and fault ride-through in the event of a fault in the master module.

4.5.2 'Non-dedicated Master' Control Scheme

In order to avoid system collapse with a faulty master module, a 'non-dedicated master' approach is proposed, which enables the role of 'master' to be reallocated to another healthy module when the original master module fails. Because each module has the ability to become a master if required, any module may malfunction without affecting the operation of the whole system. The failure flow graph for a 4-module converter is shown in Fig.4.18 and the detailed description of the control is given as follows.

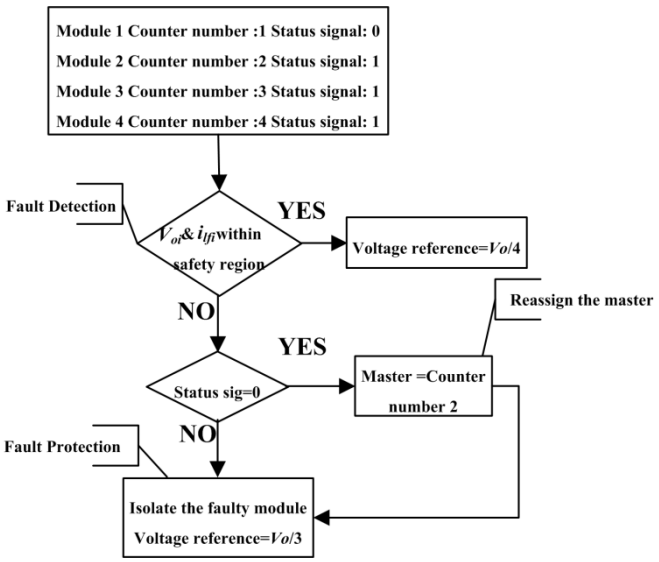


Fig.4.18: Flow chart for the 'non-dedicated master' control scheme

For an *n* module converter, each module is assigned with a specific numerical identifier between 1 and *n*, where *n* stands for number of modules. Meanwhile, the control system assigns the status signal '0' to a master module and '1' to the remaining modules, which are slaves. The fault detection and protection function will be actived when the affected modules' output voltages or currents are outside the predefined limits. When '*k*' slave modules fail the voltage reference for the remaining healthy slave modules is updated to $V_o^*/(n\text{-}k)$. The master module will remain the same. When a master module fails, one of the healthy slave modules will be assigned to become a new master module and the voltage reference for the slave modules must be updated. The faulty master module must be isolated immediately.

4.5.3 Simulation Validation for Master-Module Fault

In order to assess the proposed control scheme for the IPOS DC/DC converter, the system shown in Fig.4.19, consisting of a generator connected to an uncontrolled diode rectifier and an IPOS modular DC/DC converter with rated output power of 5 MW is simulated. Generator output voltage is 2500 V at 50 Hz, the medium-frequency transformer operates at 5 kHz and has a turns-ratio of 2500:8250 V, and the load voltage is maintained at 33 kV.

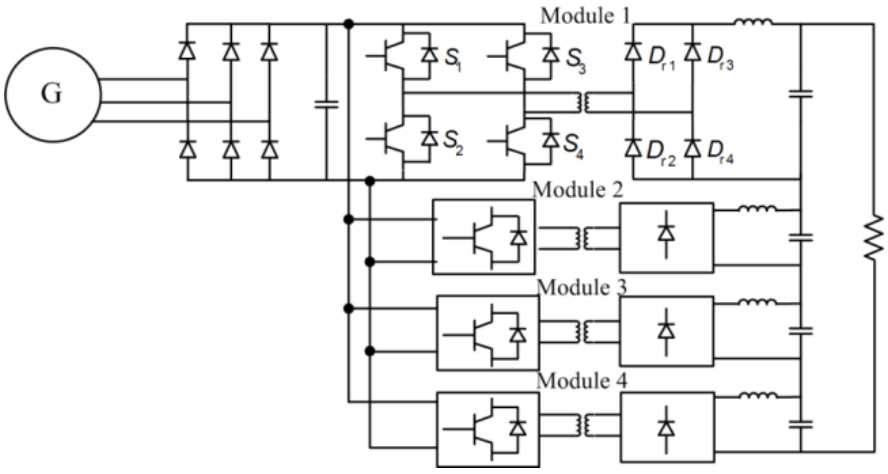
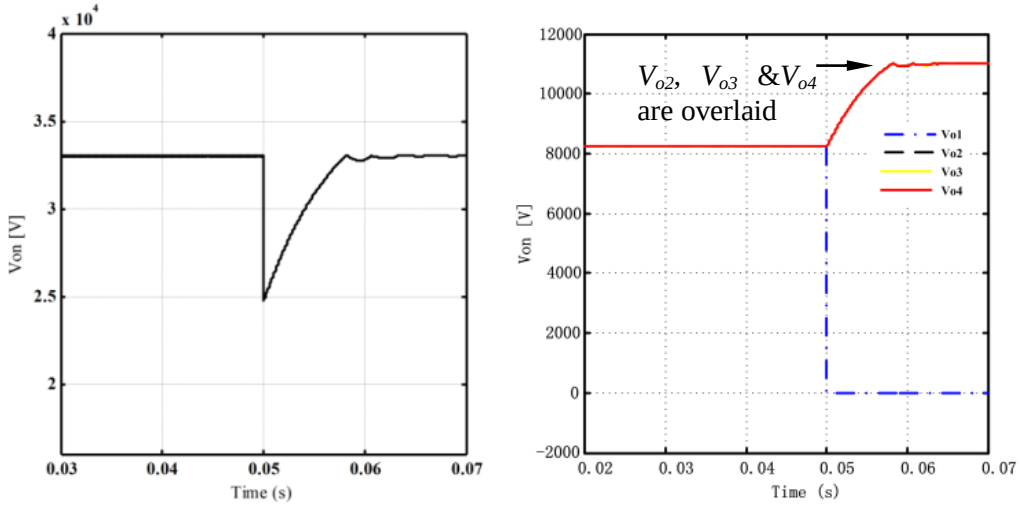


Fig.4.19: High-power system used in fault study

Module 1 is initially chosen as the master module. To test the effectiveness of the power balancing function when parameter mismatch is considered, the following mismatches are assumed: +10 % in transformer turns-ratio of module 1 and +10 % in

the output filter capacitor of module 2. To show enhanced system reliability when the master' module fails, a permanent short-circuit fault is applied at the output terminals of the master module (module 1) at t=50 ms. Selected results obtained from this case are summarised in Fig.4.20.



(a) (b)

Fig.4.20: Dyanmic response of the system to failure of the master master module (a) load voltage (b) module output voltages

Fig.4.20 (a) shows the converter output voltage V_o and Fig.4.20 (b) shows the individual module output voltage (V_{o1}, V_{o2}, V_{o3} and V_{o4}). Observe that in the pre-fault condition the proposed control scheme is able to ensure equal output voltage sharing amongst the modules, despite the presence of substantial parameters mismatches in various modules. Following the fault at t=50 ms, the faulty module is isolated and the output voltages of the remaining healthy modules have increased to compensate the lost module (to keep the output voltage constant as in pre-fault). These results show that the proposed control scheme manages failure of the master module, whilst ensuring continuous operation and equal voltage sharing amongst the remaining healthy modules.

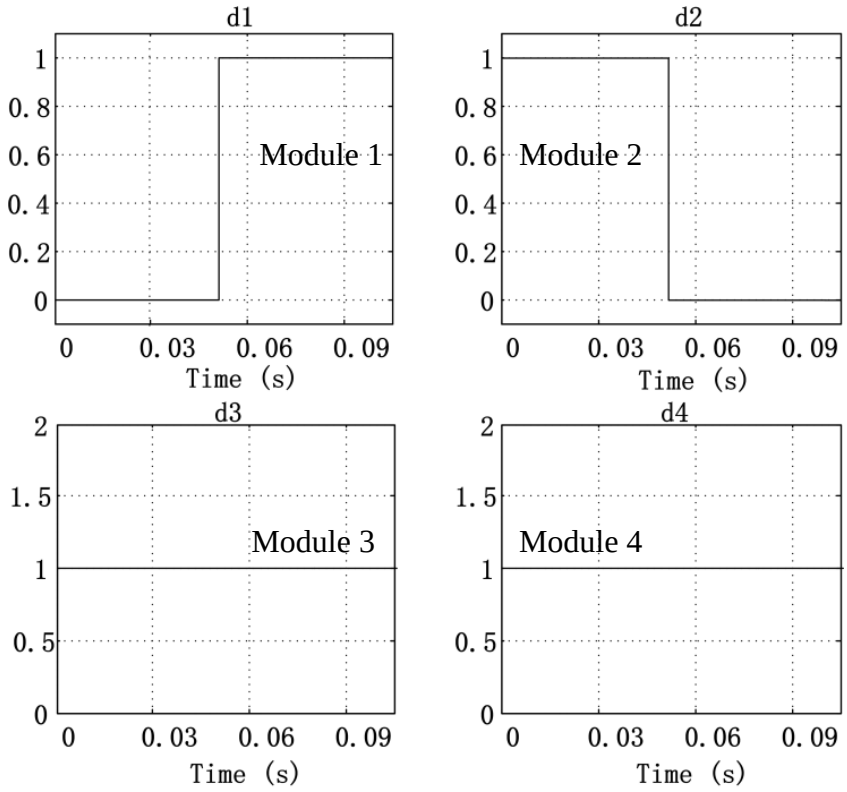


Fig.4.21: Allocation of ‘master’ and ‘slave’ roles

Following the fault, the ‘non-dedicated master’ control function reallocates the role of ‘master’ to a healthy module, which in this case is module 2. This process is illustrated in Fig.4.21 which shows the signals that define ‘master’ and ‘slave’ status of the modules. The i^{th} module is defined as ‘master’ or ‘slave’ when d_i=0 or d_i=1 respectively. It can be seen that, following the fault, Module 1 is deselected as ‘master’ module and Module 2 is selected as the new ‘master’.

The full-scale simulation of the 5 MW converter is used a means of substantiation at typical voltage and current ratings expected in a DC collection network. In addtion, ensuring power balance between the modules prevents exposure of single a module to excessive voltage stress beyond its tolerable limits at the output stage and excessive current stresses at the input stage. Additionally, a scaled-down experiment set-up and experimental results are presented to corroborate the theoretical design.

4.6 Experimental Set-Up and Validation

4.6.1 Experimental Set-Up

To validate the proposed control scheme, a prototype of 4-module IPOS connected modular DC/DC converter shown in Fig.4.22 rated at 200 W per module was built. The proposed control system was implemented using an Infinoeon Technology Tricore TC1796 microcontroller.

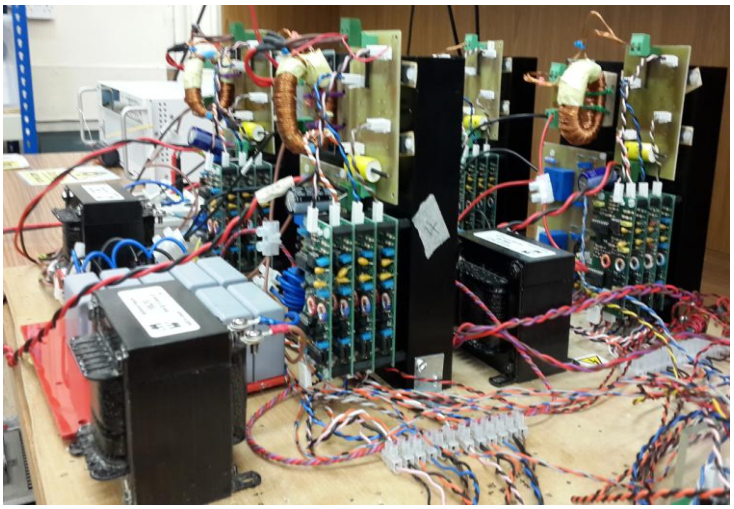


Fig.4.22: IPOS connected modular DC/DC converter test rig

The application of the medium- or high-frequency transformer could lead to a smaller size of the converter. However, the performance and the sizing are dependent upon the material properties. It has been stated in Chapter 3 that a NANOPERM core transformer is applied and the design detail is given as follows.

Table 4.6: List of parameters for transformer rating

Parameters	***Values***
Primary voltage (V_{pri})	40 V
Secondary voltage (V_{sec})	40 V
Ideal Turn ratio (n_{ideal})	1
Transformer Efficiency (η_t)	0.99
Output power (P_{out})	200 W

The maximum duty cycle D_{max} is approximate 0.95. The required transformer turns-ratio can be calculated as (4.58).

$$n = \frac{D_{max}}{n_{ideal}} = \frac{0.95}{1} = 1:1.11 \tag{4.58}$$

Assuming the number of primary turns is $N_1 = 40$ turns, the secondary turns are obtained as shown in (4.59).

$$N_2 = n \times N_1 = 1.11 \times 40 = 45 \text{ turns} \tag{4.59}$$

The required area product (cm^4) is calculated by (4.60),

$$AP = \frac{P_t 10^4}{k f_s B_{\max} K_u J} \tag{4.60}$$

where k is 4 for square-wave profile, transformer switching frequency f_s is 2.5 kHz, B_{max}=0.8×B_{sat}=0.8×1.2=0.96, the window utilisation factor K_u=0.4, and current density J is chosen as 460A/cm^2. Hence, the required area produce is given by (4.61) and a 'Magnetec GmbH M-014-04' core is consequently selected with the specifications defined by (4.62)-(4.64).

$$AP = \frac{P_{out} 10^4}{k f_s B_{\max} K_u J} = \frac{200 \times 10^4}{4 \times 2.5 \times 10^3 \times 0.96 \times 0.4 \times 460} = 1.1435 \text{ cm}^4 \tag{4.61}$$

$$A_c = 0.44 \text{ cm}^2 \tag{4.62}$$

$$W_a = 6.621 \text{ cm}^2 \tag{4.63}$$

$$\mu_r = 3000 \text{ at 10 kHz} \tag{4.64}$$

The filter can reduce the noise injected at the input side, picked up by the connection wires and the control board, to increase quality of the output by reducing the voltage and current ripples. The LC filter is therefore defined by voltage and current ripple limits. The selection for the output capacitance value is determined by the allowable output ripple voltage, which is 1 % of the output voltage (V_o=20 V).

$$\Delta V = 0.01 \times V_o = 0.01 \times 20 = 0.2 \text{ V} \tag{4.65}$$

Specifying the output ripple current at 10 % of full load current (I_o=4 A), the ripple current will be as shown in (4.66). Estimating the time constant defined by the

capacitor and its equivalent series resistance (R_{ESR}) to be $R_{ESR}C_{out}$=50 μs (time constant is typically in the range 50- 80 μs for aluminium electrolytic capacitor), the required equivalent series resistance for the capacitor is given by (4.67).

$$\Delta I = 0.1 \times I_o = 0.1 \times 4 = 0.4\,\mathrm{A} \tag{4.66}$$

$$R_{ESR} = \frac{\Delta V}{\Delta I} = \frac{0.2}{0.4} = 0.5\ \Omega \tag{4.67}$$

Hence, the required output capacitance is obtained as (4.68). According to the current ripple requirements, the required inductance can be obtained as (4.69). The main parameters of the system are listed in Table 4.7.

$$C_f = \frac{50\mu}{R_{ESR}} = \frac{50\mu}{0.5} \geq 100\mu F \tag{4.68}$$

$$L_f = \frac{V_{in} D_{\max}}{2\Delta I_o f} = \frac{20 \times 0.95}{2 \times 0.4 \times 5 \times 10^3} \geq 4.75\,\mathrm{mH} \tag{4.69}$$

Table 4.7: List of parameters for experimental system

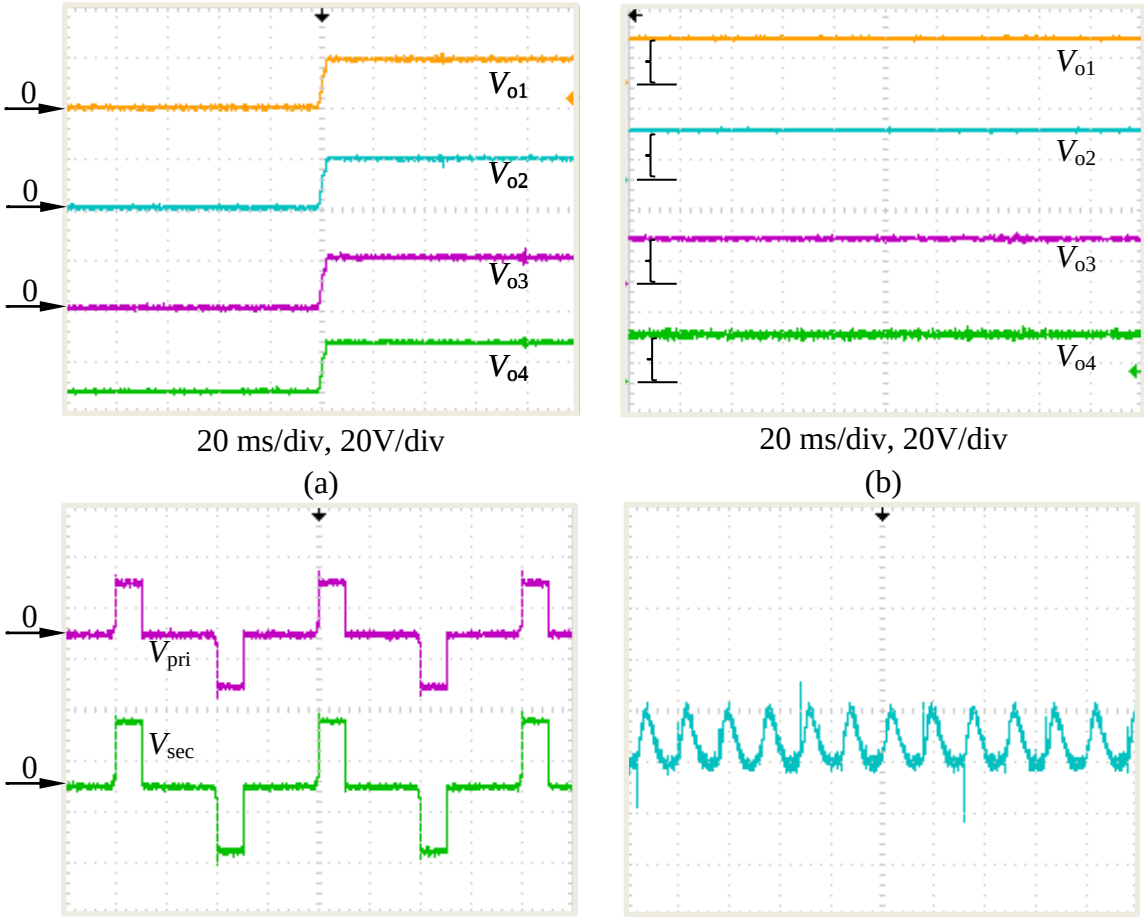
Parameter	***Experimental Values***	***Parameter***	***Experimental Values***
Converter Rated Power	200 W	Transformer Turns-Ratio	T_1 =1:1.4 T_2 =1:1.2 T_3 =1:1.3 T_4 =1:1.2
Number of Modules	4		
Input DC Voltage	20 V	Output Inductance	L_1 =6.8 mH L_2 =5.0 mH L_3 =5.9 mH L_4 =6.3 mH
Output DC Voltage	80 V		
PWM Carrier Frequency	5 kHz	Output Capacitance	C_1 =160 μF C_2 =160 μF C_3 =200 μF C_4 =200 μF

Selected experimental results obtained from this prototype are summarised as follows.

4.6.2 Experimental Validation of Normal Operation

To demonstrate the robustness of the power (output voltage) sharing that the proposed control strategy can offer, Fig.4.23 (a) and (b) present individual module

output voltages (V_{o1}, V_{o2}, V_{o3} and V_{o4}) during start-up and steady-state operation of the 4-module DC/DC converter being studied. Observe that the experimental output voltages of all four modules of the DC/DC converter being test are tightly regulated during start-up and steady state when the output voltage reference is ramped from 0 to 80 V within 10 ms. Fig.4.23 (c) shows the voltage waveforms across the coupling transformer primary and secondary windings, and Fig.4.23 (d) shows samples of the converter's discontiuous input current. These results are achieved despite the noticeable mismatch in transformer turns-ratios, module filter capacitances and inductances.



20 ms/div, 20V/div
(a)

20 ms/div, 20V/div
(b)

50 us/div, 20V/div
(c)

50 us/div, 2V/div
(d)

Fig.4.23: Experimental results illustrating normal operation of the converter (a) modular output voltage during start-up (b) steady-state modular output voltage (c) voltage waveform presented to the primary and secondary windings of the high-frequency transformer and (d) discontinuous input current in normal operation with proposed control strategy

4.6.3 Experimental Validation of Transient Operation

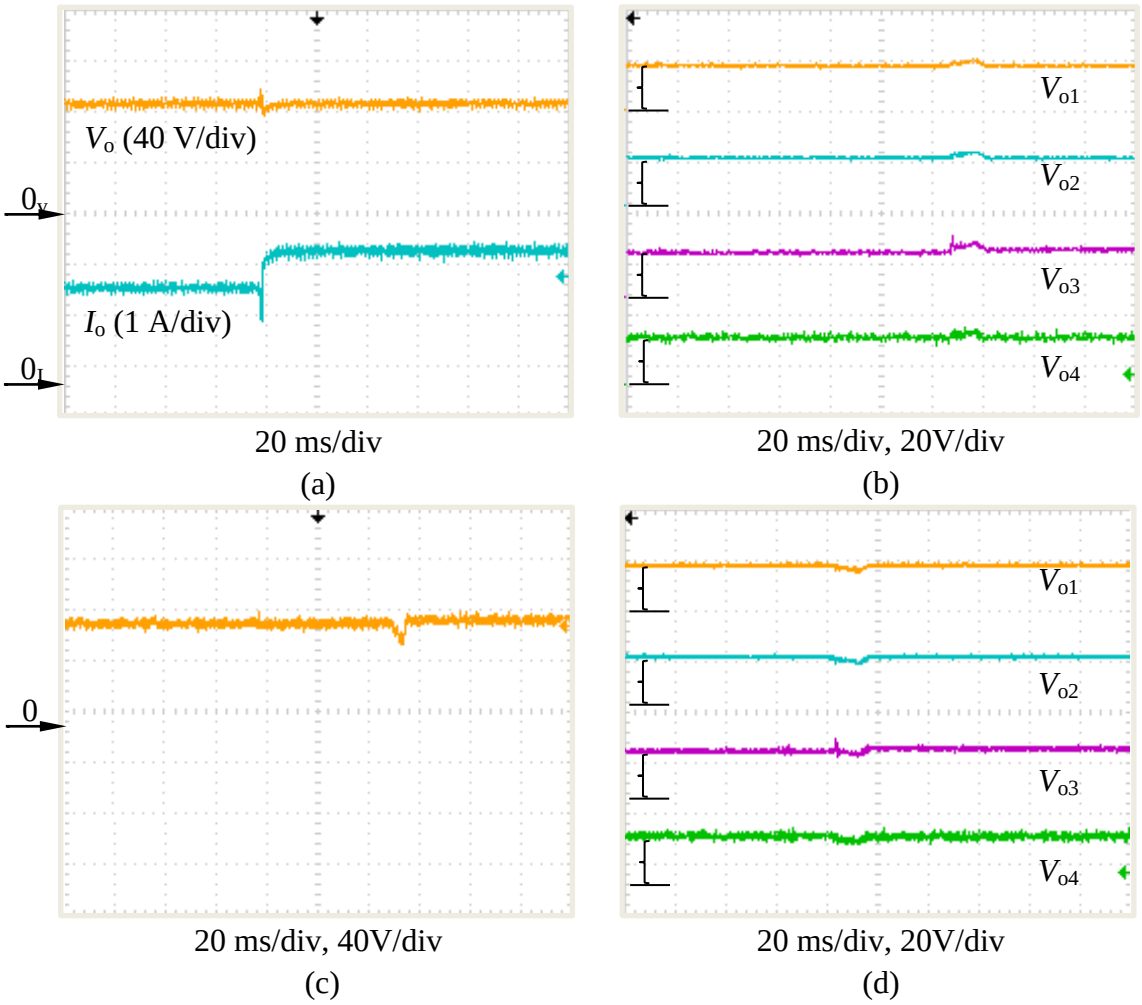


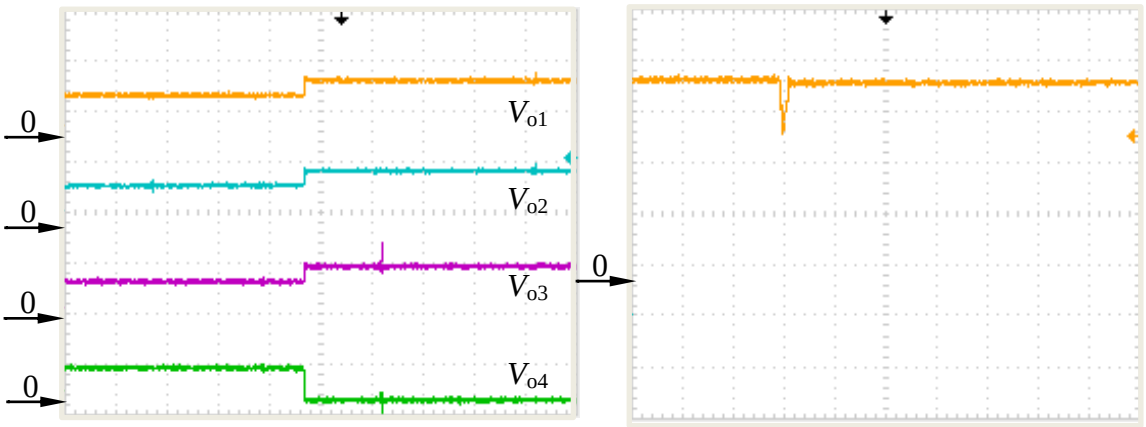
Fig.4.24: Experimental results with proposed control strategy (a) output voltage and current response and (b) modular output voltage as the load resistance is decreased (c) output voltage and current response and (d) modular output voltage as the load resistance is increased

Fig.4.24 (a), (b), (c) and (d) show selected experimental results obtained during a load transient to illustrate the dynamic response of the IPOS connected modular DC/DC converter when the proposed control scheme is employed. Fig.4.24 (a) and (b) illustrate voltage performances when load resistance is decreased. Notice that Fig.4.24 (a) shows the overall output voltage (V_o) is regulated exactly at the desired set-points before and after the change in the load resistance and output current (I_o) is increased as the load resistance is decreased. Observe that the output voltage and current in Fig.4.24 (a) and the individual modules output voltages (V_{o1}, V_{o2}, V_{o3} and

V_{o4}) in Fig.4.24 (b) only exhibit minimum transients following the increase in load (decrease of the load resistance from 40 Ω to 32 Ω). The transient response to a step increase in load resistance (increase of the load resistance from 32 Ω to 40 Ω) is shown in Fig.4.24 (c) and (d), where output voltage and individual modules output voltages (V_{o1}, V_{o2}, V_{o3} and V_{o4}) are regulated at the desired reference value after a short duration with minimal oscillation, the steady-state condition is recovered after 10 ms.

4.6.3 Experimental Validation of Fault-Tolerant Operation

To demonstrate the fault-tolerant capability of the proposed 'non-dedicated master' control scheme, a short-circuit fault is applied at the output terminals of master module (module 4 in the experimental test rig).



100 ms/div, 20V/div (a)

10 ms/div, 20V/div (b)

Fig.4.25: Experimental results illustrating fault-tolerant operation of the converter(a) modular output voltage and (b) output voltage response during master-module fault transient with proposed control strategy

During the pre-fault condition, the load voltage is equally shared amongst the modules. Following detection of the fault, module 4 is isolated and its output voltage falls to zero, as shown in Fig.4.25 (a). Meanwhile, the 'non-dedicated master' control function reallocates the role of master to module 1 and the output voltages of the remaining healthy modules are boosted to $⅓V_o$ to compensate for the lost contribution of the faulty module. Output voltage V_o is therefore maintained at its pre-fault value, after a short duration voltage dip, and is shared equally between the healthy modules, see Fig.4.25 (b). These results show that the proposed control

scheme is capable of managing a master module fault, whilst ensuring continuous operation of and equal voltage sharing amongst the remaining healthy modules.

In comparison to the dedicated master-slave control strategy which responds appropriately only to slave module faults, these experimental results with the proposed 'non-dedicated master' control scheme show that it enables the converter being investigated to ride through fault conditions by permitting arbitrary reallocation of the role of 'master' to a healthy module. More importantly, this is achieved without any compromise to power sharing between the modules. However, to ensure the voltage and current stresses in each module, for constant load voltage, remain within the permissible range for continuous operation, both control strategies rely on the use of 'k' redundant modules to replace up to 'k' faulty modules from a total of '$n+k$' modules.

4.7 Summary

This chapter presents a robust control strategy suitable for MVDC applications that ensures equal power sharing between modules of the IPOS connected modular DC/DC converter when modules have parameter mismatches and module failures. Therefore, for medium-voltage application, modules will not be exposed to the risk of damage from over-voltages during transients. The nonlinear controller has an advantage over linear PI controller in terms of improved transient response and robustness to parameter variations. With regard to (n+1) redundancy, the commonly-used fixed 'master-slave' scheme has problems associated with ensuring (n+1) redundancy in the event of a fault in the master module. The proposed control scheme develops an enhanced controller based on the concept of the 'non-dedicated master' that permits arbitrary reallocation of the role of 'master' to another healthy module when the original master module fails. This allows fault-tolerant operation to be achieved independent of fault location without any compromise to power sharing between the modules. The viability of the control scheme has been confirmed through simulation and experimentation, where the results show that the converter system being studied exploits true (n+1) redundancy to maintain power balanced amongst the remaining healthy modules during internal faults. The converter

topology and control strategy can be readily extended to converters composed from any number of modules.

4.8 Chapter Reference

[1] R. Xinbo, C. Wu, C. Lulu, C. K. Tse, Y. Hong and Z. Tao, "Control Strategy for Input-Series&Output-Parallel Converters," Industrial Electronics, IEEE Transactions on, vol. 56, no. 4, pp. 1174-1185, 2009.

[2] S. Jianjiang, L. Jie and H. Xiangning, "Common-Duty-Ratio Control of Input-Series Output-Parallel Connected Phase-shift Full-Bridge DC/DC Converter Modules," Power Electronics, IEEE Transactions on, vol. 26, no. 11, pp. 3318-3329, 2011.

[3] C. Wu, R. Xinbo, Y. Hong and C. K. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," Power Electronics, IEEE Transactions on, vol. 24, no. 6, pp. 1463-1474, 2009.

[4] H. Yuehui, C. K. Tse and R. Xinbo, "General Control Considerations for Input-Series Connected DC/DC Converters," Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 56, no. 6, pp. 1286-1296, 2009.

[5] P. J. Grbovic, "Master/Slave Control of Input-Series- and Output-Parallel-Connected Converters: Concept for Low-Cost High-Voltage Auxiliary Power Supplies," Power Electronics, IEEE Transactions on, vol. 24, no. 2, pp. 316-328, 2009.

[6] R. Xinbo, C. Wu, C. Lulu, C. K. Tse, Y. Hong and Z. Tao, "Control Strategy for Input-Series & Output-Parallel Converters," Industrial Electronics, IEEE Transactions on, vol. 56, no. 4, pp. 1174-1185, 2009.

[7] S. Deshang, D. Kai and L. Xiaozhong, "Duty Cycle Exchanging Control for Input-Series-Output-Series Connected Two PS-FB DC-DC Converters," Power Electronics, IEEE Transactions on, vol. 27, no. 3, pp. 1490-1501, 2012.

[8] J. T. Matysik, "A New Method of Integration Control with Instantaneous Current Monitoring for Class D Series-Resonant Converter," Industrial Electronics, IEEE Transactions on, vol. 53, no. 5, pp. 1564-1576, 2006.

[9] A. A. Aboushady, "Design, Analysis and Modelling of Modular Medium-Voltage DC/DC Converter Based Systems," PhD thesis, Departement of Electronics and Electrical Engineering, University of Strathclyde, Glasgow, 2012.

[10] M. Castilla, L. Garcia de Vicuna, J. M. Guerrero, J. Matas and J. Miret, "Sliding-Mode Control of Quantum Series-Parallel Resonant Converters via Input-Output Linearization," Industrial Electronics, IEEE Transactions on, vol. 52, no. 2, pp. 566-575, 2005.

[11] J. Y. Hung, W. Gao and J. C. Hung, "Variable Structure Control: A Survey," Industrial Electronics, IEEE Transactions on, vol. 40, no. 1, pp. 2-22, 1993.

[12] Q. Wu, P. Sekhavat, S. Peles, R. F. Abo-Shanab and N. Sepehri, "An improved design procedure of Lyapunov feedback control," in Computational Intelligence in Robotics and Automation, Proceedings 2001 IEEE International Symposium on, pp. 486-491, 2001.

[13] M. Ghandhari, “Control Lyapunov functions: A control strategy for damping of power oscillations in large power systems,” Royal Institute of Technology, TRITA-EES-0004, ISSN 1100-1607, 2000.
[14] F. Clarke, "Lyapunov Functions and Feedback in Nonlinear Control," Optimal Control, Stabilization and Nonsmooth Analysis, Lecture Notes in Control and Information Science M. de Queiroz, M. Malisoff and P. Wolenski, eds., pp. 267-282: Springer Berlin Heidelberg, 2004.
[15] P. Parks, “Comment on "A new proof of the Routh-Hurwitz stability criterion by the second method of Lyapunov with applications to optimum transfer functions",” Automatic Control, IEEE Transactions on, vol. 9, no. 3, pp. 319-322, 1964.
[16] R. A. Rohrer and H. Nosrati, “A Modified Forward Euler Approach to Stable Step Response Computations,” Circuits and Systems, IEEE Transactions on, vol. 28, no. 3, pp. 180-186, 1981.
[17] K. B. Janiszowski, “A Modification and the Tustin Approximation,” Automatic Control, IEEE Transactions on, vol. 38, no. 8, pp. 1313-1316, 1993.
[18] E. I. Jury, “A Simplified Stability Criterion for Linear Discrete Systems,” Proceedings of the IRE, vol. 50, no. 6, pp. 1493-1500, 1962.
[19] K. D. Young, V. I. Utkin and U. Ozguner, “A Control Engineer's Guide to Sliding Mode Control,” in Variable Structure Systems, 1996. VSS '96. Proceedings., 1996 IEEE International Workshop on, pp. 1-14, 1996.
[20] P. F. Donoso-Garcia, P. C. Cortizo, B. R. de Menezes and M. A. Severo Mendes, “Sliding-Mode Control for Current Distribution in Parallel-Connected DC-DC Converters,” Electric Power Applications, IEE Proceedings -, vol. 145, no. 4, pp. 333-338, 1998.
[21] W. Junxiao, L. Shihua, Y. Jun, W. Bin and L. Qi, “Extended State Observer-based Sliding Mode Control for PWM-based DC&DC Buck Power Converter Systems with Mismatched Disturbances,” Control Theory & Applications, IET, vol. 9, no. 4, pp. 579-586, 2015.
[22] T. Siew-Chong, Y. M. Lai and C. K. Tse, “General Design Issues of Sliding-Mode Controllers in DC&DC Converters,” Industrial Electronics, IEEE Transactions on, vol. 55, no. 3, pp. 1160-1174, 2008.
[23] H. Sira-Ramirez and M. Rios-Bolivar, “Sliding Mode Control of DC-to-DC Power Converters via Extended Linearization,” Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on, vol. 41, no. 10, pp. 652-661, 1994.
[24] Y. He and F. L. Luo, “Sliding-Mode Control for DC-DC Converters with Constant Switching Frequency,” Control Theory and Applications, IEE Proceedings -, vol. 153, no. 1, pp. 37-45, 2006.
[25] S. Maity, “Dynamics and Stability Issues of a Discretized Sliding-Mode Controlled DC-DC Buck Converter Governed by Fixed-Event-Time Switching,” Circuits and Systems I: Regular Papers, IEEE Transactions on, vol. 60, no. 6, pp. 1657-1669, 2013.
[26] A. Dashtestani and B. Bakkaloglu, “A Fast Settling Oversampled Digital Sliding-Mode DC&DC Converter,” Power Electronics, IEEE Transactions on, vol. 30, no. 2, pp. 1019-1027, 2015.

[27] M. Lopez, L. G. de Vicuna, M. Castilla, P. Gaya and O. Lopez, "Current Distribution Control Design for Paralleled DC/DC Converters using Sliding-Mode Control," Industrial Electronics, IEEE Transactions on, vol. 51, no. 2, pp. 419-428, 2004.

[28] J. F. Tsai and Y. P. Chen, "Sliding Mode Control and Stability Analysis of Buck DC-DC Converter," International Journal of Electronics, vol. 94, no. 3, pp. 209-222, 2007/03/01, 2007.

[29] İ. Eker, "Sliding mode control with PID sliding surface and experimental application to an electromechanical plant," ISA Transactions, vol. 45, no. 1, pp. 109-118, 2006.

[30] V. Choudhary, E. Ledezma, R. Ayyanar and R. M. Button, "Fault Tolerant Circuit Topology and Control Method for Input-Series and Output-Parallel Modular DC-DC Converters," Power Electronics, IEEE Transactions on, vol. 23, no. 1, pp. 402-411, 2008.

[31] S. K. Mazumder, M. Tahir and K. Acharya, "Master&Slave Current-Sharing Control of a Parallel DC/DC Converter System Over an RF Communication Interface," Industrial Electronics, IEEE Transactions on, vol. 55, no. 1, pp. 59-66, 2008.

Chapter 5: ISIPOS Connected Modular DC/DC Converter

This chapter presents a novel configuration of modular DC/DC converter that consists of *n* phase shifted full-bridge modules, whose inputs are input-series-input-parallel connected, whilst the outputs are series connected. Having introduced the proposed power converter concept, power sharing issues in input-series-input-parallel output-series (ISIPOS) connected modular DC/DC converter are examined. Following that, the design of the control topology is given. In addition, the performance of the proposed control scheme in terms of power sharing ability are compared with that of the widely-used common duty-cycle control approach, and both simulation and experimental results are presented to test the viability of the different control schemes. Moreover, its fault-tolerant operation is highlighted, and performance regarding the fault detection and redundancy of the proposed converter are validated through application-level simulations and scaled-down experiments.

5.1 ISIPOS Connection Background

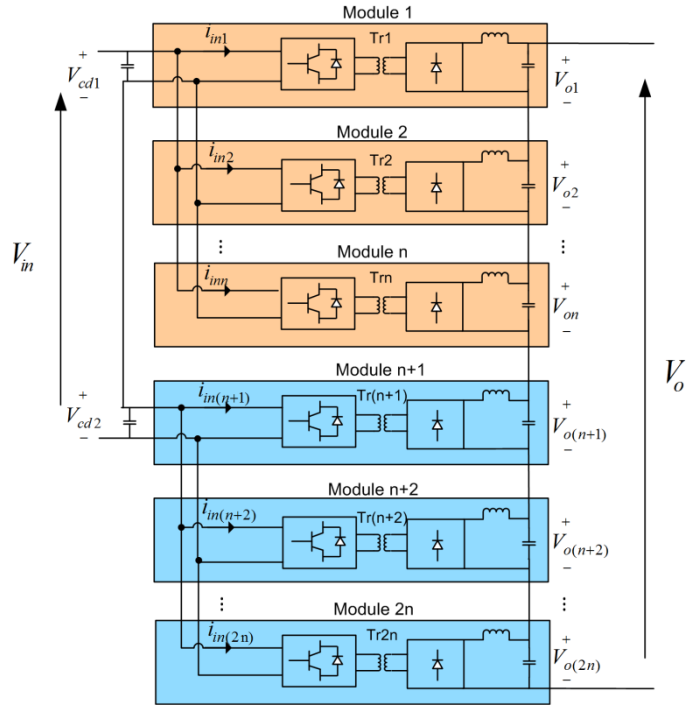


Fig.5.1: ISIPOS converter topology with full-bridge DC/DC modules

Fig.5.1 shows the structure of a 2*n*-module ISIPOS DC/DC converter with two parallel arms (each has *n* modules) being series connected at the front end, where the number of parallel and series connected modules can be extended to any number according to the application requirements.

Input-series-input-parallel connection of the modules allows reduction of the current and voltage stresses in the power devices, thereby enabling device ratings and switching frequency to be further optimised compared with input-parallel connection. With output-series connection, the turns-ratios of the isolation transformers can be reduced, leading to a reduction in leakage inductance. Additionally, ISIPOS connection presents a number of attractive properties: each module only contributes a small fraction of the total power and operates at voltages and currents that can be supported by current device rating; the modular structure allows the converter to be re-configured and higher switching frequency can be achieved without significant design challenges; and redundant cells in this modular configuration provide fault ride-through operation [1-3].

5.2 Power Sharing Issue with ISIPOS Connected Modular DC/DC Converter

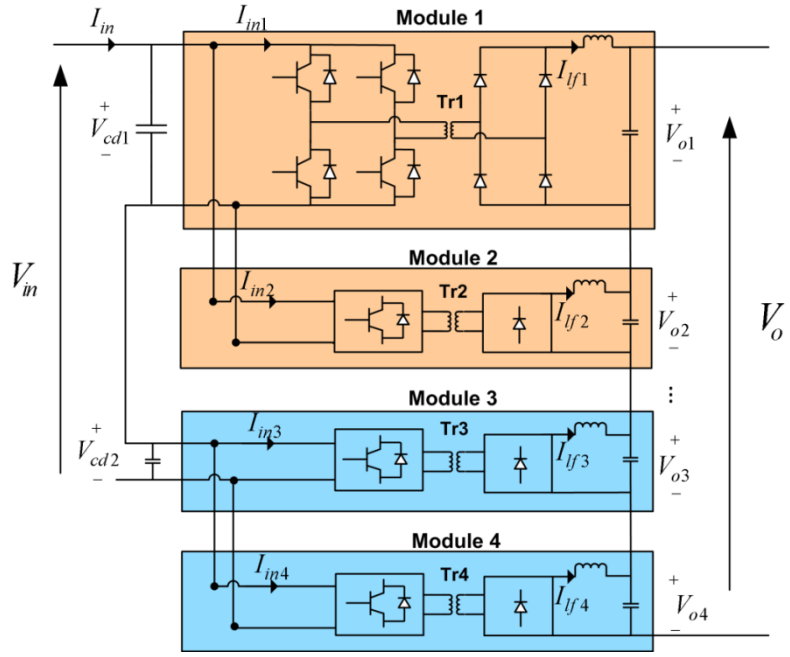


Fig.5.2: ISIPOS connected 4-module system

Fig.5.2 shows an illustrative schematic diagram of the 4-module ISIPOS DC/DC converter that forms the basis of the study, where n=2 in Fig.5.1. Assuming all four modules in Fig.5.2 are lossless, the relationships between the input and output powers of each module can be expressed as (5.1),

$$\begin{cases} V_{cd1} I_{in1} = V_{o1} I_o \\ V_{cd1} I_{in2} = V_{o2} I_o \\ V_{cd2} I_{in3} = V_{o3} I_o \\ V_{cd2} I_{in4} = V_{o4} I_o \end{cases} \tag{5.1}$$

where V_{cd1} is the DC input voltage for modules 1 and 2 due to the parallel connection; V_{cd2} is similarly the DC input voltage for Modules 3 and 4, I_{in1}, I_{in2},…,I_{in4} are input currents to modules 1 to 4, V_{o1},V_{o2},…,V_{o4} are output voltages from modules 1 to 4; I_{lf1}, I_{lf2},…, I_{lf4} are output inductance currents in modules 1 to 4, and I_o is load current. In the steady-state condition, the average filter capacitor current is zero, and therefore output filter inductor currents are identical except for a small ripple component. If

output voltage sharing (OVS) is achieved, then $V_{o1}=V_{o2}=V_{o3}=V_{o4}$. Substituting this result into (5.1) yields (5.2).

$$V_{cd1}I_{in1}=V_{cd1}I_{in2}=V_{cd2}I_{in3}=V_{cd2}I_{in4} \tag{5.2}$$

Equation (5.2) implies that $I_{in1}=I_{in2}$ and $I_{in3}=I_{in4}$. In addition, due to the input series connection, $I_{in1}=I_{in3}=I_{in2}=I_{in4}=½I_{in}$ can be derived, which lead to $V_{cd1}=V_{cd2}$. It should be noted that input power balancing can be achieved as long as OVS is achieved under steady-state conditions. Alternatively, if all modules share the same input power, which means modules 1 and 2 (similarly for modules 3 and 4) share the same input current and modules 1 and 3 share the same input voltage, OVS can be achieved. However, input voltage sharing control is indispensable in managing disturbances in input-series connection systems for transient conditions [3-7]. One effective way of finding the relationship between the input and output power stages, and control requirement of the proposed ISIPOS connected modular converter, is to investigate the consequences of input and output side control strategies.

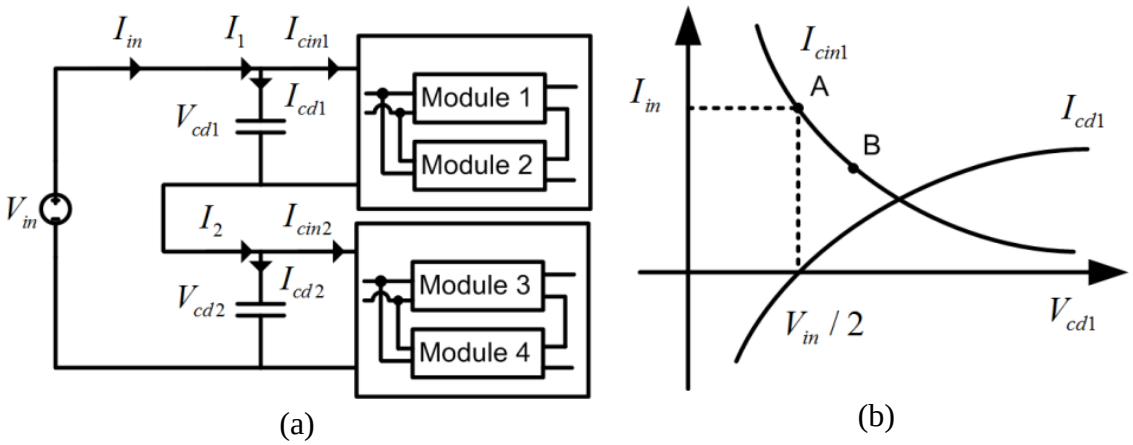
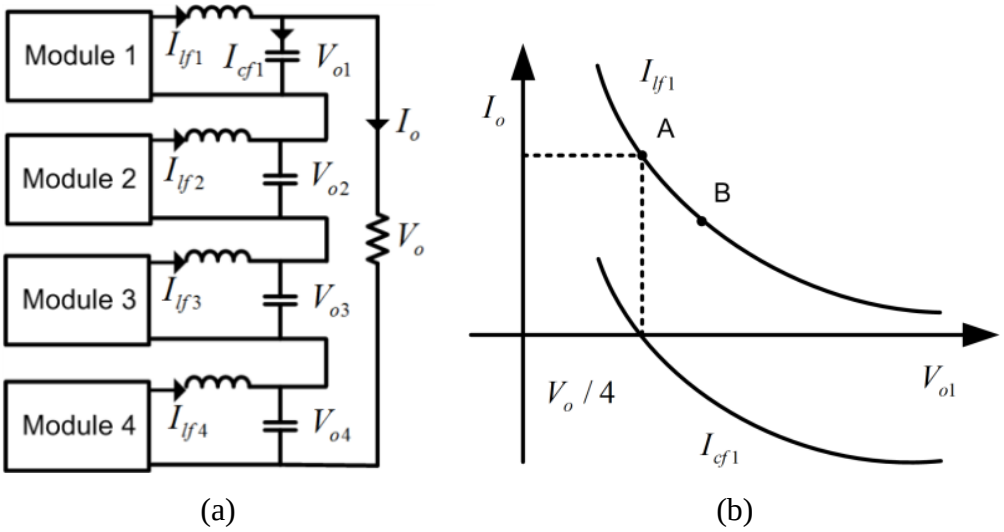


Fig.5.3: ISIPOS DC/DC converter (a) output side control and (b) operating point

The schematic diagram of Fig.5.3 (a) illustrates application of an output side control strategy to the proposed converter. OVS is achieved through output side control, where the module behaves as a constant power sink seen from the input side, with constant output current and equally shared output voltages. Thus, any increase of V_{cd1} leads to a decrease of I_{cin1}, so that system equilibrium operating point moves from A to B, as shown in Fig.5.3 (b). At point B, I_{cin1} is smaller than input current I_{in} so that input filter capacitor current I_{cd1} becomes positive, which further increases V_{cd1}. Therefore, the equilibrium point cannot be resumed as the increase in input voltage

V_{in1} leads to further increase of itself, eventually leading to a runaway condition between V_{cd1} and V_{cd2}. This means that any input disturbance may result in an inversely proportional current-voltage relationship. OVS cannot therefore provide input power sharing for the input-series stage, as shown in Fig.5.3 (a) and (b).



(a) (b)

Fig.5.4: ISIPOS DC/DC converter (a) input side control and (b) operating point

Fig.5.4 (a) and (b) highlight the consequences of input side control. Modules behave as constant power sources seen from the output side, with equally shared input voltage and current. Thus, an increase in V_{o1} leads to a decrease in I_{lf1} which drives the system from the equilibrium operating point A to B, as shown in Fig.5.4 (b). Now, I_{lf1} is smaller than load current I_o, so that current I_{cf1} becomes negative, discharging the capacitor and driving the operating point back to A. Input side control can therefore lead to power balance in the converter.

To realise input side control, a dedicated input voltage control loop is essential for stable operation of the input-series stage. For the input-parallel connection, however, modules can be balanced either by input current balancing or by output voltage balancing [3, 8]. Due to discontinuity of the input current, output voltage balancing control is used for the parallel-connected modules to avoid the need for high-cost, high-bandwidth current transducers. To build the proposed control strategy, small-signal analysis is necessary and is described in the following section.

5.3 Novel Control Strategy in Normal Operation

5.3.1 Small-Signal Modelling for ISIPOS Connected Four-module Converter

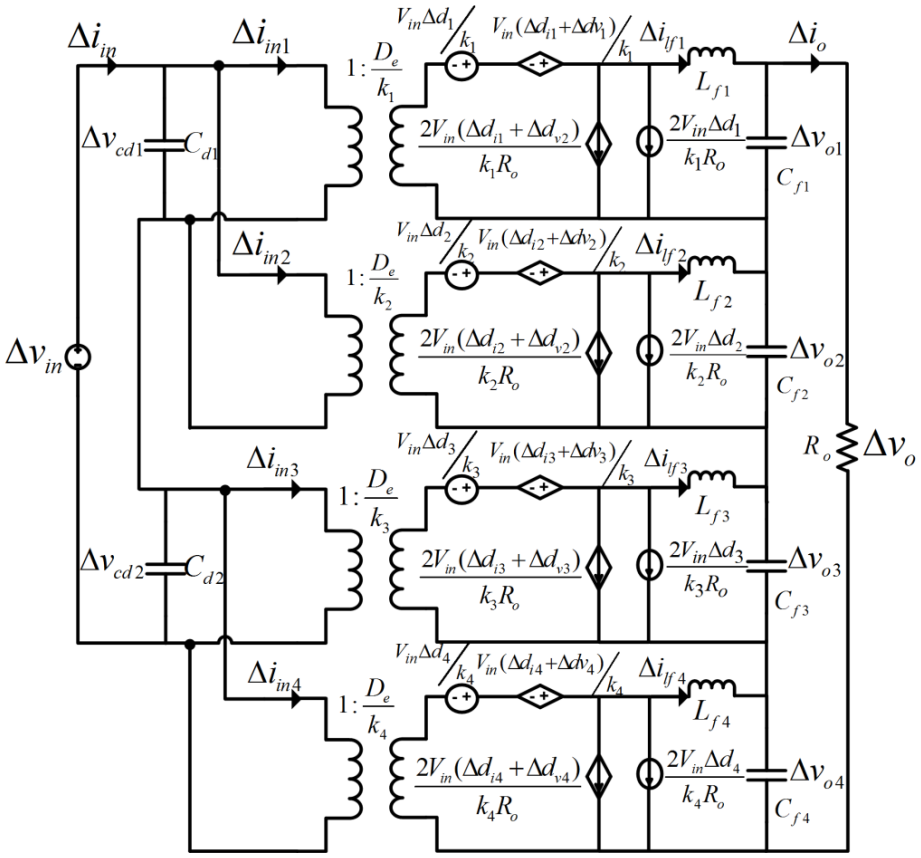


Fig.5.5: Small-signal equivalent circuit of the ISIPOS connected 4-module converter

The small-signal model of the 4-module ISIPOS connected DC/DC converter shown in Fig.5.5 is built based upon a single module converter model [2], where k_1, k_2, k_3 and k_4 are transformer turns ratios, D_e is the effective duty cycle per module, and L_{f1}, L_{f2}, L_{f3}, L_{f4}, C_{f1}, C_{f2}, C_{f3} and C_{f4} are filter inductances and capacitances for the four modules. Input voltage perturbation is represented by Δv_{in}, input voltage perturbation components for modules 1 and 2, and for modules 3 and 4 are Δv_{cd1} and Δv_{cd2} respectively, input current perturbations for the four modules are Δi_{in1}, Δi_{in2}, Δi_{in3} and Δi_{in4} respectively, and filter inductor current and capacitor voltage perturbations are represented by Δi_{lf1}, Δi_{lf2}, Δi_{lf3}, Δi_{lf4}, and Δv_{o1}, Δv_{o2}, Δv_{o3} and Δv_{o4} respectively. Δd_1, Δd_2, Δd_3 and Δd_4 are the duty cycle perturbations, and Δd_{v1}, Δd_{v2}, Δd_{v3}, Δd_{v4}, Δd_{i1}, Δd_{i2},

Δd_{i3} and Δd_{i4} represent perturbations of the duty cycle due to the input voltage and output current, as defined in (5.3),

$$\begin{cases} \Delta d_{v1} = \Delta d_{v2} = \dfrac{32 L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{cd1} \\ \Delta d_{v3} = \Delta d_{v4} = \dfrac{32 L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{cd2} \\ \Delta d_{ij} = -\dfrac{8 L_r f_s}{k V_{in}} \Delta i_{lfj} \end{cases} \tag{5.3}$$

where j=1, 2, 3 and 4 and L_r is the transformer leakage inductance,.

To simplify the analysis, it is assumed that four modules have the same effective duty cycles, transformer turns-ratios, and capacitor and inductor values [6]. The corresponding equations, produced by application of KVL in Fig.5.5, are shown in (5.4). The KCL equations for the output side, comprising the output impedance perturbation $\Delta V_o/\Delta R_o$ contributed as Δi_o, are given by (5.5).

$$\begin{cases} \dfrac{D_e \Delta v_{cd1}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) = s L_f \Delta i_{lf1} + \Delta v_{o1} \\ \dfrac{D_e \Delta v_{cd1}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = s L_f \Delta i_{lf2} + \Delta v_{o2} \\ \dfrac{D_e \Delta v_{cd2}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_3 + \Delta d_{v3} + \Delta d_{i3}\right) = s L_f \Delta i_{lf3} + \Delta v_{o3} \\ \dfrac{D_e \Delta v_{cd2}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_4 + \Delta d_{v4} + \Delta d_{i4}\right) = s L_f \Delta i_{lf4} + \Delta v_{o4} \end{cases} \tag{5.4}$$

$$\begin{cases} \Delta i_{lf1} + \Delta i_o = s C_f \Delta v_{o1} + \dfrac{\Delta v_o}{R_o} \\ \Delta i_{lf2} + \Delta i_o = s C_f \Delta v_{o2} + \dfrac{\Delta v_o}{R_o} \\ \Delta i_{lf3} + \Delta i_o = s C_f \Delta v_{o3} + \dfrac{\Delta v_o}{R_o} \\ \Delta i_{lf4} + \Delta i_o = s C_f \Delta v_{o4} + \dfrac{\Delta v_o}{R_o} \end{cases} \tag{5.5}$$

Adding the four expressions defined in (5.4) and substituting (5.3) into the result with the assumption that Δv_{cd1}=Δv_{cd2}=Δv_{in}/2 yields (5.6).

$$\Delta v_{in}(\frac{2D_e}{k}+\frac{32L_rD_ef_s}{k^3R_o})+\frac{V_{in}}{2k}\left(\Delta d_1+\Delta d_2+\Delta d_3+\Delta d_4\right)= \\ (sL_f+\frac{4L_rf_s}{k^2})(\Delta i_{lf1}+\Delta i_{lf2}+\Delta i_{lf3}+\Delta i_{lf4})+\Delta v_o \tag{5.6}$$

Assuming $\Delta v_{in}=0$ and $\Delta d_j=0$, (5.6) leads to (5.7) (j=1, 2, 3 and 4).

$$(sL_f+\frac{4L_rf_s}{k^2})(\Delta i_{lf1}+\Delta i_{lf2}+\Delta i_{lf3}+\Delta i_{lf4})+\Delta v_o=0 \tag{5.7}$$

Adding (5.5) yields (5.8).

$$\Delta i_{lf1}+\Delta i_{lf2}+\Delta i_{lf3}+\Delta i_{lf4}+4\Delta i_o=sC_f(\Delta v_{o1}+\Delta v_{o2}+\Delta v_{o3}+\Delta v_{o4})+\frac{4\Delta v_o}{R_o} \tag{5.8}$$

Recognizing that $\Delta v_{o1}+\Delta v_{o2}+\Delta v_{o3}+\Delta v_{o4}=\Delta v_o$, and substituting (5.8) into (5.7), the relationship between voltage output and current output is obtained as (5.9).

$$G_{ovi}=\frac{\Delta v_o}{\Delta i_o}=\frac{4L_fs+\frac{16L_rf_s}{k^2}}{s^2L_fC_f+s(\frac{4L_f}{R_o}+\frac{4L_rf_sC_f}{k^2})+1+\frac{16L_rf_s}{k^2R_o}} \tag{5.9}$$

Assuming $\Delta v_{in}=0$ and $\Delta d_k=0$ (k=1, 2, 3 and 4, and $k\neq j$) and substituting (5.3) into (5.6), the relationship between voltage output and duty cycle can be represented as (5.10), and the relationship between output current and duty cycle can be represented as (5.11).

$$G_{ovd}=\frac{\Delta v_o}{\Delta d_j}=\frac{V_{in}}{2k[s^2L_fC_f+s(\frac{4L_f}{R_o}+\frac{4L_rf_sC_f}{k^2})+1+\frac{16L_rf_s}{k^2R_o}]} \tag{5.10}$$

$$G_{oid}=\frac{\Delta i_o}{\Delta d_j}=\frac{V_{in}}{2k[s^2L_fC_fR_o+4L_fs+\frac{4L_rf_sC_fR_o}{k^2}s+R_o+\frac{16L_rf_s}{k^2}]} \tag{5.11}$$

Equations (5.10) and (5.11) are used in designing individual module output voltage and inner current controllers respectively. Considering the series pair of modules 1 and 3, (5.12) can be derived from Fig.5.5.

$$\begin{cases} \dfrac{k}{D_e}(\Delta i_{in} - sC_d\Delta v_{cd1}) = \dfrac{2V_{in}}{kR_o}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) + \Delta i_{lf1} \\ \dfrac{k}{D_e}(\Delta i_{in} - sC_d\Delta v_{cd2}) = \dfrac{2V_{in}}{kR_o}\left(\Delta d_3 + \Delta d_{v3} + \Delta d_{i3}\right) + \Delta i_{lf3} \end{cases} \tag{5.12}$$

Neglecting duty cycle perturbations due to input voltage and output current, subtraction of the two equations in (5.12) leads to (5.13). Subtraction of the first and third equations in (5.4) leads to (5.14), and from (5.5) the modular voltage and current relationship can be obtained as (5.15).

$$\frac{k}{D_e}sC_d(\Delta v_{cd2} - \Delta v_{cd1}) = \frac{2V_{in}}{kR_o}\left(\Delta d_1 - \Delta d_3\right) + \Delta i_{lf1} - \Delta i_{lf3} \tag{5.13}$$

$$\frac{D_e}{k}(\Delta v_{cd2} - \Delta v_{cd1}) + \frac{V_{in}}{2k}\left(\Delta d_3 - \Delta d_1\right) = s\mathrm{L}_f(\Delta i_{lf3} - \Delta i_{lf1}) + \Delta v_{o3} - \Delta v_{o1} \tag{5.14}$$

$$\begin{cases} \Delta v_{o1} = \dfrac{1}{sC_f}\left(\Delta i_{lf1} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \\ \Delta v_{o2} = \dfrac{1}{sC_f}\left(\Delta i_{lf2} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \\ \Delta v_{o3} = \dfrac{1}{sC_f}\left(\Delta i_{lf3} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \\ \Delta v_{o4} = \dfrac{1}{sC_f}\left(\Delta i_{lf4} - \dfrac{\Delta v_{o1} + \Delta v_{o2} + \Delta v_{o3} + \Delta v_{o4}}{R_o}\right) \end{cases} \tag{5.15}$$

Rearranging (5.15), the relationship between modular voltage output and inductor current can be represented as (5.16),

$$\begin{cases} \Delta v_{o1} = g_1\Delta i_{lf1} - g_2\left(\Delta i_{lf2} + \Delta i_{lf3} + \Delta i_{lf4}\right) \\ \Delta v_{o2} = g_1\Delta i_{lf2} - g_2\left(\Delta i_{lf1} + \Delta i_{lf3} + \Delta i_{lf4}\right) \\ \Delta v_{o3} = g_1\Delta i_{lf3} - g_2\left(\Delta i_{lf1} + \Delta i_{lf2} + \Delta i_{lf4}\right) \\ \Delta v_{o4} = g_1\Delta i_{lf4} - g_2\left(\Delta i_{lf1} + \Delta i_{lf2} + \Delta i_{lf3}\right) \end{cases} \tag{5.16}$$

where

$$\begin{cases} g_1 = \dfrac{sC_f R_o + 3}{s^2 C_f{}^2 R_o + 4sC_f} \\ g_2 = \dfrac{1}{s^2 C_f{}^2 R_o + 4sC_f} \end{cases} \tag{5.17}$$

Substituting (5.17) into (5.14) yields (5.18).

$$\begin{aligned} &\frac{D_e}{k}(\Delta v_{cd2} - \Delta v_{cd1}) + \frac{V_{in}}{2k}\left(\Delta d_3 - \Delta d_1\right) \\ &= (sL_f + g_1 + g_2)(\Delta i_{lf3} - \Delta i_{lf1}) + \Delta v_{o3} - \Delta v_{o1} \end{aligned} \tag{5.18}$$

Substituting (5.18) into (5.14) yields (5.19).

$$\frac{\Delta v_{cd1} - \Delta v_{cd2}}{\Delta d_1 - \Delta d_3} = \frac{-\dfrac{2V_{in}}{kR_o}(g_2 + g_1 + sL_f) - \dfrac{V_{in}}{2k}}{\dfrac{D_e}{k} + sCd\,\dfrac{k}{D_e}(g_1 + sL_f + g_2)} \tag{5.19}$$

This can be rewritten as (5.20),

$$\Delta v_{cd2} = \Delta v_{cd1} + A(s)(\Delta d_3 - \Delta d_1) \tag{5.20}$$

where

$$A(s) = -\frac{\dfrac{2V_{in}}{kR_o}(g_2 + g_1 + sL_f) + \dfrac{V_{in}}{2k}}{\dfrac{D_e}{k} + sCd\,\dfrac{k}{D_e}(g_1 + sL_f + g_2)} \tag{5.21}$$

Assuming that Δv_{in}=0 and Δv_{cd1}=-Δv_{cd2}, the relationship between input capacitor voltage and duty cycle is obtained as (5.22).

$$\begin{bmatrix} \Delta v_{cd1} \\ \Delta v_{cd2} \end{bmatrix} = \begin{bmatrix} \dfrac{A(s)}{2} & -\dfrac{A(s)}{2} \\ -\dfrac{A(s)}{2} & \dfrac{A(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_3 \end{bmatrix} \tag{5.22}$$

The transfer function described in (5.22) is used in designing the input voltage sharing controller. If input current control is required, the relationship between input current and duty cycle shown in (5.23) can be used,

$$\begin{bmatrix}\Delta i_{in1}\\ \Delta i_{in2}\end{bmatrix}=\begin{bmatrix}\frac{B(s)}{2} & -\frac{B(s)}{2}\\ -\frac{B(s)}{2} & \frac{B(s)}{2}\end{bmatrix}\begin{bmatrix}\Delta d_1\\ \Delta d_2\end{bmatrix}$$
$$\begin{bmatrix}\Delta i_{in3}\\ \Delta i_{in4}\end{bmatrix}=\begin{bmatrix}\frac{B(s)}{2} & -\frac{B(s)}{2}\\ -\frac{B(s)}{2} & \frac{B(s)}{2}\end{bmatrix}\begin{bmatrix}\Delta d_3\\ \Delta d_4\end{bmatrix} \quad (5.23)$$

where

$$B(s)=D_e(\frac{2V_{in}}{R_o}+g_3-g_4)$$
$$\begin{cases} g_3=\dfrac{ac-2bc}{(a+b)(a-3b)} \\ g_4=\dfrac{bc}{(a+b)(a-3b)} \end{cases} \quad (5.24)$$
$$\begin{cases} a=sL_f+\dfrac{sC_f R_o+3}{s^2 C_f{}^2 R_o+4sC_f}+\dfrac{4L_r f_s}{k^2} \\ b=-\dfrac{1}{s^2 C_f{}^2 R_o+4sC_f} \\ c=\dfrac{V_{in}}{2k} \end{cases}$$

5.3.2 Lyapunov Controller Design and Stability Criteria Analysis

It has been established in Chapter 4 that a Lyapunov controller is capable of robust performance in response to load, input and other parameter variations. For an ISIPOS connected modular DC/DC converter, it has been introduced to control the output voltage. A novel linearised equivalent large-signal model of ISIPOS connected modular DC/DC converter incorporating closed-loop output voltage control is presented in Fig.5.6, which provides a linear representation of converter behavior under large-signal variation for faster control response and better disturbance rejection capability.

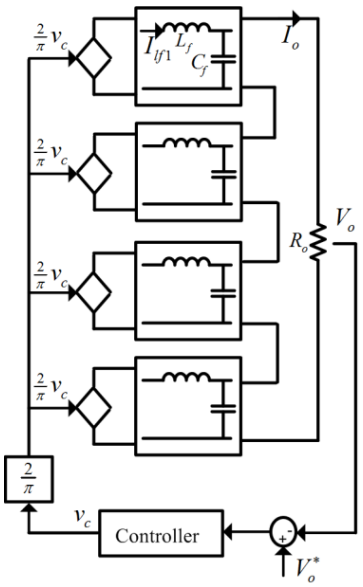


Fig.5.6: Reduced equivalent model for the ISIPOS DC/DC 4-module system

From Fig.5.6, the transfer function for ISIPOS converter can be derived as (5.25),

$$G_{oc} = \frac{V_o(s)}{v_c(s)} = \frac{8}{\pi} \frac{1}{L_f C_f s^2 + 1} \tag{5.25}$$

where $\bar{v}_{rec}$ is the average value of the voltage at the input to the LC filter tank.

The objective is to control the ISIPOS DC/DC converter output voltage error as defined in (5.26).

$$e = V_o^* - V_o \tag{5.26}$$

A function $r = \dot{e} + ae$ is defined, where α is an arbitrary real constant. A control-Lyapunov candidate $v(x)$ is then as in (5.27), which is positive definite for all $V_o^* \neq 0$ and $V_o \neq 0$. Its derivative is given in (5.28), where k is strictly a positive proportionality constant [9]. Substituting (5.28) into (5.27) yields (5.29).

$$v = \frac{1}{2} r^2 \tag{5.27}$$

$$\dot{v} = (\dot{e} + \alpha e)(\ddot{e} + \alpha \dot{e}) = -kv < 0 \tag{5.28}$$

$$(\ddot{e} + \alpha \dot{e}) = -\frac{1}{2} \beta (\dot{e} + \alpha e) \tag{5.29}$$

From Fig.5.6, (5.30) and (5.31) can be derived. Control variable v_c can then be explicitly included in the second order transfer function of the output voltage (5.32).

$$\frac{dI_{lf1}}{dt} = \frac{1}{L_f}(\frac{2}{\pi}v_c - \frac{1}{4}V_o) = \frac{1}{L_f}(\frac{2}{\pi}v_c - V_{o1}) \tag{5.30}$$

$$\frac{dV_{o1}}{dt} = \frac{1}{4}\frac{dV_o}{dt} = \frac{1}{C_f}(I_{lf1} - I_o) = \frac{1}{C_f}(I_{lf1} - \frac{V_o}{R_o}) \tag{5.31}$$

$$\ddot{V}_o = \frac{1}{C_f}(\frac{8v_c}{L_f\pi} - \frac{V_o}{L_f} - \frac{4\dot{V}_o}{R_o}) \tag{5.32}$$

Assuming V_o^* to be constant, $\dot{e} = -\dot{V}_o$ and $\ddot{e} = -\ddot{V}_o$. Substituting these results into (5.29) gives (5.33). This, in turn, yields (5.34).

$$\ddot{V}_o = \frac{\alpha k}{2}(V_o^* - V_o) - \frac{k}{2}\dot{V}_o - \alpha\dot{V}_o \tag{5.33}$$

$$v_c = \frac{\alpha k C_f L_f \pi}{16}e + \frac{C_f L_f \pi}{8}(\frac{k}{2} + \alpha - \frac{4}{R_o C_f})\dot{e} + \frac{\pi}{8}V_o \tag{5.34}$$

Notice that the first and second terms of (5.34) imply that a PD controller is sufficient to ensure stability of the overall output voltage, where '*e*' will decay to 0 as the system output voltage V_o converges to its desired reference set point. The $\pi V_o/8$ feed-forward term improves disturbance rejection and initial transient during start-up. Therefore, (5.34) can be rewritten as (5.35).

$$v_c = k_p e + k_d \dot{e} + \frac{\pi}{8}V_o \tag{5.35}$$

Using the same method as shown in the previous chapter, the Routh-Hurwitz stability criterion demonstrates that if proportional and derivative gains k_p and k_d are both positive, the system is stable.

5.3.3 Overall Control Strategy

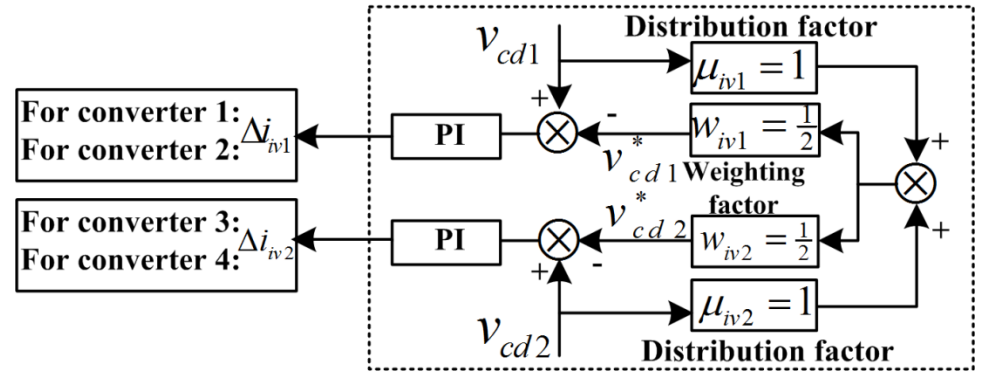
It was discussed previously that in order to ensure safe, reliable and stable operation in the presence of internal parameter mismatches and external transients, dedicated power balancing control which provides power balance amongst all the modules is indispensable for ISIPOS connecte a modular DC/DC converter control. This study proposes a dedicated power sharing control scheme, which involves input voltage sharing between input-series output-series connected modules to correct the

differences between these modules, e.g. modules 1 and 3 in Fig.5.2, and output voltage sharing to manage disturbances between input-parallel output-series connected modules, e.g. modules 1 and 2 or modules 3 and 4 in Fig.5.2.

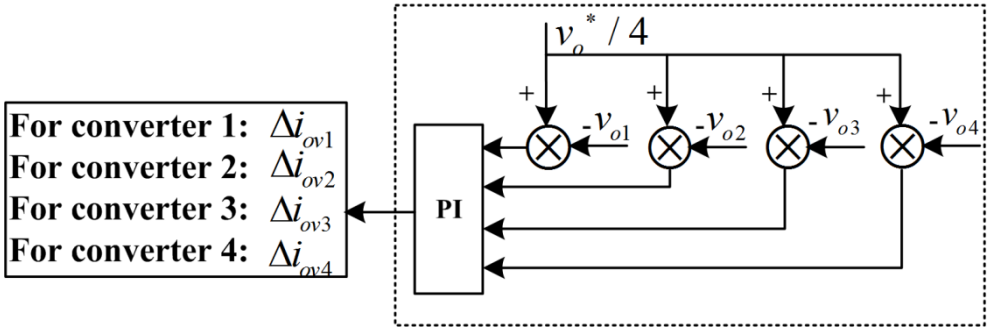
For input-series connected modules, input capacitor voltages V_{cd1} and V_{cd2} are sensed. Input voltage sharing reference signals for the modules are generated using distribution factors μ_{iv1}, and μ_{iv2} which, in this case, define the proportions of voltages V_{cd1} and V_{cd2}, and weighting factors W_{iv1}, and W_{iv2} which are the multiplying factors used in the calculation shown in Fig.5.7 (a). Average active sharing is used so that $\mu_{iv1}=\mu_{iv2}=1$ and $W_{iv1}= W_{iv2}=1/2$. The voltage reference for the modules is therefore given by (5.36). Alternatively, a fixed voltage reference of $V_{in}/2$ could be used. The main advantage of using the dynamic voltage reference in (5.36) rather than a fixed voltage reference is that it minimizes the interaction amongst the different control loops and results in better transient performance [10]. Average output voltage sharing is implemented by correcting the voltage difference signals to generate inductor current contributions Δi_{iv1} for modules 1 and 2, and Δi_{iv2} for modules 3 and 4.

$$v_{ref} = \frac{v_{o1} + v_{o2}}{2} \tag{5.36}$$

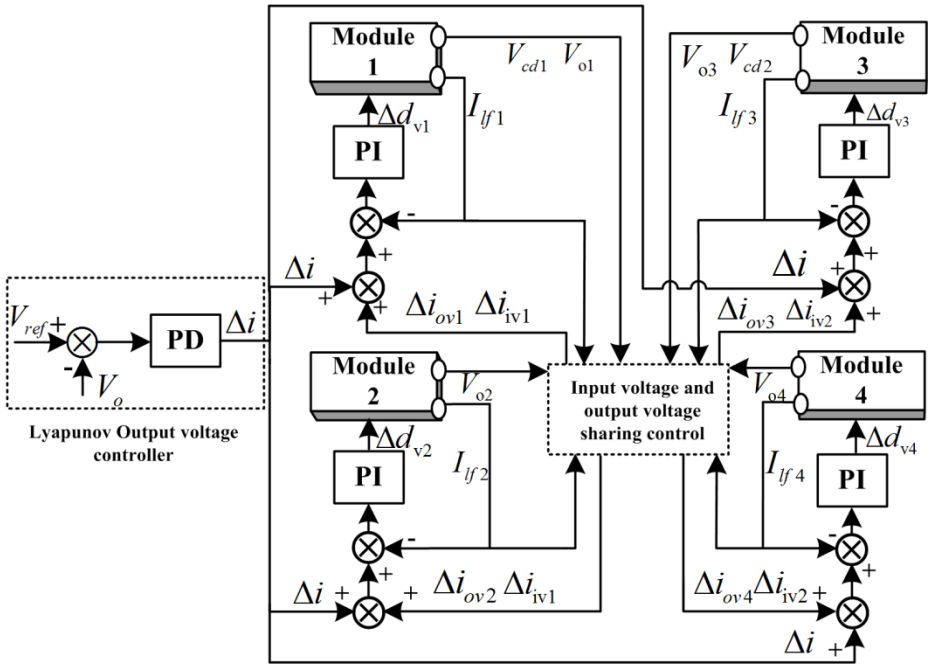
Fig.5.7 (b) shows the output voltage sharing controller that ensures input power sharing between the parallel-connected modules. After sensing the module output voltages, the controller compensates for any disturbance in the converter by minimising the differences between the individual module outputs and $V_o^*/2n$, where in this case n=2, to generate inductor current contributions Δi_{ov1}, Δi_{ov2}, Δi_{ov3} and Δi_{ov4}.



(a)



(b)



(c)

Fig.5.7: ISIPOS DC/DC converter (a) input voltage sharing controller (b) output voltage sharing controller (c) overall control

As shown in Fig.5.7 (c), the Lyapunov controller contributes the main current signal Δi to all modules using the procedure described in the previous section to control the output voltage. During normal operation, the majority of the reference currents to the current controllers will be contributed from the individual PI output voltage controllers of Fig.5.7 (b), with a contribution from the PD output voltage controller of Fig.5.7 (c), as each individual module output voltage controller tracks its set-point with zero steady-state error, and a contribution from the PI input voltage sharing control loop of Fig.5.7 (a) which has been limited. However, it should be noted that the overall output voltage control loop that uses PD control plays the most crucial role should some of the modules fail and during other major transient events. Referring to Fig.5.7 (c), the current contributions produced by the three controllers shown in Fig.5.7 are summed to provide the module current reference in (5.37). Individual inner current control loops, which are capable of guaranteeing current performance, are added to obtain the duty cycle contributions from current references Δi_1, Δi_2, Δi_3 and Δi_4 generated in (5.37).

$$\begin{cases} \Delta i_1 = \Delta i + \Delta i_{ov1} + \Delta i_{iv1} \\ \Delta i_2 = \Delta i + \Delta i_{ov2} + \Delta i_{iv1} \\ \Delta i_3 = \Delta i + \Delta i_{ov3} + \Delta i_{iv2} \\ \Delta i_4 = \Delta i + \Delta i_{ov4} + \Delta i_{iv2} \end{cases} \tag{5.37}$$

The proposed control strategy is assessed by considering the impact of mismatches between the modules, and transient operating conditions in ISIPOS connected modular DC/DC converter. Both simulation and experimental results are presented in the following section to examine and verify its performance in the context of parameter mismatch and transience.

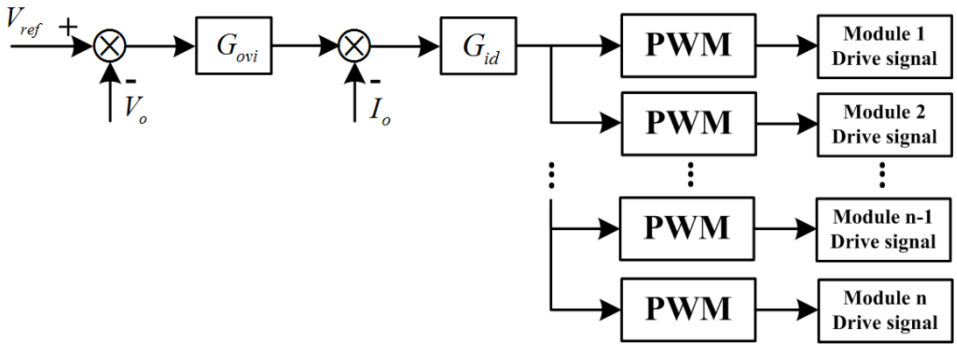


Fig.5.8: Common duty-cycle control

To assess the performance improvement offered when the converter is regulated using the proposed control scheme, results are compared with those obtained from the widely used common duty-cycle control scheme [11, 12] shown in Fig.5.8.

5.3.4 Simulation Validation of Normal Operation

For simulation verification, the ISIPOS connected modular DC/DC converter, shown in Fig.5.2, consists of 4-module with a nominal rating of 1 MW in total. To test the power balancing ability of the proposed control strategy when coping with uncertainties, some component parameters are purposely assumed to be different. Parameter mismatches, including input capacitance, transformer turns-ratios, and output inductances and capacitances, as specified in Table 5.1 are introduced.

Table 5.1: List of parameters for ISIPOS connected 4-module DC/DC converter

Parameter	***Experimental Values***	***Parameter***	***Experimental Values***
Converter Rated Power	1 MW	Transformer Turns-Ratio	T_1 =1:6.8 T_2 =1:6.4 T_3 =1:6 T_4 =1:6.4
Number of Modules	4		
Input DC Voltage	2200 V	Output Inductance	L_1 =50 mH L_2 =60 mH L_3 =50 mH L_4 =60 mH
Output DC Voltage	22.5 kV		
PWM Carrier Frequency	2.5 kHz	Output Capacitance	C_1 =300 μF C_2 =350 μF C_3 =300 μF C_4 =330 μF
Input Capacitance	C_{d1} =50 μF C_{d2} =80 μF		

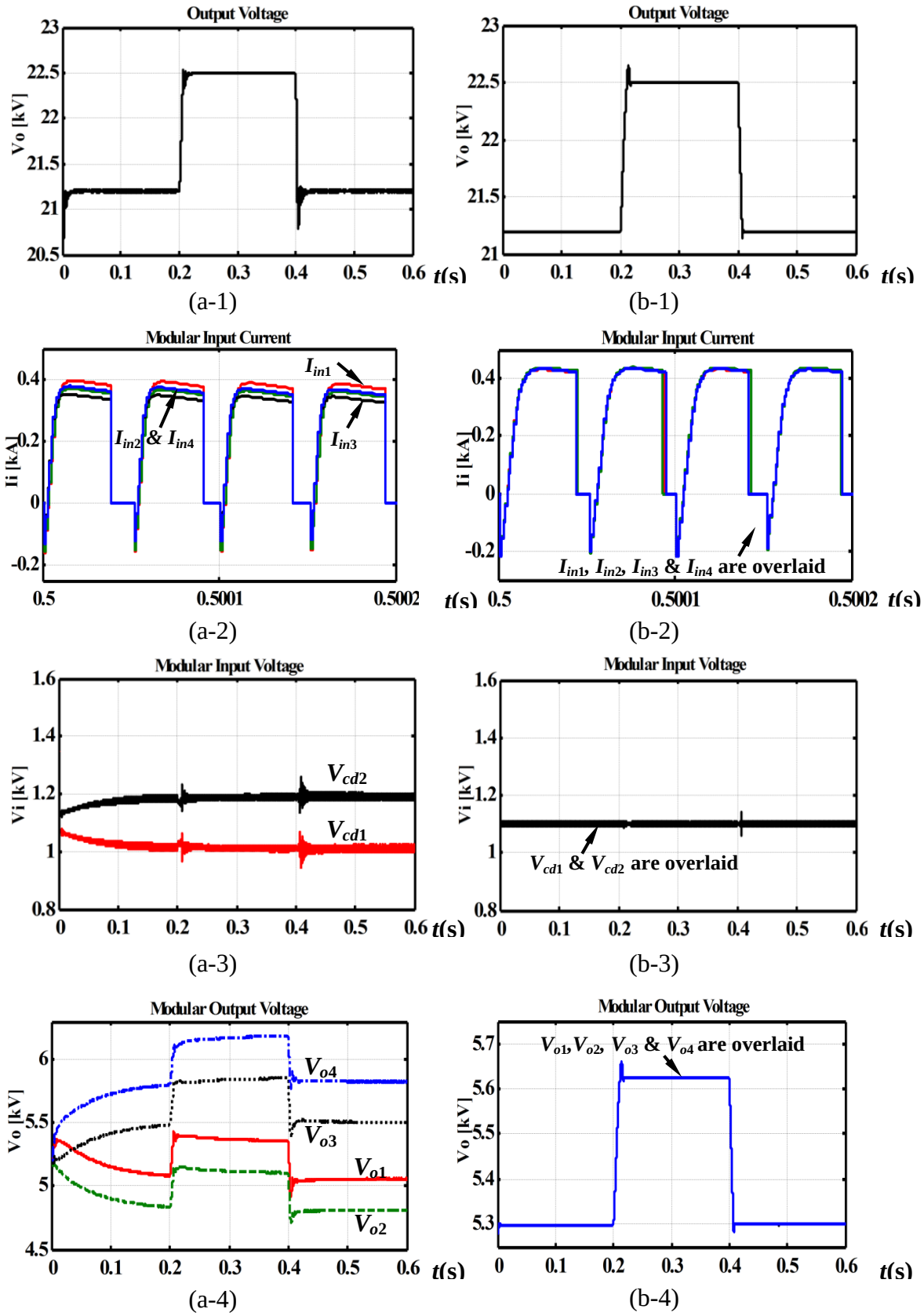


Fig.5.9: Dynamic responses of the ISIPOS converter to a step change in load voltage, with mismatched parameters (a) common duty-cycle control (b) proposed control

Fig.5.9 (a) and (b) respectively show the voltage and current performance of the ISIPOS converter under common duty-cycle control and under the proposed control scheme.

Fig.5.9 (a-1) illustrates output voltage performances and Fig.5.9 (a-2) and (a-3) illustrate the consequences of the control without dedicated input voltage sharing control, indicating that with large input filter capacitor mismatch, as will be the case with large electrolytic capacitors, significant differences in leakage currents may cause serious divergence of voltages across input balancing capacitor [13]. The maximum difference in modular input currents is between module 1 and module 3 and is approximately 12.5 % of the nominal current of module 1. Similarly, mismatch in transformer turns-ratio, and output capacitance and inductance significantly degrade the power sharing performance. Under common duty-cycle control, output voltages of all modules exhibit significant voltage ripple, with a worst-case peak voltage ripple of approximately 15 % of the average load voltage as shown in Fig.5.9 (a-4).

The simulation results from Fig.5.9 (a) show that the performance of common duty-cycle control is significantly affected by the mismatches. In contrast, the proposed power sharing control scheme is able to compensate the mismatch as shown in figure Fig.5.9 (b), where input voltage, current and modular voltage outputs are overlaid. These results show that the proposed power balancing control scheme is able to compensate any negative influences resulting from system parameter mismatch and transience.

In addition, a scaled-down experimental rig of ISIPOS connected modular DC/DC converter with 4-modules given was built to validate the proposed control scheme.

5.3.5 Experimental Validation of Normal Operation

The experimental prototype shown in Fig.5.10 with 4 full-bridge DC/DC modules as illustrated in the Chapter 4, was applied to validate the proposed converter with ISIPOS connection and control scheme. In this experiment, two input capacitances are connected in series to form the two parallel arms and two Hall-effect voltage sensors measure input capacitor voltages.

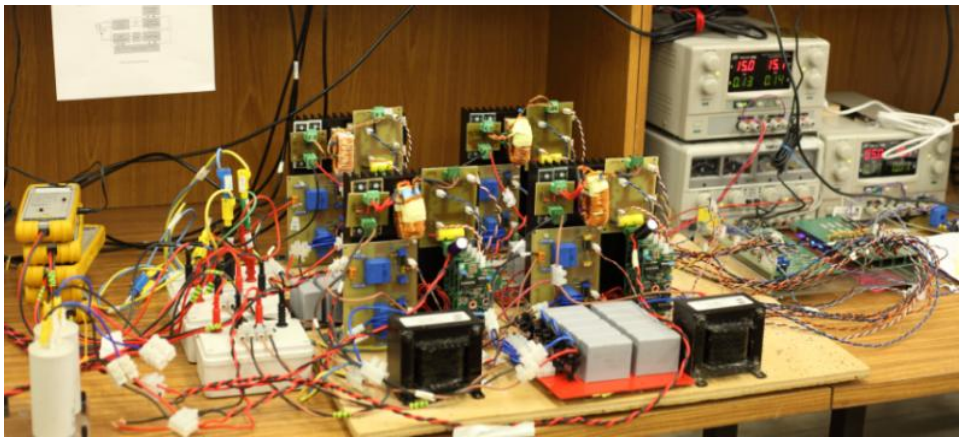


Fig.5.10: ISIPOS connected full-bridge DC/DC converter test rig

The schematic diagram of this 200 W experimental system is shown in Fig.5.11. The control system is implemented using same Infineon Tricore TC1796 DSP used previously, and the modular input voltages, output voltages and inductor currents are measured using Hall-effect sensors and fed into the DSP. The main parameters of this experimental system are listed in Table 5.2.

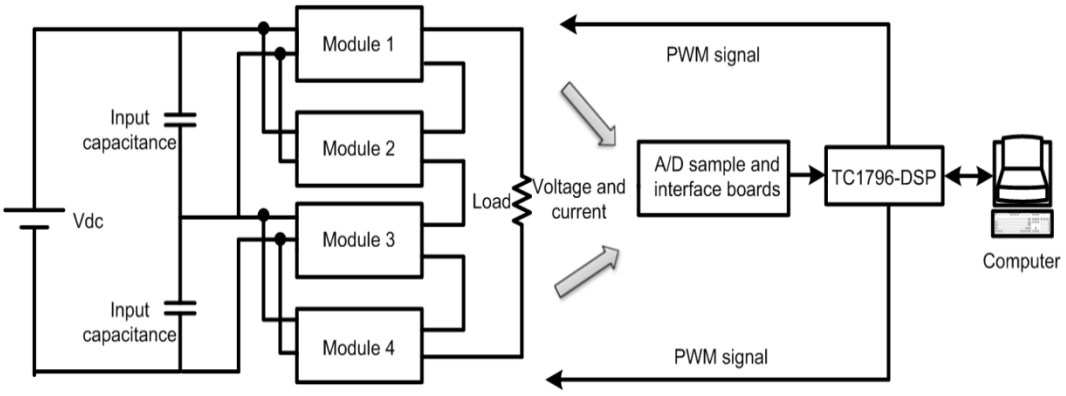
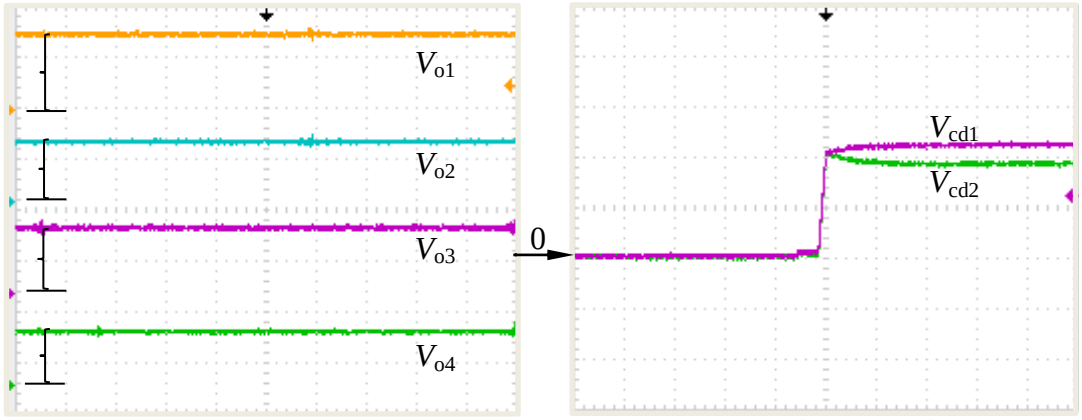


Fig.5.11: Schematic diagram of the proposed ISIPOS converter experimental system

Table 5.2: List of parameters for experimental system

Parameter	***Experimental Values***	***Parameter***	***Experimental Values***
Converter Rated Power	200 W	Transformer Turns-Ratio	T_1 =1:1.4 T_2 =1:1.2 T_3 =1:1.3 T_4 =1:1.2
Number of Modules	4		
Input DC Voltage	40 V	Output Inductance	L_1 =6.8 mH L_2 =5.0 mH L_3 =5.9 mH L_4 =6.3 mH
Output DC Voltage	80 V		
PWM Carrier Frequency	2.5 kHz	Output Capacitance	C_1 =160 μF C_2 =160 μF C_3 =200 μF C_4 =200 μF
Input Capacitance	C_{d1} =45 μF C_{d2} =40 μF		

Fig.5.12 shows the voltage performance of the ISIPOS converter under common duty-cycle control and under the proposed control scheme. Fig.5.12 (a) and (c) show modular output voltages V_{o1}, V_{o2}, V_{o3} and V_{o4} being regulated at the desired closed-loop output voltage reference of 80 V under common duty-cycle control and the proposed control strategy respectively. Fig.5.12 (c) shows that the proposed control scheme ensures that output voltage is equally shared amongst the modules. Without the dedicated power balancing controller, each module operates at a different voltage, as shown in Fig.5.12 (a), thus leading to unbalanced power distribution amongst the modules. As shown, despite the mismatches, OVS is achieved with the proposed control scheme. Fig.5.12 (b) and (d) show input voltage sharing performance between V_{cd1} and V_{cd2}. Fig.5.12 (b) shows start-up of input capacitance voltages V_{cd1} and V_{cd2} when same duty cycle is applied to the modules. It can be seen that there is a difference between the two voltages. Fig.5.12 (d) shows the results of employing the proposed control to balance input capacitance voltages. As shown, despite the mismatches, IVS is achieved with the proposed control scheme.

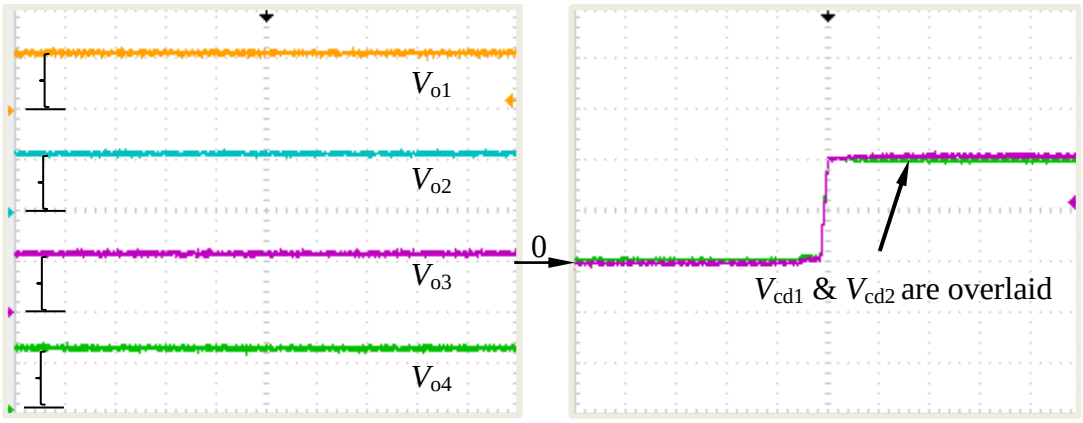


20 ms/div, 20 V/div

(a)

100 ms/div, 10 V/div

(b)



20 ms/div, 20 V/div

(c)

100 ms/div, 10 V/div

(d)

Fig.5.12: Experimental results illustrating normal operation of the converter with common duty-cycle control (a) modular output voltage (b) input capacitance voltages and the performances with proposed control (c) modular output voltage (d) input capacitance voltages

Fig.5.13 shows selected experimental results for dynamic operation of the ISIPOS connected modular converter, with mismatches between the modules components. The control action is not active at first and same duty cycle is applied to the modules shown as in Fig.5.13 (a),. At t=150 ms, control action is activated to achieve IVS. This shows the effectiveness of the proposed control on power sharing between the modules. The steady-state input voltage distribution is given in Fig.5.13 (b), which shown $V_{cd1} = V_{cd2}$ with the input voltage control.

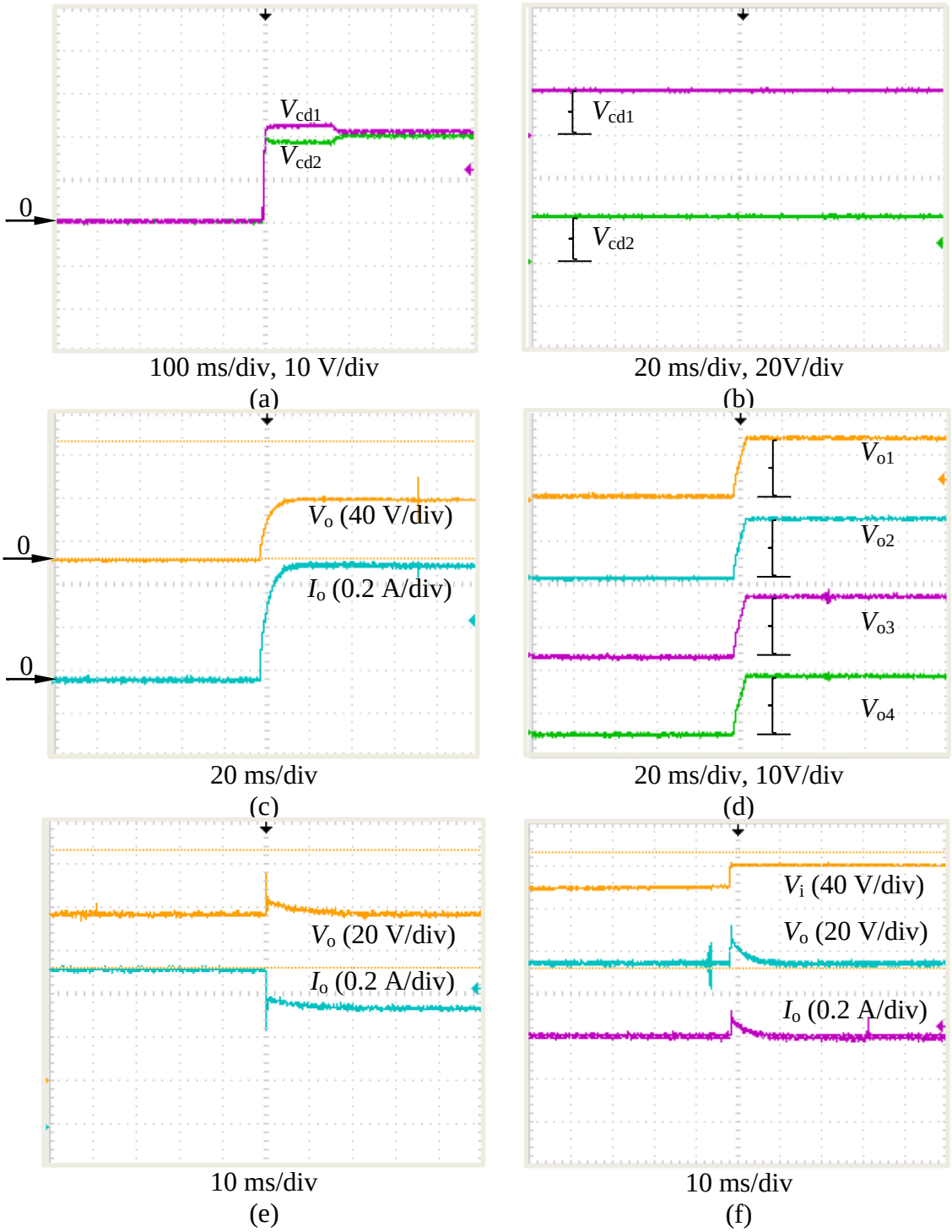


Fig.5.13: Experimental results illustrating dynamic operation of the converter (a) input capacitance voltages with control enabled at 150 ms (b) steady-state input capacitance voltages with control (c) output voltage and current during start-up transient (d) modular output voltages during start-up transient (e) output voltage and current response during load change transient and (f) input voltage, and output voltage and current response to a step input voltage increase

Fig.5.13 (c) shows output voltage and current during start-up, where output voltage is regulated to the designed steady-state value of 60 V after 10 ms. Fig.5.13 (d) shows the modular output voltages during the start-up process, and illustrates that they maintain balanced throughout, thereby proving the ability of the control scheme. The transient response to a step increase in load resistance is shown in Fig.5.13 (e), where output voltage is regulated at the desired reference value after a short duration perturbation, and the current is decreased due to the increase in load resistance. Input voltage, output voltage and output current performance in response to a step increase in input voltage are presented in Fig.5.13 (f). The responses to the load and input voltage transients are robust with minimal oscillation, and the steady-state condition is recovered after 10 ms.

Application of the widely-used common duty-cycle control scheme to the proposed converter is likely to lead to non-uniformly distributed power amongst the modules, and would result in reduced reliability. In contrast, it can be observed that the proposed control scheme successfully addresses the conditions of unbalanced transformer turns-ratios, and mismatched capacitances and inductances amongst the modules by balancing the input capacitor voltage and modular output voltages under normal operation. Also, the experimental results for the proposed control scheme show that it enables the converter being investigated to ride through transient conditions, with well-controlled power balancing, and output voltage and current characteristics that exhibit minimum over-shoots.

Power sharing control has been demonstrated to effectively balance power distribution whilst dealing with dynamic operation using a 4-module simulation system rated at 1 MW and a 4-module scaled-down laboratory test rig. More importantly, reliability is an established metric for converter design, especially for high-power medium-voltage converters.

5.4 Control Scheme under Faulted Operation

5.4.1 Fault Detection and Redundancy Control Scheme

One of the merits of using this modular architecture is the increased reliability it provides due to the designed level of redundancy. Additional modules than are

required to provide the load power and voltage may be introduced to manage events where modules fail. Each module will therefore operate at power level lower than its rating under normal operation. When a fault occurs, the modularity feature allows the converter to isolate the faulty module and be re-configured using the remaining healthy modules to supply the load using a pre-designed control strategy. However, there is often a trade-off between the extra cost caused by the redundant modules and the impact of the failure [14].

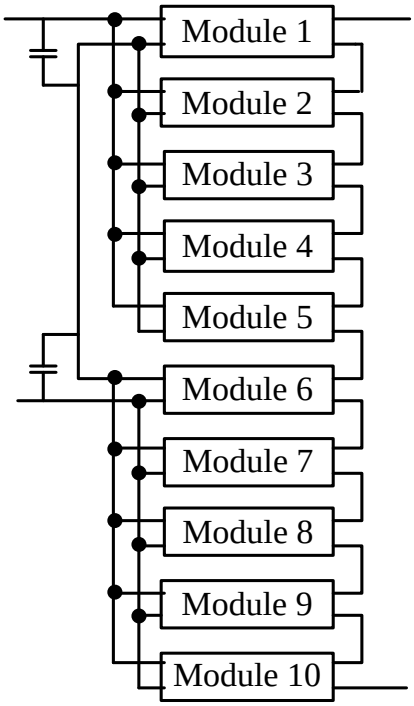


Fig.5.14: ISIPOS connected 10-module system

Provision of redundancy can be illustrated by the converter in Fig.5.1 with 10-modules and the faulty module is module 5. Fault detection can be realised by monitoring the modular output voltage. In this case as shown in Fig.5.14, if the output voltage falls outside a predefined range, e.g. $V_o/10.5<V_o<V_o/9.5$, the protection mechanism is activated. The faulty module is isolated by blocking its front-end pulse width modulated H-bridge converter and bypassing its output diode bridge using a combination of a bypass switch and a bleed resistor to dissipate the energy stored in the filter capacitor. Following that, there are two ways of obtaining fault-tolerant operation for this 10-module system. The first method is to isolate module 5, maintain input capacitor voltage balance, and increase the output voltages of the remaining

healthy modules (modules 1, 2, 3, and 4) in the upper parallel-connected arm to compensate the lost module 5 by changing the modular output voltage references from $V_o^*/10$ to $V_o^*/8$. The references for the 5 modules in the lower parallel-connected arm remain at $V_o^*/10$. By doing this, the input currents to the modules in the upper parallel arm are boosted to increase the input powers. In the second method, module 5 and one module in the lower arm, e.g. module 6, are isolated to keep the symmetrical structure of the system. The outputs from all of the remaining healthy modules are boosted to track the new reference $V_o^*/8$.

From the stability point of view, the second method maintains the symmetrical structure, which may simplify control action. However, it requires to isolate one health module in the lower arm. Therefore, the first option is adopted in this study. Simulation results are given in the next section to verify its performance during fault-tolerant operation.

Table 5.3: List of parameters for ISIPOS connected 10-module DC/DC converter

Parameter	***Simulation Values***	***Parameter***	***Simulation Values***
Converter Rated Power	5 MW	Transformer Turns-Ratio	T_1 =1:1.4 T_2 =1:1.45 T_3 =1:1.4 T_4 =1:1.45 T_5 =1:1.4 T_6 =1:1.45 T_7 =1:1.4 T_8 =1:1.45 T_9 =1:1.4 T_{10}=1:1.45
Number of Modules	10		
Input DC Voltage	5 kV		
Output DC Voltage	28 kV		
PWM Carrier Frequency	2.5 kHz		
Input Capacitance	C_{d1} =5000 μF C_{d2} =5500 μF	Output Capacitance	C_1 =400 μF C_2 =450 μF C_3 =400 μF C_4 =450 μF C_5 =400 μF C_6 =450 μF C_7 =400 μF C_8 =450 μF C_9 =400 μF C_{10}=450 μF
Output Inductance	L_1 =50 mH L_2 =55 mH L_3 =50 mH L_4 =55 mH L_5 =50 mH L_6 =55 mH L_7 =50 mH L_8 =55 mH L_9 =50 mH L_{10}=55 mH		

5.4.2 Simulation Validation of Fault-Tolerant Operation

The system parameters are listed in Table 5.3. Note that some parameters are chosen to introduce mismatch between the modules.

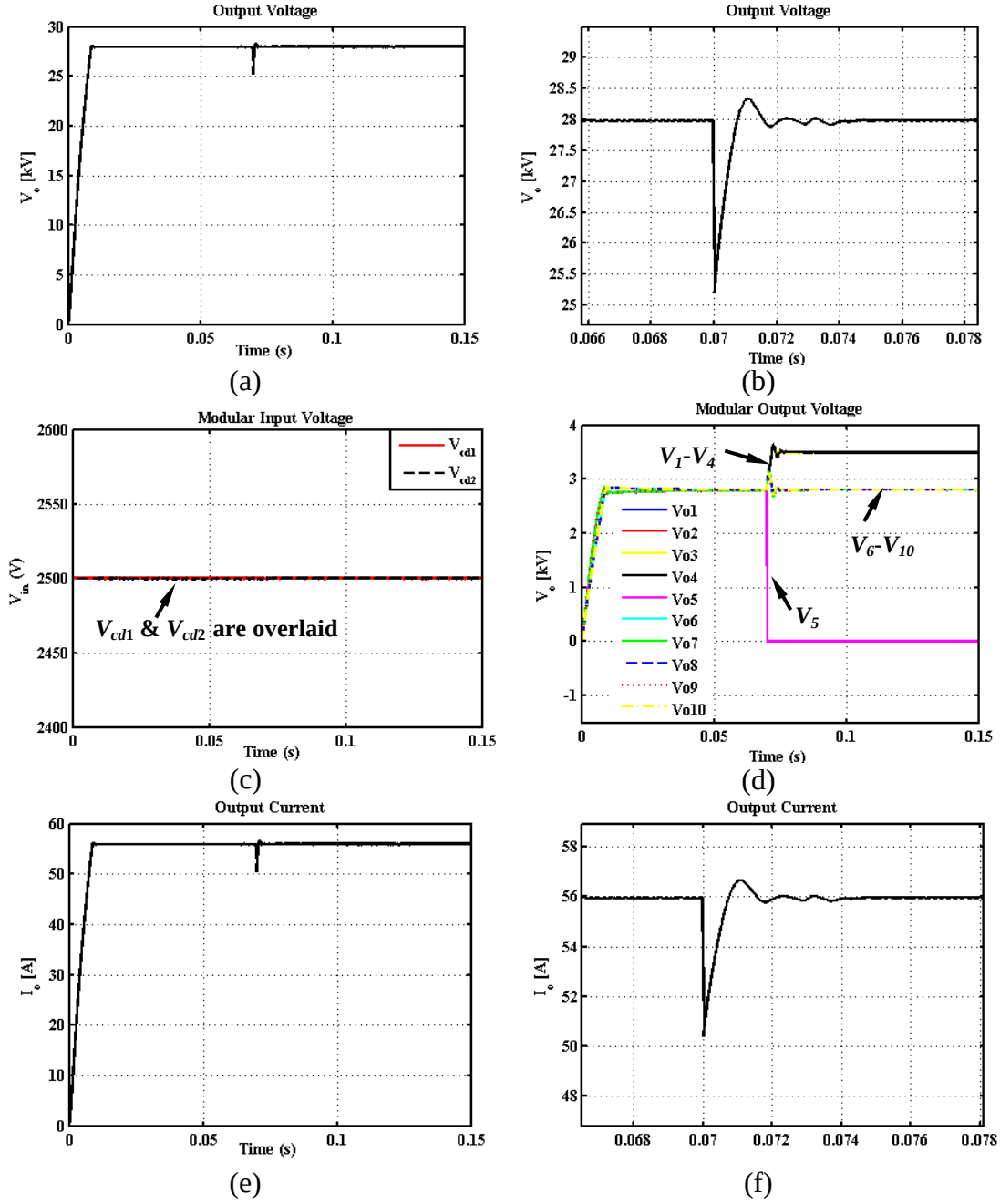


Fig.5.15: Simulation results illustraing fault-tolerant operation when a short circuit fault is applied to the output of module 5 (a) output voltage (b) detail of output voltage transient (c) input capacitance voltages (d) modular output voltages (e) output current and (f) detail of output current transient

Fig.5.15 presents selected simulation results illustrating fault-tolerant operation, with mismatches between module parameters. The fault occurs to module 5 at t=75 ms. It can be seen from Fig.5.15 (a) and (b) that converter output voltage V_o recovers its pre-fault value after a short time period. Following the fault, the faulty module 5 is bypassed and its output becomes 0. Fig.5.15 (c) shows that the control loop can ensure input capacitor voltage balance even under the fault condition. The output voltages of the remaining modules in the upper arm are boosted to compensate and the modules in the lower arm retain their pre-fault outputs, as shown in Fig.5.15 (d). Fig.5.15 (e) and (f) show the output current disturbance caused by the fault, but the recovery time is only a few milliseconds.

These simulation results show that, with parameter mismatches in the system, the proposed control scheme provides fault-tolerant operation by isolating the faulty module and using the selected modules to compensate. This fault-tolerant operation demonstrates that the proposed converter offers high reliability, which is an important factor in medium-voltage applications.

5.4.3 Experimental Validation of Fault-Tolerant Operation

In order to demonstrate the fault-tolerant ability of the ISIPOS connected modular DC/DC converter, a fault is created in the 4-module DC/DC converter by applying a short-circuit fault to the output of module 4. During the pre-fault period, the load voltage is equally shared amongst the modules as shown in Fig.5.13. Following detection of the fault, module 4 is isolated and its output voltage falls to zero. Meanwhile, the output from module 3 is increased to compensate and the other module outputs remain at their pre-fault values, as shown in Fig.5.16 (a). A detailed view of the module output voltages (V_{o1}, V_{o2}, V_{o3}, V_{o4}) is shown in Fig.5.16 (b). However, for this case with a low number of converter modules, module 3 output voltage experiences a large overshoot due to the 50 % step increase in the input voltage to module 3 resulting from control action following the fault. This issue would be less significant in a practical high-power medium-voltage system, which would require a DC/DC converter with a much larger number of modules, leading to a smaller transient change of input voltage under the same fault conditions.

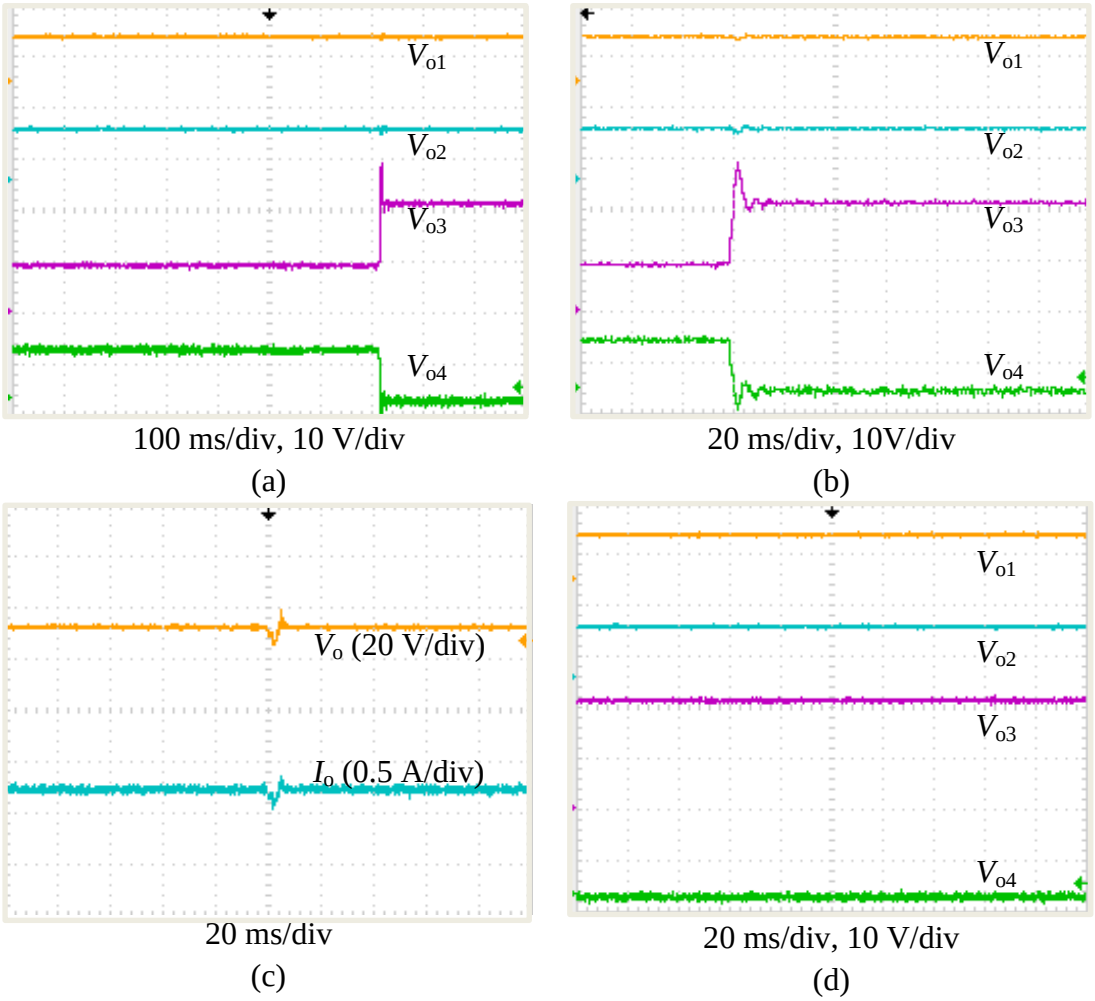


Fig.5.16: Experimental results illustrating fault-tolerant operation of the converter when a short circuit fault is applied to the output of module 4 (a) modular output voltages (b) detail of modular output voltages (c) output voltage and output current during transient and (d) modular output voltages under steady-state conditions

Fig.5.16 (c) shows output voltage V_o and output current I_o transients following the fault. The proposed control scheme provides a fast dynamic response after a short duration (<10 ms) transient, and maintains at its pre-fault value. For the steady-state condition after the fault, output voltage is shared equally between healthy modules 1, 2 and 3 as shown in Fig.5.16 (d). These results show that the proposed control scheme is capable of managing internal module failure, whilst ensuring continuous operation of and equal voltage sharing amongst the remaining healthy modules. Although there are not enough modules to demonstrate the equal power sharing performance following the fault, the concept of balancing input capacitor voltages, isolating the

faulty module and boosting the outputs of the remaining healthy modules from that parallel-arm are illustrated in this experiment.

5.5 Summary

A novel ISIPOS connected modular DC/DC converter topology is proposed in this chapter. With this new topology, the proposed DC/DC converter has the ability to further expand the benefits of parallel-series connection of low-power rating modules. The proposed control scheme incorporates power sharing to adjust the individual control signals produced by the outer Lyapunov output voltage controller. IVS and OVS control loops are employed to achieve power sharing between the modules, with mismatched parameters. Fault detection and redundancy can be easily employed in this converter due to its modularity. System-level simulation and scaled-down experimental results confirms that the proposed control scheme applied to the new ISIPOS DC/DC converter is reliable for uniform power sharing and fault-tolerant operation. The proposed converter and control strategy can be extended to any number of modules and any allowable level of redundancy, making it a promising topology for high-power medium-voltage DC/DC conversion applications.

5.6 Chapter Reference

[1] S. Chunwei, R. Zhao, L. Wangqing and Z. Zheng, "A novel control strategy for input-parallel-output-series inverter system," in Electrical Machines and Systems (ICEMS), 2011 International Conference on, Beijing, pp. 1-5, 2011.

[2] R. Xinbo, C. Wu, C. Lulu, C. K. Tse, Y. Hong and Z. Tao, "Control Strategy for Input-Series & Output-Parallel Converters," Industrial Electronics, IEEE Transactions on, vol. 56, no. 4, pp. 1174-1185, 2009.

[3] C. Wu, R. Xinbo, Y. Hong and C. K. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," Power Electronics, IEEE Transactions on, vol. 24, no. 6, pp. 1463-1474, 2009.

[4] Y. Hong, R. Xinbo and C. Wu, "The input voltage sharing control strategy for input-series and output-parallel converter under extreme conditions," in Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE, pp. 662-667, 2009.

[5] R. Xinbo, C. Lulu and Z. Tao, "Control Strategy for Input-Series Output-Paralleled Converter," in Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE, pp. 1-8, 2006.

[6] S. Deshang, D. Kai and L. Xiaozhong, “Duty Cycle Exchanging Control for Input-Series-Output-Series Connected Two PS-FB DC-DC Converters,” Power Electronics, IEEE Transactions on, vol. 27, no. 3, pp. 1490-1501, 2012.

[7] J. W. Kimball, J. T. Mossoba and P. T. Krein, “A Stabilizing, High-Performance Controller for Input Series-Output Parallel Converters,” Power Electronics, IEEE Transactions on, vol. 23, no. 3, pp. 1416-1427, 2008.

[8] D. Qing, Q. Bojin, W. Tao, Z. Tao and L. Xiao, “A High-Power Input-Parallel Output-Series Buck and Half-Bridge Converter and Control Methods,” Power Electronics, IEEE Transactions on, vol. 27, no. 6, pp. 2703-2715, 2012.

[9] A. A. Aboushady, “Design, Analysis and Modelling of Modular Medium-Voltage DC/DC Converter Based Systems,” PhD thesis, Departement of Electronics and Electrical Engineering, University of Strathclyde, Glasgow, 2012.

[10] S. N. Manias and G. Kostakis, “Modular DC-DC convertor for high-output voltage applications,” Electric Power Applications, IEE Proceedings B, vol. 140, no. 2, pp. 97-102, 1993.

[11] S. Jianjiang, L. Jie and H. Xiangning, “Common-Duty-Ratio Control of Input-Series Output-Parallel Connected Phase-shift Full-Bridge DC/DC Converter Modules,” Power Electronics, IEEE Transactions on, vol. 26, no. 11, pp. 3318-3329, 2011.

[12] R. Giri, V. Choudhary, R. Ayyanar and N. Mohan, “Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing,” Industry Applications, IEEE Transactions on, vol. 42, no. 4, pp. 1101-1111, 2006.

[13] K. Jeong-il, R. Chung-Wook, M. Gun-Woo and Y. Myung-Joong, “Design of phase-shifted parallel-input/series-output dual inductor-fed push-pull converter for high-power step-up applications,” in Industrial Electronics Society, IECON '01. The 27th Annual Conference of the IEEE, pp. 1249-1254, 2001.

[14] V. Choudhary, E. Ledezma, R. Ayyanar and R. M. Button, “Fault Tolerant Circuit Topology and Control Method for Input-Series and Output-Parallel Modular DC-DC Converters,” Power Electronics, IEEE Transactions on, vol. 23, no. 1, pp. 402-411, 2008.

Chapter 6: DAB Modules with ISIPOS Connection

This chapter proposes a new high-power ISIPOS connected modular DC/DC converter, where the DAB DC/DC converter is employed as the basic module in the primary and secondary sides. This converter arrangement enables bidirectional power transfer, which is essential for DC energy transfer and storage systems. Each DAB module is operated in a single-phase-shift (SPS) mode, thus achieving easy implementation. The control strategy presented in Chapter 5 is extended to the DAB based ISIPOS connected modular DC/DC converter to enable power sharing between the modules and facilitate fault-tolerant operation. The viability and effectiveness of the proposed control method are demonstrated through simulation of power sharing performance and fault-tolerant operation in a 1 MW DC/DC converter. This simulation is supported by experimental results obtained from a 15 kW DAB test rig with 1.7 kV silicon-carbide MOSFET devices. Experimental data from these tests were used to propose a concept design for a scaled-up 5 MW version of this topology.

6.1 DAB Converter Background

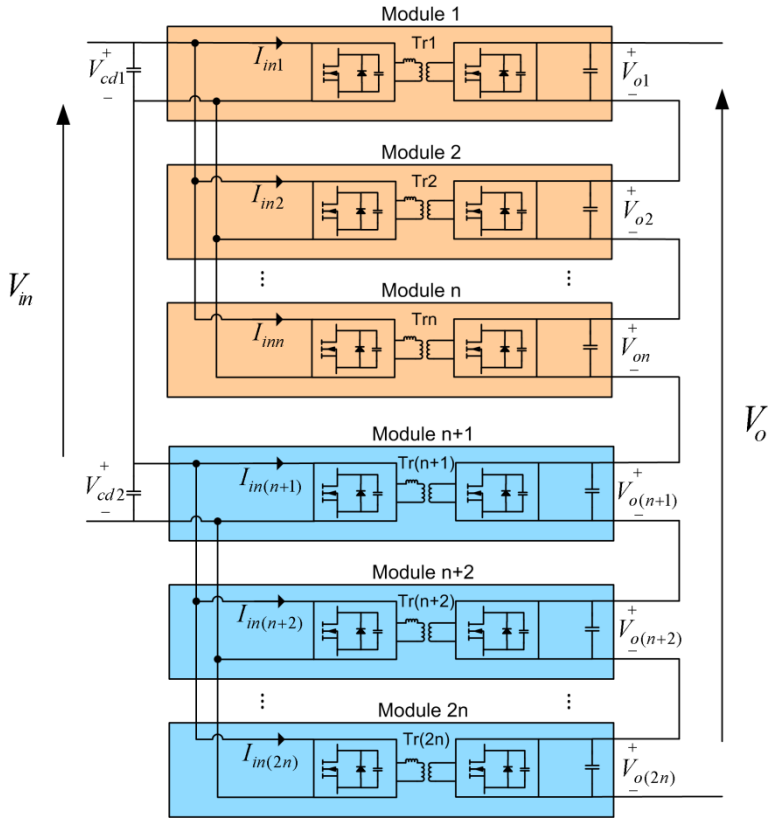


Fig.6.1: ISIPOS converter topology with DAB modules

Chapters 4 and 5 demonstrated the successful operation of IPOS and ISIPOS connected modular DC/DC converters with phase shifted full-bridge modules to applications with uni-directional power flow. This chapter extends the IPOS and ISIPOS connection concept to bi-directional power flow, which is required for a range of applications such as bi-directional energy transfer between two DC buses and energy storage in renewable energy system, batteries, and hybrid electric vehicles (HEV) [1, 2]. For the proposed offshore wind farm DC collection network, the bidirectional DC/DC converter is a promising solution for wind turbine black-start operation.

Fig.6.1 shows the proposed structure of a 2*n*-module ISIPOS connected modular DC/DC converter. The low-voltage input stage is made up from two series-connected blocks, each of which comprises *n* parallel-connected DAB modules, whilst the high-voltage output is derived from the series connection of DAB modules. The number of

parallel and series connected modules can be extended to any number according to the application requirements.

The high-power bidirectional DC/DC converter is perceived as one of the key enabling components of DC energy transfer and storage systems, and needs to be designed for high reliability and efficiency. The ISIPOS connected modular structure presents a number of attractive features in high-power applications, which have been outlined in Chapter 5. Considering the modular topology a DAB converter with a transformer to provide galvanic isolation, presented in Chapter 3, has been shown to be an attractive solution for high-power applications since its introduction in 1988 [3]. It is therefore employed as the basic module on the primary and secondary sides due to it having most favorable features in terms of small filter components, mature technology, and low switching loss and device stress amongst bidirectional DC/DC converters. The DAB converter offers bidirectional power flow by manipulating the phase shift between the high-frequency square wave output voltages of the two bridges. In addition, ZVS operation over a reasonable operating range can be achieved without additional resonant circuits by incorporating the transformer leakage inductance, thus achieving high efficiency. Note that the converter may lose soft switching ability under light load conditions and in practice the soft switching limits the phase shift variation. Voltage step-up can be achieved both through the choice of the parallel/series connection and the transformer turns ratios, however module turns ratios close to unity are preferred in order to match device voltage ratings.

6.2 Control Strategy for New ISIPOS DC/DC Converter

The details of the control scheme for a 4-module ISIPOS connected modular DC/DC converter shown in Fig.6.2 are presented in the following section, where V_{in} and V_o are the input and output voltage of the converter respectively, V_{cd1} is the DC input voltage for modules 1 and 2 due to the parallel connection, V_{cd2} is similarly the DC input voltage for modules 3 and 4, I_{in} is the input current of the converter, I_{in1}, I_{in2},…,I_{in4} are input currents to modules 1 to 4, V_{o1},V_{o2},…,V_{o4} are output voltages for modules 1 to 4, I_{lf1}, I_{lf2},…, I_{lf4} are output inductor currents for modules 1 to 4, and I_o is load current.

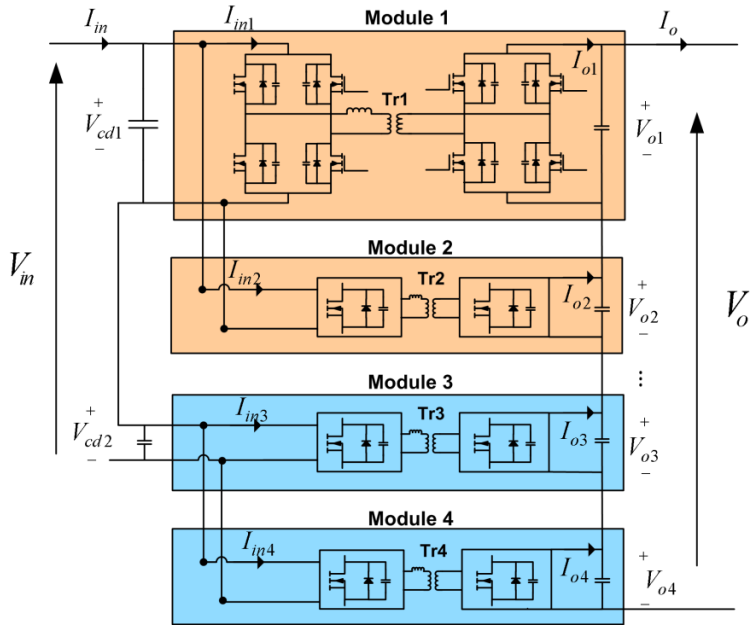


Fig.6.2: ISIPOS converter topology with four DAB modules

6.2.1 Power Sharing Control

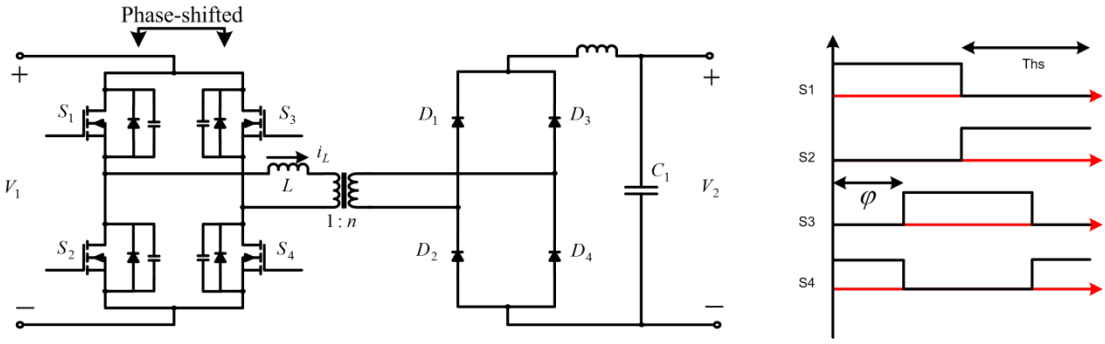


Fig.6.3: Phase-shift operating waveform for full-bridge DC/DC converter

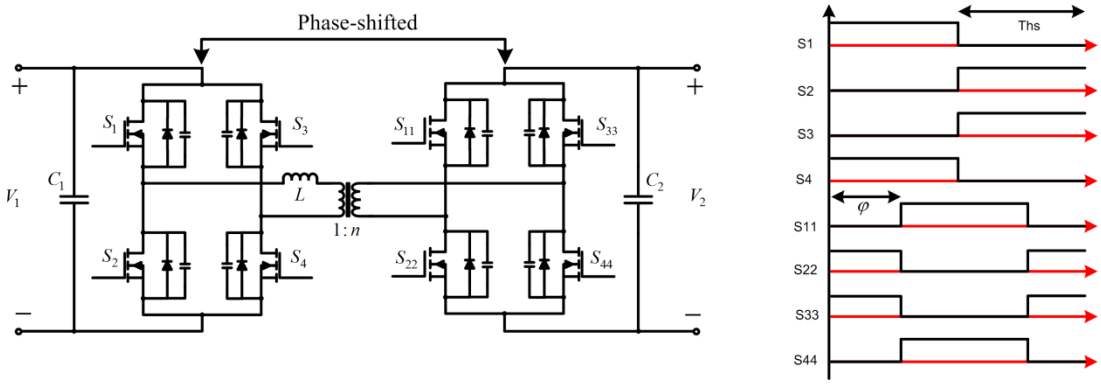


Fig.6.4: Phase-shift operating waveform for DAB DC/DC converter

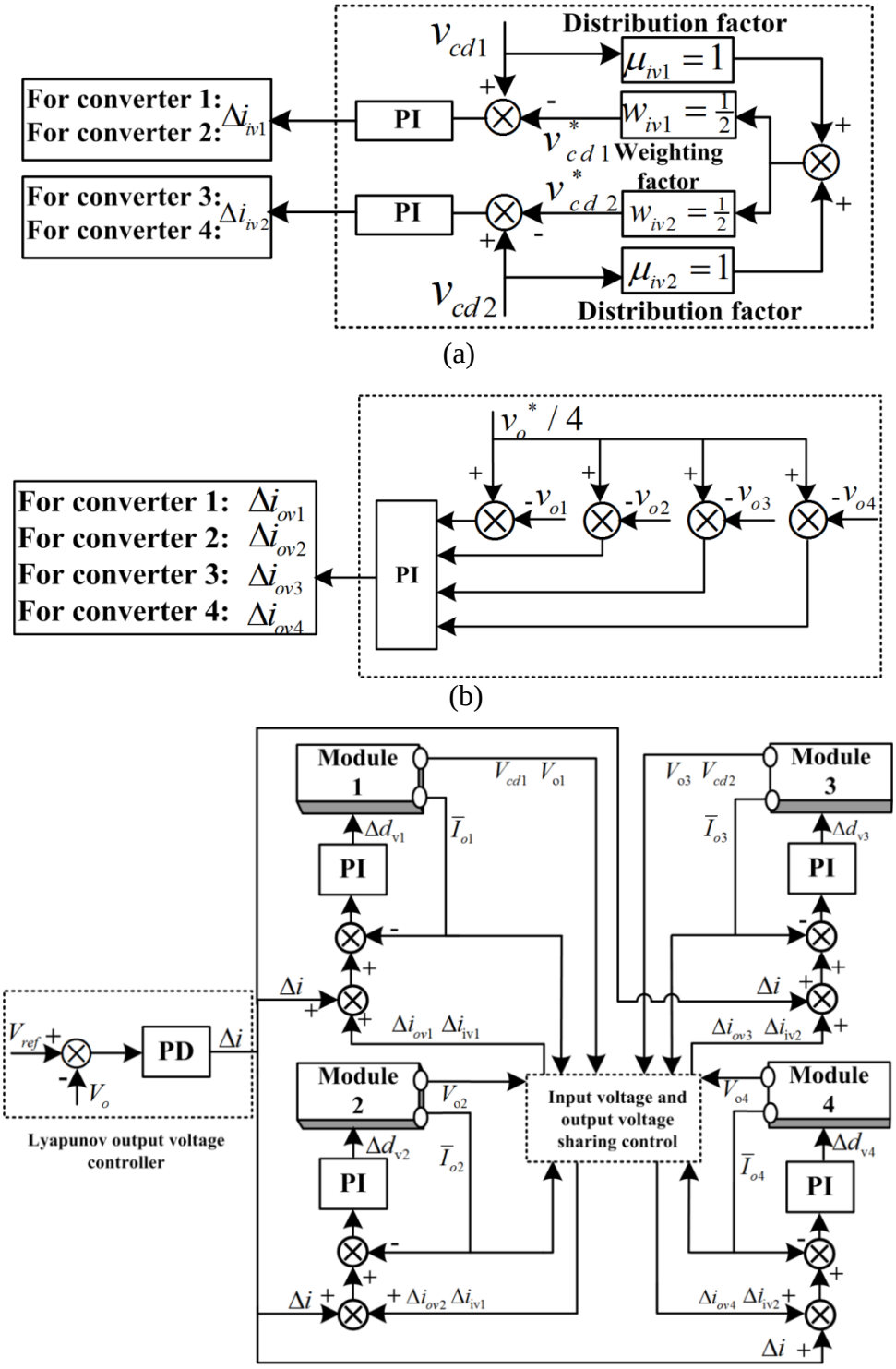


Fig.6.5: ISIPOS DC/DC converter (a) input voltage sharing controller (b) output voltage sharing controller (c) overall control

Due to using the same ISIPOS structure, power sharing in this new converter is similar to that in the ISIPOS connected converter with phase shifted full-bridge

modules, which has been fully addressed in Chapter 5. Apart from the differences in the assignment of the phase shift signals shown in Fig.6.3 and Fig.6.4 between phase shifted full-bridge converter and dual-active bridge converter, all the control aspects, including the Lyapunov output voltage control and power balancing methods are implemented in the same manner as introduced in Chapter 5.

For the converter proposed in this chapter, a dedicated input voltage control loop is employed for stable operation of the input-series stage as shown in Fig.6.5 (a) whilst output voltage balancing control is used for the input-parallel connection as shown in Fig.6.5 (b). The inner current loops shown in Fig.6.5 (c) use the mean value of the currents (I_{o1}, I_{o2}, I_{o3} and I_{o4}) before the output filter capacitance due to the lack of output filter inductance.

6.2.2 Fault-Tolerant Operation Control

It has been stated that the proposed parallel-series connected modular converter has internal fault management capability with a designed level of redundancy. This is achieved through re-configuration of the power circuit such that faulty modules can be blocked and power-redistributed in order to allow continued system operation without any performance degradation. The provision of redundancy with the ISIPOS structure has been fully illustrated in Chapter 5, as well as the detection of the faulty module. However, unlike the converter with full-bridge modules which requires additional bypass switches and bleed resistors to bypass the output bridge as stated in Chapter 4 and Chapter 5, the converter with DAB modules can block both bridges without additional devices, indicating less cost and a simpler control scheme.

The effectiveness of the proposed control strategy is assessed in the following section, which considers the impact of mismatches amongst modules, and internal module failure operation in the 4-module ISIPOS connected modular converter shown in Fig.6.2.

6.2.3 Simulation Validations of Power Sharing Performance

Comparison between the widely used common duty-cycle control scheme shown in Chapter 5 and the proposed control scheme is presented to assess the performance improvement offered when the ISIPOS connected modular DC/DC converter is regulated using the proposed power sharing controller in the context of parameter mismatches, including input capacitance, transformer turns-ratio, and output capacitance mismatches, as specified in Table 6.1.

Table 6.1: List of parameters for ISIPOS connected 4-module DC/DC converter

Parameter	***Simulation Values***	***Parameter***	***Simulation Values***
Converter Rated Power	1 MW	Input DC Voltage	2 kV
Number of Modules	4	Output DC Voltage	18 kV
PWM Carrier Frequency	2.5 kHz	Input Capacitance	C_{d1} =500 μF C_{d2} =800 μF
Transformer Turns-Ratio	T_1 =1:6.3 T_2 =1:6.4 T_3 =1:6.3 T_4 =1:6.4	Output Capacitance	C_1 =300 μF C_2 =350 μF C_3 =300 μF C_4 =330 μF

The ISIPOS converter, shown in Fig.6.2, consisting of 4 DAB modules, with a nominal rating of 1 MW is presented to test the power balancing ability. The control scheme presented is tested by applying a step change in load voltage from 18 kV to 18.5 kV at t=0.1 s and back to 18 kV at t=0.2 s. Note that the interleaved control is not implemented in this case in order to have a better comparisons of the power sharing performances.

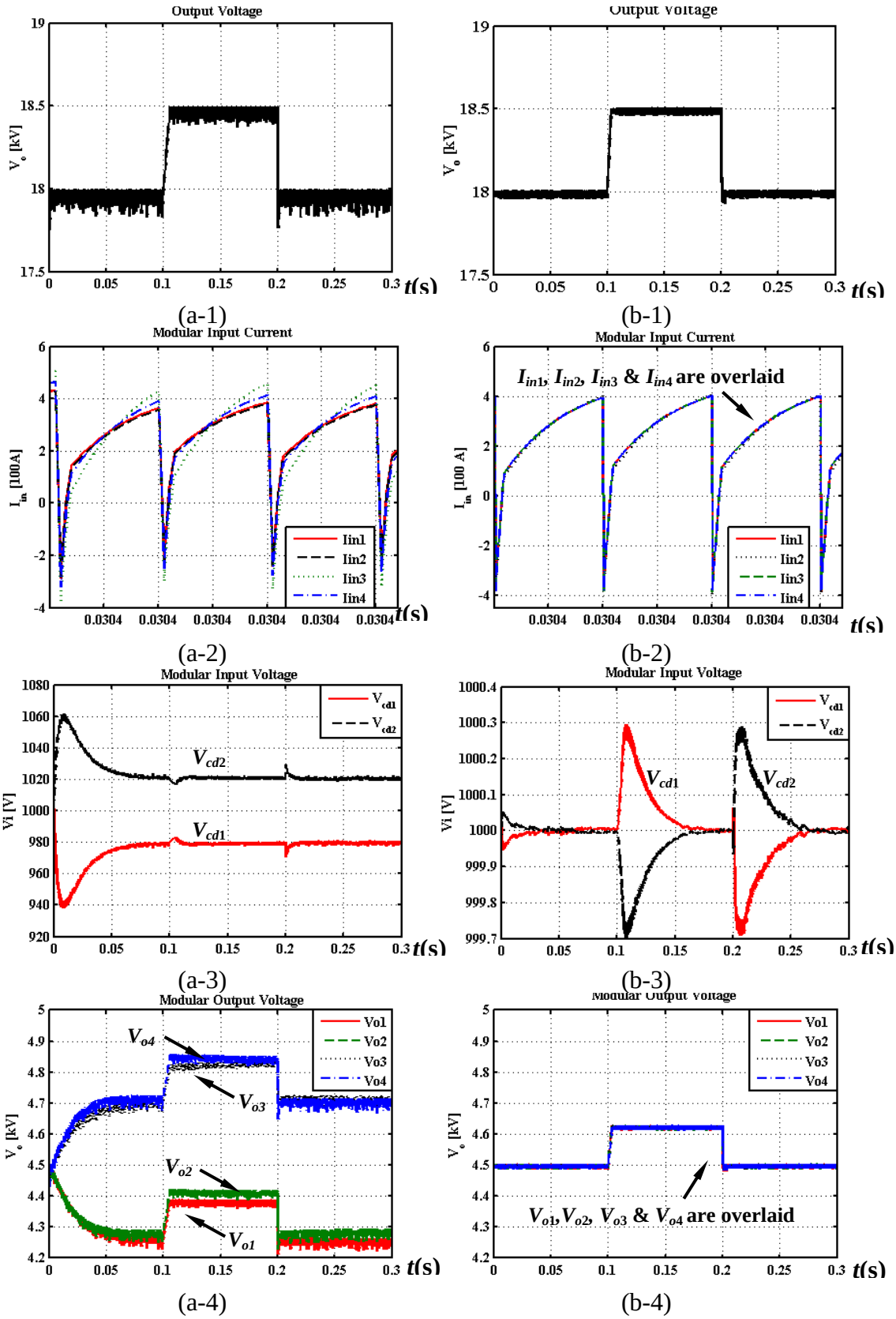


Fig.6.6: Simulation results to a step change in load voltage, with mismatched parameters (a) with common duty-cycle control (b) with proposed control

Fig.6.6 (a) shows the simulation results with common duty-cycle control, whilst Fig.6.6 (b) shows the results with the dedicated power sharing control, where in both cases the values of the input capacitors, output capacitors and transformer turns-ratios are made to be different as shown in Table 6.1. From Fig.6.6 (a-2) and Fig.6.6 (b-2), it can be seen that the dedicated output voltage sharing controller shown in Fig.6.5 (b) helps to equalise the input currents, therefore ensuring that each module contributes equally to the output voltage. Meanwhile, it is demonstrated in Fig.6.6 (a-3) and Fig.6.6 (b-3) that the proposed input voltage sharing controller maintains input capacitor voltage balance. Hence, the proposed control scheme is capable of ensuring power balance between the modules in the presence of module component mismatches.

6.2.4 Simulation Validations of Fault-Tolerant Operation

This section presents an investigation into fault-tolerant operation with the proposed control scheme under internal module fault conditions. An ISIPOS connected modular converter, as shown in Fig.6.1 but with 10 modules, provides the basis for the study.

Table 6.2: List of parameters for ISIPOS connected 10-module DC/DC converter

Parameter	***Simulation Values***	***Parameter***	***Simulation Values***
Converter Rated Power	5 MW	Input DC Voltage	5 kV
Number of Modules	10	Output DC Voltage	28 kV
PWM Carrier Frequency	5 kHz	Input Capacitance	C_{d1} =4000 μF C_{d2} =4200 μF
Transformer Turns-Ratio	T_1 =1:1.4 T_2 =1:1.45 T_3 =1:1.4 T_4 =1:1.45 T_5 =1:1.4 T_6 =1:1.45 T_7 =1:1.4 T_8 =1:1.45 T_9 =1:1.4 T_{10}=1:1.45	Output Capacitance	C_1 =150 μF C_2 =180 μF C_3 =150 μF C_4 =180 μF C_5 =150 μF C_6 =180 μF C_7 =150 μF C_8 =180 μF C_9 =150 μF C_{10}=180 μF

In order to show the effectiveness of the control scheme, a short-circuit fault is applied to module 5 at t=75 ms. Once the faulty module is detected by the detection scheme presented in Chapter 5 and blocked, the remaining healthy module outputs must be boosted to compensate for the loss, as presented in Chapter 5. Note that apart from the fault condition, the simulation model also includes various mismatches between module parameters, which are listed in Table 6.2.

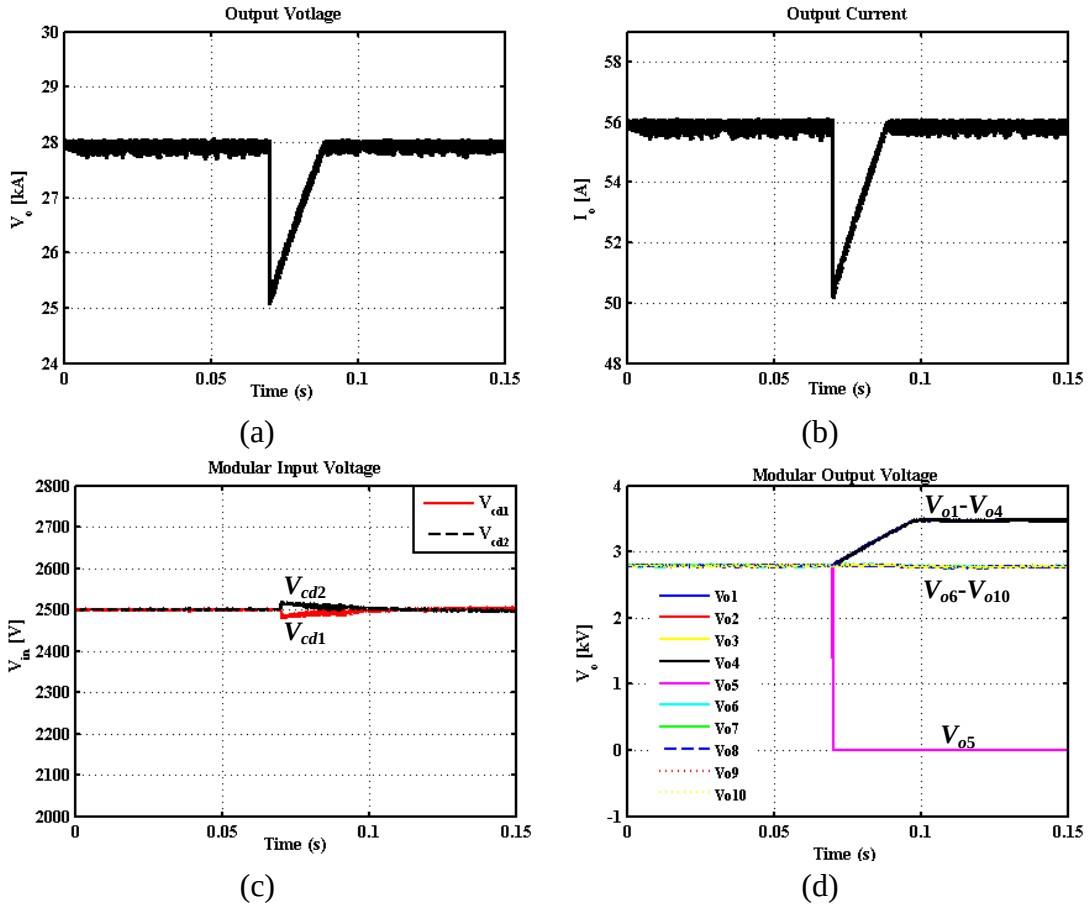


Fig.6.7: Simulation results illustrating dynamic performances of the converter when a short circuit fault is applied to the output of module, with mismatched parameters (a) output voltage (b) output current (c) modular input voltage and (d) modular output voltage

Simulation results highlighting converter performance under the proposed fault-tolerant control scheme when a short-circuit fault is applied to module 5 are presented in Fig.6.7. Fig.6.7 (a) shows that output voltage V_o recovers to the desired value within a few milliseconds following the fault. Fig.6.7 (b) shows the output

current I_o disturbance caused by the fault. The input voltage, shown in Fig.6.7 (c), is evenly distributed amongst the upper and lower parallel connected arms following the disturbance. In addition, V_{o1}, V_{o2}, V_{o3} and V_{o4} in the upper arm are equally boosted to compensate the loss of V_{o5}, whilst V_{o6}, V_{o7}, V_{o8}, V_{o9} and V_{o10} in the lower arm are unaffected as shown in Fig.6.7 (d). Note that all the sharing performances are realised under conditions of mismatched converter modules, indicating that the proposed control scheme is able to not only ensure system reliability in the event of internal module faults but also to sustain high performance.

6.3 Experimental Set-up and Results

The system design is for a 5 MW DC/DC converter based on an ISIPOS configuration and consisting of 2*n* DAB modules. To investigate potential hardware implementation, a scaled-down single module is built, with the aim of investigating the required footprint for a realistic module, analysing the loss mechanisms, and better understanding how a single realistic module building block can be replicated and connected to form a whole system. The set-up and experimental results for the 15 kW laboratory prototype are presented in this section.

6.3.1 Experimental Set-up

Although the proposed multi-module converter allows implementation using low-power rating switches, the optimisation of module number depends on the choice of switches which need to be specified to address the high-power DC/DC converter. Mainly, there are three commonly used switches: Si-MOSFET, IGBT and SiC-MOSFET devices, which will be evaluated in the following sections.

The Si-MOSFET has been widely used in many applications since its introduction in the 1970s. It provides a number of appealing advantages including high switching speed, simple drive requirements, low Rds_{on}, and suitability for extended duration operation. However, the application of MOSFETs is limited by the reduced performance of high-voltage devices. Whist switching speeds can remain high, high-voltage MOSFETs show increased conduction losses and poor reverse recovery characteristics in the integral anti-parallel diode. Si power MOSFETs are available to the 1 kV range and are most applicable below the 300 V range. For this application,

it is likely that Si-MOSFET DC/DC modules would result in an excessive module count.

The IGBT was first introduced in 1981, combining a MOS gate with bipolar transistor characteristics to achieve efficient high voltage ratings and simple gate drive [4]. IGBTs are considered to be the best candidate amongst the switching devices which enable operation at high voltage where MOSFETs are not applicable due to the limitation of voltage rating and on-state resistance. However, the capability of switching frequency decreases as the device voltage level increases. Present IGBTs are limited to 4.5-6.5 kV, with most common commercial IGBTs suited to operation at 1-2.5 kV with reasonable efficiency at frequency less than 4 kHz [4, 5].

Emerging silicon-carbide MOSFET devices presents an attractive solution being considered for high-power converters which may extend MOSFET switching into MW power range and frequency in the MHz range [6]. In addition to improved high voltage performance, SiC exhibits higher temperature rating and performance than conventional Si, leading to increased power density owing to the higher operating temperature provided by these wide band gap semiconductors. Currently 1.7 kV SiC MOSFET devices are readily available in the market, and third generation products are aiming at voltage levels of 2.5-4.5 kV.

The choice of switches is very application-specific. In principle, the choice of the constituent devices of the module aims to optimise efficiency and power density. However this must be balanced against the choice of module number which must avoid excess complexity whilst being capable of delivering redundant operation. Amongst the devices discussed, evaluations are based on the trade-offs between the module voltage level and switching frequency ability.

Si-MOSFETs are suited to modules specified to operate at voltages below 300V. Although the technology enables the highest switching frequency, the lowest voltage capability results in the highest number of modules. IGBTs could provide greater module voltage, however, the switching frequency is limited to the range of 2-10 kHz depending upon the choice of module voltage and power capacity. Whilst module number for IGBT based modules will be less than that of MOSFET based

module, the reduced switching frequency will introduce the penalty of increased transformer size and weight. SiC-MOSFETs could provide a compromise of achieving higher frequency compared with that of IGBTs and raised voltage level compared with that of Si-MOSFETs. In addition, loss analysis [7] has clarified that the efficiency of a DAB with mature SiC devices may reach 99 %. Note that the cost, size, switching frequency and thermal requirements of the application should all be considered when choosing the switching devices.

Based on a review of properties, the SiC-MOSFET was chosen as the device type for the evaluation module, to achieve a low-loss, high power density bi-directional DAB building block for ISIPOS DC-DC converters.

Table 6.3: List of parameters for experimental system

Parameters	***Values***
Converter Rated Power	15 kW
Input DC Voltage	1 kV
Input Capacitor	≥ 20 μF
Output Voltage	1 kV
Output Current	10 A
Output Capacitor	≥ 14 μF
Resonant Capacitor	4.4 ηF
Transformer Turn Ratio	1:2
Transformer Frequency	50 kHz
Primary Leakage Inductance	10 μH
Transformer Efficiency	99.4 %
External Leakage Inductor	85 μH
Estimated Converter Efficiency	>93% with power density of 800 W/kg

The CREE CAS300M17BM2 SiC-MOSFET was selected to enable normal operation at V_{in}=1 kV, V_{out}=1 kV, and a maximum output voltage V_{out}=1.5 kV during redundancy-mode operation. The detailed specifications of the 15 kW laboratory prototype module are given in Table 6.3. Note that prototype module validation is

limited to V_{in}≤500 V, I_{out}≤10 A by power supplies available in the laboratory, and that manufacture of the transformer and the leakage inductors was outsourced to PaytonGroup.

The estimated converter efficiency considers the switching losses, conduction losses, gate losses incurred inside the inverter, diode losses associated with non-synchronous rectification and power losses introduced by the transformer and inductor.

6.3.2 Experimental Results

Based on the specificaions given in Table 6.3, a 15 kW prototype single unit DAB converter was built, as shown in Fig.6.8. The proposed control system was implemented using an Infinoeon Technology TC1796 Tricore microcontroller. To demonstrate the efficiency that can be achieved with the prototype, a set of synchronous rectification tests were carried out with V_{in}=V_{out}=300 V and V_{in}=V_{out}=500 V at 50 kHz operating frequency. Note that the discontinuous current conduction approach is applied and the output is a passive load.

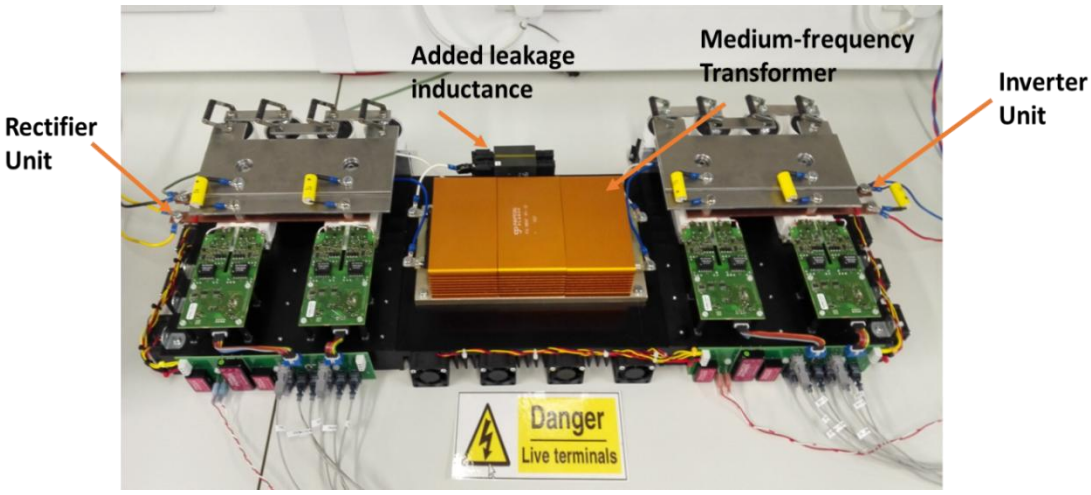


Fig.6.8: Single unit DAB DC/DC converter test rig

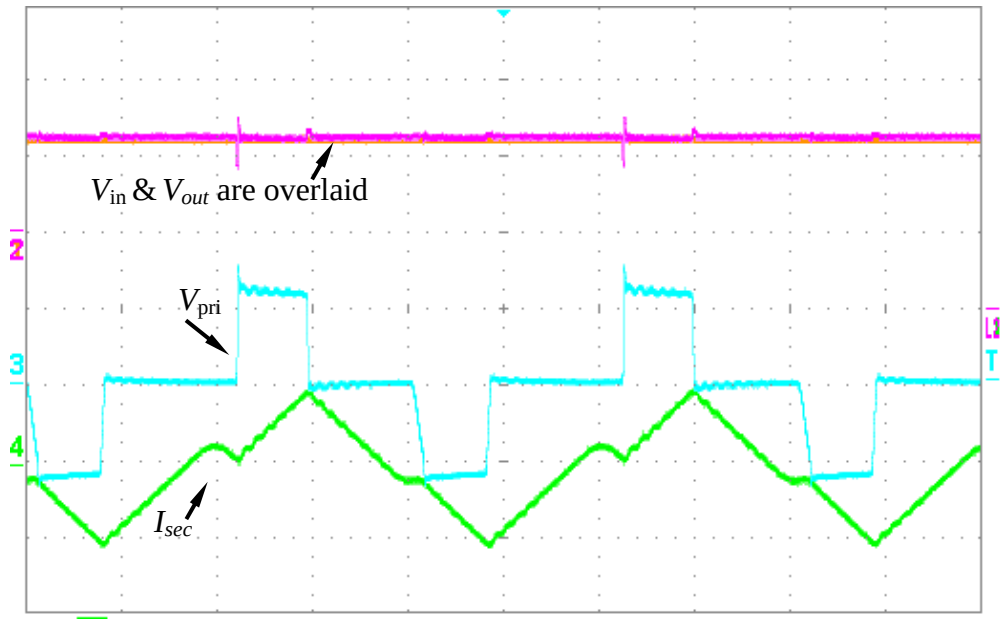


Fig.6.9: Synchronous rectification experimental results with 300 V input voltage: V_{in}, V_{out} and V_{pri} with 250 V/div, and I_{sec} with 1 A/div. Timebase =5 µs/div.

Given V_{in}=V_{out}=300 V, Fig.6.9 presents input voltage V_{in}, output voltage V_{out}, transformer primary voltage V_{pri} and secondary current I_{sec} waveforms, at load current of 1.75 A. Fig.6.10 shows the associated results when V_{in} and V_{out} equal 500 V at load current of 3.03 A.

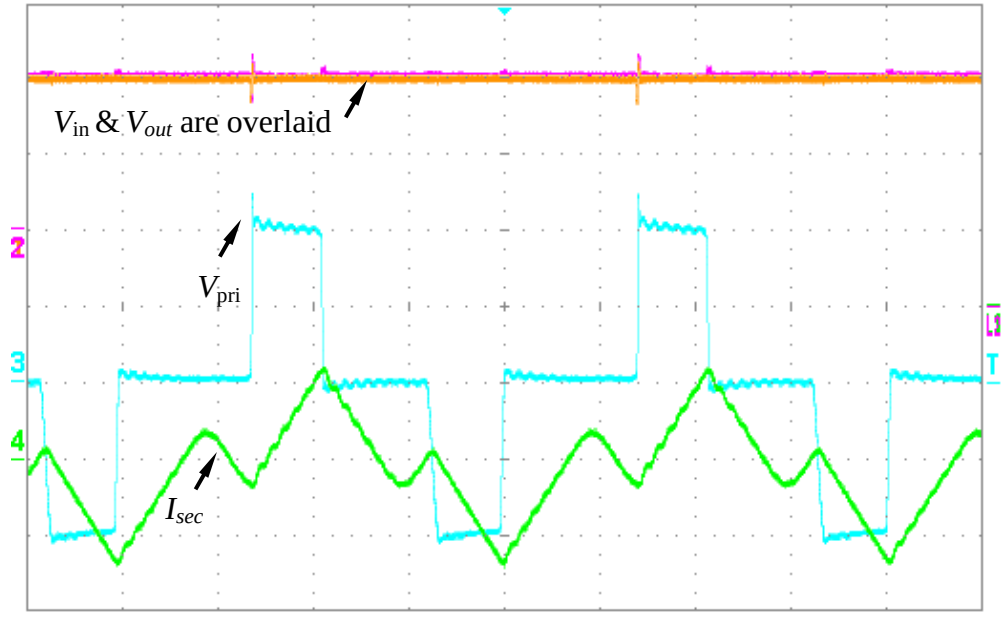


Fig.6.10: Synchronous rectification experimental results with 500 V input voltage: V_{in}, V_{out} and V_{pri} with 250 V/div, and I_{sec} with 2 A/div. Timebase =5 µs/div.

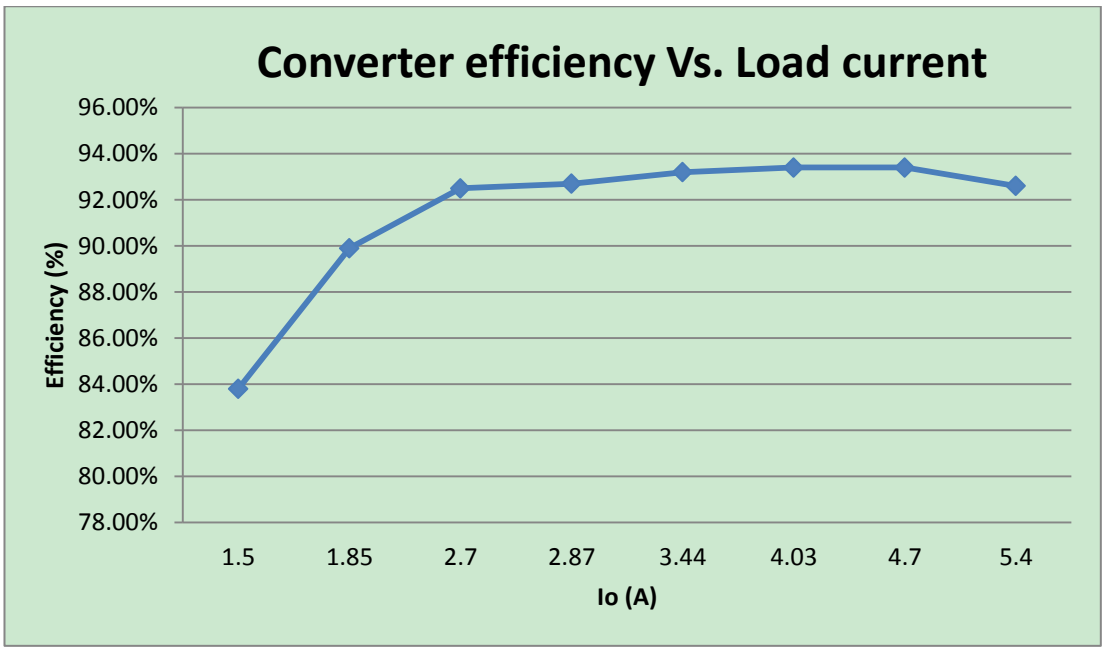


Fig.6.11: Measured converter efficiency with V_{in}=V_{out}=300 V

The input power is measured using DC voltage input and RMS current measurement taken from the DC source, whilst the output power of the prototype module is monitored with a power analyser. Following the same procedure, the conversion efficiency of the prototype was calculated for several load current values and is shown in Fig.6.11. Observe that, during light load conditions, converter efficiency exhibits an increasing trend as load is increased. Efficiency starts to decrease under high load conditions. Note that higher efficiency can be expected with higher operating voltage.

6.4 Scaled-up Example

The circuit configuration of a 5 MW, 50 kV output, 100 A DC/DC converter consisting of 100 kW DAB modules with SiC-MOSFETs, which can be obtained through scaling up the power level of the presented 15 kW module by a factor of 10, is shown in Fig.6.12.

Since the optimum input voltage for single module is 1 kV, the 4 kV input voltage can be obtained using a design with four parallel arms being series connected at the front end. With series connection at the outputs, the proposed converter topology can realise high input to output ratio with low module transformer turns-ratios. In this

case, isolation transformers with unity turns ratio can be achieved which results in simple construction and minimum leakage inductance. Additionally, interleaved control of the module switches can decrease the output ripple considerably, which corresponds to reduce output filter requirements [8]. From calculation, 50 modules are required to address 5 MW power rating. Considering fault-tolerant operation, a level of designed redundancy is provided in this configuration, leading to 56 modules in total.

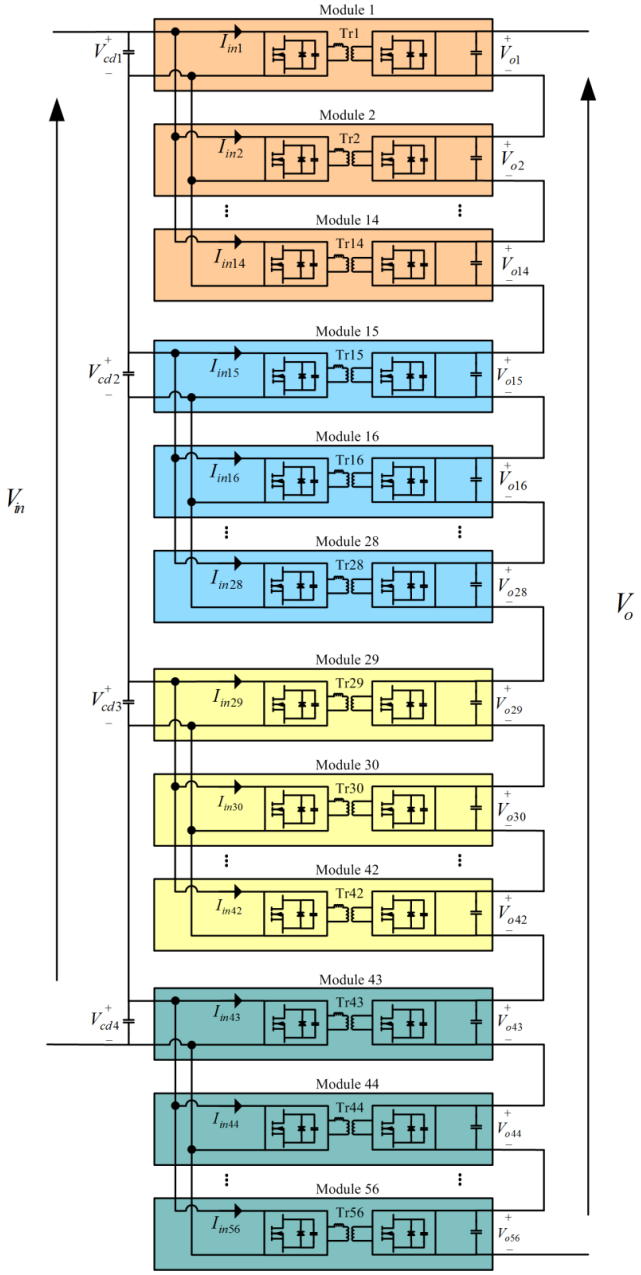


Fig.6.12: 5 MW DC/DC converter with proposed 100 kW DAB module

6.5 Summary

The novel ISIPOS connected topology is applied to a DAB module topology in this chapter. The control scheme proposed in Chapter 5, incorporating power sharing control and fault-tolerant operation, is successfully employed in this converter and simulation results are provided to validate the converter's ability to provide reliable power sharing and fault-tolerant operation. Moreover, a realistic 15 kW DAB module, using 1.7 kV 300 A silicon carbide devices, is built in order to inform design considerations regarding the required footprint for a realistic module, the loss mechanisms, and how a single realistic module building block can be replicated and connected to form a whole ISIPOS converter system. The set-up and experimental results of the 15 kW prototype unit are presented, with an emphasis on the choice of power switches. In addition, a scaled-up converter with targeted 5 MW power capacity, consisting of 56 100 kW DAB modules, shows the possibilities of this proposed ISIPOS DC/DC converter in medium-voltage high-power applications.

6.6 Chapter Reference

[1] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," Industry Applications, IEEE Transactions on, vol. 28, no. 6, pp. 1294-1301, 1992.

[2] F. Z. Peng, L. Hui, S. Gui-Jia and J. S. Lawler, "A new ZVS bidirectional DC-DC converter for fuel cell and battery application," Power Electronics, IEEE Transactions on, vol. 19, no. 1, pp. 54-65, 2004.

[3] R. W. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in Industry Applications Society Annual Meeting, 1988., Conference Record of the 1988 IEEE, pp. 796-805 vol.1, 1988.

[4] G. Ortiz, J. Biela, D. Bortis and J. W. Kolar, "1 Megawatt, 20 kHz, isolated, bidirectional 12kV to 1.2kV DC-DC converter for renewable energy applications," in Power Electronics Conference (IPEC), 2010 International, pp. 3212-3219, 2010.

[5] R. L. Steigerwald, R. W. De Doncker and M. H. Kheraluwala, "A comparison of high-power DC-DC soft-switched converter topologies," Industry Applications, IEEE Transactions on, vol. 32, no. 5, pp. 1139-1145, 1996.

[6] S. Inoue and H. Akagi, "A Bi-Directional Isolated DC/DC Converter as a Core Circuit of the Next-Generation Medium-Voltage Power Conversion System," in Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE, pp. 1-7, 2006.

[7] Z. Biao, S. Qiang, L. Wenhua and S. Yandong, “Overview of Dual-Active-Bridge Isolated Bidirectional DC&DC Converter for High-Frequency-Link Power-Conversion System,” Power Electronics, IEEE Transactions on, vol. 29, no. 8, pp. 4091-4106, 2014.

[8] P. S. Shenoy and P. T. Krein, “Local control of multiple module dc-dc converters,” in Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on, Boulder, CO, pp. 1-6, 2010.

Chapter 7: Conclusions

Studies have shown that MVDC connection may be advantageous for long cable networks, such as the collection grids for offshore wind farms. Realising the benefits of MVDC will require the use of high-power DC/DC converters capable of operating at the required network voltage, e.g. a wind generator 2-6 kV DC link must be stepped-up to a voltage (30-60 kV DC) compatible with an efficient wide area network connection, which is beyond the voltage capability of existing power semiconductors. Concerning the challenging in DC/DC conversion of the offshore DC collection network, the study performed through out the thesis has convered the issues as the parallel-series connected modular DC/DC converter topologies, control designs, with emphasis on the power sharing control between the modules under conditions of module parameter mismatch and internal fault-tolerant operation.. To sum up, all the DC/DC converters presented in this thesis could be good potential solutions for high-power DC/DC conversion. The conclusion for each chapter, the main contributions of this investigation, and suggestions for future research are presented in the following sections.

Chapter 1 introduces the background to offshore wind energy development, explains the benefits of the MVDC collection network for offshore wind farms and discusses the challenges in applying present DC/DC converter topologies at the required network voltages. In addressing the challenges, Chapter 2 reviews four converter topologies that are potentially suitable for high-power medium-voltage application. In contrast to other alternatives, the proposed parallel-series connected modular converters with low-power rating transformer-coupled modules present many advantages, such as lower *dv/dt*, smaller footprint (lighter weight and smaller size), high efficiency and higher reliability, making the converter especially suitable for the proposed MVDC application. Chapter 3 assesses four different parallel-series connections, potential module topologies and different choices of transformer cores. From these assessments, an IPOS connected phase shifted full-bridge module, and DAB module with medium-frequency NANOPERM transformer is selected.

In Chapter 4, a new ‘master-slave’ control strategy is proposed for the IPOS connected modular converter to ensure equal power sharing between the modules when modules have mismatched parameters. Non-linear controller is introduced to offer improved transient response and robustness to parameter variations when compared to a conventional PI controller. The feasibility for power sharing is assessed through simulation and experimental results that are presented based on a 10-module application-level simulation and a 4-module scaled-down experimental test rig respectively. High reliability is one of the important merits of the proposed converter due to its inherent redundancy feature. With regard to redundancy for internal module faults, especially in the event of a fault in the master module, the new ‘non-dedicated master’ control scheme allows fault-tolerant operation to be achieved independent of fault location without any compromise to power sharing between the modules. The validity of the presented fault-ride-through control scheme has been confirmed by simulation and experimentation.

Chapter 5 extends the parallel-series connection presented in Chapter 4 to a new ISIPOS connection. This new high-power DC/DC converter, where full-bridge DC/DC modules are input-series-input-parallel output-series connected, is a promising topology for high-power medium-voltage applications since the input-series-input-parallel connection enables device rating and switching frequency to be further optimised compared with input-parallel connection. For the new connection, this chapter presents the power balancing principle and control scheme that provide equal power distribution between modules during steady-state and dynamic conditions. In addition, emphasis has been placed on fault-tolerant operation by exploiting modularity to provide redundancy in the event of any failure. The power sharing control ability of the proposed control scheme is shown to effectively balance power distribution during dynamic operation, and the converter exploits (n+1) redundancy with the proposed fault detection and redundancy control strategy. Operation is confirmed through simulation and experimentation.

To address the issue of bidirectional power transfer, a new high-power DC/DC converter with ISIPOS connection is developed in Chapter 6 to allow bidirectional power flow, using a DAB module topology. Its power balancing method and fault operation are analysed, and its feasibility is assessed through 1 MW and 5 MW

converter simulations. In addition, a 15 kW DAB module prototype, implemented using 1.7 kV 300 A silicon-carbide MOSFETs, shows the possibilities of this proposed ISIPOS DC/DC converter in high-power medium-voltage applications.

7.1 Author's Contribution

The main research contributions presented in this thesis are:

- A high-power DC/DC converter with IPOS connected transformer-coupled modules, which is scalable for high-power medium-voltage applications, is proposed for MVDC collection networks for offshore wind farms.
- The transfer functions obtained from small-signal modelling and from linearised large-signal modelling of the IPOS DC/DC converter are presented to assist in understanding converter behaviour, and in designing the controller.
- A power sharing control scheme, which includes a Lyapunov-based output voltage controller, modular output voltage controllers and inner current controllers, is proposed to achieve power balancing between the modules. Theoretical analysis and experimental results show that the non-linear controller, based on the large-signal model, facilitates faster dynamic response at start-up and higher disturbance rejection capability in comparison with a conventional linear controller.
- A new controller, based on the concept of the 'non-dedicated master', is developed for the IPOS connected modular converter to address the issue of master module failure in the commonly-used fixed 'master-slave' scheme by permitting arbitrary reallocation of the role of 'master' to another healthy module when the original master module fails. This new control scheme allows fault-tolerant operation to be achieved independent of fault location.
- A modified ISIPOS connected modular DC/DC converter brings further optimisation to the converter by introducing novel input-series-input-parallel connection, which in effect results in lower power rating of individual modules compared with the IPOS connected modular DC/DC converter.
- Theoretical analysis regarding power sharing in the ISIPOS converter is

presented. Based on this, an effective control strategy for power balancing between modules in the presences of module parameter mismatches, and fault-tolerant operation are developed for this new ISIPOS converter.

- Extension of the proposed uni-directional ISIPOS connected modular DC/DC converter to a converter with bidirectional power flow capability is realised in order to meet the development of renewable energy. With the proposed dedicated power sharing control and fault-tolerant operation control, the new converter consisting of transformer-coupled DAB modules has no difficulty in term of power sharing and internal module fault operation.
- The three presented multi-module converters consisting of *n* transformer-coupled modules, whose inputs and outputs are parallel or series connected, are all well suited for an offshore DC collection grid due to several attractive properties, including that each module only contributes a small fraction of the total power and operates at voltages and currents that can be supported by available power semiconductors, that the modular structure allows the converter to be re-configured and higher switching frequency can be achieved without significant design challenges, and that redundant modules in this modular configuration provide fault ride through operation with the designed level of redundancy, which all make deployment of DC collection networks in offshore wind farm applications more feasible and effective. Note that the proposed converters and control strategies can be readily extended to any number of modules and any allowable level of redundancy, making them promising for high-power applications.

7.2 Suggestions for Future Research

Three types of parallel-series connected modular DC/DC converters that are suitable for high-power medium-voltage application have been proposed in this thesis to address the challenges of high-power DC/DC converters. The appropriateness for offshore collection applications such as scalability, high efficiency, low production cost, small footprint, high reliability and controlled *dv/dt* has made this type of converter the most promising solution. Additionally, the proven viability and

robustness of the converter topologies and control schemes also increase confidence in the proposed solution. However, there are more suggestions for future research regarding the converters presented in this thesis.

- The ISIPOS connection can be further extended to input-series-input-parallel, output-series-output-parallel (ISIPOSOP) connection.
- More work is needed in order to validate the proposed converter topologies and the control schemes in the context of the offshore DC collection network, where the terminal of the DC/DC converter is connected to a voltage source instead of a resistive load.
- The increased operating frequency of the AC link can reduce the size and weight of the transformer. However, the maximum reduction that can be achieved will be limited by insulation and isolation requirements. Further investigation is required to analyse the most suitable switching frequency, considering transformer size, cost and power loss. Another possibility is to use a single multi-phase transformer to replace the isolated transformers in each module.
- The crucial aspect of using redundant modules to provide redundancy is the trade-off between cost and reliability. The most cost-effective level of redundancy should be identified.

.

Appendices

The appendices show details of the practical implementation, including the test rigs, circuit boards and also program codes. The list of tables and figures, and the author's publications are also presented.

Appendix A

This appendix shows the structures of the two experimental prototypes used in this study.

A.1 Experimental Prototype A

This section presents the hardware components and controller used in the practical implementation of the proposed DC/DC converter consisting of four full-bridge modules. Note that both of the IPOS connected modular converters presented in Chapter 4 and the ISIPOS connected modular converter presented in Chapter 5 use the same prototype to verify the proposed power sharing control scheme and fault-tolerant operation. Table A.1 shows the main components of the hardware structure.

Table A.1 List of the main components in the prototype

Component Number	***Component Name***
A1.1	Digital Signal Processor
A1.2	DSP Interfacing Circuits
A1.3	Gate Drive Circuits
A1.4	Voltage and Current Measurement Circuits
A1.5	DC Voltage Source
A1.6	Digital Oscilloscope
A1.7	Four Full-bridge DC/DC Modules

A.1.1 Digital Signal Processor

The Infineon Tricore 1796 32-bit microcontroller DSP shown in Fig.A.1 measures digitised voltage and current signals, then uses these as feedback to perform the proposed control algorithm that generates the driving signals for the power switches. The main features of the TC1796 DSP are:

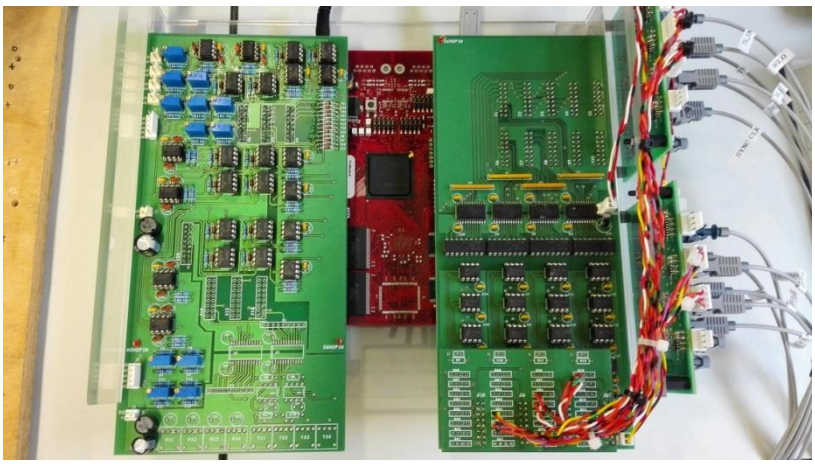


Fig.A.1: Infineon 32-bit TriCore 1796 DSP (the lower board) with two interface boards (two upper boards)

The main features of TC1796 are listed below:

- Maximum CPU clock frequency 150 MHz at full automotive temperature range from -40 $^{\circ}$C to +125 $^{\circ}$C
- Single precision floating point unit (FPU)
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
- Two 16-channel Analog-to-Digital Converter (ADC) units with selectable 8-bit, 10-bit, or 12-bit resolution and one 4-channel fast analog-to-digital converter unit (FADC) supports 10-bit resolution with maximum conversion time of 280 ns.
- Multiple on-chip memories including 2 Mbyte Program Flash Memory with ECC, 128 Kbyte data flash memory, 192 Kbyte on chip SRAM and 16 Kbyte instruction cache
- Two general purpose timer array modules (GPTA) and separate local timer cell array (LTCA2) with the ability of digital signal filtering and timer functionality
- Clock Generation Unit with PLL

- 123 digital general purpose I/O lines, 4 input lines and digital I/O ports with 3.3 V capability
- Requires only a single 3.3 V supply

A.1.2 DSP Interfacing Circuits

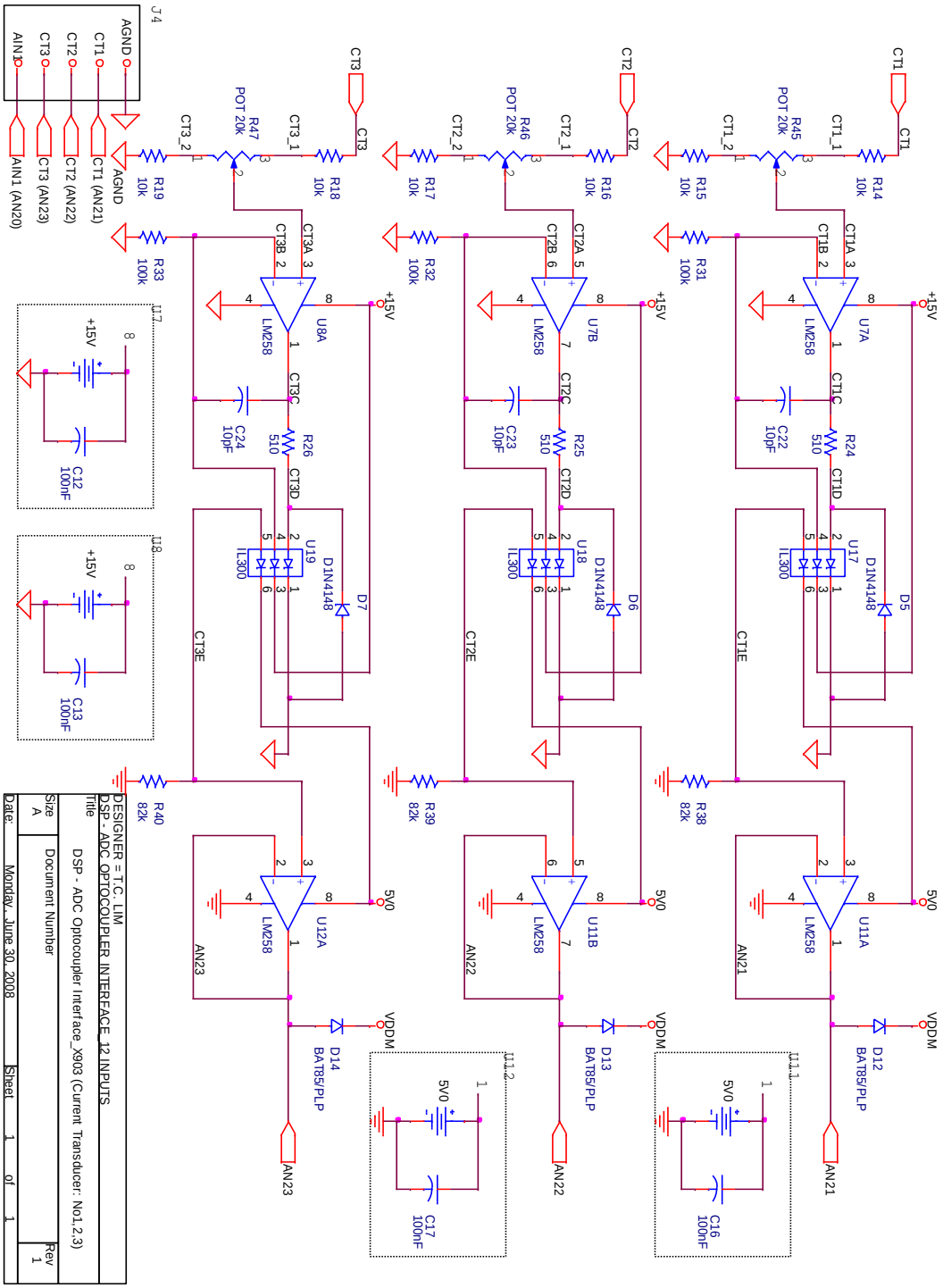
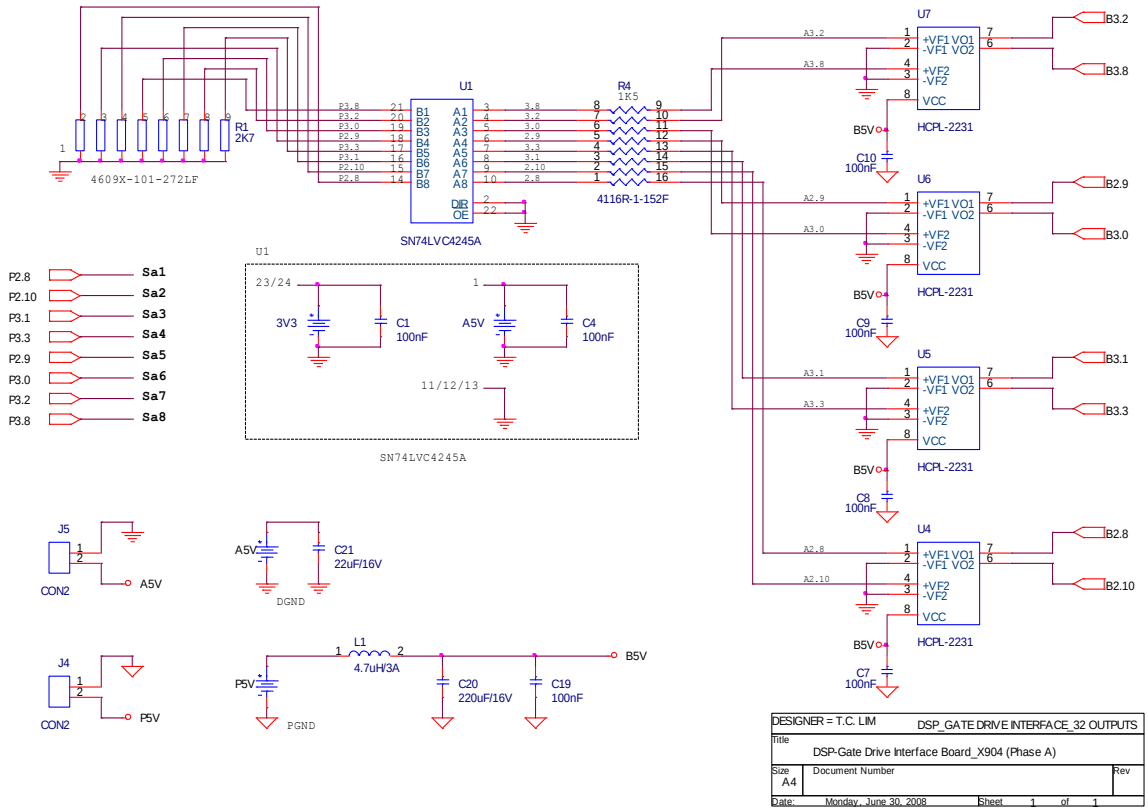


Fig.A.2: Interfacing circuit schematic of the ADC channels



LAYOUT OF OUTPUT PINS ON CONNECTION BOARD

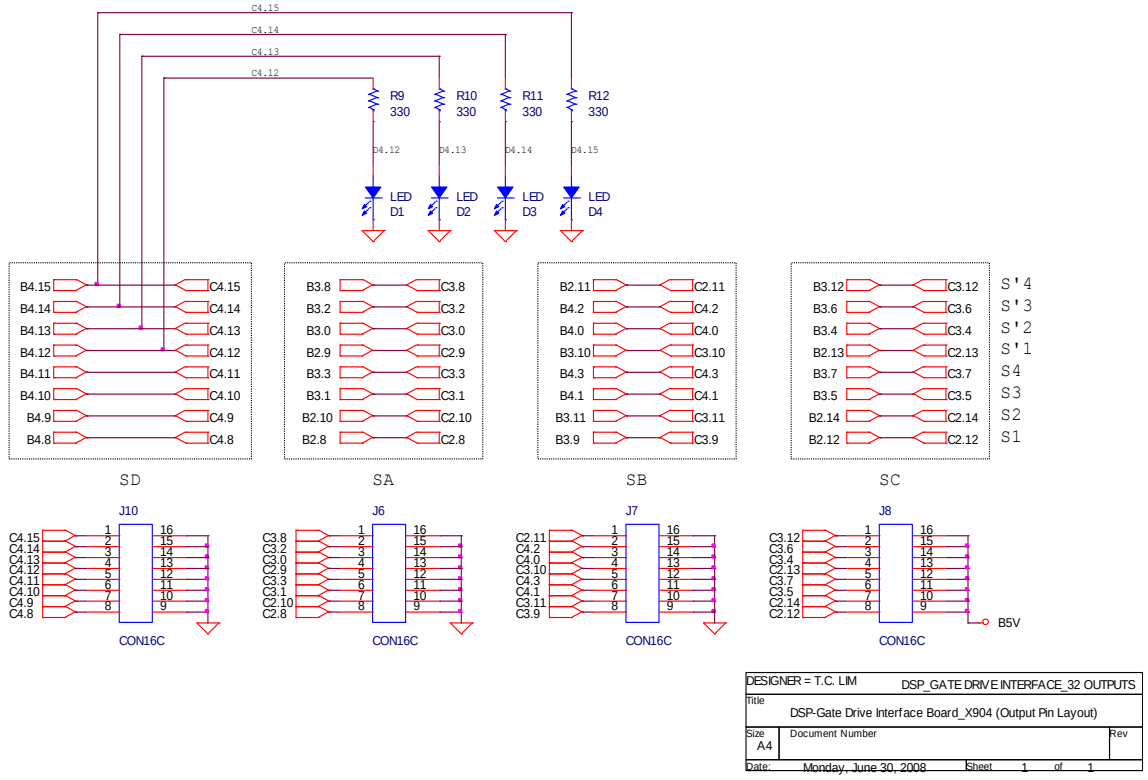


Fig.A.3 Interfacing circuit schematic of the PWM channels

The two interface boards implemented in this circuit are shown in Fig.A.1, with one circuit isolating the ADC channels of the controller from the voltage and current transducer circuits, and the other isolating the PWM channels from the gate drive circuits and scaling-up the PWM output from 3.3 V to 5 V. The two circuit schematics are given in Fig.A.2 and Fig.A.3 separately. Note that the interfacing circuits require DC supplies with different grounds in order to bias the various control circuits.

A.1.3 Gate Drive Circuits

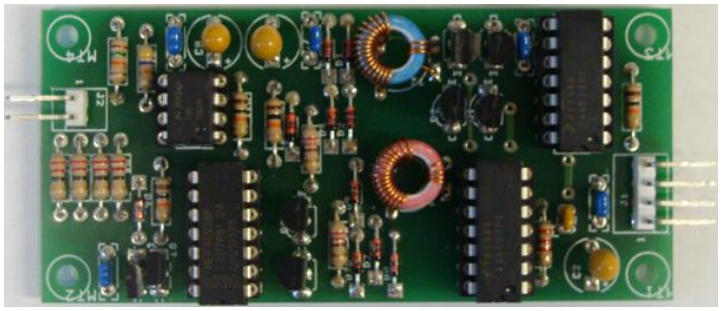


Fig.A.4 Gate drive circuit

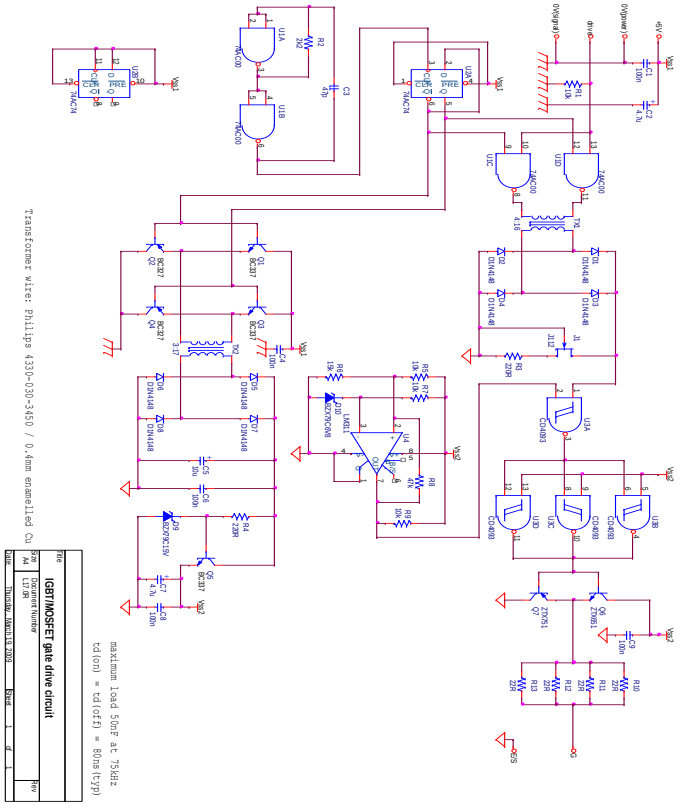


Fig.A.5 Gate drive circuit schematic

Fig.A.4 shows the gate drive circuit implemented in this test rig and the circuit schematic is shown in Fig.A.5. The gate drive circuit is used to provide electrical isolation between the PWM interface circuit and gate drive circuits, amplify the 5 V PWM signal output from the DSP interfacing board to 15 V for the power switches and source enough current for the switching devices to be turned on.

A.1.4 Voltage and Current Measurement Circuits

The voltage transducer shown in Fig.A.6, based around an LEM-LV 25-P sensing device, is used to measure voltage signals and has a sensing range of 0-500 V and an output range of 0-10 V. In the current transducer shown in Fig.A.7, an LEM-LA 55-P Hall-effect sensing device is employed to measure both AC and DC, and has a sensing range of 0-50 A. The LV 25-P and LA 55-P transducer data sheets are provided and the actual transducer circuits are shown in Fig.A.8.

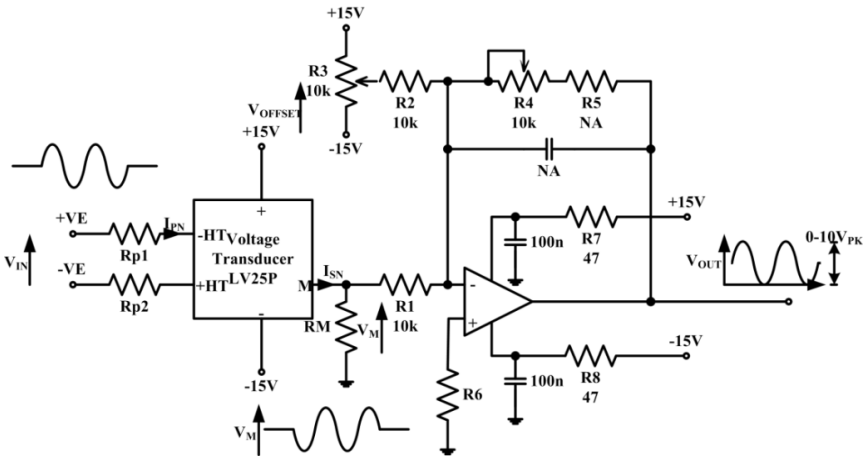


Fig.A.6: Hall-effect voltage transducer circuit schematic

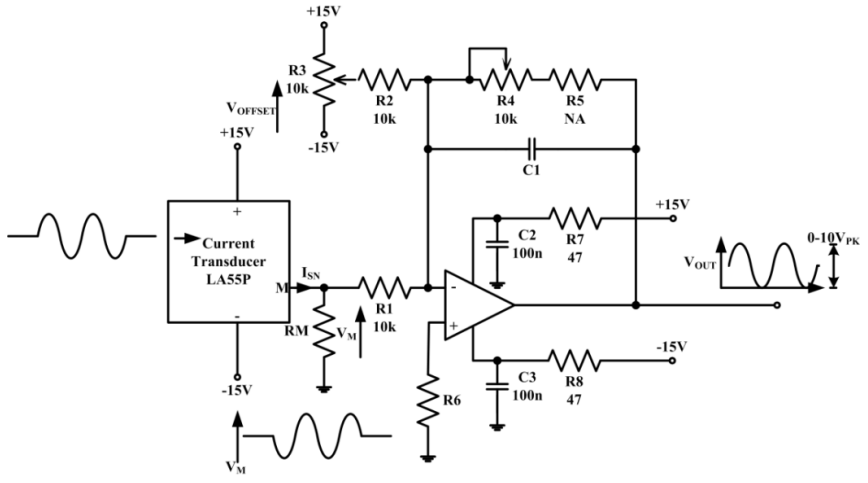
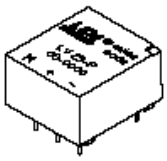


Fig.A.7: Hall-effect current transducer circuit schematic

Voltage Transducer LV 25-P

I_{PN} = 10 mA
V_{PN} = 10 .. 500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current		10		mA
I_P	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 10 mA_{max}	30	190	Ω
		@ ± 14 mA_{max}	30	100	Ω
	with ± 15 V	@ ± 10 mA_{max}	100	350	Ω
		@ ± 14 mA_{max}	100	190	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@±15 V) + I_S		mA
V_d	R.m.s. voltage for AC isolation test [1], 50 Hz, 1 mn		2.5		kV

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 0.9		%
		@ ± 15 V (± 5 %)	± 0.8		%
ε_L	Linearity		< 0.2		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.15	mA
I_{OT}	Thermal drift of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time [2] @ 90 % of $V_{P\,max}$		40		µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Primary coil resistance @ T_A = 70°C		250	Ω
R_S	Secondary coil resistance @ T_A = 70°C		110	Ω
m	Mass		22	g
	Standards [3]		EN 50178	

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

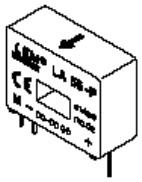
Notes : [1] Between primary and secondary
[2] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit)
[3] A list of corresponding tests is available

981125/14

Current Transducer LA 55-P

I_{PN} = 50 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).



Electrical data

I_{PN}	Primary nominal r.m.s. current				50		A
I_P	Primary current, measuring range				0 .. ± 70		A
R_M	Measuring resistance @		T_A = 70°C		T_A = 85°C		
			$R_{M\,min}$	$R_{M\,max}$	$R_{M\,min}$	$R_{M\,max}$	
	with ± 12 V	@ ± 50 A_{max}	10	100	60	95	Ω
		@ ± 70 A_{max}	10	50	60[1]	60[1]	Ω
	with ± 15 V	@ ± 50 A_{max}	50	160	135	155	Ω
		@ ± 70 A_{max}	50	90	135[2]	135[2]	Ω
I_{SN}	Secondary nominal r.m.s. current				50		mA
K_N	Conversion ratio				1 : 1000		
V_C	Supply voltage (± 5 %)				± 12 .. 15		V
I_C	Current consumption				10 (@ ± 15 V) + I_S		mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 mn				2.5		kV

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25°C	@ ± 15 V (± 5 %)		± 0.65	%
		@ ± 12 .. 15 V (± 5 %)		± 0.90	%
ε_L	Linearity			< 0.15	%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.2	mA
I_{OM}	Residual current [3] @ I_P = 0, after an overload of 3 x I_{PN}			± 0.3	mA
I_{OT}	Thermal drift of I_O	0°C .. + 70°C	± 0.1	± 0.5	mA
		- 25°C .. + 85°C	± 0.1	± 0.6	mA
t_{ra}	Reaction time @ 10 % of $I_{P\,max}$			< 500	ns
t_r	Response time @ 90 % of $I_{P\,max}$			< 1	µs
di/dt	di/dt accurately followed			> 200	A/µs
f	Frequency bandwidth (- 1 dB)			DC .. 200	kHz

General data

T_A	Ambient operating temperature		- 25 .. + 85	°C
T_S	Ambient storage temperature		- 40 .. + 90	°C
R_S	Secondary coil resistance @	T_A = 70°C	80	Ω
		T_A = 85°C	85	Ω
m	Mass		18	g
	Standards [4]		EN 50178	

Notes : [1] Measuring range limited to ± 60 A_{max}
[2] Measuring range limited to ± 55 A_{max}
[3] Result of the coercive field of the magnetic circuit
[4] A list of corresponding tests is available

Features

- Closed loop (compensated) current transducer using the Hall effect
- Printed circuit board mounting
- Insulated plastic case recognized according to UL 94-V0.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

980706/8

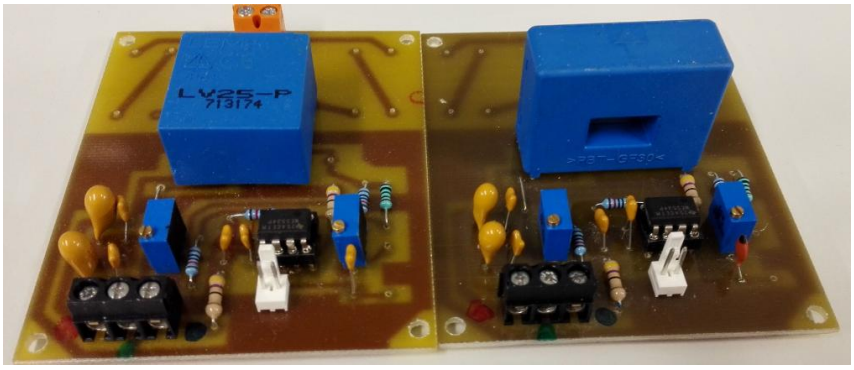


Fig.A.8: Voltage and current transducer

A.1.5 DC Voltage Source

An Argantix 600 V, 25 A DC power supply, shown in Fig.A.9, is used provide the DC voltage to the experimental test rig.

Fig.A.9 DC power supply

A.1.6 Digital Oscilloscope

A Tektronix TDS 2024 200 MHz, 2 GS/s digital oscilloscope, shown in Fig.A.10, is used to measure the voltage and current signals from current and voltage probes.

Fig.A.10 Digital oscilloscope

A.1.7 Four Full-bridge DC/DC Modules

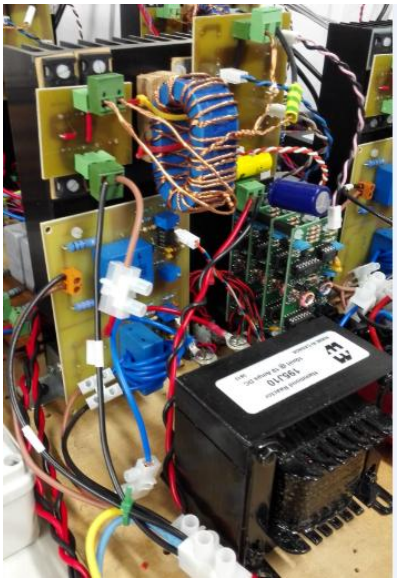


Fig.A.11: Single full-bridge DC/DC module

FORM Identifier: F 108 Revision: 04 Page: 1/1	Product specification for inductive components	MAGNETEC GmbH Industriestrasse 7 D-63505 Langenselbold

☐

Client:	MAGNETEC	Magnetec P/N:	M-134	Magnetec A/N:	12119
Client's P/N:	-	PS Index:	01	PS Revision:	00
Subject:	EMC Wandler			Type:	E

1. Mechanical Outline

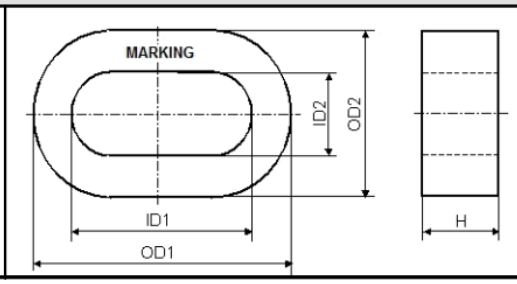
Nominal core dimensions:

50 x 40 x 20

Finished product dimensions:

OD ≤ **60,0 (1) / 40,0 (2)**
ID ≥ **43,0 (1) / 25,0 (2)**
H ≤ **22,3**

[dimensions] = mm



2. Core data

Core material:	**NANOPERM®**	L_{Fe} = **14,1 cm**	A_{Fe} = **0,8 cm²**
Nominal values:	Permeability level	@ frequency	@ H peak
	45.000	**10 kHz**	**3,0 mA/cm**

3. Inspection values

	Measured value	Measurement limits	Frequency	Ieff x N [mA x turn]
	AL1 [µH]	**20,0 - 40,0**	**10 kHz**	**30,0**

4. Core finishing

Type:	**Epoxy coated**
Marking:	**MAGNETEC M-134-01 YM (YM = Year/Month), acc. to IEC 62 5.1**
Packaging:	**14 pcs. per layer; 5 layers per carton box; PU = 60 pcs.**

5. Comments:

Index / Revision	Alteration	Date
01 / 00	Product Specification	13.08.2001

Created:	Á. Kovách 13.08.2001	Approved (Techn):	F. Zámborszky 13.08.2001	Approved (Quality):	V. Káposztás 13.08.2001	Released:	F. Rauscher 17.08.2001

Fig.A.12 Magnatec NANOPERM nano-crystalline core data

A single module, as shown in Fig.A.11, consists of one inverter bridge constructed using Infineon IPB027N10N3 MOSFETs (G V_{DS}=100 V and $R_{ds(on)}$=2.7 mΩ), one Magnatec GmbH M-134-01-E NANOPERM® nano-crystalline core transformer, one bridge rectifier constructed using Infineon SIDC23D60E6 diodes, and an output LC filter.

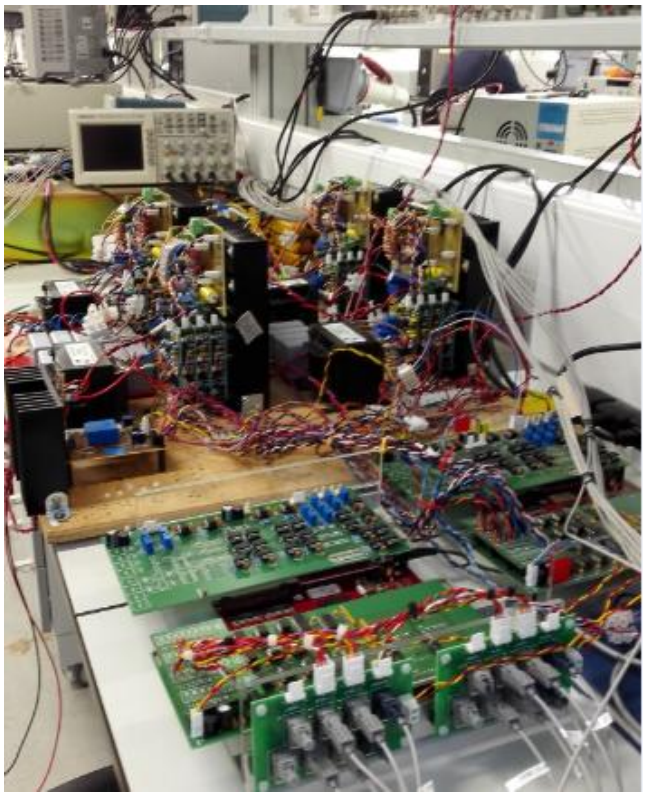


Fig.A.13 Experimental prototype A

The complete prototype IPOS (or ISIPOS) connected modular DC/DC converter with four full-bridge modules is shown in Fig.A.13. Apart from the previously mentioned main components, the prototype also includes multi-meters, current and voltage probes, and a resistor bank.

A.2 Experimental Prototype B

The main components of the 15 kW DAB DC/DC converter presented in Chapter 6 are introduced in this section. Note that the controller, DC voltage source and biasing DC supply used in this experimental test rig are the same as those used in prototype A. Table A.2 shows the main components in the hardware structure.

Table A.2 List of the main components in the prototype

Component Number	*Component Name*
A.2.1	Two inverter/rectifier units with CREE SiC-MOSFET CAS300M17BM2
A.2.2	Power Analyser
A.2.3	Transformer with added leakage inductance
A.2.4	Digital Oscilloscope

A.2.1 Inverter/rectifier Unit

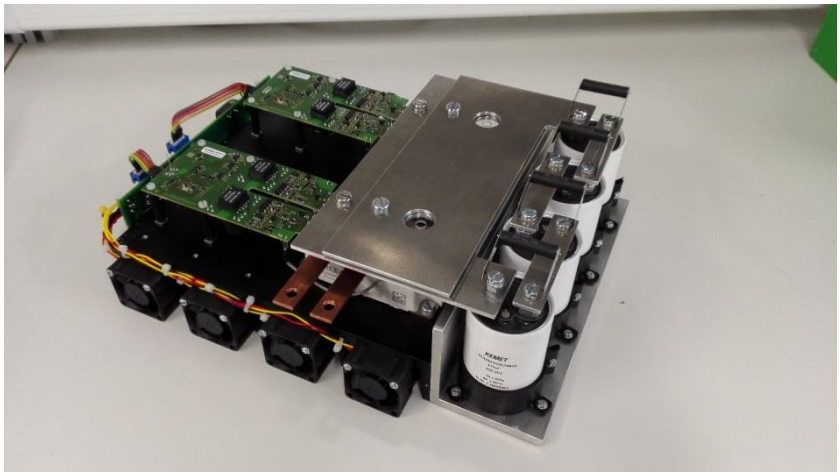


Fig.A.14: Inverter/rectifier unit

Table A.3 List of the main components in an inverter/rectifier unit

Component Name	*Component Value*	*Quality*
Input capacitor	470 μF, 450 V	4
Output capacitor	470 μF, 450 V	4
Heatsink 1	0.3 °C/W, 250 x 250 x 40 mm	1
Heatsink 2	0.33 °C/W, 200 x 250 x 40 mm	1
Axial fan	40MM, 12VDC, 0.133A	8
SiC-MOSFET	1700 V 325 A	2
Gate drive board	1700 V	2

The prototype consists of two inverter/rectifier units.

A.2.2 Power Analyser

The PM100 single phase power analyser from Voltech is used to measure the output power, therefore deliver accurate power efficiency.

Fig.A.15 Power Analyser

A.2.3 Transformer

The outsource transformer from PaytonGroup is rated at 20 kVA with 1:2 turn ratio and 10 μH leakage inductance. The maximum voltage operating level is 1 kV. The added leakage inductance is 85 μH.

A.2.4 Digital Oscilloscope

The 500 MHz, 2 GS/s LeCroy wave jet 354 digital oscilloscope shown in Fig.A.16 is used to measure the voltage and current signals from current and voltage probes.

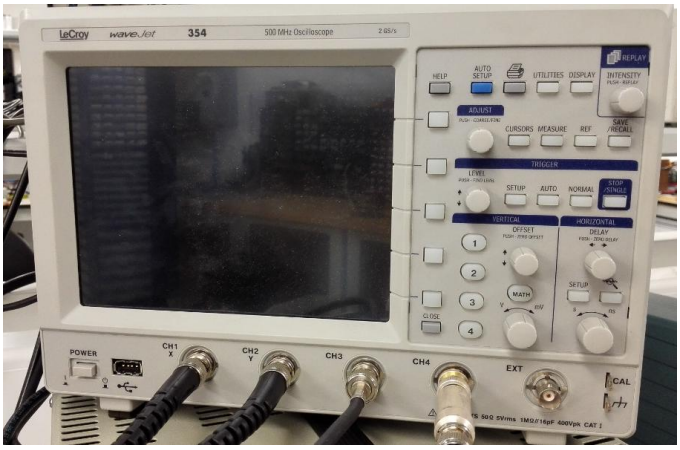


Fig.A.16 Digital oscilloscope

The complete prototype of the proposed DAB DC/DC converter is shown in Fig.A.17.

Fig.A.17 Experimental prototype B

Appendix B

The selected program codes for experimental validations are presented.

B.1 Normal Operation of IPOS Connected DC/DC Converter

A. Common duty-cycle control

```
/*
**********************************************************************
@Note
OUTPUT-0 P2-8 LTC3  Module 1 Leading High
OUTPUT-1 P2-9 LTC7  Module 1 Lagging High
OUTPUT-2 P2-10 LTC5  Module 1 Leading Low
OUTPUT-3 P2-11 LTC33  Module 4 Lagging Low
OUTPUT-8 P3-0 LTC9  Module 1 Lagging Low
OUTPUT-9 P3-1 LTC11  Module 2 Leading High
OUTPUT-11 P3-3 LTC13  Module 2 Leading Low
OUTPUT-14 P3-6 LTC15  Module 2 Lagging High
OUTPUT-17 P3-9 LTC19  Module 3 Leading High
OUTPUT-18 P3-10 LTC23  Module 3 Lagging High
OUTPUT-19 P3-11 LTC21  Module 3 Leading Low
OUTPUT-20 P3-12 LTC17  Module 2 Lagging Low
OUTPUT-24 P4-0 LTC25  Module 3 Lagging Low
OUTPUT-25 P4-1 LTC27  Module 4 Leading High
OUTPUT-26 P4-2 LTC31  Module 4 Lagging High
OUTPUT-27 P4-3 LTC29  Module 4 Leading Low
**********************************************************************
*/

// USER CODE BEGIN (GPTA0_General,7)
// Variable declarations
```

```
int db=60;              //deadband
double buf1v1 = 0.0;        //module 1 voltage   once
double buf2v1 = 0.0;        //module 2 voltage
double buf3v1 = 0.0;        //module 3 voltage
double buf4v1 = 0.0;        //module 4 voltage
double buf1i1 = 0.0;        //module 1 current
double buf2i1 = 0.0;        //module 2 current
double buf3i1 = 0.0;        //module 3 current
double buf4i1 = 0.0;        //module 4 current
double bufLoadv1 = 0.0;     //converter load voltage
double buf1v2 = 0.0;        //module 1 voltage   twice
double buf2v2 = 0.0;        //module 2 voltage
double buf3v2 = 0.0;        //module 3 voltage
double buf4v2 = 0.0;        //module 4 voltage
double buf1i2 = 0.0;        //module 1 current
double buf2i2 = 0.0;        //module 2 current
double buf3i2 = 0.0;        //module 3 current
double buf4i2 = 0.0;        //module 4 current
double bufLoadv2 = 0.0;     //converter load voltage
int Ts=3997;                //counter for one cycle
int TON,TON_C;              //open loop on and off time
double Tc = 4E-4;           //time per cycle
double t;                   //time to control the current reference value
int JJ=1;                   //time to step change for current reference
int II=1;           // pattern 1 and pattern 2 chosen value
int del =100;               //for phase shift control
int del1;
int del2;
int del3;
int del4;

// USER CODE BEGIN (SRN22,1)
// Control algorithm
void INTERRUPT (GPTA0_SRN22INT) GPTA0_viSRN22(void)
{
// USER CODE BEGIN (SRN22,2)
// USER CODE END
if(GPTA0_SRSS2_LTC01)      //  LTC1 event (= compare with last timer)
{
GPTA0_SRSC2 = 0x00000002; //  reset LTC1 service request bit
// USER CODE BEGIN (SRN22,4)
// USER CODE BEGIN (SRN22,4)
del = hard_one_module_PI_part_Y.del1 *1998;
//////////////////////////////////////////////////////
///////Signal for converter 1//////////////////////////
GPTA0_LTCXR02=db;                                       //phase shift pwm
GPTA0_LTCXR03=1998;
GPTA0_LTCXR04=3997;
GPTA0_LTCXR05=1998+db;
GPTA0_LTCXR06=db+del;
GPTA0_LTCXR07=del+1998;
GPTA0_LTCXR08=del;
GPTA0_LTCXR09=1998+db+del;
//////////////////////////////////////////////////////
///////Signal for converter 2//////////////////////////
GPTA0_LTCXR10=db;                                       //phase shift pwm
GPTA0_LTCXR11=1998;
GPTA0_LTCXR12=3997;
```

```
GPTA0_LTCXR13=1998+db;
GPTA0_LTCXR14=db+del;
GPTA0_LTCXR15=del+1998;
GPTA0_LTCXR16=del;
GPTA0_LTCXR17=1998+db+del;
//////////////////////////////////////////////////////
///////Signal for converter 3//////////////////////////
GPTA0_LTCXR18=db;                                       //phase shift pwm
GPTA0_LTCXR19=1998;
GPTA0_LTCXR20=3997;
GPTA0_LTCXR21=1998+db;
GPTA0_LTCXR22=db+del;
GPTA0_LTCXR23=del+1998;
GPTA0_LTCXR24=del;
GPTA0_LTCXR25=1998+db+del;
//////////////////////////////////////////////////////
///////Signal for converter 4//////////////////////////
GPTA0_LTCXR26=db;                                       //phase shift pwm
GPTA0_LTCXR27=1998;
GPTA0_LTCXR28=3997;
GPTA0_LTCXR29=1998+db;
GPTA0_LTCXR30=db+del;
GPTA0_LTCXR31=del+1998;
GPTA0_LTCXR32=del;
GPTA0_LTCXR33=1998+db+del;

//////////////////////////////////////////////////////
///////Get the ADC signal and transfer//////////////////
ADC0_vStartSingleAutoscan();
while (ADC0_ASCRP & 0x000020F0)
;
bufLoadv1 = 0.035526*(ADC0_CHSTAT12 & 0x00000fff)-27.9947;
buf1v1 = 0.03525*(ADC0_CHSTAT4 & 0x00000fff)-29.1849;          //module 1 real voltage
buf2v1 = 0.03687*(ADC0_CHSTAT7 & 0x00000fff)-39.6738;          //module 2 real voltage
buf3v1 = 0.02519*(ADC0_CHSTAT6 & 0x00000fff)-17.7889;    //module 3 real voltage
buf4v1 = 0.03125*(ADC0_CHSTAT5 & 0x00000fff)-23.53125;    //module 4 real voltage
buf1i1 = 0.004694*(ADC0_CHSTAT11 & 0x00000fff)-1.2486;    //module 1 real current
buf2i1 = 0.004476*(ADC0_CHSTAT10 & 0x00000fff)-1.07412;          //module 2 real current
buf3i1 = 0.00311*(ADC0_CHSTAT9 & 0x00000fff)-0.4981;   //module 3 real current
buf4i1 = 0.00335*(ADC0_CHSTAT8 & 0x00000fff)-0.5395;    //module 4 real current
bufLoadv2 = 0.03676*(ADC0_CHSTAT12 & 0x00000fff)-29.3014;
buf1v2 = 0.03752*(ADC0_CHSTAT4 & 0x00000fff)-30.5065;          //module 1 real voltage
buf2v2 = 0.03309*(ADC0_CHSTAT7 & 0x00000fff)-34.9743;          //module 2 real voltage
buf3v2 = 0.02635*(ADC0_CHSTAT6 & 0x00000fff)-18.3136;    //module 3 real voltage
buf4v2 = 0.02809*(ADC0_CHSTAT5 & 0x00000fff)-20.955;    //module 4 real voltage
buf1i2 = 0.0045*(ADC0_CHSTAT11 & 0x00000fff)-1.116;    //module 1 real current
buf2i2 = 0.004198*(ADC0_CHSTAT10 & 0x00000fff)-0.87735;          //module 2 real current
buf3i2 = 0.003093*(ADC0_CHSTAT9 & 0x00000fff)-0.41134;          //module 3 real current
buf4i2 = 0.0033*(ADC0_CHSTAT8 & 0x00000fff)-0.4356;    //module 4 real current
ADC0_vStartSingleAutoscan();
while (ADC0_ASCRP & 0x000020F0)
;

//////////////////////////////////////////////////////
///////Input to PI calculation//////////////////////////
//////////////////////////////////////////////////////
///////Voltage set up reference code//////////////////
t = JJ*Tc;
```

```
            if (t <= 10)            //10s
            {
            hard_one_module_PI_part_U.Load_V_output=20;
            JJ=JJ+1;
            }
else if (t <= 20)       //20s
{
hard_one_module_PI_part_U.Load_V_output=40;
            JJ=JJ+1;
            }
else if
            {
hard_one_module_PI_part_U.Load_V_output=60;
            }
hard_one_module_PI_part_U.Module_Voltage = 0.5*( bufLoadv1+ bufLoadv2);  // read load data
hard_one_module_PI_part_U.Kp_Module_V = 0.07;
hard_one_module_PI_part_U.Ki_Module_V = 12;
hard_one_module_PI_part_U.Module_1_Voltage = 0.5*(buf1v1+buf1v2);  // read module 1 data
hard_one_module_PI_part_U.Kp_Module_1_V = 0.007;
hard_one_module_PI_part_U.Ki_Module_1_V = 30;
hard_one_module_PI_part_U.Module_1_Current = 0.5*(buf1i1+buf1i2);
hard_one_module_PI_part_U.Kp_Module_1_I= 0.65;
hard_one_module_PI_part_U.Ki_Module_1_I =100;

hard_one_module_PI_part_U.Module_2_Voltage = 0.5*(buf2v1+buf2v2);  // read module 2 data
hard_one_module_PI_part_U.Kp_Module_2_V = 0.007;
hard_one_module_PI_part_U.Ki_Module_2_V = 30;
hard_one_module_PI_part_U.Module_2_Current = 0.5*(buf2i1+buf2i2);
hard_one_module_PI_part_U.Kp_Module_2_I= 0.65;
hard_one_module_PI_part_U.Ki_Module_2_I =100;
hard_one_module_PI_part_U.Module_3_Voltage = 0.5*(buf3v1+buf3v2);  // read module 3 data
hard_one_module_PI_part_U.Kp_Module_3_V = 0.007;
hard_one_module_PI_part_U.Ki_Module_3_V = 30;
hard_one_module_PI_part_U.Module_3_Current = 0.5*(buf3i1+buf3i2);
hard_one_module_PI_part_U.Kp_Module_3_I= 0.65;
hard_one_module_PI_part_U.Ki_Module_3_I =100;
hard_one_module_PI_part_U.Module_4_Voltage = 0.5*(buf4v1+buf4v2);  // read module 4 data
hard_one_module_PI_part_U.Kp_Module_4_V = 0.007;
hard_one_module_PI_part_U.Ki_Module_4_V = 30;
hard_one_module_PI_part_U.Module_4_Current = 0.5*(buf4i1+buf4i2);
hard_one_module_PI_part_U.Kp_Module_4_I= 0.65;
hard_one_module_PI_part_U.Ki_Module_4_I =100;

//////////////////////////////////////////////////////
///////Call PI Calculation Function//////////////////////////
hard_one_module_PI_part_step();
// USER CODE END
}
// USER CODE BEGIN (SRN22,8)
// USER CODE END
} //  End of function GPTA0_viSRN22
*/

//////////////////////////////////////////////////////
///////PI Calculation Function //////////////////////////
#include "hard_one_module_PI_part.h"
#include "hard_one_module_PI_part_private.h"
```

```
/* Block signals and states (auto storage) */
D_Work_hard_one_module_PI_part hard_one_module_PI_part_DWork;
/* External inputs (root inport signals with auto storage) */
ExternalInputs_hard_one_module_ hard_one_module_PI_part_U;
/* External outputs (root outports fed by signals with auto storage) */
ExternalOutputs_hard_one_module hard_one_module_PI_part_Y;
/* Model step function */

void hard_one_module_PI_part_step(void)
{
real_T rtb_Sum8;
real_T rtb_Saturation;
real_T rtb_Sum13;
real_T rtb_Saturation1;
real_T rtb_Sum14;
real_T rtb_Saturation2;
real_T rtb_Sum15;
real_T rtb_Saturation3;
real_T rtb_Sum16;
real_T rtb_Saturation4;

//////////////////////////////////////////////////////
///////Output Voltage Loop ////////////////////////////
rtb_Sum8 = hard_one_module_PI_part_U.Load_V_output -
   hard_one_module_PI_part_U.Module_Voltage;
rtb_Saturation = hard_one_module_PI_part_U.Kp_Module_V * rtb_Sum8 +
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE *
hard_one_module_PI_part_U.Ki_Module_V;
if (rtb_Saturation >= 7.0) {
rtb_Saturation = 7.0;
} else {
if (rtb_Saturation <= 0.0) {
rtb_Saturation = 0.0;
}
}
//////////////////////////////////////////////////////
///////Module 1 current loop////////////////////////////
rtb_Sum13 = rtb_Saturation - hard_one_module_PI_part_U.Module_1_Current;
rtb_Saturation1 = hard_one_module_PI_part_U.Kp_Module_1_I * rtb_Sum13 +
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_c *
hard_one_module_PI_part_U.Ki_Module_1_I;
if (rtb_Saturation1 >= 0.975) {
rtb_Saturation1 = 0.975;
} else {
if (rtb_Saturation1 <= 0.025) {
rtb_Saturation1 = 0.025;
}
}
//////////////////////////////////////////////////////
///////Module 2 current loop////////////////////////////
rtb_Sum14 = rtb_Saturation - hard_one_module_PI_part_U.Module_2_Current;
rtb_Saturation2 = hard_one_module_PI_part_U.Kp_Module_2_I * rtb_Sum14 +
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_d *
hard_one_module_PI_part_U.Ki_Module_2_I;
if (rtb_Saturation2 >= 0.975) {
rtb_Saturation2 = 0.975;
} else {
if (rtb_Saturation2 <= 0.025) {
```

```
rtb_Saturation2 = 0.025;
}
}
/////////////////////////////////////////////////////
///////Module 3 current loop//////////////////////////
rtb_Sum15 = rtb_Saturation - hard_one_module_PI_part_U.Module_3_Current;
rtb_Saturation3 = hard_one_module_PI_part_U.Kp_Module_3_I * rtb_Sum15 +
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_e *
hard_one_module_PI_part_U.Ki_Module_3_I;
if (rtb_Saturation3 >= 0.975) {
rtb_Saturation3 = 0.975;
} else {
if (rtb_Saturation3 <= 0.025) {
rtb_Saturation3 = 0.025;
}
}
/////////////////////////////////////////////////////
///////Module 4 current loop//////////////////////////
rtb_Sum16 = rtb_Saturation - hard_one_module_PI_part_U.Module_4_Current;
rtb_Saturation4 = hard_one_module_PI_part_U.Kp_Module_2_I * rtb_Sum16 +
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_f *
hard_one_module_PI_part_U.Ki_Module_4_I;
if (rtb_Saturation4 >= 0.975) {
rtb_Saturation4 = 0.975;
} else {
if (rtb_Saturation4 <= 0.025) {
rtb_Saturation4 = 0.025;
}
}
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE += 2E-5 *
rtb_Sum8;
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_c += 2E-5 *
rtb_Sum13;
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_d += 2E-5 *
rtb_Sum14;
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_e += 2E-5 *
rtb_Sum15;
hard_one_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_f += 2E-5 *
rtb_Sum16;
```

Note that the variable declarations of the proposed control scheme are similar with that of common duty-cycle control, therefore for other operation conditions only the control algorithm code is given here.

B. Proposed control scheme

```
/////////////////////////////////////////////////////
//////////Converter 1 - Slave //////////
rtb_Sum8 = ipos_module_PI_part_U.Load_V_output_ref/4 -
ipos_module_PI_part_U.Module_1_Voltage;
u = ipos_module_PI_part_U.Kp_Module_1_V * rtb_Sum8 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE *
ipos_module_PI_part_U.Ki_Module_1_V;
if (u >= 10.0) {
```

```
u = 10.0;
} else {
if (u <= 0.0) {
u = 0.0;
}
}
rtb_Sum7 = u- ipos_module_PI_part_U.Module_1_Current;
u_1 = ipos_module_PI_part_U.Kp_Module_1_I * rtb_Sum7 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_c *
ipos_module_PI_part_U.Ki_Module_1_I;
if (u_1 >= 0.95) {
u_1 = 0.95;
} else {
if (u_1 <= 0.05) {
u_1 = 0.05;
}
}
ipos_module_PI_part_Y.del1 = u_1;
////////////////////////////////////////////////////
//////////Converter 2 - Slave ////////////////////
rtb_Sum9 = ipos_module_PI_part_U.Load_V_output_ref/4 -
ipos_module_PI_part_U.Module_2_Voltage;
u1 = ipos_module_PI_part_U.Kp_Module_2_V * rtb_Sum9 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE *
ipos_module_PI_part_U.Ki_Module_2_V;
if (u1 >= 10.0) {
u1 = 10.0;
} else {
if (u1 <= 0.0) {
u1 = 0.0;
}
}
rtb_Sum6 = u1 - ipos_module_PI_part_U.Module_2_Current;
u_2 = ipos_module_PI_part_U.Kp_Module_2_I * rtb_Sum6 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_n *
ipos_module_PI_part_U.Ki_Module_2_I;
if (u_2 >= 0.95) {
u_2 = 0.95;
} else {
if (u_2 <= 0.05) {
u_2 = 0.05;
}
}
ipos_module_PI_part_Y.del2 = u_2;
////////////////////////////////////////////////////
//////////Converter 3 - Slave ////////////////////
rtb_Sum10 = ipos_module_PI_part_U.Load_V_output_ref/4 -
ipos_module_PI_part_U.Module_3_Voltage;
u2 = ipos_module_PI_part_U.Kp_Module_3_V * rtb_Sum10 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE *
   ipos_module_PI_part_U.Ki_Module_3_V;
if (u2 >= 10.0) {
u2 = 10.0;
} else {
if (u2 <= 0.0) {
u2 = 0.0;
}
}
```

```
rtb_Sum11 = u2 - ipos_module_PI_part_U.Module_2_Current;
u_3 = ipos_module_PI_part_U.Kp_Module_3_I * rtb_Sum11 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_n *
ipos_module_PI_part_U.Ki_Module_3_I;
if (u_3 >= 0.95) {
u_3 = 0.95;
} else {
if (u_3 <= 0.05) {
u_3 = 0.05;
}
}
ipos_module_PI_part_Y.del3 = u_3;
////////////////////////////////////////////////
//////////Converter 4 - Master ////////////////////
rtb_Sum12 = ipos_module_PI_part_U.Load_V_output_ref -
ipos_module_PI_part_U.Module_Voltage;
X= ipos_module_PI_part_U.Kp_Module_V * (rtb_Sum12 - rtb_Sum12_2);
rtb_Sum12_2 = rtb_Sum12;
u3 = X + ipos_module_PI_part_U.Kd_Module_V * rtb_Sum12;
if (u3 >= 10.0) {
u3 = 10.0;
} else {
if (u3 <= 0.0) {
u3 = 0.0;
}
}
rtb_Sum13 = u3 – u – u1 – u2;
u_4 = ipos_module_PI_part_U.Kp_Module_4_I * rtb_Sum13 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_n *
ipos_module_PI_part_U.Ki_Module_4_I;
if (u_4 >= 0.95) {
u_4 = 0.95;
} else {
if (u_4 <= 0.05) {
u_4 = 0.05;
}
}
ipos_module_PI_part_Y.del4 = u_4;
```

B.2 Fault Operation of IPOS Connected DC/DC Converter

```
////////////////////////////////////////////////
//////////Fault Detection ////////////////////
if (ipos_module_PI_part_U.Load_V_output_ref/4.5 <= ipos_module_PI_part_U.Module_4_Voltage
<= ipos_module_PI_part_U.Load_V_output_ref/3.5) {
ipos_module_PI_part_Y.del1 = u_1;
ipos_module_PI_part_Y.del2 = u_2;
ipos_module_PI_part_Y.del3 = u_3;
ipos_module_PI_part_Y.del4 = u_4; //repeat the previous code for normal operation
} else {
////////////////////////////////////////////////
//////////Converter 1 – New Master //////////
rtb_Sum8 = ipos_module_PI_part_U.Load_V_output_ref -
ipos_module_PI_part_U.Module_Voltage;
X = ipos_module_PI_part_U.Kp_Module_V * (rtb_Sum8 - rtb_Sum8_2);
rtb_Sum8_2 = rtb_Sum8;
u= X + X + ipos_module_PI_part_U.Kd_Module_V * rtb_Sum8;
```

```
if (u >= 10.0) {
u = 10.0;
} else {
if (u <= 0.0) {
u = 0.0;
}
}
rtb_Sum7 = u - u1 – u2;
u_1 = ipos_module_PI_part_U.Kp_Module_1_I * rtb_Sum7 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_c *
ipos_module_PI_part_U.Ki_Module_1_I;
if (u_1 >= 0.95) {
u_1 = 0.95;
} else {
if (u_1 <= 0.05) {
u_1 = 0.05;
}
}
ipos_module_PI_part_Y.del1 = u_1;
//////////////////////////////////////////////////
//////////Converter 2 - Slave ////////////////////
rtb_Sum9 = ipos_module_PI_part_U.Load_V_output_ref/3 -
ipos_module_PI_part_U.Module_2_Voltage;
u1 = ipos_module_PI_part_U.Kp_Module_2_V * rtb_Sum9 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE *
ipos_module_PI_part_U.Ki_Module_2_V;
if (u1 >= 10.0) {
u1 = 10.0;
} else {
if (u1 <= 0.0) {
u1 = 0.0;
}
}
rtb_Sum6 = u1 - ipos_module_PI_part_U.Module_2_Current;
u_2 = ipos_module_PI_part_U.Kp_Module_2_I * rtb_Sum6 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_n *
ipos_module_PI_part_U.Ki_Module_2_I;
if (u_2 >= 0.95) {
u_2 = 0.95;
} else {
if (u_2 <= 0.05) {
u_2 = 0.05;
}
}
ipos_module_PI_part_Y.del2 = u_2;
//////////////////////////////////////////////////
//////////Converter 3 - Slave ////////////////////
rtb_Sum10 = ipos_module_PI_part_U.Load_V_output_ref/3 -
ipos_module_PI_part_U.Module_3_Voltage;
u2 = ipos_module_PI_part_U.Kp_Module_3_V * rtb_Sum10 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE *
   ipos_module_PI_part_U.Ki_Module_3_V;
if (u2 >= 10.0) {
u2 = 10.0;
} else {
if (u2 <= 0.0) {
u2 = 0.0;
}
```

```
}
rtb_Sum11 = u2 - ipos_module_PI_part_U.Module_2_Current;
u_3 = ipos_module_PI_part_U.Kp_Module_3_I * rtb_Sum11 +
ipos_module_PI_part_DWork.DiscreteTimeIntegrator_DSTATE_n *
ipos_module_PI_part_U.Ki_Module_3_I;
if (u_3 >= 0.95) {
u_3 = 0.95;
} else {
if (u_3 <= 0.05) {
u_3 = 0.05;
}
}
ipos_module_PI_part_Y.del3 = u_3;
}
```

B.3 Normal Operation of ISIPOS Connected DC/DC Converter

Module 1 is chosen as the example to explain the control algorithm.

```
//////////////////////////////////////////////////
///////////ISIPOS proposed control scheme //////////////////////
//////////////////////////////////////////////////

////////////Load voltage regulation/////////

rtb_load = ISIPOS_controlled_PI_U.Load_ref -
ISIPOS_controlled_PI_U.Load_real_voltage;
d_total = ISIPOS_controlled_PI_U.Kp_Module_Load *
rtb_load + ISIPOS_controlled_PI_DWork.DiscreteTimeIntegrator_DSTATE_k *
ISIPOS_controlled_PI_U.Ki_Module_Load;
if (d_total >= 0.975) {
d_total = 0.975;
} else {
if (d_total <= 0.025) {
d_total = 0.025;
}
}
//////////////////////////////////////////////////
////////////Module 1 2 and 3 4 voltage sharing part//////////
rtb_voltage_1_3 = ISIPOS_controlled_PI_U.Module_1_Voltage_1 -
(ISIPOS_controlled_PI_U.Module_1_Voltage_1 +
ISIPOS_controlled_PI_U.Module_3_Voltage_1) * 0.5;
d_V_1 = ISIPOS_controlled_PI_U.Kp_Module_1_U * rtb_voltage_1_3
+ ISIPOS_controlled_PI_DWork.DiscreteTimeIntegrator_DSTATE_e *
ISIPOS_controlled_PI_U.Ki_Module_1_U;
if (d_V_1 >= 0.2) {
d_V_1 = 0.2;
} else {
if (d_V_1 <= -0.2) {
d_V_1 = -0.2;
}
}
//////////////////////////////////////////////////
////////////Module 1 output voltage sharing part//////////
rtb_voltage_1 = ISIPOS_controlled_PI_U.Load_real_voltage/4- ISIPOS_controlled_PI_U.Module_1_
Voltage_2;
rtb_pi_1_2 = ISIPOS_controlled_PI_U.Kp_Module_1_V * rtb_voltage_1+
ISIPOS_controlled_PI_DWork.DiscreteTimeIntegrator_DSTATE *
ISIPOS_controlled_PI_U.Ki_Module_1_V;
```

```
if (rtb_pi_1_2 >= 0.2) {
rtb_pi_1_2 = 0.2;
} else {
if (rtb_pi_1_2 <= -0.2) {
rtb_pi_1_2 = -0.2;
}
}
////////////////////////////////////////////////
///////////Module 1 duty cycle//////////
ISIPOS_controlled_PI_Y.phaseshift_1 = d_V_1 + d_total + rtb_pi_1_2;
if (ISIPOS_controlled_PI_Y.phaseshift_1 >= 0.975) {
ISIPOS_controlled_PI_Y.phaseshift_1 = 0.975;
} else {
if (ISIPOS_controlled_PI_Y.phaseshift_1 <= 0.025) {
ISIPOS_controlled_PI_Y.phaseshift_1 = 0.025;
}
}
```

B.4 Fault Operation of ISIPOS Connected DC/DC Converter

The control algorithm code for Module 3 is given as an example.

```
////////////////////////////////////////////////
//////////Fault Detection ////////////////////
if (ISIPOS_controlled_PI_U.Load_real_voltage /4.5 <= ipos_module_PI_part_U.Module_4_Voltage
<= ISIPOS_controlled_PI_U.Load_real_voltage /3.5) {
//repeat the previous code for normal operation
} else {
////////////////////////////////////////////////
///////////Module 3 4 and 1 2 voltage sharing part//////////
rtb_voltage_3_1 = ISIPOS_controlled_PI_U.Module_1_Voltage_3 -
(ISIPOS_controlled_PI_U.Module_1_Voltage_1 +
ISIPOS_controlled_PI_U.Module_3_Voltage_1) * 0.5;
d_V_3 = ISIPOS_controlled_PI_U.Kp_Module_3_U * rtb_voltage_3_1
+ ISIPOS_controlled_PI_DWork.DiscreteTimeIntegrator_DSTATE_e *
ISIPOS_controlled_PI_U.Ki_Module_3_U;
if (d_V_3 >= 0.2) {
d_V_3 = 0.2;
} else {
if (d_V_3 <= -0.2) {
d_V_3 = -0.2;
}
}
////////////////////////////////////////////////
///////////Module 3 output voltage sharing part//////////
rtb_voltage_3 = ISIPOS_controlled_PI_U.Load_real_voltage/2- ISIPOS_controlled_PI_U.Module_3_
Voltage_2;
rtb_pi_3_4 = ISIPOS_controlled_PI_U.Kp_Module_3_V * rtb_voltage_3+
ISIPOS_controlled_PI_DWork.DiscreteTimeIntegrator_DSTATE *
ISIPOS_controlled_PI_U.Ki_Module_3_V;
if (rtb_pi_3_4 >= 0.2) {
rtb_pi_3_4 = 0.2;
} else {
if (rtb_pi_3_4 <= -0.2) {
rtb_pi_3_4 = -0.2;
}
}
////////////////////////////////////////////////
```

```
////////////Module 1 duty cycle//////////
ISIPOS_controlled_PI_Y.phaseshift_1 = d_V_3 + d_total + rtb_pi_3_4;
if (ISIPOS_controlled_PI_Y.phaseshift_1 >= 0.975) {
ISIPOS_controlled_PI_Y.phaseshift_1 = 0.975;
} else {
if (ISIPOS_controlled_PI_Y.phaseshift_1 <= 0.025) {
ISIPOS_controlled_PI_Y.phaseshift_1 = 0.025;
}
}
}
```

B.5 DAB Synchronous Rectification

```
//////////////////////////////////////////////////
////////////Open loop synchronous rectification for DAB module at 50 kHz//////////
void INTERRUPT (GPTA0_SRN22INT) GPTA0_viSRN22(void)
{
// USER CODE BEGIN (SRN22,2)
// USER CODE END
if(GPTA0_SRSS2_LTC01)       //  LTC1 event (= compare with last timer)
{
GPTA0_SRSC2 = 0x00000002; //  reset LTC1 service request bit
// USER CODE BEGIN (SRN22,4)
x=42;
GPTA0_LTCXR10=5;
GPTA0_LTCXR11=98;
GPTA0_LTCXR12=197;
GPTA0_LTCXR13=98+5;
GPTA0_LTCXR14=5+x;
GPTA0_LTCXR15=95+x;
GPTA0_LTCXR16=x;
GPTA0_LTCXR17=98+5+x;
GPTA0_LTCXR18=5;
GPTA0_LTCXR19=x;
GPTA0_LTCXR20=98+x;
GPTA0_LTCXR21=98+5;
GPTA0_LTCXR22=98+5;
GPTA0_LTCXR23=98+x;
GPTA0_LTCXR24=x;
GPTA0_LTCXR25=5;
// USER CODE END
}
// USER CODE BEGIN (SRN22,8)
// USER CODE END
```

Appendix C

Lists of figures and tables in the thesis:

C.1 Lists of Figures

C.2 Lists of Tables

Appendix D

Author's publications

1. Yiqing Lian, Grain Adam, Derrick Holliday, Stephen Finney, 'Modular Input-parallel-output-series DC/DC Converter Control with Fault Detection and Redundancy', IET Generation, Transmission & Distribution Journal, Volume 10, Issue 6, 21 April 2016, p.1361–1369, doi: 10.1049/iet-gtd.2015.0789.

Abstract:

Large offshore wind farms require extensive sub-sea cables within the collection network. Present solutions are based around medium-voltage AC collection networks.

Recent studies have highlighted the potential benefits of DC collection networks. However, achieving DC/DC conversion at the required voltage and power levels presents a significant challenge for wind-turbine power electronics. This paper proposes an alternative DC collection network based around a modular DC/DC converter with input-parallel output-series (IPOS) connection. This modular topology can overcome the limitations imposed by semiconductor voltage ratings and provides fault-tolerant operation. Small-signal analysis of the converter is presented to be used to facilitate controller design for the converter input and output stages. A new master-slave control scheme and distributed voltage sharing controllers are proposed that ensure power sharing under all operating conditions, including during failure of a master module. This control scheme achieves fault-tolerant operation by allowing the status of master module to be reallocated to any healthy module. The proposed control scheme is validated using simulation and experimentation, considering active power sharing between modules with parameter mismatch.

2. Yiqing Lian, Grain Adam, Derrick Holliday, Stephen Finney, 'Medium-Voltage DC/DC Converter for Offshore Wind Collection Grid', IET Renewable Power Generation Journal, Volume 10, Issue 5, May 2016, p.651–660, doi: 10.1049/iet-rpg.2015.0376.

Abstract:

A novel modular DC/DC converter with input-series-input-parallel output-series connection to realise a DC collection power network for large-scale wind farms is presented. The proposed topology uses interconnection of multiple modular cells with low rated voltage and power to enable operation with high voltage at the input and output. Low rated power of individual modules in the proposed DC/DC converter permits the use of a high-frequency ac link, resulting in a significant reduction in transformer size and weight, which makes deployment of DC collection networks in offshore wind farm applications more feasible and effective. In addition, a robust control scheme is developed to ensure power sharing between practical modules with parameter mismatch and during transient conditions. Small- and large-signal analyses are performed in order to deduce the control structure for the converter input and output stages. Simulation and experimental results demonstrate

and validate the proposed converter and associated control scheme.

3. Yiqing Lian, Derrick Holliday, Stephen Finney, 'Dual-Active Bridge Converter with Input-Series-Input-Parallel Output-Series Connection', in 8th IET International Conference on Power Electronics, Machines and Drives, 2016, accepted for publication.

Abstract:

The high-power bidirectional DC/DC converter is perceived as one of the key enabling components of DC energy transfer and storage systems, and needs to be designed for high reliability and efficiency. This paper proposes a new high-power input-series-input-parallel output-series (ISIPOS) connected modular DC/DC converter, where the dual-active bridge (DAB) DC/DC converter is employed as the basic module on the primary and secondary sides, with a control strategy that enables power sharing between the modules under any steady-state and transient conditions with mismatched components. In addition, fault tolerant operation is presented. The viability and effectiveness of the proposed control method are demonstrated using MATLAB simulation of power sharing performance and fault tolerant operation.

4. Yiqing Lian, Grain Adam, Derrick Holliday, Stephen Finney, 'Modular Input-Series-Input-Parallel Output-Series DC/DC Converter Control with Fault Detection and Redundancy', in IEEE Energy Conversion Congress and Exposition (ECCE) Conference, Montreal, QC, 2015, pp. 3495-3501.

Abstract:

A novel high-power modular input-series-input-parallel output-series connected DC/DC converter for medium voltage application is proposed. Emphasis has been placed on power sharing control to compensate parameter mismatches and achieve equal power distribution between modules. Converter control is extended to achieve fault-tolerant operation by exploiting modularity to provide redundancy in the event of any failure. The proposed control scheme is validated through application-level simulations and scaled down experiments to testify the reliability of the proposed control for ensuring power sharing between modules under a range of operating conditions. The results validate the proposed converter and associated control scheme indicating this to be a promising topology for high-power medium-voltage

applications.

5. Yiqing Lian, Grain Adam, Derrick Holliday, Stephen Finney, 'Active Power Sharing in Input-Series-Input-Parallel Output-Series Connected DC/DC Converters', in IEEE Applied Power Electronics Conference and Exposition (APEC) Conference, Charlotte, NC, 2015, pp. 2790-2797.

Abstract:

A high-capacity DC/DC converter with novel input-series-input-parallel output-series connection and with autonomous power sharing between modules is proposed. The proposed scheme is well suited for large-scale wind farm DC collection networks, as it avoids the charging current issues associated with its AC counterpart, and offers lower losses and reduced size and weight when a medium- or high-frequency transformer is used. Small-signal analysis is used to derive the control structures for the converter input and output stages. The proposed control scheme is validated through simulation and experimentation, including demonstration of autonomous power sharing between modules under several operating conditions.

6. Yiqing Lian, Derrick Holliday, Stephen Finney, 'Modular Input-parallel-output-series DC/DC Converter Control with Fault Detection and Redundancy', in 11th IET International Conference on AC and DC Power Transmission, Birmingham 2015, pp. 1-8.

Abstract:

Large offshore wind farms will require an extensive sub-sea power network to provide internal interconnection. Present solutions are based around conventional medium-voltage AC architectures. This paper proposes an alternative DC collection network based around modular DC/DC converters with input-parallel-output-series (IPOS) connection. Small-signal analysis of the converter is presented, to assist in control scheme development for the converter input and output stages. A Lyapunov controller is embedded within the conventional output voltage sharing control loop. A master-slave control scheme is proposed to ensure power sharing under a range of operating conditions, and provides fault-tolerant operation since the status of 'master' can be reallocated in the event that the present 'master' module fails.

7. Yiqing Lian, Stephen Finney, 'DC Collection Networks for Offshore Generation', in 2nd IET Renewable Power Generation Conference (RPG 2013), Beijing, 2013, pp. 1-4.

Abstract:

Onshore wind farms can now be regarded as a mature technology, capable of providing increasing levels of clean energy. The development of offshore wind technology will provide the ability to harness much larger wind energy resource. Offshore wind arrays present many new challenges including the electrical power system which provides the internal collection system and the connection to the on-shore power network. For remote offshore wind farms, high voltage direct current (HVDC) transmission will be required to transmit power from the wind farm to the shore. The use of HVDC has the effect of decoupling the wind farms internal collection network from the rest of the power grid, thereby removing the requirement for a conventional alternating current (AC) network. This paper discusses the use of a direct current (DC) collection system for offshore wind farms, with particulars emphasis of DC-DC converter requirements. The proposed converter is validated by the simulation model and the performances e.g. switching losses, conduction losses are investigated.

8. Yiqing Lian, Andrew Kenyon, David Pattison, Christos Tachtazis, Maria Segovia-Garcia, Alison Cleary, Francis Quail, 'Wind Turbine Gearbox Ice Sensing and Condition Monitoring for Fault Prognosis and Diagnosis', in International Congress of Condition Monitoring and Diagnostic Engineering Management (COMADEM), 2013.

Abstract:

The gearbox is seen as one of the most important assets of a wind turbine, so a major concern is how to keep it running smoothly to maximise its service time and reduce the cost. However, wind turbines are often located at remote locations where icing is possible and likely, e.g. high altitudes or cold regions. This challenges the wind turbine stability and causes a variety of problems. Furthermore, rapid expansion of wind energy, along with high operation and maintenance costs, all lead to the need for a condition monitoring system which can offer diagnostics of present condition and prognostics of future condition to improve the reliability of wind turbine and

reduce the cost of unscheduled maintenances and unexpected failures. The proposed approach is demonstrated by using a Bayesian Belief Network and Dynamic Bayesian Network under Labview and GeNIe respectively. The proposed procedure is applied on a wind turbine gearbox model to show its feasibility.

9. Yiqing Lian, Adam Stock, Bill Leithead, 'Investigating the Effectiveness of Implementation of Power Adjusting Controller on 2 MW Wind Turbine', in 8th PhD Seminar on Wind Energy in Europe, 2012.

Abstract:

The UK government has set a target 20 % of electricity generation from renewable sources by 2020. Among various renewable technologies, the environmental benefits and cost-competitiveness have driven the rapid expansion of wind power as a significant green source in recent decades. However, there are certain characteristics of the wind energy challenge today's power system operation. For example, the system inertia is linked to the synchronous generation to power system, due to different electromechanical characteristics; this inherent link is not present in wind turbine generation. In this study, a controller for 2 MW wind turbine which gives more flexible operation is used to generate boosted power to provide synthetic inertia and to limit the impact on frequency control of the power system. This paper basically focuses on the study and implementation of the power adjusting controller on 2 MW wind turbine model to analyse the effectiveness. A Simulink model is developed in Matlab including the features of wind turbine, wind and controller.