PARTIAL DISCHARGE BEHAVIOUR UNDER AC AND DC CONDITIONS INCLUDING NOVEL MANUFACTURE TECHNIQUES FOR VOID-TYPE DIELECTRIC SAMPLES

A thesis presented in fulfilment of the requirement for the degree of

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AUTHORS DECLARATION

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ABSTRACT

The move from centralised electricity generation, near centres of demand, to distributed generation has brought justification for the use of high voltage direct current (HVDC) transmission techniques. One key application is the transmission of power from offshore wind farms, there is a breakeven distance where conventional high voltage alternating current (HVAC) transmission is less cost effective than HVDC transmission. The condition monitoring of HVDC transmission networks will be paramount to minimise any unnecessary system downtime. The primary method to monitor the condition of an insulation system is the measurement of partial discharge (PD). This thesis develops the understanding around sensor installation, sample behaviour under DC conditions and novel manufacture methods for void type dielectric samples.

The first area of interest to this thesis was the development of a method to assess the effect of the electromagnetic field emissions from HVDC converter station on the behaviour of high frequency current transformers (HFCT). A range of sensors of different constructions were tested in a controlled electromagnetic field environment. The relative immunity of the sensors to the incident field was derived using the method.

The second phase of this work investigated the behaviour of a range of dielectric samples under AC and DC conditions. Existing analysis techniques were explored based on recommendations in IEC 60270 and literature to date. The behaviour of a void type sample was explored further through the variation of test history such as; grounding period, DC polarity and AC/DC variation.

The final section of research focused on the development of novel manufacturing techniques and the behaviour of void type samples under AC and DC conditions. The proposed techniques made use of two very different manufacturing approaches; 3D printing and subsurface laser etching (SSLE). In this study, 3D printing was found to be more successful in enabling void type PD behaviour. Initial explorations were made of AC/DC PD behaviour of multiple void samples and thermally aged samples.

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LIST OF ABBREVIATIONS

ABS	Acrylonitrile Butadiene Styrene
AC	Alternating Current
BNC	Bayonet Neill–Concelman
BTL	Bell Telephone Laboratories
CCD	Charge Coupled Device
DC	Direct Current
DPSS	Diode Pumped Solid State
DRT	Desired Room Temperature
DSC	Differential Scanning Calorimetry
EAP	Equalised Aging Process
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EUT	Equipment Under Test
FDM	Fused Deposition Modelling
FEA	Finite Element Analysis
FFT	Fast Fourier Transform
FTIR	Fourier-Transform Infrared Spectroscopy
GTEM	Gigahertz Transverse Electromagnetic
HFCT	High Frequency Current Transformer
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
LCC	Line Commutated Converter
LDPE	Low Density PolyEthylene
LED	Light Emitting Diode
LFAC	Low Frequency Alternating Current
MI	Mass Impregnated
MMC	Modular Multilevel Converter

NPL	National Physical Laboratory
PC	Personal Computer
PD	Partial Discharge
PDIV	Partial Discharge Inception Voltage
PET	Polyethylene Terephthalate
PLA	PolyLactic Acid
PRPD	Phase Resolved Partial Discharge
PSA	Pulse Sequence Analysis
RF	Radio Frequency
RMS	Root Mean Squared
SEM	Scanning Electron Microscope
SLA	Stereolithography
SLM	Spatial Light Modulation
SLS	Selective Laser Sintering
SSLE	Subsurface Laser Etching
STL	Standard Triangle Language
TEM	Transmission Electron Microscopy
TEV	Transient Earth Voltage
TF	Time Frequency
UV	Ultra Violet
VSC	Voltage Source Converter
XLPE	Cross-Linked Polyethylene

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1. INTRODUCTION

The motivation for this research is based around the increased interest in power systems incorporating high voltage direct current (HVDC) transmission links. The reactive power losses of high voltage alternating current (HVAC) transmission are seen as a barrier in subsea/underground applications in particular. The breakeven distance is the distance at which the cost of an AC transmission system matches that of a DC transmission system (consists of the terminal costs and the cable/line costs). Currently the breakeven distance for subsea/underground cables is 50-100 km and 600 km for overhead lines [1]. The move to HVDC transmission for overhead lines is seen as less of a priority in the UK but more of a priority in developing nations such as China, India and Brazil where overhead line transmission distances is in excess of 600 km. Range extending techniques are receiving increased interest for HVAC transmission such as low frequency AC transmission (LFAC) and in-line reactive power compensation with operators reluctant to adopt DC transmission. As such this research is more focused on the UK scenario and cable systems as opposed to overhead lines. Applications of HVDC transmission relevant in the UK are:

- Links to mainland Europe, Ireland and Scandinavia for power trading activities
- Connection of distributed generation sources in isolated locations of the UK
- Interconnection of the UK power network to alleviate bottle necks where AC power system is running at capacity

Additionally, 2020 government and European Union targets are in place for the electricity heat and transport sectors. In the electricity sector the government has committed to 20% of energy from renewable sources by 2020. The most developed renewable energy generation technique to deploy in the UK is wind power and due to increasing issues with the cumulative impact of onshore wind the most promising area for development is that of offshore wind. A particular application of interest for HVDC transmission links is the connection of remote offshore wind farms due to the transmission distances involved. Figure 1 details the average water depth and distance to shore for online, under construction and consented wind farms in January 2017 for Europe.

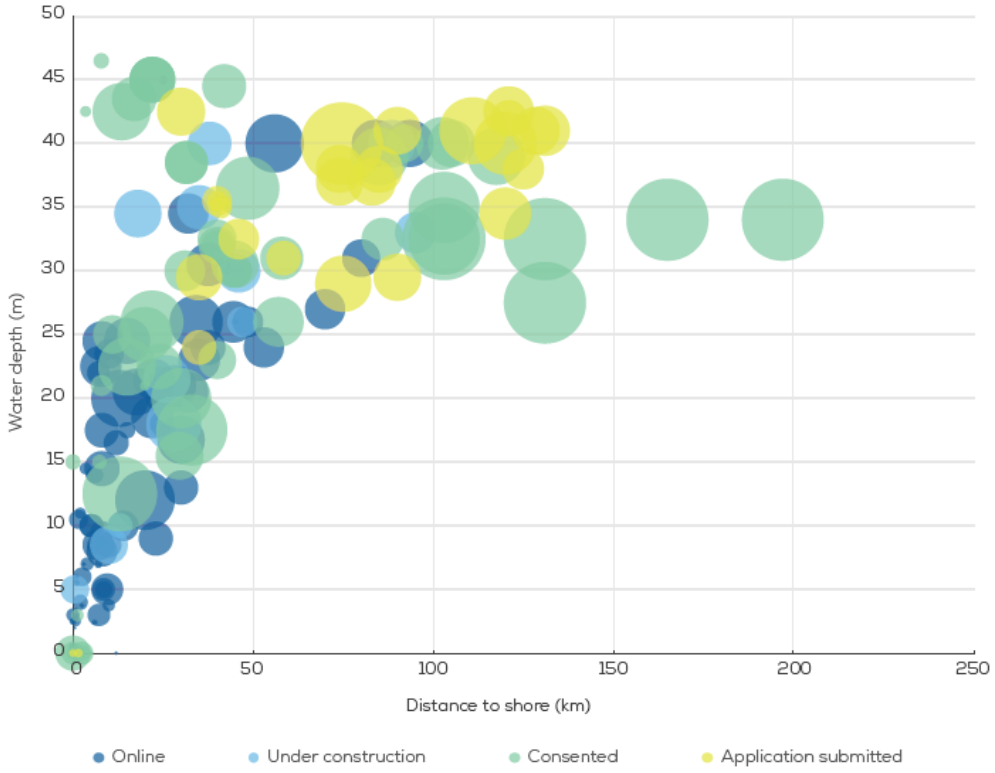


Figure 1 - Average water depth and distance to shore of online, under construction and consented wind farms in 2016 (Dot size indicates relative capacity of the wind farm) [2].

This data indicates that wind farms are moving into deeper water which is further from shore and a significant number of the consented and under construction wind farms are around the breakeven distance of 50-100 km. The topic of particular interest to this research is the condition monitoring of the HVDC transmission link. The HVDC transmission link is a critical connection between the offshore wind farm and the UK grid; any loss of the link would bring significant costs in repairs and lost revenue from power transfer activities. The application of condition monitoring would aim to minimise system outages whereby faults can be tracked to reduce the system downtime and enable scheduling of repairs to be implemented. One condition monitoring technique which is generally implemented on critical AC transmission links is the monitoring of partial discharge (PD).

PD detection under AC conditions is a well-established tool applied to AC systems for insulation monitoring. Under AC conditions a number of different PD detection techniques are available dependent on the application of interest. However, even

under AC conditions, PD remains a complex phenomenon with many measurement and diagnostic challenges remaining. In comparison, PD detection under DC conditions has received less interest with most power systems being solely AC networks to date.

A PD is a small breakdown which does not completely bridge the gap between the conductor and ground, within the IEC 60270 standard [3] a PD event is defined as:

> *"localized electrical discharge that only partially bridges the insulation between conductors and which can or can not occur adjacent to a conductor"*

Essentially electrical discharge activity centres on the ionisation of materials to produce charge carriers [4]. Electrical impact ionisation is the primary ionisation mechanism in electrical discharges. The free electrons can impact on the outer electrons of atoms and molecules, if the free electrons have enough energy they can knock the outer electron out of its orbit. This process leads to a positive ion and a further free electron. An externally applied field determines the energy of the free electrons, in this case the externally applied field is generally the electric field. Electric field driven discharges can also be produced by AC electric fields (generally extinguish and reignite every time the electric field reverses polarity) [5].

A PD event is produced when there is a defect in the insulation of an electrical system. PD generally occurs when a manufacturing defect is present or degradation occurs over time in the insulation of an electrical system. The most common defect evident in cable systems is that of gas filled voids in the form of air bubbles or at interfaces between different insulation systems/cable accessories.

The presence of a PD producing defect can accelerate the aging of the insulation in the cable system. Initially the defect will produce PD events of a small magnitude and at a low frequency of occurrence. Gradually, as the insulation degrades further through this initial PD activity, the charge magnitude in the PD events will also increase and the frequency of occurrence will increase. The trending of PD data over a long time period or regular time intervals will enable the observable changes in the insulation system to be quantified. If allowed to degrade to dangerous levels electrical trees can form and eventually breakdown of the insulation system can occur. The failure of the insulation system has both safety and financial implications for the system operator. The early detection of such faults would have significant benefits to the system operator.

The two main cable types currently used in subsea and underground applications are Mass Impregnated (MI) and extruded Polymeric Insulation [6]. MI is the most established cable technology; cables with this type of insulation have been in service for many years with good reliability and performance. An illustration of a MI cable is shown in Figure 2.

Figure 2 - Nexans mass impregnated cable [7]**.**

The operational temperature for MI is 55°C, the central conductor is often copper but may be aluminium for reasons of cost. The insulation consists of layers of high density oil impregnated paper. The insulation is coated in extruded lead to add protection and prevent water ingress. The metallic armouring is coated in a plastic based layer as the final barrier to the external environment. This type of cable is suitable for both the voltage source converter (VSC) and line commutated converter (LCC) topologies [8].

The less mature technology is the extruded polymeric cable with the most popular extruded insulation being cross linked polyethylene (XLPE). An example of an XLPE cable is illustrated in Figure 3.

Figure 3 - ABB 525 kV XLPE submarine cable [9]**.**

The cable consists of the copper or aluminium central conductor with a polyethylene insulator extruded over the conductor. The extrusion process is automated to ensure the consistency of the cable insulation is to a defined standard. There is further shielding incorporated beneath the extruded lead sheath, metallic armouring and final waterproof plastic coating. The XLPE cable can operate at a higher temperature (70°C) than MI cables, this allows a larger flow of current through the conductor. XLPE cables have been employed for both current and voltage source converter topologies [8], [10], [11].

The current trend for cables is moving towards XLPE insulation but some high profile projects employ MI due to the known and trusted cable design [12]. There is increasing interest into the use of insulation material which is easier to recycle than XLPE. The cable itself is a massive part of the infrastructure expenditure in a HVDC system. The cables can only be manufactured in certain lengths (through manufacturing or transport/logistical restrictions) either factory or field joints are required to meet the cable length requirements. Defects can occur during manufacture or during the jointing of cable lengths in the form of gas filled voids, contaminants or mechanical damage [13]–[16].

The application of HVDC systems as a tool to transport power from remote generation sources or when overhead lines cannot be employed emphasises the importance of investigating PD behaviour of representative defects under DC conditions. The main defect of interest in this thesis is the behaviour of gas filled voids under AC, DC conditions and possible novel methods of manufacturing dielectric samples.

1.1. MOTIVATION

Partial discharge for AC voltage is phase dependant and different characteristics can be deduced for different defects that produce partial discharge. Under DC conditions there is no recognised standard approach, the main parameters that are available to use are the discharge magnitude and the time of occurrence of the partial discharge. The AC and DC partial discharge traces are illustrated in Figure 4.

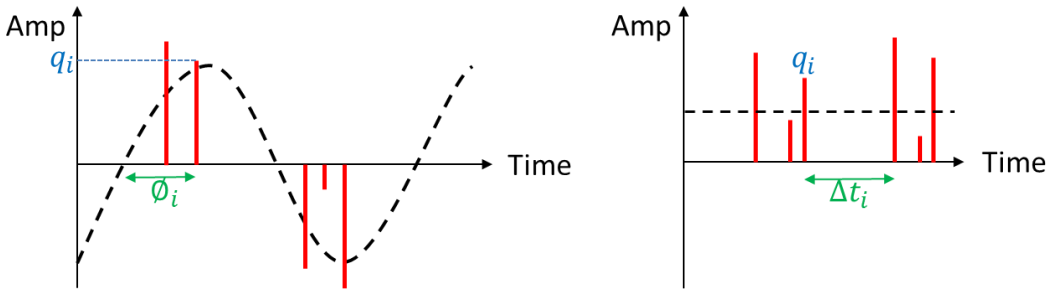


Figure 4 - Partial discharge for AC (left) and DC (right) voltages

No large change is required to the test set-up used in AC studies in order to conduct PD tests under DC conditions. This enables existing infrastructure used for AC PD detection to be used for PD measurements under DC conditions.

The fundamental early work in the field of Partial Discharge in HVDC systems was conducted at Delft Institute of Technology a summary of the work is discussed by Morshuis *et al*. [17]. This paper discusses the key details of three PhDs conducted in this field:

- The first thesis referenced is the work of Fromm who investigated the physics of partial discharges for DC voltage and the partial discharge events were characterised by the time of occurrence and the magnitude of the PD [18].
- The second thesis was by Beyer who used PD analysis on HVDC equipment and classification methods were discussed for PD at DC voltage [19].
- The final thesis referenced was that of Jeroense, mass impregnated cables were investigated for PD and associated test methods were developed [20].

More recent publications investigating the behaviour of PD under DC conditions have been from the University of Bologna [21]–[24] and researchers around the world [25]–[27].

To date, limited work has been carried out on the immunity testing of HFCTs to understand how the sensors respond when installed in a converter station environment. The converter station will have electromagnetic field effects from the converters themselves this study presents a method for testing the immunity of HFCTs when exposed to a controlled electromagnetic field. The behaviour of a void type dielectric sample under DC and varied DC conditions has been an area of interest for some time [28]–[30]. However, limited work has been conducted to

understand the effect of the immediate test history on void type samples. As a result, areas of interest to this work include; the grounding period required to discharge a void type sample, the behaviour of a void type sample under repeated DC PD testing and polarity reversals has received limited attention. HVDC cables are exposed to cycles of tests during prequalification and type testing, the linking of how the various cycles could affect each other is a key area of interest.

The manufacturing process for creating gas filled voids in dielectric has received significant attention to date [31]–[34]. The two methods currently employed to create cavities in dielectric samples are; the injection of air bubbles in epoxy resin discs and the stacking films/sheets to create cylindrical voids. In this work two novel methods are presented to enable void type defects, of a defined geometry, to be introduced inside the dielectric sample. The first method employs 3D printing building on findings from a previous study [35] and the second investigates sub surface laser etching (SSLE). Generally, both methods allow greater control of the void and sample geometry. The most successful method identified in this study was 3D printing and this method was subsequently used to investigate the behaviour of single cylindrical and spherical voids under AC and DC conditions. Indeed, the controllability of the 3D print method allowed the exploration of different defect geometries and the inclusion of multiple defects with defined separation distances. Furthermore, the inclusion of multiple serial and parallel voids in dielectric samples was explored using 3D printing, samples were tested under AC and DC conditions.

Additionally, the thermal aging of dielectric samples manufactured using 3D printing was investigated to determine the temperature effect on PD behaviour. The aim was to accelerate aging under elevated temperatures, the PD behaviour of thermally aged samples was tested under both AC and DC conditions.

1.2. CONTRIBUTIONS

The main objectives of this thesis are:

- Enhance the understanding of HFCT behaviour in an electromagnetic field environment
- Aid understanding of void type PD behaviour under AC and DC conditions
- Investigate the effect that the immediate test history of a dielectric sample has on DC PD behaviour

- Explore alternative methods for the creation of internal voids in dielectric samples
- Apply challenging use cases to the most promising manufacturing method
- Survey the possible approaches to enable the accelerated aging of dielectric samples produced using the most promising approach

The contributions from this thesis are subsequently outlined in chapters 2 to 8; the summary of the contributions are as follows:

- PD measurement sensors will be exposed to significant electromagnetic fields in the actual real life application environment (HVDC converter station). The evaluation of HFCT behaviour when exposed to a controlled electromagnetic field is explored in chapter 2.
    - A method is presented to enable HFCTs to be exposed to a controlled electromagnetic field, using the existing infrastructure of the GTEM cell in the high voltage lab.
    - HFCTs of different construction were exposed to the electromagnetic field and the relative sensitivity of the HFCTs to the electromagnetic field was recorded for different orientations.
    - The HFCTs with aluminium enclosures were less susceptible to electromagnetic field effects than the casings made from HDPE findings which could allow refinement of sensor design or shielding approaches.
- The behaviour of three generic samples under AC and DC conditions is explored in chapter 3.
    - A method for AC PD testing is presented to confirm the PD behaviour from the three samples was as expected.
    - A method for DC PD testing is presented utilising the ramp test method.
    - The analysis of the resulting PD activity was of specific interest with suggested approaches from standards and publications investigated. These analysis methods are employed later in this thesis based on the findings in this chapter.
- The effect of test history on PD behaviour under DC conditions for an aged void type sample is examined in chapter 4. The variation of test conditions

was of particular interest in prequalification/type testing of cable systems and to understand the effect of test history on DC PD behaviour.

  - The grounding period between subsequent DC ramp tests on a void type sample is investigated and observable changes in PD behaviour were reported for different grounding periods prior to positive DC ramp tests.
  - The application of repeated positive DC ramp tests on internal void PD behaviour is investigated. The main observable effect was the reduction of larger PD events over the initial hold at $9V_R/5$ when the insulation was capacitively graded. The cumulative PD activity was shown to systematically reduce in subsequent ramp tests.
  - The variation of polarity for subsequent DC ramp tests on a void type sample was investigated. The main variation apparent was over the first few minutes at $9V_R/5$, where PD magnitude and repetition rate were affected.
  - The inclusion of an AC PD test between DC PD testing is used to investigate the behaviour of void type sample and the results are presented. AC PD testing could take place during prequalification or type testing if the cable system design allows AC energisation. The AC PD test and the second DC ramp test varied from the initial tests conducted on the sample, clearly showing that the test history had an impact.

- A novel method of using a 3D printer to manufacture defined void type defects using ABS plastic is identified and carried out in chapter 5.
  - The method outlines the 3D modelling, manufacture process and final sample preparation prior to electrical testing.
  - The AC PD behaviour of dielectric samples with no defects, spherical voids and cylindrical voids are presented. Panchen's law was used to predict the AC inception voltage for the induced defects. The inception voltages were close to the predictions from Panchen's law and φ-q-n plots were used to analyse the resulting PD behaviour.
  - The DC PD behaviour was presented for virgin samples with no defects and cylindrical voids. During prolonged DC PD testing limited

PD activity was observed in the samples up to two times the peak value of the AC inception voltage.

- The method proposed in chapter 5 was further employed to investigate the inclusion of multiple defects in dielectric samples in chapter 6 together with the AC/DC PD behaviour of the samples.
    - The number of cylindrical voids in a dielectric sample was varied through the design of samples in a 3D modelling package with a controlled void geometry.
    - Parallel voids were investigated, one specific challenge highlighted during the manufacturing process was the alignment of the two halves of the sample. Serial voids were formed by stacking single void samples.
    - Samples were tested under AC conditions and φ-q-n plots were used to compare PD activity of the samples with varied geometry. Variations in the inception voltage of sustained PD were evident for the different geometries.
    - The samples were tested under DC conditions using the ramp test method. Generally, as more parallel voids were included the PD magnitude and number of PD events increased. Limited PD activity was observed for the serial arrangement but the PD magnitude was generally smaller than that of a single void in the same insulation thickness.
- Potential accelerated aging processes for 3D printed dielectric samples were considered and investigated in chapter 7.
    - A method was presented to enable the thermal aging of dielectric samples, with single cylindrical voids.
    - The thermal aging of thermoplastic samples posed significant challenges with the warping of samples and changes in geometry. The acceptable temperature range for the thermal aging of ABS 3D printed samples was determined.
    - AC PD tests were used to confirm that a void type defect still existed in the sample under test and to determine the peak value of the AC inception voltage.

- In the samples which were aged below 99.4 °C observable changes in PD behaviour were apparent during the DC PD ramp tests. In the samples aged above 99.4 °C the changes in geometry had a larger effect than the thermal degradation of the dielectric material.

- The use of subsurface laser etching to create defined voids in films is examined in chapter 8.
  - Samples were manufactured with defects introduced through the thickness of polypropylene films. A wide range of defect types from single voids to arrays of voids. Panchen's law was used to predict inception voltages.
  - AC PD testing was conducted on the range of samples to determine if internal PD was evident from the samples. The threshold for maximum voltage was set through testing films with no defects. No internal PD was detected in samples.
  - Samples were dissected and SEM imaging was used to determine whether voids exist inside the films. The images of the cross sectional view confirmed that the intended defect was an area of damaged material and not a single void.
- Finally chapter 9 outlines the key results, conclusions and future work is considered.

For additional information the journal and conference papers from work in this thesis are outlined in the following subsections.

1.2.1. JOURNAL

The journal paper to date produced during the completion of this thesis are listed below.

[1] E. Corr, A. Reid , X. Hu, W.H. Siew, M. Zhu, M. Judd, M. Seltzer-Grant and R. Giussani, "Partial Discharge Testing of Defects in Dielectric Insulation Under DC and Voltage Ripple Conditions", CIGRE Science & Engineering, June 2018.

1.2.2. CONFERENCE

The work in this thesis was presented at 7 national and international conferences. The conference papers generated by this thesis are outlined below.

[1] M. Seltzer-Grant, W. H. Siew, E. Corr, X. Hu, M. Zhu, M. Judd, A. Reid, A. Neumann, "Laboratory and Field Partial Discharge Measurement in HVDC

Power Cables", Proc. 9th International Conference on Insulated Power Cables (Jicable), June 2015.

[2] M. Judd, W. H. Siew, X. Hu, E. Corr, M. Zhu, A. Reid, O. El-Mountassir, M. Urizarbarrena Cristobal, R. Giussani and M. Seltzer-Grant, "Partial Discharges under HVDC Conditions", Euro TechCon, December 2015.

[3] A. Reid, M. Seltzer-Grant, R. Giussani, W. H. Siew, E. Corr, M. Zhu, X. Hu, M. Judd and O. El-Mountassir, "Investigating the Effects of VSC Harmonic Content on PD Characteristics in HVDC Insulation Systems", EPRI HVDC & FACTS Conference, August 2015.

[4] E. Corr, W.H. Siew, "Analyses of partial discharges in dielectric samples under DC excitation", Universities Power Engineering Conference (UPEC), September 2015.

[5] E. Corr, W.H. Siew, "Condition monitoring of HVDC transmission systems for offshore wind", EAWE 12th PhD seminar on Wind Energy in Europe, May 2016.

[6] E. Corr, W. H. Siew, W. Zhao, "Long Term Testing and Analysis of Dielectric Samples Under DC Excitation", IEEE Electrical Insulation Conference (EIC), June 2016.

[7] E. Corr, W. H. Siew, W. Zhao "PD activity in void type dielectric samples for varied DC polarity", IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP), October 2016.

1.3. THESIS OUTLINE

The thesis contents and associated contributions will be outlined in this section. In chapter 1, the PhD research is introduced along with the background information and motivation for the research. The Contributions to the field are highlighted and the thesis contents are outlined.

Chapter 2 details a method to the characterisation of HFCTs to confirm the manufacturers stamped values. A method is presented to determine the scaling factor (pC/mV) of the detection methods used in the AC and DC test circuits using a void type sample, a calibrator unit and an oscilloscope. The final method presented in this chapter was the immunity testing of HFCTs in a controlled electromagnetic field, this was in order to simulate the electromagnetic field emission in a converter station. The controlled electromagnetic field was generated in the GTEM cell in the

Strathclyde HV lab. The effect of varying the orientation of the sensors and sensors of different construction were discussed.

Chapter 3 details the AC and DC testing of generic samples namely void type (inherited sample), surface and a sample with a metallic protrusion. A test method is presented for AC PD testing, with the voltage incrementally increased until repetitive and sustained PD was observed from each test sample. The aim was to determine the peak value of the AC inception voltage (V_R) and to confirm the dominant source of PD from each sample. A method for DC PD testing uses the peak value of the AC inception voltage to determine the hold voltages ($V_R/2$, V_R and $3V_R/2$) in a ramp and hold technique. The three DC PD data sets were analysed using:

- Revisions to IEC 60270 for the analysis of DC PD activity. The PD activity could be differentiated based on the behaviour observed.
- Recommended methods were also applied to the data sets.
- Analysis was conducted on the measured quantities of charge magnitude and time of occurrence. Focus was placed on the statistical variation and sequence of PD events.

Chapter 4 details testing conducted on a void type dielectric sample under varied voltage conditions. The primary aim was to investigate the effect of the immediate test history on the DC PD behaviour of the sample. The second was to understand how a void type defect will respond under the tests conducted during prequalification/type testing of HVDC cable systems [36]. A number of studies were performed:

- An investigation into the grounding period between subsequent DC PD tests from 32 days to 3 days.
- The repeated application of DC ramp tests one after the other with lower levels of PD observed over the initial hold at $3V_R/2$ PD as DC tests were repeated.
- The inclusion of an AC test between two DC ramp tests was also investigated with the PD behaviour over the initial hold period varying.

The main variation evident in all tests was while the insulation was capacitively graded (following a voltage change) where the PD magnitude and repetition rate were most affected.

In chapter 5 a novel method was developed to enable the creation of defined void type defects using 3D printing. The design, manufacture and final assembly of dielectric samples with voids prior to electrical testing is outlined. The limitations of the technique were explored and a method was devised to remove the requirement for overhangs in the 3D model. Samples with no defects, cylindrical and spherical voids were manufactured using a commercially available 3D printer. The samples were initially tested under AC conditions to confirm the dominant source of PD was from the induced void. Virgin samples were tested under DC conditions and limited PD activity was observed during extended DC PD tests (hold periods of in excess of 2 hours).

In Chapter 6 a method is presented detailing the design and manufacture of 3D printed dielectric samples with multiple voids. The chapter acts an exploratory study of the 3D printing technique and the possible opportunities presented by the approach. Samples with parallel and serial voids were manufactured. Virgin samples were tested under AC conditions and compared to known behaviour in available literature. Virgin samples were also tested under DC conditions a limited number of PD events were detected in each case. The resulting PD events was analysed and compared to single void samples in each case.

In chapter 7 investigations are conducted around the accelerated aging of 3D printed dielectric samples. A method was developed to enable the thermal aging of dielectric samples manufactured using a 3D printer. A challenge encountered was the changes in geometry evident when samples where heated above 100 °C. Aging methods enable the relative age of the samples at elevated temperatures to be equated to the age at ambient temperature. The aged samples were tested under AC conditions first to confirm the insulation was still intact and the PD behaviour was still void like. The samples were also tested under DC conditions using the ramp test method. The changes in geometry apparent above 100 °C had a larger effect than the thermal aging of the dielectric material. At temperatures below 100 °C observable changes in PD behaviour under AC and DC conditions were apparent.

In chapter 8 a novel method is presented to create internal voids in film samples using subsurface laser etching (SSLE). SSLE is commonly used to create very controlled optical changes inside scintillator crystals. This chapter investigates the possibility of using SSLE to manufacture defined defects in film samples. A partner university provided the access to a bespoke SSLE machine and the time of a trained

technician to operate the system. A wide range of defects from a 5 μm square defect all the way up to a 100x100 μm and 40 μm defect were introduced in 125 μm and 190 μm polypropylene film samples. The control of defect size was possible by varying key parameters of the laser in the SSLE machine. The main question posed of this method was whether the laser burns optically changed material or whether a void type defect was introduced. No consistent internal void type PD behaviour was detected under AC conditions. SEM images of the cross section of the voids confirmed that the anticipated void was not present inside the film sample. Instead an area of damaged material was evident.

Chapter 9, the final chapter, outlines the key results and conclusions from the experimental work detailed in the thesis. Future work relating to the research in the thesis was also discussed.

2. CALIBRATION OF SENSORS AND MEASURMENT TECHNIQUES

This chapter details the testing conducted on high frequency current transformers (HFCT) for deployment in a high voltage direct current (HVDC) systems. An existing method was employed to characterise an unknown sensor or to confirm the transfer impedance stamped on the HFCT by the manufacturer. A method to determine the scaling factor of the most sensitive HFCT was developed for the AC and DC test circuits. A further method is introduced to assess the immunity of the respective sensors to controlled electromagnetic fields.

HFCT's are likely to remain important technologies for HVDC monitoring applications. The deployment of the sensors in a HVDC substation environment will expose the sensors to significant electromagnetic interference (EMI). An evaluation of several different PD sensors has been carried out to determine the effect of EMI on the sensors. The following sections will discuss HFCT characterisation, the scaling factor of PD pulses and PD sensor interference testing.

2.1. ASSOCIATED LITERATURE

A range of literature sources have been consulted for the content in this chapter. The characterisation of HFCTs, calibration of electric field sensors and the electromagnetic field emission in converter stations will be investigated.

The characterisation of HFCTs is generally conducted in the frequency or time domain. A number of methods are presented to determine the transfer function of a HFCT in both the frequency and time domain [37], [38]. The frequency domain method uses a source to produce a sinusoidal current signal for which the frequency is varied over a range to determine the output voltage from the HFCT under test. The transfer function of a HFCT is defined as the voltage output divided by the current input from the source. Generally, a network analyser is used to conduct such tests however, the availability of such equipment is often an issue [39]–[41].

The paper by Xioa Hu *et al.* [42] presents a novel method for determining the transfer function using a composite time domain method, this method compared well with the traditional frequency domain measurements.

Methods have been developed for the calibration of electromagnetic field sensors in transverse electromagnetic field cells which allow the generation of an electromagnetic field for the sensors to measure [43], [44]. Test methods which have been developed at the University of Strathclyde investigate the transient calibration of electric field sensors in a gigahertz transverse electromagnetic (GTEM) cell [45], [46]. In this work the electric field inside the GTEM cell is not calibrated, instead, an electric field sensor with a known transfer function was used and the voltage response was recorded. The sensor under test was installed and the response was recorded. The transfer function for the sensor under test was determined by performing a fast fourier transform (FFT) on the two voltage measurements. With the voltage measurements now in the frequency domain, the voltage response of the sensor under test was divided by the voltage response of the reference sensor, and finally, multiplied by the transfer function of the reference sensor. The accuracy of the transfer function of the reference probe was important in determining the transfer function of the sensor under test. The exposure of sensors used to detect magnetic fields to an electromagnetic field has received limited attention to date.

The switches incorporated in HVDC systems emit electromagnetic fields during the switching process of the HVDC system. The electric field emission of these switches will be investigated in this section. The electric field emission from the switches in a HVDC system has received interest since the early days of HVDC systems when mercury valves and thyristors were used [47]. This study found the radio interference recorded was related to the firing angle (α) of the thyristor valve. The interference was zero when $\alpha=0°$ and maximum when $\alpha=90°$. Mercury valves were found to release more radio noise than thyristors.

A later study investigated the level of electric field emission inside the converter halls of two early HVDC systems [48].

- The first was a mix of thyristors and mercury valves which had a maximum electric field measurement of 1.8 kV/m inside the valve hall and 0.28 kV/m outside the valve hall (during normal operation).
- The second system was a back to back converter with only thyristors. The electric field measurement inside the valve hall was 0.7 kV/m and the measurement system could not detect the electric field outside the converter hall.

A more recent study by Hu *et al.* [49] focused on an 800 kV 6250 A thyristor valve. The paper investigates the near field electromagnetic disturbances from the converter valve by installing the probe in close proximity to the converter valve. A wide frequency range was considered, the largest electric and magnetic field emissions were apparent at 50 Hz. At 50 Hz the largest electric field detected was 2034.3 V/m and the magnetic field was 165.53 μT. The disturbance level decayed with frequency and above 1.7 MHz the level matched the background noise.

There are limited papers focusing on the electric field emission of voltage source converters (VSC) converter stations. A study looking at VSC developed a model and compared this to actual measurements made in a HVDC converter platform [50]. The model uses the method of moments and antenna theory to determine the radiated emissions. The measurement of electric field had a maximum value of 105 dBμV/m (0.18 V/m) at 4.5 MHz. It was expected that the relatively low measures of electric field in the paper was due to the relatively high frequency range considered and dissipation of emissions due to the enclosure of the converters. The enclosure is generally designed like a faraday cage to reduce electromagnetic emissions from the converter with shielding provided by metal insulated panels.

The electric field emission of multilevel modular converter (MMC) has received less attention to date [51]. The electric field emission from a ±320 kV, VSC based, MMC HVDC system with 18 converter towers is discussed. The method of moments was used to determine the electromagnetic radiation for a number of different frequencies. The electric field emission around the converter was defined in four directions and 6 frequencies. The largest electric field emissions were found for the frequencies of 0.15 MHz and 1 MHz generally, as the frequency was increased the electric field magnitude reduced. The largest electric field at 0.15 MHz was 17 V/m near the DC bus bar. The largest electric field at 1 MHz was 20 V/m near the AC bus bar. The electric field reduced significantly when the distance from the converter was around 40 m. The paper mentions IEC 61000 [52] titled electromagnetic compatibility (EMC). The standard defines the necessary stages to ensure EMC compatibility. The main areas of interest are; the electromagnetic (EM) environment, the measurement of EMI, testing methods and the mitigation of EMI.

In terms of operating frequency of the converters a thyristor scheme has a maximum limit of 500 Hz [53], VSC schemes will generally operate in the multi kHz range [54] and MMC can operate as frequencies as low as the fundamental frequency (50 Hz)

[55]. The harmonics will be at multiples of these fundamental frequencies with the magnitude of the harmonics reducing for higher multiples of the fundamental.

The use of a GTEM cell to simulate transverse electromagnetic fields representative of that observed in converter stations will be investigated in this chapter. Specifically the behaviour of a HFCT when exposed to controlled electromagnetic field conditions will be explored.

2.2. SENSOR OPERATION: HIGH FREQUENCY CURRENT TRANSFORMER (HFCT)

A HFCT consists of a circular core (ferrite based) positioned around the primary circuit with a number of windings wrapped around the ferrite core inside the HFCT. In this case, the primary winding consists of a single turn (the cable under test) and the secondary consists of many turns (tens to hundreds) inside the HFCT. The current flowing through the primary circuit induces a magnetic field in the secondary windings of the HFCT and results in a proportional current in the HFCT windings. The ferrite core has a high permeability and facilitates the generation of a magnetic field through the secondary windings of the HFCT. A load (generally a 50 Ω input impedance in the measuring system) is installed across the terminals of the HFCT and measurement systems detect the voltage across this load. The general setup is shown in Figure 5.

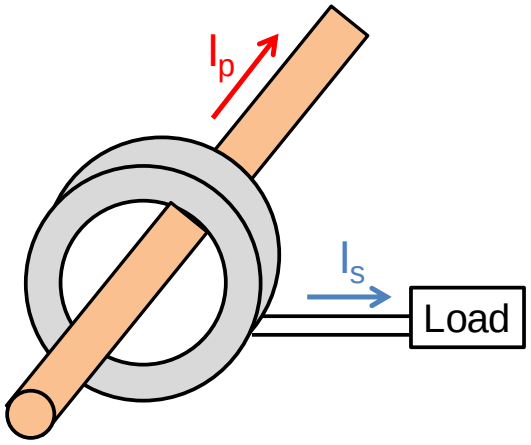


Figure 5 - Current transformer

The behaviour is the same as that of a transformer, the relation between the key quantities in the primary and secondary windings is given in (1).

$$\frac{V_s}{V_p} = \frac{N_s}{N_p} = \frac{I_p}{I_s} \quad (1)$$

The above can be rearranged to allow the determination of the current in the secondary winding (2).

$$I_s = \frac{N_p}{N_s} I_p \quad (2)$$

Thus by measuring the low level current in the secondary circuit the current flowing in the primary can be calculated. This principle can be used to detect the resulting current pulse produced during PD activity in the primary circuit and therefore calculate the charge contained within the detected current impulse (3).

$$q = \int_{t_0}^{t_1} i(t)dt \quad (3)$$

This relation can be rearranged to calculate the charge of the current pulse in the primary winding of the cable under test. The terminals of the HFCT are connected across the input impedance of the measurement system (50 Ω) and a voltage pulse is registered. The charge contained in the voltage pulse detected by the monitoring system is shown in (4).

$$q = \frac{1}{Z_{TR}} \int_{t_0}^{t_1} v(t)dt \quad (4)$$

Z_{TR} is the transfer impedance (mV/mA) of the HFCT onto the 50 Ω load (input impedance of the measurement system) when an input current is passing through the primary windings, the transfer impedance is defined in (5).

$$Z_{TR} = \frac{Output\ of\ the\ HFCT\ onto\ 50\Omega\ (mV)}{Input\ current\ (mA)} \quad (5)$$

The transfer impedance is generally stamped on HFCTs following the calibration process by the HFCT manufacturer. The HFCT characterisation process will be discussed in the following section.

2.3. CHARACTERISATION METHOD

In this section a method is presented for the characterisation for HFCT sensors. This method would be required either if the calibration certificate was not available or the sensor's calibration needed to be periodically verified during the sensors service life. The method is based on previous work by Xiao Hu *et al.* [42]. This section details the methodology employed to characterise the response of three HFCTs over the frequency range of interest.

2.3.1. METHOD: HFCT CHARACTERISATION

In this method a network analyser was used to characterise a number of HFCTs. A network analyser can be used to determine the gain response of the device under study over the frequency range of interest. Essentially a network analyser has:

- An internal signal generator to excite the device under study
- A receiver to recover the device response
- Internal logic
- A display screen

The Hewlett Packard 8714C RF network analyser was employed with:

- Frequency range of 0.3-3000 MHz
- 'RF out' port was used to supply the signal being generated
- 'RF in' was used to return the device response to the network analyser
- The frequency response is determined by internal logic
- Computed response is displayed to the user

The network analyser was used to characterise a number of HFCTs over the frequency range from 0.3 MHz to 80 MHz (more focused on the range of interest). The test set-up is illustrated in Figure 6.

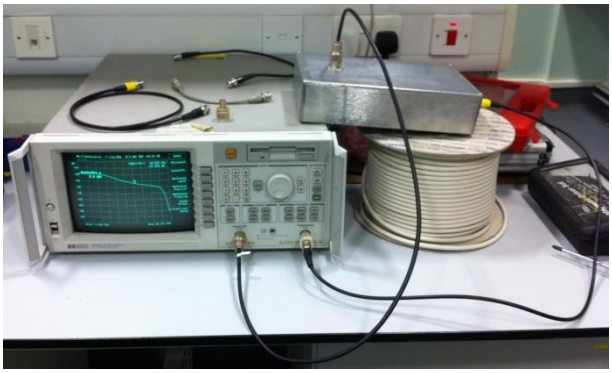


Figure 6 - HFCT characterisation test set-up

Initially, the network analyser was calibrated using the Bayonet Neill–Concelman (BNC) cables which will be employed in further characterisation tests. The HFCT under test was enclosed in an aluminium box to minimise interference and ensure an accurate representation of the HFCT transfer function. Within the enclosure, the HFCT is installed around a copper rod and both are insulated from the enclosure case. An illustration of the test circuit is shown in Figure 7. The method was adopted from work by Xiao Hu at the University of Strathclyde [37].

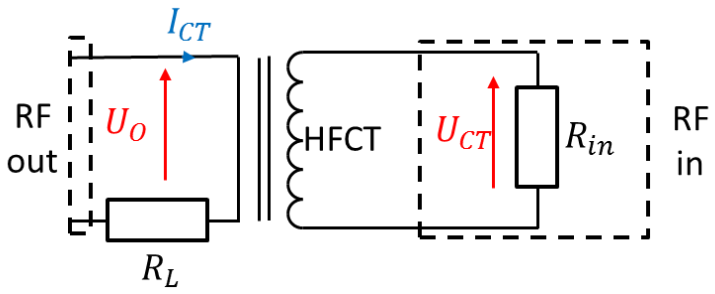


Figure 7 - HFCT characterisation test circuit and connections to network analyser ('RF in' and 'RF out')

The 'RF out' port from the network analyser passed through the centre of the HFCT (via the copper rod) and was connected to R_L which was a 50 Ω termination. The HFCT was connected to the 'RF in' of the network analyser and the voltage was measured across the input impedance of the network analyser R_{in} (which was 50 Ω). The network analyser was run and the gain of the HFCT was recorded on the network analyser display.

Three HFCTs (HFCT HC 100/50, HFCT 75/35 and HFCT 100/50 ALU) were tested using this method. The response of the HFCTs over the frequency range of interest (0-80 MHz) is shown in Figure 8.

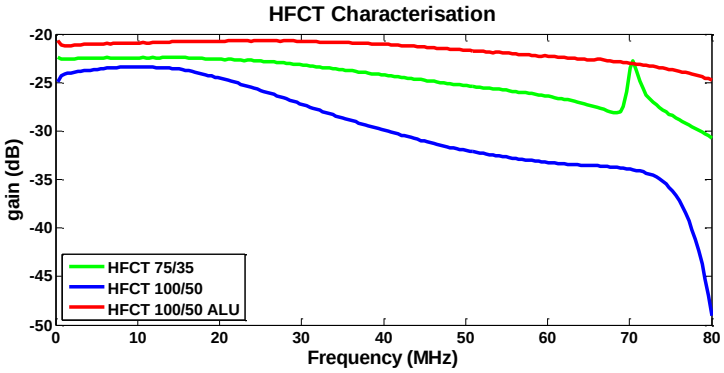


Figure 8 - HFCT gain (dB) over the frequency range of 0-80 MHz

The general process below outlines the requirements to calculate the transfer impedance of the HFCT over the frequency range of interest. The transfer impedance is the current through the device divided by the voltage across the device. The *Transmission (dB)* is the gain registered by the network analyser, P_{trans} is the power transmitted through the device and P_{inc} is the incident power (10 dBm).

2.3.1.1. Calculation of current through the HFCT

The incident power (P_{inc}) from the network analyser was 10 dBm and the load resistance (R_L) was 50 Ω. The voltage across the primary winding (U_O) can be determined using (6).

$$U_0 = \sqrt{P_{inc} R_L} \tag{6}$$

With U_O known the current through the HFCT (I_{CT}) can be calculated from (7).

$$I_{CT} = \frac{U_0}{R_L} \tag{7}$$

2.3.1.2. Calculation of voltage across the HFCT

In order to calculate the voltage across the HFCT windings (U_{CT}) the following equation was used as the basis for further calculations.

$$Transmission(dB) = 10\log\left(\frac{P_{trans}}{P_{inc}}\right) \quad (8)$$

The above equation was re-arranged to determine the power transmitted through the device (P_{trans}).

$$\frac{Transmission(dB)}{10} = \log\left(\frac{P_{trans}}{P_{inc}}\right) \quad (9)$$

Using the laws of logarithms equation (9) above can be rearranged from above to provide the following.

$$10^{\left(\frac{Transmission(dB)}{10}\right)} = \frac{P_{trans}}{P_{inc}} \quad (10)$$

Further rearrangement yields the power transmitted through the device.

$$P_{trans} = P_{inc} * 10^{\left(\frac{transmission(db)}{10}\right)} \quad (11)$$

The steps above have allowed P_{trans} to be calculated and with knowledge that the input resistance (R_{in}) was 50 Ω. The voltage across the HFCT can be calculated using (12).

$$U_{CT} = \sqrt{P_{trans}R_{in}} \quad (12)$$

With U_{CT} and I_{CT} now known for the HFCT in question, the transfer impedance (X_{CT}) can be calculated.

$$X_{CT} = \frac{U_{CT}}{I_{CT}} \tag{13}$$

2.3.2. RESULTS: HFCT CHARACTERISATION

The method above allowed the transfer impedance of the three HFCTs to be calculated across the frequency range of interest as shown in Figure 9.

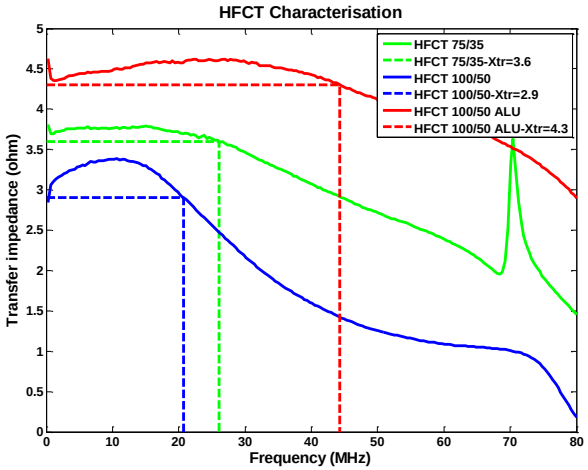


Figure 9 - HFCT characterisation results (solid lines indicate the results obtained from the test methodology, dotted lines show the stamped transfer impedances for each HFCT with the vertical lines indicating the upper -3 dB point)

The results match the associated data sheet with the HFCTs up to 80 MHz. The manufacturer's test method covers the frequency range up to 300 MHz. This method enables a greater confidence in the sensor response and allows systematic testing of HFCTs to be conducted. The sensor's marked transfer impedance (derived using an alternative method by the manufacturer) matches the value obtained using this characterisation method. The manufacturers data for the five HFCTs considered in this study are detailed in Table I.

Table I - HFCT manufacturers data

Sensor Name	Transfer impedance (mV/mA)	-3 dB frequency response (MHz)	Max 50 Hz AC current (A)	Casing material
75/35	3.6	100 – 25	45	HDPE
100/50	2.9	100 – 20	80	HDPE
100/50 ALU	4.3	100 – 25	350	Aluminium
140/100	3.2	100 – 12	300	HDPE
140/100 HC	1.8	350 – 35	1000	Aluminium

2.4. SCALING FACTOR OF PD PULSES

This section details the test method for determining the sensitivity of the PD measurement sensor for further PD measurements employing the 100/50 ALU HFCT. In this work the Lemke LDS-6 calibrator was used to apply a pulse with a known charge across a void type sample. This would enable the measurement range of the measuring impedance/HFCT in pC to be known for future PD testing. This type of analysis has been conducted in the past [56] this work was repeated to establish a baseline for testing conducted as part of this thesis.

2.4.1. DIRECT MEASUREMENT OF CALIBRATOR PULSES

The Lemke LDS-6 calibrator was directly connected to the Lecroy 104Xi oscilloscope to measure the magnitude of the voltage pulses emitted from the calibrator. A Tektronix TDS 2024 oscilloscope was used to record the output from the calibrator, with the Tektronix scope only having a 1 MΩ input, a 50 Ω feed-through termination was used to get the voltage output across a 50 Ω load. The direct pulses produced by the calibrator shown in Table II.

.

Table II - Calibrator voltage pulses when directly connected to the Tektronix TDS 2024 oscilloscope

Calibrator output	500 pC	100 pC	20 pC	5 pC
Calibrator output onto 50 Ω (mV)	696	152	34.4	16

The peak voltage output of the calibrator was non-linear and similar behaviour was observed while using a Lecroy 104 Xi oscilloscope. This was not expected but the behaviour exhibited by the calibrator was consistent over the study period. It is anticipated that there With the voltage output from the calibrator known, the voltage output from the sensors when the calibrator was applied to the AC and DC test circuits can be determined. These test circuits and baseline measurements will be used in this thesis. This work is detailed in the following sections.

2.4.2. AC TEST CIRCUIT ANALYSIS

The following measurement setup (Figure 10) was used without the AC test set energised to establish the response of the 100/50 ALU HFCT to calibrator pulses. The LDS-6 calibrator was installed across the void sample. The output from the Lemke measuring impedance (LDM 5/U) was directly connected to the oscilloscope input (via a 50 Ω through termination).

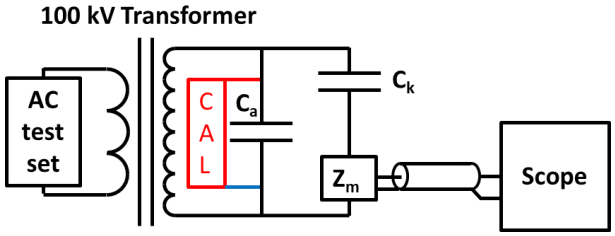


Figure 10 - AC PD measurement with calibrator installed across the void type sample and the measuring impedance connected to the oscilloscope

The peak value of the voltage pulse recorded on the Tektronix TDS 2024 oscilloscope when connected to the measuring impedance is detailed in Table III.

Table III - Measuring impedance response to calibrator pulse across the void type test sample

Calibrator output	500 pC	100 pC	20 pC	5 pC
HFCT output onto 50 Ω (mV)	400	73.6	15.4	3.2
Scaling Factor (pC/mV)	1.25	1.36	1.3	1.56

The scaling factor was also calculated for the four calibration settings both the maximum output (500 pC) and the minimum (5 pC) could be recorded.

2.4.3.DC TEST CIRCUIT ANALYSIS

The DC test circuit (Figure 11) was constructed by adding a capacitor (C_k), diode (D), inductor (L) and resistor (R_D). The components are manufactured by HighVolt and is designed to provide a practically continuous DC output according to IEC 60060-1 [57] between 20-80% of the rated voltage. The standard stipulates that the ripple must be less than 3% of the DC output. Again, the test setup was not energised. The LDS-6 calibrator was installed across the void type dielectric sample. Under DC conditions a HVPD 100/50 HFCT was used to detect the PD activity. The HFCT is generally employed for detecting PD activity in cable systems due to the versatility in final positioning of the sensor. The output of the HFCT was connected to the input of the Tektronix TDS 2024 oscilloscope (via a 50 Ω feed-through termination). The test circuit detailing the position of the calibrator is shown in Figure 11.

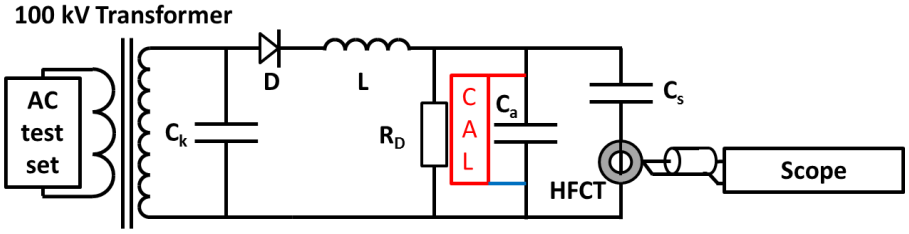


Figure 11 - DC test circuit detailing the position of the HFCT across the test sample and the HFCT directly connected to the oscilloscope

The peak value of the voltage pulses recorded by the Tektronix TDS 2024 oscilloscope are detailed in Table IV.

Table IV - Peak values of the voltage pulses recorded by the oscilloscope when connected to the HFCT

Calibrator output	500 pC	100 pC	20 pC	5 pC
HFCT output onto 50 Ω (mV)	56	12.6	Not detectable	Not detectable
Scaling Factor (pC/mV)	8.9	7.94	N/A	N/A

It is clear that the scaling factor has degraded compared to that of the measuring impedance so much so that the 20 pC and 5 pC pulses could not be measured. In the not detectable state the response of the HFCT could not be differentiated from the background noise. A more sensitive HFCT with a larger transfer impedance may have enabled the response to be above the background noise, alternatively signal conditioning around reducing the background noise would improve the behaviour in this low amplitude range. Having performed these experiments the behaviour of the PD measurement system under both AC and DC conditions has been determined. There was no limitation evident in the AC test circuit but under DC conditions the 20 pC and 5 pC pulses could not be detected (based on available calibrator settings).

2.5. IMMUNITY TESTING METHOD

This section details the testing conducted on HFCTs and a transient earth voltage (TEV) sensor when these sensors were exposed to a controlled electromagnetic field. The overall aim of this method is to introduce a process whereby the relative immunity of sensors can be tested in a known electromagnetic field environment. This is of interest because it simulates the electromagnetic field environment that these sensors will be exposed to inside a HVDC converter station.

Interference testing on the PD sensors supplied by HVPD was conducted using the Strathclyde GTEM cell. The HVPD sensors tested in this study were as follows:

- 75/35P HFCT
- 100/50 HFCT
- 140/100 HFCT
- 100/50ALU HFCT
- 140/100HC HFCT

- TEV

These sensors represent a range of PD sensors with different designs and casings. The theory that impacts sensor behaviour, method employed and results for each sensor are outlined in the following sections.

2.5.1. THEORY: INTERFERENCE TESTING

The skin effect was considered for conductive materials to describe how the current density reduces below the surface of the conductor. The skin depth is the depth below the surface of the conductor for the current density to falls below 1/e, 37 % of the value at the surface. The penetration depth of the electromagnetic field for the sensor casings of interest will be the driving force for the relative immunity of the sensors tested. A practical formula for skin depth (δ) is given by equation (14).

$$\delta = \sqrt{\frac{2\rho}{(2\pi f) \times (\mu_0 \mu_r)}} \tag{14}$$

With ρ being the resistivity of the medium (Ω.m), f is the frequency of the electromagnetic wave (Hz), μ_0 is the permeability of free space ($4\pi x10^{-7}$ H/m) and μ_r is the relative permeability of the medium (μ_{r_cu}=0.999994, μ_{r_alu}=1.000022). The two casings studied in this work are Aluminium and HDPE plastic. The skin depth of HDPE is significantly higher (minimum of ten orders of magnitude) than that of aluminium and copper. The variation of skin depth between 50 Hz and 2 GHz is illustrated in Figure 12.

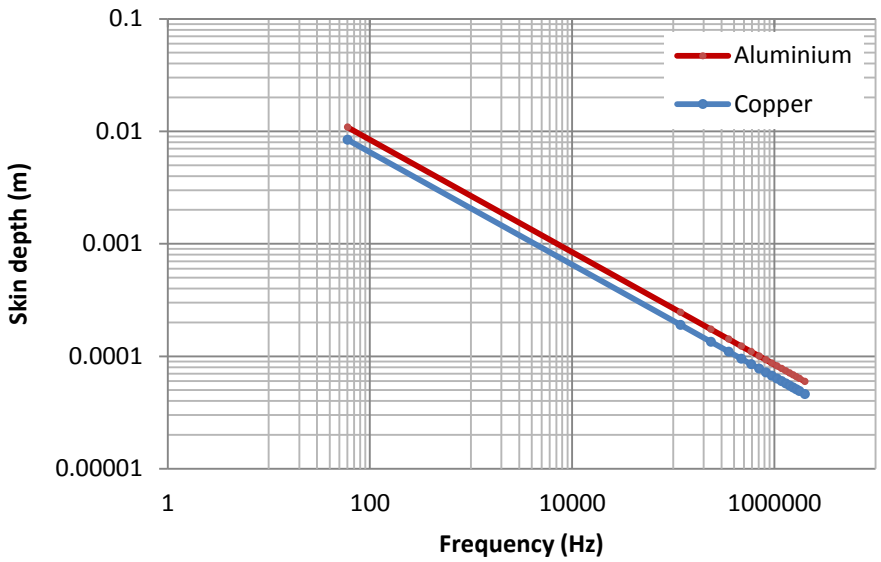


Figure 12 - Variation of skin depth with frequency for aluminium and copper

As the frequency increases the skin depth reduces due to the effective resistance of the conductor to increasing. Copper and alloys with extremely high permeability are potential materials that could be employed to allow thinner casings that more effectively dissipate the electromagnetic field effects on the windings of the HFCT.

2.5.2. METHOD: INTERFERENCE TESTING

The PD sensors were tested in the GTEM cell in the high voltage lab at the University of Strathclyde, an illustration of the GTEM cell is shown in Figure 13. A GTEM cell is generally used to calibrate electric field sensors such as UHF sensors.

In this work the GTEM cell was used to expose a PD sensor to a controlled electromagnetic field to determine the sensor response when exposed to a controlled electromagnetic field. The voltage response of the sensor to a controlled electromagnetic field will be calculated for a number of HFCTs and a TEV. This setup emulates the conditions PD sensors will be exposed to in environments where significant electromagnetic fields may be present, for example in the converter hall of a HVDC installation. In a HVDC system the power electronic devices, central to the system operation, emit electromagnetic fields during high frequency switching operations.

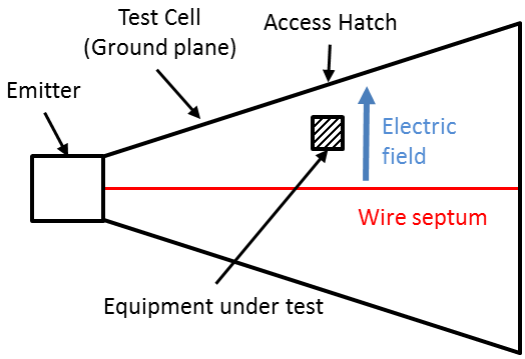


Figure 13 - Diagram of GTEM cell

The function of the GTEM cell is to guide an electromagnetic transient from the emitter to the equipment under test. The electric field is generated between the wire septum and the cell wall. The current carrying conductor of the wire septum will generate a magnetic field, in the top half of the GTEM cell the magnetic field is perpendicular to the electric field (i.e. pointing out of the page at right angles). The input to the GTEM cell is a fast transient (step input) which generates the electric field. The step input is 10 V (rise time less than 50 pS) and the peak amplitude of the electric field was 35 V/m at the access hatch of the GTEM cell [46]. The sensor response is detected using a Lecroy 104Xi oscilloscope (bandwidth 1 GHz) before the arrival of the reflected pulse from the end of the GTEM cell (approximately 10 nS). The overall system layout is detailed in Figure 14.

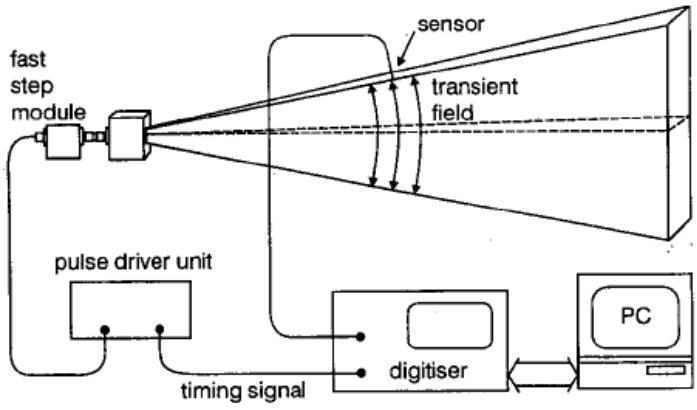


Figure 14 - Architecture of the transient calibration system [46]

The output of a picosecond pulse generator (repetition rate set at 0.1 kHz) was connected to the emitter of the GTEM cell. The equipment under test (EUT) and the

timing signal from the pulse generator was connected to the LeCroy 104Xi oscilloscope using two separate channels. The data recorded by the LeCroy 104Xi was transferred to a PC running a LabVIEW virtual instrument (VI) for data logging and subsequent data analysis in the VI.

Prior to system operation a calibration procedure was completed using a sensor with a known transfer function (H_{ref}). The calibration procedure allows the transfer function of the cell (H_{cell}) and system (H_{sys}) to be determined. Following the calibration procedure the transfer function for the sensor under test (H_{sens}) was determined.

The transient system calibration uses a reference probe with a known transfer function, in this case the monopole was used as the transfer function can be derived. The transfer function (H_{ref}) of the monopole is given by (15).

$$H_{ref} = \frac{V_L}{E_I} = \frac{h_e Z_L}{Z + Z_L} \tag{15}$$

In (15) E_I is the electric field at right angles to the ground plane (the cell wall). V_L is the voltage across the load impedance (Z_L). The effective height (h_e) and impedance (Z) are frequency dependant functions of the probes dimensions [46]. The frequency dependant transfer function for the monopole probe was derived in [46], the transfer function over frequency is detailed in Figure 15.

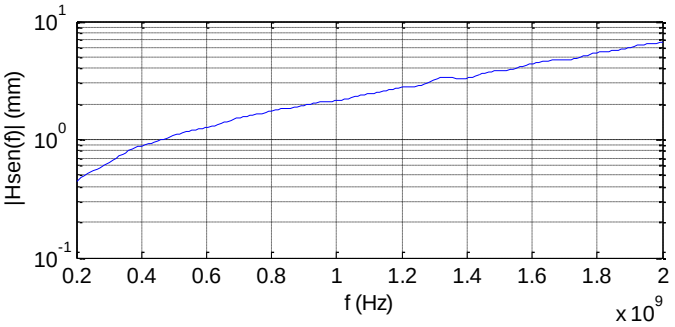


Figure 15 - Monopole frequency dependant transfer function

A swept frequency calibration was conducted at the national physical lab (NPL) on the monopole [46]. The maximum error in the transfer function derived for the

monopole using the transient technique at UoS was 1.7 dB when compared to the swept frequency response at NPL.

The determination of the unknown transfer function (H_{sens}) of the EUT is graphically represented in Figure 16.

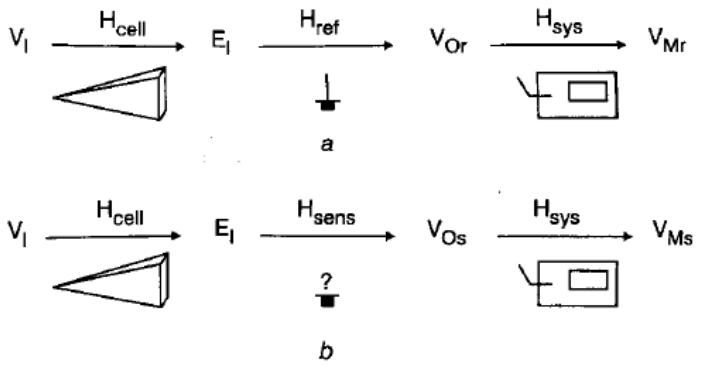


Figure 16 - System diagram for transfer function derivation [46]

V_I is the input voltage to the GTEM cell, E_I is the electric field apparent at the hatch of the GTEM cell, V_O is the output voltage from the sensor and V_M is the measured output voltage (includes overall system response). The system is initially calibrated using the reference probe with a known transfer function (H_{ref}) to enable the determination of H_{sens} (16).

$$H_{sens} = \frac{V_{Os}}{E_I} = \frac{V_{Ms}}{H_{sys}E_I} \tag{16}$$

The reference probe was installed in the GTEM cell and the sensor response (V_{Mr}) to the transient field (E_I) was logged and stored during calibration (as opposed to calibrating the incident electric field). The EUT was installed in the GTEM cell and the response (V_{Ms}) was logged using the measurement system. The incident electric field, whilst the EUT was installed in the GTEM cell, can be represented by (17).

$$E_I = \frac{V_{Mr}}{H_{sys}H_{ref}} \tag{17}$$

Substituting (17) into (16) enables the transfer function of the EUT to be calculated using the measured responses (18).

$$H_{sens} = \frac{V_{Ms}}{V_{Mr}} H_{ref} \tag{18}$$

Equation (18) was implemented in the 'UHF sensor Calibration' LabVIEW program on the PC with the voltage responses converted to frequency responses using FFT methods. The LabVIEW software determines the electromagnetic field response of the sensor under test over the frequency range of 0-2000 MHz. Indeed, the frequency response of the measurement system was not required to calculate the response of a sensor to an incident electromagnetic field and is one particular benefit of this approach. Using a reference sensor with a known transfer function (H_{ref}) was crucial to this methods success, in this case a monopole sensor was utilised. The monopole probe was previously calibrated by the National Physical Laboratory (NPL) [46], the calibrated and measured values were in close agreement.

The orientation of the EUT in the GTEM cell was varied and the response of the sensor to an electromagnetic field in that orientation was recorded using the LabVIEW software. The EUT was varied in orientation with respect to the cell wall and wire septum. Two variations were derived to investigate the effect of a resulting electromagnetic field on the EUT.

- In variation one the electric field passed through the cross section of the HFCT
- In variation two the electric field was directed through the centre of the HFCT

The following angles were used to define the orientation of the HFCT in the GTEM cell for each measurement for variation one.

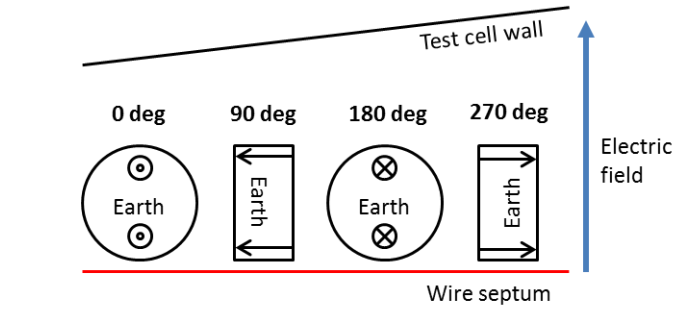


Figure 17 - Variation one with electric field passing through the cross section of the HFCT for four different orientations in the GTEM cell (emitter to the LHS)

Following this, variation two consisted of the EUT being rotated in the other sense (wire septum being the axis of rotation. The electric field was directed through the centre of the HFCT. The following labelling was used to define the orientation of the EUT in the GTEM cell.

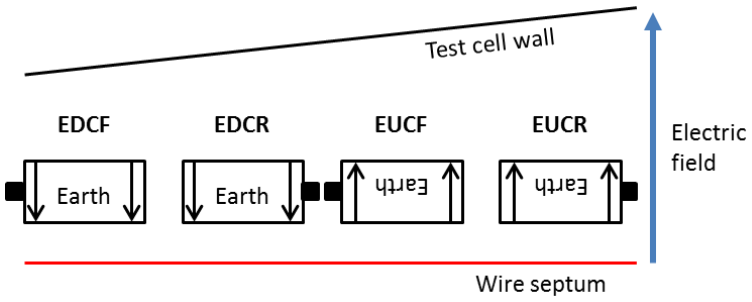


Figure 18 - Variation two with electric field passing through the centre of the HFCT for four different orientations in the GTEM cell (emitter to the LHS)

The naming convention adopted above was as follows:

- EDCF – Earth label down and BNC connector forward
- EDCR – Earth label down and BNC connector rearward
- EUCF – Earth label up and BNC connector forward
- EUCR – Earth label up and BNC connector rearward

To allow the measurements above to be conducted, an adjustable mounting plate was fabricated (this plate would allow additional incremental measurements to be made in the future). The mounting plate had a number of holes allowing the adjustment of the orientation of the EUT inside the GTEM cell. The HFCTs were suspended using tie wraps to position the sensor at the desired orientation.

The HFCTs were initially tested independently inside the GTEM cell. This method was expanded to include a cable section inside the centre of the HFCT to determine how the sensitivity to an electromagnetic field would be affected. This phase was included to explore whether the inclusion of a cable inside the HFCT affected the sensor response to an external electromagnetic field. The cable section was left open circuit during the application of electromagnetic fields inside the GTEM cell.

Generally HFCTs are installed in a number of ways to allow the detection of the PD pulses emitted from an insulation defect. The most common method is to place the HFCT on the cable sheath on its own. Alternatively the HFCT could be installed on the conductor but the cable sheath must be brought back through the centre of the HFCT.

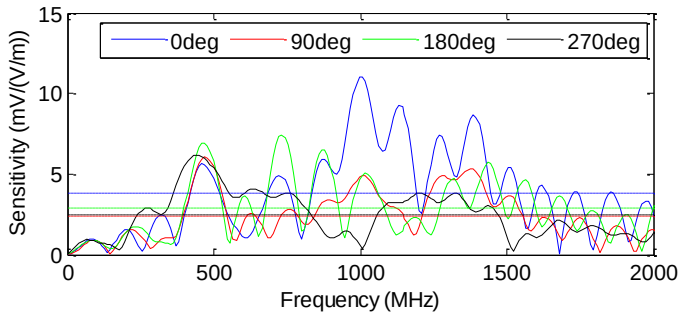
The results of this work allowed a method to test sensors in a representative electromagnetic field environment to be developed. A range of HFCTs are tested, with different transfer impedances and casings. The behaviour of HFCTs in a controlled electromagnetic field will be investigated and the best performing HFCT will be identified.

2.5.3. RESULTS: INTERFERENCE TESTING SENSORS ALONE

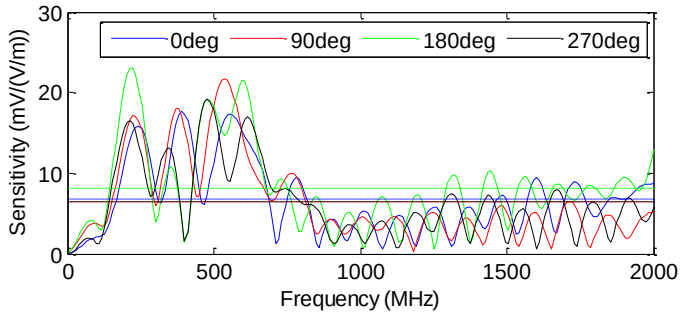
In the first phase of testing, the sensors were tested with no cable section inside the HFCTs. That is the HFCT was suspended from the mounting plate and connected to the measurement system. The subsequent sections present the results from each PD sensor interference test using the method discussed above.

2.5.3.1. Variation one: sensor rotated perpendicular to the electric field

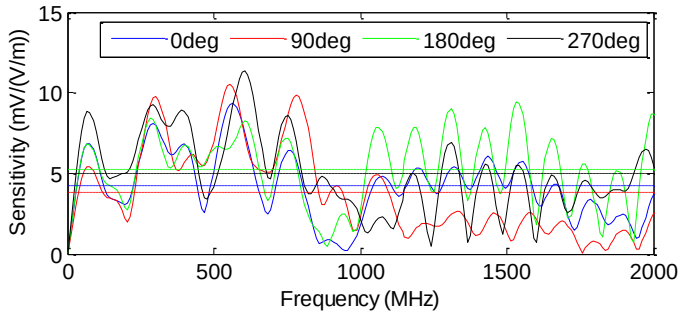
The HFCTs most affected by the electromagnetic field generated inside the GTEM cell had the high density polyethylene (HDPE) plastic casings. The sensitivity to electromagnetic field for the HDPE casing HFCTs is illustrated in Figure 19 for the frequency range of 0-2000 MHz.



(a)



(b)

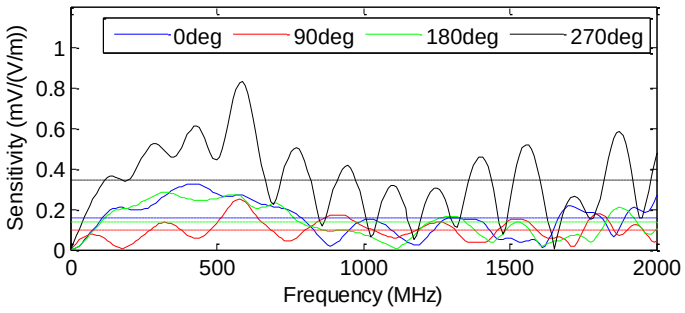


(c)

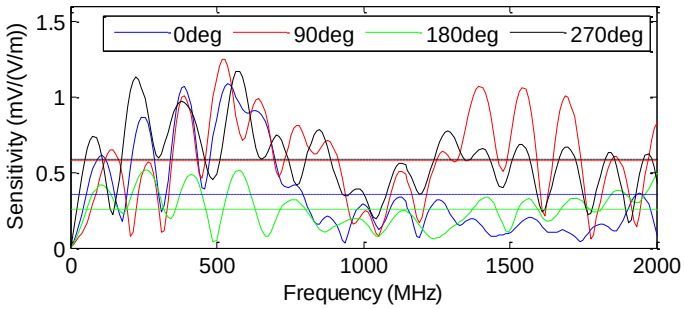
Figure 19 - Sensitivity over the frequency range of interest for the HDPE plastic casing HFCTs: (a) HVPD 75/35 HFCT (b) 100/50 and (c) 140/100 (dashed line detailing averaged values)

The 100/50 HFCT with the HDPE casing was found to have the highest sensitivity to electromagnetic field over the frequency of 100-700 MHz. The 140/100 HFCT was more sensitive to the electromagnetic field than the smallest 75/35 HFCT.

The sensitivity of the HFCTs with aluminium casings was also determined for variation one. The sensitivity to the generated electromagnetic field for the two HFCTs for the frequency range of 0-2000 MHz is detailed in Figure 20.



(a)



(b)

Figure 20 - Sensitivity over the frequency range of interest for the aluminium casing HFCTs: (a) HVPD 100/50 ALU HFCT and (b) HVPD 140/100 HC HFCT (dashed line detailing averaged values)

The sensitivity of the 100/50 ALU HFCT was higher for the full frequency range in the 270 deg orientation. It is anticipated that the alignment of the magnetic field in this orientation has led to an increase in sensitivity as the electric field effects will be consistent for the four orientations. The BNC connection was always pointing upwards inside the GTEM cell for variation 1 so the increased thickness of the HFCT casing at this point will not play a part. The HFCT least affected by the electromagnetic field generated inside the GTEM cell for variation one was the 100/50 ALU HFCT. The 140/100 HFCT was generally more sensitive to the electromagnetic field across all four variations.

2.5.3.2. Variation two: sensor rotated around the electric field

In variation two the electric field passed through the centre of the HFCT. The orientation of the HFCT was altered in a number of ways. Firstly the direction of the earth label on the HFCT, was either up (same way as the electric field) or down (reverse to electric field) with respect to the septum in the GTEM cell. A further

variation was applied whereby the BNC connector was either forward or rearward when positioned in the GTEM cell.

The results of testing the HFCTs in variation two will be presented in the following section. The HFCTs with HDPE plastic casings were tested for the four orientations in variation two. The sensitivity to the electromagnetic field generated inside the GTEM cell for the three HFCTs with HDPE casings is illustrated in Figure 21.

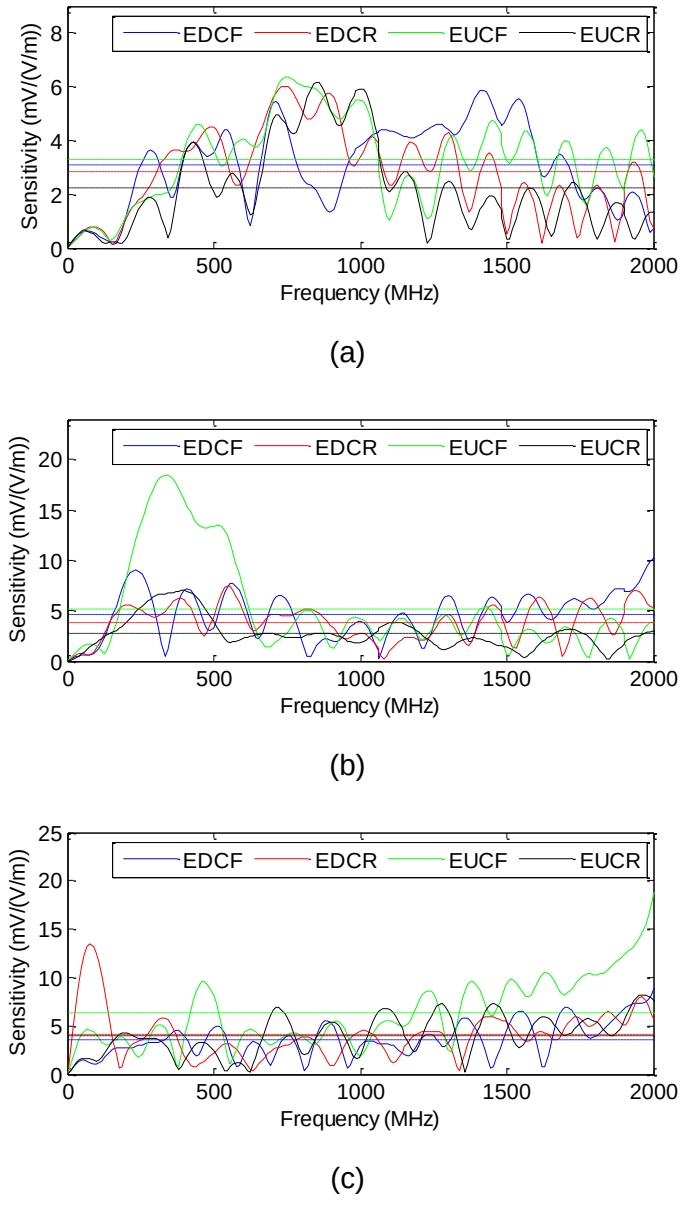
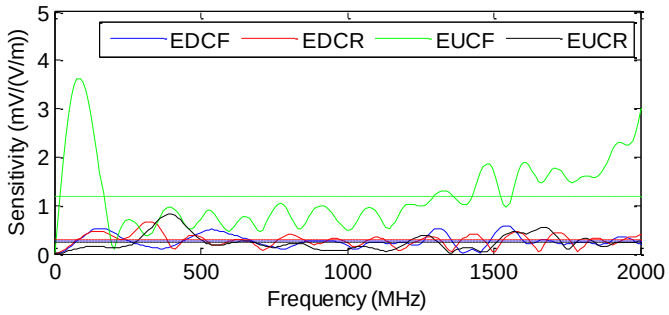


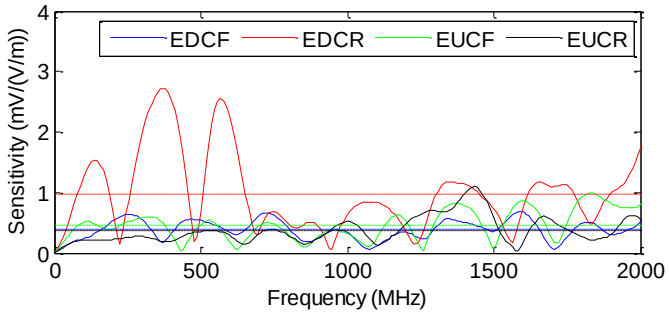
Figure 21 - Sensitivity over the frequency range of interest for the HDPE plastic casing HFCTs: (a) HVPD 75/35 HFCT (b) 100/50 and (c) 140/100 (dashed line detailing averaged values)

The orientation particularly affected (highest peak and average sensitivity) was when the earth label was pointing upwards and the connection to the HFCT was forwards (EUCF) for all HFCTs. The HFCT most affected by the exposure to the electromagnetic field inside the GTEM cell was the 100/50. The 140/100 HFCT was also most sensitive to electromagnetic fields. The HFCT which was least affected by the electromagnetic field in the GTEM cell was the 75/35 HFCT.

The HFCTs with aluminium casings were also tested in the variation two orientations. The sensitivity to electromagnetic field was recorded over the frequency range 0-2000 MHz and is shown in Figure 22.



(a)



(b)

Figure 22 - Sensitivity over the frequency range of interest for the aluminium casing HFCTs: (a) HVPD 100/50 ALU HFCT and (b) HVPD 140/100 HC HFCT (dashed line detailing averaged values)

In variation two, the 140/100HC HFCT was shown to be the least sensitive to the electric field passing through the centre of the HFCT when the two HFCTs with aluminium casings were compared. Interestingly, the 140/100HC HFCT was most sensitive when the earth was down and the connector was to the rear (EDCR). This was different to all the other sensors which recorded the highest sensitivity when the

earth arrow was pointing upwards and the connector on the HFCT was pointing rearwards (EUCR) in the GTEM cell.

2.5.1. RESULTS: INTERFERENCE TESTING SENSORS AND CABLE SECTION

The test method was expanded to include a length of cable within the centre of the HFCT during the immunity testing inside the GTEM cell. This testing was conducted to determine the effect of the cable section on the sensor response due to the electromagnetic field in the cell. The cable was located inside the centre of the HFCT using foam spacers to ensure a tight fit inside the HFCT. The cable was a Prysmian 11 kV cable with EPR insulation the length of the cable was 130 mm. The testing was conducted on the two 100/50 HFCTs, one being the HDPE casing and the other being the Aluminium casing.

Figure 23 - 100/50 HFCTs with 11 kV Prysmian EPR cable HDPE casing (left) and aluminium casing (right)

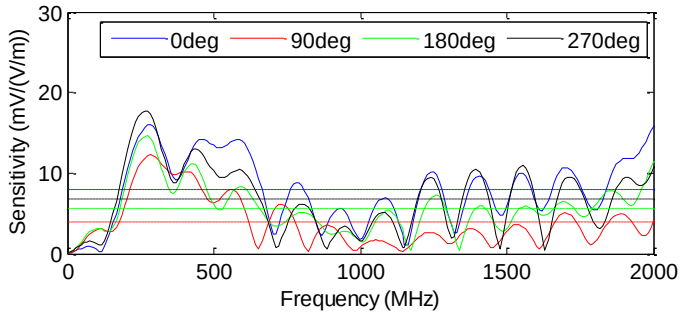
The two variations used in previous testing were applied to the two sensors and the response of the sensors was determined. The sensor responses were compared to when no cable was present inside the centre of the HFCT. The results of this investigation are detailed in the following subsections.

2.5.1.1. Variation one: sensor rotated perpendicular to the electric field

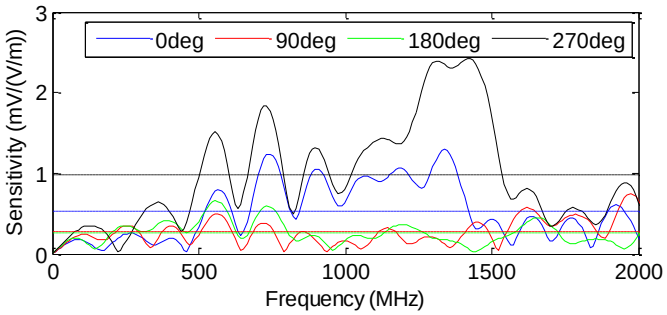
Variation one demonstrated when the electric field was passed through the cross section of the HFCT. The responses of the two HFCTs with the cable section within the centre of the HFCT are illustrated in Figure 24.

In variation one, the response of the 100/50 HFCT with HDPE casing has mainly altered over the frequency ranges of 100-700 MHz and 1200-2000 MHz. Over the range 100-700 MHz the sensitivity to the incident electromagnetic field has reduced for the four orientations. In contrast, for the frequency range of 1200-2000 MHz the

sensor was more sensitive to the incident electromagnetic field. The sensitivity of the 100/50 ALU HFCT was mainly altered over the frequency range of 700-1700 MHz otherwise the sensitivity was very similar. Over the frequency range of 700-1700 MHz the sensitivity increased significantly. The average sensitivity of the 100/50 ALU with the cable section was higher than with no cable section.



(a)



(b)

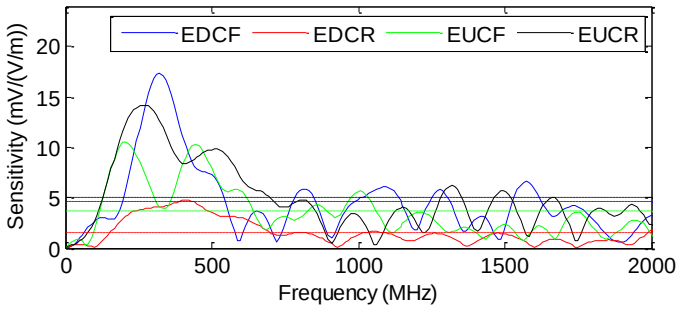
Figure 24 - Variation one with cable inside the HFCTs (a) 100/50 with HDPE casing (b) 100/50 with aluminium casing

2.5.1.2. Variation two: sensor rotated around the electric field

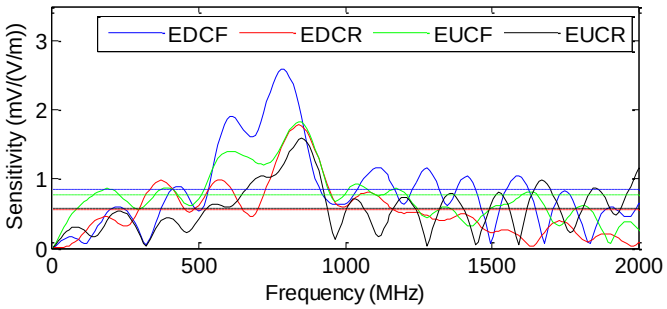
In variation two the HFCT was orientated so that the electric field passes through the centre of the HFCT in the four defined orientations. The response of the two 100/50 HFCTs with the EPR cable installed in the centre of the HFCT are detailed in Figure 25.

The effect of including a cable section inside the 100/50 HFCT with a HDPE casing was minimal with a slight increase in sensitivity for some orientations over the frequency range of 100-600 MHz. The mean sensitivity for the four orientations was very similar with and without the cable section inside the HFCT. The 100/50 ALU

HFCT was more affected by the inclusion of a cable section. A distinct peak in sensitivity was introduced over the frequency range of 500-900 MHz when the cable section was included. In general, over the full frequency range the sensitivity of the 100/50 ALU HFCT increased when the cable section was included.



(a)



(b)

Figure 25 - Variation two with cable inside the HFCTs (a) 100/50 with HDPE casing (b) 100/50 with aluminium casing

2.5.2. RESULTS: TEV SENSOR TESTING IN ELECTRIC FIELD ENVIRONMENT

An alternative sensor made available by HVPD was the transient earth voltage (TEV) sensor. This type of sensor is generally used in the detection of PD emitted from earth bonded metal surfaces. Radio frequency signals emitted from the defect inside the metal cladding meets the metal cladding and breaks out at joints in the cladding or other openings in the housing. Generally, a number of these sensors are placed round the housing of interest and are used to locate where the PD producing defect is located inside a metal housing (time of flight method used). The casing of the sensor was made of HDPE plastic. This sensor could be subject to

electromagnetic fields in the HVDC environment, as such the response of this sensor to a controlled electromagnetic field was tested.

The TEV was tested to determine the sensitivity over the same frequency range of interest. Variation one was conducted with the TEV suspended inside the GTEM cell and the TEV was rotated around the incident electric field. The orientation (viewed from the emitter end of the GTEM cell) was varied as illustrated in Figure 26.

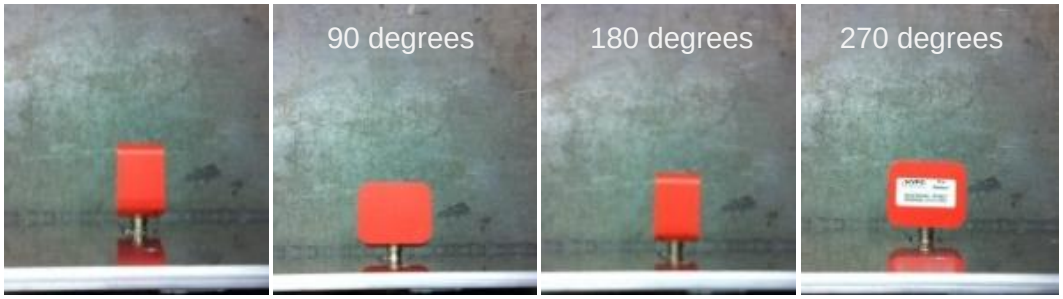


Figure 26 - Orientations of TEV in variation one viewed from GTEM emitter

Variation two was conducted with the TEV mounted on the hatch inside the GTEM cell, this is how the sensor would be installed in the application environment. The orientation of the TEV (viewed from the emitter end of the TEM cell) for each angle is illustrated in Figure 27.

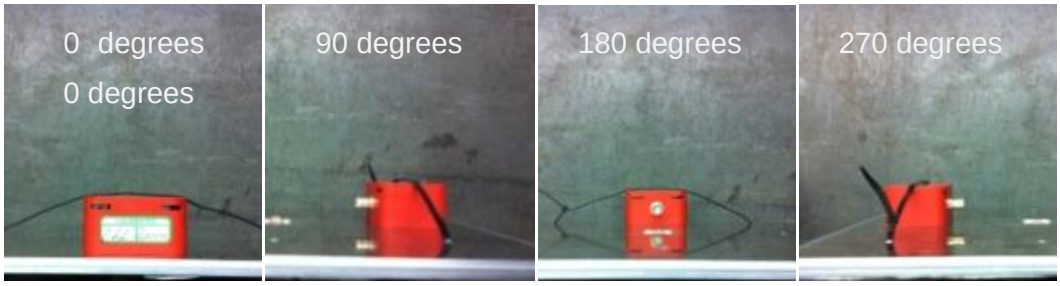
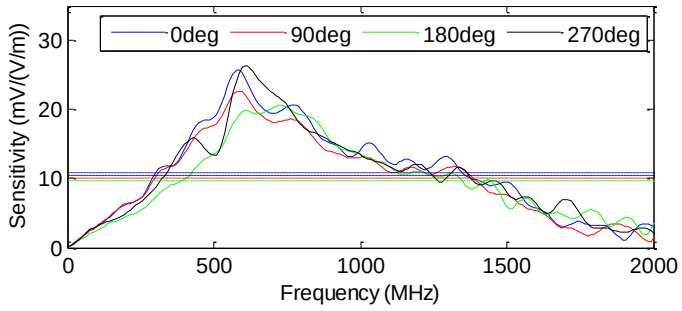
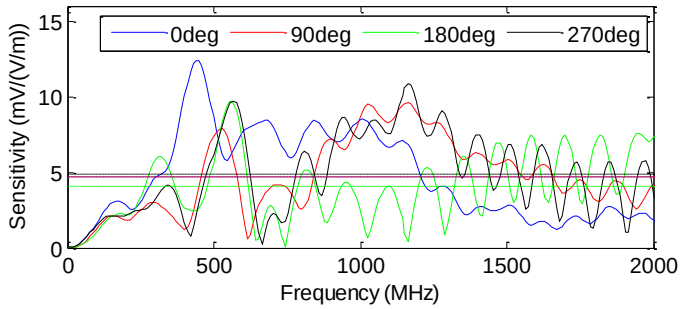


Figure 27 - Orientations of TEV in variation two viewed from GTEM emitter

The response of the TEV to an electromagnetic field inside the GTEM cell for variation one are shown in Figure 28 for the frequency range 0-2000 MHz.



(a)



(b)

Figure 28 - Sensitivity over the frequency range of interest for the TEV: (a) HVPD TEV for variation one and (b) HVPD TEV for variation two (dashed line detailing averaged values)

The results for variation one was similar as the sensor was simply rotated and no major change was observed in sensor response. The sensitivity of the TEV in variation two is significantly lower than in variation one. Variation one should have the highest sensitivity as the TEV is installed using the magnetic face on enclosures to monitor PD emission – the working face of the sensor is exposed during this variation. Thus the shielding included in the sensor design is acting to reduce the effect of an external electromagnetic field on the sensor.

2.5.3. Summary of Immunity Testing Results

The results for the interference testing on the HFCTs are summarised in this section. The results for variation one are summarised in Table V.

The 100/50 HFCT with the HDPE casing was the sensor which was most affected by the exposure to the electromagnetic field through the cross section of the HFCT inside the GTEM cell. The sensor which was least sensitive to the incident electromagnetic field was the 100/50 ALU HFCT. There was no particular orientation identified which yielded a high response to the incident electromagnetic field.

Table V - Summarised table of results for variation one (electric field through cross section of the HFCT)

Casing material	Sensor name	Average sensitivity (mV/(V/m)) over the frequency range at each angle				Mean sensitivity (mV/(V/m))
		0 deg	90 deg	180 deg	270 deg	
HDPE	75/35	**3.81**	2.43	2.87	2.46	2.89
	100/50	6.79	6.48	**8.19**	6.4	6.97
	140/100	4.21	3.78	**5.22**	5.02	4.56
Aluminium	100/50ALU	0.16	0.10	0.14	**0.35**	0.19
	140/100HC	0.36	**0.58**	0.26	**0.58**	0.45

The results for variation two are summarised in Table VI for the four orientations of the five HFCTs.

Table VI - Summarised table of results for variation two (electric field passing through centre of the HFCT)

Casing material	Sensor name	Average sensitivity (mV/(V/m)) over the frequency range at each angle				Mean sensitivity (mV/(V/m))
		Edwn_CF	Edwn_CR	Eup_CF	Eup_CR	
HDPE	75/35	3.08	2.82	**3.28**	2.24	2.86
	100/50	4.57	3.88	**5.17**	2.75	4.09
	140/100	3.61	4.11	**6.3**	4.04	4.52
Aluminium	100/50 ALU	0.27	0.28	**1.2**	0.24	0.5
	140/100 HC	0.38	**0.98**	0.46	0.37	0.55

The sensor which had the highest sensitivity to the electromagnetic field generated inside the GTEM cell for variation two was 140/100 HFCT with HDPE casing. The sensor which was least sensitive to the electromagnetic field generated inside the

GTEM cell was the 100/50 ALU sensor. In general, highest sensitivity to the electromagnetic field for all the sensors was when the each earth label was placed upwards and the BNC connection was pointing forward (EUCF orientation). The sensor with the largest transfer impedance (most sensitive) was one of the least sensitive to the electromagnetic field generated inside the GTEM cell. Similar to variation one the two sensors with aluminium casings were least sensitive to the electromagnetic field generated inside the GTEM cell for variation two.

The mean response of the aluminium casing HFCTs was higher in variation two and in contrast the mean response of the HFCTs with HDPE casings was higher in variation one. The largest change in sensitivity to electromagnetic field for the two variations was observed for the 100/50 ALU HFCT. The mean sensitivity in variation two was 163.16 % higher than that recorded in variation one. The sensitivity of the 100/50 HFCT with the HDPE casing was 70.4 % higher in variation one than variation two.

The inclusion of a length of EPR insulated 11 kV Prysimian cable during immunity testing was investigated for the 100/50 HFCTs with HDPE and aluminium casings. The results with and without the cable sample for variation one (electric field passing through the cross section of the HFCT) are summarised in Table VII.

Table VII - Summarised table of results for variation one comparing inclusion of a section of cable

Casing material	**Sensor name**	**Cable section**	**Average sensitivity (mV/(V/m)) over the frequency range at each angle**				**Mean sensitivity (mV/(V/m))**
			0 deg	**90 deg**	**180 deg**	**270 deg**	
HDPE	**100/50**	No	6.79	6.48	**8.19**	6.4	6.97
HDPE	**100/50**	Yes	**7.92**	3.89	5.61	6.76	6.05
Aluminium	**100/50ALU**	No	0.16	0.10	0.14	**0.35**	0.19
Aluminium	**100/50ALU**	Yes	0.53	0.27	0.26	**0.98**	0.51

The sensitivity recorded for the HFCT with the HDPE casing was on average, for the four orientations in variation one, 15.2 % higher without the cable sample inside the HFCT. In contrast, the sensitivity of the HFCT with the Aluminium casing was on average 168.4 % higher when the cable section was inside the HFCT. The proximity of the cable section to the HFCT has affected the sensitivity of the HFCT with the aluminium casing.

The same test was conducted for variation two (electric field passing through the centre of the HFCT) using the same two 100/50 HFCTs with different casings. The comparison between the sensitivity results with and without the cable section is summarised in Table VIII.

Table VIII - Summarised table of results for variation two comparing inclusion of a section of cable

Casing material	Sensor name	Cable section	Average sensitivity (mV/(V/m)) over the frequency range at each angle				Mean sensitivity (mV/(V/m))
			EDCF	EDCR	EUCF	EUCR	
HDPE	**100/50**	No	4.57	3.88	**5.17**	2.75	4.09
HDPE	**100/50**	Yes	4.6	1.59	3.68	**4.99**	3.72
Aluminium	**100/50ALU**	No	0.27	0.28	**1.2**	0.24	0.5
Aluminium	**100/50ALU**	Yes	**0.85**	0.55	0.77	0.58	0.69

The sensitivity of the 100/50 HFCT with a HDPE casing was 9.9 % higher when there was no cable section included inside the HFCT. The sensitivity of the 100/50 HFCT with an aluminium casing was 38 % higher when the cable section was included inside the HFCT. The 100/50 ALU sensor is still the least sensitive to the electromagnetic field but the inclusion of the cable section has affected the electromagnetic field response in variation one and two.

The summary of the average sensitivity for the HVPD TEV sensor when exposed to the electromagnetic field inside the GTEM cell are detailed in Table IX.

In variation one the PD detecting face was exposed inside the GTEM cell. The highest average sensitivity of all the sensors tested was recorded consistently for the four orientations in variation one. In variation two, the TEV was installed on the

inside of the GTEM cell with the sensing face against the hatch. Thus the back face of the sensor was exposed to the controlled electromagnetic field as it would be in the installed test environment. The sensitivity of the TEV in this variation was lower indicating the screening included within the sensor and was comparable to the plastic casing HFCTs.

Table IX - Summary of TEV sensitivity for the two variations and each orientation

TEV Variation	Average sensitivity (mV/(V/m)) over the frequency range at each angle				Mean sensitivity (mV/(V/m))
	0 deg	90 deg	180 deg	270 deg	
one	10.88	10.01	9.71	10.53	10.28
two	4.72	4.74	4.03	4.89	4.6

2.6. DISCUSSION

A method was presented for the characterisation of HFCTs, this would be required when the sensor does not have a calibration certificate or for routine frequency response testing of the sensor during deployment. The testing was performed in an aluminium enclosure to minimise external noise effects during the characterisation process. The network analyser returned a gain (dB) over the frequency range 0.3 to 80 MHz. Calculations were presented to enable the transfer impedance of the HFCT to be calculated across the frequency range. This method correlated well with the manufacturer's data sheets for the three HFCTs tested in the study.

A method was presented to enable the scaling factor (pC/mV) of the PD sensing element (measuring impedance and a HFCT). The direct output of the calibrator was recorded and this was compared to both the measuring impedance (AC PD measurements) and the HFCT (DC PD measurements). The method found that the scaling factor for the measuring impedance ranged from 1.25-1.56 pC/mV and the scaling factor for the HFCT ranged from 7.94-8.9 pC/mV. Additionally, the 20 and 5 pC pulses could not be recorded using the HFCT in the DC test circuit. This work enabled the measurement range for each sensor to be understood when performing subsequent AC and DC PD tests later in this thesis.

The final application environment for DC PD measurement is a converter station which will be subject to significant uncontrolled electromagnetic fields. A method was presented to allow the immunity testing of a HFCT to be performed using the GTEM cell in the high voltage lab at Strathclyde University. A controlled electric field is generated between the septum (conductor) and the cell wall whilst a step pulse was injected at the emitter of the test cell. The magnitude of the electric field at the test hatch of the GTEM cell was 35 V/m. Based on available literature this is representative of the field emission from modern thyristor (31.63 V/m) and VSC converter stations (20 V/m). The sensitivity (mV/(V/m)) of the sensor to the controlled electromagnetic field was calculated using software developed for the calibration of UHF sensors. UHF sensors are used to detect incident electric fields thus this application uses the GTEM cell as a tool to apply controlled electromagnetic fields to a HFCT (a sensor which detects PD using the magnetic field generated by a current carrying conductor). The method allows an understanding of sensor response to be understood when exposed to a controlled electromagnetic field.

The electromagnetic field response of the sensors was tested for two variations to determine if a particular variation of the sensor to an electromagnetic field was a potential issue:

- In the first variation the electric field passed through the cross section of the HFCT (variation one)
- In the second variation the electric field passed through the centre of the HFCT (variation two).

Four different orientations were applied to each variation to assess if any effect was apparent by aligning the sensor a particular way. When the electric field was passing through the centre of the HFCT (variation two) the average sensitivity over the frequency range was higher for three of the five HFCTs tested. In comparison, the sensitivity was lower when the electric field was passing through the cross section of the HFCT (variation one). The HFCTs which had aluminium casings had a lower sensitivity to the applied electromagnetic field in the GTEM cell for both variations. The aluminium enclosure acted to shield the ferrite core and windings inside the casing from the induced electromagnetic field inside the GTEM cell. The expectation is that for particular orientations the magnetic flux will couple with more of the windings than in other orientations. There is also an expectation that at UHF

frequencies the ferrite core cannot respond fast enough thus becomes a loosely would coil on a ferrite core. With the coil of wire now being significant compared to the signal wavelength at UHF, transmission line effects and capacitive coupling will come into play. The windings may act as an antenna and couple with the electric field in a complex way. The main recommendation from these observations would be to use HFCTs with aluminium casings and take care to ensure that potential sources of electric field do not align with passing through the centre of the HFCT. Publications to date [51] on the electric field conditions inside the converter hall suggest a clearance distance of 40 m allows a large attenuation of electric field from the converters more than 200 m reduces the electric field experienced significantly.

The interference test method was expanded through the inclusion of a section of 11 kV EPR Prysmian cable inside the centre of the 100/50 HFCTs. Both the HDPE casing and Aluminium casing 100/50 HFCTs were tested with the cable section included in the centre of the HFCT. The inclusion of a cable section inside the 100/50 HFCT with a HDPE casing reduced the sensitivity. However, the sensitivity of the 100/50 HFCT with HDPE casing was 15.2% higher in variation one. In variation two the sensitivity was 9.9 % higher when no cable section was inside the HFCT. In contrast, when the cable section was inside the 100/50 ALU HFCT the sensor was more affected by the incident electromagnetic field for both variations. The sensitivity of the 100/50 ALU HFCT was 168.4 % higher in variation one and 38 % higher when a cable section was inside the HFCT compared to no cable inside. The expectation is that the coupling with the electric field will be quite different when the cable section was included in the centre of the HFCTs. The capacitive coupling between the cable section and the HFCT will be quite different for the aluminium casing and the HDPE casings. It may be possible to explain the effects further through detailed modelling of the scenarios.

2.7. CONCLUSIONS

Literature relating to the calibration of magnetic field sensors, calibration of electric field sensors and the electric field emission in converter stations has been presented. A test method for the calibration of magnetic field sensors was adopted in this work based on available literature. A GTEM cell which is used to calibrate electric field sensors was employed to understand the response of magnetic field sensors when exposed to a controlled electromagnetic field. The electric field generated in the GTEM cell was compared to findings reported in available literature

for the main converter topologies. The objective of this work was to understand the impact on magnetic field sensors exposed to controlled electromagnetic fields. The main application of this knowledge is on the design of magnetic field sensors or the deployment of sensors inside HVDC converter stations or environment with electromagnetic field effects.

An existing method for the characterisation of HFCTs was adopted based on the work of Xiao Hu *et al.* [42] and was used to confirm the transfer function of the HFCTs under test. The scaling factor of the PD measurement sensors was determined for the measuring impedance in the AC test circuit and the HFCT employed for DC PD measurements in this thesis. The understanding of sensor performance is key to ensure confidence in the measurement equipment and test setup for all future work in this thesis.

A method was derived to enable magnetic field sensors to be exposed to controlled electromagnetic fields using a GTEM cell, generally employed to characterise electric field sensors. The understanding of sensor response to external electromagnetic field effects from converters is an important consideration when measuring PD activity in a HVDC system. Such a method will allow sensor designs to be refined to ensure the rejection of a specific frequency range of electromagnetic fields and consideration of suppression techniques. A range of HFCTs and a TEV were tested to determine the immunity of the sensors when exposed to a controlled electromagnetic field. The HFCT least sensitive to the incident electromagnetic field had an aluminium casing and internal shielding was particularly effective. The adoption of such sensors would be recommended over HFCTs with plastic casings which feature reduced shielding for the ferrite core and windings.

An additional area of interest was the variation in orientation of the magnetic field sensors to the incident electric field. Generally, the HFCTs were more sensitive to the incident electric field when the electric field passed through the centre of the HFCT. The refinement of PD sensors for high electromagnetic field environments could be further developed using this method. The inclusion of cable sections inside the HFCT was explored to get an initial understanding of the effect of the sensor installation. The aim was to explore the positioning of PD measurement equipment in a converter hall and the relative orientation of sensors. This range of testing could inform best practices for the location of PD sensors in a converter hall and the final orientation of the sensors when being finally located.

In terms of future work, it would be interesting to explore:

- Possible mitigation techniques for the shielding of the HFCT from the electromagnetic effects. The main area for development is in considering alternative casing materials (highly conductive materials or alloys with extremely high permeability) to improve the immunity of the sensor to the electromagnetic fields of the final application environment.
- The method presented could be employed to allow the sensor design to be tuned to reject the electromagnetic field environment.
- The relationship between the electric field typically seen in the converter station to that exposed inside the GTEM cell could be further explored particularly for VSC converter stations where there are limited publications. The incident electric field at the test hatch of the GTEM cell was 35 V/m. The reported electric fields inside converter stations are highly dependent on the converter topology: 1.8 KV/m (mercury valve hall), 31.63 V/m (thyristor valve hall) and 20 V/m (VSC MMC converter hall).
- The inclusion of different types of cable inside the HFCT during exposure to electromagnetic fields to see how the sensor response to an electromagnetic field would be altered (only EPR was considered). This would entail trialling different installation options and determining the best practice for installing HFCTs in a converter station.
- The best practice for sensor installation could be expanded to include the orientation of the sensor as well as the relative position in the converter hall without compromising the PD measurement process.

3. AC AND DC PD TESTING OF DIELECTRIC SAMPLES

This section details the background information and literature related to the testing of dielectric samples. AC and DC test methods are presented for testing dielectric samples in a lab environment. These test methods will be used throughout this thesis. The generic dielectric samples represent different possible sources of PD within a HVDC system. The results from DC PD testing is presented and conclusions drawn for further DC PD analysis. The recommended analysis methods from IEC 60270 [3], methods from available literature and some alternative analysis approaches were applied to the PD data from the dielectric samples. The main focus of this chapter is to identify lenses that can be applied to DC PD data to differentiate and understand what PD is apparent in a HVDC system. The DC PD data recorded in this work is based on the time of occurrence and PD magnitude calculated by an IEC standard PD measurement system.

3.1. ASSOCIATED LITERATURE

The behaviour of common insulation defects was the main area of consideration in this chapter. The publication by Mizzanti *et al.* provides the fundamental background information for the behaviour of HVDC insulation [58]. Recent guidelines [36] detail best working practices for the testing and diagnosis of faults in polymeric materials for HVDC insulation systems from design to final implementation. One approach to monitor the condition of the insulation of an electrical system is through the monitoring of PD.

PD detection under AC conditions is a well-established tool for insulation monitoring. In AC equipment, a number of different PD detection techniques are available dependent on the particular application. Even under AC conditions, PD remains a complex phenomenon that still poses challenges for measurement and diagnosis. In comparison, PD detection under DC conditions has received less research attention until recently. A useful introduction to work on PD in HVDC insulation can be found in [17] More recent publications on PD detection under HVDC conditions are available in [25], [26], [28].

This work aims to further the understanding of PD behaviour in dielectric samples under DC conditions by comparing their AC and DC PD characteristics. Identifying the type of PD apparent in an HVDC system will be an important factor for

diagnosing defects. In the measurements presented in this chapter, PD pulses under DC conditions were characterized by their magnitude and time of occurrence and a number of classification techniques are explored. The analysis of PD from different types of defect under AC conditions has received more attention to date [31], [59], [60]. Under DC conditions the same detection equipment can be used but the diagnosis of PD activity is less well defined. The main methods applied have been based on the statistical analysis of PD pulses [21], [27], [61]. Section 11 of IEC 60270 [3] includes four methods of presenting statistical results, which were utilized for analysis in this chapter.

The sample under test in this work has five parallel voids, research to date [62] has shown that the electric fields of multiple voids, in close proximity, are affected by one another [63]. Voids in parallel (arranged horizontally) were found to have a lower inception voltage than voids in series (arranged vertically) [62]. Similarly, parallel voids were found to produce PD events of larger magnitude than serial voids [62]. One effect recorded was the rise in apparent charge produced during detected PD events in samples with adjacent voids.

The two common methods used in the analysis of PD under AC conditions are:

- Phase resolved PD (PRPD) plots
- Pulse sequence analysis (PSA)

PRPD analysis is used in this work to confirm the PD behaviour of the dielectric samples. Two key parameters of the PD events are required to produce a PRPD plot; the charge contained in the PD current pulse and a phase reference to the HVAC sine wave. The phase location and relative spread of the PD activity is used for the identification of different defect types [64]. Pulse sequence analysis considers the relationship between a series of PD events. The sequence of PD events has been shown to be affected by the characteristics of a particular scenario under study [65]. Previous PD events have been shown to affect future PD events due to the influence of space charge [66].

In contrast, under DC conditions PD generally occurs less frequently and is more likely to occur during voltage changes [17]. The parameters available in the analysis of PD under DC excitation are the apparent charge and its time of occurrence. The analysis of these parameters is best suited to statistical techniques. Statistical analysis has been adopted to demonstrate that different sources of PD can be

distinguished. This study applies the statistical analysis techniques proposed in IEC 60270 [67] to demonstrate the PD behaviour of common defects under HVDC conditions. Other recommended techniques are explored with focus on the measured quantities of charge magnitude and time of occurrence.

3.2. THEORY

Fundamental differences exist in the mechanisms that drive PD at AC and DC applied voltages. While AC PD phenomena are well understood through lab and field experience, more research is needed into diagnostic interpretation of the phenomena under DC conditions.

3.2.1. AC PD

PD activity under AC conditions can be modelled by using capacitors to represent the bulk properties of the insulation system. A common model used to represent AC PD resulting from a void in a solid dielectric is the three capacitor model [17]. The gas filled void (Figure 29) is represented by C_c, the insulation in series with the void is represented by C_b and the remaining insulation is represented by C_a. Under AC conditions the voltage polarity reverses every half cycle. When the electric field in the cavity exceeds the PD inception level, a PD will occur. As the capacitance of the void discharges, the voltage across the void drops. The reliance of PD activity on the applied voltage leads to a phase-synchronization of PD activity under AC conditions. Under AC conditions the field enhancement is dictated by the relative permittivity and the shape of the void defect [68]

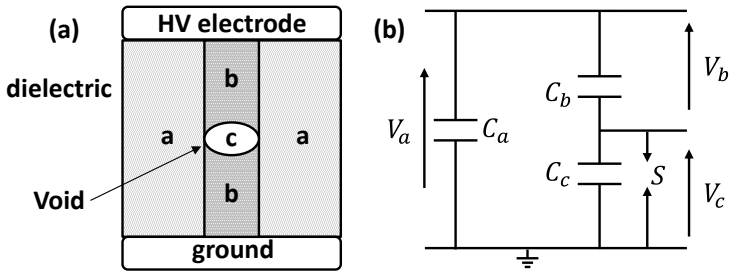


Figure 29 - (a) Illustration of void type defect indicating which sections of insulation correspond to which capacitances and spark gap (*S*). (b) Three capacitor model for AC PD.

3.2.1.DC PD

Under DC conditions the voltage is generally constant thus the three-capacitor model would reach steady-state and activity would cease. The DC PD model requires adaptation (Figure 30) of the AC model to reflect the charge dissipation from the void defect into the surrounding dielectric [17]. This is achieved through the addition of resistors in parallel with each capacitor. Under DC conditions the repetition rate of PD is dependent on the applied voltage magnitude and the conductivity of the insulation surrounding the void.

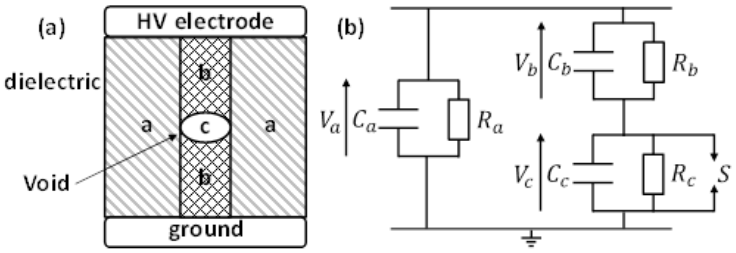


Figure 30 - (a) Illustration of void type defect indicating which sections of insulation correspond to which capacitances, resistances and spark gap (*S*) (b) Three capacitor model adapted for DC PD.

In contrast to AC, PD under DC conditions has no phase reference thus characterization must be based upon correlating PD magnitude with other quantities such as time of occurrence or time-difference between consecutive pulses. At DC, discharges take place in the manner of a relaxation oscillator, where the field in the cavity is built up through charging of the capacitive defect through the leakage resistance of the dielectric, with amplitude and rate of discharge being in proportion to the magnitude of the applied voltage. Under DC conditions the conductivity of the insulation and the shape of the void determine the field enhancement.

3.3. TEST METHODS

The adopted test methods under AC and DC conditions are discussed in the following subsections.

3.3.1. AC TEST METHOD

This sub-section discusses the method applied to determine the inception voltage of sustained PD activity from dielectric samples whilst under AC excitation. A further goal of the AC tests was to confirm the dominant source of PD from the three dielectric samples under test.

AC tests were performed using the calibrated IEC60270 standard measurement system shown in Figure 31. The test circuit is comprised of:

- AC test set
- A 100 kV transformer
- The sample under test (represented by the capacitance C_t)
- A coupling capacitor (C_k)
- Measuring impedance (Z_m).
- The IEC 60270 measurement system (bandwidth was 100 – 400 kHz) which also controls the AC test set

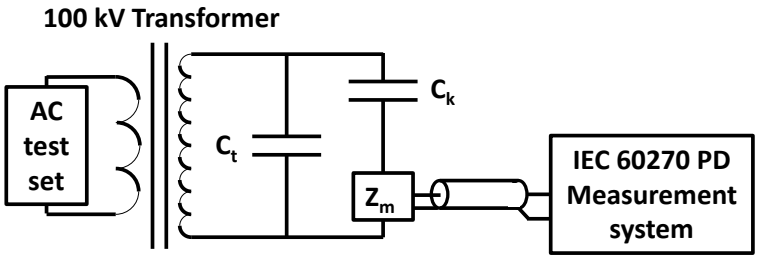


Figure 31 - AC test circuit.

The AC tests were performed by incrementally increasing the voltage of the AC supply until sustained PD was apparent from the sample under test. The inception voltage was deemed to be the voltage at which repetitive and sustained PD was observed on the IEC standard measurement system [64]. PD activity at the inception voltage was then recorded over a 10 second period in phase-resolved format by the IEC 60270 measurement system. These AC tests served to confirm the dominant source of PD for each of the dielectric samples.

3.3.2.DC TEST METHOD

The aim of the DC test method is to determine the DC voltage at which sustained PD was observed. The test circuit illustrated in Figure 32 includes:

- The AC test set
- single phase 100/0.38 kV transformer
- AC coupling capacitor (C_k)
- Diode (D)
- Inductor (L)

- 230:1 resistive divider (R_D)
- Sample under test (C_t)
- DC coupling capacitor (C_s)
- HFCT (Z_{trans}=4.3 Ω)

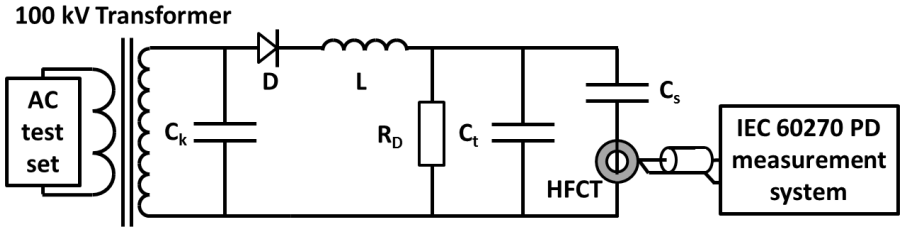


Figure 32 - DC test circuit.

PD pulses were recorded using the same IEC PD measurement system used for the AC tests. The sensor connected to the measurement system was a high frequency current transformer (HFCT) with a nominal transfer impedance of 4.3 Ω and a bandwidth of 100 kHz – 20 MHz. A pulse injection calibration unit was used to ensure the output from the HFCT could be quantified as an apparent charge on the IEC 60270 measurement system.

A key aspect of the DC testing is the ramp test profile [30], [69]. The ramp test uses the peak value V_R of the AC inception voltage as a basis for defining the voltage variation with respect to time. The ramp test consists of three voltage increments (as shown in Figure 33) after which the voltage is held constant at $V_R/2$, V_R and $3V_R/2$ for 30 minutes each, followed by a final ramp down period ($3V_R/2$ to 0 V) occurring within 30 seconds. The data under analysis in this work is the 30 minute hold data at each of the 3 voltage steps.

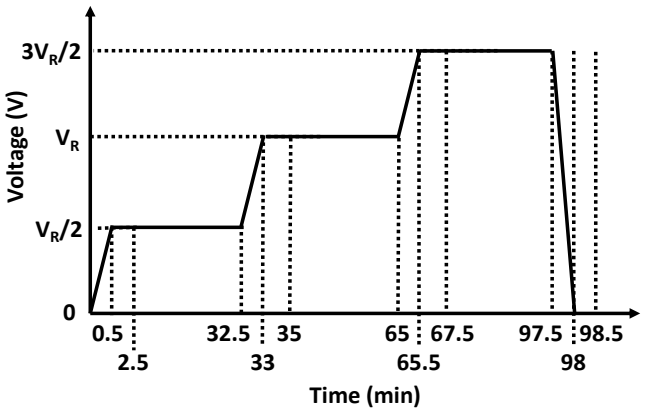


Figure 33 - The ramp test profile for DC testing.

The use of the ramp test method allows defined and repeatable DC PD tests to be performed on the dielectric sample under test. A number of analysis techniques will be applied to the DC PD data for the dielectric samples under test.

3.4. SAMPLES UNDER TEST

The dielectric samples under test in this chapter are detailed in this section. The samples were chosen to represent the common PD mechanisms observed in HVDC insulation systems.

Samples were selected to produce different types of PD that might occur in an HVDC insulation system. The three samples are as follows:

- **'Five void sample'**: consisted of five voids (Figure 34(a)) in an epoxy resin disc with two brass plane electrodes fixed to its upper and lower faces. The diameters of the voids were 0.59, 0.46, 0.43, 0.32 and 0.21 mm. This sample was chosen to represent internal PD activity. This sample was inherited from previous studies conducted at Glasgow Caledonian University. The sample contains five voids but the discharges observed are likely to be from the largest voids.
- **'Metallic protrusion sample'**: consisted of a point-plane test cell in air (Figure 34(b)). The sample was unconventional due to the large diameter of the rod used to make the point. The steel rod was 3 mm in diameter with a point formed at a 90° angle. The brass plane was 50 mm in diameter and the separation between the point and plane was 10 mm. This sample was

chosen to ensure PD occurred from this metallic type protrusion defect at voltages within the range of the DC power supply.

- **'Ceramic bushing sample'**: formed using a ceramic bushing from an 11 kV transformer (Figure 34(c)). A brass high voltage terminal was attached to the top of the insulator and a braided wire was wrapped round the bushing. This sample was constructed to stimulate surface discharge across the ceramic insulator.

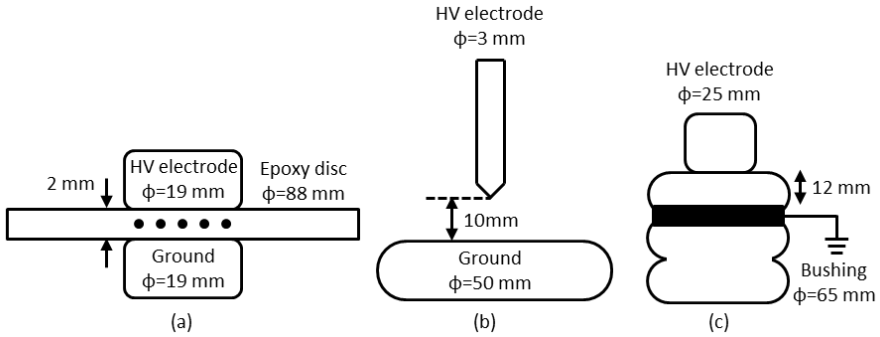


Figure 34 - The dielectric samples used in this chapter. (a) Five void (b) Metallic protrusion (c) Ceramic bushing.

3.5. RESULTS

The results from AC and DC testing will be discussed in the following sections for the three samples described above. The relative humidity is presented in each test and is based on measurements at Glasgow airport [70] with the error to the high voltage lab being ±1%.

3.5.1. AC TEST RESULTS

The results from AC testing on the dielectric samples are detailed in this sub section. The main purpose of the AC testing was to determine the AC inception voltage and to confirm the dominant PD type in each dielectric sample.

The five void sample had an inception voltage of 8 kV rms, the IEC PD level at this voltage was 680 pC. The measurement system calculates the IEC PD level using a method from IEC 60270 standard [3]. The relative humidity during this test was 76% [70]. This was a high PD level for a void sample but this sample included five voids so a larger PD magnitude was expected with the five voids being in parallel [62]. The PRPD plot for the five void sample at 8 kV is shown in Figure 35. The

discharges generally occur in advance of the test voltage peaks PRPD plots displaying this trend are typical of internal discharge.

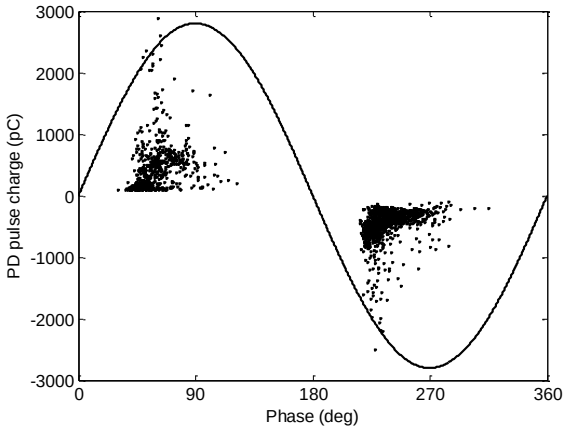


Figure 35 - PRPD plot for the five void sample at 8 kV.

The metallic protrusion sample had an inception voltage of 5.8 kV rms the IEC PD level at this voltage was 4.8 nC. The relative humidity during this test was 86% [70]. The PRPD plot for the metallic protrusion sample at 5.8 kV is detailed in Figure 36. The metallic protrusion sample produced no PD at 5.6 kV, with PD activity immediately apparent at 5.8 kV. The PRPD plot shows that the majority of PD activity occurs at a phase of 90 degrees, this matched expected behaviour from a metallic type protrusion defect. The PD on the negative half cycle was below the detection threshold of 751 pC.

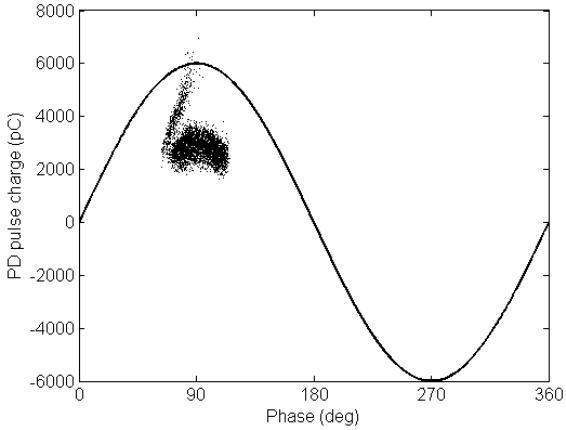


Figure 36 - The PRPD plot for the metallic protrusion sample at 5.8 kV.

The ceramic bushing sample had an inception voltage of 4.7 kV rms, the IEC PD level at this voltage was 3.5 pC. The relative humidity during this test was 86% [70]. When the voltage was increased to 7.3 kV the IEC PD level was 618 pC. The PRPD plot for the ceramic bushing at 4.7 kV is shown in Figure 37. PD activity occurs predominantly before the AC voltage peaks. The PRPD plot also shows a larger number of smaller discharges in the negative half cycle and a smaller number of larger discharges in the positive half cycle. A PRPD plot of this nature is typical of surface discharge [64].

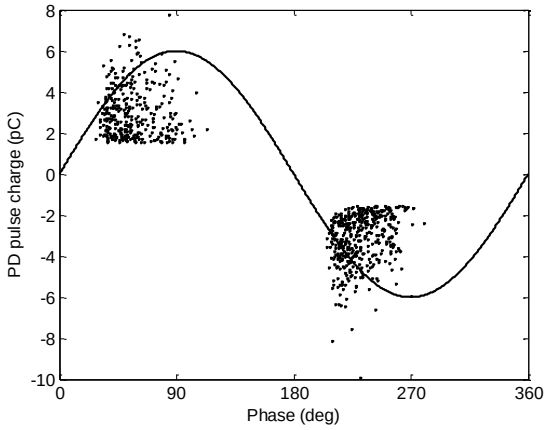


Figure 37 - The PRPD plot for the ceramic bushing sample at 4.7 kV.

There was a relative difference between the PD magnitudes from the three dielectric samples. In all samples the supply voltage was incrementally increased by 0.1 kV until repetitive and sustained PD was observed.

3.5.2.DC TEST RESULTS

The DC test results will be discussed in this section. The first sub section details the application of suggested methods from IEC 60270 [3]. The further sections investigate the application methods proposed by literature [17] with focus placed on the charge of the PD events, the time between PD events and the sequence of PD events. The analysis of charge magnitude and time between PD events will be explored in detail. Statistical analysis techniques will be applied to the PD data sets and the findings will be reported.

3.5.2.1. Application of methods suggested in IEC 60270

IEC 60270 [3] recommends two methods for evaluating PD test data:

- Firstly, the pattern of consecutive charge pulses for a PD test period of 30 minutes at constant DC test level.
- Secondly, the cumulative PD pulse charge recorded over the 30 minutes PD test period.

Two further methods were recommended for performing statistical analysis on the PD data:

- Firstly, the number of pulses whose apparent charge exceeds a specified threshold level for the PD data under test - this was termed exceeding frequencies of PD pulses.
- The second analysis method details the total number of PD pulses whose charge lies within a defined set of ranges of PD magnitude for the PD data under test - this was termed class frequencies of PD pulses. These methods were applied to the PD data gathered during the 30 minute hold at $3V_R/2$.

The dielectric samples have been shown to exhibit the expected PD behaviour under AC conditions. DC testing will be performed on these dielectric samples with known defects. The results from testing the same samples under DC conditions are presented using the suggestions in IEC 60270 for analyzing PD under DC conditions. The PD data under analysis was gathered at the highest test voltage ($3V_R/2$), during which PD pulses were measured over 30 minutes to allow statistical analysis. In some cases the maximum hold DC voltage had to be modified based on the level of observed PD activity.

The AC inception voltage for the five void sample was 8 kV rms, giving a peak voltage of V_R=11.3 kV this was used to derive three hold voltages (5.6 kV, 11.3 kV and 17 kV) for the ramp testing on this sample. The voltage was ramped up to $3V_R/2$ (17 kV) but following the 2 minute wait period (which is necessary to ensure any that PD activity detected is not caused by the recent voltage change), only limited PD activity was detected. The voltage was increased to 20 kV where 36 PD events were recorded. The relative humidity during this test was 79% [70]. The plot in Figure 38 (a) shows the pulses detected from the sample whilst the voltage was held at 20 kV for 30 minutes. The plot in Figure 38 (b) shows the accumulated PD charge over the measuring period. Figure 38 (c) illustrates the exceeding frequencies of PD pulses. Figure 38 (d) shows the class frequencies of PD pulses.

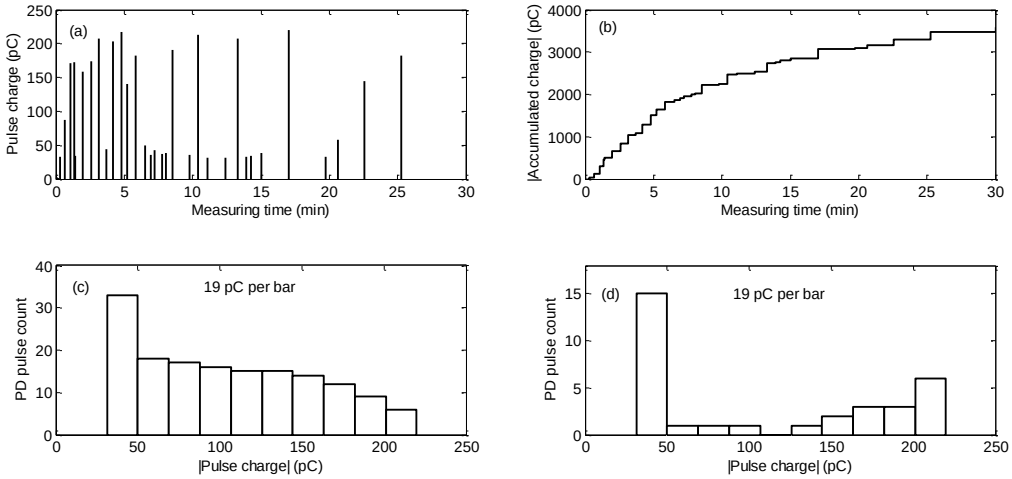


Figure 38 - Five void sample. (a) Consecutive charge pulses recorded at 20 kV in 30 mins (b) Accumulated pulse charges recorded over the 30 min test period (c) Exceeding frequencies of PD pulses (d) Class frequencies of PD pulses.

For the metallic protrusion sample a peak voltage V_R=8.2 kV was used to derive the three hold voltages (4.1 kV, 8.2 kV and 12.3 kV) for ramp testing. However, the PD became very active at 10 kV whilst ramping up the voltage from V_R, to avoid a breakdown event the voltage was not increased further. The relative humidity during this test was 89% [70]. Over 340,000 PD pulses were acquired in just 6 mins 40 s. The plot in Figure 39 (a) shows the detected pulses while Figure 39 (b) shows the accumulated PD charge over the measuring period. Figure 39 (c) illustrates the exceeding frequencies of PD pulses. Figure 39 (d) shows the class frequencies of PD pulses.

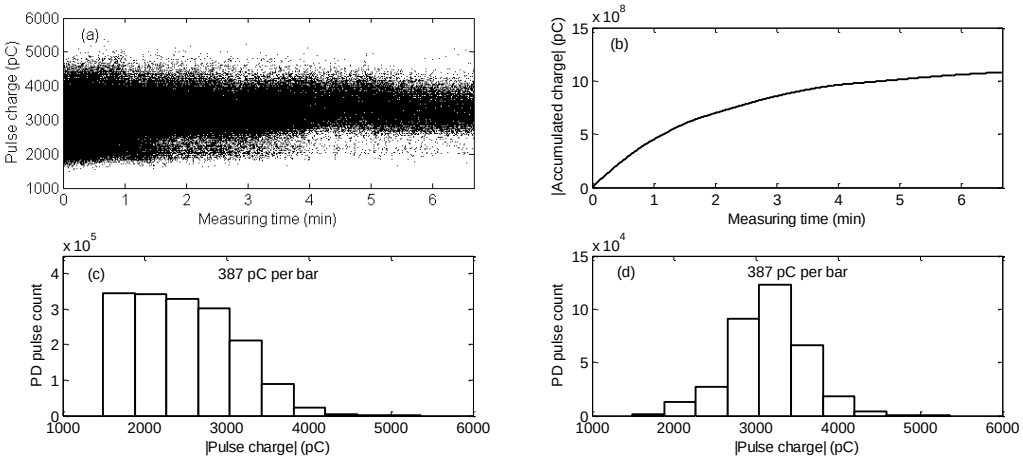


Figure 39 - Metallic protrusion sample. (a) Consecutive charge pulses recorded at 10 kV in 6.67 mins (b) Accumulated pulse charges recorded over the 6.67 min test period (c) Exceeding frequencies of PD pulses (d) Class frequencies of PD pulses.

The AC inception voltage for the ceramic bushing sample was 4.7 kV rms. The peak voltage (V_R=6.6 kV) was used to derive three hold voltages (3.3 kV, 6.6 kV and 10 kV) for the ramp testing on this sample. The voltage was ramped up to $3V_R/2$ (10 kV) following the 2 minute wait 30 minutes of PD data was recorded. The PD was consistent and sustained at $3V_R/2$ and 195 PD events were recorded. The relative humidity during this test was 79% [70]. The first plot in Figure 40 (a) details the pulse charges emitted from the sample whilst the voltage was held at 10 kV for 30 minutes. The second plot, Figure 40 (b), is that of the accumulated charge over the measuring period. Figure 40 (c) illustrates the exceeding frequencies of PD pulses. Figure 40 (d) shows the class frequencies of PD pulses.

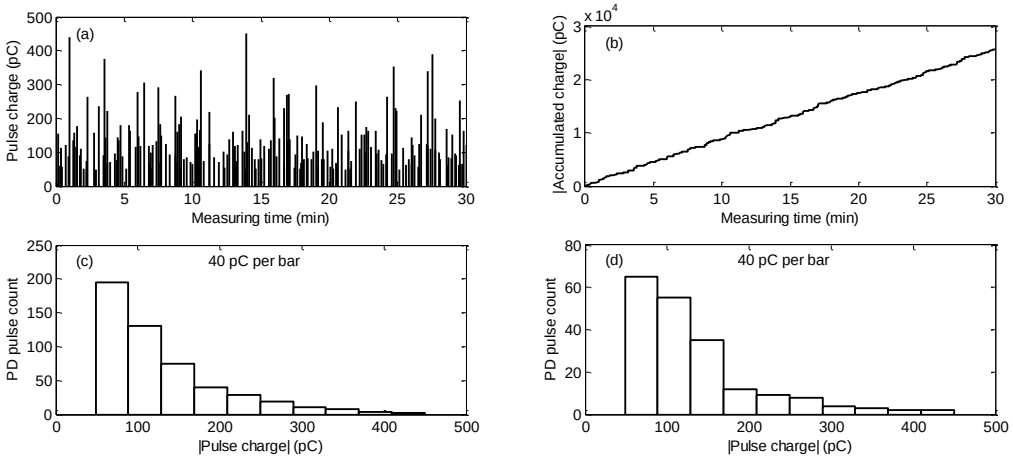


Figure 40 - Ceramic bushing sample. (a) Consecutive charge pulses recorded at 10 kV in 30 mins (b) Accumulated pulse charges recorded over the 30 min test period (c) Exceeding frequencies of PD pulses (d) Class frequencies of PD pulses.

The use of the IEC 60270 recommended methods allows a generic representation of the PD behaviour under DC conditions to be presented. The use of the 4 methods allows differences between PD sources to be apparent.

3.5.2.2. Magnitude of PD events

This section investigates the charge magnitude and difference in charge magnitude of PD events for the dielectric samples. As the charge magnitude of the PD event is a direct measurement, the simplest initial filtering approach is to classify PD activity according to PD magnitude. The methods presented assume that the filtering process has been completed and can be used to confirm the source of PD activity or

to highlight PD activity which has not been classified correctly. Both of these approaches will be discussed below.

The relation between discharge magnitude and average magnitude of its successor/predecessor was investigated [17]. This method takes into account the behaviour of discharges succeeding the pulses of a certain charge magnitude. The calculation centres on determining the average charge of successive pulses (q_{suc}) where the charge magnitude is within a certain range (e.g 1-2 pC). In this analysis the charge magnitude data was split into 10 charge magnitude bins and the average value of q_{suc} was calculated for each particular bin. Figure 41 details the charge magnitude versus average q_{suc} for the three dielectric samples.

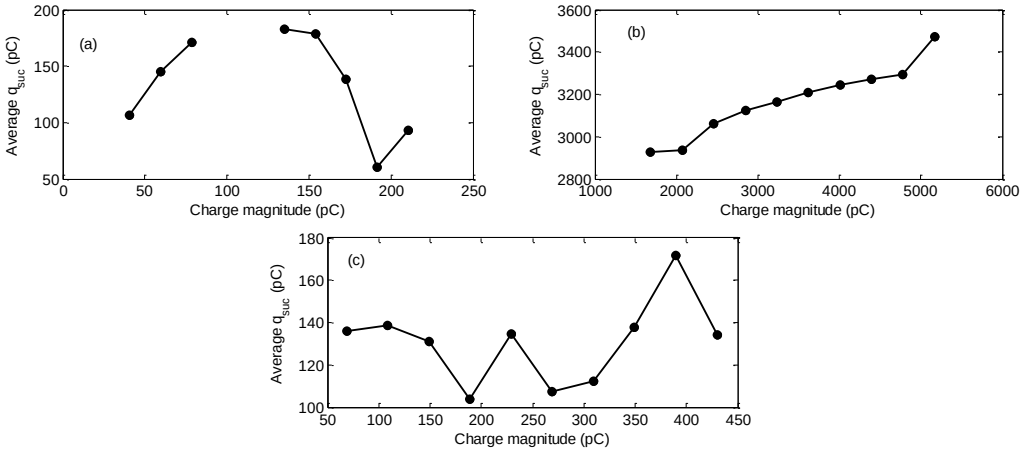


Figure 41 - Charge magnitude vs average magnitude of its successor (a) five void (b) metallic protrusion and (c) ceramic bushing

The range of average magnitude for q_{suc} was similar for the void sample (60.37-182.5 pC) and the bushing (103.6-171.7 pC). In contrast, the average q_{suc} for the metallic protrusion was significantly higher than the other two samples (2926-3471 pC). In literature [17] it was found that the average value of q_{suc} was independent of charge magnitude for a void type sample. This appears to be correct from the data gathered whilst testing a sample with five voids however the results are based on limited data (Figure 41 (a)). The same should be true for the metal protrusion defect but there appears to be a correlation between charge magnitude and q_{suc} (Figure 41 (b)). A negative correlation was expected between the charge magnitude and the average value of q_{suc} for the ceramic bushing sample. No real correlation was

apparent (Figure 41 (c)) for the surface discharge occurring across the surface of the ceramic bushing sample.

The same method was used to calculate the average magnitude of the predecessor (q_{pre}) for 10 charge magnitude bins. Figure 42 details the charge magnitude versus q_{pre} for the three dielectric samples.

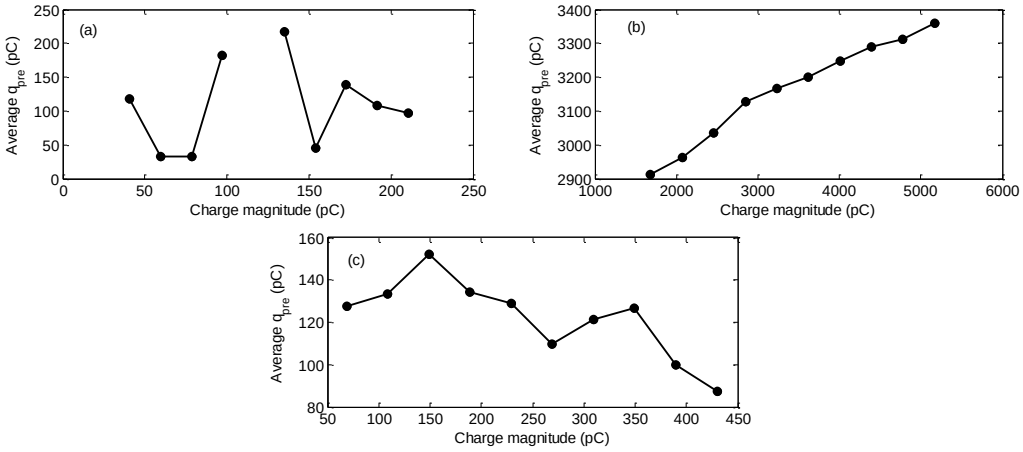


Figure 42 - Charge magnitude vs average magnitude of its predecessor (a) five void (b) metallic protrusion and (c) ceramic bushing

The range of average q_{pre} for the void sample (32.61 to 217.2 pC) was similar to that of the bushing sample (87.21 to 152.1 pC). The range of average q_{pre} for the metallic protrusion (2913 to 3360 pC) was higher than that for the other two dielectric samples but this was reflected in the higher magnitude of PD activity, in general, the metallic protrusion sample has a positive correlation between charge magnitude and the average value of q_{pre} (Figure 42 (b)). There is a negative correlation between the charge magnitude and average q_{pre} for the surface discharge on the ceramic bushing (Figure 42 (c)). The calculation of average q_{suc}/q_{pre} for a range of charge bins offered limited correlation other than for the metallic protrusion sample. The limited amount of PD data for the five void and ceramic bushing samples may be a reason for the lack of correlation.

The behaviour of q_{suc} and q_{pre} versus charge magnitude of the current PD pulse was plotted for the three dielectric samples in Figure 43.

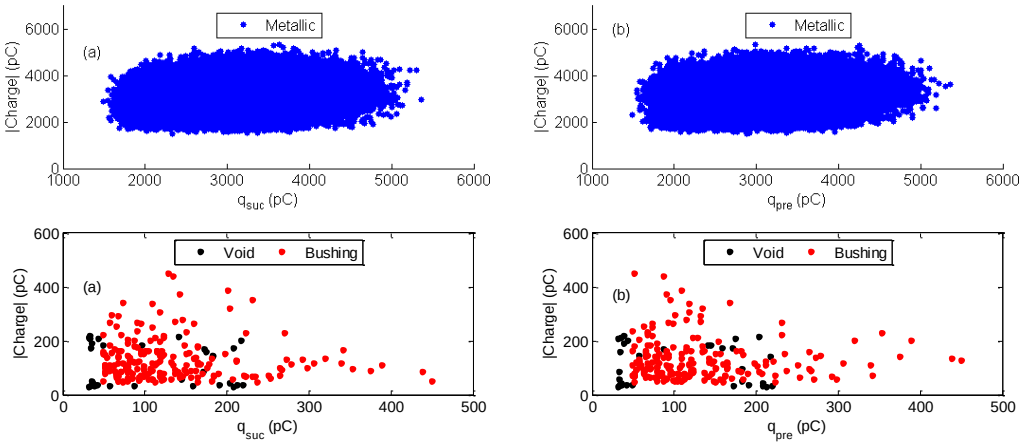


Figure 43 - (a) q_{suc} versus charge magnitude of current PD event (b) q_{pre} versus charge magnitude of current PD event

The relative clustering of q_{suc} and q_{pre} versus charge magnitude was very similar with slight differences when comparing the same dielectric sample. The main differences exist when comparisons were made between the different dielectric samples. In particular, the metallic protrusion sample stands out due to the large amplitude of PD events. The behaviour of the five void and ceramic bushing samples was very similar. This approach allows quick differentiation between internal/surface discharge and the PD evident from a metallic protrusion.

The next phase of analysis (Figure 44) looks at the relative difference between successive (Δq_{suc}) previous (Δq_{pre}) PD events and the magnitude of the current PD event.

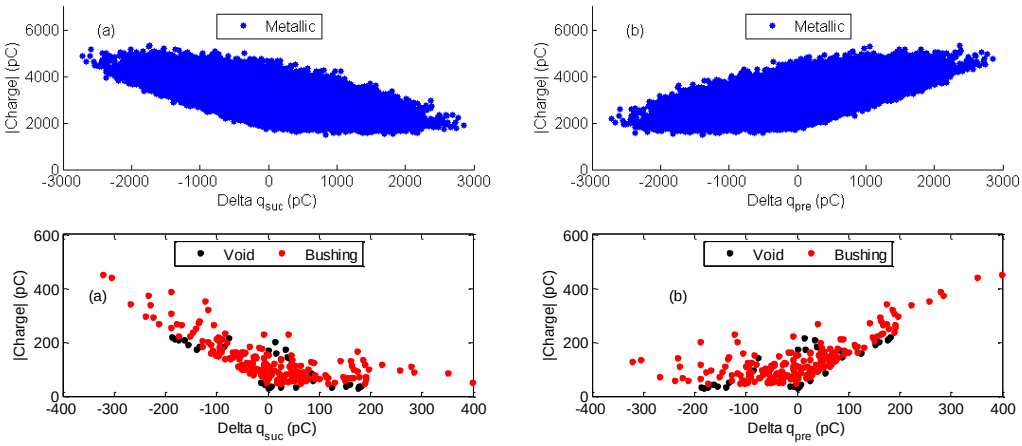


Figure 44 - Difference in charge magnitude versus charge magnitude of current PD event (a) Δq_{suc} versus charge magnitude (b) Δq_{pre} versus charge magnitude

The large magnitude of PD events and relative spread of $\Delta q_{suc}/\Delta q_{pre}$ versus current charge magnitude was highlighted in the plot above. The ceramic bushing and five void samples were closely matched but the relative spread of $\Delta q_{suc}/\Delta q_{pre}$ was wider for the ceramic bushing sample. The main challenge would be trying to differentiate the void and surface discharge if the HVDC system exhibited both. This analysis highlighted the cyclic nature of PD activity and relative variation of PD activity for different sources of PD.

The relative change in charge magnitude of PD between PD events was highlighted by plotting PD event number versus $|\Delta q|$ as shown in Figure 45.

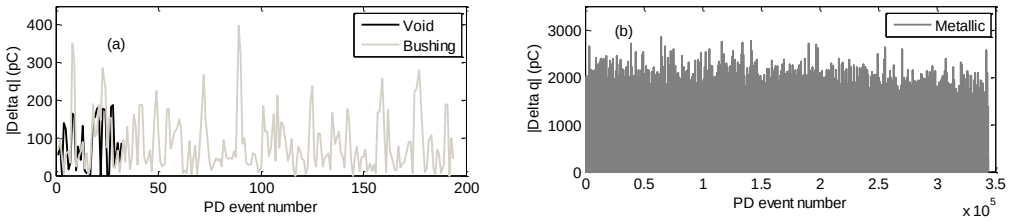


Figure 45 - PD event number versus $|\Delta q|$ (a) five void and ceramic bushing (b) metallic protrusion

The clear differentiation can again be made between the PD activity from the metallic protrusion sample and the five void/ceramic bushing. The variation of $|\Delta q|$ with PD event number for the five void and ceramic bushing samples was very similar and difficult to differentiate. This approach offers limited differentiation between PD sources other than the obvious difference in $|\Delta q|$ between the metallic protrusion and the five void/ceramic bushing samples.

Histograms of $|\Delta q|$ were generated for the three dielectric samples and are shown in Figure 46.

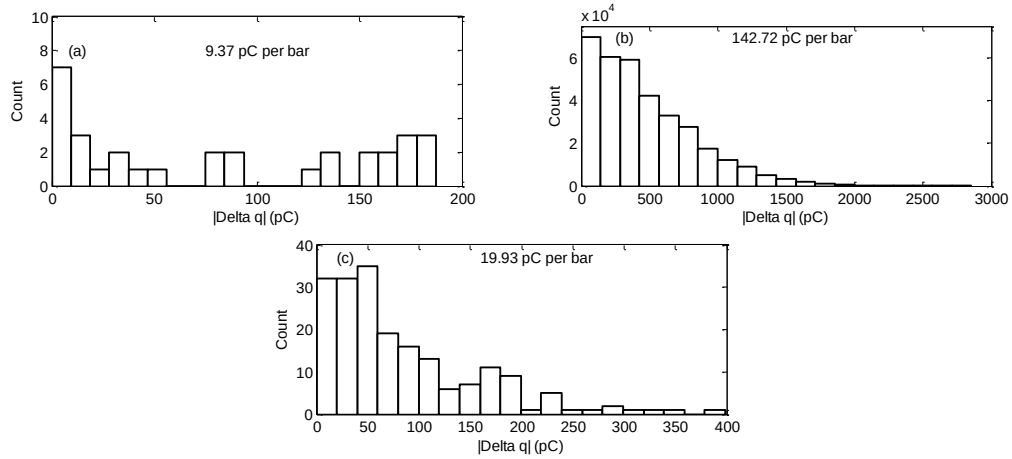


Figure 46 - Δq histograms (a) five void (b) metallic protrusion (c) ceramic bushing

All three histograms of $|\Delta q|$ have characteristic peaks to the left hand side at the lower end of the charge range. The peaks evident for each were; five void (0-9.37 pC), metallic protrusion (0-143 pC) and ceramic bushing (39.9-59.8 pC). The $|\Delta q|$ histograms confirm the difficulty in using $|\Delta q|$ for further analysis. The main challenge would be the differentiation between sources of PD in a HVDC system with all histograms having the majority of data at the left hand side.

3.5.2.3. Time between PD events

This section investigates the time between PD events. If the HVDC system exhibits a number of different PD producing defects initial filtering must be conducted to ensure the time between PD events is from the same source. The best initial filtering method would be to classify the PD activity according to PD magnitude. The use of the methods in this section will allow a further lens to be applied in the analysis to ensure the PD source has been classified correctly. A number of approaches looking at the time between DC PD events were investigated for the dielectric samples. The approaches will be discussed in detail below.

The first method under investigation was the relationship between discharge magnitude and the average time interval to its successor/predecessor for the three dielectric samples. This method has been previously investigated [17]. The discharge magnitudes were binned into 10 data sets where the time to the successor (t_{suc}) was averaged for each data set. Figure 47 details the charge magnitude versus average time to its successor for the three dielectric samples.

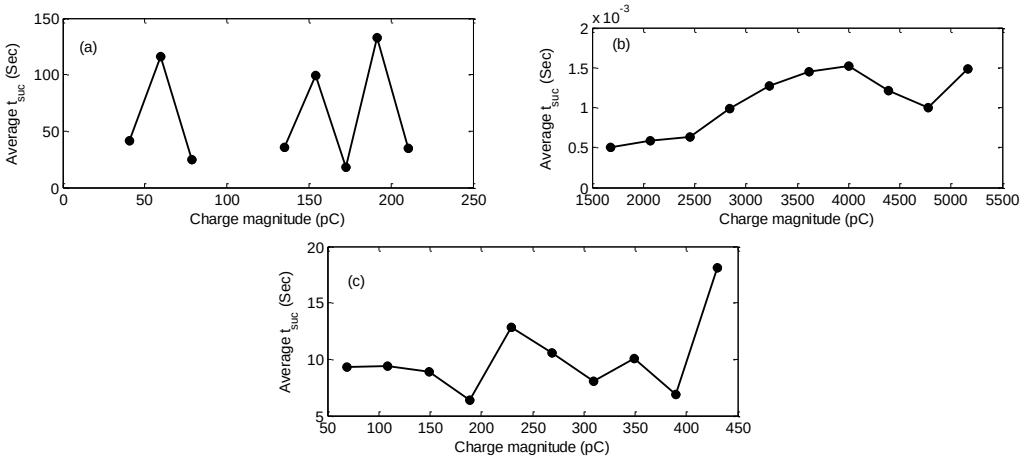


Figure 47 - Charge magnitude vs average t_{suc} (a) five void (b) point plane and (c) ceramic bushing

There was a relatively wide spread of the average t_{suc} for each charge magnitude bin for the five void sample (17.79-133 Sec). The average time to the successive PD event for the ceramic bushing sample had a reduced spread compared to the five void sample (6.39-18.1 Sec) but was larger than the metallic protrusion (0.5-1.52 mSec). The only plot which shows some form of correlation is that of the metallic protrusion (Figure 47 (b)). There was an expectation that the five void sample would exhibit a positive correlation with t_{suc} but this may be complicated by the five void sample containing multiple voids as opposed to a single void in the literature [17]. Also, from literature, the positive correlation only holds for Townsend like discharges and for larger discharges (streamer type) the correlation disappears [17]. The expectation is that as the five void sample is heavily aged the discharges will be more streamer like this may be the cause for lack of correlation in the data. The average time to the predecessor (t_{pre}) (Figure 48) was also calculated for the 10 bins of charge magnitude data.

Similarly, the largest range for t_{pre} was for the five void sample (21.16-283.9 Sec), in the middle was the ceramic bushing sample (3.4-13.15 Sec) and the lowest range was for the metallic protrusion sample (0.134-1.5 mSec). The correlation evident for t_{suc} was not apparent for t_{pre} for the metallic protrusion sample. The lack of DC PD data for the five void and ceramic bushing samples may explain deviation from expected behaviour. The average range of time between PD events (t_{suc} and t_{pre})

would be the most effective way to differentiate dominant sources of PD in a HVDC system.

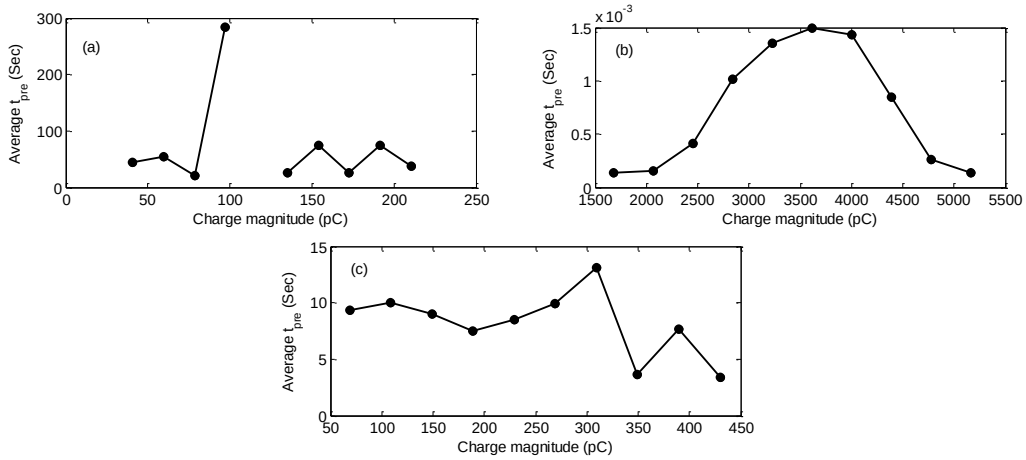


Figure 48 - Charge magnitude vs average t_{pre} (a) five void (b) metallic protrusion and (c) ceramic bushing

The variation of t_{suc} and t_{pre} with charge magnitude of the current event for the three dielectric samples is illustrated in Figure 49.

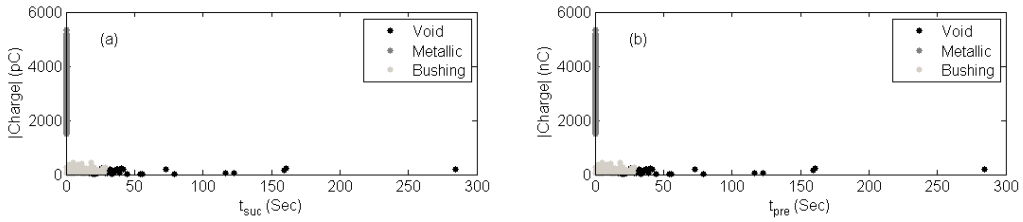


Figure 49 - Comparison of the three dielectric samples (a) t_{suc} versus charge magnitude (b) t_{pre} versus charge magnitude

The behaviour of the metallic protrusion stands out with the relatively large PD events and short time to t_{suc}/t_{pre}. The two plots look very similar due to the small difference in charge magnitude. The behaviour of the five void and ceramic bushing samples was more similar in terms of PD magnitude. The main differentiation between the two samples was the larger time between PD events for the void sample.

The time between PD events (*Δt*) for the dielectric samples was analysed further with *Δt* histograms generated for the data sets (number of bins set to 20) as shown in Figure 50.

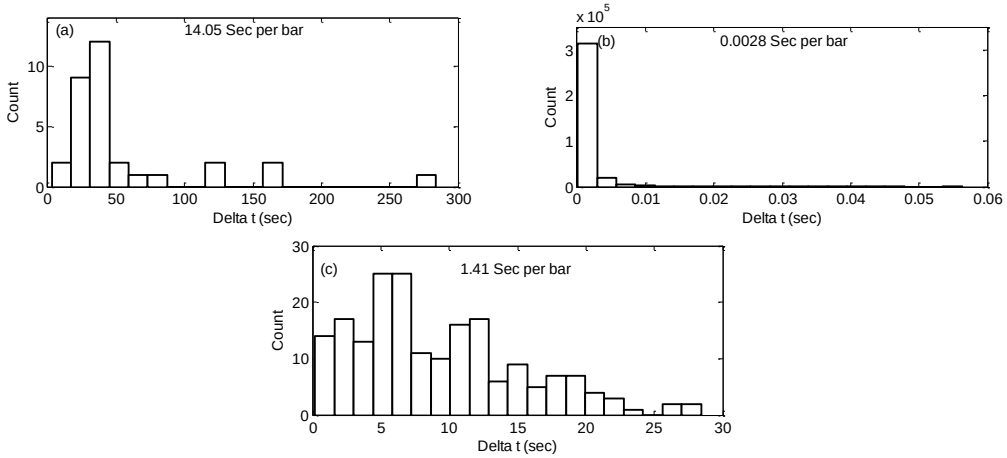


Figure 50 - *Δt* histograms (a) five void sample (b) metallic protrusion and (c) ceramic bushing

The different behaviour of the samples was highlighted in the time difference histograms. In the histogram for the five void sample, the peak *Δt* between PD events was for the bin ranging from 31-45 seconds (lower end of the *Δt* range). 50 % of the time differences for the metallic protrusion sample lie in the bin 0 – 2.91x10^{-3} seconds. The largest count for *Δt* for the ceramic bushing occurs in the two bins ranging from 4.43 to 7.25 Seconds. The peaks and relative ranges of *Δt* between PD events are different for each dielectric sample. This is similar to the histograms of charge magnitude so these sources could be differentiated given the relative spread of *Δt* data.

The behaviour of PD event number versus *Δt* was also investigated to track the relative difference between the dielectric samples. Figure 51 shows the variation of *Δt* with the PD event number for the three dielectric samples.

Δt increases with PD event number for the void sample due to the requirement for the recovery of the voltage across the void (minimum breakdown voltage) and availability of the starting electron inside the void (via a trapped electron or from external sources). The contrast between the consistency of the surface discharge on the ceramic bushing and the behaviour of the five void sample allows a clear differentiation of the PD activity from the two sources. The large number of PD

events and the short time between PD events for the metallic protrusion required the data to be presented on a separate plot. The direct comparison of these variables is more difficult due to the samples at hand and difference in Δt between the samples. The main advantage of this approach is the differentiation between the five void and ceramic bushing samples. An approach to analytically observe this would be to record and trend the relative change of Δt on the HVDC monitoring system. An approach of thresholding Δt to allow categorisation could also be investigated with $\Delta t_{void} > \Delta t_{bushing} > \Delta t_{metallic}$.

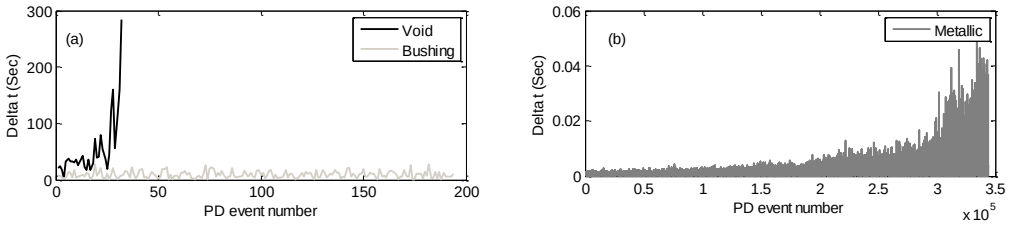


Figure 51 - PD event number versus Δt (a) five void and ceramic bushing (b) metallic protrusion

3.5.2.4. Combination of $|\Delta q|$ and Δt

The combination of $|\Delta q|$ versus Δt for the three dielectric samples was also investigated (Figure 52).

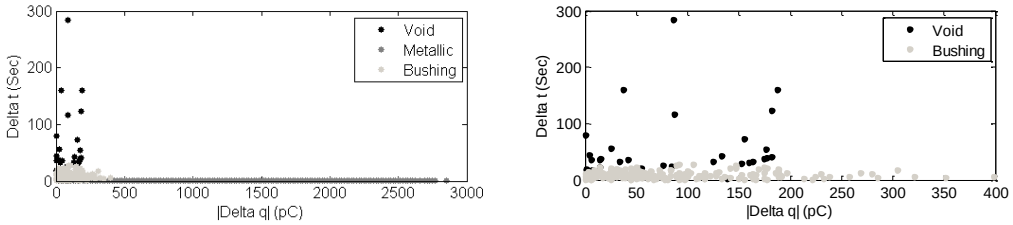


Figure 52 - Δq versus Δt (a) five void, metallic protrusion and ceramic bushing (b) five void and ceramic bushing

This approach enables the differentiation of the PD behaviour through considering the time and the charge differences between subsequent PD events. Three clusters of data are evident over the $|\Delta q|$ and Δt ranges. The first and most obvious is the wide range of $|\Delta q|$ and short Δt for the metallic protrusion sample. The approach segregates the data for the five void and ceramic bushing samples with the $|\Delta q|$

range being wider for the ceramic bushing and the Δt range being shorter. The results are summarised in Table X.

Table X - Comparison of $|\Delta q|$ and Δt for the three dielectric samples

	Five void		Metallic protrusion		Ceramic bushing	
	$\|\Delta q\|$(pC)	Δt (Sec)	$\|\Delta q\|$(pC)	Δt (Sec)	$\|\Delta q\|$(pC)	Δt (Sec)
Min	0	2.88	0	$1x10^{-4}$	0	0.19
Max	187.34	284.41	$2.85x10^{3}$	0.056	398.66	28.4

The obvious challenge would be differentiating the sources of PD but this approach could enable a sense check to confirm the allocated PD activity is consistent with the anticipated result. The relative difference between the three sources of PD can be highlighted through the use of a $|\Delta q|$-Δt-N plot. The event count (N) was generated using the histogram function in Matlab and the number of bins was set to 20. The plots for the three samples are shown in Figure 53.

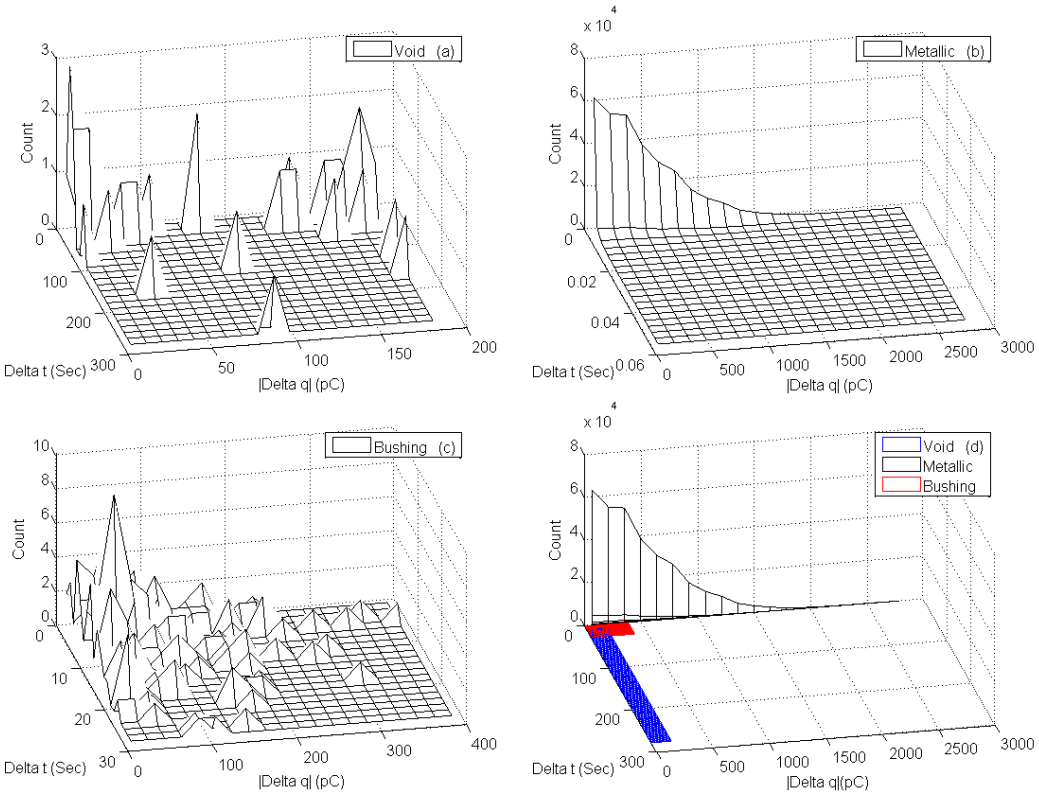


Figure 53 - $|\Delta q|$-Δt-N plot for the dielectric samples (a) five void sample (b) metallic protrusion (c) ceramic bushing (d) comparison of all on one plot

The three |*Δq*|-*Δt*-*N* plots show the difference in PD activity between the three dielectric samples adding this extra dimension allows the relative concentrations of data to be visualised. The five void sample has no clear peak and a wide spread in |*Δq*| and *Δt* planes. In contrast, the large number of PD events for the metallic protrusion highlights a clear peak at the lower end of the *Δt* scale and across a wide range of |*Δq*|. The PD behaviour of the ceramic bushing sample has with a wider range of *Δt* but reduced range of |*Δq*| with a clear cluster of data.

The relative activity of the three samples is very different but the PD data in the |*Δq*|-*Δt* plane (Figure 53 (d)) highlights the segregation of the PD data. The lack of a reference quantity reduces the effectiveness of the approach but the differentiation of PD data using |*Δq*| and *Δt* is quite effective in itself. A similar approach could be used to produce a surface plot of |*q*|-*Δt*-*N* it leads to a similar plot but the segregation is not as clear with the use of charge magnitude.

3.5.2.5. Skewness and Kurtosis

The statistical analysis of the DC PD data was explored further for the three dielectric samples under test. The mean ($\bar{x}$) value is a measure of the central tendency or expected value of the data set under investigation. The standard deviation (σ) is a measure to determine the relative spread of data in the set from the mean value. The shape of the distributions was assessed in terms of skewness and kurtosis. Skewness is a measure of the symmetry of the distribution around the mean of the sample [71], as defined in the following equation:

$$s = \frac{\frac{1}{n}\sum_{i=1}^{n}(x_i - \bar{x})^3}{\left(\sqrt{\frac{1}{n}\sum_{i=1}^{n}(x_i - \bar{x})^2}\right)^3} \tag{19}$$

A normal (symmetrical) distribution has a skewness of zero. A positive skew has a longer tail to the right hand side of the mean and a negative skew has a longer tail to the left hand side of the mean.

Kurtosis is a measure of the sharpness of the peak of a distribution when compared to a normal distribution [71], and is defined by:

$$k = \frac{\frac{1}{n}\sum_{i=1}^{n}(x_i - \bar{x})^4}{\left(\frac{1}{n}\sum_{i=1}^{n}(x_i - \bar{x})^2\right)^2} \quad (20)$$

The kurtosis for a normal distribution would be three. When the kurtosis is greater than three the distribution is said to be leptokurtic, the data has a more defined peak than a normal distribution. When kurtosis is less than three the distribution is said to be platykurtic, the peak is less pronounced.

The first statistical parameter to be studied is the mean values of the three PD quantities of interest for the dielectric samples Table XI.

Table XI - Comparison of mean ($\bar{x}$) values for the PD quantities of interest for the three dielectric samples

Sample	Variable	$\|Q\|$ (pC)	Δt (Sec)	$\|\Delta q\|$ (pC)
Five void	$\bar{x}$	108.36	55.65	84.3
Metallic protrusion	$\bar{x}$	3.15×10^3	0.0012	469.33
Ceramic bushing	$\bar{x}$	132.24	9.27	84.24

The mean value of $|Q|$ and $|\Delta q|$ was similar for both the five void and ceramic bushing samples. In contrast the mean values for $|Q|$ and $|\Delta q|$ was significantly higher. The quantity where the mean values for the three dielectric samples were different was for Δt. This is in line with previous findings where the time between PD events was an effective differentiator between PD sources.

Normality tests were conducted using a Kolmogorov-Smirnov test in OriginLab on the data sets ($|Q|$, Δt and $|\Delta q|$) for each dielectric sample. Normality was rejected in all the data sets to a 95% confidence level. With none of the distributions being normal the standard deviations were not considered.

The skewness of the data sets for each dielectric sample are summarised in Table XII.

Table XII - Comparison of skewness (s) for the PD quantities of interest for the three dielectric samples

Sample	Variable	$\|Q\|$	Δt	$\|\Delta q\|$
Five void	*s*	0.24	2.48	0.17
Metallic protrusion	*s*	-0.092	5.49	1.1
Ceramic bushing	*s*	1.65	0.78	1.43

The majority of values for skewness are positive suggesting that the tail on the right is longer for the majority of data sets in this study. The one exception is a very slight negative skew of the charge magnitude data for the metallic protrusion sample. The largest positive skew observed was the Δt data for the metallic protrusion sample. The clearest differentiation in skew is for the Δt data set.

The final statistical parameter under study is that of kurtosis, the kurtosis of the data sets is detailed in Table XIII.

Table XIII - Comparison of kurtosis (k) for the PD quantities of interest for the three dielectric samples

Sample	Variable	$\|Q\|$	Δt	$\|\Delta q\|$
Five void	*k*	1.29	9.4	1.39
Metallic protrusion	*k*	3.48	49.18	4.17
Ceramic bushing	*k*	5.88	3.07	5.04

The majority of values of kurtosis are greater than three that is the distributions are more leptokurtic. The only exception is the kurtosis of $|Q|$ and $|\Delta q|$ for the void sample where the kurtosis is less than three with the distribution being platykurtic. This makes sense with the histograms of $|Q|$ and $|\Delta q|$ for the five void sample having a less pronounced peak compared to the other dielectric samples. The Δt data sets for the three dielectric samples are all leptokurtic suggesting pronounced peaks within the respective distributions.

The use of these statistical measures allows a quantitative comparison to be developed without the requirement for a user to analyse distributions of data. Throughout the analysis of the PD parameters the analysis of Δt allowed easier differentiation between the three sources of PD. The importance of Δt in any DC PD analysis was confirmed in this statistical analysis. Overall this type of analysis will be

helpful for cataloguing typical PD activity for known defect types in a PD monitoring system for HVDC insulation.

3.6. DISCUSSION

PD was generally only apparent from the samples when the DC voltage was increased to $3V_R/2$ (1.5 times the peak AC inception voltage). This is as expected from available literature [17]. Under DC conditions, generally no sustained PD activity was detected until the voltage was held at $3V_R/2$. The metallic protrusion was the only sample to produce regular and sustained PD below $3V_R/2$. This is most likely because the close proximity of the point to the plane enables charge to traverse the gap quickly and be removed from the vicinity of the point, meaning a regular and frequent train of current pulses traverses the gap.

PD under AC excitation was generally higher in magnitude and more frequent than PD for the same sample under DC conditions. This matches the expectation from literature [17] with DC PD behaviour exhibiting lower magnitude and repetition rates. The exception was the ceramic bushing sample where a maximum PD level of 450 pC was detected at DC compared to only 9 pC under AC conditions. Note that the DC data was acquired at a higher voltage, which could contribute to the higher PD magnitude. In addition, the coupling of the HFCT to the earth lead, which is the conductor at which the PD pulse are generated, will give greater sensitivity in this case compared to the other PD samples.

The plotting methods recommended in IEC 60270 [3] enable the PD activity to be represented in a generic way for comparison. The most effective plots were the representation of the accumulated pulse charges over the test period and the class frequencies of PD pulses. These two approaches will be used in further analysis. In terms of the recommended plotting methods, the PD activity from the metallic protrusion sample is the easiest to distinguish by visual inspection.

The investigation of charge magnitude highlighted interesting behaviour and useful approaches to analyse the charge data. The relationship between charge magnitude and the average charge magnitude of its successor and predecessor was investigated for the three dielectric samples. The variation of average q_{suc} with charge magnitude for the three samples was:

- No correlation was expected for the five void and the metallic protrusion samples, this was true for the five void sample.

- There was a positive correlation for the metallic protrusion.
- A negative correlation was expected for the ceramic bushing sample but this was not apparent.

Similarly for the relationship between charge magnitude and q_{pre}:

- No correlation was apparent for the five void sample (as expected).
- There was a positive correlation for the metallic protrusion test cell, not expected from literature. This is likely to be due to the non standard design of the point (8 mm diameter with a 45° point).
- A slight negative correlation was observed for the bushing sample exhibiting surface discharge activity.

The study of charge magnitude and q_{suc}/q_{pre} offered limited correlation for the five void and ceramic bushing samples, one reason may be the lack of PD data.

The charge of the successor (q_{suc}) and predecessor (q_{pre}) was explored further through scatter plots of q_{suc}/q_{pre} versus current charge magnitude. There was a clear cluster of data for the metallic protrusion at a significantly higher PD magnitude. The behaviour observed for the five void and ceramic bushing samples was similar therefore difficult to compare.

The relative difference between successive (Δq_{suc}) previous (Δq_{pre}) PD events and the magnitude of the current PD event was studied. Again, the dominance of the metallic protrusion was highlighted and the similarity between the five void and ceramic bushing samples made differentiation problematic. Δq_{suc} and Δq_{pre} was also plotted against PD event number and the five void/ceramic bushing samples were difficult to specify. Histograms of Δq were generated and all histograms had a defined peak at the left hand side and tails to the right. These findings made any differentiation challenging using visual inspection.

The time between PD events was analysed, obviously the PD activity would need to be segregated in some way to allow the generation of time between PD events for specific sources. The time between PD events could be used to confirm correct initial classification by PD magnitude or similar. The analysis of time between PD events was first investigated in two ways the time interval to its successor (t_{suc}) and the time interval to its predecessor (t_{pre}). Initially, the charge magnitudes were separated into 10 bins and the average time to successor and predecessor was calculated for each bin. There was an expectation that the five void sample would

exhibit a positive correlation but this was not evident. This was possibly due to the sample having five voids or the discharges may have been streamer like where the correlation failed in previous studies [17]. The only correlation observed was for the metallic protrusion sample where a positive correlation was evident for t_{suc}. Observable differences were apparent for the histograms of t_{suc} and t_{pre} for the three samples. Characteristic peaks were evident for the three samples at different values of t_{suc} and t_{pre}. The study of time difference histograms was, based on these three samples, the most promising analysis technique to differentiate/characterise the time difference of PD activity from PD sources.

The variation of t_{suc} and t_{pre} was studied in more detail with a scatter plot generated of t_{suc}/t_{pre} versus charge magnitude of current PD event. This approach allowed the clustering of data on these plots with three defined clusters according to the dielectric samples. The use of charge magnitude and time between PD events was effective in segregating the data. The five void sample generally had smaller PD events occurring less frequently in contrast the metallic protrusion had large PD events occurring very frequently. The ceramic bushing sample was somewhere in the middle in terms of PD magnitude and time between PD events. Histograms of time between PD events were generated and clear differences were apparent for the three dielectric samples.

The time between PD events was also plotted against PD event number. This approach allowed the differentiation of PD behaviour for the five void and ceramic bushing samples. The time between PD events for the void sample generally increased as the voltage was held constant in contrast the time between PD events for the ceramic bushing sample remained consistent through the test. This emphasised the typical behaviour observed in a void with the wait for the voltage across the void to recover and a starting electron to begin the ionisation process. A possible categorisation of PD could be to threshold the time between events with the knowledge that $\Delta t_{void} > \Delta t_{bushing} > \Delta t_{metallic}$.

The combined investigations of $|\Delta q|$ and Δt generated a scatter plot of $|\Delta q|$ versus Δt for the three dielectric samples. Using this approach, the differentiation between the PD activity from the three dielectric samples was possible. There was some crossover between the five void and ceramic bushing samples but the classification was well defined otherwise. The main reason the classification worked was that the ranges of $|\Delta q|$ and Δt for the three dielectric samples were diverse enough. There

could be cases when the sources of PD are more closely matched meaning that classification is more challenging.

This approach was expanded into a 3 dimensional plot, a $|\Delta q|$-Δt-N plot, to enable an understanding to be developed of the relative spread of data within this plot as detail is lost due to the nature of the scatter plot. The relative difference in these $|\Delta q|$-Δt-N plots was clear with the three sets of data occupying different locations in the plot. This approach was found to be more effective than plotting $|q|$-Δt-N as the charge magnitude data of the five void and ceramic bushing samples was very similar.

The mean, skewness and kurtosis of the key PD quantities were studied. The key quantities were charge magnitude, time difference between PD events and difference in charge magnitude between PD events. Standard deviation was not considered as the data sets for the three dielectric samples failed the Kolmagorov-Smirnov test at a 95% confidence level. The overall aim of this work was to allow a statistical assessment of the key PD quantities from different PD sources removing the need for visual inspection of PD data. The most effective quantity to differentiate PD sources was found to be the time difference between PD events. A variation was evident for the mean time between PD events, skewness and kurtosis for the time between PD events. In contrast the statistical analysis of charge magnitude and charge magnitude between PD events were similar for the three test cells.

3.7. CONCLUSIONS

Literature related to the PD behaviour of dielectric samples under AC and DC conditions was reviewed. The analysis techniques under AC and DC conditions were also investigated.

This chapter has compared AC and DC testing of several dielectric samples with PD-producing defects. The AC and DC test methods were presented which will be used throughout this thesis. The AC testing was used to confirm the inception voltage of PD and the dominant PD source through reference to the PRPD behaviour. The AC inception voltage was used to define the voltages to be applied during DC ramp testing of the samples. The ramp test method enables repeatable DC testing to be performed on the generic samples.

Revisions to IEC 60270 test methods were employed to statistically analyze the test results from the three samples under DC conditions, showing clear differences in

their characteristics that would potentially allow them to be distinguished. The recommendations allow a generic representation of DC PD behaviour to be analysed effectively.

The investigation of the DC PD quantities of charge magnitude and time between PD events were conducted for the three dielectric samples under test. The main challenge associated with analysing PD apparent from a HVDC system exhibiting multiple sources of PD is picking out the different behaviour. The first lens to apply is the differentiation of PD sources using charge magnitude of PD. Then look at studying the charge between PD events and time between PD events to confirm correct classification of PD activity. The work revealed the value in studying the time between PD events to differentiate PD activity apparent in a HVDC system. An analysis method using both charge variation and time between PD events using a $|\Delta q|$-Δt-N plot was presented and the three PD sources could be differentiated.

Methods to quantify the statistical behaviour of data sets were explored with the overall aim of defining the distribution of PD data under study. The measures of statistical behaviour applied were the mean, skewness and kurtosis. The use of time between PD events was the most effective quantity to apply statistical analysis methods.

The most promising methods identified in this chapter will be applied to the DC PD data under analysis in the remainder of this thesis. The behaviour of void type dielectric samples is of particular interest in this thesis and will be explored further in the following chapters. Initially, the dielectric sample with 5 voids will be tested under varied voltage conditions then novel manufacturing techniques for creating gas filled voids in insulation material will be explored.

In terms of future work:

- The primary aim will be to develop more dielectric samples to allow AC and DC PD testing to be conducted.
- The main area of interest is exploring the PD behaviour of void type samples under DC conditions.
- The manufacture of virgin samples is important as it would be interesting to compare the behaviour of the heavily aged sample in this work to a virgin sample.

- The development/evolution of DC PD behaviour during the aging process would also be interesting to explore.
- The behaviour of a void type sample during different voltage regimes has received increased attention to date, incorporating this and ramp testing would be valuable.
- The immediate test history of a void type sample is known to affect the DC PD behaviour. Investigating this for a range of conditions would be useful for future test standards and understanding of insulation behaviour under varied voltage conditions.
- Consider altering the ramp and hold technique to be based on the number of PD events recorded rather than the hold period. This would allow the PD sources to be compared on a like for like basis.

4. VARIATION OF VOLTAGE APPLIED TO A VOID TYPE SAMPLE

This chapter builds on the methods and analysis techniques introduced in chapter 3 to investigate PD behaviour of void type defects under varied DC polarity tests. During prequalification/type tests insulation system are exposed to varied voltage conditions, this work considers the behaviour of a void type dielectric sample during simplified but representative tests. The immediate test history of the void type dielectric sample was varied. The tests are conducted on a void type dielectric sample, with an unknown history, are presented to inform how a void type defect will respond under varied conditions in a HVDC system.

The AC and DC PD test methodologies from Chapter 3 were applied to the sample as a base line of PD behaviour. The first study performed was an investigation into the grounding period between subsequent DC PD tests from 32 days to 3 days. Another study performed was the repeated application of one polarity and varied polarity DC ramp tests. The inclusion of an AC test between two DC ramp tests was also investigated with the PD behaviour altered over the full 80 minute hold period.

This work aims to inform how a void type sample responds under varied DC conditions, typically seen during DC insulation system prequalification and type testing. This work seeks to highlight the change in dominant behaviour from initially capacitive to resistive behaviour following a voltage change. Analysis methods are presented to differentiate the different phases of PD behaviour during the 80 minute hold period.

4.1. ASSOCIATED LITERATURE

The main test standard of interest to this work was Cigre TB 496 [72] which details test recommendations for DC extruded cable systems. The tests of interest to this work was the load cycle/polarity reversal testing carried out during the prequalification and type testing of cable samples for DC systems. A further area of interest is during routine testing where AC testing can be performed if the system design allows.

The prequalification and type test procedures will be introduced in the following sections. The prequalification procedure consists of a series of three tests:

- **Long duration voltage test -** over a 360 day duration a range of load cycle, high load, polarity reversal and zero load tests are applied to the system under test (dependant on converter topology).
- **Superimposed impulse voltage test -** used at the end of the long duration test to confirm the reliability of the insulation system.
- **Examination -** consists of a dissection of the cable system to inspect for weakening of the insulation.

Type testing subjects the cable sample to characteristics typical of the intended application environment [72]. The 4 tests performed during type testing are as follows:

- **Mechanical preconditioning test -** to subject the system to the maximum mechanical stress over the lifetime of the system (handling, installation and recovery).
- **Load cycle test -** the cable system is subjected to thermal cycles over a 24 or 48 hour period at a set voltage. The polarity of the voltage for subsequent load cycles is varied. The load cycles for LCC and VSC systems are different.
- **Polarity reversal test -** sample subjected to cycles of polarity reversal over a 24 hour period.
- **Superimposed impulse voltage test -** is used to confirm that the insulation of the cable system is still intact following the load cycle/polarity reversal tests.

The aspects of interest in the prequalification and type tests are those of the load cycles and polarity reversal tests. The load cycle testing for LCC and VSC are slightly different in terms of the numbers of load cycles at each stage and LCC has an additional stage of eight “24 hours” load cycles with polarity reversals at U_{TP1}.

- 24 hour load cycles consist of 8 hours of heating followed by 16 hours of cooling.
- 48 hour load cycles consist of 24 hours is heating and 24 hours is cooling. During the heating cycles the voltage remains at the defined voltage.
- The polarity reversal test consists of three polarity reversals every 24 hours and the recommended time for polarity reversal is within 2 minutes.

- AC testing is recommended during routine testing of system components if the insulation system and cable design allow AC testing to be performed.

The literature review for DC PD testing of dielectric samples was summarised in Chapter 3. A position paper from the IEEE DEIS HVDC Cable Systems Technical Committee [73] summarises a protocol for the measurement of space charge in HVDC cable systems during prequalification or type tests. Focus is placed on the measurement of space charge with varied poling time, depolarization time and variation of temperature. The objective of the protocol is to determine the resultant electric field and any disturbance due to space charge in the cable sample before and after the prequalification tests.

Early work by Bever *et al.* [30] investigated DC ramp testing of dielectric samples namely capacitors. The ramp testing was employed to allow the application of a controlled and repeatable DC ramp to the dielectric sample under test. It was reported that under identical and repeated ramp testing that PD activity in subsequent tests was much reduced due to the injected space charge. It was also reported after a ramp test that the PD results from a tubular capacitor were reasonably repeatable after several days with the capacitor shorted to ground over this period. The paper also provided some suggestions for DC PD testing:

- Be aware of injected space charge effects, polarization and hysteresis – ferroelectric effects in the test object
- Even for non ferroelectric materials one should wait 24 hours before restarting testing – with the sample shorted meanwhile
- Pay attention to the previously applied voltage (test history):
    - A repeat in polarity will the second time give very few PD pulses (unless degradation has taken place)
    - For trend interpolation, two sets of data should be taken after life exposure – once in the same polarity as life exposure and then reversed. This will bring back a large number of PD events. Alternatively the life test can be done at elevated temperature (85 °C) with the turn of sequence above.

The areas of particular interest to this work are

- The effect of space charge
- The grounding period for void type dielectric samples

- The test history of the dielectric sample.

The current understanding of space charge behaviour under DC conditions will be investigated. DC PD behaviour is related to space charge accumulation in dielectric samples [74]. Space charge accumulation after each PD event can affect partial discharge inception voltage (PDIV) partial discharge amplitude, delay time for starting electron and the repetition rate [75]. Under DC conditions the accumulation of space charge is more of an issue than under AC conditions where the electric field polarity variation prevents charge from penetrating the bulk of the insulation [75].

Space charge is retained in traps in dielectrics even after the voltage is removed [76]. The relative depth and number of traps has been found to contribute to the rate of charge decay [75] explaining the relative differences of charge decay in different materials. The initial electron required to start the PD process can be provided by trapped charge at the boundary between the cavity and the dielectric [74]. The charge could be deposited from previous PD activity or could be due to charge transport from the electrodes to the cavity.

The formation of space charge takes time to build up following a voltage polarity change and during depolarization it takes time for space charge to decay [20]. Under polarity reversal it is possible to reverse the space charge distributions so that the distribution has the same shape but opposite polarity to those obtained initially [77]. This phenomenon has been reported in a number of papers [78] and is known as the ‘mirror effect’. In order to remove space charge the de polarization voltage is applied for a specific period of time and then removed and the specimen is placed under short circuit conditions to enable charge dissipation [76].

To date the grounding period or investigating the discharge time of void type dielectric samples and the relation of grounding period to PD activity has not been investigated in great detail. Publications covering the discharging of dielectric samples have been presented; the derivation of resistivity [79], the study of polarization/depolarization current in polymeric samples with voids [80] and other equipment [81], [82].

The variation of the voltage conditions applied to dielectric samples has received increased attention. The consideration of combined AC/DC stresses [29] and the effect of voltage ripple under DC conditions on the behaviour of dielectric samples

[28], [83], [84]. The investigation of repeated DC PD tests on a void type dielectric sample has been considered [17] but detailed results have not been presented. There is a gap in current research to study the effect of previous DC PD tests on the current DC ramp test, some observations were presented [30]. More detailed analysis [17], [85] presents findings from voltage variations and polarity changes. The electric field distribution in the dielectric sample is determined by the characteristics of the insulation system at hand. During the initial application of a DC voltage across a dielectric sample the electric field is capacitively graded and once the polarization process is complete the field can be defined as resistively graded. During this phase of polarization the insulation system has increased levels of conductivity. The PD repetition rate during this polarization process is higher and can last for some time. This effect was more apparent when the polarity is reversed.

This chapter will investigate the possible impact of the load cycle and the polarity reversal tests. This work aims to understand how a void type defect inside a cable system may behave under these voltage changes. No provision was available to initiate the temperature effects as such the effects of voltage variations alone will be investigated. The effect of AC testing in between DC energisation on PD activity will also be investigated.

The measurement of space charge was not possible in this work but an understanding of the effect of space charge on PD has been highlighted by the work above. The work presented in this chapter details how DC PD activity in a void sample varied for the investigation around the grounding period of dielectric samples and for a range of conditions similar to those outlined in the prequalification and type testing of HVDC cables. Areas of interest to this work are the separation of the PD activity related to the capacitive behaviour and the resistive behaviour of the insulation. The test method and experimental results will be discussed in the following sections.

4.2. ELECTRIC FIELD GRADING THEORY

A good review of modelling the electric field grading in insulation samples is detailed in a paper from Lemke [86]. The history around the development of the abc model introduced in chapter 3 is outlined. Later papers have developed this work for AC conditions [87], [88]. Under DC conditions the abc model must be adjusted to include resistances for the charge dissipation from the void to the surrounding

dielectric (as shown in Figure 30). The time constant for charging the cavity in this model is given by equation (21) [17].

$$\tau = \frac{R_b R_c (C_b + C_c)}{R_b + R_c} \tag{21}$$

R_b and C_b is the resistance and capacitance of the epoxy insulation in series with the void (above and below). R_c and C_c is the resistance and capacitance of the air filled void itself. The capacitance and resistance values for the five voids inside the epoxy resin disc were determined using equations (22) and (23).

$$C = \varepsilon_0 \varepsilon_r \left(\frac{A}{d}\right) \tag{22}$$

$$R = \frac{\rho L}{A} \tag{23}$$

With ε_0=8.85x10^{-12} F/m, ε_r the relative permittivity (ε_{r_air}=1 and ε_{r_epoxy}=3). A is the area of the void, d is the separation distance of the parallel plates. ρ is the resistivity of the material (ρ_{air}=1x10^{12} Ω.m and ρ_{epoxy}=1.3x10^{16} Ω.m), L is the length of the conductor and A is the area of the conductor (void in this case). The relations for the individual capacitance and resistances are as follows (equations 24-27).

$$C_b = \varepsilon_0 \times \varepsilon_{r\_epoxy} \left(\frac{A_{void}}{G_{insul} - G_{void}}\right) \tag{24}$$

$$R_b = \frac{\rho_{epoxy} \times (G_{insul} - G_{void})}{A_{void}} \tag{25}$$

$$C_c = \varepsilon_0 \times \varepsilon_{r\_air} \left(\frac{A_{void}}{G_{void}}\right) \tag{26}$$

$$R_b = \frac{\rho_{epoxy} \times G_{void}}{A_{void}} \tag{27}$$

The capacitance, resistance and time constant to charge each of the five individual voids are detailed in Table XIV.

Table XIV - Capacitance, resistance and time constant for charging the five voids in the epoxy resin disc

Void (mm)	C_b (F)	R_b (Ω)	C_c (F)	R_c (Ω)	τ (Sec)
0.59	2.06×10^{-14}	1.29×10^{15}	1.64×10^{-14}	7.01×10^{18}	47.71
0.46	1.15×10^{-14}	2.32×10^{15}	1.28×10^{-14}	9×10^{18}	56.19
0.43	9.83×10^{-15}	2.7×10^{15}	1.2×10^{-14}	9.62×10^{18}	58.87
0.32	5.09×10^{-15}	5.22×10^{15}	8.9×10^{-15}	1.29×10^{19}	73.02
0.21	2.06×10^{-15}	1.29×10^{15}	5.84×19^{-15}	1.97×10^{19}	101.97

The minimum time to charge the largest void is 47.71 seconds and the time between PD events is likely to be longer due to the time delay for a starting electron. Thus following the initial capacitive grading region, identified by large PD events with short times between PD events, the insulation will be graded using the model discussed above. It can be assumed that once the time between PD events exceeds this minimum value then the capacitive grading of the insulation has ceased. A series of tests will be conducted to test this assumption and this will be used to determine the grading of the insulation.

4.3. TEST METHODS

This section will describe the sample under test and the individual tests to be applied to each sample. All of the tests were on the same void type dielectric sample. The dielectric sample was energised under the following regimes to see the effect on measured PD activity:

- Standard AC PD test
- Standard DC ramp profile
- Investigation of grounding period between subsequent DC ramp tests
- Repeated applications of positive ramp tests
- Variation in polarity between subsequent ramp tests
- AC test between two DC ramp tests

The inherited dielectric sample was manufactured in 2006 at Caledonian University and has been subjected to extensive tests over the years. The use of this heavily aged sample will provide a good basis for comparison with virgin samples and

provide an insight into the how a heavily aged sample will behave. The individual tests listed above will be described in the following sections.

4.3.1. SAMPLE UNDER TEST

The dielectric sample was designed to represent internal discharge, five voids in the form of air bubbles were induced during the casting process of an epoxy disc. Two plain brass electrodes (diameter of 19 mm with a round of radius of 5 mm) were glued to the upper and lower faces of the epoxy disc directly above the five voids. The construction process ensured that the voids are all the same depth (five parallel voids) and the approximate diameters of the voids are as follows; 0.59, 0.46, 0.43, 0.32 and 0.21 mm. An illustration of the cross sectional view of the sample is shown in Figure 54.

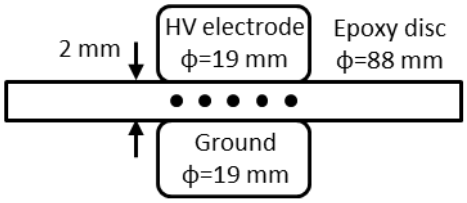


Figure 54 - Illustration of five voids in an epoxy resin disk (not to scale)

4.3.2. STANDARD AC AND DC PD TESTS

The standard test methods for AC and DC PD testing are detailed in chapter 3, the work described here makes use of the two methods and the analysis methods which were most effective. The sample was initially tested under AC conditions to confirm the dominant source of PD and to determine the inception voltage (voltage at which repetitive and sustained PD occurred). The ramp test method was employed to ensure repeatable DC tests could be conducted on the sample. In this phase of testing the hold period at $9V_R/5$ was extended from 30 minutes to 80 minutes. The DC PD data under analysis in this chapter is the data recorded during this 80 minute hold period. The hold period was extended to allow the transition from capacitive to resistive grading to be evident in the DC PD data for analysis purposes.

4.3.3. GROUNDING PERIOD

An investigation into the influence of the grounding period on PD activity recorded during identical DC ramp tests and PD behaviour was devised. The same ramp test

profile was used and the only variation between the tests was the grounding period. The grounding period was varied between 32 days and 3 days. The overall aim of this work was to understand the effect of grounding period on DC PD activity during an 80 minute hold period.

4.3.4. REPEATED APPLICATION OF POSITIVE RAMP TESTS

In this phase of work the void type dielectric sample was exposed to three identical positive DC ramp tests, as shown in Figure 55.

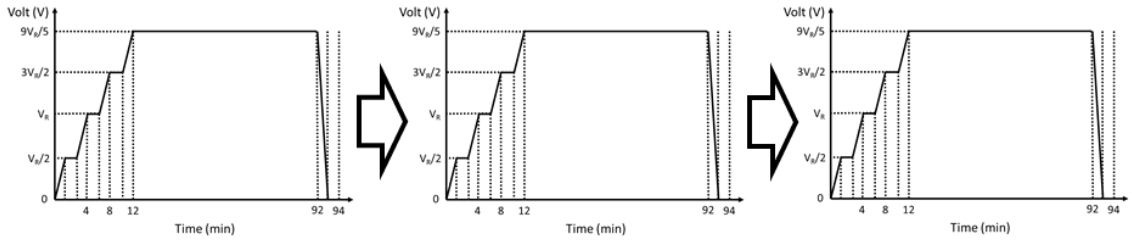


Figure 55 - Illustration of three repeated positive ramp tests

The previously defined ramp profile was used each time. After the completion of each test the power supply was shut down and the test set was grounded (generally for 30mins). The aim of this test was to understand how the PD activity varied during the repeated application of positive ramp tests.

4.3.5. VARIATION IN POLARITY OF RAMP TESTS

This work involved the initial application of a positive ramp test followed by a negative ramp test and finally a further positive ramp test, as shown in Figure 56.

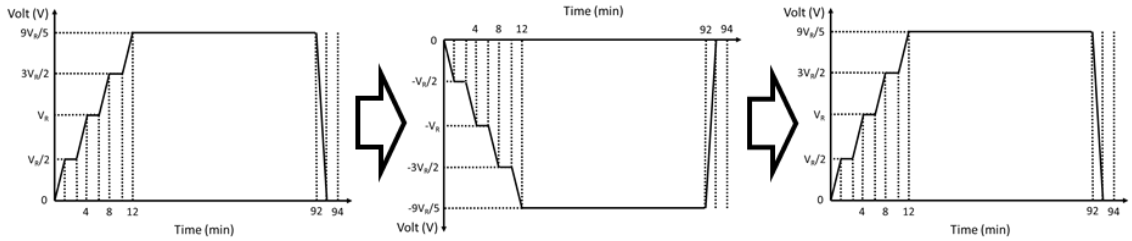


Figure 56 - Illustration of variation in polarity of ramp tests

The ramp profile used for positive and negative ramp tests was identical with the only change being the polarity. After the completion of each test the power supply

was shut down and the test set was grounded (generally for 30 minutes) between each test. During this time the diode in the rectifier was re-orientated to reverse the polarity of the DC voltage across the sample under test. The objective of these tests was to understand the effect of polarity variation on DC PD activity.

4.3.6. AC TEST BETWEEN TWO DC RAMP TESTS

During this phase of testing a positive ramp test was initially performed, followed by an AC PD test and finally a further positive ramp test was conducted as shown in Figure 57.

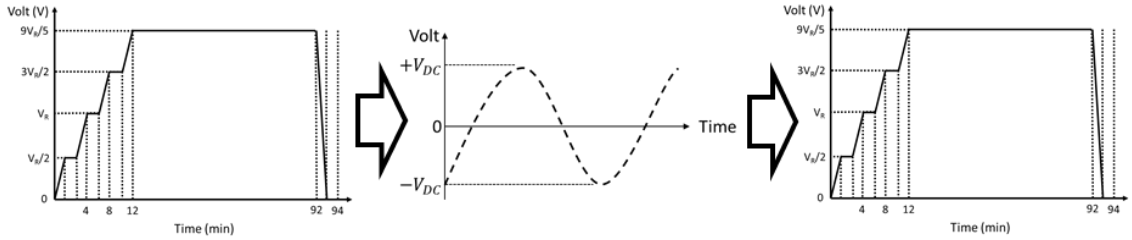


Figure 57 - Illustration of AC test between two positive ramp tests

After the completion of each test the power supply was shut down and the test set was grounded. The time to change the test circuit from a DC circuit to an AC circuit was around 30 minutes. This test was of interest as some cable designs permit the inclusion of AC PD testing. The area of interest was the impact of an AC PD test on the subsequent PD activity during the positive ramp test.

4.4. RESULTS

The results from the above tests are presented in this section.

4.4.1. STANDARD AC AND DC PD TESTS

The voltage of the AC test set was incrementally increased until repetitive and sustained PD was observed from the test sample, this was identified as the inception voltage. The inception voltage for the five voids in epoxy was found to be 8 kV rms. The φ-q-n plot for the five void sample at 8 kV is detailed in Figure 58 for 30 seconds of PD activity.

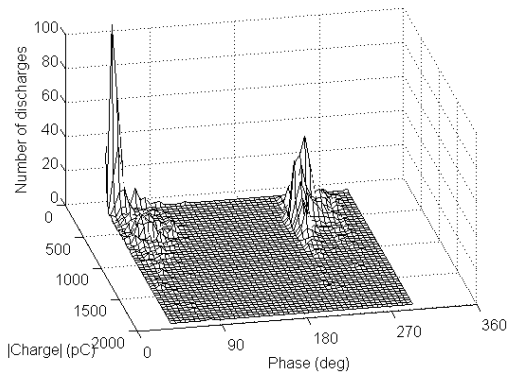


Figure 58 - φ-q-n plot for the AC PD test on the five void sample at 8 kV rms.

The φ-q-n behaviour for a void type discharge leads the test voltage peak and the PD activity generally extinguishes after the test voltage peaks (90 and 270°). The φ-q-n plot shows similar behaviour in the first and third quadrants, as expected for a void type discharge. This test confirms the dominant source of PD from the test sample and also defines the inception voltage which was used then to inform the voltages used during DC testing.

The DC ramp test profile was defined by the peak value of the AC inception voltage (V_R). Based on test experience with this sample in chapter 3, the voltage steps in the ramp profile were defined as $V_R/2$, V_R, $3V_R/2$ and $9V_R/5$. The voltage was held constant for 4 minutes at the three lower voltages, of 5.9, 12 and 17 kV, and for 80 minutes at the highest voltage of 20 kV. The data under analysis in this work is that of the 80 minutes of hold data at ±20 kV.

4.4.2. GROUNDING PERIOD TESTS

The DC PD behaviour of the sample was investigated for different grounding periods prior to performing the next positive DC ramp test on the sample. In this work the number of days refers to the number of days that the sample was grounded before performing the following positive DC ramp test. The tests and grounding periods were performed in the high voltage lab at an ambient temperature of 25 °C.

Figure 59a details the number of PD events recorded during each DC ramp test. The data was split into the data recorded during the 80 minute hold at +20 kV and the remaining data recorded during the ramp test. Figure 59b details the cumulative charge level over the 80 minute hold at +20 kV.

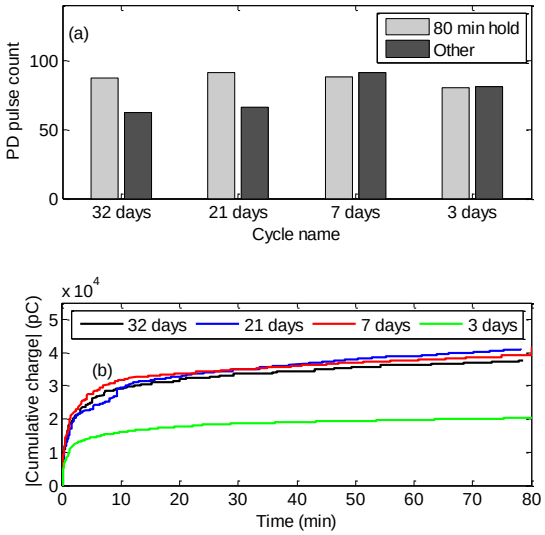


Figure 59 - Variation of grounding period between PD tests (a) PD pulse count for the three positive ramp tests (b) measuring time vs cumulative charge.

The results of Figure 59a show that the total number of PD events recorded during the 80 minute hold at +20 kV was: 87 PD events (32 days), 91 PD events (21 days), 88 PD events (7 days) and 80 PD events (3 days). Overall the number of PD events for the 3 day grounding period is similar to the three DC ramp tests. The more revealing plot is that of the cumulative record of PD activity over the 4 tests (Figure 59b). The hold at +20 kV which had 3 days of grounding prior to the ramp test has a lower cumulative charge count than grounding periods of 7, 21 and 32 days. The three longer grounding periods exhibited very similar cumulative charge behaviour over the 80 minute hold period suggesting that equilibrium occurred after 7 days.

The main difference in the cumulative charge plots is during the initial minutes of PD activity where the capacitive effects are more dominant following a voltage change. Following this period the delta between the cumulative plots is more constant suggesting similar PD behaviour over this period.

In order to understand the differences in PD behaviour between the different grounding periods the PD quantities of charge and the time of occurrence was analysed in more detail. The key statistical measures for charge magnitude, difference in charge magnitude and time difference between PD events are detailed in Table XV.

Table XV - Charge magnitude ($|q|$) of PD events, difference in charge magnitude ($|\Delta q|$) and time between events (t) for variation of grounding periods

Variable	32 days	21 days	7 days	3 days
$Mean_{|q|}$ (pC)	432.53	451.13	447.3	253.38
$S_{|q|}$	1.93	2.38	2.59	2.63
$K_{|q|}$	6.19	7.97	10.31	13.47
$mean_{|\Delta q|}$ (pC)	365.85	319.07	351.42	176.13
$S_{|\Delta q|}$	1.75	2.27	1.95	2.76
$k_{|\Delta q|}$	5.87	7.81	6.80	12.72
$mean_t$ (Sec)	54.83	52.13	54.9	60.28
S_t	1.64	1.04	0.55	1.37
K_t	4.43	2.97	1.52	3.87

The main difference in the data was that for $|q|$ and $|\Delta q|$ the mean was generally lower for reduced grounding periods. The skewness and kurtosis for $|q|$ and $|\Delta q|$ were generally more positive as the number of grounding days reduced. The positive skew suggests more data is concentrated at the lower end of the scale and a longer tail was evident to the right. The measures of kutosis were generally greater than three with more obvious leptokurtic behaviour evident as the grounding period was reduced.

The three key measures identified above were plotted against PD event number as shown in Figure 60. The general increase in t_{suc} with PD event number was evident for all three grounding periods. A smaller deviation of t_{suc} was evident for the grounding periods of 7 and 3 days. The behaviour of $|q_{suc}|$ and $|\Delta q_{suc}|$ was very similar with the general trend being a reduction in magnitude with PD event number. An interesting observation in the three plots is the relative change which occurred around PD events 50-60 which was the increase in t_{suc} and the stabilisation of $|q_{suc}|/|\Delta q_{suc}|$. There is a fundamental change in behaviour from initially large PD events with short times between PD events to smaller PD events with longer times between PD events. This may be the transition from capacitively graded insulation to resistively graded insulation evident in the data.

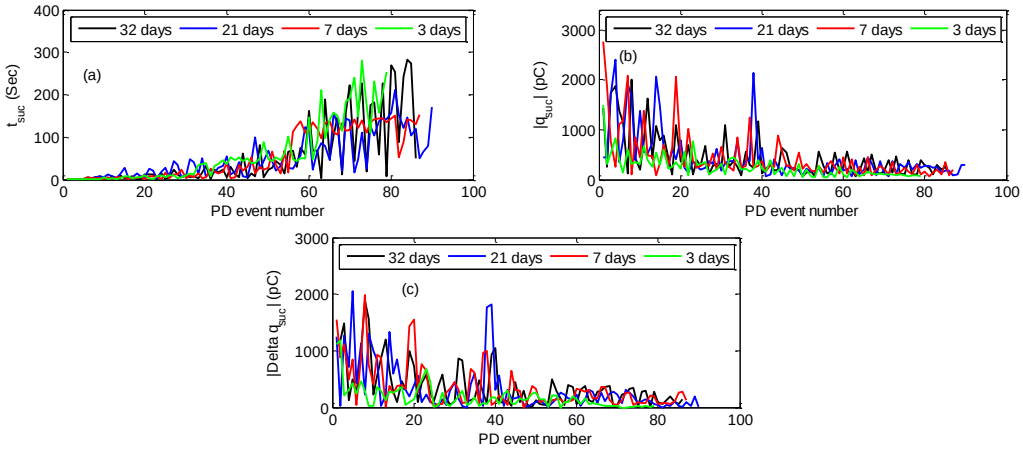


Figure 60 - Comparison of the holds at +20 kV for the four grounding periods (a) PD event number versus time to successor (t_{suc}) (b) PD event number versus charge magnitude of the successor ($|q_{suc}|$) (c) PD event number versus difference in charge magnitude of the successor ($|\Delta q_{suc}|$)

The three quantities were next compared to charge magnitude of the current PD event (Figure 61).

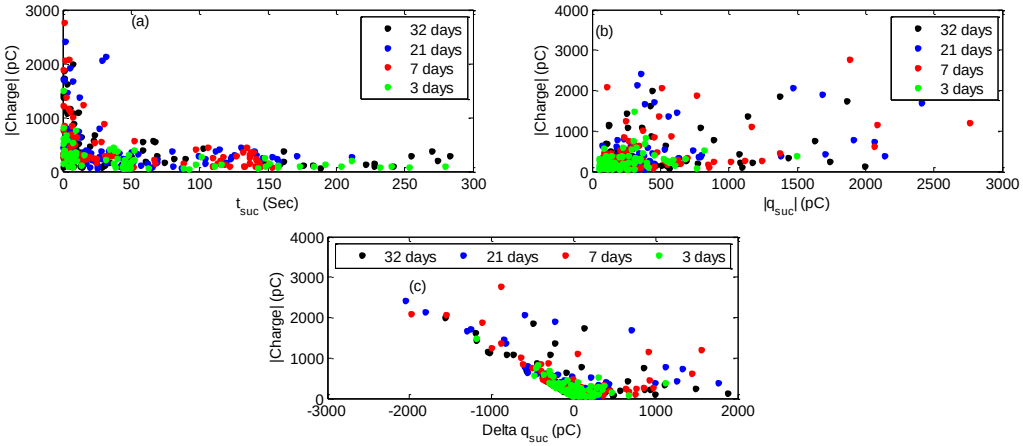


Figure 61 - Comparison of the holds at +20 kV for the four grounding periods (a) t_{suc} versus charge magnitude (b) $|q_{suc}|$ versus charge magnitude (c) Δq_{suc} versus charge magnitude

A cluster was evident at the lower end of t_{suc} (0-30 seconds) with large PD events apparent. A second cluster with reduced charge magnitude was evident for t_{suc} at 30-150 seconds. A third group of data was evident with further reduced magnitude for t_{suc} ranging from 150-300 seconds. Similar behaviour was observed for $|q_{suc}|$ and Δq_{suc} versus charge magnitude of current PD event with a clear cluster for the lower range of $|q_{suc}|$ and Δq_{suc} typically seen after 60 PD events. The large initial PD

events with short t_{suc} due to capacitive effects could be differentiated from the smaller PD events with larger t_{suc}.

$|\Delta q|$ was plotted against Δt for the data from the four hold periods as shown in Figure 62.

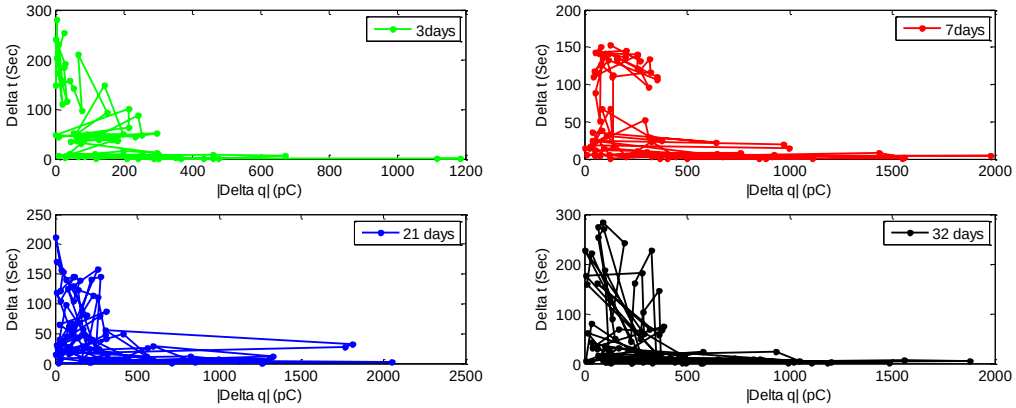


Figure 62 - $|\Delta q|$ versus Δt for 3 days, 7 days, 21 days and 32 days grounding periods.

The lines are included in the scatter plot to enable the relation between subsequent PD events. The transition from large $|\Delta q|$, over the Δt range of 0 to 50 seconds, to smaller $|\Delta q|$ with Δt over than 50 seconds is clear. Over the initial PD events, the charge magnitude varies by a large amount and the time between PD events is less than 50 seconds, this can be observed as horizontal lines between PD events on the plots. For the later PD events the charge magnitude varies by a smaller amount (max 400 pC) and the time between PD events was longer leading to vertical lines between PD events on the plots. These observations may be related to transition from capacitively graded insulation (large PD events in quick succession) to resistively graded insulation (smaller PD events less regularly). This transition in PD behaviour matches the previously calculated time constant of 47.71 seconds for the DC abc model with the difference in delay time for the starting electron leading to a spread in Δt of 50-300 seconds.

To understand the relative concentration of the PD data on the plots above a $|\Delta q|$ vs Δt vs N plot was generated for the PD data following the four grounding periods and is presented in Figure 63.

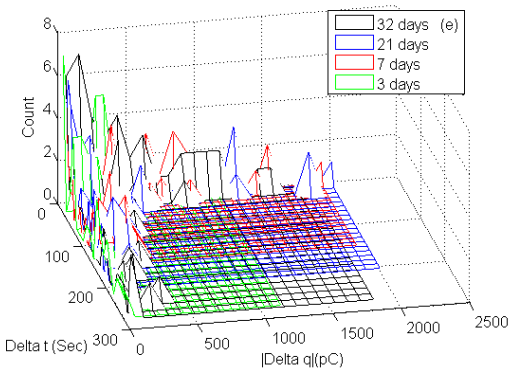


Figure 63 - $|\Delta q|$ vs Δt vs N plot for the four grounding periods

The first cluster evident was the data with a wider spread of $|\Delta q|$ and short Δt between PD events for the three data sets with extended grounding periods. This behaviour may be related to the capacitive grading of the insulation and the extension of the grounding period could have enhanced the capacitive response of the insulation. All plots exhibit a second cluster of data with a smaller spread of $|\Delta q|$ but wider range of Δt and this response was extended when the grounding period of the dielectric sample was reduced. The results of such analysis can guide testing toward examination of either capacitive or the resistively graded insulation behaviour. If the capacitive response of fully discharged dielectric samples is of interest then extended grounding periods could be required. If the resistive grading is of interest then there is limited value in discharging the dielectric sample for extended periods.

4.4.3. REPEATED APPLICATION OF POSITIVE RAMP TESTS

In this section the dielectric sample was subjected to repeated ramp tests of positive DC polarity in quick succession. A bar chart detailing the PD events recorded for the three tests are shown in Figure 64a. The cumulative charge activity during the three subsequent 80 minute holds are detailed in Figure 64b.

The largest and most frequent PD events occurred during the first positive ramp test when 179 events were recorded and the least occurred in the third positive ramp test when 76 events were recorded. These results are split into the data gathered during the 80 minute hold and data gathered during the rest of the DC ramp test. When the dielectric sample was exposed to three positive tests in succession the

number of PD events recorded generally reduced test on test (both as a whole and for the 80 minute hold at +20 kV).

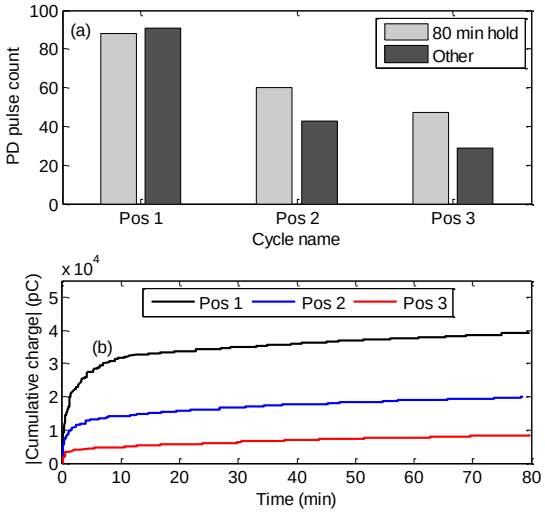


Figure 64 - Three cycle positive ramp tests (a) PD pulse count for the three positive ramp tests (b) measuring time vs cumulative charge

The cumulative build-up of charge from the resulting PD events varied for the three subsequent tests. The first 80 minute hold, at 20 kV, had the highest cumulative charge over the 80 minute test and the lowest accumulation of charge was for the final positive hold, at 20 kV. The main difference in PD behaviour was during the initial few minutes with larger PD events evident in the first positive hold.

The PD activity appears to be similar but, in general, the PD pulses from the first positive test have a higher magnitude and are more frequent. This was expected from the reported behaviour in previous studies [17] documenting the PD behaviour for an insulation which was capacitively graded.

A summary of the statistical parameters for the charge magnitude and time between events for the three subsequent ramp tests are detailed in Table XVI. The mean for $|q|$ and $|\Delta q|$ reduced when the dielectric sample was exposed to repeated positive ramp tests. In contrast, the mean for time between PD events increased when the dielectric sample was exposed to repeated positive ramp tests. The skewness was always positive, meaning that the majority of the data was to the left of the mean and a longer tail was evident on the right. The kurtosis for $|q|$ and $|\Delta q|$ was always greater than three (normal distribution) but no trend was apparent when repeated

positive ramp tests were conducted. The kurtosis of *t* was initially less than three for the first two holds at +20 kV and then was greater than three for the final hold at +20 kV.

Table XVI - Charge magnitude (|*q*|) of PD events, difference in charge magnitude (|*Δq*|) and time between events (*t*) for repeated positive DC ramp tests

variable	Pos 1	Pos 2	Pos 3
$\mathbf{Mean_{|q|}}$ **(pC)**	447.30	334.65	181.35
$\mathbf{S_{|q|}}$	2.60	3.33	2.87
$\mathbf{k_{|q|}}$	10.31	16.07	11.68
$\mathbf{mean_{|\Delta q|}}$ **(pC)**	351.42	230.52	148.94
$\mathbf{S_{|\Delta q|}}$	1.95	3.55	2.06
$\mathbf{k_{|\Delta q|}}$	6.80	17.21	6.99
$\mathbf{mean_t}$ **(Sec)**	54.91	79.94	103.84
$\mathbf{S_t}$	0.55	0.20	1.07
$\mathbf{K_t}$	1.52	1.46	4.43

The relation between PD event number and the quantities identified in Table XVI for the three holds at +20 kV are illustrated in Figure 65.

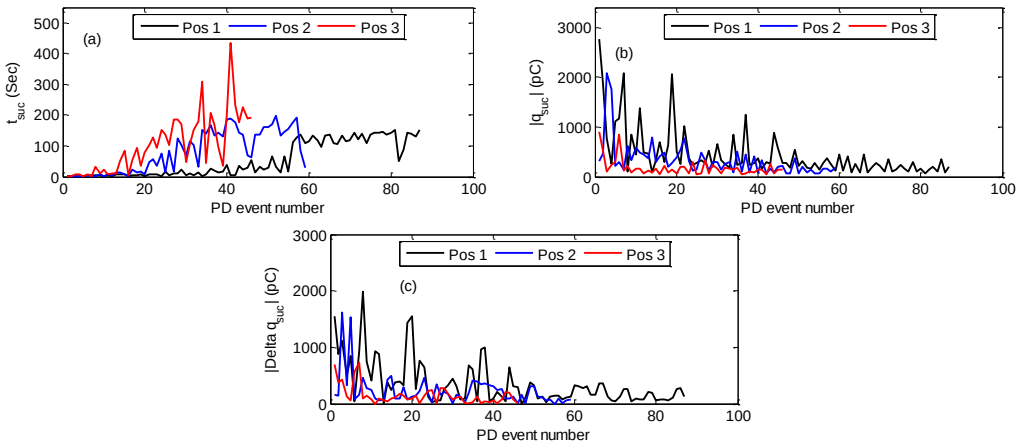


Figure 65 - Comparison of hold data at +20 kV for repeated positive ramp tests (a) PD event number versus time to successor (t_{suc}) (b) PD event number versus charge magnitude of the successor ($|q_{suc}|$) (c) PD event number versus difference in charge magnitude of the successor ($|\Delta q_{suc}|$)

The t_{suc} for the three sequential positive ramp tests varied significantly between the three tests, the general trend for all three was for t_{suc} to increase with PD event number. It became clear that less PD events occurred before the time between PD events increased during the third hold at +20 kV. The general trend for $|q_{suc}|$ and $|\Delta q_{suc}|$ was a reduction then stabilisation after a certain number of PD events. In the first hold at +20 kV the stabilisation occurred after 40-50 PD events. In contrast, after less than 10 PD events $|q_{suc}|$ and $|\Delta q_{suc}|$ were stabilised in the third hold at +20 kV. These general observations match the expected PD behaviour in terms of the capacitive and resistive grading of the insulation. PD activity in a capacitively graded insulation are generally larger and of a higher repetition rate [17]. The three quantities of interest were plotted against charge magnitude of the current PD event as shown in Figure 66.

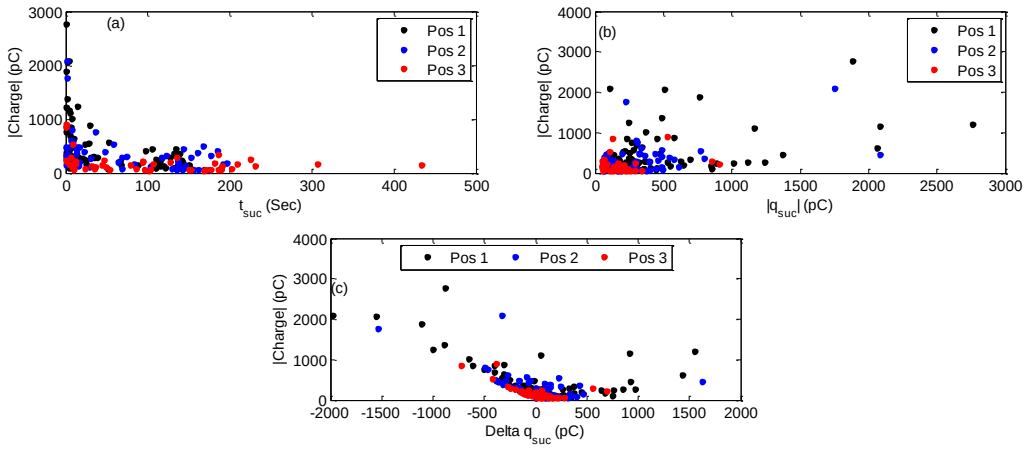


Figure 66 - Comparison of the holds at +20 kV for the three positive ramp tests (a) t_{suc} versus charge magnitude (b) $|q_{suc}|$ versus charge magnitude (c) Δq_{suc} versus charge magnitude

In Figure 66a there is a cluster for the t_{suc} range of 0-50 seconds, over this range the charge magnitude is large. A second cluster of smaller magnitude events is evident with a t_{suc} range of 50-500 seconds. In the plots of $|q_{suc}|$ and Δq_{suc} versus charge magnitude, a cluster of data was apparent for Δq_{suc} less than ±500 pC and charge magnitude less than 600 pC. The outliers are typical of the PD activity related to the capacitive grading of the insulation. $|\Delta q|$ was plotted against Δt for the three holds at +20 kV with lines included to show the relation of subsequent PD activity to the previous as shown in Figure 67.

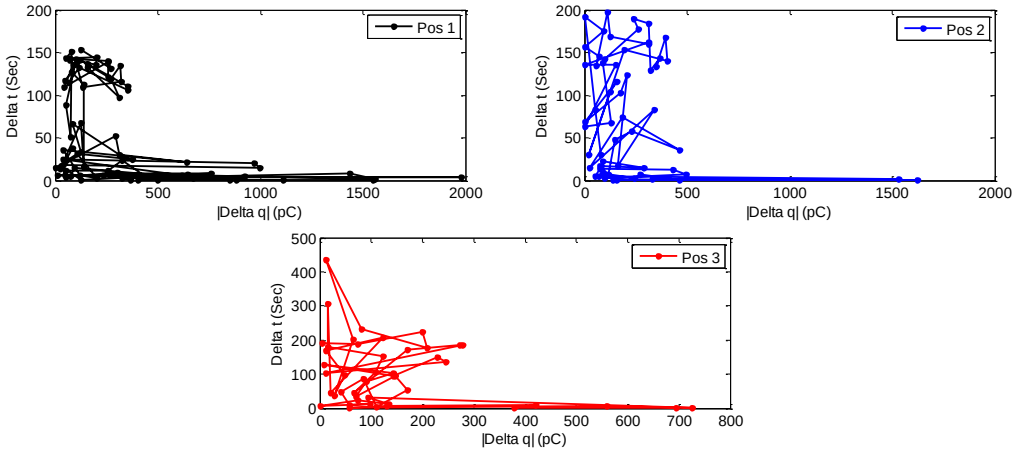


Figure 67 - $|\Delta q|$ versus Δt for the holds at +20 kV: first positive hold (Pos 1), the second positive hold (Pos 2) and the third positive hold (Pos 3).

The plots of Figure 67 are particularly revealing with all 3 showing the initially large $|\Delta q|$ PD events with short Δt between these initial PD events. This activity can be patterned through the horizontal plot lines, resulting from this initial PD activity. Following this initial activity the PD develops with a reduction in $|\Delta q|$ but increase in Δt, with the pattern of this activity being more spontaneous/vertical lines between PD events. The transition in PD behaviour matches the calculated time constant of 47.71 seconds. The difference in delay time for the starting electron has lead to a spread in Δt of 50-450 seconds. The relative spread of PD activity can be analysed in more detail through the $|\Delta q|$-Δt-N plot shown in Figure 68

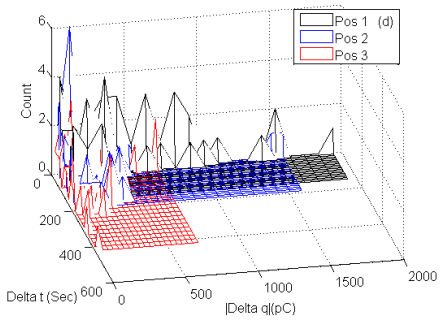


Figure 68 - $|\Delta q|$-Δt-N plot for the three holds at +20 kV

The comparison of the three holds at +20 kV on one plot, emphasised the variation from the first hold at +20 kV to the third hold at +20 kV. In the first hold at +20 kV,

PD events with a large $|\Delta q|$ and short Δt were evident in high counts, this activity occurred over the initial minutes at the hold voltage of +20 kV. In the third hold, at +20 kV, the PD activity with large $|\Delta q|$ and short Δt was significantly reduced. The repeated positive ramp tests brought about smaller $|\Delta q|$ and an increase in Δt between subsequent PD events, as further positive ramp tests were conducted on the sample. This change in PD behaviour emphasised the reduced capacitive effects inside the insulation when repeated positive ramp tests were conducted.

4.4.4. VARIATION IN POLARITY OF DC RAMP TESTS

In this section, tests were performed to study the variation of PD behaviour when the dielectric sample was subjected to DC ramp tests of varied polarity. This effectively simulates, on a longer time period, how a void type sample would respond during polarity reversal tests. A particular area of interest is how the capacitive grading of the insulation affects PD activity over the initial minutes following a voltage change.

Tests of three cycles of DC ramp tests were performed; the results and analysis are detailed.

In this study a positive ramp test was conducted, then the test circuit was adjusted to enable a negative ramp test to be performed and finally the test circuit was reverted to allow a further positive ramp test. The PD pulse count for the polarity reversal test is shown in Figure 69a and the cumulative charge plot for the three holds at ±20 kV is in Figure 69b.

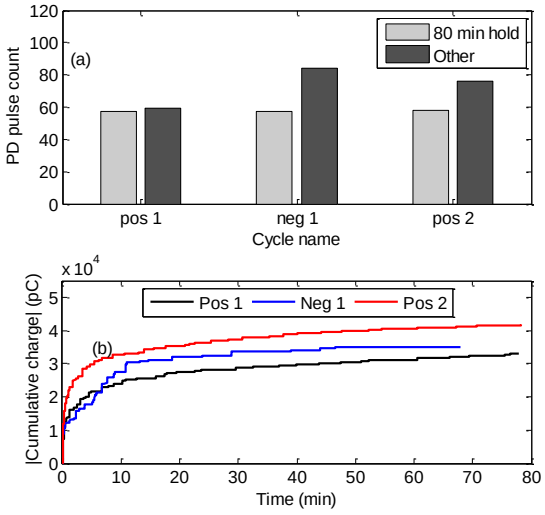


Figure 69 - Three cycle positive and negative ramp tests (a) PD pulse count for the three positive ramp tests (b) measuring time vs cumulative charge.

The largest number of PD events occurred during the negative ramp (118 PD events) and the least during the first positive voltage test (85 PD events). As expected, the positive ramps produced PD with a positive polarity and the negative ramp produced PD of a negative polarity. The plot of time versus cumulative charge (Figure 69b) details the cumulative effect of more sustained PD activity for the negative and second positive voltage ramps. The second positive ramp test shows increased PD activity over the initial minutes of the hold at +20 kV. The increased PD magnitude and repetition rate was most likely due to the capacitive grading of the insulation. The use of the negative ramp has accentuated the capacitive behaviour causing increased PD activity thereafter. An interesting observation was the difference in the shape of the cumulative charge plot between the positive hold data and the negative hold data. The positive hold has a steady almost Bowden curve, whereas, the negative has an almost straight line relation up to 10 minutes into the hold. The relative frequency and magnitude of PD events increased during and after the negative ramp test.

A summary of the charge magnitude values and time between events for the three subsequent ramp tests are detailed in Table XVII.

Table XVII - Charge magnitude ($|q|$) of PD events, difference in charge magnitude ($|\Delta q|$) and time between events (t) for three cycle positive and negative DC ramp tests

Variable	Pos 1	Neg 1	Pos 2
$Mean_{|q|}$ (pC)	581.45	615.83	721.52
$S_{|q|}$	1.05	1.53	1.70
$k_{|q|}$	2.80	4.87	5.26
$mean_{|\Delta q|}$ (pC)	322.81	579.20	464.51
$S_{|\Delta q|}$	1.38	1.42	1.16
$k_{|\Delta q|}$	3.89	4.30	3.66
$mean_t$ (Sec)	83.43	72.74	82.30
S_t	0.43	3.01	0.68
K_t	1.91	13.40	2.18

Throughout the three ramp tests with polarity variation the mean value, skewness and kurtosis all increased for charge magnitude test on test. In terms of charge difference between PD events, the largest mean value, skewness and kurtosis was evident for the hold at -20 kV. This was to be expected with the polarity variation, however it was interesting this trend was not evident in the charge magnitude data. When the time difference between PD events was considered the shortest mean time between PD events was evident for the hold at -20 kV but also the largest skewness and kurtosis was evident. The negative ramp test has had an effect on PD activity in the second positive hold at +20 kV. Evidence for this is an increase in mean PD magnitude for the second hold at +20 kV and a reduction in the mean time between PD events.

The variation of the three key quantities identified above with PD event number is illustrated in Figure 70 for the three ramp tests conducted.

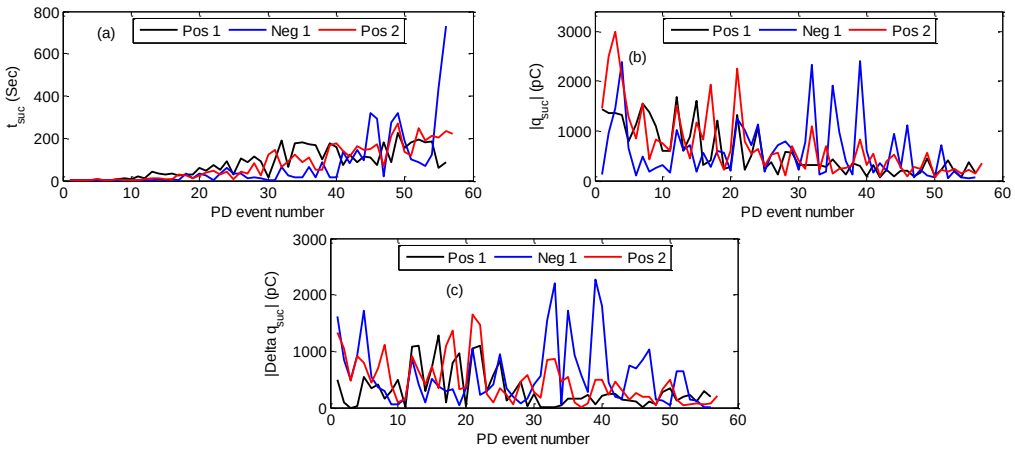


Figure 70 - Comparison of hold data at ±20 kV for the three cycle polarity variation tests (a) PD event number versus time to successor (t_{suc}) (b) PD event number versus charge magnitude of the successor ($|q_{suc}|$) (c) PD event number versus difference in charge magnitude of the successor ($|\Delta q_{suc}|$)

The variation of t_{suc} with PD event number was very similar for the two holds at +20 kV, the hold at -20 kV had some deviation throughout the 80 minute hold period. All three data sets have the general trend of t_{suc} increasing with PD event number. The main difference between the first hold at +20 kV and the two following holds, at ±20 kV, was that more PD events occurred prior to t_{suc}, increasing almost linearly. There was less PD events with a short t_{suc} during the first hold at +20 kV. This type of behaviour could be linked to an increase in the capacitive grading of the insulation

following a voltage polarity reversal. $|q_{suc}|$ and $|\Delta q_{suc}|$ generally reduced with PD event number for the three holds at ±20 kV. The reduction and stabilisation of $|q_{suc}|$ and $|\Delta q_{suc}|$ with PD event number was most evident for the first hold at +20 kV prior to any polarity variation. When the polarity was varied this reduction and stabilisation was not as clear. This could point to an extension of the time period that the insulation is capacitively graded and a subsequent delay for the insulation to transfer to being resistively graded.

The relations of the key quantities to the charge magnitude of the current PD event are illustrated in Figure 71.

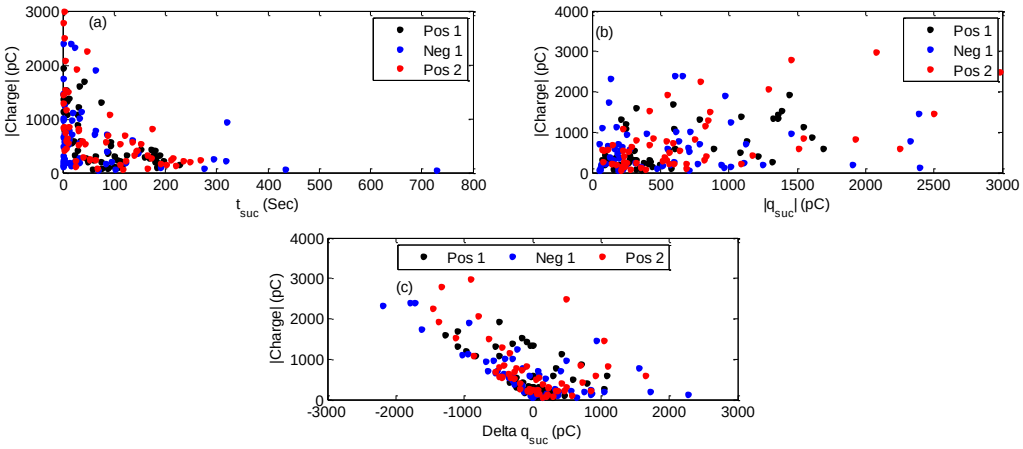


Figure 71 - Comparison of the holds at ±20 kV for the three polarity reversal ramp tests (a) t_{suc} versus charge magnitude (b) $|q_{suc}|$ versus charge magnitude (c) Δq_{suc} versus charge magnitude

The cluster for t_{suc} ranging from 0-50 seconds which was evident for the three holds at +20 kV was also evident for the three holds at ±20 kV. The data in this range of t_{suc} are generally large magnitude PD events which occur at the beginning of the 80 minute hold period which is assumed to be related to the capacitive grading of the insulation. A second cluster of smaller PD events ranges from 50-300 seconds and, outside this, there are some outliers mainly from the hold at -20 kV. The relation between $|q_{suc}|$ and magnitude of current PD pulse consists of two clusters of data:

- The first cluster being the $|q_{suc}|$ 0-400 pC and charge magnitude less than 800 pC this activity is related to the PD activity occurring when t_{suc} ranges from 50-300 seconds.

- The second of these clusters is the data which is scattered outside the first cluster which related to the PD activity occurring in quick succession (0-50 sec) at the start of the hold period.

Similar behaviour was evident when Δq_{suc} was plotted against charge magnitude. $|\Delta q|$ was plotted against Δt for the three holds at ±20 kV with lines included to show the relation of subsequent PD activity to the previous, as shown in Figure 72.

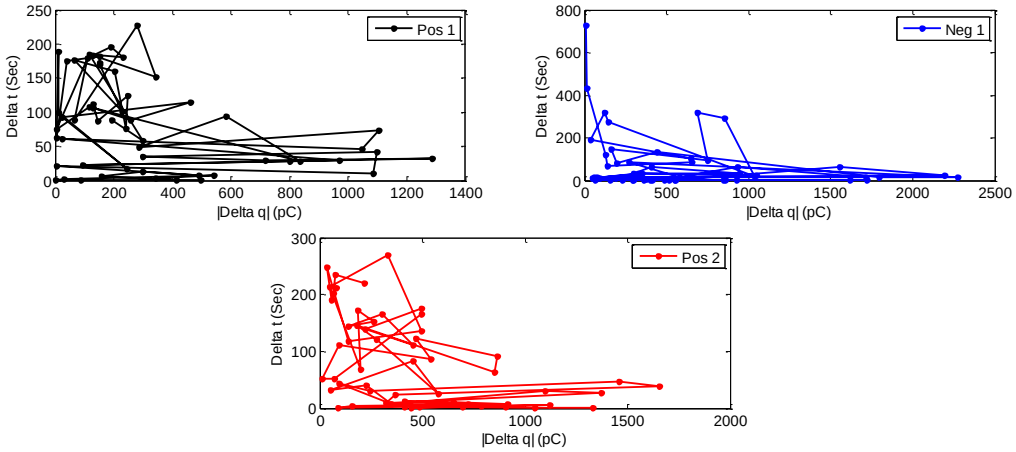


Figure 72 - $|\Delta q|$ versus Δt for the holds at ±20 kV: first positive hold (Pos 1), the first negative hold (Neg 1) and the second positive hold (Pos 2).

These plots show the development of PD activity, the main observations are that during the initially large PD activity occurring in quick succession (insulation capacitively graded) and the linking of subsequent PD activity results in horizontal traces across the $|\Delta q|/\Delta t$ plot. Following this phase the time between PD events increases and the difference in charge magnitude between PD events reduces, resulting in a trace which is more sporadic than the initial phase. This behaviour may be the transition to a resistively graded insulation. Both holds at +20 kV show these two phases, but, the hold at -20 kV appears to have a wider Δt range for the capacitive grading (0 to 180 sec) due to the polarity reversal. The transition in PD behaviour matches the calculated time constant of 47.71 seconds for the two holds at +20 kV. The difference in delay time for the starting electron has lead to a spread in Δt of 50-260 seconds for the holds at +20 kV.

The relative concentration of PD activity on the plots above can be understood through the use of a $|\Delta q|$ vs Δt vs N plot shown in Figure 73.

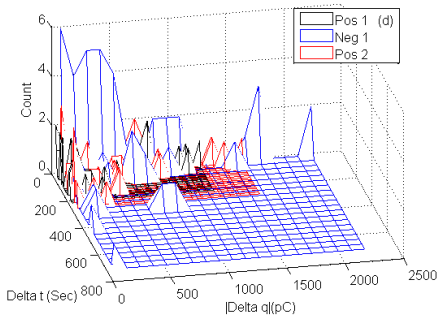


Figure 73 - $|\Delta q|$ vs Δt vs N plot for the three holds at ±20 kV

The three data sets are directly compared and the relative change in behaviour can be observed. The polarity reversal has extended the scale on the $|\Delta q|$ and the Δt axis for the hold at -20 kV and the second hold at +20 kV. Further testing consisting of 3 positive and 3 negative ramp profiles confirmed the observed behaviour held true for further polarity variations.

4.4.5. AC TEST BETWEEN TWO DC RAMP TESTS

Test standards suggest that AC testing can be conducted on DC equipment if the system design allows. This work investigates the use an AC PD test in between two positive DC ramp tests and reports on the effect on PD behaviour from the dielectric sample under test. The time period to change the test circuit from testing DC to AC and from AC to DC was 30 minutes, longer than the 2 minutes in [72] but in quick succession.

In the first DC test, 161 PD events were recorded over the full 94 minute ramp test, 80 of which were during the hold at +20 kV. The 10 second AC test resulted in 779 PD events. The PD activity observed in the AC test was of lower magnitude than the original AC PD test and the inception voltage of 9 kV rms was higher than the original of 8 kV rms. The φ-q-n plot for the AC test in this phase of testing is shown in Figure 74. The majority of PD activity is in the first and third quadrants confirming internal discharge. The PD magnitude is significantly lower than observed in the initial AC PD test. The DC ramp test prior to AC testing has had an impact on the AC PD behaviour. In the second DC ramp test, 105 PD events were recorded, 38 of the events were recorded during the 80 minute hold at +20 kV.

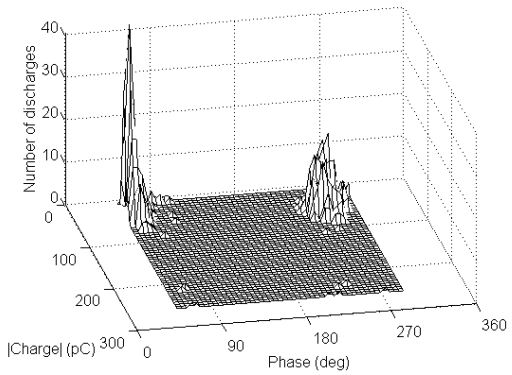


Figure 74 - AC test φ-q-n plot at 9 kV rms

The relative PD activity over the two positive DC ramp tests is detailed in Figure 75a. The cumulative PD activity for the two holds at +20 kV is shown in Figure 75b.

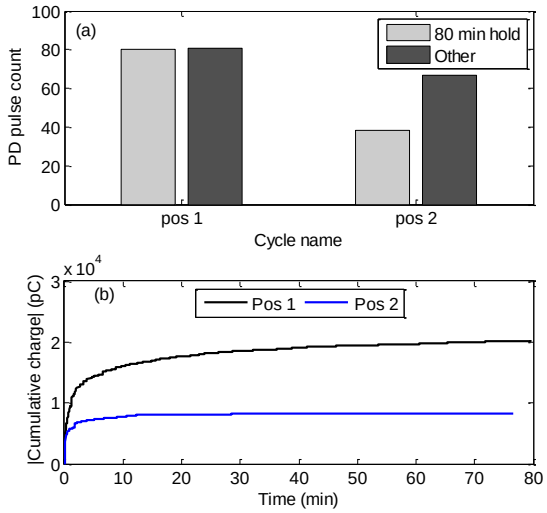


Figure 75 - Two positive ramps with an AC test in between (a) PD pulse count for the three positive ramp tests (b) measuring time vs cumulative charge.

The AC test has reduced the number of PD events recorded in the second hold at +20 kV. Inspection of Figure 75b shows that the AC test between the two DC cycles has led to a reduction in cumulative charge magnitude in the second positive test. The main change in behaviour was over the capacitive region in the first 10 minutes at +20 kV.

Table XVIII details statistical measures for charge magnitude, difference in charge magnitude and time between PD events for the two holds at +20 kV.

The mean values for $|q|$ and $|\Delta q|$ have reduced between the first and second hold at +20 kV. The skewness and kurtosis remained similar for both variables. In terms of time between PD events, the mean value increased. Skewness and kurtosis also increased with the largest change evident for the value of kurtosis. In summary, the dielectric sample was less active and, when the PD events occurred, they were generally of smaller magnitude in the second hold at +20 kV.

Table XVIII - Charge magnitude ($|q|$) of PD events, difference in charge magnitude ($|\Delta q|$) and time between events (t) for two positive ramp tests separated by an AC PD test

Variable	Pos 1	Pos 2
$Mean_{|q|}$ (pC)	253.38	217.98
$S_{|q|}$	2.63	3.02
$k_{|q|}$	13.47	13.01
$mean_{|\Delta q|}$ (pC)	176.13	163.19
$S_{|\Delta q|}$	2.76	2.83
$k_{|\Delta q|}$	12.72	12.17
$mean_t$ (Sec)	60.28	123.97
S_t	1.37	2.83
K_t	3.87	13.43

The variation of time to successor (t_{suc}), charge magnitude of the successor $|q_{suc}|$ and difference in charge magnitude to the successor ($|\Delta q_{suc}|$) are plotted against PD event number in Figure 76. Inspection of the PD event number versus t_{suc} reveals that there is a distinct difference between the first hold at +20 kV and the second hold at +20 kV. The increase in t_{suc} with PD event number, shown in the second hold at +20 kV, occurs earlier and there is a step up in t_{suc} after PD event number 33. Similar behaviour was observed when $|q_{suc}|$ and $|\Delta q_{suc}|$ were plotted against PD event number. In general, the magnitude of $|q_{suc}|$ and $|\Delta q_{suc}|$ was smaller and stabilises after 20 PD events during the second hold at +20 kV. The general trend is for t_{suc} to increase with PD event number and for $|q_{suc}|/|\Delta q_{suc}|$ to reduce or stabilise with PD event number.

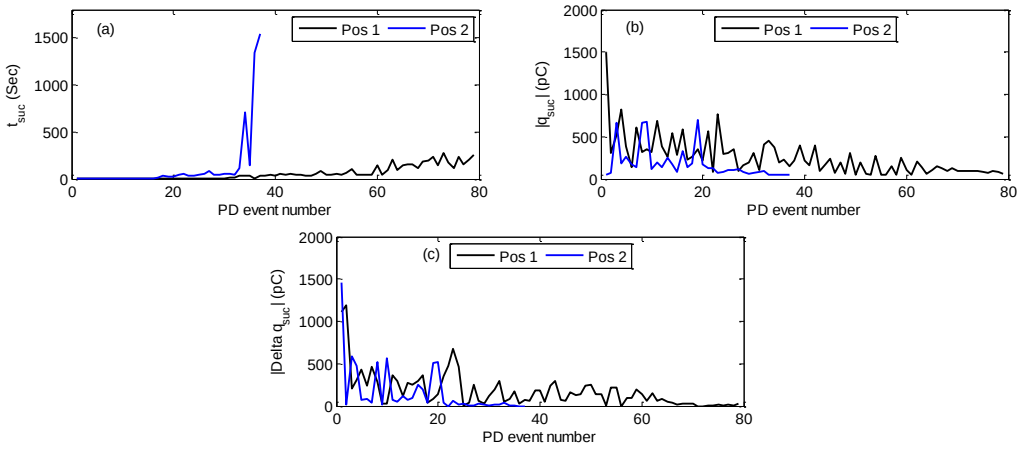


Figure 76 - Comparison of hold data at +20 kV for the two positive holds (a) PD event number versus time to successor (t_{suc}) (b) PD event number versus charge magnitude of the successor ($|q_{suc}|$) (c) PD event number versus difference in charge magnitude of the successor ($|\Delta q_{suc}|$)

The same three variables were also plotted against the current charge magnitude (Figure 77).

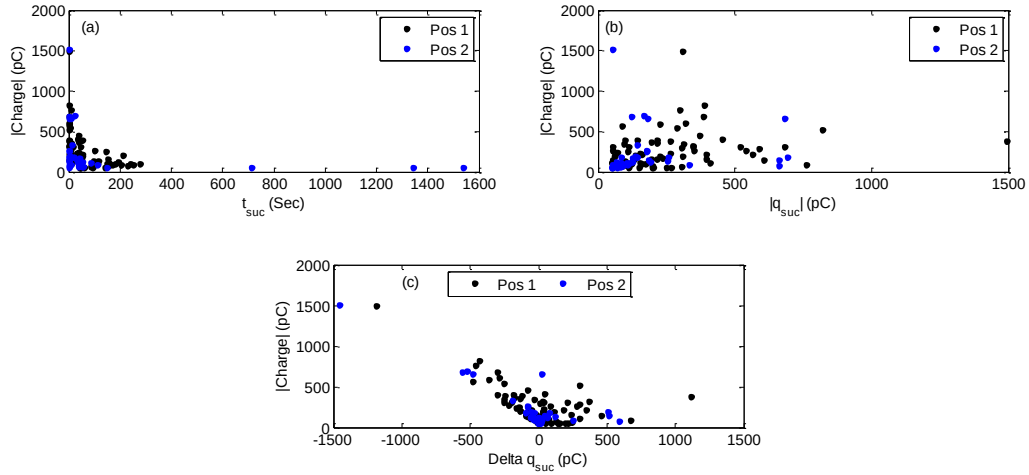


Figure 77 - Comparison of the holds at +20 kV for the two positive holds (a) t_{suc} versus charge magnitude (b) $|q_{suc}|$ versus charge magnitude (c) Δq_{suc} versus charge magnitude

The concentration of larger PD events with short time to successor (0-50 seconds) was evident in both data sets; the previously identified first cluster. There are reduced PD events for the second cluster (50-300 seconds) in the second hold, at +20 kV, following the AC energisation of the dielectric sample. In the second hold at +20 kV PD events of low magnitude occurred over more dispersed time intervals (up to 1500 seconds). The behaviour of $|q_{suc}|$ with charge magnitude confirmed previous

findings, with a cluster evident when $|q_{suc}|$ was approximately equal to the current charge magnitude. The outliers of this cluster are related to the initial 10 minutes of PD data. Similar behaviour was observed when $|\Delta q_{suc}|$ was closer to zero and charge magnitude of the current PD event was less than 300 pC.

$|\Delta q|$ was plotted against Δt for the two holds at +20 kV with lines included to show the relation of subsequent PD activity to the previous, as shown in Figure 78.

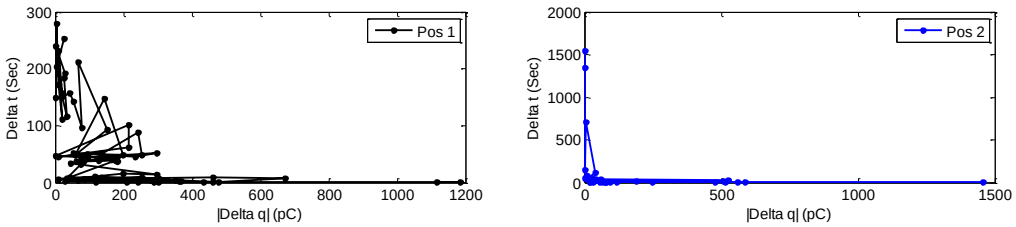


Figure 78 - $|\Delta q|$ versus Δt for the holds at +20 kV: first positive hold (Pos 1) and the second positive hold (Pos 2).

The first hold at +20 kV was consistent with previous findings, with the initial PD activity having a large range of $|\Delta q|$ and short range of Δt (0-50 seconds). Following this initial phase the PD activity develops whereby $|\Delta q|$ reduces and Δt increases. This behaviour holds for the initial phase of PD activity but in the second phase the range of $|\Delta q|$ is reduced and the range of Δt was significantly increased. This type of behaviour in the second phase was apparent when the polarity of the previous DC ramp test was opposite to the currently applied. The transition in PD behaviour matches the calculated time constant of 47.71 seconds for the first hold at +20 kV. The difference in delay time for the starting electron lead to a spread in Δt of 50-300 seconds at +20 kV. In the second hold at +20 kV the spread of Δt has increased and a range of 50-1500 seconds was apparent.

In order to better understand the distribution of data on the plot above a $|\Delta q|$ vs Δt vs N plot is detailed in Figure 79. In the first positive hold, the data is concentrated across a short Δt range but relatively wide range of $|\Delta q|$. This activity is believed to be related to the capacitive grading of the insulation. In the second positive hold, a small number of events were recorded for the region with larger Δt values and small values of $|\Delta q|$, previously termed the second phase of PD activity where the insulation should be more resistively graded. The inclusion of an AC PD test

between two positive DC ramp tests has been shown to alter the PD activity observed from a void type dielectric sample.

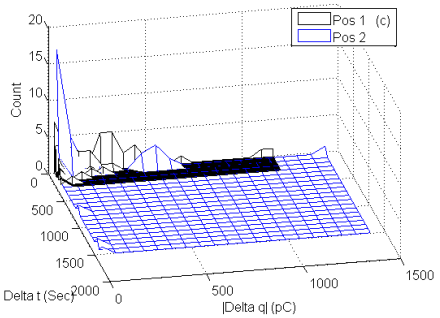


Figure 79 - $|\Delta q|$ vs Δt vs N plot for the two holds at +20 kV

4.5. DISCUSSION

A range of test cases were developed to allow the grounding period and the application of varied voltage conditions to be investigated. The main objective was to build an understanding around the behaviour of a void type sample under these varied voltage conditions.

The time constant for charging the cavity was first determined for each of the five parallel voids individually. The shortest time constant was for the largest 0.59 mm diameter void at 47.71 seconds. This is the minimum time period for the void to be charged, generally the time will be longer due to the availability of a starting electron. This calculation was used to justify the electric field grading of the insulation following a voltage change. Capacitively graded insulation will exhibit large discharges in quick succession and once this threshold has been exceeded the grading of the insulation is no longer only capacitive. This step change in PD activity was apparent throughout the range of tests presented in this chapter.

During DC PD testing a ramp test method was used on the dielectric sample under test. The ramp test method ensured:

- Repeatable tests could be applied to the dielectric sample
- The hold voltages in the ramp test method were defined by the peak value of the AC inception voltage (V_R) in initial AC PD testing of the sample
- The hold voltages used in the DC ramp test method were; $V_R/2$, V_R, $3V_R/2$ and $9V_R/5$.

- The dielectric sample was generally only active at $9V_R/5$ (20 kV)
- The data under investigation was the 80 minutes of hold data at $9V_R/5$

The grounding period between subsequent DC ramp tests on a void type dielectric sample was investigated. This topic has received limited attention to date and guidelines from previous work are very general [30]. The observations from this testing were:

- Repeated positive DC ramp tests with the grounding period prior to subsequent ramp tests varied between 3 and 32 days
- A grounding period of 7 days was found to result in similar PD activity as that of 21 and 32 days
- This work recommends that the dielectric sample under test with void type defects required a minimum of 7 days of grounding at room temperature prior to subsequent DC tests to ensure the PD activity is representative of a discharged sample
- The main indicator of a discharged sample was the behaviour apparent on a cumulative charge plot, which was used to determine the overall effect on PD behaviour during the repeated DC PD tests. Using this method, straight forward comparison could be made between the tests
- The main difference in PD behaviour was over the initial 10 minutes where the largest and most frequent PD events were recorded

The main finding from this work was that the capacitive grading of the insulation was strongly affected by the grounding period prior to the DC ramp test. If the capacitive region is important to the PD study being conducted, then the grounding period should be considered prior to commencing DC PD tests. The use, and combined use, of charge difference and time between PD events were effective in allowing two phases of PD activity to be distinguished over the 80 minute hold period. The sequence of PD events allowed the different activity to be distinguished.

The grounding period could be reduced by increasing the temperature during grounding to increase the charge mobility and reduce the requirement for extended grounding periods. This work focused on understanding how the void type sample discharged under ambient lab based conditions. Not all test samples can be exposed to elevated temperatures through external heating or heating through exposure to high currents to heat the system prior to discharging. As a result of this

some HVDC systems will discharge under atmospheric conditions meaning this testing is directly relevant.

The void type dielectric sample was exposed to repeated cycles of positive ramp tests with limited down time between subsequent ramp tests. The aim of this phase of testing was to determine the effect of repetitive applications of positive DC voltage on the PD behaviour of the void type sample. The main outcomes from this work were:

- The number of PD events and the cumulative PD over the 80 minute hold periods was shown to reduce as the sample was exposed to further positive DC ramp tests
- The main effect on PD activity was over the initial 10 minutes of the 80 minute hold period at +20 kV
- The magnitude of the PD events reduced and the time between PD events increased as the dielectric sample was exposed to repeated positive ramp tests
- The inspection of time to previous PD event versus charge magnitude revealed two clusters of data the first being the large PD events occurring in quick succession and the second cluster being the smaller and less frequent PD events.

The extension of the hold period could introduce a further cluster with longer periods to previous discharge and smaller charge magnitude. The timeline of PD activity from the capacitive region to the resistive region following a voltage change is an interesting area of investigation highlighted by this work. Limited publications have considered the transition region generally the objective of published material is to report on long term PD activity under DC conditions.

The void type sample was exposed to three ramp tests where the polarity of the ramp was reversed for each subsequent ramp test. Within the Cigre test standard there are polarity reversals which are to be conducted in a set time window of 2 minutes. The findings of this work were:

- The reversals in this case took in the region of 20 minutes for the system to be shut down grounded and the diode in the test circuit reversed before proceeding onto the next ramp test (limitation of available system)

- The shorter time between reversals will most likely produce more pronounced capacitive grading inside the insulation accentuating the effects reported in this work
- The number of PD events recorded during the 80 minute hold was highly variable when the polarity was varied
- The highest number of PD events was recorded during the hold at -20 kV and the least during the first hold at +20 kV
- The cumulative charge behaviour observed was variable in particular for the holds at -20 kV
- The largest cumulative charge measurement was for the hold at -20 kV and the least being for the first hold at +20 kV
- The cumulative charge behaviour for the holds at +20 kV was more consistent with the cumulative charge behaviour increasing test on test
- Interestingly, the shape of the cumulative charge plot for the holds at +20 kV was different to that at -20 kV
    - The cumulative charge plot for the positive hold was almost Bowden like but the cumulative charge plot for the negative hold was more of a straight line relation during the initial 10 minutes

In the final phase of testing the dielectric sample was exposed to a positive ramp, then an AC test and finally a second positive ramp test was performed. The Cigre test standard specifies that if the DC system design allows, then AC testing can be performed. The aim of this work was to determine whether the AC PD test affected the DC PD tests or vice versa. The findings were:

- The test circuit had to be altered to allow the DC testing, then the AC testing and finally the DC testing. The approximate time for changeover was 30 minutes and therefore not instantaneous
- The number of PD events recorded in the second hold at +20 kV was half of that recorded in the first positive hold
- Approximately 10 times more PD events were recorded in the 10 seconds of PD data for the AC test when compared to the first 80 minute hold at +20 kV

Interestingly, the inception voltage for sustained PD in the AC test was 9 kV rms, this was higher than the initial AC test of 8 kV. The magnitude of PD activity was also significantly lower, 0-300 pC, compared to 0-2000 pC in the initial AC test. The

PD behaviour was still internal discharge, with PD activity occurring in the first and third quadrants. The PD behaviour in the first and second holds at +20 kV was different, this is best highlighted by the plot of cumulative charge over the 80 minute hold period. The main difference was the reduction in PD activity over the first 10 minutes of the 80 min hold at +20 kV related to the capacitive grading of the insulation. There was an expectation that the AC PD test would displace the accumulated space charge and lead to significant field enhancement on the re-energisation of the sample under DC conditions. This would in theory lead to more PD events which were larger in magnitude. It may be that the elevation of the applied AC voltage has affected the availability of the starting electron. Interestingly, both the initial capacitive region and also the resistive region were affected with a reduction in PD repetition rate. It would be interesting to explore the behaviour when an AC PD test was conducted between two negative ramp tests, this may offer further insights into the behaviour observed.

4.6. CONCLUSIONS

The work presented in this chapter highlights how a void type sample behaves for different grounding periods and under varied voltage conditions. The grounding period of a void type dielectric sample prior to DC PD testing has not been investigated in detail to date.

One application where the voltage conditions are varied was for the recommended Cigre test method [72] for DC power cables. The tests of particular interest are the prequalification and type tests. These tests include load cycling and polarity reversal tests, involving voltage variation and thermal variation. An attempt has been made to understand how a void in a dielectric behaves under these types of voltage conditions. No attempt was made to include the thermal variation that the sample would have experienced during the prequalification/type testing. To date, the majority of DC PD testing on dielectric samples has been performed under steady state controlled DC conditions, this work looks to understand how the test conditions may affect PD behaviour.

The development of a time line of PD activity from a void type sample has not been considered nor presented in detail to date. The test history of the sample under test was also investigated to determine the affect the PD behaviour observed during an

80 minute hold at $9V_R/5$. In order to do this a range of test scenarios were developed and the resulting PD activity was recorded and analysed.

A review of literature was conducted on papers studying the effect of voltage variations on internal void PD behaviour. It was clear that the influence of space charge would be a factor in the testing performed therefore an understanding of the effect of space charge on PD behaviour was developed. One of the limitations of the test facilities available was that there was no means of measuring space charge. This would have allowed a visualisation of the build-up of space charge during the tests.

An area of consideration was the initial capacitive grading of the insulation following a voltage change and how the grading of the insulation transitions to be resistively graded. Publications have presented the large magnitude PD activity with high repetition rate from capacitively graded insulation samples following a voltage change [17]. No work has considered the transition region from capacitively to resistively graded insulation. The shortest time constant to charge one of the parallel voids was calculated to be 47.71 seconds. This can be employed to differentiate the initial capacitively graded insulation whereby large PD activity with short times between events was apparent. A clear step change in PD activity was consistently apparent when the time between PD events exceeded 50 seconds throughout the different tests. This can be employed to determine the time required for the capacitive PD behaviour to cease (time versus Δt plot) by applying this threshold value.

An AC PD test was first conducted as per IEC 60270 standard. The dielectric sample was confirmed to have PD behaviour consistent with that of internal voids. In this phase of testing the peak value of the AC inception voltage was determined. The inception voltage was used as an input to subsequent DC ramp tests on the sample. This initial confirmation was critical prior to conducting further testing on the sample.

The ramp test method was used throughout the DC PD testing to ensure repeatable tests could be conducted:

- The first scenario studied was the repeated application of a positive ramp with the grounding period prior to each ramp test varied by days.

- In the second case, three positive ramp tests were performed in quick succession.
- In the third case the polarity of the second ramp was negative and the first and third was positive.
- The final investigation was when and AC PD test was conducted on the sample between two positive ramp tests.

This work identified the changes in PD behaviour during these different voltage regimes. The largest effect apparent was when the insulation was capacitively graded. The main quantities of interest from this work were:

- Charge magnitude
- Difference in charge magnitude
- Time between PD events.

The analysis approaches of most use in this work were:

- Plotting cumulative charge over time
- Comparing the three quantities with PD event number
- Comparing the three quantities with charge magnitude
- The difference in charge magnitude and time difference between PD events to discern the different phases of PD activity from the sequence of PD activity
    - The use of lines on the plot to link particular activity to either the capacitive region (generally short Δt and wide range of $|\Delta q|$) or the resistive region (wide range of Δt and a more concentrated range of $|\Delta q|$)
    - Further expanded through the $|\Delta q|$-Δt-N plot allowing a visualisation of the distribution of data

The behaviour of a void type dielectric sample particularly in the capacitive region was found to be affected by:

- The grounding period
    - The behaviour was unaffected if the grounding period (at ambient temperature) was at least 7 days
- The polarity of the previously applied DC voltage

    - If the sample was exposed to repeated positive ramp tests the PD activity in the capacitive PD activity reduced in magnitude and frequency of occurrence
    - When the polarity was reversed the PD activity of the capacitive PD activity increased in magnitude and frequency of occurrence
- The application of an AC test between two positive DC ramp tests
    - Reduced the capacitive PD magnitude and frequency of occurrence

This work has shown the value in varying the applied voltage to samples and the consideration of the immediate test history of the sample under test. To date the majority of studies have considered ideal conditions for DC voltage tests, this is not the case in the real world where test history and voltage fluctuations are apparent. Understanding the behaviour of an insulation system under various regimes is critical to the monitoring of insulation condition and detection of faults.

Future work building on this study could include:

- The expansion of the capability of the high voltage lab with respect to the measurement of space charge.
- The use of alternative power supplies/test setups which allow the polarity reversal to occur within the 2 minutes defined in the test standard.
- The introduction of harmonic ripple through an alternative power supply or manual variation of the voltage applied to the test sample.
- The addition of heating cycles would be of interest.
- The expansion of the test time to similar periods as the test standard would be interesting to see if the cluster theory evolves as the test period is expanded.
- The expansion of the testing into a range of test samples, to ensure the reported behaviour is consistent for a number of similar samples.
- The sample under test was a heavily aged sample which was inherited it contained multiple voids. It would be interesting to see how a virgin sample (as a new cable sample would be) with a single void behaves during the same tests.

5. MANUFACTURING DIELECTRIC SAMPLES USING 3D PRINTING

Having looked at the behaviour of an inherited void type sample in chapters 3 and 4 the next focus of investigation is the creation of samples. This chapter details the development of a manufacture method to produce defined voids in samples using 3D printing. A review of literature is presented detailing manufacturing of voids in dielectric samples, AC/DC testing of void type samples and papers associated with 3D printing. The main currently available 3D printing methods were investigated and the most feasible solution was proposed. The design, manufacture and assembly of dielectric samples which were 3D printed are discussed in detail.

The main aim of this work was to develop a method whereby gas filled voids could be introduced inside a dielectric with a defined geometry. The main challenge of manufacturing voids inside a dielectric sample was the overhang capability of the 3D printer. When the 3D printer was forming the ceiling of the void inside the dielectric sample deformation could occur due to the print material being unsupported.

A number of different samples were designed and manufactured; samples with no defects, spherical and cylindrical voids which were later considered and compared. Paschen's law was used to predict the AC PD inception voltage for the 3D printed samples.

Building on the work in chapters 3 and 4 samples were initially tested under AC conditions and the resulting PD activity was recorded on φ-q-n plots. The sample with the most consistent PD behaviour was tested under DC conditions.

The findings of the above work will be discussed and presented in this chapter in terms of applying the test methodologies to a range of samples and drawing conclusions on the manufacture technique.

5.1. ASSOCIATED LITERATURE

The first area of investigation was to understand the current methods of introducing voids in dielectric samples for electrical testing. The primary methods of producing controlled voids inside dielectric materials are:

- The injection of air bubbles inside epoxy resin disc samples to form spherical voids

- The stacking of sheets of insulation samples and introducing holes in certain layers to form a void of defined geometry, normally cylindrical voids.

The inclusion of voids in dielectric samples has mainly been investigated under AC conditions to date. Epoxy resin is generally used when forming spherical voids, this requires skill and knowledge during the manufacturing process. This can also be a very time consuming process, especially if a number of samples are required.

Early work by Moriuchi *et al.* [89] investigated the method of inducing spherical voids of 1-2 mm in diameter inside an epoxy resin disc during the curing process. Gutfleisch *et al.* [90] also injected air bubbles during the gellation of the epoxy resin sample. In this work, a small block of cured epoxy was cut out of the main sample. The small bock was placed between two electrodes (in the desired position) and the same epoxy was used to form the remainder of the sample.

Morshuis *et al.* [91] performed AC PD testing of a 3 mm spherical void in an epoxy resin disc using the manufacturing method proposed by [90]. A variation of the method was later employed at Glasgow Caledonian University [92] and the University of Southampton [93], where a controlled volume of air was injected into the epoxy resin samples during the curing process to form a spherical void. The volume of injected air determined the size of the induced spherical void, following the casting process the void was cut out of the epoxy sample. The control of void position in the final dielectric sample was possible by performing a second casting process around the trimmed casting which included the void.

The paper [94], [95] details the AC testing of a range of spherical voids formed in epoxy resin test samples. The AC frequency, voltage and void size were varied in the study with the effects on PD activity reported. A further paper [96] from the same authors considered the modelling and experimental testing of spherical voids in epoxy. The size and temperature of the voids was varied, both parameters were found to affect the resulting PD behaviour.

A more recent publication by Fabiani *et al.* [33] uses the two step method whereby the void was first formed in a sample then cut out and a second casting process ensured that the void was formed in the middle of the final sample. Electrical aging was conducted on a range of samples, following this raman-spectroscopy and scanning electron microscope (SEM) imaging were used to detect changes in the dielectric samples.

The manufacture of cylindrical voids is a more straightforward process generally achieved by stacking thin sheets of insulators. An early publication by, Okamoto *et al.* [97], studied the behaviour of a range of cylindrical voids under AC conditions.

Danikas [98] considered the discharge current emitted from cylindrical voids of a set diameter but with varied height. The number of sheets of polyethylene was always seven and the height of the void was increased by substituting whole sheets for one with a hole.

Ramachandra *et al.* [99] investigated the behaviour of a cylindrical void in sheets of polypropylene films from capacitors.

The behaviour of a cylindrical void between sheets of LDPE insulation was studied by Mizutani *et al.* [100]. The paper mainly investigated the behaviour of cylindrical voids over time with changes in behaviour apparent over the prolonged AC testing.

Wang *et al.* [101] studied the aging behaviour of stacked film samples. A cylindrical hole was made in the middle layer which was low density polyethylene (LDPE) and this sheet was sandwiched between two sheets of cross linked polyethylene (XLPE). Great care was taken to seal the assembly in a vacuum to allow testing of the sample between two electrodes immersed in mineral oil. Generally, to date the position of the void has been in the middle of the insulation between the two plain electrodes.

Research from Montanari *et al.* [102] studied the inclusion of cylindrical voids near the surface of one of the electrodes. Differences were evident on the PRPD plot at the inception voltage after a 20 minute hold with asymmetry evident in the first and third quadrants. The lack of symmetry was less evident when the voltage was 1.5 times the inception voltage. A similar effect was evident when one of the electrode surfaces was rough leading to areas of high electric field.

Hikita *et al.* [103] modelled, then experimentally tested, void type samples. The relationship between void size and the apparent charge of PD events was modelled. An experiment was conducted to determine the inception voltage for a spherical void in epoxy resin. A lowering of the PDIV was evident when an X-ray source was positioned close to the sample under test. The X-ray source provided the starting electron for the ionisation process. Further work considering the X-ray irradiation process is presented in [104].

The comparison of PD behaviour from spherical and cylindrical voids was considered by Adhikari *et al.,* while at Glasgow Caledonian University, looking at both injected air bubbles and stacked sheets of insulation [31]. The layered cylindrical void was found to have a lower inception voltage than the naturally formed cylindrical void of the same diameter. The samples were subjected to the same voltage excitation and the PD magnitude from the cylindrical void was higher than that from the spherical void (expected due to the cylindrical void having a lower inception voltage).

An alternative method of introducing cylindrical voids was presented by Illias *et al*. [105]. The sample consisted of a steel rod, around which, an insulation layer was formed by melting LDPE granules. A hole was drilled in the LDPE insulation and was plugged by a piece of LDPE leaving a defined cylindrical void in the insulation. A sheet of copper was installed on the outside to act as the cable sheath. The behaviour observed was compared to a developed model. This technique was employed earlier by the same author to introduce a cylindrical void inside the XLPE insulation on a 22 kV cable sample [106].

Under DC conditions, the use of dielectric samples with manufactured void type defects has received less attention to date. Early work by Fromm *et al.* [18] considers the DC PD behaviour of air filled voids. The voids were formed by stacking polyethylene film samples with the middle sample having a hole forming a cylindrical void. The relation of PD activity to a developed model was investigated. The behaviour of successive discharges was also of particular interest.

Work by Rahimi *et al.* [107] investigates the DC PD behaviour of four insulation defects, one of which was a spherical void. The void sample contained a spherical void in epoxy resin. Analysis methods adopted included the use of time frequency (TF) mapping and the study of the memory effect to distinguish different PD sources.

A paper from Inburgia *et al.* [34] investigated the behaviour of a void type sample under DC test conditions. The cylindrical void was formed by stacking sheets of kapton foils. The study considered the behaviour of space charge and PD activity for a sample with no defect and the void type defect.

The consideration of void type samples under ripple conditions has received increased attention. The paper Dezenzo *et al.* [108] considers the behaviour of an

air bubble in epoxy resin during voltage ripple conditions. The PRPD analysis technique was adopted to study the results of PD activity under voltage ripple conditions. A repeating sequence was superimposed on top of the DC voltage. Two different concentrations of PD data were evident, the first was at the peak voltage, and the second region was stochastically distributed.

Romano *et al.* [109] presents analysis of a void type defect under a DC periodic (DCP) waveform. PRPD analysis was applied to the PD data due to synchronisation of the measurement system to the DCP waveform. The approach allowed the state of the insulation system under study to be characterised in less time and more PD activity was apparent than under DC conditions.

A number of papers have been published by Farg *et al.* [28], [84], [110] related to PD behaviour of void type samples under ripple conditions. The samples under test are all spherical voids in epoxy resin discs. PD activity under ripple conditions was of a higher repetition rate and was synchronised with the periodic variation of the supply voltage.

An area of interest is the types of defects that exist in cable systems, the paper from Kubota *et al.* [111] presents the development of 500 kV XLPE cables. The development of manufacturing techniques is presented. The paper highlights the variation of voids, protrusions and impurities for improvements in manufacturing techniques. Defects of several tens of μm were typical in 1975 this has reduced to less than 10 μm in 1994. The manufacturing cables are tightly controlled by standards.

2002 Ohki *et al.* [112] detail the findings from development work on a 500 kV XLPE cable system. The insulation performance in cable joints was related to the size of contaminants and voids. The permissible levels were:

- 2 mm for fabric contaminants
- 100 μm for other contaminants
- 25 μm for voids

The sampling of cable joints was more challenging than the manufacture of the cable insulation. Particular focus was placed on; process control, use of clean rooms, resin inspection and X-ray imaging of joints.

Two publications from Robinson *et al.* [13], [113] investigate the inspection of cable joints using X-ray techniques. A charged coupled device (CCD) camera was

employed to negate issues found when using X-ray film. The inclusions and voids in the joint/insulation can be imaged following manufacture/jointing. The X-ray image is overlaid onto the conventional image to allow the defects to be visualised. Alternative approaches use ultra sound to image the representative defects in cable insulation/joints [114], [115]. Commonly coupling mediums are required to reduce the impedance mismatch. Approaches to negate the coupling medium have been explored by using low frequency sensors.

2007 Mazzanti *et al.* [116] presents an aging model for insulation life. The model aims to predict the behaviour of insulation with defined defects with particular physical properties. The background of manufacturing developments is outlined. The improvements in manufacturing techniques have meant that the voids/protrusions studied range from a few microns to tens of microns.

To date the 3D printing of antennas has received significant attention for ABS [117] and PLA [118]. The ability to print complex shapes with varying degrees of fill material was of particular interest in this field to maximise the surface area of the antenna structure. 3D printing has been used in a number of studies related to the behaviour of insulation systems to date. One paper [119], used 3D printing to produce two halves of an insulator where a defect was introduced (a piece of 3M semicon tape) between the two halves of the insulator (mating face). This paper uses the 3D printed part to allow access to the central conductor and studies the effect on the electric field from the bushing when foreign materials are included. An electric field probe is moved around the bushing during energisation to measure the effect of the foreign material on the electric field at key points of the bushing.

An interesting couple of papers from Nguyen *et al.* [35], [120] investigates the behaviour of a 3D printed part with a cylindrical void. An acrylonitrile butadiene styrene (ABS) material is used in a fused deposition method (FDM) 3D printer. No support material was required during the manufacture of the air void in the insulation due to the sample being produced in two halves. The papers considered AC PD testing on the sample and prolonged testing under AC conditions, the resultant PD behaviour was shown to be internal discharge.

5.2. MANUFACTURING 3D PRINTED DIELECTRIC SAMPLES

The process of manufacturing dielectric samples with voids will be investigated in this section. The first topic is an analysis of the available 3D printing methods.

5.2.1. 3D PRINTING METHODS

The 3D printing methods currently available will be introduced and a review of each method will be conducted. The aim is to find the most appropriate method to manufacture dielectric samples with voids of a defined geometry.

A significant constraint was whether the 3D printer is available 'in house' at Strathclyde, fortunately this constraint did not adversely affect the study. Otherwise, significant costs could result from a third party 3D printing company as a significant number of samples will be required during the testing and proving of the method. The printing methods introduced in the following subsections are:

- Fused Deposition Modelling (FDM) printing
- Polyjet printing
- Stereolithography Apparatus (SLA) printing
- Selective Laser Sintering (SLS) printing

5.2.1.1. Fused deposition modelling (FDM) printing

The most common 3D printing method is that of FDM. In this approach the raw material is a roll of filament (filament diameter 1.75 mm) which is fed to a heated extruder; the extruder acts as a print head. The extruder is mounted on linear actuators enabling accurate positioning in all three axis (using x, y and z coordinates) to facilitate the building of a 3D part. The two most common filaments types for FDM printers are acrylonitrile butadiene styrene (ABS) and polylactic acid (PLA). The build volume of the 3D printer is the volume of the printer where a 3D printed part can be produced. Generally, the extruder is moved in the x and y axis and the build plate (where the material is deposited to form the part) moves in the z-axis. Some FDM 3D printers come with a heated build plate which is required for printing with ABS filament.

The main concern with producing parts using FDM is ensuring that the finished part is sealed. The printer deposits layers of filament at a set layer height, a defined fill pattern and percentage fill material. There is a possibility of leakage either between the layers or between neighbouring channels of filament. It is important to ensure that air cannot feed the void inside the part and also that no water or mineral oil can penetrate the part and affect the behaviour of the sample. Acetone is commonly used to seal and join 3D printed parts if the whole part cannot be printed in one operation (too big for the build volume of the printer). Acetone has best results on

ABS and has mixed results on different PLA filaments. Another common sealing approach is to use epoxy resin to coat the 3D printed part.

A key feature required for this study is the ability of the printer to perform printing on overhangs, this is because overhangs will exist in the curved ceiling of a spherical void or flat ceiling of a cylindrical void. Generally, FDM printers achieve the largest overhang angle prior to significant sagging in the part. In 3D printing, overhangs are either avoided, or alternatively support material is built into the design of parts to prevent any sagging of print material.

FDM printers are available 'in-house' at Strathclyde both in the design manufacture and engineering management (DMEM) department and in the Strathclyde Fablab. The most cost effective approach was to join the Fablab, using a monthly membership, and then pay material costs (55p/10g) as appropriate. The printers available at Strathclyde using this approach are: MakerBot 2, MakerBot 2X and the Leapfrog Creatr XL. The specification of the FDM 3D printers available in the Fablab are detailed in Table XIX.

Table XIX - Specifications of the FDM 3D printers available in the UoS Fablab

Key quantity	**3D printer systems available at UoS**		
	MakerBot Replicator 2	**MakerBot Replicator 2X**	**Leapfrog Creatr XL**
Min layer height (µm)	100	100	20
Max layer height (µm)	300	300	N/A
Positioning precision (µm)	x-y: 11 Z: 2.5	x-y: 11 Z: 2.5	X-Y: 17 Z: 20
Filament diameter (mm)	1.75	1.75	1.75
Build volume Length x width x height (cm)	28.5 x 15.3 x 15.5	24.6 x 15.2 x 15.5	23 x 27 x 60
Heated bed	no (so only PLA)	yes	yes

5.2.1.2. Polyjet printing

An alternative 3D printing approach is that of Polyjet from a company called Stratasys. The basic operating principles are the same as an inkjet printer. The raw material is a liquid solution which is cured when exposed to ultra violet (UV) light. The print head moves in the x and y axis, depositing thin layers, then a UV light on the print head is used to cure the deposited layer. The build plate moves in the z axis allowing the progressive layers to be deposited onto the object being printed. The main constraint with a Polyjet 3D printer is that no overhangs are permitted past 90 degrees and, as such, no dielectric sample can be made containing a void in one piece. The printer software automatically adds support material to any feature in the part requiring support (no form of user control) and as a result any dielectric sample would need to be produced as an assembly of parts. It is not possible to join Polyjet parts using acetone so a further material such as glue/bonding agent would need to be introduced. This would have further complications in terms of the electrical behaviour observed from the manufactured sample.

A Polyjet 3D printer is available 'in-house' at Strathclyde in the DMEM department. The costs are relatively high as machine time and material costs will be charged. The lack of control over the printer operation is a distinct disadvantage of this approach. The specification of the Polyjet printer available in the DMEM department is detailed in Table XX.

Table XX - Stratasys Ployjet Objet Eden 350 specification

Key quantity	**Objet Eden 350**
Min layer height (µm)	30
max layer height	N/A
positioning precision (dpi)	x-y: 600 Z: 1600
Filament dia (mm)	N/A
build volume (mm)	342 x 342 x 200
heated bed	N/A

The chemical composition of the Polyjet materials are not defined in the available data sheet, more focus is placed on the mechanical properties. To date limited work has been conducted looking into the electrical properties of Polyjet materials. Testing would be required to define the breakdown strength and dielectric properties of the Polyjet materials.

5.2.1.3. Stereolithography apparatus (SLA) printing

An alternative 3D printing approach is to use a process called sterolitography apparatus (SLA) printing. SLA uses a bath of print solution and a UV light source to solidify the build material. The curing of the liquid build material into solid layers using a UV light source is known as photopolymerization. The build floor either moves out of the bath or into the bath as the individual layers of build material are cured by the light source. SLA requires drain holes to allow uncured resin to be removed as the part is being built in a solution of build material. The liquid photopolymer resin is supplied in a cartridge and is a thermosetting plastic.

SLA would not be an appropriate process to create voids due to the need for drain holes. If SLA was used the void would need to be created using an assembly of parts, which brings with it the bonding issues previously discussed. The liquid resin and a light source can be used to bond parts together however this approach was not available ‘in house’ at Strathclyde. As such, use of this method would involve significant costs (using an external supplier) and would be inferior FDM method due to SLAs inability to create a void without an assembly of parts.

5.2.1.4. Selective laser sintering (SLS) printing

Selective laser sintering (SLS) uses a laser beam to cure powder. The laser moves through the x and y axis and is used to solidify a powder. The laser beam scans across the layer of powder and selectively sinters the powder. When a particular layer has been cured the base plate drops down and a sweeper sweeps a further layer of powder for the laser to cure. This method is similar to SLA in that access must be available post processing to remove the uncured powder (drain holes or similar) where compressed air is usually used to blow out powder residue.

As previously highlighted the need to manufacture a void by assembling parts brings with it complications that discount this as an ideal production process. This approach is not available ‘in-house’ at Strathclyde as such any fabrication would

need to be carried out by an external supplier whilst not being ideal in terms of producing a single pass void.

Having considered the various alternatives available it was concluded that the locally available FDM printers were both the technically and financially the best alternative. The use of the Fablab will allow many samples to be produced using commercially available equipment. An added advantage of the Fablab is that users learn to operate the equipment to produce their own samples without technician support which greater flexibility and rapid turnaround of samples.

5.2.2. 3D MODELLING

The component to be printed was first designed in a 3D modelling package. Autodesk offer free student licences and the Autodesk Inventor package is a common 3D modelling packages used in industry. The part is modelled by sketching geometries in the x-y planes then extruding/revolving the sketches in the z axis to form a 3D part. Two different models were developed;

- A void formed in one piece
- An assembly of parts

The 3D models were generated for each approach, then they were exported as an standard triangle language (STL) file which is used as an input file to the 3D printer. The file allows the printer software to map the slices of the 3D part to be printed. The printer software derives the G-code commands for the x, y and z coordinates for the print head during the printing process. G-code is commonly used in programming computer numerically controlled (CNC) equipment. The single piece and assembly of parts models will be introduced in the following subsections.

5.2.2.1. Single piece assembly

Using Inventor a void can be modelled inside a disc using the ‘revolve’ modelling command. Initially a half slice through the thickness of the disk is sketched (light blue outline) and the profile is revolved around the z-axis (Figure 80).

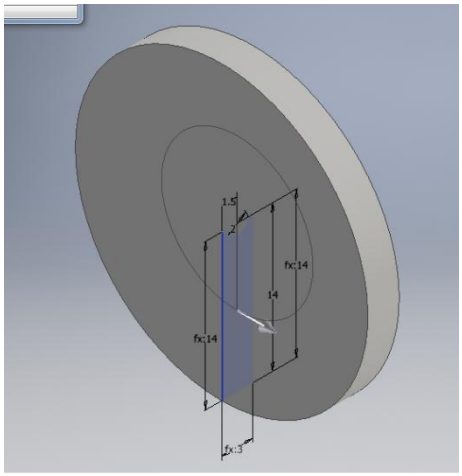


Figure 80 - Revolve of single part (spherical void) blue shaded section is the initial sketch to be revolved into the disc containing a void

This method enables a disk with a defined geometry of void, to be formed in one piece. This approach was successfully used to develop the models for a single piece disc with both cylindrical and spherical cavities. The samples will be printed to test the overhang capability of the FDM 3D printer.

5.2.2.2. Multiple part assembly

The approach of creating the void in the dielectric sample using multiple parts is investigated in this section. This method would be used if the void could not be formed in one piece due to deformation during 3D printing of the overhang in the ceiling of the void. A number of options were available to form the dielectric sample in an assembly of parts. The first of which (Figure 81a) was to use the method adopted by Nguyen *et al.* [35], [120] which was to 3D print the sample in two half discs then join using acetone bonding for ABS. The second approach was to form a disc with a hole right through it and use two pins with a half sphere revolved out of it (Figure 81b) so that when the two pins were inserted a spherical void was formed.

Having experimented with both methods the most appropriate approach was to form the sample in an upper and lower half similar to that adopted by Nguyen *et al.*. The key advantage was that the parts were easier to align during assembly and subsequent sealing of the part from the environment.

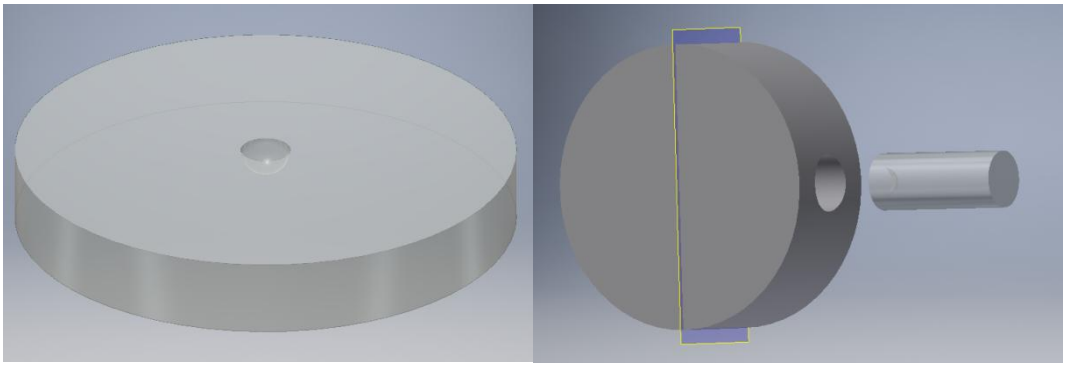


Figure 81 - Dielectric sample as an assembly of parts (a) two half discs joined to form a complete cylindrical void (b) disc with a hole through it and a pin with the void geometry revolved out the end

5.2.3. SAMPLE MANUFACTURE

This section details the investigations of printing parts using a MakerBot replicator 2X FDM 3D printer. The filament chosen for the FDM machine was ABS due to the dielectric behaviour of this plastic. The process of setting up the printer, the material and initial trial runs of 3D printed samples will be discussed in this section.

5.2.3.1. 3D printing process

The final step in the modelling process was to export the 3D model from Autodesk Inventor as an STL file. An STL file details the triangular surfaces that make up a 3D model. The STL file was the input file accepted by the MakerBot printer software, enabling the model to be imported into the MakerBot desktop software. In this package the model is imported and scaled to the desired size and the orientation of the part on the print bed can be set (important for the half disc samples). The location at which the print takes place on the print bed can also be specified. Generally, the front edge of the print bed was more successful on the available printer. An image of a part (light grey disc) on the print bed (dark grey square grid) is shown in Figure 82.

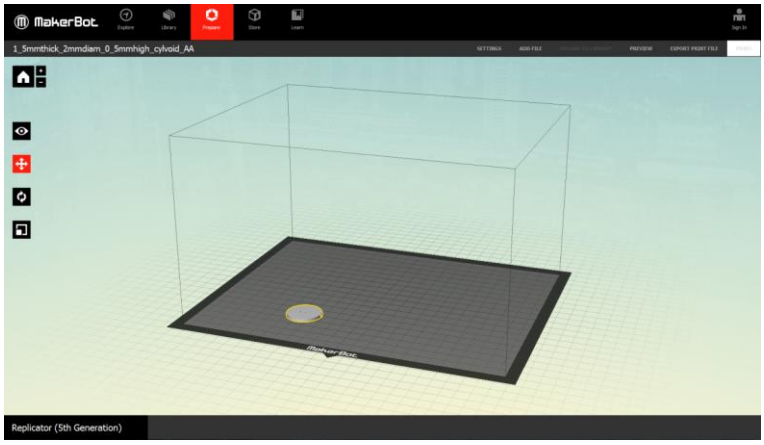


Figure 82 - Disc in the MakerBot software prior to printing (max build volume shown by black hairlines)

With the print location specified, the part in the correct orientation and the part scaled to the desired size the print settings can be chosen. Figure 83 shows the print settings window.

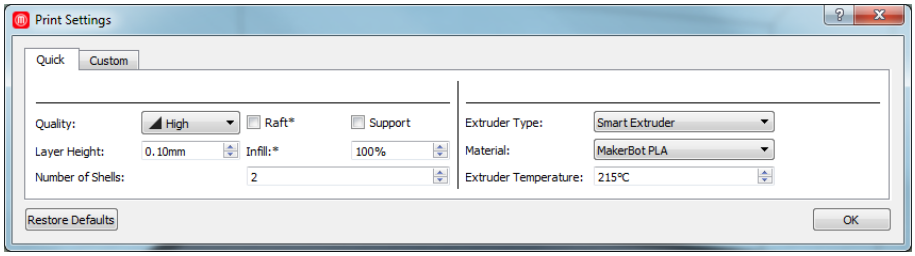


Figure 83 - Print settings window in the MakerBot software

'Quality' is the first option, the program provides 3 settings; low, standard and high. In all samples the high quality setting was used which sets the layer height of print material to the minimum of 0.1 mm (maximum of 0.3 mm). The 'number of shells' setting sets the number of outlines of the intended part that the printer will do, Figure 84 shows a print with 2 shells in the print preview mode.

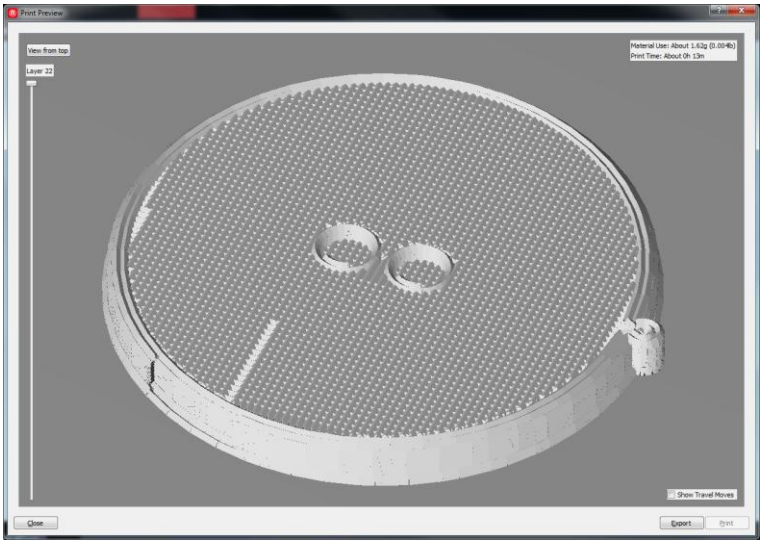


Figure 84 - Print preview in MakerBot software (view of a 2 shell part with two cylindrical voids)

The ‘Raft’ selector option (which can be enabled or disabled) results in a large base being printed to prevent the part warping. Whilst providing a more stable sample this option was found to use a large amount of print material if a number of samples are being produced. An illustration of a raft is shown in Figure 85 in the print preview mode.

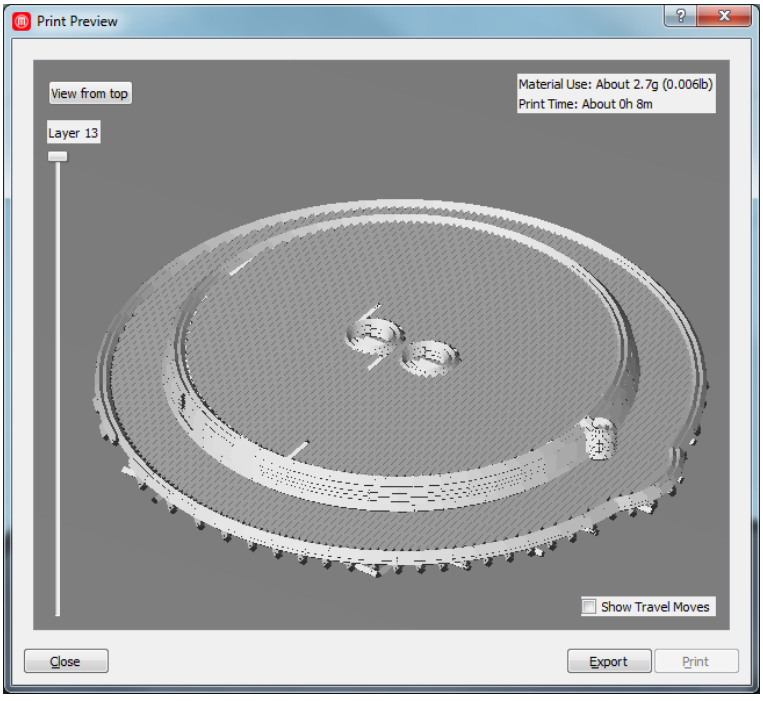


Figure 85 - Print preview in MakerBot software (showing a raft below the sample)

Whilst warping was an issue, this could be overcome by the inclusion of a sacrificial layer (later sanded away) negated any warpage and the need to use a raft. The ‘support’ option selector in MakerBot can be selected to add structural supports. As structural supports would fill the void space, this option could not be used in this application.

MakerBots ‘infill’ setting allows the % volume of print material to be specified by the user. 100 % infill was used in all samples to avoid air filled voids to be dispersed through the volume of the part. The ‘material’ type selector was always set to MakerBot ABS and the ‘extruder temperature’ setting was set to 230 °C. More advanced custom settings are available allowing a wide range of parameters to be modified an illustration of some of the settings are detailed in Figure 86.

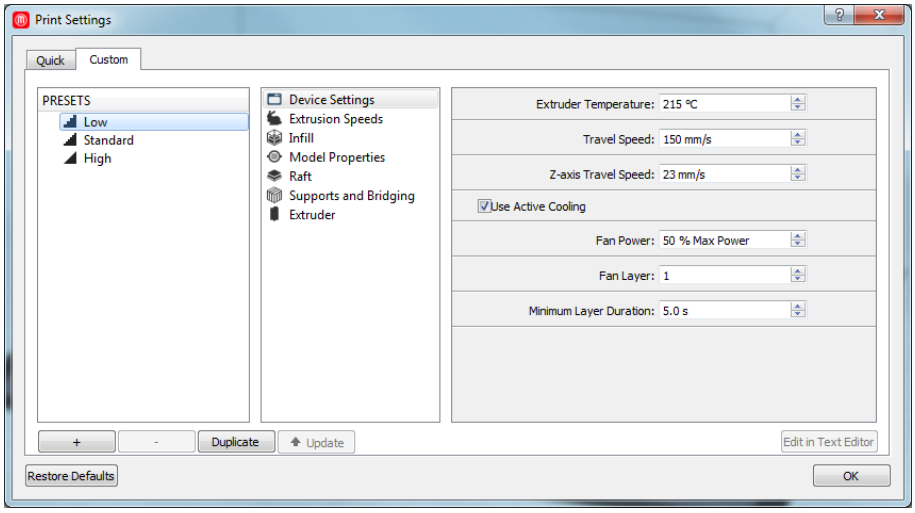


Figure 86 - MakerBot custom print settings window

The ‘print preview’ option allows the individual print layers to be viewed and the ‘travel moves’ (can be enabled) to see how the printer plans to deposit the print material. The ‘print preview’ mode also approximates the material use (by weight) and the projected print time for the part.

The first step in the 3D printing process is to level the build plate of the 3D printer. Levelling is achieved by placing a sheet of paper on the build plate and selecting the ‘utilities’ section of the menu on the MakerBot replicator printer. The user must make sure that no print filament has remained on the printer nozzle from a previous job as

this can void the levelling process and lead to the build plate being too far away from the print head. The printer utility leads the user through the process by systematically moving the print head round the build plate where the user can adjust the mountings on the build plate. A sheet of paper is used as a spacer between the print head/build plate, the user should feel some resistance when moving the paper spacer. If the build plate is too close to the print head then the print material can block the nozzle and back up inside the print head. If the build plate is not level a failure often occurred while depositing the first layer. If the build plate is too far away from the print head then the first layer will not properly adhere to the build plate and significant warping will occur if the part manages to stick to the build plate.

With the levelling complete the user can export the print file to the printer from the MakerBot desktop. The MakerBot replicator 2X printer will take 5-10 minutes to heat the build plate to 110 °C and the printer nozzle to 230 °C. Best adhesion between the 3D printed part and the build plate was found when a mix of ABS and PLA filament dissolved in acetone was coated on the build plate. This was especially effective when applied in the final stages of heating the build plate, with the mix only needing to be applied to the points on the build plate where the parts will be printed.

Between four and six samples were produced in one batch to save time in manufacturing the dielectric samples. Pronounced warping was a problem when too many samples were present in one batch. The parts quickly cooled between layers getting deposited and this lead to more pronounced warping and in extreme cases print failures. The cooling leads to tension building between subsequent layers in the structure of the 3D printed part.

5.2.3.2. Print material

The two most popular filament materials are Acrylonitrile butadiene styrene (ABS) and Polylactic Acid (PLA). Both are available at Strathclyde and are described below.

5.2.3.2.1. Acrylonitrile butadiene styrene (ABS)

ABS is a thermoplastic that can be easily recycled by reheating and as a result ABS is a popular 3D print filament. ABS requires a 3D printer with a heated build plate to ensure the deposited print layers remain warm to prevent warping. An added benefit of ABS is that separate parts can be joined using acetone and also vapour sealed which allows the production of watertight 3D printed parts. To date the application of

3D printed parts are mainly limited to mechanical applications and, as such, limited electrical data is available from material manufacturers. When no data was available, published sources were used for the key properties of ABS as listed in Table XXI.

Table XXI - Key properties of ABS plastic [121], [122]

Property	Value
Composition (%)	ABS resin=98, Styrene=0.1
Dielectric constant (ε_r)	3.2-3.3
Conductivity (S/m)	$1x10^{-13}$
Breakdown voltage (kV/mm)	20-25
Melting point (°C)	softens above 100
Decomposition (°C)	>250

5.2.3.2.2. Polylactic Acid (PLA)

PLA is a popular filament material used in 3D printing as it is a biodegradable thermoplastic, derived from renewable resources such as corn starch. The main benefit of PLA is that the printer does not need a heated build plate. The main drawback is that vapour smoothing cannot always be applied to PLA parts, as the chemical reaction is very dependent on the filament manufacturer. A further disadvantage is that the joining of PLA parts is not as easy as ABS plastic. The data sheets from the filament manufacturers are again more focused on the mechanical specifications of PLA. Where no data was available published electrical properties of PLA were substituted. The properties of PLA are detailed in Table XXII.

The electrical properties of epoxy resin, the most common manufacturing approach used to date for void samples, are very similar to that of ABS. A typical dielectric constant is 3.5 [31] and breakdown voltage of 19.7 kV/mm [123].

Table XXII - Key properties of PLA plastic [124]–[126]

Property	Value
Composition (%)	1,4-Dioxane-2,5-dione, 3,6-dimethyl-, (3R-cis)-, polymer with (3S-cis)-3,6-dimethyl-1,4-dioxane-2,5-dione and trans-3,6-dimethyl-1,4-dioxane-2,5-dione > 98
Dielectric constant (ε_r)	3.1
Conductivity (S/m)	$1.8x10^{-16}$
Breakdown voltage (kV/mm)	24.5-31.5
Melting point (°C)	150-180
Decomposition (°C)	>250

5.2.3.3. Manufacture of samples

This section outlines the findings from manufacturing the samples using the two methods discussed previously. The generic steps in the manufacture process will be outlined first.

One clear observation was the relative roughness of the upper face of the printed part and the possibility of unevenness of the face on the print bed. This was solved by adding 'sacrificial' print material to the upper and lower faces of the 3D model (Figure 87) material was later removed. The provision of a 0.3 mm sacrificial layer was sufficient to obtain a suitably smooth surface after dry sanding.

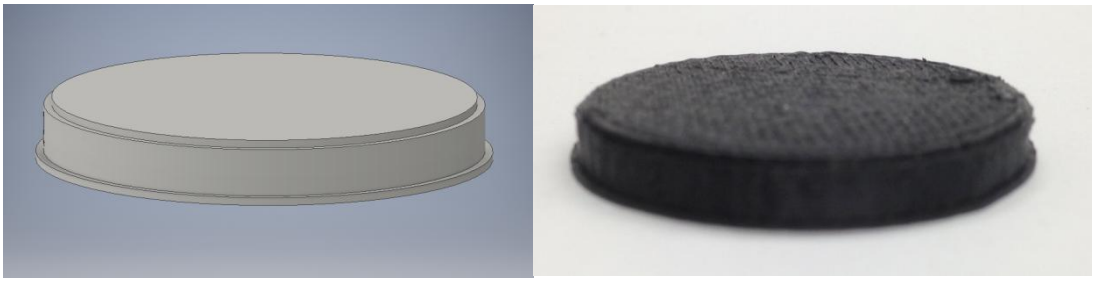


Figure 87 - Sacrificial layers added to the upper and lower faces of the insulation sample

An effective smoothing process was to start with 120 grit paper, to remove the bulk of the sacrificial layer, then follow with 320 grit paper and finally use 1000 grit paper.

ABS filament will absorb water, to avoid this, smoothed surfaces were treated and sealed with acetone rather than introducing further material to seal the surface. The acetone was applied using a brush to provide an even coat across each face. Lacquer or epoxy filler would smooth the surface but would introduce a further triple junction. The acetone melts the surface then evaporates to leave a sealed water tight surface.

Figure 88 - One piece sample images; raw printed part with sacrificial material (left) sample following the sanding process (middle) and sample following the vapour sealing process (right)

The specific findings of the two methods will be discussed in the following subsections.

5.2.3.3.1. Void in one piece

Initially an ABS spherical void sample was printed then cut in half to confirm the presence and quality of the void. The cross sectional view is detailed in Figure 89.

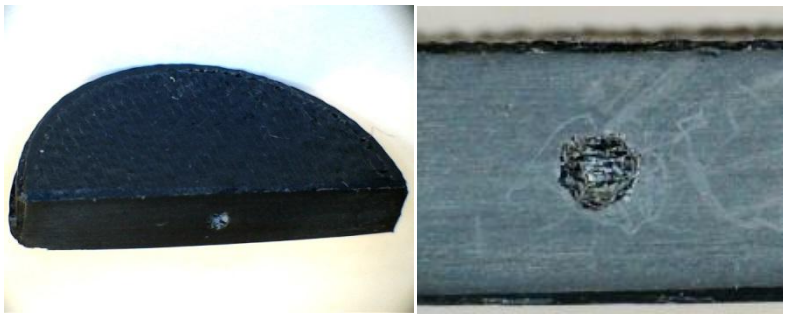


Figure 89 - Single piece 2 mm spherical void cross sectional view

The cross sectional view shows that there is some deformation apparent in the upper face of the spherical void cavity. It was deduced that this had occurred as a result of the printing process, when no support material was used. As a further

check a two test pieces were made, this consisted of two half discs printed in two ways:

- The lower half to illustrate the bowl part of the sphere (Figure 90a)
- The upper half (Figure 90b) to represent the ceiling of the spherical void.

Figure 90 - 2 mm spherical void in two halves (a) lower half (b) upper half

The test pieces show that a spherical void was being created inside the dielectric sample using an FDM 3D printer. Some deformation was evident when forming the ceiling of the spherical void.

The second void introduced in a single piece sample was that of a cylindrical void. The dimensions were set the same as the paper by Nguyen *et al.* [35] to enable comparison of AC test results. A 180° slice of a disc with a cylindrical void was manufactured and on close examination, it was evident that the ceiling of the cylindrical void had sagged during the print process. Images of the 180° slice of a disc with a cylindrical void are illustrated in Figure 91.

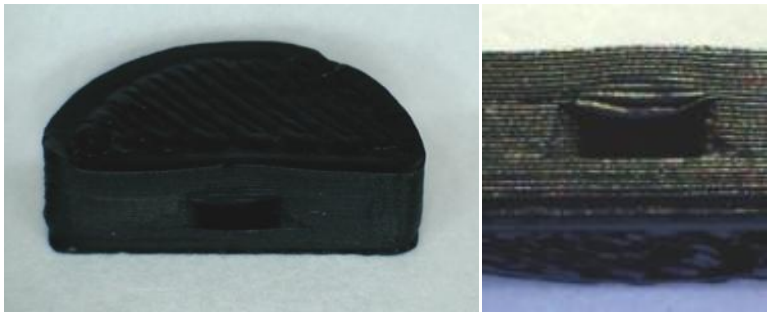


Figure 91 - 180° slice of a disc with a cylindrical void of 2 mm diameter and 1 mm high

This sample configuration resulted in the void ceiling suffering with the print layers separating, leading to further smaller voids in the dip in the ceiling. Based on this initial sample it was apparent that producing a cylindrical void in one piece was not as viable as a spherical void.

5.2.3.3.2. Void in two halves

To avoid issues with sagging and layer separation reported previously, samples were manufactured in half discs with the intended void on the upper face of the part. Figure 92 shows the designed and printed half discs.

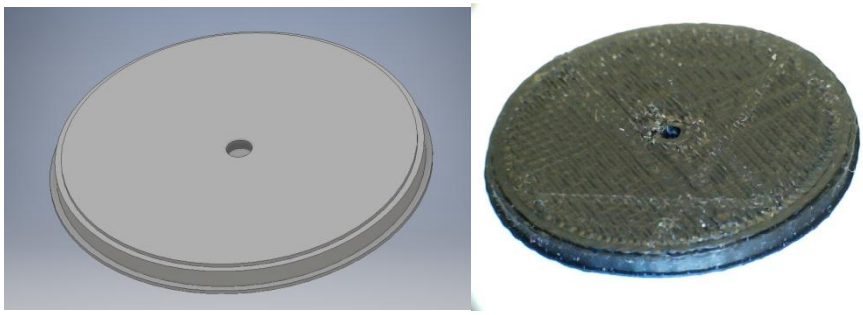


Figure 92 - Half disc single void; 3D model of the half disc (left) and raw printed prior to sanding process (right)

Following the printing process the two half discs are brought together to form a full disc with a void midway through the sample. The benefit from this method is that the void has no overhangs. The same method can be used to produce both cylindrical and spherical voids. The half discs also incorporate the sacrificial material (0.3 mm on each face) to allow smoothing prior to joining the two parts to form the dielectric sample.

The joining process involves the use of acetone initially the parts are carefully cleaned and extra care was taken to ensure no debris was inside the void itself. The next step involves the joining, acetone was liberally applied to one face and the second was quickly mated to this part, care is taken to ensure that the parts are well aligned and pressure was applied to ensure good adhesion. The part was put under a weight for 5-10 minutes while the acetone evaporated and the ABS junction solidified.

Figure 93 - Joining process (a) sanding of upper and lower faces to remove sacrificial material on each half sample(b) half samples prior to joining process

The next step was to use acetone to seal round the circumference of the sample (the mating point of the two halves) the action of the acetone moulds the two parts together. The final step was the vapour smoothing of the upper and lower faces of the dielectric sample where an even coating of acetone is applied to the two faces individually.

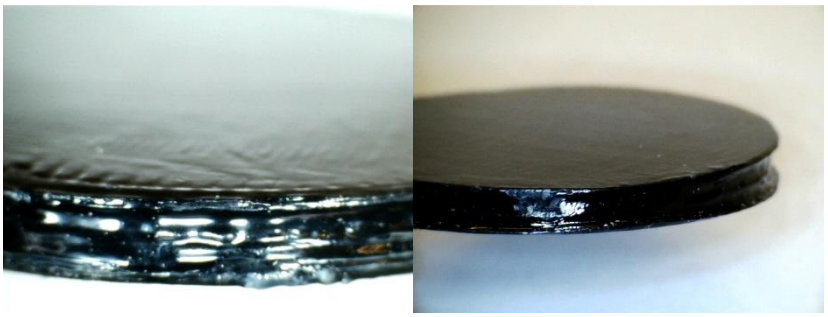


Figure 94 - Detailed view of joint between the two discs (following vapour smoothing)

This method ensures that the void was formed and was unaffected by any sagging during the printing process. This approach does have the possibility of introducing a void or alien particles during the joining process. The method is valid for any void geometry.

Samples with spherical and cylindrical voids were manufactured to allow the testing described in the following sections. Table XXIII details the samples produced using the two methods.

Table XXIII - Sample types produced during manufacturing (Manuf. Method 1 = 1 piece, 2 = 2 piece)

Manuf. method	Defect type	Defect size (mm)	Thickness (mm)	Sample ID's
1	None	N/A	3	No void A and B
	Spherical	2	4	Spherical void D and E
	Cylindrical	2x1 (dia.xhei.)	3	No samples made
2	None	N/A	3	No void C and D
	Spherical	2	4	Spherical void C, F, G, H and I
	Cylindrical	2x1 (dia.xhei.)	3	Cylindrical void A, B, C, D and E

5.3. PD INCEPTION VOLTAGE

Predictions for the PD inception voltage under AC conditions were made using Paschen's law for the two defect types introduced above. Paschen's law has been previously used to predict the breakdown voltage for gas filled voids. The breakdown voltage depends on some key properties of the void; the pressure (*P*) of the gas inside the void and the height of the void (*L*). According to Paschen's law the breakdown voltage of a gas filled void is a function of the pressure and the height of the void *V=f(PL)*. The breakdown strength (E_g) of the gas inside the void can be determined using the following derived from test data using Paschen's curve.

$$\frac{E_g}{P} = A + \left[\frac{B}{(PL)^C}\right] \tag{28}$$

Where A, B and C are constants for a fixed range of *PL* values which are only valid for air. Available literature [127] provided values of A=30.25 kV/Kpa, B=3.12 kV and C=0.675. The void pressure is estimated based on available literature [127]. The above relation was used to determine the breakdown strength of the void in question. The inception voltage (V_i) can be derived from equation (29) and the previously calculated E_g.

$$V_i = \frac{E_g[G + L(\varepsilon_r - 1)]}{\varepsilon_r} \quad (29)$$

Where *G* was the insulation thickness and ε_r was the relative permittivity of the insulation material.

A key additional factor for AC PD inception is the introduction of the free electron to start the ionisation process. A time lag may exist before the free electron appears to begin the ionisation process, central to the initiation of PD. As such the inception voltage of PD may be higher than the prediction from Paschen's law. This method was used to predict the inception voltage for the two defects manufactured using 3D printing.

The inception voltages for the spherical and cylindrical void defects were simulated. The thickness of the individual samples will vary due to the manufacturing process but the intended sample thickness was assumed. The relative permittivity was assumed to be the mid-range value from the reference material. The air pressure was assumed to be atmospheric pressure as the void was formed in air at atmospheric pressure. The variables used as an input to the calculations are detailed in Table XXIV.

Table XXIV - Paschen's law model data for spherical and cylindrical voids

Variable (identifier)	Defect type	
	Spherical void	**Cylindrical void**
***G* (m)**	$4x10^{-3}$	$3x10^{-3}$
$\boldsymbol{\varepsilon_r}$	3.25	3.25
***P* (kPa)**	100	100
***L* (m)**	$2x10^{-3}$	$1x10^{-3}$

Initially *PL* was calculated to allow variable A, B and C to be determined. This enabled the breakdown strength of the gas inside the void to be calculated using equation 28. Finally, the inception voltage could be calculated using equation 29. Table XXV details the results from the calculations.

Table XXV - Results from calculations using Paschen's law for spherical and cylindrical voids

Variable (identifier)	Defect type	
	Spherical void	cylindrical void
***PL* (kPa.m)**	0.2	0.1
***A* (kV/kPa.m)**	30.25	30.25
***B* (kV)**	3.12	3.12
C	0.675	0.675
E_g (kV/m)	3.95×10^3	4.5×10^3
V_i (kV)	10.3	7.3

The prediction of inception voltage for the spherical void was 10.3 kV rms and the cylindrical void was 7.3 kV rms. Both predictions were well below the dielectric strength of ABS (20 kV/mm). A summary of the inception voltages for the samples tested under AC conditions are detailed in Table XXVI.

Table XXVI - Samples with defects tested under AC conditions and PDIV according to Paschen's law

Defect	Defect size (mm)	Thickness (mm)	Sample ID's	Predicted inception voltage (kV rms)
None	N/A	3	No void A, B, C and D	N/A
Spherical	2	4	Spherical void C, D, E, F, G and H	10.3
Cylindrical	2x1 (dia.xhei.)	3	Cylindrical void A, B and C	7.3

5.4. TEST METHODS

This section details the test cell and the experimental methods employed in testing the dielectric samples under AC and DC excitation.

5.4.1. TEST CELL

A test cell was manufactured to enable dielectric samples to be tested, the test setup is shown in Figure 95.

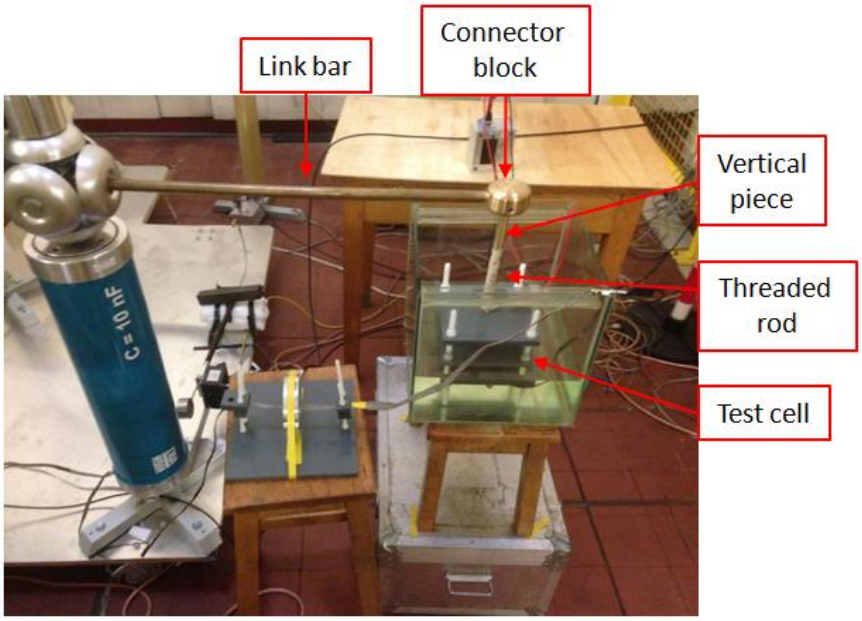


Figure 95 - Test cell immersed in the oil bath and high voltage connection

The test cell was comprised of:

- Two plates which are joined to one another using M10 nylon threaded rod (also act as legs)
- The plates have an M8 thread cut into the centre this accepts the M8 threaded rods that are mounted to the upper and lower plain electrodes
- The electrodes are made of a 19 mm in diameter brass rod, 10 mm high and have a 5 mm radius of curvature on the mating face
- The test cell was also immersed in a bath of mineral oil to minimise the effect of the triple junction between air, electrode and dielectric sample.

The connection between the coupling capacitor and the test cell consisted of:

- A link bar (650 mm long) which goes from the corona cap on the coupling capacitor to the connector block
- The connector block (60 mm in diameter and 40 mm high), allows the downwards connection
- The final connection to the threaded rod on the test cell is made via a brass vertical piece (100 mm long and 19 mm in diameter)

- In the connector block pockets allow the insertion of the vertical piece/link bar and grub screws enable the mechanical fixing of the parts to one another

In each electrical test a set torque (0.3 Nm) was applied to the upper electrode to ensure constant pressure was applied to each test sample.

5.4.2. AC TEST METHOD

This sub-section discusses the method applied to determine the inception voltage of sustained PD activity from dielectric samples whilst under AC excitation. A further goal of the AC tests was to confirm the dominant source of PD from the three dielectric samples under test. The test circuit was the same as used in chapter 3.

5.4.3.DC TEST METHOD

The DC test method will be discussed in this sub-section. The IEC 60270 standard test circuit was the same as used in chapter 3. The PD activity was recorded using:

- An IEC standard PD measurement system (bandwidth 100-400 kHz) was used to record PD activity
- A High Frequency Current Transformer (HFCT) detected the PD pulses (transfer impedance of 4.3 Ω and a bandwidth of 100 kHz to 20 MHz)
- A pulse injection calibration unit was used to ensure the output from the HFCT could be quantified as an apparent charge on the IEC 60270 measuring system.

An essential part of the DC testing is the ramp test profile. The ramp test, as discussed in chapter 3, uses the inception voltage under AC conditions (peak value) as an input (this voltage is termed V_R). The ramp test consists of three voltage steps where the voltage is held ($V_R/2$, V_R and $3V_R/2$) constant for 30 minutes.

5.5. TEST RESULTS

This section details the results from testing the dielectric samples under AC and DC excitation. Initially tests were performed under AC conditions and

5.5.1.AC TEST RESULTS

AC testing was performed to confirm the dominant PD source in the dielectric sample under test. Two different manufacturing approaches were considered; the first approach was to make the sample in one piece and the second was to make

the sample in two halves. Three design types were manufactured for each manufacturing approach: a sample containing no defect, a sample with a spherical void and a batch with cylindrical void. For each design type three individual samples were produced. The data under analysis was the 30 seconds of PD data at the PD inception voltage. The results are summarised in Table XXVII.

Table XXVII - Summary table for AC PD testing on manufactured samples (Manuf. Method 1 = 1 piece, 2 = 2 piece)

Defect [Manuf.]	Sample ID	Defect size (mm)	Thickness (mm)	Predicted inception voltage (kV rms)	Actual inception voltage (kV rms)
None [1]	A	N/A	3	N/A	14.1
	B				14.2
None [2]	C				14
	D				11.8
Sph. [1]	D	2	4	10.3	10.1
	E				10.3
Sph. [2]	C				9
	F				9.2
	G				9.1
	H				9.2
Cyl. [2]	A	2x1 (dia.xhei.)	3	7.3	7.3
	B				7.4
	C				7.3

The AC test results and φ-q-n are discussed in the following sections.

Samples with no manufactured defect, this was to confirm that the test set-up was PD free and no spurious PD was apparent from the sample. The defect free samples were used to determine the maximum allowable voltage before damage occurred to the dielectric (ABS plastic). Samples made in one piece and two halves

were tested under AC conditions. The dielectric samples were 3 mm thick and 28 mm in diameter.

- **None in one piece**: Two samples produced in one piece with no defect were tested under AC conditions. PD was first apparent above 10 kV rms in the two samples. As the applied voltage was incrementally increased the PD magnitude increased and the PD activity spread across all four quadrants in the φ-q-n plots. This behaviour indicates damaged dielectric material rather than a PD producing defect. The φ-q-n plots for the two samples at 14 kV are shown in Figure 96.

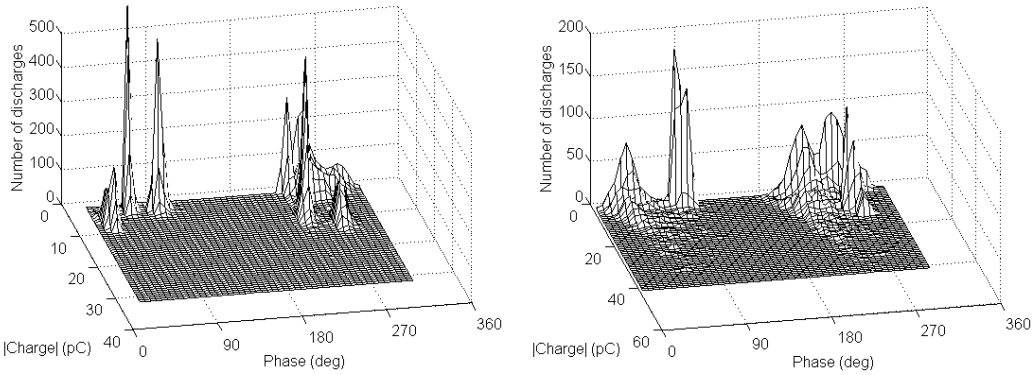


Figure 96 - One piece no void sample A 14.1 kV rms 30 second segment 1 (left) One piece no void sample B 14.2 kV rms 30 second segment 1 (right)

- **None in two pieces:** The samples manufactured in two halves were tested under AC conditions. Sustained PD activity was first evident at 14.2 KV rms in no void sample C and 11.8 kV rms in no void sample D. In both cases the PD initiates in the 4th quadrant which is not typical of void type PD indicating the PD is most likely due to material damage due to excessive voltage magnitude The φ-q-n plot for a 5 minute recording of PD activity at each voltage level is shown in Figure 97.

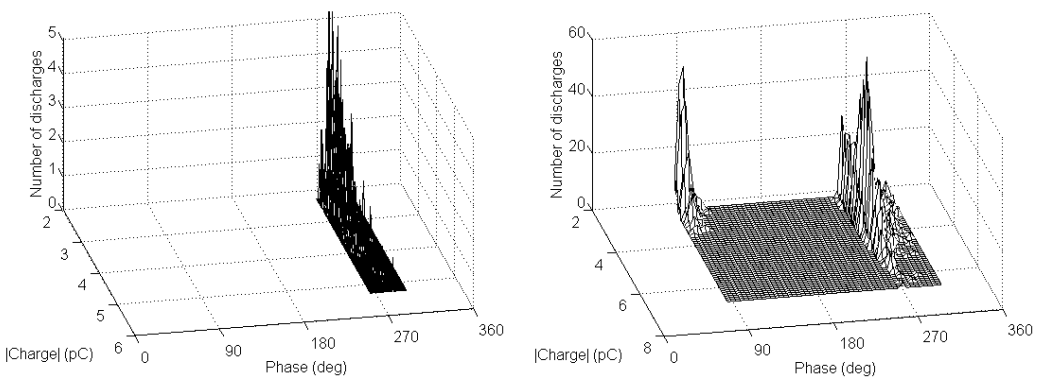


Figure 97 - No void sample C 14 kV rms (left) and no void sample D 11.8 kV rms (right)

AC PD testing was conducted on 2 mm diameter spherical void samples. A 2 mm spherical void was included midway through the thickness and in the centre of a 4 mm thick 28 mm diameter dielectric sample. The spherical void sample was initially produced in one piece and then in two halves to see if void type discharges could be observed.

- **Spherical void in one piece:** Two samples with 2 mm diameter spherical voids were tested under AC conditions and PD was first sustained above 10 kV in both cases. Void type discharges were evident from sample D, with the majority of PD activity leading the test voltage peaks. The behaviour of sample E was less like void type discharges with the majority of PD activity occurring nearer to the test voltage peaks. The behaviour was similar to that of the defect free sample with PD apparent across all quadrants. The φ-q-n plots for both samples at the inception voltage are shown in Figure 98.

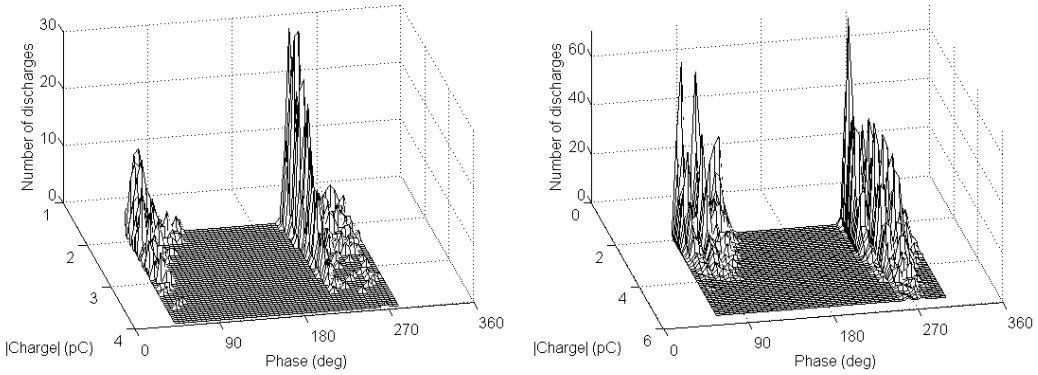


Figure 98 - 2 mm spherical void sample D 10.1 kV rms 30 second segment 1 (left) and 2 mm spherical void sample E 10.3 kV rms 30 second segment 1 (right)

- **Spherical void in two pieces:** During AC testing it was apparent that there was internal discharge. Four spherical void samples were tested and the inception voltage was consistently at or just above 9 kV rms. The inception voltage matched well with the prediction from Paschen's law of 10.3 kV rms. The PD behaviour is consistent with a void with the majority of PD activity occurring in the first and third quadrants before the test voltage peak. The PD activity extinguished at 9 kV after a prolonged hold period. This was expected for a void type dielectric sample with the requirement for a free electron to start the ionisation process inside the void. The φ-q-n plot for the four samples at the inception voltage is shown in Figure 99.

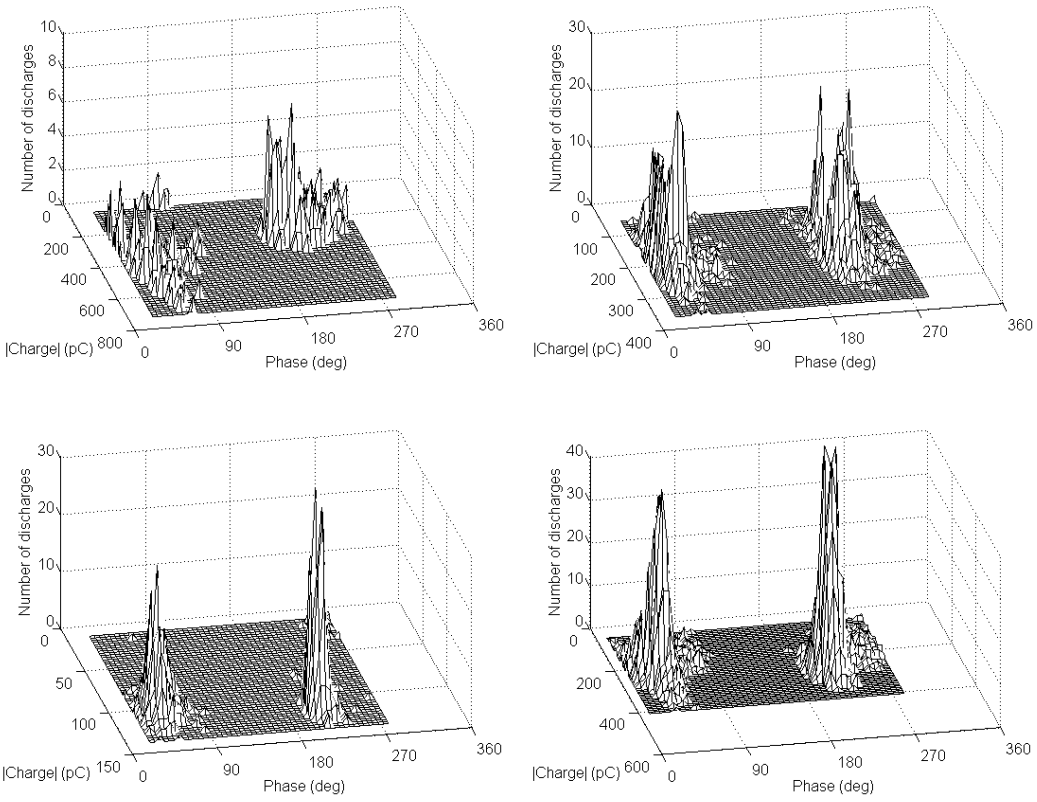


Figure 99 - 2 mm spherical void sample C 9 kV rms 30 second segment 3 (upper left), 2 mm spherical void sample F 9.2 kV rms 30 second segment 1 (upper right) and 2 mm spherical void sample G 9.1 kV rms 30 second segment 1 (lower left), 2 mm spherical void sample H 9.2 kV rms 30 second segment 2 (lower right)

The cylindrical void defect was 2 mm wide by 1 mm high and was within a 28 mm diameter disc which was 3 mm thick. The single piece samples suffered from

sagging in the ceiling of the void, It was decided that the change in geometry was not acceptable so a cylindrical void in one piece was not considered during the testing.

- **Cylindrical void in two pieces:** Three cylindrical void samples formed by joining two half discs were tested. The inception voltage for sustained PD was very close to that of the prediction from Paschen's law of 7.3 kV rms for all samples. PD activity was concentrated in the first and third quadrants. The distribution of PD events in the two quadrants was similar which was as expected for a void type discharge. Some variability in PD magnitude and number of discharges was evident for the three dielectric samples. The main concentration of PD events from the sample was for a charge magnitude100-200 pC in all samples. The φ-q-n plot at the inception voltage for the three samples is detailed in Figure 100.

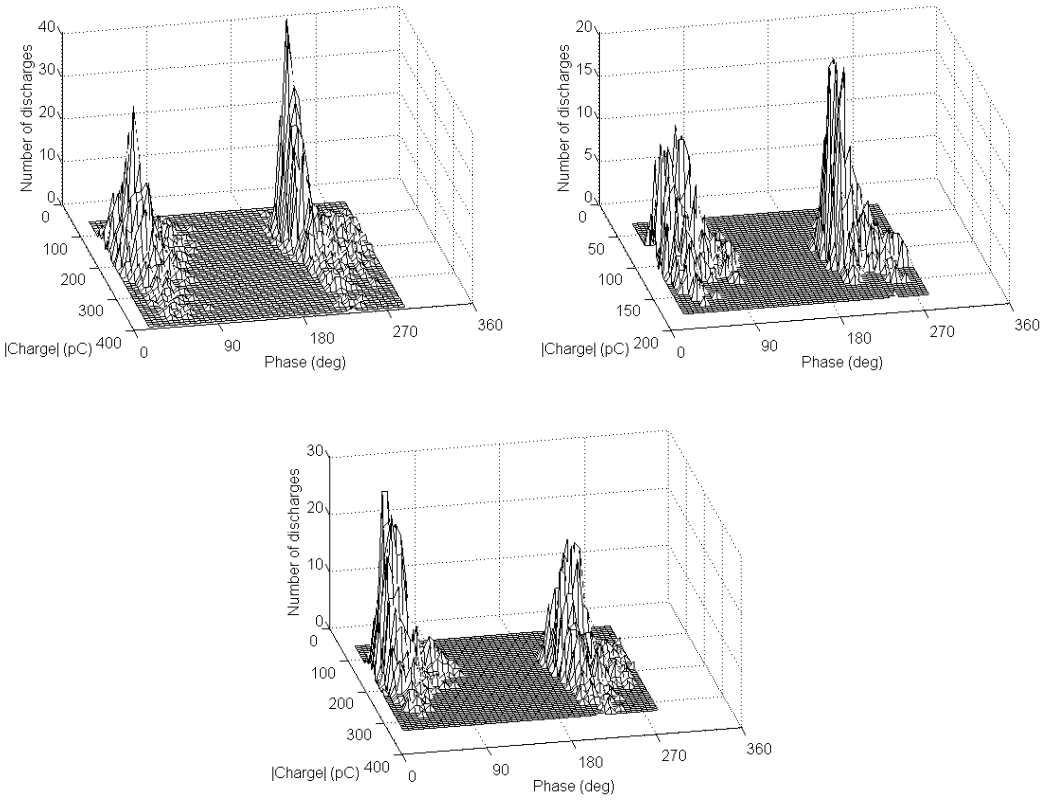


Figure 100 - 2 mm cylindrical void samples; A 7.3 kV rms 30 second segment 2 (upper left), B 7.4 kV rms 30 second segment 2 (upper right) and C 7.3 kV rms 30 second segment 4 (lower)

5.5.1.1. Summary from AC testing

The main finding from AC PD testing was that the samples manufactured in two halves exhibited consistent internal discharge. Generally when the dielectric sample was made in one piece the ceiling of the void was distorted during 3D printing. This had an adverse effect on the PD behaviour for the spherical void with limited PD apparent from the samples. A summary of the AC PD data for the samples is shown in Table XXVIII.

Table XXVIII - Summary of AC PD data for 15000 AC cycles (Manuf. Method 1 = 1 piece, 2 = 2 piece)

Defect [Manuf.]	ID	Number of PD events		mean phase (deg)		Mean |charge| (pC)		Max |charge| (pC)	
		+VE	-VE	+VE	-VE	+VE	-VE	+VE	-VE
None [1]	A	38981	87593	70.2	257.1	4.6	5.9	32.1	32.1
	B	180954	149120	79.3	259.9	2.7	7.1	8.9	20.1
None [2]	C	1	2905	107.7	283.4	2.3	2.6	2.3	5.3
	D	5270	20057	93.2	271.8	2.5	3.4	3.9	6.8
Sph. [1]	D	2639	4083	71.3	228.9	2.4	2.9	4.7	5.4
	E	22280	43868	86.5	266.5	2.3	2.9	4.5	6.8
Sph. [2]	C	881	1130	52.5	220.1	314.5	241.7	733.5	429.9
	F	3516	3562	39.9	228.9	225.6	230.9	365.2	331.3
	G	668	684	48.3	214.9	109.5	114.8	139.4	134.8
	H	23580	22742	44.6	224.7	153.9	210.1	421.7	436.9
Cyl. [2]	A	3880	3389	45.2	225.8	168.7	161.9	374.1	396.6
	B	3877	4337	47.7	221.8	102.2	109.3	212.2	212.7
	C	2112	2058	41.8	224	166.3	179.6	289	330.7

The inception voltage for the spherical void samples was around 9 kV and the predicted inception using Paschen's law was 10.3 kV. The inception voltage for the cylindrical void (7.3 kV rms) matched the prediction from Paschen's law. Based on

these findings Paschen's law was more accurate for cylindrical voids than the spherical voids. This matches expectation with Paschen's law based on a void defect with parallel walls/ceilings (cylindrical void). The electric field inside the spherical void is more uniform than that of a cylindrical void [56]. The field enhancement inside the spherical void is stronger but more importantly the larger surface area of the cylindrical void offers more potential discharge sites. Thus the availability of a starting electron is the limiting factor for the spherical void. The dielectric samples with a cylindrical void exhibit the most repetitive and sustained internal like discharge due to the availability of the starting electron. The PD activity in the spherical voids would extinguish quicker at the inception voltage.

The most repeatable internal discharge behaviour was from the 2 piece cylindrical void samples as such samples with this type of defect were selected for further DC testing.

5.5.2.DC TEST RESULTS

This section details the DC PD testing performed on virgin 3D printed dielectric samples made of ABS plastic in two halves. Initially dielectric samples with no defects were tested to confirm the test setup was PD free. Following this virgin two half cylindrical void samples were tested. The following sections detail the results from DC testing of the dielectric samples. The DC testing used the ramp test method and the hold period for each voltage was 2 hours and the voltage steps were derived from the peak value of the AC inception voltage.

Table XXIX - Summary table for DC PD testing on manufactured samples (manuf. Method 1 = 1 piece, 2 = 2 piece)

Defect [Manuf.]	Sample ID	Defect size (mm)	Thickness (mm)	First DC PD pulse (kV)	AC inception voltage (kV rms)
None [2]	C	N/A	3	42	14
Cyl. [2]	C	2x1 (dia.xhei.)	3	21	7.3
	D			17.6	
	E			11.7	
Sph. [2]	I	2	4	21	9.2

The detailed results are discussed below:

- **No void:** samples in two pieces were tested under DC conditions to confirm that the test setup was PD free. The aim was to determine the voltage at which PD was observed from the sample/test setup. This is to define the voltage limit for further DC PD testing carried out of 3D printed samples. During the test the DC voltage was incrementally increased from 8.8 kV to 47 kV. PD was first observed at 42 kV then ceased and reappeared at 47 kV with a maximum magnitude of 500 pC. The ramp profile and PD pulses are illustrated in Figure 101.

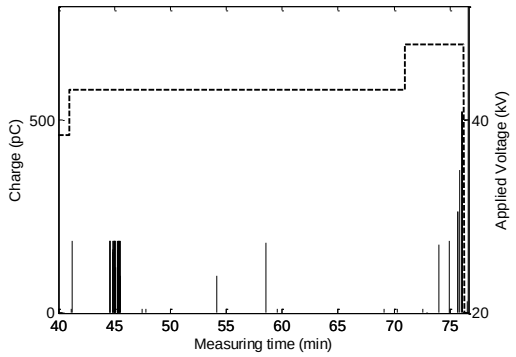


Figure 101 - No void C ramp test profile for holds at 42 kV and 48 kV and recorded PD pulses

- **Cylindrical and spherical voids:** The AC inception voltage for the cylindrical void was 7.3 kV rms thus the peak value (V_R) was 11.7 kV. The five hold voltages in the ramp profile were:V_R/2 (6 kV), V_R (11.7 kV), 3V_R/2 (17.6 kV), 9V_R/5 (21 kV) and 2V_R (23.4 kV). In each voltage step the voltage was held constant for 2 hours.
    - **Cylindrical void in two pieces:** Three samples were tested and limited PD activity was observed during the DC ramp testing.
    - **Spherical void in two pieces:** One sample was tested over a period of two days and on the second day one pulse was recorded when increasing the voltage to 21 kV

The individual DC PD pulses recorded during the ramp tests are summarised in Table XXX.

The main result from testing the cylindrical and spherical voids under DC conditions was that the samples were not particularly active. The lack of PD activity is a good sign that the test setup was PD free.

Table XXX - Summary of DC PD pulses in pC from the samples, change means recorded during a voltage change

Voltage (kV)	Sample ID and pulse magnitude (pC)				
	No void C	cyl. C	cyl. D	cyl. E	Sph. I
6					
11.7				93 (change)	
17.6			37		
21		132.88 (change)			174 (change)
23.4				78 (change)	

5.6. DISCUSSION

The process of designing, manufacturing and electrical testing of these samples was presented. A number of 3D printing methods were considered, FDM was chosen. The 3D modelling package of Autodesk Inventor was available free to students and was very capable in producing the 3D parts to be exported to the 3D printer software then printed.

One FDM 3D printer was used this was the MakerBot replicator 2X, which has a minimum layer height of 0.1 mm. Spherical voids were difficult to manufacture with a diameter of 1 mm so 2 mm was chosen for ease of manufacture. Other FDM 3D printers can print at layers of 0.02 mm but this system was not available at the start of the manufacture process (now available in house at UoS). The improvement in the resolution of 3D printers is inevitable with technological enhancements in the software/hardware of the systems. This will enable refinement of the defects manufactured inside the dielectric samples.

A wide range of filament materials are available for FDM machines the two most common filament types are ABS and PLA. If alternative filaments were being considered the filament type would alter the behaviour during printing. Some materials can permit larger overhangs so there may be further avenues to explore to

print samples in one piece. The switch in filament type could mean that the method used for 2 half joining and sealing of (using acetone) could no longer work. This difficulty of joining was apparent with PLA, with weaker joints and more difficulties with sealing the outer surface.

A test cell was developed to test the disc samples under AC and DC conditions, the test cell was shown to be PD free up to 11 kV rms AC and 42 kV DC using defect free dielectric samples. A critical aspect was the use of an oil bath and mineral oil to minimise any triple junction effects between the electrode, air/oil and insulator interface. The repeatability of testing was important two measures introduced:

- The use of a torque screwdriver to apply a set torque of 0.3 Nm between the plain electrodes and the sample under test ensured consistent preloading was applied to the samples under test.
- The second measure was to use rigid connections between the AC/DC test set and the test cell.

AC PD tests on the samples with defects revealed that the samples produced in two halves had PD inception voltages closer to the prediction from Paschen's law. The manufacture of dielectric samples with spherical voids in 1 piece produced inconsistent PD activity which could not be conclusively attributed to internal discharge. The dielectric sample with a cylindrical void suffered from significant sagging on the ceiling of the void so was not electrically tested. The manufacture of defects in 2 halves was very controllable and the AC PD activity reflected this with consistent inception voltages and PD behaviour. Interestingly the predicted inception voltage using Paschen's law was closer for the cylindrical void than for the spherical void. The larger surface area of the cylindrical void is the most likely explanation. The PD activity also extinguished and reignited over extended periods, this behaviour is typical of internal voids.

The manufacture process of producing samples in two halves does introduce the possibility that inclusions could exist between the two mating faces. The dominant PD producing defect will be the induced void but there is the possibility of additional smaller PD activity from inclusions. A possible refinement would be to join the two halves in a clean room/controlled environment to mitigate the risk of inclusions.

Two defect types were considered in this work; spherical voids and cylindrical voids. The use of the approach to manufacture alternative defects could be explored

further. The ability to model different defects is a distinct advantage of producing dielectric samples using 3D printing. The use of 3D scanners to produce a 3D model and then print the defects the combination of these two approaches could be a useful area of further work. This would allow common defects from cable insulation to be reproduced in controlled samples.

The application of this technique in other scenarios could also be explored. An alternative defect type could be the inclusion of particulates, this could be done by performing the printing process then pausing at a particular layer then inserting the particle then continuing the print process. The position of the defect was always midway through the sample it is known that the position of the void in relation to the electrodes alters the AC PD behaviour [102]. Multiple voids were not considered in this work but the controllability of this approach would allow defined multiple voids to be included in a dielectric sample. The limited PD activity recorded from virgin cylindrical void samples could be explored by trying to either electrically or thermally age samples to see how the PD activity develops in artificially aged samples.

5.7. CONCLUSIONS

Literature relating to the existing manufacturing techniques was reviewed and applications of 3D printing to date were explored. One author had two publications investigating the behaviour of 3D printed samples with internal voids under AC conditions. This work expanded on this study by considering different defect types under both AC and DC conditions.

This chapter presented a novel method for the production of void type defects inside a dielectric sample using a 3D printing manufacturing technique. The FDM 3D printing technique was chosen due to:

- The overhang capability
- The user controls for the print process
- The wide range of filaments available
- The availability of a MakerBot 3D printer ‘in-house’ at the University.

This work showed that a commercially available FDM 3D printer could allow void type dielectric samples to be produced. Autodesk inventor was used to model the samples of interest. Different designs of defects were explored:

- No void
- Spherical void
- Cylindrical void

The best results were obtained when the samples were assembled in two pieces, due to the limitations related to the overhang capability of the 3D printer. This was mainly due to the issues observed when trying to produce defects with overhangs where subsequent layers were deformed leading to possible voids. The single piece samples with a void suffered deformation at the ceiling of the void where the material had an overhang which was unsupported.

A critical stage of producing samples in two halves was the jointing process and final vapour sealing using acetone. The sealing of the samples prevented water and mineral oil absorption. The key finding from using this manufacture method was the significant time saving for producing samples. It took approximately 2 hours to produce each sample, a significant time saving compared to the curing process for the current leading approach using epoxy resin. This may be longer than stacking films to form a defect but the difficulty in sealing layers of films is a distinct disadvantage when trying to manufacture air sealed voids. The controllability of the 3D printing approach to vary the defect size, position and geometry is a significant advantage for future studies of internal defects.

AC PD testing was first conducted to determine the voltage limits of defect free samples. Inception of material damage was observed at 10.2 kV for single piece sample and 11.2 kV for two halves. This was lower than anticipated from reference data it is expected that the polymer blend used to allow 3D printing is different to the reference material. Another issue may be the 3D printing process itself with the way that the filament is deposited possibly leading to a structure with small defects through it lowering the dielectric strength. The careful design of defects to ensure the Paschen's prediction was lower than this material damage point ensured that internal PD was apparent from samples under study.

With the limits established, the samples with manufactured defects were studied with focus placed on the inception voltage and PD activity. The confirmation of operational limits ensured that a confidence could be placed on recorded PD activity for samples with manufactured defects. Paschen's law was used to predict the

inception voltage for the samples under study. The prediction was more accurate for the cylindrical void defects than for spherical voids. The most consistent PD activity was generated by the cylindrical void samples assembled in two halves. The larger surface area of the cylindrical void allowing more potential discharge sites was expected to be the main cause of consistent PD initiation.

The most promising samples and assembly approach was tested under DC conditions. The cylindrical void samples made in two halves were chosen for further DC PD testing. During the subsequent DC testing minimal PD was observed from the dielectric samples during long test periods. This was promising in terms of confirming that the test setup was PD free. The main outcome was that virgin samples with manufactured defects exhibit limited DC PD activity during 2 hour hold periods for DC ramp testing up to $2V_R$. The extension of the voltage range could allow further PD activity. A possible way of stimulating PD would be to age the samples using electrical or thermal means.

Areas of future work make use of the versatility of the approach and consider incorporating other techniques from product design fields such as:

- Variation of filament materials, could allow printing in one piece
- Variation of induced defects and sample geometry
- Consideration of inclusions, could be added by pausing the printing process
- Variation in the number of defects in the dielectric sample
- Use of 3D scanning techniques to image defects and construct a 3D model to 3D print the imaged defects
- Accelerated aging of 3D printed samples to stimulate more PD under DC conditions
- Further developments in the 3D printing equipment will come in the future allowing printed parts with finer resolution
- Application of the technique to more complex insulation samples, bushings or even to simulate cable insulation etc.

6. AC/DC TESTING OF DIELECTRIC SAMPLES WITH MULTIPLE VOIDS

This chapter details the manufacture and testing of 3D printed dielectric samples with multiple void type defects. On reviewing the available literature, it was apparent that few investigations have been carried out on dielectric samples with multiple voids under DC conditions and, as such, this is considered a novel contribution to the field. The behaviour of PD under AC conditions in parallel and serial voids has been reported in a number of sources to date. The PD behaviour of single voids was compared to multiple parallel and serial voids under AC and DC test conditions. The samples under test are virgin, the defects are all cylindrical voids which are arranged in parallel or serial. Parallel voids all exist at the same depth in the insulation and are evenly aligned to one another across the dielectric (Figure 102 (a)). Serial voids are a chain of voids aligned through the dielectric between the electrodes. (Figure 102 (b)).

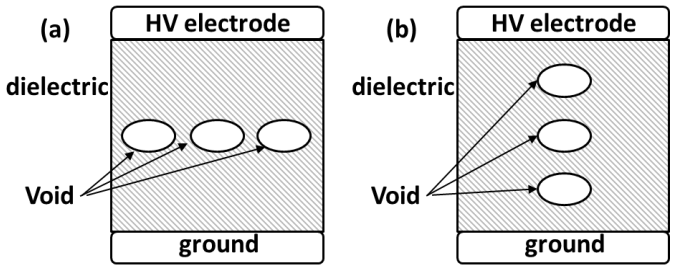


Figure 102 - View of parallel and serial void arrangements between two plain electrodes (a) three parallel voids the dielectric (b) three serial voids the dielectric

This chapter will firstly look at the available literature to understand the current knowledge in this area, to identify gaps so that useful investigations can be performed. In order to support that investigation a series of tests will be conducted with careful consideration of the manufacturing technique discussed in chapter 5.

The following sections will detail: the associated literature, the design, manufacture of samples, the electrical testing of the developed samples, the analysis of the test results and finally the overall conclusions from this work.

6.1. ASSOCIATED LITERATURE

A number of researchers have investigated the behaviour of multiple voids under AC conditions. To date no investigations have been conducted on dielectric samples containing multiple voids under DC conditions. A summary of the investigations conducted under AC conditions are outlined below.

An early paper from Kubler [128] investigates the behaviour of dielectric samples with one or two spherical cavities for a range of geometries. Differences were evident for samples with multiple voids in terms of the repetition rate and the discharge magnitude.

Agoris *et al.* [129] present an equivalent circuit model for two cavities in close proximity. The model was based on the three capacitor model with the dielectric sample broken down into the capacitance of the individual voids. The aim of the work was to investigate the interaction of two neighbouring cavities in a solid dielectric under AC conditions.

In the paper from Jeon *et al.* [130] a numerical simulation of single voids, two parallel voids, two serial voids and two oblique voids was considered. The numerical simulation agreed well with test results for the three different dielectric samples. The serial arrangement of voids was found to reduce the electric field inside the voids and the inception voltage was found to be higher than that of a single void. The parallel arrangement of voids had a similar inception voltage as the single void.

The work of Shin *et al.* [131] investigates the PD behaviour of different arrangements of cylindrical voids. The cylindrical voids are in parallel and series having been manufactured by layering LDPE sheets which were then press-moulded to form one single sample. The PD behaviour of the serial and parallel voids was found to be different. The main observable behaviour of the parallel voids when compared to the serial voids was that: the inception voltage was lower, the average PD magnitude was higher and more PD events were detected. The lower electric field across the two serial voids and larger surface area for the parallel voids were thought to be two key reasons for the difference in the observed behaviour.

Danikas [132] investigated the effect of two or more adjacent cavities in stacked polyethylene sheets forming cylindrical voids. The rise time for a single void and two parallel voids was comparable, however, the apparent charge for the two parallel voids was roughly twice that of the single void. Three cavities were also

considered, the rise time increased and the apparent charge was three times larger than the single void. The breakdown occurring in one cavity may affect the other cavity with transient overvoltages [129]. The results indicate a possible triggering mechanism whereby a discharging cavity may ignite a discharge in a neighbouring cavity. The distance between cavities was identified as being critical and worthy of further research.

Adhikari *et al.* [133] compared the behaviour of a single void, two parallel voids and two serial voids under AC conditions. The samples were manufactured by layers of polyethylene terephthalate (PET) sheets and voids formed by removing circular sections from the sheets. Paschen's law was used to determine the inception voltage. The electric field across parallel voids is higher than that of serial voids; approximately 10 % higher [130]. The inception voltage of serial voids was higher than parallel voids. The inception voltage for the parallel voids was lower than that for a single void. When parallel voids were compared to serial voids, at the same test voltage, more discharges and larger PD events were evident. The main difference was the voids in the serial arrangement were exposed to weaker electric fields with the parallel voids having a larger surface area. The phase distribution of PD activity from the serial voids was wider than that of the parallel voids. A single void sample was electrically aged and PD activity was found to increase in repetition rate and magnitude over a 2 hour period at 3.5 kV.

A further paper from Adhikari [62] focused on the degradation of insulation containing single, parallel and series cylindrical voids. The voids were formed by layering sheets of PET. The PD process can lead to chemical changes on the surface of the voids. Fourier transform infrared (FTIR) spectroscopy was used to analyse the surface degradation inside the voids. The three samples tested were exposed to the same AC voltage during an aging process. The largest chemical change was observed for the single void, there was a lower change in surface chemistry for the parallel voids and the lowest chemical change was observed for the serially arranged voids. A larger number of PD events were recorded for the single void when compared to the two parallel or serial voids. The increased levels of PD activity were thought to contribute to the increased degradation observed on the surface of the single void.

Illias *et al.* [63] conducted PD measurements on dielectric samples made of epoxy resin with two spherical voids. The voids in the samples were created by injecting

two air bubbles into two blocks of partly cured epoxy resin. The two blocks were positioned in close proximity and a further casting was performed so as the two air bubbles were positioned in parallel. Two dielectric samples were manufactured; one with two spherical voids of the same size and the other has two voids of different sizes. The discharges from each void were apparent in both samples for PRPD plots and PSA. In both samples the different activity could be distinguished. In the sample with voids of the same size high intensity low PD activity was apparent from one void and less frequent but larger PD was apparent from the other. When the first PD event occurs in one of the voids the electric field reduces in the void, this directly affects the field in the second void which also reduces. This subsequently leads to a reduction in PD activity in the second void with the requirement to wait for a starting electron. In the sample with voids of different sizes two 'turtle' shaped PRPD plots were evident for the two voids. The larger PD activity was attributed to the larger void and the repetition rate of both voids was similar. When a PD event occurs in the smaller void and, when the field reduces in the smaller void, the electric field in the larger void was not affected; resulting in minimal effect on the PD activity of each void. There was an expectation that if the void separation increased to a critical distance then the PD activity would simply overlap one another; that is to say the voids will not affect one another. A further paper from Illias *et al.* [134] also invested the serial arrangement of spherical voids in epoxy resin. The modelling of multiple voids was presented for finite element analysis (FEA) software. The aim of the work was to determine the inception voltage and the electric field distribution inside the voids for different arrangements of serial voids. When these serially arranged voids were considered it was found that the electric field inside the voids was strongly affected. The electric field magnitude was lower and the PD inception voltage was higher for serially arranged voids when compared to parallel voids.

Bruce *et al.* [135] examines the use of PSA for three different cylindrical void defects formed by layering sheets of PET. The defects introduced were: a single void, two serial voids, two parallel voids. The main parameters of interest were the time of occurrence of PD, the supply voltage and the discharge magnitude. Differences were noted for the three defect types for the voltage differential, time differential and voltage/time differential plots. The PRPD plot for the serial void showed 2 amplitude bands for each polarity, the largest activity was in the negative half cycle. A larger

number of smaller discharges were evident for the two parallel voids but the overall shape was similar to that of the single void (fewer large PD events were apparent).

The paper by Euler *et al.* [136] details the modelling of multiple void defects on COMSOL to understand the electric field distribution inside the voids. Ten different multiple void scenarios were studied in the paper. The scenarios were each modelled and then test cells were manufactured to enable physical testing. Key statistical measures for the charge magnitude of recorded PD events were: maximum value, mean value, standard deviation, skewness and kurtosis. The extension of this work involves the use of AI, a neural network or similar to allow the activity detected to be identified.

6.2. MANUFACTURE OF MULTIPLE VOID DIELECTRIC SAMPLES

The following section details the manufacture process employed in producing dielectric samples with parallel and serial voids. A detailed description of the 3D printing of dielectric samples has been outlined in chapter 5. The nuances of manufacturing dielectric samples with multiple defects using 3D printing will be highlighted in the sections below.

6.2.1. PARALLEL VOID DIELECTRIC SAMPLE DESIGN

The sample was modelled in Autodesk Inventor and was exported from the modelling software as an STL file. The STL file can be opened on the MakerBot Desktop 3D printer software prior to commencing printing of the part. The manufacturing method, described in chapter 5, of creating the sample in two halves was used for this work. The dielectric samples were 28 mm in diameter and 3 mm thick with cylindrical voids of 2 mm in diameter and (with the two halves mated) the void height was 1 mm.

3D models were produced allowing the incorporation of two, three, four and five voids in parallel in each half of the dielectric sample. Initially, a disc of the required geometry was extruded then a second extrusion removed the material from the disc surface to form the void. The voids were defined in a 2D sketch and this was used to 'cut' the cylindrical voids out the surface of the disc.

The separation of the voids was 2 mm in the two-void and four-void samples. In the three-void samples the separation was 1.46 mm and in the five-void samples the separation to the central void was 0.83 mm. The 3D models of each half disc are detailed in Figure 103.

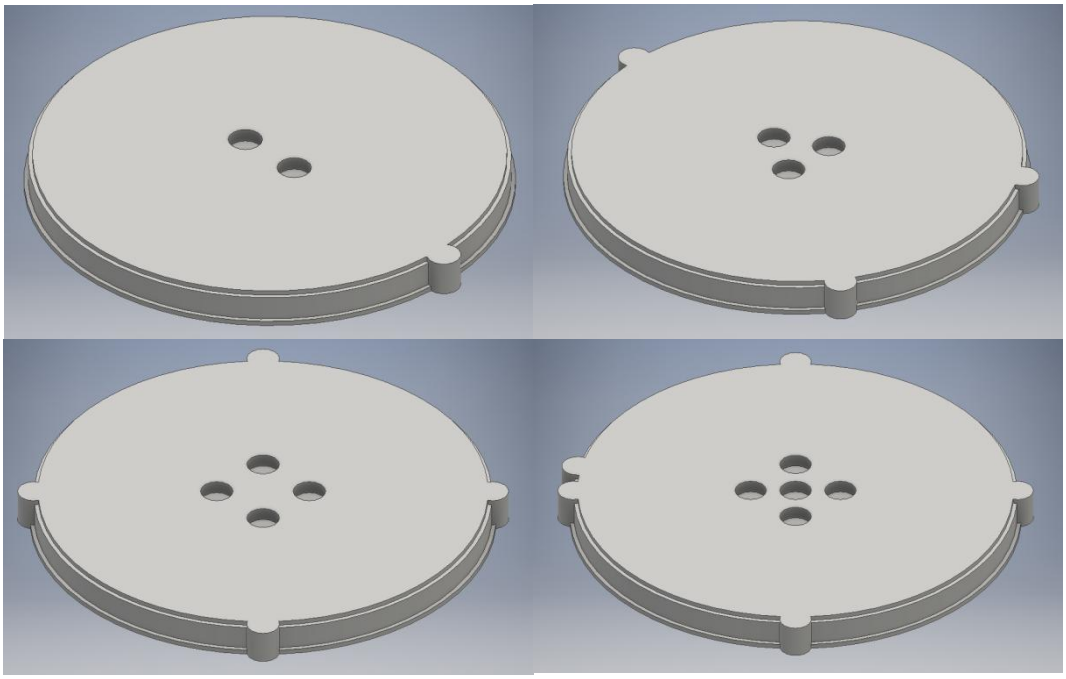


Figure 103 - Images of the parallel voids in a half disc models (all voids cylindrical 2 mm diameter and 0.5 mm high); two parallel voids in a half disc (upper left), three parallel voids in a half disc (upper right), four parallel voids in a half disc (lower left) and five parallel voids (lower right)

The images show the inclusion of the gauge lines for the sacrificial layers on the upper and lower faces of the half samples (stepped region on circumference). The lugs for aligning the two halves and identifying the number of voids inside each sample are also illustrated.

6.2.2. SERIAL VOID SAMPLE DESIGN

Serial void defects were formed by stacking two samples one on top of the other, no change was made in terms of the modelling process as outlined in chapter 5. The samples used in this phase consisted of discs with no defects and discs with single cylindrical voids. The discs with no defects were 3 mm thick and 28 mm in diameter. The disc with a cylindrical void (2 mm in diameter and 1 mm high) were also 3 mm thick and 28 mm in diameter. Three arrangements were considered during this phase:

- Two discs with no defects stacked
- One disc with no defect on top of a single void defect
- Two single voids stacked

The stacked samples were not fixed to one another they were stacked and installed between the two plain electrodes of the test cell. A torque screwdriver was used to apply a set torque of 0.3 Nm to the upper electrode prior to electrical testing.

6.3. MANUFACTURE OF MULTIPLE VOID SAMPLES

The same MakerBot replicator 2X 3D printer highlighted in chapter 5 was used to print the dielectric samples. Developing a reliable and repeatable process was crucial to ensure sample consistency and as such the process is presented below outlining the key steps in the procedure.

- Ensure the nozzle of the printer is clear of any debris
- Use a sheet of paper and perform the levelling process according to the process outlined on the printer (accessed via utilities>level build plate)
- Import the stl file into the 'MakerBot Desktop' program
- Position the model in the desired location on the build plate in the 3D printer software
- Ensure the scaling of the part is correct
- Select the settings tab at the top of the view window, the settings used were;
    - deselect the 'raft/support' options
    - select 'quality' as high
    - 'layer height' was set at 0.1 mm and 'infil' was 100 %
- Select the 'print preview' tab at the top of the view window, this allows the run time and the print process can be interrogated. The 'export tab' prints the part.
- Once the part has been sent to the printer, the printer will go into a warm up mode where the build plate will heat up to 110 °C and the print nozzle will heat up to 230 °C
- It was found that applying the ABS filament and acetone whilst the build plate was heating up was very effective. This approach enabled better bonding of the initial 3D printed layers to the build plate to prevent the part lifting and warping.
- Following the heat up phase the printer will begin by laying the test line deposited across the front of the build plate which confirms the filament feeding through fine and that the deposited filament is consistent (initial system check).

- The printer will deposit the filament in the desired profile on the build plate. Care must be taken to ensure that the material is properly bonded to the build plate. If the build plate is not level then issues should be immediately evident.
- Possible issues that may be encountered:
    - If the build plate is too close to the nozzle then the filament may become ‘backed up’ and no/minimal material is deposited
    - If the build plate is too far away from the nozzle then the filament may not stick to the build plate
- It is important to monitor the print process to ensure it is performed correctly
- Following the successful print the parts can be removed using a spatula
- The next stage consists of sanding to remove the ‘sacrificial layers’ on the upper and lower faces of the parts, as follows:
    - Care must be taken during the surface preparation and storage of raw printed parts as ABS plastic absorbs water
    - Initially 120 grit sandpaper used followed by 320 grit and finally 1000 grit allowing the smooth surface finish
    - During the surface preparation the thickness of the parts was carefully monitored to ensure that it ended up the desired thickness and the gauge lines on the sides of the parts were used to ensure that material was removed from both faces evenly
- The individual halves of the samples are then cleaned with care taken to ensure all debris is removed from the voids
- Acetone is used to bond the halves together. One half receives a heavier coat and the two halves are quickly mated before the acetone evaporates/ABS solidifies
- During the mating process care was taken to ensure the lugs on the outer circumference were matched up. The joined parts are then left under a weight
- The final stage consists of sealing the joint between the two halves and sealing the upper and lower faces of the disc. This ensures both a sealed void and will minimise any water/mineral oil ingress during handling and electrical testing

Images of manufactured parallel voids are detailed in Figure 104 before, surface preparation, joining and final sealing.

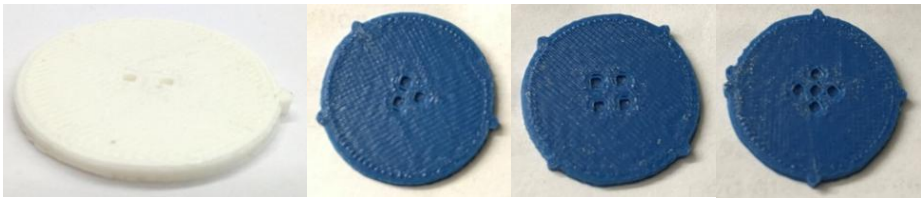


Figure 104 - Parallel void half discs after manufacture: two cylindrical voids, three cylindrical voids, four cylindrical voids and five cylindrical voids (locating lugs shown on outer circumference of disc)

The assembled discs are illustrated in Figure 105.

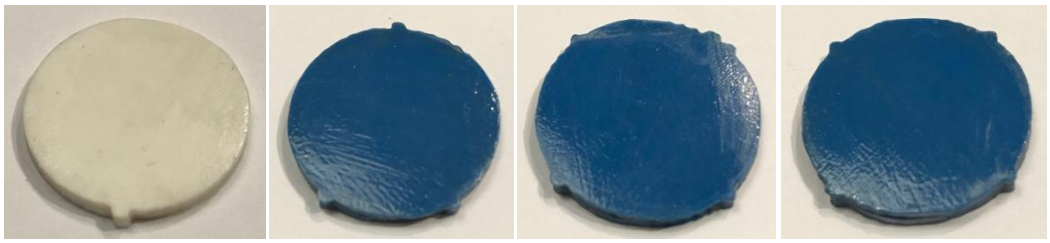


Figure 105 - Assembled parallel void samples: two cylindrical voids, three cylindrical voids, four cylindrical voids and five cylindrical voids

6.4. PD INCEPTION VOLTAGE

Based on analysis conducted in chapter 5, the PD inception voltage predicted by Paschen's law was very accurate for a single void. With no changes to the input data for the Paschen's law model for parallel voids, the model predicts the same inception voltage of 7.3 kV rms for the parallel voids.

The stacking of samples to form serial voids has increased the thickness of the sample, thus the PD inception voltage will be higher. The inception voltage for a single cylindrical void defect in the stacked samples (larger value of *G*) was simulated in this section. The variables used as an input to the calculations are detailed in Table XXXI.

Table XXXI - Paschen's law model input data for cylindrical void in a 6 mm thick insulation sample

Variable (units)	Value
***G* (m)**	$6x10^{-3}$
ε_r	3.25
***P* (kPa)**	100
***L* (m)**	$1x10^{-3}$

A, *B* and *C* were selected using ref for a PL value of 0.1 kPa.m. This enabled the breakdown strength of the gas inside the void to be calculated using equation 28 from which the inception voltage was calculated using equation 29 (both from chapter 5). Table XXXII details the results from the calculations.

Table XXXII - Results from Paschen's law calculations for the cylindrical void in a 6 mm thick insulation sample

Variable (units)	Value
***PL* (kPa.m)**	0.1
***A* (kV/kPa.m)**	30.25
***B* (kV)**	3.12
C	0.675
E_g **(kV/m)**	$4.50x10^{3}$
V_i **(kV)**	11.42

The prediction of inception voltage was 11.43 kV rms, well below the dielectric strength of the film material (20 kV/mm). These predictions were used as a basis for the experimental work conducted in the following sections.

6.5. EXPERIMENTAL METHODS

The test methods proposed in chapter 3 were employed for AC and DC PD testing on the parallel and serial void samples. The ramp test method was used during DC PD testing, with the hold periods set at 2 hours to allow more PD events to occur. Samples were both AC and DC tested, all samples were virgin for each test and this

was their first energisation following manufacture. The samples tested in this chapter are outlined in Table XXXIII.

Table XXXIII - Details of samples tested in this chapter

Defect type	Sample tested under AC	Sample tested under DC	Thickness (mm)
One void	Cyl. void A	Cyl. void C	3
Two parallel voids	Two-void A	Two-void B	3
Three parallel voids	Three-void A	Three-void B	3
Four parallel voids	Four-void A	Four-void B	3
Five parallel voids	Five-void A	Five-void B	3
Single void	Single-void A, Single-void B	Single-void C, Single-void D	6
Two serial voids	Serial-void A	Serial-void B	6

6.6. TEST RESULTS

The results from AC testing are reported in section 6.6.1 and the DC test results are outlined in section 6.6.2 for both parallel and serial voids.

6.6.1. AC TEST RESULTS

The AC PD behaviour of the parallel void samples is reported in section 6.6.1.1 and serial voids are reported in 6.6.1.2.

6.6.1.1. AC testing on parallel voids

This section outlines the AC PD testing performed on the parallel void samples. The main objective of these tests was to confirm that the dominant source of PD was internal discharge and to determine the AC inception voltage for DC PD testing. The change in behaviour with the number of voids will also be investigated under AC

conditions. The behaviour of a single cylindrical void was documented in chapter 5 the φ-q-n plot for the second 30 seconds at 7.2 kV rms is detailed in Figure 106.

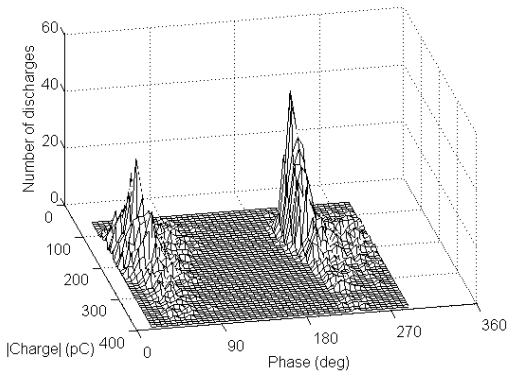


Figure 106 - Cyl. void A φ-q-n plot at 7.2 kV rms (30 second segment 2)

Samples with two, three, four and five parallel void samples were tested under AC conditions to determine the AC inception voltage. The φ-q-n plots for the first 30 seconds of PD activity at the inception voltage for each of the parallel void samples are detailed in Figure 107.

A summary of the parallel void samples is as follows:

- **Two-void A:** Inception voltage was 7.2 kV rms. The majority of PD occurs in the first and third quadrants. The peaks in PD activity are less evident than that of the single void sample.
- **Three-void A:** Inception voltage was 8.4 kV rms which was higher than both the single and the two parallel void samples. The PD in the positive half cycle is more like a rabbit ear compared to the focused PD activity in the negative half cycle during the first 30 seconds.
- **Four-void A:** had an inception voltage of 9 kV rms. There was a distinct increase in the smaller PD events but generally more PD events were evident across the first and third quadrants.
- **Five-void A:** the inception voltage was 8.5 kV rms. A reduction in PD activity was also evident from the 4 void sample, albeit the 4 void sample had a higher inception voltage.

Table XXXIV, below, summarises these results.

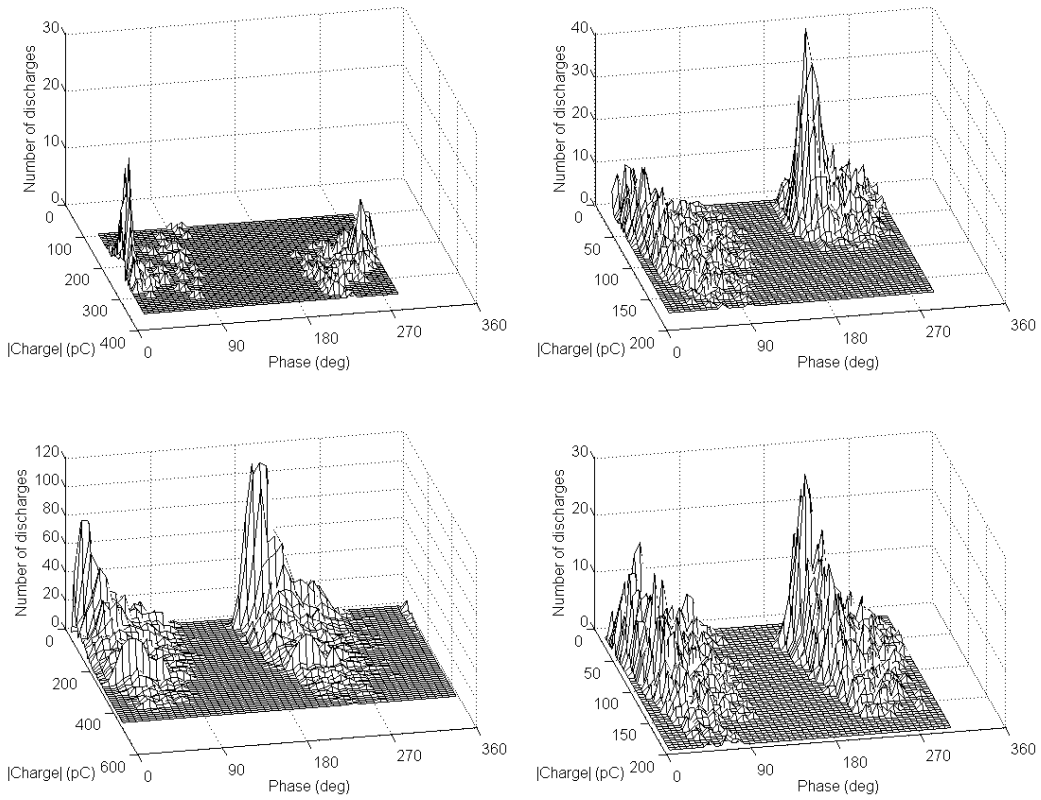


Figure 107 - φ-q-n plots for the parallel void samples; two-void A 7.2 kV rms first segment (upper left), three- void A 30 seconds at 8.4 kV rms first segment (upper right), four-void A at 9 kV rms first segment (lower left) and five-void A at 8.5 kV rms first segment (lower right)

Table XXXIV - PD behaviour for the parallel void samples at the PD inception voltage (PDIV) for the first 15000 cycles

Number of voids	PDIV (kV)	Number of PD events	Max |Charge| (pC)	Mean |Charge| (pC)
1	7.3	7269	396.6	165.52
2	7.2	7822	390.03	233.84
3	8.4	12193	194.35	66.3
4	9	32565	549.78	162.92
5	8.5	17814	550.86	135.32

The PDIV for the two parallel void sample was slightly lower than the sample with one void. In contrast, the inception voltage for the three, four and five parallel voids was higher. It is evident that as the number of parallel voids increased the number of

PD events generally increased. The only exception to this was that more events were detected for the sample with four parallel voids than the sample with five. One reason for this increase could be the fact that the inception voltage for the four voids was higher and, generally, as the applied voltage increases, the number of PD events will increase. The increase in PD events when more parallel voids were introduced matches expectation as more potential discharge sites were available.

The maximum PD magnitude generally increased as more parallel voids were introduced. The maximum was similar for the single and two parallel void samples but was significantly lower for the three parallel void sample. The samples with four and five parallel voids had the largest maximum PD magnitude. There was no clear trend with the variation of mean value of PD magnitude and the number of parallel voids.

Table XXXV, below, provides a further breakdown of PD data by separating the data into the positive and negative half cycles of the AC reference voltage.

Table XXXV - Comparison of PD behaviour in the first 15000 positive (+VE) and negative half (-VE) cycles for the parallel void samples at each inception voltage

Number of voids	Number of PD events		mean phase (deg)		Mean |charge| (pC)		Max |charge| (pC)	
	+VE	-VE	+VE	-VE	+VE	-VE	+VE	-VE
1	3880	3389	45.22	225.76	168.69	161.89	374.11	396.6
2	4125	3697	30.69	257.12	229.22	238.99	340.85	390.03
3	5020	7173	52.29	223.42	77.69	58.33	194.35	164.87
4	16854	15711	42.36	225.69	154	172.49	420.26	549.78
5	8986	8828	44.45	225.12	133.42	137.25	440.47	550.86

As can be seen the number of PD events in the positive and negative half cycles are very similar for all the samples. This was expected for void type samples midway through the insulation. The largest mismatch was for the three parallel voids. The mean phase was very similar for all the samples. The only exception was the two parallel void sample which exhibited PD behaviour at earlier phases in both half cycles. The mean charge and maximum charge of PD events was similar in both

half cycles for the majority of samples. The largest variations were evident for the four and five parallel voids, with the largest PD events recorded in the negative half cycle in each case.

The number of PD events for the parallel void samples at the inception voltages was compared for the first 15000 cycles (300 seconds) of the AC reference. The data was split into ten consecutive 30 second segments with the number of PD events summed over each segment (Figure 108).

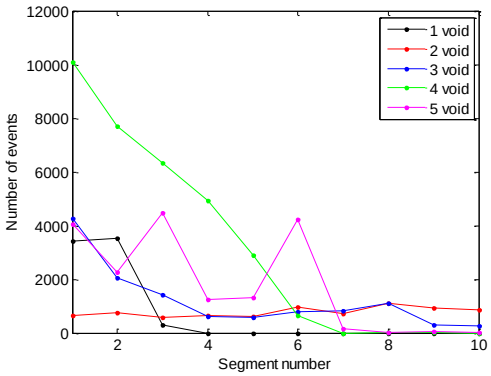


Figure 108 - Comparison of the number of PD events over the first ten 30 second segment at the PDIV for each parallel void sample

The majority of the samples exhibit a characteristic drop in PD activity over the first 10 segments (single, three, four and five). The sample with two parallel voids has sustained PD activity over the full period. This could suggest that the sample is at a higher voltage, with respect to the inception, than the other samples.

The variation of PD activity over the 15000 cycles was studied in more detail, scatter plots were produced to show the variation of PD magnitude at each inception voltage over the 300 second measurement window (Figure 109).

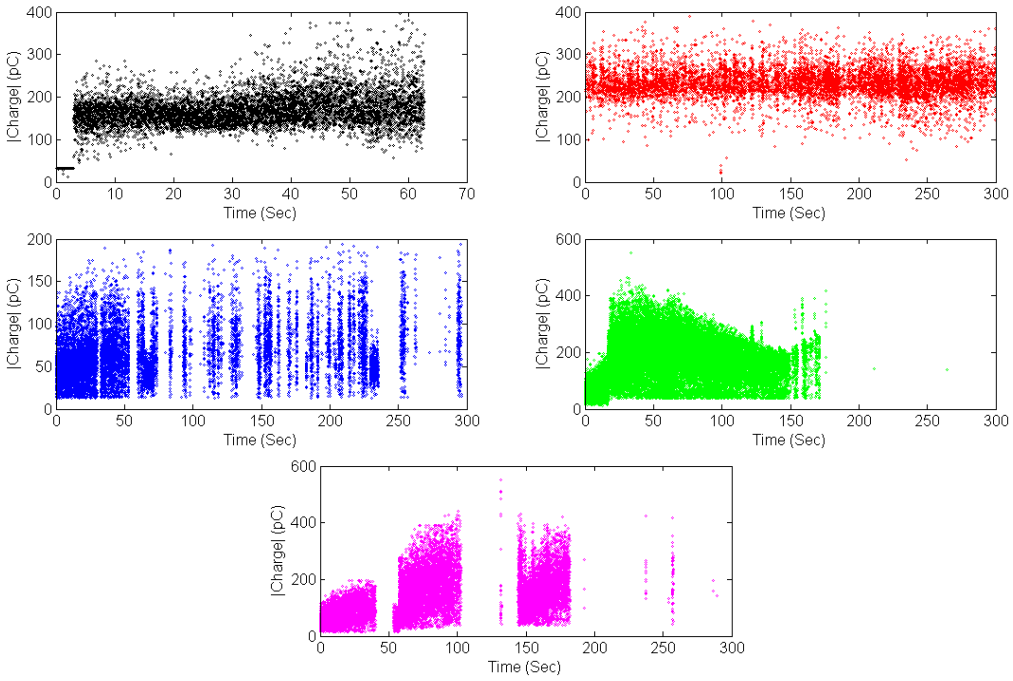


Figure 109 - Charge magnitude behaviour over the first 15000 cycles at the inception voltage for each sample: Cyl void A (black), two-void A (red), three-void A (blue), four-void A (green) and five-void A (magenta)

There was a variation in PD activity observed during the 300 second measurements:

- **Cyl. Void A:** emitted PD activity of increasing magnitude for the first 60 seconds and no PD activity was evident for the remaining time.
- **Two-void A:** emitted consistent PD activity over the 300 seconds duration.
- **Three-void A:** emitted PD activity in bursts with the PD magnitude steadily increasing over the 300 seconds.
- **Four-void A:** the PD activity increased rapidly over the first 30 seconds then steadily reduced until around 150 seconds. After 150 seconds bursts of PD activity were apparent for 20 seconds then the activity ceased.
- **Five-void A:** emitted three bursts of PD activity (each burst 40-50 seconds) during the bursts the PD activity increased in magnitude.

This analysis has highlighted the inconsistency of the PD activity from the sample with three or more parallel voids. Despite the inconsistency more PD events were recorded from these samples over the 300 second measurements.

The phase of PD occurrence for the parallel void samples was studied over the 300 second measurement window in Figure 110

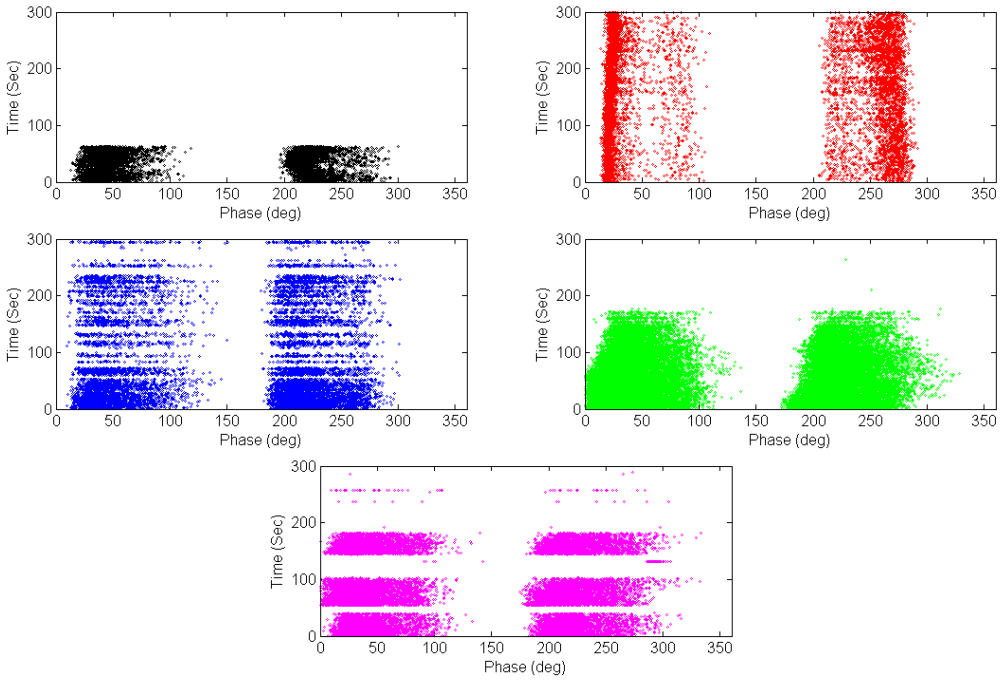


Figure 110 - Variation of phase for the first 15000 cycles at the inception voltage for each parallel void sample: Cyl. Void A (black), two-void A (red), three-void A (blue), four-void A (green) and five-void A (magenta)

The phase variation of the single and two serial voids was more concentrated over a shorter phase range in the first and third quadrants. In contrast the three, four and five parallel voids PD behaviour was over full first and third quadrants. It was also apparent over time that the range of phase occurrence reduced during the bursts of PD activity. This was particularly evident for the three and four void samples.

All samples were exposed to 9 kV rms and the same analysis was conducted to determine any changes in PD activity. The number of PD events for the parallel void samples at 9 kV rms was compared for the first 15000 cycles (300 seconds) of the AC reference (Figure 111).

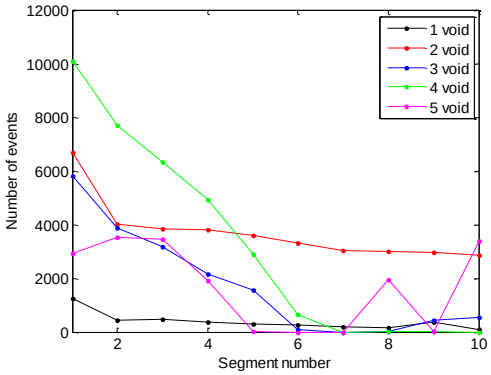


Figure 111 - Comparison of PD events over the first 5 minutes around 9 kV for the first 5 minutes (each segment is 30 seconds of PD data)

In terms of the number of PD events:

- **Cyl. Void A** was the least active and is less active than during the 15000 cycles at the inception voltage. Consistent PD was apparent for the sample over the ten segments at 9 kV rms.
- **Two-void A** had a larger number of PD events, when compared to the activity at the inception voltage. There was a slight drop in PD activity over the 10 segments but the sample was very active.
- **Three-void A** was initially more active than at the inception voltage but reduced significantly up to segment six.
- **Four-void A** was gathered at 9 kV so was the inception voltage.
- **Five-void A** behaves in a similar erratic manner with the maximum number of events not exceeding 4000 per segment.

6.6.1.2. AC testing of serial voids

The single void sample was formed by stacking a disc with no void and one with a cylindrical void. The orientation of the two discs was varied; first the void was closer to the HV electrode (single-void A) and secondly the void was closer to the ground electrode (single-void B). The serial void sample (serial-void A) was formed by stacking two discs with single voids which were then installed between the two plain electrodes of the test cell. The φ-q-n plots for the first 30 seconds at the inception voltage are shown in Figure 112.

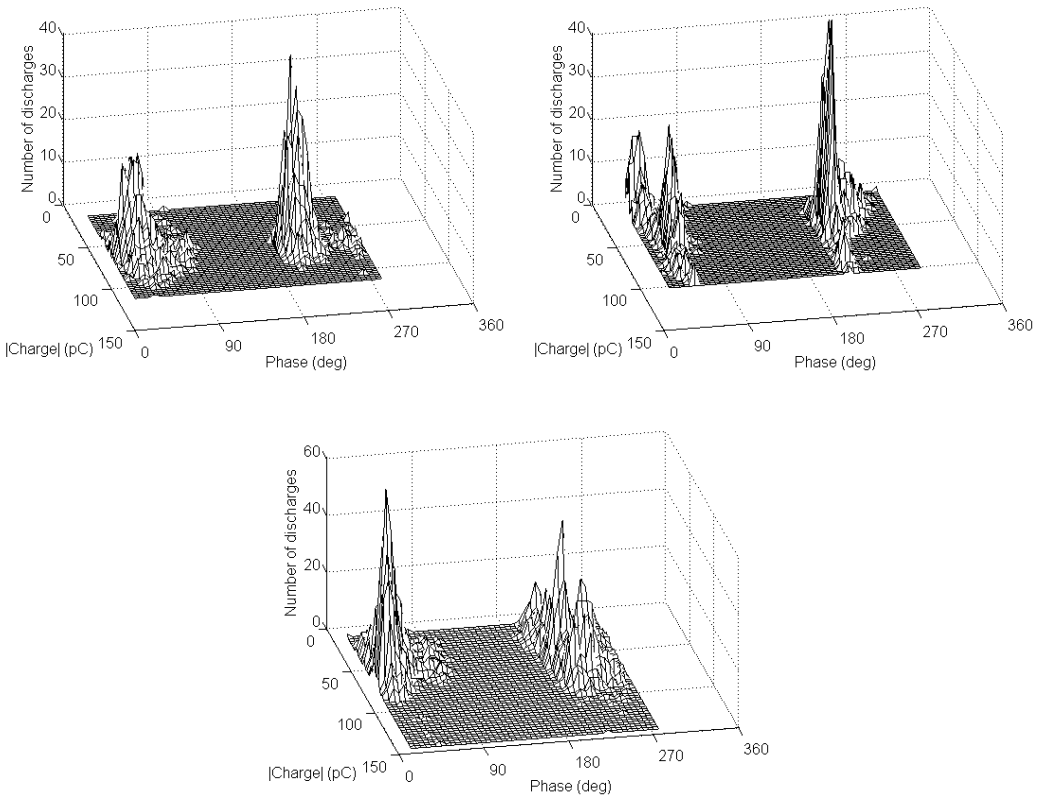


Figure 112 - φ-q-n plots for the single and serial voids; single-void A 30 seconds at 14.2 kV rms first segment (upper left), single-void B at 14.1 kV rms third segment (upper right) and serial-void A at 13 kV rms first segment (lower)

The inception voltages were as follows:

- Single-void A was 14.2 kV rms
- Single-void B was 14.1 kV rms
- Serial-void A was 13 kV rms

The inception voltage for the single void samples was found to be higher than the prediction from Paschen's law (11.43 kV rms). The inception voltage for serial void samples was also found to be lower than that of the single void. The inception voltage was expected to be higher than that of a single void but the results showed this was not the case.

A summary of the PD activity over the first 15000 cycles at each inception voltage is detailed in Table XXXIV.

Table XXXVI - PD behaviour for the serial void samples at the inception voltage for the first 15000 cycles

Defect type	PDIV (kV)	Number of PD events	max PD mag (pC)	Mean PD mag (pC)
single-void A	14.2	16649	143.52	66.4
single-void B	14.1	27363	133.21	55.48
serial-void A	13	28611	145.58	57.33

A similar number of PD events were recorded for the single void B and serial void A, with more PD events recorded than the test on single void A. The maximum PD magnitude was similar for the single and serial voids. The mean PD magnitude was highest for the first orientation of the single void. The PD data was separated into the positive and negative half cycles for the AC reference voltage. Table XXXV, below, presents a summary of the data for the first 1500 AC cycles.

Table XXXVII - Comparison of PD behaviour over the first 15000 cycles at the PDIV in the positive and negative half cycles for the serial void samples

Defect type	Number of PD events		Mean phase (deg)		Mean |charge| (pC)		Max |charge| (pC)	
	+VE	-VE	+VE	-VE	+VE	-VE	+VE	-VE
single-void A	8689	7960	50.74	220.19	61.36	71.91	143.52	108.27
single-void B	14174	13189	48.02	232.36	49.35	62.06	119.02	133.21
serial-void A	13929	14682	40.45	228.35	55.11	59.44	141.26	145.58

The number of events, mean phase and mean charge were all very similar in the positive and negative half cycles for all tests. The maximum charge magnitude for the single-void A and single-void B shifts from the positive half cycle in single-void A (void closer to HV electrode) to the negative half cycle in single-void B (void closer to the ground electrode). The maximum charge magnitude in each half cycle for the serial voids was closely matched.

The number of PD events for the single and serial void samples at each inception voltage was compared for the first 15000 cycles (300 seconds) of the AC reference (Figure 113).

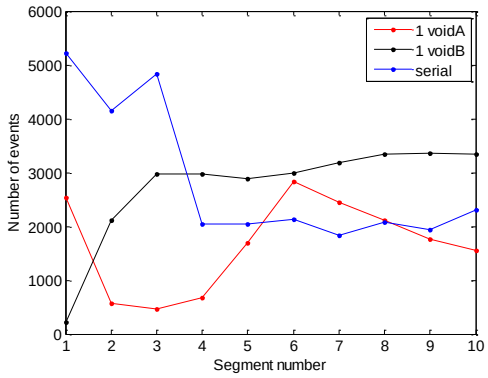


Figure 113 - Comparison of PD events over the first 5 minutes at the PDIV of each sample for the first 5 minutes (each segment is 30 seconds of PD data): single-void A (red), single-void B (black) and serial-void A (blue)

The number of PD events varied as follows for the samples tested:

- **Single-void A** was initially high over the first segment but behaves erratically over the remaining segments, with decreases and increases in PD activity.
- **Single-void B** behaves more consistently once the number of PD events reaches 3000 in segment three.
- **Serial-void A** was initially very active over the first three segments then also stabilises around 2000 PD events per segment.

The reduced PD activity in serial voids was evident when single-void B was more active between segments 4 and 10 at the inception voltage.

A scatter plot of PD magnitude over time was used to show the variation of PD activity over the first 15000 cycles at the inception voltage (Figure 114).

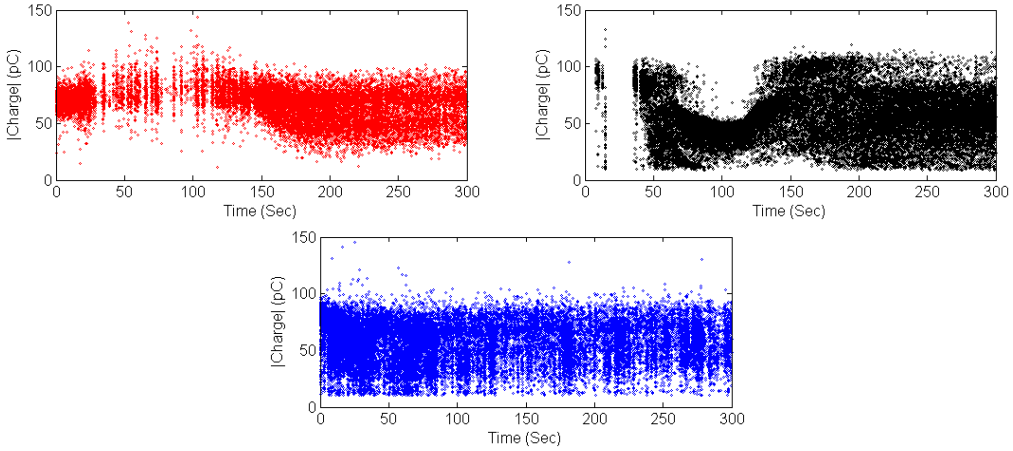


Figure 114 - PD magnitude variation over the first 15000 cycles at the inception voltage: single-void A (red), single-void B (black), serial-void A (blue)

The variation of PD magnitude in the samples was as follows:

- **Single-void A** was initially moderately active for the first 25 seconds and then from 25 to 110 seconds there was a reduction in PD activity. The PD activity increased after this point with consistent discharges up to 300 seconds.
- **Single-void B** had limited PD apparent over the first 40 seconds; following this large PD events were evident for 20 seconds. Between 70 seconds and 140 seconds the maximum PD magnitude halved to 50 pC, after this point the PD magnitude recovered to a maximum of 100 pC.
- **Serial-void A** initially had very intense over the first 120 seconds then reduced in concentration after this period.

The phase variations of discharges with respect to the AC supply are illustrated in Figure 115 for the first 15000 cycles. The single-void A sample suffered a reduction in PD activity this led to PD activity occurring earlier in the negative half cycle over this period (25-110 seconds), subsequently the phase behaviour stabilised. The single-void B sample experienced a reduction in PD magnitude over the period 70-100 seconds. As a result the reduction led to a phase delay in the inception of PD activity during the AC cycles over this time period. The serial-void A sample had consistent phase behaviour over the 300 seconds.

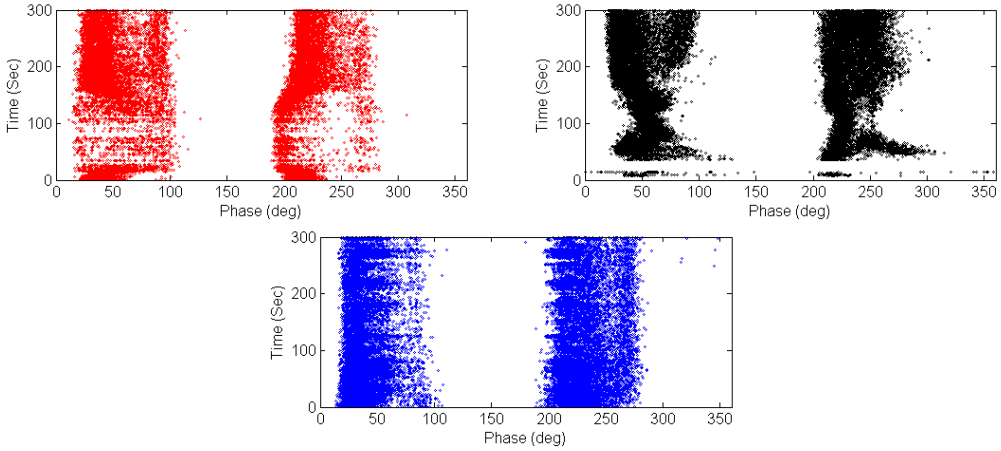


Figure 115 - Phase behaviour over the first 15000 cycles at the inception voltages: single void orientation A (red), single void orientation B (black), serial voids (blue)

6.6.2.DC TEST RESULTS

The following section details the test results from DC PD tests on samples. The DC PD tests conducted on parallel voids is detailed in 6.6.2.1 and serial voids are discussed in 6.6.2.2. Due to the limited PD activity recorded during the DC PD testing, the findings have been presented via a table for ease of analysis.

6.6.2.1. DC testing of parallel voids

The parallel void samples tested were as follows:

- **Cyl. Void C** - contains a single cylindrical void
- **Two-void D** - contains two cylindrical voids in parallel
- **Three-void B** - contains three cylindrical voids in parallel
- **Four-void B** - contains four cylindrical voids in parallel
- **Five-void B** - contains five cylindrical voids in parallel

The DC PD test results for the parallel void samples are summarised in Table XXXVIII, the PD data was separated into that which was recorded during voltage changes and then during voltage holds.

In general for the parallel voids, during voltage changes the PD magnitude was significantly higher than when the voltage was held constant. This matches the behaviour reported in chapter 4 where larger PD events were evident during voltage

changes. The virgin samples with parallel voids exhibited a limited number of PD events but significantly more than the sample with a single void. The PD magnitude and number of PD events increased as more parallel voids were added to the dielectric sample under DC conditions. This matches reported behaviour under AC conditions [133].

Table XXXVIII - Summary table of the DC PD activity from the parallel void samples

Quantity	Number of parallel voids				
	1	**2**	**3**	**4**	**5**
Mean |Charge| AC (pC)	165.52	233.84	66.3	162.92	135.32
Mean |Charge| DC voltage change (pC)	85.5	97.33	110.91	151.79	107.63
No events during changes	2	5	9	5	10
mean |Charge| DC voltage hold (pC)	37	35.22	61.56	49.19	89.98
No events hold	1	1	3	7	5

6.6.2.2. DC testing of serial voids

The serial void samples tested under DC conditions were as follows;

- Single-void C was made up of a single cylindrical void stacked on top of a disc with no defect (same as single-void A from the AC PD testing).
- Serial-void B was formed by staking two discs each with a single cylindrical void.

The summary of DC PD results for the single void and serial void samples is shown in Table XXXIX.

No PD activity was recorded during the voltage hold periods for single-void C and three PD events were recorded during the voltage changes. The PD recorded during the voltage changes for serial-void B was similar but smaller than that for the single void. This matches expectation whereby smaller PD events were anticipated for serially arranged voids when compared to single voids [133]. The extension of the test programme and number of samples would enable further test data to be gathered and more firm conclusions on the behaviour observed. In particular the

elevation of the applied voltage may stimulate further discharge events during the hold periods in the DC ramp test.

Table XXXIX - Summary of the DC PD activity for the single and serial void samples

Quantity	single-void C	serial-void B
Mean |Charge| AC (pC)	66.4	55.48
Mean |Charge| DC voltage change (pC)	43.91	31.48
No events during changes	3	3
mean |Charge| DC voltage hold (pC)	None	34.69
No events hold	0	1

6.6.2.3. Summary of DC PD testing

The samples with parallel voids exhibited more PD activity in general both during voltage changes and the hold periods. The PD magnitude of the parallel voids was larger than that of a single void. This was to be expected with parallel voids offering more potential discharge sites through the increase of surface area. In the case of the serial void the magnitude of PD events recorded was lower for the two serial voids than the single void during voltage changes. The number of PD events recorded was very similar for the single and serial voids. In both of the above cases the observed behaviour matched the behaviour expected under AC conditions. The PD was recorded for the single void during a hold period so this cannot be compared.

6.7. DISCUSSION

This chapter has focused in detail at multiple parallel and serial voids for which there is a gap in the available literature. To date the majority of studies have investigated the behaviour of parallel and serial voids under AC conditions. In this study, a number of samples were manufactured using a 3D printer to produce defined dielectric samples with various defects. The different scenarios presented represent initial explorations of the manufacturing technique. A series of tests were conducted which investigate PD behaviour under AC and DC conditions. This work has built on earlier findings in order to produce consistent samples to study the gap found in the literature.

The design process utilised was very similar to that used in chapter 5. However, the incorporation of multiple parallel voids required a different modelling approach from that listed in chapter 5. During modelling the half disc of the dielectric was extruded then a second extrusion was required to remove the cylindrical defects from the face of the half disc. The inclusion of cylindrical voids using this process was relatively simple during the modelling stage, however if multiple spherical voids were to be introduced the process would be more challenging. This could be explored in further work and it would be interesting to compare parallel cylindrical voids to parallel spherical voids. The separation distance was not considered in detail in this work but the distance between the voids is a very important parameter which affects the PD behaviour observed. The minimum separation distance in this work was 0.83 mm and the maximum was 2 mm. The PD activity reported for spherical void defects in close proximity [63] was not evident in the AC PD data for these samples. This could be further explored through designing samples with varied separation distances. The combination of the 3D modelling and the manufacture process will allow a sensitivity analysis to be conducted into different voids geometries and void spacing.

The 3D printing process allowed the repeatable manufacture of half disc samples with multiple voids. The 3D printer did have a set profile that it ran through in the x-y plane (not a smooth circle). The addition of locating lugs ensured that matching defects were mated together during the joining process. This was important when considering parallel void layouts that needed specific alignment. The lugs also allow the quick identification of the type of defect introduced inside the sample. This would be valuable when considering defects of different sizes and layouts in any sensitivity analysis.

The parallel voids samples had different inception voltages during the AC PD testing. The prediction of the inception voltage was 7.3 kV rms using Paschen's law, for a 1 mm high defect in a 3 mm thick insulation sample. The inception voltage for the single void was 7.3 kV rms and for the two parallel voids was 7.2 kV rms. The inception voltages for the samples with more than two parallel voids were higher; for three parallel voids was 8.4 KV, four parallel voids was 9 kV and five parallel voids was 8.5 kV. Previous papers reported that the inception voltage for two parallel voids was lower than that of a single void, this was the case in this work when two voids were in parallel. The main reason for the lower inception voltage is the field

enhancement which occurs in parallel voids. There was an expectation that the inception voltage for the three, four and five parallel void samples would be similar. One reason for the variation could be the availability of a starting electron to start the ionisation process. The layout of the voids, the distance between the voids or the insulation material may not be providing the field enhancement inside the neighbouring voids, as reported in previous studies [133].

The AC testing of a single void and serial voids in a 6mm thick insulation produced mixed results. There was an expectation that the serial voids would have a higher inception voltage than the single void. The inception voltage of single-void A was 14.2 kV rms and single-void B was 14.1 kV rms. The inception voltage for serial-void A was 13 kV, lower than the single void. In both orientations of the single void the inception voltage was similar so effect of charge movement through the dielectric can be neglected. Another aspect was the alignment of the two cylindrical voids in series, there may have been some misalignment allowing the electric field to be larger than anticipated inside the two serial voids [136]. A further consideration was the separation of the serial voids through the thickness of the dielectric sample, this has not been considered in publications to date. The separation of the voids in this work was 3 mm, this could be a reason for the difference in inception voltage. A further reason may also be the delay in the availability of the starting electron, but the repeated result for the single void makes this difficult to justify.

Under DC conditions the majority of PD was apparent during voltage changes and limited PD events occurred during the hold periods of 2 hours. The lack of PD data is most likely due to the fact that the dielectric samples are virgin and have experienced no electrical or thermal aging prior to the DC PD testing. Exploring the aging of 3D printed sample would be an interesting avenue for future work.

Despite the lack of PD activity interesting observations were made for the two different DC tests conducted. The first case was the consideration of parallel voids. The mean magnitude and number of PD events during voltage changes increased as more parallel voids were introduced. Similarly the mean PD magnitude and number of PD events also increased for PD events recorded during the holds at defined voltage levels when more parallel voids were introduced. This was expected with the field enhancement which occurs in parallel voids but also the surface area of potential discharge sites increases as more parallel voids are added.

The second case when single and serial voids were considered cannot be directly compared to the parallel void case as the insulation thickness was increased to allow serial voids to be introduced. During voltage changes larger PD events (on average) were recorded from the single void than from the serially arranged void. Only 3 PD events were recorded for each sample during voltage changes so limited data has been used to make the average values. During the voltage hold no PD activity was recorded from the single void sample and one PD event was recorded for the serial voids. The PD activity recorded for the single and serial voids was lower than that of the parallel voids, the main cause was thought to be the increase in insulation thickness rather than the layout of voids. The direct comparison of the AC/DC PD behaviour of single, parallel and serial voids would be interesting. This would be achieved by designing samples with the same insulation thickness to allow comparisons to be drawn.

6.8. CONCLUSIONS

Literature related to investigations around the behaviour of parallel and serial voids has been identified and discussed. The literature review highlighted a gap in current knowledge around the behaviour of parallel/serial voids under DC conditions. The use of the approach presented in chapter five allows the creation of defined defects in insulation samples. The controllability of the approach was a distinct advantage and worth an initial exploratory investigation.

A method has been presented in this study to allow the design and manufacture of virgin parallel/serial cylindrical voids. The approach will enable the inclusion of defined defects at particular locations inside the dielectric sample. The controllability is a key aspect to facilitate the work in this chapter but also for future studies considering a range of defects and separation distances for multiple defects. The existing manufacturing approaches do not offer this level of control for defects inside a dielectric sample. One limitation was the requirement to produce the samples in halves to negate the issues with printing the ceiling of both cylindrical and spherical voids. The method was effective and parallel voids could be included in the half discs using 3D printing.

In this work the behaviour of parallel voids were compared to a single void and serial voids were compared to a single void. This forms an initial study to demonstrate the

versatility of the manufacturing technique; it highlights that there is further work in exploring the behaviour of defects located in close proximity.

The same method was applied to the 3D printing and assembly process for all 3D printed samples no matter the changes in the number of parallel voids. The only additional complexity was the requirement to align the two halves during the joining process. For this reason locating lugs were included to simplify the process and to allow the quick identification of defect type inside the sample. This approach was effective and would be recommended in future studies.

The AC PD behaviour of a single void was compared to that of two, three, four and five parallel voids. The inception voltage for a single void and two parallel voids was, close to the prediction using Paschen's law. The inception voltage was higher for the three, four and five parallel voids. The expectation from previous work was that the inception voltage for parallel voids would be lower than that of the single void due to field enhancement inside the neighbouring voids. The increase in inception voltage may be due to a delay in the availability of a starting electron, the layout of the voids or the insulation material may not allow the enhancement of electric field inside the void. In general, when more parallel voids were included more PD events occurred at the PD inception voltage. The sample with two parallel voids exhibited the most consistent PD behaviour at the inception voltage.

The AC PD behaviour of serial voids compared to a single void was also studied. The inception voltage for the two serial voids was lower than that of the single void. The expectation was that the inception voltage for the two serial voids would be higher than that of the single void. This was not the case, the main reasons for this could be; the delay in the starting electron, alignment of the two serial voids (possible offset) or the separation of the two voids through the thickness (has not been studied in detail to date). This work would benefit from further investigation such as a sensitivity analysis of the key changes in geometry such as separation of serial voids. A larger mean PD magnitude was recorded for the single void compared to that of the serial voids.

The ramp test method was used to determine the DC PD behaviour of the virgin samples under test. The repeatability of the DC ramp test was important and allowed comparisons between PD behaviour of different dielectric samples. An important stage was the identification of the voltage limits with non-defective samples prior to the DC ramp testing on samples with defects. This approach is

advised for future studies with multiple samples with the same defects where comparisons are required.

Under DC conditions as the number of parallel voids increased the more PD events were apparent. This matches expectation whereby the samples with more parallel voids have a larger surface area with more potential discharge sites for PD activity to occur. There was less PD events recorded under DC conditions for serial and single voids. When the serial voids were compared to a single void, the PD magnitude was generally smaller in magnitude during voltage changes. The single void under study produced no PD activity during the hold periods so could not be compared to serial voids. The expansion of both arrangements to more samples would allow more PD data to be recorded and allow more conclusive results.

Future work relating to this study includes:

- Exploring the behaviour of different defect geometries in parallel and serial would be an interesting aspect of study, this work only considered cylindrical voids.
- Specific samples could be manufactured to allow the direct comparison between parallel and serial voids. This would require an increase in the insulation thickness of the parallel void samples to allow two serial voids to be included.
- Investigating the void separation of parallel voids has been considered to date but no work has focused on the serial separation of voids and the influence of this on PD activity.
- Detailed analysis of parallel voids and serial voids could be conducted by producing a range of samples using 3D modelling and 3D printing.
- The effect of different void sizes in close proximity has been investigated under AC conditions but could be considered in future DC studies.
- The aging of the samples would be an interesting area of investigation either electrically under AC conditions or through the thermal aging of samples. The expectation was that aged samples would produce more PD under DC conditions, based on the activity reported in chapters 3 and 4 on a heavily aged parallel void sample.

7. ACCLERATED AGING OF 3D PRINTED DIELECTRIC SAMPLES

This chapter details the testing of dielectric samples manufactured using 3D printing and the thermal aging of these samples prior to electrical testing. The overall aim was to produce samples which have been exposed to accelerated aging to determine if the AC and DC PD behaviour was significantly affected by the thermal stressing of the samples. Specifically this work looks at the difference between samples exposed to elevated temperatures for prolonged periods and samples stored at ambient temperature. In addition this chapter explores the ability of 3D printed parts to withstand elevated temperatures and the physical changes due to the thermal aging. As well as examining PD of aged samples this section will explore and compare temperature related influences on 3D printed dielectric samples.

7.1. ASSOCIATED LITERATURE

A number of papers to date have studied the aging of dielectric materials, a summary of the most relevant work will be discussed in this section, with a focus on the modelling, physical, electrical and thermal aging.

A summary of work to date was presented by Fothergill *et al.* [137] in relation to the ARTEMIS project. Three main modelling methodologies were highlighted [138]–[140]. In this paper specific focus was placed on the physical measurement that can be performed to allow the electro-thermal aging to be related to the models. Approaches investigated included; differential scanning calorimetry (DSC), Fourier transform infrared (FTIR) spectroscopy, transmission electron microscopy (TEM), space charge measurements and Luminescent techniques. The samples under analysis were peelings from XLPE cable samples which had been exposed to different electrical and temperature regimes to determine the relative changes in the samples.

Li *et al*. [141] investigated the behaviour of XLPE samples which were removed from cable samples of different ages. PEA, DSC and FTIR measurements were performed on the samples. The space charge behaviour was altered for the samples of different ages.

A number of papers on theoretical models related to electrical and thermal aging were reviewed and are summarised below. In an early paper from Paloniemi [142] a review is conducted on the chemical and physical aging mechanisms. The theory of equalised aging processes (EAP) was presented with particular focus on the thermal aging process.

Later work from Dissado *et al.* [138] investigated the role of space charge in the electrical aging of insulating materials under DC conditions. The effect of space charge on the aging of insulation samples subjected to thermos-electrical stressing is reported. A model is developed and discussed detailing how space charge could contribute to material aging when combined with thermo-electrical stresses.

Wu *et al.* [143] presents a percolation model for the breakdown strength of dielectrics. The model estimates the breakdown strength of the dielectric sample at hand. Electrical aging is considered to be an increase in trap density, resulting in a reduction in the electric field required for a breakdown.

Crine [144] uses a previously presented aging model to interpret the electrical aging of polymer materials. A critical electrical field is defined which, when exceeded irreversible changes occur leading to accelerated aging. The permanent changes occur to intermolecular bonds of the polymer. Space charge is considered a consequence rather than a cause of aging in polymers (i.e. space charge is formed after the changes at a molecular level).

Mazzanti *et al.* [145] discuss the role of space charge in the aging process of insulation systems. Space charge is argued to drive the aging process from initial energisation to forming micro defects in the insulation. Following the formation of these micro defects PD can occur in the insulation. Specific focus is placed on the development of manufacturing processes of insulation to minimise the size of defects introduced. The authors call for enhanced understanding of the effect of aging at a molecular level.

A paper by Alghamadi *et al*. [146] details simulations for aging models using a DMM life model. The simulations investigated the behaviour of PET films under DC conditions and temperatures of 110 and 180 °C. The simulations showed the structural changes due to the electro-thermal aging these changes can lead to failure paths within the structure of the material.

Further papers which study the aging of dielectric materials in general were reviewed with a number of particular interest summarised below.

A technical report [147] from Bell telephone laboratories (BTL) presented findings on the aging problems in plastics. BTL found that continued exposure of polymers to sunlight, air, oxygen, water, cold, heat and micro-organisms can cause polymers to decompose. This decomposition known as aging, can lead to brittleness and future failure. BTL used accelerated aging techniques to ensure systems operating for the full design life (some 20 years in the telephone industry). The first accelerated aging test procedure developed by BTL for polyethylene equated 100 hours of aging to 1 year of outdoor exposure. Recently, the methods were re-evaluated and were judged conservative; the 100 hours of aging was actually equivalent to 3 years of outdoor exposure. The accelerated aging methods mainly centre on the exposure of samples to UV light. The light effectively oxidises the plastic through the development of carbon-oxygen chemical group called carbonyl. The light accelerates the aging of the carbon from the plastic and oxygen in the air to form the carbonyl group. Unexposed polyethylene contains minimal carbonyl groups. The formation of the carbonyl groups effectively breaks up the long chain hydrocarbons into smaller chains leading to a reduction in toughness and ultimately leads the material to become brittle. BTL used spectroscopy to detect these chemical changes of the polymer.

In the paper [148] manufactured samples were exposed to thermal and electrical aging. A number of samples were exposed to different temperatures and electrical stress levels. Following the aging process scanning electron microscope (SEM) imaging was used to determine the structural changes in the samples. Electrical measurements were performed to determine the dielectric constant and loss factor. Large changes were evident in the structure of the samples when exposed to both temperature and voltage.

Work by Densley *et al.* [149] investigated the multistress aging of solid dielectric extruded type insulation under dry conditions. The main aging mechanisms are identified as electrical, mechanical and thermal. These multistress aging mechanisms for solid insulation are explored in the paper. A range of aging models are considered as well as their effectiveness for the study of accelerated aging tests on solid insulation.

The experimental study by Griffiths *et al.* [150] investigates the electrical and thermal endurance of polymers in a dry scenario. This paper built on previous work by extending beyond previous published work. Testing was conducted on XLPE cable samples under electrical/thermal stress conditions and the resultant endurance data was compared to a range of available models.

A more recent publication from Tzimas *et al.* [151] presented the results of electrical endurance tests on XLPE peelings. The peelings were subjected to different pre-stressing of electrical, thermal and combined electro-thermal stressing. The samples which were exposed to thermal pre-stressing had a reduced endurance capability when compared to samples exposed to electrical pre-stressing. The samples which had been subjected to combined electro-thermal pre-stressing had the most affected endurance capability of all the samples tested. The thermal endurance models were used to justify the accelerated aging observed for samples exposed to combined stress. The electrical field was seen to act as an accelerator in the thermal aging process. Space charge measurements were also used to give an idea of pre-stressing history of the peelings under investigation. Only measurable changes in endurance capability were observed at the upper limit of the electrical and thermal stressing.

Kemari *et al.* [152] conducted accelerated thermal aging on PVC disc samples for a range of temperature utilising a set time period of 2016 hours. The alternating current applied to the dielectric samples was analysed. The magnitude and harmonic distortion of the current waveforms was studied using the FFT method. The current waveform was shown to increase in magnitude and the harmonic distortion was found to be low (due to the large fundamental) in samples aged at higher temperatures.

Wei *et al*. [153] investigates the combined electro-thermal aging of transformer paper. Measurements of PD, TSDM and SEM imaging were employed to determine the changes in behaviour during the aging process. An increase in PD magnitude and repetition rate was evident at higher stress levels and over the aging periods of each test.

A range of papers specifically study the thermal aging of insulation samples.

For example, Montanari *et al.* [154] discuss the thermal aging of XLPE samples using different methods. The first was the conventional method where a range of

temperatures are selected and aging is conducted for a set time. At set time intervals, a range of measurements are performed to determine the material properties. This allows a thermal endurance graph to be derived using electric strength measurements. The second method utilised analytical test methods to determine the activation energy. It was found that this method can be used to form an accurate characterisation. Based on measurements articulated in the paper the author deduced that the oxidation was the main form of degradation evident.

Boubakeur *et al.* [155] investigated the thermal aging of XLPE cable samples at four temperatures ranging from 80 to 140 °C. Following the aging process a range of tests were conducted; inception voltage of PD, determination dielectric loss index (product of loss factor and relative permittivity). The inception voltage for PD was shown to reduce with increasing temperature and aging time. The dielectric loss index was found to increase with temperature and aging time.

The paper from Boukezzi *et al.* [156] presents the use of X-ray imaging to track the changes in crystallinity in XLPE insulation from cables. The changes were observed by aging XLPE samples at different temperatures. The crystallinity was shown to increase at the beginning of aging then decrease. The reduction was more evident as the aging temperature was increased. Using Arrhenius law the activation energy and temperature index was derived.

The paper [157] investigates the aging due to partial discharge activity in aged and unaged oil impregnated paper samples. The samples had a disk shaped cavity between the sheets of paper. The samples were aged thermally. The samples which were subjected to thermal aging were aged for 13, 25 or 31 days at 160 °C (no mention of a particular test standard). The PD inception voltage, breakdown voltage and the time for breakdown to occur were all recorded during the experiment. The time to breakdown for aged and unaged samples was very similar. The number of PD events and magnitude was found to initially increase until a peak was found then the activity decayed until breakdown occurred. PD activity in aged samples was found to be of higher magnitude and more PD events were recorded. It was also found that the aged samples had a higher breakdown voltage (11 kV compared to 10 kV). It was concluded that the aged samples could withstand PD activity more effectively than the unaged paper.

Li *et al*. [158] aged LDPE samples at 90 and 100 °C between 1 and 15 days, this was below the melting temperature of LDPE (105-115 °C). PEA, DC conductivity

and DSC measurements were performed on the aged samples. There was a point in the aging process (5 days) when there was a suppression of the charge injection leading to the breakdown voltage increasing and the conductivity reducing. At longer aging periods the breakdown strength reduced and the conductivity increased.

The conductivity changes in the insulation are an important aspect for the behaviour of DC PD activity. A range of papers have studied the changes in conductivity of aged insulation samples [159]–[161]. The DC conductivity of the insulation was found to increase with aging time and aging temperature for a range of dielectric materials. The conductivity of the insulation is a critical property which determines the field enhancement inside the void and ultimately leads to changes in the repetition rate and PD magnitude under DC conditions.

The dielectric samples under consideration in this chapter are made of ABS plastic and therefore a range of previous work investigating the thermal aging of ABS plastic was also consulted.

A paper by Tiganis *et al.* [162] was focused on the degradation of the mechanical properties. Thermo-oxidative aging was observed at temperatures of 120 °C whereby the mechanical properties of the samples were significantly affected by the temperature exposure. In comparison, at temperatures of 90°C and 100 °C, the degradation of mechanical properties was less significant.

Another paper [163] investigates the accelerated thermal aging of ABS at elevated temperatures above 80 °C. At 120 °C the impact resistance of the samples was found to be severely affected. FTIR used to inspect the chemical composition of the thermally aged samples chain scission and cross linking was observed.

Next a number of relevant test standards related to accelerated aging were investigated.

ASTM-D149 [164] titled standard test method for dielectric breakdown voltage and dielectric strength of solid electrical insulating materials at commercial power frequencies mainly deals with breakdown testing of solid insulating materials.

ISO 188 [165] details accelerated aging and mainly presents the analysis of mechanical properties of the materials. Specific focus is placed on the properties of the oven. This document refers to ISO 23529 [166] was recommended for aging temperatures and duration of aging tests.

ASTM D3045-92 [167] titled standard practice for heat aging of plastics without load. This document details the exposure conditions for oxidation or degradation of plastic when exposed solely to hot air. The procedure for heat exposure was introduced not the test method or specimen. The practice is intended to be used as a guide to compare thermal aging characteristics of materials for a particular property that may vary with temperature exposure. The practice also details a procedure for determining a thermal aging characteristic over a range of temperatures to enable the determination of the value of the equivalent property at a lower temperature. Severity of exposure to elevated temperatures depends on the temperature and the time period of exposure generally longer exposure times are more effective than temperature elevation. It is also suggested a minimum of three samples of each material for each aging temperature be used. It also suggests, when determining a property change due to temperature a minimum of four temperatures should be used.

IEC 60216 [67] presents accelerated aging procedures and the interpretation of the results. The accelerated aging procedure goes from the preparation of sample specimens, the reporting of test results and the evaluation of data. The number of specimens for thermal aging is recommended as five. In terms of exposure temperatures the specimens should be exposed to no less than three temperatures preferably at least four temperatures covering a sufficient range. Aging times of 500 to 20,000 hours are recommended with care taken not to reduce the time by increasing the temperature as transition temperatures can complicate matters.

ASTM F1980 [168] is a standard guide for accelerated aging of sterile barrier systems for medical devices. The thermal aging apparatus, aging theory, aging plan and post aging tests are discussed. An area of specific interest is the accelerated aging theory and the relations around the Arrhenius equation. An accelerated aging factor can be derived from a listed equation which in turn allows the calculation of an accelerated aging time. The accelerated aging time is the time required to conduct the same aging cycle at a defined ambient temperature.

Based on the literature review material the thermal aging of dielectric samples was deemed an effective way to accelerate the aging of dielectric samples. In some publications the thermal aging of samples was a more effective way of aging samples. The method presented in ASTM F1980 will be employed to allow the derivation of the equivalent aging time at ambient temperature to the known aging

time at elevated temperatures. The Arrhenius equation is the basis of this and will be discussed in the following section.

7.2. ARRHENIUS EQUATION

By the late 1800's an increase in temperature was known to speed up chemical reactions in everyday life and science experiments. Before the work of Arrhenius it was known that a 10 degree rise in temperature led to a doubling of chemical reaction rates in chemistry studies [168]. Arrhenius brought together known concepts and laws to devise the Arrhenius equation (equation 30) to account for the temperature dependence of chemical reactions.

$$K = Ae^{-E_a/RT} \tag{30}$$

The variables in equation (30) are as follows:

- Number of reactions per second (K)
- Pre-exponential factor (*A*) or the total number of collisions per second
- Activation energy (E_a)
- Temperature in Kelvin (*T*)
- The universal gas constant (*R*)

The increase of temperature or reduction in activation energy will increase the number of collisions. A decrease in activation energy can be achieved by using a catalyst. The pre-exponential factor can be removed by equating the reaction rate and temp for the two cases can be shown by equations (31) and (32).

$$K_1 = Ae^{-E_a/RT_1} \tag{31}$$

$$K_2 = Ae^{-E_a/RT_2} \tag{32}$$

The two can be simplified then equated, first natural log of both (31) and (32) yields (33) and (34).

$$\ln(K_1) = \ln\left(Ae^{-\frac{E_a}{RT_1}}\right) \quad (33)$$

$$\ln(K_2) = \ln\left(Ae^{-\frac{E_a}{RT_2}}\right) \quad (34)$$

The product rule was used to separate terms as shown in (35) and (36).

$$\ln(K_1) = \ln(\mathrm{A}) + ln\left(e^{-\frac{E_a}{RT_1}}\right) \quad (35)$$

$$\ln(K_2) = \ln(\mathrm{A}) + ln\left(e^{-\frac{E_a}{RT_2}}\right) \quad (36)$$

Since $\ln(e^x)=x$ rearrangement of equations (35) and (36) yields (37) and (38).

$$\ln(K_1) = \ln(\mathrm{A}) - \left(\frac{E_a}{RT_1}\right) \quad (37)$$

$$\ln(K_2) = \ln(\mathrm{A}) - \left(\frac{E_a}{RT_2}\right) \quad (38)$$

Rearrangement to move the pre-exponential factor the left results in equations (39) and (40).

$$\ln(A) = \ln(\mathrm{k}_1) + \left(\frac{E_a}{RT_1}\right) \quad (39)$$

$$\ln(A) = \ln(\mathrm{k}_2) + \left(\frac{E_a}{RT_2}\right) \quad (40)$$

Equating equations (39) and (40) and further simplification is shown in equations (41) to (44).

$$\ln(\mathrm{k}_1) + \left(\frac{E_a}{RT_1}\right) = \ln(\mathrm{k}_2) + \left(\frac{E_a}{RT_2}\right) \quad (41)$$

$$\ln(\mathrm{k}_1) - \ln(k_2) = \left(\frac{E_a}{RT_1}\right) - \left(\frac{E_a}{RT_2}\right) \quad (42)$$

$$\ln\left(\frac{k_2}{k_1}\right) = \left(\frac{E_a}{RT_1}\right) - \left(\frac{E_a}{RT_2}\right) \quad (43)$$

$$\ln\left(\frac{k_2}{k_1}\right) = \frac{E_a}{R}\left(\frac{1}{T_1} - \frac{1}{T_2}\right) \quad (44)$$

Equation (44) can be used to confirm the validity of the Q_{10} coefficient formula by substituting values into the expression. Temperature values can be substituted and the variation of activation energy can be determined for a range of reaction rate ratios (k_2/k_1). For a particular scenario the activation energy required to result in a k_2/k_1 ratio of 2 can be determined. The Q_{10} temperature coefficient formula [168] can be employed to relate a temperature variation to the change in chemical reaction rates in using equation 45.

$$Q_{10} = \left(\frac{k_2}{k_1}\right)^{\frac{10}{T_2 - T_1}} \quad (45)$$

Where Q_{10} is the aging factor defined as 2 for a 10 deg increase (k_2/k_1 ratio of 2), T_2 is the accelerated aging temp (°K), T_1 is the ambient temperature (°K). The Q_{10} value determines the relation between the reaction rates over the temperature difference range. Rearrangement of equation 45 yields equation 46 in terms of the ratio of the reaction rates.

$$\frac{K_2}{K_1} = (Q_{10})^{\frac{T_2 - T_1}{10}} \quad (46)$$

The accelerated aging time ($Time_2$) is defined in equation (47) as the desired room temperature ($Time_1$) shelf life divided by the accelerated aging factor.

$$Time_2 = \frac{Time_1}{\left(\frac{k_2}{k_1}\right)} \quad (47)$$

One limitation of this approach is that above 60°C the errors are also multiplied by the factor of two used to represent Q_{10}. [168] recommends the T_2 in excess of 60 °C is not recommended as many polymers experience a higher probability non-linear changes. This work uses this approach to relate thermally aged samples to samples stored at room temperature.

7.3. METHOD FOR ELECTRICAL TESTING OF THERMALLY AGED SAMPLES

The dielectric samples were manufactured using the method presented in chapter 5. The defects introduced were 2 mm diameter 1 mm high cylindrical voids in the middle of and midway through a 3 mm thick 28 mm diameter disc. The preparation of the samples was varied in two ways for the thermal aging of the 3D printed dielectric samples:

- The first was to prepare the half discs, join them and seal to form the whole discs with defects prior to the thermal aging.
- The second way was to subject the raw 3D printed discs to perform thermal aging then prepare the half discs, join and seal.

The thermal aging apparatus consists of a Towers electric oven (Figure 116). The oven has a heated element in its base and has a thermostat on the side to control the oven temperature.

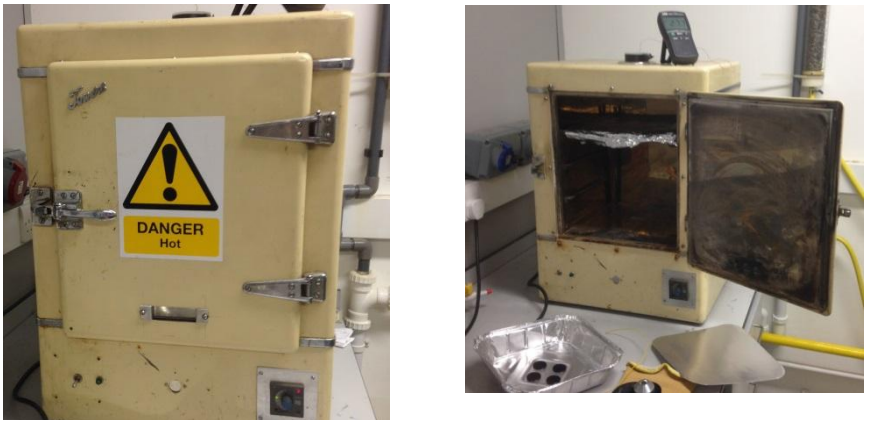


Figure 116 - Thermal aging equipment (a) Towers electric oven thermostat in bottom right of faceplate (b) Oven internals aluminium tray and k-series thermal probe

Secondary confirmation of oven temperature was possible via a k series thermal probe that was installed in the ceiling of the oven. The temperature of the oven was available via the display of the TES 1131 K-series thermometer. The samples to be aged were placed in an aluminium tray and the shelf inside the oven was moved to the top of the oven. This was to ensure the tray containing the samples was as close to the temperature probe as possible.

Equations (46) and (47) from the Q_{10} rule can be used to determine k_2/k_1 and $Time_2$. The sample was exposed to an elevated temperature (T_2) for a defined $Time_2$. This $Time_2$ can be equated to a room temperature time ($Time_1$) for an equivalent sample aging at room temperature (T_1) of 25 °C. The maximum $Time_2$ considered in this study was 168 hours. A range of five different temperatures were selected to enable the behaviour of the 3D printed parts to be understood below and above the glass transition temperature of ABS. The glass transition temperature of ABS is 100-105 °C.

The aging cycles which will be conducted in this chapter are detailed in Table XL. The table lists the aging ID number, the accelerated aging temperature, accelerated aging time, room temperature and the room temperature time.

The cylindrical void samples were exposed to these aging cycles to accelerate the aging of the samples. The dimensional properties of the samples were measured before and after thermal aging to determine whether any change occurred during the thermal aging process.

Table XL - Aging cycles to be conducted: aging ID number, accelerated aging temperature (T_2), accelerated aging time ($Time_2$), room temperature (T_1) and equivalent room temperature time ($Time_1$)

Aging ID	Sample IDs	T_2 (°C)	$Time_2$ (hours)	T_1 (°C)	$Time_1$(hours)
1	2F, 2G, 2H and 2I	60.8	48	25	543
2	Aged E, F, G and H	80.4	168	25	7816.6
3	Aged A, B, C and D	99.4	168	25	29172.4
4	N/A	113.4	5.5	25	2520.4
5	N/A	115.4	6	25	3158.4
6	Aged I and J	114.6	168	25	83663.9
7	Aged K	136.7	168	25	387092.1

Following the aging cycles, the samples were subjected to AC and DC PD testing using the same methods proposed in chapter 3, the test cell presented in chapter 5 was used in this work.

The AC PD testing was used to confirm that the dominant source of PD was still internal discharge and to determine the peak value of the AC inception voltage for DC PD testing. The dielectric samples were subsequently tested under DC conditions using the ramp test method. The aim of this work is to determine whether the thermal stressing prior to PD testing has any effect on the AC and DC PD behaviour of the samples under test. These test results are presented in the following section.

7.4. TEST RESULTS

The test results are split into three different areas the first being the observations from thermal aging of the dielectric samples and the physical changes in the samples. The second is the AC PD testing of aged samples and the final section is the DC PD testing of samples.

7.4.1. THERMAL AGING OF SAMPLES

This section will discuss the aging cycles carried out and the changes in geometry evident in the dielectric samples. The seven aging cycles are detailed in Figure 117. The temperature of the oven was manually recorded during the thermal aging processes.

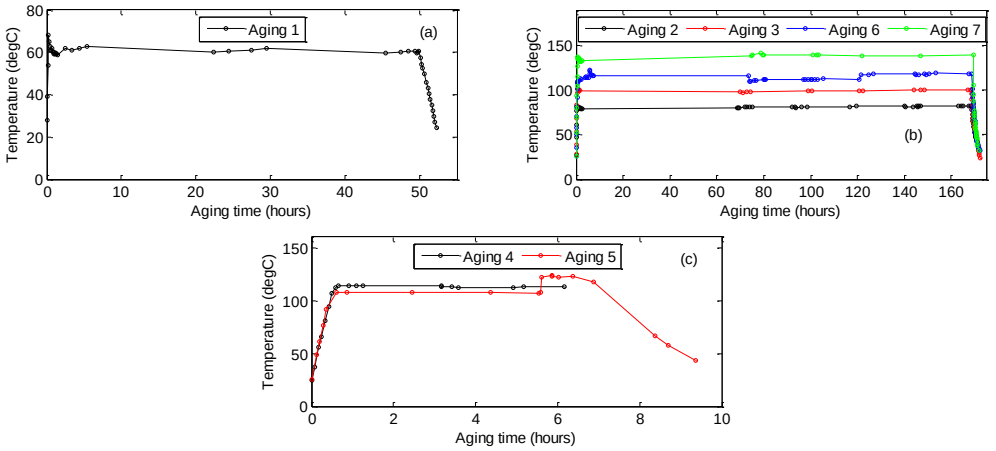


Figure 117 - Thermal aging profiles; (a) aging cycle one 48 hours at an average temperature of 60.8 °C (b) aging cycle two 168 hours at 80.4 °C, aging cycle three 168 hours at 99.4 °C, aging cycle six 168 hours at 114.6 °C and aging cycle seven 168 hours at 136.7 °C (c) aging cycle four 5.5 hours at 113.4 °C and aging cycle five 6 hours at 115.4 °C

Aging profiles one, four and five were short term tests to determine the effect of temperature on the samples. The longer term aging of the samples was carried out in aging cycles two, three, six and seven. The gap in temperature measurements for the long term aging cycles from 5 hours to 70 hours was due to the thermal aging tests performed over a weekend without any monitoring.

The overall aim was to establish allowable limits for thermal aging and produce dielectric samples without significant changes in geometry that have been exposed to accelerated aging.

7.4.2. GEOMETRY CHANGES

The recorded changes in geometry during the seven aging cycles are outlined in this section for each aging cycle.

In aging cycle one four samples were heated at an average temperature of 60.8 °C for 48 hours. In aging cycle two four samples were subjected to 168 hours of thermal aging at an average temperature of 80.4 °C. Minimal changes were observed for these samples.

In aging cycle three four samples were aged at an average temperature of 99.4 °C for 168 hours. The thickness increased and the diameter of the samples reduced. The upper face had appeared to ‘puff up’ in the centre of the disc. This was most

likely caused by the pressure build up inside the cylindrical void. Figure 118 shows a cross sectional view of aged sample A.

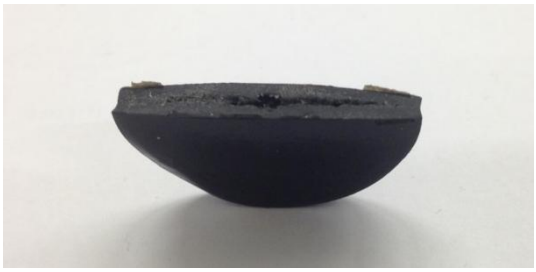


Figure 118 - Aging cycle three thermally aged sample A at 99.4 deg for 168 hours cross sectional view

The purpose of aging cycles four and five was purely exploratory, Figure 119 shows one half disc from each of the two aging cycles. The aim was to understand how samples could be exposed to temperatures above 100 °C, without experiencing the issues of aging cycle three. Two strategies were employed:

- The first approach (aging cycle four) was to thermally age the half discs with cylindrical voids - significant warpage was evident so the thermal aging was stopped.
- In the second method (aging cycle five) a 2 kg weight was placed on the two half discs - the temperature was gradually increased up to a maximum of 123.0 °C without significant warping occurring.

Figure 119 - Aging cycle four half sample aged at 113.4 °C for 5 hours (left) and aging cycle five half sample aged up to 123 °C with 2 kg weight to prevent warpage (right)

In aging cycle six four half discs were aged above the glass transition temperature of ABS (100 °C). The average temperature during the 168 hour hold was 114.6 °C. Aging cycle six uses the 2 kg weight employed in aging cycle five to prevent warpage of the half discs.

In aging cycle seven four half discs were heated for 168 hours at an average temperature of 136.7 °C, Figure 120 shows the four aged samples beside an un-aged sample. The main observations post heating was that the diameter of the half discs had reduced (as well as the diameter of the void) and the thickness of the discs increased.

Figure 120 - Aging cycle seven the four samples subjected to thermal aging (upper) unheated sample (lower)

A summary of the mean percentage changes in the thickness and diameter of the samples for the seven aging cycles is shown in Table XLI.

The largest percentage change in thickness was observed for the samples from aging cycle three. It must be noted that samples aged in cycles one to three were joined and sealed prior to the aging. The move to aging the discs in the raw printed form reduced the increase in thickness in aging cycle four. The inclusion of a weight on top of the raw printed half disc (aging cycles five, six and seven) ensured that the percentage change in thickness remained similar for the three cycles. The largest percentage reductions in diameter were evident for aging cycles six and seven. All 3D printed discs reduced in diameter and the increase in average aging temperature accentuated the effect.

Only samples from aging cycles two, three and seven will be tested under AC conditions. The samples from aging cycles one and six were not tested under AC conditions to maximise the number of virgin thermally aged samples that could be tested under DC conditions. Samples from aging cycles one, two, three, six and seven will be tested under DC conditions in this chapter. The changes in geometry

for aging cycle six and seven were thought to negatively affect the PD behaviour this will be first tested under AC conditions. The short term of aging cycles four and five were mainly used as a learning exercise to determine the physical changes of the samples at elevated temperatures.

In general, when the temperature of the thermal aging was pushed above 100 °C significant changes in geometry were apparent. It is expected that the changes in geometry will have a larger effect than the thermal aging of the ABS plastic, particularly for aging cycles six and seven.

Table XLI - Summary of mean percentage changes in geometry for the aging cycles

Mean quantity	Aging cycle						
	1	**2**	**3**	**4**	**5**	**6**	**7**
Sample IDs	2F, 2G, 2H and 2I	Aged E, F, G and H	Aged A, B, C and D	N/A	N/A	Aged I and J	Aged K
Average temp (°C)	60.8	80.4	99.4	113.4	115.4	114.6	136.7
Aging time (hours)	48	168	168	5.5	6	168	168
Change in thickness (%)	+0.52	+1.86	+44.01	+13.93	+9.39	+15.54	+11.20
Change in diameter (%)	-0.082	-0.15	-2.18	-5.69	-3.73	-7.57	-6.86

7.4.3. AC PD TESTING

The results from AC PD testing conducted on samples from three of the aging cycles are presented in this section. The φ-q-n plots for three samples exposed to each of the aging cycles are detailed in Figure 121.

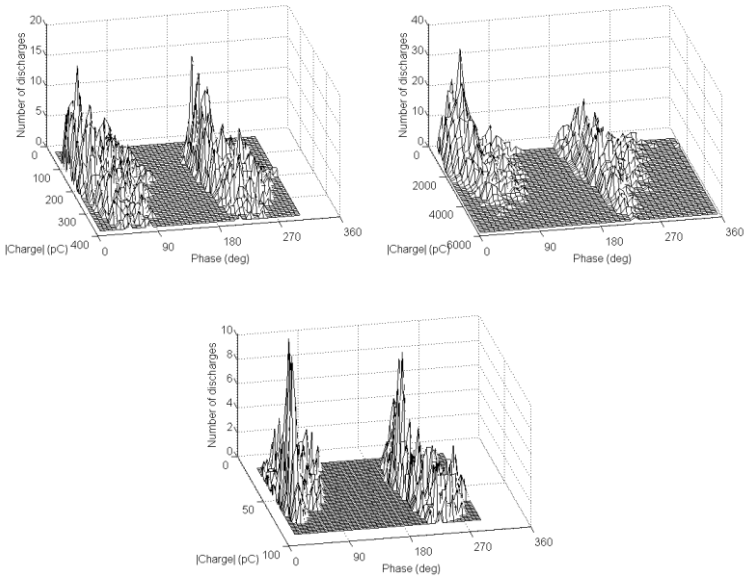


Figure 121 - Comparison of φ-q-n plots: aging cycle two sample H at 6.3 kV rms 30 second segment 4 (upper left), aging cycle three sample B at 9.1 kV rms in 30 second segment 1 (upper right) and aging cycle seven sample K at 9.2 kV rms 30 second segment 1 (lower)

In aging cycle two sample H was tested and internal discharge was apparent from the sample at 6.3 kV rms.

In aging cycle three sample B was tested under AC conditions and the PD activity was recorded. Repetitive and sustained PD was observed in aged sample B at 9.1 kV rms. The behaviour is typical of internal discharge with the majority of PD occurring in the 1st and 3rd quadrants. With the knowledge of the changes in geometry experienced in the samples for aging cycle three. That is the single cylindrical void expanded out to form a large number of voids in parallel where the two half discs peeled apart. There is a distinct spread in PD data with significantly larger PD events recorded than for the original cylindrical void. These results are consistent with the findings of [133] with respect to parallel voids where PD activity with larger magnitude was reported for multiple parallel voids. The inception voltage was also higher than the original 1 mm high defect. Assuming that the 1mm increase in the thickness of the sample led to a 1mm increase in void height the inception voltage can be recalculated.

Paschen's law predicts an inception voltage of 10 kV for a void height=1.918 mm and insulation thickness=3.858 mm. The variation of void height within the disc from very small voids at the edge to a large cavity in the centre would explain the lower

inception voltage than anticipated. The change in void height was the most likely reason for the rise in PD inception voltage.

Sample K which was formed from the half discs from aging cycle seven had an inception voltage of 9.2 kV rms. The expectation is that the reduction in the diameter has affected the inception voltage and also the PD activity at the inception voltage. The PD magnitude is relatively small and the number of PD events was quite low. This was expected with the reduction in diameter limiting the number of potential discharge sites.

A summary table of the AC PD data for the five AC PD tests at each partial discharge inception voltage (PDIV) is shown in Table XLII.

Table XLII - Summary of AC PD data at each PDIV for the aged samples

Aging cycle	Sample ID	PDIV (kV)	Number of PD events	Max |Charge| (pC)	Mean |Charge| (pC)
2	Aged H	6.3	33082	404.25	118.68
3	Aged D	7.1	23242	4139.7	808.76
7	Aged K	9.2	10230	101.89	51.08

The inception voltage was lowest for sample H from aging cycle two at 6.3 kV rms. This was lower than that of the un-aged single cylindrical void sample from chapter 5. In contrast the inception voltage for the aging cycles with higher average temperatures (aging 3 and 7). The primary reason for the reduction in the inception voltage is the reduction in surface area of the void due the contraction of the diameter of the sample. This is also reflected in the reduction in the number of PD events recorded with less discharge sites available in the smaller diameter void. The largest PD event was recorded for sample D which was exposed to aging cycle three the increase in thickness of the sample directly increased the height of the void. A larger void is known to result in larger PD events.

Table XLIII - Summary of AC PD data at each PDIV for the aged samples data separated according to the phase of the AC supply; the positive half cycle (+VE) and the negative half cycle (-VE)

Aging cycle (sample ID)	Number of PD events		mean phase (deg)		Mean |charge| (pC)		Max |charge| (pC)	
	+VE	-VE	+VE	-VE	+VE	-VE	+VE	-VE
2 (H)	16797	16285	44.42	224.61	105.52	132.26	384.46	404.25
3 (D)	8666	14576	50.75	226.55	930.12	736.61	4139.7	3722.5
7 (K)	5051	5179	36.31	234.1	46.34	55.7	84.94	101.89

In general, the number of PD events in each half cycle was similar for all the AC PD data. The main difference was evident for sample D where there was significantly more PD events in the negative half cycle. This unbalance could point towards the void being closer to a particular electrode. This difference was not particularly evident in the PD magnitude data with a small difference apparent for all the samples under test.

The variation of the number of PD events over the first 15000 cycles at each PDIV for the five samples is shown in Figure 122.

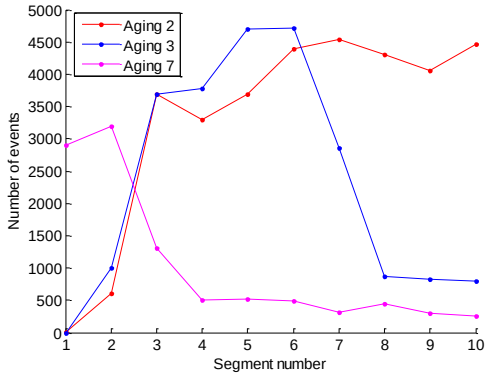


Figure 122 - Comparison of the number of PD events per 30 second segment for the first 10 segments at the AC PDIV

In aging cycles two and three the PD activity was limited over the first few segments then sustained PD activity was established in segment 3 in both cases. The PD activity in aging cycle two continues to grow in the number of PD events over the 10

segments. The number of PD events for aging cycle three initially increases then reduces significantly in segment 8. In aging cycle 7, the number of PD events was initially 3000 events per 30 second segment. The number of events drops significantly in segment 3 and 4 and stabilises around 500-300 events per segment.

The variation of PD magnitude over the first 15000 AC cycles (300 second) at the inception voltage is shown in Figure 123.

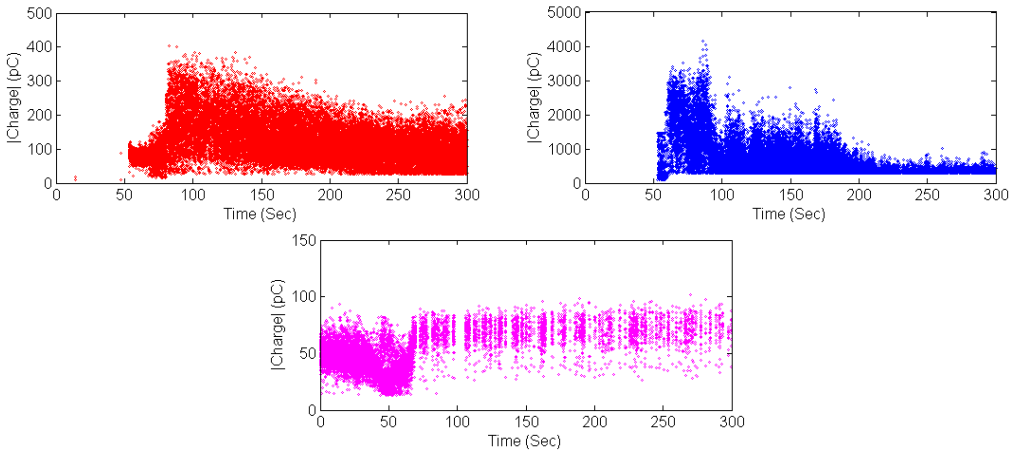


Figure 123 - Variation of AC PD magnitude over the first 300 seconds at PDIV; aging cycle two sample H (red), aging cycle three sample D (blue) and aging cycle seven sample K (magenta)

In both aging cycle two and three the PD magnitude starts to increase after a 50 seconds then comes to a maximum before 100 seconds. Following this, the PD activity reduces in magnitude over the remaining time. In aging cycle seven the intense PD activity is evident at the start over the first 70 seconds. For the remainder of the time the intensity reduces but the PD magnitude increases and the PD activity are in bursts for the remaining time. The PD magnitude in the sample expose to aging cycle seven is significantly less than that of the AC PD test on the aging cycle two sample.

The phase of occurrence of the PD activity in relation to the AC supply over time is presented in Figure 124.

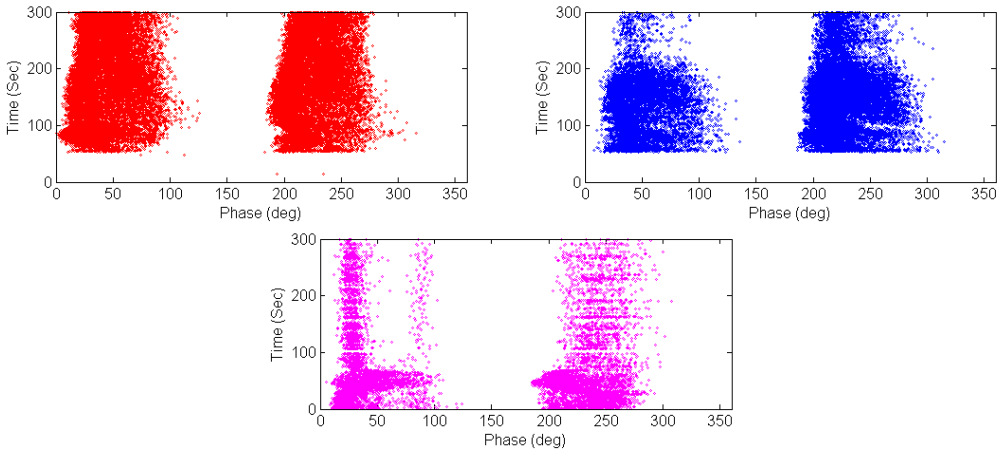


Figure 124 - Phase of PD occurrence over the first 300 seconds at PDIV; aging cycle two sample H (red), aging cycle three sample D (blue) and aging cycle seven sample K (magenta)

The high intensity and consistent PD behaviour in aging cycle two is evident. In contrast, the phase behaviour of the sample exposed to aging cycle three has a wider phase range. It is also evident that the imbalance between the positive and negative half cycles occurs over the final 100 seconds. The intensity of the phase behaviour reduces in the positive half cycle compared to that in the negative half cycle over the same time period. In aging cycle seven the PD activity occurs over a wide phase range and becomes particularly focused in the first quadrant compared to that in the third quadrant. This confirms that a smaller void exists with less but more focused PD activity evident.

The AC PD testing has shown that the samples from aging cycle two exhibited PD which was more like a single void discharging. The samples from aging cycles three and seven have all had some significant change in geometry that has affected the PD behaviour observed. Samples exposed to the same aging cycles will be tested under DC conditions in the following section.

7.4.4.DC PD TESTING

This section details the DC PD testing conducted on the samples exposed to thermal aging cycles. Samples from aging cycles one, two, three, six and seven were PD tested under DC conditions. Where possible DC PD tests were conducted on multiple samples exposed to each thermal aging cycle, in some cases this was not possible (aging cycle seven). The DC PD test results are presented in the following sections.

In aging cycle one four samples which were aged at an average temperature of 60.8 °C were PD tested under DC conditions. The four samples exhibited more PD events than the single void sample tested under DC conditions in chapter 5. Two samples (2G and 2H) had no PD activity during any of the 2 hour hold periods but samples 2F and 2I had significantly more PD events during the hold periods.

The samples from aging cycle two were aged at an average temperature of 80.4 °C for 168 hours. Three samples were tested under DC conditions samples E, F and G. Thermally aged samples E and F were tested using the defined hold periods. Aged G was tested a little different the voltage was increased directly to 25.8 kV and was held constant at this voltage for 9 hours and 53 minutes but the only activity observed was during the ramp up to 25.8 kV. Generally, more PD events were apparent during the hold periods for samples E and F than aging cycle one and aged sample G (single voltage step and 10 hour hold).

Two samples from aging cycle three were tested under DC conditions using the ramp test method. There were more PD events and in general they were larger than the PD activity recorded during the DC PD tests on samples from aging cycles one and two. The main reason for this difference in activity is the change of geometry in the sample which has also increased the size of the void (in diameter and height). The defect in the sample could be equated to a number of parallel voids across the thickness of the sample. This leaves more potential sites for PD activity to occur thus increased activity was observed in both cases.

Two dielectric samples (aged samples I and J) which were aged using thermal aging cycle six were tested under DC conditions. In the DC PD data a limited number of PD events were recorded during voltage changes or hold periods. Sample I was badly affected by noise from testing conducted in a neighbouring lab. During the holds at 19.7 kV and 26 kV noise was apparent for extended periods. The PD magnitude was negative and positive polarity all less than 15 pC this behaviour was not apparent in any other samples to date. One reason for the lack of PD activity is the fact that the overall diameter of the sample reduced whilst the thickness increases. The surface area of the void has reduced, leading to fewer sites to initiate PD activity and a reduction in overall PD activity.

One dielectric sample (aged sample K) from aging cycle seven was tested under DC conditions no PD activity was recorded during the ramp test. This sample suffered from a significant reduction in the diameter of the void during the thermal aging

process. The geometry change has undoubtedly affected the resulting DC PD activity. The maximum AC PD magnitude was 101.89 pC, so any PD activity could also have been a fraction of this and difficult to detect.

The findings from the DC PD testing conducted on the thermally aged samples with the PD activity recorded during voltage changes and hold periods separated. A summary table comparing unaged and aged samples is detailed in Table XLIV.

The samples aged below 100 °C (aging cycle one and two) had the smallest dimensional changes so are best compared with one another. In the samples from these cycles the PD magnitude and number of PD events was shown to increase when the temperature was increased. In aging cycle three the change in geometry of the void itself led to a sample that was very active with large PD events. The two changes in void geometry for aging cycle three was the increase in height and diameter of the void. The increase in diameter was thought to be more important as this allowed more potential discharge sites to exist. Aging cycles six and seven were adversely affected by the changes in geometry of the overall dielectric sample. In particular, the reduction in diameter of the disc led to a reduction in the diameter of the cylindrical void. This change led to less potential discharge sites and the delay in electron availability at these sites may be the reason for the difference in the inception voltage under AC conditions for these smaller voids.

Table XLIV - Summary table of DC PD testing on unaged and aged samples

Quantity	virgin cylindrical void	Aging cycle			
		1	2	3	6
Sample IDs	Cyl. Void C	2F, 2G, 2H and 2I	Aged E, F and G	Aged B and D	Aged I and J
Aging temperature (°C)	N/A	60.8	80.4	99.4	114.6
Mean |Charge| AC (pC)	14.56	untested	118.68	808.76	untested
Number of samples tested	3	4	3	2	2
max |Charge| during volt change (pC)	132.88	163.33	172.3	352.47	47.17
mean |Charge| DC voltage change (pC)	101.29	94.57	76.31	160.99	32.79
No events during changes	3	7	10	15	3
max |Charge| during hold (pC)	37	78.78	174.89	497.88	64
mean |Charge| DC voltage hold (pC)	37	26.36	52.44	107.1	37.86
No events hold	1	9	13	38	2

7.5. DISCUSSION

A range of temperatures were considered and ASTM F1980 [168] was used to equate a sample which has been thermally aged to the equivalent time at an ambient temperature of 25 °C for the same aging to occur. Thermal aging was conducted over a range of temperatures (60.8 to 136.7 °C) for up to 168 hours. The

temperature of the oven during the thermal aging process was manually recorded. The temperature sensor was placed as close to the samples as possible inside the oven to ensure the temperature of the samples was being measured. The assembly of dielectric samples was varied in two ways prior to the thermal aging process:

- The first approach involved the preparation of the two halves for joining, the joining process and final sealing prior to aging
- The second approach was to use the raw printed half discs then after the aging process the half discs were prepared for joining, joined and sealed

The first approach suffered limited dimensional changes during aging cycle one and two (up to an average temp of 80.4 °C). In cycle three when the average temperature was 99.4 °C the upper half disc mushroomed up in the middle of the sample (average increase of +44.01 %). The layers appeared to peel apart due to the pressure that built up inside the cylindrical void. The second approach was employed to allow the samples to be heated above 100 °C. In order to minimise the warpage of these discs a 2 kg weight this was successful. A second effect which became apparent was the reduction in diameter of the half discs as the temperature was increased up to a maximum average of 136.7 °C. This also reduced the diameter of the cylindrical void with the largest effect evident following aging cycle seven. The samples from aging cycles six and seven suffered from significant changes in geometry. The expectation was that these changes in geometry would have a larger effect than the thermal aging of the dielectric material. The main outcome from the thermal aging process was that it was challenging to age 3D printed samples above 100 °C due to warpage and dimensional changes.

The AC PD testing of the aged samples was a valuable sense check prior to conducting DC PD testing. The PDIV for aging cycle two (6.3 kV) was lower than that of the virgin sample (7.3 kV rms). The mean charge of PD activity at the inception voltage was higher in aging cycles one and two than the virgin sample. Void type discharge was evident on the φ-q-n plot for these samples. The sample aged in cycle three had an inception voltage of 9.1 kV rms and the PD magnitude was significantly higher. The main reason was the increase in void size in height and width. The sample from aging cycle seven had higher inception voltages (9.2 kV rms) and lower PD activity. On the φ-q-n plot internal discharge was still evident.

During DC PD testing as many samples were tested as possible for each aging cycle, this was to enable as much DC PD data to be gathered as possible. In some

cases (aging cycle seven) the physical changes of the sample meant no void was still present so only one sample was assembled from the samples with the largest voids. The ramp test method was employed with voltage hold periods of 2 hours. In general, more and larger PD events were evident from the samples from aging cycles one and two than the virgin samples from chapter 5. The samples from aging cycle three were the most active with large PD events recorded and significantly more activity also apparent. The samples exposed to aging cycle six had limited PD activity, more similar to that of a virgin sample. No PD was observed from the single sample exposed to aging cycle seven.

7.6. CONCLUSIONS

The electrical and thermal aging of samples was investigated through a search of available literature. Based on available literature the most effective way to age dielectric samples was to combine electrical and thermal aging to dielectric samples simultaneously. The thermal aging of dielectric samples was determined to be more effective than electrical aging based on literature sources. The long term electrical aging of samples was challenging in the available lab facilities. This study considered the PD behaviour of thermally aged void type dielectric samples under AC and DC conditions. The method from ASTM F1980 [168] was employed to determine equivalent aging time of the samples at elevated temperatures to that of samples aging at ambient temperature.

The thermal aging of 3D printed parts brought significant challenges mainly due to the fact that the print material is a thermoplastic, as such any heating leads to the softening of the ABS. A range of temperatures was considered to determine the changes in geometry and the possible aging by performing PD measurements on the samples. When the material was heated geometric changes were evident. The main outcome was that it was challenging to thermally age 3D printed samples above 100 °C due to warpage and dimensional changes. The recommendation would be to age samples at a maximum average temperature of 80.4 °C and increase the aging time beyond 168 hours. Further steps in the aging temperatures may enable a higher acceptable temperature to be established.

The AC PD testing of the aged samples was a valuable sense check prior to conducting DC PD testing. The PDIV for aging cycle two (6.3 kV) was lower than that of the virgin sample (7.3 kV rms). The mean charge magnitude of PD activity at

the inception voltage was higher in aging cycles one and two than the virgin sample. This shows that the aging temperature did have an effect on the aged samples. The samples in the other aging cycles all suffered from significant changes in geometry which was more dominant than the aging of the dielectric material.

Under DC conditions the samples aged below 99.4 °C were more active and PD events were on average larger than that of the virgin samples from chapter 5. The samples aged above 99.4 °C suffered significant changes in geometry, this affected the DC PD behaviour with generally smaller and less frequent PD events apparent. The changes in geometry had a larger effect than the degradation of the dielectric material when the aging temperature was above 99.4 °C.

Areas of investigations for future work include:

- The investigation of electrical aging as the effects were mainly due to the fact that ABS is a thermoplastic
- Alternative filament materials could be considered which could have a different response to the thermal aging process. This could include reduced changes in geometry at elevated temperatures or an alternative glass transition temperature
- The design of the sample itself could be altered to improve the thermal response, possibly thicker samples or thicker sacrificial layers
- Alternatively the geometric changes due to elevated temperature could be trialled and the anticipated changes could be designed into the samples. This would ensure the samples are the required size at the end of the thermal aging process
- The elongation of the thermal aging time rather than increasing the aging temperature could also be considered. Alternative temperature ranges below and around 100 °C could be investigated in more detail
- The inclusion of material testing to determine key properties (dielectric strength, permittivity etc.) could also be examined
- The dissection of samples and SEM imaging before and after thermal aging would also be interesting avenues to explore

8. METHOD TO INTRODUCE VOIDS USING SSLE

This chapter details the investigations of inducing a void type defect inside a dielectric material. The method of sub surface laser engraving (SSLE) was employed to determine if small controllable voids can be introduced into the sample. In this chapter the technique and common application areas will be outlined. The test setup and electrical test method will be introduced. Samples with no defects were initially tested under AC conditions to determine the voltage threshold for electrical testing. The test results from AC PD testing of the samples are detailed for the wide range of defects created in the dielectric material. The main objective is to determine whether this method is a valid approach of introducing void type defects inside an insulation sample. A further objective is to investigate the type of defect introduced through using a SEM system to image the cross section of samples with manufactured defects. Within this study no internal PD activity was evident from a wide range of manufactured defects inside PET film samples. It is expected that further exploration of the technique could unlock interesting avenues of research.

8.1. ASSOCIATED LITERATURE

The literature review from chapter 5 considered a wide range of papers related to different methods to consistently create voids will not be considered in this chapter. The approach considered in this chapter is very similar to that of the 3D printing method from chapter 5 but could allow smaller defects to be introduced inside the dielectric sample. The literature review for this chapter will focus on the studies to date surrounding micro voids, the SSLE technique and applications of SSLE to date.

Early work from Densley *et al.* [169] considered spherical voids of tens of micrometers in diameter. The concentration of these microspheres and the size was studied. The PD activity observed was reported and compared to samples with no voids. Care was taken during the manufacturing process such that the PD activity would be detectable, by limiting the thickness of the insulation samples to less than 0.5 mm. The microspheres were formed by immersing hollow glass and phenolic spheres in the polyester resin. The inception voltage for PD activity was significantly higher than predicted using Paschen's law.

Burgener *et al.* [170] considers the time delay for the arrival of a starting electron for the ionisation process central to PD activity. Calculations were conducted to

understand the probability of occurrence of PD activity with the aim of understanding the key properties of the void that affect PD inception. The geometry of the void was found to have a larger effect than the void pressure and the type of voltage applied when the electric field was high enough.

Lerchbacher *et al.* [171] investigated the PD behaviour of epoxy resin samples with micro voids. The samples were formed by casting epoxy resin discs and hollow glass spheres were included during the casting process. The diameter of the micro spheres ranged from 75-106 μm. During testing the test cell was immersed in mineral oil which allowed the oil reservoir to be heated to allow the variation of temperature for the samples.

Ueta *et al.* [172] investigated the behaviour of micro defects which could not be picked up by the quality control process at the factory producing epoxy insulators. The three representative defects were defined as cracks, voids and delamination. Approaches were developed to manufacture the three defect types in insulation samples. The PD behaviour of such defects are investigated and discussed. The samples with crack defects had the lowest breakdown voltage.

Lu *et al.* [173] describes the use of a 'laser inside carving machine' to manufacture a void in acrylic. The paper describes the void being embedded in the acrylic between the electrodes. It is unclear whether the acrylic is formed by stacking sheets with one sheet having a cylindrical void removed by the laser. No other publications on this topic could be found and limited detail was presented in this paper.

Yanaze *et al.* [174] investigate the PDIV and breakdown voltage of insulating material with multiple micro cavities (5, 11 and 34 μm). The samples were exposed to X-ray radiation to provide the starting electron for the ionisation process. This was found to minimise the time lag for the starting electron. The breakdown voltage and PDIV was found to be higher for the samples with smaller cavities.

Literature related to the sub surface laser etching (SSLE) process was investigated. To date this technique has not been applied to electrical testing of dielectric samples. A review article on the application of lasers for micromachining is [175]. The system operation is discussed and can generally induce an optical change or even a void. A general review of techniques is outlined with the main application being waveguides and the ablation (material removal) of the parent material.

The publication [176] considers the development of ultra fast laser systems. The reducing cost of these systems will allow increased adoption in scientific and medical fields. Applications of ultra fast laser systems includes; high accuracy machining, optical variation of materials and surgical tools. The review article from Keller [177] presents the developments of ultrafast laser systems. The general trend is for the reduction in size of the systems, increase in power intensity and rapid rise in repetition rates.

The paper from Salter *et al.* [178] investigates how the depth range of the laser system can be extended for ultrafast laser machining. This is achieved by using a liquid crystal spatial light modulator (SLM). The application of a method to fabricate single and multiple points was presented.

One area which has received significant interest is the use of SSLE to optically change scintillator crystals. Early work by Moriya *et al.* [179] investigated the application of SSLE to scintillators for position emission tomography (PET) used for molecular and genomic imaging. SSLE was used to produce refractive index changes inside the crystal. The arrays engraved were 2D and of various patterns using a neodymium-doped yttrium aluminium garnet (Nd:YAG) laser. Later work from Moriya *et al.* [180] expanded on the approach. Specific focus was placed on the capability of the SSLE system to induce defects in thicker scintillation crystals and to reduce the total laser energy required. Approaches to enable this were analysed. An optical microscope was used to study the defects introduced during the SSLE process.

Yamauchi *et al.* [179] details the development of a depth of interaction detector for use in PET. A LYSO scintillator pillar was segmented using SSLE.

Konstantinou *et al.* [181]–[183] have a number of publications related to the use of SSLE. SSLE was used to create optical barriers inside pixelated scintillator crystals for gamma radiation detectors. The approach allows a wide range of pixel geometries to be included inside the crystal. The SSLE process allows optical discontinuities to be introduced in the form of micro cracks and micro-ablations. The geometry of the engraved points was modelled on a 3D modelling package then transferred to the bespoke SSLE system. The controllability of the approach was a distinct advantage in allowing non-conventional shapes to be included inside the crystal.

Hunter *et al.* [184] studied the use of SSLE to allow depth dependant light sharing between a pair of crystals in a dMiCE discrete scintillation detector. Early approaches required that the crystal be cut and an interface was manually formed (a basic manual sanding action). A SSLE system was employed to quickly introduce a boundary in the crystal to control light distribution. The SSLE process is automated so brings significant time savings and was relatively inexpensive.

An important area of study is detecting and measuring voids created in material without the need to destroy the sample. Contin *et al.* [185] present a study using X-ray computed tomography (X-CT) to deduce the features inside the insulation wrapped round the copper bars from AC machines. A portion of the insulation was removed from the copper bar. A 3D representation of the makeup of the insulation is provided by the system with voids highlighted as grey areas on the scanned image. The X-ray source passes through the insulation sample and a charge-coupled device (CCD) was used to detect the X-rays. The intensity of the X-rays is determined by the density of the insulation. The sample was rotated in small steps to allow the reconstruction of a 3D image by combining the responses of the CCD. The approach allowed a representation of the small voids between insulation layers.

8.2. MANUFACTURING METHOD

This section examines the SSLE manufacturing methods and associated systems. Two batches of dielectric samples with defects will be created then tested. Paschen's law was used to predict the inception voltage for the range of defects introduced in each batch. Tests will be performed to both assess the void creation process and compare with predicted results

8.2.1. SUB SURFACE LASER ENGRAVING (SSLE) PROCESS

SSLE is commonly used to create 3D images in glass blocks to enable the visualisation of 3D models. To date, the main applications of SSLE have been to change the optical performance of the parent material. Limited work has been carried out to exploit SSLE in the production of voids in materials. The creation of defects utilising this method is completely novel.

A 3D image of the pattern to be engraved can be generated by a user. This is used as an input to the laser control software to determine the operation of the laser. Figure 125 shows the level of detail and fine control (micron level) that can be achieved using SSLE.

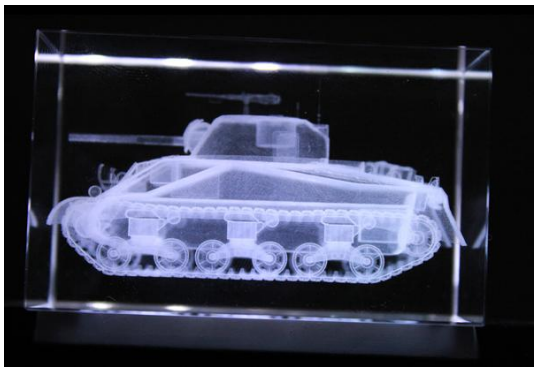


Figure 125 - A 3D image inside a block of glass using a commercially available SSLE machine [186]

The method was first used in the 1990's and has become more cost effective over the years with improvements in laser technology. The majority of commercially available SSLE machines use diode pumped solid state (DPSS) laser. The diode within the laser degrades over time and is an expensive consumable. The operation of such a system requires significant skill and experience especially to develop the 3D image and to ensure the setup is appropriate for the material at hand.

The SSLE process relies on the base material being transparent to enable the focusing of the laser beam to a particular location inside the base material. The most common material used in this process is glass, however many transparent plastics can also be engraved. The technique relies on the laser beam being focused on a certain point inside the volume of the material. The focal point of the beam vaporises the base material at a precise and controllable location. The focal point is generally very small and only the material within the area of the focal point is affected which allows for the fine control of etching. There is a limitation on the size of defect introduced during this process, if the defect is too large then material fracture can occur.

Typical SSLE systems operate at high speed at a micron precision level. The SSLE machine consists of three main subsystems:

- The laser is used to form the high intensity light beam required to vaporise the base material during sub surface etching.
- The actuation system enables the orientation of the laser head to be varied in x, y and z coordinates above the base plate of the machine (where the material is placed).

- The controller is used to determine the operation of the laser beam whether it be intensity, the focusing point of the beam of light and the movement of the actuators (laser head) to enable the production of the desired 3D image.

8.2.2.SSLE SYSTEM EMPLOYED

An SSLE machine was made available by the department of engineering science at Oxford University. The machine was operated by Dr Patrick Salter who is an experienced and skilled operator. The system used was built and developed by the team at Oxford and, as such, is a bespoke device [178], a schematic diagram of the system is detailed in Figure 126.

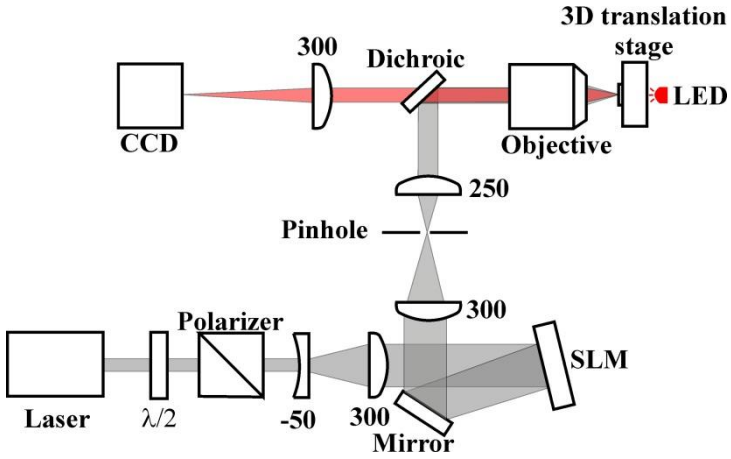


Figure 126 - Nanofab system schematic detailing the LED illuminated inspection stage (upper in red) and the laser focusing stage (lower in grey) [178]

As can be seen in Figure 126, the laser beam is attenuated by a half wave plate and a polariser (Glan-Laser). The laser beam was then expanded onto a reflective phase-only liquid crystal spatial light modulator (SLM). A mirror then reflects the laser beam onto the focusing stage where the laser beam and the image from the objective lens were imaged onto each other. This required the use of achromatic lenses to focus the two light sources to the same point at the pinhole. This allowed the site that the laser beam will be focused on to be visualised using a light emitting diode (LED) light source and charge-coupled device (CCD) essentially a light sensor. In this work a Brightfield microscope (illuminated by the LED light) enabled the inspection of the specimen during fabrication.

The system is comprised of two key subsystems the laser/focusing system and the imaging to monitor the fabrication process. The laser is manufactured by Spectre-physics and consists of a regeneratively amplified titanium sapphire. The specification of the laser system is outline in Table XLV.

Table XLV - Properties of the Spectre-physics Solstice laser unit [178]

Property	Value
Pulse length (fs)	100
Repetition rate (kHz)	1
Central wavelength (nm)	790
Maximum pulse energy (mJ)	2

During the fabrication process the polymer sample was mounted on a three axis air-bearing transition stage (Aerotech ABL10100 (x, y) and ANT95-3-V (z)). The system was initially trialled on spare samples allowing the focusing and laser settings to be dialled in. Based on the trials a single 'burn' had approximate dimensions of 1x1 μm across the plane of the polymer (X and Y directions) and 4 μm through the thickness of the film sample (Z direction). Defects larger than this were produced by scanning this 'core unit' to form the defined defect geometry as a volume. The process of introducing the defined defects was very fast with the majority of time being the mounting/alignment of the sample prior to the fabrication process.

8.2.3. DIELECTRIC MATERIAL

The dielectric materials used for this work were sheets of polyethylene terephthalate (PET). The film material was manufactured by Dupont Teijin films and is their Mylar A grade. Films of two thicknesses were considered; 125 μm and 190 μm. Mylar was employed in this work as it was spare material left over from a previous study. One option could have been to consider materials already used in the SSLE process such as glass. The key specifications from the Mylar data sheet [187], [188] are detailed in Table XLVI.

The dielectric strength tests [164] quoted in the data sheet were conducted using a ramp up of 500 V per second until breakdown occurs, thus these breakdown strength values should be higher than is achievable in the HV lab. After consultation

with the Oxford group it was agreed that this material was suitable for SSLE, the materials 'haze' value was a significant factor in this decision.

Table XLVI - Key properties from Mylar data sheet [187], [188]

Film thickness (µm)	**125**	**190**
Breakdown strength (kV)	13.5	17.5
Haze (%)	45	82

A key property not available on the data sheet was the dielectric constant. Further work was carried out with Dupont Teijin films to determine the dielectric constant, a value of 3.3 [189] was anticipated, this will be used for theoretical calculations.

8.2.4. MANUFACTURED DEFECTS

The defects described in the following section were produced in two batches:

- The first trial batch consisted of a wide range of defects with variations in the x and y axis to see if any PD could be observed using this method.
- The second batch took forward the most promising defect types and varied the defect heights in the z-axis to lower the PD inception voltage. All defects were introduced midway through the thickness of the films.

8.2.4.1. Batch 1: Trial

Table XLVII details the film thickness, the defect introduced and each defect has been given an identifier (to aid the discussion below).

Table XLVII - Details on defects induced in the film sample for batch 1

Sheet thickness (µm)	Identifier	Defect type
125	A1, A2	single defect ~5 µm
	B1, B2	2 defects (~5 µm) with 10 µm separation
	C1, C2	~40 µm channel
	D1, D2	single 5 µm defect on the surface
190	A1, A2	20x20 µm square defect
	B1, B2	10 x 10 grid of defects, 20 µm spacing
	C1, C2	single defect (~5 µm)
	D1, D2	100x100 µm square defect

Microscope images of the 125 µm defects are shown in Figure 127 all images are to the same scale.

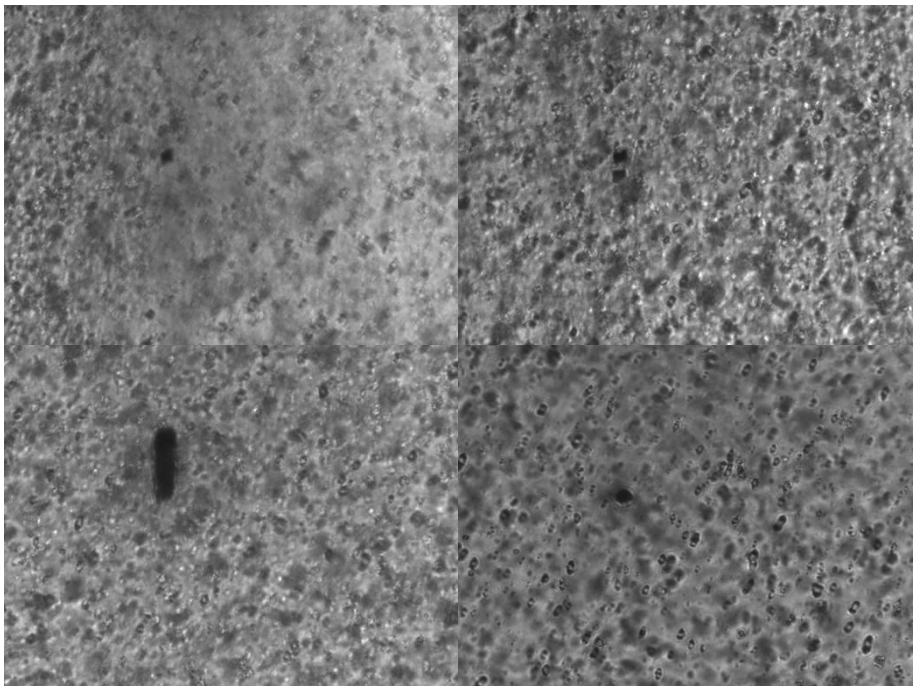


Figure 127 - Images of defects (a) single 5 µm defect (b) two 5 µm defects (c) ~40 µm channel (d) single 5 µm defect on the surface

Some diffusion of the image is evident due to the defects being introduced midway through the thickness of the dielectric. Figure 128 shows the images of the defects inside the 190 µm film samples (all images to the same scale).

The approximate geometry of the defects in the z axis (through the film thickness) was 4 µm. No attempt was made in these samples to apply variation in the z direction.

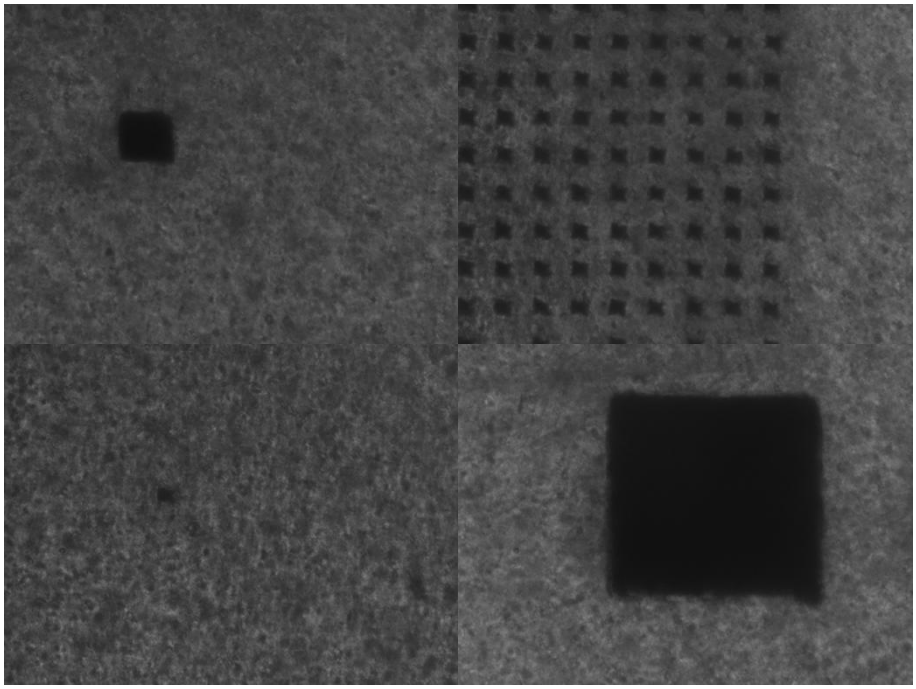


Figure 128 - Defects inside the 190 µm films (a) single 40 µm defect in the middle of the film (b) a 10 by 10 grid of defects in middle of layer (c) single 5 µm defect (d) single 100 µm defect

8.2.4.2. Batch 2: Refined Batch

The second batch was solely based on the 125 µm film with the aim of maximising the ratio of void to overall film thickness and to increase the size of the void in the x-y axis. A void with a larger surface area (x-y axis) allows more potential discharge sites to exist. The increase in capacitance due to a larger void height (z-axis) enables larger PD events to be apparent from the void in question during electrical testing. The defects introduced in batch 2 are shown in Table XLVIII.

Table XLVIII - Details on defects induced in the film samples for batch 2

Sheet thickness (µm)	Identifier	Defect type
125	A1-A3	100x100 µm approx. 10 µm depth
	B1-B3	100x100 µm approx. 25 µm depth
	C1-C3	100x100 µm approx. 40 µm depth

For the processing in Batch 2, a pulse energy of 250 nJ was used and fabricated a 100x100 µm square by scanning the focus at 0.2 mm/s with a line separation of 1 µm. The geometry of this defect required multiple scans through the thickness of the film. Samples A had 2 layers of this structure separated axially by 5 µm, Samples B had 5 layers and Samples C had 8 layers. As the defect geometry was the same when viewed on an optical microscope images of sample A1 and C3 are detailed in Figure 129.

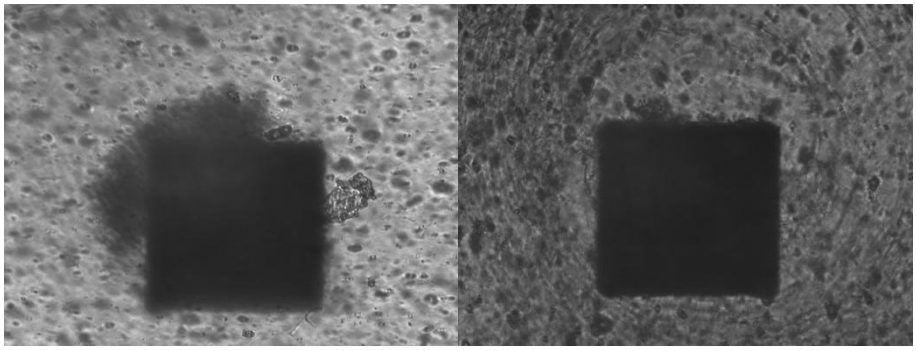


Figure 129 - Images of batch 2 (a) sample A1 a 100x100 µm defect which is approximately 10 µm depth (b) sample C3 a 100x100 µm defect which is approximately 40 µm depth

8.2.5. PASCHEN'S LAW

The aim of this sub-section is to predict the AC inception voltage for the defects introduced in the film material. In this work Paschen's law was used to determine the inception voltage of PD activity. This modelling approach was been used in chapter 5 to predict the inception voltage of PD under AC conditions. The prediction for the inception voltage for batch 1 and 2 is discussed in the following sections.

8.2.5.1. Batch 1

The Paschen's law model was used to determine the inception voltage for the defects introduced in Batch 1. Both 125 and 190 µm film samples were used in

batch 1, all samples had the same defect size through the thickness of the film, which was 4 µm. The inception voltage for the film samples with 4 µm high defects were simulated with the variables in the calculations as detailed in Table XXIV.

t_s is the film thickness, ε_r is the relative permittivity, P is void pressure and the spacing across the void (height) is L. Initially, PL was calculated to allow variable A, B and C to be determined. This enabled the breakdown strength (E_g) of the gas inside the void to be calculated using equation 28. Finally the inception voltage could be calculated using equation 29.

Table XLIX - Paschen's law model data for 125 and 190 µm films

Variable	Film thickness (µm)	
	125	**190**
***G* (µm)**	125	190
ε_r	3.3	3.3
***P* (kPa)**	100	100
***L* (µm)**	4	4

Table L details the results from the calculations.

Table L - Results from calculations using Paschen's law for 125 and 190 µm films

Variable	Film thickness (µm)	
	125	**190**
***PL* (kPa.m)**	$4x10^{-4}$	$4x10^{-4}$
***A* (kV/kPa.m)**	329.39	329.39
***B* (kV)**	$12.077x10^{-6}$	$12.077x10^{-6}$
C	2.2495	2.2495
E_g (kV/m)	$8.6104x10^{4}$	$8.6104x10^{4}$
V_i (kV)	3.5016	5.1975

The prediction of inception voltage was 3.5 kV rms for the 125 µm film and 5.2 kV rms for the 190 µm film, well below the dielectric strength of the film material. The main assumption in these calculations was that the void pressure was 100 kPa.

8.2.5.2. Batch 2

Batch 2 only used the 125 µm film samples. The geometry of the defect in the z-axis was varied, three void heights were considered; 10, 25 and 40 µm. The geometry of the void in the x and y axis was fixed at 100 µm to ensure a large surface area for PD to initiate. The aim of this work was to lower the inception voltage further and confirm whether there was any internal PD from the test samples.

Paschen's law was used to determine the inception voltage for the three void geometries. The variables used as an input to the calculations are shown in Table LI.

Table LI - Paschen's law model data for 125 µm film with 10, 25 and 40 µm high defects

Variable	Void height (µm)		
	10	**25**	**40**
***G* (µm)**	125	125	125
ε_r	3.3	3.3	3.3
***P* (kPa)**	100	100	100
***L* (µm)**	10	25	40

With *PL* calculated the values of *A*, *B* and *C* could be derived, this allowed the breakdown strength to be calculated and finally prediction of the inception voltage. The results from the calculations are detailed in Table LII.

The calculations predicted an inception voltage of 1.6 kV rms for the 10 µm high defect, 1.15 kV rms for the 25 µm and 1.05 kV for the 40 µm high defect. The inception voltages are significantly lower than the previous 4 µm defect in batch 1. The wide range of defect size in the x, y and z-axis should be sufficient to enable conclusions to be drawn on whether a void type defect can be effectively introduced using the SSLE process.

Table LII - Results from calculations using Paschen's law for 125 µm film with 10, 25 and 40 µm high defects

Variable	Void height (µm)		
	10	**25**	**40**
***PL* (kPa.m)**	$1x10^{-3}$	0.0025	0.004
***A* (kV/kPa.m)**	30.25	30.25	30.25
***B* (kV)**	3.12	3.12	3.12
C	0.675	0.675	0.675
E_g (kV/m)	$3.6074x10^4$	$2.083x10^4$	$1.5990x10^4$
V_i (kV)	1.6179	1.152	1.0514

8.3. AC PD TEST METHOD FOR FILM SAMPLES

The test methodology, circuit and test cell detailed in chapter 5 were employed to test both batches of samples. AC PD test method for film samples us is based on another method presented in chapter 5. Samples were tested under AC conditions to confirm whether internal PD activity was apparent.

Great care was taken to ensure each test was identical so as not to skew results and allow valid comparison of samples. The physical connection between the coupling capacitor and the test cell was consistent, through using the rigid brass connections detailed in chapter 5. A torque screwdriver (Wera 7460) with a pre-set torque of 0.3 Nm was used to apply the same toque to the samples when clamped between the two plane electrodes. The test cell was also placed in an oil bath to remove any effects at the triple junction between the electrode, dielectric sample and surrounding air. Additionally, to ensure the test setup was PD free, initial testing of non-defective samples was conducted.

8.4. TEST RESULTS

This section details the results from AC testing performed on the film samples. Samples with no defects were first tested to ensure the test cell was PD free and also to determine the voltage at which PD activity relating to material damage became apparent. Following this verification stage, samples with manufactured defects were tested to determine the inception point of repetitive and sustained PD activity.

8.4.1. NON-DEFECTIVE SAMPLES

The sample under test had no manufactured defect to enable the determination of the upper voltage limit for AC testing on the defective samples.

Non-defective samples of 125 µm and 190 µm film were tested under AC conditions. During AC testing of the 125 µm sample no PD was detected up to 8.7 kV rms (12.4 kV peak). The 190 µm non-defective sample was PD free up to 11.3 kV rms (16 kV peak). Generally, above these two voltage levels the PD activity would quickly increase. PD was generally apparent across the full phase range, this was indicative of damaged dielectric rather than a defective sample or PD producing defect (Figure 130).

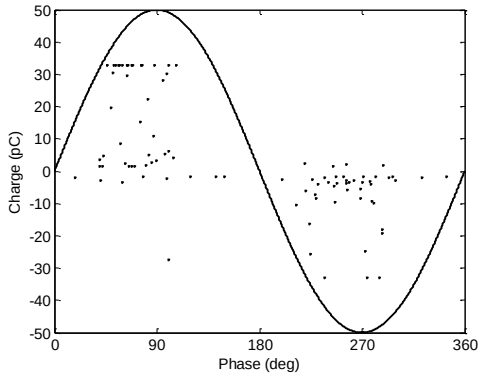


Figure 130 - Non defective 125 µm film at 10 kV rms

8.4.2. BATCH 1

The verification test above has proven that the test setup is PD free and established an understanding of the behaviour of the film materials under AC excitation. A wide range of different defects were introduced to see the relative effects in terms of AC PD behaviour. The defects introduced ranged from small single defects to large arrays of defects. The summary of AC PD test results is detailed in Table LIII.

Table LIII - Sample details and observations from AC PD tests on each sample from batch 1

Film thickness (μm)	Identifier	Defect type	Observation during AC PD test
125	A1	single defect ~5 μm	Sample broke down at 8.6 kV rms
	B1	2 defects (~5 μm) with 10 μm separation	No PD up to 8.2 kV rms
	C1	~40 μm channel	PD at 8.3 kV which quickly increased in magnitude
	D1	single defect on the surface	No PD up to 8.3 kV rms
190	A1	20x20 μm square defect	No PD up to 11.2 kV rms
	B1	10x10 grid of defects, 20 μm spacing	PD observed at 10.5 kV rms
	C1	single defect (~5 μm)	No PD up to 11.3 kV rms
	D1	100x100 μm square defect	No PD up to 11.3 kV rms

The breakdown in the 125 μm sample A1 occurred at the triple junction interface, the possible cause could have been the presence of an air bubble compromising the insulation of the mineral oil. The PRPD plots for the samples that emitted PD are detailed in Figure 131.

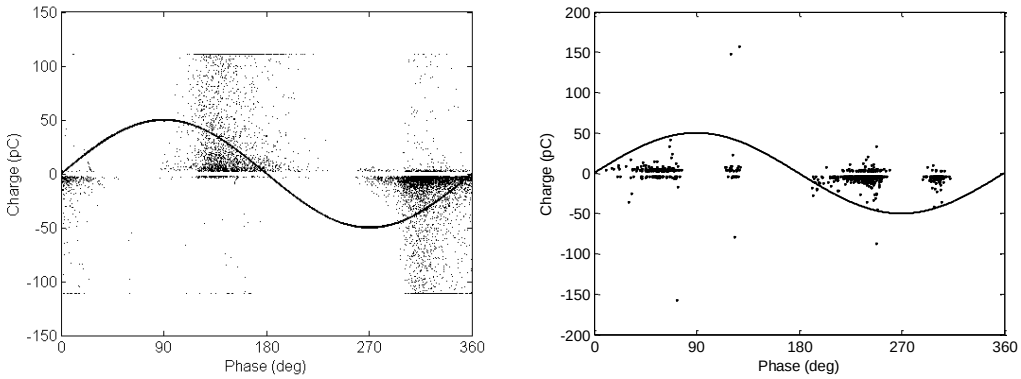


Figure 131 - 190 µm defect B1 at 10.5 kV rms for 20 sec (left) 125 µm defect C1 at 8 kV rms for 52 seconds (right)

Only one sample exhibited any PD activity below the defined breakdown voltages and that was the 190 µm film sample B1. The PD activity occurred in the 2nd and 4th quadrants as opposed to the 1st and 3rd quadrants expected for void type discharges. The activity appears to be more like material damage with PD occurring over a wide phase range in each quadrant. The second sample to emit PD was 125 µm sample C1 with small PD events observed at 8.3 kV over a 1 minute measurement period. This PD activity was recorded at the voltage limit defined from testing defect free 125 µm film samples.

In both cases it is difficult to justify that the PD activity recorded is internal discharges with the most likely cause being material damage. The samples for batch 2 were altered in two ways:

- Enlarging the defects induced in the x, y and z axis. The enlargement in the x and y directions would increase the surface area of the void allowing more potential discharge sites
- Increasing the defect size in the z direction acts to lower the PD inception voltage.

8.4.3.BATCH 2

Tests were carried out on three defects types within batch 2, each defect had the same geometry in the x-y axis. The only variation was the defect size in the z-axis (through the thickness of the sample) and the defect was always introduced midway through the 125 µm film sample. Three different defect heights were laser etched into the film material these were; 10, 25 and 40 µm. Three identical samples were produced for each defect type and each sample was tested under AC conditions.

The aim was to determine whether internal PD activity was emitted from the SSLE manufactured defects.

A summary of the AC PD test results for batch 2 is presented in Table LIV.

Table LIV - Sample identifier, defect type (XxYxZ) and observations from AC PD tests on each sample from batch 2

Identifier	Defect type (µm)	Observation from AC PD test
A1-A3	100x100x10	A1 broke down at 9.5 kV rms A2 minimal PD up to 8.4 kV rms A3 minimal PD up to 8.5 kV rms
B1-B3	100x100x25	B1 minimal PD up to 8.4 kV B2 minimal PD up to 8.5 kV B3 random burst of data at 8.7 kV rms
C1-C3	100x100x40	C1 interesting PD at 7.9 kV C2 similar PD at 7.9 kV behaviour changed at 8.6 kV C3 no meaningful PD up to 8.3 kV rms

The A1-A3 defects exhibited no sustained internal like PD activity under AC conditions. Any activity that was observed was well above the inception voltage predicted by Paschen's law (1.62 kV rms) and around the defined voltage limit.

The B1-B3 defects exhibited no repetitive internal PD activity during AC PD testing. The expectation was that PD would initiate above 1.15 kV rms but no repetitive and sustained PD was observed around this voltage level.

The C1-C3 defects were also tested under AC conditions, the first sample under test was sample C1. The PD behaviour observed in this sample was somewhat different with behaviour looking more like internal PD as illustrated in Figure 132.

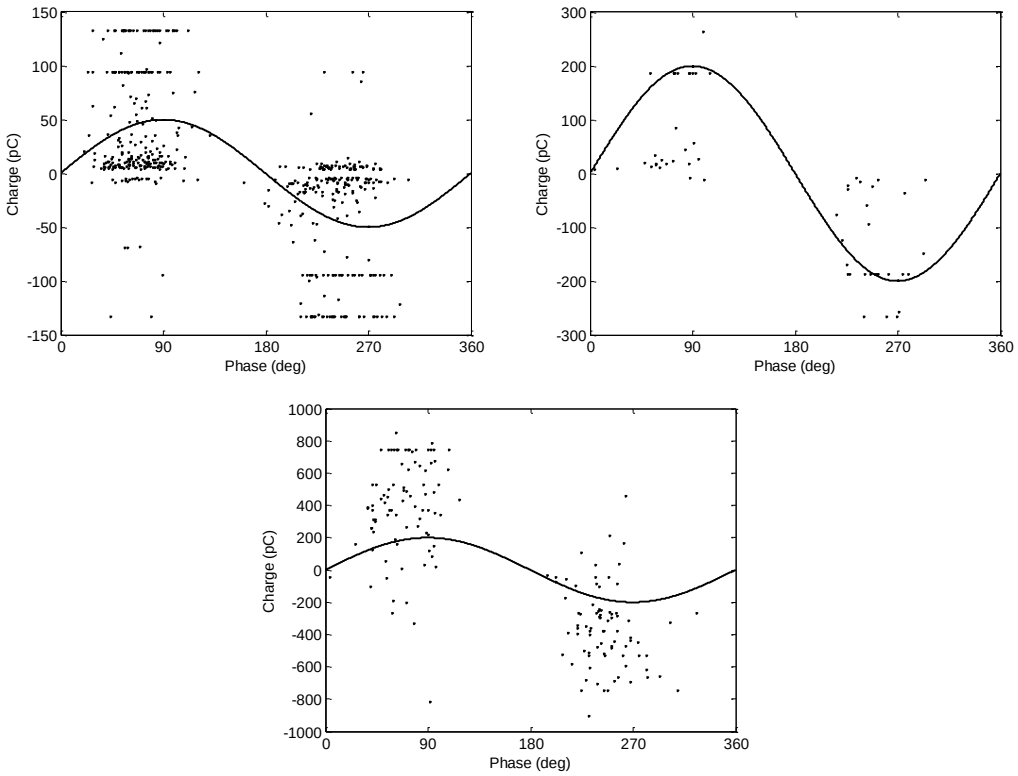


Figure 132 - Sample C1 AC PD measurements at 7.9 kV rms; 30 second segment one (upper left), 30 second segment two (upper right) and 30 second segment four (lower)

There was some spread of PD activity into the second and fourth quadrants, indicating material damage rather than internal PD activity. The second 40 µm high defect under AC test was sample C2, PD was first apparent at 7.9 kV rms over the first 100 second PD measurement (Figure 133) and extinguished over the following 100 second PD measurement.

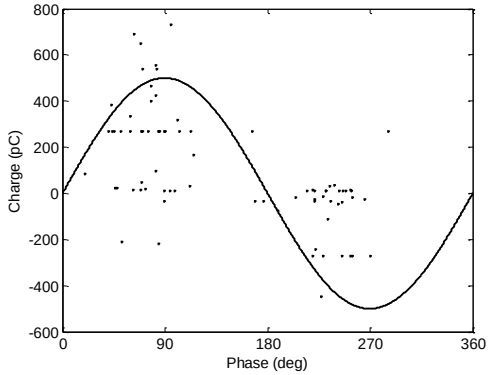


Figure 133 - Sample C2 two 100 second PD measurements at 7.9 kV rms

This type of behaviour is typical of internal voids where PD activity can extinguish. As the voltage is so high and PD is not restricted to the 1st and 3rd quadrants, it appears that the breakdown voltage could have been lowered. The voltage was increased to 8.6 kV rms where the PD activity in Figure 134 was recorded over 100 seconds.

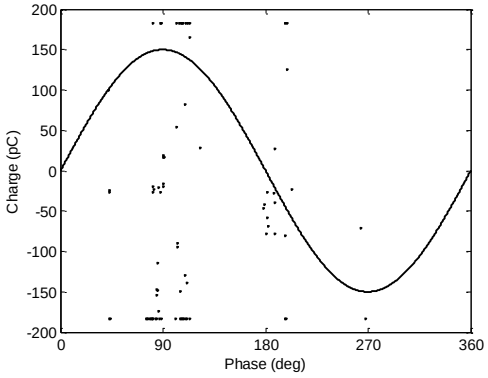


Figure 134 - Sample C2 100 seconds at 8.6 kV rms

This PD activity points further towards material damage with PD of varied polarity and with no real phase relation to the AC supply voltage. The final 40 µm high defect under test was sample C3 a fault occurred during the test (1 minute into a 5 minute measurement) with the Lemke system which resulted in a loss of the voltage measurement. The phase at which PD was occurring is not apparent in the data, the PD activity following the fault is detailed in Figure 135.

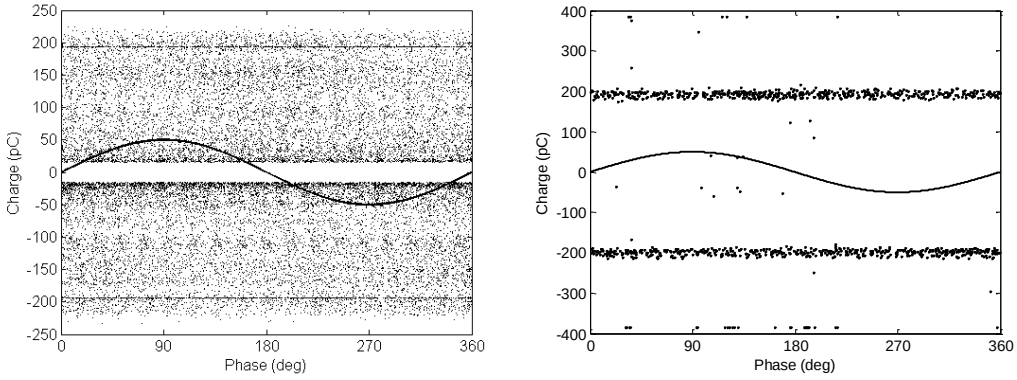


Figure 135 - Sample C3 two 100 second PD measurements at 8.3 kV rms

The results point to material damage as the voltage was close to the defined limit. PD was observed in the first and third quadrants for the first two 40 μm high defect samples but did spread into the neighbouring second and fourth quadrants. No significant PD occurred below 7.9 kV rms, this was significantly higher than the inception predicted by Paschen's law (1 kV). This could be explained by the induced defects not actually being large air filled voids but possibly a series of smaller voids. There is also the possibility that the intended defects are in actual fact simply regions of optically changed material.

8.5. SEM IMAGING

In order to investigate the type of defect introduced an SEM system was employed to image the induced defects through the cross section of the film sample. The SEM system employed was a Hitachi S-3000N, which was available within the electrical engineering department at the University of Strathclyde.

Sample C2 (100x100x40 μm defect) from batch two was cut in half through the induced defect using a scalpel. Optical images of the two halves following the cutting process are shown in Figure 136.

Figure 136 - Optical images of defect C2

The half samples were mounted using blu tac on the mounting plate of the SEM system for imaging. The cross section of each sample was scanned and the system was focused on the induced defects in each half of defect C2. The only obvious difference in the cross section for the two halves is illustrated in Figure 137.

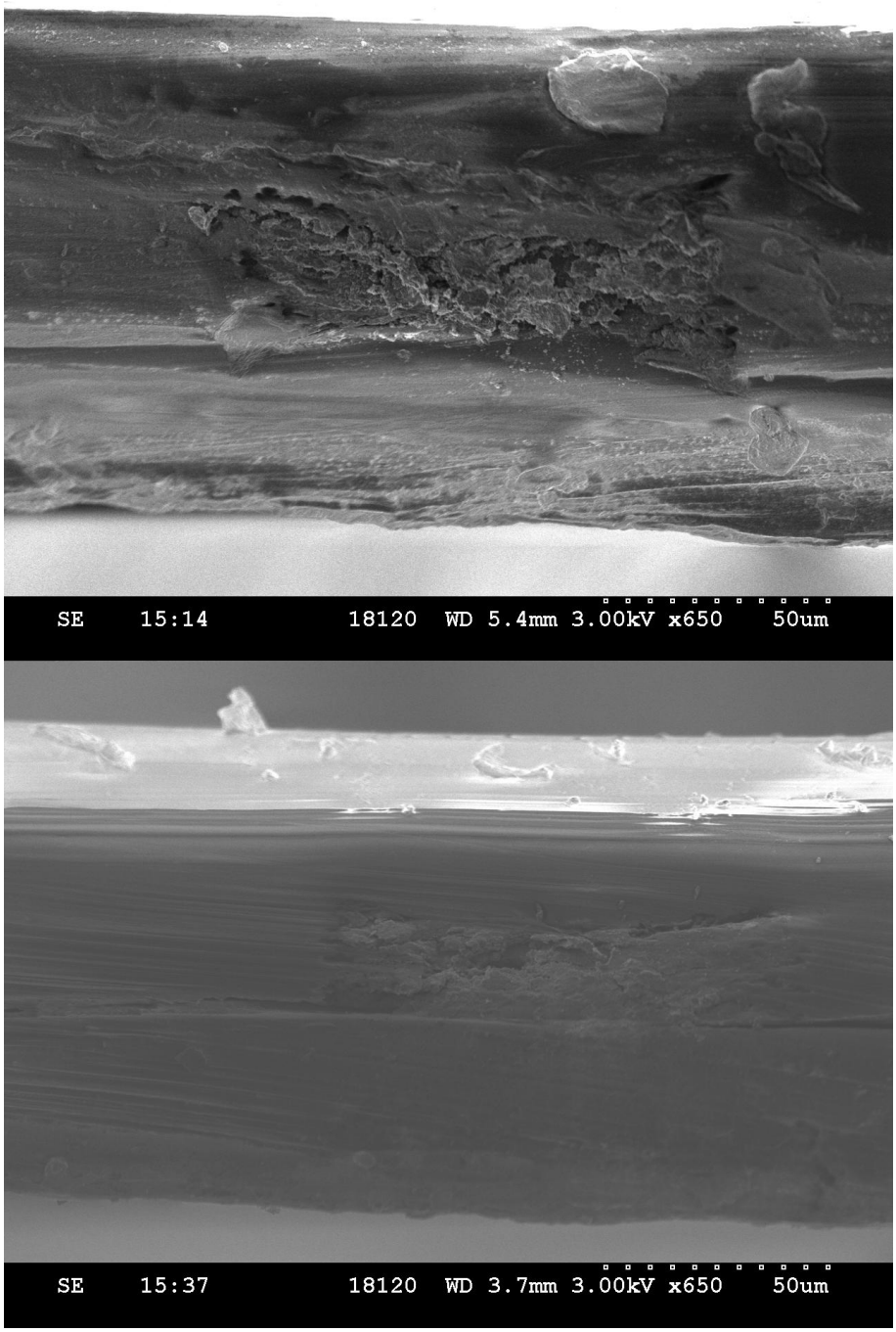


Figure 137 - SEM images of the two halves of sample C2

The magnification is the same for each image and the outline of a defect with the specified size is apparent in each half (approximately 100 µm wide and 40 µm high). More detail is evident in the upper image with material appearing to sag due to the heating from the SSLE process. A similar effect is apparent in the lower image but was less obvious. These images confirm that the laser system did not initiate a

single void of 100x100x40 µm it appears to be an area of damaged material with a series of smaller voids linked by deformed material. This is in contrast to the defect geometry expected using an optical microscope.

8.6. DISCUSSION

The literature review discussed studies on micro voids, the SSLE technique and applications of SSLE to date. The majority of applications have harnessed the optical change caused by the ablation process of the SSLE machine. The controllability of SSLE systems in creating intricate optical changes in optically clear materials was a particular advantage of the technique. No studies have considered using the voids that are produced during the ablation process. The ability to use a SSLE system to 'burn' a defect into an insulation sample was deemed research worthy due to the wide range of possible further applications of the technique, its accuracy and precision.

The access to an SSLE machine was the primary challenge in this work as it is a specialist piece of equipment. No equipment was available 'in house' and after consultation with Prof. Alan Kemp of Strathclyde he suggested the group of Prof. Martin Booth at Oxford as a strong application based research group. Contact with Prof. Booth led to discussions with Dr Patrick Salter who agreed to assist with the research. Two batches of samples were produced with a range of defects so AC PD testing could be conducted in the high voltage lab at Strathclyde. The SSLE system employed by Dr Salter was a bespoke device and is not available commercially. The requirement for access to specialist equipment would reduce the number of research institutions that could carry out this type of work, this could be why little work has been conducted in this area.

Different defects were produced by using a single 'burn' of 1x1x4 µm as the building block to make the larger defects. The inspection of samples using an optical microscope showed the defined defects with the required overall dimensions (in the x and y axis). The consideration of varying the building block size would be an interesting avenue to explore. A limitation will be the size of a single 'burn' beyond a particular point material fracture can occur.

Building on work carried out in chapter 5, care was taken to validate the voltage limits and to ensure no spurious PD was apparent from the test setup. The voltage limit was the point at which PD occurred consistent with material damage in the film

samples (125 µm = 8.7 kV rms, 190 µm = 11.3 kV rms). The defined voltage limits were below that of the Dupont data sheet due to the ramp method employed in the breakdown tests (125 µm = 13.5 kV pk, 190 µm = 17.5 kV pk). The variation was expected as the electrode configuration was different and the standard breakdown test had a voltage ramp rate of 500 V/s.

The majority of PD activity recorded in tests on samples with manufactured defects occurred close to the defined voltage limits. In many cases the PD activity recorded was over a wider phase range than would be expected for void type discharges. The expectation was that the reported PD was more consistent with material damage than internal discharge from induced defects. One area of consideration has to be the delay for a starting electron, with the voids being relatively small this delay time could be significant. In one test, setup error was evident for 125 µm sample A1 which broke down at the triple junction interface. On a number of occasions, after this test, air bubbles were observed in and around the electrode, oil and film interface (mainly around the ground electrode). Care was taken to manipulate the test cell to allow the air bubbles to roll off the surface of the film sample.

The defects introduced and tested are just a small sample of what can be achieved using this manufacturing technique. A distinct advantage is the control of defect size and relative speed of the process. Despite the lack of success in this first pass, undoubtedly this approach merits further study from the variation of laser settings, material type, material thickness and the intended defect geometry. The close combination of the laser etching process and the imaging of induced defects would be valuable in further studies of this technique.

SEM imaging confirmed that the SSLE process induced an area of damaged material with a series of small voids. There may be operational and material changes to enable the approach to be more successful. The use of imaging techniques that do not confuse the optical changes of the material with physical changes inside the material was particularly valuable.

8.7. CONCLUSIONS

Publications to date involving SSLE were reviewed with focus placed on the system operation and applications of the technique. The applications to date make use of the optical changes that can result from the laser ablation process, no work makes use of the defect introduced inside the material. Papers relating to the study of micro

voids were also reviewed. This work formed an initial study investigating the PD behaviour and analysing the defects introduced using SEM imaging. Further exploratory studies are required to determine relative merits of adopting this approach.

The main output from this chapter was a novel method for manufacturing internal void type defects inside film materials. No internal PD was observed in either of the two batches of samples. This preliminary study does not rule out the approach as many avenues have not been explored. The ability to introduce defects inside insulation samples after the manufacture of the insulation is an area worth further investigation. Current methods require that researchers induce defects in samples during the manufacture process (casting of epoxy resin) or layers of material to form defects. The opportunity to use insulation samples directly from the supplier and introduce defects inside the insulation sample is not possible using existing approaches. Many areas of criticism for existing approaches is related to the mix of the polymer/insulation sample and whether the dielectric material is representative of what is in the field.

SSLE machines are less accessible and harder to use than the commercially available 3D printer systems. In this research it was difficult to find an available SSLE system, the general availability of equipment and people was not explored. After some investigations, assistance was gratefully received from the department of engineering science at the University of Oxford. Without this assistance the method could not have been considered. Dr Patrick Salter at Oxford introduced defects with a defined geometry inside the PET film material using a bespoke system. This approach could not be implemented in a research group without access to such specialist equipment, this could be a barrier to further studies in this technique.

A repeated single ‘burn’ of 1x1x4 µm this was used as a building block for larger defects, no attempt was made to increase the size of this single burn. The defined defects were visible using an optical microscope. One interesting aspect was the ability to introduce arrays of small defects and this was trialled. The machining process itself was a very quick process for the operator once the settings of the SSLE system were dialled in. This approach could allow a large number of dielectric samples with defects to be produced very quickly, each defect was added in a number of minutes to the film samples. The size and complexity of the defect obviously affects the machining time.

The experimental setup was verified using defect free film samples to define the voltage limit and confirm no spurious PD activity. Above these voltage levels the non-defective film samples exhibited PD behaviour consistent with that of damaged insulation, PD generally occurred across the full AC sine wave. This approach of using non-defective samples to first prove the test circuit and test the limits of the materials worked well in providing a basis for further PD measurements using this PET film material. The full immersion of the test setup in mineral oil negated triple junction effects. The rigid brass electrical connection to the AC test and the use of the torque screwdriver to preload the samples with the same torque ensured repeatability and consistency for the test setup.

The inception voltage of PD activity for the samples with defects was significantly higher than predicted using Paschen's law. It was expected that the inception voltage would be higher than predicted due to the characteristic delay in availability of a starting electron for the ionisation process. No sustained PD activity was observed below 7.9 kV for all samples, this was relatively close to the point at which material damage was evident in the defect free film samples. Generally, the recorded PD activity was relatively large and occurred over a wide phase range, meaning material damage was most likely the cause of this PD activity.

The SEM imaging confirmed that the SSLE laser system introduced an area of damaged material with a random spacing of smaller voids. The use of SEM is recommended to image through the cross section of the induced defect. This enabled the separation of the optical and physical changes in the samples with defects.

In terms of future work there are many avenues that could be explored:

- Considering alternative materials that may behave differently to the ablation process of the SSLE machine.
- A range of defects were introduced but further investigations into the variation of the size of the single 'burn' which was the building block for all defects considered could be beneficial.
- The application of the technique to alternative sample types; thicker film sheets, transparent sheets of plastic or even cable insulation would be very interesting.

- The combination of exploratory SSLE studies for different materials/defect types and imaging the induced defects using non-destructive/destructive means will be critical in the development process/refinement of this technique. This would be in the form of a sensitivity study.
- There could be many applications where this technique would be useful to induce defects in the final insulation systems (transparency required). To allow this an understanding of the depth that defects can be added would need to be trialled.
- In the literature review for electrical testing, X-ray tests were conducted on micro voids to supply the starting electron for the ionisation process and reduce the time lag. A similar approach could be employed to rule out the delay for starting electron in future studies.

9. CONCLUSIONS AND FUTURE WORK

This final chapter summarises the conclusions and future work highlighted in the seven technical chapters presented in this thesis. The core areas of interest in this thesis were:

- The consideration of how an environment with significant electromagnetic fields affects magnetic field PD sensors.
- The behaviour of a void type dielectric sample was explored and specific focus was placed on the immediate test history of the sample and the effect this had on DC PD behaviour observed.
- Two methods were presented to enable void type dielectric samples to be produced and the resulting AC/DC PD behaviour was investigated. The most promising method was explored further through considering the behaviour of multiple voids and the accelerated aging of samples.

Within these key areas many avenues of further investigations exist, the conclusions from this phase of work will be discussed in the following section.

9.1. CONCLUSIONS

The conclusions from the seven technical chapters (chapters 2-8) are outlined individually.

9.1.1. CHAPTER 2

A novel method was presented to enable the response of a HFCT, a magnetic field sensor, in an electromagnetic field environment. A literature review was conducted to enable an understanding of the electric field magnitude that PD sensors could be exposed to in a HVDC converter station. The electric field emission inside converter halls of different topologies from literature was as follows: mercury valves (1.8 kV/m), thyristor valves (31.63 V/m) and a voltage source converter based multilevel converter (20 V/m). The knowledge of how a magnetic field sensor is affected by electromagnetic field emissions will be beneficial to system operators to prevent misdiagnosis of insulation faults on the system.

A GTEM cell is used to calibrate electric field sensors by applying a controlled electric field. In this work, the GTEM cell was employed to expose a range of HFCTs to a controlled electric field of 35 V/m at the test hatch. A range of HFCTs were tested at defined orientations to the resulting electromagnetic field inside the GTEM

cell. A difference in sensitivity to electromagnetic field was found between HFCTs with HDPE plastic casings and HFCTs with an aluminium casing. The ferrite core and windings of HFCTs experienced additional shielding from the electromagnetic field environment when the HFCT had an aluminium casing. The adoption of this method will enable the development of future sensors tailored to the final application environment.

9.1.2. CHAPTER 3

AC and DC PD test methods were presented and the behaviour of generic insulation samples was studied. Focus was placed on the differentiation of the PD activity under DC conditions.

Recommended methods from IEC60270 for DC PD analysis were applied to the three PD data sets, these methods were effective to enable differentiation. The DC PD data under analysis was that of the charge magnitude and time between PD events. The analysis of these quantities was considered using different lenses to allow the differentiation of the three sources. The time difference between PD events was found to be a more revealing measure than charge difference between PD events to differentiate PD sources.

The consideration of both charge difference between subsequent PD events and time difference between PD events was investigated in the form of a $|\Delta q|$-Δt-N plot. The PD sources were found to occupy different regions of the plot based on the characteristic behaviour of the three sources considered in this study. This method could provide a valuable assessment tool to differentiate PD sources in a HVDC system.

9.1.3. CHAPTER 4

The behaviour of a heavily aged void type dielectric sample under varied voltage conditions was investigated. The first objective was to understand how a void type sample would behave during tests similar to prequalification and type testing. A second objective was to evaluate how the immediate test history of the void type sample affected the DC PD behaviour of the sample.

The main effect evident was the variation of DC PD behaviour over the initial minutes following a voltage change whilst the insulation was capacitively graded. The PD activity reduced in frequency and magnitude when ramp tests of the same polarity or AC PD tests were conducted in quick succession. The variation in the

polarity of subsequent ramp tests acted to increase the frequency and magnitude of the PD in the capacitive region. The time constant to charge the largest void was calculated to be 47.71 seconds using the DC abc model. This was employed to differentiate the PD activity related to capacitively graded insulation (large PD activity with short times between events was apparent) from resistively graded insulation. A clear step change in PD activity was consistently apparent when the time between PD events exceeded 50 seconds throughout the different tests. The expectation was that the time between PD events would be longer than this threshold due to the delay in the availability of the starting electron. This approach can be employed to determine the time required for the capacitive PD behaviour to cease by calculating and applying the threshold value for the sample of interest.

A particular area of interest was the transition of the insulation sample from capacitively to resistively graded and changes in behaviour were reported. The immediate test history of the dielectric sample was found to affect the PD activity during DC ramp testing and care must be taken to ensure the immediate test history will not adversely affect the PD activity of interest. The sequence of PD tests on dielectric samples was shown to affect the void type DC PD behaviour observed and understanding the effects is critical to ensuring HVDC insulation systems are defect free.

9.1.4. CHAPTER 5

In chapter 5, the development of a novel manufacturing method for void type samples using 3D printing was presented. An analysis of available 3D printing methods was detailed and FDM was identified as the most appropriate method. Commercial FDM 3D printers available ‘in-house’ at the University of Strathclyde were considered. The process of modelling, manufacturing and preparing the samples for electrical testing was presented.

Three sample types studied in this work were: defect free, spherical and cylindrical voids. Two manufacturing methods were employed, the first was to print the sample in one piece and the second was to print the sample in two half discs. Following a surface preparation stage the half discs were joined using acetone and then vapour sealed using acetone.

The samples manufactured in one piece suffered from sagging in the ceiling of the void during the printing process, this was found to adversely affect PD activity. The

samples made in two halves had a similar PD inception voltage as the prediction from Paschen's law. The PD activity for the samples made in two halves was more consistent with the internal discharges reported for both spherical and cylindrical voids in insulation samples.

More consistent PD activity was observed from the cylindrical void sample under AC conditions than the spherical void samples. The ramp test method was used for testing under DC conditions, limited PD events were recorded on a number of virgin spherical and cylindrical void samples. The findings matched behaviour reported to date for studies on virgin dielectric samples with minimal PD activity recorded over many hours of DC PD testing.

9.1.5. CHAPTER 6

A method was presented for the manufacture of parallel and serial cylindrical voids based on the method presented in chapter 5. The objective of this work was to investigate the versatility of the 3D printing approach and to study PD behaviour under AC and DC conditions for serial and parallel void arrangements. The design, manufacture and final assembly of the dielectric samples was outlined.

The parallel void samples were made in two halves and additional locating lugs were added to ensure correct alignment of the defects. Serial voids were produced by stacking samples with single voids. The behaviour of a single void was compared to two, three, four and five parallel voids. The AC inception voltage was similar for the single void (7.3 kV rms) and two parallel voids (7.2 kV rms). The inception voltage was higher for the three (8.4 kV rms), four (9 kV rms) and five (8.5 kV rms) parallel voids.

In general, more PD events were recorded in the samples with three to five parallel voids but the PD magnitude at the inception voltage was lower. The inception voltage for two serial voids was found to be lower than that of a single void, this was not expected. Possible causes could be the separation of the voids through the dielectric sample or the misalignment of the two serial voids.

Under DC conditions as the number of parallel voids increased so did the number of PD events and PD magnitude. Less PD events were evident in the serial arrangement and the PD magnitude was smaller than that of the single void. The controllability of the approach enabled the manufacture of defined voids within ABS plastic samples.

9.1.6. CHAPTER 7

A method was presented to investigate the accelerated aging of void type dielectric samples produced using 3D printing. Available literature was consulted and the ability to thermally age 3D printed samples with single cylindrical voids was studied.

A range of aging cycles were conducted at average temperatures ranging from 80.4 to 136.7 °C for aging periods of 168 hours. Significant changes in geometry were evident at temperatures above 99.4 °C. The thickness of the samples was found to increase and the diameter reduced during the thermal aging process.

AC PD testing was conducted on samples aged below 99.4 °C, limited changes in geometry were evident and the inception voltage was lower than that of the virgin sample. Under both AC and DC conditions, more PD events were recorded and the PD magnitude was also larger from the aged samples suggesting the aging had an effect.

The main outcome from the thermal aging was to ensure the aging temperature was below an average temperature of 99.4 °C and to elongate the aging time rather than to push the temperature up on 3D printed samples. The main challenge for the thermal aging of 3D printed samples was due to the fact that ABS is a thermoplastic so softening occurred during temperature increases. Due to the printing process, the materials that can be considered using 3D printing will all experience softening at particular temperatures so samples made using this method may be better suited to electrical aging.

9.1.7. CHAPTER 8

A novel method was proposed to use a machining process called subsurface laser etching (SSLE) to introduce defined voids inside dielectric samples. The associated literature related to micro voids, the SSLE process and applications to date of the SSLE technique was presented.

The majority of applications employing SSLE have made use of the changes in optical properties of materials under study, limited work has considered the void which is produced during the ablation process of the laser. The SSLE machining process was outsourced to experienced colleagues in the department of Engineering Science at Oxford University.

Two batches of defects were manufactured inside PET film samples. This ranged from single 5 µm defects to the largest defect of 100x100x40 µm and arrays of

defects were considered. The defects were formed by using 1x1x4 µm burn as the building block for the larger defined defects. The limitation of the size of burn is determined by the fracture properties of the material under study.

Initially, samples with no defects were tested under AC conditions to determine the voltage limits at which material damage was apparent. AC PD testing was conducted on the two batches of samples but no internal PD was apparent only material damage was evident close to the defined voltages. SEM imaging was employed to determine the geometry of the induced defects through the sample cross section. This work was unsuccessful in generating internal PD but many avenues of investigation still exist for this method as this was the first exploration of this technique.

9.2. FUTURE WORK

Following on from the work carried out in this thesis, the following areas of future work are recommended. These key areas of future work are:

- The enhanced understanding of sensor behaviour in an electromagnetic field environment
- Understanding of void type behaviour under varied voltage conditions
- The further development of the two novel manufacturing approaches proposed in this thesis.

9.2.1. SENSOR BEHAVIOUR IN AN ELECTROMAGNETIC FIELD ENVIRONMENT

The method proposed in chapter 2 could allow the development of sensors specifically designed to be installed in an electromagnetic field environment. The effect of the electromagnetic field environment on the measurement system has not been considered in this work but would be an interesting avenue to explore in future studies. Alternatively, an enclosure or shielding system could be designed and tested using the proposed method. Developments to the GTEM itself would be limited based on the size of the cell but some adaptations could be possible to allow larger electromagnetic fields to be generated. Significant increases in the electromagnetic field at the test hatch may require an alternative test setup, in this case parallel plates may be more effective. Such an adaptation of the test setup may allow the study of more complex arrangements of installed HFCTs. Only a limited number of studies have investigated the electromagnetic field emission in modern converter halls. One paper [51] considered the behaviour of the multilevel

converter topology, future advancements in converter design are likely to lower the electromagnetic field emissions from the converter but these developments may bring alternative challenges.

9.2.2. VOID TYPE PD BEHAVIOUR UNDER VARIED VOLTAGE CONDITIONS

The work in this thesis considered one heavily aged dielectric sample and how the behaviour changed under varied voltage conditions. The study of a range of aged samples from virgin to heavily aged would be interesting to explore using the method presented in chapter 4. The variation of defect geometry could enable the derivation of certain key responses for particular defects under varied voltage conditions. This would allow the response following a voltage change to be attributed to a known defect type and help to diagnose certain fault conditions. The inclusion of voltage ripple effects would be interesting and is a research area receiving increased attention at present. The main difference would be the smaller voltage variations which occur over a significantly shorter timescale and the relative variation of voltage around the PD inception voltage. The expansion of the time periods of the voltage holds in the ramp test method would allow the timeline of PD activity under DC conditions following a voltage change to be investigated further. The opportunity to characterise the response of a HVDC system or components under voltage variations merits further investigation. This could aid understanding of health measurement schemes throughout different stages of the lifecycle.

9.2.3. DEVELOPMENT OF NOVEL MANUFACTURING TECHNIQUES

Two manufacturing techniques were presented in this thesis for the creation of void type defects in dielectric samples. The future work around each method will be discussed individually in the following sections.

9.2.3.1. 3D printing

The method employing a commercially available 3D printer, proposed in chapter 5, considered one filament material (ABS) but a wide range of filaments are commercially available. The change in filament material would pose challenges in producing the dielectric samples in two halves (if the acetone has no effect). There could also be opportunities with some materials available that cope better with overhangs, possibly allowing production of samples in one piece.

More advanced 3D printing systems are being developed that allow increased resolution in printed parts. These developments could also provide opportunities in

how samples are manufactured or assembled. Currently, the behaviour of spherical and cylindrical voids was presented but no alternative defects have been considered. The expansion of the type of defects that can be introduced inside dielectric samples could be critical in some application areas.

The combination of 3D scanning and 3D printing, where a characteristic defect could be scanned then reproduced using a 3D printer, would be a novel application directly relevant to industry where manufacturing issues can be tested in a controlled dielectric sample. The study of inclusions during the printing process would also be possible using the 3D printing method, this would require a pause in the printing process. The consideration of characteristic defects out with cable samples would be very interesting such as bushing insulators etc.

The behaviour of parallel and serial cylindrical voids was examined under AC and DC conditions. The variation of defect type, geometry, relative separation of parallel and serial voids would be interesting avenues to explore further using the 3D printing method.

The accelerated aging of 3D printed samples was possible using thermal aging. In addition, the expansion of aging time rather than the temperature would be recommended for future studies. It may be more appropriate to electrically age these samples due to ABS being a thermoplastic. With a reliable accelerated aging method in place an understanding of the development of DC PD activity at different aging periods could be understood. The aim would be to develop of a library of aged sampled allowing the age related characteristic responses during the ramp test method to be derived. The relation of PD behaviour in these samples during voltage changes to defect type/severity/age would be a powerful tool to HVDC system operators to understand the behaviour of the insulation system.

9.2.3.2. SSLE

The lack of success of the SSLE method presented should not rule out further investigations around this approach. The primary advantage of the technique was that defects could be induced inside samples after the manufacture of the insulation material. This approach removes the need for the researcher to manufacture polymer samples of industry standard. The relevancy of polymer samples in research studies to actual samples in industry is a common area of concern.

The controllability of the technique is a distinct advantage for particular shapes or arrays of defects. Only PET film samples were considered in this work and a small range of defects were studied. The variation of material type could identify materials that respond differently to the laser ablation process. Considering materials of different thicknesses from μm to tens of mm could yield additional areas for development of the technique. It may be that the use of thicker plastic sheets allow more powerful laser ‘burns’ to be used before material fracture occurs.

The type of defects that the system induces may be typical of particular defects found in certain applications. The application areas of the technique are wide ranging one could be to introduce defects inside cable insulation (the method requires a semi opaque insulation). The linking of 3D scanning techniques and the control of the SSLE system is also applicable for this technique, this would allow the reproduction of defined defects from the field inside dielectric samples.

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