Design and Analysis of a New Model Predictive Current Controller for Grid Connected Converters

PhD Thesis

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Abstract

In recent years, the threat of climate change has led to significant interest in the installation of small-scale, renewable electrical generators due to their ease of installation in remote areas and low capital cost. These distributed energy resources are highly variable in nature and are often connected to the utility grid, mandating the use of a grid-connected converter. The power injected into the power system should be of a high quality to meet local regulations, therefore, the design of these grid-connected systems has received considerable attention in literature.

In this thesis, state of the art control algorithms for grid-connected converters are reviewed and classified. Then, key limitations in the existing literature are identified and explained.

A new modulated model predictive current controller is proposed, which offers reduced computational burden compared with the prior art, allowing more time to perform additional control functions. The variable switching frequency of existing model predictive controllers is fixed and the power quality is improved. Simulation results are included to prove the equivalent performance of the new approach, whilst the practical implementation in hardware is studied to prove that the computational burden is reduced significantly.

The effects of parameter mismatch and grid voltage discretization on the controller are studied. The impact of these phenomena on the calculation of the duty factors is examined and a compensation strategy is derived. The limitations of compensating the effects precisely are discussed and a simplified solution is proposed. Simulation results verify the effectiveness of the proposed compensation.

The proposed controller is then extended to unbalanced systems. A Kalman filter estimator is used to extract the positive and negative sequence components and a new calculation time compensation technique is proposed, which offers superior accuracy to existing approaches. The system stability is verified theoretically. Simulation and experimental results are included to prove the superiority of the proposed technique. Despite the improved performance, the execution time is also reduced compared with existing techniques.

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Dedication

Thanks to my parents John and Allison, who have always encouraged me to do my best and grab any opportunities that come up. I would not have completed this PhD without your support. This work is dedicated to you.

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Acronyms

ABC artificial bee colony.

AC alternating current.

ADC analogue to digital converter.

ARX autoregressive with exogenous terms.

CB-MMPC carrier-based modulated model predictive power control.

CCS Code Composer Studio.

CPU central processing unit.

DAC digital to analogue converter.

DC direct current.

DER distributed energy resource.

DG distributed generation.

DNO distribution network operator.

DSO distribution system operator.

DSP digital signal processor.

ECKF extended complex Kalman filter.

EMI electromagnetic interference.

EMPC explicit model predictive control.

ESL equivalent series inductance.

FCS-MPC finite control set model predictive control.

FMCDM fuzzy multi-criteria decision making.

FOC field oriented control.

FVVV-MPC floating virtual voltage vector model predictive control.

GaN gallium nitride.

GPC generalised predictive control.

IC integrated circuit.

IDE integrated development environment.

IGBT insulated gate bipolar junction transistor.

IMPCC improved model predictive current control.

JTAG joint terminal access group.

LC-MPPC low-complexity model predictive power control.

MIMO multiple input, multiple output.

MLCC multilayer ceramic capacitor.

MMPC modulated model predictive control.

MPC model predictive control.

MPC-DSVM model predictive control discrete space vector modulator.

PCB printed circuit board.

PI proportional-integral.

PLL phase locked loop.

PR proportional-resonant.

PWM pulse width modulation.

RF radio frequency.

RMS root mean square.

Si silicon.

SiC silicon carbide.

SMPC sequential model predictive control.

SPEN SP Energy Networks.

SSE steady-state error.

SSEN Scottish and Southern Energy Networks.

THD total harmonic distortion.

TSO transmission system operator.

USB universal serial bus.

VCC vector current control.

VOC voltage oriented control.

VSC voltage source converter.

WBG wide band gap.

Chapter 1

Introduction

In recent years, patterns of extreme weather, flooding, wildfires and tropical storms have thrust climate change into the heart of the public conscience. Governments around the world have come under increasing pressure to meet the energy demands of modern society while curtailing harmful emissions of greenhouse gases and reducing our dependence on fossil fuels [1]. Since the turn of the century, many governments have incentivised greater uptake of renewable energy sources. However, these new technologies pose new technical challenges, from the individual generator hardware level, through to the national power system level.

Climate change due to greenhouse gas emissions is the single largest motivator for increasing uptake of renewable energy. The Intergovernmental Panel on Climate Change (IPCC) is an international body comprising 195 member states. Its role is to assess the published literature and provide a scientific basis for governments to develop their climate policies [2]. Its sixth annual assessment report, published in August 2021, found unequivocally that human activity has warmed the Earth's atmosphere, causing widespread and rapid changes to the biosphere [3]. Furthermore, the report finds that the observed increases in greenhouse gases (GHG) since 1750 have been unequivocally caused by human actions and that each of the last four decades has been successively warmer than any decade since 1850 [3]. Global surface temperature from 2001-2020 was 0.99°C higher than 1850-1900. The report finds it highly likely that GHG emissions were the main driver of tropospheric warming since 1979 [3]. The report concludes

that global surface temperatures will continue to rise until at least 2050 and warming of 1.5-2°C will be exceeded this century unless significant reductions in CO2 emissions are realised [3].

In the United Kingdom (UK), transport accounts for the largest share of greenhouse gas emissions [4]. Stated government policy is to ban the sale of new petrol and diesel cars from 2030, with all new cars to be fully zero-emission at the tailpipe from 2035. It is noted that there are already over 175,000 zero-emission vehicles in the UK and a further 198,000 plug-in hybrid vehicles. The UK government estimates that switching to electric vehicles could increase electricity demand by approximately 20% in 2050, relative to a system with no EVs [5]. Under the Committee on Climate Change's sixth carbon budget, the Balanced Pathway to Net Zero calls for variable renewables to account for 60% of generation by 2030, 70% by 2035, and 80% by 2050 [6]. This requires generation by offshore wind to increase from 265 TWh in 2035 to 430 TWh in 2050, while solar generation increases from 10 TWh in 2019 to 85 TWh in 2050. The government believes that an affordable system, consistent with the vision of achieving net zero is likely to be composed largely of wind and solar energy [7].

1.0.1 Renewable Distributed Energy Resources

Renewable energy sources may be located almost anywhere, with solar photovoltaic systems being suitable for installation on roofs of houses, whilst hydro power is best suited to areas with high rainfall and a natural valley to focus the flow [8]. For this reason, the term distributed energy resource (DER) has come to be used to describe these energy sources. Due to the remote nature and small scale of some installations, they are often connected to the low-voltage electrical distribution network, rather than the high-voltage transmission network that larger generators would typically connect to. Generators connected to the distribution network rather than the transmission network are often referred to as distributed generation (DG), and their capacity can range from a few kilowatts to hundreds of megawatts [9, 10].

1.0.2 Distributed Generation Challenges and Opportunities

In a conventional, fossil fuel-burning power station, the heat from combustion is used to turn water to high-pressure steam which drives a turbine and generator [11]. Similarly, in nuclear power stations, heat from nuclear fission is used to turn the water to steam and drive a turbine [12]. In both cases, the rate of heating and flow of steam can be accurately and predictably controlled to maintain a given turbine speed, allowing the generator to remain synchronised with the electrical grid.

Most renewable energy sources are based on extracting energy from some natural phenomenon like the sun, wind, rain, tide or waves. By their very nature, these sources are variable and often hard to predict. In the case of photovoltaic solar panels, energy is extracted from the sunlight, with the energy output changing depending on the time of day, cloud cover, orientation of the panel and so on. For wind power, energy is extracted from moving air by a turbine, with the energy output changing depending on the wind speed and direction.

A summary of the common types of DG and their integration challenges is provided in Table 1.1.

Table 1.1: Overview of distributed generation types.

Distributed Energy Resource	Description	Advantages	Disadvantages	Interfacing Challenge	Examples
Solar Photovoltaic (PV)	Solar radiation incident on panel produces voltage	Low capital cost No moving parts	Large surface area required Low output during winter	DC voltage level changes depending on incident radiation	[13, 14]
Solar Thermal	Solar radiation boils water producing steam to drive a turbine	High efficiency	Only suitable for equatorial areas with high irradiation	Suitable for direct grid connection like conventional generator	[15, 16]
Wind	Moving air drives a turbine which drives a generator	Large resource to be tapped, depending on location	Wind speed variable Unsightly turbines complained about	AC voltage magnitude and frequency vary with wind speed	[17, 18]
Hydro	Moving water drives a turbine which drives a generator	Small systems may be installed in existing waterways	Large flood planes often required	AC voltage magnitude and frequency vary with water speed and flow	[19, 20]
Tidal	Moving water drives a turbine which drives a generator	Highly predictable	Difficulty of installation and maintenance	AC voltage magnitude and frequency vary with water speed and flow	[21, 22]
Wave	Moving water moves a float which drives a generator	Waves rarely interrupted. Most countries have some coastline	High costs Difficulty of installation and maintenance	AC voltage magnitude and frequency vary with wave amplitude and wavelength	[23, 24]

It is clear from Table 1.1 that DERs are diverse, both in the nature of the energy source and in the way that they are interfaced with the utility grid. In fact, the use of distributed generators has already changed the way that generation is dispatched in the system. Distributed generators offer several advantages at the technical, economic, and societal levels, as well as a presenting several technical challenges. These issues are explored further in the following sections.

1.0.3 Societal Opportunities and Challenges

Distributed generation has become attractive to the public. Some DG units are rated at only a few kilowatts, making them compact enough for installation in private dwellings and small businesses [25]. Increased uptake of these small systems, coupled with government subsidy has driven down the cost of manufacture and installation. Furthermore, the ability to sell excess energy to the grid in exchange for a feed-in tariff has made installing small DG systems an attractive investment [26].

However, the increasing uptake of renewable energy, the associated government spending and energy policy in general continue to attract significant debate. Some argue that renewable uptake should be accelerated to reduce dependence on fossil fuels [27], whilst others are quick to warn against increasing our dependence on what they see as experimental energy sources [28].

1.0.4 Economic Opportunities and Challenges

Privatization of the electricity network has allowed new suppliers to enter the market, with small scale generation systems becoming an attractive investment even for individual homeowners. This has the potential to increase competition in the marketplace and reduce reliance on a small number of generation owners.

For many countries, fossil fuels must be imported, making one country dependent on another, and inevitably coupling the energy market with the politics of the day. The risks of relying on imports for energy needs have been laid bare following the recent conflict in Ukraine, with global oil prices soaring [29], and countries forced to do business with gas suppliers they have publicly derided [30]. Energy independence is

a key driver for the installation of a diverse range of distributed generators, since the system is less dependent on fuels from a small number of sources.

On the other hand, fossil fuel-based generators are generally seen as reliable and predictable, with well established market mechanisms and supply chains in place. Changing over to highly variable renewable energy sources to meet the demands of modern society poses questions around security of supply and reliability.

1.0.5 Technical Advantages

Electricity network reliability may be broadly defined as the system's ability to meet the energy needs of its customers at all times. In common with many other industries, reliability has generally been achieved through redundancy, with sufficient generation, transmission, and distribution capacity to meet demand even in the face of plant failures. The increased flexibility of DG coupled with its proximity to domestic customers has the potential to improve reliability without costly redundancy. On site power generation also has the potential to improve supply reliability for customers requiring uninterrupted service.

Distributed generation also has the potential to reduce transmission and distribution losses due to the positioning of generators closer to the point of use, potentially even on the roof of the very house that the power will be used in. Distributed generation also has the flexibility to address local power quality concerns, through localised voltage support and harmonic control. Similarly, the presence of some generation close to the point of use has the potential to reduce the burden on the distribution network, reducing component stress.

At the same time, diversifying the generation mix has the potential to improve overall system robustness. Since DGs can generate power locally and supply it to nearby loads, a situation can arise where a segment of the network becomes disconnected from the national system, yet customers continue to receive supply from nearby DGs [31]. A power island may be defined as a section of the power network comprising generators and loads which becomes electrically isolated from the wider system. At the time of writing, islanding is considered undesirable from both a safety and control perspective.

However, it is possible that in future, islanding will come to be viewed as an option to allow some customers to remain supplied whilst others experience outages [32].

1.0.6 Technical Challenges

In its simplest form, the electrical output of most DGs is either DC or a variable frequency and magnitude AC waveform, which is unsuitable for direct connection to the energy system. Therefore, power electronic interfaces are required. The pulse width modulated (PWM) inverter connected via a power filter has emerged as the best candidate for the hardware element of the interface. However, this introduces additional cost, power losses, interference issues and reliability concerns compared with directly connected synchronous machines.

a. Hardware Challenges

The design of the hardware itself has received considerable attention in literature, from the semiconductor level to the topology of the converter through to the digital control implementation. The design of switch-mode converters continues to progress at the hardware level, with academia and industry always seeking to switch faster [33], block higher voltages [34], improve electromagnetic compatibility [35] and survive in increasingly difficult environments [36] all while trying to reduce costs.

b. System-level Control Challenges

At the system level, large power systems were historically dominated by large synchronous generators and the systems were managed based on the well-known characteristics of such machines. With the increasing penetration of converter-interfaced generators, the influence of these large synchronous machines is being reduced. Every time a conventional gas or oil power plant is replaced by a wind or solar farm, the behaviour of the power system strays further from the well understood synchronous machine model [37]. Stability of converter-dominated power systems has been a critical research topic in recent years [38–42].

c. Protection Challenges

The conventional power system is designed to operate radially, meaning that power should be generated at a few large sites then distributed outwards towards the load. The addition of generators at the periphery of the network has made reverse power flow a concern, both in terms of unpredictable behaviour and the potential for segments of the network to remain live even when upstream generation has seemingly been disconnected. The protection of the power system becomes more difficult as a result. Academia and industry alike have identified concerns surrounding protection discrimination, coordination and speed of operation.

d. Power Quality Challenges

The need to meet local grid regulations means that the output of grid-connected generators needs to maintain a high power quality during normal operation [43]. If the control algorithm and interfacing filter of the grid-connected inverter are not designed carefully, both high- and low-order current harmonics may flow into the grid, reducing the power quality. However, the grid-interface converters can employ a wide range of control algorithms, therefore, they may be designed to offer various benefits to the system.

1.1 Future Power Systems

Traditionally, responsibility over dispatch of generation and configuration of the network has rested with the national transmission system operator (TSO). However, as power systems move away from large-scale centralised generators towards small-scale distributed generators, local distribution network operators (DNOs) will increasingly need to utilise and control distribution-connected service providers. This has led to the emergence of the distribution system operator (DSO) concept in recent years, where the DNO is empowered and indeed required to exercise greater control over the dispatch and coordination of their section of the system.

In their Distribution System Operator Strategy [44], SP Energy Networks (SPEN)

identify four key drivers for the DSO concept, namely:

- **Decarbonisation** - The drive to achieve Net Zero carbon emissions will lead to a greater proportion of transport and building heating being electrified and increased levels of distributed generation.
- **Decentralisation** - As large fossil-fuel-burning power stations go offline, and small-scale distributed generators come online, the percentage of generation connected at the distribution level will increase and greater control will need to be exercised at the local level.
- **Democratisation** - As consumers become more energy aware and adopt smart meters, intelligent electric vehicle chargers and home energy management systems, an opportunity will arise to source network services from individual consumers and small communities.
- **Digitalisation** - as IT, communication technologies and mathematical modelling tools improve, it becomes possible to forecast and control the system behaviour in a more optimal way.

Similarly, in their Delivering DSO progress update [45], Scottish and Southern Energy Networks (SSEN) identify the following building blocks to ensure a safe, reliable and secure grid:

1. Securely developing and operating an active distribution system comprising networks, demand, generation and other flexible DER
2. Taking into account two-way energy flows and greater supply intermittency
3. Coordinating information exchange between the DSO and TSO to balance the whole system
4. Procedures, using and coordinating flexibility services to balance the local grid

1.2 Research Motivation

There are common themes emerging in the approaches of SPEN and SSEN towards future power networks. From this, it is clear that future, grid-connected power electronic converters must be:

1. **Flexible** - they must be able to operate in different modes, prioritising active power or reactive power to meet the needs of the grid.

2. **Highly Controllable** - they must be able to be dispatched individually to export required amounts of power and must respond quickly to changes in their set-points.

3. **Distribution Network Compatible** - they must be able to be connected to the distribution network where the voltages may be unbalanced or distorted.

Existing controllers for grid-connected power converters can be classified into classical control based around linear feedback controllers, and modern controllers including predictive and adaptive techniques. Many predictive current controllers suffer from variable switching frequency, which leads to poor power quality and difficulty in designing the output filter. Furthermore, they can only create a small number of output voltages, leading to poor steady-state accuracy.

Previous attempts to correct these limitations have led to the emergence of modulated predictive control approaches, however, they suffer from high complexity and incur a high computational burden. Furthermore, they are not directly applicable to unbalanced systems. If the computational burden of these predictive current controllers is not reduced, the sampling period must be increased to allow more time. Alternatively, more capable and expensive microcontrollers must be used which increases the system cost and makes predictive control unattractive for widespread use.

To this end, this work explores the predictive control of grid-connected power converters, with a particular focus on reducing their computational burden, and improving their suitability for connection to unbalanced networks. The state of the art in model predictive current controllers is studied in depth and a new optimiser is proposed

which reduces the computational burden and makes predictive control more suitable for widespread use. Furthermore, the proposed controller is extended to unbalanced grids, making it suitable for use in distribution networks.

1.3 Thesis Contributions

This work makes two main contributions to the field of grid-connected power converters. These are listed as follows:

1. A new model predictive current controller is proposed with reduced computational burden, superior steady-state accuracy and optimised transient response.

2. A new model predictive current controller for unbalanced grids is proposed.

1.4 Summary of Published Work by the Author

The author has published the contributions of this thesis in a high-quality peer-reviewed journal and at a peer-reviewed academic conference as follows:

- E. T. Andrew, K. H. Ahmed and D. Holliday, "A New Model Predictive Current Controller for Grid Connected Converters in Unbalanced Grids," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2022.3158016.

- E. T. Andrew, K. Ahmed and D. Holliday, "A New Modulated Model Predictive Current Controller with Reduced Computational Burden," 2021 9th International Conference on Smart Grid (icSmartGrid), 2021, pp. 254-258, doi: 10.1109/icSmartGrid52357.2021.9551222.

1.5 Thesis Overview

Chapter 1 explains why climate change has made integration of renewable energy a key research topic in recent years and why the control of grid-connected power converters is crucial for future power networks. The chapter concludes by outlining the motivation behind this work together with the main contributions of the thesis.

Chapter 2 provides a comprehensive review of the state-of-the-art in control of grid-connected power converters. The general requirements for current control are outlined, then the main types of controller are briefly reviewed. The motivation for predictive control techniques is then explained and the state of the art in predictive control is studied in detail. The chapter concludes by identifying key shortcomings in the existing literature.

Chapter 3 describes a new implementation of model predictive current control which offers significantly reduced computational burden without sacrificing performance. Simulation results are included which prove that the proposed current controller achieves identical performance in steady-state and transient conditions to the established technique, while experimental results show that the proposed controller requires 46% less computation time.

Chapter 4 extends the work of Chapter 3 to unbalanced systems by adding a Kalman filter estimator to extract the positive and negative sequence components of the grid voltage. A new calculation time compensation technique is also proposed and the grid voltage discretization compensation strategy outlined in chapter 3 is extended to the unbalanced system. Finally, the system stability is verified theoretically. Simulation and laboratory results are included to prove the robustness of the proposed controller and support the theoretical analysis. The THD for the proposed controller is reduced and, despite the improved performance, the execution time is also reduced.

Chapter 5 describes the development of a hardware prototype and the supporting software used to validate the control algorithms proposed in this thesis. The hardware design is discussed first. The motivation for the build is outlined, then the specific design objectives are listed and the main design decisions and component selections are discussed. The software design is discussed second. The specific design objectives are listed and a few key implementation issues are discussed. Technical schematics for the final design are included in Appendix A.

Chapter 6 concludes the thesis and makes recommendations for future work.

Chapter 2

Review of Grid-Connected Current Control Strategies

The purpose of this chapter is to explain the importance of current control in grid-connected voltage source converters, before outlining the motivation for this research. First, the role of the current controller is outlined. Then, the main types of current controller are introduced and reviewed. Model predictive control (MPC) is then described and its suitability as a current control technique is discussed. The state of the art in MPC current control is analysed and key limitations in the existing literature are highlighted.

2.1 Role of the Current Controller

In recent years, three-phase two-level VSCs have been used extensively, from electric vehicle drives to grid-connected systems [46, 47]. Increasing use of renewable energy has also led to increasing use of grid-connected converters [48, 49]. Therefore, current control in three-phase DC/AC converters is one of the most widely studied subjects in modern power electronics [50].

Over the years, a broad range of control methods have been developed for grid-connected power converters. The literature is extensive and explores issues from high-level grid control and economic concerns [51] down to the fine details of the modulation

scheme used to synthesise the final output voltage of the converter [52]. From a control perspective, accuracy and ageing effects, tuning difficulty and lack of upgrade potential have rendered linear analogue controllers largely obsolete outside of a few niche applications. Discrete digital controllers are now the preferred platform for real time control of power electronic systems and drives. Modern microcontrollers offer a plethora of real time control peripherals, coupled with highly capable central processing units (CPUs), often augmented with hardware floating point support [53].

Consider the simple two-level grid connected VSC shown in Figure 2.1. The phase voltages and currents are measured and fed into the controller. The high-level controller receives some reference signal, often active and reactive power references, and produces a current reference signal. The current controller receives this reference and must decide how best to operate the switches to track the given reference, either by directly setting the state of each switch, or by sending a reference signal to an additional modulation stage. There are many possibilities for the algorithm employed within the current control block. In general, the current controller should satisfy the following criteria:

1. **Steady State Accuracy** - The actual current should track the reference signal with minimal steady-state error.

2. **Transient Response** - The actual current should return to the reference signal value as quickly as possible after a reference change without significant overshoots or oscillation.

3. **Waveform Quality** - The current waveform should be of a high-quality with low harmonic content to achieve a high power quality.

4. **Disturbance Rejection** - Changes in the grid voltage should be taken into account.

5. **Fault Handling** - The output current should be minimised during a fault or overload condition.

6. **DC Link Utilisation** - The converter should be able to export maximum possible power for a given DC link voltage to ensure best utilization of the components.

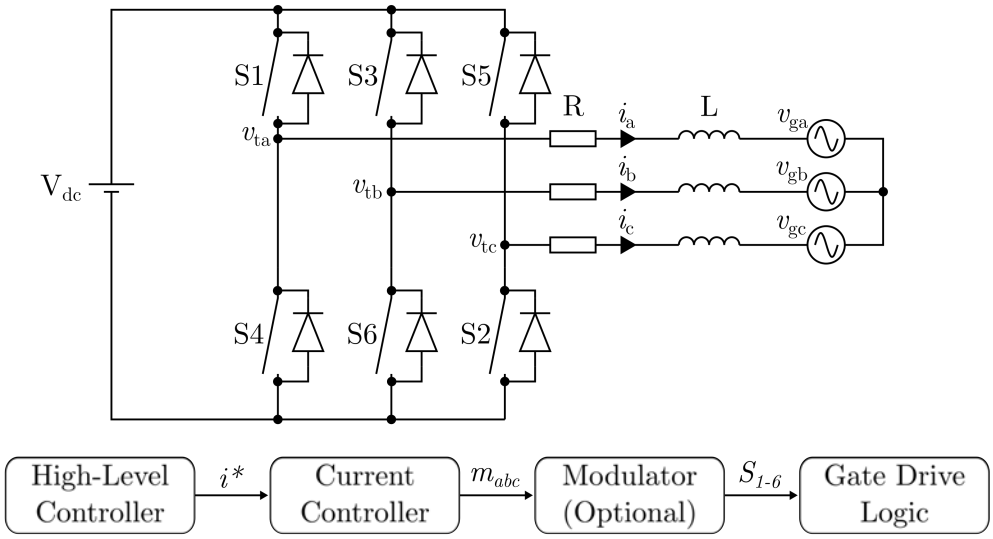


Figure 2.1: Two-level grid-connected voltage source converter with current control scheme.

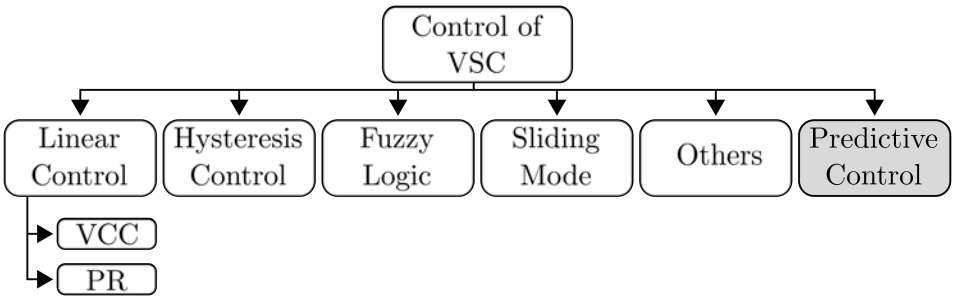


Figure 2.2: Broad classification of power converter control methods.

Furthermore, the presence of a controller in each grid connected converter means that the behaviour of entire groups of converters in a given part of the power network is linked. Therefore, the design and tuning of the current controller are critical for reliable operation of the network.

2.2 Classification of Control Techniques

Many control strategies have been proposed for power converters. In Figure 2.2, a broad classification is shown similar to that proposed in [54]. In the following subsections, each of the control families shown in Figure 2.2 is described and their advantages and

disadvantages are briefly discussed.

2.2.1 Linear Control

Linear control in relation to power electronics typically refers to classical feedback control systems designed in the frequency domain. Linear controllers include synchronous reference frame techniques based around proportional-integral (PI) controllers, stationary reference frame techniques based around resonant controllers, and rarer alternatives such as pole-placement techniques [55] and state feedback [56]. However, there are two main types of linear controller in common use for grid-connected converters: vector current control (VCC) and proportional resonant (PR) control. Both have been widely used to control grid-connected VSCs and are explored briefly in the following subsections.

a. Vector Current Control

The most common current controller used in DC/AC power converters is vector current control (VCC). In the VCC, the instantaneous phase angle of the grid voltage is used to transform the system to a synchronous reference frame comprising DC-equivalent quantities. This allows the currents to be regulated using simple proportional-integral (PI) controllers. Furthermore, with proper orientation of the synchronous reference frame, one DC quantity can be made to represent the active power while the other represents the reactive power, allowing decoupled control over these two variables, known as voltage oriented control (VOC). Similarly, in a machine drive application, proper orientation of the synchronous reference frame allows decoupled control over torque and flux, known as field oriented control (FOC).

One of the main advantages of VCC is that the DC-equivalent quantities can be regulated with theoretically zero steady-state error, meaning the VCC has excellent steady-state accuracy [57]. Furthermore, additional feed-forward and feedback paths may be added to the controller to improve disturbance rejection and start-up behaviour.

An inherent limitation of VCC techniques is that the entire system performance depends upon the estimated phase angle used to convert between the stationary and

synchronous reference frames. A phase-locked loop (PLL) is typically used to synchronise with the grid, and the behaviour of the complete system becomes linked to the behaviour of the PLL leading to design challenges [58, 59]. The design of the phase locked loop (PLL) is an active topic of research, and increasingly advanced techniques continue to emerge to prove the stability of the phase locked loop (PLL) in all conditions [60]. This is particularly relevant in weak grids, where it is known that synchronisation instability may arise [61].

Similarly, the PI controllers used to regulate the controlled variables must be tuned. It is common practice to adopt a nested structure, with an inner current loop and an outer voltage or power control loop. Typically, the inner current loop is tuned first to achieve a desired bandwidth, then the outer loop is tuned to achieve a particular phase margin, settling time, bandwidth or other figure of merit [62–65]. However, the controller gains must be tuned carefully to achieve good performance with acceptable stability margin.

As with most classical control techniques, the transient behaviour of VCC is relatively poor compared with more advanced techniques [66–68], since the VCC acts on the measurements at the present moment and does not consider the future behaviour of the system.

Furthermore, VCC techniques are designed based on a linear model of the system. Where the system is nonlinear, either the system is linearised around a single operating point and loss of performance either side of the operating point is accepted, or the system is linearised at multiple points and multiple gains are computed to be used depending on the operating point, known as gain scheduling. However, this complicates the control design considerably.

When applied to unbalanced grids, VCC approaches generally separate the control problem into positive and negative sequence reference frames [69], requiring double the control effort [70]. The PLL must also be designed to perform well during balanced and unbalanced conditions [71], with unbalanced PLL topologies often being highly complex and difficult to tune to achieve adequate stability margin [72].

b. Proportional Resonant Control

To avoid the need to synchronise with the grid, controllers have been proposed which operate directly on the sinusoidal control variables in a stationary reference frame. The ideal proportional-resonant (PR) controller is tuned to have infinite gain at the grid frequency, allowing it to drive the steady-state current error to zero at the grid frequency, while rejecting the influence of harmonics. PR controllers can also regulate unbalanced currents inherently, unlike dq-frame controllers which require modification [73].

However, PR controllers pose many design challenges of their own. In fact, the PR controller can be thought of as a VCC transformed to a stationary reference frame, and the mathematical equivalence between the synchronous, dq-frame controller and the stationary PR controller has attracted much analysis in the literature [74–77].

To achieve zero steady-state error, the PR controller should have infinite gain at the grid frequency, however, this cannot be achieved in a real digital system. Some work has been carried out to mitigate these differences between the ideal case and the discrete implementation [78–80]. Much like the VCC, extensive research has also been carried out into the parameter design of the controller and selection of the gains [81–83].

The design and tuning of PR controllers continues to attract research interest. In [84], new performance criteria and tuning rules are proposed and in [85], a tuning procedure is proposed to achieve a particular transient response.

2.2.2 Hysteresis Control

In hysteresis current control, the output current in each phase leg of the converter is compared with a reference and the output voltage is switched high or low to keep the current within a specific range, known as the hysteresis band. These controllers offer intuitive behaviour, simple implementation, excellent robustness and fast dynamics, limited only by the maximum switching speed of the switches and the time constant of the load [50].

However, in three phase systems, the three current controllers used for the phase legs can adversely interact with each other since, in the absence of a neutral connection,

the control problem has only two degrees of freedom while three controllers are actually employed. Through this coupling mechanism, the instantaneous current error can actually reach double the hysteresis band [86, 87]. Furthermore, since the output state of the converter is changed at the instant when the current error threshold is crossed, hysteresis current controllers typically suffer from variable switching frequency, leading to resonance problems and difficulties in calculating the switching losses [87].

Nevertheless, hysteresis current controllers continue to attract the interest of researchers and techniques have been proposed to vary the width of the hysteresis band to fix the switching frequency, such as in [88], where the derivative of the current error is used and in [89], where the average output voltage of the converter is used.

2.2.3 Fuzzy Logic

Fuzzy logic uses 'if-then' rules to decide control actions based on inputs. Provided there is adequate knowledge of the system and the rules are suitably designed, it can be applied to high-order and nonlinear systems which would be difficult to model mathematically and control by other means. Fuzzy logic control is robust and rejects disturbances effectively [90], however its accuracy depends on the number of inputs considered and the fuzzy rule table, therefore, there is a trade-off between execution time and accuracy. The fuzzification and defuzzification processes must also be considered, therefore, the controller tuning can become difficult and the hardware implementation can become very computationally complex [91].

In spite of this, fuzzy logic has been applied to a few power electronics applications. In [92], fuzzy logic is used to remove the switching table from a direct power controller, however, the fuzzy controller in the inner loop depends heavily on the outer loop which is still based on PI control [93], therefore, the fuzzy logic does not consider the whole system [94].

2.2.4 Sliding Mode

Sliding mode control is known for its robustness, good stability and good performance in a wide range of operating conditions. When applied to power electronics, it is not

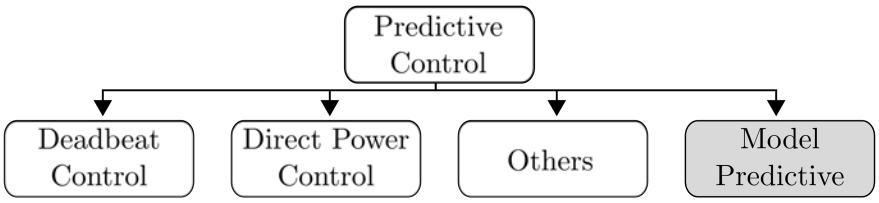


Figure 2.3: Broad classification of power converter control methods.

necessary to use an averaged model of the system [95–97]. Due to these advantages, sliding mode control has been used in several applications, from machine drives [98,99] to grid-connected systems [99,100].

However, sliding mode control suffers from chattering which leads to variable and relatively high switching frequencies, which causes high switching losses [101]. Attempts have been made to address this such as in [96], where an additional space vector modulator is added to guarantee fixed switching frequency [102].

2.2.5 Others

Aside from those summarised above, other controllers have been proposed for the control of power electronic converters, offering advantages in specialist applications, such as backstepping control [103], boundary control [104] and H∞ repetitive control [105]. However, these techniques have not attracted the same attention as those mentioned previously.

2.3 Predictive Control

Predictive control encompasses a broad range of controllers which employ a mathematical model of the system to predict its future outputs, thereby allowing some optimal control action to be selected in advance. Many predictive controllers directly select the switching action based on the required high-level control input, therefore, the cascaded structure common in linear control schemes is avoided. Nonlinear behaviour can also be modelled, removing the need to linearise the system. In the following subsections, each of the predictive controller types shown in Figure 2.3 is described and their advantages

and disadvantages are briefly discussed.

2.3.1 Deadbeat Control

In deadbeat control, the predictive model is rearranged to directly calculate the ideal output to achieve theoretically zero steady-state error at the end of the next sampling period. Deadbeat control calculates a reference voltage which, combined with a modulation stage, guarantees a fixed switching frequency [106–108]. The controller is conceptually simple and offers low computational burden.

The main drawback of deadbeat control is that the output is directly calculated using the system parameters, therefore, errors in the controller parameters reduce the robustness of the control. Variations of deadbeat control intended to improve its robustness can be very complex and difficult to implement [54]. Furthermore, since an ideal output voltage is calculated, the actual converter voltage limitations are not considered.

2.3.2 Direct Power Control

Direct power control (DPC) is derived from direct torque control (DTC) which has been applied to machines. At each sampling instant, it decides which of the available voltage vectors will drive the active and reactive power towards the reference value. It uses a switching table to select the appropriate output voltage based on the sign of the desired power change [109] and the grid voltage angular position [110] or virtual flux vector position [111].

The main drawbacks of table-based DPC are the requirement for a high sampling frequency to achieve acceptable performance and the resulting variable switching frequency [112,113], otherwise, table-based direct power control methods suffer from ripple in the power [114, 115].

In predictive direct power control, the switching actions are decided based on the minimisation of a cost function based on a predictive model [116]. In finite set predictive DPC, a single vector is selected based on the minimisation of a cost function [117–119]. To overcome these limitations, it has been proposed to include a zero vector in the switching period. This is known as duty cycle control or two-vector DPC [120–

124]. However, when only two vectors are applied during the switching period, a complete range of output voltages cannot be synthesised and the performance is not optimal. Therefore, it has been proposed to switch between two active vectors and the zero vectors during the switching period [125–127], however, the resulting duty factor calculations are complex. Alternatively, DPC schemes enhanced by a space vector modulation stage have been proposed (DPC-SVM) [128], however, the tuning effort is increased [113].

2.3.3 Model Predictive Control

Like many control strategies, model predictive control (MPC) has its origins in human behaviour. Humans are effective control systems as they are able to use anticipation or prediction to assess how their actions will affect the outcome. For example, when driving a car, humans know approximately how much the car will change course for a given rotation of the steering wheel. Classical control methods are generally unable to mimic this behaviour as they rely on past data to decide on control actions and have no knowledge of the system dynamics. When using a classical control scheme such as PI, the control action is calculated based on past errors and the error at the present instant. For this reason, it has been claimed that the PI-way of driving a car would be to block out the windscreen and drive by only looking in the mirrors.

The term MPC describes a range of control methods which make use of a system model in the decision making process. More formally, MPC uses a dynamic model of the process to predict the future evolution of the control variables over the sample time. These predictions are evaluated based on a cost function, then, the sequence that minimises the cost function is chosen. MPC deals with multiple input, multiple output (MIMO) systems, those with constraints or delays and even nonlinear systems inherently. It can also accommodate systems with challenging dynamics, which may be described by high-order models where classical control methods are difficult to apply.

A recent review found that the number of papers on MPC for power converters published annually has been doubling every three years since the year 2000 [129].

a. Application of MPC to the Two-Level VSC

Even a very simple power electronic converter, constitutes a multiple input, multiple output (MIMO) system. As well as being a MIMO system, there are hard constraints on the system, such as the limited DC link voltage and current handling capability of the switches. Moreover, there may be multiple control objectives, which must be considered, such as the current tracking error, active and reactive power error or the minimization of the ripple in one or more of those quantities. With this in mind, the optimization problem is clearly a very complex one to solve, especially since it must be solved by an embedded microcontroller in real time at sampling frequencies in the kilohertz range.

Early research efforts into MPC for power converters sought to reduce the complexity of the optimization problem. In the case of a converter with 6 switches, there are 64 possible states that the converter can be in at any given time. Of these, only 8 are possible without shorting the DC supply. If the system is treated as only having 8 candidate inputs, rather than a continuously variable input, then the optimization task can be easily reduced to one of predicting the plant behaviour for all 8 possible inputs and selecting the best one. Controllers exploiting this fact are generally known as finite control set model predictive control (FCS-MPC), due to the reduction in the available control set from a continuous range to 8 finite possibilities.

Advances in high-performance embedded microcontrollers have led to FCS-MPC gaining increased attention [130], including for grid connected applications [131–137].

Typically, the controlled variables of interest are predicted using a mathematical model of the system. This is generally the current but may also be the active and reactive power, or the speed or torque in a machine drive application. In fact, in [138] and [139], it has been proposed to consider the thermal stress on the switches when selecting the optimal voltage vector. These predictions are then compared with their desired reference values using a cost function to generate a list of costs if each possible output voltage vector were to be applied. A typical cost function to regulate current

is:

$$G_x = \left[i^*_{\alpha\beta(k+1)} - i^{v_x}_{\alpha\beta(k+1)} \right]^2, x \in [0, 7] \tag{2.1}$$

where, $i^{v_x}_{\alpha\beta(k+1)}$ is the current predicted one step in advance as though each of the eight voltage vectors were applied for one whole sampling period. Alternatively, the cost function may be designed to minimise the active and reactive power error as follows:

$$G_x = \left[P^*_{(k+1)} - P^{v_x}_{(k+1)} \right]^2 + \left[Q^*_{(k+1)} - Q^{v_x}_{(k+1)} \right]^2, x \in [0, 7] \tag{2.2}$$

where, $P^{v_x}_{(k+1)}$ is the active power and $Q^{v_x}_{(k+1)}$ is the reactive power predicted one step in advance as though each of the eight voltage vectors were applied for one whole sampling period. Additional control objectives may be combined within the cost function. For example, active and reactive power tracking may be prioritised, while current error is also considered, as follows:

$$G_x = \left[P^*_{(k+1)} - P^{v_x}_{(k+1)} \right]^2 + \left[Q^*_{(k+1)} - Q^{v_x}_{(k+1)} \right]^2 + \lambda \left[i^*_{\alpha\beta(k+1)} - i^{v_x}_{\alpha\beta(k+1)} \right]^2, x \in [0, 7] \tag{2.3}$$

where, λ is some weighting factor that adjusts whether the power error or current error has the largest effect on the cost. Alternatively, current error may be prioritised, with the additional objective of minimising the change in current during the sample period to reduce ripple as follows.

$$G_x = \left[i^*_{\alpha\beta(k+1)} - i^{v_x}_{\alpha\beta(k+1)} \right]^2 + \lambda \left[i_{\alpha\beta(k+1)} - i^{v_x}_{\alpha\beta(k)} \right]^2, x \in [0, 7] \tag{2.4}$$

where, λ is some weighting factor that adjusts whether the predicted current error, or the predicted current change has most influence on the cost. In [140], a multiobjective cost function was employed which considers the active and reactive power tracking, the balancing of the dc capacitor voltages and the minimisation of the switching frequency.

$$G_x = \left[i^*_{\alpha\beta(k+1)} - i^{v_x}_{\alpha\beta(k+1)} \right]^2 + \lambda_{dc} \left[\Delta V^{v_x}_{c(k+1)} \right] + \lambda_{sw} \left[N_c \right], x \in [0, 7] \tag{2.5}$$

where, λ_{dc} is the weighting factor for the dc voltage balance, λ_{sw} is the weighting factor for the switching frequency, $\Delta V_{c(k+1)}^{v_x}$ represents the difference in capacitor voltages if vector x is chosen and N_c represents the number of commutations.

For any of the cost functions described in (2.1), (2.2), (2.3) or (2.4), (2.5) the optimum output voltage vector may be selected simply by sorting the calculated costs, G, and selecting the smallest. Therefore, a seemingly complicated optimisation problem may be solved relatively easily using a brute force approach.

2.3.4 Others

As well as those mentioned previously, some other predictive controllers have been proposed, such as hysteresis-based predictive control [141].

In [142], a hysteresis predictive current controller was proposed which reduces commutations of the inverter switches, however, the solution is based on look-up tables which must be populated. Similarly, in [143], a predictive hysteresis current control for grid connected voltage source converters was presented. However, the proposed controller requires complex filtering and an estimation of the grid frequency.

2.4 Conventional FCS-MPC

Finite control set model predictive control (FCS-MPC) simplifies the current control problem by assuming that the converter only has 8 candidate output states, rather than a continuously variable output voltage. This simplifies the optimization task to one of predicting 8 possible currents and selecting the best one. The resulting controller has several attractive properties, such as the ease with which the optimisation can be performed online, the intuitive implementation of the controller and the ease with which additional objectives can be added to the controller.

In spite of its advantages, finite control set model predictive control (FCS-MPC) has several serious shortcomings. Existing attempts to address each of these shortcomings are reviewed in the following subsections.

2.4.1 Cost Function Design

Some FCS-MPC cost functions such as (2.3), (2.4) and (2.5) feature weighting factors which may be difficult to select analytically. Optimisation of the cost function weighting factors can be very challenging where the cost function includes multiple objectives. For this reason, many strategies have been proposed to optimise their value in advance or tune them online, combine them into fewer weighting factors or remove them entirely. As well as the calculation of the weighting factors, the design of the cost function itself is of interest. In [144], it has been demonstrated that the selection of the ℓ_2-norm (the sum of the squares of the error components) versus the ℓ_1-norm (the sum of the absolute values of the error components) produces a notable difference in the tracking error, proving that seemingly subtle differences in the cost function design can yield significant effects which are sometimes unexpected.

In [145], guidelines were proposed to aid in the selection of the weighting factors which stop short of actually calculating their values. In [146], an analytical technique was proposed to optimise the weighting factor values in advance, while in [147] and [148], algebraic methods were proposed to select their optimum values. Alternatively, algebraic techniques may be used to combine the control variables into a single hybrid variable as in [149], where torque and stator flux are combined into a single variable.

Various adaptive controllers have been proposed to tune the weighting factors online. In [150, 151], artificial neural networks were proposed to tune the cost function weighting factors. In [152], the authors proposed using a fuzzy multi-criteria decision making (FMCDM) algorithm to select the weighting factors. In [153] and [154], tuning procedures based on a genetic algorithms were proposed and in [155], an artificial bee colony (ABC) algorithm with multi-objective optimisation capability was used to supervise the cost function weighting factor selection. However, the use of advanced techniques to tune the weighting factors has been criticised as going against the conceptual simplicity of model predictive control [156]. Indeed, in [157], a separate optimisation process is performed simply to calculate the weighting factors to be used in the main optimisation process.

To avoid the need for weighting factors entirely, controllers with multiple sequential

or parallel cost functions have been proposed. A new strategy called sequential model predictive control (SMPC) was proposed in [158], where a single cost function was used for each control objective and was solved sequentially. In the included example for a machine drive application, one cost function was used to select two candidate vectors which minimise the torque error, then a second cost function selected the one which minimised the flux error. A similar but distinct solution was proposed in [159], where a parallel structure was employed to optimise the torque and flux separately, then an adaptive mechanism considered the vectors selected by each cost function and chose the one which was mutually beneficial. However, the sequential structure may introduce stability concerns [160]. In [161], a hybrid arrangement of sequential and parallel cost functions was proposed.

Similarly, in [162], it has been proposed to switch between different cost functions depending upon the conditions of the system. For example, to use one cost function optimised for transient conditions and another cost function optimised for steady-state accuracy. Similarly, it has been proposed to deal with some of control variables outside of the optimisation process, such as in [163], where it was proposed to include an event-trigger in the controller, where the current output is maintained until the error exceeds a given value, avoiding the need to include a switching penalty in the cost function. This idea was applied to a two-level three-phase VSC in [164,165], leading to a reduction in the switching losses.

2.4.2 Single Vector Limitation

At each sampling instant, the cost function is evaluated and the optimum vector is selected. Unless, by coincidence, one of the 8 possible currents produced is exactly equal to the current reference, then the FCS-MPC cannot track the current reference exactly. In other words, the FCS-MPC suffers from a finite steady-state error in steady-state and cannot achieve a deadbeat response. FCS-MPC cannot achieve zero steady-state error [166].

Worse still, the optimiser may select a new vector at every sampling instant or it may apply the same vector more than once. This leads to variable switching frequency.

In [167], a bandstop filter was included in the cost function, however, it reduces the dynamic performance of the algorithm.

To reduce the current ripple, it has also been proposed to increase the length of the prediction horizon [168–172]. Considering the system behaviour over a longer period of time can also address resonance issues [173, 174] and improve stability [175]. However, FCS-MPC uses and exhaustive search algorithm, therefore, the optimisation burden increases exponentially with increasing prediction horizon length [176] and special optimization algorithms are therefore needed [177].

2.4.3 Computational Burden

The computational burden of FCS-MPC has been criticized [178,179], since all available voltage vectors are evaluated when only one is actually required [180]. In [181], a deadbeat controller was used to identify the optimum sector, narrowing the candidate vectors from eight to three. In [180], the reference voltage vector required to achieve zero error was calculated first to allow the closest active vector to be identified without an exhaustive evaluation. In [182] and [183], a deadbeat control stage was used to narrow down the candidate vectors.

2.4.4 Vulnerability to Parameter Mismatch

The performance of any model predictive controller is dependent on the model used. If the model does not accurately reflect the behaviour of the system, then the predictions will be incorrect and the control decisions will not be optimal. The parameters of the model must therefore be as close as possible to the parameters of the system being controlled. FCS-MPC suffers from reduced performance when the model parameters are mismatched [184]. Parameter mismatch can occur in two main situations. Firstly, the parameters may change after the controller is designed, due to ambient conditions such as temperature or network switching. Secondly, the parameters may be unknown where it is required to insert an off-the-shelf converter to a given grid in a plug-and-play manner [185].

One strategy to address parameter mismatch is to estimate the parameters online

in real time to correct the model. Online parameter estimation has been proposed [186, 187] as well as observer-based disturbance correction [188–190]. However, such estimators are often relatively complicated and increase the system complexity [191]. Furthermore, the parameter estimators are often based on the system model, therefore, they may not address robustness issues where the model dynamics are incorrect.

Alternatively, model-free predictive control has been proposed [192–197] which removes the parameter-dependent predictive model entirely. An initial attempt at a model-free controller was presented in [192], where a lookup table is maintained describing how the converter is expected to behave for each available vector. However, if a given voltage vector is not applied for several sampling periods, the corresponding data in the lookup table is not updated, leading to increased current ripple [191] and possible instability [185]. Furthermore, the current must be sampled around the switching instant and if a delay is inserted to avoid picking up spikes, it must be tuned based on the behaviour of the individual converter [194]. In [194], an improvement was proposed where stagnant voltage vectors are applied every 50 sampling intervals whether optimal or not to ensure they are updated. However, this leads to a sub-optimal vector being applied [191]. In [198], this same idea was applied to a three-phase grid connected system. In [199], an improvement was proposed which can perform the current prediction for all voltage vectors using only the known responses for the last three vectors applied, however, there are 210 possible permutations, resulting in a high computational burden [185, 191]. In [200], the possible permutations were grouped according to whether active or zero vectors are applied and their relative positions as defined in [199].

To avoid the limitations of table-based model-free techniques, other methods have been proposed based on ultra-local models [201] and autoregressive with exogenous terms (ARX) models [202]. This method was first proposed in [203], and has since been applied to power electronics applications [204–206], however, the ultra-local model is relatively complicated and uses a variety of control parameters which must be found empirically which limits the ease of application [191]. The methods based on ultra-local models also need to be tuned to ensure satisfactory performances, while those based

on ARX models need an online adaptive algorithm to calculate the model coefficients.

2.5 Constant Switching Frequency Model Predictive Control

By far the most serious limitation with FCS-MPC is the fact that it can only apply one vector per sampling period, leading to inevitable steady-state error, high current ripple, poor power quality and variable switching frequency. To address these limitations, MPC approaches with fixed switching frequency have been proposed and are reviewed in the following subsections.

2.5.1 Low Complexity MPC

Techniques which use the negative complex conjugate of the apparent power to directly select the best active vector have been proposed, known as low-complexity model predictive power control (LC-MPPC) [119]. Initially, this was also a one-vector, variable switching frequency technique, however, in [124], the LC-MPPC was enhanced by including a zero vector during the switching period and in [122], this approach is further improved by allowing a second active vector to be applied instead of a zero vector to further reduce the error. These two-vector techniques fix the switching frequency, however, applying only two vectors means that a comprehensive range of output voltages cannot be synthesised, therefore zero steady-state error cannot be achieved. The LC-MPPC was applied to an unbalanced system in [207], however, only the single vector version is used. To reduce the complexity of the controller under unbalanced grid conditions, the extended instantaneous power theory was used in [208] and [209]. Whilst the proposed method does not require any power compensation or tuning, the computational burden is high [210].

2.5.2 Multiple Vector MPC

In [126], a multiple-vector technique was proposed where the phase angle of the optimal voltage vector is determined by minimising the cost function for two active vectors, then

the magnitude of the active vector is found by minimising a cost function including a zero vector. A good steady-state performance was achieved, at the expense of very high computation [127]. Alternatively, universal multiple-vector (UMV)-based MPC has been proposed, which achieves the same performance as two-vector techniques but with much less computation [211], however, the optimality of the selected duty factor is not guaranteed, therefore, zero steady-state error cannot be guaranteed [132]

a. Carrier Based Model Predictive Control

In [212] a carrier based technique was proposed, which is shown to have equivalent performance [213] to space vector modulation, whilst offering lower computational burden [214]. In [214], a new carrier-based modulated model predictive power control (CB-MMPC) strategy was proposed. Unlike other works on carrier based control based on PI-controllers [215–217], this controller is based on MPC. It differs from the prior work in [218, 219], since the error between the reference duty factor and the calculated duty factor for the next period is input to the cost function. The proposed technique is also more robust than model-based deadbeat controllers such as [220, 221]. However, the proposed technique is difficult to extend to converter topologies where the number of available voltage vectors is increased.

b. Continuous Control Set Predictive Control

Continuous control set MPC (CCS-MPC) offers a fixed switching frequency, simplifying the filter and thermal design [222], however, the optimisation process can be highly complex when constraints are considered [134]. Two of the most commonly used CCS-MPC approaches are generalized predictive control (GPC) and explicit MPC (EMPC). Both can be implemented with long prediction horizons, since the optimization complexity is almost independent of the horizon length and much of the calculation can be done offline in advance [134].

In [223], an explicit model predictive controller (EMPC) was proposed, where the control problem is formulated as a multi-parametric program which is solved offline for all possible states. The calculated solutions are then stored in a lookup table giving

an optimal solution as a function of the control state which can be looked up quickly online using a binary search tree technique [223,224]. This approach is most applicable where a large number of system constraints exist, mandating a complex optimisation process which is best performed offline [225]. EMPC is fully applicable to non-linear and constrained systems [223, 224] however, for unconstrained systems, simpler and more efficient solutions have been proposed such as generalised predictive control (GPC), which uses a transfer function model of the system and disturbances.

Generalised Predictive Control (GPC) was first proposed for real time control of power electronics in 2001, casting aside accusations that it is too computationally expensive for practical implementation in real time [226]. GPC is a subset of MPC applicable to linear and unconstrained systems, offering improved disturbance rejection and reduced steady-state error even with model parameter mismatch [227, 228]. GPC is suitable for long prediction horizons, therefore, it can effectively control systems with slower dynamics, such as the DC link voltage in inverter applications [227]. GPC offers an analytical solution to the optimization problem which can be computed in advance [172,228]. In [225], a complete design procedure for generalised predictive control of a grid connected converter was presented. Nevertheless, the theory and implementation of GPC remains complex, therefore, GPC is not very popular in practice [229]. A discrete-time system model is needed, which is often based on a zero-order hold, averaged model which neglects the switching behaviour of the converter. This is adequate for most purposes, however, it may sometimes be desirable to model the switching behaviour at a finer resolution where the filter resonance and switching frequencies are close [230].

c. Model Predictive Control with Space Vector Modulation

Another method to increase the range of output voltages compared to FCS-MPC is the use of virtual voltage vectors [182,231–233], which are then synthesised using a discrete space vector modulator. The resulting technique is known as model predictive control discrete space vector modulator (MPC-DSVM). This in effect transforms the two level VSC into a multilevel converter from a control point of view. As more virtual vectors

are created, the distance between them decreases, the output becomes smoother and the power quality improves. However, the need to evaluate virtual voltage vectors dramatically increases the computational burden [234]. For example, in [231], the system was augmented by up to 30 virtual voltage vectors on top of the 8 fundamental vectors, meaning that there will be 38 iterations of the current prediction and 38 evaluations of the cost function [182]. The natural next step is to try and narrow down the range of virtual voltage vectors to only a few candidates which need to be evaluated [232–236]. The methods proposed in [136, 236] are sensitive to changes in inductance as well as lacking a clear way to choose how many vectors should be analysed.

A key limitation of the MPC-DSVM approach is that the resolution of the possible output voltages is dependent on how many virtual vectors have been defined. More virtual vectors leads to a smoother range of outputs, but with more computation. This limitation has recently been addressed in [234], where a deadbeat controller first calculates the approximate output voltage, then, floating virtual voltage vectors are defined around the locus of this reference vector and are evaluated based on a cost function. This technique is referred to as floating virtual voltage vector model predictive control (FVVV-MPC). However, the range of output voltages is still not continuous, and a decision has to be made regarding how many FVVVs should be defined and what their distance from the reference should be.

In [237], virtual vectors were filtered and a modulator was employed, however, this slows down the transient response [234].

2.5.3 Model Predictive Pulse Pattern Control

To improve the current quality of voltage source converters, it has been proposed to calculate optimised pulse patters offline in advance, then apply them in real time to the switches to achieve very low current distortions. However, such systems typically require a very low control bandwidth and have poor transient performance.

In [238], it has been proposed to apply optimised pulse patterns as part of a receding horizon control strategy. The resulting controller is referred to as model predictive pulse pattern control (MP^3C). However, this technique has been criticised as the switching

model is simplified and solving the optimisation in real time is highly challenging, requiring trade-offs to be made to achieve a solution with realistic resources [239].

2.6 Modulated Model Predictive Control

First shown for a cascaded H-bridge back-to-back converter in [240], modulated MPC (MMPC or M^{2}PC) integrates a modulation stage with an FCS-MPC, ensuring a fixed frequency [134]. It can involve multiple control objectives such as minimizing the tracking error, reducing switching losses or avoiding certain switching states [241] and has gained significant traction in the literature [132, 218, 219, 240, 242–245]. An MPC with optimised overmodulation has been proposed in [245], however, the calculations involved have been criticized [132].

In [244], the current error produced by each voltage vector is calculated, then the two vectors producing the lowest error are identified. Their duty factors are then calculated by solving a system of linear equations. However, the resulting algorithm is essentially a deadbeat controller, therefore, it is vulnerable to modelling errors such as parameter mismatches and un-modelled delays [246].

There are two methods to compute the duty factors in MMPC: to assume that the duty factor for each vector should be inversely related to the cost function for that vector, or to use a deadbeat control to calculate them directly, which may lead to an infeasible solution.

In [244] the current error was used to calculate the application times of the active and zero vectors with zero tracking error.

In [245], the behaviour of beyond the linear modulation region was examined, and an algorithm was proposed to extend MMPC into the over-modulation region in an optimal way. The resulting technique achieves a deadbeat response in the linear region and tends towards the FCS-MPC case in the over-modulation region, which is known to be optimal. This approach is refined in [178], where Pythagoras theorem was used to remove trigonometric functions from the controller to improve the performance on DSPs. However, the computational burden remains high [132].

In [132], a modified model predictive controller (M^3PC) was proposed with improved steady-state and transient performance.

2.7 Summary

As described in Chapter 1, future grid-connected converters need to be flexible, highly controllable and compatible with distribution networks. Therefore, the design of the current controller is a key concern for the development of future power networks.

In this chapter, the state of the art in the control of grid-connected converters has been presented and reviewed. Predictive control methods have emerged as a promising alternative to classical linear techniques, due to their improved transient response. More recently, model predictive control has been proposed for grid-connected systems, due to its fast transient response and ability to consider multiple control objectives. A summary of the various techniques is included in Table 2.1.

Table 2.1: Overview of predictive control techniques.

Technique	Description	Advantages	Disadvantages	Examples
Conventional FCS-MPC	One vector selected through brute force optimisation	Fast transient response No modulator needed Conceptually simple	Variable switching frequency Non-zero steady-state error	[168, 169]
Low complexity MPC	Vector selected using power error	Low complexity	Basic scheme suffers from variable switching frequency	[119, 124]
Carrier based MPC	Existing FCS-MPC combined with sine-triangle modulator	Reduced computation vs MPC-DSVM Robust vs deadbeat control	Difficult to extend to topologies with more available vectors	[212, 214]
Explicit MPC	Optimisation problem solved offline and solutions stored	Complex, multi-objective constrained optimisations possible	Need to solve offline Complicated implementation	[223, 224]
Generalised MPC	Subset of MPC applicable to linear and unconstrained systems	Long horizon possible Robust against parameter mismatch	Theory and implementation complex	[226, 228]
MPC with SVM	FCS-MPC with additional virtual vectors and modulator added.	Fixed switching frequency Improved power quality	Computational burden rises with vector count Discontinuous range of output voltages	[231, 232]
Model predictive pulse pattern control	Optimised switching patterns calculated in advance	Very low current distortions	Low control bandwidth Need to calculate patterns offline	[238, 239]
Modulated MPC	Vectors selected then duty factors set according to vector costs	Fixed switching frequency Improved power quality	Computational burden high	[134, 240]

Model predictive control has been widely used in grid-connected systems in recent years, however, the following key limitations were identified with the existing literature:

1. Existing FCS-MPC approaches have a variable switching frequency, which leads to poor power quality and difficulty in designing the output filter.

2. Existing FCS-MPC approaches can only create a small number of possible output voltages, leading to poor steady-state accuracy.

3. Existing MMPC approaches offer fixed switching frequency, however, they suffer from high complexity and incur a high computational burden.

Chapter 3

New Modulated Model Predictive Control with Reduced Computational Burden

In this chapter, a new predictive current controller is proposed which achieves performance equivalent to the conventional modulated model predictive current control whilst incurring a reduced computational burden. The proposed controller is then extended beyond the linear modulation region and an improvement to the conventional over modulation algorithm is proposed. Furthermore, the influence of parameter mismatch on the controller is examined, and the effects of grid voltage discretization are compensated.

The remainder of this chapter is organized as follows. Section 3.1 derives a discrete mathematical model of a voltage source converter (VSC). Section 3.2 describes how the active vectors are selected in a conventional modulated model predictive control (MMPC) scheme and proposes an alternative method. Section 3.2.2 describes how the proposed algorithm can be extended to the over modulation region. Section 3.3 describes how the reference currents are generated and how calculation delay is compensated. Section 3.5 examines how parameter mismatch affects the proposed control and proposes a grid voltage compensation strategy. Section 3.6 studies the proposed

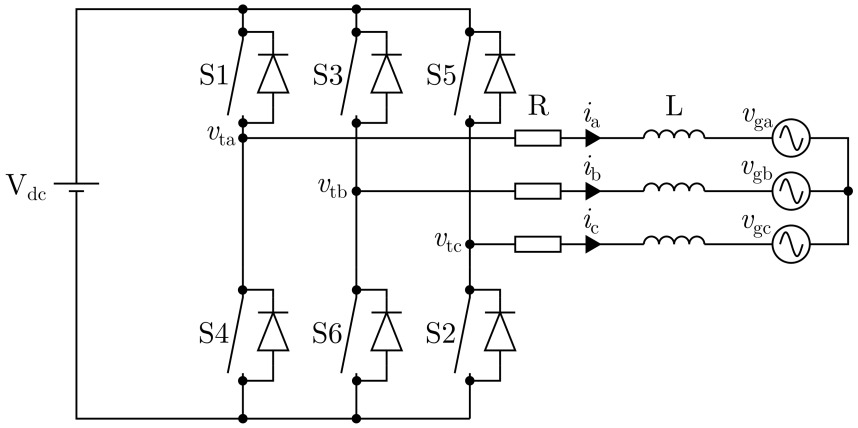


Figure 3.1: Two-level grid-connected VSC with inductive filter.

technique in simulation. Section 3.7 includes the results of the practical experiments which support the simulation results.

3.1 Dynamic System Model

A circuit diagram of a grid-connected VSC is shown in Figure 3.1. By applying Kirchhoff's voltage law, the converter terminal voltage can be described in terms of the grid current by the following system of differential equations in the stationary reference frame:

$$\begin{bmatrix} v_{t\alpha} \\ v_{t\beta} \end{bmatrix} = \begin{bmatrix} v_{g\alpha} \\ v_{g\beta} \end{bmatrix} + R \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.1}$$

where, $v_{g\alpha}$ and $v_{g\beta}$ are the stationary components of the grid voltage, i_α and i_β are the stationary components of the grid current and L and R are the inductance and resistance of the interfacing filter respectively. To allow for the development of a digital control algorithm, the continuous model of (3.1) must be converted to discrete time. The system can be approximately discretized using the forward Euler approximation

for the current derivative:

$$\frac{di_\alpha}{dt} \approx \frac{i_{\alpha(k+1)} - i_{\alpha(k)}}{T_s} \tag{3.2}$$

where, $i_{\alpha(k+1)}$ is the grid current sampled at instant k+1, $i_{\alpha(k)}$ is the grid current sampled at instant k and T_s is the sampling time. An identical method is used for the β-component. By substituting (3.2) into (3.1) and rearranging for $i_{\alpha\beta(k+1)}$, a discrete predictive model is obtained describing the future grid current as a function of the proposed terminal voltage and the system parameters as follows:

$$\begin{bmatrix} i_{\alpha(k+1)} \\ i_{\beta(k+1)} \end{bmatrix} = \left(1 - R\frac{T_s}{L}\right) \begin{bmatrix} i_{\alpha(k)} \\ i_{\beta(k)} \end{bmatrix} + \frac{T_s}{L} \left(\begin{bmatrix} v_{t\alpha(k)} \\ v_{t\beta(k)} \end{bmatrix} - \begin{bmatrix} v_{g\alpha(k)} \\ v_{g\beta(k)} \end{bmatrix} \right) \tag{3.3}$$

In the predictive model (3.3), the current $i_{\alpha\beta(k)}$ and grid voltage $v_{g\alpha\beta(k)}$ at instant k, together with the resistance R and inductance L are dictated by the system, therefore, the controller only has the freedom to select a value of $v_{t\alpha\beta(k)}$.

3.2 Selection of Active Vectors

The objective of the model predictive current controller is to find the optimum terminal voltage $v_{t\alpha\beta(k)}$ to minimize the current tracking error. In the conventional finite control set model predictive control (FCS-MPC), the controller selects only one output votlage vector and applies it for the whole switching period. However, in the modulated model predictive control (MMPC), the controller selects two active vectors which are applied along with the zero vectors, effectively implementing a space vector modulation strategy.

The first stage in the MMPC algorithm is, therefore, to select an optimum voltage vector v_{opt} and second-best vector v'_{opt}, which will form the active vectors for the space vector modulation. The calculation of their respective duty factors is handled separately. In the conventional MMPC, the same optimisation approach is adopted as in FCS-MPC, where a cost function is evaluated exhaustively for all available output voltage vectors and compared with the reference. Typically, a quadratic cost function

is used to ensure good regulation of both the alpha and beta components as follows:

$$G_x = \left[i^*_{\alpha\beta(k+2)} - i^{v_x}_{\alpha\beta(k+2)} \right]^2, x \in [0, 7] \tag{3.4}$$

where, $i^{v_x}_{\alpha\beta(k+2)}$ is the current predicted two steps in advance as though each of the eight voltage vectors were applied for one whole sampling period. The best and second-best vectors are selected by sorting the calculated costs G_x by magnitude and selecting the lowest and second-lowest costs respectively. This is computationally expensive since the variables in (3.3) and (3.4) are complex valued and the expression must be evaluated repeatedly even though only three of the predicted currents are ultimately useful. Figure 3.2 shows a detailed view of the available output voltage vectors for the VSC and the currents which would result from applying each of them for one whole sampling period as calculated by (3.3). An arbitrary current reference vector is also shown. Clearly, the optimum vector v_{opt} and second-best vector v'_{opt} will be those which are closest to the reference when mapped to the current domain by (3.3). In the example shown, i^2 is optimal and i^1 is second-best, therefore, the controller should modulate between v^2 and v^1 and the zero vectors. In this work, it is proposed to reduce the computation required to implement this process. In Figure 3.2, an arbitrary current reference vector is included. In fact, if the direction of the reference vector with respect to the stationary reference frame is known, the optimum vectors can be identified without having to repeatedly evaluate the cost function. Firstly, since the predicted current hexagon is not centered at zero, a complex direction vector, $i^{dir}_{\alpha\beta}$ is obtained by subtracting the current generated by applying the null vector $i^{v_0}_{\alpha\beta}$ from the current reference vector $i^*_{\alpha\beta}$.

As shown in Figure 3.3, the quadrant to which this direction vector points can then be efficiently obtained using compare-to-zero checks. For example, if $Re\left(i^{dir}_{\alpha\beta}\right) > 0$ and $Im\left(i^{dir}_{\alpha\beta}\right) > 0$, then the direction vector points to the first quadrant. From there, this quadrant is split into three subsectors. In subsector 'A', v^2 is optimal and v^3 is second best, in subsector 'B' v^2 is optimal and v^1 is second best and in subsector 'C' v^1 is optimal and v^2 is second best. The subsector required can be easily identified by

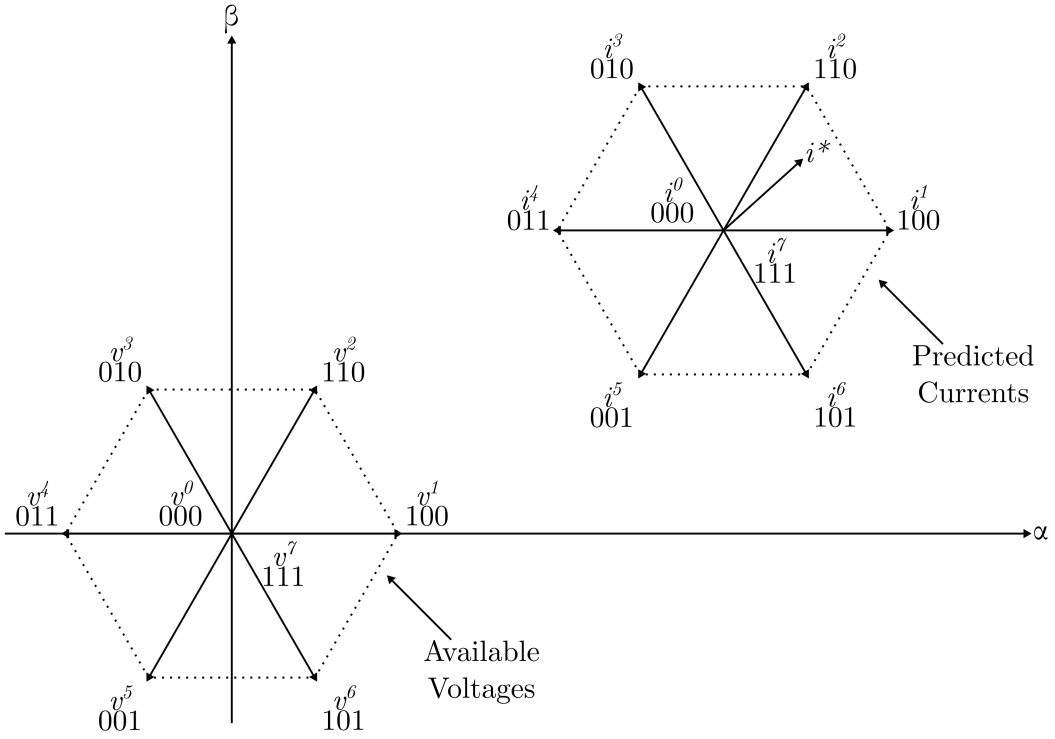


Figure 3.2: Available voltage vectors and their resulting predicted currents.

exploiting the exact values of the tangent function. For example, if

$$\frac{Im\left(i_{\alpha\beta}^{dir}\right)}{Re\left(i_{\alpha\beta}^{dir}\right)} > \sqrt{3} \tag{3.5}$$

then the direction vector lies in subsector 'A' and v^2 and v^3 should be selected as the optimum and second-best vectors respectively. Using a similar procedure, the active vectors can be identified rapidly using simple compare-to-zero and compare-to-constant operations for all quadrants and subsectors and the selected vectors are the same as if the vectors had been exhaustively evaluated.

3.2.1 Calculation of Duty Factors

Once v_{opt} and v'_{opt} are selected, their relative duty factors must be calculated. Within the linear modulation region, the current error should be reduced to zero by the end of

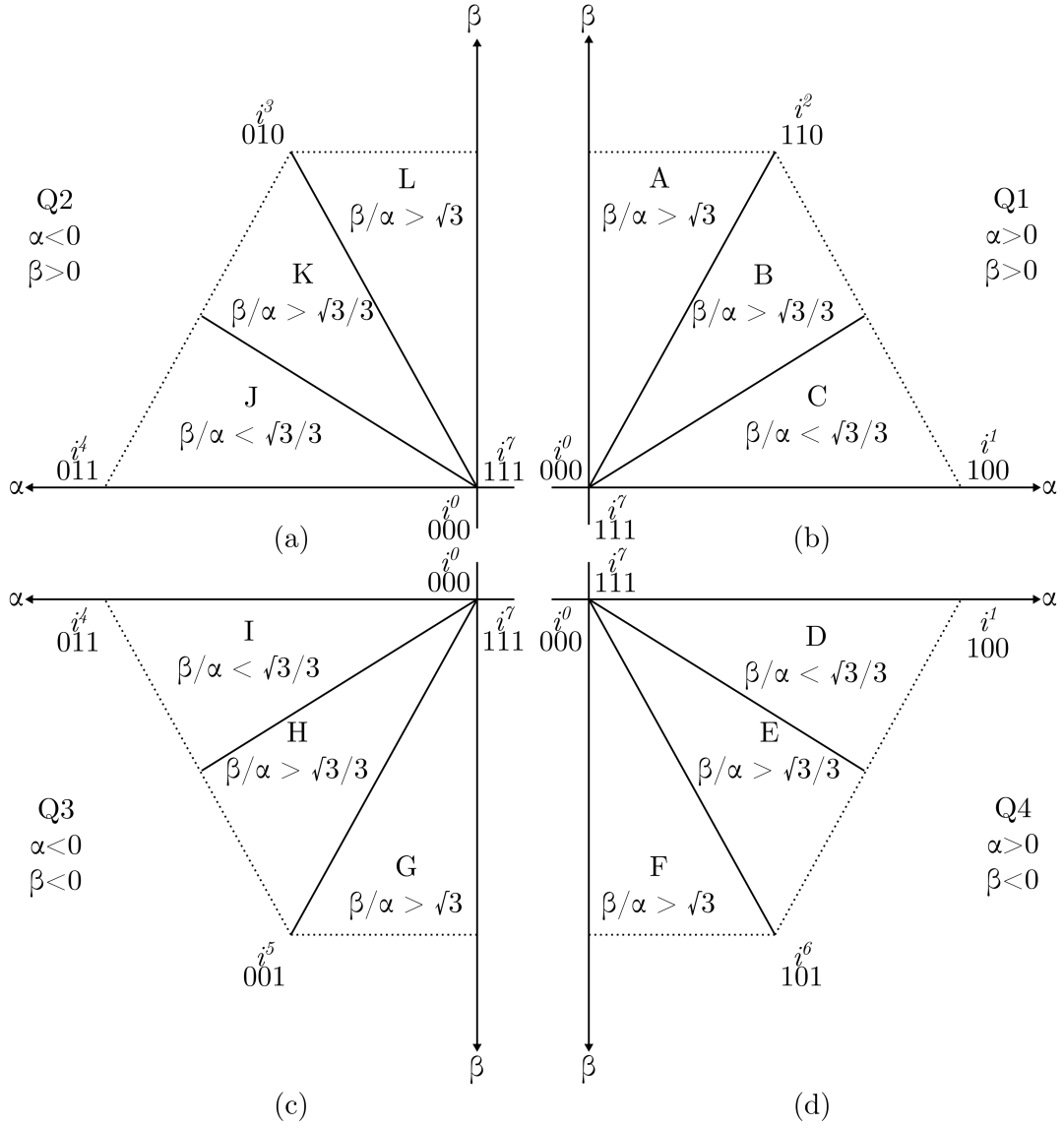


Figure 3.3: Quadrant and subsector identification.

the sampling period, according to the principle of deadbeat control. The duty factors for the active and zero vectors can be found by solving the following system of equations:

$$i_\alpha^{v_{opt}} d_1 + i_\alpha^{v'_{opt}} d_2 + i_\alpha^{v_0} d_0 = i_\alpha^* \tag{3.6}$$

$$i_\beta^{v_{opt}} d_1 + i_\beta^{v'_{opt}} d_2 + i_\beta^{v_0} d_0 = i_\beta^* \tag{3.7}$$

$$d_1 + d_2 + d_0 = 1 \tag{3.8}$$

where, $i_\alpha^{v_{opt}}$, $i_\alpha^{v'_{opt}}$ and $i_\alpha^{v_0}$ are the currents which would result from applying v_{opt}, v'_{opt} or either of the zero vectors for one whole sampling period respectively and d_1, d_2 and d_0 are the duty factors for the active and zero vectors respectively. When (3.6) through (3.8) are solved, the following expressions are obtained for the duty factors of the active vectors:

$$d_1 = -\frac{(i_\alpha^{v_0} i_\beta^{v'_{opt}} - i_\alpha^{v'_{opt}} i_\beta^{v_0} - i_\alpha^{v_0} i_\beta^{*} + i_\alpha^{*} i_\beta^{v_0} + i_\alpha^{v'_{opt}} i_\beta^{*} - i_\alpha^{*} i_\beta^{v'_{opt}})}{(i_\alpha^{v_0} i_\beta^{v_{opt}} - i_\alpha^{v_{opt}} i_\beta^{v_0} - i_\alpha^{v_0} i_\beta^{v'_{opt}} + i_\alpha^{v'_{opt}} i_\beta^{v_0} + i_\alpha^{v_{opt}} i_\beta^{v'_{opt}} - i_\alpha^{v'_{opt}} i_\beta^{v_{opt}})} \tag{3.9}$$

$$d_2 = \frac{(i_\alpha^{v_0} i_\beta^{v_{opt}} - i_\alpha^{v_{opt}} i_\beta^{v_0} - i_\alpha^{v_0} * i_\beta^{*} + i_\alpha^{*} i_\beta^{v_0} + i_\alpha^{v_{opt}} i_\beta^{*} - i_\alpha^{*} i_\beta^{v_{opt}})}{(i_\alpha^{v_0} i_\beta^{v_{opt}} - i_\alpha^{v_{opt}} i_\beta^{v_0} - i_\alpha^{v_0} i_\beta^{v'_{opt}} + i_\alpha^{v'_{opt}} i_\beta^{v_0} + i_\alpha^{v_{opt}} i_\beta^{v'_{opt}} - i_\alpha^{v'_{opt}} i_\beta^{v_{opt}})} \tag{3.10}$$

Again, d_0 is found using (3.8).

3.2.2 Extension to the Over-modulation Region

During large changes in the converter operating conditions, such as a drop in the DC link voltage, increase in the grid voltage or ramping up of the power reference, the current controller may be unable to achieve a given current set point within one sampling period due to the limitation of the available DC voltage. When considered geometrically, during periods of over modulation, the current reference vector lies outside the predicted current hexagon shown in Figure 3.2. While the optimizer will still select the two closest active vectors, the equations (3.6)-(3.8) will yield an infeasible solution for the duty factors where $d_1 + d_2 > 1$.

It was proposed in [245] to augment the controller with additional equations which can be used to select the optimum duty factors even if the requested output voltage lies beyond the linear range. In cases of over modulation, the duty factor for the zero vectors will naturally be zero to achieve the maximum possible output voltage magnitude. The output voltage is then synthesised from either one or two active vectors, depending on the reference. Where only one vector is used, the system converges towards the FCS-MPC case, which is known to be optimal for large transient errors [245]. Figure 3.4 illustrates the three modes of operation. The theoretical background for the over modulation method is examined in [245] and is repeated here only insofar as is necessary

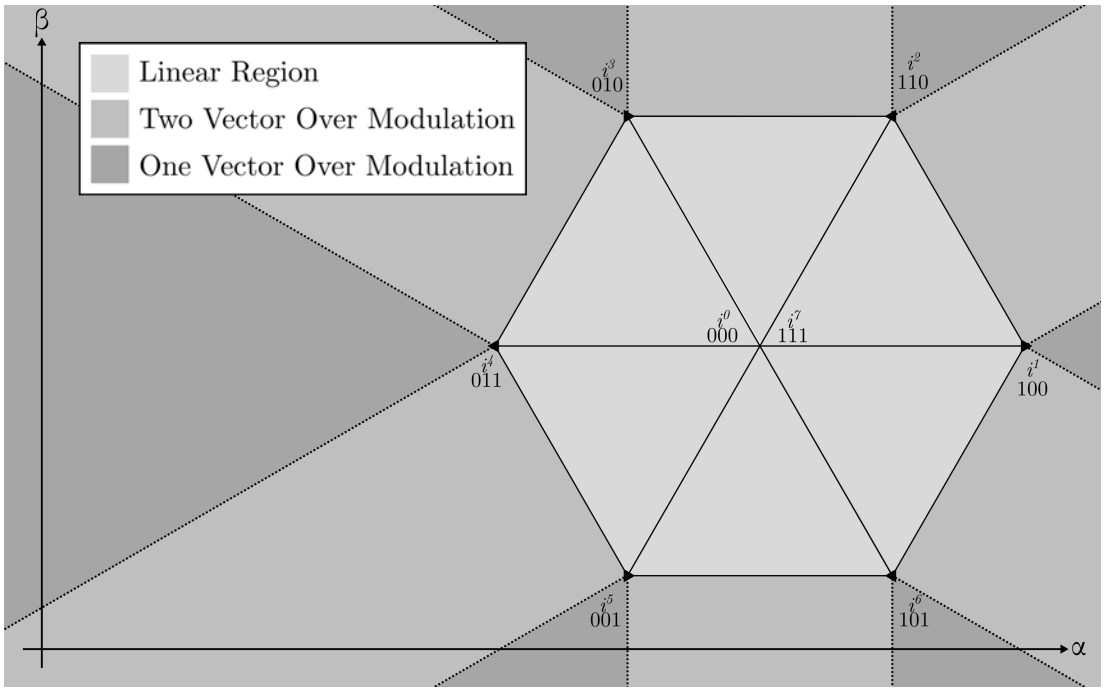


Figure 3.4: Zones where linear modulation, one vector over modulation and two vector overmodulation apply.

to explain the proposed simplification.

a. Two-Vector Over Modulation

The first scenario that can occur is where the current reference vector lies outwith the linear modulation region, but between two active vectors. Figure 3.5 shows such a reference. The region of interest is marked Zone 1. A circle is inscribed with its centre at the end of the current reference vector. The circle is expanded outward until it meets the linear modulation region at point A. This indicates that the minimum error is achieved where the vector i_{OM} is applied. Within Zone 1, the vectors v_{opt} and v'_{opt} are applied to create the current i_{OM}, which is known to be closest to i^* whilst respecting the modulation constraints. The relative duty factors for v_{opt} and v'_{opt} are obtained by considering the position of point A. The duty factor of v_{opt} is proportional to X_2 whilst the duty factor of v'_{opt} is proportional to X_1. The magnitudes of X_1 and

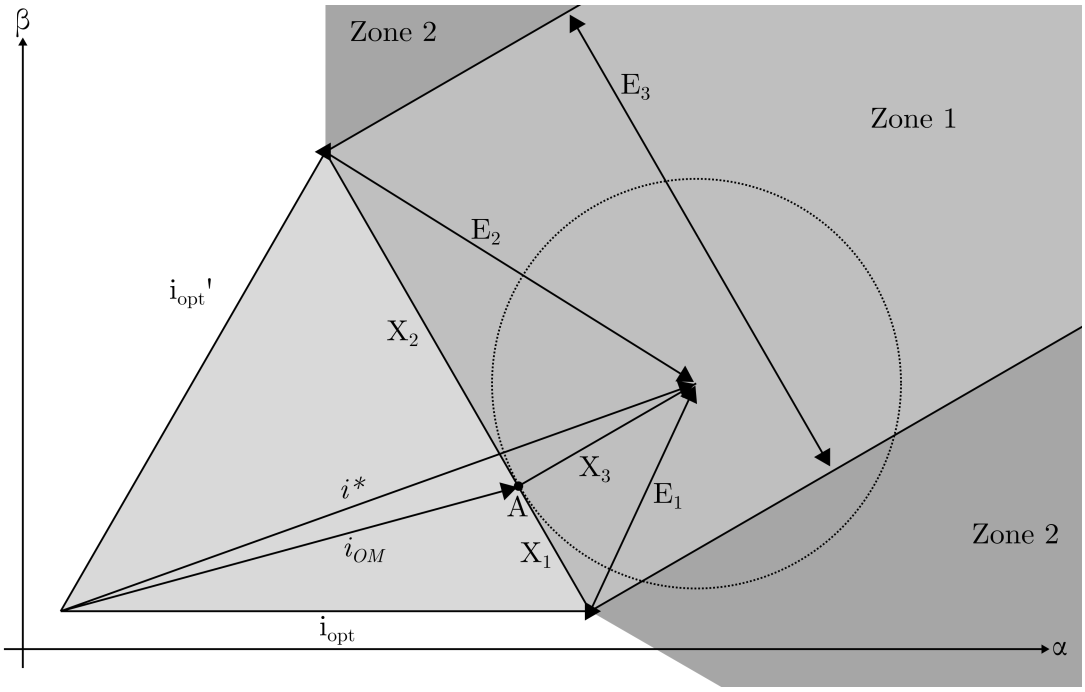


Figure 3.5: Vector diagram where a current reference vector lies outside the linear modulation region.

X_2 are obtained by first calculating the vectors E_1, E_2 and E_3 as follows:

$$E_1 = i^* - i_{opt} \tag{3.11}$$

$$E_2 = i^* - i'_{opt} \tag{3.12}$$

$$E_3 = i'_{opt} - i_{opt} \tag{3.13}$$

The magnitude of vectors X_1 and X_2 are then found using Pythagoras' theorem as follows:

$$|X_1| = \frac{1}{2}\left(\frac{|E_1|^2 - |E_2|^2 + |E_3|^2}{|E_3|}\right) \tag{3.14}$$

$$|X_2| = \frac{1}{2}\left(\frac{|E_2|^2 - |E_1|^2 + |E_3|^2}{|E_3|}\right) \tag{3.15}$$

Finally, the duty factors are obtained by normalising the magnitudes of X_1 and X_2 with respect to the total distance E_3 as follows:

$$d_1 = \frac{|X_2|}{|E_3|} \tag{3.16}$$

$$d_2 = \frac{|X_1|}{|E_3|} \tag{3.17}$$

As stated previously, $d_0 = 0$ during over modulation conditions. If the magnitudes of either X_1 or X_2 are greater than the magnitude of E_3, this leads to a duty factor greater than unity, indicating that one-vector over modulation is not applicable. In this case, the reference vector lies in Zone 2.

b. One-Vector Over Modulation

The second over modulation scenario which can occur, is where the reference vector lies outwith the linear region, but in the triangular areas extending from the points of i_{opt} and i'_{opt}. These regions are marked Zone 2 in Figure 3.5. In these zones, either v_{opt} or v'_{opt} should be applied for the whole sampling period, in effect, causing the controller to behave like the conventional FCS-MPC.

c. Proposed Simplification

In both [245] and [178], checks were performed to see whether the current reference lies closer to i_{opt} or i'_{opt} during over modulation. However, this is unnecessary, since if the reference vector was closer to i'_{opt} then clearly i'_{opt} would have been selected as i_{opt} in the first place. The over-modulation algorithm can therefore be simplified as shown in Figure 3.6, where only two comparison operations are required to identify which modulation scenario is required. One to establish whether over-modulation is required and another to establish whether one active or two active vectors must be used.

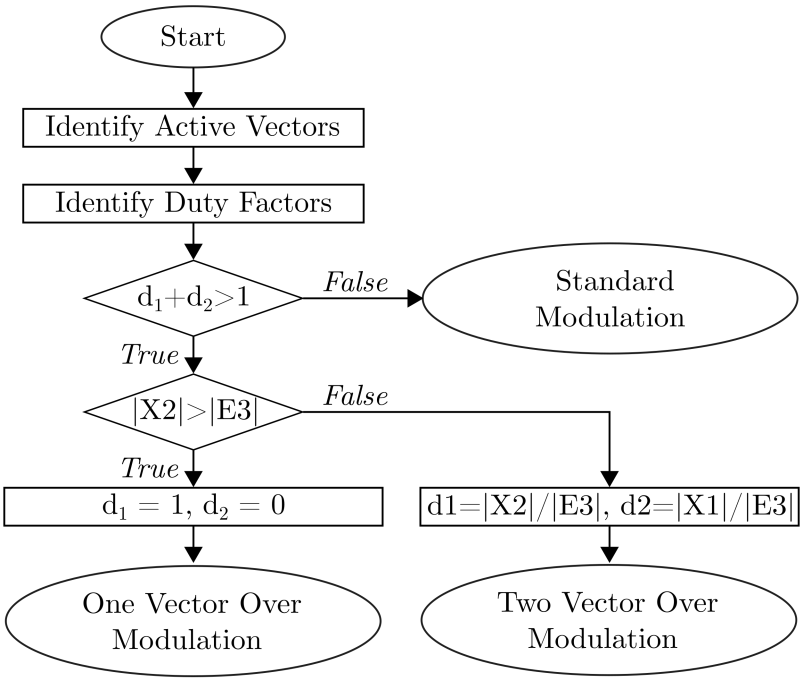


Figure 3.6: Flowchart of the proposed MMPC algorithm with optimized over-modulation.

3.3 Current Reference Generation

To export a required active and reactive power to the grid, reference currents must be calculated according to the grid voltage. The current references are found by solving the following equation:

$$\begin{bmatrix} P^* \\ Q^* \end{bmatrix} = \frac{3}{2} \begin{bmatrix} v_{g\alpha(k)} & v_{g\beta(k)} \\ v_{g\beta(k)} & -v_{g\alpha(k)} \end{bmatrix} \begin{bmatrix} i^*_{\alpha(k)} \\ i^*_{\beta(k)} \end{bmatrix} \tag{3.18}$$

As with any digital control scheme, MPC samples the input variables at regular instants and then performs calculations based on these measurements. If the system is sampled at instant k, by the time the necessary calculations have been performed, the control decision may be out of date when it is applied. To compensate this delay, the controller may extrapolate future quantities to be used to solve for the optimum control action to be applied at instant $k+1$ to minimize the cost function at $k+2$. The future current references and grid voltages can be extrapolated using a second-order Lagrange

quadratic formula as follows [247]:

$$i^*_{(k+1)} = 3i^*_{(k)} - 3i^*_{(k-1)} + i^*_{(k-2)} \tag{3.19}$$

$$i^*_{(k+2)} = 3i^*_{(k+1)} - 3i^*_{(k)} + i^*_{(k-1)} \tag{3.20}$$

where, $i^*_{(k+2)}$ is the current reference extrapolated for instant k+2, $i^*_{(k+1)}$ is the current reference extrapolated for instant k+1, $i^*_{(k)}$ is the known current reference at instant k, $i^*_{(k-1)}$ is the previous current reference at k–1 and $i^*_{(k-2)}$ is the previous current reference at instant k–2. The same technique is used to extrapolate the future grid voltages.

3.4 Synthesis of the Output Voltage with a Standard PWM Module

Most basic microcontrollers offer a timer peripheral, which can generate simple PWM waveforms. More advanced microcontrollers designed with power electronic applications in mind may offer dedicated PWM modules which offer additional functionality. Typical features include the ability to periodically trigger ADC sampling, the ability to generate hardware interrupts to execute time-critical tasks or additional logic to allow rapid shutdown in response to a fault without involving the CPU. Regardless of the exact microcontroller used, the core methodology for generating the PWM is the same. The timer or PWM peripheral will contain a digital counter which increments or decrements according to a clock. A 'period' value is generally held in a register and when the count reaches this value, it either resets to zero, or begins decrementing to zero depending on the configuration. As the counter increments or decrements, the current value is compared with a reference value held in a 'compare' register. If the two are equal, an action may be triggered, such as setting the PWM output high or low. Differing actions may be taken depending on whether the timer was counting up or down at the time when the comparison was performed.

Figure 3.7 shows a very typical PWM timer configuration. The main timer is

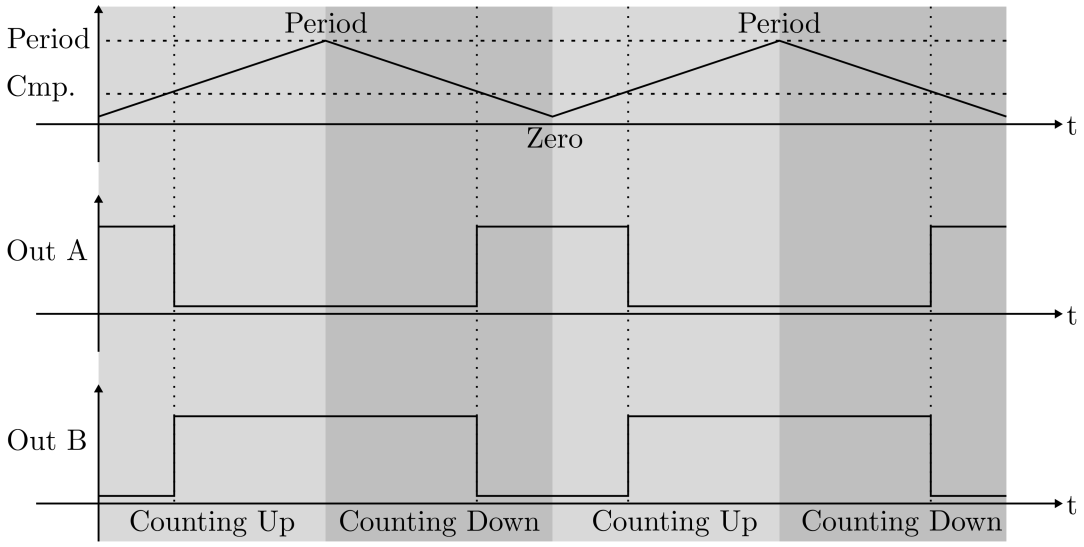


Figure 3.7: Typical complementary active high PWM generation.

set to 'up/down' mode. The comparator is configured to set one output low when the comparison is true on the up count, or set the output high if the comparison is true on the down count. A second comparator is configured to do the opposite: set the other output high when the comparison is true on the up count, or set the output low if the comparison is true on the down count. This generates the well known 'complementary active-high' PWM waveform which can be used to control the high- and low-side switches in a half-bridge circuit. It should be noted that dead time has been neglected in Figure 3.7. This can be added by using a second comparator unit and different compare value to cause the 'a' and 'b' outputs to switch at different instants, or by selecting a microcontroller with dedicated dead band logic independent of the counter/compare logic. For a typical vector current controller, whose output is a modulation index between -1 and 1, all that is required is a simple shift-and-scale function to convert the modulation index to a compare value between zero and the 'period' value. This value can then be loaded directly into the 'compare' register at the end of every current control iteration and the process is complete. However, the output of the MMPC is in the form of numbered vectors and three dwell times. Therefore, additional logic is required to convert these parameters into simple compare

values which can be input to a standard PWM peripheral. For implementation of the modulation, it is more convenient to work in terms of duty factor than dwell times, therefore, the calculated dwell times are first transformed into duty factors between 0 and 1 as follows:

$$d_0 = \frac{\tau_0}{T_s} \tag{3.21}$$

$$d_1 = \frac{\tau_1}{T_s} \tag{3.22}$$

$$d_2 = \frac{\tau_2}{T_s} \tag{3.23}$$

where, d_0 is the duty factor of the zero vectors, d_1 is the duty factor of the optimum vector and d_2 is the duty factor of the second best vector. The switching sequence of the vectors is illustrated in Figure 3.8, where v_{opt} and v'_{opt} are shown as vectors 3 and 2 respectively and arbitrary dwell times are used. As shown in Figure 3.8, vectors 0 and 7 are used to create the total zero vector contribution. v_0 is applied for $\frac{\tau_0}{4}$ at the start and end of the sampling window and v_7 is applied for $\frac{\tau_0}{2}$ in the middle. Therefore, as a minimum, the duty factor for each phase must be half of the zero vector dwell time. Therefore, the initial, temporary values for the duty factors are set as follows:

$$d_a = \frac{d_0}{2} \tag{3.24}$$

$$d_b = \frac{d_0}{2} \tag{3.25}$$

$$d_c = \frac{d_0}{2} \tag{3.26}$$

Next, phase 'a' is considered. Vectors 1, 2 and 6 all involve setting phase 'a' high. Therefore, if either v_{opt} or v'_{opt} is equal to 1, 2 or 6 (one of them must always be) then

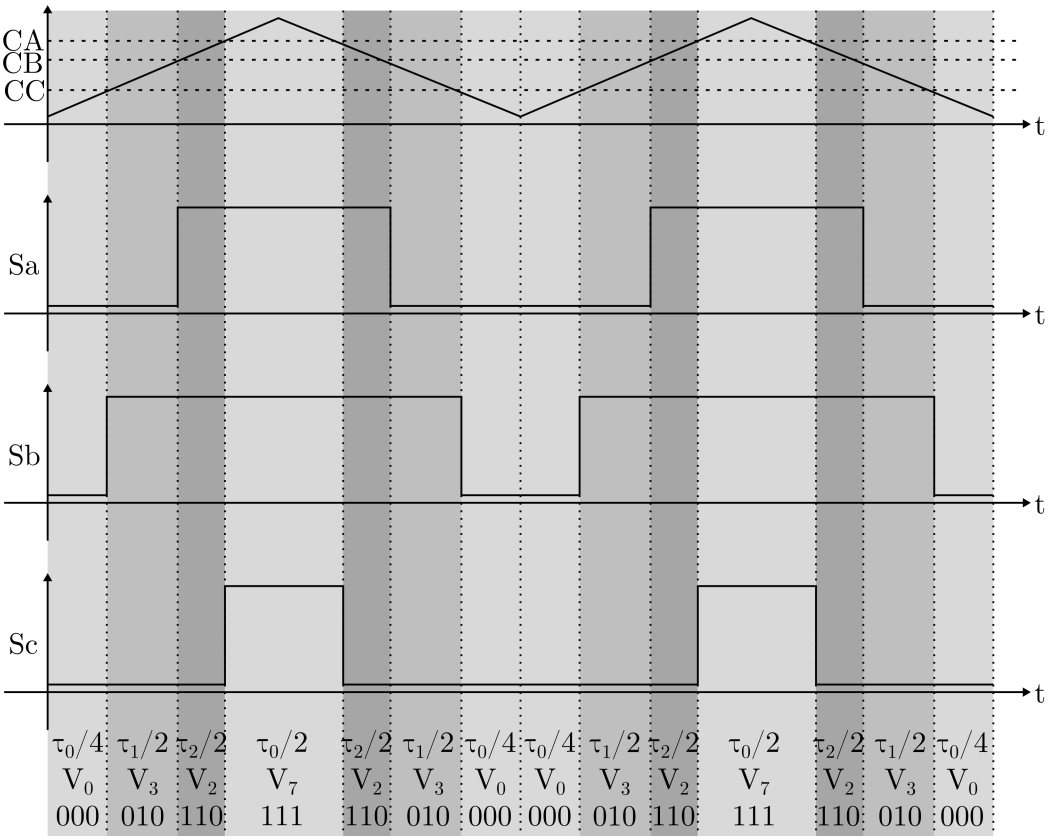


Figure 3.8: Example of the MMPC switching sequence, showing the triangular counter waveform and the status of each phase over two sampling periods.

the phase 'a' duty factor is increased by the duty factor of relevant vector as shown:

$$\text{if}(v_{opt} = 1,\ 2 \text{ or } 6)$$
$$d_a = d_a + d_1 \tag{3.27}$$
$$\text{if}(v'_{opt} = 1,\ 2 \text{ or } 6)$$
$$d_a = d_a + d_2 \tag{3.28}$$

Similarly, for phase 'b', vectors 2, 3 and 4 all involve setting phase 'b' high. Therefore, if either v_{opt} or v'_{opt} is equal to 2, 3 or 4 (one of them must always be) then the phase

'b' duty factor is increased by the duty factor of relevant vector as shown:

$$\text{if}(v_{opt} = 2, 3 \text{ or } 4)$$
$$d_b = d_b + d_1 \tag{3.29}$$
$$\text{if}(v'_{opt} = 2, 3 \text{ or } 4)$$
$$d_b = d_b + d_2 \tag{3.30}$$

Finally, for phase 'c', vectors 4, 5 and 6 all involve setting phase 'c' high. Therefore, if either v_{opt} or v'_{opt} is equal to 4, 5 or 6 (one of them must always be) then the phase 'c' duty factor is increased by the duty factor of relevant vector as shown:

$$\text{if}(v_{opt} = 4, 5 \text{ or } 6)$$
$$d_c = d_c + d_1 \tag{3.31}$$
$$\text{if}(v'_{opt} = 4, 5 \text{ or } 6)$$
$$d_c = d_c + d_2 \tag{3.32}$$

3.5 Impact of Parameter Mismatch and Discretization

The effectiveness of any MPC scheme is governed by the accuracy of the predictive model used. The predictive current formula (3.3) is widely accepted in literature and has been used in many MPC and deadbeat control implementations. However, there are few significant assumptions made, namely:

1. The modelled parameters L and R used in the controller are equal to their actual values in the real system.
2. The current derivative is accurately approximated by the forward Euler method.
3. The grid voltage is constant during the sample period.

The impact of parameter mismatch was explored in [248], where a range of incorrect inductance and resistance values were inserted into the predictive model (3.3) and the resulting erroneous predictions are compared with predictions using the same formula

but with the actual values of L and R. As expected, the minimum error occurs where L and R used in the predictive formula are equal to their actual values. However, this existing work does not consider the effects of grid voltage discretization and the accuracy of the forward Euler approximation. These combined effects have not been investigated properly for MPC systems in literature.

Figure 3.9a shows the effect of a similar parameter mismatch on the MPC proposed in this paper. The modelled inductance and resistance R_0 and L_0 are kept constant inside the controller, while the actual values in the real system, R and L, are varied. The actual measured output current of the proposed MPC is compared with the current references given by (3.18). This ensures that the effects of changing grid voltage and the Euler approximation are also exposed. The steady-state error (SSE) is calculated as follows:

$$SSE_{\%} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(i^{*}_{a(k)} - i_{a(k)}\right)^{2}} * 100\% \tag{3.33}$$

where, N is the number of samples and phase 'a' is used for the calculations. Changing the real inductance above or below its modelled value inside the controller leads to an increase in the steady-state error. This is expected since an incorrect inductance will lead to an incorrect output voltage being calculated. The resistance mismatch effect is minimal since the resistance is an order of magnitude smaller than the inductive reactance at the grid frequency. Inspection of Figure 3.9a suggests that the steady-state error is minimized when the actual inductance of the real system L is less than its modelled value inside the controller L_0. This differs from the previous conclusion in [248] since, in this case, the actual current is compared with the reference current, therefore the accuracy of the Euler approximation and the effect of grid voltage discretization are also considered. The predictive model of (3.3) assumes that the grid voltage is constant during the sampling period. In fact, the grid voltage is a continuous sinusoidal waveform, as shown in Figure 3.10. Instead of using the approximate model (3.3), it is possible to obtain an exact analytical expression for the future grid current by solving the continuous differential equation of (3.1). Taking the alpha component

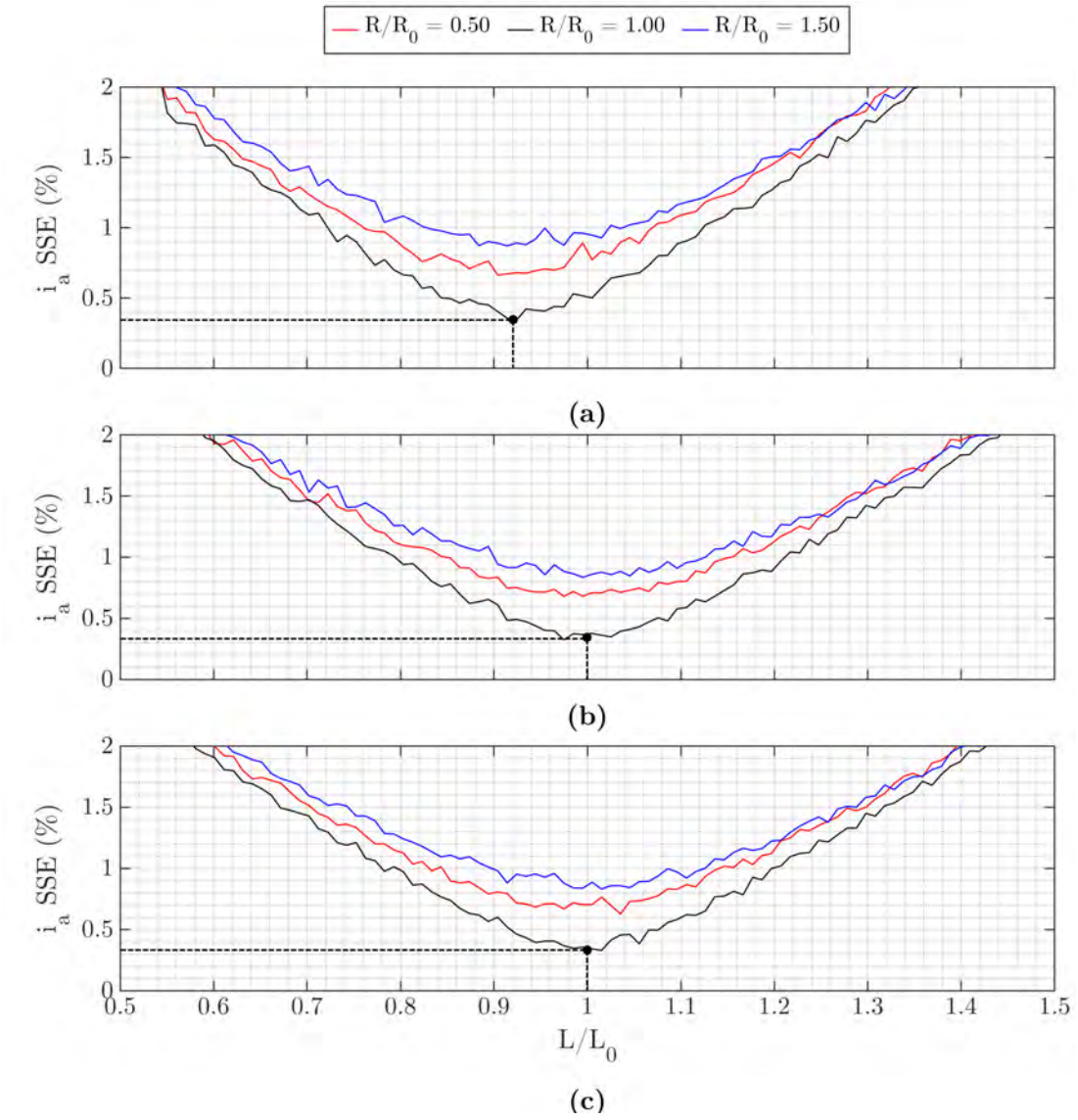


Figure 3.9: Steady-state current error when the resistance and inductance of the actual system are varied from 0.5 to 1.5pu while the values used inside the controller are kept constant. The system parameters are as shown in Table 3.1. The error is plotted as a function of the mismatch where (a) the grid voltage discretization is not compensated, (b) the grid voltage discretization is compensated exactly using (3.35) and (c) the grid voltage discretization is compensated approximately using the method proposed in (3.36).

as an example, a sinusoidal grid voltage is assumed, given by:

$$v_{g\alpha}(t) = V_{g\alpha}^{pk} sin(\omega t + \omega t_o) \tag{3.34}$$

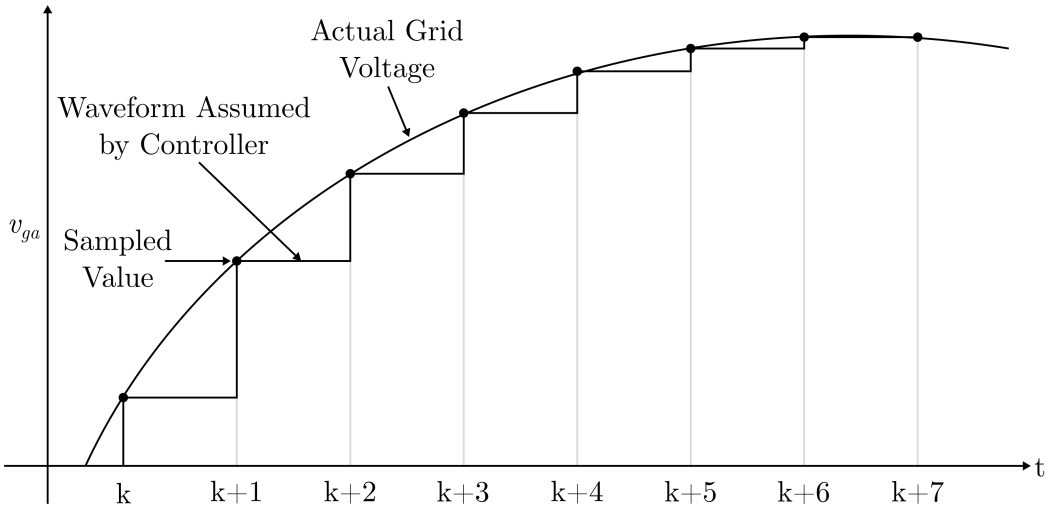


Figure 3.10: Actual grid current waveform compared to the discretized version assumed by the controller.

where, $V_{g\alpha}^{pk}$ is the peak grid voltage, ω is the angular frequency of the grid and t_0 is an initial time corresponding to the instantaneous phase angle of the grid. This grid voltage is substituted into the differential equation (3.1) and the equation is solved for time $t = T_s$ as shown in (3.35).

$$\begin{aligned} i_{\alpha(k+1)} = e^{-\frac{RT_s}{L}} & \left(i_{\alpha(k)} - \frac{R^2 v_{t\alpha(k)} - R^2 v_{g\alpha}^{pk} sin(\omega t_0)}{R(L^2\omega^2 + R^2)} \right. \\ & \left. + \frac{L^2 v_{t\alpha(k)}\omega^2 + LR v_{g\alpha}^{pk}\omega cos(\omega t_0)}{R(L^2\omega^2 + R^2)} \right) \\ & + \left(\frac{R^2 v_{t\alpha(k)} + L^2 v_{t\alpha(k)}\omega^2 - R^2 v_{g\alpha}^{pk} sin(\omega t + \omega t_0)}{R(L^2\omega^2 + R^2)} \right. \\ & \left. + \frac{LR v_{g\alpha}^{pk} cos(\omega t + \omega t_0)}{R(L^2\omega^2 + R^2)} \right) \end{aligned} \tag{3.35}$$

Figure 3.9b shows that the current error is minimized when the precise predictive formula (3.35) is used in place of (3.3) in the controller and R and L are perfectly matched with their correct values in the real system. However, evaluating (3.35) requires knowledge of the angular velocity of the grid voltage ω, the peak value of the grid voltage $V_{g\alpha}^{pk}$ and the instantaneous phase of the grid voltage, ωt_0. Since none of these parameters

are known to the current controller, it cannot use the exact formula to solve for the predicted grid current. A new method is needed to predict the grid current more accurately than (3.3) but without the computational complexity and unknown parameters required by (3.35). Therefore, a simple modified grid voltage value is included in (3.3) which takes into account that the voltage is changing over the sampling time. For the first prediction step, a modified value for $v_{g\alpha(k)}$ is needed.

During the period where the grid voltage is rising, if the value of $v_{g\alpha(k)}$ is used in the calculations, then the predicted current will be overestimated since the voltage is actually higher than this for most of the sampling period. Conversely, if the value of $v_{g\alpha(k+1)}$ is used, the current is underestimated since the grid voltage is actually lower than this for most of the sampling period. The same logic applies during the period where the grid voltage is falling. If the value of $v_{g\alpha(k)}$ is used,the predicted current will be underestimated since the voltage is lower than this for most of the sampling period and if the value of $v_{g\alpha(k+1)}$ is used, the current is overestimated since the grid voltage is higher than this for most of the sampling period. In short, some value between $v_{g\alpha(k)}$ and $v_{g\alpha(k+1)}$ will provide a better approximation of the grid voltage between the sampling instants.

The arithmetic mean of $v_{g\alpha(k)}$ and $v_{g\alpha(k+1)}$ is simple to calculate and provides a good approximation of the grid voltage over a sample period. The predictive formula (3.3) is changed to include the modified grid voltage term as follows:

$$\begin{bmatrix} i_{\alpha(k+1)} \\ i_{\beta(k+1)} \end{bmatrix} = \left(1 - R\frac{T_s}{L}\right) \begin{bmatrix} i_{\alpha(k)} \\ i_{\beta(k)} \end{bmatrix} + \frac{T_s}{L} \left(\begin{bmatrix} v_{t\alpha(k)} \\ v_{t\beta(k)} \end{bmatrix} - \frac{1}{2} \left(\begin{bmatrix} v_{g\alpha(k)} \\ v_{g\beta(k)} \end{bmatrix} + \begin{bmatrix} v_{g\alpha(k+1)} \\ v_{g\beta(k+1)} \end{bmatrix} \right) \right) \tag{3.36}$$

Similarly, the mean of $v_{g\alpha(k+1)}$ and $v_{g\alpha(k+2)}$ may be used for the second prediction stage. The effectiveness of this proposed modification is shown in Figure 3.9c where minimum error is achieved where the actual parameters R and L are perfectly matched with their modelled values R_0 and L_0 and the approximate compensation method in (3.36) is used. Comparison between Figure 3.9c and Figure 3.9b proves that the proposed

Table 3.1: Simulation Parameters for the proposed MMPC and conventional MMPC.

Parameter	Symbol	Value	Unit
Nominal Grid Phase Voltage (RMS)	V_g	100	V
Grid Fundamental Frequency	f_{grid}	50	Hz
Switching Frequency	f_{sw}	10	kHz
DC Link Voltage	V_{dc}	400	V
Filter Inductance	L	10	mH
Filter Resistance	R	0.1	Ω
Rated Power	P_{rated}	2	kW
Rated Current (Peak)	i_{rated}	9.428	A

approximate compensation is equally as effective as the exact compensation but with significantly less computational burden and no reliance on unknown parameters.

3.6 Simulation Results

The proposed simplified MMPC algorithm is studied using the Matlab/Simulink package to verify its effectiveness. The parameters of the simulation are shown in Table 3.1. The choice of filter components is consistent with [115, 127, 131, 184, 208, 248–251]. The steady-state current at full rated power for the proposed MMPC and the conventional MMPC is shown in Figure 3.11. The proposed MMPC offers identical performance to the conventional MMPC. The total harmonic distortion (THD) and SSE are the same in both cases. The output currents of both controllers have little ripple and the THD is low, therefore, a high power quality is achieved in both cases. The harmonic spectrum of the output current is studied in Figure 3.12. As expected, the proposed MMPC and conventional MMPC have identical harmonic spectra, with the harmonics centred around the switching frequency. The transient behaviour of the proposed controller is also studied during a step change in active power from zero to rated power at unity power factor. The currents are shown in Figure 3.13 and the active and reactive powers are shown in Figure 3.14. The fast transient response associated with MPC is evident for both controllers and a steady-state is reached in 1.5 ms. Figure 3.11 and Figure 3.13 combined prove that the proposed implementation of MMPC achieves identical performance to the established technique during both steady-state and transient

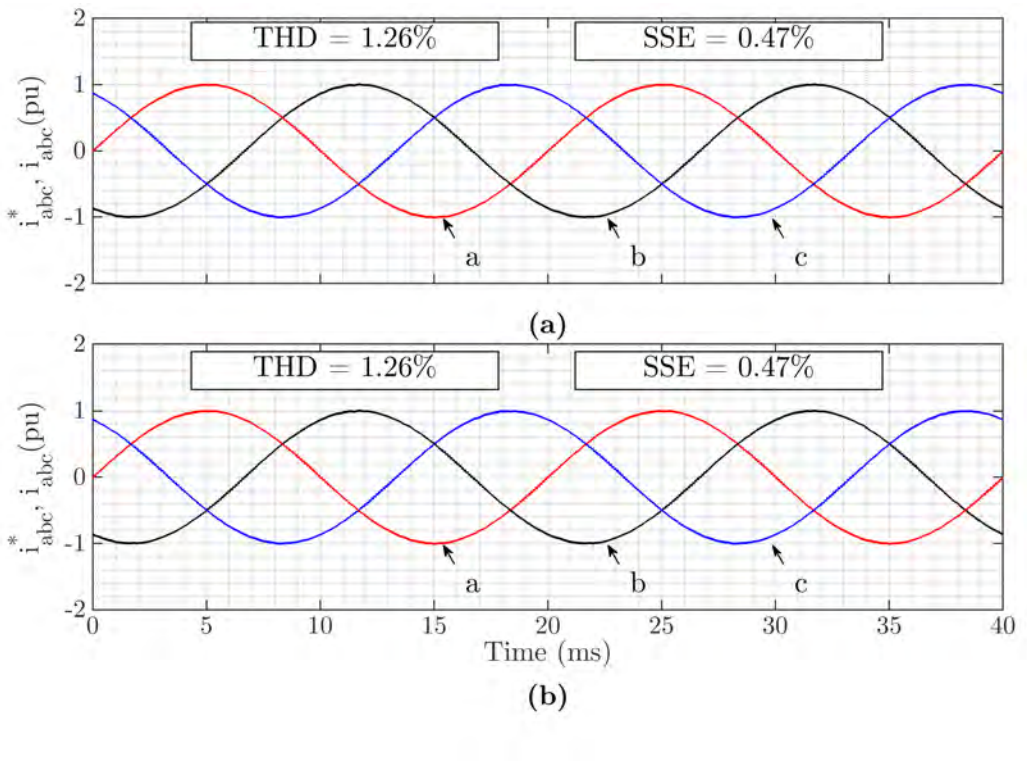


Figure 3.11: Steady-state current for (a) the proposed MMPC and (b) the conventional MMPC.

operation.

3.7 Experimental Results

The proposed MMPC algorithm was implemented on a Texas Instruments TMS320F28379D microcontroller forming part of a two-level grid-connected VSC system as shown in Figure 3.15 A digital output pin is set high when the analogue-to-digital (ADC) results are ready and the current control tasks begin, then it is set low again when the calculations are complete to verify the reduction in computation time. Figure 3.16a shows the computation time for the proposed MMPC and Figure 3.16b shows the computation time for the conventional implementation.

As shown in Figure 3.16, the execution time of the conventional MMPC algorithm is 20.5 μs while the proposed algorithm executes in only 11.1 μs. This represents a reduction in computation time of 46% for no reduction in performance. The reduced

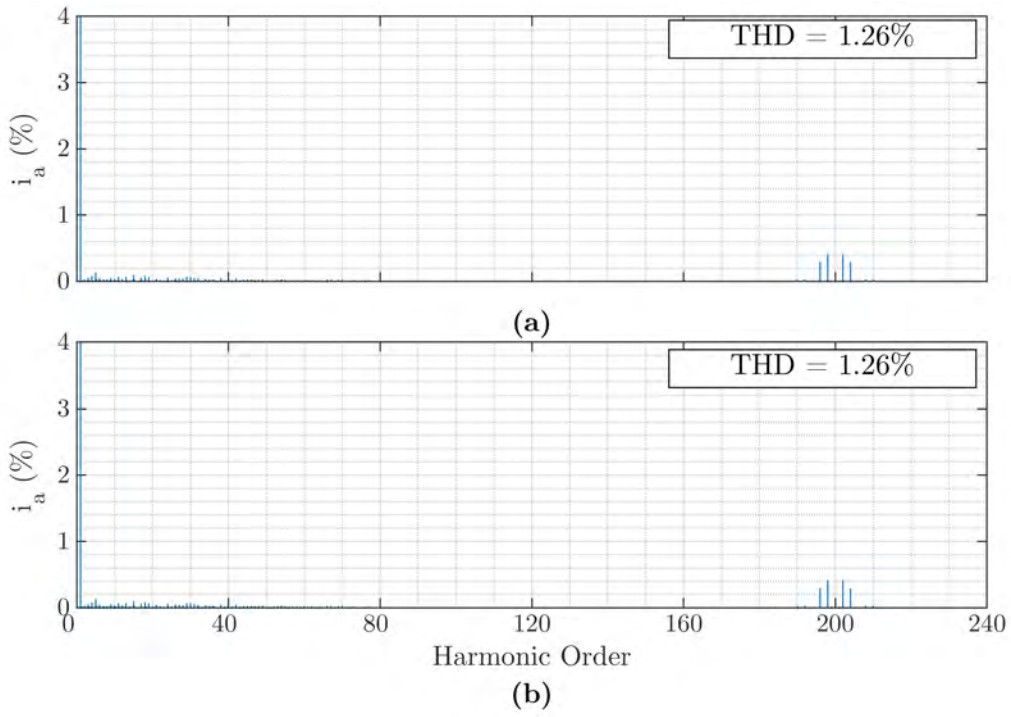


Figure 3.12: Harmonic spectrum for (a) the proposed MMPC and (b) the conventional MMPC.

execution time of the proposed algorithm means that the sampling frequency could be increased to a maximum of 90 kHz, compared with 49 kHz for the conventional technique. Alternatively, where faster sampling is not required, a lower cost and less capable microcontroller could be used, or time could be committed to performing other tasks.

3.8 Summary

An efficient implementation of the MMPC current control algorithm has been proposed. Simulation results have been shown which prove that the proposed current controller achieves identical performance in steady-state and transient conditions as the established technique. Experimental data has been included to verify the reduction in computational burden. The proposed method achieves identical performance to the well-known algorithm while requiring 46% less computation time.

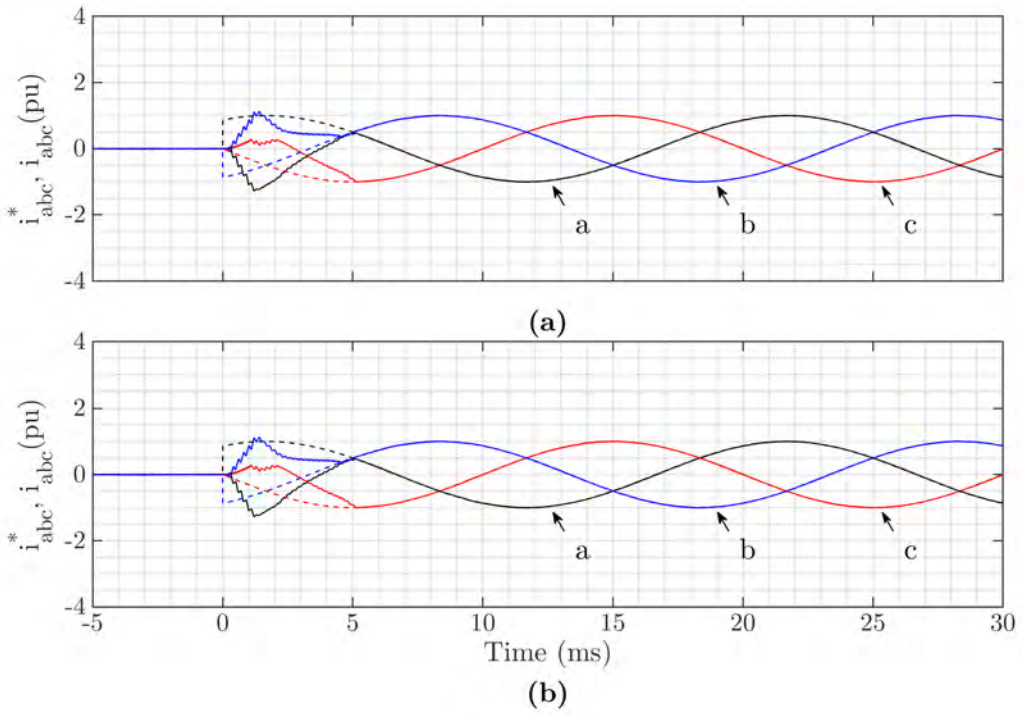


Figure 3.13: Current during a step change from zero to full power for (a) the proposed MMPC and (b) the conventional MMPC.

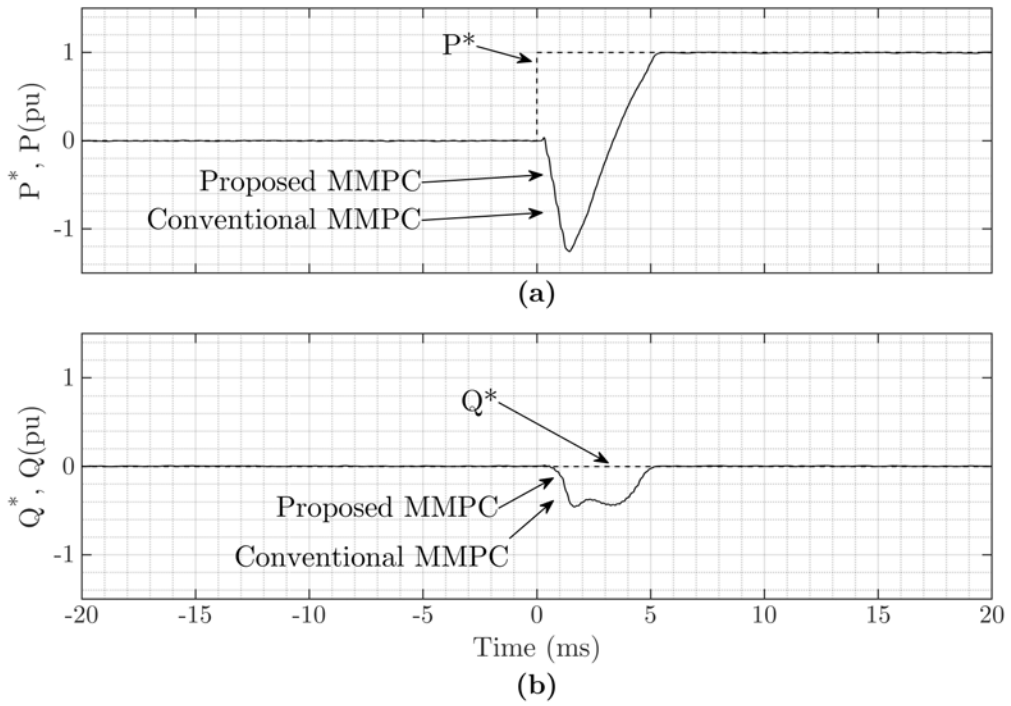


Figure 3.14: Active and reactive power tracking during a step change from zero to full power (a) the active power (b) the reactive power.

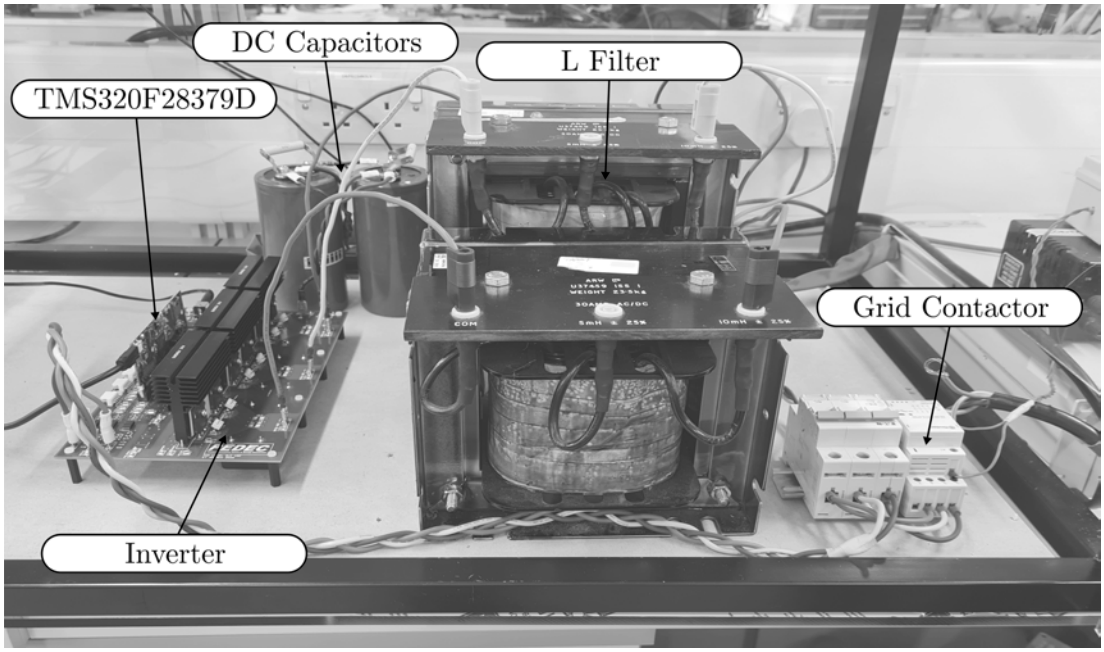


Figure 3.15: The hardware test rig.

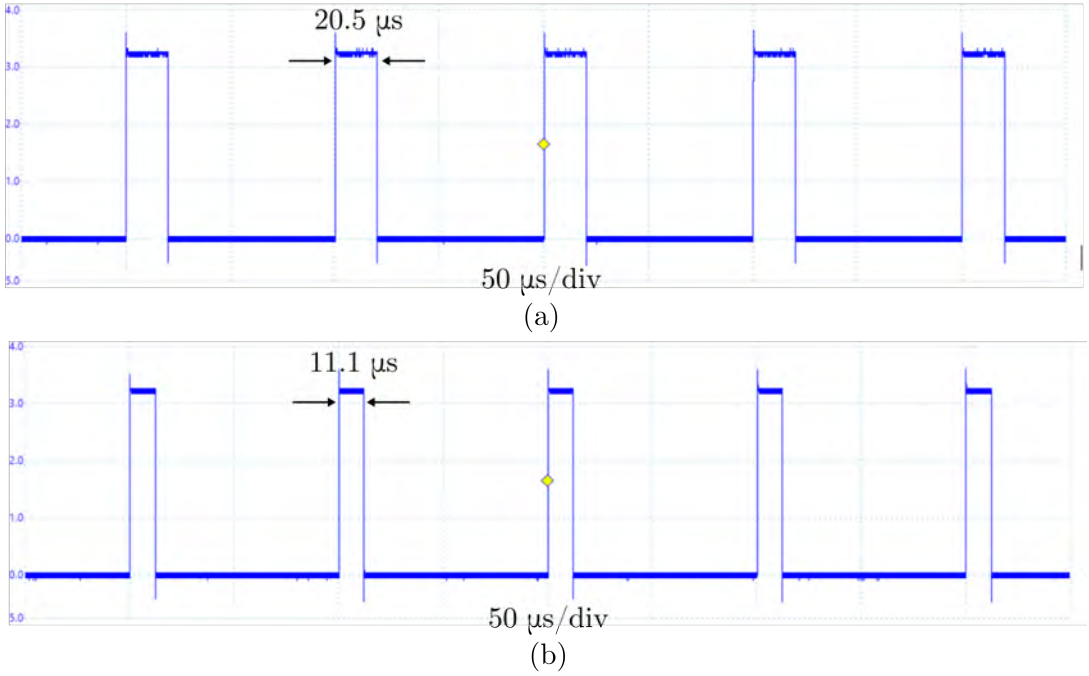


Figure 3.16: Execution time of (a) the proposed MMPC and (b) the conventional MMPC.

Chapter 4

New Modulated Model Predictive Control for Unbalanced Grids

Distributed energy resources are often connected to low-voltage distribution networks where the grid voltages may be unbalanced, making the control design challenging.

The method of symmetrical components allows an unbalanced set of three-phase voltages to be decomposed into three balanced components, known as the positive, negative and zero sequence components. In a three-wire system, the zero-sequence component is unable to flow. The presence of a negative sequence component in the grid voltage leads to an unwanted ripple in the output active power at twice the fundamental grid frequency. However, if the symmetrical components of the grid voltage are known, separate references may be generated for the positive and negative sequence currents which allows the ripple in the active power to be eliminated.

In this chapter, a new model predictive current controller is proposed for unbalanced grids. The improved MMPC proposed in chapter 3 is enhanced by adding a Kalman filter estimator to extract the positive and negative sequence components of the grid voltage. A new calculation time compensation technique is also proposed, which offers superior accuracy to existing approaches. The grid voltage discretization compensation

strategy outlined in chapter 3 is also applied to the unbalanced system and its effectiveness is demonstrated. Finally, the system stability is verified theoretically. Simulation and laboratory results are included to prove the robustness of the proposed controller and support the theoretical analysis.

The rest of the chapter is organized as follows. Section 4.1 studies the state of the art in model predictive current controllers in unbalanced systems. Section 4.2 describes the modified extended complex Kalman filter (ECKF) estimator. Section 4.3 describes the proposed control system. Section 4.4 verifies that the proposed controller is stable in the sense of Lyapunov in the vicinity of the steady-state. Section 4.5 studies the proposed control system in simulation and compares it with two existing MPC controllers. Section 4.6 includes the results of the experimental validation. Section 4.7 compares the computational burden of the proposed technique and the conventional MPC.

4.1 MPC in Unbalanced Systems

Uneven loading across the phases, unbalanced line and transformer impedances, nonlinear loads and asymmetrical grid faults can combine to create unbalance in the grid voltages which must be considered during the control design [251, 252]. Several techniques have been proposed to allow model predictive current controllers to be applied to unbalanced systems.

The symmetrical component approach is the most common technique and many methods have been proposed to extract the symmetrical components [253]. MPC controllers have been proposed using delayed signal cancellation (DSC) [137,254]. However, the delay makes it unattractive for situations with a high current control bandwidth. To avoid the drawbacks of DSC, MPC current controllers have been proposed using PLLs [207, 255]. This introduces all the challenges of PLL design to a system which would otherwise operate entirely in a stationary frame. In [251], a predictive controller was proposed using a neural network to separate the sequence components, however, the learning rate must be tuned carefully and many trigonometric calculations are re-

quired. In [256] and [257], state observers were employed. However, the system is complex and the gains must be tuned carefully to ensure stability [258]. In [249], a sliding-mode grid voltage observer for unbalanced grids (SMGVO) was proposed, however, a frequency-locked loop (FLL) is required which brings all the well-known challenges of FLLs [258]. In [259], a new state-space formulation of the symmetrical component extraction problem has been developed and an extended complex Kalman filter (ECKF) was proposed to estimate the symmetrical components even in noisy systems. Moreover, the ECKF estimator compares well with the techniques examined in [260], where the response times of dual second order generalized integrator (DSOGI), moving average filter (MAF), delayed signal cancellation (DSC) and delay operation period filter (DOPF) based techniques are estimated.

Recently, in [251] a neural network based virtual flux (NN-VF) estimator is proposed to accurately and quickly detect the positive and negative sequence components of the grid voltage. The estimator is coupled with a predictive direct power control (VF-PDPC) to achieve a complete control solution for a voltage source converter in an unbalanced grid. The proposed estimator avoids cascaded delays present in cascaded filter approaches and the complex tuning procedure required for observer based approaches. However, the tuning procedure lacks an analytical solution [261]. In [262, 263], neural network voltage estimators are proposed, however, too many parameters need to be adjusted online [258].

Virtual flux estimation under unbalanced grid conditions is initially explored in [264], where a direct power control with space vector modulation for unbalanced grids is proposed, however, a PLL and low pass filter are employed which degrades the transient performance of the system. To calculate the virtual flux, a pure integration is required which is sensitive to dc-drift and initial bias in practical implementations [258]. To address this, low-pass filters have been used instead of pure integrators, however, they introduce inevitable gain and phase errors [265, 266].

Adaptive state observers are proposed in [257] and [256] to extract the positive and negative sequence components of an unbalanced grid voltage. However, the observer gains must be tuned carefully to ensure the stability of the observer [258]. In [249], a

sliding-mode observer (SMO) is proposed, however, the grid frequency is needed which must be estimated separately by a PLL.

4.2 Modified Extended Complex Kalman Filter

This section describes the proposed ECKF which is used to extract the instantaneous positive and negative sequence components of the grid voltage. A modification is then proposed to estimate the voltages two steps in advance to compensate the calculation time. The positive and negative sequence components can be expressed in complex exponential form as follows:

$$V^+ = v_\alpha^+ + jv_\beta^+ = A^+ e^{j\omega k T_s} \tag{4.1}$$

$$V^- = v_\alpha^- + jv_\beta^- = A^- e^{-j\omega k T_s} \tag{4.2}$$

where, v_α^+ is the real component of the positive sequence voltage, v_β^+ is the imaginary component of the positive sequence voltage, A^+ is the amplitude of the complex space vector, ω is the angular frequency of the grid voltage, k denotes the k-th sampling instant and T_s is the sampling time. A similar naming convention is used for the negative sequence components. The modified ECKF requires the system to be described by a state transition model and a measurement model of the form:

$$x_{(k+1)} = f\left(x_{(k)}, u_{(k)}\right) + w_{(k-1)} \tag{4.3}$$

$$z_{(k)} = h\left(x_{(k)}\right) + v_{(k)} \tag{4.4}$$

where, $f\left(x_{(k)}, u_{(k)}\right)$ is a non-linear function relating the future state $x_{(k+1)}$ to the current state $x_{(k)}$ and current inputs $u_{(k)}$, and $h\left(x_{(k)} + v_{(k)}\right)$ is a non-linear function relating the current measurement $z_{(k)}$ to the current state $x_{(k)}$. Also, $w_{(k-1)}$ and $v_{(k)}$ are zero-mean Gaussian noises describing the noise in the process and measurement models, with covariance matrices D and E respectively.

To develop a state space model in the format of (4.3) and (4.4) , $x_{0(k)} = e^{j\omega T_s}$, $x_{1(k)} = A^+ e^{j\omega k T_s}$ and $x_{2(k)} = A^- e^{-j\omega k T_s}$ are selected as the state variables. At each

sampling instant, the positive sequence voltage rotates by one time step in the positive direction, whilst the negative sequence voltage rotates by one time step in the negative direction. Furthermore, it is assumed that the angular displacement from one sampling instant to the next is constant, therefore:

$$\begin{aligned} x_{(k+1)} &= f\left(x_{(k)}, u_{(k)}\right) + w_{(k-1)} \\ \begin{bmatrix} x_{0(k+1)} \\ x_{1(k+1)} \\ x_{2(k+1)} \end{bmatrix} &= \begin{bmatrix} x_{0(k)} \\ x_{0(k)}x_{1(k)} \\ \frac{x_{2(k)}}{x_{0(k)}} \end{bmatrix} + w_{(k-1)} \end{aligned} \tag{4.5}$$

Alternatively, (4.5) can be expressed in state space form as:

$$\begin{bmatrix} x_{0(k+1)} \\ x_{1(k+1)} \\ x_{2(k+1)} \end{bmatrix} = A_d \begin{bmatrix} x_{0(k)} \\ x_{1(k)} \\ x_{2(k)} \end{bmatrix} \tag{4.6}$$

where, the discrete state transition matrix is given by:

$$A_d = \begin{bmatrix} 1 & 0 & 0 \\ 0 & x_{0(k)} & 0 \\ 0 & 0 & \frac{1}{x_{0(k)}} \end{bmatrix} \tag{4.7}$$

The only quantity which can actually be measured is the grid voltage, which is the sum of the positive and negative sequence components, therefore:

$$\begin{aligned} z_{(k)} &= h\left(x_{(k)}\right) + v_{(k)} \\ z_{(k)} &= \left[x_{1(k)} + x_{2(k)}\right] + v_{(k)} \end{aligned} \tag{4.8}$$

The modified ECKF linearizes the system around the previous state estimate. This involves computing the first-order partial derivatives of the process and measurement

matrices at each time step. The Jacobians are calculated using:

$$F_{(k-1)} = \frac{\partial f}{\partial x}\Big|_{\substack{x=\hat{x}^{+}_{(k-1)} \\ u=u_{(k-1)}}} \tag{4.9}$$

$$H_{(k)} = \frac{\partial h}{\partial x}\Big|_{x=\hat{x}^{-}_{(k)}} \tag{4.10}$$

where $H_{(k)}$ is the linearized measurement matrix and $F_{(k-1)}$ is the linearized state transition matrix. Applying (4.9) and (4.10) to the state transition model (4.5) and measurement model (4.8) yields:

$$F_{(k-1)} = \begin{bmatrix} 1 & 0 & 0 \\ x_{1(k)} & x_{0(k)} & 0 \\ -\frac{x_{2(k)}}{x^2_{0(k)}} & 0 & \frac{1}{x_{0(k)}} \end{bmatrix} \tag{4.11}$$

$$H_{(k)} = \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} \tag{4.12}$$

Finally, if D is increased, $B^{-}_{(k)}$ will increase, therefore, the Kalman gain $K_{(k)}$ will increase as well. This means less emphasis is placed on the predictive model and changes in the measurements will be reflected more quickly in the estimated voltages, but more measurement noise will be observed on the estimator outputs. Similarly, if E is increased, the Kalman gain $K_{(k)}$ will decrease. Thus, more emphasis is placed on the latest measurements leading to more noise propagating through to the estimator output. However, the response to changes in the measurements will be faster. D and E are determined empirically as:

$$D = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0.01 & 0 \\ 0 & 0 & 0.01 \end{bmatrix} \tag{4.13}$$

$$E = \begin{bmatrix} 5 + j5 \end{bmatrix} \tag{4.14}$$

The modified ECKF can then be implemented using the following equations for the prediction stage:

$$\hat{x}^{-}_{(k)} = f\left(\hat{x}^{+}_{(k-1)}, u_{(k-1)}\right) \tag{4.15}$$

$$B^{-}_{(k)} = F_{(k-1)} B^{+}_{(k-1)} F^{T}_{(k-1)} + D \tag{4.16}$$

where $\hat{x}^{-}_{(k)}$ is the uncorrected state estimate, $f\left(\hat{x}^{+}_{(k-1)}, u_{(k-1)}\right)$ is the non-linear system model, $B^{-}_{(k)}$ is the uncorrected state error covariance matrix and $B^{+}_{(k-1)}$ is the corrected state error covariance matrix. At every iteration, the uncorrected state updates are corrected using the latest measurements. The update stage uses the following equations:

$$\tilde{y}_{(k)} = z_{(k)} - h\left(\hat{x}^{-}_{(k)}\right) \tag{4.17}$$

$$K_{(k)} = B^{-}_{(k)} H^{T}_{(k)} \left(E + H_{(k)} B^{-}_{(k)} H^{T}_{(k)}\right)^{-1} \tag{4.18}$$

$$\hat{x}^{+}_{(k)} = \hat{x}^{-}_{(k)} + K_{(k)} \tilde{y}_{(k)} \tag{4.19}$$

$$B^{+}_{(k)} = \left(I - K_{(k)} H_{(k)} B^{-}_{(k)}\right) \tag{4.20}$$

where $K_{(k)}$ is the Kalman gain.

4.2.1 Proposed Modification

If the system is sampled at instant k, by the time when the necessary calculations have been performed, the control decision may be out of date when it is applied. To compensate for this, the controller may extrapolate future quantities and instead solve for the optimum control action to be applied at instant $k+1$ to minimize the cost function at $k+2$. A modification to the ECKF is proposed to also estimate the grid voltage at instants $k+1$ and $k+2$. The change in the state variables over time is described by (4.6). Since the system state at instant k has already been estimated, (4.6) can be used to advance the estimates by one time step as follows:

$$\hat{X}^{+}_{(k+1)} = A_d \hat{X}^{+}_{(k)} \tag{4.21}$$

Similarly, advancing (4.6) by one time step and substituting for (4.21) gives:

$$\hat{X}^{+}_{(k+2)} = A_d \hat{X}^{+}_{(k+1)} = A_d^2 \hat{X}^{+}_{(k)} \tag{4.22}$$

Since the new equations calculate the grid voltage two steps in advance, the current references can be calculated directly for instant k+2. This removes the need to extrapolate the current references, further improving the noise rejection of the controller. Furthermore, the estimated future grid voltages are used in the grid voltage discretization technique.

4.3 Proposed Control System

A complete MPC system is proposed to regulate the active and reactive power exchanged between a grid-connected converter and an unbalanced grid. The system diagram is shown in Figure 4.1.

4.3.1 Current Reference Generation

To export the required active and reactive power into the grid, the reference currents must be calculated as a function of the grid voltage as described in [267]. The modified ECKF estimates the grid voltage at instant $k + 2$, therefore, the current references may be calculated directly for instant $k + 2$. The references are calculated to prevent

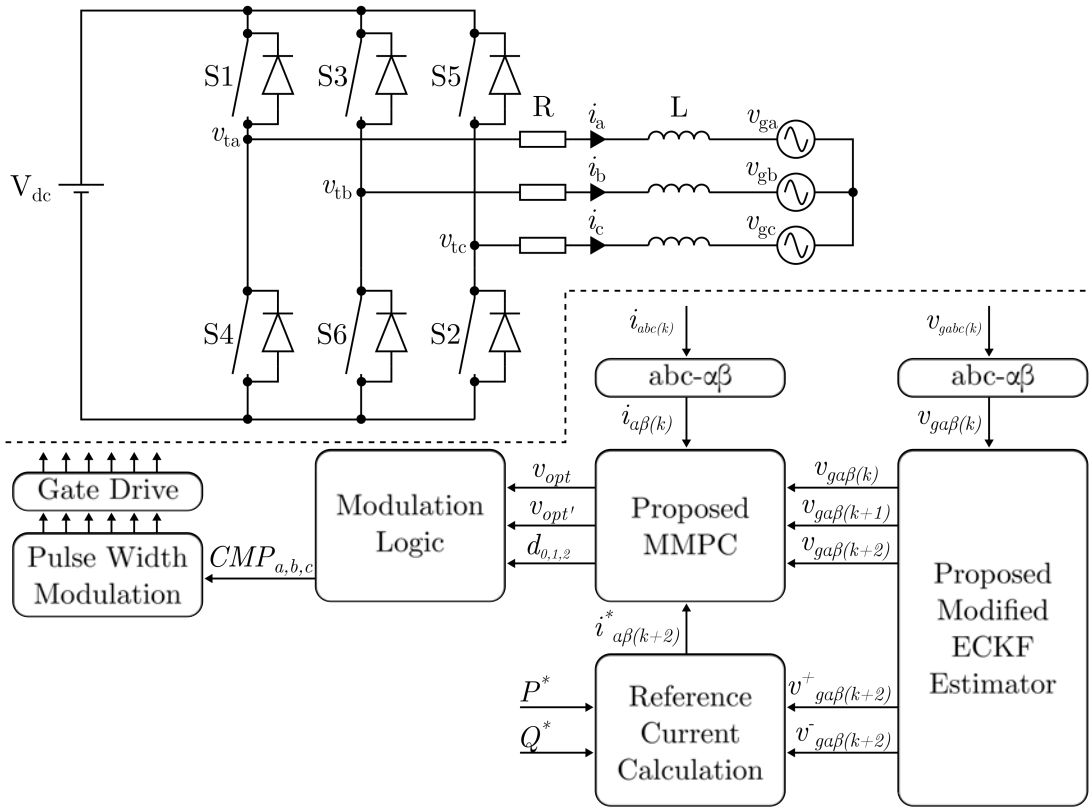


Figure 4.1: The complete MPC control system.

oscillation of the active power as follows:

$$i^{*+}_{\alpha(k+2)} = \frac{P^* v^+_{g\alpha(k+2)}}{A} + \frac{Q^* v^+_{g\beta(k+2)}}{B} \tag{4.23}$$

$$i^{*+}_{\beta(k+2)} = \frac{P^* v^+_{g\beta(k+2)}}{A} - \frac{Q^* v^+_{g\beta(k+2)}}{A} \tag{4.24}$$

$$i^{*-}_{\alpha(k+2)} = -\frac{P^* v^-_{g\alpha(k+2)}}{A} + \frac{Q^* v^-_{g\beta(k+2)}}{A} \tag{4.25}$$

$$i^{*-}_{\beta(k+2)} = -\frac{P^* v^-_{g\beta(k+2)}}{A} - \frac{Q^* v^-_{g\alpha(k+2)}}{A} \tag{4.26}$$

$$\begin{aligned} where \;\; A &= \left[\left(v^+_{g\alpha(k+2)}\right)^2 + \left(v^+_{g\beta(k+2)}\right)^2\right] \\ &\quad - \left[\left(v^-_{g\alpha(k+2)}\right)^2 + \left(v^-_{g\beta(k+2)}\right)^2\right] \\ B &= \left[\left(v^+_{g\alpha(k+2)}\right)^2 + \left(v^+_{g\beta(k+2)}\right)^2\right] \\ &\quad + \left[\left(v^-_{g\alpha(k+2)}\right)^2 + \left(v^-_{g\beta(k+2)}\right)^2\right] \end{aligned}$$

where, $v^{+}_{g\alpha(k+2)}$ and $v^{+}_{g\beta(k+2)}$ are the positive sequence components of the grid voltage at instant $k+2$, $v^{-}_{g\alpha(k+2)}$ and $v^{-}_{g\beta(k+2)}$ are the negative sequence components of the grid voltage at instant $k+2$ and P^* and Q^* are the active and reactive power references respectively.

4.4 Stability Analysis

It is essential that the converter output current tracks the reference, therefore, the predictive control equations should be designed such that the current tracking error converges to zero. In order to prove the theoretical stability of the proposed nonlinear system in the surroundings of the steady-state, Lyapunov stability theory is used. Let there be some error between the actual grid voltage $v^{*}_{g\alpha(k)}$ and the voltage estimated by the modified ECKF $v^{e}_{g\alpha(k)}$. Similarly, let there be an error between the ideal terminal voltage which would lead to zero error, $v^{*}_{t\alpha(k)}$, and the actual terminal voltage of the converter $v_{t\alpha(k)}$. Therefore:

$$v^{*}_{g\alpha(k)} = v^{e}_{g\alpha(k)} + \lambda_{(k)} \tag{4.27}$$

$$v_{t\alpha(k)} = v^{*}_{t\alpha(k)} + \eta_{(k)} \tag{4.28}$$

where $\lambda_{(k)}$ is the grid voltage estimation error that satisfies $\|\lambda_{(k)}\| \leq \varphi$ with a constant $\varphi > 0$ and $\eta_{(k)}$ is the terminal voltage error that satisfies $\|\eta_{(k)}\| \leq \psi$ with a constant $\psi > 0$. According to (3.36), the future grid current is given by:

$$\begin{aligned} i_{\alpha(k+1)} = &\left(1 - R\frac{T_s}{L}\right) i_{\alpha(k)} \\ &+ \frac{T_s}{L}\left(v_{t\alpha(k)} - \frac{1}{2}\left(v^{e}_{g\alpha(k)} + v^{e}_{g\alpha(k+1)}\right)\right) \end{aligned} \tag{4.29}$$

where $v_{t\alpha(k)}$ is the actual terminal voltage of the converter and the 'e' superscript denotes that these grid voltage values were estimated by the modified ECKF. Similarly, in an ideal scenario, the current reference would be tracked with zero steady-state error,

therefore, the following equation can also be stated:

$$i^*_{\alpha(k+1)} = \left(1 - R\frac{T_s}{L}\right) i_{\alpha(k)} + \frac{T_s}{L}\left(v^*_{t\alpha(k)} - \frac{1}{2}\left(v^*_{g\alpha(k)} + v^*_{g\alpha(k+1)}\right)\right) \tag{4.30}$$

where $v^*_{t\alpha(k)}$ is the ideal converter terminal voltage to achieve zero error and $v^*_{g\alpha(k)}$ and $v^*_{g\alpha(k+1)}$ are the actual grid voltages. The current tracking error can be calculated as follows:

$$\Delta i_{(k+1)} = i_{\alpha(k+1)} - i^*_{\alpha(k+1)} \tag{4.31}$$

Substituting for the actual current given by (4.29) and the ideal current given by (4.30) yields:

$$\begin{aligned}\Delta i_{(k+1)} = &\left[\left(1 - R\frac{T_s}{L}\right) i_{\alpha(k)} \right.\\ &\left. + \frac{T_s}{L}\left(v_{t\alpha(k)} - \frac{1}{2}\left(v^e_{g\alpha(k)} + v^e_{g\alpha(k+1)}\right)\right)\right] - \\ &\left[\left(1 - R\frac{T_s}{L}\right) i_{\alpha(k)} \right.\\ &\left. + \frac{T_s}{L}\left(v^*_{t\alpha(k)} - \frac{1}{2}\left(v^*_{g\alpha(k)} + v^*_{g\alpha(k+1)}\right)\right)\right]\end{aligned} \tag{4.32}$$

Assuming that $v^*_{g\alpha(k+1)} \approx v^*_{g\alpha(k)}$ and $v^e_{g\alpha(k+1)} \approx v^e_{g\alpha(k)}$, the future current error can be restated as:

$$\begin{aligned}\Delta i_{(k+1)} &= \frac{T_s}{L}\left[\left(v_{t\alpha(k)} - v^*_{t\alpha(k)}\right) + \left(v^*_{g\alpha(k)} - v^e_{g\alpha(k)}\right)\right] \\ &= \frac{T_s}{L}\left[\eta + \lambda\right]\end{aligned} \tag{4.33}$$

According to [268], a control Lyapunov function must satisfy the following stability criteria:

$$V(\Delta i_{(k)}) \geq a_1 \left|\Delta i_{(k)}\right|^l, \forall \Delta i_{(k)} \in G \tag{4.34}$$

$$V(\Delta i_{(k)}) \leq a_2 \left|\Delta i_{(k)}\right|^l, \forall \Delta i_{(k)} \in \Gamma \tag{4.35}$$

$$V(\Delta i_{(k+1)}) - V(\Delta i_{(k)}) < -a_3 \left|\Delta i_{(k)}\right|^l + a_4 \tag{4.36}$$

where a_1, a_2, a_3 and a_4 are positive constants, $l \geq 1$, $G \subseteq R^n$ is a positive control invariant set and $\Gamma \subset G$ is a compact set. A Lyapunov function is proposed as:

$$V_{(k)} = \frac{1}{2} \Delta i_{(k)}^T \Delta i_{(k)} \tag{4.37}$$

The change of the Lyapunov function is given by:

$$\Delta V_{(k)} = V_{(k+1)} - V_{(k)} \tag{4.38}$$

By substituting for (4.33) and (4.37), the change in the Lyapunov can be expressed as:

$$\begin{aligned} \Delta V_{(k)} = \frac{1}{2} \Bigg(\frac{T_s}{L} \Big[\Big(v_{t\alpha(k)} - v^*_{t\alpha(k)} \Big) \\ + \Big(v^*_{g\alpha(k)} - v^e_{g\alpha(k)} \Big) \Big] \Bigg)^T \Bigg(\frac{T_s}{L} \Big[\Big(v_{t\alpha(k)} - v^*_{t\alpha(k)} \Big) \\ + \Big(v^*_{g\alpha(k)} - v^e_{g\alpha(k)} \Big) \Big] \Bigg) - \frac{1}{2} \Delta i_{(k)}^T \Delta i_{(k)} \end{aligned} \tag{4.39}$$

The voltage vector $v_{t\alpha(k)}$ is bounded by the available DC link voltage. The current $i_{\alpha(k)}$ and voltage $v_{g\alpha(k)}$ are also bounded, therefore, $v^*_{t\alpha(k)}$ is bounded. By substituting for (4.27) and (4.28), the following is obtained:

$$\Delta V_{(k)} \leq -\frac{1}{2} \Delta i_{(k)}^T \Delta i_{(k)} + \frac{1}{2} \left(\frac{T_s}{L} \right)^2 (\lambda + \eta)^2 \tag{4.40}$$

Therefore, the stability conditions set out in (4.34)-(4.36) are satisfied by the following constants:

$$a_1 = 1, a_2 = 1, a_3 = \frac{1}{2}, a_4 = \left(\frac{T_s}{L}\right)^2 (\lambda + \eta)^2 \tag{4.41}$$

This implies that the system is stable in the sense of Lyapunov and that the currrent control error converges to a compact set as:

$$\upsilon = \left\{ \Delta i \| \|\Delta i\| \leq \left(\frac{T_s}{L}\right) (\lambda + \eta) \right\} \tag{4.42}$$

4.5 Simulation Results

The effectiveness of the proposed control system is studied using Matlab/Simulink simulations with the parameters shown in Table 4.1. A MPC current controller enhanced with virtual vectors called floating virtual voltage vector model predictive control (FVVV-MPC) was recently proposed in [234] and is used as a reference for comparison. Also, an improved model predictive current control (IMPCC) for unbalanced grids was recently proposed in [137] and is also included for comparison. Since the proposed method applies three vectors per sampling period while the IMPCC applies only one, the sampling frequency for the IMPCC is set two times higher to achieve the same switching frequency at best effort. This is consistent with the approach taken in [219], where the finite control set model predictive control (FCS-MPC) is sampled twice as fast as the modulated model predictive control (MMPC). The modified ECKF estimator is examined first, then the effectiveness of the complete control system is studied.

4.5.1 The Modified Extended Complex Kalman Filter Results

The effectiveness of the modified ECKF estimator is studied using a range of balanced and unbalanced voltage measurements corrupted by random noise. The output of the modified ECKF estimator is shown in Figure 4.2. The same simulation is run 100 times with random noise and the results are plotted on top of each other to validate

Table 4.1: Simulation Parameters for the proposed MMPC, FVVV-MPC and IMPCC.

Parameter	Symbol	Value	Unit
Nominal Grid Phase Voltage RMS	V_g	100	V
Grid Fundamental Frequency	f_{grid}	50	Hz
Switching Frequency (MMPC and FVVV-MPC)	f_{sw}	10	kHz
Sampling Frequency (IMPCC)	f_s	20	kHz
Voltage Measurement Noise Variance	σ_v^2	1	V
DC Link Voltage	V_{dc}	400	V
Filter Inductance	L	10	mH
Filter Resistance	R	0.1	Ω
Rated Power	P_{rated}	2	kW
Rated Current (Peak)	i_{rated}	9.428	A

the stability of the estimator in a range of random scenarios. In Figure 4.2a, the input voltage waveform is shown. In Figure 4.2b and Figure 4.2c, the estimated positive and negative sequence components are shown, with the results of the 100 Monte Carlo runs superimposed. The input voltage signals are initially balanced, and the system is in steady-state. At t = 25 ms, the magnitude of phase 'a' is increased by 30%, while phase 'b' remains constant and phase 'c' is given by $-v_{ga(k)} - v_{gb(k)}$ in a three-wire system. At t = 75 ms, the input voltages return to a balanced state. At t = 125 ms, the magnitude of phase 'a' is reduced by 30% whilst phase 'b' remains constant. Finally, at t = 175 ms, the input voltages return to a balanced state. The stability of the modified ECKF estimator is clearly demonstrated in Figure 4.2b and Figure 4.2c, where the estimator produces a stable estimate of the positive and negative sequence components for all 100 runs. The estimator responds to step change in voltage immediately and the estimated positive sequence component settles to a new steady-state in less than 2 ms. This compares favorably with conventional delayed signal techniques which do not respond correctly for one quarter-period of the input waveform.

The superior noise rejection capability of the modified ECKF estimator is shown in Figure 4.3, where an input voltage waveform is shown, together with the voltages estimated for instant $k + 1$ and $k + 2$, as well as the current reference for instant $k + 2$. The left column of plots shows the modified ECKF, whilst the right column shows a conventional delayed signal cancellation technique. As shown in Figure 4.3, the

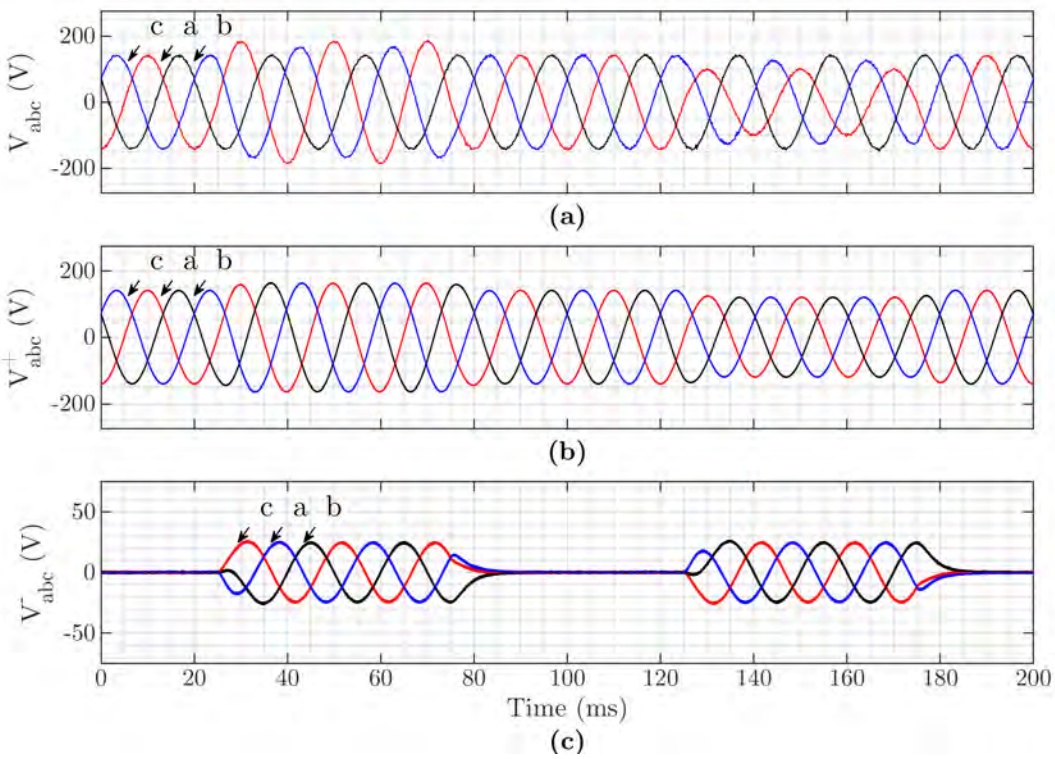


Figure 4.2: Simulation results for the modified ECKF estimator: (a) input voltage waveform corrupted by noise (b) estimated positive sequence component and (c) estimated negative sequence component.

modified ECKF estimator exhibits superior noise rejection and produces more accurate estimates of the phase voltages and, as a result, less noisy current reference signals. The vulnerability of the delayed signal technique to noise is clearly demonstrated. As shown in Figure 4.3c and Figure 4.3e, the ECKF produces smooth estimates of the grid voltage components even where there is noise on the input signal, while the delayed signal and Lagrange method shown in Figure 4.3d and Figure 4.3f amplifies this noise. Furthermore, Figure 4.3g and Figure 4.3h show that the ECKF produces a smooth current reference, while the conventional delayed signal technique produces large a noisy reference signal.

Another limitation of the conventional Lagrange delay compensation technique is its behaviour during transient conditions. Since the delayed signal technique uses stored values from previous iterations, it exhibits undefined behaviour during step changes in references. Figure 4.4 shows an input voltage waveform during a voltage step change,

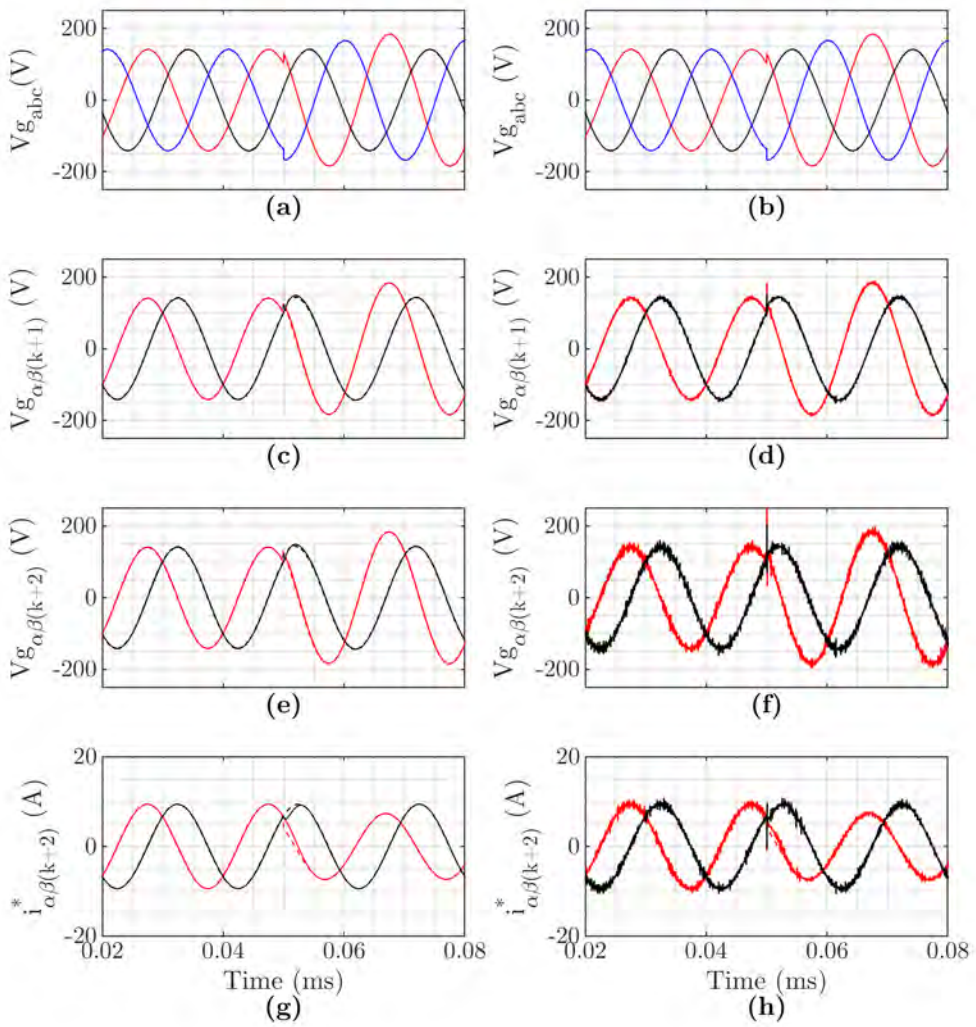


Figure 4.3: Comparison between ECKF estimator and the delayed signal cancellation and Lagrange method highlighting the noise rejection properties: (a) the measured grid voltage for the ECKF (b) the measured grid voltage for the conventional delayed signal/Lagrange method (c) the grid voltage in the $\alpha\beta$-frame at instant $k+1$ for the ECKF (d) the grid voltage in the $\alpha\beta$-frame at $k+1$ for the conventional delayed signal/Lagrange method (e) the grid voltage in the $\alpha\beta$-frame at $k+2$ for the ECKF (f) the grid voltage in the $\alpha\beta$-frame at $k+2$ for the conventional delayed signal/Lagrange method (g) the current reference in the $\alpha\beta$-frame at $k+2$ for the ECKF (h) the current reference in the $\alpha\beta$-frame at $k+2$ for the conventional delayed signal/Lagrange method.

together with the voltages estimated for instant $k+1$ and $k+2$, as well as the current reference for instant $k+2$. The left column of plots shows the modified ECKF, whilst

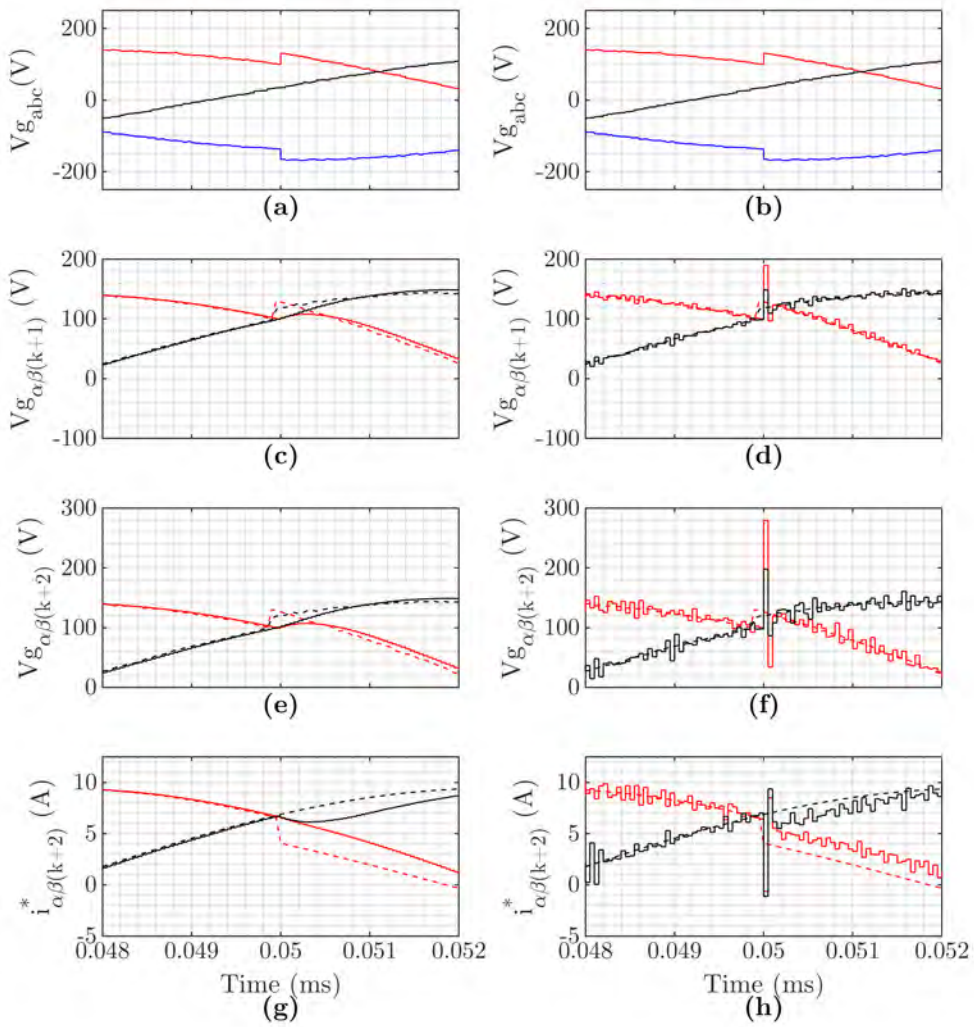


Figure 4.4: Zoomed comparison between ECKF estimator and the delayed signal cancellation and Lagrange method highlighting spikes during changing conditions: (a) the measured grid voltage for the ECKF (b) the measured grid voltage for the conventional delayed signal/Lagrange method (c) the grid voltage in the $\alpha\beta$-frame at instant $k+1$ for the ECKF (d) the grid voltage in the $\alpha\beta$-frame at $k+1$ for the conventional delayed signal/Lagrange method (e) the grid voltage in the $\alpha\beta$-frame at $k+2$ for the ECKF (f) the grid voltage in the $\alpha\beta$-frame at $k+2$ for the conventional delayed signal/Lagrange method (g) the current reference in the $\alpha\beta$-frame at $k+2$ for the ECKF (h) the current reference in the $\alpha\beta$-frame at $k+2$ for the conventional delayed signal/Lagrange method.

the right column shows a conventional delayed signal cancellation technique. Again, the superiority of the proposed ECKF estiamtor technique is clearly demonstrated. As

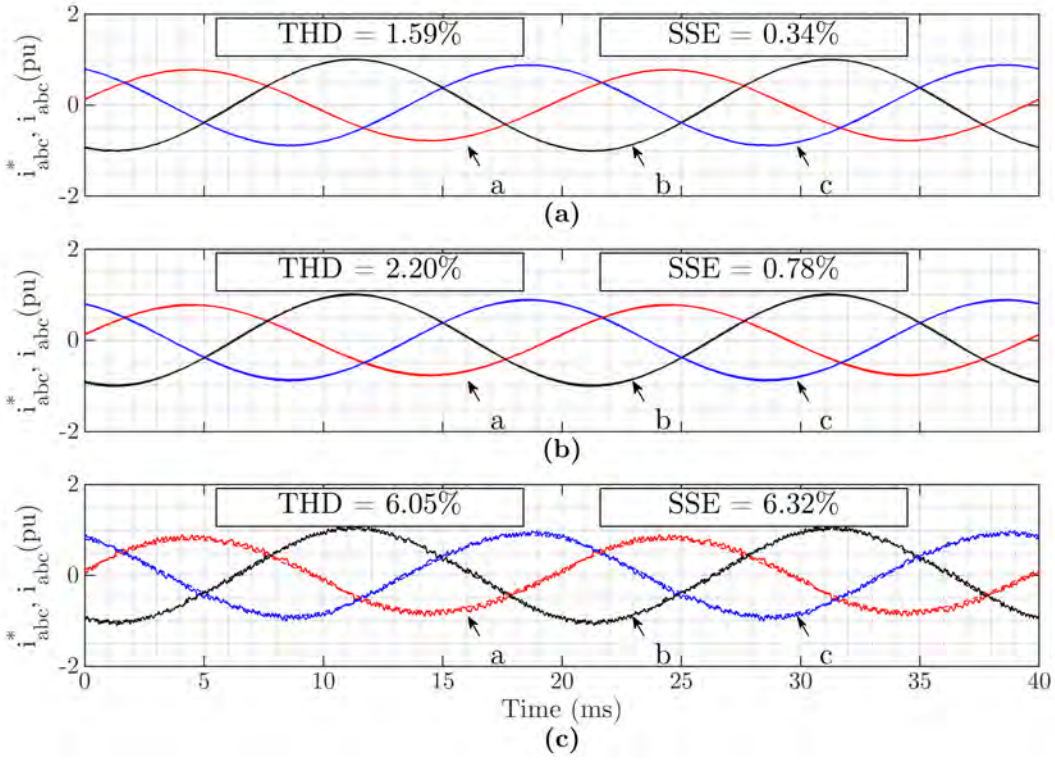


Figure 4.5: Current tracking performance: (a) proposed MMPC (b) conventional FVVV-MPC and (c) conventional IMPCC.

shown in Figure 4.4c and Figure 4.4e, the ECKF produces smooth estimates of the grid voltage components during the step change, while the delayed signal and Lagrange method shown in Figure 4.4d and Figure 4.4f introduces unwanted spikes. Furthermore, Figure 4.4g and Figure 4.4h show that the ECKF produces a smooth current reference, while the conventional delayed signal technique introduces large spikes in the reference signal.

4.5.2 Proposed Control System

The steady-state current tracking under unbalanced conditions is studied in Figure 4.5. The magnitude of phase 'a' is 30% greater than phase 'b', while phase 'c' is given by $-v_{ga(k)} - v_{gb(k)}$. Figure 4.5 shows the grid current from the proposed MMPC, the conventional FVVV-MPC and the conventional IMPCC. It can be clearly seen that the current quality is improved for the proposed MMPC, and the steady-state error is lower

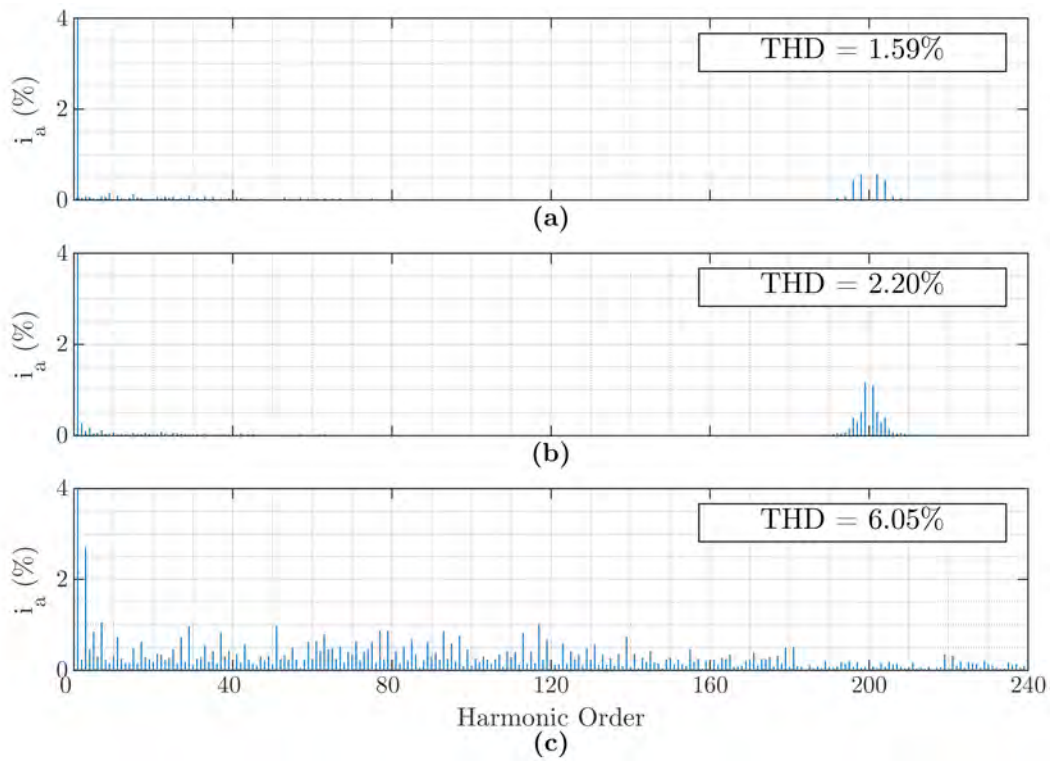


Figure 4.6: Current harmonic spectrum: (a) proposed MMPC (b) conventional FVVV-MPC and (c) conventional IMPCC.

than both the FVVV-MPC and the IMPCC. The harmonic spectrum of the output current is studied in Figure 4.6. As expected, the harmonics for the proposed MMPC and the conventional FVVV-MPC are centered around the switching frequency, while for the conventional IMPCC, there is a spread spectrum of harmonic content. The THD for the proposed controller is 1.59% whilst for the FVVV-MPC it is 2.20% and for the IMPCC controller it is 6.05%, therefore, a significant improvement in power quality has been achieved. The transient performance of the current controller is also studied during a step change in active power reference from zero to rated power at unity power factor. Figure 4.7 shows the active and reactive power of all three controllers during the step change. The IMPCC benefits from a higher sampling frequency, however, the proposed MMPC benefits from over-modulation capability, therefore the proposed controller offers comparable transient performance to the conventional IMPCC. The FVVV-MPC does not benefit from the increased sampling frequency of the IMPCC

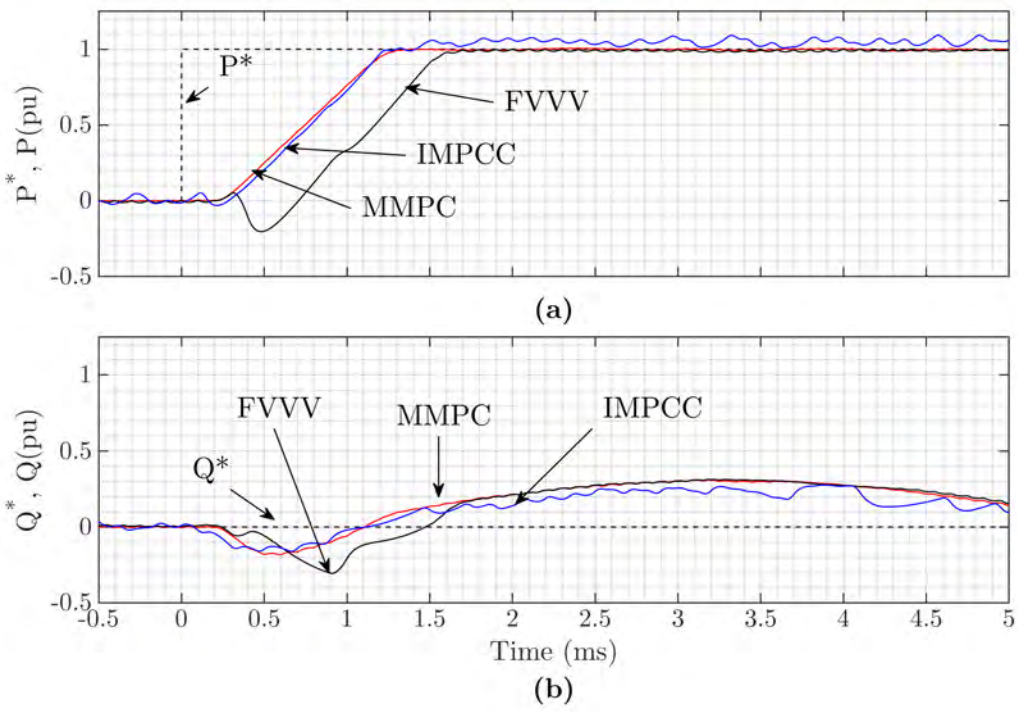


Figure 4.7: Dynamic active and reactive power tracking for the proposed MMPC, conventional FVVV-MPC and conventional IMPCC: (a) active power and (b) reactive power.

Table 4.2: Comparison of controllers studied.

Parameter	Proposed MMPC	FVVV-MPC [234]	IMPCC [137]
THD	Lowest	Low	High
SSE	Lowest	Low	High
Transient Response	Fast	Slow	Fast
Power Ripple	Lowest	Low	High

nor the overmodulation capability of the proposed MMPC, therefore, its transient performance is slower. The proposed MMPC with its improved current quality offers the lowest power ripple. The advantages and disadvantages of the proposed MMPC, conventional FVVV-MPC and conventional IMPCC are summarised in Table 4.2.

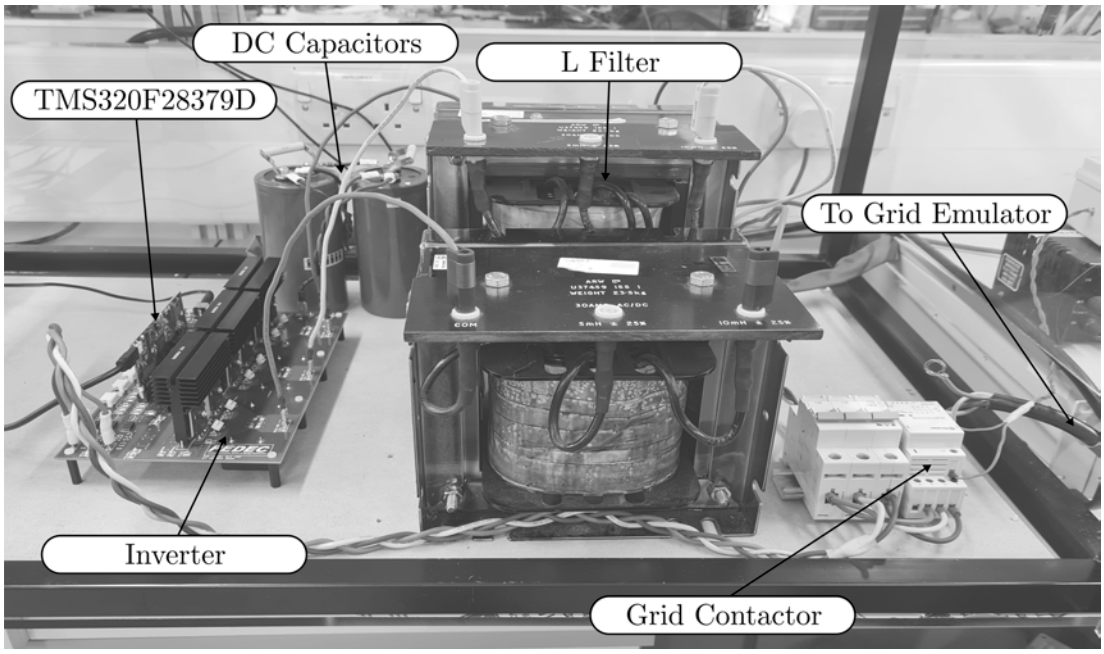
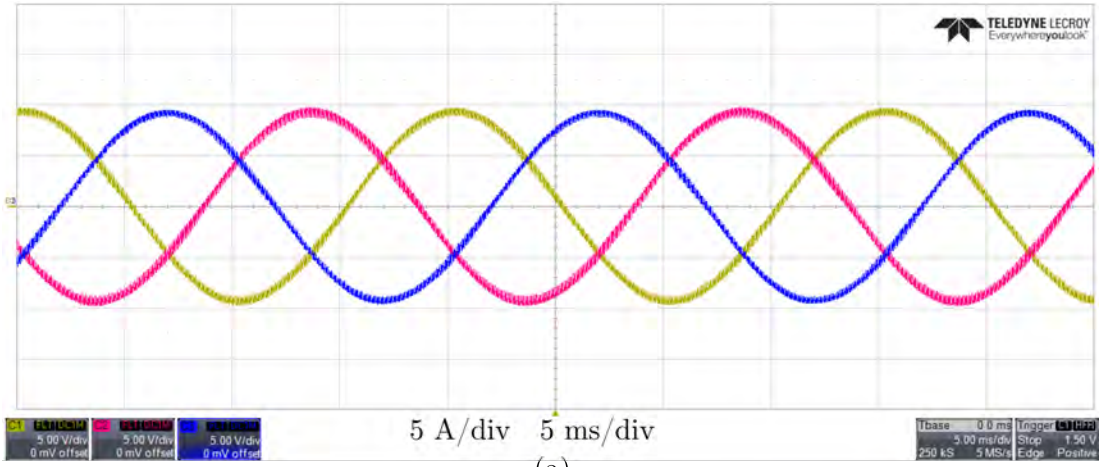


Figure 4.8: The hardware test rig.

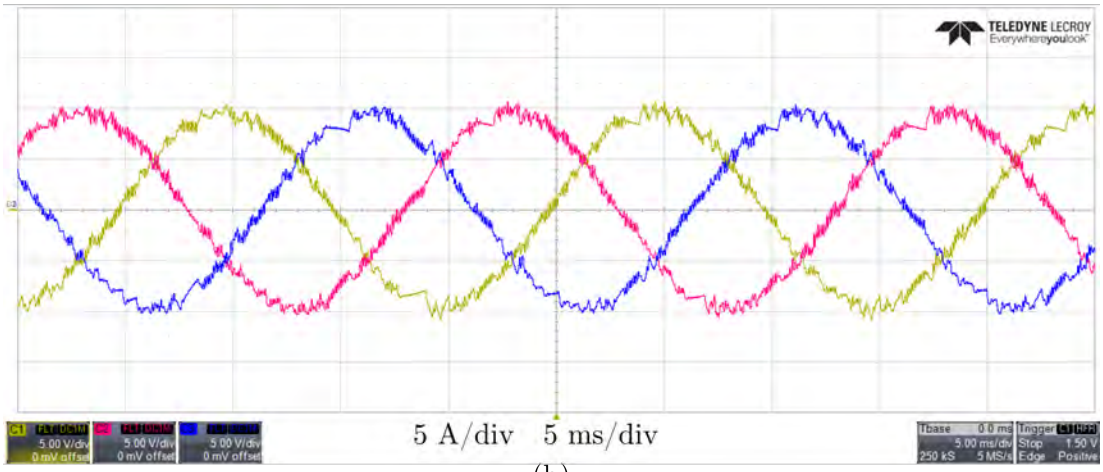
4.6 Experimental Validation

The proposed MMPC was implemented in the laboratory to verify the performance of the complete control system. Since conventional FCS-MPC is more prevalent in the literature than virtual-vector based MPC due to its faster response, the IMPCC was selected for comparison in the experiments. The experimental test rig is shown in Figure 4.8 and the system parameters are as shown in Table 4.1. The steady-state current under balanced conditions is studied in Figure 4.9, while the steady-state current under unbalanced conditions is studied in Figure 4.10, where the magnitude of phase voltage 'a' is 30% greater than phase 'b', while phase 'c' is given by $-v_{ga(k)}-v_{gb(k)}$.

Figure 4.9 and Figure 4.10 show the experimental results for the proposed MMPC and the IMPCC under both balanced and unbalanced conditions. In both cases, the current quality is improved for the proposed MMPC compared with the IMPCC technique. The harmonic spectrum of the experimental output currents under unbalanced conditions is shown in Figure 4.11. The harmonics for the proposed MMPC are centered around the switching frequency, while for the conventional IMPCC, there is a spread spectrum



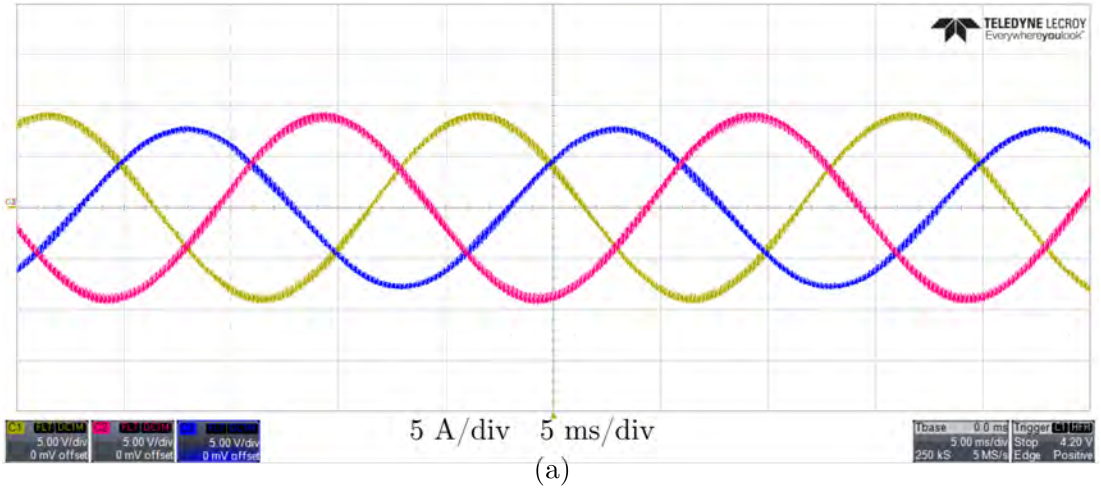
(a)



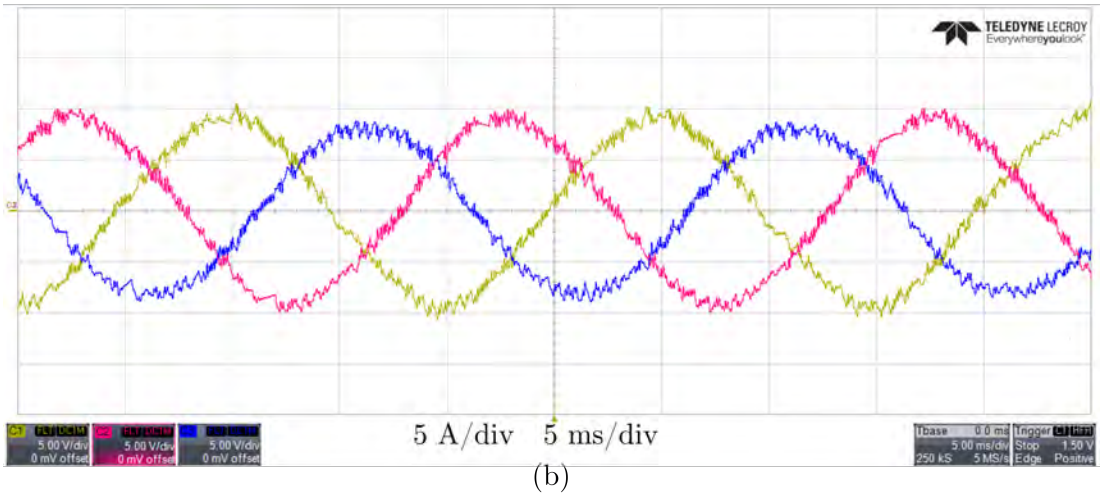
(b)

Figure 4.9: Current under balanced conditions: (a) proposed MMPC and (b) conventional IMPCC.

of harmonic content. The THD for the proposed controller is 2.47% whilst for the conventional controller it is 5.4%. This is close to the the simulation result. Next, the effectiveness of the proposed controller in compensating for unbalanced grid voltages was examined. Figure 4.12 shows the outputs of the proposed controller in a range of balanced and unbalanced scenarios, with and without negative sequence voltage compensation. Figure 4.12a shows the calculated active and reactive power at full rated power in a balanced grid, with currents as shown in Figure 4.12b. Figure 4.12c shows the calculated powers where the phase 'a' voltage is increased by 30% and the negative sequence voltage is not compensated. The resulting balanced currents are shown in



(a)



(b)

Figure 4.10: Current under unbalanced conditions: (a) proposed MMPC and (b) conventional IMPCC.

Figure 4.12d. Finally, Figure 4.12e shows the calculated powers where the phase 'a' voltage is increased by 30% and the negative sequence component is compensated by the modified ECKF estimator. The resulting unbalanced currents are shown in Figure 4.12f. The effectiveness of the proposed controller is clearly demonstrated. Near zero steady-state error is achieved under balanced and unbalanced operation and constant active power is exported to the grid with high power quality.

The transient power tracking performance of both current controllers is also studied in experiment during a step change in active power reference from zero to rated power at unity power factor. Figure 4.13 shows the active and reactive power of both

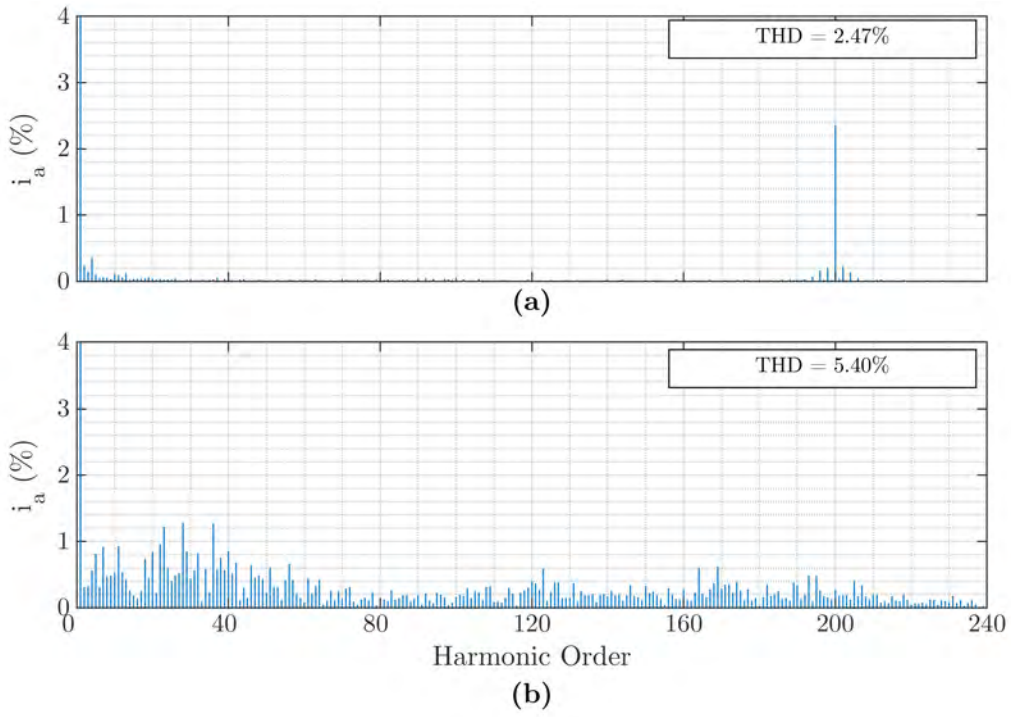


Figure 4.11: Experimental current harmonic spectrum: (a) proposed MMPC and (b) conventional IMPCC.

controllers during the step change. Both controllers have similar responses, however, the proposed MMPC has superior steady-state performance, with reduced ripple in the active power. The output currents of both controllers during the step change from zero to rated power at unity power factor are shown in Figure 4.14. Both controllers track the reference quickly, achieving a steady-state in 2.5 ms, however, the proposed MMPC achieves a higher current quality, as shown in Figure 4.14a. Figure 4.15 shows the phase 'a' currents compared with their reference during the step change. It can be seen from Figure 4.15 that the proposed MMPC has comparable transient performance to the conventional IMPCC, however, the current ripple is reduced and the power quality is improved.

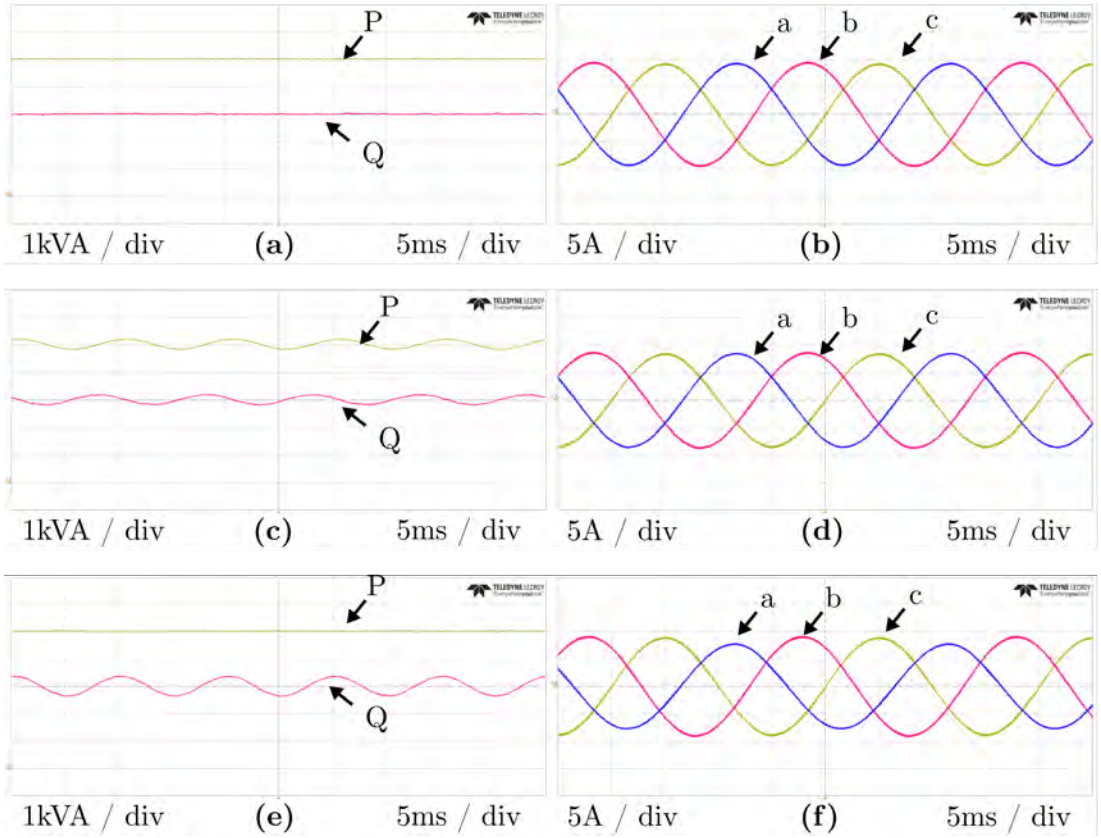


Figure 4.12: Experimental results for the proposed controller: (a) PQ in balanced grid (b) currents in balanced grid (c) PQ in unbalanced grid without compensation (d) currents in unbalanced grid without compensation (e) PQ in unbalanced grid with compensation (f) currents in unbalanced grid with compensation.

4.7 Computational Burden

The MMPC controller proposed in this paper and the conventional IMPCC were implemented in the laboratory using a Texas Instruments TMS320F28379D microcontroller. At the start of the sampling period, a microcontroller pin is set high and at the end of the current control algorithm the pin is set low. The actual calculation time is then measured using an oscilloscope. For the chosen switching frequency of 10 kHz, the sampling period is 100 μ. The execution times for the two techniques are shown in Figure 4.16. The execution time of the proposed controller is 12.5 μs, while the execution time of the conventional IMPCC controller is 13 μs. To achieve a minimum switching frequency of 10 kHz, the IMPCC must be executed twice per switching period, mean-

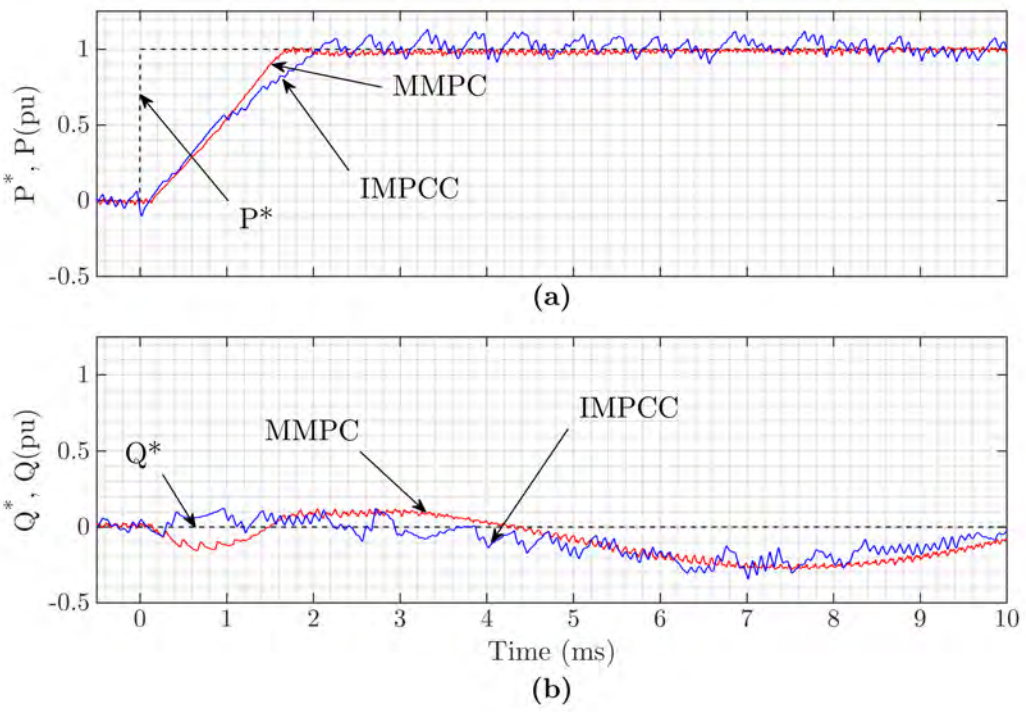
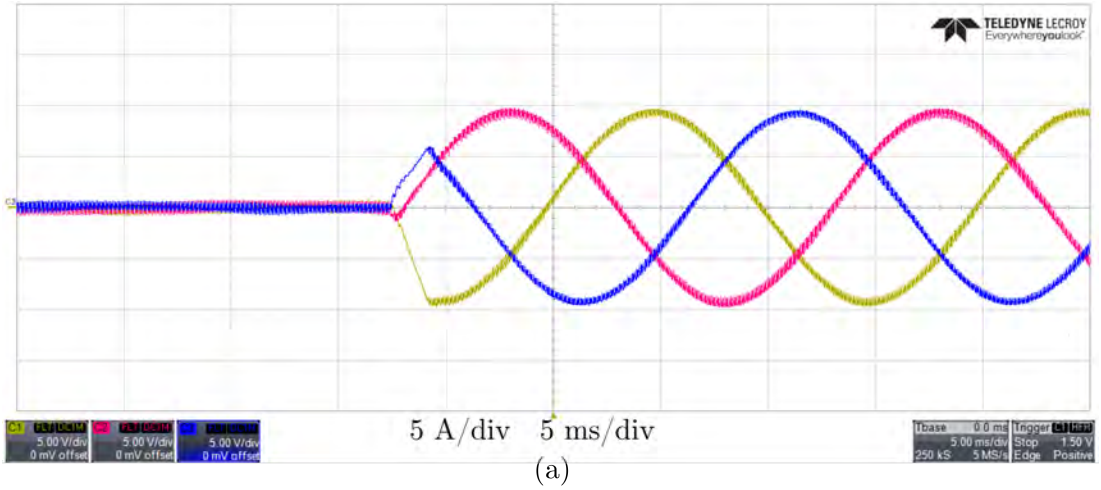


Figure 4.13: Dynamic active and reactive power tracking: (a) the active power (b) the reactive power.

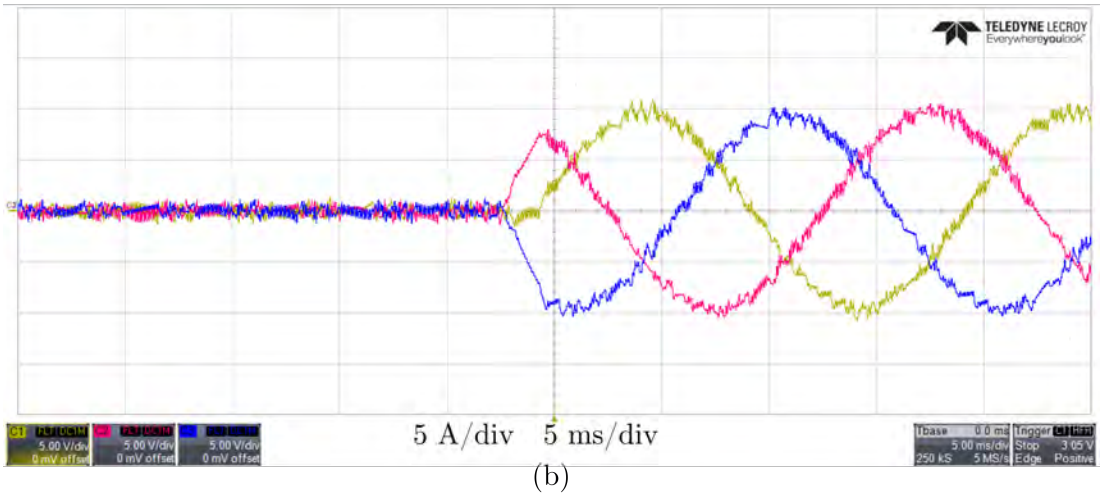
ing that only 37 μs is available to include any extra control algorithms to achieve the minimum switching frequency of 10 kHz. In comparison, the proposed MMPC offers 87.5 μs of additional time. In summary, the proposed MMPC has twice the available extra program execution time compared with the conventional IMPCC to achieve the same switching frequency. For example, if it is required to design a converter with higher switching frequency, such as 40 kHz, then the proposed MMPC can be used but the conventional IMPCC cannot.

4.8 Summary

In this chapter, a new model predictive current controller has been proposed for unbalanced grids. By utilising the improved MMPC proposed in chapter 3, the variable switching frequency problem of conventional MPC has been addressed in a computationally efficient way. The ECKF estimator which has been proposed previously for



(a)



(b)

Figure 4.14: Three phase currents during step change from zero to full rated power: (a) proposed MMPC and (b) conventional IMPCC.

protection purposes is also extended to the new application of current control and its suitability for this purpose has been proven. The ECKF has also been modified to provide a new calculation time compensation technique offering superior accuracy to the well-known Lagrange technique. The proposed controller has been studied in simulation and validated experimentally. Simulation and practical results have confirmed the excellent performance of the system compared with existing approaches. Low steady-state error and high power quality are achieved and a fast transient response is provided.

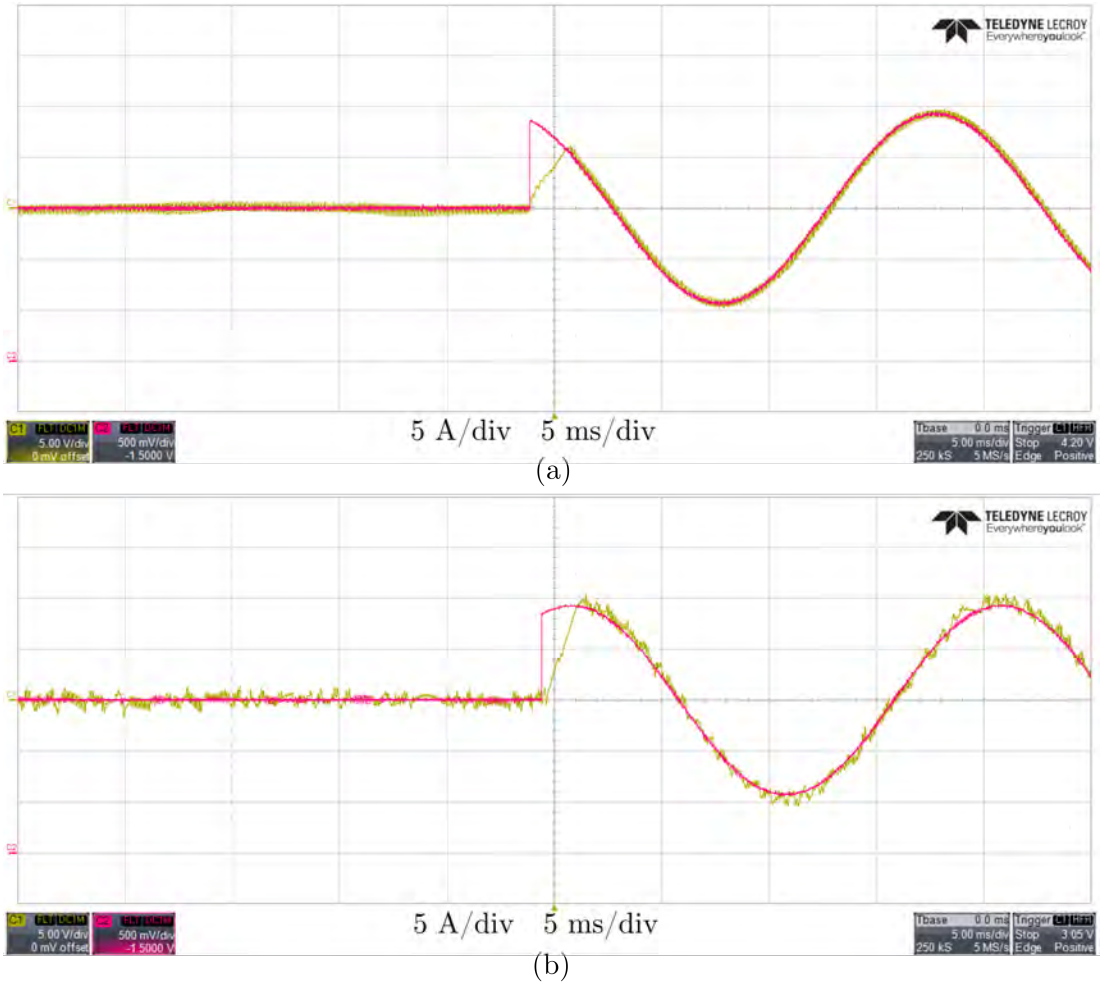
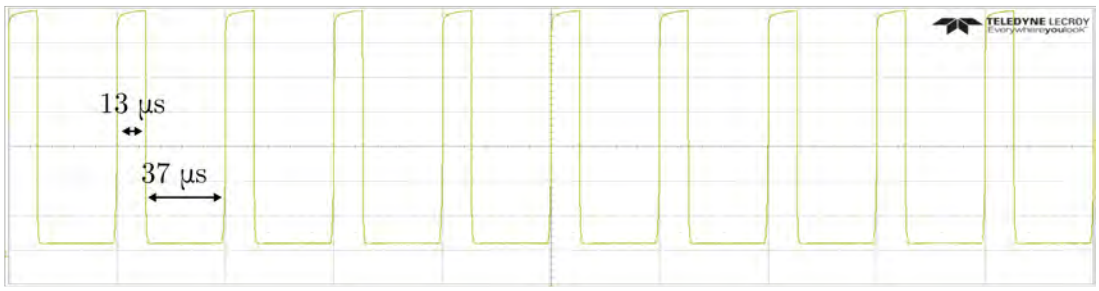


Figure 4.15: Phase 'a' current and reference superimposed during step change from zero to full rated power: (a) proposed MMPC and (b) conventional IMPCC.

500 mV / div **(a)** 50µs / div



500 mV / div **(b)** 50µs / div

Figure 4.16: Execution time: (a) the proposed controller and (b) the existing IMPCC controller.

Chapter 5

Development of a Hardware Prototype and Supporting Software

The purpose of this chapter is to describe the flexible power electronic converter constructed to validate the control algorithms proposed in this thesis, together with the software written to implement the proposed controllers. The chapter is divided into two main sections. The hardware design is discussed first. The motivation for the build is outlined, then the specific design objectives are listed and the main design decisions discussed. Technical schematics for the final design are included in Appendix A. The software design is discussed second. The specific design objectives are listed and a few key implementation issues are discussed.

5.1 The Proposed Converter Hardware

5.1.1 Key Design Decisions

A comprehensive discussion of every component selected for inclusion in the converter design is beyond the scope of this thesis. However, a few crucial decisions taken during the design are discussed in the following sections.

a. User Safety

Safety is of paramount importance in constructing any electrical system, and careful regard must be had for the benefits of testing at realistic power levels versus the dangers of using high voltages and currents. To validate the control algorithms proposed in this thesis to an acceptable standard, it was necessary to test at typical grid voltages. As a rule of thumb, voltages above 50 V should be considered hazardous, therefore, the voltages specified for this converter build must be treated with extreme caution.

Due to the need to capture experimental data, it was anticipated that the converter would be connected to a host PC for programming and monitoring during operation. Furthermore, for reasons of practicality, it was expected that standard, non-isolated oscilloscope probes would be used to observe low voltage PWM and analogue signals being output by the controller. With this in mind, it was critical that no high voltages from the power circuit of the converter could propagate into the low voltage control circuitry. It was decided that any required interface between the high voltage circuit and the control circuit would need to be through galvanically isolated components. A block diagram showing the required interconnections is shown in Figure 5.1.

Shown to the right of Figure 5.1 are the subsystems which operate at high voltages. Shown in the centre are the low voltage control circuits and shown on the left are the systems that the user must interact with. Of critical importance are the systems which cross the boundary between blocks, as these must prevent dangerous voltages from crossing into safety critical areas. If any one system introduces a conducting path from one region to the other, all of the benefits of isolation are lost. Of particular interest are the voltage and current sensors, the gate drivers and the gate drive bias supplies, because the design of these is at the discretion of the author and they will each be responsible for preventing high voltages from the power circuit entering the lower voltage areas.

b. Choice of Semiconductor Technology

The choice of semiconductors for power electronic applications may be broadly categorised into standard silicon (Si) devices, or wide band gap (WBG) silicon carbide (SiC)

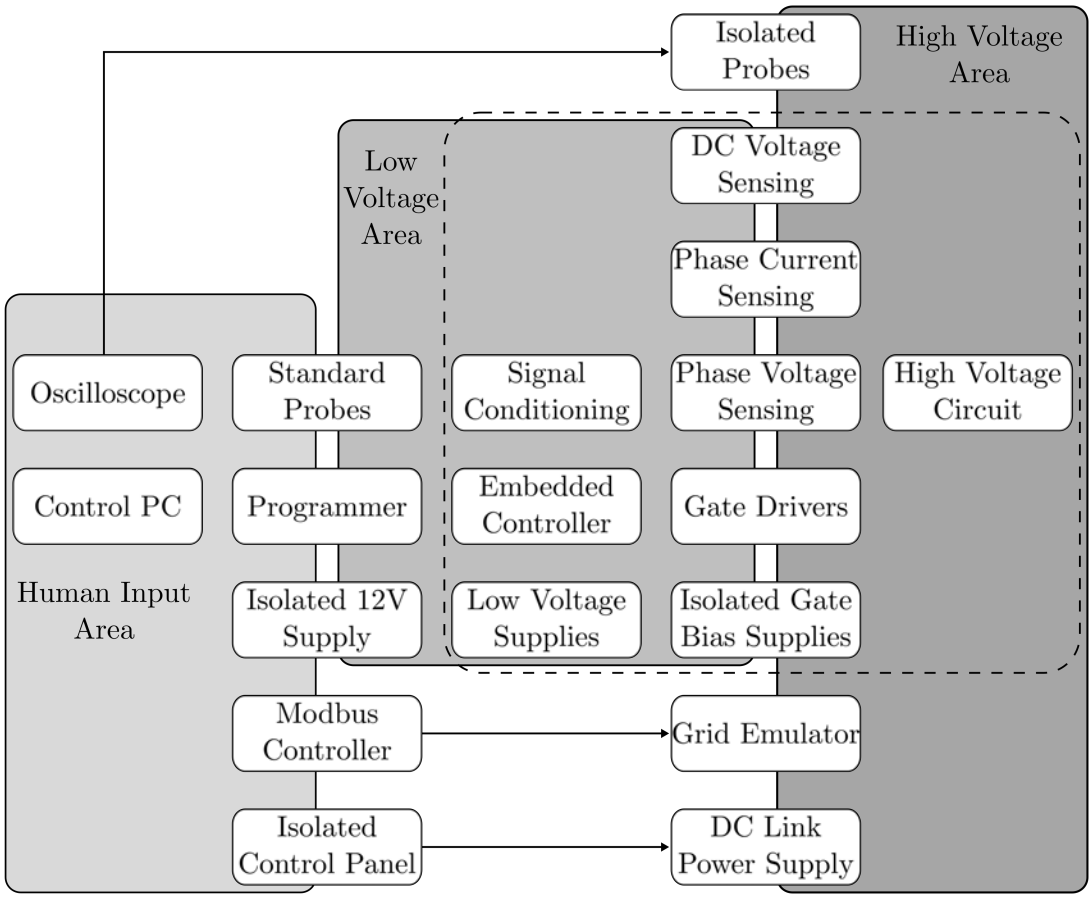


Figure 5.1: Isolation block diagram. Subsystems within the dashed line were designed entirely by the author.

or gallium nitride (GaN). In general, WBG devices offer lower switching losses which permits higher switching frequencies, allowing smaller passive components and cooling solutions to be used, increasing overall power density. Higher voltage blocking capabilities also allow use in higher power applications, as well as allowing simpler two-level topologies to be employed at high voltages. At the time of writing, WBG devices are gaining increasing traction in a broad range of power electronic applications, however, their relative cost and challenging design means that Si devices remain dominant.

For both WBG technologies, very high di/dt may lead to voltage spikes due to stray inductances in the power and gate drive loops and very high dv/dt may lead to currents flowing in the junction capacitances, leading to Miller turn-on [269]. These parasitic inductances and capacitances may also lead to ringing, generating EMI [269].

The need to minimise stray inductances means that component layout and routing is much more critical when dealing with WBG semiconductors compared with their Si counterparts [270].

SiC is currently the more mature technology compared with GaN [271]. Compared with Si, it has a high critical field strength which makes ultra-high voltage blocking practical (> 10 kV) [33]. Its lower specific on resistance also means a SiC device can be smaller than an equivalent Si device [33]. The smaller device leads to lower parasitic capacitances and inductances [33]. High thermal conductivity also aids heat extraction and cooling [269], therefore SiC excels in high-temperature applications [272]. However, the higher cost compared with Si devices has limited use to high performance applications [271]. SiC devices also have poor short-circuit withstand capability, therefore dedicated gate drivers with integrated protection are often used [273].

GaN has an even wider band gap than SiC, greater critical field strength and improved electron mobility [274]. For this reason, it excels in very high-frequency, high-efficiency applications [272] where superior electron mobility permits very high switching frequencies, even compared with SiC. This has led to GaN being widely adopted for radio frequency (RF) applications. However, GaN has a much lower thermal conductivity than SiC, making it less suitable for high thermal loads. Furthermore, care must be taken not to exceed the relatively low gate breakdown voltage [269].

For the converter design described in this thesis, a SiC JFET (UJ3C065030K3S) from UnitedSiC [275] was selected for the following reasons:

1. The SiC device offers low switching losses, simplifying thermal design.

2. High switching frequency capability makes the converter more flexible for future projects.

3. The JFET accepts unipolar gate drive (O V off, 12V on), simplifying gate driver design.

c. Isolated Current and Voltage Sensing

Three of the converter subsystems which must cross the boundary from the high voltage region to the low voltage control region as shown in Figure 5.1 are the DC link voltage sensing, the phase current sensing and the phase voltage sensing. These systems must accurately transfer measurements across the isolation boundary without creating a conducting path that could allow high voltages to leak into the low voltage area.

There are two main methods of measuring current. The first is to pass the current through a known resistance then measure the volt drop across it and compute the current based on ohm's law. Typically, very small value resistances are used to minimise the resulting power dissipation. This small voltage is then fed into an isolated difference amplifier which produces a voltage proportional to the current in the resistor. This small voltage is then transferred across the isolation using capacitive [276], magnetic [275] or optical [277] coupling, depending on the exact amplifier selected. The fixed resistance is known as a shunt resistor, therefore, current sensors using this approach are known as shunt-based current sensors. The second method is to deduce the current from the magnetic field it produces, known as the Hall-effect. These sensors may be further categorised into open-loop [278] and closed-loop [279]. In the open-loop sensor, the output of the sensor is a voltage, similar to shunt-based techniques. In the closed-loop sensor, the output is a smaller current, which may be transformed into a voltage at the receiving end using a resistor. There are many technical and economic trade-offs associated with shunt- versus Hall-based current sensing techniques. For a thorough analysis of the differences, the reader is directed to [280].

For isolated measuring of voltages, the same general rules apply. Isolated voltage amplifiers may be used to transfer a signal across the isolation boundary using capacitive, magnetic or optical coupling. Alternatively, the voltage may be transformed to a small current using a known resistance, then this current may be measured using a Hall-effect sensor as before.

For the converter design described in this thesis, a shunt-based sensor with isolated differential amplifier was selected for the current measurement, while an isolated voltage amplifier was selected for the DC voltage sensing. The following factors led to this

decision:

1. The current levels are relatively low (< 25 A), therefore, a small current shunt is practical with minimal power loss and space requirements.
2. A shunt and isolated amplifier are more compact and cheaper than closed-loop Hall-based current sensors.
3. A shunt and isolated amplifier are more accurate than open-loop Hall-based current sensors [280].
4. The isolated current sense amplifier selected can be repurposed to sense the phase voltage as well, due to its bidirectional input stage, as shown in Appendix A.
5. The isolated current sense and voltage amplifiers selected have identical differential output stages, therefore, the same analogue signal conditioning circuitry can be employed for both.

d. The Embedded Microcontroller System

To validate the control algorithms proposed in this thesis, an embedded microcontroller would be needed that could be programmed with the control algorithm under test then execute it in real time. There were two main options for integrating the control: to have some sort of docking system for an off-the-shelf microcontroller development board with all its ancillary circuitry or to integrate the bare microcontroller integrated circuit (IC) itself, together with all its ancillary circuitry directly onto the PCB. The merits and limitations of each approach were considered carefully, as summarised in Table. 5.1.

The following essential criteria for the microcontroller system were identified:

1. Floating point capable
2. Flexible timer peripheral for generation of PWM signals
3. Multiple ADC channels for sampling of measured variables

Table 5.1: Considerations when Docking a Microcontroller Development Board versus Directly Integrating the Microcontroller

Docking a Microcontroller Development Board	Directly Integrating the Microcontroller
• Higher cost • Shorter time to deployment • Reduced risk of errors in the design • USB to JTAG already implemented • Long distance from ADC driver amplifiers to input pins • Poorer separation of analogue and digital signals • Long signal traces prone to EMI	• Lower cost • Longer development time • Increased risk of errors in the design • USB to JTAG needs to be implemented • ADC driver amplifiers can be placed next to input pins • Possibility of zoning analogue and digital signals • Shorter signal traces more immune to EMI

4. Flexible interrupt structure for dealing with control, protection and communication tasks

5. DAC outputs to observe internal variables

6. Compatible with open-source or low cost programming environment with real time debugging tools

With these issues considered, the Texas Instruments TMS320F28379D microcontroller from the C2000 family was selected, mounted on the TMDSCNCD28379D Control Card development board. This microcontroller offers the following key features:

1. Dual core 200 MHz 32-bit CPU with floating point and trigonometric math support.

2. Analogue subsystem with 4 ADCs with multiplexed inputs for up to 24 channels.

3. Enhanced PWM units offering 24 channels of PWM with advanced timing options.

4. Three DAC modules.
5. USB 2.0 module with potential for advanced data-logging options.
6. Free and unlimited integrated development environment for programming and debugging.

In addition, the C2000 family can be programmed using Simulink Embedded Coder offering the choice between model-based, or pure C-code programming for ultimate flexibility.

5.1.2 Proposed Design

With the key design decisions made and core components selected, a PCB was designed to implement the system. Figure 5.2 shows a 3D render of the underside of the PCB. Each of the three phases of the converter comprises an identical block of subsystems whose layout is duplicated for each phase, namely: a high and low side switch, two gate drivers, a polypropylene DC link capacitor, DC link snubber capacitors, snubbers across the switches, two gate drive bias supplies and a current sense amplifier. Similarly, on the low voltage side, the analogue signal conditioning circuitry is duplicated for the three phases. Figure 5.3 shows a 3D render of the top of the PCB as viewed from the control side. Of particular interest is the mounting point for the Texas Instruments Control Card, allowing the microcontroller to be changed easily if it is damaged, or to allow a different member of the Control Card product line to be used. Figure 5.4 shows a 3D render of the top of the PCB as viewed from the high power side. Figure 5.5 shows the actual converter constructed in the lab.

5.1.3 Particular Challenges Encountered

The converter hardware developed comprises over 500 components, therefore it would not be possible to describe in detail every aspect of the design. A few particularly challenging design issues and the solutions adopted are discussed in the following sections.

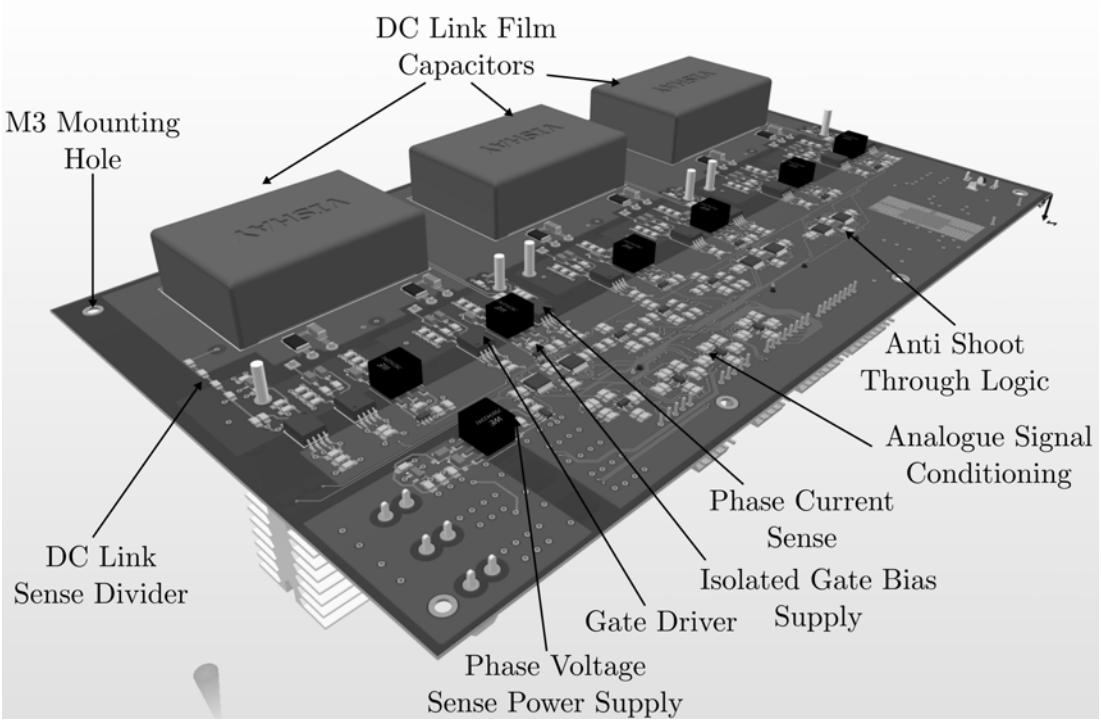


Figure 5.2: Annotated 3D render of the bottom side of the converter PCB.

a. Layout Challenges with Wide Band Gap Semiconductors

Wide bandgap semiconductors like SiC and GaN transition from off to on and vice versa much faster than their Si counterparts. While this is helpful in reducing switching losses, it posses a number of challenges to the circuit designer. All cabling in the test rig, traces on the PCB and even leads of the components have a small but finite inductance. Similarly, any pair of conductors in close proximity have a capacitance between them. These parasitic inductances and capacitances can suffer resonance issues when excited by the rapidly rising and falling edges produced by the wide band gap switches.

Of particular concern are the stray inductances between the two switches forming a half bridge. These inductances are shown in Figure 5.6a. There is also a parasitic inductance between the switch node and the converter output L_{p3}, however, this is not important since it simply adds to the much larger filter inductor L_{filter}. When $Q1$ switches off, it attempts to abruptly cut off current flowing through L_{p1} while rapidly trying to establish a current through L_{p2}. This large di/dt leads to a voltage spike which

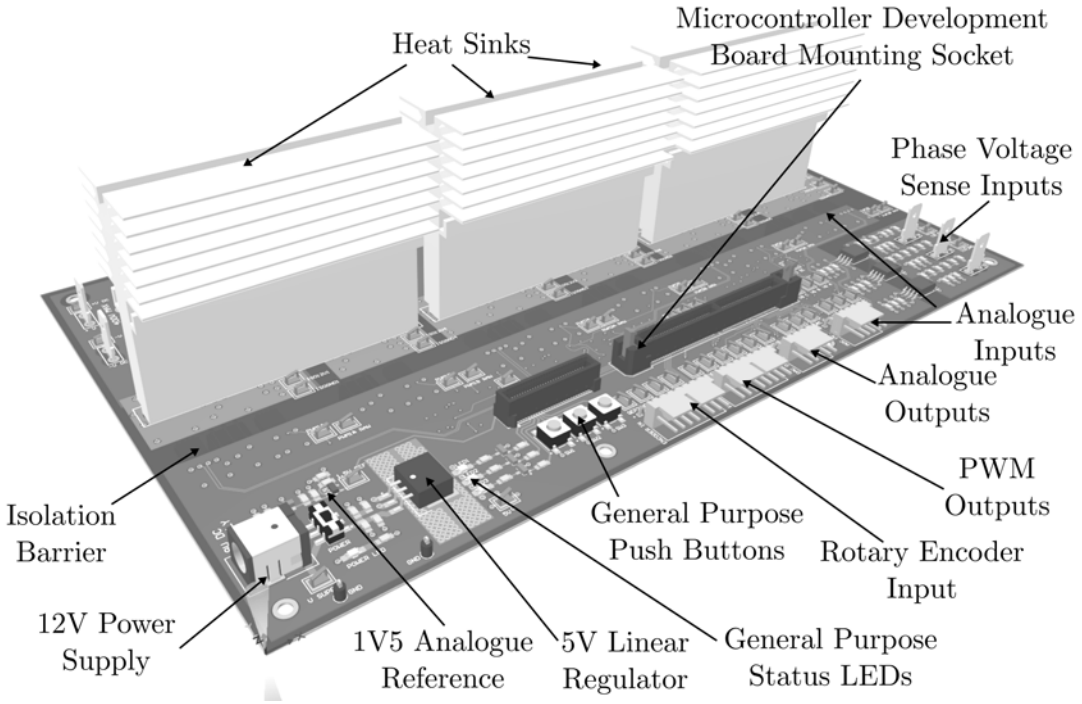


Figure 5.3: Annotated 3D render of the top side of the converter PCB viewed from the control side.

causes EMI issues or, at worst, exceeds the voltage rating of the switch and destroys it. This effect can be mitigated partially by observing good PCB layout practices. Positioning the top and bottom switch of each half bridge as close as possible to each other minimises the parasitic inductance. For additional protection, an RC snubber can be placed across the switch to damp the voltage spike. Since WBG devices have very low output capacitances, relatively small values of snubber capacitance can have a large impact on reducing overshoots [281]. The position of the RC snubbers is shown in Figure 5.6b. Similarly, the cables connecting the DC power supply to the DC link inputs of the converter have a finite inductance. This means there may be a dip in the DC link voltage during switch transitions. A four pronged approach was adopted to mitigate this. Firstly, large electrolytic bulk capacitors were installed as close as possible to the converter and connected with short wires. Secondly, low equivalent series inductance (ESL) polypropylene film capacitors were included in the converter PCB as close as possible to each half bridge. Third, a multilayer ceramic capacitor

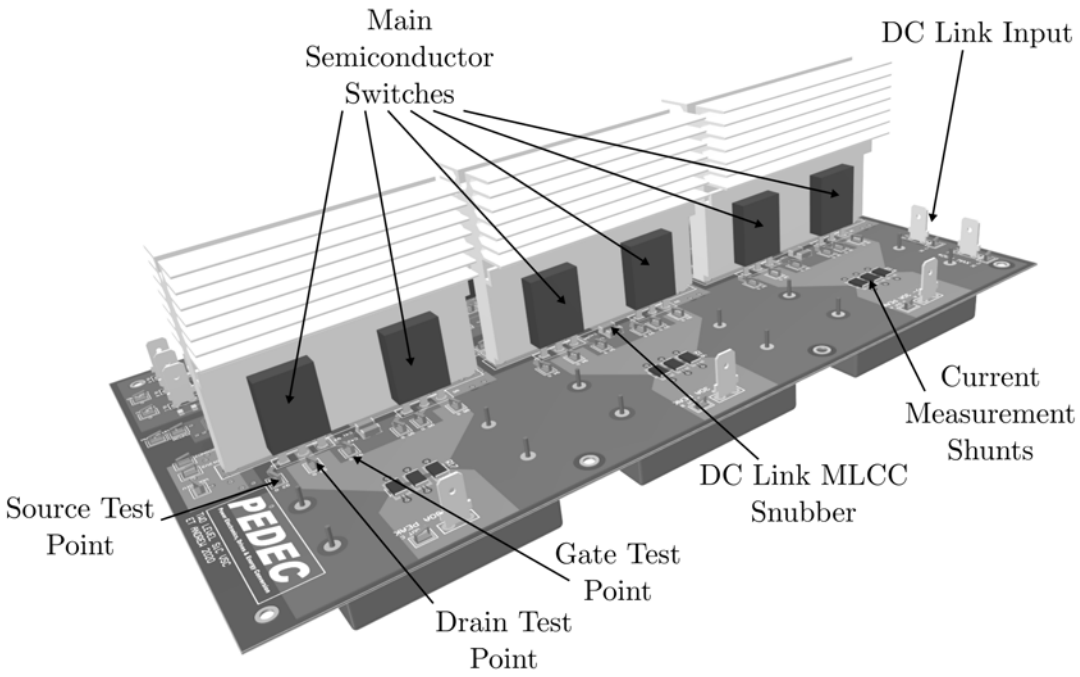


Figure 5.4: Annotated 3D render of the top side of the converter PCB viewed from the power side.

(MLCC) was installed across the DC link as close as possible to each half bridge to provide a very low equivalent series inductance (ESL) reservoir of charge as close to the switches as possible. Finally, all cable connections were twisted to minimise their inductance. These features are illustrated in Figure 5.7.

b. Handling High Currents and Voltages on a PCB

The need to operate at realistic voltage and power levels means that the converter must be able to withstand voltages in excess of 400 V and currents in excess of 15 A. Proper spacing of high voltage components and traces is essential to avoid flashover or tracking between conductors [282]. In short, it is desirable to keep conductors at high voltages as far away from each other as possible. On the other hand, traces handling high currents should be kept short and wide to minimise the PCB inductance and resistance [283]. Placing lots of large, wide conductors onto a PCB where it is necessary to keep conductors as far away from each other as possible is a design challenge in itself.

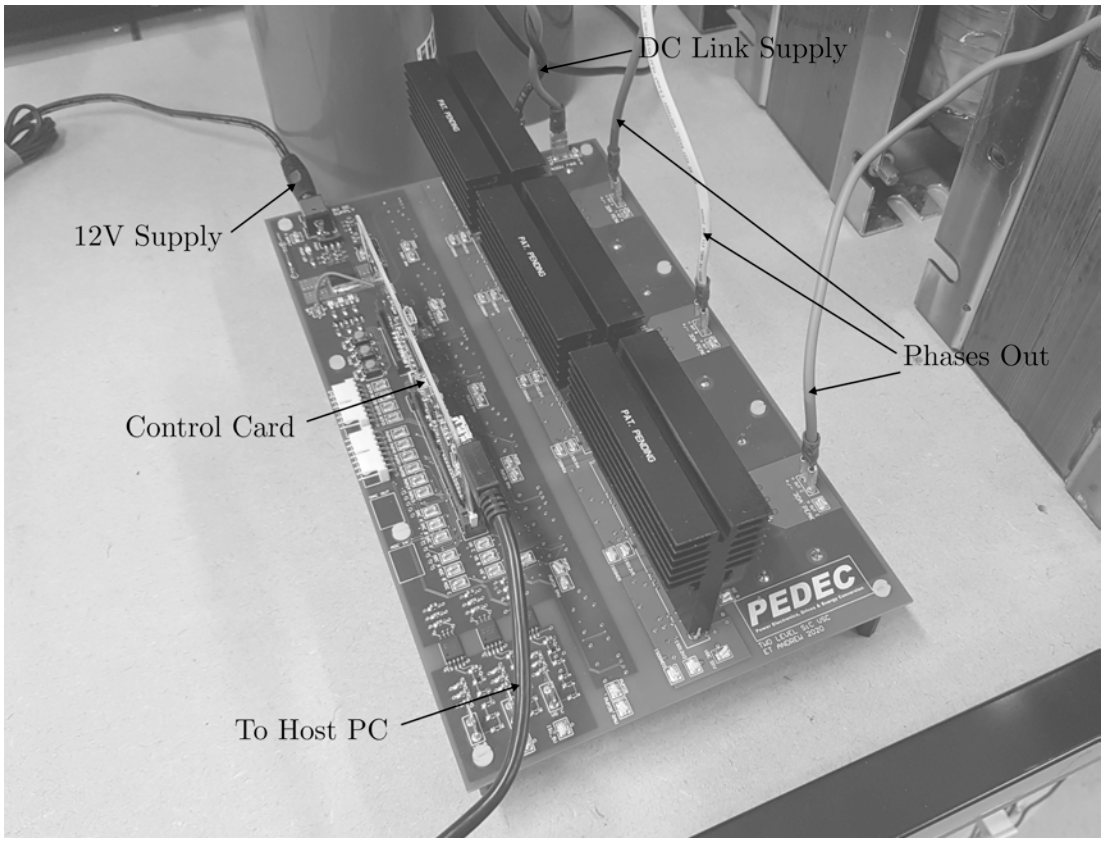


Figure 5.5: Photograph of the actual constructed converter.

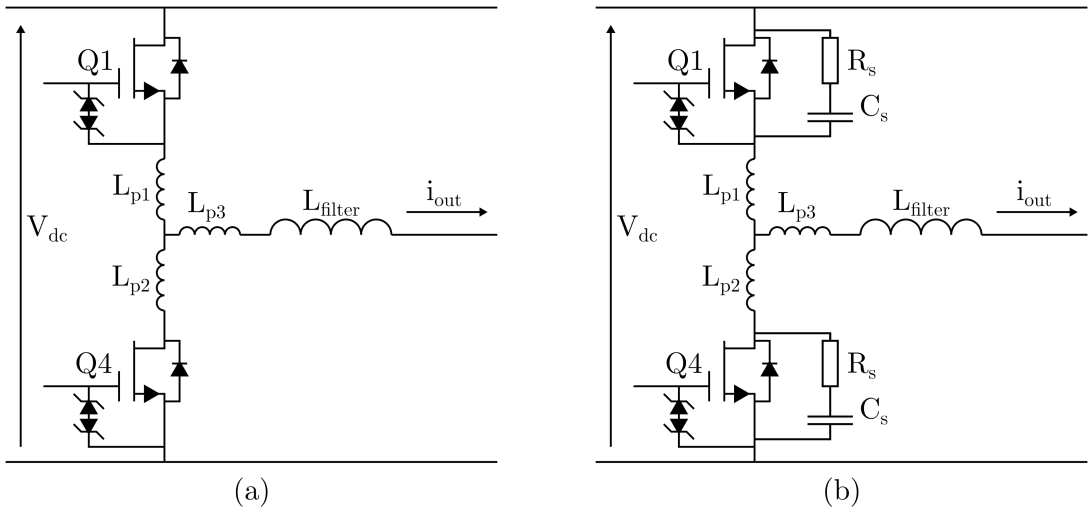
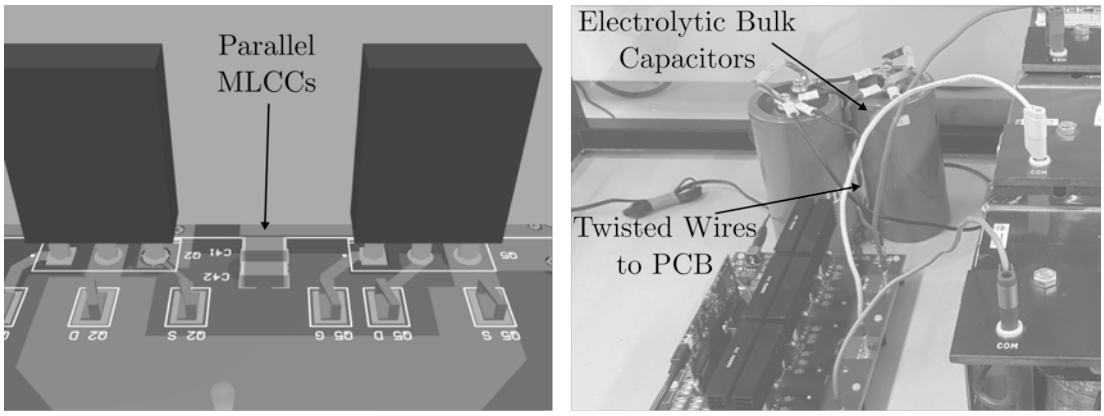


Figure 5.6: Half bridge circuit showing the effect of stray inductance at the switch node (a) without snubber (b) with RC snubber.



(a) (b)

Figure 5.7: Parasitic inductance reduction methods including (a) the PCB features (b) external features.

The copper layout proposed is shown in Figure 5.8. As shown in Figure 5.8a, large areas of copper are used to carry the main phase currents and filled areas are connected to the source pin of each switch, aiding in the creation of a low inductance gate loop. Figure 5.8b and Figure 5.8c show that large rectangular pours on the internal layers are used for the DC link, maximising the capacitive effect. The vias are spaced so that current can flow between them, preventing break up of the plane and reducing inductance. Figure 5.8d shows the bottom layer which is reserved for the shunt resistor traces, whose lengths are equalised as much as possible. The traces are also routed close together to ensure that induced noise is common to both traces and is cancelled out by the differential amplifier.

c. PCB Stack-up

The number of copper layers in a printed circuit board can be chosen by the designer, however, it should be subject to a cost-benefit analysis. One- or two-layer boards are cheap to manufacture and offer enough routing space for the most basic designs. Four-layer boards generally allow a power and ground plane to be used, making routing of power connections easier and improving the EMC performance. Six-layer boards and beyond offer further improved routing space, the possibility of multiple power and ground planes and improved EMC performance [284]. For the purposes of this design,

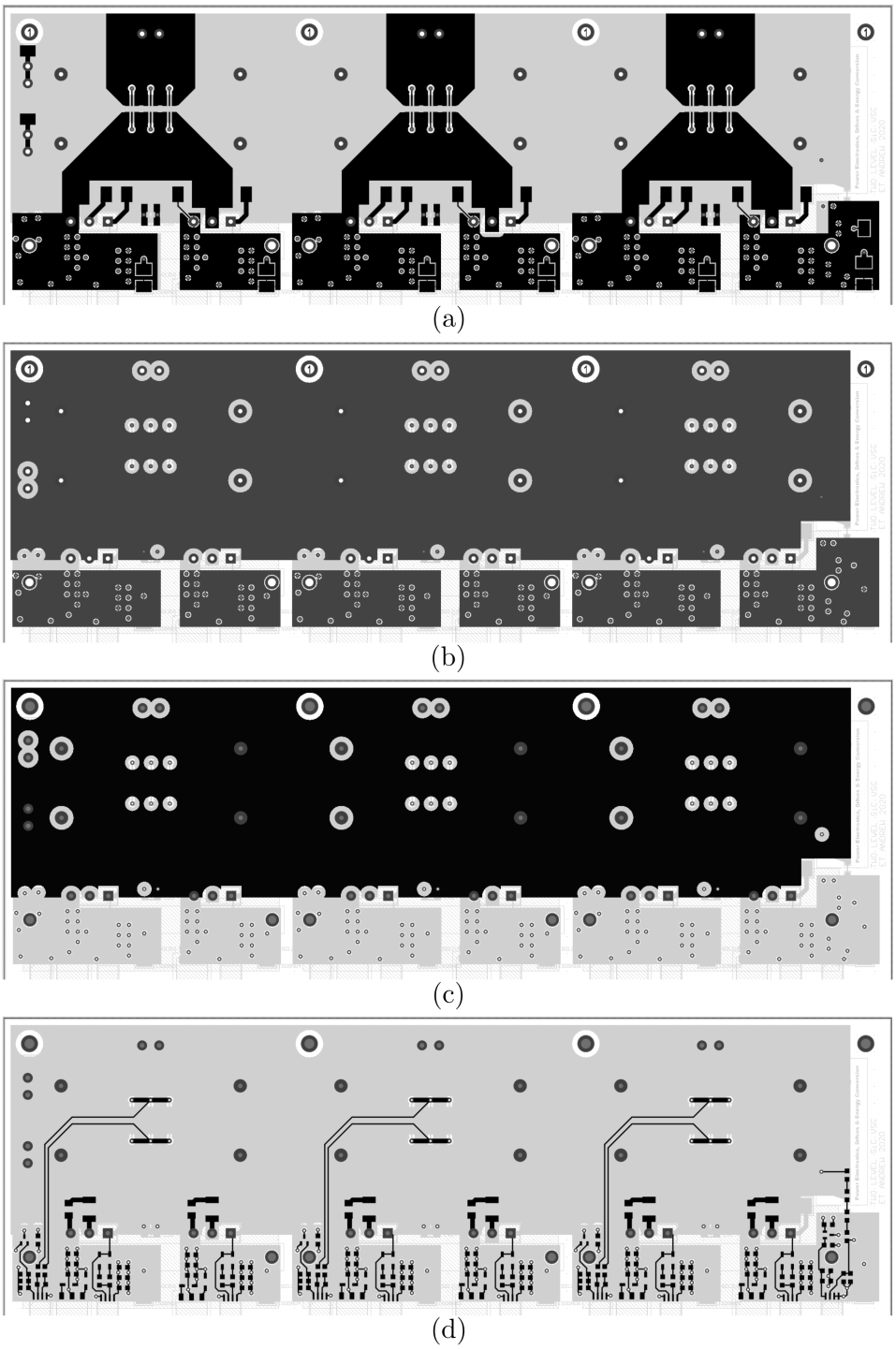


Figure 5.8: Copper layers for the high voltage area (a) the top layer with the phase outputs (b) layer 2 with +Vdc (c) layer 3 with -Vdc (d) bottom layer with the shunt sense connections.

a four-layer board was selected for the following reasons:

1. Four layers offers one layer each for the DC ground, DC bus voltage and phase output.
2. Most of the control circuitry requires only 5V, therefore, one power plane and one ground plane are adequate.
3. Four-layer boards are not much more expensive than two layers, but much cheaper than six layers.

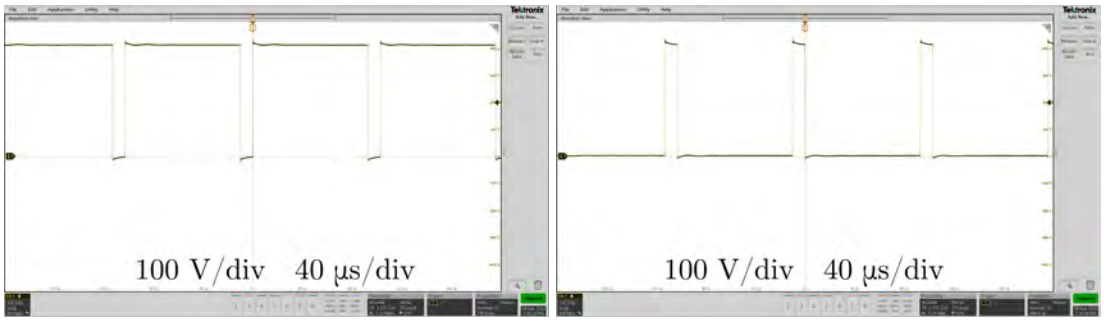
d. Test and Debug Access

Throughout the PCB, there are many signals of interest which must be checked periodically for debugging or calibration purposes. The final PCB design incorporates over 70 surface mount test points for oscilloscope probes.

e. Connectivity with the Microcontroller

The Texas Instruments control card makes all of its input and output signals available through an edge connector. This is inherently undesirable from a signal zoning perspective, since analogue and digital signals are in close proximity [284]. This also means that the analogue signal conditioning circuitry must be located some physical distance from the analogue to digital converter (ADC), which is sub-optimal for fast charging of the sampling capacitor [285].

To mitigate these issues, the analogue signal conditioning amplifiers are positioned as close as possible to the control card connector. There remains an inevitable distance between the amplifiers and the analogue to digital converter (ADC) inputs, however, the fundamental frequency of interest is relatively slow changing at 50 Hz, therefore, there should be no need to rapidly charge or discharge the sampling capacitor. The effect of noise induced in the long signal traces should be minimised by sampling on a PWM timer-zero to ensure that switching spikes have subsided before the sample is taken.



(a) (b)

Figure 5.9: Drain-source voltage for (a) the high-side switch (b) the low-side switch.

The digital signals coming out of the controller could also be degraded by the relatively long signal traces. However, the anti-shoot through logic and the gate drivers both feature Schmitt trigger inputs, therefore, they should reject most noise on the signals.

5.1.4 Hardware Testing

To assess the effectiveness of the PCB design and the behaviour of the RC snubber circuit used on each of the SiC switches, the drain-source voltages were examined. Figure 5.9 shows the drain-source voltages across the high- and low-side switches while the converter operates as a synchronous buck converter with fixed duty factor of 10%. The DC input voltage is 400 V. Figure 5.10 shows example drain-source voltages captured at arbitrary points on a sinusoidal current. As shown in Figure 5.9, the drain-source voltages for both the high- and low-side switches have very little overshoot, indicating the effectiveness of the PCB layout and snubber circuit. This is further demonstrated in Figure 5.10 where detailed views of the switching transitions for the high- and low-side switches are shown. Figure 5.9 and Figure 5.10 show the fast switching behaviour of the SiC switches together with the damped turn-off waveform due to the RC snubber circuit.

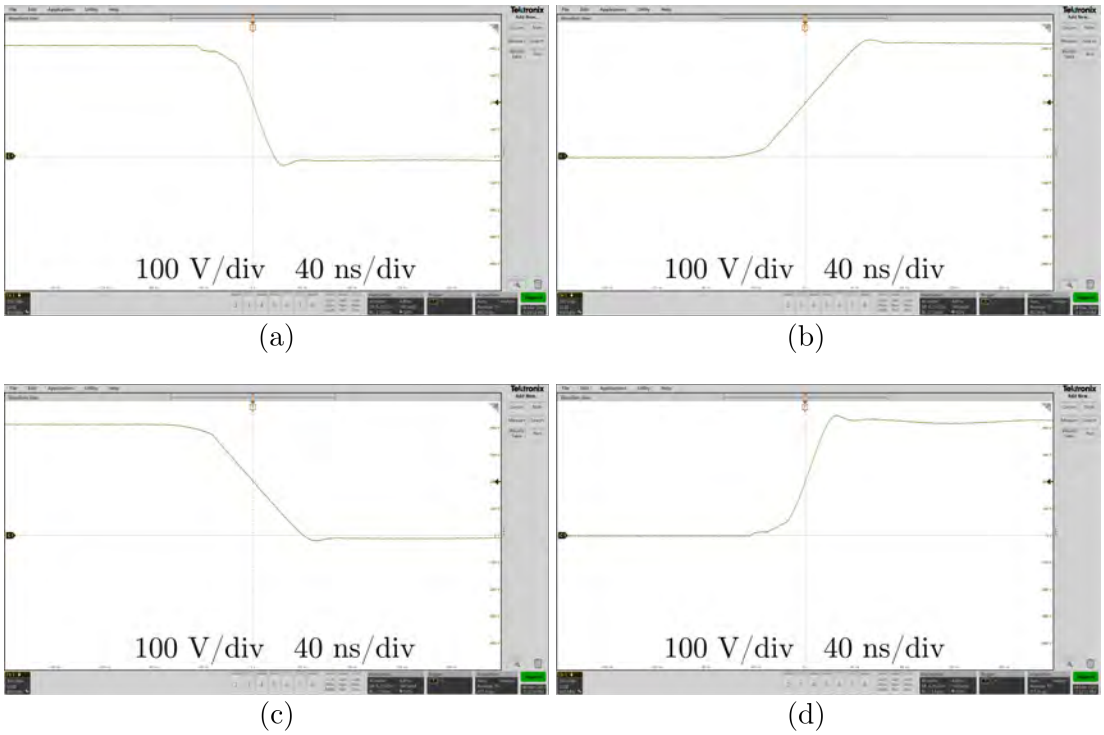


Figure 5.10: Indicative drain-source voltages captured at arbitrary points on a sinusoidal current waveform for (a) the high-side switch during turn-on (b) the high-side switch during turn-off (c) the low-side switch during turn-on (d) the low-side switch during turn-off.

5.2 The Converter Software

The Texas Instruments C2000 family of microcontrollers are designed for a broad range of real time control applications. Like any microcontroller, they could potentially be programmed at the assembler level, however, given the complexity of the control algorithms likely to be implemented, it is expected that the vast majority of applications will be implemented in C code. Texas Instruments provide their own integrated development environment (IDE), Code Composer Studio (CCS), free of charge to support their portfolio of microcontrollers and DSPs.

By the time all of the required mathematics and peripheral control functions are included, the software required to implement the control algorithms proposed in this thesis runs to some length. Clearly, it would not be possible to describe in detail all of

the software written, therefore, the purpose of the following sections is to describe the methodology used and a few specific problems encountered.

5.2.1 Key Design Decisions

It was anticipated that several model predictive controllers would be implemented in hardware over the course of the research project. Furthermore, it was expected that conventional vector current controllers would be implemented for comparison purposes. Some features would be common to all controllers, such as the transformation of raw ADC results to actual voltages and currents, while other features such as the current control algorithm itself would be quite different. There would be fundamental differences in the way that each controller interacted with the hardware. In the case of conventional vector current controllers, the output of the controller would be three duty factors. In the case of a conventional FCS-MPC, the output of the controller would be a vector number which would need to be decoded to a given switch state, output immediately and held that way for the whole sampling period. Finally, in the case of the MMPC, the controller output would be two vector numbers and three dwell times, therefore, this would need to be converted to three duty factors. In short, it was anticipated that each controller would influence the hardware in different ways, therefore, a highly modular software approach would be required.

5.2.2 Proposed Software Structure

There are four distinct levels to the proposed software structure as follows:

1. **driverlib** - Off-the-shelf low level drivers provided by Texas Instruments providing one level of abstraction above the register level. eg.

   EPWM_setCounterCompareValue(...); to place a numerical value into the counter/compare register.

2. **Custom Math Functions** and **Peripheral Functions** - Functions written by the author to provide vector and matrix math operations and control the peripherals at a higher level of abstraction. eg. *peripheral_epwm_set_mod(...);* to set a

particular modulation index between -1 and 1, without worrying about the actual compare value.

3. **Control Functions**, **Filter Functions**, **Kalman Filter Functions**, **Debugging Functions** and **Measurement Functions** - Functions written by the author which use the custom math and peripheral functions to perform common control tasks. eg. *kalman_update(...);* to update the Kalman filter without worrying about the maths required.

4. **Control Implementations** - The highest level of the hierarchy implementing a complete controller, called by the ADC interrupt. eg. *eckf_mmpc(...);* to implement a complete MMPC current controller with ECKF estimator without worrying about the individual steps.

The software structure and the component files are illustrated in Figure 5.11. Each of the header files shown in Figure 5.11 contains several functions to perform control tasks corresponding roughly to the name of the header file. For example, *control_pq_calc.h* contains functions to calculate the current reference for a required active power in the abc, dq and $\alpha\beta$ reference frames, for both balanced and unbalanced systems, such as *calc_current_ref_ab_unbalanced(...)*.

5.2.3 Software Execution

In general, the microcontroller initialises itself at start-up, then calls functions written by the author to setup the peripherals as required by the control algorithm under test. When this is complete, the PWM module is started and the current control algorithm is called periodically.

5.2.4 Particular Challenges Encountered

Much of the required functionality is built up using simple logical and mathematical operations. However, a few implementation challenges were encountered which are discussed in the following sections.

a. Handling of Complex Numbers and Complex Matrices

Custom functions were written to perform basic tasks like addition, subtraction, multiplication and division. More advanced functions to calculate dot products and vector angles and sort complex valued arrays by magnitude were also written. Wherever possible, the data structures containing the real and imaginary components are passed by reference to the functions that manipulate them, avoiding the overheads associated with creating fresh copies on the stack [286].

The implementation of the extended complex Kalman filter required mathematical operations to be performed on matrices populated with complex numbers. An additional collection of functions was written which uses combinations of the basic complex maths functions to perform matrix arithmetic.

b. Verification of Control Mathematics

The implementation of Kalman filter in particular requires several matrix math operations. These are then implemented as a series of complex math operations, which in turn boil down to individual floating point math operations. Across these levels of abstraction, with functions calling functions, there is a high likelihood of programmer error, leading at best to a compilation error or, at worst, a sudden failure at runtime leading to a loss of control of the live system. Perhaps worse still, is the possibility of an intermittent problem which produces unwanted results but is hard to trace.

To maximise the chances of the control mathematics working as intended, a design process was adopted which aimed to identify logical issues early. First, the proposed algorithms were tested using the graphical building blocks within Simulink. This offered the fastest testing and ease of modification. Next, the proposed controller was implemented entirely within a Matlab function block within Simulink. This meant that graphical blocks were no longer used and the Matlab function was much closer to an eventual C program. Logical and timing issues were often identified at this point. Also, variables which needed to retain their value across controller iterations were easily identified at this stage. Next, the algorithm was implemented in C code and compiled as a Windows terminal application. This meant that the Matlab program and the C code

could be stepped through simultaneously and the variable values compared at every step. This allowed a number of mathematical errors to be identified and corrected, as well as C-specific issues, like incorrect array indices to be identified and fixed. Finally, the C code was copied across to CCS and deployed to the hardware. By this point, most logical and mathematical errors had been ironed out, reducing the risk of a problem developing at runtime and freezing the control at a critical point.

c. Viewing Internal Variables

There are many variables of interest within the microcontroller itself which are helpful to view in real time as the controller is running. The PCB design routes the DAC outputs of the controller to a connector and a set of test points. Therefore, some method was needed to route combinations of signals to the DACs with proper shifting and scaling applied. This functionality was implemented in the *debug_logic.h* header file. A long list of boolean flags is used to determine which signal should currently be routed to the DACs. These flags can be changed at runtime using the JTAG debugger within CCS. Figure 5.12 shows an example where the debug flag is set to output the current reference signal in real time while a high-bandwidth current probe is used to measure the actual current. This debugging functionality allows the controller tracking to be verified in real time.

5.3 Remarks on C code versus Model Based Code Generation

In recent years, Mathworks have developed the Embedded Coder package, an add-on to their popular Simulink simulation package, allowing discrete models composed of graphical building blocks to be automatically converted to C code and deployed to hardware. The Texas Instruments C2000 family is one family which is supported by Embedded Coder and simulated controllers can be made to run on the C2000, in theory, with the click of a button. This approach has come to be known as model based code generation. In many control applications, the engineer will have already validated the

proposed controller in simulation, therefore, the ability to generate working microcontroller software from this model without ever setting foot in a microcontroller IDE is certainly appealing.

That being said, model based code generation is not without its pitfalls. It is the author's opinion that the ability to generate code without ever thinking in terms of bits in registers is not always a good thing. Even in a simple power electronic control application a PWM peripheral triggers the ADC, then the ADC end-of-conversion triggers an interrupt which executes the current controller. The relative timings of these actions must be given careful consideration, lest the ADC sample during a switch transition and pick up transient spikes, or the current controller execute too soon and use the previous set of measurements. Therefore, it is the authors belief that being able to program the hardware using high level graphical blocks should be seen as useful tool for the experienced engineer and never as a shortcut for a novice to program microcontrollers without fully understanding the hardware.

The control algorithms presented in this thesis have been implemented entirely in C code without the use of Embedded Coder. This approach offers the following advantages:

1. Full control of the peripherals is available at the register level, allowing unusual modulation patterns to be implemented.

2. Interrupt Service Routines can be programmed individually, ensuring that all time-critical actions occur at the proper moment.

3. Interrupt Service Routines can edit the peripheral registers in between sampling instants to behave differently or achieve different sample timing at the next controller iteration.

Nevertheless, implementing the control algorithms in C code has required a significant time investment.

5.4 Summary

In the past, converters have been constructed from discrete silicon IGBT modules, separate gate drive boards and bulky Hall effect current sensors. This approach does not fully leverage the advantages of modern WBG semiconductors and compact sensing solutions. Furthermore, since these converters are often controlled using real time computers, the limitations of standard microcontrollers are not encountered. It is not uncommon to see control algorithms proposed with vast numbers of floating point and trigonometric calculations which would not be practical for real world use.

This chapter has described a modern three-phase DC/AC converter design which is fully self contained, easy to test, debug and calibrate and incorporates a modern, industry standard microcontroller with flexible programming options. Furthermore, a suite of software has been developed allowing advanced control algorithms to be efficiently built up from fundamental building blocks. Practical results have been shown proving the effectiveness and flexibility of the overall design.

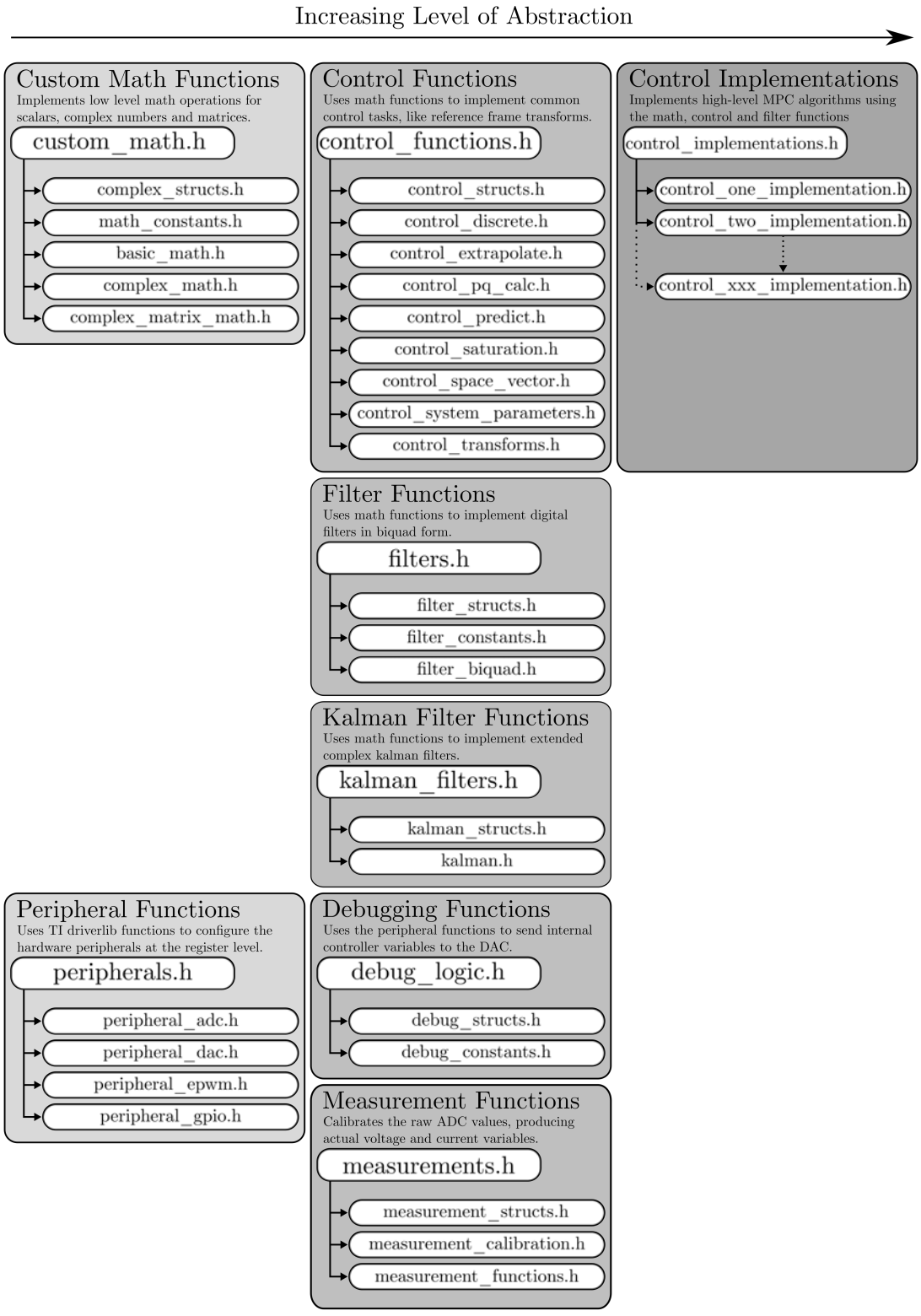


Figure 5.11: Structure of the controller software.

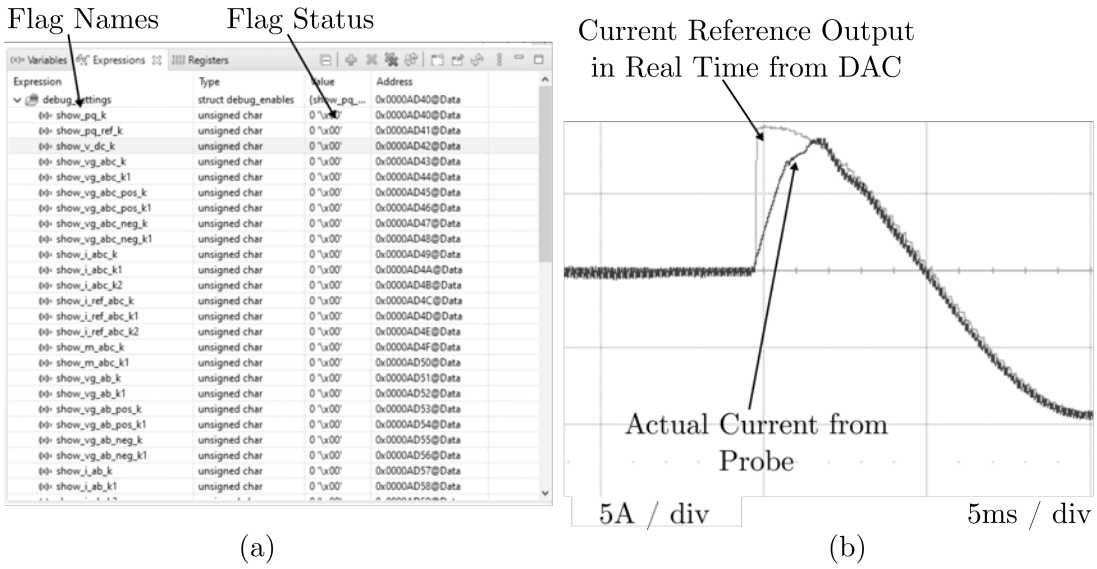


Figure 5.12: Debugging example where the current reference is routed to the DACs, showing (a) the debug flags as shown in the JTAG variable window (b) the resulting DAC output and actual current superimposed.

Chapter 6

Conclusions

Future power networks are anticipated to feature large numbers of small scale distributed generators, therefore, the control of grid-connected interfacing inverters has attracted considerable research attention in recent years. This thesis has presented several contributions to knowledge in the field of predictive control of grid connected converters.

6.1 Summary of Conclusions

In chapter 3, a new formulation of the model predictive current control optimization stage was proposed. The new optimiser selects the active vectors to be used with significantly less computation than existing approaches. Simulation and experimental results are included to demonstrate that these improvements are made without sacrificing controller performance.

Furthermore, in chapter 3, an existing over modulation algorithm was analysed and simplified to reduce its complexity. The new algorithm allows the proposed controller to achieve optimised performance beyond the linear modulation region without incurring the additional computational cost of existing techniques. Together, these contributions resulted in reduced computational burden with no reduction in performance. The calculation burden is shown to be reduced by 46% when implemented on a typical microcontroller.

Moreover, in chapter 3, the issue of parameter mismatch and grid voltage discretization was considered in greater depth than in previous works. The impact of sampling the grid voltage and assuming that it is constant over the sampling period is analysed mathematically and an ideal compensation strategy is derived. The limitations of the ideal compensation for a practical system are described and an approximate compensation method is proposed. The new compensation method is shown to achieve similar results to the exact method without adding complexity to the overall controller.

In chapter 4, methods of current control in unbalanced grids were studied and their limitations were identified. The controller proposed in chapter 3 was extended to unbalanced systems by the addition of a Kalman filter estimator to separate the symmetrical components of the grid voltage. The currents are effectively controlled even in the unbalanced system without using a PLL.

Furthermore, in chapter 4, a new calculation time compensation method is proposed based on the Kalman filter estimator which achieves superior accuracy and noise rejection compared with the prior art. All of these enhancements are achieved without increasing the computational burden of the controller, and it is demonstrated that the calculation time is less than an existing controller. The outcome of this work was presented as a peer reviewed journal paper in IEEE Transactions on Power Electronics.

Finally, in chapter 5, a hardware converter design was developed to permit testing of the various controllers studied in this thesis under realistic conditions. This design has been used successfully to capture the experimental data presented in this thesis and in the related peer reviewed publications. The design has also been used by other students within the research group to gather results for their own published work.

6.2 Suggestions for Future Work

The work presented in this thesis has laid a solid foundation for the development of grid-connected converter systems. Suggestions for future work on the control system include:

- Investigation of whether an adaptive controller could be used to further reduce

the effects of parameter mismatch and grid voltage discretization.

- Investigation of whether the Kalman filter state matrix can be augmented with additional variables to estimate and compensate harmonic components in the estimated voltages.

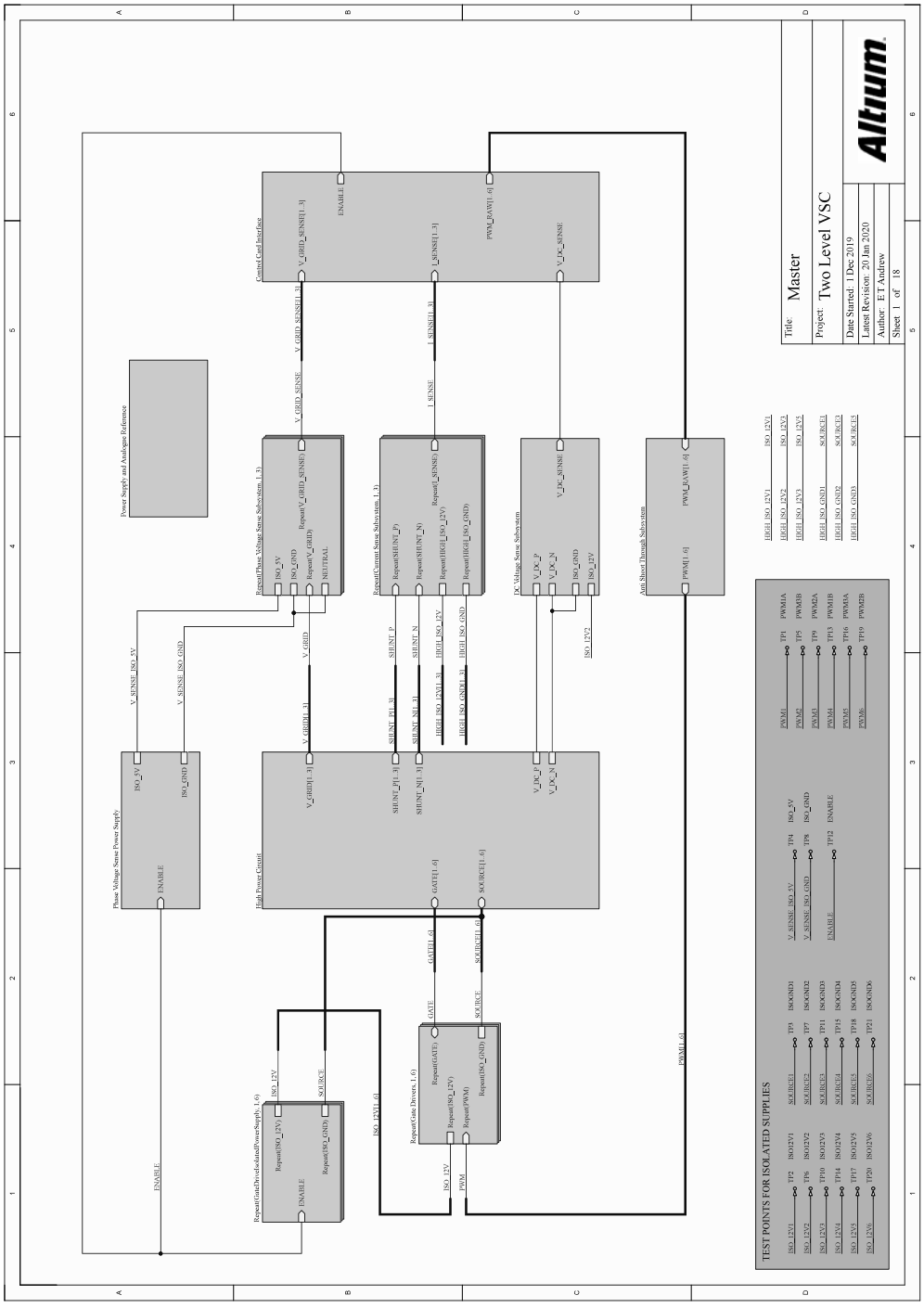
Suggestions for future work on the hardware prototype include:

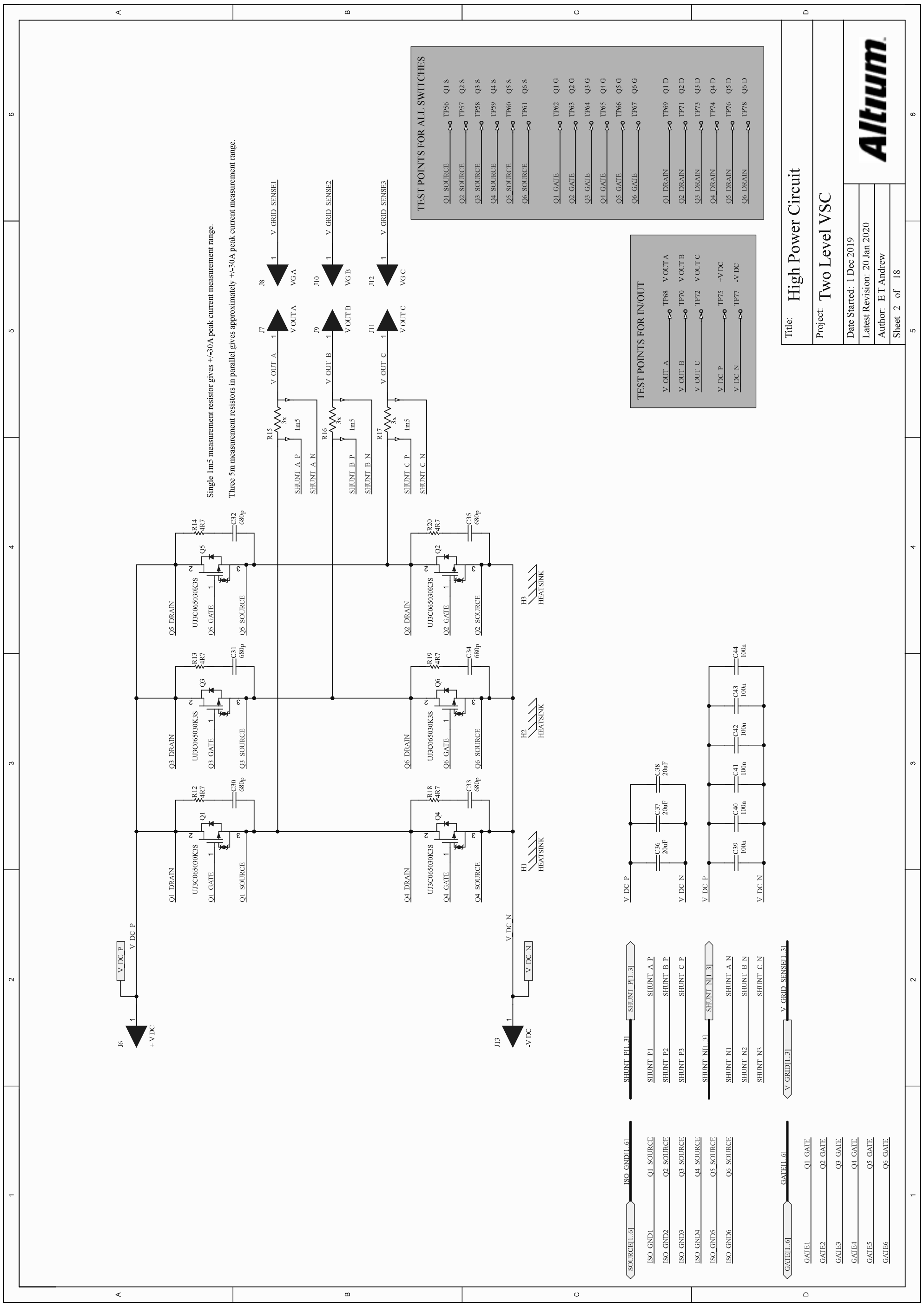
- Improvement in the robustness of the inverter by including over-current and switch desaturation protection.
- Implementation of hardware safing logic to protect against disconnection or failure of the embedded processor.
- Implementation of negative gate drive voltage output to allow standard SiC MOSFETs to be driven, improving flexibility.
- Implementation of USB2.0 communications for real-time data logging and plotting through a graphical user interface.

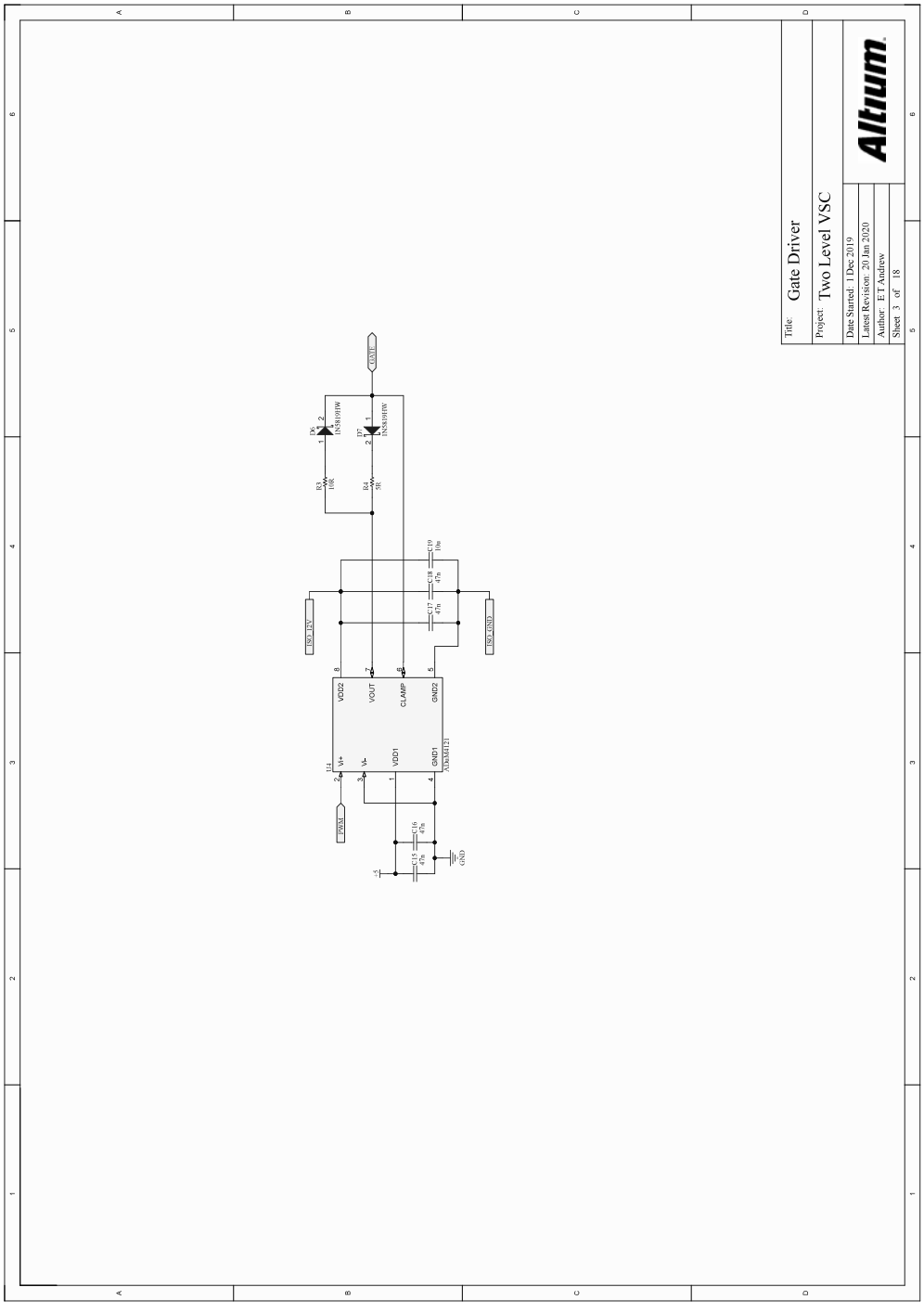
Appendix A

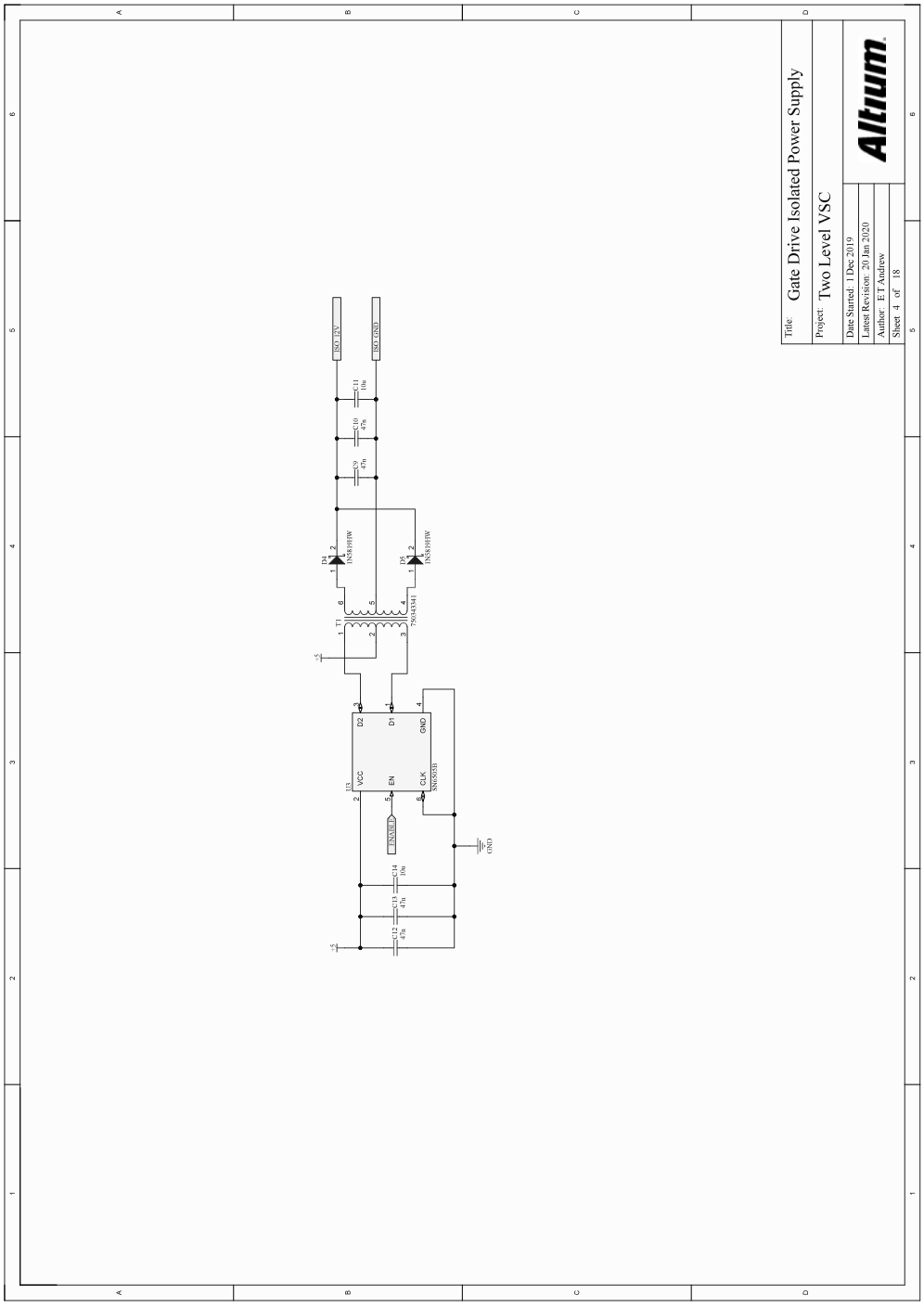
Converter Schematics

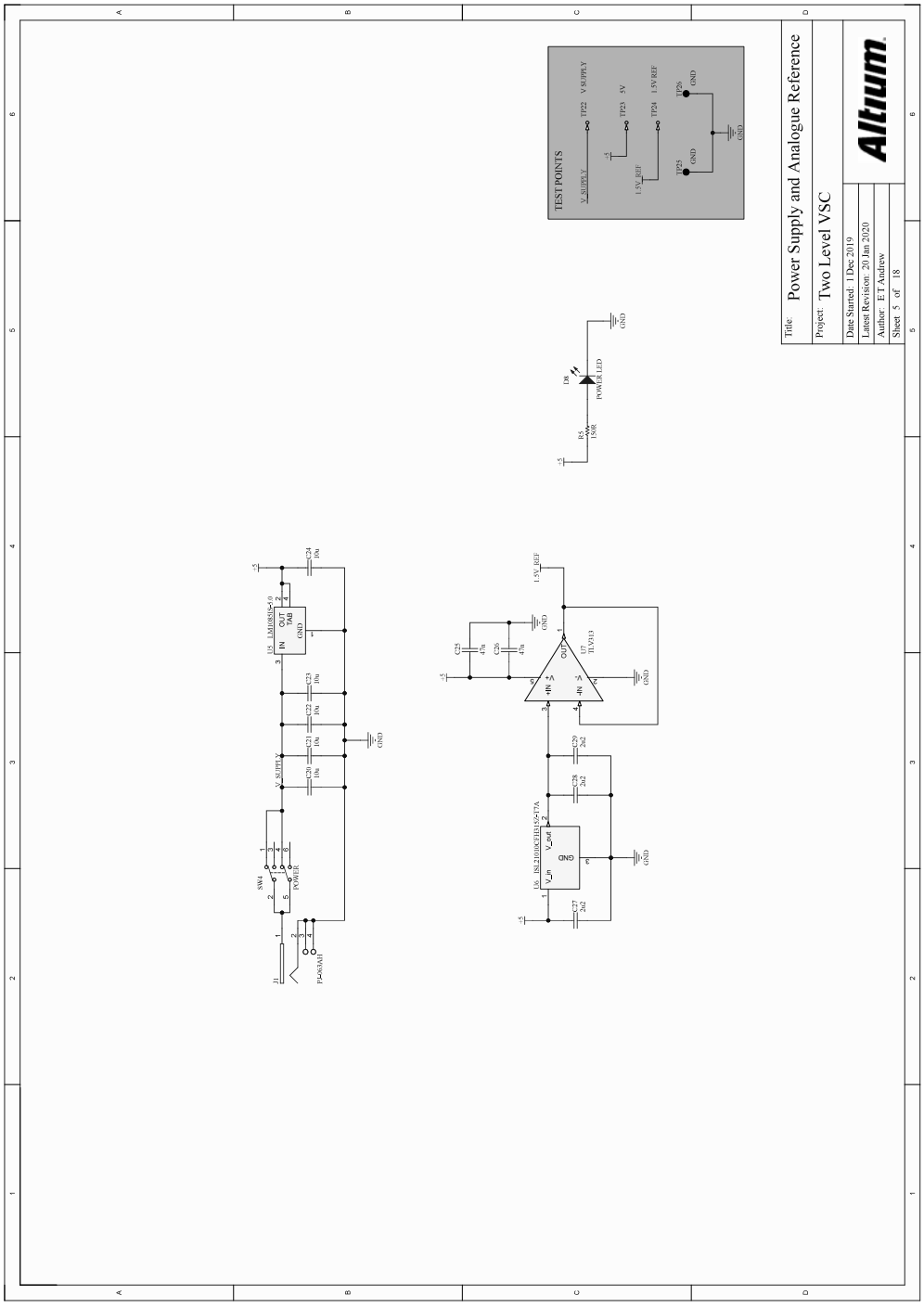
Appendix A. Converter Schematics

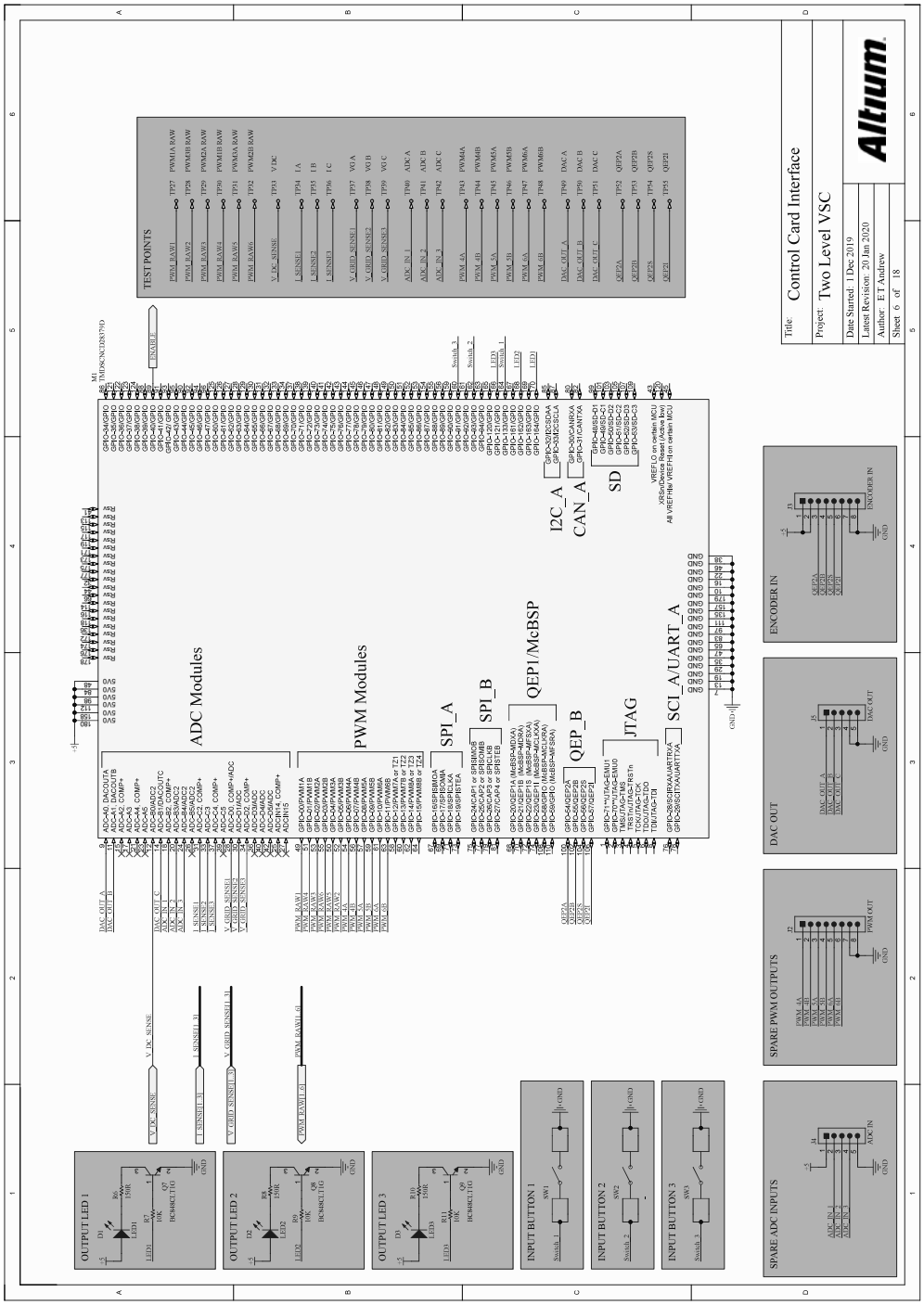


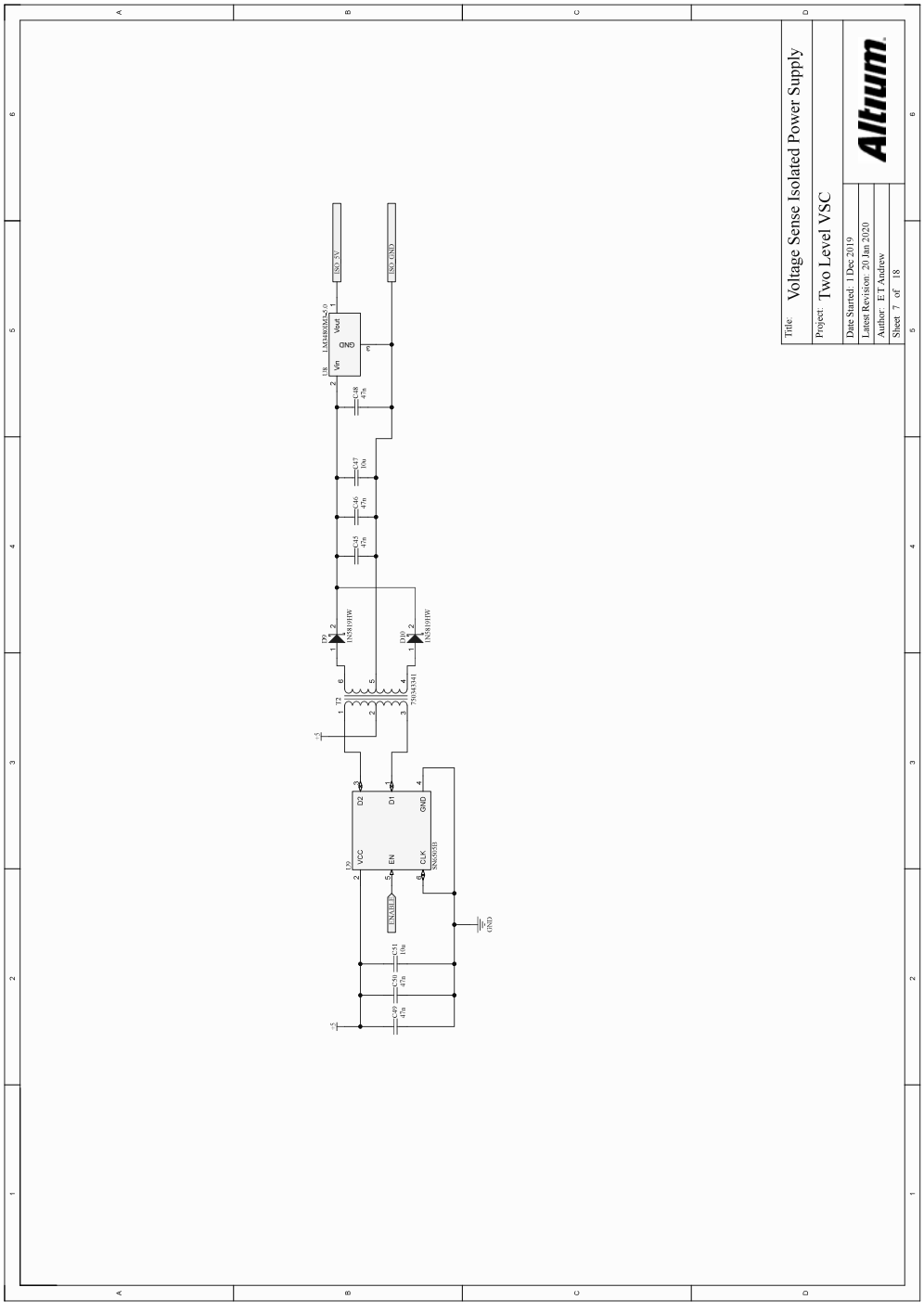

TEST POINTS FOR ALL SWITCHES
TEST POINTS FOR IN/OUT
Title: High Power Circuit
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: ET Andrew
Sheet 2 of 18

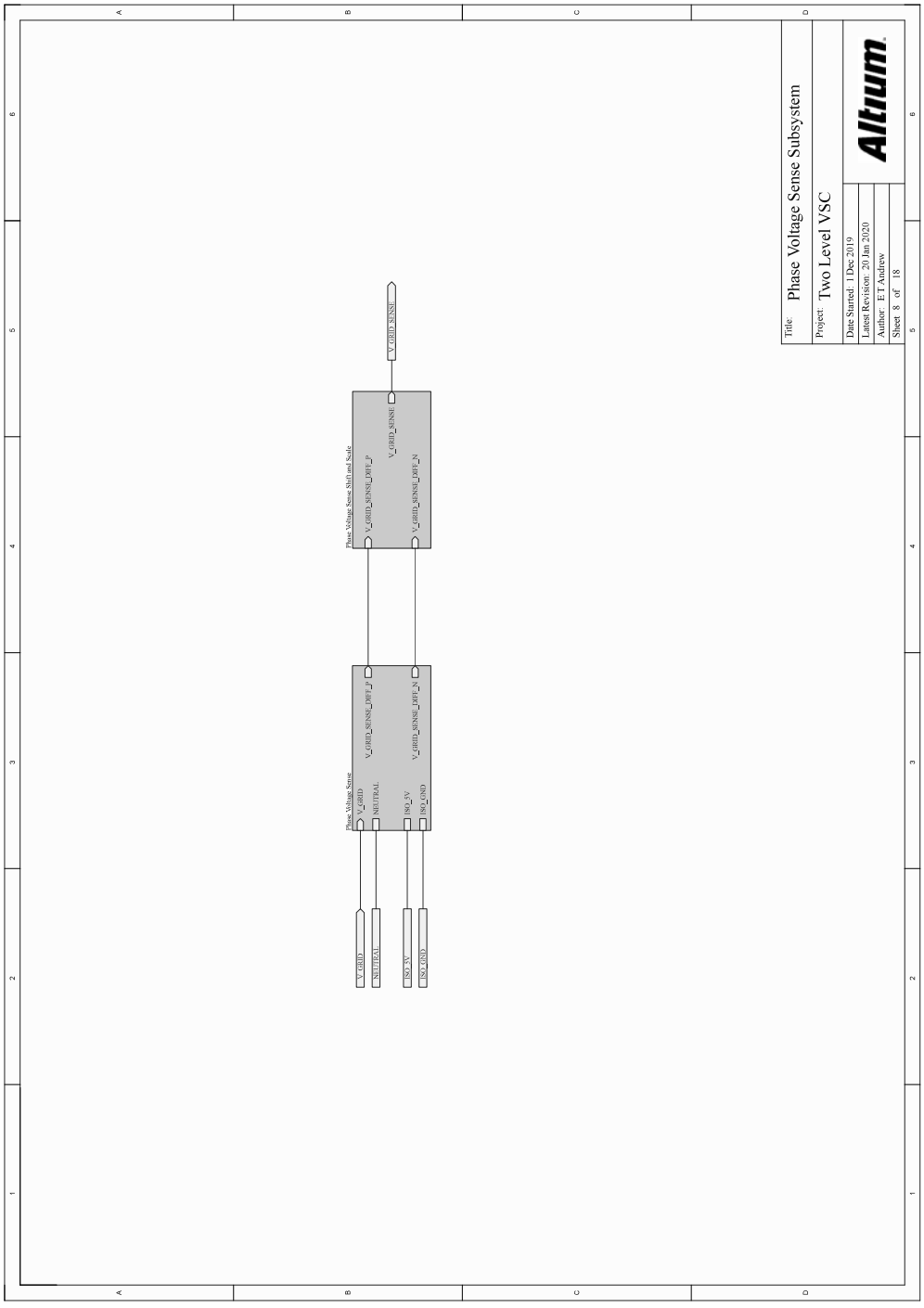

Title: Gate Driver
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 3 of 18
Altium
GATE
D8
1N5819HW
D7
1N5819HW
R3
10K
R4
5R
C19
10n
C18
47n
C17
47n
DSC_12V
DSC_GND
VDD2
VOUT
CLAMP
GND2
VDD1
GND1
U14
V+
V-
C15
47n
C16
47n
+5
GND

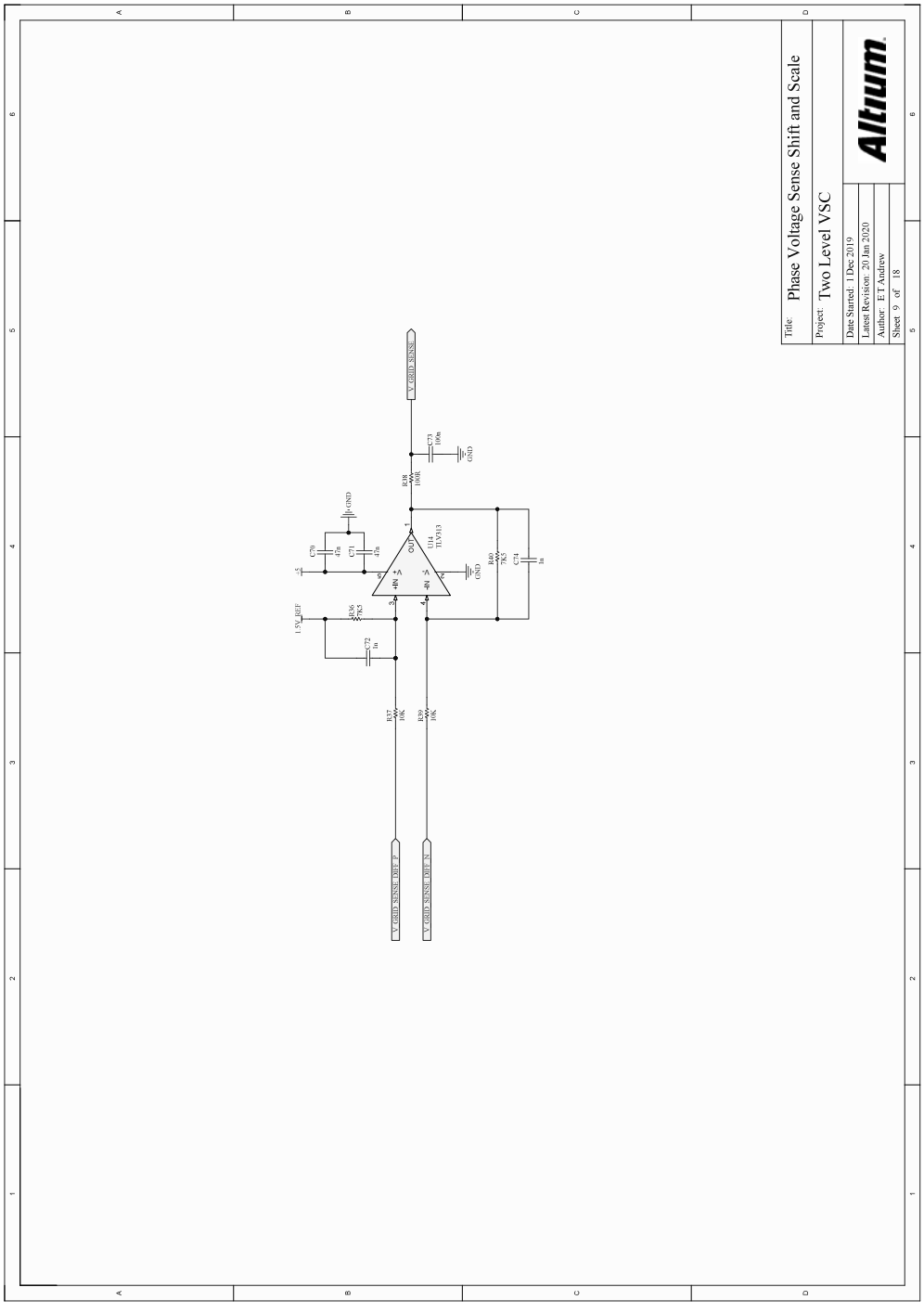

Title: Gate Drive Isolated Power Supply
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 4 of 18
Altium
ISO +12V
ISO GND
C11 10u
C10 47n
C9 47n
D4 1N5819HW
D5 1N5819HW
T1 750343641
+5
U3 VCC EN CLK D2 D1 GND SN6505B
ENABLE
GND
C14 10u
C13 47n
C12 47n
+5

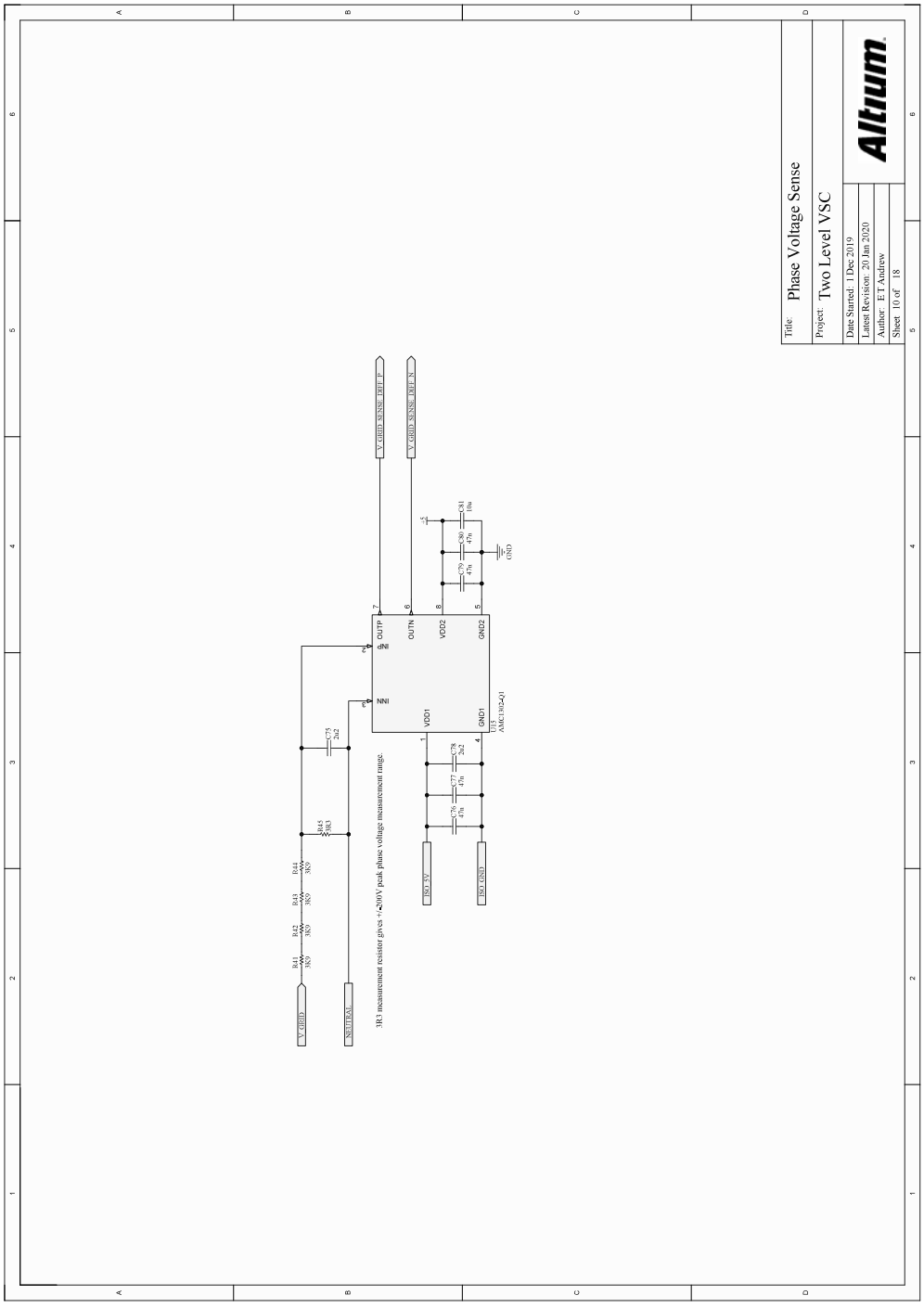

TEST POINTS
V_SUPPLY
TP22
TP23
TP24
TP25
TP26
5V
1.5V REF
GND
Title: Power Supply and Analogue Reference
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 5 of 18
Altium
POWERLED
SW4
POWER
LM1085S-3.0
TLV313
ISL21010CFH152F-T7A

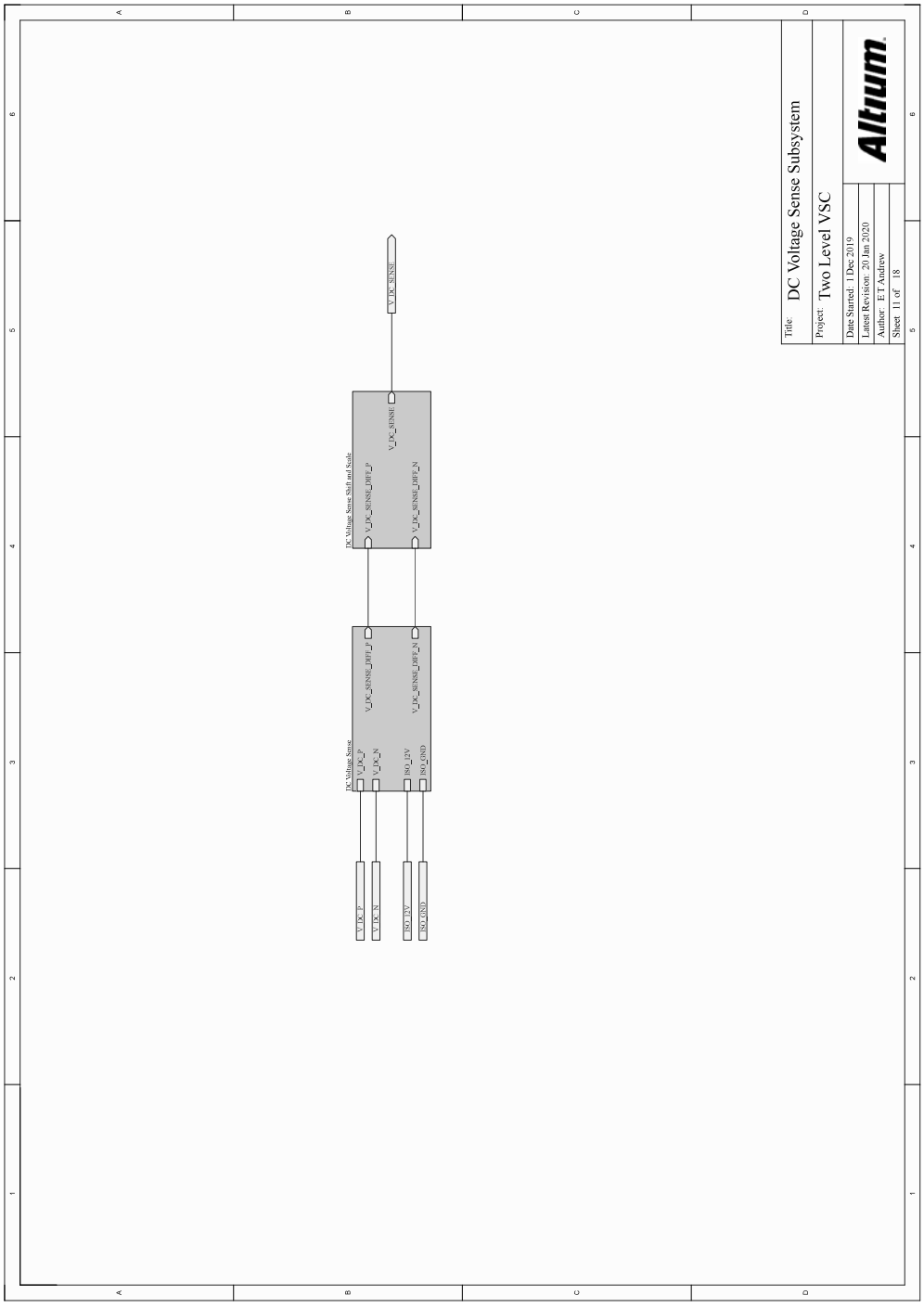

Title: Control Card Interface
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jun 2020
Author: E T Andrew
Sheet 6 of 18
Altium
TEST POINTS
ADC Modules
PWM Modules
SPI_A
SPI_B
QEP1/McBSP
QEP_B
JTAG
SCI_A/UART_A
I2C_A
CAN_A
SD
OUTPUT LED 1
OUTPUT LED 2
OUTPUT LED 3
INPUT BUTTON 1
INPUT BUTTON 2
INPUT BUTTON 3
SPARE ADC INPUTS
SPARE PWM OUTPUTS
DAC OUT
ENCODER IN

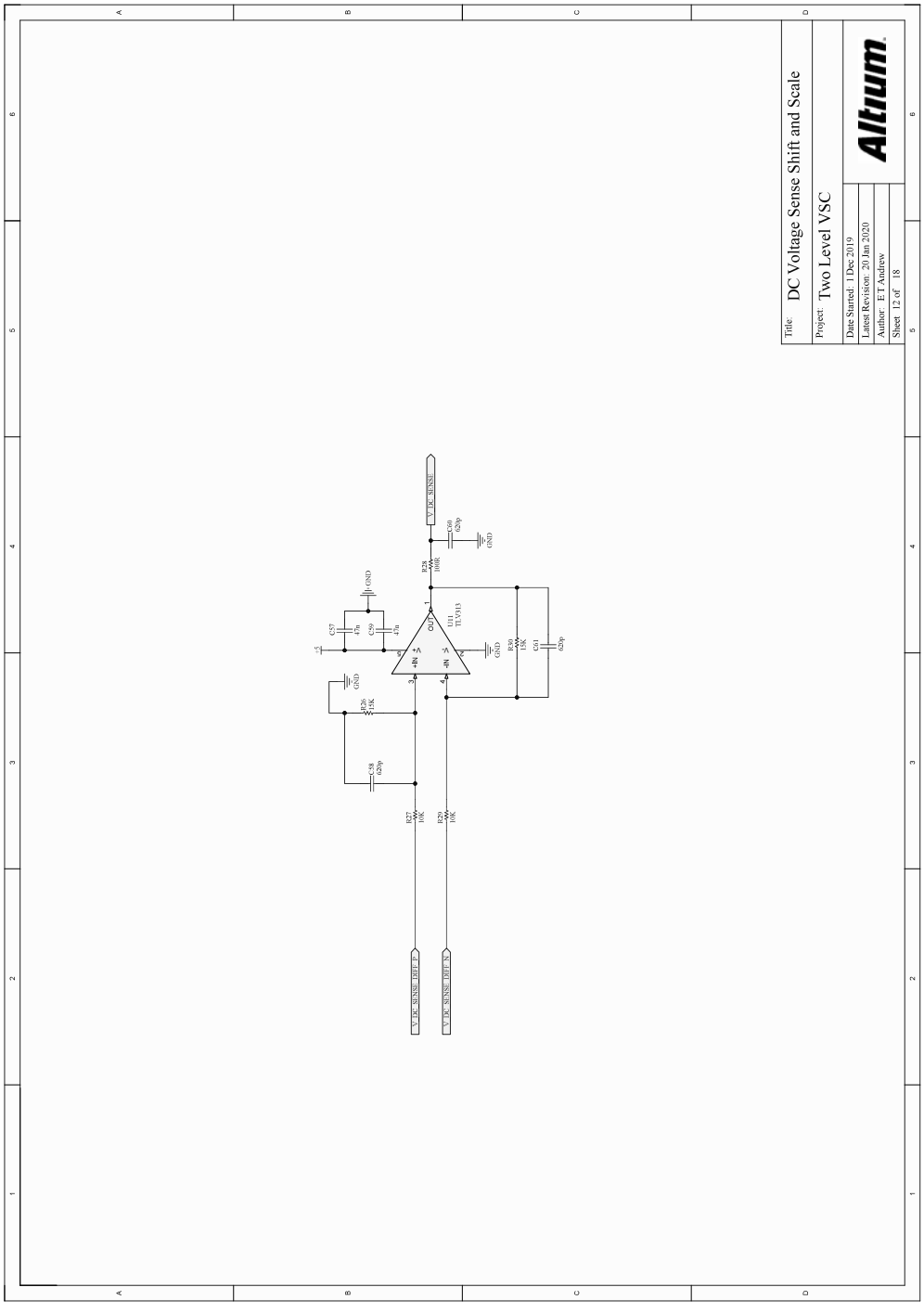

Title: Voltage Sense Isolated Power Supply
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 7 of 18
Altium
ISO +5V
ISO GND
LM1085IS-5.0
Vout
GND
Vin
U8
C48 47n
C47 10u
C46 47n
C45 47n
D9 1N5819HW
D10 1N5819HW
T7 750345341
+5
U9 VCC EN D2 D1 GND CLK SN6505B
LNK304LD
C51 10u
C50 47n
C49 47n
GND

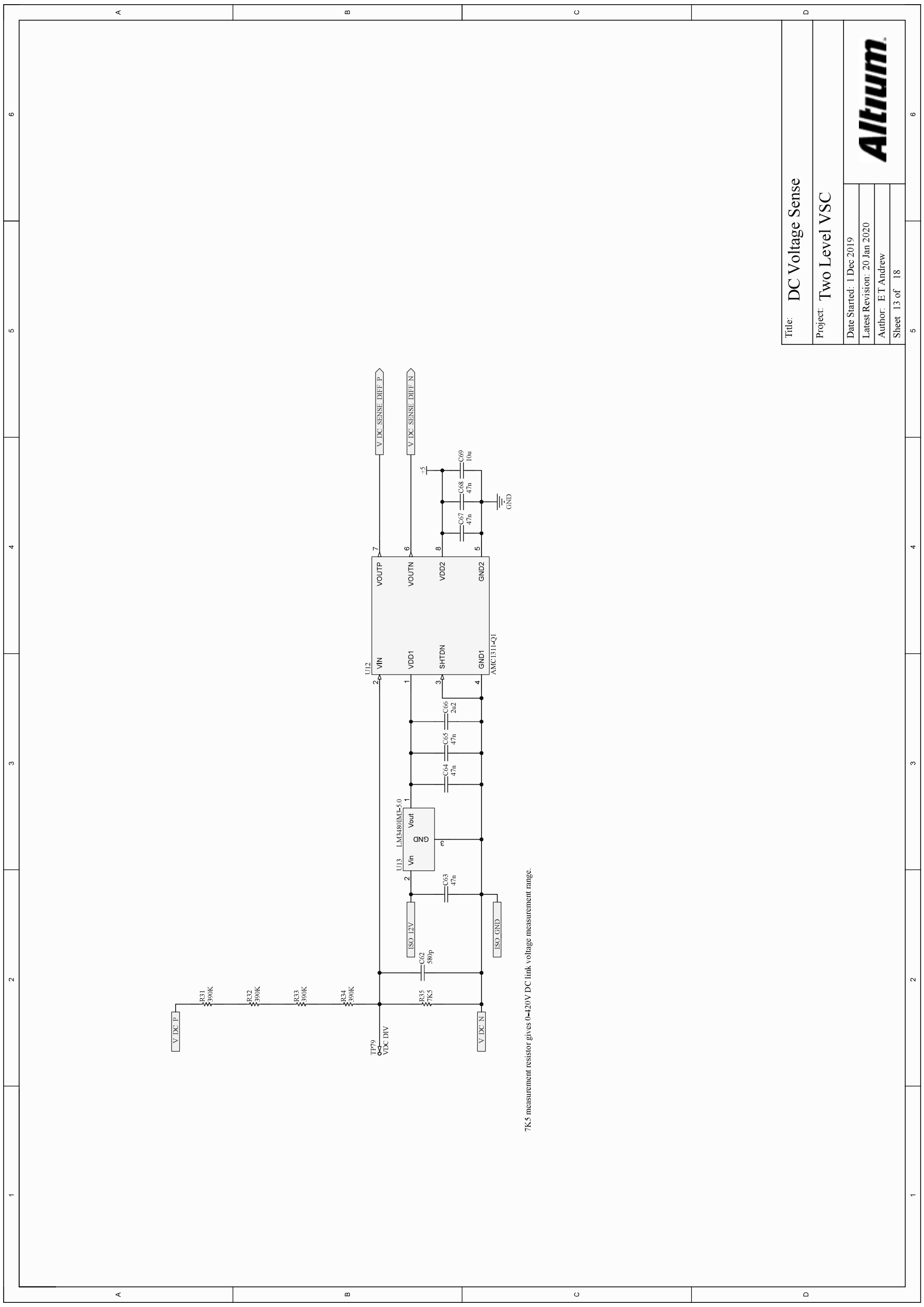

Phase Voltage Sense Subsystem
Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 8 of 18
Altium
Phase Voltage Sense
V_GRID
NEUTRAL
ISO_5V
ISO_GND
V_GRID_SENSE_DIFF_P
V_GRID_SENSE_DIFF_N
Phase Voltage Sense Shift and Scale
V_GRID_SENSE_DIFF_P
V_GRID_SENSE_DIFF_N
V_GRID_SENSE
V_GRID_SENSE

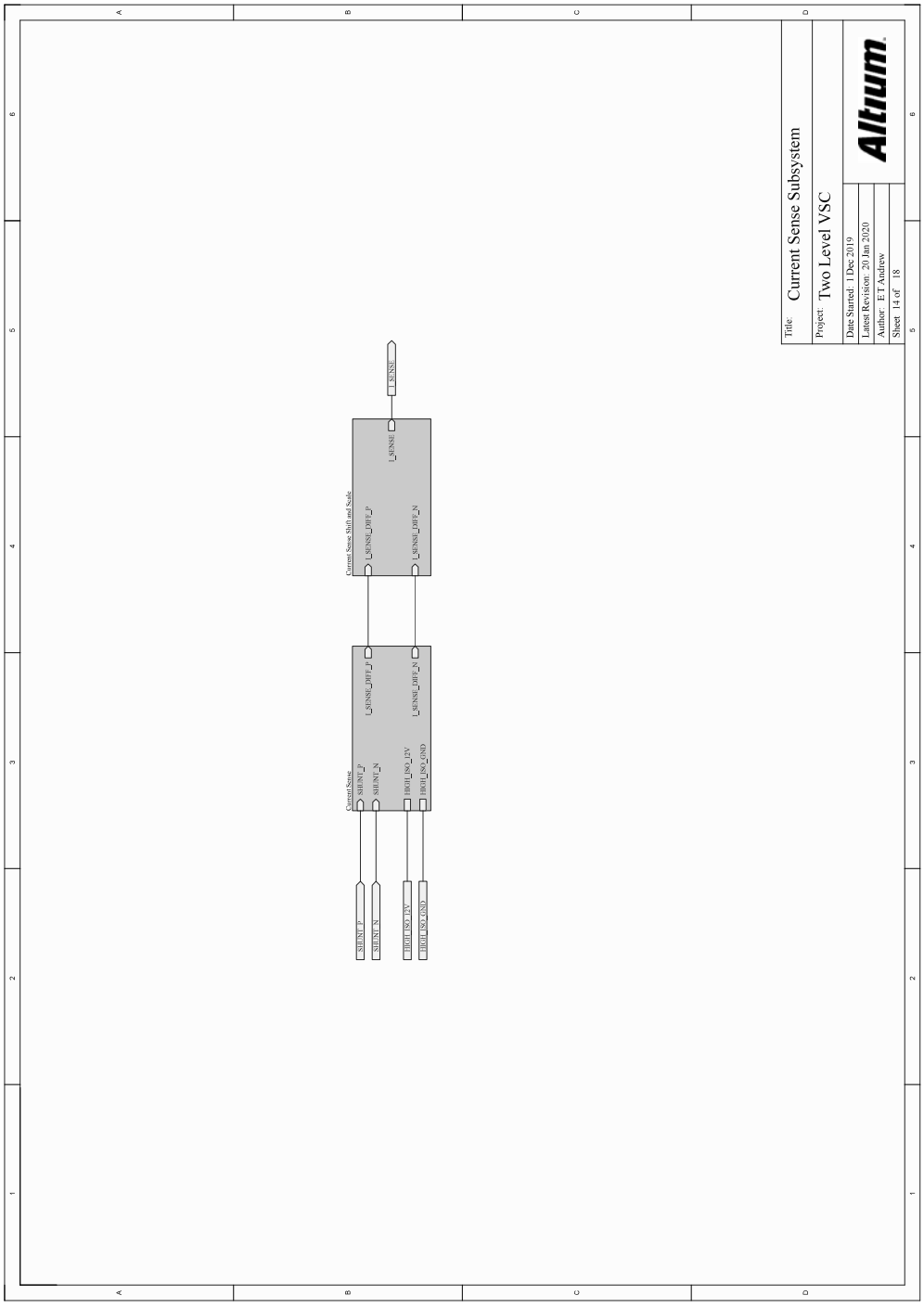

Title: Phase Voltage Sense Shift and Scale
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 9 of 18
Altium
V_GRID_SENSE
C73
100n
GND
R38
100R
GND
C70
47n
C71
47n
U14
TLV313
R40
2K
C74
1n
GND
1.5V_DIFF
R36
1K5
C72
1n
R37
10K
R39
10K
V_GRID_SENSE_DIFF_P
V_GRID_SENSE_DIFF_N

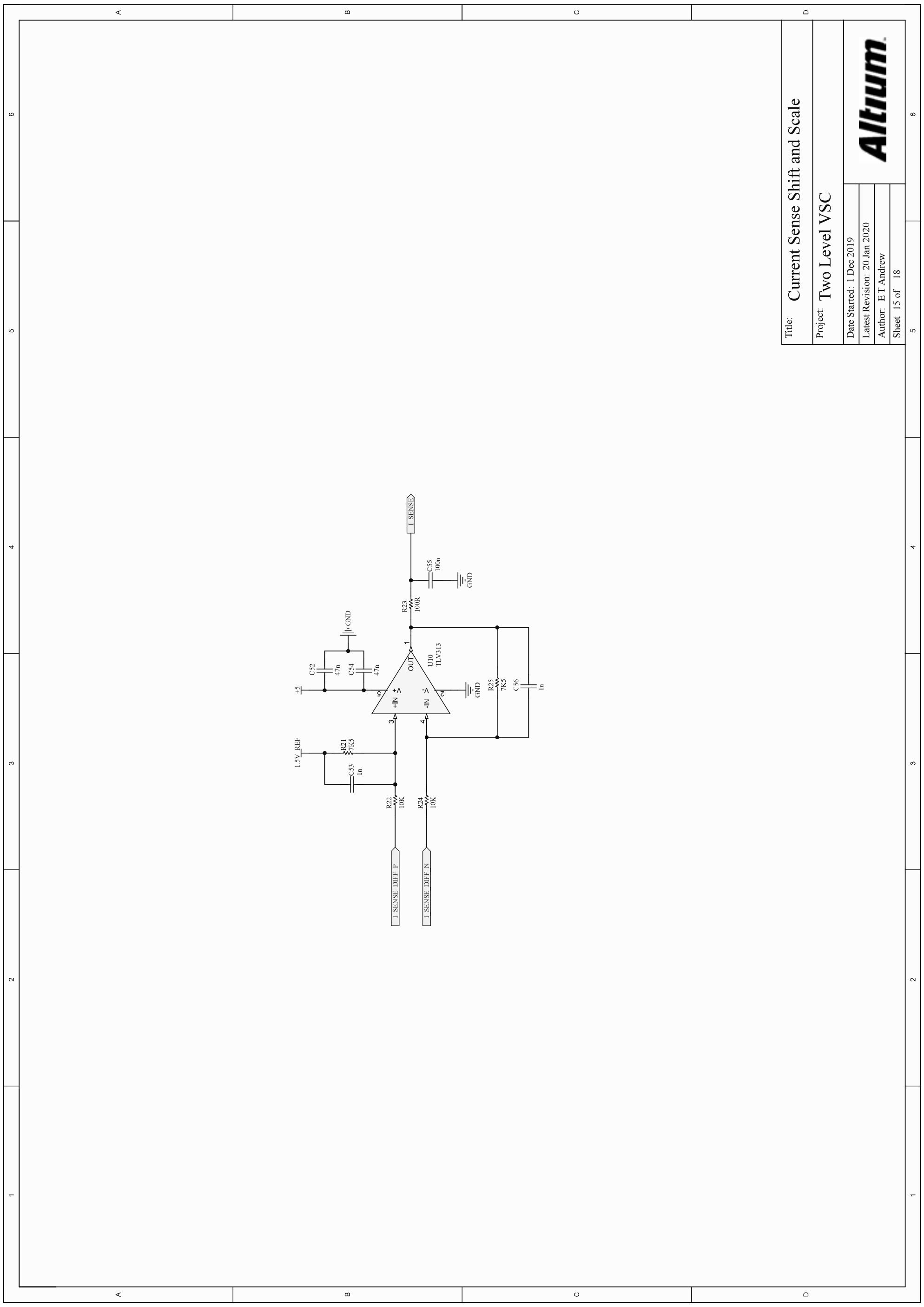

Title: Phase Voltage Sense
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 10 of 18
Altium
V_GRID_SENSE_DIFF_P
V_GRID_SENSE_DIFF_N
OUTP
OUTN
VDD2
GND2
INP
INN
VDD1
GND1
ISO7230CDWR
AMC1302-Q1
C84 10u
C80 47n
C79 47n
GND
C75 2n2
R45 39R3
R44 30R
R43 30R
R42 30R
R41 30R
C78 2n2
C77 47n
C76 47n
ISO_5V
ISO_GND
V_GRID
NEUTRAL
39R3 measurement resistor gives +/-290V peak phase voltage measurement range.

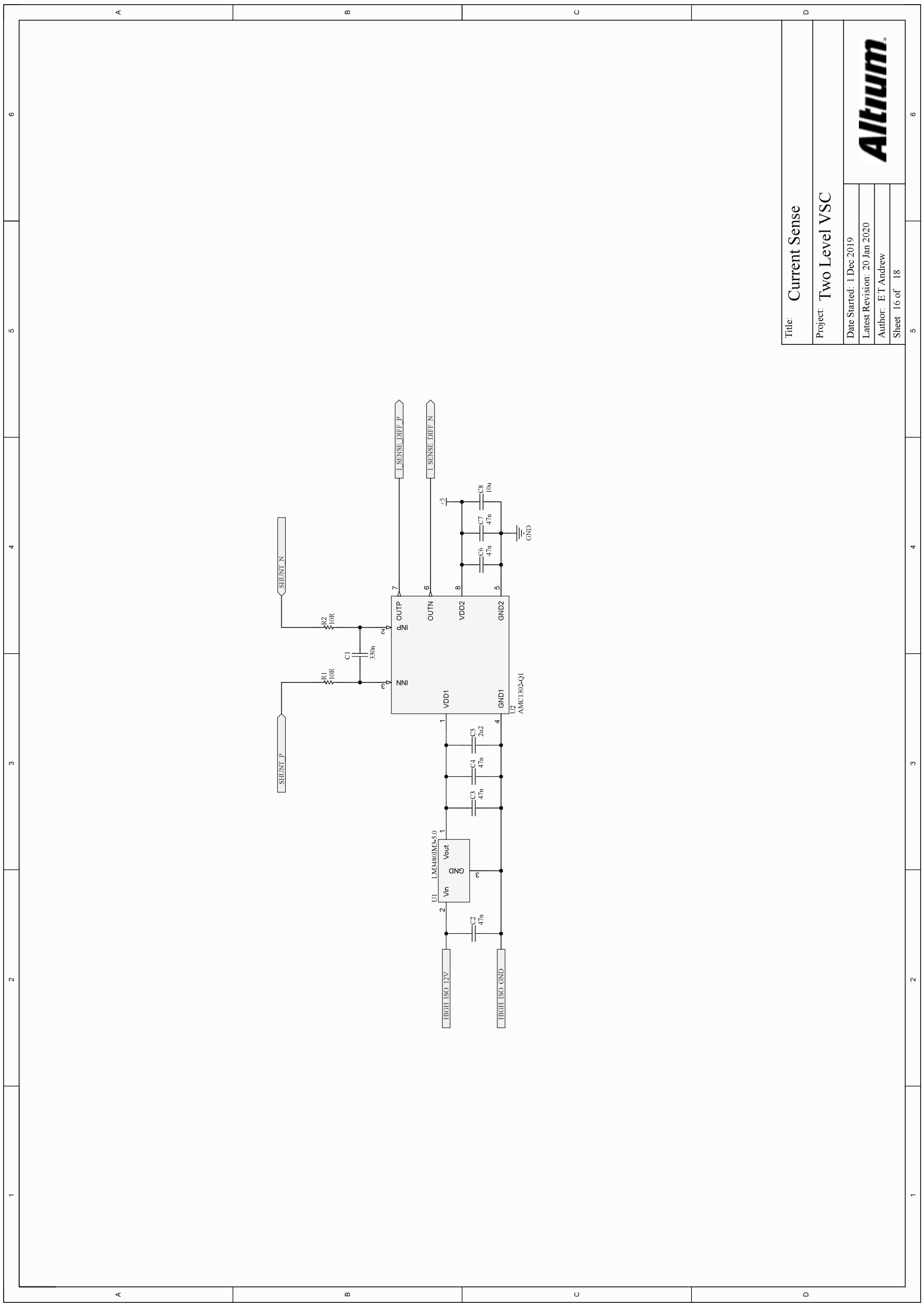

DC Voltage Sense Subsystem
Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 11 of 18
Altium
V_DC_SENSE
DC Voltage Sense Shift and Scale
V_DC_SENSE_DIFF_P
V_DC_SENSE_DIFF_N
DC Voltage Sense
V_DC_P
V_DC_N
ISO_12V
ISO_GND

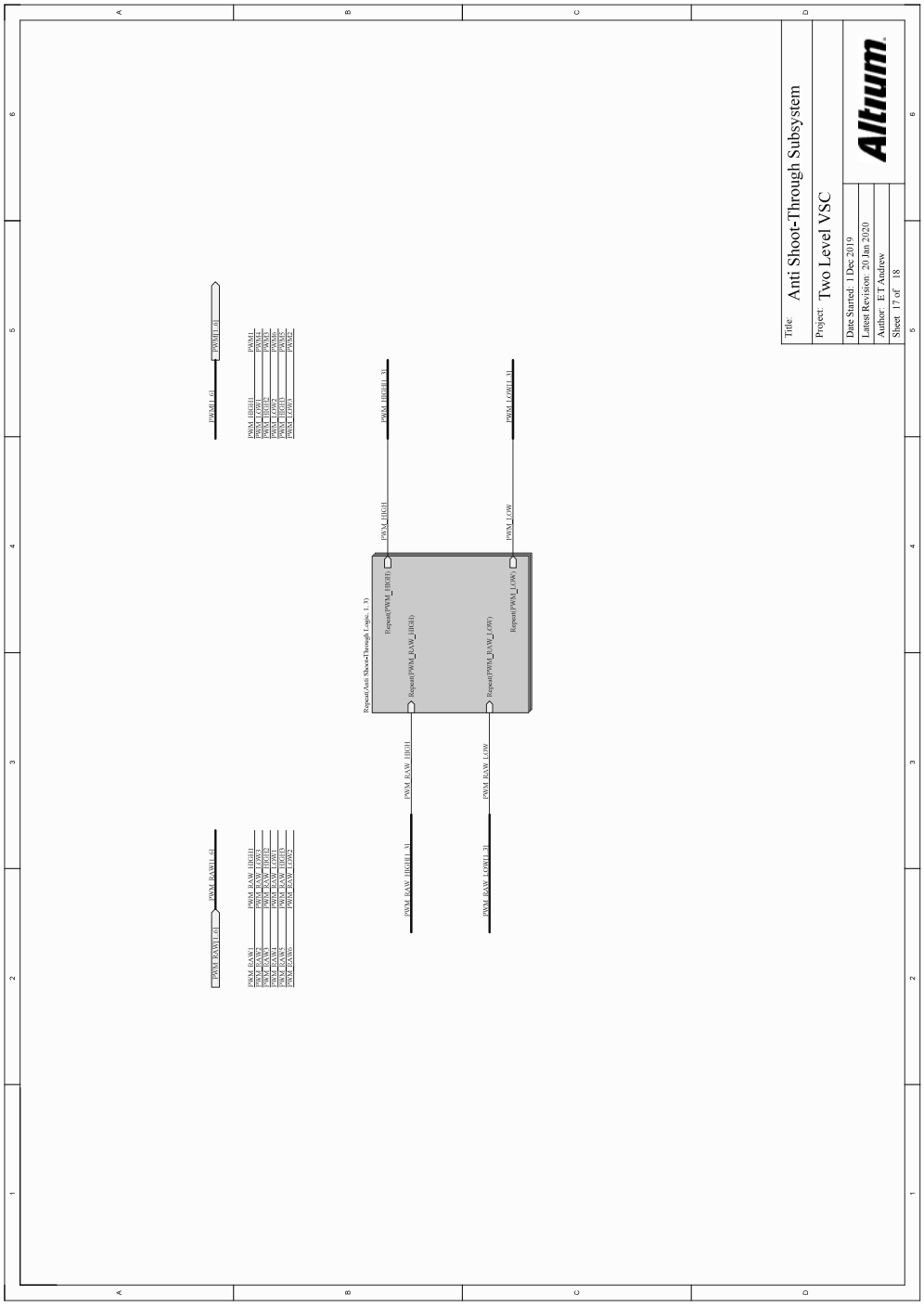

Title: DC Voltage Sense Shift and Scale
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 12 of 18
Altium
V_DC_SENSE
C60 620p
GND
R28 100K
GND
C57 47n
C59 47n
U11 TLV313
OUT
+IN
-IN
V+
V-
GND
R30 15K
C61 620p
R26 15K
GND
C58 620p
R27 10K
R29 10K
V_DC_SENSE_DIFF_P
V_DC_SENSE_DIFF_N

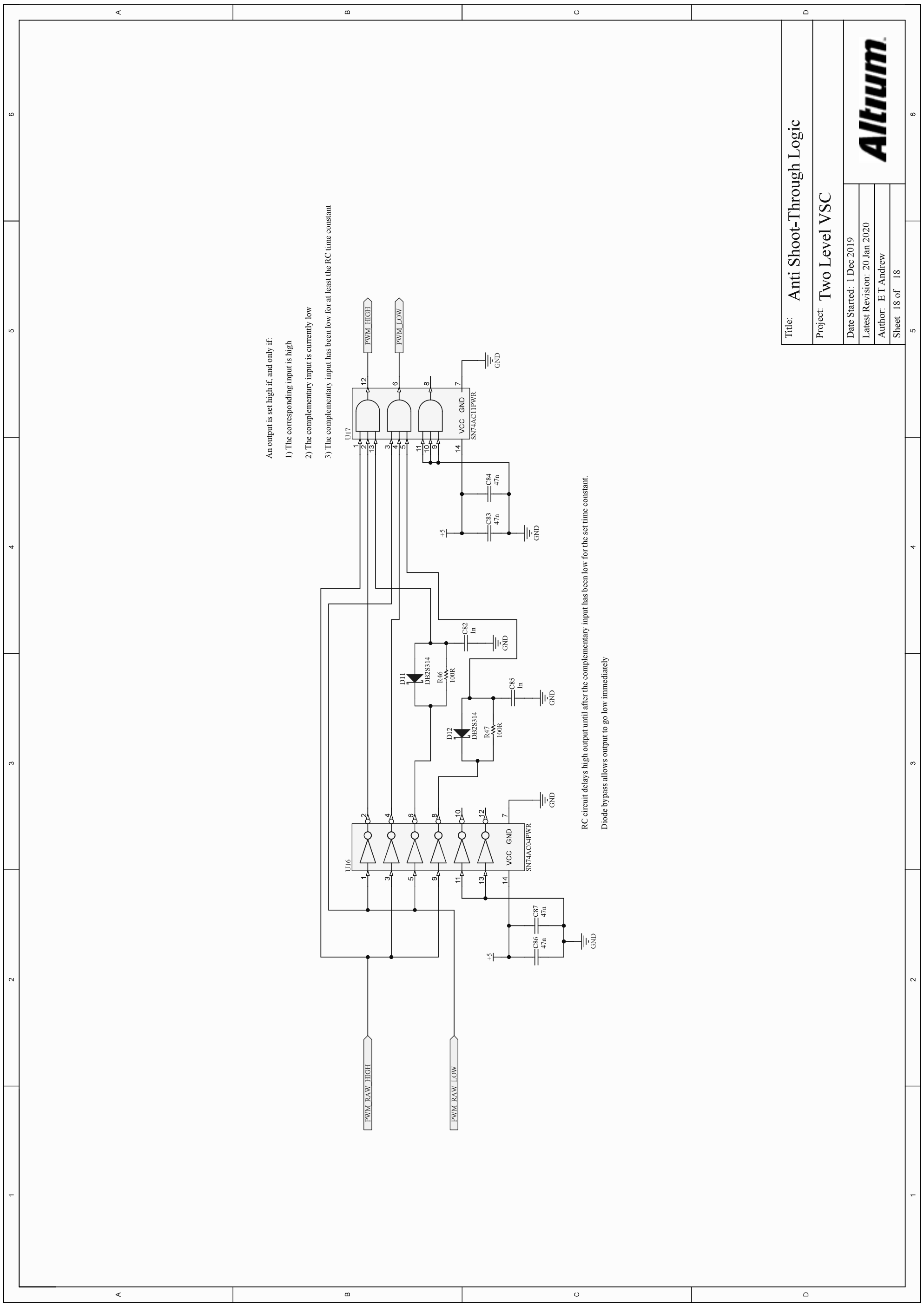

Title: DC Voltage Sense
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: ET Andrew
Sheet 13 of 18
7K5 measurement resistor gives 0-420V DC link voltage measurement range.


Current Sense
SHUNT_P
SHUNT_N
HOST_SIG_12V
HOST_SIG_GND
L_SENSE_DIFF_P
L_SENSE_DIFF_N
Current Sense Shift and Scale
L_SENSE
L_SENSE
L_SENSE_DIFF_P
L_SENSE_DIFF_N
Title: Current Sense Subsystem
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 14 of 18
Altium


Title: Current Sense Shift and Scale
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: ET Andrew
Sheet 15 of 18
U10
TLV313
I_SENSE_DIFF_P
I_SENSE_DIFF_N
1.5V_REF
GND


Title: Current Sense
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: ET Andrew
Sheet 16 of 18
Altium
SHUNT_P
SHUNT_N
I_SENSE_DIFF_P
I_SENSE_DIFF_N
HIGH_ISO_12V
HIGH_ISO_GND
AMC1302-Q1
LM3480IM3-5.0
GND


Title: Anti Shoot-Through Subsystem
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: E T Andrew
Sheet 17 of 18
Altium
PWM_RAW[1..6]
PWM_RAW1
PWM_RAW2
PWM_RAW3
PWM_RAW4
PWM_RAW5
PWM_RAW6
PWM_RAW_HIGH[1..3]
PWM_RAW_LOW[1..3]
PWM_RAW_HIGH1
PWM_RAW_LOW1
Repeat/Anti Shoot-Through Logics_1_3
Repeat(PWM_HIGH)
Repeat(PWM_RAW_HIGH)
Repeat(PWM_RAW_LOW)
Repeat(PWM_LOW)
PWM_HIGH[1..3]
PWM_LOW[1..3]
PWM_HIGH1
PWM_LOW1
PWM[1..6]
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6


Title: Anti Shoot-Through Logic
Project: Two Level VSC
Date Started: 1 Dec 2019
Latest Revision: 20 Jan 2020
Author: ET Andrew
Sheet 18 of 18
Altium
An output is set high if, and only if:
1) The corresponding input is high
2) The complementary input is currently low
3) The complementary input has been low for at least the RC time constant
RC circuit delays high output until after the complementary input has been low for the set time constant.
Diode bypass allows output to go low immediately
PWM_HIGH
PWM_LOW
PWM_RAW_HIGH
PWM_RAW_LOW
U17
SN74AC11PWR
U16
SN74AC04PWR
GND

Appendix B

Selected Software Extracts

B.1 Implementation of the Digital Biquad Filter

The function in Listing B.1 implements a biquad filter with selectable channel count and filter order.

Listing B.1: C code implementation of the digital biquad filter

```
1  void biquad_update (biquad_data * p_data)
2  {
3     float32_t b0 = 0;
4     float32_t b1 = 0;
5     float32_t b2 = 0;
6     float32_t a1 = 0;
7     float32_t a2 = 0;
8     uint16_t curr_chan = 0;
9     uint16_t curr_sec = 0;
10
11    for(curr_chan = 0; curr_chan < p_data->n_channels; curr_chan++)
12    {
13       for(curr_sec = 0; curr_sec < p_data->n_sections; curr_sec++)
14       {
15          if(curr_sec != 0)
16          {
17             p_data->x[curr_chan] = p_data->y[curr_chan];
18          }
19
20          b0 = p_data->p_coeffs[curr_sec][0];
21          b1 = p_data->p_coeffs[curr_sec][1];
22          b2 = p_data->p_coeffs[curr_sec][2];
23          a1 = p_data->p_coeffs[curr_sec][4];
24          a2 = p_data->p_coeffs[curr_sec][5];
25
26          p_data->y[curr_chan] = b0 * p_data->x[curr_chan] +
                p_data->s1_k_1[curr_chan][curr_sec];
27
28          p_data->s1_k = p_data->s2_k_1[curr_chan][curr_sec] +
                b1*p_data->x[curr_chan] - a1*p_data->y[curr_chan];
```

```
29
30          p_data->s2_k = b2*p_data->x[curr_chan] - a2*p_data->y[curr_chan];
31
32          p_data->s1_k_1[curr_chan][curr_sec] = p_data->s1_k;
33          p_data->s2_k_1[curr_chan][curr_sec] = p_data->s2_k;
34       }
35    }
36    return;
37 }
```

The biquad filter shown in Listing B.1 requires filter coefficients to realise the required filter response. The filter coefficients can easily be calculated using the second order segments 'sos' function in Matlab as shown in B.2. The coefficients are then printed using C code array syntax so that they can be copied and pasted straight into the microcontroller code.

Listing B.2: Matlab script to compute biquad filter coefficients

```
1  clear all; close all; clc;
2
3  %% Section 1 - Design an n-th Order Butterworth Filter
4  n = 1; % Filter Order
5  fc = 8000; % Cutoff frequency
6  fs = 20000; % Sampling frequency
7  Ts = 1/fs; % Sampling Period
8  ftype = 'low'; % Filter type
9
10 [z,p,k] = butter(n,fc/(fs/2),ftype);
11 sos = zp2sos(z,p,k);
12
13 %% Section 2 - Output the SOS Coefficients in a C code Matrix Format
14 fprintf("{\n");
15 for row = 1:ceil(n/2)
16    if row == ceil(n/2)
17       fprintf("\t{%f, %f, %f, %f, %f, %f}\n", sos(ceil(n/2),:));
18    else
19       fprintf("\t{%f, %f, %f, %f, %f, %f},\n", sos(row,:));
20    end
21 end
22 fprintf("};\n");
```

B.2 Implementation of the Extended Complex Kalman Filter

The function in Listing B.3 implements an extended complex kalman filter update step.

Listing B.3: C code implementation of the extended complex kalman filter

```
1  void kalman_update (kalman_data * p_data)
```

```
2  {
3     comp_num temp_a;
4     comp_num temp_b;
5
6     #include "temp.h"
7
8     // A priori state estimate, X_apriori
9     p_data->pp_X_apriori[0][0] = p_data->pp_X_apost[0][0];
10    comp_mul((*(p_data->pp_X_apost+1)+0),(*(p_data->pp_X_apost+0)+0),
          (*(p_data->pp_X_apriori+1)+0));
11    comp_div((*(p_data->pp_X_apost+2)+0),(*(p_data->pp_X_apost+0)+0),
          (*(p_data->pp_X_apriori+2)+0));
12
13    // Linearised state transition matrix, F
14    p_data->pp_F[0][0].real = 1;
15    p_data->pp_F[0][0].imag = 0;
16    p_data->pp_F[0][1].real = 0;
17    p_data->pp_F[0][1].imag = 0;
18    p_data->pp_F[0][2].real = 0;
19    p_data->pp_F[0][2].imag = 0;
20    p_data->pp_F[1][0] = p_data->pp_X_apost[1][0];
21    p_data->pp_F[1][1] = p_data->pp_X_apost[0][0];
22    p_data->pp_F[1][2].real = 0;
23    p_data->pp_F[1][2].imag = 0;
24    comp_mul((*(p_data->pp_X_apost+0)+0),(*(p_data->pp_X_apost+0)+0), &temp_a);
25    comp_div((*(p_data->pp_X_apost+2)+0), &temp_a, &temp_b);
26    comp_mul_real_scalar(&temp_b, -1, &temp_a);
27    p_data->pp_F[2][0] = temp_a;
28    p_data->pp_F[2][1].real = 0;
29    p_data->pp_F[2][1].imag = 0;
30    temp_a.real = 1;
31    temp_a.imag = 0;
32    comp_div(&temp_a,(*(p_data->pp_X_apost+0)+0), &temp_b);
33    p_data->pp_F[2][2] = temp_b;
34
35    // A priori process covariance matrix, P_apriori
36    comp_mat_mul(p_data->pp_F, p_data->pp_P_apost, temp_mat_a, 3, 3, 3); //
          Compute F*P_k_1
37    comp_mat_conj_trans (p_data->pp_F, temp_mat_b, 3, 3); // Compute F'
38    comp_mat_mul(temp_mat_a, temp_mat_b, temp_mat_c, 3, 3, 3); // Compute
          F*P_k_1*F'
39
40    comp_mat_add(temp_mat_c, p_data->pp_Q, p_data->pp_P_apriori, 3, 3); //
          Compute P_k = F*P_k_1*F' + Q;
41
42    // The measurement residual, Y
43    comp_mat_mul(p_data->pp_H, p_data->pp_X_apriori, temp_mat_f, 1, 3, 1); //
          Compute H*X_apriori
44    comp_mat_sub(p_data->pp_Z, temp_mat_f, p_data->pp_Y, 1, 1); // Compute Z -
          H*X_apriori
45
46    // The Kalman gain matrix, K
47    comp_mat_mul(p_data->pp_P_apriori, p_data->pp_H_t, temp_mat_d, 3, 3, 1);
          // Compute P_k*H'
48    comp_mat_mul(p_data->pp_H, p_data->pp_P_apriori, temp_mat_e, 1, 3, 3); //
          Compute H*P_k
49    comp_mat_mul(temp_mat_e, p_data->pp_H_t, temp_mat_f, 1, 3, 1); // Compute
          H*P_k*H'
50    comp_mat_add(p_data->pp_R, temp_mat_f, temp_mat_g, 1, 1); // Compute R +
          H*P_k*H'
51    comp_mat_inv (temp_mat_g, temp_mat_f, 1); // Compute inv(R + H*P_k*H')
52    comp_mat_mul(temp_mat_d, temp_mat_f, p_data->pp_K, 3, 1, 1); // Compute
```

```
        P_k*H' * inv(R + H*P_k*H')
53
54      // A posteriori state estimate, X_apost
55      comp_mat_mul(p_data->pp_K, p_data->pp_Y, temp_mat_d, 3, 1, 1); // K*Y
56      comp_mat_add(p_data->pp_X_apriori, temp_mat_d, p_data->pp_X_apost, 3, 1);
            // Compute X_apriori + K*Y
57
58      // A posteriori process covariance matrix, P_apost
59      comp_mat_mul(p_data->pp_K, p_data->pp_H, temp_mat_a, 3, 1, 3); // K*H
60      comp_mat_sub(p_data->pp_I, temp_mat_a, temp_mat_b, 3, 3); // Compute I -
            K*H
61      comp_mat_mul(temp_mat_b, p_data->pp_P_apriori, p_data->pp_P_apost, 3, 3,
            3); // Compute (I - K*H)*P
62
63      temp_mat_f[0][0].real = 0;
64      temp_mat_f[0][0].imag = 0;
65
66      return;
67  }
```

B.3 Implementation of MMPC Modulation Stage

The function in Listing B.4 calculates and sets the counter/compare values for a centre-aligned PWM module to output two active vectors and two zero vectors with the specified dwell times.

Listing B.4: C code calculation of counter/compare values to output given vectors with given dwell times

```
1   void peripheral_epwm_set_vector_dwell (uint16_t pwm_half_period,
2   uint16_t vec_one,
3   uint16_t vec_two,
4   float32_t raw_duty_one,
5   float32_t raw_duty_two)
6   {
7      float32_t duty_zero = 0;
8      float32_t duty_one = 0;
9      float32_t duty_two = 0;
10     float32_t raw_duty_zero = 0;
11     float32_t duty_zero_over_two = 0;
12     float32_t duty_a = 0;
13     float32_t duty_b = 0;
14     float32_t duty_c = 0;
15     float32_t compare_a = 0;
16     float32_t compare_b = 0;
17     float32_t compare_c = 0;
18
19     // Saturate duty cycles between 0 and 1
20     if(raw_duty_one >= 1){duty_one = 1;}
21     else if(raw_duty_one <= 0){duty_one = 0;}
22     else {duty_one = raw_duty_one;}
23
24     if(raw_duty_two >= (1-raw_duty_one)){duty_two = (1-raw_duty_one);}
25     else if(raw_duty_two <= 0){duty_two = 0;}
```

```
26      else {duty_two = raw_duty_two;}
27
28      raw_duty_zero = 1 - duty_one - duty_two;
29
30      if(raw_duty_zero >= 1){duty_zero = 1;}
31      else if(raw_duty_zero <= 0){duty_zero = 0;}
32      else {duty_zero = raw_duty_zero;}
33
34      duty_zero_over_two = duty_zero/2;
35
36      // Phase A
37      duty_a = duty_zero_over_two;
38      if((vec_one == 1)||(vec_one == 2)||(vec_one == 6))
39      {
40      duty_a = duty_a + duty_one;
41      }
42      if((vec_two == 1)||(vec_two == 2)||(vec_two == 6))
43      {
44      duty_a = duty_a + duty_two;
45      }
46
47      // Phase B
48      duty_b = duty_zero_over_two;
49      if((vec_one == 2)||(vec_one == 3)||(vec_one == 4))
50      {
51      duty_b = duty_b + duty_one;
52      }
53      if((vec_two == 2)||(vec_two == 3)||(vec_two == 4))
54      {
55      duty_b = duty_b + duty_two;
56      }
57
58      // Phase C
59      duty_c = duty_zero_over_two;
60      if((vec_one == 4)||(vec_one == 5)||(vec_one == 6))
61      {
62      duty_c = duty_c + duty_one;
63      }
64      if((vec_two == 4)||(vec_two == 5)||(vec_two == 6))
65      {
66      duty_c = duty_c + duty_two;
67      }
68
69      compare_a = pwm_half_period - duty_a*pwm_half_period;
70      compare_b = pwm_half_period - duty_b*pwm_half_period;
71      compare_c = pwm_half_period - duty_c*pwm_half_period;
72
73      EPWM_setCounterCompareValue(EPWM1_BASE, EPWM_COUNTER_COMPARE_A, compare_a);
74      EPWM_setCounterCompareValue(EPWM2_BASE, EPWM_COUNTER_COMPARE_A, compare_b);
75      EPWM_setCounterCompareValue(EPWM3_BASE, EPWM_COUNTER_COMPARE_A, compare_c);
76
77      return;
78  }
```

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