University of Strathclyde

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Multilevel Voltage Source Converters in High Voltage Direct Current Transmission Systems

by

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Dedicated to my family

Abstract

This research focuses on voltage source multilevel converters in high voltage direct current (HVDC) transmission systems. The first Voltage Source Converter based HVDC (VSC-HVDC) systems with series connected IGBTs in a two-level converter represented a solution to meet industrial and economical requirements but is associated with significant drawbacks such as high *dv/dt* and *di/dt,* high switching loss, and poor output voltage and current quality. To overcome these issues, the multilevel converter was proposed for HVDC application.

The Modular Multilevel Converter (M2C) was the first multilevel converter to be commercially used in the power industry. In this thesis, the M2C is investigated mainly in terms of operating principle, capacitor size and capacitor voltage ripple, capacitor voltage balancing technique and modulation scheme. The results of this investigation show that the M2C offers the following features: improved efficiency, lower supporting voltage and current in the switching devices and low *dv/dt*. These features make the M2C suitable for HVDC systems.

Two new operational principles and modulation strategies for a Hybrid Cascaded Multilevel Converter (HCMC) are proposed in this thesis. Both modulation schemes extend the modulation index linear range and improve the output waveform quality. This gives the HCMC a higher power density than any known multilevel converter topology for the same dc link voltage and switching device rating.

Simulations for both types of multilevel converter (M2C and HCMC) are supported by practical results from scaled hardware laboratory converters.

Mathematical analysis and calculation of conversion loss for both types of multilevel converter and for the conventional two-level converter are performed. It is shown that both M2C and HCMC provide lower conversion loss compare to the conventional two-level converter.

A control strategy for these two multilevel converters in point-to-point and multi-terminal HVDC systems is also studied. Simulation results show that these two converters are able to operate over the entire specified P-Q capability curve and are capable of riding through ac faults without imposing any over-voltage or over-current on the converter switches.

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List of Symbols

C	cell capacitance (F)
C_{dc}	DC link capacitance (F)
d	duty cycle
E_{bank}	energy held in H-bridge capacitors (J)
E_{out}	total output energy (J)
E_{on}	turn-on energy coefficient of IGBT (J)
E_{off}	turn-off energy coefficient of IGBT (J)
E_{rec}	reverse recovery energy coefficient of Diode (J)
f_c	carrier frequency (Hz)
f_s	switching frequency (Hz)
i_a	phase current (A)
I_{arm1}	upper arm current in one phase leg of M2C (A)
i_{dc}	DC link current (A)
I_m	peak phase current (A)
I_{mean}	average current from simulation (A)
I_{on}	IGBT/Diode average turn-on current (A)
I_{off}	IGBT/Diode average turn-off current (A)
i_{Sa1}	upper IGBT current of main bridge in HCMC (A)
i_{S13}	upper IGBT current of H-bridge cell in HCMC (A)
i_{Da1}	upper Diode current of main bridge in HCMC (A)
i_{D13}	upper Diode current of H-bridge in HCMC (A)
i_{rms}	*rms* current of phase current *(A)*
i_{sa}	auxiliary switch current in one M2C cell (A)
i_{sm}	main switch current in one M2C cell (A)
k_1,k_2	constant determined by linearizing the switching energy graph
L	phase inductor (H)
m	modulation index
P	average instantaneous active power exchange with load (W)
$P_{conduction}$	conduction loss (W)
$P_{switching}$	switching loss (W)
Q	net charge of the H-bridge cell capacitors (C)

$Q_{1,2}$	reactive power of ac system (VAr)
R	phase resistor (Ω)
S_N	nominal apparent power of the converter *(VA)*
T_s	switching period (s)
v_a	phase voltage (V)
v_{am}	voltage at the terminal of two-level converter (V)
v_{arm1}	upper arm voltage in one phase leg of M2C (V)
V_c	capacitor voltage (V)
$V_{con1,2}$	converter station voltage (V)
V_{dc}	DC link voltage (V)
v_{HB}	voltage across H-bridge (V)
v_h	harmonic voltage of H-bridge cells (V)
v_{h+3}	harmonic voltage of H-bridge cells with 3rd harmonic injection (V)
$V_{S1,2}^{d,q}$	AC system voltage *dq* components (V)
ξ	percentage of voltage ripple (%)
θ	voltage angle between converter station and ac system (*rad*)
ω	angular velocity (*rad/s*)
φ	power factor

List of Abbreviations

AC	Alternative Current
APOD	Alternative Phase Opposition Disposition
CSC	Current Source Converter
DBPWM	Dead Band Pulse Width Modulation
DC	Direct Current
FACTS	Flexible AC Transmission Systems
FFT	Fast Fourier Transform
GTO	Gate Turn-Off Thyristor
GS	Grid Side
HCMC	Hybrid Cascaded Multilevel Converter
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LCC	Line-Commutated Converter
M2C	Modular Multilevel Converter
MLC^2	Multilevel-Clamped Multilevel Converters
MT	Multi-Terminal
NPC	Neutral-Point Clamped
PD	Phase Disposition
PI	Proportional-Integral
PLL	Phase-Locked Loop
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
SCR	Silicon Controlled Rectifier
SFO	Switching Frequency Optimal
SHE	Selective Harmonic Elimination
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
WF	Wind Farm

Table of Contents

CHAPTER 1

1. Introduction

1.1 Background

Electrical plants generate power in the form of ac voltages and currents. This power is transmitted to the load centres using three-phase, ac transmission lines. However, under certain circumstances, dc transmission lines are desirable. This alternative becomes economically attractive where a large amount of power is to be transmitted over a long distance from a remote generating plant to the load centre. The breakeven distance for HVDC overhead transmission lines usually lies somewhere in a range of 300-400 miles and 50-75 miles for submarine cables [1]. In addition, many other factors, such as the improved transient stability and the dynamic damping of the electrical system oscillations, may influence the selection of dc transmission in preference to ac transmission. It is possible to interconnect two ac systems, which are at two different frequencies or which are not synchronized, by means of an HVDC transmission line.

In the past 50 years, High Voltage Direct Current (HVDC) systems have employed several types of switching devices: the mercury-arc valve; the silicon controlled rectifier (thyristor); the Insulated Gate Bipolar Transistor (IGBT), the Gate Turn-off Thyristor (GTO) [2]. Originally, mercury-arc rectification was found to be the most suitable for handling large currents and made high voltage direct current transmission a reality. In the late 1950s, the silicon controlled rectifier (SCR) led to the development of line-commutated, current source converter technology. This improved converter technology led to further development of HVDC transmission systems. More recently, the advent of high capacity, self-commutating GTO and IGBT devices has allowed the development of voltage source HVDC transmission. This approach has realised HVDC Light and HVDC Plus which have extended the range of application of HVDC systems [3-5].

HVDC transmission based on the Voltage Source Converter (VSC) can overcome the functional limits of Current Source Converter (CSC) HVDC but comes with its own set of performance compromises. Initially converters for voltage source HVDC employed conventional two- or three-level inverters with composite switches made up of large numbers of series connected power semiconductor devices. This approach has proven viable up to voltages of 300kV [6] but is limited by the need to compromise between switching loss and power quality.

VSC based HVDC is a multi-variable strongly coupled nonlinear system [7, 8]. It can control active and reactive power independently and can supply both active and passive networks [9, 10]. Reverse power flow can be implemented by reversing the direction of dc current without changing the dc voltage polarity. There is no need for communication between converters and this reversible current feature is helpful in multi-terminal DC systems, allowing both convenient power flow control and high reliability [11].

Multilevel converters overcome the need for series connected switches whilst delivering reduced loss and improved output power quality. A wide range of multilevel converter topologies have been proposed and some have been successfully applied to medium voltage drives [12, 13], however, most multi-level topologies are unsuited for scaling up for application to HVDC transmission systems [14].

The most common types of multilevel converters used in medium and high voltage applications are:

- Diode-clamped multilevel converter
- Flying-capacitor multilevel converter
- Cascaded multilevel converter with separate dc source

The diode-clamped multilevel converter is most widely used in the industrial world [15, 16]. However, with increased output voltage levels, inherent voltage imbalance occurs on dc capacitors, which results in the need for external balancing circuits for the dc capacitors. The expense of capacitors at a low carrier frequency and complex capacitor balancing techniques are major disadvantages of the flying-capacitor multilevel converter [17]. The well-known cascaded multilevel

converter has substantial advantages, especially in the application of the static synchronous compensator (STACOM) but numerous isolated power supplies are required for real power exchange. This has been achieved at medium voltage levels through the use of complex, multi-winding transformers, however this approach is not suited for use with a high voltage dc bus topology [18].

The Modular Multilevel Converter (M2C), Figure 1-1, and by implication the H-bridge modular converter have been shown to be viable for HVDC transmission systems [19]. This approach significantly reduces switching losses and grid-side power filters requirements. The limitation of the M2C concept is the cell capacitors which provide a set of virtual dc sources for the multi-level converter. Unlike the dc link capacitor of a conventional two level inverter, the M2C cell capacitance acts in series with the power transfer path. Thus the capacitors must be rated for the fundamental current and must have high capacitance to limit the cell voltage excursions. The cell capacitors require voltage balance control which increases system complexity and their large capacitance contributes to increasing the converter footprint.

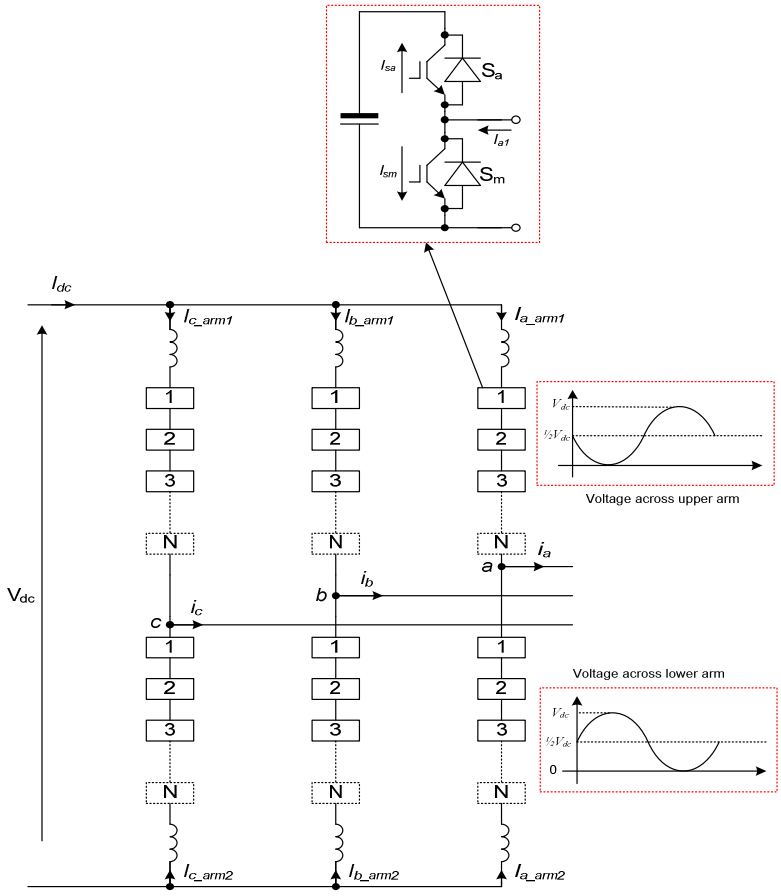

Figure 1-1: Three-phase of the N-level M2C.

Recently mixed topology 'Hybrid' converters (Figure 1-2) have been proposed which combine different multi-level converter topologies in order to optimise different aspects of converter performance [20]. The basic concept involves the use of a two-level converter in series with cascaded H-bridge cells. These cells can be powered with electrically isolated separate active dc sources or by means of floating capacitors. Variants employ isolated sources because both high- and low-voltage stages contribute to the fundamental voltage. For HVDC, the generation of multiple isolated dc power supplies is impractical, thus the H-Bridge voltage is provided by cell capacitors. Although the voltage components synthesised by the H-Bridge cells may not contribute to real power transfer, they may be used to cancel harmonics and contribute to reactive power transfer.

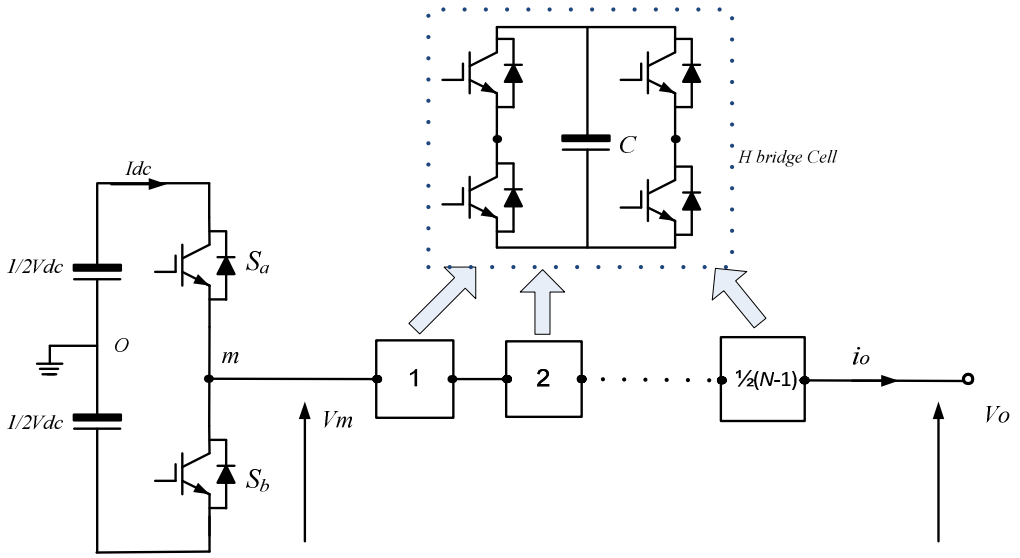

Figure 1-2: Hybrid multilevel converters with *½(N-1)* H-bridge cells in ac side.

1.2 Motivation

The basic form of the VSC-HVDC converter will combine high-voltage operation with low losses and low output voltage harmonics with minimized hardware foot-print and system complexity. Development of HVDC networks will require extended converter functionality, most notably the ability to control or block current flow into a suppressed dc network voltage. Several different multi-level converter topologies can be employed in a HVDC transmission system. The dominant VSC topologies for HVDC systems are either the conventional two-level converter with series connected semiconductors or the multilevel M2C.

The M2C approach achieves multi-level operation with a modular and scalable hardware topology. In addition to standard converter control functions, a robust capacitor balancing technique is required for the M2C to maintain cell voltages. The modulation scheme should be robust and expandable to any voltage level number. The emerging Hybrid Cascaded Multilevel topology gives an extended modulation index linear range and provides reverse blocking dc link fault capability. Effective operation of this circuit requires capacitor balance control and synchronization between fundamental power control and harmonic cancelation if using independent

control. The harmonic cancelation algorithm should ensure that H-bridge cell numbers are minimized whilst providing a high-quality output voltage.

1.3 Objectives

In this research, operation of the Modular Multilevel Converter (M2C) and the Hybrid Cascaded Multilevel Converter (HCMC) has been investigated. Two new PWM schemes for HCMC and an SPWM scheme for M2C are proposed to achieve following points:

- The modulation scheme for M2C should be robust and expandable to any voltage level number.
- H-bridge cell capacitor balancing for HCMC can be achieved independent of modulation index and power factor.
- The high-voltage two-level converter is switched at a frequency close to the fundamental power frequency, resulting in low switching loss, by using an independent control scheme.
- Low-distortion output voltage with low switching loss in both the two level and cascaded H-Bridge stages.
- Low output dv/dt as with multilevel operation and voltage total harmonic distortion (THD) lower than that of the conventional two-level converter.
- H-Bridge cell voltage is compatible with a single semiconductor device.
- The H-Bridge cells only act to cancel harmonic power flow, resulting in a reduced capacitance requirement.
- The ac side H-Bridge cells may be set to block, thereby protecting the inverter in the event of a dc side fault and preventing ac flow into a fault on the dc network.
- Extended modulation index linear range to 1.218 and 2 for real and reactive power applications respectively, using sinusoidal PWM with 3rd harmonic subtraction.

1.4 Methodology and Scope of the Research

Switching functions and averaging of the currents and voltages over one switching cycle are used as the main tools for developing the mathematical models and analytical methods presented in this thesis.

In order to establish a model of the VSC based HVDC system and design its controller, the synchronous reference frame is used. The control strategies presented in this thesis are based on the mathematic model of the converter in the synchronous reference frame, whence the power flow can be controlled by the amplitude and phase angle of the ac-side current [21]. A simplified synchronous *d-q* frame based HVDC model is suitable for simulation and analysis, since it offers quick dynamic response and sensitivity to system parameters [10].

The multilevel converter simulations are supported by experimental results obtained using scaled hardware laboratory converters.

1.5 Thesis Organization

This thesis is organized into eight chapters:

Chapter 1 presents the general background of multilevel converter topologies in HVDC transmission system applications, and the motivation and objectives of this research.

Chapter 2 introduces several multilevel converter topologies that are used in industry. The advantages and disadvantages of these topologies are compared with the conventional two-level converter. Operating principles and converter applications are also presented.

Chapter 3 presents a detailed discussion of different Pulse Width Modulation (PWM) techniques for multilevel converters, namely carrier-based PWM, third harmonic reference injection and Selective Harmonic Elimination PWM (SHE-PWM). Different modulation techniques are compared by mathematical analysis and MATLAB/ SIMULINK simulations.

Chapter 4 presents the concept and operating principle of the Modular Multilevel Converter (M2C), and cell capacitor balancing techniques for three- and five-level M2C are introduced. The derived mathematical expressions for capacitor voltage ripple and capacitor size are presented at the medium voltage level (20kV dc voltage). Both simulation and experimental result support this chapter.

Chapter 5 introduces the main concept and two operating modes of the Hybrid Cascaded Multilevel Converter (HCMC). These two operating modes employ different PWM schemes: one is independent control of two-level and H-bridge cells using SHE-PWM, and the other is Sinusoidal Pulse Width Modulation (SPWM) with third harmonic subtraction. Mathematical analysis of capacitor size and voltage ripple, and power flow are presented. Both simulation and experiments results are presented validate the two PWM schemes.

Chapter 6 presents an analytical evaluation of conduction and switching losses for the proposed multilevel converters. The derived mathematical expressions are based on sinusoidal current and voltage assumptions. The conversion losses of the M2C and the hybrid cascaded multilevel converter are compared. Also, theoretical and experimental conversion losses of the hybrid cascaded multilevel converter are presented.

Chapter 7 considers the multilevel converter in an HVDC transmission system application, where the general system description and operation are presented. The control strategies for two-terminal and multi-terminal HVDC systems are discussed. Both M2C and HCMC operating during HVDC transmission system steady-state and transients are simulated in MATLAB/SIMULINK.

Chapter 8 draws general conclusions and presents recommendations for the future research.

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CHAPTER 2

2 Converter Topologies in HVDC Transmission Systems

2.1 Introduction

A HVDC transmission systems can be based on either current or voltage source converters. The second generation HVDC system employed a current source converter that used thyristors as the switching devices. This type of transmission system has been widely used in the power transmission industry for over five decades and it is also known as a line commutated converter high-voltage direct current (LCC-HVDC) transmission system. Its main advantages are low conversion losses (mainly on-state losses, due to thyristor low on-state forward voltage drop) and high overload capacity. However, its switching frequency is limited to the ac network power frequency. The main disadvantages of LCC-HVDC transmission systems are:

- Large passive filters must to be installed for low-order harmonic mitigation, and an additional damping filter is required (thereby increasing system losses).
- Slow dynamic response as its switching frequency is the same as the ac network power frequency.
- Active and reactive output power cannot be controlled independently.
- It cannot be connected to a passive ac network where the ac system has a low network source impedance.
- It has a large footprint, which is not desirable for offshore wind farms due to high installation and maintenance costs.
- It is susceptible to ac network disturbances, which may temporarily shut down the system [1].

A voltage source converter based high voltage direct current (VSC-HVDC) transmission system uses self-commutated devices such as the insulated gate bipolar transistor (IGBT) as its main switching device, which provides better performance than the conventional LCC-HVDC system. The first VSC-HVDC systems used series connected IGBTs (Figure 2-1) with a switching frequency of less than 2kHz. The adoption of IGBTs in VSC-HVDC transmission systems allows the use of high frequency pulse width modulation (PWM) that resulting in a fast dynamic response and independent control of the active and reactive powers. Hence voltage support of the grid can be achieved without compromise to the basic active power transmission function. Also ac fault ride through ability can be achieved. The HVDC system can remain connected and help ac network recovery. Furthermore, the use of a 1 to 2kHz switching frequency is sufficient to separate the harmonics from the power frequency, therefore only small size ac filters need to be used to mitigate the high order harmonics. Consequently, the system footprint is expected to be smaller than the conventional LCC-HVDC system. However, a disadvantage of the VSC-HVDC is higher switching losses. Additionally, it is vulnerable to dc side short circuit faults due to the large dc link capacitance compared with conventional HVDC systems.

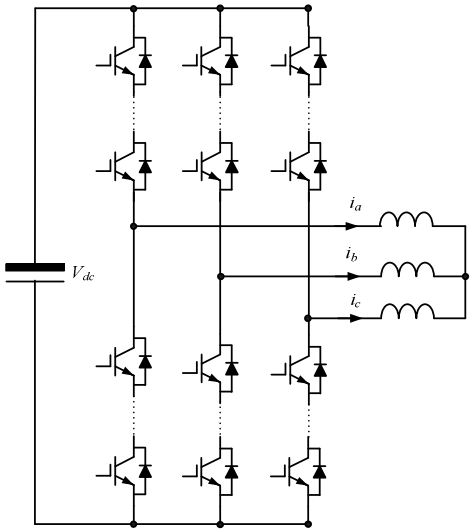


Figure 2-1: Conventional series connected two-level converter.

2.2 Conventional Two-level Converter

A typical three-phase, two-level VSC using IGBTs is shown in Figure 2-2. Two stacks of IGBTs are connected in series in each leg, where the voltage stress for each stack equals to the dc link voltage. The switching frequency of each IGBT is the same as the carrier switching frequency.

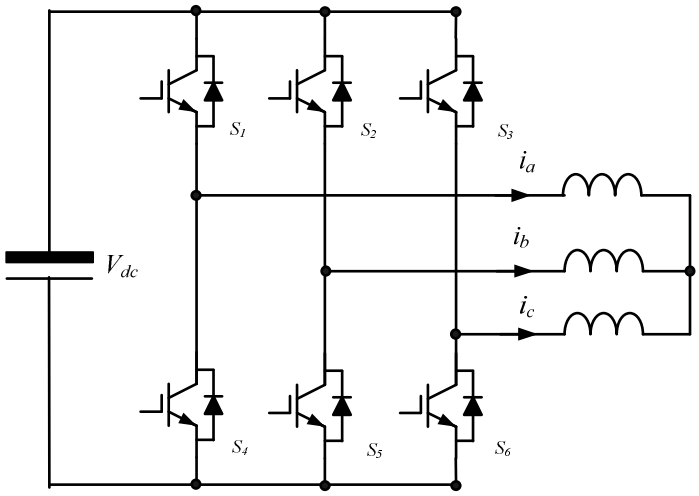


Figure 2-2: Conventional two-level converter.

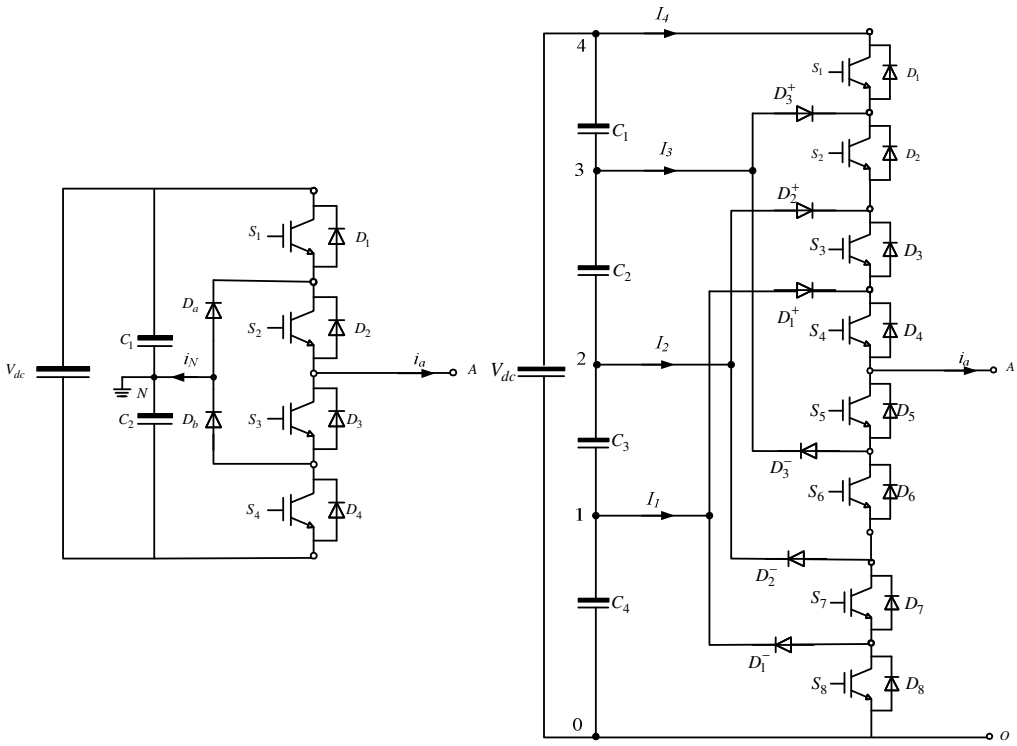
A two-level converter with a high number (n>100) of series connected IGBTs represents a solution to meet the requirements of industry and economical needs such as modular construction and scalability. However, it has significant drawbacks:

- A bulky passive ac filter is needed in order to suppress undesired harmonics.
- High *dv/dt* and *di/dt* cause unwanted EMC disturbance and large voltage and current stress on each device.
- High switching loss.
- The energy stored in the dc capacitor results in high dc fault current and damage if a short circuit fault occurs on the dc bus.

2.3 Diode Clamped Multilevel Converter

The diode-clamped multilevel converter employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. The first neutral

point clamped (NPC) multilevel inverter was a three-level inverter, proposed by Nabae *et al.* in 1980 [2] and extended to *N* levels by Bhagwat in 1983 [3]. A generalized version of the diode-clamped converter consists of *N*-1 capacitors connected in series across the dc bus, so that inverter can generate *N* voltage levels per phase. One bridge arm is composed of 2×(*N*-1) series connected switches, and (*N*-1) ×(*N*-2) diodes are used to clamp the switch voltages. This topology produces *N* levels in the phase voltage and 2×(*N-1*) levels in the line voltage, during normal operation.



(a) (b)

Figure 2-3: One phase of diode-clamped converter (a) three-level leg (b) five-level leg.

Figure2-3a shows the circuit diagram of one phase of a three-level diode-clamped converter. Each leg is composed of four active switches with four anti-parallel diodes. The dc bus capacitor is split into two, providing a neutral point *N*. The difference between the three-level diode-clamped inverter and the conventional two-level inverter is the clamping diodes D_a and D_b. When switches S_2 and S_3 are turned on, the inverter output terminal A is connected to the neutral point through one of the

clamping diodes D_a or D_b. The voltage across each of the dc capacitors is normally equal to half of the total dc voltage $V_{dc.}$ When current i_N flows into the neutral point N, the capacitors C_1 or C_2 can be charged or discharged, causing neutral-point voltage deviation.

The output voltage V_a has three states 0, $\pm½V_{dc}$. Switches S_1 and S_2 are turned on for $½V_{dc,}$ switches S_2 and S_3 are turned on for the 0 level, and switches S_3 and S_4 are turned on for voltage level - ½ V_{dc}. D_a and D_b clamp specific switch voltages to half the dc bus voltage. For instance, when switches S_1 and S_2 turn on, $V_a = V_{dc}$; diode D_b balances the voltage sharing between S_3 and S_4 with S_3 blocking the voltage across C_2 and S_4 blocking the voltage across $C_{1.}$

Table 2-1 shows switching state arrangements for S_1 to S_4 respectively [4]. The gate signals can be generated by modulation methods introduced in Chapter 3.

Table 2-1: Switching states combinations of one leg of three-level Diode-clamped inverter.

Switching state	Device switching status(Phase A)				Terminal voltage V_{AO}
	S_1	S_2	S_3	S_4	
1	On	On	Off	Off	$½V_{dc}$
0	Off	On	On	Off	0
-1	Off	Off	On	On	- ½ V_{dc}

Figure2-3b shows the circuit diagram of one phase of a five-level diode-clamped converter, where the clamping diodes are of the same voltage rating. There are four capacitors across the dc link, which divides the dc bus voltage into five levels: $½V_{dc}$, $¼V_{dc}$, 0, $-¼V_{dc}$, $-½V_{dc}$. There are 8 series switches in each arm, S_1 to S_8, and the clamping diodes $D_1^+, D_1^-, D_2^+, D_2^-, D_3^+, D_3^-$ are used to clamp the voltage on each switch to one capacitor voltage level. To produce a five voltage level sequence $½V_{dc}$, $¼V_{dc}$, 0, $-¼V_{dc}$, $-½V_{dc}$, four adjacent switches could be switched on/off together sequentially.

Some features of the diode-clamped multilevel inverter are:

1) High voltage rating required for blocking diodes. Although each active switching device is only required to block a voltage level of $V_{dc}/(N\text{-}1)$, the clamping diodes need to have different reverse voltage ratings. If the

blocking voltage rating of each diode is the same as that of the switching devices, the number of diodes required for each phase is $N_d=(N-1)\times(N-2)$, where N denotes the number of levels. When N is sufficiently high, the number of diodes makes the system impractical.

2) Capacitor voltage unbalance. In most applications, a power converter needs to transfer real power from ac to dc or dc to ac. For more than three levels, dc link capacitor voltage imbalance increases with decreasing power factor and capacitor voltage balancing methods must be applied to maintain the voltage constant [5, 6].

2.4 Flying Capacitor Multilevel Converter

The Flying Capacitor Multilevel Converter was introduced by T.A. Meynard et al. in 1992 [7]. The capacitors in combination with the switches are used to synthesize different voltage levels at the converter output. The flying capacitor inverter offers flexible switch combinations for synthesizing the output voltage [8, 9].

Figure 2-4 shows the circuits for one leg of three-level and five-level flying capacitor multilevel converter. In Figure 2-4a, three output voltage level can be synthesized: 0, $\pm\frac{1}{2}V_{dc}$.

The steps to synthesize the five-level voltages are:

1. For an output voltage level $V_{AO}=\frac{1}{2}V_{dc}$, turn on all the upper-half switches S_1 to S_4.
2. For an output voltage level $V_{AO}=\frac{1}{4}V_{dc}$, there are four combinations:
   a. on devices: S_1, S_2, S_3, and S_8.
   b. on devices: S_2, S_3, S_4, and S_5.
   c. on devices: S_1, S_3, S_4, and S_6.
   d. on devices: S_1, S_2, S_4, and S_7.
3. For an output voltage level $V_{AO}=0$, there are six combinations:
   a. on devices: S_1, S_2, S_7, and S_8.
   b. on devices: S_3, S_4, S_5, and S_6.
   c. on devices: S_1, S_3, S_6, and S_8.
   d. on devices: S_1, S_4, S_6, and S_7.
   e. on devices: S_2, S_4, S_5, and S_7.
   f. on devices: S_2, S_3, S_5, and S_8.

4. For an output voltage level $V_{AO} = -¼V_{dc}$, there are four combinations:
   a. on devices: S_1, S_6, S_7, and S_8.
   b. on devices: S_4, S_5, S_6, and S_7.
   c. on devices: S_3, S_5, S_6, and S_8.
   d. on devices: S_2, S_5, S_7, and S_8.
5. For an output voltage level $V_{AO} = -½V_{dc}$, turn on all lower half switches, S_5 to S_8.

An N-level converter has $2\times(N-1)$ line voltage levels. Assuming that each capacitor has the same voltage rating as the switch, the dc bus needs N-1 capacitors for an N-level converter, and $½(N-1)\times(N-2)$ clamping capacitors. Because of the large number of capacitors required and inherent capacitor shortcomings, research and application of the flying capacitor multilevel inverter is limited.

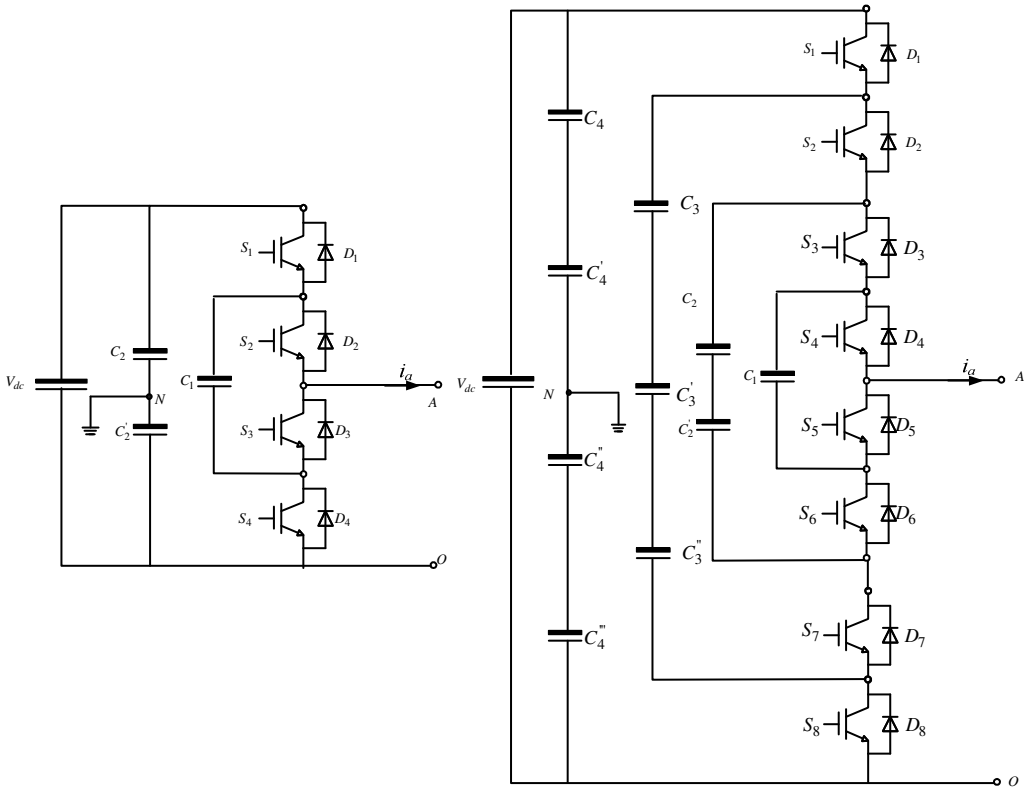


Figure 2-4: Flying capacitor circuits (a) three-level leg (b) five-level leg.

The advantages of the flying capacitor converter are:

- Large storage capacitance provides ride-through capability during power outage. Switch combination redundancy for balancing different voltage levels. Both real and reactive power flow can be controlled, making it a voltage source converter candidate for high voltage dc transmission.

Disadvantages are:

- An excessive number of storage capacitors are required when the number of converter output levels is high. High-voltage systems are more difficult to package and more expensive because of the required bulky capacitors. Converter control is complicated, and the switching frequency and switching losses will be high with real power transmission.

2.5 Cascaded H-bridge Multilevel Converter

The cascaded H-bridge multilevel converter is based on the series connection of H-bridge cells to achieve medium-voltage operation. It requires a number of isolated dc sources to supply each H-bridge cell as shown in Figure 2-5 [10].

Each power cell is capable of producing output voltages $\pm V_{dc}$, or 0 by connecting the dc source to the output terminals using different combinations of the four switches. The two series switches in each leg of each cell (e.g. S_1 and S_3) form complementary switch pairs, where one switch is turned on /off, and the other switch must be off/on.

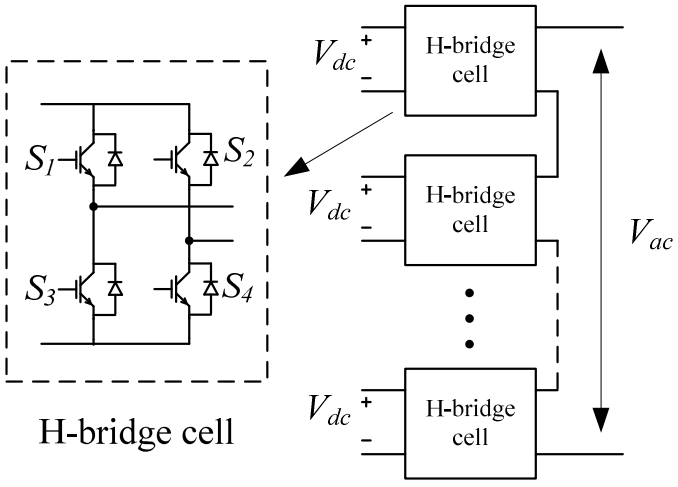


Figure 2-5: Cascaded H-bridge converter with electrically isolated DC sources.

The operating status of the switches can be represented by switch states shown in Table 2-2. Switch state '1' denotes that the switches S_1 and S_4 are on and the inverter terminal voltage V_{ac} is $+V_{dc}$, whereas '-1' indicates that the switches S_2 and S_3 conduct, leading to $V_{ac} = -V_{dc}$. Switch state '0' signifies that either the upper two switches S_1 and S_2 or the lower two switches S_3 and S_4 are on.

The cascaded multilevel converter is not suitable for HVDC transmission systems due to the absence of a common dc link. However it has been proposed for photovoltaic grid integration [11] and electric hybrid vehicles [12].

Table 2-2: Switching states combinations of one cell of Cascaded H-bridge Multilevel Converter.

Switching state	Device switching status (Phase A)				Terminal voltage V_{ac}
	S1	S2	S3	S4	
1	On	Off	Off	On	$+V_{dc}$
0	Off	Off	On	On	0
	On	On	Off	Off	
-1	Off	On	On	Off	$-V_{dc}$

2.6 Modular Multilevel Converter

The Modular Multilevel Converter (also known as M2C) is the latest converter topology adopted in HVDC systems [13-16], It has been used in the first commercial application of multilevel HVDC converters known as HVDC PLUS [17]. This topology is highly attractive for HVDC applications since the structure of the M2C allows operation at high voltage with low harmonic content, without the use of ac filters (where this is appropriate), and also without the need to increase the switching frequency. This converter will be studied in detail in this thesis.

2.7 Other Converter Topologies

Multilevel-Clamped Multilevel Converter (MLC^2) was proposed by P. Rodriguez et al. in 2011[18]. This topology is based on a multilevel clamp concept combined with

a Neutral-Point-Clamped (NPC) converter to produce an increased number of levels without an excessive part count or additional complexity. However, issues regarding power losses and capacitor voltage balancing were not addressed.

Use of the Z-source inverter for WECS was investigated [19, 20] as a possible solution for grid interfacing. A unique impedance network is employed in the DC side rather than a single capacitor or inductor. Unlike the conventional VSC or CSC, the input voltage can be stepped up and down [21], which is convenient for grid connection and DC link control. Also the input and output can be voltage or current sources.

The matrix converter has been investigated as an alternative to conventional ac/dc/ac conversion for wind energy applications [22, 23]. An array of controlled bidirectional switches is used as the main power elements to interface a three phase generator to the grid [24]. It allows independent control of voltage magnitude, frequency, phase angle and power factor [25]. The main advantage compared to conventional ac/dc/ac conversion is that there is no dc link, and therefore no bulky capacitors. However, due to the absence of energy storage elements, ride through capability and input and output decoupling do not exist [24]. The gain is less than unity and if the input is a voltage source the output is a current source, and vice versa.

2.8 Comparison

Table 2-3: Comparisons of component requirements per leg of multilevel converters.

N-level in phase	Multilevel Topologies			
	Diode clamp	Flying capacitor	Cascaded H-bridge	M2C
Phase levels	*N*	*N*	*N(odd)*	*N*
Line levels	*2 N+1*	*2 N+1*	*2 N*	*2N+1*
Main switching devices	(*N*-1)×2	(*N* -1)×2	(*N* -1)×2	(*N* -1)×2
Main diodes	(*N* -1)×2	(*N* -1)×2	(*N* -1)×2	(*N* -1)×2
Clamping diodes	(*N* -1)×(*N* -2)	-	-	-
DC bus capacitors	(*N* -1)	(*N* -1)	(*N* -1)/2	-
Balancing capacitors	-	½ (*N* -1)×(*N* -2)	-	(*N* -1)×2

Table 2-4: Comparison of different inverter based HVDC systems.

	LCC based	VSC based	
	LCC	Two level	M2C
Switching device	Thyristor	IGBT	IGBT
Switching loss	Negligible	High	Low
On-state loss	Low	Moderate	Moderate
Active power control	Continuous ±10% to ±100%	Continuous 0 to ±100%	Continuous 0 to ±100%
Independent control of active and reactive power	No	Yes	Yes
Reactive power demand	50% to 60%	No	No
AC filters	Large	Small	No
AC fault ride through ability	Possible with high risk of commutation failure	Excellent	Excellent
DC fault ride through ability	Excellent	Poor	Moderate

2.9 Summary

The modern power industry requires power converters to operate under medium-voltage and high-power conditions, which are beyond the capability of single semiconductor switches. The multilevel inverter is an option to provide high voltage while the power semiconductors withstand rated voltage. There are three basic multilevel inverter topologies: the neutral point/diode clamped multilevel inverter, the flying capacitor multilevel inverter and the cascaded H-bridge multilevel inverter. Compared with the conventional two-level inverter topology, multilevel inverters generate lower harmonic distortion, require approximately half the switching frequency of a two-level converter to generate output voltage with the same quality, have a lower voltage stress across a single switch, and facilitate higher power ratings [26].

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CHAPTER 3

3 Pulse Width Modulation Techniques

3.1 Introduction

The Voltage Source Converter (VSC) is the key technology behind application of advanced power electronics apparatus for electronically controlled modern power systems. It is also the backbone of modern High Voltage Direct Current (HVDC) transmission systems and Flexible AC Transmission Systems (FACTS) devices such as static synchronous reactive power compensators (STATCOM) for both distribution and transmission systems. The reduction of switching losses in VSCs is of prime importance in industrial applications. Exact switching transitions, being able to increase the converter bandwidth, and reduce or eliminate maximum number of harmonics represent key developments for these converters. Hence, for any pulse width modulation (PWM) scheme, a primary objective is to calculate the duty cycles for the converter switches that produce the desired low frequency voltage and current. The secondary objective is to determine the most effective way of arranging the switching processes to minimize unwanted harmonic distortion, switching loss, etc. [1]. Usually PWM techniques can be evaluated in terms of the following criteria: wide linear modulation range, low switching loss, low Total Harmonic Distortion (THD) in the output voltage and current waveform spectra, low switching device stresses, and ease of implementation [2].

For multilevel converter carrier-based PWM [3-5], Space Vector PWM (SVPWM) [6, 7], staircase fundamental frequency switching and fundamental frequency Selective Harmonic Elimination PWM (SHE-PWM) [8, 9] methods are widely used and discussed in the open literature.

3.2 Carrier-Based Pulse Width Modulation

Carrier-based PWM techniques control each converter phase leg individually. Comparison between one or more carrier signals and the modulating signal determines the on/off action for the specific switch in one phase leg, and the width of each generated pulse is varied in proportion to the amplitude of the modulating signal [10]. The gating pulses can be placed symmetrically in the centre of the switching period or asymmetrical on one side, depending on the carrier shape employed (saw-tooth or equilateral triangle). Carrier-based PWM can be implemented using different sampling techniques [1]:

- *Naturally sampled* PWM: Switching instant occurs at the intersection of the low frequency target reference waveform and the high frequency carrier waveform.
- *Regular sampled* PWM: Switching instant occurs at the intersection between the low frequency regularly sampled target reference waveform and the high frequency carrier waveform.
- *Direct* PWM: Switching instant occurs so that the integrated area of the low frequency target reference waveform over the carrier interval is the same as the integrated area of the converter switched output.

Based on the carrier waveform level and phase angle differences, multi-level carrier-based PWM can be divided into two schemes:

- Level-shifted multi-carrier modulation:

For an *N*-level output phase voltage, *N-1* triangular carriers are required. All of these carriers have the same frequency and amplitude. The *N-1* triangular carriers are vertically disposed such that the bands they occupy are contiguous. There are three schemes for level-shifted multi-carrier modulation.

i. Alternative phase opposition disposition (APOD): Each carrier waveform is shifted by 180^{o} from the adjacent carrier waveform.
ii. Phase opposition disposition (POD): Carrier waveforms above the zero reference are in phase but shifted by 180^{o} from those carrier waveforms below the zero reference.
iii. Phase disposition (PD): All carrier waveforms are in phase.

- Phase-shifted multi-carrier modulation:

All the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by:

$$\theta_{sh} = \frac{360^{\circ}}{(N-1)} \tag{3.1}$$

Where N is the output phase voltage level.

Based on the target reference signal differences, multilevel carrier-based PWM can be divided into these schemes:

- Sinusoidal pulse width modulation (SPWM): Where the modulating signal is a pure sinusoidal reference and compared with the triangular carrier waveform to generate switching signals for the switches.
- Third-Harmonic-Injection pulse width modulation (THI-PWM): Injection of harmonics into a pure sinusoidal modulating signal can increase the dc link voltage utilization in over-modulation while retaining the linearity between the modulating signal and the modulated output waveform, and improved THD. The maximum modulation index that can be achieved by harmonic injection PWM is $2/\sqrt{3}$ in the linear modulation mode. A 1/6 third harmonic component [1] can be added to the pure sinusoidal waveform to increase the maximum output line-to-line voltage. A ¼ third harmonic injection [6] achieves the lowest THD in the output line-to-line voltage.
- Switching frequency optimal pulse width modulation (SFO-PWM): Where zero sequence components are injected into the modulating signal (equation 3.2 to 3.5). This approach can extend the linear range of the modulation index by 15% before over-modulation. Another feature is that the switching pattern is similar to space vector modulation.

$$v_{zero} = \frac{\max(v_a + v_b + v_c) + \min(v_a + v_b + v_c)}{2} \tag{3.2}$$

$$v_a^* = v_a - v_{zero} \tag{3.3}$$

$$v_b^* = v_b - v_{zero} \tag{3.4}$$

$$v_c^* = v_c - v_{zero} \tag{3.5}$$

Where v_j^* (j=a,b,c) is the resultant modulating signal.

- Dead Band pulse width modulation (DBPWM): If the neutral point of the load is floating, on an instantaneous basis, keeping one inverter leg clamped does not result in loss of control of the three output line currents [11]. DBPWM allows each phase of the converter to remain inactive for 1/3 of the line cycle thus the switching actions of a DPWM modulator are 2/3 those of a continuous modulator with an identical carrier frequency. Fewer switching actions lead to lower switching loss. The analytical expression for the reference waveform is:

$$v = k \sin \omega t + e_i$$

$$e_i = \begin{cases} k - u^*_{\max} & \left|u^*_{\max}\right| > \left|u^*_{\min}\right| \\ -k - u^*_{\min} & \left|u^*_{\max}\right| < \left|u^*_{\min}\right| \end{cases} \Bigg\} 0 \le k \le 2/\sqrt{3}$$

Where: $u^*_{\max}$ and $u^*_{\min}$ are the maximum and minimum values of the three instantaneous sinusoidal modulating signals.

The literature review focuses on naturally sampled SPWM with different carrier waveforms for multilevel converters.

3.2.1 Analysis of carrier-based PWM

Analysing the harmonic distribution of a pulse width modulated converter output voltage waveform is quite complex and is often performed using Fast Fourier Transform (FFT) analysis. It is based on the concept that any time-varying waveform can be described by an infinite series of harmonic components. The most well adopted analytical method of determining the harmonic components of power electronic converters was proposed by Bowes and Bird in 1975 [12]. They assumed two time variables: one representing the time variation of the high-frequency carrier wave and the other representing the low-frequency reference waveform. Both of these variables are considered independent and periodic. The harmonics of a PWM switched waveform can be expressed in a general form as a summation Fourier series [13]:

$$F(t)=\frac{A_{00}}{2}+\sum_{n=1}^{\infty}(A_{0n}\cos n\omega_0 t+B_{0n}\sin n\omega_0 t)+\sum_{m=1}^{\infty}(A_{m0}\cos n\omega_c t+B_{m0}\sin n\omega_c t)$$
$$+\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}(A_{mn}\cos((m\omega_c+n\omega_0)t)+B_{mn}\sin((m\omega_c+n\omega_0)t)) \quad (3.6)$$

Where:

$\frac{A_{00}}{2}$	is the dc offset.
$\sum_{n=1}^{\infty}(A_{0n}\cos n\omega_0 t+B_{0n}\sin n\omega_0 t)$	is the fundamental component and baseband harmonics.
$\sum_{m=1}^{\infty}(A_{m0}\cos n\omega_c t+B_{m0}\sin n\omega_c t)$	is the carrier harmonics.
$\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}(\begin{matrix}A_{mn}\cos((m\omega_c+n\omega_0)t\\ B_{mn}\sin((m\omega_c+n\omega_0)t)\end{matrix}+)$	is the side-band harmonics.

The complex coefficients for (3.6) can be expressed by:

$$\overline{C_{mn}}=A_{mn}+jB_{mn}=\frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}F(x,y)e^{j(mx+ny)}dxdy \quad (3.7)$$

Where $F(x)=F(\omega_c t)$ represents the carrier waveform function.

$F(y)=F(\omega_0 t)$ represents the reference waveform function.

Mathematical model for the carriers required to generate N-level voltage output

For an *n*-level converter, n upper carriers and n lower carriers can be defined as:

$$v_{upper\_k}=v_{offset\_k}+\frac{1}{n-1}(\sin^{-1}(\sin(\omega_c t+\theta_k))+1) \quad (3.8)$$

Where: $v_{offset\_k}=1-\frac{2k}{n-1};k=1,2,....\frac{1}{2}(n-1)$

$$v_{lower\_k}=v_{offset\_k}+\frac{1}{n-1}(\sin^{-1}(\sin(\omega_c t+\theta_k))-1) \quad (3.9)$$

Where: $v_{offset\_k}=1-\frac{2(k-1)}{n-1};k=\frac{1}{2}(n+1),\frac{1}{2}(n+2).....(n-1)$

For different carrier patterns:

$$\begin{aligned}&\text{PD: } \theta_k = 0 \quad \forall k \; k = 0 \;\text{ to }\; k = n-1 \\ &\text{POD: } \;\theta_0 \text{ to } \theta_{n-1/2} = 0\,, \;\; \theta_{n+1/2} \text{ to } \;\theta_{n-1} = \pi \\ &\text{APOD: } \;\theta_{even} = 0 \text{ and } \;\theta_{odd} = \pi\end{aligned} \tag{3.10}$$

For three-level Phase Disposition (PD), Phase opposition disposition (POD) and Alternative phase opposition disposition (APOD) modulation schemes, the upper and lower carriers can be expressed by:

$$v_{upper} = \frac{1}{2}[\frac{2}{\pi}\sin^{-1}(\sin(\omega_c t)+1)] \tag{3.11}$$

$$v_{lower} = \frac{1}{2}[\frac{2}{\pi}\sin^{-1}(\sin(\omega_c t+\theta)-1)] \tag{3.12}$$

Where $\theta = 0$ for PD carriers, and $\theta = \pi$ for POD and APOD carriers.

For five-level Phase Disposition (PD), Phase opposition disposition (POD) and Alternative phase opposition disposition (APOD) modulation schemes, the upper and lower carriers can be expressed by:

$$\begin{aligned}v_{upper\_1} &= \frac{1}{2}+\frac{1}{4}[\frac{2}{\pi}\sin^{-1}(\sin(\omega_c t+\theta_1)+1)] \\ v_{upper\_2} &= \frac{1}{4}[\frac{2}{\pi}\sin^{-1}(\sin(\omega_c t+\theta_2)+1)]\end{aligned} \tag{3.13}$$

$$\begin{aligned}v_{lower\_1} &= \frac{1}{4}[\frac{2}{\pi}\sin^{-1}(\sin(\omega_c t+\theta_3)-1)] \\ v_{lower\_2} &= -\frac{1}{2}+\frac{1}{4}[\frac{2}{\pi}\sin^{-1}(\sin(\omega_c t+\theta_4)-1)]\end{aligned} \tag{3.14}$$

Where $\theta_1 = \theta_2 = \theta_3 = \theta_4 = 0$ for PD carriers

$\theta_1 = \theta_2 = 0, \theta_3 = \theta_4 = \pi$ for POD carriers.

$\theta_1 = \theta_{30} = 0, \theta_2 = \theta_4 = \pi$ for APOD carriers

Figure 3-1 to Figure 3-6 show these three schemes of PWM signal generation for three-level and five-level diode clamped/M2C converters.

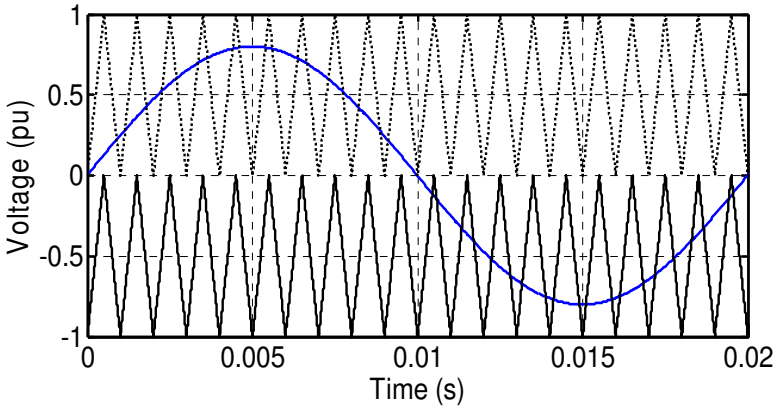


Figure 3-1: PWM signal generation for three-level diode clamped/M2C converter using PD carrier.

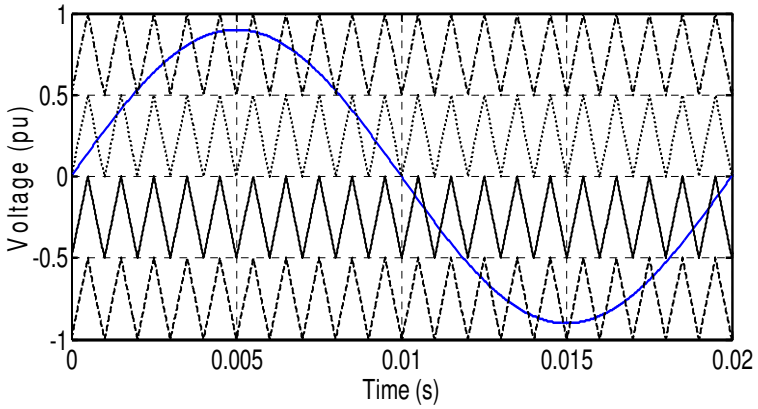


Figure 3-2: PWM signal generation for five-level diode clamped/M2C converter using PD carrier.

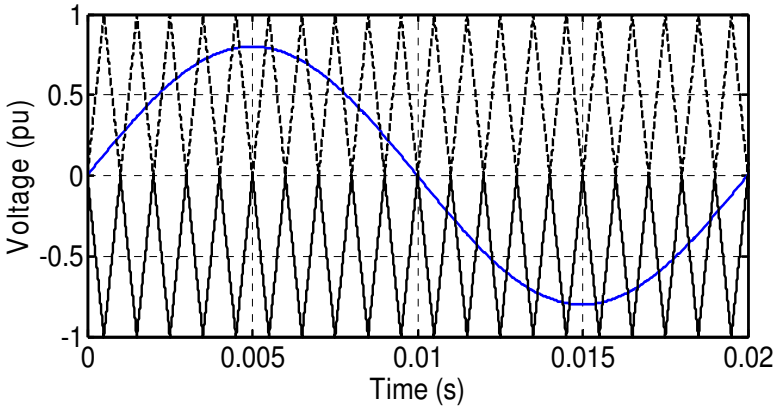


Figure 3-3: PWM signal generation for three-level diode clamped/M2C converter using POD carrier.

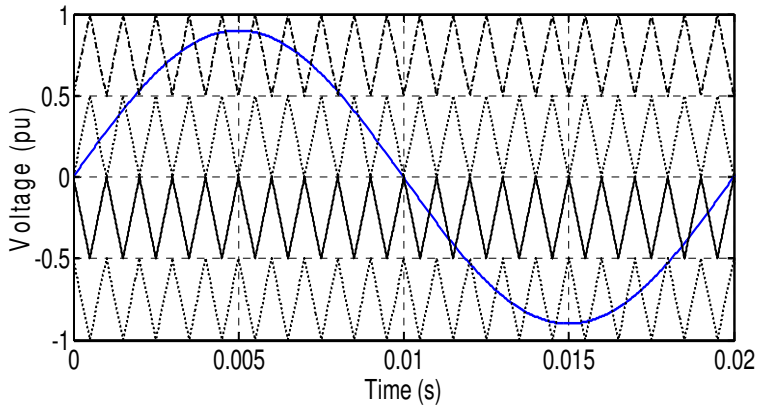


Figure 3-4: PWM signal generation for five-level diode clamped/M2C converter using POD carrier.

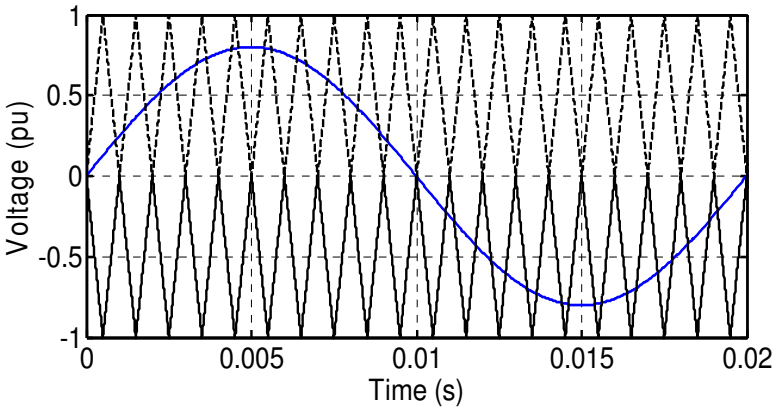


Figure 3-5: PWM signal generation for three-level diode clamped/M2C converter using APOD carrier.

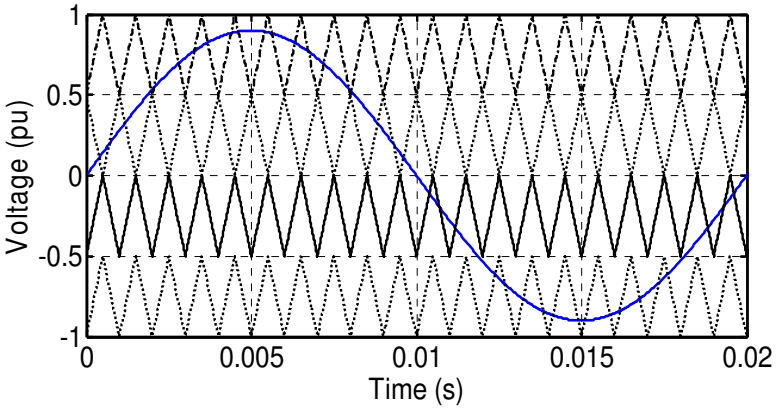


Figure 3-6: PWM signal generation for five-level diode clamped/M2C converter using APOD carrier.

Harmonic analysis

Three-level SPWM with PD carriers:

Figure 3-7 shows PWM signal generation for two cycles of the carrier signal waveforms. The two intersection points in the upper carrier are: $x_{r1} = -\frac{1}{\pi} M \sin y - 1$ and $x_{f1} = \frac{\pi}{2} M \sin y + \frac{\pi}{2}$ (where y is the carrier waveform and shown in Figure 3-7). When the output voltage varies between ½Vdc and 0, while the two intersection points in the lower carrier are: $x_{r2} = -\frac{2}{3} M \sin y + \pi$ and $x_{f2} = -\frac{\pi}{2} M \sin y - 2\pi$ when the output voltage varies between -½Vdc and 0.

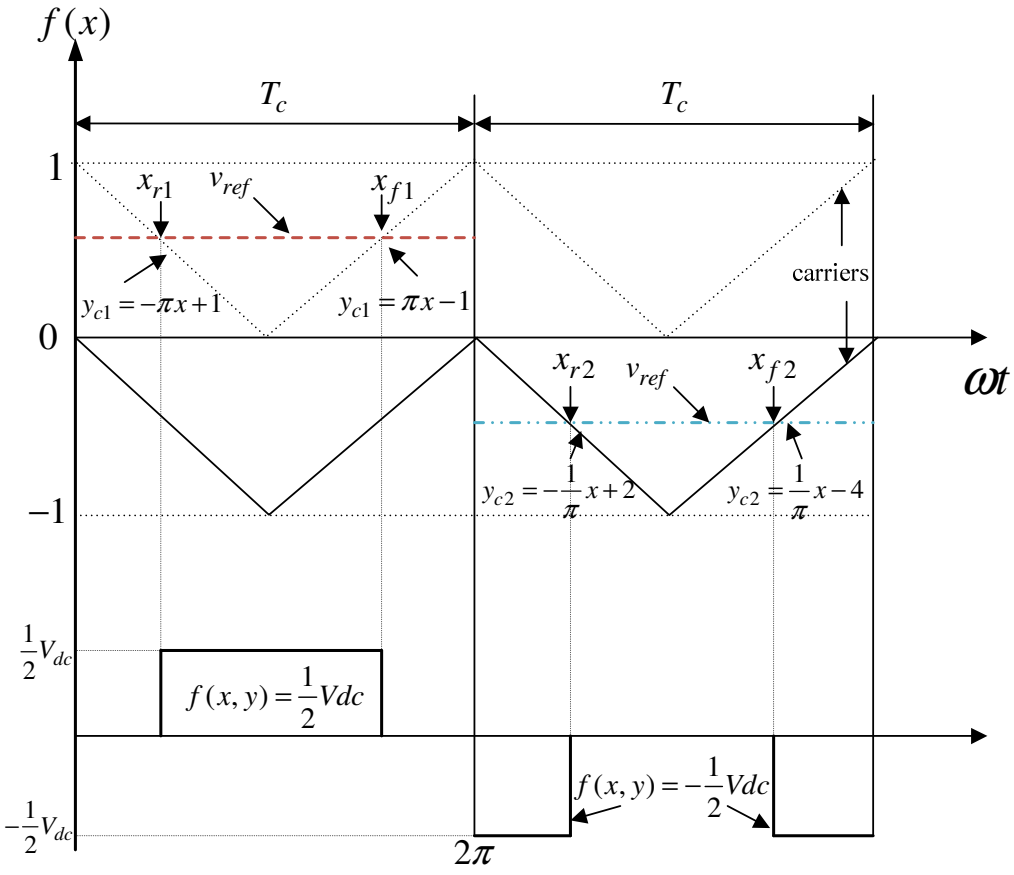


Figure 3-7: Two cycles of reference and carrier signal waveforms by using PD carrier (where in the first cycle, the reference is crossing the upper carrier, and in the second cycle, the reference is crossing the lower carrier).

Based on equation (3.6), the complex coefficient C_{mn} can be derived:

$$C_{mn} = \frac{V_{dc}^2}{4\pi^2}[\int_0^{\pi}\int_{x_{r1}}^{x_{f1}} e^{j(mx+ny)}dxdy + \int_{\pi}^{2\pi}(\int_{\pi}^{x_{r1}} e^{j(mx+ny)}dxdy + \int_{x_2}^{2\pi} e^{j(mx+ny)}dxdy)]$$

$$C_{00} = 0$$

$$C_{01} = \frac{1}{2}MV_{dc} \qquad (3.15)$$

$$C_{0n} = 0, \forall n > 1$$

$$C_{m0} = -\frac{2V_{dc}}{2m\pi}\sum_{k=1}^{\infty}\frac{J_{(2k-1)}m\pi M}{2k-1}(1-\cos(m+n)\pi)$$

$$C_{mn} = \frac{V_{dc}}{2m\pi}(1-\cos(m+n)\pi)(J_n(m\pi M)\sin\frac{n\pi}{2})$$

$$+\frac{2}{\pi}\sum_{\substack{k=1,\\ |n|\neq 2k-1}}^{\infty} J_{(2k-1)}(m\pi M)\frac{(2k-1)\cos\frac{n\pi}{2}}{(2k-1+n)(2k-1-n)}$$

Where J stands for the Bessel function of the first kind: $J_\alpha(x) = \sum_{q=0}^{\infty}\frac{(-1)^q}{q!\Gamma(q+\alpha+1)}(\frac{1}{2}x)^{2q+\alpha}$.

The C_{m0} term indicates the carrier harmonic components of the phase voltage are only non-zero when *m* is odd, which means only odd order carrier harmonics exist.

The C_{mn} term indicates the sideband components are separated by $2\omega_0$, with even order sideband harmonics (*n*=even) spread around the odd carrier components (*m*=odd) and odd order sideband harmonics (*n*=odd) spread around the even carrier components (*m*=even).

Three-level SPWM with POD/APOD carriers:

With POD/APOD carrier based PWM, the mathematical analysis results are the same, as displayed in Figure 3-8, but the difference between POD/APOD carriers and PD carriers is the integration limits are determined by the lower carrier. The two intersection points in the upper carrier are: $x_{r1} = -\frac{1}{\pi}M\sin y - 1$ and $x_{f1} = \frac{\pi}{2}M\sin y + \frac{\pi}{2}$ (where y is the carrier waveform and shown in Figure 3-8). When the output voltage varies between ½V_{dc} and 0, while the two intersection

points in the lower carrier are: $x_{r2} = \pi M \sin y + 3\pi$ and $x_{f2} = -\pi M \sin y + 3\pi$ when the output voltage varies between -½V_{dc} and 0.

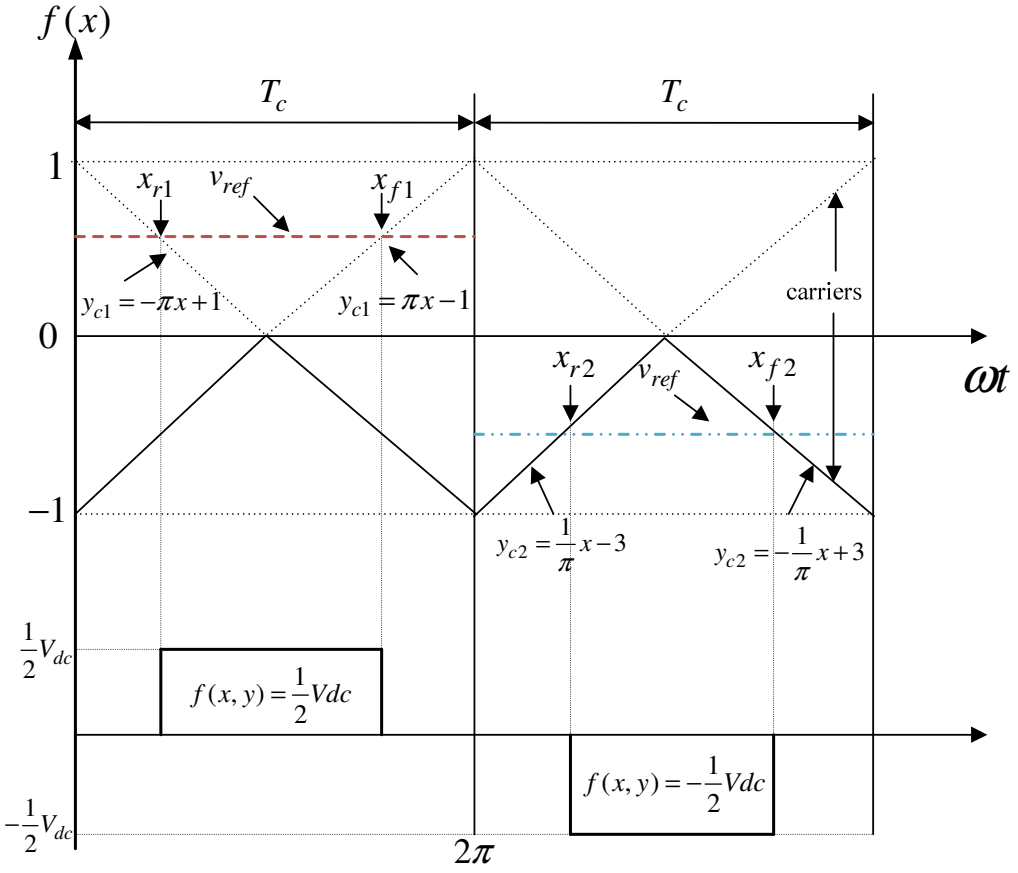


Figure 3-8: Two cycles of reference and carrier signal waveforms by using POD/APOD carrier (where in the first cycle, the reference is crossing the upper carrier, and in the second cycle, the reference is crossing the lower carrier).

$$C_{mn} = \frac{V_{dc}^2}{4\pi^2}\left[\int_0^{\pi}\int_{x_{r1}}^{x_{f1}} e^{j(mx+ny)}dxdy + \int_{\pi}^{2\pi}\left(\int_{x_{r2}}^{x_{f2}} e^{j(mx+ny)}dxdy\right)\right]$$

$$= \frac{V_{dc}}{\pi m}\sin\left(\frac{n\pi}{2}\right)J_n(m\pi M)$$

$$C_{00} = 0 \qquad (3.16)$$

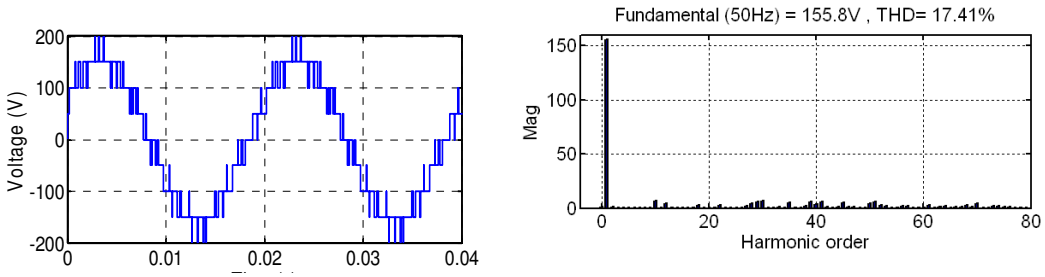
$$C_{01} = \frac{1}{2}MV_{dc}$$

$$C_{0n} = 0, \forall n > 1$$

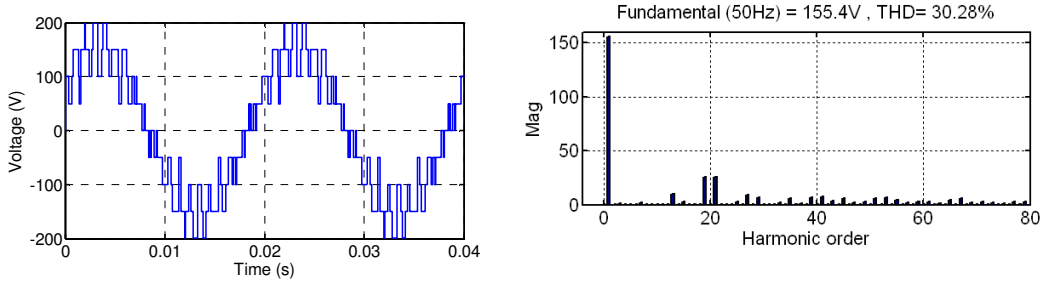
$$C_{m0} = 0, \forall m > 1$$

In three-level POD/APOD carrier PWM, the carrier harmonics are absent; only odd sideband harmonics spread around carrier components.

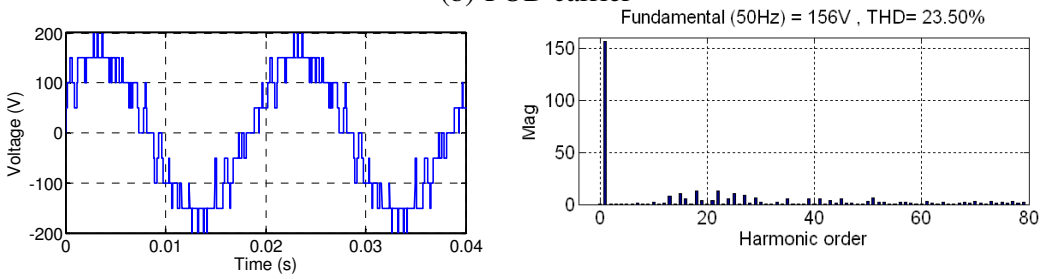
Simulations



(a) PD carrier



(b) POD carrier



(c) APOD carrier

Figure 3-9: Line voltage and spectrum of a five-level Diode-Clamped Converter with PD, POD and APOD carriers ($M=0.8$, $V_{dc}=200V$,$f_c=1000Hz$).

Based on the simulation results (Figure 3-9), PD PWM provides lower THD than POD and APOD. This is because in the PD PWM scheme, the carrier harmonic components are common to the phase-leg voltages and cancel in the line-to-line voltage. This makes the PD PWM scheme superior to the other two PWM schemes, thus PD PWM will be used in this thesis.

3.2.2 Third Harmonic Reference Injection

Third Harmonic Injection was firstly introduced in 1975 by Buja and Indri [14]. The main purpose of the injection is to increase the maximum modulation index of a three-phase converter system by including a certain amount of common mode third order harmonic in to PWM reference signal of each phase. This third order harmonic

component only exists in the output phase voltage not the line-to-line output voltage, since the common mode component is cancelled in the three-phase system. If the three-phase output phase voltage reference waveforms are:

$$\begin{aligned} V_{a(ref+3rd)} &= V_{dc}[M\cos\omega t + M_3\cos 3\omega t] \\ V_{b(ref+3rd)} &= V_{dc}[M\cos(\omega t - 120^\circ) + M_3\cos 3\omega t] \\ V_{c(ref+3rd)} &= V_{dc}[M\cos(\omega t + 120^\circ) + M_3\cos 3\omega t] \end{aligned} \tag{3.17}$$

The line-to-line voltage V_{ab} will be calculated as:

$$\begin{aligned} V_{ab} &= V_{a(ref+3rd)} - V_{b(ref+3rd)} = V_{dc}[M\cos\omega t - M\cos(\omega t - 120^\circ)] \\ &= MV_{dc}[\frac{3}{2}\cos\omega t - \frac{\sqrt{3}}{2}\sin\omega t] = \sqrt{3}MV_{dc}\cos(\omega t + 30^\circ) \end{aligned} \tag{3.18}$$

From (3.18) it can be observed that the third order component is cancelled in the line-to-line output voltage.

To calculating the magnitude of the third order harmonic injected to the sinusoidal reference waveform, (3.17) is divided by MV_{dc}. Equations (3.17) and (3.18) can be redefined in the per unit system:

$$v = \cos\theta + k\cos 3\theta \tag{3.19}$$

Where $k = M_3 / M$ represents the parameter to be optimized to reduce the maximum value of the function below unity. The maximum value of (3.19) is defined at the point where its derivative is zero, as shown in (3.20):

$$\frac{dv}{dt} = \cos\theta + k\cos 3\theta = \sin\theta + 3k\sin 3\theta = 0 \tag{3.20}$$

Substituting $\sin 3\theta = (4\cos^2_\theta - 1)\sin\theta$ into (3.19) the expression of v can be obtained:

$$v = -\frac{1}{3}(3k-1)\sqrt{\frac{3k-1}{3k}} = -\frac{1}{3}(3k-1)\sqrt{1-\frac{1}{3}k} \tag{3.21}$$

The maximum value of v can be obtained the derivative with respect to k is equal to zero:

$$\frac{dv}{dk} = -\sqrt{1-\frac{1}{3}k}(1+\frac{1}{6k}) = 0 \tag{3.22}$$

So k has two possible values:

$$k = \frac{1}{3} \text{ or } k = -\frac{1}{6}$$

The value of $k = -\frac{1}{6}$ produces a maximum of $v = \sqrt{3}/2$, recalculating that $V_a = MV_{dc}$, the maximum phase output voltage can be obtained:

$$v_{a,\max} = \sqrt{3}/2MV_{dc}$$

Hence the modulation index M increases to $2/\sqrt{3}$=1.15 before phase voltage v exceeds one per unit.

This analysis shows that the modulation index can be increased by 15.5% by including a one-sixth third order harmonic into the target reference sinusoidal waveform.

Figure 3-10 shows a five-level phase voltage PD PWM reference waveform with 1/6 third harmonic injection, (*M=1,f_c=1000Hz).*

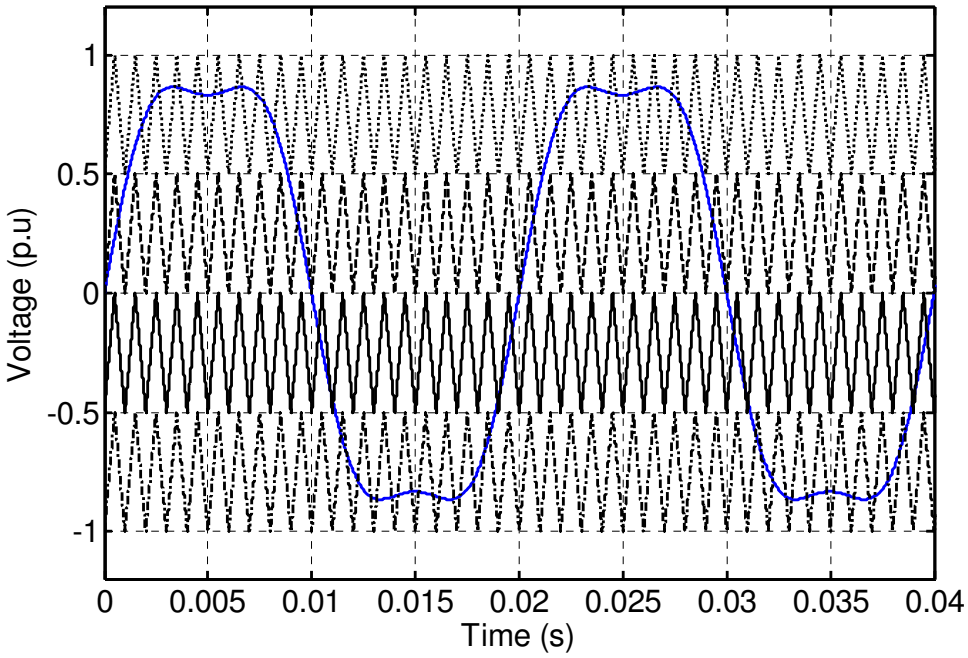


Figure 3-10: Five-level phase voltage PD PWM reference waveform with 1/6 third harmonic injection, (*M=0.8, f_c=1000Hz).*

3.3 SHE-PWM

SHE-PWM offers tight control of the harmonic spectrum of a given voltage waveform with a low number of switching transitions. However, many switching angles must be calculated based on the order harmonics to be cancelled, thus the system is non-linear and transcendental equations with trigonometrically terms need to be solved [8, 9].

Bipolar SHE-PWM is a switching scheme involving harmonic elimination that has been widely applied for many years to conventional two-level converters in both single- and three-phase systems. The angles are distributed to the two level transitions of the first quarter period. Assuming that there are *k* switching instants between zero and the first level are *k* (where *k* is always an odd number) and the total number of switching actions is equal to *N*, the equations describing SHE-PWM is given in equation (3.23) [5, 15-17].

$$\begin{aligned}
&\sum_{i=1}^{k}(-1)^{-1}\cos(\alpha_i)+\sum_{i=k+1}^{N}(-1)^{i-1+k}\cos(\alpha_i)=\frac{\pi}{4}M\\
&\sum_{i=1}^{k}(-1)^{-1}\cos(5\alpha_i)+\sum_{i=k+1}^{N}(-1)^{i-1+k}\cos(5\alpha_i)=0\\
&\sum_{i=1}^{k}(-1)^{-1}\cos(n\alpha_i)+\sum_{i=k+1}^{N}(-1)^{i-1+k}\cos(n\alpha_i)=0
\end{aligned} \qquad (3.23)$$

Where: α_i are the switching angles for each switching instant, and ($\alpha_1 < \alpha_2 < \cdots < \alpha_n < \frac{2}{\pi}$). i is the number of harmonics to be eliminated.

As an example, if 5th, 9th, 7th and 11th order harmonic are going to be cancelled and the magnitude of the fundamental component is 0.9 per unit, the nonlinear equations are calculated to yield four α angles:

$$\alpha_1 = 11.78^\circ, \alpha_2 = 23.02^\circ, \alpha_3 = 41.69^\circ, \alpha_4 = 48.79^\circ$$

Figure 3-11 shows the phase voltage and its spectrum of a two-level converter with SHE that cancels the 5th, 7th and 11th order harmonics (the 9th is co-phasal and is hence cancelled in three-phase system).

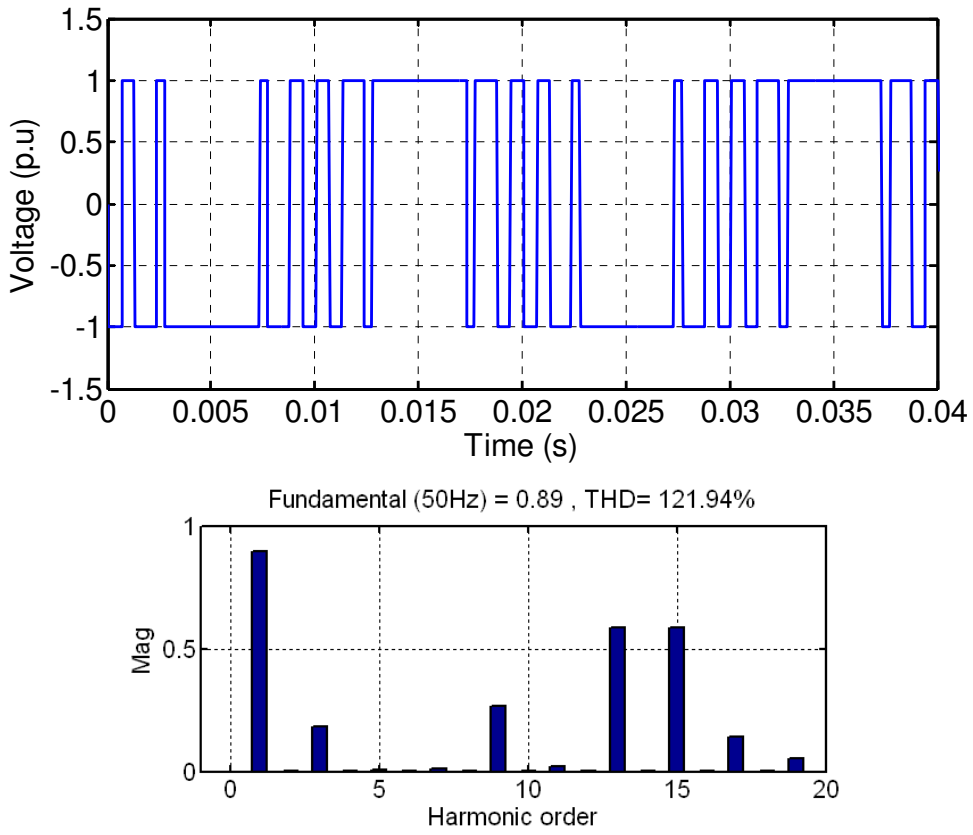


Figure 3-11: Phase voltage and its spectrum of a two-level converter with selective harmonic elimination that cancel 5^{th}, 7^{th} and 11^{th} order harmonic.

3.4 Summary

The main PWM techniques discussed, analysed and simulated in this chapter are carrier-based modulation and SHE modulation. Phase disposition PWM is selected and used in this thesis due to its superior harmonic performance over its counterparts. A review of third harmonic injection into the modulating waveform to increase modulation index has been presented.

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CHAPTER 4

4 Modular Multilevel Converters

4.1 Introduction

The Modular Multilevel Converter is an emerging multilevel converter topology which was introduced in 2001[1-4]. This topology is highly attractive for medium and high voltage application e.g. Medium Voltage Drive and HVDC applications. It has been used in the first commercial application of multilevel HVDC converter known as HVDC PLUS [5]. The structure of the modular multilevel converter allows to operate at high voltage with low harmonic content without the use of ac filters (where is appropriate), and without the need to increase the switching frequency [6].
This topology overcomes the main disadvantages of the conventional multilevel converter and provides a set of attractive features:

- Modular construction: Within each module, the voltage level is clamped and may be set to a level compatible with single device voltage rating. By using a proper control strategy, the identical modular cells are scalable to different output voltage levels.
- Capacitor balancing is feasible for any number of levels, regardless of operation conditions.
- Low Total Harmonic Distortion and low stress on each switching device.
- Failure management: Protection of all converter cells against mechanical destruction in the case of a short circuit or insulation failure. Because of the realization of redundancy, a failed cell can be replaced by a redundant cell in the arm which gives flexibility.
- Low manufacturing cost: with increased voltage levels, harmonic filters size can be reduced, resulting in a significant cost reduction.

4.2 Operating Principle

The principle of operation of the modular multilevel converter was discussed in [7-10]. Figure 4-1 shows the three-phase modular converter with N cells per arm. Each converter phase generates N voltage levels at output phases a, b and c referred to the supply mid-point '0'. The voltage across each cell capacitor is $\frac{1}{N} V_{dc}$ and the voltage stress across each switching device is limited to one capacitor voltage. Arm inductance L limits the inrush and circulating currents due to instantaneous voltage imbalance in the cell capacitors and the possibility of capacitors connected across the dc link having a voltage that does not sum to the dc link voltage during cell switching state changes. Proper converter operation requires a robust capacitor voltage balancing strategy to ensure that the voltage across each switching device is controlled over the entire operating range [11, 12].

Figure 4-2 shows one phase of a three-level modular multilevel converter. Each cell consists of two switching devices. When the switch S_m is turned on and S_a is off, the output voltage is 0. When the switch S_a is turned on and S_m is off, the output voltage is V_{dc}. The two switches in each cell must be operated in a complementary manner. Each capacitor voltage in each cell must be maintained at ½V_{dc}. The four main switches are $S_{m1}, S_{m2}, S_{m3}, S_{m4}$, and the four auxiliary switches are $S_{a1}, S_{a2}, S_{a3}, S_{a4}$ which comprise four complementary switch pairs (S_{m1}, S_{a1}), (S_{m2}, S_{a2}), (S_{m3}, S_{a3}), (S_{m4}, S_{a4}). In the three-level converter, there are 3 output voltage states: 0 and ±½V_{dc}. Assuming the dc source midpoint as the output voltage reference, there are six switch combinations that synthesize three output voltage levels. At each instant the leg must be controlled so that the upper and lower arm voltages sum to V_{dc}.

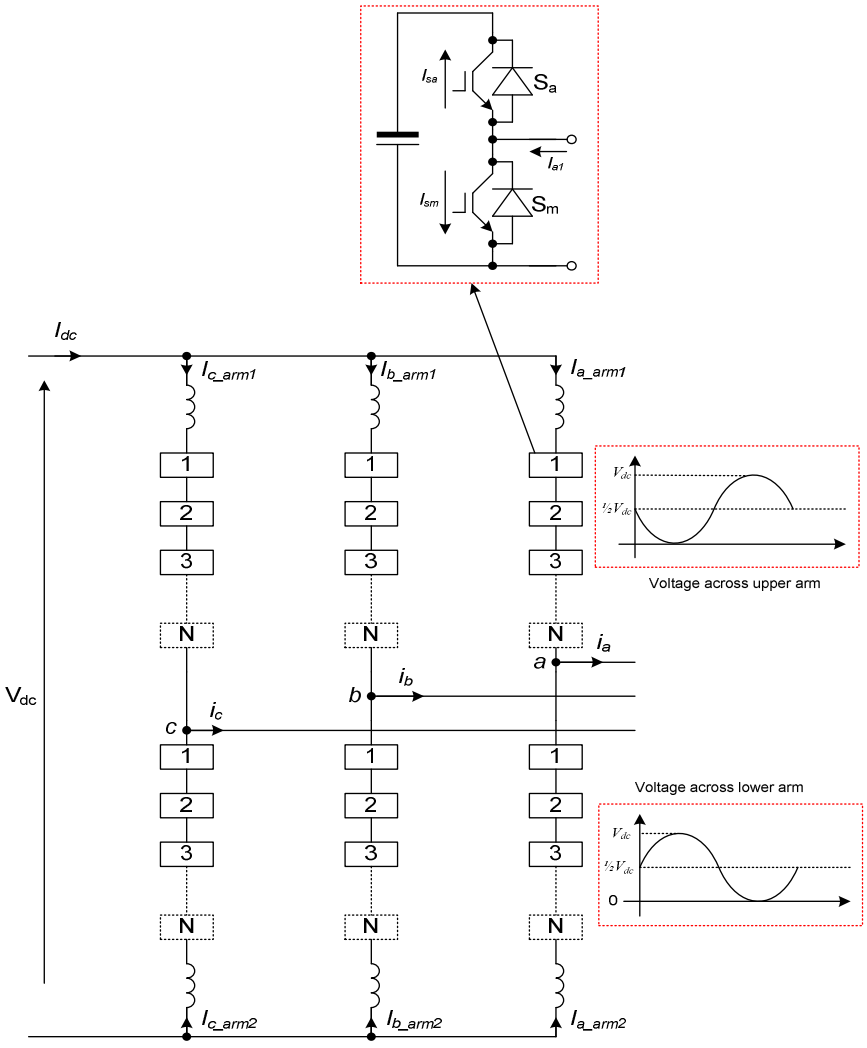


Figure 4-1: Three-phase of the *N*-level M2C.

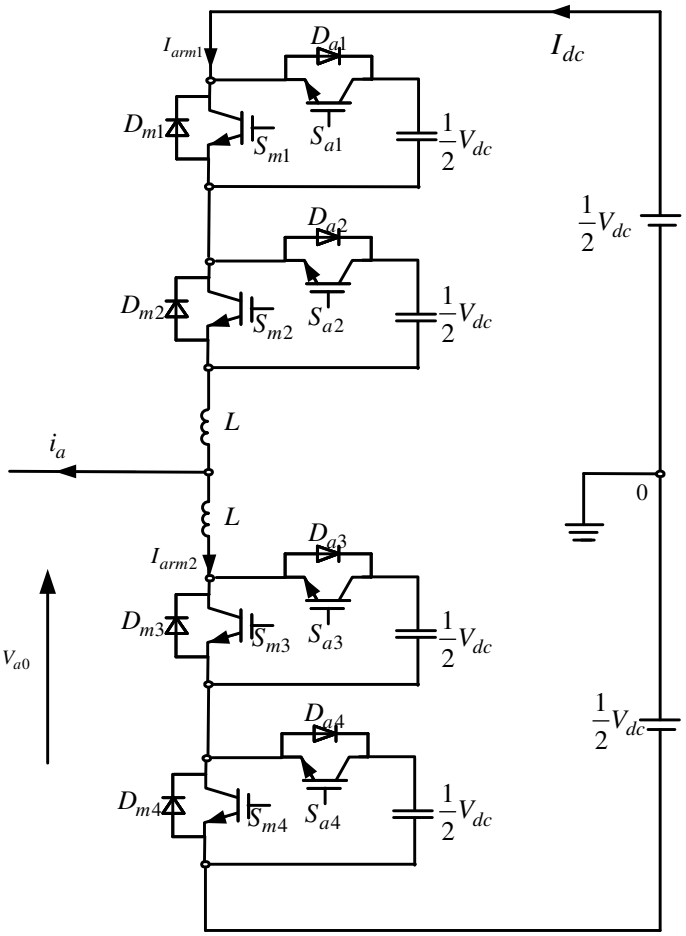


Figure 4-2: Phase 'a' of a 3-level M2C.

For voltage level $V_{a0} = \frac{1}{2}V_{dc}$, S_{m1}, S_{m2} from the upper arm and S_{a3}, S_{a4} from the lower arm, are on.

For voltage level $V_{a0} = 0,$ the four switch combinations are:

S_{m1}, S_{m3} and S_{a2}, S_{a4} on

S_{m2}, S_{m3} and S_{a1}, S_{a4} on

S_{m2}, S_{m4} and S_{a1}, S_{a3} on

S_{m1}, S_{m4} and S_{a2}, S_{a3} on

For voltage level $V_{a0} = -\frac{1}{2}V_{dc}$, S_{a1}, S_{a2} from the upper arm and S_{m3}, S_{m4} from the lower arm, are on.

Table 4-1 summarizes all the switch states and conduction loop. 1 indicates that a switch is turned on and 0 indicates that a switch is turned off.

Table 4-1: Switching state of three-level M2C.

Switching States				V_{ao}	Conducting devices	
S_{m1}	S_{m2}	S_{m3}	S_{m4}		$i_a > 0$	$i_a < 0$
1	1	0	0	$1/2V_{dc}$	$S_{m1}, S_{m2}, S_{a3}, S_{a4}$	$D_{m1}, D_{m2}, D_{a3}, D_{a4}$
1	0	1	0	0	$S_{m1}, D_{a2}, D_{m3}, S_{a4}$	$D_{m1}, S_{a2}, S_{m3}, D_{a4}$
0	1	1	0		$D_{a1}, S_{m2}, D_{m3}, S_{a4}$	$S_{a1}, D_{m2}, S_{m3}, D_{a4}$
0	1	0	1		$D_{a1}, S_{m2}, S_{a3}, D_{m4}$	$S_{a1}, D_{m2}, D_{a3}, S_{m4}$
1	0	0	1		$S_{m1}, D_{a2}, S_{a3}, D_{m4}$	$D_{m1}, S_{a2}, D_{a3}, S_{m4}$
0	0	1	1	$-1/2V_{dc}$	$D_{m1}, D_{m2}, D_{a3}, D_{a4}$	$S_{m1}, S_{m2}, S_{a3}, S_{a4}$

4.3 Pulse width modulation

In regard to a modular and scalable topology, the applied modulation scheme should be expandable to any voltage level number. Therefore, at lower numbers of voltage levels, a carrier-based strategy is used to control the switching states. As the number of voltage levels increases, carrier-based PWM can be replaced by a 'staircase' type modulation. By using a phase disposition (PD) carrier strategy, the *n*-level M2C needs *n*-1 triangular carriers, with the same frequency and amplitude, from 1 to -1 [13, 14]. A sinusoidal reference waveform (with triplens if desired) is compared to the triangular carrier waveforms and the gate signal to each IGBT is controlled according to the comparison results. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is switched off.

For a modular multilevel converter, the modulation index, *m*, and the frequency ratio, m_f, are defined as for conventional multilevel PWM [15, 16]:

$$m = \frac{2A_m}{(n-1)A_c} \tag{4.1}$$

$$m_f = \frac{f_c}{f_m} \tag{4.2}$$

Where A_m and A_c denote the amplitudes of the modulating and carrier signals respectively, and f_m and f_c denote their respective frequencies.

4.3.1 Illustrative example: three-level capacitor voltage balancing method

Figure 4-3 shows two triangular carrier waveforms and one sinusoidal reference waveform. When the reference signal is greater than the upper triangular signal the output voltage level equals ½V_{dc}, and when the reference signal is less than the lower triangular signal, the output voltage level equals -½V_{dc}. The last condition is voltage level 0 which can be generated by 4 different conditions. These combinations are referred to as redundant switch states. In a modular multilevel converter, the redundant switch states are groups of switch states that produce the same phase voltage rather than the line-to-line voltage, as in the case of conventional multilevel converters.

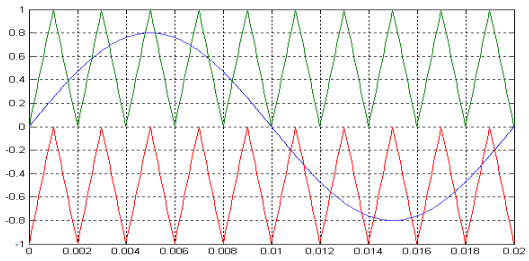


Figure 4-3: Carrier and reference waveforms for 3-level M2C.

If phase *a* is connected to either the positive or negative dc rails to synthesize voltage levels ½V_{dc} and -½V_{dc}, the load connection has no effect on the capacitor voltages. When phase a is connected to the zero level, the upper capacitor always charges during the positive half of the load current ($i_a > 0$), while the lower capacitors discharge during the negative half of the load current ($i_a < 0$), the upper capacitors discharge while the lower capacitor charge.

Figure 4-4 shows four switch combinations when phase *a* is attached to the zero voltage level. The load connection in Figure 4-4(a) represents the switch combination (1010) which can cause voltage imbalance due to the connection of one output phase to the point between capacitor C_2 and C_4. If the current direction indicated in Figure 4-4a is assumed positive, for $i_a > 0$ the lower capacitor C_4 discharges and upper capacitor C_2 charges, while the upper capacitor discharges and the lower charges for $i_a < 0$.

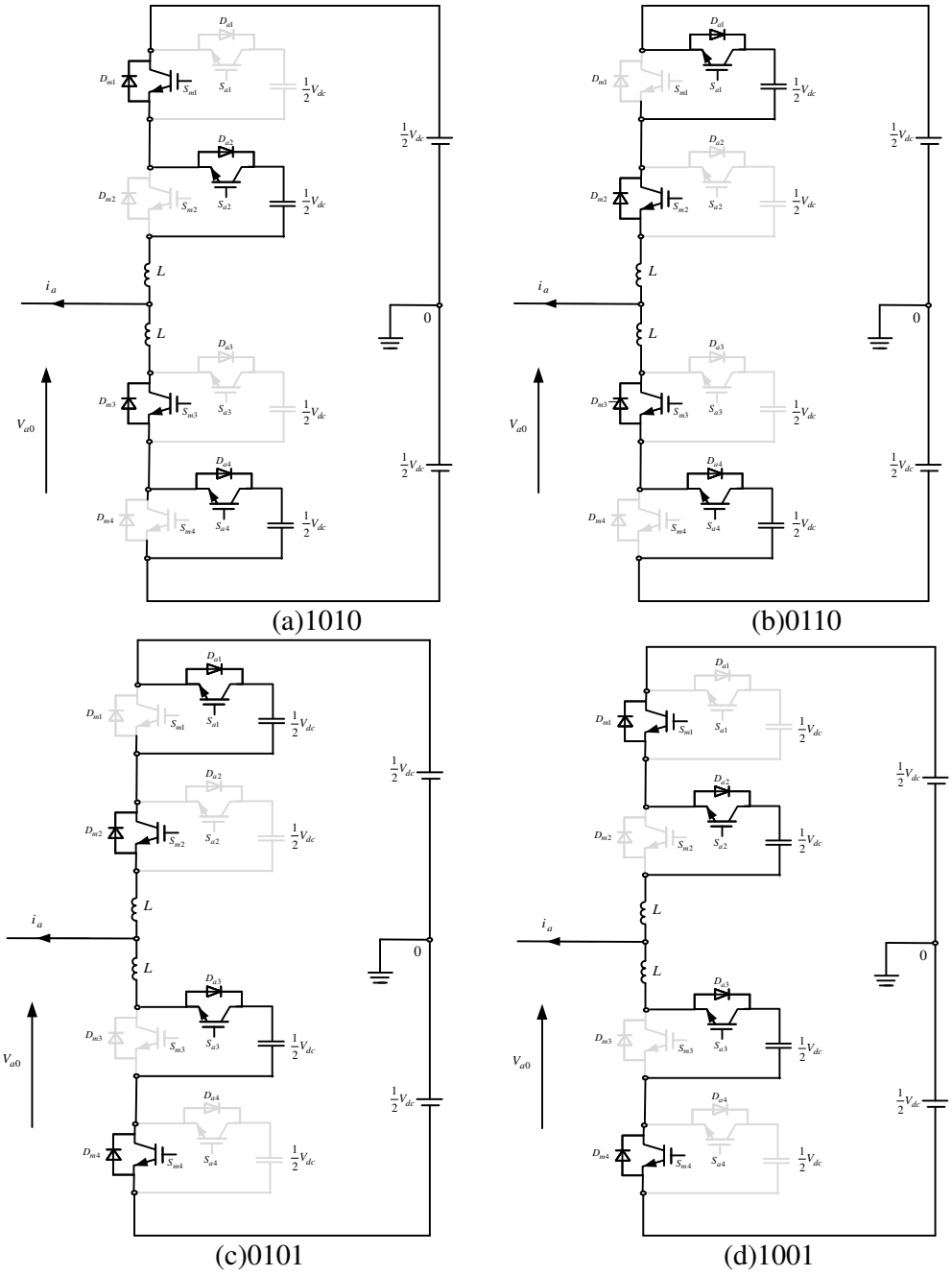


Figure 4-4: Four possible load connection to zero voltage level in a three-level M2C.

The load connection shown in Figures 4-4(a)-(d) represent the redundant switch states (1010, 0110, 0101, 1001) which are effective for balancing purposes because the upper and lower capacitors are alternatively used as energy tanks to supply power to the load. Any capacitor voltage balancing strategy using carrier-based or space vector modulation must use these switch combinations periodically and for a relatively short duration in order to compensate for capacitor voltage error. Table 4-2 summarizes all of the switch combinations and their effect on each capacitor voltage.

Table 4-2: Effect of redundant switch states of three-level modular converter on capacitor voltage.

Switch states	Load current		Effect on capacitors voltages
	Direction	Path	
(A) 1010	$i_a > 0$	$S_{m1}D_{a2} \& S_{a4}D_{m3}$	$C_2 \uparrow$ and $C_4 \downarrow$
	$i_a < 0$	$S_{a2}D_{m1} \& S_{m3}D_{a4}$	$C_4 \uparrow$ and $C_2 \downarrow$
(B)0110	$i_a > 0$	$S_{m2}D_{a1} \& S_{a4}D_{m3}$	$C_1 \uparrow$ and $C_4 \downarrow$
	$i_a < 0$	$S_{a1}D_{m2} \& S_{m3}D_{a4}$	$C_4 \uparrow$ and $C_1 \downarrow$
(C)0101	$i_a > 0$	$S_{m2}D_{a1} \& S_{a3}D_{m4}$	$C_1 \uparrow$ and $C_3 \downarrow$
	$i_a < 0$	$S_{a1}D_{m2} \& S_{m4}D_{a3}$	$C_3 \uparrow$ and $C_1 \downarrow$
(D)1001	$i_a > 0$	$S_{m1}D_{a2} \& S_{a3}D_{m4}$	$C_2 \uparrow$ and $C_3 \downarrow$
	$i_a < 0$	$S_{a2}D_{m1} \& S_{m4}D_{a3}$	$C_3 \uparrow$ and $C_2 \downarrow$

Where: $\uparrow$ means the capacitor is charged, $\downarrow$ means the capacitor is discharged.

Based on these facts, the developed capacitor voltage balancing method for a three-level converter can be summarized as followed:

i. The capacitor voltages are measured periodically, and the upper group and lower group are sorted in ascending voltage order.
ii. During positive load current, select a switch state that charges the upper capacitor with the minimum voltage and discharges the lower capacitor with the maximum voltage.
iii. During negative load current, select a switch state that charges the upper capacitor with the maximum voltage and discharges the lower capacitor with the minimum voltage.

By this method, the voltage balance of the cell capacitors is maintained.

4.3.2 Five-level capacitor voltage balancing method

In the five-level modular converter shown in Figure 4-5, there are 70 switch states for each phase (Table 4-3). These switch states can be used collectively to generate a five-level waveform in each phase of the converter.

The capacitor balancing strategy for a five-level modular converter is similar to that for a three-level modular converter, and can be summarized as followed:

i. $V_{ao} = ½V_{dc}$:

$i_a > 0$	$S_{mj} = 1 \& S_{m(j+4)} = 0$	j varies from 1 to 4.
$i_a < 0$	$S_{mj} = 1 \& S_{m(j+4)} = 0$	

ii. $V_{ao} = ¼V_{dc}$:

$i_a > 0$	One capacitor from the upper group with the minimum voltage to be charged. Three capacitors from the lower group with the maximum voltages to be discharged.
$i_a < 0$	One capacitor from the upper group with the maximum voltage to be discharged Three capacitors from the lower group with minimum voltage to be charged.

iii. $V_{ao} = 0$:

$i_a > 0$	Two capacitors from the upper group with the minimum voltage to be charged Two capacitors from the lower group with the maximum voltages to be discharged.
$i_a < 0$	Two capacitors from the upper group with the maximum voltage to be discharged Two capacitors from the lower group with minimum voltage to be charged.

iv. $V_{ao} = -¼V_{dc}$:

$i_a > 0$	Three capacitors from the upper group with the minimum voltage to be charged. One capacitor from the lower group with the maximum voltages to be discharged.
$i_a < 0$	Three capacitors from the upper group with the maximum voltage to be discharged One capacitor from the lower group with minimum voltage to be charged.

v. $V_{ao} = -½V_{dc}$:

$i_a > 0$	$S_{mj} = 0 \& S_{m(j+4)} = 1$	j varies from 1 to 4.
$i_a < 0$	$S_{mj} = 0 \& S_{m(j+4)} = 1$	

Table 4-3: Summary of the effect of five-level modular converter switch state on capacitor voltage.

voltage levels	No. of switching states	Current direction & capacitors condition	
		$i_a > 0$	$i_a < 0$
½V_{dc}	1	$C_j \rightarrow \& C_{j+4} \downarrow$	$C_j \rightarrow \& C_{j+4} \uparrow$
+¼V_{dc}	$(C_1^4)^2 = 16$	$C_{1\_\min}^{upper4} \uparrow \& C_3^{upper4} \rightarrow$ $C_{3\_\max}^{lower4} \downarrow \& C_1^{lower4} \rightarrow$	$C_{1\_\max}^{upper4} \downarrow \& C_3^{upper4} \rightarrow$ $C_{3\_\min}^{lower4} \uparrow \& C_1^{lower4} \rightarrow$
0	$(C_2^4)^2 = 36$	$C_{2\_\min}^{upper4} \uparrow \& C_2^{upper4} \rightarrow$ $C_{2\_\max}^{lower4} \downarrow \& C_2^{lower4} \rightarrow$	$C_{2\_\max}^{upper4} \downarrow \& C_2^{upper4} \rightarrow$ $C_{2\_\min}^{lower4} \uparrow \& C_2^{lower4} \rightarrow$
-¼V_{dc}	$(C_1^4)^2 = 16$	$C_{3\_\min}^{upper4} \uparrow \& C_1^{upper4} \rightarrow$ $C_{1\_\max}^{lower4} \downarrow \& C_3^{lower4} \rightarrow$	$C_{3\_\max}^{upper4} \downarrow \& C_1^{upper4} \rightarrow$ $C_{1\_\min}^{lower4} \uparrow \& C_3^{lower4} \rightarrow$
-½V_{dc}	1	$C_j \uparrow \& C_{j+4} \rightarrow$	$C_j \downarrow \& C_{j+4} \rightarrow$

Definitions: notation $C_{1\_\min}^{upper4}$ means choose one capacitor with minimum voltage from upper 4 capacitors.

Where: j varies from 1 to 4, $\uparrow$ means the capacitor is charged, $\downarrow$ means the capacitor is discharged and $\rightarrow$ means the capacitor state remains unchanged.

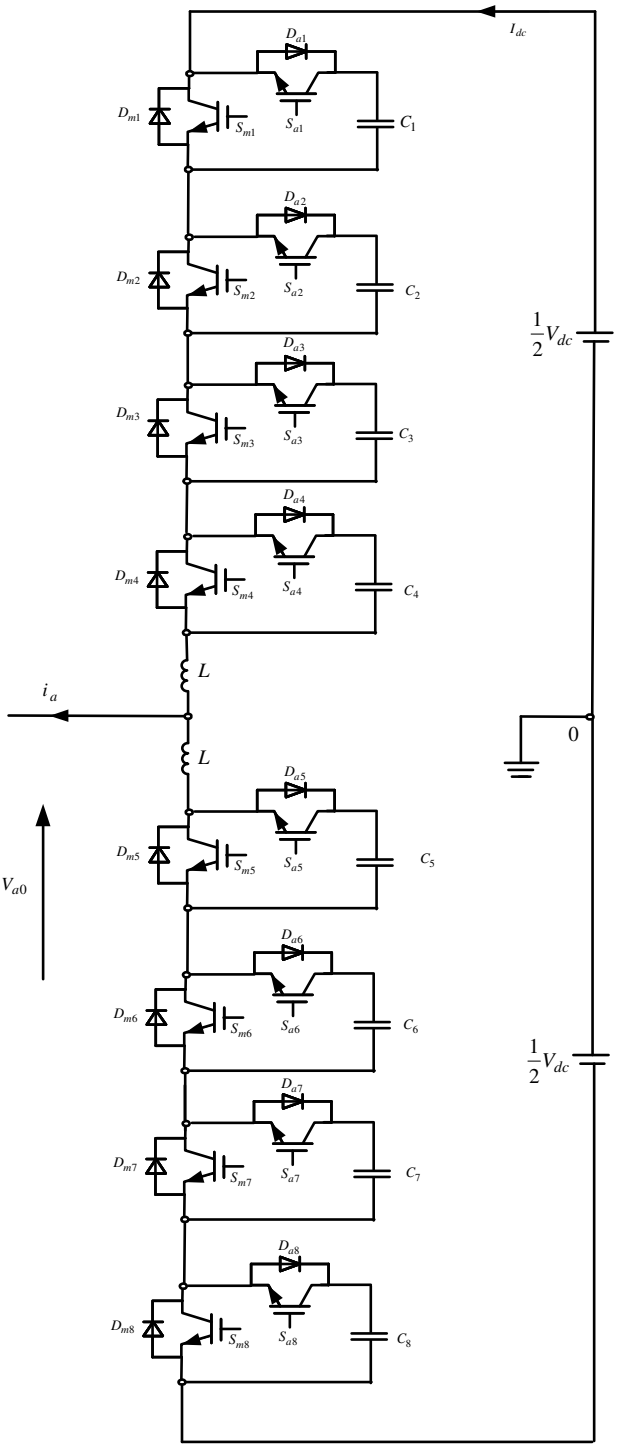


Figure 4-5: One phase of a 5-level M2C.

4.4 Mathematical analysis

4.4.1 Cell capacitors sizing

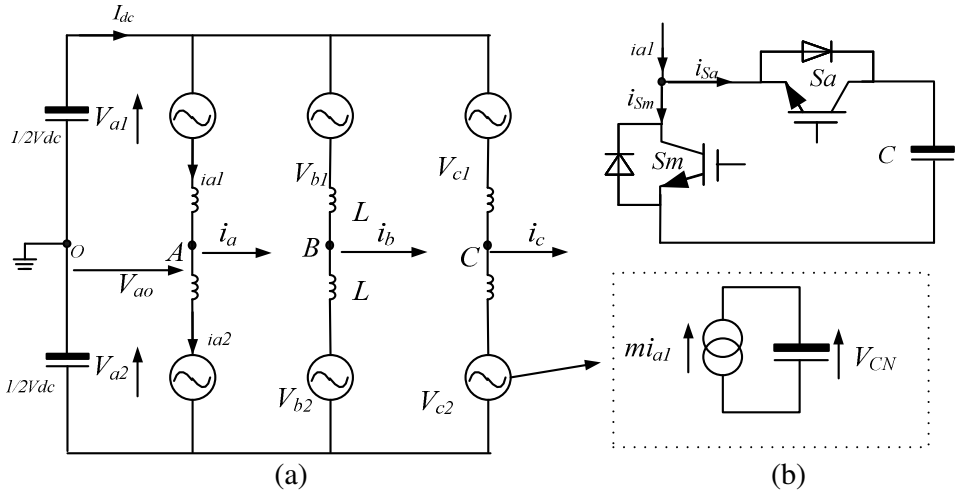


Figure 4-6: (a) linear model for M2C and (b) Current distribution in one cell.

Figure 4-6 shows an averaged bulk model for an M2C circuit, M2C cells in each arm are considered to be a controllable voltage sources. In each cell, two IGBTs are considered as a controllable current source, where the current magnitude is decided by modulation index *m*. From Figure 4-6, it can be derived that Modular multilevel converter upper and lower arm voltages in the same phase leg are defined by:

$$V_{a1}(t) = \tfrac{1}{2}V_{dc}(1 - m\sin\omega t)$$
$$V_{a2}(t) = \tfrac{1}{2}V_{dc}(1 + m\sin\omega t) \tag{4.3}$$

Where V_{dc}, *m,* and ω represent total converter dc link voltage, modulation index and output voltage fundamental frequency in rad/s respectively. Assuming the converter is lossless, the power balance equation can be expressed as:

$$P_{dc} = V_{dc}I_{dc} = 3\times\tfrac{1}{2}V_m I_m \cos\varphi = P_{ac\_3\phi} \tag{4.4}$$

Since for sinusoidal pulse with modulation, $V_m = \tfrac{1}{2}mV_{dc}$, the dc current component per arm is:

$$\tfrac{1}{3}I_{dc} = \tfrac{1}{4}mI_m \cos\varphi \tag{4.5}$$

Where phase current $i_a = I_m \sin(\omega t - \varphi)$. Thus, the arm current of the phase 'a' can be expressed as:

$$I_{a1} = \tfrac{1}{3}I_{dc} + \tfrac{1}{2}i_a \tag{4.6}$$

Combining equations (4.5) and (4.6), the arm current can be expressed as:

$$I_{a1} = \tfrac{1}{3} I_{dc}\left[1 + \frac{2}{m\cos\varphi}\sin(\omega t - \varphi)\right] \tag{4.7}$$

Letting $q = \dfrac{2}{m\cos\varphi}$, equation (4.7) can be rewritten as:

$$I_{a1} = \tfrac{1}{3} I_{dc}\left[1 + q\sin(\omega t - \varphi)\right] \tag{4.8}$$

For cell capacitance sizing, assume all six arms of the converter contribute equal power. Therefore the instantaneous power the upper arm exchanges with the ac side is:

$$P_{arm1} = \tfrac{1}{2} V_{dc}(1 - m\sin\omega t) \times \tfrac{1}{3} I_{dc}(1 + q\sin(\omega t - \varphi)) \tag{4.9}$$

The average power the upper arm exchanges with the ac side over the full fundamental cycle is:

$$\overline{P}_{arm1} = \frac{1}{2\pi}\int_0^{2\pi} \tfrac{1}{2} V_{dc}(1 - m\sin\omega t) \times \tfrac{1}{3} I_{dc}(1 + q\sin(\omega t - \varphi))\, d\omega t = \tfrac{1}{6} P_{dc}(1 - \tfrac{1}{2} qm\cos\varphi) \tag{4.10}$$

By substituting $q = \dfrac{2}{m\cos\varphi}$ in equation (4.10), it reduces to zero. This demonstrates the natural balancing of the modular converter cell capacitors if they are modulated correctly.

For cell capacitance sizing of the modular converter with *N* cells per arm, the total pulsation energy can be obtained from the integration of P_{arm1} between θ_1 and θ_2.

Where: $\theta_1 = -\sin^{-1}(\dfrac{1}{q}) + \varphi$

$$\theta_2 = \pi + \sin^{-1}(\frac{1}{q}) + \varphi$$

Where θ_1 and θ_2 are the zero crossing points of the current defined by equation (4.8) and provide the limits of integration to enable calculation of the cell capacitor pulsation energy.

Therefore, the total exchanged energy between the capacitor and the ac side can be expressed as:

$$W_c = \frac{1}{\omega}\int_{\theta_1}^{\theta_2} \tfrac{1}{2}V_{dc}(1 - m\sin\omega t) \times \tfrac{1}{3}I_{dc}(1 + q\sin(\omega t - \varphi))d\omega t$$
$$= \frac{1}{3\cdot\omega} P_{dc}\cdot q\cdot(1-\frac{1}{q^2})^{3/2} \tag{4.11}$$

The Pulsation of energy per each cell for N cell in one arm is:

$$W_c = \frac{1}{3\cdot\omega\cdot N} P_{dc}\cdot q\cdot(1-\frac{1}{q^2})^{3/2} \tag{4.12}$$

For a three-level modular converter, N=2 and $q = \frac{2}{m\cos\varphi}$. Therefore equation (4.12) reduces to (4.13):

$$W_c = \tfrac{1}{3}P_{dc}\frac{(2-m^2)}{\omega m} \tag{4.13}$$

Assuming the cell capacitor maximum and minimum voltages are V_{cmax} and V_{cmin} respectively, the pulsating energy each cell capacitor exchanges with ac side is:

$$W_c = \tfrac{1}{2}C\left(V_{c\max}^2 - V_{c\min}^2\right) = C\left(V_{c\max} - V_{c\min}\right)\tfrac{1}{2}\left(V_{c\max} + V_{c\min}\right) = C\Delta V_{\max}\overline{V}_c \tag{4.14}$$

where C is cell capacitance, ΔV_{max} is the maximum allowable voltage ripple, and $\overline{V}_c$ is average cell voltage. By equating equations (4.12) and (4.13), the cell capacitance is:

$$C = \frac{P_{dc}(2-m^2)}{3\omega m\Delta V_{\max}\overline{V}_c} \tag{4.15}$$

Assuming $\overline{V}_c = \tfrac{1}{2}V_{dc}$ and $\xi = \frac{\Delta V_{c\max}}{\overline{V}_c}$ (percentage voltage ripple), equation (4.15) can be rewritten as:

$$C = \frac{P_{dc}(2-m^2)}{3\omega m\xi\overline{V}_c^2} = \frac{4P_{dc}(2-m^2)}{3\omega m\xi V_{dc}^2} \tag{4.16}$$

From equation (4.16), the converter is design to operate at high modulation indices requiring relatively small cell capacitance compared to those designed to operate at low modulation indices. Also, the lower the cell voltage, the larger the cell capacitance. For example, a 20kV, 20MW converter, the cell capacitance required such that the voltage does not exceed 5% when operated at 0.9 modulation index is:

$$C = \frac{20\times10^6\times(2-0.9^2)}{3\times2\pi\times50\times0.9\times0.05\times(10\times10^3)^2} \approx 5mF$$

4.4.2 Capacitor voltage ripple

The modular multilevel converter cell capacitors experience relatively high voltage due to the flow of the fundamental current component through the capacitors. Therefore, the capacitors are required to store more energy than in two-level and neutral-point clamped converters in order to maintain the cell capacitor voltage ripple across within acceptable limits. The cell capacitor voltage can be expressed using a linearized switching function. If the phase current is assumed constant within each switching cycle, the switching function can be replaced by device duty cycle. For the three-level modular multilevel converter controlled using SPWM for instance, when $0 \le \omega t \le \pi$, the time at voltage level $+½V_{dc}$ is $T_c m \sin \omega t$ and time at the 0 voltage level is $T_c(1 - m \sin \omega t)$ In the negative half cycle, the time at voltage level $-½V_{dc}$ is $-T_c m \sin \omega t$ and the time at 0 is $T_c(1 + m \sin \omega t)$. Output voltage levels $+½V_{dc}$ and $-½V_{dc}$ do not affect the state of charge of the cell capacitor. Only switch combinations that connect the output phase to '0' affect the state of charge of the cell capacitors. The time at the 0 voltage level is distributed equally between the cells capacitors, assuming the capacitor voltage balancing strategy that uses redundant switch states is ideal, and uses these capacitors for an equal period of time over the full fundamental cycle [17-19]. So, an expression for capacitor voltage can be based on one capacitor. The average current flowing through the capacitor in each cell can be expressed by:

$$\overline{i}_{sa} = \tfrac{1}{2}(1 - m \sin \omega t) i_{a1} \tag{4.17}$$

$$\overline{i}_{sm} = \tfrac{1}{2}(1 + m \sin \omega t) i_{a1} \tag{4.18}$$

Where: i_{a1} is the converter upper arm current, $\overline{i}_{sa}$ is the average current of the auxiliary switch s_a (the same as the capacitor current), and $\overline{i}_{sm}$ is the main switch average current (Figure 4-6). Therefore, the voltage across each cell capacitor can be related to the local average current that flows through the cell capacitor:

$$C \frac{dv_c}{dt} = \overline{i}_{sa} \tag{4.19}$$

Therefore, the voltage cross the capacitor C is:

$$\begin{aligned} v_c(\omega t) &= \frac{1}{\omega C} \int [\tfrac{1}{2}(1 - m \sin \omega t)(\tfrac{1}{3} I_{dc} + \tfrac{1}{2} I_m \sin(\omega t - \varphi))] d\omega t \\ &= \frac{1}{\omega C} [\tfrac{1}{6} I_{dc} m \cos \omega t - \tfrac{1}{4} I_m \cos(\omega t - \varphi) + \tfrac{1}{8} I_m \sin(2\omega t - \varphi)] + A \end{aligned} \tag{4.20}$$

If the capacitor initial voltage is ½V_{dc}, and recalculating that $\frac{1}{3}I_{dc} = \frac{1}{4}mI_m \cos\varphi$ the constant A is:

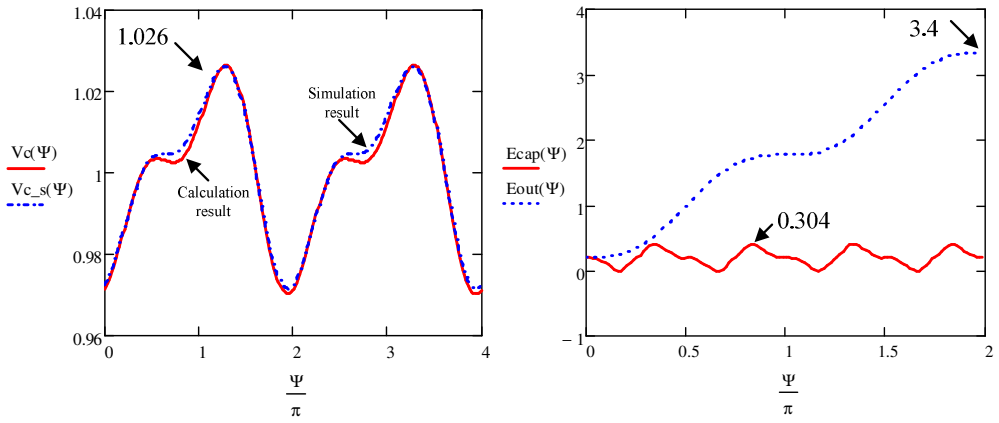
$$A = \tfrac{1}{2}V_{dc} - \frac{1}{\omega C}(\tfrac{1}{8}m^2 I_m \cos\varphi - \tfrac{1}{2}I_m \cos\varphi - \tfrac{1}{8}mI_m \sin\varphi) \tag{4.21}$$

Finally, the voltage across each cell capacitor C is:

$$\begin{aligned} v_c(\omega t) = {} & \tfrac{1}{2}V_{dc} + \frac{I_m}{\omega C}[\tfrac{1}{8}m^2 \cos\varphi\cos\omega t - \tfrac{1}{8}m^2 \cos\varphi \\ & + \tfrac{1}{8}m\sin(2\omega t - \varphi) - \tfrac{1}{2}\cos(\omega t - \varphi) + \tfrac{1}{2}\cos\varphi + \tfrac{1}{8}m\sin\varphi] \end{aligned} \tag{4.22}$$

The first term of the equation (4.22) represents the desired settling point of the capacitor voltage, while the remaining terms represent the ripple voltage which depends on cell capacitance, load power factor, modulation index, and phase current magnitude. Also, observe that the capacitor voltage ripple of the three-level M2C contains fundamental components and a second harmonic term. The second harmonic term in the capacitor voltage is related to the product of the sinusoidal modulation and the sinusoidal phase current.

Figure 4-7a shows the theoretical and simulation waveform of the capacitor ripple referred to ½V_{dc} and Figure 4-7b shows the peak stored energy by the cell capacitor and total output energy per cycle. The ratio of energy output over one cycle to peak energy stored by the cell capacitor is 0.204/3.4=6%. With a target system modulation index m=0.9 and load power factor *p.f.* =0.72 lagging.



(a) (b)

Figure 4-7: (a) Theoretical and simulation voltage waveform across the upper arm capacitor, (b) energy stored in cell capacitor bank and total output energy per cycle (b) when modulation index m=0.9 and load power factor p.f.=0.72 lagging.

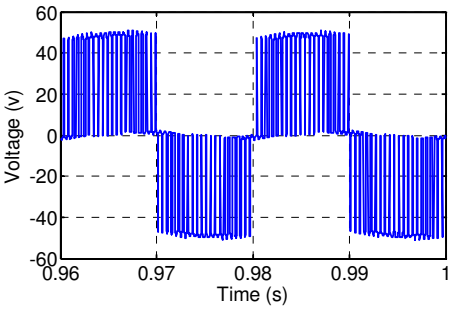
4.5 Simulations

To illustrate the ability of the modular multilevel converter to operate independently of load power factor and modulation index, the modular converter in Figure 4-1 is simulated under different operating conditions and with different cell numbers. Carrier-based SPWM and an embedded capacitor balancing strategy are used to control the converter switching devices in order to generate the desired output phase voltage and to force the capacitor voltages to follow their set points. A three-level M2C is simulated at dc voltage level of 100V and a switching frequency of 2.1kHz, to allow comparison with the experimental results. All other simulations are considered with dc rail voltage of 20kV, and a 2.1kHz switching frequency. The quality of the output voltage waveform and capacitor voltage balancing are evaluated [20, 21] by simulation at different modulation indices and load power factors.

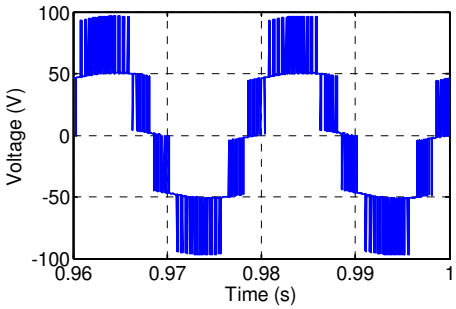
4.5.1 Simulations for three-level M2C

Case I: Modulation index m=0.9, power factor=0.72lagging

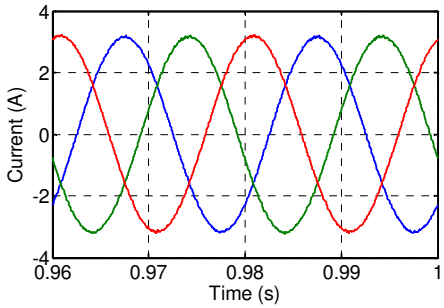
Figure 4-8 shows the simulation results obtained when the three-level converter with 1mF cell capacitors, and arm inductance of 3mH, operates at 0.9 modulation index and 0.72 power factor lagging. The ac side used an RL load with 25Ω resistance and 0.035H inductance (the same parameters are used experimentally). From the output voltage waveforms in Figure 4-8a and Figure 4-8b, phase and line voltage show that the modular converter generates high quality output voltage with relatively low harmonic content and low *dv/dt* (principle of minimum switching losses, one voltage level per switching cycle is maintained). Figure 4-8c shows that the modular converter produces high quality load current at high power factors, by utilizing its arm inductances as low pass filters. The initial value of cell capacitor of each arm are different; the two upper arm capacitors are set to 60V, while the two lower arm capacitors are set to 40kV. Figure 4-8c(ii) shows phase current and its associated upper and lower arm currents. Despite the phase current being sinusoidal and dc offset free, the arm currents contain dc offset proportional to the peak phase current, load power factor, and modulation index. Unlike the conventional voltage source converters with discontinuous arm current, the arm current of the modular converter is continuous as shown in Figure 4-8c(ii).



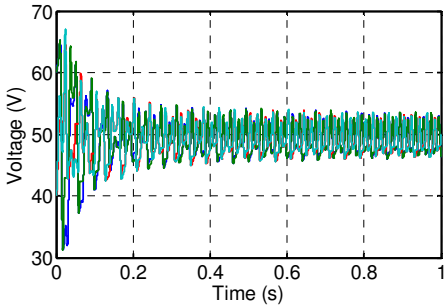
a) Phase voltage referred to supply mid-point.



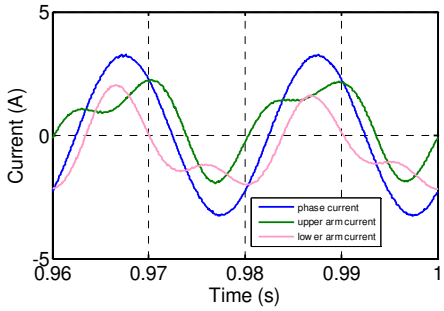
b) Line voltage.



(i)

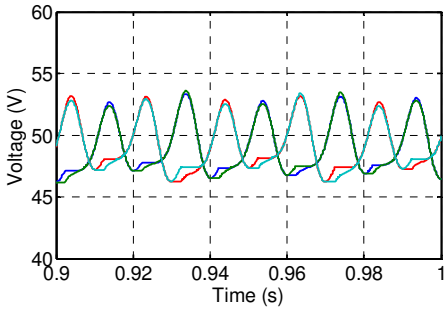


(i)



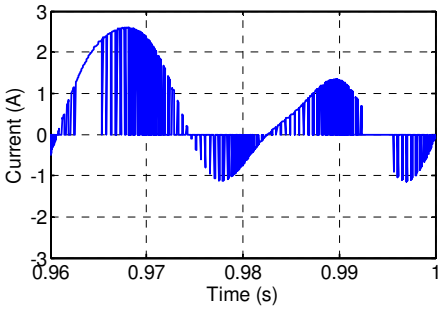
(ii)

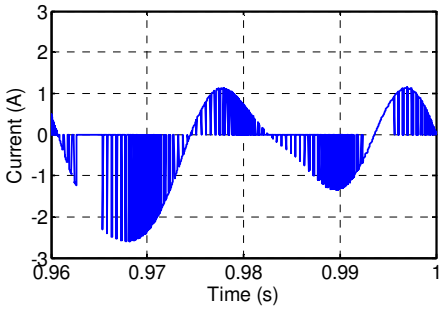
c) Three-phase current waveform and current in the upper and lower arm of phase a.



(ii)

d) Capacitor voltage of phase a and expanded version of (i).





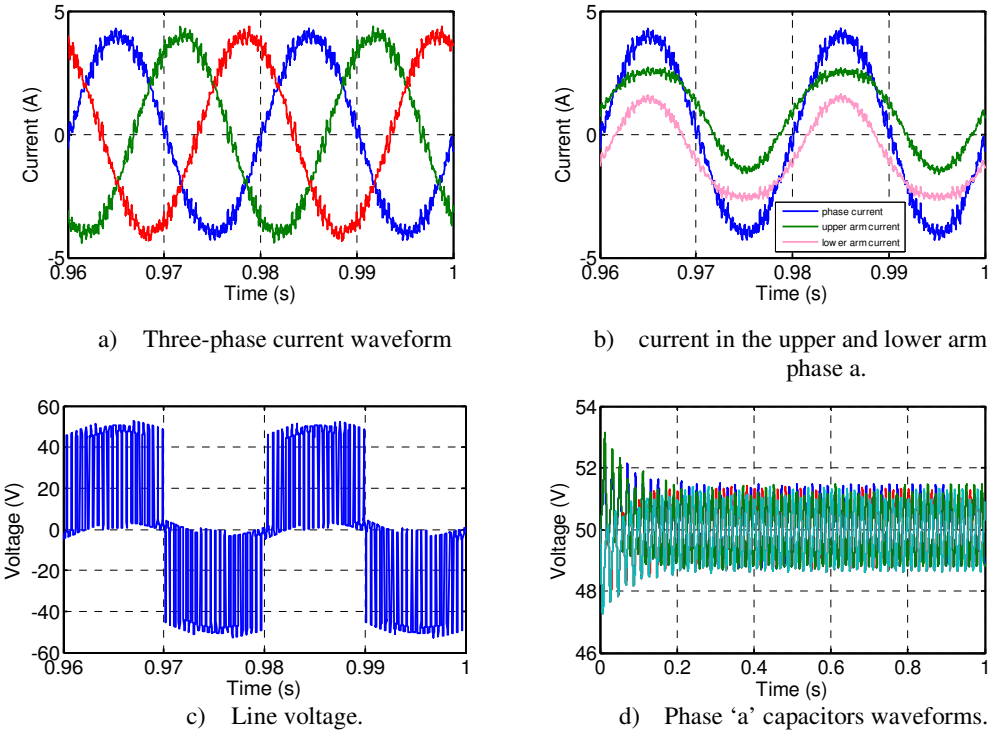
e) Current waveforms in the main and complementary switches in one cell.

Figure 4-8: Waveforms obtained when three-level modular converter is simulated at 0.9 modulation index and 0.72 power factor lagging.

This may eliminate the need for dc side filters in applications such as STATCOM or HVDC converters, as the emitted audible noise is extremely low (but this is true only with a large number of cells per arm).The results in Figure 4-8d show that the voltages across the cell capacitors of the three-level modular converter are maintained around the desire set-point after taking nearly 0.1 second to balance and reach ½Vdc. Figure 4-8 e shows the current waveforms of two complementary switches of one M2C cell. The switching frequency per device under this operating condition is less than half the carrier frequency and the equivalent switching frequency on the output phase voltage is the same as the carrier frequency. With an increased number of cells per arm, the switching frequency per device is expected to be reduced considerably.

Case II: Modulation index m=0.8, power factor=1

Figure 4-9 shows the results when the converter is operated at 0.8 modulation index and unity power factor.



a) Three-phase current waveform

b) current in the upper and lower arm of phase a.

c) Line voltage.

d) Phase 'a' capacitors waveforms.

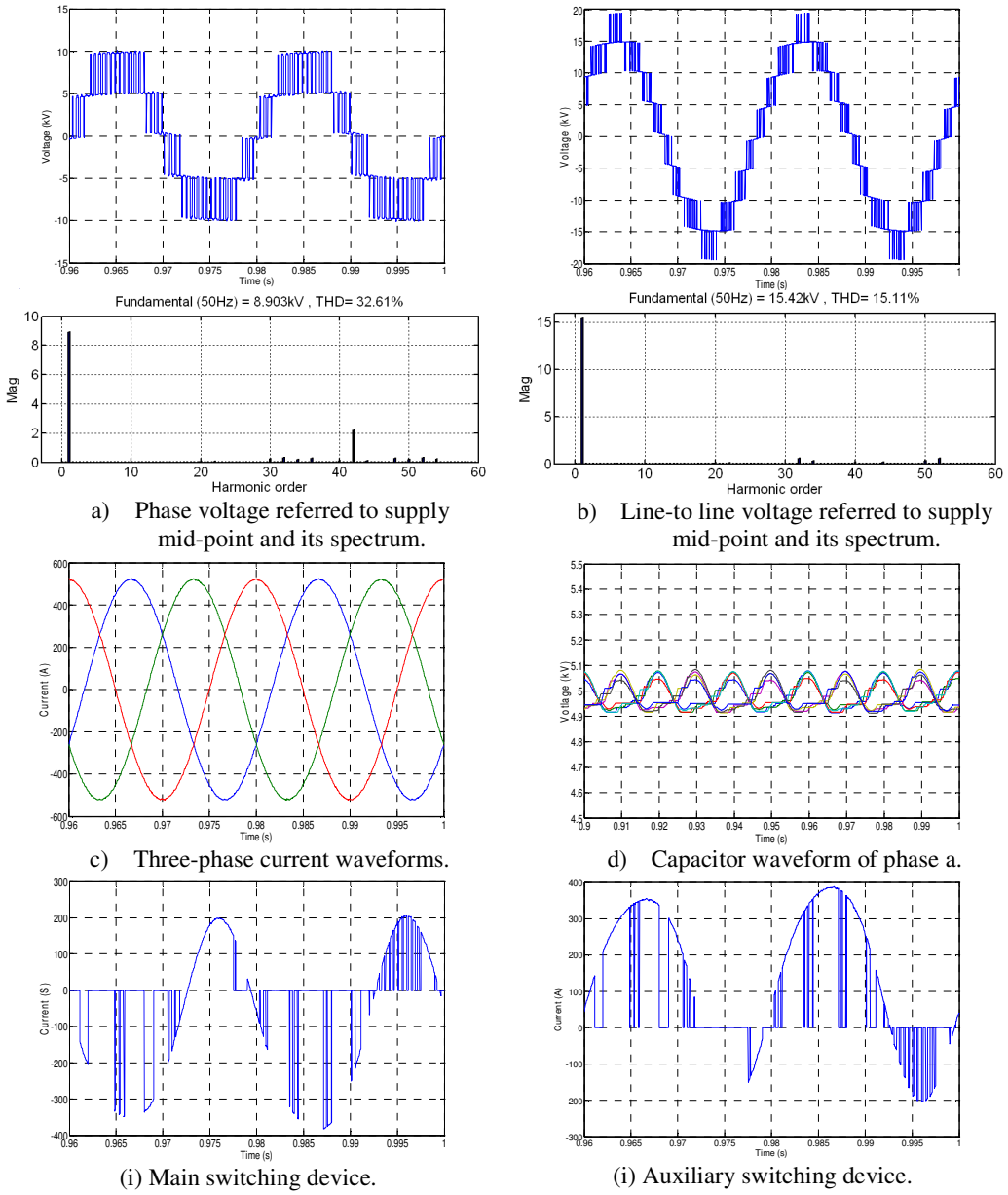
Figure 4-9: Waveforms obtained when three-level modular converter is simulated at 0.8 modulation index and unity power factor.

The converter is able to operate without any difficulties in terms of cell capacitor voltage balancing, and produces high quality current at high power factors. This

demonstrates the ability of the modular converter to operate over the full modulation index linear range independent of load power factor. Experimental results provide further validation in section 4.6.

4.5.2 Simulations for five-level M2C

Figure 4-10 shows the simulation results obtained when the five-level converter with 2200μF cell capacitors and 1mH arm inductance operated at 0.9 modulation index and 0.88 power factor lagging.



a) Phase voltage referred to supply mid-point and its spectrum.

b) Line-to line voltage referred to supply mid-point and its spectrum.

c) Three-phase current waveforms.

d) Capacitor waveform of phase a.

(i) Main switching device.

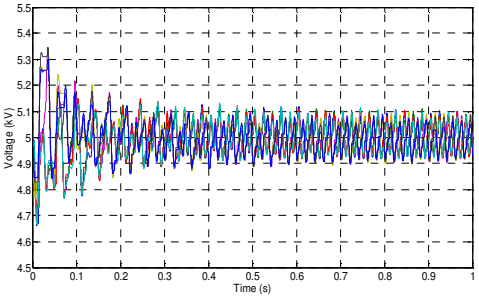
(i) Auxiliary switching device.

e) Current waveforms in the main and complementary switches in one cell.

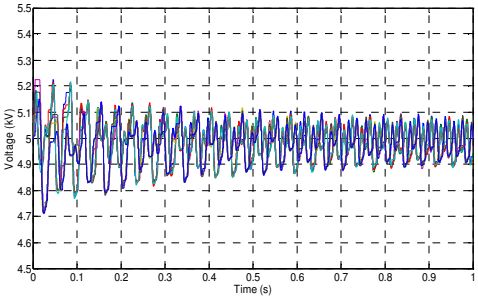
Figure 4-10: Waveforms obtained when five-level modular converter is simulated at 0.9 modulation index and 0.88 power factor lagging.

It can be observed that the line-to-line voltage total harmonic distortion and voltage stress on switching devices for the five-level converter is reduced to half of the three-level converter.

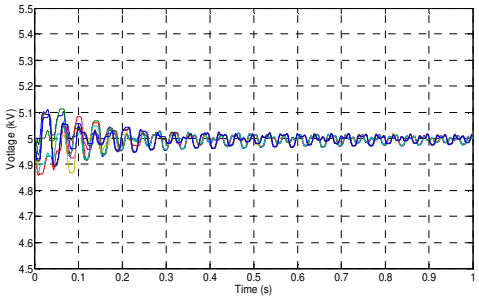
The effects of load power factor and modulation index on capacitor voltage balance of the five-level modular converter are evaluated. To show the effect of load power factor on capacitor voltage balance, a modulation index of m=0.9 with different load power factors is considered. In the case of zero power leading, a small value of inductance is included in the load circuit to attenuate the switching frequency component. The results (shown in Figure 4-11) demonstrate that capacitor voltage balance in a five-level M2C is not dependent on the load power factor.



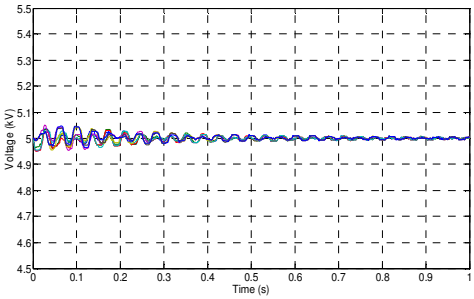
(i) Modulation index m=0.9 and unity power factor.



(ii) Modulation index m=0.9 and 0.8 power factor lagging.



(iii) Modulation index m=0.9 and zero power factor lagging.



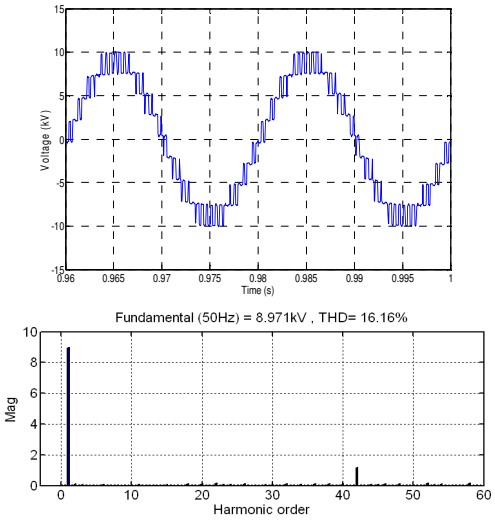
(iv) Modulation index m=0.9 and zero power factor leading.

Figure 4-11: Effect of power factor on voltage balance of cell capacitors.

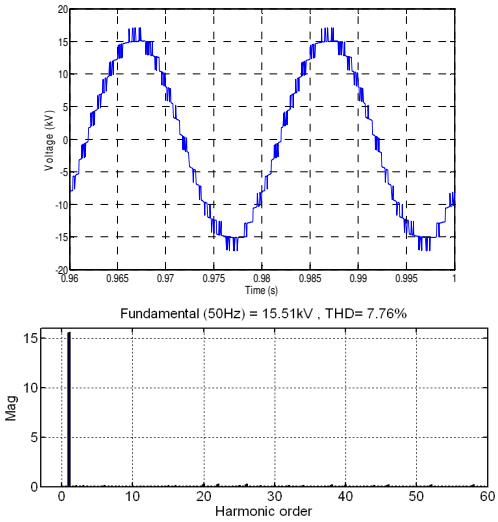
4.5.3 Simulations for nine-level M2C

Figure 4-12 shows the simulation results when the nine-level converter with 2200μF cell capacitors and 1mH arm inductance is operated at 0.9 modulation index and 0.88 power factor lagging. Observe that the line-to-line voltage total harmonic distortion and voltage stress on switching devices for the nine-level converter is reduced to half

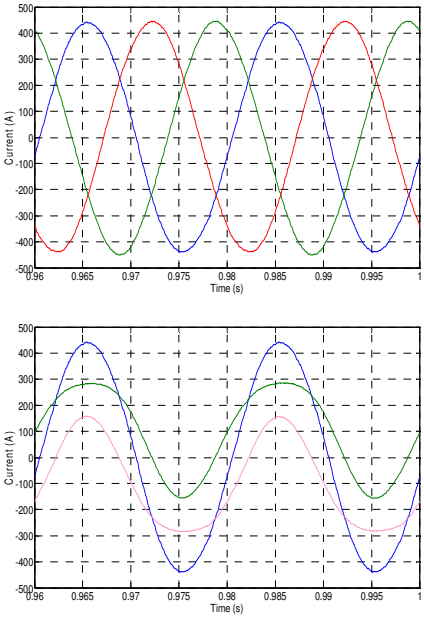
that of the five-level converter.



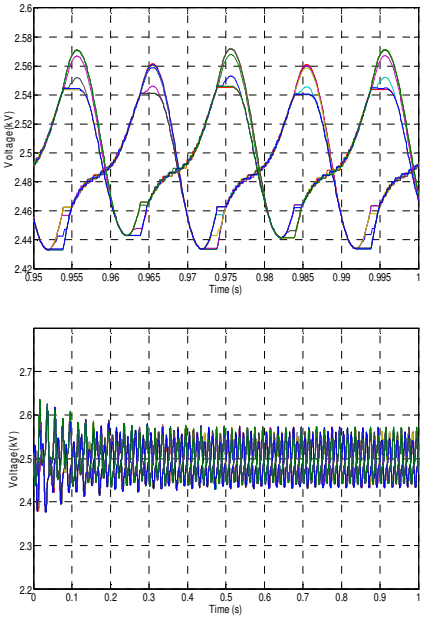
a) Phase voltage referred to supply mid-point and its spectrum.



b) Line-to line voltage referred to supply mid-point and its spectrum.



c) Three-phase current waveform and current in the upper and lower arm of phase a.

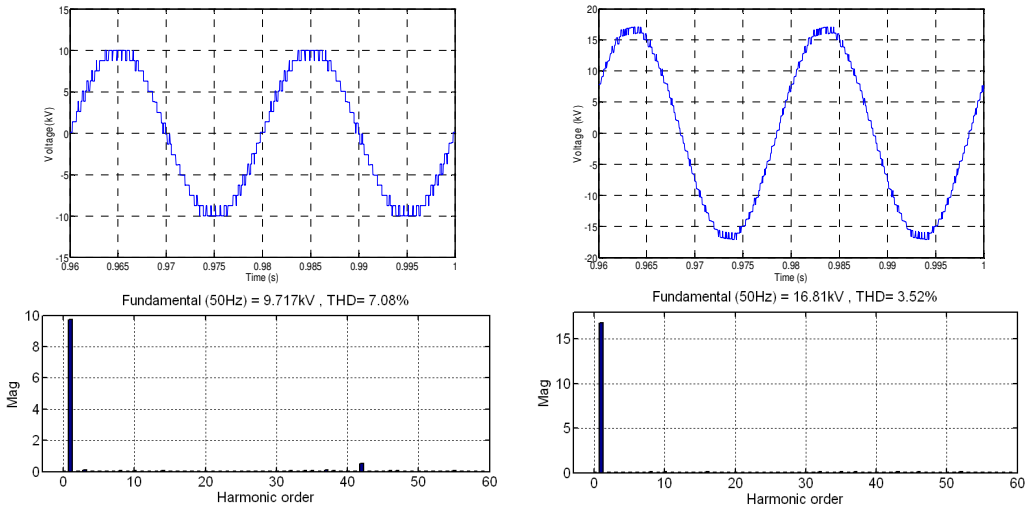


d) Capacitor voltage of phase a and expanded version of the capacitor voltage.

Figure 4-12: Waveforms obtained when nine-level modular converter is simulated at 0.9 modulation index and 0.88 power factor lagging.

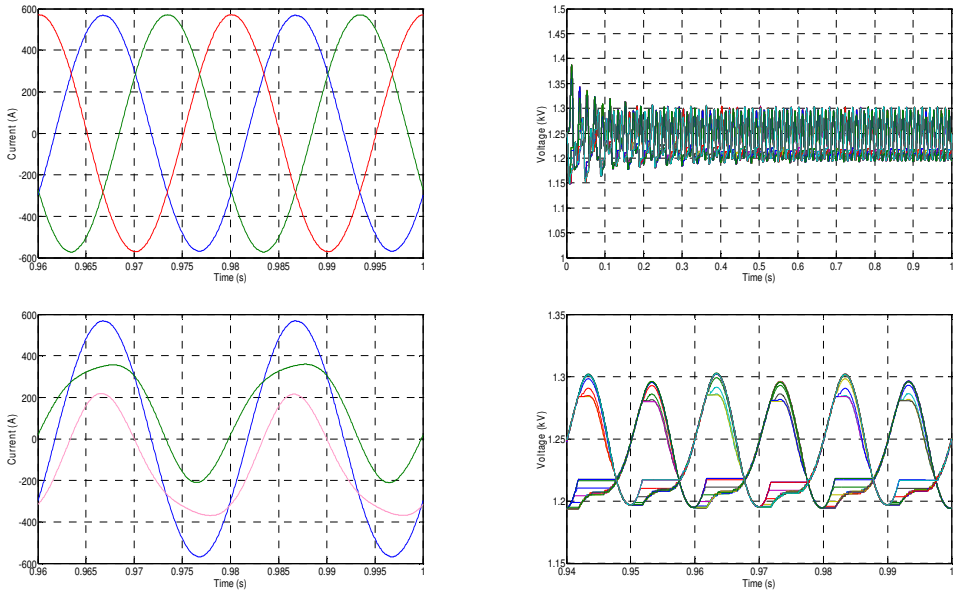
4.5.4 Simulations for seventeen-level M2C

Figure 4-13 shows the line-to-line voltage waveforms and their spectra for 17-level M2C, and the voltage across the 32 capacitors in one phase leg of the M2C. Phase voltage and line-to-line voltage waveforms in Figure 4-13a and Figure 4-13b.



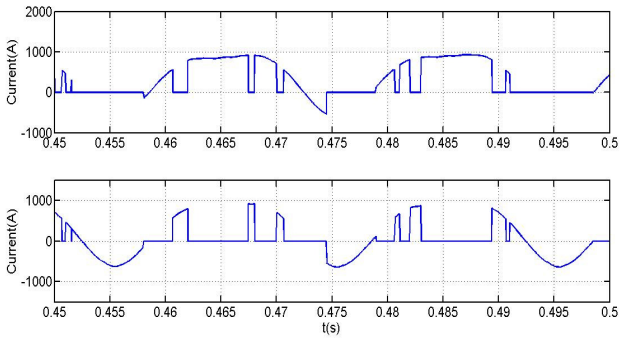
a) Phase voltage referred to supply mid-point and its spectrum.

b) Line-to line voltage referred to supply mid-point and its spectrum.



c) Three-phase current waveform and current in the upper and lower arm of phase a.

d) Capacitor voltage of phase a and expanded version of the capacitor voltage.



e) Current waveforms in the main and auxiliary switch of top cell of 17-level M2C.

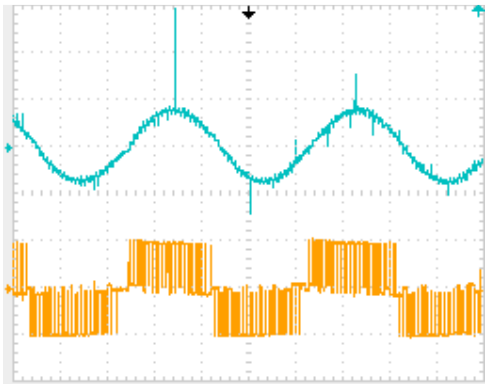
Figure 4-13: Waveforms obtained when seventeen-level modular converter is simulated at 1 modulation index and 0.88 power factor lagging.

Figure 4-13b show that the 17-level M2C produces an output voltage with the least harmonic distortion and lowest voltage stress on the switches compared to the three, five and nine level converters. The results in Figure 4-13c shows the arm current in the M2C, and current waveforms for the devices within one cell of the M2C (mainly, the current waveforms in the main and auxiliary devices). Note that the auxiliary device is the switch that connected in series with the cell capacitor. Figure 4-13c shows that the arm current of the M2C is continuous but contains a dc component. The existence of this dc component in the arm increases the conduction loss of the M2C compared to the losses of the two-level converter. This is despite a significant reduction in current stresses in the switching devices of the M2C. Based on Figure 4-13e, the effective switching frequency per device is only 200Hz in the M2C. This reflects in a significant reduction in M2C losses.

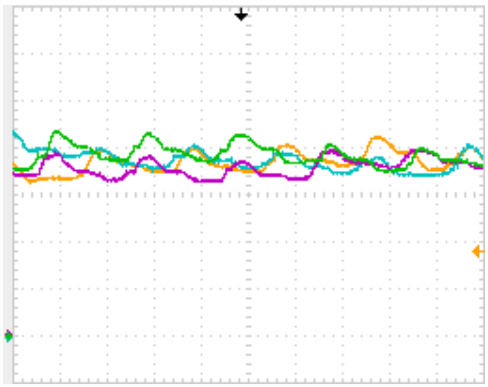
4.6 Experimental validation

This section provides experimental validation of the analysis and simulation results presented. The practical results are obtained from one phase-leg of a prototype three-level modular converter with a 100V dc link voltage, 1mF cell capacitors, and arm inductance of 3mH (see Appendix A.1). The converter is controlled using SPWM with a 2.1kHz switching frequency. An Infineon Technology Tri-core microcontroller TC 1796 is used to program the modulation and capacitor voltage balancing strategy. Figure 4-14 and Figure 4-15 show the experimental results obtained at 0.72 power factor lagging with modulation index m=0.9, and unity power factor with modulation index m=0.8 respectively. The converter operates successfully in both cases and cell capacitor voltage balancing is maintained. From the phase voltage and current waveforms in Figure 4-14a and Figure 4-14b, the modular converter with only two cells per arm produces high quality phase current, utilizing its upper and lower arm inductors as low-pass filters, as demonstrated in the simulations. From the current waveforms of devices S_a and S_m (Figure 4-14d and Figure 4-14e), these three-level modular switching devices operate at half the carrier frequency, as demonstrated in the simulation. This confirms the suitability of the modulation and capacitor voltage balancing method employed for high-voltage applications where the switching frequency per device and semiconductor losses are

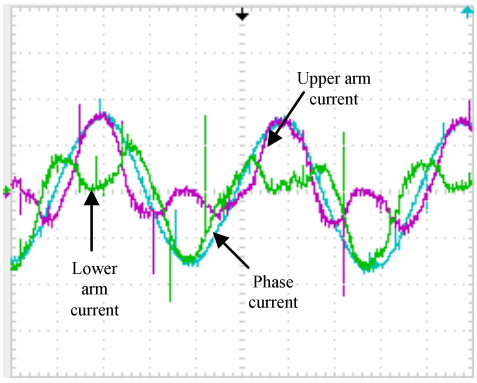
restrictive factors. Even though the upper and lower arm currents include a dc offset and distortion their sum remains sinusoidal and equal to the phase current [9, 19, 22-25].



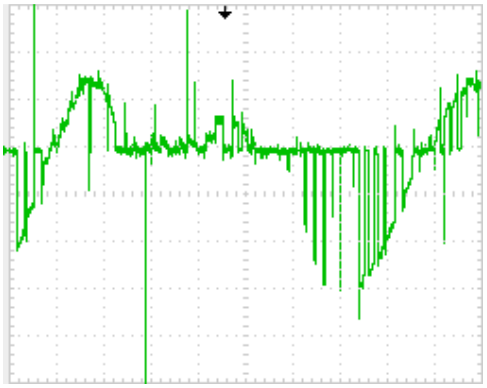
a) Load voltage and current
(scale: 5ms/div, 100v/div, 1A/div).



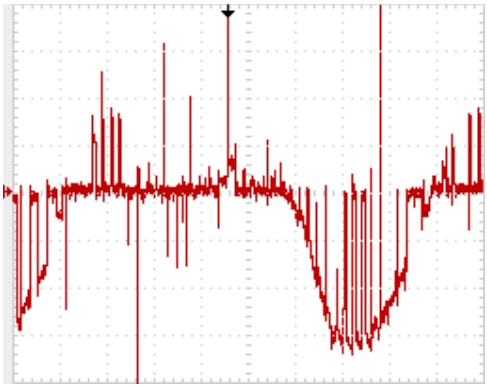
b) Voltage across four cell capacitors of the phase-leg
(scale: 10ms/div, 10v/div).



c) Current in the upper and lower arms of the phase leg
(scale: 5ms/div, 1A/div).

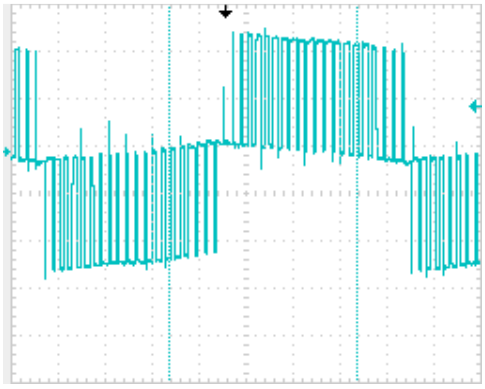


d) Current in one device (IGBT and diode) of a cell.
(scale: 2.5ms/div, 1A/div).

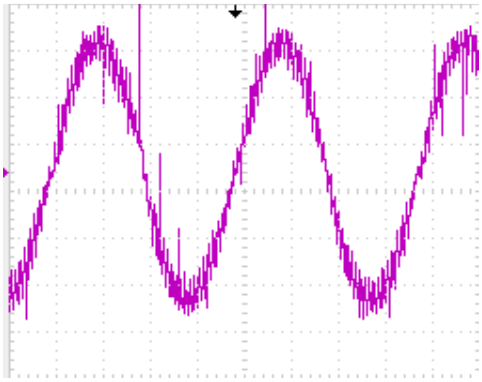


e) Current in the other device (IGBT and diode) of a cell.
(scale: 2.5ms/div, 1A/div).

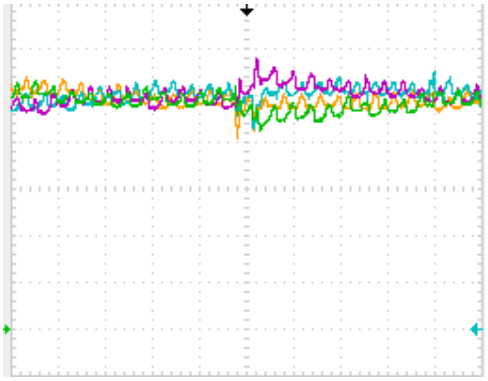
Figure 4-14: Experimental waveforms obtained from a one-phase 3-level modular multilevel converter experiment at 0.9 modulation index and 0.72 power factor lagging.



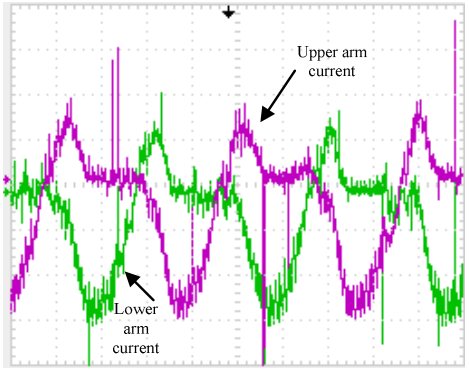
a) Load voltage
(scale: 5ms/div, 50v/div).



b) Load current
(scale: 5ms/div, 0.5Av/div).



c) Voltage across four cell capacitors of the phase-leg
(scale: 10ms/div, 10v/div).



d) Current in the upper and lower arms of the phase leg
(scale: 5ms/div, 0.5A/div).

Figure 4-15: Experimental waveforms obtained from one-phase 3-level modular multilevel converter experiment at 0.8 modulation index and unity power factor.

4.7 Summary

This chapter analyses the M2C operating principle, capacitor size and voltage ripple of the modular multilevel converter when SPWM modulated. It also experimentally validates the analysis provided and demonstrates the advantages of the modulation and capacitor balancing strategy. As the M2C is the only multilevel converter able to exploit the full potential of multilevel modulation, it has been selected as representative of multilevel converters in this investigation. The results of this investigation show that the M2C offers the following features: improved efficiency, lower voltage across and current through the switching devices, extremely low *dv/dt*

and audible noise resulting from small voltage steps, and low switching frequency per device. These results confirm the suitability of the multilevel converter, such as the M2C, for medium- and high-voltage applications, such as reactive power compensation, medium voltage drive systems, interfacing for renewable power plants using wind and solar energy, and high voltage dc transmission systems.

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CHAPTER 5

5 Hybrid Cascaded Multilevel Converter

5.1 Introduction

The use of power electronic converters in medium and high-voltage applications has increased significantly in the last decade. This increase is dominated by the use of these converters as interfacing units for renewable power generation and reactive power compensation at medium-voltage, and for high-voltage dc (HVDC) transmission systems [1-5]. Recently a new generation of viable voltage source multilevel converters have emerged, which includes the modular multilevel converter, H-bridge modular converters, and the alternative arm modular converter [3, 4, 6]. These converters can achieve improved efficiency and better power quality but have the disadvantage of increased complexity and converter footprint [5, 7, 8]. Some of these converters offer the feature of dc fault blocking capability, the ability to block the active power exchange between the ac and dc sides, and reactive power between converters and the ac side, hence there is no current flow in the converter switches during dc side faults [9, 10]. The H-bridge and the alternative arm modular multilevel converter, and the hybrid multilevel converter with H-bridge cells in the ac side offer the feature of dc fault reverse blocking capability.

Several versions of the hybrid multilevel converter with ac side cascaded H-bridge cells are discussed in [1, 11-18]. The basic concept involves the use of a two-level converter in the high-voltage stage in series with cascaded low-voltage H-bridge cells. These cells can be powered from isolated separate active dc sources or by means of floating capacitors. Variants employ isolated sources because both high and low voltage stages contribute to the fundamental voltage. However, this approach is unlikely to be practical for large cell numbers. There are two alternative operating modes. The first mode employs the series H-Bridge string to compensate for the low frequency harmonics generated by the high voltage two-level conversion stage. The

H-Bridge cells do not contribute to real power flow, eliminating the need for isolated power supplies. This approach offers a number of features [9].

- Low switching frequency of the principal two level inverter.
- No requirement for isolated dc sources.
- The H-Bridge capacitors are only subjected to harmonic power flow, resulting in reduced cell capacitance requirements.
- The series H-Bridge cells can be employed for reverse blocking of dc link faults from ac side currents.

The second mode is when using standard multilevel modulation, capacitor voltage balancing can be achieved using phase voltage redundant switch states. The two-level bridge and H-bridges operating as one unified unit with SPWM can extend the modulation index linear range and produce better output voltage and current waveform quality. This approach has advantages of:

- Minimized output voltage spikes when using different modulation strategies on the two-level bridge and the H-bridges.
- Extended modulation index linear range to 1.218 and 2 for real and reactive power applications, respectively.
- Reverse blocking dc link fault capability is retained.

5.2 Operating Principle

Figure 5-1 shows a single-phase hybrid multilevel converter with two H-bridge cells per phase. It generates seven or nine-level voltage waveforms at the output phase a_0 relative to supply mid-point 0. The two-level converter stage requires hard-switched self-commutated switching devices capable of supporting the full dc link voltage V_{dc}. For medium to high voltage applications, series connection will be required. The series H-bridge cells use low voltage rated IGBTs with a maximum voltage stress limited to the cell capacitor voltage. Proper operation of the converter in Figure 5-1 requires robust capacitor voltage balancing to ensure that the voltage across each cell capacitor does not exceed the switch device rating under all conditions.

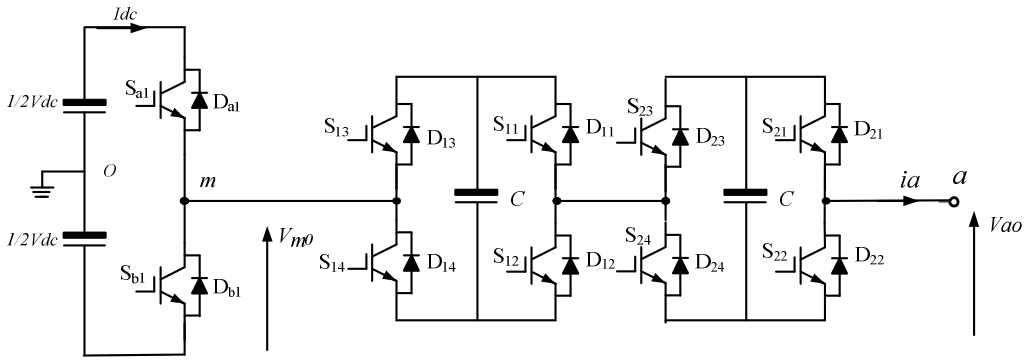


Figure 5-1: Hybrid multilevel converters with 2 H-bridge cells in ac side.

5.2.1 Independent control using SHE- PWM and high frequency PWM

Figure 5-2 shows a generalized version of a single-phase hybrid voltage source multilevel converter with *N* H-bridge cells per phase, which is capable of generating *4N+1* voltage levels at the output phase 'a_0' relative to the supply mid-point '0', where *N* is the number of H-bridge cells per phase. An H-bride cell generates three-level voltage waveforms, V_{dc}/N, 0 and $-V_{dc}/N$, at its terminals. The H-bridge cell's bi-polar capability allows the hybrid multilevel converter to correct or distribute any capacitor voltage imbalance that may occur during its operation independent of load power factor and modulation index. For a large number of H-bridge cells, the converter generates near pure sinusoidal voltage at the converter output, as depicted in Figure 5-2. Figure 5-2 shows voltage waveforms at the two-level converter output, 'a_m' referred to '0', across the H-bridge cells and output phase of the hybrid multilevel converter, 'a_0' referred to '0', assuming a large number of H-bridge cells. The converter in Figure 5-2 uses the two-level converter to synthesize the desire fundamental voltage component by switching between $+½V_{dc}$ and $-½V_{dc}$ using SHE-PWM. The H-bridge cells act as a series active power filter to attenuate the low order harmonics existing in the output phase voltage of the two-level converter stage and create a multilevel voltage waveform with voltage steps equal to the cell capacitor voltage. This will result in the maximum output fundamental voltage being $4/\pi = 1.27$ (corresponding to the two-level converter square-wave output voltage). This reduces voltage stress (low *dv/dt*) on the winding of the interfacing transformer or any other load connected at the converter ac side The distinct feature of the hybrid converter in Figure 5-2 is that the switches of the

two-level converter and H-bridge cells are operated at a relatively low switching frequency, resulting in low switching losses. Additionally, the converter provides dc blocking capability but has the potential for reducing cell capacitance relative to the M2C since the H-Bridge cells only compensate for the harmonics.

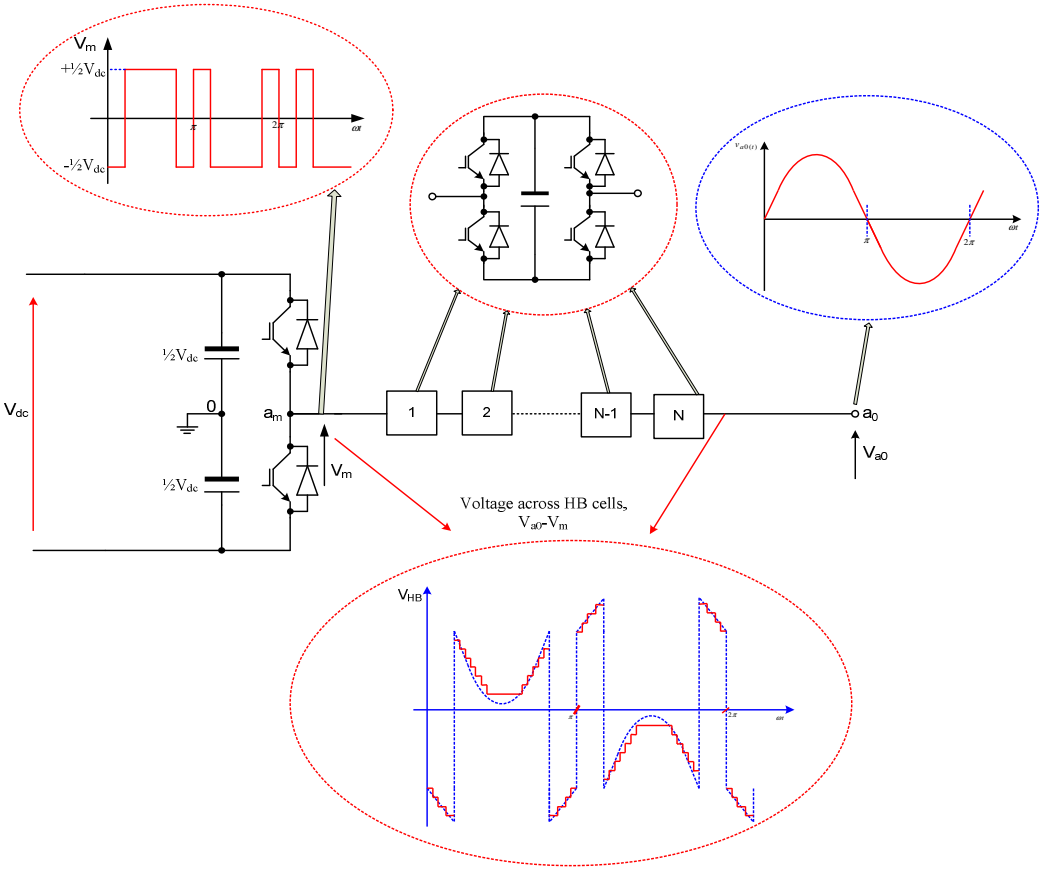


Figure 5-2: Hybrid multilevel converters generalized with *N* H-bridge cells per phase, *4N+1* voltage levels per phase.

5.2.2 SPWM with 3rd harmonic subtraction

Figure 5-3a shows a hybrid multilevel converter, HCMC, with two ac side H-bridge cells per phase. Each H-bridge cell blocks ¼V_{dc}, where V_{dc} is the total dc link voltage. Therefore, the number of H-bridge cells required must be selected such that when they are connected in series, they block ½V_{dc}. When these H-bridge cell capacitors are fully utilized, the hybrid converter in Figure 5-3a generates nine voltage levels per phase between 'a' and '0', as shown Figure 5-3b. Table 5-1 summarizes the switch states of the nine-level hybrid converter in Figure 5-3a, including the effect of phase current polarity on each cell capacitor state of charge. Noticed that capacitor

voltage imbalance is created when the converter generates voltage levels $\pm V_{dc}$, $\pm\frac{3}{4}V_{dc}$, $\pm\frac{1}{2}V_{dc}$, and $\pm\frac{1}{4}V_{dc}$. Nonetheless, at voltage levels $\pm\frac{1}{2}V_{dc}$ capacitor voltage imbalance can be avoided by using switch combinations (vi) and (xv) that bypass cell capacitors C_1 and C_2. When the converter generates a '0' voltage level, both cell capacitors can be charged or discharged either with positive or negative phase current, i_a. This indicates that capacitor voltage balancing of the HCMC in Figure 5-3a is achievable only when voltage imbalance is created when switching between different voltage levels, and can be compensated at the '0' voltage level. This may limit the maximum achievable modulation index. Voltage balance of the H-bridge floating capacitors is achieved by switching the appropriate capacitors according the switch states summarized in Table 5-1, taking into consideration the phase current polarity.

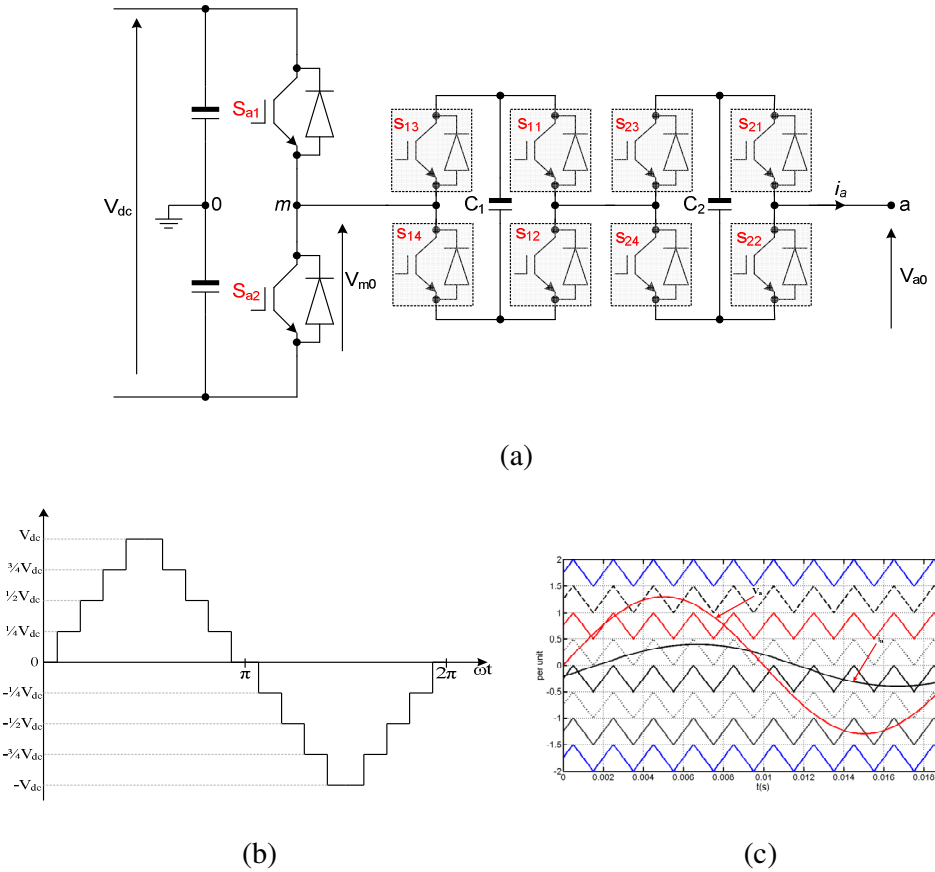


Figure 5-3: Hybrid multilevel converter:
(a) One-phase of a nine-level hybrid cascaded converter,
(b) Phase voltage at converter output 'a' relative to supply mid-point '0'
(c) normalized reference voltage, load current and carrier waveforms.

Table 5-1: Summary of the switch combinations of the nine-level hybrid converter with ac side cascaded H-bridge cells.

Voltage levels	Switch combinations	Effect of current polarity on capacitor voltage	
		$i_a>0$	$i_a<0$
V_{dc}	*i)* $½V_{dc}+V_{c1}+V_{c2}$	$C_1\downarrow C_2\downarrow$	$C_1\uparrow C_2\uparrow$
$¾V_{dc}$	*ii)* $½V_{dc}+V_{c1}$	$C_1\downarrow C_2\rightarrow$	$C_1\uparrow C_2\rightarrow$
	iii) $½V_{dc}+V_{c2}$	$C_1\rightarrow C_2\downarrow$	$C_1\rightarrow C_2\uparrow$
$½V_{dc}$	*iv)* $½V_{dc}+V_{c1}-V_{c2}$	$C_1\downarrow C_2\uparrow$	$C_1\uparrow C_2\downarrow$
	v) $½V_{dc}-V_{c1}+V_{c2}$	$C_1\uparrow C_2\downarrow$	$C_1\downarrow C_2\uparrow$
	vi) $½V_{dc}$	$C_1\rightarrow C_2\rightarrow$	$C_1\rightarrow C_2\rightarrow$
$¼V_{dc}$	*vii)* $½V_{dc}-V_{c1}$	$C_1\uparrow C_2\rightarrow$	$C_1\downarrow C_2\rightarrow$
	viii) $½V_{dc}-V_{c2}$	$C_1\rightarrow C_2\uparrow$	$C_1\rightarrow C_2\downarrow$
0	*ix)* $½V_{dc}-V_{c1}-V_{c2}$	$C_1\uparrow C_2\uparrow$	$C_1\downarrow C_2\downarrow$
	x) $-½V_{dc}+V_{c1}+V_{c2}$	$C_1\downarrow C_2\downarrow$	$C_1\uparrow C_2\uparrow$
$-¼V_{dc}$	*xi)* $-½V_{dc}+V_{c1}$	$C_1\downarrow C_2\rightarrow$	$C_1\uparrow C_2\rightarrow$
	xii) $-½V_{dc}+V_{c2}$	$C_1\rightarrow C_2\downarrow$	$C_1\rightarrow C_2\uparrow$
$-½V_{dc}$	*xiii)* $-½V_{dc}+V_{c1}-V_{c2}$	$C_1\downarrow C_2\uparrow$	$C_1\uparrow C_2\downarrow$
	xiv) $-½V_{dc}-V_{c1}+V_{c2}$	$C_1\uparrow C_2\downarrow$	$C_1\downarrow C_2\uparrow$
	xv) $-½V_{dc}$	$C_1\rightarrow C_2\rightarrow$	$C_1\rightarrow C_2\rightarrow$
$-¾V_{dc}$	*xvi)* $-½V_{dc}-V_{c1}$	$C_1\uparrow C_2\rightarrow$	$C_1\downarrow C_2\rightarrow$
	xvii) $-½V_{dc}-V_{c2}$	$C_1\rightarrow C_2\uparrow$	$C_1\rightarrow C_2\downarrow$
$-V_{dc}$	*xviii)* $-½V_{dc}-V_{c1}-V_{c2}$	$C_1\uparrow C_2\uparrow$	$C_1\downarrow C_2\downarrow$

Where: $\uparrow$ means the capacitor is charged, $\downarrow$ means the capacitor is discharged, and $\rightarrow$ means the capacitor state remains unchanged.

5.3 Pulse Width Modulation with Third Harmonic Subtraction

5.3.1 Independent control using SHE- PWM and high frequency PWM

Figure 5-4(i) a shows two-level, fundamental and third harmonic voltage waveforms normalized to $½V_{dc}$. Figure 5-4 (i) b shows a normalized reference voltage for the cascaded H-bridge cells, which is obtained by subtracting the two-level converter stage output voltage from the desire fundamental voltage component, both normalized by $½V_{dc}$. It can be observed that the normalized H-bridge reference voltage exceeds 1 per unit ($½V_{dc}$) at several points. This means more H-bridge cells are required to successfully synthesize the normalized voltage waveform in Figure 5-4b. In order to reduce number of H-bridge cells required to achieve minimum conversion losses and a small footprint, a normalized H-bridge reference signal must

be suppressed such that its positive and negative peaks must be between 1 and -1, as shown in Figure 5-4c. The waveform in Figure 5-4c can be achieved when a third harmonic component with appropriate peak value is injected into the normalized H-bridge reference signal in Figure 5-4b. From Figure 5-4b, it can be observed that the positive and negative peaks of the normalized H-bridge reference voltage occur at $\omega t = \alpha$ and its complementary angle ($\pi - \alpha, \pi + \alpha, 2\pi - \alpha$). It can be noticed that by subtracting third harmonic component with peak equal to that of fundamental voltage at $\omega t = \alpha$ from the normalized H-bridge reference voltage in Figure 5-4b, the H-bridge reference waveform in Figure 5-4c can be obtained. By equating the third harmonic component to the fundamental component at $\omega t = \alpha$, the following expression is obtained:

$$m_{3h} \sin 3\alpha = m \sin \alpha \tag{5.1}$$

From the Fourier series of the two-level converter output voltage in Figure 5-5(i) a, fundamental voltage can be related to modulation index and α as follow:

$$2\cos\alpha - 1 = m \tag{5.2}$$

From equations (5.1) and (5.2), the magnitude of the third harmonic injected component to achieve the compensating waveform in Figure 5-5(i) c is:

$$m_{3h} = m\frac{\sin\alpha}{\sin 3\alpha} = \frac{4}{\pi}\frac{1}{m+2} \tag{5.3}$$

where modulation index is normalized such that $0 \le m \le 1$.

Therefore optimal third harmonic injection that ensures the H-bridge normalized reference voltage is bounded between 1 and -1, over the full modulation index linear range is:

$$v_{3h} = m_{3h} \sin 3\omega t = \frac{4}{\pi}\frac{1}{m+2}\sin 3\omega t \tag{5.4}$$

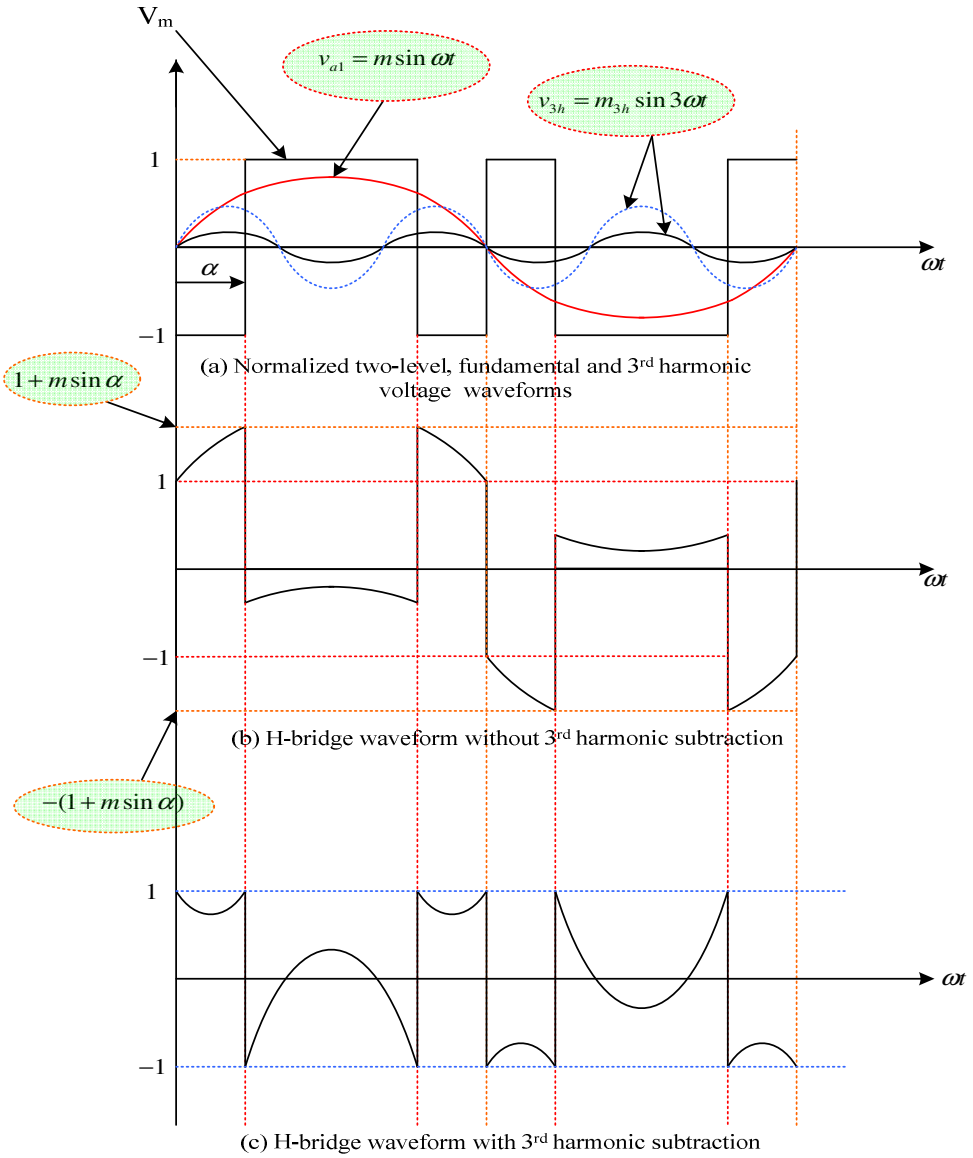
The Fourier coefficient for the voltage across the H-bridge normalized by ½Vdc prior to third harmonic injection is:

$$\begin{aligned} a_n &= 0 \\ b_n &= \frac{4}{\pi}\sum_{n=odd}^{\infty}\frac{1}{n}\left(1 - 2\cos n\alpha\right) \end{aligned} \tag{5.5}$$

Therefore, the third harmonic component in the H-bridge voltage, after subtraction of the third harmonic describes by equation (5.3) can be expressed as:

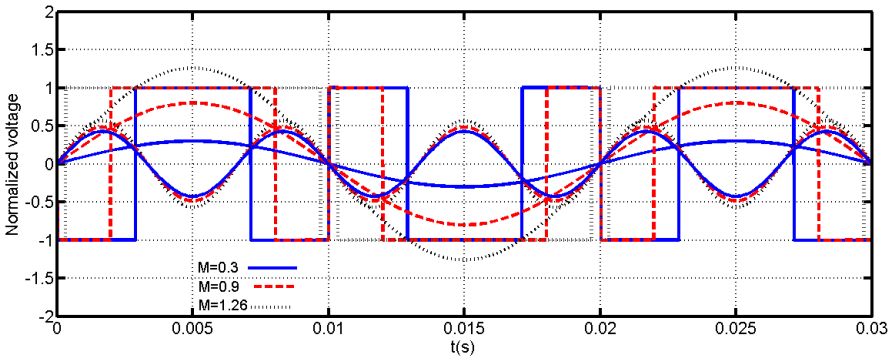
$$b_3^{'} = \frac{4}{\pi}\left[\frac{1}{3}(1-2\cos 3\alpha) - \frac{1}{m+2}\right] \tag{5.6}$$

From equation (5.6), the use of third harmonic subtraction according to equation (5.3), only cancels the extra third harmonic component that causes the positive and negative peaks of the H-bridge reference voltage to exceed 1 and -1, as demonstrated in Figure 5-5(ii) d and Figure 5-5(ii) e, without affecting the improvement that can be achieved in the dc link utilization by using SHE-PWM. Figure 5-5(ii) d and Figure 5-5(ii) e demonstrate the optimality of the presented third harmonic over the extended modulation index linear range and its ability to suppress the peaks of the H-bridge normalized reference voltage.

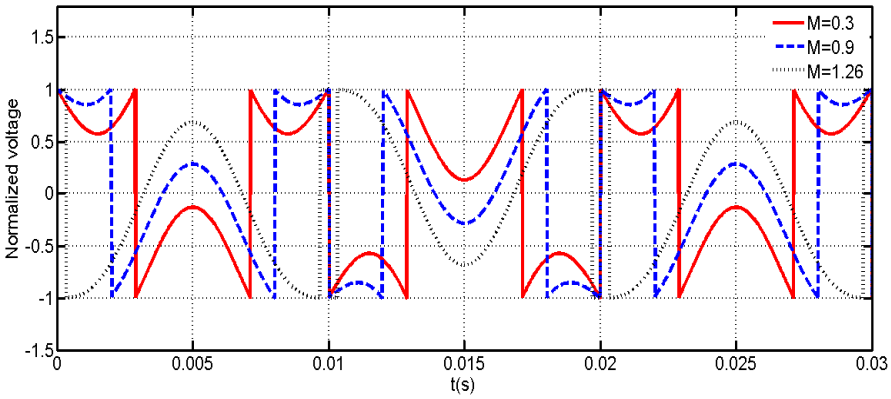


(i)

Figure 5-4: Waveforms describing the modulation strategy for the hybrid multilevel converter with cascaded H-bridges in the ac side.



(d) Waveforms show normalized two-level converter terminal voltage and its fundament component, and optimal third harmonic voltage required to suppress H-bridge reference voltage between 1 and -1 for different modulation indices.



(e) Normalized H-bridge reference voltage for different modulation indices after injection of optimal third harmonic voltage.

(ii)

Figure 5-5: Waveforms describing the modulation strategy for the hybrid multilevel converter with cascaded H-bridges in the ac side.

5.3.2 SPWM with 3rd harmonic subtraction

Based on Table 5-1, Figure 5-3b and Figure 5-3c the hybrid multilevel voltage source converter appears to have the ability to extend the modulation linear range up to 2 per unit or even higher, where the modulation index is defined as $m=V_1/\frac{1}{2}V_{dc}$. V_{dc} and V_1 represent the two-level converter dc link voltage and the peak phase fundamental voltage respectively. This is because the virtual dc link created by the H-cell floating capacitors of the hybrid multilevel converter in Figure 5-3a permits modulation of its output voltage between $\pm V_{dc}$ rather than $\pm\frac{1}{2}V_{dc}$ as in other voltage source converter topologies. Figure 5-3c shows normalized (by $\frac{1}{2}V_{dc}$) reference voltage and carrier waveforms, and load current with arbitrary phase angle φ. Assume the load current is $i_a = I_m \sin(\omega t - \varphi)$ and the normalized phase reference voltage is defined as $v_a = m\sin\omega t$. Also assume that the normalized reference

voltage crosses the lines that represent the normalized voltage levels 0.5pu ($¼V_{dc}$), 1pu ($½V_{dc}$) and 1.5pu ($¾V_{dc}$), separate the contiguous bands at α_1, α_2 and α_3 respectively. The angles α_1, α_2 and α_3 can be defined as: $\alpha_1 = \sin^{-1} 1/2m$, $\alpha_2 = \sin^{-1} 1/m$ and $\alpha_3 = \sin^{-1} 3/2m$. Based on observation of operation analysis in Section 5.2.2 and Table 5-1, the maximum modulation index limit where the capacitor voltage balancing of the hybrid cascaded multilevel can be attained, will be established based on charge balance. This implies that the charge imbalance created when the converter output phase is connected to voltage levels V_{dc}, $¾V_{dc}$, $½V_{dc}$ and $¼V_{dc}$ must be compensated at the '0' voltage level. For the hybrid converter in Figure 5-3a, this observation can be expressed mathematically by:

$$\begin{aligned} &|Q(0)| + |Q(\tfrac{3}{4}V_{dc})| \geq |Q(\tfrac{1}{4}V_{dc})| \\ &\text{or} \\ &|Q(0)| + |Q(\tfrac{1}{4}V_{dc})| \geq |Q(\tfrac{3}{4}V_{dc})| \end{aligned} \qquad (5.7)$$

where $Q(0)$, $Q(¼V_{dc})$ and $Q(¾V_{dc})$ represent the net charge exchange of the cell capacitors at *'0'*, $¼V_{dc}$ and $¾V_{dc}$ as ac line currents flow. Table 5-2 summarizes the normalized times at each voltage level during the transition of the normalized reference voltage within the first half cycle between different contiguous bands.

Table 5-2: Summary of normalized times spent (duty cycles) at each voltage level during converter operation in first half cycle of the reference voltage.

Voltage level	Reference voltage location	Duty cycle
0	$0 \leq v_{ref} < \frac{1}{2}$	$1 - d_4 = 1 - 2 \cdot m \sin \omega t$
$\frac{1}{4}V_{dc}$	$0 \leq v_{ref} < \frac{1}{2}$	$d_4 = 2 \cdot m \sin \omega t$
	$\frac{1}{2} \leq v_{ref} < 1$	$1 - d_3 = 2 - 2 \cdot m \sin \omega t$
$\frac{1}{2}V_{dc}$	$\frac{1}{2} \leq v_{ref} < 1$	$d_3 = 2 \cdot m \sin \omega t - 1$
	$1 \leq v_{ref} < \frac{3}{4}$	$1 - d_2 = 3 - 2 \cdot m \sin \omega t$
$\frac{3}{4}V_{dc}$	$1 \leq v_{ref} < \frac{3}{4}$	$d_2 = 2 \cdot m \sin \omega - 2$
	$\frac{3}{4} \leq v_{ref} < 2$	$1 - d_1 = 4 - 2 \cdot m \sin \omega t$
V_{dc}	$\frac{3}{4} \leq v_{ref} < 2$	$d_1 = 2 \cdot m \sin \omega - 3$

Assuming the modulation index is in the range $1<m\leq1.5$ (modulation range of

interest in most high-voltage applications), the net charge that the H-bridge floating capacitors can exchange when the converter output phase is attached at voltage levels *0*, *¼V_{dc}* and *¾V_{dc}* is expressed by equation (5.8), (5.9) and (5.10):

$$\begin{aligned} Q(0) &= \left[\int_0^{\varphi/\omega} -i_a(1-d_4)d + \int_0^{\alpha_1/\omega} i_a(1-d_4)dt + \int_{(\pi-\alpha_1)/\omega}^{\pi/\omega} i_a(1-d_4)dt \right] \\ &= -\tfrac{1}{2}\frac{I_m}{\omega}\left[\begin{array}{l} -4+4m\sin\varphi-4m\varphi\cos\varphi+ \\ \dfrac{\sqrt{4m^2-1}}{m}\cos\varphi+4m\cos\varphi\sin^{-1}\dfrac{1}{2m} \end{array} \right] \end{aligned} \tag{5.8}$$

$$Q(\tfrac{1}{4}V_{dc}) = \int_0^{\alpha1/\omega} i_a d_4 dt + \int_{\alpha_1/\omega}^{\alpha_2/\omega} i_a(1-d_3)dt + \int_{(\pi-\alpha2)/\omega}^{(\pi-\alpha1)/\omega} i_a(1-d_3)dt + \int_{(\pi-\alpha1)/\omega}^{\pi/\omega} i_a d_4 dt \tag{5.9}$$

$$= \frac{I_m\cos\varphi}{\omega}\left[4m\sin^{-1}\frac{1}{2m} + \frac{\sqrt{4m^2-1}}{m} - 2\frac{\sqrt{m^2-1}}{m} - 2m\sin^{-1}\frac{1}{m} \right]$$

$$Q(\tfrac{3}{4}V_{dc}) = \int_{\frac{\alpha_2}{\omega}}^{(\pi-\alpha_2)/\omega} i_a d_2 dt = \frac{I_m\cos\varphi}{\omega}\left[-2\frac{\sqrt{m^2-1}}{m} - 2m\sin^{-1}\frac{1}{m} + m\pi \right] \tag{5.10}$$

Substituting equations (5.8), (5.9) and (5.10) into inequality (5.7), gives the following nonlinear transcendental equation:

$$4+4m\varphi\cos\varphi-4m\sin\varphi-3\frac{\sqrt{4m^2-1}}{m}\cos\varphi-12m\cos\varphi sin^{-1}\frac{1}{2m}+2m\pi\cos\varphi\le 0 \tag{5.11}$$

Equation (5.11) shows that hybrid multilevel converter capacitor voltage balancing using multilevel sinusoidal pulse width modulation is power factor and modulation index dependent when $1<m\le 1.5$. When the converter is operated at zero power factor lagging or leading (*φ=½π*, *cosφ=0* and *sinφ=1*), the inequality (5.11) diminishes for all modulation indices *m≥1*. This indicates that the modulation index linear range can be extended up to 2 per unit. When the power factor is increased to unity, inequality (5.11) reduces to:

$$4-3\frac{\sqrt{4m^2-1}}{m}-12m\,sin^{-1}\frac{1}{2m}+2m\pi\le 0 \tag{5.12}$$

Solution of inequality (5.12) shows that the maximum achievable modulation index is *m*≤1.218. Above this limit capacitor voltage balancing becomes load power factor dependent. This is because the regions around the '0' voltage level where the

H-bridge floating capacitors can be balanced becomes narrow, and the net charge Q(0) may not be sufficient to correct the voltage imbalance created at voltage levels ¼V_{dc} and ¾V_{dc} because $\left|Q(\frac{3}{4}V_{dc})\right| - \left|Q(\frac{1}{4}V_{dc})\right| >> |Q(0)|$ as demonstrated in Figure 5-6a.

When ½<m≤1, Q(¾V_{dc})=0 and equation (5.8) remains valid for charge exchange at the '0' voltage level. However, the net charge exchange at voltage level ¼V_{dc} must to be recalculated as follow:

$$Q\left(\tfrac{1}{4}V_{dc}\right) = \frac{I_m cos\varphi}{\omega}\left(4msin^{-1}\frac{1}{2m} + \frac{\sqrt{4m^2-1}}{m} - m\pi\right) \tag{5.13}$$

When the modulation index is ½<m≤1, the range is $|Q(\tfrac{1}{4}V_{dc})| >> |Q(0)|$. This indicates voltage balance of the H-bridge cell floating capacitors is highly dependent on load power factor. These capacitors over-charge as the load power factor approaches unity.

For modulation indices 0<m≤½, Q(¾V_{dc})=0 and the net charge the H-bridge floating capacitors exchange at voltage levels 0 and ¼V_{dc} is recalculated as:

$$Q(0) = \frac{1}{\omega} I_m cos\varphi(m\pi - 2) \tag{5.14}$$

$$Q(\tfrac{1}{4}V_{dc}) = \frac{1}{\omega}\pi m I_m cos\varphi \tag{5.15}$$

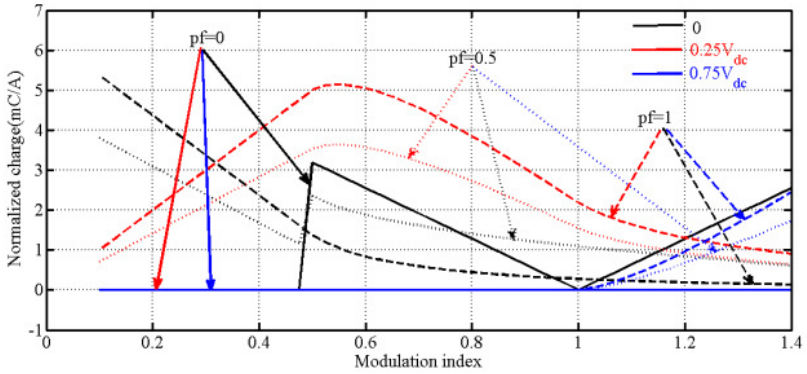
Based on equations (5.14) and (5.15), and Figure 5-6a capacitor voltage balancing remains power factor dependent as modulation index decreases until $m = 1/\pi \approx 0.31$. This is because $\left|Q(\tfrac{1}{4}V_{dc})\right| >> Q(0), \forall m, 0.31 < m \le \tfrac{1}{2}$. Below this range, capacitor voltage balancing is attainable independent of load power factor as $\left|Q(0)\right| \ge Q(\tfrac{1}{4}V_{dc})$ as indicated in Figure 5-6a.

The plots for the net charges versus modulation index at voltage levels 0, ¼Vdc and ¾Vdc in Figure 5-6a, are obtained with power factors of unity, 0.5 lagging and 0. Based on Figure 5-6a and the previous analysis, the dependency of capacitor voltage balancing in the hybrid cascaded multilevel converter on modulation index and load power factor becomes severe for modulation indices 0.4≤m<1. This is because the net charge for balancing action at the '0' voltage level may not be sufficient to maintain voltage balance of the H-bridge floating capacitors as depicted in Figure

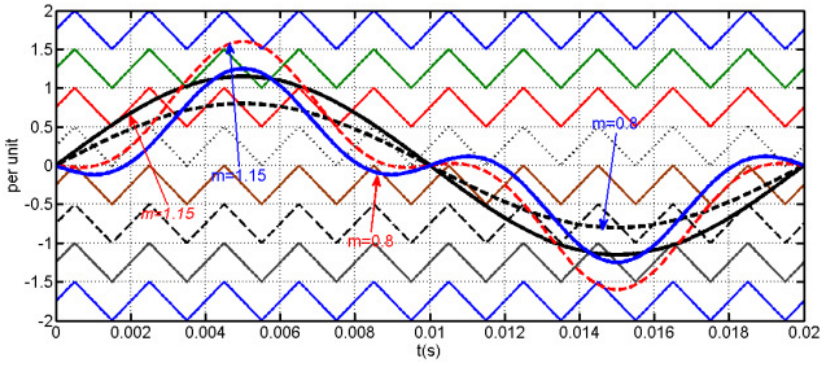
5-6a. Such dependency on load power factor and modulation index can be avoided by extending the regions where a zero voltage level can be produced and capacitor voltage balancing action is performed using necessary redundant switch combinations as shown in Figure 5-6b. This can be achieved by modifying the normalized reference voltage as follow:

$$v_a(t) = m\sin\omega t - \frac{\sqrt{2}}{\pi}\sin 3\omega t$$

Figure 5-6b shows the normalized reference voltages before and after modification, with 0.8 and 1.15 modulation indices. The regions where capacitor voltage balancing can be achieved are expanded considerably. This can be further illustrated by considering the angles where both references cross the 0.5pu line in Figure 5-6.



(a)



(b)

Figure 5-6: (a) Net charges H-bridge floating capacitors exchange at voltage levels 0, ¼V_{dc} and ¾V_{dc}, and (b) Waveforms illustrate extension of the regions where '0' voltage level can be generated.

Table 5-3 summarizes the angles for sinusoidal and sinusoidal plus third harmonic injection references at 0.8 and 1.15 modulation indices. Third harmonic injection extends the capacitor balancing region in the first quarter of the fundamental cycle

for 0.8 and 1.15 modulation indices by 15° and 16.4° respectively. This increases the net charge that can be manipulated in order to ensure voltage balance of the H-bridge cell capacitors, independent of load power factor, see Table 5-3. Also the modified reference voltage crosses the '0' voltage level within the first quarter at $\beta = \sin^{-1}\frac{1}{2}\left(3-\frac{m\pi}{\sqrt{2}}\right)^{\frac{1}{2}}$, allowing manipulation of the charge at the '0' voltage using switch combinations (ix) and (x) in Table 5-1, without significantly increasing the switching frequency of the H-bridges or switching of more than one voltage level at the converter output voltage. Therefore it can be concluded that the use of third harmonic injection with the HCMC may be necessary for capacitor voltage balancing over the extended range of modulation indices and power factors as demonstrated in Figure 5-6 and Table 5-3.

Table 5-3: Summary of the angles where sinusoidal and modified reference voltage crosses the boundary line 0.5 that represents the boundary between 0 and ¼Vdc, where net resultant charge range that can be extended.

Reference voltage	α_1 at m=0.8	α_1 at m =1.15
Sinusoidal	38.7°	25.8°
Sinusoidal plus 3rd harmonic	53.7°	45.2°
	Q(0) at m=0.8	Q(0) at m=1.15
SPWM	$0.45\times10^{-3}I_m$	$0.21\times10^{-3}I_m$
SPWM plus 3rd harmonic	$2.15\times10^{-3}I_m$	$1.53\times10^{-3}I_m$

5.4 Capacitor voltage ripple and power flow analysis

5.4.1 Capacitor voltage ripple

Since the hybrid converter in Figure 5-1 changes its state several times during one fundamental period, switching function represents a suitable tool to describe its ac and dc side dynamics. The voltage at the terminals of the two-level converter stage (Figure 5-1) referred to imaginary supply mid-point can be expressed as:

$$V_{am}(t) = \tfrac{1}{2}V_{dc}(2S_{a1}(t)-1) \qquad (5.16)$$

Where S_{a1} represent state of the two-level converter upper switch, '1' denotes on-state

and '0' the off-state.

Total voltage across the cascaded H-bridge cells in Figure 5-1 can be expressed by:

$$V_{HB}(t) = \sum_{j=1}^{N} (S_{j1}(t) - S_{j3}(t)) V_{cj} \tag{5.17}$$

Where N represent number of cascaded H-bridge cells, and S_{j1} and S_{j3} represent the two upper switches of cell j.

Differential equation describing dc side dynamics of each H-bridge cell can be written as:

$$\frac{d}{dt} V_{cj} = (S_{j1}(t) - S_{j3}(t)) \, i_a / C_j \tag{5.18}$$

Where j varies from 1 to N.

For a single-phase hybrid multilevel converter with ac side cascaded H-bridge cells, ac dynamics can be described as:

$$\frac{d}{dt} i_a = (V_{a0}(t) - R i_a(t)) / L \tag{5.19}$$

Where i_a, R, L represent phase current, resistance and inductance respectively.

A switching function can be used to represent converter steady-state and dynamic performance with greater detail. In order to derive approximate mathematical expressions that can be used to understand the dynamics of the HCMC, equations (5.17) and (5.18) must be replaced by their equivalents using averaging over the switching period, assuming equal probability for selection of the switch states that produce the same voltage levels.

Therefore, equation (5.17), which describes the voltage across the cascaded H-bridge cells, can be replaced by (refer to Figure 5-5):

$$V_{HB}(t) = \begin{cases} \frac{1}{2} V_{dc} (m \sin \omega t + 1 - m_{3h} \sin 3\omega t) & 0 \le \omega t < \alpha, \pi - \alpha \le \omega t < \pi, \pi + \alpha \le \omega t < 2\pi - \alpha \\ \frac{1}{2} V_{dc} (m \sin \omega t - 1 - m_{3h} \sin 3\omega t) & \alpha \le \omega t < \pi - \alpha, \pi \le \omega t < \pi + \alpha, 2\pi - \alpha \le \omega t < 2\pi \end{cases} \tag{5.20}$$

The differential equation (5.18) that describes H-bridge cell dc dynamics in the seven-level hybrid multilevel converter in Figure 5-1is:

$$\frac{d}{dt}V_{cj}=\begin{cases}\left(d_1+\frac{1}{2}d_2\right)\frac{i_a}{C_j} & 0\le\omega t<\alpha,\pi-\alpha\le\omega t<\pi\\ \left(d_1+\frac{1}{2}d_2\right)\frac{i_a}{C_j},(V_{HB}(t)\ge 0.5) & \\ \frac{1}{2}d_2\frac{i_a}{C_j},(0.5>V_{HB}(t)\ge 0) & \\ \frac{1}{2}d_3\frac{i_a}{C_j},(0>V_{HB}(t)\ge -0.5) & \alpha\le\omega t<\pi-\alpha,\pi+\alpha\le\omega t<2\pi-\alpha\\ \left(d_4+\frac{1}{2}d_3\right)\frac{i_a}{C_j},(V_{HB}(t)<-0.5) & \\ \left(d_4+\frac{1}{2}d_3\right)\frac{i_a}{C_j} & \pi\le\omega t<\pi+\alpha,2\pi-\alpha\le\omega t<2\pi\end{cases} \quad (5.21)$$

Where $j=1,\ 2,\ d_1=2\bar{V}_{HB}-1$, $d_2=2\bar{V}_{HB}$, $d_3=2\bar{V}_{HB}+1$ and $d_4=2(\bar{V}_{HB}+1)$, and $\bar{V}_{HB}$ represents the H-bridge voltage in equation (5.19) normalized by ½V_{dc}.

Equations (5.16), (5.19), (5.20), and (5.21) represent an average model that describes the behaviour of the hybrid multilevel VSC with two ac side cascaded H-bridge cells.

Expressions for the H-bridge cell capacitor voltage over a full fundamental period are obtained by solving equation (5.21), assuming steady-state phase current of the form $i_a(t)=I_m\sin(\omega t-\varphi)+I_{m3h}\sin(3\omega t-\varphi_3)$. This assumption is valid for the single-phase case only. In the three-phase case, $I_{m3h}=0$, due to cancelation of the third harmonic voltage component in the line voltage. Hence phase current become purely sinusoidal.

$0\le\omega t<\alpha,\pi-\alpha\le\omega t<\pi$

$$V_c(t)=\left\{\frac{1}{24\omega C}\begin{bmatrix}36\left(m\,\mathrm{I_m}\cos\varphi 1-m_{3h}I_{m3h}\cos\varphi_3\right)\omega t-18m\left(\mathrm{I_m}\sin(2\omega t-\varphi_1)-I_{m3h}\sin(\omega t-\varphi_3)\right)\\ -18m_{3h}\,\mathrm{I_m}\sin(2\omega t+\varphi_1)+9\left(m_{3h}\,\mathrm{I_m}\sin(4\omega t-\varphi_1)-mI_{m3h}\sin(4\omega t-\varphi_3)\right)\\ -16\left(3I_m\cos(\omega t-\varphi_1)+I_{m3h}\cos(3\omega t-\varphi_3)\right)+6m_{3h}I_{m3h}\sin(6\omega t-\varphi_3)\end{bmatrix}\right\}+K_0 \quad (5.22)$$

$\alpha\le\omega t<\pi-\alpha,\ \frac{1}{2}<m\le 1$

$$V_c(t)=\left\{\frac{1}{24\omega C}\begin{bmatrix}12\left(m\,\mathrm{I_m}\cos\varphi 1-m_{3h}I_{m3h}\cos\varphi_3\right)\omega t-6m\left(\mathrm{I_m}\sin(2\omega t-\varphi_1)-I_{m3h}\sin(\omega t-\varphi_3)\right)\\ +3\left(3m_{3h}\,\mathrm{I_m}\sin(4\omega t-\varphi_1)-mI_{m3h}\sin(4\omega t-\varphi_3)\right)\\ -12\left(3I_m\cos(\omega t-\varphi_1)+I_{m3h}\cos(3\omega t-\varphi_3)\right)+2m_{3h}I_{m3h}\sin(6\omega t-\varphi_3)\end{bmatrix}\right\}+K_1 \quad (5.23)$$

$$\pi \le \omega t < \pi + \alpha, 2\pi - \alpha \le \omega t < 2\pi$$

$$V_c(t) = \left\{ \frac{1}{24\omega C} \begin{bmatrix} 36\left(m\,\mathrm{I_m}\cos\varphi 1 - m_{3h} I_{m3h}\cos\varphi_3\right)\omega t - 18m\left(\mathrm{I_m}\sin(2\omega t - \varphi_1) - I_{m3h}\sin(\omega t - \varphi_3)\right) \\ +9\left(m_{3h}\,\mathrm{I_m}\sin(4\omega t - \varphi_1\right) - mI_{m3h}\sin(4\omega t - \varphi_3) \\ -44\left(3I_m\cos(\omega t - \varphi_1) + I_{m3h}\cos(3\omega t - \varphi_3)\right) + 6m_{3h} I_{m3h}\sin(6\omega t - \varphi_3) \end{bmatrix} + K_2 \right. \quad (5.24)$$

$$\pi + \alpha \le \omega t < 2\pi - \alpha, \tfrac{1}{2} < m \le 1$$

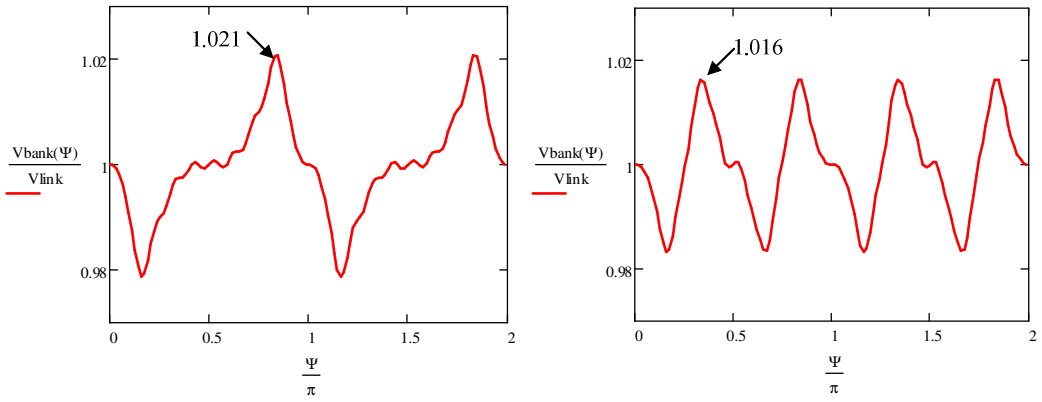
$$V_c(t) = \left\{ \frac{1}{24\omega C} \begin{bmatrix} 12\left(m\,\mathrm{I_m}\cos\varphi_1 - m_{3h} I_{m3h}\cos\varphi_3\right)\omega t - 6m\left(\mathrm{I_m}\sin(2\omega t - \varphi_1) - I_{m3h}\sin(\omega t - \varphi_3)\right) \\ +3\left(m_{3h}\,\mathrm{I_m}\sin(4\omega t - \varphi_1\right) - mI_{m3h}\sin(4\omega t - \varphi_3) \\ -8\left(3I_m\cos(\omega t - \varphi_1) + I_{m3h}\cos(3\omega t - \varphi_3)\right) + 2m_{3h} I_{m3h}\sin(6\omega t - \varphi_3) \end{bmatrix} + K_3 \right. \quad (5.25)$$

The integration constants K_0 to K_3 are obtained based on the H-bridge cell capacitor initial voltage. As an example for $I_{m3h} = 0$ (three-phase case), equation (5.22) reduces to:

$$0 \le \omega t < \alpha, \pi - \alpha \le \omega t < \pi$$

$$V_c(t) = \frac{1}{24\omega C} \begin{bmatrix} 36m\,\mathrm{I_m}\cos\varphi_1 \omega t - 18m\,\mathrm{I_m}\sin(2\omega t - \varphi_1) + 9m_{3h}\,\mathrm{I_m}\sin(4\omega t - \varphi_1) \\ -48I_m\cos(\omega t - \varphi_1) \end{bmatrix} + K_0 \quad (5.26)$$

Equation (5.26) demonstrates that the H-bridge cell capacitor may experience a lower current loading in the three-phase case than in the single-phase case. This is due to the absence of the third harmonic component of the current that may flow through the H-bridge cell capacitors. This may also be reflected in the capacitor size and converter losses. Figure 5-7 shows one cycle of the capacitor voltage ripple referred to ½V_{dc}: (a) shows the capacitor ripple in the single-phase case with a certain 3rd harmonic component in the output current, and (b) shows the capacitor ripple in the three-phase system with a purely sinusoidal output current.



(a) (b)

Figure 5-7: Capacitor voltage ripple referred to ½ V_{dc} (a) single-phase case (b) three-phase case (modulation index m=1, power factor $p.f.$ =1).

5.4.2 Power flow and energy circulation analysis

Since the cascaded H-bridge cells of the HCMC in Figure 5-1 only compensate for harmonics as depicted in Figure 5-2, the average active power these cells exchange with the load over a full fundamental period must be zero. To prove this observation mathematically, the H-bridge reference voltage is recalled in equation (5.27):

$$V_{HB}(t)=\begin{cases}\frac{1}{2}V_{dc}(m\sin\omega t+1-m_{3h}\sin 3\omega t) & 0\le\omega t<\alpha,\pi-\alpha\le\omega t<\pi,\pi+\alpha\le\omega t<2\pi-\alpha\\ \frac{1}{2}V_{dc}(m\sin\omega t-1-m_{3h}\sin 3\omega t) & \alpha\le\omega t<\pi-\alpha,\pi\le\omega t<\pi+\alpha,2\pi-\alpha\le\omega t<2\pi\end{cases} \quad (5.27)$$

If the phase current is:

$$i_a(t)=I_m\sin(\omega t-\varphi) \quad (5.28)$$

Where I_m is peak phase current and φ donates power factor angle.

The average instantaneous power cascaded H-bridge cells exchange with the load can be expressed as:

$$P=\frac{1}{2\pi}[\int_0^{\alpha}d_1 i_a d\omega t+\int_{\alpha}^{\pi-\alpha}d_2 i_a d\omega t+\int_{\pi-\alpha}^{\pi}d_1 i_a d\omega t\int_{\pi}^{\pi+\alpha}d_2 i_a d\omega t+\int_{\pi+\alpha}^{2\pi-\alpha}d_1 i_a d\omega t+\int_{2\pi-\alpha}^{2\pi}d_2 i_a d\omega t]\cdot\frac{1}{2}V_{dc} \quad (5.29)$$

Then:

$$P=\tfrac{1}{2}V_{dc}\left(\pi m I_m\cos\varphi-4I_m\cos\varphi(2\cos\alpha-1)\right) \quad (5.30)$$

By recalling equation (5.2)

$$P=\tfrac{1}{2}V_{dc}\left(\pi m I_m\cos\varphi-4I_m\cos\varphi\times\tfrac{1}{4}m\pi\right)=0 \quad (5.31)$$

Where $d_1=2\bar{V}_{HB}-1$, $d_2=2\bar{V}_{HB}$, $d_3=2\bar{V}_{HB}+1$ and $d_4=2(\bar{V}_{HB}+1)$, and $\bar{V}_{HB}$ represents H-bridge voltage in equation (5.20) normalized by ½V_{dc}.

The relationship between switching angle for 2-level main bridge and modulation

index m is given by equation (5.2). Calculation of the harmonic magnitudes to be provided by the H-bridge compensator can be expressed by:

$$V_h(n,M)=\frac{2}{\pi}\left(\int_0^{\alpha(m)}-\sin(n\cdot\theta)d\theta+\int_{\alpha(m)}^{\pi-\alpha(m)}\sin(n\cdot\theta)d\theta+\int_{\pi-\alpha(m)}^{\pi}-\sin(n\cdot\theta)d\theta\right) \quad (5.32)$$

Where: n is the harmonic order.

Figure 5-8 shows fundamental voltage magnitude and 3rd to 11th harmonic magnitude versus modulation index *m*.

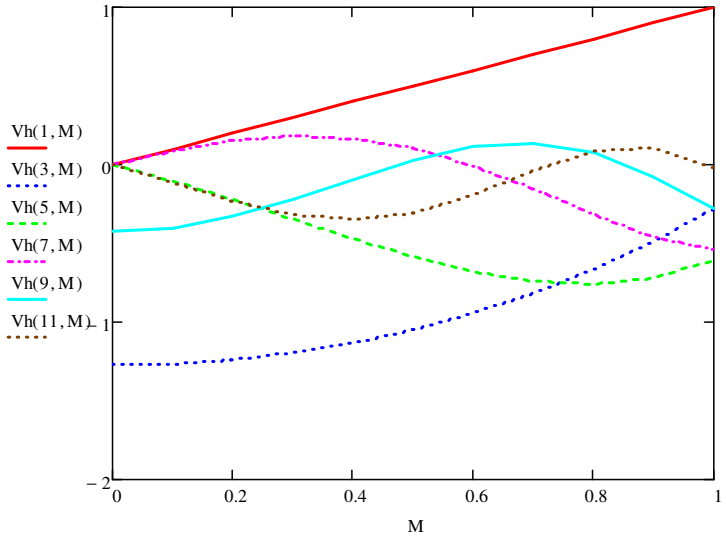


Figure 5-8: Fundamental and low-order harmonics versus modulation index.

The total compensating waveform up to the X^{th} harmonic can be derived by:

$$V_h(\theta)=\sum_{n=2}^{X}V_h(n,m)\cdot\sin(n\cdot\theta) \quad (5.33)$$

The compensating waveform requires H-bridge cells operating at unity modulation index, hence the compensating waveform can be rewritten:

$$V_h(\theta)=\sum_{n=2}^{X}V_h(n,1)\cdot\sin(n\cdot\theta) \quad (5.34)$$

If a specific 3rd harmonic magnitude is subtracted from the compensating waveform to recalculate the compensating waveform to be bounded within ± 1, then the new compensating waveform is expressed by:

$$V_{h+3}(\theta)=\sum_{n=2}^{X}V_h(n,1)\cdot\sin(n\cdot\theta)-K_3\sin(3\cdot\theta) \quad (5.35)$$

Where K_3 is the magnitude of the 3rd harmonic.

Assuming the output current is sinusoidal and at unit power factor to simplify the mathematical analysis, the energy that must be held in the H-bridge capacitor bank is given by:

$$E_{bank}(\theta) = \int_0^{\theta} P_{bank}(\theta) d\theta \tag{5.36}$$

Where $P_{bank}(\theta) = I_m \sin(\theta) \cdot V_{h+3}(\theta)$

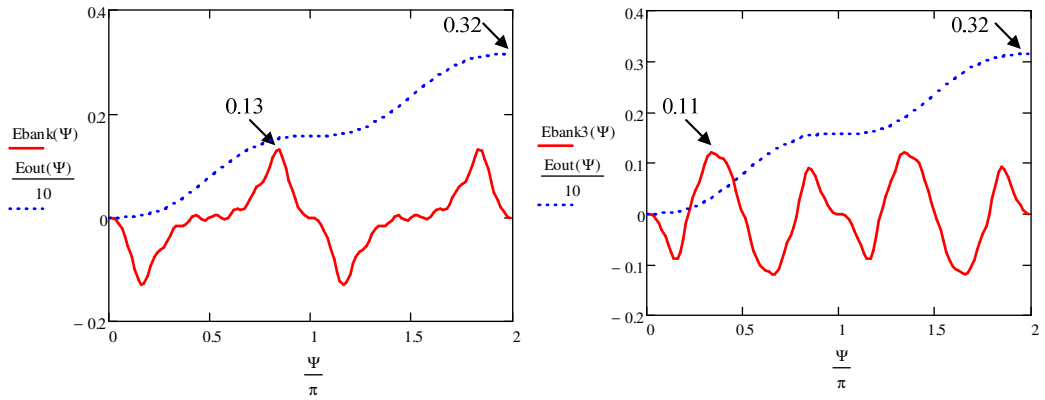
Total output energy transferred from the DC link is:

$$E_{out}(\theta) = \int_0^{\theta} P_{out}(\theta) d\theta \tag{5.37}$$

Where:

$$P_{out}(\theta) = I_m \sin(\theta) \cdot V_h(1, m)$$

Assuming a modulation index m=1 and unity power factor, a 3rd harmonic component magnitude of 0.42 is subtracted from the compensation waveform, (after normalizing the voltage and current to unity). The peak energy stored energy by the compensating H-bridge cells and total output energy per cycle of the fundamental with and without 3rd harmonic injection are shown in Figure 5-9. The ratios of energy output over one cycle to peak energy stored by the H-bridges with and without 3rd harmonic subtraction are 0.13/3.2=4.06% and 0.11/3.2=3.4% respectively.



(a) (b)

Figure 5-9: Energy stored in H-bridge capacitor bank and total output energy per cycle, (a) without 3rd harmonic subtraction (b) with 3rd harmonic subtraction.

5.5 Simulations

5.5.1 Independent control using SHE-PWM and high-frequency PWM

5.5.1.1 Control strategy

Provided zero average power from the cascaded H-bridge cells is exchanged with the load over the full fundamental period, cell capacitor voltage balance of the HCMC in Figure 5-1 can be maintained theoretically. However, due to switching device nonlinearities, tolerances in cell capacitance values, and an imperfect modulation strategy, a capacitor voltage balancing method is required to ensure that the cell capacitor voltages are maintained around the set-point, compatible with the voltage ratings of the switching devices within each H-bridge cell. Such a capacitor voltage balancing method must also account for H-bridge losses. The simulation uses H-bridge cell redundant switch states that produce the same voltage levels but with different impact on the state-of-charge of the cell capacitors, to maintain cell capacitors voltage balance. This necessitates charge or discharge of the cell capacitors depending on their voltage magnitude and the polarity of the load current. A small fundamental voltage is required to interact with fundamental current flowing through the cascaded H-bridge cells in order to compensate for the H-bridge losses. This small fundamental component ΔM is obtained from a proportional-integral (PI) controller that forces all the cell capacitors to converge toward a desire set-point, as shown in Figure 5-10. By adding to the predefined modulation index M, the expected sinusoidal output voltage is achieved. The compensation waveform for the H-bridge cells is obtained by subtraction of the two-level inverter output voltage, with an m-dependant 3^{rd} harmonic component, from the sinusoidal waveform. The H-bridge cells are modulated with high-frequency PD carrier PWM to produce a multilevel output voltage.

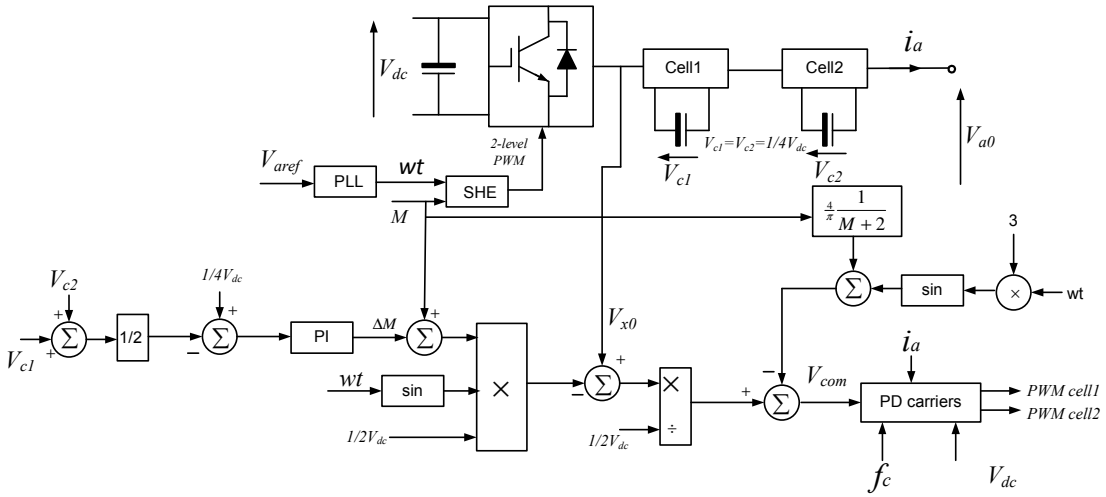


Figure 5-10: Schematic diagram illustrates modulation and capacitor voltage balancing of the hybrid multilevel converter with two ac side cascaded H-bridge cells.

5.5.1.2 Performance evaluation

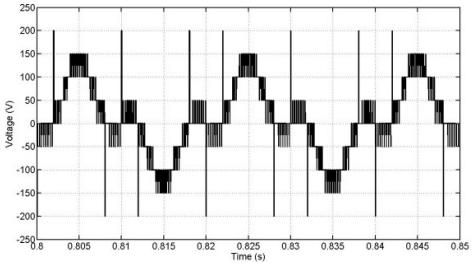
To demonstrate the feasibility of the proposed modulation strategy applied to the HCMC, the converter in Figure 5-2 is modelled and simulated under three different conditions. The first case considers a three-phase hybrid multilevel converter with two H-bridge cells (Figure 5-1) to demonstrate the viability of the presented modulation strategy. The second case considers the scalability of the concept to medium-voltage applications. Seven and ten cells in the ac side of the hybrid multilevel converter are simulated under different operating conditions. The third case simulates the HCMC in a high-voltage application: specifically, a three-phase hybrid converter with 20 ac side cascaded H-bridge cells is simulated under different power factors and modulation indices.

Case I: Three-phase Hybrid cascaded multilevel converter with two ac side cascaded H-bridge cells

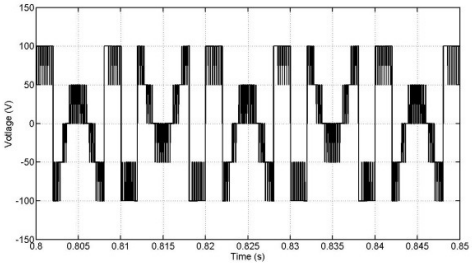
The two-level converter stage and ac side cascaded H-bridge cells are controlled using SHE and level shifted PWM with 4kHz switching frequency, respectively. The dc link of the two-level converter stage is 200V, and each H-bridge cell capacitor is regulated at 50V and incorporates 1mF of capacitance. The ac side uses an RL load with 25Ω resistance and 0.035H inductance. To illustrate that with the presented

modulation strategy the HCMC can operate independent of load power factor and modulation index, the converter in Figure 5-1 is simulated at different power factors and modulation indices.

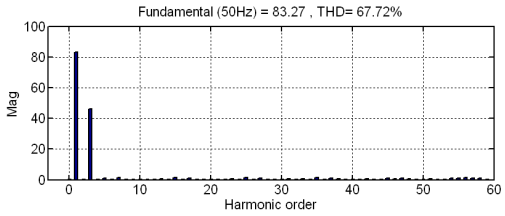
Figure 5-11a and b show phase voltage relative to the supply mid-point, and total voltage across the cascaded H-bridge cells. The principle of multilevel modulation only permits the switching of one voltage level within each switch cycle, but here this is violated several times within one fundamental period. These violations can be observed in the voltage across cascaded H-bridge cells by the abrupt switching instants between $+½V_{dc}$ and $–½V_{dc}$. This causes synchronization problems due to the difficulties in tracking such sharp edges, hence preventing simultaneous switching of the two-level converter stage and the H-bridge cells. These switching delays cause spikes in the converter output voltage. Figure 5-11c and d show the spectrum of phase voltage, V_{a0} and the voltage across the H-bridge cell, V_{HB}. Notice the presence of the third harmonic in both phase and H-bridge cell voltages as demonstrated by equation (5.6). This shows that the presented modulation strategy uses the third harmonic to minimize the number of H-bridge cells required such that the voltage across these cells sum to $½V_{dc}$, which is equivalent to 1 per unit peak of the H-bridge normalized reference voltage, in maximising dc link voltage utilization. The presented modulation strategy extends the linear modulation index range beyond 1.15, up to 1.27. Figure 5-11e shows the two-level converter output voltage referred to the supply mid-point, where SHE-PWM is used to adjust the fundamental magnitude. Figure 5-11f shows capacitor voltage across the H-bridge cells. Observe that the H-bridge capacitor voltages are maintained at $¼V_{dc,}$ as demonstrated in Figure 5-11g. Figure 5-11h shows the line voltage and three-phase current. The spectrum of the voltage across all the H-bridge cells contains a small fundamental component to maintain voltage balance of the cell capacitors and compensate for the losses, as explained in 5.5.1.1 and Figure 5-10.



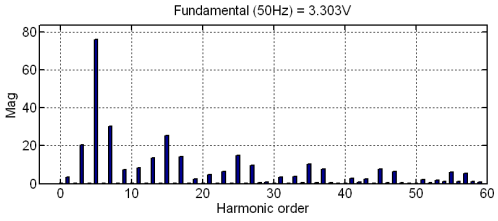
a) Phase voltage, V_{a0} referred to supply mid-point.



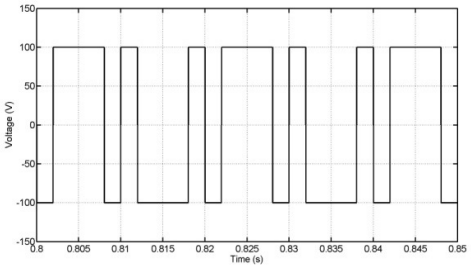
b) Voltage across ac side cascaded H-bridge cells.



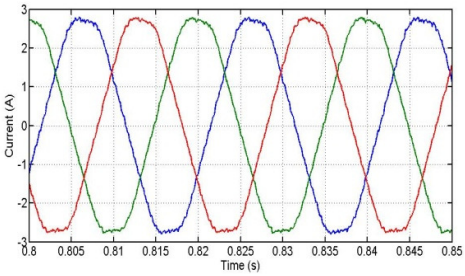
c) Spectrum of phase voltage, V_{a0}.



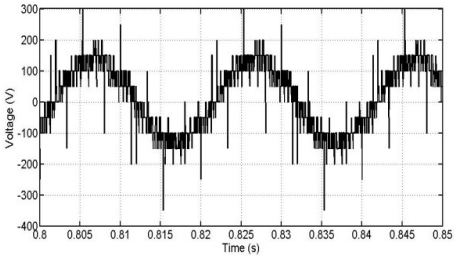
d) Spectrum of voltage across ac side cascaded H-bridge cells.



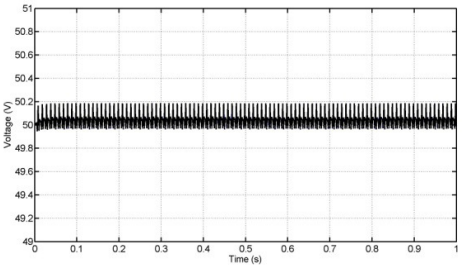
e) Two-level converter output voltage referred to supply mid-point.



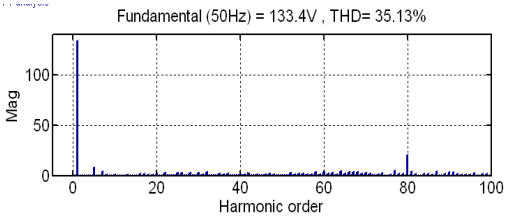
f) Voltage across capacitors of the ac side cascaded H-bridge cells.



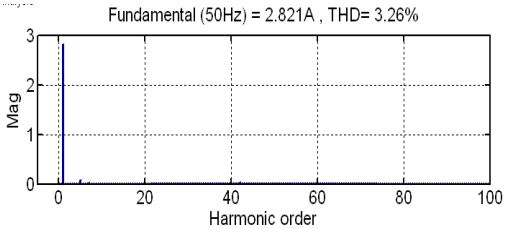
g) Line voltage.



h) Three-phase current.



i) Spectrum of line voltage.

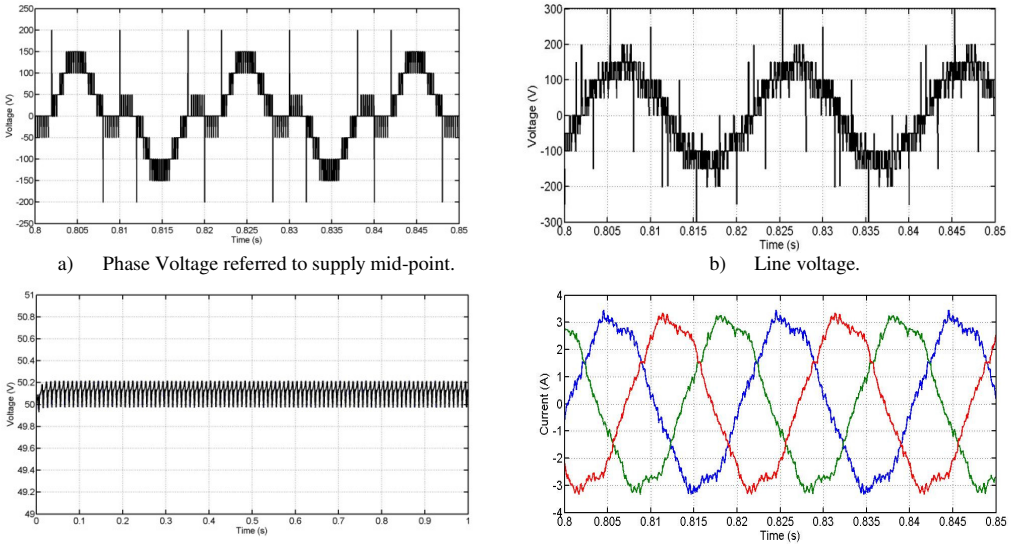


j) Spectrum of three-phase current.

Figure 5-11: Waveforms obtained when hybrid multilevel converter in Figure 5-1, with 200V dc link voltage, operates at 0.8 power factor lagging and 0.9 modulation index.

Figure 5-12 shows phase voltage, voltage across the H-bridge cells, capacitor voltages and phase current obtained when the converter operates at a modulation index of 0.8 and unity power factor. The output voltage and current waveforms are shown with distortion since no inductance is incorporated in the load.

Figure 5-11 and Figure 5-12 demonstrate operation of the HCMC independent of load power factor. To further demonstration the extension of the modulation index linear range while the HCMC provides real power, simulation results are presented in Figure 5-13 when the converter in Figure 5-1 operates at 0.9 power factor lagging and a modulation index of 1.27. The converter is able to cope without any difficulty, the voltage stresses across the H-bridge capacitors being controlled.



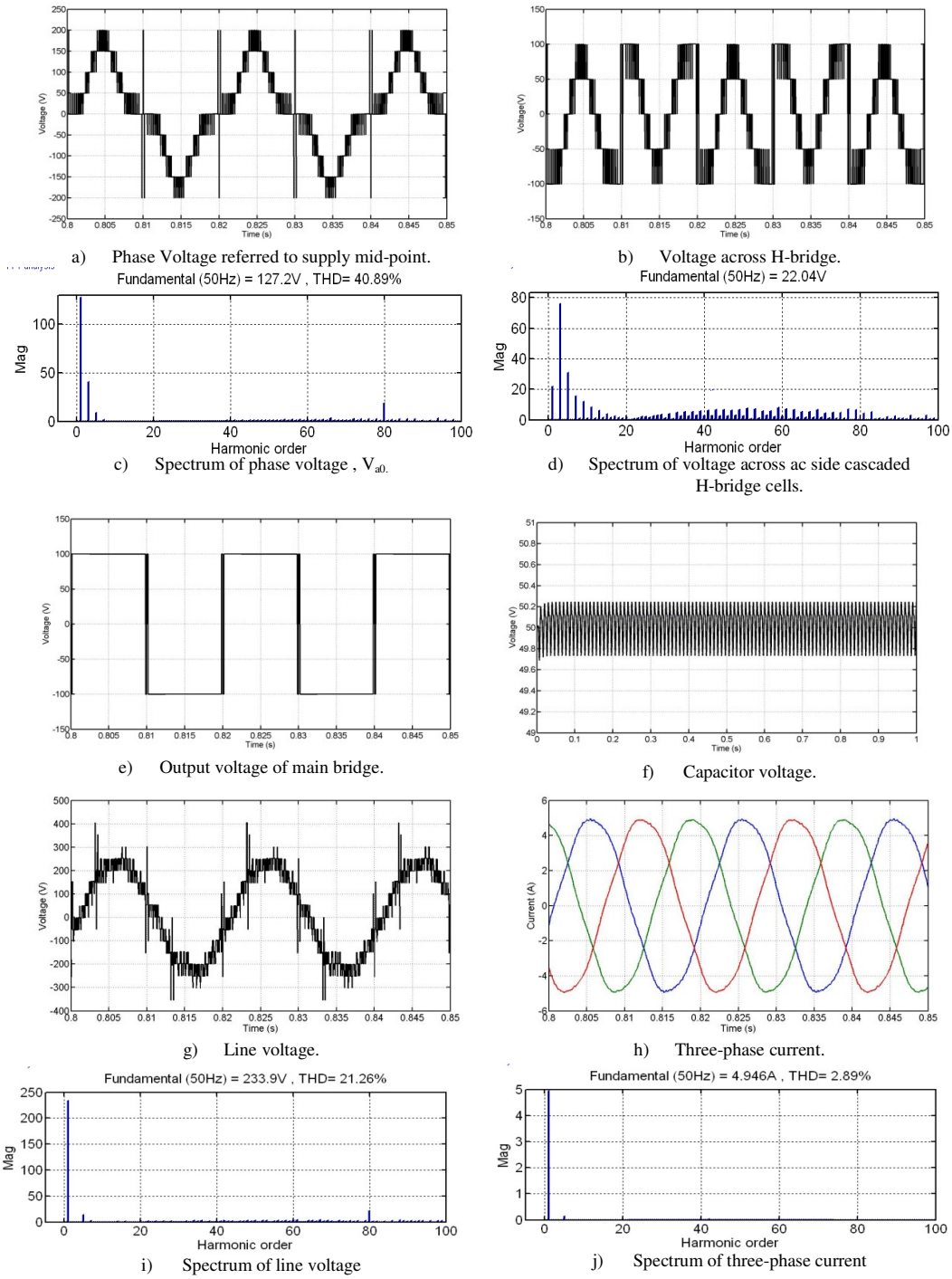
a) Phase Voltage referred to supply mid-point.

b) Line voltage.

c) Capacitor voltage.

d) Three-phase current.

Figure 5-12: Waveforms obtained when hybrid multilevel converter in Figure 5-1, with 200V dc link voltage, operates at unity power factor and 0.8 modulation index.



a) Phase Voltage referred to supply mid-point.

b) Voltage across H-bridge.

c) Spectrum of phase voltage , V_{a0}.

d) Spectrum of voltage across ac side cascaded H-bridge cells.

e) Output voltage of main bridge.

f) Capacitor voltage.

g) Line voltage.

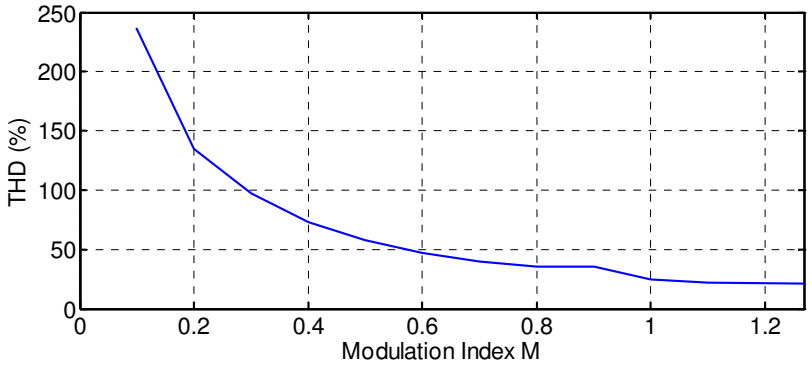
h) Three-phase current.

i) Spectrum of line voltage

j) Spectrum of three-phase current

Figure 5-13: Waveforms obtained when hybrid multilevel converter in Figure 5-1, with 200V dc link voltage operates at 0.9 power factor lagging and 1.27 modulation index.

Figure 5-14 shows the relationship between line-to-line voltage THD and modulation index. As the modulation index increases, line-to-line voltage THD decreases.



k) Relationship betwwen line-to-line voltage THD with modulation index.

Figure 5-14: shows the relationship between line-to-line voltage THD and modulation index.

Case II: Scalability to Medium-Voltage applications

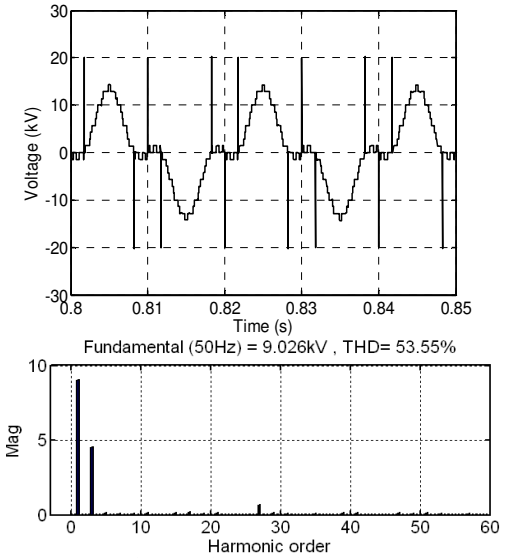
To demonstrate that the HCMC is also suitable for medium to high voltage applications and is capable of operating over the entire linear range of modulation indices and power factors, two HCMC with seven and ten H-bridge cells in the ac side are considered. All simulations use a dc rail voltage of 20kV, 5000μF cell capacitors, and a switching frequency of 1.35kHz. By simulating at different modulation indices and load power factors, the quality of the output voltage waveform and capacitor voltage balancing are evaluated.

HCMC with seven H-bridge cells in ac side:

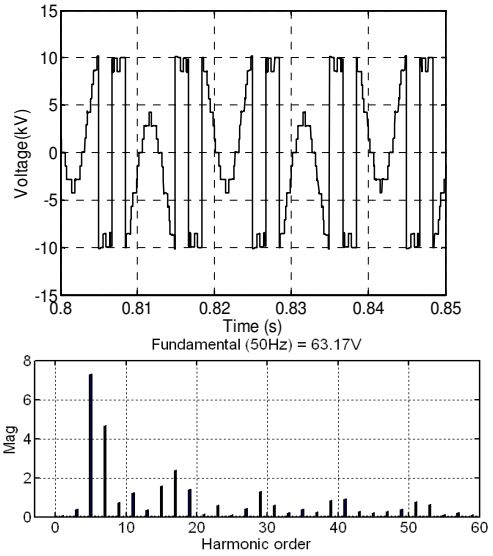
Modulation index m=0.9, power factor=0.88 lagging

Figure 5-15 shows the simulation results for a HCMC with seven H-bridge cells each blocking 1.43kV. The HCMC delivers 16MW, with a 20kV dc link voltage, operating at 0.8 power factor lagging and 0.8 modulation index. Figure 5-15a shows that the third harmonic is the dominant phase voltage harmonic. Figure 5-15b shows that the H-bridge cells contain a small fundamental component of 63.17V (0.7% of the fundamental phase voltage) plus harmonics. This fundamental voltage is associated with the active power required to maintain the average cell voltage at 1.43kV. From Figure 5-15c, the line-to-line voltage contains several non-triplen harmonics: 5^{th}, 7^{th}, 11^{th} and 13^{th}. Large spikes in the phase and line-to-line voltage can be observed. As with the HCMC with two H-bridge cell in the ac side, these spikes also due to the inability of the H-bridge cells to track the step edges in the

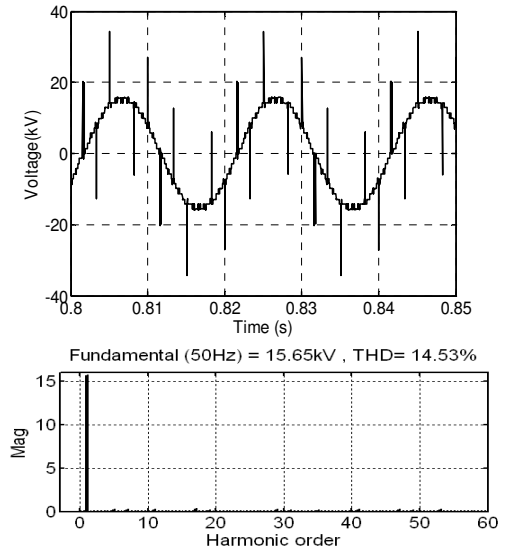
reference modulating signal. Figure 5-15d shows the voltage at the terminal of the main two-level bridge and its spectrum, it contains large amount of low order harmonics that needs to be cancelled by H-bridge cells.



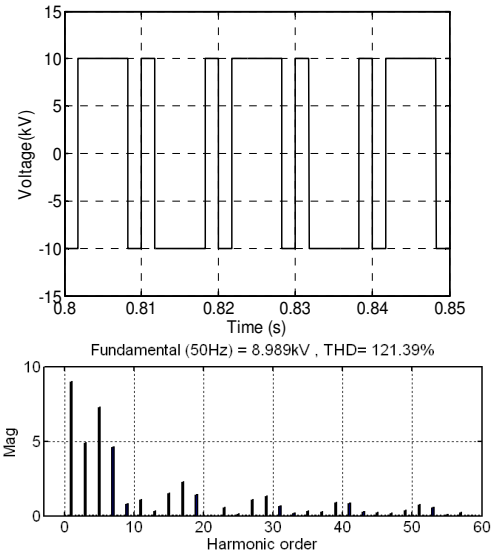
a) Phase voltage and its spectrum.



b) Voltage across H-bridge cells and its spectrum.



c) Line-to-line voltage and its spectrum.

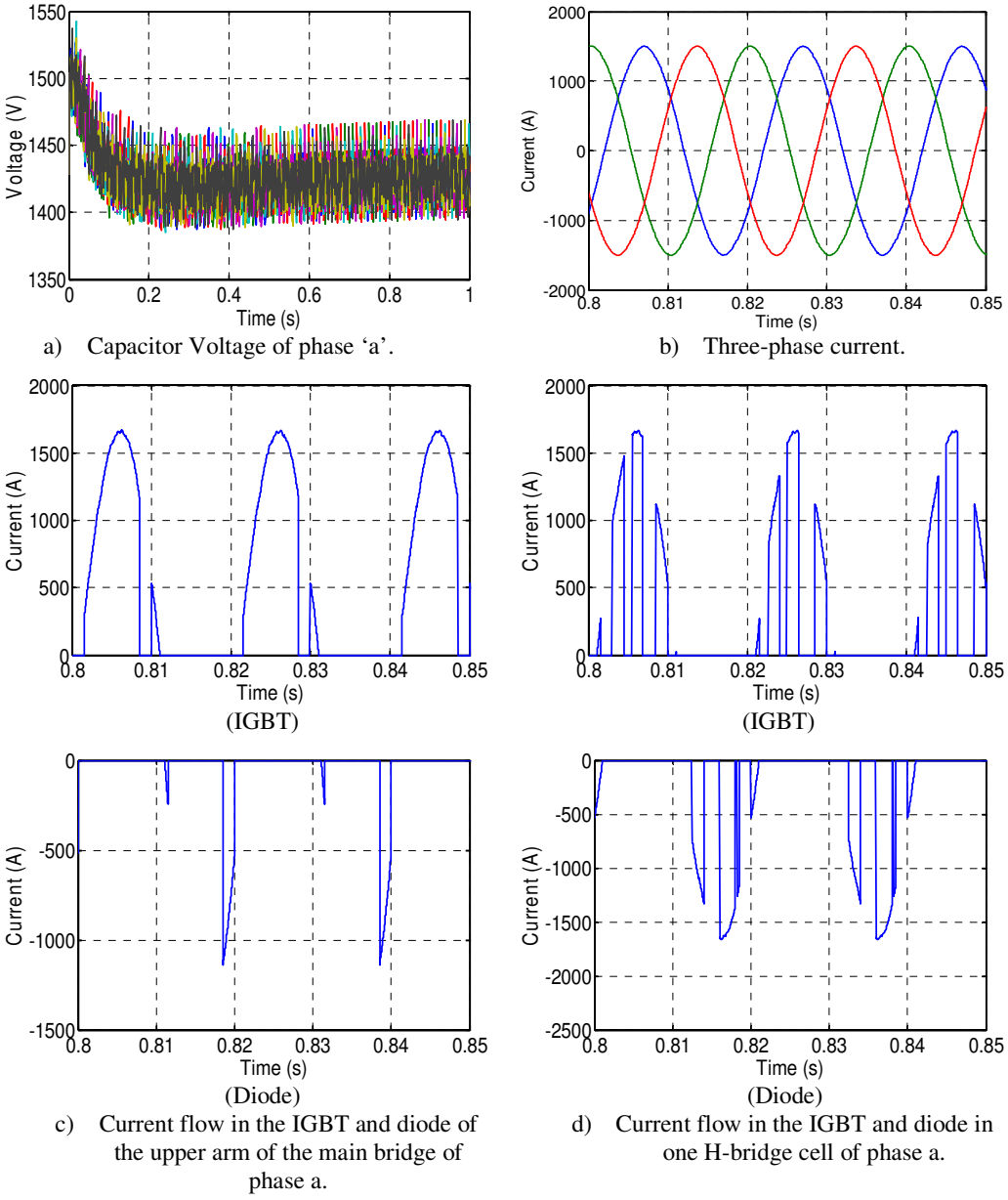


d) Voltage at the terminal of the main two-level bridge and its spectrum.

Figure 5-15: Waveforms obtained when hybrid multilevel converter with seven H-bridge cells in ac side, with 20KV dc link voltage operates at 0.8 power factor lagging and 0.8 modulation index.

Figure 5-16a shows that the seven cell capacitors are stabilized at 1.43kV in phase a, as also in phases b and c. Figure 5-16c and Figure 5-16d show the current waveforms of an IGBT and diode in the upper arm of the main bridge and one switch in an

H-bridge cell in phase a. The two-level main bridge operates at 150Hz per fundamental cycle, meaning there are only four switching instants in each cycle which reduces the switching losses of the two-level main bridge. Although cumulatively the seven H-bridge cells operate at 1.35kHz, the effective switching frequency of each switch is low, only 200Hz as shown (Figure 5-16d) by the IGBT voltage from one cell.



a) Capacitor Voltage of phase 'a'.

b) Three-phase current.

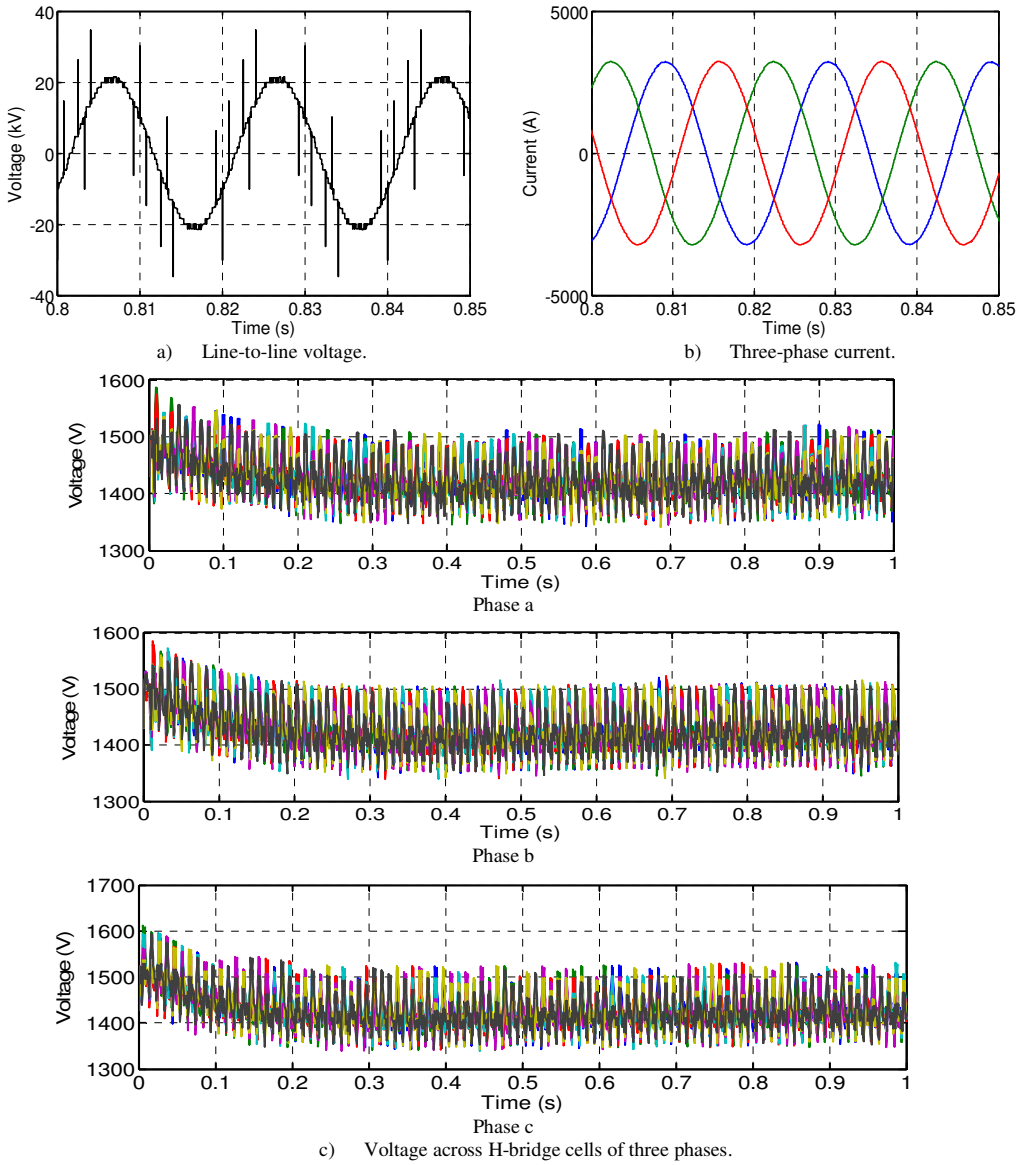
c) Current flow in the IGBT and diode of the upper arm of the main bridge of phase a.

d) Current flow in the IGBT and diode in one H-bridge cell of phase a.

Figure 5-16: Waveforms obtained when hybrid multilevel converter with seven H-bridge cells in ac side, with 20KV dc link voltage operates at 0.8 power factor lagging and 0.8 modulation index.

Modulation index m=1.2, power factor=0

Figure 5-17 shows the simulation waveform results when the converter operates with modulation index of 1.2 and zero power factor. Figures 5-17a and b show the line-to-line voltage and three-phase current: the current waveform quality is better than the waveform obtained from case I. With the ac side H-bridge cell number increasing, better current waveform quality can be expected. Despite the fundamental current and voltage being 90° out of phase, voltage balancing of the H-bridge cell capacitors is maintained at the desired point which is shown in Figure 5-17c.



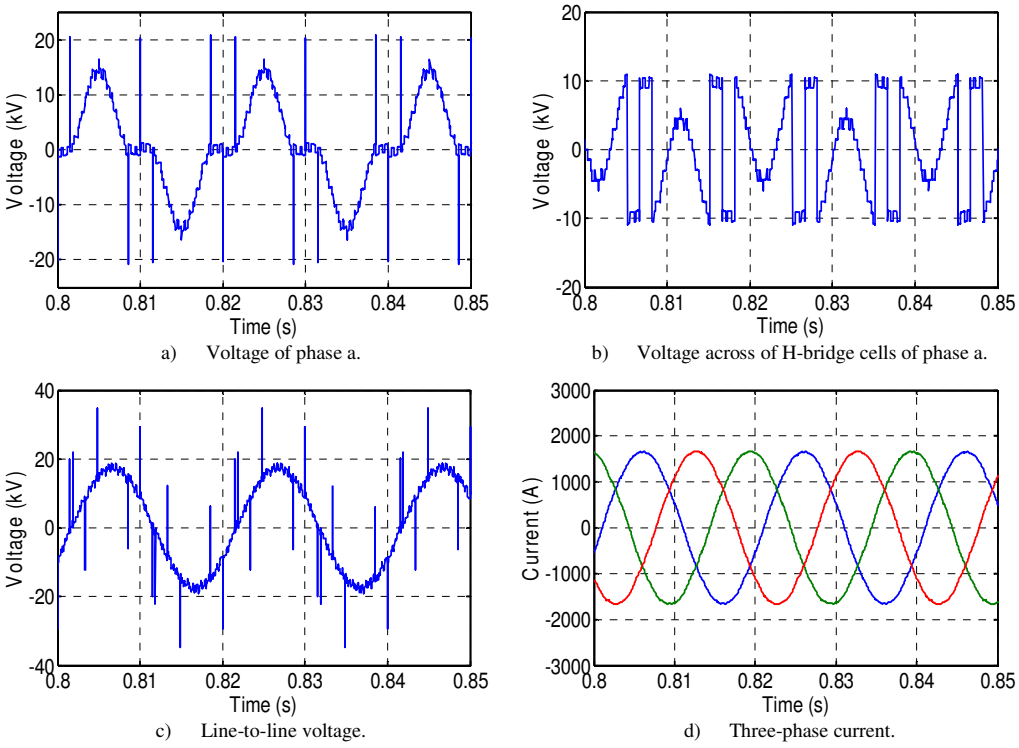
a) Line-to-line voltage. b) Three-phase current.

c) Voltage across H-bridge cells of three phases.

Figure 5-17: Waveforms obtained when hybrid multilevel converter with seven H-bridge cells in ac side, with 20kV dc link voltage operates at zero power factor lagging and 1.2 modulation index.

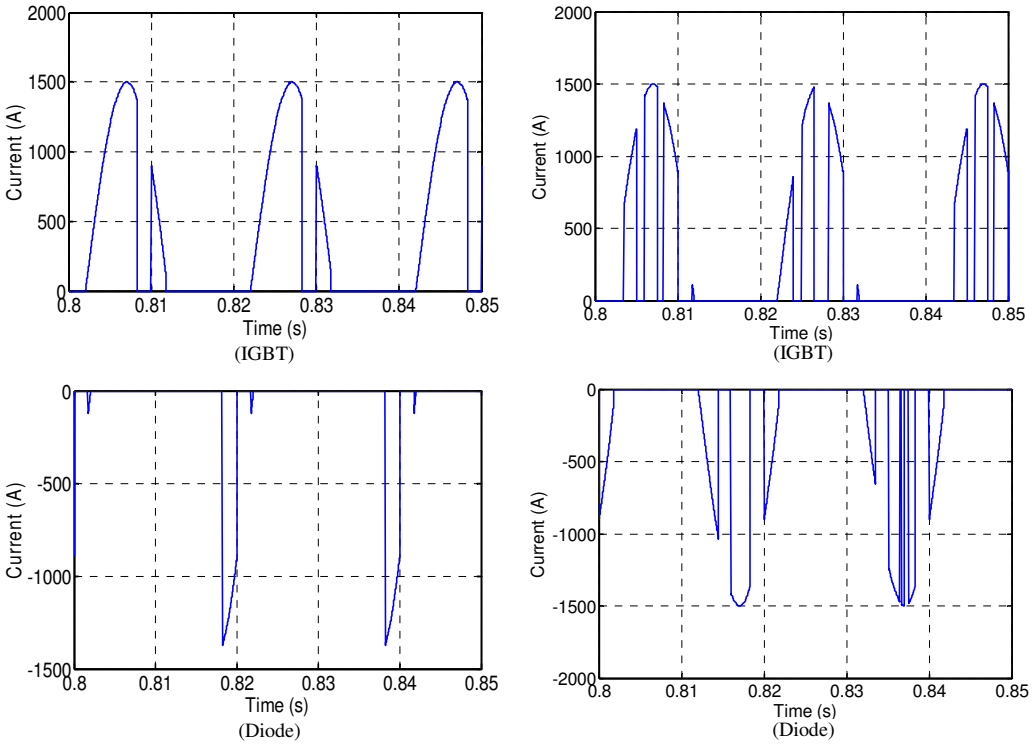
HCMC with ten H-bridge cells in the ac side:

Figure 5-18 shows simulation waveforms for an HCMC with ten H-bridge cells each blocking 1.5kV. The converter delivers 19MW, with a 20kV dc link voltage and operates at 0.95 power factor lagging and unity modulation index. Figure 5-18a to Figure 5-18c shows the HCMC control strategy is viable if the fundamental voltage of the H-bridge cells is locked in phase with the phase current, whence H-bridge cell voltage balance can be maintained independent of load power factor and modulation index. From Figure 5-19a and Figure 5-19b,the two-level main bridge operating frequency is 150Hz, the same as the seven-level version while the effective switching frequency of the H-bridge cell switches is reduced from 200Hz to 150Hz, since ten H-bridge cells create more redundancy for capacitor balancing requirements, thus reducing the switching loss of each cell.



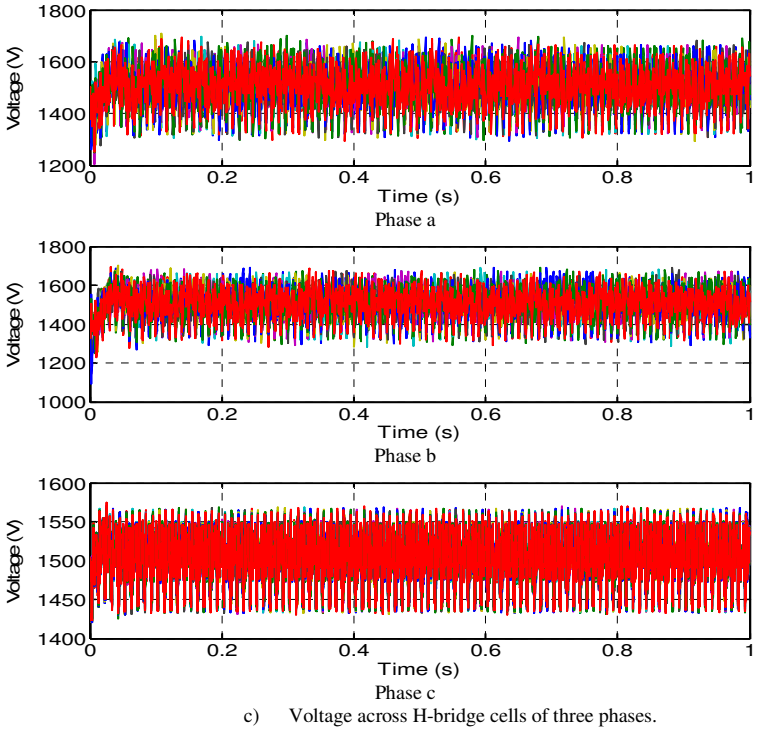
a) Voltage of phase a.
b) Voltage across of H-bridge cells of phase a.
c) Line-to-line voltage.
d) Three-phase current.

Figure 5-18: Waveforms obtained when hybrid multilevel converter with ten H-bridge cells in ac side, with 20KV dc link voltage operates at 0.95 power factor lagging and unity modulation index.



a) Current flow in the IGBT and diode of the upper arm of the main bridge of phase a.

b) Current flow in the IGBT and diode in one H-bridge cell of phase a.



c) Voltage across H-bridge cells of three phases.

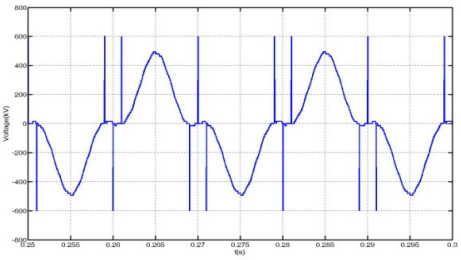
Figure 5-19: Waveforms obtained when hybrid multilevel converter with ten H-bridge cells in ac side, with 20kV dc link voltage operates at 0.95 power factor lagging and unity modulation index.

Case III: Scalability to High-Voltage applications

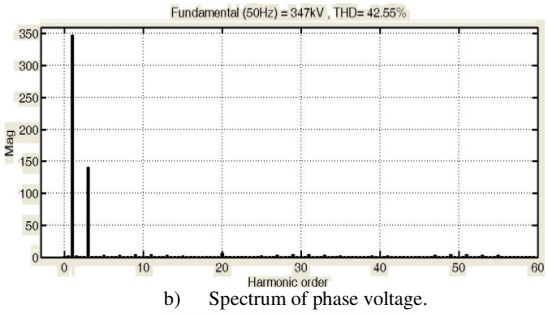
HCMC with Twenty H-bridge cells in ac side:

To demonstrate the viability of the HCMC in high-voltage applications, a three-phase hybrid converter with a 600kV dc link voltage, 20 cells (with 4mF of capacitance, blocking 15kV, and capable of generating 81 voltage levels) is simulated. In this case, the cascaded H-bridge cells are controlled using multilevel PWM with a 1kHz switching frequency. To show that the converter with a large number of H-bridge cells can operate independent of load power factors and modulation index, the converter is simulated at different load power factors and modulation indices. The results are shown in Figure 5-20 and Figure 5-21.

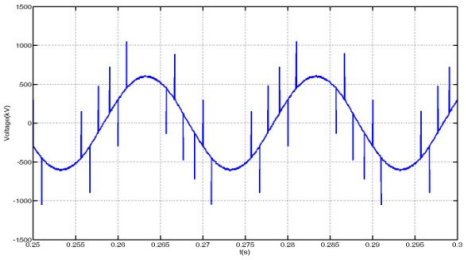
The results in Figure 5-20 are when the hybrid converter with 20 cells per phase is operated at 1.15 modulation index and 0.95 load power factor lagging. This case shows that the proposed modulation strategy generates more fundamental voltage than any other voltage source converter presented in the literature. This feature can be utilized to reduce converter semiconductor losses by delivering a specific amount of power at higher voltage, hence the converter switches experience lower currents. Figure 5-20a and b show phase voltage referred to the supply mid-point and its spectrum. The phase voltage remains distorted as in the single-phase case, due to the presence of a significant amount of third harmonic (Figure 5-20b). The line voltage and its spectrum shown in Figure 5-20c and Figure 5-20d respectively, demonstrate the viability of the hybrid converter in high-voltage applications, as they present high quality voltage on the ac side with extremely low harmonic distortion and *dv/dt*. The spikes in the HCMC output voltage can be removed by using small ac filters. Figure 5-20e and Figure 5-20f respectively show the voltage across the 20 H-bridge cells of one phase and its spectrum. A large number of cells per phase permits good tracking of the H-bridge reference voltage and harmonic attenuation at the converter output using a relatively low switching frequency. Unlike the single-phase case, Figure 5-20g shows the three-phase hybrid multilevel converter using a modulation strategy with optimal third harmonic subtraction injects pure sinusoidal currents. Therefore, this converter may be suitable for three-phase applications only. Figure 5-20h shows that the voltages across the capacitors of H-bridge cells of the three phases are maintained at the desire set point. This ensures the voltage stresses on the H-bride cells switches are controlled.



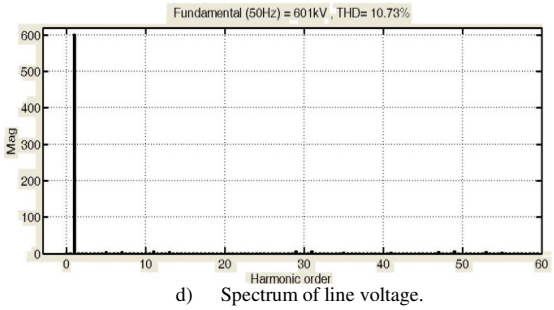
a) Phase voltage referred to supply mid-point.



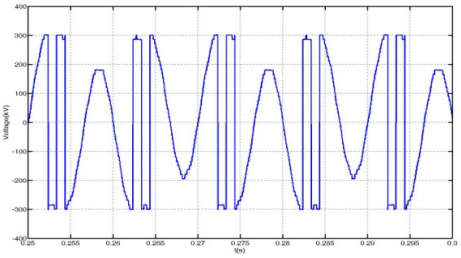
b) Spectrum of phase voltage.



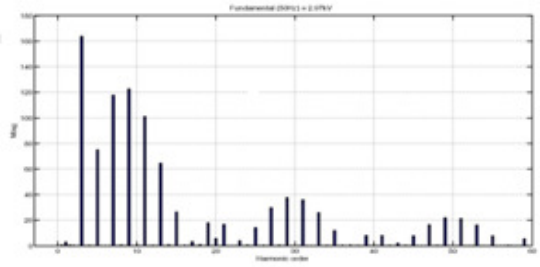
c) Line-to-line voltage.



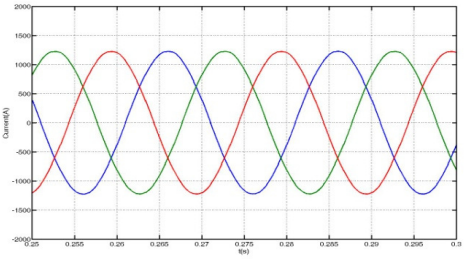
d) Spectrum of line voltage.



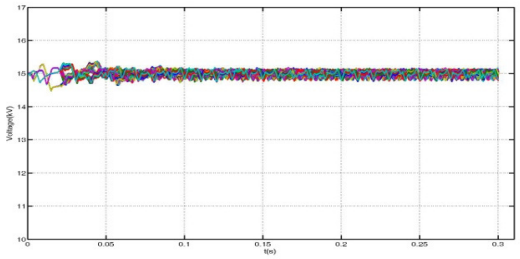
e) Voltage waveform across 20 H-bridge cells.



f) Spectrum of voltage across H-bridge cells.



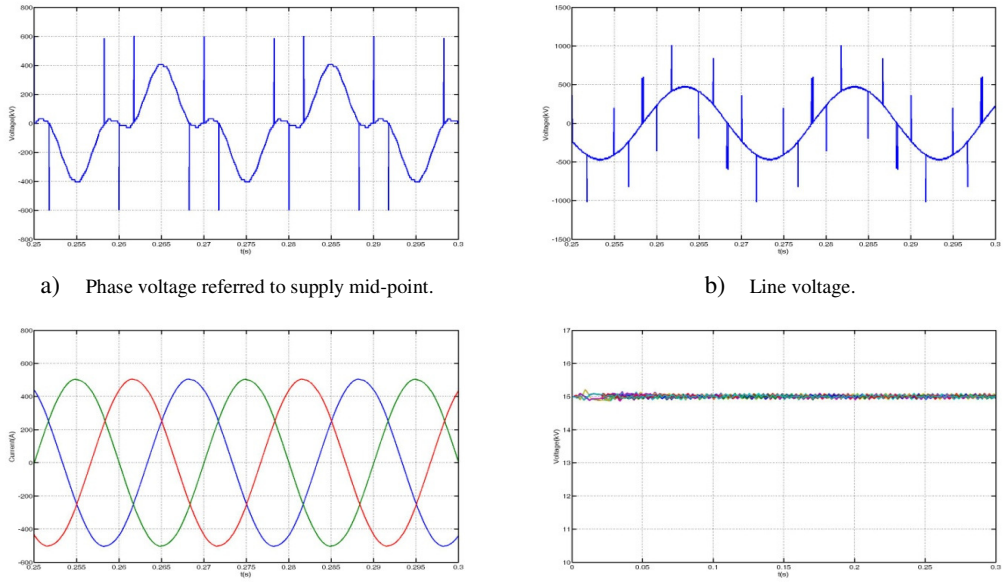
g) Phase currents.



h) Voltage across 60 H-bridge capacitors of the three-phase.

Figure 5-20:Waveforms obtained when hybrid converter with 20 cells per phase is operated 1.15 modulation index and 0.95 power factor lagging

Figure 5-21 shows the simulation results when the hybrid converter operates at 0.9 modulation index and 0.4 power factor lagging. This case demonstrates the suitability of the hybrid converter in reactive power applications. The converter is able to operate successfully without compromising the quality of the output voltage and currents, and maintains voltage balance of the H-bridge cell capacitors.



a) Phase voltage referred to supply mid-point.

b) Line voltage.

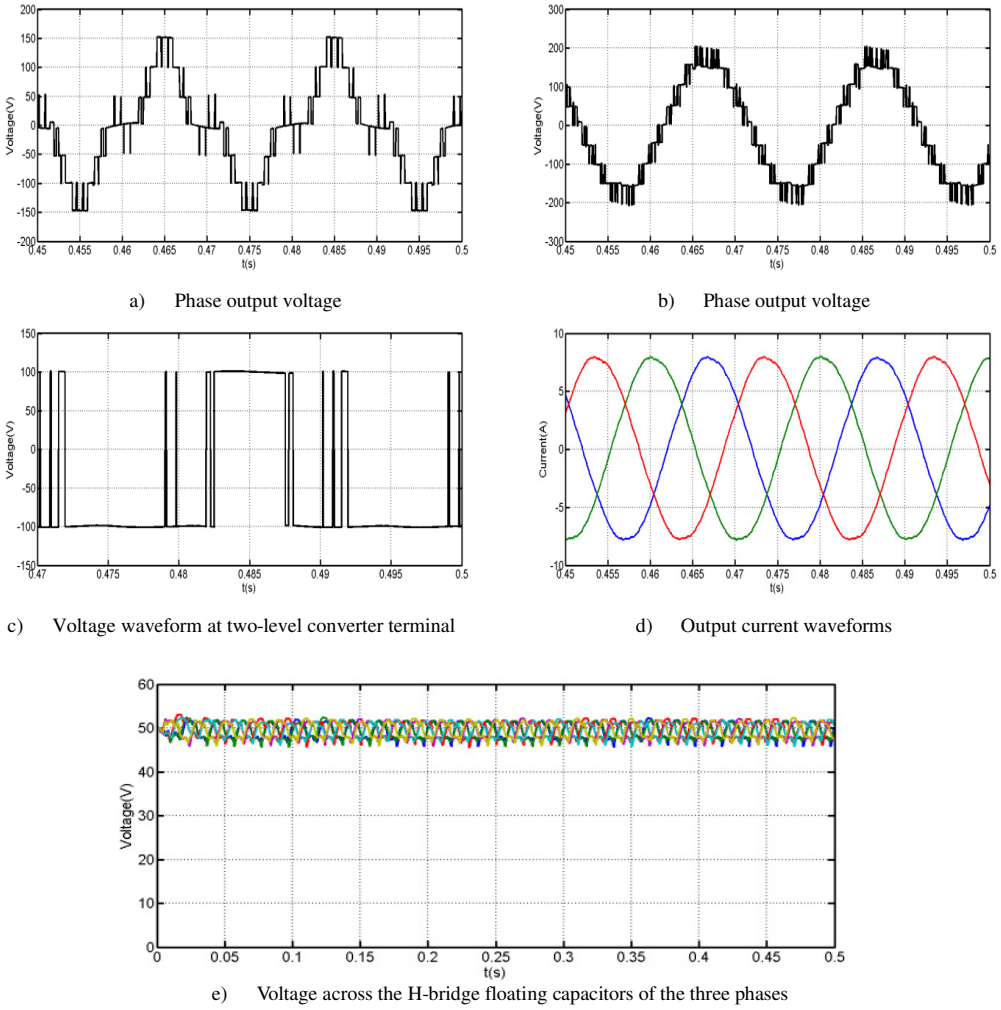
c) Phase currents.

d) Voltage across 60 H-bridge cell capacitors.

Figure 5-21: Waveforms obtained when a three-phase hybrid converter with 20 cells per phase is operated 0.9 modulation index and 0.4 power factor lagging

5.5.2 SPWM with 3rd harmonic subtraction

To demonstrate the viability of the HCMC as a universal converter for real and reactive power applications, the following simulations consider a nine-level converter with two cells per phase, with a 200V dc link voltage, and controlled using SPWM with third harmonic subtraction, at a 1.35kHz switching frequency. Each H-bridge capacitor blocks 50V and has a value of 4.7mF per cell. To demonstrate that the HCMC can operate independent of load power factor over an extended modulation index range, the converter in Figure 5-3 is simulated with several modulation indices and load power factors. Figure 5-22 shows waveforms at unity modulation index and 0.8 power factor lagging. Figure 5-22a and Figure 5-22b respectively show the phase and line voltage at the converter terminals. Switching of more than one voltage level is avoided in both the phase and line output voltages. Figure 5-22c shows the two-level converter main bridge operates at a relatively low frequency of approximately 300Hz. This is will be further reduced for hybrid converter having a large numbers of cells per phase. Figure 5-22d shows the high quality load current waveforms supplied by the converter at a 1.35kHz switching frequency. Voltage balance of the H-bridge floating capacitors is maintained around the desired set point of ¼Vdc, as depicted in Figure 5-22e, due to the proposed modification (Section 5.3.2) introduced to the normalized reference voltages.



a) Phase output voltage

b) Phase output voltage

c) Voltage waveform at two-level converter terminal

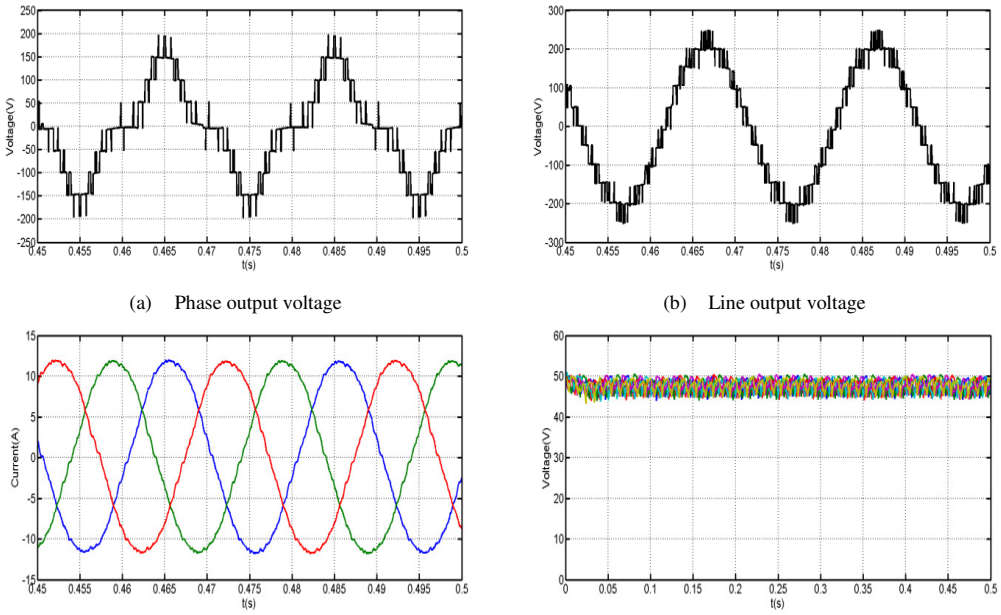
d) Output current waveforms

e) Voltage across the H-bridge floating capacitors of the three phases

Figure 5-22: Waveforms demostrating operation of hybrid cascaded voltage source multilevel converter in real power applications (modulation index m=1 and load power factor=0.8 lagging)

Figure 5-23 demonstrates that the proposed third harmonic subtraction scheme enables the hybrid converter to operate independent of load power factor over an extended modulation index linear range and confirms the validity of the capacitor voltage balancing limits established in section 5.3.2. Figure 5-23a and Figure 5-23b respectively display the phase and line output voltages generated by the hybrid converter with two cells per phase when the modulation index is 1.2 and 0.98 power lagging. The phase voltage in Figure 5-23a shows the converter utilizes the floating H-bridge capacitors to extend the modulation index linear range beyond 1.15, boosting the fundamental output voltage. This is achieved without undesirable switching transitions in the converter output voltage as shown in Figure 5-23a and

Figure 5-23b. Figure 5-23c shows the output current waveform at a high power factor and a 1.35kHz carrier frequency. Voltage balance of the floating H-bridge cell capacitors is maintained with the high modulation index and near unity power factor. This confirms the ability of HCMC to operate in active and reactive power applications with an extended modulation index as theoretically demonstrated in Section 5.3.2.



(a) Phase output voltage

(b) Line output voltage

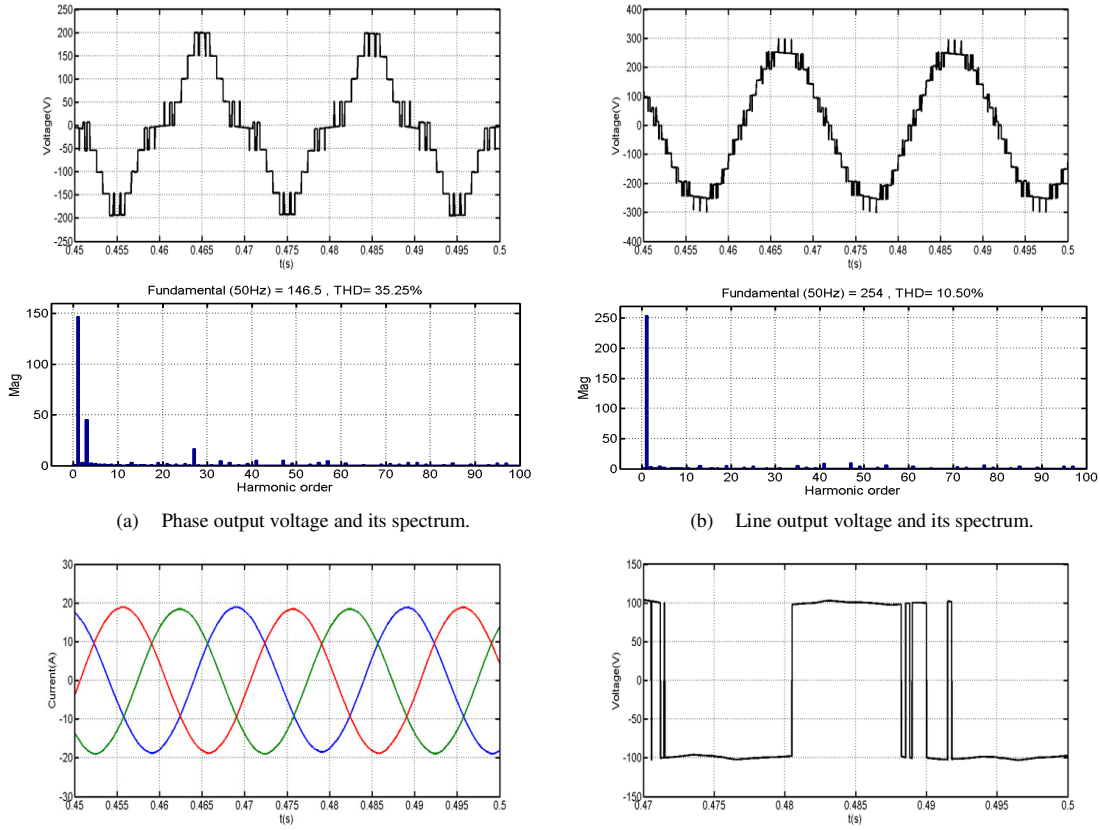
(c) Output current waveforms

(d)Voltage across the H-bridge floating capacitors of the three phases.

Figure 5-23: Waveforms demostrate operation of the hybrid cascaded voltage source multilevel converter in real power applications with extended modulation index (modulation index m=1.2 and load power factor=0.98 lagging)

To further illustrate the fundamental voltage boosting capability of the HCMC in reactive power applications, the modulation index is increased to 1.5 and the load power factor is reduced to 0.3 lagging. Figure 5-24 shows the converter remains operational with capacitor voltage balancing maintained tightly around ¼V_{dc}. The results in Figure 5-24a and Figure 5-24b show converter phase and line output voltages, and their spectra. The injected third harmonic in the phase voltage does not appear in the line voltage. Utilization of the H-bridge floating capacitors as a virtual dc link in low power factor applications permits the hybrid cascaded converter to boost the fundamental output voltage, as demonstrated in Figure 5-24a and Figure 5-24b. Figure 5-24c displays the high quality load current waveforms supplied by the converter at a high modulation index, without resurgence of low order harmonics as

with other VSCs when operated in the over-modulation region. From the voltage waveforms at the two-level converter terminals shown in Figure 5-24d, it can be observed that the switching rate of the two-level converter is significantly reduced. This is because in low power factor applications, the capacitor charging actions can be performed at not only '0' and $½V_{dc}$ voltage levels, but other voltage levels can also contribute, utilizing a current phase shift relative to the fundamental voltage (power factor angle).



(a) Phase output voltage and its spectrum.

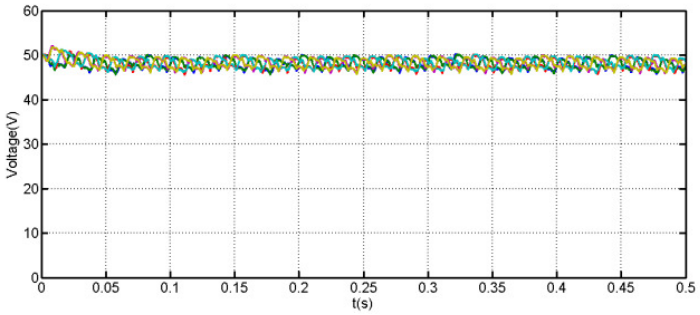
(b) Line output voltage and its spectrum.

(c) Three-phase current.

(d) Voltage waveform at two-level converter terminal.

Figure 5-24: Waveforms demostrating operation of hybrid cascaded voltage source multilevel converter in applications involving large reactive power with extended modulation index (modulation index m=1.5 and load power factor=0.3 lagging)

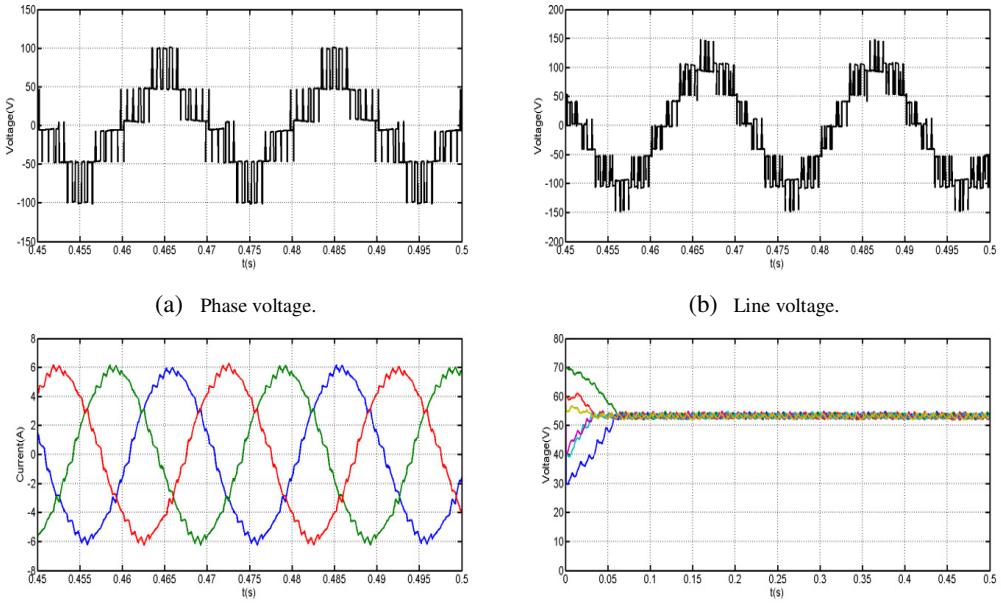
Figure 5-25 shows that the voltages across the H-bridge cell floating capacitors remain around $¼V_{dc}$ as desired. This may permit the hybrid converter to operate in reactive power applications at higher terminal voltages than other converters, with reduced currents in switching devices and without an increase in switching device voltage stresses. Hence lower conversion losses may be achieved.



(e) Voltage across the H-bridge floating capacitors

Figure 5-25: Waveforms demostrating operation of hybrid cascaded voltage source multilevel converter in applications involving large reactive power with extended modulation index (modulation index m=1.5 and load power factor=0.3 lagging)

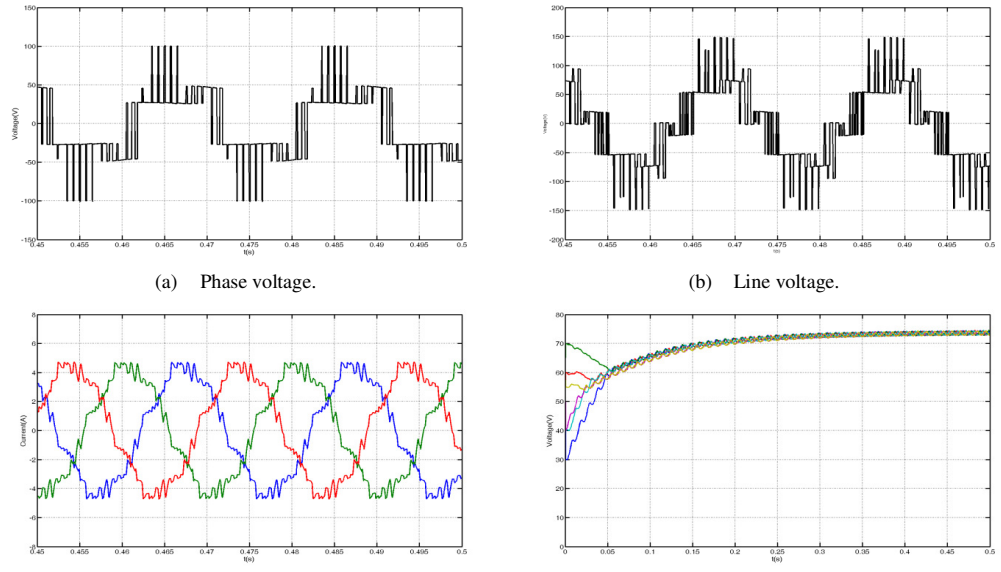
Figure 5-26 and Figure 5-27 respectively present results with and without the proposed modification to the reference voltage (Section 5.3.2). With the reference modification, capacitor voltage balancing of the H-bridge floating capacitors is maintained tightly around $¼V_{dc}$, while with standard multilevel SPWM without third harmonic injection, capacitor voltage balancing fails. This is due to insufficient energy around the '0' voltage level that can be manipulated, as in this modulation index range $Q(¾V_{dc})=0$ and $|Q(¼V_{dc})|>>|Q(0)|$. Injection of the third harmonic minimizes capacitor voltage imbalance by extending the balancing region around the '0' voltage level. Capacitor voltage drift from $¼V_{dc}$ is within 2.5V (Figure 5-27d), compared to 25V in Figure 5-27d with SPWM. As a consequence of capacitor voltage imbalance the converter generated voltage and current waveforms in this modulation index range deteriorate significantly, as shown in Figure 5-27a through Figure 5-27c.



(a) Phase voltage. (b) Line voltage.

(c) Phase current waveforms. (d) Votage across the H-bridge floating capacitors.

Figure 5-26: Waveforms demonstrating operation of hybrid cascaded voltage source multilevel converter at low modulation index and H-bridge with unequal cell capacitor initial voltages (modulation index m=0.6 and load power factor=0.98 lagging).



(a) Phase voltage. (b) Line voltage.

(c) Phase current waveforms. (d) Voltage across the H-bridge floating capacitors.

Figure 5-27: Waveforms illustrating operational limitation of hybrid cascaded voltage source multilevel converter at low modulation index (with SPWM without proposed modification) and unequal H-bridge cell capacitors initial voltages (modulation index *m=0.6* and load power factor=0.98 lagging).

5.6 Experimental Validation

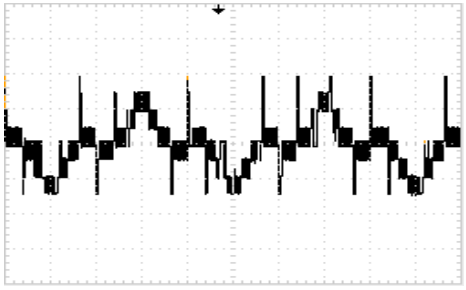
5.6.1 Independent control using SHE-PWM and high-frequency PWM

This section provides experimental validation of the analysis and simulation results presented. Practical results from two prototypes are presented: a single-phase seven-level hybrid multilevel converter with two ac side cascaded H-bridge cells (see in Appendix A.1.2) and a three-phase hybrid multilevel converter with two ac side cascaded H-bridge cells (see Appendix A.1.3).

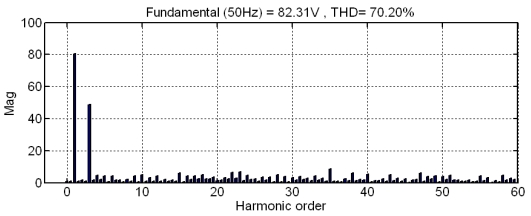
5.6.1.1 Single-phase experiment results

The dc link voltage of the main two-level converter stage is 200V and each H-bridge cell supports 50V, with 1mF capacitance. The H-bridge cells are controlled using 4kHz multilevel SPWM, as in the simulations. (Such a high switching frequency is selected to facilitate demonstration of the concept with a reduced number of cells). The main two-level converter stage is controlled using SHE-PWM, and only sets the fundamental voltage magnitude, as previously described. An Infineon Technology Tri-core microcontroller TC1796 is used to implement the modulation and capacitor voltage balancing strategy.

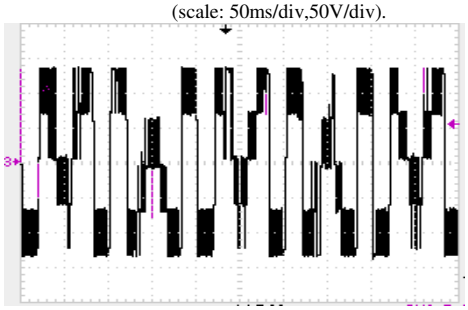
Figure 5-28 shows the results at 0.63 modulation index and 0.87 load power factor lagging. Figure 5-28a and Figure 5-28b show the phase voltage relative to the supply mid-point and its spectrum. As shown in Figure 5-28a, the hybrid converter with only two cascaded H-bridge cells produces seven voltage levels per phase. Transitions are generally restricted to one voltage level per switching cycle, although this is violated during H-bridge cell transitions between $½V_{dc}$ and $–½V_{dc}$. The spike widths appearing in the converter output voltage are wider than those shown in the simulations. This is due to the insertion of dead time that aggravates synchronization between switching the H-bridge cells and the two-level converter stage, and to the difficulty the H-bridge cells experience in tracking the step ends in the reference voltage. Figure 5-28c and Figure 5-28d show the voltage waveform across the H-bridge cells and its spectrum. Figure 5-28c shows that the H-bridge cells attempt to track the H-bridge reference provided by the modulator. The spectrum of the voltage across H-bridge cells contains a small fundamental component associate with the active power required to maintain the H-bridge cell capacitor voltages around the set point and to compensate for semiconductor losses.



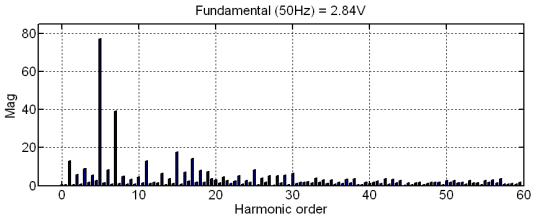
a) Phase voltage referred to supply mid-point (scale: 50ms/div,50V/div).



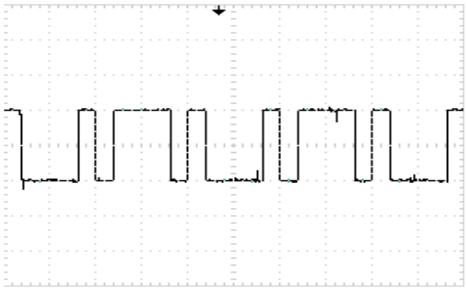
b) Phase voltage referred to supply mid-point spectrum



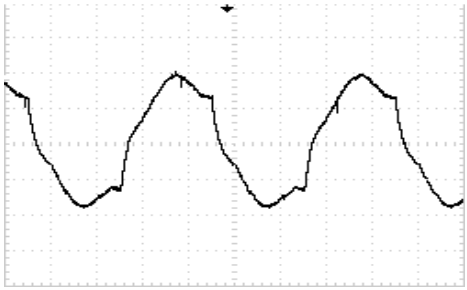
c) Voltage across H-bridge scale: (50ms/div, 20V/div).



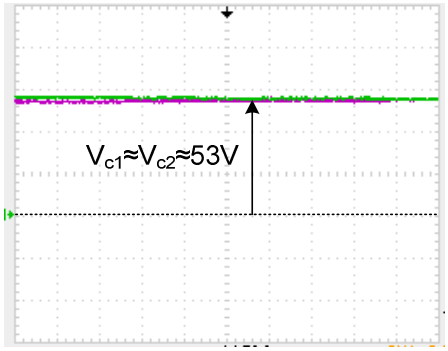
d) Voltage across H-bridge spectrum



(e) Main bridge output voltage scale: (50ms/div, 100V/div)



f) Phase current scale: (50ms/div, 2.5A/div)



g) Capacitor voltage Scale: (50ms/div, 20V/div)

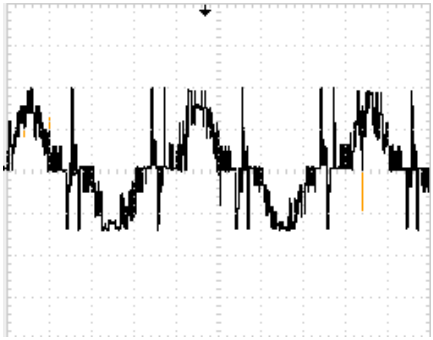
Figure 5-28: Experimental waveforms for the hybrid multilevel converter of Figure 5-1, with 200V dc link voltage, and operating at 0.87 power factor lagging and 0.63 modulation index.

Figure 5-28e shows the two-level converter output voltage referred to the supply mid-point. The phase current shown in Figure 5-28f is not a pure sinusoid, because it contains a significant third harmonic component inherited from the phase voltage

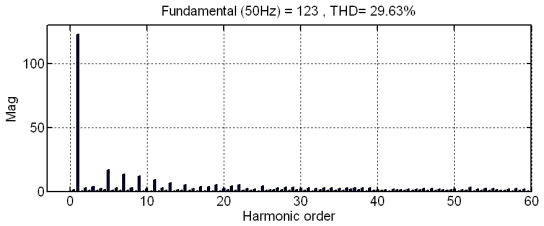
shown in Figure 5-28a and Figure 5-28b. The spikes in the phase voltage also contribute to phase current distortion. Figure 5-28g shows the H-bridge capacitor voltages are maintained slightly above 50V set point.

The results presented in Figure 5-29 are for the prototype hybrid converter operating with a 0.95 modulation index and 0.87 power factor lagging. Figure 5-29a shows that the hybrid converter with only two cascaded H-bridge cells produces nine voltage levels per phase. This is achieved because the third harmonic subtraction maximizes the use of the H-bridge cells without creating capacitor voltage imbalance. From the phase voltage spectra of Figure 5-29b and Figure 5-29d, a high modulation index is achieved when the harmonic energy in the H-bridge cell voltage is concentrated at the third harmonic in order to improve utilization of the H-bridge. Figure 5-29e shows the voltage waveform at the two-level converter output referred to supply mid-point, and Figure 5-29f shows phase current. The voltages across the H-bridge cell capacitors are maintained around 50V.

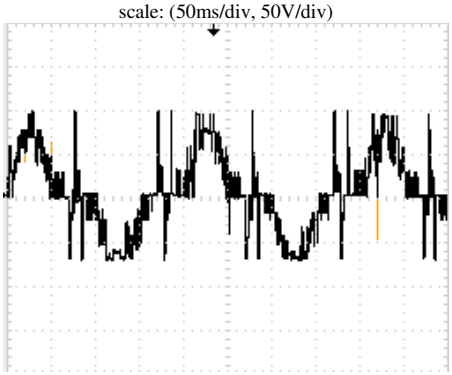
Figure 5-30 shows the results when the hybrid converter is operated at a modulation index m=0.91 and unity load power factor. The converter load power factor variation does not significantly affect converter operation or voltage stress on the H-bridge cell switches. The results in Figure 5-28, Figure 5-29 and Figure 5-30 confirm that the HCMC is able to operate independently of load power factor and modulation index.



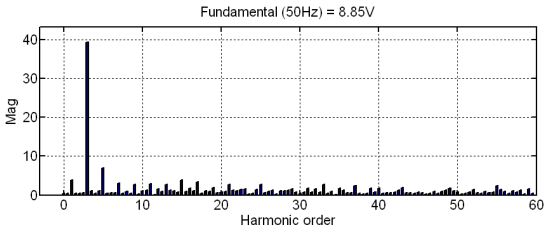
a) Phase voltage referred to supply mid-point
scale: (50ms/div, 50V/div)



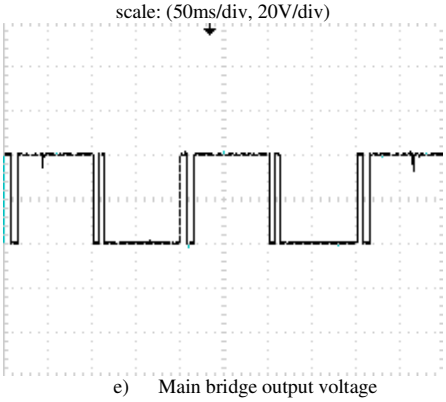
b) Phase voltage referred to supply mid-point spectrum



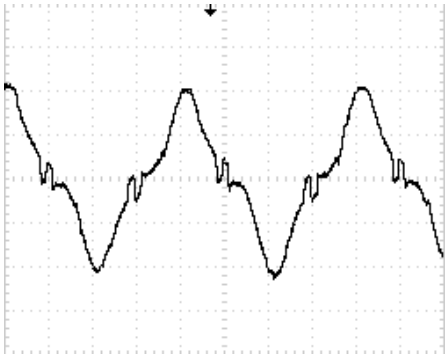
c) Voltage across H-bridge
scale: (50ms/div, 20V/div)



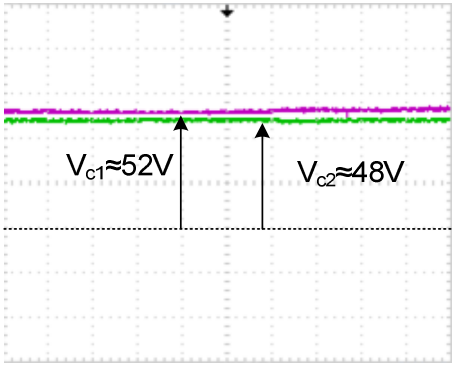
d) Voltage across H-bridge spectrum



e) Main bridge output voltage
scale: (50ms/div, 100V/div)

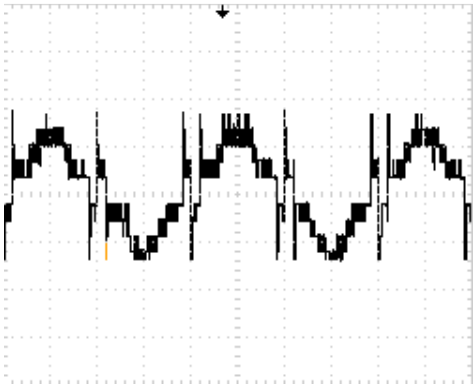


f) Phase current
scale: (50ms/div, 2.5A/div)

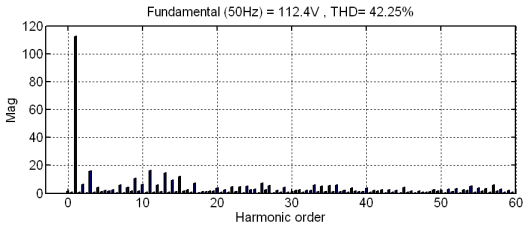


g) Capacitor voltage
scale: (50ms/div-, 20V/div).

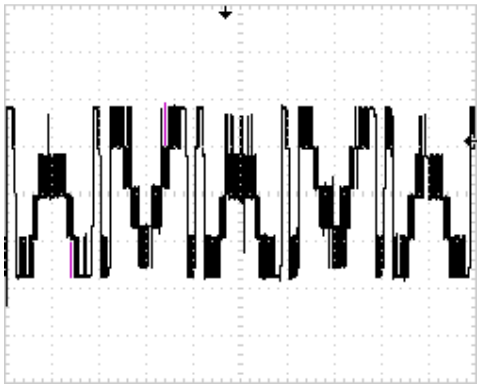
Figure 5-29: Experimental waveforms for the hybrid multilevel converter of Figure 5-1, with 200V dc link voltage, and operating at 0.87 power factor lagging and 0.95 modulation index.



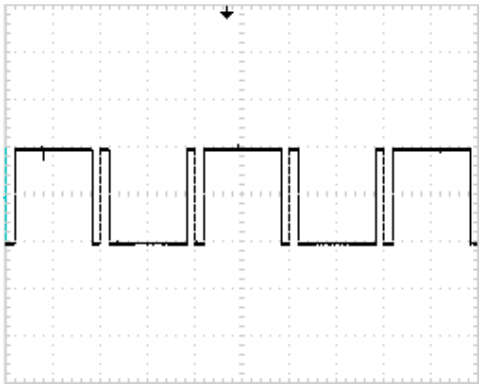
a) Phase voltage referred to supply mid-point.
scale: (50ms/div, 50V/div)



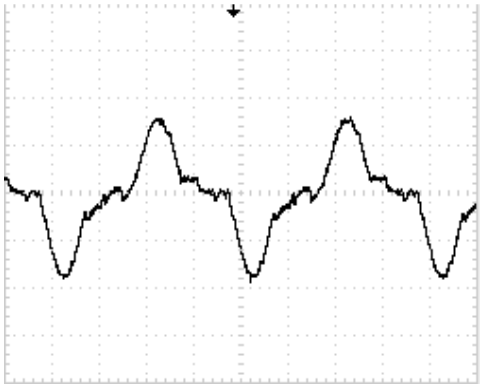
b) Phase voltage referred to supply mid-point spectrum



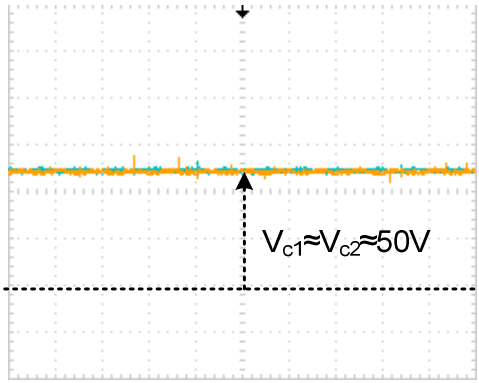
c) Voltage across H-bridge
scale: (50ms/div, 50V/div)



d) Main bridge output voltage
scale: (50ms/div, 100V/div)



e) Phase current
scale: (50ms/div, 2.5A/div)



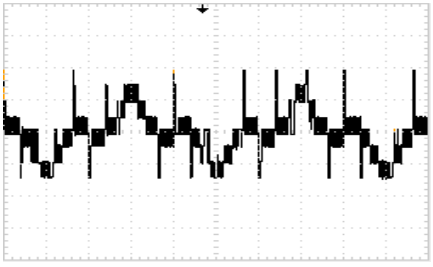
f) Capacitor voltage
scale: (50ms/div, 20V/div)

Figure 5-30: Experiment waveforms for the hybrid multilevel converter in Figure 5-1, with 200V dc link voltage, operating at unity power factor and 0.91 modulation index.

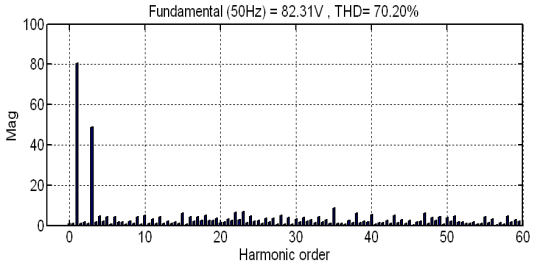
5.6.1.2 Three-phase experiment results

In order to show that the presented modulation strategy extends the modulation index linear range of the HCMC beyond the usual range of 0 to 1.15 with possible space vector modulation and conventional third harmonic injection, experimental results obtained at 0.8, 1.15 and 1.20 modulation indices and different load power factors are presented. The dc link voltage of the main two-level converter stage is 200V and each H-bridge cell supports 50V, with 3.3mF capacitance. The H-bridge cells are controlled using 4kHz multilevel SPWM.

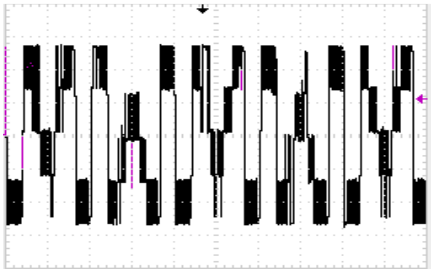
Figure 5-31 shows the results when a prototype hybrid converter (see Appendix A.1.3) is operated at 0.8 modulation index and 0.9 load power factor lagging. Figure 5-31a and Figure 5-31b present phase voltage relative to supply mid-point and its spectrum. Figure 5-31b shows that the hybrid converter with only two cascaded H-bridge cells produces seven voltage levels per phase. Transitions are generally restricted to one voltage level per switching cycle, although this is violated during H-bridge cell transitions between $\frac{1}{2}V_{dc}$ and $-\frac{1}{2}V_{dc}$. Also the width of the spikes that appear in the converter output voltage are wider than those shown in the simulations. This is due to the insertion of the dead time that aggravates synchronization between switching the H-bridge cells and the two-level converter stage, and is also due to the difficulty the H-bridge cells experience in tracking step ends in the reference voltage provided by modulator. Figure 5-31c and Figure 5-31d show the voltage waveform across the H-bridge cells and its spectrum. Figure 5-31c shows that the H-bridge cells attempt to track the H-bridge reference provided by the modulator. Also the spectrum of the voltage across H-bridge cells contains a small fundamental component that is associated with the active power required for maintaining the H-bridge cell capacitor voltage at the desired set point and to compensate for semiconductor losses. Figure 5-31e shows the two-level converter output voltage referred to supply mid-point. Figure 5-31f shows that the H-bridge capacitor voltages are maintained slightly above desired set point of 50V. The line voltage and its spectrum presented in Figure 5-31g and Figure 5-31h, show that there is no third harmonic component in the line voltage since it is cancelled by the 3-line system connection.



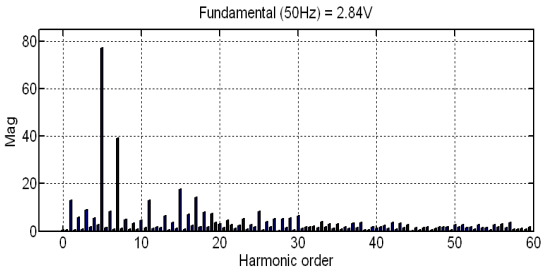
a) Phase voltage referred to supply mid-point
scale: (50ms/Div, 50V/Div)



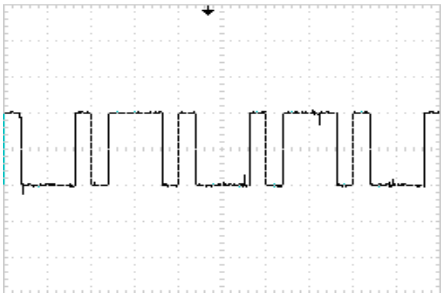
b) Phase voltage referred to supply mid-point spectrum



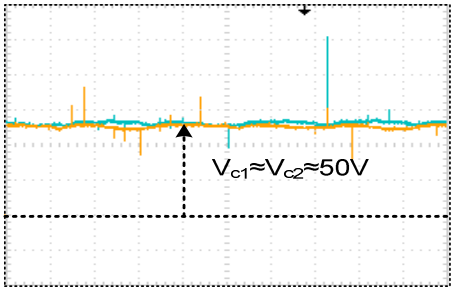
c) Voltage across H-bridge
scale: (50ms/Div, 20V/Div)



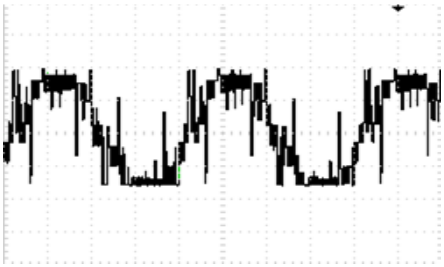
d) Voltage across H-bridge spectrum



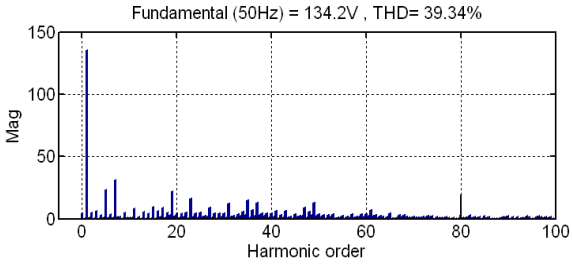
e) Main bridge output voltage
scale: (50ms/Div, 100V/Div)



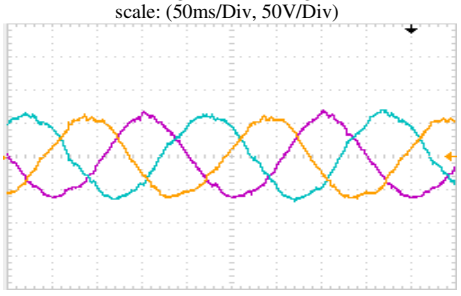
f) Capacitor Voltage
scale: (50ms/Div, 20V/Div)



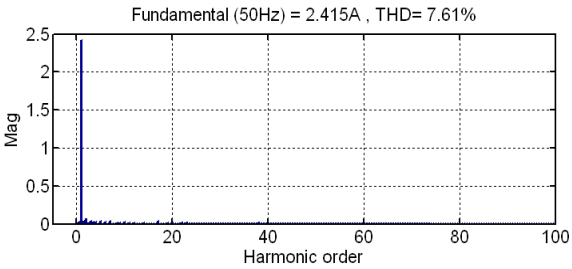
g) Line voltage
scale: (50ms/Div, 50V/Div)



h) Spectrum of line voltage

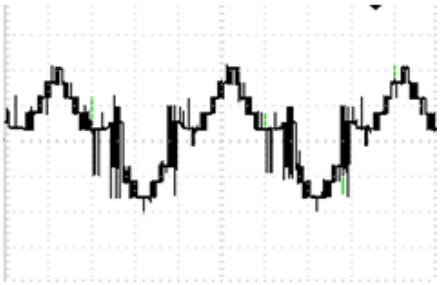


i) Three-phase current
scale: (50ms/Div, 2.5A/Div)

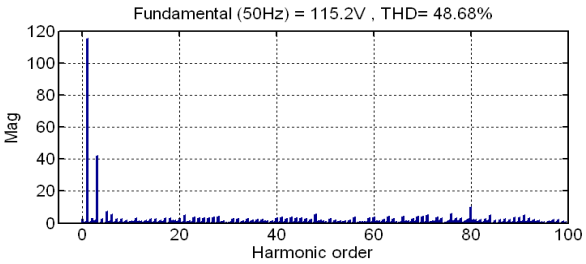


j) Phase current spectrum

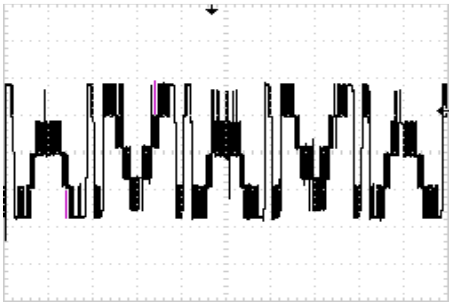
Figure 5-31: Experimental waveforms for the hybrid multilevel converter with 200V dc link voltage, and operating at 0.9 power factor lagging and 0.8 modulation index.



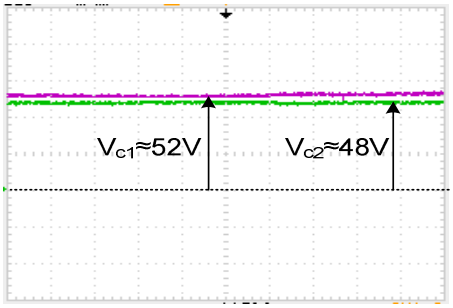
a) Phase voltage referred to supply mid-point
scale: (50ms/Div, 50V/Div)



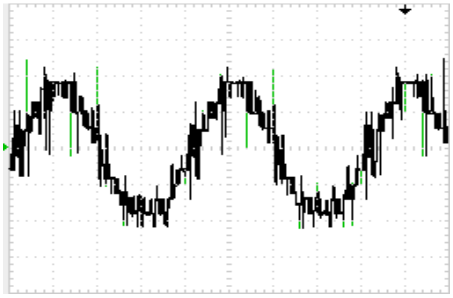
b) Phase voltage referred to supply mid-point spectrum



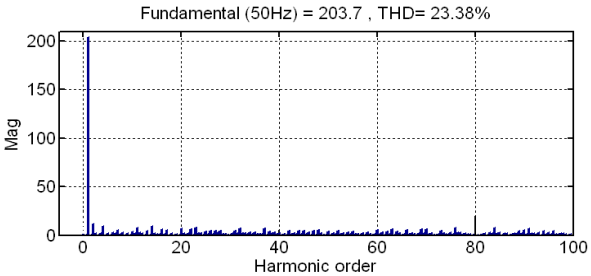
c) Voltage across H-bridge
scale: (50ms/Div, 50V/Div)



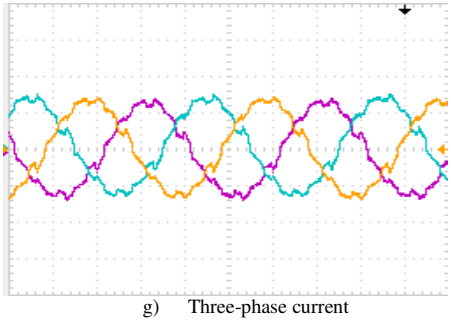
d) Capacitor voltage
scale: (50ms/Div, 20V/Div)



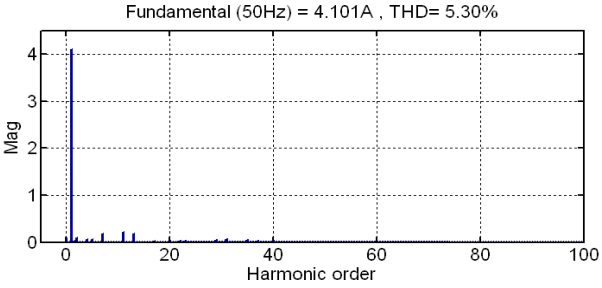
e) Line voltage
Scale: (50ms/Div-x-axis, 100V/Div-y-axis)



f) Line voltage spectrum

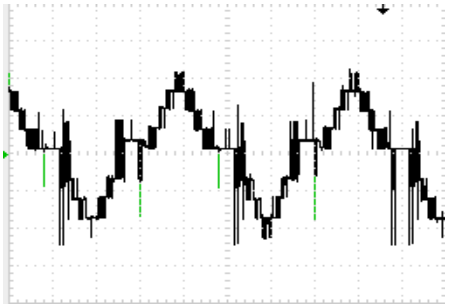


g) Three-phase current
scale: (50ms/Div, 2.5AV/Div)

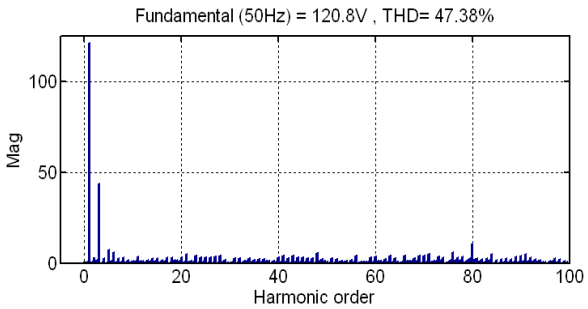


h) Current spectrum

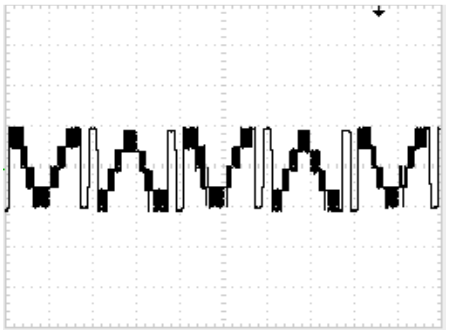
Figure 5-32: Experimental waveforms for the hybrid multilevel converter with 200V dc link voltage, and operating at unity power factor and 1.15 modulation index.



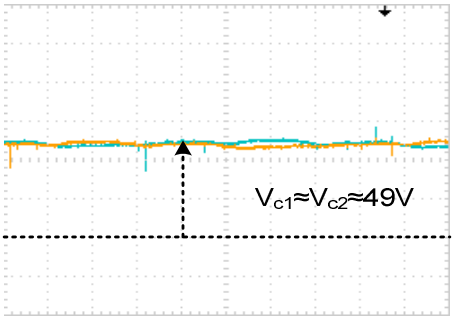
a) Phase voltage referred to supply mid-point
scale: (50ms/Div, 50V/Div)



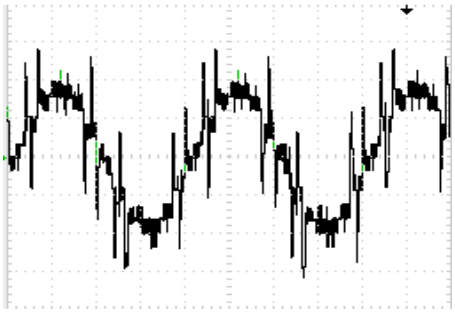
b) Phase voltage referred to supply mid-point spectrum



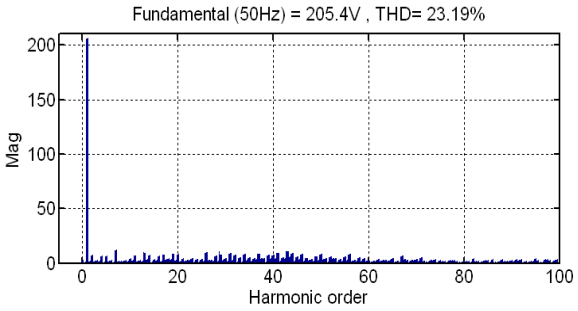
c) Voltage across H-bridge
scale: (50ms/Div, 20V/Div)



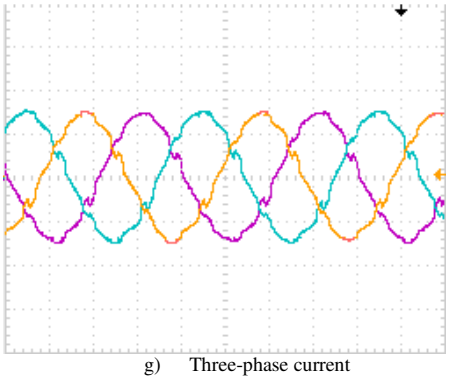
d) Capacitor Voltage
scale: (50ms/Div, 20V/Div)



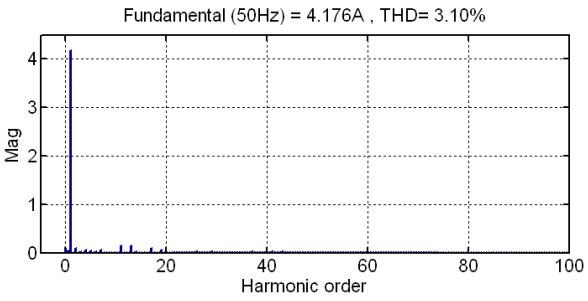
e) Line voltage
scale: (50ms/Div, 100V/Div)



f) Spectrum of line voltage



g) Three-phase current
scale: (50ms/Div, 2.5A/Div)



h) Current spectrum

Figure 5-33: Experimental waveforms for hybrid multilevel converter with 200V dc link voltage, and operating at 0.87 power factor lagging and 1.2 modulation index.

The results shown in Figure 5-32 are for the prototype hybrid converter is operated with 1.15 modulation index and unit power factor and Figure 5-33 is when the converter operates with 1.2 modulation index and 0.87 power factor lagging.

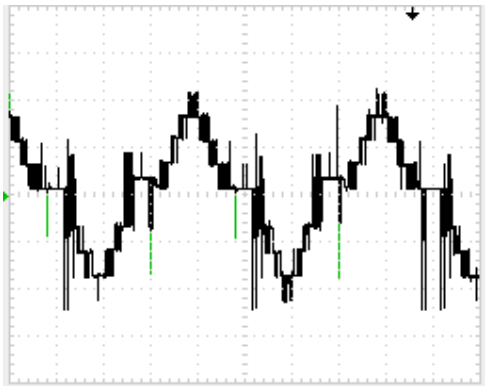
Figure 5-32a shows that the hybrid converter with only two cascaded H-bridge cells produces nine voltage levels per phase. This is achieved when the third harmonic subtraction maximizes the use of the H-bridge cells without creating a capacitor voltage imbalance. Based on Figure 5-31, Figure 5-32 and Figure 5-33, variation of the load power factor does not significantly affect converter operation or the voltage stress on the H-bridge cell switches. These figures confirm that the HCMC is able to operate independently of load power factor and modulation index. The small amount of low order harmonics in the three-phase current is due to low number of H-bridge cells in the test prototype. Current quality is improved if the number of H-bridge cells is increased.

5.6.2 SPWM with 3rd harmonic subtraction

To validate the extension of the modulation index linear range of the hybrid multilevel converter in real power applications, a prototype three-phase hybrid cascaded converter (see Appendix A.1.3) is used with a 200V dc link voltage and two cells per phase. Each floating cell capacitor blocks 50V with 3.3mF electrolytic capacitance per cell. The carrier frequency is 4kHz. The HCMC is controlled using carrier based PWM with extended balancing regions around the zero voltage level. This is to avoid synchronization issues that may arise if the high-voltage stage (two-level converter) and low-voltage stage (H-bridge cells) are controlled independently. A 32-bit Tri-core TC1796B microcontroller with floating point capability is used to implemented with the proposed modulation and capacitor voltage balancing strategies.

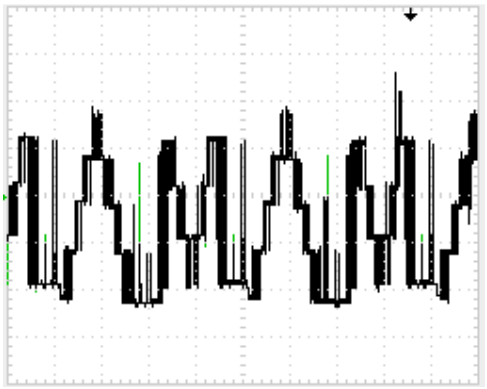
Figure 5-34 shows the results when the prototype (see Appendix A.1.3) is operated with a 1.15 modulation index and 0.9 power factor lagging. The phase voltage relative to ground ‘0’ contains spikes when the output phase is switching between ‘0’ and $\pm\frac{1}{4}V_{dc}$ voltage levels. This is because transitions from ‘0’ to these voltage levels sometimes necessitate switching of more voltage levels, depending on the state of

charge of the H-bridge cell capacitors and switch state used to achieve the '0' voltage level. For example, if the '0' voltage level is achieved using state $½V_{dc}$-V_{c1}-V_{c2}, switching to the -¼V_{dc} voltage level necessitates switching of the dc link voltage of the two-level converter and several voltage levels in the H-bridge cells; this can be observed in Figure 5-34c and Figure 5-34d. Comparing with the 150Hz switching frequency of the two-level converter using independent control, two-level converter switching frequency using standard SPWM is higher, and may result in switching loss increases. The dead time between the complementary switches in the two-level converter stage and H-bridge cells is another factor that influences the magnitude and width of these output voltage spikes (a 2μs dead time has been used). In this converter topology, dead time prevents smooth transition between voltage levels during switching of more than one voltage level, as each switching device required finite time to change its state. Figure 5-34a and Figure 5-34b show that when the converter switch states are fully utilized, the hybrid cascaded converter with two cells per arm generates 9 and 17 voltage levels in the phase and line voltages respectively. Therefore it is expected to generate high quality output voltage with a low number of cascaded H-bridge cells. Figure 5-34d shows that with the proposed reference voltage that utilizes third harmonic subtraction, the two-level converter stage switches between $½V_{dc}$ and -$½V_{dc}$ only when the converter phase output voltage is switching between '0' and ±¼V_{dc}. These switching actions are necessary in order to balance the H-bridge cell capacitors as explained in the Section 5.3.2. Figure 5-34e shows that the voltage across the H-bridge cell floating capacitors of the phase 'a' is maintained at ±¼V_{dc} (50V) as expected, despite the converter being operated at a high modulation index of 1.15 and 0.9 power factor lagging. This result confirms the viability of the proposed approach in extending the modulation index range when the hybrid cascaded converter is used in real power applications, without the need to increase the number of H-bridge cascaded cells. Figure 5-34f shows the current waveforms are sinusoidal despite the spikes shown in the phase and line voltages in Figure 5-34a and Figure 5-34b.

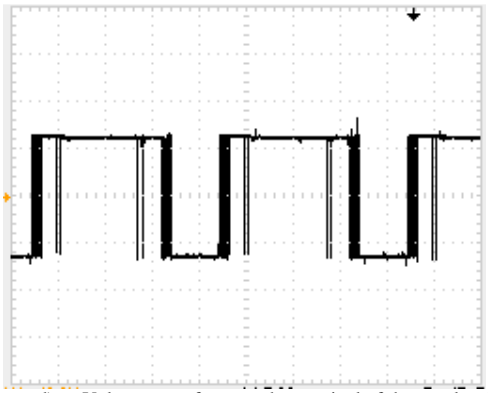


a) Phase voltage relative to supply mid-point
scale: (50ms/Div, 50V/Div)

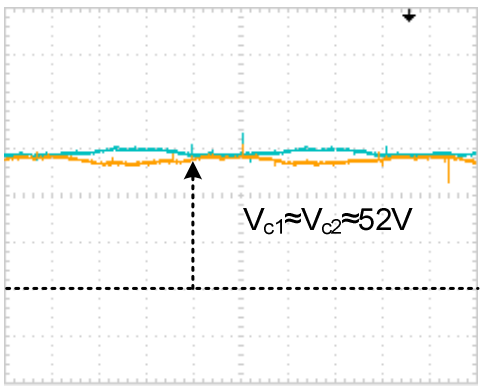
b) Line voltage
scale:(50ms/Div, 50V/Div)



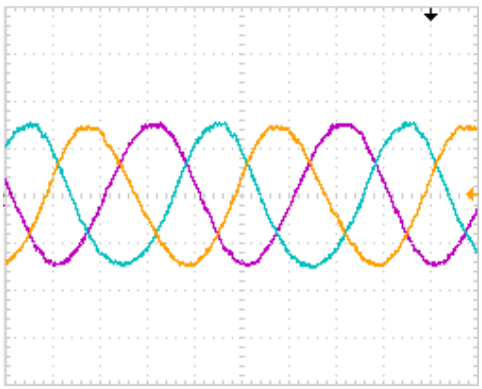
c) Total voltage across two H-bridge cells of the phase A (output phase a relative to m)
scale: (50ms/Div, 50V/Div)



d) Voltage waveforms at the terminal of the two-level converter relative to supply mid-point
scale: (50ms/Div, 100V/Div)



e) Voltage across capacitors of the phase A
scale: (50ms/Div, 20V/Div)

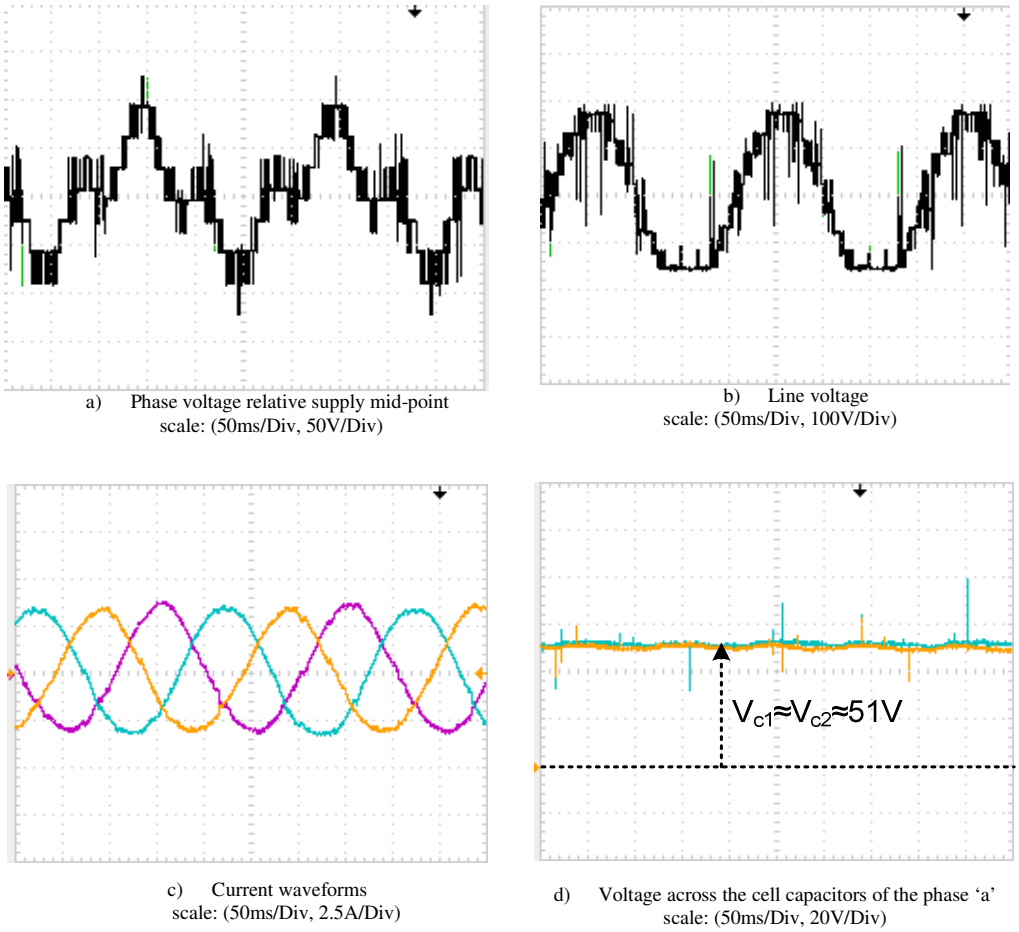


f) Current waveforms
scale: (50ms/Div, 2.5A/Div)

Figure 5-34: Experimental waveforms illustrating the performance of the hybrid cascaded multilevel converter with two cells per phase when operated at m=1.15 and 0.9 power factor lagging.

For further demonstration of the ability of the HCMC to operate independently of modulation index and load power factor, the converter is operated with unity modulation and near unity load power factor.

Figure 5-35a to d show phase and line voltage, phase current, and voltage across the cell capacitors. The system is able to operate with voltage stress on the switching devices maintained tightly, as the voltages across the floating cell capacitors are maintained at ¼V_{dc}.



a) Phase voltage relative supply mid-point
scale: (50ms/Div, 50V/Div)

b) Line voltage
scale: (50ms/Div, 100V/Div)

c) Current waveforms
scale: (50ms/Div, 2.5A/Div)

d) Voltage across the cell capacitors of the phase 'a'
scale: (50ms/Div, 20V/Div)

Figure 5-35: Experimental waveforms illustrating the hybrid cascaded converter operating with unity modulation index and power factor approaching unity (0.98 power factor lagging)

5.7 Comparison

- Modulation strategy

Two modulation strategies have been applied to the HCMC. By using SHE-PWM in the two-level converter and standard PWM in the H-bridge cells, a low switching frequency in the two-level converter and a reduction in H-bridge cell number are achieved, However, spikes appear in the phase and line-to-line voltages, which means a low order harmonic filter will be required before connection to the grid. By using standard SPWM with 3rd harmonic subtraction, improved line-to-line voltage without spikes is achieved, but incurs a trade-off between increased switching frequency of two-level converter and the improved line voltage quality.

- Hardware implementation

Since two different switching frequencies are used to independently control the two-level converter and the H-bridge cells, synchronisation issues arise. During experimentation, MATLAB embedded code was used in a DSP to generate control signals for the IGBTs. By extracting the signals generated for the upper IGBTs of the two-level converter in order to control the series cells, rather than using the two-level converter output voltage reduces synchronisation time delay. The remaining delay still compromises performance. This issue was accounted for by increasing the switching frequency of the H-bridge cells to 4kHz, which reduces the time difference between switching of the two-level converter and the H-bridge cells. This is at the expense of increased system conversion losses. This issue disappears with the system using SPWM with 3rd harmonic subtraction, since the two-level converter and the H-bridge cells are treated as single unit.

5.8 Summary

This chapter presented two new operational principles and modulation strategies that permit a hybrid multilevel converter with ac side cascaded H-bridge cells to operate independently of modulation index and load power factor, with an extended modulation index linear range and a reduced number of H-bridge cells. The validity of the presented modulation and capacitor voltage balancing strategies were confirmed by simulation and experimentally. Scalability of the hybrid converter to

high-voltage applications was also investigated. Some of the key features of the proposed modulation and capacitor voltage balancing method are summarized as follows:

- The positive and negative peaks of the H-bridge cell reference voltage is suppressed to between 1 and -1, hence reducing the required number of H-bridge cells such that the sum of their voltages must equal ½V_{dc}. This means the number of cell capacitors reduces to one quarter of that required with the modular multilevel converter. As a result the hybrid multilevel converter that uses the presented modulation and capacitor voltage strategy is expected to have a smaller footprint.
- The modulation index linear range is extended. This allows the HCMC to have a higher power density than any known multilevel converter topology discussed in the literature for the same dc link voltage and switching device rating. This feature can be used to lower converter semiconductor losses in applications that use an interfacing transformer by raising the ac voltage at the converter side, hence lowering the current flow in the converter switches.
- The methods are scalable, without significant difficulty, for application to converters with a large number of H-bridge cells. In the case of a three-phase converter with a large number of cells, it produces near sinusoidal voltage at the converter output as demonstrated in the Simulation section. In this case, the current loading on the cell capacitors is significant reduced due to the absence of the harmonic currents associated with the third harmonic and its multiples. This allows the use of small cell capacitors without increasing capacitor voltage ripple.

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CHAPTER 6

6 Switching and Conduction Losses

6.1 Introduction

In the design stage of any power converter, estimation of switching device electrical loadings and power losses provide useful information regarding device ratings, thermal circuit sizing, and conversion efficiency. Therefore, this chapter evaluates the power loss performance of the main two converter topologies investigated in this thesis, namely, the modular multilevel converter (M2C) and the hybrid cascaded multilevel converter (HCMC). Several methods for power converter loss estimation have been reported in the literature [1]. The most direct method for quantifying conversion on-state and switching losses is to measure the voltage drop across and current flowing through the power semiconductor switches. This is difficult to accomplish for multilevel converters due to large number of power devices normally used in these topologies, and their accessibility. Additionally, a large number of high bandwidth voltage and current probes may be necessary to measure the fast switching transitions of the power semiconductors. Considering the number of probes and the fast sample rate required, it would not be feasible to simultaneously record all of the data for even one cycle of operation. Other methods for loss estimation are based on heat measurement with calorimeters. However, these methods measure overall losses, and are not directly based on experiments making it difficult to match exactly same the operating conditions (especially semiconductor temperatures) when evaluating the different methods. Hence, purely experimental results are not completely useful for a fair comparison. Other methods based on a hybrid combination of simulation and experimental measurement, theoretical models and data sheet information have been reported in [2, 3]. Such methods are more suitable for this task, especially for a multilevel converter. Using a simulation basis, they can be easily applied to multilevel converters, without the increasing the difficulties introduced by the number of semiconductors and high bandwidth probes.

The loss calculation method that samples the discontinuous current within a switching cycle T_s, and transforms this into a continuous microscopic average or root mean square signal presented in [4, 5] is used within this chapter. This approach is applicable when the switching frequency is much higher than the fundamental frequency, since the current shape within one switching period can be considered linear without significantly sacrificing calculation accuracy.

Self-commutated power devices such as the IGBT have two main power loss mechanisms, conduction and switching losses [6-9]. Diode losses are predominately the sum of conduction and recovery losses. A systematic derivation of conduction and switching losses will be conducted for the standard two-level converter, and the three-level modular converter, and then extended to the modular converter and the hybrid cascaded converter with a large number of levels.

6.2 Conduction loss modelling

Conduction losses are those that occur while the power device is in the conduction on-state. Due to the voltage drop across switching devices, power dissipation during conduction is computed by multiplying the on-state saturation voltage by the on-state current:

$$P = V_{on} \cdot i_o \tag{6.1}$$

The device voltage is a function of the current [4, 7, 10-12], and can be expressed by:

$$V_{on} = R_{on} \cdot i_o + V_{fo} \tag{6.2}$$

Where R_{on} is the forward resistance of the device.

i_o is the output load current.

V_{fo} is the forward voltage drop across the device with no load.

In an inverter, if the frequency ratio is bigger then 15, the output current can be assumed to be sinusoidal:

$$i_o(t) = I_o \cdot \sin(\omega t - \varphi) \tag{6.3}$$

Where: φ is the power factor angel between current and voltage.

For a power switching device, the typical voltage/current (V_{CE}/I_{CE}) graph shown in Figure 6-1 is approximated by linearizing the forward resistance of the devices

obtained from output characteristics such as those shown in Figure 6-2:

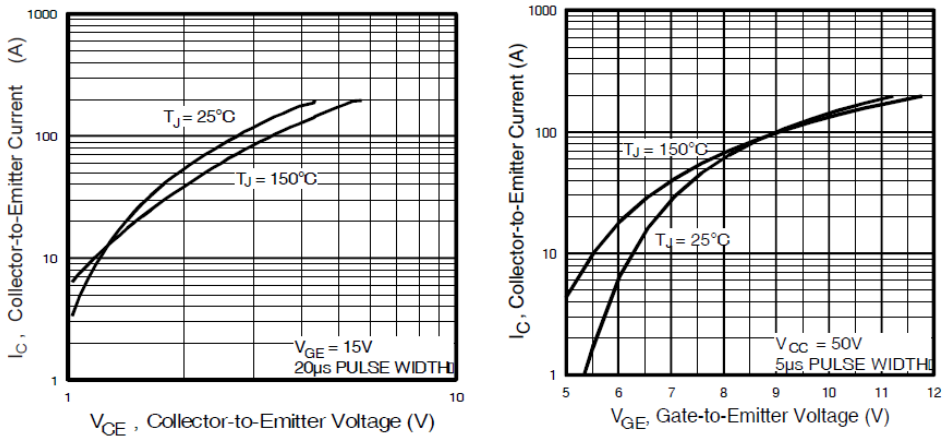

Figure 6-1: Typical output characteristics for an IRG4PC40FDPbF IGBT [14].

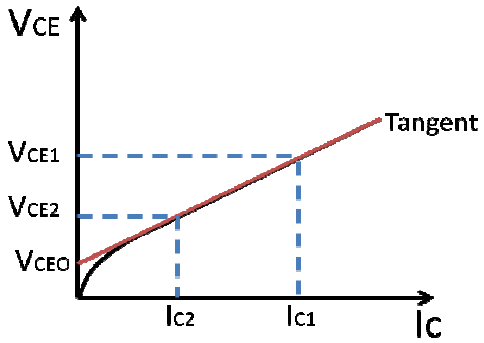

Figure 6-2: Estimation of IGBT forward resistance from the output characteristics.

The values of R_{on} can be obtained from the output characteristics shown in Figure 6-2 as follows:

$$R_{on} = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{V_{CE1} - V_{CE2}}{I_{C1} - I_{C2}} \tag{6.4}$$

Similarly, for a diode, conduction voltage also can be obtained from a simple linearization of the exact diode *V/I* characteristic:

$$V_D = R_D \cdot i_o + V_{D0} \tag{6.5}$$

Where V_{D0} is the voltage drop at rated current of the diode.

R_D is the forward resistance of the diode.

Calculation of V_{D0} and R_D is similar to the calculation of V_{fo} and R_{on}.

The conduction loss expression for a switching device is therefore calculated as:

$$P_c = \frac{1}{T}\int_0^T V_{on}(t)\cdot i_o(t)dt = \frac{1}{T}\int_0^T [V_{fo} + R_{on}\cdot i_o(t)]\cdot i_o(t)dt$$
$$= \frac{1}{T}\int_0^T V_{f0}\cdot i_o(t)dt + \frac{1}{T}\int_0^T R_{on}\cdot i_o^2(t)dt \qquad (6.6)$$
$$= V_{on}\cdot \overline{I_{av}} + R_{on}\cdot I_{rms}^2$$

Where T is the fundamental period and $\overline{I_{av}}$ and I_{rms}^2 are the average and *rms* values of current i_o in the switching device over one fundamental period.

The expression for the local average and *rms* currents within one switching period can be approximated as:

$$\overline{i_o} = \frac{1}{T_s}\int_0^{T_s} i_o(t)dt = d_0\cdot i_o(t) \qquad (6.7)$$

$$i_{rms}^2 = \frac{1}{T_s}\int_0^{T_s} i_o^2(t)dt = d_0\cdot i_o^2(t) \qquad (6.8)$$

Where d_o is the duty cycle of the switching device.

6.3 Switching loss modelling

Switching loss is the power dissipation during the power semiconductor device turn-on and turn-off switching transitions. The most accurate method of determining switching losses is to plot the current and voltage waveforms in the controllable switch during the switching transition, and they multiply the waveforms point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy at turn-on or turn-off. The diode can be considered as an ideal switch at turn-on, since it turns on rapidly compared to the controllable switch. The switching energy of a diode at turn-on can therefore be neglected. However, the switching energy at turn-off cannot be neglected, since the diode current reverses during the reverse-recovery time. Hence, the switching loss estimation method will consider IGBT turn-on and turn-off losses and diode turn-off losses [2, 4].

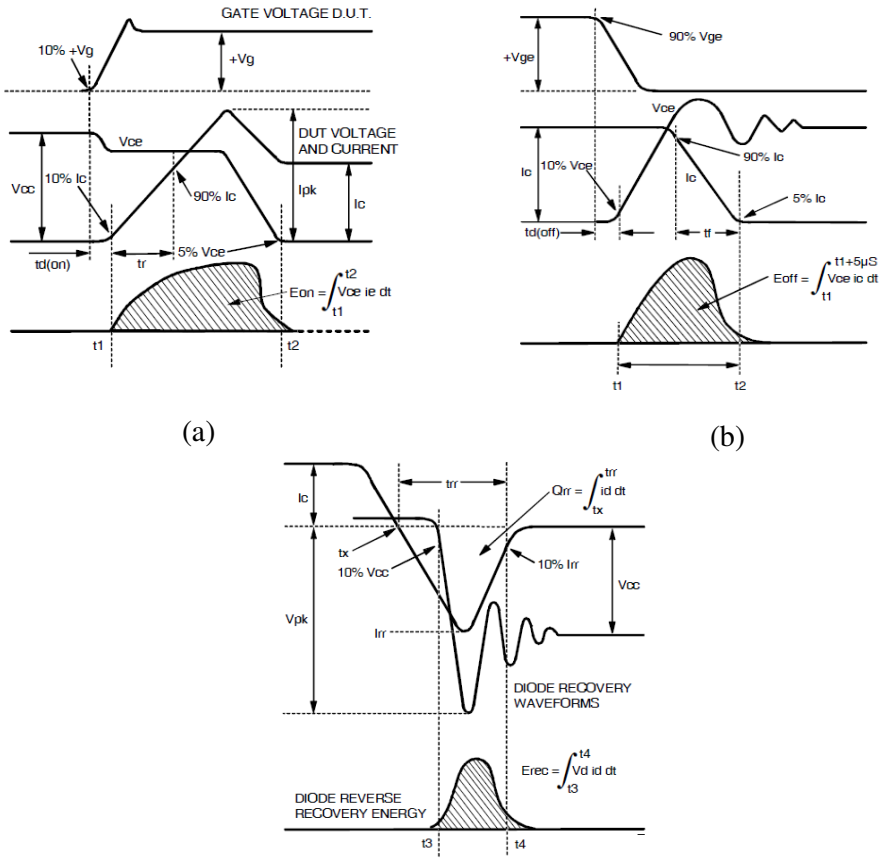

Figure 6-3: Hard switching characteristic a) IGBT turn-on b) IGBT turn-off c) Diode turn-off [2, 4].

In one inverter leg, during IGBT turn-on, as shown in Figure 6-3a, the current starts to increase, gradually transferring (commutating) the load current from the freewheeling diode to the IGBT (the opposite diode is turning off). When the current through the IGBT i_o reaches the load current I_{pk}, it continues to increase since the IGBT must provide the load current plus the reverse recovery current of the opposite diode. This increases power losses during turn-on.

During IGBT is turned off as shown in Figure 6-3b, the voltage across the IGBT increases until it reaches the dc link voltage V_{DC}. Then the opposite diode is forward biased and starts to conduct. The current through the IGBT decreased rapidly producing an overshoot in the collector-emitter voltage V_{CE} due to parasitic inductance. In addition, after the initial change in current, the current slope decreases due to the charges stored in the internal base of the BJT that part of the IGBT. This is referred to the tail section of the IGBT turn-off switching dynamics.

Finally, during diode turn-off as shown in Figure 6-3c, when the reverse recovery current returns from it negative peak value to zero, the voltage across the diode increases from the forward voltage to the blocking voltage.

The data sheets quote switching energies are for a certain reference voltage V_{ref} equal to the blocking state voltage of the IBGT prior to the corresponding commutation, and a reference current I_{ref} which is the on-state current [2, 4, 12].
The individual switching losses can therefore be expressed by:

$$P_{IBGT} = f_s \cdot (E_{on} + E_{off}) \cdot \frac{V_{dc}}{V_{ref}} \cdot \frac{i_o}{I_{ref}} \tag{6.9}$$

$$P_{diode} = f_s \cdot E_{rec} \cdot \frac{V_{dc}}{V_{ref}} \cdot \frac{i_o}{I_{ref}} \tag{6.10}$$

Finally, total switching losses can be expressed by:

$$P_{total} = f_s \cdot (E_{on} + E_{off} + E_{rec}) \cdot \frac{V_{dc}}{V_{ref}} \cdot \frac{i_o}{I_{ref}} \tag{6.11}$$

Where E_{on}, E_{off} and E_{rec} are the turn-on, turn-off energy for IGBT and reverse recovery energy for diode.

There are different methods for estimating switching losses. The most commonly used approach is to approximate the switching energy as a function of collector-emitter current [8]:

$$E_{switching} = k_1 i_o + k_2 \tag{6.12}$$

Where: k_1 *and* k_2 are the constant terms determined from the linearized switching energy graph given in a device datasheet, as shown in Figure 6-4.

Therefore the average switching loss for the multi-level inverter can be expressed by:

$$P_{switching} = \frac{f_s}{2\pi} \int_{\alpha}^{\beta} (k_1 \cdot i_0 + k_2) d\omega t \tag{6.13}$$

Where f_s is the switching frequency.

α, β are the angle switching device turn-on duration of one fundamental period provides limits of integration.

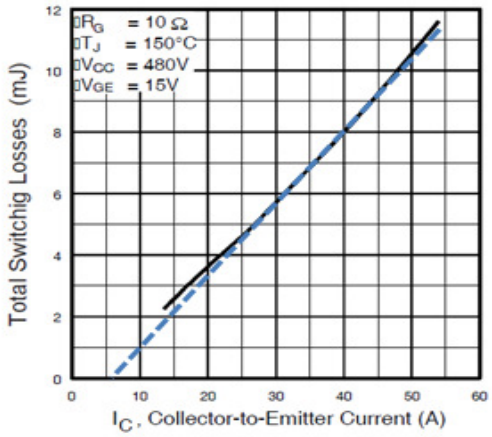

Figure 6-4: Linearized switching loss characteristic of an IRG4PC40FDPbFs IGBT versus Collector-Emitter Current.

6.4 Conduction and switching losses

The parameters used in calculating conduction and switching losses in the simulations of the two-level, M2C and HCMC are given in Table 6-1. For the two-level conventional converter, a 1.5kV blocking voltage gives a best fit linear characteristic for calculating conduction and switching losses. The number of series connected devices is 20kV/1.5kV=13.3, that is, 14 devices in series. For an *N*-level M2C, each cell is rated at $\frac{1}{N-1}V_{dc}$. For three-level, five-level and nine-level converters, the number of series connected devices in each cell is $\frac{20kV}{1.5kV(N-1)}$ where *N*=3,5,9. For the HCMC with two cells, seven cells and ten cells in the ac side, the number of series connected devices in the main bridge is the same as for the two-level conventional converter, which is $2\cdot 7$ per arm. For the ac side cells, in the two cell version, each cell should block 5kV which means 5kV/1.5kV=3.3 devices in series, i.e. 4 series connected IGBTs. In the seven and ten cell versions, no series connection is required with the cells.

All converter power losses are calculated under three different operating conditions:

(a) when the converter delivers 16MW at 11kV and a 0.8 power factor lagging.

(b) when the converter delivers 20MVAr at 11kV (pure reactive power only).

(c) when the converter delivers 20MW at 11kV and unity power factor (real power only).

The two-level converter, the M2C and the HCMC are simulated with a switching frequency of 1.35kHz. With multi-level converters, the switching frequency is defined as the number of times to the converter changes state, which is not the same as the switching frequency of each device.

Data for the FF400R33KF2C IGBT is used in the calculations. The forward resistance, typical forward voltage drop and the free-wheel diode total switching energy losses during turn-on and turn-off and reverse recovery losses where are obtained from the datasheet.

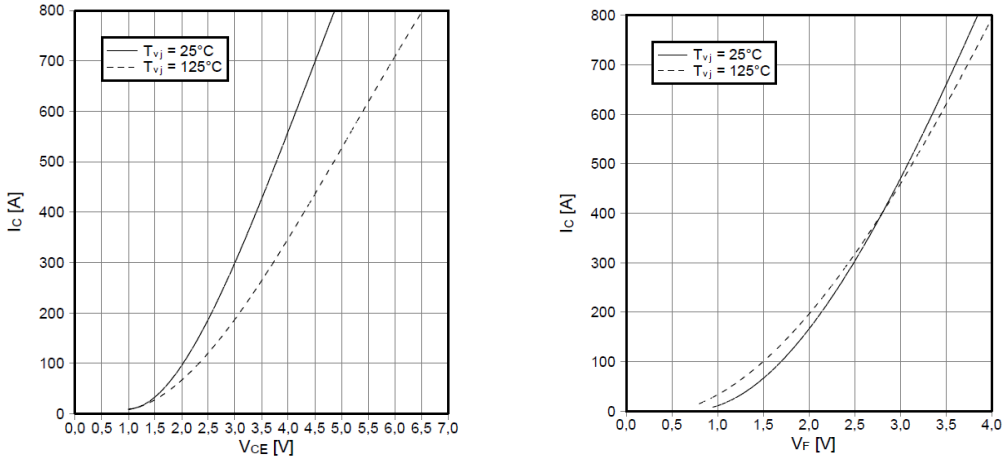

Figure 6-5: Typical FF400R33KF2C IGBT output characteristics [13].

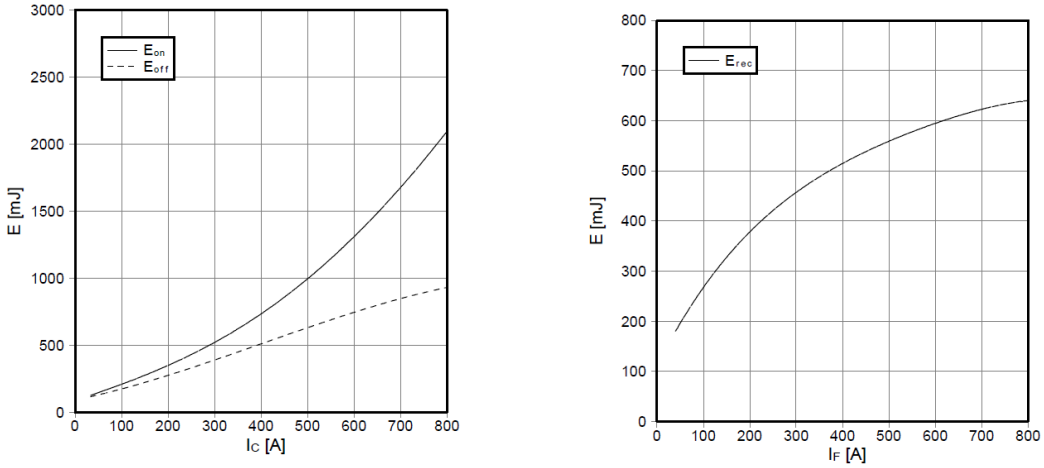

Figure 6-6: Typical FF400R33KF2C IGBT switching energy characteristics [13].

Table 6-1: Converter data used in simulation power loss estimation

DC link voltage	*20kV*	K_{I_on1}	*0.0016J/A*
		K_{I_on2}	*0.029J*
Converter rating	*20MVA*	K_{I_off1}	*0.0017J/A*
Carrier frequency	*1.35kHz*	K_{I_off2}	*0.35J*
R_{on}*(IGBT)*	*1.75mΩ*	K_{D_off1}	*0.0006J/A*
R_D*(diode)*	*1.64mΩ*	K_{D_off2}	*0.398J*
V_{f0}*(IGBT)*	*1.2V*	*Cell capacitor*	*2.2mF*
V_{D0}*(diode)*	*1.05V*	*IGBT rating*	*3.3kV*
Number of series devices per leg(two-level & HCMC main bridge)	*14*	*Number of series devices per cell (five-level M2C & HCMC with two cells in ac side)*	*4*
Number of series devices per cell (three-level M2C)	*7*	*Number of series devices per cell (nine-level M2C)*	*2*

6.4.1 Conventional two-level converter

- *Conduction losses*

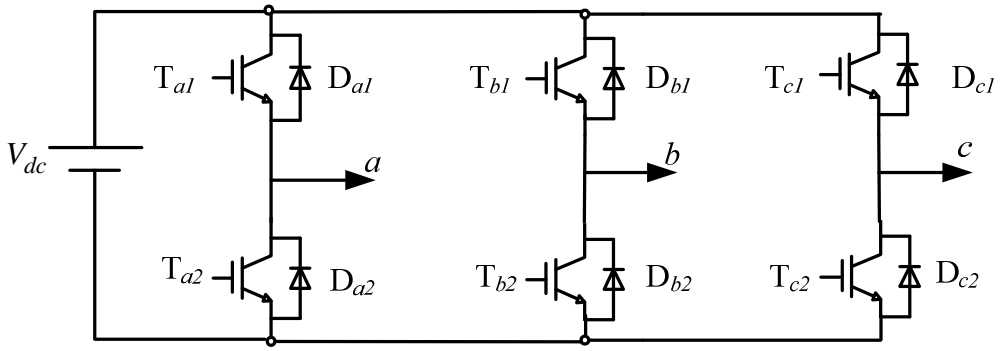

Figure 6-7: Conventional two-level converter.

Figure 6-7 shows a conventional two-level converter. The load current $i_a(t)$ and modulation waveform $v_a(t)$ of the phase *a* are defined as:

$$i_a(t) = I_o \sin(\omega t - \varphi) \tag{6.14}$$

$$v_a(t) = m \cdot \sin \omega t \tag{6.15}$$

The duty cycle of the switch T_{a1} is $d_{a1} = \frac{1}{2}(1 + m \sin \omega t)$ and the period during which it conducts current over the carrier period T_s is $d_{a1} \cdot T_s$. Switch T_{a2} conducts current for the period $(1 - d_{a1}) \cdot T_s$.

Current flow in switches T_{a1} and T_{a2} , and in their corresponding freewheel diodes devices D_{a1} and D_{a2} is defined by:

$$I_{Ta1,av} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} d_{a1} i_a d\omega = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} \frac{1}{2}[1+m\sin\omega t]\cdot I_o \sin(\omega t-\varphi) d\omega$$
$$= \frac{I_o}{8\pi}[4+\pi m\cos\varphi] \tag{6.16}$$

$$I^2_{Ta1,rms} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} d_{a1} i_a^2 d\omega = \frac{I_o^2}{24\pi}[3\pi+8m\cos\varphi] \tag{6.17}$$

$$I_{Da1,av} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} d_{a1} i_a d\omega = \frac{I_o}{8}[\pi m\cos\varphi-4] \tag{6.18}$$

$$I^2_{Da1,rms} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} d_{a1} i_a^2 d\omega = \frac{I_o^2}{24\pi}[3\pi-8m\cos\varphi] \tag{6.19}$$

$$I_{Ta2,av} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} (1-d_{a1}) i_a d\omega = -\frac{I_o}{8\pi}[4+\pi m\cos\varphi] \tag{6.20}$$

$$I^2_{Ta2,rms} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} (1-d_{a1}) i_a^2 d\omega = \frac{I_o^2}{24\pi}[3\pi+8m\cos\varphi] \tag{6.21}$$

$$I_{Da2,av} = -I_{Da1,av} \tag{6.22}$$

$$I^2_{Da2,rms} = I^2_{Da1,rms} \tag{6.23}$$

Therefore, based on equation (6.6) and equation (6.16) to (6.23), the total conduction losses for the IGBT and diode can be estimated as:

$$P_{conduction} = \begin{pmatrix} \frac{I_o^2}{24\pi}(3\pi+8m\cos\varphi)\cdot R_{on} + \frac{I_o}{8\pi}(4+\pi m\cos\varphi)\cdot V_{f0} + \\ \frac{I_o^2}{24\pi}(3\pi-8m\cos\varphi)\cdot R_D + \frac{I_o}{8\pi}(\pi m\cos\varphi-4)\cdot V_{D0} \end{pmatrix} \tag{6.24}$$

- *Switching losses*

For the two-level converter the IGBT switching losses are the sum of the turn-on and turn-off switching losses based on equation (6.13). Specifically:

$$P_{swithcing\_IGBT} = \frac{f_s}{4\pi}\int_{\varphi}^{\pi+\varphi} [(k_{I\_on1}+k_{I\_off1})\cdot I_o \sin(\omega t-\varphi)+k_{I\_on2}+k_{I\_off2}] d\omega t \tag{6.25}$$

$$= \frac{f_s \cdot (k_{I\_on1} + k_{I\_off1}) \cdot I_o}{2\pi} + \frac{f_s}{4}(k_{I\_on2} + k_{I\_off2})$$

The diode switching losses are predominantly recovery loss, which can be expressed as:

$$\begin{aligned} P_{switching\_diode} &= \frac{f_s}{4\pi} \int_{\varphi+\pi}^{2\pi+\varphi} [(k_{D\_off1} \cdot I_o \sin(\omega t - \varphi) + k_{D\_off2}] d\omega t \\ &= \frac{f_s \cdot k_{D\_off1} \cdot I_o}{2\pi} + \frac{f_s}{4} \cdot k_{D\_off2} \end{aligned} \tag{6.26}$$

Equations (6.25) and (6.26) assume sinusoidal load current with peak I_o, and that the carrier frequency is high compared to the fundamental frequency, this enables the current within a carrier period to be assumed constant.

Table 6-2 shows the conversion losses of the two-level converter under the three previously specified operating conditions.

Table 6-2: Summary of two-level conventional converter conversion losses.

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)
Conduction loss (kW)	124.3kW
Switching losses (kW)	270.8kW
Total conversion losses (kW)	395.1kW (1.97%)
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)
Conduction loss (kW)	122.6kW
Switching losses (kW)	270.3kW
Total conversion losses (kW)	393.4kW (1.96%)
Operating condition (c)	20MVA at 11kV and unity power factor
Conduction loss (kW)	126kW
Switching losses (kW)	270.8kW
Total conversion losses (kW)	396.8 kW (1.98%)

6.4.2 Modular Multilevel Converter (M2C) Conversion Loss

6.4.2.1 Three-level M2C

- *Conduction losses*

For the 3-level modular converter as shown in Figure 6-8 , the on-state duty cycle of each switching device over one period of output voltage is required to calculate the average conduction loss in the converter using carrier-based PWM. The conducting device depends on the switching state and the load current as shown in Table 6-3.

Table 6-3: summary of all the switch states and conduction devices.
1: switch on and 0: switch off.

Switching States				V_{ao}	Conducting devices	
S_{m1}	S_{m2}	S_{m3}	S_{m4}		$i_a > 0$	$i_a < 0$
1	1	0	0	$1/2V_{dc}$	$S_{m1}, S_{m2}, S_{a3}, S_{a4}$	$D_{m1}, D_{m2}, D_{a3}, D_{a4}$
1	0	1	0	0	$S_{m1}, D_{a2}, D_{m3}, S_{a4}$	$D_{m1}, S_{a2}, S_{m3}, D_{a4}$
0	1	1	0		$D_{a1}, S_{m2}, D_{m3}, S_{a4}$	$S_{a1}, D_{m2}, S_{m3}, D_{a4}$
0	1	0	1		$D_{a1}, S_{m2}, S_{a3}, D_{m4}$	$S_{a1}, D_{m2}, D_{a3}, S_{m4}$
1	0	0	1		$S_{m1}, D_{a2}, S_{a3}, D_{m4}$	$D_{m1}, S_{a2}, D_{a3}, S_{m4}$
0	0	1	1	$-1/2V_{dc}$	$D_{m1}, D_{m2}, D_{a3}, D_{a4}$	$S_{m1}, S_{m2}, S_{a3}, S_{a4}$

The duty cycle of the switch S_{m1} is $d_{m1} = d_{p\_1} + \frac{1}{2} d_{p\_0} = \frac{1}{4} m \sin \omega t + \frac{1}{4}$ and current flows through the main switching devices during the carrier period T_s is $d_{m1} \cdot T_s$.

Where $d_{p\_1} = \frac{1}{2} \cdot m \cdot \sin\theta$ and $d_{p\_0} = \frac{1}{2} \cdot (1 - m \cdot \sin\theta)$.

The currents in the switching devices are:

$$I_{Sm1,av} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} d_{m1} i_a d\omega = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} \frac{1}{4} [1 + m \sin \omega t] \cdot I_o \sin(\omega t - \varphi) d\omega$$
$$= \frac{4 I_o}{\pi} [\pi m \cos\varphi + 4] \tag{6.27}$$

$$I^2_{Sm1,rms} = \frac{1}{2\pi} \int_{\varphi}^{\pi+\varphi} d_{m1} i_a^2 d\omega = \frac{12 I_o^2}{\pi} [3\pi + 8m \cos\varphi] \tag{6.28}$$

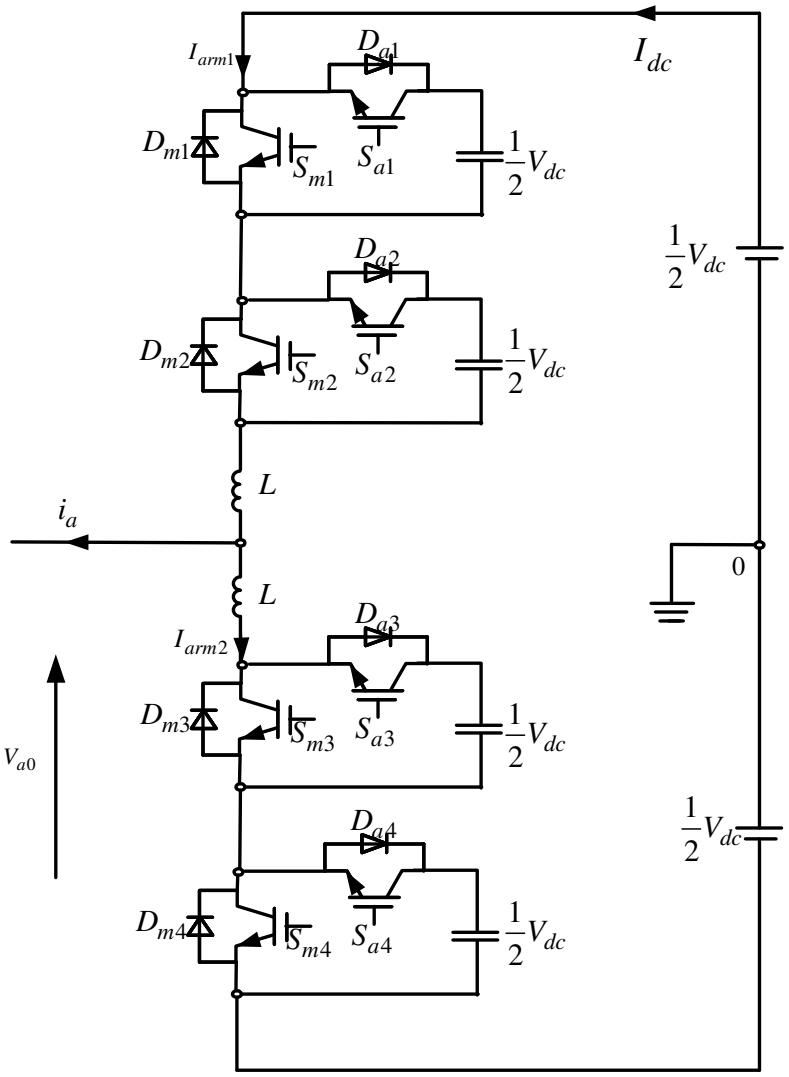

Figure 6-8: Phase 'a' of a 3-level M2C.

$$I_{Dm1,av} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} d_{m1} i_a \, d\omega = \frac{4I_o}{\pi}[\pi m \cos\varphi - 4] \tag{6.29}$$

$$I^2_{Dm1,rms} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} d_{m1} i_a^2 \, d\omega = \frac{12I_o^2}{\pi}[3\pi - 8m\cos\varphi] \tag{6.30}$$

$$I_{Sa1,av} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} (1-d_{m1}) i_a \, d\omega = \frac{4I_o}{\pi}[12 - \pi m \cos\varphi] \tag{6.31}$$

$$I^2_{Sa1,rms} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} (1-d_{m1}) i_a^2 \, d\omega = \frac{12I_o^2}{\pi}[9\pi - 8m\cos\varphi] \tag{6.32}$$

$$I_{Da1,av} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi}(1-d_{m1})i_a d\omega = -\frac{4I_o}{\pi}[\pi m\cos\varphi + 12] \tag{6.33}$$

$$I^2_{Da1,rms} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi}(1-d_{m1})i_a^2 d\omega = \frac{12I_o^2}{\pi}[9\pi + 8m\cos\varphi] \tag{6.34}$$

$$\begin{aligned} &I_{Sm2,av} = I_{Sm1,av}, I_{Sm3,av} = I_{Sm4,av} = -I_{Sm1,av} \\ &I^2_{Sm2,rms} = I^2_{Sm3,rms} = I^2_{Sm4,rms} = I^2_{Sm1,rms} \\ &I_{Dm1,av} = I_{Dm2,av}, I_{Dm3,av} = I_{Dm4,av} = -I_{Dm1,av} \\ &I^2_{Dm2,rms} = I^2_{Dm3,rms} = I^2_{Dm4,rms} = I^2_{Dm1,rms} \end{aligned} \tag{6.35}$$

Therefore, the total conduction loss for one switching device, including IBGT and diode, can be estimated as:

$$P_{conduction} = \begin{pmatrix} \frac{12I_o^2}{\pi}(3\pi + 8m\cos\varphi)\cdot R_{on} + \frac{4I_o}{\pi}(4 + \pi m\cos\varphi)\cdot V_{f0} + \\ \frac{12I_o^2}{\pi}(3\pi - 8m\cos\varphi)\cdot R_D + \frac{4I_o}{\pi}(\pi m\cos\varphi - 4)\cdot V_{D0} \end{pmatrix} \tag{6.36}$$

- *Switching losses*

Since the switching instant S_{m1} is determined by the balancing requirements of the cell capacitors, the switching frequency in consecutive fundamental cycles may not be constant. However, it will be constant over several cycles. Therefore, the effective switching frequency per switch is the average switching frequency over several fundamental periods. The discontinuous nature of device current is ignored when calculating the switching energy loss. Instead the continuous current is used to estimate the equivalent switching energy loss per switch over the fundamental period, which is then divided by the effective switching period in order to obtain the switching power loss.

The IGBT switching losses are the sum of the turn-on and turn-off switching losses based on equation (6.13). Specifically:

$$P_{swithcing\_IGBT} = \frac{f_s}{2\pi}\int_{\varphi}^{\pi+\varphi}[(k_{I\_on1} + k_{I\_off1})\cdot I_o\sin(\omega t - \varphi) + k_{I\_on2} + k_{I\_off2}]d\omega t \tag{6.37}$$

$$= \frac{f_s \cdot (k_{I\_on1} + k_{I\_off1}) \cdot I_o}{\pi} + \frac{f_s}{2}(k_{I\_on2} + k_{I\_off2})$$

As the diode switching losses are predominantly recovery loss, and can be expressed as:

$$P_{swithcing\_diode} = \frac{f_s}{4\pi} \int_{\varphi+\pi}^{2\pi+\varphi} [(k_{D\_off1} \cdot I_o \sin(\omega t - \varphi) + k_{D\_off2}] d\omega t$$
$$= \frac{f_s \cdot k_{D\_off1} \cdot I_o}{\pi} + \frac{f_s}{2} \cdot k_{D\_off2} \quad (6.38)$$

In this case, the effective switching frequency for each individual switching device is obtained from MATLAB simulations under the same operation conditions. Taking operation condition (a) as an example, the operating modulating index is:

$$M = \frac{2\sqrt{2}V_L}{\sqrt{3}V_{dc}} \approx 0.9$$

The full-load current (neglecting the current harmonics) at 0.8 power factor lagging is given by:

$$I_L = \frac{P}{\sqrt{3} \cdot V_L \cos\varphi} = \frac{16MW}{\sqrt{3} \times 11kV \times 0.8} \approx 1049.8A$$

($I_o = \sqrt{2} I_L$ Assuming star connected load).

The effective switching frequency for the devices S_{m1} and S_{a1} are: S_{m1}=500Hz (main switch) S_{a1}=700Hz (auxiliary switch). Practically, since the current sharing between the IGBT and its freewheel diode depend on load power factor, the actual effective switching frequencies of the IGBTs and diodes are less the values obtained. However, for simplification purposes, the effective switching frequencies used in estimating the switching and recovery power losses for both the IGBTs and diodes are 500Hz for the main switch and 700Hz for the auxiliary switch. Therefore, an efficient way of obtaining the effective switching frequency per switch (IGBT and diode) is to count the number of current commutations over an integral number of fundamental cycles and then calculate the average switching frequency for one fundamental cycle.

IGBT S_{m1} and diode D_{m1} (main switch):

P_{sm1}=0.985kW

P_{dm1}=0.644kW

IGBT S_{a1} and diode D_{a1} (main switch):

P_{sa1}=1.159kW

P_{da1}=0.902kW

Total switching and recovery losses in one cell are:

P=7×(P_{sm1}+ P_{dm1}+ P_{sa1}+P_{da1})=25.83kW

Therefore, the total switching and recovery losses, where each switching device blocks 1.5kV not 1.8kV (switching loss is based on 1.8kV in the datasheet), is given by 1.5/1.8×25.83kW=21.525kW

Table 6-4 shows the conversion losses of the three-level M2C under three different operating conditions.

Table 6-4: Summary of three-level M2C conversion losses

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)
Conduction loss (kW)	126.2kW
Switching losses (kW)	258.3kW
Total conversion losses (kW)	384.5kW (1.92%)
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)
Conduction loss (kW)	142.8kW
Switching losses (kW)	274.5kW
Total conversion losses (kW)	417.3kW (2.02%)
Operating condition (c)	20MVA at 11kV and unity power factor
Conduction loss (kW)	131.04kW
Switching losses (kW)	223.7kW
Total conversion losses (kW)	354.74kW (1.77%)

6.4.2.2 Five-level M2C

- *Conduction losses*

The duty cycles d_1 to d_4 represent the time spent at each voltage level as a ratio of the carrier period T_s. The duty cycles of the four upper main switches (see Chapter 4 Figure 4-5) of the five-level converter are:

$$d_1 = 2 \cdot m \cdot \sin\theta - 1, d_2 = 2 \cdot m \cdot \sin\theta, d_3 = 2 \cdot m \cdot \sin\theta + 1, d_4 = 2 \cdot (m \cdot \sin\theta + 1) \quad (6.39)$$

The duty cycle of the switch S_{m1} is $d_{m1} = d_1 + \frac{1}{4}d_2 + \frac{1}{2}d_3 = \frac{7}{2}m\sin\omega t - \frac{1}{2}$ with

current circulated through the main switching devices for a period $d_{m1} \cdot T_s$ during the carrier period T_S. The currents in the switching devices are:

$$I_{Sm1,av} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} d_{m1} i_a d\omega = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} [\frac{7}{2} m \sin\omega t - \frac{1}{2}] \cdot I_o \sin(\omega t - \varphi) d\omega$$
$$= \frac{2I_o}{\pi}[7\pi m \cos\varphi - 4] \tag{6.40}$$

$$I^2_{Sm1,rms} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} d_{m1} i_a^2 d\omega = \frac{6I_o^2}{\pi}[28m\cos\varphi - 3\pi] \tag{6.41}$$

$$I_{Dm1,av} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} d_{m1} i_a d\omega = \frac{2I_o}{\pi}[7\pi m \cos\varphi + 4] \tag{6.42}$$

$$I^2_{Dm1,rms} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} d_{m1} i_a^2 d\omega = -\frac{6I_o^2}{\pi}[28m\cos\varphi + 3\pi] \tag{6.43}$$

$$I_{Sa1,av} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} (1-d_{m1}) i_a d\omega = \frac{2I_o}{\pi}[7\pi m \cos\varphi + 4] \tag{6.44}$$

$$I^2_{Sa1,rms} = \frac{1}{2\pi}\int_{\varphi}^{\pi+\varphi} (1-d_{m1}) i_a^2 d\omega = \frac{6I_o^2}{\pi}[3\pi - 28m\cos\varphi] \tag{6.45}$$

$$I_{Da1,av} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} (1-d_{m1}) i_a d\omega = \frac{2I_o}{\pi}[4 - 7\pi m \cos\varphi] \tag{6.46}$$

$$I^2_{Da1,rms} = \frac{1}{2\pi}\int_{\varphi+\pi}^{2\pi+\varphi} (1-d_{m1}) i_a^2 d\omega = \frac{6I_o^2}{\pi}[3\pi + 28m\cos\varphi] \tag{6.47}$$

$$I_{Sm2,av} = I_{Sm1,av}, I_{Sm3,av} = I_{Sm4,av} = -I_{Sm1,av}$$
$$I^2_{Sm2,rms} = I^2_{Sm3,rms} = I^2_{Sm4,rms} = I^2_{Sm1,rms}$$
$$I_{Dm1,av} = I_{Dm2,av}, I_{Dm3,av} = I_{Dm4,av} = -I_{Dm1,av} \tag{6.48}$$
$$I^2_{Dm2,rms} = I^2_{Dm3,rms} = I^2_{Dm4,rms} = I^2_{Dm1,rms}$$

The average and *rms* currents in the lower four cells are the same as for the upper four. Therefore, the total conduction losses for one switching device, including the IBGT and the diode, can be estimated as:

$$P_{conduction} = \left(\begin{array}{l} \frac{6I_o^2}{\pi}(28m\cos\varphi - 3\pi)\cdot R_{on} + \frac{2I_o}{\pi}(7\pi m\cos\varphi - 4)\cdot V_{f0} + \\ -\frac{6I_o^2}{\pi}(28m\cos\varphi + 3\pi)\cdot R_D + \frac{2I_o}{\pi}(4 + 7\pi m\cos\varphi)\cdot V_{D0} \end{array} \right) \quad (6.49)$$

- *Switching losses*

Calculation of five-level M2C switching losses follows the same procedure as for the three-level M2C.

Table 6-5 shows the conversion losses of the five-level M2C under three different operating conditions.

Table 6-5: Summary of five-level M2C conversion losses

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)
Conduction loss (kW)	130.56kW
Switching losses (kW)	171.2kW
Total conversion losses (kW)	301.76kW (1.51%)
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)
Conduction loss (kW)	142.08kW
Switching losses (kW)	183.5kW
Total conversion losses (kW)	325.58 (1.62%)
Operating condition (c)	20MVA at 11kV and unity power factor
Conduction loss (kW)	153.6kW
Switching losses (kW)	159.4kW
Total conversion losses (kW)	313kW (1.56%)

6.4.2.3 Nine-level M2C

For nine-level and seventeen-level M2C, the average and root mean currents required to estimate the conduction losses using equation (6.6) are obtained from simulation. This approach is used due to the increased complexity of an analytical approach for estimation of device average and root mean square currents. The switching loss per IGBT due to turn-on and turn-off in the nine-level M2C is estimated as:

$$P_{switching\_IGBT} = f_s[k_{I\_on1}\cdot\overline{I_1} + k_{I\_off1}\cdot\overline{I_2} + k_{I\_on2} + k_{I\_off2}] \quad (6.50)$$

Where $k_{I\_on1}, k_{I\_off1}, k_{I\_on2}, k_{I\_off2}$ are constants determined by linearizing the switching energy curves in the data sheet, $\bar{I}_1$ and $\bar{I}_2$ are average currents at turn-on

and turn-off instants over the full fundamental period, and f_s is the frequency at which each device operates.

The recovery losses in the freewheeling diodes are given by:

$$P_{switching\_diode} = f_s[k_{D\_off1} \cdot \overline{I_2} + k_{D\_off2}] \tag{6.51}$$

Where k_{D_off1} and k_{D_off2} are constants determined by linearizing the switching energy graph in the data sheet.

When the converter delivers 20MW at 0.8 power factor lagging with a modulation index of 0.9, the average and RMS device currents in one cell are:

Main switch	IGBT	$I_{mean} = 765A, I_{rms} = 1250A, \overline{I}_{on} = 1440A, \overline{I}_{off} = 1400A$
	Diode	$I_{mean} = 150A, I_{rms} = 400A, \overline{I}_{off} = 1500A$
Auxiliary switch	IGBT	$I_{mean} = 160A, I_{rms} = 350A, \overline{I}_{on} = 1400A, \overline{I}_{off} = 700A$
	Diode	$I_{mean} = 100A, I_{rms} = 400A, \overline{I}_{off} = 1500A$

Table 6-6 shows the conversion losses of the nine-level converter under three different operating conditions.

Table 6-6: Summary of nine-level M2C conversion losses

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)
Conduction loss (kW)	153.6kW
Switching losses (kW)	94.8kW
Total conversion losses (kW)	248.4kW (1.24%)
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)
Conduction loss (kW)	167.3kW
Switching losses (kW)	108.6kW
Total conversion losses (kW)	275.9kW (1.37%)
Operating condition (c)	20MVA at 11kV and unity power factor
Conduction loss (kW)	158.4kW
Switching losses (kW)	87.1kW
Total conversion losses (kW)	245.5kW (1.22%)

6.4.2.4 Seventeen-level M2C

Calculation of seventeen-level M2C conduction and switching losses follows the same procedure as the calculations for nine-level conventional converter.

Table 6-7 shows the conversion losses of the seventeen-level converter at three different operating conditions.

Table 6-7: Summary of seventeen-level M2C conversion losses

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)
Conduction loss (kW)	170.8kW
Switching losses (kW)	42.4kW
Total conversion losses (kW)	213.2kW (1.06%)
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)
Conduction loss (kW)	190.1kW
Switching losses (kW)	67.1kW
Total conversion losses (kW)	257.2kW (1.28%)
Operating condition (c)	20MVA at 11kV and unity power factor
Conduction loss (kW)	175.7kW
Switching losses (kW)	36.96kW
Total conversion losses (kW)	212.7 kW (1.06%)

6.4.3 Hybrid Cascaded Multilevel converter Conversion Loss

6.4.3.1 HCMC with two cells in the AC side

Figure 6-9 shows one phase of an HCMC with 2 cells in the ac side.

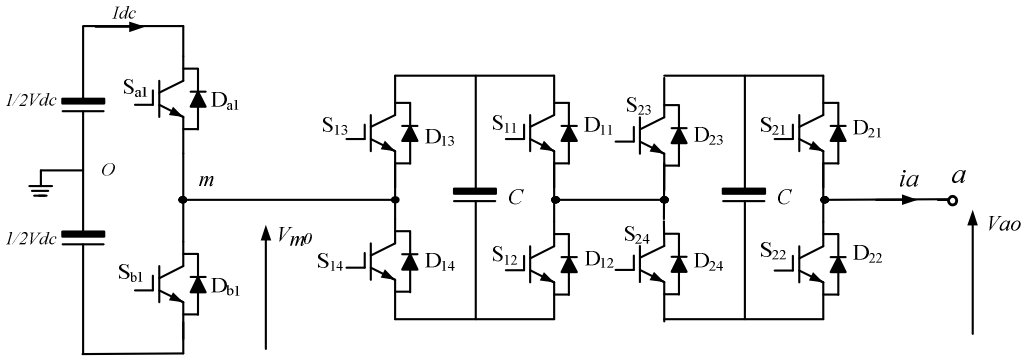

Figure 6-9: Hybrid multilevel converters with 2 H-bridge cells in the ac side.

- *Conduction losses*

Main bridge two-level converter:

The main two-level converter is used to synthesize the desire fundamental voltage component by switching between $+½V_{dc}$ and $-½V_{dc}$ using selective harmonic elimination (SHE-PWM) which the switching frequency is 150Hz. This is illustrated in Figure 6-10. For simplicity, the current harmonics are neglected and the load current per phase is assumed to be:

$$i_a = I_o \sin(\omega t - \varphi) \tag{6.52}$$

Where I_o is the peak current and φ is the phase angle.

The average and *rms* current in the converter switching devices can be obtained as follows:

Switch Sa1:

The current flow in switch S_{a1} can be defined as:

$$i_{Sa1} = \begin{cases} i_a & \alpha \le \omega t \le \pi - \alpha \;\&\; \pi \le \omega t \le \pi + \varphi \\ 0 \end{cases} \tag{6.53}$$

Therefore the average and *rms* currents in S_{a1} are given by:

$$\begin{aligned} I_{Sa1\_av} &= \frac{1}{2\pi}\left(\int_{\alpha}^{\pi-\alpha} I_o \sin(\omega t - \varphi) d\omega t + \int_{\pi}^{\pi+\varphi} I_o \sin(\omega t - \varphi) d\omega t\right) \\ &= \frac{I_o}{2\pi}[\cos(\alpha - \varphi) + \cos(\alpha + \varphi) - \cos(\varphi) + 1] \end{aligned} \tag{6.54}$$

$$\begin{aligned} I^2_{Sa1\_rms} &= \frac{1}{2\pi}\left(\int_{\alpha}^{\pi-\alpha} I_o^2 \sin^2(\omega t - \varphi) d\omega t + \int_{\pi}^{\pi+\varphi} I_o^2 \sin^2(\omega t - \varphi) d\omega t\right) \\ &= \frac{I_o^2}{2\pi}[\cos(\alpha - \varphi)\cdot\sin(\alpha - \varphi) + \cos(\alpha + \varphi)\cdot\sin(\alpha + \varphi) + \cos(\varphi)\cdot\sin(\varphi) + \varphi] \end{aligned} \tag{6.55}$$

Diode Da1:

The current flow in diode Da1 is defined by:

$$i_{Da1} = \begin{cases} i_a & \pi + \varphi \le \omega t \le \pi + \alpha \;\&\; 2\pi - \alpha \le \omega t \le 2\pi \\ 0 \end{cases} \tag{6.56}$$

The average and *rms* currents in diode D_{a1} are given by:

$$I_{Da1\_av} = \frac{1}{2\pi}\left(\int_{\pi+\varphi}^{\pi+\alpha} I_o \sin(\omega t-\varphi)d\omega t + \int_{2\pi-\alpha}^{2\pi} I_o \sin(\omega t-\varphi)d\omega t\right)$$
$$= \frac{I_o}{2\pi}[\cos(\alpha-\varphi)+\cos(\alpha+\varphi)-\cos(\varphi)-1] \quad (6.57)$$

$$I^2_{Da1\_rms} = \frac{1}{2\pi}\left(\int_{\pi+\varphi}^{\pi+\alpha} I_o^2 \sin^2(\omega t-\varphi)d\omega t + \int_{2\pi-\alpha}^{2\pi} I_o^2 \sin^2(\omega t-\varphi)d\omega t\right)$$
$$= \frac{I_o^2}{2\pi}[-\cos(\alpha-\varphi)\cdot\sin(\alpha-\varphi)-\cos(\alpha+\varphi)\cdot\sin(\alpha+\varphi)+\cos(\varphi)\cdot\sin(\varphi)-\varphi] \quad (6.58)$$

Since the current and voltage waveforms have quarter and half wave symmetry, the average and *rms* currents in the devices S_{a2} and D_{a2} are identical to those in devices S_{a1} and D_{a1}.

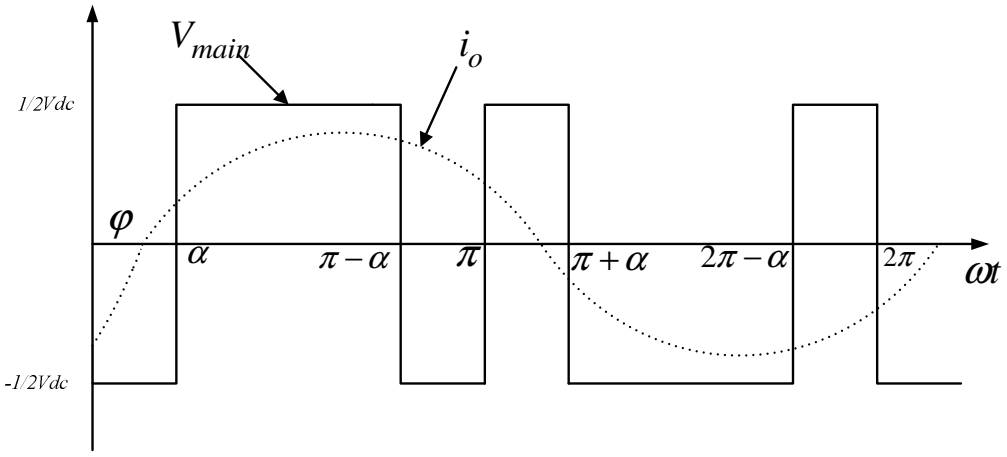

Figure 6-10: Main two-level bridge switching pattern.

H-bridge chain cells (S_{11}, D_{11}) and (S_{21}, D_{21}):

The current flow in devices (S_{11}, D_{11}) and (S_{21}, D_{21}) can be defined as:

$$i_{S11} = i_{S21} = \begin{cases} i_a & \varphi \le \omega t \le \alpha \;\&\; \pi-\alpha \le \omega t \le \pi \\ 0 \end{cases}$$
$$i_{D11} = i_{D21} = \begin{cases} i_a & 0 \le \omega t \le \varphi \;\&\; \pi+\alpha \le \omega t \le 2\pi-\alpha \\ 0 \end{cases} \quad (6.59)$$

Therefore, the average and *rms* currents in these devices are:

$$I_{S11\_av} = I_{S21\_av} = \frac{1}{2\pi}\left(\int_{\varphi}^{\alpha} I_o \sin(\omega t-\varphi)d\omega t + \int_{\pi-\alpha}^{\pi} I_o \sin(\omega t-\varphi)d\omega t\right)$$
$$= \frac{I_o}{2\pi}[-\cos(\alpha-\varphi)-\cos(\alpha+\varphi)+\cos(\varphi)+1] \quad (6.60)$$

$$I_{S11\_rms}^2 = I_{S21\_rms}^2 = \frac{1}{2\pi}\left(\int_{\varphi}^{\alpha} I_o^2 \sin^2(\omega t-\varphi)d\omega t + \int_{\pi-\alpha}^{\pi} I_o^2 \sin^2(\omega t-\varphi)d\omega t\right)$$
$$= \frac{I_o^2}{2\pi}[\cos(\alpha-\varphi)\cdot\sin(\alpha-\varphi) - \cos(\alpha+\varphi)\cdot\sin(\alpha+\varphi) + \cos(\varphi)\cdot\sin(\varphi)+\varphi] \quad (6.61)$$

$$I_{D11\_av} = I_{D21\_av} = \frac{1}{2\pi}\left(\int_{0}^{\varphi} I_o \sin(\omega t-\varphi)d\omega t + \int_{\pi+\alpha}^{2\pi-\alpha} I_o \sin(\omega t-\varphi)d\omega t\right)$$
$$= \frac{I_o}{2\pi}[-\cos(\alpha-\varphi) - \cos(\alpha+\varphi) + \cos(\varphi) - 1] \quad (6.62)$$

$$I_{D13\_rms}^2 = I_{D23\_rms}^2 = \frac{1}{2\pi}\left(\int_{0}^{\varphi} I_o^2 \sin^2(\omega t-\varphi)d\omega t + \int_{\pi+\alpha}^{2\pi-\alpha} I_o^2 \sin^2(\omega t-\varphi)d\omega t\right)$$
$$= \frac{I_o^2}{2\pi}\left[\begin{array}{c} -\cos(\alpha-\varphi)\cdot\sin(\alpha-\varphi) + \cos(\alpha+\varphi)\cdot\sin(\alpha+\varphi) \\ +\cos(\alpha-\varphi)\cdot\sin(\alpha-\varphi) - \alpha \end{array}\right] \quad (6.63)$$

Since two H-bridge cells is operating as a five-level converter and devices (S_{11},D_{11}), (S_{12},D_{12}), (S_{21},D_{21}) and (S_{22},D_{22}) operate in a discontinuous mode over the entire fundamental cycle, the discontinuous currents in these devices are replaced by their equivalent continuous currents using a local average (average over one switching cycle). To perform this transformation, assume the carrier frequency is much higher than the fundamental frequency, then the modulating signal V_{HB} can be considered constant within each carrier period as shown in Figure 6-11. Duty cycles are used to obtain the local average and *rms* currents within one carrier cycle, and are defined as follows:

$$D_1 = 2V_{HB} - 1,\ D_2 = 2V_{HB},\ D_3 = 2V_{HB} + 1,\ D_4 = 2(V_{HB} + 1)$$

Where:

$$V_{HB}(t) = \begin{cases} m\sin\omega t + 1 - m_{3h}\sin 3\omega t & 0 \le \omega t < \alpha, \pi-\alpha \le \omega t < \pi, \pi+\alpha \le \omega t < 2\pi-\alpha \\ m\sin\omega t - 1 - m_{3h}\sin 3\omega t & \alpha \le \omega t < \pi-\alpha, \pi \le \omega t < \pi+\alpha, 2\pi-\alpha \le \omega t < 2\pi \end{cases}$$

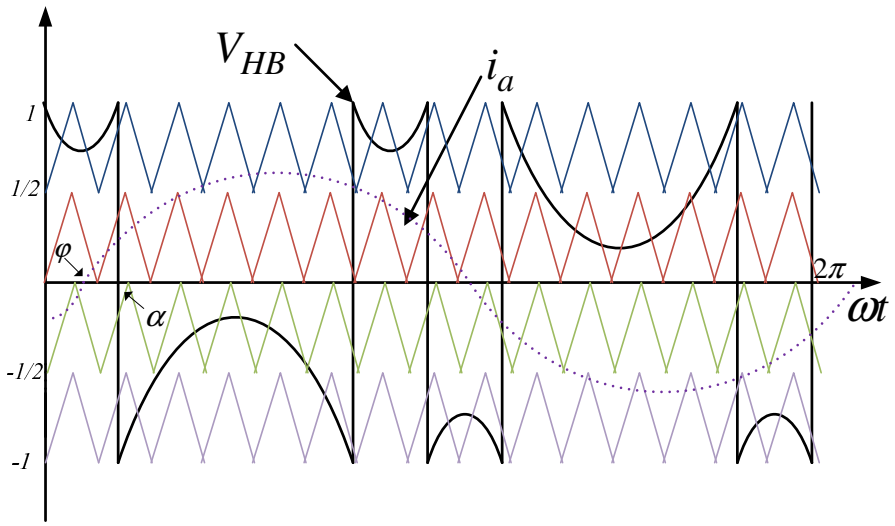

Figure 6-11: Five-level PD carriers, H-bridge modulating signal and load current waveforms.

The case to follow assumes $\varphi < \alpha$ and based on Figure 6-11, and $V_{HB} \geq -0.5$ when $\alpha \leq \omega t \leq \pi - \alpha$ and $0 \leq V_{HB} \leq 0.5$ when $\pi + \alpha \leq \omega t \leq 2\pi - \alpha$. The local average and *rms* currents in switching devices S_{11} and D_{11}, within one carrier period, are obtained as follows:

In the period $0 \leq \omega t \leq \alpha$, the output phase switches between 0 and +½V_{dc}, whence the local average and *rms* currents within one switching cycle are:

For $0 < \omega t < \varphi$

$$\begin{aligned} \bar{i}_{D11} &= (D_1 + \frac{1}{2} D_2) i_a \\ \bar{i}^2_{D11\_rms} &= (D_1 + \frac{1}{2} D_2) i_a^2 \\ \bar{i}_{S11} &= 0 \\ \bar{i}^2_{S11\_rms} &= 0 \end{aligned} \tag{6.64}$$

For $\varphi \leq \omega t \leq \alpha$

$$\begin{aligned} \bar{i}_{S11} &= (D_1 + \frac{1}{2} D_2) i_a \\ \bar{i}^2_{S11\_rms} &= (D_1 + \frac{1}{2} D_2) i_a^2 \\ \bar{i}_{D11} &= 0 \\ \bar{i}^2_{D11\_rms} &= 0 \end{aligned} \tag{6.65}$$

In the period $\pi - \alpha \leq \omega t \leq \pi$, the converter output phase switches between 0 and +½V_{dc} (in this region, for a lagging and unity power factor there is no current flow in

the diode), therefore the local average and RMS currents within one switching cycle are:

$$\begin{aligned}
\overline{i}_{S11} &= (D_1 + \frac{1}{2}D_2)i_a \\
\overline{i}^2_{S11_rms} &= (D_1 + \frac{1}{2}D_2)i_a^2 \\
\overline{i}_{D11} &= 0 \\
\overline{i}^2_{D11_rms} &= 0
\end{aligned} \tag{6.66}$$

In the period $\pi + \alpha < \omega t \le 2\pi - \alpha$ the converter switches between 0 and ¼V_{dc}, therefore the average and *rms* currents within one switching cycle are expressed as:

$$\begin{aligned}
\overline{i}_{D11} &= \frac{1}{2}D_3 i_a \\
\overline{i}^2_{D11_rms} &= \frac{1}{2}D_3 i_a^2 \\
\overline{i}_{S11} &= 0 \\
\overline{i}^2_{S11_rms} &= 0
\end{aligned} \tag{6.67}$$

Therefore the average and *rms* currents in switching devices ($S_{11}$and S_{21}) and (D_{11} and D_{21}) over the full fundamental period are given by:

IGBT S_{11}:

$$I_{S11\_av} = \frac{1}{2\pi}\left[\int_{\varphi}^{\alpha}(D_1 + \tfrac{1}{2}D_2)i_a d\omega t + \int_{\pi-\alpha}^{\pi}(D_1 + \tfrac{1}{2}D_2)i_a d\omega t + \int_{\pi}^{\pi+\varphi}(D_4 + \tfrac{1}{2}D_3)i_a d\omega t\right] \tag{6.68}$$

$$I^2_{S11\_rms} = \frac{1}{2\pi}\left[\int_{\varphi}^{\alpha}(D_1 + \tfrac{1}{2}D_2)i_a^2 d\omega t + \int_{\pi-\alpha}^{\pi}(D_1 + \tfrac{1}{2}D_2)i_a^2 d\omega t + \int_{\pi}^{\pi+\varphi}(D_4 + \tfrac{1}{2}D_3)i_a^2 d\omega t\right] \tag{6.69}$$

Diode D_{11}:

$$I_{D11\_av} = \frac{1}{2\pi}\left[\int_{0}^{\varphi}(D_1 + \tfrac{1}{2}D_2)i_a d\omega t + \int_{\pi+\varphi}^{\pi+\alpha}(D_4 + \tfrac{1}{2}D_3)i_a d\omega t + \int_{\pi+\alpha}^{2\pi-\alpha}\tfrac{1}{2}D_3 i_a d\omega t\right] \tag{6.70}$$

$$I^2_{D11\_rms} = \frac{1}{2\pi}\left[\int_{0}^{\varphi}(D_1 + \tfrac{1}{2}D_2)i_a^2 d\omega t + \int_{\pi+\varphi}^{\pi+\alpha}(D_4 + \tfrac{1}{2}D_3)i_a^2 d\omega t + \int_{\pi+\alpha}^{2\pi-\alpha}\tfrac{1}{2}D_3 i_a^2 d\omega t\right] \tag{6.71}$$

Knowledge of the above currents facilitates estimation of the conduction loss in each switching devices in the HCMC with two H-bridge cells in ac side.

- *Switching losses*

The switching losses of the main two-level bridge switches are obtained as follow:

Main bridge two-level converter:

Switch S_{a1}:

Based on Figure 6-10, switch S_{a1} continuously conducts during period $\alpha \le \omega t \le \pi - \alpha$.

$$P_{Switching\_Sa1} = \frac{f_{s\_M}}{2\pi}\int_{\alpha}^{\pi-\alpha}[(k_{I\_on1}+k_{I\_off1})I_0\sin(\omega t-\varphi)+(k_{I\_on2}+k_{I\_off2})]d\omega t$$
$$= \frac{f_{s\_M}(k_{I\_on1}+k_{I\_off1})I_o}{2\pi}[1+cos\varphi]+\frac{f_{s\_M}(k_{I\_on2}+k_{I\_off2})}{2\pi}(\pi-\varphi) \quad (6.72)$$

$$P_{Switching\_Da1} = \frac{f_{s\_M}}{2\pi}\int_{\pi+\varphi}^{\pi+\alpha}[k_{D\_off1}I_0\sin(\omega t-\varphi)+k_{D\_off2}]d\omega t$$
$$= \frac{k_{D\_off1}f_{s\_M}I_0}{2\pi}[1-\cos\varphi]+\frac{k_{D\_off2}f_{s\_M}\varphi}{2\pi} \quad (6.73)$$

Where $f_{s\_M} = 150Hz$. The switching losses in the lower devices (S_{a2} and D_{a2}) of the main bridge are identical to those in the top (S_{a1} and D_{a1}).

H-bridge chain cells (S_{13},D_{13}) and (S_{11}&D_{11}):

Switches S_{13} and D_{13}:

$$P_{Swithcing\_S13} = \frac{f_s}{2\pi}\int_{0}^{\varphi}[(k_{I\_on1}+k_{I\_off1})I_0\sin(\omega t-\varphi)+(k_{I\_on2}+k_{I\_off2})]d\omega t$$
$$= \frac{(k_{I\_on1}+k_{I\_off1})f_sI_o}{2\pi}[1-cos\varphi]+\frac{(k_{I\_on2}+k_{I\_off2})f_s\varphi}{2\pi} \quad (6.74)$$

$$P_{Switching\_D13} = \frac{f_s}{2\pi}\int_{\varphi}^{\pi}[k_{D\_off1}I_o\sin(\omega t-\varphi)+k_{D\_off2}]d\omega t$$
$$= \frac{k_{D\_off1}f_sI_o}{2\pi}[1+cos\varphi]+\frac{k_{D\_off2}f_s}{2\pi}(\pi-\varphi) \quad (6.75)$$

The switching losses in the lower devices (S_{14} and D_{14}) of the cells are identical to those in the top (S_{13} and D_{13}).

Switches S_{11} and D_{11}:

$$P_{Switching\_S11} = \frac{1}{2\pi}\int_{\pi}^{\pi+\varphi}[(k_{I\_on1}+k_{I\_off1})I_0\sin(\omega t-\varphi)+(k_{I\_on2}+k_{I\_off2})]d\omega t$$
$$= \frac{(k_{I\_on1}+k_{I\_off1})f_sI_m}{\pi}+\tfrac{1}{2}(k_{I\_on2}+k_{I\_off2})f_s \quad (6.76)$$

$$P_{Switching\_D11} = \frac{f_s}{2\pi}\int_{\pi+\varphi}^{2\pi+\varphi}[k_{D\_off1}I_o\sin(\omega t-\varphi)+k_{D\_off2}]d\omega t$$
$$= \frac{k_{D\_off1}f_sI_o}{\pi}+\tfrac{1}{2}k_{D\_off2}f_s \quad (6.77)$$

In this case, the effective switching frequency for each individual switching device is obtained from MATLAB simulations under the same operation conditions.

Table 6-8 shows the conversion losses of the HCMC with two H-bridge cells in the ac side at three different operating conditions.

Table 6-8: Summary of HCMC with two H-bridge cells in the ac side conversion losses.

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	140.4	92.7
Switching losses (kW)	42.3	78.6
Total conversion losses (kW)	354kW (1.77%)	
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	104.2	86.1
Switching losses (kW)	33.5	75.2
Total conversion losses (kW)	299kW (1.5%)	
Operating condition (c)	20MVA at 11kV and unity power factor	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	131.4	82.9
Switching losses (kW)	40.8	68.7
Total conversion losses (kW)	323.8 kW (1.61%)	

6.4.3.2 HCMC with seven cells in the AC side

For the HCMC with seven and ten cells in the ac side, the average and *rms* currents required to estimate the conduction losses equation (6.6), are obtained from simulation. This approach is used due to increased complexity of an analytical approach for estimation of device average and root mean square currents. The switching loss per IGBT due to turn-on and turn-off in the HCMC with seven and ten cells in the ac side is estimated using the equation (6.50), while the recovery losses in

the freewheeling diodes are calculated using equation (6.51). The average current at turn-on, turn-off, and diode reverse recovery instants over the full fundamental period are also obtained from simulations.

The conduction and switching losses of the two-level main bridge are remained same with the HCMC with two H-bridge cells due to switching pattern for the two-level main bridge is only depended on the modulation index.

Table 6-9 shows the conversion losses of the HCMC with seven H-bridge cells in the ac side at three different operating conditions.

Table 6-9: Summary of HCMC with seven H-bridge cells in ac side conversion losses

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	140.2	122.3
Switching losses (kW)	42.3	42.63
Total conversion losses (kW)	347.43kW (1.73%)	
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	104.2	116.2
Switching losses (kW)	33.5	47
Total conversion losses (kW)	300.9kW (1.51%)	
Operating condition (c)	20MVA at 11kV and unity power factor	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	131.4	108.9
Switching losses (kW)	40.8	57.6
Total conversion losses (kW)	338.7 kW (1.69%)	

6.4.3.3 HCMC with ten cells in the AC side

The loss calculation procedure for the HCMC with ten cells in the ac side is same as that for the HCMC with seven cells. Table 6-10 shows the conversion losses for the ten H-bridge cells case, under the three different operating conditions.

Table 6-10: Summary of HCMC with ten H-bridge cells in ac side conversion losses

Operating condition (a)	20MVA at11kV and power factor of 0.8 lagging (inverter with limited reactive power capability)	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	140.4	141.2
Switching losses (kW)	42.3	41.5
Total conversion losses (kW)	365.4kW (1.82%)	
Operating condition (b)	20MVA at 11kV and zero power factor (reactive power applications)	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	104.2	136.4
Switching losses (kW)	33.5	40.2
Total conversion losses (kW)	314.2kW (1.57%)	
Operating condition (c)	20MVA at 11kV and unity power factor	
	Two-level main bridge	H-bridge cells
Conduction loss (kW)	131.4	120.5
Switching losses (kW)	40.8	42.8
Total conversion losses (kW)	335.5kW (1.67%)	

6.5 Experimental Conversion Losses

For comparison with the simulations, experimental losses are presented for the three operation conditions:

(1) V_{dc}=200V, modulation index M=1.2, power factor $p.f.$=0.9 lagging.

(2) V_{dc}=200V, modulation index M=1.15, power factor $p.f.$=unity.

(3) V_{dc}=200V, modulation index M=0.8, power factor $p.f.$=0.9 lagging.

The three-phase output active fundamental power delivered to the load due to the fundamental supply component is monitored with a power analyser; dc voltage and current measurement are taken from the dc source.

The switching device parameters of switching device for the Nine-level HCMC circuit are shown in Table 6-11. To allow comparison, the operating conditions for the simulated conversion losses based on the mathematical analysis in 6.4.3.1 are to the experiments.

Table 6-11: Converter data used in experiments power loss estimation[14].

DC link voltage	*200V*	K_1	*0.231J/A*
		K_2	*1.16J*
IGBT rating	*600V*	R_{on}*(IGBT)*	*15.9mΩ*
Carrier frequency	*4 kHz*	R_D*(diode)*	*50mΩ*
V_{f0}*(IGBT)*	*1.07V*	V_{D0}*(diode)*	*1.1V*

Table 6-12: Summary of HCMC with two H-bridge cells in ac side conversion losses both in simulation and experiment.

	Simulation	Experiment			
Condition (1)	P_c=8.3W	P_{dc}=701W	V_{dc}=200V	P_f=675.8W	I_{line}=2.953A
	P_s=13.9W		I_{dc}=3.505A		V_{line}=145.2V
	P_{loss}=22.2W	P_{loss}=25.2W (3.59%)			
Condition (2)	P_c=7.9W	P_{dc}=750W	V_{dc}=200V	P_f=725.9W	I_{line}=2.9A
	P_s=12.5W		I_{dc}=3.75A		V_{line}=144V
	P_{loss}=20.4W	P_{loss}=24.1W (3.21%)			
Condition (3)	P_c=3.1W	P_{dc}=303.2W	V_{dc}=200V	P_f=292.5W	I_{line}=1.707A
	P_s=5.6W		I_{dc}=1.52A		V_{line}=97.02V
	P_{loss}=8.7W	P_{loss}=10.7W (3.52%)			

Note: P_f indicates the power associated with the fundamental frequency component.

From Table 6-12 the experimental conversion losses agree with those obtained using mathematical analysis. Compare to the mathematical analysis results, the experimental conversion loss values are increased in the experiments because the switching frequency is increased to 4kHz (f_s=1.35kHz in mathematical analysis) to obtain better quality of output voltage and current waveforms. The lack of H-bridge cells and due to synchronous issues when using independent control strategy, the switching losses increase dramatically.

6.6 Summary

Table 6-13: Conversion losses summary of the M2C and HCMC with cells in the ac side.

a) 20MVA at11kV and a power factor of 0.8 lagging (inverter with limited reactive power capability).

		M2C			
		3-level	5-level	9-level	17-level
a)	Conduction Loss (kW)	126.2	130.56	153.6	170.8
	Switching Loss (kW)	258.3	171.2	94.8	42.4
	Total Loss (kW)	384.5(1.92%)	301.76(1.51%)	248.4(1.24%)	213.2(1.06%)
		Hybrid Cascaded Multilevel Converter			
		2-cells	7-cells	10-cells	
a)	Conduction Loss (kW)	262.5	192.5	281.6	
	Switching Loss (kW)	120.9	84.93	83.8	
	Total Loss (kW)	354 (1.77%)	347.43(1.73%)	365.4(1.82%)	

b) 20MVA at 11kV and zero power factor (reactive power applications).

		M2C			
		3-level	5-level	9-level	17-level
b)	Conduction Loss (kW)	142.8	142.08	167.3	190.1
	Switching Loss (kW)	274.5	183.5	108.6	67.1
	Total Loss (kW)	417.3(2.02%)	325.58(1.62%)	275.9(1.37%)	257.2(1.28%)
		Hybrid Cascaded Multilevel Converter			
		2-cells	7-cells	10-cells	
b)	Conduction Loss (kW)	190.3	220.4	240.6	
	Switching Loss (kW)	108.7	80.5	73.7	
	Total Loss (kW)	299(1.5%)	300.9 (1.51%)	314.3 (1.57%)	

c) 20MVA at 11kV and unity power factor.

		M2C			
		3-level	5-level	9-level	17-level
c)	Conduction Loss (kW)	131.04	153.6	158.4	175.7
	Switching Loss (kW)	223.7	159.4	87.1	36.96
	Total Loss (kW)	354.74(1.77%)	313(1.56%)	245.5(1.22%)	212.7(1.06%)
		Hybrid Cascaded Multilevel Converter			
		2-cells	7-cells	10-cells	
c)	Conduction Loss (kW)	214.3	240.3	251.9	
	Switching Loss (kW)	109.5	98.4	83.6	
	Total Loss (kW)	323.8(1.61%)	338.7(1.69%)	335.5(1.67%)	

As the number of levels/cells increases, the effective switching frequency per switch decreases which leads to a switching loss reduction, while the conduction losses increase due to more switches conducting at any given time. For the M2C, it can be concluded that as the number of levels/cells increases, efficiency increases. For HCMC, it can be concluded that as the number of levels/cells increases, efficiency slightly decreases due to the increased number of devices are conducting over the fundamental cycle. However, the efficiency of HCMC is still higher than that of the conventional two-level converter.

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CHAPTER 7

7 Application of Multilevel Voltage Source Converters in High-Voltage Direct Current (HVDC) Transmission Systems

7.1 Introduction

Offshore wind farms have been identified as a key solution for combating global warming and meeting government renewable targets. An HVDC transmission system has a number of advantages for integrating large wind farms over conventional ac connection techniques, such as [1-3]:

1) Transmission distance is not limited by cable charging currents.
2) Power flow magnitude and direction are fully defined and controlled.
3) Fewer cables are required and the absence of a reactive power component in the dc system results in significant economic and environmental benefit.
4) Improved system fault ride through capability.

Of the two main dc transmission technologies, the voltage source converter, VSC, based HVDC scheme is superior to the LCC scheme in terms of [4, 5]:

1) Active power and reactive power can be controlled independently.
2) No voltage polarity reversal is required to reverse the power flow direction.
3) Black start capability.
4) Operation with weak and low short-circuit ratio ac networks, and with passive loads is possible.
5) Converters of the dc transmission system can provide leading or lagging reactive power that eliminates the need for reactive power compensation at converter stations.
6) Raised switching frequency allows reduction of harmonic filtering requirements.

HVDC transmission systems based on the VSC have been proposed for transmitting

power between conventional ac networks and offshore wind farms with reduced power losses and improved system stability. VSC-HVDC is suited to multi-terminal (MT) dc transmission systems for connecting different areas or wind farms dispersed over a wide area. However, control, operation and management of more than 2 grid side VSCs (GSVSC) is significantly more complex and challenging [6].

7.2 VSC-HVDC Operation and Control

7.2.1 System description

Figure 7-1 shows a two terminal VSC-HVDC link. The main function of the system is to transmit DC power from the rectifier side to inverter side. As shown in Figure 7-1, it consists of DC-link capacitors, two converter stations, high-pass filters, phase reactors, transformers and DC cable [7, 8].

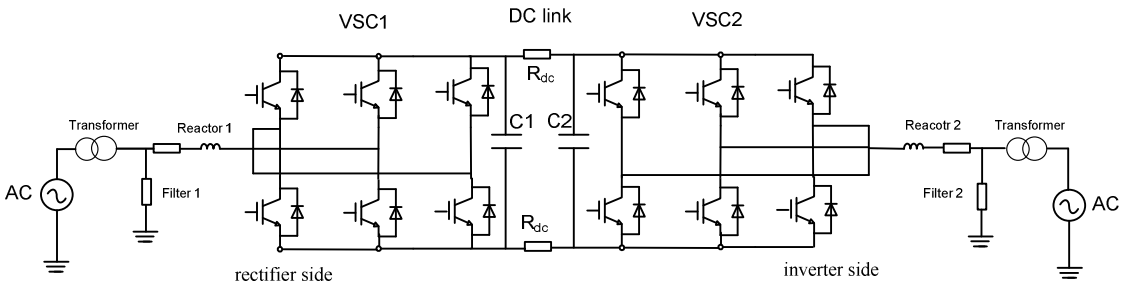


Figure 7-1: VSC-HVDC system topology.

- Converters

The converters are two level VSCs employing IGBT power semiconductors. One converter operates as a rectifier and the other as an inverter. The two converters are connected either back-to-back or through a dc cable, depending on the application [9].

- Transformers

Normally, the converters are connected to the ac system via a transformer. The most important function of the transformer is to transform the voltage of the ac system to a magnitude suitable for the converter. It can use a simple connection (two-winding instead of three to six-winding transformers used for LCC schemes). The leakage inductance of the transformer is usually in the range 0.1-0.2p.u [10].

- Phase reactors

The phase reactors are used for controlling both the active and reactive power flow by regulating the currents through them. The reactors also function as ac filters to reduce the high frequency current harmonics generated by the VSCs. The reactors are essential for both the active and reactive power flow, since these properties are determined by the power frequency voltage across the reactors. The reactors are usually about 0.1-0.2p.u. impedance [10].

- AC filters

The ac voltage output contains harmonic components, generated by the IGBTs switching action. These harmonics must not be injected into the ac system, cause malfunction of ac system equipment or cause radio and telecommunication disturbances. High-pass filter branches are installed to attenuate these high-order harmonics. With VSC there is no need to compensate any reactive power consumed by the converter itself and the current harmonics on the ac side are related directly to the PWM frequency. The low-order harmonic content in the current is small. Therefore the amount of filtering required in these converters is reduced dramatically in comparison to the requirement of naturally commutated converters.

- DC capacitors

On the dc side there are two capacitor stacks of the same capacitance. The size of the capacitors depends on the required dc voltage. The objective of the dc capacitor is primarily to provide a low inductance path for the turn-off current, and energy storage to enable control of power flow.

The dc side capacitor design is an important part of HVDC system design. Due to PWM switching action in the VSC-HVDC, the current flowing to the dc side of a converter contains harmonics, which result in ripple on the dc side voltage. The magnitude of the ripple depends on the dc side capacitance, current, and the switching frequency.

The design of the dc capacitor should not only be based on steady-state operation. During disturbances in the ac system (faults, switching action) large power oscillations may occur between the ac and dc sides. This in turn will lead to oscillations in the dc voltage and to dc over-voltages that may stress the circuit components. It is important to consider the transient voltage variation constraint

when the dc capacitors are selected. Small dc capacitance C_{dc} can be used, which should theoretically result in a faster converter response and provide energy storage for power flow control. The dc capacitance is characterized by a time constant τ, defined as the ratio between the stored energy at rated dc voltage and the nominal apparent power of the converter:

$$\tau = \frac{\frac{1}{2} C_{dc} V_{dcN}^2}{S_N} \tag{7.1}$$

Where V_{dcN} denotes the nominal dc voltage and S_N is the nominal apparent power of the converter. The time constant is equal to the time needed to charge the capacitor from zero the rated voltage V_{dcN} if the converter is supplied with a constant active power equal to S_N. The time constant τ is selected to be less than 5ms to satisfy the requirements of a small ripple and small transient over-voltage on the dc voltage, which will be verified by simulation. This relatively small time constant allows fast control of active and reactive power [10-12].

7.2.2 System operation

The fundamental operation of VSC-HVDC can be explained by considering a two terminal ac systems as two idea ac voltage source (Figure 7-2). On the inverter ac side, the converter can be modelled as a controlled voltage source V_{con2} and can be expressed as:

$$V_{con2} = \frac{1}{2} M V_{dc} \sin(\omega t + \varphi) + harmonics \tag{7.2}$$

Where M is the modulation index and φ is the power factor.

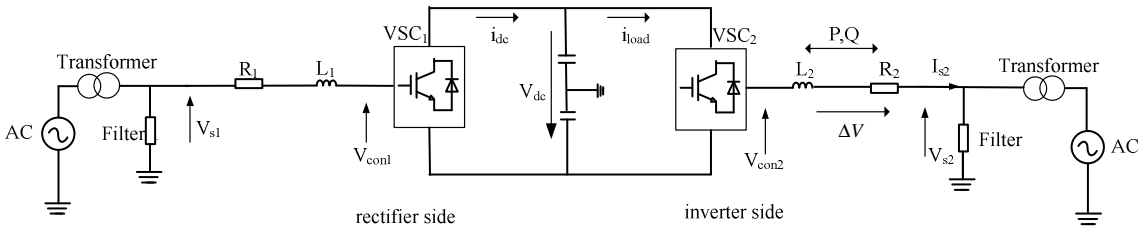


Figure 7-2: Basic structure of a VSC-HVDC system.

The active power P_2 and reactive power Q_2 of the converter station sent to the ac system is coupled with the impedance X_2, can be calculated using equations (7.3) and (7.4). The losses of the phase reactor are neglected.

$$P_2 = \frac{V_{con2} V_{s2} \sin \delta}{X_2} \tag{7.3}$$

The reactive power flow is determined by voltage drop ΔV shown in Figure 7-2 is related to the amplitude of converter's voltage V_{con2} as follows:

$$Q_2 = \frac{V_{s2}(V_{con2} \cos \delta - V_{s2})}{X_2} \tag{7.4}$$

Where δ is the angle between V_{con2} and V_{s2}.

The P-Q envelope depicted in Figure 7-3 presents the active and reactive power capability of the VSC-HVDC system, Ideally, a VSC is able to operate anywhere within the full circle. Practical limitations are applied, restricting the active and reactive powers to within limits (a VSC has local capacitive storage). The controllable active power can be transferred in both directions with equal maximum value [13-16].

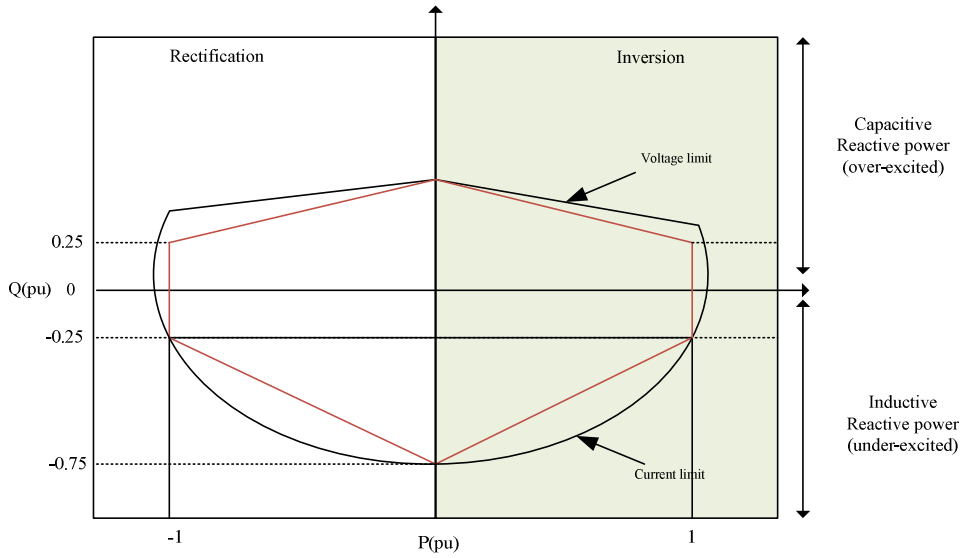


Figure 7-3: Active and reactive power capability curve of a VSC-HVDC system.

7.2.3 Control System

The VSC-HVDC control system shown in Figure 7-4 is based on two control loops: an inner current control loop controlling the ac current and an outer control loop controlling dc voltage, active power, reactive power and ac voltage or frequency, depending on the control strategy. The choice of which controller is used to calculate the converter current reference values depends on the application. If the load is a passive system, the VSC-HVDC can control frequency and ac voltage. If the load is an established ac system, the VSC-HVDC can control ac voltage and power flow [11, 17-21].

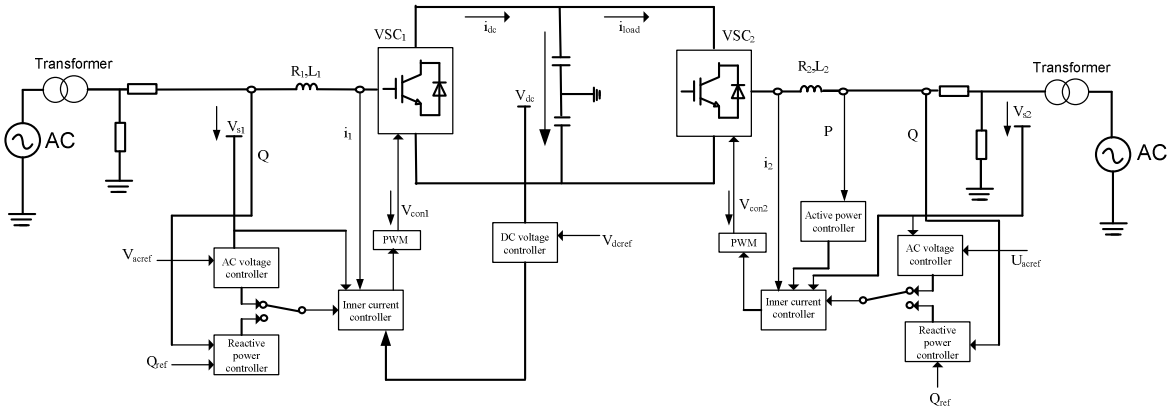


Figure 7-4: VSC-HVDC control system structure.

7.2.3.1 The inner current controller

The inner current control loop can be implemented in the *dq*-frame, using a two-phase rotating reference frame via Park's transform. In the control scheme analysis, the reference frame is selected so that the ac source voltage is on the d-axis. Therefore, active power exchange between the ac system and the dc link can be controlled by the *d*-axis current component, and the reactive power can be controlled by the *q*-axis current component [22-25].

From the Figure 7-4, the left-hand side converter station denoted by VSC_1 as a rectifier, and the right-hand side converter station denoted by VSC_2 operates as inverter.

For the rectifier, the voltage equations in the synchronous *d-q* frame are:

$$V_{s1}^{d} = R_1 I_1^{d} + L_1 \frac{di_1^{d}}{dt} - \omega L_1 i_1^{q} + V_{con1}^{d}$$
$$V_{s1}^{q} = R_1 I_1^{q} + L_1 \frac{di_1^{q}}{dt} + \omega L_1 i_1^{d} + V_{con1}^{q} \tag{7.5}$$

Instantaneous power extracted from the AC source to the DC link can be expressed as:

$$p_1 = \frac{3}{2}\left(V_{s1}^{d} i_1^{d} + V_{s1}^{q} i_1^{q}\right)$$
$$q_1 = \frac{3}{2}\left(V_{s1}^{d} i_1^{q} - V_{s1}^{q} i_1^{d}\right) \tag{7.6}$$

Where

$V_{s1}^{d,q}$ are the *d*- and *q*-axis components of the ac source voltage.

$i_1^{d,q}$ are the current components.

$V_{con1}^{d,q}$ are the converter voltage components.

R_1, L_1 are the equivalent resistance and inductance of transmission line.

ω is the source angular frequency.

Subscript '1' denotes quantities relating to VSC_1 and subscript '2' denotes quantities relating to VSC_2.

For the inverter VSC_2 in Figure 7-4, the voltage equations in the synchronous *d-q* frame are:

$$V_{con2}^{d} = R_2 I_2^{d} + L_2 \frac{di_2^{d}}{dt} - \omega L_2 i_2^{q} + V_{s2}^{d}$$
$$V_{con2}^{q} = R_2 I_2^{q} + L_2 \frac{di_2^{q}}{dt} + \omega L_2 i_2^{d} + V_{s2}^{q} \tag{7.7}$$

The transformation from the three-phase system to the *dq*-frame is:

$$X_{dq0} = KX_{abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{7.8}$$

Where X can be either the voltage or current of a converter station.

7.2.3.2 The outer controller

- DC voltage controller

The aim of voltage control is to regulate the converter output voltage at the reference value as the converter outputs the required active power into the ac grid. At the dc side, the dc capacitor supports the dc bus voltage and the dc cable or line is the channel for the active power flow. The energy stored in the capacitor varies (fluctuates) if the active power is not in balance between the two sides of the VSC station. Fixed dc voltage control maintains the dc voltage by changing the active power exchanged between the VSC and the ac grid.

The dc link voltage V_{dc} is sensed and compared to the voltage reference V_{dc_ref}, as shown in Figure 7.5. The resulting error yielded feeds a PI controller which generates the reference I_{d_rer} for the ac active power currents in the synchronous rotation frame. In this control scheme, the output dc voltage is controlled by the outer voltage loop, and the inner feed forward decoupled PI current regulators ensure that the input ac currents track their references. VSC_2 operates as the dc controller.

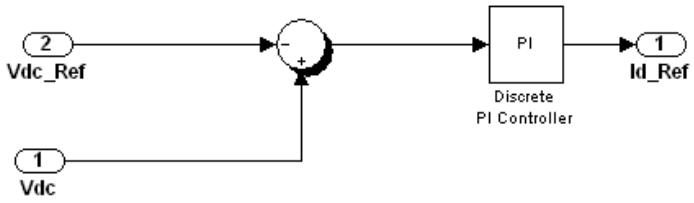


Figure 7-5: DC voltage controller.

- Active power controller

An active power controller is used to specify the power to be exported or imported between the two active systems. VSC_1 operates as the active power controller. The principle is illustrated by Figure 7-6:

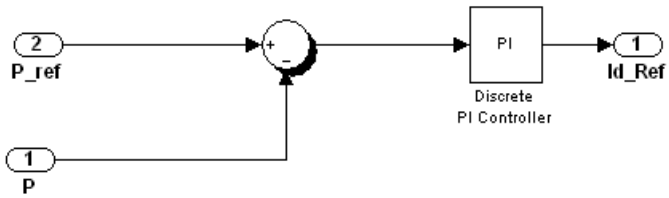


Figure 7-6: Active power controller.

P_{ref} is the active power reference. The active power error term (P_{ref} -P) is passed through a PI controller to generate the reference value of d-axis current component i_{ref1}^{d}. If more accurate control of the active power is needed, a combination of a feedback and open loop control can be used.

- Reactive power controller

The reactive power controller is similar to the active power controller.

- The ac voltage controller

As shown in the Figure 7-2, the voltage drop ΔV across the reactor X_2 can be described as:

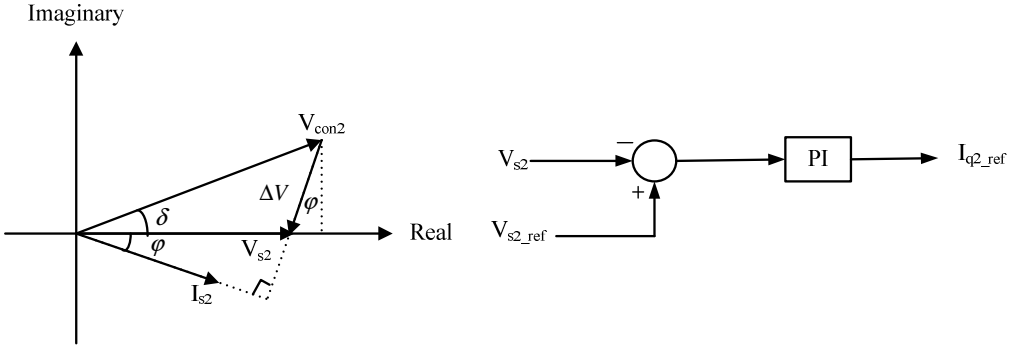
$$\Delta V = V_{con2} - V_{s2} = \Delta V_p + j\Delta V_q$$
$$= \frac{R_2 P + X_2 Q}{V_{s2}} + j\frac{X_2 P - R_2 Q}{V_{s2}} \tag{7.9}$$

If $\Delta V_q \ll V_{s2} + \Delta V_p$

Then

$$\Delta V \approx \frac{R_2 P + X_2 Q}{V_{s2}} \tag{7.10}$$

For ac networks most power circuits satisfy $X_2 \gg R_2$, therefore the voltage drop ΔV is considered to depend only on the reactive power flow Q. The phasor diagram and block diagram of the ac voltage controller follow:



Where δ is the angle between V_{con2} and V_{s2}. φ is the power factor.

Figure 7-7: Phasor diagram and ac voltage controller.

- The frequency controller

The purpose of the frequency controller is to maintain the converter output frequency at its reference value. The change in power for a given change in frequency in an interconnected system is known as the 'stiffness' of the system [26]. The power-frequency characteristic can be approximated by a straight line, whence it is feasible to use a PI controller in the feedback loop of the frequency and the control error can be reduced to zero in steady state. The block diagram of the frequency controller is shown in Figure 7-8:

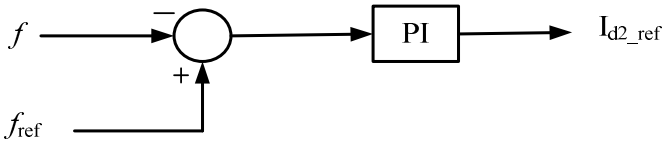


Figure 7-8: Frequency controller.

7.3 Multi-terminal (MT) HVDC system operation and Control

7.3.1 System outline

Figure 7-9 shows the multi-terminal (MT) HVDC system layout. The system consists of four terminals with two WFVSCs and GSVSCs. The four terminals are connected by four dc cables but other connection arrangements are also applicable, such as connection to one common point.

The WFVSCs control the ac voltage seen by the wind generators. The wind generators (and their power converters) act to extract the maximum energy. The HVDC link collects the wind farm energy, having been converted from ac to dc. The dc power is then transmitted to the GSVSCs via dc cables. The two GSVSCs transfer the dc power into the respective AC grids, according to pre-defined arrangements. In addition, they also provide reactive power/ac voltage control for the connected grids. This support feature can be useful as the grid network at the point of connection is sometimes weak, with a low short circuit ratio (SCR). A high-frequency filter (HFF) is connected at each VSC output terminal to absorb the high-frequency harmonics generated by the converters [6, 27-36].

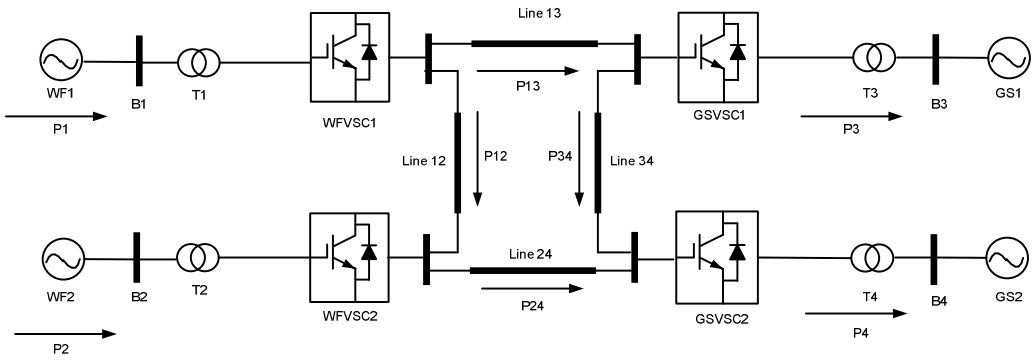
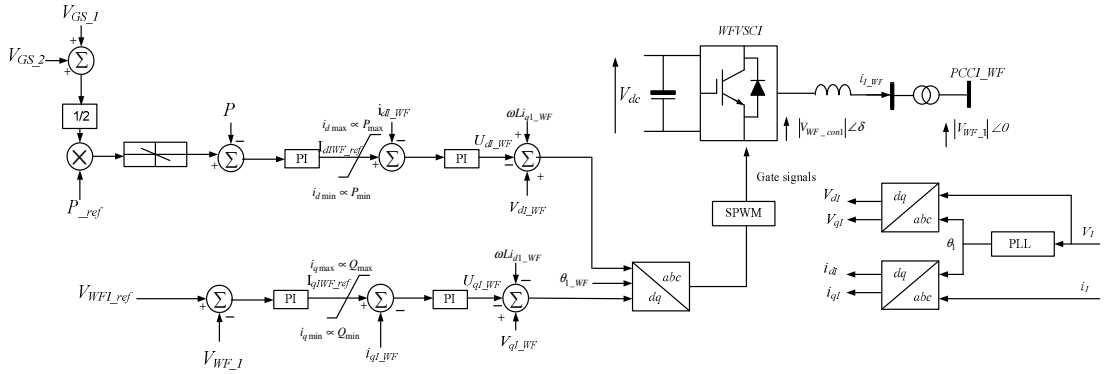


Figure 7-9: Layout of the proposed MT-HVDC system.

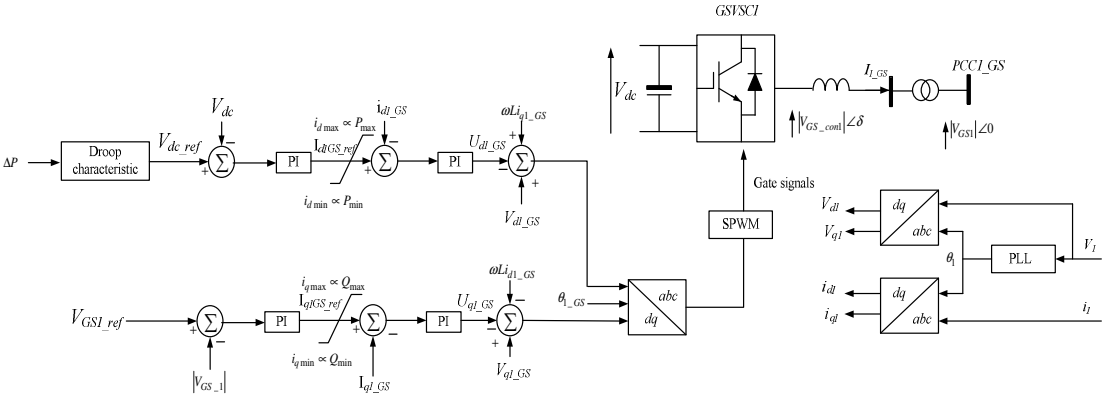
7.3.2 Control system

Depending on the operating arrangement, different control strategies can be employed for an MT-HVDC system. In the MT-HVDC transmission system in Figure 7-9, converters $WFVSC_1$ and $WFVSC_2$ are assigned to control the active power flow, while converters $GSVSC_1$ and $GSVSC_2$ control the dc link voltage.

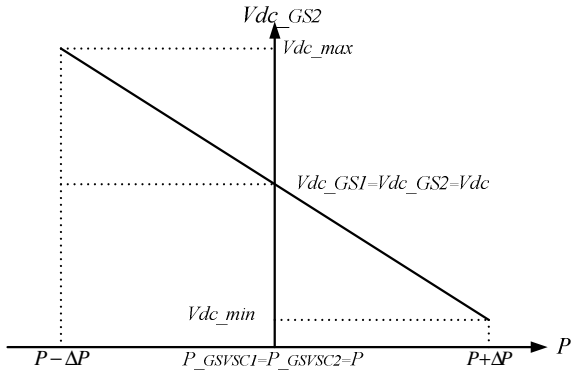
Figure 7-10a shows the control system for converter $WFVSC_1$ which is also applicable to $WFVSC_2$. The control scheme uses a standard decoupled *d,q* strategy to control active and reactive power with feed-forward terms to improve system disturbance rejection. Active power control allows the converters to adjust the active power command proportionally to the average reduction in the voltage magnitudes at buses B_3 and B_4. A rate limiter is used to control the power slope during active power ramping. Figure 7-10b shows the control system for converter $GSVSC_1$ which is also applicable to $GSVSC_2$. The detail of the active power-dc voltage droop is shown in Figure 7-10c. Voltage droop control can be used to distribute the power to different ac nodes via the HVDC link. In some circumstances droop control of the GSVSCs could be arranged to transfer real power to the HVDC link, where this power must be compensated by another GSVSC (or accepted by a wind farm, for instance when providing power to black start the wind farm). In normal operation, $GSVSC_1$ and $GSVSC_2$ equally share the power delivered from the WF side, and droop control is designed for active power exchange between $GSVSC_1$ and $GSVSC_2$ according to the dc voltage change ΔP is the active power that can be exchanged between converters $GSVSC_1$ and GSVSC2.



(a)



(b)



(c)

Figure 7-10: (a) and (b) control system of the converter station in wind farm side and grid side, (c) active power-dc voltage droop characteristic.

The relationship between ΔP and the reference dc voltage of converter $GSVSC_2$, when the dc link of the converters $GSVSC_1$ is held at V_{dc}, is given by equation (7.11) [31, 34]:

$$V_{dc4} = \frac{1}{2}V_{dc} + \sqrt{\frac{1}{4}V_{dc}^2 - R\Delta P} \tag{7.11}$$

Where R is the effective resistance of the line connecting $GSVSC_1$ and $GSVSC_2$.

Therefore inclusion of an active power-dc voltage droop characteristic allows converters $GSVSC_1$ and $GSVSC_2$ to respond to any load demand irrespective of their control mode [35, 37].

7.4 Simulations

To analyse to proposed control system, three simulations were performed:

- Five-level M2C in a two terminals HVDC system.
- Hybrid Cascaded Multilevel Converter with 7 cells in the ac side, in a two terminals HVDC system.
- Two-level converter in a four terminals MT-HVDC system.

The study is focused on the performance of the VSC-HVDC at steady state, load change and disturbances in supplying network and grid side.

7.4.1 Five-level M2C in an HVDC Transmission system

As shown in Figure 7-11, all simulations were performed with two five-level M2C converters. In wind energy generation, a doubly-fed induction generator (DFIG) or a full sized converter are usually adopted, hence network frequency variations have no direct influence on power generation. The wind farms are therefore substituted by an infinite voltage source with a constant voltage amplitude and phase angle. The ac system voltage on both sides is 230kV 2000MVA, and the rated dc voltage is 275kV [38].The reactor is 0.12 p.u. and the converter switching frequency is 2.1kHz. The power flow directions are assumed positive. The active and reactive power capability is as shown in Figure 7-3.

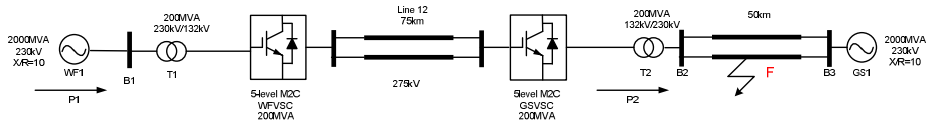


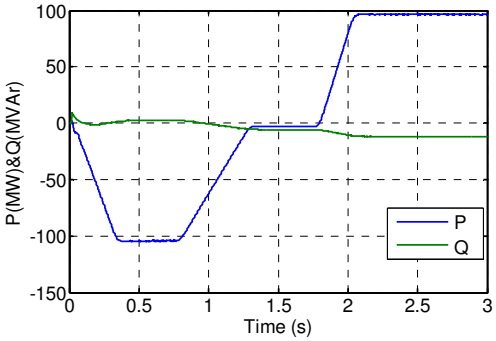
Figure 7-11: Test system of five-level M2C based HVDC system.

Case I: Steady-state performance and active power reversal

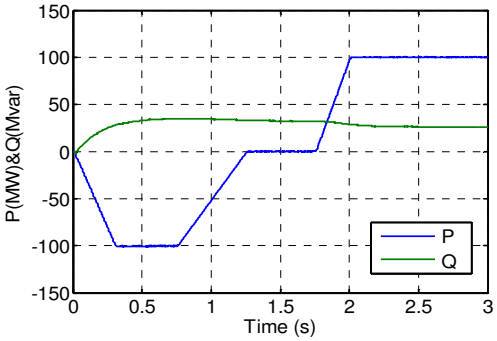
Figure 7-12 illustrates system performance when the system exports 100MW from the grid side (GS) to wind farm (WF). From t=0.75s, the system is switched to a 'sleep' mode which means two converter stations operate as two independent STATCOMs regulating the ac voltage at buses B_1 and B_2. At t=1.75s, the active power is reversed, with the GS receiving 100MW active power from the WF side as can be seen in Figures 7-12 a and b. The dc voltage in the GS converter is stabilized at 275kV, while in the WF side there is a small step change due to active power reversal shown in Figure 7-12c. The system is stable with the voltage stresses across the switching devices controlled during the entire operating period. Also there is an absence of high and low frequency harmonic components from the dc link current. This means that dc filters are not required. An expanded view of dc current without ac filtering is shown in Figure 7-12d. Figures 7-12e and f show the current waveforms at bus B_2 and its expanded waveform. As can be seen, the M2C produces high quality current waveform. Figure 7-12h shows the line voltage at the converter terminals, confirming the interfacing transformers of both converters experience low voltage stress compared to those on a conventional two-level converter. This is due to switching of relatively small voltage steps, at a reduced switching frequency per device.

Case II: Transient performance on load change and three-phase fault

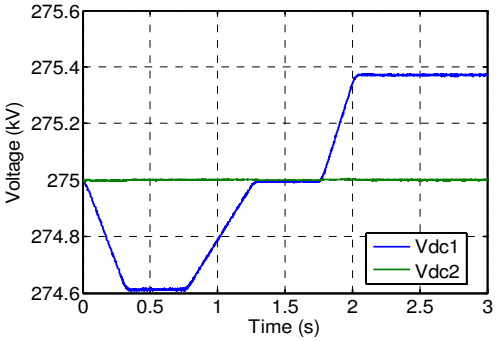
To evaluate the transient performance of an M2C based HVDC system, the system in Figure 7-11 experiences a load change of 100+j60 MVA at the GS load and a three-phase fault at point F with a duration of 140ms. The results are shown in Figure 7-13. The HVDC system using an M2C is able to recover from a solid three-phase fault at point F without difficulty in terms of voltage stress on the converter switches that may result from cell capacitor voltage balancing problems or current stresses. Observe from Figures 7-13a and b that converter VSC_2 has responded to the sudden increase in reactive power demand due to the introduction of the 100+j60 MVA load at bus B_2 when t=0.75s while this sudden change at bus B_2 doesn't affect bus B_1. The occurrence of the three-phase fault at point F at t=1.6s. The duration of this fault is 140ms. Figure 7-13c shows that dc fault voltage at VSC_2 terminal is limited which proves the feasibility of the proposed control strategy.



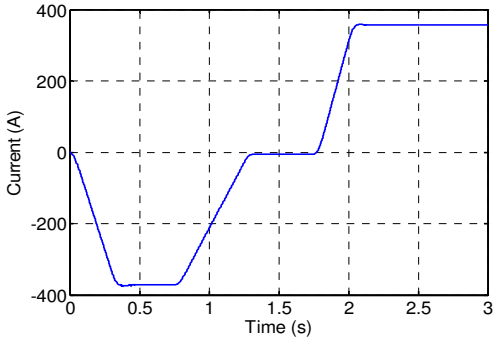
(a) Active power and reactive power at bus B_1.



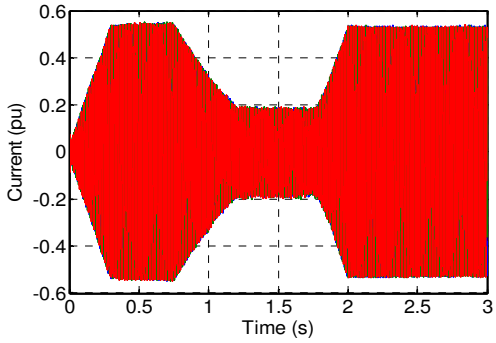
(b) Active power and reactive power at bus B_2.



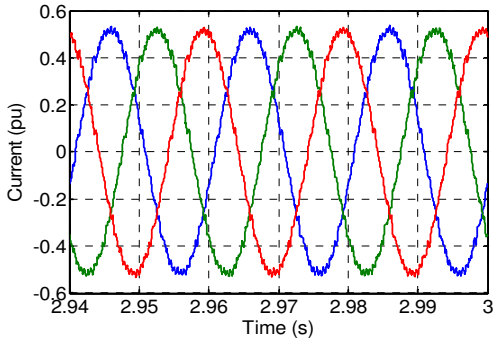
(c) DC voltage of the converter VSC_1 and VSC_2.



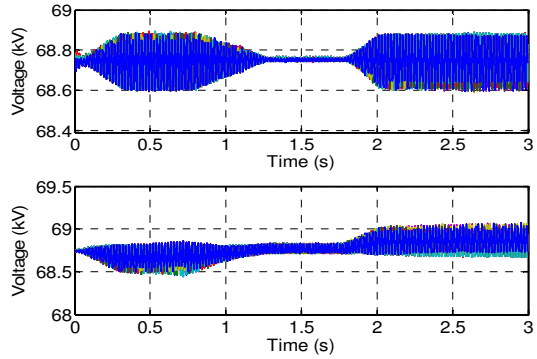
(d) Current in the dc line.



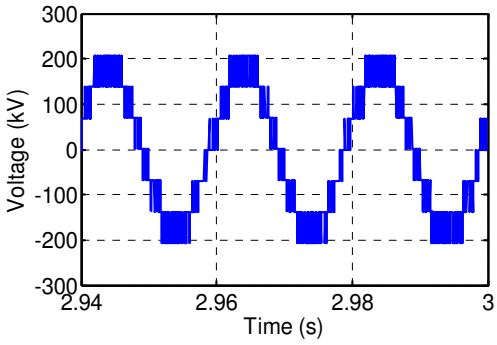
(e) Current waveforms at bus B_2.



(f) Expanded current waveforms at bus B_2.

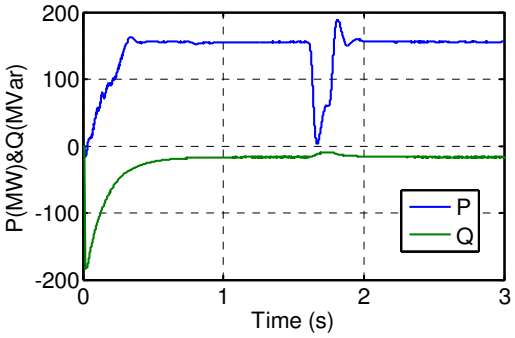


(g) Voltage across cell capacitors of converter VSC_1 and VSC_2.

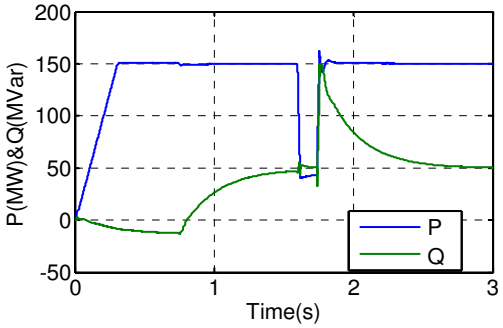


(h) Line Voltage waveform at converter VSC_2.

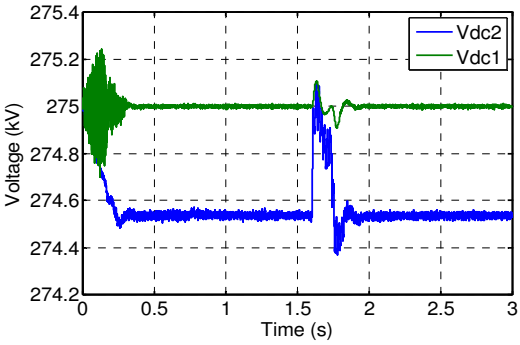
Figure 7-12: Simulation waveforms for steady-state five-level M2C HVDC system.



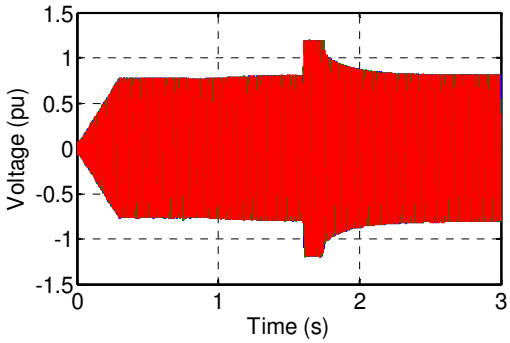
a) Active power and reactive power at bus B_1.



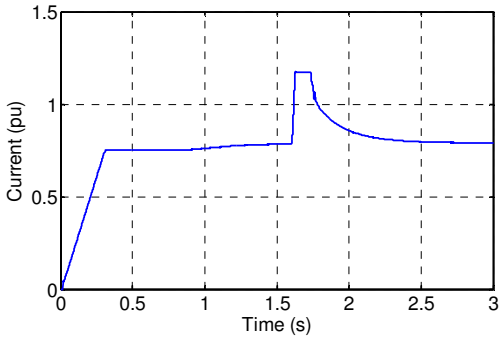
b) Active power and reactive power at bus B_2.



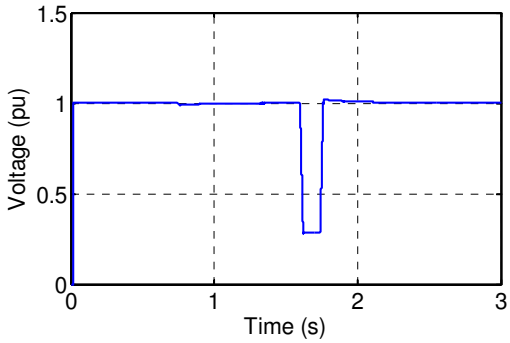
c) DC link voltage at converter VSC_1 and VSC_2.



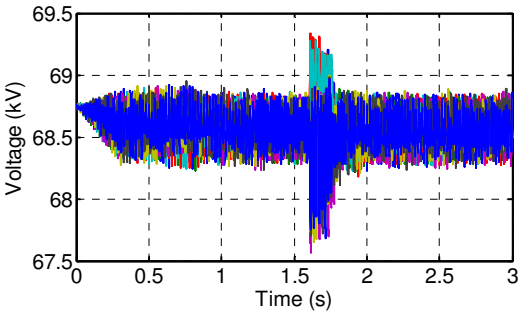
d) Current waveforms at bus B_2.



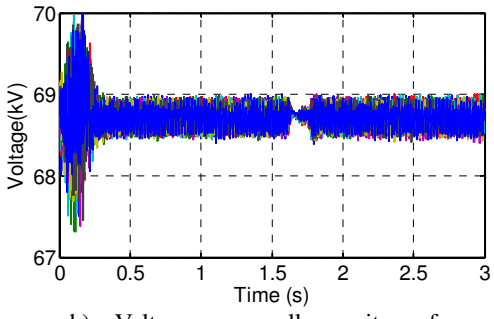
e) Current waveforms at bus B_2.



f) Voltage magnitude of bus B_2.



g) Voltage across cell capacitors of converter VSC_2.



h) Voltage across cell capacitors of converter VSC_1.

Figure 7-13: Simulation waveforms showing transient performance of a five-level M2C HVDC system.

The peak current during the fault period is controlled, as can be seen in Figures 7-13d and e; this may allow converter VSC_2 to provide the necessary reactive power support to the GS ac network provided the fault remains to prevent voltage instability at the network GS, without increasing the risk of converter switch over-current. Figure 7-13f shows the decrease in voltage magnitude of bus B_2 to 0.3 p.u. during the fault, and its recovery immediately after the fault is clear. Capacitor voltage in both rectifier and inverter remains stable as shown in Figures 7-13g and h.

7.4.2 HCMC with 7 cells in the ac side in a HVDC Transmission System

To demonstrate the hybrid multilevel converter with ac side cascaded H-bridges in HVDC applications, a three-phase HCMC with a 275kV dc link voltage and 7 cells (with 4mF cell capacitance, each blocking 19.6kV, and capable of generating 29 voltage levels as shown in Figure 7-14), is simulated. In this case, the cascaded H-bridge cells are controlled using multilevel PWM with a 1.35kHz switching frequency.

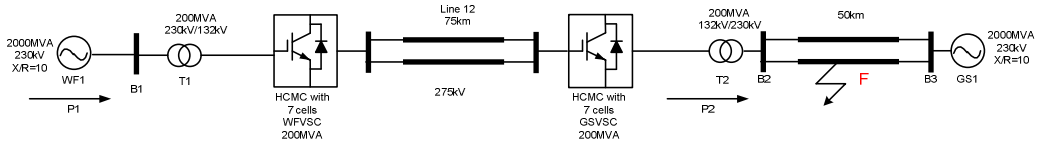
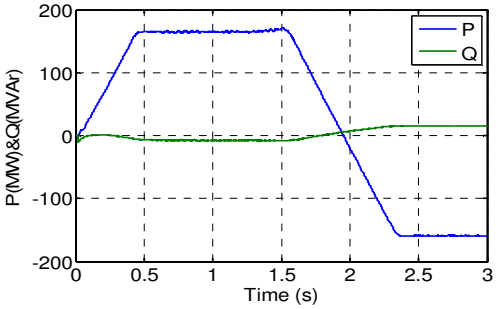


Figure 7-14: 200MW 275kV HVDC system based on HCMC with 7 cells in the ac side.

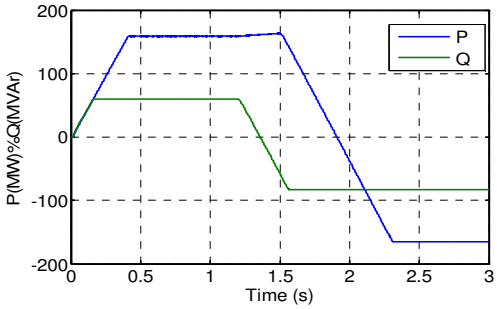
Case I: Steady-state performance and active power reversal

Figure 7-15 illustrates the steady-state performance of the HCMC with 7 cells in the ac side, with an active power reversal command. VSC_1 is commanded to ramp up the exported active power from 0 to 160MW within 0.4s. During the same period, a reactive power command is given to the VSC_2 to increase reactive power exchange with the grid from 0 to 60MVAr (inductive) within 0.15s. At t=1.2s, another reactive power command is given to the inverter to change the reactive power exchange with the grid from 60MVAr (inductive) to 80MVAr (capacitive) within 0.35s. At t=1.5s, another active power command reverses the power flow from 160MW to -160MW within 0.8s, the dc current correspondingly reverses the direction and dc voltage at VSC_2 terminal increases by 0.6 kV and then decreases to 274.4kV to response to the power command, which can be seen from Figures 7-15a to d. Figure 7-15g shows

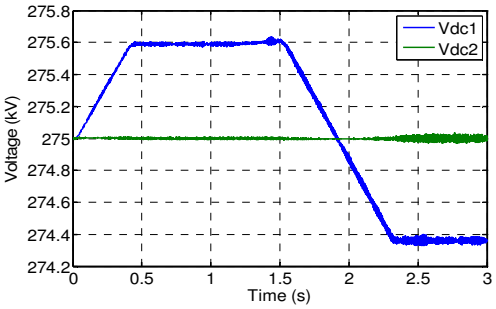
voltage balance across the H-bridge cells is sensitive to reactive power change (magnitude and direction), due to cell capacitor voltage balancing depending on the small active power component during the reactive power change. This dependence may limit the converter from rapidly recovering from some faults.



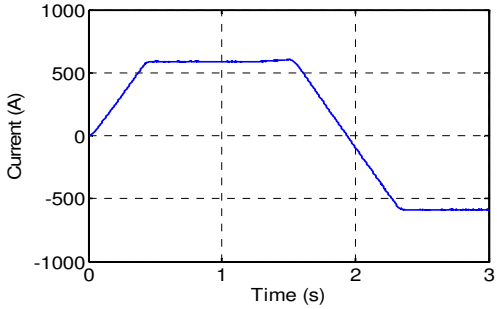
a) Active power and reactive power at bus B_1.



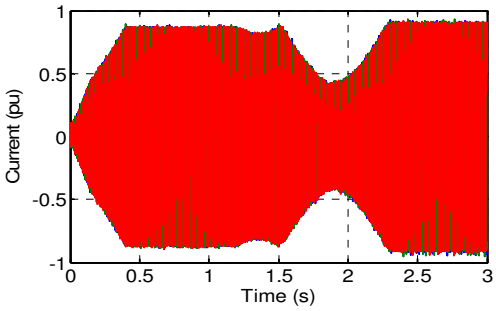
b) Active power and reactive power at bus B_2.



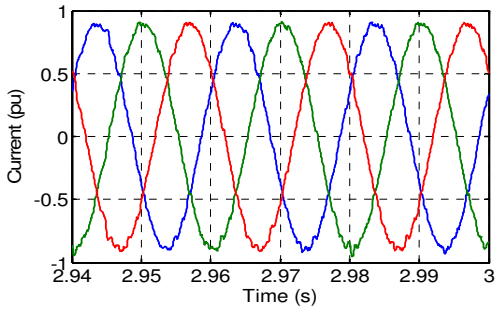
c) DC voltage of the converter VSC_1 and VSC_2.



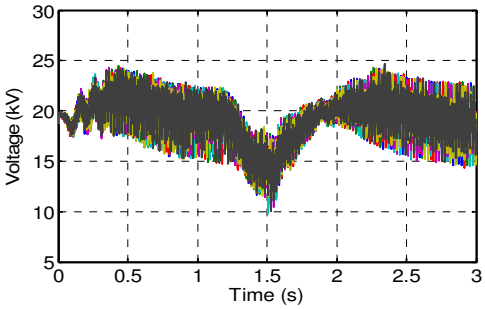
d) Current in the dc line.



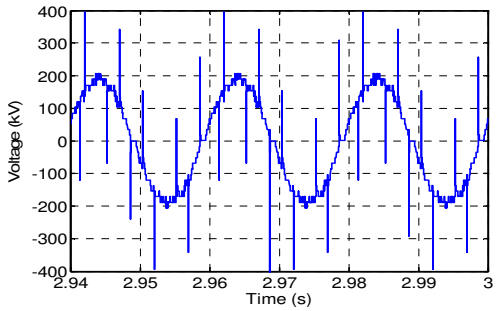
e) Current waveform injected into bus B_2.



f) Expanded current waveforms at bus B_2.



g) Voltage across H-bridge cell capacitors of VSC_2.



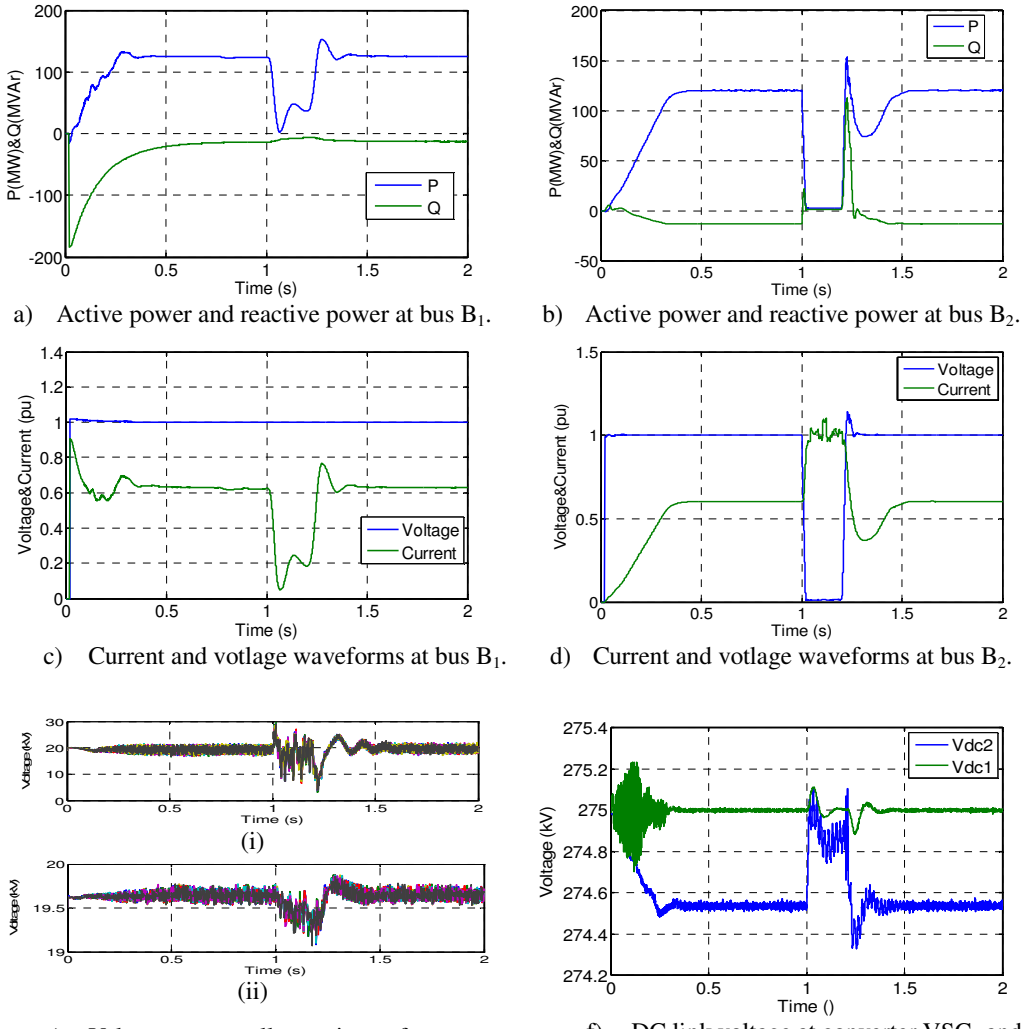
h) Line-to-line Voltage waveform at converter terminal before the interfacing inductor.

Figure 7-15: Key waveforms of the steady-state of an HCMC with 7 cells in the ac side in a 275kV HVDC system.

The line voltage contains spikes, as shown in Figure 7-15h, can be eliminated using an interfacing reactor or small ac filter.

Case II: Transient performance on three-phase fault

To demonstrate hybrid converter ac side fault response, the system in Figure 7-11 is subjected to a three-phase fault of 200ms duration at point F in the middle of the line. The simulation results are shown in Figure 7-16.



a) Active power and reactive power at bus B_1.

b) Active power and reactive power at bus B_2.

c) Current and votlage waveforms at bus B_1.

d) Current and votlage waveforms at bus B_2.

(i)

(ii)

e) Voltage across cell capacitors of converter VSC_2 (i) and VSC_1(ii).

f) DC link voltage at converter VSC_1 and VSC_2.

Figure 7-16: Key waveforms of the transient performance of an HCMC with 7 cells in the ac side in a 275kV HVDC system.

During the ac fault, due to the significantly reduced ac voltage, the active power generated by the wind farm is reduced by the power command given to converter

VSC_1, which is made sensitive to any change of voltage magnitude on bus B_1 and B_2 as can be seen in Figures 7-16a and d. Capacitor voltage magnitudes in both the rectifier and inverter remain stable as shown in Figure 7-16e. This prevents trapped energy in the dc link causing the dc link voltage to rises dramatically as shown in Figure 7-16f. The system remains stable during the fault period. When the fault is cleared, the system recovers rapidly within 200ms.

7.4.3 Four-terminal HVDC system

In order to demonstrate the validity of the proposed control strategy, the four-terminal system in Figure 7-9 is simulated. Converters $WFVSC_1$ and $WFVSC_2$ control active power and $GSVSC_1$ and $GSVSC_2$ regulate the dc link voltage at 275kV. $GSVSC_2$ incorporates dc voltage droop control to enable active power sharing between $WFVSC_1$ and $WFVSC_2$ at any ratio. The converters are modelled as 300MVA two-level converters using SPWM with a carrier frequency of 2.1kHz. The system rating is shown in Figure 7-17, where the power flow directions indicated are assumed positive.

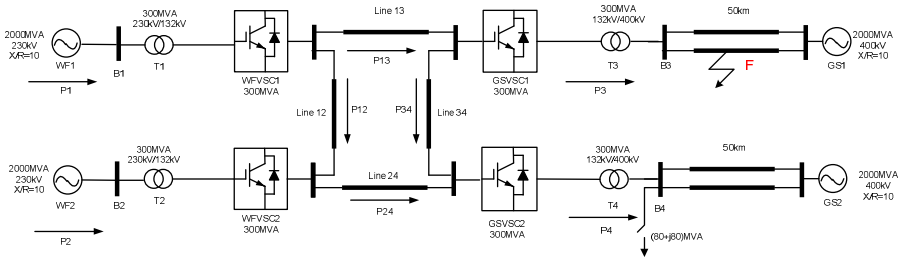
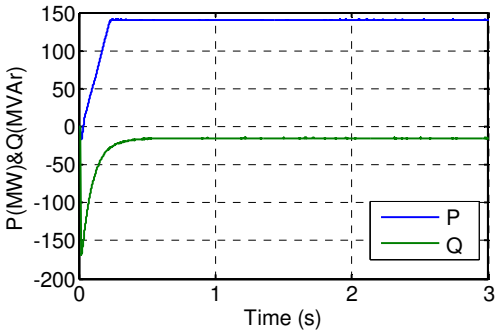


Figure 7-17: Four-terminal voltage source converter DC transmission system.

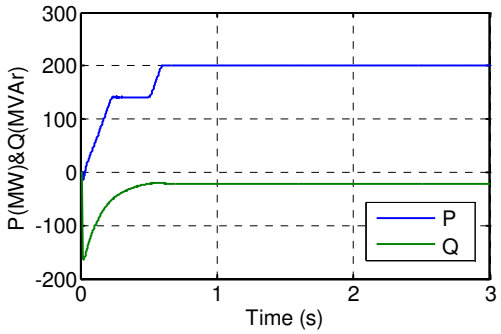
Case I: Steady-state performance and active power management

In order to evaluate the proposed active power-dc voltage droop characteristic in the power management control strategy, the four-terminal system shown in Figure 7-17 is simulated. Initially, both $WFVSC_1$ and $WFVSC_2$ export 140MW, and after t=0.5s, VSC_2 starts to export 200MW while the active power exported by $WFVSC_1$ remains 140MW as shown in Figures 7-18a and b. Under this operational condition, both $GSVSC_1$ and $GSVSC_2$ regulated the terminal dc voltage at 275kV which means $GSVSC_1$ and $GSVSC_2$ share the active power exported from the wind farm side while there is no active power flow between $GSVSC_1$ and $GSVSC_2$ as shown in Figure 7-18h. At time t=0.8s, the active power-dc voltage droop control of converter

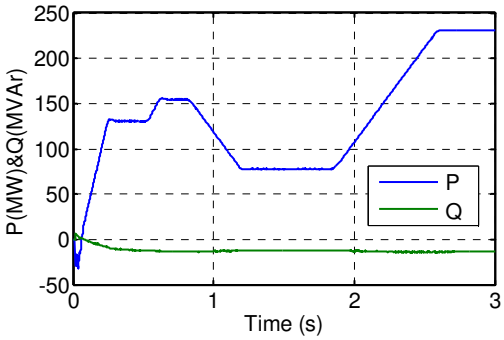
$GSVSC_2$ is activated to increase the active power delivered to converter $GSVSC_2$ by 70MW by reducing the dc link voltage of converter $GSVSC_2$ to 0.2kV.



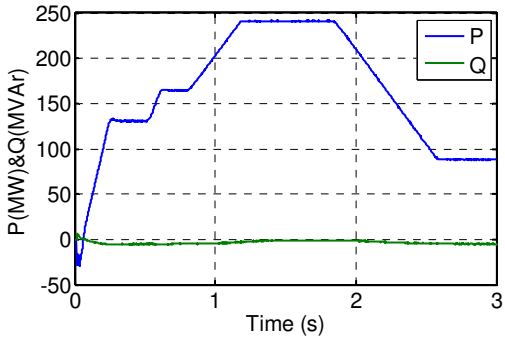
a) Active and reactive power at bus B_1.



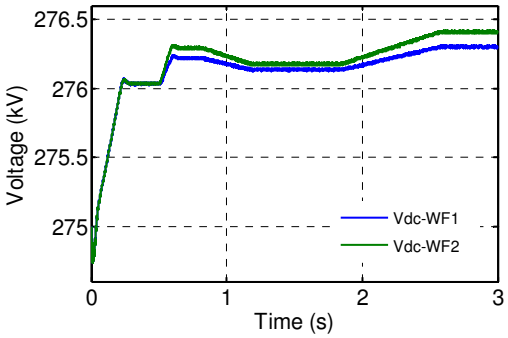
b) Active and reactive power at bus B_2.



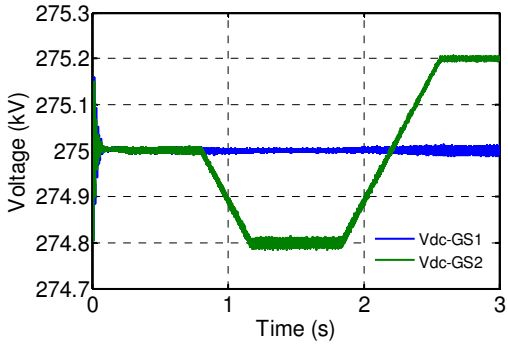
c) Active and reactive power at bus B_3.



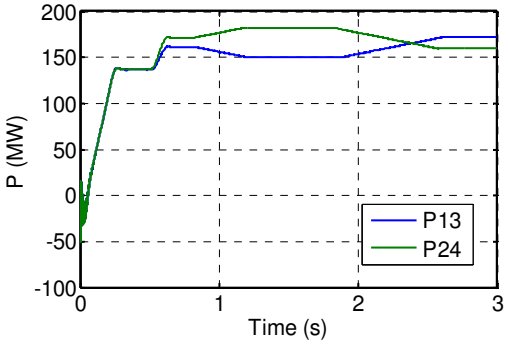
d) Active and reactive power at bus B_4.



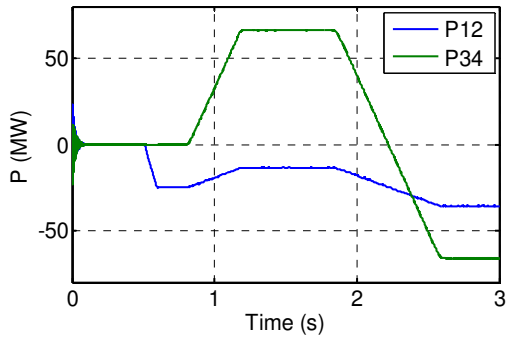
e) DC link voltage at WF_1 and WF_2.



f) DC link voltage at GS_1 and GS_2.



g) Power flow in the dc link (P_{13} and P_{24}).



h) Power flow in the dc link (P_{12} and P_{34}).

i)

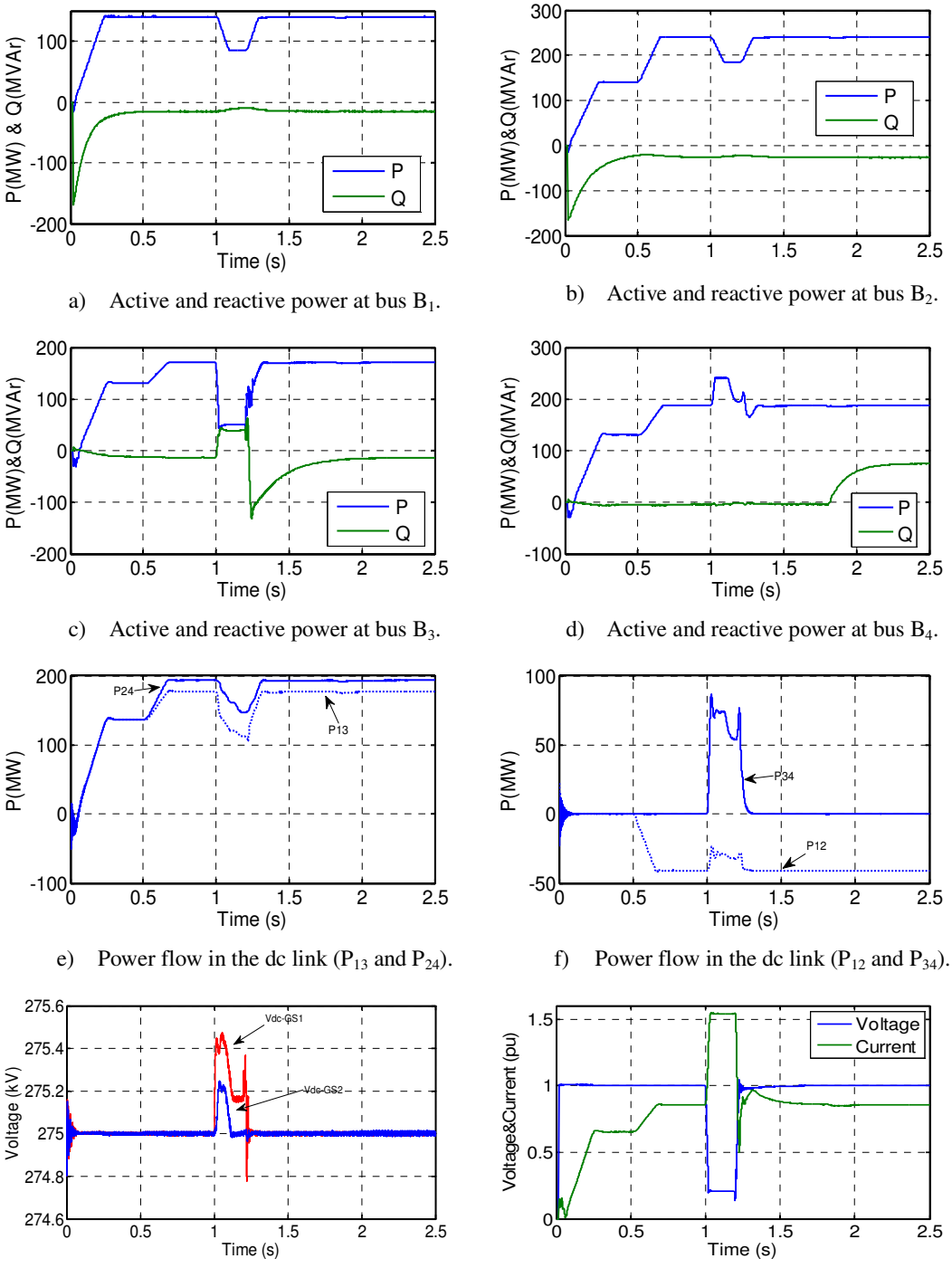
Figure 7-18: Waveforms demonstrating power management using active power-dc voltage droop characteristic.

During this period, the dc link voltage of $GSVSC_1$ remains at 275kV which leads to active power flow from $GSVSC_1$ to $GSVSC_2$ as shown in Figure 7-18c to f. At time t=1.5s, another power command to converter $GSVSC_2$ reverses the active power sharing. The active power delivered to $GSVSC_2$ is decreased to 90MW while the active power delivered to $GSVSC_1$ increases to 230MW. This command is activated by increasing the dc link voltage of $GSVSC_2$ by 0.2kV as shown in Figure 7-18f. Figure 7-18g and Figure 7-18h show the power flow between the four converter stations. These results establish the effectiveness of active power-dc voltage droop control for power management in multi-terminal dc transmission systems.

Case II: Transient performance on load change and ac side fault

This section investigates the response of the multi-terminal dc transmission system in Figure 7-19 to a load change at bus B_4 and a solid three-phase fault at point F. Both $WFVSC_1$ and $WFVSC_2$ export 140MW initially. After t=0.5s, $WFVSC_2$ starts to export 240MW as shown in Figure 7-19a and b. At t=1s the system is subjected to a three-phase fault at point F with a duration of 200ms and at t=1.8s a load of 80+j80 MVA is connected to bus B_4. The system responds to these events without affecting the overall system stability. The system treats the introduction of 80+j80 MVA load at bus B_4 as a local event, and its impact is limited to GS_2. As a result, converter $GSVSC_2$ increases it reactive power output in order to support the voltage at bus B4 as shown in Figure 7-19c and d. The impact of the three-phase fault at point F is universal, for two reasons. The first reason is that during the fault period, the active power transfer capability of converter $GSVSC_1$ is significantly reduced as the voltage magnitude at bus B_3 collapses to 20% of the nominal value as shown in Figure 7-19h. This causes the dc link voltage of converter $GSVSC_1$ to rise, transferring the active power that cannot be delivered through converter $GSVSC_1$ to $GSVSC_2$ as can be seen in Figure 7-19f and g. As a result, the power delivered through $GSVSC_2$ increases during the fault period shown in Figure 7-19d. The second reason is that the adopted recovery strategy compromises the decoupling feature of a VSC-HVDC transmission system in favour of minimizing the dc side trapped energy in order to reduce any converter voltage stresses due to a sudden rise of the dc link voltage. Figure 7-19d to Figure 7-19f show transient active power flow between dc links during a three-phase fault. Adjustment of the power commands to the converters controlling the active power, successfully limits the dc link voltage rise at the

terminal of converter GSVSC$_1$. Figure 7-20b shows the expanded view of the current injected into bus B$_3$ during the fault period.



a) Active and reactive power at bus B$_1$.

b) Active and reactive power at bus B$_2$.

c) Active and reactive power at bus B$_3$.

d) Active and reactive power at bus B$_4$.

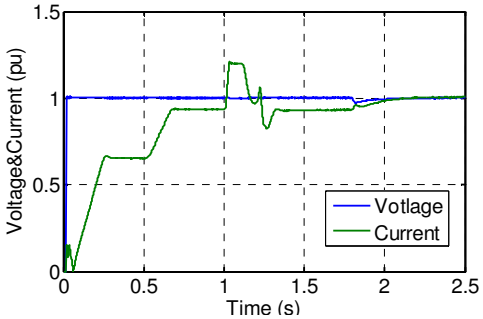
e) Power flow in the dc link (P$_{13}$ and P$_{24}$).

f) Power flow in the dc link (P$_{12}$ and P$_{34}$).

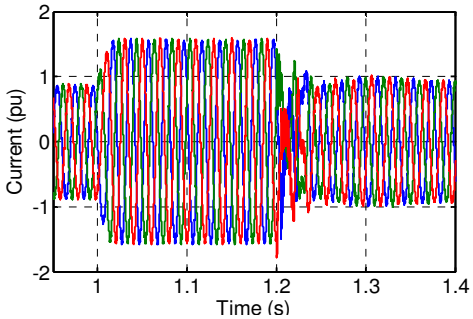
g) DC link voltage at GS$_1$ and GS$_2$.

h) Voltage and Current magnitude at B$_3$.

Figure 7-19: Simulation waveforms showing system performance during a load change at bus B$_4$ and a three-phase fault at point F.



a) Voltage and Current magnitude at B_4.



b) Current injected by converter $GSVSC_1$ into bus B_3 during three-phase fault at point F.

Figure 7-20: Simulation waveforms showing system performance during a load change at bus B_4 and a three-phase fault at point F.

7.5 Summary

This chapter investigated multi-level voltage source converters in HVDC and multi-terminal dc Transmission system applications. Using PWM control of a voltage source converter enables independent control of real and reactive powers within the system limits. Different controllers can be used depending on the application. The five-level M2C based HVDC system simulation results show this HVDC system is able to operate over the entire specified P-Q capability curve. By using a higher level M2C converter, the ac and dc filters, and interfacing reactor might be eliminated due to the low *dv/dt* experienced by the switches in the future. It can also be concluded that an M2C based HVDC system is capable of riding through any ac faults without posing any risk to the converter switches from over-voltage or over-current. Using the hybrid cascaded multilevel converter does not compromise black start capability and eliminates the need for start-up equipment to charge and discharge the H-bridge cell capacitors. The hybrid cascaded multilevel converter offers the feature of dc fault reverse blocking capability, since it is able to block active power exchange between the ac and dc sides, and reactive power between converters and the ac side. In a multi-terminal HVDC system, the proposed control strategy improves control flexibility and allows the converter controlling the dc voltage to respond to any power demand. The strategy minimizes converter over-voltage on the dc side, hence minimizes the dc side trapped energy, thus eliminating the need for a dc chopper on the dc side.

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CHAPTER 8

8 Conclusions

8.1 General Conclusion

The multi-level converter is the backbone of HVDC transmission system development, having better output waveform quality with lower harmonic content when compared to a conventional two-level converter. Additional advantages are the small ac side filter requirement and lower conversion loss. This thesis reports the investigation of two multi-level converter topologies: the Modular Multi-level Converter (M2C) and the Hybrid Cascaded Multi-level Converter (HCMC), both of which can be deployed in HVDC systems. A general review of multi-level converter types and their open-loop modulation techniques has been presented. A generalized approach for conversion loss calculation with carrier-based pulse width modulation has been studied. Two new modulation techniques for HCMC are proposed to achieve lower H-bridge cell capacitance and extended the modulation linear range. Both of these modulation techniques are validated and assessed by practical tests.

Chapter 1 discussed the development of multilevel converter topologies in HVDC transmission systems and proposed two multilevel converter topologies which are suitable for HVDC application. Three types of conventional multilevel converters were investigated in Chapter 2. Different modulation techniques for the M2C and the hybrid cascaded multilevel converter, (HCMC), were compared in Chapter 3.

Chapter 4 analyzed the M2C operating principle, capacitor size and ripple when SPWM modulated. The chapter also presented experimental validation of the analysis provided and demonstrated the advantages of the modulation and capacitor balancing strategy. The M2C offers the following features: improved efficiency, lower voltage and current in the switching devices, and low *dv/dt*. These features make the M2C suitable for HVDC systems.

Chapter 5 presented two new operating principles and modulation strategies that permit the hybrid cascaded multilevel converter to operate independent of modulation index and load power factor. Low-distortion output voltage and current waveforms can be achieved based on the effective H-bridge cell capacitor balancing technique. Extending the modulation index linear range provides better utilization of the HVDC link voltage since a higher fundamental output voltage for a given HVDC link improves power transfer for a given line voltage. Third harmonic subtraction from the modulating waveform minimizes the number of H-bridge cells. This reduces the additional losses. The potential benefits of the hybrid cascaded multilevel converter are dc fault reversed blocking capability, since it is able to block active power exchange between the ac and dc sides, and reactive power exchange between converters and the ac side. The validity of the presented modulation and capacitor voltage balancing schemes were confirmed by simulation and experimentation.

Since the two-level converter and the H-bridge cells of the HCMC use independent modulation control (SHE-PWM and high-frequency PWM), practical synchronization issues arise. This issue was addressed by increasing the switching frequency, which reduces the time difference between switching of the two-level converter and the H-bridge cells. This is at the expense of increased system conversion losses. The issue does not arise with the system using SPWM with 3rd harmonic subtraction, since the two-level converter and the H-bridge cells are treated as single system.

Under the same voltage conditions (for instance, V_{dc}=200V), the H-bridge cell capacitance (1mF) when using SHE-PWM and high frequency PWM is smaller than the capacitance (4.7mF) when using standard PWM. This is because the H-bridge capacitors are only subjected to harmonic power flow in the independent control modulation scheme, while in a standard PWM scheme, the H-bridge capacitors are subjected to active power flow.

Chapter 6 presents mathematical analysis and calculation of conversion losses for the two types of multilevel converters and the conventional two-level converter. Three, five, nine, and seventeen level conversion losses for the M2C, and conversion losses

for two, seven, and ten cells in the ac side of the HCMC were calculated. A simulation and experimental conversion loss comparison of the HCMC with two H-bridge cells in the ac side, was also carried out.

Both the M2C and HCMC have lower conversion losses than the conventional two-level converter. As the number of levels/cells increases, efficiency increases. The HCMC has higher conduction losses than the M2C due to H-bridge cells used in this topology, while half-bridge cells are used in the M2C. This extra HCMC loss is the penalty for inherent dc blocking capability.

Chapter 7 investigated the M2C and HCMC multilevel converters in HVDC and multi-terminal dc transmission system applications. Both steady-state and transient performance were analysed in order to verify the control strategies employed. Simulation results show these two converters in an HVDC system are able to operate over the entire specified P-Q capability curve and are capable of riding through any ac faults without posing any risk to the converter switches from over-voltage or over-current.

8.2 Author's Contribution

The author's contributions can be summarized as follows:

- Two new operating principles and modulation techniques have been proposed for the HCMC. One uses independent control of the two-level and cascaded H-bridge cells, and employs the series H-bridge string to compensate for the low frequency harmonics generates by the high voltage two-level conversion stage. The other operational mode treats the HCMC as one unit and uses sinusoidal PWM with 3rd harmonic subtraction in the modulation scheme.
- By using an independent control system for the HCMC, the H-bridge capacitors are only subjected to harmonic power flow, resulting in a reduced cell capacitance requirement, and the sinusoidal output voltage magnitude may be increased up to $4/\pi = 1.27$ p.u. This will decrease the transformer and inverter rating by 12% due to the increased fundamental component of the output voltage.
- Capacitor voltage balancing can be achieved using phase voltage redundant

switch states. By using standard multilevel modulation, the linear modulation range is extended to 1.218 and 2 for real and reactive power applications, respectively.

- The proposed switch strategy reduces the overall conduction loss and switching loss of the HCMC, compared to conventional two-level converter losses.
- Mathematical analysis for capacitor voltage ripple and capacitor size was presented for both the M2C and the HCMC, which gives guidance for the required cell capacitance when applied to medium-voltage or HVDC transmission system applications.
- Theoretical analysis of conversion and switching losses of the M2C and HCMC has been performed. This analysis gives an accurate method by which to calculate multilevel converter losses for a lower number of levels. As the number of output voltage levels increase, reasonable assumptions regarding losses must to be made due to the increasing complexity of the mathematical calculations.
- An effective control strategy for the multi-level converter in HVDC and multi-terminal HVDC systems was developed. Active and reactive powers can be control independently. An HVDC system using an M2C is able to recover from solid three-phase faults without any difficulty in terms of voltage stresses on the converter switches that may result from cell capacitor voltage unbalance or current stresses. In a multi-terminal HVDC system, the proposed control strategy allows the converter controlling the dc voltage to response to any power demand. Active power-dc voltage droop control for power management is feasible for multi-terminal dc transmission systems.

8.3 Suggestions for future research

Research undertaken in this thesis addressed some of the challenges regarding the use of a multilevel converter in HVDC transmission system application in terms of capacitor balancing technique, minimizing conversion loss, reducing *dv/dt*, and improving the quality of the output voltage. Suggestions for future research are:

- The independence of the HCMC control system should be optimized in order to dampen reactive power oscillations and minimize cell over-voltage magnitudes.

- Further investigation is required in relation to connection of the HCMC to the grid, and its ability to meet the grid code. The switching frequency should be carefully selected in order to separate the sidebands from the baseband, yet allow the converter to response fast enough to any network alteration.

Appendices

The appendices show details of the practical implementation. The test rigs, circuit boards as well as program codes are presented. The list of tables and figures, and the author's publications are also included.

A Experimental Components

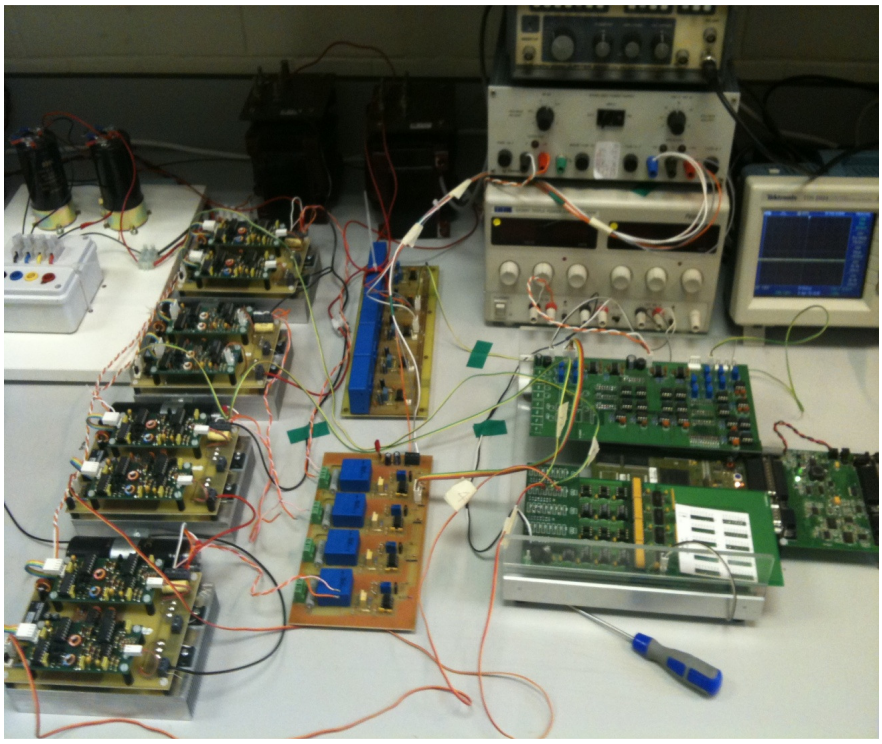
A.1 Test Rig Structure

As the chapters have covered different topics, three different test rigs have been set up for practical implementation.

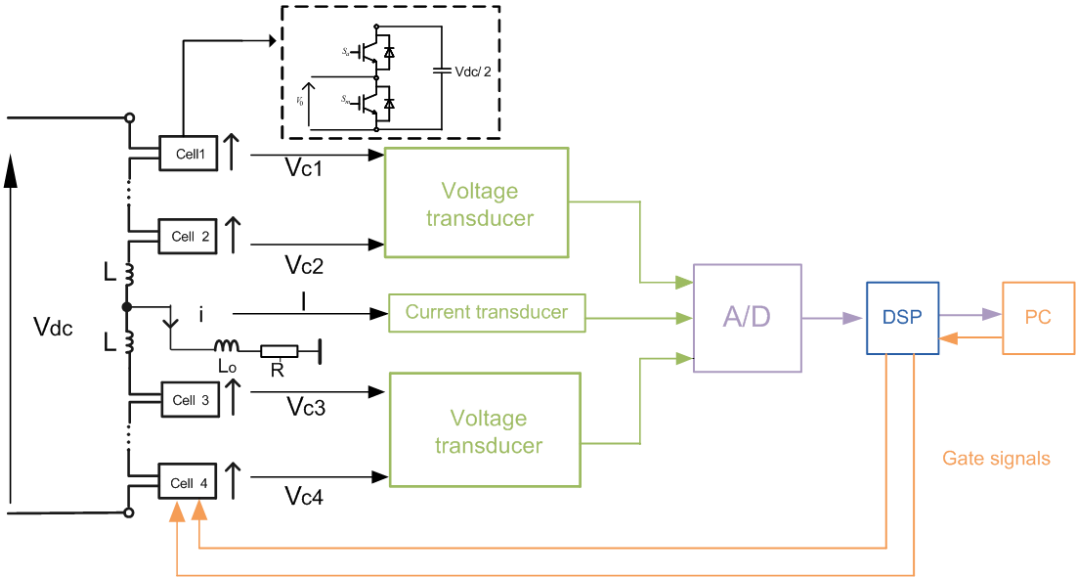
A.1.1 Modular Multilevel Converter in Chapter 4

The test rig as shown in Figure A-1 is set up to verify the control and PWM strategy for single-phase three-level M2C. It mainly includes the following components:

- 100V DC voltage source
- Four 1mF cell capacitors
- Two 3mH arm inductors
- Four cells of M2C modules
- TriCore 1796B digital signal processor
- Interface circuits for DSP
- Gate drive circuits
- Voltage and current measurement circuits



(a)



(b)

Figure A-1: System photo of M2C (a) test rig (b) schematic diagram in Chapter 4.

A.1.2 Single-phase Hybrid Cascaded Multilevel Converter in Chapter 5

The test rig as shown in Figure A-2 and Figure A-3 are set up to verify the control and PWM strategy for single-phase nine-level Hybrid Cascaded Multilevel Converter. It mainly includes the following components:

- 200V DC voltage source
- Two 1 mF cell capacitors for H-bridge
- Two cells of H-bridge modules
- One conventional two-level converter
- TriCore 1796B digital signal processor
- Interface circuits for DSP
- Gate drive circuits
- Voltage and current measurement circuits

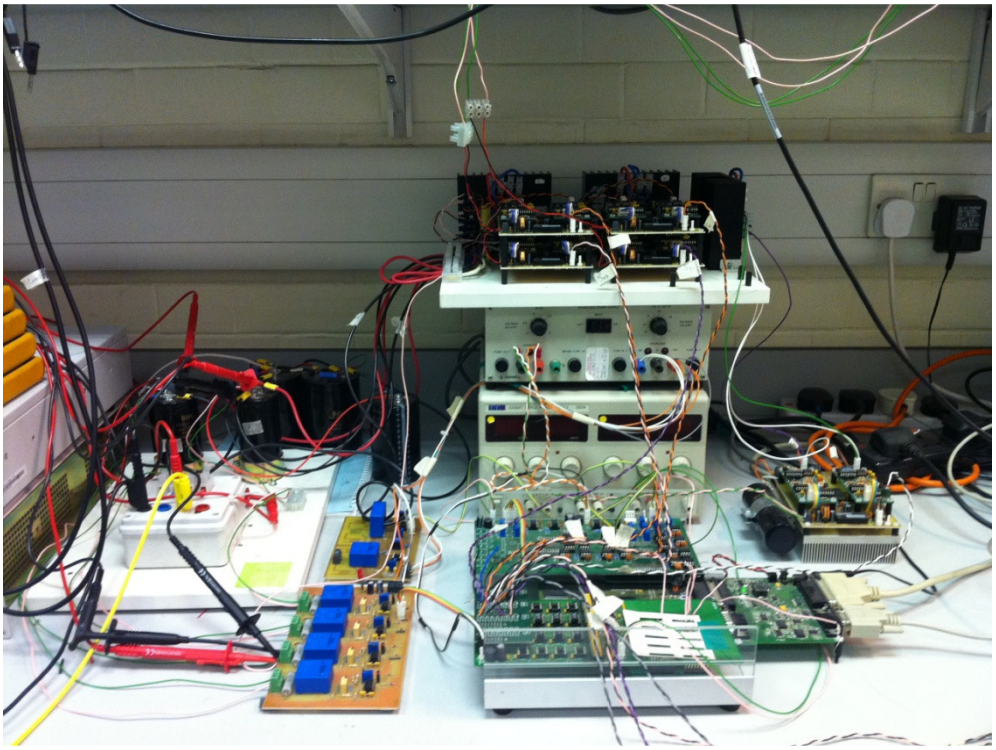


Figure A-2: System photo of single phase nine-level Hybrid Cascaded Multilevel Converter test rig.

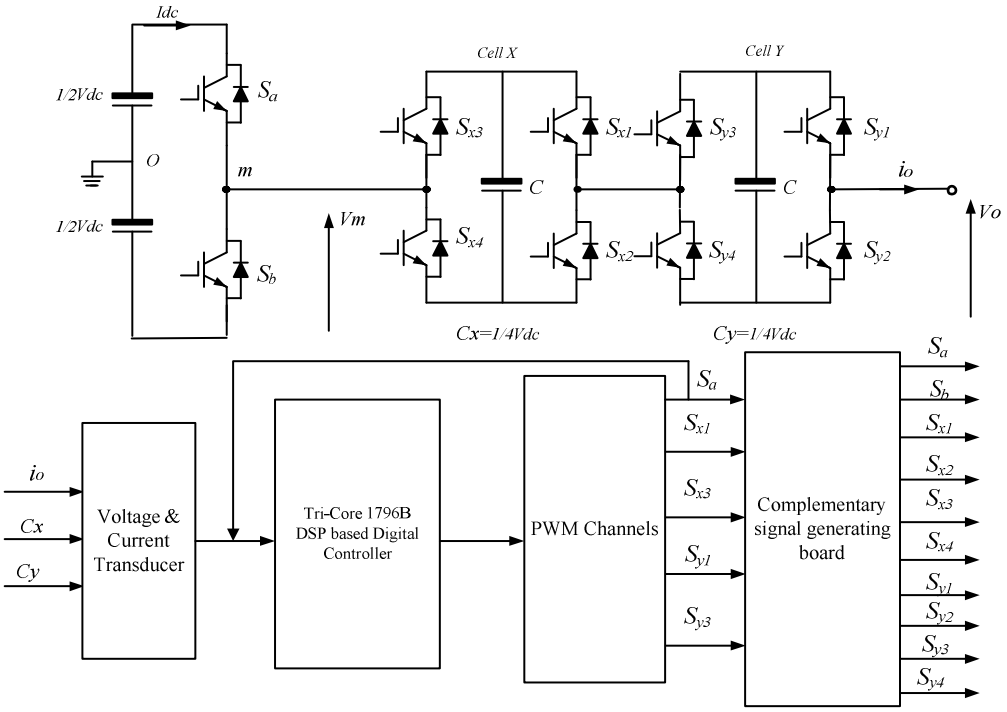
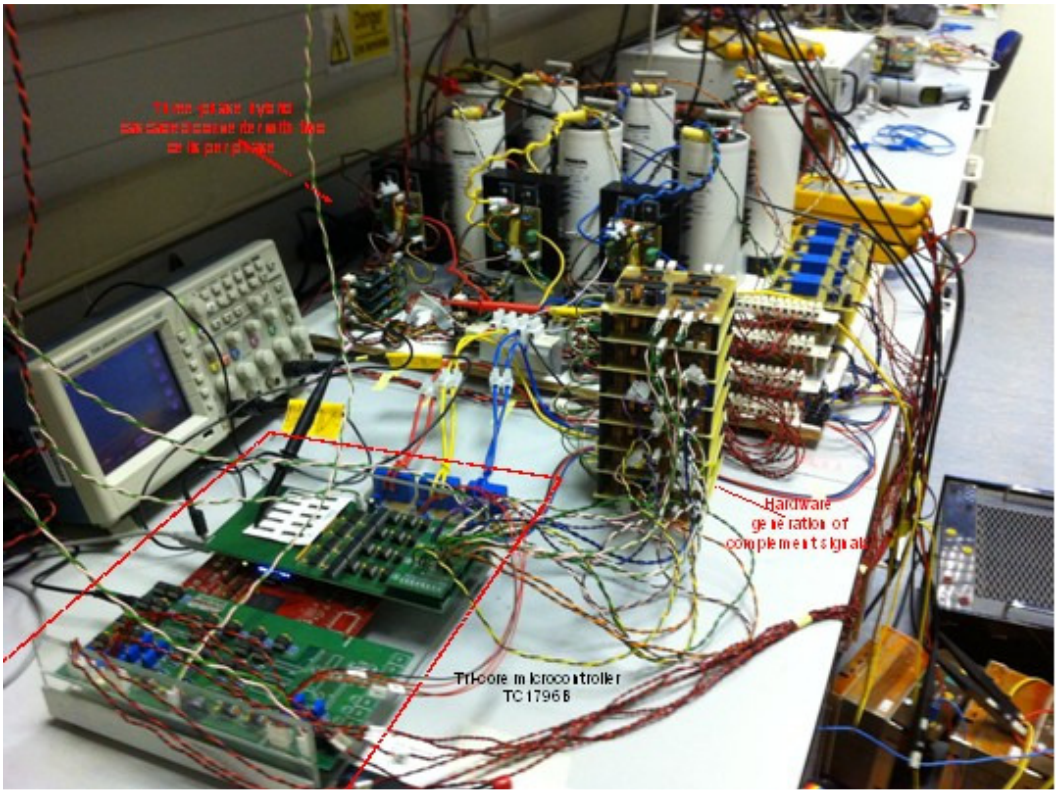


Figure A-3: System photo of single phase nine-level Hybrid Cascaded Multilevel Converter test rig schematic diagram in Chapter 5.

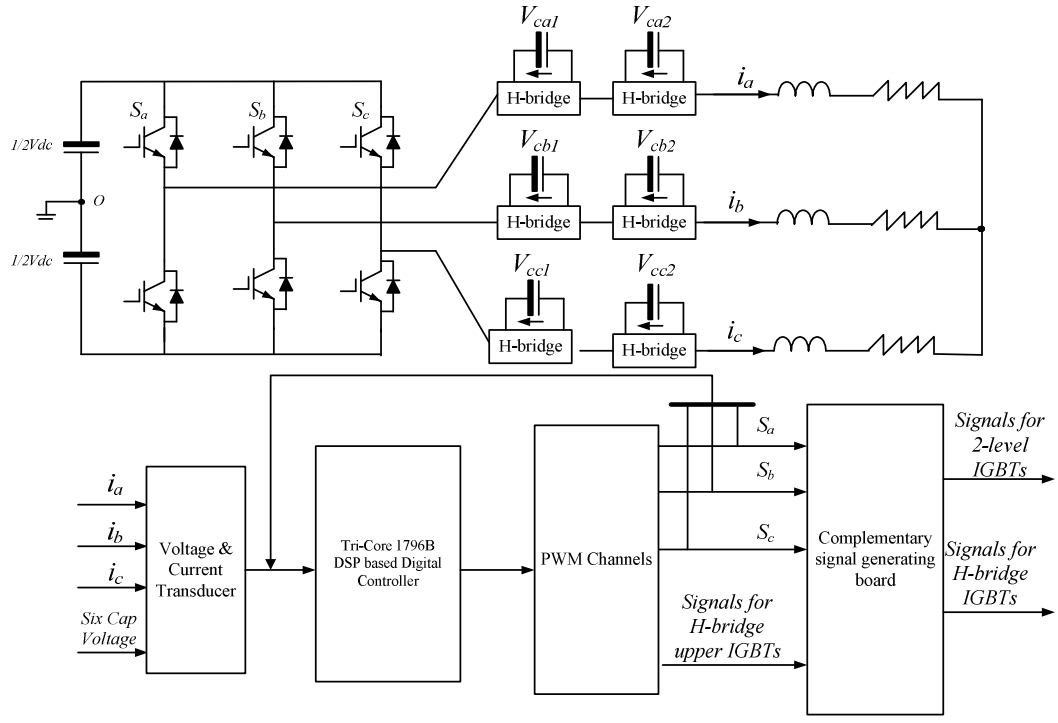
A.1.3 Three-phase Hybrid Cascaded Multilevel Converter in Chapter 5

The test rig as shown in Figure A-4 is set up to verify the control and PWM strategy for three-phase nine-level Hybrid Cascaded Multilevel Converter. It mainly includes the following components:

- 200V DC voltage source
- Six 3.3 mF cell capacitors for H-bridge
- Six cells of H-bridge modules
- One conventional two-level converter
- TriCore 1796B digital signal processor
- Interface circuits for DSP
- Gate drive circuits
- Voltage and current measurement circuits



(a)



(b)

Figure A-4: System photo of three-phase nine-level Hybrid Cascaded Multilevel Converter test rig (a) and schematic diagram (b) in Chapter 5.

A.2 Test Rig Components

The main components used in the practical implementations are introduced in this section.

A.2.1 Digital Signal Processor

The main task of the digital signal processor (DSP) is to sense the circuit analogue signals and to generate the required switching pattern driving signals for power electronic devices according to the implemented software algorithm. The 32-bit *TriCore*1796B DSP shown in figure A-5 is employed as the controller for all practical implementations.

The main features of the DSP related to the practical implementation are listed below:

- High-performance 32-bit super-scalar *TriCore* V1.3 CPU with 4-stage pipeline
  –Superior real-time performance
  –Strong bit handling
  –Fully integrated DSP capabilities
  –Single precision Floating Point Unit (FPU)
  –150 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  –16 Kbyte Parameter Memory (PRAM)
  –32 Kbyte Code Memory (CMEM)
- Multiple on-chip memories
  –2 Mbyte Program Flash Memory with ECC
  –128 Kbyte Data Flash Memory usable for EEPROM emulation
  –192 Kbyte on chip SRAM
  –16 Kbyte Instruction Cache
  –16 Kbyte BootROM
- 32-bit External Bus Interface Unit (EBU) with
- High performing on-chip bus structure
- Versatile On-chip Peripheral Units
  –Two General Purpose Timer Array Modules (GPTA) with additional Local

Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management

–Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution

–One 4-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, min. conversion time of 280ns

- 123 digital general purpose I/O lines, 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP3, DMA)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
-

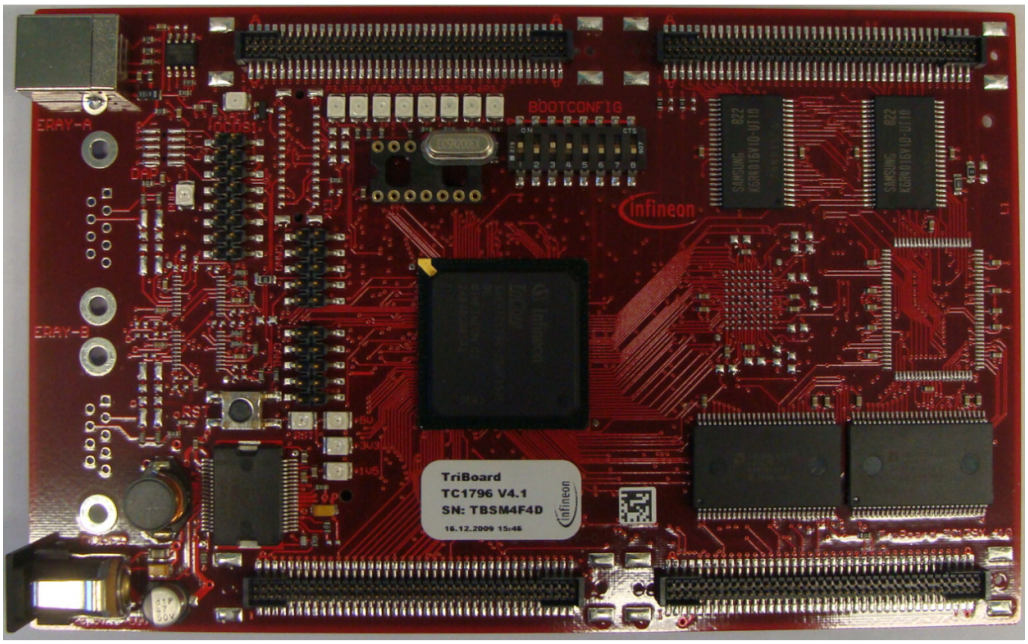


Figure A-5: DSP,32-bit *TriCore*1796B

A.2.2 Interface Circuits

Two interface boards are used to electrically isolate the DSP from external circuits using optocouplers due to protection reasons. One board isolates the ADC channels of the DSP from the voltage and current transducer circuits; while the other one isolates the PWM channels on the DSP from the driving circuits. The photo of the interface boards is shown in Figure A-6, with their circuit schematics shown in Figure A-7 and A-8.

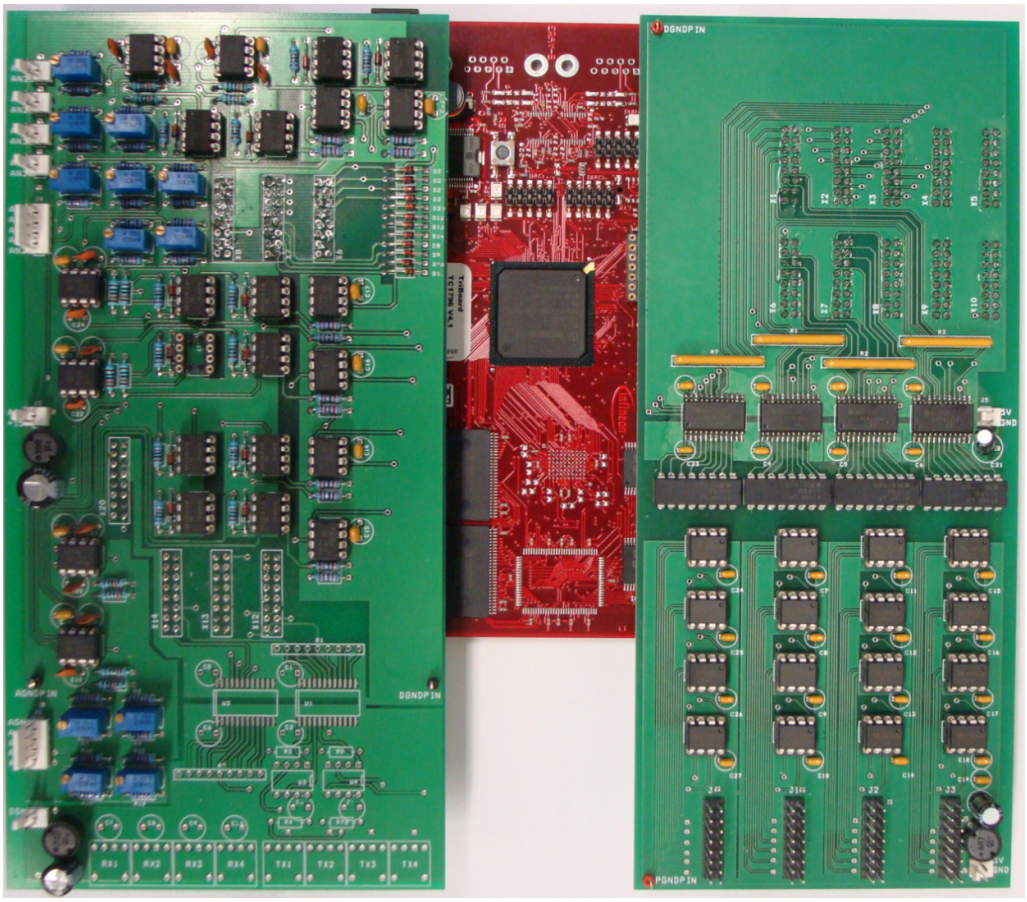
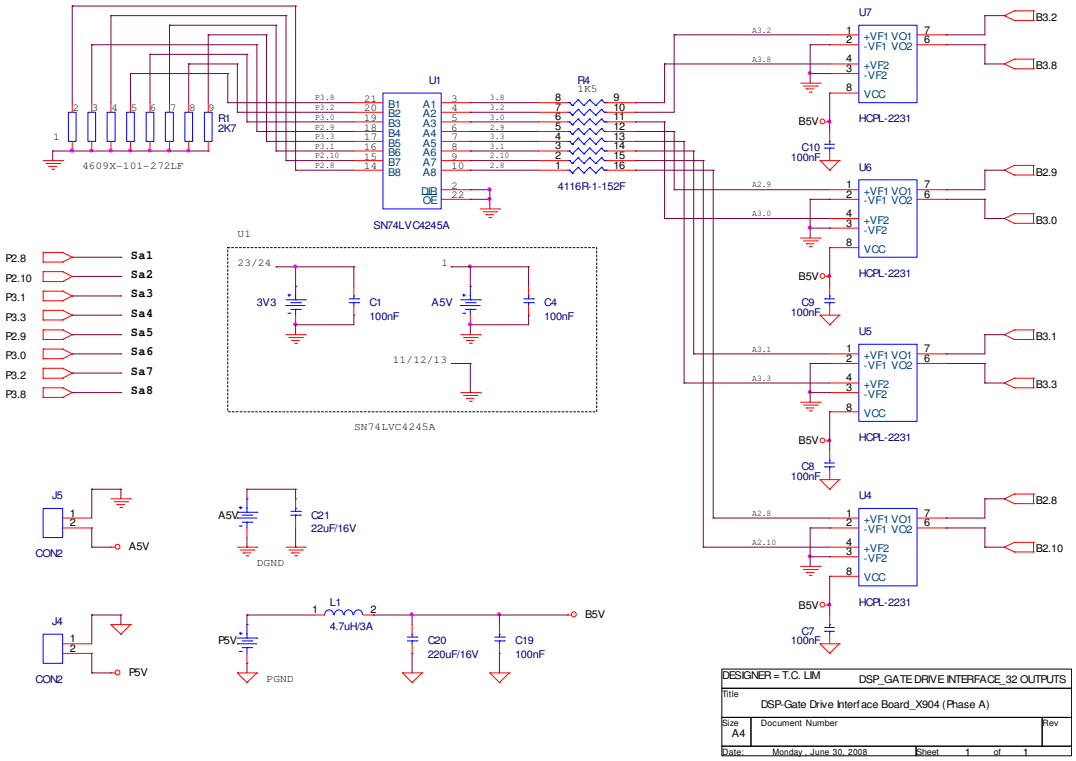


Figure A-6: Interfacing boards.



LAYOUT OF OUTPUT PINS ON CONNECTION BOARD

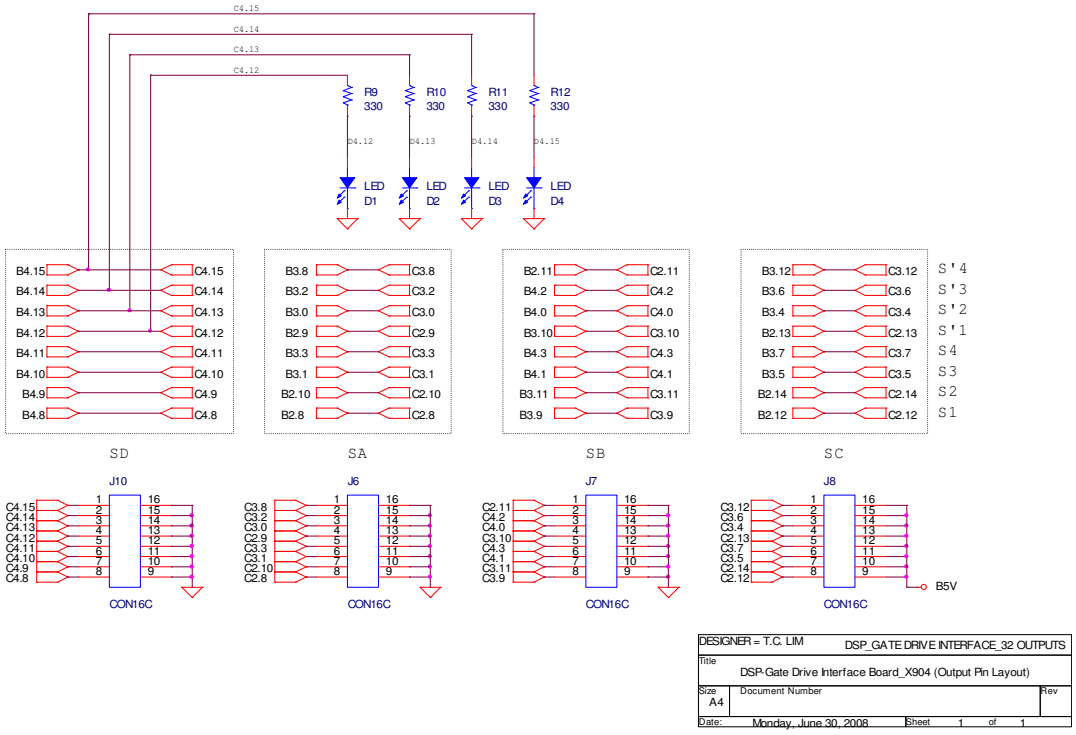


Figure A-7: Interface circuit schematic for PWM channels

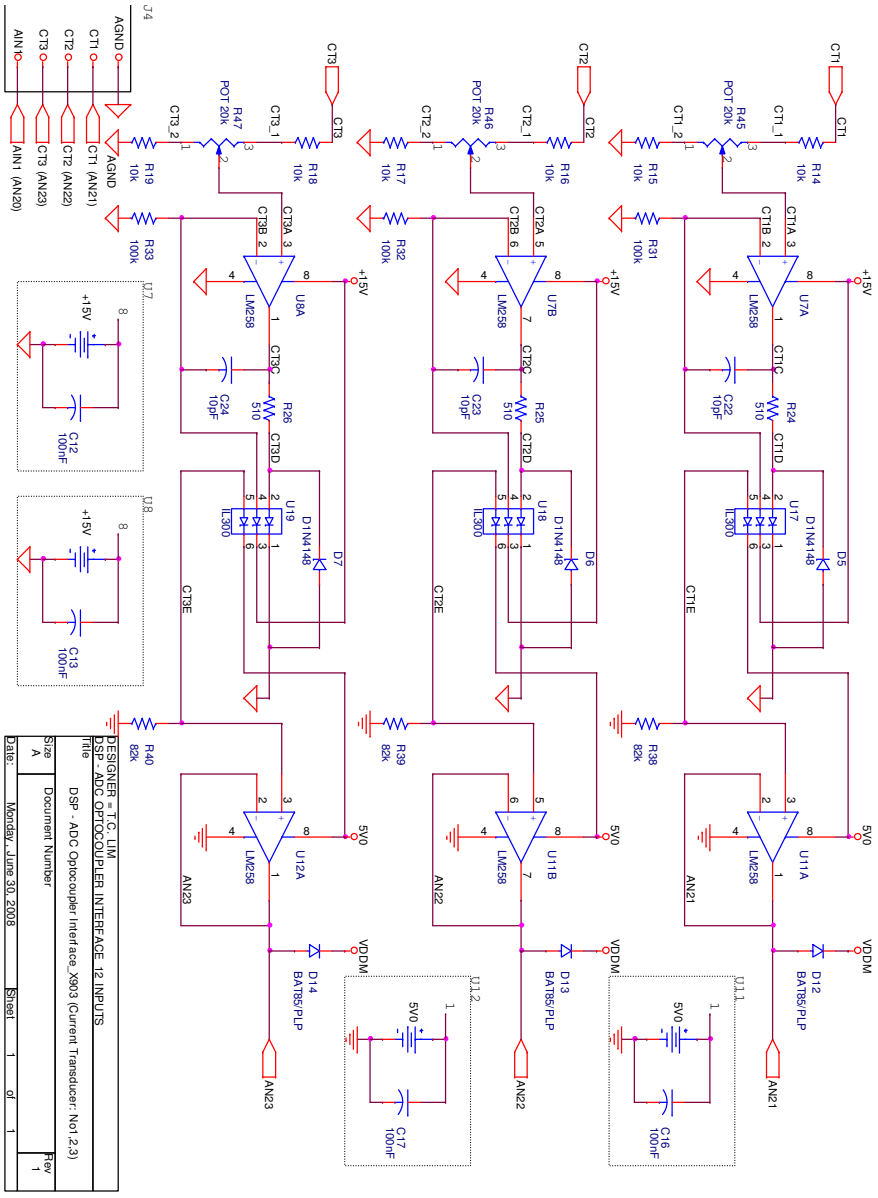


Figure A-8: Interface circuit schematic for ADC channels

A.2.3 Gate Drive Circuit

The gate drive circuit should be able to supply enough gate drive voltage and to source enough current for the switching devices to operate. The electrical isolation between the interface circuit and gate drive circuit is implemented using optocoupler. Figure A-9 shows the gate drive circuit photo and figure A-10 shows the circuit schematic.

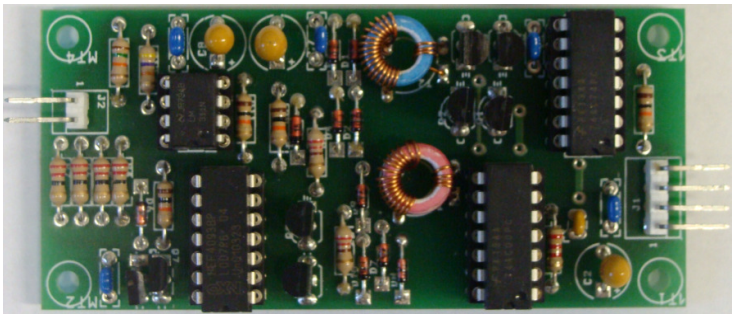


Figure A-9: Gate drive circuit photo.

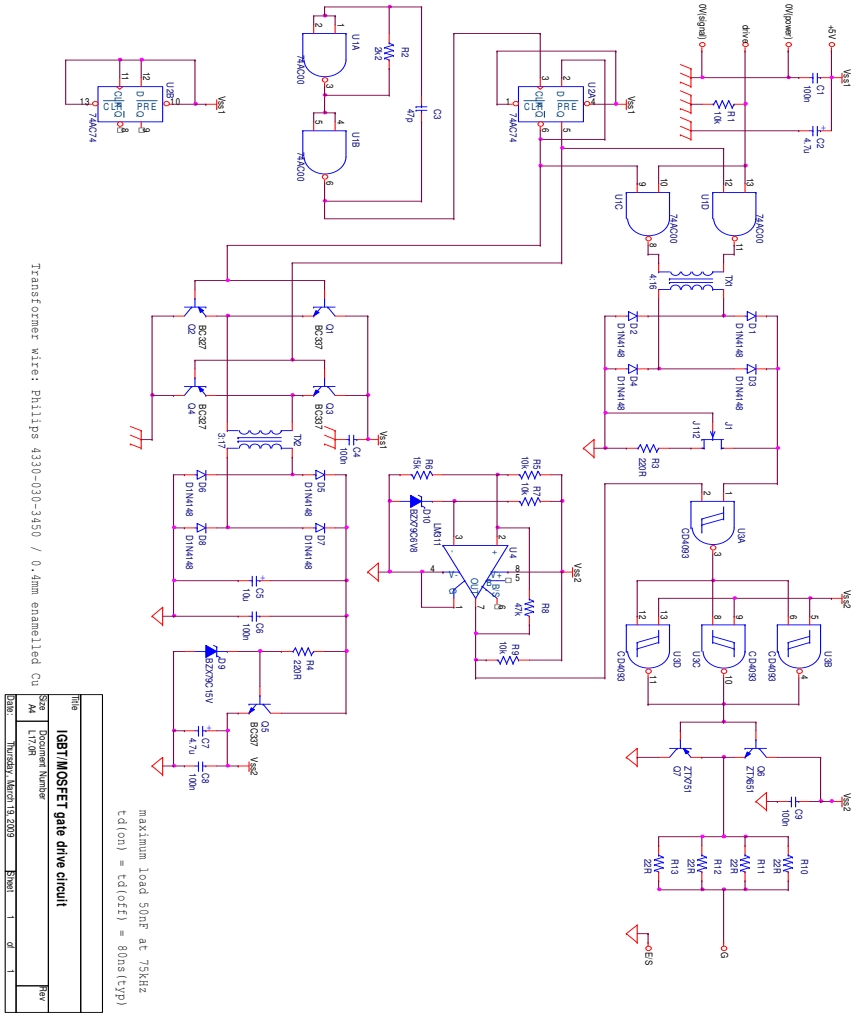


Figure A-10: Gate drive circuit schematic.

A.2.4 Voltage and Current Transducers

An accurate current data is required for the controller. The current transducer circuit schematic is shown in figure A-11. The transducer used is Hall effect current sensing device LA55P, which has high accuracy, good linearity and optimized response time with its features attached below. The photo of both transducers is given in Figure A-13.

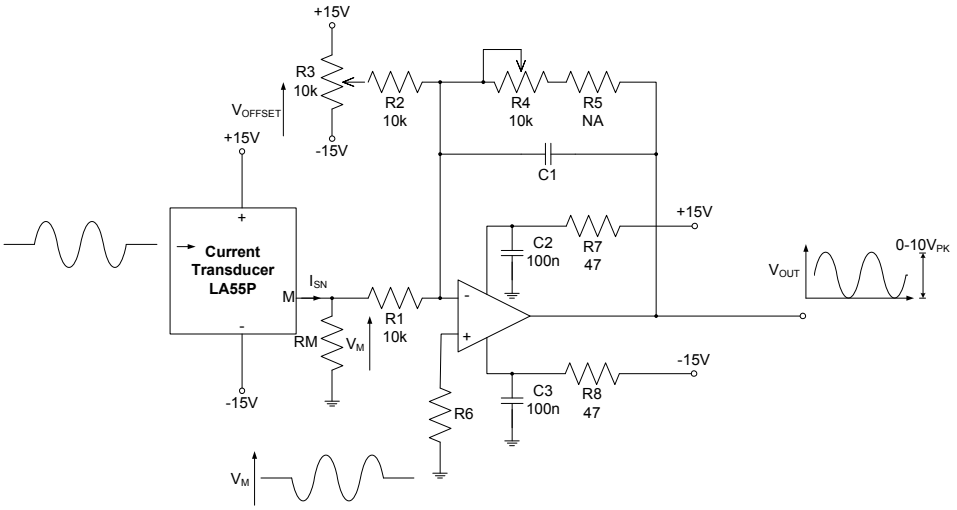


Figure A-11: Current transducer circuit schematic.

The voltage transducer circuit schematic is shown in Figure A-12. The voltage transducer LV25P uses Hall effect to measure the voltage signal.

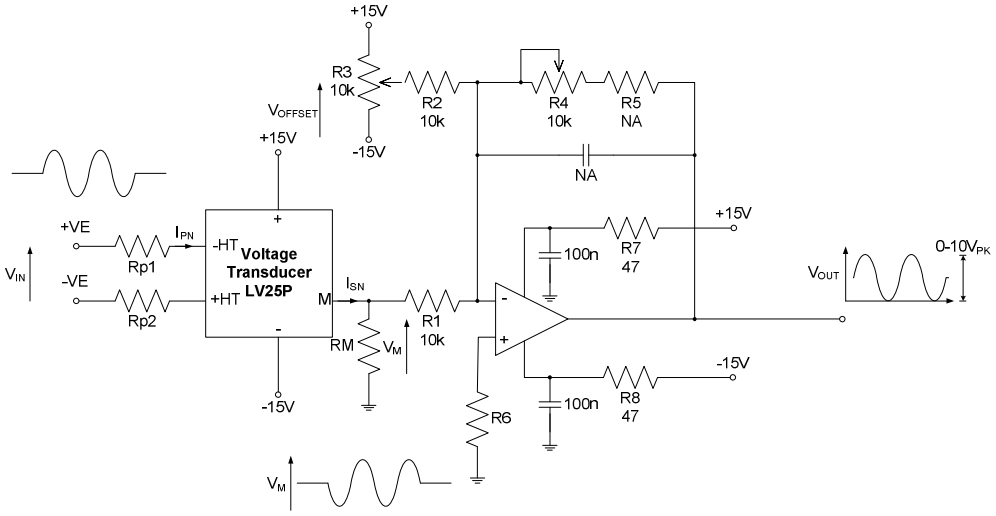


Figure A-12: Voltage transducer circuit schematic.

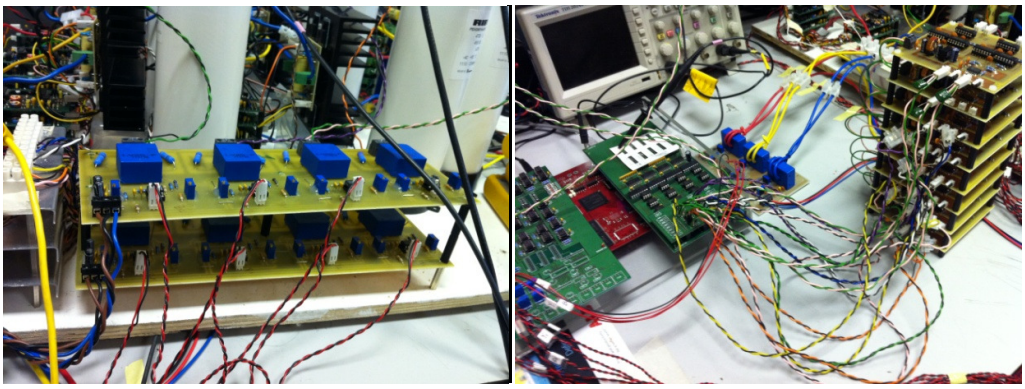


Figure A-13: Photo of voltage and current transducers.

A.2.5 Complementary Signal Generating Board

The complementary signal generating boards are used for generate complementary signals for two IGBTs in the same leg with 1µs dead time as shown Figure A-14 and Figure A-15.

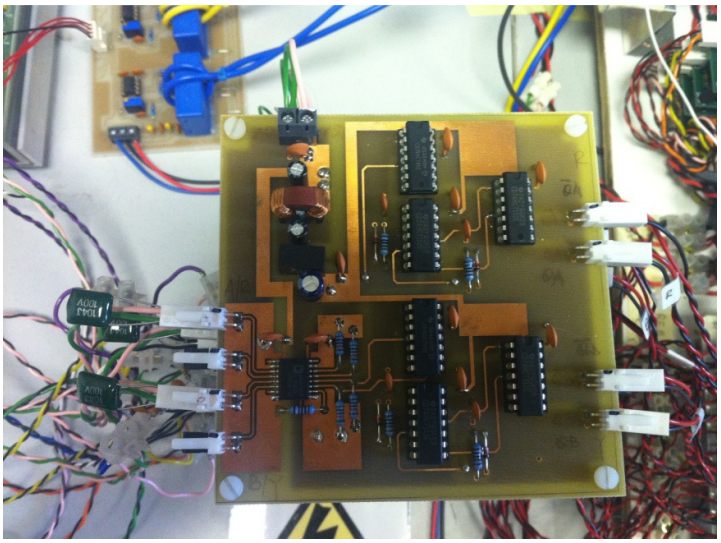


Figure A-14: Photo of complementary signal generating board.

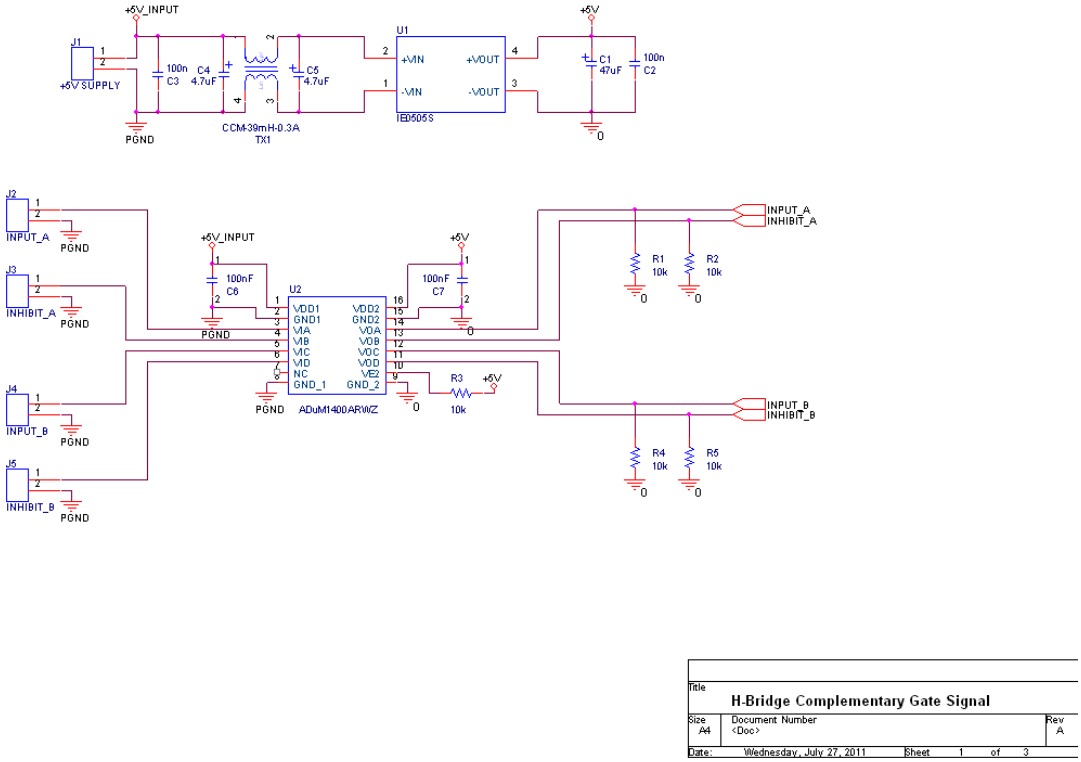


Figure A-15: Complementary gate signal generating board circuit schematic.

B Program Code

B.1 M2C simulation code

B.1.1 Three-level M2C code

```
function y = PWM_FCN(t,u)
va=u(1);vb=u(2);vc=u(3);
Vc1=u(4);Vc2=u(5);Vc3=u(6);Vc4=u(7);Ia=u(8);
%SPWM Modulation
fc=2100;
xc=2*pi*fc*t;
yc1=0.5*((2/pi)*asin(sin(xc))+1);
yc2=0.5*((2/pi)*asin(sin(xc))-1);
%Balancing
Ku_max=max(Vc1,Vc2);Ku_min=min(Vc1,Vc2);
KL_max=max(Vc3,Vc4);KL_min=min(Vc3,Vc4);

%Phase A
UP=[1 1 0 0 0 0 1 1];LW=[0 0 1 1 1 1 0 0];
A=[1 0 1 0 0 1 0 1];B=[0 1 1 0 1 0 0 1];C=[0 1 0 1 1 0 1 0];D=[1 0 0 1 0 1 1 0];
if(va>=yc1)
    sa=UP;

elseif(va<yc1&&va>=yc2)
    if(Ia>0)
        %During +ve current
        if(Vc1==Ku_min)
            if(Vc3==KL_max)
                sa=C;
            else
                sa=B;
            end
        else
            if(Vc3==KL_max)
                sa=D;
            else
                sa=A;
            end
        end
    else
        %During -ve current
        if(Vc3==KL_min)
            if(Vc1==Ku_max)
                sa=C;
            else
                sa=D;
            end
        else
            if(Vc1==Ku_max)
                sa=B;
            else
                sa=A;
            end
        end
    end
else
    sa=LW;
end

y =sa;
```

B.2.2 Five-level M2C

```
function y = PWM_FCN(t,u)
va=u(1);vb=u(2);vc=u(3);
Vc1=u(4);Vc2=u(5);Vc3=u(6);Vc4=u(7);Vc5=u(8);Vc6=u(9);Vc7=u(10);Vc8=u(11);Ia=u(12);

VC_UG=[Vc1,Vc2,Vc3,Vc4];
VC_LG=[Vc5,Vc6,Vc7,Vc8];
VC_US=sort(VC_UG);VC_LS=sort(VC_LG);
%SPWM Modulation
fc=2100;
xc=2*pi*fc*t;
yc1=0.5+0.25*((2/pi)*asin(sin(xc))+1);
yc2=0.25*((2/pi)*asin(sin(xc))+1);
yc3=0.25*((2/pi)*asin(sin(xc))-1);
yc4=-0.5+0.25*((2/pi)*asin(sin(xc))-1);
%Balancing
Ku_max=max(VC_UG);Ku_min=min(VC_UG);
KL_max=max(VC_LG);KL_min=min(VC_LG);
Sa=[0; 0; 0; 0; 0; 0; 0; 0];
%Phase A
%Voltage level +Vdc/2
if(va>=yc1)
    %Upper switches
    for II=1:4
        Sa(II)=1;
        Sa(II+4)=0;
    end
    %During +1/4Vdc
elseif(va<yc1&&va>=yc2)
    %Voltage level +Vdc/4
    %When Ia>0, this voltage level is produced by selecting one capacitor with minimum
    % voltage from the upper group and three capacitors  with maximum voltage from the bottom
group.
    %When Ia<0 one capacitor with maximum voltage is selected from the upper group and
    %three with the minimum voltage magnitudes are selected from the lower group.
    if(Ia>=0)

        for II=1:4
            %Upper switches
            if(VC_UG(II)==Ku_min)
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Lower switches
            if(VC_LG(II)==KL_min)
                Sa(II+4)=1;
            else
                Sa(II+4)=0;
            end
        end
    else
        %Ia<0
        for II=1:4
            %Upper switches
            if(VC_UG(II)==Ku_max)
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Lower switches
            if(VC_LG(II)==KL_max)
                Sa(II+4)=1;
            else
                Sa(II+4)=0;
            end
        end
    end
    %During 0 Vdc
    elseif(va<yc2&&va>=yc3)
        if(Ia>=0)
        for II=1:4
```

```
            %Switching of the upper group
            if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4))
                Sa(II+4)=0;
            else
                Sa(II+4)=1;
            end
        end
    else
        %Ia<0
        for II=1:4
            %Switching of the upper group
            if(VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2))
                Sa(II+4)=0;
            else
                Sa(II+4)=1;
            end
        end
    end
    %During -1/4 voltage
elseif(va<yc3&&va>=yc4)
    if(Ia>=0)
 for II=1:4
            %Upper switches
            if(VC_UG(II)==Ku_max)
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Lower switches
            if(VC_LG(II)==KL_max)
                Sa(II+4)=0;
            else
                Sa(II+4)=1;
            end
 end
    else
        %Ia<0
        for II=1:4
            %Upper switches
            if(VC_UG(II)==Ku_min)
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Lower switches
            if(VC_LG(II)==KL_min)
                Sa(II+4)=0;
            else
                Sa(II+4)=1;
            end
        end
    end

%during -1/2V voltage
elseif(va<=yc4)
    for II=1:4
        Sa(II)=0;
        Sa(II+4)=1;
    end
end
y=Sa;
```

B.2.3 Nine-level M2C

```
function y = PWM_FCN(t,u)
va=u(1);vb=u(2);vc=u(3);
Vc1=u(4);Vc2=u(5);Vc3=u(6);Vc4=u(7);Vc5=u(8);Vc6=u(9);Vc7=u(10);Vc8=u(11);
Vc9=u(12);Vc10=u(13);Vc11=u(14);Vc12=u(15);Vc13=u(16);Vc14=u(17);Vc15=u(18);Vc16=u(19
);
Ia=u(20);

VC_UG=[Vc1,Vc2,Vc3,Vc4,Vc5,Vc6,Vc7,Vc8];
VC_LG=[Vc9,Vc10,Vc11,Vc12,Vc13,Vc14,Vc15,Vc16];
VC_US=sort(VC_UG);VC_LS=sort(VC_LG);
%SPWM Modulation
fc=2100;
xc=2*pi*fc*t;
yc1=0.75+0.125*((2/pi)*asin(sin(xc))+1);
yc2=0.5+0.125*((2/pi)*asin(sin(xc))+1);
yc3=0.25+0.125*((2/pi)*asin(sin(xc))+1);
yc4=0.125*((2/pi)*asin(sin(xc))+1);
yc5=0.125*((2/pi)*asin(sin(xc))-1);
yc6=-0.25+0.125*((2/pi)*asin(sin(xc))-1);
yc7=-0.5+0.125*((2/pi)*asin(sin(xc))-1);
yc8=-0.75+0.125*((2/pi)*asin(sin(xc))-1);
%Balancing
Ku_max=max(VC_UG);Ku_min=min(VC_UG);
KL_max=max(VC_LG);KL_min=min(VC_LG);
Sa=[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0];
%Phase A
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Voltage level +Vdc/2
if(va>=yc1)
    %Upper switches
    for II=1:8
        Sa(II)=1;
        Sa(II+8)=0;
    end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc1&&va>=yc2)     %%Voltage level +Vdc3/8   (1 upper 7 lower)
  if(Ia>=0)
        for II=1:8
            %Upper switches
            if(VC_UG(II)==Ku_min)
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Lower switches
            if(VC_LG(II)==KL_min)
                Sa(II+8)=1;
            else
                Sa(II+8)=0;
            end
        end
    else
        %Ia<0
        for II=1:8
            %Upper switches
            if(VC_UG(II)==Ku_max)
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Lower switches
            if(VC_LG(II)==KL_max)
                Sa(II+8)=1;
            else
                Sa(II+8)=0;
            end
        end
 end

    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    elseif(va<yc2&&va>=yc3)   %%Voltage level is 1/4 Vdc    (2 upper 6 lower)
```

```
    if(Ia>=0)
        for II=1:8
            %Switching of the upper group
            if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2))
                Sa(II+8)=1;
            else
                Sa(II+8)=0;
            end
        end
    else
        %Ia<0
        for II=1:8
            %Switching of the upper group
            if(VC_UG(II)==VC_US(7)||VC_UG(II)==VC_US(8))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(7)||VC_LG(II)==VC_LS(8))
                Sa(II+8)=1;
            else
                Sa(II+8)=0;
            end
        end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc3&&va>=yc4)   %%Voltage level is 1/8 Vdc (3 upper 5 lower)
   if(Ia>=0)
        for II=1:8
            %Switching of the upper group
            if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3))
                Sa(II+8)=1;
            else
                Sa(II+8)=0;
            end
        end
    else
        %Ia<0
        for II=1:8
            %Switching of the upper group
            if(VC_UG(II)==VC_US(6)||VC_UG(II)==VC_US(7)||VC_UG(II)==VC_US(8))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(6)||VC_LG(II)==VC_LS(7)||VC_LG(II)==VC_LS(8))
                Sa(II+8)=1;
            else
                Sa(II+8)=0;
            end
        end
    end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc4&&va>=yc5)   %%Voltage level is 0Vdc (4 upper 4 lower)
              if(Ia>=0)
                  for II=1:8
                      %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
)
```

```
                    Sa(II)=0;
                else
                    Sa(II)=1;
                end
                %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
)
                    Sa(II+8)=1;
                else
                    Sa(II+8)=0;
                end
            end
        else
            %Ia<0
            for II=1:8
                %Switching of the upper group

if(VC_UG(II)==VC_US(5)||VC_UG(II)==VC_US(6)||VC_UG(II)==VC_US(7)||VC_UG(II)==VC_US(8)
)
                    Sa(II)=0;
                else
                    Sa(II)=1;
                end
                %Switching of the lower group

if(VC_LG(II)==VC_LS(5)||VC_LG(II)==VC_LS(6)||VC_LG(II)==VC_LS(7)||VC_LG(II)==VC_LS(8)
)
                    Sa(II+8)=1;
                else
                    Sa(II+8)=0;
                end
            end
        end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc5&&va>=yc6)   %%Voltage level is -1/8Vdc (5 upper 3 lower)
 if(Ia>=0)
       for II=1:8
           %Switching of the upper group
           if(VC_UG(II)==VC_US(6)||VC_UG(II)==VC_US(7)||VC_UG(II)==VC_US(8))
               Sa(II)=1;
           else
               Sa(II)=0;
           end
           %Switching of the lower group
           if(VC_LG(II)==VC_LS(6)||VC_LG(II)==VC_LS(7)||VC_LG(II)==VC_LS(8))
               Sa(II+8)=0;
           else
               Sa(II+8)=1;
           end
       end
   else
       %Ia<0
       for II=1:8
           %Switching of the upper group
           if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3))
               Sa(II)=1;
           else
               Sa(II)=0;
           end
           %Switching of the lower group
           if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3))
               Sa(II+8)=0;
           else
               Sa(II+8)=1;
           end
       end
   end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc6&&va>=yc7)   %%Voltage level is -1/4Vdc (6 upper 2 lower)
   if(Ia>=0)
       for II=1:8
           %Switching of the upper group
           if(VC_UG(II)==VC_US(7)||VC_UG(II)==VC_US(8))
```

```
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(7)||VC_LG(II)==VC_LS(8))
                Sa(II+8)=0;
            else
                Sa(II+8)=1;
            end
        end
    else
        %Ia<0
        for II=1:8
            %Switching of the upper group
            if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2))
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2))
                Sa(II+8)=0;
            else
                Sa(II+8)=1;
            end
        end
    end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc7&&va>=yc8)   %%Voltage level is -3/8Vdc (7 upper 1 lower)
if(Ia>=0)
 for II=1:8
            %Upper switches
            if(VC_UG(II)==Ku_max)
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Lower switches
            if(VC_LG(II)==KL_max)
                Sa(II+8)=0;
            else
                Sa(II+8)=1;
            end
 end
    else
        %Ia<0
        for II=1:8
            %Upper switches
            if(VC_UG(II)==Ku_min)
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Lower switches
            if(VC_LG(II)==KL_min)
                Sa(II+8)=0;
            else
                Sa(II+8)=1;
            end
        end
    end

 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  elseif(va<=yc8)         %%Voltage level is -1/2Vdc (4 upper 4lower)
    for II=1:8
        Sa(II)=0;
        Sa(II+8)=1;
    end
end
y=Sa;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

B.2.4 Seventeen-level M2C

```
function y = PWM_FCN(t,u)
va=u(1);vb=u(2);vc=u(3);
Vc1=u(4);Vc2=u(5);Vc3=u(6);Vc4=u(7);Vc5=u(8);Vc6=u(9);Vc7=u(10);Vc8=u(11);
Vc9=u(12);Vc10=u(13);Vc11=u(14);Vc12=u(15);Vc13=u(16);Vc14=u(17);Vc15=u(18);Vc16=u(19
);Vc17=u(20);Vc18=u(21);Vc19=u(22);
Vc20=u(23);Vc21=u(24);Vc22=u(25);Vc23=u(26);Vc24=u(27);Vc25=u(28);Vc26=u(29);Vc27=u(3
0);Vc28=u(31);Vc29=u(32);
Vc30=u(33);Vc31=u(34);Vc32=u(35);
Ia=u(36);

VC_UG=[Vc1,Vc2,Vc3,Vc4,Vc5,Vc6,Vc7,Vc8,Vc9,Vc10,Vc11,Vc12,Vc13,Vc14,Vc15,Vc16];
VC_LG=[Vc17,Vc18,Vc19,Vc20,Vc21,Vc22,Vc23,Vc24,Vc25,Vc26,Vc27,Vc28,Vc29,Vc30,Vc31,Vc3
2];
VC_US=sort(VC_UG);VC_LS=sort(VC_LG);
%SPWM Modulation
fc=1200;
xc=2*pi*fc*t;
yc1=0.875+0.0625*((2/pi)*asin(sin(xc))+1);
yc2=0.75+0.0625*((2/pi)*asin(sin(xc))+1);
yc3=0.625+0.0625*((2/pi)*asin(sin(xc))+1);
yc4=0.5+0.0625*((2/pi)*asin(sin(xc))+1);
yc5=0.375+0.0625*((2/pi)*asin(sin(xc))+1);
yc6=0.25+0.0625*((2/pi)*asin(sin(xc))+1);
yc7=0.125+0.0625*((2/pi)*asin(sin(xc))+1);
yc8=0.0625*((2/pi)*asin(sin(xc))+1);
yc9=0.0625*((2/pi)*asin(sin(xc))-1);
yc10=-0.125+0.0625*((2/pi)*asin(sin(xc))-1);
yc11=-0.25+0.0625*((2/pi)*asin(sin(xc))-1);
yc12=-0.375+0.0625*((2/pi)*asin(sin(xc))-1);
yc13=-0.5+0.0625*((2/pi)*asin(sin(xc))-1);
yc14=-0.625+0.0625*((2/pi)*asin(sin(xc))-1);
yc15=-0.75+0.0625*((2/pi)*asin(sin(xc))-1);
yc16=-0.875+0.0625*((2/pi)*asin(sin(xc))-1);
%Balancing
Ku_max=max(VC_UG);Ku_min=min(VC_UG);
KL_max=max(VC_LG);KL_min=min(VC_LG);
Sa=[0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0];
%Phase A
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Voltage level +Vdc/2
if(va>=yc1)
    %Upper switches
    for II=1:16
        Sa(II)=1;
        Sa(II+16)=0;
    end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc1&&va>=yc2)     %%Voltage level +Vdc7/16   (1 upper 15 lower)
  if(Ia>=0)
        for II=1:16
            %Upper switches
            if(VC_UG(II)==Ku_min)
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Lower switches
            if(VC_LG(II)==KL_min)
                Sa(II+16)=1;
            else
                Sa(II+16)=0;
            end
        end
    else
        %Ia<0
        for II=1:16
            %Upper switches
            if(VC_UG(II)==Ku_max)
                Sa(II)=0;
            else
                Sa(II)=1;
```

```
            end
            %Lower switches
            if(VC_LG(II)==KL_max)
                Sa(II+16)=1;
            else
                Sa(II+16)=0;
            end
        end
    end

    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    elseif(va<yc2&&va>=yc3)   %%Voltage level is 3/8 Vdc    (2 upper 14 lower)
    if(Ia>=0)
        for II=1:16
            %Switching of the upper group
            if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2))
                Sa(II+16)=1;
            else
                Sa(II+16)=0;
            end
        end
    else
        %Ia<0
        for II=1:16
            %Switching of the upper group
            if(VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                Sa(II+16)=1;
            else
                Sa(II+16)=0;
            end
        end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc3&&va>=yc4)   %%Voltage level is 5/16 Vdc (3 upper 13 lower)
   if(Ia>=0)
        for II=1:16
            %Switching of the upper group
            if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3))
                Sa(II+16)=1;
            else
                Sa(II+16)=0;
            end
        end
    else
        %Ia<0
        for II=1:16
            %Switching of the upper group
            if(VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                Sa(II)=0;
            else
                Sa(II)=1;
            end
            %Switching of the lower group
            if(VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                Sa(II+16)=1;
            else
```

```
            Sa(II+16)=0;
        end
    end
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc4&&va>=yc5)   %%Voltage level is 1/4Vdc (4 upper 12 lower)
            if(Ia>=0)
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
)
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
)
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US
(16))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS
(16))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc5&&va>=yc6)   %%Voltage level is 3/16 Vdc (5 upper 11 lower)
if(Ia>=0)
      for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group
```

```
if(VC_UG(II)==VC_US(12)||VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US
(15)||VC_UG(II)==VC_US(16))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(12)||VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS
(15)||VC_LG(II)==VC_LS(16))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            end

 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc6&&va>=yc7)   %%Voltage level is 1/8Vdc (6 upper 10 lower)
   if(Ia>=0)
       for II=1:16
           %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5)||VC_UG(II)==VC_US(6))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5)||VC_LG(II)==VC_LS(6))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(11)||VC_UG(II)==VC_US(12)||VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US
(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(11)||VC_LG(II)==VC_LS(12)||VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS
(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc7&&va>=yc8)   %%Voltage level is 1/16Vdc (7 upper 9 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5)||VC_UG(II)==VC_US(6)||VC_UG(II)==VC_US(7))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group
```

```
if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5)||VC_LG(II)==VC_LS(6)||VC_LG(II)==VC_LS(7))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(10)||VC_UG(II)==VC_US(11)||VC_UG(II)==VC_US(12)||VC_UG(II)==VC_US
(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(10)||VC_LG(II)==VC_LS(11)||VC_LG(II)==VC_LS(12)||VC_LG(II)==VC_LS
(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            end

 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  elseif(va<yc8&&va>=yc9)         %%Voltage level is 0 Vdc (8 upper 8 lower)
    if(Ia>=0)
 for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5)||VC_UG(II)==VC_US(6)||VC_UG(II)==VC_US(7)||VC_UG(II)==VC_US(8))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5)||VC_LG(II)==VC_LS(6)||VC_LG(II)==VC_LS(7)||VC_LG(II)==VC_LS(8))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(9)||VC_UG(II)==VC_US(10)||VC_UG(II)==VC_US(11)||VC_UG(II)==VC_US(
12)||VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_
US(16))
                        Sa(II)=0;
                    else
                        Sa(II)=1;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(9)||VC_LG(II)==VC_LS(10)||VC_LG(II)==VC_LS(11)||VC_LG(II)==VC_LS(
12)||VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_
LS(16))
                        Sa(II+16)=1;
                    else
                        Sa(II+16)=0;
                    end
                end
            end
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
elseif(va<yc9&&va>=yc10)        %%Voltage level is -1/16 Vdc (9 upper 7 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(10)||VC_UG(II)==VC_US(11)||VC_UG(II)==VC_US(12)||VC_UG(II)==VC_US
(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                       Sa(II)=1;
                    else
                       Sa(II)=0;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(10)||VC_LG(II)==VC_LS(11)||VC_LG(II)==VC_LS(12)||VC_LG(II)==VC_LS
(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                       Sa(II+16)=0;
                    else
                       Sa(II+16)=1;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5)||VC_UG(II)==VC_US(6)||VC_UG(II)==VC_US(7))
                       Sa(II)=1;
                    else
                       Sa(II)=0;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5)||VC_LG(II)==VC_LS(6)||VC_LG(II)==VC_LS(7))
                       Sa(II+16)=0;
                    else
                       Sa(II+16)=1;
                    end
                end
            end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc10&&va>=yc11)        %%Voltage level is -1/8 Vdc (10 upper 6 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(11)||VC_UG(II)==VC_US(12)||VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US
(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                       Sa(II)=1;
                    else
                       Sa(II)=0;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(11)||VC_LG(II)==VC_LS(12)||VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS
(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                       Sa(II+16)=0;
                    else
                       Sa(II+16)=1;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5)||VC_UG(II)==VC_US(6))
                       Sa(II)=1;
                    else
                       Sa(II)=0;
```

```
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5)||VC_LG(II)==VC_LS(6))
                        Sa(II+16)=0;
                    else
                        Sa(II+16)=1;
                    end
                end
            end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%
elseif(va<yc11&&va>=yc12)        %%Voltage level is -3/16 Vdc (11 upper 5 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(12)||VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US
(15)||VC_UG(II)==VC_US(16))
                        Sa(II)=1;
                    else
                        Sa(II)=0;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(12)||VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS
(15)||VC_LG(II)==VC_LS(16))
                        Sa(II+16)=0;
                    else
                        Sa(II+16)=1;
                    end
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group

if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
||VC_UG(II)==VC_US(5))
                        Sa(II)=1;
                    else
                        Sa(II)=0;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
||VC_LG(II)==VC_LS(5))
                        Sa(II+16)=0;
                    else
                        Sa(II+16)=1;
                    end
                end
            end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc12&&va>=yc13)        %%Voltage level is -1/4 Vdc (12 upper 4 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group

if(VC_UG(II)==VC_US(13)||VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US
(16))
                        Sa(II)=1;
                    else
                        Sa(II)=0;
                    end
                    %Switching of the lower group

if(VC_LG(II)==VC_LS(13)||VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS
(16))
                        Sa(II+16)=0;
                    else
                        Sa(II+16)=1;
                    end
```

```
            end
        else
            %Ia<0
            for II=1:16
                %Switching of the upper group
if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3)||VC_UG(II)==VC_US(4)
)
                    Sa(II)=1;
                else
                    Sa(II)=0;
                end
                %Switching of the lower group
if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3)||VC_LG(II)==VC_LS(4)
)
                    Sa(II+16)=0;
                else
                    Sa(II+16)=1;
                end
            end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc13&&va>=yc14)        %%Voltage level is -5/16 Vdc (13 upper 3 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group
if(VC_UG(II)==VC_US(14)||VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                    Sa(II)=1;
                else
                    Sa(II)=0;
                end
                %Switching of the lower group
if(VC_LG(II)==VC_LS(14)||VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                    Sa(II+16)=0;
                else
                    Sa(II+16)=1;
                end
            end
        else
            %Ia<0
            for II=1:16
                %Switching of the upper group
                if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2)||VC_UG(II)==VC_US(3))
                    Sa(II)=1;
                else
                    Sa(II)=0;
                end
                %Switching of the lower group
                if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2)||VC_LG(II)==VC_LS(3))
                    Sa(II+16)=0;
                else
                    Sa(II+16)=1;
                end
            end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
elseif(va<yc14&&va>=yc15)        %%Voltage level is -3/8 Vdc (14 upper 2 lower)
if(Ia>=0)
 for II=1:16
          %Switching of the upper group
                if(VC_UG(II)==VC_US(15)||VC_UG(II)==VC_US(16))
                    Sa(II)=1;
                else
                    Sa(II)=0;
                end
                %Switching of the lower group
                if(VC_LG(II)==VC_LS(15)||VC_LG(II)==VC_LS(16))
                    Sa(II+16)=0;
                else
                    Sa(II+16)=1;
                end
```

```
                end
            else
                %Ia<0
                for II=1:16
                    %Switching of the upper group
                    if(VC_UG(II)==VC_US(1)||VC_UG(II)==VC_US(2))
                        Sa(II)=1;
                    else
                        Sa(II)=0;
                    end
                    %Switching of the lower group
                    if(VC_LG(II)==VC_LS(1)||VC_LG(II)==VC_LS(2))
                        Sa(II+16)=0;
                    else
                        Sa(II+16)=1;
                    end
                end
          end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
 elseif(va<yc15&&va>=yc16)   %%Voltage level is -7/16Vdc (15 upper 1 lower)
if(Ia>=0)
 for II=1:16
           %Upper switches
           if(VC_UG(II)==Ku_max)
               Sa(II)=1;
           else
               Sa(II)=0;
           end
           %Lower switches
           if(VC_LG(II)==KL_max)
               Sa(II+16)=0;
           else
               Sa(II+16)=1;
           end
 end
    else
        %Ia<0
        for II=1:16
            %Upper switches
            if(VC_UG(II)==Ku_min)
                Sa(II)=1;
            else
                Sa(II)=0;
            end
            %Lower switches
            if(VC_LG(II)==KL_min)
                Sa(II+16)=0;
            else
                Sa(II+16)=1;
            end
        end
    end
      %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  elseif(va<=yc16)         %%Voltage level is -1/2Vdc (0 upper 16lower)
    for II=1:16
        Sa(II)=0;
        Sa(II+16)=1;
    end
end
y=Sa;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

B.2 Hybrid Cascaded Multilevel Converter simulation code

B.2.1 HCMC with 2 H-bridge cells

```
function y = PWM_FCN(t,u)
V_H=u(1);
ia=u(2);
vc1=u(3);
vc2=u(4);
Vdc=u(5);
V_C=[vc1,vc2];
Cmax=max(V_C);Cmin=min(V_C);
%SPWM Modulation
fc=4000;
xc=2*pi*fc*t;
yc1=0.5+0.25*((2/pi)*asin(sin(xc))+1);
yc2=0.25*((2/pi)*asin(sin(xc))+1);
yc3=0.25*((2/pi)*asin(sin(xc))-1);
yc4=-0.5+0.25*((2/pi)*asin(sin(xc))-1);

y=[0; 0; 0; 0];
if(V_H>=yc1)
    %output +Vdc/2 (1/4 1/4)

     y=[1; 0; 1; 0];
elseif(V_H<yc1&&V_H>=yc2)
    %output +1/4Vdc (1/4 0   -----    0 1/4)

     if((ia>=0&&vc1==Cmax)||(ia<0&&vc1==Cmin))
        %use switch combination (ii)
        y=[1; 0; 1; 1];
    else
        %use switch combination (i)
        y=[1; 1; 1; 0];
    end

elseif(V_H<yc2&&V_H>=yc3)
     %output 0Vdc (1/4  -1/4  -----    -1/4 1/4  -------0 0)

    if((ia>=0&&vc1==Cmax)||(ia<0&&vc1==Cmin))
        y=[1; 0; 0; 1];
    elseif((ia>=0&&vc2==Cmax)||(ia<0&&vc2==Cmin))
        y=[0; 1; 1; 0];
    else
        y=[1; 1; 1; 1];
    end
elseif(V_H<yc3&&V_H>=yc4)

    %connect the output to -Vdc/4 (-1/4 0  ------  0 -1/4)
    if((ia>=0&&vc1==Cmin)||(ia<0&&vc1==Cmax))
        %use switch combination (ii)
        y=[0; 1; 1; 1];
    else
        %use switch combination (i)
        y=[1; 1; 0; 1];
    end

else
    %connect the output to -1/2Vdc (-1/4  -1/4)
    y=[0; 1; 0; 1];
end
```

B.2.2 HCMC with 7 H-bridge cells

```
function [sys,x0]=HB_PWM_7Cells(t,x,u,flag)
if(flag==0)
    x0=[];
    sys=[0;0;14;10;0;1];
elseif(flag==3)
    va=u(1);ia=u(2);vc1=u(3);vc2=u(4);vc3=u(5);vc4=u(6);vc5=u(7);vc6=u(8);
    vc7=u(9);vdc=u(10);
    VC=[vc1 vc2 vc3 vc4 vc5 vc6 vc7];
    VCS=sort(VC);
    %Generation of carriers for 10 HB cells arranged as PD
          f=50;
          wt=2*pi*f*t;
          Beta=0;
          xc=27*wt+Beta;
          Kr=2/pi;
          N=15;
          KNorm=1.0;
          TUP=(Kr*asin(sin(xc))+1)/(N-1);
          TLW=(Kr*asin(sin(xc))-1)/(N-1);

           for I=1:(N-1)/2
              Voff1=1-2*I/(N-1);
              K=I+(N-1)/2;
              Voff2=1-2*(K-1)/(N-1);
              yc(I)=Voff1+TUP;
              yc(K)=Voff2+TLW;
           end
             yc=KNorm*yc;
          yc1=yc(1);yc2=yc(2);yc3=yc(3);yc4=yc(4);yc5=yc(5);yc6=yc(6);
          yc7=yc(7);yc8=yc(8);yc9=yc(9);yc10=yc(10);yc11=yc(11);yc12=yc(12);
          yc13=yc(13);yc14=yc(14);
     %end
     %PWM signals generation
     %Let NC is number of cells
%
%      %&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&&
     NC=7;
     if(va>=yc1)
        %+1.0
        for II=1:NC
            sa(II,1)=1;sa(II,3)=0;
        end
     elseif(va<yc1&&va>=yc2)
        %+6/7
        if(ia>=0)
            for II=1:NC
                if(VC(II)==VCS(1))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC
                if(VC(II)==VCS(NC))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
     elseif(va<yc2&&va>=yc3)
        %+5/7
        if(ia>=0)

            for II=1:NC
                if(VC(II)==VCS(1))
                    sa(II,1)=0;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
```

```
            end
        end
    else
        %ia<0
        for II=1:NC
            if(VC(II)==VCS(NC))
                sa(II,1)=0;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    end
elseif(va<yc3&&va>=yc4)
    %+4/7
    if(ia>=0)

        for II=1:NC
            if(VC(II)==VCS(1))
                sa(II,1)=0;sa(II,3)=1;
            elseif(VC(II)==VCS(2))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    else
        %ia<0
        for II=1:NC
            if(VC(II)==VCS(NC))
                sa(II,1)=0;sa(II,3)=1;
            elseif(VC(II)==VCS(NC-1))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    end
elseif(va<yc4&&va>=yc5)
    %+3/7
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
                sa(II,1)=0;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                sa(II,1)=0;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    end
elseif(va<yc5&&va>=yc6)
    %+2/7
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
                sa(II,1)=0;sa(II,3)=1;
            elseif(VC(II)==VCS(3))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    else
        %ia<0
        for II=1:NC
```

```
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                sa(II,1)=0;sa(II,3)=1;
            elseif(VC(II)==VCS(NC-2))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    end
elseif(va<yc6&&va>=yc7)
    %+1/7
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                sa(II,1)=0;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                sa(II,1)=0;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    end
elseif(va<yc7&&va>=yc8)
    %0
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                sa(II,1)=0;sa(II,3)=1;
            elseif(VC(II)==VCS(4))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                sa(II,1)=0;sa(II,3)=1;
            elseif(VC(II)==VCS(NC-3))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=1;sa(II,3)=0;
            end
        end
    end

elseif(va<yc8&&va>=yc9)
    %-1/7

    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                sa(II,1)=1;sa(II,3)=0;
```

```
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc9&&va>=yc10)
    %-2/7
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(NC-2))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(3))
                sa(II,1)=1;sa(II,3)=1;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc10&&va>=yc11)
    %-3/7
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc11&&va>=yc12)
    %-4/7
     if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC)))
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(NC-1))
                sa(II,1)=1;sa(II,3)=1;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1)))
                sa(II,1)=1;sa(II,3)=0;
```

```
            elseif(VC(II)==VCS(2))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc12&&va>=yc13)
    %-5/7
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc13&&va>=yc14)
    %-6/7
     if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC)))
                sa(II,1)=1;sa(II,3)=1;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1)))
                sa(II,1)=1;sa(II,3)=1;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end

else
    %-1
         for II=1:NC

                sa(II,1)=0;sa(II,3)=1;

        end
end


sys=[sa(1,1);sa(1,3);sa(2,1);sa(2,3);sa(3,1);sa(3,3);sa(4,1);sa(4,3);sa(5,1);sa(5,3);
sa(6,1);sa(6,3);sa(7,1);sa(7,3)];
sys=[yc1;yc2;yc3;yc4;yc5;yc6;yc7;yc8;yc9;yc10;yc11;yc12;yc13;yc14];
else
   sys=[];
end
```

B.2.3 HCMC with 10 H-bridge cells

```
function [sys,x0]=HB_PWM_10Cells(t,x,u,flag)
if(flag==0)
    x0=[];
    sys=[0;0;20;13;0;1];
elseif(flag==3)
    va=u(1);ia=u(2);vc1=u(3);vc2=u(4);vc3=u(5);vc4=u(6);vc5=u(7);vc6=u(8);
    vc7=u(9);vc8=u(10);vc9=u(11);vc10=u(12);vdc=u(13);
    VC=[vc1 vc2 vc3 vc4 vc5 vc6 vc7 vc8 vc9 vc10];
    VCS=sort(VC);
    %Generation of carriers for 10 HB cells arranged as PD
          f=50;
          wt=2*pi*f*t;
          Beta=0;
          xc=27*wt+Beta;
          Kr=2/pi;
          N=21;
          KNorm=1.5;
          TUP=(Kr*asin(sin(xc))+1)/(N-1);
          TLW=(Kr*asin(sin(xc))-1)/(N-1);

           for I=1:(N-1)/2
              Voff1=1-2*I/(N-1);
              K=I+(N-1)/2;
              Voff2=1-2*(K-1)/(N-1);
              yc(I)=Voff1+TUP;
              yc(K)=Voff2+TLW;
           end
             yc=KNorm*yc;
          yc1=yc(1);yc2=yc(2);yc3=yc(3);yc4=yc(4);yc5=yc(5);yc6=yc(6);
          yc7=yc(7);yc8=yc(8);yc9=yc(9);yc10=yc(10);yc11=yc(11);yc12=yc(12);
          yc13=yc(13);yc14=yc(14);yc15=yc(15);yc16=yc(16);yc17=yc(17);yc18=yc(18);
          yc19=yc(19);yc20=yc(20);
     %end
     %PWM signals generation
     %Let NC is number of cells
     NC=10;
     if(va>=yc1)
        %+1.5
        for II=1:NC
            sa(II,1)=1;sa(II,3)=0;
        end
     elseif(va<yc1&&va>=yc2)
        %+1.35
        if(ia>=0)
            for II=1:NC
                if(VC(II)==VCS(1))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC
                if(VC(II)==VCS(NC))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
     elseif(va<yc2&&va>=yc3)
        %+1.2
        if(ia>=0)

            for II=1:NC
                if(VC(II)==VCS(1))
                    sa(II,1)=0;sa(II,3)=1;
                else
```

```
            sa(II,1)=1;sa(II,3)=0;
        end
    end
else
    %ia<0
    for II=1:NC
        if(VC(II)==VCS(NC))
            sa(II,1)=0;sa(II,3)=1;
        else
            sa(II,1)=1;sa(II,3)=0;
        end
    end
end
elseif(va<yc3&&va>=yc4)
    %+1.05
    if(ia>=0)

    for II=1:NC
        if(VC(II)==VCS(1))
            sa(II,1)=0;sa(II,3)=1;
        elseif(VC(II)==VCS(2))
            sa(II,1)=1;sa(II,3)=1;
        else
            sa(II,1)=1;sa(II,3)=0;
        end
    end
else
    %ia<0
    for II=1:NC
        if(VC(II)==VCS(NC))
            sa(II,1)=0;sa(II,3)=1;
        elseif(VC(II)==VCS(NC-1))
            sa(II,1)=1;sa(II,3)=1;
        else
            sa(II,1)=1;sa(II,3)=0;
        end
    end
end
elseif(va<yc4&&va>=yc5)
    %+0.9
    if(ia>=0)

    for II=1:NC
        if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
            sa(II,1)=0;sa(II,3)=1;
        else
            sa(II,1)=1;sa(II,3)=0;
        end
    end
else
    %ia<0
    for II=1:NC
        if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
            sa(II,1)=0;sa(II,3)=1;
        else
            sa(II,1)=1;sa(II,3)=0;
        end
    end
end
elseif(va<yc5&&va>=yc6)
    %+0.75
    if(ia>=0)

    for II=1:NC
        if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
            sa(II,1)=0;sa(II,3)=1;
        elseif(VC(II)==VCS(3))
            sa(II,1)=1;sa(II,3)=1;
        else
            sa(II,1)=1;sa(II,3)=0;
        end
    end
else
    %ia<0
```

```
            for II=1:NC
                if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                    sa(II,1)=0;sa(II,3)=1;
                elseif(VC(II)==VCS(NC-2))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
    elseif(va<yc6&&va>=yc7)
        %+0.6
        if(ia>=0)

            for II=1:NC
                if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                    sa(II,1)=0;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC
                if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                    sa(II,1)=0;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
    elseif(va<yc7&&va>=yc8)
        %+0.45
        if(ia>=0)

            for II=1:NC
                if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                    sa(II,1)=0;sa(II,3)=1;
                elseif(VC(II)==VCS(4))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC
                if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                    sa(II,1)=0;sa(II,3)=1;
                elseif(VC(II)==VCS(NC-3))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
    elseif(va<yc8&&va>=yc9)
        %+0.3
        if(ia>=0)

            for II=1:NC

if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3))||(VC(II)==VCS(4)))
                    sa(II,1)=0;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC

if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2))||(VC(II)==VCS(NC-3)))
                    sa(II,1)=0;sa(II,3)=1;
```

```
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
    elseif(va<yc9&&va>=yc10)
        %+0.15
        if(ia>=0)

            for II=1:NC

if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3))||(VC(II)==VCS(4)))
                    sa(II,1)=0;sa(II,3)=1;
                elseif(VC(II)==VCS(5))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC

if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2))||(VC(II)==VCS(NC-3)))
                    sa(II,1)=0;sa(II,3)=1;
                elseif(VC(II)==VCS(NC-4))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
    elseif(va<yc10&&va>=yc11)
        %0
        if(ia>=0)

            for II=1:NC

if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3))||(VC(II)==VCS(4))||(VC(II)==V
CS(5)))
                    sa(II,1)=0;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        else
            %ia<0
            for II=1:NC

if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2))||(VC(II)==VCS(NC-3))||
(VC(II)==VCS(NC-4)))
                    sa(II,1)=0;sa(II,3)=1;
                else
                    sa(II,1)=1;sa(II,3)=0;
                end
            end
        end
    elseif(va<yc11&&va>=yc12)
        %-0.15
        if(ia>=0)

            for II=1:NC

if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2))||(VC(II)==VCS(NC-3)))
                    sa(II,1)=1;sa(II,3)=0;
                elseif(VC(II)==VCS(NC-4))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        else
            %ia<0
            for II=1:NC
```

```
if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3))||(VC(II)==VCS(4)))
                    sa(II,1)=1;sa(II,3)=0;
                elseif(VC(II)==VCS(5))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        end
    elseif(va<yc12&&va>=yc13)
        %-0.3
         if(ia>=0)

            for II=1:NC

if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2))||(VC(II)==VCS(NC-3)))
                    sa(II,1)=1;sa(II,3)=0;

                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        else
            %ia<0
            for II=1:NC

if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3))||(VC(II)==VCS(4)))
                    sa(II,1)=1;sa(II,3)=0;

                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        end
    elseif(va<yc13&&va>=yc14)
        %-0.45
        if(ia>=0)

            for II=1:NC
                if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                    sa(II,1)=1;sa(II,3)=0;
                elseif(VC(II)==VCS(NC-3))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        else
            %ia<0
            for II=1:NC
                if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                    sa(II,1)=1;sa(II,3)=0;
                elseif(VC(II)==VCS(4))
                    sa(II,1)=1;sa(II,3)=1;
                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        end
    elseif(va<yc14&&va>=yc15)
        %-0.6
        if(ia>=0)

            for II=1:NC
                if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1))||(VC(II)==VCS(NC-2)))
                    sa(II,1)=1;sa(II,3)=0;

                else
                    sa(II,1)=0;sa(II,3)=1;
                end
            end
        else
            %ia<0
```

```
        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2))||(VC(II)==VCS(3)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc15&&va>=yc16)
    %-0.75
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(NC-2))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(3))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc16&&va>=yc17)
    %-0.9
     if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC))||(VC(II)==VCS(NC-1)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1))||(VC(II)==VCS(2)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc17&&va>=yc18)
    %-1.05
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC)))
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(NC-1))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1)))
```

```
                sa(II,1)=1;sa(II,3)=0;
            elseif(VC(II)==VCS(2))
                sa(II,1)=1;sa(II,3)=1;
            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc18&&va>=yc19)
    %-1.2
     if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1)))
                sa(II,1)=1;sa(II,3)=0;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
elseif(va<yc19&&va>=yc20)
    %-1.35
    if(ia>=0)

        for II=1:NC
            if((VC(II)==VCS(NC)))
                sa(II,1)=1;sa(II,3)=1;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    else
        %ia<0
        for II=1:NC
            if((VC(II)==VCS(1)))
                sa(II,1)=1;sa(II,3)=1;

            else
                sa(II,1)=0;sa(II,3)=1;
            end
        end
    end
else
    %-1.5
         for II=1:NC

                sa(II,1)=0;sa(II,3)=1;

        end
end


sys=[sa(1,1);sa(1,3);sa(2,1);sa(2,3);sa(3,1);sa(3,3);sa(4,1);sa(4,3);sa(5,1);sa(5,3);
sa(6,1);sa(6,3);sa(7,1);sa(7,3);sa(8,1);sa(8,3);sa(9,1);sa(9,3);sa(10,1);sa(10,3)];
else
   sys=[];
end
```

B.2.4 HCMC with 2 H-bridge cells using SPWM with 3rd harmonic subtraction

```
function y=Modulator(t,u)

va=u(1);
ia=u(2);
vc1=u(3);
vc2=u(4);
vdc=u(5);
w=100*pi;
xc=27*w*t;
x3=3*w*t;
Y=va-sqrt(2)/pi*sin(x3);
k=2/pi;
yc1=0.75+0.125*((2/pi)*asin(sin(xc))+1);
yc2=0.5+0.125*((2/pi)*asin(sin(xc))+1);
yc3=0.25+0.125*((2/pi)*asin(sin(xc))+1);
yc4=0.125*((2/pi)*asin(sin(xc))+1);
yc5=0.125*((2/pi)*asin(sin(xc))-1);
yc6=-0.25+0.125*((2/pi)*asin(sin(xc))-1);
yc7=-0.5+0.125*((2/pi)*asin(sin(xc))-1);
yc8=-0.75+0.125*((2/pi)*asin(sin(xc))-1);

V_C=[vc1,vc2];
Cmax=max(V_C);Cmin=min(V_C);

y=[0; 0; 0; 0; 0];
if(Y>=yc1)
    %output +Vdc (1/2 1/4 1/4)

     y=[1; 1; 0; 1; 0];
elseif(Y<yc1&&Y>=yc2)
    %output +3/4Vdc (1/2 1/4 0   -----   1/2 0 1/4)

    if((ia>=0&&vc1==Cmax)||(ia<0&&vc1==Cmin))
        %use switch combination (ii)
        y=[1; 1; 0; 1; 1];
    else
        %use switch combination (i)
        y=[1; 1; 1; 1; 0];
    end

elseif(Y<yc2&&Y>=yc3)
    %output +1/2Vdc (1/2 0 0   -----   1/2 0 0)

   y=[1; 1; 1; 1; 1];

elseif(Y<yc3&&Y>=yc4)
    %output +1/4Vdc (1/2 -1/4 0   -----   1/2 0 1/4)

    if((ia>=0&&vc1==Cmin)||(ia<0&&vc1==Cmax))
        %use switch combination (ii)
        y=[1; 0; 1; 1; 1];
    else
        %use switch combination (i)
        y=[1; 1; 1; 0; 1];
    end

elseif(Y<yc4&&Y>=yc5)

    %connect the output to 0 (1/2 -1/4 -1/4  -------  -1/2 1/4 1/4)
    if((ia>=0&&Cmin>=vdc/4)||(ia<0&&Cmax<vdc/4))
      y=[0; 1; 0; 1; 0];
    else
       y=[1; 0; 1; 0; 1];
    end

elseif(Y<yc5&&Y>=yc6)
    %connect the output to -Vdc/4 (-1/2 1/4 0  ------  -1/2 0 1/4)
    if((ia>=0&&vc1==Cmax)||(ia<0&&vc1==Cmin))
        %use switch combination (ii)
        y=[0; 1; 0; 1; 1];
    else
```

```
        %use switch combination (i)
        y=[0; 1; 1; 1; 0];
    end

elseif(Y<yc6&&Y>=yc7)
    %output -1/2Vdc (-1/2 0 0   -----   -1/2 0 0)

   y=[0; 1; 1; 1; 1];

elseif(Y<yc7&&Y>=yc8)
    %output -3/4Vdc (-1/2 -1/4 0   -----   -1/2 0 -1/4)

    if((ia>=0&&vc1==Cmin)||(ia<0&&vc1==Cmax))
        %use switch combination (ii)
        y=[0; 0; 1; 1; 1];
    else
        %use switch combination (i)
        y=[0; 1; 1; 0; 1];
    end

else
    %connect the output to -Vdc
    y=[0; 0; 1; 0; 1];
end
```

B.3 Program code for experimental validation

B.3.1 Three-level single-phase M2C

```
function y = fcn(u)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
va=u(1);ia=u(2);vc1=u(3);vc2=u(4);vc3=u(5);vc4=u(6);
fs=2100;Ts=1/fs;DT=1.25e-6;KT=10e6;

if(va>=0)
    %Positive half cycle of reference voltage
    T1=Ts*(1-va);
    if(ia>=0)
        %During positve half of phase current
        if(vc1<vc2&&vc4>vc3)
            %select switch state (i)
            P_index=1;
        elseif(vc1<vc2&&vc3>vc4)
            %select switch state (ii)
            P_index=2;
        elseif(vc2<vc1&&vc4>vc3)
            %select switch state (iii)
            P_index=3;
        else
            %select switch state (iv)
            P_index=4;
        end
    else
        %During negative half of phase current
        if(vc1>vc2&&vc4<vc3)
            %select switch state (i)
            P_index=1;
        elseif(vc1>vc2&&vc3<vc4)
            %select switch state (ii)
            P_index=2;
        elseif(vc2>vc1&&vc4<vc3)
            %select switch state (iii)
            P_index=3;
        else
            %select switch state (iv)
            P_index=4;
        end
    end
else
    %Negative half cycle of reference voltage
    T1=-Ts*va;
    if(ia>=0)
        %During positve half of phase current
        if(vc1<vc2&&vc4>vc3)
            %select switch state (i)
            P_index=-1;
        elseif(vc1<vc2&&vc3>vc4)
            %select switch state (ii)
            P_index=-2;
        elseif(vc2<vc1&&vc4>vc3)
            %select switch state (iii)
            P_index=-3;
        else
            %select switch state (iv)
            P_index=-4;
        end
    else
        %During negative half of phase current
        if(vc1>vc2&&vc4<vc3)
            %select switch state (i)
            P_index=-1;
        elseif(vc1>vc2&&vc3<vc4)
            %select switch state (ii)
            P_index=-2;
```

```
        elseif(vc2>vc1&&vc4<vc3)
            %select switch state (iii)
            P_index=-3;
        else
            %select switch state (iv)
            P_index=-4;
        end
    end
end

%Determination of rising and falling edges of the PWM signals
if(P_index==1)
    %Sa1 and Sx1
    Tra1=T1+DT;Tfa1=Ts-DT;
    Trx1=DT;Tfx1=T1-DT;
    %Sa2 and Sx2
    Tra2=DT;Tfa2=Ts-DT;
    Trx2=0;Tfx2=0;
    %Sa3 and Sx3
    Tra3=DT;Tfa3=T1-DT;
    Trx3=T1+DT;Tfx3=Ts-DT;
    %Sa4 and Sx4
    Tra4=0;Tfa4=0;
    Trx4=DT;Tfx4=Ts-DT;

elseif(P_index==2)
    %Sa1 and Sx1
    Tra1=T1+DT;Tfa1=Ts-DT;
    Trx1=DT;Tfx1=T1-DT;
    %Sa2 and Sx2
    Tra2=DT;Tfa2=Ts-DT;
    Trx2=0;Tfx2=0;
    %Sa3 and Sx3
    Tra3=0;Tfa3=0;
    Trx3=DT;Tfx3=Ts-DT;
    %Sa4 and Sx4
    Tra4=DT;Tfa4=T1-DT;
    Trx4=T1+DT;Tfx4=Ts-DT;
elseif(P_index==3)
    %Sa1 and Sx1
    Tra1=DT;Tfa1=Ts-DT;
    Trx1=0;Tfx1=0;
    %Sa2 and Sx2
    Tra2=T1+DT;Tfa2=Ts-DT;
    Trx2=DT;Tfx2=T1-DT;
    %Sa3 and Sx3
    Tra3=DT;Tfa3=T1-DT;
    Trx3=T1+DT;Tfx3=Ts-DT;
    %Sa4 and Sx4
    Tra4=0;Tfa4=0;
    Trx4=DT;Tfx4=Ts-DT;
elseif(P_index==4)
    %Sa1 and Sx1
    Tra1=DT;Tfa1=Ts-DT;
    Trx1=0;Tfx1=0;
    %Sa2 and Sx2
    Tra2=T1+DT;Tfa2=Ts-DT;
    Trx2=DT;Tfx2=T1-DT;
    %Sa3 and Sx3
    Tra3=0;Tfa3=0;
    Trx3=DT;Tfx3=Ts-DT;
    %Sa4 and Sx4
    Tra4=DT;Tfa4=T1-DT;
    Trx4=T1+DT;Tfx4=Ts-DT;
elseif(P_index==-1)
    %Sa1 and Sx1
    Tra1=0;Tfa1=0;
    Trx1=DT;Tfx1=Ts-DT;
    %Sa2 and Sx2
    Tra2=T1+DT;Tfa2=Ts-DT;
    Trx2=DT;Tfx2=T1-DT;
    %Sa3 and Sx3
    Tra3=DT;Tfa3=Ts-DT;
    Trx3=0;Tfx3=0;
```

```
    %Sa4 and Sx4
    Tra4=DT;Tfa4=T1-DT;
    Trx4=T1+DT;Tfx4=Ts-DT;
elseif(P_index==-2)
    %Sa1 and Sx1
    Tra1=0;Tfa1=0;
    Trx1=DT;Tfx1=Ts-DT;
    %Sa2 and Sx2
    Tra2=T1+DT;Tfa2=Ts-DT;
    Trx2=DT;Tfx2=T1-DT;
    %Sa3 and Sx3
    Tra3=DT;Tfa3=T1-DT;
    Trx3=T1+DT;Tfx3=Ts-DT;
    %Sa4 and Sx4
    Tra4=DT;Tfa4=Ts-DT;
    Trx4=0;Tfx4=0;
elseif(P_index==-3)
    %Sa1 and Sx1
    Tra1=T1+DT;Tfa1=Ts-DT;
    Trx1=DT;Tfx1=T1-DT;
    %Sa2 and Sx2
    Tra2=0;Tfa2=0;
    Trx2=DT;Tfx2=Ts-DT;
    %Sa3 and Sx3
    Tra3=DT;Tfa3=Ts-DT;
    Trx3=0;Tfx3=0;
    %Sa4 and Sx4
    Tra4=DT;Tfa4=T1-DT;
    Trx4=T1+DT;Tfx4=Ts-DT;
else
    %P_index==-4
    %Sa1 and Sx1
    Tra1=T1+DT;Tfa1=Ts-DT;
    Trx1=DT;Tfx1=T1-DT;
    %Sa2 and Sx2
    Tra2=0;Tfa2=0;
    Trx2=DT;Tfx2=Ts-DT;
    %Sa3 and Sx3
    Tra3=DT;Tfa3=T1-DT;
    Trx3=T1+DT;Tfx3=Ts-DT;
    %Sa4 and Sx4
    Tra4=DT;Tfa4=Ts-DT;
    Trx4=0;Tfx4=0;
end
y = [Tra1 Tfa1 Trx1 Tfx1 Tra2 Tfa2 Trx2 Tfx2 Tra3 Tfa3 Trx3 Tfx3 Tra4 Tfa4 Trx4 Tfx4]*KT;
```

B.3.2 HCMC with 2 H-bridge cells using independent control

Part 1: Two-level converter

```
function [Ton_H,Toff_H,VT] = fcn(M,Fs,F,T_PWM_COUNT,Q, Theta)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
W=2*pi*F;
Ts=1/Fs;
a=0.5*(1+0.25*pi*M);b=acos(a);
c=W*Ts;
N=Fs/F;
II=Theta/c;
N1=floor(b/c);N2=N/2-N1;N3=N/2;N4=N/2+N1;N5=N-N1;

if (II<N3)
   if ((II<=N1)||(II>=N2))

      Ton_H=T_PWM_COUNT/2;
      Toff_H=T_PWM_COUNT/2;
      VT=-1;

   else
      Ton_H=Q;
      Toff_H=T_PWM_COUNT-Q;
       VT=1;
    end
else
    if((II<N4)||(II>=N5))
      Ton_H=Q;
      Toff_H=T_PWM_COUNT-Q;
      VT=1;

    else
       Ton_H=T_PWM_COUNT/2;
       Toff_H=T_PWM_COUNT/2;
       VT=-1;
     end
end
```

Part 2: H-bridge cells

```
function [Tr11,Tf11,Tr13,Tf13,Tr21,Tf21,Tr23,Tf23]= fcn(va,ia,vc1,vc2,T_PWM_COUNT,Q)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
Ts=T_PWM_COUNT;
N=2;
Vc=[vc1 vc2];
Kmax=max(Vc);Kmin=min(Vc);
Txr=zeros(2,3);Txf=zeros(2,3);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
if(va>=0.5)
    %Swithcing between 1/2Vdc to 1/4 Vdc
    Th=Ts*(2*va-1);T1=Ts-Th;
    if(ia>=0)
        for II=1:2
            if(Vc(II)==Kmax)
                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
            else
                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Q;Txf(II,3)=T1;
            end
        end

    else
        %ia<0
        for II=1:2
            if(Vc(II)==Kmin)
                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
```

```
                Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
            else
                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Q;Txf(II,3)=T1;
            end
        end
    end
elseif(va<0.5&&va>=0)
    %switching between 1/4Vdc and 0Vdc
    Th=2*Ts*va;T1=Ts-Th;
    if(ia>=0)
           for II=1:2
               if(Vc(II)==Kmax)
                   Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                   Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
               else
                   Txr(II,1)=T1;Txf(II,1)=Ts;
                   Txr(II,3)=Q;Txf(II,3)=Ts-Q;
               end
           end

    else
        %ia<0
           for II=1:2
               if(Vc(II)==Kmin)
                   Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                   Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
               else
                   Txr(II,1)=T1;Txf(II,1)=Ts;
                   Txr(II,3)=Q;Txf(II,3)=Ts-Q;
               end
           end
    end

  elseif(va<0&&va>=-0.5)
    %switching between 0Vdc and -1/4Vdc
    Th=Ts*(1+2*va);T1=Ts-Th;
    if(ia>=0)
           for II=1:2
               if(Vc(II)==Kmin)
                   Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
                   Txr(II,3)=Q;Txf(II,3)=Ts-Q;
               else
                   Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                   Txr(II,3)=Q;Txf(II,3)=T1;
               end
           end
    else
        %ia<0
           for II=1:2
               if(Vc(II)==Kmax)
                   Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
                   Txr(II,3)=Q;Txf(II,3)=Ts-Q;
               else
                   Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                   Txr(II,3)=Q;Txf(II,3)=T1;
               end
           end
    end

  else
    %switching between -1/4Vdc and -1/2Vdc
    Th=2*Ts*(1+va);T1=Ts-Th;
    if(ia>=0)
        for II=1:2
           if(Vc(II)==Kmin)
               Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
               Txr(II,3)=Q;Txf(II,3)=Ts-Q;
           else
               Txr(II,1)=Q;Txf(II,1)=Th;
               Txr(II,3)=Q;Txf(II,3)=Ts-Q;
           end
        end
```

```
    else
        %ia<0
        for II=1:2
            if(Vc(II)==Kmax)
                Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
                Txr(II,3)=Q;Txf(II,3)=Ts-Q;
            else
                Txr(II,1)=Q;Txf(II,1)=Th;
                Txr(II,3)=Q;Txf(II,3)=Ts-Q;
            end
        end
    end

end

Tr11=Txr(1,1);Tf11=Txf(1,1);Tr13=Txr(1,3);Tf13=Txf(1,3);
Tr21=Txr(2,1);Tf21=Txf(2,1);Tr23=Txr(2,3);Tf23=Txf(2,3);
```

B.3.3 HCMC with 2 H-bridge cells using SPWM with 3rd harmonic subtraction

```
function [Tr11,Tf11,Tr13,Tf13,Tr21,Tf21,Tr23,Tf23,Ton_H,Toff_H]=
fcn(va,ia,vc1,vc2,T_PWM_COUNT,Q,vdc)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
Ts=T_PWM_COUNT;
Ton_H=0;Toff_H=0;
N=2;
Vc=[vc1 vc2];
Kmax=max(Vc);Kmin=min(Vc);
Txr=zeros(2,3);Txf=zeros(2,3);
%%%%%%%%%%%%%%%%%%%% %Swithcing between Vdc to 3/4
Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
if(va>=1.5)

    Th=Ts*(4*va-3);
    Ton_H=Q;Toff_H=Ts-Q;
    if(ia>=0)

        for II=1:2
            if(Vc(II)==Kmax)

                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
            else

                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Th;Txf(II,3)=Ts-Q;
            end
        end

    else
        %ia<0

        for II=1:2
            if(Vc(II)==Kmin)

                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
            else

                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Th;Txf(II,3)=Ts-Q;
            end
        end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%switching between 3/4Vdc and
1/2Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    elseif(va<1.5&&va>=1)

    Th=Ts*(4*va-2);
    Ton_H=Q;Toff_H=Ts-Q;
```

```
    if(ia>=0)

            for II=1:2
                if(Vc(II)==Kmax)

                    Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                    Txr(II,3)=Th;Txf(II,3)=Ts-Q;
                else

                    Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                    Txr(II,3)=Q;Txf(II,3)=Ts-Q;
                end
            end

    else
        %ia<0

            for II=1:2
                if(Vc(II)==Kmin)

                    Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                    Txr(II,3)=Th;Txf(II,3)=Ts-Q;
                else

                    Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                    Txr(II,3)=Q;Txf(II,3)=Ts-Q;
                end
            end
    end
%%%%%%%%%%%%%%%%%switching between 1/2Vdc and
1/4Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
     elseif(va<1&&va>0.5)

    Th=Ts*(4*va-1);
    Ton_H=Q;Toff_H=Ts-Q;
    if(ia>=0)

            for II=1:2
                if(Vc(II)==Kmin)

                    Txr(II,1)=Q;Txf(II,1)=Th;
                    Txr(II,3)=Q;Txf(II,3)=Ts-Q;
                else

                    Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                    Txr(II,3)=Q;Txf(II,3)=Ts-Q;
                end
            end

    else
        %ia<0

            for II=1:2
                if(Vc(II)==Kmax)

                    Txr(II,1)=Q;Txf(II,1)=Th;
                    Txr(II,3)=Q;Txf(II,3)=Ts-Q;
                else

                    Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                    Txr(II,3)=Q;Txf(II,3)=Ts-Q;
                end
            end
    end
%%%%%%%%%%%%%%%%%%switching between 1/4Vdc and
0Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    elseif(va<0.5&&va>=0)
    %switching between 1/4Vdc and 0Vdc
    Th=Ts*(4*va);
    if(ia>=0)
        if(Kmin>vdc/4)
            Ton_H=Q;Toff_H=Th;
            for II=1:2
              if(Vc(II)==Kmin)
```

```
                Txr(II,1)=Th;Txf(II,1)=Ts-Q;
                Txr(II,3)=Q;Txf(II,3)=Th;

            else

                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Q;Txf(II,3)=Th;
            end
          end
       else
           Ton_H=Q;Toff_H=Ts-Q;
          for II=1:2
            if(Vc(II)==Kmin)

               Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
               Txr(II,3)=Q;Txf(II,3)=Ts-Q;

            else

                Txr(II,1)=Q;Txf(II,1)=Th;
                Txr(II,3)=Q;Txf(II,3)=Ts-Q;
            end
          end
        end

   else
       %ia<0
        Ton_H=Q;Toff_H=Th;
       if(Kmax<vdc/4)
          for II=1:2
            if(Vc(II)==Kmax)

               Txr(II,1)=Th;Txf(II,1)=Ts-Q;
               Txr(II,3)=Q;Txf(II,3)=Th;

            else

                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Q;Txf(II,3)=Th;
            end
          end
       else
          Ton_H=Q;Toff_H=Ts-Q;
          for II=1:2
            if(Vc(II)==Kmax)

               Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
               Txr(II,3)=Q;Txf(II,3)=Ts-Q;

            else

                Txr(II,1)=Q;Txf(II,1)=Th;
                Txr(II,3)=Q;Txf(II,3)=Ts-Q;
            end
          end
        end
   end

%%%%%%%%%%%%%%%%%% %switching between 0Vdc and
-1/4Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
   elseif(va<0&&va>=-0.5)
    %switching between 0Vdc and -1/4Vdc
    Th=Ts*(4*va+1);
    if(ia>=0)
       for II=1:2
          if(Kmin>0.25*vdc)
             Ton_H=Ts/2;Toff_H=Ts/2;
             if(Vc(II)==Kmax)
                 Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                 Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
             else
                 Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                 Txr(II,3)=Th;Txf(II,3)=Ts;
```

```
            end
        else
            Ton_H=Q;Toff_H=Th;
            if(Vc(II)==Kmax)
                Txr(II,1)=Th;Txf(II,1)=Ts-Q;
                Txr(II,3)=0;Txf(II,3)=Th;
            else
                Txr(II,1)=Th;Txf(II,1)=Ts;
                Txr(II,3)=Q;Txf(II,3)=Ts-Q;
            end
        end
    end
else
    %ia<0
    for II=1:2
        if(Kmax<0.25*vdc)
            Ton_H=Ts/2;Toff_H=Ts/2;
            if(Vc(II)==Kmin)
                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Ts/2;Txf(II,3)=Ts/2;
            else
                Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                Txr(II,3)=Th;Txf(II,3)=Ts;
            end
        else
            Ton_H=Q;Toff_H=Th;
            if(Vc(II)==Kmin)
                Txr(II,1)=Th;Txf(II,1)=Ts;
                Txr(II,3)=Q;Txf(II,3)=Th;
            else
                Txr(II,1)=Th;Txf(II,1)=Ts-Q;
                Txr(II,3)=Q;Txf(II,3)=Ts-Q;
            end
        end
    end
end
%%%%%%%%%%%%%%%%%%%%%%switching between -1/4Vdc and
-1/2Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    elseif(va<-0.5&&va>=-1)

    Th=Ts*(4*va+2);
    Ton_H=Ts/2;Toff_H=Ts/2;
    if(ia>=0)

          for II=1:2
              if(Vc(II)==Kmax)

                  Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                  Txr(II,3)=Th;Txf(II,3)=Ts-Q;
              else

                  Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                  Txr(II,3)=Q;Txf(II,3)=Ts-Q;
              end
          end

    else
        %ia<0

          for II=1:2
              if(Vc(II)==Kmin)

                  Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                  Txr(II,3)=Th;Txf(II,3)=Ts-Q;
              else

                  Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                  Txr(II,3)=Q;Txf(II,3)=Ts-Q;
              end
          end
    end
 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%switching between -1/2Vdc and
-3/4Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
   elseif(va<-1&&va>=-1.5)
```

```
    Th=Ts*(4*va+3);
    Ton_H=Ts/2;Toff_H=Ts/2;
    if(ia>=0)

           for II=1:2
              if(Vc(II)==Kmin)

                 Txr(II,1)=Q;Txf(II,1)=Th;
                 Txr(II,3)=Q;Txf(II,3)=Ts-Q;
              else

                 Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                 Txr(II,3)=Q;Txf(II,3)=Ts-Q;
              end
           end

    else
       %ia<0

           for II=1:2
              if(Vc(II)==Kmax)

                 Txr(II,1)=Q;Txf(II,1)=Th;
                 Txr(II,3)=Q;Txf(II,3)=Ts-Q;
              else

                 Txr(II,1)=Q;Txf(II,1)=Ts-Q;
                 Txr(II,3)=Q;Txf(II,3)=Ts-Q;
              end
           end
    end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%switching between -3/4Vdc and
-Vdc%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    else

    Th=Ts*(4*va+4);
    Ton_H=Ts/2;Toff_H=Ts/2;
    if(ia>=0)

       for II=1:2
          if(Vc(II)==Kmin)

             Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
             Txr(II,3)=Q;Txf(II,3)=Ts-Q;
          else

             Txr(II,1)=Q;Txf(II,1)=Th;
             Txr(II,3)=Q;Txf(II,3)=Ts-Q;
          end
       end

    else
       %ia<0

       for II=1:2
          if(Vc(II)==Kmax)

             Txr(II,1)=Ts/2;Txf(II,1)=Ts/2;
             Txr(II,3)=Q;Txf(II,3)=Ts-Q;
          else

             Txr(II,1)=Q;Txf(II,1)=Th;
             Txr(II,3)=Q;Txf(II,3)=Ts-Q;
          end
       end
    end

end

Tr11=Txr(1,1);Tf11=Txf(1,1);Tr13=Txr(1,3);Tf13=Txf(1,3);
Tr21=Txr(2,1);Tf21=Txf(2,1);Tr23=Txr(2,3);Tf23=Txf(2,3);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

C List of Tables and Figures

C.1 List of Figures

C.2 List of Tables

D Published Work by the Author

1. Yushu Zhang, G.P. Adam, T.C.Lim, Stephen J. Finney, Barry W. Williams, "Voltage Source Converter in High Voltage Applications: Multilevel versus Two-level Converters," The IET conference on AC and DC power transmission (ACDC 2010), London, 2010.

Abstract:

The Modular Multilevel Converter (M2C) is an emerging and highly attractive multilevel converter topology for medium and high voltage applications. This paper presents a detail comparison between the two-level and 17-level M2C when used in medium-voltage (MV) applications. The comparison focuses on the practical issues such as waveform quality, switching frequency per device and conversion looses (conduction losses and switching losses).

2. Yushu Zhang, G.P. Adam, T.C.Lim, Stephen J. Finney, Barry W. Williams, "Analysis and Experiment Validation of a Three-level Modular Multilevel Converter," 8th International Conference on Power Electronics—ECCE Asia (IEEE ICPE-ECCE Asia), Korea, 2011.

Abstract:

This paper presents analysis of the effect of modulation strategy on the modular multilevel converter including sub-module capacitor size calculation, capacitor ripple and capacitor balancing strategy. Simulation and experimental results validate the analysis presented and some features such as effective switching frequency per device and current and voltage stress on each device compared to other methods, are addressed.

3. Yushu Zhang, G.P. Adam, T.C.Lim, Stephen J. Finney, Barry W. Williams, "Mathematical Analysis and Experiment Validation of Modular Multilevel Converter," Korean Journal of Power Electronics, JPE Vol. 12, No. 1 January, 2012.

Abstract:

This paper describes operating and capacitor voltage balancing of the modular multilevel converter. The paper focuses on sizing of the cell capacitor and establishes approximate expressions for the capacitor voltage. Simulations and experiments results obtained from three-level modular converter are used to demonstrate its viability in medium voltage applications. It is shown that the modular converter can operate over the full modulation index linear range independent of load power factor.

4. Yushu Zhang, G.P. Adam, T.C.Lim, Stephen J. Finney, Barry W. Williams, "Hybrid Multilevel Converter: Capacitor Voltage Balancing Limits and its Extension," IEEE Transactions on Industrial Informatics special issue on Digital Control System in Power Electronics and Electrical Drives, 2012, Accepted.

Abstract:

This paper presents theoretical analysis of a network fault tolerant hybrid cascaded multilevel converter when operated as one unit using multilevel pulse width modulation. Based on this analysis the modulation index range is established where voltage balance of the H-bridge floating capacitors of the hybrid converter can be attained independent of load power factors. A strategy is proposed for the extension of the modulation index linear range where the hybrid cascaded multilevel converter can be operated independent of load power factor and capacitor voltage balancing problems. The validity of the theoretical analysis and proposed extended modulation index linear range have been confirmed using simulations and experimentation. The presented analysis and proposed modulation linear range extension can be extended to hybrid converter with a large number of H-bridge cells.

5. Yushu Zhang, G.P. Adam, T.C.Lim, Stephen J. Finney, Barry W. Williams, "A Hybrid Cascaded Multilevel Converter," IEEE Transactions on Power Electronics, submitted.

Abstract:

This paper re-introduces a hybrid multilevel converter which is capable of operating independent of load power factor, modulation index and suitable for medium to

high-voltage applications. This is achieve by adopting a new modulation strategy that utilizes third harmonic subtraction in order to offer a set of advantages: wide modulation index linear range, small required capacitor size and smaller footprint, zero net power exchange between the cell capacitors and load is guaranteed over the entire operating conditions. This paper establishes an optimal magnitude of third harmonic to be subtracted by the H-bridge cells to ensure proper converter operation. The validity of the presented modulation and capacitor voltage balancing is confirmed by simulation and experimentation on a scale model and prototype. The scalability of the hybrid multilevel converters to high-voltage applications is demonstrated using simulations, including start-up and shut down without the need for auxiliary circuitry.