Modelling, Control and Analysis of HVDC Voltage-Source Converters in Weak AC Grids

PhD Thesis

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18th June 2023

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Contents

Abstract

An increase in renewable and distributed electricity generation, long-distance transmission, and interconnected power grids means that the prevalence of converter-based systems in the power network has increased rapidly over the last 30 years, and is expected to rise further over the coming decades. The high penetration of converter-based generation in the UK and in many other power systems worldwide presents a challenge for power system control because the high impedance of these systems represents a reduction in the local short circuit ratio (SCR) of the grid. A low SCR, known as a weak grid, in turn presents challenges for the stability and control of additional power converters that are connected to the AC network. The AC power grid of the future will require converter control that can operate safely, maintain stability, and provide rated power transfer even in these weakening grid conditions. This is particularly pertinent for high-voltage, direct-current (HVDC) transmission for two reasons. Firstly, because HVDC is used to transmit power over long distances from a high-supply, low-demand region, one or both converter stations are likely to be in a particularly weak grid area with little or no synchronous generation. Secondly, HVDC transmission almost always involves very high power transfer, which decreases the effective short circuit ratio 'seen' by the converter and exacerbates the control problem. This thesis therefore addresses some of the key challenges surrounding the control of voltage-source converter (VSC)-HVDC in very weak AC grids.

This work presents modelling techniques, stability analyses and comprehensive assessment methods for different grid-following and grid-forming of voltage-source converter controllers. Linearized small-signal models are developed for conventional vector current control, power synchronization control and a simple virtual synchronous ma-

chine controller. Other linearised modelling approaches such as impedance models and the Jacobian transfer matrix model are also discussed. To validate and extend the results of linearised analysis, a number of time-domain simulation and modelling techniques are also presented. These include an averaged model in MATLAB/Simulink and switching models running in a control hardware-in-the-loop (CHiL) setup on two types of real time digital simulator (RTDS).

The purpose of the small-signal and time-domain analyses is to investigate the absolute stability limits of each type of control and to describe the interactions that occur between different controller elements when operating in very weak AC grids. The stable operating space for the controller tunings of vector current control and power synchronization control is described under a number of dynamic performance and grid strength constraints, giving tuning recommendations and maximum performance limits. The stability analysis developed is then used to propose a standardized assessment framework for any VSC controller in a very weak AC grid. The objective of this framework is to provide a standardized set of time and frequency domain tests that can be applied to any grid-connected VSC. The assessment should be applicable to any type of weak grid-connected VSC controller at any level of implementation (e.g. small-signal analytical model through to operational controllers implemented in hardware). This comprehensive assessment framework is used to compare the vector current control, power synchronization control and virtual synchronous machine controllers using small-signal models, time-domain simulations and control hardware-in-the-loop RTDS experiments to demonstrate the versatility and robustness of the proposed framework for controllers with very different structures.

The final area of research in this thesis is the concept of dual-infeed VSC-HVDC in weak grid areas. The increasing number of HVDC infeeds inevitably means that high-power converter systems are operating in increasingly close electrical proximity. Interactions between controllers on different infeeds, and the implications that this has for optimum tuning are investigated. The effect of the strength of the coupling between infeeds (modelled by varying tie-line impedance) and the impact of high frequency resonances in dual-infeed systems are also investigated. Both small-signal analytical

modelling and control hardware-in-the-loop RTDS experiments are used to perform these analyses, with additional discussion on the modelling of time delays in analytical dual-infeed systems.

Acknowledgements

Above all I would like to thank my supervisors, Dr. Khaled Ahmed and Dr. Agustí Egea-Àlvarez, for their expert guidance, continuous support and good humour throughout my studies. Special mention must be made of their abundant patience in coaxing polite review responses out of a forthright Yorkshire-woman.

Thanks also go to all those at the Wind & Marine Energy Systems CDT who have been dependable friends and drinking partners for the last four years, and particularly to Drew Smith for his tireless attempts to keep us all in line. Similarly, I am immensely grateful to all those in the PEDEC group at the University of Strathclyde for enduring my most stupid questions.

To all the folks that I have lived with over the years in Glasgow - Jess Knapton, Tom Craven, Eloise Myers, Lara Tulloch, Anna Stephens and Allison Graham - I extend my sincere thanks for your excellent acting skills and impressive patience when enduring unintelligible monologues about power electronics.

Last but very much not least, I am incredibly grateful to my family for their support throughout my life. Thank you to my brother, Sam, for always being willing to watch Lord of the Rings in grumpy silence whenever required, and most of all to my parents for first instilling in me a love of science. They have since provided support, wise counsel and a sympathetic ear at all times, as well as suffering through many research-inspired tantrums during the lockdown period. I could not be where I am today without them.

Chapter 0. Acknowledgements

Chapter 1

Introduction

1.1 Background

1.1.1 Evolving Power Systems

The latest report by the Intergovernmental Panel on Climate Change (IPCC) confirms that the climate crisis is accelerating at an alarming rate, and any hope of halting a devastating rise in global temperatures will require rapid decarbonisation of energy supplies worldwide [1]. The energy sector (electricity and heat generation) accounted for 35% of global carbon emissions in 2021, despite reaching a global installed capacity of 837 GW of wind generation and 885 GW of solar photo-voltaic (PV) generation [2–4]. Electricity demand is also predicted to increase in the coming decades as transport and manufacturing processes are electrified in an effort to reduce the emissions of those sectors [5, 6]. Power systems across the world must therefore facilitate further integration of renewable energy generation and energy storage whilst also meeting increased demand. The IEA predicts that renewable annual net capacity additions will reach 450 GW/year by 2027 under their 'Main Case' scenario, or over 600 GW/year under the 'Accelerated Case' scenario (Fig. 1.1). In the UK itself, the government commitments to achieve net-zero carbon emissions by 2050 mean that a further estimated 320 TWh of low-carbon generation will be added to the network in the next 10 years, of which the majority will be wind or solar PV capacity [7].

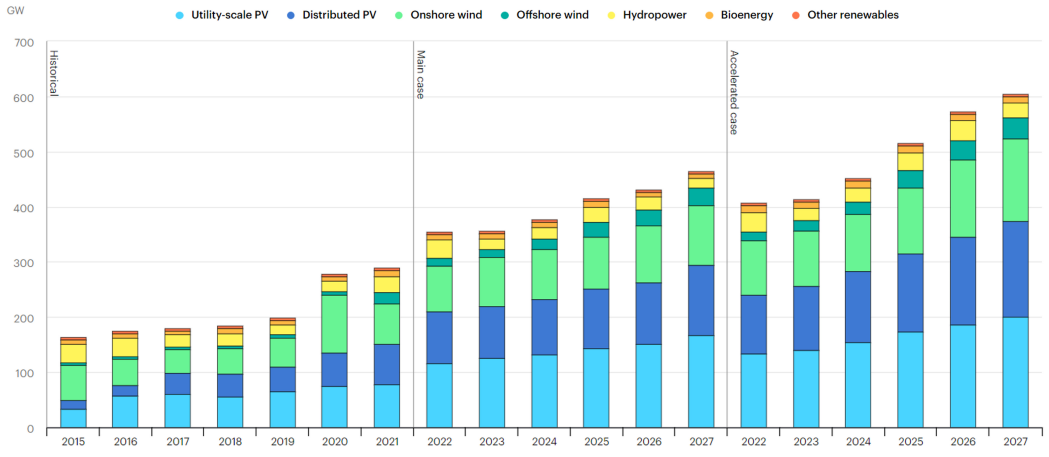

Fig. 1.1: IEA renewable annual net capacity additions by technology, main and accelerated cases, 2015-2027 [8]

This increased penetration of high-impedance, low-inertia generation (such as wind and solar PV) combined with an inevitable decrease in synchronous generation (i.e. coal and CCGT plants) means that the electricity grid has become much weaker over recent years and is set to become much more so. An AC grid is defined as weak when the short circuit ratio (SCR) < 3, and very weak when SCR < 2 [9]. A weak AC grid has significant implications for the implementation and control of the power electronic converters that interface the AC grid to both renewable plants and high-voltage, direct-current (HVDC) transmission links. These evolutions in the nature of power generation are vital if the world is to meet its net-zero commitments and limit global heating. However, a cycle of destabilisation is possible as the penetration of power converters increases, in turn causing a weakening of the AC grid, and in turn threatening the safe operation of existing and future power converters. Power system infrastructure must therefore evolve simultaneously to mitigate this threat to energy stability and reliability.

1.1.2 HVDC Transmission

HVDC transmission is the most efficient method for transmitting power across large distances. Substation and other infrastructure for HVDC has a higher capital installa-

tion cost than the equivalent high-voltage, alternating-current (HVAC) equipment, but significantly lower losses. This makes HVDC the preferred choice for transmission over long distances, particularly for transmission via subsea cables. This trade-off is shown in Fig. 1.2.

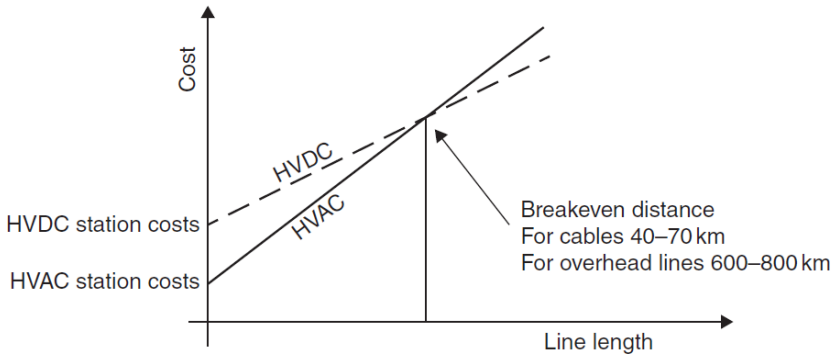

Fig. 1.2: Cost comparison of HVDC and HVAC [10]

The recent expansion of renewable and distributed generation has led to an increased requirement for HVDC transmission for two reasons:

- Distances to offshore wind farms are increasing, such that HVDC transmission is more economically viable than HVAC for transmission to shore.
- Renewable resources are often congregated in sparsely populated areas with low electricity demand. Transmission from low-demand, high-supply areas to high-demand regions is now required over long distances and at high power levels.

In the UK, consent has been granted for multiple HVDC links to connect high-resource regions to high-load regions (e.g. Eastern HVDC link and Viking [11,12]) and to import power from offshore wind farms (e.g. Dogger bank interconnector [13]). HVDC links that were installed prior to 1997 employed Line-Commutated Converter (LCC) technology based on thyristor valves. LCC-HVDC systems have demonstrated capability at high transmission voltages and power transfer, and perform well in the event of DC faults. However, LCC-HVDC lacks black-start capability, offers no independent control of active and reactive power, and has a large footprint [14]. Voltage-Source Converter

(VSC)-HVDC systems can overcome these limitations and, perhaps most crucially, have been shown to offer improved performance in weak AC grids [15, 16]. A summary comparison of the main advantages and disadvantages of LCC- and VSC-HVDC is given in Table 1.1.

Table 1.1: Summary comparison of LCC- and VSC-HVDC advantages and disadvantages

	LCC-HVDC	VSC-HVDC
Advantages	Low switching losses	Independent control of active and reactive power
	Naturally fails in short-circuit	Power flow reversal without DC voltage reversal
	Excellent overcurrent capability	Higher switching frequency gives reduced harmonics
	Lower costs than VSC-HVDC	Black-start capability
	Good DC fault response	Good AC fault response
	Established and mature technology	Can connect to passive AC systems
	Low on-state voltage drop	Operation as as STATCOM at zero active power
Disadvantages	Low order harmonics require large filters	Higher cost than LCC due to large number of switches
	No independent active and reactive power control	Higher switching losses and conduction losses
	Slow response time	Naturally fails in open circuit
	Power reversal requires DC-voltage reversal	High dv/dt transients present at connecting points
	Vulnerable to commutation failures	Lower power capability than LCC
	Requires large reactive power compensation	Uncontrolled diode bridge behaviour in DC fault

As wind farms move further offshore and transmission distances between renewable generation and load regions increases, more and more HVDC transmission links will be required to provide efficient, high power transfer over these long distances. The evolution of the power system discussed in Section 1.1.1 means that these transmission links will most likely use VSC technology at converter stations to interface with the

increasingly weak AC grid and to provide ancillary services in place of synchronous generation.

1.2 Research Motivation

Weakening AC grids and an increased demand for HVDC transmission mean that VSC-HVDC is likely to play a significant role in future power systems. However, the robustness of VSC-HVDC in a weak AC grid is dependent on robust converter control. Vector current control (VCC) is the established, standard control method for VSC-HVDC in strong grids due to the decoupled active and reactive power control and inherent current limiting capability. However, standard VCC becomes increasingly susceptible to low-frequency resonances and instability as the grid becomes very weak [9, 17, 18]. Proposals to increase the stability boundary of VCC have included tuning modifications, additional control loops, virtual impedances and gain scheduling. Novel strategies of grid-forming control (based on the inherent synchronisation of synchronous machines) are also gaining in popularity for operation in very weak or islanded AC grids [18–20]. Comparing the control interactions, operational boundaries and dynamic performance of all of these control methods in very weak AC grids remains an open research question, attracting significant research attention e.g. [18, 21–35]. If global targets for renewable energy generation and carbon emission reduction are to be met, the stability and control of weak grid-connected VSC-HVDC must be improved further. This will require an examination of the limitations of existing control methods and an objective comparison of current strategies. Studies into the interactions of multiple VSC-HVDC systems in close electrical proximity will also be required to enable the necessary expansion of HVDC transmission in a power system increasingly dominated by power converters. With this goal in mind, this work seeks to explore the performance of various control methods for VSC-HVDC in very weak AC grids under a wide range of controller operating conditions.

1.3 Aims and Objectives

The overall research question that this work seeks to address is:

'How can we accurately compare the performance boundaries of VSC-HVDC control methods in very weak AC grids, and how is this affected by the introduction of multiple VSC-HVDCs in close electrical proximity?'

To consider the multiple aspects of this question, the following aims and objectives were proposed for this work:

- To model vector current-controlled VSC-HVDC in a very weak AC grid and assess the full controller performance limits.
- To model a grid-forming VSC-HVDC control strategy in a very weak AC grid and assess the full limits of the controller performance.
- To develop an assessment method for existing and proposed VSC-HVDC controllers such that objective comparison of various control strategies in very weak AC grids can be performed.
- To investigate the controller interactions, power limits and resonances present for vector current-controlled VSC-HVDC in dual-infeed HVDC systems in weak AC grids.

1.4 Publications

This project has resulted in the following publications to date:

I. J. F. Morris, K. H. Ahmed and A. Egea-Àlvarez, "Analysis of Controller Bandwidth Interactions for Vector-Controlled VSC Connected to Very Weak AC Grids," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 7343-7354, Dec. 2021.

II. J. F. Morris, K. H. Ahmed and A. Egea-Àlvarez, "Power-Synchronization Control for Ultra-Weak AC Networks: Comprehensive Stability and Dynamic Performance Assessments", *IEEE Open Journal of the Industrial Electronics Society*, Aug. 2021.

III. J. F. Morris, K. H. Ahmed and A. Egea-Àlvarez, "Standardized Assessment Framework for Design and Operation of Weak AC Grid-Connected VSC Controllers", *IEEE Access*, July 2021.

IV. S. Coffey, J. F. Morris and A. Egea-Àlvarez, "Stability Limits and Tuning Recommendations For Standard Vector Current Control Providing Inertia Support", *2021 IEEE Madrid PowerTech*, Madrid, Spain, June 2021.

1.5 Thesis Structure

The rest of this thesis is structured as follows:

Chapter 2 presents a review of the existing literature on the control of VSC-HVDC in weak AC grids. Section 2.1 covers single-infeed VSC-HVDC systems and Section 2.2 reviews research into dual- and multi-infeed VSC-HVDC systems connected in close electrical proximity.

Chapter 3 contains derivations and validation of the small-signal analytical models of VSC-HVDC systems and control strategies that will be studied in this work. Linearized models of vector current control (VCC), power synchronisation control (PSC) and a simple virtual synchronous machine (VSM) control method are derived, as well as the linearised simplified AC grid.

Chapter 4 presents an analysis of the controller bandwidth interactions present in vector current controlled VSC-HVDC in very weak AC grids, and establishes a stable operating region in terms of controller tunings. Dynamic performance and robustness to changes in SCR are considered and results are validated with control hardware-in-the-loop (CHiL) experiments.

Chapter 5 presents a comprehensive assessment of power synchronisation control for VSC-HVDC in very weak AC grids. The controller dynamics are assessed, a stable operating region is established and CHiL experiments are performed to validate this stability boundary and the transient performance within the stable operating space.

Chapter 6 develops a novel standardized assessment framework for analysis and comparison of any VSC-HVDC control method. The framework provides tuning, time-domain and frequency-domain tests that are applicable to any form of VSC-HVDC controller and can be performed with analytical or time-domain models or full hardware implementations. Three types of VSC-HVDC controller (VCC, PSC and VSM control) are compared to demonstrate the versatility and robustness of the proposed framework for controllers with very different structures.

Chapter 7 investigates the effect of adding a second VSC-HVDC infeed in close electrical proximity to an existing weak grid-connected VSC-HVDC. Analytical models, time-domain simulation and CHiL experiments are used to determine maximum active power transfer limits, control interactions, tuning implications and the effect of high-frequency resonances in the dual-infeed system.

Chapter 8 provides general conclusions, a summary of the author contributions of this work and recommendations for future studies based on the findings in this thesis.

Chapter 2

Literature Review

This chapter presents an overview of the current literature relating to single-infeed and multi-infeed VSC-HVDC. Limitations of vector-controlled VSC-HVDC in very low SCR AC grids are discussed and potential improvements are suggested in various works. Other authors present entirely novel control strategies for weak AC grid operation. Within the multi-infeed VSC-HVDC literature, the quantification of multi-infeed systems is discussed as well as interactions between converter stations and the resulting impacts on controller performance.

2.1 Single-infeed VSC stability and control

The two most significant challenges yet to be resolved for very weak grid-connected VSCs are 1) to maximise bidirectional active power transfer; 2) to be sufficiently robust (stable) under parameter uncertainty or changes in SCR. Many efforts have been made to improve very weak grid-connected VSC performance in these respects. However, evaluation of such control strategies has not been standardized in academic literature. The main causes of instability for VSCs in very weak AC grids are classified into two main factors in the literature. The first key factor is the controller synchronization method. For standard VCC, the converter-controller system is synchronized to the grid via the phase-locked loop (PLL), whose effect on stability is highlighted in [23–29].

At high PLL bandwidth, fast changes in the controller phase angle cause rapid changes in current injections, which in turn perturb the AC busbar voltage such that the PLL cannot lock on to the correct phase angle [21]. The second factor that contributes to instability is the other controller elements, as investigated in [22, 24, 27–29]. All aspects of the controller structure are critical for overall stability of very weak grid-connected VSCs. However, in all literature works, analysis is focused on only one aspect of the controller at a time, such that potential interactions between these components are overlooked. This single-variable analysis is often based on the assumption that the inner and outer control loops are decoupled by their different time scales and thus can be considered separately [24]. However, stability analysis which varies the parameters of the cascaded control loops simultaneously is not performed to verify this assumption.

To mitigate the destabilizing effects of the PLL, control methods have been proposed to enhance or modify conventional vector current control. In [22] and [30], an artificial bus has been used to add impedance compensation to the PLL while [25] and [27] focus on re-tuning the PLL. This invariably requires slowing down the PLL, which leads to a slower controller response and poor transient performance [21, 22, 31]. Other control strategies attempt to remove the PLL completely. Direct power control (DPC) improves dynamic performance compared to conventional VCC with a very slow PLL, however there is limited work on very weak grid performance at this stage [32]. A frequency-synchronization control (FSC) method removes the PLL and appears to show improved stability in weak AC grids, but there is no inherent current-limiting capability [33]. A noteworthy strategy proposed to eradicate the issue of PLL dynamics in weak AC grid-connected VSCs is power synchronization control (PSC). PSC eliminates the PLL entirely and instead emulates the synchronization behaviours of synchronous machines [18, 36]. Proponents of PSC claim that the maximum active power transfer in weak AC grids can be much higher than with standard VSC and the system damping is improved with this approach [22]. Case studies employing back-to-back VSCs between two weak AC grids and for the connection of wind farms to a weak grid using PSC have also shown good stability performance at high active power transfer and adequate fault-ride-through behaviour [37, 38]. Transient performance is explored further in [39]

to demonstrate that PSC can re-synchronize with the grid within approximately one period of oscillation after a fault. Recently, a feedforward enhancement of PSC has also been proposed to address the poor performance of PSC in strong AC grids [40]. However, a full assessment of the effect of tuning variations on steady-state and dynamic performance of PSC in weak AC grids has not yet been completed in the literature. In [41], a robust tuning method for the active power loop was proposed for a simplified model of PSC but the AC voltage control and high-pass filter tunings are neglected. Similarly, although [42] and [43] have examined the effect of the power synchronization and AC voltage control bandwidths on system damping pole and placement respectively, neither study examined the detailed interactions of these controller elements nor used wide enough ranges of tunings to explore the full parameter space. It was also assumed that the precise grid conditions were known and constant. In all of these works, performance is evaluated at only a single controller tuning point, which is determined by a trial and error tuning processes [36] or using a simplified model to analytically tune just one control loop [41]. All of these methods propose to address the limitation of the PLL claim to offer improved power transfer and stability compared to conventional VCC. However, the nature of the assessment performed to reach this conclusion varies widely within the literature. No comprehensive evaluation is performed to determine if the optimum controller tuning has indeed been achieved or whether improved transient or power transfer performance can be achieved at an alternative operating point. By definition, these proposed controllers are also developed under the assumption that the PLL is the most significant cause of instability, which overlooks the contribution of other control loops.

The limitations imposed by the outer loops are the second major contributor to instability in weak grid-connected VSCs. One suggested improvement is to add feedforward terms to the reactive power control in order to speed up this outer loop [27, 30, 44]. To improve the system damping, [28] introduces current-error based compensators to the VSC voltage reference, while gain-scheduling and cross-coupling terms in the outer loop were proposed in [34] to decouple the d- and q-axis control. Each of these strategies performs better than conventional VCC but, as with the PLL-focused

controllers, these works do not consider multiple controller operating points. This limited analysis does not accurately evaluate the complete stability boundary of any given strategy and prevents the fair comparison of the various enhanced VCC methods. Each of the modified VCC control strategies targets the PLL- or controller-induced instability with precise controller tuning that assumes accurate system quantification and, in some cases, requires gain scheduling based on the grid impedance and real-time power transfer (e.g. [34]). Impedance estimation methods are either intrusive or slow and cannot be implemented in all weak grid systems. Sensitivity analysis is therefore important in weak AC grids and sensitivity of individual controller tunings was examined in several works e.g. [21, 24, 29]. The sensitivity of the active and reactive power loops was studied in [24], but this work ignores the inner current loop, assuming that the different time-scales of the cascaded loops prevent any interaction. Conversely, [29], considered only current time-scale stability effects and demonstrated the positive damping effect of the current controller on terminal voltage as the current control bandwidth increases. These studies do not consider the sensitivity of more than two variables simultaneously i.e. at best, the tuning of two control loops is examined at a fixed power level or one control loop tuning is examined at varying power level. The coupled impact of more than one control loop on the maximum power transfer is not assessed. In addition, the controller bandwidth ranges covered are often small (less than one order of magnitude) and so the full extent of each effect may not be covered.

In summary, the current literature presents a variety of approaches to the problem of VSC control in very weak AC grids, stemming from an array of different beliefs as to the core mechanisms causing instability. However, the field lacks any linearise approach for evaluating novel control strategies across a wide range of operating points. As such, it is impossible to determine the true value of any alleged advances in weak grid control with respect to the current industry standard. There may also be destabilizing influences requiring further research that remain hidden by this narrow evaluation approach. There is therefore a need, not only for an ideal weak grid-connected VSC control strategy, but also for a linearise, comprehensive assessment framework that both controller developers and industry operators can use to select, tune and evaluate

VSC controllers for the demanding conditions of weak AC systems.

2.2 Multi-infeed HVDC stability and control

The prevalence of HVDC transmission in power systems is increasing, driven primarily by the need to connect renewable energy generation to the grid from remote locations and the desire to trade in international energy markets for improved grid balancing. This trend inevitably leads to a requirement to place multiple converters in close electrical proximity to each other, creating multi-infeed HVDC systems (MI-HVDC) [45]. Although single-infeed HVDC is now an established technology, questions remain around the effects of MI-HVDC on power transfer capability and system interactions and stability, particularly if the AC grid is weak at the point of connection. Interaction phenomena in MI-HVDC systems take a number of forms, but the four most basic and significant are transient overvoltage effects (TOV), harmonic performance, control performance and commutation failure behaviour [46]. TOV and commutation failure are most significant for LCCs (though voltage transients are still an important consideration for VSCs). However, this study will first focus on VSC-only MI-HVDC and so will ignore these effects for now. The primary interaction phenomenon to be studied is the control performance, including voltage and power stability. Due to the relative novelty of the field of MI-HVDC, a significant amount of research attention is still focused on proposing new indices, factors or ratios to quantify the system. These can broadly be split into three categories: interaction factors, stability factors, and modified SCRs. The categorisation of some common indices for MI-HVDC system quantification is shown in Fig. 2.1.

Interaction factors aim to quantify how a change in one system variable (usually voltage or power) at one converter bus interacts with that system variable at a neighbouring bus. The original example of these, still widely used, is the Multi Infeed Interaction Factor (MIIF) proposed by CIGRE in [46]. When a voltage change, ΔV_n, is applied to bus n, the change in voltage at bus e, ΔV_e, is measured, and an interaction ratio is calculated. Converter buses that infinitely far apart electrically have a MIIF of 0, whilst the same converter bus will have a MIIF of 1. This is a useful indication

of voltage interaction within a MI-HVDC system, but it has a number of drawbacks. Firstly, the MIIF is usually calculated by simulation, which may be time-consuming and yet inexhaustive. Some analytical methods for calculating the MIIF have been proposed (e.g. [47, 48]) but this relies on accurate impedance modelling of all converter buses, which may not be easily calculable. The nodal voltage interaction factor (NVIF) can be derived from the Jacobian power flow matrix and is therefore another analytical equivalent to the empirical MIIF [49]. Corresponding interaction factors for the power and current can also be derived (NVPF and NCIF, respectively). However, whether empirically or analytically calculated, an inherent shortcoming of the MIIF (or NVIF) is that it was designed for analysis of LCC-HVDC systems. Although some studies have extended its use to hybrid MI-HVDC (e.g. [50]), the MIIF cannot be used for any VSC station employing constant AC voltage control (which is likely to be the favoured control mode in weak AC grids). A modified index, the Multi-infeed Voltage Interaction Factor (MVIF) is proposed in [51] to address this limitation by considering the ratio of the magnitudes of the voltage vector changes. Thus, the MVIF can be non-zero even in constant AC voltage control mode because of the change in voltage angle. These interaction factors all offer a measure of the voltage or power coupling between converter buses in close proximity when the whole system is operating within the stability boundary.

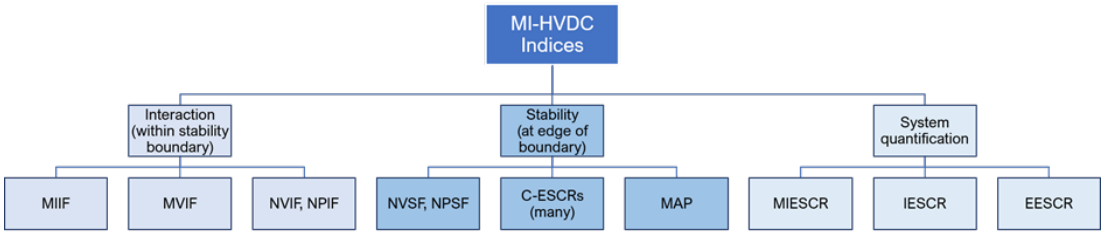

Fig. 2.1: Categorisation of indices for quantification of MI-HVDC systems.

The second category of system indices containis stability factors, which aim to locate the stability boundary itself. The simplest of these are the nodal voltage sensitivity factor (NVSF) and the nodal power sensitivity factor (NPSF) proposed in [52]

and [53]. The NVSF is the voltage change at a node caused by a change in reactive power injection. Stable operation is represented by a small, positive value of the NVSF; an increasing NVSF corresponds to a reducing stability margin, transition to instability occurs when NVSF becomes infinite and a negative value of NVSF occurs in the unstable region. Like the NVIF, the NVSF can also be derived from the Jacobian matrix. However, as a metric dependent on voltage magnitude changes, it is again inappropriate for VSCs in constant voltage control mode. Equivalent power and current sensitivity factors are derived and discussed in [49]. These sensitivity factors are useful for directly determining the stability boundary in multi-infeed LCC-HVDC, but they are not applicable to all forms of VSC control. This limits their use in hybrid or VSC-only MI-HVDC. Two other useful indices for examining the stability boundary are multi-infeed versions of the Critical Effective Short Circuit Ratio (CESCR) and the Maximum Available Power (MAP). These metrics are linked, since the CESCR is the minimum ESCR at which the system can achieve MAP. Increasing the power or decreasing the ESCR beyond this point will push the system unstable. For each of the modified ESCR metrics discussed in the next section, a corresponding CESCR and MAP can be defined which identifies the stability boundary.

The final group of system indices is modified SCRs, which aim to measure the effective strength of the combined AC grid and MI-HVDC system. Proposals for a multi-dimensional version of the ESCR to quantify MI-HVDC systems are numerous in the literature. These include the Multi-Infeed Effective Short-Circuit Ratio (MIESCR) [46], an Impedance-based Effective Short Circuit Ratio (IESCR) [54], an Equivalent Effective Short-Circuit Ratio (EESCR) [55] and a Generalized Effective Short Circuit Ratio (GESCR) [56]. Of these, the EESCR proposed in [55] is the simplest metric, since it is based on a single-infeed representation of a MI-HVDC system; it can therefore be calculated in the same way as the ESCR for a single-infeed system once the model has been collapsed into this form. The familiarity and simplicity of this method has obvious advantages, and the stability boundary can be found by extending this to calculate the critical EESCR. However, reduction of the model to this extent has a number of limitations given the assumptions and simplifications required. The GESCR

in [56] is also based on a single-infeed equivalent model of the MI-HVDC system (here called a 'coupled single-port model'), but also takes into account a 'reactive power-voltage dependence compensation factor' in order to represent the impact of various DC control characteristics. Again, this method has the benefit of simplicity, but the reduced model can only be used for overall system quantification, not any local analysis at each converter bus. The IESCR proposed in [54] is modelled in a different way to the EESCR or GESCR (small-signal modelling of the entire network rather than reduction to single-infeed) but has the same objective, namely to take into account the impedance of all other converters in the system. An equivalent impedance is calculated for the whole network, as seen from the converter bus under consideration. This arguably achieves the same result as reducing the system to a single-infeed model, though the primary model is small-signal rather than steady-state power flow equations in this case. Whichever modelling approach is used, the requirement to take into account the impedance of other converters on the network is clearly significant. The MIESCR provides a different way of approaching the system quantification. MIESCR is a well-established index presented by CIGRE as a generalisation of the ESCR for multi-infeed systems. This is a very useful indicator of system strength and has direct parallels to well-understood, single-infeed indices. However, calculation of the MIESCR is reliant on the MIIF, which, as discussed, is computationally expensive and primarily designed for LCC-HVDC only. A final index is the Apparent Increase in Short Circuit Ratio (AISCR) presented in [57]. This is calculated empirically from EMT simulation and represents the increase in SCR that must be applied to a single-infeed LCC-HVDC system in order to match the performance of an LCC in a dual-infeed system with a VSC (i.e. the VSC has improved the voltage stability of the LCC, equivalent to increasing the SCR by a certain amount). This assumes that addition of a converter station and infeed will improve the system stability, which may not be the case for VSC-based MI-HVDC. It also does not encapsulate the final state of the system, only the change imposed by the transition from single- to multi-infeed.

The methods of modelling MI-HVDC systems include a range of small- and large-signal techniques, and can include the full complexity of the system of can be reduced

to simpler representations. As discussed above, both [55] and [56] propose equivalent single-infeed models, which allows for system quantification with well-established metrics used for single-infeed HVDC systems (e.g. ESCR, CESCR/MAP). This has obvious advantages for simplicity and the ability to apply tried and tested techniques. However, the behaviour at individual converter buses is hidden by this method and interaction studies cannot be applied to reduced models. Single-infeed models appear to be most useful for generating a multi-infeed equivalent ESCR or CESCR for a 'first-pass' system analysis. Another common approach is the use of the Jacobian power flow matrix e.g. in [49, 51–53, 58]. This method is particularly useful for examining nodal interaction and sensitivity factors, since these can be derived directly from the matrix elements [49]. Using the Jacobian matrix in this way produces analytical expressions which can also indicate which system or control parameters have the most significant impact on a given metric or index. However, for MI-HVDC with more than two links, the Jacobian is large and complex; even for a dual-infeed system, a reduced or simplified Jacobian is often used for efficiency. This trade-off may reduce accuracy. As for single-infeed investigations, small-signal analysis is a popular approach for MI-HVDC, including in [54, 59–61]. Construction of the small-signal model is either performed by linearisation of a MATLAB/Simulink time-domain model [59] or by direct linearisation of the governing grid-connected converter equations, including the converter control [54, 60]. This method is time-consuming during the derivation stage but allows for much faster analysis once modelling is completed and can retain all the detail of the converter-controllers. Eigenvalue stability analysis, modal participation factors and system damping can be easily extracted from the resultant small-signal model, giving significant stability insights at all converter stations. The small-signal models in [62, 63] are also used to create an impedance-based MIMO model of the coupling between HVDC infeeds, which allows the whole system to be analysed with familiar Nyquist, bode plot and eigenvalue techniques. Finally, some studies rely almost entirely on simulation (usually PSCAD/EMT) for modelling of the MI-HVDC system [57,64,65]. This is the most detailed approach but is slow and computationally expensive.

The literature discussed so far has focused on the tools developed to analyse MI-

HVDC systems. Having an effective toolkit of interaction and stability factors and modelling approaches is undoubtedly essential for MI-HVDC analysis, but there has been an over-emphasis so far in the literature on developing and validating these measures rather than employing them for comparative stability studies. Nevertheless, some studies have directly investigated MI-HVDC stability under varying operating conditions. The impact of wind speed and SCR changes for a hybrid, dual-infeed HVDC system between two wind farms and two AC grids is studied in [66]. Most interestingly, the authors vary the SCRs of the two AC grid systems simultaneously and measure the feasible power injection into each grid. The wind speeds at each farm are also varied simultaneously. However, no control parameters are varied and the results are derived from Newton-Raphson evaluation of the steady-state power-flow equations. This is very computationally slow and does not take into account transient performance or small-signal behaviour. Similar variation of the SCR is performed in [63] to demonstrate the presence of low-damped resonances in a VSC-only MI-HVDC system. Line length is also considered, and it is shown that the consideration of high-frequency network modes and harmonic response from the VSC is necessary. This work identifies interaction modes influenced by the converter control but does not offer any insight into the impact of controller tuning on these modes, nor the implications for maximum power transfer or dynamic performance. Other works examine the effect of the outer loop control strategies at the converter buses. For example, [51] examines a hybrid, tri-infeed HVDC system. System and control parameters are varied (AC grid impedance, the LCC extinction angle and the VSC reactive power transfer) and then the control strategies of both the LCC (power control vs current control) and the VSC (reactive power control vs AC voltage control) are compared for the effect on voltage interaction. An interaction factor is used as the sole evaluation metric in this study (namely the MVIF – the primary goal of this study was to develop and validate this factor) and so no information is gathered about the precise location of the stability boundary. There is also no consideration of the effect of simultaneous changes to any of these parameters. Similarly, a hybrid MI-HVDC system is used in [64] to compare performance under traditional VSC control and a power control method. In this study,

stability is verified directly by simulation rather than using eigenvalue analysis or any of the derived metrics discussed above. This therefore limits any insight into where the stability boundary precisely lies or the comprehensive limitations of each control approach. Another novel control approach is developed and compared in [67], which uses the Reduced North Scotland grid as an illustrative model. This study suggests that, in the general case, increasing the AC voltage bandwidth pushes system eigenvalues towards the right-hand plane (RHP) and increases the terminal voltage during a major disturbance. A similar effect is seen when decreasing the SCR of the AC grid. However, the authors do not investigate whether this interaction phenomenon can be improved by re-tuning of any of the control loops at either station, but instead move straight to changing the controller structure. This modified controller is applied to all the converter buses, which are also tuned with the same gains. There is no investigation as to how the system might behave if different tunings are applied at the different converter stations in either the AC voltage control or other control loops. In [59], a dual-infeed VSC-HVDC system is used to examine the effect of four different outer loop control strategies; reactive power control, AC voltage control, AC voltage droop control and remote bus voltage control. Within this study, the AC system SCR is also varied via the AC line length. The small-signal analysis used in [59] provides insight into the damping, and therefore the stability margins, of the respective strategies and grid conditions, but the controller parameters are fixed throughout the study and the exact stability boundaries or system limitations under each control strategy are not fully quantified. Some modification of controller tunings in a dual-infeed, hybrid HVDC system is performed in [54]. However, only the PLL gains of the VSC and the extinction angle control gain of the LCC are varied (and not simultaneously). In addition, the main goal of [54] was to present and validate a new version of the ESCR and so this is the only metric used to assess the impact of controller gain variation. Neither the stability boundary nor the interactions between converter buses are quantified, nor are the effects of other controller parameters. The PLL tuning is also examined in sensitivity studies in [68, 69], which provide the most in-depth examination of controller tunings within MI-HVDC. In [69], it is shown that decreasing the proportional gain of the PLL

at either converter station in a hybrid, dual-infeed HVDC system (one LCC, one VSC), increases the stability. Decreasing the VSC AC voltage control proportional gain or increasing the VSC active power control proportional gain also increases stability. This feasible region of PLL proportional gains at both the LCC and VSC stations and the VSC AC voltage proportional gains is presented as a surface in [68]. The impact of outer loop control bandwidths for the same hybrid, dual-infeed HVDC system is examined again in [70]. However, the main goal of this study is to validate a novel SISO model for the MI-HVDC system and so only limited Nyquist plot analysis is used to examine these effects. There is also no simultaneous variation of the controller tunings, and the system SCRs are fixed during the tuning sensitivity study. None of the studies in [54, 68–70] consider the impact of control parameters on dynamic performance, nor the behaviour of VSC-only MI-HVDC. There is also a focus on identifying the modes and participation factors of various system interactions, rather than the quantitative impact on maximum power transfer, dynamic performance and robustness.

2.3 Summary

As discussed in Chapter 1, the resilience of power systems as converter penetration increases will depend on robust converter control. This chapter has reviewed state of the art control methods for improving the stability and performance of VSC-HVDC in weak AC grids. Adaptions to conventional vector current control and entirely new grid-forming approaches have been discussed. Although many possible solutions have been proposed, objective and comprehensive comparison is lacking in the existing literature and the operating region for performance analysis is often very limited. For multi-infeed VSC-HVDC systems, approaches to better quantify MI-HVDC systems have been collated and reviewed. The literature discusses some of the tuning implications for MI-HVDC in weak AC grids, but with very limited comparison to single-infeed systems and with limited analysis of the effects of each part of the controller. Most research for MI-HVDC focuses on hybrid systems (i.e., with one LCC-HVDC link and one VSC-HVDC link) with limited analysis of entirely VSC-based MI-HVDC systems.

Chapter 3

VSC-HVDC Modelling

Small-signal modelling is an established technique for analysis of non-linear systems at a given operating point. Full state-space small-signal models are derived in this chapter for vector current control, power synchronization control and a simple virtual synchronous machine controller. Some common alternative analytical modelling techniques such as impedance modelling and the Jacobian transfer matrix method are also discussed. The state-space models form the basis for stability and performance analyses in Chapters 4 to 7.

3.1 Vector Current Control

The schematic diagram of the grid-connected VSC system under investigation is presented in 3.1. Positive power indicates that the converter is in rectifying mode; negative power implies inverting mode. U_g is the grid voltage, U_f is the voltage at the point of common coupling (PCC) and U_c is the converter voltage. The AC grid is represented by a Thevenin equivalent impedance $Z_g = R_g + \omega_g L_g$, where ω_g is the grid frequency and R_g and L_g are the Thevenin-equivalent grid resistance and inductance. The VSC is connected via a coupling impedance $Z_c = R_c + \omega_g L_c$ where R_c and L_c are the resistance and inductance of the inductive filter between the converter and the grid. The control system for standard VCC-VSC is shown in Fig. 3.1 including an inner current loop (ICL), outer active power loop (APL), outer AC voltage loop (AVL) and PLL. Control

is performed in the *dq*-frame, which is synchronized to the PCC grid voltage via the reference phase angle produced by the PLL. All inputs to the PLL and controller are measured at the PCC through a first-order low-pass filter.

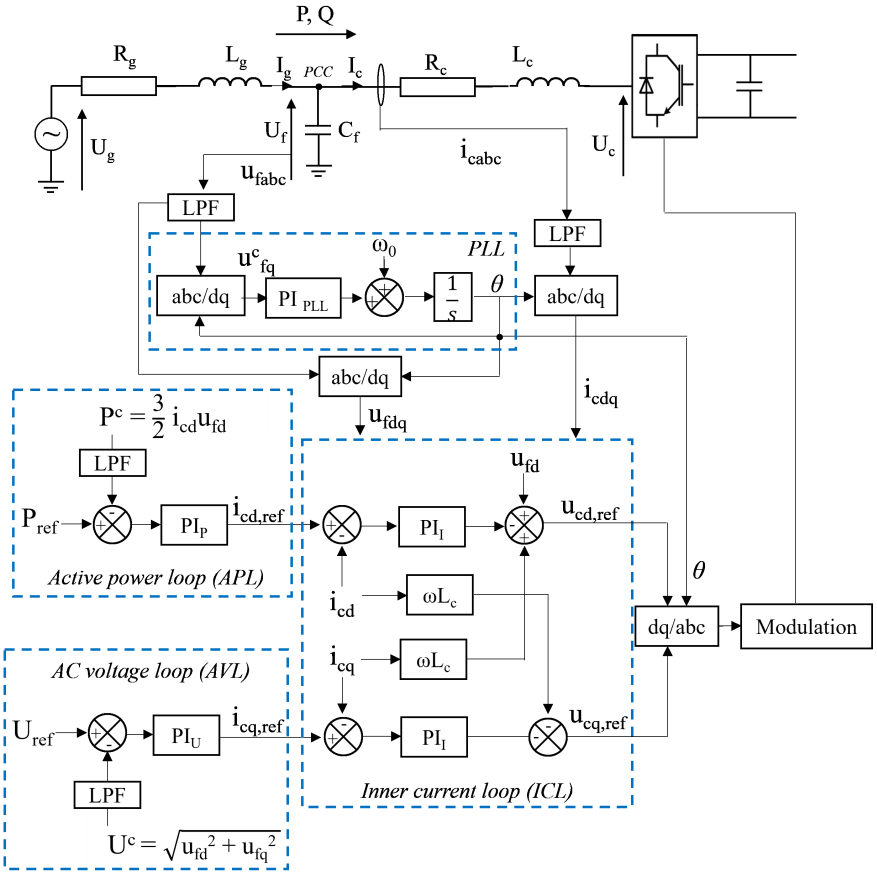

Fig. 3.1: Schematic of single-infeed VSC-HVDC study system with VCC.

3.1.1 State-space small signal model

The state-space representation is a well-established form of small-signal modelling for grid-connected VSCs. The model derived in this section is based on state-space models in [34] and [36]. In this section, the superscript '^{c}' denotes the converter frame and the superscript '^{f} denotes a low-pass filtered variable. The subscript '$_0$' denotes a steady-state linearisation point.

AC grid

The dynamic system equations for the AC grid in Fig. 3.1 are given in full in Appendix A.1. These equations are linearised to give the following state-space representation in (3.1) to (3.8), where the system parameters are as defined in Section 3.1.

$$\Delta \dot{x}_{grid} = A_{grid}\Delta x_{grid} + B_{grid}\Delta u_{grid} \tag{3.1}$$

$$\Delta y_{grid} = C_{grid}\Delta x_{grid} \tag{3.2}$$

$$\Delta x_{grid} = \begin{bmatrix} \Delta i_{cd} & \Delta i_{cq} & \Delta u_{fd} & \Delta u_{fq} & \Delta i_{gd} & \Delta i_{gq} \end{bmatrix} \tag{3.3}$$

$$\Delta u_{grid} = \begin{bmatrix} \Delta v_d & \Delta v_q & \Delta e_d & \Delta e_q \end{bmatrix} \tag{3.4}$$

$$\Delta y_{grid} = \begin{bmatrix} \Delta i_{cd} & \Delta i_{cq} & \Delta u_{fd} & \Delta u_{fq} & \Delta U & \Delta P \end{bmatrix} \tag{3.5}$$

$$A_{grid} = \begin{bmatrix} -\frac{R_c}{L_c} & \omega & \frac{1}{L_c} & 0 & 0 & 0 \\ -\omega & \frac{R_c}{L_c} & 0 & \frac{1}{L_c} & 0 & 0 \\ -\frac{1}{C_f} & 0 & 0 & \omega & \frac{1}{C_f} & 0 \\ 0 & -\frac{1}{C_f} & -\omega & 0 & 0 & \frac{1}{C_f} \\ 0 & 0 & -\frac{1}{L_g} & 0 & -\frac{R_g}{L_g} & \omega \\ 0 & 0 & 0 & -\frac{1}{L_g} & -\omega & -\frac{R_g}{L_g} \end{bmatrix} \tag{3.6}$$

$$B_{grid} = \begin{bmatrix} -\frac{1}{L_c} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_c} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_g} & 0 \\ 0 & 0 & 0 & \frac{1}{L_g} \end{bmatrix} \tag{3.7}$$

$$C_{grid} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & \frac{u_{d0}}{U_0} & \frac{u_{q0}}{U_0} & 0 & 0 \\ 0 & 0 & \frac{3i_{gd0}}{2} & \frac{3i_{gq0}}{2} & \frac{3u_{fd0}}{2} & \frac{3u_{fq0}}{2} \end{bmatrix} \tag{3.8}$$

Inner current loop

The inner control loop uses a proportional-integral (PI) controller to adjust the converter current. Decoupling terms on each axis are used for independent d- and q-axis current control. The ICL control laws are:

$$\Delta u_{cd,ref} = \Delta u_{fd} - F_{CL}(s)\big(\Delta i_{cd,ref} - \Delta i_{cd}\big) + \omega L_c \Delta i_{cq} \tag{3.9}$$

$$\Delta u_{cq,ref} = -F_{CL}(s)\big(\Delta i_{cq,ref} - \Delta i_{cq}\big) - \omega L_c \Delta i_{cd} \tag{3.10}$$

where, $F_{CL}(s) = k_{p-I} + k_{i-I}/s$ and k_{p-I} and k_{i-I} are the ICL proportional and integral gains, respectively. The controller gains are tuned using $k_{p-I} = L_c/\alpha$ and $k_{i-I} = R_c/\alpha$ where α is the current loop time constant, such that $\alpha = 1/\omega_{ICL}$. Inputs to the inner loop are in the converter frame; as such, the ICL state space equations are also used to calculate the power and voltage in the converter frame (ΔP^c and ΔU^c). The state space representation of the inner loop is given in full in (3.11) to (3.17).

$$\Delta \dot{x}_{il} = B_{il} \Delta u_{il} \tag{3.11}$$

$$\Delta y_{il} = C_{il} \Delta x_{il} + D_{il} \Delta u_{il} \tag{3.12}$$

$$\Delta u_{il} = \begin{bmatrix} \Delta i_{cd,ref} & \Delta i_{cq,ref} & \Delta i^c_{cd} & \Delta i^c_{cq} & \Delta u^c_{fd} & \Delta u^c_{fq} \end{bmatrix} \tag{3.13}$$

$$\Delta y_{il} = \begin{bmatrix} \Delta v^c_d & \Delta v^c_q & \Delta P^c & \Delta U^c \end{bmatrix} \tag{3.14}$$

$$B_{il} = \begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.15}$$

$$C_{il} = \begin{bmatrix} -k_{i-I} & 0 & 0 & 0 \\ 0 & -k_{i-I} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{3.16}$$

$$D_{il} = \begin{bmatrix} -k_{p-I} & 0 & k_{p-I} & \omega L_c & 1 & 0 \\ 0 & -k_{p-I} & -\omega L_c & k_{p-I} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{u_{d0}}{U_0} & \frac{u_{q0}}{U_0} \\ 0 & 0 & \frac{3u_{fd0}}{2} & \frac{3u_{fq0}}{2} & \frac{3i_{gd0}}{2} & \frac{3i_{gq0}}{2} \end{bmatrix} \tag{3.17}$$

Outer loops

Current references for the inner loop are calculated based on the active power error (giving the d-axis current reference) and the AC voltage magnitude error (giving the q-axis current reference) as shown in shown in Fig. 3.1. The outer loop control laws are thus:

$$\Delta i^c_{cd,ref} = F_P(s)\big(\Delta P^c_{ref} - \Delta P^{cf}\big) \tag{3.18}$$

$$\Delta i^c_{cq,ref} = F_U(s)\big(\Delta U^c_{ref} - \Delta U^{cf}\big) \tag{3.19}$$

where, ΔP^{cf} is the filtered active power at the PCC, ΔU^{cf} is the filtered AC voltage magnitude at the PCC, $F_P(s) = k_{p-P} + k_{i-P}/s$ (where k_{p-P} and k_{i-P} are the APL proportional and integral gains, respectively) and $F_U(s) = k_{p-U} + k_{i-U}/s$ (where k_{p-U} and k_{i-U} are the AVL proportional and integral gains, respectively). The state-space representation of the APL and AVL are shown in (3.22) to (3.27).

$$\Delta \dot{x}_{ol} = B_{ol} \Delta u_{ol} \tag{3.20}$$

$$\Delta y_{ol} = C_{ol} \Delta x_{ol} + D_{ol} \Delta u_{ol} \tag{3.21}$$

$$\Delta x_{ol} = \begin{bmatrix} \Delta e_p & \Delta e_u \end{bmatrix} \tag{3.22}$$

$$\Delta u_{ol} = \begin{bmatrix} \Delta P^c_{ref} & \Delta U^c_{ref} & \Delta P^{cf} & \Delta U^{cf} \end{bmatrix} \tag{3.23}$$

$$\Delta y_{ol} = \begin{bmatrix} \Delta i_{cd,ref} & \Delta i_{cq,ref} \end{bmatrix} \tag{3.24}$$

$$B_{ol} = \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \tag{3.25}$$

$$C_{ol} = \begin{bmatrix} k_{i-P} & 0 \\ 0 & k_{i-U} \end{bmatrix} \tag{3.26}$$

$$D_{ol} = \begin{bmatrix} k_{p-P} & 0 & -k_{p-P} & 0 \\ 0 & k_{p-U} & 0 & -k_{p-U} \end{bmatrix} \tag{3.27}$$

PLL and Park transforms

Synchronization between the AC grid and the converter-controller is achieved with a reference angle produced by the PLL, as shown in Fig. 3.1. This gives the PLL control law in (3.28).

$$\theta_{PLL} = \left(k_{p-pll} + \frac{k_{i-pll}}{s} \right) u^c_{fq} \tag{3.28}$$

where the q-axis bus voltage in the converter frame, u^c_{fq}, is defined as:

$$u^c_{fq} = Im\{\mathbf{u_f} e^{-j\theta_{PLL}}\} = u_{fq} \cos\theta_{PLL} - u_{fd} \sin\theta_{PLL} \tag{3.29}$$

Taking $F_{PLL}(s) = \left(k_{p-pll} + \frac{k_{i-pll}}{s}\right)$ and substituting into (3.28) gives:

$$\theta_{PLL} = F_{PLL}(s)(u_{fq}\cos\theta_{PLL} - u_{fd}\sin\theta_{PLL}) \tag{3.30}$$

Linearising (3.30) gives:

$$\begin{aligned}\Delta\theta_{PLL} = &\frac{-F_{PLL}(s)\sin\theta_{u0}}{1 + F_{PLL}(s)(u_{fd0}\cos\theta_{u0} + u_{fq0}\sin\theta_{u0})}\Delta u_{fd} \\ &+ \frac{F_{PLL}(s)\cos\theta_{u0}}{1 + F_{PLL}(s)(u_{fd0}\cos\theta_{u0} + u_{fq0}\sin\theta_{u0})}\Delta u_{fq}\end{aligned} \tag{3.31}$$

In this analysis, θ_{u0} is always zero and so only the second term of this expression is preserved. Equation (3.31) therefore becomes:

$$\Delta\theta_{PLL} = \underbrace{\frac{F_{PLL}(s)}{s + u_{fd0}F_{PLL}(s)}}_{G_{PLL}(s)}\Delta u_{fq} \tag{3.32}$$

The PLL gains can be calculated using:

$$\tau_{pll} = \frac{2\zeta}{\omega_{pll}}, \quad k_{p-pll} = \frac{2\zeta\omega_{pll}}{u_{fd0}}, \quad k_{i-pll} = \frac{k_{p-pll}}{\tau_{pll}} \tag{3.33}$$

where, ζ is the PLL damping factor, ω_{pll} is the PLL bandwidth (in rad/s) and τ_{pll} is the PLL time constant (in s/rad) [71].

The Park transformations to convert the PCC voltage, u_f, and converter side current, i_c, from the grid dq frame to the converter dq frame are given by:

$$\mathbf{u_f}^c = \mathbf{u_f}e^{-j\theta_{PLL}} \quad , \quad \mathbf{i_c}^c = \mathbf{i_c}e^{-j\theta_{PLL}} \tag{3.34}$$

Linearising the component form of (3.34) gives:

$$\begin{bmatrix}\Delta u_{fd}^c\\ \Delta u_{fq}^c\end{bmatrix} = \begin{bmatrix}\cos\theta_{u0} & \sin\theta_{u0} & -u_{fd0}\sin\theta_{u0} + u_{fq0}\cos\theta_{u0}\\ -\sin\theta_{u0} & \cos\theta_{u0} & -u_{fd0}\cos\theta_{u0} - u_{fq0}\sin\theta_{u0}\end{bmatrix}\begin{bmatrix}\Delta u_{fd}\\ \Delta u_{fq}\\ \Delta\theta_{PLL}\end{bmatrix}$$
$$\begin{bmatrix}\Delta i_{cd}^c\\ \Delta i_{cq}^c\end{bmatrix} = \begin{bmatrix}\cos\theta_{u0} & \sin\theta_{u0} & -i_{cd0}\sin\theta_{u0} + i_{cq0}\cos\theta_{u0}\\ -\sin\theta_{u0} & \cos\theta_{u0} & -i_{cd0}\cos\theta_{u0} - i_{cq0}\sin\theta_{u0}\end{bmatrix}\begin{bmatrix}\Delta i_{cd}\\ \Delta i_{cq}\\ \Delta\theta_{PLL}\end{bmatrix} \tag{3.35}$$

The inverse transformation, from converter dq frame to grid dq frame, is applied to the VSC converter voltage (3.36) and linearised (3.37).

$$\mathbf{v}^c = \mathbf{v}e^{j\theta_PLL} \tag{3.36}$$

$$\begin{bmatrix}\Delta v_d^c\\ \Delta v_q^c\end{bmatrix} = \begin{bmatrix}\cos\theta_{u0} & -\sin\theta_{u0}(-v_{d0}\sin\theta_{u0} - v_{q0}\cos\theta_{u0})\\ \sin\theta_{u0} & \cos\theta_{u0}(v_{d0}\cos\theta_{u0} - v_{q0}\sin\theta_{u0})\end{bmatrix}\begin{bmatrix}\Delta v_d^c\\ \Delta v_g^c\\ \Delta\theta_{PLL}\end{bmatrix} \tag{3.37}$$

Filters

Low-pass filtering is required in real systems in order to remove noise and switching-frequency harmonics. The filter delay also breaks the algebraic loops present in the time-domain model. These filters must therefore be included in the small-signal model. The simple, first-order filter in (3.38) is applied to the bus voltage, converter side current, active power and AC voltage magnitude in both models.

$$\frac{1}{\tau_f s + 1} \tag{3.38}$$

However, when applying this filter to the bus voltage and converter-side current in the dq frame, cross-coupling effects (which reflect the cross-coupling terms in the inner current loop) must be taken into account. The state space representation of (3.38) including these cross-coupling terms is shown in (3.39) to (3.44).

$$\Delta \dot{x}_{lpf} = A_{lpf}\Delta x_{lpf} + B_{lpf}\Delta u_{lpf} \tag{3.39}$$

$$\Delta y_{lpf} = C_{lpf}\Delta x_{lpf} \tag{3.40}$$

$$\Delta u_{lpf} = \begin{bmatrix} \Delta i_{cd} & \Delta i_{cq} \end{bmatrix} \tag{3.41}$$

$$\Delta y_{lpf} = \begin{bmatrix} \Delta i^{f}_{cd} & \Delta i^{f}_{cq} \end{bmatrix} \tag{3.42}$$

$$A_{lpf} = \begin{bmatrix} -1/\tau_f & \omega \\ -\omega & -1/\tau_f \end{bmatrix} \tag{3.43}$$

$$B_{lpf} = \begin{bmatrix} 1/\tau_f & 0 \\ 0 & 1/\tau_f \end{bmatrix} \tag{3.44}$$

$$C_{lpf} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3.45}$$

Full Linearized Model

Each of the state space models in this section is connected as shown in Fig. 3.2. The inputs to the full system model are the active power and AC voltage references (ΔP^{c}_{ref} and ΔU^{c}_{ref}) and the outputs are power and AC voltage in the converter frame (ΔP^{cf} and ΔU^{cf}).

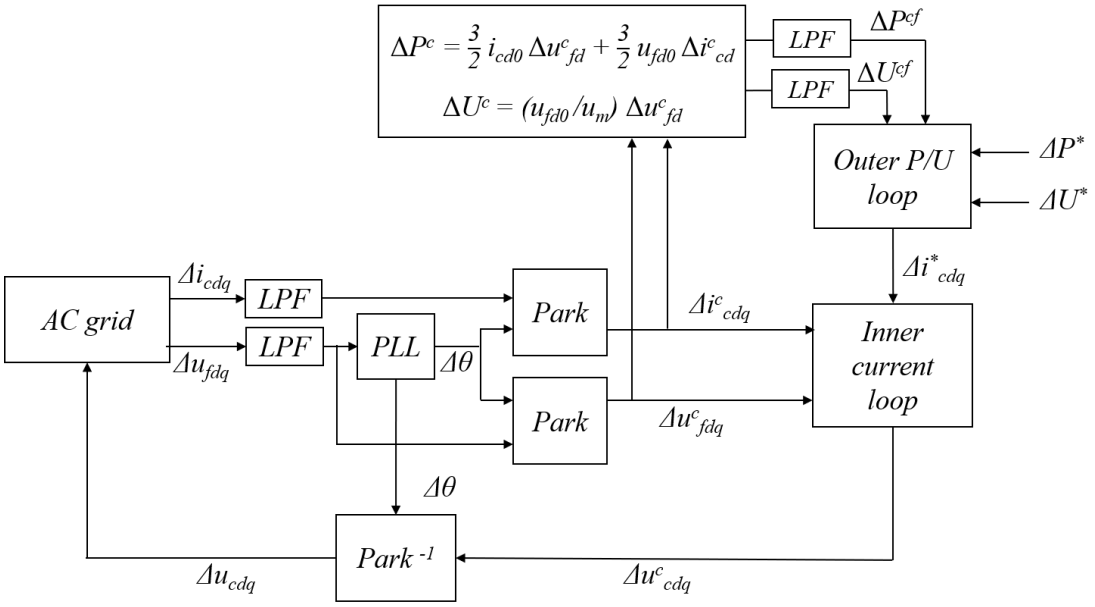

Fig. 3.2: Connected small signal model of the VSC system

Validation

The small signal model is validated by comparison with a non-linear MATLAB/Simulink time-domain simulation of the full system. Fig. 3.3 shows the results of 0.1 p.u. voltage and power steps in the small signal and time domain models. The small signal model shows very good transient agreement with the time-domain model and is therefore valid for small signal stability analysis.

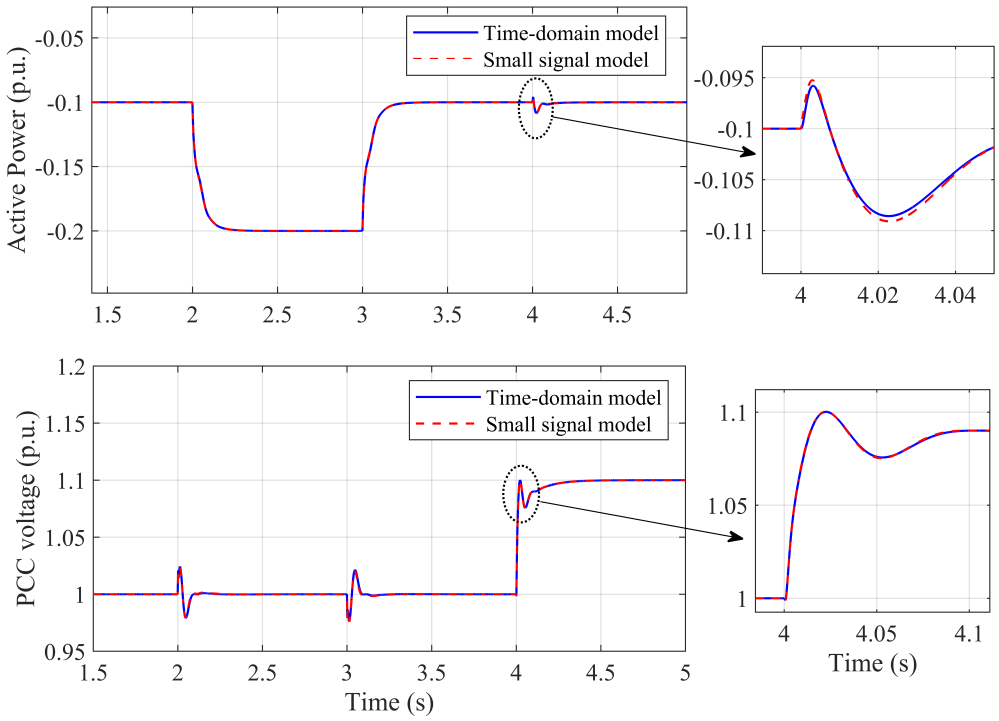

Fig. 3.3: Small signal model validation with active power and PCC voltage response to 0.1 p.u. power and voltage step changes.

3.1.2 Impedance model

Impedance modelling is based on the same linearised system equations as state-space modelling, but these are manipulated such that the VSC can be represented by an equivalent output admittance in parallel with a current source [72, 73]. The main advantage of this alternative representation is that the admittance of a real system can be measured without any knowledge of the actual system parameters. This allows for analysis of grid-connected converter systems as 'black boxes' where the actual system parameters are unknown. The reciprocity between the state-space and impedance models also means that an impedance model can be used to corroborate stability analyses performed with a state-space model. Since the stability methodology that will be presented in Chapter 4 is novel, this secondary analysis is an important, independent validation of the developed method. In this section, an impedance model of a grid-connected VCC-VSC is derived; this model will be used to validate the state-space

small-signal model results in Chapter 4.

The converter-grid system can be represented by the Norton-Thevenin equivalent model in Fig. 3.4 where the VSC converter is represented by a current source with an output admittance $\mathbf{Y}(s)$, while the AC grid is modelled by a voltage source in series with an impedance, $\mathbf{Z_g}(\omega_g, s)$. This leads to equation 3.46 for the converter output current.

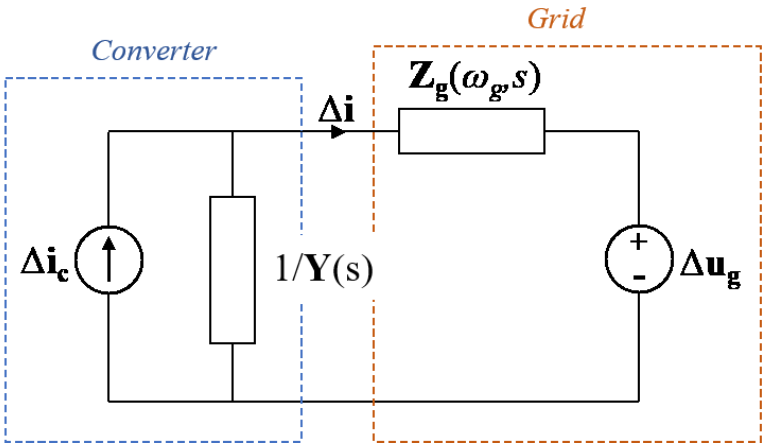

Fig. 3.4

$$\Delta\mathbf{i} = \Big[\Delta\mathbf{i_c} - \mathbf{Y}(s)\Delta\mathbf{u_g}\Big] \cdot \frac{1}{\Big[\mathbf{I} + \mathbf{Y}(s)\mathbf{Z_g}(\omega_g, s)\Big]} \tag{3.46}$$

where,

$$\mathbf{Z_g}(\omega_g, s) = \begin{bmatrix} R_g + sL_g & -\omega_g L_g \\ \omega_g L_g & R_g + sL_g \end{bmatrix} \tag{3.47}$$

As established in [73], the stability of the system can be determined by applying the Nyquist stability criterion to the open-loop gain $\mathbf{Y}(s)\mathbf{Z_g}(\omega_g, s)$ or by examining the poles of the closed loop, $[\mathbf{I} + \mathbf{Y}(s)\mathbf{Z_g}(\omega_g, s)]^{-1}$. For this analysis, the impedance model is deemed to be stable if all closed-loop poles exist in the left-hand plane. The converter admittance is derived in the grid frame and described in equations 3.48 to 3.50 and Fig. 3.5. For simplicity, this impedance model retains only the ΔP, ΔU and Δu_{fd} filters shown in Fig. 3.1. Further details of the impedance model derivation are given in Appendix A.2.

$$\Delta \mathbf{i_c} = \mathbf{Y}(s)\Delta \mathbf{u_f} \tag{3.48}$$

$$\Delta \mathbf{i_c} = \mathbf{G_c}(s)\Delta \mathbf{i_{cref}} + \mathbf{Y_i}(s)\Delta \mathbf{u_f} \tag{3.49}$$

$$\Delta \mathbf{i_c} = \mathbf{G_c}(s)\left[\mathbf{G_0}(s)\Delta \mathbf{u_f}\right] + \mathbf{Y_i}(s)\Delta \mathbf{u_f} \tag{3.50}$$

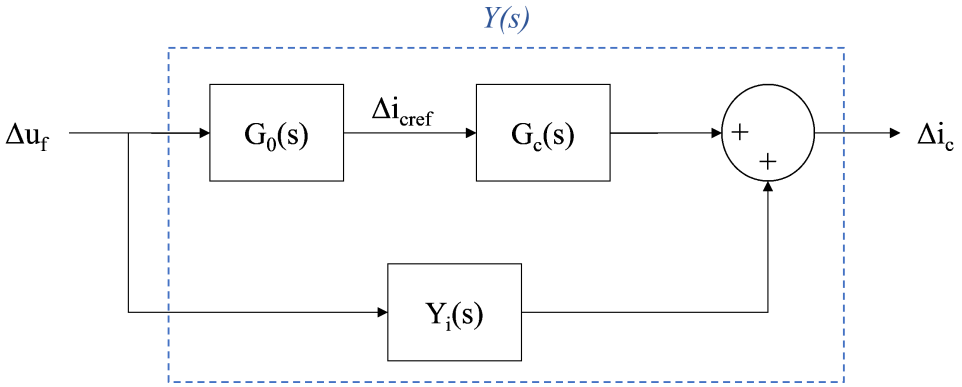

Fig. 3.5

where the components of Fig. 3.5 are given by:

$$\mathbf{G_c}(s) = \begin{bmatrix} \frac{1}{1+s\alpha} & 0 \\ 0 & \frac{1}{1+s\alpha} \end{bmatrix} = \begin{bmatrix} g_c(s) & 0 \\ 0 & g_c(s) \end{bmatrix} \tag{3.51}$$

$$\mathbf{Y_i}(s) = \begin{bmatrix} \frac{1-H_{u\text{-}dd}(s)}{F_{CL}(s)+R_c+sL_c} & \frac{aG_{pll}(s)-H_{u\text{-}qd}(s)}{F_{CL}(s)+R_c+sL_c} \\ 0 & \frac{1+bG_{pll}(s)}{F_{CL}(s)+R_c+sL_c} \end{bmatrix} \tag{3.52}$$

$$\mathbf{G_0}(s) = \begin{bmatrix} -G_{pd}(s) & -G_{pq}(s) \\ -H(s)F_U(s)\frac{u_{fd0}}{u_m} & -H(s)F_U(s)\frac{u_{fq0}}{u_m} \end{bmatrix} \tag{3.53}$$

$$\begin{cases} G_{pd}(s) = \dfrac{1.5H(s)F_P(s)\left(i_{cd0} + u_{fd0}y_{dd}(s)\right)}{1 + 1.5u_{fd0}g_c(s)H(s)F_p(s)} \\ G_{pq}(s) = \dfrac{1.5H(s)F_P(s)\left(i_{cq0} + u_{fd0}y_{qd}(s)\right)}{1 + 1.5u_{fd0}g_c(s)H(s)F_p(s)} \end{cases} \tag{3.54}$$

$$\begin{cases} a = u_{cqo} + \omega L_c i_{cd0} - F_{CL}(s) i_{cq0} \\ b = u_{cdo} - \omega L_c i_{cq0} - F_{CL}(s) i_{cd0} \end{cases} \tag{3.55}$$

$F_{CL}(s)$, $F_P(s)$ and $F_U(s)$ are defined in Section 3.1.1 and further expressions within 3.51 to 3.55 to are described in the Appendix A.2.

3.2 Power Synchronization Control

The power-synchronization control structure as described fully in [18, 36] is shown in Figure 3.6. The AC grid structure is again modelled as a Thevenin equivalent RL grid, as described in Section 3.1. Control is performed in the *dq*-frame, which is synchronized via the power synchronization loop (PSL) working on the active power error. An AC voltage loop (AVL) with integral control is embedded to determine the d-axis converter voltage reference and a high-pass current filter (HPF) is employed to damp low-order harmonic resonances, which arise due to the very high reactance of the weak AC grid which decreases in frequency as the grid SCR decreases [17, 72]. All inputs to the controller are measured at the PCC through a first-order low-pass filter.

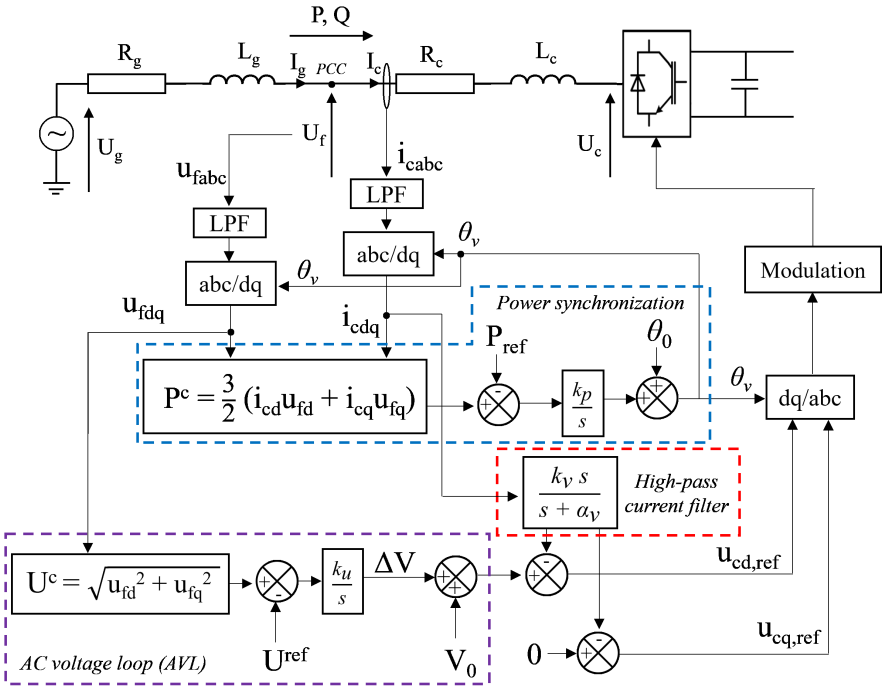

Fig. 3.6: Schematic diagram of VSC and AC grid test system with power synchronization control.

The eventual goal of developing these models will be to produce an assessment framework for any controller structure, and so the state-space model of PSC is developed in the same form as the VCC model in Section 3.1.1 i.e. the AC grid system representation is identical and the controller representation should have the same inputs and outputs to the grid such that controllers can be exchanged easily. This full, 'modular' state-space model is derived in Section 3.2.1. Impedance model and Jacobian transfer matrix representations of PSC, similar to those developed in [42, 43] will be explored as part of the generalised assessment framework in Chapter 6.

3.2.1 State-space small signal model

The AC grid, Park and inverse Park transformations and low-pass measurement filters employed in PSC are the same as those described and modelled in Section 3.1.1. Active power control and synchronization with the AC grid are both provided by the power

synchronization loop (PSL). The PSL acts on the power error to produce a reference angle, which is used as an input to the frame transformations in 3.35 and 3.37. The linearised PSL control law is given in 3.56.

$$\Delta\theta_v = \frac{k_p}{s}\left(\Delta P^{cf} - \Delta P^{c}_{ref}\right) \tag{3.56}$$

where, ΔP^{cf} is the filtered active power at the PCC in the converter frame, ΔP^{c}_{ref} is the active power reference, k_p is the PSL integral gain and $\Delta\theta_v$ is the controller reference angle.AC voltage control is used in this study (i.e. instead of reactive power control) in order to support the grid voltage of the ultra weak AC grid. The linearised control law for the AC voltage loop (AVL) is:

$$\Delta V = \frac{k_u}{s}\left(\Delta U^{cf} - \Delta U^{c}_{ref}\right) \tag{3.57}$$

where, ΔU^{cf} is the filtered AC voltage magnitude at the PCC in the converter frame, ΔU^{c}_{ref} is the AC voltage reference, k_u is the AVL integral gain and ΔV is the converter voltage reference deviation. In the state-space representation, the PSL and AVL are combined into a single outer loop block of the form,

$$\Delta\dot{x}_{OL} = B_{OL}\Delta u_{OL} \tag{3.58}$$

$$\Delta y_{OL} = C_{OL}\Delta x_{OL} \tag{3.59}$$

with state, input and output vectors:

$$\Delta x_{OL} = \begin{bmatrix}\Delta e_P & \Delta e_U\end{bmatrix}^T \tag{3.60}$$

$$\Delta u_{OL} = \begin{bmatrix}\Delta P^{c}_{ref} & \Delta U^{c}_{ref} & \Delta P^{cf} & \Delta U^{cf}\end{bmatrix}^T \tag{3.61}$$

$$\Delta y_{OL} = \begin{bmatrix}\Delta\theta & \Delta V\end{bmatrix}^T \tag{3.62}$$

The corresponding state-space matrices are:

$$B_{OL} = \begin{bmatrix}-1 & 0 & 1 & 0\\ 0 & -1 & 0 & 1\end{bmatrix} \tag{3.63}$$

$$C_{OL} = \begin{bmatrix} k_p & 0 \\ 0 & k_u \end{bmatrix} \tag{3.64}$$

In order to damp out the grid-frequency resonances in the system, a high-pass current filter is included to the converter voltage reference, such that the linearised converter voltage control law becomes:

$$\Delta u_{cd,ref} = \Delta V - H_{HP}(s)\Delta i^c_{cd} \tag{3.65}$$

$$\Delta u_{cq,ref} = -H_{HP}(s)\Delta i^c_{cq} \tag{3.66}$$

where the high-pass current filter (HPF) is given in 3.67.

$$H_{HP}(s) = \frac{k_v s}{s + \alpha_v} \tag{3.67}$$

where, k_v is the HPF gain and α_v is the HPF cut-off frequency. The converter voltage controller including the high-pass filter has the state-space form,

$$\Delta \dot{x}_{VC} = A_{VC}\Delta x_{VC} B_{VC}\Delta u_{VC} \tag{3.68}$$

$$\Delta y_{VC} = C_{VC}\Delta x_{VC} + D_{VC} u_{VC} \tag{3.69}$$

with input and output vectors:

$$\Delta u_{VC} = \begin{bmatrix} \Delta V & \Delta i^c_{cd} & \Delta i^c_{cq} \end{bmatrix}^T \tag{3.70}$$

$$\Delta y_{VC} = \begin{bmatrix} \Delta u^c_{cd} & \Delta u^c_{cq} \end{bmatrix}^T \tag{3.71}$$

The corresponding state-space matrices are:

$$A_{VC} = \begin{bmatrix} -\alpha_v & 0 \\ 0 & -\alpha_v \end{bmatrix} \tag{3.72}$$

$$B_{VC} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{3.73}$$

$$C_{VC} = \begin{bmatrix} -k_v\alpha_v & 0 \\ 0 & -k_v\alpha_v \end{bmatrix} \tag{3.74}$$

$$D_{VC} = \begin{bmatrix} 1 & k_v & 0 \\ 0 & 0 & k_v \end{bmatrix} \tag{3.75}$$

The above state-space models of the controller are connected to the linearised grid model and the full small signal model is shown in Figure 3.7.

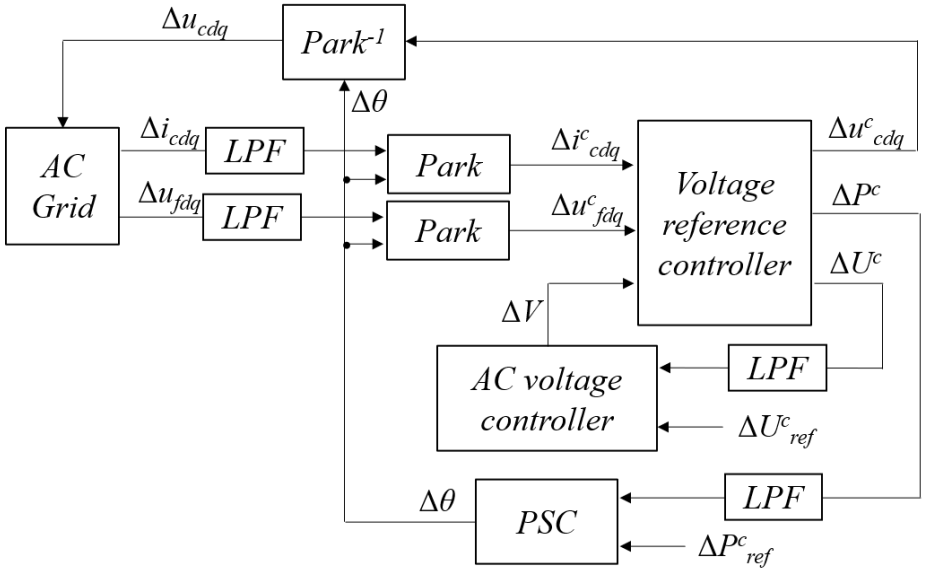

Fig. 3.7: Connected small-signal model of LCL-AC grid system and PSC controller.

Validation

The small signal model is validated by comparison with a non-linear MATLAB/Simulink time-domain simulation of the full system. Fig. 3.8 shows the results of 0.05 p.u. voltage and power steps in the small signal and time domain models. The small signal model shows very good transient agreement with the time-domain model and is therefore valid for small signal stability analysis.

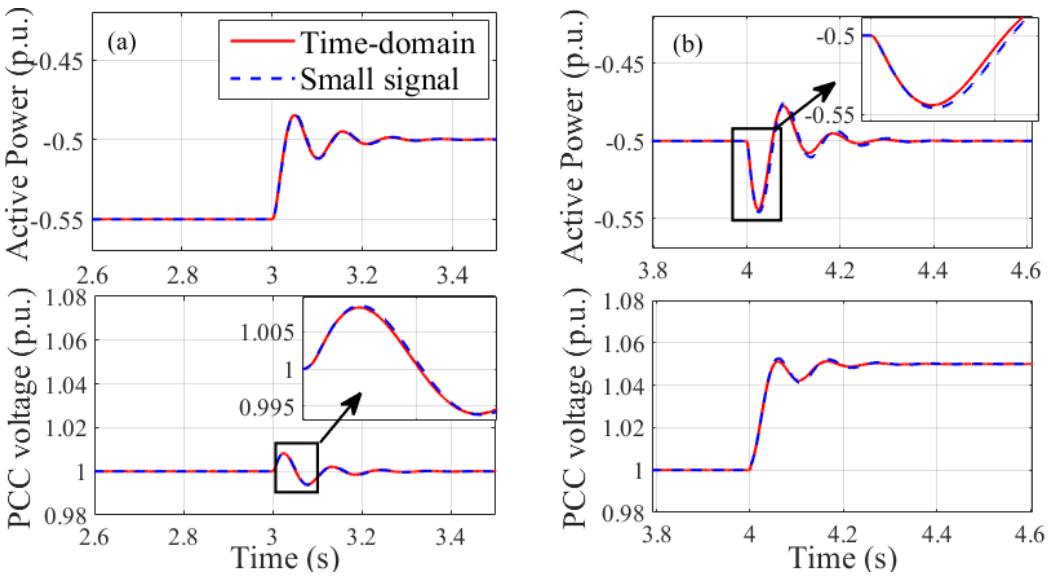

Fig. 3.8: Grid-connected PSC small signal model validation with active power and PCC voltage response to 0.05 p.u. power and voltage step changes.

3.3 Virtual Synchronous Machine

Many forms of virtual synchronous machine control exist in the literature, but all aim to emulate the inherent synchronization of mechanical synchronous machines. For this work, the simplest VSM controller is employed, implementing the second order swing equation for the active power control and synchronization, and a PI controller for the AC voltage control. This control structure is shown in Fig. 3.9. All inputs to the controller are measured at the PCC through a first-order low-pass filter and the AC grid is as presented and modelled in Section 3.1. The tunable control elements are the gain of the active power synchronization (k_{p-P_v} and k_{i-P_v}) and the gains of the AC voltage PI controller (k_{p-U_v} and k_{i-U_v}).

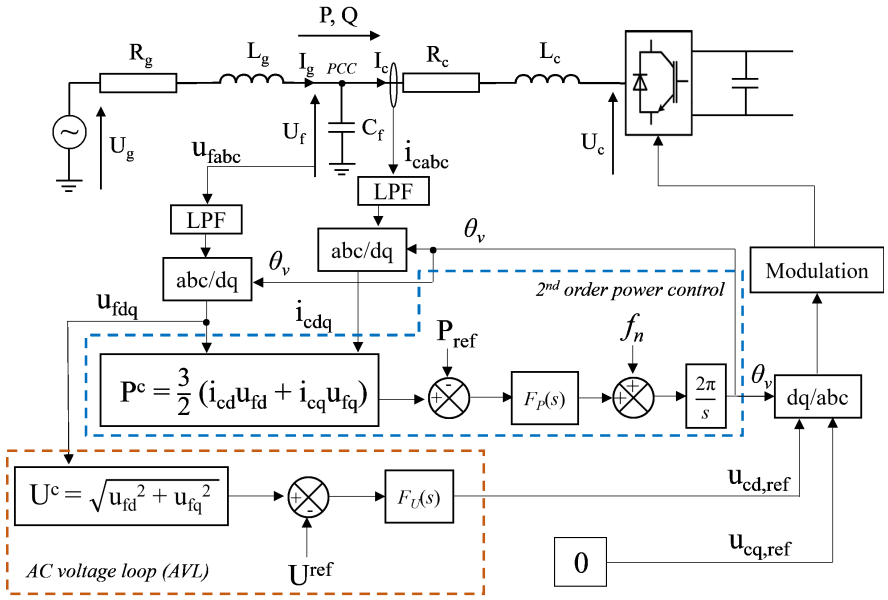

Fig. 3.9: VSM control structure.

The linearised state-space equations for the power control and reference angle generation are:

$$\Delta \dot{x}_P = B_P \Delta u_P \tag{3.76}$$

$$\Delta y_P = C_P \Delta x_P \tag{3.77}$$

where, the input and output vectors are $\Delta u_P = \begin{bmatrix} \Delta P^c_{ref} & \Delta P^{cf} & \Delta f_{p,ref} \end{bmatrix}^T$ and $\Delta y_P = \Delta f_P$ respectively. The corresponding state-space matrices are:

$$B_p = \begin{bmatrix} -1 & 1 & 0 \end{bmatrix} \tag{3.78}$$

$$C_p = \frac{k_{i-Pv}}{S_{base}} \tag{3.79}$$

$$D_p = \frac{1}{S_{base}} \begin{bmatrix} -k_{p-Pv} & k_{ip-Pv} & 1 \end{bmatrix} \tag{3.80}$$

The small-signal voltage reference control is given by the linearised equations:

$$\Delta \dot{x}_U = B_U \Delta u_U \tag{3.81}$$

$$\Delta y_U = C_U \Delta x_U \tag{3.82}$$

where, the input and output vectors are $\Delta u_U = \begin{bmatrix} \Delta U^c_{ref} & \Delta U^{cf} \end{bmatrix}^T$ and $\Delta y_p = \begin{bmatrix} \Delta u^c_{cd} & \Delta u^c_{cq} \end{bmatrix}^T$, respectively. The corresponding state-space matrices are:

$$B_U = \begin{bmatrix} 1 & -1 \end{bmatrix} \tag{3.83}$$

$$C_U = \begin{bmatrix} k_{i-Uv} & 0 \end{bmatrix} \tag{3.84}$$

$$D_U = \begin{bmatrix} -k_{p-Uv} & -k_{p-Uv} \\ 0 & 0 \end{bmatrix} \tag{3.85}$$

Validation

The small signal model is validated by comparison with a non-linear MATLAB/Simulink time-domain simulation of the full system. Fig. 3.10 shows the results of a 0.05 p.u. power step in the small signal and time domain models. The small signal model shows very good transient agreement with the time-domain model and is therefore valid for small signal stability analysis.

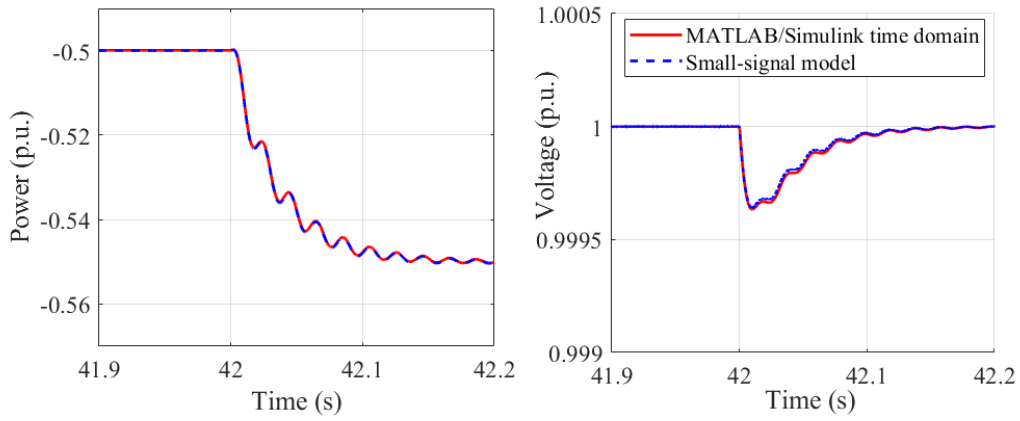

Fig. 3.10: Grid-connected VSM small signal model validation with active power and PCC voltage response to a 0.05 p.u. power step change.

3.4 Summary

The small-signal models derived in this chapter for vector current control, power synchronization control and a simple virtual synchronous machine control have been validated against MATLAB/Simulink time-domain simulations and can therefore be used for eigenvalue stability analysis and comparison is this work. All aspects of the control structures and synchronization have been modelled and the linearised control models have been constructed so as to be compatible with the same linearised AC grid model.

Chapter 4

Novel Controller Interaction Analysis of Vector Current-Controlled VSC-HVDC

In this chapter, time- and frequency-domain stability assessments are performed to evaluate the stability limits, robustness and dynamic performance of vector current control for VSC-HVDC in very weak AC grids. The goal of this analysis is to provide a more comprehensive analysis of the precise limits of VCC than has previously been perfomred, and to investigate how the different elements of the controller interact at different bandwidths. The stability impact of individual cascaded loops within each control structure is quantified and the interactions between any two control loops are assessed. The impact of three-way interactions on stability is also examined in order to extract all controller operating points that can provide both stable operation and acceptable dynamic performance at a fixed power transfer level. Robustness to changes in SCR is also examined.

4.1 Study Parameters

The performance of VCC-VSC in a very weak grid will be assessed via two metrics:

1. The bidirectional active power transfer limits of the converter-controller system as a function of the bandwidth of each control loop.

2. The construction of a number of 'stability bubbles' which represent the stable operating space for given active power transfer and dynamic performance requirements.

The first metric is addressed in Section 4.2 and the concept of the stable operating region is introduced and analysed in Section 4.3. Both forms of evaluation use a novel stability methodology which is based on conventional eigenvalue analysis and is explained in detail in Sections 4.2 and 4.3. The AC grid, VSC and vector current controller for this study are as presented in Section 3.1. A very weak AC grid with SCR = 1 is used and the AC system parameters are based on the study systems in [18, 44]. The SCR is based on the rated active power of the converter and defines the impedance of the AC grid from the PCC. These parameters are detailed in Table 4.1. In order to avoid low frequency passive resonances on the AC side, the filter capacitance, C_f , is zero [44, 74]. All reactive power will instead be provided by the VSC and it is therefore overrated to approximately 1.58 p.u. apparent power. The VSC voltage rating is 1.22 p.u..

Table 4.1: AC system parameters

Parameter	Value
AC system rated voltage, RMS line (kV)	195
AC system rated power (MW)	350
AC system frequency (Hz)	50
SCR	1
X/R ratio	10
DC link rated voltage (kV)	200
LPF filter time constant (s)	1×10^{-4}
AC system inductance, L_g (H)	0.3441
AC system resistance, R_g (Ω)	10.8104
Filter/transformer inductance, L_c (H)	0.0692
Filter/transformer resistance, R_c (Ω)	1.0864
Filter capacitance, C_f (μF)	0

4.2 Two-way Controller Interactions

In this study, the small-signal model derived in Section 3.1 is used to determine the active power limits for VCC-VSC across a wide range of controller bandwidths. At each operating point, the maximum active power (measured at the PCC) that can be exchanged between the grid and the VSC whilst maintaining stability is calculated in both inverting and rectifying modes. For the ICL and PLL, the bandwidths can be varied directly by controlling α and τ_{pll} and are therefore defined by these quantities as in Section 3.1.1. For the APL and AVL, no single parameter in the small signal model can exactly define the bandwidth due to the system cross-coupling. However, the integral gains k_{i-P} and k_{i-U} can be used as proxies for the APL and AVL bandwidths respectively while the proportional gains are kept constant. An approximate value of the +/- 3 dB bandwidth can then be extracted from the respective channel of the small signal model. This stability limit approach builds on existing eigenvalue stability methods. However, current eigenvalue analysis examines the influence of only one variable (either active power transfer level or the tuning of one controller parameter); this methodology determines the stability limit as a function of three variables (two

controller tunings and the active power). For each set of controller parameters, small signal models are constructed at power steps of 0.001 p.u. in the interval -1.0 to 1.0 p.u. using initial conditions calibrated from the time-domain simulation. Eigenvalue analysis is then used to determine if each of these systems is stable. The boundaries between stability and instability are determined by linear bisection, giving the inverting and rectifying active power transfer limits for that controller configuration. This process is repeated with the gains of two control loops fixed while the gains of the other two control loops are varied simultaneously. This iterative process is shown in the flowchart in Fig. 4.1. Values for the controller gains when a given loop is fixed are based on [44] and given in Table 4.2. The gain and bandwidth ranges covered when varying a given loop are given in Table 4.3. These ranges were chosen to provide at least one order of magnitude variation in ICL bandwidth and at least two orders of magnitude variation in APL, AVL and PLL bandwidths about the 'default' settings.

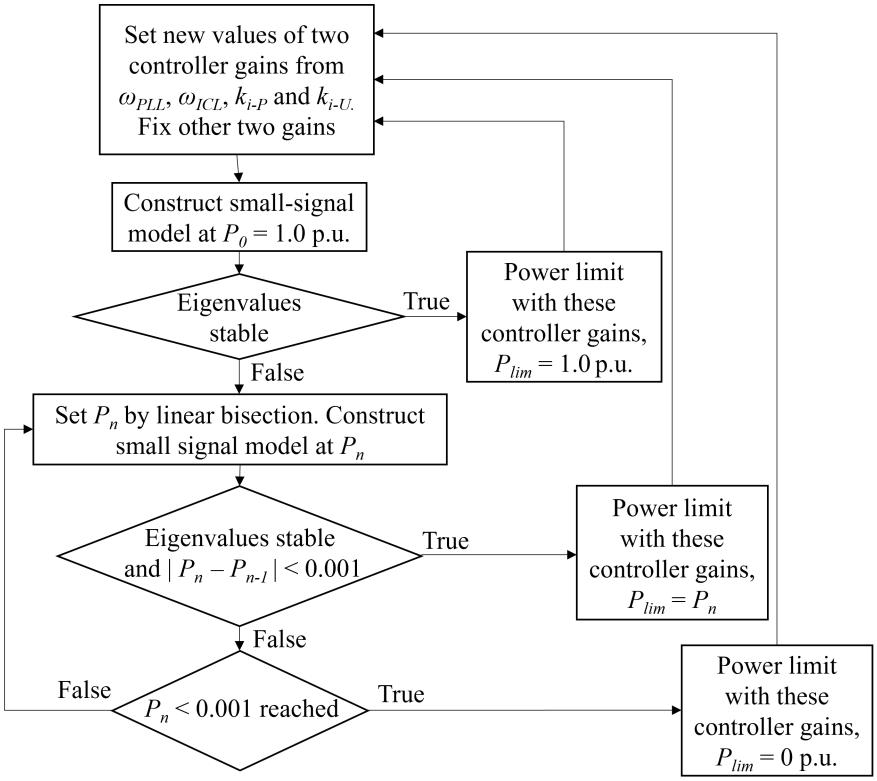

Fig. 4.1: Flowchart of the stability analysis methodology to determine active power limits at a broad range of controller tunings.

Table 4.2: Default VCC tuning parameters

Control loop	Parameters	Value
ICL	$\alpha = 1/\omega_{ICL}$ (s)	0.0015
	k_{p-I}	13.8
	k_{i-I}	217.3
PLL	$\tau_{pll} = k_{p-pll}/k_{i-pll}$ (s/rad)	0.159
	k_{p-pll}	1.315×10^{-5}
	k_{i-pll}	8.263×10^{-5}
APL	k_{p-P}	1×10^{-6}
	k_{i-P}	1×10^{-3}
AVL	k_{p-U}	2×10^{-2}
	k_{i-U}	0.3

Table 4.3: VCC operating point ranges

Control loop	Parameter	Parameter range	Equivalent bandwidth range
ICL	α (s)	$10^{-4} - 10^{-3}$	$\omega_{ICL} = 100 - 1000$ Hz
PLL	τ_{pll} (s/rad)	$0.0045 - 0.45$	$\omega_{PLL} = 0.5 - 50$ Hz
APL	k_{i-P}	$10^{-4} - 10^{-2}$	$\omega_{APL} \approx 2.5 - 480$ Hz
AVL	k_{i-U}	$0.03 - 30$	$\omega_{AVL} \approx 0.5 - 230$ Hz

The operating point sweeps performed with the small signal model for maximum power transfer are shown in Fig. 4.2 to Fig. 4.7. Fig. 4.2 shows the active power transfer limits for varying ICL and PLL bandwidths, demonstrating two distinct high-stability regions at low and high PLL bandwidth in the inverting mode, and an overall increase in stability with increasing ICL bandwidth. A low PLL bandwidth is proposed in e.g. [25, 35] to stabilize very weak grid AC systems. However, this proposed wider range analysis reveals an additional stable region at higher PLL bandwidths – this observation is analysed further in the discussion. As discussed in [75], a slower ICL with respect to the PLL is destabilizing in both power directions due to the impact

on the negative-real-part of the input-admittance. Fig. 4.3 shows the active power transfer limits for varying APL and PLL bandwidths. Fig. 4.3(a) shows a very similar pattern for the PLL bandwidth impact, but this effect is less exaggerated for the APL-to-PLL interaction than the ICL-to-PLL interaction. A slow APL improves stability in both power directions at all PLL bandwidths. The APL is shown in [24] to impact the PLL-related dominant oscillation mode. A fast APL increases the negative damping of this mode and thus destabilizes the system. Fig. 4.4 shows the active power transfer limits for varying AVL and PLL bandwidths. In this case, two regions of stability at low and high PLL bandwidths are again visible in the inverting mode. However, a high AVL bandwidth increases stability at low PLL bandwidth, but the reverse holds at high PLL bandwidth. This is due to the competing influences of the non-minimum phase behavior of the power response and the negative damping off the PLL mode on the system stability. A step increase in the active power reference will increase i_{cd}, but in very weak AC grids this will cause a decrease in the PCC voltage. The AVL produces reactive power to support the voltage, but there is a delay in the control which leads to an initial decrease in the power [44]. As such, speeding up the AVL to decrease this non-minimum phase behavior will stabilize the system. However, as discussed in [24], the negative damping of the PLL-related dominant oscillation mode first increases and then reduces as the AVL bandwidth is increased. These competing mechanisms lead to complicated trends in the stability limits when the AVL is considered. In rectifying mode, stability decreases with increasing AVL and PLL bandwidths as the negative damping effects of the PLL mode dominate. Fig. 4.5 shows the active power transfer limits for varying APL and ICL bandwidths. In inverting mode (Fig. 4.5(a)), stability is almost independent of APL bandwidth, but in rectifying mode a fast APL causes significant instability, particularly when the ICL is slow. This echoes the pattern seen in Fig. 4.3. If the APL bandwidth is too fast, the inner and outer loops are no longer decoupled by their different time scales and this destabilizes the system. Fig. 4.5 shows the active power transfer limits for varying AVL and ICL bandwidths. In inverting mode, a fast AVL is stabilizing. In this case the PLL bandwidth is fixed at 1 Hz (as per the 'default' values in Table 4.2) and so the non-minimum phase effect of

the power response dominates over the negative damping of the PLL mode. However, the AVL-to-ICL interaction is more complex in rectifying mode. When the ICL is fast, a slower AVL is stabilizing. As the ICL bandwidth decreases below approx. 680 Hz, the optimum AVL bandwidth increases. In rectifying operation, the negative damping of the PLL-mode competes more strongly with the non-minimum phase behavior of the power response, leading to a complex stability pattern. Fig. 4.7 shows the active power transfer limits with varying APL and AVL bandwidths. Increasing the APL bandwidth decreases stability as seen in Fig. 4.3 and Fig. 4.5. There is an optimum, intermediate value of AVL bandwidth as different system modes dominant stability, as discussed in Fig. 4.4. For clarity, k_{i-U} is plotted as the proxy for AVL bandwidth in Fig. 4.7 due to the impracticality, discussed in Section IV, of directly specifying the bandwidth in the small signal model. The dq-frame cross-coupling means that the AVL bandwidth at a given value of k_{i-U} varies slightly as the APL bandwidth is varied (via k_{i-P}) so each curve would require a unique axis in order to directly plot the bandwidth. However, an additional scale showing the approximate AVL bandwidth is included within Fig. 4.7.

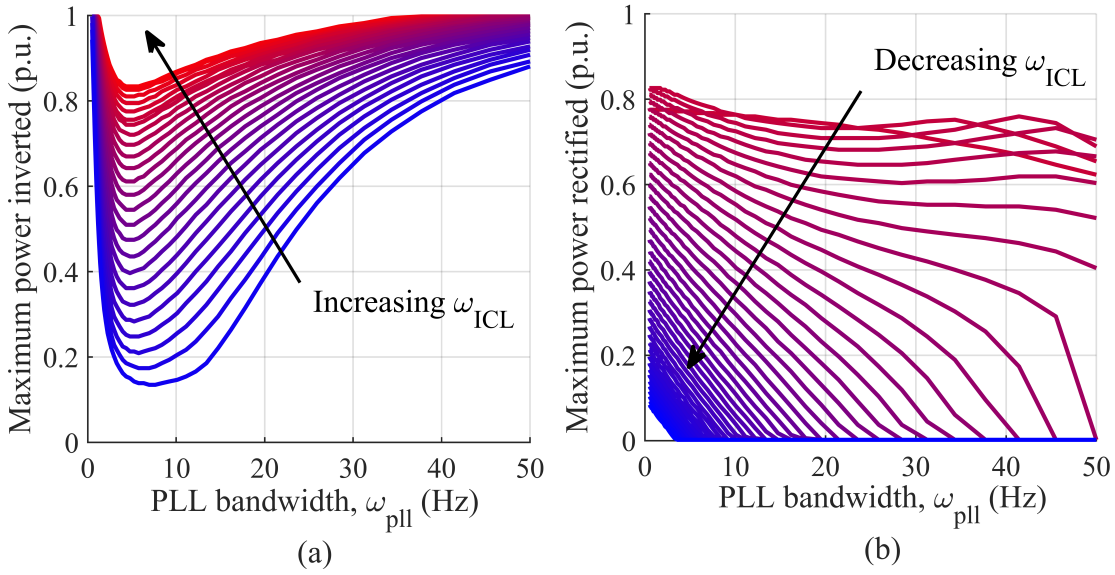

Fig. 4.2: Maximum active power transfer as a function of ICL and PLL bandwidths (low ICL bandwidths shown in blue and high ICL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

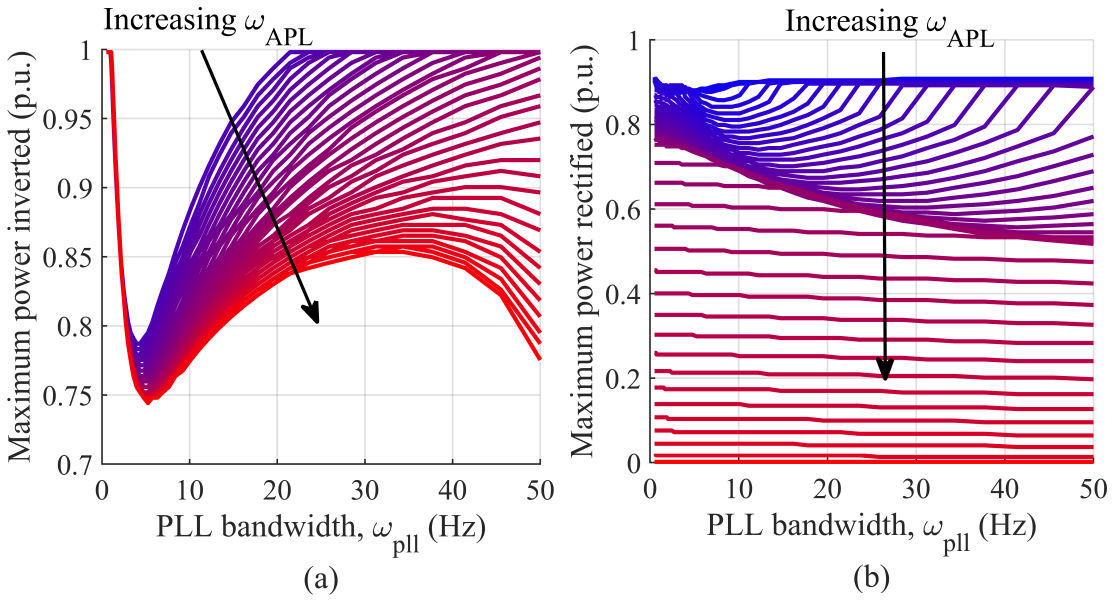

Fig. 4.3: Maximum active power transfer as a function of APL and PLL bandwidths (low APL bandwidths shown in blue and high APL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

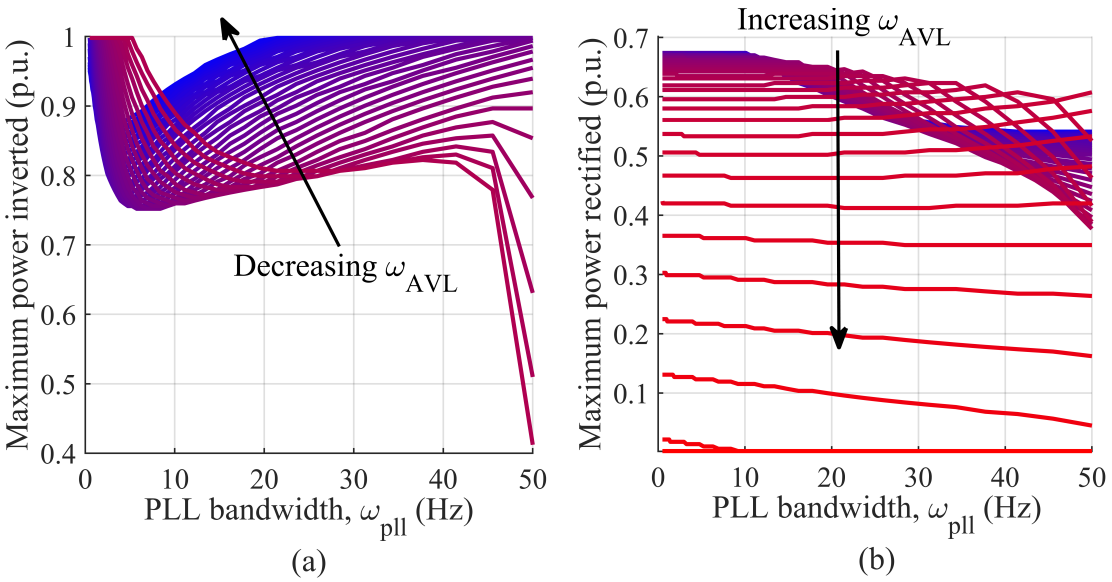

Fig. 4.4: Maximum active power transfer as a function of AVL and PLL bandwidths (low AVL bandwidths shown in blue and high AVL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

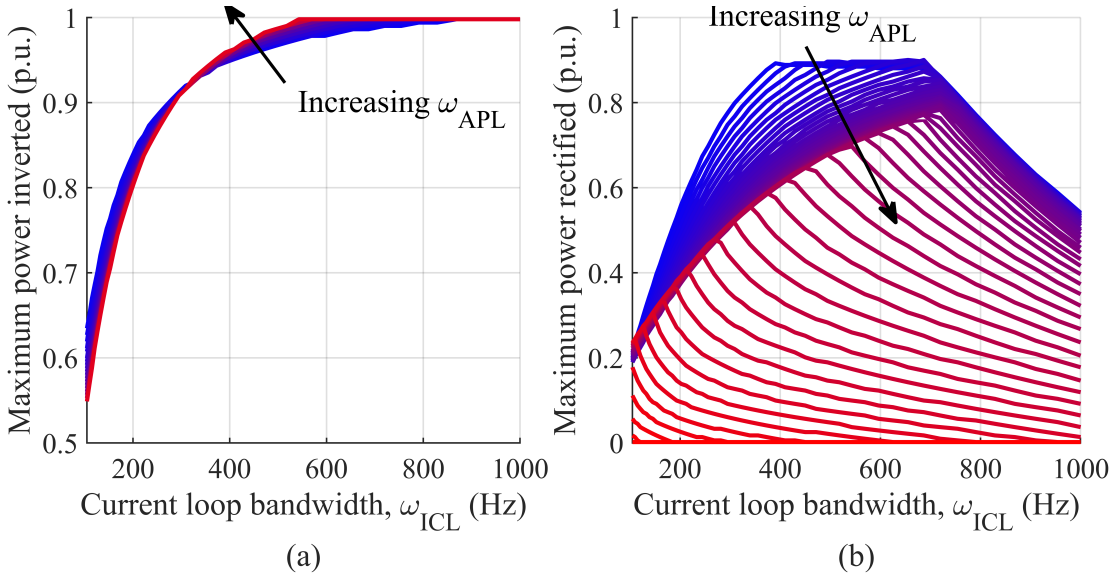

Fig. 4.5: Maximum active power transfer as a function of APL and ICL bandwidths (low APL bandwidths shown in blue and high APL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

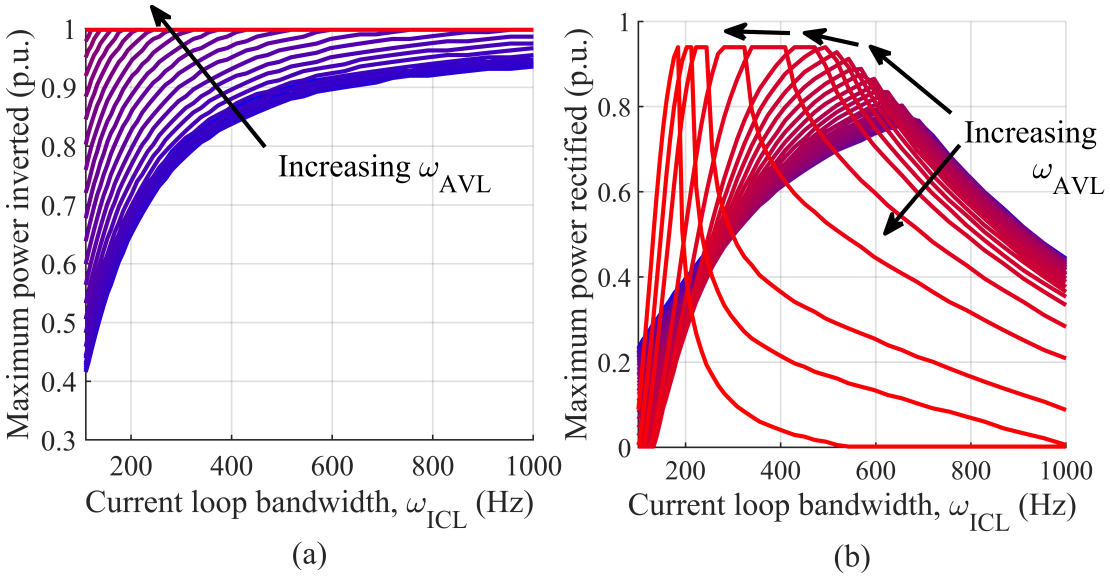

Fig. 4.6: Maximum active power transfer as a function of AVL and ICL bandwidths (low AVL bandwidths shown in blue and high AVL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

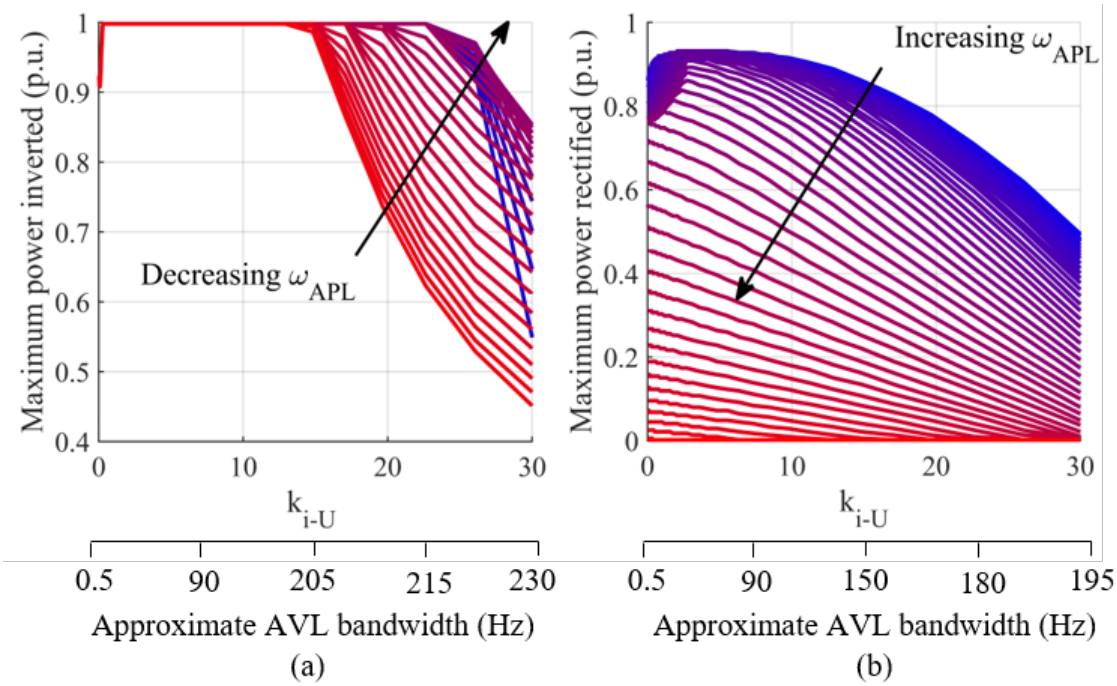

Fig. 4.7: Maximum active power transfer as a function of APL and AVL bandwidths (low APL bandwidths shown in blue and high APL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

4.2.1 Discussion - general observations

In inverting mode, rated active power can be transferred if appropriate controller parameters are chosen. However, in rectifying mode, rated active power cannot be achieved at any operating point. Small signal stability is more sensitive to controller tuning and control loop interactions in rectifying mode than in inverting mode. This makes intuitive sense given the asymmetry between active power exchanged and converter voltage angle in the steady-state [76]. A fast ICL with respect to the outer loops is required for maximum stability. In general, slowing down the APL, AVL and PLL (i.e. decreasing the bandwidths) improves the system stability. The exception to this is the AVL at some operating points and the multiple stable regions of PLL bandwidth in inverting mode. With a slow ICL or fast PLL, increasing the AVL bandwidth can increase the maximum active power transfer (e.g. Fig. 4.4(a) and Fig. 4.7). The impact of grid strength on stability can be more easily examined using the impedance model derived

in Section 3.1.2. Fig. 4.8 shows the bode diagram of the closed-loop impedance model, $[\mathbf{I} + \mathbf{Y}(s)\mathbf{Z_g}(\omega_g, s)]^{-1}$ at SCR = 1, 2, 3 and 5. In Fig. 4.8, part (a) shows the bode diagram from Δu_{fd} to Δi_{cd}, part (b) shows the bode diagram from Δu_{fq} to Δi_{cd}, part (c) shows the bode diagram from Δu_{fd} to Δi_{cq} and part (d) shows the bode diagram from Δu_{fq} to Δi_{cq}. For SCR = 1, all of the responses in Fig. 4.8 show very strong resonances at the PLL bandwidth (1 Hz) but these resonances are almost non-existent when the grid is strengthened. A large grid impedance amplifies the coupling between the grid and the controller via the PLL and thus decreases the stable operating region of vector control. The effect of the PLL is examined more closely in the following section.

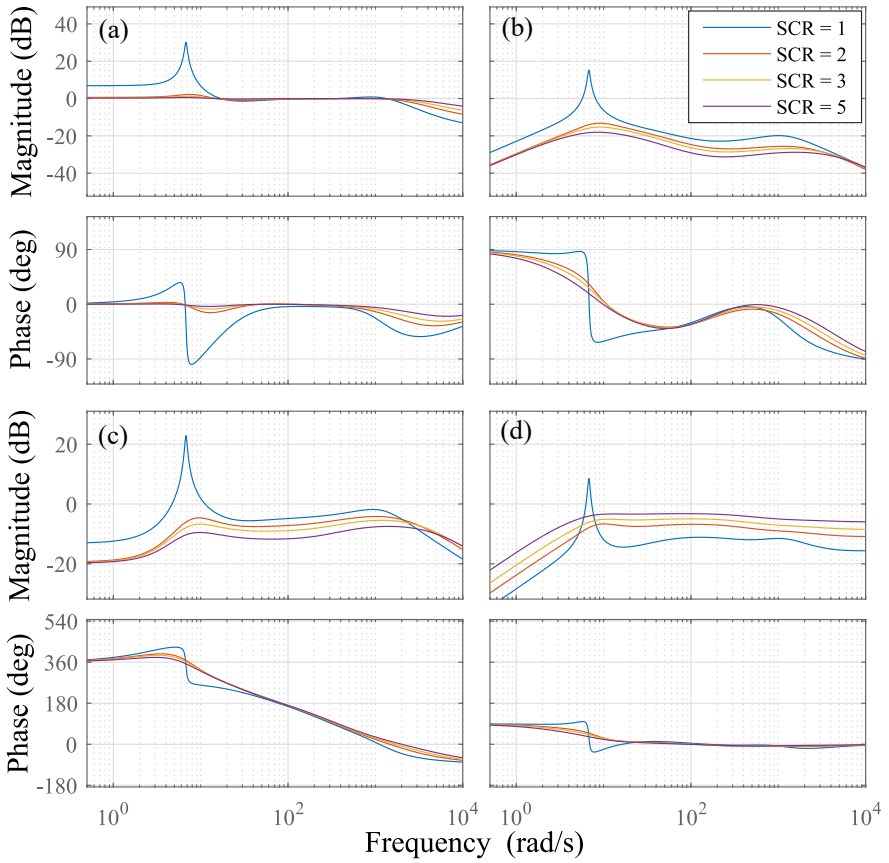

Fig. 4.8: Bode diagram of the closed-loop impedance model at varying SCR: (a) Δu_{fd} to Δi_{cd}, (b) Δu_{fq} to Δi_{cd}, (c) Δu_{fd} to Δi_{cq}, and (d) Δu_{fq} to Δi_{cq}.

4.2.2 PLL operating regions

Fig.s 4.2(a), 4.3(a) and 4.4(a) show two distinct regions of high system stability for inverting operation. Optimum performance (i.e. maximum active power injection to the AC grid) is achieved at both very low PLL bandwidth ($\omega_{PLL} < 5$ Hz) and some higher PLL bandwidths ($\omega_{PLL} > 30$ Hz). This stability variation is again easier to analyze using the impedance model developed in Section 3.1.2. As discussed, stability is determined by the impedance ratio $\mathbf{Y}(s)\mathbf{Zg}(\omega_g, s)$; specifically, it is the dq component of each impedance which is limiting in very weak AC grids i.e. i_{cd} to u_{fq}. Fig. 4.9 shows the bode diagrams of $[Y(s)]_{dq}^{-1}$ and $Z_{g-dq}(\omega_g, s)$ for PLL bandwidth from 0.5 Hz to 50 Hz. A magnitude of $[Y(s)]_{dq}^{-1}$ below the $Z_{g-dq}(\omega_g, s)$ grid impedance magnitude is one indicator of system instability. It can be seen that this occurs only at intermediate values of PLL bandwidth. At high ω_{PLL}, the VSC behaves as a grid-following converter i.e. the controller reference frame is synchronized to transient changes in the PCC voltage phase via the PLL. However, at very low ω_{PLL} the PLL effectively provides a fixed reference angle, which depends only on the steady-state value of the PCC voltage phase. This leads to an interesting phenomenon at low ω_{PLL} in which the controller appears to mimic some of the behaviours of grid-forming operation. Between these regions, active power transfer performance is significantly reduced as the PLL is too slow to synchronize effectively with the grid, but too fast to provide a fixed reference angle. Depending on the power transfer and transient performance requirements, VSCs in weak AC grids could therefore be deployed in a conventional grid-following mode or in this quasi-fixed-angle mode by simply changing the PLL bandwidth. Regardless of the mode selection, the operating point must be comfortably within one of these stable regions.

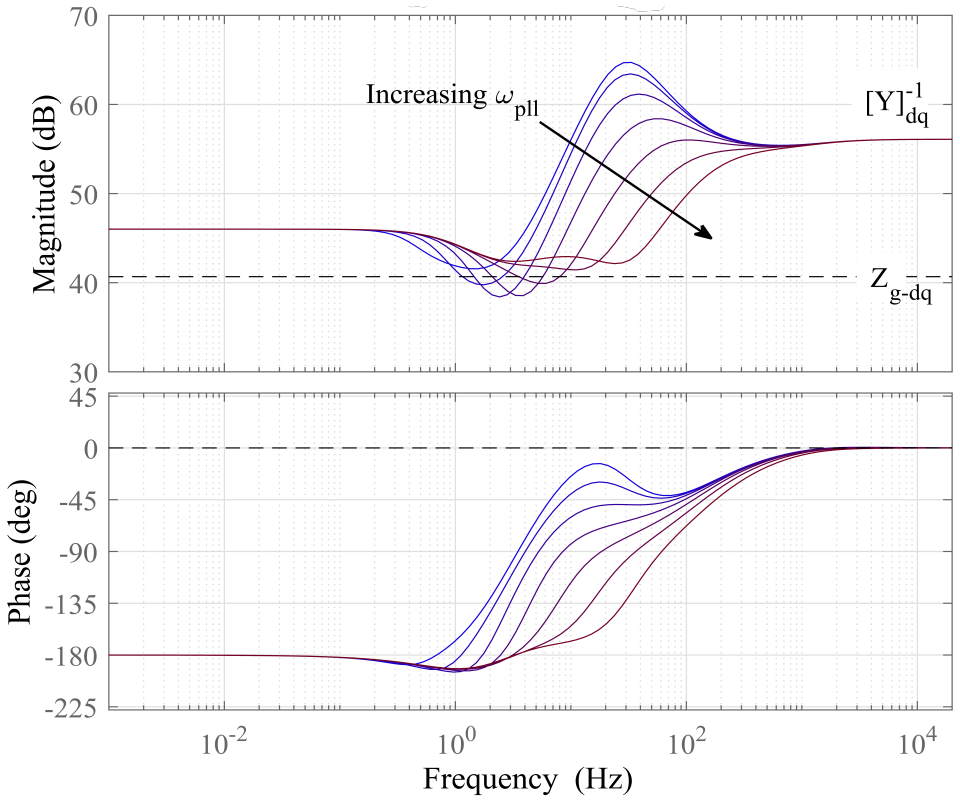

Fig. 4.9: Bode diagram of the *dq* VSC and grid impedances with varying PLL bandwidth.

These distinct regions of high stability are not present in rectifying operation, but there is an overall decrease in stability as PLL bandwidth increases. It would therefore be recommended that operation with a slow PLL bandwidth is chosen in systems where bi-directional power flow is required. However, for rectifying operation alone there is no requirement to avoid intermediate PLL bandwidth values.

4.3 Stability Boundary and Safe Operating Region

4.3.1 Stable operating regions

The operating point sweeps described in Section 4.2 can be applied, with appropriate modifications, to all VCC-based VSC control strategies. This gives a much more detailed view of system stability and controller interactions than the single operating point analyses that are commonly performed. Insights are also provided into the robust-

ness of conventional VCC to tuning variations. The output of this more comprehensive evaluation is thus a stability bubble of operating points as which stable operation is ensured. A suggested definition for this region is:

> *All operating points at which the system remains stable for* $\leq$ ***1.0 p.u.*** *active power transfer into the AC grid (i.e. inverting) and for* $\leq$ ***0.70 p.u.*** *active power transfer into the DC link (i.e. rectifying).*

A rectifying power level of 0.7 p.u. is chosen to ensure a large enough operating region for meaningful analysis. Evidently, this is difficult define in four-dimensional space if considering all controller components. However, as discussed earlier in section 4.2, a fast ICL is considered a basic requirement for vector control. Therefore, this region is defined only as a function of the PLL, APL and AVL bandwidths. This stability bubble definition is technology agnostic, so any stability analysis method (e.g. impedance modelling, eigenvalue analysis, bode diagrams) can be used to determine the controller parameters which satisfy these criteria. For this work, stability is assessed using eigenvalue analysis of the state space small signal model. The eigenvalues of this MIMO system, λ_{PU}, are a function of ω_{APL}, ω_{AVL}, ω_{PLL}, ω_{ICL}, P^c_{ref} and U^c_{ref}. By setting the ICL bandwidth at the 'default' value given in Table 4.2 and $\Delta U^c_{ref} =$ 1.0 p.u., minimum power transfer levels can then be chosen so that the eigenvalues now depend only on the APL, AVL and PLL bandwidths. The small signal model is reproduced at every combination of these bandwidths for the ranges in Table 4.3 and the system eigenvalues are checked for stability. This process is described in the flowchart in Fig. 4.10. This criterion produces a stability bubble of PLL, APL and AVL controller tunings, shown in Fig. 4.11. This region represents all combinations of PLL, APL and AVL parameters which can achieve between -1.0 p.u. and 0.7 p.u. power transfer.

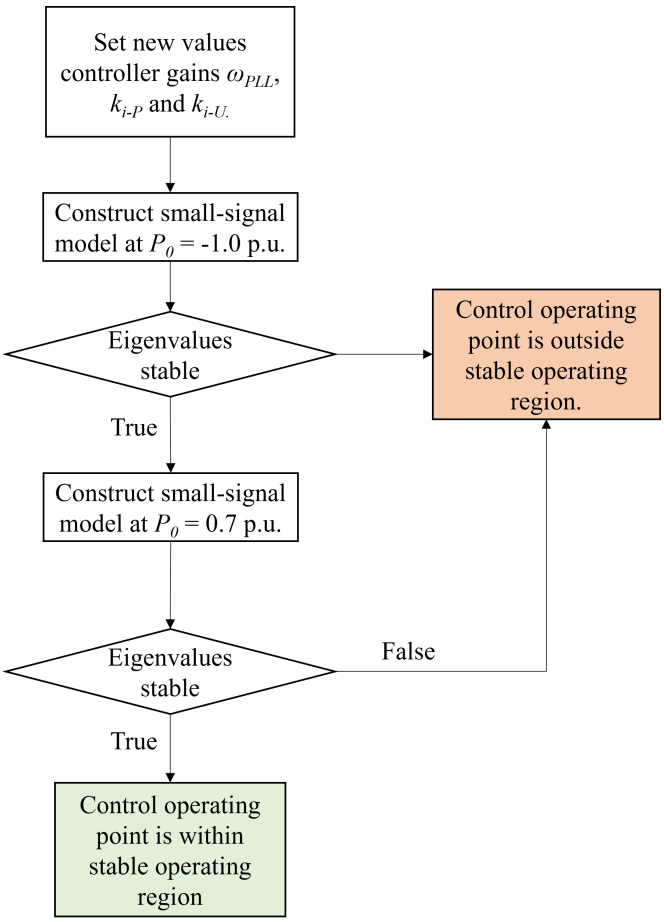

Fig. 4.10: Flowchart of the stability analysis methodology to determine stable operating region as a function of controller tunings.

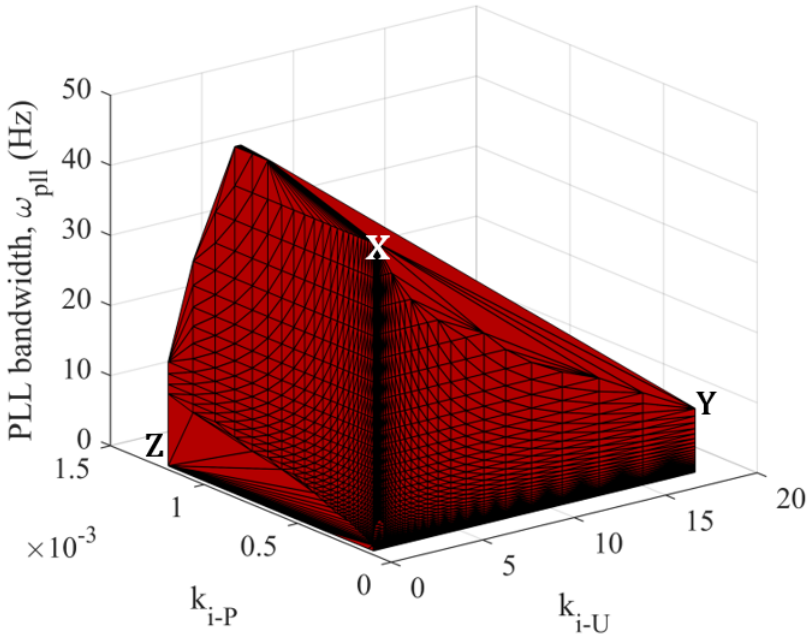

Fig. 4.11: Stable operating region for -1.0 p.u. $< P <$ 0.7 p.u.

Time-domain simulations at the 'corners' of this stability region (X, Y, Z) are shown in Fig. 4.12 to validate the stability boundary. These points were selected in order to cover a broad range of operating points within the stability bubble and a different controller parameter is used to induce instability in each case. Fig. 4.12(a) corresponds to point, X, marked on Fig. 4.11 and instability is caused by perturbing the PLL bandwidth. Fig. 4.12(b) corresponds to point, Y, and instability is caused by perturbing the AVL bandwidth. Fig. 4.12(c) corresponds to point, Z, and instability is caused by perturbing the APL bandwidth. At, X, and, Y, the inverting mode is the limiting case (at -1.0 p.u.), and at, Z, the rectifying mode is limiting (at 0.7 p.u.). The controller parameters at these points are given in Table 4.4.

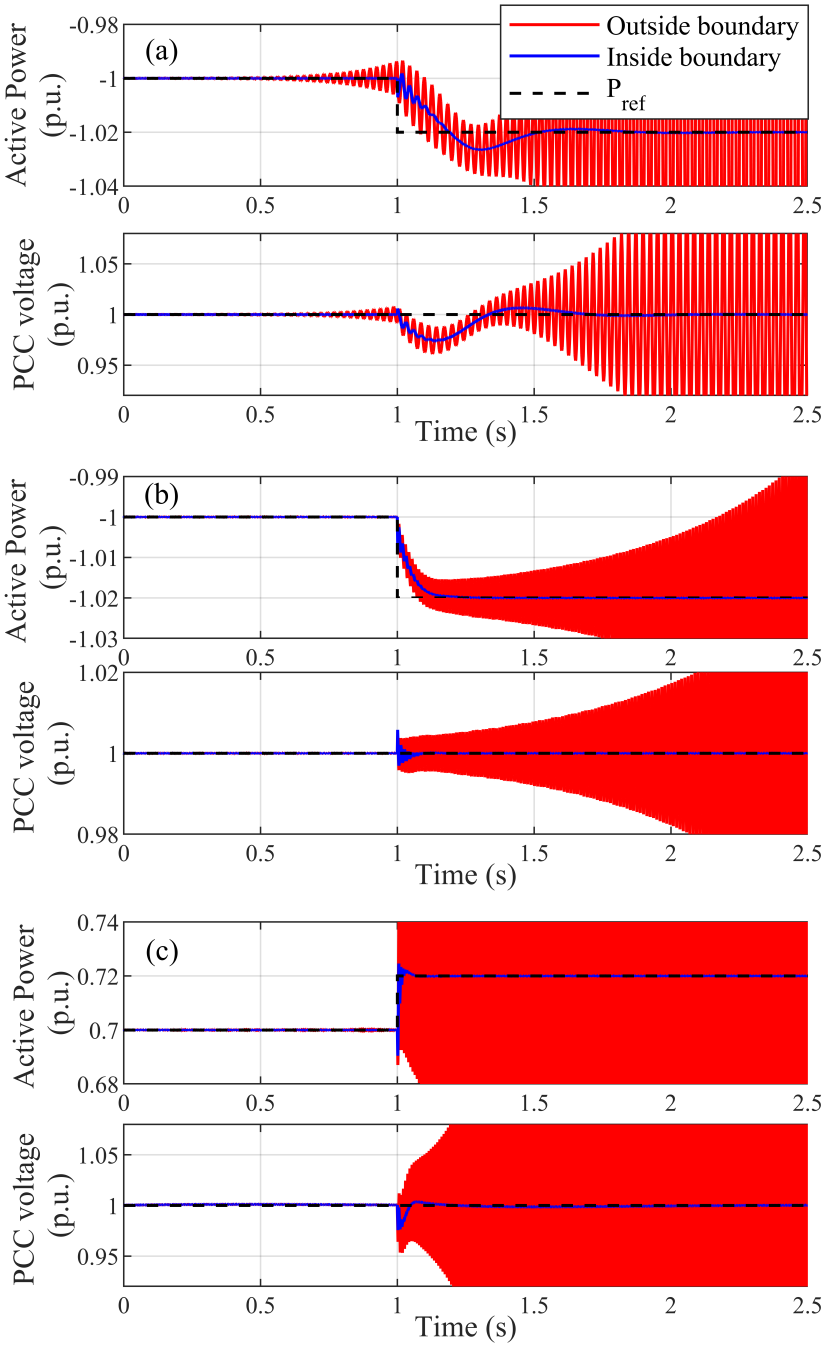

Fig. 4.12: Active power and PCC voltage responses to a 0.02 p.u. step in active power inside (blue) and outside (red) the stability boundary at (a) point X, (b) point Y and (c) point Z in Fig. 4.11

Table 4.4: Controller parameters at small signal stability boundary

Corner point	Parameters within boundary (stable)	Parameters outside boundary (unstable)
X	$\omega_{pll} = 44$ Hz $k_{i-P} = 1 \times 10^{-4}$ $k_{i-U} = 0.1$	$\omega_{pll} = 45$ Hz $k_{i-P} = 1 \times 10^{-4}$ $k_{i-U} = 0.1$
Y	$\omega_{pll} = 9.5$ Hz $k_{i-P} = 1 \times 10^{-4}$ $k_{i-U} = 18.0$	$\omega_{pll} = 9.5$ Hz $k_{i-P} = 1 \times 10^{-4}$ $k_{i-U} = 18.3$
Z	$\omega_{pll} = 0.5$ Hz $k_{i-P} = 1.2 \times 10^{-3}$ $k_{i-U} = 0.3$	$\omega_{pll} = 0.5$ Hz $k_{i-P} = 1.3 \times 10^{-3}$ $k_{i-U} = 0.3$

4.3.2 CHiL validation

In order to validate that the full power range shown in Fig.4.11 is achievable in control hardware (which is limited by switching frequencies and processing speeds), control hardware-in-the-loop (CHiL) experiments are performed using the RTDS and microcontroller setup shown in Fig. 4.13. The microcontroller is a TI C2000 Real-Time controller which is interfaced to the RTDS with the same inputs and outputs as would be received from the grid. The system is programmed via RSCAD and Simulink/C++ and a schematic of the CHiL connections and signal routings is shown in Fig. 4.14. The time step of the RTDS, $T_{s,plant}$, is 3.2 μs and the microcontrollers use a control time step, $T_{s,control}$, of 10 μs (equivalent to a 10 kHz switching frequency). A full ramp to -1.0 p.u. power (inverting) and to 0.7 p.u. power (rectifying) is performed with this set-up and is shown in Fig. 4.15. This confirms that the power range assessed in Fig. 4.11 is indeed stable in a control hardware implementation.

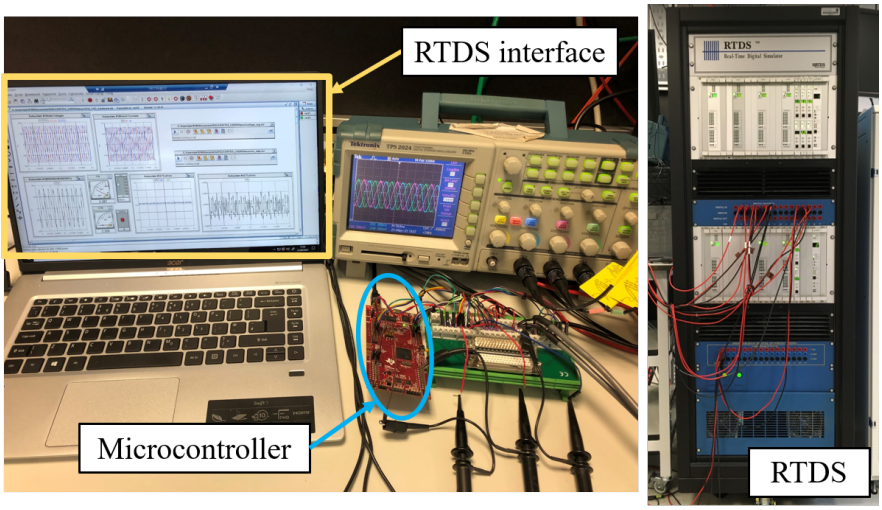

Fig. 4.13: RTDS and control hardware-in-the-loop test setup.

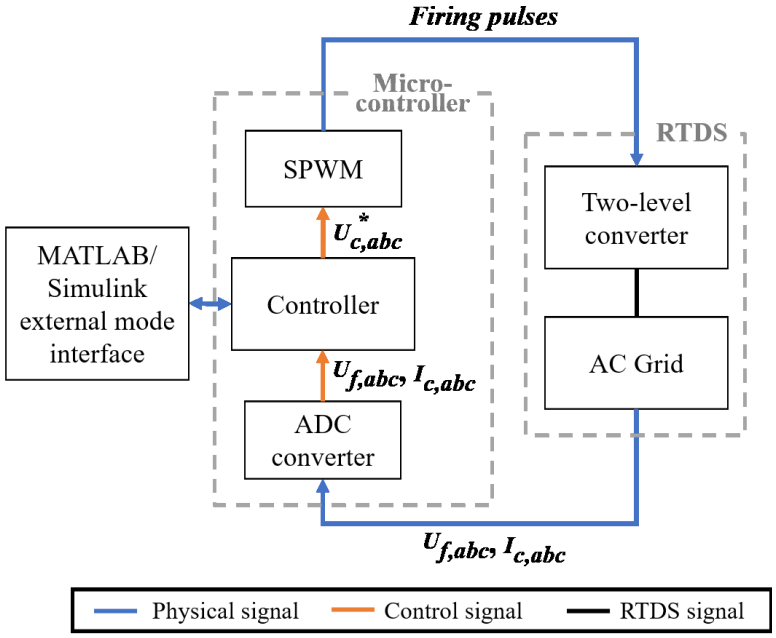

Fig. 4.14: Schematic of the CHiL setup and signal routing between the microcontroller and RTDS.

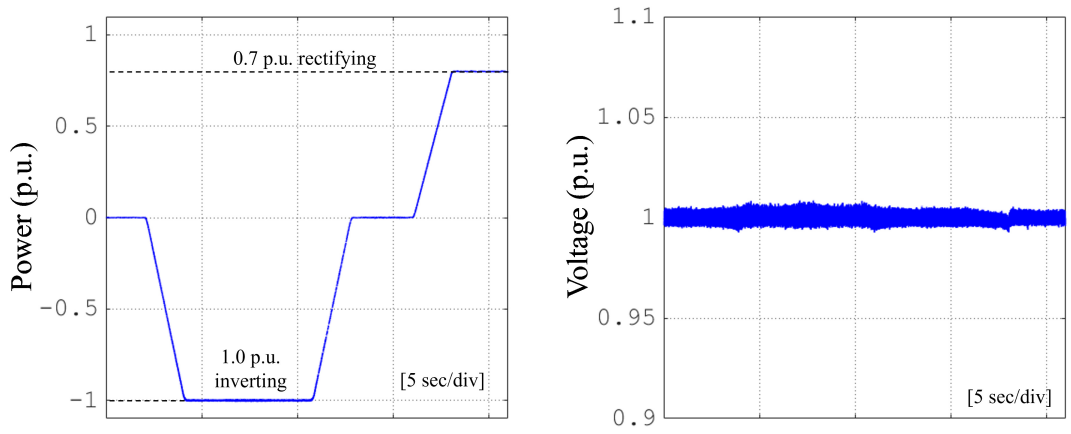

Fig. 4.15: CHiL experimental results across the full power range (-1.0 to 0.7 p.u.): (a) active power and (b) PCC voltage magnitude

4.3.3 Robustness

The stability region presented in Section 4.3 should be robust enough under different SCR or errors in grid impedance uncertainty. This can be tested by reproducing the stability bubble at different SCR. Fig. 4.16 shows the same stability bubble in Fig. 4.11 (at SCR = 1) and the equivalent stable operating regions for SCR = 2 and SCR = 3. The stability bubbles at SCR = 3 and SCR = 2 include all the stable operating points for SCR = 1. The SCR = 1 condition is therefore the limiting state for stability and so analysis at this point is sufficient to ensure stable operation at higher SCR.

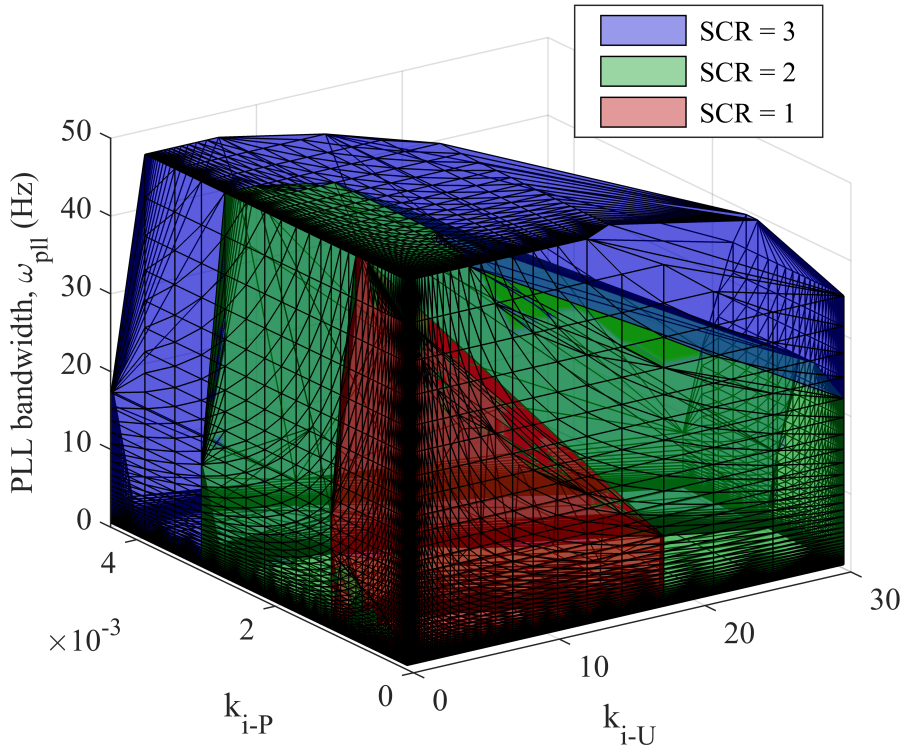

Fig. 4.16: Stable operating region for -1.0 p.u. $< P <$ 0.7 p.u. at SCR = 1, 2 and 3.

4.3.4 Dynamic performance

The results in Section 4.2 suggest that the VCC-VSC can operate stably across a wide range of controller tunings. Indeed, there appear to be regions where large parameter changes have a negligible impact on the system stability limit e.g. Fig. 4.6(a) shows that, at high AVL bandwidth, the ICL bandwidth has minimal impact on the power transfer limit. However, the dynamic performance at these points is very different. The above stability bubble analysis should therefore be extended to consider the operating region where both stability and acceptable transient performance are achieved. Operating regions are defined for which the stability condition in Section 4.3 is met, and where the system step response meets the following requirements:

1. Overshoot $< 20\%$

2. Settling time (within 2% of steady-state value) < 0.75 s

For a unit step in active power demand at the specified power transfer levels (-1.0 p.u. and 0.7 p.u.), Fig. 4.17 shows the outer stability bubble from Fig. 4.11 and an inner dynamic performance bubble. This dynamic performance bubble represents all combinations of PLL, APL and AVL parameters which can achieve between -1.0 and 0.7 p.u. power transfer and at which a unit power step meets the transient performance requirements above; as expected, the operating region for acceptable transient performance is smaller than that for absolute stability.

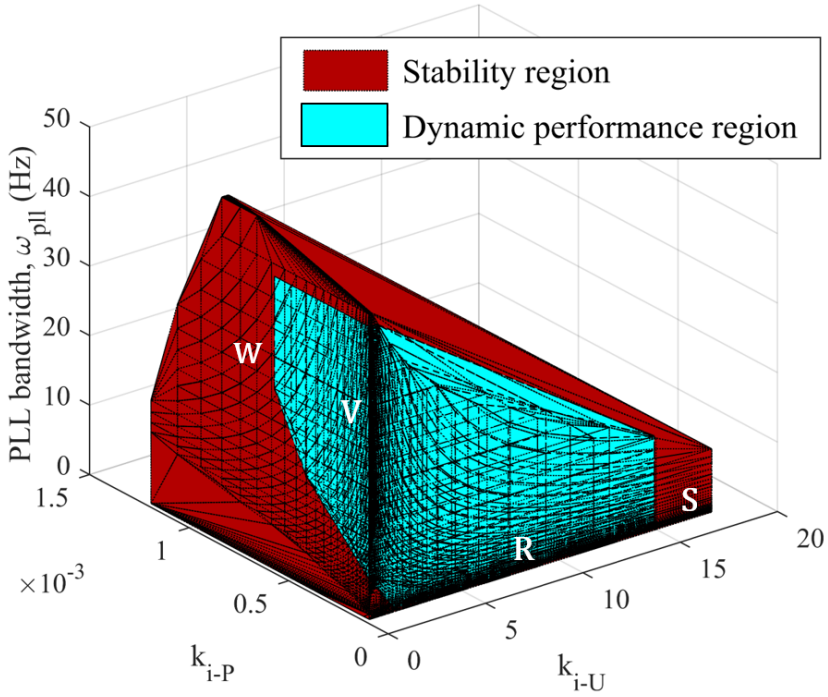

Fig. 4.17: Stable operating region for -1.0 p.u. $< P <$ 0.7 p.u. (red) and acceptable transient performance region (cyan) (a unit step for active power demand).

Fig. 4.18 shows examples of time-domain simulations within this dynamic stability region and within the intermediate region of absolute stability with unacceptable transient performance. The controller parameters at these points are given in Table 4.5 and are marked on Fig. 4.17. This analysis can therefore be used to investigate dynamic performance, and the sensitivity of transient performance to controller tuning, without the requirement for protracted time-domain simulations.

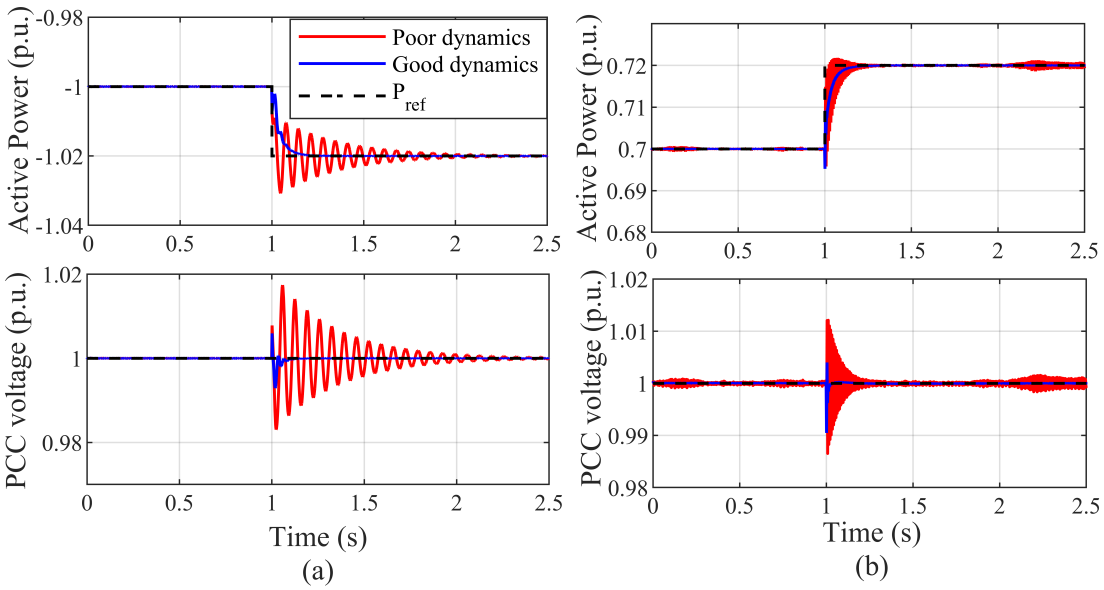

Fig. 4.18: Active power and PCC voltage responses to a 0.02 p.u. power step inside and outside the dynamic performance bubble at (a) points V and W, Fig. 4.17 and at (b) points R and S, Fig. 4.17.

Table 4.5: Controller parameters at small signal stability boundary

Operating point (Fig. 4.17)	Controller parameters	Dynamic performance
V	$\omega_{pll} = 30$ Hz $k_{i-P} = 1 \times 10^{-4}$ $k_{i-U} = 3$	Good
W	$\omega_{pll} = 30$ Hz $k_{i-P} = 6 \times 10^{-4}$ $k_{i-U} = 3$	Poor
R	$\omega_{pll} = 0.5$ Hz $k_{i-P} = 1.3 \times 10^{-4}$ $k_{i-U} = 7$	Good
S	$\omega_{pll} = 0.5$ Hz $k_{i-P} = 1.3 \times 10^{-4}$ $k_{i-U} = 17$	Poor

Once again, this dynamic performance result can be validated using the RTDS setup described in Section 4.3.2. In Fig. 4.19, a 0.1 p.u. step in active power reference is applied at one of the dynamic stability boundaries marked in Fig. 4.17. Though the system remains stable in both cases, there is a significant deterioration in transient response when moving outside of the dynamic performance operating region.

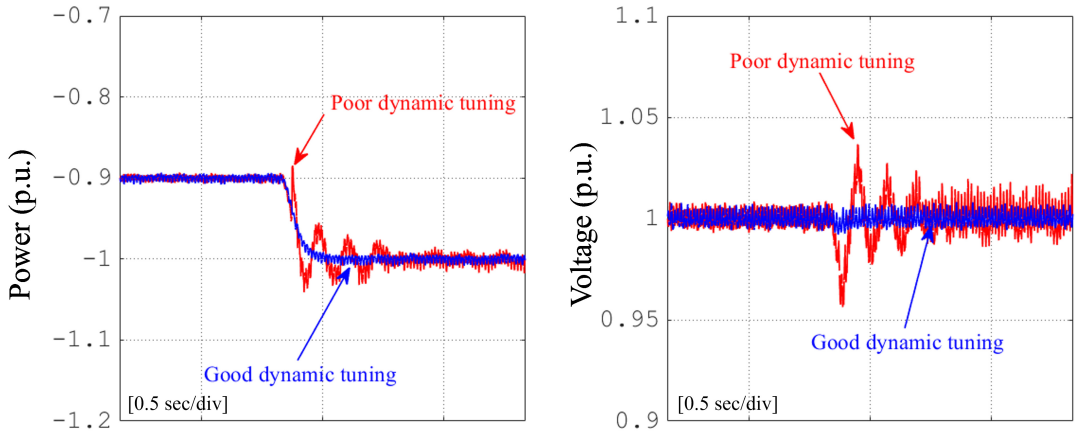

Fig. 4.19: CHiL experimental results of active power and PCC voltage responses to a 0.1 p.u. power step inside and outside the dynamic performance bubble at points V and W, Fig. 4.17

4.4 Summary and Design Recommendations

This chapter has established bidirectional active power transfer limits for classical vector control of VSCs across a broad range of controller operating points. All interactions between inner and outer control loops and the PLL were shown to produce a significant impact on system stability and therefore must not be neglected in favour of a focus on the PLL alone. The controller parameter sweeps performed in this analysis provided an objective evaluation of VCC-based VSC control strategies. The study considered the performance at a wide range of controller bandwidths to inform transient performance and stability insights, rather than studying a single operating point as is considered in existing literature. Observing the effect of controller bandwidth also revealed distinct stable operating regions for the PLL, showing that multiple modes of operation

can be achieved with intelligent tuning of a single VSC control structure. This allows for more widespread implementation of established VCC-VSC technologies in AC grids with fluctuating impedance and variable control requirements. A stable operating region was established for VCC-VSC within which stability can be guaranteed at a given active power transfer level. The validity of operating across this power range was confirmed using CHiL RTDS experiments. The consideration of wider operating points has also shown to be significant for achieving acceptable dynamic performance. The operational envelope for good dynamic performance was smaller than that for absolute stability but still covered a range of controller operating points. Operating at controller gains within this region was shown to achieve rated power transfer in inverting mode and good dynamic performance with no changes to the conventional VCC control structure. Controller interactions and dynamic performance considerations are overlooked by conventional controller analysis at a single operating point, and so this method offered considerably higher objectivity and robustness for evaluation of vector control based VSC. Practical recommendations which arose from this work included the avoidance of intermediate PLL bandwidths (approx. 5 – 30 Hz), which offered poor stability, and the implementation of customized control tunings for inverting and rectifying operation. Care should also be taken to ensure that the PLL and ICL bandwidths are considered when tuning the q-axis outer loop bandwidth. When these interactions were taken into account, conventional VCC was shown to perform much better than is currently assumed and can inject nominal active power to a very weak AC grid with no modifications to the controller structure.

Chapter 5

Comprehensive Stability Analysis of Power-Synchronization Control for VSC-HVDC

Power-synchronization control (PSC) is a promising control strategy to improve the stability and performance of voltage-source converters (VSCs) in very weak AC grids. However, evaluation of PSC to date has investigated performance only at single controller operating points, rather than holistically varying multiple controller gains. In this chapter, small-signal eigenvalue analysis is used to comprehensively analyze PSC-VSC stability. The maximum active power transfer of PSC is established across a broad range of controller tunings and the two-way and three-way couplings between the power-synchronization control, AC voltage control and high-pass current filter gains are quantified. A new stable tuning region is introduced, which represents the controller parameter space for stable operation. The robustness of this operating region to SCR changes is also investigated. The stability boundary and dynamic performance are validated using control hardware-in-the-loop experiments with a real-time digital simulator.

5.1 Study Parameters

Comprehensive assessment of PSC follows a similar framework to the VCC evaluation in Chapter 4, but with alternative tuning parameters to be considered. Once again, two metrics are assessed:

1. The bidirectional active power transfer limits of the converter-controller system as a function of the bandwidth, or gain, of each control loop.

2. The construction of a number of 'stability bubbles' which represent the stable operating space for given active power transfer and dynamic performance requirements.

For PSC, the three controller variables examined are the power synchronization loop (PSL) bandwidth the AC voltage loop (AVL) bandwidth and the high-pass current filter (HPF) gain. Two-way controller interactions and the active power transfer limits are presented in Section 5.2 and stability bubbles for PSC are established in Section 5.3. The AC grid, VSC and power synchronization controller for this study are as presented in Section 3.2. A very weak AC grid with SCR = 1 is used and the AC system parameters are detailed in Table 5.1.The filter capacitor, C_f, is modelled for completeness but can also introduce resonances to the system [44] and so a negligible value of filter capacitance is used for this study.

Table 5.1: AC system parameters

Parameter	Value
AC system rated voltage, RMS line (kV)	195
AC system rated power (MW)	350
AC system frequency (Hz)	50
SCR	1
X/R ratio	10
DC link rated voltage (kV)	200
LPF filter time constant (s)	1×10^{-4}
AC system inductance, L_g (H)	0.3441
AC system resistance, R_g (Ω)	10.86
Filter/transformer inductance, L_c (H)	0.0692
Filter/transformer resistance, R_c (Ω)	1.0864
Filter capacitance, C_f (μF)	0

5.2 Two-way Controller Interactions

The PSL and AVL controller bandwidths and the HPF gain are varied simultaneously and at each operating point, the maximum active power (measured at the PCC) that can be exchanged between the grid and the VSC is calculated in both inverting and rectifying modes. In this MIMO system, there is cross-coupling between the d- and q-axis control and so no single parameter can independently control or define the PSL and AVL controller bandwidths. However, there is a correlation between the integral gains, k_p and k_u, and the PSL and AVL bandwidths, and so these gains are used as substitutes for direct control of the respective bandwidths. The +/- 3dB bandwidth can then be calculated in MATLAB for each channel of the MIMO small-signal model to provide an estimate of the PSL and AVL channel bandwidths. At each unique controller tuning, the maximum active power that can be injected into the grid or the DC link is determined. Eigenvalue analysis has previously been used to assess the impact of only a single variable (one controller tuning or the active power level). The proposed method instead establishes the stability limits as three variables are changed (two controller tunings and the active power). A small signal model is created at

each unique controller operating point and the eigenvalues of each of these models is examined to find the active power transfer limits at that controller tuning. This process is shown in Fig. 5.1 and should be repeated in both inverting and rectifying modes. The input to the process is ranges of k_p, k_u and k_v to be tested (from Table 5.3) and the output is a matrix of the active power transfer limit, P_{lim}, calculated at each set of controller gains.

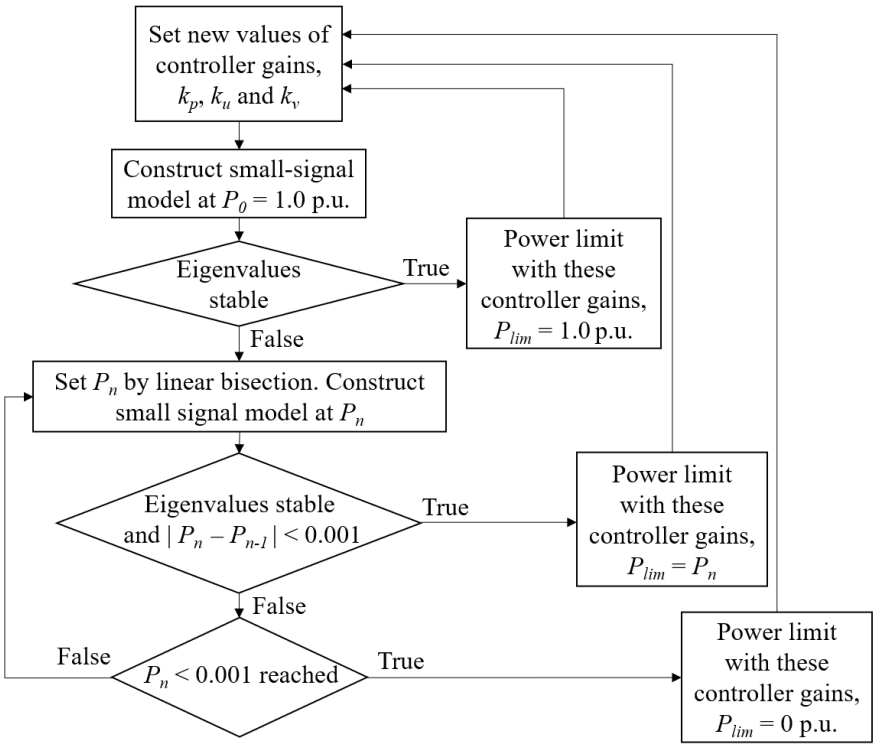

Fig. 5.1: Flowchart of the stability analysis methodology to determine active power limits at a broad range of controller tunings.

To set each new controller tuning, the gains of two control parameters are simultaneously adjusted whilst all other parameters are kept constant. This produces comprehensive active power limits as a function of two controller tunings. This is then repeated for all combinations of any two controller parameters. Values for the controller gains when a given loop is fixed are based on [36] and given in Table 5.2. The gain and approximate controller bandwidth ranges (i.e. the +/- 3dB bandwidth calculated in MATLAB from the respective channel of the MIMO small-signal model) covered when

varying a given loop are given in Table 5.3, where ω_P is the approximate active power controller bandwidth and ω_U is the approximate AC voltage controller bandwidth.

Table 5.2: Default PSC tuning parameters

Control loop	Parameters	Value
PSL	k_p	2.5×10^{-7}
AVL	k_u	50
	k_v	60
HPF	α_v	40 rad/s

Table 5.3: PSC operating point ranges

Control loop	Gain	Parameter range	Equivalent bandwidth range
PSL	k_p	0.5×10^{-7} - 15×10^{-7}	$\omega_P \approx 0.5$ - 100 Hz
AVL	k_u	0.1 - 1000	$\omega_U \approx 0.02$ - 50 Hz
HPF	k_v	0 - 500	-

5.2.1 Discussion

Performing sweeps across the controller tuning ranges in Table 5.3 produces a 3D surface corresponding to the maximum active power transfer that is achievable at a given controller operating point. As discussed, the gains k_p and k_u are used as proxies for ω_P and ω_U, respectively. The parameter gain range for k_p is 0.5 $\times 10^{-7}$ – $\times 10^{-7}$ rad/Ws, which corresponds to $\omega_P \approx 0.5$ – 100 Hz. The parameter gain range for k_u is 0.1 – 1000, which corresponds to $\omega_U \approx 0.02$ – 50 Hz. The surface in Figure 5.2 represents the active power limit with varying PSL and AVL bandwidths. It can be seen that reducing both the PSL and AVL bandwidths increases the active power transfer limit. The result that slowing down the AVL increases stability appears in contrast with [42], which shows that increasing the AVL bandwidth increases the system damping. However, this is likely due to the HPF tuning, which has a significant effect

on the system damping and can 'override' the impact of other loops in this respect. This is explored further in Section 5.2.2. Figure 5.3 shows the active power limit with changing HPF gain and PSL bandwidth and shows that the HPF gain must be within a narrow range (approx. $10 < k_v < 200$ V/A) to maintain system stability. If the HPF is well tuned and the PSL bandwidth is reduced, the active power can reach the limit determined by the converter rating in both inverting and rectifying modes (-1.0 p.u. and 0.95 p.u. respectively). Stability is more sensitive to HPF tuning if the PSL bandwidth is fast. Regions of high power transfer stability exist at both high and low PSL bandwidths, but for intermediate tunings corresponding to approximately 5 Hz $< \omega_P <$ 60 Hz there is a reduction in achievable active power. The active power limit as a function of HPF gain and AVL bandwidth is shown in Figure 5.4. Again, for maximum power transfer, the HPF gain must be within a range $\sim 10 < k_v < 200$ V/A to maximise the stable power limit. Similar to the pattern seen in Figure 6, there is a region of reduced stability at intermediate AVL bandwidths, approximately 5 Hz $< \omega_U <$ 35 Hz. All control loops have a similar qualitative impact in inverting and rectifying modes, but with slightly lower power transfer levels in rectifying mode due to the asymmetry of VSC systems in weak AC grids [76].

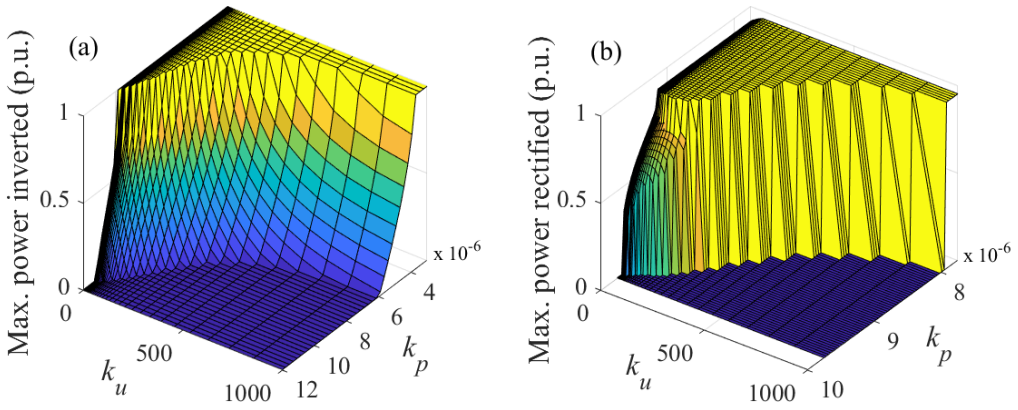

Fig. 5.2: Maximum active power transfer as a function of AVL and PSL bandwidths in (a) inverting mode, and (b) rectifying mode.

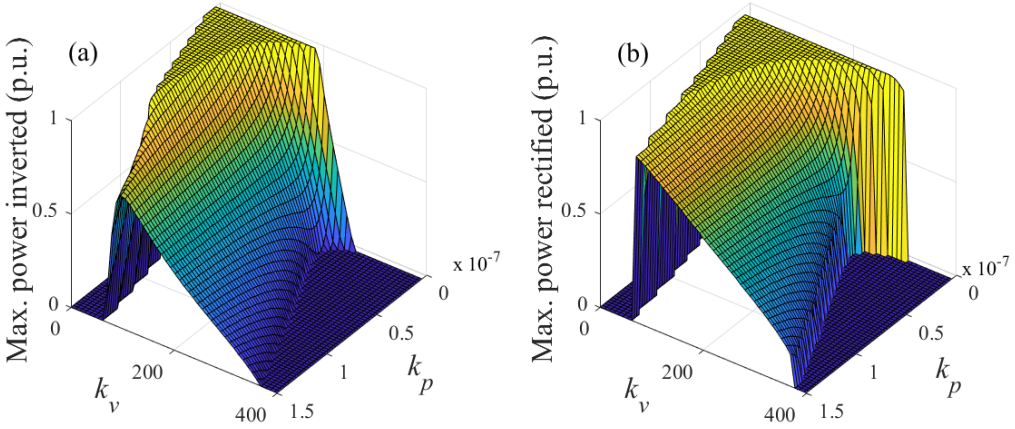

Fig. 5.3: Maximum active power transfer as a function of HPF gain and PSL bandwidth in (a) inverting mode, and (b) rectifying mode.

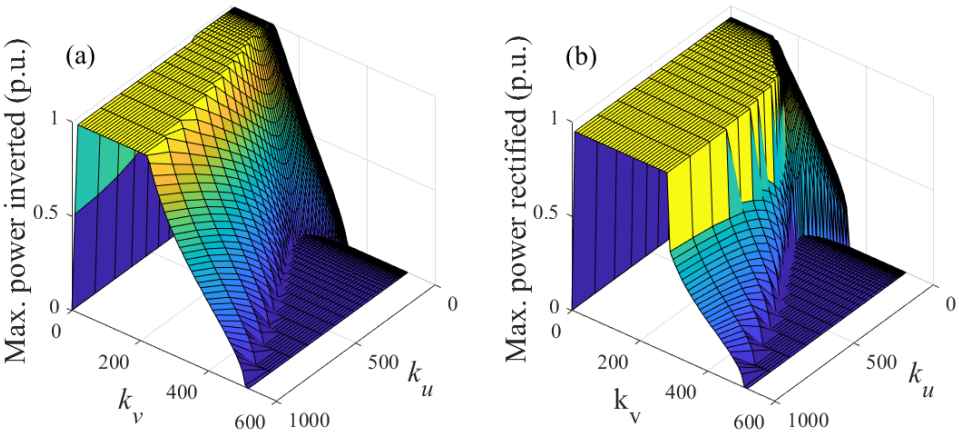

Fig. 5.4: Maximum active power transfer as a function of HPF gain and AVL bandwidth in (a) inverting mode, and (b) rectifying mode.

5.2.2 Effects of individual controller gains

Power Synchronization

As discussed in Section 5.2.1, slowing down the PSL improves stability and therefore increases the maximum active power transfer. However, when the HPF gain is too high, the stable power limit is reduced for 5 Hz $< \omega_P <$ 60 Hz (Fig. 5.3). This suggests that two different modes of operation are possible. When the PSL is very slow, the controller effectively provides a fixed reference angle, thus emulating some

of the behaviors normally associated with grid-forming converter control. With a fast PSL, the controller behaves as expected and provides a varying reference angle that is synchronized to the active power error. However, in general, PSC is limited to slow synchronization speeds for improved robustness, as is discussed further in Section 5.3.

High-pass Current Filter

The HPF has an optimum gain (k_v), which is between 10-200 V/A depending on the values of other controller parameters. This trade-off in gain occurs because, in the closed-loop system, the high-pass filter has a positive damping effect on the grid-frequency resonance (50 Hz) but introduces a lower frequency resonance near the filter cut-off frequency. This lower-frequency resonance becomes more dominant as the filter gain is increased, as shown in the closed-loop power response bode plots at varying k_v in Fig. 5.5 (using a range of $0 < k_v < 150$ V/A, all other gains at the default values in Table 5.2). Fig. 5.3 and Fig. 5.4 also show that the system becomes increasingly sensitive to the HPF gain as the PSL or AVL bandwidths are increased. Therefore, if fast PSL or AVL dynamic performance is required, the HPF must be very carefully tuned. Dynamic performance is explored further in Section 5.3.

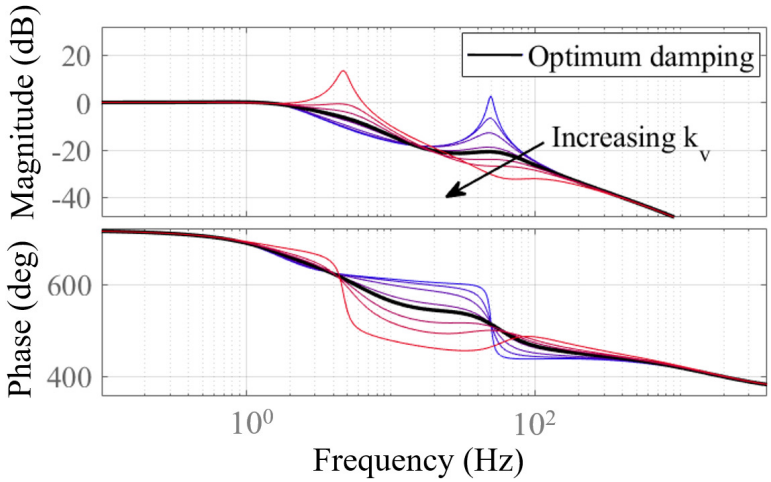

Fig. 5.5: Bode diagram of the closed loop power response with varying HPF gain, $0 < k_v < 150$ (low k_v shown in blue and high k_v shown in red).

AC Voltage Control

Very low and high AVL bandwidths can achieve high active power transfer and system stability. However, as with the PSL, there exists an intermediate range of AVL bandwidths at which the maximum active power transfer is reduced. This is due to the presence of a dominant pole pair, which moves towards the RHP and back again as AVL bandwidth increases. This destabilizing pole pair movement is shown in the pole map of the controlled system in 5.6.

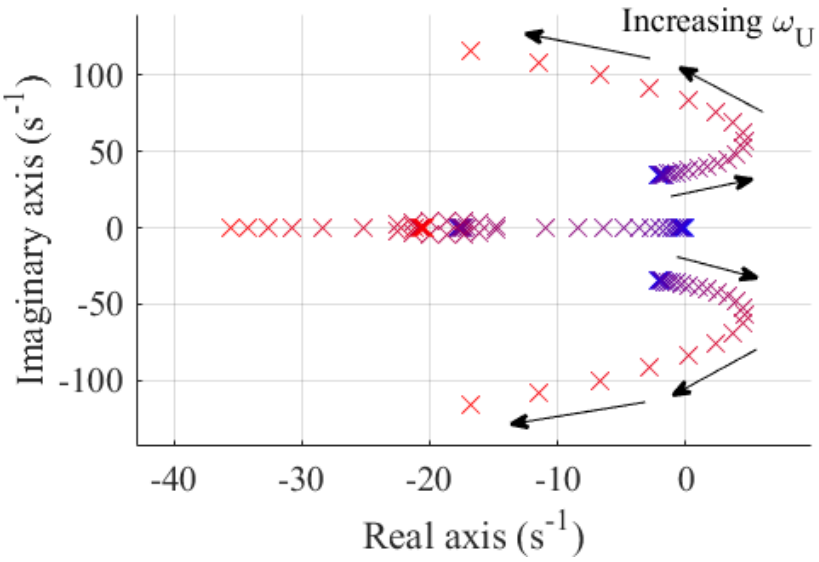

Fig. 5.6: Pole map of controlled system with varying AVL gain, $0.1 < k_u < 1000$ (low k_u shown in blue and high k_u shown in red).

5.3 Stable Operating Region and CHiL Validation

Assessing stability over a broad controller operating region as described in Section 5.2 gives a much more detailed view of system stability and controller interactions than the single controller operating point analyses that have been performed for PSC so far. As was demonstrated with VCC in Section 4.3, this more comprehensive evaluation can again be used to create a stability bubble of the controller operating points for which stable operation is ensured. For PSC, the suggested definition for this region is:

All operating points at which the system remains stable for $\leq$ ***1.0 p.u.*** *active power transfer into the AC grid (i.e. inverting) and for* $\leq$ ***0.85 p.u.*** *active power transfer into the DC link (i.e. rectifying).*

A rectifying power level of 0.85 p.u. is chosen to correspond to the same over-voltage required for -1.0 p.u. power transfer, which is approximately 1.15 p.u. This stability bubble is described in terms of the PSL and AVL bandwidths and the HPF gain and is shown in Fig. 5.7.

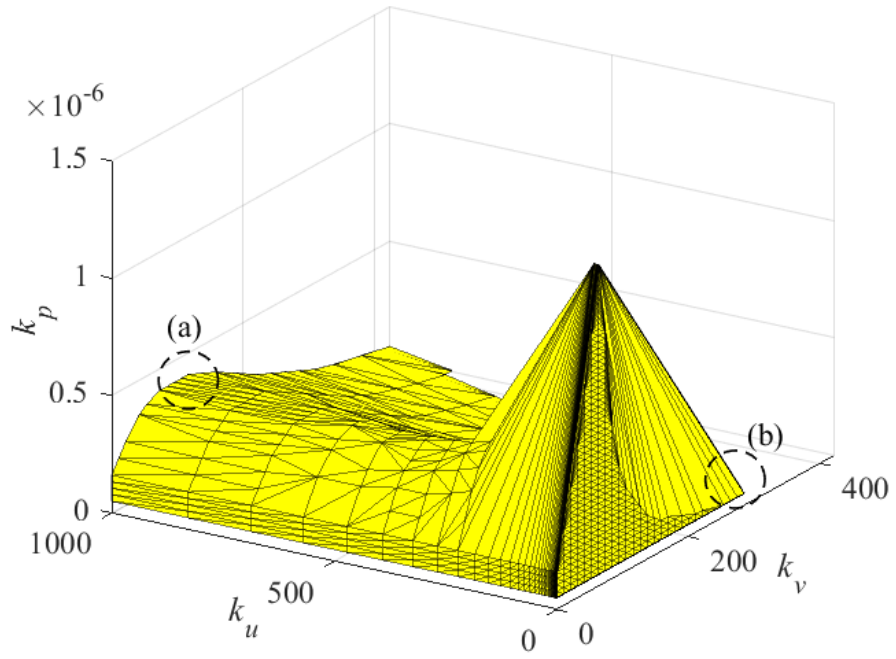

Fig. 5.7: Stable operating region for -1.0 $< P <$ 0.85 p.u. in SCR = 1 AC grid. Boundary points (a) and (b) marked for CHiL validation.

In order to validate the location of this stability boundary, CHiL experiments are performed using the same RTDS and microcontroller setup as was introduced in Section 4.3 of Chapter 4. The microcontroller is a TI C2000 Real-Time controller which is interfaced to the RTDS with the same inputs and outputs as would be received from the grid. The system is again programmed via RSCAD and Simulink/C++ and the schematic of CHiL connections and signal routings is reproduced in Fig. 5.8. The

time step of the RTDS, $T_{s,plant}$, is 3.2 μs and the microcontrollers use a control time step, $T_{s,control}$, of 10 μs (equivalent to a 10 kHz switching frequency). To validate the stability boundary presented in Fig. 5.7, the controller tunings are perturbed at two controller operating points near to the stability boundary. The system is pushed from within the boundary (stable) to just outside the boundary (unstable). The three-phase PCC voltage and converter current waveforms for this experimental validation are shown in Fig. 5.9. Fig. 5.9(a) shows the instability produced in the PCC voltage and converter current when the PSL gain is increased (at operating point (a) on Fig. 5.7), and Fig. 5.9(b) shows the instability produced in the PCC voltage and converter current when the PSL gain is increased (at operating point (b) on Fig. 5.7). Table 5.4 gives the controller tunings at these validation points.

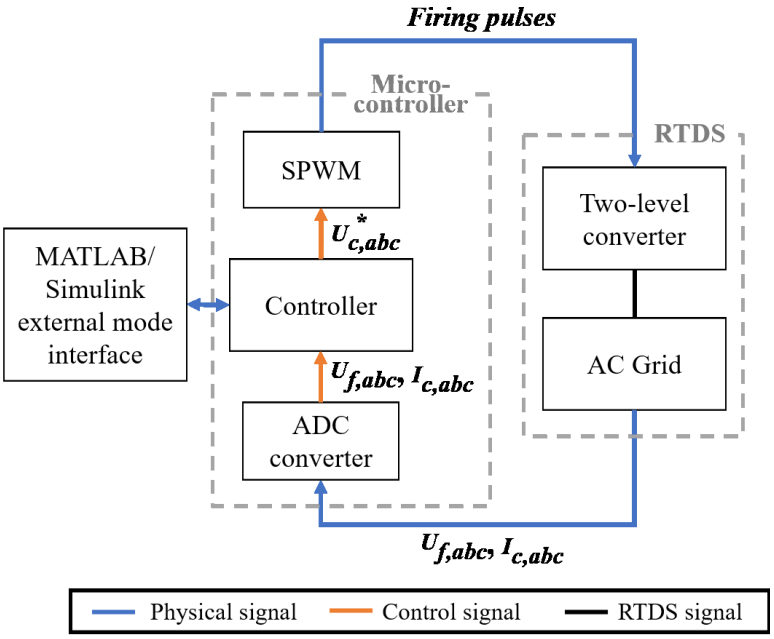

Fig. 5.8: Schematic of the CHiL setup and signal routing between the microcontroller and RTDS.

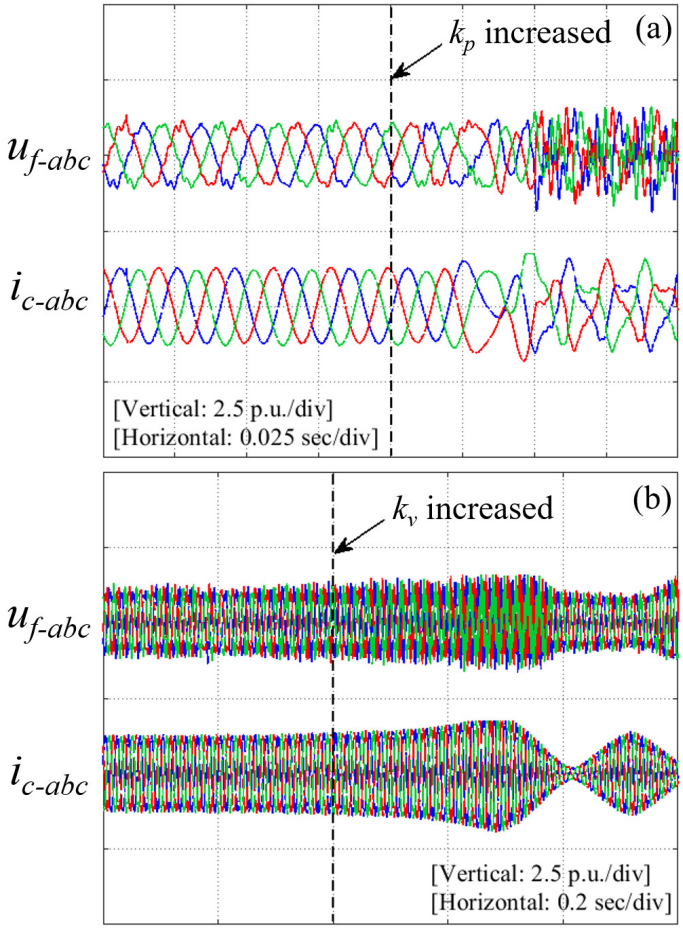

Fig. 5.9: CHiL experimental results within (blue) and outside (red) the stable tuning region at points (a) and (b) marked on Fig. 5.7

Table 5.4: Controller parameters at small signal stability boundary

Corner point	Parameters within boundary (stable)	Parameters outside boundary (unstable)
(a)	$k_p = 4.5 \times 10^{-7}$ $k_v = 400$ $k_u = 1000$	$k_p = 4.5 \times 10^{-7}$ $k_v = 450$ $k_u = 1000$
(b)	$k_p = 13 \times 10^{-7}$ $k_v = 64$ $k_u = 1$	$k_p = 13.5 \times 10^{-7}$ $k_v = 64$ $k_u = 1$

As seen in Section 5.2, stability is strongly dependent on correct tuning of the high-pass current filter. Choosing an appropriate value of k_v allows a much faster PSL to be employed. This speeds up the controller response but leads to a very large overshoot if the PSL is too fast. This effect can be seen in the power step responses at different values of k_p in Fig. 5.10. The non-minimum phase behavior of the system is also exacerbated as k_p is increased, as shown in the inset of Fig. 5.10. Dynamic performance considerations, which limit the value of k_p, are explored further later in this section.

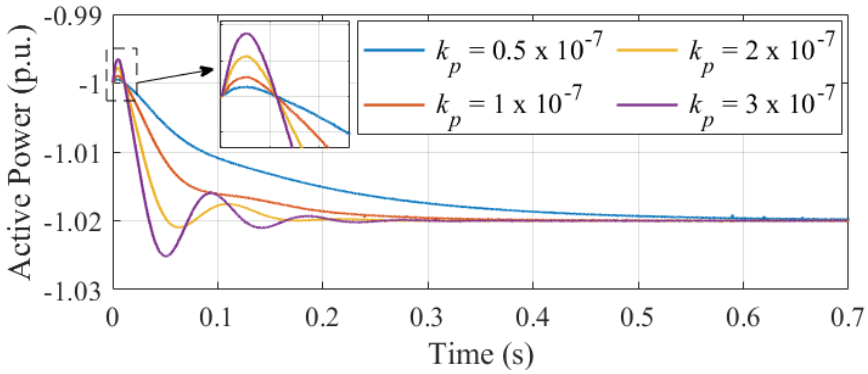

Fig. 5.10: Active power response to a 0.02 p.u. step at P = -1.0 p.u., $k_v = 65$, $k_u = 50$ and varying k_p.

For different systems and power transfer requirements, the stable tuning region must be modified. If the converter voltage and apparent power are allowed to reach overrated limits of 1.2 p.u. and 1.35 p.u., respectively, then up to 0.95 p.u. rectifying power can be achieved. The stable tuning region for this higher power level is shown in Figure 5.11. Points within this region are all combinations of PSL, AVL and HPF tunings which remain stable between -1.0 p.u. and 0.95 p.u. active power transfer. As expected, the stable operating region is reduced when the power level is increased. Regardless of the control method employed, the power transfer of VSCs in rectifying mode in an very weak grid is ultimately limited by the reactive power requirement. Breaching this limit requires additional reactive compensator hardware, which is beyond the scope of this work.

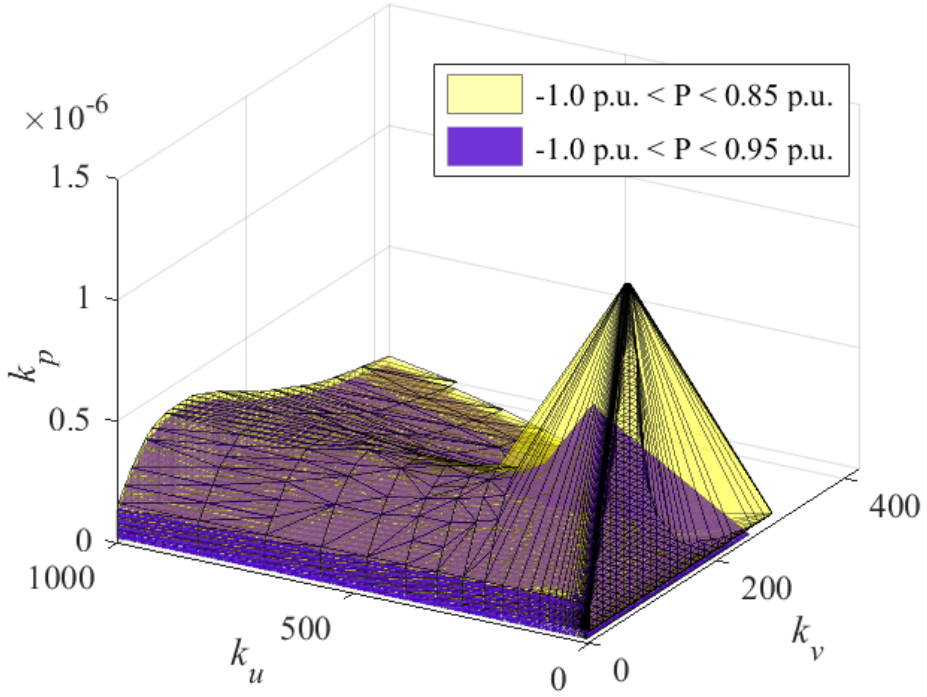

Fig. 5.11: Stable operating region for -1.0 p.u. $< P <$ 0.85 p.u. (yellow) and -1.0 p.u. $< P <$ 0.95 p.u. (purple).

Robustness

The robustness of the stability bubble under different SCRs, or errors in grid parameter estimation, should also be considered. This can be tested by reproducing the stability bubble in Fig. 5.7 at different SCR. Fig. 5.12 shows the equivalent stable operating regions for SCR = 1, 2 and 3. These stability bubbles have a significant region of overlap but, critically, none is perfectly coincident or contains all the stable operating points of another grid setting. This implies that PSC tuning is strongly dependent on the grid conditions and this tuning may need to be refined for both increases and decreases in grid impedance.

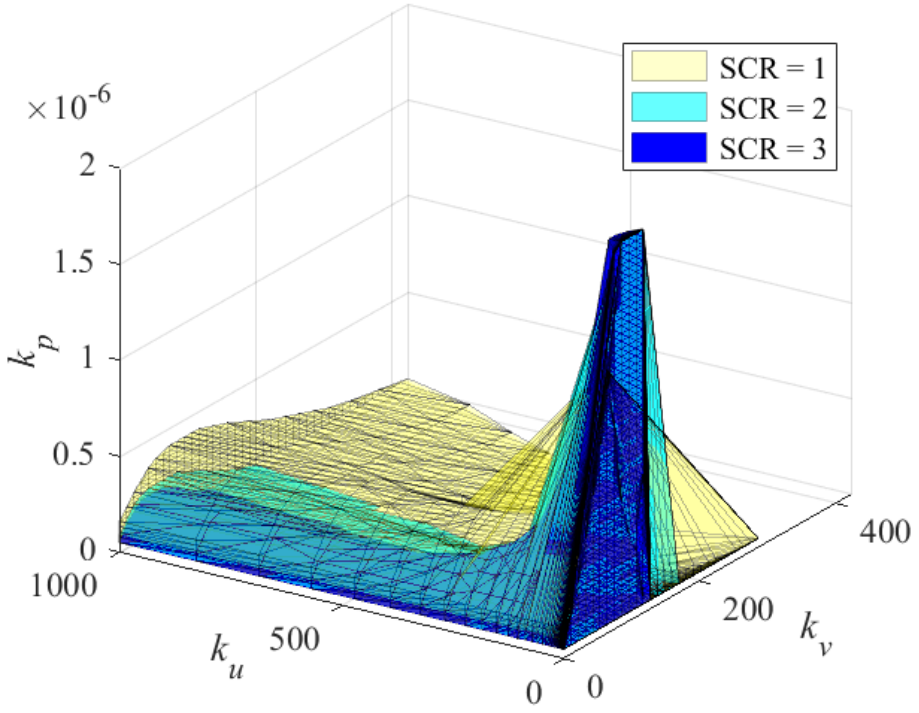

Fig. 5.12: Stable operating region for -1.0 p.u. $< P <$ 0.85 p.u. at SCR = 1, 2 and 3.

Increasing the SCR increases the range of stable PSL bandwidths but decreases the overall stable operating space. Physically, this is due to the very fast changes in voltage that occur in strong grids. PSC is an inherently slow control strategy and so cannot synchronize fast enough with these quick voltage fluctuations. This also explains why the stable operating space at higher SCR is concentrated towards larger values of k_p (and thus faster power synchronization controller bandwidths) in Fig. 5.12. At higher SCR, the system is also more sensitive to the HPF tuning, with gains above $k_v \approx$ 150 causing significant destabilization. This shift of the stable operating space as grid impedance varies is a potential drawback to PSC as it is susceptible to instability if the grid conditions have not been accurately quantified and incorrect controller tunings chosen. In weak AC grids, very small changes in impedance result in a large difference in voltage angle and so small errors in parameter estimation have a significant impact on the system operating point. This parameter uncertainty must be taken into account if employing PSC in areas of changing or uncertain grid strength given the demonstrated

tuning sensitivity. However, if tuned correctly, there is an adequate operating region for which PSC remains stable for all SCR 1 to 3. This region is shown in Fig. 5.13.

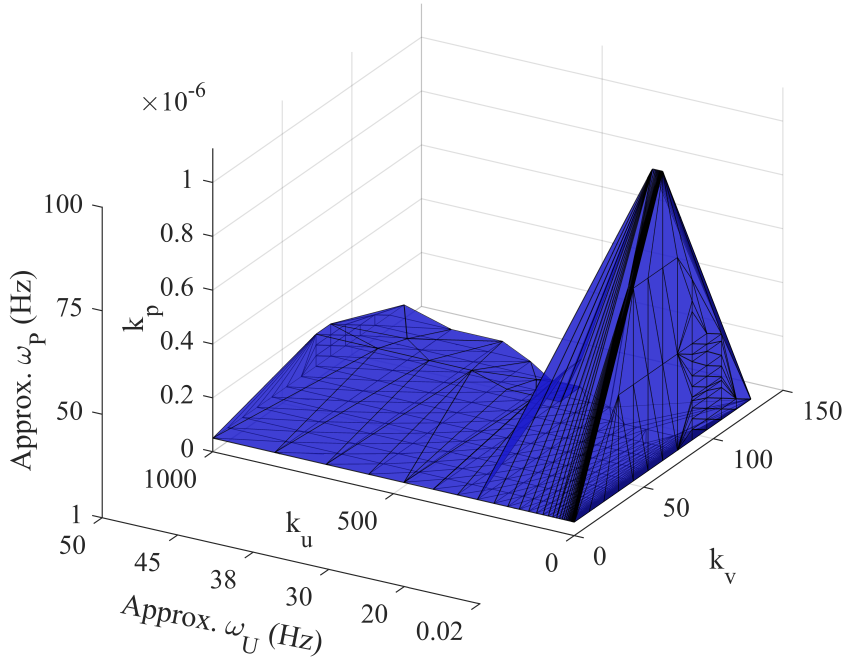

Fig. 5.13: Stable operating region for -1.0 p.u. $< P <$ 0.85 p.u. at all SCRs from 1 to 3.

Dynamic performance

The parameter sweeps in Section 5.2 and the stable tuning regions in Section 5.3 demonstrate that the PSC-VSC can maintain stability when tuned to a number of controller operating points. However, the analysis so far does not consider the differences in transient performance at each of the tunings within the stable parameter space. A second analysis, which considers the controller operating region for stability and good transient performance, should therefore be performed. New stable tuning regions are defined which meet the criteria used in Section 5.3 to form Fig. 5.7, but within which the response to a unit active power step meets certain dynamic requirements. Two levels of transient performance conditions are imposed on the overshoot (OS) and the 2% settling time (ST):

1. 'Moderate': Overshoot $< 20\%$, settling time (within 2% of steady-state value) < 0.75 s
2. 'Good': Overshoot $< 10\%$, settling time (within 2% of steady-state value) < 0.50s

At the active power transfer levels - 1.0 p.u. and 0.85 p.u., an active power step change is applied to small-signal models across the controller parameter space. Fig. 5.14 shows the Fig. 5.7 stable region and two dynamic performance regions with each of these 'moderate' and 'good' transient requirements imposed. All PSC tunings which maintain system stability between the power limits -1.0 and 0.85 p.u. and meet the above dynamic performance requirements for a unit step change to the power reference are contained in these inner dynamic performance regions. The stable tuning regions for 'moderate' and 'good' transient performance comprise a more limited range of controller operating points than for simple stability, as would be intuitively predicted. Fig. 5.15 shows time domain simulations at points within each of the stability regions in Fig. 5.14. Controller tunings at each of these validation points are shown in Table 5.5.

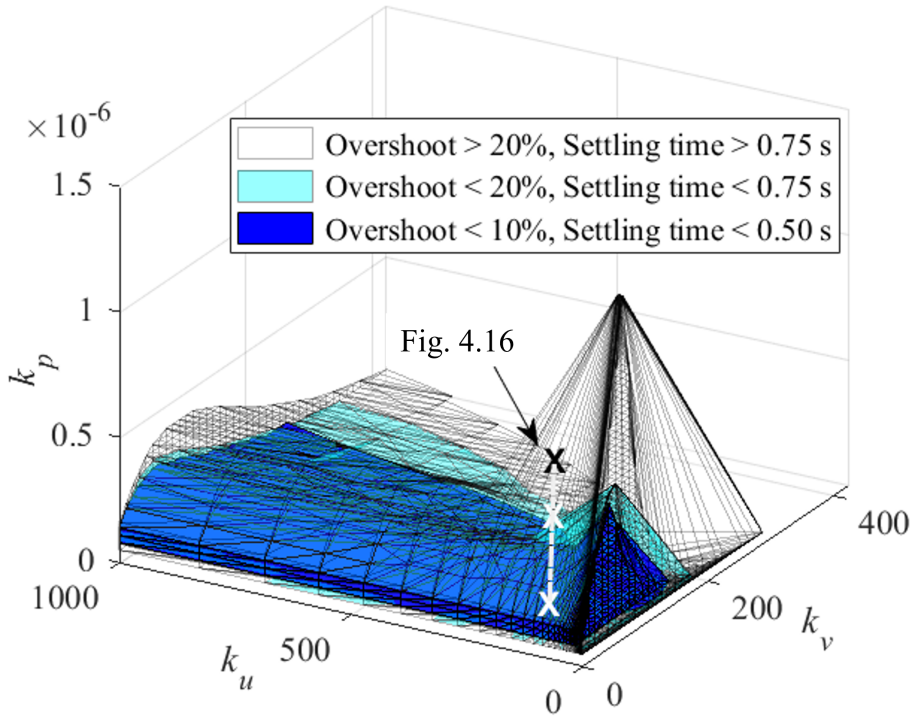

Fig. 5.14: Stable operating region for -1.0 p.u. $< P <$ 0.85 p.u. (white), 'moderate' transient performance region (cyan) and 'good' transient performance region (blue) for a unit step for active power demand.

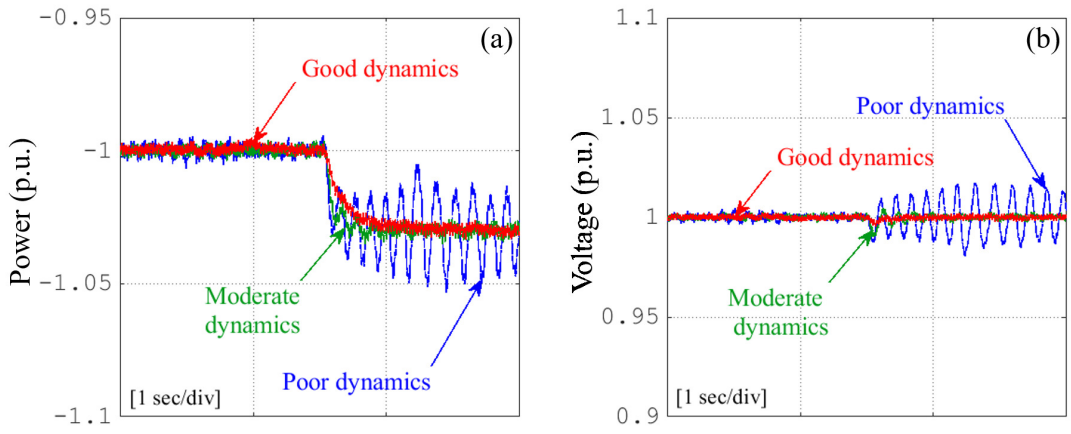

Fig. 5.15: CHiL experimental results for dynamic performance validation: response of (a) converter active power and (b) PCC voltage to a step change in power demand at points marked 'X' on Fig. 5.14

Table 5.5: Controller parameters at dynamic performance points

Operating point	Controller parameters	Dynamic performance
(a)	$k_p = 1 \times 10^{-7}$, $k_v = 50$, $k_u = 1000$	Good
	$k_p = 4.5 \times 6^{-7}$, $k_v = 50$, $k_u = 1000$	Moderate
	$k_p = 9 \times 10^{-7}$, $k_v = 50$, $k_u = 1000$	Poor
(b)	$k_p = 4.5 \times 10^{-7}$, $k_v = 100$, $k_u = 1000$	Good
	$k_p = 0.5 \times 10^{-7}$, $k_v = 300$, $k_u = 1000$	Moderate
	$k_p = 0.5 \times 10^{-7}$, $k_v = 400$, $k_u = 1000$	Poor

The difference in dynamic performance produced by operating in each layer of the stable tuning regions can be clearly seen in Fig. 5.14. This method therefore provides a much faster way of assessing dynamic performance than computationally expensive time-domain simulations. Taking dynamic performance into account primarily reduces the acceptable range of PSL gains. This is due to the large overshoot that is caused by a very fast PSL, as was demonstrated in the step change responses in Fig. 5.10. PSC is therefore limited in the feasible synchronization and power response speeds it can provide. This also limits the possible applications of PSC because it will not be suitable in strong grids where voltage fluctuations are fast and thus a fast controller is essential. These dynamic performance criteria can also be applied to the higher power stable tuning region in Fig. 5.11. However, no controller operating points were found which could meet either the 'moderate' or 'good' transient behaviour limitations at 0.95 p.u. rectifying power level.

5.4 Summary and Design Recommendations

In this chapter, a comprehensive evaluation of power-synchronization control has been performed at a more complete scope of controller operating points than previous works (which generally consider only one operating point). The achievable active power transfer limits in both inverting and rectifying mode have been established across this range

and the stable operating region has been quantified. The coupled impacts of the power synchronization loop, AC control loop and high-pass current filter gains have been assessed, revealing that the high-pass filter has the potential to increase the stable operating space if correctly tuned and that tuning of this gain is increasingly critical as the PSL or AVL bandwidths increase. The boundary of this stable operating space was validated with CHiL RTDS experiments. PSC was relatively robust to overestimations of the system SCR (i.e. underestimate of grid impedance) but less so to underestimations of SCR. Correct tuning of the HPF is critical to improve the robustness of PSC and overall PSC performance is better in weak AC grids than strong grids. Analysis across the whole stable tuning region has revealed a smaller operational envelope, which also provides good dynamic performance. This region has an upper limit on the PSL gain due to the large overshoot caused by a fast PSL. If the converter is overrated, a stable operating region exists such that transfer of 1.0 p.u. active power in inverting mode and 0.95 p.u. power in rectifying mode is possible. However, the dynamic performance at this very high rectifying power level was shown to be poor. The tuning recommendations arising from this work were that the HPF gain must be kept within a fairly narrow band, i.e. $10 < k_v < 200\text{V/A}$. This tuning was critical in stronger grids and with a fast PSL or AVL. In general, slowing down the PSL and AVL increased stability and achievable active power transfer.

Chapter 6

Novel Standardized Controller Assessment Framework

In this chapter, a linearised, comprehensive stability assessment framework is proposed for evaluating the stability limits, robustness and dynamic performance of any voltage-source converter control structure in very weak AC grids. This follows on from the assessments of vector current control and power synchronization control, but expands the assessment to be applicable to any weak-grid connected VSC-HVDC controller at any stage of design and implementation.

6.1 Framework Overview

The wide range of grid-following and grid-forming controllers proposed for weak AC grid-connected VSCs can have very different configurations, including different synchronization methods, cascaded structures and choice of high-level control variables (e.g. reactive power versus AC voltage control). Because of this variety, assessment of VSC control strategies has never been standardized or formalized in academic studies. Each controller designer has generally chosen their own evaluation methods and metrics when researching new controllers, performing a varying set of reference step changes or fault conditions to the proposed controller at only a single operating point. This inconsistent approach has meant that a fair, objective comparison between VSC con-

trol strategies has so far been impractical in the context of academic research. Power network operators do not have the tools to make an informed choice to select the best control strategy for their system parameters and performance requirements. In addition, power grid-connected converter designers without access to restricted industry tools cannot fairly evaluate their work against the current industry standard or quantify the full strengths and weaknesses of a given strategy. This chapter presents a novel standardized assessment framework for all VSC controllers. The evaluation procedure can be applied to analytical converter-controller models at the design stage or to real grid-connected converters already implemented in operation. Three stages of assessment are used to evaluate: 1) the effect of controller tunings and bandwidths across a broad range of operating points, 2) the controller performance in the time-domain and 3) the controller stability in the frequency-domain. Multiple paths through the framework are provided to accommodate designers (with a full knowledge of the analytical equations behind the system) and operators (with unmodifiable, 'black box' systems), alike.

The flowchart of the proposed assessment framework is shown in Fig. 6.1. There are 3 possible paths through the framework, which depend on the objectives of the user. In the case of controller designer, the full analytical model of the controller-under-test is known, and therefore assessment should include a tuning and bandwidth assessment and any frequency-domain analysis can make use of the analytical model. The objective in the designer case is to compare the performance of a novel controller to existing methods or to compare multiple strategies in order to select the most appropriate controller for a given system. However, in the case of a system operator, the controller-under-test is much closer to a 'black box', with the exact structure unknown. The operator may be provided with some controller parameters to modify and tune, but in other instances the converter-controller may be completely hidden such that no tuning changes can be made. The objective in the operator case is to assess the performance of the controller in the grid system for which it is intended, either in the fixed, pre-tuned state or with a tuning and bandwidth assessment included. Whether or not tuning can be performed, any frequency domain analysis in the operator case will require frequency scanning as

the full analytical model remains unknown. In the following sections, the operator case with fixed tuning will be known as case (a), the operator case with modifiable tuning is case (b) and finally the designer case will be known as case (c).

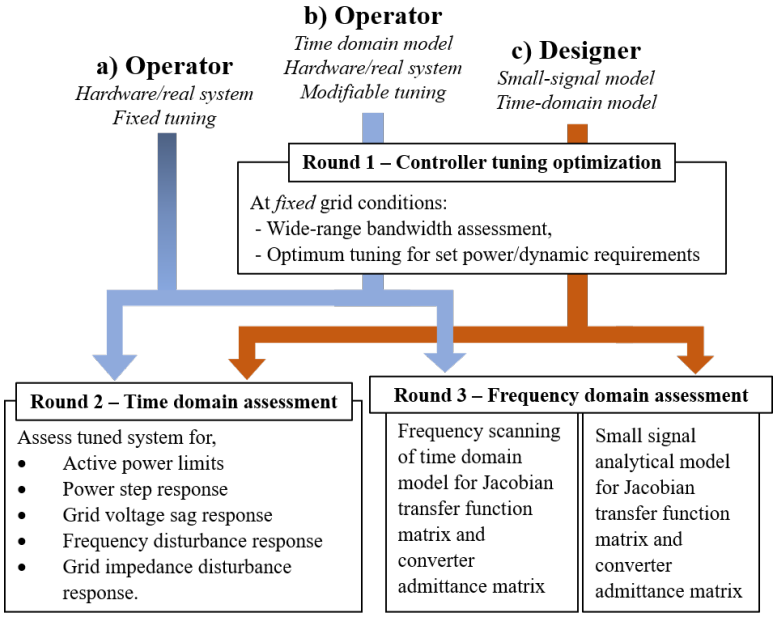

Fig. 6.1: Flowchart of generalised assessment framework for comparison of weak grid-connected VSC control strategies.

6.1.1 Round 1 – Controller tuning optimization

The first stage of the assessment procedure is applied in cases (b) and (c) only, i.e. for operators with an unknown but tunable controller, and for designers. The goal of this stage is to perform an assessment of controller performance across a wide range of controller bandwidths in order to find the optimum tunings as defined by a given set of active power transfer and dynamic performance requirements. This provides the feasible tuning and bandwidth ranges of the controller-under-test that can be implemented to meet the operational requirements. The tuning step is performed by examining stability and dynamic performance at a wide range of controller parameters. This process does not require knowledge of the converter-controller analytical model as the stability and step response data can be gathered from either a 'black box' time-domain model or a small-signal analytical model.

6.1.2 Round 2 – Time-domain assessment

This stage of the framework is applied by operators and designers in all cases. A set of 5 standardized tests are performed in the time-domain on the AC grid-connected converter-controller system. These tests inform the power limits, dynamic performance, robustness and frequency response of the tuned controller, and are detailed in Table 6.1. Grid parameters are held constant in all cases except during test 4, which requires a step change in grid impedance. In all cases, the controller aims to hold the PCC voltage at 1.0 p.u. and the converter current is not limited.

Table 6.1: Time domain assessment test descriptions.

Test	Description	Result(s)/metric(s)
1	Active power reference ramp (-1.0 p.u. to 1.0 p.u) at 0.5 p.u./s	Bidirectional active power limits, tracking errors
2	0.1 p.u. step change in active power reference at P = -0.9 p.u., U = 1.0 p.u.	Settling times, overshoots
3	25% voltage sag at the AC grid (U_g) for 500ms	Settling times, overshoots
4	1.0 p.u. step changes in SCR of AC grid at P = -0.9 p.u. (SCR 1 to SCR 2 to SCR 3)	Stability, overvoltage
5	1 Hz step change in grid frequency at P = -0.9 p.u.	Stability, inertia provided, overvoltage

6.1.3 Round 3 - Frequency-domain assessment

This stage of the framework can also be applied by operators and designers in all cases, but the process of extracting the frequency domain data is case-dependent. In case (a) and (b) where the controller structure is unknown, frequency scanning must be performed to extract the Jacobian transfer function matrix and the converter admittance

matrix. In case (c), the analytical model of the converter-controller is known and so these matrices can be derived directly from the state space or impedance small-signal models.

6.2 Assessment Results for VCC, PSC and VSM Control

The proposed framework can be used to assess any VSC controller. In this section, its flexibility will be demonstrated by evaluating the performance of three common VSC controllers with distinct structures, namely:

1. Standard vector current control (VCC)
2. Power-synchronization control (PSC)
3. Virtual synchronous machine (VSM)

Each controller is modelled in the time-domain (using MATLAB/Simulink) with small-signal analytical models and control hardware-in-loop RTDS experiments. This allows each controller to be treated as if it belongs to any of the three operator/designer cases in the proposed framework. The same AC grid system is used for all controllers under test and is shown in Fig. 6.2. The Thevenin-equivalent AC grid resistance and impedance are R_g and L_g, the AC filter resistance and impedance are Rc and Lc, the converter voltage and current are U_c and I_c, the AC filter bus voltage is U_f, and the grid voltage and current are U_g and I_g. The AC system parameters are given in Table 6.2.

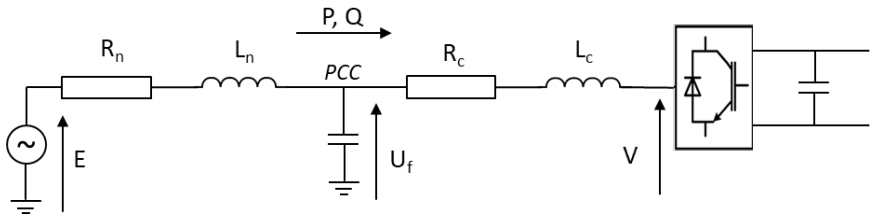

Fig. 6.2: AC Grid-connected converter system under test.

Table 6.2: AC system parameters

Parameter	Value
AC system rated voltage, RMS line (kV)	195
AC system rated power (MW)	350
AC system frequency (Hz)	50
SCR	1
X/R ratio	10
DC link rated voltage (kV)	200
LPF filter time constant (s)	1×10^{-4}
AC system inductance, L_g (H)	0.3441
AC system resistance, R_g (Ω)	10.86
Filter/transformer inductance, L_c (H)	0.0692
Filter/transformer resistance, R_c (Ω)	1.0864

The structure of each controller is shown in Fig.s 6.3, 6.4 and 6.5 respectively. Full details of the derivation of the small-signal model for each controller can be found in Chapter 3.

The VCC strategy is implemented in the dq-frame with outer loop active power, AC voltage control and inner loop current control. This control structure is shown in Fig. 6.3. PI controllers are used for the PLL, active power control, AC voltage control and current control. Their transfer functions are $F_{PLL}(s)$, $F_P(s)$, $F_U(s)$ and $F_I(s)$, respectively, in Fig. 6.3. A fast current loop is generally considered essential for stable VCC and so these gains are held fixed throughout the study. During the tuning assessment in Round 1, the proportional gains of the active power and AC voltage controllers (k_{p-P} and k_{p-U} respectively) are held constant whilst the integral gains (k_{i-P} and k_{i-U} respectively) are varied so as to vary the bandwidth of each loop. The PLL bandwidth is set directly using the proportional and integral gains according to [71]. Remaining gain values that are held fixed are detailed in Table A.1 in the Appendix.

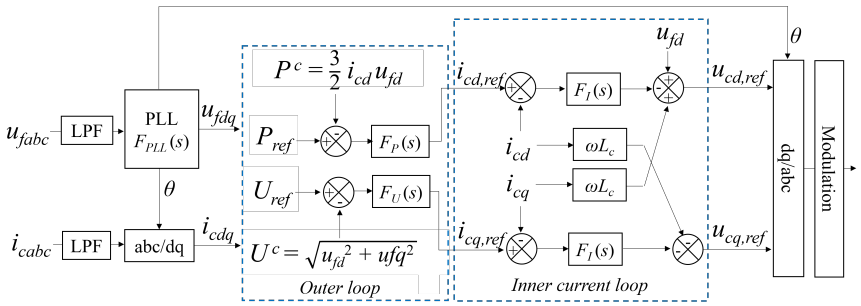

Fig. 6.3: VCC control structure.

The PSC strategy uses first order control of the active power error for synchronization and control of active power. This control structure is shown in Fig. 6.4 and developed in full in [36], where the detailed small-signal model is also given. In fault conditions, a back-up PLL and current controller are employed to limit the converter current. Fault conditions are outside the scope of this work and so, for clarity, these elements are not shown. For the Round 1 tuning optimization, the integral gains k_p and k_u of the power-synchronization and voltage control loops are varied to change the bandwidth of the respective loops. The high-pass filter gain, k_v, is also varied to investigate the effect on stability. The remaining gain values are fixed at the values given in Table A.1 in the Appendix.

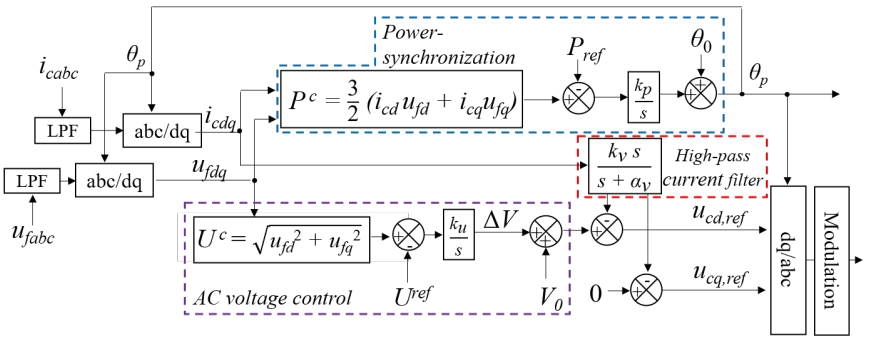

Fig. 6.4: PSC control structure.

A simple VSM controller is employed, implementing the second order swing equation for the active power control and synchronization, and a PI controller for the AC voltage control. This control structure is shown in Fig. 6.5. As with the VCC strategy, the proportional gain (k_{p-Uv}) of the AC voltage gain is held fixed so that variation of the

integral gain (k_{i-Uv}) can be used to control the bandwidth of this loop. Tuning of the PI controller for synchronization and active power control is much more sensitive than the AC voltage control, and so both the proportional and integral gains of the active power control (k_{p-Pv} and k_{i-Pv} respectively) are varied in Round 1 tuning stage.

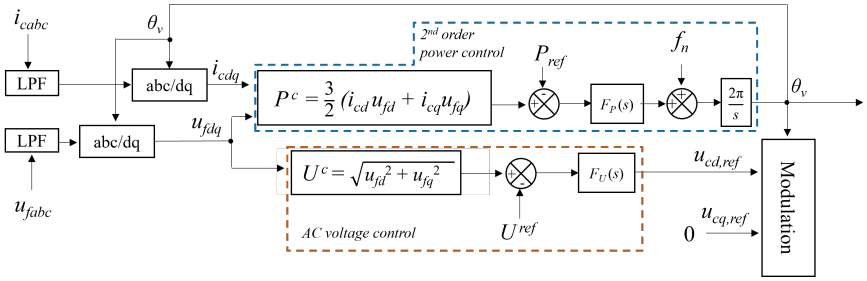

Fig. 6.5: VSM control structure.

6.2.1 Round 1 – Controller tuning optimization

For the demonstration in this chapter, the small-signal models were used to gather Round 1 tuning results for expediency. The goal is to assess the effect of the bandwidth (i.e. the +/- 3 dB bandwidth) of each controller element on stability. However, there is significant cross-coupling between the d- and q-axes in weak AC grid-connected VSC systems, and so the tuning parameters of individual loops cannot usually directly determine the loop bandwidth. Therefore, a set of controller gains are used as proxies for the bandwidth of each control loop. The parameters varied and the ranges covered in this assessment are given in Table 6.3, with an approximate indication of the relevant bandwidth range covered. For each controller, the three associated parameters listed in Table 6.3 are varied simultaneously across the whole range. The small-signal stability and dynamic response to a step change in active power demand at P = -1.0 p.u. and P = 0.89 p.u. (i.e. just below the theoretical limit of an SCR = 1 grid, as calculated in [21]) are measured at each distinct operating point. This produces a 3D volume which represents all the controller tunings that provide stability and a specified level of dynamic performance within these power limits. For this example, stable operating regions are presented which show the controller tuning parameter space that ensures stability and the following minimum requirements of dynamic performance:

1. 2% settling time (ST) $<$ 5 s, overshoot (OS) $<$ 50%

2. 2% settling time (ST) $<$ 1 s, overshoot (OS) $<$ 20%

3. 2% settling time (ST) $<$ 0.5s, overshoot (OS) $<$ 15%

The stability regions representing these points for the VCC, PSC and VSM controllers are shown in Fig. 6.6, Fig. 6.7 and Fig. 6.8, respectively. The optimum tuning for each controller is then calculated as the 'centre of gravity' of the innermost stability bubble (i.e. the centre point of the bubble with the best dynamic performance). These tuning points meet all the stability and dynamic performance requirements and have the greatest stable operating space around them, which provides maximum robustness against tuning errors. These points are also marked on Fig. 6.6, Fig. 6.7 and Fig. 6.8 and detailed in Table 6.4. The optimum tunings constitute the results from Round 1 of the assessment and the controller parameters will be fixed at these values in Rounds 2 and 3. If an alternative tuning procedure is required for a specific application, this can be used in place of Round 1 without affecting the rest of the framework steps.

Table 6.3: Parameter and bandwidth ranges for Round 1 assessment.

	Parameter	Range	Equivalent bandwidth range
	τpll (s/rad)	0.0045 – 0.45	ω_{pll} = 0.5 – 50 Hz
VCC	k_{i-P}	10^{-4} – 10^{-2}	$\omega_P \approx$ 2.5 – 480 Hz
	k_{i-U}	0.03 – 30	$\omega_U \approx$ 0.5 – 230 Hz
	k_p	0.5 x 10^{-7} – 15 x 10^{-7}	$\omega_P \approx$ 0.5 – 100 Hz
PSC	k_u	0.1 – 1000	$\omega_U \approx$ 0.02 – 50 Hz
	k_v	0 – 500	-
	k_{p-Pv}	0.1 – 20	$\omega_P \approx$ 0.1 – 60 Hz
VSM	k_{i-Pv}	0.1 – 4000	$\omega_U \approx$ 0.02 –100 Hz
	k_{i-Uv}	0.01 – 1000	

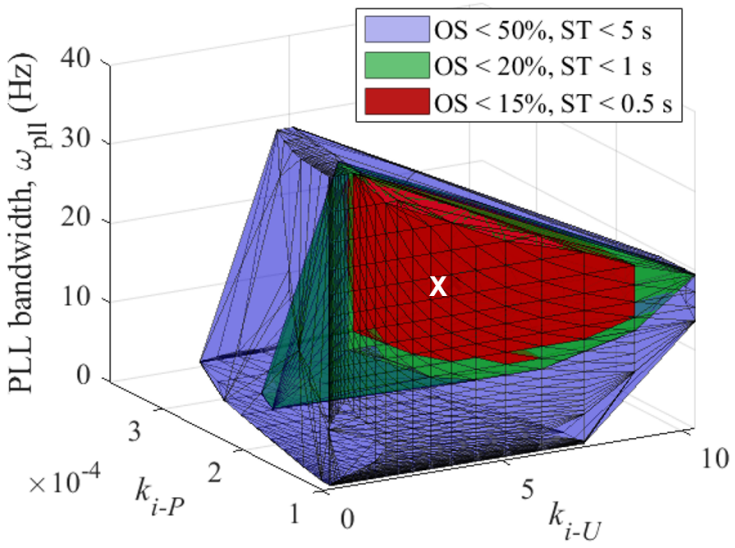

Fig. 6.6: Stability bubbles for VCC with poor dynamic performance (blue), moderate dynamic performance (green) and good dynamic performance (red).

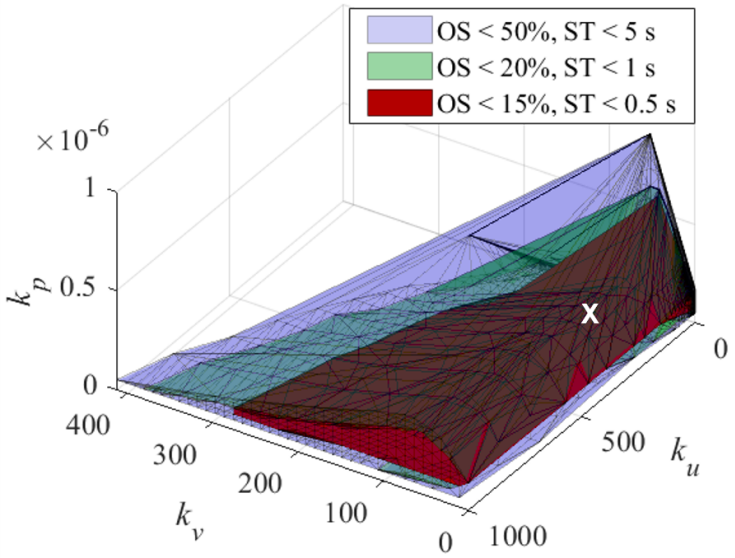

Fig. 6.7: Stability bubbles for PSC with poor dynamic performance (blue), moderate dynamic performance (green) and good dynamic performance (red).

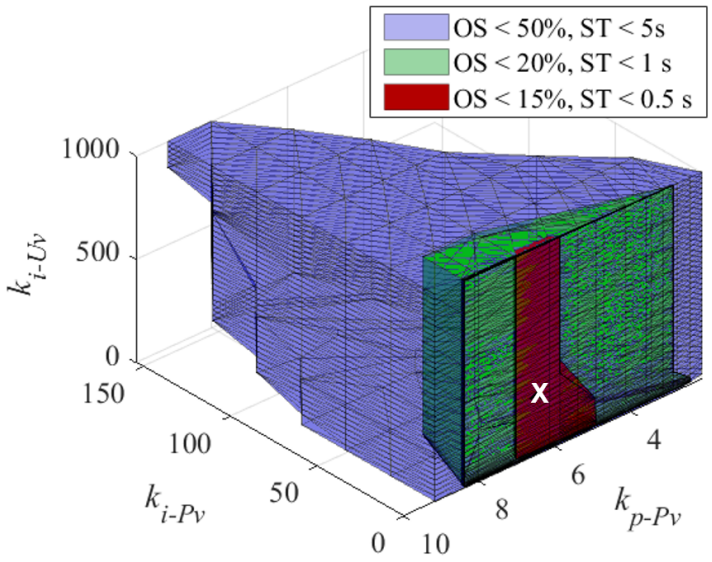

Fig. 6.8: Stability bubbles for VSM with poor dynamic performance (blue), moderate dynamic performance (green) and good dynamic performance (red).

Table 6.4: Round 1 results -optimum controller tunings.

Control	Optimum tuning
VCC	$\omega_{pll} = 22.8$Hz, $k_{i-P} = 1.1\text{x}10^{-4}$, $k_{i-U} = 3.88$
PSC	$k_p = 1.69\text{x}10^{-7}$, $k_u = 394.78$, $k_v = 91.2$
VSM	$k_{i-Uv} = 321.6$, $k_{p-Pv} = 5.880$, $k_{i-Pv} = 0.4826$

6.2.2 Round 2 – Time-domain assessment

The performance of each controller in the time-domain can be analysed using the tests described in Table 6.1. For this demonstration, the results from Round 1 are used to tune each controller and the five time-domain tests are executed using control hardware-in-the-loop (CHiL) RTDS experiments. A Texas Instruments C2000 microcontroller is connected to the RTDS with an identical interface as would be used to connect to the grid, and the system is controlled in RSCAD and Simulink/C++. This stage of assessment can also easily be performed with a simple time-domain simulation, a small-signal model, or the experimental set-up demonstrated here. Pre-tuned controllers can

also be tested at this stage without performing the Round 1 tuning assessment.

Test 1 - Active power ramp

Active power demand ramps at 0.5 p.u./s are applied in both inverting and rectifying mode to determine the power transfer limits of each controller with SCR = 1 and the voltage deviation during the ramp. In inverting mode, the power demand reaches 1.0 p.u. but in rectifying mode the active power ramp stops at 0.80 p.u. so as to stay within the converter rating limits. The CHiL experimental results for this test on each controller are shown in Fig. 6.9 and Fig. 6.10. All three controllers can achieve the theoretical active power transfer limits in both inverting and rectifying modes. The VSM is the slowest controller, but all three controllers have a similar power tracking error throughout the ramp and show good voltage support.

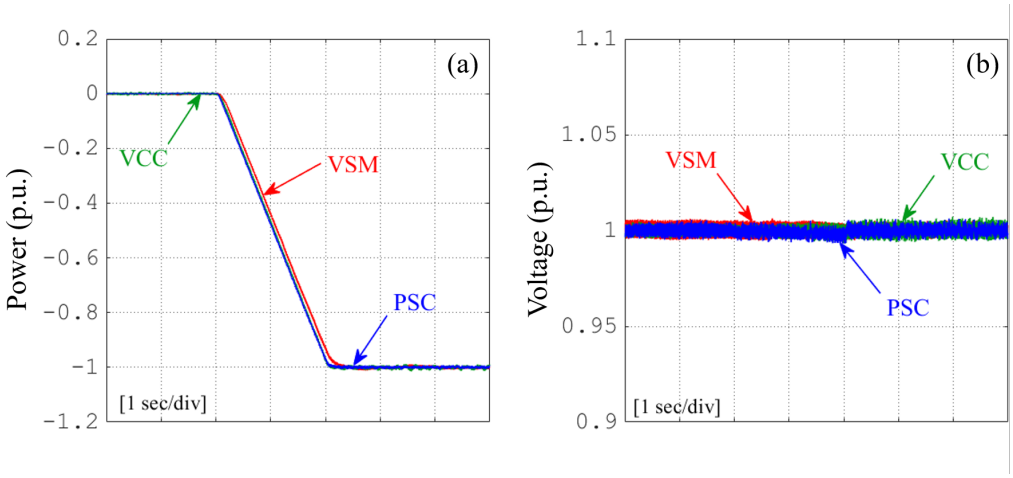

Fig. 6.9: CHiL experimental results with an inverting ramp: (a) active power and (b) PCC voltage magnitude, VCC (green), PSC (blue) and VSM control (red).

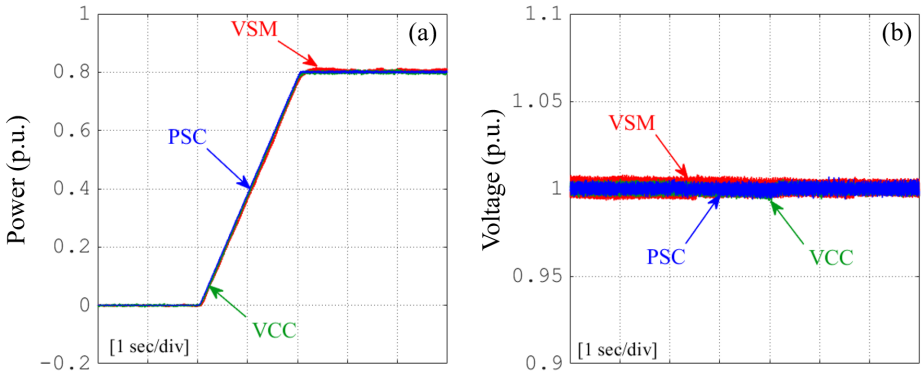

Fig. 6.10: CHiL experimental results with a rectifying ramp: (a) active power and (b) PCC voltage magnitude, VCC (green), PSC (blue) and VSM control (red).

Test 2 - Active power demand step

A step of 0.1 p.u. is applied to the active power reference at P = -0.9 p.u. to reach rated active power injection. The CHiL experimental results for this test are shown in Fig. 6.11. All three controllers show a good dynamic power response, but the VCC and PSC have an obvious voltage undershoot due to stronger coupling between the power reference and the PCC voltage (discussed further in Section 6.2.3). The VSM has a slower response than PSC or VCC, but the voltage support during the power step is excellent. Both VSM and PSC exhibit slight non-minimum phase behaviour in the power response.

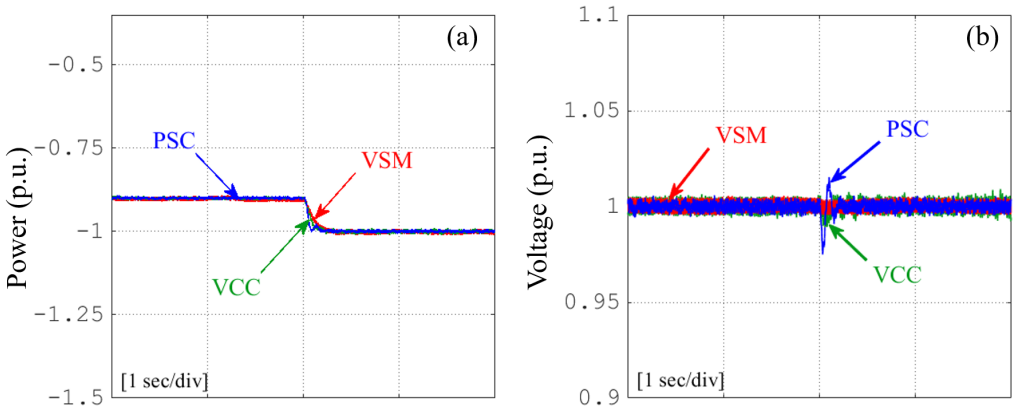

Fig. 6.11: CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a step change of 0.1 p.u. in active power demand at P = -0.9 p.u., U = 1.0 p.u. with VCC (green), PSC (blue) and VSM control (red).

Test 3 - AC grid voltage sag

For this test, a 25% voltage sag, lasting 500 ms, is applied to the grid voltage (U_g). Before the event, the system in inverting 0.9 p.u. active power. The control performance is measured according to the system stability both during the sag event and after it is cleared, and the overall voltage deviation at the PCC. The CHiL experimental results for this test are shown in Fig. 6.12. As expected, the VCC performs best under such sag conditions due to the inherent current limiting capability of the controller. Although the VSM and PSC-controlled systems are able to recover stability and reference power transfer once the sag is cleared, there is an unacceptable power oscillations during the sag event. Under PSC, the PCC voltage is also highly oscillatory during the sag, but the VSM provides much better voltage support. This difference in voltage stability between the two grid-forming controllers is largely influenced by the coupling between power and voltage under PSC. Fig. 6.13 shows the system frequency response from P to U_f with PSC and VSM controllers. The gain margin of PSC is much smaller than that of VSM, indicating stronger coupling between P and U_f and reduced voltage stability when the power is perturbed.

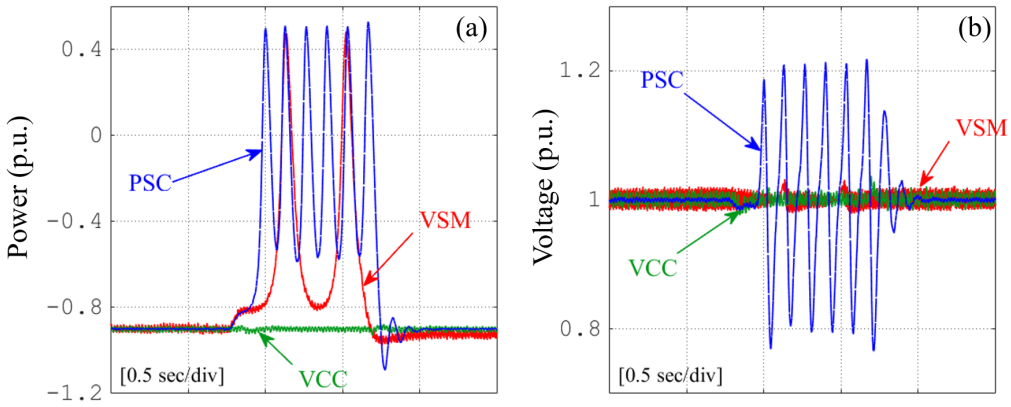

Fig. 6.12: CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a 25% voltage sag in AC grid voltage (U_g) with 500 ms at $P = -0.9$ p.u. for VCC (green), PSC (blue) and VSM control (red).

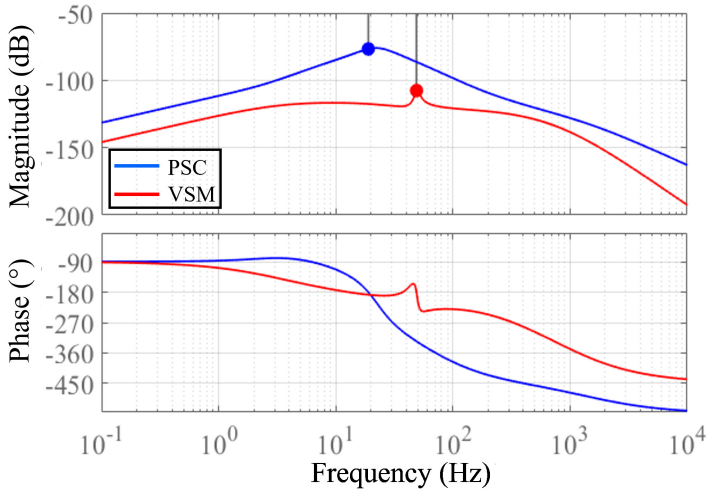

Fig. 6.13: Frequency response from active power, P, to PCC voltage magnitude, U_f , for PSC (blue) and VSM control (red).

Test 4 - Grid impedance step

A step change in grid impedance is performed by opening a breaker on a pair of parallel lines, such that the AC grid changes from SCR = 1 to SCR = 2, is allowed to settle for 5 s, and then changes from SCR = 2 to SCR = 3. The CHiL experimental results for this test are shown in Fig. 6.14. All three control strategies maintain stability and power tracking at the impedance step changes. However, the PSC and VSM show large transitory power oscillations, with a similar maximum power overshoot (the inset of Fig. 6.14(a) shows a close-up view of this power transient with the VSM trace brought to the front of the scope). These temporary power fluctuations could cause instability if there are any errors at all in the parameters used to tune the system. PSC also shows a significant voltage oscillation at each impedance change, which could lead to voltage collapse if any system parameters have not been accurately quantified. After the initial transients, the steady- state performance of VCC and PSC appears unchanged as the grid is strengthened, but the power quality of the VSM deteriorates as the SCR is increased, i.e. the VSM appears to become less stable as the grid strength increases.

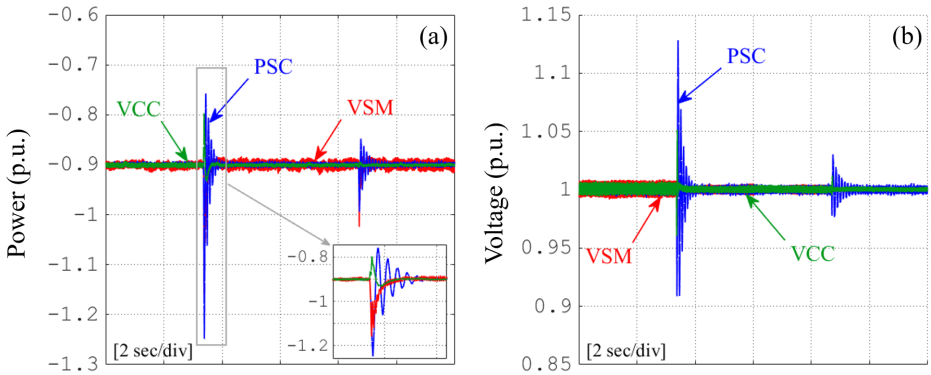

Fig. 6.14: CHiL experimental results: (a) active power and (b) PCC voltage magnitude to step changes in grid SCR from SCR = 1 to SCR = 2 and from SCR = 2 to SCR = 3 with VCC (green), PSC (blue) and VSM control (red).

The decreased stability of VSM at higher grid SCR may be addressed by retuning the controller, but effective control is therefore dependent on regular, accurate impedance estimation. Conversely, for the VCC system, the weakest grid is the limiting condition for tuning the controller, so stability in a SCR = 1 grid is sufficient to ensure

stability at higher SCRs. This is demonstrated by the stable tuning regions for moderate dynamic performance (OS $<$ 20%, ST $<$ 1s, as in Section 6.2.1) at different grid SCRs, shown in Fig. 6.15, Fig. 6.16 and Fig. 6.17. With VCC control, Fig. 6.15 shows that increasing the grid SCR increases the size of the stability region in all directions. The same comparison is made for PSC in Fig. 6.16, which shows that there is a large region of overlap between the stable operating regions at different grid strengths, but none of the regions are perfectly coincident. The overlap region is even smaller for VSM control, as shown in Fig. 6.17. This means that stability must be verified under every possible grid condition if employing PSC or VSM control in a variable grid; no single set of grid parameters can be guaranteed to be the limiting condition. If VCC is employed, tuning only needs to be performed at the weakest possible grid setting.

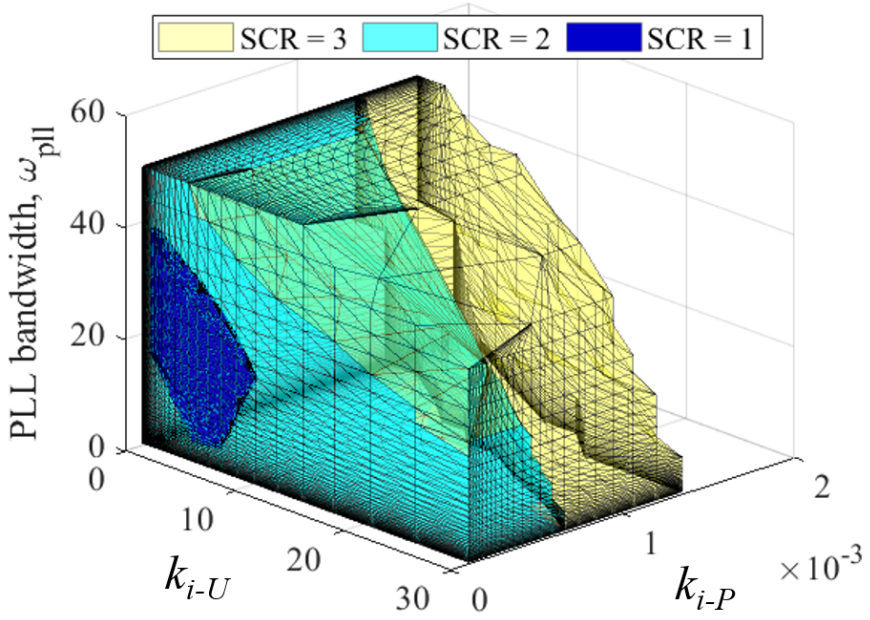

Fig. 6.15: Stable operating region for moderate dynamic performance with VCC at SCR = 3 (yellow), SCR = 2 (cyan) and SCR = 1 (blue).

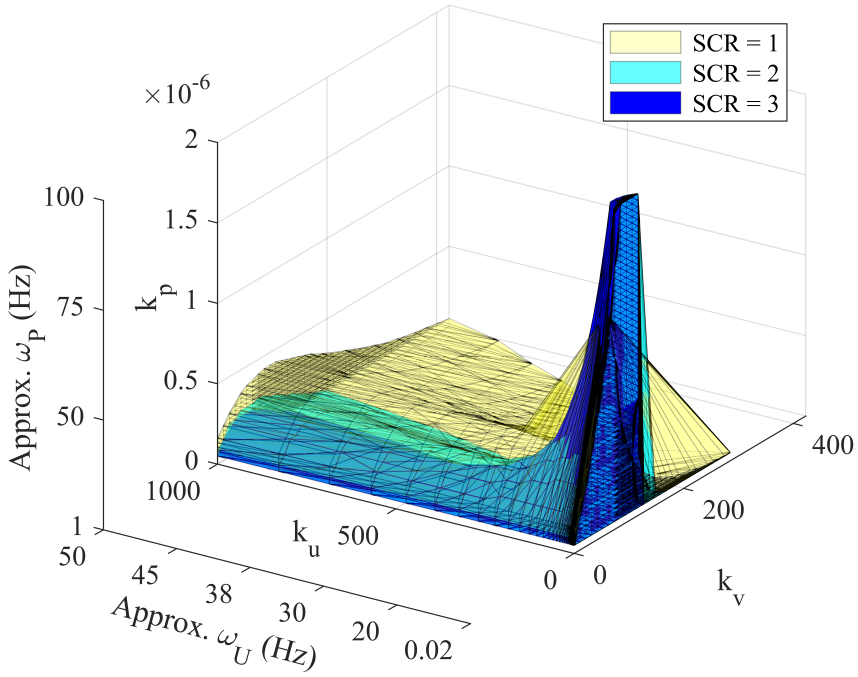

Fig. 6.16: Stable operating region for moderate dynamic performance with PSC at SCR = 3 (yellow), SCR = 2 (cyan) and SCR = 1 (blue).

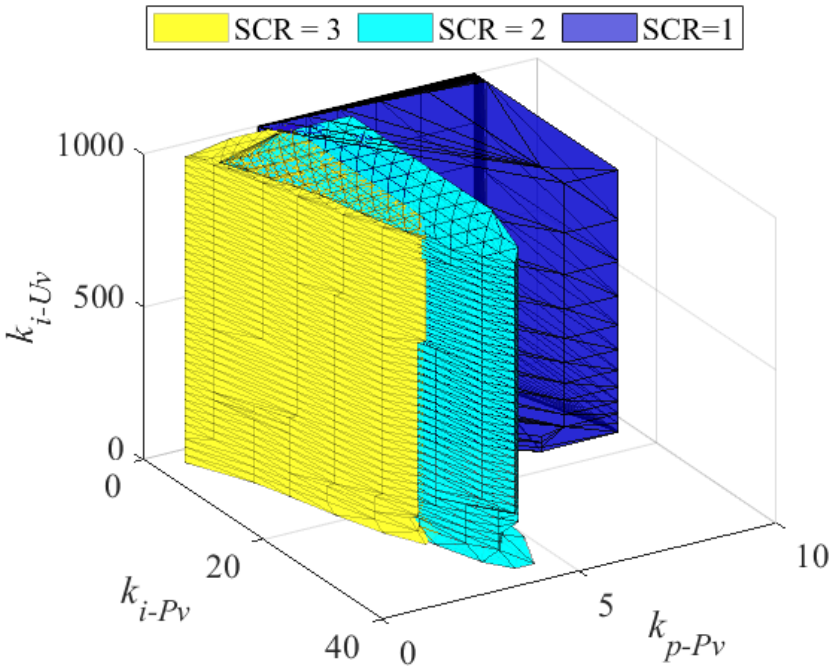

Fig. 6.17: Stable operating region for moderate dynamic performance with VSM control at SCR = 3 (yellow), SCR = 2 (cyan) and SCR = 1 (blue).

Test 5 - Grid frequency drop

To test the inertial response of the three controllers, a frequency drop of 1 Hz is applied to the AC grid. Before the frequency event, the converter is injecting 0.9 p.u. active power into the grid. The CHiL results for this test are shown in Fig. 6.18. It can be seen that the VCC grid-following control successfully maintains the active power demand during the frequency event but does not provide any additional power injection into the grid to respond to the frequency drop. However, good voltage and power support is provided throughout. The VSM provides an inertia-emulating response by injecting an extra 0.075 p.u. active power into the grid at the frequency event and then returning eventually to the original, pre-event power level. The PSC also injects additional active power, but at a constant value throughout the period of the frequency event due to the inherent droop behaviour. The PSC also shows a small voltage oscillation (related to the coupling discussed in Fig. 6.13) that is not seen with VSM or VCC.

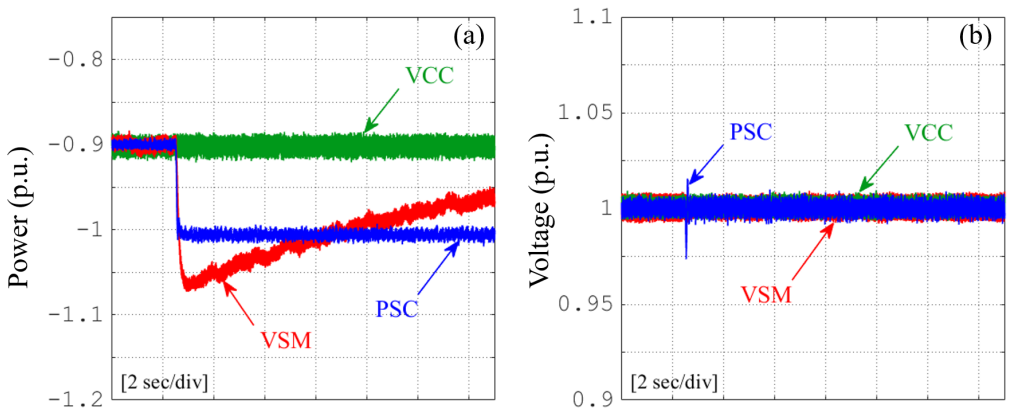

Fig. 6.18: CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a 1 Hz drop in AC grid frequency and 0.25 Hz/s recovery with VCC (green), PSC (blue) and VSM control (red).

6.2.3 Round 3 - Frequency-domain assessment

Impedance transfer function matrix

The most common and established form of frequency-domain assessment for AC grid-connected VSCs is the Norton-equivalent admittance-impedance model. As discussed in Section 6.1.3, the impedance of the converter-controller can be generated via frequency scanning (in cases (a) and (b)) or using the full analytical model (in case (c)). For this comparison, the converter impedances are extracted from the small-signal models and further details of impedance modelling for the respective controllers can be found in [42,72,73]. The converter and grid are represented as a current source in parallel with a Norton-equivalent impedance, $Z_c(s)$, and a voltage source in series with a Thevenin-equivalent impedance, $Z_g(\omega_g, s)$, respectively, as shown in Fig. 6.19, where ω_g is the nominal grid frequency [73].

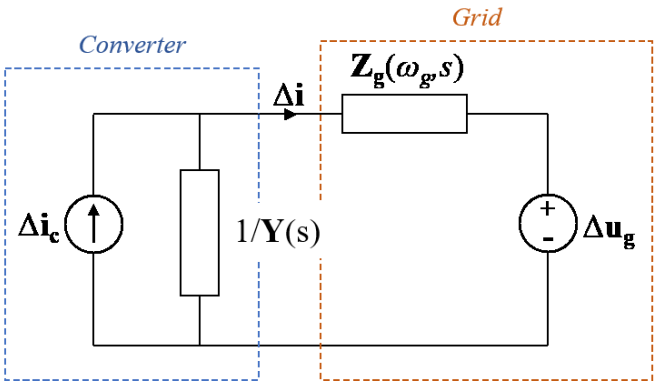

Fig. 6.19: Equivalent circuit diagram of the system impedance model.

The bode plots of the $Z_c(s)$ impedance matrix in the dq-frame for each controller at SCR = 1, $P = -1.0$ p.u. are shown in Fig. 6.20, along with the grid impedance frequency response. Stability of the system is governed by the ratio of $Z_g(s)/\ Z_c(s)$, which can be interpreted graphically to a certain extent by the phase margin where the magnitudes of $Z_c(s)$ and $Z_g(s)$ intersect [73]. It can be seen that this intersection occurs at a higher frequency for VCC than for the other two controllers, where greater phase loss has occurred and so the phase margin is correspondingly smaller. Fig. 6.20(b) and (c) also show that the off-diagonal impedances of VCC are higher than either PSC or VSM at high frequencies, implying stronger cross-coupling between the converter voltages and currents at high frequencies. The assumptions made for VCC in strong grids of independent power and voltage control therefore cannot be applied in these operating conditions. The VSM shows a resonance at the grid frequency (50 Hz), which is far less prominent in either PSC or VCC control. This resonance may cause oscillations if additional damping is not employed.

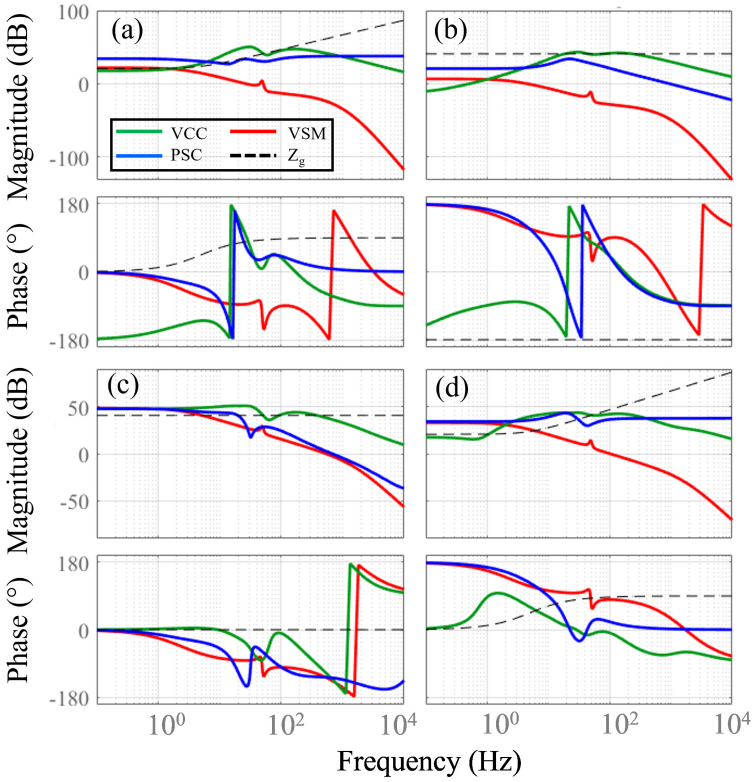

Fig. 6.20: Bode plots of the converter impedances, $Z_c(s)$, for VCC (green), PSC (blue) and VSM control (red) in a SCR = 1 grid with impedance $Z_g(s)$: (a) from i_{cd} to u_{fd} (b) from i_{cq} to u_{fd} (c) from i_{cd} to u_{fq} and (d) from i_{cq} to u_{fq}.

Jacobian transfer function matrix

The Jacobian transfer function matrix, $J(s)$, of the controlled, AC grid-connected converter system is defined as:

$$\begin{bmatrix} \Delta P \\ \Delta U \end{bmatrix} = \begin{bmatrix} J_{P_{ref}P}(s) & J_{U_{ref}P}(s) \\ J_{P_{ref}U}(s) & J_{U_{ref}U}(s) \end{bmatrix} \begin{bmatrix} \Delta P_{ref} \\ \Delta U_{ref} \end{bmatrix} \tag{6.1}$$

The Jacobian form is used in particular in [18, 36] for modelling PSC, but it can also be applied to any other VSC control strategy that employs active power and AC voltage control (the AC voltage control can also be substituted for reactive power control). This form of the system allows analysis of the upper level system coupling and the condition of the controlled process. Fig. 6.21 shows the bode plots of the

Jacobian transfer function matrix of each of the controllers under test. If the off-diagonal magnitudes exceed the diagonal magnitudes, the process is ill-conditioned [77] and this has a corresponding impact on the time-domain performance. For instance, it can be seen that the magnitude of $J_{UrefP}(s)$ in Fig. 6.21(b) is greater than the diagonal transfer functions for all three controllers, suggesting that the active power is strongly coupled to the AC voltage reference. This effect can be seen in the time-domain by performing a step change in AC voltage reference using the CHiL RTDS experimental set-up, as shown in Fig. 6.22. Applying a 0.1 p.u. step change in Uref produces a large deviation in P with all three control strategies. In contrast, the magnitudes of $J_{PrefU}(s)$ in Fig. 6.21(c) are smaller than the diagonal transfer functions and so the effect of a power reference change on the PCC voltage is much smaller, as was demonstrated by the power reference step in Fig. 6.11. Again, the VSM shows a resonance at 50 Hz grid frequency.

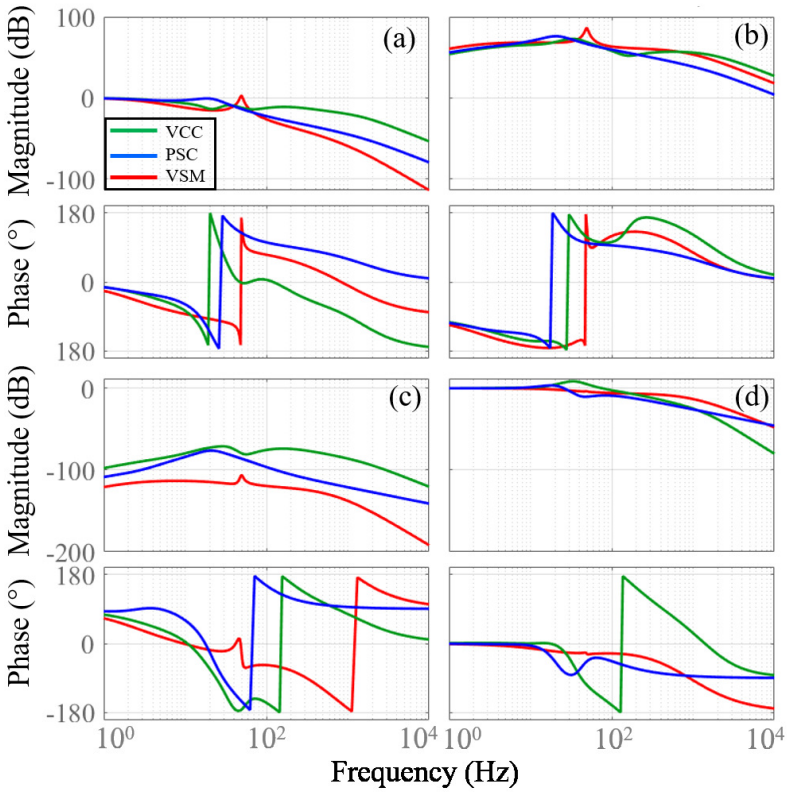

Fig. 6.21: Bode plots of the Jacobian transfer function matrix for VCC (red), PSC (green) and VSM control (blue) in a SCR = 1 grid: (a) from P_{ref} to P, (b) from U_{ref} to P, (c) from P_{ref} to U and (d) from U_{ref} to U.

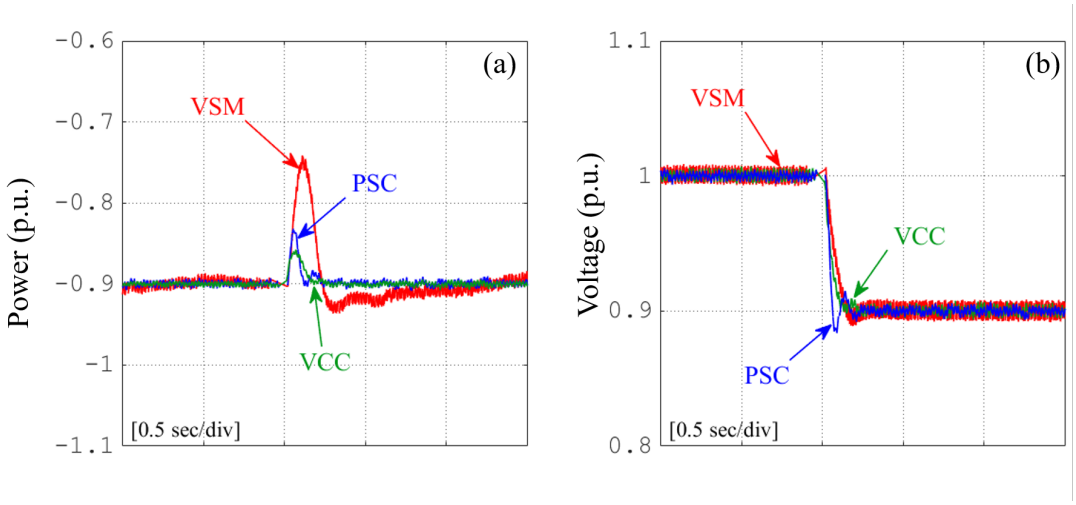

Fig. 6.22: CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a step change of 0.1 p.u. in voltage reference at $P = -0.9$ p.u., $U = 1.0$ p.u. with VCC (green), PSC (blue) and VSM control (red).

6.2.4 Comparison between the three controllers

The results of the standardized assessment framework for VCC, PSC and VSM in a very weak AC grid have revealed significant advantages and disadvantages of each strategy. Round 1 results show that all three controllers have a sufficient parameter space that can achieve stable operation with good dynamic performance between the theoretical limits of -1.0 p.u. and 0.89 p.u. active power transfer in a SCR = 1 AC grid. All three control strategies provide good voltage support and the same active power limits during a reference ramp. However, VSM control is slower than the other two control strategies. The VCC is the most robust to increases in grid strength (i.e. increase in SCR) without re-tuning. Though stable, the PSC exhibits large voltage and power oscillations during a grid parameter change and the VSM shows increasing oscillations in active power as the grid is strengthened. The PSC and VSM can inject additional active power to support the grid during frequency disturbances. Although the VCC does not offer inertia support, it shows good voltage support during frequency event and the active power is maintained at the reference level throughout. This comprehensive assessment suggests that VCC is the most robust choice for variable (or unknown) AC grid impedance systems, but independent active power and voltage control cannot

be assumed in a very weak AC grid. For frequency support applications, the VSM or PSC strategies are preferable and, of these strategies, the VSM control provides better voltage support in a very weak AC grid. However, additional damping should be considered for VSM control. PQ cross-coupling is strong for all controllers because of the high impedance of the AC grid. A summary of the performance of the VCC, PSC and VSM under this framework is given in Table 6.5.

Table 6.5: Summary of inverter controller performance

	VCC	PSC	VSM
-1.0 $< P <$ 0.89 p.u.	Yes	Yes	Yes
U_f support in power step	Good	Moderate	Good
U_f support in voltage sag	Good	Poor	Poor
Grid strength robustness	Good	Re-tune	Re-tune
Inertia emulation	No	Yes	Yes
PQ cross-coupling	Strong	Strong	Strong

VSC controllers with non-classical structures or additional complexity – such as model predictive control (MPC), passivity-based control and additional droop controls – can also be assessed using this framework. For these alternative controllers, the Round 2 (time-domain) and Round 3 (frequency-domain) assessments can be applied directly as described in sections 6.2.2 and 6.2.3, using either models or full hardware implementation. The optional Round 1 tuning stage should be adapted to include the most relevant additional controller parameters. For example, for MPC, the effect of the prediction horizon and choice of cost function on the stable controller operating space should be considered. In this case, multiple stable operating regions would be constructed during Round 1 with different baseline prediction algorithms. For droop-controlled VCC, the droop gain would be considered as an extra tuning variable in this step.

6.3 Summary

This chapter has proposed a standardized assessment framework for performance analysis of any VSC controller at the design or implementation stage. The modular assessment format accommodated all controllers from analytical models at the design stage to pre-tuned 'black box' controllers installed in a real ac grid system. Three stages of assessment were proposed to perform tuning, time-domain and frequency-domain analyses. The first stage incorporated a tuning assessment across a much broader range of controller operating points and bandwidths than are usually considered and varied three controller parameters simultaneously to establish the safe operating region for that controller. Imposing dynamic performance constraints on this area of stable operating points narrowed down the stable region so that an optimum tuning point can be extracted. These tunings were carried forward to the second stage where control hardware-in-the-loop RTDS experiments were performed to compare the active power limits, dynamic response to power and voltage changes, robustness to grid impedance and the frequency disturbance response. In the third stage, the Jacobian transfer function matrices and impedance matrices were extracted to compare cross-coupling, condition of the process and resonances. An example analysis of VCC, PSC and VSM control strategies using the proposed framework showed that these control strategies offer comparable performance in steady-state, non-fault conditions, but the grid-forming controllers give a slower response. VCC was the most robust strategy for sag conditions or changes in grid impedance but demonstrated strong cross-coupling in the frequency domain.

Chapter 7

Dual-Infeed VSC-HVDC in Weak Grids

This chapter examines the modelling of dual-infeed VSC-HVDC using vector current control, and the effect of controller tunings, tie-line length and SCR on the maximum active power transfer and system resonance. Direct comparison is also made to the performance of a single-infeed VSC-HVDC system without the secondary infeed present. Small-signal modelling and MATLAB/Simulink time-domain simulations with averaged VSC models are used for the initial analysis, and control hardware-in-the-loop (CHiL) experiments with a PLECS real-time digital simulator (RTDS) are used to validate the findings. It is found that the dual-infeed system can perform comparably to the single-infeed system if the controller is re-tuned correctly. However, the resonance in the system is significant if the tie-line length is short and this means it is essential that time delays are taken into account in small-signal analysis.

7.1 Introduction

The underlying assumption of the multi-infeed HVDC literature reviewed in Section 2.2 is that the addition of a second (or multiple) HVDC infeeds to a weak AC grid will inevitably destabilize the system i.e. it is assumed that the control performance of a MI-HVDC system will always be worse than that of a single-infeed HVDC system in

a weak AC grid. However, there have been limited attempts so far in the literature to comprehensively compare and quantify the stability and power transfer capabilities of single-infeed and dual-infeed HVDCs system in very weak AC grids. In each of the sensitivity and tuning studies for MI-HVDC systems in [51, 54, 59, 63, 67–69], there is a strong focus on resonance and interaction modes, but there is no comparison to the baseline performance of a single-infeed HVDC system. It is also generally assumed in all of these works that all HVDC feeds connecting to an AC network will be injecting power into the AC grid, i.e. that both converter stations will be operating as inverters. However, the increasing interconnectivity of the global power network and the need to simultaneously import power from offshore resources and export power to higher demand locations means that MI-HVDC converters may often be working in opposing modes. The question of the impact of these operating modes, and how this effects the comparison with a single-infeed HVDC system, has not been adequately answered in the literature. This chapter therefore explores whether the addition of an extra HVDC link in close electrical proximity to an existing, weak-grid connected HVDC infeed can in fact be beneficial to stability, dynamic performance and maximum power transfer. Differences in controller tuning requirements for the dual-infeed system are studied, as well as the impact of changing power flow direction. Due to the high-voltage, high-power systems being studied and the relative novelty of MI-HVDC research, there are very few studies which attempt to validate the findings with hardware, or via the intermediate step of combining RTDS with control hardware-in-the-loop (CHiL). It has been implicitly assumed that the simplifications and modifications made in order to accurately model and simulate single-infeed systems will be the same as those required for MI-HVDC, and hence that stability analysis simply requires reformulating the system under test. However, attempts to validate the stability limits of a weak AC grid MI-HVDC system using a CHiL/RTDS set-up have shown significant discrepancies between the analytical and CHiL systems, particularly with respect to the effect of high-frequency resonances which are present when a dual-infeed system is strongly coupled (i.e. has a short tie-line length). This high-frequency resonance is seen in the analytical model, but is not the limiting factor for stability, and very short tie-lines

can be employed without apparently destabilizing the small-signal system. In contrast, below a certain tie-line length, very large oscillations are seen in the CHiL experimental set-up which rapidly destabilize the system. This discrepancy can be compensated for by addition of a 4th order Pade approximation time delay in the small-signal model. The presence of this time delay significantly shifts the balance of which interactions in the system play the biggest role in determining overall stability. This chapter will therefore also summarise some of these modelling discrepancies and the adjustments that must be made to accurately model weak grid-connected dual-infeed VSC-HVDC systems in the frequency domain.

7.2 Study System and Modelling

The system modelled in this study for all small-signal analysis, MATLAB/Simulink simulation, and PLECS CHiL experiments is shown in Fig. 7.1. In the analytical and MATLAB/Simulink model, the VSCs are averaged models represented by controllable voltage sources. For the CHiL experiments, both VSCs are two-level switching models. Both of the VSC controllers employ conventional vector current control, as described in Section 3.1. The system power levels and default power flow directions are based on the Shetland-Caithness-Moray HVDC links in Northern Scotland [12,78]. SYS2 represents the Shetland-Caithness Viking HVDC link which is rated at 600 MW and is expected to be importing power into the Caithness substation from the Shetland renewable resources. SYS2 will therefore be modelled as a fixed link which is constantly inverting 1.0 p.u. power (i.e., injecting into the grid). SYS1 represents the Caithness-Moray link which is rated at 800 MW. In this link, power flow can be varied in both magnitude and direction for the purposes of the study. The parameters for both infeeds and the grid are given in Table 7.1.

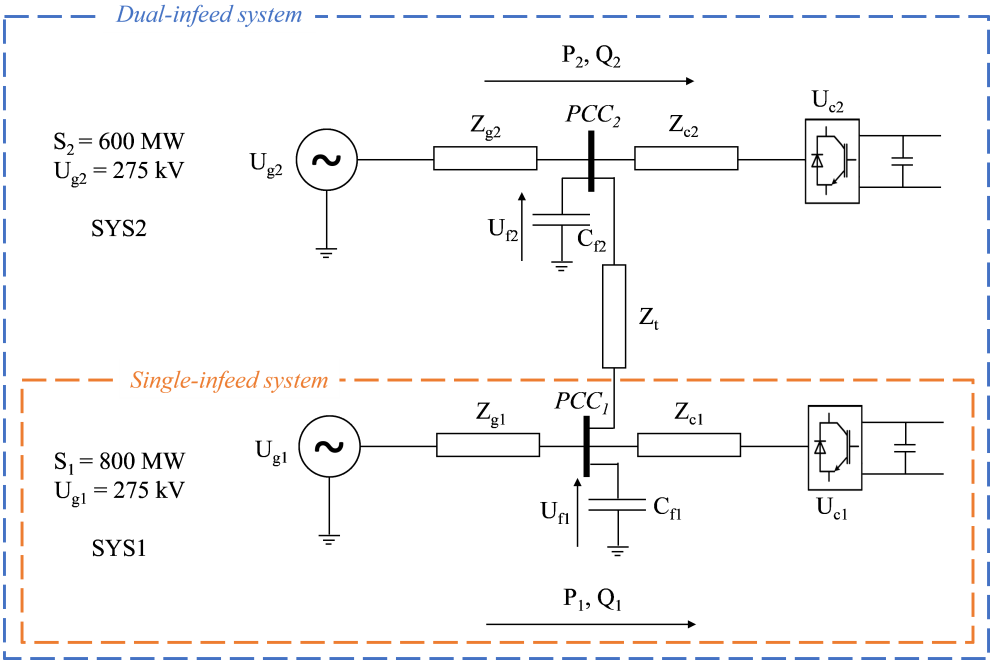

Fig. 7.1: Single-line diagram of the dual-infeed VSC-HVDC system.

Table 7.1: Dual-infeed system parameters

	Parameter	Value
SYS1	AC system rated voltage, RMS line (kV)	275
	AC system rated power (MW)	800
	AC system frequency (Hz)	50
	SCR	1
	X/R ratio	10
	AC system inductance, L_{g1} (H)	0.2994
	AC system resistance, R_{g1} (Ω)	9.4062
	Filter/transformer inductance, L_{c1} (H)	0.0602
	Filter/transformer resistance, R_{c1} (Ω)	0.9453
	Filter capacitance, C_{f1} (μF)	1.347
SYS2	AC system rated voltage, RMS line (kV)	275
	AC system rated power (MW)	600
	AC system frequency (Hz)	50
	SCR	1
	X/R ratio	10
	AC system inductance, L_{g2} (H)	0.3992
	AC system resistance, R_{g2} (Ω)	12.5416
	Filter/transformer inductance, L_{c2} (H)	0.0802
	Filter/transformer resistance, R_{c2} (Ω)	1.2604
	Filter capacitance, C_{f2} (μF)	1.010
Tie-line	Resistance, R_t (Ω/km)	0.029
	Impedance, L_t (H/m)	0.001
	Tie-line length, D_t (km)	50
Converter	DC link rated voltage (kV)	300
	Switching frequency, $1/T_{s,control}$ (kHz)	10
	RTDS time step, $T_{s,plant}$ (μs)	4

The small-signal models for each grid, RCL filter and VSC are as presented in Section 3.1. The tie-line is modelled as a lumped parameter RL line, synchronized to the voltage angle at PCC_1. The tie-line is thus represented by the state-space equations 7.1 to 7.5, with the state-space matrices given in 7.6 to 7.8.

$$\Delta \dot{x}_t = A_t \Delta x_t + B_t \Delta u_t \tag{7.1}$$

$$\Delta y_t = C_t \Delta x_t \tag{7.2}$$

$$\Delta x_t = \begin{bmatrix} \Delta i_{td} & \Delta i_{tq} \end{bmatrix} \tag{7.3}$$

$$\Delta u_t = \begin{bmatrix} \Delta u'_{fd,2} & u'_{fq,2} & u_{fd,1} & u_{fq,1} \end{bmatrix} \tag{7.4}$$

$$\Delta y_t = \begin{bmatrix} \Delta i_{td} & \Delta i_{tq} \end{bmatrix} \tag{7.5}$$

$$A_t = \begin{bmatrix} -\frac{R_t}{L_t} & \omega_g \\ -\omega_g & \frac{R_t}{L_t} \end{bmatrix} \tag{7.6}$$

$$B_t = \begin{bmatrix} \frac{1}{L_t} & 0 & -\frac{1}{L_t} & 0 \\ 0 & \frac{1}{L_t} & 0 & -\frac{1}{L_t} \end{bmatrix} \tag{7.7}$$

$$C_t = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{7.8}$$

where, $u'_{fd,2}$ and $u'_{fq,2}$ represent the PCC_2 voltages referred to the synchronization angle at PCC_1, in order to be in the same reference frame. The equations for this transformation are given in 7.9. The tie-line currents must also be referred to the synchronization angle at PCC_2 in order to be in the same reference frame when used in the SYS2 grid and converter equations. This transformation is given in 7.10. These equations assume that $\Delta\theta_{10} = \Delta\theta_{20} = 0$.

$$\begin{bmatrix} \Delta u'_{fd,2} \\ \Delta u'_{fq,2} \end{bmatrix} = \begin{bmatrix} 1 & 0 & u_{fq0,2} & -u_{fq0,2} \\ 0 & 1 & -u_{fd0,2} & u_{fd0,2} \end{bmatrix} \begin{bmatrix} \Delta u_{fd,2} \\ \Delta u_{fq,2} \\ \Delta\theta_1 \\ \Delta\theta_2 \end{bmatrix} \tag{7.9}$$

$$\begin{bmatrix} \Delta i'_{td} \\ \Delta i'_{tq} \end{bmatrix} = \begin{bmatrix} 1 & 0 & i_{tq0} & -i_{tq0} \\ 0 & 1 & -i_{td0} & i_{td0} \end{bmatrix} \begin{bmatrix} \Delta i_{td} \\ \Delta i_{tq} \\ \Delta \theta_1 \\ \Delta \theta_2 \end{bmatrix} \tag{7.10}$$

7.3 Validation with CHiL RTDS

In the CHiL experimental set-up, the plant and two-level VSCs are modelled on a Plexim RT Box 3, which is programmed in PLECS Blockset with a step size, $T_{s,plant} = 4$ μs. The VSC controllers are modelled using two TI C2000 microcontrollers on F23879D Launchpads which use a control time step, $T_{s,control} = 10$ μs. This corresponds to a switching frequency of 10 kHz. Each microcontroller interfaces independently with the RT Box via analogue and digital I/Os and output data is either viewed with a DAC output and oscilloscope or saved to a USB Flash Drive in the RT Box and plotted offline in MATLAB. This CHiL setup is shown in Fig. 7.2.

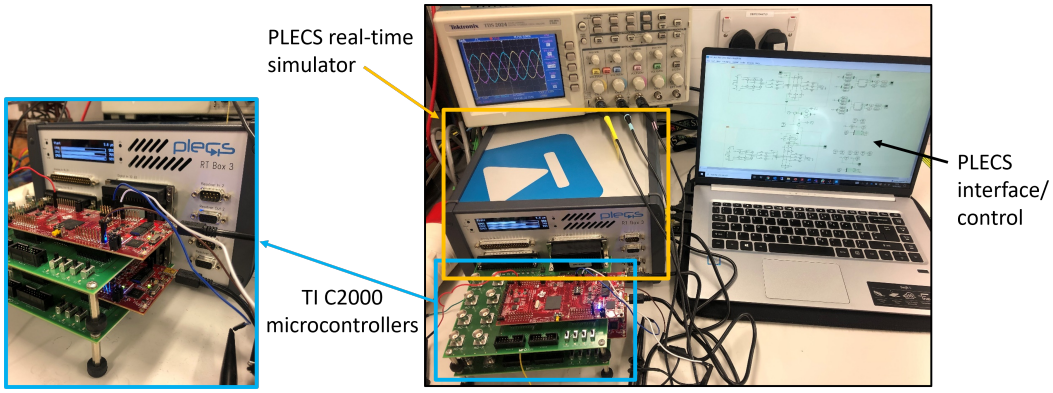

Fig. 7.2: Experimental set-up for CHiL experiments with PLECS RTDS and microcontrollers.

The CHiL experimental set-up is used to validate the small-signal model derived in Section 7.2. Fig. 7.3 shows the power and voltage response of the CHiL experimental results, the Simulink time-domain model and the small-signal analytical model for a 0.1 p.u. active power step change in SYS1 at 0.5 p.u. inverting. For this validation the tie-line length, D_t, is 50 km.

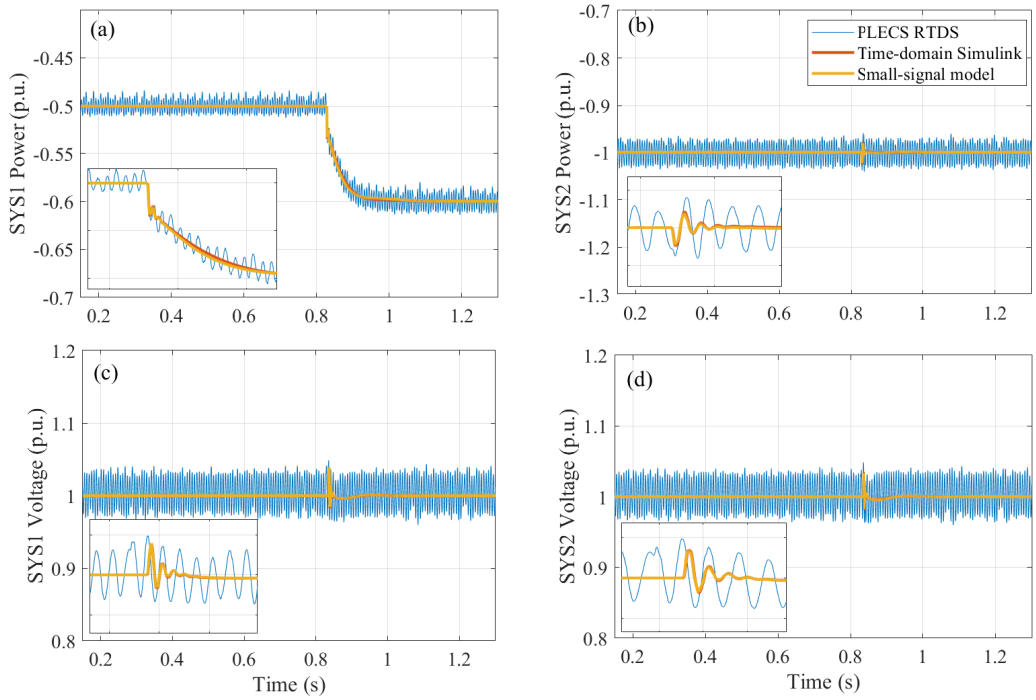

Fig. 7.3: Validation of the small-signal model with Simulink time-domain simulation and PLECS CHiL experimental results. Active power step of 0.1 p.u. applied to SYS1 at 0.5 p.u. inverting power, with $D_t = 50$ km

During the validation process it was found that, when D_t was reduced to below $\sim$ 20 km, the PLECS CHiL system became unstable whilst the small-signal model did not. This is due to the inherent time delays present in the microcontrollers and communication with the RTDS. It is conventional to assume a time delay of approximately $1.5{*}T_{s,control}$, which in this case would correspond to 150 μs. The actual time delay in the PLECS system was found by adding a 4th order Pade approximation time delays to the small-signal model at the voltage reference point and increasing this delay gradually until the stability boundaries were consistent with the CHiL experimental results. This method suggested a time delay of 175 μs was present in the PLECS CHiL setup, which is close to the predicted 150 μs. The active power step response of the CHiL system and small-signal model with and without this time delay is shown in Fig. 7.4, showing that the small-signal model only accurately represents the instability when the time delay is present.

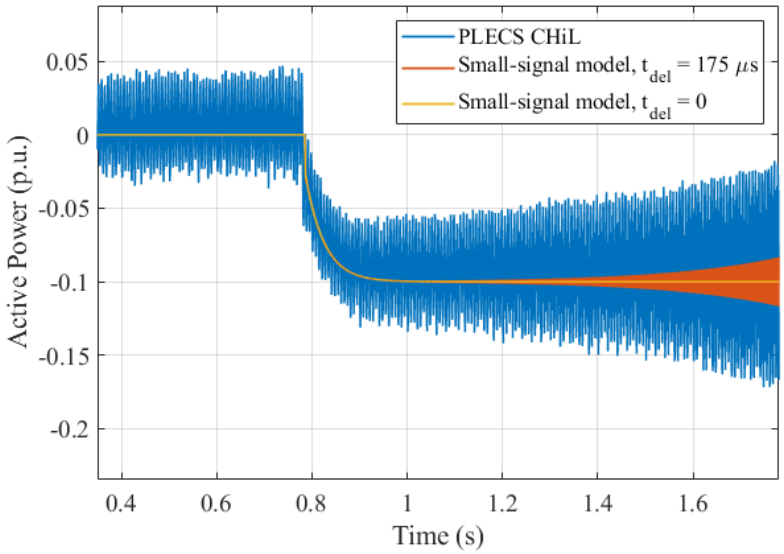

Fig. 7.4: Validation of the small-signal model with added time delay and PLECS CHiL experimental results.

Including this time delay is critical to accurately modelling the stability boundaries of the dual-infeed VSC-HVDC system with strong coupling (i.e., a short tie-line length). The necessity of modelling this delay is much stronger in the dual-infeed case than for single-infeed modelling – often, small-signal and impedance models can be largely accurate for single-infeed stability analysis even if this time delay is neglected. However, as demonstrated, this assumption could vastly overestimate system stability for dual-infeed systems that are strongly coupled. It is therefore vital that system time delays are taken into account for MI-HVDC modelling. For the validation shown in Fig. 7.3 and for all the analyses in this chapter, the small-signal model includes this 175 μs time delay.

7.4 Re-Tuning for Dual-Infeed Operation

The performance of VCC-VSC in weak AC grids is very sensitive to the controller tuning. It cannot be assumed that the optimal tuning for a dual-infeed system will be the same as for a single-infeed system, and any comparison between two such systems without re-tuning will be inconclusive. Depending on the requirements and limita-

tions of the system, control designers and operators may have different tuning goals. Whatever goals are chosen (e.g. minimum stability margins, dynamic performance, disturbance rejection), a wide range of values for the controller parameters being tuned should be explored to avoid the trap of local maxima. VCC-VSC systems in very weak AC grids have small stability margins, and so maximising these margins is a popular tuning goal. However, maximum stability margins in weak AC grids are (in general) achieved with a slow PLL and slow outer control loops, which can give very poor dynamic performance. Therefore, for this comparison of single- and dual-infeed VSC systems, the controller tuning assessment will examine both the small-signal stability and the dynamic performance as the controller tunings are varied across a broad range of controller operating points. For this initial broad range assessment, the chosen performance metric will be the maximum active power (MAP) that can be achieved through the variable feed, SYS1. Rather than producing a single, optimised set of tuning parameters for a given single performance metric, this method presents a visualisation of the feasible operating space for the controller tunings of single- and dual-infeed systems and provides a comparison of the MAP in each system at a wide range of tunings.

The small-signal model is used to calculate the MAP through SYS1 (henceforth referred to as MAP_1) as a function of the tunings of the inner current loop (ICL), phase-locked loop (PLL), active power loop (APL) and AC voltage loop (AVL). Two control parameters are varied at any given time so that the interactive effect of these parameters can be seen. This process is first performed to tune the inner control loops (i.e. the ICL and PLL), with all other control parameters fixed at the values given in Table 7.2. The bandwidths of the ICL and PLL can be directly varied through control of α and ω_{PLL}. Fig. 7.5 shows MAP_1 as a function of ICL and PLL bandwidths in (a) inverting and (b) rectifying modes for the single-infeed system and a dual-infeed systems (tie-line length, $D_t = 50$ km). In inverting mode (injecting power into the grid), maximum power is achieved when $\omega_{PLL} > 30$ Hz and $\omega_{ICL} < 500$ Hz and both the single- and dual-infeed systems can achieve rated power (-1.0 p.u.). In both systems, a slow ICL and fast PLL are optimal to maximise the stability margins. In rectifying mode, maximum power is achieved at $\omega_{ICL} \approx 500$ Hz and $\omega_{PLL} < 25$ Hz for both

systems. Under rectifying operation, MAP_1 is higher for the dual-infeed system (0.98 p.u.) than for the single-infeed system (0.627 p.u.).

Table 7.2: Default VCC controller tuning parameters for dual-infeed.

	Control loop	Parameters	Value	
			Inverting	Rectifying
SYS1	ICL	$\alpha = 1/\omega_{ICL}$	0.001	0.002
	PLL	ω_{PLL} (Hz)	10	50
	APL	k_{p-P1}	1×10^{-6}	1×10^{-6}
		k_{i-P1}	1×10^{-3}	1×10^{-3}
		k_{p-U1}	2×10^{-2}	1×10^{-2}
	AVL	k_{i-U1}	3	3
SYS2	ICL	$\alpha = 1/\omega_{ICL}$	0.002	
	PLL	ω_{PLL} (Hz)	50	
	APL	k_{p-P2}	1×10^{-6}	N/A
		k_{i-P2}	1×10^{-3}	
		k_{p-U2}	2×10^{-2}	
	AVL	k_{i-U2}	3	

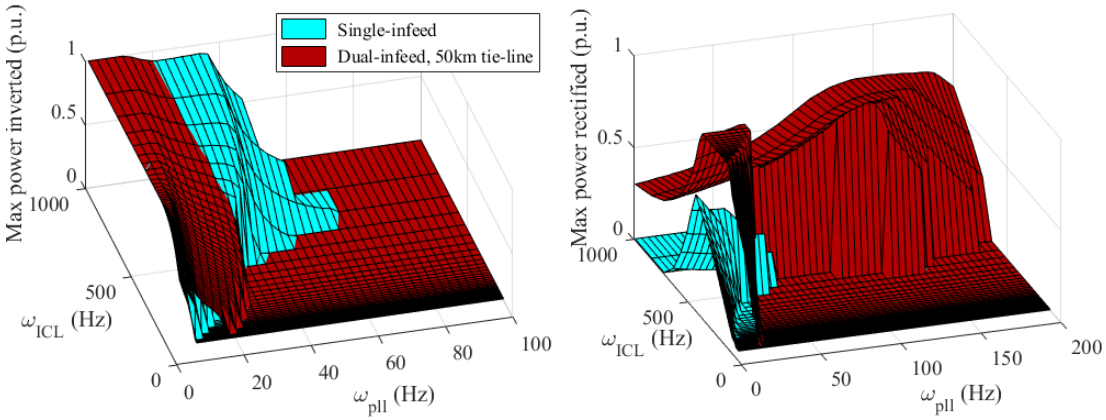

Fig. 7.5: Inner loop tuning, (a) inverting and (b) rectifying modes.

From these results, the ICL and PLL tunings can be fixed according to the regions with highest MAP_1 in Fig. 7.5. The tuning process is then repeated for the outer control loops (APL and AVL). In this case, the loop bandwidths cannot be directly determined by a single control parameter due to cross-coupling within the system.

However, the integral gains, k_{i-P1} and k_{i-U1} can be used as proxies for the APL and AVL bandwidths, respectively, if the proportional gains are held fixed. The MAP_1 values for the single- and dual-infeed systems as a function of k_{i-P1} and k_{i-U1} are shown in Fig. 7.6, again in both inverting (a) and rectifying (b) modes. For the outer loop tuning, it is clear that the single-and dual-infeed systems have different optimum operating points, particularly in inverting mode. For both power flow directions, the single-infeed system can tolerate higher values of k_{i-U1} (and therefore a faster AVL) but much lower values of k_{i-P1} (and therefore a slower APL). This implies that the dual-infeed system may a provide faster power response than the single-infeed system, but at the cost of a slower voltage response. As was seen when performing the inner loop tuning, in inverting mode, both systems can achieve rated active power injection to the grid (-1.0 p.u.). However, in rectifying mode the dual-infeed system can still achieve a higher maximum value of MAP_1 (1.0 p.u.) than the single-infeed system (0.86 p.u.). The outer loop tuning stage has increased the single-infeed MAP_1 relative to the inner loop tuning stage.

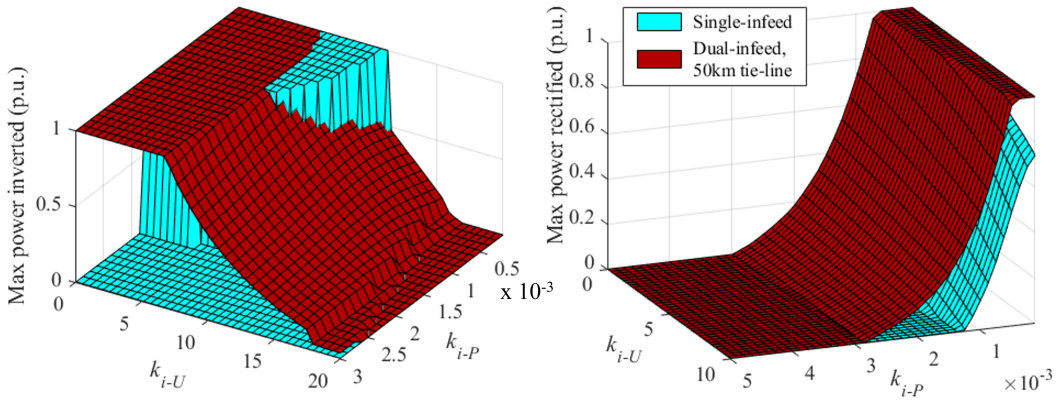

Fig. 7.6: Outer loop tuning, (a) inverting and (b) rectifying modes.

This assessment over a wide range of controller tunings in therefore gives approximate ranges for the optimum tuning of each system. A critical point to note is that both the single and dual-infeed systems must be tuned differently for inverting and rectifying operation in order to maximise active power transfer. Failure to re-tune the system in different operating modes will lead to a vast underestimation of the system capabilities.

The final, precise controller tuning must take into account both stability margins and dynamic performance. When considering system stability margins, slower outer loops are, in general, more stable in weak AC grids. This is demonstrated in Fig. 7.7, which shows the eigenvalue loci of the single- and dual-infeed systems as a function of k_{i-U1} for the range covered in Fig. 7.6. The dominant high-frequency eigenvalues move towards the RHP as k_{i-U1} is increased, showing that slower AVL speeds provide a larger stability margin. However, this produces poor voltage dynamic performance in the PCC voltage, as demonstrated in Fig. 7.8.

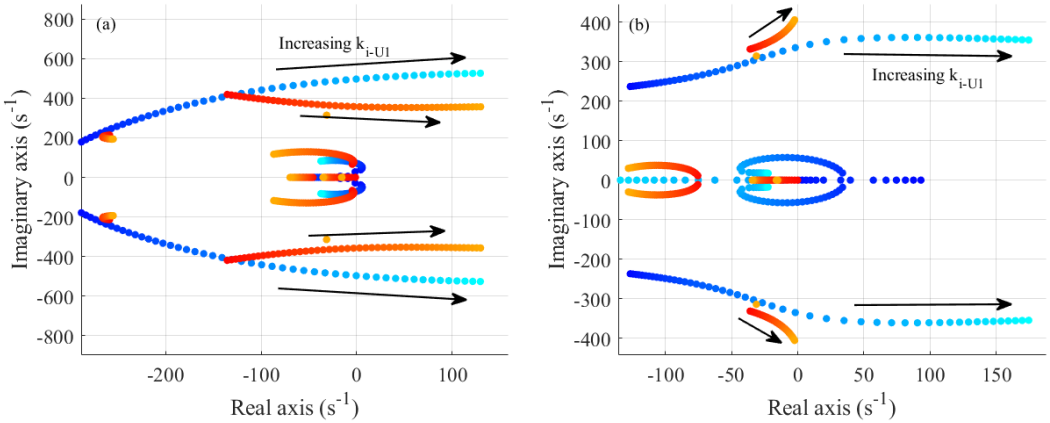

Fig. 7.7: Dominant system eigenvalues with varying k_{i-U1} in (a) inverting mode and (b) rectifying mode. Single-infeed (small k_{i-U1} in red, larger k_{i-U1} in orange) and dual-infeed (small k_{i-U1} in blue, larger k_{i-U1} in cyan) systems.

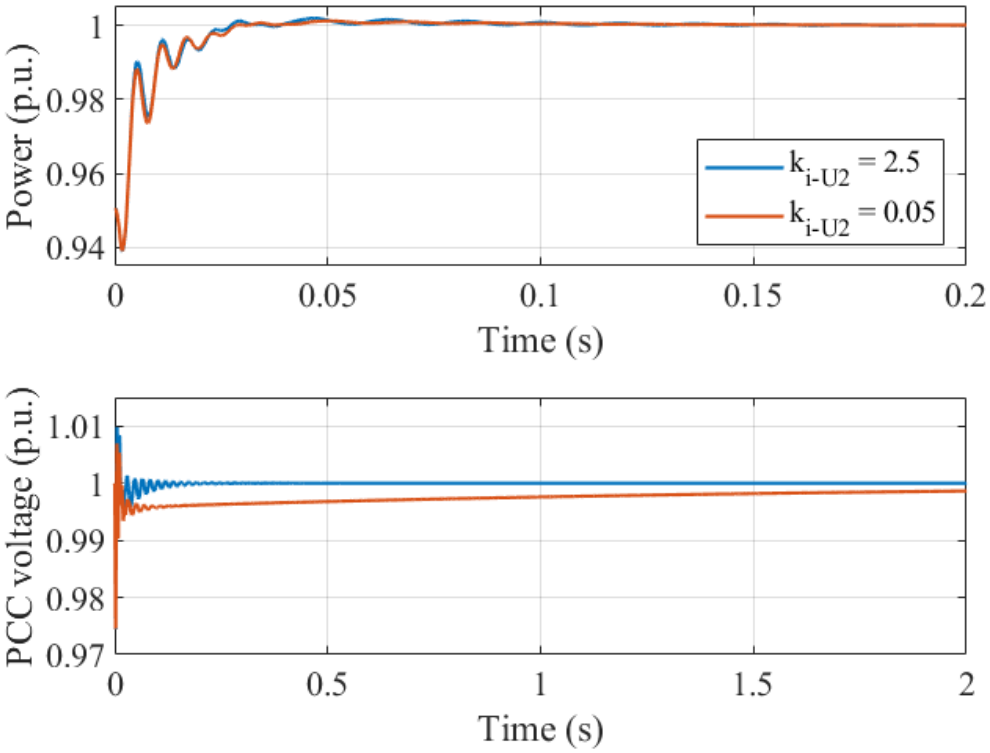

Fig. 7.8: Active power and PCC voltage response to a 0.05 p.u. step in $P_{ref,1}$ at $P_1 = 0.95$ p.u.

Due to these dynamic performance considerations, the final tuning for each system is chosen such that it is comfortably within the high stability regions on Fig. 7.5 and Fig.7.6, but also ensures acceptable dynamic voltage performance. For this assessment, a maximum $U_{pcc,1}$ settling time of 1 s and steady-state error < 0.001 p.u. is chosen, but these conditions can be adapted to specific system requirements. The final tunings under these specifications are given in Table 7.3. It can be shown that weakest grid situation is the limiting factor for controller tuning, i.e. any controller tuning that produces a stable system in a grid with a given SCR will remain stable if the grid strength is increased (discussed further in Section 4.3.3). Therefore, by tuning at SCR = 1, the system is tuned for the 'worst case scenario' and these tunings will be maintained as the grid is strengthened later on. We can conclude from this process that:

(a) the presence of a secondary HVDC infeed in close electrical proximity requires re-tuning of the system. Dual-infeed system requires a slower AVL but can tolerate a faster APL, paticularly in inverting mode,

(b) if tuned optimally, the maximum value of MAP_1 for the dual-infeed system can exceed that of the single-infeed system.

Table 7.3: Final tunings for SYS1 in the dual-infeed system.

	Dual-infeed		Single-infeed	
	Inverting	Rectifying	Inverting	Rectifying
ICL	$\omega_{ICL} = 1000$ Hz	$\omega_{ICL} = 500$ Hz	$\omega_{ICL} = 1000$ Hz	$\omega_{ICL} = 500$ Hz
PLL	$\omega_{PLL} = 10$ Hz	$\omega_{PLL} = 5$ Hz	$\omega_{PLL} = 10$ Hz	$\omega_{PLL} = 5$ Hz
APL	$k_{i-P1} = 1 \times 10^{-3}$	$k_{i-P1} = 0.5 \times 10^{-3}$	$k_{i-P1} = 0.5$ x 10-3	$k_{i-P1} = 0.1 \times 10^{-3}$
AVL	$k_{i-U1} = 2$	$k_{i-U1} = 3$	$k_{i-U1} = 5$	$k_{i-U1} = 3$

7.5 Tie-line Length and Maximum Active Power

The analysis of MAP_1 across the whole controller tuning space suggests that, if correctly tuned, the dual-infeed system can achieve higher power transfer in a very weak grid than a single-infeed system. However, Section 7.4 has only considered one value of D_t and SCR. The small signal model can again be used to calculate the MAP_1 for each system under a variety of tie-line length and grid strength conditions. The variation of MAP_1 as a function of D_t and SCR for the single- and dual-infeed system is shown in Fig. 7.9. The value of SCR applies to both SYS1 and SYS2 in the dual-infeed case.

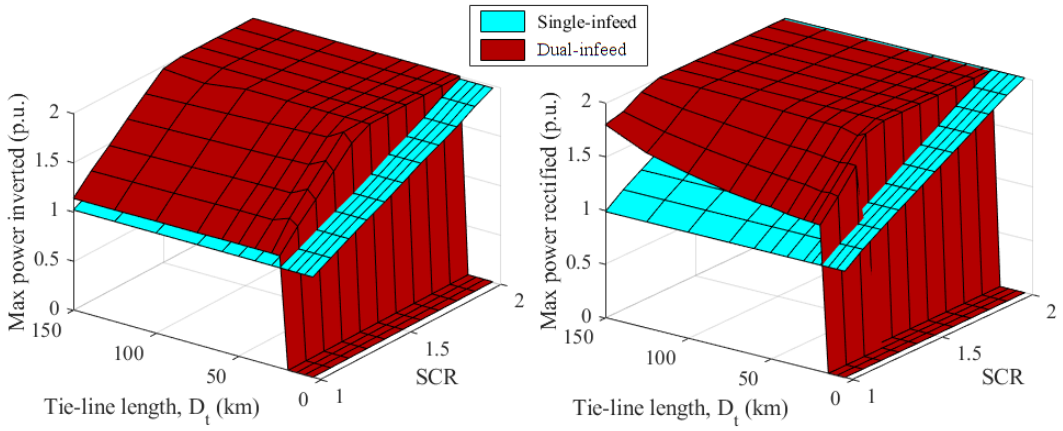

Fig. 7.9: Maximum active power transfer through SYS1 (MAP_1) as a function of tie-line length and grid SCR for the dual-infeed system (red) and as a function of SCR for the single-infeed system (blue).

The tie-line length has a relatively small impact on MAP_1, except when $D_t < 25$ km (distance values applicable only to this specific system). In this case, no power can be transferred in either direction due to the destabilizing effect of the high frequency resonance (discussed further in the next section). In both cases, stability decreases slightly as D_t is decreased – this effect can be seen in the pole map in Fig. 7.10 which shows that the dominant eigenvalues move towards the right-hand plane as D_t is decreased. This effect is more prominent in rectifying mode, likely due to the fact that the current in the tie-line is greater in this mode as the power flows are in opposite directions.

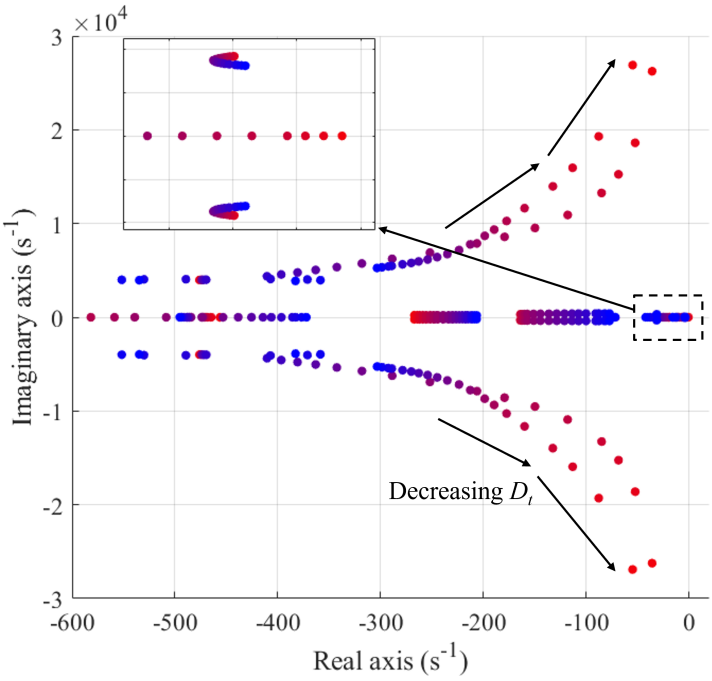

Fig. 7.10: Pole map of the small-signal model eigenvalues as D_t varies from 150 km (blue) to 2.5 km (red).

7.6 Resonance

A key feature that can be seen when examining the CHiL experimental results for a dual-infeed with a short tie-line is a strong, high-frequency resonance. This resonance, of approximately 1450-1500 Hz, is not seen in the long D_t cases with weaker coupling, though in all cases there is also a resonance at 150 Hz i.e., at the 3rd harmonic of the grid frequency. This high-frequency resonance when D_t is short is shown in the inset of Fig. 7.11.

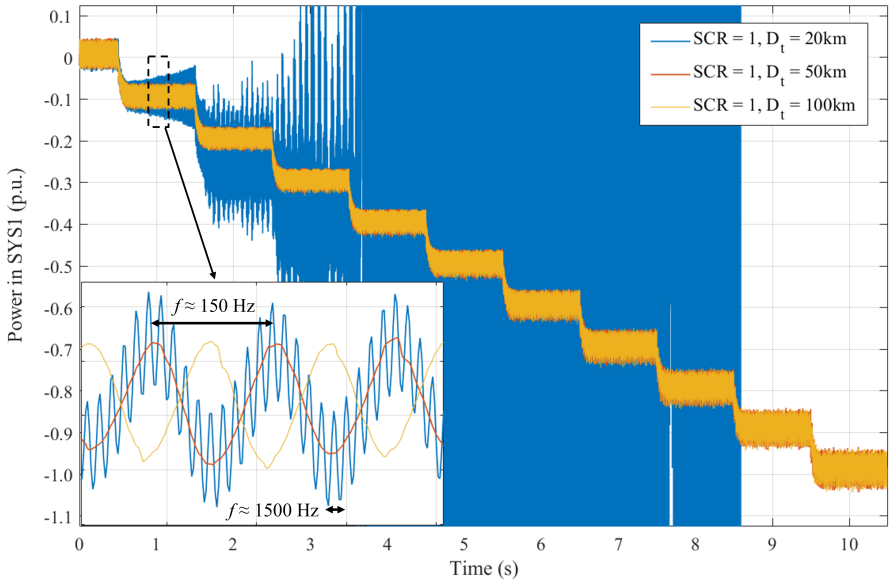

Fig. 7.11: CHiL experimental results of SYS1 active power steps in inverting mode with varying tie-line length. Inset, high frequency resonance present as tie-line length is decreased below a critical value.

The high-frequency resonance demonstrated by the CHiL system is also present in the small-signal model. However, critically, in the small-signal model this resonance is not sufficient to destabilize the system if the control time delay is not modelled, as was discussed in Section 7.3. Even when D_t is reduced to 5 km such that the resonance becomes very large and of a much higher frequency, the small-signal model eigenvalues suggest that stability is maintained if $t_{del} = 0$. If the time delay is modelled at the 175 μs value established in Section 7.3, then this resonance becomes much larger in the small-signal model and does indeed show that the system becomes unstable. The effect of including the time delay in the analytical model can be seen in the frequency response plot of $P_{ref,1}$ to P_1 with varying t_{del} shown in Fig. 7.12.

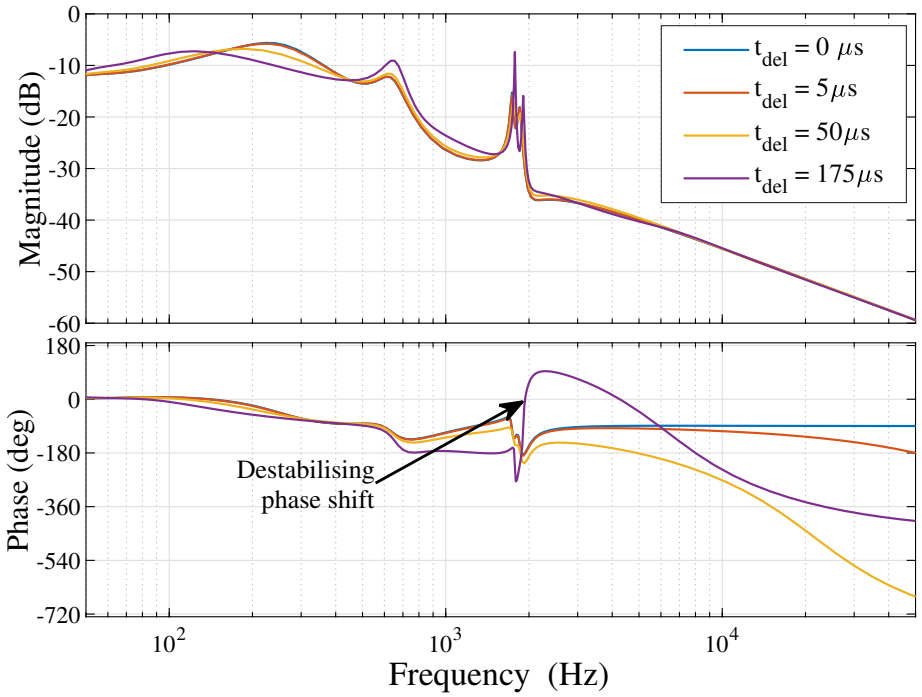

Fig. 7.12: Frequency response of $P_{ref,1}$ to P_1 with varying t_{del}.

Effect of SCR

The stability of the dual-infeed system in CHiL tests is less dependent on the grid SCR than might be expected – increasing the grid SCR does increase the stability at short D_t, but not very significantly. This is likely because the location and magnitude of the high-frequency resonance is more dependent on the tie-line length rather than the grid parameters. This can be seen in the frequency response plot in Fig. 7.13, where increasing the SCR has a very limited effect on the HF resonant peak. The CHiL results in Fig. 7.14 also show that, although slightly higher power can be achieved when the grid is strengthened, the HF resonance is still present and ultimately destabilizing, even with a strong grid, SCR = 10.

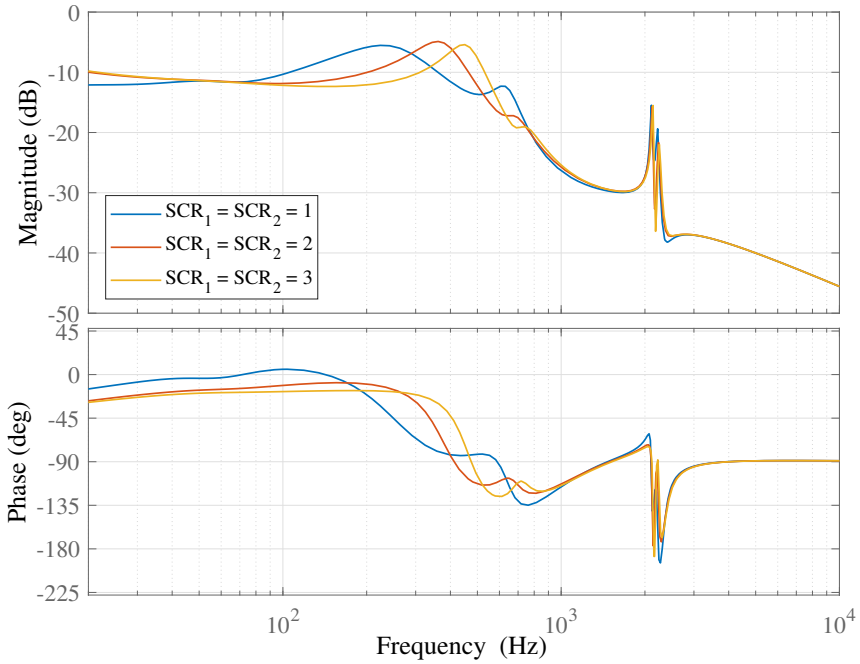

Fig. 7.13: Frequency response of $P_{ref,1}$ to P_1 with varying grid SCR.

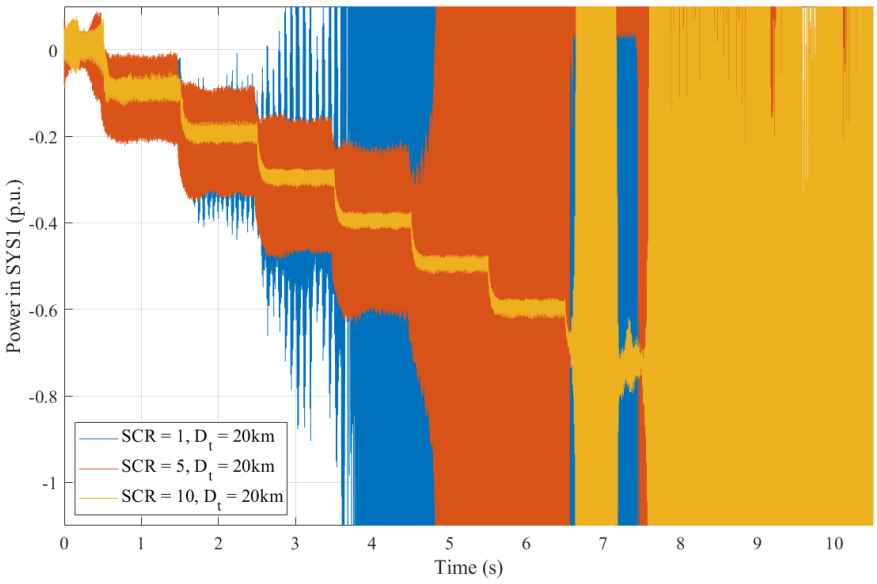

Fig. 7.14: CHiL experimental results of SYS1 active power steps in inverting mode with strong coupling (D_t = 20 km) and varying grid SCR.

Effect of Switching Frequency

The additional destabilization of the CHiL system is also somewhat dependent on switching frequency. The above tests were all performed with $f_{sw} = 10$ kHz. If this is increased to $f_{sw} = 15$ kHz, the system is slightly more stable, as shown in Fig. 7.15. Under these conditions, the minimum D_t for some power transfer to be possible in SYS1 is now ~ 18 km. However, this value of f_{sw} is higher than is realistically feasible to be implemented in hardware. If f_{sw} is reduced below 10 kHz, stability deteriorates even further and D_t must be kept much longer to maintain stability in the system.

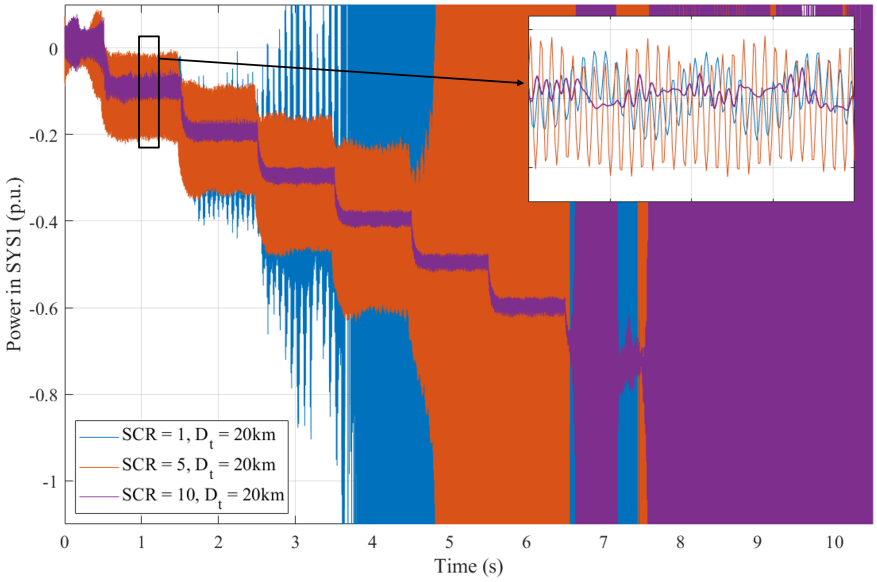

Fig. 7.15: CHiL experimental results of SYS1 active power steps in inverting mode with strong coupling ($D_t = 20$ km) and varying VSC switching frequency

7.7 Summary

This chapter has examined the stability and feasible control operating region of a dual-infeed VSC-HVDC system in a very weak AC grid. When compared to a single-infeed system, the presence of an additional VSC-HVDC link in close electrical proximity does not degrade the stability or power transfer capability of the link under study as long as the tie-line between the dual infeeds is greater than a certain critical value. If the tie-line

is below this critical value, a high-frequency resonance is generated which destabilises the network and prevents any power flow in the link under study. Because of the effect of this resonance, stability is more dependent on the tie-line length than the grid SCR, but the stability can be improved slightly by increasing the switching frequency of the VSCs. In any case, the original system (SYS1) must be re-tuned when operating as a dual-infeed system rather than as single-infeed. When performing analytical modelling, the destabilising effect of the high-frequency resonance must be taken into account by introducing a time delay in the small signal model that is representative of the time delay in the real hardware system. These stability and resonance results have been validated with CHiL experimental tests with a PLECS RTDS and individual microcontrollers for each VSC control.

Chapter 8

Conclusions

8.1 General Conclusions

This work has studied a range of modelling, control and analysis methods for VSC-HVDC in very weak AC grids at a much broader range of operating points than has previously been considerd. In Chapter 3, linearised small-signal models for VCC, PSC and VSM control were developed, as were linearised models of the VSC, RCL filter and simplified AC grid. These models were validated with time-domain simulations and form the baseis of the analytical modelling performed in the rest of the thesis.

Chapter 4 established the active power transfer limits for classical vector control of VSC-HVDC a broad range of controller operating points. The interactions between inner and outer control loops and the PLL were studied showing that all aspects of the controller have a significant impact on system stability. This analysis also isolated distinct stable operating regions for the PLL tuning to allow for use of established VCC-VSC technologies in AC grids with fluctuating impedance and variable control requirements. Stable operating and dynamic performance regions were established for VCC-VSC, within which stability can be guaranteed at a given active power transfer level and minimum dynamic performance requirements are met. This research suggested that certain intermediate PLL bandwidths (approx. 5 – 30 Hz) should be avoided and that control tunings should be customized for inverting and rectifying operation. Overall, conventional VCC was shown to perform much better than is currently as-

sumed and was able inject nominal active power to a very weak AC grid with no modifications to the controller structure.

Chapter 5 presented a comprehensive evaluation of power-synchronization control for VSC-HVDC in very weak AC grids. The active power transfer limits in both inverting and rectifying mode were assessed in terms of the coupled impacts of the power synchronization loop, AC control loop and high-pass current filter gains. This revealed that the high-pass filter has the potential to increase the stable operating region if carefully tuned, and has a larger impact at high PSL or AVL bandwidth. The robustness of PSC to the system SCR examined and showed that PSC is more robust in weak AC grids than strong AC grids, ,and in strong grids the HPF tuning is particularly critical. A smaller operating region which also provides good dynamic performance was also isolated. This region is mostly limited by the PSL gain which can cause large overshoots if tuned too high. In an SCR = 1 AC grid, active transfer of 1.0 p.u. active power in inverting mode and 0.95 p.u. power in rectifying mode was possible, assuming the converter voltage is slightly overrated. At the highest rectifying power levels, dynamic performance was significantly degraded. It was also found that a slower PSL and AVL increases stability and achievable active power transfer, but degrades dynamic performance. CHiL RTDS experiments were used to validate the stable operating region and the dynamic performance of the controller.

In Chapter 6, a standardized assessment framework has been developed for performance analysis of any VSC controller at the design or implementation stage. The modular assessment format accommodates all controllers from analytical models at the design stage to pre-tuned 'black box' controllers installed in a real AC grid system. Three stages of assessment are proposed to perform tuning, time-domain and frequency-domain analyses. CHiL RTDS experiments have been performed to compare the active power limits, dynamic response to power and voltage changes, robustness to grid impedance and the frequency disturbance response. In the third stage, the Jacobian transfer function matrices and impedance matrices were extracted to compare cross-coupling, condition of the process and resonances. An example analysis of VCC, PSC and VSM control using the proposed framework has shown that these strategies of-

fer comparable performance in steady-state, non-fault conditions, but the grid-forming controllers give a slower response. VCC is the most robust strategy for sag conditions or changes in grid impedance but demonstrates strong cross-coupling in the frequency domain.

Finally, Chapter 7 has directly compared the performance of single- and dual-infeed VSC-HVDC in very weak AC grids. When an additional infeed is connected, the system must be re-tuned to optimise performance, but if this is done correctly then the dual-infeed system can offer comparable or improved stability compared to the single-infeed system. However, there is a limitation on the maximum electrical proximity of the dual-infeed links (modelled as a minimum tie-line length) due to the high-frequency resonance present in the system. This resonance is strongly destabilising when $D_t < 20$ km. When performing small-signal analysis on the dual-infeed system it is vital that the system time delays are included in the analytical model else the impact of this resonance will be underestimated, leading to an overestimation of stability. These dual-infeed results have been validated with CHiL and RTDS experiments.

8.2 Author Contributions

The key contributions resulting from the work undertaken in this thesis include:

- Comprehensive analysis of the power transfer limits, control interactions, dynamic performance and grid-impedance robustness of vector current control for VSC-HVDC in very weak AC grids.
- In-depth analysis of the control interactions of power synchronisation control for VSC-HVDC and an examination of the influence of controller tuning on dynamic performance, robustness and active power transfer.
- Development of a novel assessment framework for VSC-HVDC control which is standardized and applicable to all grid-following and grid-forming VSC-HVDC control methods.
- Direct comparison of dual- and single-infeed VSC-HVDC systems for maximum

active power transfer across a broad range of controller tuning operating points.

- Comparison of the joint effects of tie-line length (i.e. strength of coupling) and AC grid SCR on the maximum active power transfer of dual-infeed VSC-HVDC in a very weak AC grid.

- Analysis of the high-frequency resonance introduced by dual-infeed VSC-HVDC in a very weak AC grid and the critical importance of time delays for the accurate modelling of this resonance.

8.3 Future Work

The work presented in this thesis can help to better control existing VSC-HVDC in weak AC grids, and to integrate more VSC-HVDC links into power networks in the UK and the rest of the world. Further research which would help this aim by building on the findings in this thesis include:

- Investigating the effect of using alternative topologies of VSC-HVDC in very weak AC grids. The latest modular multilevel converters (MMCs) are significantly more complex than the two-level converter employed in this work, with up to 401 voltage levels in the full-bridge form [79]. This introduces interactions and stability phenomena that will require the development of a new set of modelling, analysis and evaluation tools to fully analyse their effect in a weak AC system with multiple VSC-HVDC converters in close electrical proximity. Grid-forming control methods such as PSC and VSM control are also likely to have different behaviours when employed with more complex MMC-VSCs.

- Application of the proposed standarized assessment framework to assess a VSC-HVDC converter controller already in operation with full-power hardware e.g. the VSC stations for the Caithness-Moray HVDC link which terminates in a weak AC grid. This could be used to compare the performance of the existing control strategy implemented in power hardware with other alternative control methods.

- Expansion of the dual-infeed investigations in Chapter 7 to assess more complex integration of multiple HVDC infeeds terminating in weak AC grids. This could include hybrid LCC-HVDC and VSC-HVDC systems, islanded networks and comparison with multi-terminal HVDC.
- Analysis of the DC link dynamics and how these may affect the stability limits found in this work.
- Investigation into the effects of filter time constants and structures in all types of grid-following and grid-forming controllers studied.

These future studies should take into account the stable controller operating regions established in this work and look to include novel control strategies that are constantly being proposed and adapted in both academic literature and industry implementation.

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Appendix A

Appendix

A.1 AC Grid Linearized Equations

The governing equations for the grid-connected VSC system shown in Fig. 3.1 are,

$$L_c \frac{di_{cd}}{dt} = u_{fd} - R_c i_{cd} - u_{cd} + \omega L_c i_{cq} \tag{A.1}$$

$$L_c \frac{di_{cq}}{dt} = u_{fq} - R_c i_{cq} - u_{cq} - \omega L_c i_{cd} \tag{A.2}$$

$$C_f \frac{du_{fd}}{dt} = i_{gd} - i_{cd} + \omega C_f u_{fq} \tag{A.3}$$

$$C_f \frac{du_{fq}}{dt} = i_{gq} - i_{cq} - \omega C_f u_{fd} \tag{A.4}$$

$$L_g \frac{di_{gd}}{dt} = u_{fd} - R_g i_{gd} + u_{gd} + \omega L_g i_{gq} \tag{A.5}$$

$$L_g \frac{di_{gq}}{dt} = -u_{fq} - R_g i_{gq} + u_{gq} - \omega L_g i_{gd} \tag{A.6}$$

Linearizing,

$$sL_c \Delta i_{cd} = \Delta u_{fd} - R_c \Delta i_{cd} - \Delta u_{cd} + \omega L_c \Delta i_{cq} \tag{A.7}$$

$$sL_c \Delta i_{cq} = \Delta u_{fq} - R_c \Delta i_{cq} - \Delta u_{cq} - \omega L_c \Delta i_{cd} \tag{A.8}$$

$$C_f \Delta u_{fd} = \Delta i_{gd} - \Delta i_{cd} + \omega C_f \Delta u_{fq} \tag{A.9}$$

$$C_f \Delta u_{fq} = \Delta i_{gq} - \Delta i_{cq} - \omega C_f \Delta u_{fd} \tag{A.10}$$

$$sL_g\Delta i_{cd} = -\Delta u_{fd} - R_g\Delta i_{cd} + \Delta u_{gd} + \omega L_g\Delta i_{cq} \tag{A.11}$$

$$sL_g\Delta i_{cq} = -\Delta u_{fq} - R_g\Delta i_{cq} + \Delta u_{gq} - \omega L_g\Delta i_{cd} \tag{A.12}$$

A.2 Impedance Model Derivation

Current loop law for the d-axis:

$$\Delta u^c_{cd} = -F_{CL}(s)\big(\Delta i_{cdref} - \Delta i^c_{cd}\big) + \Delta u^c_{fd} + \omega L_c\Delta i^c_{cq} \tag{A.13}$$

Converting the converter and grid voltages and currents to the grid frame using the linearised Park transformation in () gives,

$$\Delta u_{cd} + u_{cqo}\Delta\theta_{pll} = -F_{CL}(s)\big(\Delta i_{cdref} - \Delta i_{cd} - i_{cqo}\Delta\theta_{pll}\big) + \Delta u^f_{fd} + \omega L_c\Delta i_{cq} - i_{cdo}\Delta\theta_{pll} \tag{A.14}$$

where the filtered grid voltage is,

$$\Delta u^f_{fd} = H_{u\text{-}dd}(s)\Delta u_{fd} + H_{u\text{-}qd}(s)\Delta u_{fq} \tag{A.15}$$

and,

$$\begin{aligned} H_{u\text{-}dd}(s) &= \frac{s\tau_f + 1}{(s\tau_f + 1)^2 + (\omega\tau_f)^2} \\ H_{u\text{-}qd}(s) &= \frac{\omega\tau}{(s\tau_f + 1)^2 + (\omega\tau_f)^2} \end{aligned} \tag{A.16}$$

Substituting this control equation into the linearised grid equations gives,

$$\begin{aligned} \big(F_{CL}(s) + R_c + sL_c\big)\Delta i_{cd} = F_{CL}(s)\Delta i_{cdref} + \big(\omega L_c i_{cd0} - F_{CL}(s)i_{cq0} + u_{cqo}\big)G_{pll}(s)\Delta u_{fq} \\ + (1 - H_{u\text{-}dd}(s))\Delta u_{fd} - H_{u\text{-}qd}(s)\Delta u_{fq} \end{aligned} \tag{A.17}$$

$$\begin{aligned} \therefore \Delta i_{cd} = \frac{F_{CL}(s)}{\big(F_{CL}(s) + R_c + sL_c\big)}\Delta i_{cdref} + \frac{1 - H_{u\text{-}dd}(s)}{\big(F_{CL}(s) + R_c + sL_c\big)}\Delta u_{fd} \\ + \frac{G_{pll}(s)\big(\omega L_c i_{cd0} - F_{CL}(s)i_{cq0} + u_{cqo}\big) - H_{u\text{-}qd}(s)}{\big(F_{CL}(s) + R_c + sL_c\big)}\Delta u_{fq} \end{aligned} \tag{A.18}$$

Repeating for the q-axis,

$$\Delta i_{cq} = \frac{F_{CL}(s)}{\big(F_{CL}(s) + R_c + sL_c\big)}\Delta i_{cqref} + \frac{1 + G_{pll}(s)\big(u_{cdo} - \omega L_c i_{cq0} - F_{CL}(s) i_{cd0}\big)}{\big(F_{CL}(s) + R_c + sL_c\big)}\Delta u_{fq} \tag{A.19}$$

However,

$$F_{CL}(s) = k_{p-I} + \frac{k_{i-I}}{s} = \frac{L_c}{\alpha} + \frac{R_c}{s\alpha}$$

$$\therefore \frac{F_{CL}(s)}{F_{CL}(s) + R_c + sL_c} = \frac{1}{1 + s\alpha}$$

$$\therefore \Delta \mathbf{i_c} = \underbrace{\begin{bmatrix} \frac{1}{1+s\alpha} & 0 \\ 0 & \frac{1}{1+s\alpha} \end{bmatrix}}_{\mathbf{G_c}(s)} \Delta \mathbf{i_{cref}} + \underbrace{\begin{bmatrix} \frac{1-H_{u\text{-}dd}(s)}{F_{CL}(s)+R_c+sL_c} & \frac{aG_{pll}(s)-H_{u\text{-}qd}(s)}{F_{CL}(s)+R_c+sL_c} \\ 0 & \frac{1+bG_{pll}(s)}{F_{CL}(s)+R_c+sL_c} \end{bmatrix}}_{\mathbf{Y_i}(s)} \Delta \mathbf{u_f} \tag{A.20}$$

The transfer function matrix from $\Delta \mathbf{u_f}$ to $\Delta \mathbf{i_{cref}}$ is derived from consideration of the outer loop control laws. For the d-axis,

$$\Delta i_{cdref} = F_P(s)\big(\Delta P_{ref} - H(s)\Delta P\big) \tag{A.21}$$

$$\Delta i_{cdref} = -1.5H(s)F_P(s)\big(i_{cd0}\Delta u_{fd} + i_{cq0}\Delta u_{fq} + u_{fd0}\Delta i_{cd}\big) \tag{A.22}$$

$$\begin{aligned}\Delta i_{cdref} = -1.5H(s)F_P(s)\big(i_{cd0}\Delta u_{fd} + i_{cq0}\Delta u_{fq} + u_{fd0}(g_c(s)\Delta i_{cdref} \\ + y_{dd}(s)\Delta u_{fd} + y_{qd}(s)\Delta u_{fq})\end{aligned} \tag{A.23}$$

$$\begin{aligned}\Delta i_{cdref}\big(1 + 1.5H(s)F_P(s)u_{fd0}g_c(s)\big) = -1.5H(s)F_P(s)\big((i_{cd0} + u_{fd0}y_{dd}(s))\Delta u_{fd} \\ + (i_{cq0} + u_{fq0}y_{qd}(s))\Delta u_{fq}\big)\end{aligned} \tag{A.24}$$

$$\implies \Delta i_{cdref} = -G_{pd}(s)\Delta u_{fd} - G_{pq}(s)\Delta u_{fq} \tag{A.25}$$

where,

$$G_{pd}(s) = \frac{1.5H(s)F_P(s)(i_{cd0} + u_{fd0}y_{dd}(s))}{1 + 1.5u_{fd0}g_c(s)F_p(s)H(s)}$$

$$G_{pq}(s) = \frac{1.5H(s)F_P(s)(i_{cq0} + u_{fd0}y_{qd}(s))}{1 + 1.5u_{fd0}g_c(s)F_p(s)H(s)} \tag{A.26}$$

$$F_P(s) = k_{p-P} + \frac{k_{i-P}}{s}$$
$$F_U(s) = k_{p-U} + \frac{k_{i-U}}{s}$$

For the q-axis,

$$\Delta i_{cqref} = F_U(s)\big(\Delta U_{ref} - H(s)\Delta U\big) \tag{A.27}$$

$$\Delta i_{cqref} = -H(s)F_U(s)(\frac{u_{fd0}}{u_m}\Delta u_{fd} + \frac{u_{fq0}}{u_m}\Delta u_{fq}) \tag{A.28}$$

$$\implies \Delta\mathbf{i_{cref}} = \underbrace{\begin{bmatrix} -G_{pd}(s) & -G_{pq}(s) \\ -H(s)F_U(s)\frac{u_{fd0}}{u_m} & -H(s)F_U(s)\frac{u_{fq0}}{u_m} \end{bmatrix}}_{\mathbf{G_0(s)}} \Delta\mathbf{u_f} \tag{A.29}$$

A.3 Standardized Assessment Framework Gains

Table A.1: Fixed controller gain values for the standardized assessment framework.

Controller	Parameter	Fixed
VCC	α_c (s)	0.0015
	k_{p-P}	1×10^{-6}
	k_{p-U}	2×10^{-2}
PSC	α_v (rad/s)	40
VSM	k_{p-Uv}	1