Modelling of MMC-HVDC System for EMT Study

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

The modular multilevel converter (MMC) technology has been a subject of increasing importance for high voltage direct current (HVDC) systems due to its technical advantages in terms of scalability, performance and efficiency. There are already several MMC-HVDC projects in construction and operation worldwide. Offline and real-time simulations of MMC-HVDC systems prior to project construction are important for both power system operators and electrical equipment suppliers. In electromagnetic-transients (EMT) simulations, significant simulation challenges are brought by MMC-HVDC systems since a large number of sub-modules (SMs) in each MMC have to be simulated individually. Therefore, a detailed investigation on MMC-HVDC modelling methods is of great theoretical and engineering values.

In this thesis, the half-bridge (HB) MMC offline (PSCAD) and real-time (RSCAD) models with adjustable number of SMs per arm with generic and customized control functions are developed using different MMC modelling methods, namely, detailed switching, switching function, Thevenin equivalent and averaged models. The developed models are validated against benchmark models from PSCAD software libraries for accuracy during steady-steady operation, and AC and DC short circuit faults. Simulation efficiencies of different HB-MMC models are compared for offline PSCAD simulation. The comprehensive comparison of the offline simulation waveforms proves that the averaged and switching function HB-MMC models produce largely identical results as those from the Thevenin equivalent MMC model in the PSCAD MMC library, but with much greater simulation efficiency.

In this thesis, interoperability of different MMC topologies, namely, the HB, full-bridge (FB) and hybrid MMCs are assessed quantitatively. Based on the aforementioned modelling methods, FB and hybrid MMC simulation models are developed and validated. Offline and real-time three-terminal DC grid models closely resembling the Caithness-Morey-Shetland HVDC system are developed to investigate DC grid power flow control during steady-state and AC faults. Interoperability of different MMC topologies in the DC grid is assessed quantitatively using offline PSCAD and real-time RSCAD simulations.

Furthermore, a frequency-domain small-signal impedance measurement tool in RSCAD is presented to extract the impedances of MMC and connected AC networks for stability assessment. The scenario of a simplified GB AC network connected to an MMC is provided in RSCAD for real-time simulation use. Focusing on grid-connected converter system, the effect of AC cables and MMC time-domain modelling methods on their impedance are investigated. Through impedance measurement and comparison, it has been found that the different time-domain modelling methods of MMC have no significant effect on the impedance of the MMC. Since most frequency-domain analysis for MMC is based on the averaged model, this conclusion provides a theoretical basis for the frequency-domain MMC modelling research.

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Finally, I am most grateful to my parents for their unconditional support and endless love; and I want to extend the best wishes for their health and happiness.

List of abbreviations and symbols

Abbreviations

AC	Alternating Current
AM	Averaged Model
APR	Active Power Regulator
CCSC	Circulating Current Suppression Controller
CIGRE	Council on Large Electric Systems
DC	Direct Current
DCVR	DC Voltage Regulator
EMTP	Electromagnetic Transient Program
FB	Full Bridge
FBSM	Full Bridge Submodule
FD	Frequency-dependent model
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
HB	Half Bridge
HBSM	Half Bridge Submodule
HIL	Hardware In the Loop
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line-Commutated Converter
LPF	Low Pass Filter
MIMO	Multiple-Input-Multiple-Output
MLBS	Maximum-Length Binary Sequence

MMC	Modular Multi-level Converter
NG ETYS	UK National Grid Electricity Ten Year Statement
PCC	Point of Common Coupling
PI	Proportional–Integral
PLL	Phase Locked Loop
PN	Positive and Negative
PR	Proportional Resonant
PWM	Pulse Width Modulation
RMS	Root Mean Square
RTDS	Real Time Digital Simulator
SFM	Switching Function Model
SISO	Single-Input-Single-Output
SM	Submodule
TEM	Thevenin Equivalent Model
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

Symbols (in order of appearance)

V_{dc}	MMC DC link voltage
I_{dc}	MMC DC current
v_{CSM}	SM capacitor voltage
v_{SM}	SM output voltage
v_{ua}	Upper arm voltage of phase A
i_{ua}	Upper arm current of phase A
i_a	AC output current of phase A
v_a	AC output voltage of phase A
L_{arm}	Arm inductance
R_{arm}	Arm resistance

v_{ceq}	Equivalent capacitor voltage
R_C	Equivalent capacitor resistance
v_{th}	Thevenin equivalent voltage
R_{th}	Thevenin equivalent resistance
V_{carm}	Sum of capacitor voltages in one arm
ΔV_{carm}	Ripple of capacitor voltages in one arm
V_{carm}^{*}	Rated arm capacitor voltage
m	AC modulation indix
α_d	DC modulation indix
P	Active power
Q	Reactive power
i_{com}	Common mode current
i_d^a	DC harmonic component of the arm currents
i_h^a	AC harmonic component of the arm currents
V_m	Peak value of the output phase voltage
I_m	Peak value of the output phase current
$\Delta E(t)$	Energy variation on one arm
i_{capUa}	Upper arm equivalent capacitor currents
i_{capLa}	Lower arm equivalent capacitor currents
C_e	Equivalent SM capacitance for each arm
N_{SM}	The number of SMs in each arm
V_h	Historical SM voltage capacitor voltage value
Δt	Simulation time step
V_{mi}	Output voltage of the i^{th} SM of the arm
$I_c(s)$	Norton equivalent current of the converter
$Z_0(s)$	Norton equivalent impedance of the converter
$V_g(s)$	Thevenin equivalent voltage source of the grid
$Z_g(s)$	Thevenin equivalent output impedance of the grid

$V_{per(ABC)}$	Perturbation voltage injected to phase A, B, C
v_{pg}	Measured grid voltage after perturbation injection
i_{pg}	Measured grid current after perturbation injection
Y_{PP}	The “self” admittance of the positive axes
Y_{NN}	The “self” admittance of the negative axes
Y_{PN}	The “cross” admittance from N to P
Y_{NP}	The “cross” admittance from P to N
f_{FD}	Resonance frequency of the FD model
C_{FD}	Equivalent capacitance of the FD model
C_{PI}	Capacitance in pi-section model
f_{PI}	Resonance frequency of the pi-section model

Table of Contents

List of figures

List of tables

Chapter 1 Introduction

1.1 Introduction of HVDC system

The first commercial electrical power generator was a direct current (DC) generator, and consequently, the first power transmission system was constructed using DC [1][2]. Although DC had been developed and applied firstly, alternating current (AC) replaced DC for greater uses driven by the emergence of transformers and induction motors in the 1880s and 1890s [1][2]. Transformers make it very convenient to change the voltage level for transmission and distribution of electrical power. Induction motors are rigid and robust but work only with AC system. It is for these reasons that AC become the universal power transmission system [3][4]. However, for some long-distance transmissions, due to the economic, technical and environmental advantages, high voltage DC (HVDC) can be more advantageous than the AC counterpart [5][6].

Generally, in an HVDC system, power is obtained from an AC network, converted to DC in a converter station, transmitted to the receiving point via overhead lines or DC cables, and then is injected into the receiving AC network through another converter station as schematically shown in Fig. 1.1.

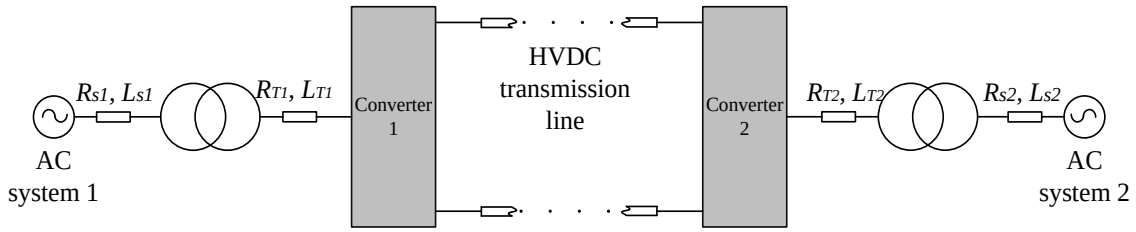


Fig. 1.1 A typical structure for the 2-terminal HVDC transmission

In the HVDC system, the power flow can be controlled accurately and quickly given a set power level and direction. There are many reasons to choose HVDC over HVAC for a particular project, and the considerations involved are also complex. Here are some common reasons for choosing HVDC [3]-[6]:

- Highly efficient long-distance power transmission
- Provision of fully controlled power flow in either direction
- Limited short-circuit currents
- Asynchronous interconnections capability
- Lower environmental impact

The first commercial HVDC transmission project in the world (a 20MW, 100kV submarine DC cable transmission project from mainland Sweden to Gotland) was put into operation in 1954 [7], marking the birth of the first generation of DC transmission technology based on mercury arc valves. In the early 1970s, thyristors began to be used in HVDC power transmission systems and soon replaced mercury arc valves, marking the birth of the second generation of HVDC power transmission technology using line commutated converters (LCC). In 1990, voltage source converters (VSC) based HVDC transmission technology was proposed by researchers at McGill University in Canada [8][9]. Since the 1990s, VSC using high-frequency semiconductor switches with fast gate turn-off capabilities and pulse width modulation (PWM) technology have been used in HVDC transmission, marking the birth of the third generation of HVDC transmission technology [8][9].

The use of VSC as opposed to an LCC offers the following advantages [10]:

- Reactive power compensation is not required by VSC. In addition, VSC can dynamically compensate the reactive power to the AC system.
- Independent control of both active and reactive power.
- VSC offers the possibility to supply passive networks, overcoming the fundamental drawback of LCC as it can only connect to active networks.
- The VSC output voltage has a lower harmonic content. This feature of VSC further reduces the filtering requirements.
- Avoidance of commutation failures due to disturbances in the connected AC network.
- VSC converter station has a smaller footprint than that is required by LCC converter station.

Given that VSC has many advantages and broader application prospects than LCC, most of the HVDC projects currently under construction or being planned are VSC-HVDC schemes. Therefore, this thesis is also focused on VSC-HVDC systems.

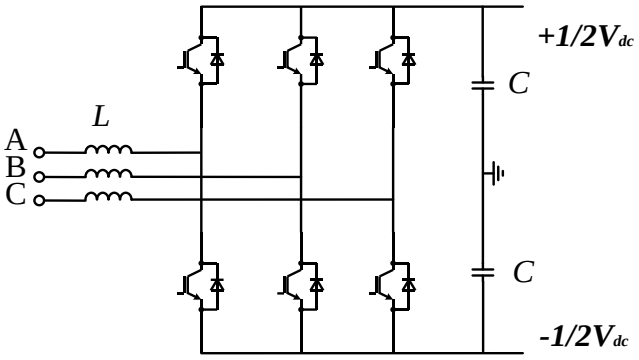
1.2 Different converter topologies in VSC-HVDC

The development of power-electronic and controllable devices in power systems, especially the improvements in the voltage and current ratings of fully controlled power-electronic devices, is expending the applications of VSC-HVDC systems. There are three main VSC structures used in the existing VSC-HVDC projects, namely, two-level converters, three-level converters and modular multi-level converters (MMC).

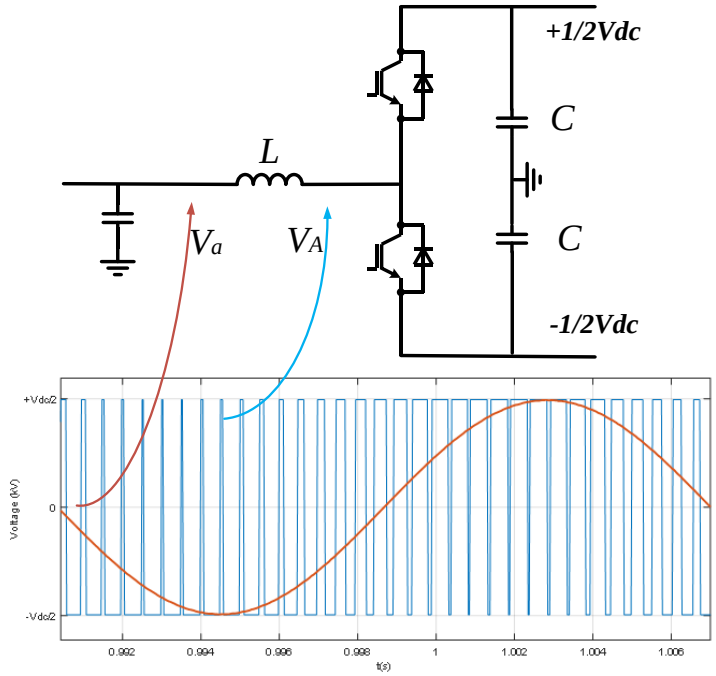
1.2.1 Two-level VSC

The two-level converter has the simplest structure. It has six arms, each of which consists of a switch (IGBT switches are used in this thesis as they are the most used technology) and an antiparallel diode, as shown in Fig. 1.2 (a). With reference to the DC neutral point, the two-level converter phase output has two voltage levels, i.e., $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$. By applying PWM techniques, the output two-level voltage resembles a sine wave fundamental with significant harmonics around the switching frequency and multiple of it, as shown in Fig. 1.2 (b).

A number of VSC-HVDC transmission projects developed by ABB in the 1990s used the 2-level topologies, e.g. the Hällsjön HVDC project, the first test transmission with a $3MW \pm 10kV$ link between Hällsjön and Grängesberg, begin to operate in March 1997; the Gotland HVDC project, the first test commercial transmission, started trial operation in 1999 [10][7]. The typical switching frequency used was 1950Hz [10][7].



(a) Basic structure



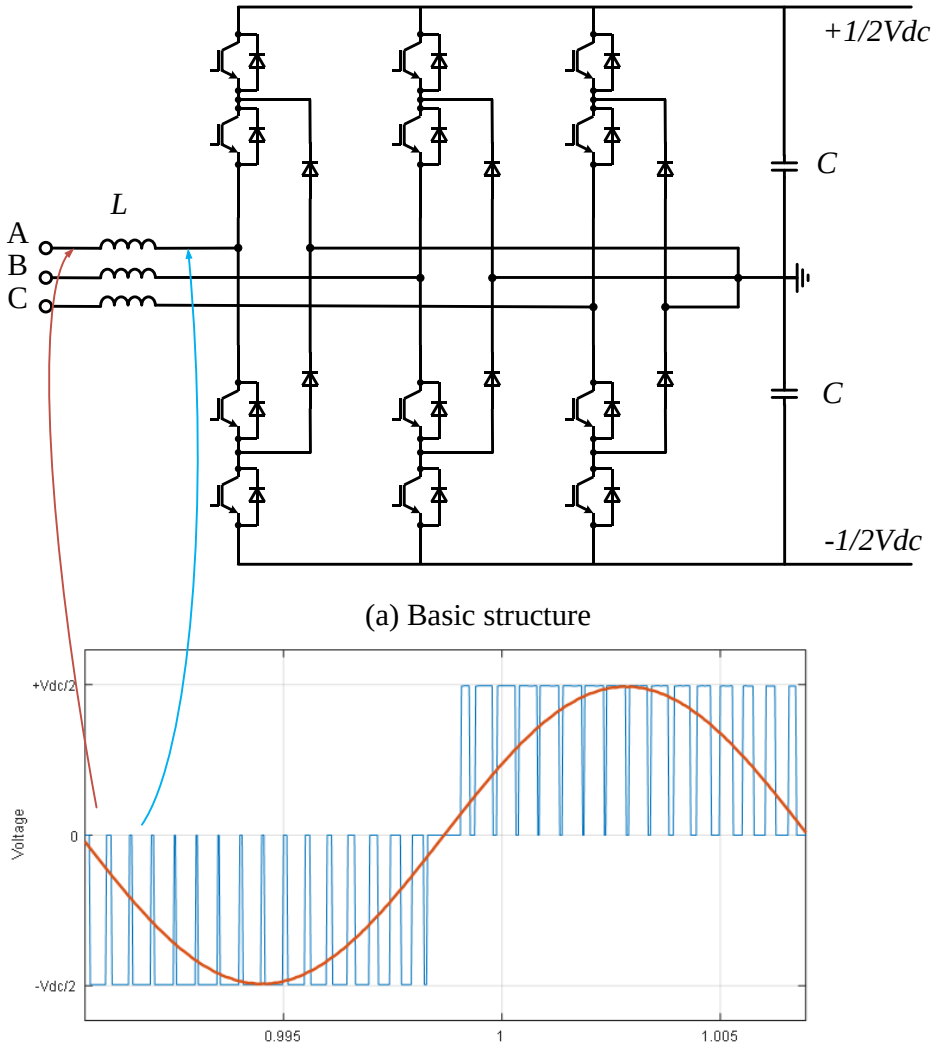
(b) Single phase output voltage

Fig. 1.2 Two-level VSC: basic structure and single phase output voltage

1.2.2 **Three-level VSC**

Fig. 1.3 (a) shows the basic structure of a 3-level diode clamped VSC [11]. Each phase of the 3-level VSC can generate three voltage levels with reference to the DC neutral point, i.e., $+\frac{V_{dc}}{2}$, 0 and $-\frac{V_{dc}}{2}$. The 3-level VSC can produce better quality output voltage waveforms compared to that from 2-level with reduced harmonic contents, as shown in Fig. 1.3 (b). The Eagle Pass 36MW back-to-back VSC-HVDC Project developed by ABB

used such a 3-level configuration, and harmonic elimination PWM technique was used with switching frequency of 1260 Hz [12][13][14].



(a) Basic structure

(b) Single phase output voltage

Fig. 1.3 Three-level VSC: basic structure and output voltage

1.2.3 **Modular multi-level converters (MMC)**

VSC-HVDC systems using the Modular Multilevel Converter (MMC) technology was developed in 2003 [15][16] and was first used in the Trans Bay Cable Project (TBC) in the U.S. in 2010 [17]. MMC contains large numbers of submodules (SMs) in each converter arm, as shown in Fig. 1.4. The typical structure of an SM is also shown in Fig. 1.4. By changing the state of the IGBTs in the SM, the SM can generate an output voltage of with 0 or v_{CSM}. This enables the MMC to generate a sinusoidal voltage from a DC

source as shown in Fig. 1.5 by switching in or out of the SMs in each arm to control the voltage of the phase.

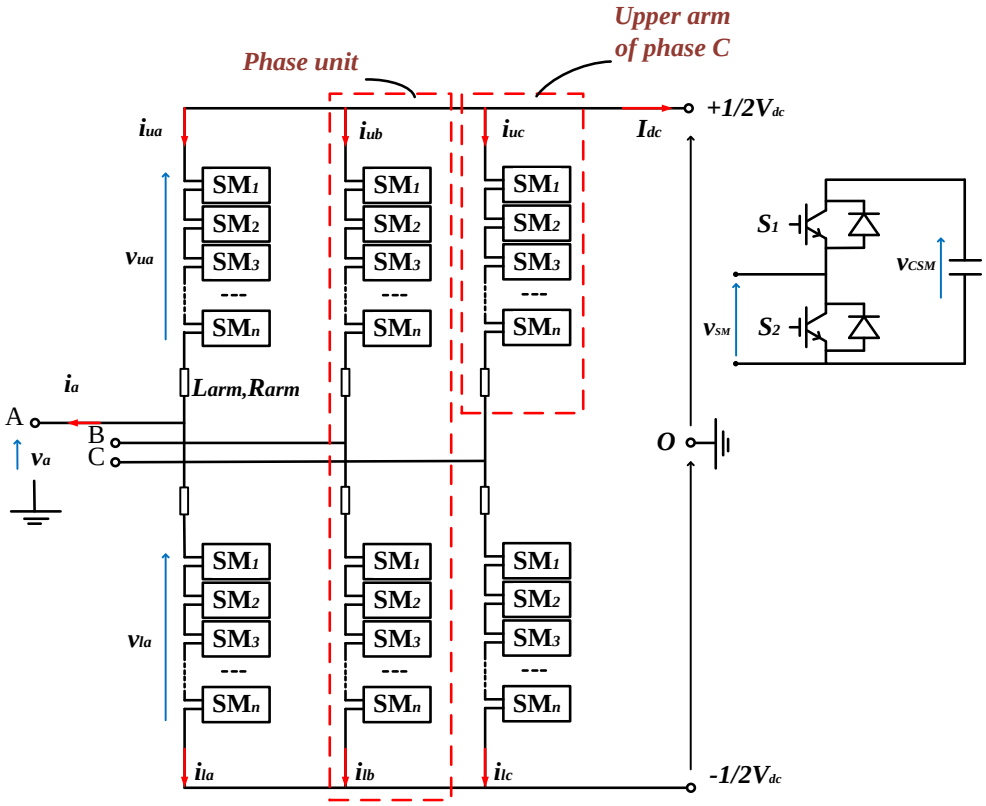


Fig. 1.4 A typical power circuit for the three-phase MMC

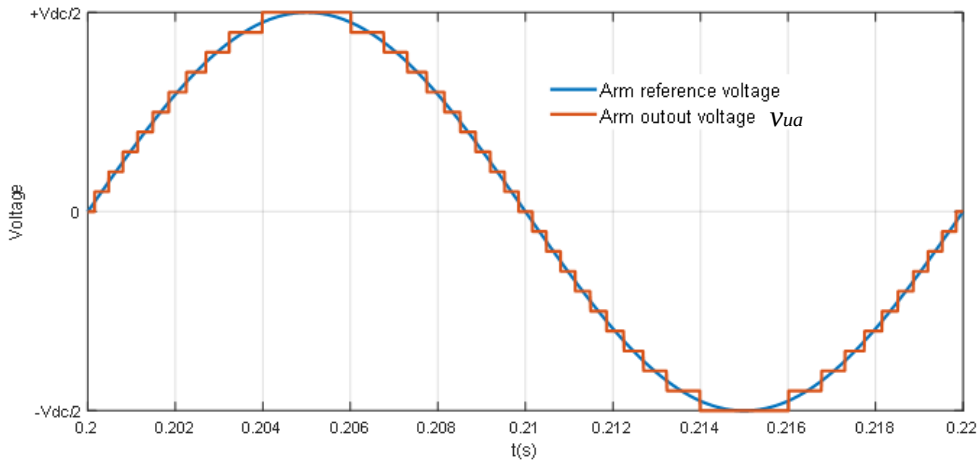


Fig. 1.5 Schematic diagram of staircase modulation of MMC

Compared with traditional 2- and 3-level VSCs, MMC offers significant advantages:

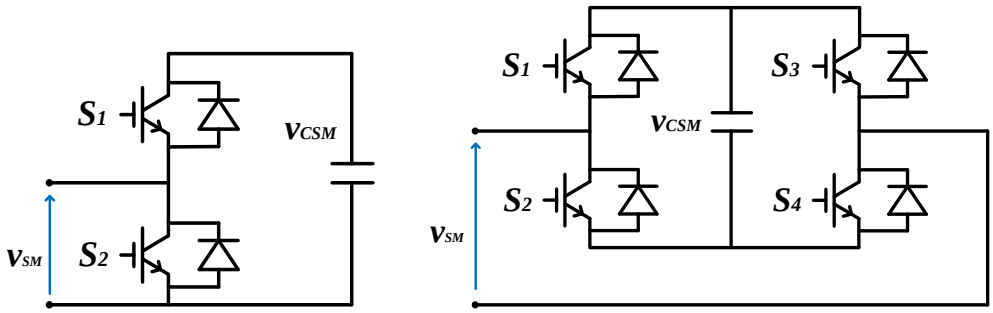
- Modular realization of its power circuit makes scalability to different power and voltage levels simpler by changing the number of SMs per arms [15][16].
- MMC with a large number of SMs generates a sinusoidal output voltage with very low harmonics [16]-[20].
- Because the SMs are switched sequentially, the operating frequency of each semiconductor switch and the voltage step to be switched are reduced so that the switching loss of MMC is very low, accounting for around 30% of the total semiconductor power loss, compared to about 70% for two-level VSCs [21-28].
- The use of distributed SM capacitors instead of concentrated DC link capacitors as in conventional two-level VSCs prevents the SM capacitors from discharging during DC faults [29]. Thus, the fault current from MMC during pole-to-pole DC short circuits is much smaller than the transient discharge current of the concentrated DC link capacitors from the two-level VSC. This is beneficial in easing the design requirement for DC circuit breakers [29][30].

1.3 Different SM topologies of MMC

According to the converter topology used in the SMs, there are 3 main MMC configurations.

In Fig. 1.6 (a), the typical structure of a half-bridge (HB) SM is shown. The output voltage of an HBSM v_{SM} equals to the capacitor voltage v_{CSM} when inserted (S_1 is ON) and approximately equals to zero when bypassed (S_2 is ON). The switching states of the SMs are determined by the control system. When MMC was first proposed, it is HBSM that was used [15][16]. In this thesis, HB-MMC is used to describe MMC with all SMs using HB topology.

The full-bridge (FB) SM as shown in Fig. 1.6 (b) was introduced in [31]. As shown, the output voltage of FBSM has three states: $v_{SM} \approx v_{CSM}$ when positively inserted; $v_{SM} \approx 0$ when bypassed; $v_{SM} \approx -v_{CSM}$ when negatively inserted. The advantage when compared to HB-MMC is that MMC with FBSM has DC fault blocking capability and greater controllability [32]. However, since the number of semiconductor devices of an FBSM is twice that of an HBSM, the devices cost and power losses of FB-MMC are higher compared to HB-MMC [32].



(a) (b)

Fig. 1.6 MMC SM topologies: (a) HBSM, (b) FBSM

By combing FB and HB SMs in each arm, as shown in Fig. 1.7, hybrid MMC was introduced in [33]. As shown, each arm has n SMs, comprising f FBSMs and $(n-f)$ HBSMs. Due to the inclusion of FBSMs (when the number of FBSMs is sufficient), the hybrid MMC can block DC faults while in the same time it has lower losses and capital costs than FB-MMC[34]-[35].

All the three MMC topologies will be studied in this thesis, and detailed descriptions will be provided in the later chapters.

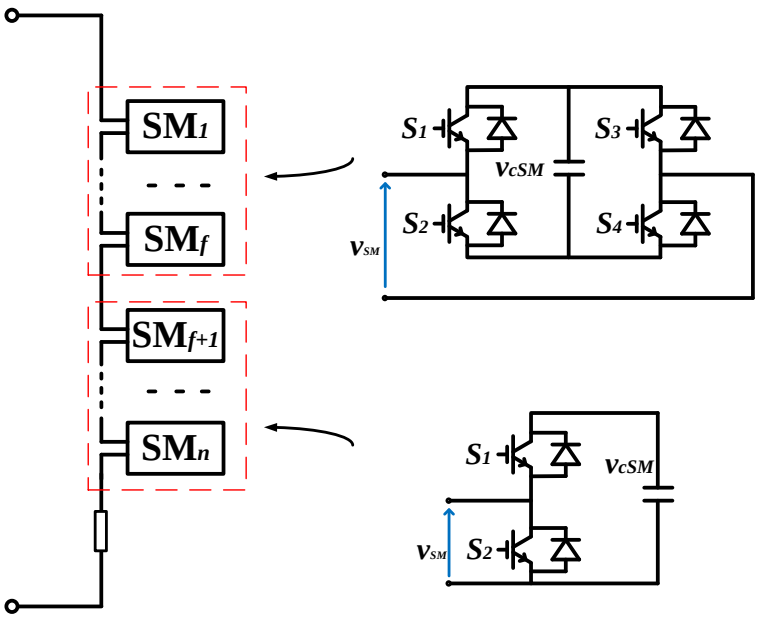


Fig. 1.7 Diagram of an arm of the hybrid MMC

1.4 MMC efficient modelling

1.4.1 MMC modelling challenges

From the above discussions, it is clear that the significant performance improvements and high reliability and availability of the MMC are achieved at the expense of increased complexity of the power circuit and control due to the required large numbers of SMs. Although the use of distributed SM in modular multilevel converter has facilitated the scalability of the converter, it has resulted in the converter with many complex dynamics. There are already several MMC projects in construction and operation worldwide. Simulating MMC prior to project construction is important for both power system operators and electrical equipment suppliers. However, a large number of SM capacitors and switching devices in each MMC present significant simulation challenges, computationally and memory-wise. The challenges of MMC simulation mainly comes from the following two aspects:

- Large numbers of nodes: Due to the large numbers of SMs in each MMC, the electrical node number is very high, which results in large admittance matrix of the converter, and inversing the large-scale matrix is hugely time-consuming during time-domain simulation [36][37][38].
- Internal dynamics of SMs: Switches are switched on and off at high frequency, so the charge and discharge state of each capacitor almost changes at each short simulation step.

1.4.2 MMC efficient modelling methods

Accurate and computational efficient MMC models are therefore required. Many different types of MMC models have been developed in several publications.

1.4.2.1 *Full physical-based model*

The full physical-based model with semiconductor physics models employed can accurately account for converter losses and approximate the switching devices' non-linear characteristics [39]. However, based on the current conventional computing power, it is more suitable for circuit simulation study considering a limited number of SMs rather

than power system simulation study as it can take a very long time to simulate even a single converter [40].

1.4.2.2 *Detailed switching model*

In the detailed switching model, the IGBT switches with anti-parallel diodes are modelled using an ideal controlled switch and two non-ideal diodes as shown in Fig. 1.8. The diodes are modelled as nonlinear resistances using the classical diode function with nonlinear characteristics from manufacturer data sheets or real measurements. By simplifying switching elements, the detailed switching model gains higher efficiency compared with the full physical-based model. However, the full detail model is still not competent for the simulation of systems with many MMCs or large DC grid as the simulation efficiency is still not high enough. This model can be used to verify the accuracy of the further simplified models or to analyse the abnormal operation of SMs [40].

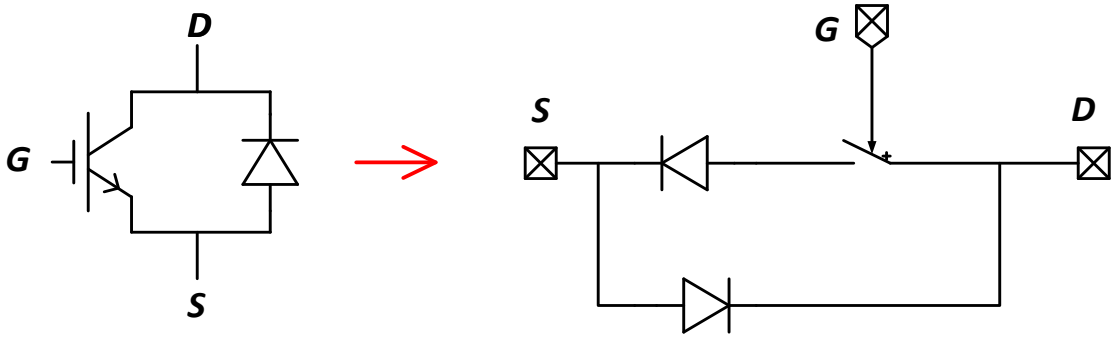


Fig. 1.8 IGBT model in MMC detailed switching model

1.4.2.3 *Thevenin equivalent model*

The Thevenin equivalent model proposed in [37] uses two-state resistance (R_{ON} *and* R_{OFF}) to represent the IGBTs' switching states and uses Electromagnetic Transient Program (EMTP) theory[41] to calculate the dynamics of the SM capacitance so that a whole arm can be represented by a Thevenin equivalent circuit. The goal of this model is to perform Thevenin equivalent of each SM, so as to algebraically superimpose all the SMs in one arm. There are three modelling steps in the Thevenin equivalent model.

The first step is the simplification of switching elements. Based on the detailed switching model, switch elements shown in Fig. 1.9(a) are further simplified. When the IGBT is on, the resistance value of the switching group is equal to R_{ON}, whereas when the switch

group is off, the resistance value is equal to R_{OFF} [42]. Since the parallel connection of an IGBT and a diode acts as a bidirectional switch and only one device is conducting at a given instance, the pair is considered as a single two-state resistance [37]. In [43], different voltages across the IGBT and diode are considered in order to obtain a more accurate value of resistance. However, this does increase the simulation burden while the gain on improved accuracy is limited [40]. The off-state resistance R_{OFF} is typically set to a very higher value, such as $1 \times e^{6}\Omega$ compared with the typical value $1 \times e^{-2}\Omega$ of the on-state resistance R_{ON} [44]. Fig. 1.9 (b) shows the SM model after simplification of the switch elements, where R_1 and R_2 represent the equivalent resistances of upper and lower switching group S_1 and S_2 in the SM respectively. The switching state of each IGBT is determined by the MMC control system which will be discussed in Chapter 2.

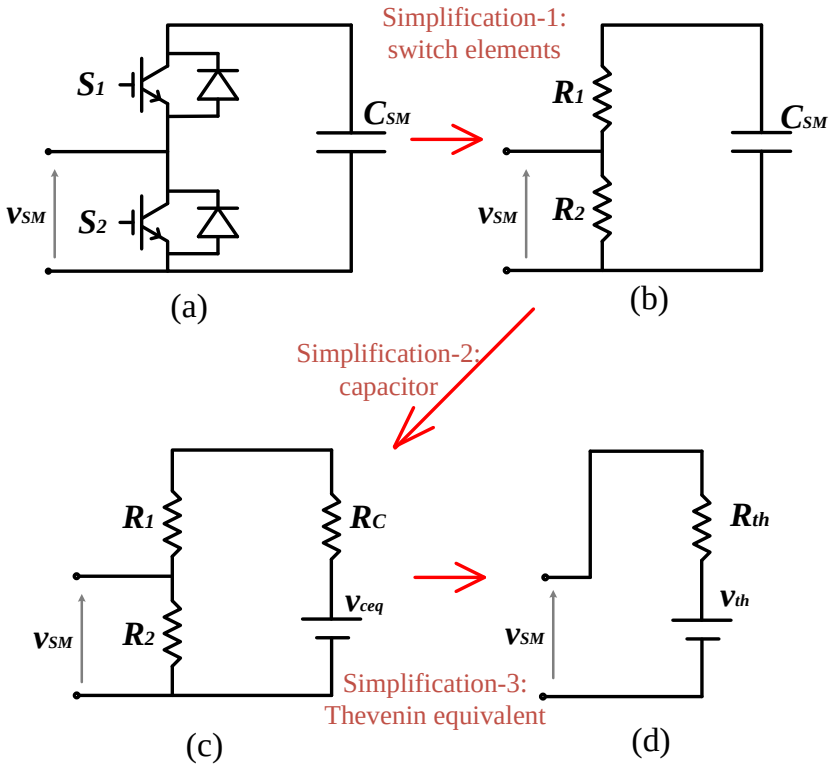
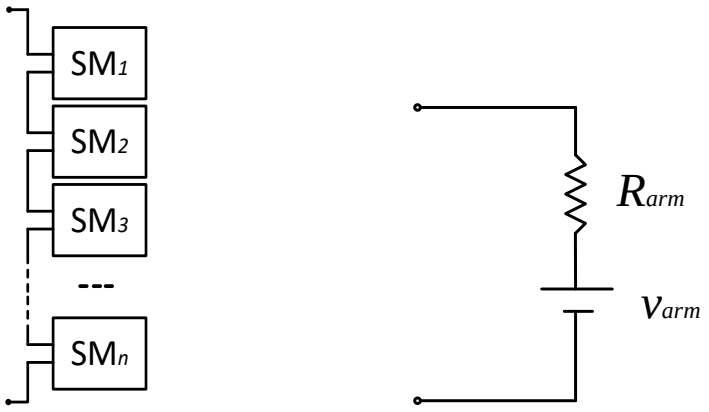


Fig. 1.9 Thevenin equivalent modelling of MMC SM: (a) electrical circuit, (b) switch elements represented by resistances, (c) capacitor represented by equivalent resistance and voltage source, (d) Thevenin equivalent circuit

The second step is to model the capacitors. In addition to implementing the simplification of switching devices, the dynamics of the capacitors need to be discretized for use in the Thevenin's equivalent model. The trapezoidal integration method is most commonly used by Electromagnetic Transient Program (EMTP) to solve the system's different equations [40][37]. This method was first applied to MMC in [37] so that the capacitor can be represented as an equivalent voltage source in series with an impedance [38] as shown in Fig. 1.9 (c). In Fig. 1.9, Thevenin equivalent resistance R_C and equivalent capacitor voltage source v_{ceq} which are both time variant are used to mimic the behaviour of capacitor C_{SM}. R_C and v_{ceq}. In the simulation, the arm current is introduced into the calculation to update and iterate the SM equivalent capacitor voltage v_{ceq} at each simulation time step. The calculation process will be shown in detail in Chapter 3.

The third step is applying Thevenin's theorem to the circuit shown in Fig. 1.9 (c) to obtain the Thevenin equivalent circuit of the SM as shown in Fig. 1.9 (d).

As each SM in the arm is simplified into the Thevenin equivalent circuit shown in Fig. 1.9 (d), combining the capacitor voltage information and the switching state of each SM, SMs connected in series in the arm can be represented by an equivalent voltage source in series with an equivalent resistance as shown in Fig. 1.10. Specific calculation details will be given in Chapter 3.



(a) (b)

Fig. 1.10 Thevenin equivalent modelling of MMC arm: (a) n SMs in one arm, (b) equivalent circuit of n SMs

In Thevenin equivalent model, each arm is represented by Thevenin equivalent circuit, so that not only the number of electrical nodes is significantly reduced, but also the number of nodes is no longer related to the number of SMs. In [40] and [43], the accuracy of this model has been verified. Variants of the Thevenin equivalent model have also been proposed in [45][46].

1.4.2.4 *Switching function model*

In the Thevenin equivalent model, the modelling step-3 in which the Thevenin's theorem is applied requires the simulation platform to perform Thevenin equivalent operations for each SM. Although Thevenin's equivalent operation has low mathematical complexity, the amount of this operation increases with the number of SMs, and when the number of SMs is large, it can still lead to significant calculation requirement. Switching function model uses switching-function-based simplification instead of Thevenin's theorem to achieve higher efficiency.

In practice, the off-resistance R_{OFF} of the IGBT is significantly larger than the on-resistance R_{ON}., Thus, the off-state of IGBT can be considered as an open circuit ($R_{OFF} = \infty$) with negligible impact on model accuracy [47].

Using the same simplification of switch elements and capacitor as described in Section 1.4.2.3, the SM circuit as shown in Fig. 1.11 is obtained. When the SM is inserted, SM equivalent resistance R_{sf} equals to IGBT on-state resistance R_{ON} plus capacitor equivalent resistance R_C and the SM equivalent voltage v_{sf} equals to capacitor equivalent voltage v_{ceq}; when the SM is bypassed, $R_{sf} = R_{ON}$ and $v_{sf} = 0$. So that the calculation of Thevenin equivalent circuit required in the Thevenin equivalent model is avoided, yielding higher computation efficiency.

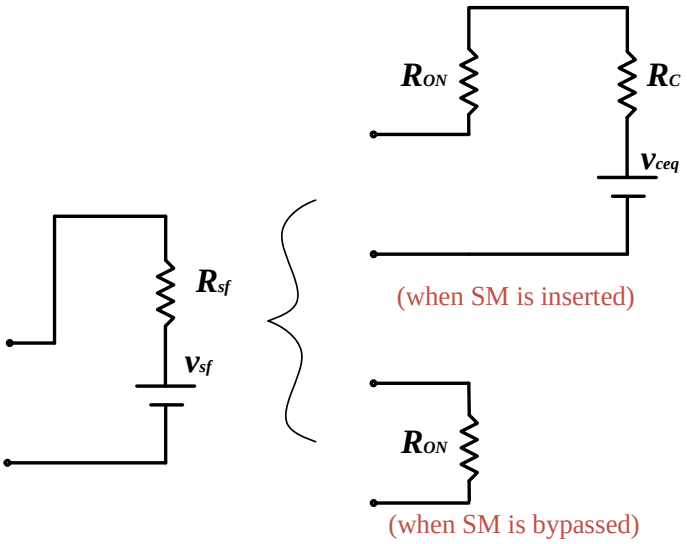


Fig. 1.11 SM equivalent circuit in the switching function model

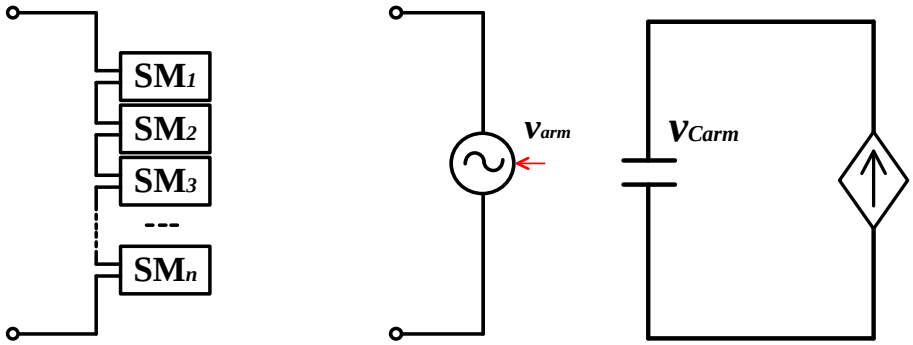
1.4.2.5 *Averaged model*

The generalized averaging method uses simplified functions and controlled sources in order to replicate the average response of the converters [50]. The averaged model has been successfully developed and widely used for modelling wind turbine [51], 3-level VSC [52] and many other areas of power systems [53]. This method was introduced to MMC-HVDC system in [54], and validation against detailed switching models was introduced in [55].

Averaged model maintains the dynamic and steady-state characteristics of the MMC but neglects the individual difference of each SM by assuming that the capacitor voltages are totally balanced among the SMs [55][56][57]. Since IGBTs and diodes are not explicitly modelled and differences of SMs are ignored, dynamics of SM capacitors in one arm are represented by one equivalent capacitor as shown in Fig. 1.12 (c). The controlled current source in Fig. 1.12 (c) is determined by the arm current and the proportion of inserted SMs in the n SMs. According to the voltage of the equivalent capacitor v_{C_arm} and the proportion of inserted SMs in arm, v_{arm} of the equivalent voltage source in Fig. 1.12 (b) is obtained. Details will be discussed in Chapter 3.

This model reduces the number of MMC nodes and greatly simplifies the internal dynamics of the SMs, and thus achieves higher efficiency than the other models. However,

the cost is that the differences between the SMs are ignored, which makes it not suitable for SM level study.



(a) (b) (c)

Fig. 1.12 Averaged MMC arm model: (a) n SMs in one arm, (b) averaged model of n SMs, (c) circuit represent energy dynamics of n SMs

1.5 Real-time digital simulation of MMC

1.5.1 Background

Simulation is an important and necessary step in the development, design and testing of power generation and transmission system. There is a variety of analogue and digital simulation tools available, and different simulation tools are used at various stages of the system development process [40]. The necessity of simulating the electromagnetic transient phenomena in the power system is that such simulation can study the stress on the device and its influence on the power system under abnormal operating conditions.

The traditional analogue transient research method is to utilize the simulator composed of scaled-down power system components connected in a similar way of the real system. Another method is based on the mathematical representation of the system and its dynamics. This kind of digital electromagnetic transients simulation was first described by H. Dommel in 1969 [58]. While unlike the analogue simulators which operate in real-time, most digital simulation platforms operate in non-real-time and the simulation speed depends on the complexity of the model and the computing power that the simulation platform can schedule.

1.5.2 **Real-time simulation of MMC**

1.5.2.1 *Real-time simulation*

A digital real-time simulator needs to solve the model equations for one time-step within the same time in the real-world clock [59]. Because of the characteristics of real-time simulation, this kind of simulation can be full digital simulation or hardware in the loop (HIL) simulation. In [60], a digital simulation platform based on a workstation was introduced to realize the real-time digital simulation of a small-scale power system. The HIL simulation refers to the situation that parts of the system are replaced by actual physical components, which means that physical devices and control platforms, such as power system protection and control devices or power electronics devices, can be connected to the simulated system in a closed-loop. The interaction between the network and protection, control, and power devices during system transients can then be studied in detail. Since the HIL test can be widely used for the development and testing of devices without connecting the device to a real system, this provides real-time simulation with a unique advantage over offline simulations [61]. Because of the broad application prospect of real-time simulation, more complicated calculation methods and more powerful processors have been gradually introduced into this field to realize the real-time digital simulation of large-scale power systems [62].

1.5.2.2 *Real-time digital simulator (RTDS)*

In this thesis, real-time digital simulator (RTDS) developed by RTDS Technologies is used as shown in Fig. 1.13 [62]. RTDS is a combination of real-time operation, flexible I/O, graphical user interface and an extensive library of accurate power system component models allowing engineers to validate the performance of power system devices and de-risk deployment[63].

On the user workstation side, the software RSCAD is used to interact with the simulator to complete tasks such as graphical programming, compilation, code transfer, and data reception. In RSCAD, models built by users using graphical programming are compiled and sent to the simulator. In the simulation device, PB5 and GPC processors are used to perform real-time calculations on the codes downloaded from RSCAD. During the real-time simulation process, the simulator can send the calculation results to RSCAD in real-time for users to read and observe. The physical connections between devices under test

and the simulator are detected and reflected in RSCAD. The RTDS simulator can also connect to physical devices, e.g., protective relays, automation controllers, power electronic controls and power hardware, through analogue & digital I/O or ethernet-based I/O to form HIL test platform.

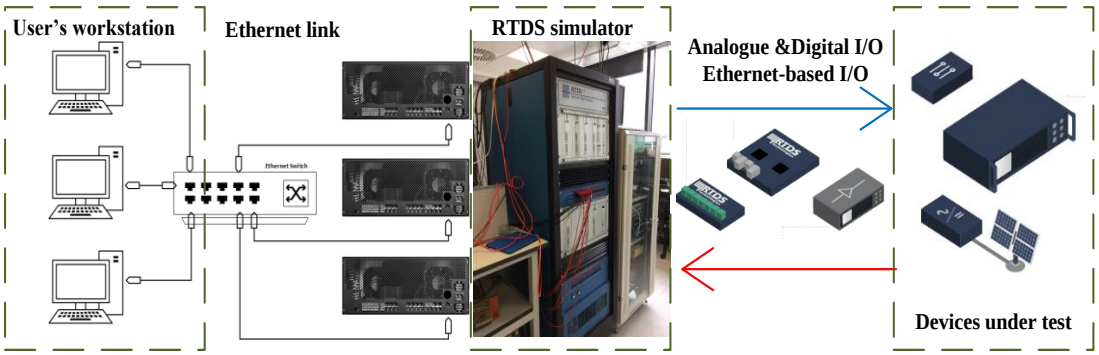


Fig. 1.13 Diagram of RTDS

1.5.2.3 *Simulation of MMC in real-time*

In order to realize the simulation of MMC on the real-time simulation platform, many methods have been proposed [62]-[68]. The common point of these methods is that the internal dynamics of the SMs and SM capacitor voltage balancing control are processed using the Field Programmable Gate Array (FPGA) devices. FPGA devices are more and more used due to the capacity to execute algorithm in parallel. The real-time simulation platform and FPGA form a HIL heterogeneous computing structure to complete the simulation. However, this method has some limitations, such as:

- Increased costs
- Separate coding and modelling on the FPGA and real-time simulation system limits the usability of the whole system

Due to the above reasons, commercial real-time simulation platforms, such as RTDS, have introduced expansion cards integrated with FPGA to implement MMC simulation specifically [67][68]. However, such expansion cards with built-in MMC models lack user-defined flexibility to some extent. In fact, on the RTDS simulation platform, the FPGA based SM-level MMC models lack user-definability, as the averaged model that can be run is provided as "black-box" models with predefined inputs and outputs and with

no access to the internal converter structure and system control by the users. The restricted access to critical internal converter and control system variables that describe system dynamics may hinder understanding of potential issues that may arise at converter and system levels. Therefore, to aid future network development, and identify potential problems and solutions, it is essential that accurate and high-fidelity converter models are available for system studies.

1.6 Small-signal stability assessment of grid-connected MMC systems

It is expected that in the next ten years, HVDC transmission links and converter-interfaced renewable sources will proliferate in the GB network, for example, the Norway-England HVDC link, the Seagreen offshore wind farm, the Dogger Bank wind farm and other projects [69]. The large-scale adoption of power electronic converters paves the way towards modern power grids with high flexibility, sustainability and improved efficiency. However, it will significantly change the characteristics of the GB grid and posing new challenges to the stability of the power system. Compared to traditional synchronous generators where dynamics are dictated by the characteristics of the machines, converter dynamics are mainly established by the converter control structure and gains. Power converters are commonly equipped with multiple control, and grid synchronisation loops for regulating the current and power exchanged with the AC grid [70]. The wide timescale control dynamics of converters can result in a coupled effect with both electromechanical dynamics of electrical generators and electromagnetic transients of power networks and can lead to oscillations across a wide frequency range.

1.6.1 Small-signal stability assessment

In 1976, Middlebrook first presented the criterion that an electrical system is stable if the Nyquist contour of the product of the source impedance and load admittance remains within the unit circle [71]. Since then, impedance-based stability analysis has been used for the power system, and a number of stability criteria have been proposed that include magnitude and phase of the impedance [72][73]. Recent studies have presented that a grid-connected converter system can be considered as a multiple-input-multiple-output (MIMO) system and related identification techniques and stability assessment methods can be used in this study [74][75]. The impedance-based stability criterion of grid-

connected inverters was proposed in [74]. If the ratio between the grid impedance and the converter impedance satisfies the Nyquist stability criterion, the system will remain stable. In order to ensure stability analysis based on this technology, the potential problem is how to obtain accurate system and converter impedances.

1.6.2 **Impedance acquisition**

There are two main ways to obtain impedances, one is to build a small-signal frequency-domain model of the system to be studied, and the other is the measuring method. The two approaches have different advantages and are suitable for various application fields.

Many small-signal MMC models have been proposed [76]-[81]. Based on the averaged MMC model without considering the dynamics of the individual SMs in each arm, converter-level internal dynamics and controllers are modelled in detail. From the detailed mathematical model, when applying small-signal stability analysis using impedances calculated from the analytical models, the effects of different control strategies and different controller parameters on system stability can be studied. However, this method is only valid for those power system devices or components whose internal structure is known. Therefore, it is not possible to obtain the impedance of 'black box' or the devices whose manufacturer keeps the internal structure confidential [82].

Impedance can be measured if adequate time-domain system model is available, and the method is much easier than establishing small-signal models. Thus, extraction of impedance has become more and more important in many applications [72][82][83][84]. Methods of extracting impedance by injecting perturbation signals have been widely used for both AC and DC systems [85]-[94]. For the AC system, the injection techniques are usually applied in DQ-frame [87][88][82][83]. Disturbance signals at different frequencies are injected into the system, and the corresponding frequency response can be measured for impedance calculation. In addition, other types of injection signals are proposed for online grid impedance identification, including the impulse signal, maximum-length binary sequence (MLBS) signals [75][90], PWM signals [92]-[94], and so on.

1.6.3 Impedance-based stability assessment of grid-connected MMC systems

Small-signal impedance measurement and impedance-based stability analysis of grid-connected converter systems have been discussed in several publications. However, in [75][76][95], AC grid is modelled as a 3-phase ideal voltage source in series with an RL branch, whereas in [75][76][82][83][91], the connection cable is either modelled as a simple inductance or being ignored. References [76]-[81] focus on MMC impedance-based stability assessment use averaged MMC model directly without considering the influence of using the simplified models on the impedance. These simplifications ignore many details, which can significantly impact on the impedance characteristics and impedance measurement.

1.7 Research scope and contributions

1.7.1 Research scope

The main purpose of this research work is to develop and validate detailed and accurate offline and real-time RTDS models of MMC and DC grids. Such models deliver a useful platform for a variety of offline and real-time studies to be carried out with good accuracy for real-time implementation without relying on external FPGAs. Impedance measurement of typical AC grid and MMC are also carried out for stability studies.

The main objectives and scopes of this research are as follow:

- To develop detailed SM-level MMC models that can facilitate testing of MMC control and protection solutions in offline and real-time, offer the users the means to use as a strong basis for explorations of multi-vendor schemes. Different modelling methods are applied and compared.
- To examine the suitability of the developed offline and real-time converter models for a detailed assessment of interoperability of MMCs with different topologies in a meshed DC grid.
- To investigate the impedance measurement from the developed time-domain MMC models and typical AC network for assessing the stability of grid-connected converter systems.

1.7.2 Thesis contributions

The main contributions of the thesis can be summarised as follows:

- Detailed submodule (SM) level half-bridge (HB), full-bridge (FB) and hybrid MMC models with adjustable number of SMs per arm and generic and customized control functions are developed and validated against benchmark models from PSCAD software libraries. The developed MMC models can facilitate testing of MMC control and protection solutions in offline and real-time, offer the users the means to use as a strong basis for explorations of multi-vendor schemes.
- Offline and real-time three-terminal DC grid models closely resembling the Caithness-Morey-Shetland HVDC system are developed to investigate DC grid power flow control during steady-state and AC faults. Interoperability of different MMC topologies in a DC grid is assessed quantitatively using offline PSCAD and real-time RSCAD simulations.
- Development of a RSCAD frequency measurement tool to extract impedances of an MMC and connected AC network for stability assessment. The scenario of GB AC network connected to an MMC is given in RSCAD for RTDS based real-time simulation use. Focusing on the grid-connected converter system, how the AC cable and MMC time-domain models that affect the impedance has been explored.

1.8 Organisation of the thesis

This thesis is organised as follows:

Chapter 2 Principles and control of MMC system

The basic principles of MMC systems, including the structure and mathematical model, and the control strategy is presented.

Chapter 3 MMC efficient modelling for electromagnetic transients (EMT) digital simulation

The main modelling methods for simulation of the MMC, namely, detailed switching, switching function, Thevenin equivalent and averaged models are discussed. Focusing on HB-MMC, the aforementioned modelling methods are applied in offline PSCAD and real-time simulator RTDS. Detailed quantitative comparison of HB-MMC modelling

methods are presented offline and real-time considering a normal steady-steady operation, AC and DC short circuit fault. Simulation efficiencies of different HB-MMC models are compared using the offline simulation times.

Chapter 4 Interoperability of different VSC topologies in HVDC grids

The main modelling methods for simulation of the MMC, namely, detailed switching, switching function, Thevenin equivalent and averaged models are developed and validated for FB- MMC and hybrid MMC consisting of 50% FB SMs and 50% HB. The suitability of the developed offline and real-time averaged converter models for the detailed assessment of interoperability of different converters in a meshed DC grid is examined. Interoperability of an HB-MMC, FB-MMC and hybrid MMC are assessed quantitatively using offline PSCAD and real-time RSCAD simulations.

Chapter 5 Extraction of small-signal impedance for stability assessment

In this chapter, an impedance measurement tool in RSCAD is presented to extract the impedances of MMC and connected AC network. A simplified GB AC network is modelled based on real power flow data and is applied in the test system. The impact of AC cables on the AC grid impedance and the influence of MMC modelling methods on the MMC impedance are studied. The method of impedance extraction in time-domain and the impedance-based stability analysis is also shown.

Chapter 5 General conclusions and future work

This chapter draws the conclusions from work presented in the previous chapters and present future work for further investigation in the related subject area.

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Chapter 2 Principles and control of MMC system

In this chapter, the basic principles of MMC systems, including the basic structure and mathematical model of MMC and the control strategy is presented. All the discussions in this chapter are based on the half-bridge MMC. Compared with full-bridge MMC and hybrid MMC, half-bridge MMC needs the least total number of power electronic devices and has the lowest cost under the same capacity [32][34]. These advantages obtained by half-bridge MMC are at the expense of DC fault blocking capability [32][34]. The characteristics of full-bridge and hybrid structures, as well as trade-offs among different topologies, will be discussed in detail in Chapter 4.

2.1 Half-bridge modular multilevel converter

2.1.1 MMC circuit configuration

A typical power circuit for the three-phase MMC is shown in Fig. 2.1 , and the O point represents the zero potential reference point, i.e., DC middle point. The converter has six bridge arms, each of which is composed of an arm inductor and N numbers of SMs, and the upper and lower bridge arms in the same phase form a phase unit. The total blocking voltage of the half-bridge SM capacitors in each MMC arm is $V_{carm} = \sum_{j=1}^{N} V_{C,j} \geq V_{dc}$, where N is the number of half-bridge SMs per arm, $V_{C,j}$ is the capacitor voltage of the jth SM,. Fig. 2.1 also shows the structure of a single half-bridge SM, where v_{SM} is the output voltage of the SM.

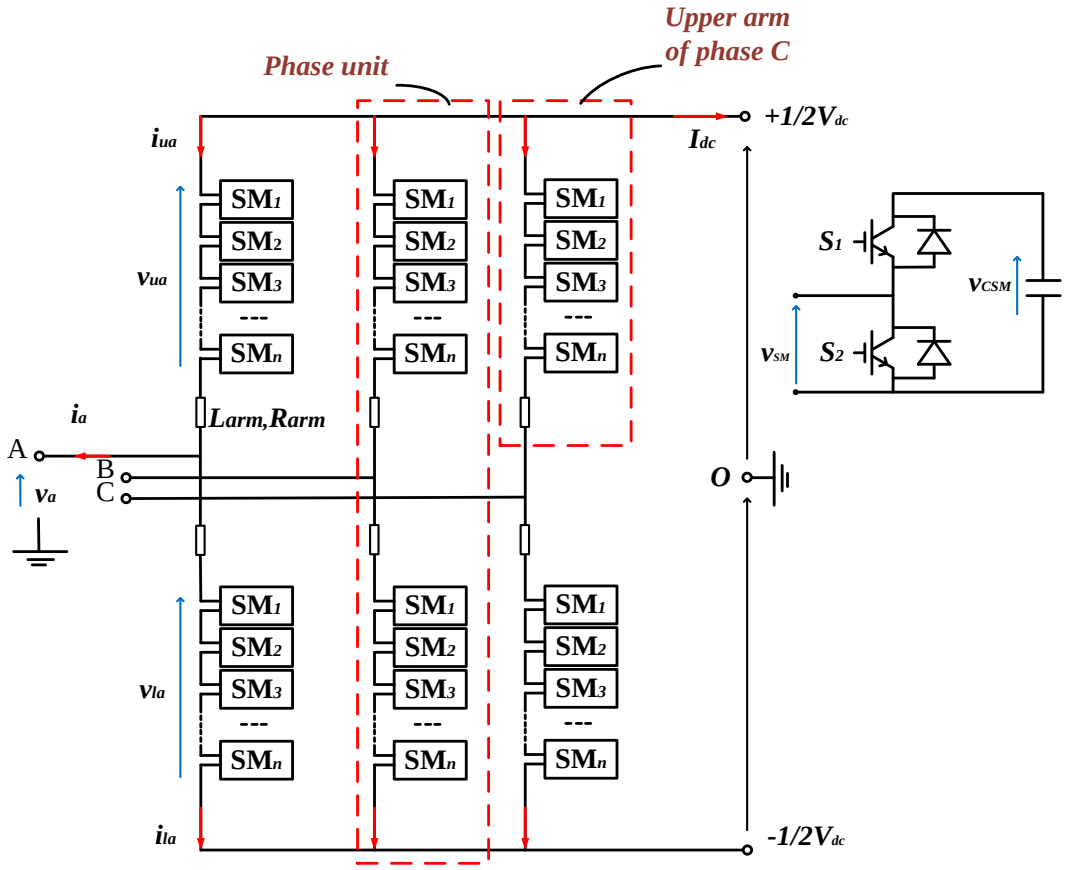


Fig. 2.1 A typical power circuit for the three-phase MMC

2.1.2 **MMC mathematical model**

From Fig. 2.1, the sum of SMs output voltages of the upper and lower arms of phase '*A*' can be expressed as:

$$v_{ua} \approx \frac{1}{2}V_{dc} - R_{arm}i_{ua} - L_{arm}\frac{d}{dt}i_{ua} - v_a \tag{2.1}$$

$$v_{la} \approx \frac{1}{2}V_{dc} - R_{arm}i_{la} - L_{arm}\frac{d}{dt}i_{la} + v_a \tag{2.2}$$

Providing the magnitudes of the AC and DC voltage drops in the arm inductors are much smaller than the DC link voltage V_{dc} and AC output voltage, (2.1) and (2.2) can be approximated as:

$$v_{ua} \approx \tfrac{1}{2}V_{dc} - v_a \approx \tfrac{1}{2}V_{dc} - \tfrac{1}{2}mV_{carm}\sin(\omega t + \delta) \approx \tfrac{1}{2}V_{carm}\left[\alpha_d - m\sin(\omega t + \delta)\right] \tag{2.3}$$

$$v_{la} \approx \tfrac{1}{2}V_{dc} + v_a \approx \tfrac{1}{2}V_{dc} + \tfrac{1}{2}mV_{carm}\sin(\omega t + \delta) \approx \tfrac{1}{2}V_{carm}\left[\alpha_d + m\sin(\omega t + \delta)\right] \quad (2.4)$$

where m and α_d represent AC and DC modulation indices, with $v_a = \tfrac{1}{2}mV_{carm}\sin(\omega t + \delta)$, and $\alpha_d = V_{dc}/V_{carm}$.

Equations (2.3) and (2.4) indicate that the upper and lower arms of each phase of the MMC operate in a complementary manner for their AC outputs.

Subtracting (2.2) from (2.1) yields:

$$v_{la} - v_{ua} = R_{arm}(i_{ua} - i_{la}) + L_{arm}\frac{d}{dt}(i_{ua} - i_{la}) + 2v_a \quad (2.5)$$

From Fig. 2.1, phase 'a' output current 'i_a' can be expressed in terms of its upper and lower arm currents 'i_{ua}' and 'i_{la}' as:

$$i_a = i_{ua} - i_{la} \quad (2.6)$$

Equation (2.6) indicates that the MMC output phase current represents differential components of the upper and lower arm currents.

After substitution of (2.6) in (2.5), the following equation is obtained:

$$\frac{1}{2}(v_{la} - v_{ua}) = \frac{1}{2}R_{arm}i_a + \frac{1}{2}L_{arm}\frac{d}{dt}i_a + v_a \quad (2.7)$$

Combined with (2.3) and (2.4), the differential component of the arm voltages represents the MMC output phase voltage 'v_a', thus:

$$\tfrac{1}{2}\left(v_{la} - v_{ua}\right) = v_a = \tfrac{1}{2}mV_{carm}\sin(\omega t + \delta) \quad (2.8)$$

Additionally, (2.7) indicates that the fundamental current flowing in each MMC phase leg is driven by the differential component of the arm voltages $\tfrac{1}{2}\left(v_{la} - v_{ua}\right)$.

Similarly, adding (2.1) and (2.2) gives:

$$v_{la} + v_{ua} = V_{dc} - R_{arm}(i_{ua} + i_{la}) - L_{arm}\frac{d}{dt}(i_{ua} + i_{la}) \quad (2.9)$$

The simplified (2.3) and (2.4) ignore the SM capacitor voltage ripples. The common-mode voltage of phase A in (2.9) can be rewritten by adding the SM capacitor voltage ripples to the sum of (2.3) and (2.4) as:

$$\alpha_d V_{carm} + \Delta V_{carm} = V_{dc} - R_{arm}(i_{ua} + i_{la}) - L_{arm}\frac{d}{dt}(i_{ua} + i_{la}) \tag{2.10}$$

It is apparent from (2.10) that the common-mode current $i_{com} = \frac{1}{2}(i_{ua} + i_{la})$ comprises of DC component which will be driven by the DC voltage difference between V_{dc} and $\alpha_d V_{carm}$, and AC component which will be driven by the AC voltage ripple in the common-mode voltage, ΔV_{carm}. Introducing common-mode current into (2.10) yields:

$$\alpha_d V_{carm} + \Delta V_{carm} = V_{dc} - 2R_{arm} i_{com} - 2L_{arm}\frac{d}{dt} i_{com} \tag{2.11}$$

After solving (2.6) and i_{com} for the upper and lower arm currents i_{ua} and i_{la}, and expressing the phase 'a' common-mode current terms of its DC and AC components as $i_{com} = I_d^a + i_h^a$, the MMC upper and lower arm currents 'i_{ua}' and 'i_{la}' can be rewritten as:

$$i_{ua} \approx I_d^a + i_h^a + \tfrac{1}{2} i_a \tag{2.12}$$

$$i_{la} \approx I_d^a + i_h^a - \tfrac{1}{2} i_a \tag{2.13}$$

where, I_d^a and i_h^a represent the DC and AC harmonic components of the upper and lower arm currents, respectively. The common-mode current of each phase represents the current component of the arm currents that flow from the upper to lower arm or vice versa, without leaking into output AC circuit. The DC component of the common-mode current is reprehensible for DC power exchange between the MMC and DC side, and its magnitude during normal operation under balanced AC grid voltage can be linked to the DC link current 'I_{DC}' as follows:

$$I_d^a \approx \tfrac{1}{3} I_{dc} \tag{2.14}$$

Alternatively, the DC component of the arm or common-mode current can be derived using the power balance equation, assuming the MMC is lossless, as:

$$P_{dc} = P_{ac} \Rightarrow V_{dc} I_{dc} = \frac{2}{3} V_m I_m \cos\varphi \tag{2.15}$$

where V_m is the peak value of the output phase voltage, I_m is the peak value of the output phase current and φ is the power factor angle. By neglecting the DC voltage drops in the arm inductors and switching devices and assuming the sum of capacitor voltages across each arm is regulated at V_{dc}, the peak phase voltage at the MMC ac terminals (V_m) can be approximated as:

$$V_m = \tfrac{1}{2} m V_{dc} \tag{2.16}$$

After substituting the expression for V_m in (2.16), the alternative expression for I_d^a in (2.17) is derived.

$$I_d^a \approx \tfrac{1}{4} m I_m \cos\varphi \tag{2.17}$$

Assuming the arm current is directly controlled with no second-order harmonic circulating current, the upper arm voltage and current of phase 'a' can be given, respectively, as:

$$v_{ua} = \frac{V_{dc}}{2} - V_m \sin\omega t \tag{2.18}$$

$$i_{ua} = \frac{I_{dc}}{3} + \frac{I_m}{2} \sin(\omega t - \varphi) \tag{2.19}$$

Combining (2.15), (2.16) and (2.19) yields the arm current:

$$i_{ua} = m \frac{I_m}{4} \cos\varphi + \frac{I_m}{2} \sin(\omega t - \varphi) \tag{2.20}$$

The instantaneous power flowing through the upper arm of phase A can be calculated as:

$$p_{ua} = v_{ua} i_{ua} = (\frac{V_{dc}}{2} - V_m \sin\omega t)(m \frac{I_m}{4} \cos\varphi + \frac{I_m}{2} \sin(\omega t - \varphi)) \tag{2.21}$$

Integrating (2.21), the energy variation $\Delta E(t)$ on the upper arm phase A can be expressed as:

$$\Delta E(t) = \frac{V_m I_m}{8\omega} \sin(2\omega t - \varphi) - \frac{V_{dc} I_m}{4\omega} \cos(\omega t - \varphi) + \frac{V_m^2 I_m}{2\omega V_{dc}} \cos\omega t \cos\varphi \tag{2.22}$$

Considering the sum of the capacitor voltages in one arm, there is:

$$\Delta E(t) = \frac{CV_c^2(t) - CV_{c0}^2(t)}{2} \tag{2.23}$$

where C is the equivalent arm capacitance. Assuming the initial sum capacitor voltage V_{c0} is balanced at $V_{carm} = \frac{V_{dc}}{\alpha_d}$, the sum of capacitor voltages $v_{carm\_ua}(t)$ is

$$v_{carm\_ua}(t) = \sqrt{\frac{2\Delta E(t)}{C} + (\frac{V_{dc}}{\alpha_d})^2} \tag{2.24}$$

Combining with (2.22), the sum of capacitor voltages $v_{carm\_ua}(t)$ can be calculated as

$$v_{carm\_ua}(t) = \sqrt{\frac{V_m I_m}{4\omega C}\sin(2\omega t - \varphi) - \frac{V_{dc} I_m}{2\omega C}\cos(\omega t - \varphi) + \frac{V_m^2 I_m}{\omega V_{dc} C}\cos\omega t \cos\varphi + (\frac{V_{dc}}{\alpha_d})^2} \tag{2.25}$$

2.2 MMC control system

This section presents the synthesis of different control layers that have been used in this thesis. A simplified per phase representation of a three-phase MMC shown in Fig. 2.2 is used throughout this section where the total voltage generated by each arm is represented using an equivalent voltage source. The current and power flow directions shown in Fig. 2.2 are considered to be positive.

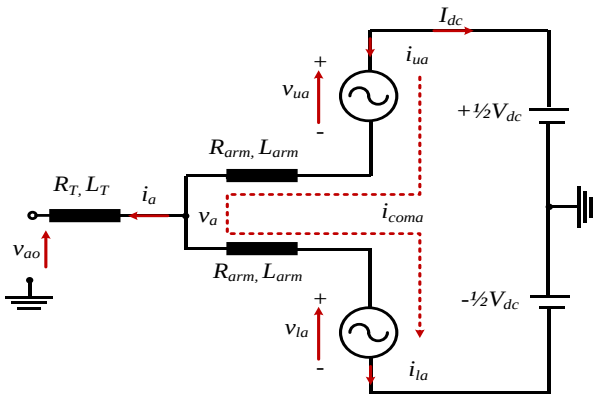


Fig. 2.2 The basic structure of a single-phase MMC

2.2.1 **MMC modelling**

As shown in Fig. 2.2, the following equations are obtained for phase '*a*':

$$\tfrac{1}{2}V_{dc} - v_{ua} - R_{arm}i_{ua} - L_{arm}\frac{di_{ua}}{dt} - v_a = 0 \tag{2.26}$$

$$\tfrac{1}{2}V_{dc} - v_{la} - R_{arm}i_{la} - L_{arm}\frac{di_{la}}{dt} + v_a = 0 \tag{2.27}$$

Similarly, considering the output circuit relative to the DC link mid-point 'o', the following equations are obtained:

$$v_{ao} = R_T i_{ao} + L_T \frac{di_{ao}}{dt} + v_a \tag{2.28}$$

Subtracting (2.26) from (2.27) and merging with (2.28), and with further algebraic manipulations, the following equation is obtained:

$$\tfrac{1}{2}(v_{la} - v_{ua}) = (\tfrac{1}{2}R_{arm} + R_T)(i_{la} - i_{ua}) + (\tfrac{1}{2}L_{arm} + L_T)\frac{d}{dt}(i_{la} - i_{ua}) + v_a \tag{2.29}$$

From the definitions of the arm currents and voltages established earlier on per phase basis, and after substitution of the definitions into (2.29) and assuming that $R_e = (\tfrac{1}{2}R_{arm} + R_T)$ and $L_e = (\tfrac{1}{2}L_{arm} + L_T)$, (2.29) is reduced to:

$$R_e i_{ao} + L_e \frac{di_{ao}}{dt} + v_a = \tfrac{1}{2}V_{carm}m_a \tag{2.30}$$

where *a* can be replaced by *b* and *c* so (2.30) can be represented as three-phase '*abc*'. After application of variant power or constant amplitude Park transformation, (2.30) is transformed into dq synchronous reference frame as:

$$\begin{aligned} R_e i_d + L_e \frac{di_d}{dt} - \omega L_e i_q + v_d &= \tfrac{1}{2}V_{carm}m_d \\ R_e i_q + L_e \frac{di_q}{dt} - \omega L_e i_d + v_q &= \tfrac{1}{2}V_{carm}m_q \end{aligned} \tag{2.31}$$

The last terms of (2.31) can be simplified as: $v_{cd}^* = \tfrac{1}{2}V_{carm}m_d$ and $v_{cq}^* = \tfrac{1}{2}V_{carm}m_q$.

2.2.2 The capacitor voltage balancing algorithm

Voltage balancing among SM capacitors in each arm is one of the main challenges for MMC. The capacitor voltage balancing controller receives the reference from the modulator and selects SMs to be inserted or bypassed based on their capacitor voltages. With the periodic change in the arm current direction, the timing of charging and discharging will also take turns. SMs with lower capacitor voltages are preferentially inserted during the charging cycle, whilst SMs with higher capacitor voltages connected during the discharge cycle, so that the capacitor voltages among the SMs in the arm can remain balanced. This is the basic principle of capacitor voltage balancing control.

There are numerous algorithms that have been developed. Some methods focus on minimizing the computational complexity in order to achieve high efficient since the capacitor voltage balancing algorithm becomes the main issue for SM-level MMC models [96][97]. Reducing the switching frequency is another aim of voltage balancing algorithms [98][107]. In [99], a capacitor voltage balancing strategy is proposed to minimize the AC circulating current. However, the sorting algorithm [19][100] is the most widely used method. In each simulation time-step, the SM capacitor voltages of each arm are measured, listed, and sorted in ascending order. SMs with the lowest capacitor voltages will be switched on when charging and SMs with the highest capacitor voltages will be switched on when discharging.

2.2.3 The inner fundamental current controller

An unbalanced three-phase variable with no zero-sequence can be decomposed into the positive and negtive-sequence components, the convetre output voltage is:

$$v_{abc}(t) = v_{abc}^{+}(t) + v_{abc}^{-}(t) \tag{2.32}$$

Then, the positive and negtive-sequence abc- to dq-frame transformations are defined as

$$v_{dq}^{+}(t) = T(\theta)v_{abc}^{+}(t) \tag{2.33}$$

$$v_{dq}^{-}(t) = T(-\theta)v_{abc}^{-}(t) \tag{2.34}$$

where

$$T(\theta) = \frac{2}{3}\times\begin{bmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta-\frac{4\pi}{3}) \\ -\sin(\theta) & \sin(\theta-\frac{2\pi}{3}) & -\sin(\theta-\frac{4\pi}{3}) \end{bmatrix} \tag{2.35}$$

and θ is the angle of V_{abc} ,which is provided by a phase-locked loop (PLL). The postive- and negtive-sequence components of the current in dq-frame can be calculated in the same way.

The positive and negative sequence current control of 2-level converters [101][102][103] can be directly applied to MMC. The control scheme is separated into an inner current loop and an outer loop. A brief description will be given in the following sections.

Equition (2.31) is rearranged as:

$$\begin{aligned} \frac{di_d}{dt} &= -\frac{R_e}{L_e}i_d + \frac{v_{cd}^* - v_d + \omega L_e i_q}{L_e} \\ \frac{di_q}{dt} &= -\frac{R_e}{L_e}i_q + \frac{v_{cq}^* - v_d - \omega L_e i_d}{L_e} \end{aligned} \tag{2.36}$$

To facilitate estimations of v_{cd}^* and v_{cq}^* using proportional-integral (PI) controllers, the terms $v_{cd}^* - v_d + \omega L_e i_q$ and $v_{cq}^* - v_d - \omega L_e i_d$ are replaced by u_d and u_q , which represent the outputs of the PI controllers in the d and q axes. Since u_d and u_q represent the outputs of the current controllers that regulate i_d and i_q , they can be expressed as:

$$\begin{aligned} u_d(t) &= K_P^i(i_d^* - i_d) + K_I^i\int(i_d^* - i_d)dt \\ u_q(t) &= K_P^i(i_q^* - i_q) + K_I^i\int(i_q^* - i_q)dt \end{aligned} \tag{2.37}$$

Thus, v_{cd}^* and v_{cq}^* can be calculated from the PI outputs (u_d and u_q) as:

$$\begin{aligned} v_{cd}^* &= u_d + v_d - \omega L_e i_q \\ v_{cq}^* &= u_q + v_d + \omega L_e i_d \end{aligned} \tag{2.38}$$

On the basis of (2.37) and (2.38), the block diagram in Fig. 2.3 is drawn. The v_{cd}^*, v_{cq}^* and $\omega L_e i_q$ in (2.38) represent the feedforward terms of the current controller.

After merging (2.36), (2.37) and (2.38), and with further algebraic manipulations, where the integral parts of u_d and u_q are replaced by λ_d and λ_q, the following state-space equation is obtained:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ \lambda_d \\ i_q \\ \lambda_q \end{bmatrix} = \begin{bmatrix} -\frac{R_e + K_P^i}{L_e} & \frac{1}{L_e} & 0 & 0 \\ -K_I^i & 0 & 0 & 0 \\ 0 & 0 & -\frac{R_e + K_P^i}{L_e} & \frac{1}{L_e} \\ 0 & 0 & -K_I^i & 0 \end{bmatrix} \begin{bmatrix} i_d \\ \lambda_d \\ i_q \\ \lambda_q \end{bmatrix} + \begin{bmatrix} \frac{K_P^i}{L_e} & 0 \\ K_I^i & 0 \\ 0 & \frac{K_P^i}{L_e} \\ 0 & K_I^i \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{2.39}$$

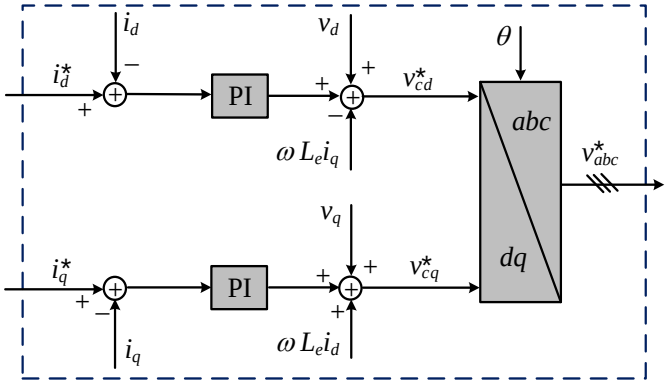


Fig. 2.3 A generic block diagram of an Inner Current Controller

$$\frac{i_d(s)}{i_d^*(s)} = \frac{i_q(s)}{i_q^*(s)} = \frac{K_P^i / L_e \, s + K_I^i / L_e}{s^2 + (K_P^i + R_e)/L_e \, s + K_I^i / L_e} \tag{2.40}$$

After comparing the denominator of (2.40) with that of the standard transfer function of a 2nd order system, the proportional and integral constants or gains of the current controllers are expressed as: $K_P^i = 2\omega_n \zeta L_e - R_e$ and $K_I^i = \omega_n^2 L_e$, where, the natural frequency ω_n and damping factor ζ can be selected, considering a number of control objectives such as settling time or peak overshoot.

2.2.4 **Positive and negative sequence inner current controllers**

Since the current controller depicted in Fig. 2.3 considers only positive sequence voltages and currents, it is only suitable for balanced operation, where negative and zero sequence components are zeros (as the practical considerations that dictate the grounding arrangement at converter side do not provide zero sequence current path). However, in order to facilitate precisely controlled operation during asymmetric AC network faults, the three-phase unbalanced voltages and currents must be decomposed into balanced sets of positive and negative sequence components and then transformed into two orthogonal planes '*dq*+' and '*dq*-' that rotate at speeds of ω and $-\omega$ respectively. In this manner, the positive and negative sequence voltages and currents could be controlled independently.

In order to distinguish between the positive and negative sequence variables, the suffix (superscripts '+' and '-') are added to the variables of the positive and negative sequence current controllers. Without repeating the above derivations, the state-space equations that describe the positive and negative sequence current controllers are:

$$\frac{d}{dt}\begin{bmatrix} i_d^{\pm} \\ \lambda_d^{\pm} \\ i_q^{\pm} \\ \lambda_q^{\pm} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_e + K_P^i}{L_e} & \dfrac{1}{L_e} & 0 & 0 \\ -K_I^i & 0 & 0 & 0 \\ 0 & 0 & -\dfrac{R_e + K_P^i}{L_e} & \dfrac{1}{L_e} \\ 0 & 0 & -K_I^i & 0 \end{bmatrix} \begin{bmatrix} i_d^{\pm} \\ \lambda_d^{\pm} \\ i_q^{\pm} \\ \lambda_q^{\pm} \end{bmatrix} + \begin{bmatrix} \dfrac{K_P^i}{L_e} & 0 \\ K_I^i & 0 \\ 0 & \dfrac{K_P^i}{L_e} \\ 0 & K_I^i \end{bmatrix} \begin{bmatrix} i_d^{\pm *} \\ i_q^{\pm *} \end{bmatrix} \tag{2.41}$$

Based on the generic current controller shown in Fig. 2.3, the block diagrams in Fig. 2.4 and Fig. 2.5 show the positive and negative sequence current controllers, respectively. Although the setting of the negative sequence current can vary according to operation requirements, maintaining balanced three-phase AC currents is assumed to be the objective in this thesis, which is achieved by setting the negative-sequence current references to zero.

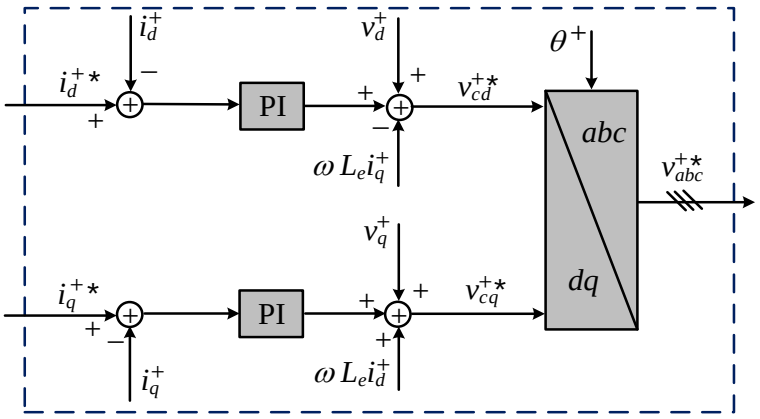


Fig. 2.4 A generic block diagram of a Positive Sequence Inner Current Controller

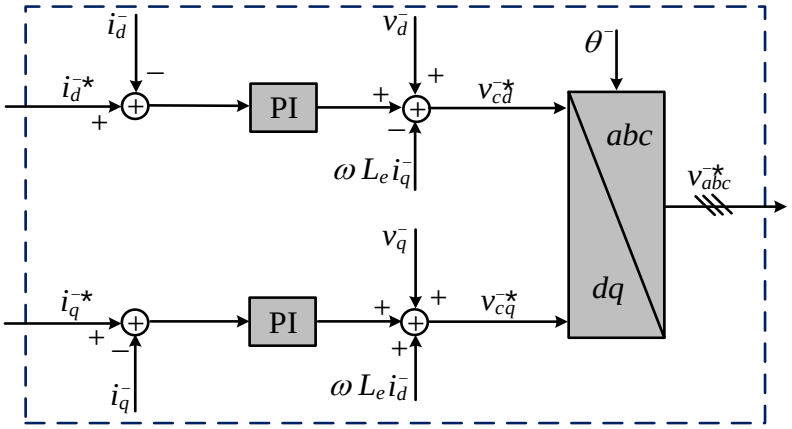


Fig. 2.5 A generic block diagram of a Negative Sequence Inner Current Controller

2.2.5 **Outer loop controllers**

MMC active and reactive power outputs can be expressed as:

$$\begin{aligned} P &= \tfrac{3}{2}(v_d^+ i_d^+ + v_q^+ i_q^+) \\ Q &= \tfrac{3}{2}(v_q^+ i_d^+ - v_d^+ i_q^+) \end{aligned} \tag{2.42}$$

In steady-state $v_q^* = 0$, (2.42) can be reduced to:

$$\begin{aligned} P &= \tfrac{3}{2} v_d^+ i_d^+ \\ Q &= -\tfrac{3}{2} v_d^+ i_q^+ \end{aligned} \tag{2.43}$$

Thus, the outer controller that exploits *d*-axis is normally used to define the active power to be imported or exported when the MMC operates as active power regulator (APR) or to set DC voltage level when the MMC operates as DC voltage regulator (DCVR). Thus, these controllers define the d-axis current references. In contrast, the outer controller that exploits the *q*-axis controls reactive power or AC voltage, and hence, it defines the *q*-axis current references. Since both components of the negative sequence current are suppressed to zero as stated above, both active and reactive powers are defined in their entireties by positive sequence currents.

Expressions in (2.43) indicating that the references for the direct and quadrature currents can be set directly as:

$$i_d^{+*} = \tfrac{2}{3}\frac{P^*}{v_d^+} \tag{2.44}$$

$$i_q^{+*} = \tfrac{2}{3}\frac{Q^*}{v_q^+} \tag{2.45}$$

where P^* and Q^* are the set-points for the reference active and reactive powers at PCC. Equivalently, the reference currents in (2.44) and (2.45) can be defined empirically, using PI controllers as:

$$\begin{aligned} i_d^{+*} &= K_P^p(P^* - P) + K_I^p\int(P^* - P)dt \\ i_q^{+*} &= K_P^q(Q^* - Q) + K_I^q\int(Q^* - Q)dt \end{aligned} \tag{2.46}$$

Similarly, when the MMC operates as DCVR, the reference of the positive sequence direct axis current can be expressed as:

$$i_d^{+*} = K_P^{dc}\left(V_{dc}^* - V_{dc}\right) + K_I^{dc}\int\left(V_{dc}^* - V_{dc}\right)dt \tag{2.47}$$

where V_{dc}^* is the reference DC link voltage. Fig. 2.6shows the generic block diagram of the outer P/Q/V_{dc} controllers.

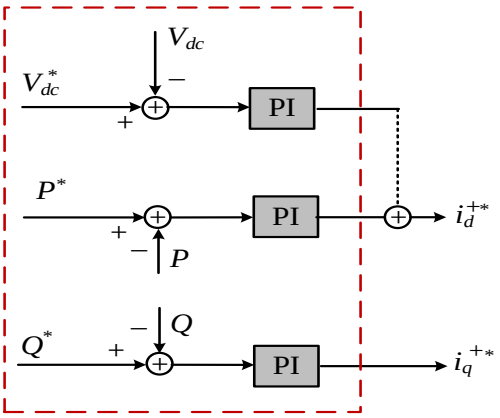


Fig. 2.6 Generic block diagram of an outer controller

2.2.6 **Circulating current suppression controller (CCSC)**

The circulating currents flow through phases increase the RMS value of arm currents and converter losses [105]. It has been proved that the circulating currents in the MMC are generated by the inner voltage differences among each phase unit [105], and their frequency being twice the fundamental frequency [106]. Increasing the arm inductance can reduce the circulating currents [106], though, a larger voltage drop is also introduced and with increased inductor cost. In [107], a circulating current suppressing controller (CCSC) to minimize the inner circulating current in an MMC is proposed.

After adding equations (2.26) and (2.27), the following equation is obtained:

$$\tfrac{1}{2}V_{dc} - \tfrac{1}{2}(v_{ua} + v_{la}) = R_{arm}\,\tfrac{1}{2}(i_{ua} + i_{la}) + L_{arm}\frac{d}{dt}\tfrac{1}{2}(i_{ua} + i_{la}) \tag{2.48}$$

Recall the definition of the common-mode current, $i_{coma} = \frac{1}{2}(i_{ua} + i_{la})$ and the common-mode component of the phase voltage, $v_{ua} + v_{la} = \alpha_d^a V_{carma}$ described earlier, (2.48) can be simplified as:

$$\tfrac{1}{2}\left(V_{dc} - \alpha_d^a V_{carma}\right) = R_{arm} i_{coma} + L_{arm}\frac{di_{coma}}{dt} \tag{2.49}$$

It is worth emphasizing that the common-mode capacitor sum, $v_{armUa} + v_{armLa} = \alpha_d^a V_{carma} + \Delta v_{carma}$ being used to describe the synthesis of the arm voltages consists of DC component 'V_{carma}' that determines the DC component of the common-

mode current and AC component ' Δv_{carma} ' which is seen as voltage ripple that drives the circulating current in phase leg. Taking these assertions into account, (2.49) can be rewritten as:

$$\tfrac{1}{2}\left[V_{dc}-\left(\alpha_d^a V_{carma}+\Delta v_{carma}\right)\right]=R_{arm}i_{coma}+L_{arm}\frac{di_{coma}}{dt} \tag{2.50}$$

Using the following definition of the common-mode currents of phase '*a*', $i_{coma}=I_d^a+i_h^a$, (2.50) can be separated into two parts, AC and DC components:

$$\tfrac{1}{2}\left[V_{dc}-\alpha_d^a V_{carma}\right]=R_{arm}I_d^a+L_{arm}\frac{dI_d^a}{dt} \tag{2.51}$$

$$-\tfrac{1}{2}\Delta v_{carma}=R_{arm}i_h^a+L_{arm}\frac{di_h^a}{dt} \tag{2.52}$$

Where, I_d^a represents the DC component of the upper and lower arm currents, and i_h^a is the inherent harmonic current in the upper and lower arm currents.

Equation (2.52) can be used in the design of the AC circulating current controller. After renaming or replacing the term $-\tfrac{1}{2}\Delta v_{carma}$ by Δv_{cir}^a, a proportional-resonant (PR) circulating current controller can be defined as in terms of three-phase quantities as:

$$\begin{aligned}
\Delta v_{cir}^a &= K_P^{cir}(i_h^{a*}-i_h^a)+\int\left[K_I^{cir}(i_h^{a*}-i_h^a)-x_a\right]dt\\
x_a &= \omega_n^2\int y_a dt\\
\Delta v_{cir}^b &= K_P^{cir}(i_h^{b*}-i_h^b)+\int\left[K_I^{cir}(i_h^{b*}-i_h^b)-x_b\right]dt\\
x_b &= \omega_n^2\int y_b dt\\
\Delta v_{cir}^c &= K_P^{cir}(i_h^{c*}-i_h^c)+\int\left[K_I^{cir}(i_h^{c*}-i_h^c)-x_c\right]dt\\
x_c &= \omega_n^2\int y_c dt
\end{aligned} \tag{2.53}$$

The time-domain implementation of an ideal PR controller is depicted in Fig. 2.7. Since the objective is to suppress the circulating currents which are dominantly 2nd order harmonic, the references for the circulating currents must be set to zero and ω_n must be

set to twice of the fundamental frequency. Fig. 2.8 shows the complete implementation of the circulating current control in s-domain.

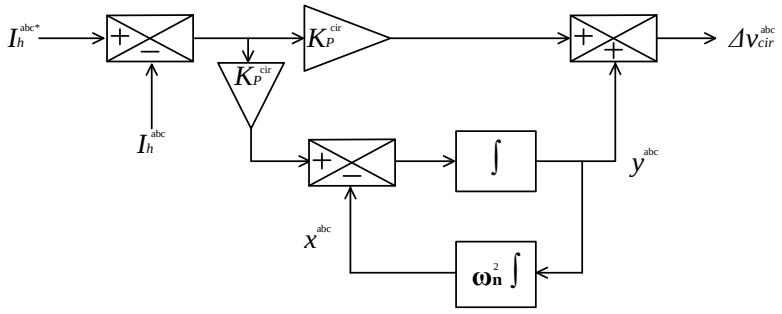


Fig. 2.7 Graphical depiction of PR controller [108]

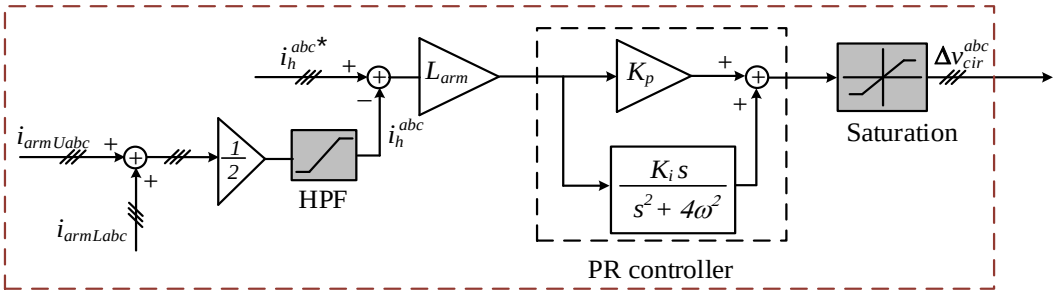


Fig. 2.8 Complete implementation of the circulating current control in s-domain

2.2.7 **Horizontal capacitor voltage balancing (phase energy balancing)**

A number of control methods have been proposed to achieve energy balance among each arm [109]-[111]. In this thesis, energy balancing control consists of two controllers including horizontal capacitor voltage balancing control which aims to keep the energies between the 3 phases balanced, and vertical capacitor voltage balancing control for keep energy balanced between the upper and lower arms in each phase.

Starting from the differential equations that describe the dynamics of the equivalent arms described earlier, that is:

$$C_e \frac{d}{dt} v_{ua} = \tfrac{1}{2}\left[a_d^a - m_a \right] i_{ua} \tag{2.54}$$

$$C_e \frac{d}{dt} v_{la} = \tfrac{1}{2}\left[a_d^a + m_a \right] i_{la} \tag{2.55}$$

Adding (2.54) and (2.55), yields:

$$C_e \frac{d}{dt} \tfrac{1}{2}\left[v_{ua} + v_{la}\right] = \tfrac{1}{4} a_d^a \left[i_{ua} + i_{la}\right] - \tfrac{1}{4} m_a \left[i_{ua} - i_{la}\right] \tag{2.56}$$

After recalling $v_{carm} = \tfrac{1}{2}\left[v_{ua} + v_{la}\right]$, $\tfrac{1}{2}\left[i_{ua} + i_{la}\right] = I_d^a + i_h^a$ and $I_d^a = \tfrac{1}{4} m I_m \cos\varphi$, (2.56) can be expressed as:

$$C_e \frac{d}{dt} \tfrac{1}{2}\left[v_{ua} + v_{la}\right] = \tfrac{1}{2} I_d^a (a_d^a - 1) + \tfrac{1}{8} m I_{\mathbf{m}} \sin(2\omega t + 2\delta + \varphi) \tag{2.57}$$

Since the purpose of the common-mode capacitor voltage sum controller is to regulate the DC component of the common-mode current, only DC parts of (2.57) are considered. Thus, (2.57) can be reduced to:

$$C_e \frac{d}{dt} \tfrac{1}{2}\left[v_{ua} + v_{la}\right] = \tfrac{1}{2} I_d^a (a_d^a - 1) \tag{2.58}$$

Setting the term $\tfrac{1}{2} I_d^a (a_d^a - 1)$ to be the output of the PI controller u_H^a that regulates the common-mode capacitor voltage sums, yields:

$$C_e \frac{d}{dt} \tfrac{1}{2}\left[v_{ua} + v_{la}\right] = u_H^a \tag{2.59}$$

where $u_H^a = \tfrac{1}{2} I_d^a (a_d^a - 1)$.

Thus, u_H^a can be expressed as in terms of three-phase quantities as:

$$\begin{aligned}
u_H^a &= K_P^H \left[V_{carm}^* - \tfrac{1}{2}\left(v_{ua} + v_{la}\right)\right] + K_I^H \left[V_{carm}^* - \tfrac{1}{2}\left(v_{ua} + v_{la}\right)\right] dt \\
u_H^b &= K_P^H \left[V_{carm}^* - \tfrac{1}{2}\left(v_{ub} + v_{lb}\right)\right] + K_I^H \left[V_{carm}^* - \tfrac{1}{2}\left(v_{ub} + v_{lb}\right)\right] dt \\
u_H^c &= K_P^H \left[V_{carm}^* - \tfrac{1}{2}\left(v_{uc} + v_{lc}\right)\right] + K_I^H \left[V_{carm}^* - \tfrac{1}{2}\left(v_{uc} + v_{lc}\right)\right] dt
\end{aligned} \tag{2.60}$$

where, V_{carm}^* is the reference for the common-mode capacitor voltage sums of the three-phase legs, and for practical reasons, $V_{carm}^* \geq V_{dc}$.

If the limited influence of the common-mode current controller is neglected, u_H^a can be used directly to modify the modulation waveforms being produced by the fundamental positive and negative sequence current controllers.

Fig. 2.9 shows the block diagram of the Horizontal Capacitor Voltage Balancing control. As shown, a low pass filter (LPF) is added to extract the average capacitor volatges by the frequency components higher than the cut-off frequency, thereby reducing interference caused by arm voltage ripple.

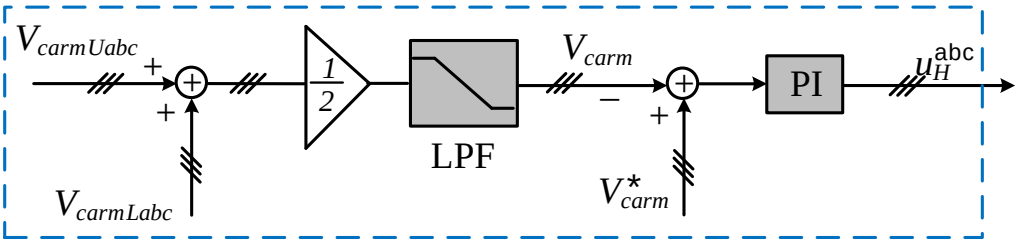


Fig. 2.9 Horizontal capacitor voltage balancing

2.2.8 **Vertical capacitor voltage balancing (arm energy balancing)**

Subtracting (2.54) and (2.55), yields:

$$C_e \frac{d}{dt}\left[V_{ua} - V_{la}\right] = \tfrac{1}{2} a_d^a \left[i_{ua} - i_{la}\right] - \tfrac{1}{2} m_a \left[i_{ua} + i_{la}\right] \tag{2.61}$$

After recalling, $i_a = i_{armUa} - i_{armLa}$ and $\frac{1}{2}\left[i_{armUa} + i_{armLa}\right] = I_d^a + i_h^a$, equation (2.61) can be rewritten as:

$$C_e \frac{d}{dt}\left[V_{carmUa} - V_{carmLa}\right] = \tfrac{1}{2} a_d^a i_{ao} - \tfrac{1}{2} m_a \left[I_d + i_h\right] \tag{2.62}$$

When the circulating currents of the three-phase legs are well suppressed, i.e. $i_h = 0$, the right side of (2.62) becomes pure sinusoidal with the fundamental frequency. However, since the purpose of vertical capacitor voltage balancing is to force the DC component of the sum of the upper capacitor voltages to be equal to that of the lower capacitor voltages (i.e., $V_{carmUa} = V_{carmLa}$ or $\Delta V_{carma} = V_{carmUa} - V_{carmLa} = 0$), only DC component of (2.62) needs to be considered in the control design.

Therefore, (2.62) can be rewritten assuming that any mismatch between DC components of the upper and lower arms' capacitor voltages of the same phase leg determines the magnitude of the additional modulation u_V^a to be added to the principle modulating signals, as:

$$C_e \frac{d}{dt} \Delta V_{carma} = u_V^a \tag{2.63}$$

If PI regulators are used, u_V^a can be expressed in terms of three-phase quantities as:

$$\begin{aligned} u_V^a &= K_P^V (\Delta V_{carm}^* - \Delta V_{carma}) + K_I^V (\Delta V_{carm}^* - \Delta V_{carma}) dt \\ u_V^b &= K_P^V (\Delta V_{carm}^* - \Delta V_{carmb}) + K_I^V (\Delta V_{carm}^* - \Delta V_{carmb}) dt \\ u_V^c &= K_P^V (\Delta V_{carm}^* - \Delta V_{carmc}) + K_I^V (\Delta V_{carm}^* - \Delta V_{carmc}) dt \end{aligned} \tag{2.64}$$

where, $\Delta V_{carm}^* = 0$ represent the reference of the differential capacitor voltages, and the outputs of this controller depicted in (2.64) are synchronized with modulating signals and then added to the principle modulating signals in a manner that they only affect the common quantities, see Fig. 2.10. The vertical capacitor voltage balancing ensures the nullification of the voltage difference between arms.

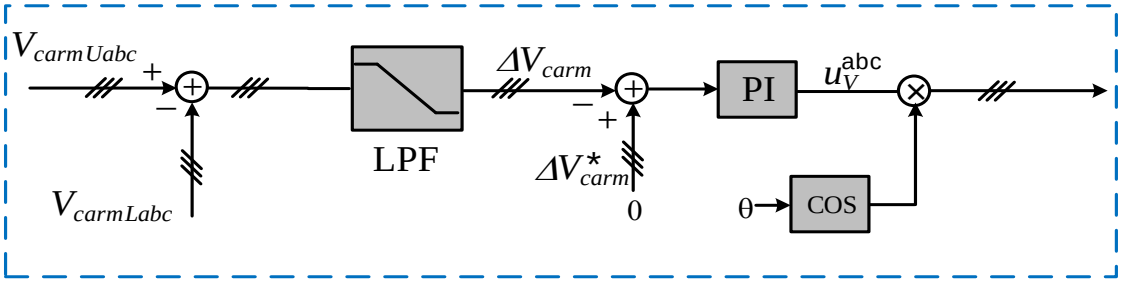
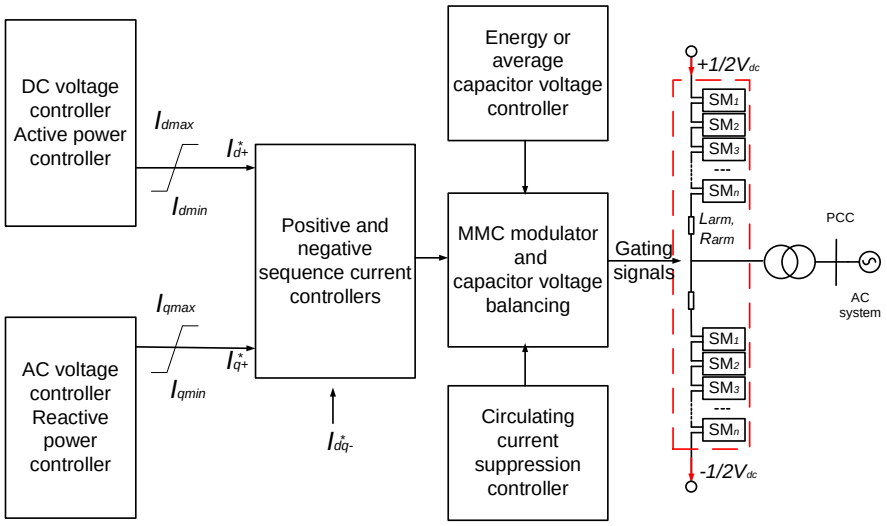


Fig. 2.10 Vertical capacitor voltage balancing

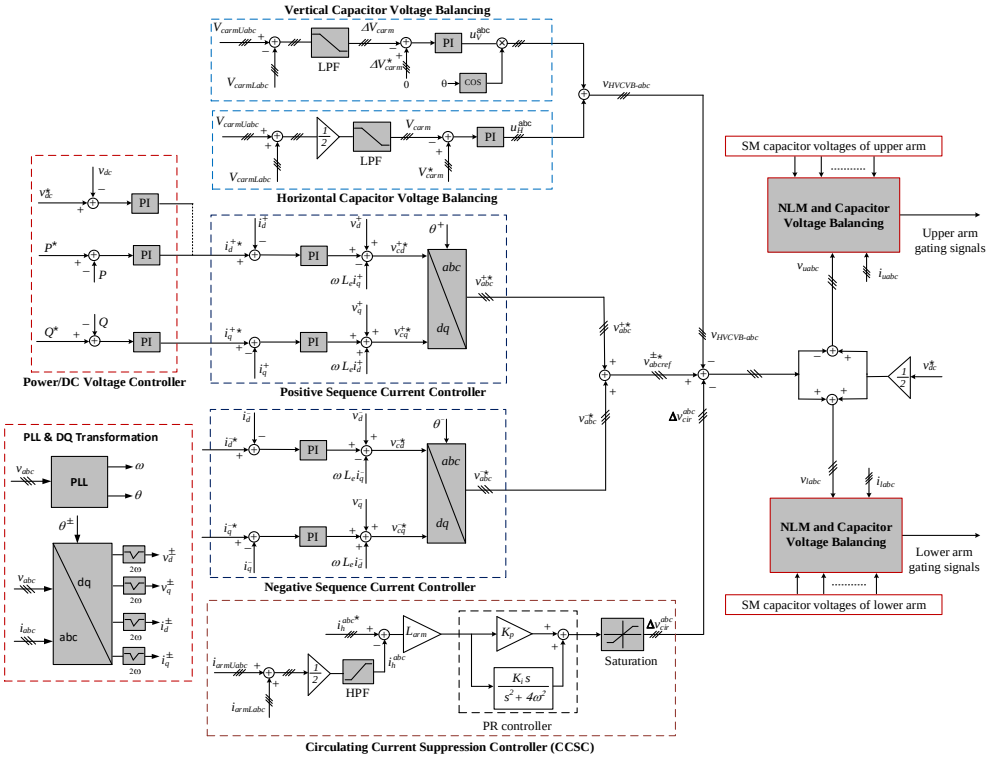
2.2.9 **Overall control system**

In summary, Fig. 2.11(a) depicts a generic control block diagram of the MMC. Since the *d*-axis is aligned with the voltage vector at PCC, this means the direct and quadrature currents represent active and reactive power components, respectively. Therefore, the outer controllers that set the active power and DC voltage orders are implemented on *d*-axis. Similarly, the outer controllers that regulate reactive power or AC voltage are implemented on q-axis. Therefore, active power/DC voltage and reactive power/AC voltage set the positive sequence direct and quadrature current orders, respectively. The negative sequence direct and quadrature current orders are set to zeros. The inner current controller regulates both positive and negative sequence currents during normal operation and limits MMC current contribution to AC faults and generates the principle AC modulating signals.

Active circulating current suppression controller is used to suppress the 2nd order harmonic currents in the MMC arm currents in order to reduce semiconductor power losses and SM capacitor voltage ripples. The horizontal capacitor voltage balancing controller facilitates regulation of half-bridge SM capacitor voltages independent of the MMC DC link voltage. This controller also modifies the principle modulation signals, particularly, their DC components. The most inner controller is the implementation of the non-distributed SM capacitor voltage balancing and modulator that ensures the voltage across each arm to be equally shared between the SM capacitors of the arm and generate the desired arm and output voltage, by selecting an appropriate number of SM capacitors to be inserted into power path and bypassed in each instant in time. A detailed block diagram that highlights individual controllers of the MMC employed are summarized in Fig. 2.11(b).



(a)



(b)

Fig. 2.11 Control block diagram of the MMC

2.3 **Summary**

In this chapter, the principles of MMC systems, including the basic structure and mathematical model of MMC is presented. The control systems used in this thesis, including SM capacitor voltage balancing controller, inner and outer current loop controllers, circulating current suppression controller and phase & arm energy balancing controllers, are discussed in detail, which will be applied in the test systems in Chapter 3, Chapter 4 and Chapter 5.

Chapter 3 MMC efficient modelling for electromagnetic transients (EMT) digital simulation

This chapter discusses the main modelling methods for simulation of the MMC, namely, detailed switching, switching function, Thevenin equivalent and averaged models. The aforementioned HB-MMC models are developed and validated by comparing the results of PSCAD offline simulation models (switching function, averaged and Thevenin equivalent MMC models) first, considering a normal steady-state operation, AC and DC short circuit fault. Then, simulation efficiencies of different HB-MMC models are compared. As a follow up of the extensive offline validations of a number of MMC models, the detailed validations of user-defined real-time HB-MMC switching function and averaged MMC models developed in RSCAD against the offline PSCAD MMC switching function models are presented. For one-to-one validation, the switching function MMC models in both platforms (PSCAD and RSCAD) have 20 cells per arm, with identical controllers and parameters. These offline and real-time simulation results show that the developed MMC models are able to replicate the typical behaviour of the MMC under normal operation and AC and DC network faults.

3.1 MMC efficient modelling methods

3.1.1 Detailed switching model

The detail switching model of the MMC can be developed based on the circuit shown in Fig. 1.4 where each half-bridge SM is described in detail, with each switching device mimics the conduction pattern and switching characteristics of physical insulated gate bipolar transistor (IGBT) and its freewheeling diode. When the arm currents defined in Fig. 1.4 are assumed to be positive, i.e. positive currents flowing into the SMs, the circuit operation can be explained as follows:

- When T_2 is on and T_1 is off, positive arm current flows through the IGBT part of the switch T_2, while negative arm current flows through its diode part. The SM capacitor is bypassed and the out voltage is zero.
- When T_2 is off and T_1 is on, positive arm current flows through the diode part of the switch T_1, while negative arm current flows through its IGBT part. The SM capacitor is inserted and the out voltage is v_c.

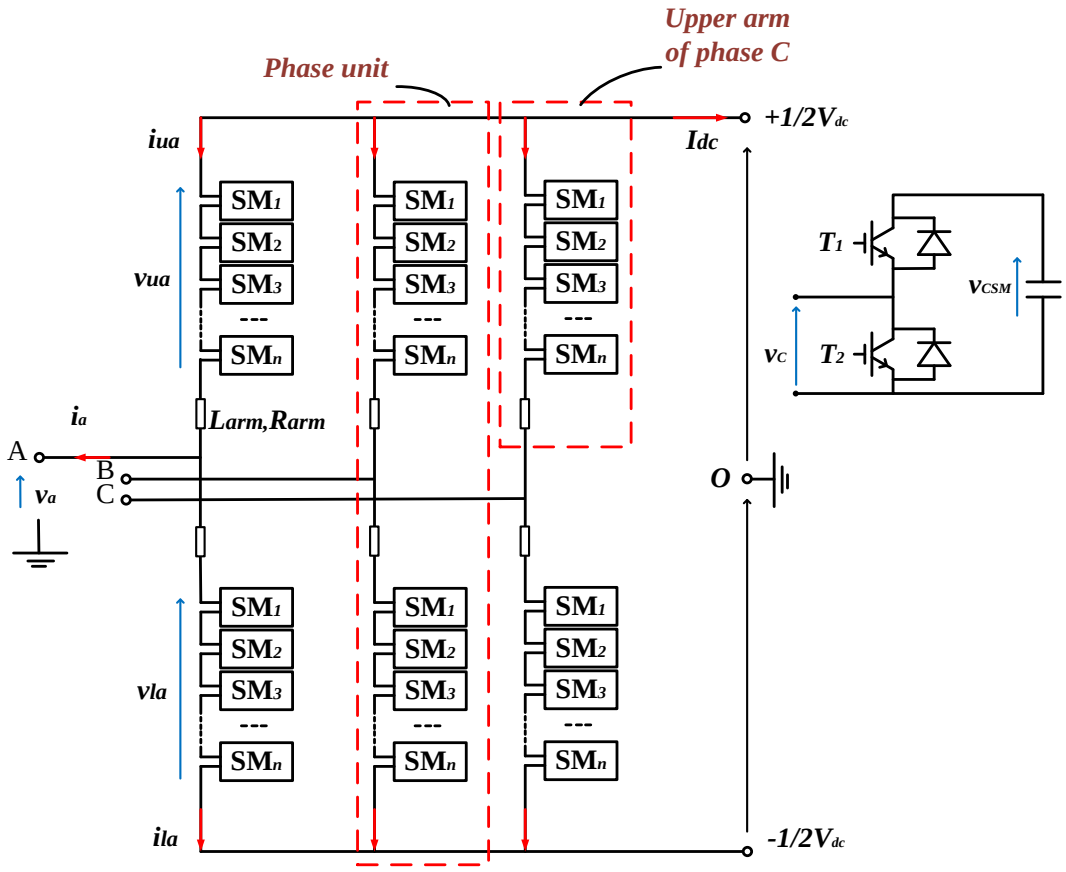


Fig. 3.1 A typical power circuit for the three-phase MMC

The detail switching representation may also account for the turn-on and turn-off transients of the switching devices and their on-state resistances and voltage drops. Such detailed representation necessitates the use of stiff solvers with small time steps in order to handle a wide range of time constants which are associated with a large number of dynamics that exist in an MMC. In addition, such detailed switching models contain large numbers of electrical nodes leading to large admittance matrices of which the inversion is computationally expensive. Thus, detail switching models take significantly long

execution time on offline simulation tools such as PSCAD or Matlab/Simulink, and place very high requirements on the processor performance of the real-time simulator, e.g. RTDS.

In summary, the above discussions highlight the need for the development of accurate and computational efficient MMC models.

3.1.2 **Averaged model**

The development of the MMC average model is promoted by the need to have computation efficient model suitable for a wide range of power system studies where the detailed internal converter behaviour and switching transients are not of interest. To achieve this objective, the following assumptions are made:

The switching voltages being developed across the upper and lower arms of each phase are replaced by their average voltages, which can be expressed as:

$$v_{armUa} = \sum_{j=1}^{N_{SM}} V_{CSMUa} s_{xj} \approx \tfrac{1}{2} V_{carmUa} \left[1 - m\sin(\omega t + \delta)\right] \approx V_{carmUa} m_{aU} \tag{3.1}$$

$$v_{armLa} = \sum_{j=1}^{N_{SM}} V_{CSMLa} s_{xj} \approx \tfrac{1}{2} V_{carmLa} \left[1 + m\sin(\omega t + \delta)\right] \approx V_{carmLa} m_{aL} \tag{3.2}$$

The inter-SM dynamics in each arm is neglected. Thus, SM capacitor voltages of each arm oscillate together (considering the SM voltages in each of the arm are balanced), with the upper and lower arms present capacitances $C_{armU} = C_{SM} / N_U$ and $C_{armL} = C_{SM} / N_L$, where the numbers of SM capacitors being inserted into power path from the upper and lower arms (N_u and N_L) can be approximated by:

$$N_U \approx \tfrac{1}{2} N_{SM} \left[1 - m\sin(\omega t + \delta)\right] \approx N_{SM} m_{aU} \tag{3.3}$$

$$N_L \approx \tfrac{1}{2} N_{SM} \left[1 + m\sin(\omega t + \delta)\right] \approx N_{SM} m_{aL} \tag{3.4}$$

Considering the definitions in (3.3) and (3.4) , the dynamics of the upper and lower SM capacitors can be approximated as:

$$\frac{C_{SM}}{N_U}\times\frac{d}{dt}V_{carmUa}\approx i_{armUa}$$
$$\frac{C_{SM}}{N_{SM}}\times\frac{d}{dt}V_{carmUa}\approx \tfrac{1}{2}\left[1-m\sin(\omega t+\delta)\right]i_{armUa} \quad (3.5)$$
$$C_e\times\frac{d}{dt}V_{carmUa}\approx m_{aU}i_{armUa}$$

$$\frac{C_{SM}}{N_L}\times\frac{d}{dt}V_{carmLa}\approx i_{armLa}$$
$$\frac{C_{SM}}{N_{SM}}\times\frac{d}{dt}V_{carmLa}\approx \tfrac{1}{2}\left[1+m\sin(\omega t+\delta)\right]i_{armLa} \quad (3.6)$$
$$C_e\times\frac{d}{dt}V_{carmLa}\approx m_{aL}i_{armLa}$$

where $C_e = C_{SM} / N_{SM}$ represents the equivalent SM capacitance for each arm and N_{SM} is the number of SMs in each arm.

From (3.5) and (3.6) , the upper and lower arms equivalent capacitor currents are:

$$i_{capUa}\approx C_e\times\frac{d}{dt}V_{carmUa}\approx m_{aU}i_{armUa} \quad (3.7)$$

$$i_{capLa}\approx C_e\times\frac{d}{dt}V_{carmLa}\approx m_{aL}i_{armLa} \quad (3.8)$$

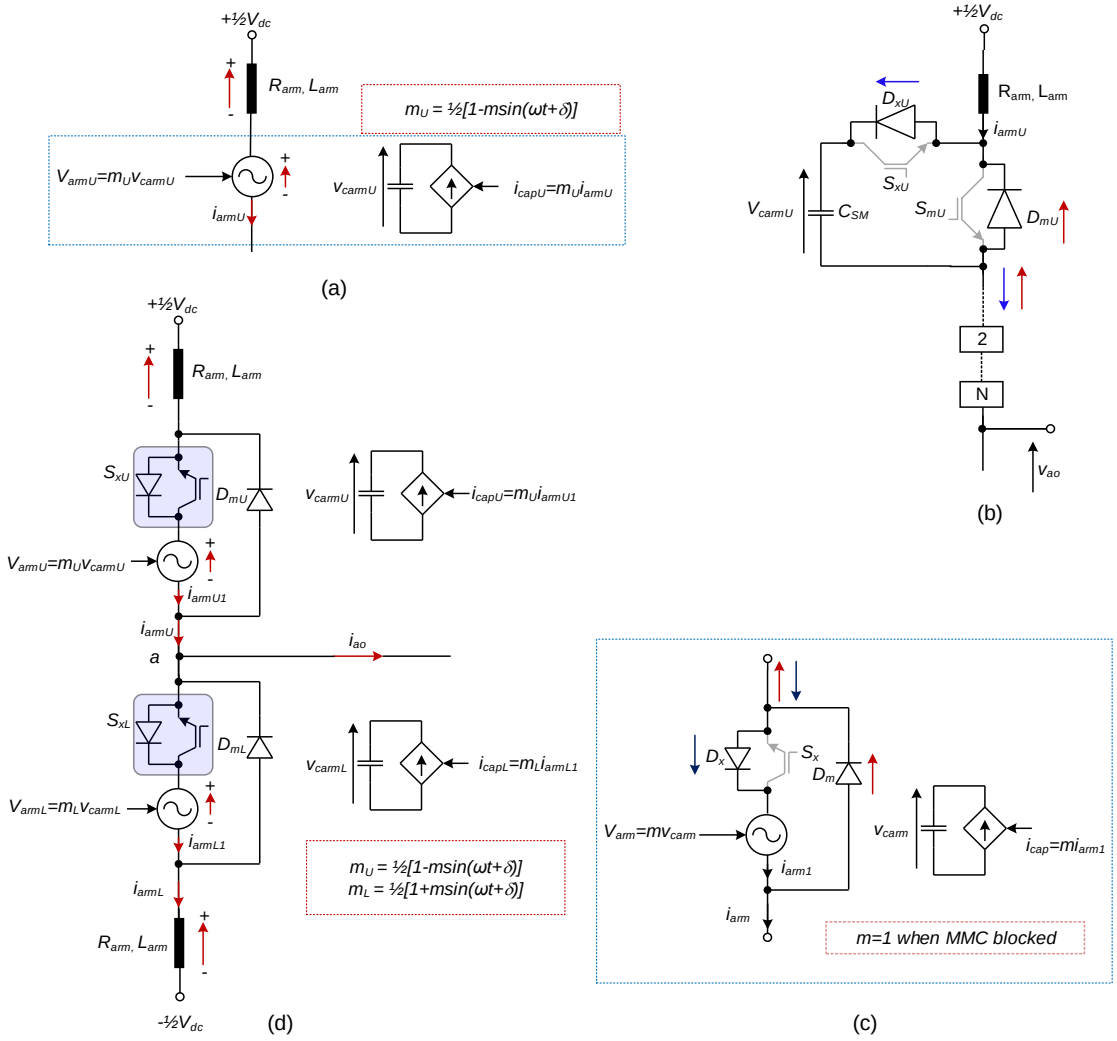


Fig. 3.2 Modular multilevel converter averaged model: (a) arm voltage calculation; (b) auxiliary circuit to present current path; (c) arm presentation; (d) phase presentation

Equations (3.1) to (3.8) can be used to calculate the average voltage and the total SM capacitor voltage of each arm when the MMC is in operation, as graphically shown in Fig. 3.2(a) for an upper arm. However, to accurately mimic the typical MMC behaviour when all its switches are blocked, i.e. all the IGBTs in the SMs are switched off (e.g. after receiving signal from protection system during a DC fault), additional considerations are required to ensure all the possible current paths are included in the model. Considering the current paths in the upper MMC arm with a detailed representation of the switching devices as shown in Fig. 3.2 (b), when the gating signals to the all the IGBTs are inhibited (or referred to as MMC blocked), the positive arm current (when i_{armU} is pointing

downward) flows through the diodes D_{xU} and the SM capacitor and thus, the arm voltage will be the combined DC voltages of the SM capacitors. Whilst the negative arm current (when i_{armU} is pointing upward) flows through the freewheeling diode D_{mU} of each SM and the SM capacitors are bypassed. Thus, the arm voltage is considered to be zero. Fig. 3.2 (c) shows the averaged model with additional IGBTs and diodes devices providing the necessary conduction path to facilitate the recreation of the MMC typical behaviour during blocked states. It is worth emphasizing that during normal operation, the switch S_x of the averaged MMC arm must remain permanently in on-state, and as the generated arm voltage V_{arm} is always positive, it forces the diode D_m to be reverse biased. Thus, the modified MMC average arm presents identical to those shown in Fig. 3.2 (a). Also, when converter blocking is activated, the switch S_x must be turned off and *m* is set to 1 to mimic the MMC behaviour stated above.

3.1.3 **Thevenin equivalent model**

This modelling method adopts the electromagnetic transient program (EMTP) simulation approach originally proposed by Dommel in [37][58][112] and has become the dominant modelling method in commercial power system software for modelling a wide range of electrical components. This method was first applied to MMC in [37], and other variants were later developed [46][48][113][114]. This modelling method treats the switch devices of the SMs as two-state switched resistances, with on-state and off-state resistances R_{ON} and R_{OFF} respectively, and each SM capacitance is replaced by its electromagnetic transient equivalent circuit. For a generic SM shown in Fig. 3.3 (a), the SM capacitor dynamic can be expressed as:

$$\frac{dV_{CSMi}(t)}{dt} = \frac{I_{ci}(t)}{C_{SM}} \tag{3.9}$$

The electromagnetic transient simulation pre-solves all differential equations using well-established numerical integration methods, with Backward Euler and Trapezoidal integration methods being widely used. For example, after solving (3.9) using trapezoidal integration method, the following equations are obtained:

$$V_{CSMi}(t) = V_{CSMi}(t-\Delta t) + \tfrac{1}{2}\frac{\Delta t}{C_{SM}}\left[I_{ci}(t) + I_{ci}(t-\Delta t)\right] \tag{3.10}$$

$$V_{CSMi}(t) = V_{CSMi}(t-\Delta t) + R_c I_{ci}(t-\Delta t) + R_c I_c(t) = V_h + R_c I_c(t) \tag{3.11}$$

where Δt is the simulation time step, $V_h = V_{CSMi}(t-\Delta t) + R_c I_{ci}(t-\Delta t)$ and $R_c = \frac{\Delta t}{2C_{SM}}$ represents the equivalent resistance of the SM capacitance equivalent circuit.

Fig. 3.3 (b) depicts the equivalent circuit of the half-bridge SM with Backward Euler and Trapezoidal integration methods. The circuit can be further simplified using Thevenin theory, where the Thevenin voltage and resistance per SM are:

$$V_{mi}(t) = \frac{R_{mi}}{R_{ci} + R_{xi} + R_{mi}} \times V_h \tag{3.12}$$

$$R_{thi} = \frac{R_{mi}(R_{ci} + R_{xi})}{R_{ci} + R_{xi} + R_{mi}} \tag{3.13}$$

The switched voltage to be developed across each arm can be calculated by:

$$V_{arm} = \sum_{i=1}^{N_{SM}} V_{mi} \tag{3.14}$$

Fig. 3.3(c) shows the block diagram of one MMC phase-leg, where the arm is modelled using the Thevenin equivalent circuit and modified to be able to mimic the typical MMC behaviour during blocking and de-blocking in a similar way as that of the averaged HB-MMC model described earlier in Section 3.1.2.

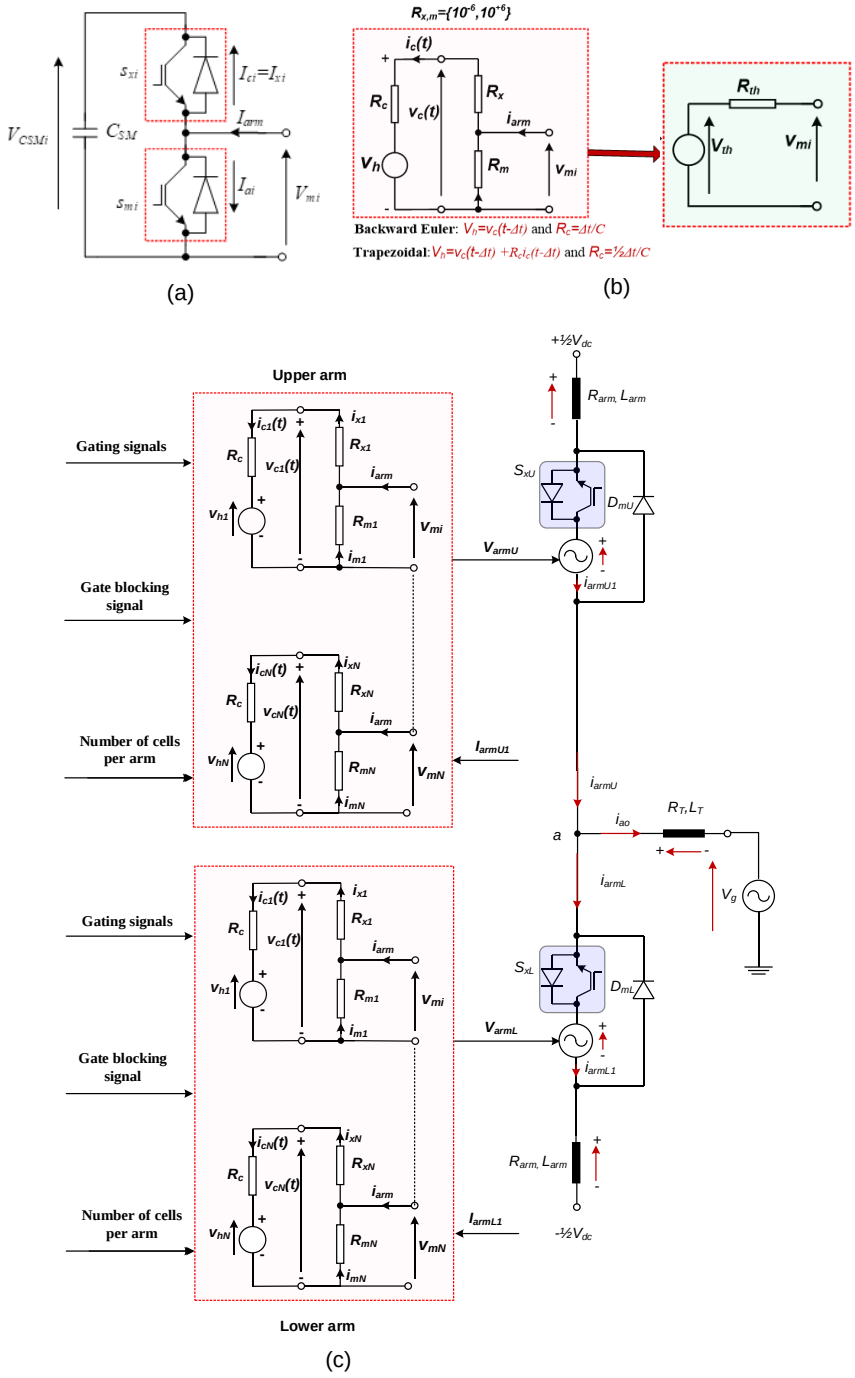


Fig. 3.3 Depiction of the MMC model based on the Thevenin equivalent circuit of the half-bridge sub-modules

3.1.4 **Switching function model**

This modelling method represents the MMC switching devices using ideal switches, where the on and off states are denoted by 1 and 0 respectively. Considering Fig. 3.4 (a)

and (b), the output voltage of a single half-bridge SM can be expressed in terms of its SM capacitor voltage and switching state of the auxiliary switch S_{xi} as:

$$v_{mi}(t) = s_{xi} V_{CSMi}(t) \tag{3.15}$$

Similarly, the SM capacitor current of each SM can be related to the MMC arm current by:

$$i_{ci}(t) = s_{xi} I_{arm}(t) \tag{3.16}$$

The SM capacitor voltage can be calculated at each time step as

$$V_{CSMi}(t) = \frac{1}{C_{SM}} \int i_{ci}(t) dt \tag{3.17}$$

Equation (3.17) is transformed into discrete from using Tustin (trapezoidal integration method) as shown in (3.10) and (3.11).

Thus, the total switching voltage across each arm can be calculated as:

$$V_{arm} = \sum_{i=1}^{N_{SM}} V_{mi} \tag{3.18}$$

The graphical representation of the MMC switching function model is shown in Fig. 3.4 (c). Similar to previously described models, further modifications are also necessary to represent the behaviour during MMC blocking state. The composite switches S_{xU} and S_{xL}, and diodes D_{mU} and D_{mL} as shown in Fig. 3.4 (c) are thus included and all the S_{xi} in the arms are set to 1 after the blocking of the converter.

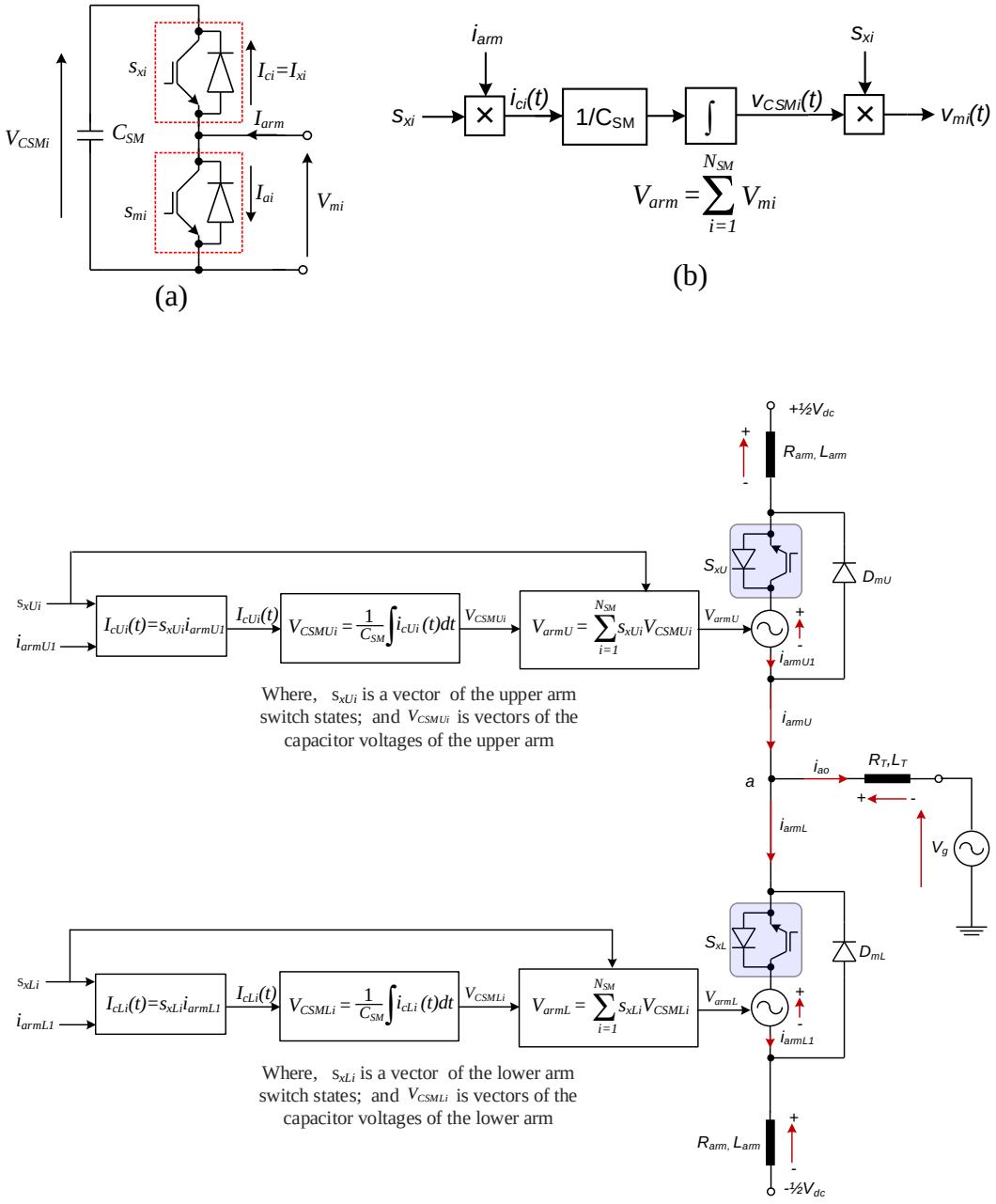


Fig. 3.4 Graphical depiction of the MMC switching function model

3.2 Development and validation of MMC offline and real-time models

3.2.1 Test system

This section uses the MMC based HVDC converter station shown in Fig. 3.5 for a wide range of studies in order to validate the accuracy of different models. The converter station in Fig. 3.5 is equipped with controllers shown in Fig. 2.11, and for ease of illustration, active power control mode is used throughout this chapter. Detailed system parameters and control parameters are depicted in Fig. 3.5 and listed in Table 1 and Table 2. The SM capacitances for the 20-SM and 350-SM MMC models and averaged MMC model to be considered are calculated assuming 30kJ/MVA [22][55]. The values of coefficient for the proportional K_P and coefficient for the integral K_I are adjusted by tuning. Parameters of all the PI controllers in this thesis are determined by tuning.

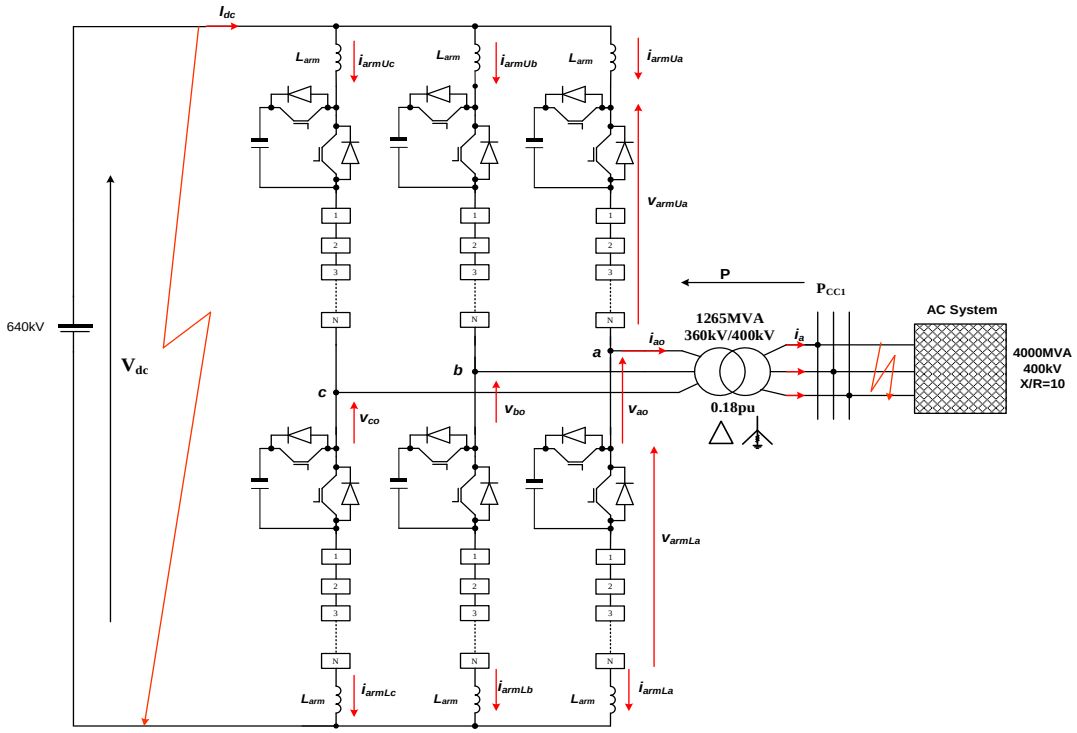


Fig. 3.5 Illustrative test system (power, current and voltage polarities in this figure are assumed to be positive)

Table 1: Test system parameters

Parameters		
MMC rated apparent power (Sn)		1265MVA
MMC rated active power (P)		1200MW
MMC rated reactive power(Q)		±400MVAr
MMC nominal DC Voltage (V_{dc})		640kV (±320kV)
MMC rated AC output voltage (line-to-line)		360kV
Arm inductance (L_{arm})		0.13pu
SM capacitance (C_{SM})	20-SM MMC	628μF
	350-SM MMCs	11mF
	Average model	31.4μF
Nominal Frequency		50Hz
Transformer rated apparent power		1265MVA
Interfacing transformer voltage ratio		400/360kV
Transformer leakage reactance		0.18pu
Transformer resistance		0.004452pu

Table 2 MMC system control parameters

MMC Controller	**Control Parameters**	
Outer Controller	**Proportional Gain (K_p)**	**Integral Time Constant (T_i)**
Active Power Controller	1×10^{-3}	8
Reactive Power Controller	10×10^{-3}	10
AC Voltage Controller	1×10^{-3}	5
DC Voltage Controller	15×10^{-3}	2.5
Inner Current Controller		
Positive Sequence Inner Controller	1.5×10^{3}	7.03×10^{-6}
Negative Sequence Inner Controller	2.26×10^{3}	7.03×10^{-6}
Auxiliary Controller		
Circulating Current Suppression Controller	1.5×10^{3}	1×10^{3}
Vertical Capacitor Voltage Balancing	3	6×10^{-3}
Horizontal Capacitor Voltage Balancing	3	6×10^{-3}

3.2.2 **Offline validation and efficiency comparison**

This section validates the performance of the averaged and switching function based MMC models against the Thevenin equivalent model of the PSCAD library. The performance of the MMC model with a reduced number of sub-modules per arm is also compared to that with a large number of sub-modules per arm, considering the test case of solid three-phase AC short circuit fault. The MMC models used in this validation are: 20-SM and 350-SM PSCAD library Thevenin Equivalent (PD), 350-SM switching function (SF) and averaged (Avg) models.

In [115], accuracy validation among MMC models are made by calculating the mean absolute error (MAE) of the waveforms. However, in this thesis, developed RTDS models are validated against offline PSCAD models, which introduces errors produced by different simulators. Another more widely used MMC models accuracy validation criterion is the overlap of waveforms [37][45][49][55][56][57][96][116]. By superimposing the waveforms generated by different models, the differences between the waveforms reflect the differences between the different models. The degree of coincidence of the waveforms reflects the similarity of the two models under that case. In this thesis, overlap method will be used for all the accuracy validation.

3.2.2.1 *Validation during normal steady-state operation*

The system operation conditions during this illustration are summarized as follows.

- The converter station regulates its reactive power output at zero throughout the simulation.
- Initially, the active power of the converter station is regulated at zero and is ramped up from 0 to 1200MW at t=1s.
- In this illustration, the sum of the SM capacitor voltages of each arm is regulated at 640kV.

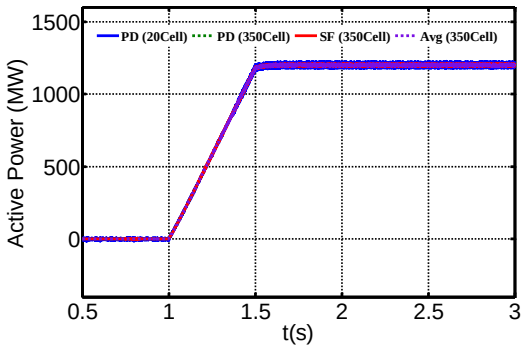
Simulation waveforms of the averaged, Thevenin equivalent (20 and 350 SM per arm), switching function (350 SM) HB-MMC models superimposed on each other are shown in Fig. 3.6. As shown, Fig. 3.6(a), (b) compare the active power of the HB-MMC models measured at PCC_1 (with the positive power flow is from AC to DC side), and DC link current (1.875kA corresponding to rated active power of 1200MW), respectively. The

waveforms in Fig. 3.6 (a) and (b) indicate that all the HB-MMC models produce identical results in terms of magnitudes and dynamics. Samples of the upper and lower arm currents and their zoomed versions displayed in Fig. 3.6 (c), (d), (e) and (f) indicate coexistence of the DC component 'I_d^a' and fundamental current '$\frac{1}{2}i_{ao}$'in the MMC arm currents as theoretically stated in (2.12) and (2.13), with circulating current component 'i_h^a' is well suppressed. From the simulation waveforms in Fig. 3.6 (c) and (d), and (e) and (f), it can be concluded that the simplifications introduced during the development of the HB-MMC averaged model, it is able to reproduce all the dynamics associated with both fundamental and DC components of the arm currents, and with the same accuracy of the Thevenin equivalent and switching function models. The plot for the common-mode current, $i_{com} = ½(i_{armUa} + i_{armLa})$ and its zoomed version in Fig. 3.6 (g) and (h) show that after proper suppression of the circulating current, the common-mode current of each phase becomes a pure DC component 'I_d^a' and equals to one-third of the DC link current 'I_{dc}', which is in line with the theoretical expression in (2.14). It is worth emphasizing that all the HB-MMC models being compared produce practically identical common-mode currents and in line with theoretical value as described earlier. Fig. 3.6 (i) and (j), and (m) and (n) confirm that the differential arm current and voltage of each phase leg represent output phase current and voltage as theoretically expressed by (2.6) and (2.9). The plots for the common-mode voltage '$(v_{armUa} + v_{armLa})$' and its zoomed version in Fig. 3.6 (k) and (l) show that after the suppression of the voltage components that drive the circulating current in each phase, the common-mode voltage '$(v_{armUa} + v_{armLa})$' becomes dominantly DC component and its value is slightly larger than the DC link voltage ($V_{dc} = 640kV$) in order to allow the power flow from AC to DC side as illustrated by (2.11). The plots in Fig. 3.6 (k) and (l) show the common-mode voltage of the 20-SM MMC exhibits higher high-frequency voltage ripples compared to 350-SM MMCs, and this is due to its larger mismatch between 'V_{dc}' and '$(v_{armUa} + v_{armLa})$' as a result of larger switching voltage (reduced number of SMs). Fig. 3.6 (o)-(q) and (r) show phase '*a*' upper and lower capacitor voltage sums. The plots in Fig. 3.6 (s) and (t), and (u) and (v) indicate that the common-mode capacitor voltage sums of the MMC are dominantly DC component plus

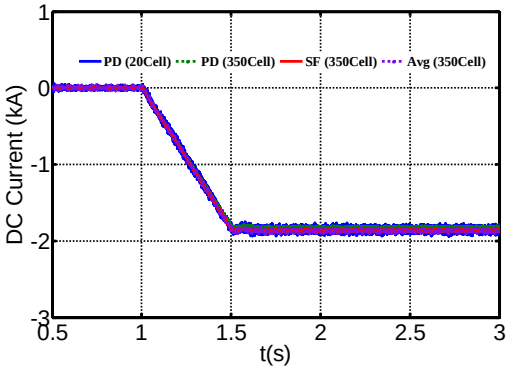
2nd order harmonic voltage, while the differential-mode capacitor voltage sums are mainly fundamental voltage.

These indicate that all the HB-MMC models being compared are able to reproduce the inter-dynamics between the MMC arms and between the SMs of the same arm with identical accuracies and in line with theoretical discussions presented in Section 3.1. From the theoretical analysis presented in Section 3.1 and the above discussions and simulation waveforms presented in Fig. 3.6, it can be concluded that the 20-SM Thevenin equivalent, 350-SM Thevenin equivalent, 350-SM switching function, and averaged MMC models being studied exhibit the typical behaviour of the MMC and adhere to well established theoretical equations that govern the operation of the MMC.

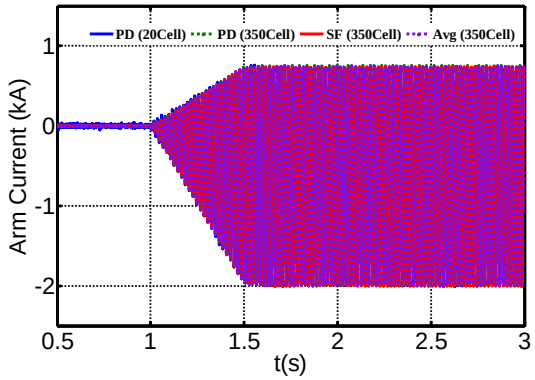
Since the comparisons include SM-level MMC models and converter-level model, SM internal behaviour and SM-level comparisons are not considered.



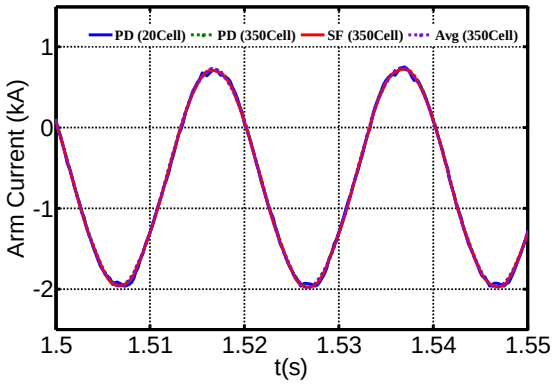
(a) Active Power 'P'



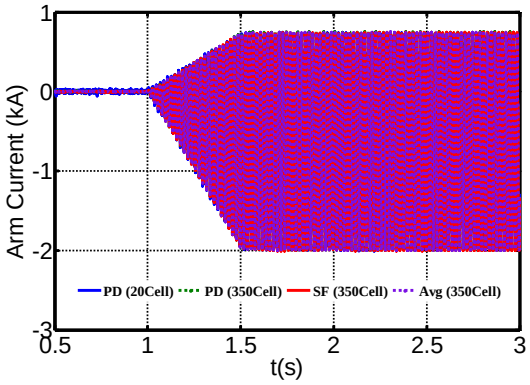
(b) DC Current 'I_{dc}'



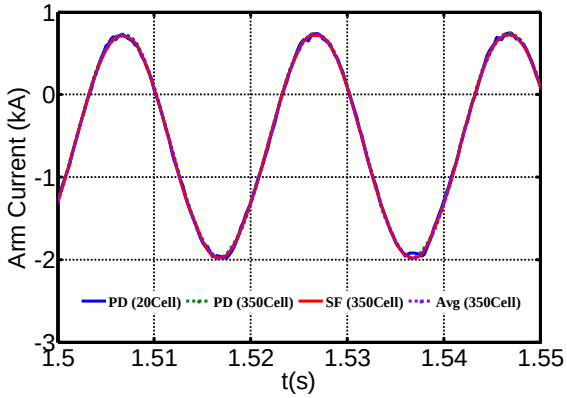
(c) Phase 'a' upper arm current, i_{armUa}



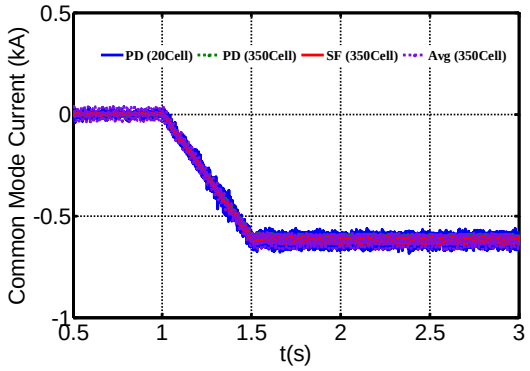
(d) Snapshot of phase 'a' upper arm current, i_{armUa}



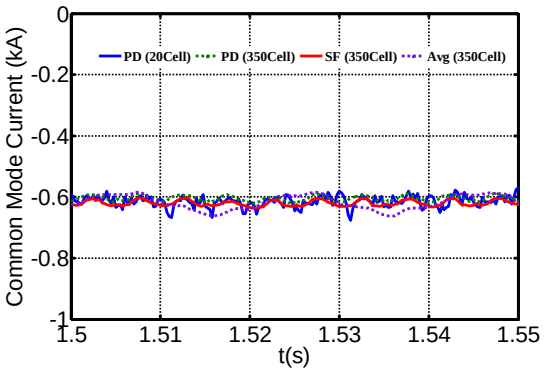
(e) Phase 'a' lower arm current, i_{armLa}



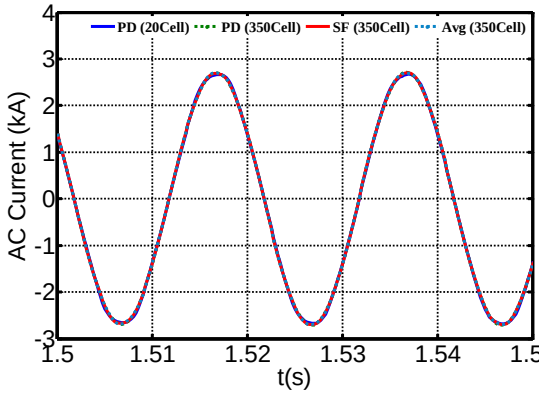
(f) Snapshot of phase 'a' lower arm current, i_{armLa}



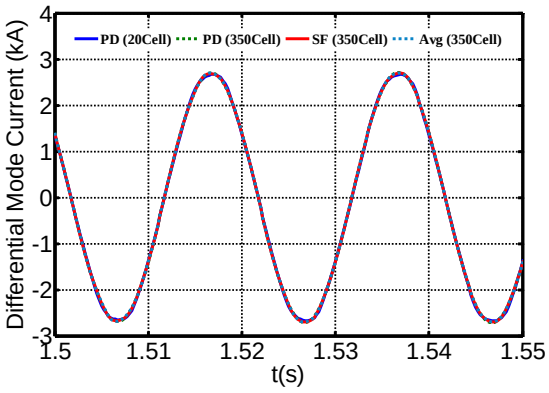
(g) Phase 'a' common-mode current, $i_{com} = \frac{1}{2}(i_{armUa} + i_{armLa})$



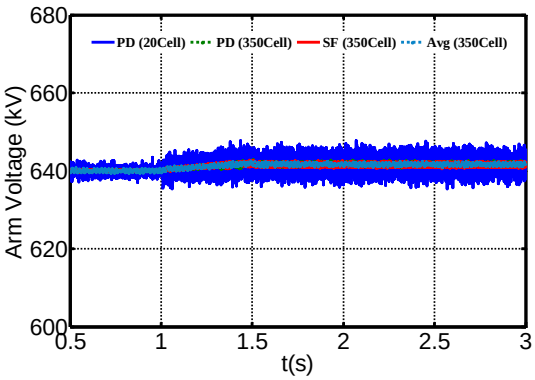
(h) Snapshot of phase 'a' common-mode current, $i_{com} = \frac{1}{2}(i_{armUa} + i_{armLa})$



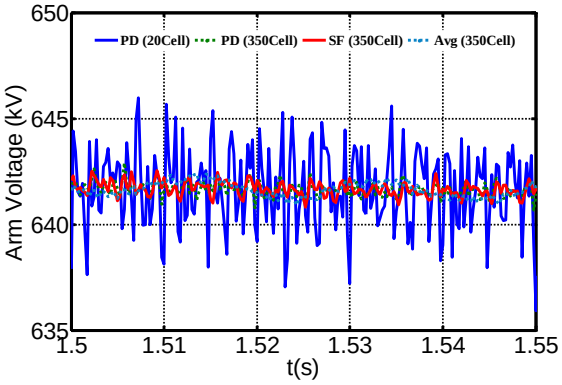
(i) Snapshot of the phase 'a' current 'i_{ao}'



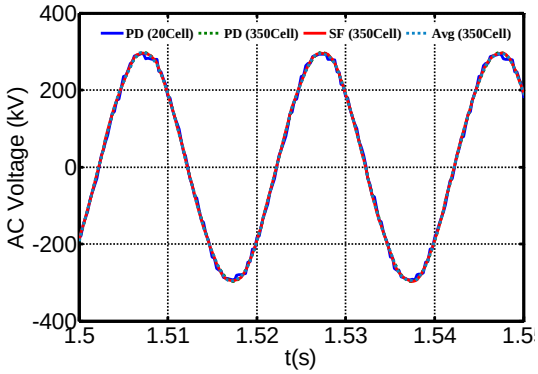
(j) Snapshot of phase 'a' differential-mode current, $(i_{armUa} - i_{armLa})$



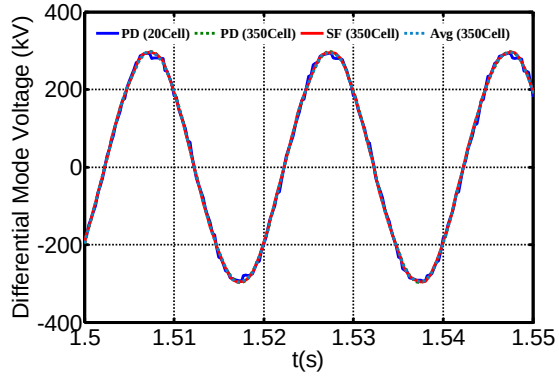
(k) Phase 'a' common-mode voltage, $(v_{armUa} + v_{armLa})$



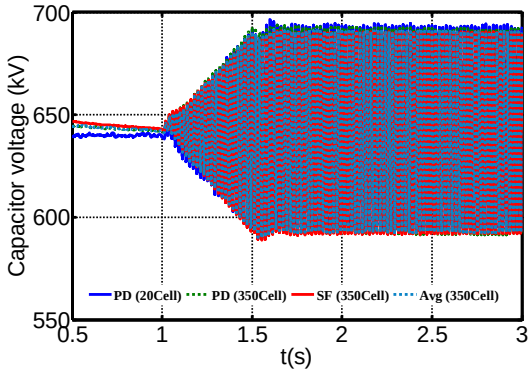
(l) Snapshot of phase 'a' common-mode voltage, $(v_{armUa} + v_{armLa})$



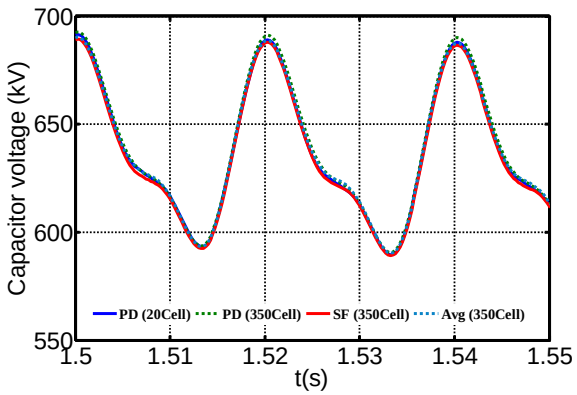
(m) Snapshot of converter terminal voltage 'v_{ao}'



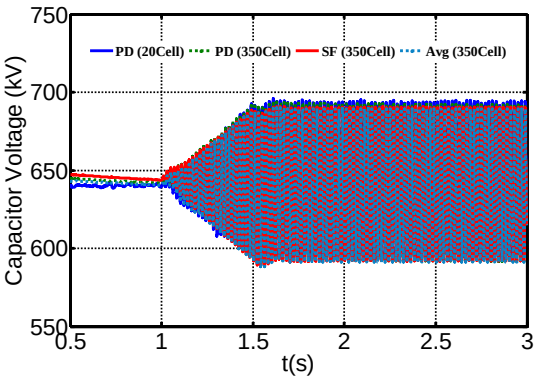
(n) Snapshot of phase 'a' differential-mode voltage, $½(v_{armLa} - v_{armUa})$



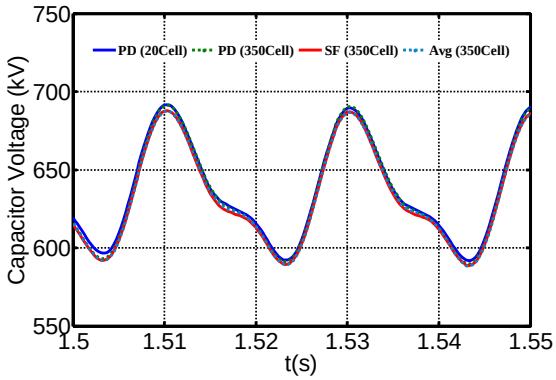
(o) Sum of the phase 'a' upper arm capacitor voltages



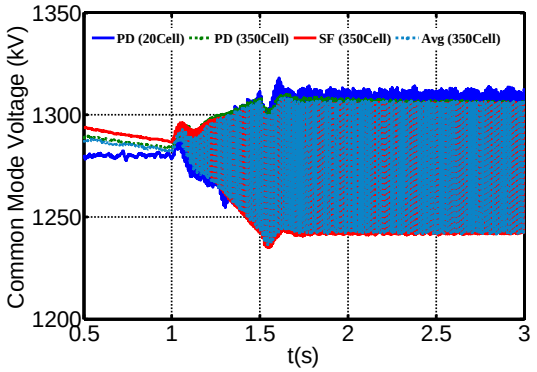
(p) Snapshot of sum of the phase 'a' upper arm capacitor voltages



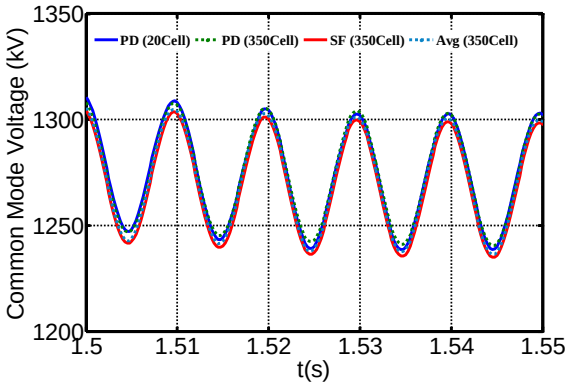
(q) Sum of the phase ‘a’ lower arm capacitor voltages



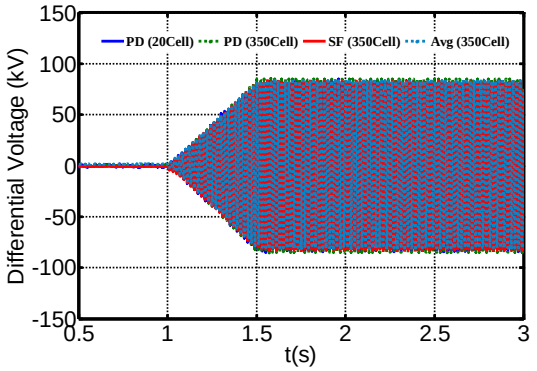
(r) Snapshot of sum of the phase ‘a’ lower arm capacitor voltages



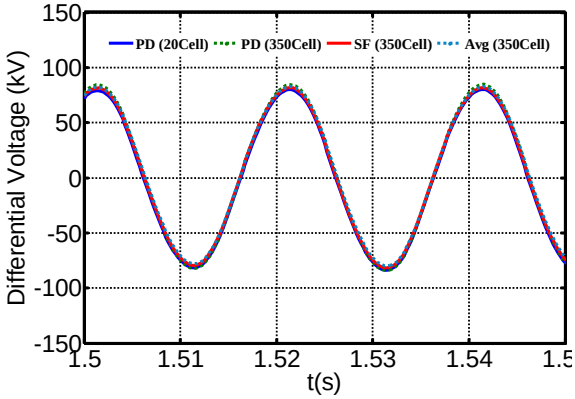
(s) Phase ‘a’ common-mode capacitor voltage sum, $\sum_{j}^{N_{SM}} V_{CSMUj} + \sum_{j}^{N_{SM}} V_{CSMLj}$



(t) Snapshot of phase ‘a’ common-mode capacitor voltage sum, $\sum_{j}^{N_{SM}} V_{CSMUj} + \sum_{j}^{N_{SM}} V_{CSMLj}$



(u) Phase ‘a’ differential-mode capacitor voltage sum, $\sum_{j}^{N_{SM}} V_{CSMUj} - \sum_{j}^{N_{SM}} V_{CSMLj}$



(v) Snapshot of phase ‘*a*’ differential-mode capacitor voltage sum, $\sum_{j}^{N_{SM}} V_{CSMUj} - \sum_{j}^{N_{SM}} V_{CSMLj}$

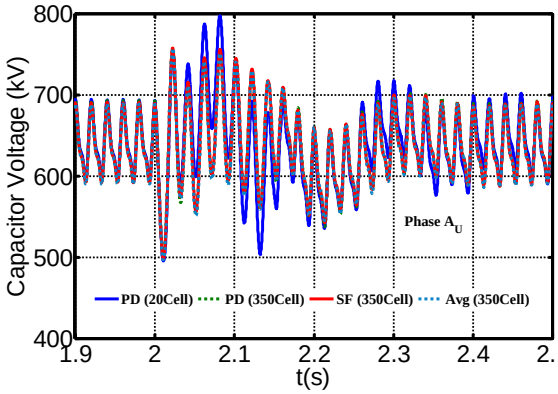
Fig. 3.6 Simulation waveforms during normal operation (‘PD’, ‘SF’ and ‘Avg’ stand for Thevenin equivalent, switching function and averaged models respectively)

3.2.2.2 *Three-phase-to-ground AC fault*

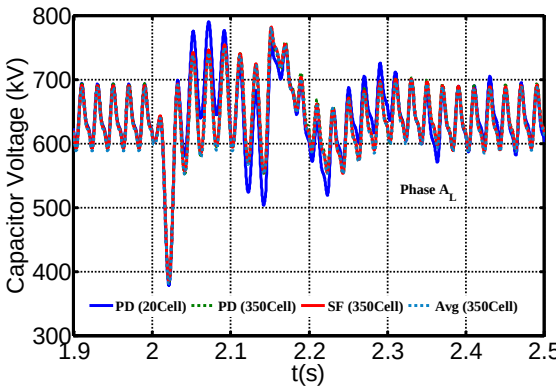
Further studies during AC faults are carried out using the 4 different models, and system operating conditions are summarised as follows:

- In pre-fault conditions, the MMC exports 1200MW from AC grid to the DC side at unity power factor.
- At t=2s, a temporary three-phase-to-ground AC short circuit fault (fault resistance equals 0.01Ω) with 140ms fault duration is applied at the point of common-coupling.
- The MMC active power set-point remains at 1200MW (unchanged) during fault and post-fault.

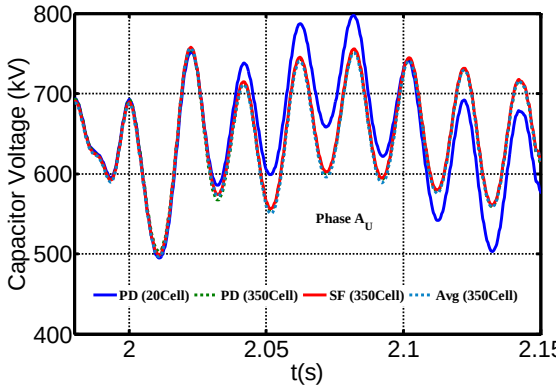
The AC fault location is at the PCC point as shown in Fig. 3.5. The temporary fault duration is set to be 140ms. Simulation waveforms that compare the responses of the above models are summarised in Fig. 3.7 and Fig. 3.8. The plots for the sum of the phase 'a' capacitor voltages and their snapshots in Fig. 3.7 (a)-(d) show that the capacitor voltages of the 20-SM MMC exhibit slightly larger oscillation compared to the rest of the models. The traces of the phase 'a' arm currents and their zoomed versions displayed in Fig. 3.7 (e)-(h) indicate that all the MMC models being compared are largely equivalent, with MMC having a reduced number of sub-modules per arm occasionally exhibits slightly larger ripple than the rest of the models during fault period, with the worst-case error of less than 0.5%. The waveforms for the other two phases are similar and thus are not included here. Fig. 3.8 (a)-(f) display the three-phase current waveforms the MMC injects into AC grid during the symmetrical three-phase fault, measured at the 400kV side of the interfacing transformer. These plots show no noticeable differences between the models being compared. Similarly, the plots for the grid voltages in Fig. 3.8 (g) to (h) are almost identical for all MMC models.


Capacitor Voltage (kV)
800
700
600
500
400
1.9
2
2.1
2.2
2.3
2.4
t(s)
Phase A_U
PD (20Cell)
PD (350Cell)
SF (350Cell)
Avg (350Cell)

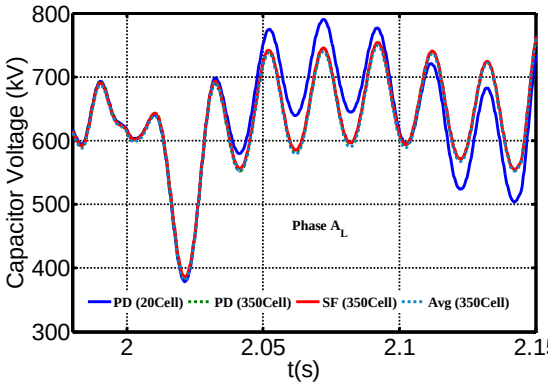
(a)


Capacitor Voltage (kV)
800
700
600
500
400
300
1.9
2
2.1
2.2
2.3
2.4
t(s)
Phase A_L
PD (20Cell)
PD (350Cell)
SF (350Cell)
Avg (350Cell)

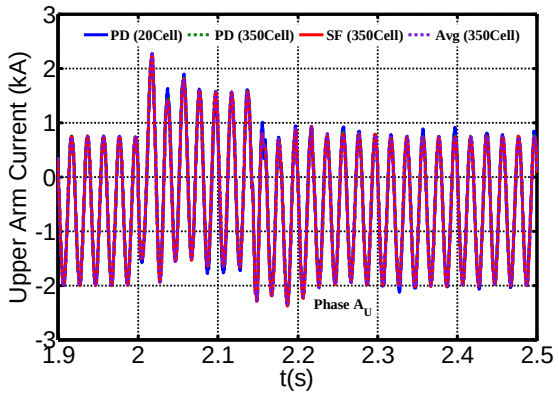
(b)


Capacitor Voltage (kV)
800
700
600
500
400
2
2.05
2.1
t(s)
Phase A_U
PD (20Cell)
PD (350Cell)
SF (350Cell)
Avg (350Cell)

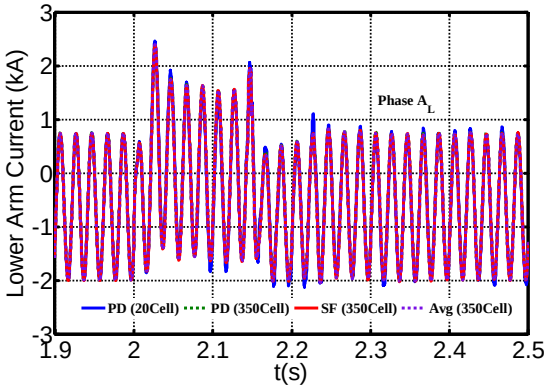
(c)


Capacitor Voltage (kV)
800
700
600
500
400
300
2
2.05
2.1
t(s)
Phase A_L
PD (20Cell)
PD (350Cell)
SF (350Cell)
Avg (350Cell)

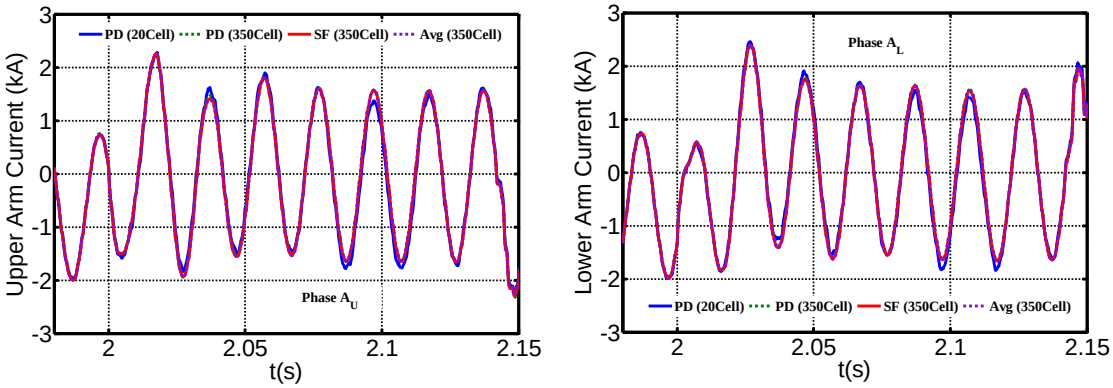
(d)


Upper Arm Current (kA)
3
2
1
0
-1
-2
-3
1.9
2
2.1
2.2
2.3
2.4
2.5
t(s)
Phase A_U
PD (20Cell)
PD (350Cell)
SF (350Cell)
Avg (350Cell)

(e)

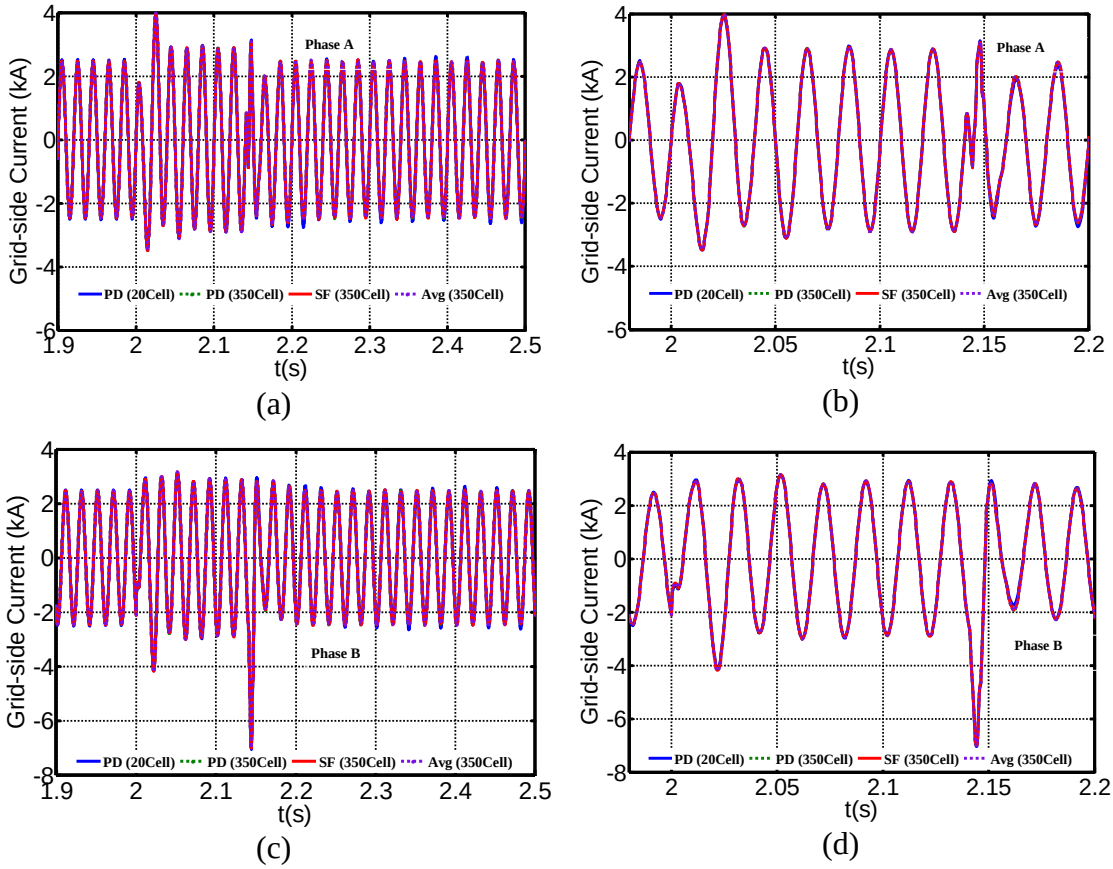

Lower Arm Current (kA)
3
2
1
0
-1
-2
-3
1.9
2
2.1
2.2
2.3
2.4
2.5
t(s)
Phase A_L
PD (20Cell)
PD (350Cell)
SF (350Cell)
Avg (350Cell)

(f)



(g) (h)

Fig. 3.7 Comparison of simulated phase-A waveforms during symmetrical three-phase AC fault compare for different developed MMC models



(a) (b)

(c) (d)

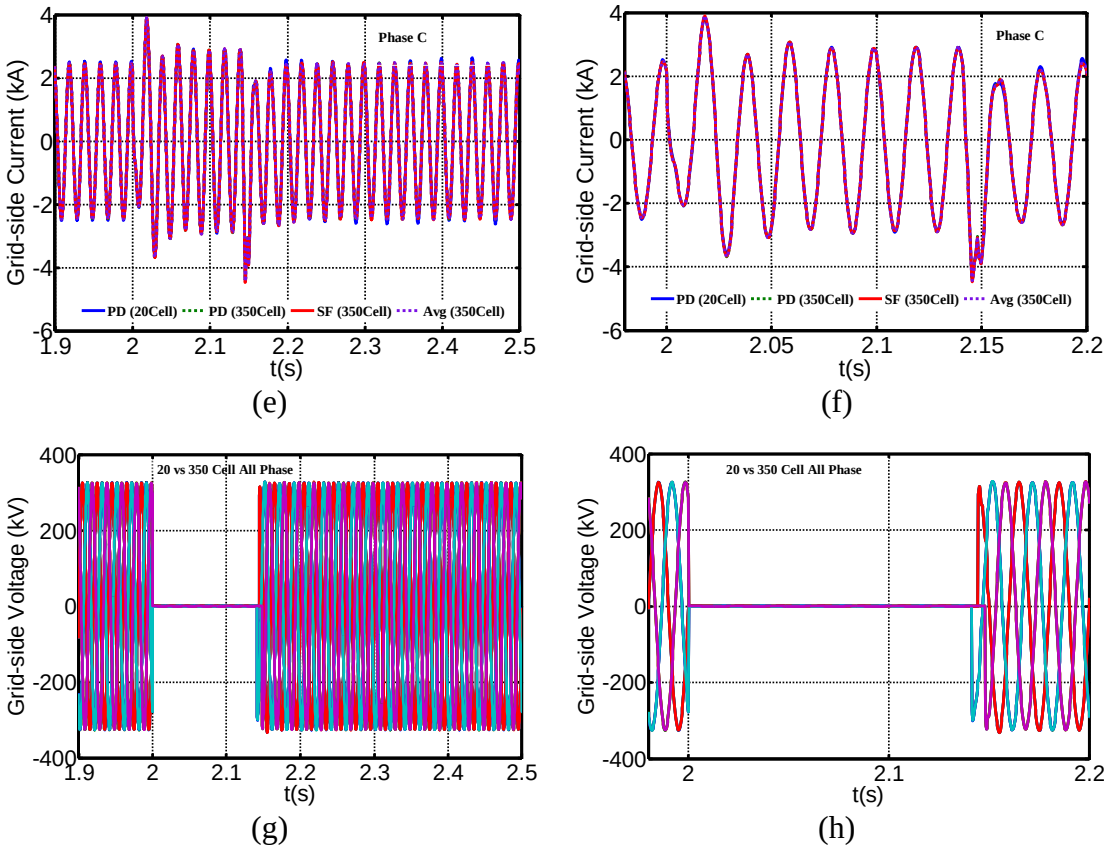


Fig. 3.8 Comparison of converter AC voltage and current of the developed MMC models to symmetrical three-phase AC network fault

3.2.2.3 *Pole-to-pole (P2P) DC short circuit fault*

System operating conditions for studies during a DC pole-to-pole faults are summarised as follows:

- In pre-fault conditions, the MMC exports 1200MW from AC grid to DC side at unity power factor.
- At t=3s, a permanent pole-to-pole DC short circuit fault (short circuit resistance equals to 0.005 Ω) is applied and converter blocking is activated after 50μs from fault inception.

In [117], a hardware demonstration with the DC fault protection operation process time equals to 41.31μs is given. 50μs is chosen in this case as DC fault protection operation process time. Fig. 3.9 compares the responses of the aforementioned MMC models to a solid pole-to-pole DC short circuit fault. The pole-to-pole DC link voltages and DC links

currents displayed Fig. 3.9 (a) and (b) indicate that the models exhibit almost identical behaviours during the DC fault transient. Fig. 3.9 (c) to (e) show that when the DC fault is detected and converter blocking is activated, the upper arm currents become unipolar and negative. These mean that the two components of arm currents during DC fault period flow through the freewheeling diodes of the main switches that bypass the SM capacitors, with the AC current in-feeds flow from the AC grid towards the DC side, and the DC fault current flows from the negative DC pole to positive DC pole through the MMC lower and upper arms. The lower arm currents have similar behaviour as the upper arm one s and thus not shown here. These typical MMC behaviours have been reproduced exactly by all MMC models. The plots in Fig. 3.9 (f) to (h) show that the upper arm SM capacitor voltages produced by all models are also similar, with the sum of the SM capacitor voltages of the MMC with 20 sub-modules per arm exhibit slightly different behaviours than the rest during normal operation, with the worst-case margin of error of less than 2%. Similar errors are observed in the sum of the capacitor voltages of the averaged and 20-SM MMC models when the converter is blocked during DC fault. Some of these observed small differences could be referred to several factors such as:

- The 20-SM MMC has much higher SM capacitor voltage than that with 350-SM MMC, and this may slightly affect the inter-SM and inter-arm dynamics, and final settling voltage for the SM capacitor following converter blocking.
- Larger switching voltage of the 20-SM MMC increases the errors between the input DC link voltage and common-mode voltage MMC presents at its DC terminal. As a consequence, for the same arm inductor, the MMCs with 20-SM per arm exhibit low-quality arm currents compared to that with a large number of sub-modules per arm.
- The assumptions made in the development of the MMC averaged model such as the SM capacitor voltages of the entire arm oscillate together (ignorance of individual SM capacitor dynamics) can slightly affect the internal dynamics of the MMC averaged model.

In general, from the results shown in Fig. 3.9 it can be concluded that all the MMC models are able to reproduce the expected MMC behaviour during pole-to-pole DC short circuit fault, with sufficient accuracies and efficiencies.

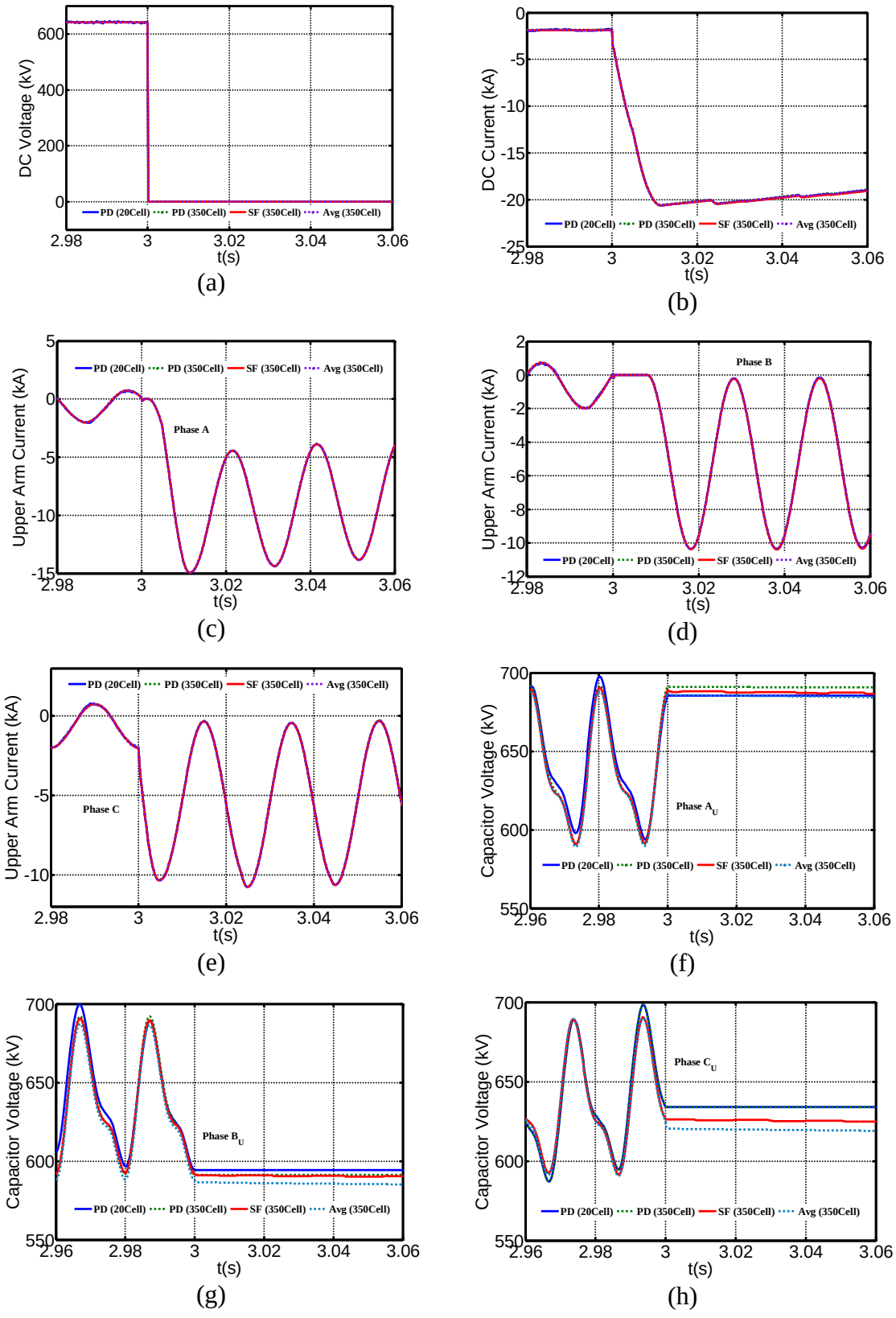


Fig. 3.9 Comparison of simulation waveforms during DC short circuit fault with different MMC models

3.2.2.4 *Comparison of simulation speed*

Simulation efficiencies of different HB-MMC models are summarized in Table 3, when all the models are configured as a single terminal, with all controllers stated earlier are incorporated, for 1-second simulations. These simulations were conducted using PSCAD 4.6 on HP computer with Intel(R) Core (TM) i7-6700 CPU @ 3.4GHz, 16GB RAM and 64-bit Windows 10 Enterprise system.

From the results displayed in Table 3, it is clear that the averaged HB-MMC model is the most efficient one and is followed by the switching function and then Thevenin equivalent, while detailed switching model is the slowest due to the largest number of electrical nodes.

Table 3 Comparison of simulation speed using different MMC models

Types of MMC Model	**No. of Sub-modules (N)**	**Simulation Run Time (10Sec)**	**Simulation Time Step (µs)**	**Channel Plot Step (µs)**
Averaged Model	350	25s	50	50
Switching Function Model	350	57s	50	50
PSCAD Thevenin equivalent	350	166s	50	50
PSCAD Thevenin equivalent	20	87s	50	50
Switching Function Model	20	34s	50	50
Detail Switching Model	20	39minutes and 54s	50	50

3.2.3 **Real-time model development and validation**

It has been proven that the MMCs with a reduced number of SMs per arm (20 SMs Thevenin equivalent model) and the averaged MMC model are capable of reproducing the typical behaviour of MMCs with a large number of SMs per arm (350 SMs Thevenin equivalent and switching function models) in Section 3.2.2, with negligible errors. It has also been established that the average and switching function MMC models offer the fastest simulation times, without significant sacrifice in the accuracy of the results in a wide range of system-level studies including AC and DC faults. Therefore, this section presents a detailed development of the real-time MMC simulation models, namely, the

20-SM switching function and averaged models, and their validation against offline PSCAD 20-SM switching models.

The operating conditions for all fault cases in this section are summarised as follows:

- The orders for the rated active and reactive powers exchange between the MMC and AC grid are 1200 MW and 400 MVAr respectively, under all operating conditions. The power flow from AC toward the converter is defined as positive.
- All fault studies are performed as successive events as summarized below:
    - At *t*=2s, a 300ms temporary solid single-phase-to-ground AC fault is applied at the point of common-coupling (PCC_1).
    - At *t*=4s, a 300ms temporary solid symmetrical three-phase-to-ground AC fault is applied at PCC_1.
    - At *t*=6s, a permanent pole-to-pole DC short circuit fault is applied in the DC side, and converter blocking is activated 50μs after fault inception.
    - In another case at *t*=3s, a permanent pole-to-ground DC short circuit fault is applied in the DC side, and converter blocking is activated 50μs after fault inception.

3.2.3.1 *Implementation in RTDS*

Fig. 3.10 depicts a generic layout of the developed MMC model using real-time digital simulation (RTDS) dual time step technique. The MMC models with the requirements of high switching frequency are built in small time step (i.e. 1.4-2.5μs), whilst the AC grid source is modelled in a larger time step (i.e. 50 μs).

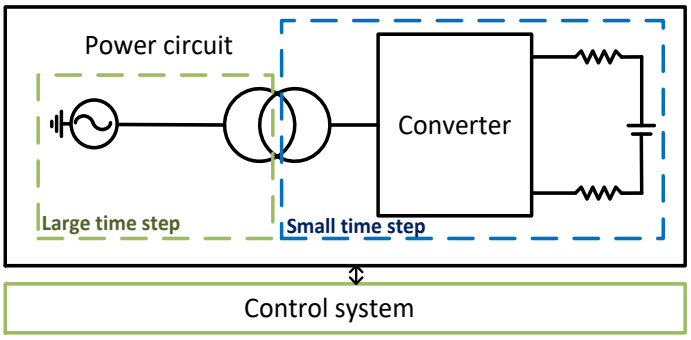


Fig. 3.10 A single terminal MMC system modelling method in RTDS

On the basis of detailed discussions of the MMC modelling presented in Section 3.1, real-time user-defined 20-SM switching function and averaged half-bridge MMC models are

developed using RSCAD in RTDS simulation platform. The developed models are validated against an offline 20-SM half-bridge MMC switching function model developed in PSCAD. The number of SMs in the developed RTDS model can be easily scaled and modified if more details are required and sufficient RTDS modelling hardware capacity is available.

The RTDS switching function and averaged HB-MMC models as shown in Fig. 3.4 and Fig. 3.2 consist of two parts:

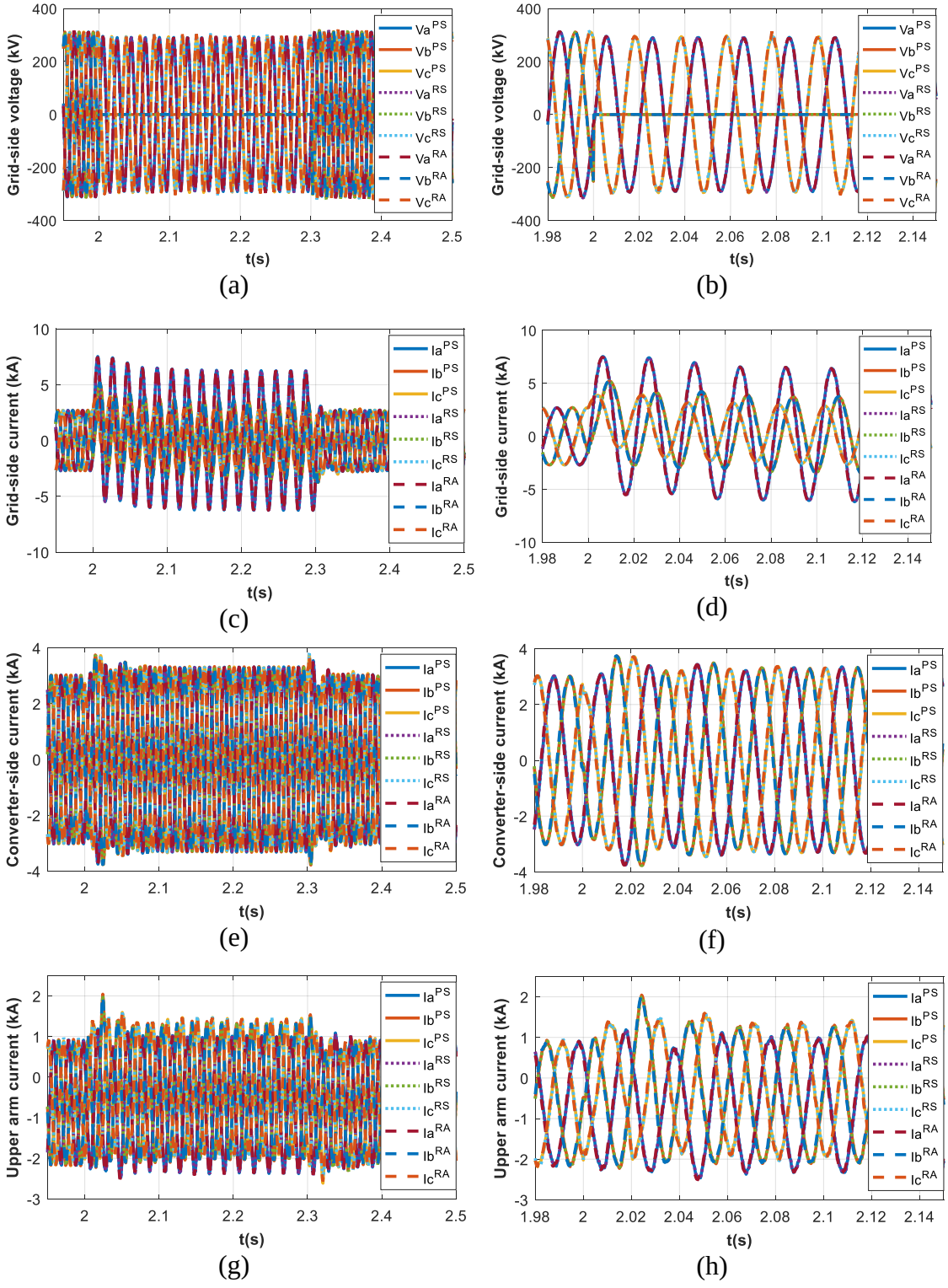
- The power circuit part which includes controllable voltage sources, arm inductors and IGBTs and diodes being used to mimic the half-bridge MMC blocking state.
- The calculation part that simulates the half-bridge MMC SM dynamics and generates the upper and lower arm voltages V_{armU} and V_{armL}.

In RTDS platform, the power circuit part of the MMC switching function and averaged HB-MMC models and its associated components such as the DC side circuit and interfacing transformer are placed in a dedicated small time step template called "VSC bridges" available in RSCAD library with time step ranging from 1.4μs to 2.5μs. While the part that calculates the SM capacitor dynamics and control systems are placed in a dedicated large time-step template of 50μs. The user-defined components that implement the calculations of SM capacitor dynamics and voltage balancing are realised in MATLAB-SIMULINK and then converted to RSCAD using the real-time embedded code generation that can optimise the generated code for a number of objectives such as code efficiency, RAM usage, traceability, etc. The whole real-time simulation model of the test system is implemented on one RTDS rack, with a PB5 card containing two processors and three GPC cards. Both processors on the PB5 card are assigned to solve the power circuit that operates at a small-time step, with the calculation part of each of the three-phase on a separate GPC processor. Since the aim is to validate the MMC behaviours under a number of operating conditions, the DC side of the half-bridge MMC is modelled by stiff DC voltage source and one pi-section per DC cable. The connection between the AC system that operates at large time-step and the MMC power circuit and its DC side components which operate at small time-step is realised by using a VSC interface transformer from the RSCAD small time-step library.

3.2.3.2 *Single-phase-to-ground AC fault*

Fig. 3.11 displays simulation waveforms for a single-phase-to-ground AC fault (fault resistance equals 0.01Ω). The controllers in the models regulate the converter negative sequence currents to be zero. The acronyms P, R, S and A displayed in the legends attached to simulation waveforms stand for offline PSCAD, RTDS, SFM and averaged model respectively. Fig. 3.11(a), (b), (c), (d), (e) and (f) show full-scaled and zoomed simulation waveforms for three-phase PCC voltages, AC currents MMC injects into PCC, and converter side AC currents. The zoomed waveforms are captured around the instant of fault inception. These waveforms show that the real-time waveforms of the 20-SM switching function and average models are identical, and both exhibit negligible errors in the first few peaks of the AC side currents (grid and converter sides). It can also be seen from Fig. 3.11 (e) and (f) that the converter three-phase currents are balanced event during the single-phase fault. Similarly, the plots for the upper arm currents displayed in Fig. 3.11 (g) and (h) also show that there are small errors in the first few peaks of the arm current following AC fault inception, but quickly disappeared. The plots for the sums of the upper SM capacitors of the three models in Fig. 3.11 (i) to (j) again indicate good match between the real-time and offline simulations. The lower arm currents and SM capacitor voltages show similar trends as those of the upper arm one and thus are not shown. Fig. 3.11(k)-(m) show that the real-time and offline simulation waveforms for the active and reactive powers, and DC link current during the single-phase AC fault are similar, with small errors appear in the reactive power during fault period. Detailed investigation of the errors observed between the reactive powers of the PSCAD and RTDS reveals that the interfacing transformer model in RSCAD is the main cause. For the same transformer parameters, the measured reactive power consumptions of the interfacing transformers are different in the two platforms (PSCAD and RSCAD), with PSCAD exhibiting a slightly higher reactive power consumption. Further investigation at control system level also shows that during the steady-state condition, the PSCAD and RSCAD achieve the same reactive power of 400MVAr by slightly different quadrature currents (i_q), with magnitudes of the errors between the two platforms being less than 20A.

The results of the detailed validation of the real-time and offline simulation shown in Fig. 3.11 confirm the suitability of the presented real-time user-defined MMC models (20-SM switching function and averaged) for studying single-phase-to-ground AC faults.



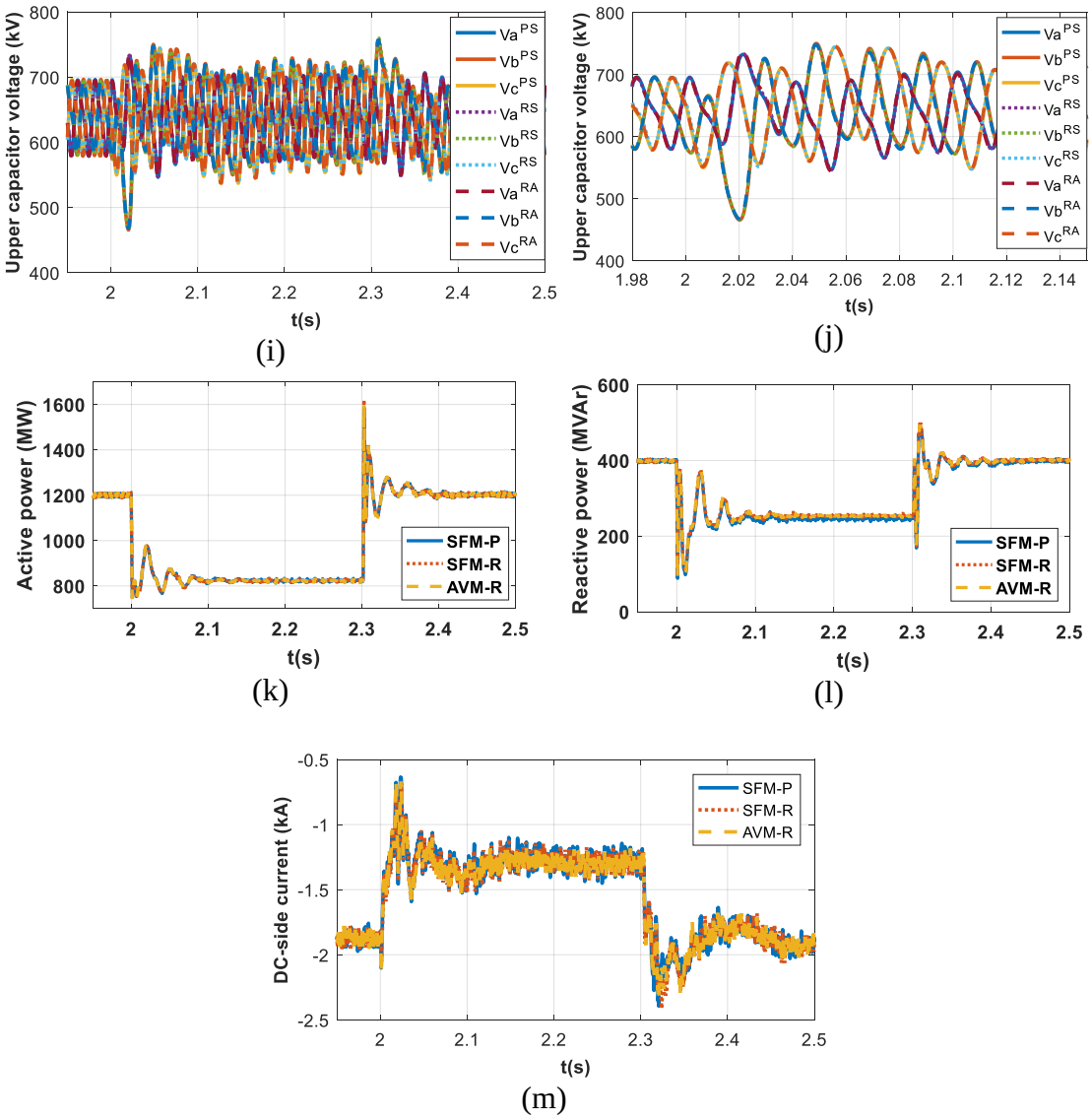


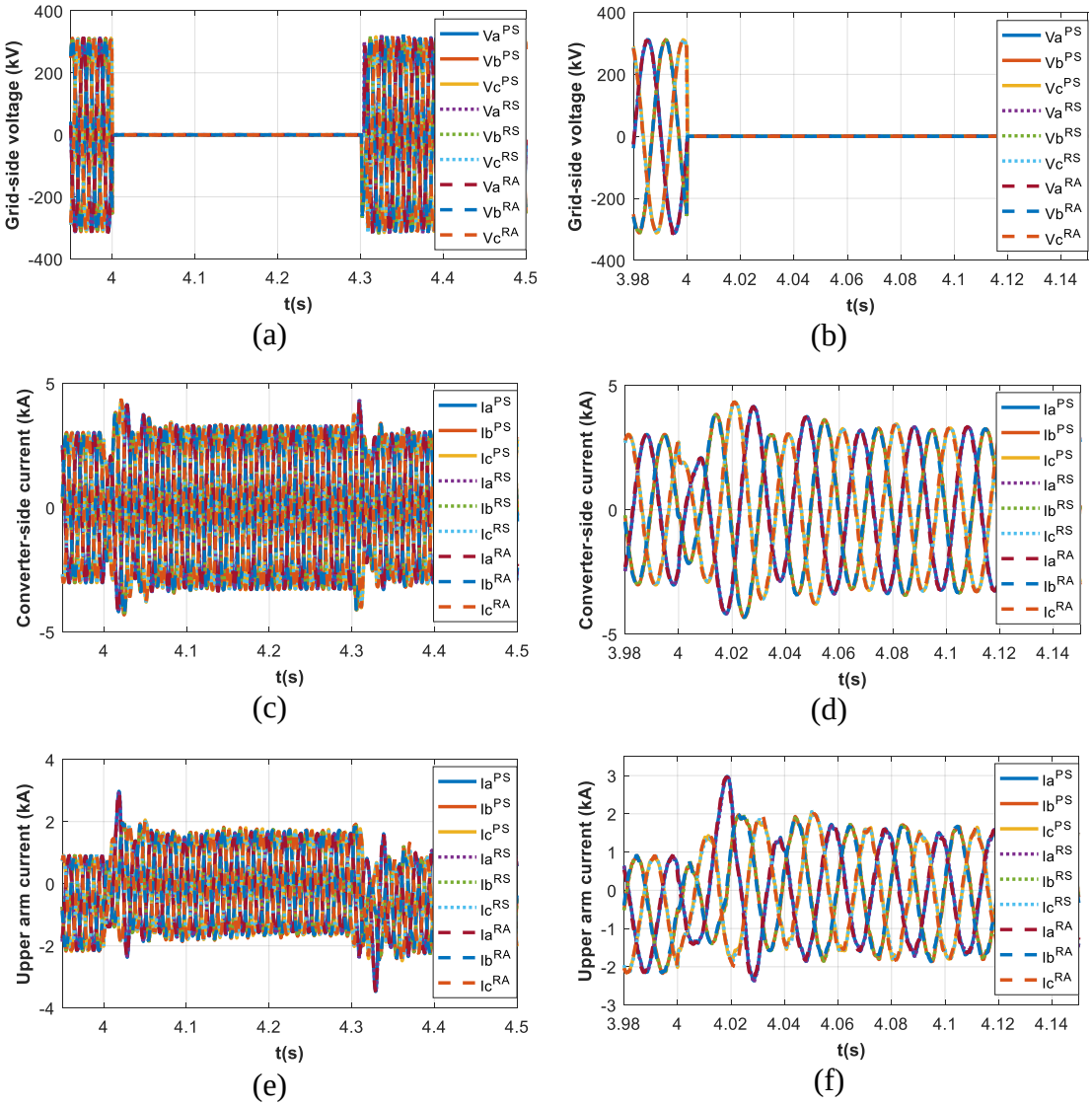
Fig. 3.11 Simulation waveforms comparing the transient behaviours of 20-SM offline and RTDS switching function models and averaged RTDS model during a single-phase-to-ground AC fault

3.2.3.3 *Three-Phase-to-Ground AC Fault*

Fig. 3.12 displays simulation waveforms for a three-phase-to-ground AC fault (fault resistance equals 0.01Ω). Fig. 3.12 (a), (b), (c) and (d), show a full-scaled and zoomed simulation waveforms for the three-phase PCC voltages and three-phase MMC converter currents. All zoomed waveforms are captured around the instant of fault inception. These waveforms show that the real-time waveforms of the 20-SM switching function and

average models are largely indistinguishable, with both exhibit negligible errors relative to that of the offline simulation. Similarly, the plots for the upper arm currents displayed in Fig. 3.12(e) and (f), and the sums of the upper SM capacitors voltage in Fig. 3.12 (g) and (h) also show a good match with negligible errors. Fig. 3.12 (i)-(k) show that the real-time and offline simulation waveforms for the active and reactive powers and DC link current during the three-phase-to-ground AC fault are similar with extremely small errors around the instants of fault inception and clearance.

Detailed corroboration of the real-time and offline simulation results shown in Fig. 3.12 confirm the suitability of the presented real-time used defined MMC models (20-SM switching function and averaged) for studying three-phase-to-ground AC faults.



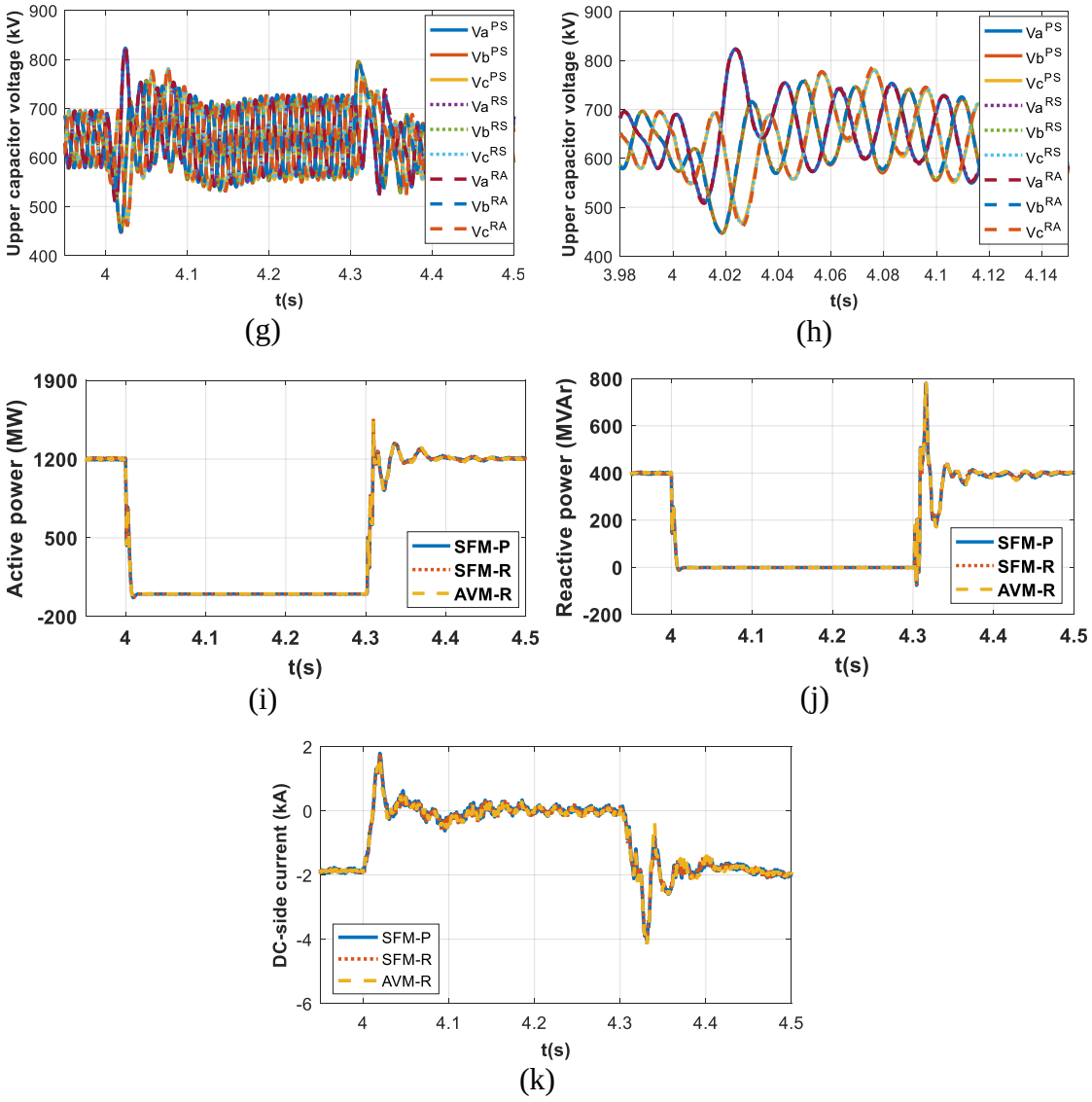


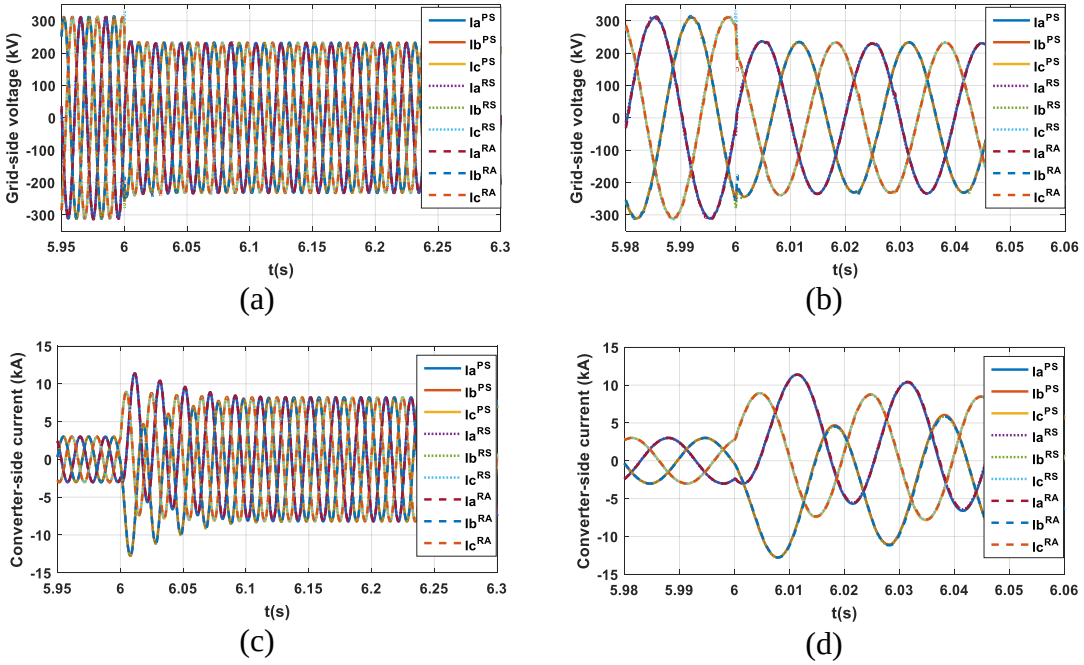
Fig. 3.12 Simulation waveforms comparing the transient behaviours of 20-SM offline and RTDS switching function models and averaged RTDS model during a three-phase-to-ground AC fault

3.2.3.4 *Pole-to-Pole DC short circuit fault*

Fig. 3.13 presents simulation waveforms for a solid pole-to-pole DC fault (short circuit resistance equals to 0.005 Ω) right at MMC DC terminals. Fig. 3.13 (a) and (b), and (c) and (d) show simulation waveforms for the three-phase PCC voltages and MMC converter side currents, including the expanded snapshots around the instant of fault inception. These traces show that all the real-time and offline simulations waveforms are

identical (real-time simulation waveforms of the 20-SM switching function and average models superimposed on that of the 20-SM offline PSCAD waveforms). Also, the upper arm currents and the sums of the upper arm SM capacitors from the real-time and offline simulations displayed in Fig. 3.13 (e) and (f), and (g) and (h) do not exhibit any visible errors in steady-state and during the DC fault. Fig. 3.13 (i)-(l) show that the real-time and offline simulation waveforms for the active and reactive powers and DC link current and voltage during the DC short circuit are similar, with a small difference in the active powers during fault period. The differences observed in the active power during the DC fault is due to small differences in the total resistance in the fault current path, due to the implementation of the parts that mimicking the blocking of physical MMC (recall that the two platforms, PSCAD and RSCAD have different implementation of the IGBTs and diodes). These differences are exacerbated during DC short circuit fault by the significant increase in the magnitude of the fault currents relative to rated currents.

Results of detailed validation displayed in Fig. 3.13 confirm the appropriateness of the presented real-time user-defined MMC models (20-SM switching function and averaged) for studying pole-to-pole DC short circuit faults.



(a) (b)

(c) (d)

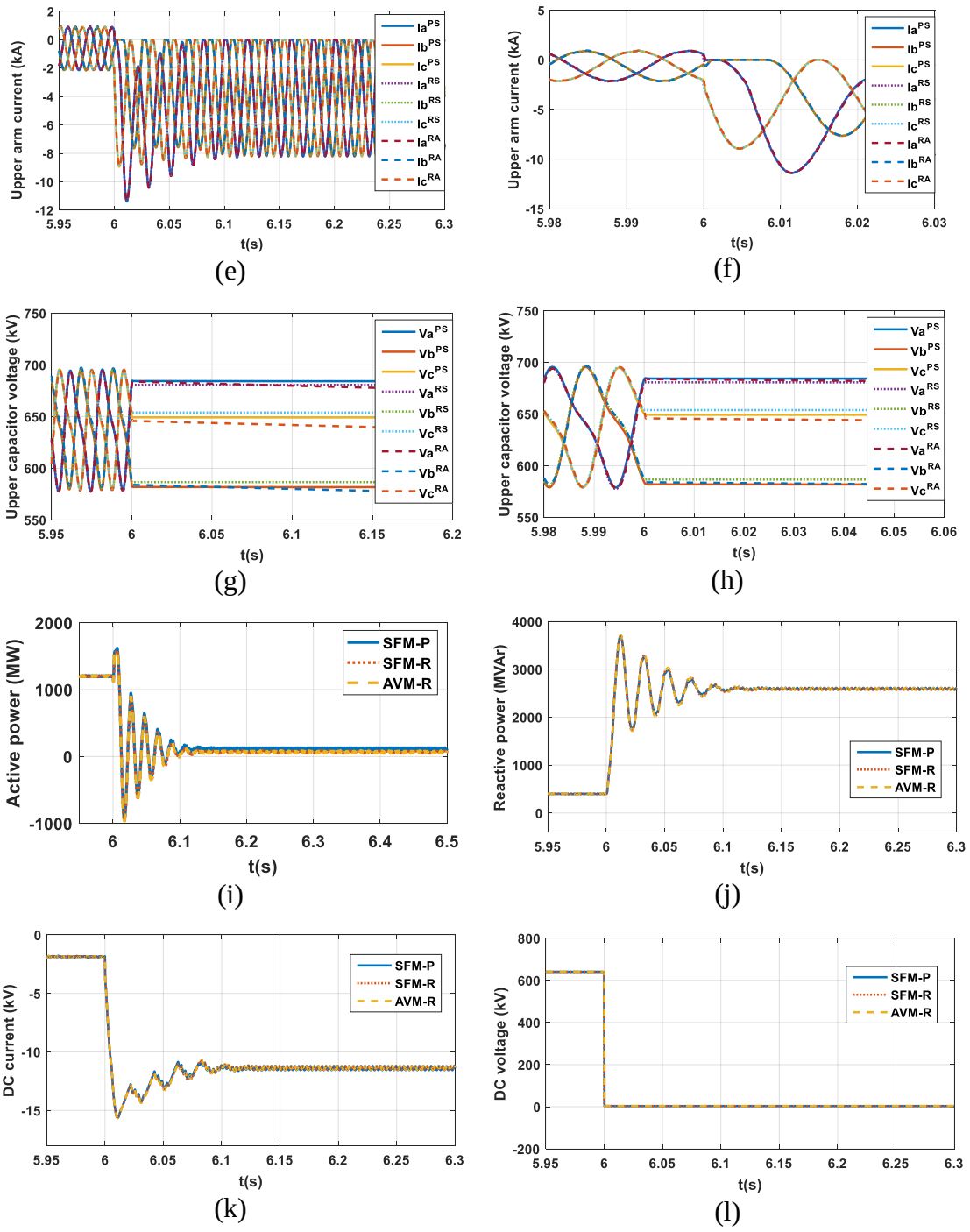


Fig. 3.13 Simulation waveforms comparing the transient behaviours of 20-SM offline and RTDS switching function models and averaged RTDS model during DC short circuit fault

Further validations during AC phase-to-phase fault and DC pole-to-ground fault have also been carried out and the results show a good match among the three different models. Due to their similarity to the previously presented results, they are not shown here.

3.3 Summary

This chapter has presented a number of modelling methods of the HB-MMC, including the theoretical basis that underpins each modelling method, and basic assumptions made in the development of each method. The comprehensive comparison of the offline simulation waveforms reveals that the averaged and switching function HB-MMC models produce practically the same results as that of the Thevenin equivalent MMC model of the PSCAD MMC library, but with much greater simulation efficiency. This conclusion is valid for a wide range of studies, including normal steady-state operation and faults. Similar voltage and current stresses are observed on the MMC active and passive components. The detailed validation of real-time user-defined switching function and averaged HB-MMC models against an offline validated PSCAD switching function model shows that the offline and real-time simulation waveforms are in good agreement during normal operation, symmetrical and asymmetrical AC faults, and DC faults.

Chapter 4 Interoperability of different VSC topologies in HVDC grids

In the last decade, a number of MMC topologies have been proposed for HVDC applications. The half-bridge (HB) and full-bridge (FB) MMCs have emerged as the preferred topologies for commercial application. In the meantime, several hybrid MMC converters have been proposed as alternatives that offer important trade-offs between footprint, semiconductor loss, resiliency to AC and DC network faults and control range, when compared to the HB-MMC and FB-MMC [34]-[35].

Although the construction of large-scale DC grids using different converter topologies is important from both practical and market point of view, particularly for prevention of monopoly in supply chains, ensuring safe and reliable operation of DC grids with such diversity, present significant technical challenges; especially, during fault conditions. Meaningful assessments of the interoperability of such complex DC grids, with equipment supplied by multiple vendors, require converter models with steady-state and transient behaviours that accurately resemble the typical behaviour of physical systems.

This chapter examines the suitability of the developed offline and real-time averaged converter models for a detailed assessment of interoperability of different converters in a meshed DC grid. Interoperability of a few selected representative converter topologies, namely, the HB and FB MMCs and hybrid MMC consisting of 50% FB SMs and 50% HB will be assessed quantitatively using offline PSCAD and real-time RSCAD simulations.

4.1 Alternative VSC topologies

The development of the FB-MMC and hybrid MMC with 50% FB SMs and 50% HB in PSCAD and RSCAD are detailed here.

4.1.1 Modelling and control of Full-bridge and Hybrid MMCs

Fig. 4.1 shows a generic power circuit of a three-phase MMC converter that consists of six arms, with each arm comprising of an inductor and a stack of FB SMs, or combination of the HB and FB SMs as displayed in Fig. 4.2. Similar to HB-MMC, each arm of the MMC in Fig. 4.1 and 4.2 must be capable of blocking the rated pole-to-pole DC voltage. Complementary operation of the arms that constitute the same phase-leg is necessary to ensure that each phase-leg inserts an appropriate number of SM capacitors (from the upper and lower arms) into the power path in order to build-up the needed instantaneous common-mode voltage to counter the DC link voltage. For each MMC phase leg containing *2N* SMs, only N_x SMs could be selected for insertion into the power path, and the remaining $2N$-N_x must be bypassed. The exact number of SMs could be inserted into power path depends on several factors such as the designed rated voltage per SM, and the type of SMs being employed in each MMC arm (HB, FB etc.) [26][118].

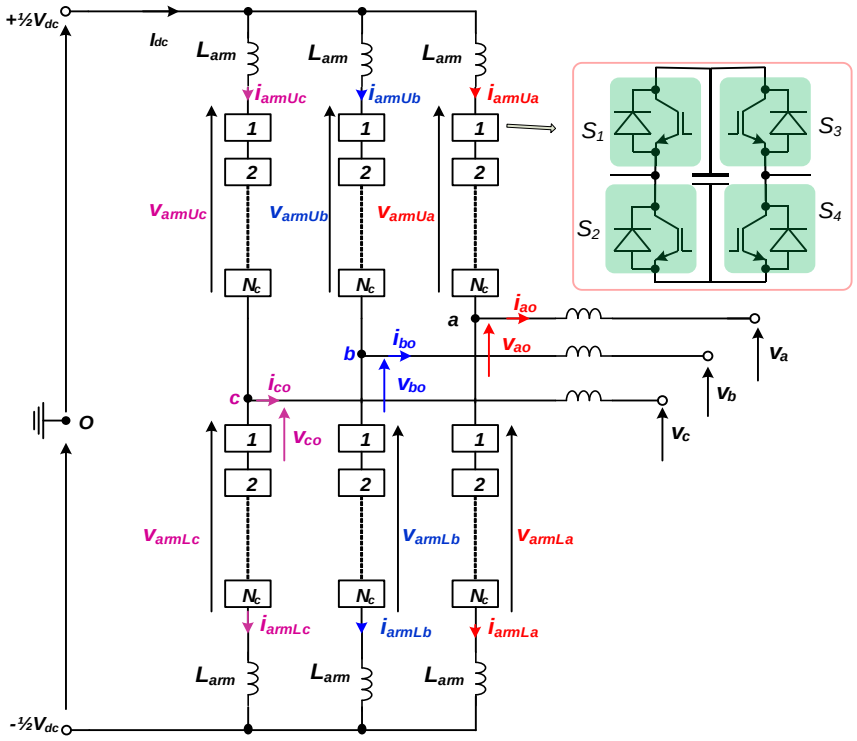


Fig. 4.1 Basic circuit of the three-phase modular multilevel converter

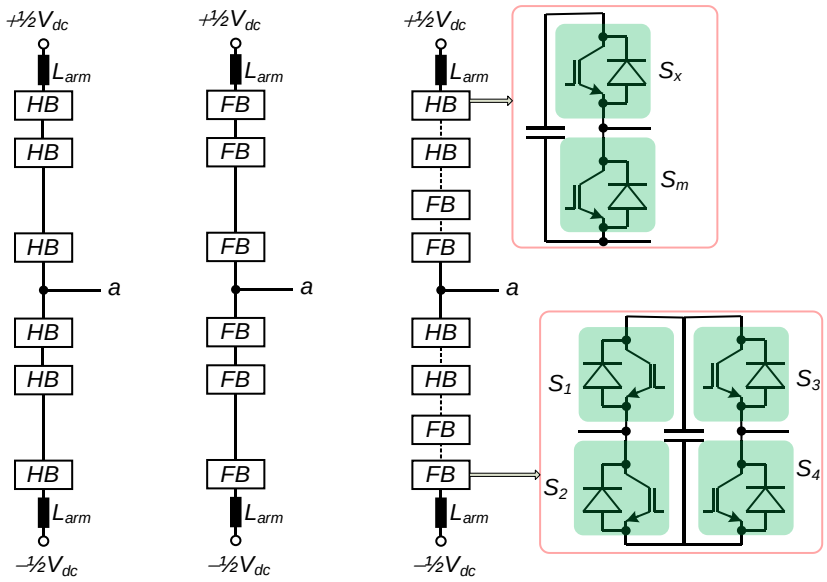


Fig. 4.2 Phase-legs of half-bridge, full-bridge and hybrid modular converters

As already being expressed in Chapter 2, the upper and lower arm voltages (V_{armU} and V_{armL}) for one phase of the generic MMC in Fig. 4.1 can be approximated as:

$$V_{armU} \approx \tfrac{1}{2} V_{carmU} \left[\alpha - m\sin(\omega t + \delta)\right] \approx V_{carmU} m_U \tag{4.1}$$

$$V_{armL} \approx \tfrac{1}{2} V_{carmL} \left[\alpha + m\sin(\omega t + \delta)\right] \approx V_{carmL} m_L \tag{4.2}$$

where V_{carmU} and V_{carmL} are the sums of the upper and lower arm capacitor voltages, which must be regulated such that $V_{carmU} = V_{carmL} = V_{carm}^{*} \geq V_{dc}$ (V_{carm}^{*} is the rated arm capacitor voltage). The DC modulation index is defined as $\alpha = V_{dc} / V_{carm}^{*}$, and m_U and m_L are the upper and lower arm modulation functions, respectively. For FB MMC, the DC modulation indexes 'α' can vary widely in the range of $-1 \leq \alpha \leq 1$.

Similar to HB-MMC, controlling the sums of the upper and lower arm capacitor voltages at $V_{carmU} = V_{carmL} = V_{carm}^{*} \geq V_{dc}$ means the existence of redundant SMs in the MMC arms. Apart from reliability improvement in HB-MMC, these redundant SMs do not offer any added value because of the well-known limitations of the unipolar HB SMs [26][118]. However, in FB and hybrid MMCs, the redundant SMs in their arms can offer additional

features such as over-modulation (ability to generate or operate with higher AC side voltage than the HB-MMC). Although hybrid MMC can offer such features during normal operation, sustaining such feature during operation with extremely low DC voltage such as active control during DC short circuit faults requires the number of FB SMs in the arms to be increased, as during such operations, FB SMs alone will be responsible for the synthesis of the negative arm voltages [27][119][120]. Apart from the aspects highlighted above, the fundamental operation and control of the FB and hybrid MMCs remain the same as that of the HB-MMC which has been extensively discussed in Chapter 2. These differences will be articulated and emphasized throughout this chapter where appropriate.

4.1.1.1 *Detailed switching model*

Typical detailed switching models of the FB and hybrid MMCs use in-depth representations of the FB and HB SMs (SM capacitors and switching devices), where each power electronics switch mimics the conduction pattern and switching characteristics of its physical equivalent (such as the IGBT and anti-parallel diode). For instance, when the arm current defined in Fig. 4.3(a) is assumed to be positive; the basic operation of the FB SM can be summarised as follows:

- Switching devices S_1 and S_2, and S_3 and S_4 represent two complementary pairs operating as two independent legs.
- When S_1 is on and S_3 is off, the FB SM in Fig. 4.3(b) generates an output voltage $V_{sm}=V_{CSM}$, where V_{CSM} represents the SM capacitor voltage. In this switching state, a positive arm current ($I_{arm}>0$) charges the SM capacitor, while the negative arm current ($I_{arm}<0$) discharges the SM capacitor. Additionally, each switching device in off-state such as S_2 and S_3 experiences voltage stress equal to capacitor voltage V_{CSM}.
- When S_1 is off and S_3 is on, the FB SM in Fig. 4.3(c) generates an output voltage $V_{sm}=-V_{CSM}$. In this switching state, a positive arm current ($I_{arm}>0$) discharges the SM capacitor, and negative arm current ($I_{arm}<0$) charges the SM capacitor. Also, both switching devices in off-state such as S_1 and S_4 experience voltage stress equal to V_{CSM}.

- When both switches S_1 and S_3 are on (or off), the FB SM in Fig. 4.3(d) and (e) generates an output voltage $V_{sm}=0$. In this switching state, both positive and negative arm currents do not affect the SM capacitor voltage.
- When all switching devices (S_1, S_2, S_3 and S_4) are gated off during blocking state as shown in Fig. 4.3(f), both positive and negative arm currents shown in red and blue find path through the anti-parallel diodes of the switches S_1, S_2, S_3 and S_4 and charge the SM capacitor.

As in HB-MMC case described in Chapter 3, DSM accounts for each IGBT turn-on and turn-off times and its on-state resistance and voltage drop. Such exhaustive representation necessitates the use of stiff solvers with small time steps leading to very longer simulation times, high computation burden, and large memory requirement.

4.1.1.2 *Switching function model*

As stated in section 3.1.4, the switching function modelling methods represent each IGBT and its anti-parallel diode by an ideal switch that denotes the on and off states by 1 and 0 respectively. Considering Fig. 4.3 (a) as the i^{th} FB SM in the MMC arm, its output voltage (V_{smi}) can be expressed in terms of the SM capacitor voltage (V_{CSMi}) and switching states of the two upper (or lower) switches S_1 and S_3 as:

$$v_{smi}(t) = (S_{i1} - S_{i3})V_{CSMi}(t) \tag{4.3}$$

Similarly, the SM capacitor current of each SM can be related to the MMC arm current by:

$$i_{csmi}(t) = (S_{i1} - S_{i3})I_{arm}(t) \tag{4.4}$$

And the SM capacitor voltage can be calculated at each time step as

$$V_{CSMi}(t) = \frac{1}{C_{SM}} \int i_{csmi}(t)dt \tag{4.5}$$

Equation (4.5) is transformed into discrete from using Tustin (trapezoidal integration method) as:

$$V_{CSMi}(t) = V_{CSMi}(t-\Delta t) + \tfrac{1}{2}\frac{\Delta t}{C_{SM}}\left[I_{csmi}(t) + I_{csmi}(t-\Delta t)\right] \tag{4.6}$$

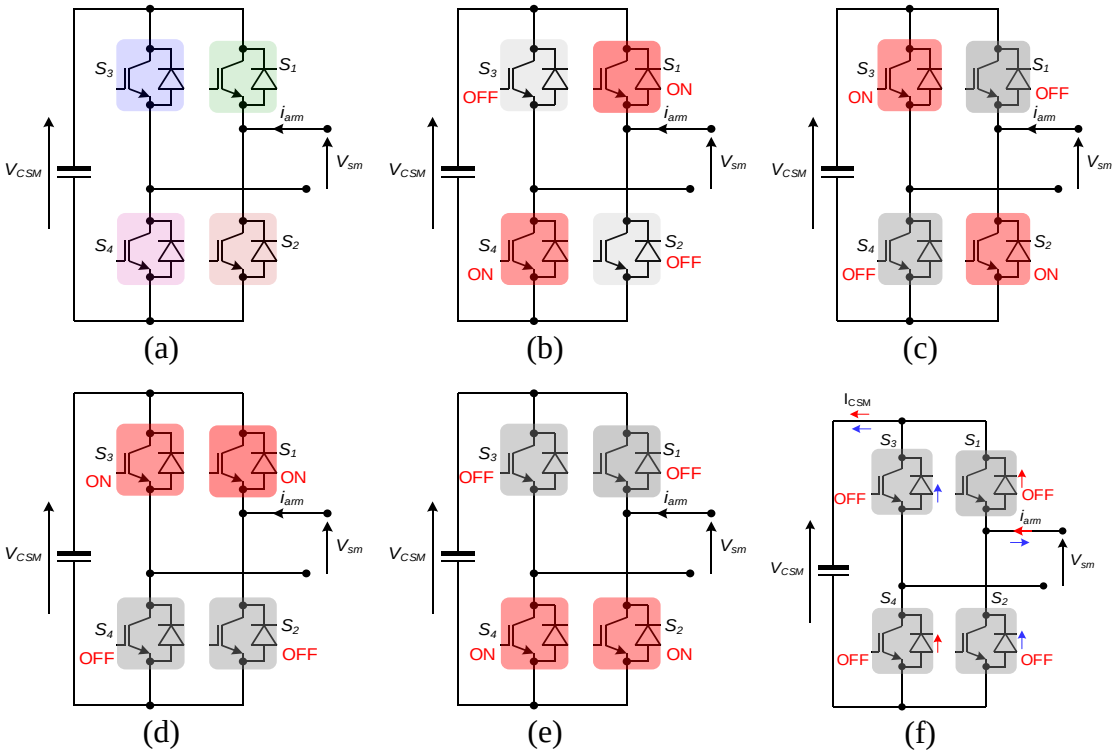


Fig. 4.3 (a) FB SM, and (b) to (f) depict its different switching states.

The total generic arm voltage is obtained by summing individual SM output voltage as:

$$V_{arm} = \sum_{i=1}^{N} v_{smi}(t) \tag{4.7}$$

Equations (4.6) and (4.7) are used to construct the FB-MMC switching function model shown in Fig. 4.4 (b) and (c). Similar to HB MMC, the realization of blocking state in FB-MMC model in Fig. 4.4 (c) is achieved by gating off all the IGBTs S_1, S_2, S_3 and S_4, and setting the upper and lower arm modulation functions $m_U = m_L = 1$. In contrast, during an operation state, the upper and lower arm voltages are realized as:

$$V_{armU} \approx V_{carmU}\left|m_U\right| \tag{4.8}$$

$$V_{armL} \approx V_{carmL}\left|m_L\right| \tag{4.9}$$

In addition, when sign(m_U)≥0 the switches S_1 and S_4 are turned on and S_2 and S_3 are turned off, and the opposite is true for sign(m_U)<0. The former scenario arises when FB-MMC arm synthesizes positive voltages, and the latter scenario occurs when the FB-MMC arm synthesizes negative voltages.

Since each arm of the hybrid MMC consists of FB and HB stacks, its switching function model is obtained simply by combining the HB-MMC and FB-MMC SFM into one which as shown in Fig. 4.5. Blocking and de-blocking states of the HB stacks can be realized as described in Section 3.1 and that of the FB stacks can be realized as described above.

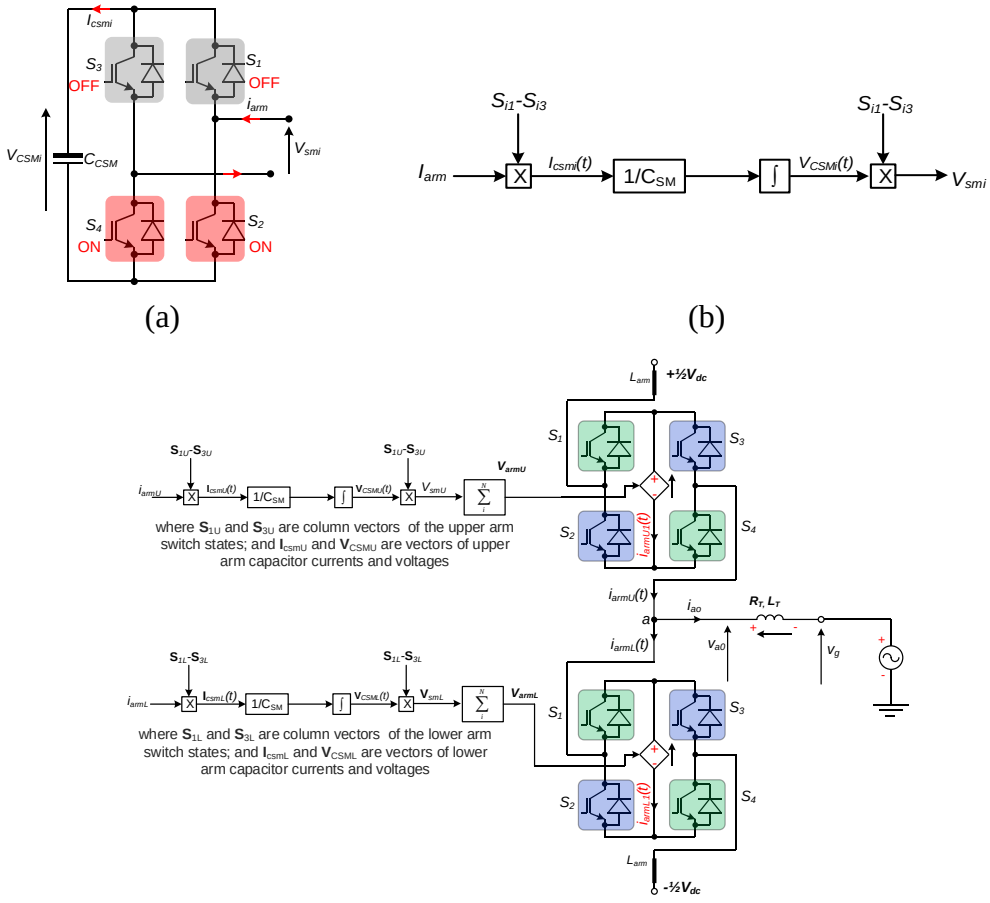


Fig. 4.4 (a) FB SM, (b) voltage calculation of one FB SM, and (c) Graphical depiction of SFM of FB-MMC

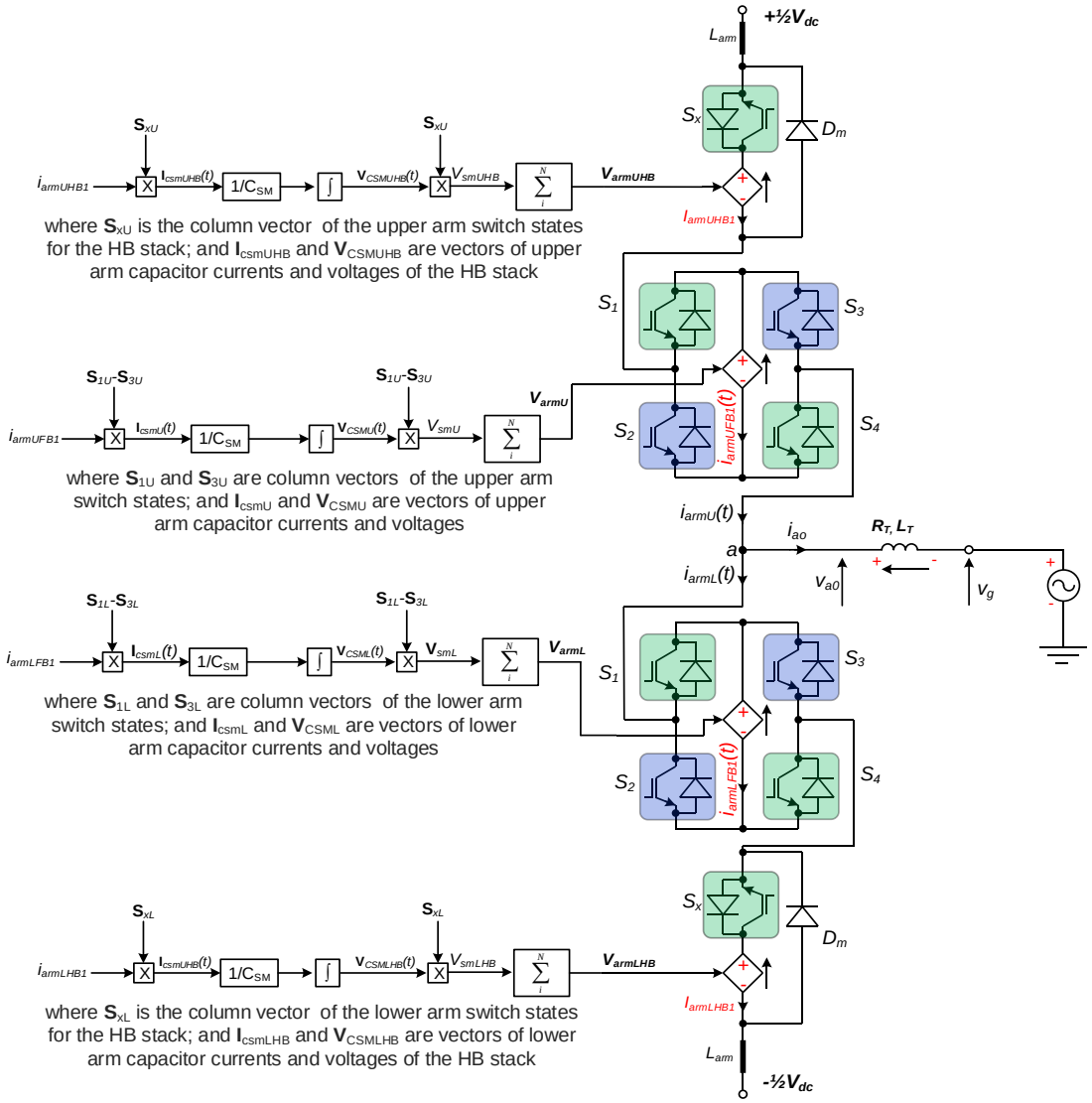


Fig. 4.5 Graphical depiction of SFM of the hybrid MMC

4.1.1.3 *Thevenin equivalent model*

In a similar way to Section 3.1.3, this section presents the Thevenin equivalent models for FB and hybrid MMCs, where the switching devices of the SMs are treated as two-state switched resistances, R_{ON} and R_{OFF} respectively, and each SM capacitance is replaced by its electromagnetic transient equivalent circuit.

For a generic SM shown in Fig. 4.6 (a), the SM capacitor dynamic can be expressed as:

$$\frac{dV_{CSMi}(t)}{dt} = \frac{I_{csmi}(t)}{C_{SM}} \tag{4.10}$$

After solving (4.10) using trapezoidal integration method, the following equations are obtained:

$$V_{CSMi}(t) = V_{CSMi}(t-\Delta t) + \tfrac{1}{2}\frac{\Delta t}{C_{SM}}\left[I_{csmi}(t) + I_{csmi}(t-\Delta t)\right] \tag{4.11}$$

$$V_{CSMi}(t) = V_{CSMi}(t-\Delta t) + R_{csm}I_{csmi}(t-\Delta t) + R_{csm}I_{csmi}(t) = V_h + R_{csm}I_{csmi}(t) \tag{4.12}$$

where $V_h = V_{CSMi}(t-\Delta t) + R_{csm}I_{csmi}(t-\Delta t)$, and $R_{csm} = \Delta t / 2C_{SM}$.

Fig. 4.6 (b) shows the equivalent circuit of the FB SM when Backward Euler and Trapezoidal integration methods are employed. This equivalent circuit can be further simplified using Thevenin theory, where the Thevenin voltage and resistance per SM are:

$$V_{th}(t) = \frac{R_{i2}R_{i3} - R_{i1}R_{i4}}{R_{ci}(R_{i1} + R_{i2} + R_{i3} + R_{i4}) + (R_{i1} + R_{i2})(R_{i3} + R_{i4})} \times V_h \tag{4.13}$$

$$R_{thi} = \frac{(R_{i1} + R_{ix})(R_{i2} + R_{iz})}{(R_{i1} + R_{ix} + R_{i2} + R_{iz})} + R_{iy} \tag{4.14}$$

where $R_{ix} = \dfrac{R_{i3}R_{csmi}}{R_{i3} + R_{i4} + R_{csmi}}$, $R_{iy} = \dfrac{R_{i3}R_{i4}}{R_{i3} + R_{i4} + R_{csmi}}$ and $R_{iz} = \dfrac{R_{i4}R_{csmi}}{R_{i3} + R_{i4} + R_{csmi}}$

The switched voltage to be developed across each arm can be calculated by:

$$V_{arm} = \sum_{i=1}^{N} V_{smi} \tag{4.15}$$

Fig. 4.6 (c) summarises per phase implementation of the Thevenin equivalent model of FB-MMC, where the SM capacitor dynamics and full converter behaviours during blocking and de-blocking are fully accounted for. Handling of blocking state during DC fault in the Thevenin equivalent FB-MMC model is similar to that of the SFM described earlier.

The Thevenin equivalent model of the hybrid MMC shown in Fig. 4.7 is obtained by combining the HB and FB MMC Thevenin equivalent models.

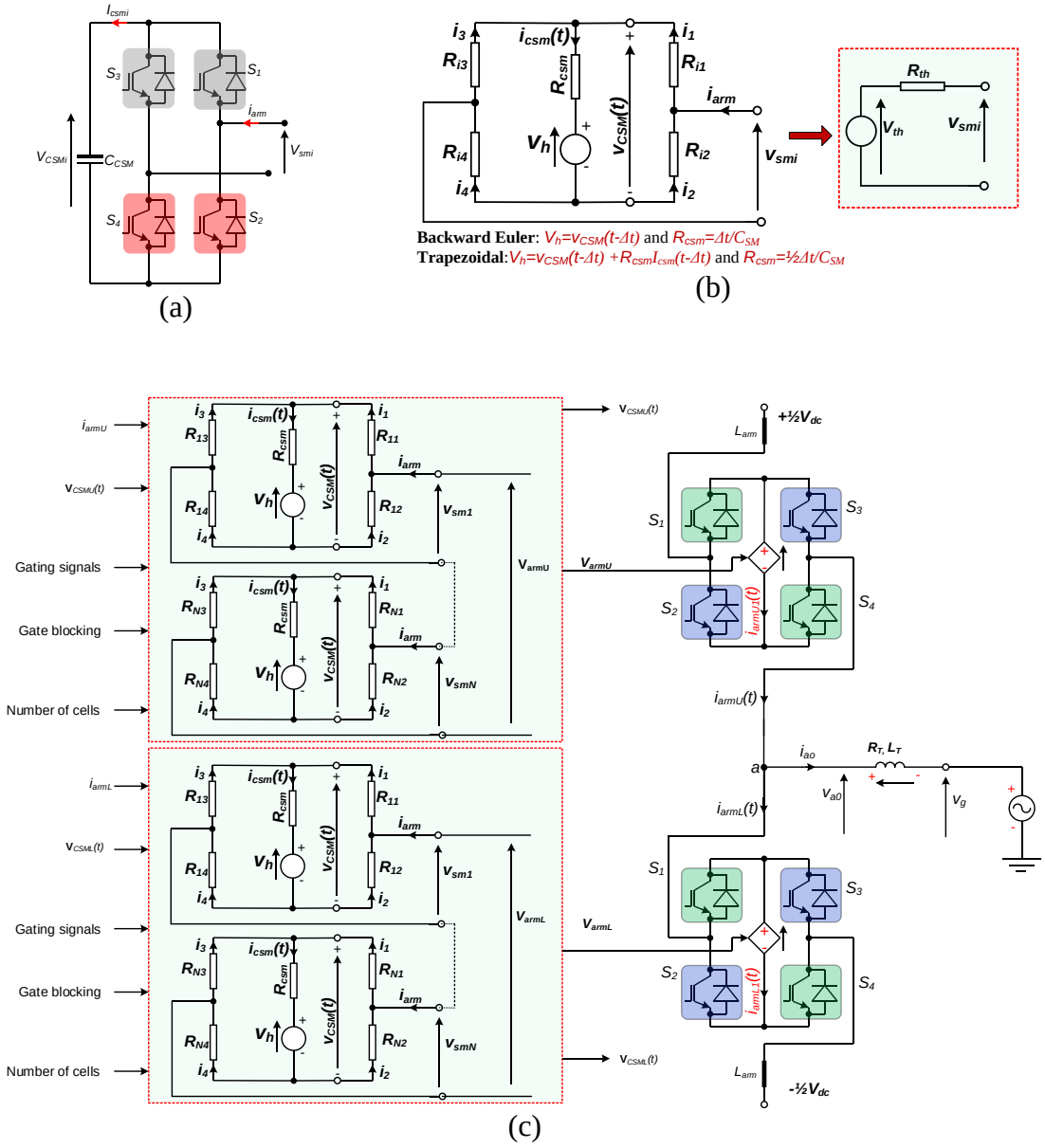


Fig. 4.6 Thevenin equivalent model of the FB-MMC

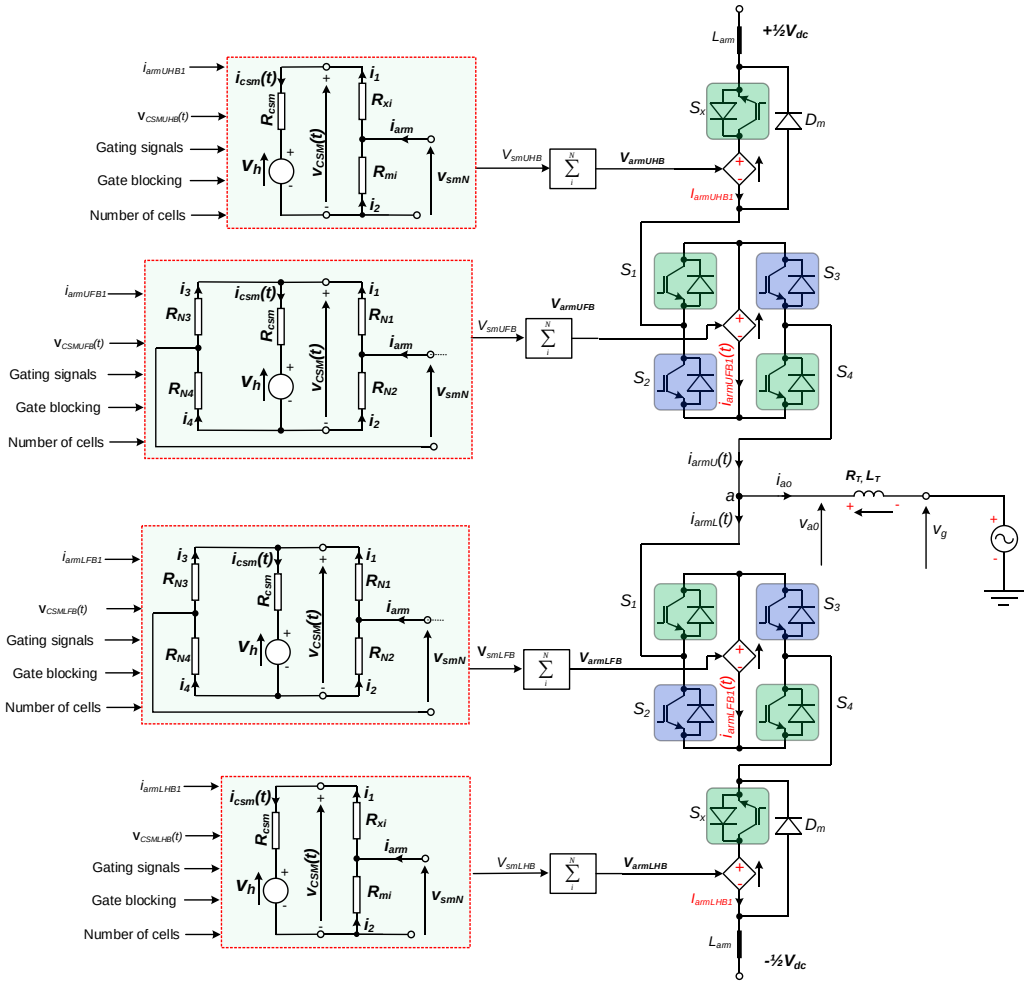


Fig. 4.7 Thevenin equivalent model of hybrid MMC

4.1.1.4 *Averaged model*

Since the HB, FB and hybrid MMCs adhere to the same operating principle during normal operation, the same assumptions made in the development of the HB-MMC averaged model also apply to the FB and hybrid MMCs. In other words, the systematic derivations of the averaged models of the FB and hybrid MMCs from the first principles are identical to that of the HB-MMC. The added features of the FB and hybrid MMCs are realizable by incorporating additional power electronics switches to mimic their physical behaviours during converter blocking and when their arms require to generate negative voltages. Fig. 4.8 depicts per arm averaged models of the FB MMCs [56][121][122][123], where the upper and lower arm voltages v_{armU} and v_{armL} and equivalent upper and lower arm capacitor currents i_{capU} and i_{capL} are approximated by:

$$v_{armU} \approx \tfrac{1}{2} V_{carmU} \left[\alpha - m\sin(\omega t + \delta)\right] \approx V_{carmU} m_U \tag{4.16}$$

$$v_{armL} \approx \tfrac{1}{2} V_{carmL} \left[\alpha + m\sin(\omega t + \delta)\right] \approx V_{carmL} m_L \tag{4.17}$$

$$i_{capU} \approx \tfrac{1}{2} i_{armU} \left[\alpha - m\sin(\omega t + \delta)\right] \approx i_{armU} m_U \tag{4.18}$$

$$i_{capL} \approx \tfrac{1}{2} i_{armL} \left[\alpha + m\sin(\omega t + \delta)\right] \approx i_{armL} m_L \tag{4.19}$$

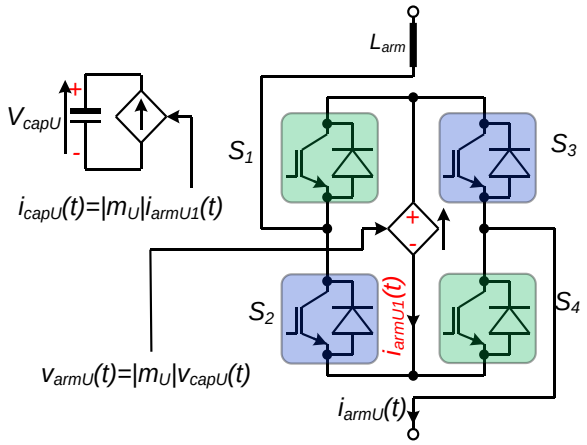


Fig. 4.8 Per arm averaged model of the FB and hybrid MMCs.

Similar to that in the FB-MMC SFM and Thevenin equivalent model, blocking state is realized by gating off all IGBTs S_1, S_2, S_3 and S_4, and setting the upper and lower arm modulation functions $m_U=m_L=1$. The upper and lower arm voltages during the de-block state are realized as:

$$V_{armU} \approx V_{carmU} \left|m_U\right| \tag{4.20}$$

$$V_{armL} \approx V_{carmL} \left|m_L\right| \tag{4.21}$$

In conjunction with (4.20) and (4.21), the auxiliary switches S_1 through S_4 are operated as follows:

a) When sign(m_U)≥0, the switches S_1 and S_4 must be turned on, and S_2 and S_3 must be turned off.
b) When sign(m_U)<0, the switches S_1 and S_4 must be turned off, and S_2 and S_3 must be turned on.

The scenario in (a) arises when the FB-MMC arm synthesizes positive voltages during normal operation with rated DC voltage, while the scenario in (b) occurs when the FB-

MMC arm synthesizes negative voltages as required during operation with extremely low DC voltage and operation with negative DC voltage.

It is worth to recall that the hybrid MMC facilitates normal and reduced DC link voltage operation and active control of DC fault current during pole-to-pole DC fault (zero DC voltage) by inserting the same number of SM capacitors with positive and negative polarities as that of the FB-MMC. Also, with the assumption that the HB and FB SMs of the hybrid MMC have same capacitances, insertion of the FB SM capacitors with positive polarities will exhibit the same behaviours at SM and arm levels as that of the HB SMs. This fact justifies the use of per arm averaged model depicted in Fig. 4.8 to represent the hybrid MMC, provided that the DC modulation control range is restricted as described above ($-\frac{1}{2} \leq \alpha \leq 1$), and the upper and lower arm modulation functions m_U and m_L are set to 0.5 during converter blocking.

4.2 Model validation

4.2.1 Implementation in RTDS

Fig. 4.9 shows a generic layout of the real-time models of the FB and hybrid MMC models implemented in RSCAD using dual time steps (multi-rate). Parts of the FB and hybrid MMC models that operate at high switching frequency are built in small time-step (i.e. 1.4-2.5µs), whilst the AC grid source and control system is modelled in a larger time step (i.e. 50 µs).

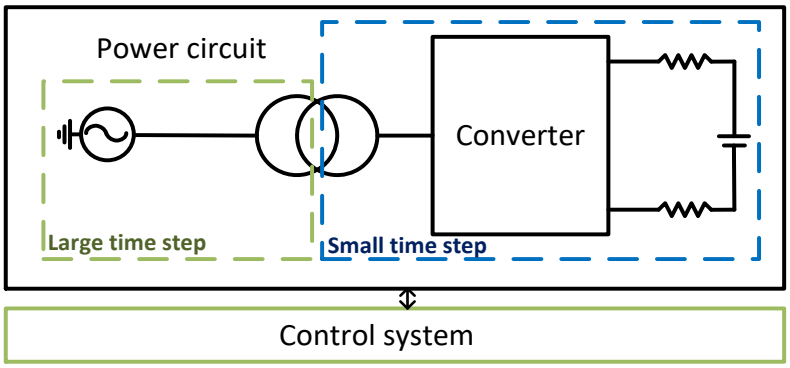


Fig. 4.9 A single terminal MMC system modelling method in RTDS

On the basis of detailed discussions of the FB and hybrid MMCs modelling presented in previous Sections 4.1, real-time user-defined 20-SM FB-MMC SFM and AM, and hybrid MMC AM are built in RSCAD-RTDS simulation platform. The developed models are validated against a number of offline models developed in PSCAD:

- FB-MMC: 20-SM SFM, Thevenin equivalent, and AM.
- Hybrid MMC: AM.

The number of SMs in the developed RSCAD-RTDS model can be easily scaled and modified if more details are required and sufficient RTDS modelling hardware capability is available.

In RTDS platform, the power circuit part of the FB and hybrid MMC models (SFM and AM) and their associated components such as the DC side circuit and interfacing transformer are modelled in the small-time step of 2.5μs. While the parts that calculate the SM capacitor dynamics and control systems are placed in a large time-step of 50μs. The user-defined components that implement the calculations of SM capacitor dynamics and voltage balancing are realised in MATLAB-SIMULINK and then converted to RSCAD using code generation. Same as for the HB-MMC described in Chapter3, the whole real-time simulation model of the test system is implemented on one RTDS rack, with a two-processor PB5 card and three GPC cards. One processor on the PB5 card is assigned for total network solution, whilst the other is assigned for the control system. Each converter requires one GPC processor to solve the power circuit that operates at the small time-step. Since the aim is to validate the MMC behaviours under a number of operating conditions, the DC side of the half-bridge MMC is modelled by a stiff DC voltage source connected to two 50km short DC cables each modelled by one pi-section. The AC side is placed at large time-step of 50μs, and the connection between the AC system at large time-step and the MMC power circuit and its DC side components at small time-step is realised through the VSC interface transformer.

4.2.2 **Test system**

This section uses one MMC converter terminal as shown in Section 3.2.1 to validate the real-time and offline FB and hybrid MMC models. The different models are:

- FB-MMC
  Offline: SFM, averaged model, and Thevenin equivalent model (TEM) provided by PSCAD.
  Real-time: SFM and averaged model
- Hybrid MMC
  Offline: averaged model
  Real-time: averaged model

A single terminal MMC-HVDC system is modelled in PSCAD and RTDS, with full sets of controllers described in Chapter 2, and detailed system parameters listed in Table 1. The SM capacitances of the FB and hybrid MMC models are the same as that for the HB-MMC. High impedance AC side grounding is adopted in the model.

As the previous study in Section 3.2 has shown that the numbers of SMs in the MMC arms have negligible impacts on MMC dynamic behaviours, this section presents the detailed validation of the real-time FB-MMC models (20-SM SFM and AM) and AM of hybrid against offline FB-MMC models (20-SM SFM, TEM and AM) and AM of the hybrid MMC respectively. The validation scenarios are listed below:

1) Full-bridge MMC validations
   - Normal operation
   - Three-phase symmetrical AC fault
   - Pole-to-pole DC short circuit fault with converter blocking
   - Pole-to-ground DC fault
   - DC voltage reversal
2) Hybrid MMC validations
   - Pole-to-pole DC short circuit fault with active control of fault current

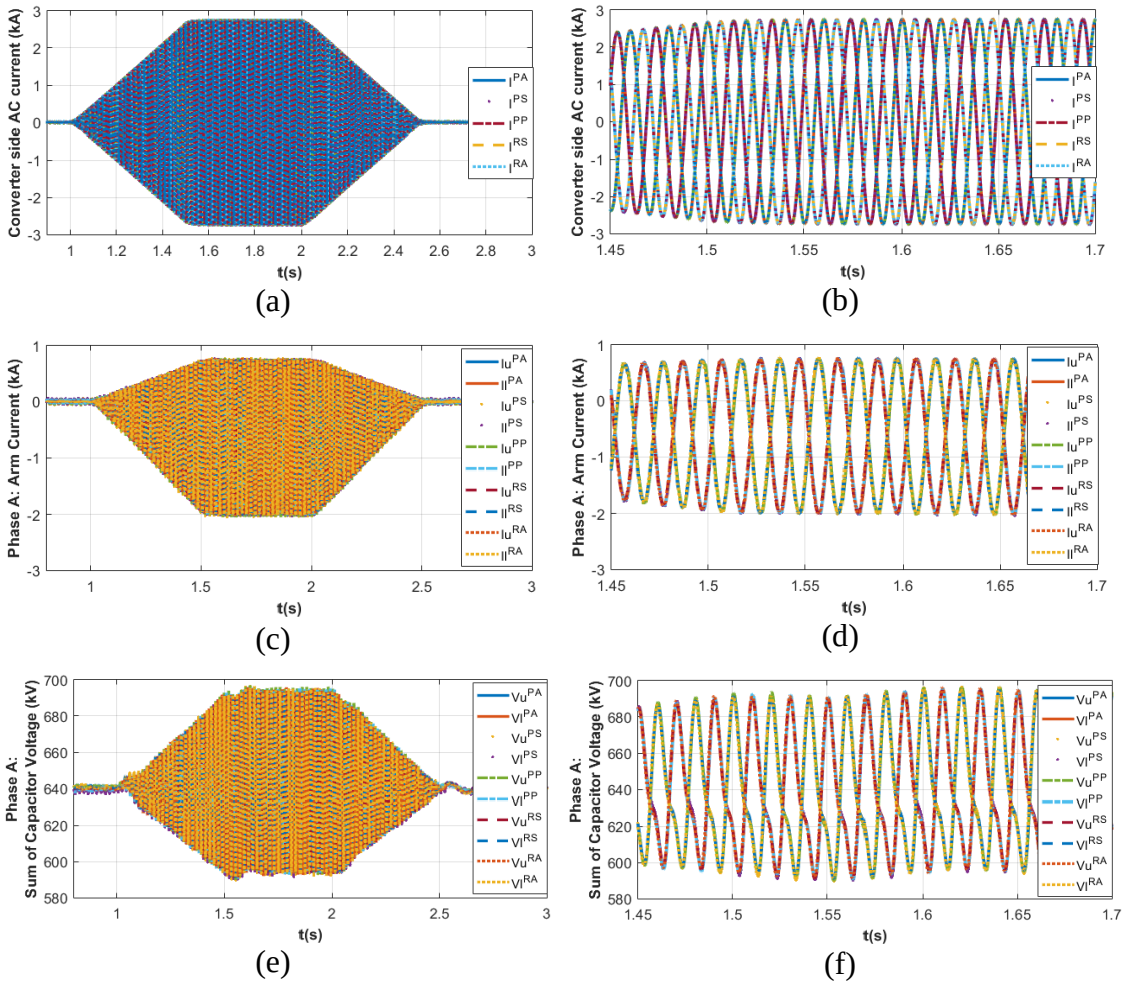
4.2.3 **Full bridge MMC model validation**

4.2.3.1 *Normal operation*

Fig. 4.10 summarises simulation waveforms of the offline and real-time user-defined FB-MMC when it operates as a power controlling converter using the control systems depicted in Fig. 2.11. The acronyms PA, PS and PP, and RS and RA displayed in the legends attached to simulation waveforms stand for offline PSCAD AM, SFM and TEM, and real-time SFM and AM respectively. During 0 to 1s, the FB-MMC controls both its

active and reactive power at zeros. At *t*=1s, active power is ramped from 0 to 1200MW at a rate of 2400MW/s, while reactive power is maintained at zero.

Fig. 4.10 (a)-(f) show the full-scale and zoomed offline and real-time simulation waveforms of the three-phase converter currents, and phase A upper and lower arm currents. These waveforms show the waveforms obtained from the offline and real-time simulation models are identical, while arm currents exhibit very small and diminishing differences during power ramps, with all arm current waveforms become identical as the system settles. The plots for the sums of the capacitor voltages displayed in Fig. 4.10 (e) and (f) show similar behaviour observed in the arm currents. The traces of the active powers, and DC link voltages and currents displayed in Fig. 4.10 (g)-(i) are almost identical, including during transition between two operating points.



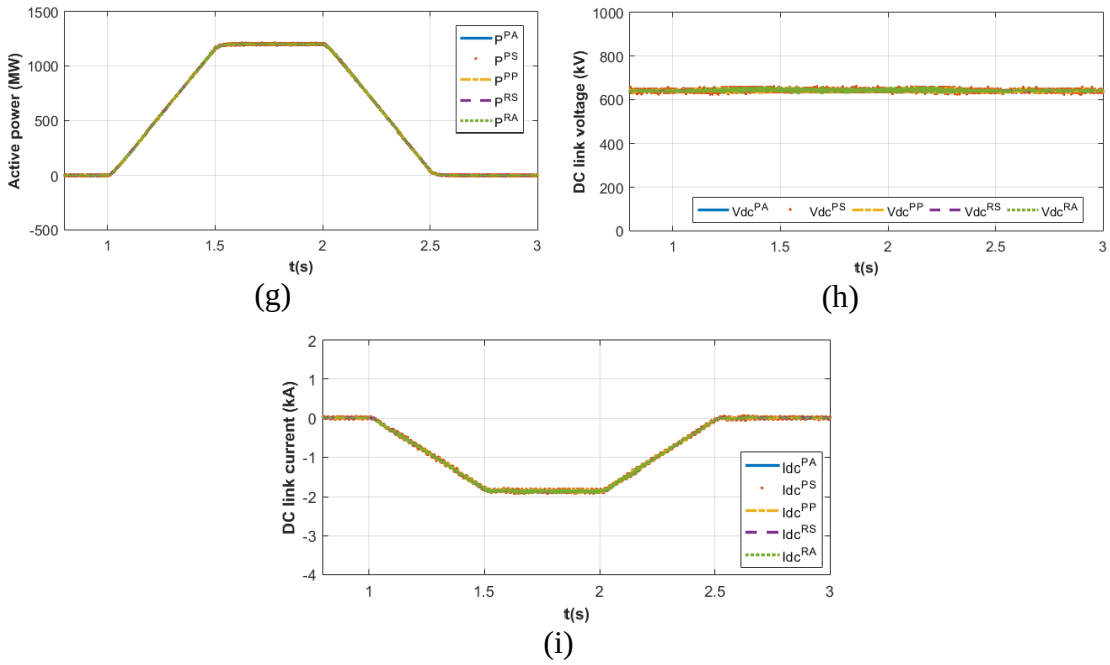


Fig. 4.10 Simulation waveforms with different FB-MMC models during normal operation: 20-SM SFM, TEM and AM)

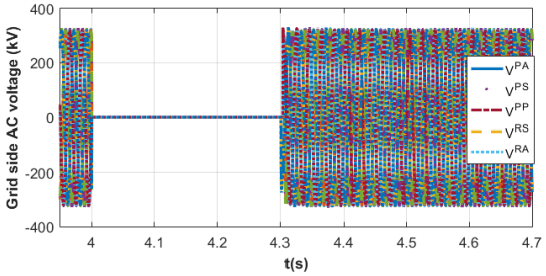
In summary, Fig. 4.10 shows all the offline and real-time simulation models being compared are capable of reproducing the dynamics of the FB-MMC as it varies its power set-points, with negligible errors.

4.2.3.2 *Three-phase-to-ground AC fault*

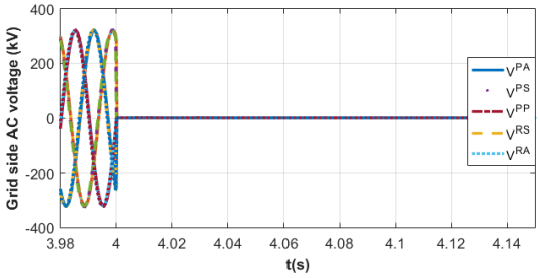
Fig. 4.11 displays simulation waveforms during a three-phase-to-ground AC fault (fault resistance equals 0.01Ω), with results of the real-time simulations (20-SM SFM and AM) superimposed on that of the PSCAD offline simulations (20-SM SFM, TEM and AM). In the pre-fault, during fault and post-fault conditions, active and reactive powers set-points are maintained at 1200 MW and 0 MVAr respectively. At *t*=4s, a temporary solid symmetrical three-phase-to-ground AC fault is applied at PCC1, with 300ms fault duration.

The AC voltage and converter current waveforms shown in Fig. 4.11 (a) and (b), and (c) and (d), prove that the different real-time and offline models having the same behaviours in terms of trend and magnitude during the three-phase AC fault. Likewise, the plots for the phase A upper and lower arm currents, and the sums of the upper and lower capacitor

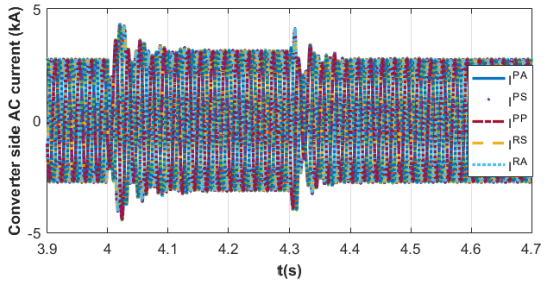
voltages in Fig. 4.11 (e)-(h) also show negligible errors. The same can be observed for the active power, DC link voltage and current during the three-phase-to-ground AC fault in Fig. 4.11 (i)-(k).



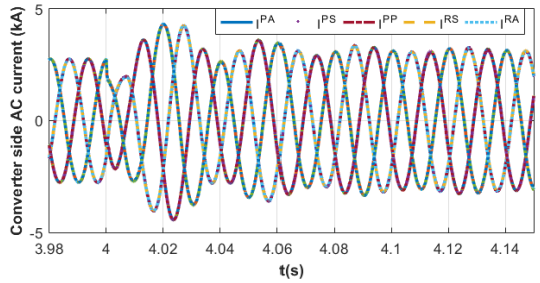
(a)



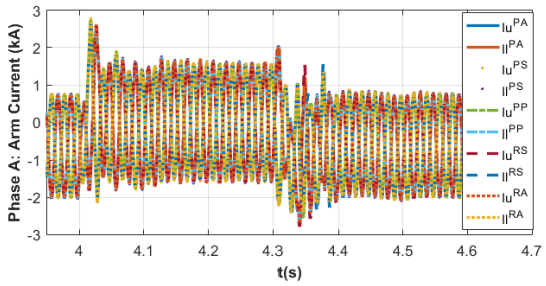
(b)



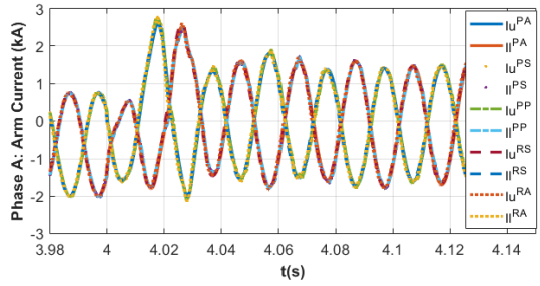
(c)



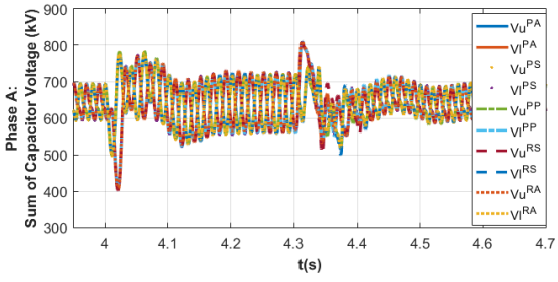
(d)



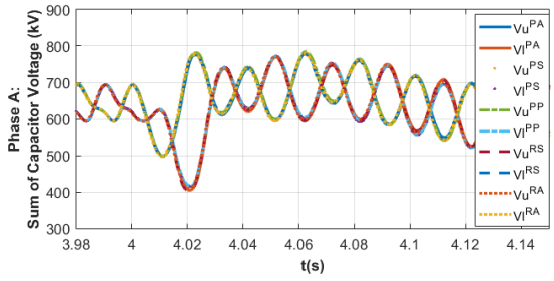
(e)



(f)



(g)



(h)

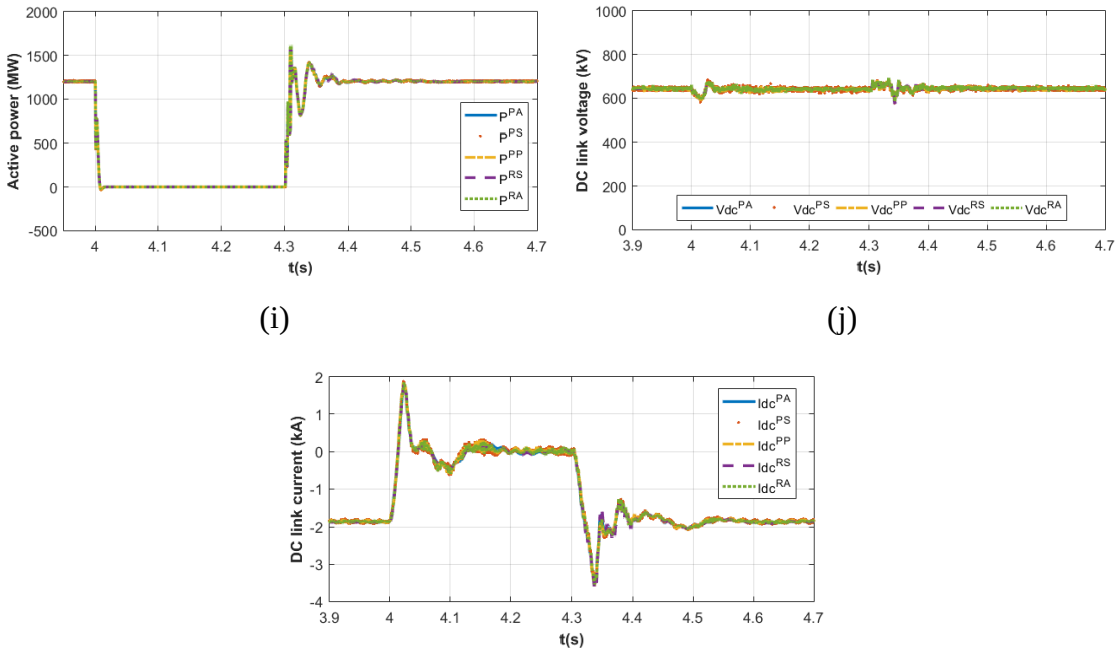


Fig. 4.11 Simulation waveforms with different FB-MMC models during a three-phase-to-ground AC fault

4.2.3.3 *Pole-to-pole DC short circuit fault with converter blocking*

Fig. 4.12 presents simulation waveforms when a solid pole-to-pole DC short circuit fault (short circuit resistance equals to 0.005 Ω) is applied at FB-MMC DC terminals at *t*=5s, as shown in Fig. 3.5, and the converter is blocked 50μs after fault inception.

Fig. 4.12 (a), (b) and (c) show simulation waveforms for the three-phase PCC voltages converter AC currents. These traces show that all the AC side waveforms (currents and voltages) of the real-time and offline simulations are identical. Similarly, the real-time and offline upper and lower arm currents, and the sums of the upper and lower arm SM capacitor voltages of phase A displayed in Fig. 4.12 (d) and (e) do not exhibit any visible errors in steady state and during the DC fault, and the same can be observed for the active powers, and DC link currents and voltages as shown in Fig. 4.12 (f), (g) and (h).

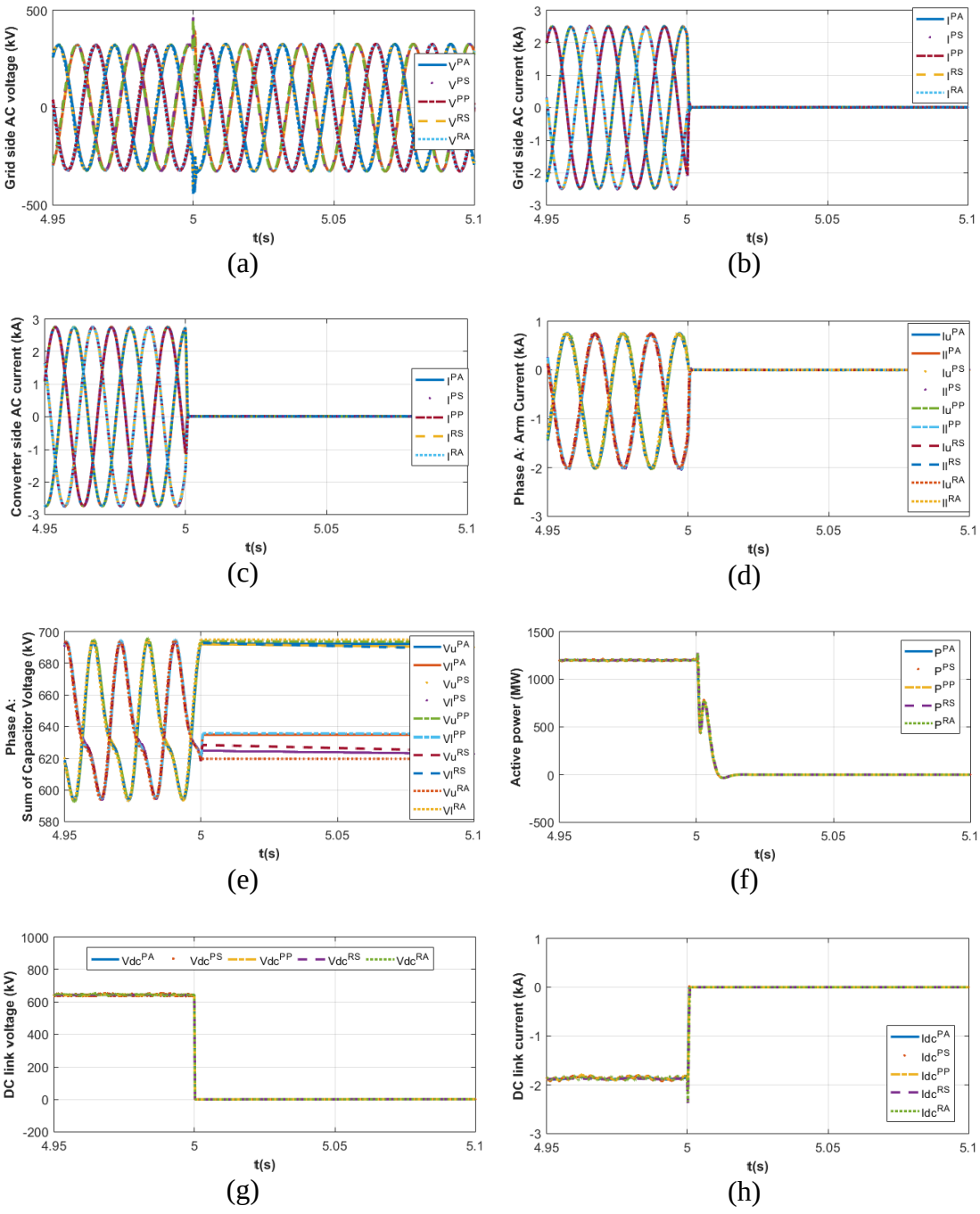


Fig. 4.12 Simulation waveforms with different offline and real-time FB-MMC models (SFM, TEM and AM) during DC short circuit fault when converter blocking activated 50μs after fault inception

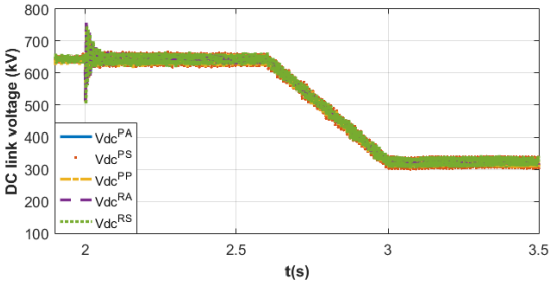
4.2.3.4 *Pole-to-ground DC fault*

Fig. 4.13 shows simulation waveforms when a pole-to-ground DC fault (fault resistance equals to 0.005 Ω) occurs at t=2s, and the DC voltage is controlled to be half of the rated value 0.6s after the fault inception in order to reduce the DC voltage stress on the healthy pole.

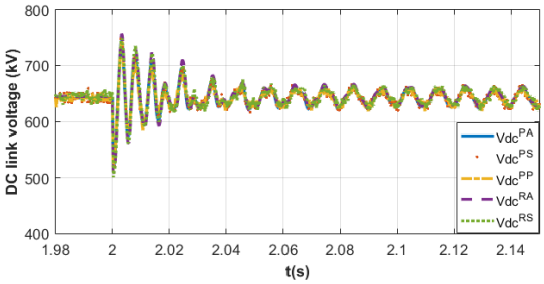
Fig. 4.13 (a)-(d) show offline and real-time simulation waveforms for the pole-to-pole and pole-to-ground DC voltages and DC link currents. The plots for DC voltages and current exhibit brief disturbances which are associated with the discharge of the faulted pole and charging of the healthy pole, and with both simulation platforms and different models show almost identical behaviours. Observed that halving of the pole-to-pole DC link voltage 0.6s from fault inception reduces the voltage stress on the healthy pole to the rated design value of 320kV. The post-fault DC current remains the same as the pre-fault value and system now transmits half of the rated power as seen in Fig. 4.13 (k).

The three-phase converter side voltages shown in Fig. 4.13 (e) and (f) indicate that the pole shift during pole-to-ground DC fault affects the converter side voltage leading to 320kV DC offshore. However, this has no impact on the converter currents as seen in Fig. 4.13 (g) and (h). The reduction of the DC link voltage also helps to reduce the DC voltage stress being exposed to insulations of the low-voltage windings of the transformer and converter side equipment. All the behaviours described above are reproduced accurately in the results of the offline and real-time simulations.

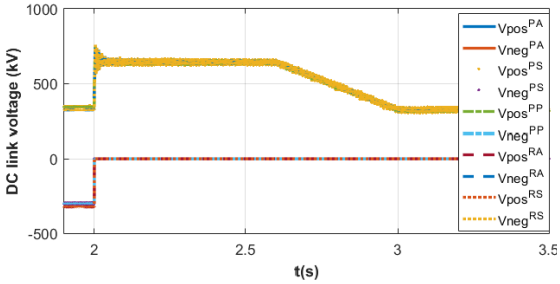
Fig. 4.13 (i) and (j) show that the arm currents of the FB-MMC remain well-controlled during pole-to-ground DC fault when pole restraining (halving of the DC voltage) is enabled, with all the offline and real-time use defined models are able to reproduce almost identical results.


DC link voltage (kV)
t(s)
Vdc^PA
Vdc^PS
Vdc^PP
Vdc^RA
Vdc^RS

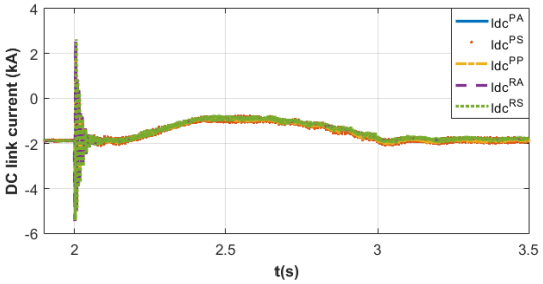
(a)


DC link voltage (kV)
t(s)
Vdc^PA
Vdc^PS
Vdc^PP
Vdc^RA
Vdc^RS

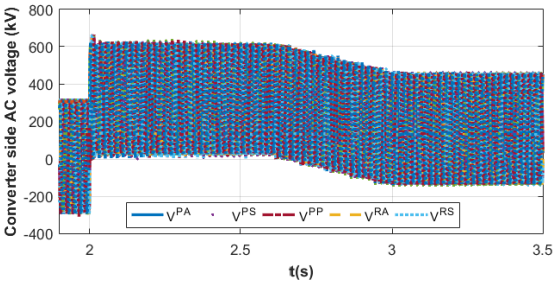
(b)


DC link voltage (kV)
t(s)
Vpos^PA
Vneg^PA
Vpos^PS
Vneg^PS
Vpos^PP
Vneg^PP
Vpos^RA
Vneg^RA
Vpos^RS
Vneg^RS

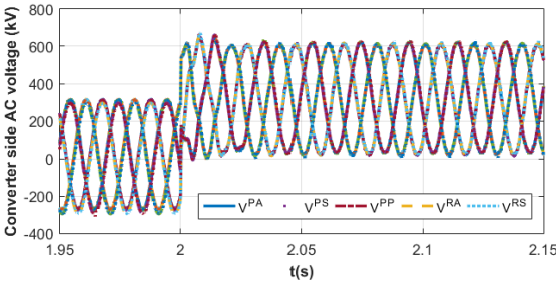
(c)


DC link current (kA)
t(s)
Idc^PA
Idc^PS
Idc^PP
Idc^RA
Idc^RS

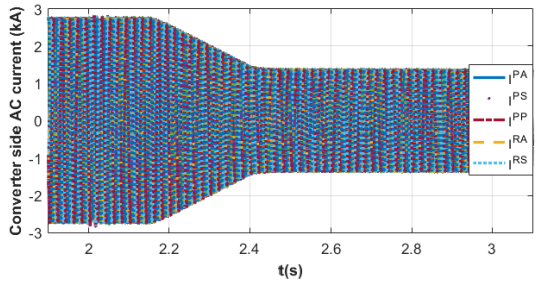
(d)


Converter side AC voltage (kV)
t(s)
V^PA
V^PS
V^PP
V^RA
V^RS

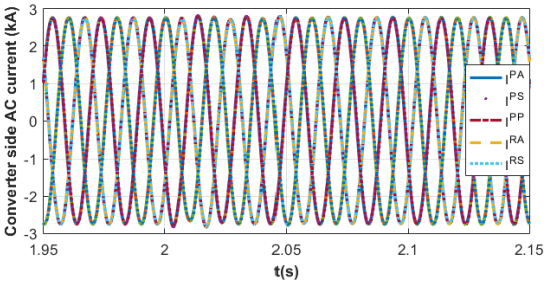
(e)


Converter side AC voltage (kV)
t(s)
V^PA
V^PS
V^PP
V^RA
V^RS

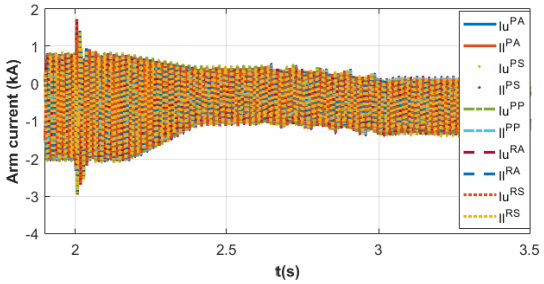
(f)


Converter side AC current (kA)
t(s)
I^PA
I^PS
I^PP
I^RA
I^RS

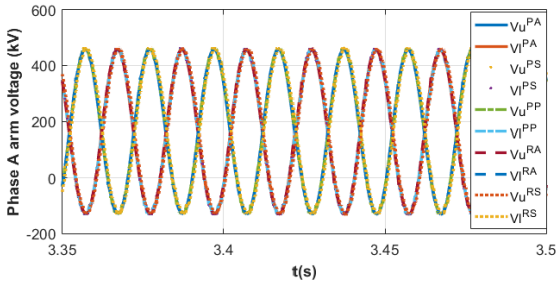
(g)


Converter side AC current (kA)
t(s)
I^PA
I^PS
I^PP
I^RA
I^RS

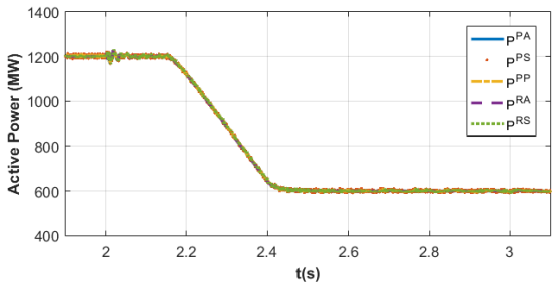
(h)


Arm current (kA)
t(s)
Iu^PA
Il^PA
Iu^PS
Il^PS
Iu^PP
Il^PP
Iu^RA
Il^RA
Iu^RS
Il^RS

(i)


Phase A arm voltage (kV)
t(s)
Vu^PA
Vl^PA
Vu^PS
Vl^PS
Vu^PP
Vl^PP
Vu^RA
Vl^RA
Vu^RS
Vl^RS

(j)



(k)

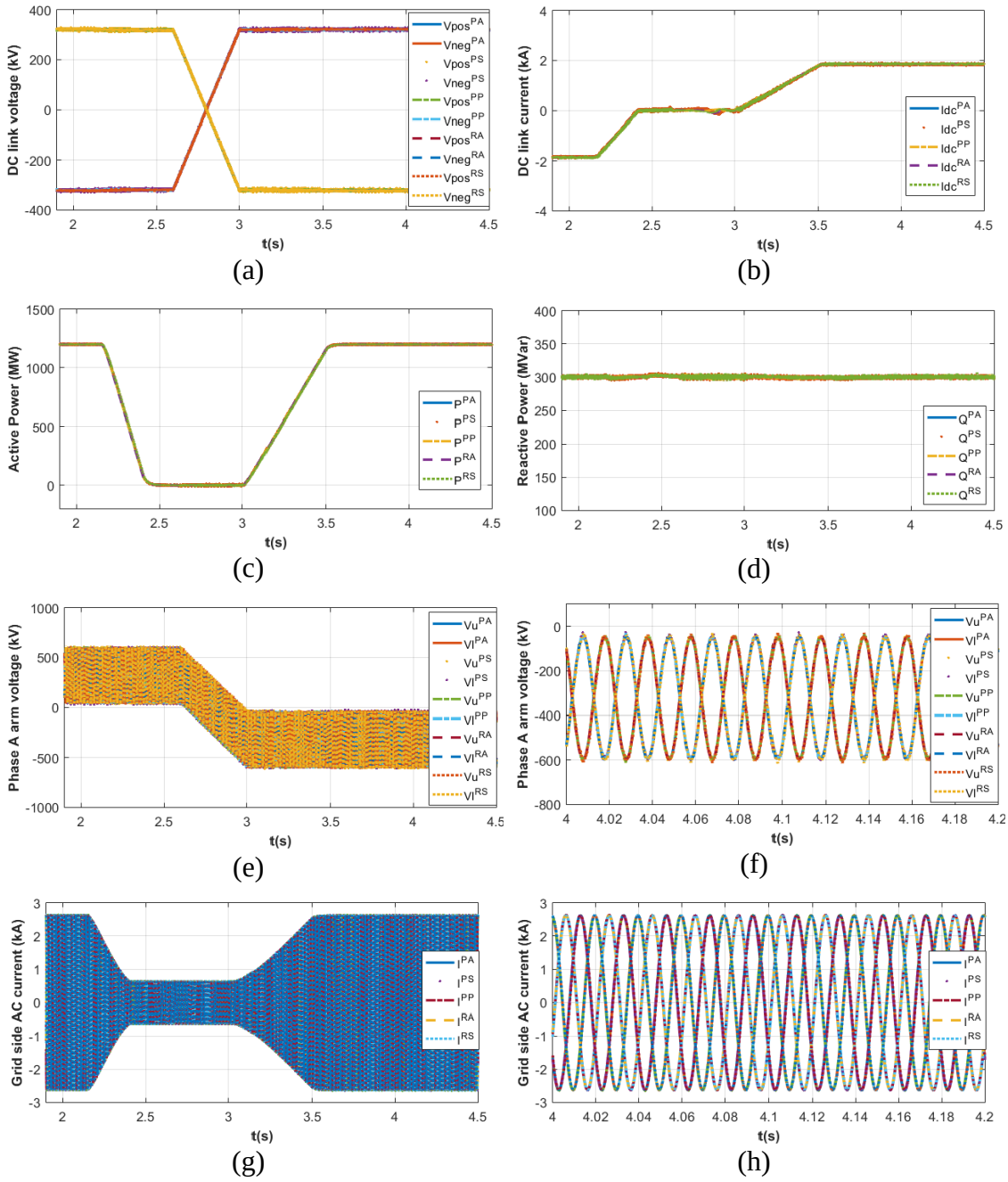
Fig. 4.13 Simulation waveforms with different offline and real-time FB-MMC models during pole-to-ground DC fault when a pole restraining is enabled 0.6s after fault inception

4.2.3.5 *DC voltage reversal*

Fig. 4.14 presents offline and real-time simulation waveforms when the FB-MMC initiates its DC voltage reversal at t=2.6s, from 640kV to -640kV, within 0.4s. Prior to the DC voltage reversal, at t=2.15s, the FB-MMC reduces its active power exchange with the AC grid from 1200MW to 0 within 0.25s. At t=3s, the FB-MMC starts the restoration of its active power exchange with the AC grid from 0 to 1200MW within 0.5s (during this period the FB-MMC operates with rated DC voltage of -640kV). During the entire operating period, the FB-MMC maintains its reactive power exchange with the AC grid constant at 300MVAr.

Fig. 4.14 (a) and (b), (c) and (d) show the simulation waveforms for the positive and negative pole DC voltages, DC current, and active and reactive powers the FB-MMC injects into PCC1. These waveforms show that different offline and real-time models of the FB-MMC produce the same responses. The results confirm the ability of these models to reproduce the bipolar operation of FB-MMC and uninterruptable STATCOM functionality, independent of the DC link voltage. Similarly, the plots for the upper and lower arm voltages shown in Fig. 4.14 (e) and their zoomed version when the FB-MMC operates with -640kV displayed in Fig. 4.14 (f) show identical results, with the DC modulation index $\alpha = -1$ (equivalent to -½V_{DC}) as anticipated. Same can also be observed for the currents the FB-MMC injects into AC grid and the upper and lower arm currents displayed in Fig. 4.14 (g) and (h), and (i) and (j). The sums of the upper and lower SM capacitor voltages of different offline and real-time models of the FB-MMC being

compared in Fig. 4.14 (k) and (m) also indicate a good match for the results produced by the models during steady-state and transients.



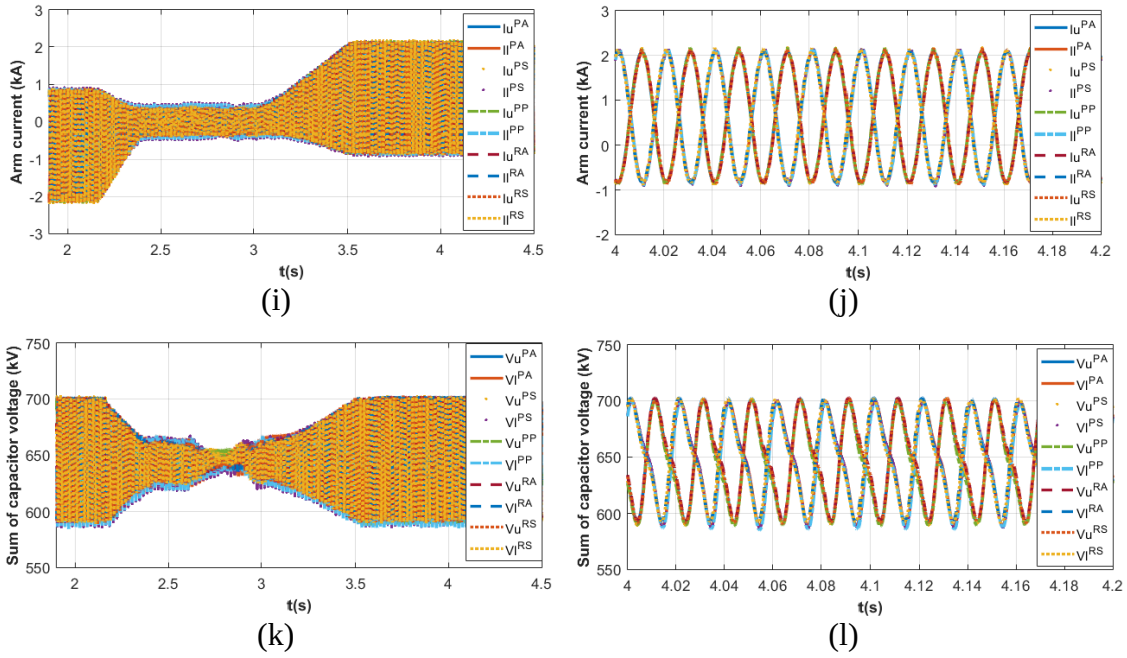


Fig. 4.14 Simulation waveforms that compare the transient behaviours of the user-defined offline and real-time FB-MMC models (SFM, TEM and AM) during DC voltage reversal

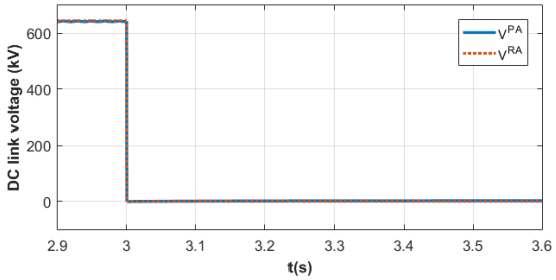
4.2.4 **Hybrid MMC model validation**

The operation of the hybrid MMC is similar to that of the FB-MMC, and thus, only selected results during a solid pole-to-pole DC short circuit fault with active fault current control is presented here. Test system is the same with the system shown in Section 3.2.1.

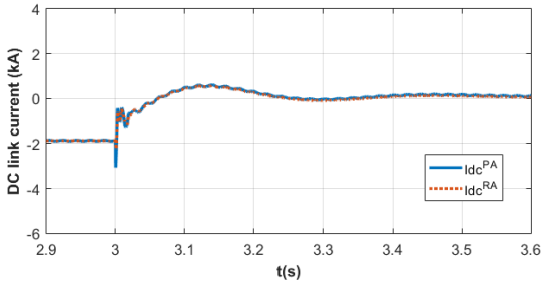
Fig. 4.15 presents simulation waveforms when a solid pole-to-pole DC short circuit fault is applied at the DC terminals of the hybrid MMC at *t*=3s, and fault control is enabled 50μs after fault inception. Fig. 4.15 (a) and (b) show pole-to-pole DC link voltage and DC current in the positive pole. These waveforms show the offline and real-time simulation models produce identical results during the DC short circuit fault, with the hybrid MMC is able to control the DC fault at zero. Fig. 4.15 (c) and (d) and (h) and (i) show the upper and lower arm currents, and three-phase currents the hybrid MMC injects into PCC1 at grid side. These waveforms show while the hybrid MMC controls DC fault current at zero during the DC fault, it retains full control over the reactive exchange with the AC grid, see Fig. 4.15 (k). The AC currents observed in the arms and output circuits of the hybrid MMC are associated with the reactive power being exchanged with the AC

grid, operating as a STATCOM. Fig. 4.15 (f) and (g) display the sums of the SM capacitor voltages of the hybrid MMC, and these plots indicate that the hybrid MMC retains full control over its SM capacitors. Fig. 4.15 (j) shows the active power that the hybrid MMC exchanges with the AC grid, which drops to zero during DC fault as expected. The results shown in Fig. 4.15 confirm that the hybrid MMC is able to control fault current during pole-to-pole DC short circuit fault.

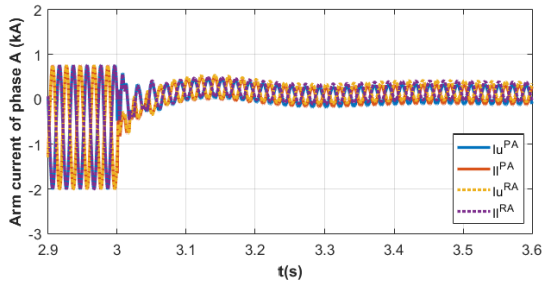
In summary, simulation waveforms presented in Fig. 4.15 confirm the validity of both offline and real-time user-defined AMs of the hybrid MMC to perform detailed studies of DC short circuit fault when fault current control is enabled.



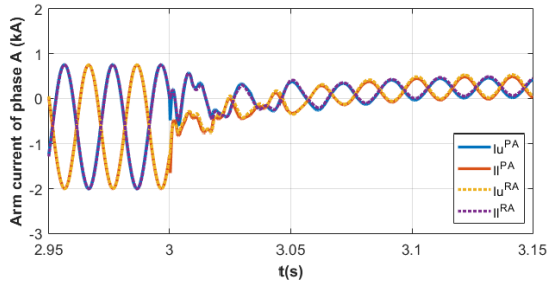
(a)



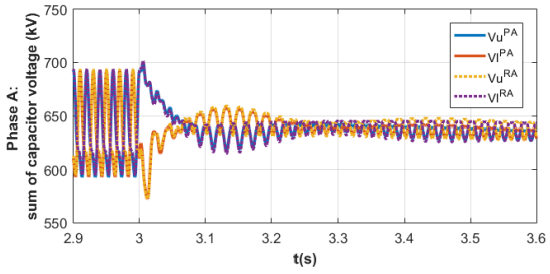
(b)



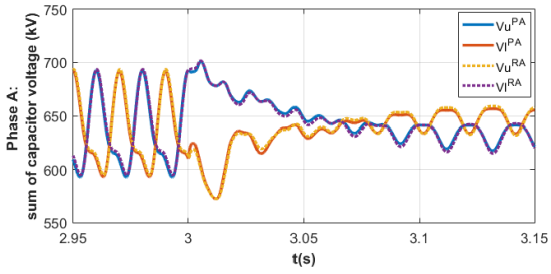
(c)



(d)



(f)



(g)

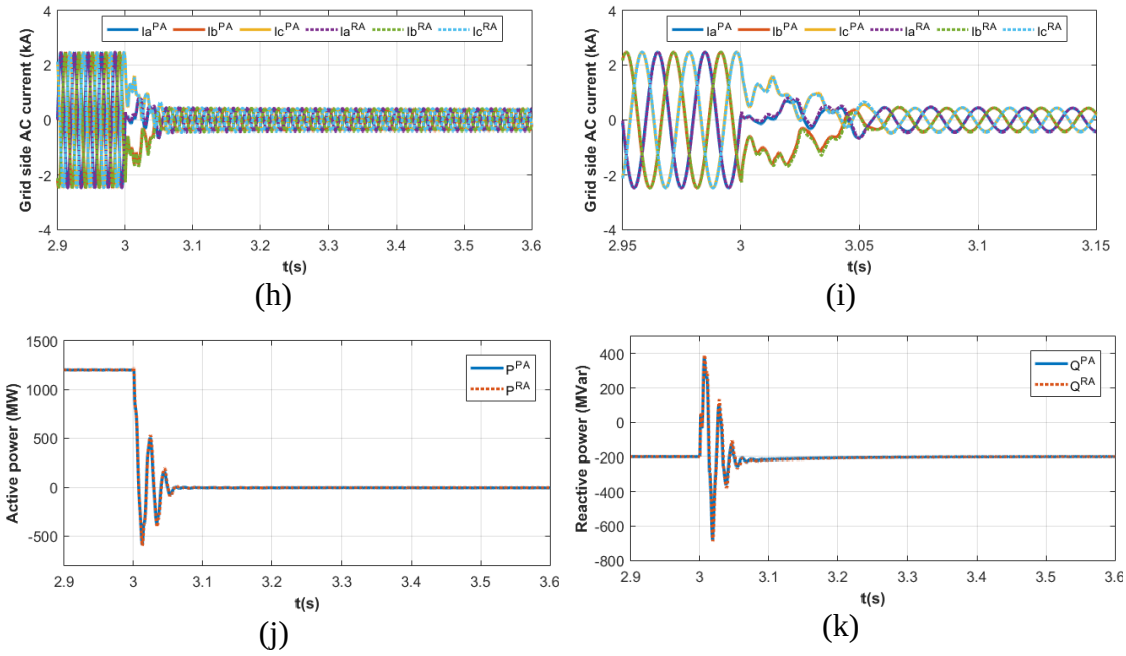


Fig. 4.15 Simulation waveforms with offline and real-time hybrid MMC AM models during DC short circuit fault when a DC fault current control is enabled

4.3 DC grid containing different MMC topologies

4.3.1 DC grid model development

Fig. 4.16 shows an example test system being used to assess the interoperability of HB, FB and hybrid MMCs in a generic DC grid. Converters T1, T2 and T3 are hybrid MMC, FB-MMC, and HB-MMC, respectively. All converters are represented in PSCAD and RTDS-RSCAD by their averaged models described in Section 4.1.1 and shown in Fig. 4.8. The control system depicted in Fig. 2.11 is incorporated into each converter station. Simulation parameters of the test systems are shown in Fig. 4.16.

The DC grid shown in Fig. 4.16 is implemented in RTDS using the concept of multi-rate, with two distinct sampling times as previously used. The power circuits of the three converters and DC cables are placed in 3 processors on GPC cards that operate at 2.5µs time step, whilst the three AC grids, control systems and part of the averaged model that calculates the capacitor voltage dynamics operate at 50µs time step placed in 2 processors on GPC card. The AC sides of the three converter models that operate at 2.5µs (small) time-steps are interfaced to the AC grids that operate at 50µs (large) time-step via three

interfacing transformers as previously described. The DC side of the converter model and associated DC cable operated at small time-step but in different processors are linked together through very short T-lines to form a DC grid.

It is worth emphasizing that the uses of T-lines for connecting converter models and DC cables that operate on different processors and the interfacing transformers for connecting system components that operate with different sample times have a negligible impact on the accuracy of the real-time simulation, which will be demonstrated later.

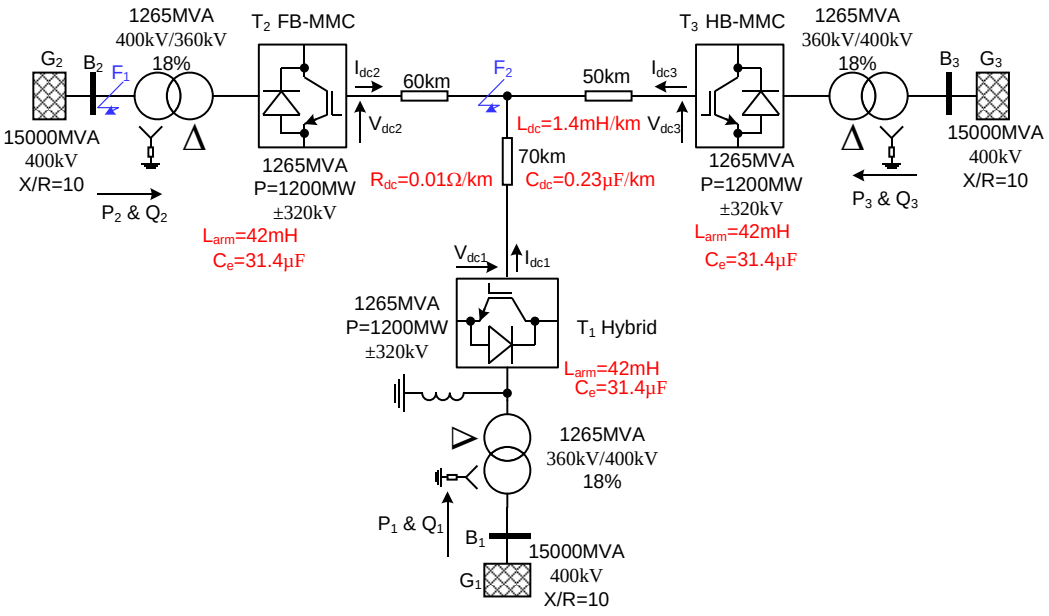


Fig. 4.16 Illustrative DC grid with multiple converter topologies

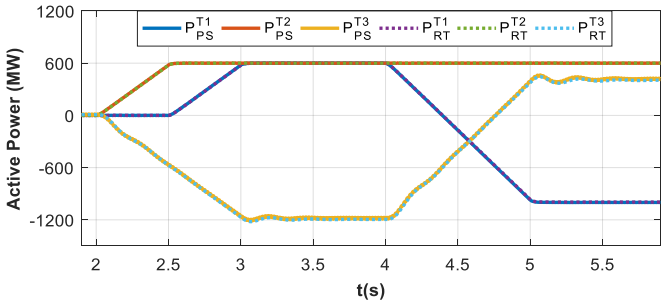
4.3.2 **Normal operation**

Fig. 4.17 displays RSCAD simulation waveforms superimposed on their PSCAD equivalents, where PS and RT subscripts stand for PSCAD and RTDS simulations respectively. In the simulations of the DC grid in Fig. 4.16, converter T_3 controls the DC grid voltage at 640kV, whilst T_1 and T_2 are operated as follows:

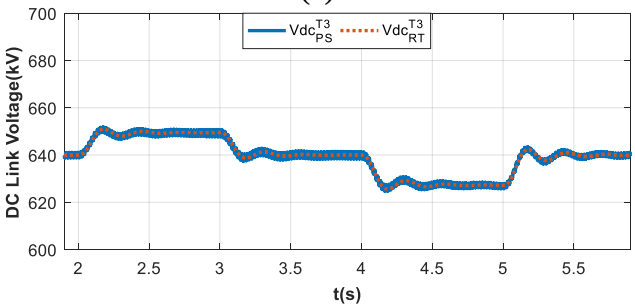
- At t=2s, T_2 ramps its active power from 0 to 600MW at a rate of 1200MW/s;
- At t=2.5s, T_1 ramps its active power output from 0 to 600MW at the same rate whereas within t=4-5s it reverses power from 600MW to -1000MW.

Throughout the simulation, converters T_1, T_2 and T_3 maintain their reactive power outputs at zero.

The active power and DC voltage in Fig. 4.17 (a) and (b) show that the DC voltage controlling converter T_3 (HB-MMC) regulates its DC link voltage tightly around 640kV and adjust its active power exchange with the AC grid G_3 as the power controlling converters T_1 (hybrid MMC) and T_2 (FB-MMC) vary their active power set-points. These expected behaviours are replicated accurately by both the offline PSCAD and real-time RTDS simulation waveforms, see Fig. 4.17 (a) and (b).



(a)



(b)

Fig. 4.17 Simulation waveforms during normal operation variation with the PSCAD and RSCAD models: (a) active powers of the T1, T2 and T3, (b) DC voltage of the converter terminal T3.

4.3.3 **Response during pole-to-pole DC short circuit fault**

This section presents DC fault simulation waveforms when a permanent pole-to-pole DC short circuit (fault resistance equals to 0.005 Ω) is applied at the main DC fault node (F_2) at t=4s whilst both converters T_1 and T_2 control their active powers at 600MW prior to the fault. All converters are blocked 50μs after fault inception. Fig. 4.18 (a) and (b) show the pole-to-pole DC voltage at F_2 and DC link currents of the three converters, with the DC link currents of the T_1 (hybrid MMC) and T_2 (FB-MMC) drop to zero after the activation of the converters blocking, while converter T_3 (HB-MMC) continues to feed current into the DC fault through its AC supply. The plots in Fig. 4.18 (c) show the active

powers of converters T_1 and T_2 drop to zero immediately after blocking, while T_3 continues to draw reduced active power from AC grid G_3 due to the high fault current. Similar behaviour can be observed from the DC current as Fig. 4.18 (d), (e) and (f) show the arm currents of T_1 and T_2 drop to zero, and that of the T_3 reverses direction and is fed from the AC side.

The DC voltages and currents, active powers and arm currents shown in Fig. 4.18 (a) through (f) are well matched between the offline and real-time simulation waveforms in terms of different dynamics and magnitudes during transients associated with the DC faults.

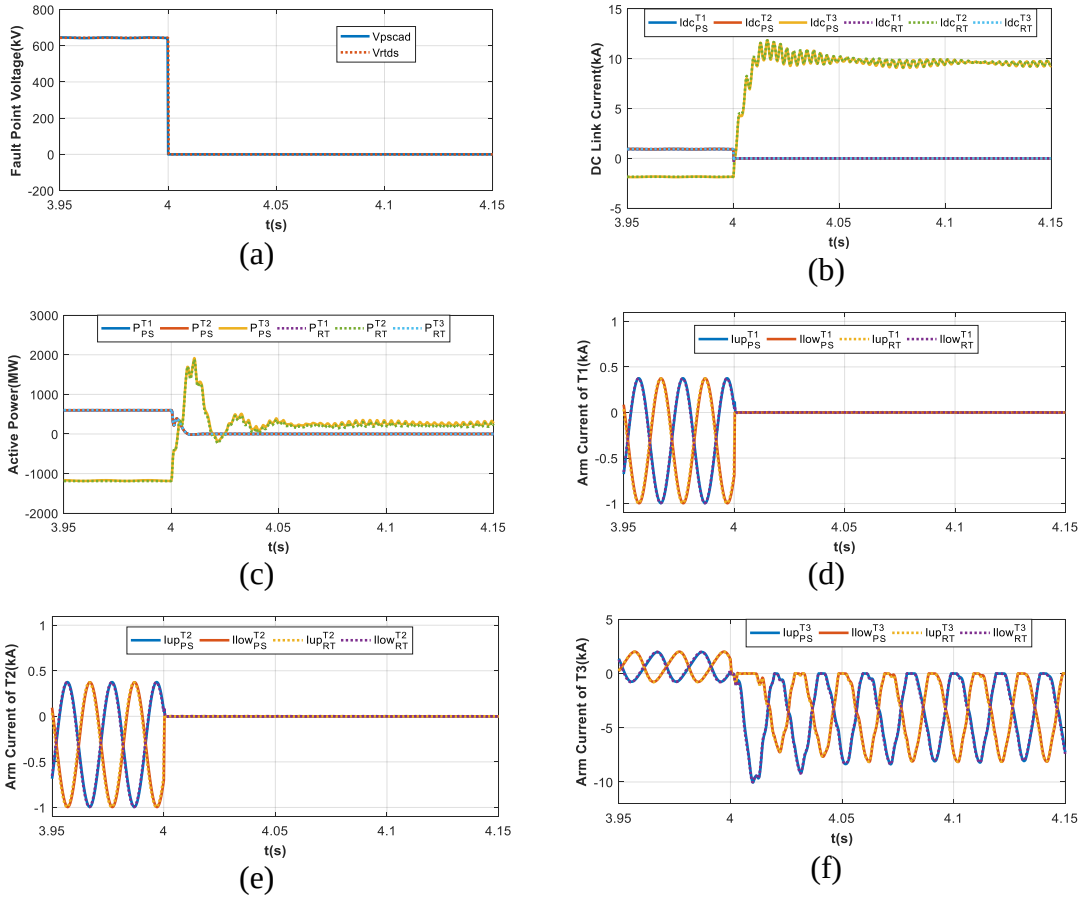


Fig. 4.18 Simulation waveforms during a pole-to-pole DC fault: (a) Pole-to-pole DC fault measured at the fault point, (b) DC-link current measured at DC terminals of converters T_1, T_2 and T_3, (c) Active powers of the converter terminals T_1, T_2 and T_3, and (d), (e) and (f) samples of the upper and lower arm currents of the converter terminals T_1, T_2 and T_3.

4.4 Summary

The modelling methods for full-bridge and hybrid MMCs are presented in this chapter. Switching function model and averaged model of full-bridge and hybrid MMCs are developed and implemented in RTDS as user-defined real-time models. These models are validated against offline PSCAD FB and hybrid MMC models. Results of comprehensive comparisons of the simulation waveforms show that the offline and real-time simulation waveforms are in full agreement during normal operation and various AC and DC faults conditions. It has shown that the FB and hybrid MMCs can provide full control of DC and AC current during DC faults conditions. The developed models can be used for a variety of system studies with high computational efficiency and accuracy examining the enhanced control and operation provided by FB and hybrid MMCs. Based on the user-defined real-time FB and hybrid MMC models developed and validated in this chapter and HB model validated in Chapter 3, a summary of detailed quantitative study that assesses the interoperability of different converter topologies that operate side-by-side in a multi-terminal DC grid has been presented. Detailed examinations of the presented results, with the simulation waveforms of the real-time models superimposed on that of the offline PSCAD, reveal that both models being compared produce practically identical results during normal and abnormal conditions. It can be concluded that the offline and real-time simulation models employed in this chapter are well-suited for a wide range of DC grid studies such as normal operation, and AC and DC faults.

Chapter 5 Extraction of small-signal impedance for stability assessment

The large-scale adoption of power electronic converters paves the way towards modern power grids with high flexibility and efficiency. However, this will significantly change the characteristics of the AC grid and pose new challenges to the stability of the power system. In 1976, Middlebrook first presented the criterion that an electrical system is stable if the Nyquist contour of the product of the source impedance and load admittance remains within the unit circle [71]. Since then, impedance-based stability analysis has been used for power systems. The impedance-based stability criterion of grid-connected inverters was proposed in [74] and if the ratio between the grid impedance and the converter impedance satisfies the Nyquist stability criterion, the system will remain stable.

In this chapter, small-signal impedances are measured from time-domain RSCAD models for stability assessment of an HVDC system. Firstly, a small signal impedance extraction method in the positive/negative (PN) frame is introduced. The scenario of a simplified GB AC network connected with an MMC is given in RSCAD for real-time simulation use. The simplified GB network contains 8 buses and 5 regions with connections and power flow mainly based on the National Grid Electricity Ten Year Statement [69]. The proposed measurement method is applied to extract the impedance of the AC grid itself. In order to explore factors that affect the terminal impedance of the AC network, HVAC cables of different lengths are included between the AC network and the MMC. In addition, a method based on curve fitting is introduced to simplify the frequency-dependent cable model into a lumped parameter model that can be used by analytical analysis and stability assessment. The impact of different MMC modelling methods on the impedance of the MMC is also studied. Finally, the impedance-based stability assessment is presented using the measured AC system and MMC impedances.

5.1 Background of impedance-based stability assessment

The essence of the impedance method for stability assessment was published in 1979 [124]. The method divides the system under study into two parts: a source and a load subsystem. In this study, the AC network represents the source, and the MMC converter represents the load subsystem. As shown in Fig. 5.1, the source is modelled by its Thevenin equivalent circuit containing an output impedance in series with an ideal voltage source, while the converter, which is modelled as a controlled current source, is presented by the impedance in parallel with a current source by its Norton equivalent. The advantage of such representation is the possibility of applying SISO control theory. This linear representation cannot represent the nonlinear power electronic circuits, and thus, it is only valid for the small-signal analysis of converter circuits.

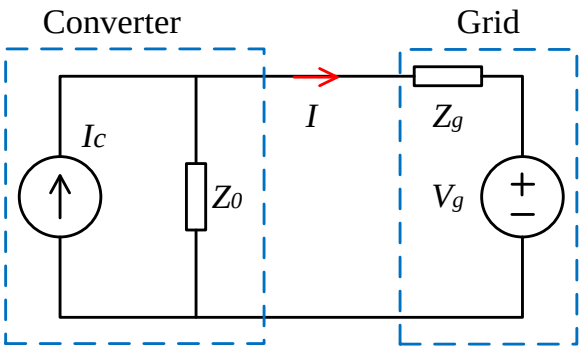


Fig. 5.1 Impedance based Small-signal equivalent circuit

The impedance-based stability criterion discussed in [74] is used in the study. Based on the equivalent circuit, the converter output current is:

$$I(s) = \frac{I_c(s)Z_0(s) - V_g(s)}{Z_0(s) + Z_g(s)} \tag{5.1}$$

which can be rearranged to:

$$I(s) = \left[I_c(s) - \frac{V_g(s)}{Z_0(s)} \right] \cdot \frac{1}{1 + \frac{Z_g(s)}{Z_0(s)}} \tag{5.2}$$

According to [74], a grid-connected converter will remain stable if the ratio of the grid impedance to the converter output impedance, $\frac{Z_g(s)}{Z_0(s)}$, satisfies the Nyquist criterion [74].

The main advantage of this method is that the stability assessment of the system only needs the equivalent impedances of the AC network and the converter without details of the inside parameters and control structures.

5.2 Impedance measurement in PN frame

Impedance-based stability analysis can be performed based on two measured impedances or based on a combination of the measured impedance and the impedance obtained from analytical models. Therefore, when making impedance measurements, consideration should be given to how to make the measured impedance more widely applicable.

Many analytical MMC models have been proposed. In [76] a harmonic-state-space MMC analytical model is proposed based on abc-frame. However, the PLL is not taken into account in this model, nor is the usually adopted dq-frame control loop. The dq-frame controllers can generate frequency coupling (positive and negative sequence) which is difficult to be reflected in abc-frame. In [80], MMC analytical model is proposed based on positive and negative (pn) frame (positive and negative sequence) with positive and negative sequence coupling considered. Due to the advantages of modelling impedances in pn frame including full consideration of frequency coupling, increased VSC analytical models are now being developed in pn-frame [125][126][127]. With this trend in mind, the impedance measurements in this chapter will be based on pn-frame.

5.2.1 Impedance measurement method

Frequency sweep is used to extract the network and MMC admittances using RSCAD simulation at the point of common coupling (PCC). Fig. 5.2 shows an example in which frequency sweep is applied to measure the impedance of the AC grid. As shown in Fig. 5.2, a three-phase voltage source $V_{per(ABC)}$ is connected in series to the measuring point, and frequency sweep is carried out. The voltage source is set to create a voltage magnitude at variable frequency. The frequency sweep is realized by continuous changes of fixed

frequency step. The steady-state time-domain voltage and current waveforms, i.e. $v_{pg(ABC)}$ and $i_{pg(ABC)}$ are measured in RSCAD.

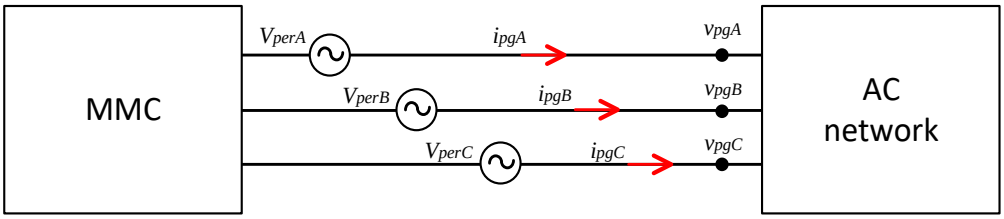


Fig. 5.2 Implementation of the frequency sweep

The measured grid voltage and current are then exported to MATLAB where Fourier analysis is carried out to calculate the voltage and current magnitudes and phases for each of the injected frequencies in the pn-frame. Due to the possible coupling between the P and N axes components, the admittances of the network at one specific frequency can be given as

$$\begin{bmatrix} i_{pgP} \\ i_{pgN} \end{bmatrix} = \begin{bmatrix} Y_{pp} & Y_{pn} \\ Y_{np} & Y_{nn} \end{bmatrix} \begin{bmatrix} v_{pgP} \\ v_{pgN} \end{bmatrix} \tag{5.3}$$

where Y_{pp} and Y_{nn} are the "self" admittances of the P and N axes, respectively. Y_{pn} and Y_{np} are the "cross" admittances from N to P and from P to N, respectively. v_{pgP} and v_{pgN} are the measured positive and negative sequence voltage at the specific frequency, respectively, whereas the i_{pgP} and i_{pgN} are the corresponding currents.

To extract the 4 admittances, two sets of voltage and current measurements for each frequency are required, and the admittances are calculated using

$$\begin{bmatrix} Y_{pp} & Y_{pn} \\ Y_{np} & Y_{nn} \end{bmatrix} = \begin{bmatrix} i_{P1} & i_{P2} \\ i_{N1} & i_{N2} \end{bmatrix} \begin{bmatrix} v_{P1} & v_{P2} \\ v_{N1} & v_{N2} \end{bmatrix}^{-1} \tag{5.4}$$

where subscripts 1 and 2 refer to the first and second injections.

When a positive sequence perturbation voltage $V_{perP(s)}$ is injected to the system as the first injection, the measured response voltage and current contain the positive sequence component of frequency s ($v_{p1(s)}$ and $i_{p1(s)}$) and the negative sequence component of

frequency $s-2\omega_0$ ($v_{N1(s-2\omega_0)}$ and $i_{N1(s-2\omega_0)}$), where ω_0 is the fundamental frequency of the system. In order to solve (5.4), the corresponding negative sequence perturbation voltage of frequency $s-2\omega_0$ is used as the second injection. When the second injection is applied, the measured responding voltage and current consist of components of frequency s ($v_{P2(s)}$ and $i_{P2(s)}$) and $s-2\omega_0$ ($v_{N2(s-2\omega_0)}$ and $i_{N2(s-2\omega_0)}$). The frequency sweep range is from 1Hz to 300Hz as the typical frequency of interest for MMC stability assessment ranges a few tens of Hertz to a few hundreds Hertz. When $s-2\omega_0<0$, the corresponding second measurement actually injects equivalent positive sequence perturbation voltage of frequency $2\omega_0-s$ instead of negative frequency voltage. Considering all the conditions mentioned above, (5.4) can be rewritten as:

$$\begin{bmatrix} Y_{pp(s)} & Y_{pn(s)} \\ Y_{np(s-2\omega_0)} & Y_{nn(s-2\omega_0)} \end{bmatrix} = \begin{bmatrix} i_{P1(s)} & i_{P2(s)} \\ i_{N1(s-2\omega_0)} & i_{N2(s-2\omega_0)} \end{bmatrix} \begin{bmatrix} v_{P1(s)} & v_{P2(s)} \\ v_{N1(s-2\omega_0)} & v_{N2(s-2\omega_0)} \end{bmatrix}^{-1} \quad (s \geq 2\omega_0)$$
$$\begin{bmatrix} Y_{pp(s)} & Y_{pn(s)} \\ Y_{np(2\omega_0-s)} & Y_{nn(2\omega_0-s)} \end{bmatrix} = \begin{bmatrix} i_{P1(s)} & i_{P2(s)} \\ i_{N1(2\omega_0-s)} & i_{N2(2\omega_0-s)} \end{bmatrix} \begin{bmatrix} v_{P1(s)} & v_{P2(s)} \\ v_{N1(2\omega_0-s)} & v_{N2(2\omega_0-s)} \end{bmatrix}^{-1} \quad (s < 2\omega_0) \tag{5.5}$$

5.2.2 **Time-domain RSCAD model formulation and impedance measurement**

In order to measure the network admittance at a specific operating point, the simplified GB AC network model is developed and connected to an MMC model in RSCAD as shown in Fig. 5.3. The DC side of the MMC model is connected to a DC source. The MMC transfers 1000MW active power to the AC grid at unity power factor. The HVAC cable connects the network model and MMC model which are implemented in two different RTDS racks. The HVAC cable is modelled by a frequency-dependent model with physical parameters and the length of the cable can be varied to represent the different connection distances of the converter from the network.

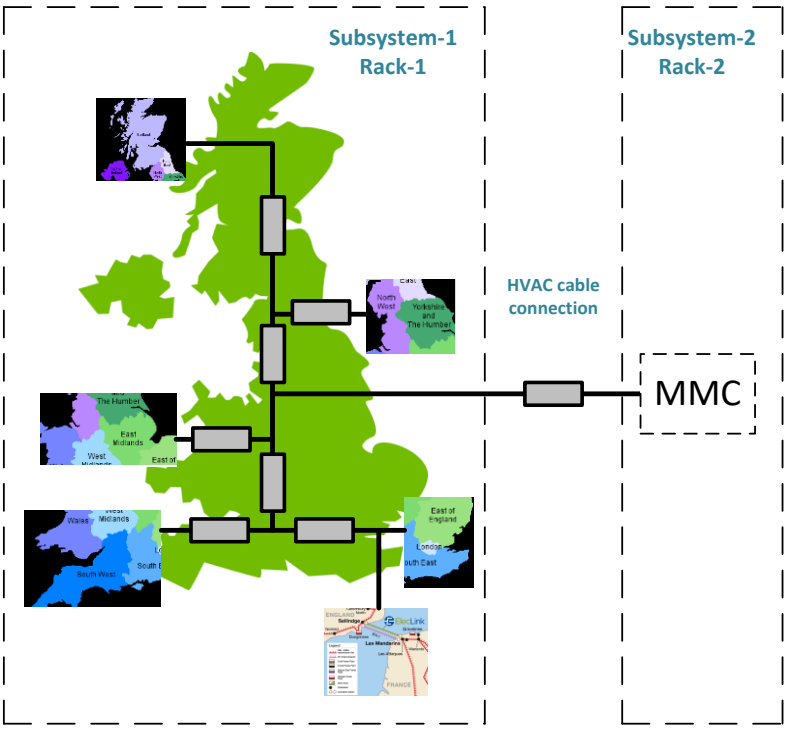
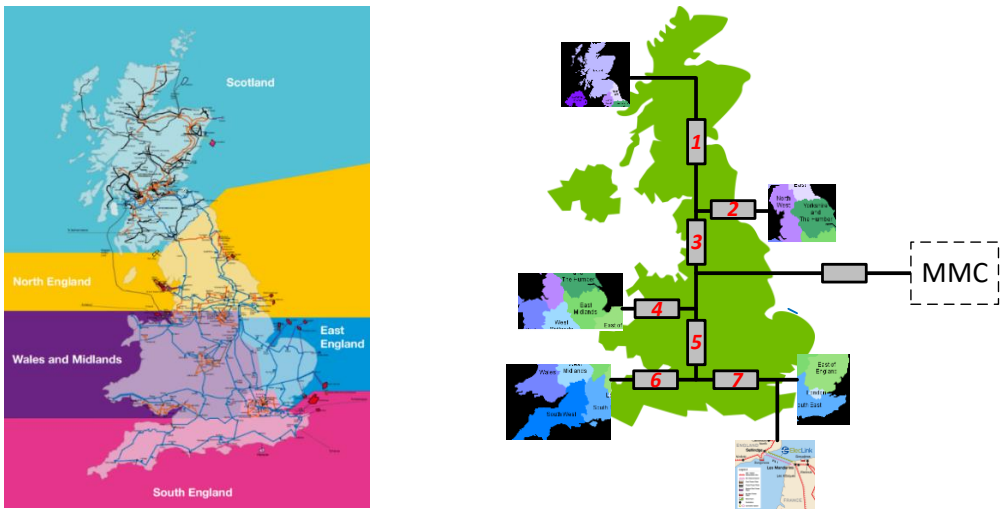


Fig. 5.3 RSCAD implementation of the AC network and MMC models

5.2.2.1 *The time-domain GB network model*

The existing simplified GB AC grid model is based on real power flow data of the eight areas as presented in the Electricity Ten Year Statement (ETYS) of the UK National Grid (NG) [69]. The AC grid model includes 5 regions of the UK, as shown in Fig. 5.4 (a) and (b), where each region is represented by an AC generator and a dynamic load. The model is developed in RTDS as a simplified 8-bus aggregated dynamic model representing key generation and load areas, as shown in Fig. 5.5. Each AC generator is modelled as an aggregated large synchronous machine with a step-up transformer (13.8kV/400kV) to represent the generation at the related area. The rating of each generator is set according to the UK 2019 load flow [69].



(a) (b)

Fig. 5.4 (a) Regional map of the UK Electricity Transmission System[69]; and (b) Simplified 8-bus GB network representation

The AC overhead transmission lines of the AC grid are modelled using PI-section line models with lumped resistance (R), capacitance (C), and inductance (L). The line parameters (R, C and L) are calculated from the power flow data (P, Q, |V| and voltage angle) provided by the NG ETYS for 2019 [69]. The same methodology for modelling the UK transmission system as presented in [128] is used, which calculates the line parameters based on the required power flow at each bus.

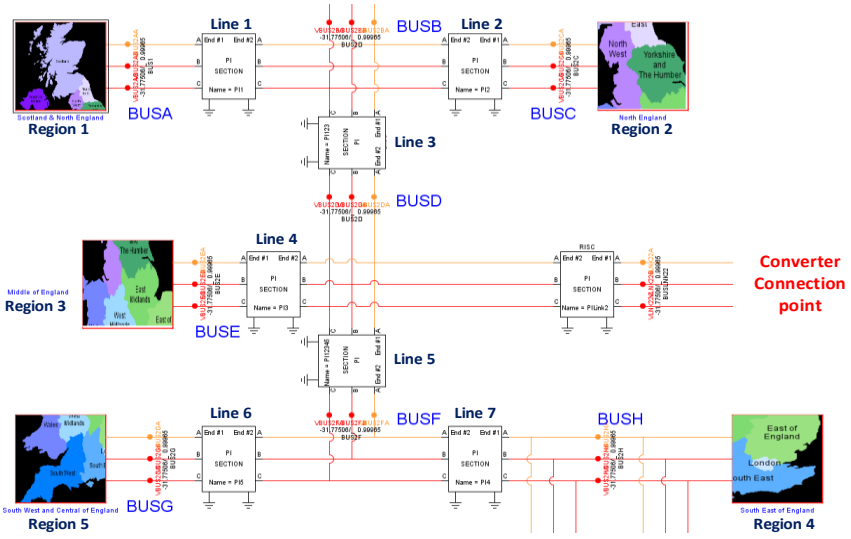


Fig. 5.5 The 8-bus network model implemented in RTDS

The parameters of the generators, loads and transmission lines of the model shown in Fig. 5.5 are listed in Table 4, Table 5 and Table 6, respectively. The loads in the RTDS model are modelled as constant power loads whose P and Q are pre-specified. Thus, the simulation calculates the admittance of each load at every time step, considering the voltage magnitude at the load terminal. The data used in this test is a simplification from the power flow data (P, Q, |V| and voltage angle) provided by the NG ETYS for 2019 [69] by merging areas together into 5 regions.

Table 4 Parameter of the generators (per unit values base on the rated voltage of 13.8kV)

	Rated MVA	X_a	X_d	X_d’	X_q	X_q’	R_a	T_{d0}’	T_{d0}’’
G1	11000	0.20	2.3	0.4	2.3	\	0.001	10	0.05
G2	20000	0.20	2.3	0.4	2.3	\	0.001	10	0.05
G3	9160	0.20	2.3	0.4	2.3	\	0.001	10	0.05
G4	14980	0.11	2.3	0.4	2.3	\	0.005	10	0.05
G5	5500	0.20	2.3	0.4	2.3	\	0.005	10	0.05

Table 5 Parameter of the loads

Regions	SG active power setting (MW)	Load	
		Active power (MW)	Reactive power (MVar)
Region 1	9350	8486	4110
Region 2	14200	12548	6077
Region 3	8794	8398	4067
Region 4	14530	17852	10005
Region 5	5500	4150	1041

Table 6 Parameters of the transmission lines (at 50 Hz)

Lines	Resistance (ohms)	Inductive reactance at 50Hz (ohms)	Capacitive reactance at 50 Hz (Mega ohms)
Line 1	2.030	25.024	0.078
Line 2	0.838	11.222	0.037
Line 3	0.007	6.232	0.007
Line 4	4.800	48.500	1.000
Line 5	0.007	6.232	0.007
Line 6	0.007	4.232	0.080
Line 7	2.816	26.122	0.080

5.2.2.2 *Impedance measurement of the GB network*

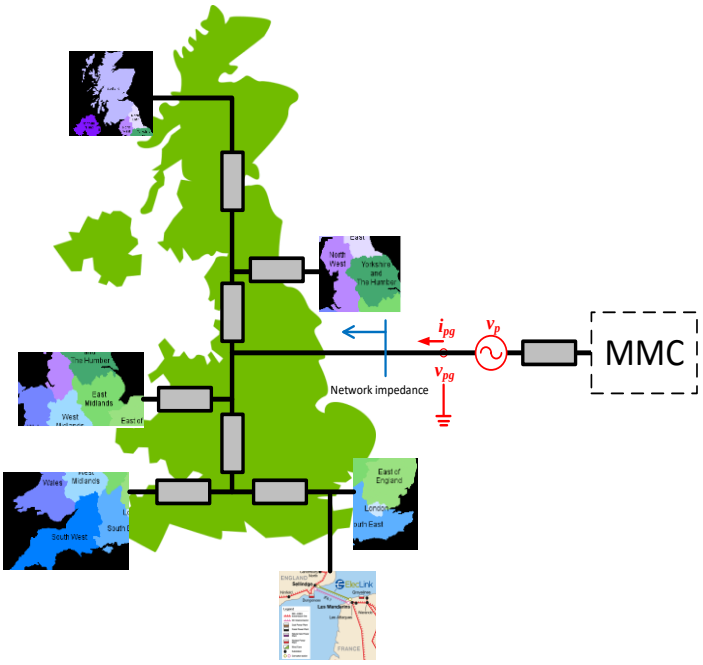
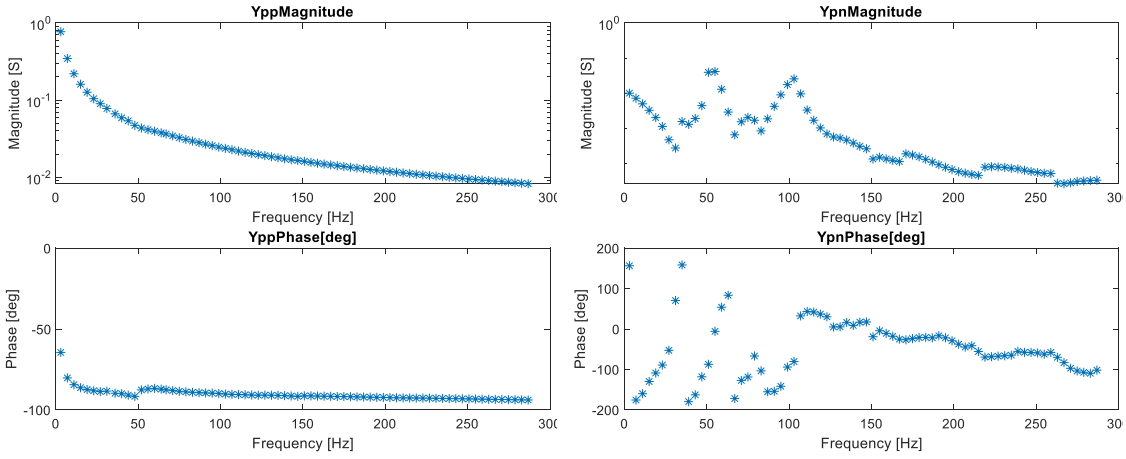


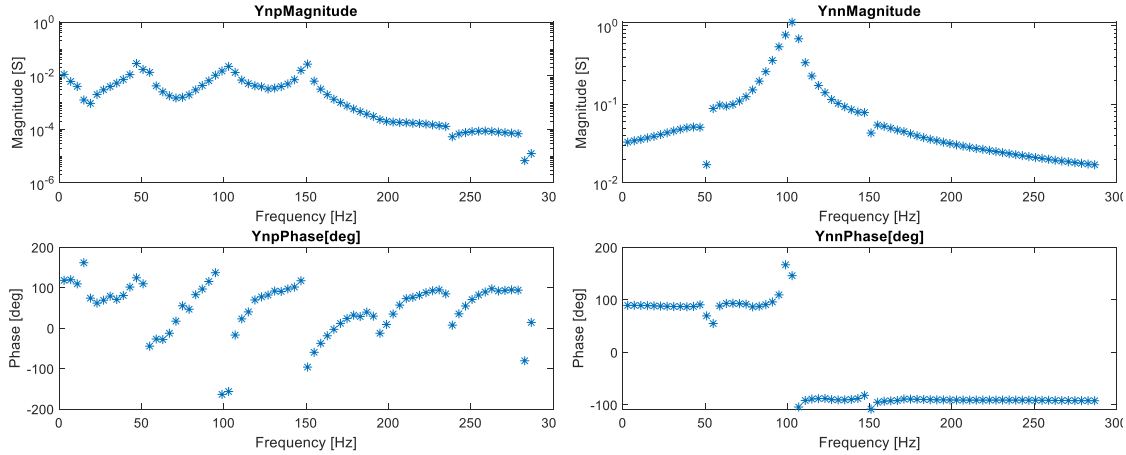
Fig. 5.6 Impedance measuring point of the GB network (excluding cable)

Fig. 5.6 shows the location of the frequency injection for impedance measurement of the GB AC network and Fig. 5.7 (a) shows the corresponding measured positive sequence admittance Ypp which appears largely inductive. As the negative sequence admittance $Y_{NN}(s-2j\omega_0)$ includes a 100Hz frequency shift, $Y_{NN}(s-2j\omega_0)$ shown in Fig. 5.7 (d) for frequency range over 100Hz has a similar shape as the $Y_{PP}(s)$ from 0Hz, whereas the shape of $Y_{NN}(2j\omega_0-s)\_magnitude$ between 0 to 100Hz is similar to the mirror shape of $Y_{PP}(s)\_magnitude$ in the same frequency range. Equally, the shape of $Y_{NN}(2j\omega_0-s)\_phase$ between 0 to 100Hz is similar to that of $Y_{PP}(s)\_phase$. When the injected frequency closes to the nominal operation frequency of 50Hz during frequency sweep, the nominal operating condition affects the measurement accuracy of the injected voltage and current at such frequency and consequently, leads to some errors of the measured admittance. As can be seen, for the specific AC network model investigated, the measured admittances are largely inductive.



(a) Y_{PP}

(b) Y_{PN}



(c) Y_{NP}

(d) Y_{NN}

Fig. 5.7 Measured network admittance seen at the network terminal

Fig. 5.7 (b) and (c) show the measured coupling admittances Y_{PN} and Y_{NP}. It can be seen that the magnitudes of Y_{PN} and Y_{NP} are much smaller than those of Y_{PP} and Y_{NN} indicating weak admittance cross-coupling between the P and N axes of the AC network. The large phase variations of Y_{PN} and Y_{NP} as shown in Fig. 5.7 (b) and (c) are due to the fact that the introduced coupling voltages and currents are all small and thus even a very small measurement error can lead to large phase variation.

From the admittance shown in Fig. 5.7, it can be observed that the dynamics of the synchronous generators and their controls do not affect the admittances of the system seen at the connection point. This is largely due to the fact that their impact frequency (below

ten hertz) is much lower than the frequency of interest for converter stability (from tens hertz to hundreds hertz). The AC network admittance appears similar to a purely inductive network.

5.2.2.3 *Cable modelling and its impact on grid admittance*

In the previous section, the grid impedance measured at the AC connection point was obtained. As the natural resonant frequencies of typical AC cables are in the frequency range of interest for converters, the existence of AC cables close to HVDC converters can potentially have a significant impact on system stability. In this section, various cable modelling methods are explored, and their impact on network impedance is assessed considering different cable lengths.

To capture the dynamics of AC cables, the frequency-dependent model is used as a benchmark. The structure and detailed parameters of the HVAC cables are given in Fig. 5.8 and Table 7, which are provided by industrial partners in PROMOTioN project funded by the European Union's Horizon 2020 scheme and will be published in the project report Deliverable 3.7: Compliance evaluation results using simulations. Based on these physical parameters and materials, the AC cable is modelled in RSCAD using Cable_V2 tool, as depicted in Fig. 5.9. It should be noted that the RTDS Cable model is limited to model the capacitive and inductive coupling within one single-phase concentric cable. Modelling of the electromagnetic coupling between parallel cables is not supported.

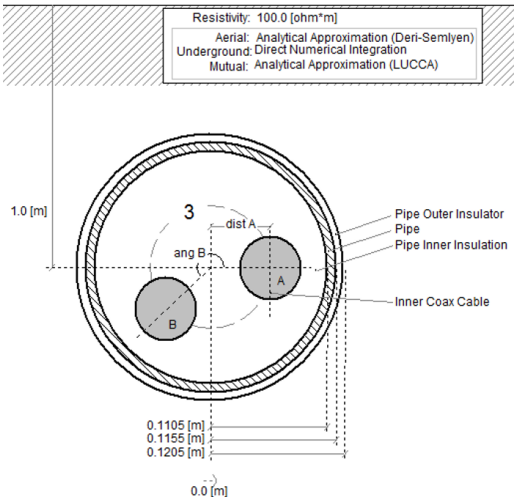
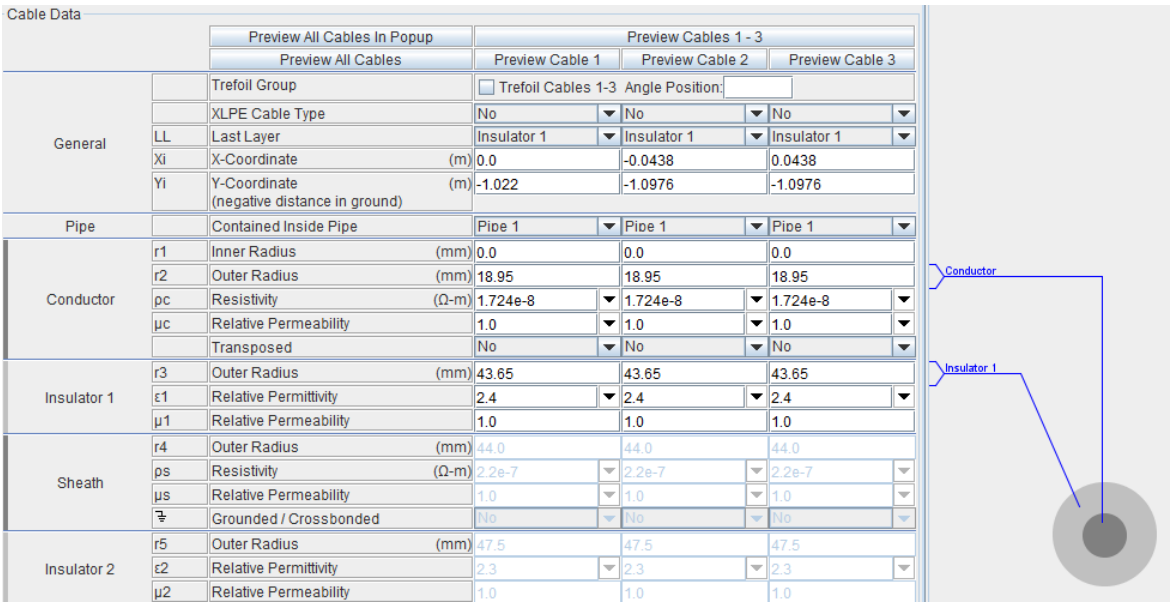


Fig. 5.8 AC cable structure

Table 7 Cable parameters from the PROMOTioN Project

Parameters	**Value**
Power	1000 MW
Frequency	50 Hz
Rated voltage	220 kV
Maximum admissible voltage	245 kV
Conductor cross-section	1000 mm^2
Conductor material	Copper
Insulation material	XLPE
Armour material	Steel
Diameter of conductor	37.9 mm
Insulation thickness	23.0 mm
Diameter over insulation	87.3 mm
Lead sheath thickness	3.1 mm
Outer diameter of the cable	241.0 mm
Capacitance	0.19 µF/km
Charging current per phase at 50 Hz	7.4 A/km
Inductance	0.38 mH/km



(a) Cable data

Pipe Data

		Preview All Pipes In Popup	
		Preview All Pipes	Preview Pipe 1
Manual Override		Specify X,Y	☑ Manually
		Specify Inner Insulator Radius	☑ Manually
		Specify Conductor (Pipe) Radius	☑ Manually
General	Xi	X-Coordinate (m)	0.0
	Yi	Y-Coordinate (m) (negative distance in ground)	-1.0725
Inner Insulator	r1	Outer Radius (mm)	110.5
	εi	Relative Permittivity	2.4
	μi	Relative Permeability	1.0
Conductor (Pipe)	r2	Outer Radius (mm)	115.5
	ρc	Resistivity (Ω-m)	1.8e-7
	μc	Relative Permeability	100.0
	⏚	Ground Pipe	Yes
Outer Insulator		Has Outer Insulation	Yes
	r3	Outer Radius (mm)	120.5
	εo	Relative Permittivity	2.4
	μo	Relative Permeability	1.0
		Conductors Per Pipe:	0
		(Pipe) Conductors Total:	0
		(Pipe + Cable) Conductors Total:	3

(b) Pipe data

Fig. 5.9 Layout of AC cable model in Cable_V2 tool (RSCAD)

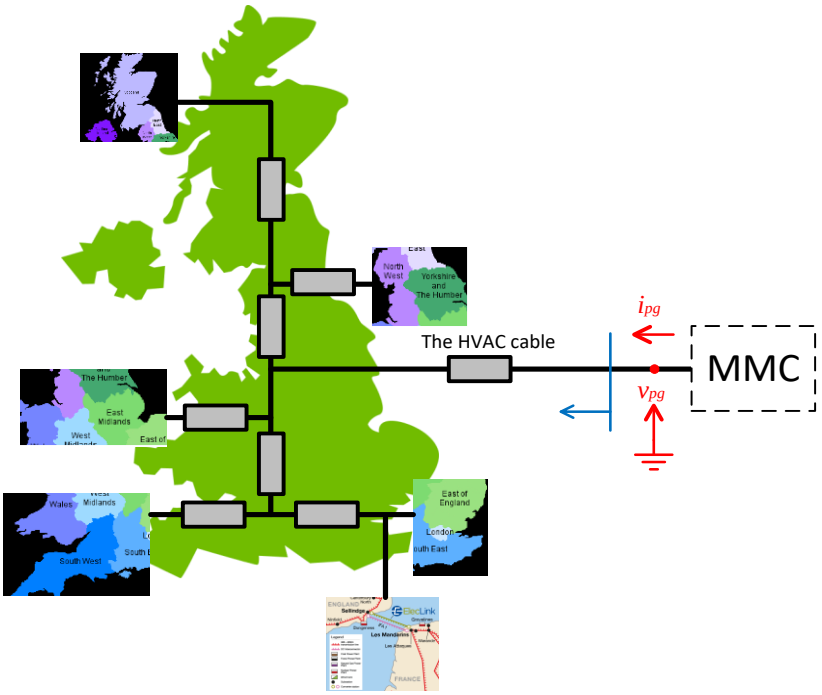
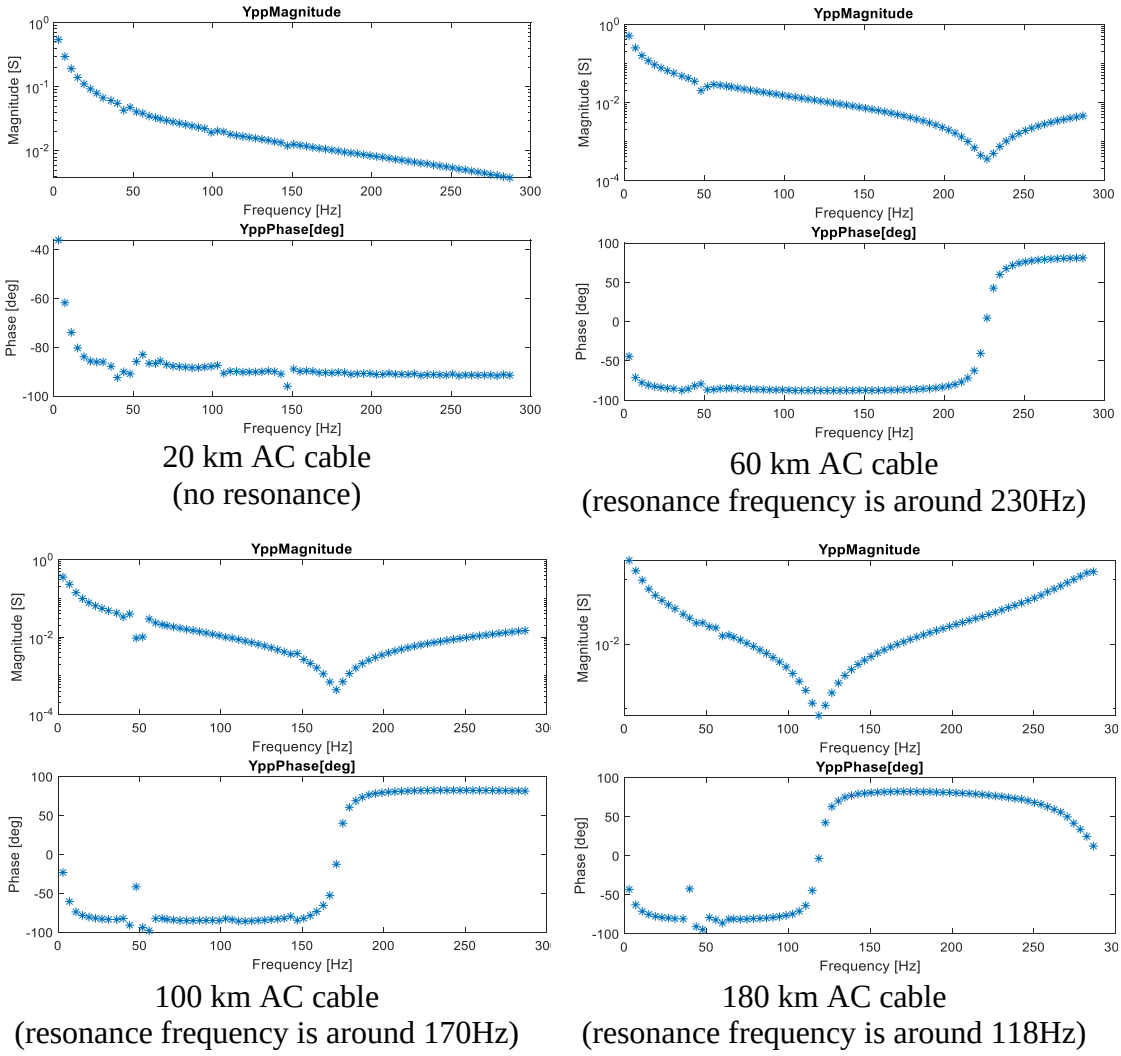


Fig. 5.10 Impedance measuring point of the AC network including HVAC cable

After moving the impedance measuring point to include the AC cable in the simplified GB network as shown in Fig. 5.10, the AC grid admittance at the MMC connection terminal is measured. The admittance Y_{PP} measured at this point varies with the length of the connecting cable between the GB network and the converter as shown in Fig. 5.11 (a)-(d). When a 20km cable is applied, the measured admittance remains largely inductive as the previous case shown in Fig. 5.7(a). However, resonance appears at around 230Hz when a 60km cable is used. The resonant frequency is reduced to 170 Hz for a 100km cable and further to 118Hz with a 180km cable. Such resonant frequencies are in the typical frequency ranges of MMC converter responses and thus it potentially can significantly impact on system stability.



20 km AC cable
(no resonance)

60 km AC cable
(resonance frequency is around 230Hz)

100 km AC cable
(resonance frequency is around 170Hz)

180 km AC cable
(resonance frequency is around 118Hz)

Fig. 5.11 Grid admittance versus different cable length

Therefore, it is necessary to consider AC cables when analysing the stability of HVDC systems. However, it is difficult to implement frequency-dependent model of AC cable in analytical studies. The underlying problem is thus how to simplify AC cable models whilst retaining accurate cable dynamic characteristics.

According to CIGRE guidebook [129], a simplified pi-section model is established for a 60km AC cable based on the physical parameters, as shown in Fig. 5.12. This lumped parameter model takes the following into account:

- Data related to the construction characteristics of the cable: layout (parallel single-core cables and pipe type cables), geometry and properties of the conducting and insulating materials (conducting and insulating layers).
- Data related to the surrounding conditions (in air, buried directly underground, in ducts, troughs or in steel pipes).
- Skin and proximity effects for the calculation of AC resistance of conductors.
- Dielectric losses, screen and armour losses, losses in steel pipes, etc.

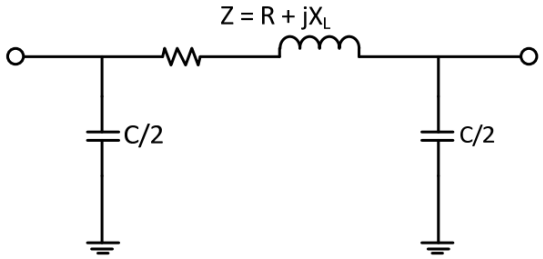


Fig. 5.12 Equivalent AC cable model using RLC representation

According to the parameters listed in Table 7 and Fig. 5.8, the measured grid admittances Y_{PP} with the 60km HVAC cable using lumped PI section model calculated using the CIGRE guidebook and frequency-dependent model are compared in Fig. 5.13.

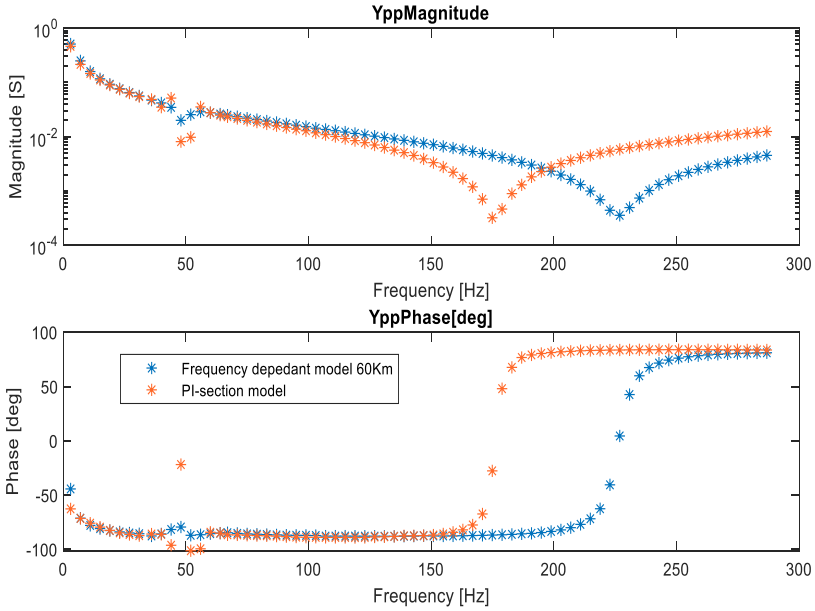


Fig. 5.13 Comparison of Grid admittances with 60 km HVAC cable using lumped RLC PI section model and frequency-dependent cable model

From Fig. 5.13, it can be observed that the lumped RLC model doesn't fit the frequency-dependent model well. The resonance frequency of the AC grid using the lumped model is 174.5Hz compared to 226.8Hz using the frequency-dependent model. The error is largely caused by using simplified formulas with approximations in the RLC model, e.g. the depth of cable and actual cross-bonded configuration are not considered in the manual calculation [129]. Additional measurements with increased PI sections using the calculated RLC model provide similar results as that of the single PI section model.

In order to obtain the lumped parameter model which can accurately represent the resonance frequency for analytical studies, the curve fitting method is applied to the RLC calculation method. Considering the resonance in the grid caused by *LC* oscillations, the resonance frequency f_{FD} of the frequency-dependent model can be approximated as:

$$f_{FD} = \frac{1}{2\pi\sqrt{LC_{FD}}} \tag{5.6}$$

Similarly, the resonance frequency f_{PI} of the AC grid using the pi-section model can be approximated as,

$$f_{PI} = \frac{1}{2\pi\sqrt{LC_{PI}}} \tag{5.7}$$

where the value of C_{PI} is calculated according to the CIGRE method [129] as

$$C_{PI} = 2\pi\varepsilon_r\varepsilon_0 / \ln(\frac{D}{d}) \tag{5.8}$$

Dividing (5.7) by (5.6) and applying further algebraic manipulations, the revised capacitance used in the simplified PI section model is thus determined by:

$$C_{PI(new)} = C_{FD} = C_{PI}\left(\frac{f_{PI}}{f_{FD}}\right)^2 \tag{5.9}$$

Using the measured resonant frequencies of 174.5Hz and 226.8Hz for the original PI section model and frequency-dependent model, the new equivalent $C_{PI(new)}$ is thus calculated using (5.9). Without changing the L and R values, the measured admittance using the revised lumped RLC model is depicted in Fig. 5.14. As can be observed, the resonance frequency shown by the new pi-section model is almost in accordance with that from the frequency-dependent model, and thus can be used for analytical system stability studies if required.

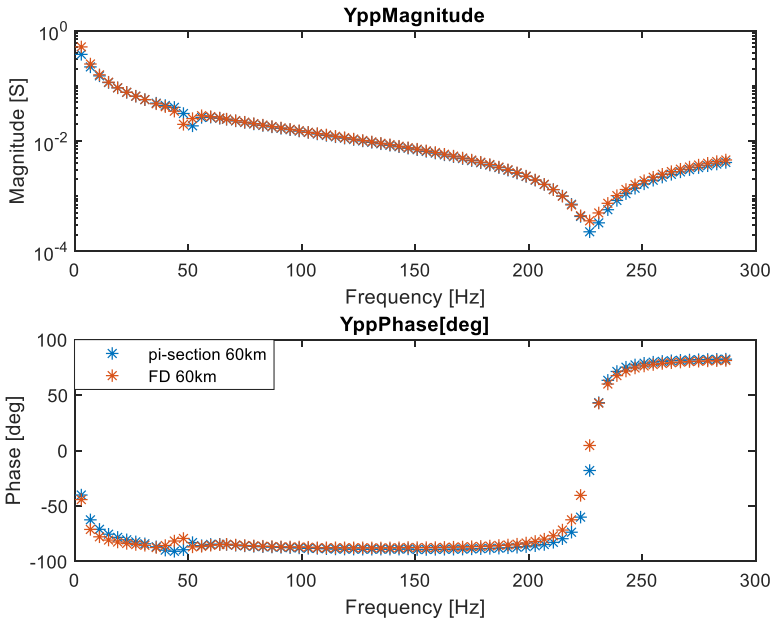


Fig. 5.14 Grid admittance using the revised lumped RLC model

5.2.3 **Impedances of MMC with different time-domain modelling methods**

Different time-domain MMC models have been developed and validated in PSCAD and RSCAD in Chapter 3 and Chapter 4. So far, many researchers have investigated the modelling methods of MMC, but hardly on the terminal characteristics of those models from the small-signal stability aspect [36]-[57]. A lot of publications have proposed frequency-domain analytical MMC models considering the effect of internal dynamics on the terminal impedance characteristics; however, all of them are based on averaged MMC model without a comparison of other time-domain modelling methods[76]-[81]. Therefore, the impact of different MMC modelling methods on the AC-side terminal impedance of the MMC remains to be studied. In the MMC topologies discussed in the previous chapters, the performance of each topology under steady-state operation has been validated. Therefore, the half-bridge topology which has the simplest structure among those topologies is used for steady-state impedance measurement and stability analysis in this section. A single terminal MMC-HVDC system is modelled in PSCAD as shown in Fig. 3.4, with full sets of controllers as shown in Fig. 2.11, and detailed system parameters listed in Table 1. The impedance measuring method as described in Section 5.2.1 is applied at MMC AC terminal as shown in Fig. 5.15 with a magnitude of the perturbation voltage equals to 3kV (around 0.8% of the converter-side rated AC voltage). The disturbance is injected at the frequency range of interest(3-287Hz) with 4Hz constant interval.

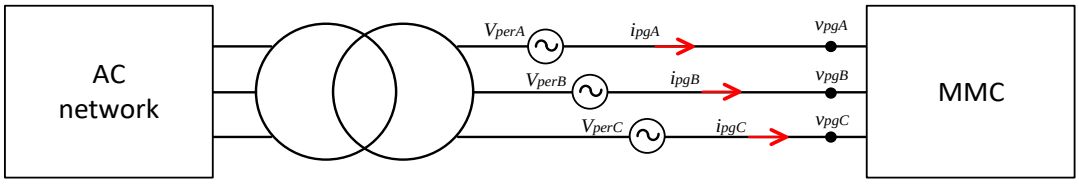
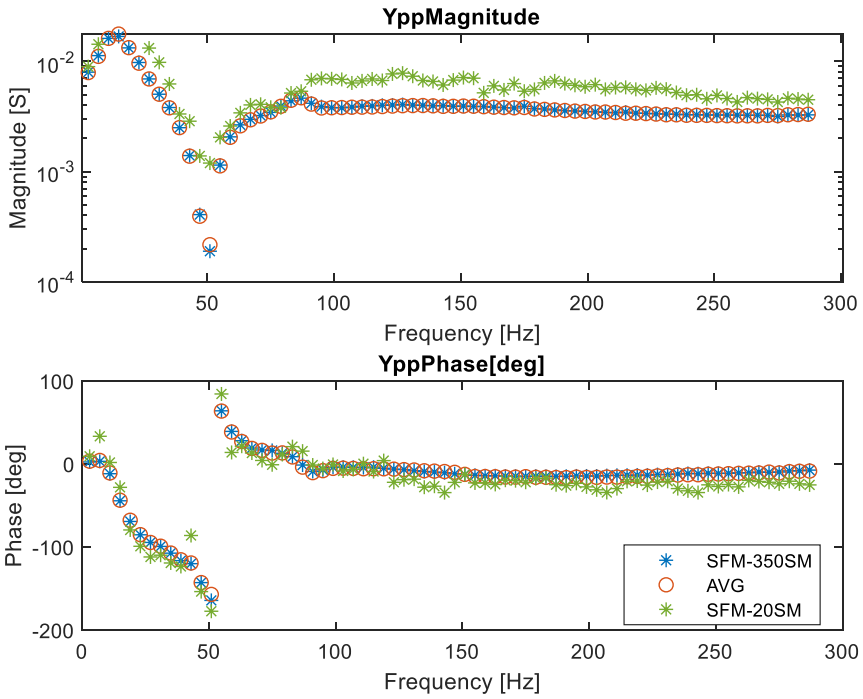
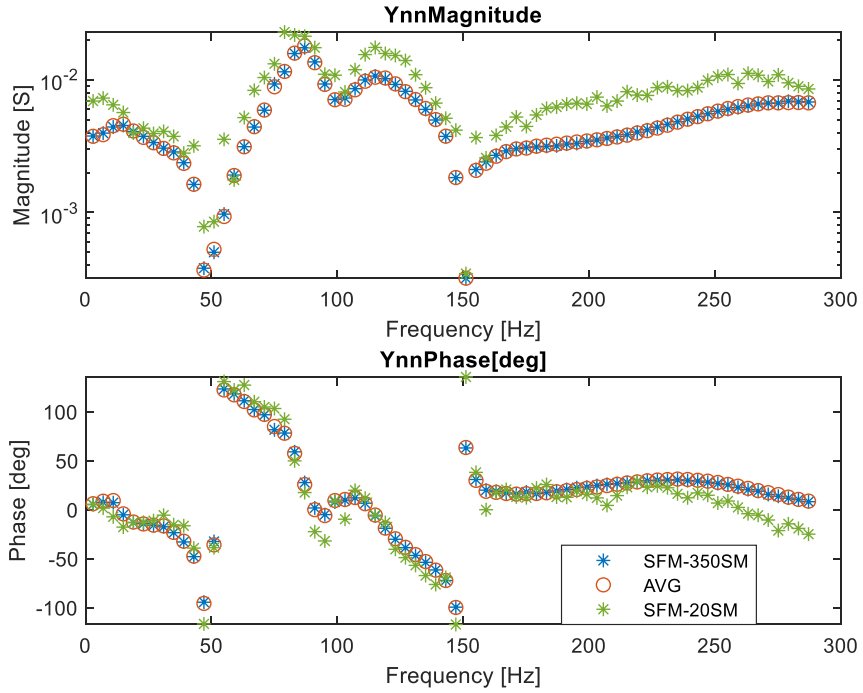


Fig. 5.15 Impedance measurement of the MMC

By applying the same impedance measurement method, the impedances of the MMC using the averaged model, SFM with 350 SMs per arm and SFM with 20 SMs per arm are compared in Fig. 5.16.



(a) Y_{pp}



(b) Y_{nn}

Fig. 5.16 Admittances comparison of averaged model and SFM with different levels

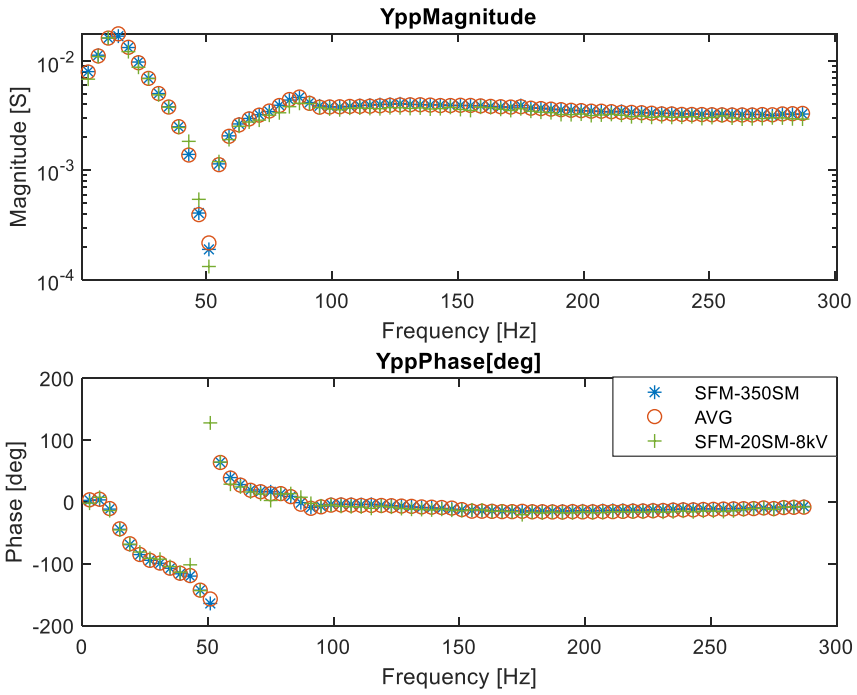
It can be observed that in comparison, the admittance of the averaged model overlaps that of the SFM with 350 SMs per arm in both magnitude and phase, and the admittance of the SFM (20 SM per arm) is also similar to those of the other two models, but with a larger magnitude. The phenomenon observed in Y_{nn} is similar to that in Y_{PP}.

In order to find out the reason why the admittance of SFM (20sm) is different from that of other models, the total harmonic distortion (THD) of the AC voltages of the three models being compared are calculated. Taking the waveforms when a 167Hz perturbation voltage is injected as an example, FFT analysis of the positive sequence phase A output voltages of the three models are carried out in MATLAB. With 50Hz as the fundamental frequency and 300Hz as the maximum frequency, FFT analysis results are shown in Table 8. According to Table 8, the AC voltage THD of SFM (20 SMs per arm) THD_{s20} is significantly higher than those of other two models. Large harmonics may affect the accuracy of the measurement and FFT analysis of the response after the injection of the perturbation voltage.

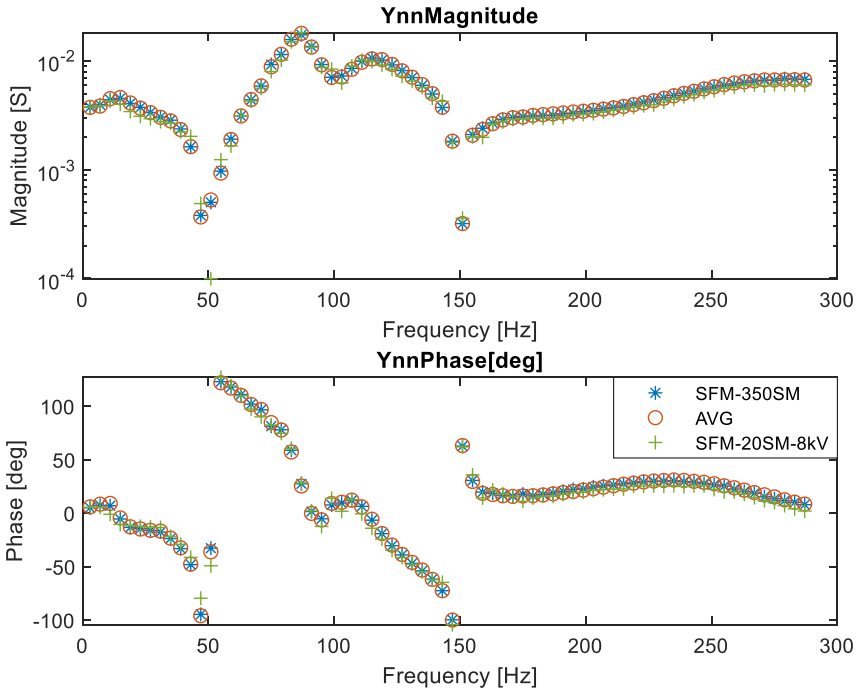
Table 8 AC voltage THD of the 3 models when a 167hz perturbation voltage is injected

Model	THD
AVG	$THD_a = 1.92\%$
SFM (350SM)	$THD_{s350} = 2.05\%$
SFM (20SM)	$THD_{s20} = 3.06\%$

In order to minimize the interference of harmonics on the impedance measurement, magnitude of the perturbation voltage injected into the SFM (20SMs per arm) is increased from 3kV to 8kV. The newly measured admittance of the SFM (20 SMs per arm) is added to the comparison as shown in Fig. 5.17. It can be observed that the admittance of SFM (20 SMs per arm) is now almost the same as those of the other models.



(a) Y_{pp}



(b) Y_{nn}

Fig. 5.17 Admittances of SFM (20 SMs per arm) with the magnitude of perturbation voltage increased to 8kV

Therefore, it can be concluded that:

- MMC Averaged model and switching function model can present almost the same external impedance on the AC side. This comparison not only validates the developed MMC models have identically same AC side impedance characteristics but also provides theoretical support for various small-signal MMC analytical models developed based on the averaged model [76]-[81].
- SFM with 20 SMs per arm and 350 SMs per arm present practically the same impedance. Given that there is already a large span between 20 and 350, this comparison also illustrates the number of SMs per arm for SFM has little effect on the AC-side impedance of the converter within a specific frequency range.
- The magnitude of the injected perturbation voltage can influence the extraction of small-signal impedance, especially when the THD of the MMC output voltage is high. Relatively high magnitude perturbation voltage will be required when the number of SM is low in the SFM in order to improve the accuracy of the impedance measurement.

5.3 Impedance-based stability assessment

A system model with an MMC connected to the simplified GB AC network is developed in RSCAD, as shown in Fig. 5.18. An averaged model MMC is connected to the GB AC network presented in Section 5.2.2.1 through a 20km frequency-dependant HVAC cable. The MMC is modelled with full sets of controllers as shown in Fig. 2.11 and detailed system parameters listed in Table 1. The frequency-domain HVAC cable with parameters and modelling details given in Table 7 and Fig. 5.9 is implemented.

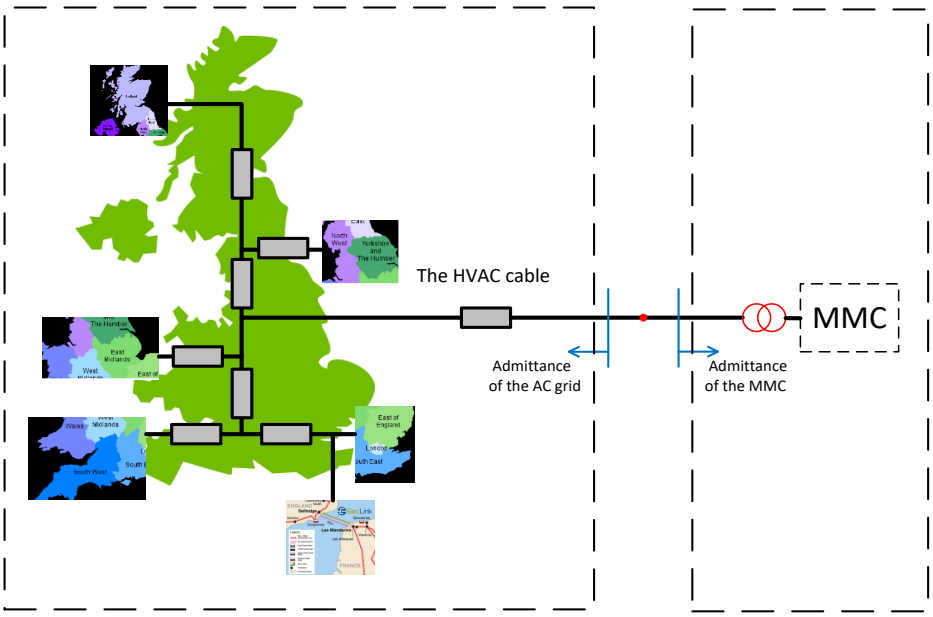
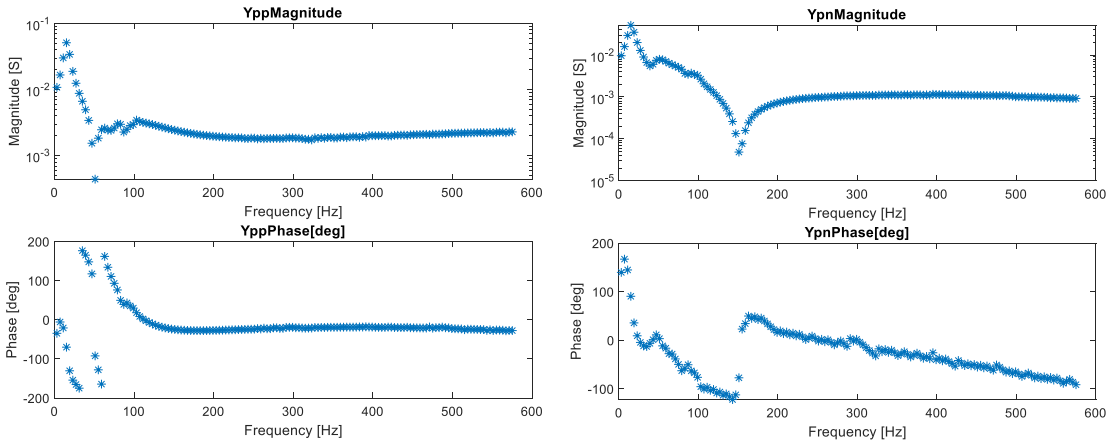
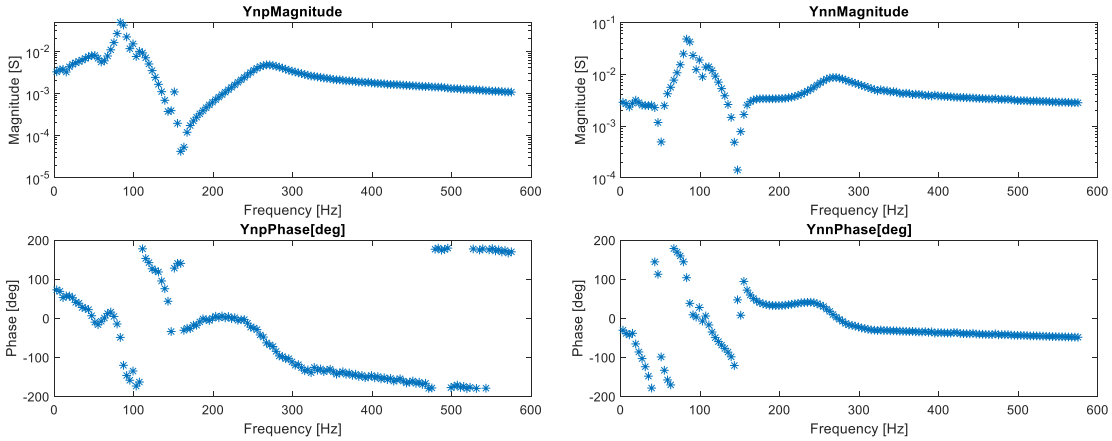


Fig. 5.18 A grid-connected converter system used for impedance-based stability assessment

The admittances of the MMC and the AC grid are measured in PN-frame, as shown in Fig. 5.19 and Fig. 5.20, using the method presented in Section 5.2.1. Frequency scan is applied from 3 Hz to 575Hz with 4Hz constant interval. The magnitude of the injected perturbation voltage is 8kV.

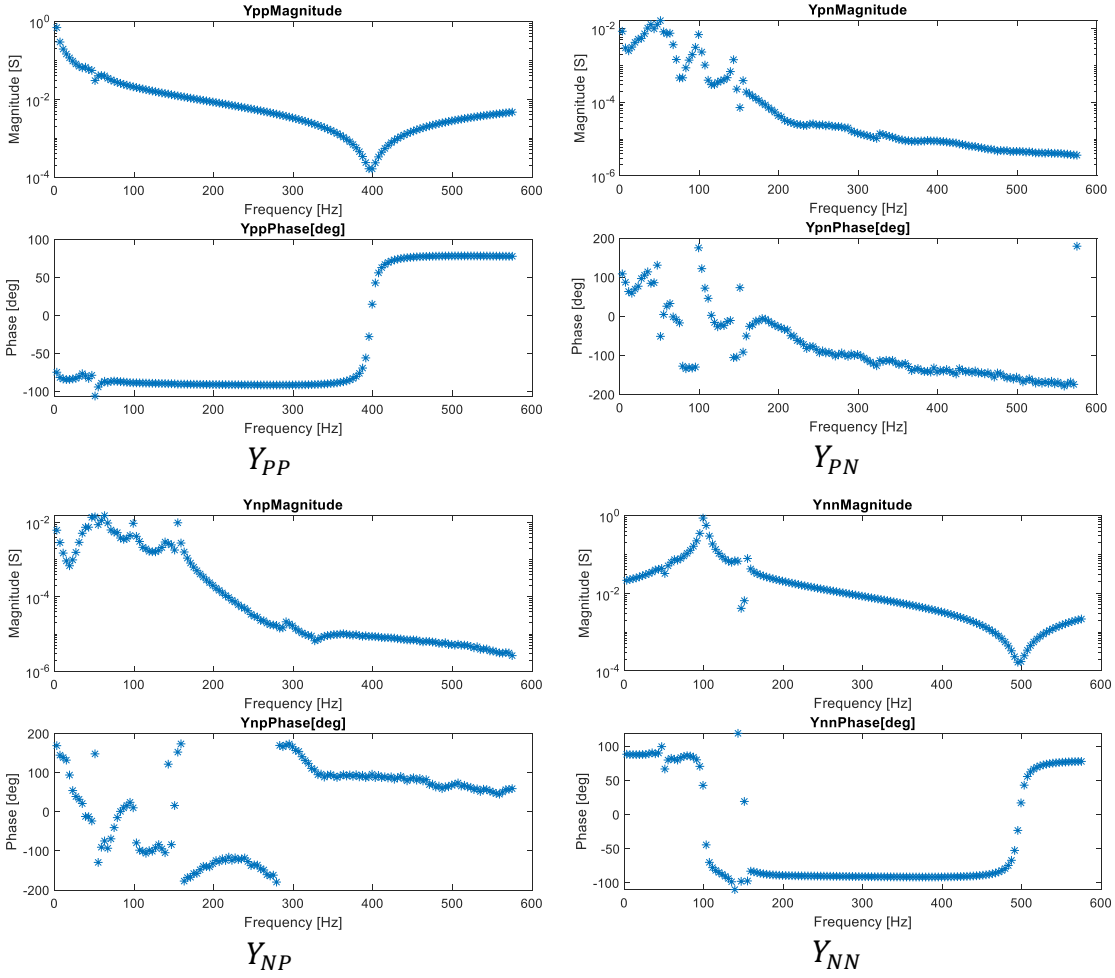


Y_{PP} Y_{PN}



Y_{NP} Y_{NN}

Fig. 5.19 Admittance of the MMC for stability analysis use

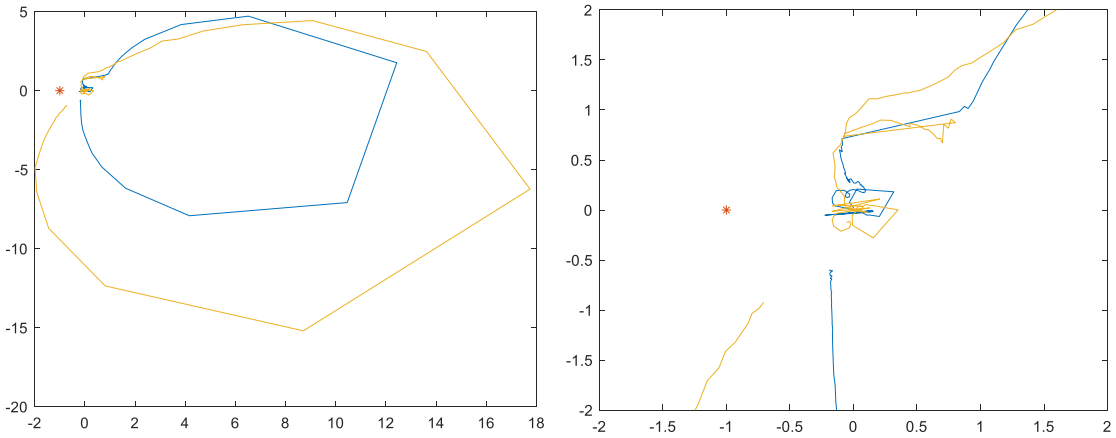


Y_{PP} Y_{PN}

Y_{NP} Y_{NN}

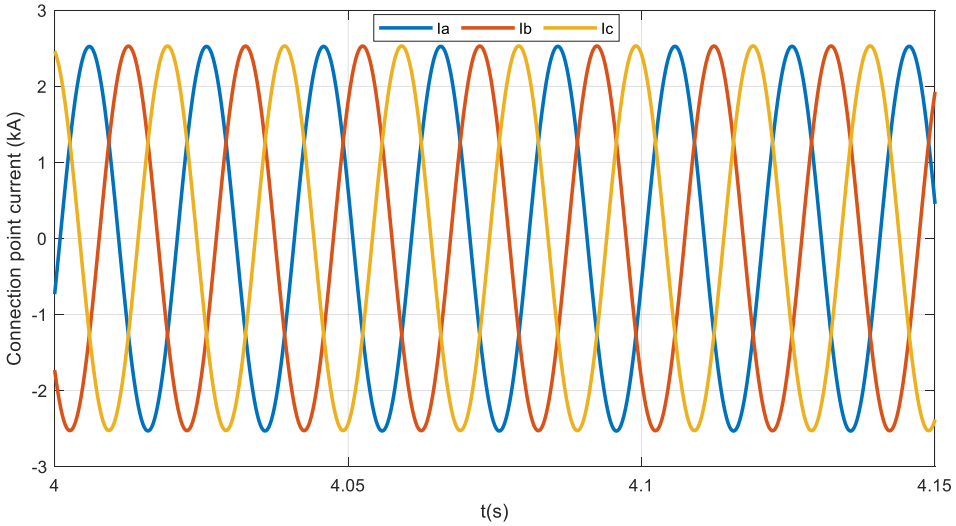
Fig. 5.20 Admittance of the AC grid for stability analysis use

The MMC in the grid-connected converter system has the same parameters as that in Section 5.2.3, however, the measured admittances differs, which due to different operating points caused by changes of the AC side. It can be observed from Fig. 5.19 and Fig. 5.20 that, the coupling admittances Y_{pn} and Y_{np} of the grid and the MMC are much smaller than Y_{pp} and Y_{nn}. The extracted admittances are used for stability assessment of the system. After applying the impedance-based stability criterion proposed in [74], Fig. 5.21 depicts the Nyquist diagram of the ratio of the grid impedance to the converter output impedance in the range 3-575Hz. According to the Nyquist criterion, the grid-connected converter system is stable due to the curve is not encircling the critical point (-1,0) [74]. The voltage and current in Fig. 5.22 are measured at the point of common coupling (PCC) in time-domain, and the system stability can also be observed in the time domain simulation, which is consistent with the conclusion of the impedance-based stability analysis.

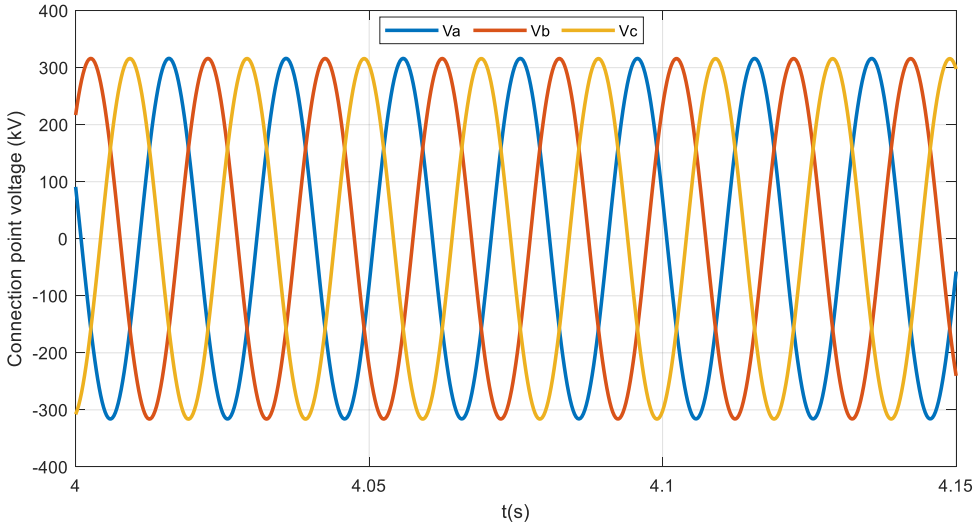


(a) Full-scale Nyquist diagram (b) Zoomed Nyquist diagram

Fig. 5.21 Nyquist diagram of the grid-connected converter system



(a) 3-phase AC current at the connection point



(b) 3-phase PCC voltages

Fig. 5.22 PCC currents and voltages

5.4 **Summary**

In this chapter, impedance measurement of the AC network and MMC has been performed. The method of impedance extraction in time-domain and the impedance-based stability analysis were described. The effects of AC cable and MMC time-domain modelling methods on the impedances have also been studied.

The results of the impedance measurement show that the AC cable connected to the converter has a significant impact on the AC grid impedance, the longer the AC cable, the lower the resonance frequency of the AC system. When the length reaches a certain level, the resonance frequency is in the typical frequency ranges of MMC converter responses and potentially this can significantly impact on system stability. In order to accurately reflect the resonance point introduced by the cable, a lumped parameter model optimization method that can be used in the frequency domain analytical model has been proposed, which address the problem that models using detailed physical parameters such as the frequency-dependant model are difficult to be applied to analytical models. This method enables the lumped parameter model to accurately reflect the frequency-domain characteristics within a certain frequency range required for research while at the same time, the simplification makes it suitable for application in analytical models.

Through impedance measurement and comparison, it has been found that the different time-domain modelling methods of MMC have no significant effect on the impedance of the MMC providing the inject disturbance is sufficiently large to mitigate the generated harmonics due to the use of a low number of SM in the switching function model. Since a large number of frequency-domain analysis for MMC are based on the averaged model, this conclusion provides a theoretical basis for the frequency-domain MMC modelling research.

Chapter 6 General conclusions and future work

6.1 General conclusions

The main purpose of this research work is to develop and validate detailed and accurate offline and real-time RTDS models of MMC and DC grids. Such models deliver a useful platform for a variety of offline and real-time studies to be carried out with good accuracy for real-time implementation without relying on external FPGAs.

In this thesis, detailed switching, switching function, Thevenin equivalent and averaged models of HB-MMC have been discussed including the theoretical basis that underpins each modelling method, and basic assumptions made in the development of each method. The aforementioned HB-MMC models were developed and validated by comparing the results of PSCAD offline simulation models (switching function, averaged and Thevenin equivalent MMC models) first, considering steady-steady operation, AC and DC short circuit faults. Then, simulation efficiencies of different HB-MMC models were compared. The comprehensive comparison of the offline simulation waveforms proves that the averaged and switching function HB-MMC models produce largely identical results as those from the Thevenin equivalent MMC model in the PSCAD MMC library, but with much greater simulation efficiency. This conclusion is valid for a wide range of studies, including normal steady-state operation and faults. Similar voltage and current stresses are observed on the MMC active and passive components. As a follow up of the extensive offline validations of a number of MMC models, the detailed validations of user-defined real-time HB-MMC switching function and averaged MMC models developed in RSCAD against the offline PSCAD MMC switching function models were presented, which shows good agreement between the offline and real-time simulation waveforms during normal operation, symmetrical and asymmetrical AC faults, and DC faults.

Switching function model and averaged model of FB and hybrid MMCs have been developed and implemented in RTDS as user-defined real-time models. These models

were validated against offline PSCAD FB and hybrid MMC models. Results of the comprehensive comparisons of the simulation waveforms show that the offline and real-time simulation waveforms are in full agreement during normal operation and various AC and DC faults conditions. The developed models can be used for a variety of system studies with high computational efficiency and accuracy in examining the enhanced control and operation provided by FB and hybrid MMCs. Based on the user-defined real-time HB, FB and hybrid MMC models, a summary of detailed quantitative study that assesses the interoperability of different converter topologies that operate side-by-side in a multi-terminal DC grid closely resembling the Caithness-Morey-Shetland HVDC system was presented. Detailed examinations of the presented results reveal that both models being compared produce practically identical results during normal and abnormal conditions.

Impedance measurement of a simplified GB AC network model and MMC has been performed. The method of impedance extraction in time-domain and the impedance-based stability analysis were described. The effects of AC cable and MMC time-domain modelling methods on the impedances were studied. The results of the impedance measurement show that the AC cable connected to the converter has a significant impact on the AC grid impedance. There is potential resonance in AC network impedance with a long cable and the longer the AC cable, the lower the resultant resonance frequency of the AC system. When the length reaches a certain level, the resonance frequency of the AC system falls in the typical frequency ranges of MMC converter responses and potentially this can significantly impact on system stability. In order to accurately reflect the resonance point introduced by the cable, a lumped parameter model optimization method that can be used in the frequency domain analytical model was proposed, which address the problem that models using detailed physical parameters such as the frequency-dependent cable model are difficult to be applied to analytical models. This method enables the lumped parameter model to accurately reflect the frequency-domain characteristics within a certain frequency range required for study while at the same time, the simplification makes it suitable for application in analytical models. Through impedance measurement and comparison, it has been found that the different time-domain modelling methods of MMC have no significant effect on the impedance of the

MMC providing the inject disturbance is sufficiently large to mitigate the generated harmonics due to the use of a low number of SMs in the switching function model. Since most frequency-domain analysis for MMC is based on the averaged model, this conclusion provides a theoretical basis for the frequency-domain MMC modelling research.

6.2 Author's contributions

The thesis contains the following main contributions:

- Detailed submodule (SM) level half-bridge (HB), full-bridge (FB) and hybrid MMC models with adjustable number of SMs per arm and generic and customized control functions are developed and validated. The developed MMC models can facilitate testing of MMC control and protection solutions in offline and real-time, offer the users the means to investigate further potential performance improvement and use as a strong basis for explorations of multi-vendor schemes. The developed models are introduced as open-access MMC models by the National HVDC Centre and available to download at www.hvdccentre.com/projects/open-access-converter-models/ . The developed models have been used in a number of projects by the National HVDC Centre.
- Offline and real-time three-terminal DC grid models closely resembling the Caithness-Morey-Shetland HVDC system are developed to investigate DC grid power flow control during steady-state and AC faults. Interoperability of different MMC topologies in a DC grid is assessed quantitatively using offline PSCAD and real-time RSCAD simulations. The models provide platforms for further investigation into DC grid operations with different DC voltage control and power dispatch strategies, the interaction of AC and DC grids including voltage and/or frequency stability, system protection, integration of renewables etc.
- Development of a RSCAD frequency measurement tool to extract impedances of an MMC and connected AC network for stability assessment. The scenario of GB AC network connected to an MMC is provided in RSCAD for RTDS based real-time simulation use. Focusing on the grid-connected converter system, how do the AC cable and MMC time-domain models affect the impedance has been explored.

6.3 Suggestions for future research

Potential areas for future research include:

- The developed lumped parameter HVAC cable model has only been validated against the frequency-dependent cable model in the frequency range of 1-300Hz. The higher frequency range can be considered for optimization of lumped parameter cable model.
- Investigate the impact of different SM capacitor voltage balancing strategies on the internal harmonics and output impedance of the MMC.
- Optimize the impedance extraction process for shorter injecting time by applying different perturbation voltage injection methods, for example, maximum-length binary sequence (MLBS) signal.
- Investigate the development of RTDS MMC models in hardware-in-the-loop test with MMC assigned in RTDS processor and part of the control system implemented in hardware.
- Implement the MMC models in FPGA devices for real-time simulation.
- Investigate the impact of different voltage balancing strategies on the time-domain simulation efficiency and MMC output impedance.
- Optimize the fault validation with protection system considered.

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Appendix: List of publications and reports

The list of publications based on this thesis is as follows:

- D. Guo, M. Rahman, G. P. Adam, L. Xu, A. Emhemed, G. Burt, Y. Audichya, "Detailed quantitative comparison of half-bridge modular multilevel converter modelling methods," in *The Journal of Engineering*, vol. 2019, no. 16, pp. 1292-1298, 3 2019.

  Abstract:

  This paper presents a detailed comparison of different modelling methods of the half-bridge modular multilevel converter (HB-MMC), namely, switching function, Thevenin equivalent, and averaged, considering both MMC implementations (large and reduced number of cells). The theoretical basis that underpins each modelling method are discussed. Offline PSCAD simulations are used to validate user-defined switching function and averaged MMC models against the Thevenin equivalent model provided in PSCAD library for accuracy, considering steady-state and DC fault conditions. Furthermore, the RTDS based real-time simulation results of the user-defined HB-MMC switching function model are validated against the above mentioned offline models, considering steady-state and DC short circuit fault operations. Simulation speed and efficiency of different offline HB-MMC models being studied here are compared. From comprehensive corroboration of different HB-MMC models presented here, it has been found that the averaged, switching function and Thevenin equivalent models produce practically identical results during steady-state and DC faults. In detailed offline and real-time simulation studies where fundamental and harmonic dynamics are of interest, switching function model is found to be faster and computational efficient compared to the Thevenin equivalent model.

- D. Guo, M. Rahman, G. P. Adam, L. Xu, A. Emhemed, G. Burt, Y. Audichya, "Interoperability of different voltage source converter topologies in HVDC grids," *15th IET International Conference on AC and DC Power Transmission (ACDC 2019)*, Coventry, UK, 2019, pp. 1-6.

  Abstract:

  This paper presents a detailed study of DC grid operation using a range of user-defined offline and real-time HVDC converter models which were rigorously validated against offline and real-time benchmarks. Provided that these models are destined for use in real-time hardware in the loop simulation and a wide range of offline system studies, this paper assesses their suitability for studying complex DC grids that consist of multiple voltage source converters which differ in their control range and fault ride-through capabilities. Detailed quantitative studies show that the offline and real-time DC grid models produce well matched results and provide efficient approaches to investigate DC grid operation during normal condition and AC and DC faults.

- R. Li, L. Xu and D. Guo, "Accelerated switching function model of hybrid MMCs for HVDC system simulation," in *IET Power Electronics*, vol. 10, no. 15, pp. 2199-2207, 15 12 2017.

  Abstract:

  An accelerated switching function model (SFM) of the hybrid modular multilevel converter comprising both full-bridge (FB) and half-bridge (HB) submodules (SMs) in each arm is presented for HVDC system simulation, where auxiliary circuits are adopted to represent all possible current paths during normal and fault conditions. The proposed SFM can represent the negative voltage generating capability of the FB SMs and the equivalent switching functions in the blocking states of the FB and HB SMs are also introduced in the proposed model to accurately replicate the potential charging of the SM capacitors, yielding improved simulation accuracy compared to other alternatives. In addition to the faster simulation speed, the proposed model accurately reproduces the converter behaviour during various operating conditions, including normal operation, AC

fault, DC fault and so on. The proposed SFMs are assessed in MATLAB/Simulink environment using both down- and full-scale HVDC links and the simulation results confirm the validity of the proposed model in terms of model accuracy and improved simulation speed.

- M. Rahman, D. Guo, G. Adam and A. Emhemed, "Converter and GB network modelling Report I: Development and Validation of Offline and Real-time User-defined Models of Alternative MMC Configurations," April 2018, the National HVDC Centre [Online]. Available: http://www.hvdccentre.com/open-source-converters/, [Accessed 29 March. 2020].

- D. Guo, M. Rahman, G. Adam and A. Emhemed, "Converter and GB network modelling Report II: Validation of Real-time User-defined MMC Models," Agust 2018, the National HVDC Centre [Online]. Available: http://www.hvdccentre.com/open-source-converters/, [Accessed 29 March. 2020].

- D. Guo, M. Rahman, G. Adam and A. Emhemed, "Converter and GB network modelling Report III: Offline DC grid model development," September 2018, the National HVDC Centre [Online]. Available: http://www.hvdccentre.com/open-source-converters/, [Accessed 29 March. 2020].

- D. Guo, M. Rahman, G. Adam and A. Emhemed, "Converter and GB network modelling Report IV: Development and Validation of Offline and Real-time User-defined Models of Alternative MMC Configurations," September 2018, the National HVDC Centre [Online]. Available: http://www.hvdccentre.com/open-source-converters/, [Accessed 29 March. 2020].

- D. Guo, M. Rahman, G. Adam and A. Emhemed, "Converter and GB network modelling Report V: DC Grid with User-defined Converter Models: Validation of Real-Time Model in RTDS against Offline Equivalents in PSCAD/EMTDC Environment," October 2018, the National HVDC Centre [Online]. Available: http://www.hvdccentre.com/open-source-converters/, [Accessed 29 March. 2020].

- D. Guo, Y. Chen, A. Egea and G. Amico, “Stability Assessment and Mitigation HVDC Converter Interactions Report I: Development and Validation of MMC Converter Impedance Models,” October 2019, the National HVDC Centre.
- D. Guo, Y. Chen and L. Xu, “Stability Assessment and Mitigation HVDC Converter Interactions Report II: Development of Typical AC Network Configuration for Converter Interaction Study,” Feburary 2020, the National HVDC Centre.