

**Novel methods for enhancing
accuracy and stability of Power
Hardware-In-the-Loop simulations**

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Declaration

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Abstract

Novel methods for the interface between the simulation and hardware of Power Hardware-In-the-Loop (PHIL) configurations have been analysed, developed and experimentally evaluated in this thesis, for enhancing the applicability of PHIL simulations, increasing its stability and accuracy performance.

Time delay is proven to be a critical limiting factor for PHIL simulations. Appropriately, a characterisation methodology for the time delay present within PHIL has been established, by which individual identification of time delay sources as well as time delay dynamics within the different components are reviewed. As a result, variable time delay has been identified within these configurations and mitigation techniques for the time delay and its variability are presented.

Furthermore, a time delay compensation scheme using Sliding Discrete Fourier Transform (SDFT) is demonstrated experimentally to improve the accuracy and stability of PHIL, even when harmonic components are present.

Detailed stability analysis of PHIL simulations performed provides clarification on the stability conditions of Ideal Transformer Method (ITM) Interface Algorithms (IAs). Additional improvements to PHIL IAs have been evaluated, with novel adaptive IAs established to provide enhanced stability.

Finally, enhancement of applicability of PHIL simulations is also experimentally proven with the implementation of an initialization process to a large scale power system application, in which the time delay compensation algorithm is also integrated.

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Glossary of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
APF	Active Power Filter
CHIL	Controller Hardware In the Loop
DAC	Digital to Analog Converter
DC	Direct Current
DER	Distributed Energy Resource
DFT	Discrete Fourier Transform
DIM	Damping Impedance Method
DPSL	Dynamic Power System Laboratory
DRTS	Digital Real Time Simulation
ESAC	Energy Source Analysis Consortium
ETYS	Electricity Ten Year Statement
FFT	Fast Fourier Transform

GB	Great Britain
GMPM	Gain Margin Phase Margin
GPS	Global Positioning System
GTAI	Giga-Transceiver Analog Input
GTAO	Giga-Transceiver Analog Output
HIL	Hardware In the Loop
HUT	Hardware Under Test
I-ITM	Current Ideal Transformer Method
I/O	Input/Output
IA	Interface Algorithm
IP	Intellectual Property
ITM	Ideal Transformer Method
LHP	Left Half Plane
MAF	Moving Average Filter
NETS	National Electricity Transmission System
PCC	Point of Common Coupling
PCD	Partial Circuit Duplication
PHIL	Power Hardware In the Loop
PI	Power Interface
PMU	Phasor Measurement Unit

PV	PhotoVoltaic
PWM	Pulse-Width Modulation
RES	Renewable Energy Source
RHP	Right Half Plane
RMS	Root Mean Square
RMSE	Root Mean Square Error
ROS	Rest Of the System
RTDS	Real Time Digital Simulator
SDFT	Sliding Discrete Fourier Transform
TSO	Transmission System Operator
V-ITM	Voltage Ideal Transformer Method
WAMPAC	Wide Area Monitoring Protection And Control
ZOH	Zero Order Hold

Chapter 1

Introduction

Electric power systems can be operated in different manners, there exist AC (alternated current) operated systems, DC (direct current) and even hybrid systems where a mix of AC and DC is used. Such systems usually involve a variety of voltage levels and characteristics but they share a common aspect, all the devices within a power system are interconnected together by the use of transformers, converters, transmission lines, etc. Consequently, all of them influence the power system behaviour and operation, causing difficulties to understand complex power system interactions in its totality [KSE15].

The complexity of modern power systems is gradually increasing with the introduction of novel power components such as Distributed Energy Resources (DERs), Renewable Energy Sources (RES) or novel transformer or substation systems that are changing conventional power system dynamics [Dir17; The13; Bel15; Tat+13; KSE15]. The integration of such components requires the modification or development of current technology already installed such as instrumentation and control devices, challenging the reliability of the entire power system [Agu+17; ZSY14; DCW17; Mom+14; He+13].

This refers not only to land-based power systems, but also to marine, aeronautical or micro-grid electric systems with high penetration of power converters and complex devices that have an impact on power system dynamics [SVM16; Kim+15; He+13; SM15].

The design and development of power system components are usually performed through computer analysis and simulation [Mon+07a]. The integration of these components and their impact in the power system need to be assessed, this could be performed experimentally with real hardware but this implies a very high risk and cost that companies are not willing to take along with a lack of flexibility to perform a large variety of test scenarios; therefore, offline simulation is commonly used for this purpose [Kot+15]. However, simulation studies introduce a number of concerns:

- A complete simulation of the power system is very difficult to achieve due to its complexity and the limitations of the software tools and computers.
- Usually there is a number of different proprietary software for the existing devices in the network that rarely will be available on its entirety [BT10; KSE15].
- Interaction between developed device simulation models and power system may not be accurately included on detailed device models developed by manufacturers [KSE15].

These obstacles are increasing the concern on testing methodologies for power system components as previous techniques (only simulation or pure hardware) are no longer affordable (in terms of time and cost) or accurate enough. As a consequence, significant effort has been performed during the last few years in the development of computer capabilities for the simulation of detailed electrical power systems in real-time [FS15], enabling the study and application of different testing procedures that are able to address the increased need for accurate testing of electrical components, improving the accuracy, cost and risk of traditional test procedures [Bla+16; Pal+17; VDC17]

The first step towards the development of new testing procedures for power components was demonstrated with the development of Hardware-in-the-Loop (HIL) simulation technique, which is able to merge the two traditional testing procedures (pure simulation and hardware) by interfacing the software simulation with the real hardware under test.

For the purpose of facilitating the assessment of the integration of complex devices or devices with unavailable proprietary software (e.g. for controllers), HIL simulation technique presents promising characteristics. This approach allows for external hardware components to be coupled with a simulated system running in real-time. Real-time simulation is needed for HIL test-beds as hardware components are coupled to the simulation, which require of a real-time exchange of information [Pal+17].

Depending on the testing scenario, a power system simulation model will have to be developed in a real-time simulation platform. These platforms can present limitations in terms of computational power, consequently the size and fidelity of the models can be limited. However, typically the power system model will try to capture the main dynamics of the system and the interactions with other components in order to provide a representative model for the hardware under test (HUT) to be accurately tested [BT10]. The behaviour of the real device within its proposed environment can be explored under relative safety conditions with minimal risk of damage to the actual hardware. The proposed environment and test scenarios can be expanded from normal conditions to include extreme events which may be difficult or dangerous to recreate in reality, but which represent events during which the device should maintain stable operation.

1.1 Research context

HIL simulations enable the implementation of very detailed and exact hardware components in a laboratory environment for its testing and development. Commonly

HIL simulations are separated into two different categories, Controller-HIL (CHIL) and Power-HIL (PHIL), depending on the type of interface required for coupling the simulated system with the Hardware Under Test (HUT) [Ngu+18]. The interface is selected in accordance with the type of HUT to be tested. More precisely, these testing methodologies are defined as:

1. *CHIL*

The exchange of information between the simulated Rest Of the System (ROS) and the hardware component is only composed by control signals and accordingly the hardware being coupled is usually "secondary" power system components such as instrumentation or controllers that only require of a low voltage and low power signal to be transmitted between them, hence the reason why sometimes this is also known as secondary HIL. However, since just low level signals are exchanged between the software simulation and the HUT, this procedure is not valid for power components such as motors, generators or power converters that require higher levels of power to be exchanged.

2. *PHIL*

When the HUT requires the exchange of higher level power signals to operate, a Power Interface (PI) is required to sit between the simulated ROS and the HUT. The PI converts the low voltage/power signals of the Digital Real-Time Simulator (DRTS) into high voltage/power signals as well as provides electrical coupling between both subsystems. The HUT responds to the PI amplified signal (current or voltage), and the measurement of this response is fed back (by the power interface or an external measurement unit) to the DRTS, closing the loop as shown in Fig. 1.1.

For developers of devices, CHIL allows them to prove and de-risk the performance and design of instrumentation and control systems in a safe and inexpensive test bed. When primary hardware prototypes are added in a PHIL environment, their entire

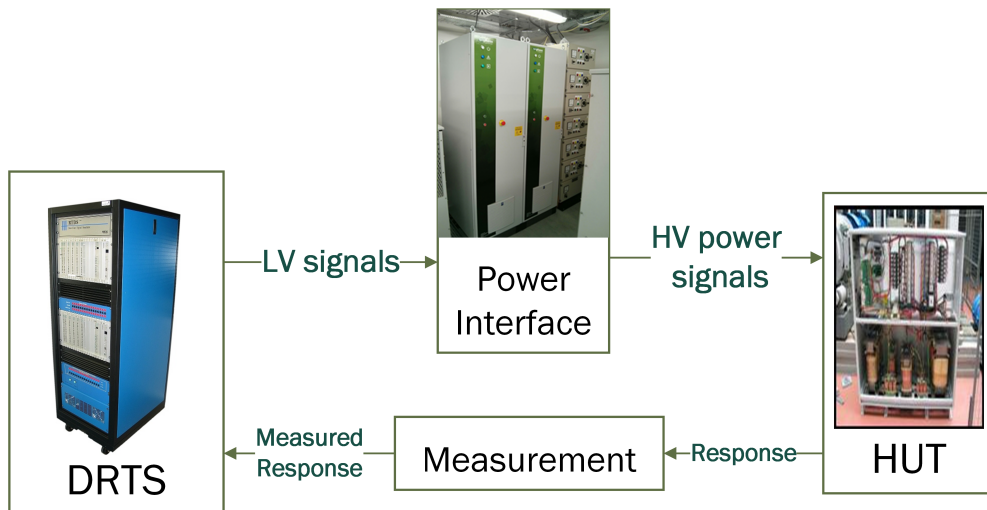


Fig. 1.1 PHIL simple structure

design (not only instrumentation and control) can also be de-risked [Edr+15]. However, detailed power system models of the network to which developed devices may be connected (the simulated part) may not be available. Indeed, often there is no single specific network, or if there is a specific network, its details may be proprietary or not fully understood accurately. The important aspect is for the designers to subject the device to a wide range of simulated scenarios which cover the full and worst-case range of conditions that the hardware might encounter during its lifetime [RGB16; KKK17].

HIL techniques allow power system network owners to create reasonably accurate models of their networks in simulation, since they will have access to the network design data. Then, they can place manufacturer-supplied controllers or primary hardware connected to their simulated systems. The network owner will rarely have access to the proprietary software contained inside the manufacturer device, so it is generally not possible to model the combined system entirely in simulation [BT10]. However, the manufacturer device can be supplied as a boxed unit and the Intellectual Property (IP) protected. The network owner can then run tests and assess the performance of the device within its specific network environment, thereby de-risking the deployment of the real product on their network [RGB16].

However, the implementation of PHIL also presents a number of challenges mainly due to the fact that the system is composed of two subsystems (the simulation and the HUT) which are now interconnected by means of a power interface, which is not part of the original system [Mon+07b]. The addition of the PI in pursuance to achieving higher power levels does imply some challenges, as the interface is not part of the original system and therefore it can modify the dynamic behaviour of the system under test, affecting the accuracy and stability of the simulation [Lau+16].

The main challenges associated with PHIL simulations which are investigated in this thesis are:

1. Time delay: The communication required between the simulation, the power interface and the measurement of the HUT response, introduces a loop delay that can affect to the accuracy and stability of PHIL simulations [Gui+14; GRB15; Jon11; RSW07]. Therefore, the loop delay needs to be clearly understood, identified and mitigated when possible for the achievement of safe and accurate PHIL testing.
2. Stability: The interface algorithms, which are responsible of the electrical coupling between the simulation and the HUT, together with the partition of the power system in two subsystems, are decisive elements for the stability of PHIL simulations [RSB08]. The stability of PHIL simulations must be ensured before the testing starts, as real equipment is being tested.
3. Accuracy: The accuracy of PHIL depends mainly on: the accuracy of the PI, the precision of the communication channel, the sensors used for the measurements and the interface algorithm used [Leh+12]. Furthermore, the total time delay of the PHIL configuration will play a major role in the accuracy of the results [GRB15]. In order to validate novel power system components and their interaction the results must be accurate.

4. Initialisation of PHIL simulation: The simulation and hardware need to be initialised and achieve steady-state in a controlled manner, before the testing of dynamic scenarios is initiated. This condition is unlike a simulation-only environment where various techniques can be used to pre-configure states and integrators so that the simulation begins at steady-state. In the HIL environment, the device designer will be forced to anticipate through the startup, initialisation, and other sequences that are imperative to get the device working from a “cold start” [Gui+18].

1.2 Research contribution

The main contributions from this thesis are summarized as:

- Realization and implementation of a novel method to accurately characterize the time delay of PHIL implementations, which provides a far more comprehensive and detailed analysis than previous approaches. Accordingly, stability and accuracy of PHIL implementations can now be accurately assessed, reducing the risk and uncertainties.
- Identification of variability in time delay within PHIL simulations, along with an analysis of the impact of the variability in PHIL stability and accuracy. Furthermore, the dynamics of the time delay variability has been integrated within the characterization method.
- Development of a method for mitigating variable delays with the introduction of an optimization algorithm for the simulation time step, aiming at the reduction of the noise of the signals on the implementation and consequently on improving the accuracy of PHIL.

- Design, analysis and validation of a new method for the compensation of time delay in PHIL implementations, which is based on phase-shifting of the phasors in a phase-by-phase and harmonic-by-harmonic manner. Hereby, PHIL simulations are now capable of accurately reproducing the existing power exchanges between simulation and hardware during steady-state conditions.
- PHIL stability analysis for ensuring a correct interpretation of the stability conditions is always achieved, avoiding misleading stability assessments.
- Development and analysis of a novel adaptive interface algorithm to cope with interface algorithms limitations, more precisely to improve the stability performance of PHIL simulations.
- Development and evaluation of a novel virtual shifting impedance method based on the stability requirements of PHIL simulations. By virtually shifting the impedance, this method accomplishes to avoid the physical shifting of components to achieve stability, increasing the applicability of the method.
- Simultaneous implementation of virtual shifting impedance method alongside the time delay compensation method, which leads to an enhanced stability performance.
- Establishment of an initialization approach for PHIL simulations to solve the limitations that the testing of power components or systems, which are not able to initialize without the other subsystem being initially connected, were bringing to PHIL simulations.

1.3 Thesis structure

The structure adopted for the completion of this thesis is presented below.

Chapter 2 introduces the main challenges existent within PHIL simulations that the contributions within this thesis aims to solve. Chapter 3 demonstrates the presence of a variable time delay in PHIL simulations and also proposes a time delay characterization approach for such implementations. Chapter 4 proposes a novel time delay compensation algorithm for the improvement of accuracy and stability of PHIL simulations. Chapter 5 presents two novel interface algorithm developments along with a detailed stability assessment of their implementation within a PHIL simulation. Chapter 6 illustrates an initialization approach for the implementation of PHIL simulations in a larger variety of applications. Finally, chapter 7 collects the conclusions and summarises the contributions from this thesis, further work identified from the results of this thesis is also presented.

1.4 List of publications

The publications which have resulted from the work completed in this thesis are:

E. Guillo-Sansano, M. H. Syed, A. J. Roscoe, G. M. Burt, F. Coffele, “Time Delay Characterization for the Improvement of Power Hardware-in-the-Loop Simulations,” *IEEE Transactions on Industrial Electronics* (under review).

Y. Wang, Y. Xu, Y. Tang, K. Liao, M. H. Syed, **E. Guillo-Sansano**, G. Burt, (in press) “Aggregated Energy Storage for Power System Frequency Control: A Finite-Time Consensus Approach,” in *IEEE Transactions on Smart Grid*.

E. Guillo-Sansano, M. H. Syed, A. J. Roscoe, G. M. Burt, “Initialization and Synchronization of Power Hardware-In-The-Loop Simulations: A Great Britain Network Case Study.” *Energies* 2018, 11, 1087.

V. H. Nguyen, Y. Besanger, Q. T. Tran, T. L. Nguyen, C. Boudinet, R. Brandl, F. Marten, A. Markou, P. Kotsampopoulos, A. A. van der Meer, **E. Guillo-Sansano**, G. Lauss, T. I.

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Chapter 2

Power Hardware in the Loop

Challenges

The main challenges that arise from a PHIL implementation are due to the fact that the test system is divided into two subsystems: i) a simulated system in real-time and ii) the HUT, both required to be interconnected by means of a power interface. The interface is a non-ideal component that is added to the test system modifying its characteristics. The main challenges for PHIL are therefore introduced by the interface, which challenges the stability and accuracy of the simulations [Ngu+18; Jon11; RSW07]. The effects that the complete interface is bringing into the test system need to be clearly analysed and understood in order to find a solution that approximates the behaviour and results of the PHIL simulation as much as possible to an ideal pure hardware testing scenario, achieving accurate and stable PHIL simulations for any test scenario.

Thus, the elements that compose the interface for PHIL simulations are required to be identified, these are:

1. Physical components: DRTS, power amplifier and the communication interface.
2. Interconnection attributes: interface algorithm and time delay.

Accordingly, the main features of the elements that form the interface of PHIL simulations are introduced in this section for an initial analysis of the challenges associated to each element.

Additionally, initialization challenges of PHIL simulations are also introduced in this chapter, as it can also bring limitations into the applicability of the PHIL simulations. This is mainly due to the stability of each subsystem, which may be dependant on its interconnection with the other subsystem, leading into a challenging initialization procedure.

2.1 Digital real-time simulation

In [Far+15], DRTS of electric power systems is defined as “the reproduction of output (voltage/currents) waveforms, with the desired accuracy, that are representative of the behaviour of the real power system being modeled”. Furthermore, detailed description of the hardware and software that comprises a DRTS (such as processors, solvers, modelling tools, communication interfaces) are also reported in [Far+15].

The main feature of DRTSs utilized for PHIL simulations is their use of fixed time-step solvers for providing real-time operation. However, this necessary condition also brings limitations in terms of the simulated models size and level of detail that can be used. This is due to the requirement of performing all the calculations for the simulated model within the assigned time-step and for every time-step during the complete simulation duration, otherwise unstable or unreliable performance can be achieved [Lan+13; Lau+16].

Accordingly, the time-step of the DRTS needs to be selected in accordance with the complexity of the simulated model and the maximum bandwidth required for the model to be accurate (of importance when simulation of power electronic components is required).

2.2 Power amplifier

Three different power amplifier types are typically used for PHIL simulations: linear, switched-mode and synchronous generator type amplifiers. A comparison between them and a discussion on their impact on PHIL simulation has been presented in [Leh+12]. When the power amplifiers are used for interfacing purposes, such as when used for PHIL applications, it can be also identified as the power interface (PI).

- Linear amplifiers are composed of transistors operating in the linear region, which present a very high dynamic performance with a short time delay [Leh+12; VLF11; Kot+15]. However, their cost and large losses typically limit their use for high power levels. These power amplifiers have been used for the testing and validation of power components and systems with PHIL simulation in [Leh+12; VLF11; Kot+15; NW15; Mar+17].
- In the other hand, switched-mode amplifiers are typically preferred for high power applications as their efficiency and flexibility is greater, although a larger time delay and slower dynamics exist typically in this case [Leh+12; Ste+10]. In [KGW17; JMJ15; Ben+11; Dar+14; SLS13], the design, development, control, and commissioning of switched-mode amplifiers of different power levels (kVA up to MVA) have been presented. Also, in [Dav18; MKB18] an analysis of the dynamics of this amplifier type is presented along with stability studies.
- The use of synchronous generator type amplifiers for PHIL applications is limited due to the slow response of the generators and a lack of flexibility for applications with unbalances and fast dynamics [Leh+12; Ros+10; Ros+11b].

Both linear and switched-mode amplifiers are typically characterised as a time delay and a second order transfer function (commonly that of a low pass filter) [Ren07]. This function reduces the gain of the higher frequency components, assisting to improve the

stability performance of PHIL simulations [Bra17]. However, actual power amplifier technology can reproduce a high number of harmonic components, therefore having a considerable high cut off frequency for the low-pass filter behaviour, allowing an accurate simulation for test systems where high frequency components are not involved. The dead-time of switched-mode amplifiers has been demonstrated to also have a slight impact into the stability as presented in [MKB18]. The time delay associated with the power amplifier is typically combined with other time delays of the PHIL configuration and is analysed in a separate section of this chapter.

2.3 Interface algorithms for PHIL

An interface can be defined as a shared boundary with information exchanges between the involved sections. For PHIL implementations the boundary is at the electrical Point of Common Coupling (PCC) of the HUT with the DRTS and the information exchanged are the voltages and currents. The specification of this interface for PHIL is defined as the Interface Algorithm (IA). This specification includes the type, quantity, and function of the interconnection circuits and the type and form of signals to be interchanged by these circuits [Edi00].

An analysis of different IAs proposed in the literature for PHIL simulations have been presented in [RSB08; Bra17]. From these analysis, the Ideal Transformer Method (ITM) and Damping Impedance Method (DIM) IAs are suggested as the most reliable ones for performing PHIL simulations in terms of stability and accuracy. This is in agreement with the large majority of PHIL simulations, which typically implement these IAs [Kot+12; Man+17; Lan+12; HTP17; LS18; Hok+18]

Therefore, only an introduction of these IA methods is presented here. Furthermore, a conventional stability assessment performance of the selected IAs is also presented.

2.3.1 ITM

This IA method was originally described in [Kuf+95], and later applied to PHIL in [RSB08], where two different types of interface were described depending on the signal being amplified, voltage-type ITM (V-ITM) when the voltage is the amplified signal and current-type ITM (I-ITM) when the current is amplified. Schematics of these two IAs are presented in Fig. 2.1, where Z_{DRTS} and Z_{HUT} represent the total impedance of the simulation and HUT respectively. T_{d1} and T_{d2} symbolize the time delay of the feed-forward and feedback path. H_{PI} is the power interface transfer function.

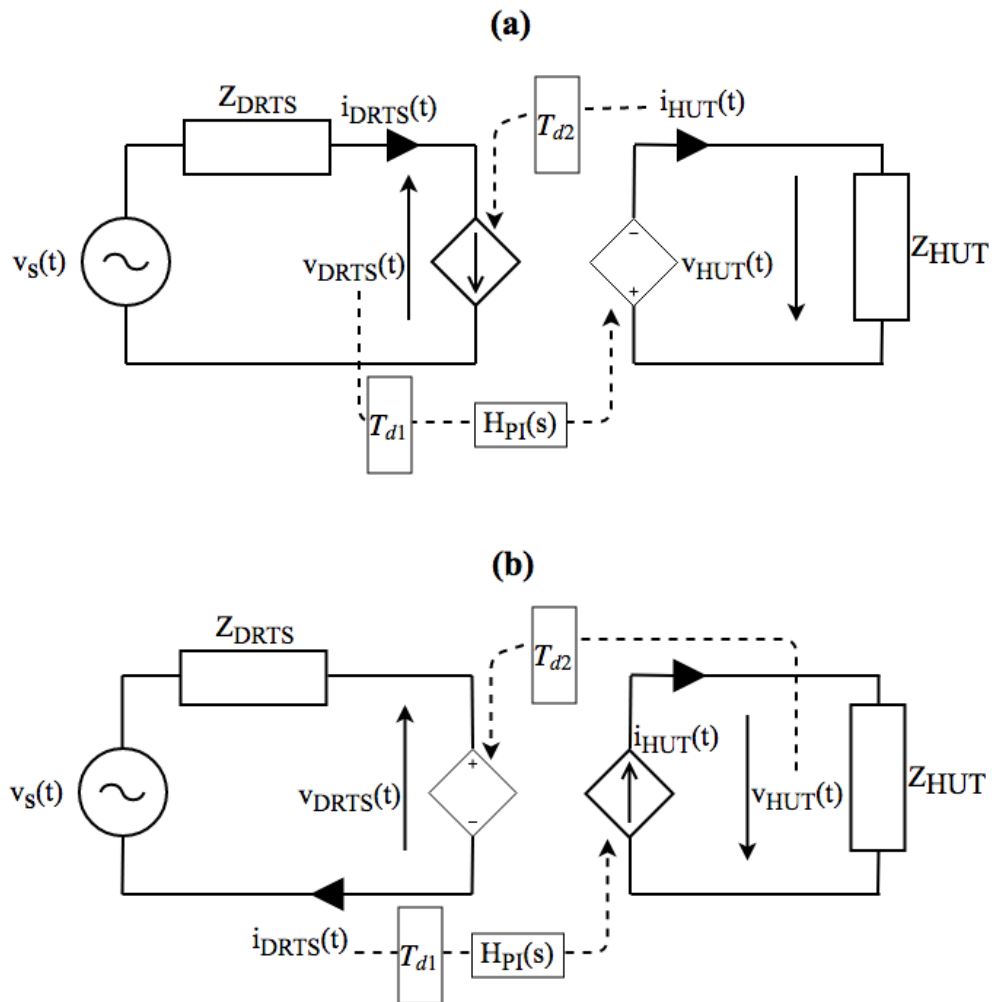


Fig. 2.1 Voltage and current type ITM IA

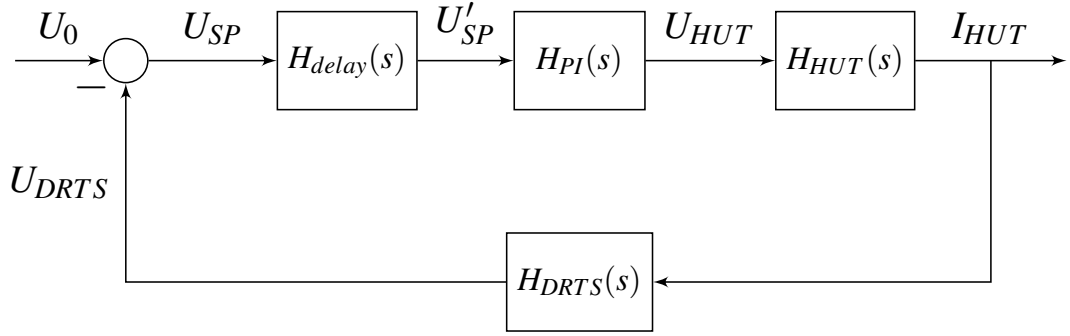


Fig. 2.2 PHIL control loop diagram.

The stability of PHIL simulations using ITM IA has been broadly discussed in the literature. Conventional stability assessments as presented in [RSB08; DGL14; Lau+11; Jon11; LLS12; HRM16; Edr+15; Bla+17; KKK17] conclude that the stability of ITM IA depends on the ratio of impedances, with some of them referring only to resistive impedances ratio [Lau+11; Jon11; KKK17] and others to impedance magnitude ratio [RSB08; DGL14; Edr+15; LLS12]. Therefore, according to these studies, to achieve a stable simulation under V-ITM (when the PI is assumed ideal, unity gain and zero time delay) the ratio of impedances must be $|Z_{HUT}(s)| > |Z_{DRTS}(s)|$. On the contrary, when I-ITM is implemented the condition is the opposite $|Z_{HUT}(s)| < |Z_{DRTS}(s)|$. These conditions are commonly established from an stability assessment of the open loop transfer function derived from the control diagram of Fig. 2.2 (for V-ITM in this case) where:

$$H_{HUT}(s) = \frac{I_{HUT}(s)}{U_{HUT}(s)} = \frac{1}{Z_{HUT}(s)} \quad (2.1)$$

$$H_{DRTS}(s) = \frac{U_{DRTS}(s)}{I_{HUT}(s)} = Z_{DRTS}(s) \quad (2.2)$$

$$H_{delay}(s) = e^{-sT_d} \quad (2.3)$$

where H_{delay} is the transfer function of the total delay of the PHIL simulation, and $T_d = T_{d1} + T_{d2}$ the total accumulated time delay. H_{HUT} is the HUT transfer function and H_{DRTS} the DRTS transfer function.

The open loop transfer function $H_{OL}(s)$, of the control loop presented in Fig. 2.2 can be represented as:

$$H_{OL}(s) = \frac{U_{DRTS}}{U_0} = H_{delay}(s) \cdot H_{PI}(s) \cdot H_{HUT}(s) \cdot H_{DRTS}(s) \quad (2.4)$$

With the power interface considered ideal, $H_{PI}(s)$ is equal to 1. This is typically considered as it does not negatively affect to the stability assessment [MKB18] due to its filtering behaviour, hence $H_{OL}(s)$ can be simplified as:

$$H_{OL_V-ITM}(s) = e^{-sT_d} \frac{Z_{DRTS}(s)}{Z_{HUT}(s)} \quad (2.5)$$

For fulfilling the Nyquist stability criterion, with e^{-sT_d} characterizing a phase reduction as the frequency increases, literature suggests the ratio $|Z_{DRTS}(s)|/|Z_{HUT}(s)|$ must be less than 1 in cases where $X_{DRTS} = 0$ and $X_{HUT} = 0$ for not encircling the point $(-1, 0)$ and achieve a stable simulation. Similar assessment of the stability can be performed for I-ITM, producing:

$$H_{OL_I-ITM}(s) = e^{-sT_d} \frac{Z_{HUT}(s)}{Z_{DRTS}(s)} \quad (2.6)$$

yielding the opposite condition to V-ITM, by which the ratio $|Z_{HUT}(s)|/|Z_{DRTS}(s)|$ must be less than 1.

2.3.2 Damping impedance method (DIM)

This IA has been presented in [RSB08] as a combination of ITM and Partial Circuit Duplication (PCD) IAs. A diagram with the topology of DIM IA is presented in 2.3, where Z^* represents the damping impedance, which for achieving an accurate simulation should be equal to Z_{HUT} . The open loop transfer function of this configuration has been presented in [RSB08; Bra17; KKK17] as:

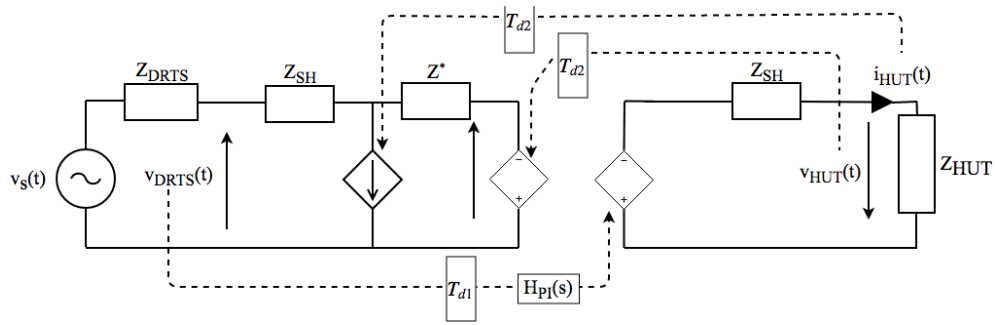


Fig. 2.3 Diagram of DIM IA

$$H_{OL_DIM}(s) = \frac{Z_{DRTS}(s)(Z_{HUT}(s) - Z^*(s))}{(Z_{HUT}(s) + Z_{SH}(s)(Z_{DRTS}(s) + Z_{SH}(s + Z^*(s))))} e^{-sT_d} \quad (2.7)$$

This IA would always be stable if $Z^* = Z_{HUT}$ as the numerator would be equal to zero; however, considerable knowledge of the HUT would be required for achieving such condition. With one of the purposes of PHIL simulations being the testing of proprietary equipment and black-box devices, this appears as an impractical interface. Nevertheless, online impedance identification of the HUT is complex but feasible as demonstrated in [Ric+17; PE13; Ric+16; RMM18; LRM16; SS14], although practically large window periods are required, for example $100ms$ is used in [Ric+17], which can risk the accuracy and stability of the simulation as the impedance will need to be modified in real-time as the HUT varies. When harmonic components and non-linear loads are present, accurate impedance identification becomes very challenging [Ric+17]. Furthermore, DIM IAs typically requires of a linking impedance which can affect to the dynamics of the system under test.

This method can therefore be limited by high penetration of converter connected generation, along with the increase of non-linear apparatus that will bring an increase in the effect of harmonic components as well as faster dynamics into future power systems. As a result, most of the PHIL simulations for research and validation of

power components and systems are being performed with the ITM method due to its straightforward implementation as well as its good accuracy, although its stability performance is not optimal [Bla+17; Kot+15; GRB15].

Accordingly, the developments proposed in this thesis have been mainly implemented with ITM IA, although some of the developments are independent of the IA and could be applied for any of the presented IAs.

From the presented ITM algorithm characteristics, it can be concluded that it is important to improve the stability of ITM IAs without affecting the good accuracy performance that it provides. Consequently, a number of interface compensation methods for the improvement of ITM IAs have been presented in the literature:

- Filtering of the feedback current: a straightforward implementation presented in [Lau+11; Kot+12] in which the addition of a low pass filter in the current feedback path of the PHIL implementation provides an improvement of the stability by limiting the frequency bandwidth of the system. However, considerable time delay is introduced by the filter which reduces the accuracy of the ITM IA implementation.
- Addition of hardware inductance: in [Kot+15; Hon+09] the stability of inductor coupled systems is studied, resulting in an increased stability of the system when part of the simulation inductance is shifted from the simulation into the hardware for V-ITM IAs.
- Multi-rating interface: in this case the digitally simulated model is partitioned into subsystems with smaller time steps which can improve the stability as presented in [LLS12; LS18]. Still, this method requires of the limitation of the bandwidth through feedback filters which affects to the accuracy.

2.4 Time delay within PHIL

The total loop delay of PHIL simulations affects the stability of the simulation, but it is often overlooked due to the importance of the IA, mainly the relationship between impedances at both sides of the interface for achieving a stable simulation when using ITM or the accuracy of the impedance estimation when DIM is used [RSB08; Tre+17].

It has been concluded from different studies that the time delay has a big impact on the accuracy of the simulation and that it has to be reduced and compensated for an accurate implementation [HTP17; HRM16; YG12; GRB15; Li+18]. This is even more relevant when evaluation of harmonic components is to be performed, as the lag of harmonic phases will be larger than at the fundamental component.

The effects that the time delay introduces into the accuracy and stability of PHIL simulation can be summarize as:

- Time delay effect on accuracy of PHIL

The main accuracy aspect affected by the time delay is the phase difference introduced between the voltage and current at the simulation PCC, that consequently affects the apparent power factor of the HUT and hence the active and reactive power exchanges are inaccurate when compared with an ideal scenario [GRB15; Li+18; Ros+10]. If interaction of the harmonic components of the HUT are acknowledged as part of the PHIL simulation, their phase relationship will be even more altered by the time delay leading to low accuracy results [Gui+14; GRB15]. Voltage and current waveforms have to be measured at the PCC in the DRTS system for detecting the time delay introduced and the accuracy effect in the phase relationship between voltage and current. Accordingly, the time delay introduced in PHIL applications needs to be measured, reduced and compensated in order to have more accurate simulations.

- Time delay effect on stability of PHIL

Stability is a crucial element to consider before implementing a PHIL simulation since an unstable PHIL configuration could cause fatal damage to the HUT and PI, and hence stability studies are usually performed before the implementation of PHIL simulations [Jon11; Lau+16]. The IA plays an important role for studying the stability of PHIL simulations as each specific IA presents particular characteristics (different signals to be exchanged, electrical elements) and therefore depending on the IA selected the time delay can have different effects on the stability.

Most of the contributions on PHIL in the literature acknowledge that time delay is important [Kot+15; LLS12; Ren+11; Lau+11; Kot+12; Gui+14; Li+18; Zha+16], however a detailed study of time delay has not been performed yet. Such a study would help better understanding of the time delay and the PHIL configuration for reducing the latency to the minimum for an improved PHIL simulation. Appropriate understanding of the time delay and its effects will lead to a reduced risk for performing PHIL experiments and at the same time it can help to increase its accuracy by mitigating and reducing the delays. Hence, identification of the components and processes that introduce the delay seems as the first step towards a better understanding. However, previous work on PHIL simulations only focus on the total or average loop delay without detailing why is the time delay produced or how it can be reduced for improving dynamic and transient behaviours of PHIL simulations [Gui+14; RSW07; Li+18; Zha+16].

For the purpose of achieving a more accurate and stable implementation of PHIL simulations, a detailed study of the time delay introduced by the different PHIL components is required. This will allow for a recommended PHIL implementation practice for achieving reduced time delays. At the same time, it will facilitate the development of compensation techniques for the time delay, which are required for stable and accurate PHIL implementations.

2.4.1 Time delay compensation

In addition, for an accurate PHIL simulation, the identified time delay needs to be compensated. Different time delay compensation techniques have been presented in the literature, these are:

- Lead compensator: Lead compensation can be used for the idealization of non-ideal interface gain [Ren+11; PH17], nonetheless this method can significantly amplify high frequency components and its applicability for complex systems and when harmonic components are present is limited.
- Fast Fourier Transform (FFT) compensation: this method consists on phase-shifting the different frequency signals according to the time delay after an FFT has pre-processed the signals [RSW07], although the use of a fixed base frequency can impair the accuracy if the frequency changes. It compensates up to the 13th harmonic due to the large computational time required to process FFTs.
- Fundamental dq compensation: time delay of the fundamental component is compensated in this case by adding an additional phase term into the dq to abc coordinate transformation [Li+18; Zha+16]. Nevertheless, when unbalanced or very distorted signals are present its accuracy can be limited, besides in this case only fundamental components have been compensated.
- Synchronous generator control compensation: in [Ros+10] a phase advance introduced into the control of the synchronous generator provides the compensation of the fundamental frequency component.

However, the presented techniques may not be sufficiently accurate when more complex networks with non-linear components (producing harmonic components) are being tested. Therefore, the need of an optimized compensation technique which takes into account the dynamics of complex power systems is identified.

2.5 Communication interface

Traditionally, analog communication interfaces have been utilized for establishing the transmission of data between DRTS and power amplifier, and also between the measured response of the HUT and DRTS [GRB15; HTP17; Kot+15]. The use of analog communication links requires of digital to analog conversion at the DRTS due to the digital nature of the DRTS, besides when switched-mode power amplifiers are used an additional analog to digital conversion is required, as the implemented control of the power amplifier is typically performed with a digital controller. Similarly, for the return path of the HUT measurement, further analog to digital conversion is required for integrating the measurement within the digital simulator.

The operation of an analog communication link is accompanied by the introduction of noise and uncertainties through the digital to analog converters (DACs) and analog to digital converters (ADCs), which can present offset errors, gain errors and noise proceeding from quantization errors [Fer+15].

On the other hand, high-speed digital communication interfaces can also be utilized for PHIL simulations [KGW17; Jen17], optimizing the interface when digital devices (as the DRTS and the controller of the switched-mode power amplifier) are part of the configuration. This configuration is generally more accurate due to the absence of ADC and DACs, mitigating the noise and uncertainties typically introduced by those components. Also, minimal time delay will be introduced into PHIL simulations with the implementation of a digital communication interface [KGW17].

2.6 Initialization of PHIL simulations

Frequently, PHIL simulations are carried out for the testing of single devices or where the HUT represents a relatively small part of the network in comparison with the simu-

lated rest of the system at the DRTS [Lan+12; Nae+15; Kot+13; PH17]. Nevertheless, this balance in PHIL between hardware and software is insufficient for other scenarios such as the validation of wide area monitoring, protection and control (WAMPAC) systems (an area of increasing interest given recent advancements in phasor measurement units (PMU) [ZCN11]) or distributed HIL simulations [Ste+17b; Lun+17; Cal+18]. In these cases, the different subsystems will be of variable size and importance, not just a simple power component but a portion of a power system, which may be required for the stable operation of the complete system. The HUT subsystem connected to the simulation subsystem can represent generation or load components, consisting of many devices interconnected or just a simple significant device. The conventional approach for setting up a particular PHIL simulation involves the following steps:

- The power network within the DRTS is initialized, achieving steady-state.
- Interface signals from the initialized DRTS simulation are then amplified by the power interface.
- The HUT response to the reproduced signal is measured and fed back to the DRTS for closing the loop, coupling both subsystems electrically.

For power systems studies, the load and generation conditions along with the power transfer at points of interest are selected from known scenarios [Gui+18]. This allows for testing under known stress conditions of the network or particular scenarios of interest. For example, a previously measured pre-fault condition of the network may be considered, where a novel control algorithm can be tested in order to evaluate if its implementation could have improved the response to the event. Accordingly, when PHIL simulations are initialized and the loop is closed, it is important to ensure that the conditions at all the buses of the test network (including the HUT terminals) are equivalent to the initial expected ones.

When the HUT is relatively small compared to the DRTS simulated power system [Lan+12; Nae+15; Kot+13], the DRTS simulation can be initialized without the HUT, hence the power system within the DRTS performs as a grid whose voltage and frequency are not dependent upon the HUT to be connected. Under these circumstances, the HUT is typically synchronized with the DRTS simulation by means of a simple switch, electrically coupling the HUT with the DRTS. Operation of the switch can introduce transient behaviours; however, when a stiff simulated grid or a modest HUT is present, the transient does not pose a significant risk for achieving a stable operating point at the start of the study. The initialization process as well as the electrical synchronization between the two subsystems (the closing of the loop) are thus relatively straightforward.

On the other hand, for cases where the network is not a stiff grid and the HUT is significant for the grid (either to be capable to initialize without it, or to remain stable if it is directly connected) an initialization procedure for the simulated part of the system including a reliable synchronization procedure is required.

Chapter 3

Time delay characterization and mitigation of delay variability for PHIL simulations

The time delay present in PHIL implementations is one of the important factors affecting stability and accuracy, therefore it is essential to identify and analyse time delay sources and their impact in a PHIL implementation. Accordingly, the first step towards the assessment of the time delay is to identify the components and processes that introduce time delay throughout the PHIL simulation loop. Then, an analysis of the interaction between the delays introduced by the different components is required. When the time delay sources and interactions have been identified, accurate characterization of the time delay is possible.

With the time delay source identification and the analysis of the interactions between the delays, variability in time delay due to the interaction of different fixed time steps from the components typically involved in the PHIL process has been identified, and its significance on stability and accuracy is studied in this chapter.

Appropriate understanding of the time delay and its effect leads to reduced risk of instabilities and inaccuracies when performing PHIL experiments and at the same time it can help to increase its accuracy by mitigating and reducing the delays.

Therefore, with the aim of providing a detailed characterization of time delays for PHIL simulations, this chapter contributions are as follows:

- A detailed analysis of time delays associated with PHIL simulations is undertaken to characterize the identified delays. Generic equations that characterize the time delay have been developed, allowing for an accurate analytical assessment of the time delay in PHIL setups.
- Contrary to the common assumption of a constant time delay, it is shown that time delay associated with a PHIL setup is typically variable.
- The impact of the identified variability in time delay on the stability and accuracy of PHIL setups is presented.
- Measures to mitigate the impact of the variability in time delay and ultimately eliminate it are proposed.
- The validity of the time delay characterization, the presence of variability in time delay and the measures proposed to mitigate or eliminate the variability are experimentally verified.

3.1 Conventional time delay characterization

Typically, PHIL simulations comprise three main components, (i) the DRTS that runs the simulation of the power system components, (ii) the PI for linking electrically the simulation with the hardware and (iii) the HUT. Conventionally, the total time delay

of a PHIL simulation is calculated as the sum of delays introduced by the interfacing components, their interactions and processes throughout the experiment loop.

In the following sections, the delay associated with each of the identified components and the processes associated with interfacing the components are analysed in detail. Any delay associated with a single component or a process will be represented by τ followed by a subscript indicating the component or process itself, while T will be used for a group of delays. An overall view of the different delays identified within this study are presented in Fig. 3.1 when switched-mode amplifiers are used.

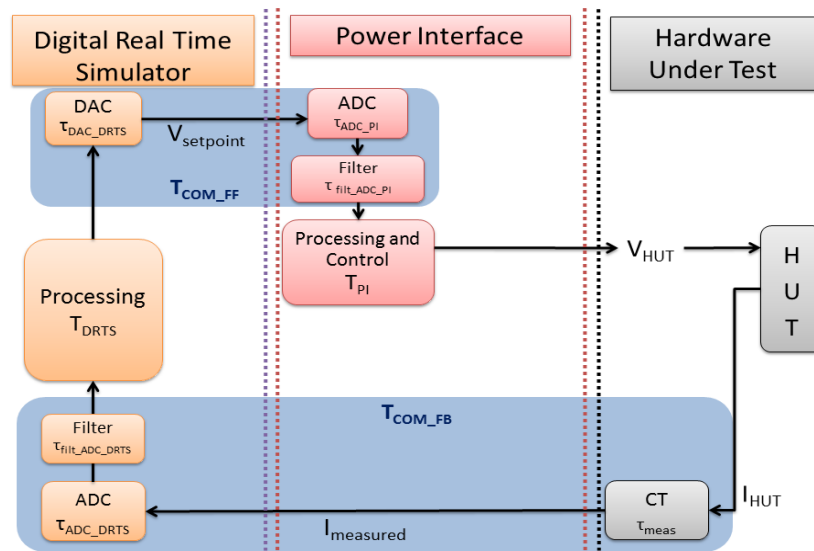


Fig. 3.1 PHIL time delay diagram with switched-mode amplifier

3.1.1 Simulation platform delay, T_{DRTS}

The DRTS used for PHIL applications is typically composed of processor cards using a fixed time-step for performing real-time simulations. An analog or digital interface for communicating with external components is also available within the DRTS. The processor card runs a real-time simulation model at a fixed time-step, while the communication

interface transfers the set-point from the simulation PCC to the PI for amplification and receives feedback from the HUT measurements (the communication link will be analysed in the following subsection for a more detailed analysis). Depending on the complexity and number of nodes of the simulated power system model, the processor card can be run at different fixed time-steps, varying from less than $1\mu\text{s}$ to $200\mu\text{s}$ and above. Therefore, due to the fixed time-step nature of the DRTS processing, the time-step of the DRTS, τ_{sDRTS} , is always constant. Furthermore, the simulated component used for the electrical coupling with the HUT, usually a controlled current or voltage source conditional to the IA selected, can introduce additional delays depending upon its implementation, $\tau_{coupling}$. Hence:

$$T_{DRTS} = \tau_{sDRTS} + \tau_{coupling} \quad (3.1)$$

3.1.2 Communication delay, T_{com}

The time produced as a result of the interconnection of the DRTS with external components for data transfer purposes, such as with the PI and HUT, is defined as the communication delay. The flow of information from the DRTS to the PI will be referred to as the feed-forward path and from the HUT measurement to the DRTS as the feedback path, with the delay associated to each path referred to as T_{comFF} , T_{comFB} respectively. The total communication delay (T_{com}) being the total contribution from both paths. There are two possibilities for the establishment of the communication link between the involved components, using analog or digital communication links. Both options are further analysed in the following subsections.

Analog communication delay, T_{Acom}

For the implementation of an analog communication link in a PHIL simulation, DACs for sending the required signals on the feed-forward path and ADCs for receiving the HUT measurements on the feedback path are required at the DRTS. Similarly, the PI requires an ADC for receiving the signal at the feed-forward path. Both of these conversion actions have a natural time delay, τ_{DAC} and τ_{ADC} respectively. The time required for the information to pass from the processor card to the ADC or DAC has been considered as part of the total delay for each conversion component due to its relatively small value (less than $1\mu s$) in comparison with other delays on the system.

It has to be noted that for large PHIL setups, where the number of inputs and outputs (I/O) is large and more than one I/O card is required, extra time delay is added due to the interconnection between I/O cards. Generally, an anti-aliasing filter is included as part of the ADC. Time delay of which (depending upon the cut-off frequency) can be larger than the actual time required for the ADC process and therefore should be considered, $\tau_{ADC_{filter}}$.

The measurement of the response of the HUT, τ_{meas} can also introduce additional delays in the feedback path. With these considerations, the time delay introduced when using analog communication in the feed-forward and feedback path of the PHIL implementation can be represented as:

$$T_{Acom_{FF}} = \tau_{DAC_{DRTS}} + \tau_{ADC_{PI}} + \tau_{filter_{ADC_{PI}}} \quad (3.2)$$

$$T_{Acom_{FB}} = \tau_{ADC_{DRTS}} + \tau_{filter_{ADC_{DRTS}}} + \tau_{meas} \quad (3.3)$$

$$T_{Acom} = T_{Acom_{FF}} + T_{Acom_{FB}} \quad (3.4)$$

where subscript DRTS and PI correspond to the components associated with the DRTS and PI respectively.

Digital communication delay, T_{Dcom}

High-speed serial protocols (such as PCIe and Aurora) are used for digital interconnection of DRTS units with PI and HUT measurements [KGW17]. Digital communication interfaces are generally more accurate (lower noise) and faster than analog communication, as DAC or ADC are not required, reducing the time delay of the PHIL simulation loop. Anti-aliasing filter is also not required in this implementation, avoiding the filtering of components of interest and thereby the consequent time delay. The digital communications interface delay depends on the latency of the optical fiber (τ_{fiber}), that for short cable runs (up to 300m) is less than $1\mu s$, and the processing delay of the algorithm ($\tau_{algorithm}$) that orchestrates the communication between the components. The delay introduced by the device used for the measurement of the HUT response has to be also considered in the feedback path.

$$T_{Dcom_{FF}} = \tau_{fiber} + \tau_{algorithm} \quad (3.5)$$

$$T_{Dcom_{FB}} = \tau_{fiber} + \tau_{algorithm} + \tau_{meas} \quad (3.6)$$

$$T_{Dcom} = T_{Dcom_{FF}} + T_{Dcom_{FB}} \quad (3.7)$$

3.1.3 Power interface delay, T_{PI}

Different power amplifier types can be used for PHIL implementations [Leh+12]. However, for this study only the most commonly used power amplifier types, switched-mode and analog power amplifiers, are assessed. Power amplifiers have a maximum ramp rate characteristic which limits their response under transient conditions, which will appear filtered depending on the characteristics of the amplifier. However, for a steady-state analysis of the time delay of PHIL implementations this delay is not affecting, as it will only affect during transient conditions.

Switched-mode power interface delay, $T_{PI_{Sw}}$

Switched-mode PIs used for PHIL applications comprise an active rectifier for the interconnection with the grid supply point and a power inverter driven by the signals received from the DRTS unit for amplification. The output of the converter is the amplified signal and is directly connected to the HUT, therefore providing the interfacing functionality. This AC/DC/AC converter operates across the four quadrants of the power plane, i.e., it can source and sink real and reactive power. This characteristic is typically required for PHIL applications as it allows for bi-directional flow of power.

The time delay introduced by switched-mode PIs is due to the inherent delay of the digital control loop architecture of power converters. This delay is constituted by: (i) one sampling period, τ_{sPI} , due to the discrete behaviour of the controller that can only update the duty ratio at the beginning of the switching cycle and (ii) an additional half time step to compare the pulse width modulation (PWM) signal with the carrier waveform, considered equivalent to a zero order hold (ZOH) [SBu06]. The total digital control loop delay, $\tau_{controlPI}$, can therefore vary depending on the implementation but it is commonly between 1.5 and 2 switching cycles. Therefore, the time delay introduced by the PI can be represented as:

$$T_{PI_{Sw}} = \tau_{controlPI} \approx 2 \cdot \tau_{sPI} \quad (3.8)$$

Linear power interface delay, T_{PI_L}

Linear power amplifiers are typically composed of parallel transistors (MOSFETs typically) operating in the linear region and capable to sink and source power [Leh+12]. The amplifier is directly controlled with an analog signal received from the DRTS, with no processing to be performed in comparison with a switched-mode amplifier. Accordingly the time delay introduced by linear power interfaces, $T_{PI_{Linear}}$, is typically

very low and it mainly depends in the specific hardware device. Although in some cases additional filters are introduced for smoothing the discrete signal behaviour received from the DRTS [Leh+12] and this would have to be considered for the time delay calculation. As a result the delay can be illustrated as:

$$T_{PI_L} = \tau_{PI_L} \quad (3.9)$$

where τ_{PI_L} depends on the particular specifications of the linear amplifier.

3.1.4 Delay introduced by other components and processes, T_{other}

The majority of the time delay is generally introduced by DRTS and PI units, however some other components or processes can introduce time delays of significant size and importance, referred to as T_{other} henceforth. Examples of such delays are: (i) digital filters added to the PHIL simulation loop to reduce the noise of measurement signals or to avoid resonances within the control of the PI [Ain+16], or (ii) low pass filters used for improving the stability of PHIL implementations [Lau+11]. The use of asynchronous filters can lead to an increase of the delay with the frequency components, impacting not only the fundamental components but also the harmonic components, potentially leading to unstable PHIL simulations.

3.1.5 Total delay, T_d

Based on the delays identified in the previous subsections, the total time delay of a PHIL simulation calculated using a conventional approach to the characterization can be defined as a function of cumulative delays, $T_d = f(T_{DRTS}, T_{com}, T_{PI}, T_{other})$ represented

as:

$$T_d = T_{DRTS} + T_{com} + T_{PI} + T_{other} \quad (3.10)$$

A diagram representation of the complete time delay cycle that a PHIL implementation with a switched-mode PI can incur on is presented in Fig. 3.1.

3.2 Proposed time delay characterization

In literature, time delay associated with PHIL simulations has been treated as constant and usually obtained by using conventional characterization approaches [Ain+16; RSW07]. Also, when considering the time delay as in Eq. 3.10 the time delay is assumed to be constant or almost constant. However, in a PHIL setup where more than one fixed time-step component is utilized, such as the DRTS and a switched-mode PI, variability in delay presents itself. This is an important aspect that has not been previously discussed in literature. The delay variability can have implications on the stability and accuracy of PHIL simulations. Therefore, in the following subsections, the proposed time delay characterization, considering the variability of the delay due to the interaction of fixed time-steps from the different components in the loop is established.

Within fixed time-step simulators, a new value of input can only be updated at the beginning of the next time-step; therefore, the variable delay introduced is the waiting time to the next step of the fixed time-step simulator. This waiting time is produced as a result of the external loop delay of the fixed time-step simulator not being an exact multiple of the its time-step.

Therefore, in this section, a novel characterization of time delay incorporating variability is proposed considering two fixed time-step components, i.e., a DRTS and a switched-mode PI.

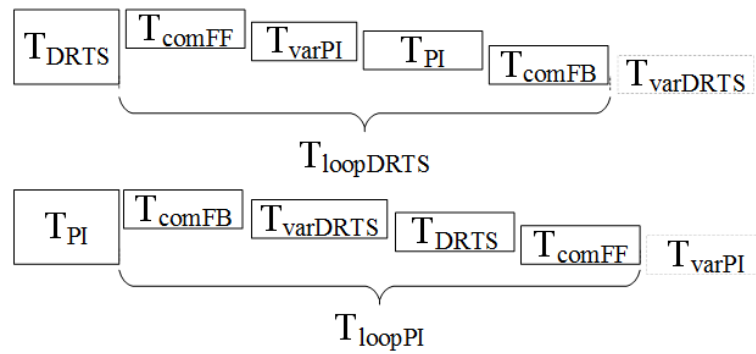


Fig. 3.2 Time delay loop for DRTS and PI.

The total external loop delay is defined as the total delay introduced by all the other (external) components that form the PHIL configuration. The external loop delay of a DRTS in a PHIL setup is illustrated in Fig. 3.2 and can be represented as:

$$T_{loopDRTS} = T_{comFF} + T_{varPI} + T_{PI} + T_{comFB} \quad (3.11)$$

where, T_{varPI} is the variable delay introduced as a result of the fixed time-step of the PI. In a similar manner, the total external loop delay of the PI in a PHIL setup is shown in Fig. 3.2 and can be represented as:

$$T_{loopPI} = T_{comFB} + T_{varDRTS} + T_{DRTS} + T_{comFF} \quad (3.12)$$

where, $T_{varDRTS}$ is the variable delay introduced due to the fixed time-step of the DRTS. These variable delays represent the waiting time prior to the start of the next time-step and are calculated as the difference between the total number of time steps elapsed from when the signal is output from the fixed time-step component and the actual time delay as presented in Eq. 3.13, with the ceiling function representing the characteristics of the fixed time-step. The difference is not typically an exact number of time steps and therefore, a variable waiting time (T_{var}) is expected. Specifically, these variable delays

are calculated as:

$$T_{varDRTS} = T_{DRTS} \cdot \text{ceil} \left(\frac{T_{loopDRTS}}{\tau_{sDRTS}} \right) - T_{loopDRTS} \quad (3.13)$$

$$T_{varPI} = T_{PI} \cdot \text{ceil} \left(\frac{T_{loopPI}}{\tau_{sPI}} \right) - T_{loopPI} \quad (3.14)$$

where $T_{varDRTS} \in \mathbb{R} : T_{varDRTS} \in [0, \tau_{sDRTS}]$, $T_{varPI} \in \mathbb{R} : T_{varPI} \in [0, \tau_{sPI}]$, and the *ceil* function represents scaling to the next integer number. Eq. 3.11 to 3.14 present four equations depending on each other, which are solved later in this Chapter by assessing values of $T_{varPI} \in [0, \tau_{sPI}]$ iteratively, as the actual value of T_{varPI} can be varying for each loop.

Therefore, in contrast with the conventional delay estimation approach (Eq. 3.10), the proposed total time delay characterization for PHIL implementations comprises a fixed delay, T_{fixed} , and a variable delay, T_{var} , as:

$$T_{fixed} = T_{DRTS} + T_{comFF} + T_{PI} + T_{comFB} \quad (3.15)$$

$$T_{var} = T_{varPI} + T_{varDRTS} \quad (3.16)$$

$$T_d = T_{fixed} + T_{var} \quad (3.17)$$

Calculating the delay with respect to the DRTS, the minimum and maximum delay of a specific PHIL implementation can be obtained as:

$$T_{d_{min}} = T_{fixed} + T_{var}]^{T_{varPI_{min}}} \quad (3.18)$$

$$T_{d_{max}} = T_{fixed} + T_{var}]^{T_{varPI_{max}}} \quad (3.19)$$

Defining n_1 and n_2 as:

$$n_1 = \text{ceil}\left(\frac{T_{d_{min}}}{T_{DRTS}}\right), n_2 = \text{ceil}\left(\frac{T_{d_{max}}}{T_{DRTS}}\right) \quad (3.20)$$

$$n = n_2 - n_1 \quad (3.21)$$

where n is the number of variability steps within the range of $T_d \in [T_{d_{min}}, T_{d_{max}}]$. Therefore, for a given PHIL setup, the time delay is characterized as

$$T_{d_{[T_{DRTS}, T_{PI}, T_{com}]}} = [T_{d_{min}}, T_{d_{max}}, n] \quad (3.22)$$

3.3 Assessment of delay variability impact on PHIL

In this section, the importance of time delay variability is stressed with an evaluation of the impact on stability and accuracy that it brings into PHIL simulations.

3.3.1 Impact of delay variability on stability

It is of utmost importance to assess the stability of PHIL simulations before its implementation, as it can cause severe damage to the HUT and PI. For this reason, the variability in delay should be given more attention as it can lead to erroneous stability assessments, risking costly laboratory equipment. In this subsection, the impact of delay variability on stability of PHIL simulations is demonstrated.

The stability assessment will be undertaken using a switched-mode PI, ITM IA and a linear load. The equivalent control loop of the a PHIL simulation with these characteristics has been shown in Fig. 2.2. The open loop transfer function, $H_{OL}(s)$, presented in Eq. 2.4 is used for the stability assessment, however for this study the PI is not assumed ideal. The transfer function of the PI, $H_{PI}(s)$, is then approximated by a

time delay and a second-order low pass filter derived from the output filter of the PI as in [Ren07]:

$$H_{PI}(s) = e^{-sT_{PI}} \cdot \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3.23)$$

where ω_n is the resonant frequency of the output filter and ζ is the damping ratio.

The stability criterion established for PHIL simulations using ITM has been well discussed in literature and when assuming ideal PI and $X_{DRTS} = X_{HUT} = 0$, it can be represented as $|Z_{HUT}| > |Z_{DRTS}|$ [Lau+11; Jon11; KKK17]. With the aim of demonstrating the impact of time delay and its variability in PHIL, the parameters Z_{HUT} and Z_{DRTS} have been chosen for a stable setup as 1.005 pu and 1 pu respectively. The damping ratio and the corresponding resonant frequency is $\zeta = 0.63$ and $\omega_n = 6523.28 \text{ rad/s}$. Assuming $T_d = [450, 650, 4]$, the stability is analysed using the Nyquist criterion for the minimum, maximum and the average time delay.

In Fig. 3.3, the open loop frequency response of the PHIL system has been plotted only with positive frequencies for a more clear representation. As can be observed, the system is stable for $T_d = 450$ and $550 \mu\text{s}$, the stability margin reducing with the increasing delay i.e., the contour moves closer to encircling the instability point (-1,0), with the system going unstable for $T_d = 650 \mu\text{s}$. To summarize, the given system lies between stable and unstable region for a varying time in the total delay of $200 \mu\text{s}$ in this case. This emphasizes the importance of considering the variability in time delay for PHIL simulations. Approximating time delay of PHIL simulations or considering the delay to be a constant increases the risk and uncertainty of the implementation.

3.3.2 Impact of delay variability on accuracy

Time delay presents itself as an additional phase difference between voltage and current at the PCC, and to assess its impact on the accuracy of PHIL simulations, the waveforms should be considered at the simulation PCC. At the HUT, the problem is not apparent,

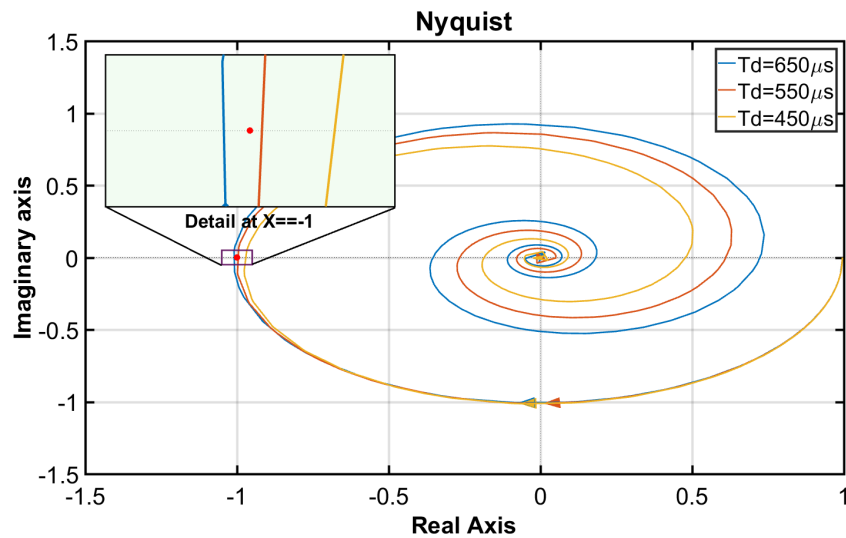


Fig. 3.3 Nyquist plot of time delay effect on PHIL

since it responds naturally (with currents) to whatever voltages it is presented with (in the case of V-ITM).

The added phase difference between voltage and current at the simulation PCC, affects the power factor of the HUT, leading to inaccurate active and reactive power exchanges compared to an ideal scenario. Furthermore, if the HUT draws harmonic currents, the phase relationships between harmonic voltages and currents in the simulation and at the HUT terminals can be significantly different, as time delay corresponds to larger phase lags at higher harmonic frequencies, leading to low accuracy results [GRB15].

Whit the presence of variable time delay, the response of the HUT seen by the simulation will present a characteristic noise introduced by the delay variations. Furthermore, this fluctuations introduce oscillatory behaviours in the injected power at the PCC which can affect the voltage, the measurement of variables of interest and even to some control strategies if no action is in place for its mitigation.

To demonstrate the impact of the variability in time delay, simulation based assessment of the system illustrated in Fig. 3.4 and with the parameters presented in the

previous subsection has been conducted and is presented in Fig. 3.5. For the first 2s of the simulation, the total time delay, T_d is varied between 450 and 550 μ s every 300 μ s. As can be observed from Fig. 3.5 (a), the system is stable with this variable delay (from 0 to 2s) as expected from the stability assessment. However, the variability in delay presents itself as an oscillation as shown when examined closely in Fig. 3.5 (b). At time $t=2$ s, the simulation is switched into a fixed delay of 550 μ s, at which point the oscillations in the waveform cease. These fluctuations will be observed as oscillations in power exchanged at the PCC, and can be significant if scaling of the currents is required. At time $t=2.1$ s, the simulation is switched from a fixed delay of 550 μ s to 650 μ s, soon after which the system becomes unstable in accordance with the analysis presented earlier and as shown in Fig. 3.5 (a).

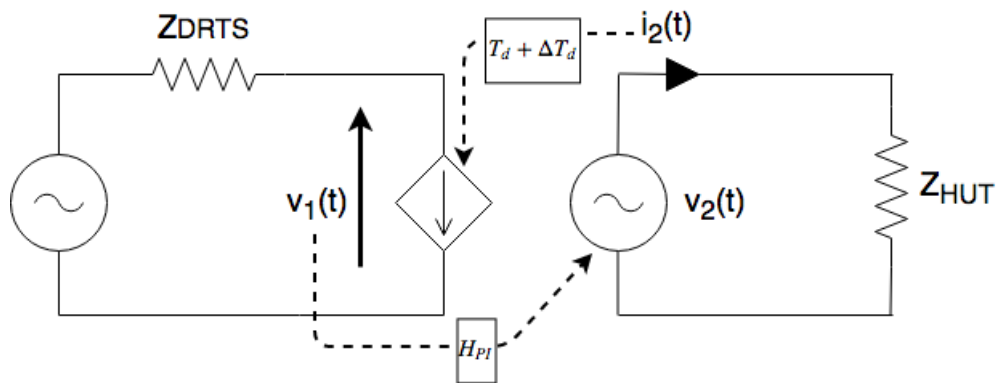


Fig. 3.4 Simulation model for accuracy assessment

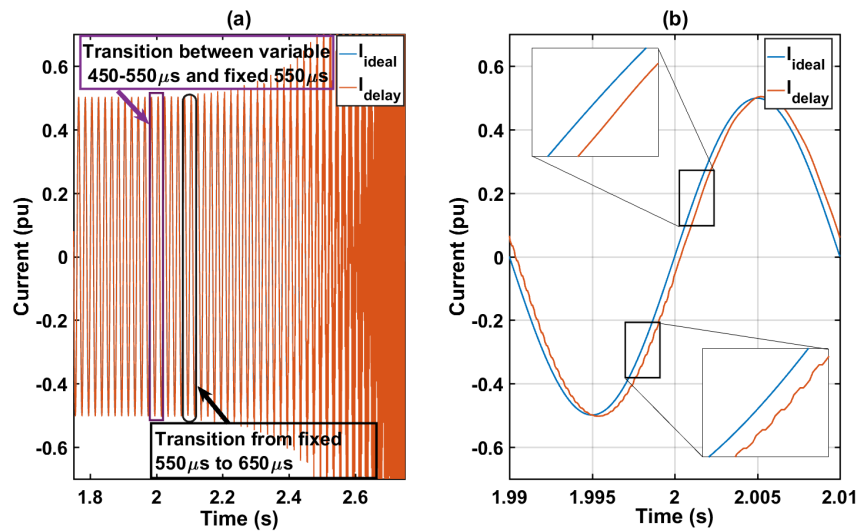


Fig. 3.5 Simulation assessment of stability and accuracy under variable time delay.

3.4 Experimental validation of the proposed time delay characterization

For the experimental validation of the time delay formulations and dynamics presented in the previous sections three different case studies have been developed which will be analysed theoretically and experimentally. The case studies are:

- ▶ Case A: Validation with a time synchronized signal.
- ▶ Case B: Validation with a PHIL platform with digital communication interface.
- ▶ Case C: Validation with a PHIL platform with analog communication interface.

For the three validation case studies, DRTS and PI with the same characteristics have been used:

- **DRTS:** A Real-Time Digital Simulator (RTDS), with capabilities similar to other DRTS in the market has been used, allowing for this study to be extrapolated to DRTS units from different providers. Various time-steps have been utilized

within each case study and these are presented individually for each case in the following subsections.

- **PI:** A switched-mode back-to-back converter is used as the PI, which can have different control frequencies (accordingly different time-steps). The control algorithm implemented in the controller has a double update rate of the PWM signal, reducing the total delay of the control loop.

3.4.1 Case A: Validation with a time synchronized signal

For an accurate analysis of the time delay and its dynamic behaviour, a time synchronized signal (with a Global Positioning System (GPS) clock) is transferred from the RTDS to the switched-mode PI real-time control target with a fast digital communication link established between RTDS and PI. The signal is then directly routed back to the RTDS for closing the loop as shown in Fig. 3.6.

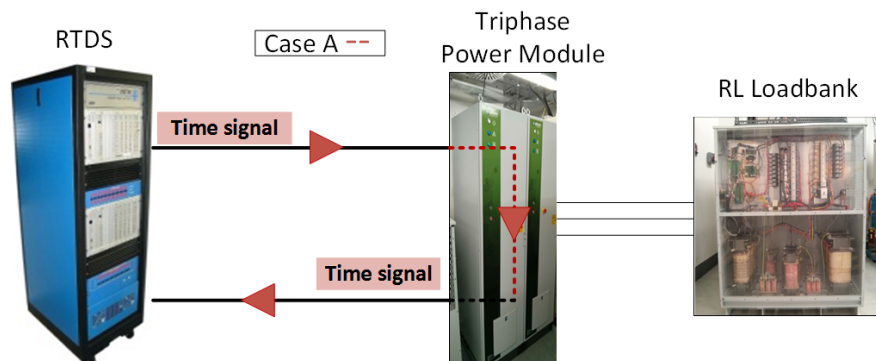


Fig. 3.6 Experimental setup with time synchronized signal

In this manner the loop delay of the setup can be analysed without uncertainties introduced by the measurement of the response. This case study is presented for an initial analysis of the characteristics of the time delay in PHIL simulations as identified in the previous sections, and hence it will provide the loop delay between the DRTS

and the PI without taking into account the HUT, allowing for the verification of the behaviour of the DRTS, PI and the digital communication link.

The time step of the PI is chosen as $\tau_{s_{PI}}=66.667\mu s$ (15kHz). In this case as the signal is directly routed to the output, T_{PI} is considered as only one time-step rather than the two typically used when the HUT currents are measured. The communication delay of the feed-forward path in this case, due to a handshake process between the two ends of the serial link has been identified as:

$$\tau_{algorithm} = \begin{cases} \tau_{s_{PI}} - \tau_{s_{DRTS}}, & \tau_{s_{PI}} > \tau_{s_{DRTS}} \\ 0\mu s, & otherwise \end{cases} \quad (3.24)$$

by which, the PI needs to be the one establishing the communication and hence if $\tau_{s_{PI}}$ is larger than $\tau_{s_{DRTS}}$ the difference in time-step is added to the communication delay, otherwise no extra delay is considered. The time delay of the fiber in this case is considered as $\tau_{fiber}=2\mu s$. These considerations will need to be assessed on a case by case basis depending on the infrastructure and devices being used for the test.

Theoretical time delay characterization

Multiple theoretical assessments have been performed for different $\tau_{s_{DRTS}}$ (from 10 to $60\mu s$ in steps of $10\mu s$ and 80, 100, 120, 150, $200\mu s$). In this case $T_{DRTS}=\tau_{s_{DRTS}}$ as no coupling delay exists. For each different T_{DRTS} assessed the values of the characterized time delay for this particular PHIL implementation have been calculated with the proposed time delay characterization. The characterized time delays for each implementation are presented in Table 3.1.

Table 3.1 Theoretical time delay characterization

PHIL Setup			Time Delay Characterization
T_{DRTS}	T_{PI}	T_{Dcom}	$T_d = [T_{d_{min}}, T_{d_{max}}, n]$
10	66.667	58.667	[140, 210, 6]
20	66.667	48.667	[140, 220, 4]
30	66.667	38.667	[150, 210, 2]
40	66.667	28.667	[160, 240, 2]
50	66.667	18.667	[150, 250, 2]
60	66.667	8.667	[180, 240, 1]
80	66.667	4	[160, 240, 1]
100	66.667	4	[200, 300, 1]
120	66.667	4	[240, 360, 1]
150	66.667	4	[300, 300, 0]
200	66.667	4	[400, 400, 0]

Experimental validation

For the experimental validation, the time synchronized signal is sent to the PI and when the time stamped signal is received at the DRTS, the actual time is compared with the signal received, in this manner an accurate calculation of the total loop delay per time-step can be determined. In Fig. 3.7, four examples of the measured total delay per time-step are shown. Each of the plots presents different variations, from $n=4$ when $\tau_{s_{DRTS}}=20\mu s$, to a fixed delay, $n=0$, when $\tau_{s_{DRTS}}=150\mu s$. The identified delay steps in these cases are equal to the ones identified theoretically and presented in Table 3.1. This process has been also carried out experimentally for all the other $\tau_{s_{DRTS}}$ theoretically assessed, with each of the experimental results generating the same delay variability characteristics as theoretically identified in Table 3.1, thereby validating the time delay characterization approach presented in this Chapter. The suitability of time delay characterization is confirmed, also proving the existing time delay variability in PHIL simulations which can adversely impact its stability and accuracy. However, a full PHIL implementation is still required for a complete analysis.

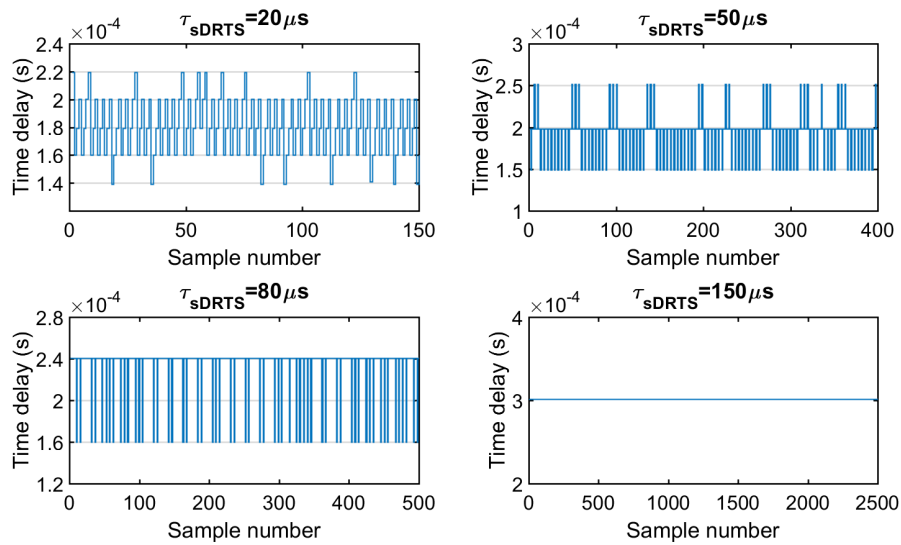


Fig. 3.7 Experimentally measured time delay variations.

3.4.2 Case B: Validation with a PHIL platform with digital communication interface.

The same configuration of DRTS, PI and digital communication link utilised in Case A has been used for this case. However, in this case a resistive load bank has been added as the HUT with its measurement processed by the PI and sent back with the digital communication link as shown in Fig. 3.8. V-ITM is chosen as the IA for this configuration, in which the systems are coupled by communicating a voltage set point to a voltage source at the hardware side (the power amplifier in voltage source mode) and the consequent current response from the HUT to a controlled current source at the simulation end [RSB08]. The simulated part of the system comprises a voltage source and a small resistive impedance $Z_{DRTS} = 0.066\Omega/phase$ that will ensure a stable PHIL implementation, as the HUT resistive impedance is much larger, $Z_{HUT} = 15.87\Omega/phase$, and therefore the condition of stability is met with a large margin. This simple configuration allows for an effective study of the time delay, as using a pure resistive component as the HUT, ensures voltage and current are in phase

when no time delay is present. Therefore, by comparing voltage and current waveforms at the simulation PCC, the total time delay can be identified. In contrast with Case A, the aim here is to identify the total loop delay of the PHIL setup, and by doing so further validate the equations described in the previous sections along with the dynamic behaviours identified.

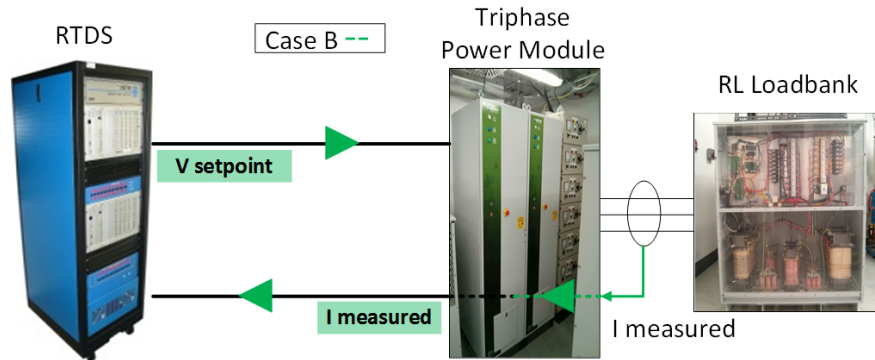


Fig. 3.8 Experimental setup for PHIL with digital link

For the theoretical assessment of the total delay when the response of the HUT is measured, T_{PI} is considered as $2\tau_{spI}$. T_{Dcom} remains the same as in Case A (the digital communication link remains same). The distribution of τ_{SDRTS} considered for the assessment of the time delay in this case are:

$$\tau_{SDRTS} = [30, 40, 60, 80, 100, 120, 150, 200]$$

With the HUT connected, its response is fed back to the DRTS, leading to a complex measurement procedure of the loop delay. This is mainly due to: (i) in this case there is no time synchronized signal available as the current measurement received at the DRTS is a different signal compared with the voltage set-point that is being sent, and (ii) the fact that the time delay has been identified to be varying in very short time periods (up to every time-step).

Therefore, solutions such as Fourier transforms (for the measurement of the phase difference of the fundamental) or the calculation of the phase difference at zero crossing of the voltage and current waveforms for evaluating the time delay are not accurate enough. The main reason being that the response will only be calculated every fundamental cycle as opposed to a per time-step solution required in this case. It has to be mentioned that there is no clear definition of time delay measurements for sinusoidal waveforms in such short windows and therefore the calculation could be done in different manners. In this case, as a resistive HUT is used, by using normalized voltage and current waveforms, the time delay has been considered as the time distance between the voltage and current waveforms when both of them present the same normalized amplitude (as in an ideal situation that would be the case at zero crossing). Hence, a procedure for identifying the time delay for each time-step has been carried out with the help of a Matlab script using the data recorded from experiments as shown in Fig. 3.9 for an example with $\tau_{sDRTS} = 30\mu s$.

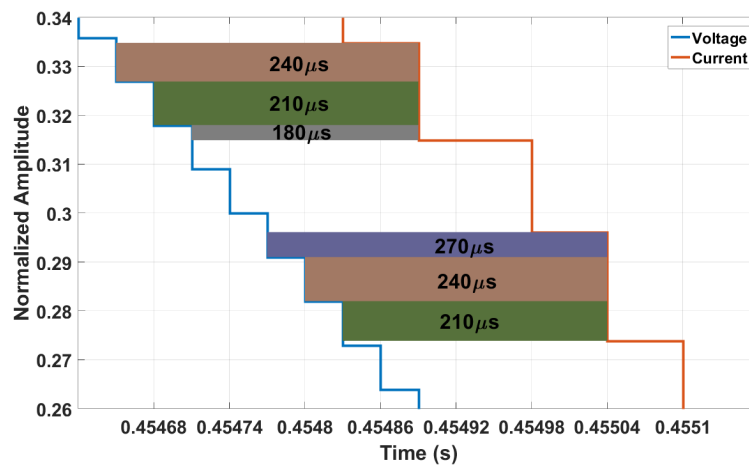


Fig. 3.9 Time delay assessment for every time step with $T_{DRTS} = 30\mu s$.

The experimental results have been obtained by calculating the delay between the voltage and current waveforms as presented in Fig. 3.9 for half cycle of the fundamental waveform and values between $0.9pu$ and $-0.9pu$ of the normalized amplitude.

The experimental results are presented in Fig. 3.10 by means of a box plot for each of the experiments performed. The components that form the whiskers of the box plot are considered to be produced by the noise introduced by the hardware and its measurements and by the actual calculation procedure of the total time delay. Consequently, in Table 3.2 theoretical and experimental time delays with $\tau_{spi}=66.667\mu s$ are presented, considering the experimental delays as the box section of each experiment (as it represents the likely range of variation or interquartile range).

Experimentally measured time delays can present a one time-step variation from the theoretically calculated delay as can be observed in Table 3.2. For the small time steps, the reduction in experimentally measured delay can occur due to the slack time (time between the finalization of the control calculation and the end of the time-step) of the PI, as this can trigger the signal to be fed back prior to the theoretically assumed end of the time-step.

The knowledge acquired from the characterization can help reduce the total loop delay of the PHIL implementation while enabling more effective time delay compensation mechanisms to be employed when the exact delay is known.

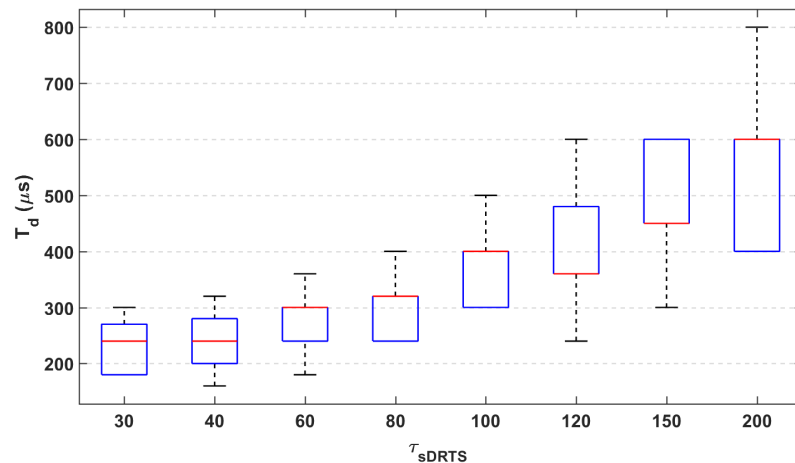


Fig. 3.10 Experimentally measured time delay for Case B

Table 3.2 Time delay of PHIL with digital communication link and $\tau_{sPI} = 66.667\mu s$

$\tau_{sDRTS} [\mu s]$	Theoretical Delay $[\mu s]$	Experimental Delay $[\mu s]$
30	[210, 270, 2]	[180, 270, 3]
40	[240, 280, 1]	[200, 280, 2]
60	[240, 300, 1]	[240, 300, 1]
80	[240, 320, 1]	[240, 320, 1]
100	[300, 400, 1]	[300, 400, 1]
120	[360, 360, 0]	[360, 480, 1]
150	[300, 450, 1]	[450, 600, 1]
200	[400, 600, 1]	[400, 600, 1]

3.4.3 Case C: Validation with a PHIL platform with analog communication interface.

For the provision of a strong validation of the theoretically identified time delay characteristics and dynamics, a different case study where the digital communication link is replaced by an analog communication link is also studied. This case study provides a higher level of uncertainty due to the addition of new components (such as ADCs and DACs) and their associated filters and dynamics, furthermore noise is typically introduced when analog signals are used. Similarly to the other case studies, first a theoretical assessment of the time delay is carried out, followed by the assessment of experimentally measured delays and a comparison of both results. The experimental configuration used for this study is presented in Fig. 3.11. A theoretical individual assessment of the time delay introduced by the different components present in the PHIL configuration of this case study has been performed as follows:

- **DRTS:** For this case study, time steps from $10\mu s$ to $100\mu s$ in steps of $10\mu s$, $120\mu s$ and $150\mu s$ within the DRTS have been considered. Additionally, from the time that the HUT response signal is received at the DRTS simulation until the signal is effectively reproduced at the output of the controlled current source (used for the ITM interface algorithm), one additional τ_{DRTS} is added to the total delay

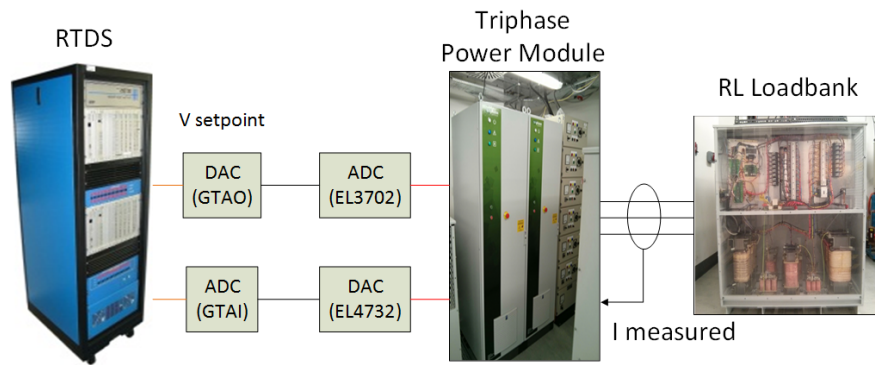


Fig. 3.11 PHIL experimental setup with analog communication interface.

in this case, effectively $\tau_{coupling} = \tau_{DRTS}$. Resulting in a total delay introduced by the DRTS of

$$T_{DRTS} = \tau_{DRTS} + \tau_{coupling} = 2 \cdot \tau_{DRTS}$$

- **PI:** In this case, a control frequency of 16kHz ($\tau_{PI} = 62.5\mu s$) is used, however the control in this implementation requires of an extra time-step for the computation to provide the control outputs, which results in the addition of an extra τ_{PI} to the total time delay. Therefore, under this special condition, the time delay introduced by the PI can be represented as:

$$T_{PI_{Sw}} = 2 \cdot \tau_{s_{PI}} + \tau_{s_{PI}} = 187.5\mu s$$

- **Communication interface:** For establishing the analog communication link, different ADCs and DACs are used at the DRTS and PI. At the DRTS, a Giga-Transceiver Analog Output (GTAO) card is used, which requires 6-8 μs for converting the data received from the processing card. The data from the processing card is transferred to the output card once per simulation time-step and the communication latency between them is of 521ns, hence the time delay of the analog output card is $\tau_{DAC_{DRTS}} \approx 8.5\mu s$. On the PI side, a Beckhoff EL3702 Analog

Input card is used for receiving the setpoint from the DRTS, with a conversion time of $\tau_{ADC_{PI}} \approx 10\mu s$ including the ADC filter. Therefore, according to Eq. 3.2,

$$T_{Acom_{FF}} = 8.5 + 10 = 18.5\mu s$$

In the feedback path, at the PI side, a Beckhoff EL4732 Analog Output card with conversion time of $\tau_{DAC_{PI}} \approx 10\mu s$ is utilized. At the DRTS end, an analog input card, Giga-Transceiver Analog Input (GTAI), is used. GTAI samples every $6\mu s$ and has a communication latency of $521ns$ with the processor card, i.e., $\tau_{ADC_{DRTS}} \approx 6.5\mu s$. The card sends the samples to the processing card once the analog to digital conversion is completed and only the last conversion previous to the start of the next processing time-step is read. Additional time delay is added by the anti-aliasing filter included within the card, the filter cut-off frequency setting can be selected from 84.2 kHz, recommended for very small time-steps (units of μs), to 10.1 kHz, to avoid introducing high order harmonic noise. The time delay introduced by the filter, $\tau_{filter_{DAC}}$, is $1.89\mu s$ and $15.75\mu s$ respectively for a 60Hz waveform. Hence, with 84.2 kHz filter being used, and assuming the delay introduced for a 50Hz signal is approximately $2\mu s$. The measurement of the response is performed by the PI, and in this case the delay introduced by the measurement is already accounted for by $T_{PI_{Sw}}$. Hence, the feedback loop delay can be calculated as Eq. 3.3,

$$T_{Acom_{FB}} = 10 + 6.5 + 2 = 18.5\mu s$$

Total delay

For the calculation of the total time delay introduced by the presented PHIL implementation, with the aforementioned individual delays, theoretical calculation of the total time delay for the specified $\tau_{s_{DRTS}}$ steps has been performed similarly to the previous

Table 3.3 Time delay of PHIL with analog communication link and $\tau_{PI} = 1/16000$

$\tau_{RTDS} [\mu s]$	Theoretical Delay [μs]	Experimental Delay [μs]
30	[300, 360, 2]	[330, 390, 2]
40	[320, 400, 2]	[320, 400, 2]
50	[350, 400, 1]	[350, 400, 1]
60	[360, 420, 1]	[360, 420, 1]
70	[420, 490, 1]	[350, 420, 1]
80	[400, 480, 1]	[350, 480, 2]
90	[450, 540, 1]	[360, 450, 1]
100	[500, 500, 0]	[300, 400, 1]
120	[480, 600, 1]	[360, 480, 1]
150	[600, 600, 0]	[300, 450, 1]

case studies. The theoretical time delay characterization for this case is presented in Table 3.3

Experimental results are presented in Fig.3.12 by means of a box plot. In the box plot, it is assumed that the interquartile range (the box without the whiskers) represents the total delay variation more accurately as the maximum and minimums are typically due to noise and inaccuracies in the calculation. Due to the analog communication approach used for this case, excessive noise is introduced, bringing uncertainty for an accurate evaluation of the total time delay in a per time-step basis.

This can be more clearly observed from Fig. 3.13, where one cycle of the voltage and current waveforms is shown. The noise from the HUT response signal (current waveform) can lead to an erroneous measurement of the time delay, even more when this is being measured in a per time-step basis. Therefore erroneously perceiving the delay as much smaller (as in the zoomed portion of the signal of Fig. 3.13 would be) or much larger under opposite circumstances. The box plot presented intends to abstract the time delay from the noise and the delay calculation inaccuracies, however the precision of the time delay assessment in this case is not guaranteed.

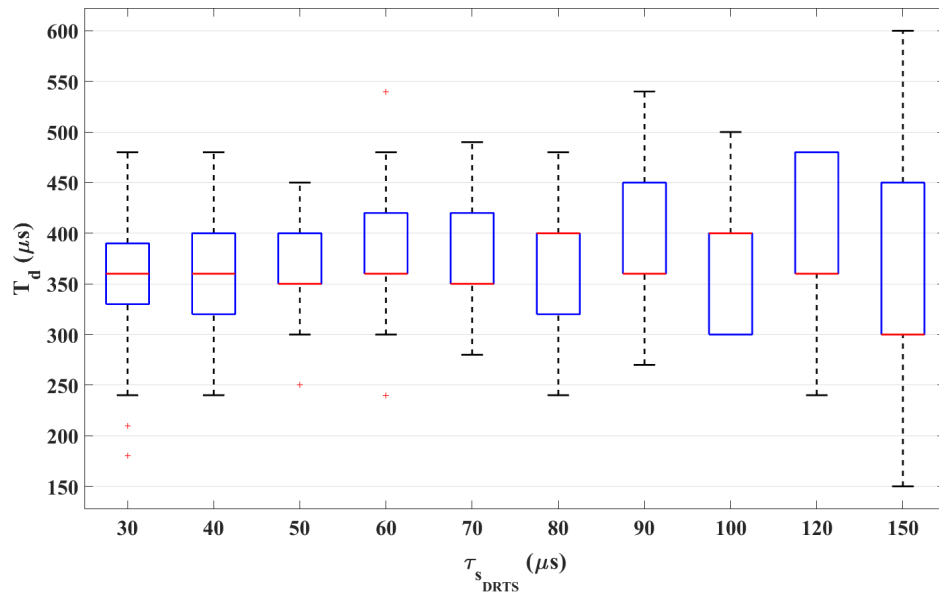


Fig. 3.12 Experimentally measured time delay for Case C

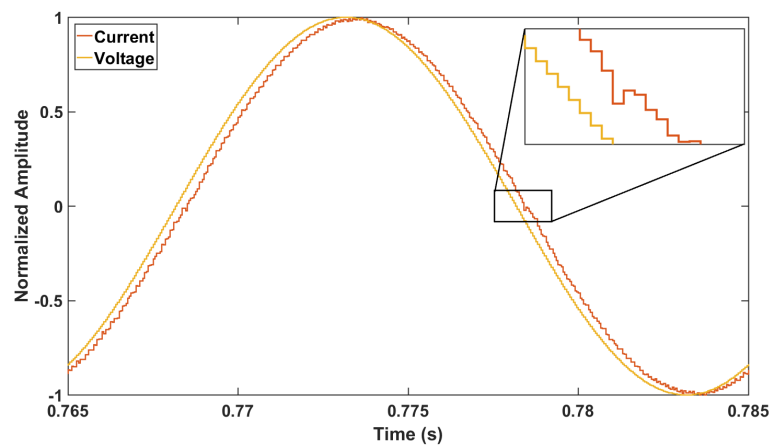


Fig. 3.13 Time delay of PHIL with analog communication link

In Table 3.3, the time delays measured experimentally and theoretically for this case are presented. These values can differ at some of the measurement points, with a larger error in the larger time-steps due to the low accuracy of such steps. Therefore, for implementations with analog communications a detailed characterization in a per time-step basis can be problematic. However, this study can lead to an improved understanding of the time delay and therefore to the adoption of an informed decision

towards the compensation or reduction of the time delay. A digital filter can be used to reduce the noise of the signal, nonetheless the signal is smoothed by the filter action and the detailed characterization is no longer precise enough.

3.5 Lessons learned from the characterization of time delay

The time delay characterization along with the assessment of the variability impact have been the main objectives of this section. However, the developed understanding and knowledge about the time delay in PHIL implementations has also lead to the identification of measures for reducing the introduced delays along with the mitigation and elimination of the time delay variability.

3.5.1 Reducing time delay

In view of the time delay characterization presented, some steps towards the reduction of the time delay have been identified, leading to an improved accuracy and stability of PHIL setups. This can be analysed by assessing individual components of the implementation.

- **DRTS:** The first item to consider towards the reduction of the time delay is to decrease the simulation time-step of the DRTS. The feasibility of decreasing the simulation time-step will depend on the computation complexity of the simulated system and the computational efficiency of the control implementation within the simulation model. However, it has to be noted that depending on the time delay characteristics, as presented in the previous section, reducing the time-step of the DRTS can lead to an increased variability in the time delay and not necessarily to a reduction of the total time delay.

- **PI:** For switched-mode PIs, similarly to DRTS, if the control time-step is reduced, the total delay can be reduced. This can be achieved in a number of ways, such as increasing the switching frequency of the converter to allow for faster control time-steps, or introducing a double update rate that will reduce the time step to half while maintaining the same switching frequency [SBu06]. Although, similarly to the DRTS, the reduction of the time-step of the PI does not guarantee a reduction on the total time delay due to the interactions with the other fixed time-step components in the PHIL implementation. Aiming at decreasing the time delay, the ideal choice would be to use linear amplifiers, as the time delay associated with these devices is significantly lower and by using them the variability introduced by the switched-mode amplifier due to the fixed time-step behaviour is removed. However, limitations on cost and power ratings due to their low efficiency can prevent its use [Leh+12].
- **Communication interface:** Replacing analog interfaces with fast digital communications protocols (such as Aurora or PCIe) using fiber optic links, avoids delays associated with ADCs, DACs and the introduction of filters, establishing a real-time connection with the external units while reducing the total time delay. This can also bring an improvement in accuracy due to the reduced noise in the signals in comparison with analog interfaces.
- **Other delays:** Using an external dedicated measurement for the HUT response, the delay can be reduced in comparison with a setup where the measurement from the PI is used. Furthermore, the use of filters, for different purposes such as anti-aliasing, for improving stability or for reducing the noise, should be carefully assessed, targeting maximum cut-off frequencies with minimum delays.

3.5.2 Mitigating and eliminating variability in time delay

The importance of identifying the variability of time delay in the assessment of stability and accuracy of PHIL setups has been stressed in this Chapter. Accordingly, a reduction or elimination of the variability would improve PHIL simulations. Discussion of possible mitigation techniques and examination of a proposed condition for achieving the elimination of variability in time delay is described below.

Mitigation of the time delay impact

To mitigate the impact of time delay variability, a low pass filter can be employed to filter out the oscillations created by the variable time delay. This is shown in Fig. 3.14, where a 2kHz low pass filter has been introduced to mitigate the oscillations present in the received signal from the HUT measurement due the presence of noise as well as time delay variability. With low filter cut-off frequencies, the oscillations will be further reduced and abated. Although, the filter will add its own delay, increasing the total time delay, which could be compensated by time delay compensation techniques (if the amount of delay introduced does not make the system unstable). Depending on the characteristics of the filter used for abating the oscillations, harmonics of interest may be filtered and the accuracy of the implementation can be reduced. It should also be noted that some filters have diverse phase lags at different frequencies (variable group delay) and if time delay is to be compensated this has to be considered. At the same time, by adding a low pass filter the stability of the PHIL simulation can be improved as has been demonstrated in [Lau+11].

Eliminating variability in time delay

Time delay variability is introduced as a result of the interaction between two components with fixed time-step computation. Therefore, the time-steps of these components

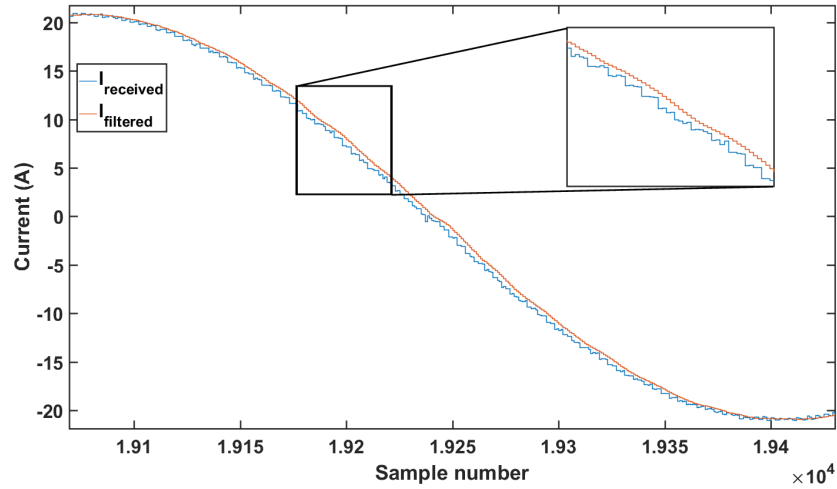


Fig. 3.14 Mitigation of delay impact with filter.

can be combined in such a way that the time delay at the PCC of the DRTS is kept constant, eliminating the delay variability. This can only be achieved when, for any possible value of T_{varPI} , the variation of the external loop delay to the DRTS, $T_{loopDRTS}$, remains within one time-step of the DRTS. The condition for achieving constant total time delay can be identified as:

$$T_d = N \cdot \tau_{sDRTS}$$

where N is an integer number that must remain constant. Therefore, the variable attributes can be identified by substituting T_d with Eq. 3.17 as:

$$T_{DRTS} + T_{comFF} + T_{varPI} + T_{PI} + T_{HUT} + T_{comFB} + T_{varDRTS} = N \cdot \tau_{DRTS}$$

where the only varying attributes are T_{varPI} , that will be assessed for all possible values, and $T_{varDRTS}$. For this assessment, T_{DRTS} is considered equal to τ_{sDRTS} , as if any $\tau_{coupling}$ is present this can be considered a fixed time delay and included as part of T_{comFF} or

T_{comFB} . The equation can then be further simplified with Eq. 3.11 as:

$$\tau_{sDRTS} + \underbrace{T_{comFF} + T_{varPI} + T_{PI} + T_{HUT} + T_{comFB}}_{T_{loopDRTS}} + T_{varDRTS} = N \cdot \tau_{sDRTS}$$

$$\tau_{sDRTS} + T_{loopDRTS} + T_{varDRTS} = N \cdot \tau_{sDRTS}$$

and by substituting $T_{varDRTS}$ with Eq. 3.13

$$\tau_{sDRTS} + T_{loopDRTS} + T_{DRTS} \cdot \text{ceil} \left(\frac{T_{loopDRTS}}{\tau_{sDRTS}} \right) - T_{loopDRTS} = N \cdot \tau_{sDRTS}$$

$$\tau_{sDRTS} + \tau_{sDRTS} \cdot \text{ceil} \left(\frac{T_{loopDRTS}}{\tau_{sDRTS}} \right) = N \cdot \tau_{sDRTS}$$

$$1 + \text{ceil} \left(\frac{T_{loopDRTS}}{\tau_{sDRTS}} \right) = N$$

with 1 being a constant integer number and therefore not affecting the equation, the final condition that will make the total loop delay constant in a PHIL implementation with switched-mode power amplifier can be expressed as:

$$\text{ceil} \left(\frac{T_{loopDRTS}}{\tau_{sDRTS}} \right) = N \quad \forall T_{varPI} \in [0, \tau_{sPI}] \quad (3.25)$$

This condition is analysed for a specific value of τ_{sDRTS} and τ_{PI} . Frequently, τ_{PI} is selected according to the power amplifier specifications (as it can incur into hardware limitations), and a selection of values of interest for τ_{sDRTS} can then be assessed. By doing so, a range of values for which the condition applies will be found. In practice, analysis of only $T_{varPI} = 0$ and $T_{varPI} = \tau_{PI}$ is sufficient for the assessment, as the results must be the same for both calculations in order to identify a condition that meets the criteria for achieving constant delay.

Ideally, the minimum value of τ_{sDRTS} that satisfies the equation would be the best choice, but depending on the PHIL implementation the delay identification can present

small errors, therefore selecting a τ_{sDRTS} for which τ_{sDRTS} immediately above and below are also constant can be more appropriate. If a large τ_{sDRTS} is identified, this might not always be an option as the increased time delay can lead the system to instability or an increased time-step might not be appropriate for the type of study being undertaken. However, if the system is stable with the increased delay and the time-step is suitable for the study to be undertaken, this option could also be chosen.

For the purpose of validating Eq. 3.25 and to provide an example, the same test case as in Case Study A from section 3.4.1 (as less noise and uncertainties are introduced in this case study), has been chosen. In this case, the parameters selected for the study are $\tau_{PI} = 66.667\mu s$ and $\tau_{sDRTS} = [1 - 200]\mu s$ in steps of $1\mu s$. The calculation for finding the τ_{sDRTS} that met the condition is presented in Table 3.4 for the first range found ($[69 - 70]\mu s$), and in Table 3.5 for the second range found ($[138 - 200]\mu s$). As a result, the ranges of τ_{sDRTS} that met the condition are $[69 - 70]\mu s$ and $[138 - 200]\mu s$. This is in alignment with the theoretical results developed for case A and presented in Fig. 3.15, validating the proposed condition for achieving constant delay. However, the range $[69 - 70]\mu s$ is probably not large enough as variations on the identified delays of the individual components by more than $1\mu s$ can make this range to fail. Therefore, selecting a τ_{sDRTS} that is within a larger range is recommended, as in practice that will be the ranges that can make the delay constant with small variations in the identified delay not affecting.

It has to be noted that if the same exercise is carried out from the PI perspective, i.e. by trying to find τ_{sDRTS} and τ_{PI} for:

$$\text{ceil}\left(\frac{T_{loopPI}}{\tau_{sPI}}\right) = K \quad \forall T_{varDRTS} \in [0, \tau_{sDRTS}] \quad (3.26)$$

this will produce a constant delay at the PI, which does not imply that the delay at the DRTS PCC will be held constant, so it is important to remark that the time delay must be measured at the DRTS PCC. Furthermore, for PHIL implementations with analog

communication, the elimination of the time delay variability in this manner can be very limited due to the uncertainties introduced by the communication link and the noise that the signal typically carries that makes challenging to accurately characterize the time delays and therefore to differentiate between variability and noise.

Table 3.4 Constant delay calculation for range 1

τ_{SDRTS}	T_{DcomFF}	T_{varPI}	τ_{PI}	T_{DcomFB}	$T_{varDRTS}$	T_d	Eq. 3.25
68	2	0	66.667	2	65.333	204	2
68	2	66.667	66.667	2	66.666	272	3
69	2	0	66.667	2	67.333	207	2
69	2	66.667	66.667	2	0.666	207	2
70	2	0	66.667	2	69.333	210	2
70	2	66.667	66.667	2	2.666	210	2
71	2	0	66.667	2	0.333	142	1
71	2	66.667	66.667	2	4.666	213	2

Table 3.5 Constant delay calculation for range 2

τ_{SDRTS}	T_{DcomFF}	T_{varPI}	τ_{PI}	T_{DcomFB}	$T_{varDRTS}$	T_d	Eq. 3.25
136	2	0	66.667	2	65.333	272	1
136	2	66.667	66.667	2	134.666	408	2
137	2	0	66.667	2	66.333	274	1
137	2	66.667	66.667	2	136.666	411	2
138	2	0	66.667	2	67.333	276	1
138	2	66.667	66.667	2	0.666	276	1
139	2	0	66.667	2	68.333	278	1
139	2	66.667	66.667	2	1.666	278	1
150	2	0	66.667	2	79.333	300	1
150	2	66.667	66.667	2	12.666	300	1
200	2	0	66.667	2	129.333	400	1
200	2	66.667	66.667	2	62.666	400	1

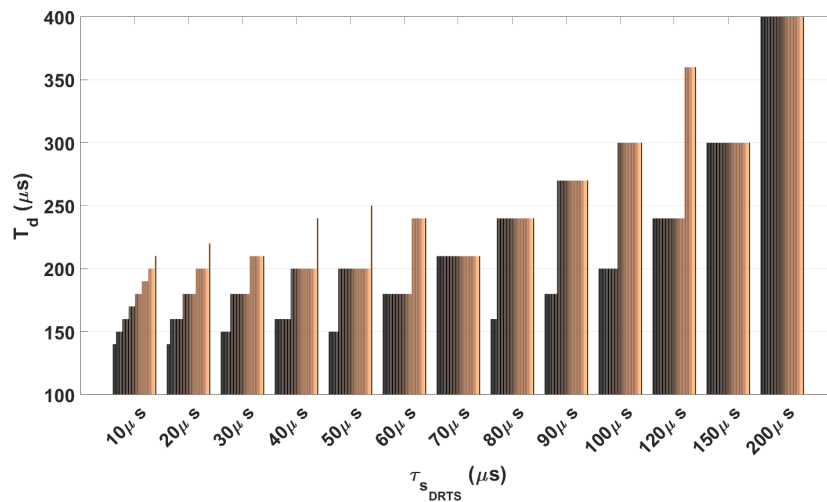


Fig. 3.15 Time delay variation distribution for theoretically assessed time synchronized signal.

3.6 Conclusions

In this Chapter, a detailed analysis and characterization of the time delay associated with PHIL simulations have been performed. Consequently, equations for accurately measure the total time delay in a PHIL simulation have been developed and validated through an experimental PHIL simulation. This allows for the identification of individual time delays as well as dynamic behaviours introduced into the simulations that can affect their accuracy and stability. Opposed to the general approach of assuming a constant time delay, the presented detailed characterization has led to the identification of a variable time delay in PHIL implementations with switched-mode PI, that has not been identified before. The impact that variable time delay introduces in accuracy and stability has been assessed, leading to conclude that this behaviour can adversely impact the stability and accuracy of PHIL simulations, and it could be associated with oscillatory behaviours detected on some PHIL simulations even when positive stability assessment results are obtained. With the knowledge acquired during the characterization of the time delay, the accuracy of stability and accuracy assessments of PHIL simulations is improved, reducing the risk of performing PHIL simulations. Furthermore, the detailed assessment

of the time delay has shown that the reduction of the time-step does not always reduce the total time delay when a switched-mode PI is used, as the time delay is variable and depends on the interaction between the fixed time-step components. An approach for mitigating the variability of time delay along with a novel method for eliminating the variability in PHIL simulations has been also presented, which can produce more accurate simulations and time delay compensation, improving PHIL simulations.

Chapter 4

Novel time delay compensation algorithm for enhanced accuracy of PHIL simulations

The associated time delay of PHIL implementations is an important characteristic that can bring PHIL experiments to experience poor accuracy results and instabilities. Therefore, it is of paramount importance to minimise the time delay and compensate for any amount that is still present after the reduction takes place, achieving accurate and stable PHIL simulations.

With this purpose, a novel time delay compensation algorithm has been developed and experimentally validated for PHIL simulations. The algorithm is based on phase shifting phase-by-phase and harmonic-by-harmonic (in the frequency domain) the signal of interest.

In this Chapter, a detailed description of the developed algorithm along with an evaluation of the impact that the introduction of the time delay compensation algorithm can bring to PHIL simulations in terms of stability and accuracy is presented.

4.1 Time delay compensation

Time delay compensation refers to the action of phase-shifting a signal by an amount equivalent to the desired time delay to be compensated. In this manner, when the phase-shift is applied, it results in the waveform being in phase with an ideal (non-delayed) waveform. For an accurate compensation not only the phase of the fundamental component is required but also the harmonic components need to be shifted appropriately.

In [CNH16; Hok+18], a lead filter is used for the compensation of the time delay; however, this compensation approach can present important limitations such as the amplification of high frequency components or the impossibility to compensate for any harmonic component, therefore being discarded for the compensation when harmonics are of interest.

For the implementation of a time delay compensation algorithm without assuming additional inductive components, the requirements are:

1. To have access to the waveform phase
2. The possibility to modify the phase

Compensation of the harmonic components brings the requirement of implementing a harmonic detection method for the identification of the components phase. Harmonic detection methods are well known from Active Power Filter (APF) applications as reported in [ABH07]. These methods are commonly divided into frequency domain and time domain methods, with the frequency domain methods based on Fourier Transforms.

From the different frequency domain harmonic detection methods presented in [ABH07], the recursive or Sliding Discrete Fourier Transform (SDFT) is preferred in comparison with the Discrete Fourier Transform (DFT), as the latter introduces high computational burden and presents a slower response. Also, when SDFT is compared against FFT, due (against the commonly held perception) to the improvement

in computation efficiency of the SDFT, an increase in the number of harmonics which can be processed is expected [Ros+11a].

From the time domain methods presented in [ABH07], the only method that meets the requirements for being a time delay compensation algorithm is the harmonic dq frame, as it is the only one in which the phases of the different components can be manipulated for applying the delay compensation technique.

Hence, SDFT and harmonic dq frame are the two recommended methods for the implementation of the time delay compensation. However, from these methods, the harmonic dq frame accuracy when unbalanced or very distorted signals are present is limited, furthermore the implementation under such a case would require of all positive, negative and zero sequence components which would greatly increase the calculation burden (even more when the number of harmonics increases). On the other hand, the limitation of the SDFT method is mainly the slow response under transient conditions, in which the transient will be filtered over the window period. Also, a careful implementation is required for an accurate performance as synchronization between the sampling and fundamental frequencies is required even under changing frequency conditions.

Both of the methods present similar response to transient events due to the filtering behaviour of both approaches; nonetheless, with the SDFT implementation requiring a per phase implementation, which results in an accurate response under unbalances and distortions, the SDFT method has been selected as the harmonic detection method for the implementation of the time delay compensation algorithm. Furthermore, dynamic phasors, such as the ones obtained with SDFT, are typically used in similar applications which could also benefit from the compensation, such as distributed real time simulations. The specific implementation along with the impact on stability that the addition of the SDFT algorithm has on the overall PHIL stability as well as the accuracy improvement introduced by the time delay compensation is presented in the

following subsections. Experimental validation of the algorithm is also performed for the acquisition of more realistic validation results.

4.2 SDFT-based time delay compensation algorithm

The time delay compensation algorithm has been developed such that it implements the compensation in a phase-by-phase and harmonic-by-harmonic manner, besides it is adaptive to variable frequency allowing for an appropriate response during frequency variations.

The compensation algorithm can be implemented similarly in the feed-forward and feedback path of the PHIL implementation, shifting either the voltage or current waveform used for the implementation of the interface between the simulation and the PI and HUT (when ITM IA is used). The implementation can also differ depending on the particular characteristics of the selected PHIL implementation, as some can have phasors being exchanged at the interfaces and some other will be exchanging time domain waveforms. However, in both cases a time to frequency domain transformation is required.

For achieving high accuracy and adequate computational performance, the time to frequency domain transformation is performed using an SDFT algorithm, which will grant access to the phase of the components. The algorithm is hosted as part of the switched-mode power amplifier control algorithm (if other types of PI are used it could also be hosted at the DRTS). An example of the developed time delay compensation algorithm in a PHIL simulation is presented in Fig. 4.1. Here, the compensation is taking place at the feed-forward path, compensating the waveform received from the DRTS by phase-shifting the waveform after performing the SDFT function. Before sending it to the controller of the PI for amplification, the new setpoint signal is transformed back into the time domain (depending on the control algorithm this step could be omitted).

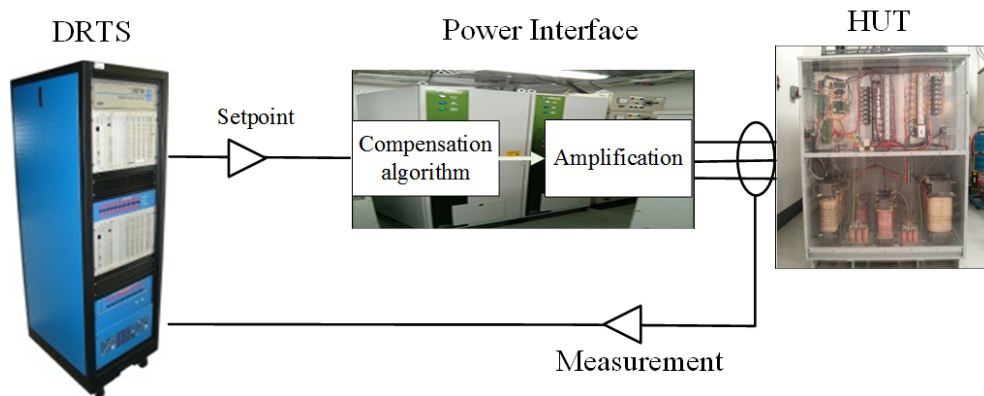


Fig. 4.1 PHIL with compensation algorithm

A diagram of the implemented compensation algorithm is presented in Fig. 4.2, where it can be observed that it is divided into two processes: (a) SDFT process and (b) waveform reconstruction. Below, a detailed description of these processes is presented.

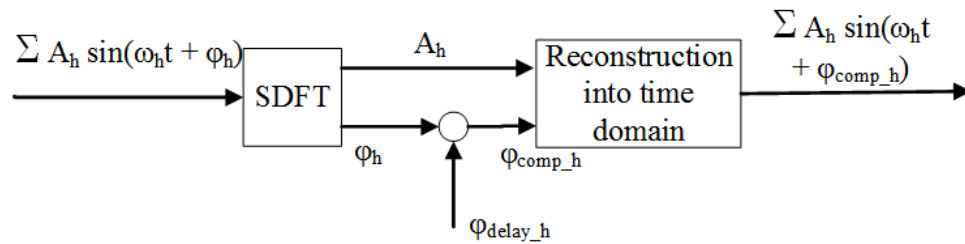


Fig. 4.2 Compensation algorithm diagram.

4.2.1 Sliding DFT algorithm

For the PHIL implementation, the requirement is to measure a number of harmonics with low spectral leakage, with a variable fundamental frequency, and with a measurement update rate that matches the frame rate of the interface controller. While it is possible to make such measurements using an FFT process [Cha+08], it requires re-execution of the entire FFT every time a new sample is acquired. By contrast, and perhaps counter-intuitively, a bank of parallel DFT processes can be constructed to produce the same measurements with a lower computational cost per frame, if the DFT code

is carefully constructed using rolling memory buffers [Ros+11a; GRB15], effectively forming a sliding or recursive DFT algorithm [JL03]. Use of a parallel DFT bank allows an increased number of harmonics to be processed, increasing the accuracy of the simulation.

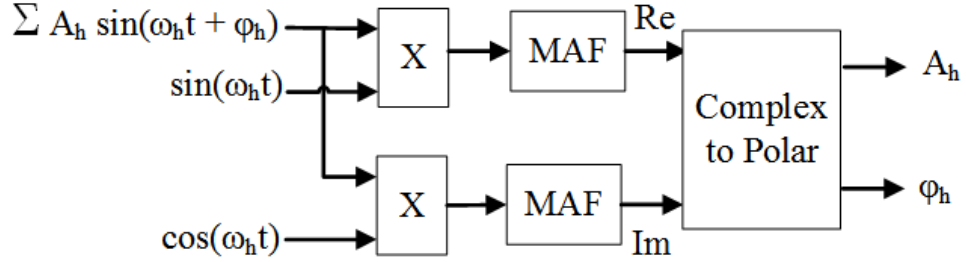


Fig. 4.3 SDFT algorithm diagram.

The implementation of the SDFT algorithm is presented in Fig. 4.3, where the convolution of the input signal with the sine and cosine of the selected harmonic frequency is filtered with a moving average filter (MAF) with a window length of one cycle of the selected frequency. The complex components are then transformed into polar form for performing the time delay compensation in the frequency domain.

The MAF can be represented in the continuous time domain as:

$$\begin{aligned} y(t) &= \frac{1}{T_w} \int_{t-T_w}^t x(t) dt \\ &= \frac{1}{T_w} \left(\int_0^t x(t) dt - \int_0^{t-T_w} x(t) dt \right) \end{aligned} \quad (4.1)$$

where $x(t)$ is the input to the MAF and $y(t)$ the output. T_w is the window length of the MAF. However, in practice, a discrete implementation is utilized which based on Eq. 4.1 results in:

$$y(k) = \frac{1}{N} \sum_{i=0}^{N-1} x(k-i) \quad (4.2)$$

where N is the number of samples within the window length T_w , which can be calculated as $N = T_w/T_s$, with T_s being the sampling period.

The main limitation of the MAF arises when the frequency of the input signal varies, leading to a non integer number of samples and hence to a lower accuracy of the process if no approach is taken for solving it. In the developed algorithm, an approach based on linear interpolation presented in [RB16] is implemented, by which the averaging window will be adaptive and exactly one cycle of the fundamental frequency.

4.2.2 Compensation and waveform reconstruction

For an accurate compensation, the phase compensation term, φ_{delay_h} , to be applied also needs to be adaptive to frequency, this can be illustrated as:

$$\varphi_{delay_h} = T_d \cdot 2 \cdot \pi \cdot f_h \quad (4.3)$$

where the frequency f_h is the actual measured frequency rather than a fixed nominal frequency. If this is assumed constant, after frequency variations a steady-state error will be present. This is further analysed in Section 4.4.

The reconstruction of the waveform into the time domain is performed using the trigonometric identity:

$$\sin(a + b) = \sin(a)\cos(b) + \sin(b)\cos(a) \quad (4.4)$$

by selecting $a = w_h t$ and $b = \varphi_{comp_h}$. In this way, the reconstruction of the waveform for each phase can be described as:

$$\sum_{h=1, \dots, N} A_h \sin(w_h t + \varphi_h) = \sum_{h=1, \dots, N} A_h (\sin(w_h t)\cos(\varphi_{comp_h}) + \sin(\varphi_{comp_h})\cos(w_h t)) \quad (4.5)$$

where the subscript h refers to each individual harmonic component being compensated, and $\sin(w_h t)$ and $\cos(w_h t)$ are the same pre-computed values used for the SDFT.

4.3 Compensation algorithm considerations on stability of PHIL

The time delay compensation algorithm has been mainly developed for the improvement of the simulation accuracy. However, the effect that this algorithm can bring to the stability of PHIL implementations also needs to be considered.

For the assessment, the transfer function of the SDFT algorithm used is considered equivalent to the transfer function of a moving average filter, which can be defined in the continuous domain as [Peñ+17; RB16]:

$$G_{SDFT}(s) = \frac{1}{T_w} \left(\frac{1}{s} - \frac{e^{-T_w s}}{s} \right) = \frac{1 - e^{-T_w s}}{T_w s} \quad (4.6)$$

where T_w is the length of the SDFT window. However, in this case the combination of the SDFT with the reconstruction needs to be considered. This is as a result of the Fourier transform "frequency-shifting" property by which the input signal is shifted by $-f_h$. This can clearly be observed in the plotted magnitude response of the SDFT transfer function presented in Fig. 4.4, where $0dB$ is applied to DC (0 harmonic) rather than the fundamental. With the reconstruction, the signal is brought back to the input signal frequency domain by applying a positive frequency shift f_h as shown in Fig. 4.5.

Therefore, the process of shifting up and down the frequency of the signal is equivalent to shifting up in frequency the SDFT transfer function by f_h as shown in 4.5, resulting then in an accurate interpretation. The frequency shift of the SDFT transfer

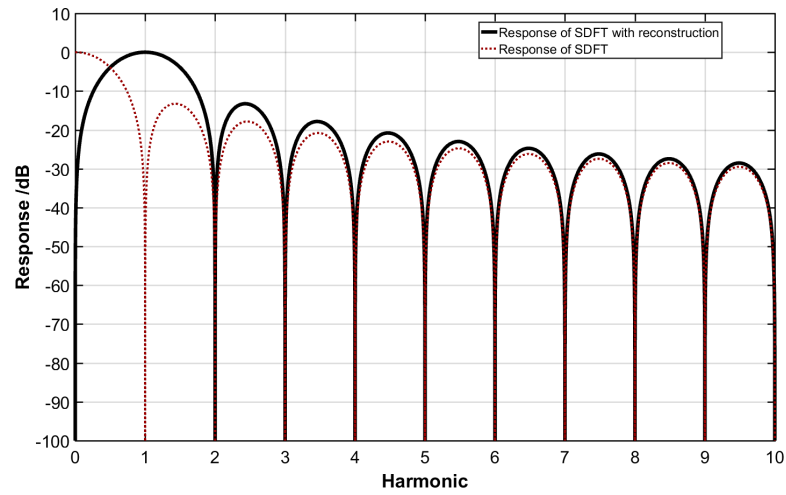


Fig. 4.4 Frequency response of SDFT and SDFT with reconstruction.

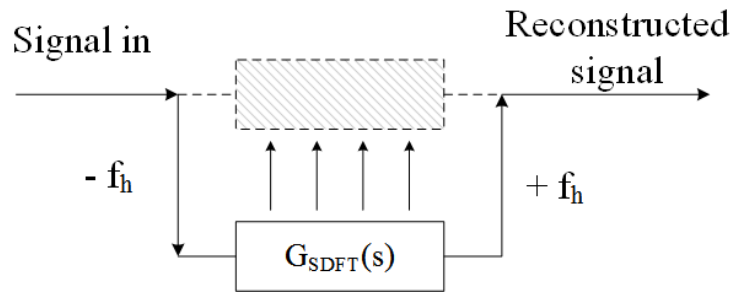


Fig. 4.5 SDFT frequency shift diagram.

function is performed by using the frequency shifting property, which is illustrated as:

$$x(t) \Leftrightarrow X(s) \quad (4.7)$$

$$x(t)e^{s_0 t} \Leftrightarrow X(s - s_0) \quad (4.8)$$

in this case,

$$s_0 = j2\pi f_h \quad (4.9)$$

which leads to a transfer function for the SDFT with reconstruction described by:

$$G_{SDFT+R}(s) = \frac{1}{(s - j2\pi f_h)T_w} \left(1 - e^{-(s - j2\pi f_h)T_w} \right) \quad (4.10)$$

This is further analysed by plotting the frequency response of the SDFT transfer function with the frequency shifted and without. As can be seen in Fig. 4.4, when the shifting is not considered only the DC component (0 harmonic) will be passed with the other components filtered out; however, when the transfer function is shifted, the fundamental component is the one presenting 0 dB gain. This is the performance expected from the compensation algorithm, confirming the appropriateness of the shifted SDFT transfer function for this case.

The time compensation can also be added to Eq. 4.10, resulting in

$$G_{SDFT+R+C}(s) = \frac{1}{(s - j2\pi f_h)T_w} \left(1 - e^{-(s-j2\pi f_h)T_w}\right) \cdot e^{j2\pi f_h T_d} \quad (4.11)$$

However, if multiple harmonic components are being analyzed with parallel SDFT functions, the representative transfer function is then described by the sum of each component transfer function as:

$$G_{SDFT+R+C_h}(s) = \sum_{h=1, \dots, N} \frac{1}{(s - j2\pi f_h)T_w} \left(1 - e^{-(s-j2\pi f_h)T_w}\right) \cdot e^{j2\pi f_h T_d} \quad (4.12)$$

where h is the number of harmonics to be processed by the DFT.

The assessment of the impact on stability that the addition of the SDFT process brings into the PHIL is performed by comparing the open loop frequency response of a typical PHIL implementation with one where the SDFT is added with different harmonic components being processed.

In Fig. 4.6, the SDFT transfer function is introduced into the V-ITM PHIL control loop (the PI is assumed ideal for simplification purposes, hence the gain of the power interface is assumed equal to 1). The open loop transfer function can be represented as:

$$H_{OL_SDFT}(s) = H_{delay}(s) \cdot H_{DRTS}(s) \cdot H_{HUT}(s) \cdot G_{SDFT_h}(s) \quad (4.13)$$

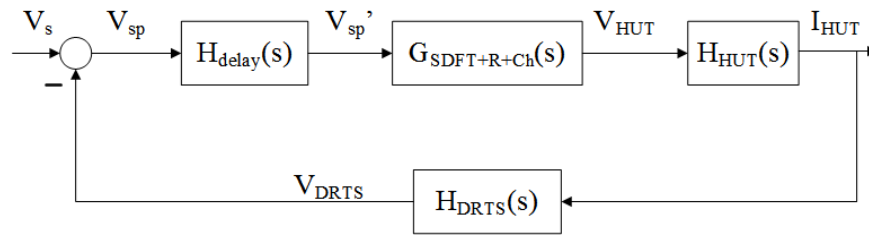


Fig. 4.6 Control loop diagram of PHIL with V-ITM and time delay compensation.

where

$$H_{delay}(s) = e^{-sT_d}$$

$$H_{DRTS} = Z_{DRTS}(s)$$

$$H_{HUT} = \frac{1}{Z_{HUT}(s)}$$

A simple scenario is used for performing the stability assessment of the open loop transfer functions, with both DRTS and HUT impedances being resistive-inductive components, and with the parameters of time delay and window period for the SDFT presented in Table 4.1.

Table 4.1 Component values for Nyquist diagram

Component	Value
R_{DRTS}	0.5Ω
L_{DRTS}	$3mH$
R_{HUT}	1Ω
L_{HUT}	$1mH$
T_w	$0.02s$
T_d	$400\mu s$

Nyquist plots of the open-loop frequency response for transfer functions with different number of compensated harmonic components are presented in Fig. 4.7, where it can be noted that by adding the SDFT function of only the fundamental component, the improvement in gain and phase margin is prominent, bringing the system to stability

with a large gain margin in comparison with the conventional PHIL implementation. However, as the number of harmonic components processed increases gain and phase margin improvement is reduced, being closer to encircle the point $(-1,0)$ as in Fig. 4.7(d), although in this case the performance is still improved under all the scenarios presented.

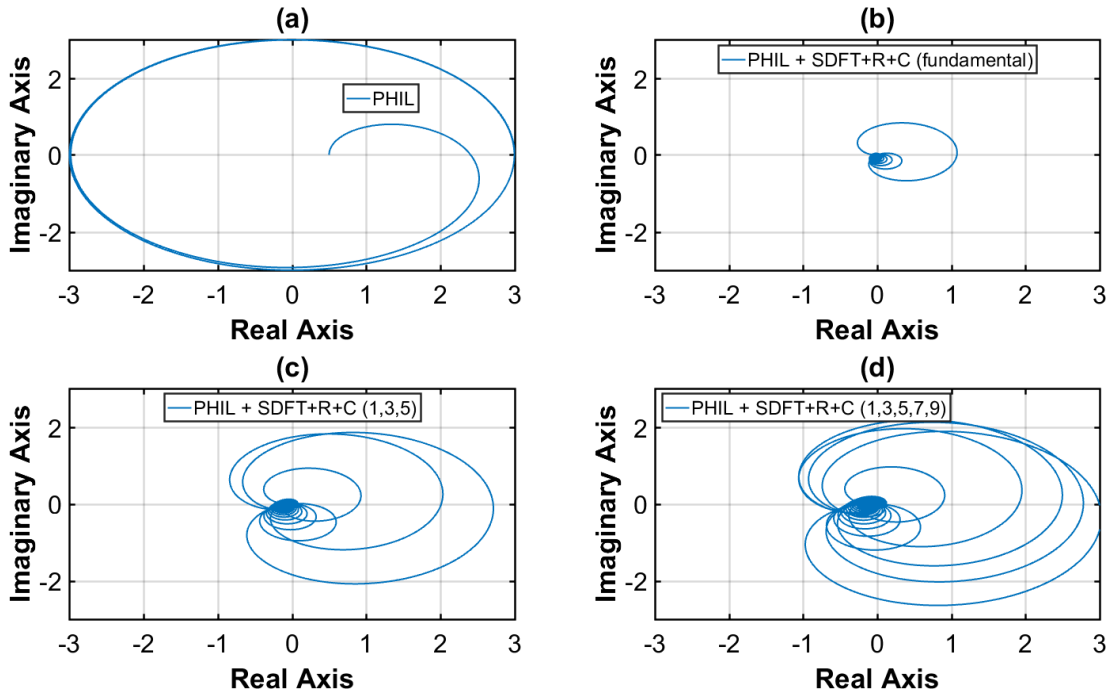


Fig. 4.7 Nyquist diagram of: (a) Typical PHIL, (b) PHIL with SDFT of fundamental frequency, (c) PHIL with parallel SDFT of fundamental and 3rd and 5th harmonics, (d) PHIL with parallel SDFT of fundamental, 3rd, 5th, 7th, 9th harmonics.

Furthermore, the addition of the compensation can also affect to the stability of the PHIL simulation. This is analysed in Fig. 4.8, where the Nyquist plots of the same configurations with and without the compensation action are presented. The compensation presents minor effects when low order harmonics are analysed; however, as the harmonic order increases the positive impact of the compensation addition is evident as shown in Fig. 4.8(d).

Nevertheless, compensation of large number of harmonics can also worsen the performance, in this case it has been identified that if all the odd harmonics up to the

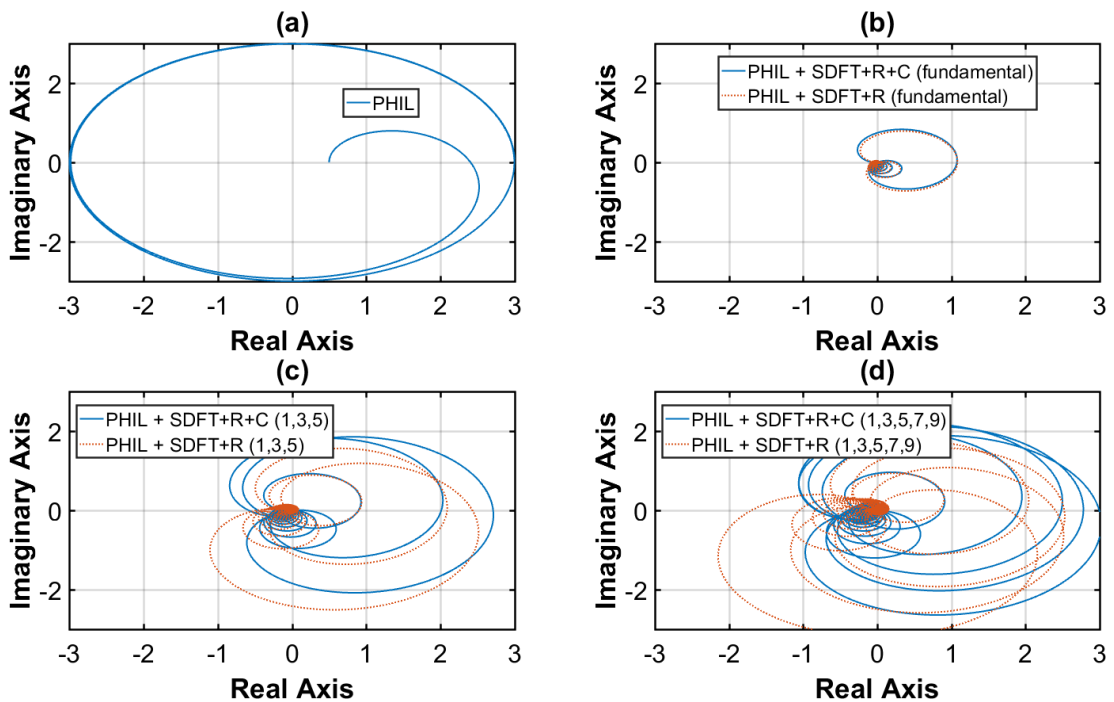


Fig. 4.8 Nyquist diagram comparison with compensation added of: (a) Typical PHIL, (b) PHIL with SDFT of fundamental frequency, (c) PHIL with parallel SDFT of fundamental and 3rd and 5th harmonics, (d) PHIL with parallel SDFT of fundamental, 3rd, 5th, 7th, 9th harmonics.

55th are processed but not compensated, the performance is then slightly deteriorated compared with Fig. 4.7(a), as can be observed in Fig. 4.9(b), however if only the 55th is required then the response will still be improved compared with the scenario without SDFT compensation.

Therefore, the improvement on stability that the addition of SDFT brings depends on the list of components as well as the specific harmonic component to be compensated (with the higher harmonics reducing the improvement).

In addition to the theoretical stability assessment, a time domain simulation has also been performed with the aforementioned parameters presented in Table 4.1 and the configuration of Fig. 4.10. This configuration contains a $230V_{rms}$ single phase, 50Hz voltage source. The time delay has been equally divided to represent the delay present in the feed-forward and feed-back path.

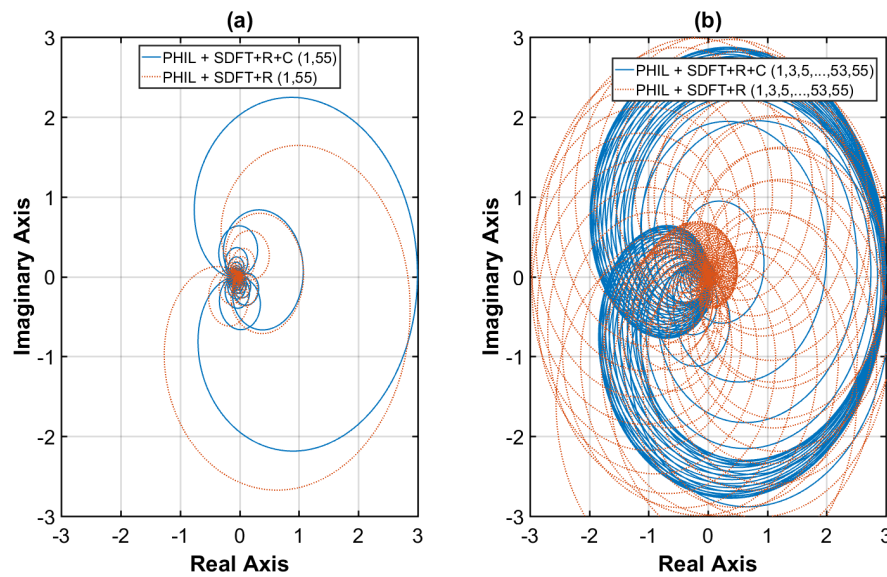


Fig. 4.9 Nyquist diagram of PHIL with and without compensation of: (a) fundamental and 55th, (b) odd harmonics up to the 55th.

The results are presented in Fig. 4.11, where the addition of the SDFT algorithm to the PHIL implementation as suggested from the theoretical results improves the stability, in this case bringing the unstable PHIL system to stability, reinforcing the results obtained from the Nyquist evaluation of the transfer functions. Nonetheless, in Fig. 4.11(d) the system goes unstable even when in Fig. 4.7(d) the point $(-1,0)$ is not encircled. This can be due to the very low gain and phase margin present in the system. For similar systems where the ratio of impedances is a deciding factor for the stability of the system, more restrictive stability criteria is typically applied (such as the Middlebrook criteria, Gain Margin Phase Margin (GMPPM) or Energy Source Analysis Consortium (ESAC) [RS14]).

The improvement of the stability presented is mainly due to the filtering characteristics of the SDFT, however this may also bring some accuracy implications which are considered in Section 4.4.

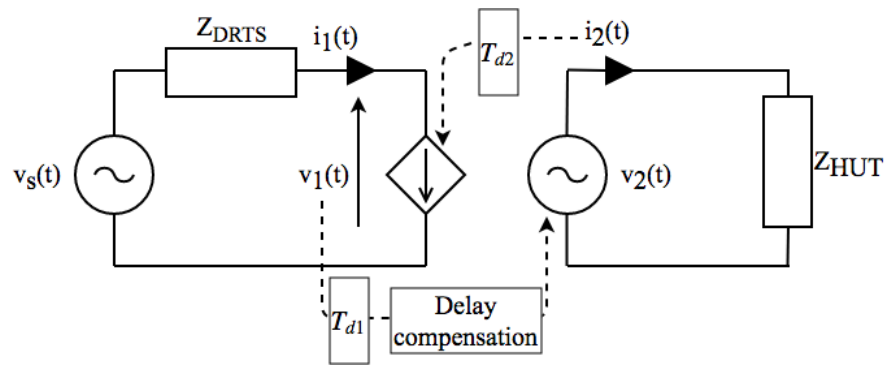


Fig. 4.10 Simulation model with compensation algorithm

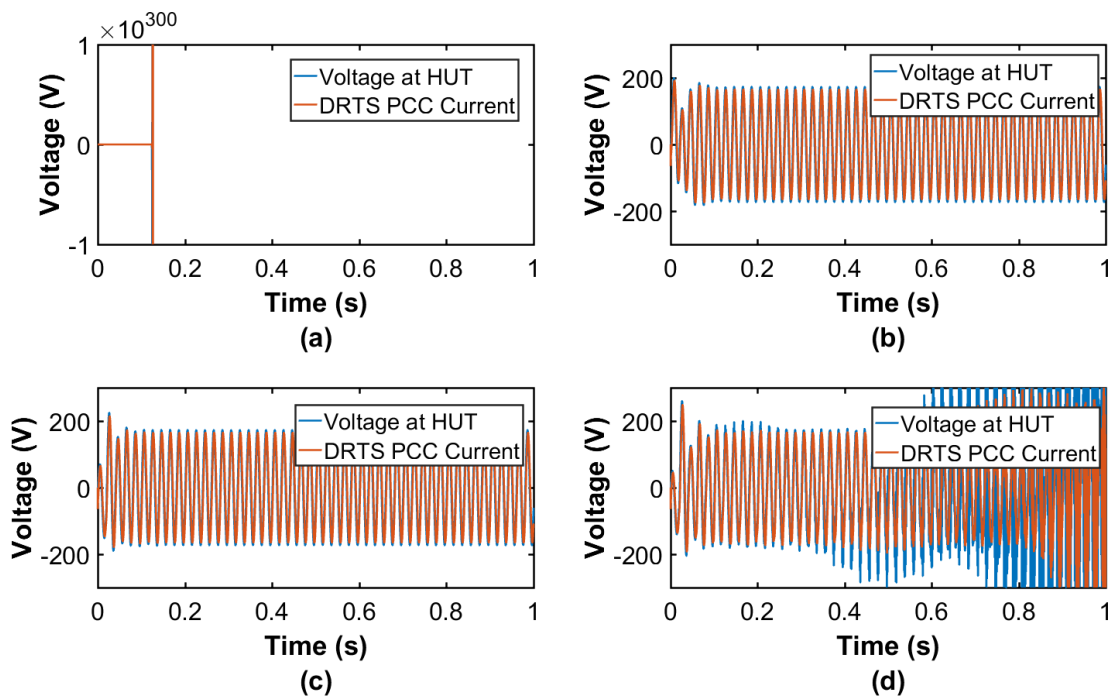


Fig. 4.11 Simulation results for: (a) PHIL without SDFT, (b) PHIL with SDFT of fundamental frequency, (c) PHIL with SDFT of fundamental and 3rd and 5th harmonics, (d) PHIL with SDFT of fundamental, 3rd, 5th, 7th, 9th harmonics.

4.4 Accuracy performance of the time delay compensation algorithm

For the accuracy performance evaluation of the proposed time delay compensation algorithm, the simplified PHIL scenario (voltage divider system) of Fig. 4.10 is also used.

The simulation assessment of the time delay compensation algorithm is performed with three different configurations, which are:

1. An ideal implementation in which no time delay or interface is present, i.e. a monolithic implementation. This configuration consists of a $230V_{rms}$ single phase, $50Hz$ voltage source; $Z_{DRTS} = 0.1\Omega$ and $Z_{HUT} = 1\Omega$; and a simulation time step of $10\mu s$. For the ideal implementation $i_1(t) = i_2(t)$ and $v_1(t) = v_2(t)$.
2. A PHIL implementation without time delay compensation algorithm, i.e. a conventional PHIL implementation. The power interface is assumed ideal and therefore with unity gain, although a time delay of $T_{d1} = 200\mu s$ is assumed to be present at the interface and $T_{d2} = 200\mu s$ at the feed-forward path.
3. A compensated PHIL configuration where the time delay compensation algorithm will phase shift the waveform by the amount of time delay existing in the system, $400\mu s$ (0.04π radians). The compensation algorithm is implemented in the feed-forward path and it is simulated with a $100\mu s$ time step, similar to the capabilities of typical switched-mode power amplifiers.

The accuracy performance of the three implementations is evaluated under four different scenarios, which are:

- Steady-state at nominal frequency
- Voltage step

- Harmonic voltage step
- Frequency ramp

4.4.1 Steady-state at nominal frequency

The simulation results from the implementation described in Fig. 4.10 when the system is at steady-state are presented in Fig. 4.12. In Fig. 4.12(a) the compensated and ideal currents are in phase, however the current from the PHIL implementation without compensation algorithm has a phase offset introduced by the time delay. Furthermore, in Fig. 4.12(b), the error of both implementations is presented as the Root Mean Square Error (RMSE) between each implementation and the ideal one. The compensated waveform error is mainly produced as a result of the slower time-step used by the compensation algorithm to more realistically emulate its implementation within a switched-mode power amplifier, this can be further observed in Fig. 4.13. The implementation without compensation, apart from the delay due to the time step of the interface, presents a larger error as the time delay of the PHIL implementation is not compensated.

If the time delay is increased, the uncompensated waveform error would escalate proportionally; however, the compensated case would remain the same for all scenarios of time delay as long as the delay is accurately determined.

4.4.2 Voltage step

A voltage step scenario has been identified for the assessment of the time delay compensation accuracy under transient conditions. A 10% voltage step up is produced at $t = 2s$ in the simulation. In Fig. 4.14(a), at $t = 2s$ the compensated current is no longer in phase or with equal amplitude as the ideal implementation. In fact, the compensated implementation requires of one cycle of the fundamental frequency to achieve steady-state accuracy, this being caused by the windowing of the SDFT function, which

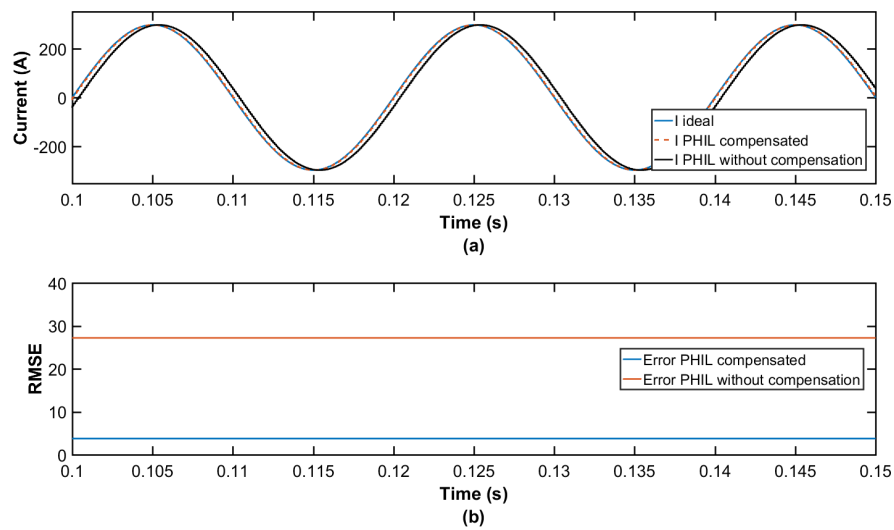


Fig. 4.12 Simulation results at steady state. (a) Steady-state current waveforms, (b) error measurement.

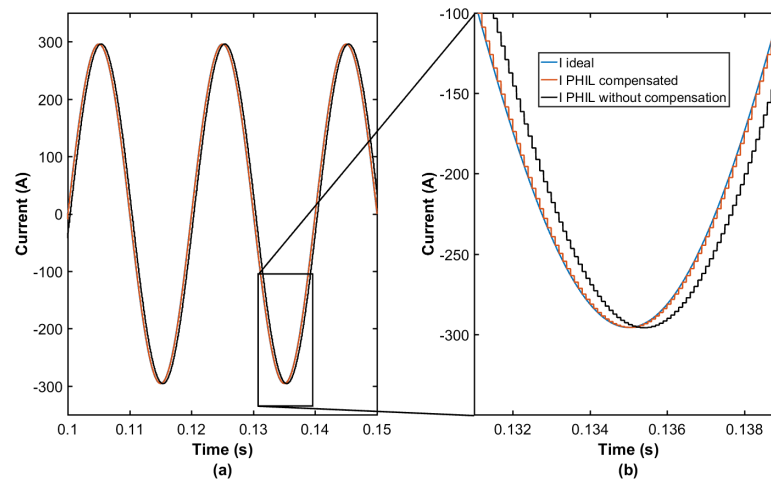


Fig. 4.13 Detail of the time delay at steady-state. (a) Currents, (b) zoomed currents.

filters the step over the window period. Although in Fig. 4.14(b) the error settles after two periods, this is only due to the Root Mean Square (RMS) calculation that adds an extra averaging period. The response of the implementation without compensation presents almost no delay to the step but as can be observed from Fig. 4.14(b), even if the response is considerably faster than the compensated implementation, because of the time delay, the error that presents is still higher than the compensated implementation.

This is an important factor to account for when the implementation of the compensation is considered, as typically the "slow" response of the SDFT can be regarded as its main drawback; nevertheless, the obtained results suggest that even if the response is slower the accuracy is still improved.

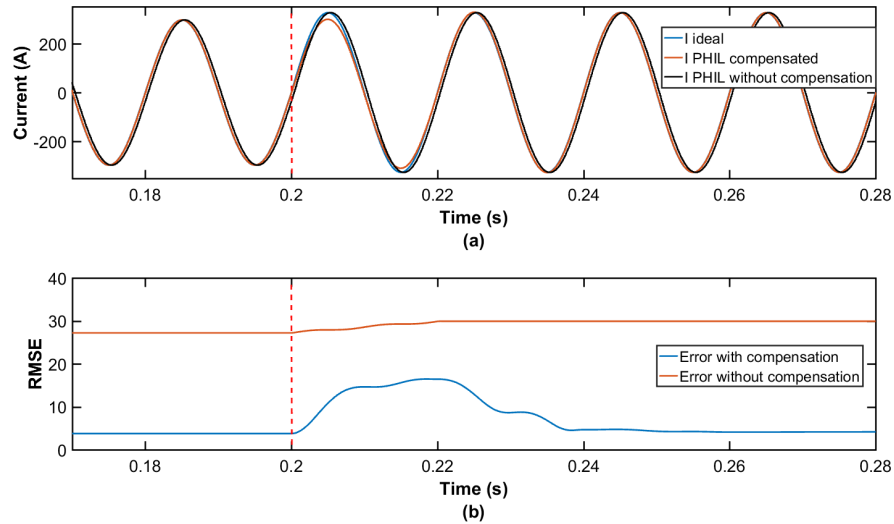


Fig. 4.14 Response of the PHIL implementation to a voltage step. (a) Current responses, (b) error measurement.

4.4.3 Harmonic voltage step

One of the main objectives of the developed time delay compensation algorithm is to compensate harmonic components in order to improve the accuracy of PHIL simulations with presence of harmonics in the system. Accordingly, a voltage harmonic source is implemented in this scenario, which introduces 5^{th} and 7^{th} harmonic components with an amplitude equal to a 10% of the fundamental component amplitude. Harmonic compensation of these components is applied in the compensation algorithm.

In Fig. 4.15, similarly to the previous scenarios, the effect of the step on the currents and the resultant measured error is presented. Complementary results to the voltage step scenario are obtained for the compensated PHIL implementation, where

after one cycle the only error is due to the time-step. Again, even during the less accurate first cycle of the time delay compensation algorithm during a transient, the compensated implementation accuracy is improved with respect to the not compensated implementation.

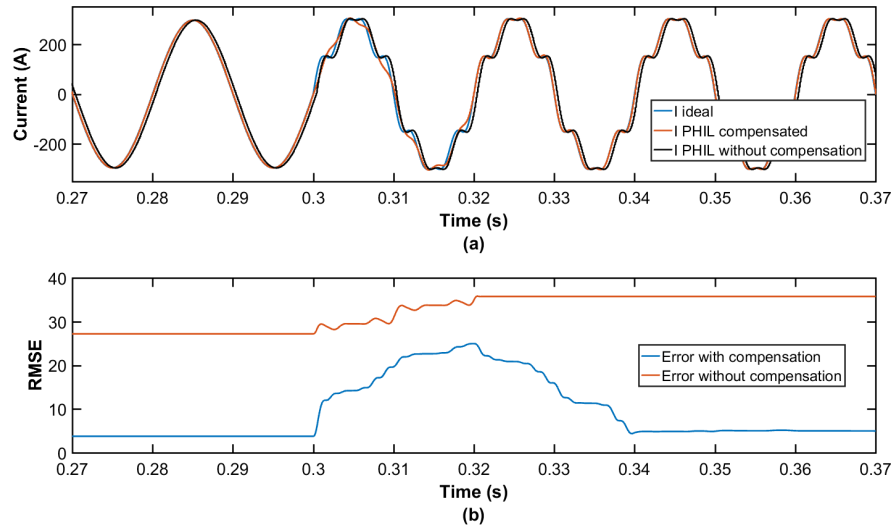


Fig. 4.15 Response of the PHIL implementation to harmonic component step. (a) Current responses, (b) error measurement.

4.4.4 Frequency ramp

In this scenario the frequency adaptability of the time delay compensation algorithm is studied. The algorithm requires of an accurate frequency measurement in order to precisely compensate, therefore in this case a direct frequency signal has been provided for the purpose of accurately evaluate the compensation algorithm avoiding inaccuracies introduced by other processes. Frequency ramp-down and ramp-up events are simulated for this assessment.

The frequency ramp-down event brings the frequency from 50Hz to 49.5Hz in 0.628s as shown in Fig. 4.16(b). Similarly to the previous scenarios, the error introduced by the compensated waveform is reduced compared with conventional PHIL implementations

as shown in Fig. 4.16(a). Furthermore, the adaptive frequency characteristic of the algorithm allows for an increased accuracy during the frequency event as illustrated in Fig. 4.16(a).

An equivalent frequency ramp-up event is simulated and the results presented in Fig. 4.16. As can be observed in Fig. 4.16(a), when a non frequency adaptive algorithm is used, a frequency offset will remain after the frequency event takes place, and depending on the settling frequency value the deviation can vary. These results expose the importance of the frequency adaptability in the compensation algorithm.

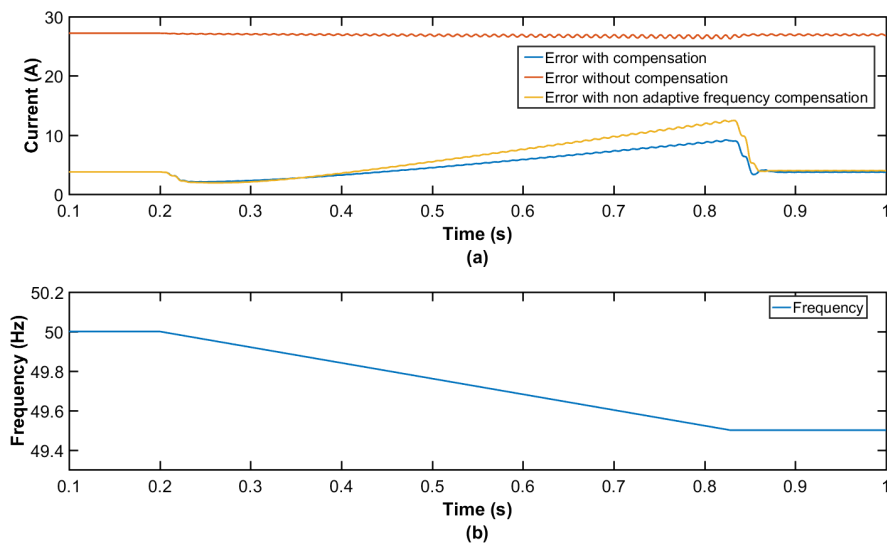


Fig. 4.16 Simulation results for a positive frequency deviation. (a) Error measurement, (b) frequency deviation.

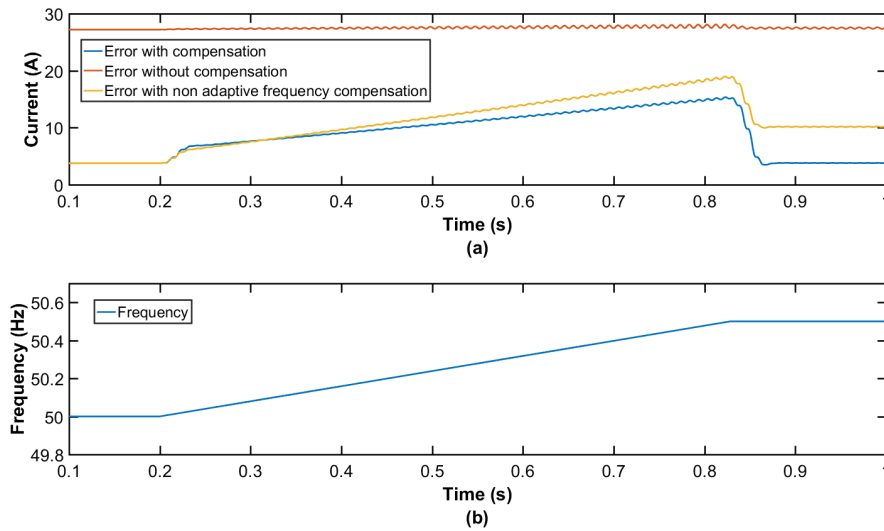


Fig. 4.17 Simulation results for a negative frequency deviation. (a) Error measurement, (b) frequency deviation.

4.5 Time delay compensation algorithm experimental validation

Experimental demonstration of the effectiveness of the time delay compensation algorithm developed is presented in this section.

Similarly to the simulation assessment, steady-state and transient scenarios are evaluated. Furthermore, the time delay of the configuration along with the computational performance of the algorithm are also assessed.

4.5.1 Experiment configuration

The PHIL configuration presented in Fig. 4.18 has been implemented in the Dynamic Power Systems Laboratory (DPSL) of the University of Strathclyde. The hardware components used for the validation are described below.

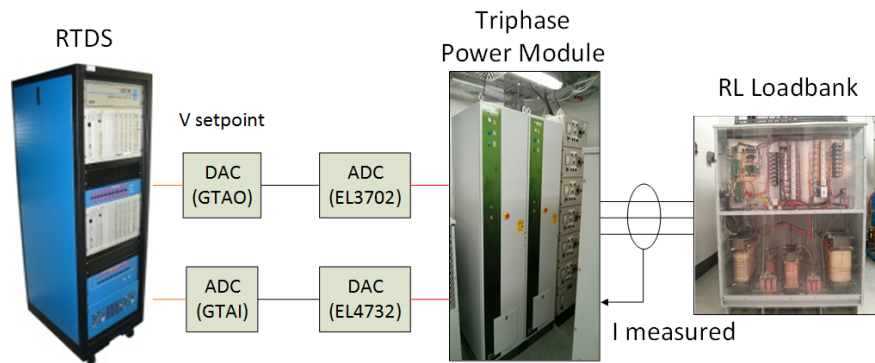


Fig. 4.18 PHIL experimental setup with analog communication interface.

DRTS

Similarly to Chapter 3, an RTDS unit is used for the simulation section of the PHIL implementation. For this experiment the time step of the simulation ($\tau_{s_{DRTS}}$) has been selected as $50\mu s$.

The processor cards used for this experiment are PB5 cards, each card containing two processors. The I/O cards required for the interconnection with external hardware are assigned to a specific processor. In this case, an analog communication link is used with the ADC function being performed by a GTA0 card with 12 optically isolated output channels. The inputs are processed with a GTAI card with 12 input channels. For the purpose of this experiment only 3 outputs and 3 inputs channels are used.

V-ITM interface algorithm is used for the experimental validation, hence the output signals are the 3-phase voltage measured at the simulation PCC, and the input signals are the 3-phase currents measured at the HUT PCC, the latter being introduced as reference to a controlled current source for electrically coupling the subsystems.

A reduced power system model composed of an infinite voltage source and a small impedance ($Z_{DRTS} = 0.026\Omega/phase$) has been used for performing the experimental validation.

Switched mode Power Amplifier

The power amplifier is a 90kVA, three phase and neutral, back-to-back power converter. This switched-mode AC/DC/AC power converter is connected to the laboratory grid network for reproducing the reference voltage, as shown in Fig. 4.19. The AC/DC converter is controlled to maintain a constant DC voltage in the DC bus. The DC/AC converter is the component controlled with the signals from the DRTS, as the output of this element will try to replicate the voltage signal taken as reference. In the scenario studied here it is not necessary to have bidirectional converters as the HUT will be a resistive load bank. However, the power converters of the power amplifier have bidirectional power flow capabilities, although this will only be required in cases where the HUT allows for bidirectional power flow.

The power amplifier switching frequency is set to 8kHz, although a double update of the PWM signal is used, having a control frequency of 16kHz. The reference signal from the DRTS is received into the control by ADCs inside the power amplifier; the measurement of the response of the HUT is also measured inside of the power amplifier and sent to the DRTS through ADC components. In this case due to the control algorithm requiring of more than one time-step to provide the duty cycle calculations, an extra time-step is provided for the calculations, which results in the response of the converter to the measured data to be applied one time-step later.

HUT

The HUT is a 3-phase variable load bank that in this case will be set to 9.06kW at 400V line-to-line. This means that the load will be of $17.51\Omega/phase$ with a tolerance of $\pm 5\%$ as per manufacturer specifications.

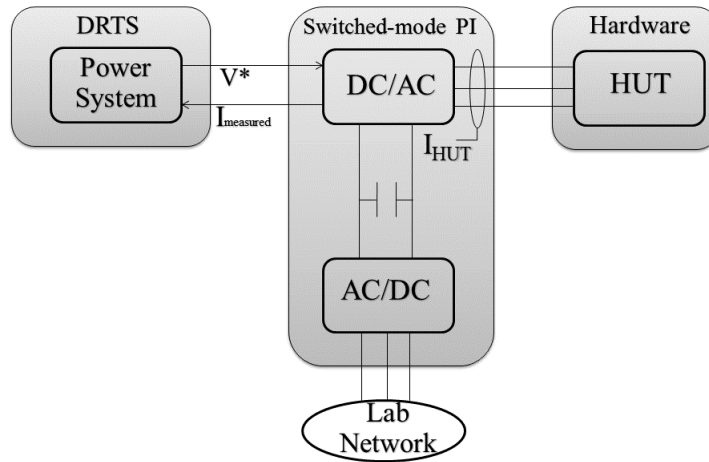


Fig. 4.19 Switched-mode power amplifier configuration.

4.5.2 Performance characteristics

Time delay

The time delay characteristics of this PHIL configuration have been analysed in Chapter 3, section 3.4.3, with an analog communication link. The characterization resulted in a time delay of $T_d = [350, 400, 1]$, measured theoretically and experimentally.

For the confirmation of the results obtained in Chapter 3 and for selecting a parameter for the compensation of time delay, the phases of the fundamental components have been analysed by performing an off-line Fourier calculation to a 0.5s waveform during steady-state. The calculation has been performed for a PHIL implementation and for a monolithic implementation for the comparison of the results. This has resulted on an average phase difference for the PHIL implementation of $\varphi_{delay} = 7.8^\circ$, while for the monolithic implementation this results in $\varphi_{delay} = 0.9^\circ$ due to the current signal being received one time-step later than the voltage (hence the 0.9° equivalent to one time-step ($50\mu s$)). Therefore the total delay that will be compensated for this

section is $\varphi_{delay} = 7.8 - 0.9 = 6.9^\circ$ or $\varphi_{delay} = 383\mu s$. As expected, the total delay to be compensated is within the characterized delay $T_d = [350, 400, 1]$, confirming the characterization results.

Computational performance

The maximum number of harmonics that can be compensated for a three phase signal with the selected PHIL configuration is analysed in this section. The number of harmonics that can be compensated in this configuration depends mainly in three factors, the time-step of the control, the complexity of the control algorithm implemented and the memory capabilities of the controller platform.

In this case, the converter control algorithm itself (not including compensation) requires of approximately $75\mu s$ for calculating new duty cycles for the converter, which requires of an extra cycle (as the control period is $T_c = 62.5\mu s$). The inverter will still be controlled at the set sample time; however, the response to the measurement data is postponed to the next period. This circumstance leaves approximately $50\mu s$ for the implementation of the compensation algorithm, although the converter requires of a minimum 10% margin for a safe operation. Therefore, a total of $43.75\mu s$ are available for the compensation algorithm. Under this situation, compensation of up to 43 components in three phases independently have been successfully achieved in terms of computation time, i.e. $1/3\mu s$ per single phase SDFT component processed. Nevertheless, limitations in the converter bandwidth would apply when high frequency harmonics are wanted to be reproduced, in this case the converter is only able to reproduce up to the 21st harmonic component and therefore this PHIL implementation is more limited by the power amplifier technical specifications rather than by the addition of the time delay compensation algorithm.

4.5.3 Steady-state experimental validation

Fundamental frequency component only

At steady state, the HUT consumes approximately $9060W$ and $0VAr$. Accordingly, it is expected that voltages and currents are in phase and the power exchanged equivalent to the load consumption. Phase a of the current of the PHIL implementation with the time delay compensation algorithm is presented in Fig. 4.20 (a), where the use of the compensation algorithm leads to an accurate current waveform as compared with the ideal implementation. However, as shown in Fig. 4.20 (b), when the time delay is not compensated, the PHIL implementation phase differs to that of an ideal (monolithic) implementation, with the phase difference being equal to the time delay. Therefore, the time delay compensation algorithm improvement will always be relative to the amount of time delay present on the system.

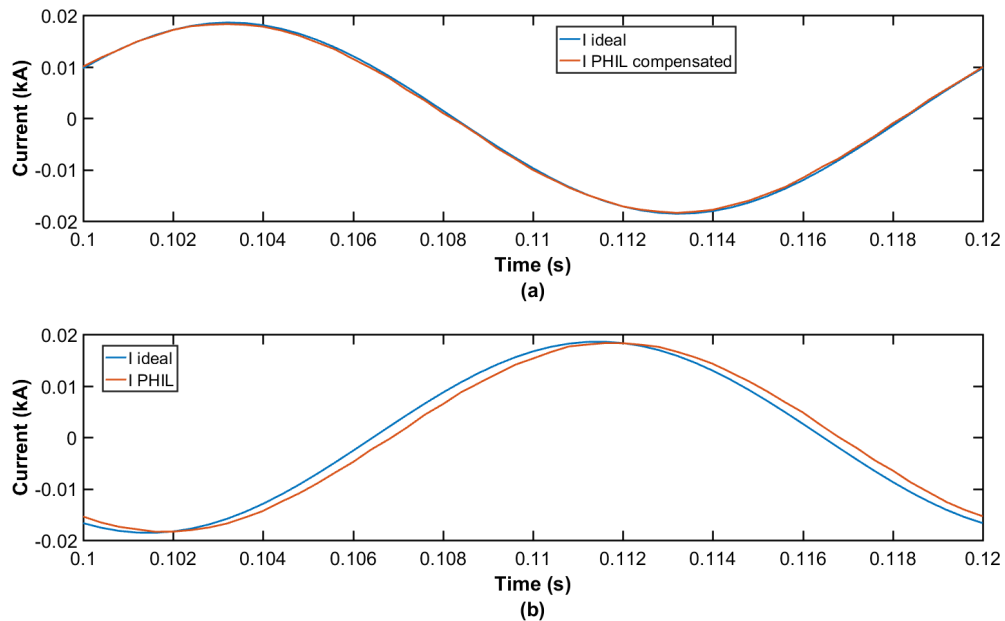


Fig. 4.20 Experimental measured currents at steady state.

The implication that this relatively small phase difference (6.9 degrees equivalent to $383\mu s$) has in the perceived powers at the simulation PCC is presented in Fig. 4.21. The

active power consumption from the load as seen from the simulation PCC is presented in Fig. 4.21 (a) and (b), where for the compensated case is of approximately $8950W$, which is within the 5% tolerance of the load. For the not compensated PHIL the active power is slightly reduced to approximately $8850W$ but still similar to the ideal active power. Nevertheless, the main impact is produced in the reactive power, as shown in Fig. 4.21 (c) and (d), where the PHIL without compensation is apparently consuming $1400Var$, which is certainly erroneous. On the other hand, the compensated implementation remains alongside the ideal result.

This is an important aspect that accentuates the importance of the compensation. For instance, the validation of the performance of a power converter with a voltage control algorithm in a PHIL implementation without time delay compensation would result in erroneous results, and similarly many other cases in which the exchanged powers between the simulation and hardware affects to the dynamics of the system and are within the validation scope.

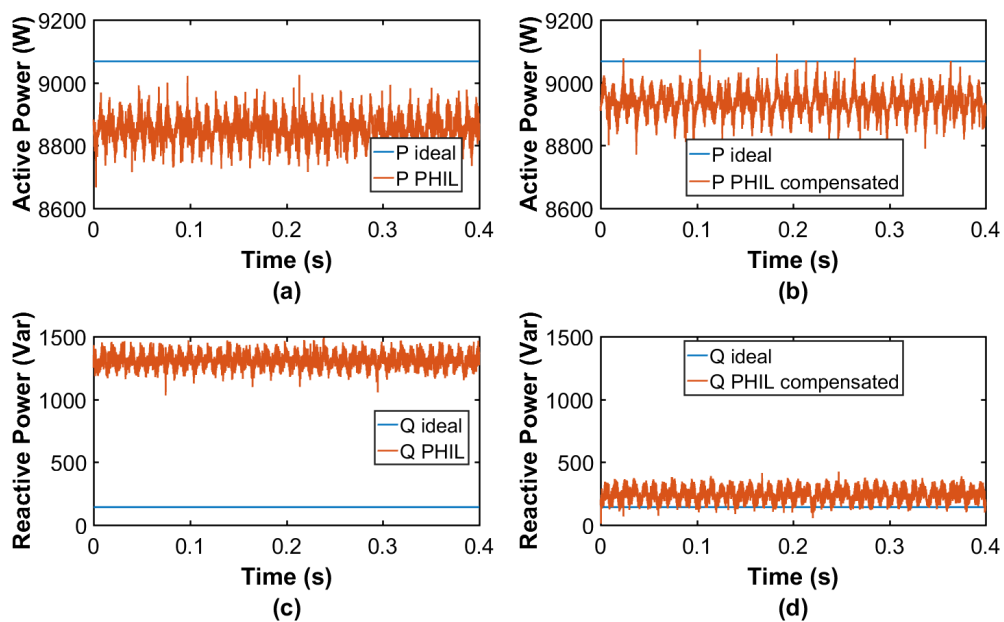


Fig. 4.21 Power measured at the simulation PCC for: (a) PHIL active power, (b) PHIL reactive power, (c) compensated PHIL active power, (d) compensated PHIL reactive power

Presence of harmonic components

For the purpose of analysing the performance of the time delay compensation algorithm, two scenarios with different harmonic content have been developed where configurations with and without the compensation algorithm are compared. The key performance value under investigation is the increase in phase difference between voltage and current at the PCC of the simulation.

The effective phase-shift introduced by the time delay on each harmonic has been examined by performing a Fourier analysis to the voltage and current waveforms produced at the simulation PCC. The Fourier analysis of the current and voltage waveforms is performed to 25 cycles of both waveforms starting at the same instant in order to achieve accurate results.

1. Presence of 5th and 7th components.

The steady-state waveform of the previous experiment has been now polluted with 5th and 7th harmonic components with a 5% amplitude of the fundamental component. In Fig. 4.22 (a), the voltage and current ideal results that have been obtained from a monolithic implementation are presented, where the amplitude of both waveforms have been normalized for facilitating the comparison between both waveforms.

In Fig. 4.22 (b) the experiment results without the compensation method are shown. Since the load is purely resistive, the voltage and current waveforms at a node are expected to be in phase, and to contain the same harmonic composition; however, it is clear that a phase shift between the fundamental voltage and current exists. Fig. 4.22 (c) shows the results when all the present harmonic components are compensated. In this case we can see that the fundamental and harmonic components are in phase as it was expected.

The time domain waveforms are not sufficient in this case to measure the impact that the compensation has on the accuracy. But more importantly it is not absolutely clear

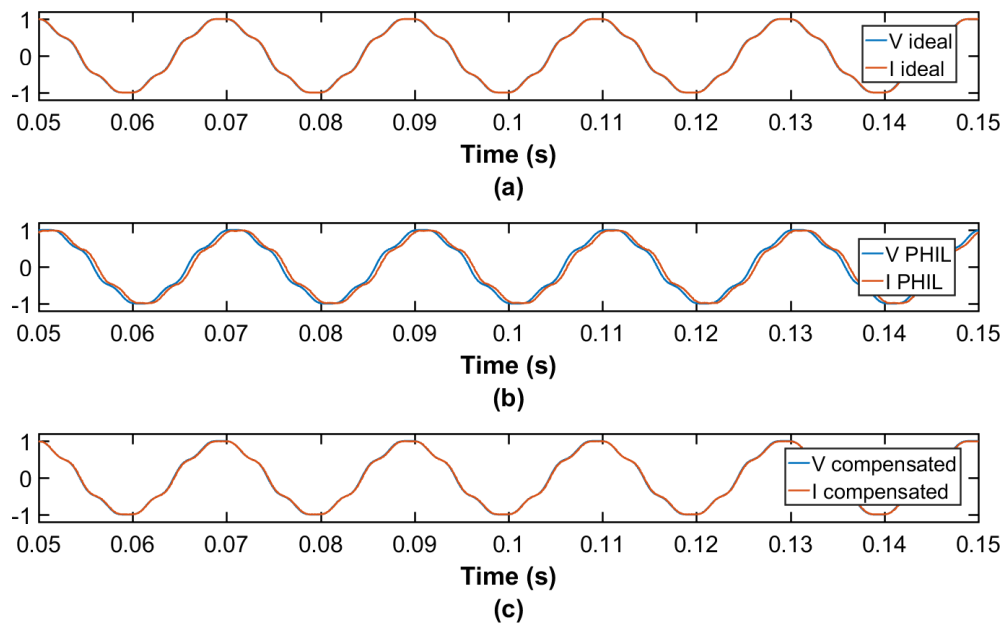


Fig. 4.22 Voltage and current waveforms with 5th and 7th harmonic components. (a) Ideal configuration, (b) conventional PHIL, (c) compensated PHIL.

that the harmonics introduced are being compensated. Therefore, a Fourier analysis of the waveforms is performed to study the phase of the harmonics for quantifying the accuracy of the method.

In Table 4.2, the results from the Fourier calculation are presented. Where the phase difference between voltage and current, φ_{diff} , of the compensated and not compensated PHIL implementations are compared with the ideal configuration for determining the total phase error that each implementation introduces.

As it is shown in Table 4.2, the not compensated configuration presents a phase error of 6.92° (equivalent to the time delay being compensated), which is also present at the harmonic components multiplied by the harmonic number, i.e. the error at the 5th harmonic component is approximately equal to five times 6.92° . However, the compensated configuration achieves an accurate compensation by which the error is reduced to almost zero for the fundamental component and less than 1.5°

Table 4.2 Phase error for experiment with presence of 5th and 7th harmonics.

Configuration	h	$\varphi_V(^{\circ})$	$\varphi_I(^{\circ})$	$\varphi_{diff}(^{\circ})$	Error ($^{\circ}$)
Ideal	1	-78.75	-79.65	0.9	-
	5	-33.74	-38.25	4.51	-
	7	168.75	162.45	6.3	-
Not Compensated PHIL	1	-104.82	-112.64	7.82	6.92
	5	-164.12	155.69	40.19	35.68
	7	-13.79	-68.52	54.73	48.43
Compensated PHIL	1	-78.75	-79.67	0.92	0.02
	5	-33.74	-39.55	5.81	1.3
	7	168.75	162.15	6.6	0.3

for the other harmonic components. This confirms the precise performance of the compensation algorithm for harmonic components.

2. Presence of 5th, 7th, 11th and 15th components.

For further testing the harmonic compensation, a scenario with a larger number of harmonic components is carried out. In this case, 5th, 7th and 11th with an amplitude of 2% of the fundamental amplitude, plus a 15th harmonic component with a 1% of the fundamental amplitude. This evaluates the performance of the compensation algorithm when higher frequency components are present, but also the accuracy of the power amplifier for reproducing such components, as the accuracy of the harmonics in this case also depends on the capabilities of the power amplifier.

In Fig. 4.23 the time domain waveforms of voltage and current for each of the configurations are presented, where the time delay presence is clear for the not compensated configuration of Fig. 4.23 (b), while the compensated PHIL phases appear to be preserved in Fig. 4.23 (c). In the same manner as for the previous scenario, the harmonic phases have been analysed by performing Fourier analysis to the waveforms, with the results presented in Table 4.3.

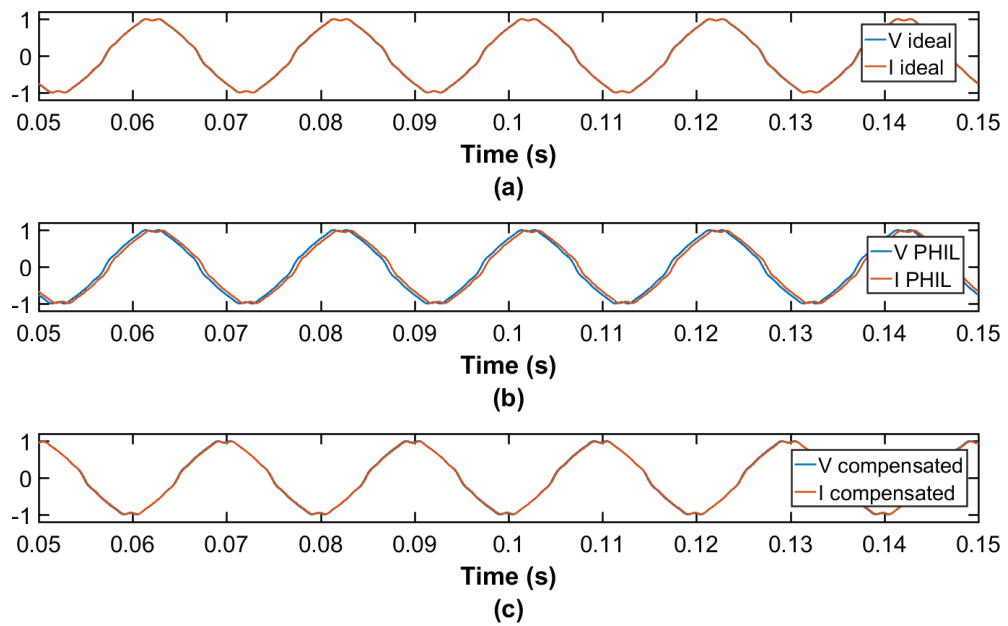


Fig. 4.23 Voltage and current waveforms with 5^{th} , 7^{th} , 11^{th} and 15^{th} harmonic components. (a) Ideal configuration, (b) conventional PHIL, (c) compensated PHIL.

The not compensated configuration still preserves the delay proportionality between the harmonic components as expected. Similarly to the previous analysis, the fundamental component is compensated with high accuracy when compensation is applied, but in this case the 5^{th} and 7^{th} harmonic components have slightly increased error in comparison with the previous scenario. This could be produced by the power amplifier and its output filter or the control itself. Nevertheless, the 11^{th} and 15^{th} components appear to be compensated accurately. A maximum of 3° error for the 5^{th} harmonic is achieved. The impact in the accuracy of the compensated PHIL implementation in comparison with the not compensated approach is considerably reduced.

The time delay introduced in the harmonic components can be very relevant when applications such as the validation and verification of active power filters is being performed through PHIL simulations. In this case due to the time delay introduced by the PHIL configuration, the APF rather than mitigating harmonics effects could

Table 4.3 Phase error for experiment with presence of 5th, 7th, 11th and 15th harmonics.

Configuration	h	$\varphi_V(^{\circ})$	$\varphi_I(^{\circ})$	$\varphi_{diff}(^{\circ})$	Error ($^{\circ}$)
Ideal	1	-85.95	-86.85	0.9	-
	5	-69.75	-74.25	4.5	-
	7	118.35	112.05	6.3	-
	11	134.55	124.65	9.9	-
	15	150.75	137.25	13.5	-
Not Compensated PHIL	1	52.67	44.87	7.8	6.9
	5	-96.62	-138.48	41.86	37.36
	7	8.71	-47.93	56.64	50.34
	11	-140.64	132.84	86.52	76.62
	15	69.96	-47.67	117.63	104.13
Compensated PHIL	1	-85.95	-86.87	0.92	0.02
	5	-69.74	-77.22	7.48	2.98
	7	118.35	110.01	8.34	2.04
	11	134.55	123.64	10.91	1.01
	15	150.75	136.72	14.03	0.53

be increasing their amplitude due to the phase error, producing the opposite desired effect.

4.5.4 Transient performance validation

10% voltage step

In this scenario a 10% voltage step is triggered at the simulated voltage source for the evaluation of the compensation algorithm performance in a realistic transient scenario. In Fig. 4.24 (a) and (b), one phase of the currents of the PHIL and compensated PHIL configurations during the voltage step are presented. As illustrated in Fig. 4.24 (c) with the RMSE between the ideal and PHIL configurations, the error that the time delay introduces is similar if not larger than the filtered response over one cycle that the compensated PHIL implementation introduces. These results are aligned with

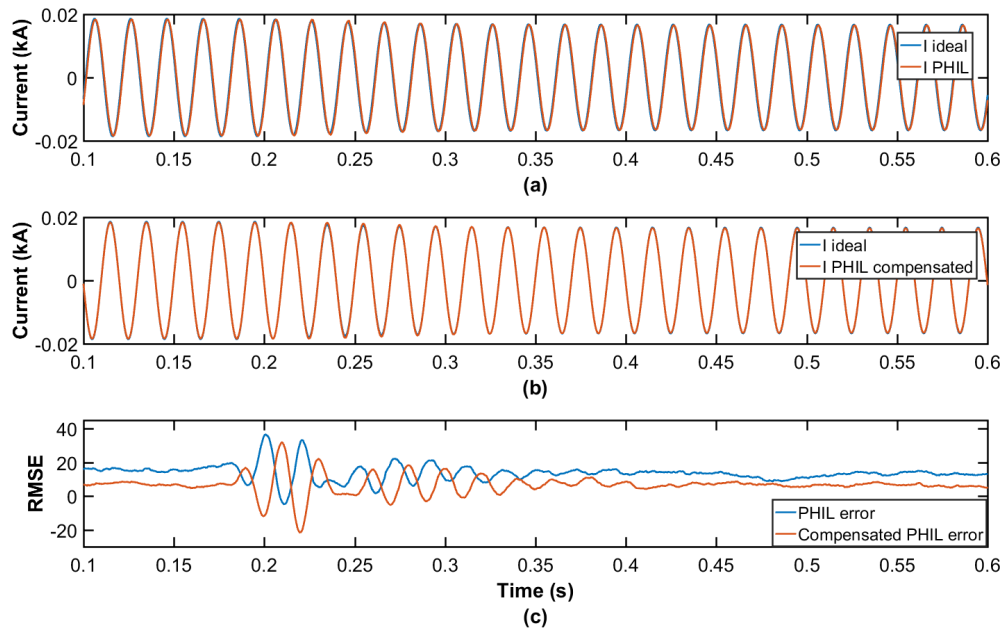


Fig. 4.24 Currents measured at the simulation PCC during a voltage step for (a) PHIL implementation (b) compensated PHIL implementation. (c) Error of both configurations.

the simulation results confirming the satisfactory performance of the compensation algorithm during transient conditions.

The power consumed by the HUT varies with the voltage, as a result a filtered step in the power emerges as seen in Fig. 4.25. In this case, the response of the PHIL implementation is slightly faster than the compensated PHIL configuration (as expected) as it appears from comparing Fig. 4.25 (a) and (c), although again the accuracy of the compensated implementation active power is comparable to the ideal response and more accurate than the not compensated implementation. Besides, the reactive power inaccuracies of the not compensated PHIL presented in Fig. 4.25 (c) are clearly mitigated with the compensation as shown in Fig. 4.25 (d).

Frequency ramp event

A frequency event that brings the frequency down from 50Hz to 49.5Hz with a 2Hz/s ramp rate is triggered at $t=0.2\text{s}$ for 0.25s in this scenario. The inaccuracies observed in

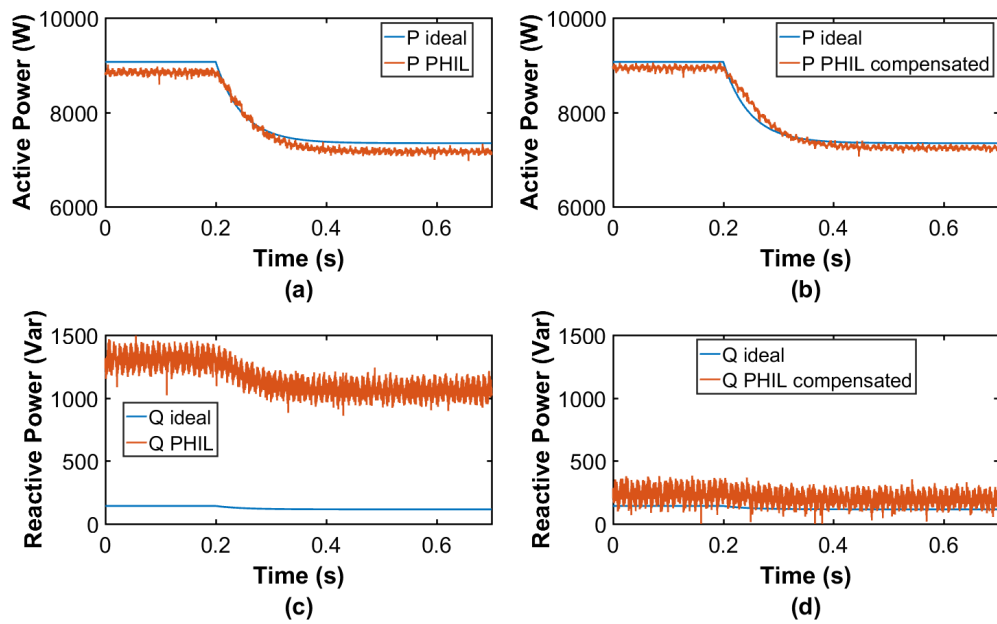


Fig. 4.25 Power response to voltage step, (a) active power with PHIL, (b) active power with compensated PHIL, (c) reactive power with PHIL and (d) reactive power with compensated PHIL.

this scenario have been very limited, with the variation in phase difference during the ramping of the frequency being the only impact in the accuracy, as presented in Fig. 4.26 with filtered phase differences between voltage and current for each implementation. Also, as discussed during the simulation analysis, the adaptive frequency approach of the compensation algorithm results in the phase difference after the event being equal to the pre-event difference, indicating that the algorithm has adapted to the new frequency after the event.

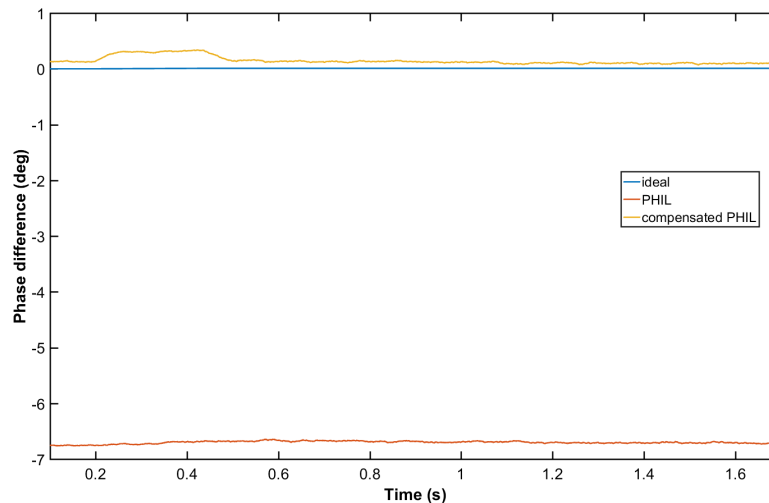


Fig. 4.26 Phase difference for a frequency ramp event.

4.6 Conclusions

With the purpose of improving the accuracy of PHIL simulations, a novel phase-shifting harmonic-by-harmonic and phase-by-phase time delay compensation method for PHIL simulations has been developed and experimentally validated in this Chapter.

The compensation method has proven to solve the inaccuracies caused by the time delay in the phase relationship between voltages and currents and in consequence to the power exchanges within PHIL simulations, by precisely compensating for the time delay, using an SDFT algorithm for the shifting of harmonic components. The experimental results presented are in accordance with the theoretical and simulated results, and therefore confirming the improved performance of PHIL simulations when the time delay compensation method is applied.

Additionally, the use of SDFT has revealed a positive impact into the stability of PHIL simulations by increasing the gain and phase margin of the implementation when the number of harmonics to compensate are no larger than up to the 55 odd harmonic in this case. With the algorithm implemented, scenarios that would be unstable are now

capable of maintaining stability with the addition of the SDFT based compensation algorithm.

In this manner, the time delay compensation will not affect to the system topology and therefore the dynamic behaviour of the original system will remain as it originally was in terms of power angles and voltage-current phase relationships for all the harmonics processed. This is a major advantage for performing PHIL simulations of low impedance power systems such as microgrids, marine or aero power systems, as consequence those systems are now able to experience an accurate PHIL simulation.

This method is also advantageous for distribution systems with an important penetration of power electronic converters, where the study of the harmonics can be essential and the accuracy of the fundamental component is not enough, with accurate harmonic analysis also required.

The main limitation of this algorithm is that it is not appropriate for the accurate reproduction of fast transients, i.e. sub-cycle step changes to the fundamental or harmonic amplitudes. The SDFT window length is finite, in this case a one cycle rectangular window, adaptive to fundamental frequency, is used. So, any step change in fundamental or harmonic content within the simulation will be represented as a smoothed ramp of the component's amplitude/phase over one cycle in the PHIL environment. However, even with this limitation the implementation of the compensated PHIL approach has proven to be more accurate during transients than the not compensated implementation.

Chapter 5

Novel interface algorithms for PHIL simulations

The requirement of including an interface between the hardware and software in PHIL systems, introduces non ideal behaviours and dynamics, such as gains and latencies, that are not expected in an electrically coupled system that by nature has no such interface. The process used for coupling different electrical subsystems by interconnecting voltages and/or currents is referred to as Interface Algorithm (IA). This algorithms are not only used for PHIL applications, but also typically used for the coupling of different sections of a simulated system with different time-steps, as multi-rate real time simulations or co-simulation environments.

The different IAs used for PHIL applications are not always applicable for all the testing scenarios, and depending on the test characteristics, the IA is selected accordingly. For example, when the HUT is known and the test scenario will not modify the ratio of impedances between the simulation and the HUT, a stability assessment can be conducted and a suitable IA chosen.

For the purpose of increasing the stability of PHIL in a wide variety of scenarios, two novel IAs are proposed in this chapter: the adaptive-ITM method and the virtual impedance shifting method.

Both of the developed approaches are based on adapting the interface according to the stability conditions required for each particular PHIL implementation. Accordingly both methods are recognised as adaptive IAs. Therefore, the identification of the minimum stability conditions that the implementation has to meet at all times is of paramount importance and a detailed stability assessment for the developed interface algorithms is required.

In the following subsections, first a brief introduction of the two proposed IAs is presented. Then, a detailed stability assessment for the identification of the stability conditions is performed. Finally, an evaluation of the performance of the two IAs under different test scenarios with varying load conditions and load types is carried out.

5.1 Adaptive-ITM Interface Algorithm

ITM and DIM IAs present stability limitations, the former is typically known to be dependant on the ratio of impedances between hardware and simulation, while the latter depends on a precise identification of the HUT impedance for an stable and accurate performance.

To improve the stability of PHIL simulations, an adaptive-ITM IA is proposed in this chapter, combining both I-ITM and V-ITM IAs. Based on their stability conditions, when a PHIL scenario becomes unstable for one of them, the other ITM variant would be stable according to the conventional stability conditions presented in Chapter 2, $|Z_{DRTS}|/|Z_{HUT}|$. Therefore if the stability conditions are known, and the parameters that influence the stability conditions can be monitored, then the IA could be adapted to remain always stable.

The developed adaptive-ITM IA is presented in Fig. 5.1. In contrast with other ITM methods available in the literature, in this case both voltage source and current source are present in both sides of the interface (simulation and hardware). The choice of which source is to be used by the IA is made with the use of a switch at each side of the interface. The switch will be controlled based on the stability conditions found for each specific case.

With the general approach to find the stability conditions of ITM IAs, the switch for changing the interfaces will be operated with a signal activated by the range $|Z_{DRTS}|/|Z_{HUT}|$ as:

$$switch = \begin{cases} V-ITM, & \text{if } |Z_{DRTS}|/|Z_{HUT}| < 1 \\ I-ITM, & \text{otherwise} \end{cases} \quad (5.1)$$

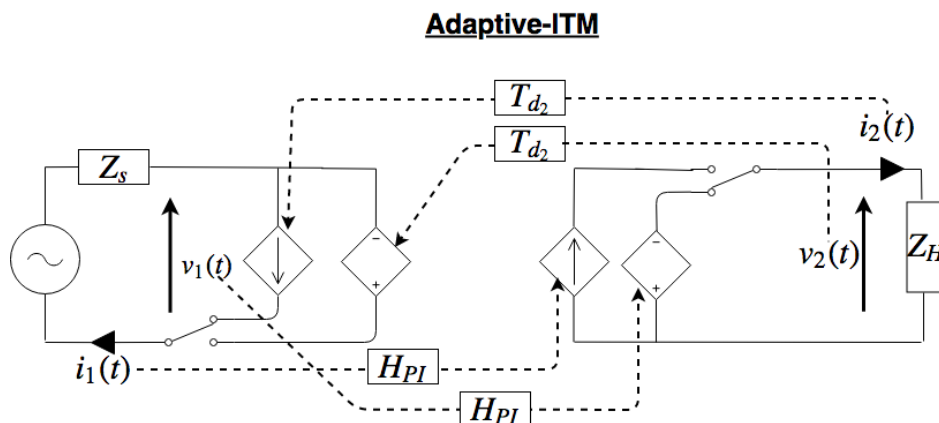


Fig. 5.1 Diagram of Adaptive-ITM IA

As a result, the PHIL simulation would always remain stable if the ratio of impedances is calculated accurately and the transition between interfaces is performed smoothly without transients. Similarly to the DIM algorithm, A-ITM does also require of the identification of the HUT impedance, nevertheless the DIM requires of a very precise identification as the accuracy depends on it, while for the A-ITM the precision has a

more limited effect into the accuracy. Crucially, the need for a real-time adjustment of the simulation impedance is not required.

5.1.1 A-ITM Performance assessment

Two different cases have been developed for the study of the performance of the proposed A-ITM IA in a simulation environment (MATLAB Simulink). First, a simple test case with a variable resistive HUT has been carried out. Then a case with a series resistive and inductive (RL) load is assessed.

Resistive Load

A variable resistor is selected as the HUT for this experiment, allowing for the study of different scenarios that can challenge the stability of PHIL simulations. A controlled voltage source along with its impedance is the simulated part of the system.

A first simulation has been performed with a resistive source impedance value of 10Ω and a variable resistor set to increase its value from 1Ω up to 50Ω in 1s as seen in Fig. 5.2 (b), therefore forcing the ratio of impedances $|Z_{DRTS}|/|Z_{HUT}|$ to breach its stability condition. During this transition, if individual voltage or current ITM methods are used, the simulation would become unstable due to the variation of the impedance. The DIM IA along with the adaptive-ITM IA are implemented with the same impedance calculation algorithm, similar to [PE13]. From the simulation, in Fig. 5.2 (a), it can be observed that both of the implementations remain stable. This is expected from DIM when the impedance identification algorithm is accurate; however, the adaptability of the ITM method proposed preserves the stability even under the breach of the stability condition. In Fig. 5.3, the exact point at which the interface is switched from V-ITM to I-ITM is presented, where a minor fluctuation is present at the

exact time that the interfaces are switched (when the measured impedance is equal to the simulation impedance, 10Ω).

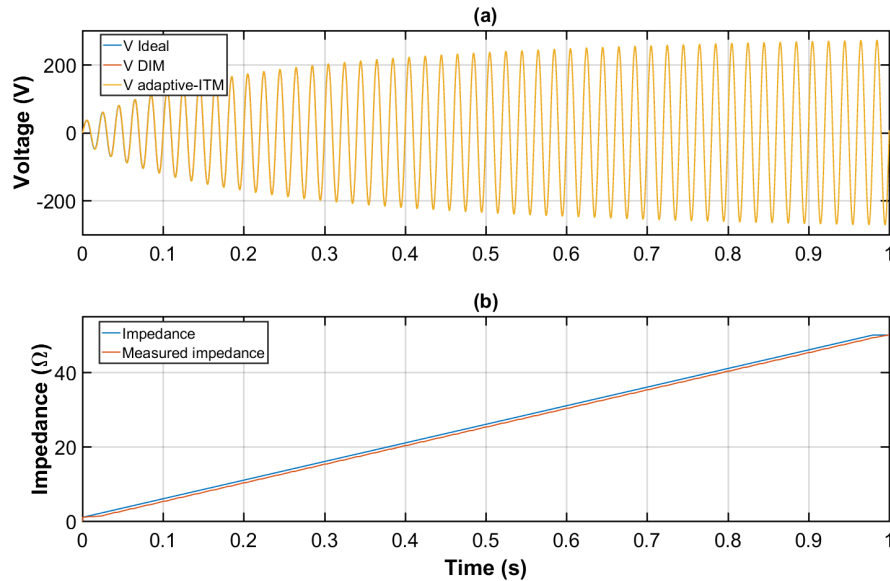


Fig. 5.2 IA comparisons with variable Resistance and measured impedance values, from V-ITM to I-ITM

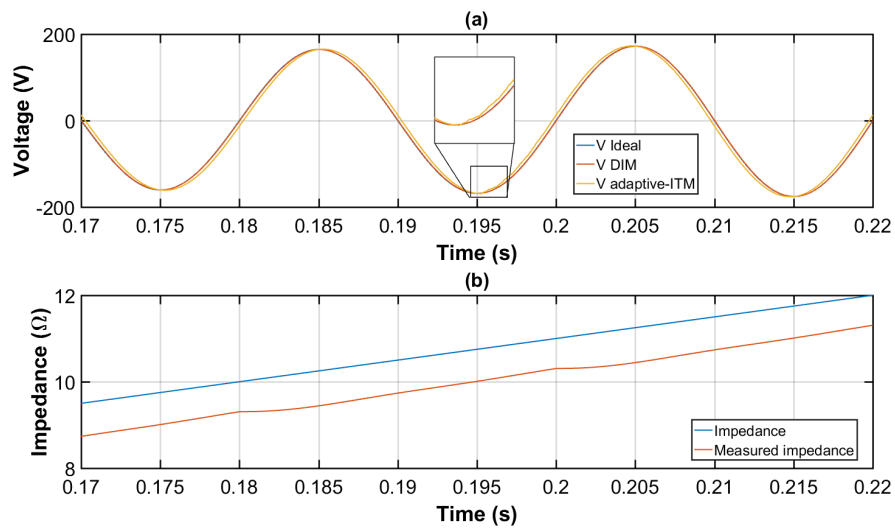


Fig. 5.3 IA comparisons with variable Resistance and measured impedance values, from V-ITM to I-ITM

For carrying out a thorough analysis, an opposite variation of the impedance is also studied (from 50Ω descending to 1Ω), where the adaptive-ITM IA starts as I-ITM and

needs to switch into V-ITM for maintaining the stability. As it is shown in Fig. 5.4, adaptive-ITM algorithm manages to maintain the stability of the simulation, although a small ripple appears at the time of switching similar to the previous scenario as seen in Fig. 5.5.

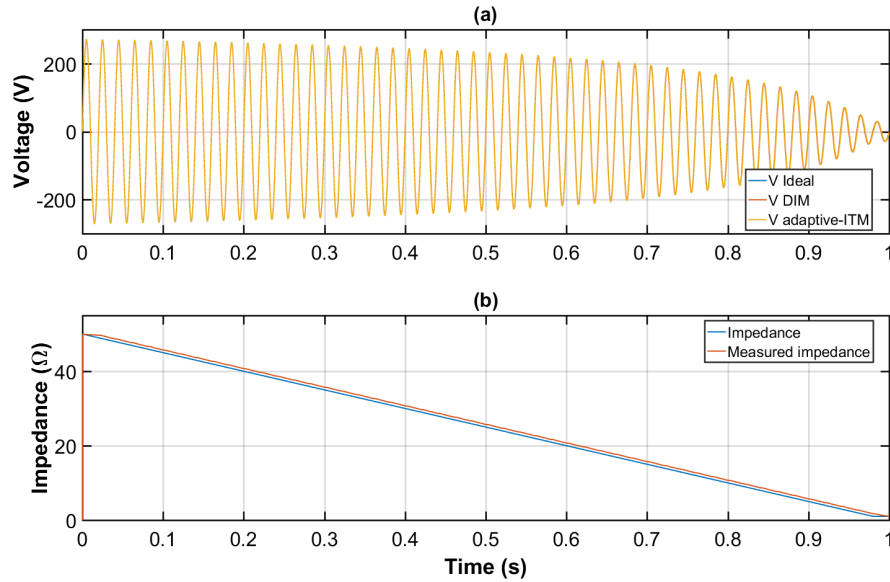


Fig. 5.4 IA comparisons with variable Resistance and measured impedance values, from I-ITM to V-ITM

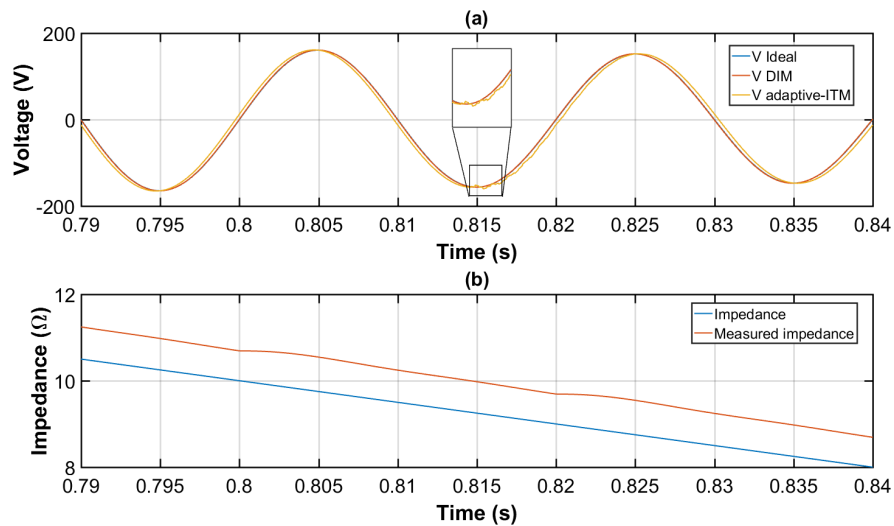


Fig. 5.5 IA comparisons with variable Resistance and measured impedance values, from I-ITM to V-ITM

Therefore, it can be concluded that the proposed adaptive-ITM IA manages to remain stable in circumstances in which typical ITM IAs are unstable, it also operates similarly to the DIM IA for scenarios where $X_{DRTS} = X_{HUT} = 0$.

Simulation of A-ITM IA with RL HUT

A second test has been carried out where the HUT and the simulation impedance are both a series RL component. Similarly to the previous scenario, the resistor on the HUT will be dynamically varied for assessing the performance of the proposed interface. The components used for this scenario are presented in Table 5.1.

Table 5.1 Component values for A-ITM with RL HUT simulation

Component	Value
R_s	0.5Ω
L_s	$0.5mH$
R_h	1 to 0.1Ω
L_h	$1mH$

The results of the simulation with adaptive-ITM are shown in Fig. 5.6, which produce a problematic behaviour. Analysing the performance we can observe that when the measurement of the impedance gets to an impedance ratio lower than 1, the interface is switched and a large transient appears, leading to the impedance ratio to go again over 1 and it is switched back to the V-ITM interface, which surprisingly remains stable even when the ratio in theory is lower than 1. This behaviour is repeated continuously, resulting in a performance of the interface which is not expected and would prevent the use of this interface.

A very important observation can be made from this simulation, even when the ratio of impedance magnitudes $|Z_{DRTS}|/|Z_{HUT}|$ is larger than 1 the PHIL implementation with a V-ITM interface remains stable. This is in contrast with conventional stability

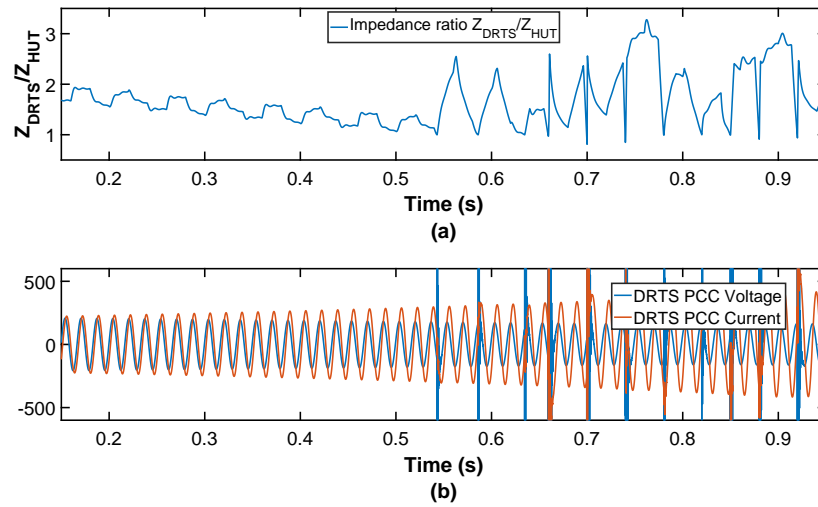


Fig. 5.6 Simulation results for A-ITM with RL load.(a)Impedance ratio, (b) Voltage and current measured.

conditions identified for such interfaces and therefore a more exhaustive study of the stability for the understanding of this behaviour has been carried out below.

5.2 Detailed stability conditions for PHIL

The adaptive-ITM IA has yielded positive results for a resistive HUT as the ratio of impedances when $X_{DRTS} = X_{HUT} = 0$ is still prevailing; however, when more complex HUT are analysed, the identified condition is no longer accurate. Therefore, in contrast with [RSB08; DGL14; Edr+15; LLS12] and as already suggested by [Kot+15; Hon+09], the stability of ITM methods does not always depends on the impedance ratio $|Z_{DRTS}|/|Z_{HUT}|$, but only for resistive scenarios. Accordingly, detailed stability study of the ITM method is required for providing more informed decisions on the transition between interfaces and achieving stable PHIL simulations.

In contrast with conventional stability assessment procedures for PHIL simulations, in which Bode or Nyquist stability criterion are used and a pure resistive impedance is assumed, in this case stability assessment based on the Routh-Hurwitz criterion is preferred. The main difference of the stability assessment performed here with respect to conventional assessments is that the impedances are not assumed purely resistive (not frequency dependant), as when inductors or capacitors are part of the system, their frequency dependency will be changing the poles and zeros placement and accordingly modifying the stability of the system.

Typically, stability studies for only one type of load have been performed [Kot+15; Hon+09], these being not sufficient for a complete stability assessment of PHIL simulations. For the evaluation of this issue, a detailed stability assessment of different combinations of hardware and software impedances has been performed to determine the parameters that will lead to a stable PHIL simulation.

5.2.1 Routh-Hurwitz stability assessment

The stability will be evaluated using the Routh-Hurwitz criterion, which will give a necessary and sufficient condition for the stability of a linear feedback system, allowing

to define the stability of the system without the need of identifying the system poles and zeros. Therefore, simplifying the study when a large number of variables are present in comparison with Bode or Nyquist stability criterion which are difficult to assess if poles and zeros are not identified.

The Routh-Hurwitz stability criterion analyses the characteristic equation of the closed loop transfer function of the system under study (the denominator). By using the Routh-Hurwitz tabular method for the assessment, the number of roots in the Right Half Plane (RHP) are counted as the number of times the sign changes in the first column of the table, this being developed as presented in Table 5.2 [DB].

Table 5.2 Routh-Hurwitz tabular method

s^n	a_n	a_{n-2}	a_{n-4}	...
s^{n-1}	a_{n-1}	a_{n-3}	a_{n-5}	...
s^{n-2}	b_1	b_2	b_3	...
s^{n-3}	c_1	c_2	c_3	...
...

where:

$$b_i = \frac{a_{n-1} \times a_{n-2i} - a_n \times a_{n-(2i+1)}}{a_{n-1}} \quad (5.2)$$

$$c_i = \frac{b_1 \times a_{n-(2i+1)} - a_{n-1} \times b_{i+1}}{b_1} \quad (5.3)$$

Stability assessment of a PHIL implementation with V-ITM IA is performed as an example of the stability assessment process. The main parameters being $T_{dmax} = T_d$, $Z_{DRTS} = R_s + j\omega L_s$ and $Z_{HUT} = R_h + j\omega L_h$, where the subscripts s and h are utilized for the DRTS and HUT components respectively. For this assessment the PI is assumed as a time delay only, which is considered as part of T_d . The control loop diagram for this implementation is presented in Fig. 5.7, and in this case the transfer functions are defined as:

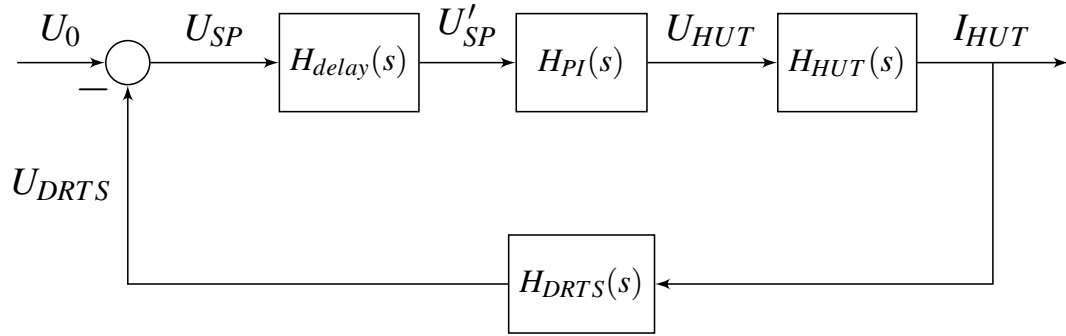


Fig. 5.7 PHIL control loop diagram.

$$H_{DRTS}(s) = R_s + sL_s$$

$$H_{HUT}(s) = \frac{1}{R_h + sL_h}$$

with the transfer function of the time delay approximated with a first order Pade approximation for its conversion into a rational function, represented by:

$$H_{delay}(s) = e^{-T_d s} \approx \frac{-\frac{T_d}{2}s + 1}{\frac{T_d}{2}s + 1}$$

The closed loop characteristic equation of the system is identified as:

$$P(s) = 1 + H_{DRTS}(s)H_{HUT}(s)H_{delay}(s) = 0$$

$$P(s) = (L_h T_d - L_s T_d)s^2 + (2L_h + 2L_s + R_h T_d - R_s T_d)s + 2R_h + 2R_s = 0$$

Applying the Routh-Hurwitz stability criterion to $P(s)$, Table 5.3 is calculated.

Table 5.3 Routh table with series RL HUT

s^2	$L_h T_d - L_s T_d$	$2R_h + 2R_s$
s^1	$2L_h + 2L_s + R_h T_d - R_s T_d$	0
s^0	$2R_h + 2R_s$	0

All the roots are in the Left Half Plane (LHP) if and only if all entries of the first column are positive, avoiding a sign change. Therefore in this case, the conditions for achieving a stable system are:

$$\begin{aligned} 1. \quad & L_h > L_s \\ 2. \quad & R_s < R_h + \frac{2(L_h + L_s)}{T_d} \end{aligned}$$

This stability conditions are very distant to the conventionally identified stability conditions for ITM IA presented in Eq. 5.1.

An equivalent stability assessment process has been performed for different arrangements of HUT resistor (R_h), inductor (L_h) and capacitor (C_h), when the simulation impedance is composed of a resistor (R_s) in series with an inductor (L_s) (as it is a typical configuration of reduced power systems). As a result, stability conditions required for the different arrangements of the HUT are presented in Table 5.4. It can be observed that when capacitive components are added to the HUT, stability tends to be at risk (except for the series RLC combination).

This is in contrast with the inaccurately commonly defined stability condition of $|Z_{HUT}|/|Z_{DRTS}|$ ratio larger or smaller than 1 for ITM IAs [RSB08; GLG10; PE13] with the PI assumed ideal. This is only accurate when HUT and DRTS impedances are only resistive. If an inductive component is present the ratio of inductors will usually be more decisive than the ratio of impedances, as in that case even if the ratio of impedances met the condition, the system would still be unstable if the ratio of inductors is not met.

Furthermore, the stability conditions can play an important role for determining the point at which the ITM interface will become unstable and apply a different interface or other stability mechanisms. However, the conditions are dependent on specific components and parameters of the simulation and HUT that can be very challenging to be individually identified on-line. As a consequence, the adaptive-ITM method without

Table 5.4 Stability conditions for V-ITM

Z_{DRTS}	Z_{HUT}	Stability conditions
$R_s L_s$	R_h	$R_h > R_s$
$R_s L_s$	L_h	1) $L_h > L_s$ 2) $R_s < \frac{2(L_h + L_s)}{T_d}$
$R_s L_s$	C_h	Unstable
$R_s L_s$	$R_h L_h$	1) $L_h > L_s$ 2) $R_s < R_h + \frac{2(L_h + L_s)}{T_d}$
$R_s L_s$	$R_h C_h$	Unstable
$R_s L_s$	$R_h L_h C_h$	1) $L_h > L_s$ 2) $R_s < R_h + \frac{2(L_h + L_s)}{T_d}$ 3) $(T_d + 2C_h R_h + 2C_h R_s) \cdot (2L_h + 2L_s + R_h T_d + R_s T_d) > 2T_d(L_h - L_s)$
$R_s L_s$	$R_h L_h$	Unstable
$R_s L_s$	$R_h C_h$	Unstable
$R_s L_s$	$R_h L_h C_h$	Unstable

additional developments is only accurate for PHIL simulations with purely resistive components.

From the evaluation of the results presented in Table 5.4, it can be observed that when an inductive component is in series with the HUT, the system is able to achieve stability if the conditions are met. Thus, for further assessment of this observation the stability study has been performed again for the unstable cases with an inductor introduced in series with the HUT, L_{sh} . As it is shown in Table 5.5, with the series inductor added to the unstable cases, all the presented cases become stable if the conditions generated from the Routh-Hurwitz stability criterion are met.

As a consequence of these observations on the stability conditions, a novel method in which simulated inductance is virtually shifted to the HUT for improving the stability of ITM algorithms has been developed.

Table 5.5 Stability conditions for V-ITM with added series L_{sh}

Z_{DRTS}	Z_{HUT}	Stability conditions
$R_s L_s$	$L_{sh} + C_h$	1) $L_{sh} > L_s$ 2) $R_s < \frac{2(L_{sh} + L_s)}{T_d}$ 3) $4L_s T_d + 4C_h L_{sh} R_s + 4C_h L_s R_s > R_s T_d^2 + 2C_h R_s^2 T_d$
$R_s L_s$	$L_{sh} + R_h C_h$	1) $L_{sh} > L_s$ 2) $R_s < R_h + \frac{2(L_{sh} + L_s)}{T_d}$ 3) $(T_d + 2C_h R_h + 2C_h R_s) \cdot (2L_{sh} + 2L_s + R_h T_d + R_s T_d) > 2T_d(L_{sh} - L_s)$
$R_s L_s$	$L_{sh} + R_h L_h$	1) $L_{sh} > L_s$ 2) $(2L_h + T_d R_h) \cdot (L_h + L_{sh}) > T_d(L_h R_s + L_s R_h)$ 3) $2R_h(L_s + L_{sh} + L_h) + 2L_h R_s > R_h R_s T_d$ 4) $(2L_h R_h + 2L_{sh} R_h + 2L_h R_s + 2L_s R_h - R_h R_s T_d)(2L_h L_{sh} + 2L_h L_s + L_h R_h T_d + L_{sh} R_h T_d - L_h R_s T_d - L_s R_h T_d) > 2L_h R_h R_s T_d(L_{sh} - L_s)$
$R_s L_s$	$L_{sh} + R_h C_h$	1) $L_{sh} > L_s$ 2) $(L_s T_d + 2C_h L_{sh} R_h + 2C_h L_s R_h) > L_s T_d + C_h R_h R_s T_d$ 3) $(2L_{sh} + 2L_s + R_h T_d - R_s T_d + 2C_h R_h R_s) \cdot (L_{sh} T_d - L_s T_d + 2C_h L_{sh} R_h + 2C_h L_s R_h - C_h R_h R_s T_d) > C_h R_h T_d(L_{sh} - L_s)(2R_h + 2R_s)$

5.3 Virtual impedance shifting method

For the improvement of the stability of PHIL simulations, a method has been developed in which impedances of the simulation and HUT are virtually modified by shifting them, for example, from simulation into the HUT for V-ITM. Physical shifting of impedances has been introduced in [Kot+15; Hon+09]; however, physical components were required to be added into the HUT to perform the impedance shift, presenting a large limitation in terms of applicability for realistically performing such shifting for multiple and varying scenarios, and also in terms of cost for high power rating scenarios.

Consequently, the virtual impedance shifting method proposed here, avoids the addition of a physical component by virtually emulating the behaviour of such shifted impedance. This can highly increase the applicability of such method as well as bring the opportunity of varying the impedance value in real-time if required, reducing the time and cost of the physical shifting methodology.

5.3.1 Implementation of virtual impedance shifting

The virtual impedance shifting method is illustrated in Fig. 5.8. This methodology requires the transformation of the measured HUT currents into the frequency domain for identifying the voltage drop created by the virtual impedance as presented in Fig. 5.8. Once the voltage drop is known, it is subtracted from the setpoint voltage received at the interface (when implemented within the switched-mode amplifier controller), and a new setpoint voltage is generated. The calculation of the new setpoint can be implemented either at the DRTS before the setpoint is sent to the power interface or at the control of the power interface if switched-mode power amplifier is used.

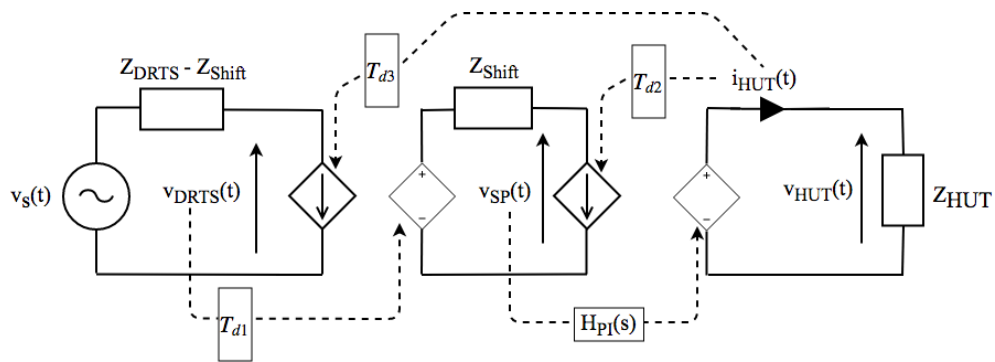


Fig. 5.8 Virtual impedance shifting diagram.

5.3.2 Stability assessment

The control loop diagram of a PHIL simulation with virtual impedance shifting and V-ITM is presented in Fig. 5.9, where the introduction of the shifting impedance creates an inner control loop, in contrast with common PHIL control diagrams where such inner loop is not present. For achieving a stable simulation both control loops, the inner and outer, must be closed loop stable.

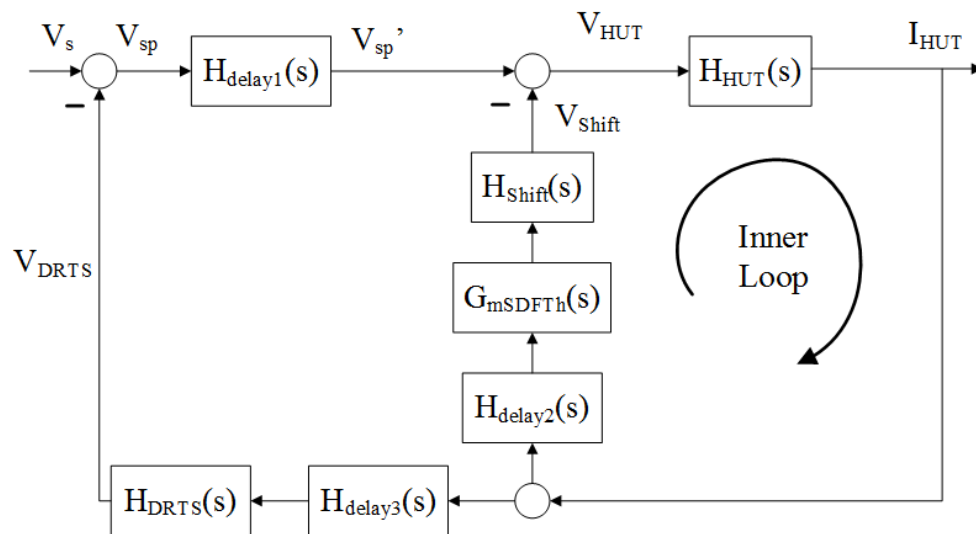


Fig. 5.9 Control loop with virtual impedance shifting

The inner loop control is presented in Fig. 5.9 with its open and closed loop transfer functions calculated with:

$$H_{DRTS}(s) = \frac{V_{DRTS}}{I_{HUT}} = Z_{DRTS}(s) \quad (5.4)$$

$$H_{HUT}(s) = \frac{I_{HUT}}{V_{HUT}} = \frac{1}{Z_{HUT}(s)} \quad (5.5)$$

$$H_{Shift}(s) = \frac{V_{Shift}}{I_{HUT}} = Z_{Shift}(s) \quad (5.6)$$

$$H_{delay1}(s) = e^{-sT_{d1}} \quad (5.7)$$

$$H_{delay2}(s) = e^{-sT_{d2}} \quad (5.8)$$

$$H_{delay3}(s) = e^{-sT_{d3}}, \quad (5.9)$$

resulting in the inner open loop transfer function described as:

$$G_{innerOL}(s) = \frac{I_{HUT}}{V_{SP'}} = H_{delay2}(s) \cdot G_{m_{SDFT_h}}(s) \cdot \frac{Z_{Shift}(s)}{Z_{HUT}(s)} \quad (5.10)$$

where $G_{m_{SDFT_h}}(s)$ is the SDFT transfer function used for measurement purposes. Eq. 5.10 is also equivalent to the transfer function of a PHIL implementation with time delay compensation presented in Eq. 4.13. Accordingly, the inner control loop stability is equivalent to that of a compensated PHIL simulation, with the shifted impedance instead of the simulation side impedance in the equation. The inner closed loop transfer function is expressed as:

$$G_{innerCL}(s) = \frac{I_{HUT}}{V_{SP'}} = \frac{1}{Z_{HUT}(s)} \quad (5.11)$$

$$1 + H_{delay2}(s) \cdot G_{m_{SDFT_h}}(s) \cdot \frac{Z_{Shift}(s)}{Z_{HUT}(s)}$$

where $H_{delay2}(s)$ represents the time delay introduced for the acquisition and processing of the current measurement, $Z_{Shift}(s)$ is the shifted impedance and $Z_{HUT}(s)$ the impedance at the HUT.

Similarly to the inner loop, the closed loop transfer functions of the outer control loop are:

$$G_{outerOL}(s) = \frac{I_{HUT}}{V_s} = \frac{H_{delay13}(s) \cdot Z_{DRTS}(s)}{Z_{HUT}(s) + H_{delay2}(s) \cdot G_{m_{SDFT_h}}(s) \cdot Z_{Shift}(s)} \quad (5.12)$$

$$G_{outerCL}(s) = \frac{I_{HUT}}{V_{SP'}} = \frac{\frac{H_{delay1}(s)}{Z_{HUT}(s) + H_{delay2}(s) \cdot G_{m_{SDFT_h}}(s) \cdot Z_{Shift}(s)}}{1 + \frac{H_{delay13}(s) \cdot Z_{DRTS}(s)}{Z_{HUT}(s) + H_{delay2}(s) \cdot G_{m_{SDFT_h}}(s) \cdot Z_{Shift}(s)}}} \quad (5.13)$$

where $H_{delay13}(s) = H_{delay1}(s) \cdot H_{delay3}(s)$.

The stability of the inner and outer closed loop control transfer functions has been evaluated by using Nyquist stability criteria. In this case, Nyquist has been preferred over Routh-Hurwitz due to the excessive complexity introduced by the SDFT transfer function for making an assessment with variables.

Therefore, for the stability assessment the parameters presented in Table 5.6 have been utilised.

Table 5.6 Component values for stability assessment of virtual impedance shifting method

Component	Value
R_{DRTS}	0.5Ω
L_{DRTS}	$3mH - L_{shift}$
R_{HUT}	1Ω
L_{HUT}	$1mH$
T_w	$0.02s$
T_{d1}	$200\mu s$
T_{d2}	$100\mu s$
T_{d3}	$200\mu s$

In Fig. 5.10, the results from the stability assessment are presented for various L_{shift} parameters and with only the fundamental frequency component being processed by the SDFT function. The stability of the outer control loop decreases as L_{shift} is reduced as shown in Fig. 5.10 (a); on the contrary, the inner loop stability is diminished as L_{shift} increases as presented in Fig. 5.10 (b). The presence of SDFT in the inner loop transfer function increases the stability of the inner loop, presenting the same response as the time delay compensation method presented in Chapter 4. However, if SDFT (or other stabilizing component) is not present for this configuration, it would not be stable due to the opposite behaviour of the control loops. Even with SDFT in the inner loop, for large values of L_{shift} the inner control loop will become also unstable.

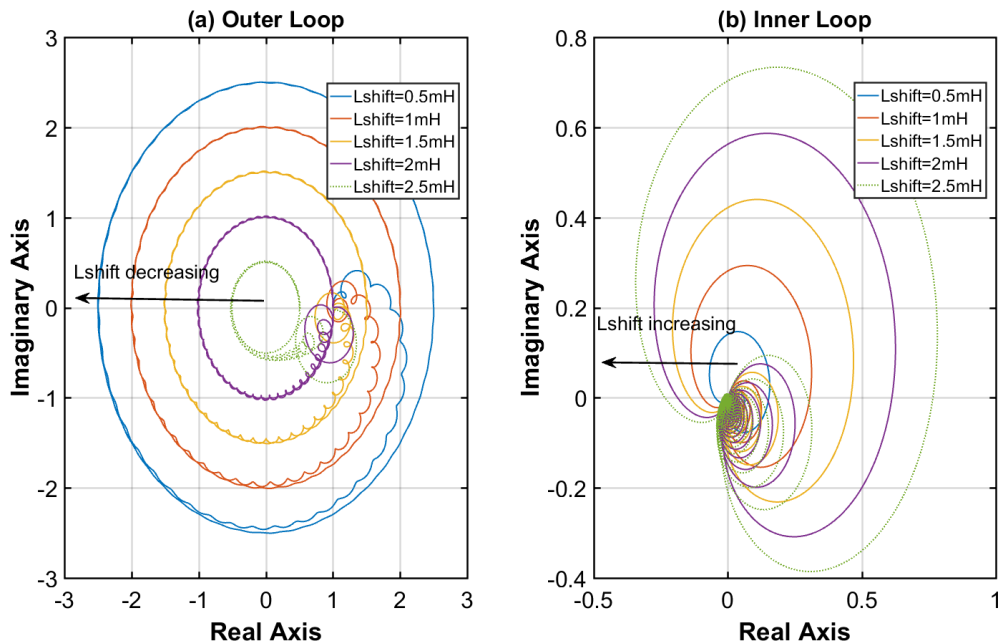


Fig. 5.10 Nyquist plot of virtual impedance shifting method for (a) open loop and (b) closed loop transfer functions.

Therefore, addition of a stability improvement component is recommended for this implementation. The addition of filters for limiting the bandwidth of the PHIL system can bring similar configurations to stability when SDFT is not present, as has been shown in [LS18] for a multi-rate partitioning case, where low pass filters with various

cut-off frequencies were added in the feedback current path. However, the addition of such filters can dramatically increase the time delay of the system depending on the cut-off frequency.

Instead of a low pass filter, the addition of the time delay compensation algorithm presented in Chapter 4 is preferred for providing the stabilizing filtering effect. This will not only provide the required stability but also the possibility of simultaneously applying the time delay compensation method with the improved accuracy that it brings. As a result, increased accuracy and stability is expected with the solely addition of one main function. The control loop diagram with the SDFT added as the filtering function in the feed-forward path is presented in Fig. 5.11.

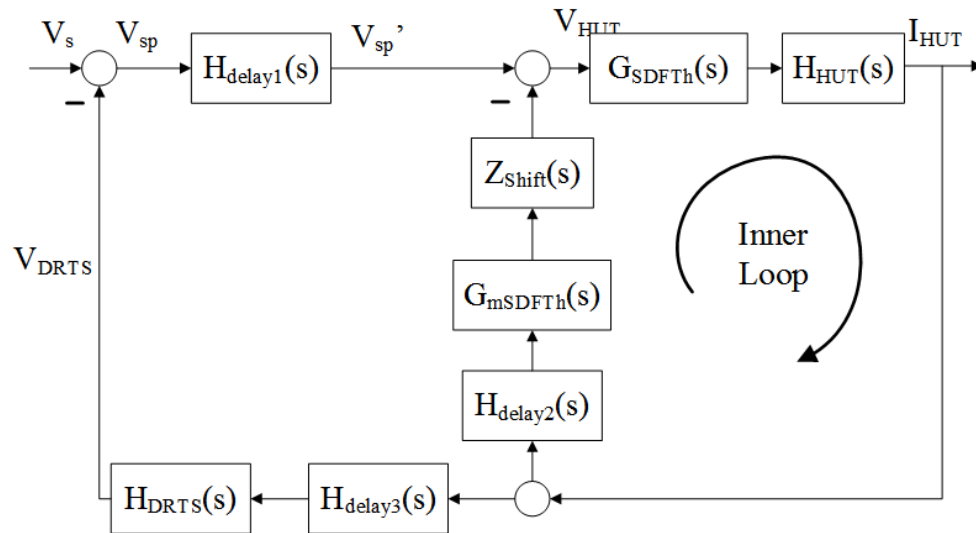


Fig. 5.11 Control loop with virtual impedance shifting

With the addition of the time delay compensation function (represented by the SDFT transfer function), the inner and outer loop transfer functions are defined as:

$$G_{innerOL}(s) = H_{delay2}(s) \cdot G_{mSDFT_h}(s) \cdot G_{SDFT_h}(s) \cdot \frac{Z_{Shift}(s)}{Z_{HUT}(s)} \quad (5.14)$$

$$G_{innerCL}(s) = \frac{G_{SDFT_h}(s) \cdot \frac{1}{Z_{HUT}(s)}}{1 + H_{delay2}(s) \cdot G_{mSDFT_h}(s) \cdot G_{SDFT_h}(s) \cdot \frac{Z_{Shift}(s)}{Z_{HUT}(s)}} \quad (5.15)$$

$$G_{outerOL}(s) = \frac{H_{delay13}(s) \cdot G_{SDFT_h}(s) \cdot Z_{DRTS}(s)}{Z_{HUT}(s) + H_{delay2}(s) \cdot G_{mSDFT_h}(s) \cdot G_{SDFT_h}(s) \cdot Z_{Shift}(s)} \quad (5.16)$$

where $G_{SDFT_h}(s)$ is presented in Eq. 4.12.

The stability is assessed under the same scenario as the implementation of the virtual impedance shifting method without the compensation, with the parameters presented in Table 5.6. The results for different values of L_{Shift} are presented in Fig. 5.12. With the addition of the compensation algorithm, it can be observed from Fig. 5.12 (a) that the gain and phase margin of the outer loop have been improved so that the system remains stable for all the cases. In contrast with the non-compensated virtual impedance shifting method, in this case the limiting control loop is the inner loop, as its gain margin is minor compared with the outer loop. Therefore, for the purpose of analysing the performance of this novel method, the Nyquist diagram of a compensated PHIL configuration (without virtual impedance shifting) is also presented in Fig. 5.12 (b). As can be observed, although the virtual impedance shifting allows for stabilizing some PHIL configurations that are unstable, the solely addition of the time delay compensation algorithm presents an improved performance as well as lower computation requirements since only a single SDFT is required.

5.3.3 Evaluation in a simulation environment

To reinforce the theoretical results, simulation of the virtual impedance shifting method with the parameters presented in Table 5.6 has also been carried out in Simulink. The

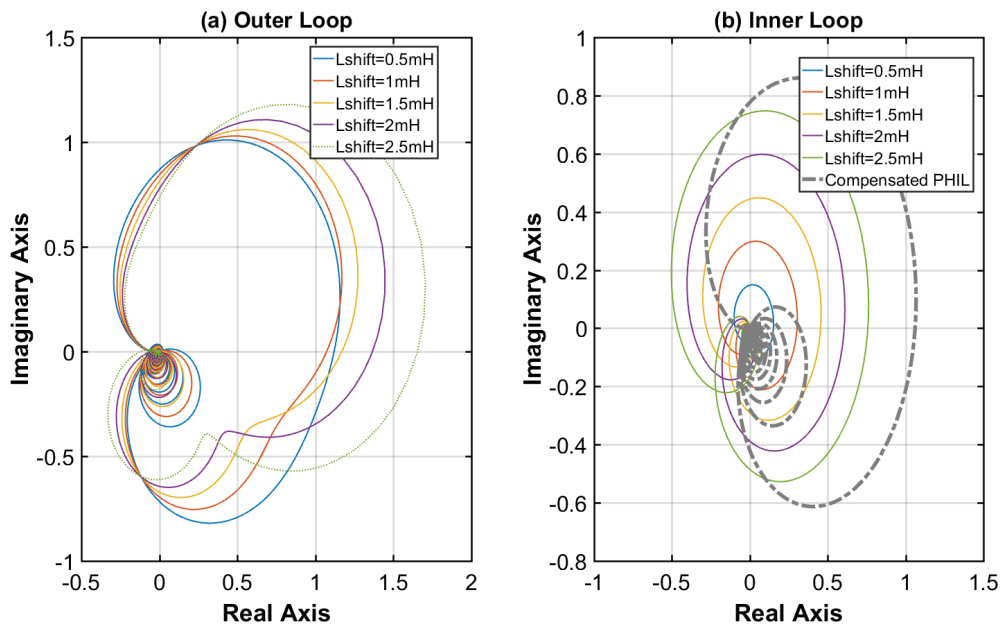


Fig. 5.12 Nyquist diagram with a comparison of the virtual impedance shifting stability and SDFT.

model configuration consists of a $230V_{rms}$ single phase, $50Hz$ voltage source, the DRTS and HUT impedances, and a simulation time-step of $1\mu s$.

The virtual impedance shifting method is analysed against a configuration where the time delay compensation is added to the virtual impedance shifting configuration and also with a PHIL simulation where only time delay compensation is present (shifting of the impedance is not implemented).

The first simulation has been performed for $L_{shift} = 1.5mH$, with the voltages and currents measured at the simulation PCC and presented in Fig. 5.13. According to the stability assessment, when only virtual impedance shifting is used the system is unstable, however when the time delay compensation is added to the configuration the system remains stable, with the results presented in Fig. 5.13 validating the theoretical results.

As a consequence, it is recommended to use the virtual impedance shifting method in conjunction with the time delay compensation for an improved performance. Nev-

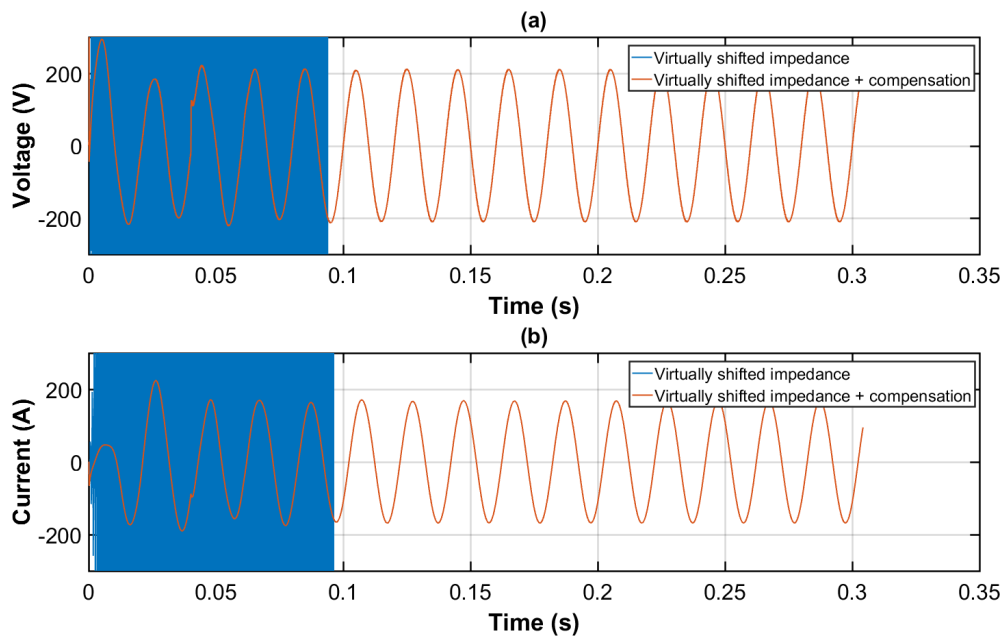


Fig. 5.13 Simulation results with $L_{shift} = 1.5mH$ for: (a) virtual impedance shifting method and (b) virtual impedance shifting with time delay compensation

ertheless, the individual implementation of the time delay compensation algorithm has proven to also enhance the stability. Therefore, for the purpose of analysing the performance of the virtual impedance shifting method, it is also compared with a PHIL simulation with time delay compensation.

In this case, according to the stability assessments both of the implementations should be stable. This is confirmed by looking at Fig. 5.14 (a) and Fig. 5.14 (b) where the voltage and current at the simulation PCC are presented. The results obtained are in line with the stability assessment performed for both of the implementations. An additional performance parameter is analysed, the RMS error of the current waveform with respect to a monolithic configuration, for assessing the accuracy performance of both implementations, which is presented in Fig. 5.15. It can be observed that the accuracy of both implementations is very similar, although during steady state the implementation with only compensation is slightly more accurate. Furthermore, a 10%

step in voltage has been produced at $t = 0.4s$ for analysing the accuracy under transient conditions; however, both configurations present very similar accuracy behaviour.

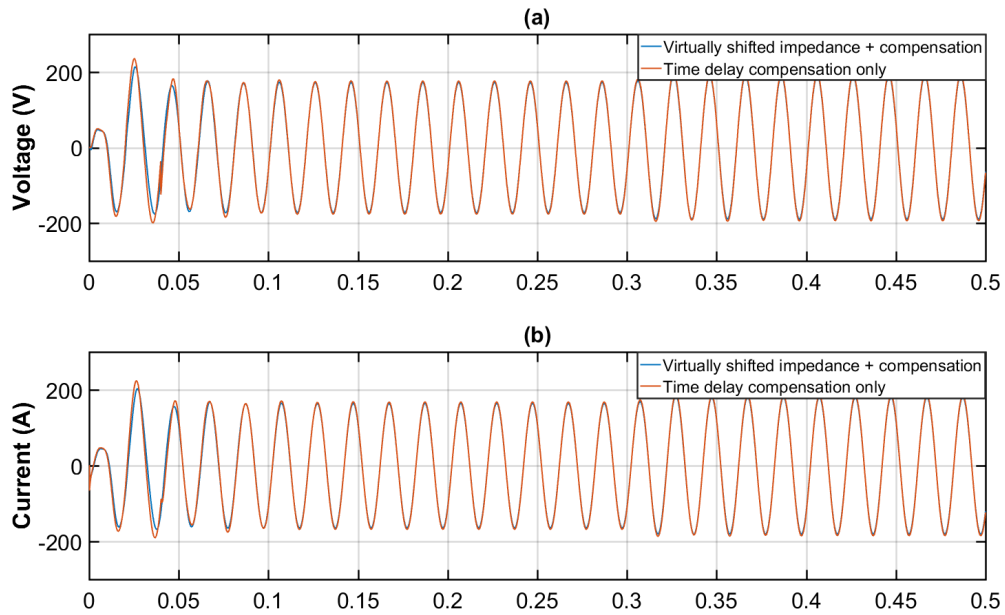


Fig. 5.14 Simulation results with $L_{shift} = 1.5mH$ for: (a) virtual impedance shifting with time delay compensation and (b) only time delay compensation.

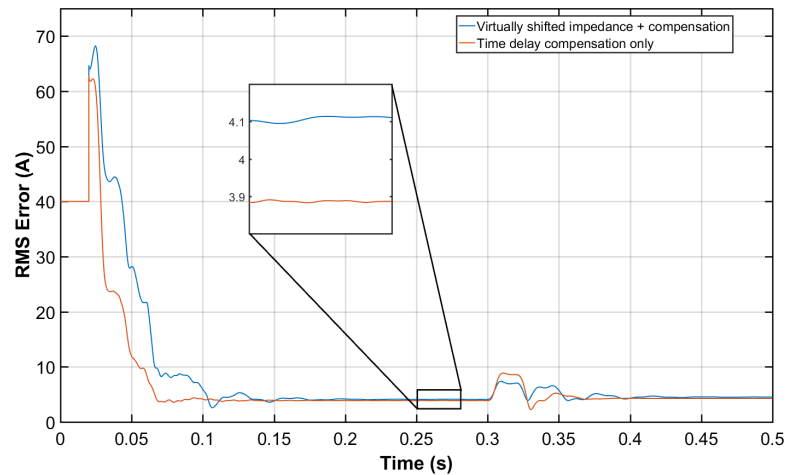


Fig. 5.15 RMS error of: (a) virtual impedance shifting with time delay compensation and (b) only time delay compensation.

With the similar behaviours in stability and accuracy presented by the virtual impedance shifting method with time delay compensation and the implementation of

only the time delay compensation it can be concluded that due to the simpler implementation as well as a reduced computation complexity of the time delay compensation algorithm, the implementation of only the time delay compensation algorithm is the recommended method for the enhancement of the stability and accuracy of PHIL simulations.

5.4 Conclusions

A novel IA, the adaptive-ITM, has been presented based on previous stability analysis performed in the literature, in which the ratio of impedances was shown as the deciding stability condition. However, with the evaluation of the adaptive-ITM it has been identified that this condition is only valid for a system where only resistive impedances are present. Therefore the application of A-ITM is possible when such a case is present in a PHIL simulation.

This has led to a more precise stability assessment in which the Routh-Hurwitz stability criteria has been used. As a result, detailed stability conditions for any type of load have been obtained in which the impedance ratio is no longer the stability condition and where the most important parameter affecting the stability of PHIL simulations with ITM IA are the inductances of the simulation and HUT.

The analysis of the stability conditions identified has contributed to the identification of a novel approach for meeting the main condition when inductances are present (the ratio of inductances). More precisely, a virtual impedance shifting method has been developed by the author. This method has been developed primarily for the improvement of the stability of PHIL simulations and accordingly the stability performance has been thoroughly evaluated. It has been found that the stability of this configuration typically requires of an additional filtering/stabilizing component for providing an improved stability performance. Consequently, the addition of the time delay compensation

algorithm (which acts as a moving average filter) has been considered, which at the same time is able to provide the accuracy improvement characteristic of the algorithm. This combination of virtual impedance shifting with time delay compensation has successfully proved the stability improvement that it can bring to PHIL simulations.

However, when this combination is compared with a PHIL configuration with only time delay compensation implemented, the performance of both implementations result in analogous performance in both, stability and accuracy. Therefore, the use of only the time delay compensation algorithm is recommended as it is a simplified approach in comparison with the virtual impedance shifting method.

Chapter 6

A novel PHIL initialization and synchronization approach for large power systems

PHIL has gained attention internationally due to its satisfactory performance for testing power and energy systems with reduced costs and risks [Edr+15; Kot+15; Kot+12; RSW07]. PHIL is preferred for testing under circumstances such as: (i) where a component is physically available and it is computationally more efficient to utilize the component within a PHIL setup rather than developing a detailed and accurate model of the component (such as photovoltaic (PV) system inverter), (ii) where novel power components need to be tested in a laboratory environment before their wide scale deployment and (iii) where the interactions of novel components with the grid need to be assessed for understanding the influence of its deployment.

The initialization of PHIL simulations has rarely been considered when performing testing and validation of power components using this approach. However, interest in applications that require larger physical systems for their validation (such as WAMPAC systems) along with the increment in distributed real-time simulations and

co-simulations [Lun+17; Ste+17b; Ste+17a], in which the initialization of the different subsystems can be critical, require of a meticulous initialization of the different subsystems.

In this chapter, the initialization and synchronization of a PHIL simulation where the HUT represents a larger portion of the test network is investigated. The options for initializing and synchronizing such PHIL configuration are presented and their applicability, advantages and disadvantages discussed. A process of initialization and synchronization using a controlled current source is further evaluated by means of two case studies undertaken on a reduced dynamic model of the Great Britain (GB) power system.

6.1 PHIL initialization and synchronization

Stability of PHIL simulations has been widely investigated in the literature [RSB08; VLF11; HRM16; DGL14; Bra17], where the main findings include the establishment of stability thresholds imposed by the IA used for the PHIL implementation. Improvements to alleviate the identified stability limitations have been proposed in [VLF11; LRM16; LS18]. However, these studies investigate the stability of an operational PHIL setup, assuming a successful simulation and hardware initialization, which have been established independently, also straightforward synchronization is assumed to be achieved. In the following sub-sections, these assumptions are shown to be a limitation for some applications and therefore options to address these challenges are explored.

6.1.1 Initialization issues

The challenges associated with initialization and synchronization of PHIL simulations emerge when the HUT represents a significant portion of the test network, such as: (i)

when the HUT is critical for initialization of the DRTS simulation and (ii) when the HUT affects the voltage and frequency of the DRTS simulation during the initialization process. These are elaborated as follows:

- **HUT critical for initialization:** In such cases, the initialization and synchronization of the PHIL experiment present a paradoxical scenario where the DRTS simulation cannot be initialized without the hardware currents, while the hardware currents cannot be produced without the DRTS simulation being initialized. For example, the DRTS simulation will fail to initialize as a result of a lack of generation, leading to insufficient synchronizing torque in the simulated network. Without the DRTS simulation initialized, the power interface will not be capable of reproducing the interface signals and therefore the HUT response cannot be synchronized. On the other hand, reproducing the interface signal during the initialization of DRTS is risky, as the signal might not be suitable for reproduction or may be beyond the safety limits of the power amplifier, the HUT or other laboratory equipment.
- **HUT affects voltage and frequency:** Here, the HUT is not critical (the simulation can start without it being connected), but it is significant enough as to affect the frequency and voltage considerably, triggering control actions from components within the simulation, leading to a modified initial state of the system, which is typically not desired. This situation can also result in impractical voltage and frequency levels for the subsequent initialization of the HUT.

6.1.2 Initialization of DRTS simulation

A solution is therefore required to overcome the aforementioned difficulties, allowing PHIL simulations to be initiated even in these situations. For this purpose, the use of an

emulated auxiliary HUT component is required. The options for emulating the HUT for enabling the initialization in such cases are identified as:

1. **Detailed simulation of HUT:** a detailed model of the HUT can be developed as part of the simulation for establishing the initial conditions of the DRTS simulation. However, creating a detailed model of the HUT can be a laborious process, and considering that the expected power flows at the PCC can typically be available for pre-set scenarios, simpler approaches may be employed for the initialization process.
2. **AC voltage source:** readily available in every power system simulation tool, voltage source models can be utilized to initialize the simulated test network. However, as AC voltage sources act as infinite sources, the power flow of the network at the PCC cannot be controlled. This would lead to, an unsuccessful initialization, as the state of the network is no longer the intended for the test scenario. Additionally, with the change in power flows, new stability analyses would need to be undertaken as the system state under which the HUT was intended to be connected is no longer the same, unless adjustment of the power setpoints is performed until the power exchanged with the infinite bus is brought to zero [Yu+16].
3. **Synchronous generator:** a synchronous generator model can control the active power at its output terminals by means of a simple set-point signal, allowing for the emulation of the required HUT active power transfers at the PCC. The reactive power of a synchronous generator is controlled adjusting the excitation system. Either manual tuning of the voltage reference to the exciter or development of a simple PI control is required to ensure the desired reactive power flow at the PCC.

4. **AC Controlled Current Source:** for the emulation of the HUT power transfer at the PCC, a controlled current source allows for a straightforward implementation with high accuracy. However, the stability may depend on the voltage source capacity of the simulated network (the stiffness of the grid). For the generation of the current signals in this approach only the measured voltage and the P and Q set points at the PCC are needed, more precisely the generated currents are calculated as:

$$I_d = \frac{P_{ref}V_d - Q_{ref}V_q}{V_d^2 + V_q^2} \quad (6.1)$$

$$I_q = \frac{P_{ref}V_q - Q_{ref}V_d}{V_d^2 + V_q^2} \quad (6.2)$$

where I_d is the direct axis current, I_q is the quadrature axis current, P_{ref} and Q_{ref} are the reference active and reactive powers to be injected at the PCC respectively, V_d is the direct axis voltage at the PCC and V_q is the quadrature axis voltage at PCC. The direct and quadrature axis voltages required can be obtained with Park's transformation as:

The three phase currents required for the current controlled source can be obtained from the quadrature and direct currents using the inverse Park's transformation as:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} \quad (6.3)$$

where θ is determined with a phase lock loop (PLL). By using this approach, the initialization is accurate and straightforward when the power transfers at the PCC are known.

The main focus here is on situations where the HUT component contributes a significant active or reactive power, without which the simulated network cannot remain

stable. In this case, the simplest approach is to implement method (4), the controlled current source. This is because it is a conventional approach that can be implemented in simulation using well-known dq axis control techniques without difficulty. These techniques are common to most conventional converter-connected generation, active front-end, and storage device technologies. In some other scenarios, it may be that the HUT properties which are required to stabilise the power network are not so much absolute balances of fundamental active and reactive power, but other properties such as synchronising torque, grid stiffness or harmonic damping. In these specific cases, a simulated HUT using a current-source approach may not be appropriate or sufficient, and a voltage-source approach may be more suitable, similarly to method (2) and (3). One potential solution has been referred to (within a simulation-only environment, without hardware) in [Yu+16].

In this chapter the AC current controlled source approach has been implemented for the initialization of a PHIL simulation. A schematic of the current source configuration for initialization purposes of PHIL simulations is shown in Fig. 6.1 for a six-area GB power system. This study presents four simulated areas within the DRTS, and two areas (Areas 1 and 2) represented in hardware. The initialization of the DRTS therefore emulates the latter with AC current sources.

6.1.3 Synchronization

In conventional PHIL simulations, the HUT is electrically coupled to the DRTS simulation (synchronized) through the action of closing a simple switch, thus closing the loop between the HUT and the DRTS. During the process of synchronization, the currents from the emulated auxiliary HUT need to be replaced with the hardware currents (i.e. the measured response from the HUT). During the process of synchronization the voltage and frequency of the network cannot exceed the safety margins of the hardware components in the laboratory, included the power interface. Additionally, when voltage

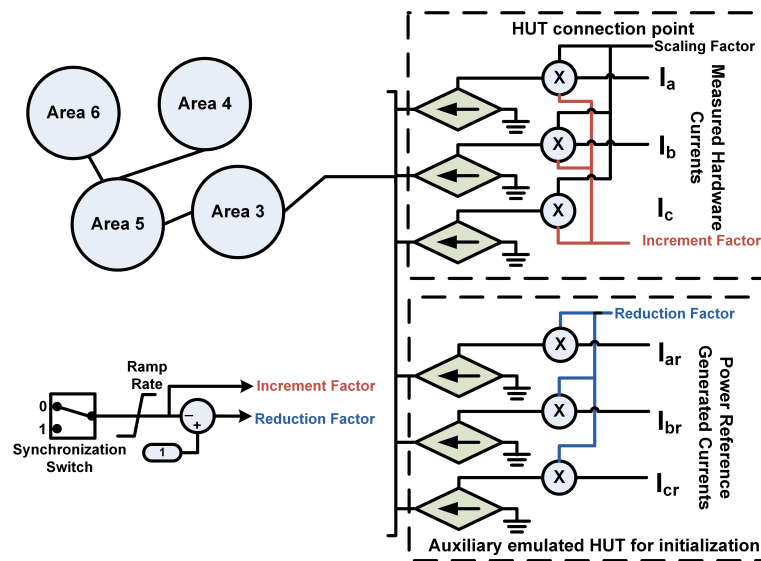


Fig. 6.1 PHIL initialization and synchronization structure used at DRTS.

or frequency control algorithms are implemented within the simulated power system, it is desired that the synchronization of the HUT causes the least possible change in system frequency and voltage for avoiding undesired control actions. The ideal synchronization method will be dependent upon the initialization approach preferred. Below, the options for performing the synchronization process are discussed.

- Detailed simulation of HUT:** This approach could be the best option for PHIL initialization purposes, assuming an accurate enough model of HUT is available; however, for the purpose of synchronization a dispatching algorithm to reduce the generation and load of the emulated HUT would be required, avoiding frequency deviations when the HUT is first connected. Subsequently, utilizing a detailed model of the HUT is highly challenging for initializing and synchronizing PHIL setups as it requires the development of dedicated HUT models and dispatch algorithms.
- AC voltage source:** This may not be the ideal approach for initialization due to its response as an infinite source, as the power output of the voltage source

cannot be directly controlled. For the synchronization process this will require of dispatch algorithm that allows the specific bus to be reduced to zero exchange of power at the same time as the HUT is connected.

- **Synchronous generator:** In order to attain a smooth transition from the emulated auxiliary HUT (the synchronous generator) and the HUT, a complex control would be needed (for the governor and excitation system) to ensure least deviation in frequency and voltage during the synchronization process. This controller would be a generic solution that could be reused; however, would be limited to scenarios where the HUT as a combination behaves as a generator only (not as a load).
- **AC Controlled Current Source:** if a controlled current source is utilized, the synchronization can be achieved with the proposed simple logic presented in Fig. 6.1. The synchronization process is initiated by means of a switch that inversely ramps up and down both controlled current sources. The ramp rate can be chosen such that it avoids creating any oscillations or transients on the system. With the currents from the emulated auxiliary HUT reduced to zero and the currents from the HUT completely connected to the simulation, the system is then said to be synchronized. Furthermore, this method allows for the detection of instabilities before the system is fully synchronized.

From these descriptions, it can be inferred that for the purpose of initialization and synchronization of PHIL setups, where the HUT represents a significant part of the test network, the most convenient option is to utilize a controlled current source. It performs ideally under all scenarios, with accurate performance and a reliable, straightforward implementation. Furthermore, it is a generic approach that can be utilized when the HUT emulates net generation or load. A recommended procedure for carrying out the initialization and synchronization is shown in Fig. 6.2 with a flowchart. This process assumes that the PHIL simulation is stable for the chosen IA. This should be ensured before the PHIL simulation initialization and synchronization procedure is initiated.

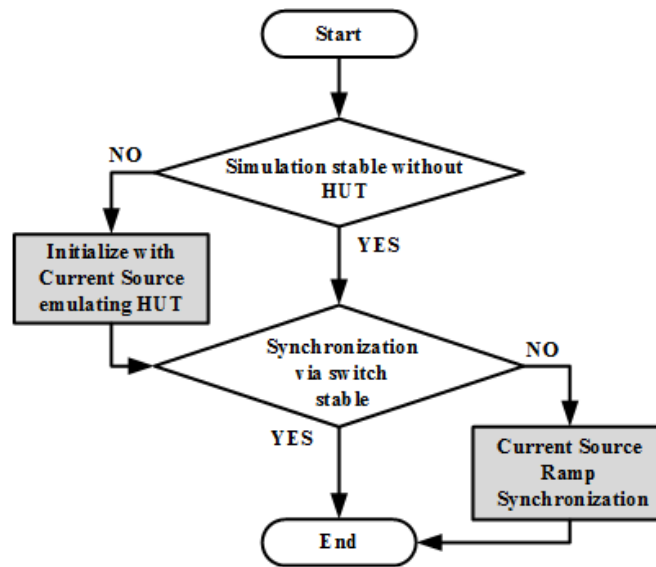


Fig. 6.2 Initialization and synchronization flowchart.

6.2 PHIL experimental configuration

The laboratory components and characteristics of the PHIL configuration selected for the validation of the proposed initialization and synchronization process are described in this section. First the real-time simulation model of the GB reference power system developed within RSCAD (power system simulation software from RTDS Technologies) is described, the characteristics of the power interface used for the interconnection of the simulated system with the hardware is presented and the HUT utilized is detailed.

6.2.1 GB Power system

A reduced six-bus dynamic model of the GB power system has been chosen to be the simulated network. A single line diagram of the GB power system is shown in Fig. 6.3 (a). The six-area power system model has been developed based on the GB National Electricity Transmission System (NETS) boundary map presented in the Electricity Ten Year Statement (ETYS) of National Grid, Transmission System Operator (TSO) of GB,

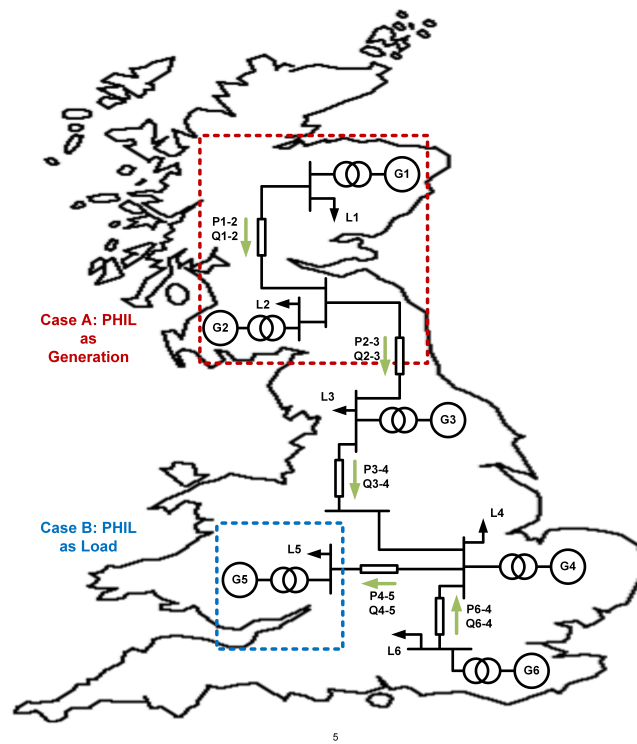


Fig. 6.3 Reduced six-bus dynamic model of the GB power system

Table 6.1 Area wise capacity and initial load condition.

	Area1	Area2	Area3	Area 4	Area 5	Area 6
Generation capacity (MVA)	11000	20000	9160	5500	15500	2000
Active power load (MW)	8468	12548	8398	2150	26852	100
Reactive power load (MVA_r)	4109	6077	4067	1041	13005	500

where the GB transmission network is grouped into six regions [Nat16]. These regions have been developed around major generation sources, power flow corridors and load centres [Nat16]. The model is based on real power flow data of the six regions. Each area is built as the combination of a lumped generator and load. Area wise generation, active and reactive power load, and inter-area power flows data is presented in Table 6.1 and Table 6.2. The model is simulated in real-time using a RTDS unit from RTDS Technologies.

Table 6.2 Inter-area power flows.

Inter-area active power flow (MW)	P1-2	P2-3	P3-4	P4-5	P6-4
	2097	8900	9105	13080	970
Inter-area reactive power flow (MVar)	Q1-2	Q2-3	Q3-4	Q4-5	Q6-4
	1328	4257	5025	7088	155

6.2.2 Power interface

The power interface is composed of a 90kVA back-to-back converter unit with a switching frequency of 8kHz responsible for amplifying the signal received from the DRTS. Different interface algorithms have been described in the literature [RSB08; LS18; LDM10; Jon11]. V-ITM IA has been selected due to its straightforward implementation and good stability performance. In the PHIL configuration used for this experiment, the power interface is also responsible for measuring the response of the HUT and sending it back to the DRTS for closing the loop with the simulation. The interface loop is implemented with an analog communication link between DRTS and the power interface. Therefore delays and noise introduced by this configuration need to be considered.

6.2.3 HUT

The HUT utilized for demonstrating the proposed initialization and synchronization process is the DPSL laboratory, which comprises a reconfigurable 125kVA, 400V three-phase AC power network with multiple controllable supplies and loads with flexible control systems and interfaces. The one-line diagram of DPSL is presented in Fig. 6.4 (b). The laboratory network is designed such that it can be split into three separate power islands (represented as cells in Fig. 6.4 (b)) with independent control, or as a centralized interconnected system.

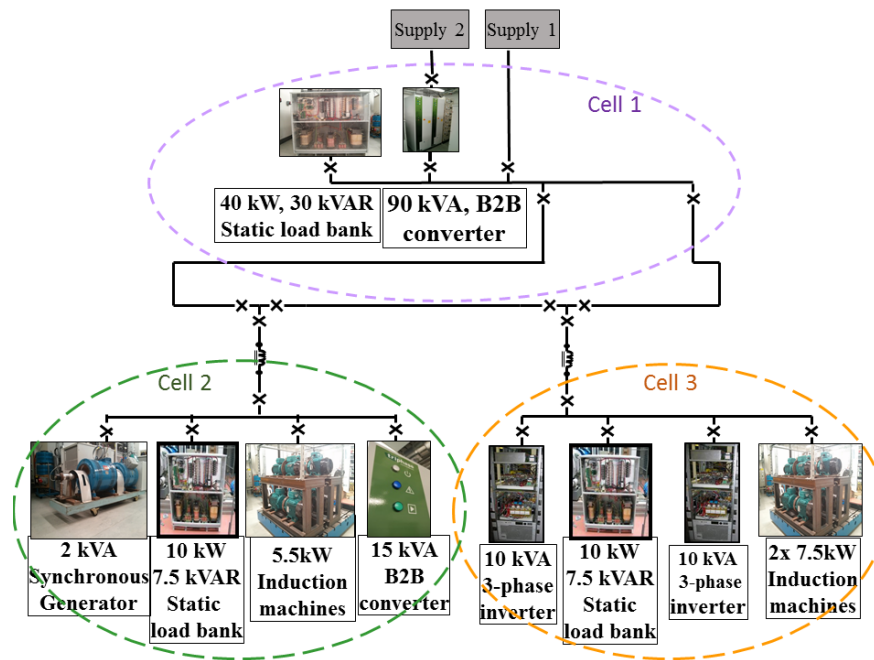


Fig. 6.4 Dynamic power system laboratory (HUT).

Only cell 2 and 3 of Fig. 6.4 (b) will form the HUT in this case, as the 90kVA unit from cell 1 will serve as the power interface. The laboratory equipment is relatively small compared to the required power transfers at the PCC, as a result the response of the HUT (the measured currents at the hardware PCC) need to be scaled up proportionally to meet the test scenario requirements. The scaling of the response does not impact the simulation results; however, it does make the system more sensitive to oscillations. Small oscillations within the HUT can now result in large power oscillations within the simulated system, which can lead to instabilities or malfunctioning of the implemented controllers. This further demonstrates the need for appropriate measures to be undertaken for initialization and synchronization, but also noise and delay variability mitigation is required for large power systems that can become sensitive to oscillations when scaled PHIL configurations are utilized.

6.2.4 Stability and accuracy considerations for the selected PHIL configuration

Stability

The stability of the proposed PHIL configuration has been proven by simulating the complete system and interface within the DRTS. The reason being that the complete model, DRTS and HUT, was already available in the simulation software. Therefore the splitting of the network has been performed in simulation to emulate the PHIL configuration, resulting in a stable PHIL system. Accordingly, due to the complex characteristics of the system under test, no additional theoretical evaluation has been performed as the stability has been confirmed with the simulation assessment.

Accuracy

For the application presented in this chapter, where active and reactive power exchanges are decisive for the precise initialization of the simulation as well as the stability of the system, the time delay introduced in the PHIL implementation is of significant importance. The main reason being the erroneous power exchanges introduced as a result of the time delay of PHIL configurations as demonstrated in Chapter 4. Furthermore, the resulting oscillations in active and reactive power produced by the variability in time delay need to be attentively considered and reduced in this case with a low pass filter as presented in Chapter 3, Section 3.5.2. The scaling of the HUT currents from laboratory scale (kVA) to simulation scale (GVA) will generate large power oscillations which can bring the system to instability or undesired control actions if no further action is taken. Accordingly, two measures have been implemented for improving the accuracy for this configuration.

First, for the mitigation of oscillations produced by the variability in time delay, as an analog communication interface is used, a low pass filter with a cut-off frequency

of 200Hz has been implemented in the current measurement feed-back path. A low cut-off frequency is required for this experiment as the scaling factor is considerably high, resulting in potentially large noise/oscillations that need to be damped. Besides, only low harmonic components presence is expected for this study and the filtering of the higher harmonic components has no relevant implications in this case.

In addition, the time delay compensation algorithm proposed in Chapter 4 is utilized for achieving accurate power exchanges and power angle/factor, consequently accomplishing the initial conditions for the experiment. With the same laboratory equipment as that of Chapter 4 being used for the experiment, the same time delay characteristics are present, more precisely $T_d = [350, 400, 1]$ with a total delay of $T_d = 383\mu s$ being compensated. However, the addition of the low pass filter introduces further delay into the system that needs to be considered. Specifically, the filter introduces a total of $\tau_{filter} = 1147.5\mu s$ which is added to the delay of the configuration, resulting in a final compensated delay of $T_d = 1530.5\mu s$. With the large delay introduced by the filter, the application of the time delay compensation becomes even more critical for such scenarios.

6.3 Experimental assessment and validation

In this section, an assessment of the proposed initialization and synchronization procedures for PHIL simulations is performed. Two case studies have been developed for this purpose, first a significant HUT that affects the PHIL initialization and synchronization if no measure is in place, followed by a case in which the simulation could be initialized without HUT, although with erroneous voltage and frequency parameters.

6.3.1 Case Study A: HUT critical for the stability of the real-time simulation.

For the first case study, the HUT represents Area 1 and 2 of the GB power system, as shown in Fig. 6.5 while the remaining areas will be part of the simulated network on the DRTS. As can be observed from Table 6.2, there is an active and reactive power flow from Area 2 to Area 3. This power flow needs to be equal to the produced by the HUT, effectively emulating generation of active and reactive power. Cell 2 and Cell 3 of the DPSL represent Area 2 and Area 1 respectively, while the 90kVA back-to-back converter is used as the power interface.

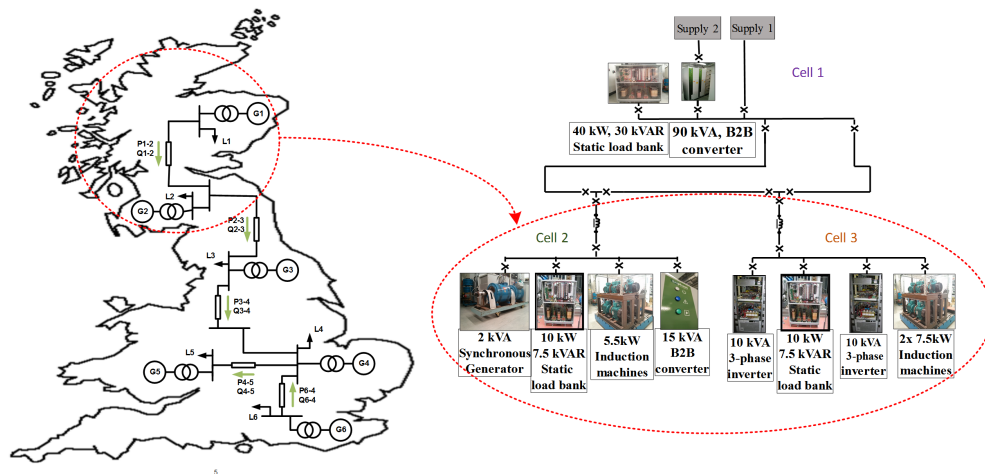


Fig. 6.5 System configuration for Case Study A.

Initialization

The active and reactive power flows from Area 2 to Area 3 are 8900 MW and 4257 MVAR respectively. When the HUT representing Area 1 and 2 is not connected to the simulated system, the remainder of the simulated GB power system (Area 3-6) within RSCAD, fails to initialize due to a lack of generation, expected to be produced by Area 1 and 2. The HUT emulates a large generation portion and the DRTS simulation model

is unstable without the HUT. Hence, the process shown in Fig. 6.2 is followed, where initialization of the real-time system with one of the initialization techniques presented is required. The AC current source approach for initialization is implemented due to its simplicity and its suitability to perform the synchronization process as previously discussed.

The schematic of the methodology used for initializing and synchronizing this PHIL implementation has been presented in Fig. 6.1. As can be observed from the figure, the auxiliary emulated HUT (the controlled current source in this case) is utilized to reproduce currents generated from the power reference i.e. 8900 MW and 4257 MVAR. Once the real-time simulation is initialized and attained steady state, the PCC voltages (scaled down to 400V) are reproduced in the laboratory using the power interface. Attempting to reproduce the simulation voltages when the simulation is not yet stabilized or initialized properly, can damage the hardware components as large transients or/and oscillations can occur. When stable voltage is achieved and successfully reproduced at the laboratory, HUT components are then connected and initialized.

Synchronization

The main objective of the synchronization is to replace the auxiliary currents generated by the controlled current sources with the measured HUT currents. This should be performed so that there is least change in frequency and voltage during the process of synchronization and least impact on the stability of the simulated network. With the DRTS successfully initialized, the voltage from the simulation is then reproduced by the power interface, allowing for the set reference power to be injected into the PCC. In this case, the net generation is produced by the 15 kVA back-to-back converter, the synchronous generator in Cell 1 and the 10 kVA inverter in Cell 2. A load bank has been added in each of the cells to represent the local loads within the two areas. By

Table 6.3 Power setpoints for hardware components for case study A.

Area	Component	P(W)	Q(Var)
Cell 2	15kVA B2B Inverter	7000	3600
	2kVA Synchronous Generator	1500	0
	Load Bank 2	-1500	0
Cell 3	10kVA Inverter	6600	1100
	Load Bank 3	-3300	0

using these three power sources, the maximum power injection is limited to 27 kVA. The parameters used for the different hardware components are listed in Table 6.3. In order to represent the 8900 MW and 4257 MVAR from Area 2, the hardware currents are scaled by means of a scaling factor. For this study, the scaling factor is chosen as $k = 9 \times 10^5$.

Consequently, the measured HUT currents, when injected into the simulation, should be equal to the auxiliary emulated HUT currents. In this case, the currents are being generated by small scale power converters which can produce harmonic components that when scaled up can generate significant distortion. This will also be mitigated with the introduced low pass filter for mitigating the oscillations produced by the variability in time delay. The results for the time delay compensation in this implementation are presented in Fig. 6.6 (a).

Once the measured hardware currents (after scaling) and the auxiliary signals used for initialization produce the same magnitude and phase, the replacement process is initiated with the activation of the synchronization switch shown in Fig. 6.1. The currents are then ramped up and down simultaneously over a period of 90 seconds as shown in Fig. 6.6 (b). The frequency and voltage at the PCC during the process of synchronization are presented in Fig. 6.6 (c) and 6.6 (d) respectively. As can be observed from the two figures, although the HUT currents have been compensated for the time delay and filter delay and are approximately similar to the emulated currents

(as shown in Fig. 6.6 (a)), there is a change in both voltage and frequency during the process of synchronization. The change in frequency is less than 0.02% and the change in voltage is less than 0.05%. This is mainly due to small inaccuracies such as losses in small impedances, measurements and control inaccuracies of the hardware assets, which in this case are not affecting to the PHIL implementation.

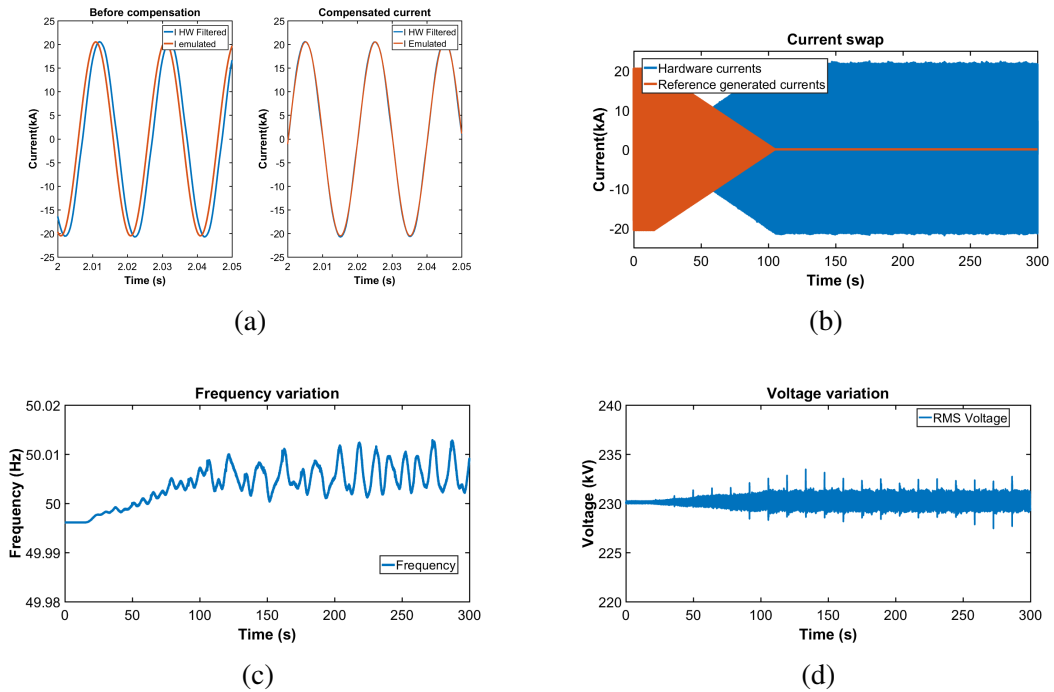


Fig. 6.6 Results for study case A: HUT critical for stability of RT simulation, (a) time delay compensation, (b) currents swapping during synchronization, (c) frequency at PCC during synchronization and (d) voltage at PCC during synchronization.

The ramp rate utilized is necessary for minimizing such impacts during the process of synchronization. Synchronizing without a ramp rate, risks transients being introduced. The ramp rate is dependent upon the acceptable variation on voltage and frequency during the process of synchronization. With the PHIL simulation fully synchronized and the power transfers set as required by the scenario, the testing of, for example, new power system control algorithms in a more realistic environment is made possible.

6.3.2 Case Study B: HUT affecting voltage and frequency during initialization.

In this case study, the HUT represents Area 5 of the GB power system, as shown in Fig. 6.7. As can be observed from Table 6.2, there is an active and reactive power flow into Area 5. Therefore, in this case, the HUT effectively emulates a consumer area at the PCC. Cell 2, Cell 3, and the 40 kVA load bank of Cell 1 combined represent Area 4, while the 90 kVA power converter from Cell 1 is used as the power interface. The specific setpoints used for each of the components in each cell are presented in Table 6.4.

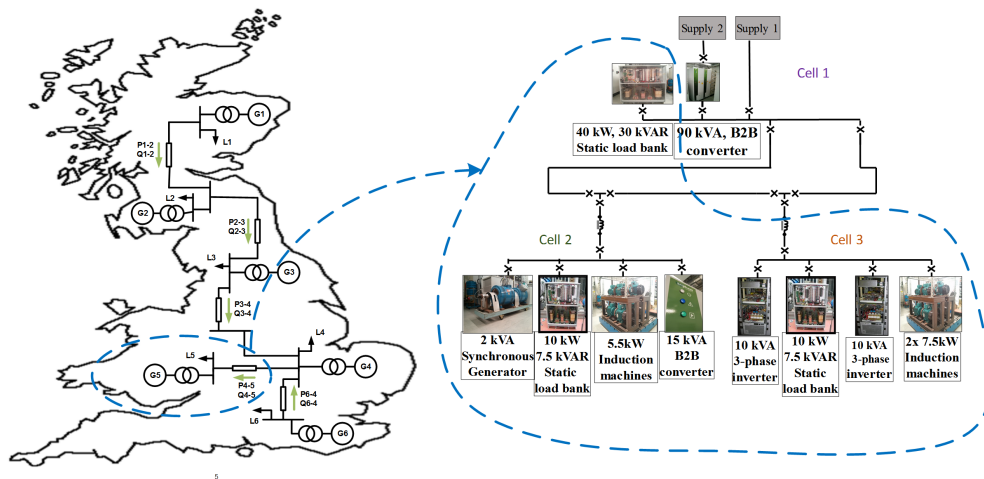


Fig. 6.7 System configuration for Case Study B.

Initialization

The schematic of the PHIL interconnection within RSCAD is presented in Fig. 6.8. The HUT emulates net consumption, and so the measured current will have opposite direction to case A and will be drawing power from the simulated power system (through the power interface). For representing the 13080 MW and 7088 MVar absorbed by

Table 6.4 Power setpoints for hardware components for case study B.

Area	Component	P(W)	Q(Var)
Cell 1	Load Bank 1	-14000	-7900
Cell 2	15kVA B2B Inverter	4500	-3000
	2kVA Synchronous Generator	1000	0
	Load Bank 2	-9000	-3500
Cell 3	10kVA Inverter	5200	0
	Load Bank 3	-9000	-3500
	Induction motor	-4700	-3000

Area 5, the hardware currents are scaled by means of a scaling factor. The scaling factor in this case is set to $k = 5 \times 10^5$.

In this case, the remainder of the GB power system (Areas 1-4 and 6) simulated within RSCAD would initialize without Area 5, as there is enough generation to support the network, unlike case A, but the system frequency would be above the initial condition (as no dispatching algorithm is implemented). The frequency deviation depends upon the droop settings. This is again undesirable as this would activate any frequency control algorithms implemented within the system. There is, of course, an option to de-activate the control during the synchronization process. However, there might be hardware limitations on the value of frequency that can be sustained/emulated within the laboratory. To avoid such risks, an auxiliary component should be utilized to initialize the test network for PHIL simulations. A dynamic load or a controlled current source can be used for this purpose.

The schematic for initialization and synchronization of PHIL at the RTDS with the current source as the initialization and synchronization component is shown in Fig. 6.8. The reference currents for the auxiliary current source can be generated as presented in Section 6.3.1. A dynamic load could be also used for the initialization, however depending on the simulation software used this can have different forms. For example, within Simulink simulation software the dynamic load is equivalent to a

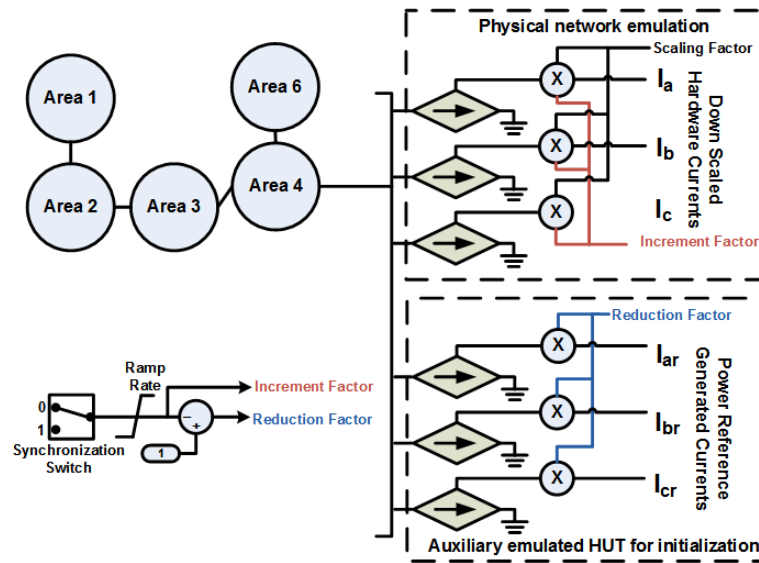


Fig. 6.8 PHIL configuration for case study B with current source.

current source, hence the method would be equivalent to the current source method presented before (and therefore can be utilized for case A and B), while within RSCAD (RTDS simulation software tool) the dynamic load model does not allow for negative power set points (rendering it unusable for case A).

Synchronization

If the current sources are used for the initialization, the same process of synchronization as presented in Section 6.3.1 can be used. In this case, the dynamic load model could also be utilized indistinctly. However, if a dynamic load is being utilized, instead of using current set points, active and reactive power set points are required (as presented in Fig. 6.9), and these can be calculated as:

$$P_{SP_dynamic} = P_{ref} - P_{HW} \quad (6.4)$$

$$Q_{SP_dynamic} = Q_{ref} - Q_{HW} \quad (6.5)$$

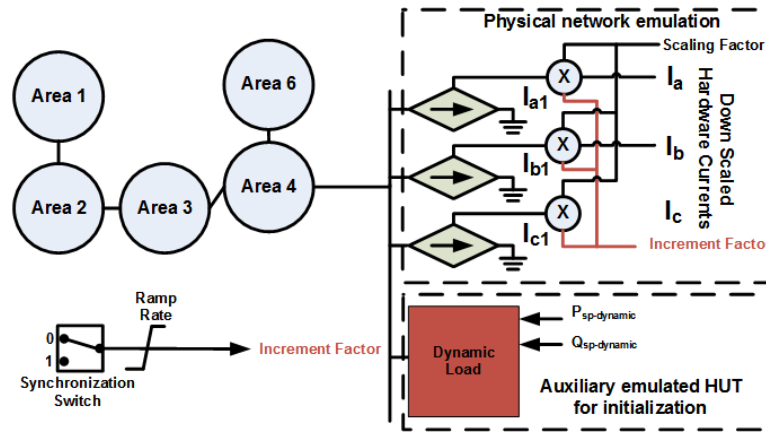


Fig. 6.9 PHIL configuration for case study B with dynamic load.

where P_{HW} and Q_{HW} are the active and reactive power drawn by the hardware respectively, and can be calculated as:

$$P_{HW} = V_a I_{a1} + V_b I_{b1} + V_c I_{c1} \quad (6.6)$$

$$Q_{HW} = \frac{1}{\sqrt{3}} (V_a (I_{b1} - I_{c1}) + V_b (I_{c1} - I_{a1}) + V_c (I_{a1} - I_{b1})) \quad (6.7)$$

where V_{abc} are the three phase voltages at PCC and I_{abc1} are the currents measured at the PCC after the increment factor. For this scenario, the current source model has been implemented. It can be observed from Fig. 6.10 that by initializing and synchronizing the PHIL implementation with the current sources, the frequency and voltage at the PCC remain at the same steady state levels as before the connection with the HUT. Also, due to the nature of the hardware used and the real measurement devices, which can introduce some noise into the signals, the frequency and voltage waveforms show more realistic dynamics in comparison with a pure simulation.

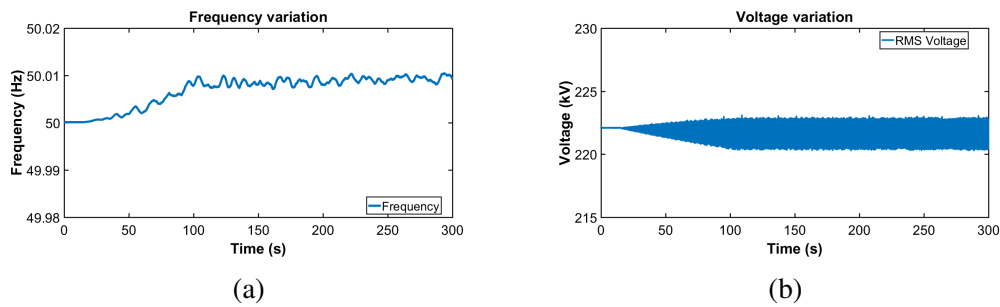


Fig. 6.10 Results for case B: affecting voltage and frequency during initialization (a) Frequency variation, (b) voltage variation

6.4 Conclusions

PHIL simulations can be complex to initialize and synchronize depending on the HUT and its significance to the dynamic behaviour and stability of the overall system under test. These circumstances represent a limiting factor on the range of scenarios in which PHIL can be applied.

In this chapter a range of possible methodologies for enabling the initialization and synchronization of such scenarios have been discussed. The evaluation of the proposed candidates has led to the identification of a recommended approach that uses current sources for initialization and symmetrical ramping rates for synchronization of PHIL simulations. As a result, improved performance and extended range of feasible PHIL scenarios can now be performed. The proposed initialization approach has been validated by experimentation of two different and realistic scenarios for the GB power system, where an accurate initialization is not possible without the proposed approach.

Furthermore, the time delay compensation algorithm presented in Chapter 4 along with one of the proposed mitigations techniques for the time delay variability (low pass filter) have also been integrated within the experiment, demonstrating the importance of its application into PHIL simulations.

Thus, safer and more stable PHIL simulations can now be carried out, which enable the validation of new distributed controllers and power system components in a wider range of realistic scenarios with PHIL.

Chapter 7

Conclusions

7.1 Conclusions

This thesis has presented evidence of the need for improved testing methodologies (such as PHIL simulations) for the analysis and validation of future power systems and their novel components. The complexity of future power systems and their components introduce challenges and limitations into traditional testing approaches that need to be resolved. PHIL is one of the validation approaches developed for this transition into more complex power systems; however, it also presents limitations on its stability and accuracy performance.

Accordingly, the main challenges and limitations of PHIL simulations have been introduced in Chapter 2. Since stability and accuracy of PHIL simulations are the main challenges, the components within the implementation that affect these aspects have been identified and described. This has led to the identification of potential improvements for PHIL simulations such as the mitigation of the effects introduced by time delays, the improvement of the stability of interface algorithms or the enhancement of conventional PHIL initialisation approaches.

A novel method to accurately characterize the time delay of PHIL implementations has been proposed in Chapter 3. The characterization is considered as a necessary first step towards the development of techniques for the mitigation of the impact that time delay introduces. The approach presented provides considerably more comprehensive, specific and accurate evaluation than conventional time delay identification techniques, reducing the risks when performing PHIL simulations.

The experimental validation of the method has identified a novel dynamic behaviour of the time delay. Crucially, and for the first time, variability in the time delay has been identified, which is introduced by the components with fixed time-step computation. The variability has been recognized as a source of inaccuracies and incorrect stability assessments, even when the simulation and interface use digital communications. This behaviour has also been integrated within the developed characterization method.

Cancellation of the variability in time delay has been proposed with the introduction of an optimization algorithm for the simulation time-step, reducing the noise of the signals on the implementation and consequently improving the accuracy. However, when analog communication is used in practice, uncertainties in exact time delay characterisation may mean that a deliberate addition of a low pass filter in the loop is a more appropriate solution in some scenarios. Therefore, mitigation techniques for the reduction of the overall time delay as well as its variability have been described, which application results in an improved accuracy of the PHIL simulation.

A new method for the compensation of time delay in PHIL simulations has been accomplished in Chapter 4, which improves the stability and accuracy of the experiments. The presented approach transforms the signal of interest from the time domain into the frequency domain and compensates for the time delay by phase-shifting the signal, in a phase-by-phase and harmonic-by-harmonic manner. The implementation of the time delay compensation has proven experimentally to improve the accuracy performance of PHIL simulations, which are now capable of accurately reproducing

the existing power exchanges between simulation and hardware during steady-state conditions. In addition, the use of SDFT for the compensation algorithm introduces an improvement on the stability of the system, increasing the gain and phase margins considerably. The applicability and performance of the method has been successfully validated in a laboratory environment. Computationally, it has been shown that only $\frac{1}{3}\mu s$ is required to compensate an individual harmonic component in each phase, so 43 harmonics can be compensated in $43\mu s$, the upper limit defined by the stability and amplifier bandwidth.

An adaptive interface algorithm (adaptive-ITM) has been developed for the improvement of the stability of conventional ITM IAs used for PHIL simulations. The stability enhancement has been validated for scenarios where the simulation and HUT impedance are only resistive. However, when other types of impedance are present, the stability condition for ITM IAs is no longer the ratio between the simulation and HUT impedance magnitudes and the proposed interface cannot be operated accurately due to the inconsistency of the stability condition.

For the determination of the stability condition of such cases, a thorough stability assessment has been performed for ensuring a correct interpretation of the stability conditions. As a result, it has been identified that when inductances are present in the implementation, the stability condition is mainly driven by the ratio of inductances. Furthermore, it is also established that an inductance in series with the HUT can improve the stability of the simulation.

Therefore, a novel virtual impedance shifting method has been proposed based on the stability conditions identified from the stability assessment for ITM algorithms when inductances are present, which typically rely on the ratio of inductances between simulation and hardware. Hence, by virtually shifting impedance from one subsystem to the other for meeting the stability conditions, the stability of PHIL simulations is

improved, increasing the applicability of the method in comparison with the current method based on the physical addition of impedances.

Moreover, the virtual impedance shifting method can be implemented simultaneously to the time delay compensation method. Nevertheless, when using the time delay compensation approach on its own, the stability of the simulation is comparable to that of the combination of virtual impedance shifting with the compensation algorithm included. The reason being that, the filter used for the SDFT calculation is the main component providing the enhancement in stability in both configurations. Therefore, for simplicity and computation performance, the implementation of only the time delay compensation is preferred.

A solution for the initialization of PHIL simulations has been proposed and experimentally validated, allowing for systems which would otherwise be unstable to be initialized in a safe manner and to be implemented for any PHIL simulation (not only the unstable ones). With the proposed addition of controlled current sources and synchronized ramping for the interconnection of the subsystems during the initialization process, PHIL simulations can now be performed for scenarios where PHIL subsystems were not able to be initialized independently.

In conclusion, this thesis has realised and proved different advanced techniques to improve PHIL simulations for a more accurate and reliable testing of power systems and novel components in a laboratory environment.

7.2 Further Work

7.2.1 Adaptive interface algorithms

The adaptive-ITM IA presented in Chapter 5 is only applicable for PHIL simulations with only resistive components. However, the adaptability of PHIL IA should also be

considered for other PHIL implementations. Therefore, adaptability of the interface depending on the stability conditions is of interest for an increase of resilience and applicability of PHIL simulations.

7.2.2 Improve applicability of time delay compensation

A novel time delay compensation algorithm has been developed in Chapter 4 for use in PHIL simulations. Nevertheless, its application into other simulation and testing approaches in which a system is divided into subsystems, such as distributed real-time simulations or co-simulations, should also be investigated. Accordingly, the integration of the time delay compensation algorithm within the DRTS or other real-time or simulation tools is also of interest.

7.2.3 Online stability identification

With stability being one of the critical aspects for PHIL simulations, the development of an online stability identification tool would be valuable. This could be performed by assessing certain (predetermined or calculated online) stability conditions or perhaps detecting characteristic oscillations that suggest that the stability of the system is under risk. Accordingly, this would allow for the start of a controlled shut down procedure of the PHIL simulation or, even better, for adapting the interface in order to continue with the simulation in a safe manner. Besides, the identification of stability conditions under the presence of non-linear loads within PHIL simulations would be valuable for achieving accurate adaptive-ITM and DIM IAs performance.

7.2.4 Standardization of PHIL configurations and procedures

A number of possibilities are available for performing PHIL simulations, with different IAs, power amplifiers, communication links and even DRTS available for selection. However, there is no guide or standard that provides clear guidance on how to perform a PHIL simulation for achieving the required goal, for example, what are the minimum requirements that a PHIL simulation have to meet for performing compliance testing of different power system components? Answering this question will greatly improve the applicability of PHIL simulations.

7.2.5 PHIL with large penetration of power converters

For the initialization of PHIL simulations with high penetration of power converters, it may be that the HUT properties which are required to stabilise the power network are not so much absolute balances of fundamental active and reactive power, but other properties such as synchronising torque, grid stiffness or harmonic damping. In these cases, a simulated HUT using a current-source approach may not be appropriate or sufficient, and a voltage-source approach may be more suitable. These type of solutions could be explored in future work, and one potential solution has been referred to (within a simulation-only environment, without hardware) in [Yu+16].

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