Enhancing Offshore Wind Farm Transmission Efficiency: HVDC Converters and DC Collection Systems

PhD Thesis

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Abstract

Offshore wind energy is one of the fastest-growing renewable energy sources, driven by consistently higher wind speeds and the availability of large installation areas. However, challenges persist, including the substantial size and weight of collection systems and the need for efficient long-distance power transmission to shore. This thesis aims to develop offshore wind power transmission systems that deliver higher efficiency, reduced costs, and minimized size and weight.

The research begins with the investigation of onshore voltage source converter (VSC)-based high-voltage direct current (HVDC) systems. Three new HVDC converter topologies are proposed, combining half-bridge submodules (HB-SMs), a minority of full-bridge submodules (FB-SMs), and antiparallel thyristors. The inclusion of thyristors improves converter efficiency and provides DC fault-blocking capability with the support of FB-SMs. Additionally, the proposed designs reduce the number of semiconductors required, resulting in cost-effective solutions.

The first topology uses thyristors in series with both HB-SMs and FB-SMs to enhance efficiency. However, its DC fault-blocking performance is relatively slow as it relies on thyristor commutation to block the AC component of the DC fault current from the grid.

The second topology addresses this limitation by employing additional thyristor branches parallel to the submodules. These branches bypass the AC fault component swiftly, isolating the DC side and enabling fast fault-blocking action.

The third topology further improves efficiency by leveraging these parallel thyristor branches during normal operation. Known as power groups, each group consists of SMs in parallel with thyristor branches. The thyristors bypass the SMs when generating zero voltage, reducing conduction losses and enhancing overall efficiency.

The thesis then focuses on the DC collection system, proposing a novel series-isolated parallel (SIP) DC collection architecture. This architecture comprises parallel wind turbine groups (WTGs), each consisting of series-connected wind turbines (WTs). The series-connected WTs utilize three-phase uncontrolled rectifiers on their DC sides, significantly improving system efficiency. Each WTG integrates a DC-DC converter that steps up the group voltage to the HVDC transmission level while isolating faults within the series string. The proposed SIP architecture enhances reliability by isolating faults at the WTG level

without requiring costly DC circuit breakers. Compared to conventional DC parallel architectures, the SIP approach achieves lower costs, reduced size and weight, and improved reliability, providing a more efficient and practical solution for offshore wind energy collection and transmission.

List of Abbreviation

AAC	Alternate arm converter
AFC	Active forced commutated
AT-AAC	Augmented trapezoidal alternate arm converter
CB	Circuit breaker
CPVC	Constant pitch voltage control
CTB-MMC	Crossing thyristor branches modular multilevel converter
DAB	Dual active bridge
EO-AAC	Extended overlap alternate arm converter
F-HTMC	Fast DC fault-blocking Hybrid thyristor-based multilevel converter
FB-MMC	Full-bridge modular multilevel converter
FB-SMs	Full-bridge submodules
HB-MMC	Half-bridge modular multilevel converter
HB-SMs	Half-bridge submodules
HACC	Hybrid alternate common arm converter
HTMC	Hybrid thyristor-based multilevel converter
HVAC	High voltage alternating current
HVDC	High voltage direct current
IPOS	Input parallel output series
LCC	Line commutated converter
LV	Low voltage
MEMC	Modular embedded multilevel converter
MMC	Modular multilevel converter
MPPT	Maximum power point tracking
MV	Medium voltage
MVAC	Medium voltage alternating current
NLC	Nearest level control
NPC	Neutral point clamped
PG	Power group
PLL	Phase locked loop
PMSG	Permanent magnet synchronous generator
PPPC	Partial power processing converter

P-WF	Parallel wind farm
S-WF	Series wind farm
SIP-WF	Series isolated parallel wind farm
SISO	Series-input-series-output
SP-WF	Series parallel wind farm
TB-MMC	Thyristor bypass-based modular multilevel converter
VPVC	Variable pitch voltage control
VSC	Voltage source converter
WF	Wind farm
WT	Wind turbine
WTG	Wind turbine group
ZVS	Zero voltage switching

List of Symbols

V_c	SM capacitor voltage
V_{c_n}	SM capacitor nominal voltage
V_{dc}	DC link voltage
ΔV	FB-SMs voltage
$\hat{v}_a$	Overall phase peak voltage
$\hat{v}_{a_1}$	Fundamental phase peak voltage
v_{a_1}	Fundamental phase voltage
v_{a_3}	Injected third harmonic voltage
k_3	Third harmonic voltage ratio
v_a	Overall phase voltage
v_{arm}	Arm voltage
v_{stack}	SMs voltage per arm
v_{valve}	Series-thyristor voltage per arm
T_c	Overall commutation time
t_q	the circuit commutation turn off time of the thyristor
T_f	Falling time of the thyristor current
T_{ov}	Overlap time between the upper and lower arms
T_p	Periodic time
ΔV_{pu}	Per unit value of the FB-SMs voltage
n_{FB}	Total FB-SMs number in each arm
n_{HB}	Total HB-SMs number in each arm
V_{thy_n}	Thyristor nominal voltage
L_a	Arm inductance
σ	maximum permitted turn-on current ramp rate of the thyristor
v_L	Arm inductance voltage
$\hat{\imath}_a$	Peak phase current
i_{arm}	Arm current
N_t	Total number of SMs per arm
ΔE_{SM}	Energy deviation of each SM in the arm
P_{stack}	SMs power per arm

n_{SM}	Total number of functionable SMs during conducting periods of the SMs
$\|\bar{S}\|$	Apparent power
$\hat{\imath}_{a_1}$	Fundamental phase peak current
ϕ	Power factor angle
$\Delta E_{SM_{pu}}^{pp}$	per unit peak-to-peak energy deviation
$\Delta E_{SM_{max}}^{pp}$	maximum peak-to-peak energy deviation
ΔV_r^{pp}	desired peak-to-peak voltage ripple ratio
C_{SM}	SM capacitance
P_r	Rated power
v_g	Grid voltage
f	Fundamental Frequency
L_{AC}	AC interfacing inductance
C_{HB}	HB-SMs capacitance
C_{FB}	FB-SMs capacitance
R_{fault}	Fault resistance
v_a^+	Upper SMs voltages per arm
v_a^-	lower SMs voltages per arm
V_{comm}^+	SMs commutation voltage of the upper arm
V_{comm}^-	SMs commutation voltage of the lower arm
i_a^+	Upper arm current
i_a^-	Lower arm current
P_{ac}	AC side active power
P_{dc}	DC side active power
I_{dc}	DC link current
i_{a_1}	Phase ‘a’ fundamental current
i_{b_1}	Phase ‘b’ fundamental current
i_{c_1}	Phase ‘c’ fundamental current
n_{OpTh}	Number of operation-thyristors (series thyristors) per arm
n_{PrTh}	Number of protection thyristors (parallel thyristors) per arm
n_{SM}^+	Number of functionable SMs during conducting periods of the SMs in the upper arm

n_{SM}^{-}	Number of functionable SMs during conducting periods of the SMs in the lower arm
P_a^+	Power of upper arm of phase 'a'
ΔE_{SM}^+	Energy deviation per SM in the upper arm
i_a^+	Upper arm current
ΔE_{HBSM}^+	energy deviation of the HB-SM
ΔE_{FBSM}^+	energy deviation of the FB-SMs
k_1	Fundamental voltage ratio
v_{stack_pred}	SMs predicted voltage
N_{SM}	Number of inserted SMs per arm
$N_{SM\ pred}$	Predicted number of inserted SMs per arm
$V_{c\ av\ PG\ i,..m}$	PG average capacitor voltages of all PGs
$PG_{i,..m}$	PG activation signals
$PG_{ready\ i,..m}$	PG ready signals
$Thy_{PG_{i,..m}}$	PG-thyristors gating signals
$N_{comp_{i,..m}}$	The voltage sign of the used FB-SMs in the activation/deactivation process
$N_{SMs_{actual}}$	The required number of inserted SMs
$N_{SMs_{comp}}$	The compensated number of inserted SMs
N_{PG}	number of activated PGs
$n_{SM\ PG}$	number of SMs per PG
$n_{FB\ PG}$	number of FB-SMs per PG
$n_{HB\ PG}$	number of HB-SMs per PG
k_{PG}	ratio of the number of activated PGs to the minimum required number of PGs
ΔN_{PG}	change in the number of activated PGs
$\hat{v}_{stack}$	Peak voltage of the SMs per arm
m	Total number of PGs per arm
$\hat{v}_{PG}$	Maximum voltage capability of each PG
$v_{thy\ valve}$	voltage of the series thyristors-valve
$\hat{v}_{thy\ valve}$	Peak voltage of the series thyristors-valve
$n_{thy\ valve}$	Number of bidirectional thyristors per thyristors-valve

n_{avail}	number of available SMs (the total number of SMs in the activated PGs)
L_{PG}	PG inductor
$V_{L_{PG}}$	The voltage used to turn on/off the PG-thyristors
i_{circ}	circulating current between the upper and lower arms
C_{stack}	SMs stack capacitance
V_{comm_2}	
$\hat{\imath}_{arm}$	Arm current peak
M	Number of parallel wind turbine groups
N	Number of series wind turbines per group
P_m	power generated by the wind turbine
c_p	power coefficient of the wind turbine
R	radius of the WT blade
ρ	air density
v_w	wind speed
λ	tip speed ratio of wind turbine
β	pitch angle of wind turbine
ω_m	Rotor speed
L_s	PMSG inductance
$E_{PM_{LL}}^{RMS}$	RMS line-induced voltage of the PMSG
ω_e	electrical angular velocity
$I_{t_1}^{RMS}$	fundamental RMS current of the PMSG
k_{PM}	stator field constant
p	pole pair number of the PMSG
P_e	Electrical power of the PMSG
ω	Operating angular frequency
ω_o	First resonant frequency of LLC resonant converter
ω_p	Second resonant frequency of LLC resonant converter
$E_{PM_{LN}}^{RMS}$	RMS phase-induced voltage of the PMSG
G_c	voltage gain of the LLC resonant converter
L_s	Series inductance of LLC resonant converter
C_s	Series capacitance of LLC resonant converter
L_p	parallel inductance of LLC resonant converter

Q	equivalent quality factor
n_t	turns ratio between the input and output sides of LLC resonant converter
m	ratio between $L_p + L_s$ and L_s of LLC resonant converter
P_c	power of the LLC converter unit
V_{o_c}	Output voltage of the LLC converter unit
V_{in_c}	Input voltage of the LLC converter unit
V_{MV}	Input voltage of the whole DC-DC converter
$\omega_{m_{Imax}}$	Rotor speed at the maximum DC current

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Chapter 1
Introduction

1. 1 Background

Renewable energy sources, such as solar and wind energy, have minimal negative impacts on the environment due to their minimal secondary waste. Hence, they are regarded as clean and sustainable energy sources [1]. Among these, wind energy is more widely implemented on a large production scale and is considered more reliable. Furthermore, offshore wind farms (WFs) are deemed even more feasible than their onshore counterparts [2]. Offshore wind energy has experienced substantial growth, with technological advancements reshaping the industry and enabling projects in previously inaccessible areas. Larger and more efficient wind turbines are now capable of generating greater power, while innovative foundation designs allow for installations in deeper waters. Sophisticated grid integration strategies ensure the smooth delivery of electricity to existing networks. These advancements have positioned offshore wind energy as a competitive alternative to fossil fuel-based power generation, attracting investment and driving rapid global deployment [3]. However, challenges remain. Offshore wind farms are typically located far from shore, requiring extensive transmission networks to transport power over long distances. Additionally, the size and weight of the converters needed for transmission create significant design and logistical obstacles. Addressing these challenges is essential for supporting the continued growth of the offshore wind energy industry.

1.1.1 HVDC Power Transmission for Offshore WFs

Traditionally, high-voltage alternating current (HVAC) technology has been used to transmit power from offshore wind farms to onshore grids. HVAC offers the advantage of avoiding the need for costly power converters on both offshore and onshore sides. However, as the transmission distance increases, so do power losses and the demand for reactive power compensation [4]. With offshore wind farms moving farther offshore to harness higher wind speeds, HVAC becomes increasingly uneconomical for long-distance transmission. In such scenarios, high-voltage direct current (HVDC) technology offers a more practical solution [5].

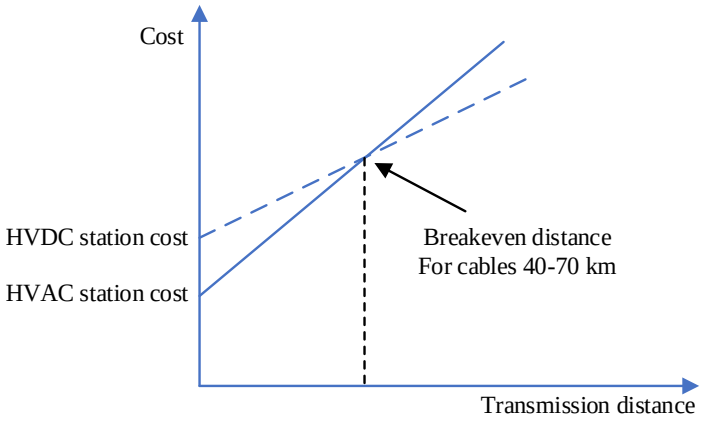


Fig. 1.1. Cost comparison between HVDC and HVAC stations against the cables transmission distance [6].

The cost comparison between HVAC and HVDC against the transmission distance as shown in Fig. 1.1 reveals a critical transmission distance typically between 40 and 70 km for subsea cables beyond which HVDC becomes more cost-effective [6]. Moreover, Table **1.1** shows some of the operational HVDC-based offshore WT power transmission projects. Most of the projects in the table are located in Germany except for Rudong which is in China. Hence, Germany owns the largest total capacity of offshore wind farms in operation.

Table 1.1: HVDC-Based offshore WF power transmission projects [7].

Project name	Distance [km]	Capacity [MW]	Voltage [kV]
BorWin1	125+75	400	±150
BorWin2	125+75	800	±300
BorWin3	130+30	900	±320
DolWin1	75+90	800	±320
DolWin2	45+90	916	±320
DolWin3	80+80	900	±320
HelWin1	85+45	576	±250
HelWin2	85+45	690	±320
SylWin1	160+45	864	±320
Rudong	70	1100	±400

HVDC systems are broadly categorized into two types: voltage source converter (VSC)-based HVDC systems and line-commutated converter (LCC)-based HVDC systems. LCC systems, first introduced in 1954 [8], offer advantages such as high surge current endurance, high efficiency, and robust DC fault ride-through capability [9]. However, LCC

systems are prone to commutation failure due to their reliance on grid voltage for thyristor operation. They also produce AC harmonic currents, necessitating large filters, and require extensive reactive power compensation due to their inability to independently control reactive power [10]. In contrast, VSC-based HVDC systems address many of LCC drawbacks. They enable independent control of active and reactive power, can connect to weak AC grids, and eliminate the need for large filters [11]. However, these benefits come at the cost of reduced efficiency, higher expenses, and the lack of inherent DC fault-blocking capability [12].

1.1.2 DC vs AC Collection for Offshore WFs

Offshore wind farms have traditionally employed AC collection systems operating at medium voltage (MV) levels (33 kV or 66 kV). In these systems, each wind turbine (WT) is equipped with a transformer that steps up the voltage to medium voltage AC (MVAC). Moreover, a large offshore HVDC converter station, including an additional bulky transformer, further steps up the voltage and converts it to HVDC for transmission, as illustrated in Fig. 1.2 [13].

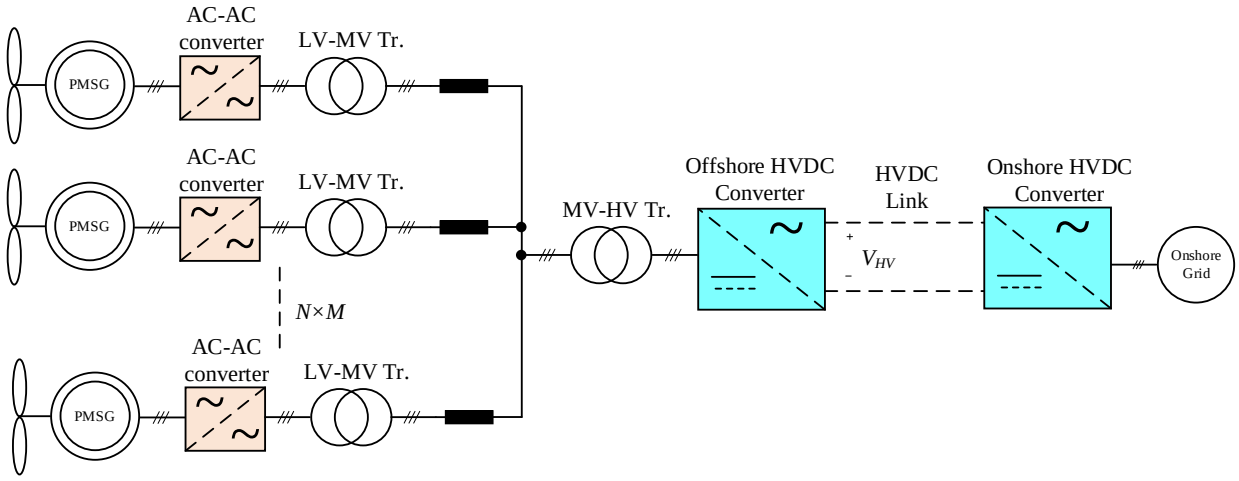


Fig. 1.2. Traditional AC Collection system for offshore wind farms.

Alternatively, DC collection systems offer significant reductions in size and weight by using medium-frequency transformers within DC-DC converters, rather than relying on low-frequency transformers [14]. The simplest form of DC collection architecture is the parallel wind farm (P-WF), where a DC-DC converter at each WT boosts the voltage from low voltage (LV) levels at the rectifier terminals to MV levels. A second DC-DC converter subsequently steps up the voltage to the HVDC transmission level, as shown in Fig. 1.3. However, this architecture suffers from higher overall losses compared to AC collection systems due to its multiple conversion stages [15].

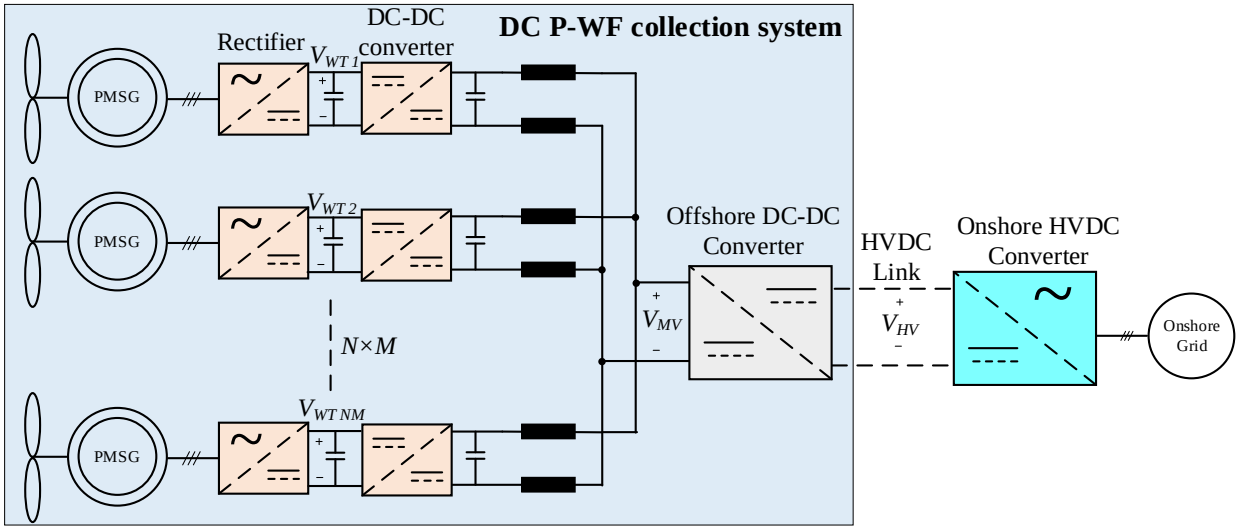


Fig. 1.3. DC parallel wind farm (P-WF) collection architecture.

However, DC collection in offshore wind farms faces several challenges, including technological gaps at the component level, controllability of DC collection systems, and compliance with current requirements for onshore grid connections [16]. Moreover, some studies suggest that DC collection-based offshore wind farms may be more expensive than conventional AC collection-based offshore wind farms [17].

1. 2 Motivation and Objectives

The global transition to renewable energy, driven by the need to reduce carbon emissions, has led to significant growth in wind energy as a reliable and widely adopted solution for large-scale power generation. offshore WFs, considered more dependable than their onshore counterparts, have experienced remarkable expansion due to technological advancements enabling projects in previously inaccessible areas. Despite this progress, offshore WFs face critical challenges, including the need for long-distance power transmission to shore and the size, weight, and efficiency limitations of offshore collection systems.

HVDC transmission systems are the most suitable technology for long-distance power transmission, offering high efficiency and reliability. Among these, the half-bridge-based modular multilevel converter (HB-MMC) is the most established VSC-based HVDC converter. However, the HB-MMC exhibits lower efficiency compared to LCC-based HVDC systems. Moreover, it lacks inherent fault tolerance unless expensive DC circuit breakers are employed. Researchers have proposed integrating full-bridge submodules (FB-SMs) into MMCs to achieve DC fault-blocking capability. However, this approach increases both converter cost and losses. Consequently, a significant research gap exists in developing a

VSC-HVDC converter that combines high efficiency, low cost, and robust DC fault-blocking capabilities.

For offshore WF collection systems, DC architectures have been explored as a means to significantly reduce size and weight by utilizing medium-frequency transformers in DC-DC converters instead of traditional low-frequency transformers. The DC parallel wind farm (P-WF) collection system utilises two DC-DC conversion stages boost the rectifier LV output to HVDC transmission levels as previously discussed. However, this approach results in higher overall losses compared to AC collection systems due to multiple conversion stages. There remains a pressing need for research to develop DC collection systems that optimize efficiency, reduce costs, and ensure high reliability.

This research aims to address these challenges by enhancing the overall offshore WF power transmission systems, improving efficiency, reducing costs, and minimizing size and weight. The focus is on advancing both onshore HVDC converters and offshore collection systems, as depicted in Fig. 1.4. The specific objectives of this thesis include:

- **Developing innovative HVDC converter topologies** to enhance the efficiency, reliability, and cost-effectiveness of offshore wind energy power transmission by reducing conduction losses, component count, and overall system costs while maintaining DC fault-blocking capabilities.
- **Performing a comprehensive comparative analysis** of the proposed HVDC converters with existing onshore HVDC converter designs in the literature, highlighting their relative advantages in terms of cost, efficiency, reliability, and fault tolerance.
- **Building an experimental prototype** to validate the proposed HVDC converter's operation and performance under realistic conditions, bridging the gap between theoretical designs and practical implementation.
- **Proposing a novel DC collection system architecture** tailored for offshore wind farms, providing high efficiency while ensuring fault tolerance and maximizing energy capture.
- **Designing and validating control strategies** for offshore WF collection systems that enable maximum power point tracking (MPPT) under varying operating conditions.

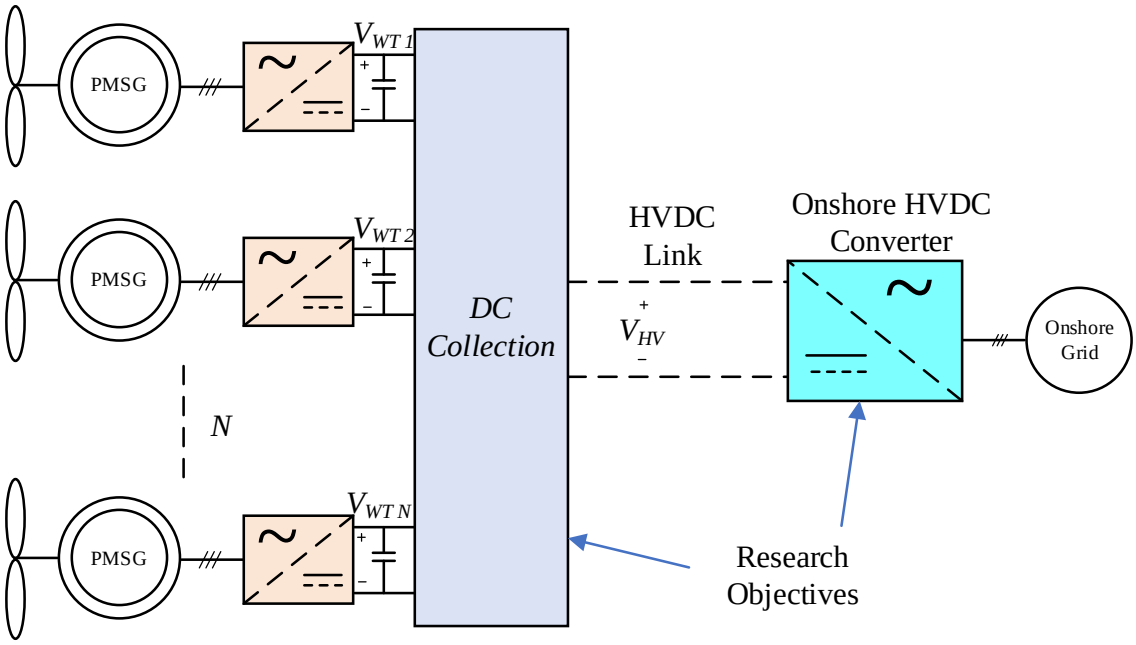


Fig. 1.4: Offshore WF power transmission systems research enhancement.

1. 3 Publication

I. **Y. N. Abdelaziz**., K. H. Ahmed, and B. W. Williams. "New hybrid thyristor-based multilevel converter with DC fault blocking capability, for HVDC applications." *IEEE Transactions on Power Electronics*, Oct. 2023.

II. **Y. N. Abdelaziz**, K. H. Ahmed, and B. W. Williams. "New fast DC fault blocking hybrid thyristor-based multilevel converter for offshore networks." *2024 Energy Conversion Congress & Expo Europe (ECCE Europe), Darmstadt, Germany, 2024, pp. 1-6*

III. **Y. N. Abdelaziz** and K. H. Ahmed. "Novel DC Series-Isolated-Parallel Wind Farms Architecture with DC Fault-Tolerance Capability", *IEEE Transactions on Sustainable Energy* (Under Review).

IV. **Y. N. Abdelaziz**, K. H. Ahmed, and B. W. Williams. "Novel Power Group Thyristor based Multilevel Converter for Offshore HVDC Power Transmission", *IEEE Transactions on Industrial Electronics* (Under Review).

1. 4 Thesis Structure

The structure of this thesis is as follows:

Chapter 2 This chapter provides a comprehensive literature review on the development of VSC-based HVDC converters, categorizing them into non-thyristor-based and thyristor-based designs. Additionally, it explores DC collection systems, focusing on parallel, series, and series-parallel wind farm architectures. The review highlights the advancements and challenges in these technologies, setting the stage for the proposed contributions in subsequent chapters.

Chapter 3 illustrates the first proposed HVDC converter, starting with its architecture, operational principles, and performance under normal and DC fault scenarios. A detailed parameter design is provided, along with simulation results from a MATLAB/SIMULINK model. Experimental validation is carried out using a scaled-down three-phase, five-level test rig. The chapter concludes with a comparative analysis of the proposed converter against other designs in the literature, emphasizing its unique advantages.

Chapter 4 focuses on the second proposed HVDC converter, detailing its structure and analysing its behaviour during normal operation. It presents a DC fault-blocking methodology, system specifications, and validation through a 401-level MATLAB simulation model. A summarized comparison with other DC fault-blocking topologies highlights the superiority of the proposed converter.

Chapter 5 details the third proposed HVDC converter with a focus on its architecture and operational analysis. A control algorithm, including a DC fault-blocking mechanism, is detailed alongside the design procedures for the converter. The chapter also includes a case study with practical parameters, MATLAB/SIMULINK model validation, and experimental results. A comparative analysis with DC fault-tolerant PG-based HVDC converters showcases the converter's performance.

Chapter 6 is dedicated to the proposed series-isolated-parallel wind farm (SIP-WF) architecture, providing an in-depth description and mathematical analysis of the wind turbines and DC-DC converters used in the system. A case study explores the limitations of the architecture, and control algorithms for two proposed methods are presented. Validation through MATLAB simulations and a comparison with the P-WF architecture using real wind data demonstrate the SIP-WF's advantages.

Chapter 7 concludes the thesis with a summary of the main findings and contributions of the research. Suggestions for future work are provided, focusing on areas

that could build upon the advancements made in this thesis, ensuring further development in HVDC converters and offshore wind farm collection systems.

Chapter 2

Literature Review

This chapter reviews advancements in HVDC converters and DC collection systems for offshore wind farms, focusing on their evolution, challenges, and trade-offs. HVDC converters have progressed from non-thyristor-based modular multilevel converters (MMCs) to thyristor-integrated designs, improving DC fault tolerance and efficiency but increasing complexity and cost. For DC collection systems, three architectures are examined: parallel (P-WF), series (S-WF), and series-parallel (SP-WF). P-WF offers high reliability but incurs higher losses, S-WF enhances efficiency with fewer conversion stages but faces reliability and fault-tolerance challenges, and SP-WF balances these issues while encountering wind curtailment and operational limitations. These developments highlight ongoing efforts to optimize offshore wind energy transmission.

2. 1 HVDC Converters Development

As established in the previous chapter, VSC-based HVDC technology overcomes many drawbacks of LCC-based HVDC systems. However, it has limitations, including lower efficiency, higher cost, and lack of DC fault tolerance. This section investigates how VSC-based HVDC converters have been developed to address these drawbacks. VSC-based HVDC converters are categorized into non-thyristor-based (only IGBTs) and thyristor-based converters, as shown in Fig. 2.1.

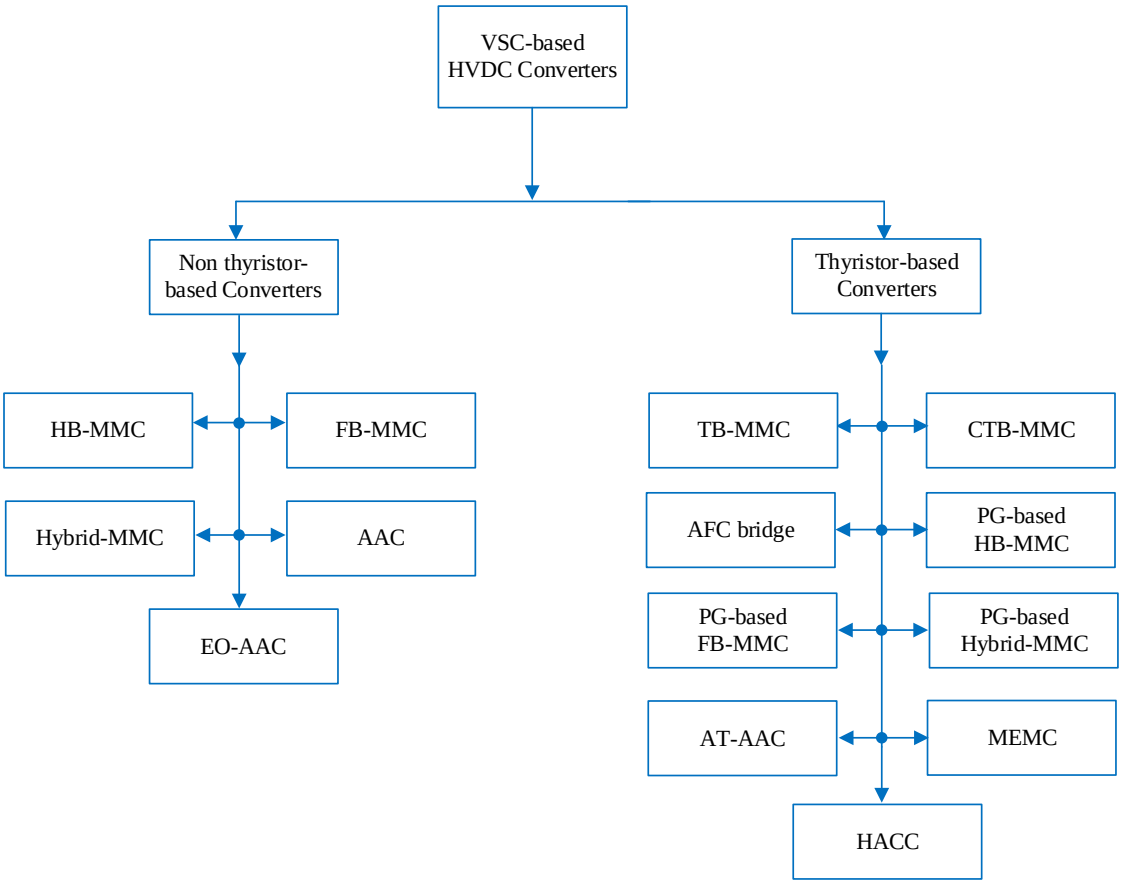


Fig. 2.1. Classification of VSC-based HVDC converters

2.1.1 Non-thyristor-based VSC-HVDC Converters

The most widely used converter in this category is the modular multilevel converter (MMC), introduced in [18]. The half-bridge MMC (HB-MMC) is extensively employed due to its modularity, scalability, redundancy, and controllability. The HB-MMC consists of six arms, each comprising cascaded half-bridge submodules (HB-SMs), as illustrated in Fig. 2.2. Each HB-SM can operate in three states: inserted (outputting capacitor voltage V_c), bypassed (outputting zero voltage), or blocked (stopping gate signals to the IGBTs during faults). In the blocked state, current can still flow from the AC to the DC side through diodes [19]. Compared to traditional two-level VSCs, HB-MMC offers higher efficiency due to low-frequency operation, though it remains less efficient than LCC-based converters.

Various modifications to HB-MMCs aim to enhance efficiency and reduce the number of components [20]. However, they remain non-DC fault-tolerant [21, 22], requiring expensive DC circuit breakers (CBs) to manage DC faults [23, 24], which increase system costs and losses.

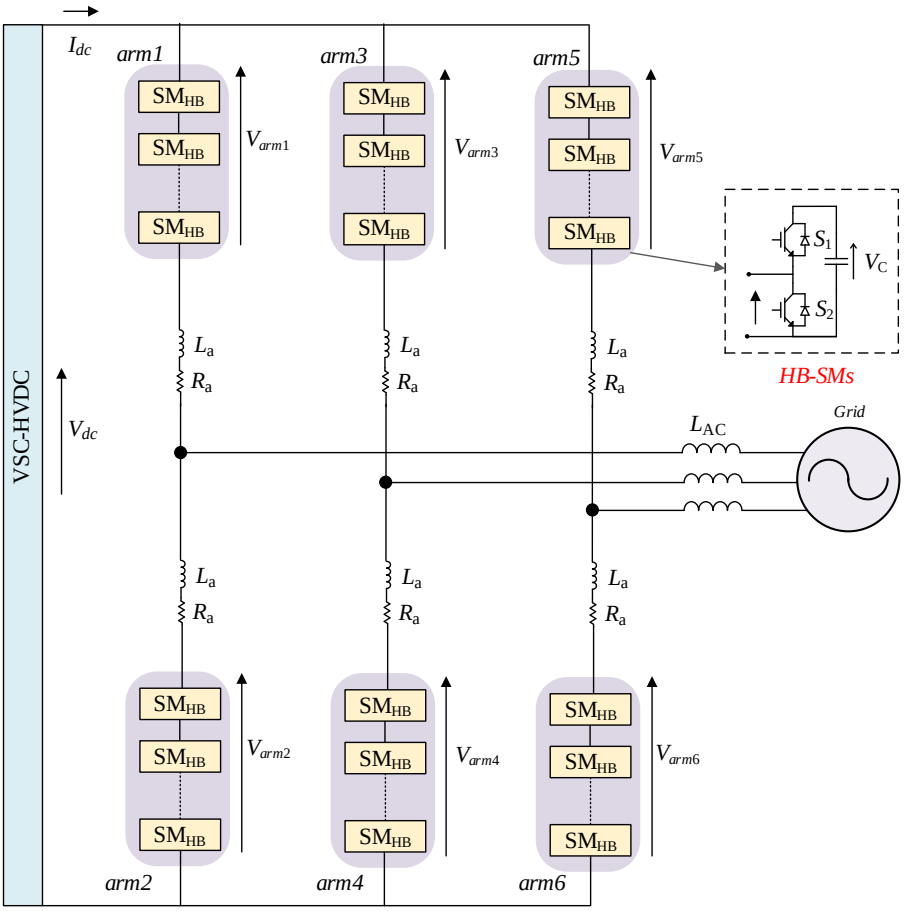
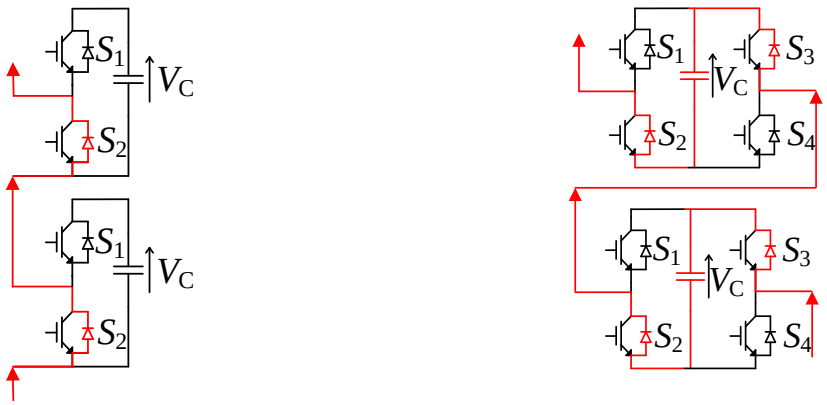


Fig. 2.2. HB-MMC converter architecture

In an attempt to address the lack of DC fault tolerance, the full-bridge MMC (FB-MMC) was developed. The FB-MMC replaces the HB-SMs with full-bridge submodules (FB-SMs), as shown in Fig. 2.4. FB-SMs can generate positive (V_c), negative ($-V_c$), or zero voltage. In the blocked state, where all the gating signals to the IGBTs are mitigated, FB-SMs fully prevent current flow, providing DC fault-blocking capability. However, this comes at the cost of doubling the number of semiconductors in the converter, which significantly increases its cost and reduces its efficiency [25].

To illustrate the difference between HB-MMC and FB-MMC in terms of DC fault interruption capability, assume a DC fault occurs at the DC side of each converter. In case of the HB-MMC, HB-SMs cannot block DC fault currents even if their gate signals are blocked, as the current would still flow through their diodes, as illustrated in Fig. 2.3(a). Conversely, FB-SMs, when in the blocking state, can inject a negative voltage to block the fault current, as depicted in Fig. 2.3(b). Therefore, during a DC fault, if both HB-SMs and FB-SMs are blocked, only the FB-SMs actively contribute to fault current suppression.



(a) (b)

Fig. 2.3. SM action during blocking state during DC fault occurrence (a) HB-SM, (b) FB-SM.

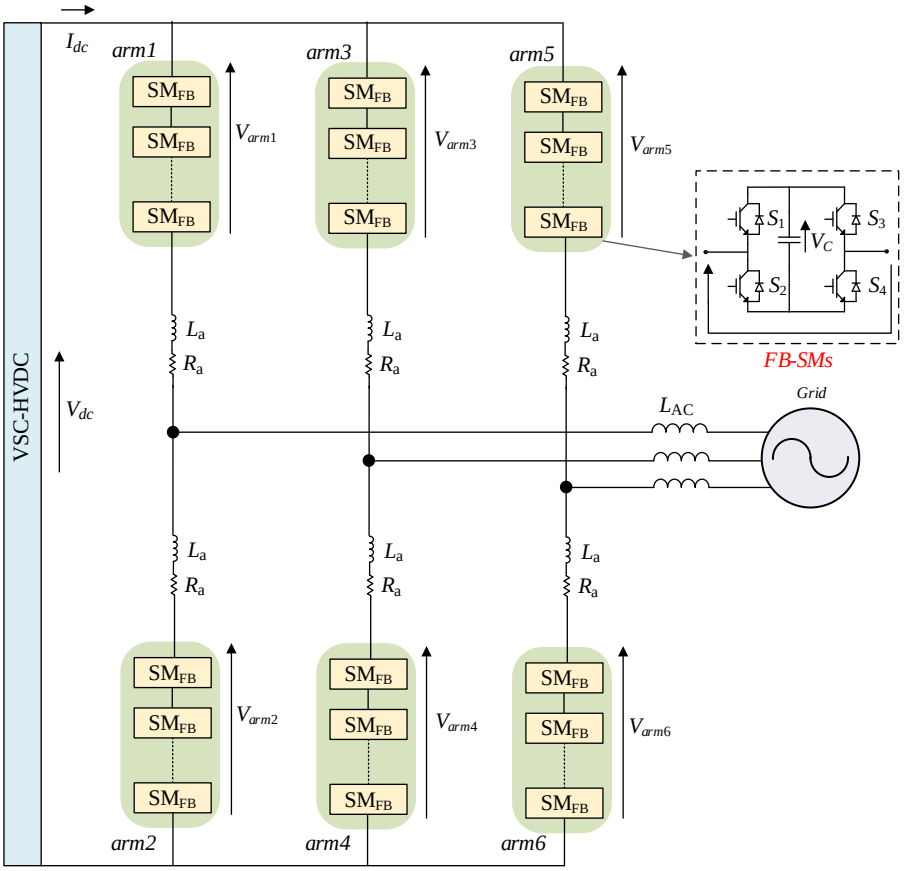


Fig. 2.4. FB-MMC converter architecture

Building on the FB-MMC, the hybrid-MMC design was introduced in [26, 27]. This design replaces some of the FB-SMs with HB-SMs, as shown in Fig. 2.5. By adjusting the ratio of FB-SMs to HB-SMs, this hybrid design offers DC fault-blocking capability while using fewer semiconductors than the FB-MMC. Despite achieving a reduction in semiconductor count, the hybrid MMC still has lower efficiency compared to the HB-MMC.

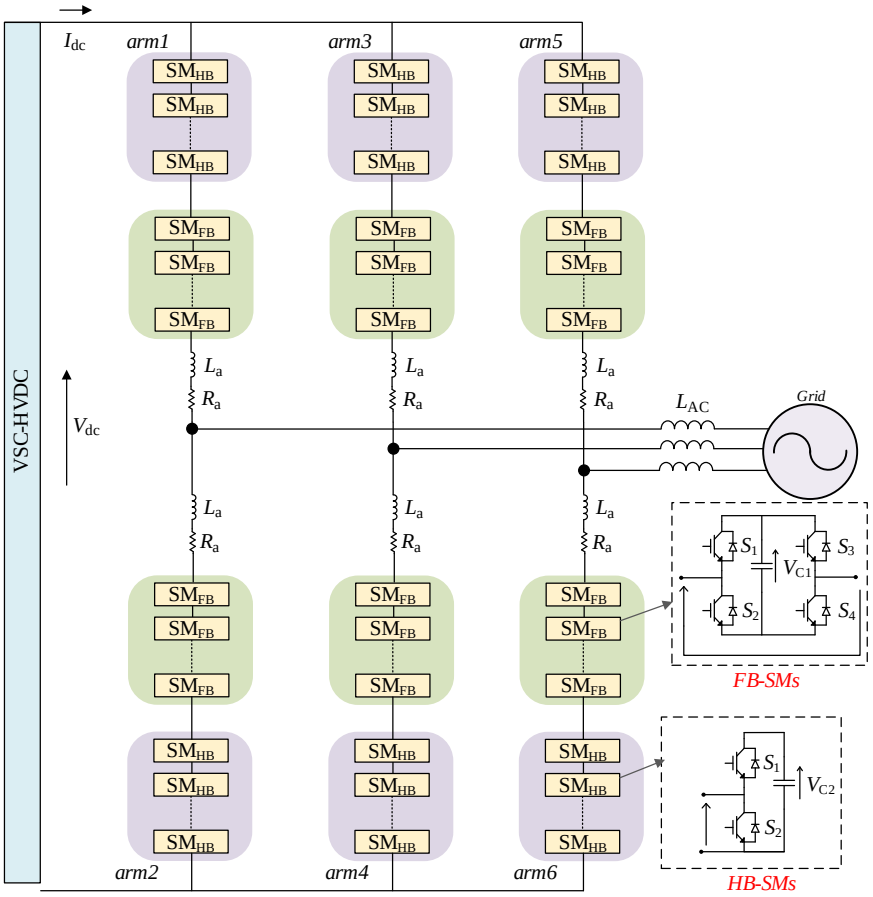


Fig. 2.5. Hybrid MMC converter architecture

An alternative modification to the FB-MMC is the alternate arm converter (AAC), proposed in [28]. This design replaces some of the FB-SMs with director switches (composed of series-connected IGBTs), as shown in Fig. 2.6. The AAC design achieves DC fault blocking with fewer semiconductors and reduces capacitance requirements, resulting in a smaller and lighter converter. Additional research into the AAC converter has led to improvements in its operation [29-31], including the extended overlap AAC (EO-AAC), which achieves a smoother current waveform and a wider operational range by subtracting a third harmonic component from the fundamental waveform. This modification, however,

requires an increased number of FB-SMs in each arm. Despite these advancements, AAC-based converters still exhibit lower efficiency than HB-MMCs and LCCs.

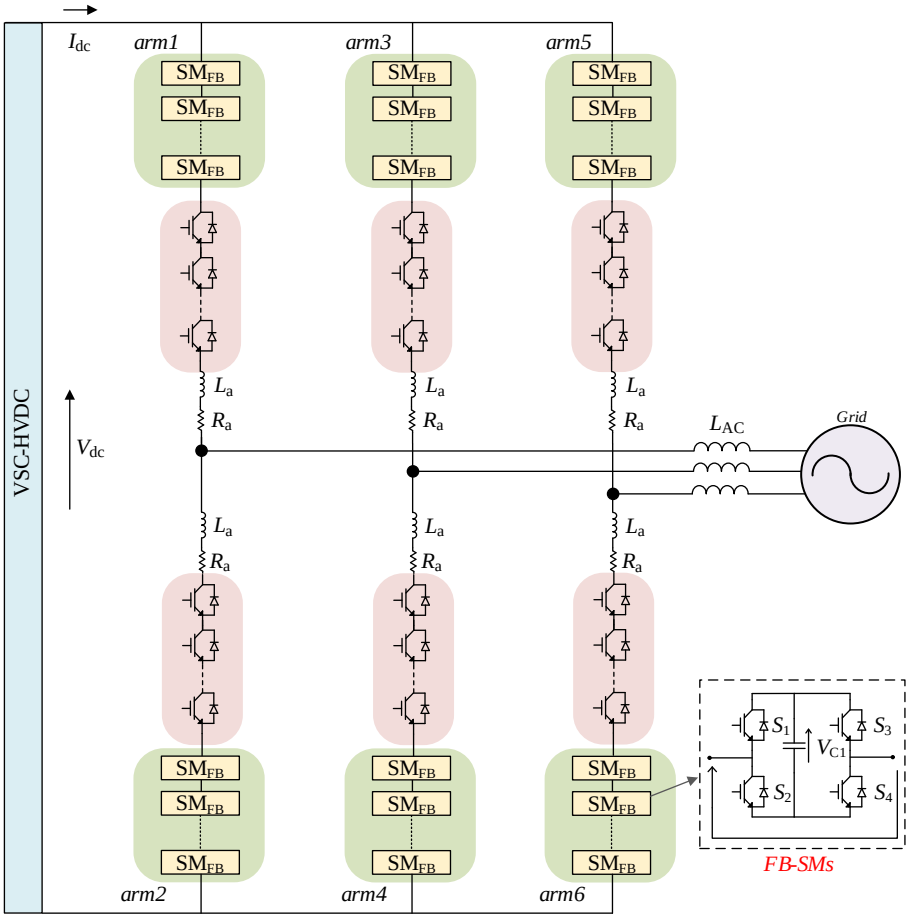


Fig. 2.6. Alternate arm converter (AAC) architecture

2.1.2 Thyristor-based VSC-HVDC Converters

Researchers have also explored the integration of thyristors into VSC-HVDC converters to improve efficiency and provide DC fault-handling capabilities.

One approach, known as the thyristor bypass-based MMC (TB-MMC), was proposed in [32]. In this design, thyristors are combined with a standard HB-MMC to add DC fault-blocking capability. As shown in Fig. 2.7, the two switches are normally closed during normal operation, and the thyristors remain in reverse blocking mode. When a DC fault occurs, the thyristors are fired, bypassing the HB-SMs, and the two switches are opened once the current in the HB-SMs drops to zero. This allows the thyristors to block the fault current in a manner similar to LCC-based converters.

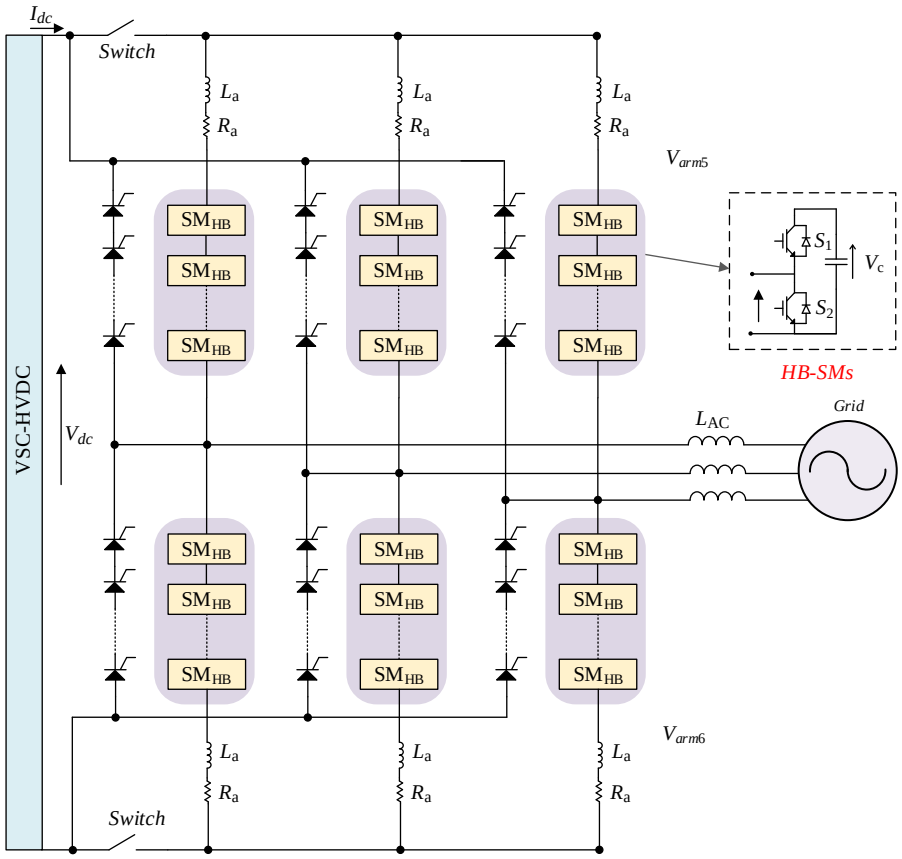


Fig. 2.7. Thyristor bypass-based MMC (TB-MMC) architecture

Another approach is the crossing thyristor branches-based MMC (CTB-MMC), proposed in [33]. This design uses unipolar FB-SMs and crossing thyristor branches to manage fault current, as shown in Fig. 2.8. The unipolar FB-SMs serve to terminate the DC component of the fault current, while the thyristor branches short-circuit the AC component, isolating it from the DC side. Since the thyristors in this configuration are only fired during faults, this topology relies solely on SMs during normal operation, and as a result, does not take advantage of lower thyristor conduction losses.

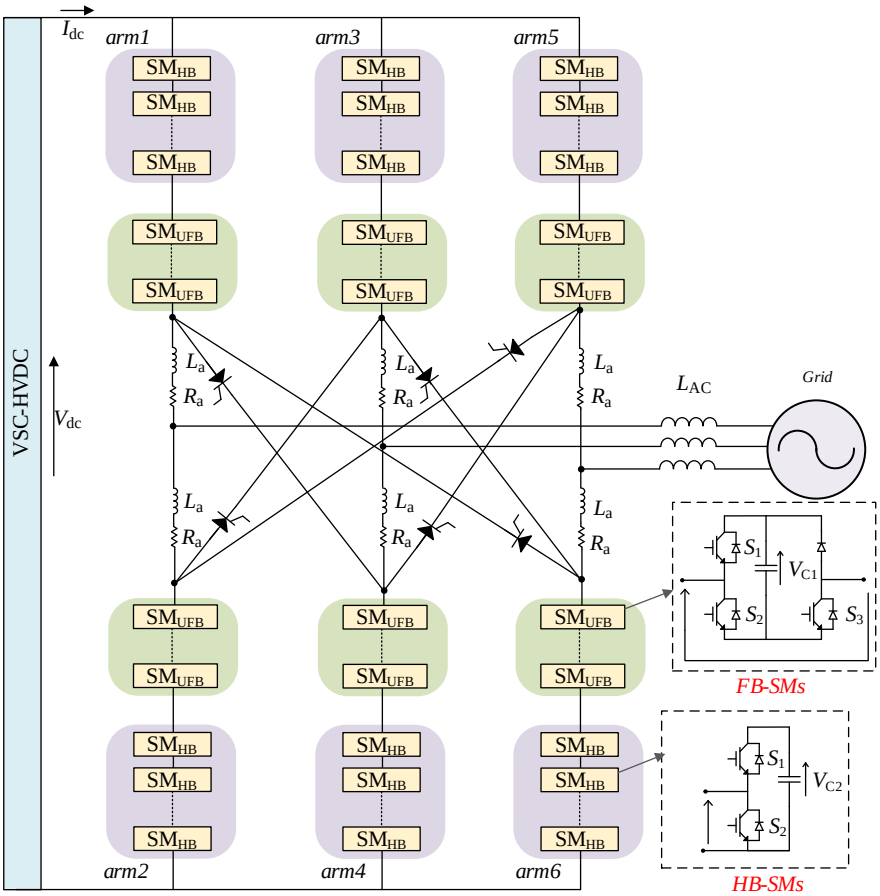


Fig. 2.8. Crossing thyristor branches-based MMC (CTB-MMC) architecture

Other literature adopts the concept of adding thyristors to VSC converters in order to increase their efficiency [34]. For instance, the active forced commutated (AFC) bridge-based converter in [35, 36], consists of antiparallel thyristor valves and a chain of FB-SMs as depicted in Fig. 2.9. In this topology, the thyristors handle the main power path, reducing conduction losses, while the FB-SMs are used for shaping the AC voltage waveform and commutating the thyristor arms. This topology achieves lower conduction losses but introduces a significant drawback: the need for a large filter at the AC link due to high harmonic content.

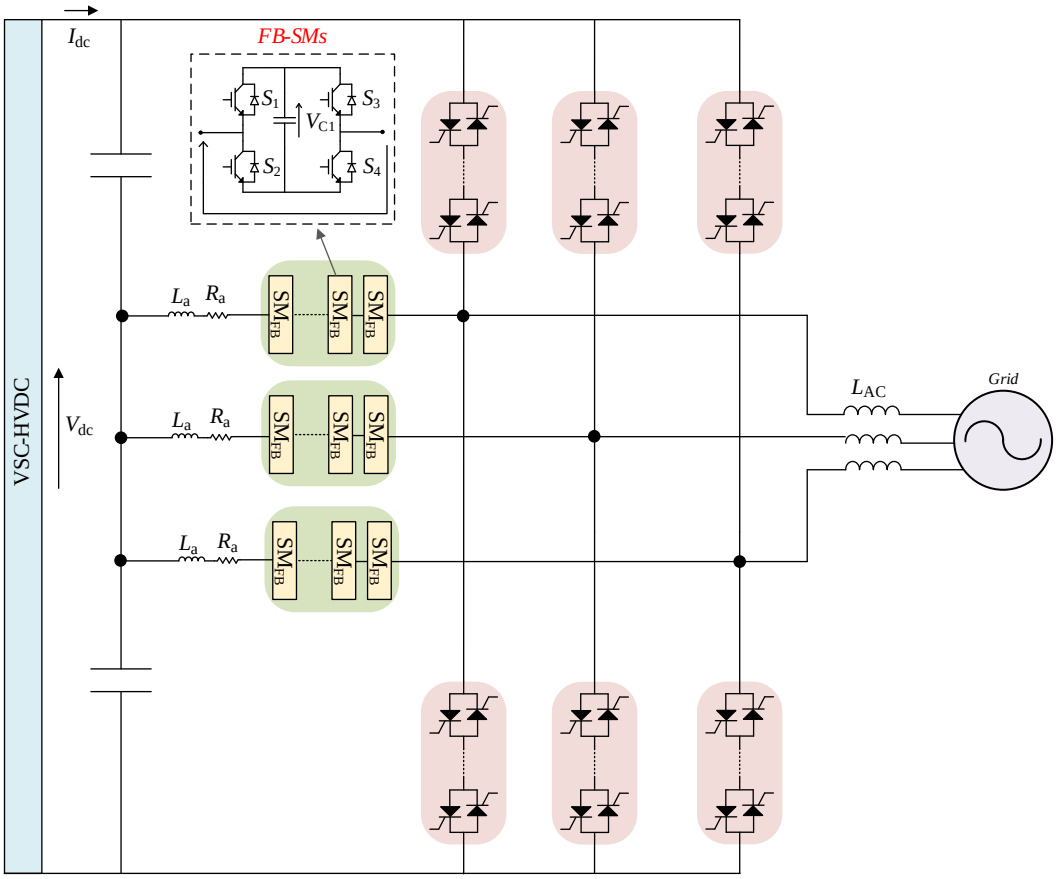


Fig. 2.9. The active forced commutated (AFC) bridge-based converter architecture.

An alternative solution involves the use of power groups (PGs) in place of traditional SMs in the MMC arms [37-39]. These PGs consist of multiple SMs in parallel with bidirectional thyristors. The thyristors bypass the SMs during periods of zero voltage generation, reducing conduction losses. This approach has been applied to both non-DC fault-tolerant converters, such as the HB-MMC, and DC fault-tolerant converters, like the FB-MMC, hybrid-MMC, and EO-AAC. New converter topologies, such as PG-FB-MMC, PG-hybrid-MMC, and augmented trapezoidal alternate arm converter (AT-AAC), have emerged as a result of this design approach. The PG-hybrid-MMC configuration, shown in Fig. 2.10, exemplifies this design. While these topologies reduce conduction losses, they require a large number of semiconductors, which significantly increases the overall converter costs.

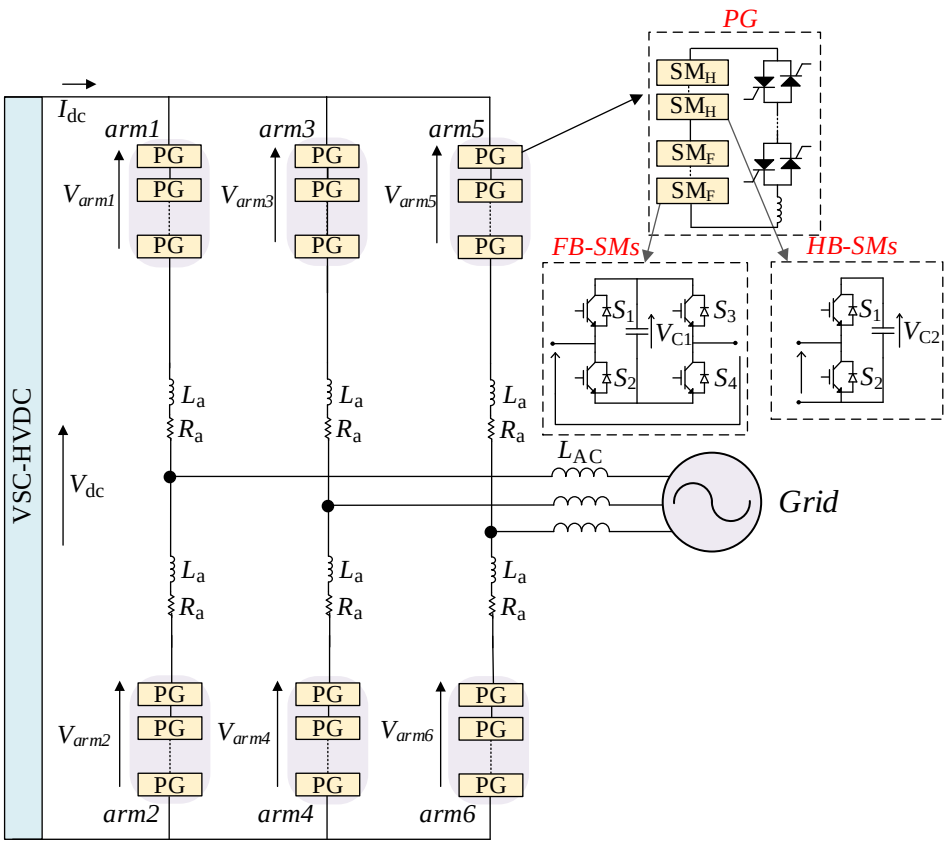


Fig. 2.10. Power group-based hybrid-MMC (PG-hybrid-MMC) architecture.

Another notable design is the modular embedded multilevel converter (MEMC), presented in [40, 41]. This converter utilizes antiparallel thyristor valves alongside SMs in a three-level structure, thereby reducing conduction losses and the storage energy requirements for the SMs. However, to achieve DC fault blocking, FB-SMs are used, which increases the number of semiconductors and the overall cost. Similarly, the hybrid alternate common arm converter (HACC) proposed in [42, 43] uses antiparallel thyristor valves to connect arms in parallel, doubling the converter power capability without doubling the number of semiconductors. Despite this, the converter suffers from discontinuous operation, and the turn-off process of the thyristor valves limits its power capability.

The HVDC converters are summarised in Table 2.1 including a brief description, advantages and disadvantages for each of them, where achieving DC fault-blocking capability in VSC-HVDC converters typically requires a significant number of FB-SMs, which increases both the cost and the losses in the system. Although incorporating thyristor branches in parallel can reduce conduction losses, these approaches introduce greater complexity and cost, further complicating the HVDC system.

Table 2.1: HVDC converters development summary

Topology	Description	Advantages	Disadvantages
HB-MMC	Uses cascaded HB-SMs. Can generate positive, zero voltage.	Modular, scalable, redundant, controllable, higher efficiency than two-level VSCs.	Non-DC fault-tolerant, requires expensive DC circuit breakers for fault management.
FB-MMC	Replaces HB-SMs with FB-SMs. Can generate positive, negative, or zero voltage.	DC fault-blocking capability.	Doubles the number of semiconductors, increasing cost and reducing efficiency.
Hybrid MMC	Combines FB-SMs and HB-SMs in a single converter.	DC fault-blocking with fewer semiconductors than FB-MMC.	Lower efficiency compared to HB-MMC.
AAC	Replaces some FB-SMs with director switches (series-connected IGBTs).	DC fault blocking with fewer semiconductors, smaller and lighter converter.	Lower efficiency than HB-MMC and LCCs, increased complexity.
EO-AAC	Modifies AAC by adding more FB-SMs for smoother current waveforms.	Wider operational range, smoother current waveform.	Requires more FB-SMs, still less efficient than HB-MMC.

Topology	Description	Advantages	Disadvantages
TB-MMC	Integrates thyristors with HB-MMC for DC fault-blocking.	DC fault-blocking capability, similar to LCC-based converters.	Does not utilize the lower thyristor conduction losses during normal operation.
CTB-MMC	Uses unipolar FB-SMs and crossing thyristor branches to manage fault current.	Isolates AC component from DC side during faults.	Does not utilize the lower thyristor conduction losses during normal operation.
AFC Bridge-Based Converter	Combines antiparallel thyristor valves with FB-SMs.	Lower conduction losses, thyristors handle main power path.	Requires large AC filters due to high harmonic content.
PG-Hybrid-MMC	Uses power groups (PGs) with bidirectional thyristors to bypass SMs.	Reduces conduction losses, applicable to both fault-tolerant and non-fault-tolerant converters.	Increases semiconductor count and overall cost.
MEMC	Uses antiparallel thyristor valves with SMs in a three-level structure.	Reduces conduction losses and storage energy requirements.	Requires FB-SMs for DC fault blocking, increasing cost and semiconductor count.
HACC	Uses antiparallel thyristor valves to connect arms in parallel.	Doubles power capability without doubling semiconductors.	Suffers from discontinuous operation, limited power capability due to thyristor turn-off.

2.1.3 Modulation Techniques

Modulation techniques for Modular Multilevel Converters (MMCs) can be categorized into carrier-based PWM techniques and non-carrier-based modulation techniques such as Nearest Level Control (NLC) [44]. Carrier-based PWM techniques include Level-Shifted Carrier PWM (LS-PWM), Phase-Shifted Carrier PWM (PSC-PWM), and Hybrid Carrier PWM, where the number of carriers used is equal to the number of submodules (SMs) per arm [45].

A) Level shifted PWM

In LS-PWM, all carriers have the same frequency and amplitude. The peak-to-peak amplitude of each carrier is $2/N_t$ pu, where N_t is the total number of SMs per arm, and they are displaced with different offsets. Variants of LS-PWM include Phase Disposition (PD), where all carriers have the same phase shift as depicted in Fig. 2.11(a), phase opposition disposition (POD), where negative carriers are 180° out of phase with the positive carriers as shown in Fig. 2.11(b), and alternative phase opposition disposition (APOD), where carriers are alternately 180° out of phase with their adjacent ones as depicted in Fig. 2.11(c).

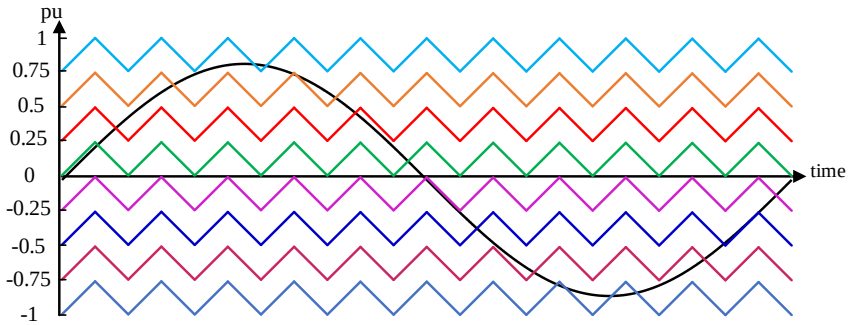
LS-PWM can introduce an imbalance in SM capacitor voltages between the upper and lower arms. If a voltage balancing algorithm is not implemented, rotational assignment of gating signals is used, where the PWM signals are not fixed to specific SMs but rotate among all available SMs.

B) Phase shifted PWM

In PSC-PWM, all carriers have the same frequency and peak to peak amplitude of 2 pu (-1 to 1) but are phase-shifted by $360^o/N_t$ with respect to each other as depicted in Fig. 2.11(d). This modulation technique typically achieves better capacitor voltage balancing compared to LS-PWM.

C) Hybrid carrier PWM

Hybrid carrier-based PWM combines features of LS-PWM and PSC-PWM. The number of MMC levels must be odd (i.e., the number of SMs per arm must be even) to implement this technique. Phase-shift disposition (PSD) is an example of hybrid carrier PWM, where half of the carriers have a peak-to-peak amplitude of 1 pu (from 0 to 1) and are phase-shifted by $(360o/(2N_t))$, while the other half have a peak-to-peak amplitude of 1 pu (from -1 to 0) and are also phase-shifted by $(360o/(2N_t))$ as depicted in Fig. 2.11(e)


pu
1
0.75
0.5
0.25
0
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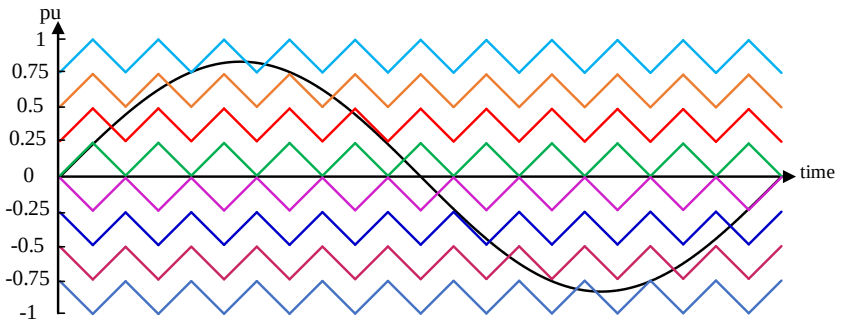
-1
time

(a)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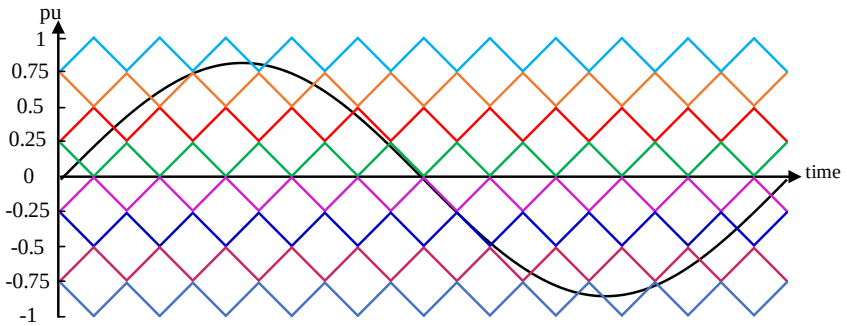
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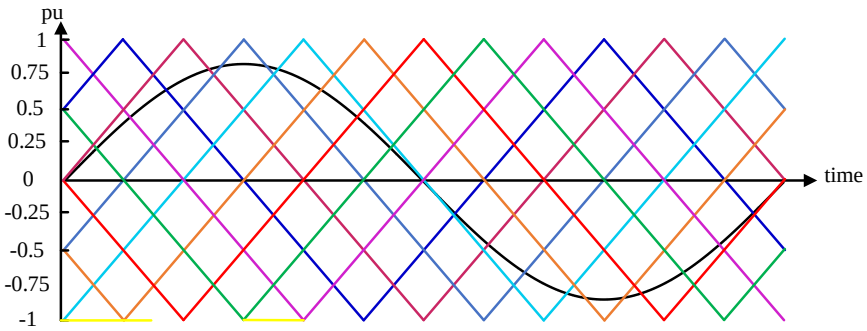
(c)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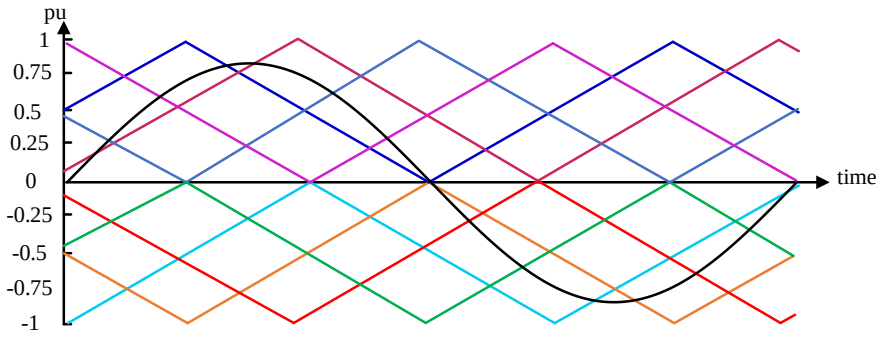
(d)



(e)

Fig. 2.11. Carrier-based PWM techniques.
(a) PD, (b) POD, (c) APOD, and
(d) PSC, (e) PSD.

D) Nearest level control (NLC)

NLC is a low-switching-frequency modulation technique suitable for MMCs with a large number of SMs per arm (typically in the hundreds). The control process, as depicted in Fig. 2.12, involves dividing the arm reference voltage by the nominal capacitor voltage V_{cn} and rounding the result to obtain an integer value for the number of inserted SMs N_{SMs}. A voltage balancing algorithm determines which SMs should be inserted or bypassed, and a pulse generator sends the required gating signals to the IGBTs based on the balancing algorithm.

The voltage balancing algorithm ensures uniform capacitor voltage distribution across SMs and is fed by the measured capacitor voltages, arm current, and the number of required SMs N_{SMs} as depicted in Fig. 2.12. In the HB-MMC voltage balancing algorithm, illustrated in Fig. 2.13, if the arm current is positive, the algorithm sorts the SMs in ascending order and inserts the lowest voltage SMs to charge, whereas if the arm current is negative, the algorithm sorts the SMs in descending order and inserts the highest voltage SMs to discharge.

In the FB-MMC voltage balancing algorithm as depicted in Fig. 2.14, if the required N_{SMs} is positive, the algorithm follows the same steps as in HB-MMC. However, if N_{SMs} is negative, the insertion logic is reversed. If the arm current is positive, the algorithm inserts the highest voltage SMs to discharge, whereas if the arm current is negative, the algorithm inserts the lowest voltage SMs to charge.

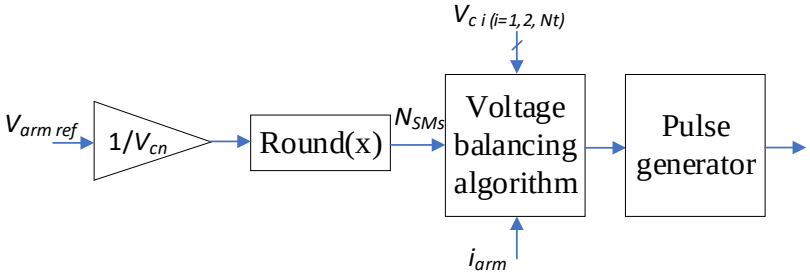


Fig. 2.12. Nearest level control (NLC)

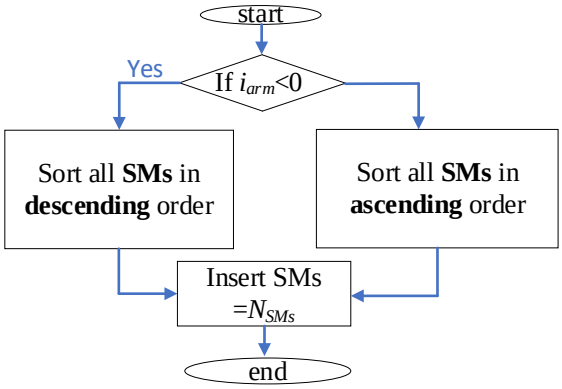


Fig. 2.13. Voltage balancing algorithm for the HB-MMC.

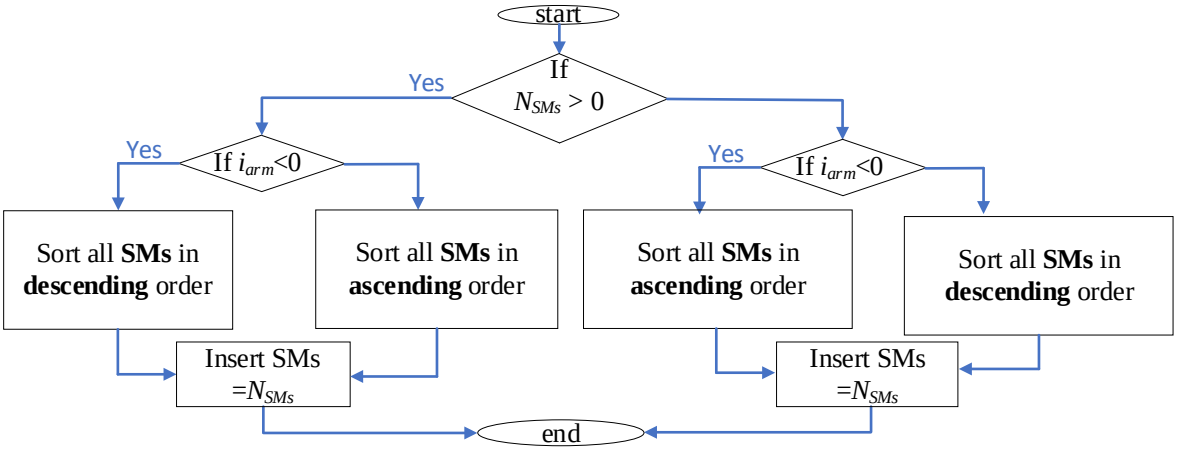


Fig. 2.14. Voltage balancing algorithm for the FB-MMC.

2. 2 DC Collections Development

As mentioned in Chapter 1, DC collection systems can significantly reduce weight and volume by utilizing medium-frequency transformers in DC-DC converters rather than bulky low-frequency transformers. This section explores the development of various DC collection architectures, namely the parallel wind farm (P-WF), series wind farm (S-WF), and series-parallel wind farm (SP-WF) configurations, along with their associated challenges and advancements.

2.2.1 Parallel Wind Farm (S-WF) DC Collection Systems

The simplest DC collection approach is the parallel wind farm (P-WF) architecture. In this configuration, a DC-DC converter at each wind turbine (WT) boosts the voltage from the low-voltage (LV) rectifier terminals to a medium-voltage (MV) level. A second DC-DC converter then steps the voltage up to the high-voltage direct current (HVDC) transmission level as depicted in Fig. 2.15. However, this architecture suffers from higher total losses due to multiple conversion stages compared to AC collection systems.

A variation of this approach was proposed in [40], where the wind turbines within the wind farm are divided into groups. In each group, the turbines are connected in parallel using only uncontrolled rectifiers. Each group has a single DC-DC converter to step up the voltage to the HVDC transmission level. While this topology eliminates the need for intermediate voltage-boosting stages, it incurs higher transmission losses due to direct parallel connections. Moreover, the single-stage voltage step-up from the WT terminal to the HVDC level presents practical implementation challenges.

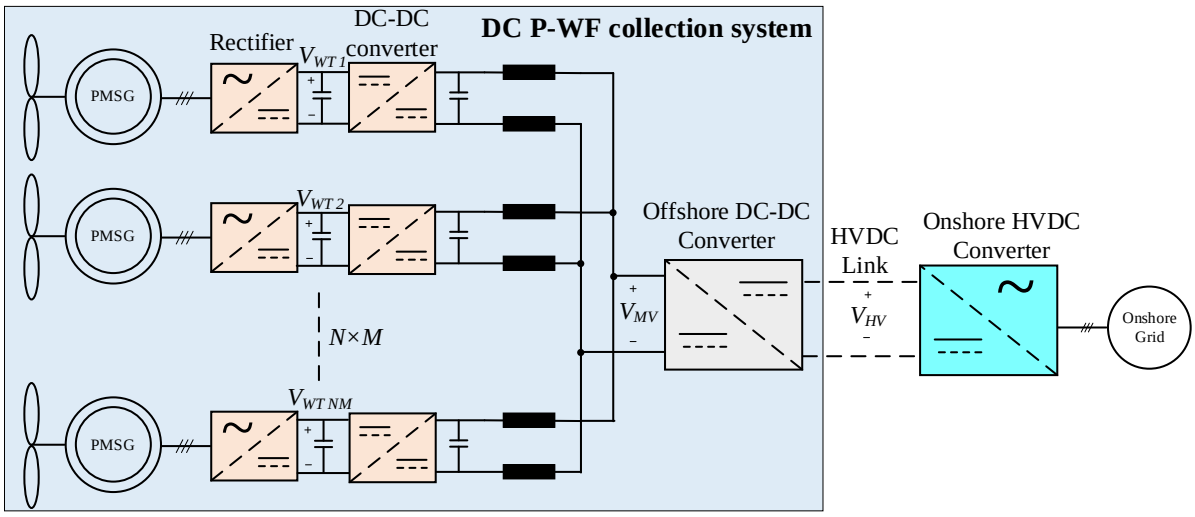


Fig. 2.15. DC parallel wind farm (P-WF) collection architecture.

2.2.2 Series Wind Farm (S-WF) DC Collection Systems

To enhance the efficiency of DC collection systems, the series wind farm (S-WF) architecture is introduced. In this configuration, a large number of WTs are connected in series to directly achieve the HVDC transmission voltage, thereby eliminating the need for a second DC-DC conversion stage [46, 47] as depicted in Fig. 2.16.

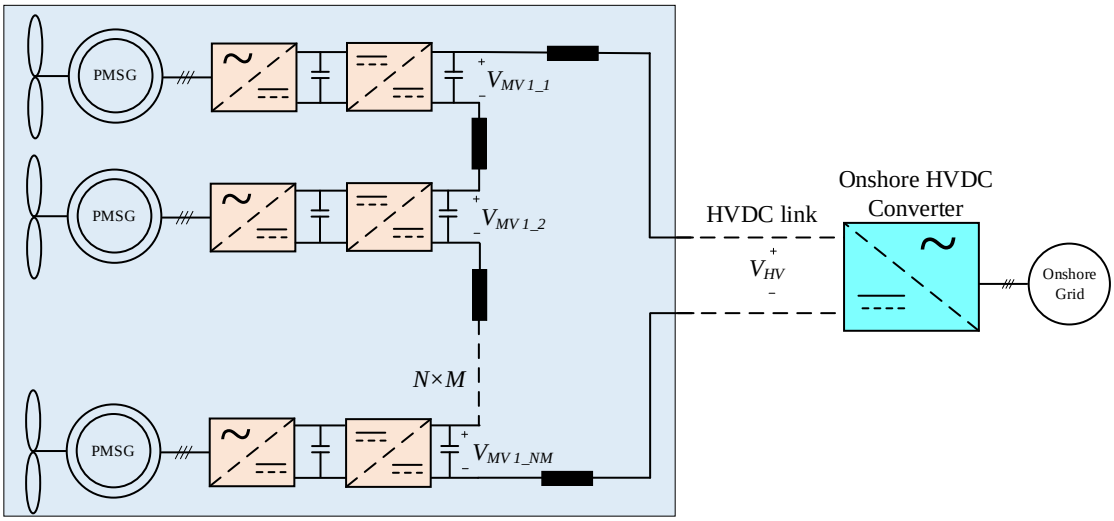


Fig. 2.16. Series wind farm (S-WF) collection architecture.

Several S-WF topologies utilize line-commutated converters (LCCs) onshore to control the HVDC current through the series-connected WTs [48-52]. To enable maximum power point tracking (MPPT) for each WT, various DC-DC converters are employed. For instance, in [49], three-phase uncontrolled rectifiers are followed by a buck converter, which ensures continuous current flow during both on and off states. A depiction of this buck-based converter is shown in Fig. 2.17. However, the utilization of buck converter limits the power and voltage capabilities of the DC-DC converter. Another literature suggests utilizing partial power processing converters (PPPC) with uncontrolled rectifiers [52] to achieve MPPT. This type of DC-DC converter only processes the power differences between the WTs, while the bulk power flows through the uncontrolled rectifiers. The DC-DC converter consists of a three-phase uncontrolled rectifier followed by an input parallel output series (IPOS) connected dual active bridges (DAB) followed by unfolder switches as depicted in Fig. 2.18. The unfolder switches are realized using contactors to reduce the losses and cost while increasing reliability. The unfolder switches are mainly used to provide positive or negative voltages at the HVDC link side hence enabling bidirectional power capability.

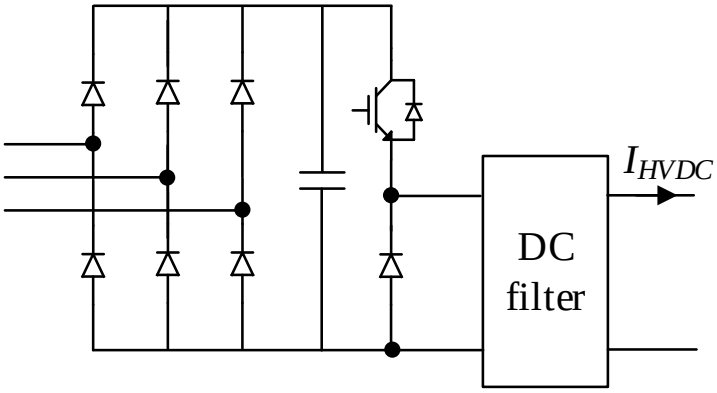


Fig. 2.17. Buck-based DC-DC converter used for each wind turbine [49].

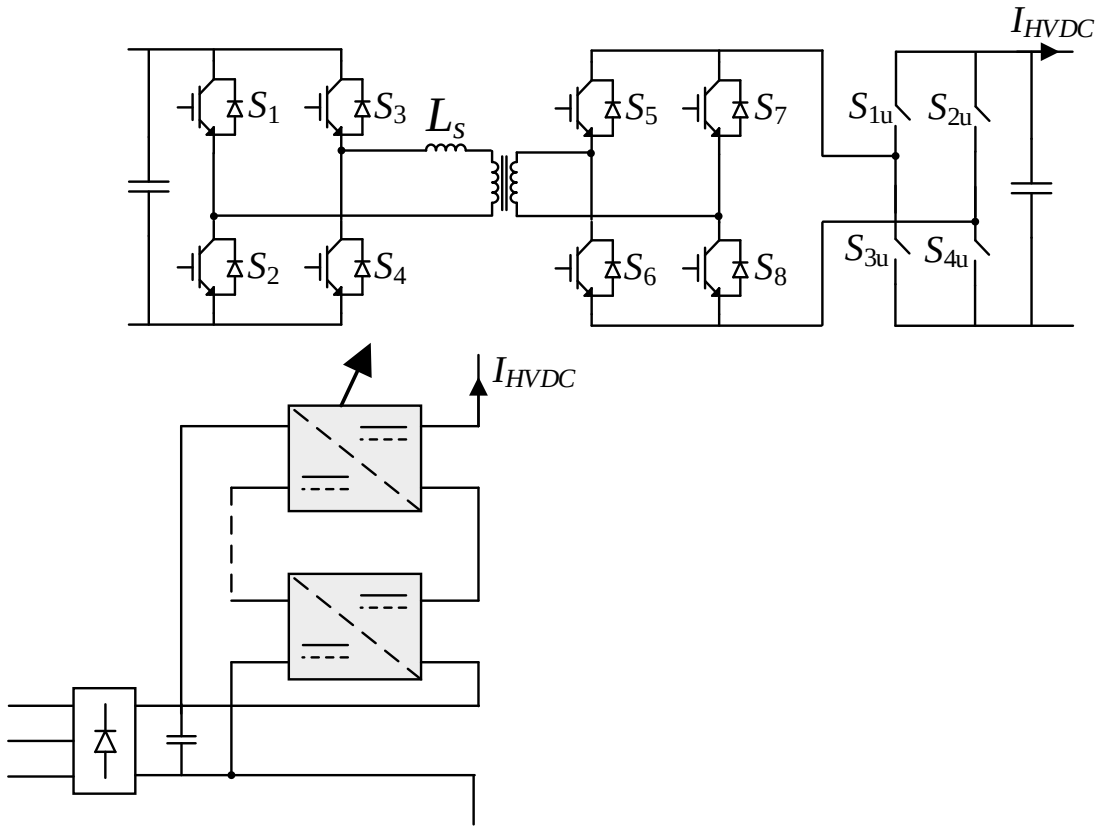


Fig. 2.18. PPPC-based DC-DC converter used for each wind turbine [52].

Nevertheless, since these architectures are based on LCC-based HVDC systems, they face challenges such as commutation failures and substantial reactive power compensation requirements on the onshore side. Additionally, achieving galvanic isolation necessitates low-frequency transformers at WT terminals, increasing the system offshore weight and volume.

On the other hand, some S-WF architectures employ voltage source converters (VSCs) instead of LCCs on shore [46, 53-57]. For example, the authors in [53] have used a half-bridge modular multilevel converter (HB-MMC) onshore to control the HVDC current. Also, to achieve MPPT for each WT, this method utilises a neutral point clamped (NPC) converter followed by two bypass switches and an auxiliary diode. A schematic of this NPC-based converter is shown in Fig. 2.19. During normal operation, the auxiliary diodes are not used and remain reversely biased by the output voltage of the NPC. Also, a parallel switch with a resistor is included to prevent any overvoltage in the DC output of the converter.

Although VSC-based S-WF systems eliminate the commutation-related issues, they often require power curtailment at the WT level to prevent overvoltage in the series-connected string. Additionally, configurations employing full-bridge MMCs (FB-MMCs) [56] provide a broader DC voltage control range but incur higher costs due to the extensive use of FB-SMs. Moreover, a low-frequency transformer is used at the WT terminals to achieve galvanic insulation which increases the footprint and weight of the system. These configurations also face reliability issues, as any open or short-circuit fault in the series string can lead to complete system shutdown unless additional components such as diode rectifiers, disconnectors, and bypass switches are employed for each group of WTs to isolate the faulted area [58, 59].

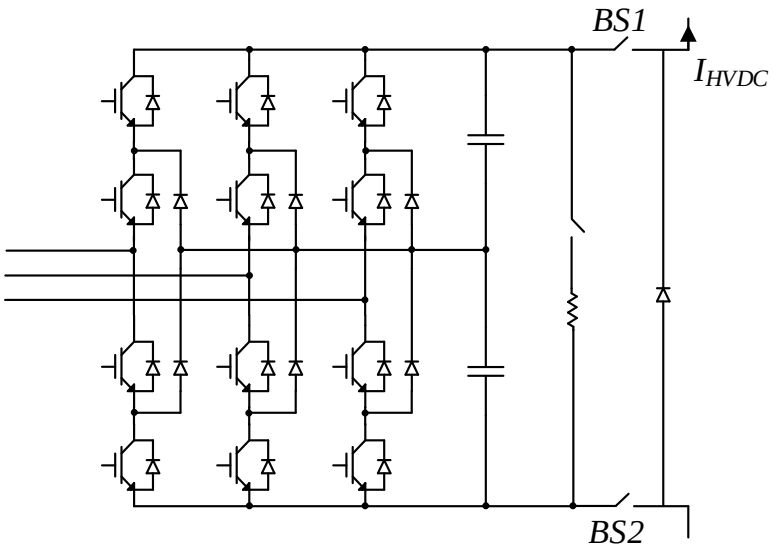


Fig. 2.19. NPC-based DC-DC converter used for each wind turbine [53].

2.2.3 Series-Parallel Wind Farm (SP-WF) DC Collection Systems

To address the challenges of P-WF and S-WF configurations, the series-parallel wind farm (SP-WF) architecture was introduced as a compromise [60]. In this design, wind turbine groups (WTGs) are connected in parallel, with each WTG consisting of a series-connected string of WTs. A DC-DC converter with voltage-boosting capability is used to achieve MPPT and step up the voltage for each WT, allowing the smaller number of series-connected WTs per WTG to reach the HVDC transmission level, as shown in Fig. 2.20. Furthermore, VSC-based HVDC system such as MMC is used onshore to control the DC voltage [61]. Each WT in this architecture employs a controlled rectifier followed by a two-stage isolated DC-DC converter, as depicted in Fig. 2.21. These converters enable MPPT and step up the DC voltage to medium voltage levels for efficient transmission [62].

Nevertheless, this architecture suffers from wind curtailment due to variations in wind speeds between WTGs to limit the overvoltage [63, 64]. Besides, the insulation of the first and the last WTs in each series-connected WTG must endure half of the full HVDC link voltage, creating operational challenges. Furthermore, a DC fault in any WTG could lead to a complete system failure unless expensive DC breakers are installed to isolate the faulted WTG.

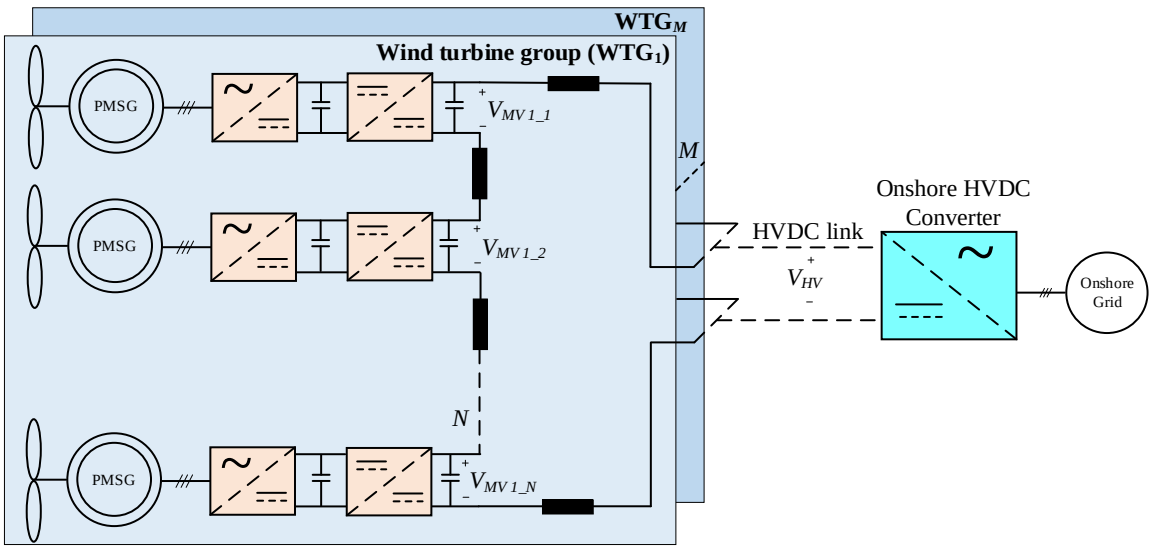


Fig. 2.20. Series-parallel wind farm (SP-WF) collection architecture.

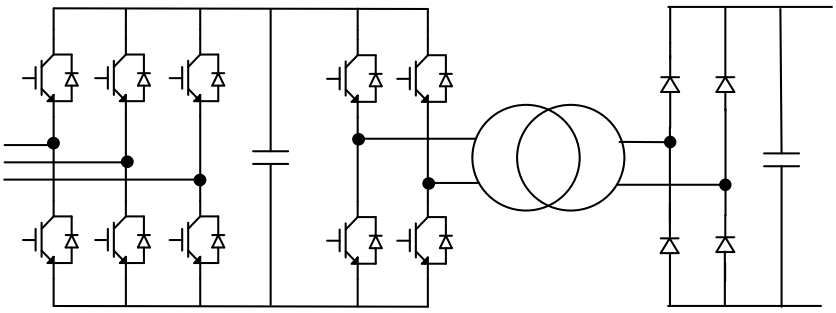


Fig. 2.21. Controlled rectifier followed by two-stage isolated DC-DC converter [61].

DC collection systems for offshore wind farms reduce transformer weight and volume by using medium-frequency transformers in DC-DC converters. Three main architectures are explored: parallel wind farms (P-WF), series wind farms (S-WF), and series-parallel wind farms (SP-WF). Among these three DC collection architectures, the P-WF offers the highest reliability and DC fault-tolerance capabilities but suffers from higher losses due to multiple conversion stages. The S-WF configuration eliminates additional conversion stages, resulting in higher efficiency, but faces challenges related to reliability issues, and fault tolerance. The SP-WF, as a hybrid design, mitigates some of these issues but suffers from wind curtailments and the reliability is still lower than that of the P-WF. Some specifications for the offshore DC collection architectures reported in literature are summarized in Table 2.2

Table 2.2: offshore DC collection architecture specifications.

Topology	Turbine ratings		HVDC link ratings	
	Voltage (kV)	Power (MVA)	Voltage (kV)	Power (MVA)
DC parallel [15]	1.2/30	5	±150	400
DC series [47]	1	2	150	346
	5	10	150	346
DC series [52]	5.8	5	150	150
DC series[56]	5	10	320	640
DC series-parallel [60]	7/11.67	10	70	120
DC series-parallel [61]	32	5	±320	300

Chapter 3

New Hybrid Thyristor-based Multilevel Converter (HTMC) for HVDC Applications with DC Fault Capability

From the discussion in Chapter 2, the main issue with the existing converters in HVDC applications is the large number of FB-SMs to achieve DC fault-blocking capability, which increases the total number of semiconductors. In this Chapter, a new hybrid thyristor-based multilevel converter (HTMC) is proposed for HVDC applications. The proposed converter utilises antiparallel thyristors, HB-SMs, and a limited number of FB-SMs. Normally, thyristors are favoured over IGBTs due to their high overcurrent capability, lower cost, lower losses, and availability at higher voltage and current ratings. These claims are validated using a MATLAB SIMULINK model and experimental results. An extensive comparison is performed using typical parameters to highlight the advantages of the proposed converter over those in the literature, in terms of semiconductor count, passive elements, current stresses, losses, cost, fault-clearing time, weight, and size.

3. 1 Proposed Topology Description

3.1.1 Proposed Converter Architecture

The proposed 3-phase HTMC has 6 arms as shown in Fig. 3.1 where each arm consists of a thyristor valve (series connection of antiparallel thyristors) and an MMC stack which is comprised of HB-SMs, and a limited number of FB-SMs. Each arm element type has a specific role during converter operation. The HB-SMs are responsible for creating the output sinusoidal AC voltage waveform. The FB-SMs create an overlap period between the lower and upper arms (where both the thyristor valves in the same leg are conducting) to retain the balance between SM capacitors. In addition, the FB-SMs are responsible for thyristor commutation in normal operation and DC fault cases (FB-SMs use their positive voltage state during normal operation commutation while their negative voltage state is used for commutation during faults). The thyristor valve is used to decrease the conduction losses in normal operation and block the fault current during fault scenarios. Both thyristor valves and HB-SMs in each arm are designed to endure $½V_{dc}$, while FB-SMs per arm are designed to generate $\pm\,\Delta V$ (to allow for the overlap and commutation times). Thus, the whole MMC stack should be able to generate from $-\Delta V$ to $½V_{dc} + \Delta V$. Note the SMs have protection

bypass thyristors as shown in Fig. 3.1 to bypass the AC component of the DC fault current until it is blocked by the thyristor valve.

3.1.2 Proposed Converter Operation and Analysis (with Third Harmonic Subtraction)

Overlap and commutation periods are essential during the operation of the proposed converter due to the utilisation of thyristors. The overlap period is important to rebalance the energy between the upper and lower SM capacitors while the commutation period is required to turn off the thyristor valves at the end of their conduction period. However, without third harmonic subtraction (only sinusoidal fundamental AC waveform) to allow even a small overlap or commutation time, a large number of FB-SMs is required, which increases the converter cost, and losses. Therefore, a third harmonic waveform is subtracted from the sinusoidal fundamental AC waveform so that the resultant waveform is characterised by a low voltage change near zero as shown in Fig. 3.2 (first drawing, in red) compared to the fundamental waveform (in green), hence a low number of FB-SMs is required. Therefore, subtracting a third harmonic waveform permits an increase in an arm overlap period and allows a longer time for force commutation of the thyristor valve while using fewer FB-SMs.

In addition, the FB-SMs can produce its negative state voltage to increase the overall phase peak voltage ($\hat{v}_a$) to $½V_{dc} + \Delta V$ as shown in Fig. 3.2. Therefore, the fundamental phase peak voltage ($\hat{v}_{a_1}$) remains at $½V_{dc}$. Hence, the fundamental phase voltage v_{a_1} is as follows:

$$v_{a_1}(t) = \hat{v}_{a_1} \sin \omega t = ½V_{dc} \sin \omega t \tag{3.1}$$

The injected third harmonic voltage (v_{a_3}) is:

$$v_{a_3}(t) = \Delta V \sin 3\omega t = k_3 \hat{v}_{a_1} \sin\ 3\omega t \tag{3.2}$$

where k_3 is the third harmonic voltage ratio. The resultant phase voltage $v_a(t)$ is:

$$v_a(t) = ½V_{dc}(\sin \omega t - k_3 \sin 3\omega t) \tag{3.3}$$

Since the MMC stack and thyristor valve are series connected and sharing the DC link voltage, the arm 1 voltage is:

$$v_{arm_1}(t) = v_{stack_1}(t) + v_{valve_1}(t) \tag{3.4}$$

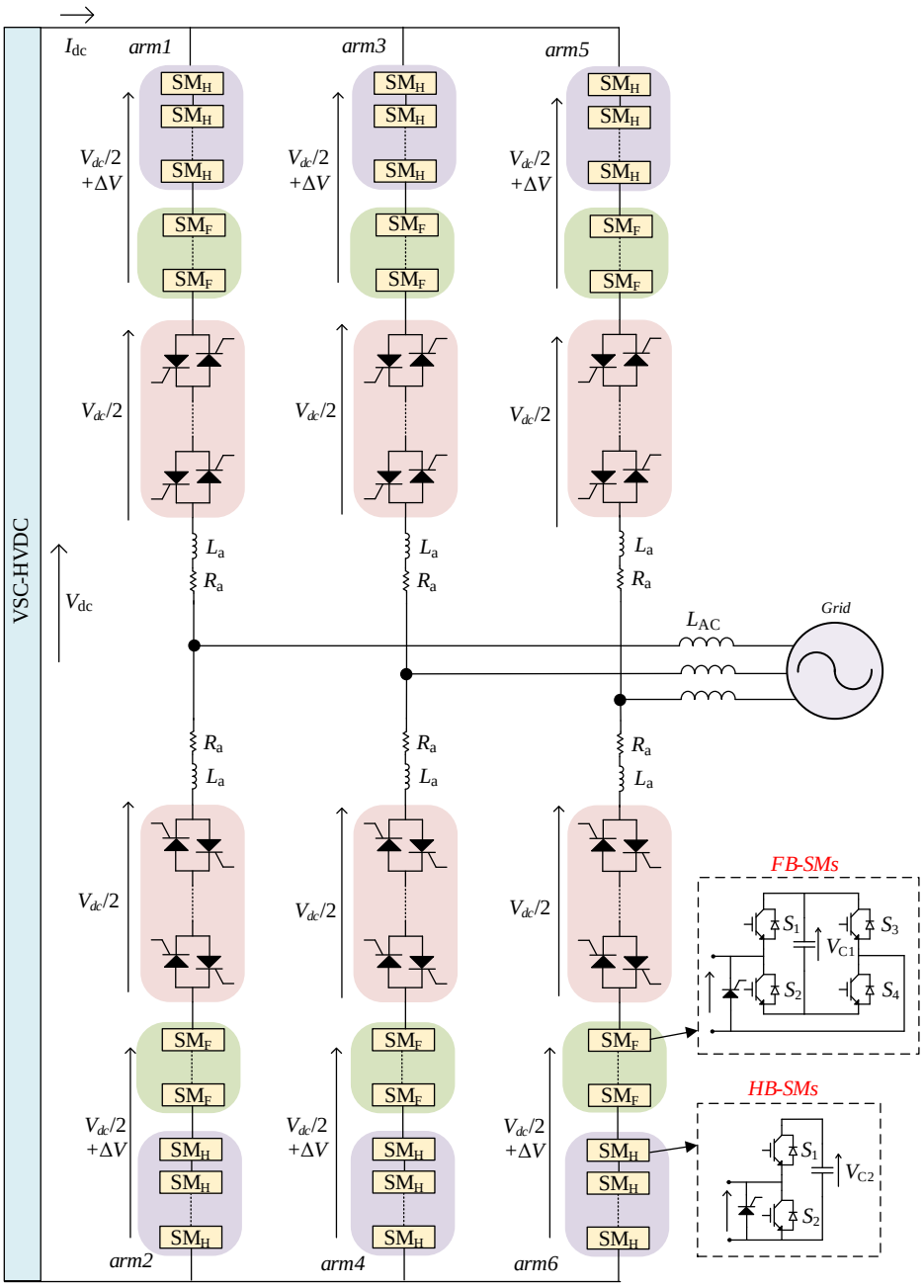


Fig. 3.1. Proposed converter architecture.

In order to provide the required phase voltage, force commutating the thyristor valve, and to maintain the maximum thyristor valve voltage at $½V_{dc}$, the MMC stack 1 voltage is given as (3.5), while MMC stack 2 voltage is given by (3.6).

$$v_{stack_1}(t) = \begin{cases} ½V_{dc} - v_a(t), & -T_{ov} < t < ½T_p \\ ½V_{dc} \text{ or } ½V_{dc} + \Delta V, & ½T_p < t < ½T_p + T_c \\ ½V_{dc} + \Delta V, & ½T_p + T_c < t < T_p - T_{ov} \end{cases} \quad (3.5)$$

$$v_{stack_2}(t) = \begin{cases} ½V_{dc} \; or \; ½V_{dc} + \Delta V, & 0 < t < T_c \\ ½V_{dc} + \Delta V, & T_c < t < ½T_p - T_{ov} \\ ½V_{dc} + v_a(t), & ½T_p - T_{ov} < t < T_p \end{cases} \quad (3.6)$$

where T_c is the overall commutation time which includes the circuit commutation turn off time of the thyristor t_q and the falling time of the current T_f. T_{ov} is the overlap time and T_p is the periodic time. The 2nd part of the v_{stack_1} equation is equal to $½V_{dc} + \Delta V$ in the case of positive arm current at the instant of commutation so that the MMC stack can provide force voltage commutation to the thyristor valve before continuing with the next part of the waveform. But in case of negative arm current, it is equal to $½V_{dc}$ so that a positive voltage can be applied to the thyristor valve for force commutation. The same applies for the first part of v_{stack_2}.

To understand the operation of the proposed converter, phase 'a' voltage waveforms in addition to MMC stacks and thyristor valves of arms 1 and 2 voltage and current waveforms are depicted in Fig. 3.2, where the dashed currents are for positive power flow while the solid currents are for negative power flow. For clarity, the dashed parts of the voltage waveforms of the MMC stack and thyristor valve correspond to the dashed arm currents. Fig. 3.2 is divided into 6 sections, 3 sections for each half cycle. Sections *a* - *c* are for the positive half cycle and are explained in the parts of Fig. 3.3, while sections *a'* - *c'* are for the negative half cycle and are explained in Fig. 3.4.

The converter operation in each section of the positive cycle are as follows:

Section *a*: MMC stack 2 provides force commutation to thyristor valve 2 by generating $½V_{dc} + \Delta V$ for positive arm current at the commutation instant (solid currents in Fig. 3.2 or by generating $½V_{dc}$ for negative arm current at the commutation instant (dashed currents in Fig. 3.2). Thyristor valve 1 is still conducting while MMC stack 1 is building the output phase voltage, so to be unaffected by commutation action.

Section *b*: Thyristor valve 1 is conducting. MMC stack 1 is building the output phase voltage while MMC stack 2 is maintained at $½V_{dc} + \Delta V$ to keep the maximum voltage on thyristor valve 2 at $½V_{dc}$.

Section *c*: Both thyristor valves are conducting (overlap period). MMC stack 1 continues to build the output phase voltage while MMC stack 2 produces the complementary voltage to maintain the leg voltage at V_{dc}. In this period, circulating current flows in both arms to balance the upper and lower SM capacitor voltages.

The converter operation in each section of the negative cycle are as follows:

Section *a'*: MMC stack 1 provides force commutation to thyristor valve 1, the same as with MMC stack 2 in section *a'*. Thyristor valve 2 is conducting while MMC stack 2 is building the output phase voltage so as not to be affected by commutation action.

Section *b'*: Thyristor valve 2 is conducting. MMC stack 2 is building the output phase voltage while MMC stack 1 is maintained at $½V_{dc} + \Delta V$ to keep the maximum voltage on thyristor valve 1 at $½V_{dc}$.

Section *c'*: Both thyristor valves are conducting (overlap period). MMC stack 2 continues to build the output phase voltage while MMC stack 1 produces the complementary voltage to keep the leg voltage at V_{dc}. Like section *c'*, circulating current flows in both arms to balance voltages on the upper and lower SM capacitors.

The same procedures are applied for the other phases but with phase shifts of -120° and 120° to the second and third phases, respectively.

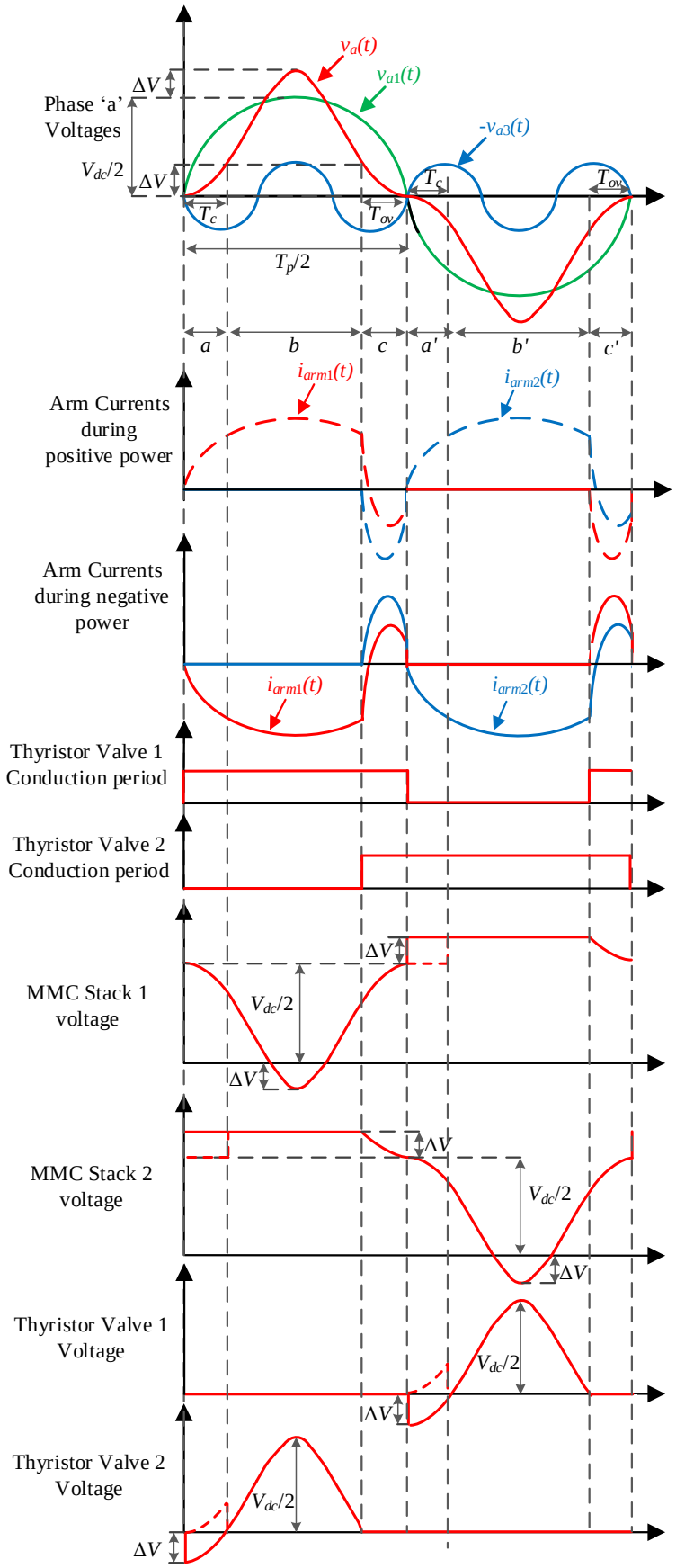


Fig. 3.2. Phase 'a' voltage waveforms and related voltage and current waveforms of the MMC stack and thyristor valve of arms 1 and 2.

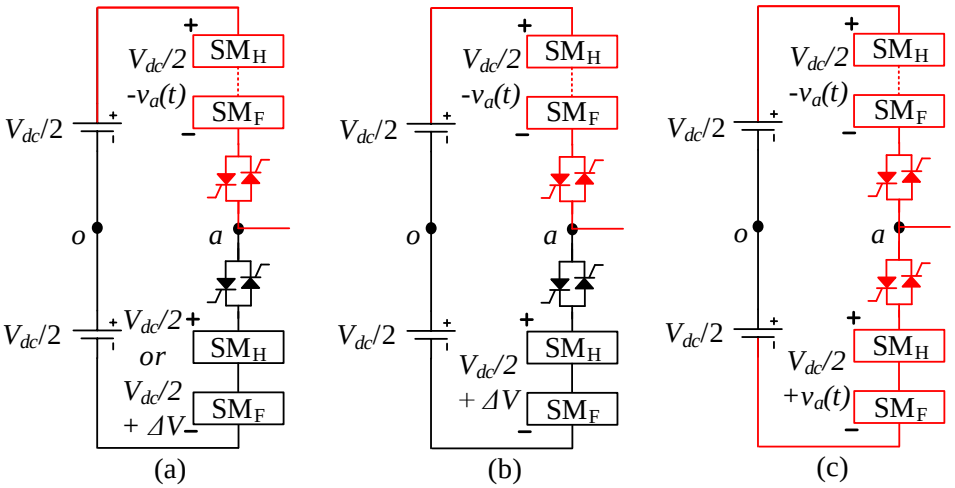


Fig. 3.3. Operation analysis diagrams of phase 'a' (positive half cycle): (a) thyristor valve 2 commutation, (b) arm 1 conduction, (c) overlap period, (d) thyristor valve 1 commutation, (e) arm 2 conduction, and (f) overlap period.

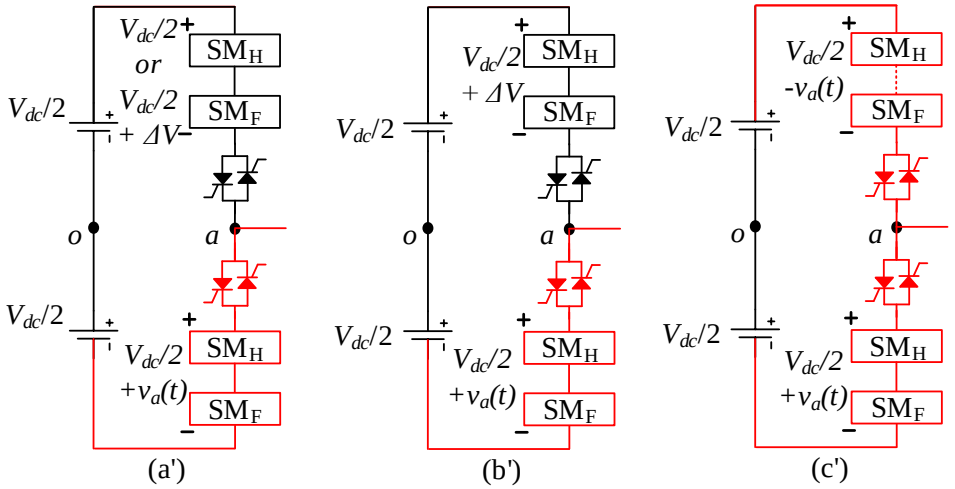


Fig. 3.4. Operation analysis diagrams of phase 'a' (negative half cycle): (a') thyristor valve 1 commutation, (b') arm 2 conduction, and (c') overlap period.

3.1.3 Proposed Topology Controller

The overall block diagram of the proposed topology controller is shown in Fig. 3.5. The control process begins by setting the reference values for active and reactive power (P^*, Q^*), which are used to generate the reference dq components of the AC currents (i_d^*, i_q^*) through PI controllers. Another set of PI controllers then computes the dq components of the fundamental AC voltage of the converter. These components are transformed into time-domain voltages using a dq/abc transformation, as illustrated in Fig. 3.5.

The stack voltage is calculated by substituting the overall obtained AC voltage, including third harmonic subtraction calculated from (3.2), into (3.5) and (3.6) to determine

the upper and lower stack voltages. The voltages for the other phases are obtained by shifting the waveforms by -120^o and 120^o. Once the stack voltage is determined, the number of inserted SMs is computed using the nearest level control (NLC) method by dividing the stack voltage by the nominal capacitor voltage V_{cn} and rounding the result to obtain an integer value. A balancing algorithm then selects which SMs should be turned on or off to maintain capacitor voltage balance. Finally, a pulse generator produces the necessary gating signals for the MMC stack IGBTs.

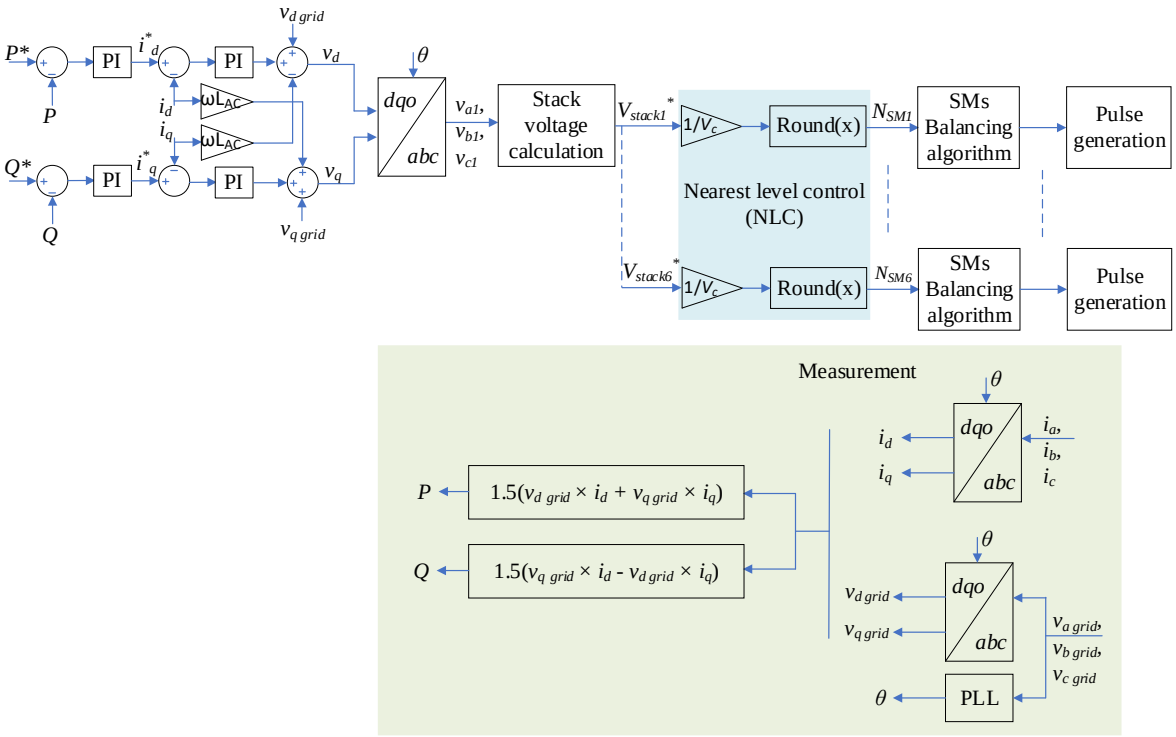


Fig. 3.5. The proposed topology control diagram

3.1.4 DC-Fault Blocking Analysis

The DC-fault current from the converter perspective can be divided into two components, namely the DC component due to the SMs capacitors discharge and the AC component due to the AC grid feeding the DC fault through the converter arms. The proposed converter can quickly interrupt the DC component (using the FB-SMs). On the other hand, the AC component is mainly terminated inherently by the thyristor valve. For a clearer illustration, an example is studied as shown in Fig. 3.6, where it is assumed that phase ‘a’ has a positive voltage (maximum magnitude), while phase ‘b’ and phase ‘c’ have negative voltages. In addition, phase ‘b’ is assumed to have the lowest voltage magnitude, near zero, hence in the overlap state. Fig. 3.6(a) shows the fault occurrence instance, before fault detection, where the blue line indicates the DC component of the fault current (in phase ‘b’

due to the overlap state), while the yellow and the red lines indicate the AC components of the DC fault. Fig. 3.6(b) shows the instant of fault detection, where the DC fault blocking procedures are initiated, all the SMs are blocked, where the FB-SMs inject their negative voltage to quickly block the DC component of the DC fault current. All antiparallel thyristor valve gate pulses are prohibited. Also, the conducting SMs protection thyristors are fired to conduct the AC components of the DC fault current until it is extinguished. Fig. 3.6(c) shows the instant where the DC component of the DC fault current is blocked. Note that if the AC component still exists in phase 'b' then it would flow in the protection thyristors in the lower arm of phase 'b' until the fault current is interrupted. Finally, Fig. 3.6(d) shows the instant where the fault current is completely terminated by the thyristor valve, where all the SMs are bypassed and the AC voltages are endured by the thyristor valve.

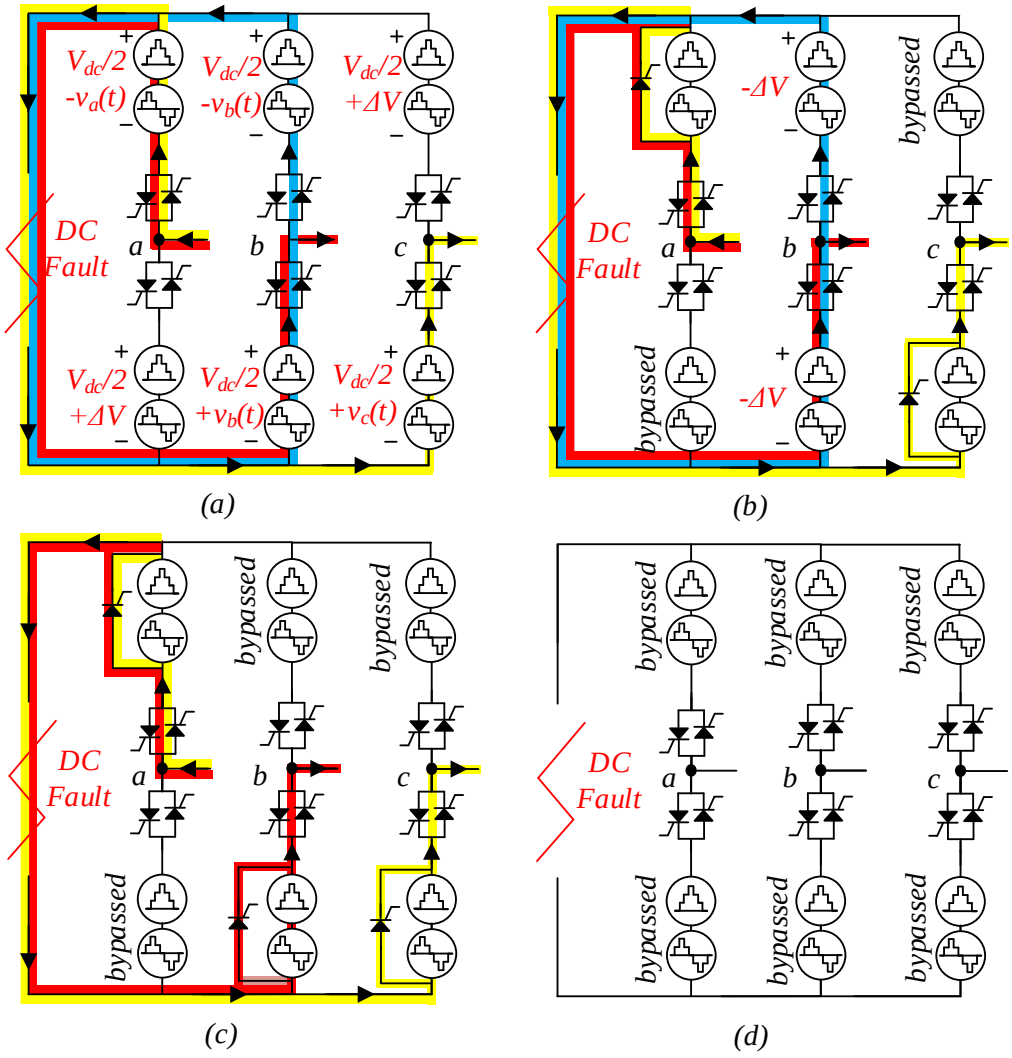


Fig. 3.6. Fault blocking operation diagram: (a) DC fault occurrence, (b) DC fault detection instant, where all fault blocking procedures are initiated, (c) DC component of the fault is interrupted, and (d) DC fault is completely eliminated.

3. 2 System Design

3.2.1 Third Harmonic Ratio and SMs/Thyristors Count

In order to determine the third harmonic ratio (k_3), the minimum overall commutation time (T_c) must be calculated. The overall commutation time (T_c) of the thyristor valves should be more than the fall time of the thyristor peak current (T_f) plus the thyristor circuit-commutation turn off time (t_q), where $T_c \geq T_f + t_q$. In the analysis, it is assumed that overall commutation time (T_c) is equal to the overlap time (T_{ov}). Since the FB-SMs are responsible for creating commutation periods, the phase voltage in (3.3) at T_c should be equal to ΔV (as depicted in Fig. 3.2 so that the MMC stack can apply negative voltage across the thyristor valve during the commutation period, as follows:

$$\frac{V_{dc}}{2}(\sin(\omega T_c) - k_3 \sin(3\omega T_c)) = \Delta V = k_3 \frac{V_{dc}}{2} \tag{3.7}$$

Hence, the relation between k_3 and T_c can be deduced as:

$$k_3 \geq \frac{\sin \omega T_c}{1 + \sin 3\omega T_c} \tag{3.8}$$

To show the effect of the third harmonic subtraction on the required ΔV (FB-SMs voltage), Fig. 3.7 shows the per unit value of the FB-SMs voltage ($\Delta V_{pu} = \Delta V / ½V_{dc}$) with and without third harmonic subtraction, where $\Delta V_{pu} = k_3$ in the third harmonic subtraction case. The required FB-SMs voltage is decreased dramatically with third harmonic subtraction, especially for $T_c > 1$ ms. The number of FB-SMs can be determined as:

$$n_{FB} = \frac{\hat{v}_{a_3}}{V_{c_n}} = \frac{k_3 V_{dc}}{2V_{c_n}} \tag{3.9}$$

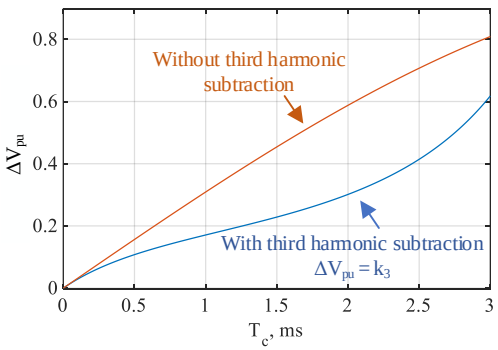


Fig. 3.7. The per unit value of the FB-SMs voltages with and without third harmonic subtraction.

where V_{c_n} is the SM capacitor nominal voltage. On the other hand, the number of HB-SMs, n_{HB}, should be based on the fundamental waveform peak voltage ($\hat{v}_{a_1}$):

$$n_{HB} = \frac{\hat{v}_{a_1}}{V_{c_n}} = \frac{V_{dc}}{2V_{c_n}} \tag{3.10}$$

For the thyristor valve, their maximum voltage is kept at $½V_{dc}$, as mentioned previously. Therefore the number of thyristors in each valve is:

$$N_{thy} = \frac{\hat{v}_{valve}}{V_{thy}} = \frac{V_{dc}}{2V_{thy_n}} \tag{3.11}$$

where V_{thy_n} is the nominal voltage of each thyristor. The number of thyristors can be equal to that of the HB-SMs if both have the same rated voltage.

3.2.2 Arm Inductance, L_a

The arm inductance (L_a) is selected such that during thyristor valve commutation, the falling time of the thyristor current from its peak value is equal to or less than the desired value T_f. Also, the arm inductance should limit the rate of the change of the thyristor current (di/dt) to less the maximum permitted turn-on current ramp rate of the thyristor, σ. Assuming a positive arm current during the instant of commutation of thyristor valve 2, MMC stack 2 generates its peak voltage of $(1 + k_3)½V_{dc}$, while MMC stack 1 builds the AC waveform. Both thyristor valves are conducting before the commutation process occurs. Therefore, with two arm inductances in each leg, the voltage applied on each arm inductance (v_L) is:

$$v_L(t) = ½(V_{dc} - v_{arm_1} - v_{arm_2}) = ½(V_{dc} - v_{stack_1} - v_{stack_2}) \tag{3.12}$$

Substituting the MMC stack voltages results in:

$$v_L(t) = ¼V_{dc}\big(\sin\omega t - k_3(1 + \sin 3\omega t)\big) = \frac{L_a\, di_{arm}}{dt} \tag{3.13}$$

Therefore, the rate of change of the arm currents is given by:

$$\frac{di_{arm}}{dt} = \frac{V_{dc}}{4L_a}\big(\sin\omega t - k_3(1 + \sin 3\omega t)\big) \tag{3.14}$$

By solving this differential equation, the arm current is:

$$i_{arm}(t) = -\frac{V_{dc}}{12\omega L_a}(k_3(3\omega t - \cos 3\omega t) + 3\cos \omega t) + c \quad (3.15)$$

Assuming that at the time of commutation ($t = 0$), the arm current equals the peak phase current ($\hat{\imath}_a$), which is the worst-case scenario, then the constant c is calculated as follows:

$$i_{arm}(0) = \hat{\imath}_a = -\frac{V_{dc}}{12\omega L_a}(3 - k_3) + c \quad (3.16)$$

$$c = \hat{\imath}_a + \frac{V_{dc}}{12\omega L_a}(3 - k_3) \quad (3.17)$$

Therefore the arm current formula during commutation is:

$$i_{arm}(t) = \hat{\imath}_a - \frac{V_{dc}}{12\omega L_a}\left(k_3(3\omega t - \cos(3\omega t) + 1) + 3(\cos(\omega t) - 1)\right) \quad (3.18)$$

It is desired that at $t = T_f$, the arm current be zero, therefore:

$$i_{arm}(T_f) = 0 = \hat{\imath}_a - \frac{V_{dc}}{12\omega L_a}\left(k_3\left(3\omega T_f - \cos(3\omega T_f) + 1\right) + 3\left(\cos(\omega T_f) - 1\right)\right) \quad (3.19)$$

Hence the arm inductance (L_a) can be calculated as (3.20).

$$L_a \leq \frac{V_{dc}}{12\omega \hat{\imath}_a}\left(k_3\left(3\omega T_f - \cos(3\omega T_f) + 1\right) + 3\left(\cos(\omega T_f) - 1\right)\right) \quad (3.20)$$

Also, the inductance should consider that the maximum permitted thyristor turn-on current ramp rate σ is not exceeded. The maximum current rate of change occurs at the instant of thyristor valve commutation. Therefore, the following equation should be satisfied, which is derived by substituting t=0 in (3.14).

$$L_a > k_3 \frac{V_{dc}}{4\sigma} \quad (3.21)$$

It is worth noting that the arm inductance is selected near the maximum value calculated from (3.20) to limit the circulating currents during overlap periods.

3.2.3 Capacitance in HB-SMs and FB-SMs

In this section, the capacitances of both HB-SMs and FB-SMs are calculated, where for an accurate evaluation of their capacitance, the conduction period of the MMC stack is

divided into two portions. The first portion occurs when the MMC stack generates a positive voltage where the energy deviation in the MMC stack is shared among all the SMs ($n_t = n_{HB} + n_{FB}$). The second portion occurs when the MMC stack generates a negative voltage where the energy deviation is endured only by the FB-SMs. The capacitance design of the proposed converter follows the same procedures as in [65]. However, the method is modified to calculate the energy deviation of each SM directly instead of the whole MMC stack, to accurately design both the HB-SMs and FB-SMs. The energy deviation of each SM in the MMC stack (ΔE_{SM}) can be calculated from:

$$\Delta E_{SM}(t) = \int_0^t \frac{P_{stack}(x)}{n_{SM}(x)} dx \tag{3.22}$$

where P_{stack} is the MMC stack power and n_{SM} is the number of the functionable SMs during the conducting periods of the MMC stack. n_{SM} depends on the MMC stack voltage as previously illustrated and obeys the following equation:

$$n_{SM}(t) = \begin{cases} n_{HB} + n_{FB} \ , & v_{stack}(t) > 0 \\ n_{FB} \ , & v_{stack}(t) < 0 \end{cases} \tag{3.23}$$

The apparent power is:

$$|\bar{S}| = \frac{3\hat{v}_{a_1}\hat{\imath}_{a_1}}{2} \tag{3.24}$$

where $\hat{v}_{a_1}$ and $\hat{\imath}_{a_1}$ are the fundamental phase peak voltage and current, respectively. The MMC stack power P_{stack} is:

$$P_{stack}(t) = v_{stack}(t)\big(i_{stack}(t)\big) = \frac{2}{3}|\bar{S}|U(t) \tag{3.25}$$

where $U(t)$ is defined as:

$$U(t) = (1 - \sin\omega t + k_3 \sin 3\omega t)(\sin(\omega t + \phi)) \tag{3.26}$$

where ϕ is the power factor angle. By substituting (3.23) and (3.25) into (3.22), the energy deviation of the HB-SM is:

$$\Delta E_{HBSM}(t) = \frac{2}{3}\frac{|\bar{S}|}{(n_{HB} + n_{FB})}\int U(x)\, dx, \qquad v_{stack}(t) > 0 \tag{3.27}$$

The integration is valid only when the MMC stack generates a positive voltage and during the MMC stack conducting period until entering the overlap state, where energy balance

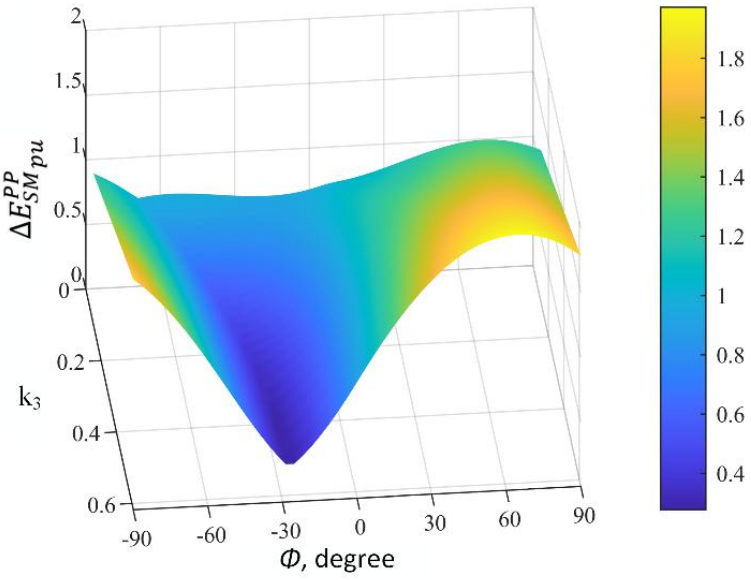
occurs between the upper and lower arms. On the other hand, by doing the same substitution, observing that $n_{FB} = (n_{HB} + n_{FB})k_3/(1 + k_3)$, the energy deviation of the FB-SMs is:

$$\Delta E_{FBSM}(t) = \frac{2}{3}\frac{|\bar{S}|}{(n_{HB} + n_{FB})} \times \begin{cases} \int U(x)\,dx\ , & v_{stack}(t) > 0 \\ \dfrac{1 + k_3}{k_3}\int U(x)\,dx, & v_{stack}(t) < 0 \end{cases} \tag{3.28}$$

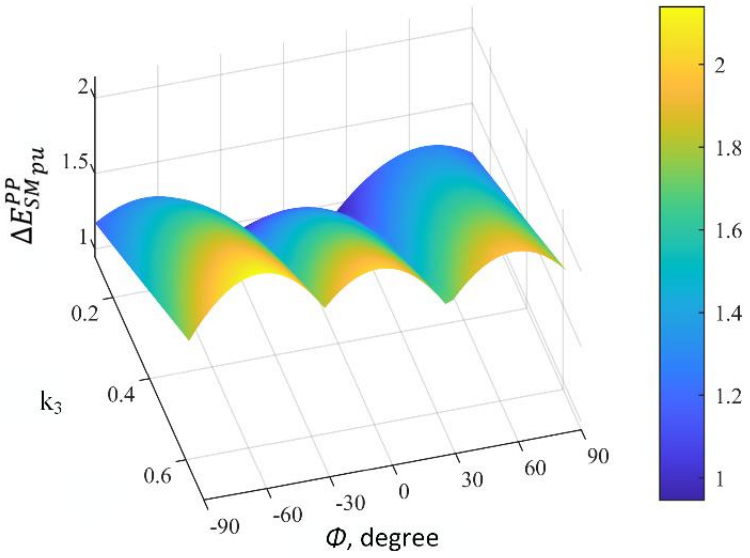
where the factor $(1 + k_3)/k_3$ appears when the MMC stack generates a negative voltage because only the FB-SMs are burdened by the energy deviation in this section. From (3.26), (3.27), and (3.28), k_3 and ϕ affect the energy deviation of the MMC stack SMs. Therefore, Fig. 3.8 is plotted to show the per unit peak-to-peak energy deviation ($\Delta E^{pp}_{SM_{pu}}$) for different values of k_3 and ϕ, which obeys:

$$\Delta E^{pp}_{SM_{pu}} = \frac{10^3 \Delta E^{PP}_{SM}(n_{HB} + n_{FB})}{|\bar{S}|} \tag{3.29}$$

where Fig. 3.8 (a) and (b) show the per unit peak-to-peak energy deviation of the HB-SMs and FB-SMs, respectively, in the MMC stack. Clearly the peak-to-peak energy deviation of both SMs increases with increasing k_3.



(a)



(b)

Fig. 3.8. The per unit peak-to-peak energy deviation of each SM in the MMC stack at different k_3 and ϕ: (a) HB-SM case and (b) FB-SM case.

On the other hand, the peak-to-peak energy deviation of the HB-SMs increases to a maximum value around ϕ=70° because the peak of the arm current matches a larger portion of the MMC stack voltage generation. However, the FB-SMs peak-to-peak energy deviation marginally changes with changing ϕ. The reason is that the FB-SMs, during the negative arm voltage generation (around zero ϕ), burden the energy deviation alone. Also, FB-SMs participate in the energy deviation with the HB-SMs resulting in a more flatten peak-to-peak energy deviation with ϕ. It can be deduced from the curves that the FB-SMs achieve a slightly higher maximum peak-to-peak energy deviation ($\Delta E_{SM\,max}^{pp}$) at each k_3 compared to that of the HB-SMs. Based on the maximum peak-to-peak energy deviation of the HB-SMs/FB-SMs at the desired k_3 deduced from Fig. 3.8 curves, and considering the desired peak-to-peak voltage ripple ratio (ΔV_r^{pp}), the SM capacitance (C_{SM}) is calculated as:

$$C_{SM} = \frac{\Delta E_{SM\,max}^{pp}}{\Delta V_r^{pp}\, V_{c_n}^2} \tag{3.30}$$

3. 3 Simulation Results Validation

The MATLAB-SIMULINK model built for HTMC validation, is based on the 401-level system developed in [66]. The point-to-point connection of the HVDC transmission system is depicted in Fig. 3.9. Since the MMC stack in each arm only handles half the DC link voltage, the MMC stack is comprised of 200 HB-SMs and 40 FB-SMs. To simulate this

large number of SMs efficiently while minimizing computational burden and enabling PWM control to capture the charging and discharging behaviour of the SM capacitors, the converter model is implemented using a switching-function approach. This is achieved by utilizing HB-MMC and FB-MMC blocks in MATLAB with switching function mode. In this mode, the converter is controlled by firing pulses generated by a PWM generator (0/1 signals). Additionally, the model accurately represents the harmonics typically produced by a PWM-controlled converter and correctly simulates rectifying operation and blanking time.

On the other hand, based on the analysis in the previous section, the converter parameters are designed and listed in Table 3.1. Since the thyristor turn off time (t_q) is typically 800 μs, it is suitable to assume that the overall commutation time is 1.26 ms, which corresponds to k_3=0.2 assuming $T_{ov} = T_c$. The arm inductance is selected as 5.5 mH based on (3.20) and (3.21). For capacitance evaluation, the maximum peak-to-peak energy deviation is determined for both SMs from the energy curves in Fig. 3.8 at $k_3 = 0.2$, where $\Delta E_{SM\,max}^{PP}$ of the HB-SM and FB-SM are found to be 5.86 kJ and 6.17 kJ, respectively. Substituting into (3.30) with ΔV_r^{pp}=0.2 (assuming a cell voltage ripple of ±10%), the capacitance of both HB-SM and FB-SM are selected to be 12.5 mF. A filter is used at the DC link terminal to smooth the DC current and limit the short circuit current. The simulation model is tested for normal operation as well as DC fault scenarios in order to validate the proposed converter.

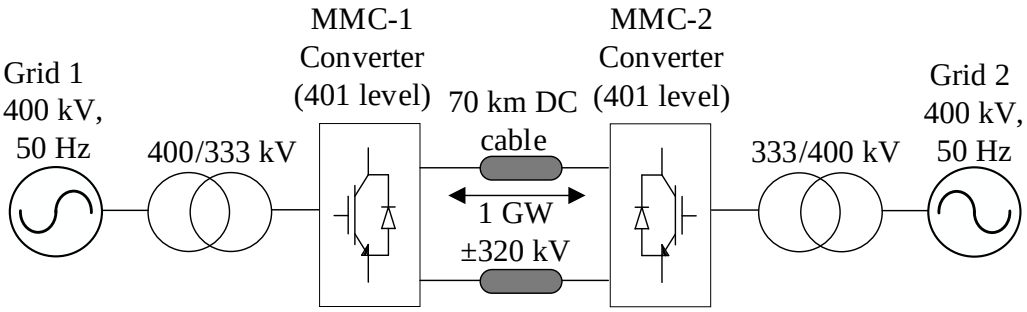


Fig. 3.9. Point-to-point 401-level HVDC transmission system.

Table 3.1: MATLAB Simulation Model Parameters

Parameter	Description	Value
P_r	Rated power	1 GW
V_{dc}	DC link voltage	$\pm$320 kV
v_g	Grid voltage	380 kV
f	Fundamental Frequency	50 Hz
L_{AC}	AC interfacing inductance	68.9 mH
T_c	Overall commutation time	1.26 ms
n_{HB}	Number of HB-SMs per arm	200
n_{FB}	Number of FB-SMs per arm	40
V_c	SM nominal voltage	1.6 kV
C_{HB}/C_{FB}	HB-SMs/FB-SMs capacitance	12.5 mF
L_a	Arm inductance	5.5 mH

3.3.1 Normal Operation

Bidirectional power flow capability is shown in Fig. 3.10(a), where power is reversed successfully in 0.5 s while maintaining zero reactive power. The line voltages and phase currents are depicted in Fig. 3.10(b) and Fig. 3.10(c), respectively, where the third harmonic waveforms do not appear. Also, the commutation time does not affect the output waveforms. The arm currents in the case of grid absorbing and injecting power are shown in Fig. 3.10(d) and Fig. 3.11(a), respectively. The arm currents do not exceed the 1 pu value in both cases, hence low controlled current stresses in the proposed converter are achieved. The stack voltages are depicted in Fig. 3.11(b) and Fig. 3.11(c) in grid absorbing and injecting cases, respectively. In the grid absorbing case, the stack generates a voltage of 0.5pu at the time of commutation because of the negative arm current. However, in the grid-injecting case, the MMC stack produces a voltage of 0.6 pu due to the positive arm current at the instant of commutation. The thyristor valve voltages are shown in Fig. 3.11(d) and Fig. 3.12(a) for absorbing and injecting cases, respectively, where the thyristor valve voltage does not exceed 0.5pu. The simulation results nearly follow the deduced waveform diagrams in Fig. 3.8. The capacitor voltages of the HB-SMs and FB-SMs are shown in Fig. 3.12(b) and Fig. 3.12(c) respectively, where the peak-to-peak voltage ripple does not exceed the 10% limit.

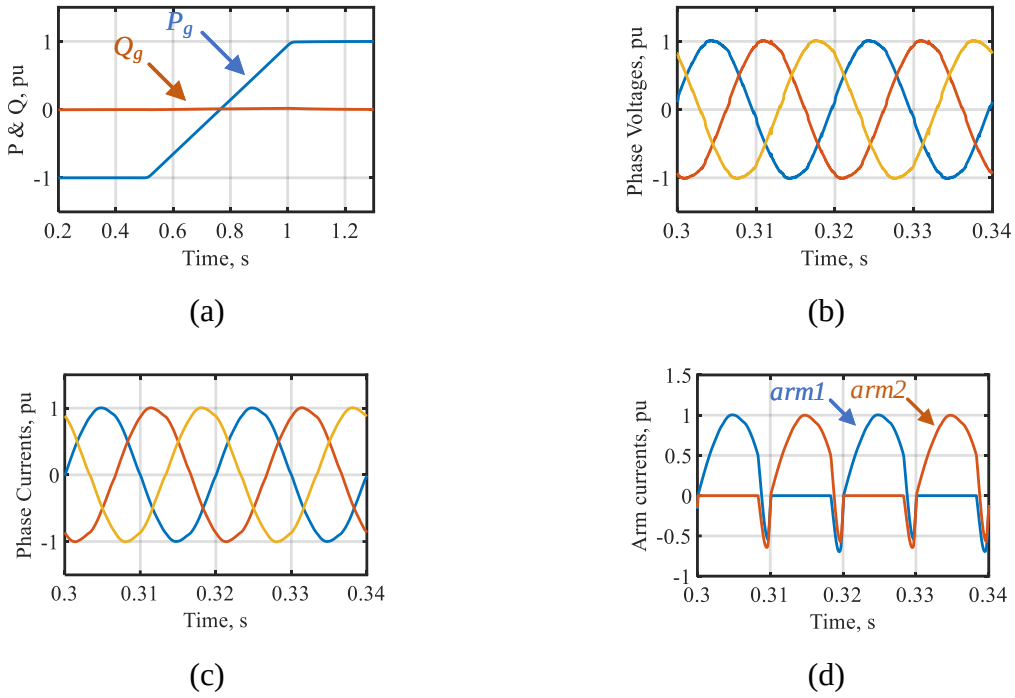


Fig. 3.10. Simulation - normal operation results: (a) The grid active and reactive power, (b) Phase voltages, (c) Phase currents, and (d) Arm currents in the grid absorption case.

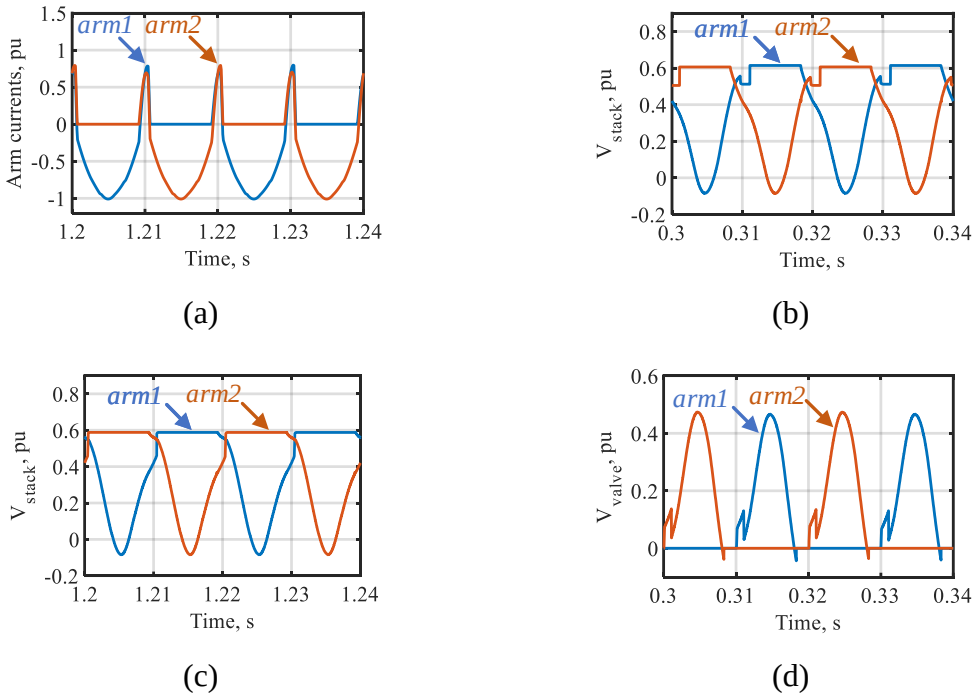
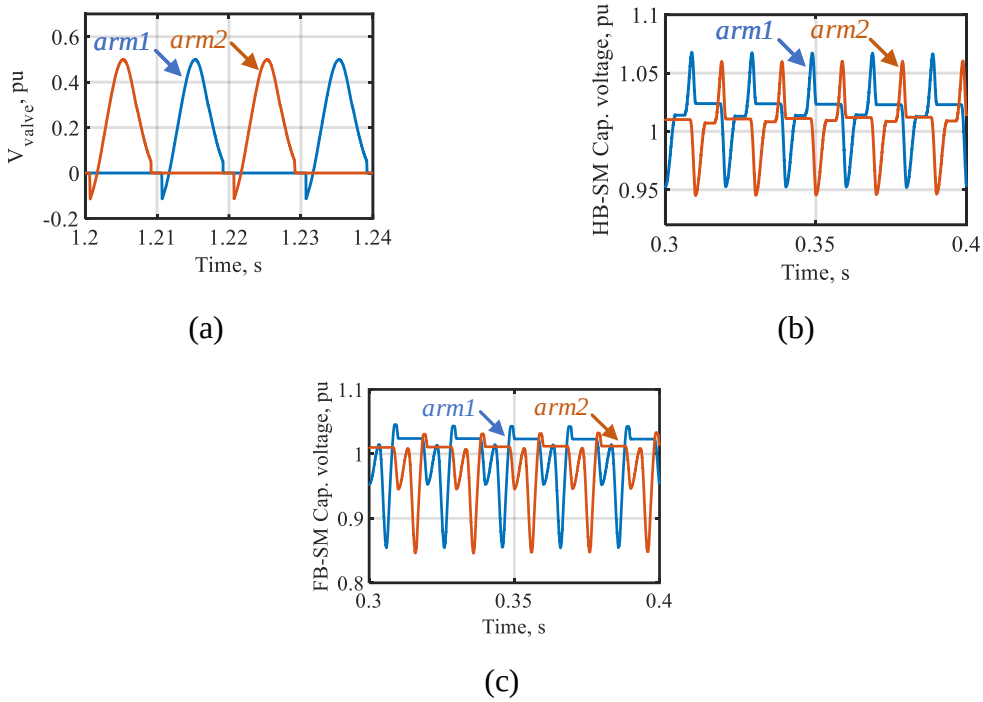


Fig. 3.11. Simulation - normal operation results: (a) Arm currents in the grid injection case, (b) MMC stack voltage in the grid absorption case, (c) MMC stack voltage in the grid injection case, and (d) Thyristor valve voltage in the grid absorption case.



(a) (b)

(c)

Fig. 3.12. Simulation - normal operation results: (a) Thyristor valve voltage in the grid injection case, (b) HB-SM capacitor voltages, and (c) FB-SM capacitor voltages.

3.3.2 DC Fault

To evaluate the DC fault-handling capability of the proposed converter, a DC fault is applied at the DC link terminal at t=0.2s and persists for 100 ms. Fig. 3.13(a) illustrates the DC link voltage and current, where the voltage collapses and the fault current rises sharply at the moment of fault occurrence. This indicates the discharge of the SM capacitors in the overlapped arms. Upon fault detection, all SMs are blocked, and the protection thyristors are triggered to bypass the AC component of the DC fault current until it is interrupted by the thyristor valve. Fig. 3.13(b) provides a zoomed view of the DC link voltage and current, showing that the DC current is quickly blocked as the FB-SMs inject a negative voltage opposing the discharging current, as depicted in Fig. 3.13(c). A further zoomed view in Fig. 3.13(d) highlights that the FB-SMs, even in their blocked state, continue to inject a negative voltage until the current is completely suppressed. The arm currents of leg 1, shown in Fig. 3.13(e) and (f), confirm that arm 1 and arm 2 are in the overlap state at the instant of the fault. Additionally, the DC component of the fault current in the arm remains below 2 pu, ensuring safe operation during the DC fault scenario. Fig. 3.13(g) and (h) depict the phase currents, demonstrating the successful isolation of the DC fault and validating the proposed converter's effectiveness in blocking DC fault currents. Furthermore, the post-fault recovery capability of the converter is also demonstrated, ensuring reliable operation following fault clearance.

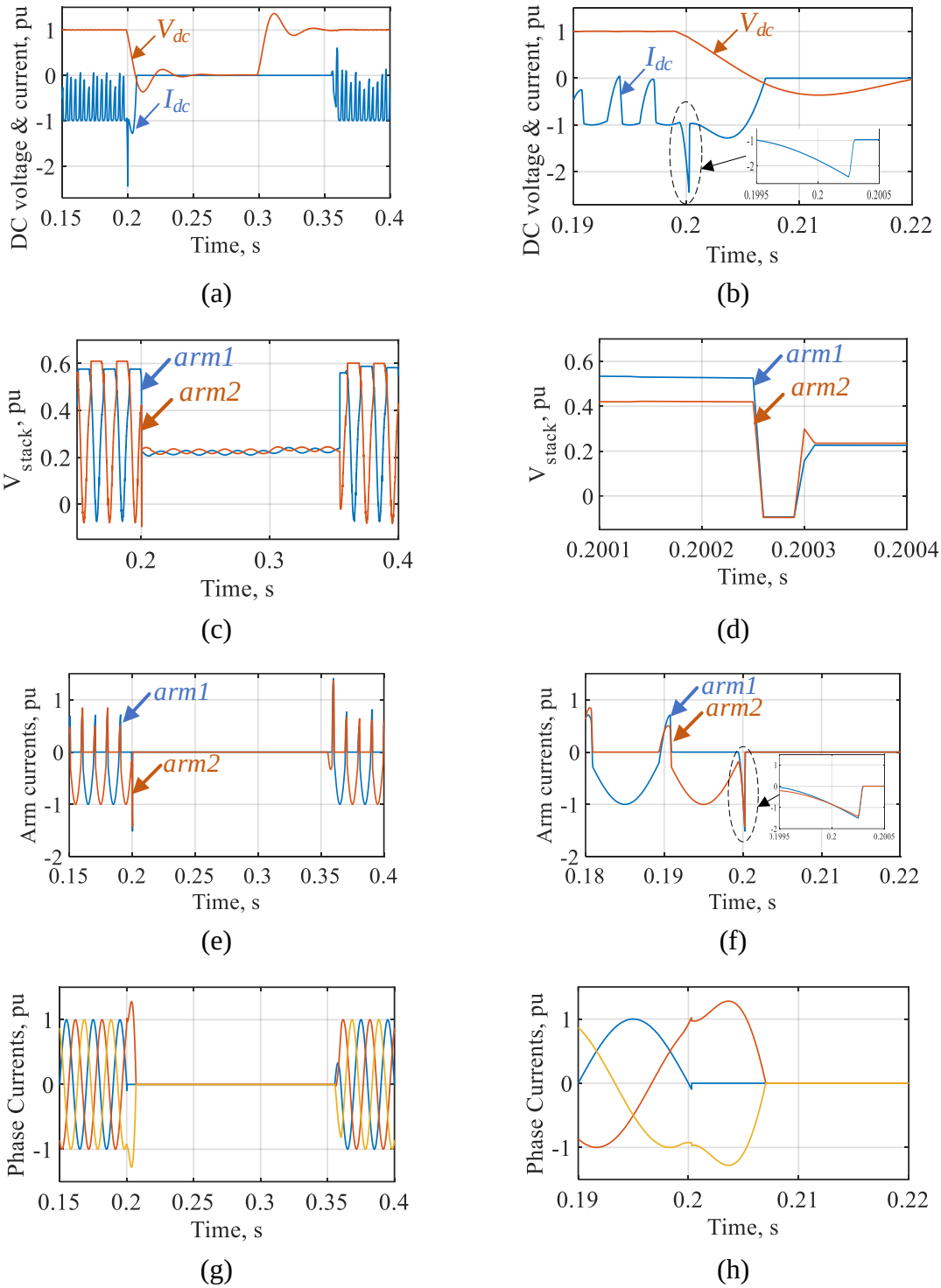


Fig. 3.13. Simulation - DC fault results: (a) DC link voltage and current, (b) zoomed DC link voltage and current (c) MMC stack voltage, (d) zoomed MMC stack voltage, (e) Arm currents, (f) zoomed arm currents, (g) Phase currents, (h)zoomed phase currents.

3. 4 Experimental Setup

A scaled-down experimental test rig is used to assess the proposed converter, using 3-phase 5-levels as shown in Fig. 3.14, where each arm has 2 HB-SMs, 1 FB-SM, and 1

antiparallel thyristor. The controller used is LAUNCHXL-F28379D that uses 200 MHz dual C28xCPUs and has around 69 GPIOS (general-purpose input output), 16 ADC (analog to digital) channels, and 12 ePWM. Furthermore, a CINERGIA grid emulator is used for grid integration. CINERGIA's grid emulators are AC programmable voltage sources specifically designed to create AC grids and emulate disturbances. The emulator used in this setup has a rated power of up to 15 kVA, with a maximum voltage of 750 V and a current rating of 60 A. On the other hand, the DC grid is emulated using a bidirectional power supply from Itech (IT6006C-500-40), which has a rated voltage of 500 V and a rated current of 40 A.

The hardware components including the IGBT device, its gate driver, thyristors and its gate driver, sensors, etc are listed in Table 3.2. The schematics for power and control circuits for the HB-SMs, FB-SMs, thyristors, and sensors are listed in Appendix A. Moreover the experimental parameters are calculated and listed in Table 3.3. Since the ratio between the FB-SMs and HB-SMs is 50%, k_3 can be increased to 0.5. Therefore, the overall commutation time T_c=1.6 ms is selected. It is worth noting that a level-shifted PWM technique is used to control the SMs of the proposed converter, with a rotational scheme implemented to achieve capacitor balancing between the upper and lower arms. Furthermore, to enable the DSP to control multiple SMs within the same arm, the reference signals from the control algorithm are compared to carriers generated within the DSP, and the corresponding gating signals are produced via GPIOs. This approach is suitable in this case, as a low switching frequency is employed— a common practice in HVDC converters to minimize switching losses.

Three cases are considered in the experimental study: normal operation, power reversal, and a DC fault.

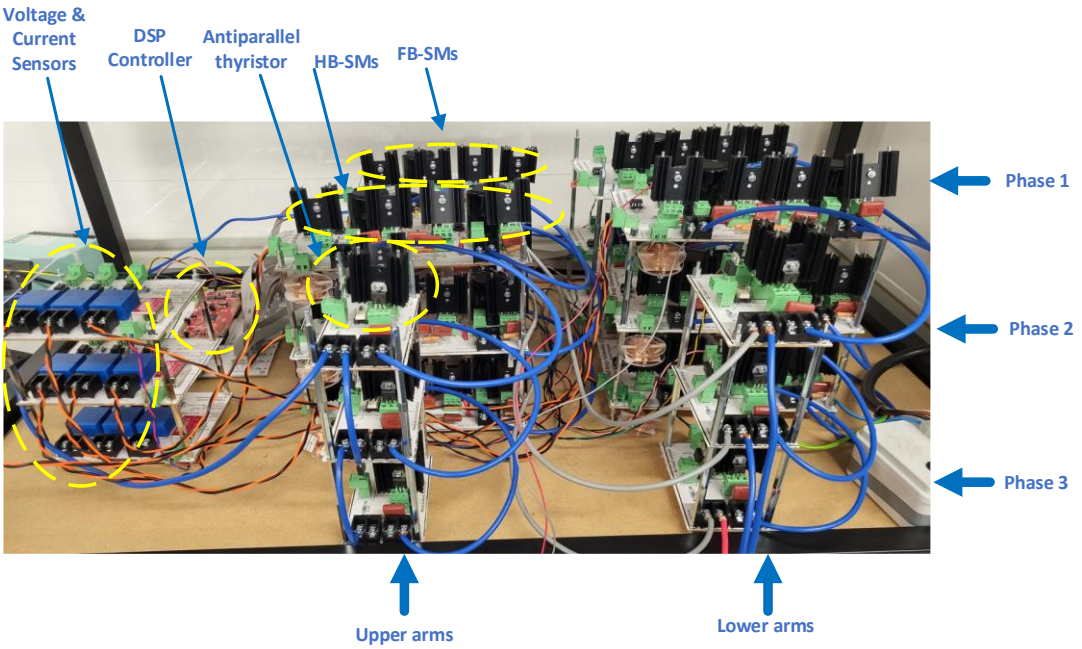


Fig. 3.14. The experimental test rig.

Table 3.2: Hardware components

Controller	DSP	LAUNCHXL-F28379D
Grid	Grid Emulator	CINERGIA's Grid Emulators (GE15)
DC grid	ITech Bidirectional Power Supply	IT6006C-500-40
IGBT	IGBT name	ONSEMI FGH40N60SMD, 600 V 80 A
	Optocoupler	6n139
	Gate driver	IR2111 (2 channels)
	DC/DC Converter	MPB1215S-1W (12 V:15 V)
Thyristor	Thyristor name	TYN640RG, 600 V 40 A
	Optocoupler	MOC3022-M (Triac)
Sensors	Voltage sensor	LV 25-P
	Current sensor	LEM LA 25-NP
	Operational amplifier	TL071ACP
	DC-DC converter	TEN 5-1223 (12 V : ±15 V)
Others	Capacitor unit	MCLPR100V109M40X6–10,000 µF, 100 V
	Power terminals	6PCV-02-006

Table 3.3: Experimental Parameters

Parameter	Description	Value
P_r	Rated power	200 W
V_{dc}	DC link voltage	140 V
v_g	Grid voltage	52 V
f	Fundamental frequency	50 Hz
fs	Switching frequency	1150 Hz
L_{AC}	AC interfacing inductance	20 mH
T_c	Overall commutation time	1.6 ms
n_{HB}	Number of HB-SMs per arm	2
n_{FB}	Number of FB-SMs per arm	1
V_c	SM nominal voltage	35 V
C_{SM}	SM capacitance	8.2 mF
L_a	Arm inductance	0.47 mH
R_{fault}	Fault resistance	8 Ω

3.4.1 Normal Operation

The proposed HTMC is connected to a 3-phase grid as shown in Fig. 3.15(a) using the grid emulator as previously discussed, where the phase currents are depicted in Fig. 3.15(b). The phase currents are not deformed by the third harmonic subtraction or by thyristor commutation action, which validates the proposed control. The arm currents of the proposed HTMC shown in Fig. 3.15(c) indicate low current stress on the semiconductors. It is worth noting that the noise seen on the arm currents are due to the snubber circuit of the series thyristors which make a path for a circulating current each time a SM is inserted or bypassed. This issue is solved in the experimental setup of Chapter 5. The MMC stacks operate with balanced SM capacitor voltages as shown in Fig. 3.15(d) thanks to the rotation scheme implemented with the level shifted PWM. The MMC stack voltages are depicted in Fig. 3.15(e), where a negative voltage exists due to the third harmonic subtraction. The thyristor valve voltages are depicted in Fig. 3.15(f), where a negative voltage occurs due to thyristor commutation action performed by the MMC stack.

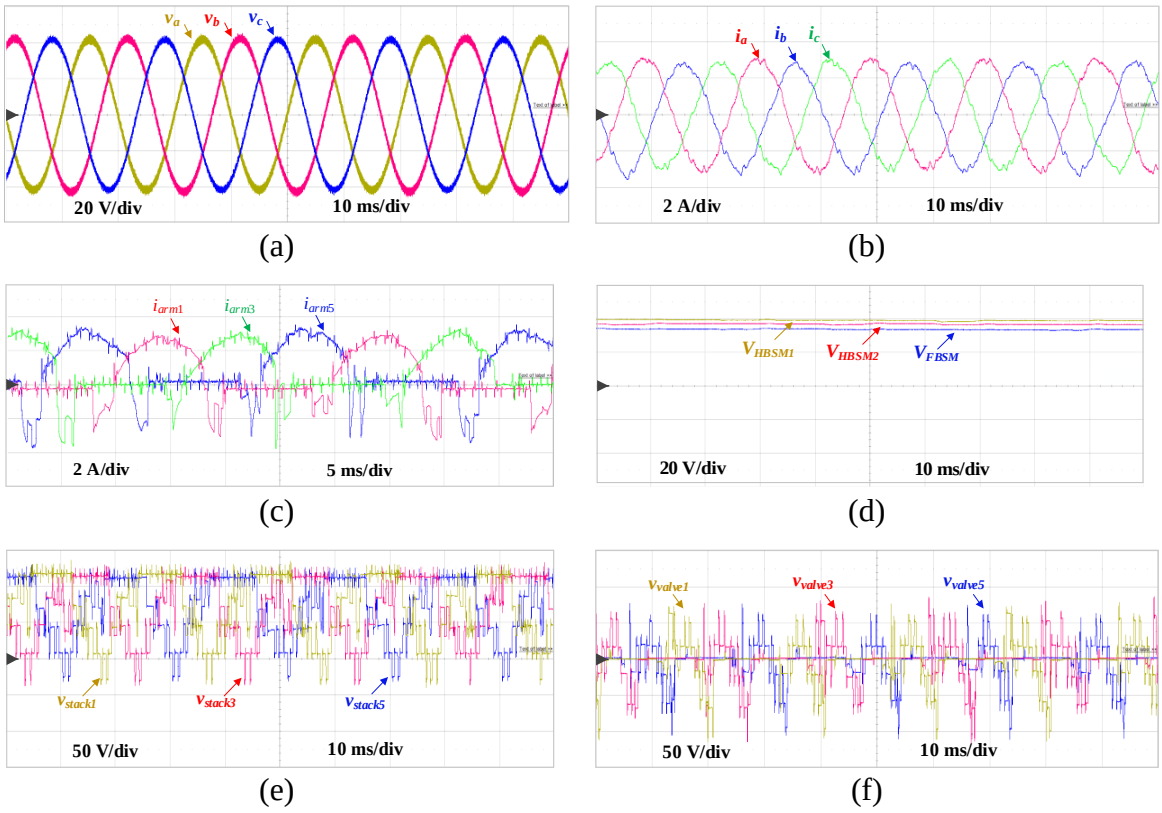


Fig. 3.15. Experimental - normal operation results: (a) The grid phase voltages, (b) Phase currents, (c) Arm Currents, (d) MMC stack 1 capacitor voltages, (e) MMC stack voltages, and (f) Thyristor valve voltages.

3.4.2 Power Reversal

To test the bidirectional capability of the proposed HTMC, the power flow is initially from the DC side to the grid at 200 W then power reversal action occurs, -200 W, while maintaining zero reactive power, as seen in Fig. 3.16(a). It is worth noting that the active and reactive power calculations are performed inside the DSP, generated through the digital to analogue converter (DAC), and then measured using an oscilloscope. The phase 'a' voltage and current are shown in Fig. 3.16(b). where the voltage and current are in-phase at the instant of positive power and out-of-phase at the instant of negative power; indicating successful power reversal operation of the proposed HTMC.

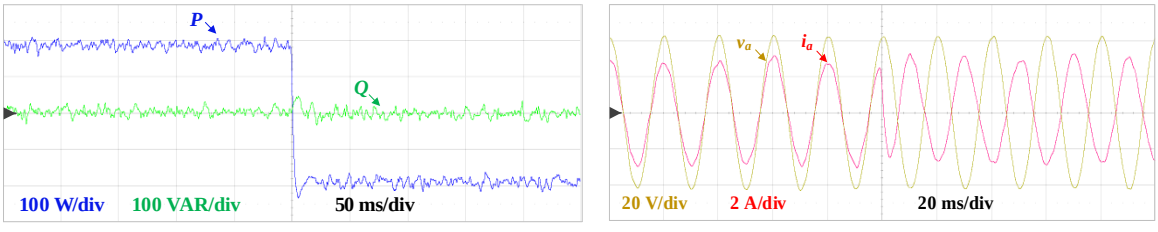
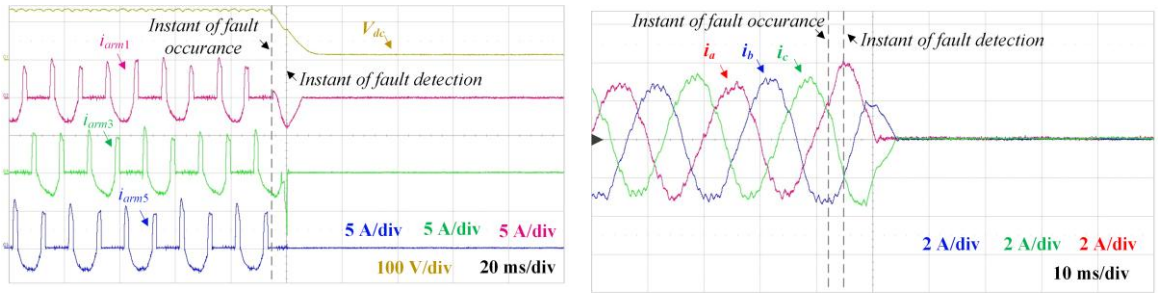


Fig. 3.16. Experimental - power reversal results: (a) Active power and reactive power and (b) Phase 'a' AC voltage, and phase 'a' AC current.

3.4.3 DC fault

To further validate the DC fault-blocking capability of the proposed converter, a DC fault is tested experimentally. The DC fault is implemented by connecting a low resistance in parallel with the DC source. It is important to set the DC source current limit to a low value to ensure that the voltage collapses instantly when the fault occurs. Fig. 3.17(a) shows that the DC link voltage starts to collapse at the instant of fault occurrence. The upper arm current of the second leg (I_{arm_3}) clearly starts to increase rapidly indicating that this arm is in the overlap state at the fault instant. After fault detection, the arm current (I_{arm_3}) is decreased rapidly to zero by the action of the FB-SMs. On the other hand, the DC fault AC component seen in arm 1 current (I_{arm_1}) is inherently extinguished by thyristor valve action. The phase currents depicted in Fig. 3.17(b) indicate successful isolation of the DC fault, validating the effective blocking of DC fault currents within the proposed converter.



(a) (b)

Fig. 3.17. Experimental – dc fault results: (a) DC link voltage and arm currents and (b) Phase currents.

3. 5 Comparison

To highlight the features and advantages of the proposed HTMC converter, an extensive comparison is performed in this section, with several converters reported in the literature, in terms of semiconductor count and type, passive elements, current stresses, losses, cost, weight, size, and dc fault clearing time. Typical ABB switches and thyristors are used in the comparison in Table 3.4.

The number of SMs per arm are calculated based on the number of levels (401) and the topology nature. Then the number of semiconductors (IGBTs and/or thyristors) are determined. Furthermore, the capacitance value in the SM for each topology is determined based on the method provided in [65]. Each SM capacitor is a combination of the capacitor labelled as C44UVGT7105M34K (1,050µF, 1,800V, 5.1kg, 5,311cm3, $136.67) [67]. Thus

parallel capacitors are utilised in the SM of each topology to reach the required value. Moreover, the capacitor rated current should be considered, where extra parallel branches can be added to decrease the capacitor current.

The conduction and switching losses are calculated based on [68], with an average switching frequency of 250 Hz. The average conduction loss ($P_{cond_{av}}$) is calculated as follows:

$$P_{cond_{av}} = f_o \int_0^{1/f_o} p_{cond_{ins}}(t)dt \tag{3.31}$$

where $p_{cond_{ins}}$ is the instantaneous conduction loss and calculated as follows:

$$p_{cond_{ins}}(t) = u_{cond}\big(i_x(t), T_j\big)\, i_x(t)\, M(m,t) \tag{3.32}$$

where u_{cond} represents the voltage drop on the power device, i_x is the arm current, M is the duty ratio which represents the time percentage of conduction. Also it is a function of the modulation index (m). Furthermore, the power device voltage drop (u_{cond}) is calculated as follows:

$$\begin{aligned} u_{cond}\big(i_x(t), T_j\big) &= \Big[U_{cond_{o_{Tref}}} + K_{T1}\big(T_j - T_{ref}\big)\Big] \\ &+ i_x(t)\Big[r_{cond_{o_{Tref}}} + K_{T2}\big(T_j - T_{ref}\big)\Big] \end{aligned} \tag{3.33}$$

where $U_{cond_{o_{Tref}}}$, K_{T1}, $r_{cond_{o_{Tref}}}$, K_{T2} are coefficients obtained from the datasheet. T_{ref} is the reference temperature (25°C or 125°C). Similarly, the average switching loss is calculated as follows:

$$P_{sw_{av}}(t) = f_o \int_0^{1/f_o} p_{sw_{inst}}(t)dt \tag{3.34}$$

where $p_{sw_{inst}}$ is the instantaneous switching loss and is calculated as follows:

$$P_{sw_{inst}}(t) = f_{sw} E_{sw} \left(\frac{V_{cn}}{V_{ref}}\right)^{K_v} \left(\frac{i_x}{i_{ref}}\right)^{K_i} \Big(1 + K_T\big(T_j - T_{ref}\big)\Big) \tag{3.35}$$

where E_{sw} is the switching energy loss and represents the sum of E_{on} and E_{off} in case of a switch and E_{rr} in case of a diode. K_T is the temperature coefficient. K_v and K_i are the voltage and current coefficients, respectively and are calculated based on [69]. V_{ref} is the reference

blocking voltage of the switch and i_{ref} is the reference current of the switch. Furthermore, some of the MATLAB scripts used in the losses calculations can be found in Appendix B at the end of the thesis.

The arm inductance value of the MMC topologies is selected to be 46 mH (0.1 pu) as suggested in [6]. On the other hand, using the design criteria proposed in Chapter 3.2.2, the arm inductance for the proposed topology is selected 5.5 mH (~0.01) pu. Since, same single arm-based operation is applied for the AAC topology, the same value is selected for the AAC topology. Moreover, regarding the size, weight, and losses of the inductors, it has been calculated based on the practical approach of designing the inductors as given in [6]. The inductance value is estimated using the following formula:

$$L = 0.2\,\text{x}10^{-6} * \pi^2 a * \frac{2a}{l_{th}} * N^2 * K \tag{3.36}$$

where N is the total number of turns and K is Nagaoka's constant.

$$K = \frac{1}{1 + 0.9\frac{a}{l_{th}} + 0.32 * \frac{t}{a} + 0.84\frac{t}{l_{th}}} \tag{3.37}$$

where, t is the thickness of turns, a is the average radius of turns, l_{th} is the length of the coil, and r_i is the radius of the wire as depicted in Fig. 3.18.

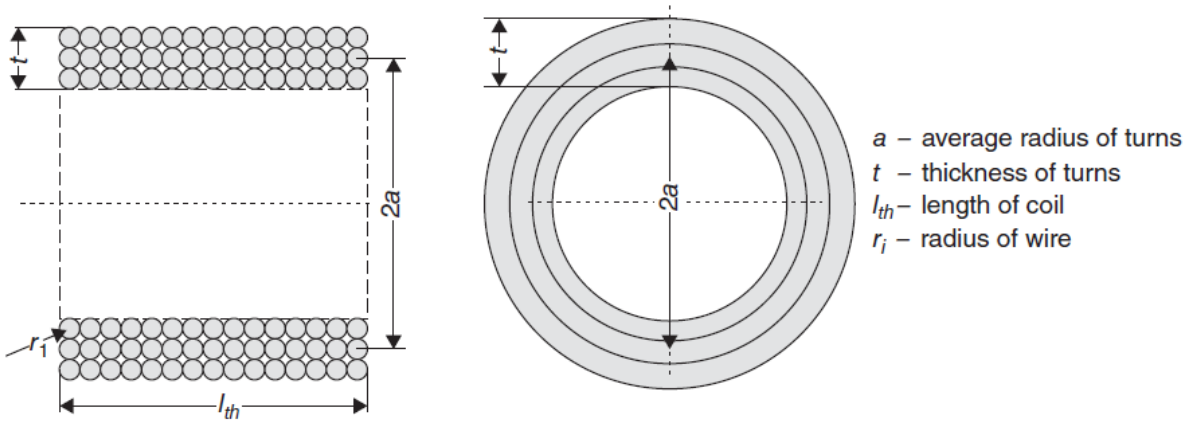


Fig. 3.18. Solenoid air-core inductor [6].

Assuming that current density is 2 A/mm2, the conductor cross section and its radius will be 500 mm2 and r_i=12.6 mm respectively. A 10% enamel insulation thickness is also assumed. Taking 11 layers and 20 turns in each layer as the same terminology used in [6], gives N=220, l_{th}=0.5544 m, and with t=0.304 m. Considering an average radius of turns a=0.5+t/2=0.6525 m, gives L=48.3 mH. The total length of the wire =842.6 m, total volume of the inductor is

1.1 m3, the total weight of the inductor 3,760 kg, and the total resistance is 0.0292 Ω. On the other hand, for the design of the arm inductor for the proposed converter, taking 5 layers and 13 turns in each layer gives N=65, l_{th}=0.36 m, and with t=0.1386 m. Considering an average radius of turns a=0.5+t/2=0.5693 m, gives L=5.3 mH. The total length of the wire =232.5 m, total volume of the inductor is 0.462 m3, the total weight of the inductor 1,038.1 kg, and the total resistance is 0.008 Ω. Furthermore, regarding the cost of the arm inductors, it can be calculated approximately by multiplying the total weight of the inductor by the price per kg of the copper. Hence, the cost per arm inductor in case of MMC topologies is 3,760x$8.37=$31,490 while the cost per arm inductor in case of the proposed topology is 1,038.1x$8.37= $8,689.

It is worth noting that all passive elements and semiconductors are considered in the size, weight, and cost calculations, where an extra 15% is assumed in the volume calculations to account for structural and cooling requirements. The total cost, weight, and volume are determined using the following equations, respectively:

$$Cost_{total} = \sum_{x} Cost_x N_x \tag{3.38}$$

$$Weight_{total} = \sum_{x} Weight_x N_x \tag{3.39}$$

$$Vol_{total} = 1.15 \sum_{x} Vol_x N_x) \tag{3.40}$$

where $Cost_x$, $Weight_x$, Vol_x, and N_x represents the cost, weight, volume and number of the x component respectively. x represents different components of the system, including capacitors (SMs and DC filter), IGBT switches, thyristors, bypass thyristors, inductors (converter arms and DC filter) Besides, the DC clearing time is based on the method provided in [33].

The comparison is carried out between non-thyristor-based converters, such as the HB-MMC with a solid-state DC CB [23, 70], FB-MMC [25], Hybrid MMC [26], and AAC [28], and thyristor-based converters such as the thyristor bypass-based MMC (TB-MMC)

[32], crossing thyristor branches-based MMC (CTB-MMC) [33], power group (PG)-based FB-MMC [37, 39] and PG-based Hybrid MMC [37, 39]; as depicted in Table 3.5. The comparison is based on a typical 401-level MMC-based HVDC system with 1 GW rated power and a ±320 kV DC link. The nominal voltage per SM is 1.6 kV while the nominal voltage per thyristor is 4 kV. The DC filter is considered in all (cost, weight, size, and losses) calculations for both the proposed and the AAC topologies. It is assumed that the DC-link filter capacitance is equivalent to a single leg as stated in [65]. From the comparison table, in terms of capacitor number, total converter weight, and size: the proposed HTMC is second after the AAC. However, considering the number of IGBTs, overall cost, and semiconductor losses: the proposed HTMC is first among all candidates, achieving the lowest number of IGBTs, cost and semiconductor losses. But, in terms of DC fault clearing time, the proposed converter achieves 15~18 ms, which is considered higher than other topologies, except the TB-MMC, due to thyristor commutation time.

Table 3.4: Typical ABB Semiconductors Parameters

Parameters	IGBT Module 5SNA 1800E330400		Thyristor 5STP 12K6500	SM Bypass thyristor 5STP 12F4200
	IGBT	Diode		
Max voltage	3300 V		6500 V	4200 V
RMS Current	1800 A		2250 A	1860 A
On-state voltage at 125°C	3.2 V	2.65 V	1.84 V	1.86 V
On-state resistance at 125°C	0.1 mΩ	0.1 mΩ	0.647 mΩ	0.545 mΩ
Turn on & off switching or reverse recovery energies at 125°C	4.3+4 J	2.3 J	0.3+4.2 J	0.3+0.8 J
Size	1010.8 cm^3		291.2 cm^3	117.25 cm^3
Weight	1.19 kg		1.15 kg	0.6 kg
Cost/unit	$2063		$904.96	$242.61

3. 6 Summary

This chapter introduced a novel Hybrid Thyristor-based Multilevel Converter (HTMC) with DC fault-blocking capability. The proposed HTMC analysis has been illustrated in both normal operation and under DC fault scenarios. In the analysis, a third

harmonic waveform has been subtracted from the fundamental waveform to take advantage of the FB-SMs negative voltage capability in normal operation. This enhances the overlapping period between the upper and lower arms and allows longer periods for thyristor commutation. Hence, at k=0.2, sufficient overlap and commutation times are achieved. The proposed converter capabilities have been validated via a 401-level MATLAB-SIMULINK model and experimentation on a scaled-down 3-phase 5-level system. A detailed comparison with alternative converters has been provided in terms of semiconductor count, passive elements, cost, current stresses, losses, DC fault-clearing speed, size, and weight. The proposed HTMC has a relatively slow fault-clearing speed since it mainly depends on the thyristor valve action. However, the proposed HTMC is first in terms of a lower IGBT count (30% lower than the next best topology), lower losses due to the usage of thyristor valves (10% lower than the nearest converter), and lower cost (19% lower than the nearest). It is second in terms of the overall weight, volume, and capacitor count. Hence, the results indicate that the proposed HTMC is a worthy candidate for HVDC applications.

Table 3.5: Key Feature Comparison of Different Converters based on 401 level HVDC system parameters

Converter Type	HB-MMC with Solid-state DC CB [23, 24]	TB-MMC [32]	FB-MMC [25]	Hybrid MMC [26]	AAC [28]	PG-based Hybrid-MMC [37, 39]	CTB-based MMC [33]	**Proposed converter (HTMC)**
No. of SMs	400x6	400x6	400x6	400x6	255x6	400x6	400x6	**240x6**
Capacitance per SM	10.5 mF	10.5 mF	10.5 mF	10.5 mF	5.25 mF	10.5 mF	10.5 mF	**12.5 mF**
Total number of capacitors	10x400x6 =24000	10x400x6 =24000	10x400x6 =24000	10x400x6 =24000	5x255x8 =10200	10x400x6 =24000	10x400x6 =24000	**12x240x8 =23040**
No. of IGBTs	2x400x6+400 =5200	2x400x6 =4800	4x400x6 =9600	4x200x6 +2x200x6 =7200	4x255x6 +200x6 =7320	4x200x6 +2x200x6 =7200	2x344x6 +3x56x6 =5400	**4x40x6 +2x200x6 =3360**
No. of Thyristors	None	200x6 =1200	None	None	None	2x200x6 =2400	200x6 =1200	**2x100x6 +40x6+200x6 =2640**
Arm inductor	46 mH (0.1 pu)	46 mH (0.1 pu)	46 mH (0.1 pu)	46 mH (0.1 pu)	5.5 mH (0.012 pu)	46 mH (0.1 pu)	46 mH (0.1 pu)	**5.5 mH (0.012 pu)**
RMS arm currents	$\frac{1}{\sqrt{3}} I_{dc}$	$\frac{1}{\sqrt{3}} I_{dc}$	$\frac{1}{\sqrt{3}} I_{dc}$	$\frac{1}{\sqrt{3}} I_{dc}$	$\frac{\pi}{6} I_{dc}$	$\frac{1}{\sqrt{3}} I_{dc}$	$\frac{1}{\sqrt{3}} I_{dc}$	$\boldsymbol{\frac{2}{3} I_{dc}}$
DC Fault clearing time	3~5 ms	19~24 ms	0.5~1 ms	1.5~3 ms	1~2 ms	1.5~3 ms	0~3 ms	**15~18 ms**
Total semiconductor losses	8.76 MW 0.876%	7.77 MW 0.777%	12.87 MW 1.287%	10.32 MW 1.032%	8.02 MW 0.802%	6.22 MW 0.622%	8.48 MW 0.848%	**5.58 MW 0.558%**
Overall Cost	$16.06 M	$14.26 M	$23.09 M	$18.13 M	$16.5 M	$20.31 M	$15.5 M	**$11.59 M**
Overall Weight	153.37 tons	155 tons	156.4 tons	153.5 tons	62.92 tons	162.2 tons	155.7 tons	**134.9 tons**
Overall Volume	160.82 m^3	160.89 m^3	165.33 m^3	162.54 m^3	74.83 m^3	164.8 m^3	161.58 m^3	**149.97 m^3**

Chapter 4

New Fast DC Fault Blocking Hybrid Thyristor-based Multilevel Converter (F-HTMC) for Offshore Networks

In this Chapter, a modification to the HTMC is proposed, referred to as fast DC fault blocking HTMC (F-HTMC), aiming to achieve rapid DC fault blocking capability and a smooth current flow at the DC side without the necessity of a large DC filter. The proposed F-HTMC incorporates additional parallel branches of bidirectional thyristors with the upper SMs. These parallel bidirectional thyristors serve the function of circulating the AC grid injection of the fault current during a DC fault, facilitating swift isolation of the DC fault. Furthermore, achieving a smooth DC current is realised by extending the overlap period to 60 degrees, extensively discussed in this Chapter.

4. 1 Converter Structure and Operation Analysis

4.1.1 Converter Structure

The Fast DC Fault Blocking Hybrid Thyristor-Based Multilevel Converter (F-HTMC) comprises a 3-phase system with six arms, as illustrated in Fig. 4.1. Each arm incorporates HB-SMs, FB-SMs, and bidirectional thyristors. The series bidirectional thyristors are designated as operation thyristors, while the parallel bidirectional thyristors are named protection thyristors. Operation thyristors operate during normal conditions, reducing conduction losses, and during DC fault cases, interrupting the fault current. Protection-thyristors, however, are exclusively functional during DC fault scenarios. On the other hand, HB-SMs generate the output AC voltage waveform, while FB-SMs ensure an overlap state, maintaining balance between the SMs within the same leg. FB-SMs also facilitate the commutation of operation thyristors at the end of their conduction cycle. Both HB-SMs and operation thyristors are rated to half of the DC-link voltage (½V_{dc}), while FB-SMs are rated to $\pm\Delta V$. Protection thyristors are rated to the sum of both HB-SMs and FB-SMs (½$V_{dc} + \Delta V$).

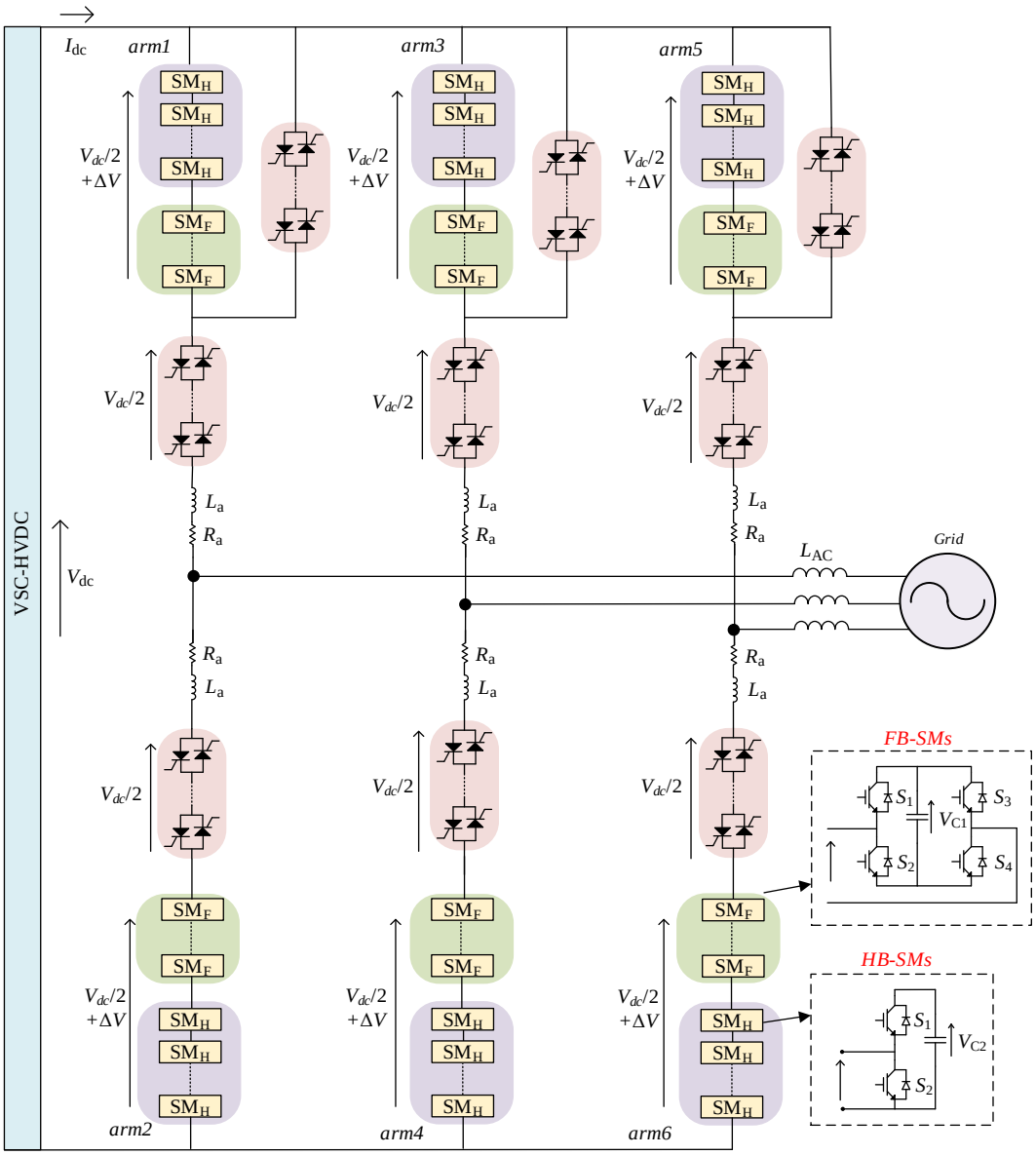


Fig. 4.1. The proposed converter structure.

4.1.2 Converter Operation Analysis

To ensure a seamless flow of DC current without the necessity of large filters, it is essential to maintain a 60-degree overlap state. This condition dictates that at any given moment, one leg is in an overlap state, ensuring an uninterrupted path for the DC current. Achieving a 60-degree overlap state would typically require a substantial quantity of FB-SMs if considering only the fundamental waveform. However, by subtracting a zero-sequence waveform from the fundamental waveform, a 60-degree overlap state can be achieved with a significantly reduced number of FB-SMs. Depending on the HB-SMs, the fundamental phase voltage peak value ($\hat{v}_{a_1}$) can be equal to $½V_{dc}$ as follows:

$$v_{a_1}(t) = \hat{v}_{a_1} \sin \omega t = ½V_{dc} \sin \omega t \qquad (4.1)$$

where ω is the angular frequency. Taking advantage of the FB-SMs negative voltage, the subtracted third harmonic waveform voltage (v_{a_3}) can be:

$$v_{a_3}(t) = \Delta V \sin 3\omega t = k_3 \hat{v}_{a_1} \sin\ 3\omega t \qquad (4.2)$$

where k_3 is the third harmonic voltage ratio. Therefore, the resultant phase voltage $v_a(t)$ can be:

$$v_a(t) = ½V_{dc}(\sin \omega t - k_3 \sin 3\omega t) \qquad (4.3)$$

To achieve required overlap time (T_{ov}) and overall commutation time (T_c), the upper and lower SMs voltages are calculated as follows:

$$v_a^+ = \begin{cases} ½V_{dc} - v_a\,, & -T_h < t < ½T_p + T_h - T_c \\ V_{comm}^+, & ½T_p + T_h - T_c < t < ½T_p + T_h \\ ½V_{dc} + \Delta V, & ½T_p + T_h < t < T_p - T_h \end{cases} \qquad (4.4)$$

$$v_a^- = \begin{cases} V_{comm}^-\ , & T_h - T_c < t < T_h \\ ½V_{dc} + \Delta V, & T_h < t < ½T_p - T_h \\ ½V_{dc} + v_a, & ½T_p - T_h < t < T_p + T_h - T_c \end{cases} \qquad (4.5)$$

$$V_{comm}^{\pm} = \begin{cases} ½V_{dc}, & i_a^{\pm} < 0 \\ ½V_{dc} + \Delta V, & i_a^{\pm} > 0 \end{cases} \qquad (4.6)$$

where v_a^+, v_a^- are the upper and lower SMs voltage, respectively, $T_h = \frac{T_{ov}+T_c}{2}$, and $V_{comm} = ½V_{dc} + \Delta V$ if the arm current is positive at the instant of commutation while $V_{comm} = ½V_{dc}$ if the arm current is negative at the instant of commutation. On the other hand, the upper and lower arm currents are as follows:

$$i_a^+ = \begin{cases} I_{dc} - i_{c_1}\,, & -T_h < t < T_h - T_c \\ i_{a_1}, & T_h - T_c < t < ½T_p - T_h \\ I_{dc} - i_{b_1}, & ½T_p - T_h < t < ½T_p + T_h - T_c \\ 0, & ½T_p + T_h - T_c < t < T_p - T_h \end{cases} \qquad (4.7)$$

$$i_a^- = \begin{cases} I_{dc} + i_{b_1}\,, & -T_h < t < T_h - T_c \\ 0, & T_h - T_c < t < ½T_p - T_h \\ I_{dc} + i_{c_1}, & ½T_p - T_h < t < ½T_p + T_h - T_c \\ -i_{a_1}, & ½T_p + T_h - T_c < t < T_p - T_h \end{cases} \qquad (4.8)$$

where, i_a^+, i_a^- are the upper and lower arm currents of phase 'a', i_{a_1}, i_{b_1}, i_{c_1} are the three phase currents, and I_{dc} is the DC current. Also, it should be noted that the falling time of the thyristor current (T_f) is neglected for simplicity. Besides, the phase currents are as follows:

$$\begin{aligned} i_{a_1} &= \hat{\imath}_{a_1} \sin(\omega t + \phi) \\ i_{b_1} &= \hat{\imath}_{a_1} \sin(\omega t - 120 + \phi) \\ i_{c_1} &= \hat{\imath}_{a_1} \sin(\omega t + 120 + \phi) \end{aligned} \tag{4.9}$$

where, ϕ is the phase shift between the AC phase voltage and current and $\hat{\imath}_{a_1}$ is the phase current peak value. Appling power balance between the AC and DC sides of the converter assuming a lossless operation as follows:

$$P_{ac} = P_{dc} = \frac{3}{2} \hat{v}_{a_1} \hat{\imath}_{a_1} \cos(\phi) = V_{dc} I_{dc} \tag{4.10}$$

Knowing that the peak phase voltage is half the DC link voltage, then I_{dc} can be calculated as follows:

$$I_{dc} = \frac{3}{4} \hat{\imath}_{a_1} \cos(\phi) \tag{4.11}$$

For a clearer explanation, Fig. 4.2 shows the operational waveforms of the F-HTMC for phase 'a' throughout the operational cycle, divided into six sections from *a* to *c* and *a'* to *c'* (three sections for each half cycle). Understanding these sections is crucial, thus more illustrations are provided where the corresponding circuit diagram of the first half cycle is detailed in Fig. 4.3, while the circuit diagrams of the second half cycle is depicted in Fig. 4.4. It is worth mentioning that the dashed lines in the voltages of the SMs and thyristors represent a positive power direction, while the solid ones represent a negative power direction.

The first half cycle illustrations are as follows:

Section *a*:

- Upper operation thyristors are triggered, initiating an overlap state where the DC current flows through both arms of phase 'a'. Currents from phases 'b' and 'c' circulate through the upper and lower arms of phase 'a' (Fig. 4.3(a)).

- Lower SMs of phase ‘a’ generate the phase voltage while the upper SMs maintain the overall leg voltage at V_{dc} because both thyristors are conducting.

Section *b*:

- Lower operation thyristors undergo forced commutation. Lower SMs generate specific voltages based on the direction of arm current flow as in (4.6).
- Upper SMs maintain the output voltage to prevent its distortion from the commutation action.
- Phase ‘a’ current now flows entirely through the upper arm (Fig. 4.3(b)).

Section *c*:

- Phase ‘a’ current flows through the upper arm while the lower arm is inactive (blocked), indicated in Fig. 4.3(c).
- The upper SMs generate phase voltage while the lower SMs maintain voltage at a level ($½V_{dc} + \Delta V$) that ensures the thyristors endure no more than $½V_{dc}$.

The second half cycle illustrations are as follows:

Section *a’*:

- Lower operation thyristors are triggered, initiating another overlap state where DC current flows through both arms.
- Similar to section *a*, currents from phases ‘b’ and ‘c’ circulate through the upper and lower arms of phase ‘a’.
- Upper arm SMs of phase ‘a’ generate phase voltage while the lower SMs maintain the overall leg voltage at V_{dc} because both thyristors are conducting (Fig. 4.3(d)).

Section *b’*:

- Upper thyristors undergo forced commutation.
- Upper SMs generate specific voltages based on the direction of arm current flow as previously illustrated to ensure proper commutation.
- Lower SMs maintain the output voltage waveform integrity.

- Phase ‘a’ current now flows entirely through the lower arm after commutation (Fig. 4.3(e)).

Section *c’*:

- Phase ‘a’ current flows through the lower arm while the upper arm is inactive (blocked) (Fig. 4.3(f)).
- Lower SMs generate the phase voltage while the upper SMs maintain voltage at a level ensuring the thyristors endure no more than $½V_{dc}$.

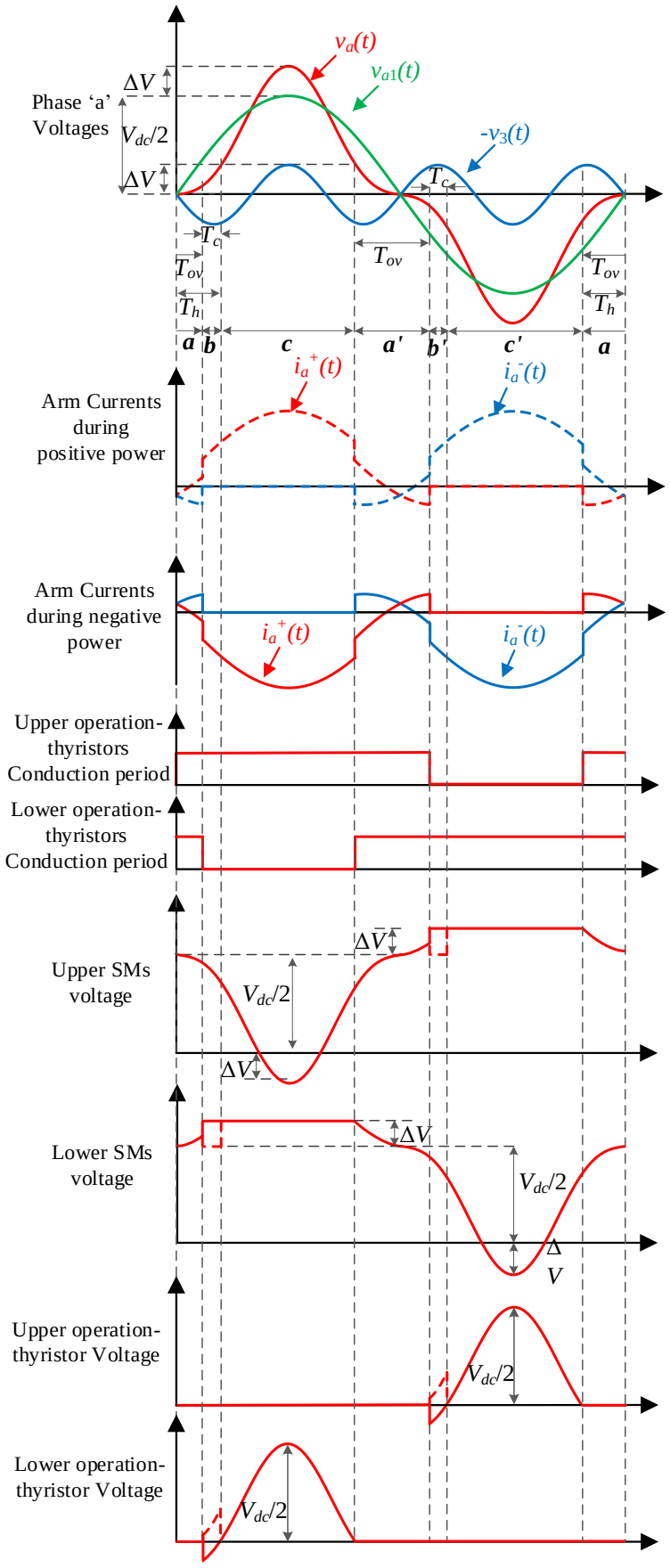


Fig. 4.2. Phase 'a' waveforms including output AC voltages and arm voltages and currents.

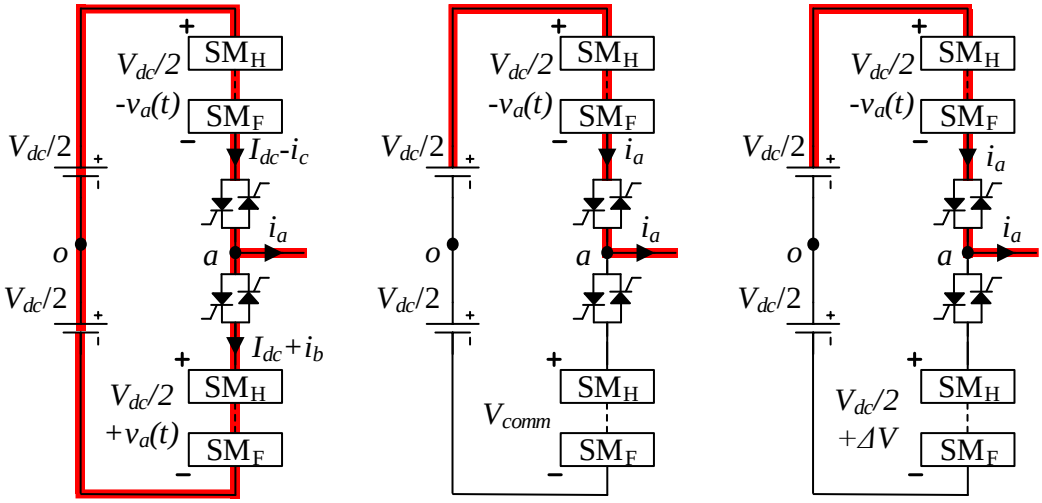


Fig. 4.3. Phase ‘a’ operation illustration (first half cycle): (a) overlap state, (b) lower arm commutation, (c) upper arm conduction.

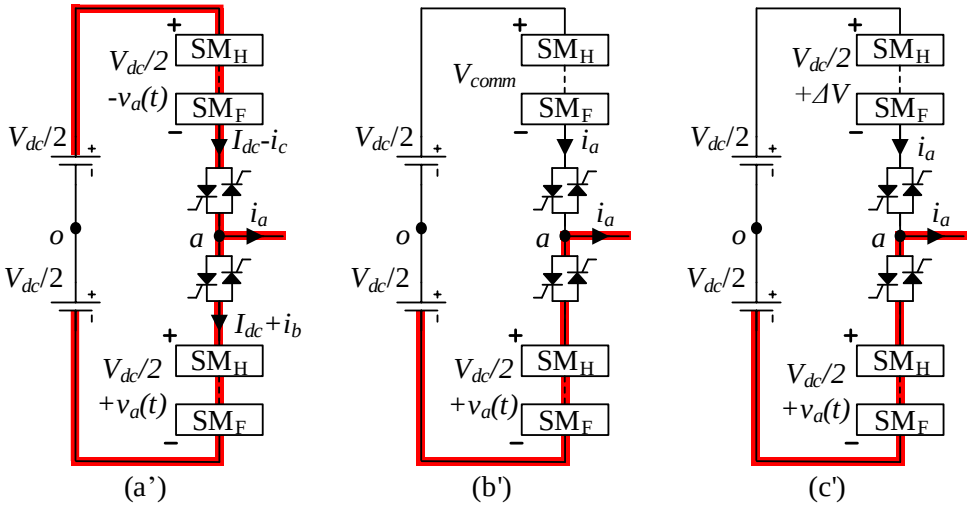


Fig. 4.4. Phase ‘a’ operation illustration (second half cycle): (a’) overlap state, (b’) upper arm commutation, (c’) lower arm conduction.

4. 2 Proposed Topology Controller

The overall block diagram of the proposed topology controller is illustrated in Fig. 4.5. Similar to the controller presented in Chapter 3, the control process begins by defining the reference values for active and reactive power (P^*, Q^*). These references are then used to generate the dq components of the AC currents (i_d^*, i_q^*) through PI controllers. Another set of PI controllers computes the dq components of the fundamental AC voltage, which are subsequently transformed into time-domain voltages using a dq/abc transformation, as shown in Fig. 3.5.

The stack voltage is determined by incorporating the overall AC voltage, including third harmonic subtraction calculated from (4.2), into (4.4) and (4.5) to derive the upper and lower stack voltages. The voltages for the other phases are obtained by shifting the waveforms by -120o and 120o. Once the stack voltage is established, the required number of inserted SMs is calculated using NLC method by dividing the stack voltage by the nominal capacitor voltage V_{cn} and rounding to the nearest integer. A balancing algorithm is then applied to determine which SMs should be activated or deactivated to ensure capacitor voltage balancing. Finally, a pulse generator generates the gating signals required to control the MMC stack IGBTs.

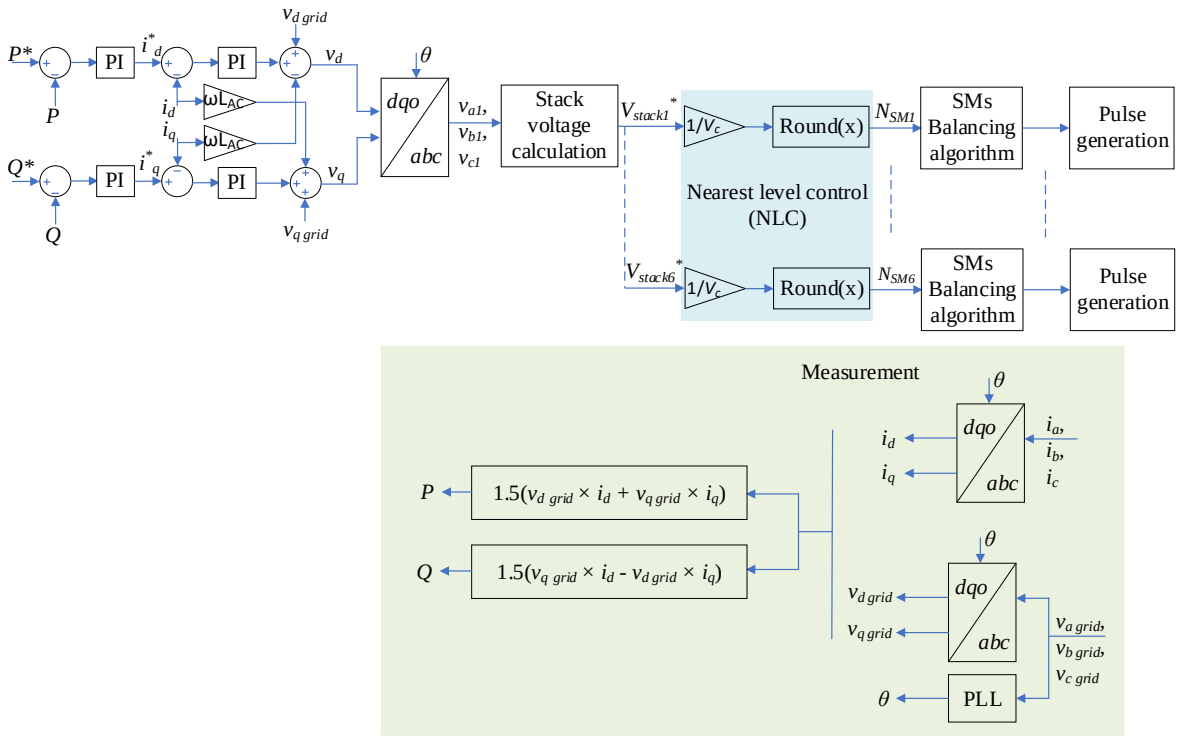


Fig. 4.5. The proposed topology control diagram

4. 3 DC Fault Blocking Capability

The F-HTMC swiftly blocks the DC fault current by completely isolating it from the DC side. An internal path is created using both the protection thyristors and the upper operation thyristors, separating the AC grid component of the DC fault current from the DC side. Subsequently, the AC component is cleared through the commutation of the operation thyristors. Conversely, the DC component of the DC fault current, originating from SM capacitors discharging, is rapidly halted due to the negative voltage capability of the FB-

SMs. To provide a more detailed explanation, the DC fault case is segmented into four sections, labelled ‘a’ to ‘d’, corresponding to the block diagrams depicted in Fig. 4.6.

Section a:

- This section shows the instant of the DC fault occurrence, where it is assumed that leg ‘b’ is in an overlap state.
- The DC fault current is comprised of AC components (generated by the AC grid) marked by red and yellow colours, and a DC component (generated due to SM capacitor discharge) marked by the blue colour as shown in Fig. 4.6(a).

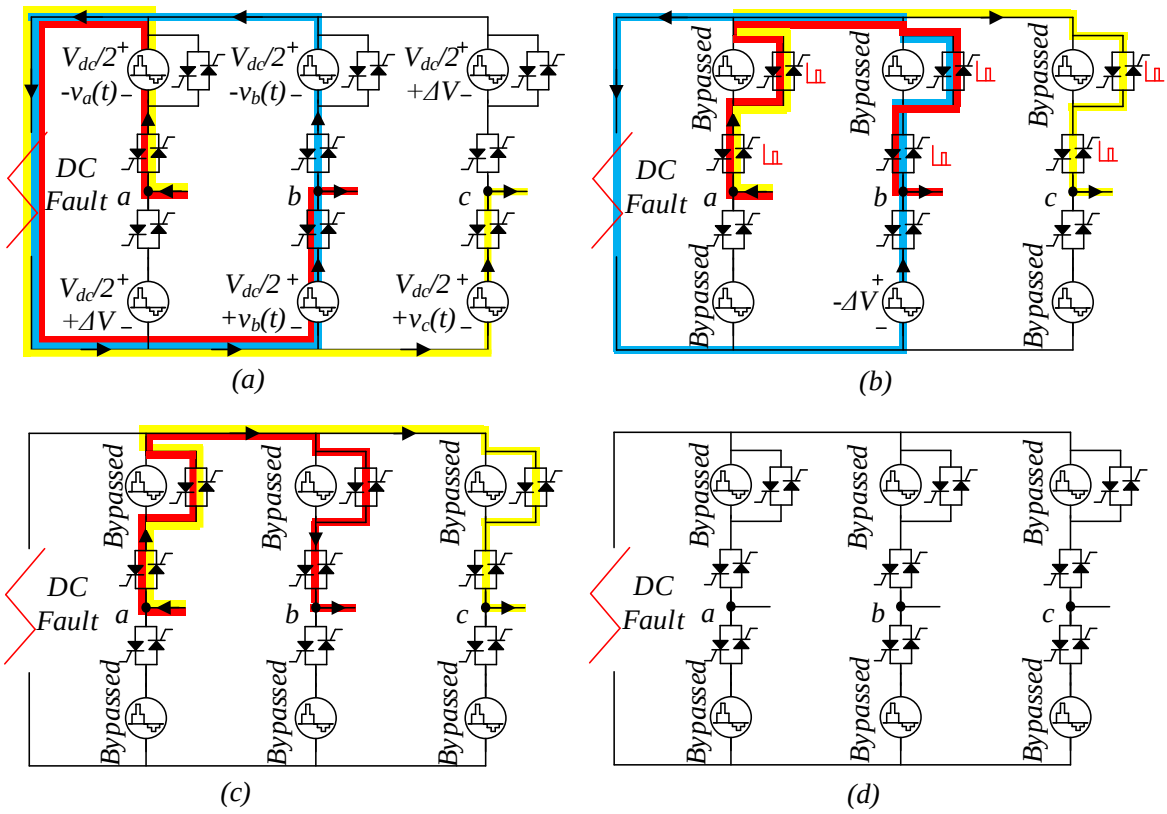


Fig. 4.6. DC fault blocking illustration: (a) DC fault occurrence, (b) DC fault detection, where the fault blocking system is initiated, (c) DC fault has been isolated completely from the DC side, (d) the fault current has been extinguished.

Section b:

- This section shows the instant of fault detection, where the fault blocking system is initiated.

- Both the protection thyristors as well as the upper operation thyristors are triggered to form an internal path for the AC components isolating it from the DC side as depicted in Fig. 4.6(b).
- The FB-SMs in the lower arm of phase 'b' generate their negative voltage ($-\Delta V$) to interrupt the DC component of the fault current.

Section c:

- This section shows the instant where the DC fault is completely isolated from the DC side as shown in Fig. 4.6(c).
- All the SMs are bypassed, and the remaining fault current is extinguished by the upper operation-thyristors commutation.

Section d:

- This section shows the instant where the AC components of the DC fault current are successfully interrupted by the operation-thyristors commutation as depicted in Fig. 4.6(d).
- The operation thyristors endure the AC voltages until the fault is cleared and normal operation is restored, or the AC side is isolated.

4. 4 System Specifications

4.4.1 Third Harmonic Voltage Ratio k_3 and Semiconductor Sizing

To determine the required third harmonic voltage ratio (k_3), several parameters need identification. First, the circuit-commutated turn-off time (t_q) can be extracted from the thyristor's datasheet. Following this, the overall commutation time (T_c) is selected to be greater than the sum of the falling time of the thyristor peak current (T_f) and t_q. Additionally, the overlap time (T_{ov}) needs to be precisely 3.34 ms, equivalent to 60 degrees, to ensure the attainment of a smooth DC current, as previously described. Furthermore, for optimal utilization of the third harmonic waveform in establishing both overlap and commutation times, the phase voltage in equation (3.3) at T_h should match the peak of the third harmonic waveform. This allows the calculation of the zero-sequence ratio as follows:

$$k_3 \geq \frac{\sin \omega T_h}{1 + \sin 3\omega T_h} \tag{4.12}$$

The value of k_3 calculated from (4.12) represents the minimum third harmonic voltage ratio that can achieve the required T_c and T_{ov}. Since the voltage of the FB-SMs per arm depends on k_3 as seen in (3.2) then the number of FB-SMs per arm (n_{FB}) is calculated as follows:

$$n_{FB} = k_3 \frac{V_{dc}}{2V_c} \tag{4.13}$$

where V_{c_n} is the nominal voltage of each SM capacitor. On the other hand, since both HB-SMs and operation thyristors per arm endure $½V_{dc}$, the number of HB-SMs (n_{HB}) and operation-thyristors (n_{OpTh}) per arm is calculated as in (4.14), and (4.15), respectively.

$$n_{HB} = \frac{V_{dc}}{2V_c} \tag{4.14}$$

$$n_{OpTh} = \frac{V_{dc}}{2V_{Thy_n}} \tag{4.15}$$

where, V_{Thy_n} represent the nominal voltage value of each thyristor. Finally, since the protection thyristors per arm endure $½V_{dc} + \Delta V$, the number of the protection thyristors per arm (n_{PrTh}) is calculated as follows:

$$n_{PrTh} = (1 + k_3) \frac{V_{dc}}{2V_{Thy_n}} \tag{4.16}$$

4.4.2 Arm Inductance, L_a

The design of the arm inductance is governed by two primary criteria: firstly, ensuring that during thyristor force commutation, the falling time of the thyristors' peak current is either equal to or less than the previously selected value (T_f). Secondly, it is essential to ensure that the maximum permitted current rate of change of the thyristor, denoted as σ, is not exceeded, a parameter found in the thyristor datasheet. It is important to note that just before the instance of the operation thyristors commutation, both arm thyristors are conducting, resulting in an overlap state where both thyristors voltages are zero. Additionally, since each leg comprises two arm inductors, the voltage per arm inductance is calculated as follows:

$$v_L = \frac{V_{dc} - v_a^+ - v_a^-}{2} \tag{4.17}$$

Substituting by the upper and lower SMs' voltages (4.4) and (4.5) at the commutation section of the lower arm, assuming a positive arm current at the lower arm:

$$v_L = \frac{V_{dc}}{4}\left(\sin \omega t - k_3(1 + \sin 3\omega t)\right) = L_a \frac{di_a^-}{dt} \tag{4.18}$$

Solving the differential equation taking into consideration the worst-case scenario, where the arm current equal to the phase peak current ($\hat{\imath}_{a_1}$) at the beginning of the commutation period ($t = T_h - T_c$). Also, the lower arm current (i_a^-) should be equal to zero at the end of the peak current falling time ($t = T_h - T_c + T_f$). Therefore, the arm inductance value can be designed as follows:

$$\begin{aligned} L_a \leq \frac{V_{dc}}{12\omega\hat{\imath}_{a_1}}\Big(&3\cos\omega\big(T_h - T_c + T_f\big) - 3\cos\omega(T_h - T_c) \\ &+ k_3\big(3\omega\big(T_f\big) - \cos 3\omega(T_h - T_c) \\ &+ \cos 3\omega\big(T_h - T_c + T_f\big)\big)\Big) \end{aligned} \tag{4.19}$$

Also, the arm inductance should limit the arm current rate of change below the maximum allowable value. Therefore, substituting by σ in (4.18) at $t = T_h - T_c$, The arm inductance value should also satisfy the following:

$$L_a > \frac{V_{dc}}{4\,\sigma}\left(\sin\omega(T_h - T_c) - k_3(1 + \sin 3\omega(T_h - T_c))\right) \tag{4.20}$$

4.4.3 SMs Capacitance, C_{HB} and C_{FB}

The capacitance calculation method used is based on the procedure detailed in [65]. However, in this study, instead of calculating the arm energy deviation as per the method described, the energy deviation for the SMs is computed. This distinction is made to differentiate between the behaviour of HB-SMs and FB-SMs. Both types of SMs charge or discharge when generating positive voltage, but only FB-SMs are involved in case of negative voltage generation. The energy deviation per SM in the upper arm ΔE_{SM}^+ is determined by the following equation:

$$\Delta E_{SM}^{+}(t) = \int_{0}^{t} \frac{P_a^{+}(x)}{n_{SM}^{+}(x)} dx \tag{4.21}$$

where P_a^+ represents the power of all the SMs in the upper arm of phase 'a' and n_{SM}^+ refer to the count of operational SMs in the upper arm. The count of operational SMs (n_{SM}^+) depends on the polarity of their voltage (v_a^+) as follows:

$$n_{SM}^{+}(t) = \begin{cases} N_{HB} + N_{FB}\ , & v_a^+(t) > 0 \\ N_{FB}\ , & v_a^+(t) < 0 \end{cases} \tag{4.22}$$

On the other hand, using the SMs voltage and current in (4.4) and (4.7), respectively, P_a^+ is calculated as follows:

$$\begin{aligned} P_a^+ &= v_a^+(t)\, i_a^+(t) \\ &= (½V_{dc} - v_a) \\ &\times \begin{cases} (I_{dc} - i_{c_1}), & -T_h < t < T_h - T_c \\ i_{a_1}, & T_h - T_c < t < ½T_p - T_h \\ (I_{dc} - i_{b_1}), & ½T_p - T_h < t < ½T_p + T_h - T_c \\ 0, & ½T_p + T_h - T_c < t < T_p - T_h \end{cases} \end{aligned} \tag{4.23}$$

The energy deviation of the HB-SM is calculated as follows:

$$\Delta E_{HBSM}^{+}(t) = \frac{1}{n_{HB} + n_{FB}} \times \int_{0}^{t} P_a^{+}(x)dx\,, v_a^{+} > 0 \tag{4.24}$$

Moreover, taking into consideration that $n_{FB} = (N_{HB} + N_{FB})k_3/(1 + k_3)$, the energy deviation of the FB-SMs is calculated as follows:

$$\begin{aligned} \Delta E_{FBSM}^{+}(t) &= \tfrac{1}{(n_{HB}+n_{FB})} \times \\ &\begin{cases} \int_0^t P_a^+(x)dx\ , & v_a^+(t) > 0 \\ \frac{1+k_3}{k_3}\int_0^t P_a^+(x)dx, & v_a^+(t) < 0 \end{cases} \end{aligned} \tag{4.25}$$

Substitute in (4.24) and (3.28) to calculate the peak-to-peak energy deviation ΔE_{SM}^{pp+} at each ϕ from -90^o to 90^o to determine the maximum peak-to-peak energy deviation $\Delta E_{SM_{max}}^{pp+}$ for the HB-SMs and FB-SMs. Finally, from the deduced $\Delta E_{SM_{max}}^{pp+}$, the SM capacitance can be calculated as follows:

$$C_{SM} = \frac{\Delta E_{SM_{max}}^{pp+}}{\Delta V_r^{pp} V_{c_n}^2} \quad (4.26)$$

where ΔV_r^{pp} is the peak-to-peak SM capacitor ripple voltage percentage.

4. 5 Simulation Results Validation

A MATLAB SIMULINK model consisting of 401 levels is constructed to validate the proposed power converter. The model is based on the system proposed in [66] depicted in Fig. 3.9, featuring a rated power of 1 GW and a DC link voltage of ±340 kV. For each SM, a voltage of 1.6 kV is chosen, requiring 200 HB-SMs per arm (operating at half the DC link voltage, as previously discussed). Similar to the previous chapter, to simulate this large number of SMs efficiently while minimizing computational burden and enabling PWM control to capture the charging and discharging behaviour of the SM capacitors, the converter model is implemented using a switching-function approach. This is achieved by utilizing HB-MMC and FB-MMC blocks in MATLAB with switching function mode. Since the overall commutation time (T_c) is the sum of thyristor falling current (T_f) and t_q which is the circuit-commutated turn-off time of the thyristor and can be assumed of approximately 800 μs, it is reasonable to assume T_c as around 1.16 ms, with T_{ov} set to 3.34 ms, resulting in a calculated suitable third harmonic voltage ratio (k_3) of 3.5. Consequently, 70 FB-SMs per arm are required. Substituting these values into equations (4.24) and (3.28), Fig. 4.7 is generated, depicting the relationship between the peak-to-peak energy deviation (ΔE_{SM}^{pp+}) of both HB-SMs and FB-SMs with the power factor angle ϕ. The maximum peak-to-peak energy deviations ($\Delta E_{SM_{max}}^{pp+}$) for the HB-SM and FB-SM are determined to be 5.68 kJ and 7.53 kJ, respectively. Substituting these values into equation (4.26) yields the SM capacitance values for the HB-SM and FB-SM, as 11.1 mF and 14.7 mF, respectively. Additionally, through calculations based on equations (4.19) and (4.20), the arm inductance is established as 7.5 mH. Comprehensive details of all simulation model parameters can be found in Table 4.1. The simulation model is tested under two scenarios: a normal operation scenario to validate bidirectional power flow and a DC fault scenario where the F-HTMC is subjected to a DC fault.

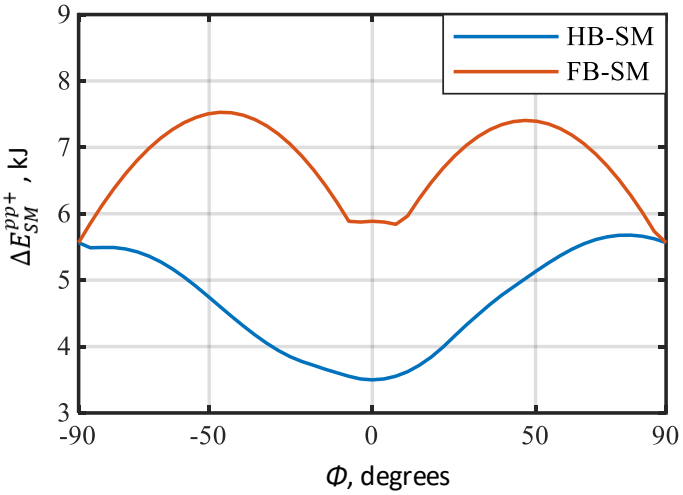


Fig. 4.7. Peak-to-peak energy deviation of the HB-SM and FB-SM against the power factor angle ϕ

Table 4.1 MATLAB Simulation Model Parameters

Parameter	Description	Value
P_r	Rated power	1 GW
V_{dc}	DC link voltage	$\pm$320 kV
v_g	Grid voltage	380 kV
f	Fundamental Frequency	50 Hz
L_{AC}	AC interfacing inductance	68.9 mH
T_c	Overall commutation time	1.16 ms
T_{ov}	Overlap state time	3.34 ms
n_{HB}	Number of HB-SMs	200
n_{FB}	Number of FB-SMs	70
V_c	SM nominal voltage	1.6 kV
C_{HB}	HB-SMs capacitance	11.1 mF
C_{FB}	FB-SMs capacitance	14.7 mF
L_a	Arm inductance	7.5 mH

4.5.1 Normal Operation Scenario

To assess the bidirectional capability of the F-HTMC, the initial test involved a full-rated power flow from the DC side to the AC grid using the proposed F-HTMC. Subsequently, within approximately 0.5 seconds, the power direction was reversed to the full

rated power in the opposite direction. The behaviour of the DC link voltage and current is depicted in Fig. 4.8(a), demonstrating smooth and ripple-free DC link current owing to the previously elucidated 60-degree overlap control strategy. Fig. 4.8(b) displays the active and reactive power of the AC grid, showcasing the maintenance of zero reactive power while the active power reverses from -1 pu to 1 pu. Phase currents are visualised in Fig. 4.8(c), whereas arm currents are detailed in Fig. 4.8(d). It can be inferred that the observed arm currents align with the theoretical assertions presented in Fig. 4.2. Notably, the arm currents exhibit a peak value of 1 pu, signifying the achievement of low current stress. Additionally, Fig. 4.9(a) and (b) illustrate the voltages across the upper SMs and operation thyristors, respectively, both in agreement with the theoretical claims as delineated in Fig. 4.2. Importantly, the operation-thyristor voltages do not surpass 0.5 pu, consistent with earlier statements in this Chapter. Finally, Fig. 4.9(c) and (d) present the voltages of HB-SMs and FB-SMs, respectively, revealing peak-to-peak voltage ripples of less than 0.2 pu, well within permissible limits.

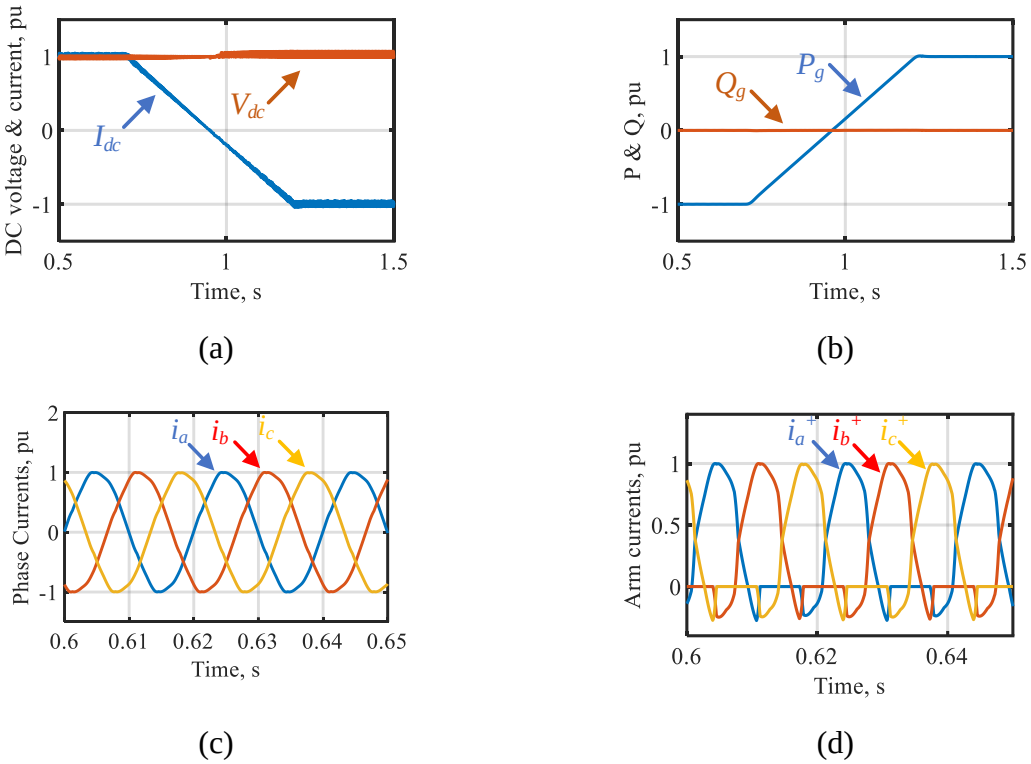


Fig. 4.8 Simulation normal operation scenario: (a) DC link voltage and current, (b) grid active and reactive power, (c) phase currents, and (d) upper arm currents.

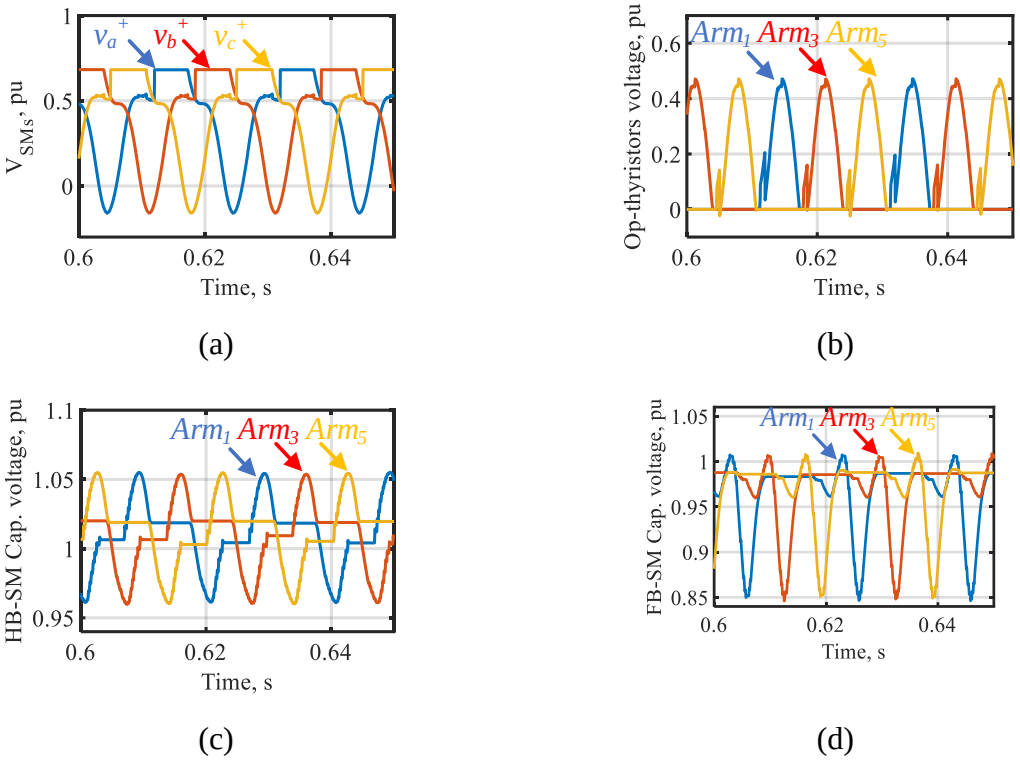


Fig. 4.9 Simulation normal operation scenario cont. (a) HB-SMs capacitor voltages, and (b) FB-SMs capacitor voltages.

4.5.2 DC Fault Scenario

To validate the DC fault blocking capability of the F-HTMC, a simulated DC fault is introduced at 0.5 s into the model. Fig. 4.10(a) illustrates the behaviour of DC voltage and current, wherein the DC voltage collapses immediately upon the fault occurrence, while the DC current starts escalating until the intervention of the FB-SMs in the F-HTMC. Notably, the rapid isolation of the DC fault is evident, achieved in less than 2 ms. Furthermore, it is worth noting that this current is the sum of different arms, thus each arm endure a current of less than 2 pu. Simultaneously, as seen in Fig. 4.10(b), the phase currents increase at the fault instant and then experience interruption by the operation-thyristors, which exhibit slower commutation due to the inherent characteristics of thyristors. Moreover, Fig. 4.10(c) demonstrates that these heightened currents predominantly flow through the upper operation-thyristors and the protection-thyristors. Moreover, Fig. 4.10(d) highlights that solely the DC component of the fault current traverses through the upper SMs, thanks to the presence of the protection-thyristors. Moreover, it can be seen that that the maximum current passing through the SMs is limited to below 2 pu, hence ensuring safe operation during DC fault scenarios.

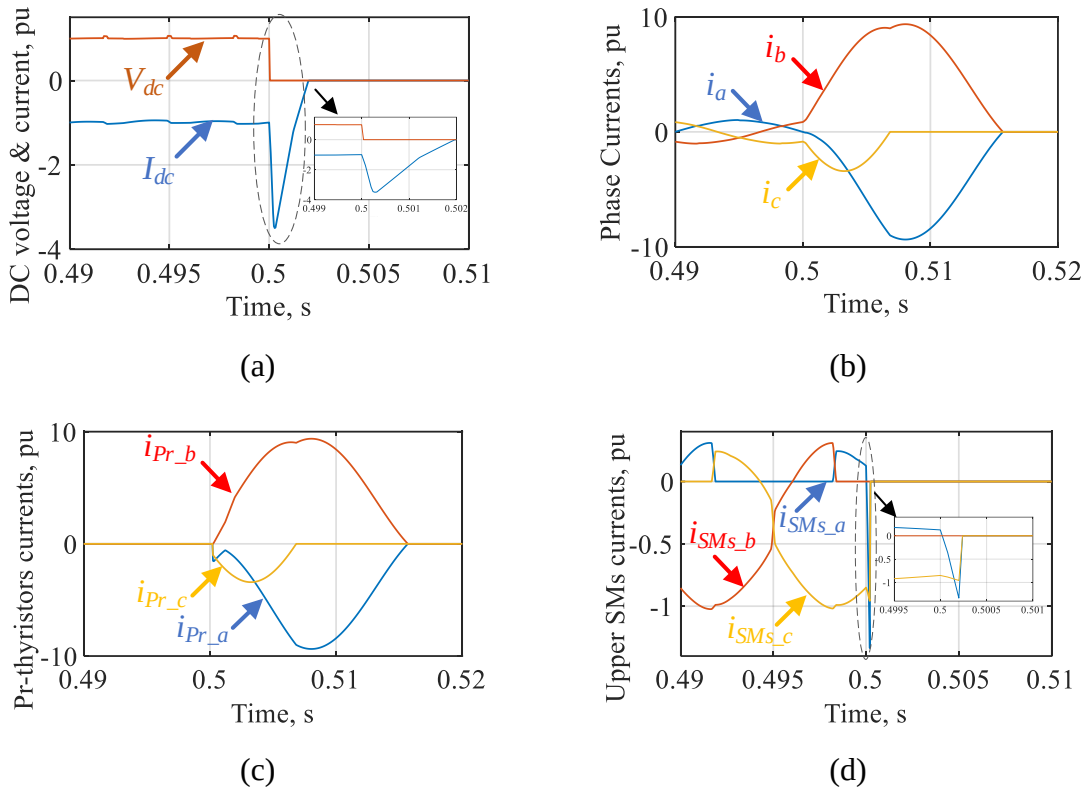


Fig. 4.10 Simulation DC fault scenario: (a) DC link voltage and current, (b) phase currents, (c) protection-thyristors currents, and (d) upper SMs currents.

4. 6 Comparison

To highlight the distinct advantages of the F-HTMC over existing literature, a comparative assessment, based on the 401-level HVDC system, is conducted among the proposed F-HTMC, HTMC [71], and CTB-MMC [33], all equipped with DC fault-blocking capabilities. The summarized comparative results are presented in Table **4.2**. The weight and the volume of each topology involve all the semiconductors, SM capacitors, and DC filters if exist. When compared to the CTB-MMC, the F-HTMC demonstrates either parity or superiority across various comparison aspects. Notably, the F-HTMC exhibits a lower count of IGBTs, reduced total semiconductor losses, and diminished overall weight and volume. Conversely, in comparison with the HTMC, although the F-HTMC incorporates a slightly higher number of IGBTs and losses, it significantly outperforms the HTMC in crucial aspects. Specifically, the F-HTMC achieves markedly lower DC fault clearing times, ensures smoother DC current, and realizes reduced overall weight and volume due to the absence of the DC filter.

As a result, the F-HTMC emerges as the preferred choice, especially in offshore applications due to its substantially lower overall weight and volume. Moreover, it proves advantageous in applications that demand extremely rapid DC fault-clearing times.

Table 4.2 401-level HVDC System Comparison Results

Converter type	CTB-MMC [33]	HTMC [71]	Proposed F-HTMC
SMs No.	400x6	240x6	270x6
IGBTs No.	2x344x6+3x56x6 =5400	4x40x6+2x200x6 =3360	4x70x6+2x200x6 =4080
Thyristors No.	200x6 =1200	2x100x6+40x6+200x6 =2640	2x100x6 +2x135x3 =2010
DC fault-clearing time	<1 ms	15~18 ms	<1 ms
DC filter	No	Yes	No
Smooth DC current	Yes	No	Yes
Total semiconductor loss	8.48 MW 0.848%	5.58 MW 0.558%	6.45 MW 0.645%
Overall weight	155.7 tons	134.9 tons	115.3 tons
Overall volume	161.58 m^3	149.97 m^3	128 m^3

4. 7 Summary

This Chapter introduces the Fast DC Fault-Blocking Thyristor-Based Multilevel Converter (F-HTMC). This HVDC converter utilizes bidirectional thyristors during normal operation to minimize conduction losses. Besides, in DC fault scenarios, parallel branches of bidirectional thyristors are used to rapidly isolate the fault current. The study includes a comprehensive analysis of its normal operation, highlighting the 60-degree overlap time that ensures a smooth DC current. Additionally, illustrations of the DC fault-blocking mechanism demonstrate the isolation and termination of fault currents from the DC side, elucidating the current pathways across the converter arms in each scenario. The Chapter validates its claims through an in-depth 401-level MATLAB Simulink model. Furthermore, a concise comparative assessment was conducted between the proposed F-HTMC and other converters documented in the literature. The findings indicate that the proposed F-HTMC exhibits comparable DC fault clearing time to the CTB, yet surpasses the CTB in various aspects such as lower losses, a reduced number of IGBTs, and decreased weight and volume. Conversely,

while the F-HTMC incurs marginally higher IGBT count and losses compared to the HTMC, it achieves smooth DC current, rapid DC-fault blocking, and reduced volume and weight, rendering it an excellent choice for offshore applications.

Chapter 5

Novel Power Group Thyristor-based Multilevel Converter for Offshore HVDC Power Transmission

In this chapter, a novel power group (PG) thyristor-based modular multilevel converter (PG-TMC) is proposed. This converter employs thyristors in parallel with the submodules (SMs) to form power groups (PGs), along with series-connected thyristor valves. This configuration achieves further reductions in conduction losses compared to previously proposed HVDC converters while maintaining DC fault-blocking capability. Each PG incorporates a hybrid combination of half-bridge submodules (HB-SMs) and full-bridge submodules (FB-SMs). Unlike other architectures, such as PG-FB-MMC, PG-hybrid-MMC, and AT-AAC, where the grid AC voltage during a DC fault is fully absorbed by the FB-SMs, the proposed design distributes the grid AC voltage during DC faults across both the series-connected thyristors and FB-SMs within the PGs. This distribution reduces the required number of FB-SMs, thereby decreasing conduction losses, cost, and the overall size and weight of the system.

5. 1 Proposed Topology Description

5.1.1 Proposed Converter Architecture

The proposed converter architecture is depicted in Fig. 5.1, where each arm consists of a series of connected bidirectional (antiparallel) thyristors, named thyristors-valve, and a series of connected PGs. Each PG consists of a hybrid connection of HB-SMs and FB-SMs, parallel bidirectional thyristors named PG-thyristors, and an inductor. The thyristors-valves function during normal operation to reduce converter conduction losses and in a DC fault scenario in blocking the grid AC voltage with the help of the FB-SMs in the PGs. The PG-thyristors are utilised during normal operation at the instant of PG zero voltage output to further reduce conduction losses. Also, the PG-thyristors are used at the instant of a DC fault to swiftly isolate the fault current from the DC side by creating alternative paths for the current until it is extinguished by thyristor commutation action. All the SMs per arm are named stack, which is used to build up the AC voltage and for thyristors-valve commutation, while the FB-SMs are also used to commutate the PG-thyristors in normal operation and also in blocking the DC-component of the fault current during a DC fault. In post-fault conditions,

the FB-SMs are utilised such that the grid AC voltage is divided across the thyristors-valve and the PGs. Therefore, the FB-SMs should be designed to endure this remaining AC voltage.

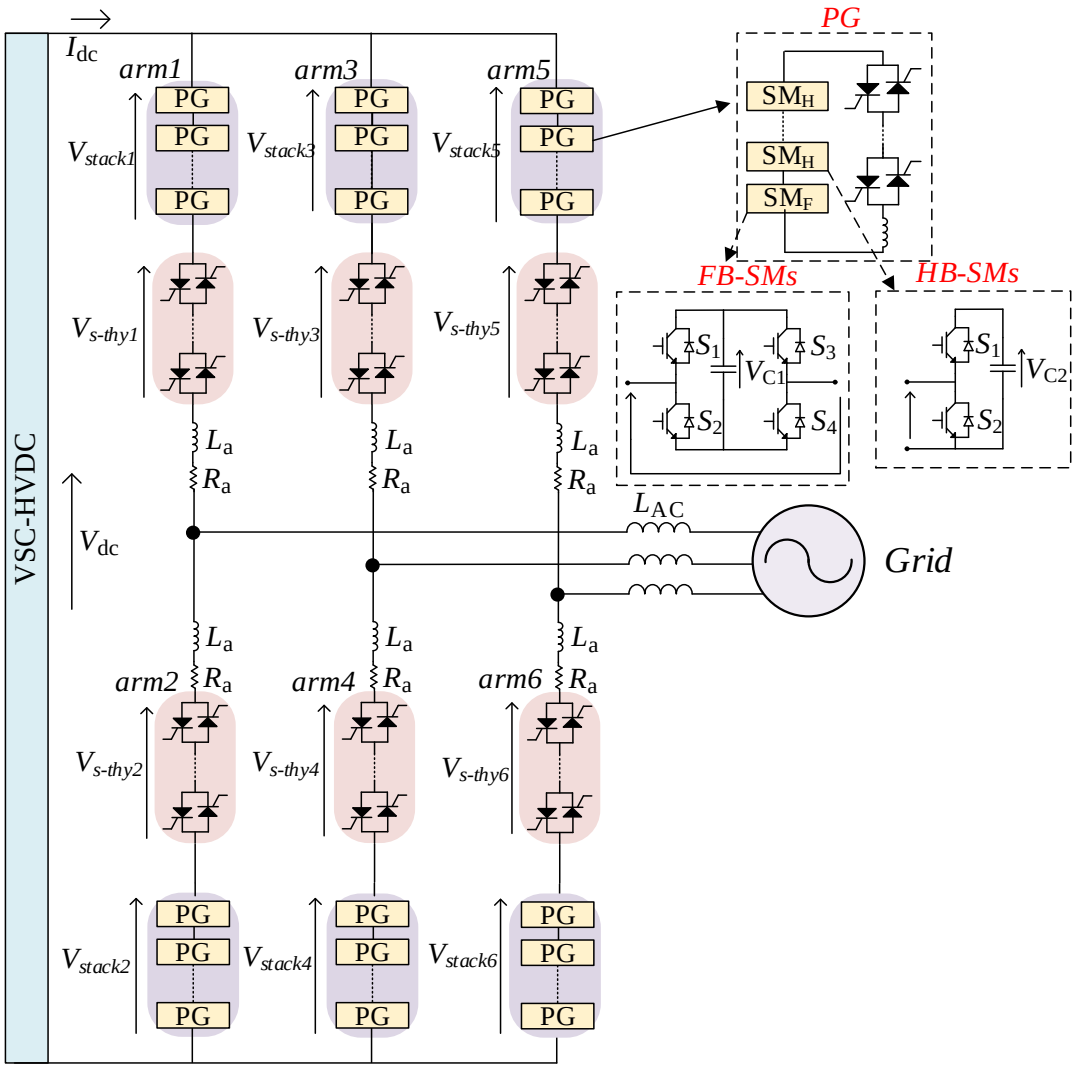


Fig. 5.1. Proposed PG and thyristor-based multilevel converter architecture.

5.1.2 Proposed Converter Operational Analysis (Optimum PG-thyristors Utilisation)

Using only the normal fundamental waveform in the converter arm results in low utilisation of the PG-thyristors since they can only be utilised when maintaining a zero PG voltage output. Therefore, by injecting a normal third harmonic waveform with a ratio of ⅙ the fundamental amplitude, the utilisation of the PG-thyristors can be significantly improved. Additionally, increasing the fundamental AC voltage peak to $k_1 \times ½V_{dc}$ would further enhance PG-thyristor utilisation, as shown in Fig. 5.2, where the stack voltage is close to zero

for most of the conduction period. The optimum value of the fundamental voltage gain, k_1, is discussed in Section VI. Therefore, the fundamental voltage waveform is:

$$v_{a_1}(t) = \hat{v}_{a_1} \sin \omega t = ½k_1 V_{dc} \sin \omega t \tag{5.1}$$

where ω is the angular frequency. The overall phase voltage after injecting the third harmonic waveform is:

$$v_a(t) = ½k_1 V_{dc}(sin\, \omega t + ⅙\, sin\, 3\omega t) \tag{5.2}$$

Since a series thyristors-valve is utilised in the arms of the proposed converter, an overlap period, T_{ov}, should be introduced to achieve a power balance between the upper and lower SMs capacitors. Therefore, the SMs voltage capability should exceed $½V_{dc}$ by ΔV to be able to maintain the leg voltage to V_{dc} for a period of time without distorting the AC waveform. This extra voltage is also used to commutate the thyristors-valve at the end of their conduction period. Therefore, the upper stack voltage (v_{stack_1}) and lower stack voltage (v_{stack_2}) should be calculated as follows:

$$v_{stack_1}(t) = \begin{cases} ½V_{dc} - v_a(t), & -\mathrm{T}_{ov} < t < ½T_p \\ V_{comm_1}, & ½T_p < t < ½T_p + T_c \\ ½V_{dc} + \Delta V, & ½T_p + T_c < t < T_p - T_{ov} \end{cases} \tag{5.3}$$

$$v_{stack_2}(t) = \begin{cases} V_{comm_2}, & 0 < t < T_c \\ ½V_{dc} + \Delta V, & T_c < t < ½T_p - \mathrm{T}_{ov} \\ ½V_{dc} + v_a(t), & ½T_p - T_{ov} < t < T_p \end{cases} \tag{5.4}$$

where T_c represents the overall thyristors-valve commutation time, T_p denotes the periodic time, and V_{comm1}, V_{comm2} signify the commutation voltage utilised to enforce thyristors-valve commutation in the upper and lower arms, respectively. V_{comm} should induce a negative voltage across the thyristors-valve in the case of positive arm current, as depicted in solid lines in Fig. 5.2, while generating a positive voltage across the thyristor-valve in the case of negative arm current, as illustrated in dashed lines in Fig. 5.2. Further details on the commutation voltage are provided in section IV.

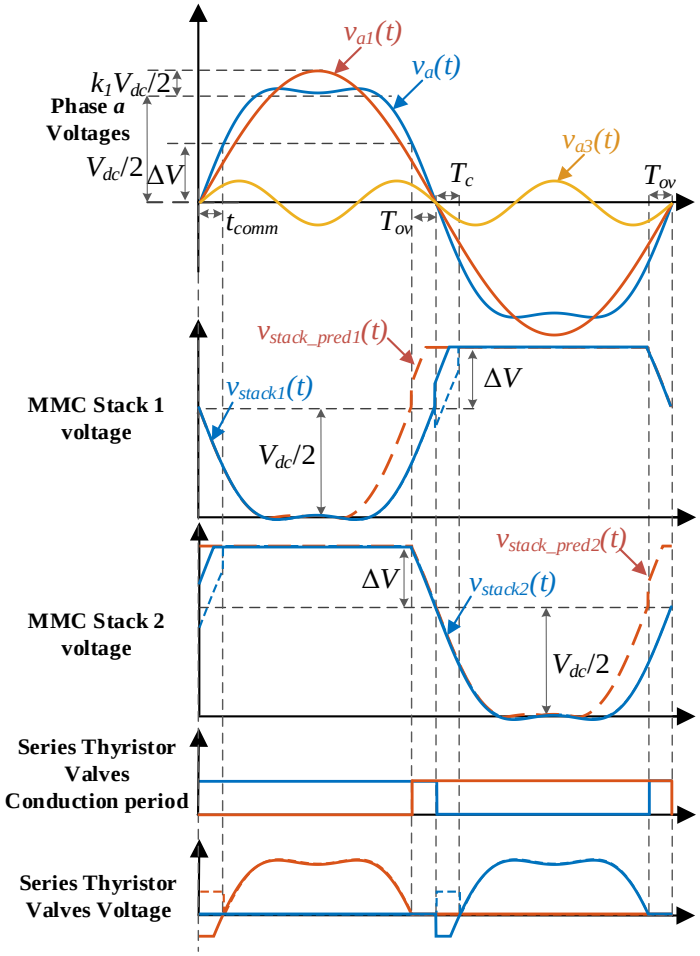


Fig. 5.2. Proposed converter operational analysis.

5.1.3 Actual and Predicted Stack Voltage

The actual stack voltage, v_{stack}, of the upper and lower arms represents the required voltage to generate the required AC voltage, which can be determined by substituting (5.2) into (5.3) and (3.6), respectively. These stack voltages are shown in Fig. 5.2 in blue colour. However, a prediction of the stack voltage ,v_{stack_pred}, is also necessary, as illustrated in Fig. 5.2 in dashed orange colour. This prediction is crucial due to the extended time required for the activation process of the PGs (PG-thyristors turning off) which typically takes around 1ms including the thyristors circuit commutation turn-off time (t_q), which is around 550 µs and the time for the current to drop to zero in the thyristors (T_f). Thus, neglecting the predicted stack voltage could result in distorted output waveforms. In other words, when the SMs in the inactivated PGs are needed to be inserted, a delay would occur until the PGs are activated and ready to generate the required voltage. Therefore, by relying on the predicted stack voltage, the PGs can be primed 1 ms in advance before their SMs are required by the

control algorithm. As depicted in Fig. 5.2 in dashed orange, the predicted stack voltage is only adjusted during the rise of the stack voltage because the PGs need to be activated only in these instances. To generate the predicted stack voltage, a time shift of 1ms is applied to the phase angle of the AC voltage, and then substituted in (5.3) and (3.6). This angle can be extracted using a phase-locked loop (PLL), but only used during the voltage rise of the stack voltage as mentioned.

5. 2 Proposed Converter Control and DC Fault Blocking Mechanism

This section first illustrates the overall proposed operation control algorithm, then details about balancing the PGs, their activation and deactivation techniques, and SM balancing. Lastly, the DC fault-blocking mechanism is discussed.

5.2.1 Overall Operation Control Structure

The overall operation control diagram is depicted in Fig. 5.3. The control begins by considering the reference active and reactive powers using conventional dq control to determine the phase voltage. Subsequently, the actual and predicted stack voltages are extracted, as illustrated in the previous section. v_{stack_pred} passes through the nearest level control (NLC) modulation to determine the equivalent number of predicted inserted SMs ($N_{SM\ pred}$). The PG average capacitor voltages of all PGs ($V_{c\ av\ PG\ i,..m}$) are utilised in the PG-restricted balancing algorithm, which outputs the PG activation signals ($PG_{i,..m}$), determining which PG becomes or remains activated/deactivated. Then the PG activation/deactivation algorithm uses these signals ($PG_{i,..m}$) to generate the $PG_{ready\ i,..m}$ signals (indicating that a PG is ready to generate any required voltage). It also generates PG-thyristors gating signals ($Thy_{PG_{i,..m}}$), $SM_{aux_{i,..n}}$ (SM signals that are used in the PG activation/deactivation process), and $N_{comp_{i,..m}}$ which represents the voltage sign of the used FB-SMs in the activation/deactivation process and is utilised during the actual stack voltage generation for compensation.

The actual stack voltage is used to determine the required number of inserted SMs (N_{SMs}), which is then subtracted by $\sum N_{comp_{i,..m}}$ to generate the compensated number of inserted SMs ($N_{SMs_{comp}}$). Finally, an SM balancing algorithm is utilised to generate the required main SMs signals (used in generating the actual required stack voltage). Then, both main and auxiliary SMs signals are used to generate suitable pulses for the IGBTs of the

corresponding SMs. The total number of PGs per arm is m, while n refers to the total number of SMs per arm. i_{arm} represents the arm current and $V_{c\,i}$ refers to the i^{th} SM capacitor voltage.

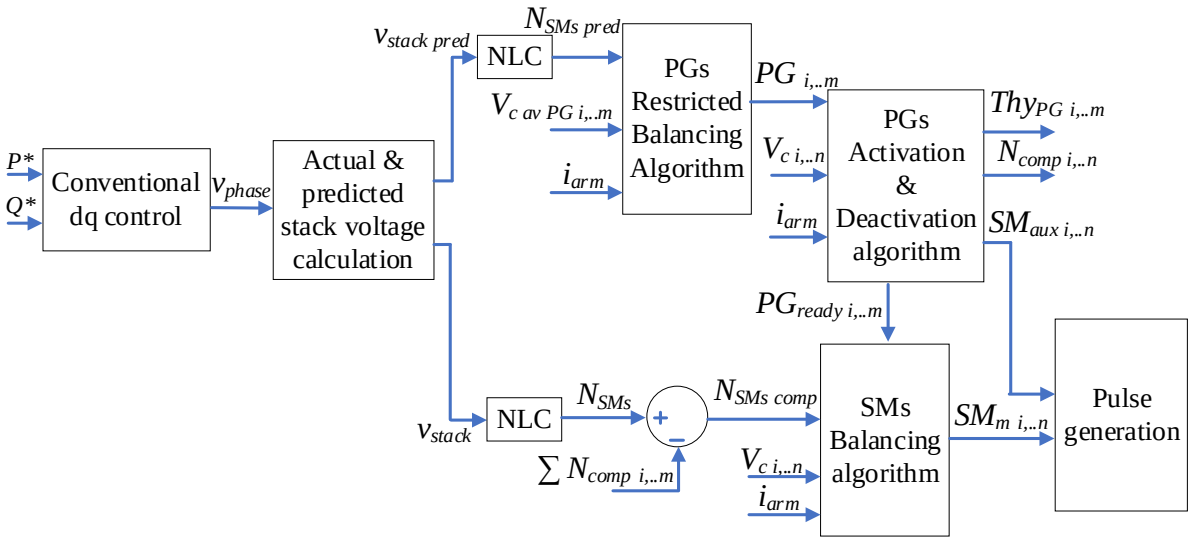


Fig. 5.3. The proposed overall operation control algorithm, where n is the total number of SMs/arm and m is the total number of PGs/arms.

5.2.2 PGs Restricted Balancing Algorithm

The PG balancing algorithm is termed 'restricted' because it does not replace any already activated PGs, even if replacing them could achieve better balancing. This restriction is due to the lengthy process of PG activation, as mentioned, hence maximising the utilisation of the PG-thyristors. Consequently, activation only occurs if the number of required PGs increases. The PG restricted balancing algorithm flow chart is depicted in Fig. 5.4, where the algorithm begins by calculating the number of activated PGs (N_{PG}), depending on the polarity of $N_{SMs\ pred}$ as in (5.5).

$$N_{PG} = k_{PG} \times \begin{cases} ceil\left(\dfrac{N_{SMs\ pred}}{n_{SM\ PG}}\right), & N_{SMs\ pred} \geq 0 \\ ceil\left(\dfrac{N_{SMs\ pred}}{n_{FB\ PG}}\right), & N_{SMs\ pred} < 0 \end{cases} \tag{5.5}$$

where $n_{SM\ PG}$, $n_{FB\ PG}$ are the total number of SMs or FB-SMs per PG, respectively, and k_{PG} is the PG gain, representing the ratio of the number of activated PGs to the minimum required number of PGs. Setting k_{PG} to 1 ensures converter operation without AC voltage distortion using the minimum activated PGs. Further increase of k_{PG} results in higher conduction losses

but reduces the required SM capacitance. Subsequently, depending on the change in the number of activated PGs (ΔN_{PG}), the algorithm proceeds. If ΔN_{PG} is positive (indicating an increase in the number of activated PGs), the algorithm sorts only the deactivated PGs and activates a number of PGs equal to ΔN_{PG}. Conversely, if ΔN_{PG} is negative, the algorithm sorts only the activated PGs and deactivates a number of PGs equal to ΔN_{PG}.

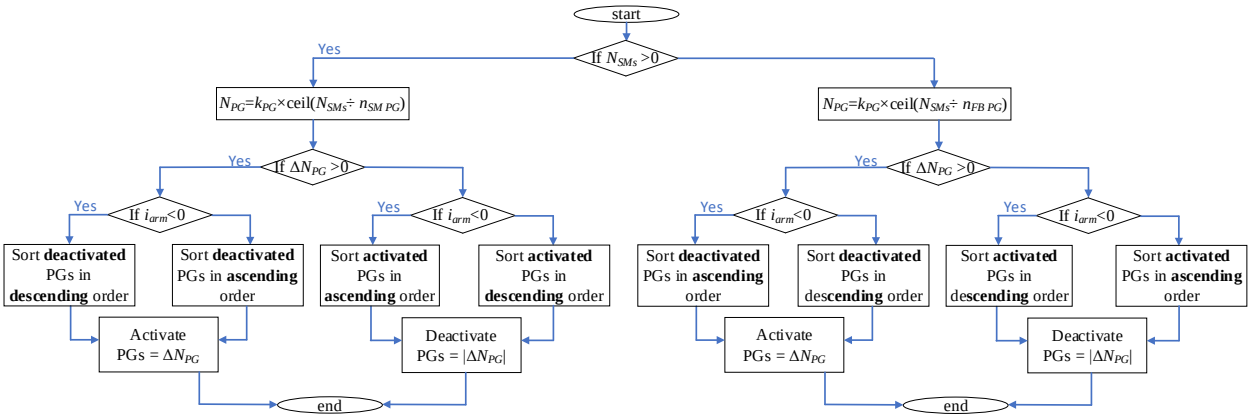


Fig. 5.4. The PGs restricted balancing algorithm.

5.2.3 PG Activation and Deactivation Algorithm

The activation and deactivation of the PGs are based on the method presented in [37], with modifications introduced to enhance control performance. Conventionally, the voltage difference between two FB-SMs is utilised instead of the total SM voltage to turn off the PG-thyristors, reducing their turn-off losses. However, a voltage difference of 200V must be maintained between these two FB-SMs which introduces a delay before turning on the PG-thyristors. Therefore, this Chapter suggests a new method to significantly decrease this delay. Assuming 4 FB-SMs per PG, the SMs balancing algorithm maintains two FB-SMs at nominal capacitor voltage (V_{c_n}) +50V (named FB-SMs$_{max}$), while the other two FB-SMs are maintained at V_{c_n}-50V (named FB-SMs$_{min}$) during normal operation. Consequently, at turning off the PG-thyristors, the voltage difference between FB-SMs$_{max}$ and FB-SMs$_{min}$ is utilised without the need for recharging or discharging before turning on the PG-thyristors. Using this approach further increases PG-thyristor utilisation.

The PG activation and deactivation algorithm flow chart is presented in Fig. 5.5 where initially the algorithm checks the change in the PG activation signals (ΔPG_i). If ΔPG_i = 1 (indicating that the PG is just activated), the activation algorithm begins by terminating the PG-thyristors gating of this particular PG. The algorithm uses the voltage difference between

FB-SMs$_{max}$ and FB-SMs$_{min}$ to introduce a reverse voltage on the PG-thyristors only until the PG-thyristors current is reduced to zero. Low voltage is used at this stage to significantly reduce turn-off losses. Then, the algorithm inserts the whole SM voltage to maintain a reverse voltage on the PG-thyristors for t_q, where N_{comp_i} is set accordingly to prevent any distortion of the arm voltage during this stage. After t_q, the algorithm bypasses all the SMs within the PG and sets N_{comp_i} back to 0, indicating that this PG is ready to generate any required voltage. Conversely, if ΔPG_i = -1 (indicating that the PG is just deactivated), the deactivation algorithm starts by setting the ready PG signal to zero. Then, the algorithm makes sure that the FB-SMs difference is greater than or equal to 200 V before turning on the thyristors. The delay here is insignificant because the difference between them should be already maintained at 200 V by the SMs balancing algorithm. Then, the algorithm initiates the turn-on process of the PG-thyristors by blocking the FB-SMs$_{max}$ and inserting the FB-SMs$_{min}$ to prevent any current discharge through the PG-thyristors. Finally, the gating signals are sent to the PG-thyristors.

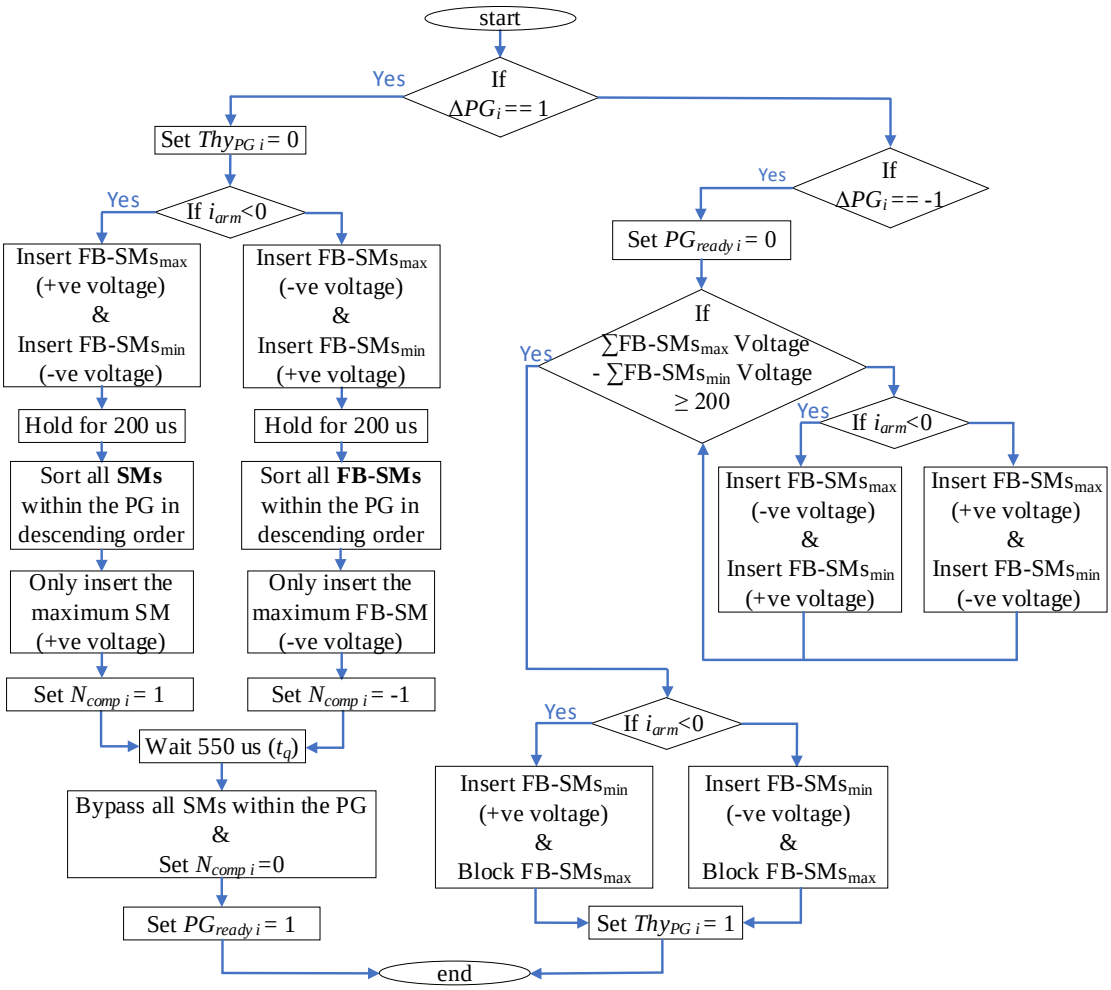


Fig. 5.5. The PGs activation and deactivation algorithm.

5.2.4 SMs Balancing Algorithm

The SMs balancing algorithm flow chart is presented in Fig. 5.6, noting that the algorithm only sorts the SMs in the activated PGs. It sorts only FB-SMs if the required number of SMs has a negative value. During normal operation, the FB-SMs$_{max}$ are maintained at V_{c_n}+ 50 V, while the FB-SMs$_{min}$ are maintained at V_{c_n}- 50 V, as illustrated in section C.

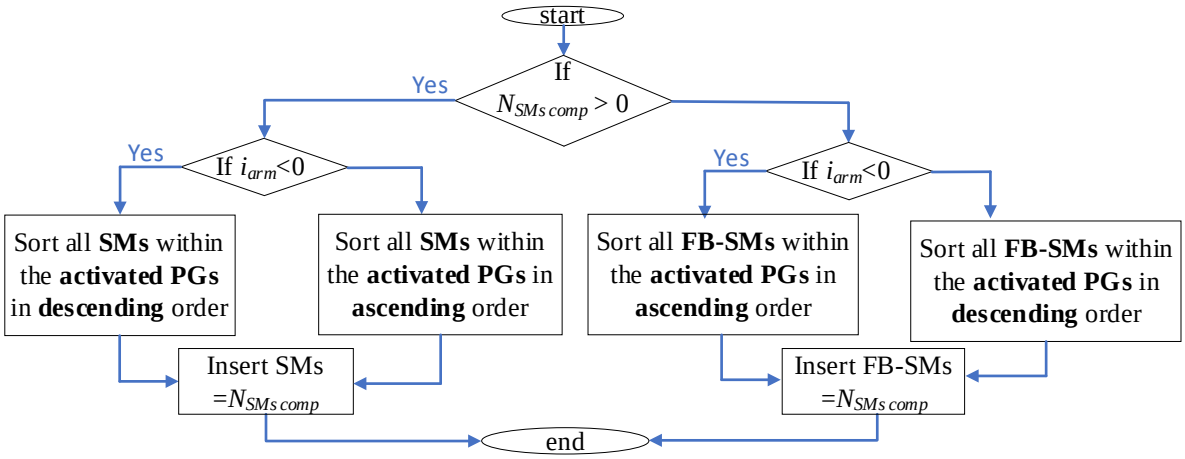


Fig. 5.6. The SMs balancing algorithm.

5.2.5 DC Fault Blocking Mechanism

a) Fault blocking method

The DC fault-blocking mechanism is illustrated in the two diagrams shown in Fig. 5.7, where the instant of the DC fault occurrence is shown in Fig. 5.7(a). The fault current is divided into DC and AC components. The DC component is generated from the capacitor discharge through the overlapped arms, specifically leg 'b' in this example, as indicated by the blue lines. The AC fault component is generated from the AC grid through the arms of the converter feeding the fault as shown by the red lines. At the instant of fault detection, the HB-SMs are bypassed, while the FB-SMs are blocked in the upper arms and in the overlapped arms. The FB-SMs in the blocking state rapidly block the DC fault component generated in the overlapped arms. Additionally, a firing pulse is sent to all the upper thyristors, including both the thyristors-valve and PG-thyristors, as depicted in Fig. 5.7(b). This bypasses the AC fault component through the upper thyristors, isolating the DC side from the fault. Finally, the fault is completely terminated by the thyristor commutation action. After the fault current is cleared in each arm, the FB-SMs should be controlled to ensure that the AC grid voltage is divided conveniently between the thyristors-valve and the PGs of each arm.

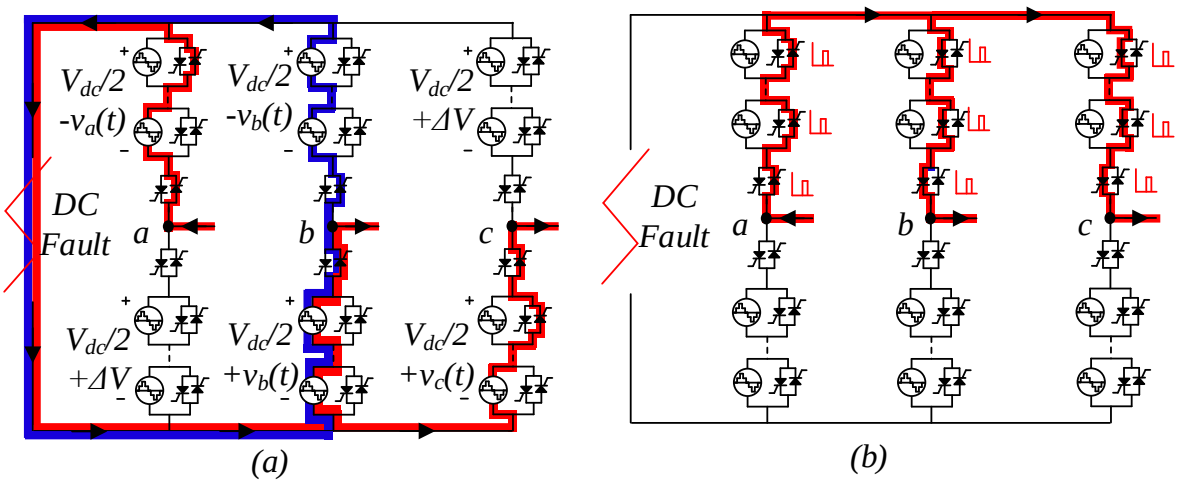


Fig. 5.7. DC fault blocking mechanism diagram: (a) instant of fault occurrence and (b) DC fault termination actions.

b) DC fault interruption time vs transmission line distance

Since only the DC component of the fault current flows through the transmission line until it is blocked by the FB-SMs, whereas the AC component circulates through the thyristors, the transmission line length only affects the DC component, as shown in Fig. 5.8.

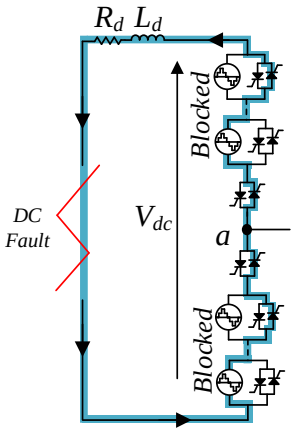


Fig. 5.8. The DC component of the fault current during a DC short circuit fault.

At the moment of fault detection (assuming i_{dc}=2 pu), the DC voltage is determined as follows:

$$V_{dc}(t) = -\left[(n_{FB-op})V_c * + \frac{n_{FB-op}}{3C}\int_{t1}^{t} i_{dc}(t)dt\right] \qquad \text{(X6)}$$

$$V_{dc}(t) = \frac{L_d di_{dc}(t)}{dt} + R_d i_{dc}(t) \tag{X7}$$

where n_{FB-op} is the number of operational FB-SMs per overlapped leg at fault detection, V_c is the capacitor voltage, C_{SM} = SM capacitance, t_1 is time of fault detection, L_d and R_d = DC line inductance and resistance.

During the overlap period, the minimum number of n_{FB-op} should be calculated where, the DC current after fault detection follows:

$$i_{dc}(t) = e^{\alpha(t-t_1)}\big(C_1 cos\beta(t-t_1) + C_2 sin\beta(t-t_1)\big) \tag{X8}$$

where the constants are:

$$\alpha = -\frac{R_d}{2L_d} \tag{X9}$$

$$\beta = \frac{1}{2}\sqrt{\frac{4n_{FB-op}}{3CL_d} - \left(\frac{R_d}{L_d}\right)^2} \tag{X10}$$

$$C_1 = i_{dc}(t_1) \tag{X11}$$

$$C_2 = -\frac{n_{FB-op}V_c}{2\beta L_d} + \frac{\alpha C_1}{\beta} \tag{X12}$$

By solving (X8), the DC fault interruption time at different fault distances is determined, ranging from 0 km (directly at the converter terminals after the filtering inductance) to 100 km of transmission lines. The results, presented in Fig. 5.9, show that the interruption time is approximately 0.5 ms for a fault occurring at the converter terminal and around 2 ms at a distance of 100 km. These results are based on the simulation parameters in section 5.5 and confirm that the fault interruption remains fast even at long distances due to the negative voltage injection capability of the FB-SMs in each arm.

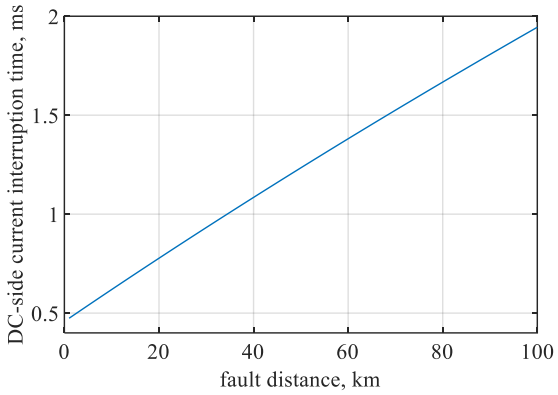


Fig. 5.9. The DC-side current interruption time against the fault distance.

5. 3 System Design

This section illustrates the design procedures of the proposed converter parameters. Assuming that v_{stack} is rated to $½V_{dc}$, then the overlap between the upper and lower arms cannot be maintained except at the instant of zero output voltage. In addition, there is no commutation capability in this case. Therefore, to achieve a suitable overlap time (T_{ov}), which should be around 1ms, assuming equal timings between the overlap and the overall commutation time (T_c), the maximum stack voltage capability ($\hat{v}_{stack}$) should be designed to be equal to $½V_{dc} + \Delta V$ where $\Delta V = v_a(T_{ov})$ as follows:

$$\hat{v}_{stack} = ½V_{dc}\left(1 + k_1(sin\,\omega T_{ov} + ⅙\,sin\,3\omega T_{ov})\right) \tag{5.13}$$

5.3.1 PGs and series thyristors-valve Design

The number of SMs and bidirectional thyristors per PG are based on [37], realising 8 SMs in parallel with 3 bidirectional thyristors per PG. However, here hybrid SMs are used in each PG instead of just FB-SMs to reduce the conduction losses and cost significantly while maintaining DC fault blocking capability due to the usage series thyristors-valve. The total number of PGs per arm (m) can be determined by:

$$m = ceil\left(\frac{\hat{v}_{stack}}{\hat{v}_{PG}}\right) \tag{5.14}$$

where $\hat{v}_{PG}$ is the maximum voltage capability of each PG. Also, after determining the suitable m, the true maximum stack voltage ($\hat{v}_{stack}$) is calculated as $\hat{v}_{PG} \times m$. The voltage of the series thyristors-valve ($v_{thy\ valve}$) can be calculated as in (5.15), which is only valid during the thyristors-valve blocking state.

$$v_{thy\ valve}(t) = V_{dc} - (v_{stack_1}(t) + v_{stack_2}(t)) \quad (5.15)$$

Therefore, the maximum voltage capability of the series thyristors-valve ($\hat{v}_{thy\ valve}$) is determined by:

$$\hat{v}_{thy\ valve} = V_{dc} - \hat{v}_{stack} \quad (5.16)$$

Thus, the number of bidirectional thyristors per thyristors-valve ($n_{thy\ valve}$) is calculated from:

$$n_{thy\ valve} = \frac{\hat{v}_{thy\ valve}}{V_{thy_n}} \quad (5.17)$$

where V_{thy_n} is the nominal voltage of each bidirectional thyristor. In order for the arm to be able to block the AC voltage during a DC fault, each arm of the converter should be able to block the AC phase voltage peak using the series thyristors-valve and FB-SMs. Therefore, the total number of FB-SMs per arm (n_{FB}) is:

$$n_{FB} \geq \frac{\hat{v}_{a_1} - \hat{v}_{thy\ valve}}{V_{c_n}} \quad (5.18)$$

n_{FB} should be selected so that the number is divided evenly among all the PGs while also satisfy (5.18). Therefore, the total number of FB-SMs per PG ($n_{FB\ PG}$) is calculated from:

$$n_{FB\ PG} = ceil\left(\frac{n_{FB}}{m}\right) \quad (5.19)$$

Finally, the total number of HB-SMs per PG ($n_{HB\ PG}$) is calculated by subtracting the total number of SMs per PG $n_{SM\ PG}$ from $n_{FB\ PG}$ as $n_{HB\ PG} = n_{SM\ PG} - n_{FB\ PG}$.

5.3.2 SMs capacitor Design

The SM capacitance is determined to endure the maximum peak-to-peak arm energy deviation without exceeding the maximum permissible capacitor voltage ripple, as illustrated in [65]. But since PGs are used with the proposed optimum balancing algorithm, only the SMs within the activated PGs should be involved in the energy deviation calculations at each instant:

$$\Delta E_{SM}(t) = \int \frac{P_{stack}(t)}{n_{avail}(t)} dt \quad (5.20)$$

where P_{stack} is the SMs stack power and n_{avail} is the number of available SMs (the total number of SMs in the activated PGs). n_{avail} is calculated depending on the number of activated PGs (N_{PG}) multiplied by the total number of SMs per PG ($n_{SM\ PG}$) in case of positive stack voltage or multiplied by the total number of FB-SMs per PG ($n_{FB\ PG}$) in case of negative stack voltage as follows:

$$n_{avail}(t) = N_{PG}(t) \times \begin{cases} n_{SM\ PG}, & v_{stack}(t) \geq 0 \\ n_{FB\ PG}, & v_{stack}(t) < 0 \end{cases} \quad (5.21)$$

where N_{PG} is determined according to (5.5), where the number of inserted SMs (N_{SM}) can be calculated by dividing the stack voltage ($v_{stack}(t)$) by the SM nominal voltage V_{c_n}. Taking into consideration that the stack current is equal to the AC current during the stack conduction period, neglecting the commutation period, the stack power is calculated as:

$$P_{stack}(t) = v_{stack} i_{stack} = ⅔|\bar{S}|H(t) \quad (5.22)$$

where $H(t)$ is defined by:

$$H(t) = \left(\frac{1}{k_1} - sin\,\omega t - ⅙\ sin\,3\omega t\right) \sin(\omega t + \phi) \quad (5.23)$$

where ϕ is the phase shift between the fundamental AC voltage and current. Also, $\bar{S}$ is the apparent power and calculated by:

$$|\bar{S}| = \frac{3}{2} \hat{v}_{a_1} \hat{\imath}_{a_1} \quad (5.24)$$

where $\hat{v}_{a_1}, \hat{\imath}_{a_1}$ are the peak fundamental phase voltage and current, respectively. Substituting (5.23) and (5.22) in (5.20), the final energy deviation equation is obtained. The integration is valid from the beginning of the conduction period of the stack until the beginning of the overlap period, because in the overlap period, the capacitor voltages naturally return to their nominal values. The maximum energy deviation per SM should be calculated for all range of ϕ [-π to π], where the capacitance design is based on the absolute maximum energy deviation per SM ($\Delta E^{pp}_{SM_{max}}$). It can be shown from (5.23) that $\Delta E^{pp}_{SM_{max}}$ depends on the variable k_1. Calculating $\Delta E^{pp}_{SM_{max}}$ for the range of k_1 from 1.15 to 1.2, the optimum k_1 is selected to achieve the minimum $\Delta E^{pp}_{SM_{max}}$. Selecting the optimum k_1 will inherently achieves maximum PG-thyristor utilisation. Finally, the capacitance is calculated according to:

$$C_{SM} = \frac{\Delta E_{SM_{max}}^{pp}}{\Delta V_r^{PP} V_{c_n}^2} \tag{5.25}$$

where ΔV_r^{pp} is the required peak-to-peak capacitor voltage ripple.

5.3.3 Inductor Design

The proposed converter comprises two inductors: the PG inductor (L_{PG}) and the arm inductor (L_a). The PG inductor (L_{PG}) should be designed to be large enough to limit the rate of change of current (di/dt) to a value below the maximum capability of the thyristor (σ), as specified in the datasheet, during the turning on/off process of the PG-thyristors. The rate of change of current is calculated as follows:

$$\frac{di}{dt} = \frac{V_{L_{PG}}}{L_{PG}} < \sigma \tag{5.26}$$

where $V_{L_{PG}}$ is the voltage used to turn on/off the PG-thyristors. Therefore, L_{PG} should be designed to be larger than $V_{L_{PG}}/\sigma$. As previously illustrated, $V_{L_{PG}}$ is the mismatch voltage between the FB-SMs, which is a small value of around 200 V, resulting in a very small inductance in the range of micro Henries. Hence, using multiple L_{PG} in the same arm will not affect the performance of the MMC arm. On the other hand, the arm inductor L_a should be selected small enough to allow for balancing the deviation between the converter leg voltage and the DC link voltage within the overlap period (T_{ov}). Applying KVL to the first leg of Fig. 4.1, neglecting the arm resistance:

$$v_{stack_1} + v_{stack_2} + 2v_L - V_{dc} = 0 \tag{5.27}$$

For simplicity, it is assumed that both stack voltages generate a constant voltage at $½V_{dc}$ with a 10% increased voltage in the upper stack. Hence, the following equation can be derived:

$$\frac{2}{C_{stack}} \int i_{circ}\, dt + 2L_a \frac{di_{circ}}{dt} = -0.05V_{dc} \tag{5.28}$$

where C_{stack} is the stack capacitance equivalent to $½V_{dc}$, and i_{circ} is the circulating current that occurs due to the voltage deviation between the converter leg (both upper and lower stacks) and DC link voltage. The circulating current equation can be calculated by solving (5.28) while assuming zero circulating current at the beginning of the overlap period.

Assuming that the converter leg capacitors discharge by the voltage mismatch during the overlap period:

$$\frac{2}{C_{stack}}\int_0^{t_{ov}} i_{circ}\,dt = -0.05V_{dc} \tag{5.29}$$

Substituting the determined circulating current equation into (5.29), the arm inductance is:

$$L_a \leq \frac{4}{\pi^2 C_{stack}} t_{ov}^2 \tag{5.30}$$

Selecting the arm inductance near the value calculated from (5.30) will inherently be high enough to limit rate of change of current to below the thyristor maximum di/dt capability.

5.3.4 Commutation Voltage (V_{comm}) Design

The design of the commutation voltage V_{comm} aims to decrease the thyristors-valve current from its peak value to zero within a predetermined time known as the current falling time T_f. For this analysis, the stack capacitance deviation can be neglected, hence the stack voltage is assumed to behave as a variable voltage source rather than variable capacitance. Substituting (5.3) and (3.6) into (5.27) while assuming the instant of thyristors-valve commutation of the lower arm with positive arm current, then the arm inductance voltage can be calculated from:

$$v_{La} = L_a\frac{di}{dt} = ½\left(½V_{dc} + v_a(t) - V_{comm_2}\right) = -V_{thy_{comm}} \tag{5.31}$$

where $V_{thy_{comm}}$ represents the voltage induced on the arm inductance to decrease the arm current in the thyristors-valve to zero during T_f. Assuming $V_{thy_{comm}}$ is a constant value, and assuming the arm current is at its peak value ($\hat{\imath}_{arm}$) at the instant of the thyristors-valve commutation, the minimum $V_{thy_{comm}}$ can be calculated as follows:

$$V_{thy_{comm}} \geq \frac{L_a\hat{\imath}_{arm}}{T_f} \tag{5.32}$$

Finally, substituting (5.32) into (5.31), V_{comm_2} can be calculated. Similarly, the commutation voltage of the upper arm can be calculated using the same procedure. It is found that using the same magnitude of $V_{thy_{comm}}$ with opposite sign works well in the case of negative arm

currents. Therefore, the final formula for the commutation voltage in the upper and lower stacks are:

$$V_{comm_1} = \begin{cases} ½V_{dc} + 2V_{thy_{comm}} - v_a(t), & i_{arm} \geq 0 \\ ½V_{dc} - 2V_{thy_{comm}} - v_a(t), & i_{arm} < 0 \end{cases} \quad (5.33)$$

$$V_{comm_2} = \begin{cases} ½V_{dc} + 2V_{thy_{comm}} + v_a(t), & i_{arm} \geq 0 \\ ½V_{dc} - 2V_{thy_{comm}} + v_a(t), & i_{arm} < 0 \end{cases} \quad (5.34)$$

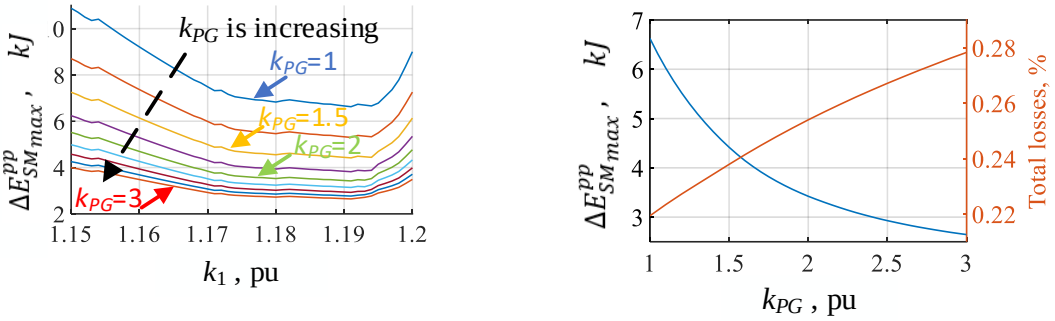
Note that the commutation voltages are limited to the stack maximum voltage. However, it will not pose an issue because after T_f, the priority is to maintain positive/negative voltage, depending on the arm current, until t_q is passed without concern about the magnitude.

5. 4 Case Study

A case study is now presented to provide a comprehensive explanation and practical implementation of the design procedures previously outlined. Initially, several assumptions are established for a 900 MW rated power system with ±300 kV DC link voltage. The PG configuration is assumed to be consistent with that described in [37], where each PG comprises 8 SMs and 3 parallel bidirectional thyristors, with each PG rated at 14.4 kV (each SM rated at 1.8 kV and each thyristor rated at 4.8 kV).

The total number of PGs per arm is calculated using (5.13) in (5.14), yielding 32 PGs. Consequently, the actual maximum stack voltage is determined to be 32×14.4 kV, resulting in 460.8 kV. The number of bidirectional thyristors per thyristor-valve ($n_{thy\ valve}$) is calculated using (5.16) in (5.17), resulting in $n_{thy\ valve} = 29$. Utilising (5.18) in (5.19), $n_{FB\ PG} = 4$, hence $n_{HB\ PG} = 4$. Proceeding to the capacitance design, Fig. 5.10(a) illustrates the absolute maximum energy deviation per SM ($\Delta E^{pp}_{SM_{max}}$) with varying k_1 and k_{PG} as discussed in Section IV-C. The plot indicates that as k_{PG} increases, $\Delta E^{pp}_{SM_{max}}$ decreases, indicating lower requirements of SM capacitance. Most values of k_{PG}, the optimal k_1 is around 1.19; hence, this value is selected for the design. Fig. 5.10(b) demonstrates $\Delta E^{pp}_{SM_{max}}$ and the total semiconductor losses percentage of the proposed converter with varying k_{PG} and maintaining k_1 at 1.19, where details about semiconductor losses can be found in Section VII. The plot reveals that as k_{PG} increases, the total losses increase while $\Delta E^{pp}_{SM_{max}}$ decreases.

The change in $\Delta E_{SM_{max}}^{pp}$ in the region of $2 < k_{PG} < 3$ is relatively minor compared to the region where $k_{PG} < 2$. Consequently, $k_{PG} = 2$ is selected as the optimum value, as it balances the SM energy requirements with the total semiconductor losses. Substituting the corresponding $\Delta E_{SM_{max}}^{pp}$ into (5.25), the SM capacitance is determined to be 6 mF. For the inductors, utilising (5.26), the suitable L_{PG} falls within the region of 30 µH. Employing (5.30), L_a is chosen to be 5 mH. Finally, utilising (5.32), the thyristor commutation voltage $V_{thy_{comm}}$ is selected to be equal to 0.1 V_{dc}.



(a) (b)

Fig. 5.10 (a) Variation of absolute maximum SM energy deviation ($\Delta E_{SM_{max}}^{pp}$) with k_1 and k_{PG}, (b) Relationship between $\Delta E_{SM_{max}}^{pp}$ and total semiconductor losses with k_{PG}.

5. 5 Simulation Results Validation

In this section, a MATLAB/SIMULINK model with 337 levels is used to validate the proposed power converter. Similar to the previous chapters, in order to simulate this large number of SMs efficiently while minimizing computational burden and enabling PWM control to capture the charging and discharging behaviour of the SM capacitors, the converter model is implemented using a switching-function approach. This is achieved by utilizing HB-MMC and FB-MMC blocks in MATLAB with switching function mode The model parameters are shown in Table 5.1, derived from the analyses conducted in Sections IV and V. A DC filter is incorporated to smooth the DC current and limit short circuit current. The proposed converter is evaluated under two scenarios: normal operation to test bidirectional power flow, and fault conditions to assess its DC fault blocking capability.

5.5.1 Normal Operation

The converter initially delivers power to the grid at 1 pu. Then, a power reversal is applied to change the power to -1 pu over a duration of 0.5s, as depicted in Fig. 5.11(a). The converter successfully achieves power reversal while maintaining zero reactive power, which validates converter controllability. The three-phase voltage and current are shown in Fig. 5.11(b) and (c), respectively. The phase current remains undistorted during thyristor commutation action. The upper arm currents are presented in Fig. 5.11(d), with the maximum value of the arm currents equalling the peak value of the output current, thereby achieving a low current stress converter operation. The stack voltage and the corresponding thyristor valve voltage are depicted in Fig. 5.12(a) and (b), respectively, following the theoretical claims illustrated in Fig. 5.2. In this case, the arm currents have a negative direction at the instant of commutation, resulting in a positive voltage being introduced on the thyristor valve during turn-off commutation. The capacitor voltages for PG_1 are shown in Fig. 5.12(c). The $FB\text{-}SMs_{max}$ and $FB\text{-}SMs_{min}$ capacitor voltages are displayed above and below the HB-SMs capacitor voltage, respectively, validating the control algorithm proposed previously. The average capacitor voltage of all PGs is depicted in Fig. 5.12(d), which confirms the effectiveness of the PG restricted balancing algorithm. The currents in both SMs and parallel thyristors in PG_1 are depicted in Fig. 5.13(a). For most of the conduction period, the current passes through the thyristors, indicating low conduction losses. Also, it verifies that the thyristors conduction state changes once every periodic cycle. The difference between the required number of SMs and the available SMs is shown in Fig. 5.13(b), illustrating the effect of the PG gain (k_{PG}=2).

Table 5.1: MATLAB/SIMULATION Model Parameters

Parameter	Description	Value
P_r	Rated power	900 MW
V_{dc}	DC link voltage	$\pm$300 kV
v_g	Grid voltage	430kV
f	Fundamental Frequency	50 Hz
L_{AC}	AC interfacing inductance	95.8 mH
T_c	Overall commutation time	1 ms
n_{PG}	Total number of power groups	32
$n_{HB\ PG}$	Total number of HB-SMs	4
$n_{FB\ PG}$	Number of FB-SMs	4
V_c	SM nominal voltage	1.8 kV
C_{HB}/C_{FB}	HB-SMs/FB-SMs capacitance	6 mF
L_a	Arm inductance	5 mH
L_{PG}	PG inductance	30 µH

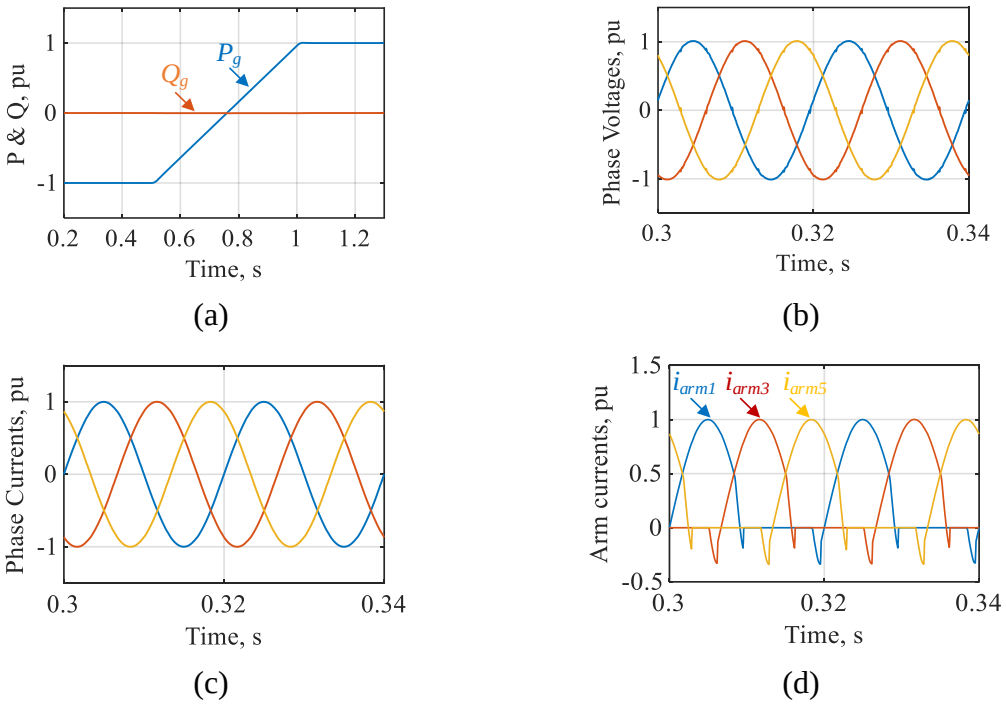


Fig. 5.11 Normal operation results: (a) grid active and reactive power, (b) phase voltages, (c) phase currents, and (d) upper arm currents.

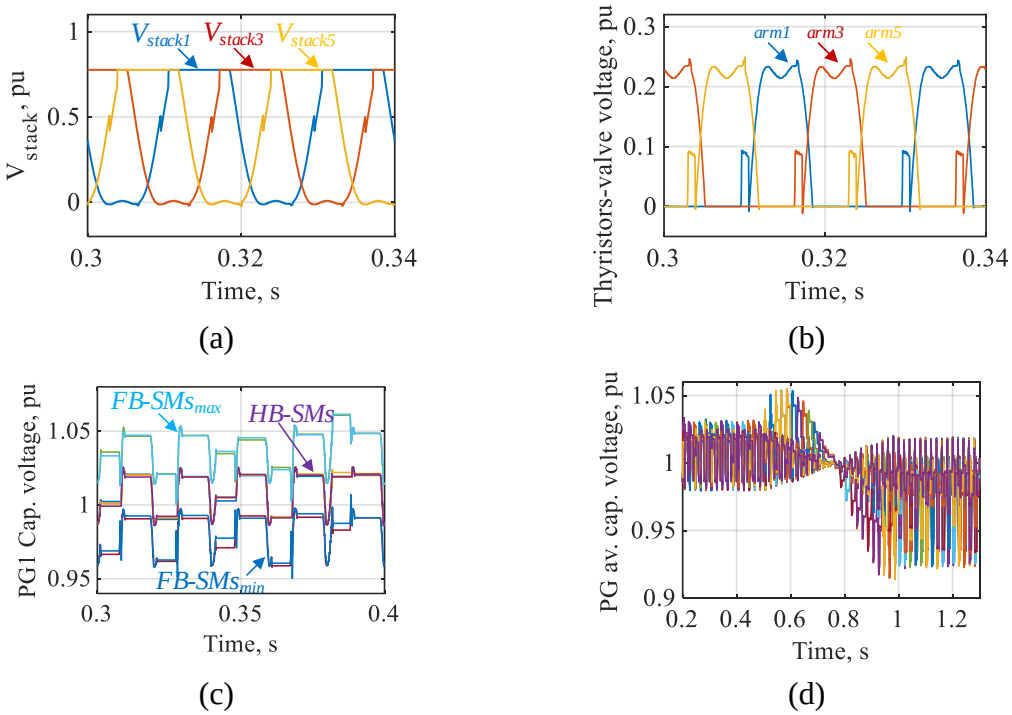


Fig. 5.12 Cont. normal operation results: (a) upper stack voltages, (b) upper thyristors-valve voltages, (c) PG1 capacitor voltages, and (d) average capacitor voltages in all PGs.

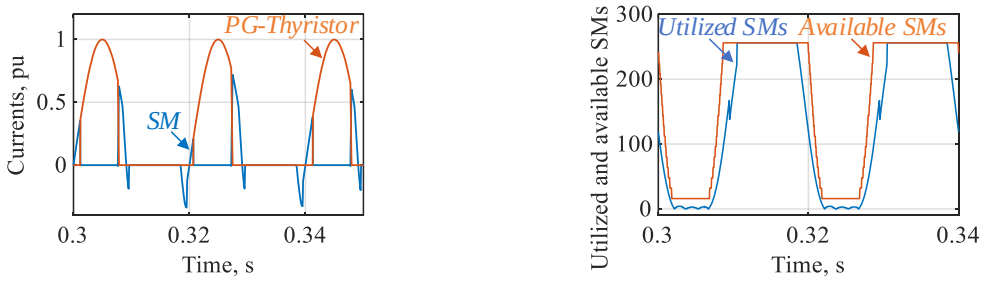


Fig. 5.13 Cont. normal operation results: (a) Current distribution between PG-thyristors and the SMs in PG 1 and (b) difference between the utilised and the available SMs.

5.5.2 DC Fault tolerance

A DC fault is introduced at 0.2s to test the DC fault-tolerant capability. In Fig. 5.14(a), the DC link voltage and current are shown. At the fault instant, the voltage collapses, while the DC current starts to increase. However, it rapidly decreases to zero after fault detection due to the action of the FB-SMs, as discussed previously. It is worth noting that this DC current is the sum of all conducting arms and does not pass through a single arm (This means that the IGBT switches in the modules do not experience current stress exceeding 2 pu.). Fig. 5.14(b) displays the AC phase currents, where the AC component of the fault current appears.

It is bypassed through the thyristors, effectively isolating this AC component from the DC side. Fig. 5.14(c) depicts the distribution of the arm current through the SMs and the PG-thyristors of PG 1. Only the DC component of the fault current passes through the SMs, peaking at less than 2 pu before being terminated by the FB-SMs. The longer/higher AC component of the fault current passes through the PG-thyristors, providing protection for the IGBTs until it is cleared by thyristor commutation. It is worth noting that the thyristors are able to withstand surge current of more than 20 times the rated current for 10 ms [72]. Finally, Fig. 5.14(d) shows the stack voltage and the series thyristor-valve voltage of arm 1 where it is evident that by controlling the FB-SMs voltage in the post-fault conditions, the grid AC voltage is suitably distributed among the PGs and the thyristor-valve.

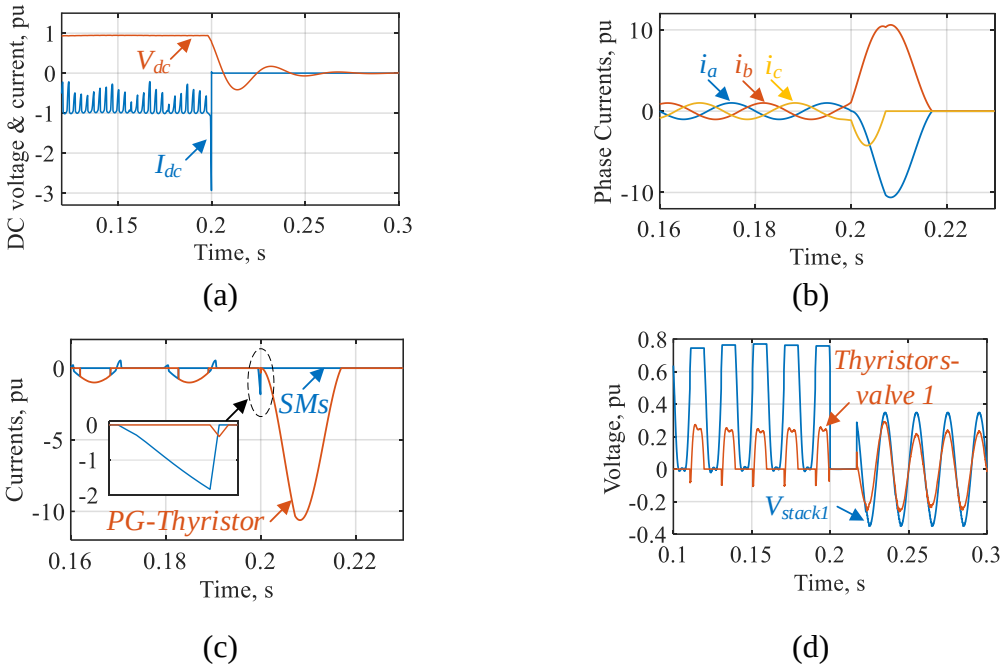


Fig. 5.14 DC fault results: (a) DC link voltage and current, (b) AC phase currents, (c) currents of the SMs and PG-thyristors, and (d) voltages of stack 1 and thyristors-valve 1

5. 6 Experimental Validation

A 5-level, 3-phase experimental test rig was constructed to validate the proposed converter as illustrated in Fig. 5.15. Each arm of the test rig consists of one PG and one series antiparallel thyristor. The PG is composed of two HB-SMs and one FB-SM, along with a parallel branch consisting of antiparallel thyristors and an inductor. Dspace is used as the controller of proposed converter which has 32 PWM outputs and 32 ADC channels. Furthermore, similar to Chapter 3, a CINERGIA grid emulator is used for grid integration and the DC grid is emulated using a bidirectional power supply from Itech (IT6006C-500-

40). The hardware components including the IGBT device, its gate driver, thyristors and its gate driver, sensors, etc are listed in Table 5.2. The schematics for power and control circuits for the HB-SMs, FB-SMs, thyristors, and sensors are listed in Appendix A. Furthermore, all the parameters of the experimental test rig are listed in Table 5.3.

Furthermore, similar to Chapter 3, a level-shifted PWM technique is used to control the SMs of the proposed converter, with a rotational scheme. Also, the reference signals from the control algorithm are compared to carriers generated within the Dspace, and the corresponding gating signals are produced via GPIOs.

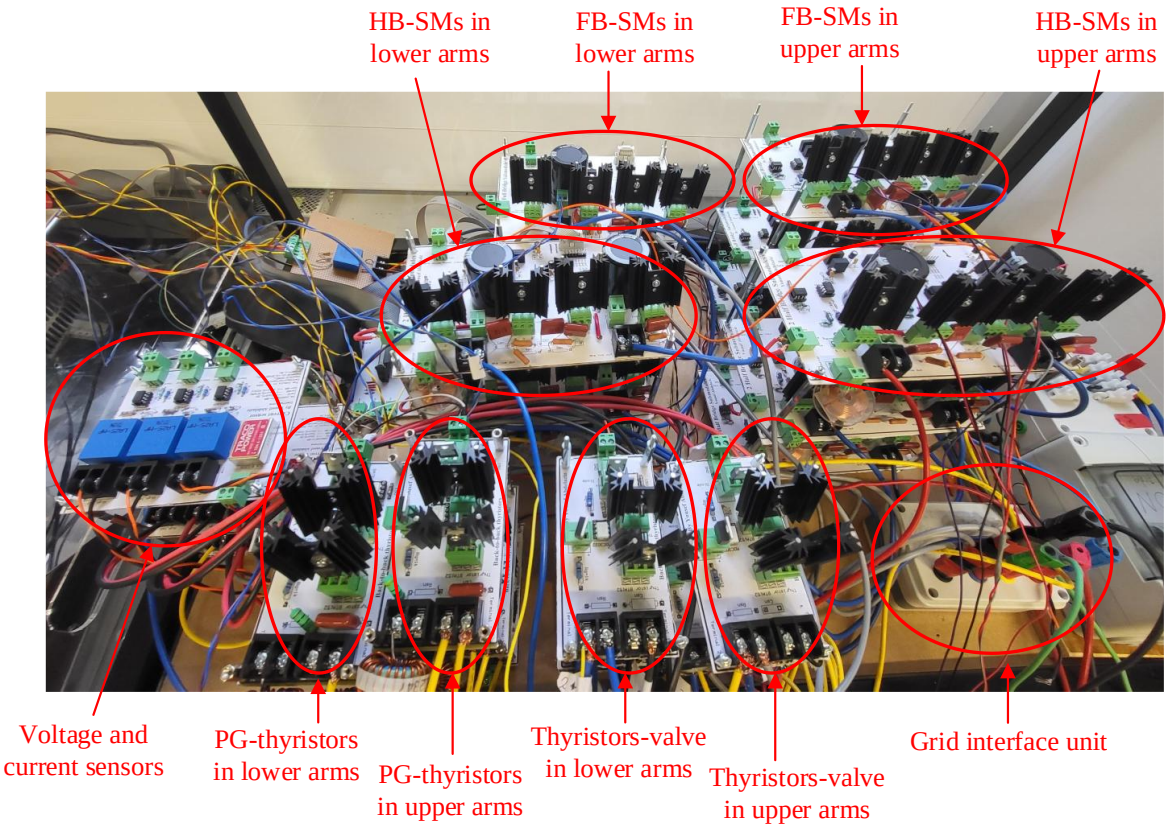


Fig. 5.15 Experimental test rig for the proposed PG thyristor-based multilevel converter.

Table 5.2: Hardware components

Controller	DSP	LAUNCHXL-F28379D
Grid	Grid Emulator	CINERGIA's Grid Emulators (GE15)
DC grid	DC Power Supply	IT6006C-500-40
IGBT	IGBT name	ONSEMI FGH40N60SMD, 600 V 80 A
	Optocoupler	6n139
	Gate driver	IR2111 (2 channels)
	DC/DC Converter	MPB1215S-1W (12 V:15 V)
Thyristor	Thyristor name	TYN640RG, 600 V 40 A
	Optocoupler	MOC3022-M (Triac)
Sensors	Voltage sensor	LV 25-P
	Current sensor	LEM LA 25-NP
	Operational amplifier	TL071ACP
	DC-DC converter	TEN 5-1223 (12 V : ±15 V)
Others	Capacitor unit	MCLPR100V109M40X6–10,000 µF, 100 V
	Power terminals	6PCV-02-006

5.6.1 Normal Operation

To test the controllability and bidirectional power capability of the proposed converter, the power is reversed from 200 W to -200 W within 1 second, while maintaining zero reactive power, as shown in Fig. 5.16(a). Similar to Chapter 3, the active and reactive power calculations are performed inside the Dspace, generated through the digital to analogue converter (DAC), and then measured using an oscilloscope. The voltage and current for phase 'a' are presented in Fig. 5.16(b). It is evident that the current is in phase with the voltage during forward power flow and shifts out of phase during reverse power flow, demonstrating the successful bidirectional operation of the proposed converter. The three-phase grid voltage and current are depicted in Fig. 5.16(c) and (d), respectively. It is clear that the phase currents are not distorted neither by the series thyristors commutation or the PG-thyristors commutation. The upper arm currents during forward and reverse power flow are depicted in Fig. 5.17(a) and (b), respectively. It is observed that peak of the arm currents matches that of the phase currents achieving low current stresses. Additionally, the arm current distribution in the first and second arm during forward and reverse power flows are depicted in Fig.

5.17(c) and (d), respectively. The results clearly show that the PG-thyristors operate during peak current instants in both cases, effectively utilizing the parallel thyristors in normal operation, thereby achieving reduced losses. The results also indicate that the PG-thyristors are fired only once per periodic cycle. Finally, the SMs capacitor voltages of the first arm are shown in Fig. 5.18(a), where the zoomed figure is depicted in Fig. 5.18(b). A balancing between the capacitors is achieved by using rotation between all the SMs during operation.

Table 5.3: Experimental Parameters

Parameter	Description	Value
P_r	Rated power	200 W
V_{dc}	DC link voltage	140 V
v_g	Grid voltage	80 V
f	Fundamental Frequency	50 Hz
fs	Switching frequency	1150 Hz
L_{AC}	AC interfacing inductance	20 mH
T_c	Overall commutation time	0.9 ms
V_c	SM nominal voltage	35 V
C_{SM}	SM capacitance	8.2 mF
L_a	Arm inductance	0.47 mH
L_{PG}	PG inductance	50 µH

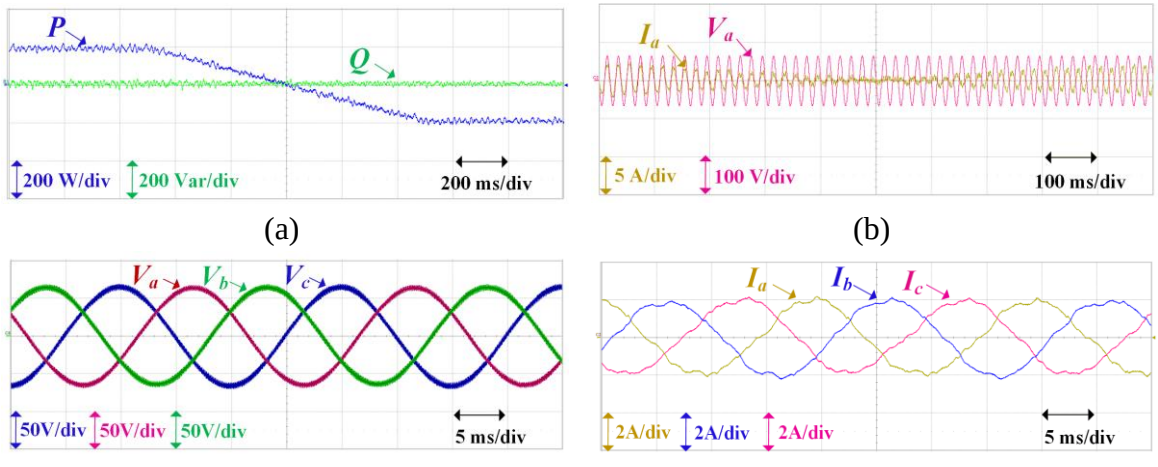


Fig. 5.16 Experimental results, normal operation: (a) Active and reactive power during power reversal, (b) phase 'a' voltage and current during power reversal, (c) three-phase grid voltage, (d) three-phase currents.

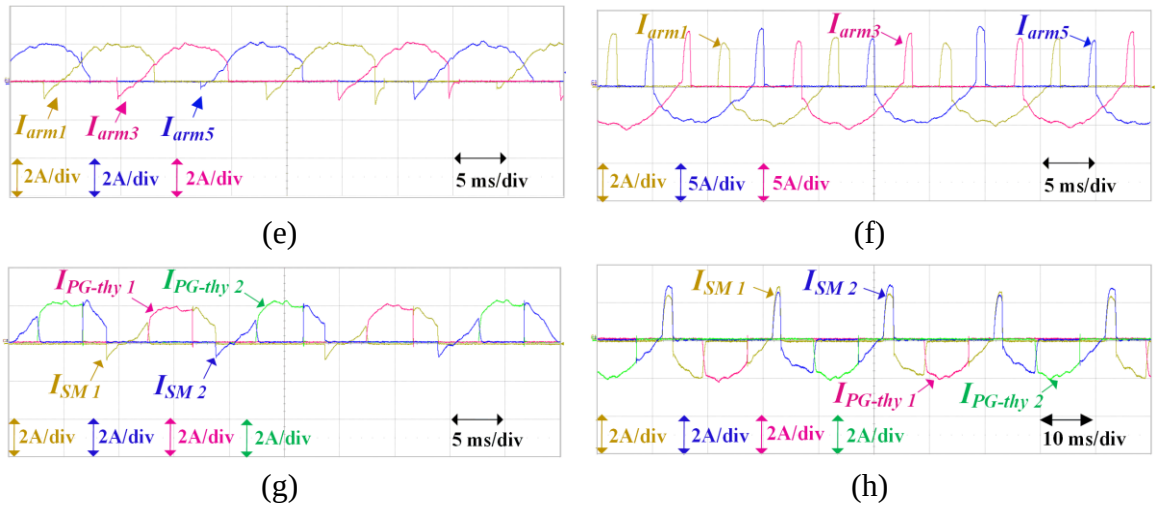


Fig. 5.17 Continue experimental results, normal operation: (a) upper arm currents during forward power flow, (b) upper arm currents during reverse power flow, (c) SM and PG-thyristor currents in the first and second arms during forward power flow, (d) SM and PG-thyristor currents in the first and second arms during reverse power flow,

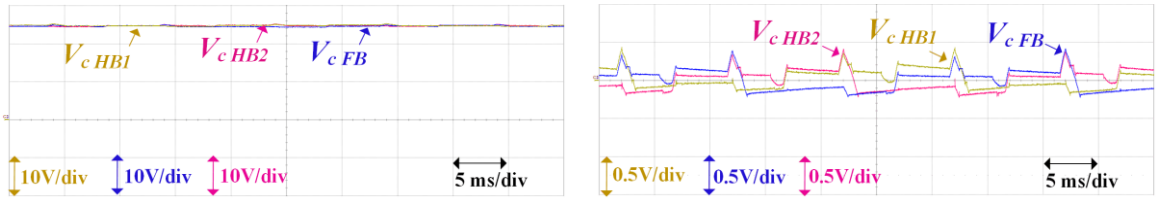


Fig. 5.18 Continue experimental results, normal operation: (a) capacitor voltages of the SMs in the first arm, (b) zoomed capacitor voltages of the SMs in the first arm.

5.6.2 DC Fault tolerance

In this scenario, a DC fault is applied to evaluate the DC fault blocking capability of the proposed converter. Similar to Chapter 3, The DC fault is implemented by connecting a low resistance in parallel with the DC source, while setting the DC source current limit to a low value. At the moment of the fault, the DC voltage collapses, as shown in Fig. 5.19(a). The phase currents increase at the moment of the fault, which is also depicted in Fig. 5.19(a). However, it can be observed in Fig. 5.19(b) that this AC current flows primarily through the upper arms, while the DC component of the fault current is blocked at almost 2 p.u. The lower arm currents are shown in Fig. 5.19(c), where only the AC component of the fault is swiftly terminated because of the firing of the upper arm thyristors. Finally, Fig. 5.19(d) shows the current distribution between the SMs and PG-thyristors during the fault. It is evident that only the DC component flows through the SMs, while the longer and larger AC

component of the fault current flows through the PG-thyristors until it is terminated by the thyristor commutation. This demonstrates the effective DC fault tolerance of the proposed converter.

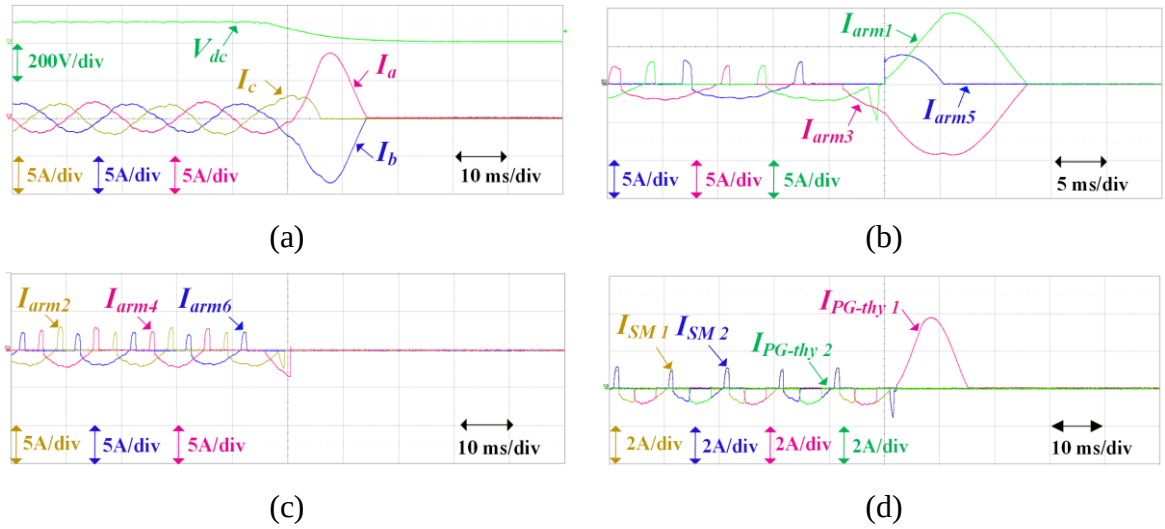


Fig. 5.19 Exp. fault scenario: (a) DC voltage and three phase currents, (b) upper arms currents, (c) lower arm currents (d) SM and PG-thyristor currents in the first and second arms.

5. 7 Comparison

A comparative analysis is conducted between the proposed converter and other DC-fault-tolerant PG-based converters, namely, PG-based FB-MMC, PG-based Hybrid-MMC, and AT-AAC, aiming to highlight the advantages and viability of the proposed topology. The comparison considers the number of SMs, semiconductors, and capacitors, as well as DC fault clearing time, semiconductor losses, overall cost, weight, and size. The comparison relies on the system specifications provided in Section V, and the typical semiconductors and capacitors utilised in the comparison are detailed in Table 5.4. The switching and conduction losses are calculated based on [68], with an average switching frequency of 250 Hz. The turn-off loss of the PG-thyristor is assumed to be 2 J, considering the utilisation of a low voltage in the turn-off process with a voltage of 200/3 V per thyristor. However, the turn-off loss for series thyristor-valve is calculated to be 28 J for each event due to the relatively high commutation thyristor voltage of the series thyristor-valve ($0.1V_{dc}/29$). The turn-on losses for all thyristors are presumed to be 2 J/kA as stated in [37], owing to the use of low voltage for turning on both PG and series thyristors. Moreover, the DC fault clearing time estimation is based on [33]. With the proposed control algorithm, all thyristors switch at the fundamental

frequency. A DC filter requires capacitance equivalent to a single leg as mentioned in [65]. The comparison results are summarised in Table 5.5, revealing several key advantages of the proposed converter PG-TMC over other configurations. Firstly, the proposed converter achieves the lowest number of PGs compared to other configurations. In terms of the DC fault clearing time, all mentioned converters are capable of swiftly blocking DC faults. The PG-TMC matches the low required capacitance per SM as that of AT-AAC, surpassing other topologies in this aspect. The proposed converter outperforms AT-AAC by requiring significantly fewer IGBTs and thyristors, attributed to its lower number of SMs and PGs. This reduction results in lower overall semiconductor losses and overall cost. The proposed converter has a smaller overall volume and lower weight compared to other configurations. These attributes make it particularly well-suited for offshore HVDC applications, where weight and volume are restrictive factors.

5. 8 Summary

A novel PG Thyristor based modular multilevel converter has been proposed, which attains DC-fault blocking capability with a reduced semiconductor count, leading to decreased semiconductor losses and overall cost. The operational analysis of the proposed converter demonstrated the utilisation of optimum arm voltage by incorporating a third harmonic waveform within the fundamental waveform. The PG control algorithm was elucidated to outline the proposed restricted balancing algorithms for PGs, as well as the activation and deactivation processes of PG-thyristors. A comprehensive design for all parameters was provided, complemented by a practical case study where the optimum value of k_1 is found to be 1.19 and the PG gain k_{PG} is determined to be 2, striking a balance between converter losses and SM capacitance energy requirements. The assertions of the Chapter were validated using a MATLAB/SIMULINK model of a 337-level system. A comparative analysis with other fault-tolerant PG-based converters revealed that the proposed converter achieves the same SM capacitance as the AT-AAC while requiring a lower IGBT count; 54% lower than that of the AT-AAC. Also, PG-TMC exhibits lower conduction losses, which are 15.61% lower than AT-AAC, and incurs a lower overall cost, which is 38.17% lower than AT-AAC. The proposed converter occupies a smaller volume and weight, with reductions of 16.65% and 14.94%, respectively, compared to AT-AAC. Therefore, the proposed converter emerges as an optimal choice among PG-based MMCs across all facets of comparison. Its

superior performance makes it highly suitable for various HVDC applications, particularly advantageous for offshore deployments due to its reduced weight and volume.

Table 5.4: Typical Semiconductors/Capacitors Parameters.

IGBT device	Infineon FZ1500R33HE3–3.3 kV 1.5 kA
IGBT on-state voltage	3 V for IGBT, 2.75 V for diode
IGBT turn on/off energy loss	2.55+2.1 J
Diode fast recovery loss	1.65 J
IGBT weight, size, cost	1.2 kg, 785 cm3, £1,459.67
Thyristor device	Infineon T2871N –8 kV 2.62 kA
Thyristor on-state voltage	1.5 V
PG-Thy. turn on/off loss	2 J/kA, 2 J
Series thy. turn on/off loss	2 J/kA, 28 J
Thyristor weight, size, cost	4 kg, 818 cm3, £3,685.50
Capacitor unit	C44UVGT7105M34K –1,050 µF, 1.8 kV
Capacitor unit cost, weight, size	5.1 kg, 5,311 cm3, £150

Table 5.5: Key Feature Comparison of Different Converters based on 337-level HVDC System Parameters.

Converter Type	PG-FB-MMC	PG-Hybrid-MMC	AT-AAC	**PG-TMC**
No. of SMs	336x6	336x6	384x6	**256x6**
No. of PGs	42	42	48	**32**
HB-SMs per PG	−	4	−	**4**
FB-SMs per PG	8	4	8	**4**
AC rms voltage	367 kV	367 kV	489 kV	**437 kV**
Rated stack Voltage	1 pu	1 pu	1.15 pu	**0.762 pu**
Capacitance per SM	9.6 mF	9.6 mF	6 mF	**6 mF**
Total number of capacitors	9 x 336 x 6 =20160	9 x 336 x 6 =20160	6 x 384 x 6 =13824	**6 x 256 x 8 =12288**
No. of IGBTs	4x336x6 =8064	4x168x6+2x168x6 =6048	4x384x6 =9216	**4x128x6+2x128x6 =4224**
No. of Thyristors	2x126x6 =1512	2x126x6 =1512	2x144x6 =1728	**2x29x6+2x96x6 =1500**
DC fault clearing time	0.5~1 ms	1.5~3 ms	0.5~1 ms	**0.5~3 ms**
SM conduction losses	0.273%	0.205%	0.153%	**0.0883%**
SM switching losses	0.101%	0.101%	0.08%	**0.0724%**
Thyristor conduction losses	0.048%	0.048%	0.046%	**0.0553%**
Thyristors turn on/off losses	0.021%	0.021%	0.022%	**0.0379%**
Total semiconductor losses	0.443% (4 MW)	0.375% (3.38 MW)	0.301% (2.71 MW)	**0.254% (2.29 MW)**
Overall converter cost	£ 20.37 M	£17.42 M	£ 21.9 M	**£13.54 M**
Overall Converter Weight	118.54 tons	116.12 tons	88.47 tons	**73.74 tons**
Overall Converter Size	131.83 m3	130 m3	94.38 m3	**80.28 m3**

Chapter 6

A Novel DC Series-Isolated-Parallel Wind Farms Architecture with DC Fault-Tolerance Capability

Offshore wind farm DC collection systems offer significantly lower weight and size compared to conventional AC collection systems. Within DC collection, series-parallel wind farm (SP-WF) architecture is considered more efficient than parallel wind farm (P-WF) architecture due to fewer power conversion stages. However, SP-WF typically experiences wind curtailment during periods of varying wind turbine generation and is generally less reliable than P-WF, as it cannot tolerate short-circuit faults. In this Chapter, a novel series-isolated-parallel wind farm (SIP-WF) architecture is proposed, which combines high efficiency and DC fault tolerance. In SIP-WF, each group of series-connected wind turbines is isolated by a DC-DC converter, enabling DC short-circuit fault blocking without the need for DC breakers, thereby enhancing reliability. The proposed SIP-WF architecture, along with two control methodologies, is validated using MATLAB SIMULINK. A comparison based on real wind data over a full year demonstrates that the proposed SIP-WF generates higher net energy than P-WF by more than 3%, while offering 50% lower initial cost, weight and volume in addition to improved reliability

6. 1 Proposed Architecture Description

The proposed novel DC series-isolated-parallel wind farm (SIP-WF) architecture is illustrated in Fig. 6.1. This architecture consists of M parallel wind turbine groups (WTGs), where each WTG comprises a series connection of N wind turbines (WTs) through their AC-DC converters. Additionally, a DC-DC converter is employed in each group to fulfil three main functions:

- Stepping up the voltage of the series-connected WTs to the HVDC transmission voltage level.
- Isolating the WTGs from each other, thereby providing DC short-circuit fault tolerance and increasing reliability.
- Enabling maximum power point tracking (MPPT) for the entire WTG.

Permanent magnet synchronous generator (PMSG)-based WTs are selected for this study due to their compact design, high power density, reduced maintenance, high efficiency, and

lack of need for external excitation. This allows the use of unidirectional converters such as diode rectifiers, which further enhance the efficiency of the overall proposed architecture. Moreover, in [73], a comparison was made between PMSG rectifiers, including VSCs with constant and variable DC voltage, and diode-bridge rectifiers. The results showed a significant reduction in losses when using diode rectifiers compared to other VSCs, thereby justifying the choice of uncontrolled diode bridge rectifiers as the AC-DC converter in the proposed topology

Additionally, it is important to note that wind speed variations among turbines in each WTG are accounted for in the MPPT. This is further discussed in this Chapter, where an optimization algorithm is proposed to achieve MPPT despite differences in wind speeds within the same WTG. More details regarding the DC-DC converter are also provided later in the Chapter.

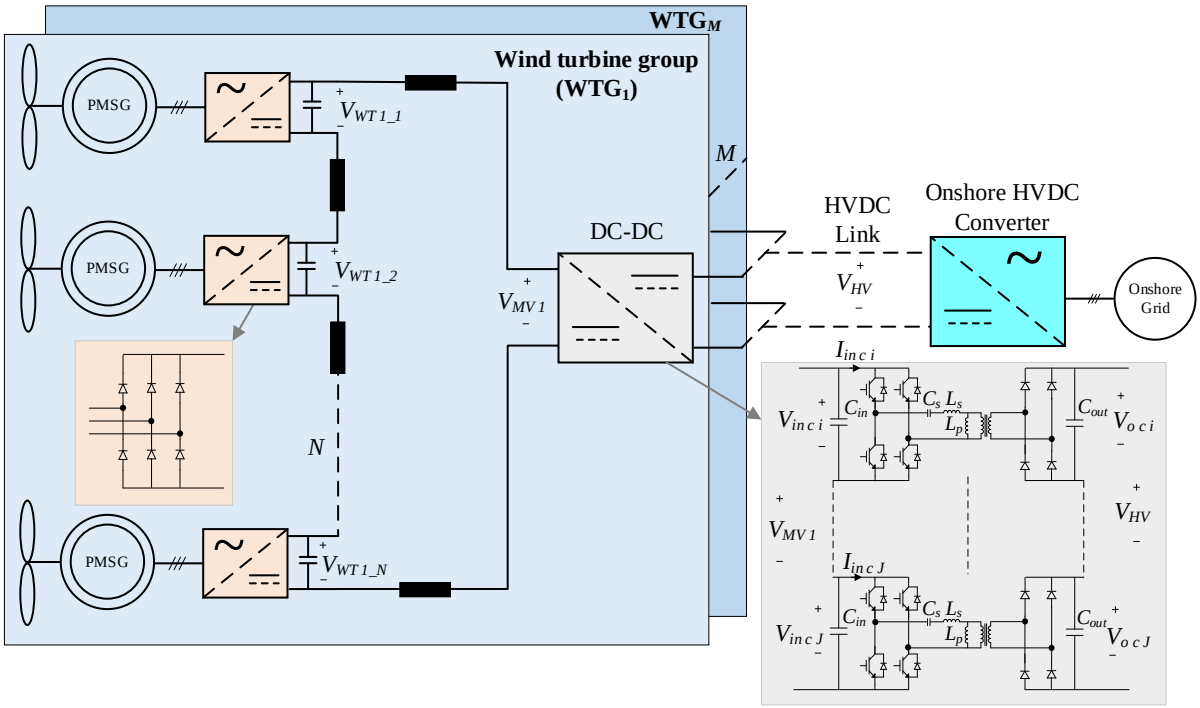


Fig. 6.1 Proposed Series-Isolated-Parallel Architecture

6. 2 Mathematical Analysis

In this section, the mathematical analysis of the wind turbine, uncontrolled diode rectifier, and DC-DC converter is presented to provide a foundation for the optimization algorithm.

6.2.1 Wind Turbine Modelling

The power generated by the wind turbine (WT) depends on wind speed and is given by [74]:

$$P_m = c_p(\lambda, \beta)\frac{\rho\pi R^2}{2}v_w^3 \tag{6.1}$$

where R is the radius of the WT blade, ρ is the air density, v_w is the wind speed, and c_p is the WT power coefficient, which depends on the tip speed ratio (λ) and the pitch angle (β). The power coefficient is calculated as follows [74]:

$$c_p(\lambda, \beta) = c_1\left(\frac{c_2}{\lambda_i} - c_3\beta - c_4\right)e^{-\frac{c_5}{\lambda_i}} + c_6\lambda_i \tag{6.2}$$

where:

$$\frac{1}{\lambda_i} = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1} \tag{6.3}$$

The WT coefficients c_1 to c_6 depends on the aerodynamic design of the WT. The tip speed ratio (λ) is calculated as follows:

$$\lambda = \frac{R\ \omega_m}{v_w} \tag{6.4}$$

where ω_m is the rotor speed. Since the WTs are connected in series within each WTG of the proposed architecture, the DC-side currents of the uncontrolled diode rectifiers remain equal, even during wind variations across the series WTs. Therefore, conventional single-unit maximum power point tracking (MPPT) methods are unsuitable. An optimization algorithm is necessary to determine the optimal operating points for all WTs in each WTG, satisfying the equal current constraint. This requires an analysis of the diode bridge rectifier, discussed in the next subsection.

6.2.2 Diode Bridge Rectifier Analysis

A balanced three-phase operation is assumed in this analysis, considering the PMSG inductance (L_{SG}) and neglecting stator resistance for simplicity. The DC voltage (V_{dc}) and current (I_{dc}) at the output of the diode bridge rectifier is calculated as follows [49, 75]:

$$V_{dc} = \frac{3\sqrt{2}}{\pi} E_{PM_{LL}}^{RMS} - \frac{3}{\pi} \omega_e L_{SG} I_{dc} \tag{6.5}$$

$$I_{dc} = \frac{\pi}{\sqrt{6}} I_{t_1}^{RMS} \tag{6.6}$$

where $E_{PM_{LL}}^{RMS}$ is the RMS line-induced voltage of the PMSG, ω_e is the electrical angular velocity, $I_{t_1}^{RMS}$is the fundamental RMS current of the PMSG. The RMS phase-induced voltage of the PMSG is given as:

$$E_{PM_{LN}}^{RMS} = k_{PM} \omega_m \tag{6.7}$$

where k_{PM} is the stator field constant. The relation between the electrical and mechanical angular velocities is:

$$\omega_e = p\omega_m \tag{6.8}$$

where p is the pole pair number of the PMSG. Substituting (6.8) and (6.7) into (6.5) and multiplying by I_{dc}, then the electrical power is calculated as follows:

$$P_e = \frac{3\sqrt{6}}{\pi} k_{PM} \omega_m I_{dc} - \frac{3}{\pi} p \omega_m L_{SG} I_{dc}^2 \tag{6.9}$$

Solving (6.9), and assuming $P_e = P_m$, the DC current is:

$$I_{dc} = \frac{3k_{PM}\omega_m - \sqrt{\omega_m(9\omega_m k_{PM}^2 - 2\pi p L_{SG} P_m)}}{\sqrt{6} L_{SG} p \omega_m} \tag{6.10}$$

6.2.3 DC-DC Converter Analysis

The selected DC-DC converter must operate over a wide range of voltages, from the minimum required voltage (one WT operating just above the cut-off speed) to the maximum required voltage (all WTs in the WTG operating at their rated speed). As stated in [76], the modular isolated LLC resonance converter achieves the best efficiency compared to L-C-C resonant converters and full-bridge converters with phase-shift control. Therefore, a series-input-series-output (SISO) configuration of multiple DC-DC converters is adopted in this Chapter, as shown in Fig. 6.1. The LLC resonance converter is detailed in [77], where the voltage gain (G_c) of the LLC resonant converter is controlled through a pulse frequency modulation (PFM) as follows:

$$G_c = \frac{n_t V_{o_c}}{V_{in_c}} = \frac{\frac{\omega}{\omega_0}\sqrt{m(m-1)}}{\sqrt{\left(\frac{\omega^2}{\omega_p^2}-1\right)+\frac{\omega^2}{\omega_0^2}\left(\frac{\omega^2}{\omega_0^2}-1\right)^2 (m-1)^2 Q^2}} \tag{6.11}$$

where ω is the operating angular frequency, ω_o is the first resonant frequency based on L_s and C_s, and ω_p is the second resonant frequency, calculated using L_p, L_s and C_s. Also, m is the ratio between $L_p + L_s$ and L_s, V_{o_c} and V_{in_c} are the output and input voltage of the LLC converter unit respectively, and n_t is the turns ratio between the input and output sides. Finally, Q is the equivalent quality factor, given by:

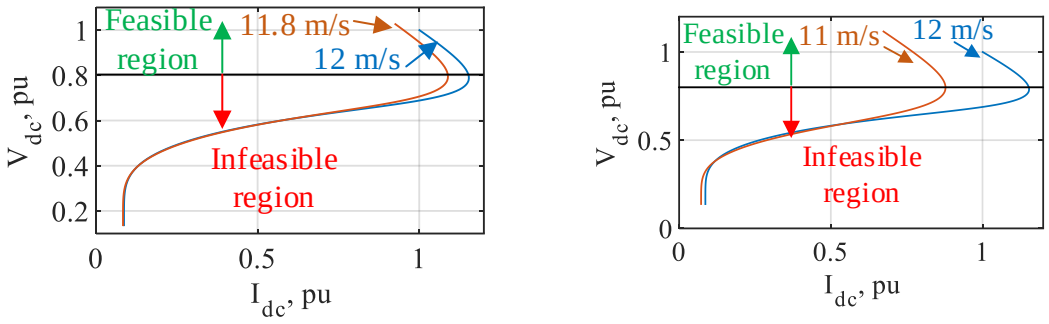
$$Q = \sqrt{\frac{L_s}{C_s}}\frac{\pi^2 m}{8n^2(m-1)V_o^2}P_c \tag{6.12}$$

where P_c is the power of the LLC converter unit. It is worth noting that the rated operating point (highest input voltage) is designed at ω_o to ensure ZVS (zero-voltage switching) throughout the entire operating range.

6. 3 Case study

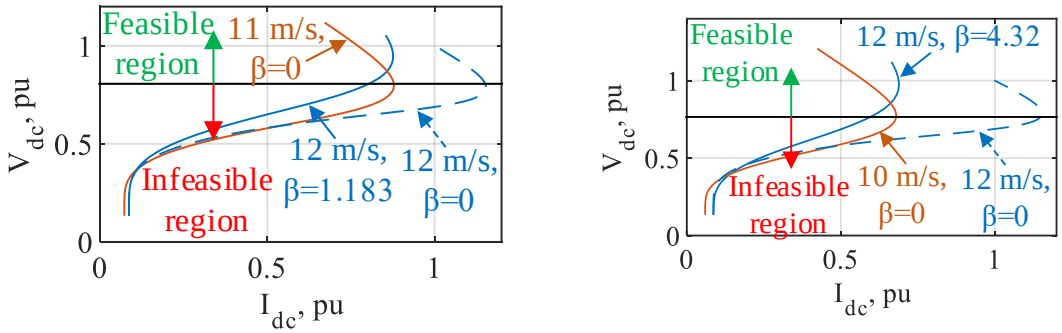
In this section, a case study is conducted to investigate the impact of series-connected wind turbines (WTs) using uncontrolled rectifiers on overall performance and wind power generation. For simplicity, two series-connected WTs are assumed. Fig. 6.2 shows the relationship between DC voltage and current for the two series WTs at different wind speeds, covering a range of rotor speeds up to the rated speed. This figure is generated by calculating the DC current at different rotor speeds values (from 0.1 to 1 pu) by substituting (6.1) into (6.10). The corresponding DC voltage is then determined at the same rotor speeds by dividing the power, calculated from (6.1), by the DC currents. This process is repeated for different wind speeds to plot the characteristics of the second wind turbine. Since the WTs are connected in series, they must have the same DC current. It was found that only above the knee point (indicated by the horizontal black line in Fig. 6.2) do the series WTs share the DC voltage regulated by the DC-DC converter. This area is considered the feasible region. However, below the knee point is considered the infeasible region, where the higher wind speed WT will dominate and operate alone at the total DC voltage. Furthermore, when there is a low wind speed deviation between the two series WTs, as shown in Fig. 6.2(a), there are multiple operating points within the feasible region, making maximum power point tracking

(MPPT) feasible for the total power. However, as the wind speed deviation increases, as seen in Fig. 6.2(b), there are no operating points for both WTs in the feasible region. In this case, the DC-DC converter is controlled such that the higher wind speed WT operates alone at its maximum power.



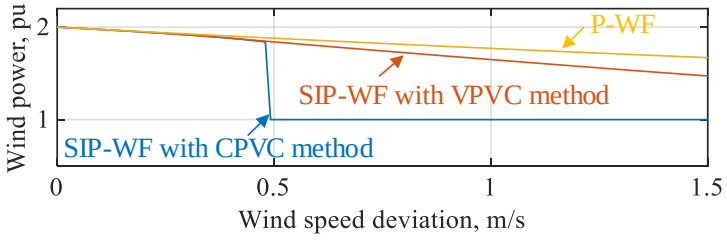
(a) (b)

Fig. 6.2 The relation between the DC voltage and current of two series WTs without pitch angle control at (a) 0.2 m/s wind speed deviation, (b) 1 m/s wind speed deviation.

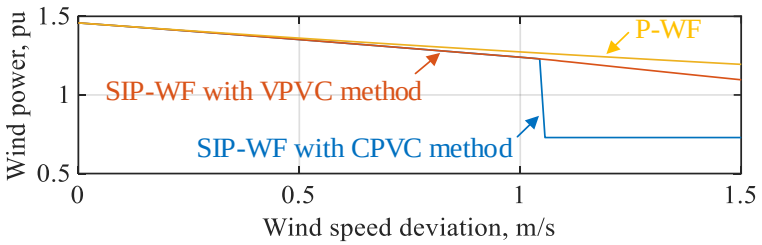


(a) (b)

Fig. 6.3 The relation between the DC voltage and current of two series WTs with controlling the pitch angles at (a) 1 m/s wind speed deviation, (b) 2 m/s wind speed deviation.



(a)



(b)

Fig. 6.4 Maximum extracted wind powers of the two WTs against the wind speed deviation between them: (a) deviation from rated wind speed (12 m/s), (b) deviation from below rated wind speed (10.8m/s).

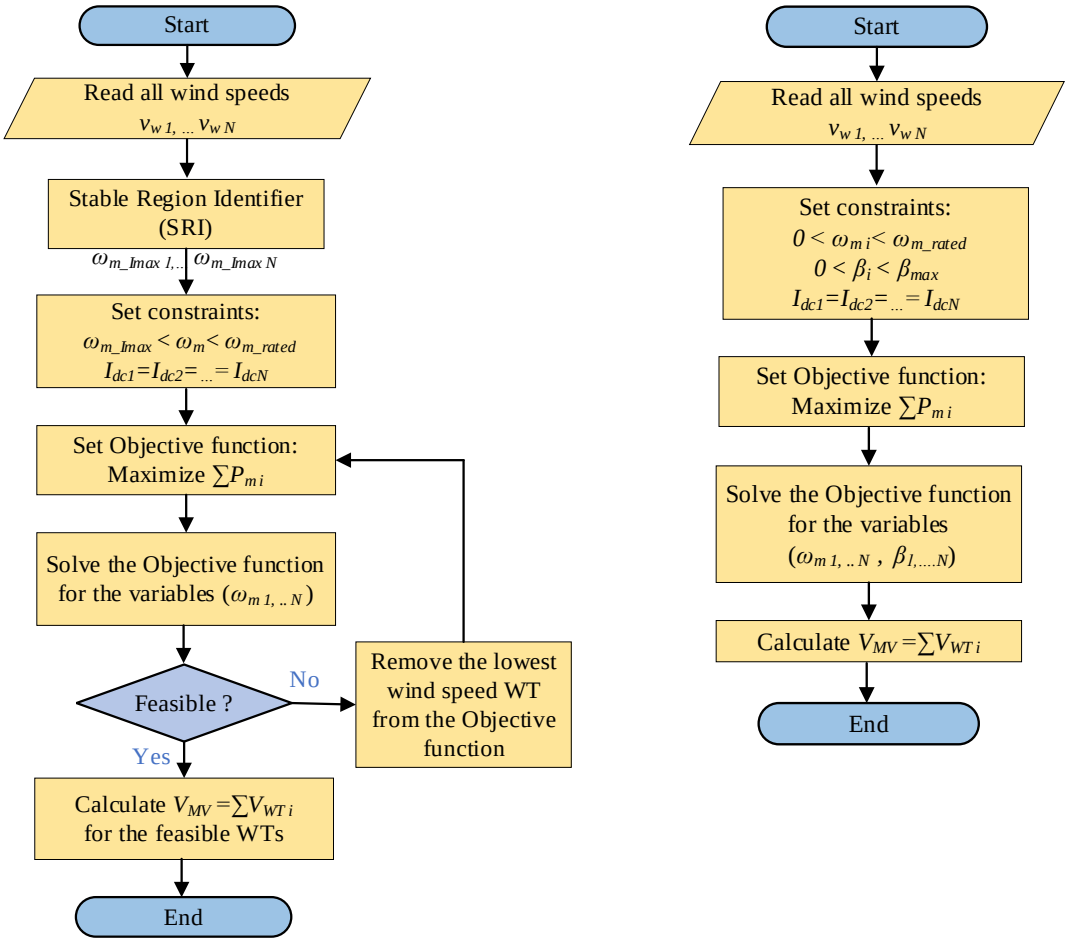
To address this issue, controlling the pitch angles (β) of the higher wind speed WTs is proposed to increase the total extracted wind power, particularly when there is a significant wind speed deviation between the WTs, as shown in Fig. 6.3. Fig. 6.3(a) and (b) illustrate the relationship between DC voltage and current when adjusting the pitch angles for 1 m/s and 2 m/s wind speed deviations, respectively. It is evident that increasing the pitch angle of the higher wind speed WT shifts the curve to the left, allowing operating points for both WTs to be found within the feasible region. Additionally, Fig. 6.4 shows the wind power extracted from the two series WTs for different wind speed deviations, comparing the cases of parallel connection (P-WF), proposed SIP-WF architecture with constant pitch voltage control (CPVC) method, and proposed SIP-WF architecture with variable pitch voltage control (VPVC) method. It should be noted that this extracted power is calculated before any conversion stages. In Fig. 6.4(a), the wind speed of the first WT is assumed to be constant at the rated wind speed, while the wind speed of the second WT deviates below the rated wind speed. In Fig. 6.4(b), the wind speed of the first WT is assumed to be constant at a value below the rated wind speed (10.8 m/s), while the wind speed of the second WT deviates below this value. It is worth noting that the extracted wind power in the case of the P-WF represents the maximum extracted power without any wind power curtailment. It can be observed that below a critical wind speed deviation, the wind curtailment is negligible, and all methods extract nearly the same maximum power. Additionally, this critical wind speed deviation increases to more than 1 m/s in the second case compared to 0.5 m/s in the first case.

6. 4 Control Algorithms

This section describes the two proposed control algorithms: constant-pitch voltage control (CPVC) and variable-pitch voltage control (VPVC). The primary goal of both methods is to optimize wind power capture while maintaining stable operation and efficient voltage regulation in the proposed SIP-WF architecture.

6.4.1 Constant-pitch voltage control (CPVC) method

In the first control method, the only controlled parameter is the input voltage of the DC-DC converter (V_{MV}). The variables in the optimization algorithm are the rotor speeds of the WTs, (ω_{m_1} *to* ω_{m_N}), where the pitch angles (β_1 to β_N) are maintained at their optimal values (which is zero below the rated wind speeds). The optimization algorithm for this control method is illustrated in Fig. **6.5**(a).



(a) (b)

Fig. 6.5 Optimization algorithm of the proposed SIP-WF control methods: (a) CPVC method, (b) VPVC method.

The first step is to identify the feasible region of each WT based on its wind speed. This is done by using (6.10) to find the rotor speed at the maximum DC current ($\omega_{m_{Imax}}$). The value of $\omega_{m_{Imax}}$ is then set as the minimum boundary for the rotor speed, with the following constraints:

$$Constraints = \begin{cases} I_{dc_1} = I_{dc_2} = \cdots = I_{dc_N} \\ \omega_{m_{Imax}i} \leq \omega_{m_i} \leq \omega_{m_{rated}} \end{cases} \quad (6.13)$$

The equal DC current constraint is calculated by substituting into (6.10) for all the corresponding WTs. The next step is to set the objective function, which maximizes the sum of wind power for each WT, as given by (6.1) as follows:

$$Objective = \sum_{i=1}^{i=N} P_{m_i} \quad (6.14)$$

If no feasible solutions are found, which may occur when there are large wind speed deviations, the algorithm removes the WT with the lowest wind speed from the objective function and repeats the previous step till a feasible solution is identified. Finally, the DC-DC converter input voltage (V_{MV}) is calculated at the optimum solution as follows:

$$V_{MV} = \frac{1}{I_{dc}} \sum_{i=1}^{i=N_f} P_{m_i} \quad (6.15)$$

where N_f is the number of feasible WTs. The overall control block diagram of the CPVC control method is illustrated in Fig. 6.6(a). It is worth noting that the V_{MV} value is equally divided among the series LLC converters, where J is the number of LLC units per DC-DC converter. Both voltage and current loops are employed before sending the reference frequency to the pulse frequency modulation (PFM). On the other hand, It should be noted that the pitch angles are controlled by a completely decoupled system to only limit the rotor speed from exceeding the rated value, especially at wind speeds above the rated value.

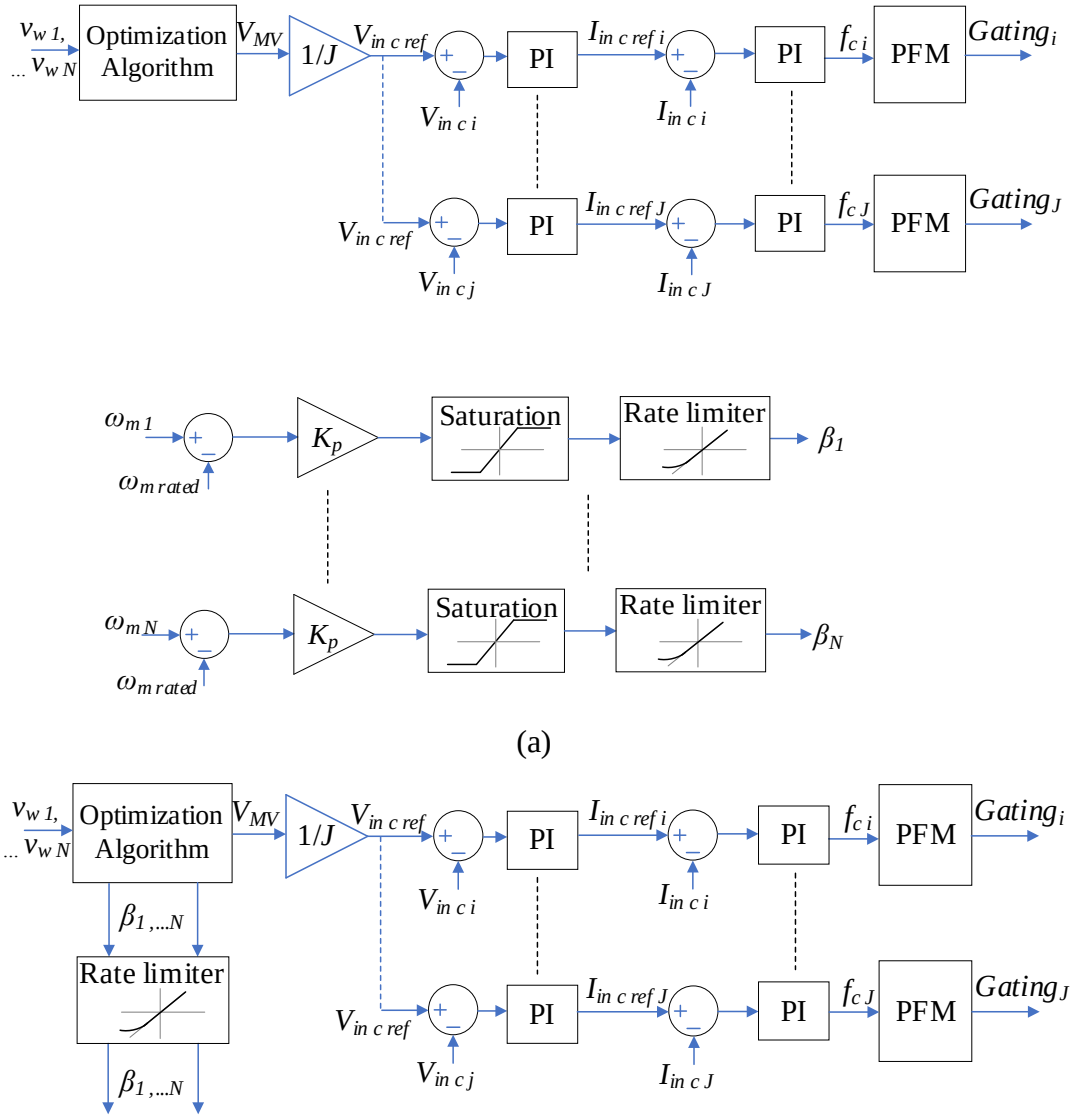


Fig. 6.6 Control block diagram for the proposed SIP-WF control methods: (a) CPVC method, (b) VPVC method.

6.4.2 Variable-pitch voltage control (VPVC) method

In the second control method, the pitch angles (β_1 to β_N) as well as the input voltage of the DC-DC converters (V_{MV}) are controlled. Hence, both rotor speeds (ω_{m_1} to ω_{m_N}) and pitch angles (β_1 to β_N) of the WTs within the WTG are considered variables in the optimization problem. This control is more complex as it requires signals for both the DC-DC converters and the internal control of the wind turbine blades. In this method, no need to identify the feasible region since the algorithm will always find an optimal solution in the feasible region by adjusting the pitch angles. The constraints for this method are as follows:

$$Constraints = \begin{cases} I_{dc_1} = I_{dc_2} = \cdots = I_{dc_N} \\ 0 \leq \omega_{m_i} \leq \omega_{m_{rated}} \\ 0 \leq \beta_i \leq \beta_{i_{max}} \end{cases} \quad (6.16)$$

The optimization algorithm of the VPVC method is depicted in Fig. **6.5**(b) and the overall control algorithm is explained in the block diagram shown in Fig. 6.6(b). It is worth noting that a rate limiter is used at the output of the pitch angle controller to simulate the slow dynamic response of the mechanical parts of the WT blades. Also, it should be noted that in this second method, the pitch angles are adjusted more frequently compared to the first method, leading to greater wear on the pitch control mechanisms. Furthermore, similar to the first control method, additional control of pitch angles is added to limit the rotor speed from exceeding the rated value in case of emergency situations, however, it is not added to Fig. 6.6(b) to prevent confusion.

6. 5 Simulation Results Validation

To validate the proposed architecture and controllers, a MATLAB SIMULINK model is developed for the proposed system, consisting of 10 WTGs, with each WTG comprising 6 WTs rated at 5 MW each. The two proposed control methods, CPVC and VPVC, are validated in this section for the proposed SIP-WF architecture, along with a comparison to the conventional parallel architecture.

Table 6.1: Wind farm parameters

Wind Turbine	
Rated Power	5 MW
Cut-in wind speed	3 m/s
Rated wind speed	12 m/s
Cut-out Wind speed	25 m/s
Rotor diameter	126 m
Blade-pitch rate limit	8°/s
PMSG generator	
Rated power	5 MW
Rated shaft speed	1.55 rad/s
Pole-pair count	290
Rated line voltage	5 kV
Synch. inductance	4.33 mH
Wind Farm Array	
N. of series WTs	6
N. of WTG	10
Total rated power	300 MW
Distance between near WTs	1 km
Internal cable size	(1000m2 Cu)
R_{cable}	17.6 mΩ/km
L_{cable}	1.3 mH/km
C_{cable}	0.19 µF/km

The parameters for the wind farm array including details of the WT and the PMSG are summarized in Table 6.1, with WT and PMSG parameters based on [49], and internal cable parameters derived from [60]. The pitch angle rate limiter is set to a maximum of 8 degrees per second as specified for a 5 MW WT in [78]. Each WT is rectified through a uncontrolled three-phase diode rectifier. Ten series-connected LLC converter units, each rated at 3 MW, are employed in the DC-DC converter for each WTG to step up the voltage to the HVDC level. The semiconductor parameters are summarized in Table 6.2. It should be noted that the base power is set as 5 MW. It should be noted that only one WTG is implemented in detail with its DC-DC converters in the MATLAB SIMULINK, where both

the wind turbine and permanent magnet synchronous machine blocks found in the MATLAB SIMULINK library are used to simulate the wind turbine. The other WTGs are simulated using an equivalent model.

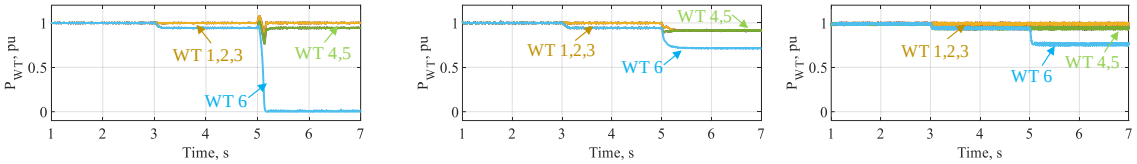
Two scenarios are tested in this section. The first scenario evaluates the normal operation of the proposed architecture with its control methods in comparison to the conventional parallel architecture, focusing on different wind speed deviations. The second scenario tests the DC fault tolerance capability to validate the high reliability of the proposed architecture.

Table 6.2: Typical Semiconductors parameters

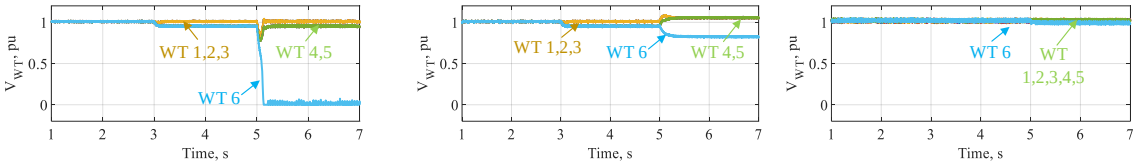
Three-phase Diode Rectifier	
Rated DC voltage & current	5.1 kV, 0.98 kA
Diode specs (Infineon D2601N)	9 kV 2.2 kA
LLC converter unit	
IGBT 5SNA 1000G650300	
P_c	3 MW
$V_{in_{c_{max}}}$	3 kV
V_{o_c}	30 kV
$1:n_t$	1:8.7
C_s	35.4 µF
L_s	44.74 µH
L_p	179 µH
f_o	4 kHz
DC-DC converter	
N. of Series converters	10
Total power	30 MW

Table 6.3: Wind speeds of the WTs per the first WTG

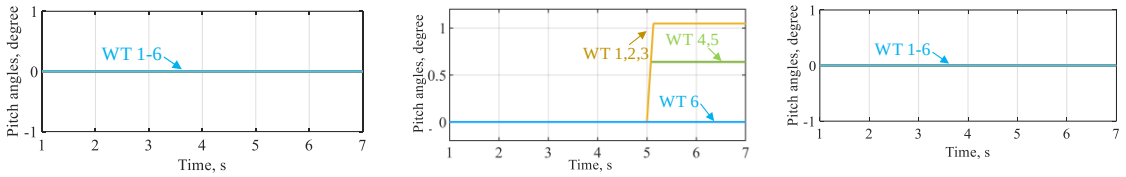
Time steps (m/s)	WT1	WT2	WT3	WT4	WT5	WT6
First	12	12	12	12	12	12
Second	12	12	12	11.8	11.8	11.8
Third	12	12	12	11.8	11.8	11



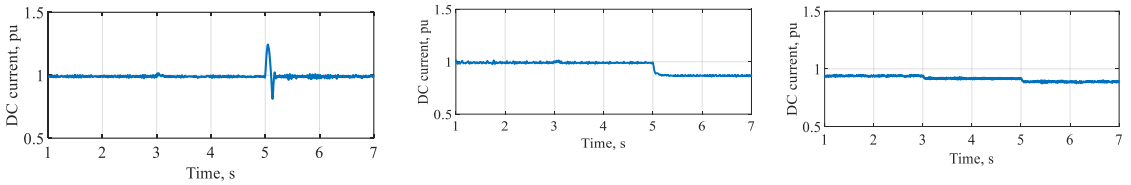
(I-a) WT captured power (II-a) WT captured power (III-a) WT captured power



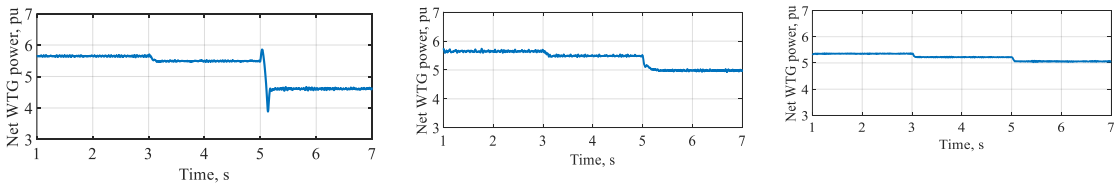
(I-b) WT DC voltages (II-b) WT DC voltages (III-b) WT DC voltages



(I-c) WT pitch angles (β) (II-c) WT pitch angles (β) (III-c) WT pitch angles(β)



(I-d) DC current (II-d) DC current (III-d) DC current



(I-e) Net WTG power (II-e) Net WTG power (III-e) Net WTG power

Fig. 6.7 Normal operation simulation results: (I) proposed SIP-WF architecture with the CPVC method, (II) proposed SIP-WF architecture with the VPVC method, (III) conventional parallel architecture P-WF.

6.5.1 Normal Operation Performance Evaluation

In this scenario, the focus is on one WTG, with the wind speeds of the 6 WTs listed in Table 6.3 for three different time steps. The results are displayed in Fig. 6.7, where columns I and II show the results for the proposed architecture with the first and second control methods, respectively, while column III presents the results for the conventional P-WF

architecture. Fig. 6.7(a) illustrates the wind power captured by the 6 WTs in all three cases before any processing stages. During the first two time steps, the captured wind power is nearly identical in all cases. However, in the third time step, the P-WF captures the most wind power, followed by the SIP-WF with VPVC method, while the SIP-WF with CPVC method captures the least due to the weakest wind speed WT not contributing to power generation, as discussed earlier in this Chapter. The voltage levels for the three cases are shown in Fig. 6.7(b), where the proposed methods use the optimization algorithm to determine voltage, while the P-WF uses standard MPPT for each WT. Fig. 6.7(c) presents the pitch angles, which are controlled only below rated speed in the case of SIP-WF with VPVC method, leading to a faster wear of the WT mechanical parts. The DC currents are shown in Fig. 6.7(d), where the SIP-WF with VPVC method shows a current reduction in the third time step due to the optimization algorithm finding a feasible operating point for different wind speeds. Finally, the net output power of the WTG after processing stages in all cases is shown in Fig. 6.7(e). During the first two time-steps, the P-WF achieves the lowest net power (around 5.3 pu) due to its higher conversion stages and, consequently, higher losses compared to the SIP-WF that achieves around 5.8 pu. In the last time step, SIP-WF with VPVC method achieves nearly the same power as P-WF generating around 5 pu, while SIP-WF with CPVC method generates the least output around 4.6 pu due to the inactive contribution of the lowest wind speed WT.

6.5.2 DC Fault Scenario

In this scenario, the entire wind farm is assumed to be operating at rated wind speed, and a temporary DC fault is introduced at t = 2 s for 150 ms in the internal transmission line connecting the WTs of WTG 1 to the DC-DC converter as shown in Fig. 6.8. The DC current at the input side of the DC-DC converter is shown in Fig. 6.9(a). At the moment the fault occurs, the current briefly reverses direction to less than 2 pu due to the capacitors discharging through the fault, then gradually decreases without requiring any intervention from the controller, indicating the fault-tolerant capability of the proposed architecture. Meanwhile, the DC current at the rectifier side is depicted in Fig. 6.9(b), where the current increases up to 3 pu and then decreases slowly due to the action of the pitch control mechanism. It should be noted that at this side only uncontrolled rectifiers exist. Furthermore, in Fig. 6.9(c), the power outputs of all 10 WTGs are shown. It is evident that, upon the occurrence of the DC fault, only the power of WTG 1 drops to zero, while the other WTGs

continue to operate unaffected, demonstrating the ability of the proposed architecture to isolate the faulted section without disrupting the operation of the healthy sections.

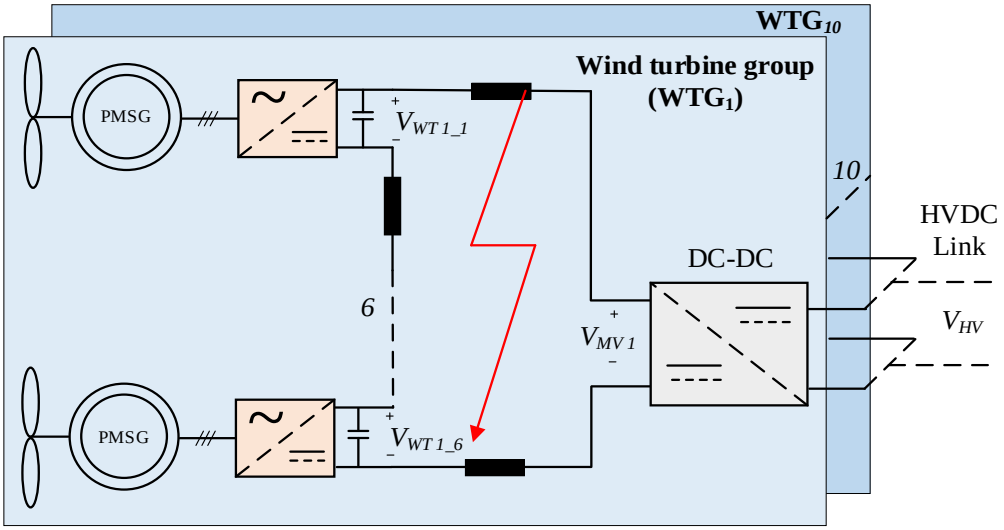
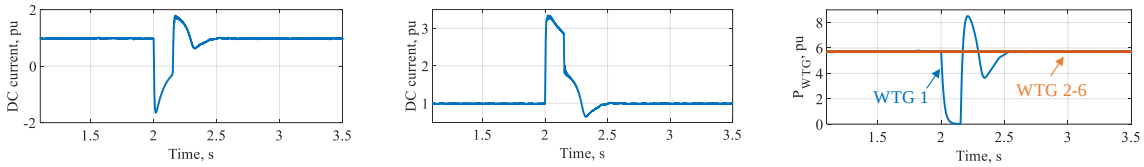


Fig. 6.8 Fault instant in the internal transmission line within WTG 1.



(a) (b) (c)

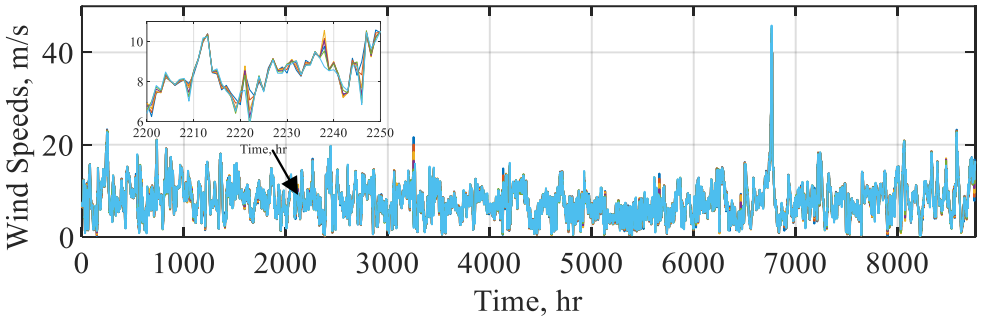
Fig. 6.9 DC fault simulation results of the proposed SIP-WF architecture: (a) DC current at the DC-DC converter input side, (b) DC current at the uncontrolled rectifiers side, (c) WTG DC powers.

6. 6 Comparison

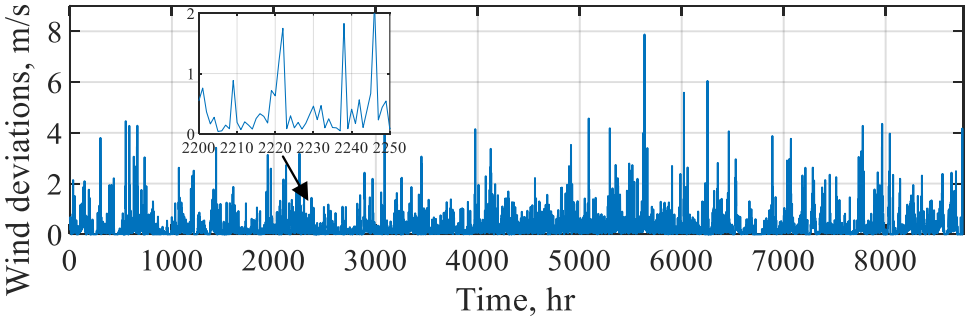
To further highlight the advantages of the proposed SIP-WF architecture and its control algorithms, CPVC and VPVC, a comparison is conducted with the conventional parallel wind farms (P-WF). The comparison is based on actual hourly wind speed data over a full year in the Gulf of Mexico [79]. The data covers a 5 km straight line, where 6 WTs are spaced 1 km apart. The hourly wind speeds for the entire year at the 6 WTs are shown in Fig. 6.10(a), while the wind speed difference between the two extremes is depicted in Fig. 6.10(b). It is clear that the wind speed differences can reach up to 8 m/s, though this is extremely rare; the average speed difference between the two extremes is 0.3 m/s. In the analysis, the power output from the WTs in P-WF is calculated using MPPT for each WT, while for the proposed

SIP-WF architecture, the control algorithms described earlier are used. The results of the comparison are summarised in Table **6.4**. Notably, the proposed SIP-WF architecture eliminates the need for a voltage boosting stage from the low-voltage (LV) level to the medium-voltage (MV) level, resulting in a significant reduction in the required LLC units. Specifically, the proposed SIP-WF requires only 30 MW of LLC units, compared to 60 MW in the P-WF, leading to lower semiconductor losses, reduced initial costs, and a smaller overall size and weight. The semiconductor losses percentages are calculated based on the method in [68], with current waveforms obtained via simulation.

Although, logically, the annual energy generated by the WTs in the P-WF is larger than that from both control methods of the SIP-WF, the P-WF has more conversion stages, resulting in higher losses. Consequently, the P-WF generates lower net annual energy than both of proposed SIP-WF control methods. Among these, the SIP-WF with VPVC method comes in the first place of achieving the highest net annual energy generation, followed by the SIP-WF with CPVC method.



(a)



(b)

Fig. 6.10 (a) Wind speeds for the 6 WTs per WTG, and (b) the maximum wind speed deviation among the WTG.

Table 6.4: SIP-WF and P-WF comparison results

Topologies	P-WF	SIP-WF	
No. of LLC converter units	(2×6+10) ×10 = 220	10×10 = 100	
Internal Transmission	0.65%	0.8%	
Semiconductor Loss	7.2%	4%	
Transformers Loss	2%	1%	
Total Losses	9.85%	5.8%	
Cost (pu)	1	0.5	
Weight & Size (pu)	1	0.5	
Control Variables	V_{dc}	V_{dc}	V_{dc}, β
Annual Energy generated (GWh)	95.444	93.987	94.9
Annual Energy loss (GWh)	9.401	5.464	5.515
Annual Net Energy (GWh)	86.043	88.738	89.385

6. 7 Summary

A novel DC Series-Isolated-Parallel wind farm (SIP-WF) architecture has been proposed in this Chapter. A detailed description of the SIP-WF architecture was provided, along with a mathematical analysis of the associated converters. Two control algorithms were developed for maximum power point tracking (MPPT) of the series-connected wind turbines (WTs) within each wind turbine group (WTG). The first control method adjusts only the voltage of the DC-DC converter, while the second method also adjusts the pitch angles (below the rated speed). The proposed architecture and its controllers were validated using a MATLAB SIMULINK model of a 300 MW wind farm system. Additionally, a comparison was carried out based on actual wind speed data for the two proposed control algorithms of the SIP-WF architecture and the conventional parallel wind farm (P-WF) architecture. Since the proposed SIP-WF architecture uses uncontrolled rectifiers instead of the first conversion stage found in P-WF, the initial cost, size, and weight of the system are reduced by nearly 50%. Although, the P-WF captures the highest annual energy, the SIP-WF with its two control methods generates higher net annual energy due to the reduced overall losses of the proposed architecture. The SIP-WF with pitch angle control increases annual energy generation by 3.88%. However, the frequent adjustment of pitch angles increases wear on the

mechanical components. On the other hand, the SIP-WF without pitch angle control still achieves a 3.13% increase in annual energy generation.

In conclusion, the proposed SIP-WF architecture offers lower overall losses, reduced initial cost, size, and volume, while also providing DC fault-blocking capability for each WTG. This makes it a promising candidate for future wind farm collection architectures

Chapter 7
Conclusions

7. 1 General Conclusions

This thesis has focused on advancing the power transmission capabilities of offshore wind turbines, with a particular emphasis on improving onshore HVDC converters and DC collection systems to address the challenges of efficiency, reliability, and cost-effectiveness. Offshore wind energy integration demands innovative solutions to manage the high-power transmission over long distances while maintaining system resilience against faults. This work introduced and evaluated novel converter topologies and collection architectures, demonstrating significant improvements in operational performance, fault tolerance, and economic feasibility. The findings contribute to enhancing the sustainability and scalability of offshore wind energy systems.

In Chapter 3, the first onshore HVDC power converter, named the Hybrid Thyristor-based Multilevel Converter (HTMC), was proposed. This converter utilizes antiparallel thyristors in series with mixed-cell submodules (SMs). A detailed analysis of its normal operation and DC fault response was conducted, and a full parameter design was developed and validated using MATLAB simulations and a hardware experimental test rig. A comparative study demonstrated that the HTMC achieves:

- 30% reduction in IGBT count compared to the next best topology.
- 30% lower conduction losses due to the use of thyristors.
- 19% cost reduction compared to lowest cost topology.

In Chapter 4, a second HVDC power converter, named the Fast DC Fault-Blocking HTMC (F-HTMC), was introduced. This design adds antiparallel thyristors in parallel with the upper SMs to provide faster DC fault-blocking capability. Key findings include:

- DC fault blocking within 1 ms, compared to 15 ms for the HTMC.

- While the F-HTMC has slightly higher IGBT count and losses than the HTMC, it offers smooth DC current flow eliminating the need for additional DC filters, resulting in reduced weight and volume.

Chapter 5 presented the third and final HVDC power converter, the Power Group Thyristor-based Multilevel Converter (PG-TMC), designed for HVDC power transmission. This power converter employs parallel branches of bidirectional thyristors with all SMs to form power groups. These thyristors provide a low-conduction path for current when the power group generates zero voltage, thereby reducing conduction losses. Key findings include:

- A detailed analysis of normal operation and DC fault-blocking mechanisms, along with control algorithms and parameter design.
- Validation through MATLAB simulations and hardware experiments.
- A comparative study with other power group-based converters revealed significant performance improvements:
    - 54% reduction in IGBT count.
    - 15.61% lower conduction losses.
    - 38.17% overall cost reduction.
    - 16.65% smaller volume and 14.95% lower weight compared to AT-AAC.

In Chapter 6, a novel DC Series-Isolated-Parallel Wind Farm (SIP-WF) architecture was developed for offshore wind turbine DC power collection, incorporating DC fault-tolerance capability. This architecture utilises parallel groups of wind turbines, with each group comprising series-connected wind turbines interfaced through uncontrolled rectifiers and a group-level DC-DC converter. Key features and findings include:

- A comprehensive description of the proposed architecture, supported by mathematical analysis and two control strategies to achieve maximum power point tracking (MPPT) for the wind turbine groups.
- Validation using MATLAB simulations and real wind data spanning an entire year.
- A comparative study with the traditional DC parallel wind farm architecture revealed:
    - 50% reduction in initial cost, size, and weight of the collection system.
    - An increase in annual energy generation by over 3% using the proposed architecture.

- The DC-DC converter isolate any faulted wind turbine group from the wind farm achieving high reliability.

In summary, this thesis has made significant strides in optimizing the design and operation of HVDC converters and DC collection systems for offshore wind farms, achieving improvements in cost, efficiency, size, and reliability. The proposed solutions address key challenges in offshore HVDC transmission and DC collection systems, contributing to the advancement of offshore wind energy integration.

7. 2 Author's contributions

- Proposed a hybrid thyristor-based multilevel converter (HTMC) with detailed architecture, operational analysis, and parameter design. The proposed converter demonstrated several notable advantages, including a significant reduction in IGBT count, lower conduction losses, and a considerable cost savings compared to existing topologies.
- Introduced the fast DC fault-blocking HTMC (F-HTMC), presenting its architecture, fault-blocking mechanism, and performance analysis. It achieved rapid DC fault-blocking within 1 ms and ensured smooth DC current flow, eliminating the need for additional DC filters.
- Designed the power group thyristor-based multilevel converter (PG-TMC) with innovative architecture and control algorithms, achieving a substantial reduction in IGBT count, lower conduction losses, significant cost savings, and reductions in both size and weight.
- Developed the series-isolated-parallel wind farm (SIP-WF) architecture for offshore wind turbines, incorporating DC fault-tolerance and presenting detailed mathematical modelling and control strategies. This architecture resulted in a notable decrease in initial cost, size, and weight, alongside an increase in annual energy generation compared to traditional designs.

- Designed and implemented two control strategies for the SIP-WF architecture to ensure maximum power point tracking (MPPT) under varying conditions.

7. 3 Future Work

- Investigate unidirectional HVDC (AC to DC) converters specifically designed for offshore wind energy power transmission and assess their performance against conventional bidirectional HVDC topologies. This would include analysing their operation and performance under real-world conditions, with a particular focus on how they compare to the commonly used bidirectional converters in terms of efficiency, power handling capacity, and operational stability. Such an investigation would provide deeper insights into the potential advantages and limitations of unidirectional systems, especially in terms of simplifying offshore power transmission and reducing the complexity of bidirectional power flows.

- Propose unidirectional HVDC converters that are optimized for offshore wind farm AC collection systems, focusing on efficiency and cost-effectiveness. These converters would be designed to optimize efficiency, reduce system costs, and ensure reliable operation in the dynamic environment of offshore wind farms. Such proposals could involve the introduction of innovative converter topologies that improve performance while minimizing both capital and operational expenditures, specifically addressing the unique requirements of offshore wind power transmission.

- Develop high-, medium-, and low-voltage DC-DC converters tailored for offshore wind farm DC collection systems to ensure efficient power transmission to shore. These converters would ensure efficient and stable power transmission to shore, minimizing losses and managing voltage fluctuations over long distances.

- Design and optimize DC-DC converters for series and series-parallel wind turbine configurations to improve efficiency and reduce system costs. These converters would be specifically optimized to handle the unique electrical characteristics and load requirements of such configurations, aiming to reduce energy losses, enhance power conversion efficiency, and lower the overall cost of the system. Research

in this area could also consider how these converters can enhance system resilience, particularly in fault conditions.

- Propose innovative DC collection system architectures utilizing series-connected wind turbines to improve efficiency, reliability, and fault isolation. These architectures would be designed to maximize system efficiency while ensuring that the system remains highly reliable, even under fault conditions. Key features could include advanced fault isolation techniques that prevent disruptions to the entire collection system and novel control strategies to enhance overall performance.

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Appendices

Appendix A: Experimental setup schematics

This appendix presents schematics of the main circuits used in the experimental setup. The setup for the proposed topology in Chapter 3 is a three-phase, five-level system, consisting of 12 half-bridge submodules, 6 full-bridge submodules, 6 antiparallel thyristors, a controller, a DC power supply, 3 voltage sensors, and 6 current sensors. For the proposed topology in Chapter 5, an additional 6 antiparallel thyristors were integrated into the system.

A.1 Half-Bridge Submodule

Fig. A.1 illustrates the schematic of two cascaded half-bridge submodules. The primary components include:

- **2 Optocouplers**: 6N139
- **2 Gate Drives:** IR2111
- **3 Isolated DC-DC Converters:** TME 1215S
- **2 IGBTs:** IRFP460

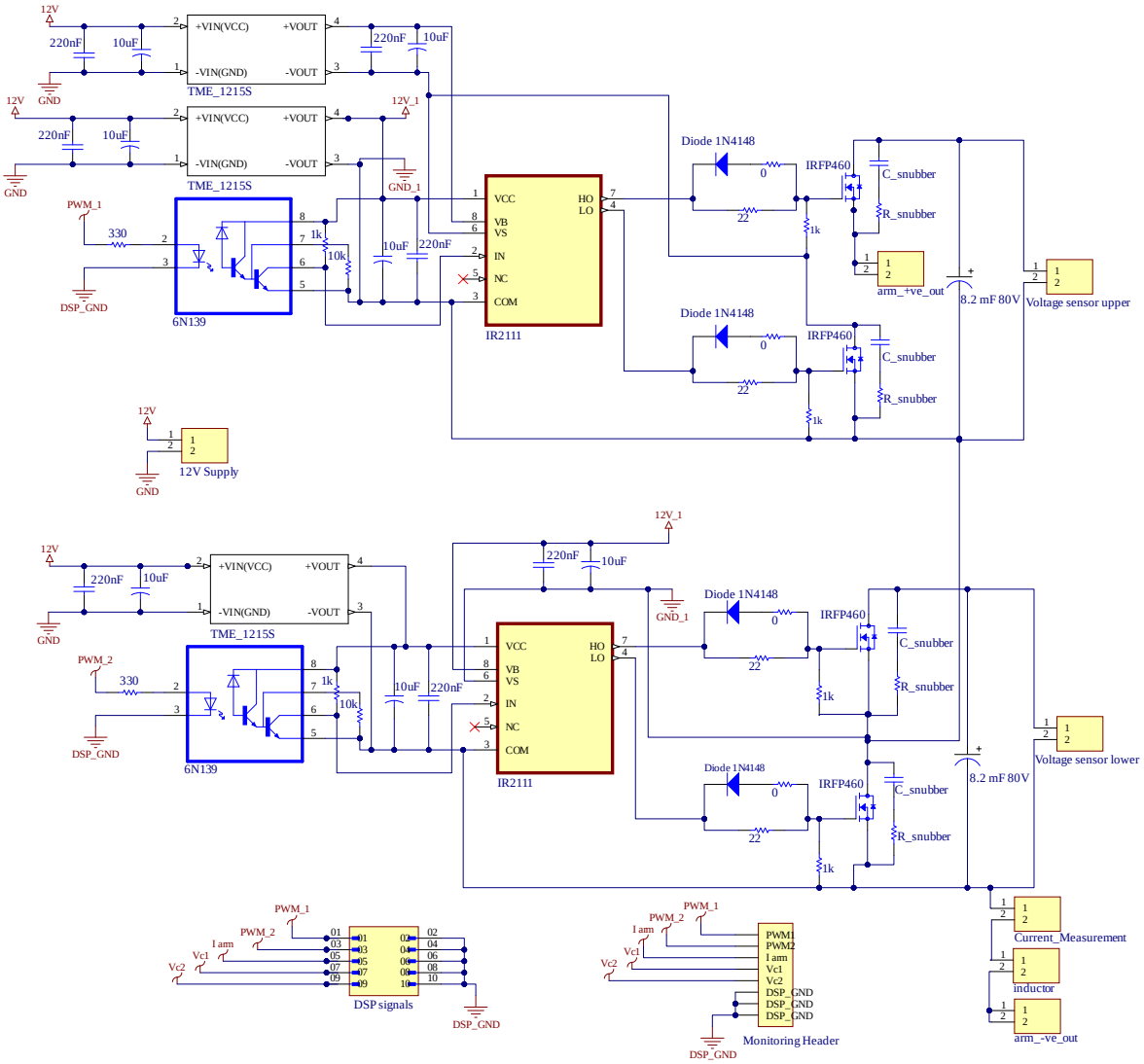

Fig. A.1 Two half bridge submodules schematic

A.2 Full-Bridge Submodule

Fig. A.2 depicts the schematic of a full-bridge submodule. The key components are:

- **2 Optocouplers:** 6N139
- **2 Gate Drives:** IR2111
- **3 Isolated DC-DC Converters:** TME 1215S (note that the connection points differ from those in the half-bridge submodule schematic)
- **4 IGBTs:** IRFP460

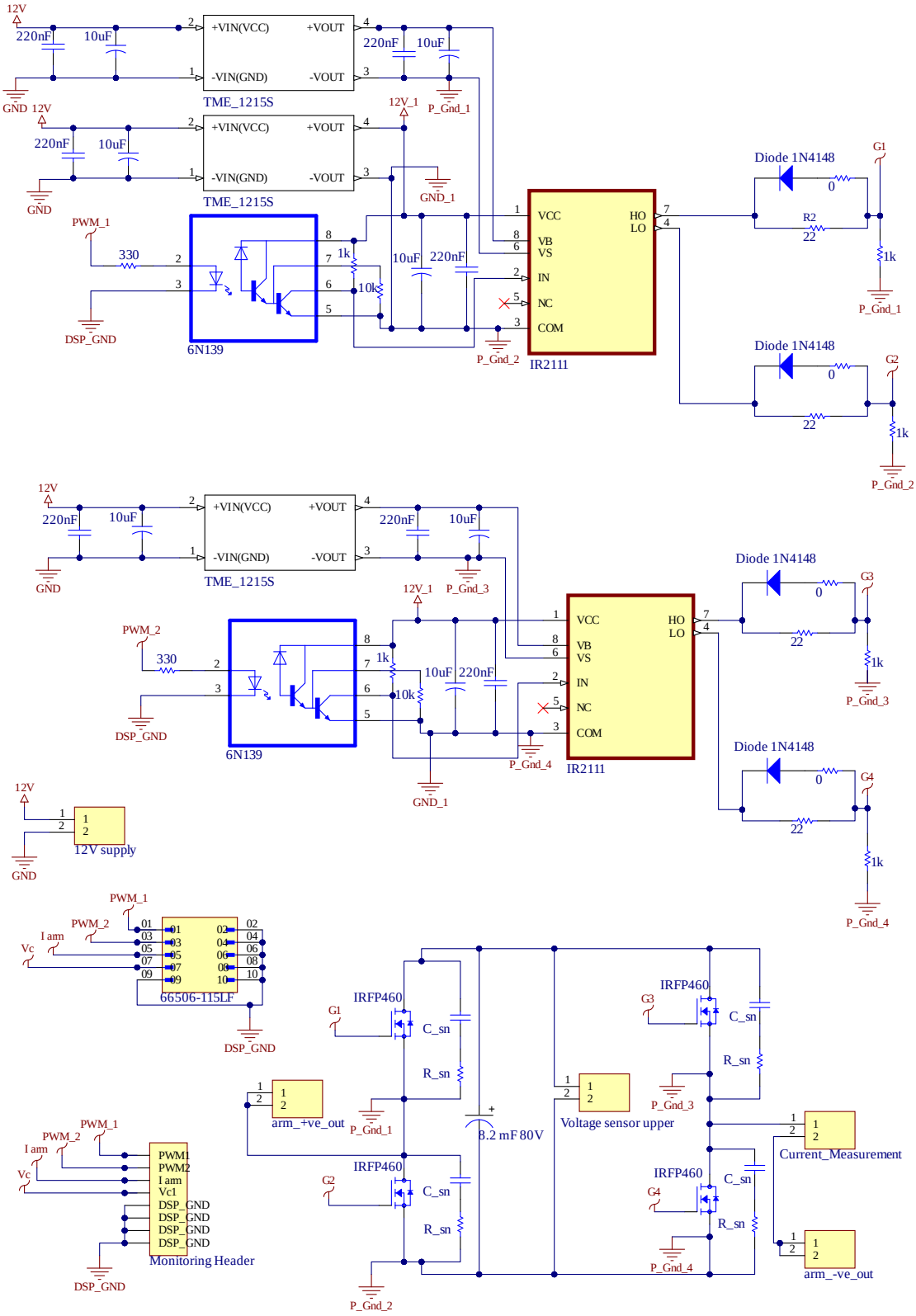

Fig. A.2 Full bridge submodule schematic

A.3 Antiparallel Thyristors

Fig. A.3 shows the schematic of antiparallel thyristors schematic. The primary components include:

- **2 Thyristor Drivers:** MOC3022
- **2 Thyristors:** TYN640RG

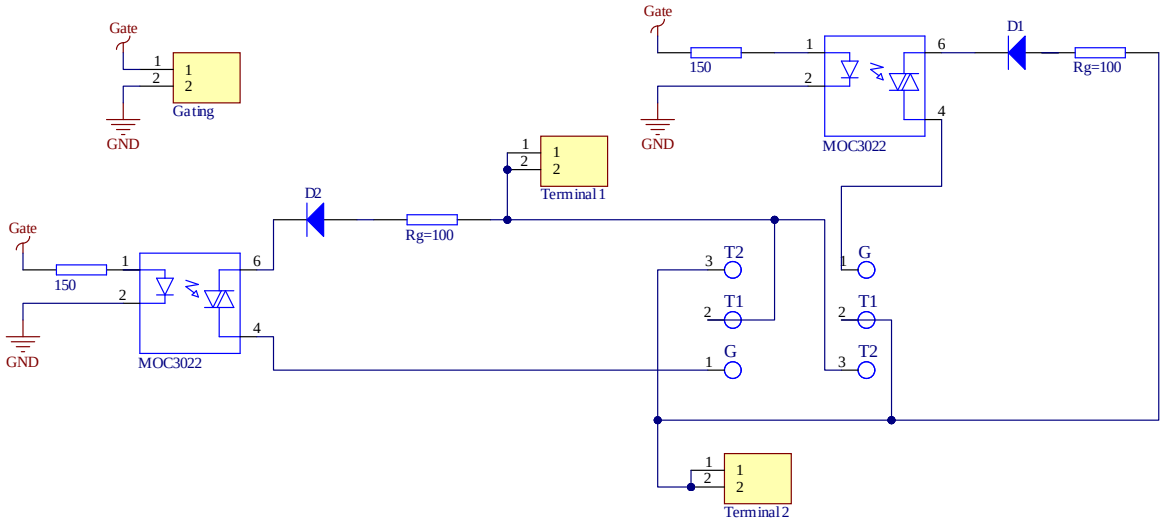

Fig. A.3 Antiparallel thyristors schematic

A.4 Voltage Sensors

Fig. A.4 illustrates the schematic for three voltage sensors used in the experimental setup. The components are:

- **3 Voltage Sensors:** LV 25-P
- **3 Operational Amplifiers:** TL071ACP
- **1 Isolated DC-DC converter:** TEN 5-1223 (used for ±15 voltage generation)

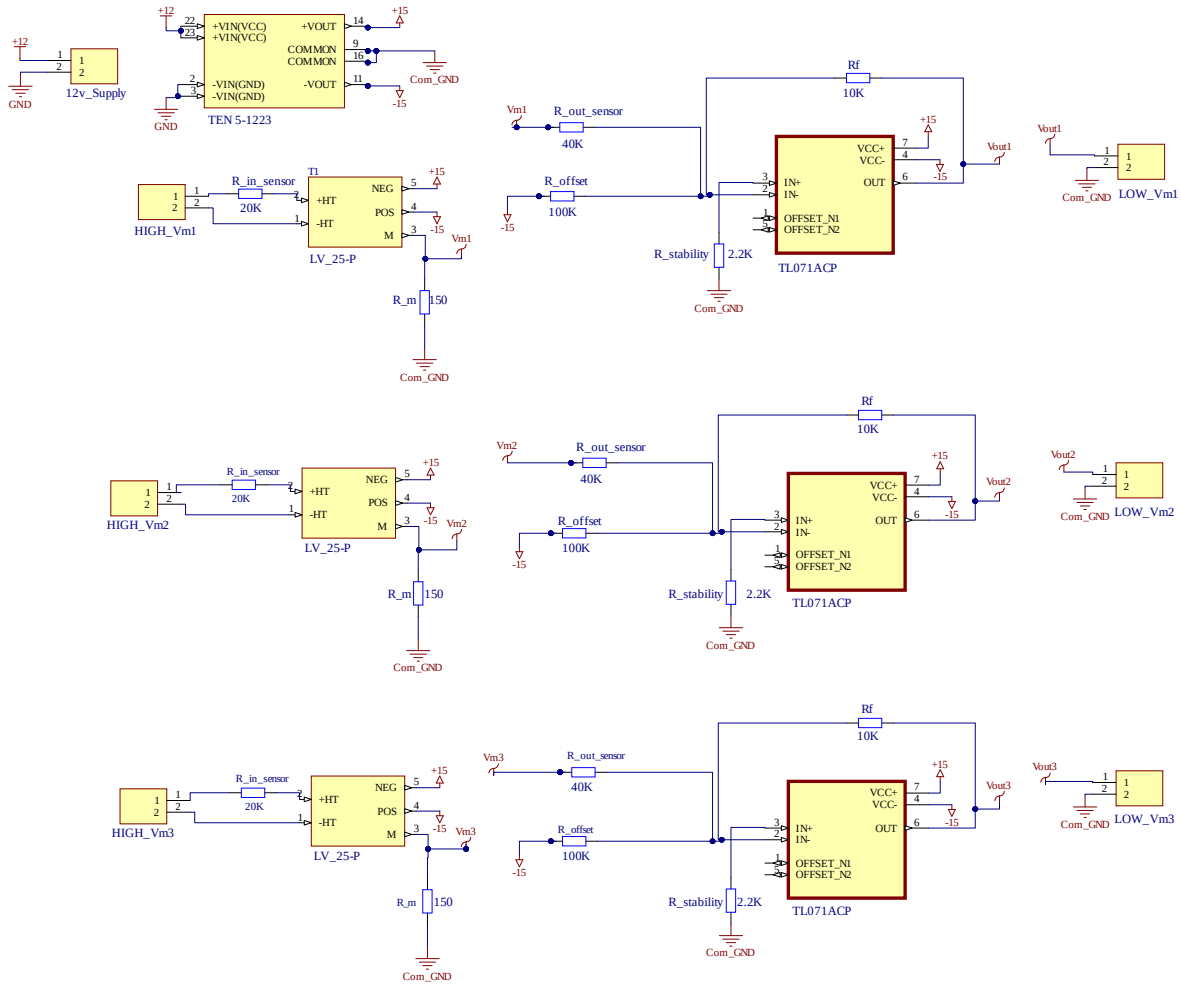

Fig. A.4 Voltage sensor schematic

A.5 Current Sensors

Fig. A.5 presents the schematic for three current sensors. The main components are as follows:

- **3 Current Sensors:** LA 25-P
- **3 Operational Amplifiers:** TL071ACP
- **1 Isolated DC-DC converter:** TEN 5-1223 (used for ±15 voltage generation)

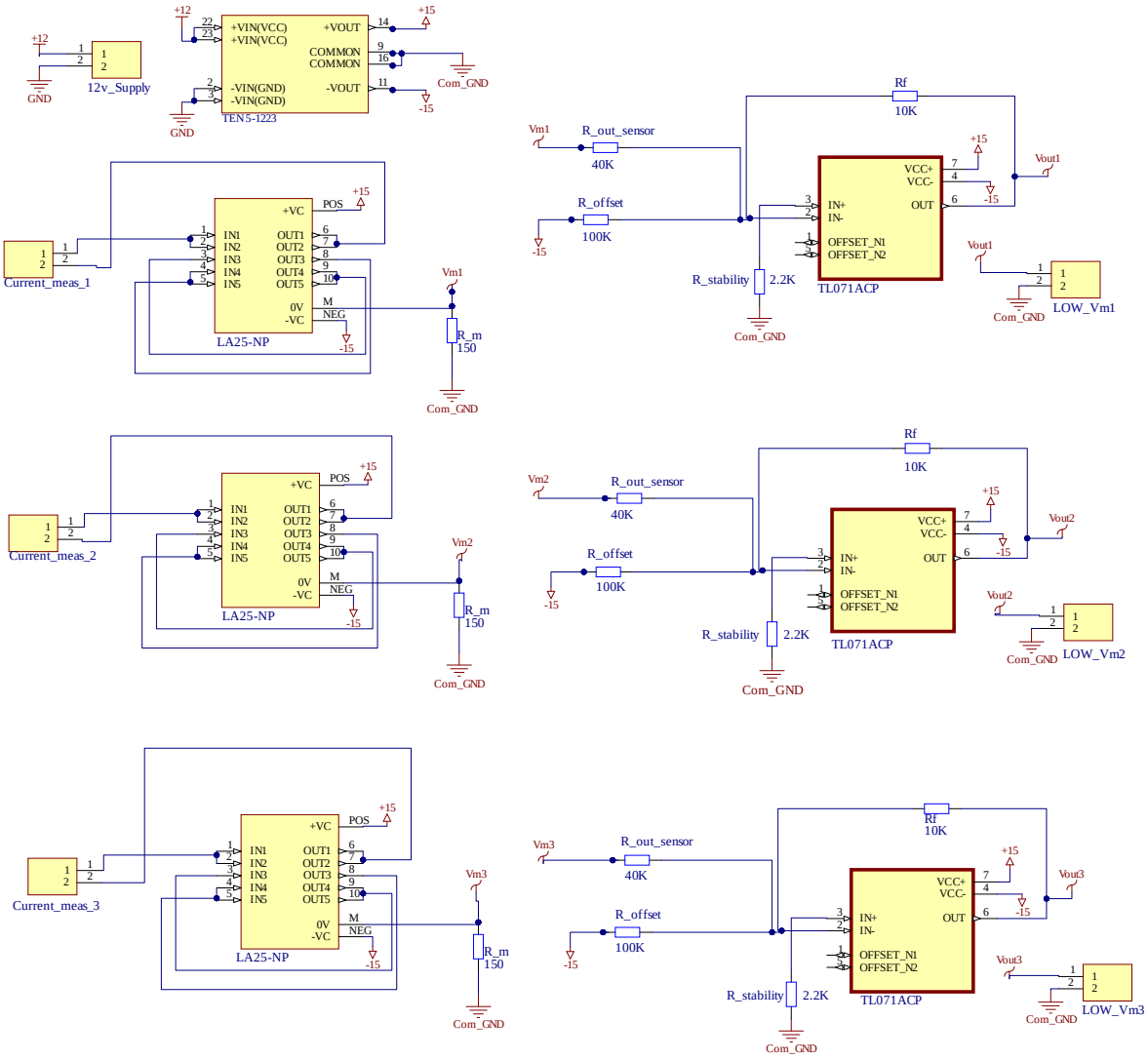

Fig. A.5 Current sensor schematic

A.6 LAUNCHXL-F28379D Interface Board

Fig. A.6 illustrates the schematic of the LAUNCHXL-F28379D interface board. The circuit includes various connectors for interfacing the driver circuits in the experimental setup with the LAUNCHXL-F28379D input/output boards.

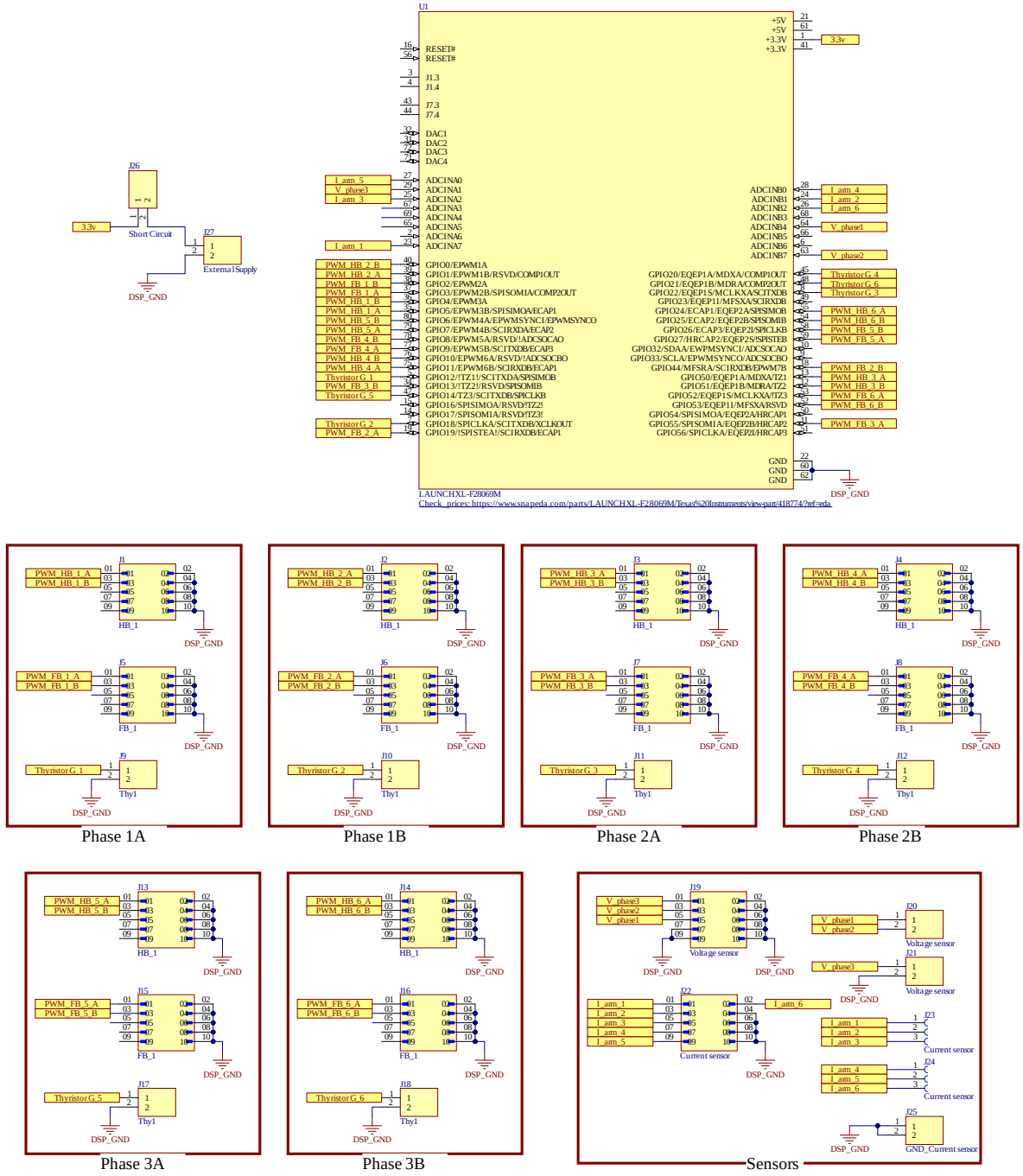

Fig. A.6 LAUNCHXL-F28379D interface board schematic

A.7 Dspace Interface Board

Fig. A.7 illustrates the schematic of the DSpace interface board. The circuit includes various connectors for interfacing the driver circuits in the experimental setup with the DSpace input/output boards.

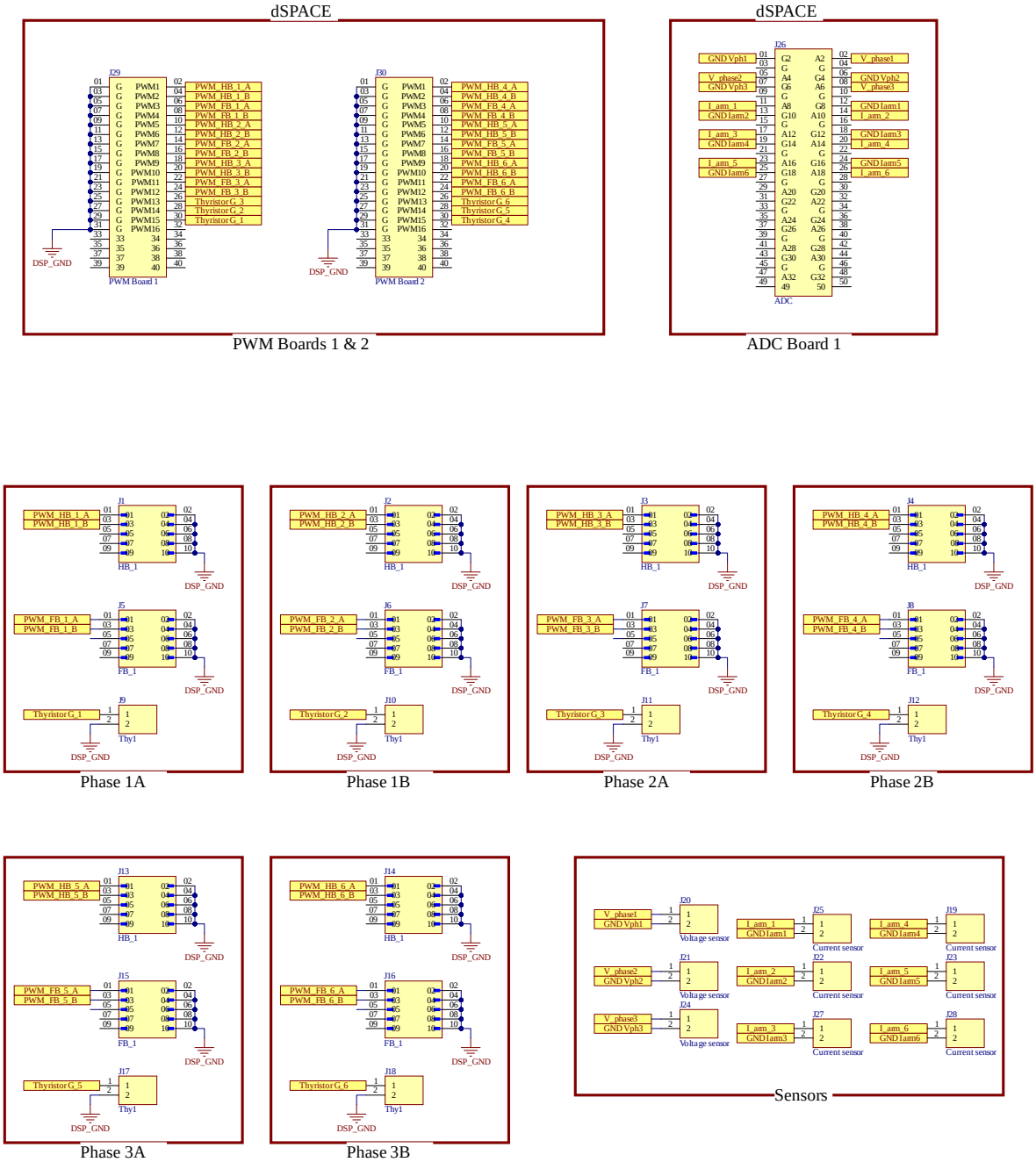

Fig. A.7 Dspace interface board schematic

Appendix B: Matlab Scripts

This appendix presents MATLAB scripts which calculates the conduction, switching, and inductor losses in a several HVDC converters. The calculations consider both semiconductor switching losses and conduction losses for both switches and diodes, as well as the resistive losses in the arm inductors.

B.1 Losses calculation of HB-MMC

% Initialization of the parameters

```
syms t
% System parameters
I_dc  = 1.5625e+03;    % DC current (A)
phi = 0 ;                % Phase shift (radians)
f_o = 50;                % Grid frequency (Hz)
w = 2 *pi*  f_o;         % Angular frequency (rad/s)
f_sw  = 250;             % Switching frequency (Hz)
V_ref  = 1800;           % IGBT Reference voltage (V)from datasheet
I_ref = 1800;            % IGBT Reference current (A)  from datasheet


% Energy losses per switching event (J)
E_on = 4300e-3;
E_off = 4000e-3;
E_rec = 2300e-3;

% Capacitor voltage (V)
Vc = 1600;

% Loss coefficients
ki_s = 1; kv_s = 1.3;
ki_d = 0.6; kv_d = 0.6;
```

```
% Number of submodules
N = 400;

% Arm parameters
R_arm = 0.0292;          % Arm resistance (ohms)
V_dc = 640e3;            % DC link voltage (V)

% Semiconductor parameters
Ucond_sw = 3.2;          % IGBT conduction voltage drop (V)
rcond_sw = 0.1e-3;       % IGBT conduction resistance (ohm)
Ucond_D = 2.65;          % Diode conduction voltage drop (V)
rcond_D = 0.1e-3;        % Diode conduction resistance (ohm)

% Modulation index
m = 1;

% Initialize index
i = 1;
```

% IGBT Duty cycle calculations

```
% Loop to compute current waveform over a switching cycle
for t0 = 0:0.0001:0.02
   i_p(i) = I_dc / 3 * (1 + (2 / (m * cos(phi))) * sin(w * t1(i) - phi));

   % Semiconductor voltage drops
   u_cond_s1 = Ucond_sw + abs(i_p(i) * rcond_sw);
   u_cond_s2 = Ucond_sw + abs(i_p(i) * rcond_sw);
   u_cond_D1 = Ucond_D + abs(i_p(i) * rcond_D);
```

```
u_cond_D2 = Ucond_D + abs(i_p(i) * rcond_D);

% Determine conduction states based on current direction
if (i_p(i) < 0)
    % Duty ratio calculation
    M_s1(i) = 0.5 * (1 - m * sin(w * t1(i)));
    M_D2(i) = 0.5 * (1 + m * sin(w * t1(i)));
    M_D1(i) = 0;
    M_s2(i) = 0;

    % Instantaneous conduction and switching losses
    pcond_inst_s1(i) = abs(u_cond_s1 * i_p(i) * M_s1(i));
    psw_inst_s1(i) = abs(f_sw * (E_on + E_off) * (Vc / V_ref)^kv_s * (i_p(i) / I_ref))^ki_s;
    pcond_inst_D2(i) = abs(u_cond_D2 * i_p(i) * M_D2(i));
    psw_inst_D2(i) = abs(f_sw * (E_rec) * (Vc / V_ref)^kv_d * (i_p(i) / I_ref))^ki_d;

    % No conduction in S2 and D1
    pcond_inst_D1(i) = 0; psw_inst_D1(i) = 0;
    pcond_inst_s2(i) = 0; psw_inst_s2(i) = 0;
else
    % Duty ratio calculation
    M_s1(i) = 0;
    M_D2(i) = 0;
    M_D1(i) = 0.5 * (1 - m * sin(w * t1(i)));
    M_s2(i) = 0.5 * (1 + m * sin(w * t1(i)));

    % Instantaneous conduction and switching losses
    pcond_inst_D1(i) = abs(u_cond_D1 * i_p(i) * M_D1(i));
    psw_inst_D1(i) = abs(f_sw * (E_rec) * (Vc / V_ref)^kv_d * (i_p(i) / I_ref))^ki_d;
    pcond_inst_s2(i) = abs(u_cond_s2 * i_p(i) * M_s2(i));
    psw_inst_s2(i) = abs(f_sw * (E_on + E_off) * (Vc / V_ref)^kv_s * (i_p(i) / I_ref))^ki_s;
```

```
        % No conduction in S1 and D2
        pcond_inst_s1(i) = 0; psw_inst_s1(i) = 0;
        pcond_inst_D2(i) = 0; psw_inst_D2(i) = 0;
    end

    % Arm inductor losses
    arm_inductor_losses(i) = i_p(i)^2 * R_arm;

    % Increment index
    i = i + 1;
end
```

%Average losses calculations

```
% Average conduction losses
pcond_avg_s1 = trapz(0.0001, pcond_inst_s1) / 0.02;
pcond_avg_s2 = trapz(0.0001, pcond_inst_s2) / 0.02;
pcond_avg_D1 = trapz(0.0001, pcond_inst_D1) / 0.02;
pcond_avg_D2 = trapz(0.0001, pcond_inst_D2) / 0.02;

% Average switching losses
psw_avg_s1 = trapz(0.0001, psw_inst_s1) / 0.02;
psw_avg_s2 = trapz(0.0001, psw_inst_s2) / 0.02;
psw_avg_D1 = trapz(0.0001, psw_inst_D1) / 0.02;
psw_avg_D2 = trapz(0.0001, psw_inst_D2) / 0.02;

% Average arm inductor losses
arm_inductor_losses_avg = trapz(0.0001, arm_inductor_losses) / 0.02;
```

% Total losses calculation

```
HBMMC_total_cond_losses = 6 * N * (pcond_avg_s1 + pcond_avg_s2 + pcond_avg_D1 + pcond_avg_D2);

HBMMC_total_sw_losses = 6 * N * (psw_avg_s1 + psw_avg_s2 + psw_avg_D1 + psw_avg_D2);

total_arm_inductor_losses_avg = arm_inductor_losses_avg * 6;

HBMMC_total_Losses = HBMMC_total_cond_losses + HBMMC_total_sw_losses + total_arm_inductor_losses_avg;

HBMMC_total_Losses_percentage = HBMMC_total_Losses / 1000e6 * 100;
```

B.2 Losses calculations of FB-MMC

% Initialization of the parameters

```
syms t;

% System parameters

I_dc = 1562.5;          % DC current (A)

phi = 0 * pi / 180;     % Phase shift (radians)

f_o = 50;               % Grid frequency (Hz)

w = 2 * pi * f_o;       % Angular frequency (rad/s)

f_sw = 250;             % Switching frequency (Hz)

V_ref = 1800;           % IGBT Reference voltage from datasheet (V)

I_ref = 1800;           % IGBT Reference current from datasheet (A)


% Energy losses per switching event (J)

E_on = 4.3e-3;

E_off = 4.0e-3;

E_rec = 2.3e-3;


% Submodule capacitor voltage (V)
```

```
Vc = 1600;

% Loss coefficients
ki_s = 1; kv_s = 1.3;
ki_d = 0.6; kv_d = 0.6;

% Converter parameters
N = 400;              % Total number of SMs per arm
V_dc = 640e3;         % DC link voltage (V)
R_arm = 0.0292;       % Arm resistance (ohms)

% Semiconductor voltage drops (V) and resistances (ohms)
Ucond_SW = 3.2;
rcond_SW = 0.1e-3;
Ucond_Diode = 2.65;
rcond_Diode = 0.1e-3;

% Number of submodules in different configurations
N_r = 400;
N_r_alt = 255;
N_r_dir = 0.5 * N_r;

% Modulation index
m = 1;

% IGBT Duty cycle calculations
i = 1;
% Loop to compute current waveform over a switching cycle
for t0 = 0:0.0001:0.02
   i_p(i) = I_dc / 3 * (1 + (2 / (m * cos(phi))) * sin(w * t1(i) - phi));
```

```
% Instantaneous conduction losses & Switching losses
u_cond_sw(i) = Ucond_SW + abs(i_p(i) * rcond_SW);
u_cond_D(i) = Ucond_Diode + abs(i_p(i) * rcond_Diode);

% FB-SMs duty cycles
if (i_p(i) < 0)
    % Active submodule switching states
    M_s1_FB(i) = 0.5 * (1 - m * sin(w * t1(i)));
    M_D1_FB(i) = 0;
    M_s2_FB(i) = 0;
    M_D2_FB(i) = 0.5 * (1 + m * sin(w * t1(i)));
    M_s4_FB(i) = 1;
    M_D4_FB(i) = 0;
else
    % Active submodule switching states
    M_s1_FB(i) = 0;
    M_D1_FB(i) = 0.5 * (1 - m * sin(w * t1(i)));
    M_s2_FB(i) = 0.5 * (1 + m * sin(w * t1(i)));
    M_D2_FB(i) = 0;
    M_s4_FB(i) = 0;
    M_D4_FB(i) = 1;
end

% Conduction losses
pcond_inst_s1_FB(i) = abs(u_cond_sw(i) * i_p(i) * M_s1_FB(i));
pcond_inst_s2_FB(i) = abs(u_cond_sw(i) * i_p(i) * M_s2_FB(i));
pcond_inst_D1_FB(i) = abs(u_cond_D(i) * i_p(i) * M_D1_FB(i));
pcond_inst_D2_FB(i) = abs(u_cond_D(i) * i_p(i) * M_D2_FB(i));
pcond_inst_s4_FB(i) = abs(u_cond_sw(i) * i_p(i) * M_s4_FB(i));
pcond_inst_D4_FB(i) = abs(u_cond_D(i) * i_p(i) * M_D4_FB(i));
```

```
    % Switching losses
    psw_inst_s1_FB(i) = abs(f_sw * (E_on + E_off) * (Vc / V_ref)^kv_s * (i_p(i) / I_ref))^ki_s;
    psw_inst_s2_FB(i) = abs(f_sw * (E_on + E_off) * (Vc / V_ref)^kv_s * (i_p(i) / I_ref))^ki_s;
    psw_inst_D1_FB(i) = abs(f_sw * E_rec * (Vc / V_ref)^kv_d * (i_p(i) / I_ref))^ki_d;
    psw_inst_D2_FB(i) = abs(f_sw * E_rec * (Vc / V_ref)^kv_d * (i_p(i) / I_ref))^ki_d;

    % Arm inductor losses
    arm_inductor_losses(i) = i_p(i)^2 * R_arm;

    i = i + 1;
end
```

%Average losses calculations

```
% Average conduction losses for FB-SMs
pcond_avg_s1_FB = trapz(0.0001, pcond_inst_s1_FB) / 0.02;
pcond_avg_s2_FB = trapz(0.0001, pcond_inst_s2_FB) / 0.02;
pcond_avg_D1_FB = trapz(0.0001, pcond_inst_D1_FB) / 0.02;
pcond_avg_D2_FB = trapz(0.0001, pcond_inst_D2_FB) / 0.02;
pcond_avg_s4_FB = trapz(0.0001, pcond_inst_s4_FB) / 0.02;
pcond_avg_D4_FB = trapz(0.0001, pcond_inst_D4_FB) / 0.02;

% Average switching losses for FB-SMs
psw_avg_s1_FB = trapz(0.0001, psw_inst_s1_FB) / 0.02;
psw_avg_s2_FB = trapz(0.0001, psw_inst_s2_FB) / 0.02;
psw_avg_D1_FB = trapz(0.0001, psw_inst_D1_FB) / 0.02;
psw_avg_D2_FB = trapz(0.0001, psw_inst_D2_FB) / 0.02;

% Average arm inductor losses
```

```
arm_inductor_losses_avg = trapz(0.0001, arm_inductor_losses) / 0.02;
```

% Total losses calculation

```
% Total losses for FB-SMs
FB_SMs_sw_losses = 6 * N_r * (psw_avg_s1_FB + psw_avg_s2_FB + psw_avg_D1_FB + psw_avg_D2_FB);
FB_SMs_cond_losses = 6 * N_r * (pcond_avg_s1_FB + pcond_avg_s2_FB + pcond_avg_D1_FB + pcond_avg_D2_FB);

% Total arm inductor losses
total_arm_inductor_losses_avg = arm_inductor_losses_avg * 6;

% Total losses in the converter
MMC_total_losses = FB_SMs_sw_losses + FB_SMs_cond_losses + total_arm_inductor_losses_avg;

% Loss percentage relative to 1 GW power
MMC_total_losses_percentage = MMC_total_losses / 1000e6 * 100;
```

B.3 Losses calculations of the hybrid MMC

% Initialization of the parameters

```
syms t;

% System parameters
I_dc = 1562.5;          % DC current (A)
phi = 0 * pi / 180;     % Phase shift (radians)
f_o = 50;               % Grid frequency (Hz)
w = 2 * pi * f_o;       % Angular frequency (rad/s)
f_sw = 250;             % Switching frequency (Hz)
V_ref = 1800;           % Reference voltage (V)
```

```
I_ref = 1800;           % Reference current (A)

% Energy losses per switching event (J)
E_on = 4.3e-3;
E_off = 4.0e-3;
E_rec = 2.3e-3;
% Submodule capacitor voltage (V)
Vc = 1600;

% Loss coefficients
ki_s = 1; kv_s = 1.3;
ki_d = 0.6; kv_d = 0.6;

% Converter parameters
N = 400;              % Total number of SMs per arm
V_dc = 640e3;         % DC link voltage (V)
R_arm = 0.0292;       % Arm resistance (ohms)

% Semiconductor voltage drops (V) and resistances (ohms)
Ucond_SW = 3.2;
rcond_SW = 0.1e-3;
Ucond_Diode = 2.65;
rcond_Diode = 0.1e-3;

% Number of submodules in different configurations
N_r = 400;
N_r_FB = 0.5 * N_r;  % Full-Bridge SMs
N_r_HB = 0.5 * N_r;  % Half-Bridge SMs

% Modulation index
m = 1;
```

```
% IGBT Duty cycle calculations
i = 1;
% Loop to compute current waveform over a switching cycle
for t0 = 0:0.0001:0.02
   i_p(i) = I_dc / 3 * (1 + (2 / (m * cos(phi))) * sin(w * t1(i) - phi));

   % Instantaneous conduction losses & Switching losses
   u_cond_sw(i) = Ucond_SW + abs(i_p(i) * rcond_SW);
   u_cond_D(i) = Ucond_Diode + abs(i_p(i) * rcond_Diode);

   % HB-SMs duty cycles
   if (i_p(i) < 0)
      M_s1(i) = 0.5 * (1 - m * sin(w * t1(i)));
      M_D1(i) = 0;
      M_s2(i) = 0;
      M_D2(i) = 0.5 * (1 + m * sin(w * t1(i)));

      % FB-SMs duty cycles
      M_s1_FB(i) = 0.5 * (1 - m * sin(w * t1(i)));
      M_D1_FB(i) = 0;
      M_s2_FB(i) = 0;
      M_D2_FB(i) = 0.5 * (1 + m * sin(w * t1(i)));
      M_s4_FB(i) = 1;
      M_D4_FB(i) = 0;
   else
      % HB-SMs duty cycles
      M_s1(i) = 0;
      M_D1(i) = 0.5 * (1 - m * sin(w * t1(i)));
      M_s2(i) = 0.5 * (1 + m * sin(w * t1(i)));
```

```
        M_D2(i) = 0;

        % FB-SMs duty cycles
        M_s1_FB(i) = 0;
        M_D1_FB(i) = 0.5 * (1 - m * sin(w * t1(i)));
        M_s2_FB(i) = 0.5 * (1 + m * sin(w * t1(i)));
        M_D2_FB(i) = 0;
        M_s4_FB(i) = 0;
        M_D4_FB(i) = 1;
    end

    arm_inductor_losses(i) = i_p(i)^2 * R_arm;
    i = i + 1;
end
```

%Average losses calculations

```
% Average conduction losses for HB-SMs
pcond_avg_s1 = trapz(0.0001, pcond_inst_s1) / 0.02;
pcond_avg_s2 = trapz(0.0001, pcond_inst_s2) / 0.02;
pcond_avg_D1 = trapz(0.0001, pcond_inst_D1) / 0.02;
pcond_avg_D2 = trapz(0.0001, pcond_inst_D2) / 0.02;

% Average switching losses for HB-SMs
psw_avg_s1 = trapz(0.0001, psw_inst_s1) / 0.02;
psw_avg_s2 = trapz(0.0001, psw_inst_s2) / 0.02;
psw_avg_D1 = trapz(0.0001, psw_inst_D1) / 0.02;
psw_avg_D2 = trapz(0.0001, psw_inst_D2) / 0.02;

% Average conduction losses for FB-SMs
pcond_avg_s1_FB = trapz(0.0001, pcond_inst_s1_FB) / 0.02;
```

```
pcond_avg_s2_FB = trapz(0.0001, pcond_inst_s2_FB) / 0.02;
pcond_avg_D1_FB = trapz(0.0001, pcond_inst_D1_FB) / 0.02;
pcond_avg_D2_FB = trapz(0.0001, pcond_inst_D2_FB) / 0.02;

% Average switching losses for FB-SMs
psw_avg_s1_FB = trapz(0.0001, psw_inst_s1_FB) / 0.02;
psw_avg_s2_FB = trapz(0.0001, psw_inst_s2_FB) / 0.02;
psw_avg_D1_FB = trapz(0.0001, psw_inst_D1_FB) / 0.02;
psw_avg_D2_FB = trapz(0.0001, psw_inst_D2_FB) / 0.02;

% Average arm inductor losses
arm_inductor_losses_avg = trapz(0.0001, arm_inductor_losses) / 0.02;
```

%%Total Losses Calculation

```
% Total losses for HB-SMs
HB_SMs_sw_losses = 6 * N_r_HB * (psw_avg_s1 + psw_avg_s2 + psw_avg_D1 + psw_avg_D2);
HB_SMs_cond_losses = 6 * N_r_HB * (pcond_avg_s1 + pcond_avg_s2 + pcond_avg_D1 + pcond_avg_D2);

% Total losses for FB-SMs
FB_SMs_sw_losses = 6 * N_r_FB * (psw_avg_s1_FB + psw_avg_s2_FB + psw_avg_D1_FB + psw_avg_D2_FB);
FB_SMs_cond_losses = 6 * N_r_FB * (pcond_avg_s1_FB + pcond_avg_s2_FB + pcond_avg_D1_FB + pcond_avg_D2_FB);

% Total arm inductor losses
total_arm_inductor_losses_avg = arm_inductor_losses_avg * 6;

% Total losses in the converter
MMC_total_losses = FB_SMs_sw_losses + FB_SMs_cond_losses + HB_SMs_sw_losses + HB_SMs_cond_losses + total_arm_inductor_losses_avg;
```

```
% Loss percentage relative to 1 GW power
MMC_total_losses_percentage = MMC_total_losses / 1000e6 * 100;
```

B.4 Losses calculation of HTMC (proposed in Chapter 3).

% Initialization of the parameters

```
syms t;

% System parameters
I_dc = 1.5625e+03;      % DC current (A)
phi = 0 * pi / 180;     % Phase shift (radians)
f_o = 50;               % Grid frequency (Hz)
w = 2 * pi * f_o;       % Angular frequency (rad/s)
f_sw = 250;             % Switching frequency (Hz)
V_ref = 1800;           % IGBT Reference voltage (V) from datasheet
I_ref = 1800;           % IGBT Reference current (A) from datasheet

% Energy losses per switching event (J)
E_on = 4300e-3;
E_off = 4000e-3;
E_rec = 2300e-3;

% Submodule capacitor voltage (V)
Vc = 1600;

% Loss coefficients
ki_s = 1; kv_s = 1.3;
ki_d = 0.6; kv_d = 0.6;
% Converter parameters
N = 400;            % Total number of SMs per arm
```

```
R_arm = 0.008;          % Arm resistance (ohms)
R_filter = 0.017;       % Filter resistance (ohms)
V_dc = 640e3;           % DC link voltage (V)

% Thyristor parameters
E_on_thy = 300e-3;
E_off_thy = 4200e-3;
N_thy = 100;

% Number of submodules
N_r = 400;
N_r_HB = 0.5 * N_r;
N_r_FB = 0.5 * 0.2 * N_r;  % k = 0.2

% Semiconductor voltage drops (V) and resistances (ohm)
Ucond_SW = 3.2;
rcond_SW = 0.1e-3;
Ucond_Diode = 2.65;
rcond_Diode = 0.1e-3;
Ucond_thy = 1.84;
rcond_thy = 0.647e-3;

% Modulation index
m = 1;
```

%IGBT Duty cycle calculations

```
i = 1;
% Loop to compute current waveform over a switching cycle
for t0 = 0:0.0001:0.02
    vac_ref(i) = sin(w * t1(i));
```

```
    % Upper arm current
    if (vac_ref(i) >= 0)
        i_p(i) = 4 * I_dc / (3 * cos(phi)) * sin(w * t1(i) - phi);
        v_p(i) = 0.5 * V_dc * (1 - (sin(w * t1(i)) - 0.2 * sin(3 * w * t1(i))));
    else
        i_p(i) = 0;
        v_p(i) = 0.5 * (1 + 0.2) * V_dc;
    end

    % Instantaneous conduction losses & Switching losses
    u_cond_sw(i) = Ucond_SW + abs(i_p(i) * rcond_SW);
    u_cond_D(i) = Ucond_Diode + abs(i_p(i) * rcond_Diode);
    u_cond_thy(i) = Ucond_thy + abs(i_p(i) * rcond_thy);

    % Duty cycle computation for HB-SMs, FB-SMs, and thyristors
    if (v_p(i) >= 0)
        % HB and FB submodules in different switching states
        if (i_p(i) < 0)
            % Assigning duty cycles for conduction states
            M_thy(i) = 1;
        else
            M_thy(i) = 1;
        end
    end

    % Inductor losses
    arm_inductor_losses(i) = i_p(i)^2 * R_arm;

    i = i + 1;
end
```

%Average losses calculations

% Average conduction losses for HB-SMs

pcond_avg_s1_HB = trapz(0.0001, pcond_inst_s1_HB) / 0.02;

pcond_avg_s2_HB = trapz(0.0001, pcond_inst_s2_HB) / 0.02;

pcond_avg_D1_HB = trapz(0.0001, pcond_inst_D1_HB) / 0.02;

pcond_avg_D2_HB = trapz(0.0001, pcond_inst_D2_HB) / 0.02;

% Average conduction losses for FB-SMs

pcond_avg_s1_FB = trapz(0.0001, pcond_inst_s1_FB) / 0.02;

pcond_avg_s2_FB = trapz(0.0001, pcond_inst_s2_FB) / 0.02;

pcond_avg_s3_FB = trapz(0.0001, pcond_inst_s3_FB) / 0.02;

pcond_avg_s4_FB = trapz(0.0001, pcond_inst_s4_FB) / 0.02;

% Average conduction losses for thyristors

pcond_avg_thy = trapz(0.0001, pcond_inst_Thy) / 0.02;

% Average arm inductor losses

arm_inductor_losses_avg = trapz(0.0001, arm_inductor_losses) / 0.02;

%Total losses calculations

% Total losses for HB-SMs

HB_SMs_sw_losses = 6 * N_r_HB * (psw_avg_s1_HB + psw_avg_s2_HB);

HB_SMs_cond_losses = 6 * N_r_HB * (pcond_avg_s1_HB + pcond_avg_s2_HB);

% Total losses for FB-SMs

FB_SMs_sw_losses = 6 * N_r_FB * (psw_avg_s1_FB + psw_avg_s2_FB + psw_avg_s3_FB + psw_avg_s4_FB);

FB_SMs_cond_losses = 6 * N_r_FB * (pcond_avg_s1_FB + pcond_avg_s2_FB + pcond_avg_s3_FB + pcond_avg_s4_FB);

```
% Total losses for thyristors
Thy_sw_losses = 6 * N_thy * (psw_avg_thy);
Thy_cond_losses = 6 * N_thy * (pcond_avg_thy);

% Total arm inductor losses
total_arm_inductor_losses_avg = arm_inductor_losses_avg * 6;

% Total losses in the converter
total_losses = HB_SMs_sw_losses + HB_SMs_cond_losses + FB_SMs_sw_losses + ...
        FB_SMs_cond_losses + Thy_sw_losses + Thy_cond_losses + ...
        total_arm_inductor_losses_avg + R_filter * I_dc^2;

% Loss percentage relative to 1 GW power
total_losses_percentage = total_losses / 1000e6 * 100;
```