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Current Source Based Wind Energy Conversion
System

by

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A thesis presented in fulfilment of the requirements for the
degree of Doctor of Philosophy

June 2015

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Acknowledgements

I would like to express my deep gratefulness to my supervisors Prof. Barry W. Williams, Dr.Derrick Holliday and Dr. Grain P. Adam for their extensive guidance, continuous support, kind advice, helpful comments and capable supervision which helped this work to be in its present form.

I also would like to acknowledge staff and colleagues in the Department of Electronic and Electrical Engineering in University of Strathclyde for their assistance and support during the years of research.

I would like to thank Arab Academy for Science and Technology and Maritime Transport, Cairo, Egypt for funding my PhD.

Finally, a heartfelt gratitude goes to my beloved parents, my wife and my children for all the sacrifices they had to make to see this through to the end and for their prayers and encouragement.

Ibrahim Abdallah

Abstract

This thesis considers the use of a full-scale back-to-back pulse width modulated current source converter (BTB-PWM-CSC) as an interfacing converter for a variable-speed wind energy conversion system (WECS) that uses a permanent magnet synchronous generator (PMSG). It has been shown that the proposed current source converter based WECS can operate successfully under maximum power point tracking and meet all grid requirements such as ac fault ride-through and power quality aspects at the point of common coupling. This thesis presents three different CSC based WECSs.

The first WECS is based on a back-to-back dual pulse width modulated current source converter (BTB-DPWM-CSC) as an interface for a dual three-phase PMSG, with two stator windings, shifted by 30° . Both the generator and grid side dual PWM rectifier and inverters (CSR and CSI) of the WECS are controlled using selective harmonic elimination (SHE) for low semiconductor loss operation. The grid side CSI is connected to the ac grid through a three-winding phase-shift transformer to benefit from cancellation of the low-order harmonics in the primary winding, which is connected to the ac grid side. The secondary and tertiary windings, which are connected to the upper and lower halves of the dual PWM-CSI, are delta and wye connected; thus, SHE is only needed to eliminate the 11th and 13th harmonics. The SHE modulation employed to control both the dual PWM-CSR and CSI has one unique pattern, which is characterised by continuous pulse angle changes and a fixed switching frequency over the full modulation index range. These attributes show that the proposed BTB-DPWM-CSC WECS is suited for multi-megawatt applications.

The second and third WECSs are based on modified three-phase and dual three-phase BTB-PWM-CSCs. These configurations are developed to address the main drawbacks of the conventional CSC employed in the first proposal, such as transient over-voltages experienced by the converter switches during commutation and semiconductor loss reduction. The latter is achieved by using a dedicated high frequency synchronization method that ensures zero current switching at the CSI terminal; thus, nearly zero switching loss is achieved. The proposed WECSs offer the

following additional advantages: reduced power circuit and control complexity; reduced switching frequency; applicable to fixed and variable frequency operation, hence, allowing maximum power point tracking with independent control of active and reactive powers delivered to the ac grid; and low-voltage ride-through capability.

Viability of the proposed WECSs are assessed using simulations performed in PSCAD/EMTDC and confirmed experimental, with results from scaled down prototypes, assessed in steady-state and dynamically under different operating conditions. It is shown that continuous and discontinuous operation of the second and third configurations provide trade-offs between overall weight and size of the WECS and high current and voltage stresses in the semiconductor switches.

List of Symbols

$\theta_1, \theta_2, \theta_3$	selective harmonics elimination angles ($^\circ$)
ω	supply frequency (rad/s)
ω_B	base frequency (rad/s)
ω_e	electrical rotating speed of the generator (rad/s)
ω_m	mechanical angular speed (rad/s)
ω_{opt}	optimal wind turbine rotational speed (rad/s)
α	phase angle of CSI output current
δ	duty cycle
ψ	flux linkage (wb)
Φ	flux (wb)
ϕ_{m1}, ϕ_{m2}	magnetization flux
μ_0	absolute permeability ($\mu_0=4\pi\times 10^{-7}$ H/m)
μ_r	core relative permeability (H/m)
\mathfrak{R}	magnetic path reluctance (H^{-1})
ρ	air density (1.225 kg/m ³)
β	blade pitch angle ($^\circ$)
λ	tip speed ratio
λ_{opt}	optimal tip speed ratio
A	cross-section area (m ²)
C_{dc}	dc-side capacitance (μF)
C_B	base capacitance (μF)
C_p	power coefficient
F_{coup}	maximum magnetic coupling coefficient between the rotor and stator (wb)
f	supply frequency (Hz)
f_{sr}	switching frequency(Hz)
$g_{m1} - g_{m6}$	switch state of the current source converter after the mapping circuit
I_{dc}	dc-link current (A)
I_L	dc-link inductance current (A)
I_s	switch current (A)
I_i	current source inverter input current (A)
i_{ia}, i_{ib}, i_{ic}	CSI output currents (A)
i_{ca}, i_{cb}, i_{cc}	ac side filter capacitor current (A)
i_{Ld}, i_{Lq}	d-q components of the terminal current (A)
i_{La}, i_{Lb}, i_{Lc}	three-phase load current (A)
i_{sd}, i_{sq}	dq components of the supply current (A)
L_B	base inductance (H)
$L_{D:}$	constant amplitude self-inductance of the D-damper winding (H)
L_{dc}	dc-link inductance (H)
$L_{f:}$	constant amplitude self-inductance of the field winding (H)
L_s	self-inductance (H)
L_L	load inductance (H)
L_m	mutual-inductance (H)
$L_{Q:}$	constant amplitude self-inductance of the Q-damper winding (H)
L_{ss}	represent the stator self and mutual inductance (H)
L_{sr}, L_{rs}	represent the stator and rotor mutual inductances (H)
l	length of the equivalent magnetic path (m)
$M_{D:}$	mutual inductance amplitude between armature and D-damper windings (H)
M_f	mutual inductance between armature winding and field winding (H)
$M_{Q:}$	inductance amplitude between armature winding and Q-damper winding (H)
m	modulation index
m_d, m_q	d-q components of the modulation index
N_1, N_2, N_3	transformer turns ratio
P_g	grid delivered active power (W)
P_g^*	grid active power reference (W)

R_D	<i>D-damper winding resistance (Ω)</i>
R_f	<i>field winding resistance (Ω)</i>
R_L	<i>load resistance (Ω)</i>
R_Q	<i>Q-damper winding resistance (Ω)</i>
R_s	<i>stator winding resistance (Ω)</i>
$S_1 - S_6$	<i>represent the CSI switch state</i>
S_r	<i>rectifier side switch</i>
T	<i>switching period (s)</i>
T_e :	<i>electromagnetic torque (Nm)</i>
T_m :	<i>mechanical torque (Nm)</i>
t :	<i>time in seconds (s)</i>
t_{on}	<i>dwelt time of the switch within each switching cycle (s)</i>
t_{off}	<i>off time of the switch within each switching cycle (s)</i>
\tilde{Q}	<i>grid reactive power (VAr)</i>
Q_g^*	<i>grid reactive power reference (VAr)</i>
V	<i>wind speed (m/s)</i>
V_{dc}	<i>dc output voltage(V)</i>
V_{in}	<i>CSI input terminal voltage(V)</i>
V_m	<i>peak phase voltage (V)</i>
v_{cr}	<i>peak values of the carrier waves (V)</i>
v_{La}, v_{Lb}, v_{Lc}	<i>three-phase load voltage (V)</i>
v_{Ld}, v_{Lq}	<i>dq components of the terminal voltages (V)</i>
v_{sd}, v_{sq}	<i>dq components of the supply voltage (V)</i>
Z_B	<i>base impedance</i>

List of Abbreviations

BC	Boost Converter
BTB	Back to Back
CCM	Continues Conduction Mode
CO ₂	Carbon Dioxide
CSC	Current Source Converter
CSI	Current Source Inverter
DSP	Digital Signal Processor
CSR	Current Source Rectifier
DCM	Discontinues Conduction Mode
DFIG	Doubly Fed Induction Generator
DPWM	Dual Pulse width Modulated
EESG	Electrically Excited Synchronous Generator
FFT	Fast Fourier Transform
GBR	Gear Box Ratio
HAWTs	Horizontal Axis Wind Turbines
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
LVRT	Low-Voltage Ride-Through
MPPT	Maximum Power Point Tracking
PCC	Point of Common Coupling
PI	Proportional Integral
PFC	Power Factor Correction
PLL	Phase Locked Loop
PM	Permanent Magnet
PMSG	Permanent Magnet Synchronous Generator
PSCAD/EMTDC	Power System Computer Aided Design / Electromagnetic Transients Including DC
PWM	Pulse Width Modulated
PV	Photovoltaic
UPS	Uninterruptible Power Supply
SCIG	Squirrel-Cage Induction Generator
SG	Synchronous Generator
SHE	Selective Harmonics Elimination
SMES	Superconducting Magnetic Energy Storage
SPWM	Sinusoidal Pulse Width Modulation
SR	Switch Resolution
STATCOM	Static Synchronous Compensator
SVM	Space Vector Modulation
THD	Total Harmonics Distortion
VAWTs	Vertical Axis Wind Turbines
VSC	Voltage Source Converter
WECS	Wind Energy Conversion System
WLSE	Weighted Least-Squares Estimation
WRIG	Wounded Rotor Induction Generator
WTE	Wind Turbine Emulator
ZCS	Zero Current Switching
ZSI	Z-Source Inverter

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Chapter 1. Introduction

The rapid increase in the demand for electrical power in recent years is an indicator of civilization, as the world's population continues to migrate from villages to cities, creating so called megacities. Fossil fuels, coal, natural gas and liquid fuel are main sources of electrical energy; however, these energy sources are not renewable and will eventually be exhausted. Additionally, these energy sources are considered to be the major contributor to global warming and environmental degradation. Although nuclear power is reliable and economically competitive for electricity generation, it has national security and long term environmental concerns, exacerbated by events like the Fukushima nuclear disaster in Japan, 2011. In response to these concerns, renewable energy such as: wind energy, solar energy and hydraulic energy have become more attractive, and as evidence, countries such as Germany have abandoned nuclear energy in favour of renewable energy. Wind energy is a clean sustainable energy source, and today it is one of the most rapidly growing renewable energy source being exploited for electricity generation [1, 2].

Power electronics plays an important role in a wind energy conversion system (WECS), and has been used intensively in fixed-speed and variable-speed WECS. In these applications, power converters are used to match the wind turbine characteristics to the grid connection requirements (frequency, voltage, control of active and reactive power, harmonics, and so on) [3-6].

1.1. Background and development of wind energy

Wind energy is the kinetic energy associated with the movement of atmospheric air. Its utilization can be dated back to 5000 BC when sail boats were propelled across the river Nile. Also, it is recorded that wind mills have converted kinetic energy into mechanical energy since 200 BC, when pumping water, grinding grain, and drive vehicles and ships in ancient China and the Middle East [7, 8].

At the beginning of the twentieth century, the first wind turbines for electricity generation were developed, but fossil fuel steam turbines used for electricity

generation spread and gained all the interest, because they can provide a more consistent power source than the wind turbine. In 1973, due to the oil crisis, wind energy started to gain popularity in electricity generation, and it provided a reliable power source by using the electrical grid as a back-up. By the end of the 1990s, wind energy emerged as an important sustainable energy resource [8, 9].

1.1.1 Wind energy environmental impact and development

Due to excessive burning of limited fossil fuels like oil, coal and natural gas, global warming has become a threat to every individual. Carbon dioxide (CO₂) gas emissions need to be reduced to preserve air quality. The Kyoto protocol implemented on February 16th, 2005 was adopted by most countries. As a result, utilization of renewable energy resources, such as solar, geothermal, and wind energy appear to be the most effective ways in achieving the targets set in Kyoto and subsequent protocols. Wind generation attracts more attention than other clean energy sources and is perceived to have the lowest environmental impact of all energy sources [7, 9-12]:

- It occupies less land area per kilowatt-hour of electricity generation than any other energy conversion system, apart from roof-top solar energy.
- It generates the energy used in its construction in 3 months of operation, yet its operational lifetime is 20-25 years.
- It has zero fuel cost, zero emissions and zero water use.
- There has been fast growth in wind turbines, power electronics, and control techniques.
- Modern wind turbines are almost silent and rotate so slowly that they are rarely a hazard to birds.

In 1980, wind turbines were rated at a few kW per unit; today there are multi-MW wind turbines. Figure 1.1 shows the evolution of wind turbine size and rated power between 1980 and 2018 (expected) [13, 14].

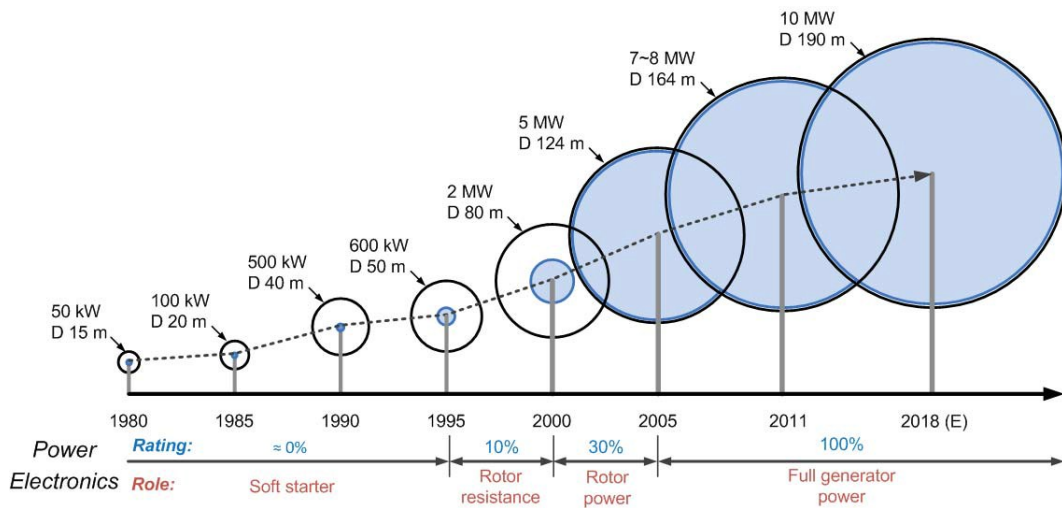


Figure 1.1 Evolution of wind turbine size and power electronics from 1980 to 2018 expected [13].

In 2008 the annual growth rates of cumulative wind power capacity have averaged 21.4%; the global wind power installed is over 318GW and in 2013 only 35GW wind power was installed, a 10GW decrease on that installed in 2012; due to a drop in the US market. Figure 1.2 shows the annual global growth of installed wind power. The largest wind energy market is Asia, which add 52% capacity per year, followed by Europe with about 32%. Figure 1.3 shows the top ten countries usage wind energy and the added capacity in 2013, where China is the market leader, followed by Germany and then the United Kingdom [7, 15]. From Figures 1.2 and Figure 1.3, wind power continues to grow and can be consider as a basic in a modern electrical energy systems. In Denmark, > 30% of the total electrical power consumption comes from wind power, and it is planned to achieve 100% non-fossil-based power generation system by 2050 [16].

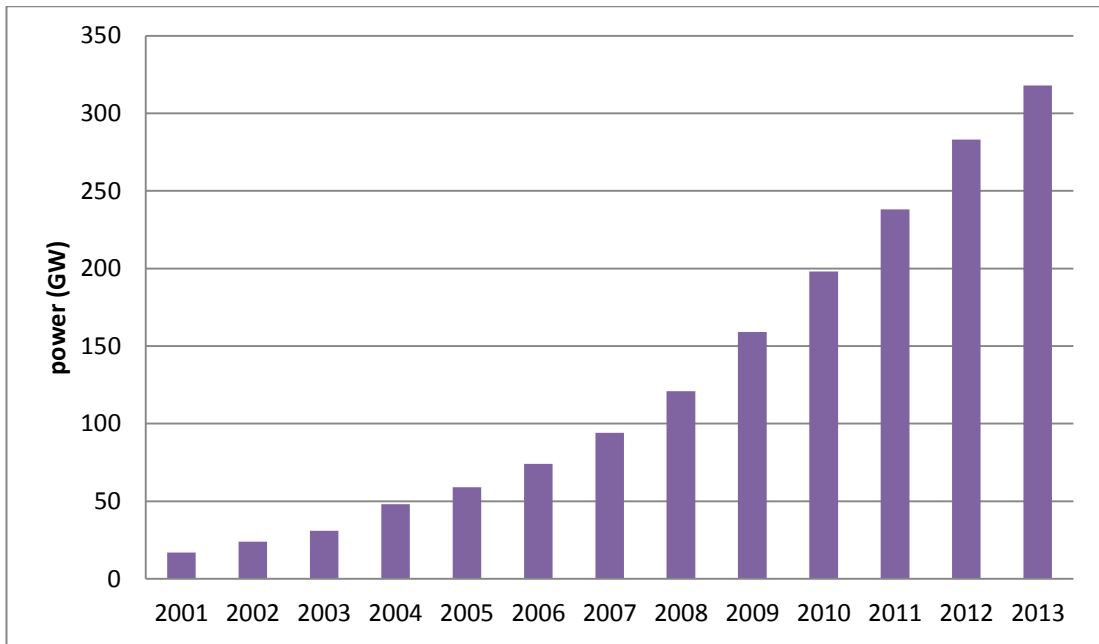


Figure 1.2 Total world wind power capacity from 2001 to 2013 [13].

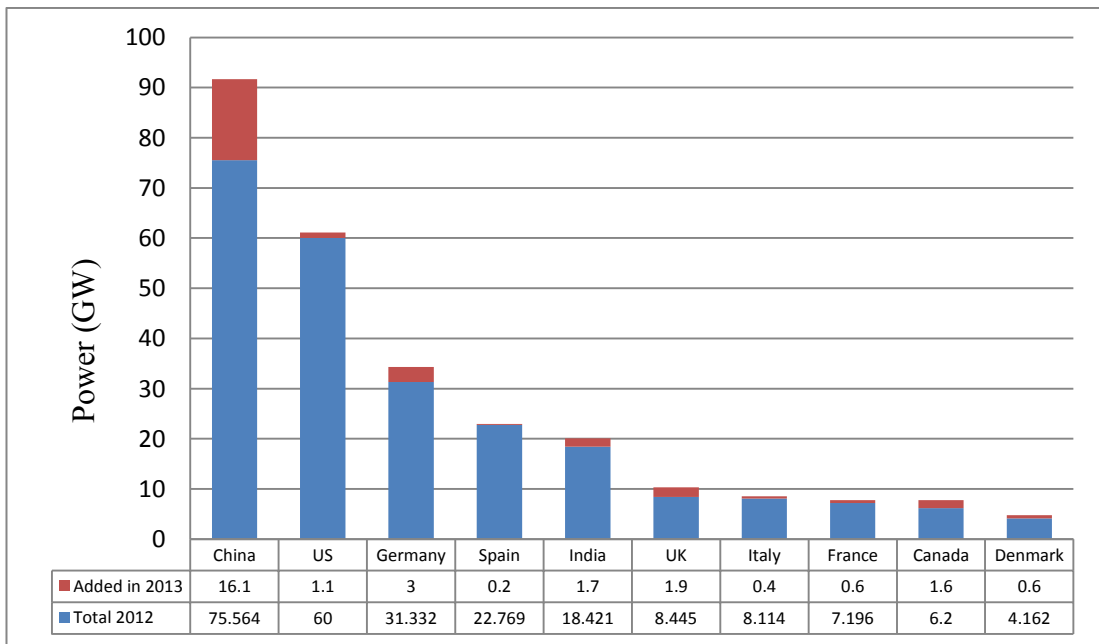


Figure 1.3 Total wind power capacity and added capacity 2013, of the top ten countries [7].

1.1.2 Wind Energy Conversion System main components

Wind turbines capture power from the wind by means of turbine blades which convert it to mechanical power. It is important to be able to control and limit the converted mechanical power during higher wind speeds (using stall control, active stall, and pitch control). A gear box is used to convert the low turbine speed to a high

speed for the generator to convert the mechanical power to electrical power. With a multi-pole large-diameter generator the gearbox may not be necessary. The generated electrical power passes through power electronic converters and a transformer with circuit breakers, before being fed into the grid [3].

1.1.3 Wind turbine classification according to the orientation axis

Wind turbines can be classified into two groups according to orientation; horizontal axis wind turbines (HAWTs) and vertical axis wind turbines (VAWTs) [17, 18]. VAWTs have the following advantages over HAWTs: 1-low starting wind speed. 2- Independence with respect to the wind direction (without yaw controller). 3- Lower noise [19, 20]. The main drawbacks of VAWTs are: 1- Not self-starting. 2- Difficulty to embed into the design a stall mechanism at high wind speed to prevent over speeding, which will cause excessive power and overvoltage if a permanent magnet synchronous generator (PMSG) is used. 3- The aerodynamic torque has a series of oscillatory components [19, 21]. These drawbacks limit the use of VAWTs in MW WECS. HAWTs are commonly used for MW WECS and are assumed in this research.

1.2. Wind turbine generator

The generator in a WECS can be categorized into four main types [14, 22]:

1. Fixed-speed squirrel-cage induction generator (SCIG).
2. Limited-variable-speed wound rotor induction generator (WRIG).
3. Variable-speed doubly fed induction generator (DFIG) with partial scale converter.
4. Variable-speed synchronous generator (SG).

1.2.1 Fixed-speed SCIG conversion concept

This is the conventional concept applied by many Danish wind turbine manufacturers during the 1980s and 1990s, with a multistage gear box placed between the turbine's hub and the generator shaft, while the generator stator is grid connected through a coupling transformer. The SCIG takes reactive power from the grid, and generates real power via slip control when driven above synchronous speed. This generation concept is robust, cheap, and easily controlled and can provide stable frequency

control due to fixed speed operation. The main drawbacks can be summarized in the following points [23, 24]:

- SCIG operates in a narrow range around synchronous speed, such as a speed higher than synchronous speed.
- Since the SCIG consumes grid reactive power, there is a large inrush current and voltage drop at the time of connection. To overcome this, a reactive power compensator is needed to reduce the SCIG reactive power demand.
- The fixed speed concept means that wind speed fluctuations are directly translated into electromechanical torque variations. These cause high mechanical and fatigue stresses on the system, and result in swing oscillations between the turbine and generator shaft.

1.2.2 Limited-variable-speed WRIG conversion concept

The limited variable speed concept uses a multiple-stage gearbox and WRIG. The WRIG stator is directly connected to the grid, where the rotor winding is connected in series with a controlled resistor bank. Variable speed operation is achieved by adjusting the energy extracted from the WRIG rotor. Since power is dissipated in the external resistor, this limits the speed range to less than 10% above synchronous speed, because increasing the variable speed range with higher slip means a high power extracted by the rotor, and a lower generator efficiency, which means a higher resistor rating. Such WECS require reactive power compensation and soft start, and due to using a multi-stage gearbox, the converter system cost increases and extra gearbox maintenance is required [23, 25].

1.2.3 Variable-speed DFIG conversion concept

The DFIG conversion concept consists of a variable speed wind turbine with a WRIG, where the WRIG stator is directly connected to the grid, and the rotor is connected to a partial-scale power electronic converter. The power converter controls the rotor frequency, thus the rotor speed. This concept extends the operating speed range to $\pm 30\%$ around the synchronous speed, with the power electronic converter rated at 25~30% of the generator capacity. Also the power electronics converter system can perform a reactive power compensation and smooth grid connection. However, its main drawbacks are the use of slip-rings and grid fault protection. It

requires a crow-bar in the rotor circuit during faults and uses a multi-stage gearbox [26-28].

1.2.4 Variable-speed synchronous generator

In the variable-speed concept, the generator is connected to the grid through a full-scale back-to-back (BTB) power electronics converter. The power electronics converter performs reactive power compensation and a smooth grid connection over the entire speed range. However, it has high power loss in the power electronics converter and is more expensive than DFIG that uses a partial-scale converter. The generator in a direct-drive WECS is connected directly to the turbine hub [29].

Types of SG for the variable-speed concept with a full-scale converter are:

1. Electrically excited synchronous generator (EESG): the EESG has two windings -a field winding on the rotor for dc excitation and a three-phase armature winding in the stator. The field winding is connected to an external dc source or to the ac grid through a ac/dc converter to provide the required field current. The stator winding delivers power to the grid through a full-scale BTB converter. The rotor converter controls the flux to minimised loss in different power ranges. But the EESG is heavy, expensive and contains more parts, due the rotor and stator winding, and a high number of poles. The slip rings and brushes in rotor winding must be maintained. To overcome the slip rings and brushes problem the brushless exciter is used. Where a small ac generator whose field circuits are mounted on the stator and armature circuits are mounted on the rotor shaft. This generator gives three-phase output and a three-phase rectifier (mounted on the shaft) is used to get dc field circuit, and it is possible to adjust the field current on the main machine by controlling the dc field current of the exciter generator [30, 31].
2. Permanent magnet synchronous generator (PMSG): the use of permanent magnets (PM) is attractive, because performance is improved and PM costs are decreasing. Using a PM instead of a wound rotor increases efficiency, reduces generator weight and increases reliability due to the absence of slip rings and brushes. However, PM machines have some disadvantages such as

high cost of the PM material, difficulties to handle in manufacture, and PM demagnetisation at high temperature [23, 32].

Drivetrain technology for variable-speed synchronous generator based WECS:

1. Direct drive (DD) drive-train (overall ratio 1:1): The advantages of direct-drive wind turbines are simplified drive train, higher overall efficiency, and higher power to weight ratio, and high reliability and availability by removing the gearbox. But generator size and cost is high.
2. Medium speed drive-train (overall ratio 10:1 to 40:1): The wind turbine is connected to a single-stage gearbox that increases the speed; the generator rated speed varies from 150 to 400 rpm. This tends to decrease the number of generator poles (reduced weight and cost)[23, 33].
3. High speed drive-train (overall ratio 100:1 or more): Replacing the DFIG with a variable-speed multiple-stage gearbox WECS, increases efficiency with a brushless generator and improves performance in case of grid fault ride. The disadvantages are: PMSG is larger and requires a more expensive full-scale converter [23].

1.3. Comparison of different wind generator systems

Table 1.1 compares five different generation systems for the same wind turbine [23], from which the following conclusions can be drawn.

- The generator in the direct-drive concept has the largest size and weight and the three-stage gearbox DFIG has the lowest size and weight, but the total weight of WECS will not be significantly different, when considering the weight of the other parts of the wind turbine blade and three-stage gearbox.
- The direct-drive PMSG concept has the highest energy yield; while the EESG direct drive is the heaviest and most expensive solution.
- The single-stage gearbox DFIG has the highest annual energy yield divided by cost and the lowest generator system cost.

Due to the attributes previously highlighted, this thesis subsequently considers only the variable speed single-stage geared concept due to its lower generator size and

weight compared to the direct-drive variable speed concept. It also overcomes the disadvantage of using a complex multistage gearbox. The single-stage PMSG has a full operating speed, unlike the DFIG, which operates at $\pm 30\%$ around synchronous speed. In addition, the full-rated power converter decouples the wind turbine and generator from the grid, giving better generator and wind turbine system performance during grid faults [22].

Table 1.1 Comparison of five different wind generator systems[23].

	DFIG three-stage gearbox	EESG direct-drive	PMSG direct-drive	PMSG single-stage gearbox	DFIG single-stage gearbox
Stator air-gap diameter (m)	0.84	5	5	3.6	3.6
Stack length(m)	0.75	1.2	1.2	0.4	0.6
Active material weight (tonne)					
Iron	4.03	32.5	18.1	4.37	8.65
Copper	1.21	12.6	4.3	1.33	2.72
PM			1.7	0.41	
Total weight	5.25	45.1	24.1	6.11	11.37
Cost (kEuro)					
Generator active materials	30	287	162	43	67
Generator construction	30	160	150	50	60
Gearbox	220	---	---	120	120
Converter	40	120	120	120	40
Other wind turbine parts	1300	1300	1300	1300	1300
Margin for company cost	250	250	250	250	250
Total cost	1870	2117	1982	1883	1837
Annual energy yield (MW h)	7690	7740	7890	7700	7760
Annual energy yield/total cost, (kWh/Euro)	4.11	3.67	3.98	4.09	4.22

1.4. Reliability and condition monitoring of WECS

To make wind power competitive with other energy sources, availability, reliability and turbine life need to be improved. Since some WECS components fail earlier than expected, condition monitoring systems are employed to ensure reliability and to recover from breakdowns. In condition monitoring systems, sensors (such as for vibration, acoustics, oil quality, strain and thermography) and signal processing are used to monitor the status of critical components such as the blades, gearbox, generator, main bearings and the tower. With data acquisition, early warnings of mechanical and electrical faults can be detected, while components are still operating, and appropriate maintenance action can be taken to avoid catastrophic failures. Thus, increasing reliability, availability, and maintenance and operational

cost reduction, are required [34, 35]. The condition monitoring system is important for both of onshore and offshore wind turbines, where bad weather conditions (storms, high tides, etc.) can prevent repair action for several weeks in an offshore situation [36]. Swedish wind power plant studies between 2000 and 2004, show that the electrical components have the highest failure percentage (17.5 %), followed by sensors (14.1%) and blades/pitch components (13.4%). In variable speed WECS the power electronics converter can reduce the mechanical stress in the drive train and this improve reliability in this part of the wind turbine [37]. But the power electronics converter has the highest failure rate in the variable-speed WECS electrical component, this due to failure in power electronics switches, cable and contacts losses caused by vibration, and capacitors failure. Failure in the power electronics converter can cause a fire in the wind turbines. This makes it more important to monitor the electrical components [38].

1.5. WECS grid code requirements

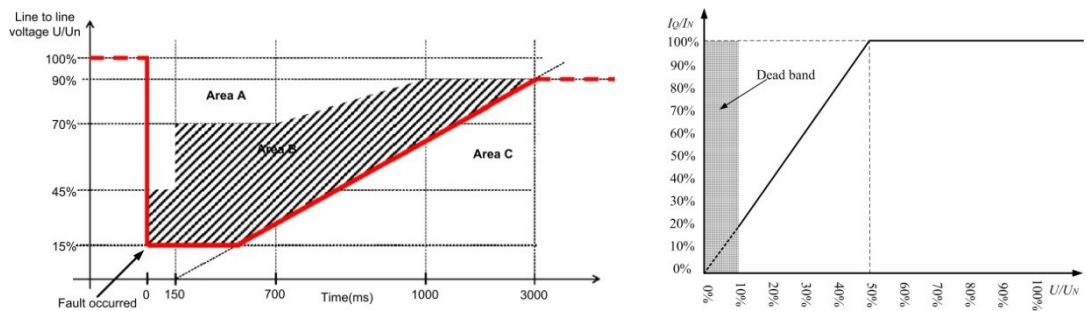
As wind power connected to the power system continues to increase, transmission system operators have become concerned about the impact of high levels of wind power generation on power systems, and have issued grid codes. The technical grid code requirements for wind turbine connection and operation can be broadly summarized into five areas [39]:

- 1) Fault ride-through requirements.
- 2) Active and reactive power responses following disturbances.
- 3) Extended variation range for the voltage–frequency.
- 4) Active power control or frequency regulation support.
- 5) Reactive power control or voltage regulation capability.

1.5.1 Fault ride-through requirements

During grid faults, a WECS is exposed to a voltage sag condition at its terminals depending on the fault type and location. Grid codes require a WECS to remain connected to the grid and supply reactive power for a given voltage dips profile. Such requirements are usually referred to as low voltage ride through (LVRT).

Among the LVRT standards, the most representative is by the German company E.ON, as shown in Figure 1.4 [40, 41]. From Figure 1.4(a), the voltage limit curve consists of three regions. Area A represents normal operation. Area B represents when the WECS should supply reactive power to the grid in order to support grid restoration, until protection devices detect the faulty area and isolate it from the rest of the network, or the grid fault continues until it reaches Area C. In Area C, the WECS can disconnect. The reactive current compensation curve in the presence of voltage-dips is shown in Figure 1.4(b) where the WECS has to supply at least 1.0 p.u. reactive current when the voltage falls below 50%. A dead band of 10% is introduced to avoid undesirable control action.



(a) Voltage limit curves to allow WECS disconnection

(b) Reactive current compensation curve in the presence of voltage-dips

Figure 1.4 Grid code LVRT requirements [38].

1.5.2 Frequency control

Grid codes specify that all generating plant should be able to operate continuously between a frequency range around the nominal grid frequency, usually between 49.5 and 50.5 Hz in Europe, and operate for different time periods with lower/higher frequencies to a minimum/maximum limit; usually 47–47.5 and 52 Hz. Beyond these limits disconnection without any time delay is required. The frequency is measured in a wind farm point of common coupling. The wind farm will produce more or less active power in order to compensate for frequency behaviour, as shown in Figure 1.5, where when the grid frequency exceeds rated value, the WECS decrease their output at a given rate. During nominal frequency, the power output is below the maximum, so if the frequency starts to drop, the wind farm would increase the power output to the maximum achievable power, whilst trying to sustain the frequency [42-44].

The frequency control participation is varies with transmission system characteristics. According to the German code, when the frequency exceeds 50.2 Hz, wind farms must reduce their active power with a 0.4 pu/Hz gradient. The British code requires that wind farms larger than 50 MW have a frequency control device capable of supplying primary and secondary frequency control, as well as over-frequency control. It also prescribes tests, which validate that wind farms indeed have the capability of the demanded frequency response [44].

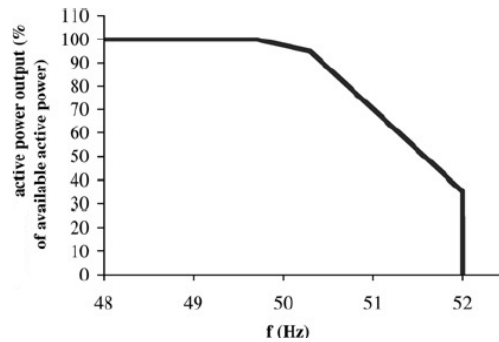


Figure 1.5 Power-frequency response curve [44].

1.5.3 Reactive power control and voltage regulation capability

The Grid Code requires that wind farms should have reactive power control capability, to regulate the voltage at the point of common coupling by producing or absorbing reactive power (capacitive/inductive power factor) to the grid in order to compensate for the voltage deviation on the grid at the point of common coupling, as shown in Figure 1.6 [44].

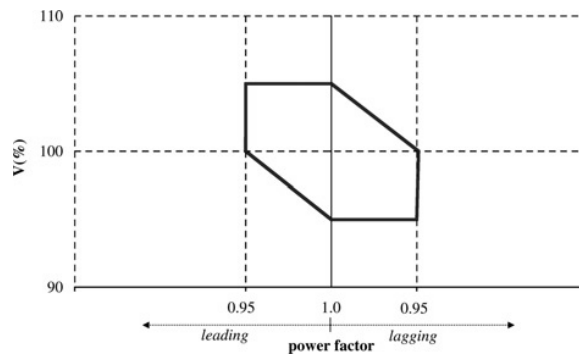


Figure 1.6 Typical requirements for power factor variation range in relation to voltage [44].

1.5.4 Active power constraints

Grid codes requires regulation capability of the active power of wind farms, where the system operator can provide short and long term frequency supports to the network [39, 43-45].

i. Absolute power control

In this type of power control the power output is regulated to a specific value or to bear a fixed relationship to the available power, even if more power can be extracted from the wind. Below this limit the wind farm can extract the maximum available power as shown in Figure 1.7(a). The absolute power controller is used when demand is low and wind power high.

ii. Delta production constraint

The wind farm is ordered to operate with a certain constant below the available power production capacity as shown in Figure 1.7(b). Thereby the wind farm can be used for the frequency control action previously described. This may also help reduce sudden changes in the output active power, which can potentially disturb network stability due to high variation in wind speed.

iii. Balance Regulation

The wind farm must be able to reduce/increase its active power delivered to the grid as shown in Figure 1.7(d). This is helpful for balancing the production and consumption of active power in the grid.

iv. **Power gradient constraint**

Power gradient sets how fast the wind farm power production can increase or decrease power output. The power increase/decrease gradient is slower than that of wind turbines. Such a limiter helps maintain production balance between wind farms and conventional power plants.

1.6. Research motivation

During the last decade, wind turbine-generator power ratings have increased from several hundreds of kW to multi-MW, with variable-speed wind energy conversion systems increasingly utilized to maximize the kilowatt-hour production of wind farms. Much research has been focused on power converter applications in variable-speed WECS. The primary tasks of these converters are [46]:

- Allow maximum power extraction from the wind turbine over a wide wind speed range
- Provide constant grid voltage and frequency, and inject a sinusoidal current into the grid with low harmonic content
- Supply grid reactive power on demand
- Meet wind energy grid codes and standards

Thus, the issue of reliable and efficient of power electronic converters is the main concern for manufacturers, researchers, and users, when operating WECS.

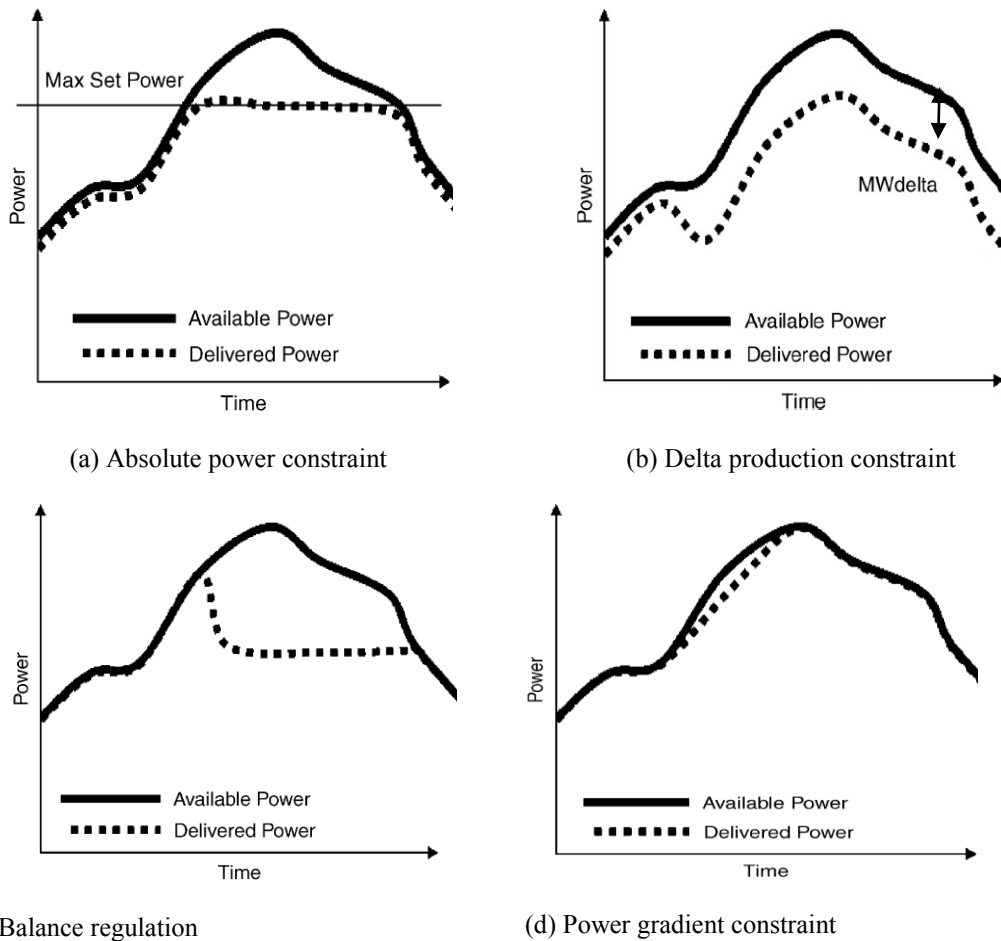


Figure 1.7 Typical active power control [39].

1.7. Objectives

This thesis focuses on current source based power electronics converter topologies, which have interesting properties and are suitable for variable-speed WECS applications. In line with this, the thesis objectives can be summarized as follows:

- Understanding current source converter (CSC) properties that are suited for WECS. To develop such understanding, CSC modulation strategies and performance of the current source inverter (CSI) and current source rectifier (CSR) are studied, including dual three-phase CSR and CSI, for medium power applications.
- For reduced power circuit and control complexity and cost, new ac-dc buck-boost converters are proposed for wind generator interfacing rather than traditional six-pulse or neutral-point clamped converters.

- Integrating the proposed ac-dc buck-boost converters with conventional CSI, to form a modified CSC based back-to-back (BTB) converter. This current type BTB converter offers the attributes of the existing voltage source converter BTB systems, but with improved system reliability.
- Three different variable-speed current source based WECS configurations are proposed:
 - 1) The first proposal utilizes a dual three-phase PMSG with a BTB dual current CSR and CSI. This configuration fulfils the requirements for multi-MW turbine-generators such as low switching frequency and high quality ac side waveforms.
 - 2) The second and third WECSs employ variant versions of the modified BTB CSC, with the second configuration suitable for fractional MW application and the third suitable for multi-MW application.

The three proposed WECSs are analysed, simulated and assessed on scaled down prototypes for proof of concept. Simulation and experimental results substantiate the proposed WECS as competitive to voltage source converter systems, which are widely used and accepted by the industry.

1.8. Structure of the thesis

The thesis consists of eight chapters.

- Chapter 1: Introduces this thesis, and includes a background, development of wind energy, classification of wind turbine generators, and wind energy grid code requirements.
- Chapter 2: Discusses modulation strategies for the two level voltage source converters (VSC) and CSC. Also the VSC and CSC are compared.
- Chapter 3: Analysis and simulation of the CSI and CSR, including CSI islanding operation. Also, different CSI and CSR control strategies are discussed; including independent control of active and reactive powers, low ac current total harmonic distortion (THD), reliable CSR dc load voltage, and fast adjustable CSI ac load voltage in islanded mode. The dual-bridge CSR and CSI are also discussed, including their controller architectures.

- Chapter 4: Presents a comprehensive discussion of several versions of the proposed ac-dc buck-boost converters and highlights their main features such as buck-boost capability in a single stage with a single switch; reduced power circuit and control complexity, stable dc voltage output in both buck and boost modes; and sinusoidal input current with near unity power factor. Single-phase, three-phase and multi-phase buck-boost converters variations are presented, including their control.
- Chapter 5: The modified CSC based BTB converter is proposed (three-phase and dual three-phase). Its main features are reduced power circuit and control complexity, and sinusoidal ac currents with high power factor achieved at both ac sides at reduced switching frequency. The basic relationships that govern steady-state converter operation are established, and filter design is included. PSCAD/EMTDC simulations and experimentation demonstrate the practicality of the proposed power conversion system, and results show that the converter has good dynamic performance, with near unity input power factor over an extended operating range.
- Chapter 6: Discusses modelling of the three-phase synchronous machine and the dual three-phase PMSG in the dq0 reference frame. These models are subsequently used to simulate the proposed wind energy conversion system in PSCAD/EMTDC modelling tools.
- Chapter 7: Three proposed variable speed WECS based on the converters discussed in previous chapters are described, simulated and experimentally evaluated.
- Chapter 8: Presents general conclusions and recommendations for future research.

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Chapter 2 Power Electronic Converters

This chapter discusses the switching techniques used to generate the gating signals for the two-level voltage source converters (VSC), and current source converters (CSC). The well-known modulation techniques for the two-level VSC are: sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), and selective harmonics elimination (SHE). A mapping technique to make SPWM signals suitable for the CSC is presented, as are SVM and the proposed SHE. A comparison between the VSC and CSC is presented at the end of the chapter, to support the direction of the proposed research on using CSC in wind energy conversion system application.

2.1 Power electronic converters

The voltage source converter (VSC) and current source converter (CSC) are two topologies used in many power conversion systems, such as: motor drives, fixed/variable frequency power supplies, uninterruptible power supplies, distributed generation and renewable energy [1].

The dc to ac converter is termed an inverter, and can be classified into a voltage source inverter (VSI) or a current source inverter (CSI). Figure 2.1(a) shows a two-level VSI, which consists of six unidirectional switches (S_1 to S_6) with anti-parallel diodes (D_1 to D_6), where the ac-side inductance filter is used to smooth the current ripple and to absorb the rapid voltage change (dv/dt). The VSI has a dc voltage supply and a capacitor at the inverter dc input. The VSI is a voltage step-down converter, which means that the peak line-to-line output voltage is less than the dc link voltage. Figure 2.1(b) shows a six-pulse CSI which is also a boost inverter [2]. It consists of six unidirectional switches with series connected diodes, to provide the reverse blocking capability of the inverter. Insulated Gate Bipolar Transistor (IGBT) packages dedicated for the VSI have built in anti-parallel diodes. The CSI requires a dc current source, which can be derived from a dc voltage source connected in series with a large dc-link inductor. The ac-side capacitance filter is used to smooth the output voltage ripple and to absorb the rapid current change (di/dt) [2-5].

Traditionally, a device that converts ac voltage to dc voltage is called a rectifier. Rectifiers can be referred to as: a voltage source rectifier (VSR) or a current source rectifier (CSR). A VSR is shown in Figure 2.1(c) where a three-phase ac-side inductive filter is used to suppress the line current ripple and bulky dc-side capacitance smooth the output voltage. The VSR is a boost type converter such that the output dc voltage is higher than the peak line-to-line supply voltage [6, 7]. The CSR is a buck type rectifier since the output voltage is less than the supply peak line-to-line voltage. The CSR requires an input LC filters and output inductance as shown in Figure 2.1(d) [8].

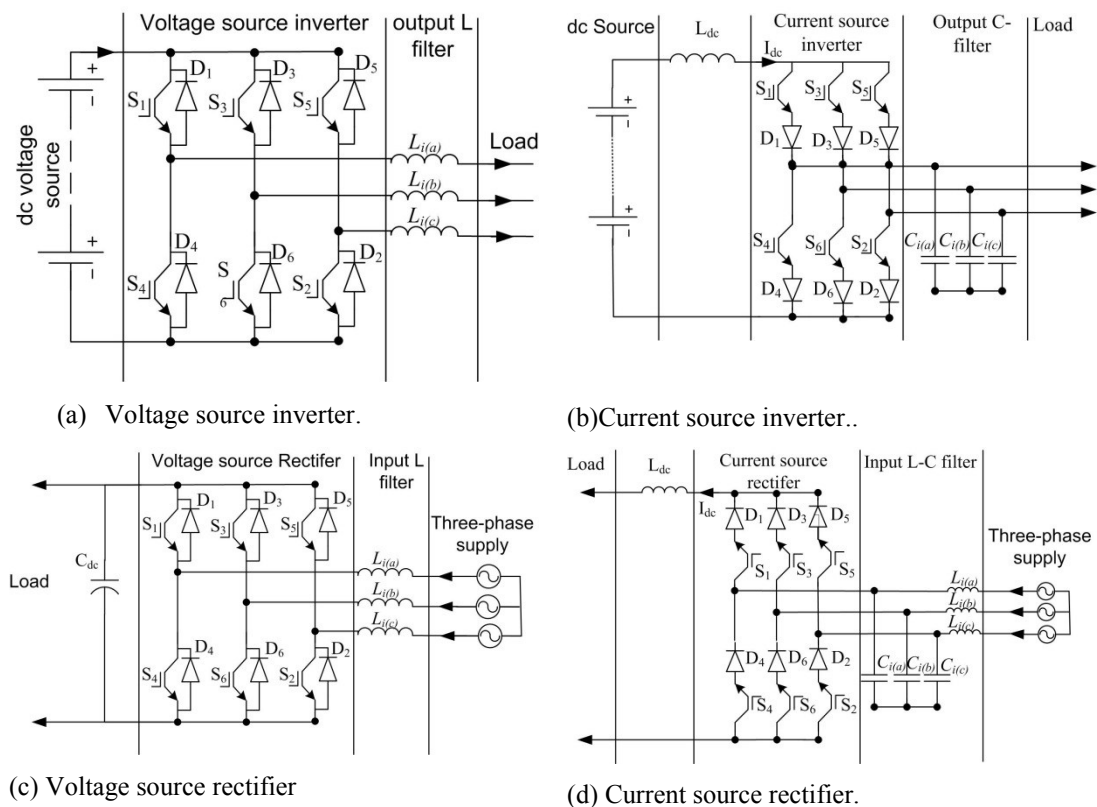


Figure 2.1 Conventional voltage source and current source converters

2.2 Voltage source converters

This section focuses on pulse width modulation (PWM) schemes for the VSI. A carrier-based sinusoidal PWM (SPWM) scheme is reviewed, followed by space vector modulation (SVM) algorithms.

2.2.1 Sinusoidal PWM Switching

The SPWM scheme compares a high frequency triangular carrier wave (v_{cr}) against three-phase sinusoidal modulating waveforms references (v_{ma} , v_{mb} , and v_{mc}) as illustrated in Figure 2.2. The three-phase sinusoidal references represents the frequency and magnitude desired for the inverter output [9].

$$m = \frac{v_m}{v_{cr}} \quad (2.1)$$

Where v_m and v_{cr} are the peak values of the modulating signal and carrier waves (v_{cr} is equivalent to half the dc source), respectively. The amplitude modulation index m is usually adjusted by varying v_m while keeping v_{cr} fixed, to control the rms value of the inverter output line-to-line voltage [10, 11].

The operation of switches (S_1 to S_6) is determined by comparing the modulating waves with the carrier wave. For phase ‘a’ (S_1 and S_4), when $v_{ma} > v_{cr}$, the upper switch S_1 in the inverter is turned on ($g_1=1$). The lower switch S_4 operates in a complementary manner and thus is switched off ($g_4=0$), and vice versa when $v_{ma} < v_{cr}$. To avoid dc link short circuit during switching transitions of the upper and lower devices in an inverter leg, a dead time period is implemented, during which both switches are off [9]. Then (g_1 to g_4) represents the gate signals of the voltage source converter leg.

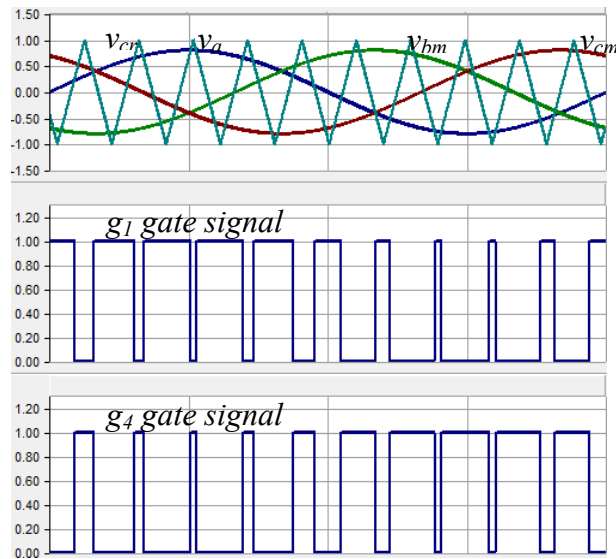


Figure 2.2 Sinusoidal pulse-width modulation (SPWM).

2.2.2 Space vector modulation algorithms

SVM is a common PWM technique applied to the inverter because of its superior harmonics and extended linear operating range. It has two features better than normal SPWM [12]:

- SVM provides a 15.5% higher fundamental amplitude than SPWM, which enables full utilisation of dc-link voltage (The modulating single of the third harmonics injection PWM (THIPWM) have also 15.5% higher fundamental amplitude [13, 14]).
- The number of switching operations is about 30% less, at the same carrier frequency.

SVM treats the inverter as a unified unit, which is mapped into eight states, The inverter states shown in Figure 2.1(a) can be represented by binary values, for example if S_1 is on ($S_1=1$) and if S_1 is off ($S_1=0$), the pairs S_1 & S_4 , S_3 & S_6 and S_5 & S_2 are complementary. This means the inverter has eight possible switch combinations, two giving a zero output (V_0 & V_7) and six non-zero vectors (V_1 to V_6), as shown on the hexagon in Figure 2.3. The angle between two adjacent non-zero vectors is 60 degrees. The two zero vectors at the centre of the hexagon, apply zero voltage to the load by conducting all the top or bottom switches (shorting the connected load) [15].

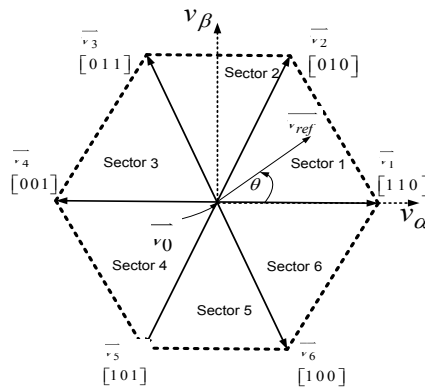


Figure 2.3 The basic switching vectors

Steps of implementing the space vector include:

1. Determine v_α , v_β , v_{ref} and angle θ

2. Determine the dwell times T_1 , T_2 and T_0
3. Determine the switching states of (S_1 to S_6)

Step 1-Determine V_α , V_β , V_{ref} and angle Θ

The instantaneous three-phase output voltage of the inverter (v_{abc}) can be transformed into a two-phase vector represented (v_α , v_β) by using an orthogonal linear transformation, called ($\alpha\beta 0$) transformation, given by [16, 17].

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \quad (2.2)$$

$$|v_{ref}| = \sqrt{v_\alpha^2 + v_\beta^2} \quad (2.3)$$

$$\theta = \tan^{-1} \left(\frac{v_\alpha}{v_\beta} \right) = \omega t \quad (2.4)$$

Step 2- Determine the time periods T_1 , T_2 and T_0

The switching time at any sector can be defined as [15, 18]:

$$T_1 = mT_s \sin\left(\frac{n}{3}\pi - \theta\right) \quad (2.5)$$

$$T_2 = mT_s \sin\left(\theta - \frac{n-1}{3}\pi\right) \quad (2.6)$$

Where T_s is the sampling time, Θ is the angle displacement between the reference vector v_{ref} , and the α axis of the space vector plane, and m is the modulation index ($m = \frac{\sqrt{3}|v_{ref}|}{v_{dc}}$).

After T_1 and T_2 are calculated, the residual sampling time is assigned to a zero vector with the condition $T_1 + T_2 < T_z$ and:

$$T_0 = T_z - T_1 - T_2 \quad (2.7)$$

Step 3-Determine the switching states of (S_1 to S_6)

The switching states can be summarized as shown in Figure 2. 4 [15, 18].

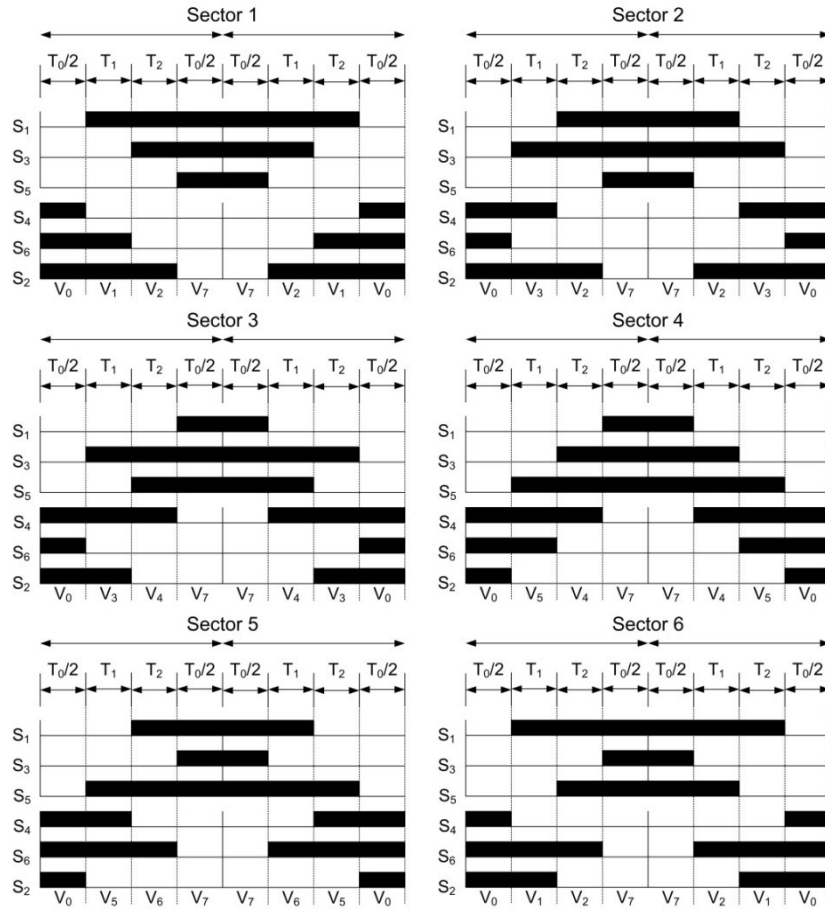


Figure 2. 4 SVM switching patterns for each sector.

2.2.3 Selective harmonic elimination (SHE)

SHE is an offline modulation scheme that eliminates a number of unwanted low-order harmonics in the inverter PWM output voltage. SHE based methods can theoretically provide the highest quality output among all the PWM methods. SHE offers several advantages compared to traditional modulation methods such as acceptable performance with low switching frequency to fundamental frequency ratios and direct control over output waveform harmonics. Figure 2.5 shows the inverter output voltage with nine pulses per half-cycle, with symmetrical switching angles around $\frac{\pi}{2}$. The normalized voltage v_0 can be expressed as a Fourier series by [19, 20]:

$$v_o = \sum_{n=1}^{\infty} B_n \sin(n\omega t) \quad (2.8)$$

$$B_n = \frac{4}{n\pi} \left[1 + 2 \sum_{i=1}^K (-1)^i \cos(n\theta_i) \right] \quad (2.9)$$

Where n is odd and takes the values 5, 7, 11, 13, 17, 19, and 23 (since the neutral point is isolated, triple harmonics do not exist), k is the harmonics can be controlled and the number of pulses per half cycle equals $(k+1)$.

In SHE the switching angles are determined by solving a set of nonlinear equations, (2.10) to eliminate the undesired low-order odd harmonics and (2.11) to control the magnitude of the fundamental output. Due to nonlinear and transcendental characteristics, such equations can only be solved numerically. To obtain fast convergence, the initial (starting) values must be chosen to be close enough to the final solutions. This is one of the most difficult tasks associated with programmed PWM techniques [21].

$$\frac{4}{n\pi} \left[1 + 2 \sum_{i=1}^K (-1)^i \cos(n\theta_i) \right] = 0 \quad (2.10)$$

$$\frac{4}{\pi} \left(\left[1 + 2 \sum_{i=1}^K (-1)^i \cos(n\theta_i) \right] - m \right) = 0 \quad (2.11)$$

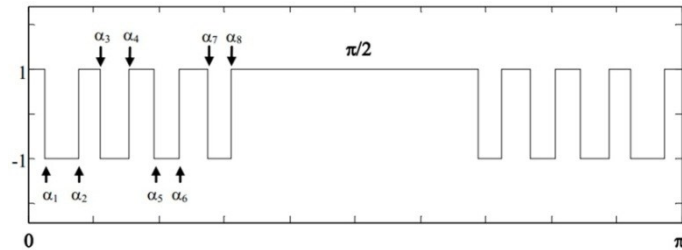


Figure 2.5 Normalized inverter output voltage.

2.3 The current source inverter

This section mainly deals with the PWM CSI. Three CSI modulation techniques are discussed: SPWM pulse mapping, space vector modulation (SVM), and selective harmonic elimination (SHE). The theoretical basis of the modulation schemes and performance will be analysed.

The CSI has the following characteristics over the conventional VSI [22, 23].

- Motor friendly waveforms because a CSI produces three-phase PWM currents instead of PWM voltages as from the VSI. With a filter capacitor installed at the inverter output, the load current and voltage waveforms are near sinusoidal. The high dv/dt output problem associated with the VSI does not exist in the CSI; because the output capacitor provides a path for the motor inductance current during changing the converter switching states.
- The CSI can boost the dc voltage to the grid voltage level.
- Reliable short-circuit protection. In case of a short circuit at the inverter output terminals, the rate of rise of the dc current is limited by the dc choke, allowing sufficient time for protection circuitry to function.

The main drawback lies in its limited dynamic performance due to the use of large dc choke inductance. An open circuit output is not allowed.

The CSI requires a three-phase capacitor C_i at its output to perform the following two functions:

- When switching states, it protects the inverter switching devices from high-voltage spikes, by providing a current path for the energy trapped in the load inductance.
- Harmonics filter and improve the load current and voltage.

The switching pattern for the CSI should generally satisfy two conditions: 1- The dc current I_{dc} should be continuous, and 2- at least one top/bottom switch must be closed at any time. This means that the oncoming switch should be turned on before the outgoing switch is turned off, and hence, overlapping periods are necessary to ensure that there is a path for the dc-link current during commutation [24]. These two switching conditions can summarize in the following two equations.

$$\begin{cases} g_{m1} + g_{m3} + g_{m5} = 1 \\ g_{m2} + g_{m4} + g_{m6} = 1 \end{cases} \quad (2.12)$$

$$\begin{cases} g_{m1} \cdot g_{m3} = g_{m3} \cdot g_{m5} = g_{m5} \cdot g_{m1} = 0 \\ g_{m2} \cdot g_{m4} = g_{m4} \cdot g_{m6} = g_{m6} \cdot g_{m2} = 0 \end{cases} \quad (2.13)$$

Where g_{m1} to g_{m6} represents the switch state of the current source converter.

2.3.1 SPWM plus mapping

The online carrier based SPWM described in section 2.2.1, which was initially developed for three-phase VSIs, can be extended to CSIs with a mapping logic [25-27], Then the advantages of the modulation scheme in VSIs are extended to the CSI.

i Mapping technique for implementation of the SPWM

This section proposes an online mapping technique for conventional SPWM gate signals (g_1 to g_6) to convert to CSC gate signals (g_{m1} to g_{m6}), as shown in Figure 2.6, Table 2.1 show CSC mapping table, which consists of six segments, each segment has a width $\frac{\pi}{3}$, as shown in Figure 2.7. This table is constructed according the following analysis on the first segment (0 to $\frac{\pi}{3}$), with the remaining five segments based on the same principle. v_{ref} has the highest absolute peak magnitude and is negative in the first segment. This translates to turn-on the corresponding lower switch of phase 'b', meaning gate $g_{m6}=1$, and from equation (2.12) the gate signals of the other two lower switches are kept off ($g_{m2}=g_{m4}=0$). Since the gate signals of the upper three switches must provide a continuous current path, g_{m1} will be high if g_1 and g_2 are high, similarly g_{m5} is high if g_5 and g_6 are high, g_{m3} will be high if g_{m1} and g_{m5} are low to secure a continuous path for the dc current I_{dc} .

Figure 2.8(a) and (b) shows the gate signals over one cycle (at $m=1$) for the upper and lower switches respectively. The gates of the upper the lower switches equals to one, meaning the proposed SPWM mapping technique secures a continuous path for the dc current and only one top/bottom switch must be closed at any time. Figure 2.9 shows an open loop simulation results of the proposed SPWM mapping technique with a 2000 Hz switching frequency, 400V dc supply voltage, 25mH dc-link inductance, 50 μ F ac-side C-filter Δ connected, and three-phase R-L load of 100 Ω and 5mH. Figure 2.9(a) and (b) shows the CSI three-phase output voltage and current.

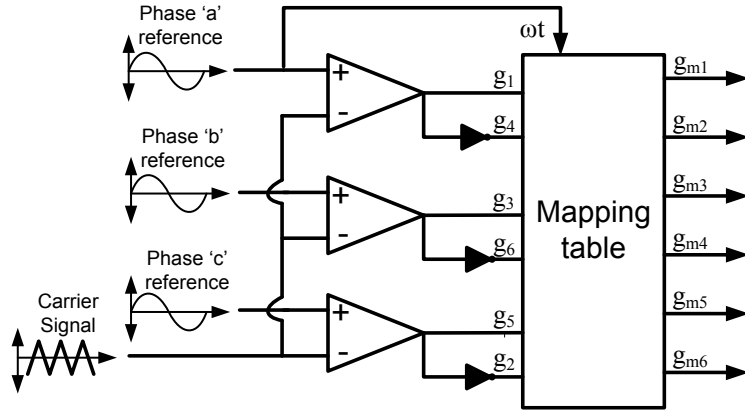


Figure 2.6 The proposed current source converter on-line mapping pattern generator.

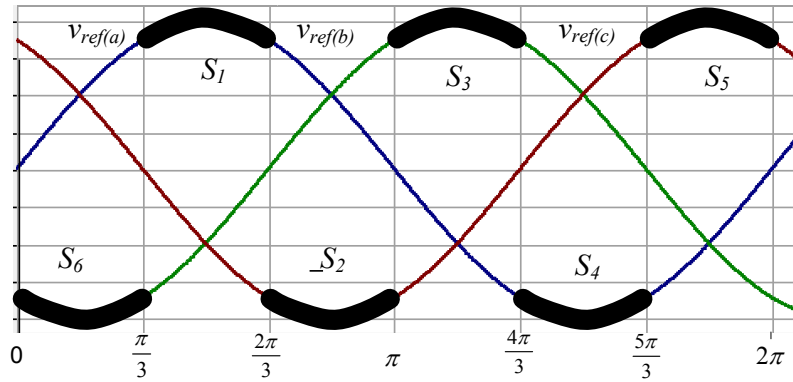


Figure 2.7 The six segments of the three-phase reference signal.

Table 2.1 CSC mapping table

ωt	Fixed switch state		Modulated switches
$0^\circ \approx 60^\circ$	$g_{m6}=1$	$g_{m2}=g_{m4}=0$	$g_{m1}=g_1 \text{ AND } g_2$ $g_{m3}=\text{NOT}((g_1 \text{ AND } g_2) \text{ OR } (g_5 \text{ AND } g_6))$ $g_{m5}=g_5 \text{ AND } g_6$
$60^\circ \approx 120^\circ$	$g_{m1}=1$	$g_{m3}=g_{m5}=0$	$g_{m2}=g_2 \text{ AND } g_3$ $g_{m4}=\text{NOT}((g_2 \text{ AND } g_3) \text{ OR } (g_6 \text{ AND } g_1))$ $g_{m6}=g_6 \text{ AND } g_1$
$120^\circ \approx 180^\circ$	$g_{m2}=1$	$g_{m4}=g_{m6}=0$	$g_{m1}=g_1 \text{ AND } g_2$ $g_{m3}=g_3 \text{ AND } g_4$ $g_{m5}=\text{NOT}((g_1 \text{ AND } g_2) \text{ OR } (g_3 \text{ AND } g_4))$
$180^\circ \approx 240^\circ$	$g_{m3}=1$	$g_{m1}=g_{m5}=0$	$g_{m2}=g_2 \text{ AND } g_3$ $g_{m4}=g_4 \text{ AND } g_5$ $g_{m6}=\text{NOT}((g_2 \text{ AND } g_3) \text{ OR } (g_4 \text{ AND } g_5))$
$240^\circ \approx 300^\circ$	$g_{m4}=1$	$g_{m2}=g_{m6}=0$	$g_{m1}=\text{NOT}((g_3 \text{ AND } g_4) \text{ OR } (g_5 \text{ AND } g_6))$ $g_{m3}=g_3 \text{ AND } g_2$ $g_{m5}=g_5 \text{ AND } g_6$
$300^\circ \approx 360^\circ$	$g_{m5}=1$	$g_{m1}=g_{m3}=0$	$g_{m2}=\text{NOT}((g_4 \text{ AND } g_5) \text{ OR } (g_1 \text{ AND } g_6))$ $g_{m4}=g_4 \text{ AND } g_5$ $g_{m6}=g_6 \text{ AND } g_1$

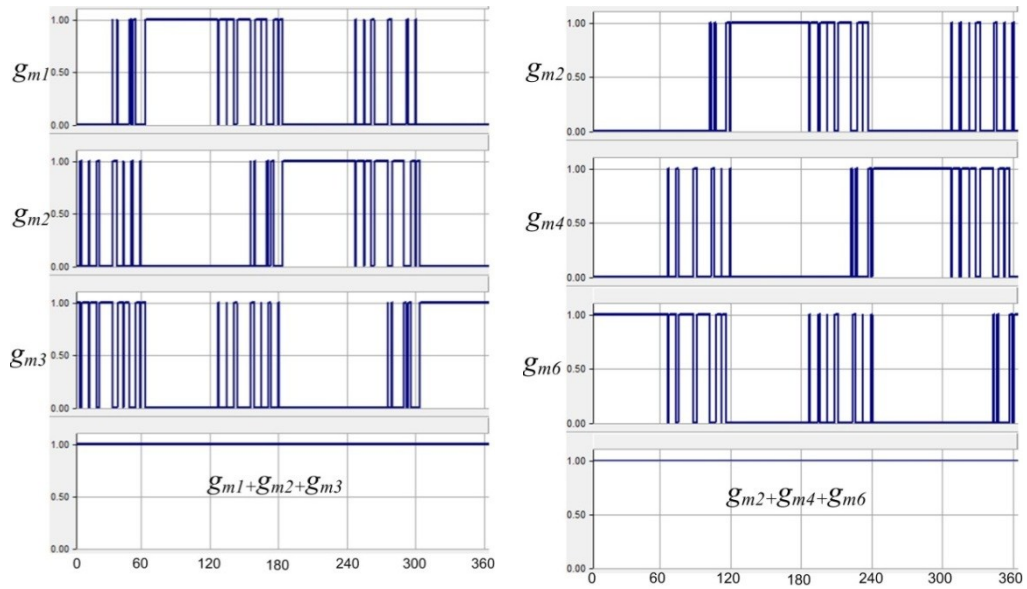
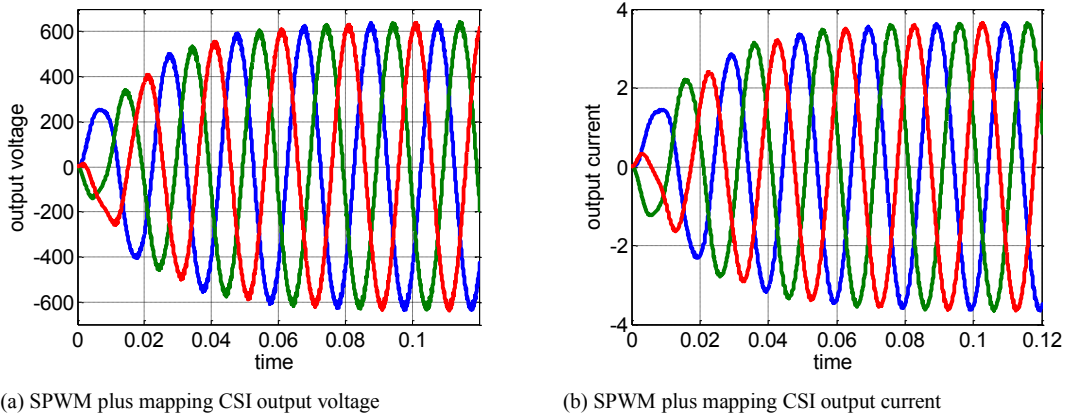


Figure 2.8 Mapped gate signals.



(a) SPWM plus mapping CSI output voltage

(b) SPWM plus mapping CSI output current

Figure 2.9 SPWM CSI open loop test.

2.3.2 Direct Space Vector PWM Switching

For the CSC, SVM is based on the possible switch combinations. From equations (2.12) and (2.13) there are six active states (dc-link inductance discharging states \bar{t}_1 to \bar{t}_6) but three zero states (dc-link inductance charging states \bar{t}_7 to \bar{t}_9), although in this case, the zero states are the activation of both switches within one leg. This is to ensure a continuous current through the dc-link inductor. These switching states can be represented by vectors in a CSI space vector diagram. Figure 2.10 shows a typical CSI space vector diagram. The vector dwelling times are calculated as follows [28, 29]:

$$T_1 = m_a T_s \sin\left(\frac{\pi}{6} - \theta + (n-1)\frac{\pi}{3}\right) \quad (2.14)$$

$$T_2 = m_a T_s \sin\left(\frac{\pi}{6} + \theta - (n-1)\frac{\pi}{3}\right) \quad (2.15)$$

$$T_z = T_s - T_1 - T_2 \quad (2.16)$$

Where $m_a = \frac{i_{ref}}{I_{dc}} = \frac{i_{i1}}{I_{dc}}$ is modulation index, i_{i1} is the peak value of the fundamental frequency component of CSI output current (i_{ia} , i_{ib} and i_{ic}), and n is the sector number.

To illustrate the switching sequence, the reference current vector \vec{i}_{ref} is estimated to be between vector \vec{i}_n and \vec{i}_{n+1} , a counter continuously counts from zero to T_s . At the beginning of each counter period T_1 and T_2 are calculated, the value of T_1 and $T_1 + T_2$ are compared with the counter value for proper vector selection. At the beginning of a sampling period the switching state of \vec{i}_n is selected, until ($T_s > T_1$) then the switching state of \vec{i}_{n+1} is selected. The corresponding zero vector \vec{i}_0 replaces \vec{i}_{n+1} if ($T_s > T_1 + T_2$), as shown in Figure 2.11 and isolated in Table 2.2 [28, 30, 31].

Figure 2.12 shows open loop simulation results of the proposed SVM CSI, with a 2kHz switching frequency, dc supply voltage=100V, dc-link inductance=25mH, ac-side C-filter=25μF Y connected, and a three-phase R-L load of 50Ω and 5mH. Figure 2.12(a) and (b) show that the SVM CSI successfully supplies the load with sinusoidal current and voltage.

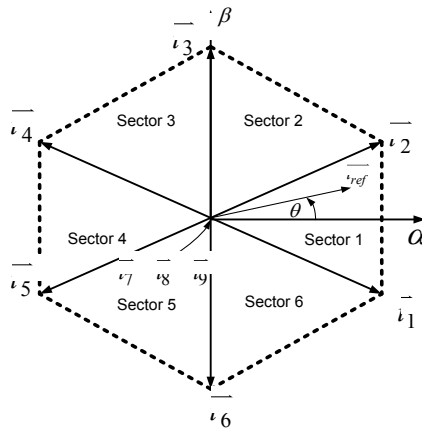


Figure 2.10 CSI space vector plane and switching states

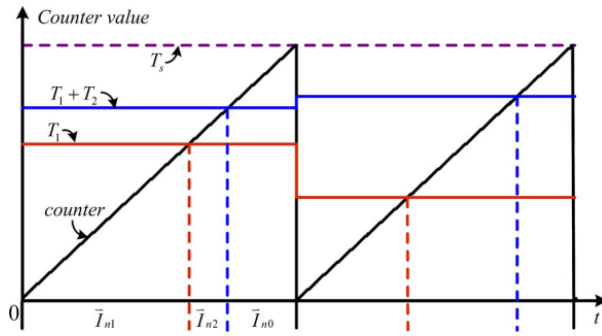
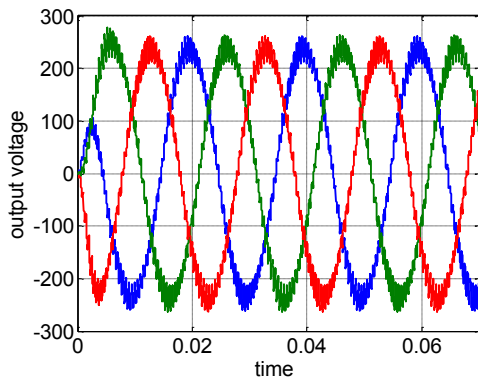


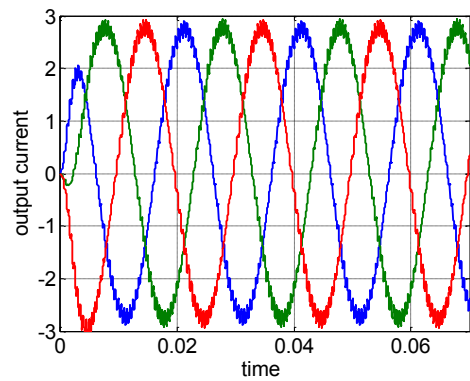
Figure 2.11 Vector selection method.

Table 2.2CSC SVM table

Sector	Vector		Corresponding zero vector	
	Vector	Gate	Vector	Gate
1	\vec{i}_1	$g_m=1$ $g_m=6$	\vec{i}_7	$g_m=1$ $g_m=4$
	\vec{i}_2	$g_m=1$ $g_m=2$		
2	\vec{i}_2	$g_m=1$ $g_m=2$	\vec{i}_9	$g_m=2$ $g_m=5$
	\vec{i}_3	$g_m=2$ $g_m=3$		
3	\vec{i}_3	$g_m=2$ $g_m=3$	\vec{i}_8	$g_m=3$ $g_m=6$
	\vec{i}_4	$g_m=3$ $g_m=4$		
4	\vec{i}_4	$g_m=3$ $g_m=4$	\vec{i}_7	$g_m=1$ $g_m=4$
	\vec{i}_5	$g_m=4$ $g_m=5$		
5	\vec{i}_5	$g_m=4$ $g_m=5$	\vec{i}_9	$g_m=2$ $g_m=5$
	\vec{i}_6	$g_m=5$ $g_m=6$		
6	\vec{i}_6	$g_m=5$ $g_m=6$	\vec{i}_8	$g_m=3$ $g_m=6$
	\vec{i}_1	$g_m=1$ $g_m=6$		



(a) SVM CSI output voltage.



(a) SVM CSI output current.

Figure 2.12 SVM CSI open loop test.

2.3.3 SHE switching scheme

Online modulation techniques such as SPWM and SVM were initially developed for the VSC and then extended to CSC. The resulting ac normalized current waveform in the CSC and the ac normalized voltage waveform in the VSC, are identical. In high power applications it is required to eliminate low-order harmonics with low-switching-frequency PWM patterns. Selective harmonic elimination (SHE) techniques provide low-order harmonic elimination with a low switching frequency [32].

The CSI SHE approach uses the chopping angles or gating patterns developed for the VSC in combination with logic circuitry to generate the gating patterns for CSC, as in [32]. [33, 34] propose SHE for the CSC, using a combination of commutations and short circuit pulses positioned to eliminate the selected lower order harmonics, with a low switching frequency with fixed fundamental ac current. In [35] a generalized CSC method is introduced to determine the number and position of the short circuit pulses for eliminating any number of harmonics as well as current magnitude control. The lowest possible frequency to achieve 5th and 7th harmonic elimination and an adjustable fundamental output current is proposed in [36].

i Lowest possible frequency to eliminate the 5th and 7th

The SHE technique proposed in [36] is discussed in this section. It uses six pulses per cycle - five to eliminate the 5th and 7th. The six pulses come from the angles θ_1, θ_2 and θ_3 as shown in Figure 2.13.

The phase current shown in Figure 2.14(b) can generally expressed as

$$i_a(\omega t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t) \quad (2.17)$$

Where n is the order of harmonics and a_n can be expressed as follows:

$$a_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} i_w(\omega t) \sin(n\omega t) d(\omega t) \quad (2.18)$$

$$a_n = \frac{4i_{dc}}{n\pi} \left[\cos(\theta_1 n) - \cos(\theta_2 n) + \cos\left(n\left(\frac{\pi}{6} + \theta_3\right)\right) - \cos\left(n\left(\frac{\pi}{3} - \theta_2\right)\right) + \cos\left(n\left(\frac{\pi}{3} + \theta_1\right)\right) - \cos\left(n\left(\frac{\pi}{2} - \theta_3\right)\right) \right] \quad (2.19)$$

To eliminate the 5th and 7th harmonic orders, a_5 and a_7 can be obtained from equation (2.19) and set to zero. The modulation index equation can be calculated as:

$$a_1 - mI_{dc} = 0 \quad (2.20)$$

The three nonlinear equations can be solved to get the variables θ_1 , θ_2 and θ_3 . The SHE tables to eliminate the 5th and 7th.

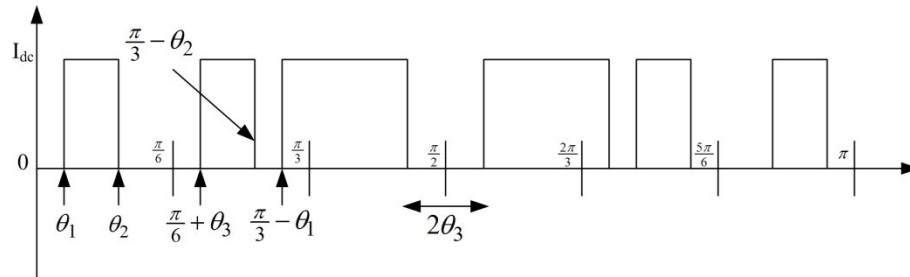


Figure 2.13 Converter half-cycle current with three independent angles.

ii Proposed SHE modulation, eliminating the 11th and 13th order harmonics

This section proposes a new SHE modulation technique which eliminates the lower order harmonics along with current magnitude modulation with a minimum switching frequency, without using short circuit pulses as in [33-35] or using a central angle pulse as proposed in [36]. The proposed SHE technique can eliminate the 11th and 13th harmonics order using one pattern with smooth pulse angle changes and with a fixed switching frequency, unlike the that proposed in [37] which uses two patterns with two switching frequencies.

Referring to Figure 2.1(b) switch S_1 gate signal is shown Figure 2.14, where three independent switching angles used to eliminate two harmonic orders. from Figure 2.14 seven current pulses per half-cycle of the fundamental frequency with only three independent switching angles θ_1 , θ_2 and θ_3 , The three switching angles provide two degrees of freedom, which can be used either to eliminate two harmonics in the

output current with modulation index control. The per filter inverter phase output current is shown Figure 2.15. Equation (2.18) can be rewritten as follows:

$$a_n = \frac{4i_{dc}}{\pi} \left[\int_{\theta_1}^{\theta_2} \sin(n\omega t) d(\omega t) + \int_{\theta_3}^{\frac{\pi}{6}} \sin(n\omega t) d(\omega t) + \int_{\frac{\pi}{3}-\theta_3}^{\frac{\pi}{3}-\theta_2} \sin(n\omega t) d(\omega t) + \int_{\frac{\pi}{3}-\theta_1}^{\frac{\pi}{2}} \sin(n\omega t) d(\omega t) \right] \quad (2.21)$$

$$a_n = \frac{4i_{dc}}{n\pi} \left[\begin{aligned} &(\cos(a_1 n) - \cos(a_2 n)) / n + (\cos(n(\pi/3 - a_1)) - \cos((n\pi)/2)) / n \\ &- (\cos(n(\pi/3 - a_2)) - \cos(-n(a_3 - \pi/3))) / n - (\cos((\pi n)/6) - \cos(a_3 n)) / n \end{aligned} \right] \quad (2.22)$$

To eliminate the 11th and 13th harmonics a_{11} and a_{13} are set to zero.

$$f_{11} = \left[\begin{aligned} &\cos(11\theta_1) - \cos(11\theta_2) + \cos(11\theta_3) + \cos((11\pi)/3 - 11\theta_1) - \\ &\cos((11\pi)/3 - 11\theta_2) + \cos((11\pi)/3 - 11\theta_3) - \sqrt{3} \end{aligned} \right] = 0 \quad (2.23)$$

$$f_{13} = \left[\begin{aligned} &\cos(13\theta_1) - \cos(13\theta_2) + \cos(13\theta_3) + \cos((13\pi)/3 - 13\theta_1) - \\ &\cos((13\pi)/3 - 13\theta_2) + \cos((13\pi)/3 - 13\theta_3) - \sqrt{3} \end{aligned} \right] = 0 \quad (2.24)$$

Equation (2.25) can derive for modulation index adjustment.

$$f = \frac{a_1}{i_{dc}} - m \quad (2.25)$$

$$f = \frac{4}{\pi} \left[\begin{aligned} &\cos(\pi/3 - \theta_1) - \cos(\pi/3 - \theta_2) \\ &+ \cos(\pi/3 - \theta_3) + \cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) - \sqrt{3} \end{aligned} \right] = m \quad (2.26)$$

Solving these three nonlinear equations (2.23), (2.24) and (2.26), varying m gives, Table 2.3. Figure 2.16 shows the FFT of the phase current at $m=1$, where the 11th and 13th harmonics are eliminated.

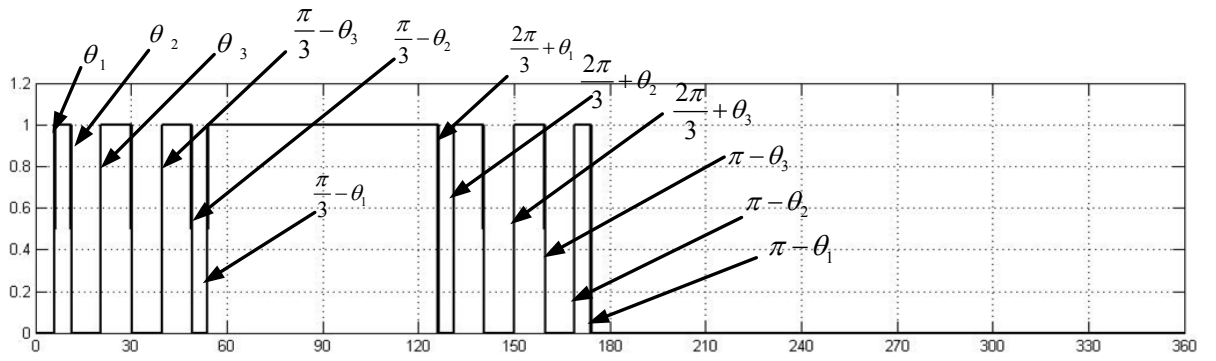


Figure 2.14 Switch S_1 gate signal waveform with three independent switching angles.

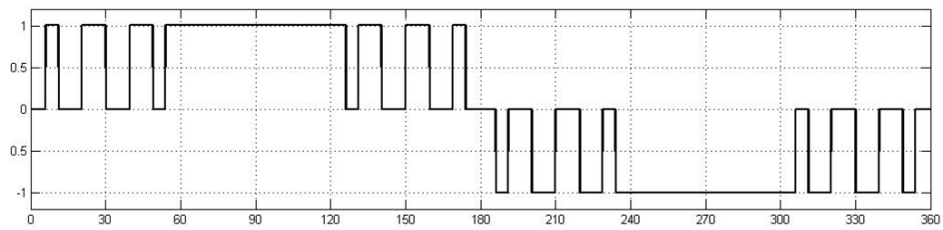


Figure 2.15 The phase current to eliminate two harmonics order.

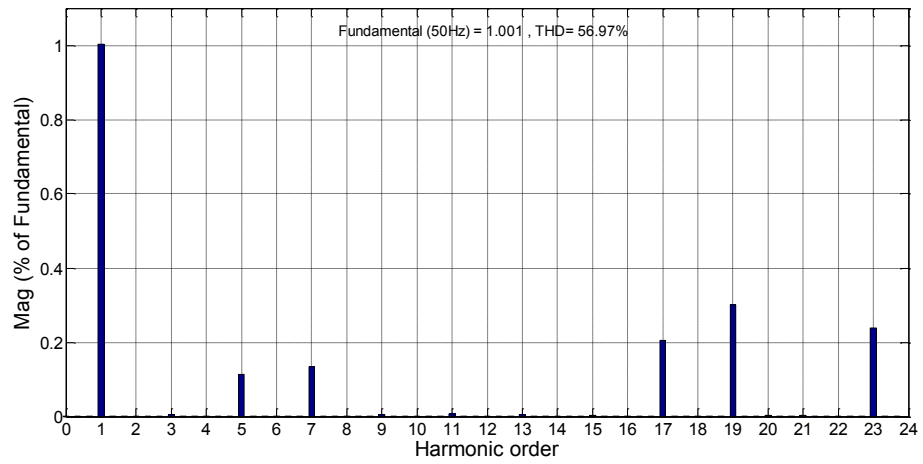


Figure 2.16 FFT for the phase current at $m=1$.

Table 2.3 SHE lookup table to eliminate the 11th and 13th harmonics order

θ_1	θ_2	θ_3	m
-29.2465	-15.2417	-14.3203	0.05
-28.4835	-15.4777	-13.6319	0.1
-26.9101	-15.9093	-12.2232	0.2
-25.2290	-16.2303	-10.7558	0.3
-23.3429	-16.3186	-9.1946	0.4
-21.0235	-15.8856	-7.4563	0.5
-17.6665	-14.1388	-5.2858	0.6
-12.5087	-9.9129	-2.0849	0.7
-4.8406	-2.5644	2.2273	0.8
0.8416	8.4149	10.3951	0.85
2.6328	11.5051	15.5528	0.9
6.0159	11.1006	20.3603	1
6.4239	11.0329	20.8085	1.01
6.8731	10.9879	21.2729	1.02
7.3502	10.983	21.7293	1.03
7.9079	11.0433	22.2101	1.04
8.5853	11.2206	22.7141	1.05
9.4902	11.6298	23.2577	1.06
10.9244	12.5955	23.8902	1.07
14.2056	15.6109	24.9459	1.08
14.8328	16.2700k	25.1626	1.081
15.5807	17.0904	25.4565	1.082
16.4875	18.1457	25.8995	1.083
17.6026	19.5722	26.6994	1.084
18.7929	21.3722	28.583	1.085

2.4 Comparison between the VSC and CSC

A comparison between voltage and current source converter technologies for high-power drives applications (greater than one MW) is presented in [24] and is summarized in Table 2.4. Ref [38] shows an efficiency comparison between three different medium voltage drive topologies: 1) a CSC based drive, 2) CSI with an 18-pulse thyristors rectifier; and 3) a three-level VSI with a 12-pulse/24-pulse diode rectifier. The third topology gives the highest efficiency, 98.77%, while the CSC based drives have the lowest, 97.65%. The efficiency difference is due to an active front end rectifier (CSR), which has higher losses than the diode rectifier, but this front end rectifier allows regenerative dynamic braking, lower THD supply current, and higher power factor.

Another comparison between a VSI with a boost converter (BC) and CSI for photovoltaic (PV) and fuel cell applications is presented in [39]. The analysis shows that the CSI has higher installed semiconductor rated current to boost the low fuel cell voltage with high current, while to the VSI plus BC needs only one power semiconductor which carries the current during boost operation. This yields

advantages for the VSI in terms of losses for both systems. Also [2] evaluates four single-stage power electronic converters for PV applications: 1) VSI, 2) CSI, 3) Z-source inverter (ZSI), and 4) CSI with series connected AC capacitors (CSI+SC). The VSI has the lowest losses, 2.2%, but requires a high PV voltage level. The CSI can operate over the full PV range but its conduction losses are higher than the VSI, 3.12%. The ZSI has the ability to buck and boost output voltage which better match PV characteristics, but it has the highest losses, 3.98%, in addition the high number of passive components increases the overall cost. For the CSI+SC, the dc-link inductance is smaller than that required for the CSI. This decreases the total losses to 3.02%. But this configuration has the drawback of low power factor due to its large series capacitance. The authors in [2] summarise stating that if all four topologies are required to operate over the whole PV V-I range, the VSI requires a boost converter, which increases total losses.

Reference [40] compares a grid connected VSI and CSI, based on switching frequency and at a low switching frequency, <10kHz, the total VSI power losses are lower than the CSI, while at a high switching frequency, the CSI has lower total power losses.

Although the CSI energy storage element is much heavier than in a VSC, it has a longer lifetime and the recent advancements in superconductor technology have led to the development of superconducting magnetic energy storage (SMES) systems, which considerably reduce the losses in the CSC energy storage element. With the development of 900V reverse-blocking IGBTs, the need for series diodes is eliminated, resulting in a reduction in the cost and conduction losses [41].

This thesis mainly concentrates on multi-megawatt WECS. Due to the stated CSC advantages and the possible use SMES, the CSC is the converter explored in the thesis. The CSC low dynamic performance is not much issue in this application, since the large size and high inertia of turbine blades, produce slow dynamics performance of the wind turbine. Also, the generator rating voltage is close to the grid voltage; this reduces CSC conduction losses due to boosting.

Table 2.4 Comparison between VSC and CSC.

Item	Voltage Source Converter	Current Source Converter
Switching Device	Asymmetrical with anti-parallel diode: IGBT, GTO, IGCT	Symmetrical: GTO, IGCT, RB-IGBT (or IGBT with series diode)
dc-side energy storage	dc-capacitor	dc-choke
Switching dv/dt	High	Low
Over-current/ short-circuit protection	Difficult (with IGCT), effective (with IGBT)	Effective and reliable
Dynamic performance	High	Low
PWM technique	Carrier based, SVM, SHE and hysteresis	Carrier based, SHE and SVM

2.5 Summary

This chapter discussed a number of modulation techniques that can be used to generate the gating signals for three-phase two-level VSCs and CSCs. For the VSC, SPWM, SVM and SHE were discussed. For the CSC, existing and proposed mapping techniques for converter gating signal generation, based on VSC SPWM, were presented. It was found that the proposed mapping technique decreases the logic circuitry and complexity compared to that of Espinoza [23]. SVM for the CSC was also discussed. Because SVM performs better when the switching frequency is greater than 2kHz, SVM is not be discussed further as this thesis is devoted to high-power medium-voltage applications where the switching frequency must be restricted to ensure low switching losses. The well established and proposed SHE implementations for the CSC were discussed. It has been found that the proposed new SHE implementation eliminates the 11th and 13th harmonics using one pattern, with smooth pulse angle changes, and with a fixed switching frequency; unlike the conventional method that uses two patterns with two switching frequencies.

The comparison between the VSC and the CSC represented at the end of this chapter shows that the CSC has advantages over the VSC such as: low switching dv/dt and reliable over-current/short-circuit protection. But the VSC has better dynamic response and higher efficiency than the CSC. Based on this comparison, the CSC was selected as a suitable converter for WECS use, thus will be studied within this thesis.

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Chapter 3 Proposed Current Source Converter Control Schemes

This chapter discusses current source inverter (CSI) and the current source rectifier (CSR) control systems in the synchronous reference frame, where Park's Transformation is used to simplify the both models. This transformation allows the use of simple proportional integral (PI) controllers to eliminate steady state errors. To enable variable frequency operation, as will be discussed in later chapters, a phase locked loop (PLL) uses weighted least-squares estimation (WLSE) to estimate the grid angle and frequency, and discussed in Appendix A. The CSI control strategy in islanded and grid mode, and also that of the CSR, are considered. Control loops are necessary to facilitate system operation with independent control of active and reactive powers, low total harmonic distortion current, and voltage harmonic distortion THD, stable dc load voltage from the CSR, and fast and adjustable ac load voltage for the CSI in islanded mode. The dual-bridge CSR and CSI for medium-voltage high-power applications are also discussed in this chapter, including the control systems. The proposed control schemes will be used to controller the grid delivered active and reactive power in wind energy application; as will be shown in Chapter seven.

3.1 Park's Transformation

The invariant power Park's Transformation used in this chapter aims to simplify system modelling and control, since in the dq synchronous reference frame all states variables become dc quantities. This makes conventional controllers such as PI sufficient to eliminate steady state error, in addition to the elimination of the time-varying nature of an ac system [1, 2].

The Park's transformation C used throughout this thesis to transform ac quantities from phase variables 'abc' to 'dq' is defined as [3, 4]:

$$C = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (3.1)$$

The inverse C^{-1} is used to convert from (dq0) to (abc) frames:

$$C^{-1} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \quad (3.2)$$

3.2 The Current Source Inverter

For many years, in medium-voltage high-power motor drives, CSI based drive systems were preferred over VSI based systems due to the following advantages: high power capability, excellent short circuit protection, controlled dc-link current, and motor-friendly waveforms [5]. Also, it was difficult to use a VSI in medium voltage applications, because high-voltage power electronics switches were not available and technology for series connection of self-commutated semiconductor devices was not readily viable [5]. On the other hand, the CSI can use high power reverse blocking switching devices such as IGBTs, which can be series connected [6-8]. The online-gating requirements of the CSI drive system are more complicated than for a VSI; for example, SPWM requires a mapping circuit that converts VSI to CSI gating signals. For this reason, the use of off-line stored pattern generation based on SHE is widely used to overcome this problem [9, 10]. In general, the CSI has a slower dynamic response than VSI, as its large dc-link inductance dominates the rate at which its dc link current (power) can be change.

Although the CSI has advantages over the VSI, its weight, size, losses and cost of its dc-link inductance limit its applications to early generation high-power motor drives. This is attested by the dwindling CSI research, while that on the VSI is thriving. Nowadays superconductor technology permits development of a dc link inductor with reduced weight, losses and size. At modest power levels, the 900V reverse blocking insulated gate bipolar transistor (RB-IGBT) allows removing of the series diode from the pulse width modulated CSI; thus, its semiconductor loss is decreased

[11, 12]. Additionally, recent developments in microprocessor technology programming techniques make the CSI applicable to many areas. The following shows applications where the CSI has potential to replace the VSI, while providing the same or better performance and efficiency:

- In medium-voltage high power-induction motor drive systems, the CSI continues to challenge the VSI [13, 14]. Especially, as control techniques (V/F) and vector control have good steady-state performance despite the low CSI dynamic response [9, 15].
- In electric vehicles, with a VSI the large electrolytic dc-link capacitor is limiting due to its short lifetime, expense and unreliability[16]. A film capacitor is used due to its long service life and self-healing capability, but it is bulky and expensive.[16-18] proposes some solutions to decreasing the dc-link capacitor size. The use of reliable and long-life dc link inductance in a CSI is attractive [19-24]. The authors in [19, 20] use a CSI with a dc-dc converter to drive a permanent magnet synchronous motor. In [22-24] the authors use the CSI in a brushless permanent magnet machines drive, and utilize the CSI boosting ability to extend the constant torque and constant power regions.
- For islanded loads, the authors in [25-28] replace the VSI with a CSI and improve CSI voltage control, to make it applicable for standalone applications like an uninterruptible power supply and a programmable ac source to an island load.
- In static synchronous compensator (STATCOM) applications most research focuses on the VSI, with little consideration given to the CSI. In [29-31], the authors consider a CSI based STATCOM due to the advantages it offers over the conventional VSI based STATCOM, like:1) dc-link inductance improves short circuit protection,2) unidirectional nature of the switches, 3) fast start-up and the energy storage devices do not need current limiting or a rectifier during start-up.
- In grid connected inverter applications, a pulse-width modulated CSI can provide independent control of active and reactive powers at the point of common coupling, as with a VSI[32, 33]. It has gained attention over the VSI

in photovoltaic (PV) and fuel cells applications due to its voltage boosting ability [7, 34]. The CSI can match the VSI and satisfy most wind energy conversion system (WECS) requirements such as: maximum power point tracking, low voltage ride-through capability, and sinusoidal grid current [35, 36].

3.2.1 The CSI in island mode

In island mode, a PWM-CSI must operate in an output voltage controlled mode where it defines the load voltage and output frequency. In this case, to create a current source, the CSI will be supplied from a fixed dc link voltage source followed by an inductor.

i Dynamic model of a CSI in islanding mode

Figure 3.1(a) shows a CSI equivalent circuit that describes its two fundamental states. The first state represents an ac current injection mode, where two switching devices from different phases (one from an upper arm and other from a lower arm) are turned on simultaneously. This state transfers the electromagnetic energy stored in the dc link inductance (L_{dc}) to the load. In this state, the pre-filter ac current for phases ‘a’ and ‘b’ for example when S_1 and S_6 are on are $i_{ia}=I_{dc}$ and $i_{ib}=-I_{dc}$ respectively. The second state represents the dc link inductor energising mode, and is achieved by turning on any two switching devices in the same phase-leg simultaneously. During this state, the CSI output filter capacitor supplies the load current; thus, the pre-filter load current i_{ia} for phase ‘a’ as an example will be zero (this corresponds to $S_1=S_4=1$). This shows this state is associated with the generation of zero current vectors during each switching cycle. Merging these two fundamental CSI states provides the equivalent circuit in Figure 3.1(b). On this basis, the CSI pre-filter ac currents and dc-link current can be expressed using switching functions as [20, 23, 24]:

$$\begin{cases} i_{ia} = S_1 I_{dc} - S_4 I_{dc} \\ i_{ib} = S_3 I_{dc} - S_6 I_{dc} \\ i_{ic} = S_5 I_{dc} - S_2 I_{dc} \end{cases} \quad (3.3)$$

Where i_{ia} , i_{ib} , and i_{ic} are the CSI output currents, I_{dc} is the dc-link current, and S_1 to S_6 represent the CSI switch state.

The relation between load voltages and ac filter capacitors current are:

$$\begin{cases} i_{ca} = C_i \frac{dv_{La}}{dt} = i_{ia} - i_{La} \\ i_{cb} = C_i \frac{dv_{Lb}}{dt} = i_{ib} - i_{Lb} \\ i_{cc} = C_i \frac{dv_{Lc}}{dt} = i_{ic} - i_{Lc} \end{cases} \quad (3.4)$$

CSI dc side dynamics can be expressed in terms of the voltage across dc-side inductor as in (3.5):

$$L_{dc} \frac{dI_{dc}}{dt} = V_{dc} - V_{in} - R_{dc} I_{dc} \quad (3.5)$$

Where the load voltages are v_{La} , v_{Lb} , and v_{Lc} ; the load currents are i_{La} , i_{Lb} , and i_{Lc} ; load resistance is R_L ; load inductance is L_L ; the capacitor currents are i_{ca} , i_{cb} , and i_{cc} ; V_{dc} is the supply voltage, L_{dc} is the dc-link inductance, and R_{dc} is the dc-link inductor internal resistance.

The CSI input terminal voltage V_{in} can be expressed in terms of the switch states and the ac load voltages by:

$$V_{in} = v_{La}(S_1 - S_4) + v_{Lb}(S_3 - S_6) + v_{Lc}(S_5 - S_2) \quad (3.6)$$

The system equations can be rewritten in the dq frame as follows[20]:

$$i_{id} = m_d I_{dc} \quad (3.7)$$

$$i_{iq} = m_q I_{dc} \quad (3.8)$$

$$V_{in} = \frac{3}{2} (m_d v_{Ld} + m_q v_{Lq}) \quad (3.9)$$

$$\begin{cases} m_d = m \cos(\alpha) \\ m_q = m \sin(\alpha) \end{cases} \quad (3.10)$$

Where m_d and m_q are the d-q components of the modulation index, m ; ω is the supply frequency in rad/s; and α is the phase angle of CSI output current.

Since the load voltage is the input for the PLL, the q component of the load voltage will equal zero ($v_{Lq}=0$), and equations (3.4) and (3.5) can be written in the dq frame as:

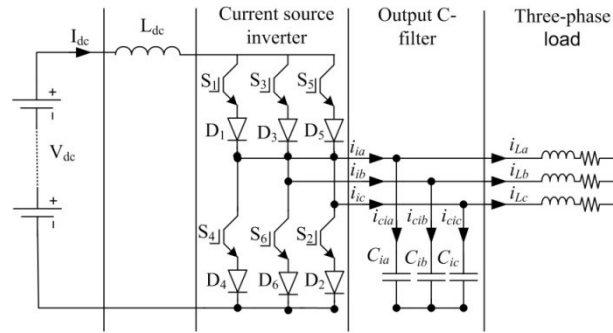
$$\frac{dv_{Ld}}{dt} = \frac{i_{id}}{C_i} - \frac{1}{C_i} i_{Ld} \quad (3.11)$$

$$i_{iq} = \omega C_i v_{Ld} + i_{Lq} \quad (3.12)$$

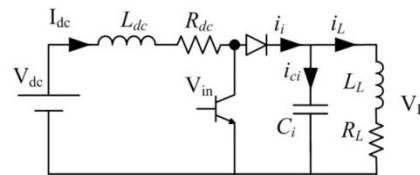
$$\frac{dI_{dc}}{dt} = -\frac{3}{2} \frac{m_d}{L_{dc}} v_{Ld} - \frac{R_{dc}}{L_{dc}} I_{dc} + \frac{1}{L_{dc}} V_{dc} \quad (3.13)$$

Where v_{Ld} and v_{Lq} , and i_{Ld} and i_{Lq} are the dq components of the terminal voltages, v_L ; and load current i_L .

Equations(3.11) to (3.13) describe the dynamic mode of the CSI in the dq frame



(a) CSI



(b) single line diagram of CSI in islanded mode.

Figure 3.1CSI in islanded mode.

ii Control strategy

The proposed controller is to supply the load but it also defines the load voltage, power frequency and has the ability to overcome a load step change with minimal oscillation. Figure 3.2 shows the control system being used on the CSI in island mode in this thesis. To calculate m_d , let $U = i_{id} - i_{Ld}$, therefore equation (3.11) can be rewritten as:

$$C_i \frac{dv_{Ld}}{dt} = U \quad (3.14)$$

The variables U can be obtained from the proportional-integral (PI) controller as follows:

$$U = K_{p1}(v_d^* - v_d) + K_{i1} \int (v_d^* - v_d) \quad (3.15)$$

Where: K_{p1} and K_{i1} are the proportional and integral gains respectively for the outer control loop.

The load and the ac-side C-filter q current components are compensated by adapting m_q as shown in the following equation:

$$m_q = \frac{\omega C_i v_{Ld} + i_{Lq}}{I_{dc}} \quad (3.16)$$

m_d and m_q are the d and q components of the modulation index m , and α is the inverter load angle which has to be added to angle ωt , where ωt is derived from the phase lock loop (PLL), to give the reference angle required by SHE and SVM gate signal generators. For SPWM m_d and m_q are converted from the dq frame to the abc frame using equation (3.2). The conversion output provides the three-phase reference signals for the SPWM which is compared with a high frequency triangular carrier signal; the output from the comparison feeds the proposed mapping technique to provide the CSI gate signals.

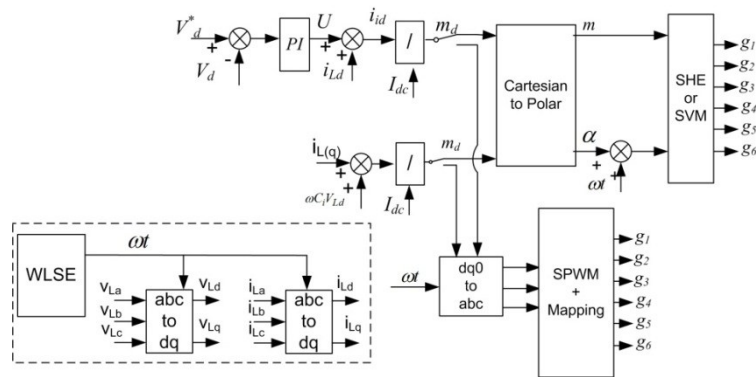


Figure 3.2 Proposed control strategy of CSI in island mode.

iii Simulation results

CSI operation in islanding mode is illustrated using PSCAD/EMTDC computer simulation, with the system parameters in Table 3.1 and the control system depicted in Figure 3.2. Simulation results presented in this section are obtained with three different modulation techniques:

- SPWM with the mapping technique discussed in Chapter two
- SHE modulation
- SVM and its comparison with mapped SPWM and SHE.

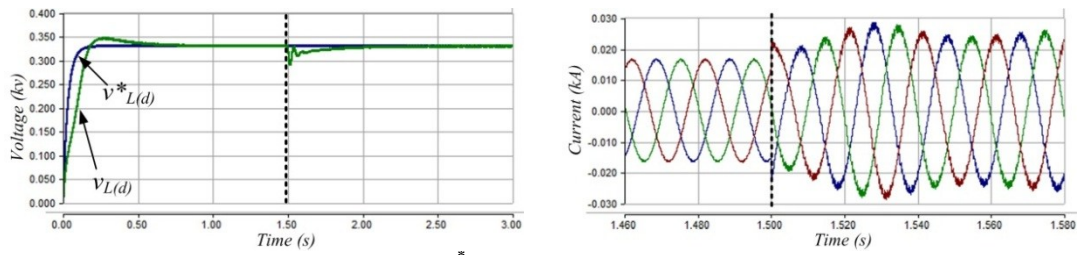
a) Mapped SPWM switching technique

This section uses SPWM with the controller in Figure 3.2 to simulate the CSI in islanding mode, during two cases. Initially, the set-point for the peak of the load voltage (V_{Ld}^*) set to 0.33kV when the three phase load consists of 20Ω resistance in series with 5mH inductance. At time $t=1.5s$, an additional three-phase resistive load of 35Ω is connected in shunt with the initial load.

Figure 3.3 shows the simulation results with mapped SPWM with a 1.2 kHz switching frequency. Figure 3.3 (a) and (b) show the load voltage magnitude and three-phase load currents when the CSI is operated in islanding mode. Figure 3.3(a) show that with the basic controller in Figure 3.2, the CSI is able to maintain constant load voltage as the load varies. Figure 3.3(b) shows the CSI injects high quality sinusoidal current into the load.

Table 3.1 CSI in island mode simulation parameters

Parameter	value
V_{dc}	0.12kV
L_{dc}	10mH
R_{dc}	0.02Ω
C_i	105μF Y-connected
R_L - L_L	20Ω and 5mH Y-connected
step load	40Ω Y-connected

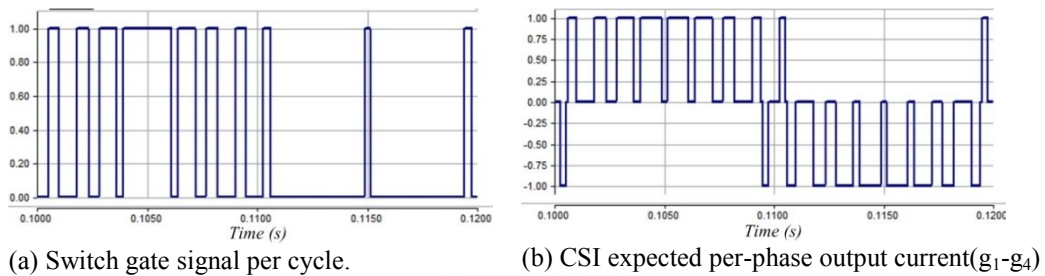


(a) reference maximum output voltage V_{Ld}^* and V_{Ld} (b) load current

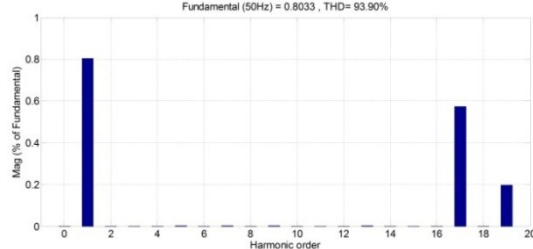
Figure 3.3 CSI controller performance in island mode, when using the mapped SPWM switching technique.

b) SHE switching

This section simulates the CSI in islanding mode with the same parameters and controller system as in Figure 3.2. In this illustration, SHE is used to eliminate the 5th, 7th, 11th and 13th harmonics from the pre-filter output phase currents. Figure 3.4(a), (b) and (c) show SHE gating signals at 0.8 modulation index, the gate signals of switch S_4 subtracted from that of the switch S_1 (which is expected to be similar to the pre-filter output phase current), and spectrum of the output phase current. The gate signal in Figure 3.4(a) consists of 10 pulses per fundamental cycle, and this means for a 50Hz fundamental frequency, the equivalent switching frequency per device is $50 \times 10 = 500\text{Hz}$. The output phase current FFT in Figure 3.4(c) shows that the 5th, 7th, 11th and 13th harmonics are eliminated from the phase current, and the peak of the fundamental output current is 80% of the dc link current. Figure 3.5(a) and (b) show SHE is able to reproduce the results obtained by the mapped SPWM technique, but with slightly higher output current ripple.

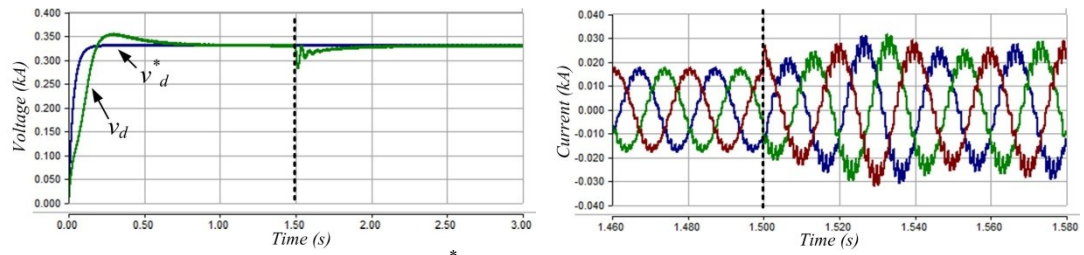


(a) Switch gate signal per cycle. (b) CSI expected per-phase output current(g_1-g_4)



(c) CSI expected per-phase output current FFT

Figure 3.4 Waveforms show the SHE gate signals.



(a) reference maximum output voltage V_{Ld}^* and V_{Ld} (b) load current

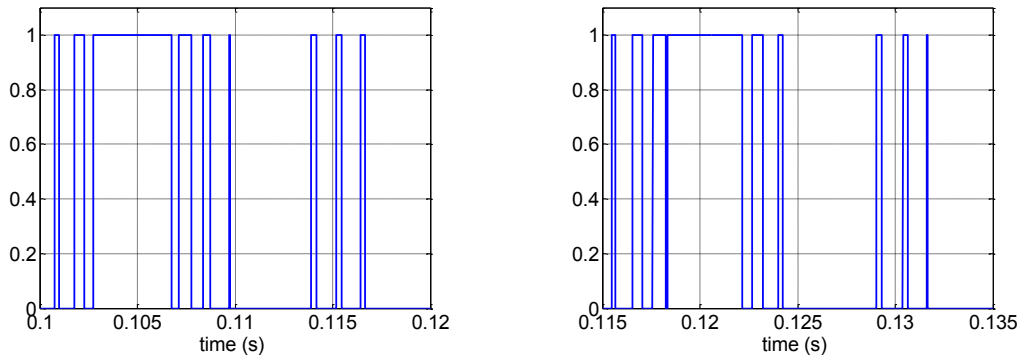
Figure 3.5 Performance waveforms of the CSI controller in island mode, using SHE switching.

c) Comparison between mapped SPWM, SVM and SHE

In this section, an open loop test is carried out using the system parameters listed in Table 3.1 and a fixed modulation index of $m=0.8$. For the mapped SPWM, a carrier frequency is selected such as the minimum frequency that gives load current with a THD less than 5%. The SVM sampling frequency is similarly selected, while the SHE eliminates the 5th, 7th, 11th and 13th harmonics. The gate signal per switch when using SHE, mapped SPWM and SVM is shown in Figure 3.4(a), Figure 3.6(a) and Figure 3.6(b) respectively. Table 3.2 shows the pre-filter inverter output current harmonic analyses; where SHE is able to eliminate the harmonics from the 5th to the 13th inclusive, but the magnitude of harmonics from 17th and above are higher when compared with the other two modulation techniques.

In terms of the load current THD profile; mapped SPWM and SVM satisfy IEEE Standard 519-1992 for medium voltage [37]. But for the SHE, the 17th harmonics order is slightly higher than allowed; this can be solved by increasing the size of ac side C-filter or by compromising with the lower order harmonics reduced but not eliminated. A table 3.2 show IEEE Standard 519-1992 and Table 3.3 confirms that SVM is the optimal switching technique.

In this thesis the preferred switching technique is SHE. SHE has the ability to eliminate specific low order harmonics, like the 11th and 13th, while higher order harmonic orders are eliminated by the transformer. Only SHE can perform this task with a low switching frequency of 300Hz.



(a) Switch gate signal per cycle using PWM plus mapping technique. (b) Switch gate signal per cycle using SVM.

Figure 3.6 Waveforms of mapped SPWM and SVM modulation gate signals.

Table 3.2 Pre-filter current harmonic analysis

Modulation technique	Frequency	THD	Harmonics (% of fundamental)								
			1 st	5 th	7 th	11 th	13 th	17 th	19 th	23 rd	25 th
Mapped SPWM	Sampling frequency=750Hz Switching frequency=450Hz	77.84%	100%	0.31%	0.11%	2.32%	1.03%	26.00%	0.26%	0.77%	4.69%
SVM	Carrier frequency=850Hz Switching frequency=450Hz	77.81%	100%	0.77%	1.91%	0.64%	7.69%	1.2%	24.34%	5.36%	2.37%
SHE	Switching frequency=500Hz	93.57%	100%	0.0%	0.0%	0.0%	0.0%	73.97%	20.49%	1.89%	0.27%

Table 3.3 Load current harmonic analysis

Modulation technique	THD	Harmonics (% of fundamental)								
		1 st	5 th	7 th	11 th	13 th	17 th	19 th	23 rd	25 th
Mapped SPWM	4.960%	100%	0.11%	0.03%	0.3%	0.0%	1.68%	0.01%	0.03%	0.15%
SVM	4.760%	100%	0.27%	0.45%	0.09%	0.77%	0.08%	1.29%	0.2%	0.08%
SHE	4.960%	100%	0.0%	0.0%	0.0%	0.0%	4.77%	1.09%	0.07%	0.01%

3.2.2 Grid connected CSI

As with a VSI, a grid-connected CSI is expected to offer the following features:

- 1) Meet power quality requirements at the point of common coupling (PCC) (low voltage and current THD, injected sinusoidal output current, and low dv/dt) and
- 2) Independent control of active and reactive powers delivered to the grid.

As with grid connected VSI, a grid connected CSI is most likely to be controlled such that it regulates the amount of active and reactive power it exchanges with ac

grid. The ac current controller must to act as first line of defence during low-voltage ride-through, as demanded in the grid code. In the internal model based control design, the first step for CSI controller design is to derive the system transfer function. In this thesis, a state-space representation is used to derive the system transfer function, which later is use to select the controller gains.

The standard state-space representation form is [31]:

$$\dot{x} = Ax + Bu \quad (3.16)$$

$$y = Cx + Du \quad (3.16)$$

Where x is the vector of state variables ($n \times 1$), \dot{x} is the time derivative of the state vector ($n \times 1$), u is the input ($m \times 1$), y is the output vector ($z \times 1$), A is the system matrix ($n \times n$), B is the input matrix ($n \times m$), C is the output matrix ($z \times n$), and D is the feed forward matrix ($m \times m$).

i CSI dynamics equations

Figure 3.7 shows a single-line diagram of a grid-connected CSI. The resistance and inductance of the distribution line are represented by R_s and L_s respectively. From Figure 3.7 the differential equations that describe the inverter ac-side and dc-side dynamics, when considering only fundamental ac currents and voltages, are:

$$i_i = C_i \frac{dv_{ci}}{dt} + i_s \quad (3.17)$$

$$v_{ci} = L_s \frac{di_s}{dt} + R_s i_s + v_s \quad (3.18)$$

$$L_{dc} \frac{dI_{dc}}{dt} = V_{dc} - V_{in} \quad (3.19)$$

The inverter dynamics can be expressed in the dq axis reference frame as:

$$\frac{dI_{dc}}{dt} = \frac{1}{L_{dc}} (V_{dc} - V_{in}) - \frac{R_{dc}}{L_{dc}} I_{dc} \quad (3.20)$$

$$\frac{dv_{cid}}{dt} = \frac{1}{C_i} m_d I_{dc} + \omega v_{ciq} - \frac{1}{C_i} i_{gd} \quad (3.21)$$

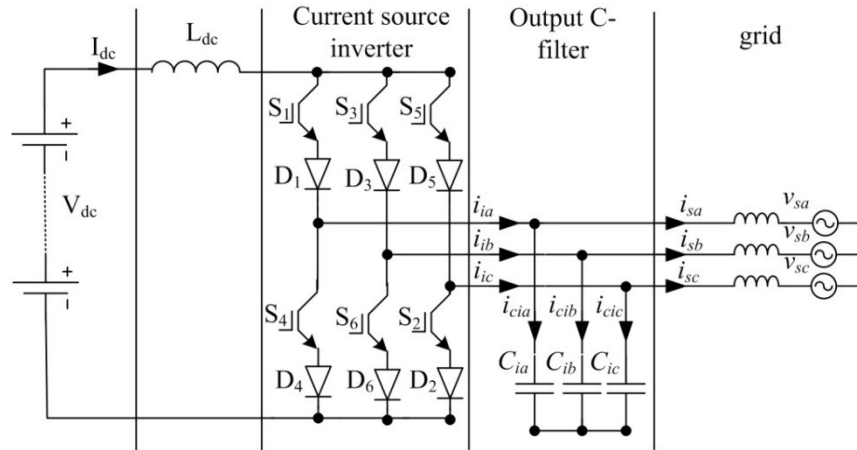
$$\frac{dv_{ciq}}{dt} = \frac{1}{C_i} m_q I_{dc} - \omega v_{cid} - \frac{1}{C_i} i_{gq} \quad (3.22)$$

$$\frac{di_{gd}}{dt} = \frac{1}{L_i} v_{cid} + \omega i_{gq} - \frac{R_g}{L_i} i_{gd} - \frac{1}{L_i} v_{gd} \quad (3.23)$$

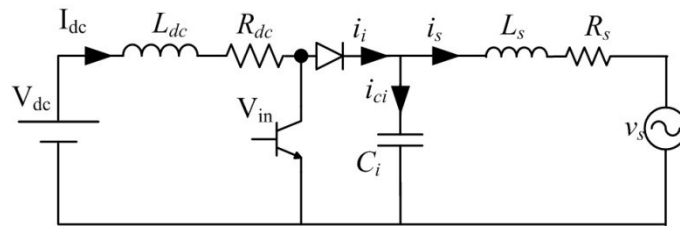
$$\frac{di_{gq}}{dt} = \frac{1}{L_i} v_{ciq} - \omega i_{gd} - \frac{R_g}{L_i} i_{gq} \quad (3.24)$$

Where the grid voltage v_s has only d component v_{ds} while the q component is $v_{qs}=0$. Since the d-axis is aligned to the voltage vector. i_{sd} and i_{sq} are the dq components of the grid current.

The dc-side dynamic equation is expressed in (3.20). Equations (3.21) and (3.22) express the capacitor filter voltage dynamics, and the grid current dynamics are described in equations (3.23) and (3.24).



(a) CSI in grid connection mode.



(b) single line diagram of grid connected CSI

Figure 3.7 CSI in grid connection mode, and single line diagram of grid connected CSI.

ii CSI grid delivered active and reactive power proposed controller.

It is required to provide independent control of the grid delivered active and reactive power. Figure 3.8 shows the CSI control system block diagram. The grid active power controller consists of two control loops, in the outer control loop equation (3.25) is used to calculate the reference grid d-component current i_{gd}^* , the error between i_{gd}^* and i_{gd} passes through the outer PI controller which estimates the Z_{dc1} . Z_{dc1} is used to calculate the reference dc-link current I_{dc}^* for the inner control loop, the error between I_{dc}^* and I_{dc} passes through the inner PI controller to estimate m_d . The reactive power controller calculates the required i_{gq}^* from equation (3.26), and a PI controller is used to calculate the value of m_q from the error between i_{gq}^* and i_{gq} . m_d and m_q reused to get the modulation index m for SHE gate signal generator, and the angle α which added to angle ωt , derived from the phase locked loop (PLL), to give the reference angle required by the SHE gate signal generator.

$$P_g^* = \frac{3}{2} v_{gd} i_{gd}^* \quad (3.25)$$

$$Q_g^* = \frac{3}{2} v_{gd} i_{gq}^* \quad (3.26)$$

To facilitate current regulator design the term $(V_{dc} - V_{in})$ can be replaced by control variable Z_{dc1} (where $Z_{dc1} = V_{dc} - V_{in}$), similarly $Z_{d1} = m_d I_{dc}$ and $Z_{q1} = m_q I_{dc}$. Where Z_{dc1} , Z_{d1} and Z_{q1} can be estimated from PI controller as follow:

$$Z_{dc1} = (V_{dc} - V_{in}) = K_{p1}(i_{gd}^* - i_{gd}) + K_{i1} \int (i_{gd}^* - i_{gd}) = K_{p1}(i_{gd}^* - i_{gd}) + \lambda_{dc1} \quad (3.27)$$

$$Z_{d1} = m_d I_{dc} = K_{p2}(I_{dc}^* - I_{dc}) + K_{i2} \int (I_{dc}^* - I_{dc}) = K_{p2}(I_{dc}^* - I_{dc}) + \lambda_{d1} \quad (3.28)$$

$$Z_{q1} = m_q I_{dc} = K_{p3}(i_{gq}^* - i_{gq}) + K_{i3} \int (i_{gq}^* - i_{gq}) = K_{p3}(i_{gq}^* - i_{gq}) + \lambda_{q1} \quad (3.29)$$

$$\frac{d\lambda_{dc1}}{dt} = K_{i1}(i_{gd}^* - i_{gd}) \quad (3.30)$$

$$\frac{d\lambda_{d1}}{dt} = K_{i2}(I_{dc}^* - I_{dc}) \quad (3.31)$$

$$\frac{d\lambda_{q1}}{dt} = K_{i3}(i_{gq}^* - i_{gq}) \quad (3.32)$$

Differential equations (3.20)to (3.32) can be written in state space form as:

$$\frac{d}{dt} \begin{bmatrix} I_{dc} \\ \lambda_{dc1} \\ v_{cid} \\ \lambda_{d1} \\ v_{ciq} \\ \lambda_{q1} \\ i_{gd} \\ i_{gq} \end{bmatrix} = \begin{bmatrix} \frac{-R_{dc}}{L_{dc}} & \frac{1}{L_{dc}} & 0 & 0 & 0 & 0 & \frac{-K_{p1}}{L_{dc}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -K_{i(1)} & 0 \\ \frac{-K_{p2}}{C_i} & 0 & 0 & \frac{1}{C_i} & \omega & 0 & \frac{-1}{C_i} & 0 \\ 0 & 0 & 0 & -K_{i2} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\omega & 0 & 0 & \frac{1}{C_i} & 0 & \frac{-(K_{p3}+1)}{C_i} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -K_{i3} \\ 0 & 0 & \frac{1}{L_i} & 0 & 0 & 0 & \frac{-R_g}{L_i} & \omega \\ 0 & 0 & 0 & 0 & \frac{1}{L_i} & 0 & \frac{-R_g}{L_i} & -\omega \end{bmatrix} \begin{bmatrix} I_{dc} \\ \lambda_{dc1} \\ v_{cid} \\ \lambda_{d1} \\ v_{ciq} \\ \lambda_{q1} \\ i_{gd} \\ i_{gq} \end{bmatrix} + \begin{bmatrix} 0 & 0 & \frac{K_{p1}}{L_{dc}} & 0 \\ 0 & 0 & K_{i1} & 0 \\ 0 & \frac{K_{p2}}{C_i} & 0 & 0 \\ 0 & K_{i2} & 0 & 0 \\ 0 & 0 & 0 & \frac{K_{p3}}{C_i} \\ 0 & 0 & 0 & K_{i3} \\ 0 & \frac{-1}{L_i} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{gd} \\ I_{dc}^* \\ i_{gd}^* \\ i_{gq}^* \end{bmatrix} \quad (3.33)$$

Equation (3.33) shows the overall state matrix that governs the grid current i_{gd} and i_{gq} and dc-side current I_{dc} controllers. The controller gains used are obtained by fine-tuning based on Eigen-value analysis of the overall state matrix.

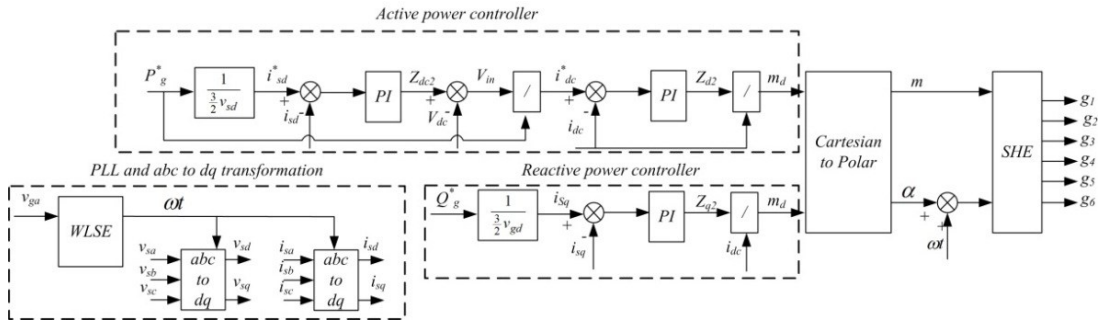


Figure 3.8 CSI control system block diagram

iii Simulation results

A three-phase grid connected CSI is simulated in this section using PSCAD/EMTDC, with the system parameters in Table 3.4. Initially, the reference active power is set to 1 MW (case1); and at $t=3.5s$, the reference active power is increased from 1MW to 1.5MW in a step fashion (case2); and its reactive power exchange with the grid is maintained at zero throughout. This scenario is chosen to illustrate the dynamic performance of the grid connected CSI when it is controlled as illustrated in Figure 3.8.

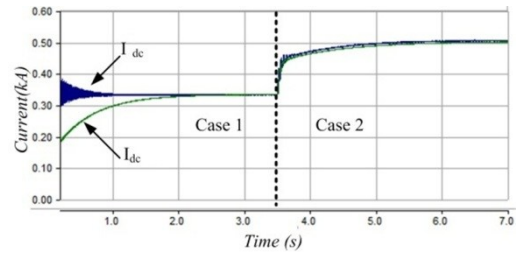
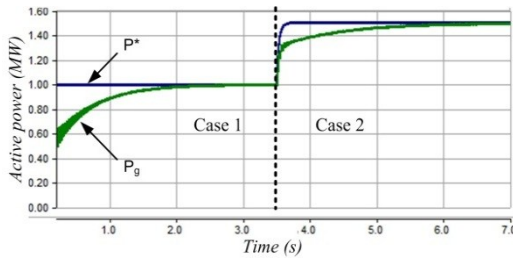
Figure 3.9 and Figure 3.10 show the simulation results of the grid connected CSI. Figure 3.9(a) shows that the proposed controller successfully follows the reference active power with minimum oscillation, while Figure 3.9(b) shows that the inner dc-link current controller regulates the dc-link current with minimum transient time to adapt the active power delivered to the grid. Reactive controller operation is observed in Figure 3.10(a) and (b). Since the reference reactive power is zero, this tends to make the CSI controller force the grid current to be in phase with the grid voltage (unity power factor) as shown in Figure 3.10(a) and (b). In Figure 3.10(a) and (b) the CSI successfully delivers to the grid sinusoidal current with low total harmonics distortion (THD). Figure 3.10(b) show the dc-link current during the step increase in the reference delivered power to the grid, where the current increases smoothly with minimal oscillation.

The performance of the reactive power controller is tested by setting the reference grid delivered active power to a fixed value of 1.5MW and by changing the grid reference delivered reactive power Q_g^* . At the beginning Q_g^* is set to 0.5MVAR (case 1), then after 3s Q_g^* step changes to zero (case 2), again after 3s more, the Q_g^* step changes to -0.5MVAR (case 3). This test will show the ability of the proposed controller to independently control the active and reactive powers. The simulation results are shown in Figure 3.11 and Figure 3.12. From Figure 3.11(a) the proposed controller keeps the grid delivered active power fixed during the simulation for the three different cases. Figure 3.11(b) shows that the proposed controller tracks the reference reactive power without oscillation and minimal transient time. Figure 3.12(a) to (c) show phase 'a' grid voltage and current, where in Figure 3.12(a) the grid current is leading, in Figure 3.12(b) the grid current is in-phase, and in Figure 3.12(c) the grid current is lagging.

The simulation results of the grid connected CSI, show that the proposed CSI is able to send to the grid high quality sinusoidal current with controlled active and reactive powers. These features qualify the CSI for WECS and PV applications.

Table 3.4 Grid connected CSI system parameters

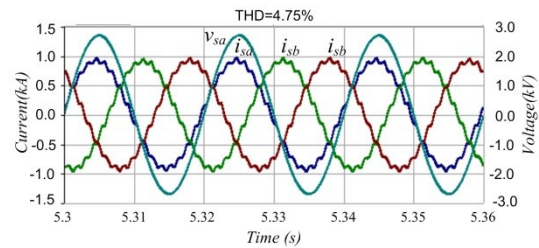
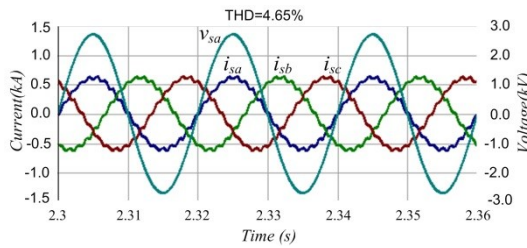
Parameter	Value
Supply voltage V_{dc}	3kV
dc-link inductance L_{dc}	20mH
Ac side C-filter	180 μ F Y connected
Transmission line equivalent inductance	1.5mH
Transmission line equivalent resistance	0.2 Ω
Grid voltage	3.3kV



(a) Grid reference active delivered power and grid delivered power.

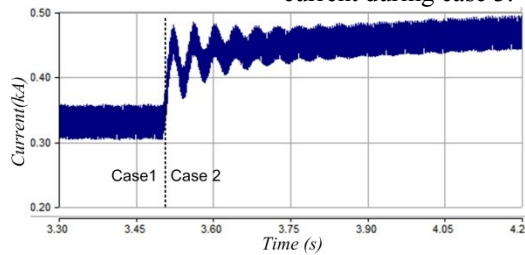
(b) dc-link reference current and actual dc-link current.

Figure 3.9 Waveforms of the overall performance of the proposed controller of grid connected CSI.



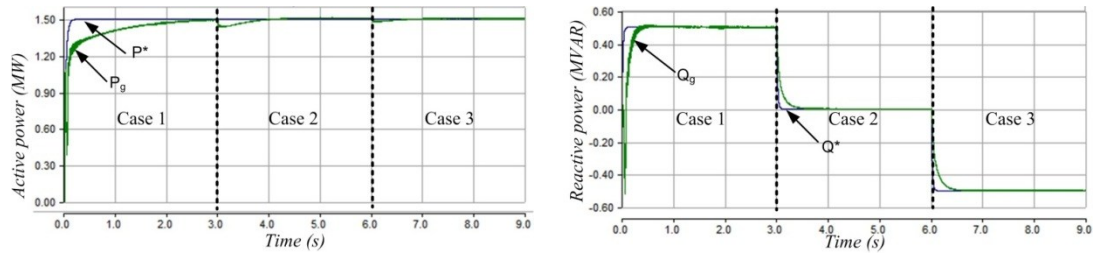
(a) Phase voltage 'a' and the three-phase grid current during case 1.

(b) Phase voltage 'a' and the three-phase grid current during case 3.



(c) dc-link current during the step change in reference active power delivered to the grid.

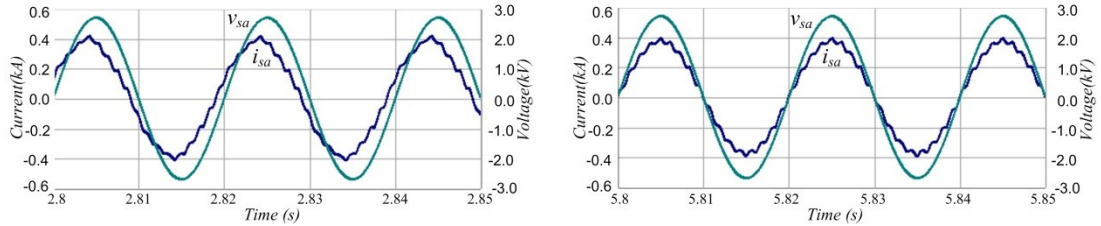
Figure 3.10 Detailed view of grid phase voltage, phase current and dc-link current of grid connected CSI.



(a) Grid delivered active power

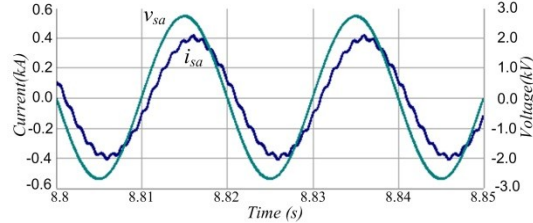
(b) Grid delivered reactive power

Figure 3.11 Waveforms of the performance of the CSI reactive power controller.



(a) Grid phase 'a' voltage and current at $P^*=1.5\text{MW}$ and $Q^*=0.5\text{MVAR}$

(b) Grid phase 'a' voltage and current at $P^*=1.5\text{MW}$ and $Q^*=0\text{MVAR}$



(c) Grid phase 'a' voltage and current at $P^*=1.5\text{MW}$ and $Q^*=-0.5\text{MVAR}$

Figure 3.12 Grid phase 'a' voltage and current for each test case of CSI reactive power controller.

3.3 Current source rectifier

Current source rectifier (CSR) is a converter where the power flow is from ac to dc side, with the converter designed to regulate the dc voltage or current. It can be found in applications such as UPS, WECS, and motor drive systems. References [1, 4, 38] discuss different CSR control strategies, all based on using the synchronously rotating reference frame. These control strategies employ two-layer closed loops; one for regulating the dc-link current, the other for grid reactive current compensation for high power factor operation. A synchronous reference frame allows the use of conventional PI controllers and steady state errors are eliminated, with an acceptable dynamic response. The CSR replaces the thyristor based rectifiers in medium voltage horsepower drive applications as shown in [39-41]. In [35, 39] the CSR was used as front end converter in WECS, where the CSR successfully extracted maximum power from the wind turbine by regulating the generator speed to optimal speed, where the turbine gives its maximum power.

3.3.1 CSR modelling

Based on the single line diagram of the CSR shown in Figure 3.13, equations(3.34) and (3.35) represent the ac-side CSR dynamics.

$$C_s \frac{dv_{Cs}}{dt} = i_s - i_r \quad (3.34)$$

$$L_s \frac{di_s}{dt} = v_s - R_s i_s - v_{cs} \quad (3.35)$$

Where C_s is the output C-filter capacitance, v_{cs} is the per-phase voltage across C-filter capacitor, i_s is the grid current, i_r is the CSR pre-filter input current, L_s is the ac-side filter inductance, and R_s is the internal resistance of the ac-side filter inductor.

Equations(3.36) and (3.37) show the dc-side dynamics.

$$I_{dc} = I_{Cdc} + I_L \quad (3.36)$$

$$L_{dc} \frac{di_{dc}}{dt} = V_{in} - R_{dc} i_{dc} - V_L \quad (3.37)$$

Where I_{dc} is the dc-link current, I_{Cdc} is the dc-link capacitor filter current, L_{dc} is dc-link inductance, V_{in} is the CSR dc-side terminal voltage, R_{dc} dc-side inductance internal resistance and V_L is load voltage.

To simplify the model it is assumed that internal resistances R_s and R_{dc} are significantly small, so can be neglected. The main dc-side energy storage elements the dc-link inductance L_{dc} , the C-filter is added to perform smoothing of the load voltage. It is selected to be less than 150 μ F, which is small in comparison with conventional voltage source rectifiers where the value can reach several thousand μ F [42, 43]. At steady state the average dc-side capacitor current over one or a number of consecutive cycles is equal to zero ($I_{dc}=I_L$).

Transformation to the dq frame gives

$$\frac{dv_{Csd}}{dt} = \frac{1}{C_s} i_{sd} - \frac{m_d}{C_s} i_{dc} + \omega v_{Cq} \quad (3.38)$$

$$\frac{dv_{Csq}}{dt} = \frac{1}{C_s} i_{sq} - \omega v_{Csq} - \frac{m_q}{C_s} i_{dc} \quad (3.39)$$

$$\frac{di_{sd}}{dt} = \omega i_{sq} - \frac{1}{L_s} v_{csd} + \frac{1}{L_s} v_{sd} \quad (3.40)$$

$$\frac{di_{sq}}{dt} = -\omega i_{sd} - \frac{1}{L_s} v_{csq} \quad (3.41)$$

$$\frac{di_{dc}}{dt} = \frac{V_{in} - V_L}{L_{dc}} \quad (3.42)$$

3.3.2 CSR control stage

The CSR controller must provide adjustable dc voltage and sinusoidal grid current with high power factor. PF correction is an important issue for a CSR because the input capacitor makes the line PF leading, which may increase the bus bar voltage and affect other loads connected on the same bus[44].

Figure 3.14 shows the proposed CSR controller, which consists of the dc voltage regulator and grid reactive power controller. In the voltage regulator, a PI controller uses the error between the reference load voltage V_L^* and the load voltage V_L to obtain the reference dc-link current I_{dc}^* as shown in equation(3.43). I_{dc}^* is multiplied by the V_L^* to give the reference required output power. Assuming lossless conversion, for power balance, the input ac power P_{ac} equals the output dc power P_{dc} . Equation (3.44) is used to calculate the inner control loop input (grid d-component current i_{sd}^*). The error between i_{sd}^* and i_{sd} passes through a PI regulator to estimate m_d as shown in equation (3.45). The reactive power controller uses a PI controller to estimate the m_q , from the error between i_{sq}^* and i_{sq} .

$$I_{dc}^* = K_{P6}(V_{dc}^* - V_{dc}) + K_{I6} \int (V_L^* - V_{dc}) dt \quad (3.43)$$

$$i_{sd}^* = \frac{V_L^* I_{dc}^*}{\frac{3}{2} V_{sd}} \quad (3.44)$$

$$m_d = K_{P7}(i_{sd}^* - i_{sd}) + K_{I7} \int (i_{sd}^* - i_{sd}) dt \quad (3.45)$$

$$m_q = K_{P8}(i_{sq}^* - i_{sq}) + K_{I8} \int (i_{sq}^* - i_{sq}) dt \quad (3.46)$$

Where: K_{P6} and K_{i6} are the outer proportional and integral gains respectively, K_{P7} and K_{i7} are the inner proportional and integral gains respectively, while K_{P8} and K_{i8} are the reactive power controller proportional and integral gains respectively.

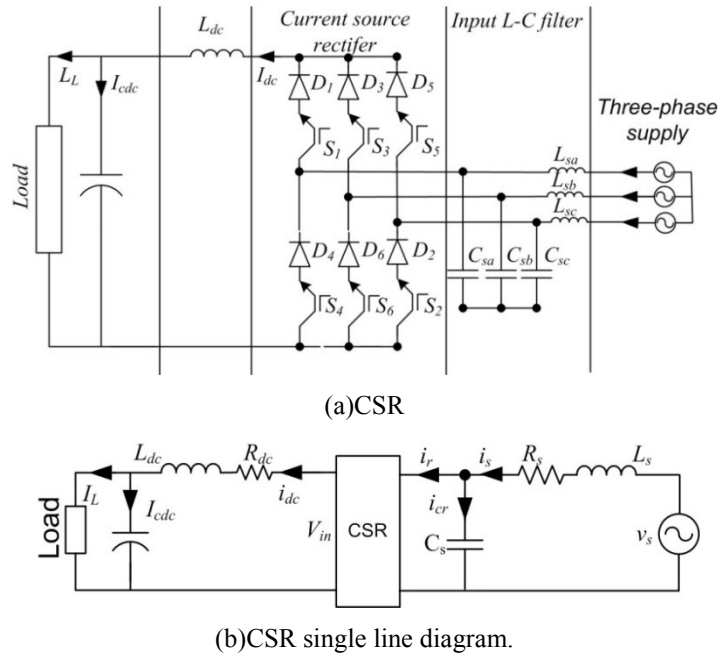


Figure 3.13 CSR and its single line diagram.

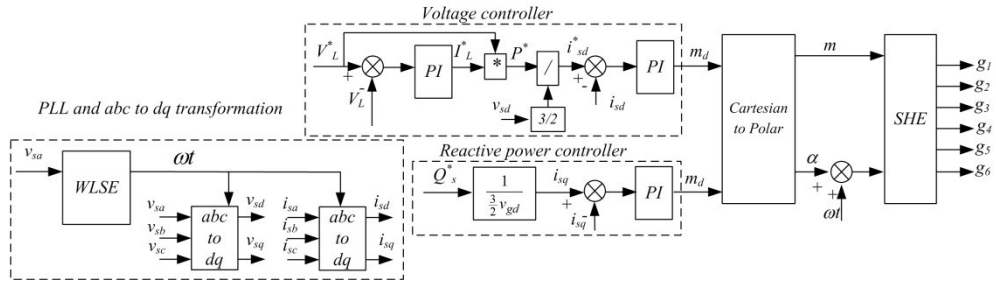


Figure 3.14 CSR proposed controller.

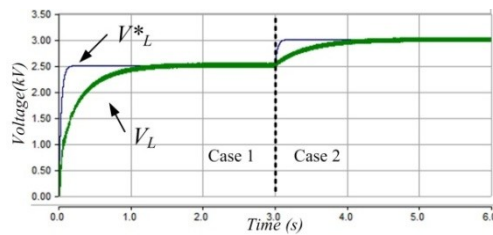
3.3.3 CSR simulation results

Figure 3.15 shows the simulation of the proposed controller and the CSR, where the overall system parameters are given in Table 3.5. The simulation scenario consists of two cases: at the beginning V_L^* is 2.5kV (case 1), then after 3s V_L^* gradually increases to 3kV (case2). The reactive power reference is always zero. Figure 3.15(a) shows that the proposed controller successfully tracks the reference load voltage without overshoot, even during a reference load voltage increase. Figure 3.15(b) show that the grid d-current component controller rapidly tracks the reference grid d-current components with minimal overshoot and undershoot. Figure 3.15(c) and (d)

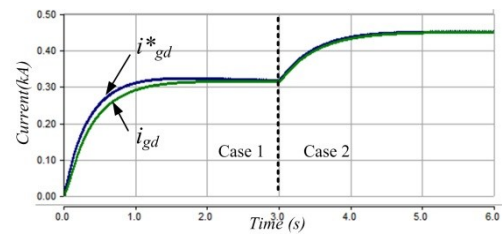
show phase voltage ‘a’ and the three-phase grid current during cases 1 and 2 respectively. The proposed CSR input current is sinusoidal with nearly unit power factor.

Table 3.5 CSR simulation system parameters.

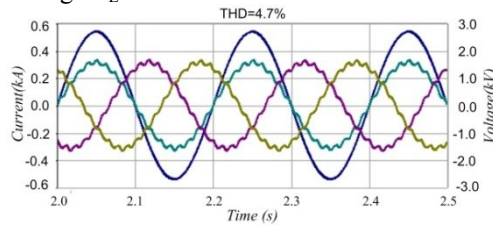
Parameter	Value
Grid voltage	3.3kV
ac-side inductance L_s	5mH
ac-side capacitance C_s	150 μ F
dc-side inductance L_{dc}	15mH
dc-side capacitance C_{dc}	150 μ F
Load resistance	5 Ω



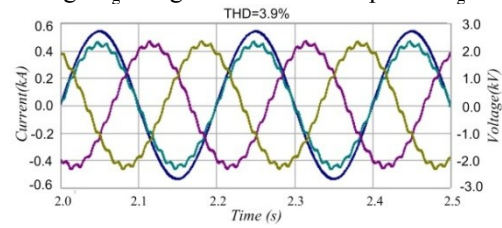
(a) The reference load voltage V_L^* and load voltage V_L .



(b) The reference grid d-current component i_{gd}^* and grid d-current component i_{gd} .



(c) Phase voltage ‘a’ and three-phase grid current during case 1.



(d) Phase voltage ‘a’ and three-phase grid current during case 2.

Figure 3.15 Simulation waveforms of the CSR.

3.4 Dual-bridge current source converter

The dual-bridge CSC is mainly used in medium-voltage high-power applications, where the switching frequency is limited and low THD grid current is required. This section discusses the dual-bridge CSR and the dual-bridge CSI. In [6, 8, 45, 46], the dual-bridge CSR is proposed as an active front end converter for medium-voltage high-power applications, where the switching frequency is limited to 350Hz without compromise to the converter’s ability to control output active and reactive power independently.

3.4.1 Dual bridge current source rectifier

Figure 3.16 show the dual-bridge CSR, which consists of two identical CSR connected in series and sourced by a phase-shifting transformer with secondary and tertiary windings delta and star connected. The primary winding is star connected. The delta winding is shifted by 30° . In the dual-bridge CSR, the transformer is used to cancel the 5th, 7th, 17th, and 19th harmonic currents [47, 48]. SHE is used to eliminate the 11th and 13th harmonics and control the fundamental current component, which in turns controls the dc-link current. With this arrangement, dual-bridge CSR draws sinusoidal input currents with a low switching frequency of 350Hz.

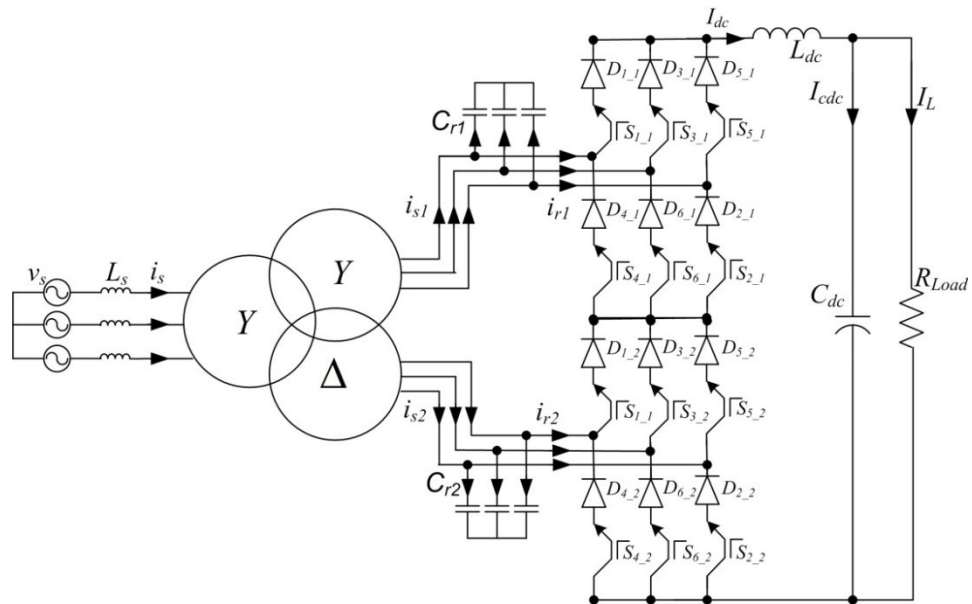


Figure 3.16 Dual-bridge CSR.

i Dual-bridge CSR modelling

Figure 3.17 shows the single line diagram of a dual-bridge CSR, assuming the line-to-line voltage of all windings are equal: $v_p=v_{s1}=v_{s2}$, and the turn ratios of the transformer secondary and tertiary windings relative to primary are $N_1/N_2=1$ and $N_1/N_3=1/\sqrt{3}$ respectively. Equations (3.47) to (3.53) describe the dynamic model of the dual-bridge CSR:

$$v_s = L_s \frac{di_s}{dt} + v_p \quad (3.47)$$

$$i_s = i_{s1} + i_{s2} \quad (3.48)$$

$$v_{s1} = L_{r1} \frac{di_{s1}}{dt} + v_{Cr1} \quad (3.49)$$

$$v_{s2} = L_{r2} \frac{di_{s2}}{dt} + v_{Cr2} \quad (3.50)$$

$$C_{r1} \frac{dv_{Cr1}}{dt} = i_{s1} - i_{r1} \quad (3.51)$$

$$C_{r2} \frac{dv_{Cr2}}{dt} = i_{s2} - i_{r2} \quad (3.52)$$

$$V_{in1} + V_{in2} = L_{dc} \frac{di_{dc}}{dt} + V_L \quad (3.53)$$

Where v_p is the transformer primary phase voltage, v_{s1} and v_{s2} are the transformer secondary phase voltage, i_s supply current, i_{s1} and i_{s2} are the transformer secondary currents, v_{Cr1} and v_{Cr2} are the voltage across the two CSR bridges, C_{r1} and C_{r2} are the two CSR bridges ac side C-filter, V_{in1} and V_{in2} are the input voltages of the two CSR bridges, L_{dc} is dc-link inductance, V_L is load voltage, L_s is the primary leakage inductance plus the inductance of the supply lines, and L_{r1} and L_{r2} are secondary Y and Δ leakage inductances- made equal[49].

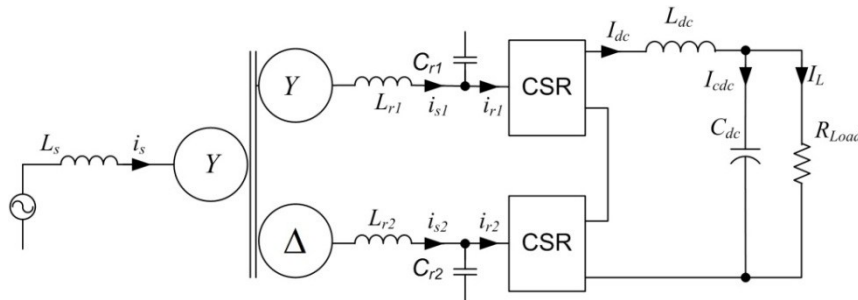


Figure 3.17 Single line diagram of dual-bridge CSR.

ii Harmonic cancellation

The single line diagram of the dual-bridge CSR in Figure 3.17 is used to simplify the analysis for the harmonic current cancellation in the primary side of the phase shifting transformer, The transformer primary current or the supply current i_s is given by equation (3.48). For a three-phase balanced system, the line currents of each transformer secondary winding i_{s1} and i_{s2} can be expressed as [46]:

$$i_{s1} = \sum_{n=1,5,7,11,13} \hat{I}_n \sin(n\omega t) \quad (3.54)$$

$$i_{s2} = \sum_{n=1,5,7,11,13} \hat{I}_n \sin(n(\omega t + \delta)) \quad (3.55)$$

\hat{I}_n is the peak of the n^{th} order harmonic current and δ is the phase shift angle.

In referring i_{s1} to the primary, the harmonic currents remain unchanged, and to refer i_{s2} , the phase angles of the harmonic currents must be introduced where ($\angle i'_{s2} = \angle i_s - \delta$ for $n = 1, 7, 13, \dots$ and $\angle i'_{s2} = \angle i_s + \delta$ for $n = 5, 11, 17, \dots$). i'_{s1} and i'_{s2} can expressed as follows [47]:

$$i'_{s1} = \hat{I}_1 \sin \omega t + \hat{I}_5 \sin 5\omega t + \hat{I}_7 \sin 7\omega t + \hat{I}_{11} \sin 11\omega t + \hat{I}_{13} \sin 13\omega t + \dots \quad (3.56)$$

$$i'_{s2} = \sum_{n=1,7,13,\dots}^{\infty} \hat{I}_n \sin(n(\omega t + \delta) - \delta) + \sum_{n=5,11,17,\dots}^{\infty} \hat{I}_n \sin(n(\omega t + \delta) + \delta) \quad (3.57)$$

For $\delta = 30^\circ$ equation (3.57) can be rewritten as:

$$i'_{a2} = \hat{I}_1 \sin \omega t - \hat{I}_5 \sin 5\omega t - \hat{I}_7 \sin 7\omega t + \hat{I}_{11} \sin 11\omega t + \hat{I}_{13} \sin 13\omega t - \dots \quad (3.58)$$

Then by substituting equations (3.56) and (3.58), the transformer primary harmonic current will be:

$$i_a = 2(\hat{I}_1 \sin \omega t + \hat{I}_{11} \sin 11\omega t + \hat{I}_{13} \sin 13\omega t + \hat{I}_{23} \sin 13\omega t + \dots) \quad (3.59)$$

From equation (3.59) the 5th, 7th, 17th, and 19th harmonic current components are cancelled from the primary current.

iii Filter capacitor

The dual-bridge CSR equivalent circuit for resonant mode is show in Figure 3.18. The converter admittance can be written in terms of filter capacitance and transformer inductances [8, 49, 50]:

$$Y_s = SC_r + \frac{1}{SL_r + \frac{1}{\frac{1}{SL_s} + \frac{SC_r}{S^2L_rC_r + 1}}} \quad (3.60)$$

The parallel resonant frequency can be calculated from the zeros of the $Y(s)$ admittance:

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \quad (3.61)$$

$$\omega_2 = \frac{1}{\sqrt{(2L_s + L_r)C_r}} \quad (3.62)$$

ω_1 depends on the transformer secondary leakage inductance. Since SHE eliminates the 11th and 13th only and the transformer secondary current contains the 5th, 7th, 15th and 17th, resonance may occur in the converter input current (i_{r1} or i_{r2}). So it is best to position the first resonant frequency between 11 to 13 pu. The position of the second resonant frequency will be shown in the simulation section.

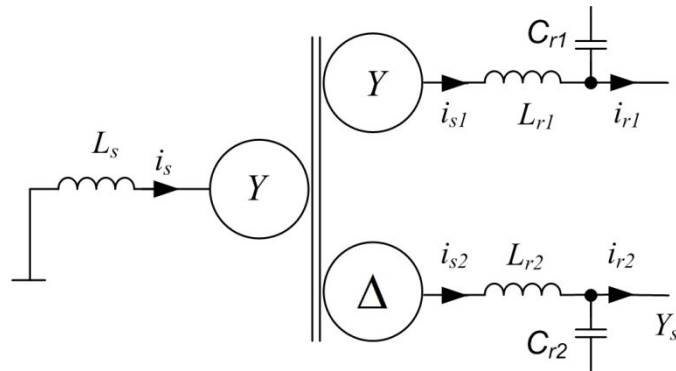


Figure 3.18 Dual-bridge CSR resonant mode equivalent circuit.

iv Control strategy

The dual-bridge CSR is required to provide a reliable dc output voltage with high power factor sinusoidal input current. In the proposed dual-bridge CSR controller, the input primary winding current is controlled. This will reduce the number of current sensors and decrease costs and controller complexity. Figure 3.19 shows the proposed controller of the dual-bridge CSR, which is similar to the controller proposed in Figure 3.14 for the CSR, but the lower converter (connected to the Δ

transformer winding) receives the angle $\alpha + \omega t$ plus a phase shift of 30° to compensate the magnetic phase shift introduced by the transformer winding.

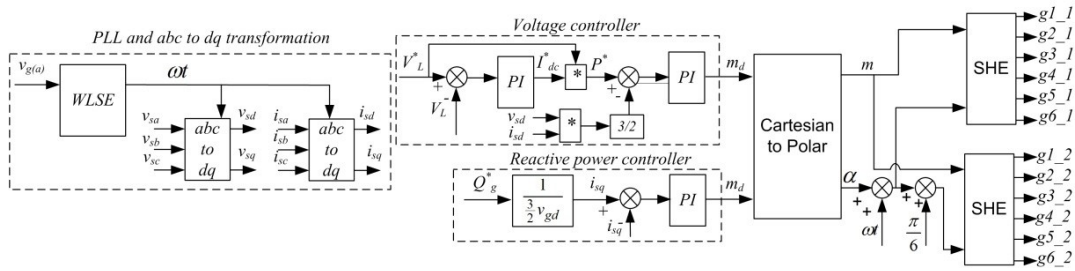


Figure 3.19 Dual-bridge CSR controller.

v Simulation results

The dual-bridge CSR controller performance is tested according to the following sequence. Initially, the reference dc load voltage V_L^* is 3kV (case 1); and at $t=3s$, the reference dc load voltage V_L^* is increased from 3kV to 6kV (case 2); and at $t=6s$, a load increase is applied by connecting a shunt resistor of 14.2Ω to the existing load resistance (case 3). During all three cases, the reference reactive power is zero. This operation sequence is chosen to examine the dynamic performance of the dual-bridge CSR previously discussed.

In this simulation, the transformer secondary leakage inductance is 0.1pu and the transformer primary side inductance plus the supply inductance is 0.15pu. According to equation(3.61), the capacitance varies from 0.06 to 0.083pu. From equation(3.62), the second resonance frequency mode will vary from 5.5 to 6.5pu. The second resonance will not excite because the lowest harmonic in the primary current is the 23rd. The transformer leakage inductances and core losses are the same pu values in the PSCAD/EMTDC library and are representative of a standard device[51].

Figure 3.20 and Figure 3.21 show the PSCAD/EMTDC model simulation results and the system parameters are given in Table 3.6. Figure 3.20 shows that the proposed controller successfully tracks the reference load voltage signal with minimal transient time. The results in Figure 3.21 show the performance of the controller during the step increase in the load. From Figure 3.21(a), the grid current in both cases was sinusoidal and in-phase with the supply voltage. Also the proposed controller successfully provides fast response and recovery from the step load increase in less

than one cycle. Figure 3.21(b) shows the dc-link current increases smoothly to compensate the load increase.

The results in Figure 3.20 and Figure 3.21 confirm that the dual-bridge CSR with the phase-shift transformer is able to provide a secure dc voltage to the load with good dynamic performance, controlled reactive power, high quality sinusoidal current and minimum switching frequency per CSR bridge -350Hz. This qualifies the proposed dual-bridge CRS for operation in high-power medium-voltage application.

Table 3.6 Dual-bridge CSR system parameters.

Parameter	Value
Grid voltage	3.3kV
Grid frequency	50Hz
Phase-shift transformer rated voltage	3.3kV
Phase-shift transformer rated power	5.1MW
Phase-shift transformer core losses	0.01puOr 51kW
ac-side capacitance $C_{r(1)}$ and $C_{r(2)}$	60 μ f Δ connection
dc side inductance L_{dc}	0.01H
dc-side Capacitance C_{dc}	75 μ F
Load resistance	14.2 Ω
step load resistance	14.2 Ω

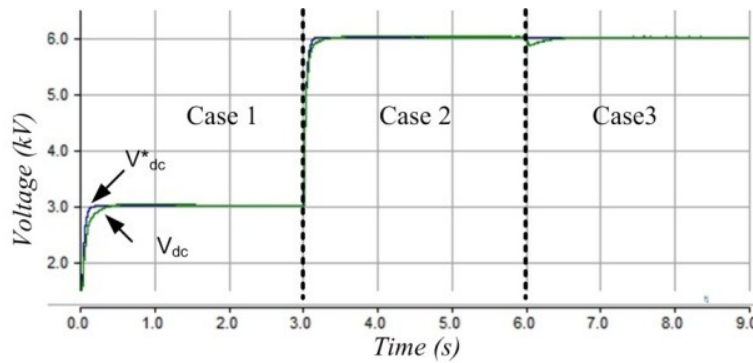
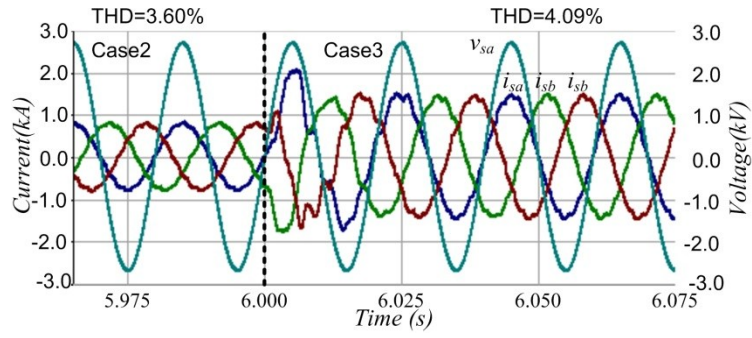
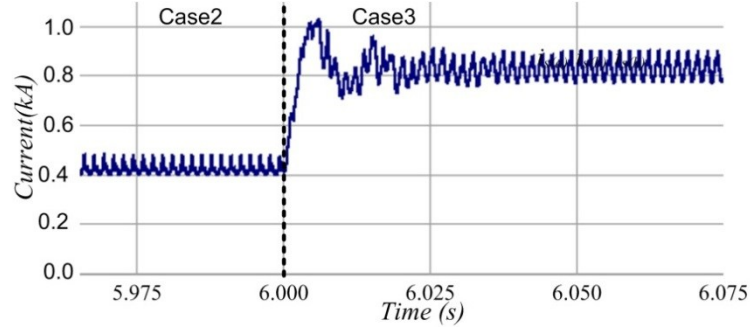


Figure 3.20 Waveforms of the overall performance of the dual-bridge CSR.



(a) the three-phase grid current and phase 'a' grid voltage during case 2 and 3.



(b) dc-link inductance current during step change on the load

Figure 3.21 Details of the dual-bridge CSR current during a load resistance step change.

3.4.2 Dual-bridge CSI

Figure 3.22 show the proposed dual-bridge CSI, which consists of two CSI connected in series, from a three winding phase-shift transformer.

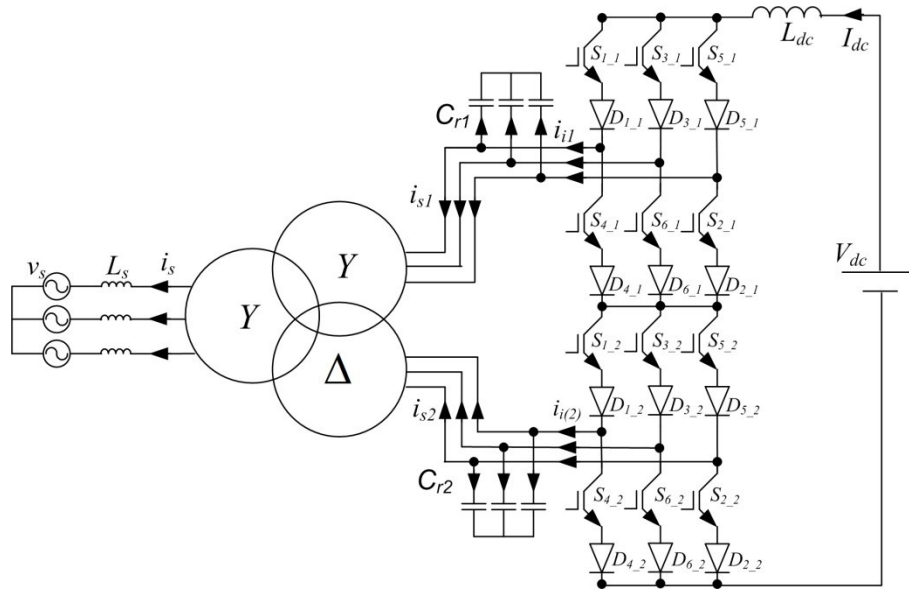


Figure 3.22 Dual-bridge CSI.

i Control strategy

The dual-bridge CSI controller is shown in Figure 3.23, and is similar to the grid connected CSI controller shown in Figure 3.8. Here the estimated m_d and m_q are converted from Cartesian to Polar to derive the modulation index m for the SHE gate signal generator, and the angle α which is added to angle ωt . A 30° phase shift is added to the lower CSI bridge to compensate the magnetic phase shift introduced by the transformer Δ winding, as discussed in the dual-bridge CSR case.

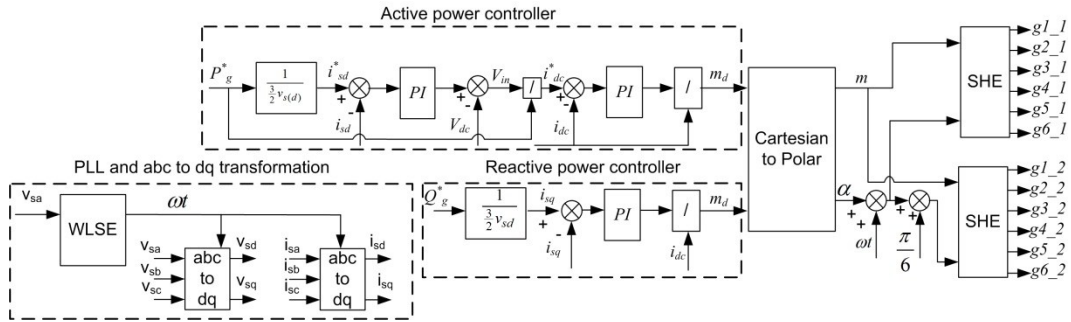


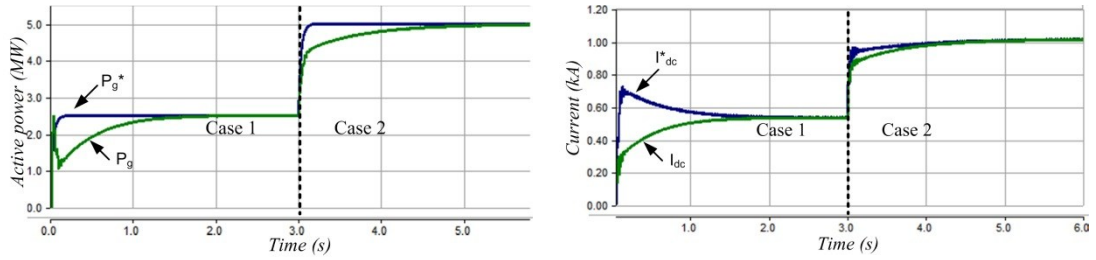
Figure 3.23 Dual-bridge CSI controller.

ii Simulation results

This section shows the performance of the proposed dual-bridge CSI in Figure 3.23 and its controller shown in Figure 3.23. The operation sequence as follows: in the beginning, the reference active delivered power P_g^* was set to 2.5MW, at $t=3s$, it is increased to 5.0MW. Figure 3.24 and Figure 3.25 show the simulation results. Figure 3.24(a) shows that the proposal controller succeeds in tracking the reference active power with minimum oscillation. Figure 3.24(b) shows that the dc-link current regulator succeeds in tracking its reference with minimum transient time. Figure 3.25(a) shows the three-phase grid current and phase voltage ‘a’ during the step increase in the reference active power delivered into grid. It is clear that the grid current increases gradually and smoothly to compensate the increase of the reference active power, with high quality sinusoidal current with low THD and high power factor. Figure 3.25(b) shows in detail the dc-link current during the step increase in the reference active delivered power, it can be observed that the dc-link current increase smoothly to compensate the step increase in the delivered power.

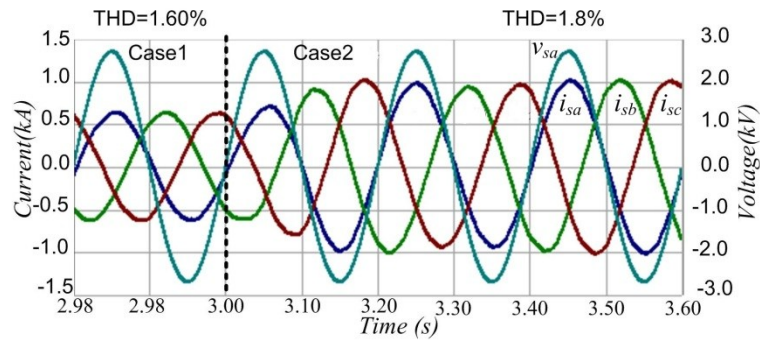
Table 3.7 Dual-bridge CSI system parameters.

Parameter	Value
Grid voltage	3.3kV
Grid frequency	50Hz
Phase-shift transformer rated voltage	3.3kV
Phase-shift transformer rated power	5.1MW
Phase-shift transformer core losses	0.01pu or 51kW
ac-side capacitance $C_{i(1)}$ and $C_{i(2)}$	60 μ F Δ connection
dc side inductance L_{dc}	0.01H
dc voltage source	6kV

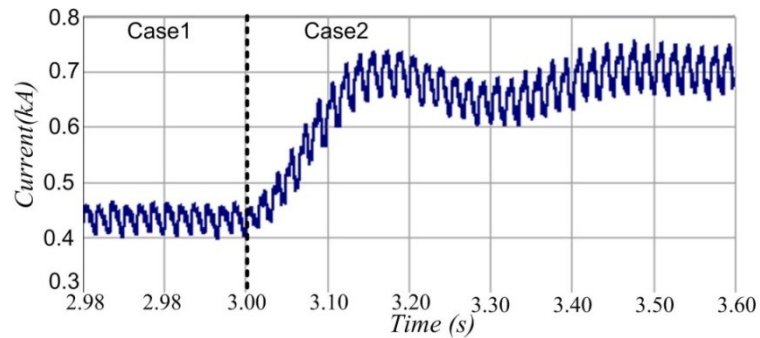


(a) Grid reference active delivered power P_g^* and grid delivered power P_g . (b) Reference dc-link current I_{dc}^* and dc-link current.

Figure 3.24 Waveforms showing the performance of the proposed dual-bridge CSI.



(a) Phase voltage 'a' and the three-phase grid current during the step change from case1 to case 2.



(b) dc-link current during the step change from case1 to case 2.

Figure 3.25 Detail view of grid voltage and current and the dc-link current of the proposed dual-bridge CSI.

An additional simulation was performed to show the performance of the reactive power controller, where $P_g^* = 2.5\text{MW}$ is maintained fixed, and Q_g^* is varied from 1MVAR to 0 at $t=3\text{s}$ and then to -1MVAR at $t=6\text{s}$. Figure 3.26 and Figure 3.27 show the simulation results. Figure 3.26(a) shows that the proposed controller delivers constant active power to the grid, only a small change occurs during the step changes to the reactive power controller reference signal where the active power controller responds fast to compensate this change. In Figure 3.27(b), the proposed controller tracks Q_g^* . Figure 3.26(c) shows the dc-link current, which does not change since the reference active delivered power is kept constant. Figure 3.27(a) to (c) show phase 'a' grid voltage and current, where the grid current in each case is leading, in-phase, and lagging, respectively.

The simulation results in Figure 3.24 to Figure 3.27 qualify the proposed dual-bridge CSI for high-power medium-voltage application and shows its ability to control the grid active and reactive powers independently.

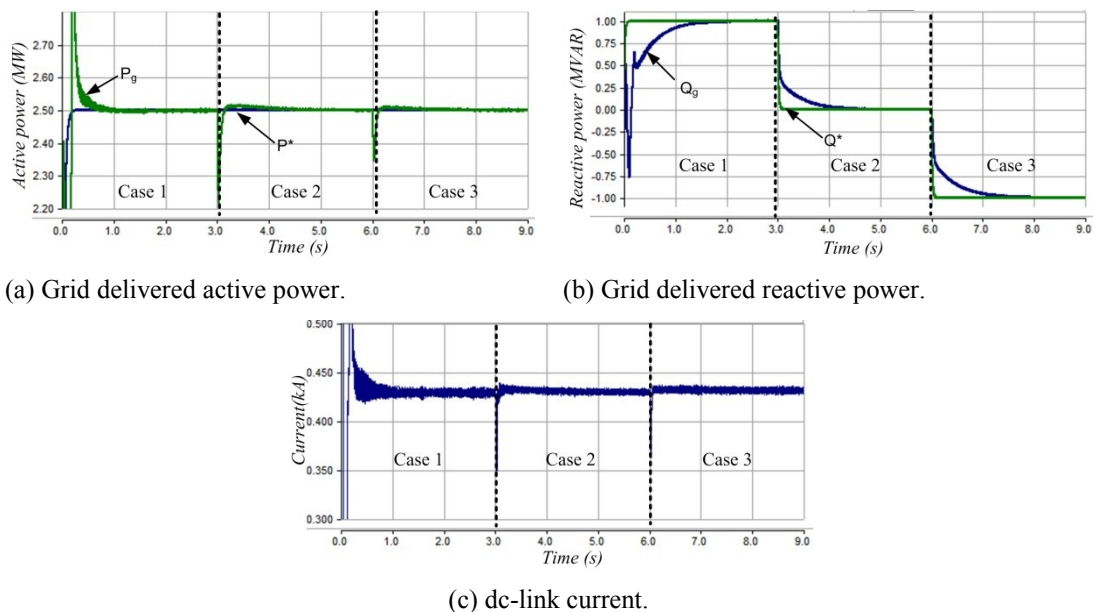


Figure 3.26 Waveforms show the performance of the dual-bridge reactive power controller.

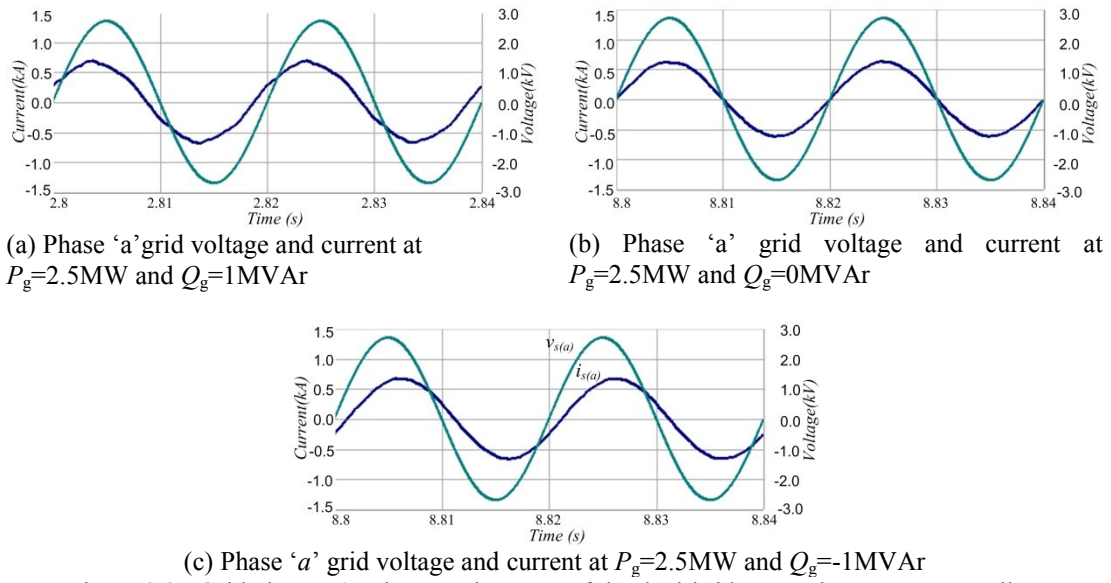


Figure 3.27 Grid phase 'a' voltage and current of the dual-bridge reactive power controller.

3.5 Summary

This chapter presented the analysis for the CSI in island mode, grid connected CSI and CSR, dual-bridge CSR, and dual-bridge CSI. A conventional proportional integral controller is used since the system modelling is in dq reference frames. For the CSI in island mode, the simulation results show that the proposed controller is able to quickly regulate the load voltage even during a load step change. Several switching techniques, for the CSI in island mode, were compared 1) mapped sinusoidal PWM, 2) SVM and 3) SHE. The comparison shows that SVM is the best modulation technique. A controller for a grid connected CSI is proposed and the simulation results show good dynamic performance, with the ability to independently regulate the grid active and reactive powers, with high quality sinusoidal grid current. The proposed CSR controller also showed good performance on regulating the load voltage even during step change on the reference output voltage and a step change in the load. Additionally the controller takes sinusoidal grid current at near unity power factor. For medium-voltage and multi-megawatt applications, the dual-bridge CSR and CSI are proposed, because of the feature of harmonics cancelation due the phase-shift transformer and SHE is used to eliminate the 11th and 13th harmonic orders with low switching frequency of 350Hz. The proposed controller provides the basic requirements such as independent control of active and reactive

powers, and low total harmonic distortion THD current with a low switching frequency.

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Chapter 4. Proposed ac-dc Buck-Boost Converters

This chapter describes the operating principles of the proposed ac-dc buck-boost converters (single-phase, three-phase, and multi-phase), and highlights their distinct attractive features, such as: buck-boost capability in a single-stage with a single switch; reduced power circuit components; stable dc voltage output; soft transient from the buck to the boost mode without different operating regimes; and sinusoidal input current with near unity power factor. The single-phase buck-boost converter is suitable for grid interfacing of small-scale renewable ac sources because it has no requirement for a pre-charging circuit for the dc side capacitor, and it has a simple linear controller. The three-phase and the dual three-phase buck-boost converters are suitable for medium-voltage and high-power applications where the switching frequency is less than 1.5kHz, with sinusoidal input current and near unity power factor at rated load. The limitation of the three-phase and the dual three-phase buck-boost converters is that the switching devices are exposed to a high voltage beyond that which can be tolerated by a single device. In the three-series connected single-phase buck-boost converters, the dc output terminals are series connected to generate high voltage. By using this approach, voltage stresses on the switching devices are greatly reduced. Simulation and experimental results will establish that the proposed converters have good dynamic performance in buck and boost modes, with near unity input power factor.

4.1. Review of ac-dc converters with reduced switch count

The uncontrolled diode bridge rectifier provides the easiest way to get a dc voltage from an ac supply. It consists of four diodes and a dc-side filter capacitor to reduce the dc voltage ripple, but injects high harmonic current into the ac grid line current. Much research has been carried out to improve the supply current quality, the power factor, and to provide adjustable output dc voltage by adding a dc-dc converter after the diode bridge rectifier [1-5].

This section summarises some of the research into ac-dc converters that reduces the number of power electronic switches.

4.1.1 Single-phase ac-dc converters with reduced switch count

Single-phase ac-dc converters with power factor correction (PFC) can be classified into two categories: single-stage and two-stage converters. Most single-stage ac-dc converters with PFC employ an H-bridge rectifier followed by a boost converter. The output dc voltage is therefore greater than or equal to the peak of the ac supply voltage [6-14]. Power factor correction is achieved by regulating the input inductor current of the boost stage. Several single-phase single-stage ac-dc buck converters have been proposed for electrical vehicle battery charging [6, 15, 16]. The authors in [17-20] proposed a two-stage ac-dc buck-boost converter that offers input PFC capability. This buck-boost converter requires independent control of the boost and buck stages, and suffers from control difficulties during buck - boost modes transitions. Additionally, it requires a large number of semiconductor devices and passive elements [21].

The single-phase buck-boost converter shown in Figure 4.1(a) was initially proposed in [22], where nonlinear control is used to regulate the output dc voltage and provide power factor correction. Although the circuit is simple, the controller requires five feedback signals, which increase the overall complexity of the implementation, and potentially cost. The performance is demonstrated in a buck mode only using simulation, with experimental substantiation. Reference [23] shows another nonlinear control study on the same circuit, with the authors proposing two control methods. The first control method regulates current in the dc-side inductor I_L instead of output dc voltage V_{dc} and it requires an additional stage to adjust the dc output voltage. The second control method regulates the dc output voltage V_{dc} directly in a single stage. However, both control methods use an extremely high switching frequency of 100kHz, but the supply current THD remains above that specified in many grid codes and standards (7.47% and 19.81% respectively). Also there are no experimental results and the simulation results are only in the buck mode. The bridgeless buck-boost converter proposed in [24] is similar to the proposed buck-boost converter show in Figure 4.1(a), except the two diodes in the bridge rectifier are replace with two power electronics withes and a freewheel diode is added to give a path for the inductance current during the discharging mode.

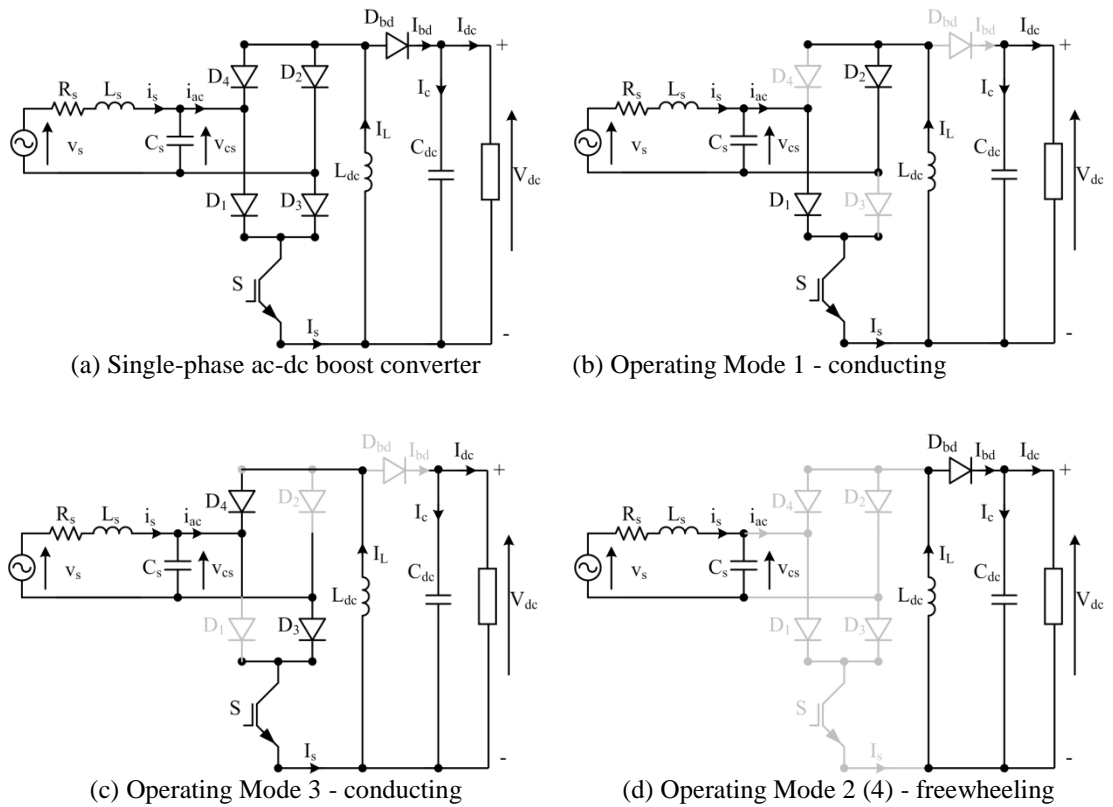


Figure 4.1 Schematic of the proposed single-phase ac-dc buck-boost converter and its 4 operating modes.

4.1.2 Three-phase ac-dc converters with reduced switch count

Three-phase ac-dc converters can be classified into three main categories: buck, boost, and buck-boost converters.

The buck converters shown in [25-27] have a reduced number of power electronic switches, three, but the number of diodes is increased and the converters require a special firing technique. The single switch buck type converter, which basically consists of a three-phase diode bridge rectifier and a buck converter, with an L-C filter in the ac side, is presented [28, 29]. The power electronic switch in the buck converter is switched at 19kHz to 87.5kHz. This high switching frequency forces the converter input current to track the input voltage waveform. Although the converter is simple, the voltage stress on the buck switch is high. In [30], the authors use two buck switches to solve this voltage issue. A similar configuration in [31] is used in a wind energy conversion system (WECS), where the converter consists of a diode rectifier, a buck converter, and a current source inverter. In [32], three independent Cuk converter modules are connected between each supply phase and the neural,

with each module performing PFC. This converter has a fast dynamic performance and high power factor.

The three-phase ac-dc boost converter in [33, 34] uses a single switch with a switching frequency greater than 20kHz. This high switching frequency allows the input current to follow the supply voltage shape, and the input filter is only needed to remove the high-frequency components from the supply current. This converter was proposed as a WECS active front end converter in [35-40], to provide a stable dc voltage for a grid-connected inverter, over the wide speed range of a synchronous generator. A multiple parallel boost unit is proposed in [41] to increase the WECS power level and decrease the current stress on the power electronic switches. The main disadvantages of these back-to-back converters are the need to pre-charge the dc-side capacitor, poor output short-circuit protection in the boost converter case, and the limitation of output power to a few kilowatts imposed by the boost converter switching frequency. The converters in [42, 43] use three single-phase ac-dc modules, where each module is connected between the phase-voltage and neutral. The main drawback of using an independent module on each phase is that operation synchronization of each module and three separate converters increase the cost.

The single-stage buck-boost converter proposed in [44] uses a buck-boost converter after a diode rectifier and L-C ac side filter. It operates at high frequency with discontinuous phase current in the ac-side C-filter, which results in naturally sinusoidal input currents. The main drawback is high voltage stress across the buck-boost switch. References [45-47] present a single-stage buck-boost converter that also operates in a discontinuous conduction mode (DCM) at a high frequency, and it uses two switches and two diodes in the dc-side, unlike that discussed in [44]. Also the configuration requires a complicated firing technique and a high speed digital signal processor (DSP), since in each sample period during the buck mode, there are six modes of operation. During the boost mode, there are seven modes of operation. In addition, the voltage stress on the switches remains high. In [48], the buck-boost converter configuration in [45-47] is modified by adding a pair of LC resonant components to each switch, to make the switches turn off with zero current (zero current switching, ZCS). But adding resonant circuits increases system complexity

and cost; in addition to a increased peak reverse blocking voltage across the switch during the off-state.

The three-phase version of the buck-boost converter shown in Figure 4.1(a) was discarded in [49, 50] on the grounds that it could not be extended to a three-phase system, due to the discontinuous and non-sinusoidal input current. While in [51, 52] the three-phase buck-boost converter considered is shown in Figure 4.9(a). It operates in a discontinuous mode using multi-resonance zero current switching, but this approach is not suitable for high-power applications since a 25kHz switching frequency is used.

4.1.3 Multi-phase ac-dc converters with reduced switch count

Multi-phase ac-dc converters with a reduced switch count are frequently used in high-power medium-voltage applications. The three-phase uncontrolled diode rectifier causes high current harmonics at the input (grid line current). These harmonic currents can be reduced by using phase-shift transformers at the ac input side. The secondary windings are designed so that the harmonics generated by one group of diode rectifiers are cancelled by those generated by the other group of diode rectifiers. In [1, 53-57], the authors use an uncontrolled three-phase diode rectifier and a multi secondary winding transformer to achieve harmonic cancellation at the input, and to provide low ripple dc supply voltage with sinusoidal, high quality and low THD, ac grid current.

The conventional WECS which uses a three-phase PMSG, with a front end converter consisting of a six pulse uncontrolled diode rectifier followed by a boost converter, and the proposed WECS which uses a six-phase PMSG and front end converter consisting of a twelve pulse uncontrolled diode rectifier followed by a boost converter, are compared in [58, 59]. The simulation and experimentation show that the dc-side current ripple and pulsating torque are less than the conventional WECS case by 60-70%. The efficiency is higher by 3%, and the boost converter inductance is smaller which tends to reduce the initial system cost. In [60] the authors use the same front end converter but the six-phase PMSG is replaced with a three-phase PMSG followed by a phase-shift transformer. In [61] a three-phase PMSG is followed by a three-phase to nine-phase isolation transformer, where each

transformer secondary winding is connected to a six pulse uncontrolled diode rectifier followed by a boost converter. Switches are added at the input and output of the boost converters to parallel and series connect the inputs and outputs respectively. By adjusting these power electronic switches, the WECS can operate in three different modes: 1 - series mode for low generator speeds, 2 - hybrid mode at medium generator speeds, and 3 - parallel mode at high generator speeds. Using the multi-phase transformer and 18-pulse rectifier improves the stator current and reduces the torque ripple, and the power level of each boost converter is reduced.

4.2. Single-phase buck-boost converter

Figure 4.1(a) shows the single-stage ac-dc buck boost converter circuit in [62], where the authors investigated this converter under discontinuous conduction of the dc-side inductor. The authors only exploit the buck mode of this converter, with power factor correction. No information is given about the input current waveform shape, modes of operation or circuit analysis.

The basic converter topology in Figure 4.1(a) includes three main parts: LC filter, diode rectifier and buck-boost chopper. The diode rectifier bridge is reversed so that the buck-boost converter gives a positive output voltage. Operating Mode 1 is where switch S is turned on during the positive half-cycle of the supply v_s , shown in Figure 4.1(b). In this mode, supply v_s energises the dc inductor L_{dc} through switch S and diodes D_1 and D_2 , while capacitor C_{dc} acts as an energy tank that supplies the load. Operating Mode 2, shown in Figure 4.1(d), is the freewheeling period, when switch S is off during the positive half-cycle of the supply v_s . The energy stored in L_{dc} during Mode 1 is used to supply the load and to recharge capacitor C_{dc} . For correct converter operation, dc capacitance C_{dc} and dc inductance L_{dc} must be sized to prevent discontinuity in the load and inductor currents. Operating Mode 3, shown in Figure 4.1(c), is when switch S is turned on during the negative half-cycle of the supply v_s . Inductor L_{dc} is re-energised through switch S and diodes D_3 and D_4 , whilst the energy stored in dc capacitor C_{dc} supplies the load. Modes 1 and 3 use the same switching device to modulate the ac source, and have the same effect on the state of charge of the dc-side elements L_{dc} and C_{dc} . Operating Mode 4 is when switch S is

turned off during the negative half-cycle of the supply v_s . Modes 2 and 4 are identical.

Differential equations (4.1) and (4.2) describe circuit operation during modes 1 and 3, whilst (4.3) and (4.4) describe circuit operation during modes 2 and 4.

$$\frac{dI_L}{dt} = -\frac{v_{cs}}{L_{dc}} \quad (4.1)$$

$$\frac{dV_{dc}}{dt} = -\frac{I_{dc}}{C_{dc}} \quad (4.2)$$

$$\frac{dI_L}{dt} = \frac{V_{dc}}{L_{dc}} \quad (4.3)$$

$$\frac{dV_{dc}}{dt} = \frac{I_L - I_{dc}}{C_{dc}} \quad (4.4)$$

The negative sign in (4.1) and (4.2) appear because the bridge rectifier is reversed.

Neglecting any resistive voltage drop, the voltage across ac source capacitor C_s is given by (4.5).

$$v_{cs} = v_s - L_s \frac{di_s}{dt} \quad (4.5)$$

The mathematical relationships describing steady-state operation are obtained using inductor zero average volt-second and capacitor voltage balance principles [63]. The voltage across dc-side inductor L_{dc} is illustrated in Figure 4.2(a). For simplicity, assume that the ac source leakage inductance L_s is sufficiently small so that v_{cs} can be considered equal to v_s without significant loss of accuracy, and the convert operate at constant duty cycle. See Figure 4.1(a). Figure 4.2(b) shows dc-side inductor current and dc-side capacitor voltage, from which the voltage across the dc-side inductor within each switching period T_s during operating modes 1 and 2 can be expressed by $v_L = -\delta v_{cs}$ and $v_L = (1-\delta)V_{dc}$ respectively, where $\delta = t_{on}/T_s$ and t_{on} is the dwell time of the switch within each switching cycle. Based on the inductor zero average volt-second principle [63], the average voltage across L_{dc} is calculated and is zero as in (4.6).

$$\bar{V}_{L_{dc}} = \frac{1}{\pi} \int_0^{\pi} [-\delta v_s + (1-\delta)V_{dc}] d\omega t = 0 \quad (4.6)$$

Where δ is the duty cycle of switch S . Assuming a sinusoidal source voltage defined by $v_s=V_m\sin\omega t$, where V_m is the peak phase voltage, ω is the supply angular frequency, and t is time, and that the average output dc voltage is defined by

$$\bar{V}_{dc} = \frac{1}{\pi} \int_0^{\pi} V_{dc} d\omega t, \text{ then equation (4.6) reduces to}$$

$$\bar{V}_{dc} = \frac{\delta}{1-\delta} \times \frac{2V_m}{\pi} \quad (4.7)$$

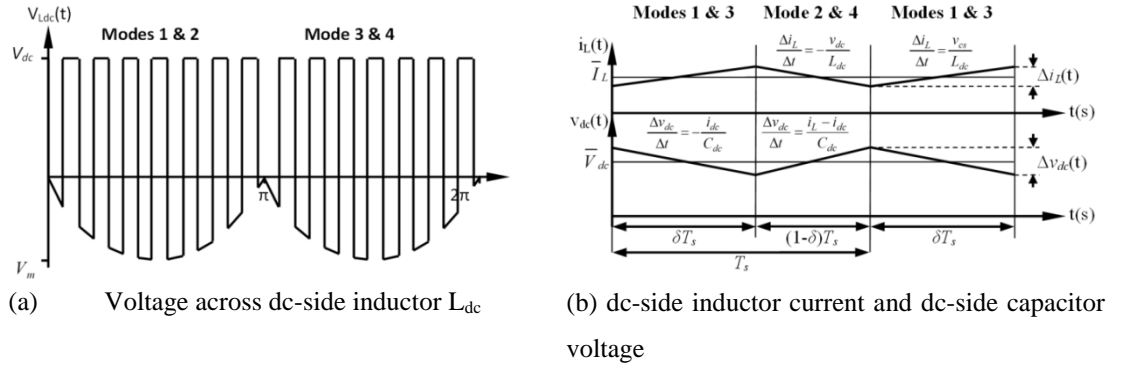


Figure 4.2 Waveforms for the proposed single-phase ac-dc buck-boost converter. [V_m is the peak of supply voltage v_s]

Since capacitor voltage balance [63] necessitates the average capacitor current \bar{I}_c over one or a number of consecutive switching cycles to be zero, the relationship between the average inductor current \bar{I}_L and load average current \bar{I}_{dc} is

$$\bar{I}_c = \frac{1}{\pi} \int_0^{\pi} [-\delta \bar{I}_{dc} + (1-\delta)(\bar{I}_L - \bar{I}_{dc})] d\omega t = 0 \quad (4.8)$$

In (4.8), the capacitor current in operating modes 1 and 3, and in modes 2 and 4 is expressed as $\bar{I}_c = -\delta \bar{I}_{dc}$ and $\bar{I}_c = (1-\delta)(\bar{I}_L - \bar{I}_{dc})$ respectively.

Equation (4.8) can be reduced to

$$\frac{1}{\pi} \int_0^{\pi} \bar{I}_{dc} d\omega t = \frac{(1-\delta)}{\pi} \int_0^{\pi} \bar{I}_L d\omega t \quad (4.9)$$

Equation (4.9) implies

$$\bar{I}_{dc} = (1 - \delta)\bar{I}_L \quad (4.10)$$

In practice, the average inductor current is maintained virtually constant, thus the dc output or load current \bar{I}_{dc} remains constant and proportional to the inductor average current, as given by (4.10). This feature can be exploited to reduce the voltage stresses on the switching devices of current source inverters and maintain a constant average input dc current when the proposed buck-boost converter is used as an active front end. For a resistive load the dc output voltage can be expressed in term of the average inductor current, as shown in (4.11).

$$V_{dc} = (1 - \delta)R_{dc}\bar{I}_L \quad (4.11)$$

L_{dc} and C_{dc} are selected based on the maximum permissible inductor current ripple and output voltage ripple, ΔI_{dc} and ΔV_{dc} respectively. Therefore, from equations (4.1) to (4.4) and Figure 4.2(b), equations (4.12) and (4.13) are obtained.

$$L_{dc} = \frac{(1 - \delta)T_s \times V_{dc}}{\Delta I_L} \quad (4.12)$$

$$C_{dc} = \frac{\delta T_s \times \bar{V}_{dc}}{\Delta V_{dc} \times R_{dc}} \quad (4.13)$$

4.2.1 Control Stage

The purpose of the controller is to force the ac line current to be sinusoidal and in phase with the input source voltage, and to control the average output dc voltage in both buck and boost operating modes.

i. Current control

The required control system structure, for sinusoidal input current at any power factor, is derived accounting for the ac fundamental frequency and dc-side dynamics. Since the output dc voltage V_{dc} is dependent on the magnitude of the voltage v_{cs}

across the input filter capacitor, differential equation (4.14) can be used as the basis for current controller design.

$$\frac{di_s}{dt} = -\frac{R_s}{L_s}i_s + \frac{(v_s - v_{cs})}{L_s} \quad (4.14)$$

The voltage v_{cs} required to force input current i_s to follow its control reference i_s^* is unknown, but can be obtained using a PI controller by setting

$$w = v_s - v_{cs} = k_p(i_s^* - i_s) + k_i \int (i_s^* - i_s) dt \quad (4.15)$$

$$\psi = k_i \int (i_s^* - i_s) dt \quad (4.16)$$

The current controller transfer function is obtained by substituting (4.16) into (4.15), and then substituting the result for $v_s - v_{cs}$ into (4.14).

$$\frac{di_s}{dt} = -\frac{(R_s + k_p)}{L_s}i_s + \frac{\psi}{L_s} + \frac{k_p i_s^*}{L_s} \quad (4.17)$$

After Laplace manipulation of (4.17) and (4.16), the transfer function is defined as

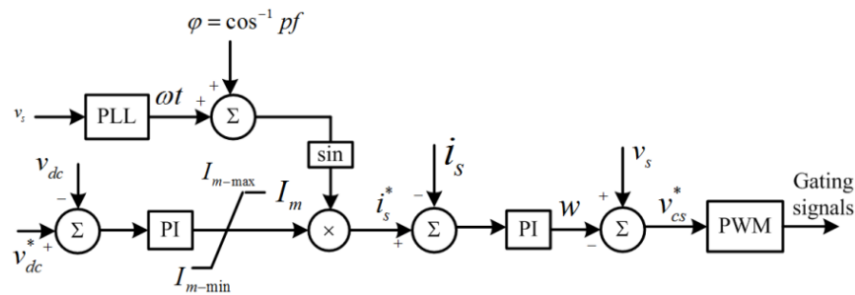
$$\frac{I_s(s)}{I_s^*(s)} = \frac{\frac{k_p}{L_s}s + \frac{k_i}{L_s}}{s^2 + \frac{R_s + k_p}{L_s}s + \frac{k_i}{L_s}} \quad (4.18)$$

From (4.15), v_{cs} can be obtained as

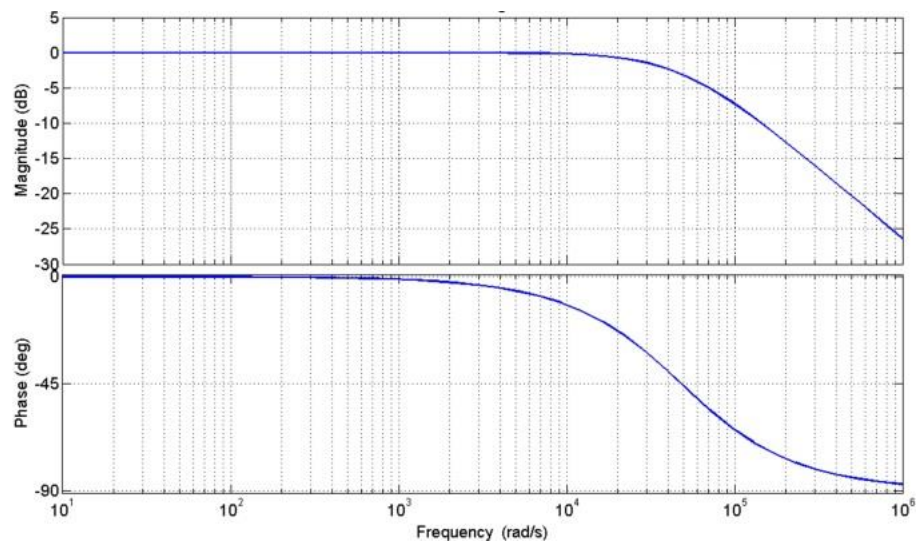
$$v_{cs} = v_s - w \quad (4.19)$$

w represents the PI controller output that regulates the converter input current, and v_s is the supply voltage that is incorporated as feed-forward control to improve the dynamic response and for controlled start-up. The block diagram of the two proposed control loops shown in Figure 4.3(a) is derived based on equations (4.15) and (4.19). The supply current can be controlled to be sinusoidal and to achieve any power factor ϕ , where $|\phi| \leq \frac{1}{2}\pi$, provided the controller for (4.18) has sufficient bandwidth so as not to introduce distortion in the normalized version of the fundamental voltage component used as a reference to the converter modulator. The gains for the inner current controller are obtained by comparing the denominator of the equation (4.18)

with a standard 2nd order system $s^2 + 2\xi\omega_n s + \omega_n^2$, where ξ and ω_n represent the damping factor and natural frequency. The natural frequency can be decided using settling time or maximum over-shoot. However, settling is preferred ($T_s \approx 4/\xi\omega_n$). Alternatively, simple pole placement can be used, where the denominator of equation (4.18) is equated to $(s+p_1)(s+p_2)$. The controller gains are finely tuned to ensure sufficient bandwidth as shown in Figure 4.3(b), to reproduce the fundamental current without any phase shift. With the selected gains of $k_p=120\text{V/A}$ and $k_i=2000\text{VA}^{-1}\text{s}^{-1}$, the closed loop poles are located at -4642 and -17.



(a) Block diagram of the proposed two control loops.



(b) Bode plots, where $k_p=120$ and $k_i=2000$

Figure 4.3 Two control loops structure and frequency response.

ii. Voltage Control

Equation (4.4) describes the converter dc-side dynamics and provides a basis for the dc voltage controller. Assuming a resistive load and substituting for \bar{I}_{dc} , results in (4.20).

$$\frac{dV_{dc}}{dt} = -\frac{\bar{V}_{dc}}{R_{dc}C_{dc}} + \frac{\bar{I}_{dc}}{C_{dc}} \quad (4.20)$$

Where \bar{V}_{dc} is the average dc link voltage, and \bar{I}_i is the average current entering the dc link node which is equal to the instantaneous dc inductor current I_L during modes 2 and 4 only. Assuming lossless conversion, power balance dictates that $P_{ac}=P_{dc}$. Therefore

$$\bar{V}_{dc}\bar{I}_i = \frac{1}{2}v_{cm}i_m \cos\phi \quad (4.21)$$

Where v_{cm} is the peak voltage across the ac side input capacitor and i_m is the peak fundamental current. Using (4.7), this can be rewritten as (4.22) from which \bar{I}_i can be obtained.

$$\bar{I}_i = \frac{1}{2} \frac{v_{cm}}{V_{dc}} \cos\phi \times i_m = \frac{\pi}{4} \frac{(1-\delta)}{\delta} \cos\phi \times i_m \quad (4.22)$$

Equation (4.22) highlights that the relationship between peak fundamental current i_m and \bar{I}_i depends upon quantities such as duty cycle, which may vary according to operating conditions. Substituting (4.22) into (4.20) gives equation (4.23).

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_{dc}C_{dc}} + A \frac{i_m}{C_{dc}} \quad (4.23)$$

Where $A = \frac{1}{4}\pi \frac{(1-\delta)}{\delta} \cos\phi$

The peak fundamental current i_m required to maintain the dc link voltage at any desired level can be estimated using PI control. Assuming that the controller gain terms also perform the necessary scaling for A in (4.23), i_m is expressed as

$$i_m = k_{pdc}(V_{dc}^* - V_{dc}) + k_{idc} \int (V_{dc}^* - V_{dc}) dt \quad (4.24)$$

$$\lambda = k_{idc} \int (V_{dc}^* - V_{dc}) dt \quad (4.25)$$

The voltage controller transfer function is obtained by substituting (4.24) into (23), resulting in (26), whilst the derivative of λ is expressed in (4.27)

$$\frac{dV_{dc}}{dt} = - \left[\frac{1}{R_{dc}C_{dc}} + \frac{k_{pdc}}{C_{dc}} \right] V_{dc} + \frac{\lambda}{C_{dc}} + \frac{k_{pdc}}{C_{dc}} V_{dc}^* \quad (4.26)$$

$$\frac{d\lambda}{dt} = -k_{idc}V_{dc} + k_{idc}V_{dc}^* \quad (4.27)$$

Taking Laplace transforms of (4.26) and (4.27), and following manipulation, results in (4.28).

$$\frac{V_{dc}(s)}{V_{dc}^*(s)} = \frac{\frac{k_{pdc}}{C_{dc}}s + \frac{k_{idc}}{C_{dc}}}{s^2 + \left[\frac{1}{R_{dc}C_{dc}} + \frac{k_{pdc}}{C_{dc}} \right]s + \frac{k_{idc}}{C_{dc}}} \quad (4.28)$$

Since the dc-side voltage change is much slower than that of the inner fundamental current due to limitations imposed by the magnitude of its energy storage devices (dc link capacitor), the gains of the outer controller loop gains are selected such that the closed loop poles or Eigenvalues are located at -37 and -12.5. The gains corresponding to these poles are $k_{pdc}=0.1A/V$ and $k_{idc}=1AV^{-1}s^{-1}$.

4.2.2 Simulation Study

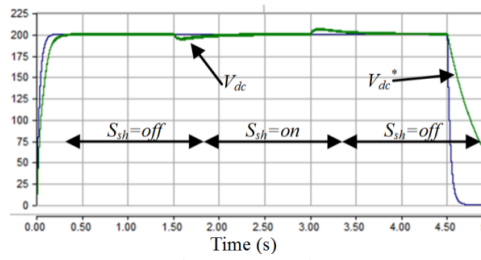
i Scaled-down simulation

PSCAD/EMTDC simulation software was used to model the buck-boost converter in Figure 4.1(a), including the current and voltage controllers defined by (4.15) and (4.24) respectively. For demonstration of the closed-loop performance, a 320W system with parameters in Table 4.1 is simulated. Initially, the converter is loaded by a resistive load consists of two series connected resistors of resistance 128Ω and 44Ω. The load is increased by shorting the 44Ω resistor using a shunt semiconductor switch (S_{sh}).

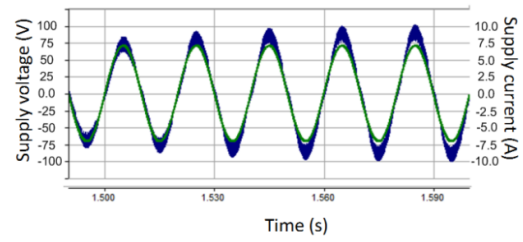
Table 4.1 Single phase system parameters

Parameter	Value
supply voltage	50V
supply frequency	50 Hz
ac side inductance	2.22mH
ac side capacitance	1 μ F
dc-side inductance	0.5mH
dc-side capacitance	2200 μ F
switching frequency	10kHz

Figure 4.4(a) shows the simulation results for the closed-loop controlled converter, where the dc link voltage is gradually increased from zero to 200V, and reduced to zero again at $t=4.5$ s. At $t=1.505$ s (at positive peak of the supply voltage), the load resistance is decreased by turning on the shunt switch S_{sh} for 1.5s, and this mimics a step change in output power from 230W to 312W, and then decreased to 230W by turning off the shunt switch (S_{sh}). Figure 4.4(a) shows the output voltage has minimum latency and over/undershoot during the load change. Simulation results in Figure 4.4(b) display supply voltage and current during the step increase in the output power. Both remain sinusoidal, with unity power factor (in phase with the supply voltage), and a rapid and smooth change in supply current is observed during the load step change. This is achieved with a 10kHz switching frequency, small ac side filter and dc-side inductance, and a sizable dc-side capacitor as an energy reservoir to prevent discontinuous load current. The soft start-up and shutdown feature demonstrated in Figure 4.4(a) makes this converter attractive as a front end for many grid-connected voltage and current source inverters since no capacitor pre-charging is required, as is the case with many other converter topologies. Thus, because of the buck-boost functionality, the inrush currents during start-up are expected to be minimal.



(a) dc output voltage



(b) Supply voltage and current during change from step increase in the output power.

Figure 4.4 Simulation results for the proposed single-phase ac-dc buck-boost converter, with $P_{\text{rated}}=320\text{W}$.

ii Converter Scalability

To show the potential for application of the proposed buck-boost converter at higher power ratings, a 3.8kW version is investigated. Simulation parameters are as in Table 4.1, except the input supply voltage v_s is increased to 220V_{RMS} and the ac side filter inductance L_s is reduced to 1mH . To test the converter's ability to provide stable dc output under different operating conditions, three cases are investigated:

Case 1: Soft start to prevent high inrush currents into the input and output capacitors.

Case 2: Dynamic response to a step increase in load from 1.58kW to 3.66kW .

Case 3: Dynamic response to a step decrease in load from 3.66kW to 1.58kW .

Figure 4.5 shows the simulated response of the converter for the three operating cases. Figure 4.5(a) shows that the converter output voltage V_{dc} closely follows its 400V dc reference, with minimum latency and over/undershoot, as the load changes. Figure 4.5 (b) shows the input current during the transition from Case 1 to Case 2, and demonstrates that it remains sinusoidal with near unity power factor. Figure 4.5(c) shows the dc output power response as the load varies during transitions between the three operating cases, and demonstrates that the control action is effective.

4.2.3 Experimental Results

Open and closed loop performance of the buck-boost converter of Figure 4.1(a) is demonstrated experimentally. The results from the open-loop tests are used to

validate the mathematical relationships presented in Section 4.2.1, without any interference from the control system. Closed-loop tests are used to illustrate converter performance when operated in grid mode, where it must comply with strict grid code requirements.

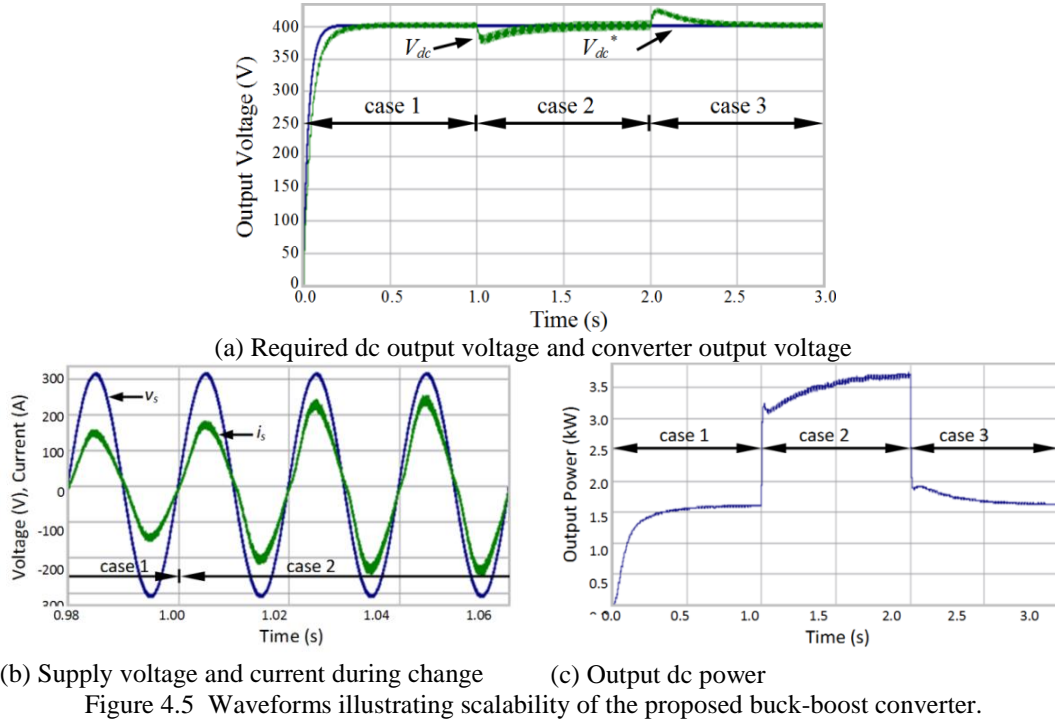


Figure 4.5 Waveforms illustrating scalability of the proposed buck-boost converter.

i Open-Loop Performance

The parameters used in the experimental validation are specified in Table 4.1. The open-loop operating scenario consists of five stages to demonstrate converter operation in both buck and boost modes. In Stage 1, the duty cycle δ is ramped from 0 to 0.25 and then maintained constant for 0.75s. In Stage 2, δ is ramped from 0.25 to 0.5 and maintained constant for 0.75s. In Stage 3, δ is ramped from 0.5 to 0.7 and maintained constant for 1s. In stages 4 and 5, δ is decreased at rates reflecting those in stages 2 and 1 respectively. Figure 4.6(a) shows converter output voltage V_{dc} during all five stages, which include both buck and boost operation. Figure 4.6(b) shows the currents in the dc-side inductor, I_{Ldc} , the load, I_{dc} , the blocking diode, I_{Dbd} , and the switch, I_s , when $\delta=0.7$. I_{Ldc} is equal to I_s during the on period of switch S , and equal to I_{Dbd} during the off period of switch S . Figure 4.6(c) shows the voltage stresses on the switch, V_s , the dc-side inductor, V_{Ldc} , and the blocking diode, V_{Dbd} , when $\delta=0.7$. From Figure 4.6(c) the average dc-side inductor voltage equals zero

over one switching (or fundamental) period. Switch voltage V_S is zero during the on period, and is equal to the sum of the dc-side inductor voltage V_{Ldc} and the supply voltage v_s during the off period. The blocking diode voltage stress V_{Dbd} is equal to the sum of the dc-side inductor voltage V_{Ldc} and the output voltage V_{dc} during the on period, whilst it is zero during the off period. These results show that the voltage ratings of switch S and blocking diode D_{bd} must be sufficient to withstand voltage stresses related to the sum of the ac source and the dc output (as with all buck-boost converters). In this experiment, blocking diode D_{bd} is rated at 600V and 40A, whilst IGBT switch S is rated at 1200V and 40A.

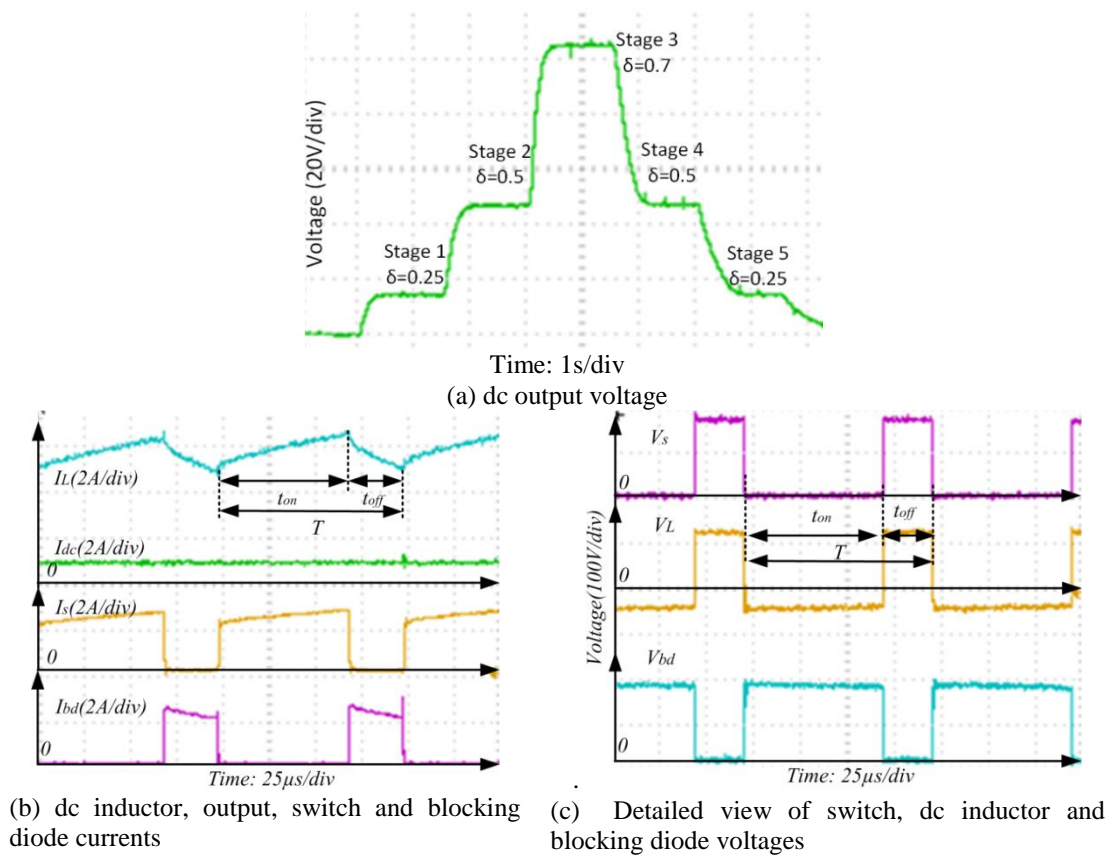


Figure 4.6 Experimental waveforms showing open-loop performance of the proposed buck-boost converter, with load resistance of 172Ω .

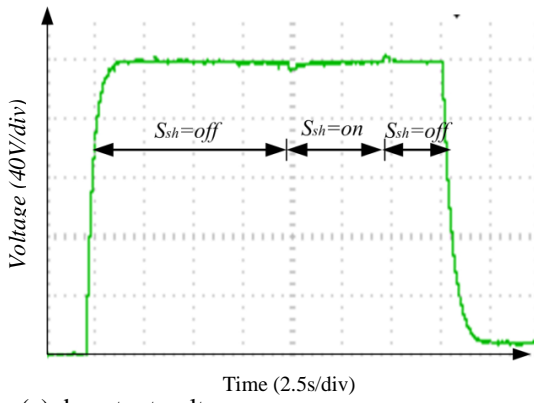
i . Closed-Loop Performance

The single-phase buck-boost converter in Figure 4.1(a) is operated under closed-loop control to substantiate the simulation results presented in Sub-section i. The system parameters and operating conditions are the same as for the simulations. The results in Figure 4.7 are obtained when the reference dc voltage is changed from 0 to 200V

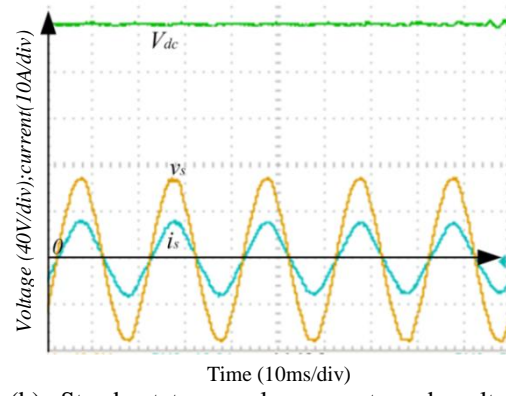
and reduced to zero after 14s (this is to demonstrate converter operation in boost and buck modes).

Figure 4.7 (a) shows that dc output voltage V_{dc} closely follows its defined reference. The dc voltage is maintained near constant as load varies. Figure 4.7 (b) shows a detailed view of the dc voltage across the load, and supply current and voltage at steady state. The converter operates at unity power factor, with 4.47% THD. Figure 4.7 (c) shows that supply current i_s and voltage v_s , and ramping up of the dc voltage during start-up, where the input supply current remains in phase and sinusoidal with the supply voltage as the dc link voltage increases. In Figure 4.7 (d) the output dc voltage experiences a small decrease during the load change, while the ac side waveform remains sinusoidal, with unity power factor.

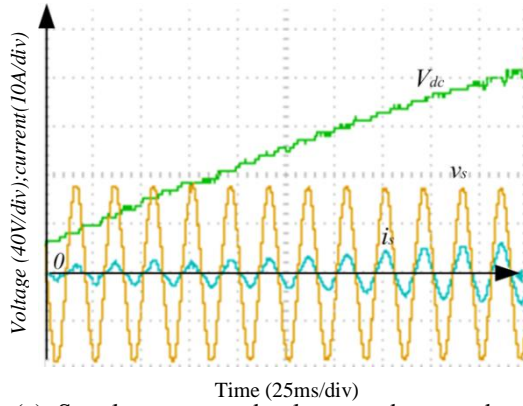
To demonstrate the power quality profile of the input current during buck and boost modes, Figure 4.8 presents supply current and voltage, and dc output voltage during different dc link reference voltages (V_{dc}^*). The waveforms in Figure 4.8(a) to (d) show the proposed buck boost converter is able to provide high quality sinusoidal supply current, with nearly unity power factor over a wide operating range.



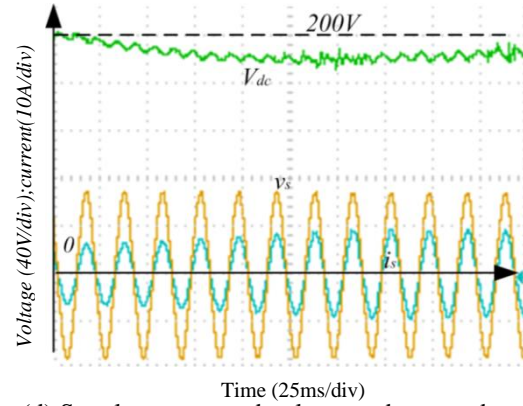
(a) dc output voltage



(b) Steady-state supply current and voltage, $V_{dc}=200V$ and $R_{dc}=172\Omega$

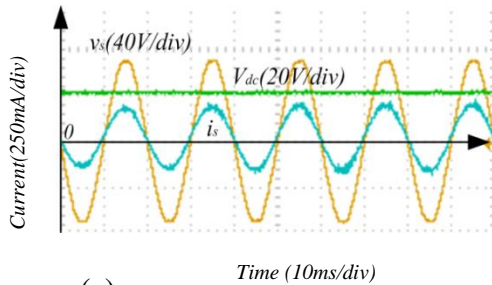


(c) Supply current and voltage, and output dc voltage during start-up

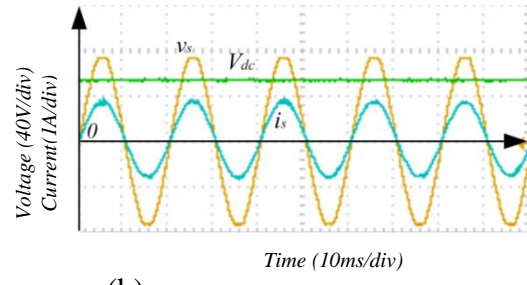


(d) Supply current and voltage and output dc voltage during step increase in output voltage

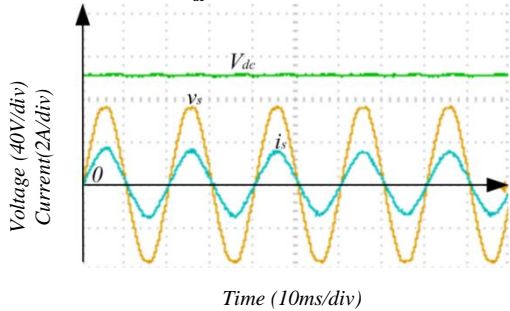
Figure 4.7 Experimental waveforms of closed-loop performance of proposed buck-boost converter, with $P=320W$.



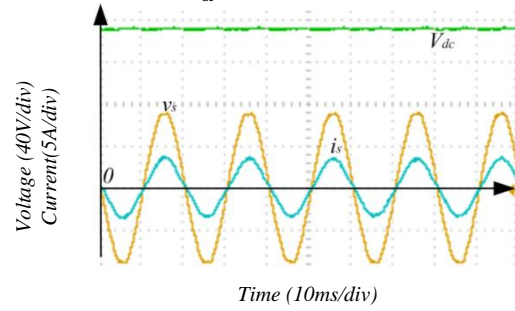
(a) Steady-state supply current and voltage
THD=2.88% at $V_{dc}^*=20V$



(b) Steady-state supply current and voltage
THD=2.08% at $V_{dc}^*=50V$



(c) Steady-state supply current and voltage
THD=3.6% at $V_{dc}^*=100V$



(d) Steady-state supply current and voltage
THD=4.09% at $V_{dc}^*=150V$

Figure 4.8 Experimental waveforms of closed-loop performance of proposed buck-boost converter, at different output dc-voltage V_{dc}^* and load resistance equals 172Ω .

4.3. Three-phase buck-boost converter

This section introduces a three-phase buck-boost converter for medium-voltage high-power applications where the switching frequency is less than 1.5kHz, and provides the filter design and power factor profile.

4.3.1 Circuit description

Figure 4.9(a) shows that the three-phase ac-dc buck-boost converter being investigated consists of a three-phase L-C filter followed by a three-phase bridge rectifier, with a series switch S placed between the bridge and the dc-side inductor L_{dc} . The three-phase buck-boost converter has seven operational modes, six of which are conducting modes whilst the seventh is an intervening freewheel mode. The different conducting modes are defined by the conduction sequence of the three-phase bridge rectifier diodes, and are shown in Table 4.2. Bridge diode conduction Mode 1 is shown as an example in Figure 4.9(b). The freewheeling mode (Mode 7) occurs when switch S is turned off, allowing dc inductor current I_L to decrease whilst charging the dc-side capacitor C_{dc} and supplying the load, as shown in Figure 4.9(c).

Table 4.2 Three-phase buck-boost converter conduction modes

	Operating Mode					
	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
Conduction period ωt	$0^\circ\text{--}60^\circ$	$60^\circ\text{--}120^\circ$	$120^\circ\text{--}180^\circ$	$180^\circ\text{--}240^\circ$	$240^\circ\text{--}300^\circ$	$300^\circ\text{--}360^\circ$
Lower active diode	D_5	D_1	D_1	D_3	D_3	D_5
Upper active diode	D_6	D_6	D_2	D_2	D_4	D_4

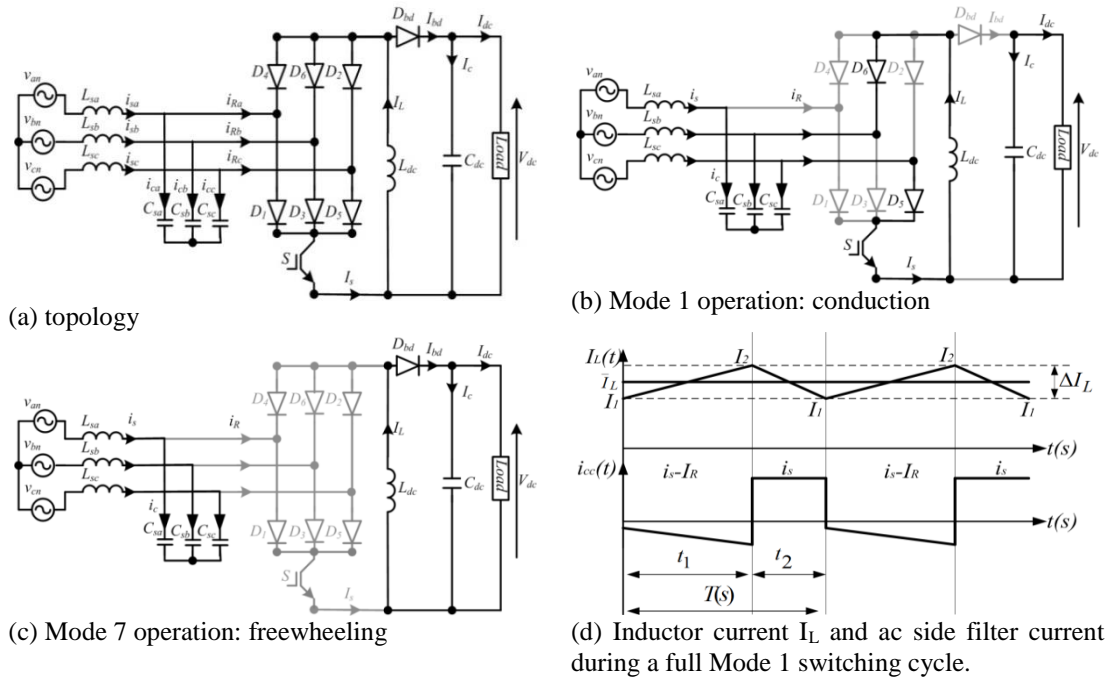


Figure 4.9 Proposed three-phase buck-boost converter and illustration of its operation modes

In Mode 1, diodes D_5 and D_6 conduct as they experience the largest line-to-line voltage; hence, the three-phase bridge dc output voltage is equal to the instantaneous ac side capacitor line-to-line voltage v_{cb} . When switch S is in the ‘on’ state, the ac side capacitor C_{sc} discharges by changing its current direction to supply dc-side inductor L_{dc} , where the dc-side inductor current I_L equals the sum of the ac side filter capacitor current i_{cc} and supply current i_{sc} . When switch S is in the ‘off’ state, the ac side capacitor C_{sc} charges and its current i_{cc} is equal to supply current i_{sc} , as shown in Figure 4.9 (c) and (d). The following assumptions are made when deriving an expression for the dc output voltage, V_{dc} .

1. The ac side capacitor operates in a continuous conduction mode.
2. The three-phase bridge average output voltage is $\frac{-3\sqrt{3}}{\pi}V_{Cm}$, where V_{Cm} is the peak fundamental phase voltage across the ac side capacitors. The negative sign reflects the inversion of the bridge output voltage with respect to the load ground.
3. The dc-side inductor current is continuous, increasing linearly from I_1 to I_2 during $0 \leq t \leq t_1$ and decreasing linearly from I_2 to I_1 during $t_1 \leq t \leq t_2$, so that $\Delta I_L = I_2 - I_1$, as shown in Figure 4.9(d).
4. The ac side current is sinusoidal and is in ac steady-state during each switching period.

Switching utilizes a combination of natural and forced commutation of the diodes, and a self-commutated switch to achieve balanced current sharing between the diodes. In Mode 1, the voltage across dc-side inductor L_{dc} equals the instantaneous value of v_{Ccb} . The differential equations describing operation during conduction Mode 1 are:

$$\frac{dI_L}{dt} = \frac{v_{Ccb}}{L_{dc}} \quad (4.29)$$

$$\frac{dV_{dc}}{dt} = \frac{-I_{dc}}{C_{dc}} \quad (4.30)$$

$$i_{sc} = i_{cc} + I_s \quad (4.31)$$

Where I_s is the instantaneous switch (IGBT) current, i_{cc} is the current in the ac filter capacitor of phase 'c', i_{sc} is phase 'c' supply current, I_{dc} is the instantaneous dc output (load) current, V_{dc} is the dc load voltage, v_{Ccb} is the line-to-line voltage across the ac filter capacitors connected between phases 'b' and 'c', and I_L is inductor current.

In freewheeling Mode 7, the dc-side equations are:

$$\frac{dI_L}{dt} = \frac{-V_{dc}}{L_{dc}} \quad (4.32)$$

$$\frac{dv_{dc}}{dt} = \frac{I_L - I_{dc}}{C_{dc}} \quad (4.33)$$

In this mode, the rectifier input currents i_{Ra} , i_{Rb} and i_{Rc} are zero. Thus equation (4.31)

becomes:

$$i_{sc} = i_{cc} \quad (4.34)$$

For phase 'c', the ac filter current is:

$$i_{cc} = C \frac{dv_{Cc}}{dt} \quad (4.35)$$

For the conducting modes, equation (4.29) becomes:

$$\Delta I_L = \frac{3\sqrt{3}}{\pi} \frac{t_1 V_{Cm}}{L_{dc}} \quad (4.36)$$

Similarly, equation (4.32) in the freewheeling mode becomes:

$$\Delta I_L = \frac{-t_2 V_{dc}}{L_{dc}} \quad (4.37)$$

From (4.36) and (4.37):

$$\frac{3\sqrt{3}}{\pi} \frac{t_1 V_{Cm}}{L_{dc}} = \frac{t_2 V_{dc}}{L_{dc}} \quad (4.38)$$

$$V_{dc} = \frac{3\sqrt{3}}{\pi} \frac{\delta}{1-\delta} V_{Cm} = 1.65 \frac{\delta}{1-\delta} V_{Cm} \quad (4.39)$$

Since dc-side capacitor voltage balance necessitates that the average capacitor current over one or a number of consecutive switching cycles is zero ($\bar{I}_c = 0$), the relationship between the average inductor current \bar{I}_L and the average load current \bar{I}_{dc} is:

$$\bar{I}_c = \frac{1}{T} \left(\int_0^{\delta T} (-I_{dc}) dt + \int_{\delta T}^T (\bar{I}_L - I_{dc}) dt \right) = 0 \quad (4.40)$$

$$\bar{I}_{dc} = (1-\delta)\bar{I}_L \quad (4.41)$$

Therefore, for a resistive load, the average dc output voltage \bar{V}_{dc} can be expressed in terms of average inductor current \bar{I}_L .

$$\bar{V}_{dc} = (1-\delta)R_{dc}\bar{I}_L \quad (4.42)$$

Since the switch current I_s equals the inductor current I_L in the conducting modes, the relation between the average switch current \bar{I}_s and the average inductor current \bar{I}_L is:

$$\bar{I}_s = \delta\bar{I}_L \quad (4.43)$$

The relationship between average switch current \bar{I}_s and the average output current \bar{I}_{dc} can be derived by substituting equation (4.41) into (4.43):

$$\bar{I}_s = \frac{\delta}{1-\delta} \bar{I}_{dc} \quad (4.44)$$

The relationship between the supply phase current and the average output current \bar{I}_{dc} can be obtained by substituting (4.44) into (4.31):

$$i_{sc} = -C \frac{dv_{Cbc}}{dt} + \frac{\delta}{1-\delta} \bar{I}_{dc} \quad (4.45)$$

Assuming lossless conversion, power balance dictates that power into the converter equals the dc output power:

$$\frac{3}{2} i_{Rm_fund} V_{cm} = V_{dc} I_{dc} \quad (4.46)$$

Where i_{Rm_fund} is the peak fundamental converter input current. Substituting (4.39) into (4.46) gives:

$$i_{Rm_fund} = \frac{2\sqrt{3}}{\pi} \frac{\delta}{1-\delta} \bar{I}_{dc} \quad (4.47)$$

The rms current in switch S can be calculated as [63]:

$$I_{s_rms} = \bar{I}_L \sqrt{\delta} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta I_L}{\bar{I}_L} \right)^2} \quad (4.48)$$

Equation (4.48) can be used to calculate the per-phase rms converter input current i_{R_rms} :

$$i_{R_rms} = \sqrt{\frac{2}{3}} I_{s_rms} = \sqrt{\frac{2}{3}} \bar{I}_L \sqrt{\delta} \sqrt{1 + \frac{1}{3} \left(\frac{1/2 \Delta I_L}{\bar{I}_L} \right)^2} \quad (4.49)$$

To facilitate rectifier input current analysis, the dc-side inductance L_{dc} is assumed sufficiently large so that the dc-side inductor current is constant (ripple free) and equals \bar{I}_L . Figure 4.10 shows rectifier input current during one fundamental cycle, and during one carrier cycle, and shows that this three-phase buck-boost converter operates with a constant duty cycle. A triangular carrier is used to ensure good

harmonic performance, with the current pulses centred within each carrier period, as shown Figure 4.10.

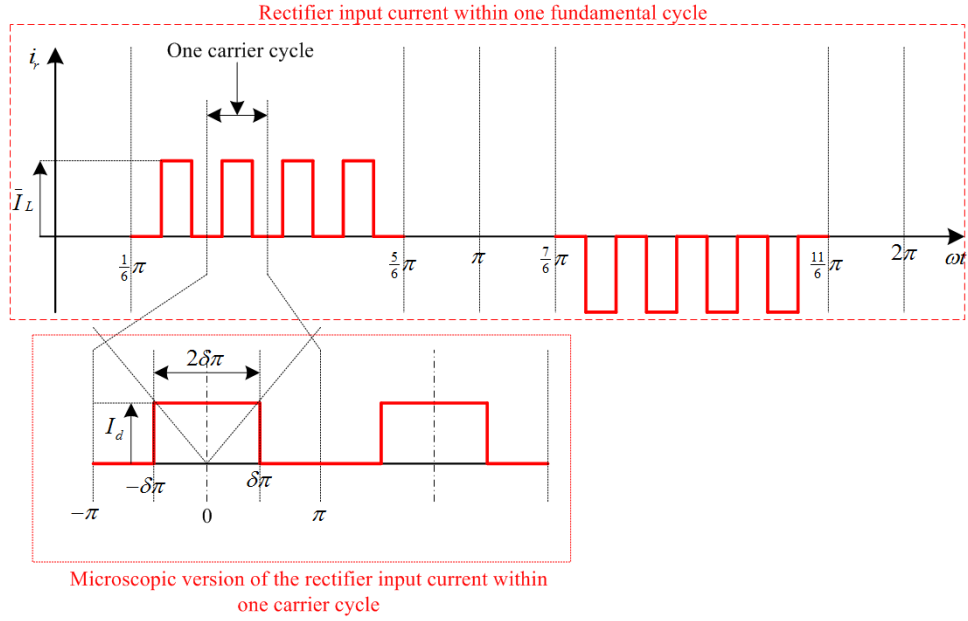


Figure 4.10 Rectifier input current during one carrier cycle.

The spectrum of the rectifier input current i_R can be obtained using the double Fourier series in complex form [64]:

$$i_{r(m,n)} = \frac{1}{2\pi^2} \left[\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} \int_{-\delta\pi}^{\delta\pi} I_L e^{j(mx+ny)} dx dy + \int_{\frac{7\pi}{6}}^{\frac{11\pi}{6}} \int_{-\delta\pi}^{\delta\pi} I_L e^{j(mx+ny)} dx dy \right] \quad (4.50)$$

Where $y = \omega_0 t$ and $x = \omega_c t$, ω_0 and ω_c respectively represent fundamental and carrier frequencies in rad/s, and m and n respectively are the orders of the carrier and baseband component harmonics.

The baseband harmonics of the rectifier input current i_R are computed by setting $m=0$ in (4.50), yielding:

$$i_{r(0,n)} = A_{0n} + jB_{0n} = \frac{j2\sqrt{3}\delta I_L}{n\pi} \quad (4.51)$$

Equation (4.51) is valid for all n that represent odd and non-triplen harmonics; otherwise $C_{0n}=0$, meaning that $A_{0n}=0$ and $B_{0n}=\frac{2\sqrt{3}\delta\bar{I}_L}{n\pi}$. The peak of the rectifier input fundamental component i_{Rm_fund} is obtained with $n=1$, so that:

$$i_{Rm_fund} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} = \frac{2\sqrt{3}}{\pi} \frac{\delta}{1-\delta} \bar{I}_{dc} \quad (4.52)$$

The peak fundamental current obtained from the double Fourier series (4.52) is the same as that obtained from the power balance equation (4.47). This validates the input current analysis presented.

The carrier frequency harmonic components are obtained by setting $n=0$ in (4.50), yielding:

$$C_{m0} = A_{m0} + jB_{m0} = \frac{4\bar{I}_L}{3m\pi} \sin(\delta m\pi) \quad (4.53)$$

From (4.53), $A_{m0} = \frac{4\bar{I}_L}{3m\pi}$ and $B_{m0}=0$. The peaks of the 1st and 2nd carrier frequency components can be obtained by setting $m=1$ and 2 respectively.

The sideband harmonics are obtained by computing (4.50) for non-zero m and n as:

$$C_{mn} = A_{mn} + jB_{mn} = \frac{j4\bar{I}_L}{nm\pi^2} \sin(\delta m\pi) \sin\left(\frac{1}{3}n\pi\right) e^{j\frac{1}{2}\pi(n+1)} \quad (4.54)$$

From(4.54), $A_{mn}=0$ and $B_{mn} = \frac{4\bar{I}_L}{nm\pi^2} \sin(\delta m\pi) \sin\left(\frac{1}{3}n\pi\right) e^{j\frac{1}{2}\pi(n+1)}$, and from the double Fourier series, the rectifier input current expressions are:

$$\begin{aligned} i_r(t) = & \frac{1}{2}A_{00} + \sum_{n=1}^{\infty} (A_{0n} \cos n\omega_0 t + B_{0n} \sin n\omega_0 t) + \sum_{m=1}^{\infty} (A_{m0} \cos m\omega_c t + B_{m0} \sin m\omega_c t) \\ & + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} (A_{mn} \cos((m\omega_c + n\omega_0)t) + B_{mn} \sin((m\omega_c + n\omega_0)t)) \end{aligned} \quad (4.55)$$

$$\begin{aligned} i_r(t) = & \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin n\omega_0 t + \frac{4\bar{I}_L}{3\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sin(\delta m\pi) \cos m\omega_c t \\ & + \frac{4\bar{I}_L}{\pi^2} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{mn} \sin(\delta m\pi) \sin\left(\frac{1}{3}n\pi\right) e^{j\frac{1}{2}\pi(n+1)} \sin((m\omega_c + n\omega_0)t) \end{aligned} \quad (4.56)$$

The first term in (4.55) represent the dc-offset when $n=m=0$. The first summation ($\sum_{n=1}^{\infty}$) defines the fundamental low-frequency harmonics which include the low-order undesired harmonics. The second summation ($\sum_{m=1}^{\infty}$) corresponds to the high-frequency carrier wave harmonics. The third summation ($\sum_{m=1}^{\infty} \sum_{-\infty}^{\infty}$) refers to the sideband harmonics, which exist as groups around the carrier harmonic frequencies [64]. Equation (4.56) provides a theoretical solution for interpreting the ac harmonic distribution of the converter under investigation, including basebands, carrier frequency, and sidebands harmonics. Also, equation (4.56) assists filter design as it provides information about the location of the dominant low-order and switching frequencies to be eliminated.

4.3.2 Control Stage

The proposed buck-boost converter provides a stable output dc voltage using the simple control structure in Figure 4.11 that consists of outer voltage and inner current control loops. In the voltage control loop, the reference dc voltage V_{dc_ref} is subtracted from the load voltage V_{dc_fb} , and then the voltage error is input to a PI controller, which generates the reference average inductor current $\overline{I_{L_ref}}$. A current limiter is used to provide overload protection. $\overline{I_{L_ref}}$ is the input to the current control loop and is subtracted from the average inductor current $\overline{I_L}$. The resulting error is input to a PI controller, whose output is compared with a triangular carrier wave to provide the gating signal required to control the buck-boost converter switch.

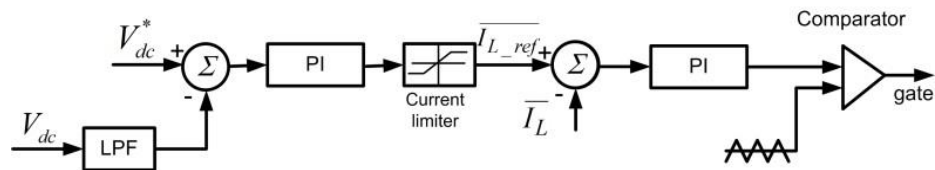


Figure 4.11 Three-phase buck-boost converter control circuit.

4.3.3 Filter Design

Like the current source rectifier, the phase current conduction period of the buck-boost converter is $\frac{2}{3}\pi$ radians per half-cycle. The design of the ac side LC filter depends on several factors, such as the rectifier switching frequency (which is between 512Hz and 1.2kHz for medium-power applications), LC resonant mode,

required line current THD, and input power factor. Equation (4.51) can be used to show that the converter input current contains high levels of the 5th and 7th harmonics. The cut-off frequency of the ac-side filter is therefore selected to be 2.5 times greater than the supply frequency f (50Hz in this case) and the input filter capacitance is 0.33pu, which is within the normal range for capacitance in high-power PWM-current source rectifiers that use a low switching frequency [65]. Simulation results for different operating conditions show that for acceptable supply current THD; the ac filter cut-off frequency must be 2.4. On this basis, the ac side filter inductance L_s can be calculated as shown in (4.57) and [31]:

$$2.4\omega_B = \frac{1}{\sqrt{L_s C_s}} \quad (4.57)$$

$$L_s = \frac{1}{5.76\omega_B^2 C_s} \quad (4.58)$$

Where ω_B is the base frequency in rad/s, C_s is the ac side filter capacitance, base capacitance $C_B = 1/\omega_B Z_B$, base inductance $L_B = Z_B/\omega_B$, and Z_B is the base impedance [66].

$$L_s = \frac{1}{5.76\omega_B^2 \left(\frac{0.33}{\omega_B Z_B}\right)} = \frac{Z_B}{1.9\omega_B} = 0.53L_B \quad (4.59)$$

Equations (4.60) and (4.61) express the ac side filter parameters based on rated line-to-line voltage V_{LL} and desired converter input power P in a star configuration, while equation (4.62) specifies the filter capacitance C_s in the delta connection case.

$$L_s = 0.53 \frac{V_{LL}^2}{2\pi f P} \quad (4.60)$$

$$C_s = 0.33 \frac{P}{2\pi f V_{LL}^2} \quad (4.61)$$

$$C_s = 0.11 \frac{P}{2\pi f V_{LL}^2} \quad (4.62)$$

4.3.4 Power factor analysis

Based on simulation and experimental results obtained under different operating conditions, the proposed buck-boost converter power factor profile depends on the converter input power, and is independent of operating mode (buck or boost). Figure 4.12 shows the power factor profile at different load conditions, using the filter values based on equations (4.60) and (4.61). The input power factor varies in the narrow range between 0.98 and 1 when the converter input power is varied between 0.8pu and 1.2pu. Between input powers of 0.7pu and 0.8pu, power factor varies between 0.95 and 0.98. Below this operating range, the converter input power factor decreases to 0.85 at 0.5pu of rated input power.

4.3.5 Three-phase buck-boost converter simulation

This section presents simulation results of the proposed buck-boost converter, using the PSCAD/EMTDC environment, with the converter operating in buck and boost modes. The converter parameters used in both the simulations and experimental validation are listed in Table 4.3.

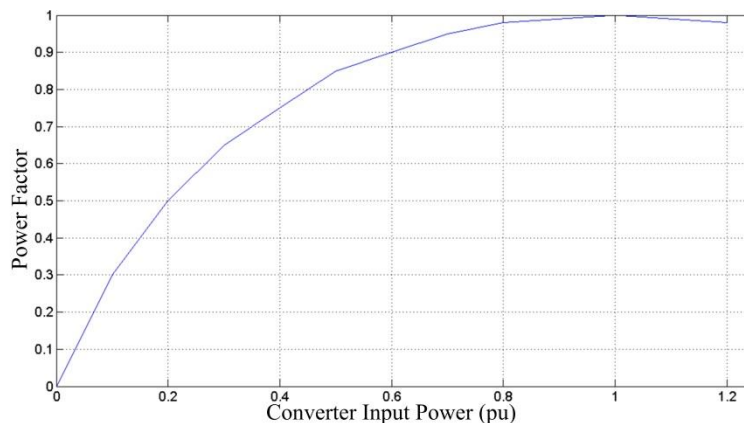


Figure 4.12 Power factor profile of the proposed buck-boost converter.

Table 4.3 Three-phase converter buck-boost parameters

Parameter	Value
Rated input power	1800W
Input supply line-to-line voltage	75V
Supply frequency	50Hz
AC side per phase filter capacitance (delta-connected)	115 μ F
AC side per phase filter inductance	5.7mH
DC-side inductance	5mH
DC-side capacitance	3300 μ F
PWM switching frequency	1.2kHz
Load resistance	26 Ω

i Scaled down simulation

Experimentation and simulation are both conducted at a rated input power of $P=1800W$. From equation (4.60) the ac side inductance is 5.3mH (experimentally, 5.7mH inductance is used due to availability), while from equation (4.62), the ac side filter capacitance is 112 μ F (experimentally, 115 μ F capacitors due to availability).

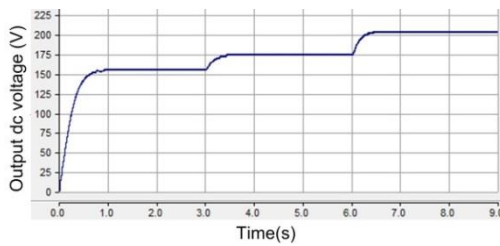
The reference dc voltage V_{dc_ref} is passed through a 1Hz low-pass filter to ramp any step change in the dc reference voltage V_{dc_ref} . This ensures controlled charging of the bulky dc-side capacitor filter, avoiding the need for a capacitor pre-charge circuit. The dc voltage reference is initially $V_{dc_ref}=154V$. At $t=3s$, the reference is stepped to $V_{dc_ref}=174V$, then at $t=6s$, the reference is stepped to $V_{dc_ref}=204V$. These values correspond to 0.55pu, 0.72pu and 1pu rated input power, respectively.

Figure 4.13 shows simulation results when the converter is operated from a 50Hz three-phase ac supply. Figure 4.13(a) shows the dc output voltage, where the converter is able to provide stable dc voltage with soft start-up. Figure 4.13(b) shows the supply current, which increases smoothly without overshoot or oscillation. Figure 4.13(c) shows the active input power at each output voltage. Figure 4.13(d) shows a detailed view of the three-phase supply current and phase-a voltage at $V_{dc_ref}=174V$, where the supply current has a THD=4.05% and a power factor of 0.956. Figure 4.13(e) shows a detailed view of the three-phase supply current and phase-a voltage at $V_{dc_ref}=204V$ where THD is 4.4% and the power factor is 0.999. The results in Figure 4.13 establish that the proposed three-phase buck-boost converter can provide high-quality sinusoidal input current at power factor dependant on

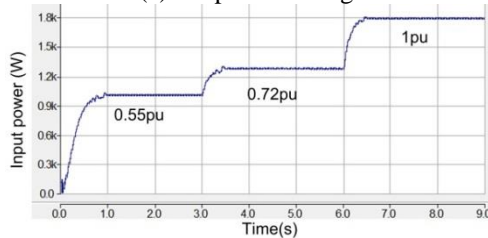
converter rated power, as mentioned in sub-section 4.3.4 and as shown in Figure 4.13.

ii Three-phase buck-boost converter scalability.

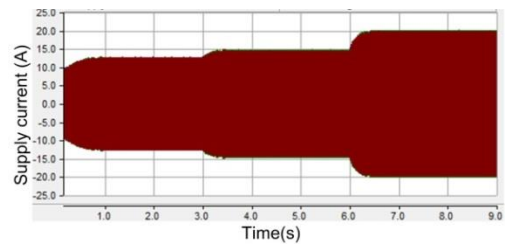
To investigate the potential applicability of the proposed buck-boost converter in high-power, medium-voltage applications, a 1MW version is connected to a 3.3kV line-to-line ac supply, with parameters listed in Table 4.4, was designed and simulated. Initially, the reference dc voltage the converter presents across 150Ω load resistance is set to 10kV. At time $t=0.75s$, the load resistance is reduced to 100 Ω to test the dynamic response of the proposed converter. The simulation results are displayed in Figure 4.14. In Figure 4.14 (a), the dc output voltage is ramped from 0 to 10kV_{dc}, and also overcomes the step increase on the load with minimum under shoot. Figure 4.14 (b) shows that the converter draws sinusoidal supply current with low distortion, the supply current THD is 3.6% and the power factor is 0.92 during case 1, and during case 2 supply current THD is 4.1% and the power factor is 0.99. The expected voltage stress on switch S, for a 3.3kV input line to line voltage and 10kV output dc voltage, is $3.3 \times \sqrt{2} + 10 = 15.7kV$, as shown in Figure 4.14(c), implying series device connection. The dc-link inductance current is shown in Figure 4.14(d), where the inductor current is continuous and increases from case 1 to case 2 to compensate the step load increase.



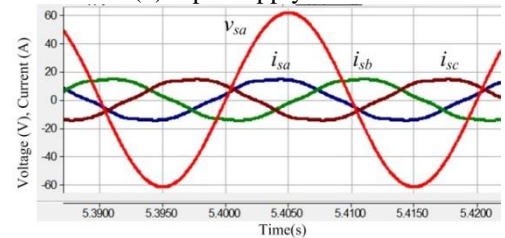
(a) Output dc voltage



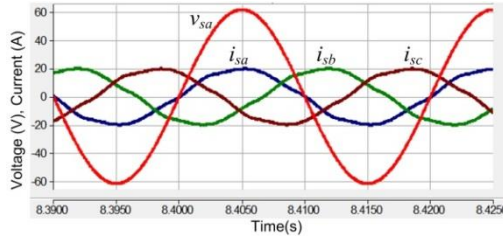
(c) Input active power profile



(b) Input supply current



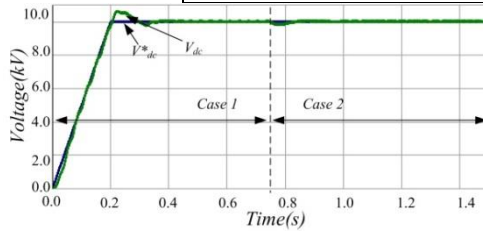
(d) Input supply three-phase currents and phase-a voltage at $V_{dc_ref}=174V$



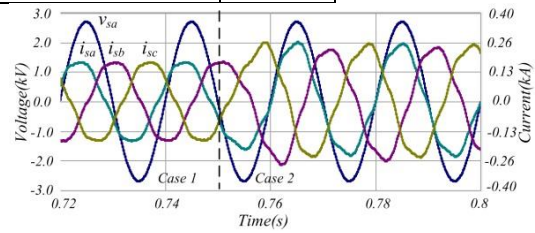
(e) Input supply three-phase currents and phase-a voltage at $V_{dc_ref}=204V$
 Figure 4.13. Simulation of the three-phase buck-boost converter during buck and boost operation modes.

Table 4.4: Proposed buck-boost medium-voltage system parameters.

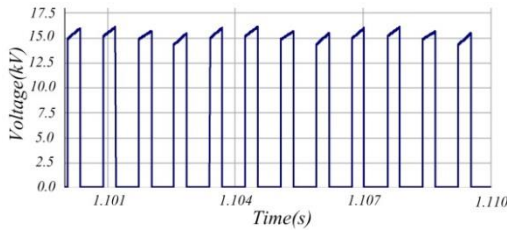
Medium-Voltage System Parameters	Rating
Rated power	1MW
Input supply line-to-line voltage	3.3kV
Supply frequency	50Hz
AC side per phase filter capacitance (Y-connected)	96 μ F
AC side per phase filter inductance	18.3mH
Dc-side inductance	10mH
Dc-side capacitance	2200 μ F
PWM switching frequency	1.2kHz
Load resistance	17.4 Ω



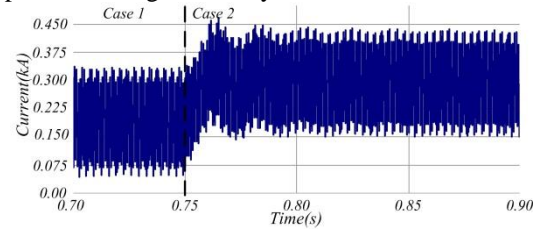
(a) Output dc voltage.



(b) Input supply current (multiplied by 2) and phase-a voltage in steady state.



(c) Output power.



(d) Switch voltage stress.

Figure 4.14: Simulation waveforms for a 1MW system, illustrating scalability of the proposed three-phase buck-boost converter.

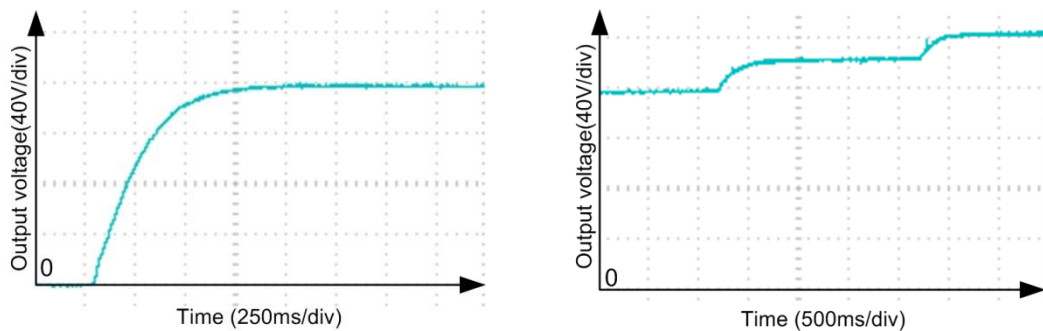
4.3.6 Three-phase buck-boost converter experimental results

Experimental results for a 1.8kW version of the proposed three-phase buck-boost converter are presented in Figure 4.15 and Figure 4.16 to substantiate the theoretical discussion in Section 4.3.1 and to confirm the simulations presented in subsection i.

The parameters used for both simulation and experimental validation are listed in Table 4.4.

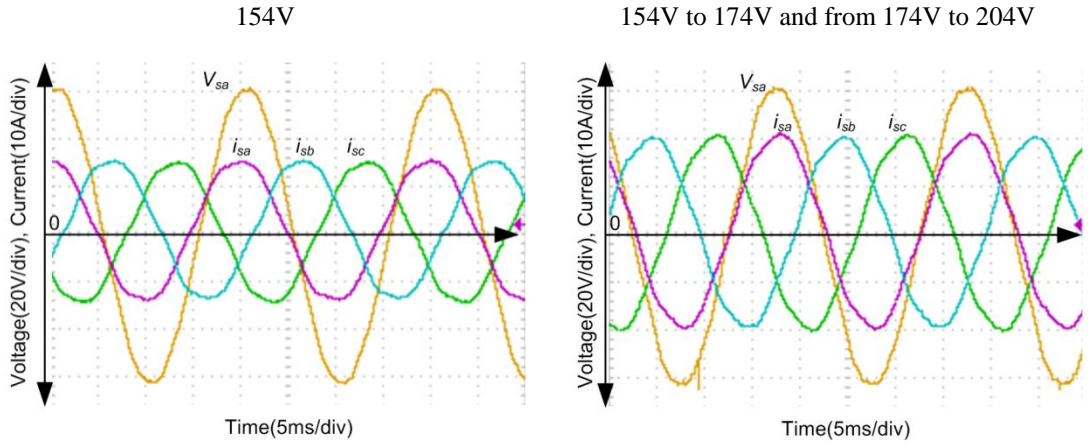
Figure 4.15(a) shows the output voltage during start-up from zero to 154V (buck mode), where the voltage build-up is stable and gradual. Figure 4.15(b) shows dc output voltage during steady state, and during the transitions from 154V to 174V and from 174V to 204V (boost modes). Figure 4.15(c) and (d) show the three-phase input currents and phase a voltage, where $V_{dc_ref} = 174V$ and $V_{dc_ref} = 204V$ respectively. The input currents are continuous and sinusoidal with limited distortion and near unity power factor, as with the simulations in Section III. These results establish that the presented ac-dc buck-boost converter could be used as an interfacing converter for permanent magnet wind-turbine generators, without the risk of pulsating torque that results with uncontrolled diode bridge rectification.

Figure 4.16(a) shows dc-side inductor current I_L , dc load current I_{dc} , and switch S and diode D_{bd} currents I_s and I_{bd} respectively. From Figure 4.16(a), the current I_L in the dc-side inductor increases during the ‘on’ period and is equal to the switch current I_s , while during the ‘off’ period the current in the inductor reduces and is equal to the blocking diode current I_{bd} . The voltage stresses across the dc-side inductor V_L , switch V_s and diode V_{bd} are shown in Figure 4.16(b), from which the inductor voltage V_L equals the supply voltage during the ‘on’ period and equals the output dc voltage during the ‘off’ period. The maximum switch voltage stress (V_{S-max}) is the sum of the peak line voltage across the ac side capacitors and the dc output voltage during the off-period. The maximum voltage stress on the blocking diode (V_{bd-max}) is the sum of the peak line voltage across the ac side capacitors and the dc output voltage during the on-period.



(a) Output dc voltage during start-up from zero to

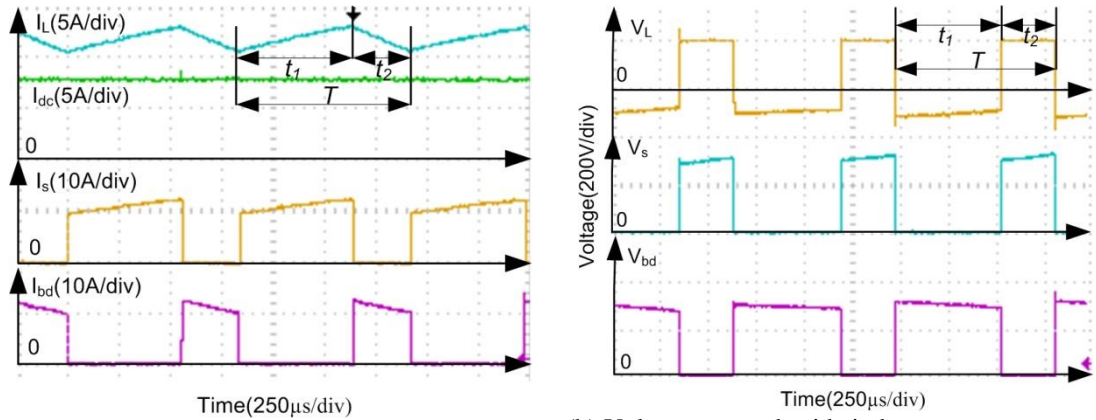
(b) Output dc voltage during transitions from



(c) Detailed view of the three-phase supply currents and phase-a voltage at 0.72pu of rated input power

(d) Detailed view of the three-phase supply currents and phase-a voltage at 1pu of rated input power.

Figure 4.15: Experimental waveforms for the 1.8kW prototype three-phase buck-boost converter demonstrating its practical viability.



(a) dc inductor currents, output dc current, bridge rectifier output current, and dc blocking diode (D_{bd}) current.

(b) Voltage across dc-side inductor, semiconductor switch S and blocking diode D_{bd} .

Figure 4.16: Experimental voltage and current waveforms for the dc-side inductor, blocking diode and switch at the rated output voltage $V_{dc_ref}=204V$.

The results in Figure 4.16 aid in the determination of the current and voltage ratings of the dc-side inductor L_{dc} , switch S , and blocking diode D_{bd} . The results presented in Figure 4.15 and Figure 4.16 establishes that the proposed buck-boost converter is a viable candidate for high-power, medium-voltage ac-dc applications. Table 4.5, which summarises the converter's performance, shows that the supply current has low THD and high power factor over a wide operating range. At 98%, the efficiency of the proposed buck-boost converter is good. The 2% power loss is due to:

- dc and ac copper resistance losses in the dc-side inductors.

- Semiconductor power losses, from the effective series connection of two diodes and an IGBT switch.
- Forward voltage drop across the power diodes (2.3V at 25 °C), and IGBT forward voltage V_{CE} (1.95V at 25 °C): these would be less significant at higher supply voltages.

Overall system efficiency is also reduced due losses in the ac side inductor.

Table 4.5 Overall performance summary of the proposal buck-boost converter.

Input Power (W)	Input Power (pu)	Power Factor	Output dc Voltage (V)	Output dc Power (W)	Overall Efficiency (%)	Supply Current THD (%)	Converter Input Power (W)	Converter Efficiency (%)
1800	1	0.996	204	1606.7	0.89	3.94	1625W	0.985
1300	0.722	0.955	174	1164	0.895	4.14	1185W	0.98
1005	0.55	0.873	154	915.6	0.91	3.87	927W	0.987

4.4. Dual three-phase buck-boost converter

Figure 4.17(a) shows the proposed dual three-phase buck-boost converter which is composed of a three phase supply connected to the primary side of phase-shifting transformer. The secondary and the tertiary windings are star and delta connected respectively, and each winding is connected to an ac side capacitor filter C_s and a three-phase diode rectifier bridge. The two three-phase diode rectifiers (D_1 to i_{12}) and the power electronic switch S are connected in series. The converter has 12 active conduction modes when the switch S is on as summarized in Table 4.6, and one freewheeling mode when the switch S is off. The operating principle is similar to the three-phase buck-boost converter.

The average output of each bridge is $-1.654V_{m1}$ and $-1.654V_{m2}$, where V_{m1} and V_{m2} are the peak fundamental of the two transformer secondary line to line voltage respectively and $V_{m1}=V_{m2}=V_m$. Similarly as described in the three-phase buck-boost conversion section, the converter voltage gain is:

$$V_{dc} = 2 \frac{3\sqrt{3}}{\pi} \frac{\delta}{1-\delta} V_m = 3.3 \frac{\delta}{1-\delta} V_m \quad (4.63)$$

4.4.1 Filter design and power factor performance

The converter admittance can be written in terms of the filter capacitance and transformer inductances [67-69] as:

$$Y(s) = SC_s + \frac{1}{SL_r + \frac{1}{\frac{1}{SL_s} + \frac{SC_s}{s^2 L_r C_s + 1}}} \quad (4.64)$$

Table 4.6 Dual three-phase buck-boost converter active modes.

Modes	1	2	3	4	5	6
ωt	0-30	30-60	60-90	90-120	120-150	150-180
Active diode	D ₂ ,D ₆ ,D ₈ &D ₁₀	D ₂ ,D ₄ ,D ₈ &D ₁₀	D ₂ ,D ₄ ,D ₉ &D ₁₀	D ₃ ,D ₄ ,D ₉ &D ₁₀	D ₃ ,D ₄ ,D ₉ &D ₁₁	D ₃ ,D ₅ ,D ₉ &D ₁₁
Modes	7	8	9	10	11	12
ωt	180-210	210-240	240-270	270-300	300-330	330-360
Active diodes	D ₅ ,D ₂ ,D ₇ &D ₁₁	D ₁ ,D ₅ ,D ₇ &D ₁₁	D ₁ ,D ₅ ,D ₇ &D ₁₂	D ₁ ,D ₆ ,D ₇ &D ₁₂	D ₁ ,D ₆ ,D ₈ &D ₁₂	D ₂ ,D ₆ ,D ₈ &D ₁₂

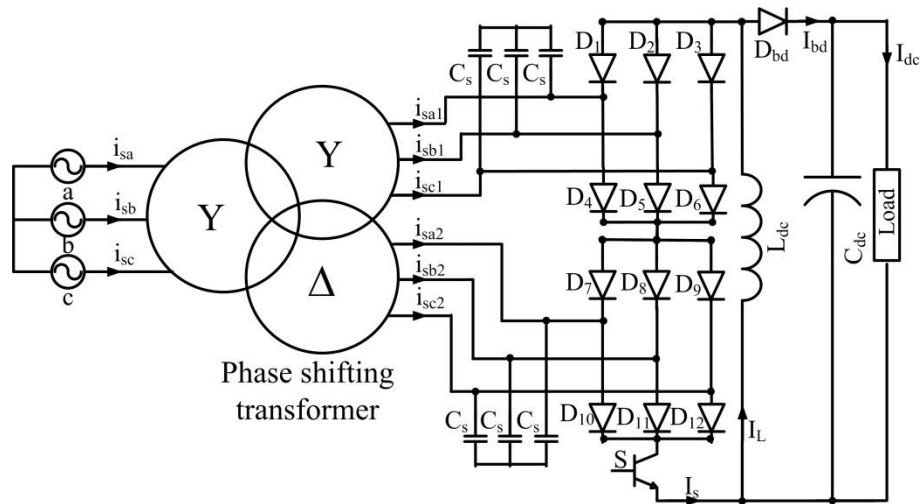


Figure 4.17: Dual three-phase buck-boost converter.

Where L_s is the primary leakage inductance plus the inductance of the supply line, and L_r is the transformer secondary leakage inductance. L_r is the secondary leakage inductance where the transformer designer ensures the Y and Δ leakage inductances are equal [69]. The parallel resonant frequency can be calculated from the zeros of $Y(s)$ admittance:

$$\omega_1 = \frac{1}{\sqrt{L_r C_s}} \quad (4.65)$$

$$\omega_2 = \frac{1}{\sqrt{(2L_s + L_r)C_r}} \quad (4.66)$$

The transformer is used to cancel the 5th, 7th, 17th, and 19th harmonic currents [66, 70], and ω_1 depends on the transformer secondary leakage inductance. Since transformer leakage inductances are known, the ac-side C-filter is selected such that the cut-off frequency is placed at nine times the base frequency ($9\omega_B$). With an ac filter designed on this basis, simulation studies show that acceptable supply current THD is achieved over the full control range.

4.4.2 Modified dual three-phase buck-boost converter

Switch S and blocking diode D_{bd} experience high voltage stress, equal to the output voltage plus peak fundamental of the two transformer secondary line to line voltages ($V_{dc}+V_{m1}+V_{m2}$). This high voltage stress would limit use of the proposed buck-boost converter in high-power medium-voltage applications. Figure 4.18 show a modified configuration that aims to share the voltage stress experience in the version in Figure 4.17 between the two switches (S_1 and S_2) and also between two blocking diodes (D_{bd1} and D_{bd2}). In this configuration, the dc side inductance is realized as centre tap inductance (with $L_{dc1}=L_{dc2}$), and two dc side capacitors ($C_{dc1}=C_{dc2}$) are connected as shown in Figure 4.18. The modified circuit retains the simplicity and performance of the original circuit, and switches S_1 and S_2 receive the same gating signals.

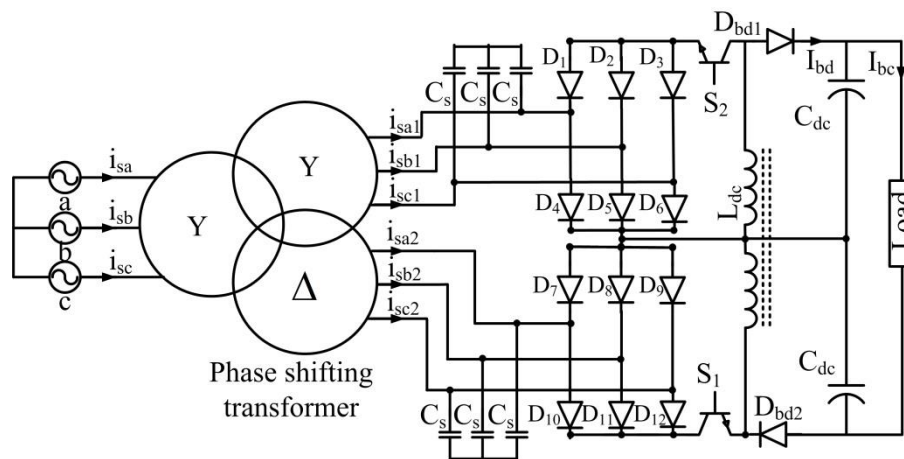


Figure 4.18 Modified configuration to share the voltage stress on the power switch and blocking diode

4.4.3 Simulation validation

The system parameters are given in Table 4.7. The operating sequence is the same operating scenario of the scalable three-phase buck-boost converter in subsection 4.3.5. The transformer primary side inductance plus the supply inductance is 0.15pu, and the secondary and tertiary leakage inductances are the same and equal to 0.1 pu. The ac-side C-filter is selected such that the cut-off frequency is nine times the base frequency ($9\omega_B$), and according to equation (4.65), the capacitor size is 0.123pu. With this capacitor bank and these transformer parameters, the converter system has unity power factor at rated load, leading input power factor higher than 0.95 at loads vary from 0.6 to 1 pu, and power factor higher than 0.9 and less than 0.95 at loads vary from 0.45 to 0.6 pu, as will show in the simulation results. Figure 4.19(a) show that the proposal converter is able to track the reference output voltage, with minimum overshoot when the load resistance is halved. Figure 4.19(b) show three-phase supply current and phase ‘a’ voltage during a step load increase. From Figure 4.19 (b) the proposed converter draws sinusoidal current from the supply, with 0.935 power factor leading at case 1 and unity power factor when the load resistance is decreased to 100Ω. The switch S is exposed to a voltage stress of 10kV approximately; see Figure 4.19 (c). Figure 4.19 (d) shows the dc-link inductor current where it increases to compensate the step load.

Table 4.7 Parameters of modified dual three-phase buck-boost converter

Parameter	Value
Rated power	1MW
Supply voltage	3.3 kV L-L
Supply frequency	50Hz
Switching frequency	1.2kHz
Transformer rated power	5MVA phase shift transformer
Transformer rated voltage	Primary side 3.3kV / two secondary sides 3.3kV
AC-side C-filter	Two 36 μ F three-phase bank
DC-side inductance	Central-taped 8mH inductance
DC-side capacitance	Two 2200 μ F

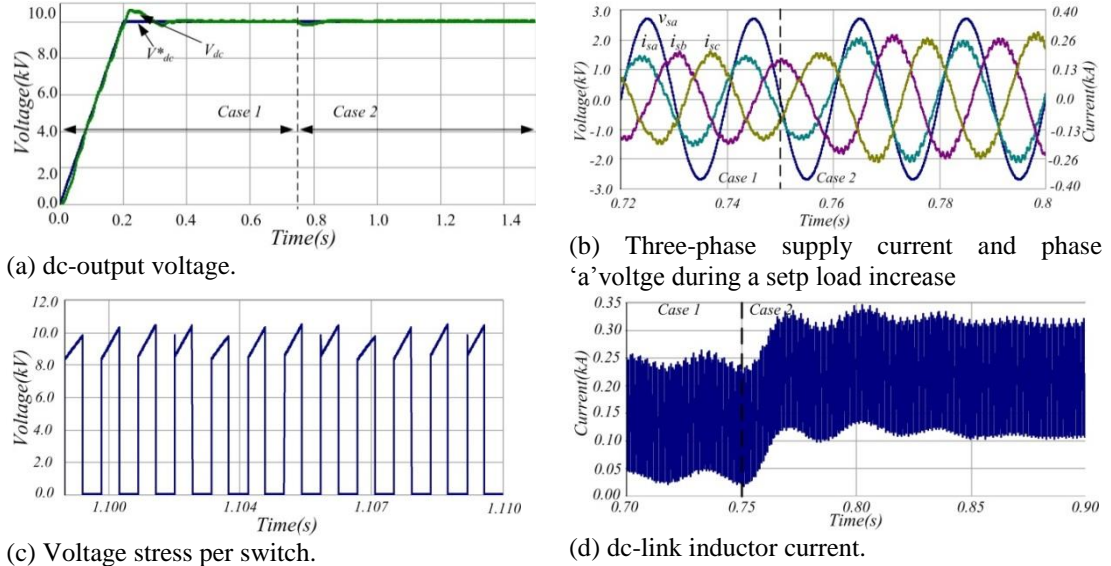


Figure 4.19 Waveforms show the overall performance of the proposed dual three-phase buck-boost converter.

4.5. Three series-connected single-phase buck-boost converters

To further reduce the voltage stresses in the semiconductor devices, the three series connected single-phase buck-boost converter in Figure 4.20(a) is proposed, which uses three single-phase buck-boost modules. The ac terminals of the diode bridge of each phase are connected to three single-phase transformers with isolated secondary windings, while the primary sides can be connected star or delta; however, star connection is shown in Figure 4.20(a). This converter has a reduced voltage stress per active switch (S_1 , S_2 and S_3) and blocking diode (D_{bd1} , D_{bd2} and D_{bd3}): reduce to the line-to-neutral voltage plus $\frac{1}{3}$ the output voltage. The proposed converter in Figure 4.20(a) can operate under continuous or discontinuous dc-link inductance current modes (CCM or DCM). Its operation modes and control strategy in CCM are the same as discussed in section 4.2 for the single-phase version. The output dc voltage for the three-phase buck-boost converter in Figure 4.20(a) is:

$$V_{dc} = 3 \times \frac{\delta}{1-\delta} \times \frac{2V_m}{\pi} \quad (4.67)$$

4.5.1 DCM analysis

For simplicity, the analysis during DCM operation is carried out on a per phase basis, and then extended to the three-phase version. Per phase analysis of the output dc voltage of a single-phase full-bridge diode is adopted.

Assume the switching and supply fundamental frequencies are f_s and f , during the analysis of each switch period the supply voltage is assumed fixed, and the voltage drop in the series elements of the input L-C filter is assumed to be sufficiently small to be neglectable. Figure 4.20(b) shows the single-phase ac-dc buck-boost converter being studied has three operating intervals in DCM:

First interval ($0 < t < t_{on}$): This mode represents the situation when the switch S is on and the dc-link inductance L_{dc} is being energised from the supply, and dc-side capacitor supplies the load with near constant current if its capacitance is sufficiently large. In this interval, the dc-link inductance voltage and current, and dc capacitor current are:

$$v_L(t) = |v_s(t_s)| = |V_m \sin \omega t_s| \quad (4.68)$$

$$\frac{di_L(t)}{dt} = \frac{|V_m \sin \omega t_s|}{L_{dc}} \quad (4.69)$$

$$i_c(t) = -\frac{V_o}{R} \quad (4.70)$$

After solving these equations, $i_L(t)$, in this interval is:

$$i_L(t) = \frac{|V_m \sin \omega t_s|}{L_{dc}} t \quad (4.71)$$

With f_s being selected to be much higher than supply frequency f , (4.71) can be used to approximate the peak inductor current (I_{Lmax}) at the instant when the switch S is turned off (at $t = t_{on} = \delta T_s$).

$$I_{Lmax} = \frac{|V_m \sin \omega t_s|}{L_{dc}} \delta T_s \quad (4.72)$$

Second interval ($t_{on} < t < t_x$): This represents the period when switch S is off and the dc-link inductor supplies the load and charges the dc-side capacitor. The voltage impressed across L_{dc} is equal to the load voltage but with negative polarity as shown in Figure 4.20 (b). Thus, the dc-link inductor voltage and current, and dc capacitor current are:

$$v_L(t) = -V_{dc} \quad (4.73)$$

$$\frac{di_L(t)}{dt} = -\frac{V_{dc}}{L_{dc}} \Rightarrow i_L(t) = -\frac{V_{dc}}{L_{dc}}(t - t_{on}) + I_{Lmax} = -\frac{V_{dc}}{L_{dc}}(t - \delta T_s) + \frac{|V_m \sin \omega t_s|}{L_{dc}} \delta T_s \quad (4.74)$$

$$i_c(t) = i_L(t) - i_o(t) = -\frac{V_{dc}}{L_{dc}}(t - \delta T_s) + \frac{|V_m \sin \omega t_s|}{L_{dc}} \delta T_s - \frac{V_{dc}}{R} \quad (4.75)$$

From Figure 4.20(b), $i_L(t_{on}+t_x)=0$ when the energy stored in the dc link inductor (L_{dc}) is exhausted; thus, t_x is:

$$t_x = \frac{|V_m \sin(\omega t_s)|}{V_o} \delta T_s \quad (4.76)$$

Alternatively, this equation can be obtained by setting the average dc link inductor voltage to zero.

Third interval ($t_{on}+t_x < t \leq T_s$): This interval represents the case when the energy stored in the dc link inductor L_{dc} is exhausted when its current drops to zero at $t=t_{on}+t_x$ before the next switching period and remains at zero. In this interval, inductor current and voltage are $i_L(t)=0$ and $v_L(t)=0$, and dc link capacitor current is:

$$i_c(t) = -i_o = -\frac{V_{dc}}{R} \quad (4.77)$$

Considering the three intervals derived, the average capacitor current during one switching cycle is:

$$\bar{i}_c = \frac{1}{T_s} \left[\int_0^{t_{on}} i_c(t) dt + \int_{t_{on}}^{t_{on}+t_x} i_c(t) dt + \int_{t_{on}+t_x}^{T_s} i_c(t) dt \right] = -\frac{V_{dc}}{R} - \frac{? V_{dc} t_x^2 + V_{dc} t_{on} t_x - V_{dc} \delta T_s t_x - |V_m \sin \omega t_s| \delta T_s t_x}{L_{dc} T_s} \quad (4.78)$$

Since the input current and output dc voltage of a single-phase full-bridge diode rectifier have half wave symmetry ($0 < \omega t < \pi$), the average capacitor current during one half of the supply cycle is:

$$\bar{i}_{c_HC} = \frac{1}{\pi} \int_0^{\pi} \left(-\frac{V_{dc}}{R} - \frac{1}{L_{dc} T_s} \left[V_{dc} t_x^2 + V_{dc} t_{on} t_x - V_{dc} \delta T_s t_x - |V_m \sin \omega t_s| \delta T_s t_x \right] \right) d\omega t_s \quad (4.79)$$

$$\bar{i}_{c_HC} = \frac{T_s V_m^2 \delta^2}{4 L_{dc} V_o} - \frac{V_{dc}}{R} \quad (4.80)$$

The steady state average capacitor current tends to zero; the converter voltage gain is:

$$V_{dc} = \frac{1}{2} \delta V_m \sqrt{\frac{T_s R}{L_{dc}}} \quad (4.81)$$

For a given dc link inductance L_{dc} , the critical duty cycle δ_c that defines the boundary between CCM and DCM can be obtained by setting $t_x = T_{off} = (1 - \delta_c) T_s$ and with $|V_m \sin \omega t_s| = V_m$. From equations (4.76) and (4.81) δ_c is:

$$\delta_c = 1 - 2 \sqrt{\frac{T_s R}{L_{dc}}} \quad (4.82)$$

In each switching period during DCM operation, the equivalent continuous current in switch S and the pre-filter input current are:

$$i_s(t) = \begin{cases} \frac{1}{2L} \delta^2 T_s V_m \sin \omega t, & 0 \leq \omega t \leq \pi \end{cases} \quad (4.83)$$

$$i_r(t) = \begin{cases} \frac{1}{2L} \delta^2 T_s V_m \sin \omega t, & 0 \leq \omega t \leq 2\pi \end{cases} \quad (4.84)$$

Equation (4.83) represents the equivalent continuous current in switch S , and (4.84) represents the fundamental component of the pre-filter input current, which is sinusoidal and in-phase with the supply voltage. Since the switched version of the input current $i_{sr}(t)$ is contained within the envelope of the supply voltage, $i_{sr}(t)$ only contains switching frequency harmonic components and their side bands. This

feature makes the ac-side L-C filter size smaller and simpler to design than the three-phase and the dual three-phase buck-boost converters discussed.

The average and root mean square current stresses in the switch S are:

$$\bar{I}_S = \frac{1}{\pi} \int_0^{\pi} \frac{\delta^2 T_s V_m \sin \omega t}{2L_{dc}} d\omega t = \frac{\delta^2 T_s V_m}{\pi L_{dc}} \quad (4.85)$$

$$I_{S_rms} = \sqrt{\frac{1}{\pi} \int_0^{\pi} \frac{\delta^4 T_s^2 V_m^2 \sin^2 \omega t}{4L_{dc}^2} d\omega t} = \frac{\delta^2 T_s V_m}{2\sqrt{2}L_{dc}} \quad (4.86)$$

The average and root mean square current in each diode of the single-phase bridge are:

$$\bar{I}_D = \frac{1}{2\pi} \int_0^{\pi} \frac{\delta^2 T_s V_m \sin \omega t}{2L_{dc}} d\omega t = \frac{\delta^2 T_s V_m}{2\pi L_{dc}} \quad (4.87)$$

$$I_{D_rms} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} \frac{\delta^4 T_s^2 V_m^2 \sin^2 \omega t}{4L_{dc}^2} d\omega t} = \frac{\delta^2 T_s V_m}{4L_{dc}} \quad (4.88)$$

Since the proposed three-phase buck-boost converter consists of three single phase modules, each phase provides $\frac{1}{3}$ of the output power, the voltage gain of the series connected buck-boost converter and δ_{cr} are:

$$V_{dc} = \frac{3}{2} \delta V_m \sqrt{\frac{T_s R}{3L_{dc}}} \quad (4.89)$$

$$\delta_{cr} = 1 - 2 \sqrt{\frac{T_s R}{3L_{dc}}} \quad (4.90)$$

4.5.2 Control strategy

Figure 4.20(c) summarises the control structure used to control the converter in Figure 4.20(a), which consists of inner and outer control loops. The outer control loop regulates the total output dc voltage V_{dc} , where a PI controller estimates the reference peak fundamental supply current I_p^* to achieve any desired dc link voltage V_{dc} . A current limiter is added in the outer control loop to protect the converter from

over load. The inner loop forces the supply current peak to follow its reference set by the outer loop and estimates the duty cycle δ of switch S .

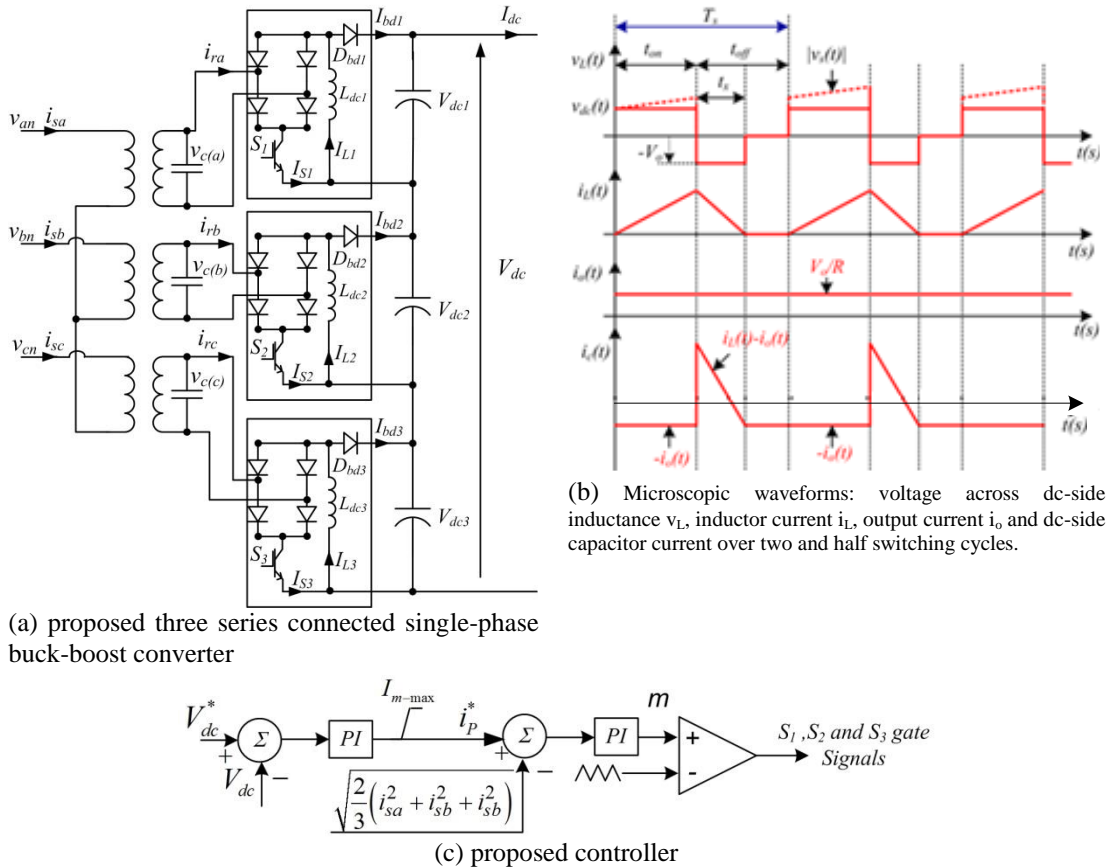


Figure 4.20 Proposed three series connected single-phase buck-boost converter.

4.5.3 Simulation validation

This section presents simulation results from PSCAD/EMTDC models of the proposed three-series single-phase connected buck-boost converter. The simulation section consists of two parts. The first part shows the closed loop results of the proposed converter shown in Figure 4.20(a) under CCM operation and the second part present DCM operation. The converter parameters are listed in Table 4.8. The converter is simulated under the same operating scenario as the scalable three-phase buck-boost converter in subsection 4.3.5.

Table 4.8 Parameters of proposed three series connected single-phase buck-boost converter under CCM and DCM operation

Parameter	CCM operation	DCM operation
Rated power	1MW	1MW
Supply voltage	3.3kV L-L	3.3kV L-L
Supply frequency	50Hz	50Hz
Switching frequency	5kHz	2.4kHz
Transformer rated power	Three single-phase transformers 1.7MVA	Three single-phase transformers 1.7MVA
Transformer rated voltage	Three single-phase transformers 1.9/1.9kV	Three single-phase transformers 1.9/1.9kV
Ac-side C-filter	Three 5 μ F	Three 50 μ F
dc-side inductance	Three 3mH	Three 750 μ H
dc-side capacitance	Three 2200 μ F	Three 2200 μ F

i Three series connected single-phase buck-boost converter under CCM operation

The closed loop results of the converter shown in Figure 4.20(a) under CCM conditions are shown in Figure 4.21. Figure 4.21(a) shows the proposed converter is able to force its dc output voltage to follow the reference voltage in buck and boost modes, including when the load resistance is decreased from 150 Ω to 100 Ω . Figure 4.21(b) shows samples of the three-phase input currents and phase ‘a’ voltage, all zoomed around the instant when the load resistance changes. Figure 4.21(c) shows a sample of the voltage stress across switch S₁, which is comparable to theoretical value stated in section 4.5, due to a small ac-side C-filter (discontinuous input capacitor currents). Figure 4.21(d) shows the dc-side inductor current is continuous as expected and increases when the load resistance is decreased.

ii Three series connected single-phase buck-boost converter under DCM operation

Figure 4.22 shows closed loop operation waveforms of the converter operating under DCM. Figure 4.22(a) shows that it is able to track the reference output voltage, including during a step change in load resistance. This is achieved rapidly and with minimal under-shoot, compared to the CCM case presented in the previous

subsection. From Figure 4.22(b), the supply current is sinusoidal and in phase with the supply voltage. Figure 4.22(c) shows the voltage stress on switch S_1 is in line with the theoretical prediction stated in section 4.5. Figure 4.22 (d) shows a zoomed version of the dc-link inductor current, and the proposed converter is seen to operate on the boundary between CCM and DCM.

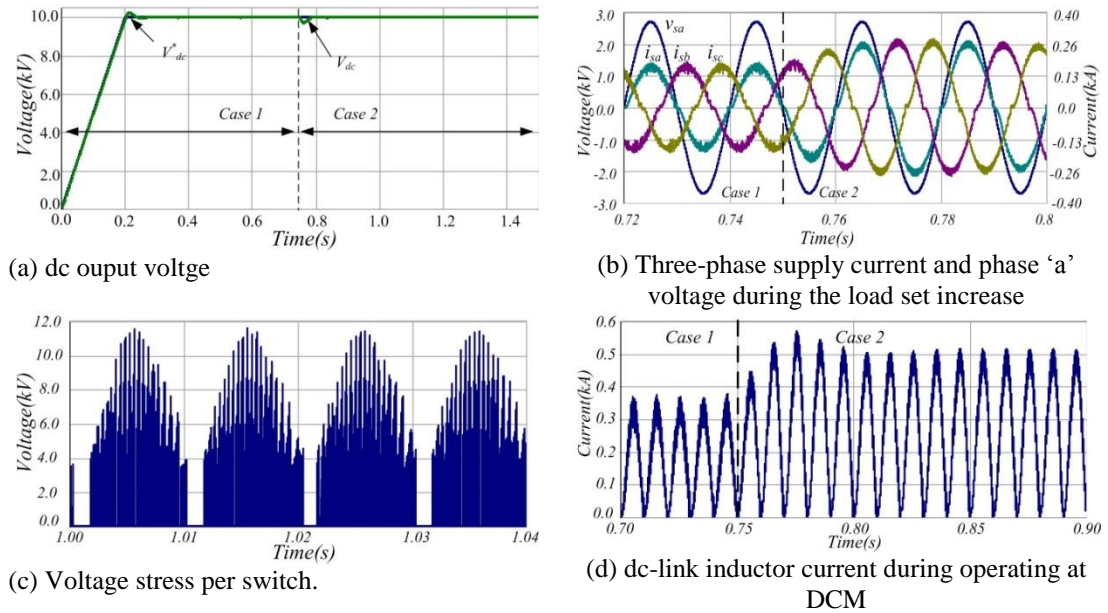


Figure 4.21 Simulations illustrate the performance of the proposed three series connected single phase buck-boost converter under CCM.

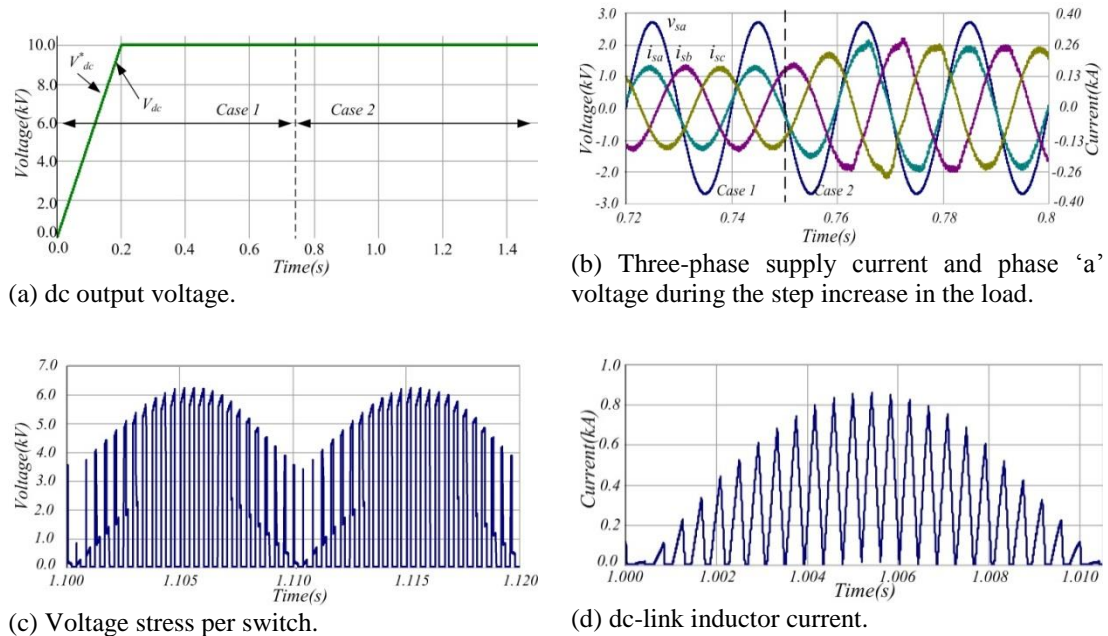


Figure 4.22 Simulation results summarizing the performance of the proposed buck-boost converter under DCM.

4.5.4 Three series connected single-phase buck-boost converter experimental results

The three-series connected single-phase buck-boost converter under DCM operation shares the voltage stress across the active switch. A 1.6kW experimental setup is tested to verify its steady state and dynamic performance under DCM operation, with the system parameters listed in Table 4.1. Figure 4.23 shows the experimental setup. The operating sequence consists of three cases. First case: the reference voltage gradually builds from zero to 330V to provide soft start-up, and the proposed converter feeds a purely resistive load of two series-connected resistors - 70 Ω and 22 Ω . Second case: the load is step increased by short circuiting the 22 Ω resistor by a semiconductor switch. The third case: the load is step decreased by turning off switch.

This operating scenario will show the dynamic performance of the proposed converter and controller. The results are displayed in Figure 4.24 and Figure 4.25. Figure 4.24 (a) shows that the proposal buck-boost converter gradually builds up the output dc voltage to its reference value. Figure 4.24 (a) and (b) show that it overcomes the step load change with minimum transient time and over/under shoot. Figure 4.24(c) and (d) shows that the supply current is sinusoidal with near unity power factor. Figure 4.25 shows that the maximum voltage stresses across the switch is about 250V, as expected from $(100\sqrt{2} + \frac{330}{3} = 251V)$.

Table 4.9 Three series connected single-phase buck-boost converter experimental parameters.

Parameter	Value
Supply voltage	100V _{L-n}
Transformer rated power	2kW
Transformer rated voltage	415/415V _{L-L}
Ac-side capacitance	20 μ F
dc-side inductance	500 μ H
dc-side capacitance	2200 μ F

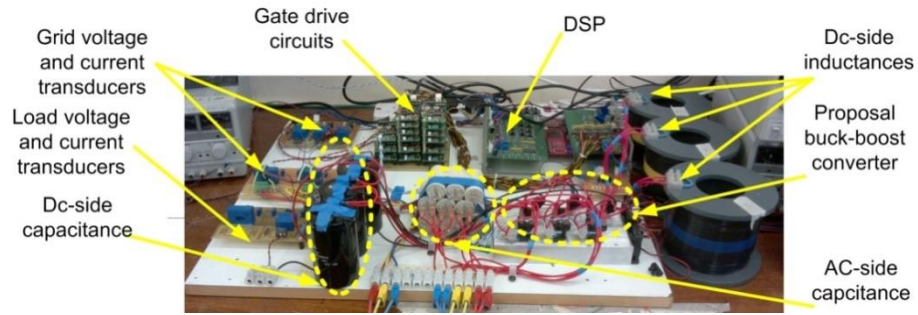


Figure 4.23 Three series connected single-phase buck-boost converter experimental test rig

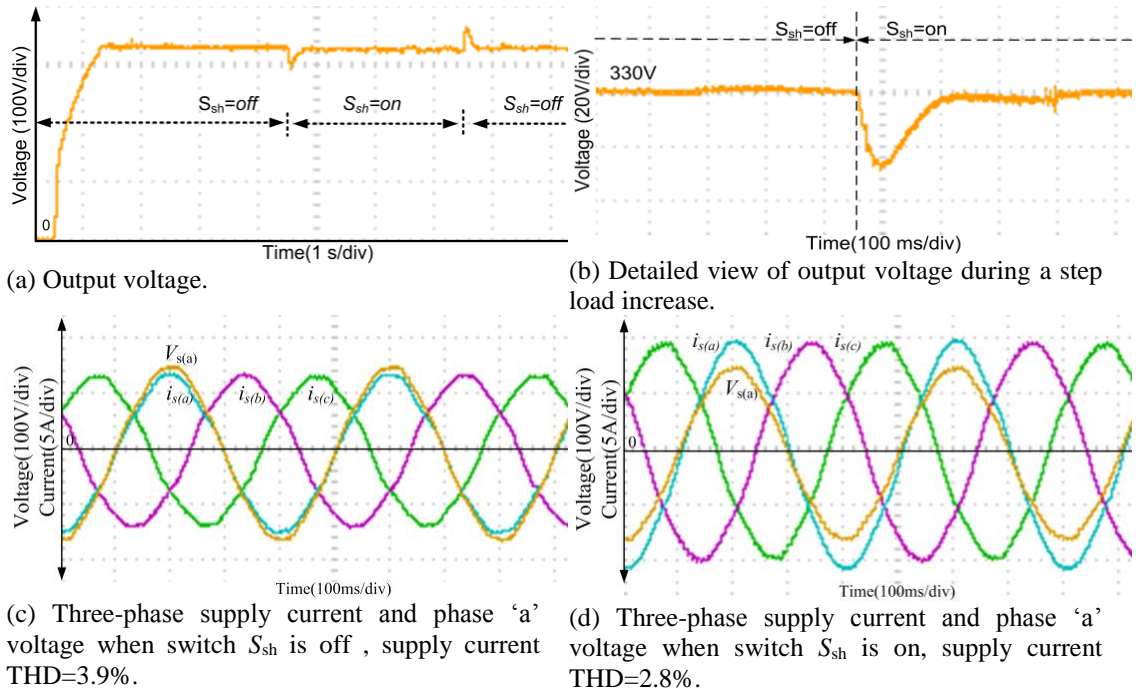


Figure 4.24 Waveforms show the overall performance of the proposed three series connected single-phase buck-boost converter.

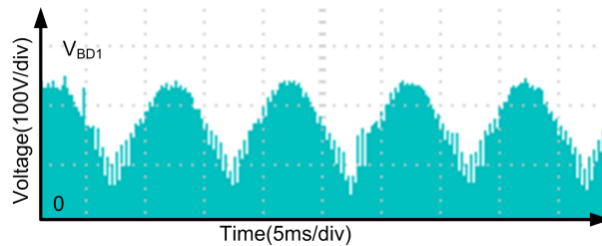


Figure 4.25 Voltage stress per-switch

4.6. Comparison between three-phase buck-boost converter, dual three-phase buck-boost converter, and three series connected single-phase buck-boost converter under DCM

The three series connected single-phase buck-boost converter under DCM has the following advantage over the three-phase and dual-three phase buck-boost converters:

- Fastest dynamic response due to using smaller dc-side inductance and medium size ac-side C-filter, see Figure 4.14(a), Figure 4.19(a), and Figure 4.21(a).
- Sinusoidal current with near unity pf over a wide range of operating conditions. Unlike the three-phase/dual three-phase buck-boost converters in Figure 4.9(a), Figure 4.17 ensures near unity power factor over a limited range according to a pre-defined profile.
- Lower semiconductor voltage stress, but the highest current stress per switch, see Figure 4.14 (c and d), Figure 4.19 (c and d), and Figure 4.21 (c and d).

For the same supply voltage and rated output power, the dual three-phase buck-boost converter has the lowest average dc-link inductor current. This is because their rectified dc output voltages are higher than that of the three-series connected single phase version, by a factor of $\sqrt{2/3}$ higher.

The three-phase buck-boost converter requires the largest ac-side filter, but does not need a transformer (or generator) in the ac-side input unlike the other two converters.

The simulation results in Figure 4.14, Figure 4.19, and Figure 4.21 shows that the proposed buck-boost converters provide high-quality sinusoidal input current with stable dc output voltage. This qualifies the proposed converters for the interfacing of permanent magnetic wind-turbine generators, and as a front-end converter for grid-connected current and voltage source converters, with black-start and shutdown capabilities.

4.6.1 10kW buck-boost converter

Based on the comparison discussed above, the three series connected buck-boost converter was selected to be tested experimentally at 10kW. System parameters are listed in Table 4.10. To demonstrate the soft start and shut-down capability, the output dc link voltage is slowly increased from 0 to 1250V by using a low pass filter (LPF) with cut-off frequency of $\frac{1}{8}s$, and when the shutdown signal received, reduced to zero using a LPF with cut-off frequency of $\frac{1}{2}s$. The results from this test are displayed in Figure 4.27. From Figure 4.27(a) the proposed converter provides a high boost with good dynamic response during soft start up, steady state and shutdown. Figure 4.27 (b) shows the steady state output voltage and the voltage stress across switch S, which is 600V, as expected ($130\sqrt{2} + \frac{1}{3} \times 1250 \approx 600$ V). Figure 4.27 (c) shows that the supply current is sinusoidal with near unity power factor (this is achieved without any dedicated control to force unity power factor operation, as stated previously). The dc-side inductor current (i_L) in Figure 4.27(d) confirms operation in DCM.

Table 4.10 10kW prototype parameters

Parameter	Value
Supply voltage	260V _{L-N}
Transformer rated power	8kVA
Transformer rated voltage	440/220V _{L-L}
ac-side capacitance	80 μ F
dc-side inductance	330 μ H
dc-side capacitance	2200 μ F
Load Resistance	150 Ω

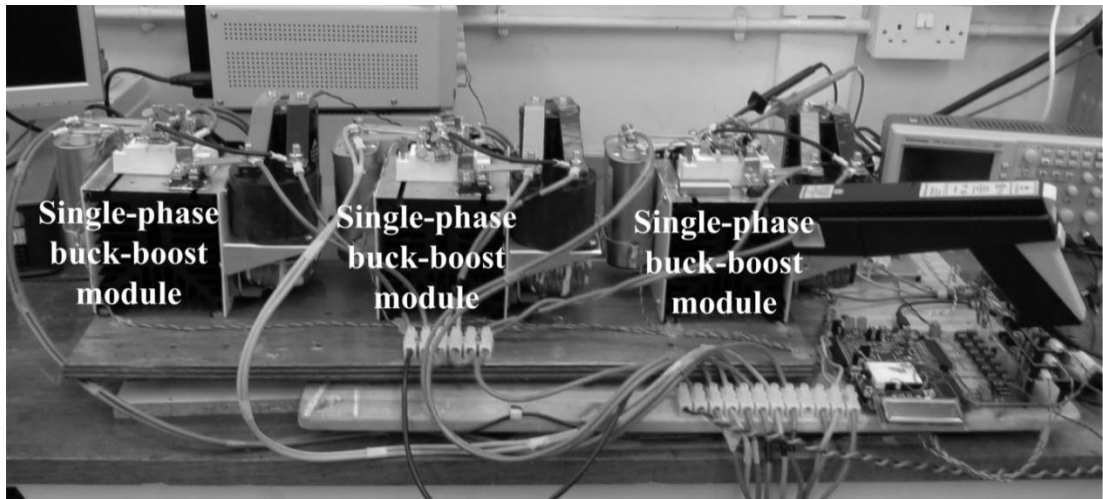


Figure 4.26 10kW experimental test rig

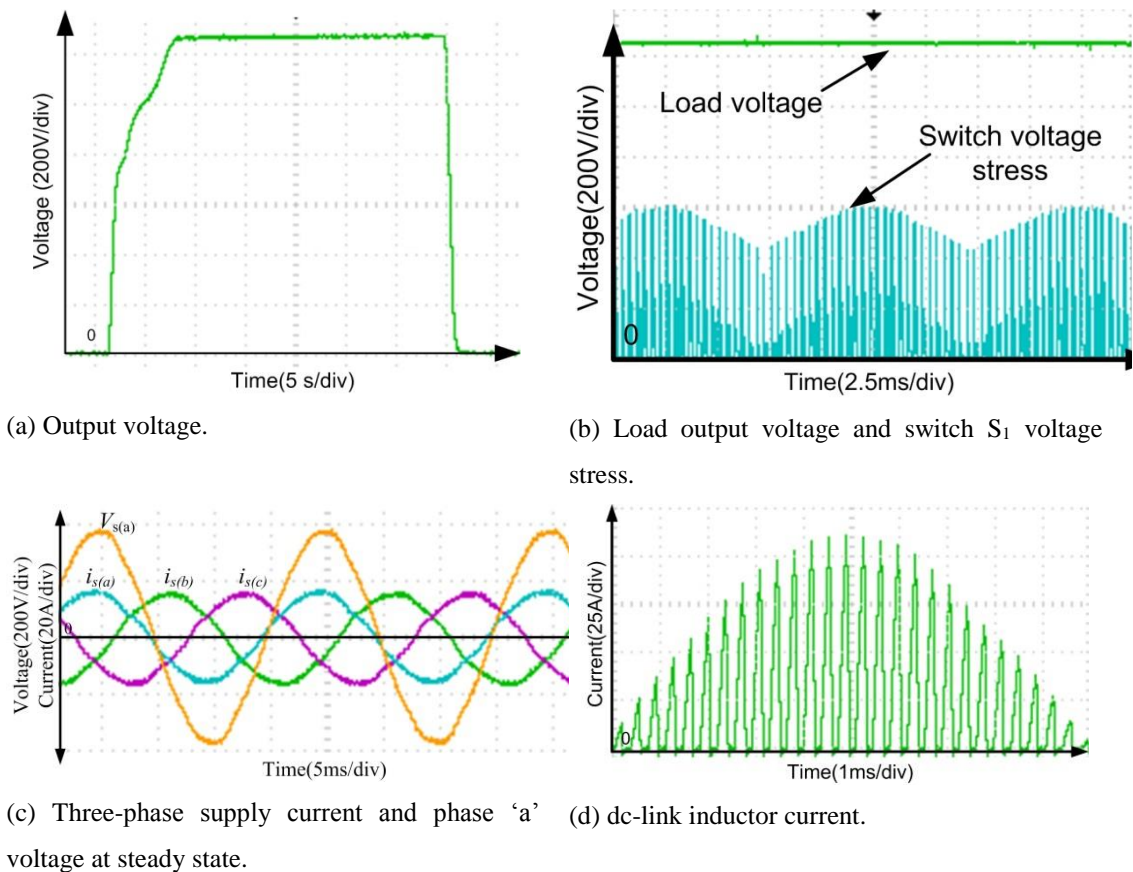


Figure 4.27 Performance waveforms of the 10kW buck-boost converter.

4.7. Generalization of a multi-phase buck-boost converter

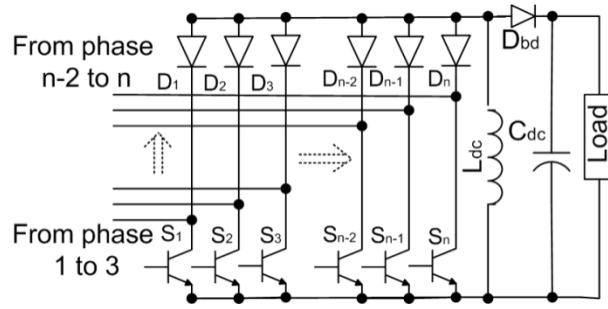
The proposed buck-boost configuration can be generalized for any number of phases, as shown in Figure 4.28(a) for parallel connection. This configuration is suitable for

high current application where a large current is shared between n-phases. The switches and diodes equally share the supply current between phases without any complicated control technique. This configuration is an improved version of the proposed bridgeless buck-boost converter shown in[24].

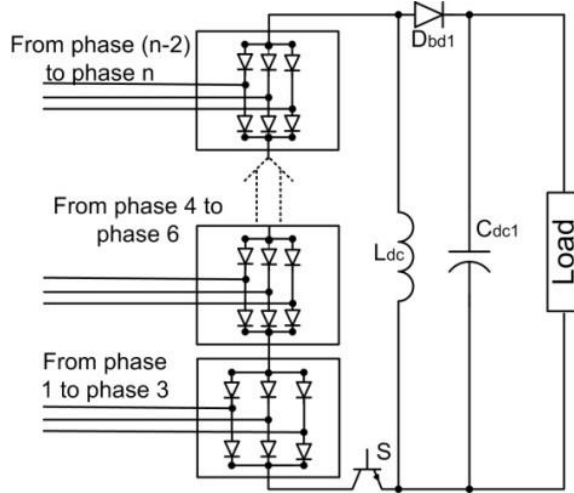
Figure 4.28(b) shows the series configuration of the proposed buck-boost converter, which consists of three-phase rectifier bridges connected in series to ensure that the current is the same in each three-phase. The switch and diode high voltage sharing problem is overcome with the configuration in Figure 4.28(c). In each case, appropriately phase shifted winding sets will eliminate harmonics.

4.8. Summary

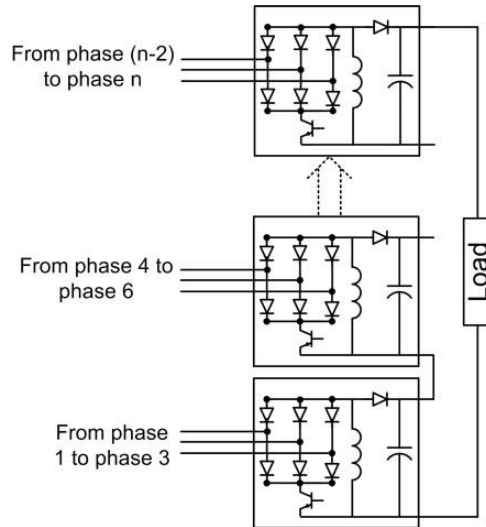
This chapter proposed single-stage, single-phase, three-phase and multi-phase ac-dc buck-boost converters with a minimal switch count. The converters achieve buck and boost operation in a single-stage, with adjustable dc output voltage in both modes, and with soft start/stop. The operating principles were discussed, and mathematical relationships describing steady-state operation were presented for the various buck-boost converters. The control structure for the single-phase version (with sinusoidal input current, nearly unity input power factor and adjustable output dc voltage) was extendable to the three-phase, dual three-phase, and three series connected single-phase ac-dc buck-boost versions. The viability of these buck-boost converters was confirmed by simulations and experimentally. The three-phase and dual three-phase versions of the proposed converter will be used in the following chapters to form modified back to back current source converters for wind energy conversion systems. The simulation and experiments conducted on three series connected single-phase ac-dc buck-boost converter under DCM showed that it had reduced voltage stresses on the blocking diodes and switch S. Also, it has better harmonic performance and input power factor profile from no-load to full-load conditions, than the other topologies. Finally, it was illustrated that the proposed buck-boost configuration can be generalized for any number of phases: parallel connected (for high current loads) and series connected (for higher voltage application).



(a) Parallel generalized configuration.



(b) Series generalized configuration.



(c) Modified series generalized configuration.

Figure 4.28 Parallel and series generalized configuration.

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Chapter 5. New Current Source Based Back to Back Converter

This chapter proposes a new back-to-back (BTB) current source converter (CSC) configuration; which addresses the main drawbacks of conventional BTB CSCs such as the over-voltage frequently experienced by switches during commutation. Additionally, it offers the following advantages: simple and easy control; sinusoidal ac currents with high power factor (PF) at both ac sides with reduced switching frequency; inverter side zero switching losses, and rectifier side soft start-up and soft shutdown. Basic relations that govern its steady-state operation are established for three-phase and dual three-phase versions of the proposed BTB CSC. This configuration comes from integrating the ac-dc buck-boost converter proposed in Chapter four with the current source inverter represented in Chapter three. PSCAD/EMTDC simulations and experimentation are used to demonstrate the practicality of the proposed power conversion systems. It is shown that both versions have good dynamic performance, with near unity input PF on the rectifier side and controllable reactive power on the inverter side. The proposed current source based BTB converter will be using in Chapter seven, as interfacing converter between the wind turbine generators with the grid.

5.1. Background

BTB converters represent the backbone of many power conversion systems. Various topologies have evolved around conventional voltage and current source converters in an attempt to meet different design and reliability constraints [1]. The conventional BTB converter consists of a rectifier side and inverter side, and the two sides are connected via an energy storage element, such as capacitor for a VSC or inductance for a CSC [2]. The VSC based BTB has a faster dynamic response and higher efficiency than the current source BTB converter [3, 4], while the current source BTB arrangement has higher reliability and inherent current limiting during dc faults, as shown in [5-7]. This section considers some BTB converters, which can perform the same functions as the conventional BTB converters.

The BTB converter proposed in [8-10] uses the dc-link midpoint connection and a four-leg converter, to reduce the switch count, and offers bidirectional power flow and power factor control. But the load and grid must have the same frequency.

References [11, 12] propose a nine switch three leg BTB converter, where the middle switch of each leg operates for both the rectifier and the inverter, and the input power transferred to the output is through the middle switches and the dc-side capacitor. This converter is attractive because it has low cost due to a reduced number of switches, plus sinusoidal input current and unity power factor. The converter operates into two modes: fixed frequency with variable output voltage; and variable frequency and variable output voltage. Each mode has its own modulation scheme. The converter gives the same performance as the conventional BTB VSC in the first mode, but when operated in the second mode it has higher total harmonic distortion (THD) and higher losses than a conventional two level BTB converter. Reference [13] uses the same approach in a wind energy conversion system (WECS) to drive a doubly fed induction generator (DFIG).

Reference [14] proposes a novel BTB VSC configuration which removes the dc-link capacitor of the inverter side. There are four diodes in the dc-link: three diodes are connected as a three-phase half-wave uncontrolled diode rectifier, and the fourth diode is connected between the two-level PWM VSC rectifier and the diode rectifier. The inverter is directly connected to the diode rectifier. This BTB configuration uses two rectifiers, the diode rectifier transfers energy from the grid to the inverter and the PWM rectifier transfers energy from the dc-link to the grid. Although this configuration has lower inverter switching losses than the conventional BTB VSC, a dc-link capacitor is still used in the PWM rectifier.

References [15, 16] propose a BTB configuration that uses two full bridge circuits, composed of reverse blocking bidirectional switches (12 switches and 12 diodes per-bridge). The link between the two converters is an ac-link and composed of low reactance rated inductance and capacitance. The supply side converter charges the ac-link by high frequency current pulses and the load side converter discharges the stored energy into the load. The converter is soft switching (switches turn on at zero voltage and turn off is capacitor buffered), can operate bi-directionally, supports any

input or output power factor, but has complicated control. This approach is modified in [17-19] where the number of switches is reduced from 24 to 20, but with the same performance. This configuration uses two ac sides unidirectional bridges (6 switches and 6 diodes per-bridge), and for ac-link current, intermediate crossover switches are added into the dc-side of each bridge.

5.2. Proposed three-phase BTB converter in island mode

Figure 5.1(a) shows the proposed BTB converter system. It consists of a three-phase bridge rectifier and associated ac filters (L_r and C_r) at the source side, and a three-phase CSI with an ac C-filter at the load side. Throughout this chapter, the CSI is assumed to operate with fixed modulation index ($m=1$) for reasons given later. The proposed BTB configuration is superior to the conventional back-to-back current source converter as it has fewer devices in conduction path, thus low on-state loss is expected. Provided diode switching losses are negligible compared those of the IGBTs, switching loss of the front end converter connected to the PMSG, are expected to be low, predominantly in switch S_r . Table 5.1 compares the proposed BTB and the conventional current and voltage source converter schemes.

Table 5.1 Comparison of the proposed back-to-back (BTB) with conventional current and voltage source converter schemes

	Proposed configuration	BTB CSC[20, 21].	BTB VSC[22, 23]
Number of switching devices in conduction path	7 devices, 3 in rectifier side and 4 in inverter side	8 devices, 4 in rectifier side and 4 in inverter side	6 devices, 3 in rectifier side and 3 in inverter side
On-state loss	medium	high	low
Switching loss	Low (dominantly at switch S_r in rectifier side, and zero in the inverter)	high	medium
Controlled start-up and shutdown	Yes	Yes	No, require pre-inserted resistor or other means to charge and dc link capacitor
Bi-directional power flow	No	No, but possible circuit reconfiguration	yes
AC fault ride-through	Yes	yes	yes

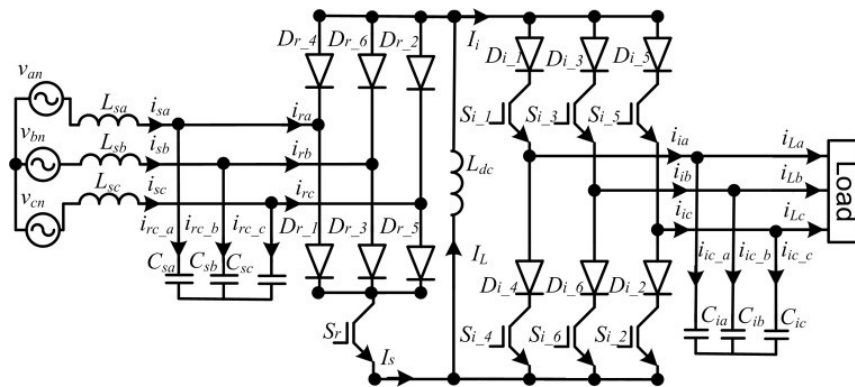
The switching period of switch (S_r) is $T=t_1+t_2$ and is divided into two operating modes. The first mode is the dc-link inductor (L_{dc}) charging mode where the switch (S_r) is on during $0 \leq t \leq t_1$. In this mode, the dc-link inductor current (I_L) rises and is

equal to the switch (S_r) current (I_s), and the input current into the CSI is zero ($I_i=0$) as shown in Figure 5.1(b). The second mode is when the switch (S_r) is off during the period $t_1 \leq t \leq t_2$. In this period, the dc-link inductor current (I_L) falls as the energy stored in this inductor during the first mode is transferred to the load, thus $I_L=I_i$ and $I_s=0$, as shown in Figure 5.1(b). The relationships between the average the dc-link inductor (\bar{I}_L), average switch (S_r) current (\bar{I}_s) and average CSI input current (\bar{I}_i) can summarised as in (5.1) and (5.2).

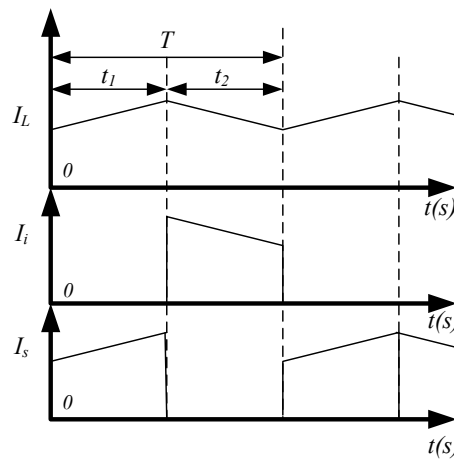
$$\bar{I}_i = (1 - \delta)\bar{I}_L \quad (5.1)$$

$$\bar{I}_s = \delta\bar{I}_L \quad (5.2)$$

where $\delta = t_1/T$ is the switch on-state duty cycle such that $0 \leq \delta \leq 1$.



(a) Proposed BTB converter



(b) dc-link current waveform during one switching cycle

Figure 5.1 Proposed three-phase BTB converter and dc-link current waveforms

5.2.1 Inverter side zero switching current

For minimum switching losses, the grid side CSI in the proposed BTB converter is controlled using selective harmonic elimination (SHE), with three notches per quarter cycle to eliminate the 5th harmonic order [24] where the notch angle is $\Theta=18^\circ$. The switching frequency (f_{sr}) of the switch S_r is 3.0kHz and grid frequency (f_g) is 50Hz. The rectifier chop pulse resolution (SR) represents the relative width in degrees of one switching cycle of S_r in one fundamental period as shown in equation (5.3). For $f_{sr}=3\text{kHz}$ and $f_g=50\text{Hz}$, $SR = 6^\circ$. To ensure zero CSI switching losses, the switching instants of the CSI devices must coincide with zero input dc-link current I_i , which is determined by the modulation of switch S_r ; as will be discussed in the simulation section. Increasing the switching frequency of switch S_r allows SHE to eliminate more low-order harmonics, and decreases the dc-link inductance L_{dc} and C-filters at both ac sides. But this increases the switching losses of S_r . Figure 5.2 shows the inverter output current with one angle to eliminate a single harmonic order.

$$SR = \frac{360f_g}{f_{sr}} \quad (5.3)$$

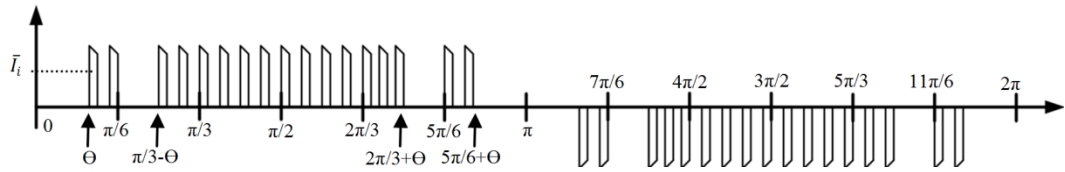


Figure 5.2 Inverter wave form of full cycle with one angle

5.2.2 Circuit analysis

Figure 5.3 shows a simplified representation of the proposed BTB converter. By applying the current divider method to the load side, the relation between per-phase rms fundamental CSI output current ($|i_i|$) and the per-phase fundamental rms load current ($|i_L|$) is:

$$|i_L| = \frac{1}{|1 + j\omega_{op} C_i Z_L|} |i_i| \quad (5.4)$$

Where ω_{op} frequencies in rad/s and Z_L is load impedance.

SHE is used to eliminate the 5th harmonic order from the CSI output current at modulation index 1, the peak fundamental CSI output current equals the average CSI input current ($\bar{I}_1 = \sqrt{2}|i_i|$). From (5.1), equation (5.4) can be rewritten in terms of the dc-link inductance current as:

$$|i_L| = \frac{(1-\delta)\bar{I}_L}{\sqrt{2}|1+j\omega_{op}C_iZ_L|} \quad (5.5)$$

Equation (5.5) shows the relation between the average the dc-link inductor (\bar{I}_L) and the per-phase fundamental rms load current ($|i_L|$).

As described in Chapter four, the peak value of the rectifier input fundamental component ($i_{r,p}$) is:

$$i_{r,p} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \quad (5.6)$$

The rms value of the rectifier input fundamental component ($|i_r|$) is:

$$|i_r| = \sqrt{6} \frac{\delta\bar{I}_L}{\pi} \quad (5.7)$$

Assuming lossless conversion, power balance dictates that power into the converter equals output power:

$$3|i_r||v_{cs}| = 3|i_L|^2 R_L \quad (5.8)$$

Where $|v_{cs}|$ the rms fundamental phase voltage is across the rectifier side capacitors and R_L is per phase load resistance. By substituting equation (5.7) into (5.8).

$$|v_{cs}| = \frac{\pi}{\sqrt{6}\delta\bar{I}_L} |i_L|^2 R_L \quad (5.9)$$

The corresponding rms fundamental supply ($|i_s|$) current can be expressed as:

$$|i_s| = \frac{|v_{cs} - v_n|}{2\pi f_s L_s} \quad (5.10)$$

Where f_s is the supply frequency

5.2.3 Supply side filters design

As discussed in Chapter 4, the rectifier side input filter will have the following values:

$$L_s = 0.53 \frac{V_{LL}^2}{2\pi f P} \quad (5.11)$$

$$C_s = 0.33 \frac{P}{2\pi f V_{LL}^2} \quad (5.12)$$

$$C_s = 0.11 \frac{P}{2\pi f V_{LL}^2} \quad (5.13)$$

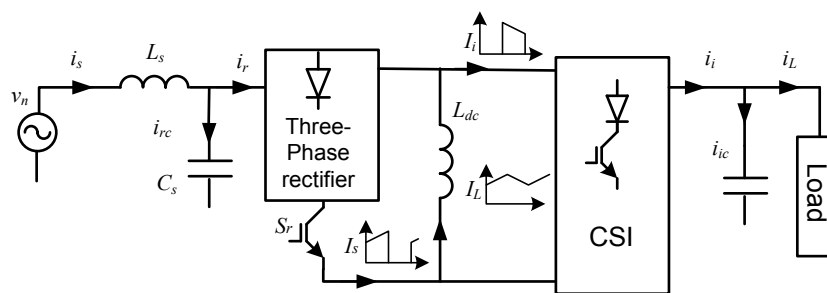


Figure 5.3 Single line diagram representation of the proposed three-phase BTB converter in island mode

Based on simulations and experimentation, with the filter values calculated based on equations (5.11) and (5.12), the input PF profile of the proposed BTB converter varies with input power as shown in Figure 5.4, at S_r switching frequency of 3.0kHz. The input PF is above 0.8 from rated input power to 40% of the rated load.

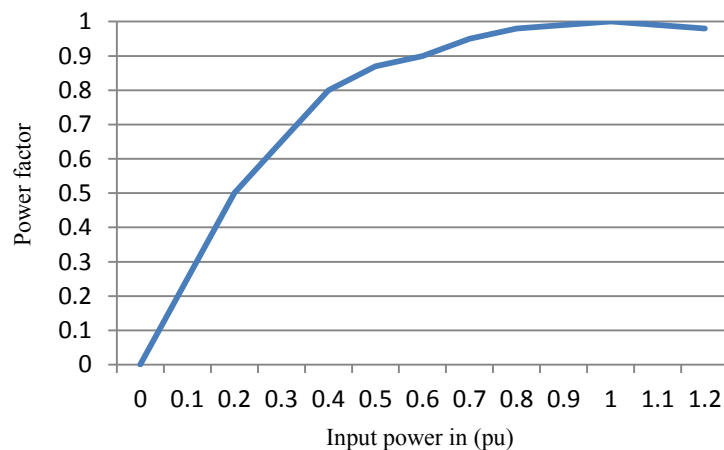


Figure 5.4 Supply current PF profile.

5.2.4 Control strategy

Since the proposed BTB power conversion system supplies an isolated three-phase load; the control strategy in figure 5.5 is adopted for switch S_r . The outer loop regulates the load voltage magnitude and sets the reference average dc link inductor current ($\overline{I_{L_ref}}$). A current limiter stage is used for system protection from over current. The inner current control loop regulates ($\overline{I_L}$) and estimates the modulation index δ for the active switch S_r .

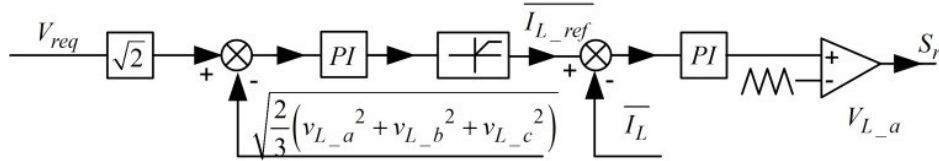


Figure 5.5 Control strategy of the BTB converter in island mode

5.2.5 Simulation results

i. Performance with island load

This section presents simulation results of the proposed BTB with the parameters listed in Table 5.2. For system soft-start-up demonstration, the reference voltage at the load terminal is increased gradually from zero to rated voltage ($R_L=10\Omega$ and $L=4mH$). At time $t=1s$, a step load change is applied by connecting an additional load of (18Ω) to the load bus, to test the dynamic performance. The results obtained are shown in Figure 5.6 and Figure 5.7. Figure 5.6(a) shows that the voltage across the load is maintained constant at 311V peak (220 rms) as the load varies. Figure 5.6(b) shows that as the load increases the dc-link average current and its reference ($\overline{I_{L_ref}}$) increase to maintain power balance between the ac and dc sides. Figure 5.6(c) shows the converter input power, where the step change on the load causes the input power to increase from 15kW (0.75pu) to 23kW (1.15pu). Figure 5.7(a) shows supply currents and phase ‘a’ voltage, as the load varies. The input PF is in line with the theoretical values in Figure 5.4. Figure 5.7(b) shows that the proposed BTB converters gradually build up the load voltage (soft start-up capability). Figure 5.7(c) shows the load current during the load step change, where the proposed BTB converter continues supplying sinusoidal current to the load

Table 5.2 Simulation setup parameters of the proposed three-phase BTB converter in island mode.

Parameter	Value
Rated input power	20kW
Supply voltage	208V L L
Supply frequency	60Hz
Rectifier side L-filter	3mH
Rectifier side C-filter	130 μ F(Δ connection)
dc-link inductance	5mH
Output frequency	50Hz
Inverter side C-filter	130 μ F(Δ connection)
Load resistance	10 Ω
Load inductance	4mH

ii. Zero switching losses consideration

The CSI of the proposed BTB has zero switching losses if the CSI changes its switching states during the dc-link inductance charging mode. This requirement restricts the ratio of the switching frequency of switch S_r to grid frequency, to be an integer multiple of 3 (in other words, integer number of pulses per 120°). This requires synchronization of the high frequency triangle carrier signal to the supply fundamental frequency.

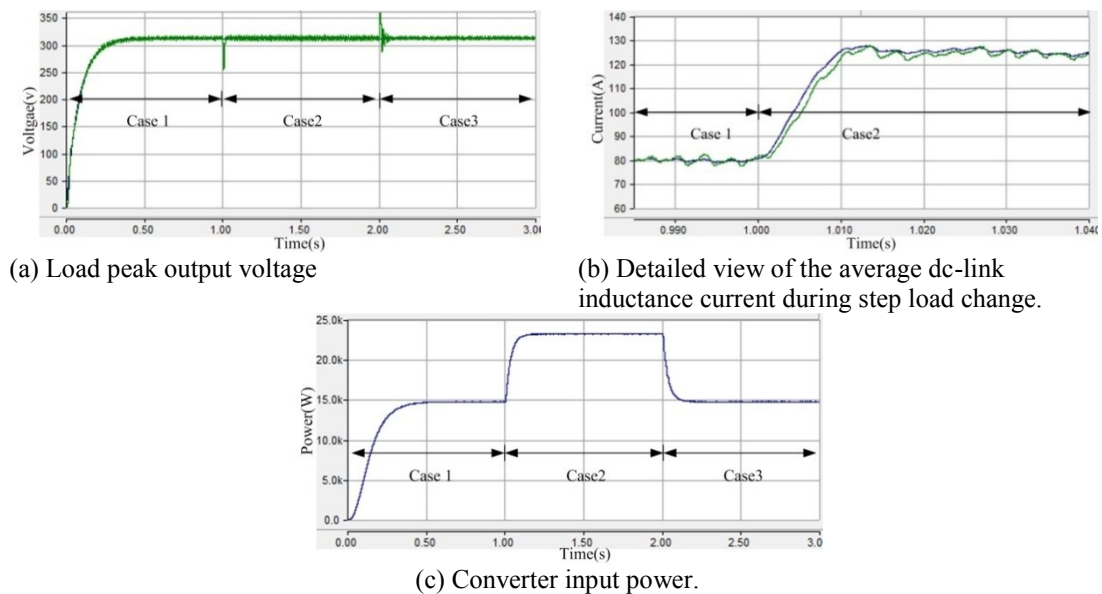
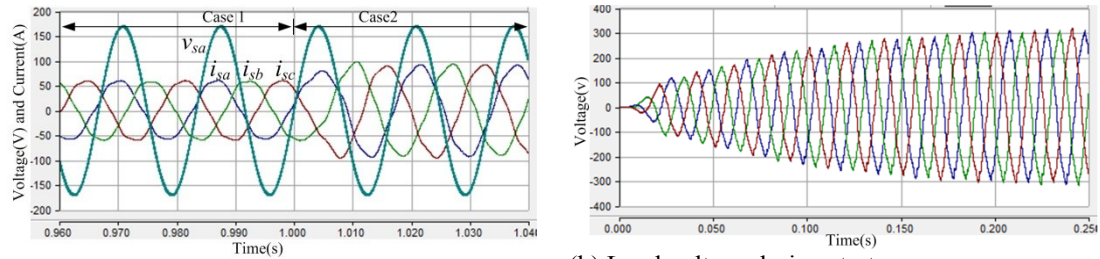
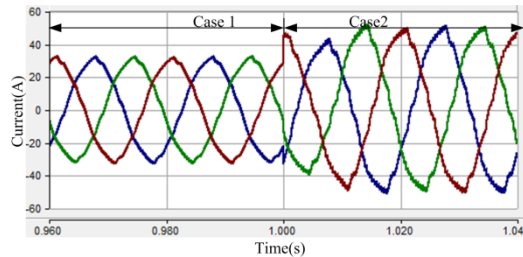


Figure 5.6 PSCAD simulation waveforms for the three-phase BTB converter in island mode



(a) Supply current during the step increase on the load. (b) Load voltage during start-up.



(c) Load current during the step increase on the load.

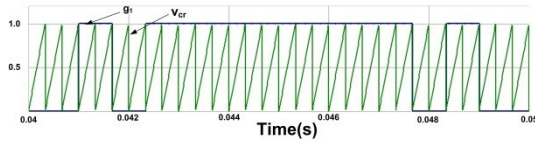
Figure 5.7 PSCAD simulation detail view of the two ac sides of the three-phase BTB converter in island mode

For example if SHE is used to eliminate the 5th harmonics order, only one notch angle is required ($\theta=18^\circ$). Considering the upper switch of phase ‘a’ S_{i_1} . (Due to the symmetrical nature of the CSI gates signals, all the other switches operate similarly). S_{i_1} turns on three times every fundamental cycle ($18^\circ \leq \omega t \leq 30^\circ$, $42^\circ \leq \omega t \leq 138^\circ$ and $150^\circ \leq \omega t \leq 162^\circ$); where ωt is the fundamental angle of the CSI as shown in Figure 5.2. The width of the first pulse is 12° . If switch S_r is turned on twice during the first pulse, this means that the switch resolution SR will be at least 6° , and then from equation(5.3), the minimum switching frequency is 3kHz. Figure 5.8(a) shows switch S_{i_1} gate signal (g_1) and S_r PWM high frequency triangle carrier signal (v_{cr}). Consider the first g_1 pulse, there are two carrier signal cycles (v_{cr}) during the first pulse, and the first carrier signal starts when the gate signal g_1 starts or changes its state from zero to one. Similarly when the gate signal ends or changes its state from one to zero, the second carrier signal ends. This means that both the gate signal and the carrier signal are synchronized and the CSI changes its switch state at zero current (zero switching losses). During grid connection, an angle α is added to ωt that allows the CSI to compensate the ac side capacitor filter current and helps it adjust the reactive power. Figure 5.8(b) shows switch S_{i_1} gate signal (g_1) and S_r PWM high frequency triangle carrier signal (v_{cr}) where $\alpha=-20^\circ$. The S_{i_1} gate signal is now better synchronized (the zero switching loss feature is no longer valid). To solve this issue, the carrier signal must be synchronised, by adding a shift angle α_2 with respect to the

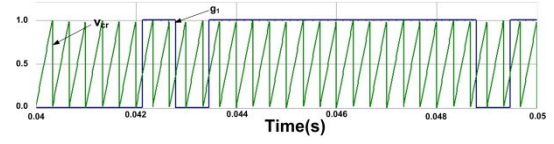
carrier frequency ωt_{cr} . Equation (5.14) is used to derive the equivalent shift value α_2 to compensate the change in α . Figure 5.8(c) and (d) show the switch S_{i_1} gate signal (g_1) and S_r PWM high frequency triangle carrier signal (v_{cr}) when $\alpha=-20^\circ$ and $\alpha=20^\circ$ respectively after applying the proposed carrier gate synchronization technique, it can be observed that the gate signal and the high frequency triangle carrier signal are now synchronized.

$$\alpha_2 = \left(\frac{\alpha f_{sr}}{f_g} - \left| \frac{\alpha f_{sr}}{f_g} \right| \right) \quad (5.14)$$

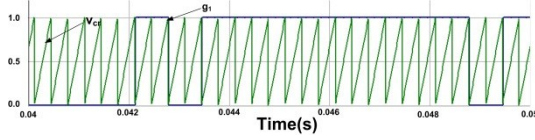
To analyse the performance of the proposal BTB converter and show that zero current switching can be achieved, Figure 5.9 show a detailed view of one CSI fundamental output cycle when SHE is used to eliminate the 5th harmonics order. From Figure 5.9(a), the CSI has pulsating current, and Figure 5.9(b) and (c) show the switch S_{i_1} current (i_{s1}), gate signal (g_1), switch S_{i_2} current (i_{s4}) and gate signal (g_4). S_{i_1} and S_{i_4} change switch states at zero current ($I_i=0$). Figure 5.9 (d) shows the CSI output current. Figure 5.10 results in the same conclusions when SHE is used to eliminate the 5th and 7th harmonics order. Two notch angles θ_1 and θ_2 are introduced, which gives two degrees of freedom to eliminate the 5th and the 7th harmonic orders. From [24], the two notch angles θ_1 and θ_2 will be 7.93° and 13.75° respectively. Switch S_{i_1} turns five times every fundamental cycle ($7.93^\circ \leq \omega t \leq 13.75^\circ$, $30^\circ \leq \omega t \leq 46.25^\circ$ and $52.07^\circ \leq \omega t \leq 127.93^\circ$; $133.75^\circ \leq \omega t \leq 150^\circ$ and $166.25^\circ \leq \omega t \leq 172.07^\circ$). The first and the last pulses have the smallest pulse width (5.82) and it is required that each have at least one pulse. From equation (5.3), switch S_r frequency is 3.3kHz. The results in Figure 5.10 (b) and (c) show that the proposal BTB converter with this switching frequency has zero switching current, with at least one pulse in the smallest pulse width period.



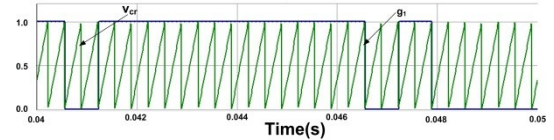
(a) g_1 and triangle carrier signal at $\alpha=0.0^\circ$ without synchronization.



(b) g_1 and triangle carrier signal at $\alpha=-20.0^\circ$ without synchronization.



(c) g_1 and triangle carrier signal at $\alpha=-20.0^\circ$ with synchronization.



(b) g_1 and triangle carrier signal at $\alpha=20.0^\circ$ with synchronization.

Figure 5.8 Waveforms of switch S_{i-1} gate (g_1) synchronisation with switch S_r PWM high frequency triangle carrier signal (v_{cr})

Figure 5.11(a) shows switch S_{i-1} current i_{s1} and gate 1 when SHE eliminates the 11th and 13th harmonic orders. The two notches angle θ_1 and θ_2 are 19° and 21.74° respective. The smallest pulse width is 2.74° , whence from equation (5.3), switch S_r frequency is 6.6 kHz. In Figure 5.11(a), switch S_{i-1} changes its state at zero current. Figure 5.11(b) shows S_{i-1} current and gate signal when SHE eliminates the 5th, 7th, 11th and 13th harmonic orders, which requires four notch angles ($\theta_1=0^\circ$, $\theta_2=1.6^\circ$, $\theta_3=15.14^\circ$ and $\theta_4=20.26^\circ$). Similarly, the smallest pulse width is 1.6° and a suitable switching frequency is 12 kHz. Figure 5.11(b) shows that the proposed BTB converter has zero switching current.

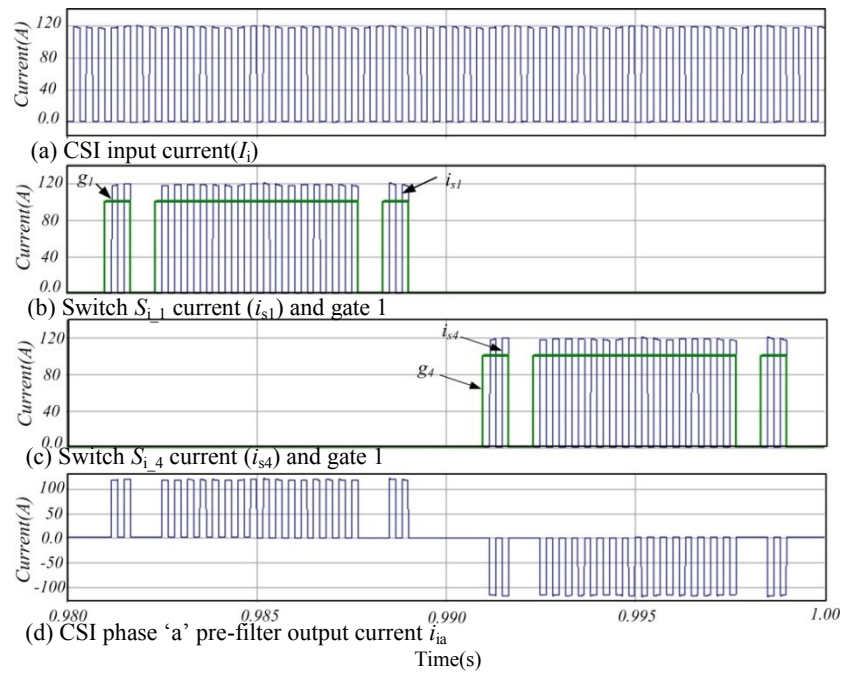


Figure 5.9 Waveforms of the proposed BTB converter with the high frequency carrier signal synchronization technique when SHE eliminates the 5th harmonic order.

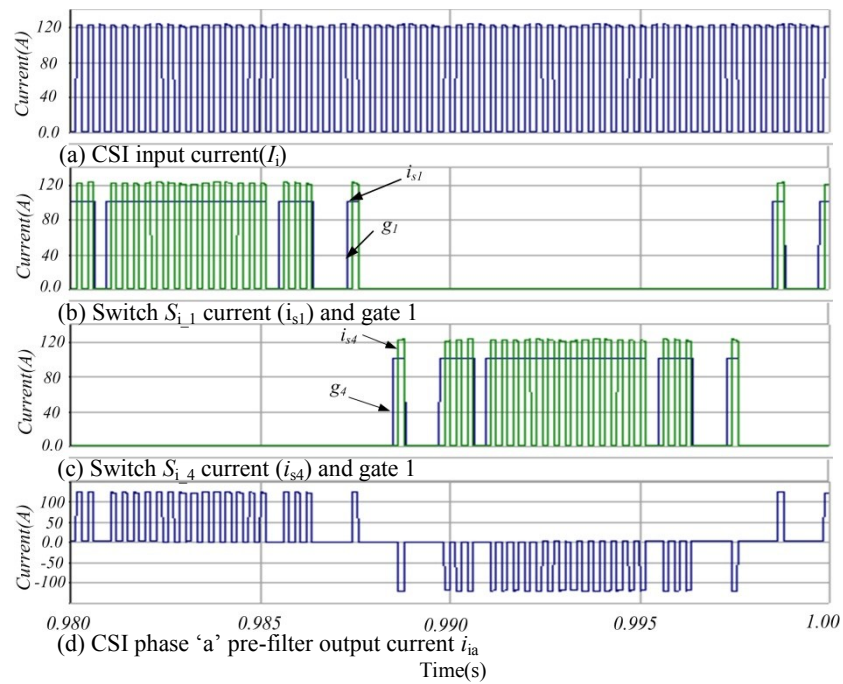
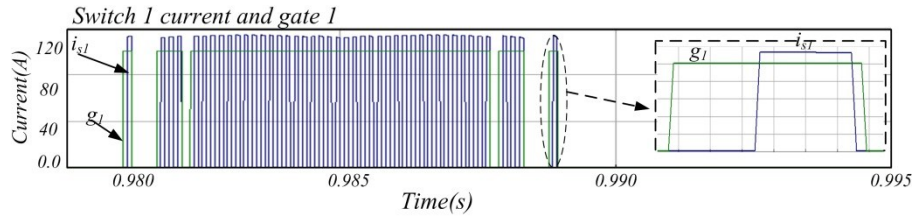
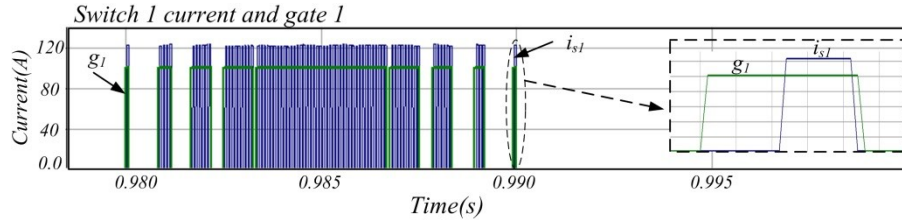


Figure 5.10 The high frequency carrier signal synchronization technique when SHE eliminates the 5th and 7th harmonic orders.



(a) Switch S_{i_1} gate signal and S_{i_1} current when SHE is used to eliminate 11th and 13th harmonic order.



(b) Switch S_{i_1} gate signal and S_{i_1} current when SHE is used to eliminate 5th, 7th, 11th and 13th harmonic order.

Figure 5.11 CSI switch current and its gate signal when SHE eliminates 11th and 13th and 5th, 7th, 11th and 13th harmonic orders.

5.2.6 Experimental results

i. Experimental validation of the zero switching losses

This section emulates the high frequency carrier signal synchronization technique performance, by analysing the expected switch currents and the expected CSI input/output current. This is to ensure that the digital signal processor (DSP) code is functioning correctly before powering the proposed BTB converter.

Figure 5.12 shows results when SHE eliminates the 5th harmonic order. A NOT gate (at the measurement signal level) is added to CSI input current. Figure 5.12(a) and (b) shows S_{i_1} and the NOT S_r gate signal which represents the CSI input current. In Figure 5.12(a) and (b) the CSI changes its switch state at zero current. The expected switch current (i_{Si_r} and i_{Si_4}) and the expected phase 'a' output current are shown in Figure 5.12(c). The expected switch current is the output of an AND gate, with input the CSI switch gate signal and the expected CSI input current. The expected CSI per-phase output current is obtained by subtracting the expected upper switch current from that of the lower switch. Figure 5.12(c) show the fast Fourier transformation (FFT) of the expected CSI output current, where the 5th harmonics are eliminated.

Figure 5.13 shows results when SHE eliminates the 5th and 7th harmonic orders. Figure 5.13(a) shows S_{i_1} gate signal and the expected CSI input current. The CSI is turned on five times to eliminate the two harmonic orders. Figure 5.13(b) is a zoomed version of Figure 5.13(a) showing that the CSI changes switch state at zero current. The expected S_{i_1} and S_{i_2} current and expected CSI phase 'a' output current are in Figure 5.13(c). Figure 5.13(d) shows the FFT of the expected CSI phase output current, where the 5th and 7th harmonic orders are reduced but not eliminated (5th is $\approx 0.8\%$ of fundamental and the 7th is $\approx 0.45\%$ of the fundamental). This is due to the DSP resolution, since the PSD controller interrupt rate is 18kHz and the grid frequency is 50Hz, as discussed in section 5.2.1. The DSP resolution is 1°. To eliminate the 5th and the 7th harmonic orders, the two notch angles θ_1 and θ_2 equals 7.93° and 13.75° respectively. But the DSP places these at 8° and 14° respectively.

The results in Figure 5.12 and Figure 5.13 shows that the proposed high frequency carrier signal synchronization technique works, and ensures zero switching losses. Also the FFT analysis of the expected CSI output current shows that the CSI eliminates the selected harmonic orders.

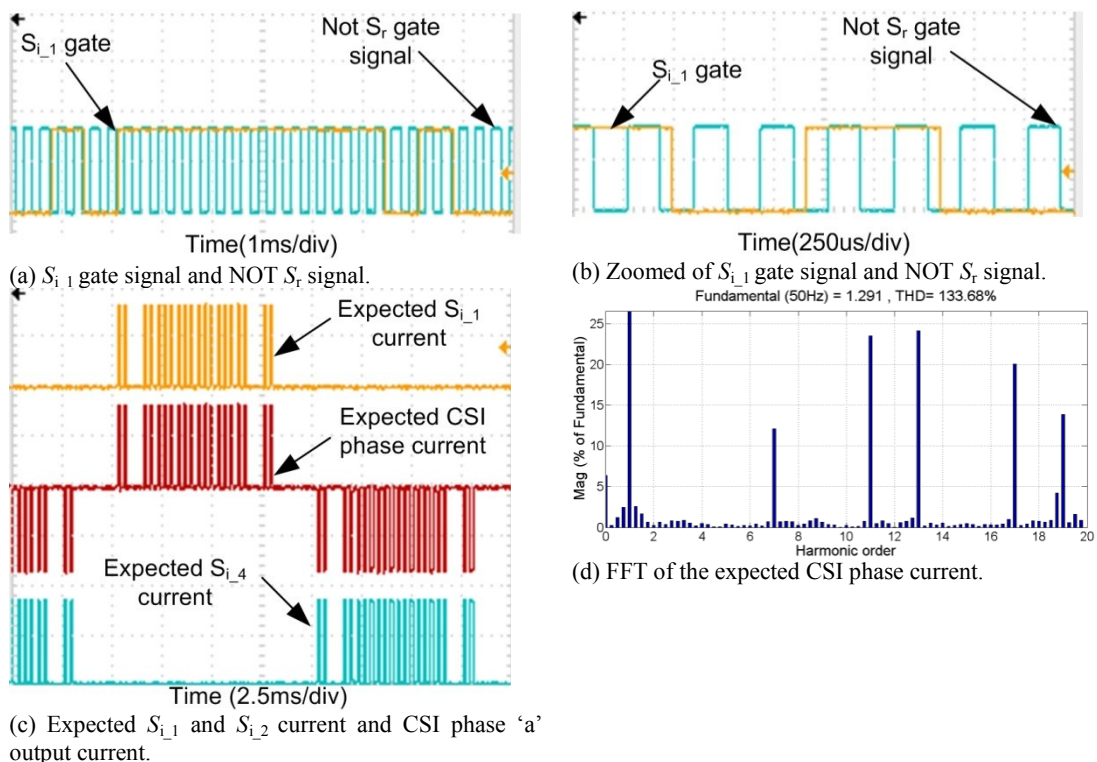


Figure 5.12 Experimental results with the high frequency carrier signal synchronization technique when SHE eliminates the 5th harmonic order.

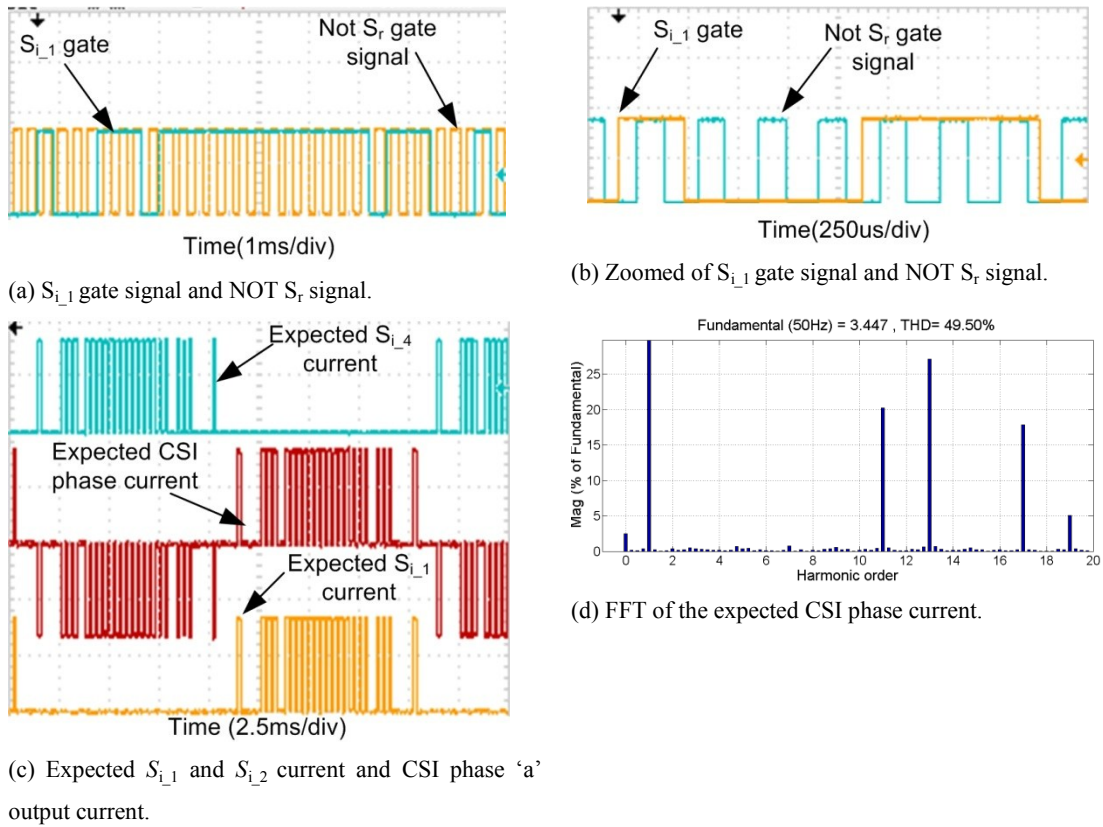


Figure 5.13 Experimental results with the high frequency carrier signal synchronization technique when SHE eliminates the 5th and 7th harmonic orders.

ii. Experimental results at island load

This section presents experimental results from the scaled down test rig of the proposed BTB, with the parameters listed in Table 5.3. The rated input power 850W. The reference output voltage is changed to initiate a step change in load. To provide soft start-up and soft change, the reference voltage is low pass filtered (3 Hz cut-off frequency). Initially the reference output voltage is set to 75V peak then increased to 90V peak, during which periods the input power monitored were 380W and 840W respectively. The experimental results in Figure 5.10 show converter overall performance. Figure 5.10(a) shows the load voltage builds up gradually during a black-start (soft start-up). Figure 5.10(b) shows the load voltage increases gradually without oscillation when the reference peak voltage changes from 75V to 90V. Figure 5.10(c) shows dc-link inductance current I_L , switch current I_S , and CSI dc input current I_i , at 8m/s wind speed. The dc-link inductance current I_L equals the switch current when switch S_r in on and equals the CSI input current I_i when off. Figure 5.10(d) shows the experimental waveform of the CSI output current i_i is

similar to the current waveform shown in Figure 5.2 and Figure 5.9. Figure 5.13 show a detail view of the three-phase load current and voltage during stage 1 and stage 2. From Figure 5.13 the proposed BTB converter supplies the load with sinusoidal voltage and current. The supply voltage and current are shown in Figure 5.14. Figure 5.14(a) and (b) show that the supply currents are sinusoidal and the PF has changed from 0.8 leading to unity.

Table 5.3: Experimental setup parameters of the proposed three-phase BTB converter in island mode

Parameter	Value
Rated input power	840W
Supply voltage	50V L-L
Supply frequency	50Hz
Rectifier side L-filter	5mH
Rectifier side C-filter	120 μ F(Δ connection)
dc-link inductance	5mH
Output frequency	50Hz
Inverter side C-filter	90 μ F(Δ connection)
Load resistance	25 Ω
Load inductance	3.3mH

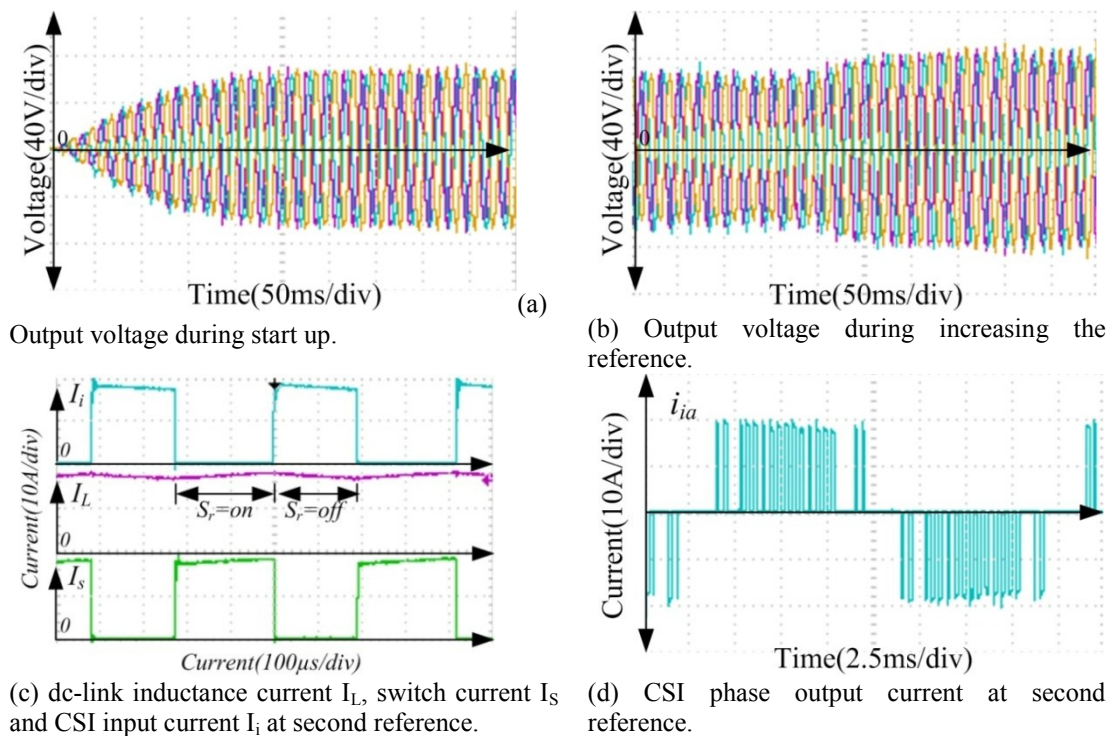
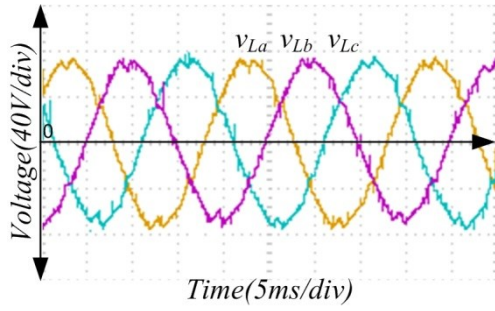
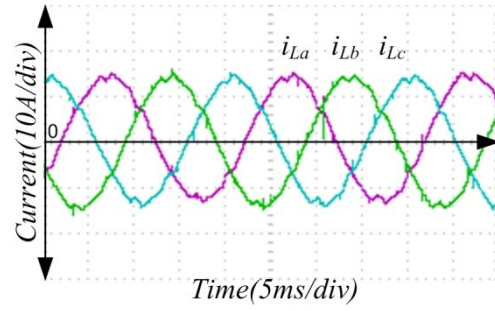


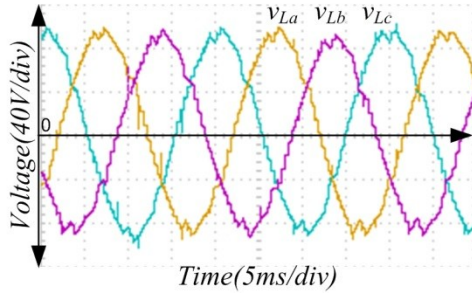
Figure 5.14 Waveforms showing the overall performance of the proposed three-phase BTB converter in island mode



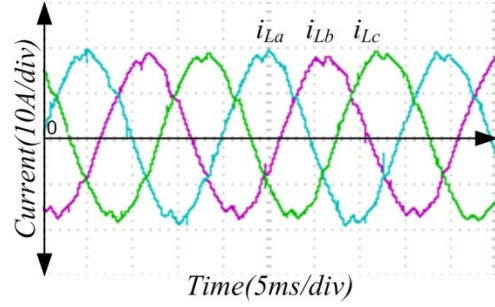
(a) Detailed view of the three-phase output voltage at stage 1.



(b) Detailed view of the three-phase output current at stage 1.

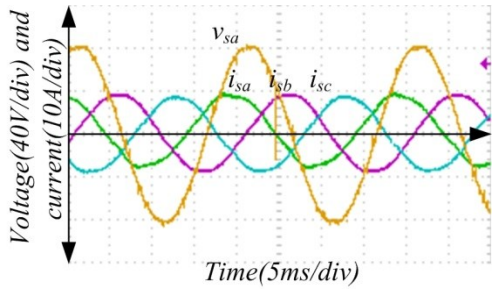


(c) Detailed view of the three-phase output voltage at stage 2.

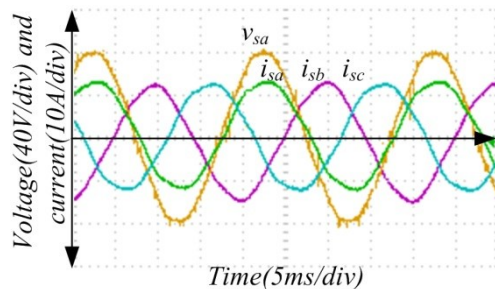


(d) Detailed view of the three-phase output current at stage 2.

Figure 5.15 Detailed view of the three-phase output voltage and currents and phase-a voltage at first and second reference output voltage of the proposed three-phase BTB converter during island mode



(a) Detailed view of the three-phase supply currents and phase-a voltage at first reference output voltage



(b) Detailed view of the three-phase supply currents and phase-a voltage at second reference output voltage

Figure 5.16 Waveforms of the three-phase supply currents and phase-a voltage at first and second reference output voltage of the proposed three-phase BTB converter during island mode

5.3. Proposed three-phase BTB converter in grid connection mode

This section shows the proposed BTB converter performance during the grid connection mode, where the controller controls the grid delivered active and reactive power. To establish the relationship between the powers delivered to the grid and the dc-link inductance current \bar{I}_L , the grid delivered active and reactive powers (P_g) and (Q_g) are expressed as:

$$P_g = \frac{3}{2} i_{s(d)} v_{s(d)} \quad (5.15)$$

$$Q_g = \frac{3}{2} i_{g(q)} v_{g(d)} \quad (5.16)$$

Where $v_{s(d)}$ is the d component of the grid voltage (V_g), assuming the grid voltage vector is aligned with the d-axis ($v_{g(q)}=0$); and $i_{g(d)}$, $i_{g(q)}$ are d and q current components that the current grid side converter injects into grid (i_g).

Based on the single line diagram representation in Figure 5.17, the equations that describe the ac side of the grid side converter are:

$$i_i = C_i \frac{dv_{ci}}{dt} + i_g \quad (5.17)$$

$$v_{ci} = L_g \frac{di_g}{dt} + v_g \quad (5.18)$$

Where v_{ci} is the voltage across CSI grid side C-filter, and L_g is the isolation transformer leakage inductance.

Equations (5.17) and (5.18) can be rewritten in the dq frame as:

$$i_{i(d)} = C_i \frac{dv_{ci(d)}}{dt} - \omega_g C_i v_{ci(q)} + i_{g(d)} \quad (5.19)$$

$$i_{i(q)} = C_i \frac{dv_{ci(q)}}{dt} + \omega_g C_i v_{ci(d)} + i_{g(q)} \quad (5.20)$$

$$v_{ci(d)} = L_g \frac{di_{g(d)}}{dt} - \omega_g L_g i_{g(q)} + v_{g(d)} \quad (5.21)$$

$$v_{ci(q)} = L_g \frac{di_{g(q)}}{dt} + \omega_g L_g i_{g(d)} \quad (5.22)$$

At steady state the CSI output $i_{i(d)}$ and $i_{i(q)}$ can be written as:

$$i_{i(d)} = i_{g(d)} (1 - \omega_g^2 C_i L_g) \quad (5.23)$$

$$i_{i(q)} = i_{g(q)} (1 - \omega_g^2 C_i L_g) + \omega_g C_i v_{g(d)} \quad (5.24)$$

$$\bar{I}_i = \sqrt{\left(i_{g(d)}(1 - \omega_g^2 C_i L_g)\right)^2 + \left(i_{g(q)}(1 - \omega_g^2 C_i L_g) + \omega_g C_i v_{g(d)}\right)^2} \quad (5.25)$$

$$\bar{I}_L = \frac{1}{(1 - \delta)} \sqrt{\left(\frac{P_g}{\frac{3}{2} v_{g(d)}}(1 - \omega_g^2 C_i L_g)\right)^2 + \left(\frac{Q_g}{\frac{3}{2} v_{g(d)}}(1 - \omega_g^2 C_i L_g) + \omega_g C_i v_{g(d)}\right)^2} \quad (5.26)$$

$$\alpha = \tan^{-1} \left(\frac{Q_g + \frac{3}{2} \omega_g C_i v_{g(d)}}{P_g} \right) \quad (5.27)$$

Equations (5.26) and (5.27) shows that the grid delivered active and reactive power can be controlled by regulating the dc-link inductance current and the CSI shift-angle α .

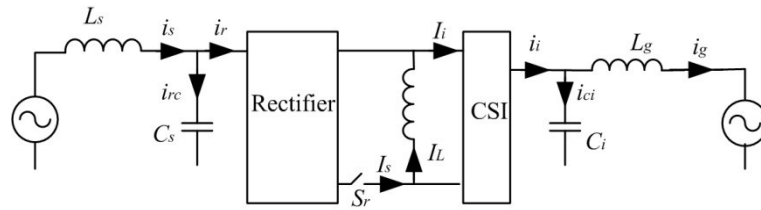


Figure 5.17 Single line diagram of the proposed three-phase grid connected BTB converter

5.3.1 Control strategy

Figure 5.18 shows the proposed controller, which consists of two independent controllers; one for the grid delivered active power and the other for grid reactive power. In the grid active power controller, the outer control loop uses a PI controller to estimate the reference average dc-link inductance current $\bar{I}_{L,ref}$, from the error between the reference active power (P_{ref}) and grid deliver power (P_g). The inner control loop detects the error between the reference dc-link inductance current and the actual average inductance current, which passes through a PI controller to estimate switch (S_r) modulation index δ .

The reactive power controller in Figure 5.18 is used to adjust the phase angle (α) between the grid voltage and current vector. The CSI injects into the grid based on the reactive power demand set point (Q_{ref}). Therefore, the required phase angle (α) for arbitrary reactive power is estimated using PI. The estimated phase angle (α) is

added to angle ωt , which is obtained from the phase locked loop (PLL), and the resultant angle $\omega t + \alpha$ is used to provide the time base for the SHE algorithm.

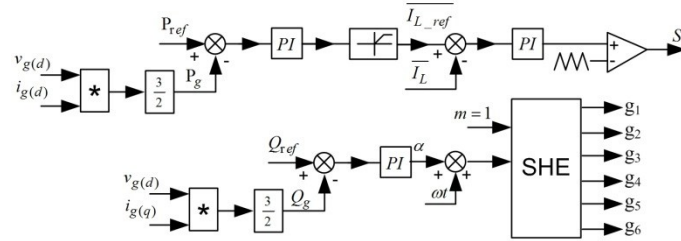


Figure 5.18 Proposed controller for the grid connected three-phase BTB converter.

5.3.2 Simulation results

In this section converter performance is assessed using PSCAD/EMDCT, and the simulation section consists of two parts: the first part tests the performance of the active power controller while setting the reference reactive power to zero, the second part keeps the reference delivered active power fixed and changes the reference reactive power. The system parameters are given in Table 5.4.

Table 5.4 Simulation parameters of the three-phase BTB converter during grid connected mode

	Value
Rectifier side parameter	
Supply voltage	208V L L
Supply frequency	60Hz
Rectifier side L-filter	3mH
Rectifier side C-filter	130 μ F(Δ connection)
Converter parameters	
dc-link inductance	5mH
Rated active power	20kW
Rated Reactive power	8kVAr
Inverter side parameters	
Grid voltage	380 VL L
Grid frequency	50Hz
Inverter side C-filter	80 μ F(Δ connection)
Transformer rated power	20kW
Transformer primary related voltage	380V L-L Y
Transformer secondary related voltage	380V L-L Y

- i. Performance of grid active power with zero reactive power reference

The simulation scenario consists of three cases, each has 2s duration and the reference grid delivered active power are 10kW, 20kW and 15kW. Figure 5.19 to Figure 5.21 show the simulation results from PSCAD/EMTDC. The results in Figure 5.19(a) show that proposed controller tracks the reference grid delivered power without over-shoot. Figure 5.19(b) shows that the average dc-link inductance current

follows the reference current, and the reference average dc-link current changes depending on the reference delivered active power change. Figure 5.20(a) to (c) shows that the CSI delivers to the grid a sinusoidal current, with low total harmonic distortion (THD), and unity PF since $Q_{ref}=0$. The results in 5.19(a) to (c) show that the rectifier has sinusoidal supply current, with the PF profile given in Figure 5.4.

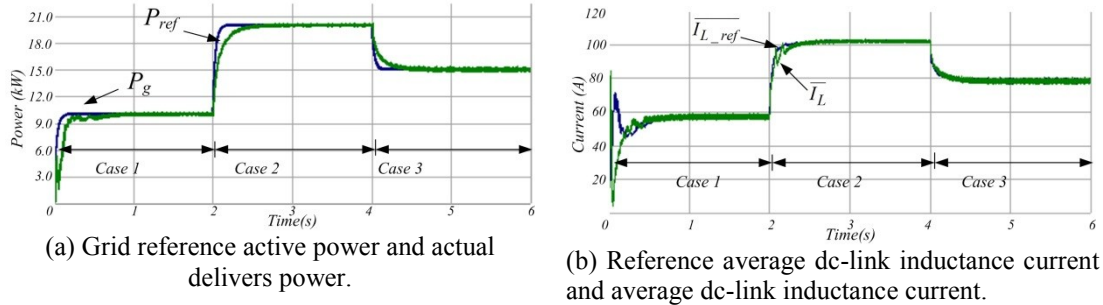


Figure 5.19 Waveforms of the active power controller of the BTB converter during the grid connection mode.

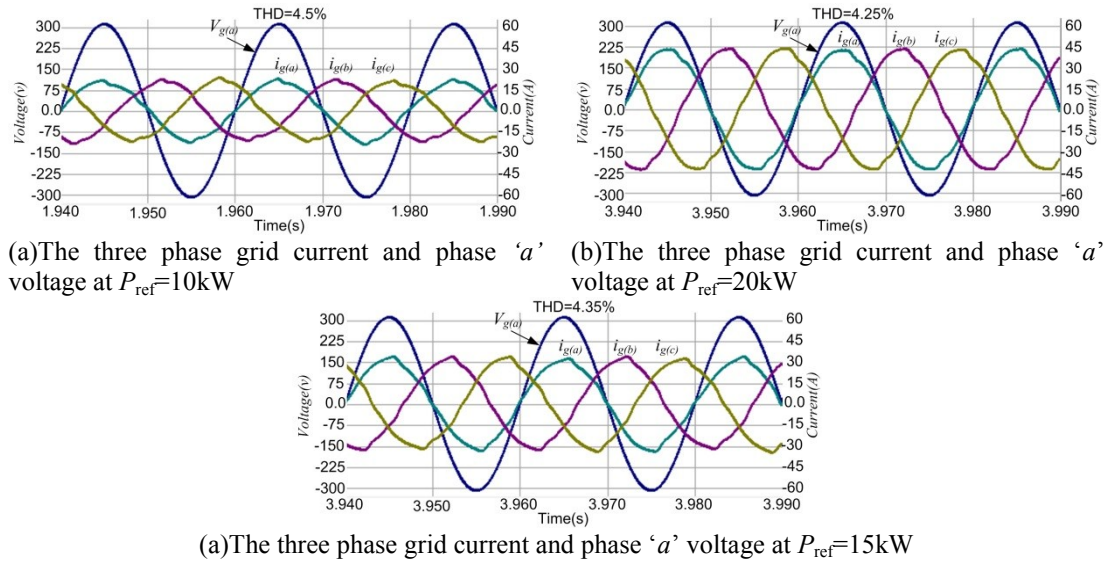


Figure 5.20 Detailed view of grid delivered current and phase 'a' voltage at each case (CSI side) of the BTB converter during the grid connection mode.

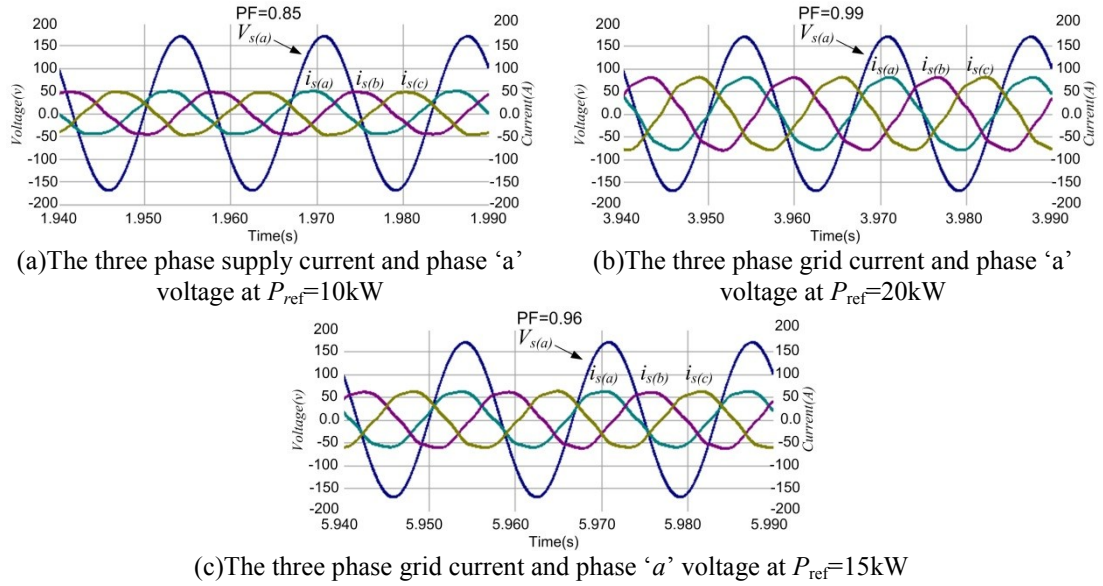
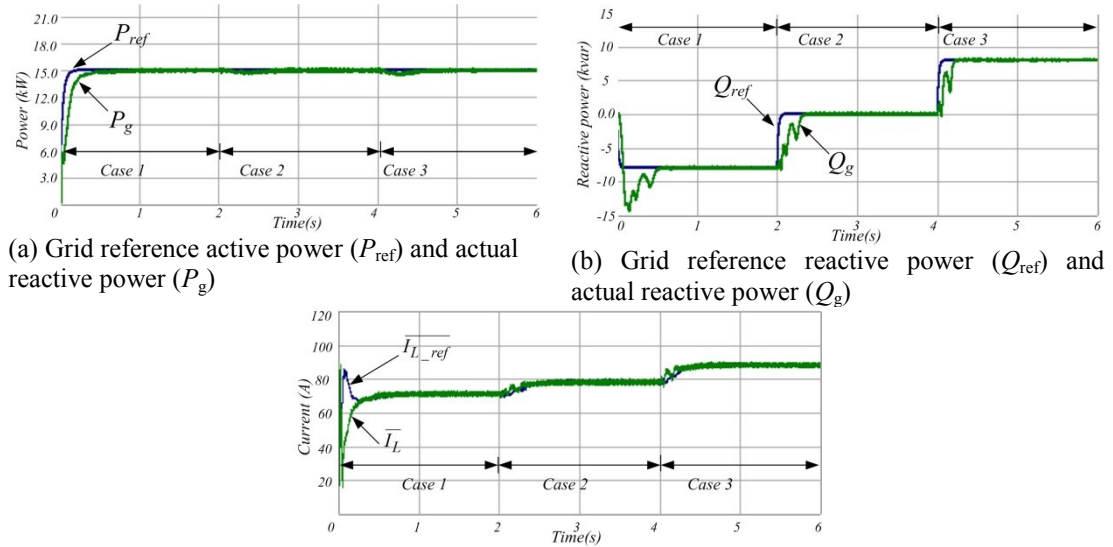


Figure 5.21 Detail view of three-phase supply current and phase 'a' voltage at each case (rectifier side) of the BTB converter during the grid connection mode.

- ii. Performance of proposed BTB converter with fixed active power and variable reference reactive power.

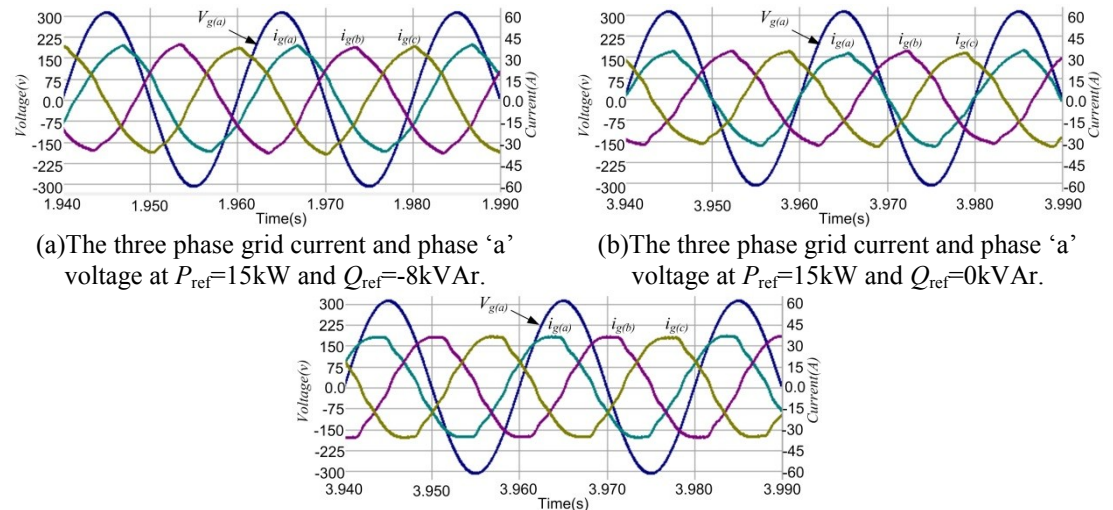
In this section the reference grid active power is kept a constant 15kW, and the reference grid reactive power Q_{ref} varies according to the following sequence. First Q_{ref} is set to -8kVAr for two seconds (case 1), then Q_{ref} gradually decreases to zero (case 2), and after two seconds Q_{ref} gradually changes to 8kVAr (case 2). This test will show the dynamic performance of the proposed reactive power controller and shows converter ability to control both grid delivered active and reactive power. Figure 5.22 and Figure 5.23 show the simulation results during reactive power control. Figure 5.22(a) shows that the proposed controller keeps the diverted active power fixed during all changes of the reactive power. Figure 5.22(b) show that the proposed reactive power controller follows the reference reactive power with good dynamic performance. Figure 5.22(c) show the average dc-link current follows the change in the reference average dc-link inductance current, the dc-link inductance current changes in each case to compensate the change in the reference reactive power, as shown by equation (5.26). Figure 5.23(a) to (c) show a detail view of the three-phase grid deliver current and phase 'a' voltage. The grid current leads the grid phase voltage in Figure 5.23(a) when reference reactive power is set to -8kVAr, and when set to zero the grid current is in phase with the grid phase voltage as shown in

Figure 5.23(b). Figure 5.23(c) show the grid current lags the grid voltage when the reference reactive power is 8kVAr.



(c) Reference average dc-link inductance current and average dc-link inductance current.

Figure 5.22 Waveforms of the overall performance of the reactive power performance of the proposal BTB converter.



(c) The three phase grid current and phase 'a' voltage at $P_{ref}=15\text{kW}$ and $Q_{ref}=8\text{kVAr}$.

Figure 5.23 Detailed view of grid delivered three-phase current and phase 'a' voltage at each case (CSI side) to show the effect of the reactive power controller.

5.4. Proposed dual three-phase BTB converter

The proposed BTB converter shown in Figure 5.1 can be extended to operate with six phases. Figure 5.24 shows the proposal current source based dual three-phase BTB converter. The supply side can be dual three-phase generator or a three-phase supply with a phase-shift transformer. The converter consists of three legs connected

in shunt. The rectifier side leg consists of two cascaded three-phase diode rectifier bridges, in series with an active switch (S_r), with two input three-phase C-filters (C_{r1} and C_{r2}). The second leg is the dc-link inductance L_{dc} , which is the energy storage element. The dual-bridge CSI is the third leg and consists of two two-level CSI bridges connected in series and two output three-phase C-filters (C_{i1} and C_{i2}) forming the grid side converter. This is connected to the grid through a three-winding phase-shift transformer. The proposed converter has the same operating modes as the three-phase version, and has the same controller loops.

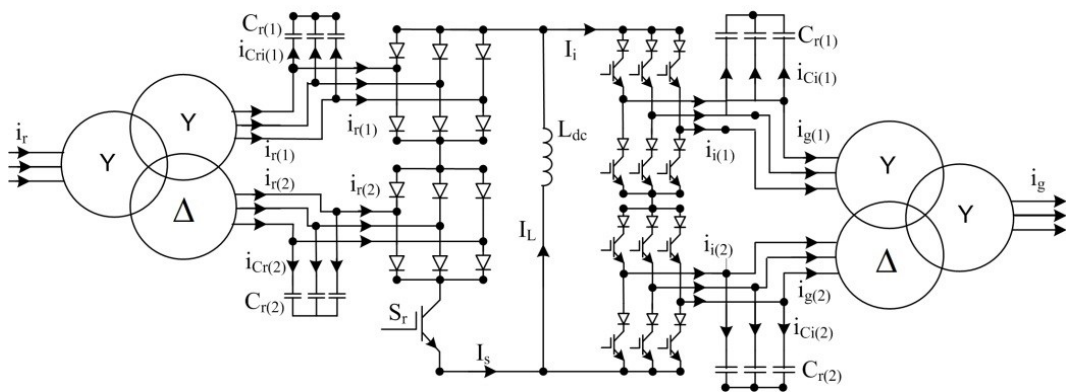


Figure 5.24 Proposed dual three-phase BTB converter.

5.4.1 Dual-bridge CSI output current harmonic cancellation, zero switching losses.

It is required from the proposed dual-bridge CSI show in Figure 5.26 to inject all the power absorbed from the supply into grid by modulating its average input dc-link current \bar{I}_L . Although the current into the dual CSI I_i is discontinuous, its average \bar{I}_i over one fundamental period is constant. The phase-shift transformer, cancels the 5th, 7th, 17th, 19th, 27th, 31st, etc. harmonic currents component [24, 25], while the inverter side C-filter has two functions: first making the dual CSI output current continuous, and second, removal of the 11th and 13th harmonics component from the dual CSI output current. The phase output current of the dual-bridge CSI is shown in Figure 5.25. To ensure zero switching losses in the dual CSI, its switching instants must coincide with zero input dc link current $I_i=0$ (as with the three-phase version)

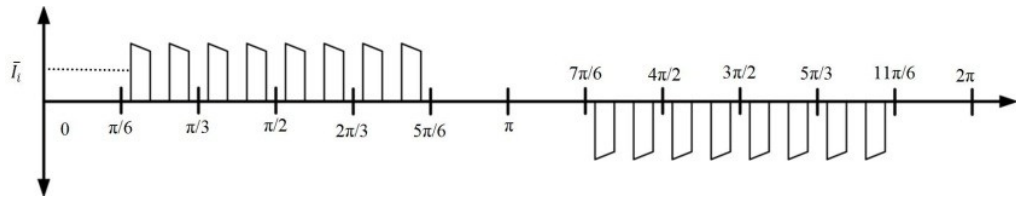


Figure 5.25 Pre-filter output phase current of the dual-bridge CSI.

5.4.2 Modified dual three-phase BTB converter

The switch S_r experiences high voltage stresses, thus requires a high number of switches connected in series. To solve this problem, the dc-link inductor is replaced by a central tap inductor, as show in Figure 5.26. The voltage stress will be shared by switches S_{r1} and S_{r2} . Switches S_{r1} and S_{r2} use the same gate signal, and the modified converter operate as the original three phase version, discussed in Chapter four.

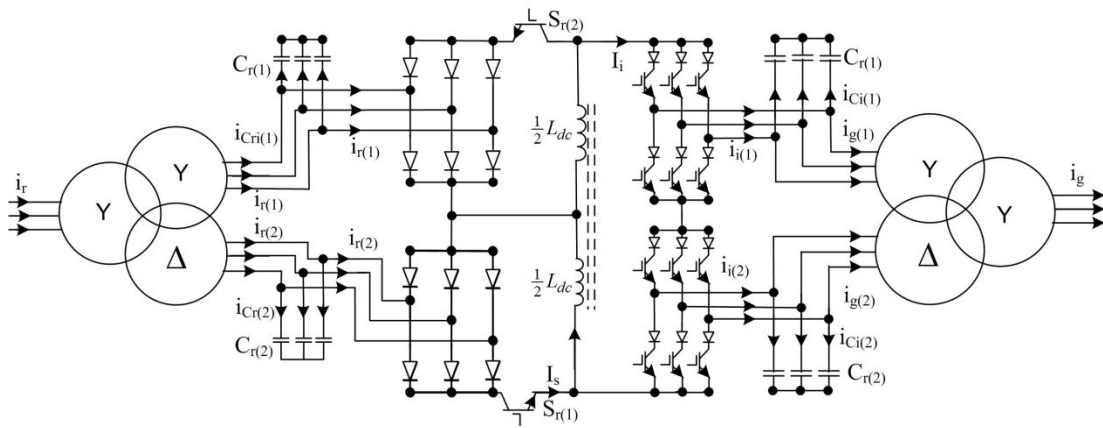


Figure 5.26 Modified dual three-phase BTB converter.

5.4.3 Simulation results

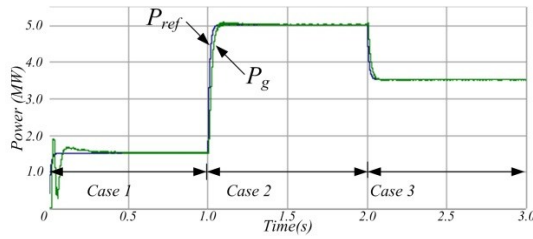
To assess the dynamic performance of the proposed dual three-phase BTB converter, its illustrative version in Figure 5.24 is simulated using PSCAD/EMTDC. The simulation section consists of two parts. First the reference grid reactive power is keep constant $Q_{ref}=0$ and the grid active power is varied; in this part the dynamic performance of the active power controller is assessed. The second part tests the dynamic performance of the reactive power controller by changing the reference reactive power whilst keeping the grid delivered active power fixed. The simulation parameters are given in Table 5.5.

i. Grid connection performance at zero reactive power reference

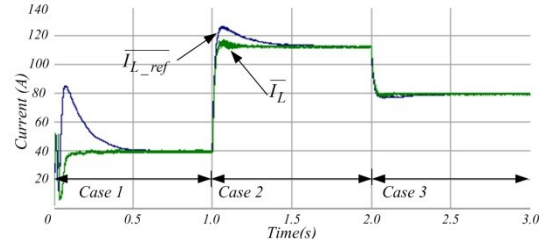
The active power controller dynamic performance is tested in three different cases, each of one second duration and the reference grid delivered active powers are 1.5MW, 5MW and 3.5MW. The simulation results are shown in Figure 5.27 to Figure 5.29. Figure 5.27(a) shows that the proposed controller smoothly tracks the reference active power with minimum transient time. Figure 5.27(b) shows that the dc-link current controller has good dynamics performance and smoothly follows the change in the reference average dc-link inductance current to compensate the change in the reference grid delivered active power. Figure 5.28 shows that the controller injects a sinusoidal current into the grid and in phase with the grid phase voltage. Also from Figure 5.28(a), the grid injected current increases rapidly and smoothly during the change from case 1 to case 2, and decreases rapidly and smoothly during the change from case 2 to case 3. Figure 5.29 shows that the proposed dual three-phase BTB converter takes from the supply, a high quality supply current with high power factor over a wide range of operation.

Table 5.5 Simulation parameters of the dual three-phase BTB converter during grid connected mode.

	Value
Rectifier side parameters	
Supply voltage	3.3kV
Supply frequency	50Hz
Phase-shifted transformer rated power	5.5 MVA
Phase-shifted transformer rated voltage	3.3 kV
Rectifier side C-filter	125 μ F Y connected
BTB Converter parameters	
Rated active power	5MW
Rated reactive power	2MVAr
dc-link inductance	10mH
Switch S_r frequency	1.2kHz
Inverter side parameters	
Inverter side C-filter	70 μ F Δ connected
Phase-shifted transformer rated power	5.5 MVA
Phase-shifted transformer rated voltage	3.3 kV
Grid rated voltage	3.3 kV
Grid rated frequency	50Hz

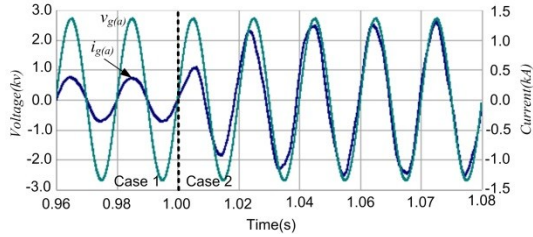


(a) Grid reference active power and actual delivers power.

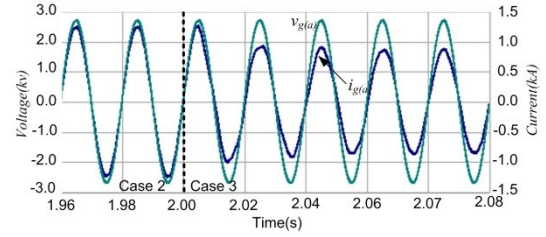


(b) Reference average dc-link inductance current and average dc-link inductance current.

Figure 5.27 Waveforms shows the overall performance of the dual three-phase BTB converter.

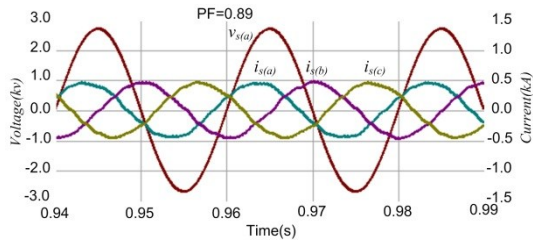


(a) detail view of the phase 'a' current and voltage during the change from case 1 to case 2

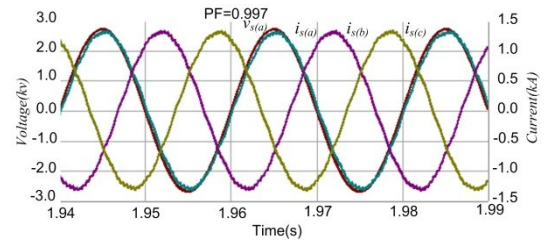


(b) detail view of the phase 'a' current and voltage during the change from case 2 to case 3

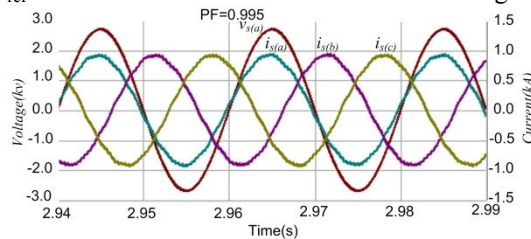
Figure 5.28 Detail view of phase 'a' current and voltage of the primary side of the phase-shift transformer in dual-bridge CSI side.



(a)The three phase supply current and phase 'a' voltage at $P_{ref}=1\text{MW}$



(b)The three phase supply current and phase 'a' voltage at $P_{ref}=5\text{MW}$

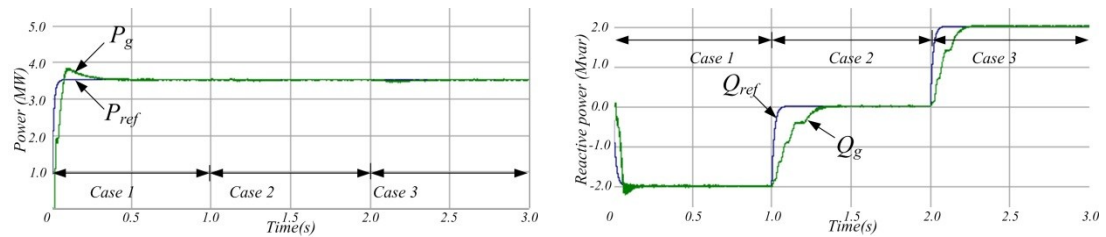


(c)The three phase supply current and phase 'a' voltage at $P_{ref}=3.5\text{MW}$

Figure 5.29 Detail view of three-phase supply current and phase 'a' voltage at each case (dual-bridge rectifier side) of the proposed dual three-phase BTB converter during the grid connection mode.

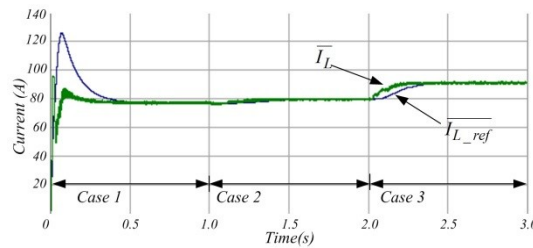
ii. Grid connection performance at fixed active power and variable reactive power

This section assesses the performance of the reactive power controller of the proposed dual three-phase BTB convert. The simulation sequence consists of three cases, each of one second duration, with reference reactive power of -2MVar, 0VAr and 2MVar respectively; whilst the grid delivered active power is constant. The PSCAD/EMTDC simulation results obtained are shown in Figure 5.30 and Figure 5.31. Figure 5.30(a) shows that the proposed controller keeps the grid delivered active power fixed in all cases. Figure 5.30(b) shows that the proposed reactive power controller tracks the reference reactive power with good dynamic performance. Figure 5.30(c) show that the dc-link inductance current changes to compensate the change in reference reactive power. The results in Figure 5.31 show that the proposed converter injects into the grid, high quality sinusoidal current, where the injected current is leading during Case 1, in-phase in Case 2, and lagging in Case 3.



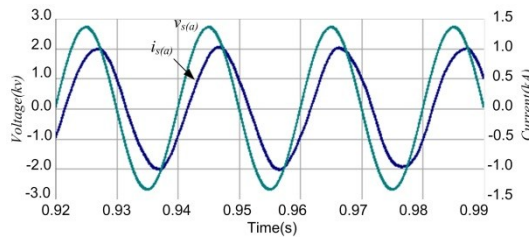
(a) grid reference active power(P_{ref}) and actual reactive power (P_g)

(b) grid reference reactive power(Q_{ref}) and actual reactive power (Q_g)

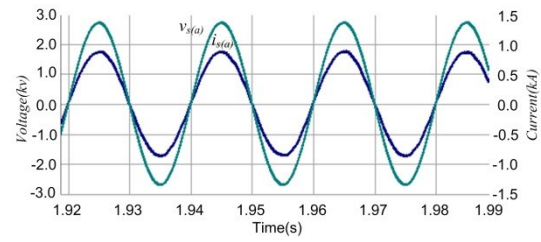


(c) Reference average dc-link inductance current and average dc-link inductance current.

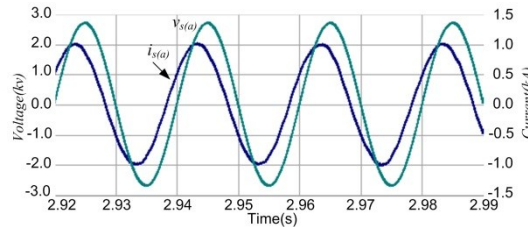
Figure 5.30 Performance waveforms of the reactive power controller of the dual BTB converter.



(a) The three phase grid current and phase 'a' voltage at $P_{ref}=3.5\text{MW}$ and $Q_{ref}=-2\text{MVar}$.



(b) The three phase grid current and phase 'a' voltage at $P_{ref}=3.5\text{MW}$ and $Q_{ref}=0\text{MVar}$.



(c) The three phase grid current and phase 'a' voltage at $P_{ref}=3.5\text{MW}$ and $Q_{ref}=2\text{MVar}$.

Figure 5.31 Detail view of phase 'a' current and voltage (dual-bridge CSI side) to show the performance of the reactive power controller.

5.5. Summary

This chapter proposed new current source based BTB converters. A three-phase version and a dual three-phase version. These new BTB converters have the following features:

- Reduced circuit and control complexity
- Sinusoidal input and output currents
- High input power factor and controllable output reactive power.
- Reduced semiconductor power loss (inverter side zero switching losses)
- Soft start-up and shut-down capability
- Reduce the over-voltage experience by switches during commutation

The performance of the proposed three-phase BTB converters was tested in island mode, showing their ability to provide a good voltage regulation even during step load change. The results obtain from both the three-phase BTB converter and the dual three-phase BTB converter in grid connection mode, show the ability to control the grid delivered active and reactive power, with sinusoidal supply current (rectifier side) and high power factor in the supply side. The grid side injected current is sinusoidal with a low THD.

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Chapter 6. Synchronous Machine and Wind Turbine Modelling

This chapter presents a dynamic model of three-phase and dual three-phase synchronous machines. The models are established for PSCAD/EMTDC modelling of the proposal wind energy conversion system (WECS) discussed in Chapter seven. The differential equations for both synchronous machines are transfer to the dq0 frame. The wind turbine models and equations are also presented in this chapter; where the wind turbine model is built to simulate the proposal wind energy conversion system and also used to build a wind turbine emulator, as part of the experimental validation of the proposed WECS; as will be shown in Chapter seven.

6.1. Background

6.1.1 Singly excited magnetic circuit

Consider a coil of N turns is wound on a core as shown in Figure 6.1, where the terminal voltage is:

$$e = \frac{d\psi}{dt} + ri \quad (6.1)$$

And the flux linkage is:

$$\psi = Li \quad (6.2)$$

Where r is the coil resistance, ψ is flux linkage, and i is coil current

The inductance, by definition, is equal to flux linkage per unit current [1].

$$L = \frac{N\phi}{i} = \frac{N^2}{\mathfrak{R}} \quad (6.3)$$

$$\phi = \frac{Ni}{\mathfrak{R}} \quad (6.4)$$

Where Φ is flux, \mathfrak{R} is magnetic path reluctance $= \frac{l}{A\mu_0\mu_r}$, μ_0 is absolute permeability ($\mu_0=4\pi\times 10^{-7}$ H/m), μ_r is core relative permeability, l the length of the equivalent magnetic path, and A is cross-section area.

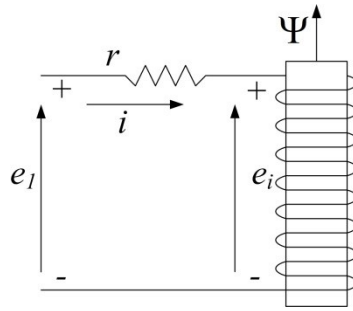


Figure 6.1 Singly excited magnetic circuit.

6.1.2 Magnetically coupled circuit

Figure 6.2 shows a magnetically coupled circuit which consists of two coils of N_1 and N_2 turns, wound on a common core.

$$e_1 = r_1 i_1 + \frac{d\psi_1}{dt} \quad (6.5)$$

$$e_2 = r_2 i_2 + \frac{d\psi_2}{dt} \quad (6.6)$$

The flux ϕ has two components: leakage flux and magnetization (or mutual) flux. The flux of each coil can be expressed as [1]:

$$\phi_1 = \phi_{l1} + \phi_{m1} + \phi_{m2} \quad (6.7)$$

$$\phi_2 = \phi_{l2} + \phi_{m2} + \phi_{m1} \quad (6.8)$$

Where ϕ_{l1} is produced by the current flow in coil 1 and links only the turns of coil 1, similarly for ϕ_{l2} . The magnetization flux ϕ_{m1} is produced by the current flow in coil 1 and links all turns of coil 1 and coil 2. Similarly for ϕ_{m2} . If saturation is neglected, the fluxes may be expressed as:

$$\Phi_{l1} = \frac{N_1 i_1}{\mathfrak{R}_{l1}} \quad (6.9)$$

$$\Phi_{m2} = \frac{N_1 i_1}{\mathfrak{R}_m} \quad (6.10)$$

$$\Phi_{l2} = \frac{N_2 i_2}{\mathfrak{R}_{l2}} \quad (6.11)$$

$$\Phi_{m1} = \frac{N_2 i_2}{\mathfrak{R}_m} \quad (6.12)$$

Where \mathfrak{R}_{l1} and \mathfrak{R}_{l2} are the reluctance of the leakage path, and \mathfrak{R}_m is the reluctance of the magnetizing fluxes.

Substituting (6.9) to (6.12) into (6.7) and (6.8) gives:

$$\phi_1 = \frac{N_1 i_1}{\mathfrak{R}_{l1}} + \frac{N_1 i_1}{\mathfrak{R}_m} + \frac{N_2 i_2}{\mathfrak{R}_m} \quad (6.13)$$

$$\phi_2 = \frac{N_2 i_2}{\mathfrak{R}_{l2}} + \frac{N_2 i_2}{\mathfrak{R}_m} + \frac{N_1 i_1}{\mathfrak{R}_m} \quad (6.14)$$

L_1 and L_2 can calculate using (6.3), (6.13) and (6.14):

$$L_1 = \frac{N_1^2}{\mathfrak{R}_{l1}} + \frac{N_1^2}{\mathfrak{R}_m} + \frac{N_1 N_2}{\mathfrak{R}_m} \quad (6.15)$$

$$L_2 = \frac{N_2^2}{\mathfrak{R}_{l2}} + \frac{N_2^2}{\mathfrak{R}_m} + \frac{N_1 N_2}{\mathfrak{R}_m} \quad (6.16)$$

The self-inductances (L_{11} and L_{22}) and the mutual-inductances ($L_{12}=L_{21}$) inductances can define as[1]:

$$L_{11} = \frac{N_1^2}{\mathfrak{R}_{l1}} + \frac{N_1^2}{\mathfrak{R}_m} \quad (6.17)$$

$$L_{22} = \frac{N_2^2}{\mathfrak{R}_{l2}} + \frac{N_2^2}{\mathfrak{R}_m} \quad (6.18)$$

$$L_m = \frac{N_1 N_2}{\mathfrak{R}_m} \quad (6.19)$$

The flux leakage can be expressed in terms of flux and inductance.

$$\psi_1 = L_{11} i_1 + L_m i_2 \quad (6.20)$$

$$\psi_2 = L_{22} i_2 + L_m i_1 \quad (6.21)$$

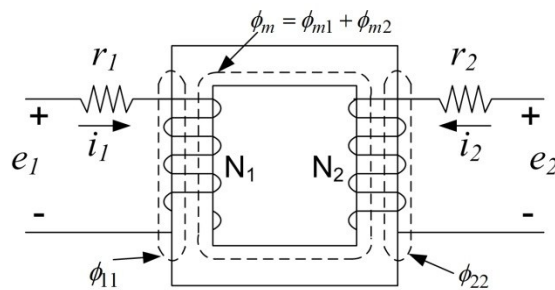


Figure 6.2 Magnetically coupled circuit.

6.1.3 Invariant Park's Transformation

Park's Transformation simplifies the mathematical equations describing a synchronous machine. By using Park's transformation the machine's electrical angle and stator quantities are projected onto the rotating d-axis and q-axis. The rotor windings are not subjected to any transformation because they are oriented in the d-axis and q-axis by the assumptions made in [1, 2].

The Park's transformation C is used to transform from (abc) to (dq0) axes and is defined as [3, 4]:

$$[C] = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (6.22)$$

Because of the orthogonal properties of the invariant Park transform, C^t will be used to convert from (dq0) to (abc) axes as $C^t = C^{-1}$:

$$[C^t] = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{\sqrt{2}} \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (6.23)$$

Voltage, current, flux linkage and impedance transformations used in this chapter are summarized as follows:

$$\begin{aligned} [V_{dq0}] &= C[V_{abc}] & [V_{abc}] &= C^t[V_{dq0}] \\ [i_{dq0}] &= C[i_{abc}] & [i_{abc}] &= C^t[i_{dq0}] \\ [\psi_{dq0}] &= C[\psi_{abc}] & [\psi_{abc}] &= C^t[\psi_{dq0}] \\ [Z_{dq0}] &= C[Z_{abc}]C^t & [Z_{abc}] &= C^t[Z_{dq0}]C \\ [L_{dq0}] &= C[L_{abc}]C^t & [L_{abc}] &= C^t[L_{dq0}]C \end{aligned} \quad (6.24)$$

6.2. Three-phase synchronous generator modelling

This section derives the dq-model for the three-phase synchronous generator (SG) as a precursor to the detailed derivation of the dq-model for the dual three-phase SG.

The three-phase SG consists of a three-phase stator winding mounted and distributed in space 120° apart around the inner surface of the stator. The field winding is

mounted on the rotor and supplied by direct current to produce the needed rotating magnetic field to generate electromotive force voltage at the stator windings. D and Q damper windings are placed in d and q axes of the rotor. The damper windings are used to suppress mechanical rotor oscillation caused by a sudden change in the electrical or mechanical load [1, 3].

6.2.1 Three-phase synchronous generator inductances calculation

Figure 6.3 shows a cross section of a salient pole synchronous generator. To simplify the derivation of the machine equations, the following assumptions are made:

- The stator windings are uniformly distributed such that the self and mutual inductances vary sinusoidally with rotor position.
- Saturation effects, eddy currents, and core losses are neglected.
- All three-phase windings are assumed balanced.

The machine inductances are categorized as [3]:

1. Stator self-inductances:

$$\begin{aligned} L_{aa} &= L_s + L_m \cos 2\theta \\ L_{bb} &= L_s + L_m \cos 2\left(\theta - \frac{2\pi}{3}\right) \\ L_{cc} &= L_s + L_m \cos 2\left(\theta + \frac{2\pi}{3}\right) \end{aligned} \quad (6.25)$$

Where L_s is the self-inductance, L_m is the mutual-inductance, and θ is the angle between magnetic axes of phase 'a' and the rotating magnetic field.

2. Stator mutual-inductance of salient pole SG:

$$\begin{aligned} L_{ab} &= -M_s + L_m \cos 2\left(\theta - \frac{\pi}{3}\right) \rightarrow L_{ab} = L_{ba} \\ L_{bc} &= -M_s + L_m \cos 2\theta \rightarrow L_{bc} = L_{cb} \\ L_{ca} &= -M_s + L_m \cos 2\left(\theta + \frac{\pi}{3}\right) \rightarrow L_{ca} = L_{ac} \end{aligned} \quad (6.26)$$

M_s is the average value of mutual inductance.

3. Rotor self-inductance:

L_f : The constant amplitude self-inductance of the field winding.

L_D : The constant amplitude self-inductance of the D-damper winding.

L_Q : The constant amplitude self-inductance of the Q-damper winding.

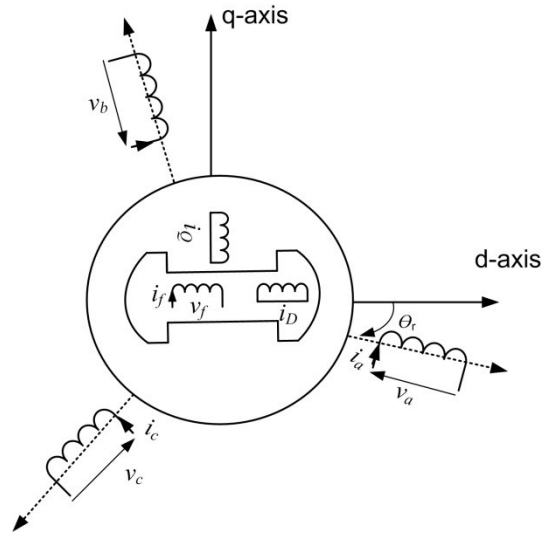


Figure 6.3 Wound rotor three phase synchrony machine.

4. Rotor mutual-inductances:

The constant mutual inductance between the field winding and the D-damper winding are:

$$\begin{aligned} L_{fD} &= L_{Df} = M_r \\ L_{fQ} &= L_{Qf} = 0 \\ L_{DQ} &= L_{QD} = 0 \end{aligned} \quad (6.27)$$

M_r is the constant mutual inductance between the field and D-damper winding.

5. Stator and rotor mutual-inductances.

$$\begin{aligned} L_{af} &= M_f \cos \theta \rightarrow L_{af} = L_{fa} \\ L_{bf} &= M_f \cos\left(\theta - \frac{2}{3}\pi\right) \rightarrow L_{bf} = L_{fb} \\ L_{cf} &= M_f \cos\left(\theta + \frac{2}{3}\pi\right) \rightarrow L_{cf} = L_{fc} \end{aligned} \quad (6.28)$$

M_f is the amplitude of the mutual inductance between the armature winding and the field winding.

$$\begin{aligned}
L_{aD} &= M_D \cos \theta \rightarrow L_{aD} = L_{Da} \\
L_{bD} &= M_D \cos\left(\theta - \frac{2}{3}\pi\right) \rightarrow L_{bD} = L_{Db} \\
L_{cD} &= M_D \cos\left(\theta + \frac{2}{3}\pi\right) \rightarrow L_{cD} = L_{Dc}
\end{aligned} \tag{6.29}$$

M_D is the mutual inductance amplitude between the armature winding and the D-damper winding.

$$\begin{aligned}
L_{aQ} &= -M_Q \cos \theta \rightarrow L_{aQ} = L_{Qa} \\
L_{bQ} &= -M_Q \cos\left(\theta - \frac{2}{3}\pi\right) \rightarrow L_{bQ} = L_{Qb} \\
L_{cQ} &= -M_Q \cos\left(\theta + \frac{2}{3}\pi\right) \rightarrow L_{cQ} = L_{Qc}
\end{aligned} \tag{6.30}$$

M_Q is the mutual inductance amplitude between the armature winding and the Q-damper winding.

The machine inductance can be written in matrix form as shown in equation (6.31), where the main diagonal comprises self-inductance coefficients.

$$L_{abc} = \begin{bmatrix} \begin{matrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ba} & L_{bb} & L_{bc} \\ L_{ca} & L_{cb} & L_{cc} \end{matrix} & \begin{matrix} L_{aF} & L_{aD} & L_{aQ} \\ L_{bF} & L_{bD} & L_{bQ} \\ L_{cF} & L_{cD} & L_{cQ} \end{matrix} \\ \begin{matrix} L_{Fa} & L_{Fb} & L_{Fc} \\ L_{Da} & L_{Db} & L_{Dc} \\ L_{Qa} & L_{Qb} & L_{Qc} \end{matrix} & \begin{matrix} L_{FF} & L_{FD} & L_{FQ} \\ L_{DF} & L_{DD} & L_{DQ} \\ L_{QF} & L_{QD} & L_{QQ} \end{matrix} \end{bmatrix} = \begin{bmatrix} L_{ss} & L_{sr} \\ L_{rs} & L_{rr} \end{bmatrix} \tag{6.31}$$

Where L_{ss} represent the stator self and mutual inductance, L_{sr} and L_{rs} represent the stator and rotor mutual inductances ($L_{rs} = L_{sr}^T$), and L_{rr} represent rotor mutual inductance.

6.2.2 Converting the inductance matrix to the dq0 frame

The machine inductance matrix can be converted to the dq0 reference frame using equations (6.32) to (6.35) [3].

$$[L_{dq0}] = [C][L_{abc}][C^t] \tag{6.32}$$

$$[L_{dq0}] = \begin{bmatrix} C & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} L_{SS} & L_{SR} \\ L_{RS} & L_{RR} \end{bmatrix} \begin{bmatrix} C^t & 0 \\ 0 & 1 \end{bmatrix} \tag{6.33}$$

$$[L_{dq0}] = \begin{bmatrix} CL_{SS}C^t & CL_{SR} \\ L_{RS}C^t & L_{RR} \end{bmatrix} \quad (6.34)$$

$$[L_{dq0}] = \begin{bmatrix} \frac{3}{2}L_m + (L_s + M_s) & 0 & 0 & \sqrt{\frac{3}{2}}M_f & \sqrt{\frac{3}{2}}M_D & 0 \\ 0 & -\frac{3}{2}L_m + (L_s + M_s) & 0 & 0 & 0 & \sqrt{\frac{3}{2}}M_Q \\ 0 & 0 & L_s - 2M_s & 0 & 0 & 0 \\ \sqrt{\frac{3}{2}}M_f & 0 & 0 & L_f & M_{fD} & 0 \\ \sqrt{\frac{3}{2}}M_D & 0 & 0 & M_{Df} & L_D & 0 \\ 0 & \sqrt{\frac{3}{2}}M_Q & 0 & 0 & 0 & L_Q \end{bmatrix} \quad (6.35)$$

Equation (6.35) shows that the transformation to dq0 provides a simplified inductance matrix which is independent of Θ .

Self-inductance coefficients can be defined as follows:

$$\text{Direct-axis synchronous inductance: } L_d = L_s + \frac{3}{2}L_m + M_s$$

$$\text{Quadrature-axis synchronous inductance: } L_q = L_s - \frac{3}{2}L_m + M_s$$

$$\text{Mutual inductance coefficient: } M_{df} = \sqrt{\frac{3}{2}}M_f, \quad M_{dD} = \sqrt{\frac{3}{2}}M_D \text{ and } M_{qQ} = \sqrt{\frac{3}{2}}M_Q.$$

Equation (6.35) can be rewritten as:

$$[L_{dq0}] = \begin{bmatrix} L_d & 0 & 0 & M_{df} & M_{dD} & 0 \\ 0 & L_q & 0 & 0 & 0 & M_{qQ} \\ 0 & 0 & L_0 & 0 & 0 & 0 \\ M_{df} & 0 & 0 & L_f & M_{fD} & 0 \\ M_{dD} & 0 & 0 & M_{fD} & L_D & 0 \\ 0 & M_{qQ} & 0 & 0 & 0 & L_Q \end{bmatrix} \quad (6.36)$$

6.2.3 Voltage equations

The SG voltage equation is given in (6.37):

$$[v_{abc}] = -[R][i_{abc}] - P[\psi_{abc}] \quad (6.37)$$

$$\psi = L_{abc}i_{abc} \quad (6.38)$$

Where:

$$[v_{abc}] = [V_a \ V_b \ V_c \ V_f \ 0 \ 0]^t$$

$$[i_{abc}] = [i_a \ i_b \ i_c \ i_f \ i_D \ i_Q]^t$$

$$[R] = \begin{bmatrix} r_s & 0 & 0 & 0 & 0 & 0 \\ 0 & r_s & 0 & 0 & 0 & 0 \\ 0 & 0 & r_s & 0 & 0 & 0 \\ 0 & 0 & 0 & r_f & 0 & 0 \\ 0 & 0 & 0 & 0 & r_D & 0 \\ 0 & 0 & 0 & 0 & 0 & r_Q \end{bmatrix}$$

Where λ is flux linkage, r_s is stator winding resistance, r_f is field winding resistance, r_D is D-damper winding resistance, r_Q is Q-damper winding resistance, and P is the differential operator $\frac{d}{dt}$.

$P[\lambda_{abc}]$ In (6.37) complicates the analysis, which can be simplified by using Park's transformation to the stator partition. The voltage equation can be converted from (abc) to (dq0) by multiplying by the converter matrix C .

$$V_{dq0} = CV_{abc} \quad (6.39)$$

The resistance voltage drop on the right hand side of (6.37) will be $CRi_{abc} = Ri_{dq0}$, the second term in the left hand side part of equation (6.37) is $C\dot{\psi}_{uv}$ and is evaluated as follows.

From equation (6.24) $\psi_{dq0} = C\psi_{abc}$ hence

$$\dot{\psi}_{uv} = \dot{\psi}_{uv} \quad (6.40)$$

$$C\dot{\psi}_{uv} = \dot{\psi}_{dq0} \quad (6.41)$$

The voltage equation in (dq0) can be written as:

$$[V_{dq0}] = -[R][i_{dq0}] - P[L_{dq0}][i_{dq0}] + \dot{C}C^t[L_{dq0}][i_{dq0}] \quad (6.42)$$

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_f \\ 0 \\ 0 \end{bmatrix} = - \begin{bmatrix} r_s & 0 & 0 & 0 & 0 & 0 \\ 0 & r_s & 0 & 0 & 0 & 0 \\ 0 & 0 & r_s & 0 & 0 & 0 \\ 0 & 0 & 0 & r_f & 0 & 0 \\ 0 & 0 & 0 & 0 & r_D & 0 \\ 0 & 0 & 0 & 0 & 0 & r_Q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \\ i_f \\ i_D \\ i_Q \end{bmatrix} - p \begin{bmatrix} L_d & 0 & 0 & M_{df} & M_{dD} & 0 \\ 0 & L_q & 0 & 0 & 0 & M_{qQ} \\ 0 & 0 & L_0 & 0 & 0 & 0 \\ M_{ff} & 0 & 0 & L_f & M_{fD} & 0 \\ M_{dD} & 0 & 0 & M_{fD} & L_D & 0 \\ 0 & M_{qQ} & 0 & 0 & 0 & L_Q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \\ i_f \\ i_D \\ i_Q \end{bmatrix} + \quad (6.43)$$

$$\omega_e \begin{bmatrix} 0 & L_q & 0 & 0 & 0 & M_{qQ} \\ -L_d & 0 & 0 & -M_{ff} & -M_{dD} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \\ i_f \\ i_D \\ i_Q \end{bmatrix}$$

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_f \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -r_s i_d - p(L_d i_d + M_{dD} i_D + M_{df} i_f) + \omega_e (L_q i_q + M_{dQ} i_Q) \\ -i_q r_s - p(L_q i_q + p M_{dQ} i_Q) - \omega_e (L_d i_d + M_{dD} i_D + M_{df} i_f) \\ -i_0 (r_s + p L_0) \\ -r_f i_f - p(L_f i_f + M_{fD} i_D + M_{ff} i_d p) \\ -r_D i_D - p(L_D i_D + M_{dD} i_d + M_{fD} i_f) \\ -r_Q i_Q - p(L_Q i_Q + M_{qQ} i_q) \end{bmatrix} \quad (6.44)$$

$$\omega_e = P_p \omega_m \quad (6.45)$$

Where P_p is the number of pole pair, ω_e is electrical rotating speed of the generator and ω_m is mechanical angular speed.

The voltage equation (6.44) can be written in term of the flux linkage matrix ψ_{dq0} .

$$\psi_{dq0} = [L_{dq0}] [i_{dq0}] \quad (6.46)$$

$$\begin{bmatrix} \psi_d \\ \psi_q \\ \psi_0 \\ \psi_f \\ \psi_D \\ \psi_Q \end{bmatrix} = \begin{bmatrix} L_d i_d + M_{dD} i_D + M_{df} i_f \\ L_q i_q + M_{dQ} i_Q \\ L_0 i_0 \\ L_f i_f + M_{fD} i_D + M_{ff} i_d \\ L_D i_D + M_{dD} i_d + M_{fD} i_f \\ L_Q i_Q + M_{qQ} i_q \end{bmatrix} \quad (6.47)$$

Substituting equation (6.49) into (6.48), the voltage equation becomes:

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \\ V_f \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -r_s i_d - p\psi_d + \omega_r \psi_q \\ -i_q r_s - p\psi_q - \omega_r \psi_d \\ -i_0 \psi_0 \\ -r_f i_f - p\psi_f \\ -r_D i_D - p\psi_D \\ -r_Q i_Q - p\psi_Q \end{bmatrix} \quad (6.49)$$

6.2.4 Torque equations

Reference [3] outline show to calculate the electromagnetic torque the from rotational coefficient matrix $[G] = \frac{-\dot{c} \cdot \psi_{dq0}}{\omega}$.

$$T_e = (\text{pole} - \text{pairs}) [i_{dq0}]^t [G] [i_{dq0}] \quad (6.50)$$

$$T_e = \text{pole_pairs} \left((L_d - L_q) i_d i_q + M_{df} i_f i_q + M_{dD} i_D i_q - M_{dQ} i_Q i_d \right) \quad (6.51)$$

Torque components:

$$\text{Cylindrical torque} = \text{pole_pairs} (M_{df} i_f i_q)$$

$$\text{Saliency torque} = \text{pole_pairs} ((L_d - L_q) i_d i_q)$$

$$\text{Damping torque} = \text{pole_pairs} (M_{dD} i_D i_q - M_{dQ} i_Q i_d)$$

From (6.47) the torque equation becomes:

$$T_e = \text{pole_pairs} (\psi_d i_q - \psi_q i_d) \quad (6.52)$$

6.2.5 Equations of motion

The SG electromechanical dynamics, when the inertia of the generator and prime-mover is combined, can be expressed using accelerating torque as:

$$T_m - T_e = J \frac{d\omega_m}{dt} + D \omega_m + D_e (\omega_m - \omega_s) \quad (6.53)$$

Where

T_m : mechanical torque, Nm.

T_e : electromagnetic torque, Nm.

J : combined moment of inertia of generator and turbine, kg.m^2 .

ω_m : angular velocity of the rotor, rad/s .

t : time in seconds, s .

D : Mechanical damper torque and is proportional to the angular velocity.

D_e : Mechanical damping torque due to current in the damper winding and is proportional to the difference between rotor speed and synchronous speed, rad/s .

6.3. Three-phase permanent magnet synchronous generator model

The permanent magnet synchronous machine is a regular synchronous machine where the dc exciter is replaced by a permanent magnet. Using a permanent magnet rotor instead of a dc exciter element, reduces the rotor and brushes losses, reduces the weight and size of the machine and increases machine reliability. The dynamic model of the three-PMSG can be described in the d-q reference system as follows.

6.3.1 Basic machine flux equations

The flux of the machine coils can be described by the following equations:

$$\psi = Li + \psi_{sf} \quad (6.54)$$

Where:

$$[i] = [i_a \quad i_b \quad i_c]^T$$

ψ_{sf} is the flux linkage from the permanent magnet rotor.

The inductance of the salient pole PMSG depends on the rotor position, since there is no winding in the rotor the machine inductance given in Equation (6.31) can be written as following [5-7]:

$$L = \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ba} & L_{bb} & L_{bc} \\ L_{ca} & L_{cb} & L_{cc} \end{bmatrix} \quad (6.55)$$

Substituting equations (6.25) and (6.26) into (6.55):

$$L = \begin{bmatrix} L_s + L_m \cos 2\theta & -M_s + L_m \cos 2\left(\theta - \frac{1}{3}\pi\right) & -M_s + L_m \cos 2\left(\theta + \frac{1}{3}\pi\right) \\ -M_s + L_m \cos 2\left(\theta - \frac{1}{3}\pi\right) & L_s + L_m \cos 2\left(\theta - \frac{2}{3}\pi\right) & -M_s + L_m \cos \theta \\ -M_s + L_m \cos 2\left(\theta + \frac{1}{3}\pi\right) & -M_s + L_m \cos \theta & L_s + L_m \cos 2\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} \quad (6.56)$$

The relationship between the rotors permanent magnetic and stator winding flux can be determined by defining coupling factors which depend on the stator and rotor mechanical positions

$$\psi_{sf} = \left[F_{coup} \cos \theta \quad F_{coup} \cos\left(\theta - \frac{2}{3}\pi\right) \quad F_{coup} \cos\left(\theta + \frac{2}{3}\pi\right) \right]^T \quad (6.57)$$

Where F_{coup} is the maximum magnetic coupling coefficient between the rotor and stator

6.3.2 Machine inductance representation in the dq0 frame

The machine inductance can be written in dq0 as follows:

$$[L_{dq0}] = C \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ba} & L_{bb} & L_{bc} \\ L_{ca} & L_{cb} & L_{cc} \end{bmatrix} C^t \quad (6.58)$$

$$[L_{dq0}] = \begin{bmatrix} \frac{3}{2}L_m + (L_s + M_s) & 0 & 0 \\ 0 & -\frac{3}{2}L_m + (L_s + M_s) & 0 \\ 0 & 0 & L_s - 2M_s \end{bmatrix} = \begin{bmatrix} L_d & 0 & 0 \\ 0 & L_q & 0 \\ 0 & 0 & L_0 \end{bmatrix} \quad (6.59)$$

The permanent magnet rotor flux linkage matrix can be transferred to the dq0 reference frame:

$$\psi_{sfdq} = C\psi_{sf} \quad (6.60)$$

$$\begin{bmatrix} \psi_{sf_d} \\ \psi_{sf_q} \\ \psi_{sf_0} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}}F_{coup} \\ 0 \\ 0 \end{bmatrix} \quad (6.61)$$

The flux linkage matrix in the dq0 frame is:

$$\begin{bmatrix} \psi_d \\ \psi_q \\ \psi_0 \end{bmatrix} = \begin{bmatrix} L_d & 0 & 0 \\ 0 & L_q & 0 \\ 0 & 0 & L_0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} \sqrt{\frac{3}{2}} F_{coup} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} F_{coup} + L_d i_d \\ L_q i_q \\ L_0 i_0 \end{bmatrix} \quad (6.62)$$

6.3.3 Three-phase PMSG voltage and torque equations in the dq0 frame

Similarly to subsection 6.2.3, the PMSG voltage equation in the dq0 is shown in (6.63) [8].

$$[V_{dq0}] = -[R][i_{dq0}] - \left(\psi_{dq0} \dot{\omega} - \omega C^r \psi_{dq0} \right) \quad (6.63)$$

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} -r i_d - p \psi_d + \omega_e \psi_q \\ -r i_q - p \psi_q - \omega_e \psi_d \\ -r i_0 - p \psi_0 \end{bmatrix} \quad (6.64)$$

The three-phase PMSG torque equation in dq0 is:

$$T_e = \text{pole_pairs} (\psi_d i_q - \psi_q i_d) \quad (6.65)$$

6.4. Dual three-phase permanent magnet synchronous generator model

Using a multi-phase machine in medium-voltage high-power applications is more attractive than using a normal three-phase machine of the same rating. The multi-phase machine gives the following benefits: lower per phase rated current, lower current and torque ripple, lower dc voltage ripple, and higher reliability [9-12].

In the late 1920's, the dual three-phase synchronous machine was used for power generation; then the extra phases were needed to overcome the limitation imposed by the fault current interrupting capacity of circuit breakers [13]. The dual three-phase permanent magnet synchronous generator (PMSG) has been proposed for power supplies on aircraft and ships for the following reasons: 1- the dual three-phase machine is able to supply AC power from one stator set and DC power through a

rectifier connected to the other stator set: this means lower cost and weight than alternative three-phase generator-transformer-rectifier systems. 2- smaller filtering size is required because the rotor inertia helps smooth fluctuations in the energy transfer [14].

The dual three-phase PMSG is composed of two symmetrical sets of three-phase windings galvanically isolated and shifted by 30° electrical, called (abc and xyz) [11, 13, 15].

6.4.1 Basic machine equations

The voltage, current and flux of the machine coils can describe by the following equations [16, 17].

$$[v] = -[R][i] - \frac{d}{dt}[\psi] \quad (6.66)$$

$$\psi = Li + \psi_{sf} \quad (6.67)$$

Where

$$[v] = [v_a \ v_b \ v_c \ v_x \ v_y \ v_z]^T$$

$$[i] = [i_a \ i_b \ i_c \ i_x \ i_y \ i_z]^T$$

$$[R] = rI_{6 \times 6}$$

ψ is flux linkage.

ψ_{sf} is the flux linkage from the permanent magnet rotor.

The inductance in salient pole machines depends on the rotor position and can be classified into two main groups: self-inductance L_{ii} of each stator phase, and mutual-inductance L_{ij} , the mutual inductance between two stator phases [13, 17, 18].

$$L_{ii} = L_s + L_m \cdot \cos(2(\theta + \alpha_i)) \quad (6.68)$$

$$L_{ij} = -M_s - L_m \cdot \cos(2(\theta + \alpha_{ij})) \quad (6.69)$$

Where:

α_i : the angle between the axis of the phase under analysis and the reference

α_{ij} : angle of the relative position between the winding of the stator and rotor

i, j equal (a, b, c, x, y and z) such that $i \neq j$

From equations(6.68) and (6.69) the self-inductance and the mutual-inductance of the dual three-phase machine can write as follows.

Machine self-inductance equations:

$$L_{aa} = L_s + L_m \cos \theta \quad (6.70a)$$

$$L_{bb} = L_s + L_m \cos 2\left(\theta - \frac{2}{3}\pi\right) \quad (6.70b)$$

$$L_{cc} = L_s + L_m \cos 2\left(\theta + \frac{2}{3}\pi\right) \quad (6.70c)$$

$$L_{xx} = L_s + L_m \cos 2\left(\theta - \frac{1}{6}\pi\right) \quad (6.70d)$$

$$L_{yy} = L_s + L_m \cos 2\left(\theta - \frac{5}{6}\pi\right) \quad (6.70e)$$

$$L_{zz} = L_s + L_m \cos 2\left(\theta + \frac{1}{2}\pi\right) \quad (6.70f)$$

$$(6.70)$$

As each stator winding is shifted in space relative to the others by 120° , the mutual inductance between each stator winding is negative. The machine mutual-inductance equations between any two stator phases are:

$$L_{ab} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{1}{3}\pi\right) \rightarrow L_{ab} = L_{ba} \quad (6.71a)$$

$$L_{ac} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta + \frac{1}{3}\pi\right) \rightarrow L_{ac} = L_{ca} \quad (6.71b)$$

$$L_{ax} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{1}{12}\pi\right) \rightarrow L_{ax} = L_{xa} \quad (6.71c)$$

$$L_{ay} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{5}{12}\pi\right) \rightarrow L_{ay} = L_{ya} \quad (6.71d)$$

$$L_{az} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta + \frac{1}{4}\pi\right) \rightarrow L_{az} = L_{za} \quad (6.71e)$$

$$L_{bc} = -\frac{1}{2}M_s - L_m \cos 2(\theta) \rightarrow L_{bc} = L_{cb} \quad (6.71f)$$

$$L_{bx} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{5}{12}\pi\right) \rightarrow L_{bx} = L_{xb} \quad (6.71g)$$

$$L_{by} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta + \frac{1}{4}\pi\right) \rightarrow L_{by} = L_{yb} \quad (6.71h)$$

$$L_{bz} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{1}{12}\pi\right) \rightarrow L_{bz} = L_{zb} \quad (6.71i)$$

$$L_{cx} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta + \frac{1}{4}\pi\right) \rightarrow L_{cx} = L_{xc} \quad (6.71j)$$

$$L_{cy} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{1}{12}\pi\right) \rightarrow L_{cy} = L_{yc} \quad (6.71k)$$

$$L_{cz} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{5}{12}\pi\right) \rightarrow L_{cz} = L_{zc} \quad (6.71l)$$

$$L_{xy} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{1}{2}\pi\right) \rightarrow L_{xy} = L_{yx} \quad (6.71m)$$

$$L_{xz} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta + \frac{1}{6}\pi\right) \rightarrow L_{xz} = L_{zx} \quad (6.71n)$$

$$L_{yz} = -\frac{1}{2}M_s - L_m \cos 2\left(\theta - \frac{1}{6}\pi\right) \rightarrow L_{yz} = L_{zy} \quad (6.71o)$$

(6.71)

Equations(6.70) and (6.71) are used to form the square inductance matrix, of order 6×6 , partitioned between the sets of phases.

$$L = \begin{bmatrix} L_{S1S1} & L_{S1S2} \\ L_{S2S1} & L_{S2S2} \end{bmatrix} \quad (6.72)$$

$$L = \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} & L_{ax} & L_{ay} & L_{az} \\ L_{ba} & L_{bb} & L_{bc} & L_{bx} & L_{by} & L_{bz} \\ L_{ca} & L_{cb} & L_{cc} & L_{cx} & L_{cy} & L_{cz} \\ L_{xa} & L_{xb} & L_{xc} & L_{xx} & L_{xy} & L_{xz} \\ L_{ya} & L_{yb} & L_{yc} & L_{yx} & L_{yy} & L_{yz} \\ L_{za} & L_{zb} & L_{zc} & L_{zx} & L_{zy} & L_{zz} \end{bmatrix} \quad (6.73)$$

Where S_1 can be (a, b and c), and S_2 can be (x, y and z).

The relationship between the rotor's permanent magnetic and stator winding flux can be determined by defining coupling factors which depends on the stator and rotor mechanical position [16, 17].

$$\psi_{sf} = F_{coup} \cos(\theta + \alpha_{if}) \quad (6.74)$$

$$\psi_{sf} = \begin{bmatrix} F_{coup} \cos(\theta + 0) & F_{coup} \cos\left(\theta - \frac{2}{3}\pi\right) & F_{coup} \cos\left(\theta + \frac{2}{3}\pi\right) \\ F_{coup} \cos\left(\theta - \frac{1}{6}\pi\right) & F_{coup} \cos\left(\theta - \frac{5}{6}\pi\right) & F_{coup} \cos\left(\theta + \frac{1}{2}\pi\right) \end{bmatrix} \quad (6.75)$$

Where F_{coup} is the maximum magnetic coupling coefficient between the rotor and stator, and α_{if} is the angle of the relative position between the stator and the rotor windings.

6.4.2 dq0 representation

dq0 is used to simplify the inductance matrix (6.73) and flux linkage from the permanent magnet rotor matrix (6.75) as shown in Section 6.1.3, The transformation matrix $C_{6 \times 6}$ is shown in equation (6.76) as represented in [19].

$$[C_{6 \times 6}] = \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix} \quad (6.76)$$

$$[C_{6 \times 6}] = \sqrt{\frac{3}{2}} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) & 0 & 0 & 0 \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 0 & 0 & 0 \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos\left(\theta - \frac{1}{6}\pi\right) & \cos\left(\theta - \frac{5}{6}\pi\right) & \cos\left(\theta + \frac{1}{2}\pi\right) \\ 0 & 0 & 0 & -\sin\left(\theta - \frac{1}{6}\pi\right) & -\sin\left(\theta - \frac{5}{6}\pi\right) & -\sin\left(\theta + \frac{1}{2}\pi\right) \\ 0 & 0 & 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \quad (6.77)$$

The inductance matrix can be transferred to dq0 frame as follows:

$$\begin{bmatrix} L_{dq01} \\ L_{dq02} \end{bmatrix} = \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix} \begin{bmatrix} L_{S1S1} & L_{S1S2} \\ L_{S2S1} & L_{S2S2} \end{bmatrix} \begin{bmatrix} C_1^T & 0 \\ 0 & C_2^T \end{bmatrix} \quad (6.78)$$

$$\begin{bmatrix} L_{dq01} \\ L_{dq02} \end{bmatrix} = \begin{bmatrix} C_1 L_{S1S1} C_1^T & C_1 L_{S1S2} C_2^T \\ C_2 L_{S2S1} C_1^T & C_2 L_{S2S2} C_2^T \end{bmatrix} \quad (6.79)$$

$$L_{dq0} = \begin{bmatrix} \frac{3}{2}L_m + L_s + M_s & 0 & 0 & \frac{3}{2}L_m & 0 & 0 \\ 0 & L_s - \frac{3}{2}L_m + M_s & 0 & 0 & -\frac{3}{2}L_m & 0 \\ 0 & 0 & L_s - 2M_s & 0 & 0 & -3M_s \\ \frac{3}{2}L_m & 0 & 0 & \frac{3}{2}L_m + L_s + M_s & 0 & 0 \\ 0 & -3M_s & 0 & 0 & L_s - \frac{3}{2}L_m + M_s & 0 \\ 0 & 0 & -3M_s & 0 & 0 & L_s - 2M_s \end{bmatrix} \quad (6.80)$$

Since the generator is surface mounted magnet type, the self-inductances of the windings in the quadrature and direct axes are the same ($L_{d1}=L_{d2}=L_d$, $L_{q1}=L_{q2}=L_q$ and $M_{s1s2}=M_{s2s1}$) [20]. Self-inductance coefficients can be defined as:

$$\text{Direct-axis synchronous inductance: } L_d = \frac{3}{2}L_m + L_s + M_s$$

$$\text{Quadrature-axis synchronous inductance: } L_q = L_s - \frac{3}{2}L_m + M_s$$

$$\text{Mutual inductance coefficient: } M_{s1s2} = \frac{3}{2}L_m$$

The permanent magnet rotor flux linkage matrix can transferred to the dq0 reference frame as:

$$\begin{bmatrix} \Psi_{sf_{d1q1}} \\ \Psi_{sf_{d2q2}} \end{bmatrix} = \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix} \begin{bmatrix} \Psi_{sf_{abc}} \\ \Psi_{sf_{xyz}} \end{bmatrix} \quad (6.81)$$

$$\begin{bmatrix} \Psi_{sf_{d1}} \\ \Psi_{sf_{q1}} \\ \Psi_{sf0} \\ \Psi_{sf_{d2}} \\ \Psi_{sf_{q2}} \\ \Psi_{sf0} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}}F_{coup} \\ 0 \\ 0 \\ \sqrt{\frac{3}{2}}F_{coup} \\ 0 \\ 0 \end{bmatrix} \quad (6.82)$$

The flux linkage matrix in the dq0 frame is shown in equations (6.83) and (6.84) .

$$[\Psi_{dq0}] = [L_{dq0}][i_{dq0}] + [\Psi_{sf(dq0)}] \quad (6.83)$$

$$\begin{bmatrix} \Psi_{d1} \\ \Psi_{q1} \\ \Psi_{o1} \\ \Psi_{d2} \\ \Psi_{q2} \\ \Psi_{o2} \end{bmatrix} = \begin{bmatrix} L_d & 0 & 0 & M_{s1s2} & 0 & 0 \\ 0 & L_q & 0 & 0 & -M_{s1s2} & 0 \\ 0 & 0 & L_0 & 0 & 0 & -3Ms \\ -M_{s1s2} & 0 & 0 & L_d & 0 & 0 \\ 0 & -M_{s1s2} & 0 & 0 & L_q & 0 \\ 0 & 0 & -3Ms & 0 & 0 & L_0 \end{bmatrix} \begin{bmatrix} i_{d1} \\ i_{q1} \\ i_{o1} \\ i_{d2} \\ i_{q2} \\ i_{o2} \end{bmatrix} + \begin{bmatrix} \sqrt{\frac{3}{2}}F_{coup} \\ 0 \\ 0 \\ \sqrt{\frac{3}{2}}F_{coup} \\ 0 \\ 0 \end{bmatrix} \quad (6.84)$$

$$\begin{bmatrix} \psi_{d1} \\ \psi_{q1} \\ \psi_{o1} \\ \psi_{d2} \\ \psi_{q2} \\ \psi_{o2} \end{bmatrix} = \begin{bmatrix} L_d i_{d1} + M_{s_1 s_2} i_{d2} + \sqrt{\frac{3}{2}} F_{coup} \\ L_q i_{q1} - M_{s_1 s_2} i_{q2} \\ L_0 i_{o1} - 3M_s i_{o2} \\ L_d i_{d2} + M_{s_1 s_2} i_{d1} + \sqrt{\frac{3}{2}} F_{coup} \\ L_q i_{q2} - M_{s_1 s_2} i_{q1} \\ L_0 i_{o2} - 3M_s i_{o1} \end{bmatrix} \quad (6.85)$$

6.4.3 Voltage equation in the dq0 frame

Equation(6.66) can transferred to the dq0 frame as shown in Sections6.1.3 and 6.2.3.

$$[V_{dq0}] = -[R][i_{dq0}] - \left(\psi_{dq0} \cdot \omega_{dq0} \right) \quad (6.86)$$

Where:

$$v_{dq0} = [v_{d1} \quad v_{q1} \quad v_{o1} \quad v_{d2} \quad v_{q2} \quad v_{o2}]^t$$

$$i_{dq0} = [i_{d1} \quad i_{q1} \quad i_{o1} \quad i_{d2} \quad i_{q2} \quad i_{o2}]^t$$

$$\begin{bmatrix} v_{d1} \\ v_{q1} \\ v_{o1} \\ v_{d2} \\ v_{q2} \\ v_{o2} \end{bmatrix} = \begin{bmatrix} -r i_{d1} - p \psi_{d1} + \omega_e \psi_{q1} \\ -r i_{q1} - p \psi_{q1} - \omega_e \psi_{d1} \\ -r i_{o1} - p \psi_{o1} \\ -r i_{d2} - p \psi_{d2} + \omega_e \psi_{q2} \\ -r i_{q2} - p \psi_{q2} - \omega_e \psi_{d2} \\ -r i_{o2} - p \psi_{o2} \end{bmatrix} \quad (6.87)$$

6.4.4 Torque equations

To complete the dual three-phase PMSG model, the electromagnetic torque is [21-23]:

$$T_e = \text{pole_pairs} (\psi_{d1} i_{q1} - \psi_{q1} i_{d1} + \psi_{d2} i_{q2} - \psi_{q2} i_{d2}) \quad (6.88)$$

6.4.5 Simulation results

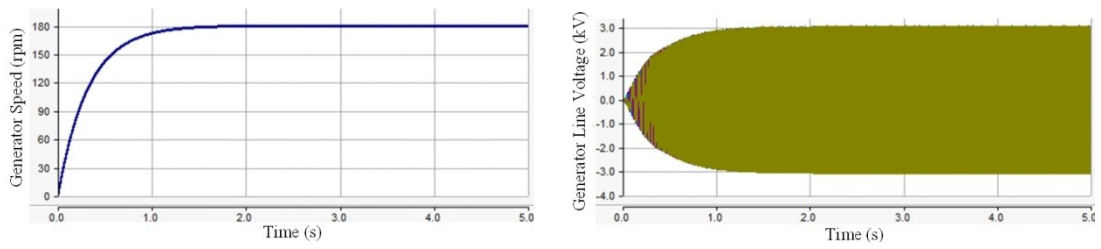
This subsection presents simulations to validate the PSCAD/EMTDC model of the dual three-phase PMSG. The PMSG model uses the generator rotor speed and input and output currents as feedback. A variable frequency PLL and transformation

matrix (6.76) is used to convert the generator output current from a phase variable representation to the dq0 reference frame. The generator output current in the dq0 frame is passed through a differential block in the simulation model to obtain $p[i_{dq0}]$, where ‘p’ represents the time derivative operation. The rotor speed, $[i_{dq0}]$ and $p[i_{dq0}]$ are substituted into equation (6.87) to give $[v_{dq0}]$. The inverting transformation $[C_{6 \times 6}]^T$, is used to convert the generator terminal voltages from the $[v_{dq0}]$ representation to the phase variable $[v]$ form.

For validation, the PMSG is connected to a resistive load of 4.356Ω per phase, which is equivalent to 5MW at rated voltage and speed, as shown in Table6.1 The generator rotor is connected to a prime mover providing an input mechanical torque of 0.265MNm. Figure 6.4 show waveforms summarizing the performance of the proposed dual three-phase PMSG model. Figure 6.4 (a) shows rotor speed and Figure 6.4 (b) and (c), shows detailed voltage waveforms, which confirm that the generator model provides a stable output voltage over the full operating range.

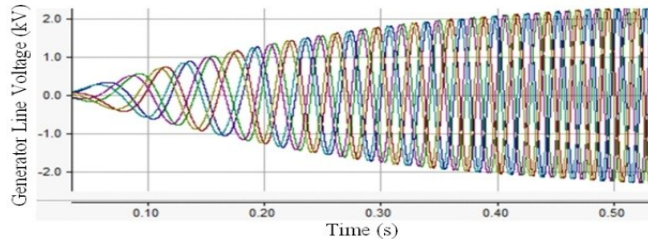
Table6.1 Dual three-phase PMSG parameters

Parameter	value
Rated power	5.2 MVA
Rated speed	180 rpm
Rated voltage	3.3 kV
Direct-axis inductance	0.008 H
Quadrature-axis inductance	0.008 H
Mutual inductance coefficient	0.001 H
Number of poles	34
Permanent magnetic flux	15 Wb



(a) Prime mover speed

(b) Generator output voltage, increasing with rotor speed



(c) Generator output voltage during start up: detailed waveforms

Figure 6.4 Waveforms showing overall performance of the dual three-phase PMSG model.

6.5. Wind turbine model and emulator

6.5.1 Wind turbine model

The wind turbine model, based on steady-state power characteristics, is described in [24]-[27]. The output aerodynamic power of the wind turbine is

$$P_{Turbine} = \frac{1}{2} \rho A C_p(\lambda, \beta) V^3 \quad (6.89)$$

Where ρ is the air density (1.225 kg/m^3), A is the rotor swept area (m^2), C_p is the power coefficient, V is the wind speed (m/s) and β is the blade pitch angle ($^\circ$). λ is the tip speed ratio(6.90):

$$\lambda = \frac{\omega_m R_t}{V} \quad (6.90)$$

Where ω_m is the rotor angular velocity (rad/s) and R_t is the rotor radius (m).

The power coefficient C_p is a nonlinear function of tip speed ratio λ and blade pitch angle β for a constant wind speed. The power coefficient C_p is maximum at λ_{opt} and is calculated using a generic equation as shown in (6.91) [28], where λ_i is defined by(6.92).

$$C_p = 0.5176 \times \left(\frac{116}{\lambda_i} - 0.4\beta - 5 \right) \times e^{\frac{-21}{\lambda_i}} - 0.006795\lambda_i \quad (6.91)$$

$$\lambda_i = \left[\frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1} \right]^{-1} \quad (6.92)$$

Figure 6.5 shows the power coefficient C_p and the tip speed ratio characteristics, for different pitch angle values. From Figure 6.5 C_{pmax} (the maximum value of C_p) is found to be 0.48 and $\lambda_{opt} = 8.1$ at $\beta=0$, meaning the power extracted from the wind is never greater than 48%. This is a consequence of aerodynamic losses which are dependent upon factors such as blade shape, weight and stiffness [24].

λ_{opt} can be used to determine the optimal turbine rotational speed ω_{opt} as shown in equation (6.93). ω_{opt} is a unique wind turbine parameter that gives maximum output power for a given wind speed. Thus, wind energy conversion system load control results in turbine rotor variable-speed operation such that maximum wind power is extracted continuously. This technique is known as maximum power point tracking (MPPT) control.

$$\omega_{opt} = \frac{V \lambda_{opt}}{R_t} \quad (6.93)$$

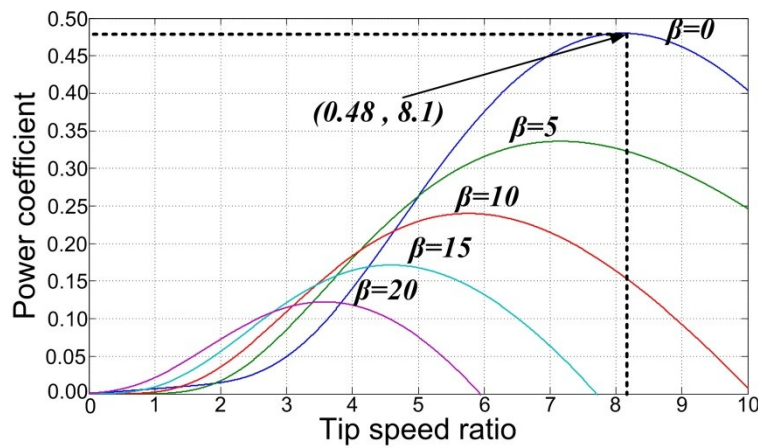


Figure 6.5 The C_p - λ characteristics, for different pitch angles.

6.5.2 Wind turbine emulator

The wind turbine emulator (WTE) is based on a microcontroller system and a separately-excited dc motor. The WTE can accurately reproduce the characteristics

of a real wind turbine by changing the produced dc motor torque and speed according to the wind turbine characteristics. To simplify WTE control, the dc motor field current is kept constant, to make the developed electromechanical torque (T_e) of the DC motor, only a function of the armature current (I_a). Equation (6.94) describes the developed electromechanical torque (T_e), with torque constant K .

$$T_e = KI_a \quad (6.94)$$

The WTE controller is shown in Figure 6.6, and developed according to:

- First the microcontroller detects motor armature current I_a and motor speed ω_m and divides the speed by the gear box ratio (GBR) to get the turbine shaft speed ω_t .
- According to the given wind speed and wind turbine model, the microcontroller calculates the corresponding turbine torque T_t .
- Turbine torque is divided by the GBR to get the reference dc motor torque T_m , which is converted to reference current I_{a_ref} by dividing by the dc motor constant K .
- The armature current error is passed through a proportional integral (PI) controller to get the reference armature voltage V_{a_ref} value.
- V_{a_ref} is an analog signal sent to the programmable dc power supply to supply the dc motor.

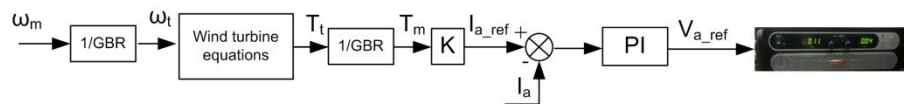


Figure 6.6 WTE control loop.

6.6. Summary

This chapter considered modelling of a three-phase synchronous generator and a dual three-phase PMSG based on Park's transformation. Then three-phase synchronous generator model and dual three-phase PMSG were discussed.

The last section of this chapter discussed the wind turbine model, showing how to obtain the optimal wind turbine speed for any wind speed. The proposed wind turbine emulator based on microcontroller system and a separately-excited dc motor, was presented. This wind turbine emulator is to be used in the experimental prototype of the proposed wind energy conversion systems, discussed in chapter seven.

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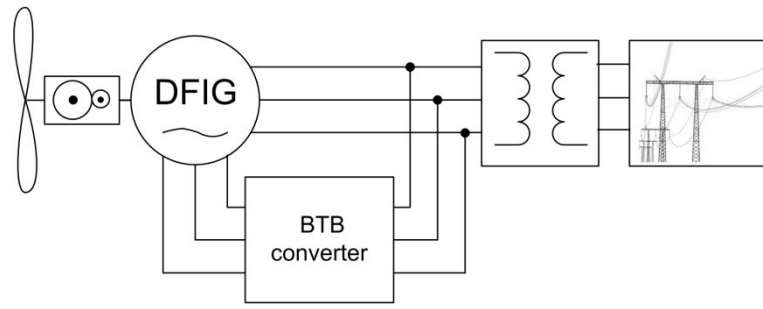
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Chapter 7. Proposed Wind Energy Conversion System

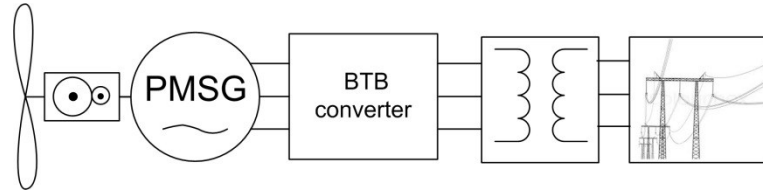
This chapter proposes three different variable speed wind energy conversion systems (WECS) that employ current source converters for interfacing between a wind generator and the grid. The proposed WECSs employ different variants of the buck-boost discussed in Chapter five. The generator side converter produces variable voltage and frequency with maximum power capturing. On the grid side, six-pulse and dual six-pulse current converters inject the generated power into the grid. The proposed WECSs offer all the features of the voltage source converter based systems such as voltage control, fault ride-through capability, and maximum power-point tracking (MPPT). These features are achieved with increased reliability and improved ac side current and voltage waveform quality, and with a reduced switching frequency. The validity of the proposed WECS is confirmed using simulations and experimentation, and major findings are highlighted.

7.1. Background

Wind energy is a growing and promising renewable energy source for small and large-scale energy harvesting. WECS can be classified into two types: fixed-speed and variable-speed. However, variable speed is preferred because it allows maximum power extraction as the wind speed varies [1, 2]. Traditionally, variable speed WECSs employ fractionally or fully rated back-to-back (BTB) converters to form the doubly fed induction generator (DFIG) or the electrically excited (or permanent magnet) synchronous generator as shown in Figure 7.1. The fully rated converter type decouples the grid side from generator side because of a dc link shunt capacitor in the voltage source converter system or the series inductor in the current source converter counterpart [3].



(a) WECS based on a fractionally rated BTB converter.



(b) WECS based on a full-rated BTB converter.

Figure 7.1 Variable-speed drive based WECS.

7.2. First proposal WECS (Dual three-phase PMSG, dual-bridge CSR and dual-bridge CSI)

Figure 7.2 shows the first WECS proposal, where both the current source rectifier and the inverter are controlled using selective harmonic elimination (SHE) in order to achieve low-loss operation. The CSI is connected to the grid through a three-winding phase shifting transformer to benefit from harmonic cancellation on the grid side (primary winding), where the secondary and tertiary windings are delta (Δ) and wye (Y) connected respectively[4]. Thus with SHE eliminating the 11th and 13th harmonics, the converter switching devices operate at a low switching frequency. SHE PWM is utilised on the CSR to provide a superior harmonic profile with minimal switching losses over a wide frequency range. The inductance between the generator side converter and the grid side converter allows placing of the heavy equipment (grid-side transformer, CSI, and dc-link inductance) at the bottom of the wind turbine tower, for ease of installation and access. The WECS is modelled in PSCAD/EMTDC, and incorporates MPPT and reactive power control. A three-bladed horizontal-axis wind turbine with no blade pitch angle control ($\beta=0$) is considered.

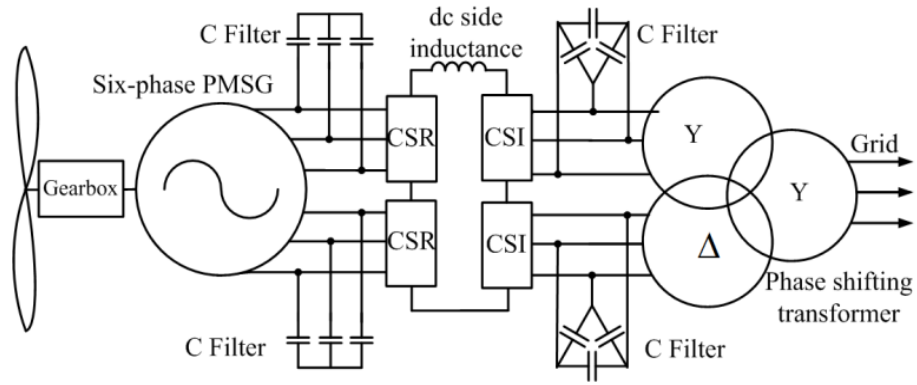


Figure 7.2 First proposal WECS.

7.2.1 Control strategy

Since the wind turbine gives it maximum output power at optimal speed ω_{op} , equation (7.1) is used to determine the optimal turbine speed at each wind speed [5, 6]. Thus, WECS load control results in variable-speed operation of the turbine rotor such that maximum power is extracted continuously from the wind (maximum power point tracking (MPPT) control).

$$\omega_{opt} = GBR \frac{V \lambda_{opt}}{R_t} \quad (7.1)$$

Where GBR is the gear box ratio, V is wind speed (m/s), λ_{opt} is the optimal tip speed ratio and equals to 8.1 as discussed in Chapter 6, and R_t is rotor radius (m).

i. Generator side converter

The generator side converter consists of two identical current source rectifiers (CSR) connected in series, in which SHE eliminates the 11th and 13th harmonics to ensure that the proposed WECS exchanges sinusoidal current from the dual three-phase PMSG with minimum pulsating torque and at a low switching frequency. A Weighted Least-Squares Estimation (WLSE) is used to detect the generator output voltage, frequency, and phase shift [7, 8].

The dual CSRs have two main control loops, where the first is the MPPT control loop, shown in Figure 7.3, which forces the wind turbine to operate at optimal speed. The system operating sequence is as follows: the controller detects the wind speed and calculates the corresponding optimal turbine speed ω_{opt} according to (7.1).

Multiplying this speed by the gearbox ratio gives the optimal generator speed ω_{G_opt} . The dc-link inductor reference current I_{Ldc_ref} is obtained from the speed controller which forces the generator speed ω_G to follow ω_{G_opt} . A proportional-integral (PI) speed controller is used. I_{L_ref} is passed to an inner controller that regulates inductor current I_{Ldc} and estimates the modulation index m for both CSR converters. Any change in the dc side inductor current changes the PMSG electromagnetic torque T_e which, in turn, changes the turbine speed.

The second control loop, in Figure 7.3, controls the generator power factor, that is, the reactive power exchange with the dual CSR converters. This controller is used to estimate angle α which is added to angle ωt , derived from the phase locked loop (PLL), to give the reference angle required by the SHE gate signal generator.

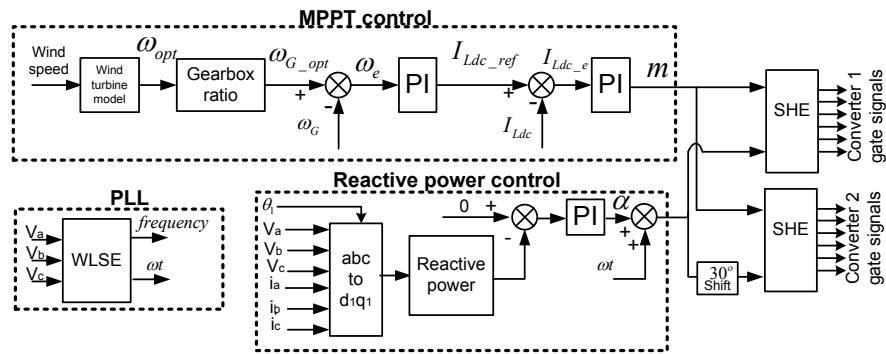


Figure 7.3 Control strategy of the first WECS proposal.

ii. Grid side converter

The grid side converter uses dual three-phase current source inverters (CSI) with a three-winding phase shifting transformer, see Figure 7.2. This transformer cancels the 5th, 7th, 17th, 19th, 27th, 31st, etc. harmonic currents [4]. The control switching patterns provided to the inverters eliminate the 11th and 13th harmonics, meaning that for a 50Hz supply, the converter switches operate at a low switching frequency of approximately 350Hz. The combination of sinusoidal current, low switching frequency and reliable high-voltage operation offered by the proposed configuration makes it particularly suited to high-power applications. The dual CSI controller operates so as to enable all of the generator output power to be injected into the grid, and to regulate the dual CSI reactive power exchanged with the grid. The dual CSI does not need to control active power since this is already controlled by adjusting the

dc-link inductor current using the generator side converter. This makes the proposed WECS both simple and easy to control.

7.2.2 Simulation results

The system parameters used in the simulation study are given in Table 7.1. The system is simulated and assessed at initial wind speed of 8m/s, which undergoes a step increase to 12.5m/s and then a step decrease to 10m/s, thus enabling examination of the dynamic performance and stability of the proposed system. According to (7.1), the optimal generator speed at each wind speed are 114.5rpm, 178.8rpm and 143rpm respectively, and the corresponding maximum generator output powers are 1.37MW, 5.26MW and 2.7MW.

Figure 7.5(a) shows that the WECS operates under optimal conditions with minimum transients at wind speed changes. Figure 7.5(b) shows the measured and reference dc side inductor currents. As the wind speed changes from 8m/s to 12.5m/s, the controller decreases the reference current to decrease the electromagnetic torque. Thus the wind turbine speed increases rapidly and vice versa during the wind speed decrease from 12.5m/s to 10m/s. Figure 7.5(c) illustrates generator output power, showing the proposed WECS tracks maximum power at different wind speeds. Figure 7.5(a) and (b) show that the dual CSI injects sinusoidal currents into the grid at unity power factor, and that voltage and current ripple are both low.

Table 7.1 First proposed WECS simulation setup parameters.

Dual three-phase PMSG Parameters	
Rated power	5.2 MVA
Rated speed	180 rpm
Rated voltage	3.3 kV
Direct-axis inductance	0.008 H
Quadrature-axis inductance	0.008 H
Mutual inductance coefficient	0.001 H
Number of poles	34
Permanent magnetic flux	15 Wb
Wind Turbine Parameters	
Rated power	5.2 MW
Cut-in wind speed	4 m/s
Rated wind speed	12.5 m/s
Cut-out wind speed	25 m/s
Rotor diameter	108 m
Rotor area	9160 m ²
Gearbox ratio	1:10
Converter Parameters	
Dual CSR C-filter	220 μ F (Y connection)
DC side inductance	20 mH
Dual CSI C-filter	30 μ F (Δ connection)
Phase-shifted transformer rated power	5.2 MVA
Phase-shifted transformer rated voltage	3.3 kV

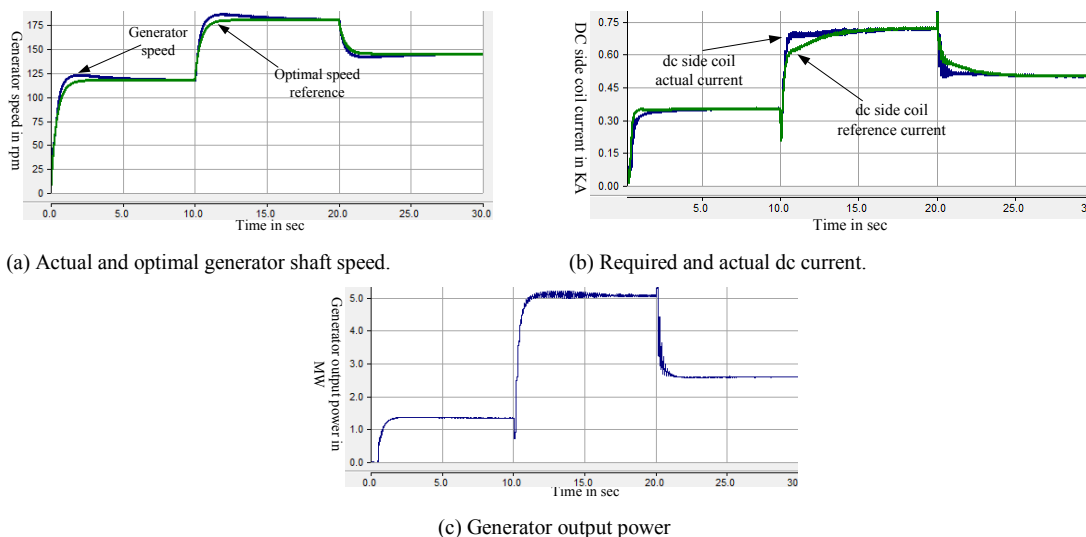
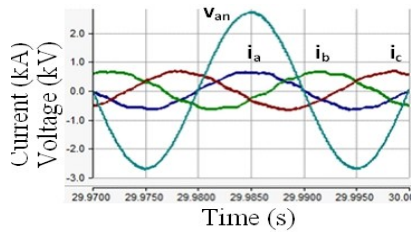
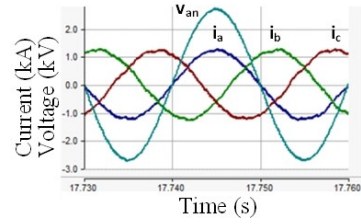


Figure 7.4 Waveforms of the overall performance of the first WECS proposal.



(a) Grid voltage and current at $V=10$ m/s



(b) Grid voltage and current at $V=12.5$ m/s

Figure 7.5 Waveforms of the dual-bridge CSI grid delivered current.

7.2.3 Experimental Validation

Figure 7.6 shows the scaled down experimental WECS based on a 2kVA dual CSI, which is operated at a constant modulation index ($m=1$) and unity power factor, with the controller forcing the dual CSI reactive power output to zero. Figure 7.7 shows sample gating signals supplied to the dual CSI that contain seven pulses per fundamental (50Hz) cycle, such that each device operates with a switching frequency of 350Hz. Figure 7.8 shows that phase ‘a’ of the grid voltage and dual CSI phase ‘a’ output current are in phase, confirming zero reactive power transfer and that sinusoidal current is injected into the grid

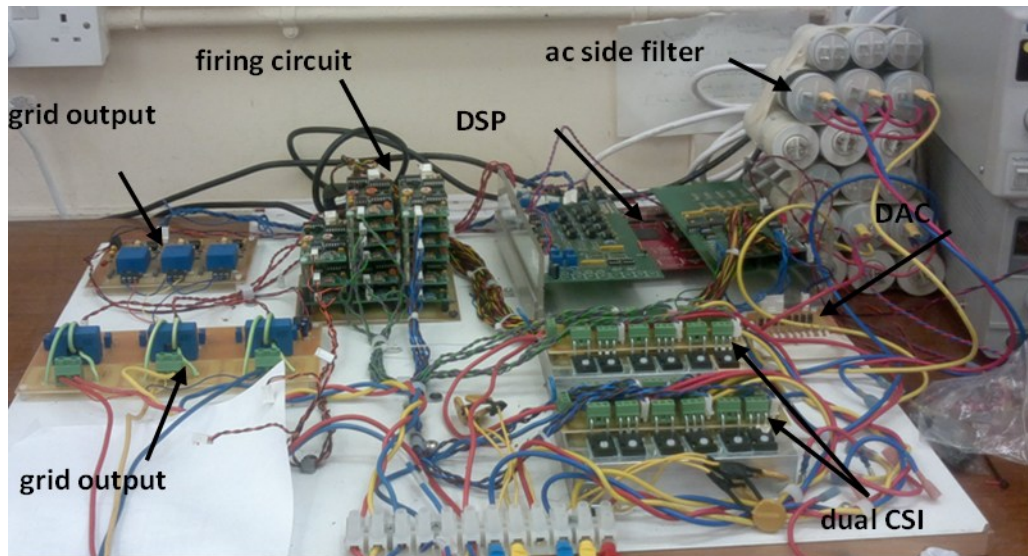


Figure 7.6 First proposal experimental test rig.

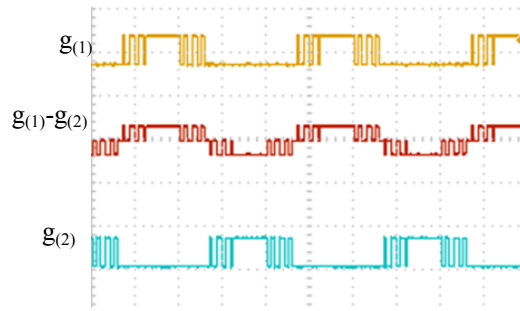


Figure 7.7 CSI 1: gate 1 (g_1) and gate 4 (g_4) signals.

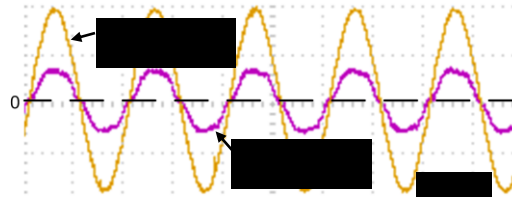


Figure 7.8 Experimental results for the proposal dual-bridge CSI (Phase 'a' grid voltage and dual CSI phase 'a' output current)

7.3. Second proposal WECS (Three-phase PMSG and the current source based three-phase BTB converter)

Figure 7.9 shows the second proposed variable speed WECS based on the three-phase BTB current source converters proposed in Chapter 5.

7.3.1 Control strategy

There are two main control loops: 1st MPPT controller and 2nd grid reactive power controller.

i. Maximum power point tracking controller

The proposed MPPT control loop consists of two control loops, (inner and outer), as shown in Figure 7.9. The outer control loop detects the wind speed and uses equation (7.1) to calculate the corresponding optimal generator speed ω_{opt} . The speed regulator based on proportional-integral (PI) control estimates the reference average dc-link inductor current $\overline{I_{L,ref}}$ for the inner control loop. The inner controller, which regulates $\overline{I_L}$, and estimates the duty cycle δ for switch S_r , necessary to control the power flow from the wind generator into the grid, as will be illustrated in the subsequent analysis.

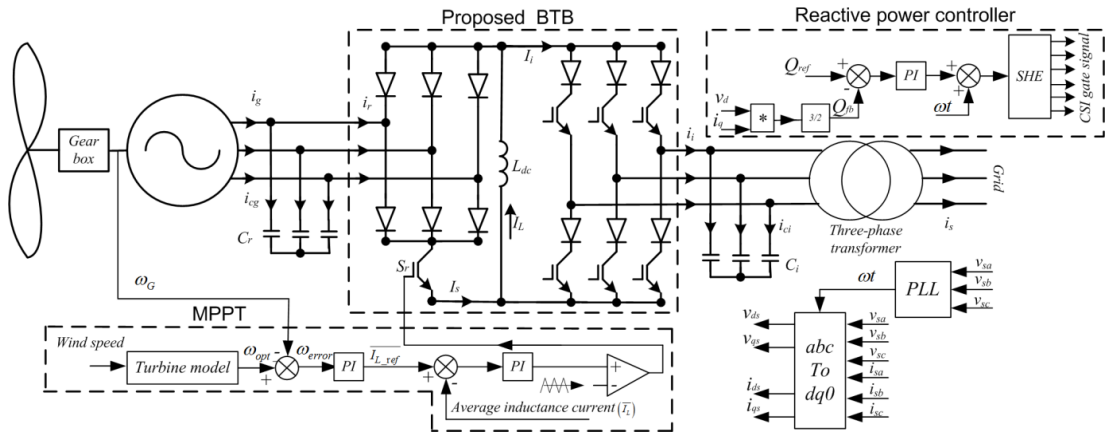


Figure 7.9 Second WECS proposal, with maximum power point tracking control loop.

The starting point to establish the relationship between the powers delivered to the grid and the dc-link inductor current \bar{I}_L , and the relation between the dc-link inductor current I_L and generator current, is the active and reactive powers P_g and Q_g :

$$P_g = \frac{3}{2} i_{ds} v_{ds} \quad (7.2)$$

$$Q_g = \frac{-3}{2} i_{qs} v_{ds} \quad (7.3)$$

Where v_{ds} is the d component of the grid voltage (V_s), assuming the grid voltage vector is aligned with the d -axis ($v_{qs}=0$), and i_{ds} , i_{qs} are d and q current components that the current grid side converter inject into grid.

Based on Figure 7.10, the steady state equations that describe the ac side of the grid side converter are:

$$v_{cid} = R_s i_{sd} - \omega_s L_s i_{sq} + v_{sd} \quad (7.4)$$

$$v_{ciq} = R_s i_{sq} + \omega_s L_s i_{sd} \quad (7.5)$$

Where L_s and R_s are the transformer leakage inductance and resistance, and v_{cid} and v_{ciq} are the d and q components of the grid side filter capacitor voltage. Similarly, the filter capacitor current i_{ci} is:

$$i_{cid} = -\omega_s C_i v_{ciq} \quad (7.6)$$

$$i_{ciq} = \omega_s C_i v_{cid} \quad (7.7)$$

The current provided by the CSI i_i is the sum of the grid current i_s and the capacitor C_i current i_{ci} . The CSI output current i_i is:

$$i_{di} = (1 - \omega_s^2 C_i L_s) i_{sd} - \omega_s C_i R_s i_{sq} \quad (7.8)$$

$$i_{qi} = (1 - \omega_s^2 C_i L_s) i_{sq} + \omega_s C_i (v_{sd} + R_s i_{sd}) \quad (7.9)$$

For modulation index $m=1$, as being considered here, the average current at the CSI input \bar{I}_i equals the peak fundamental current of I_{mi} (recall $I_{mi} = m\bar{I}_i$). The following equations result:

$$I_{mi} = \sqrt{(i_{di}^2 + i_{qi}^2)} \quad (7.10)$$

$$\bar{I}_i = I_{mi} = \sqrt{\left((1 - \omega_s^2 C_i L_s) i_{sd} - \omega_s C_i R_s i_{sq} \right)^2 + \left((1 - \omega_s^2 C_i L_s) i_{sq} + \omega_s C_i (v_{sd} + R_s i_{sd}) \right)^2} \quad (7.11)$$

Assuming that the grid reactive power controller operates at unity power factor, $i_{qs}=0$, equation (7.11) reduces to:

$$\bar{I}_i = \sqrt{\left(1 - \omega_s^2 L_s C_i \right)^2 i_{ds}^2 + \omega_s^2 C_i^2 (v_{ds} + R_s i_{ds})^2} \quad (7.12)$$

Since the current entering the CSI I_i equals the dc-link inductor current I_L when the switch S_r is off, the average dc-link inductor current \bar{I}_L can be obtained from (7.13) :

$$\bar{I}_L = \frac{1}{(1-\delta)} \bar{I}_i \quad (7.13)$$

Substitute (7.13) into (7.12) gives:

$$\bar{I}_L = \frac{1}{(1-\delta)} \sqrt{\left(1 - \omega_s^2 L_s C_i \right)^2 i_{s(d)}^2 + \omega_s^2 C_i^2 (v_{s(d)} + R_s i_{s(d)})^2} \quad (7.14)$$

Combining equation (7.2) ($i_{ds} = \frac{P_g}{1.5v_{dc}}$) and (7.14) gives:

$$\bar{I}_L = \frac{1}{(1-\delta)} \sqrt{\left(1 - \omega_s^2 L_s C_i \right)^2 \left(\frac{P_g}{1.5v_{s(d)}} \right)^2 + \omega_s^2 C_i^2 \left(v_{ds} + R_s \frac{P_g}{1.5v_{s(d)}} \right)^2} \quad (7.15)$$

Equation (7.15) describes the relationship between \bar{I}_L , and δ (switch S_r duty cycle) and active power P_g delivered to the grid.

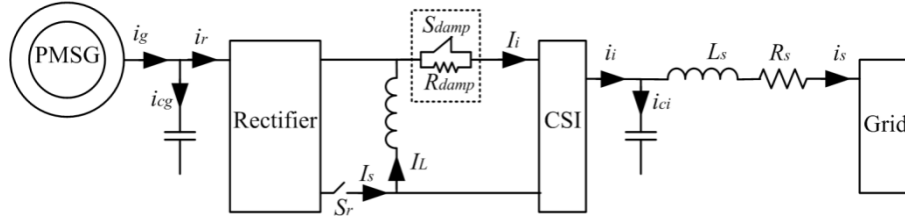


Figure 7.10 Single line diagram representation of the second WECS proposal.

Furthermore, the effect of varying δ (switch S_r duty cycle) on the average dc-link inductor current \bar{I}_L and generator current i_g can be established.

The generator side C-filter currents:

$$i_{cg(d)} = C_g(pv_{gd} - \omega_e v_{gq}) \quad (7.16)$$

$$i_{cgd} = C_g(pv_{gq} - \omega_e v_{gd}) \quad (7.17)$$

The rectifier input current is obtained by subtracting the capacitor current from the generator current. The steady state rectifier input current is shown in equations (7.18) and (7.19).

$$i_{rd} = i_{gd} + \omega_e C_g v_{gq} \quad (7.18)$$

$$i_{rq} = i_{gq} - \omega_e C_g v_{gd} \quad (7.19)$$

The peak fundamental rectifier input current can be calculated from:

$$I_{r(p)} = \sqrt{(i_{rd}^2 + i_{rq}^2)} \quad (7.20)$$

The spectrum of the rectifier input current i_R shown in Figure 7.11 can be obtained using the double Fourier series in complex form [9]:

$$i_{r(m,n)} = \frac{1}{2\pi^2} \left[\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} \int_{-\delta\pi}^{\delta\pi} I_L e^{j(mx+ny)} dx dy + \int_{\frac{7\pi}{6}}^{\frac{11\pi}{6}} \int_{-\delta\pi}^{\delta\pi} I_L e^{j(mx+ny)} dx dy \right] \quad (7.21)$$

Where $y=\omega_0 t$ and $x=\omega_c t$, ω_0 and ω_c respectively represent fundamental and carrier frequencies in rad/s, and m and n respectively are the orders of the carrier and baseband component harmonics. As described in Chapter four, the rectifier input fundamental component peak I_{rp} is:

$$I_{rp} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \quad (7.22)$$

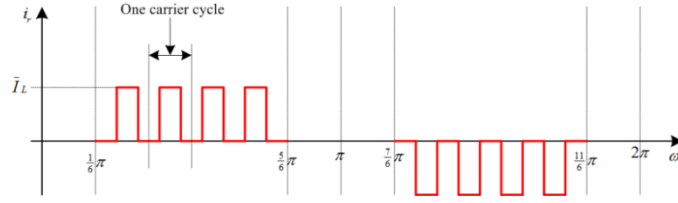


Figure 7.11 Rectifier input current within one carrier cycle.

After combining(7.18), (7.19), (7.20), and (7.22):

$$\bar{I}_L = \frac{\pi}{2\sqrt{3}\delta} \sqrt{(i_{g(d)} + w_e C_g v_{g(q)})^2 + (i_{g(q)} - w_e C_g v_{g(d)})^2} \quad (7.23)$$

From this analysis, the average dc-link inductor current \bar{I}_L is controlled by changing the duty cycle δ of switch S_r . Increasing the duty cycle δ will increase \bar{I}_L , hence according to equations (7.20) and (7.22) the generator current will increase which will tends to increase the electromagnetic torque and decrease the turbine speed. Also according to equation (7.23), the active power delivered to the grid will increase. Decreasing the duty cycle δ has the inverse effect.

ii. Grid reactive power controller

The reactive power controller in Figure 7.9 is used to adjust the phase angle α between the grid voltage and current vector. The CSI injects into the grid, based on the reactive power demand set point Q_{ref} . Therefore, the required phase angle α for arbitrary reactive power is estimated using PI control as:

$$\alpha = k_{pQ}(Q_{ref} - Q) + k_{iQ} \int (Q_{ref} - Q) dt \quad (7.24)$$

Where k_{pQ} and k_{iQ} are the proportional and integral gains of the reactive power controller. The estimated phase angle α from (7.24) is added to angle ωt from the phase locked loop (PLL), and the resultant angle $\omega t + \alpha$ is used to provide the SHE algorithm time base. Calculation of α based on (7.24) is not the same as the CSI load angle Δ , which is given by (7.25). Δ is set indirectly by the amount of active power CSI exchanges with the grid.

$$\Delta = \tan^{-1}\left(\frac{i_{id}}{i_{iq}}\right) = \tan^{-1}\left(\frac{(1 - \omega_s^2 L_s C_i) i_{ds}}{\omega_s C_i (v_{ds} + R_s i_{ds})}\right) \quad (7.25)$$

7.3.2 Simulations

Table 7.2 summarises parameters used in simulations and experimental test rig of the second proposed WECS, Figure 7.9.

Table 7.2 Simulation and experimental system parameters of the second WECS.

	Simulation	Experimentation
Wind turbine parameters		
Rated power	0.52MW	2kW
Rated wind speed	12.5m/s	12.5m/s
Cut-in wind speed	4m/s	4m/s
Cut-out wind speed	25m/s	25m/s
Rotor diameter	1.8m	1.8m
Rotor area	10178m ²	10.2m ²
Gearbox ratio	1:5.7	1:2.8
Grid parameters		
Voltage	3.3kV L-L	140V L _L
Frequency	50Hz	50 Hz
Grid connected transformer		
Power	0.5MW	2.0kW
Voltage	3.3/1.65 kVL-L	400/200V L-L
Generator parameters		
Rated power	0.51MW	6.0kW
Synchronous inductance	20mH	35mH
Number of Poles	20	4
Converter parameters		
Generator side Capacitor	200μF Y connected	150μF Y connected
dc-link inductance	10mH	12.5mH
Grid side capacitor	250 μF Y connected	100 Δ connected
Rated power	0.55MW	2kW
Rated reactive power	0.15MVAr	100VAr

i. Normal operation

To assess the dynamic performance of the proposed WECS, its illustrative version in Figure 7.9 is simulated using PSCAD/EMTDC. The wind speed is varied from 6m/s to 10m/s through intermediate steps of 8m/s and 12.5m/s, and the results are shown in Figure 7.12 and Figure 7.13. Figure 7.12(a) shows the wind PMSG generator speed follows the optimal speed provided by MPPT, as the wind speed varies. Figure

7.12(b) is a detailed view of the generator speed during the wind speed transition from 8m/s to 12.5m/s, where the generator speed is able to track optimal values, with minimal transient and time lag. The steady-state error between the measured and optimal speed is less than 1%. The two speeds converge slowly after several seconds due to large inertia of the wind turbine generator. Figure 7.12(c) shows the power the CSI exchanges with the grid as the wind speed varies according to the given profile. Figure 7.12(d) is a detailed view of the power plot in Figure 7.12(c), focused around the wind speed transition from 8m/s to 12.5m/s. The proposed WECS controller decreases the grid power to decrease the mechanical torque provided by the generator during the wind speed change from 8m/s to 12.5m/s. Decreasing the generator torque allows the wind turbine to speed up and decrease the transient time during the speed change.

Figure 7.13 is a detailed view of the grid currents and phase 'a' voltage during the wind speed profile, where the proposed WECS produces sinusoidal currents into the grid with near unity power factor over the range considered. At low wind speed, the power factor is lower, as expected for light loads.

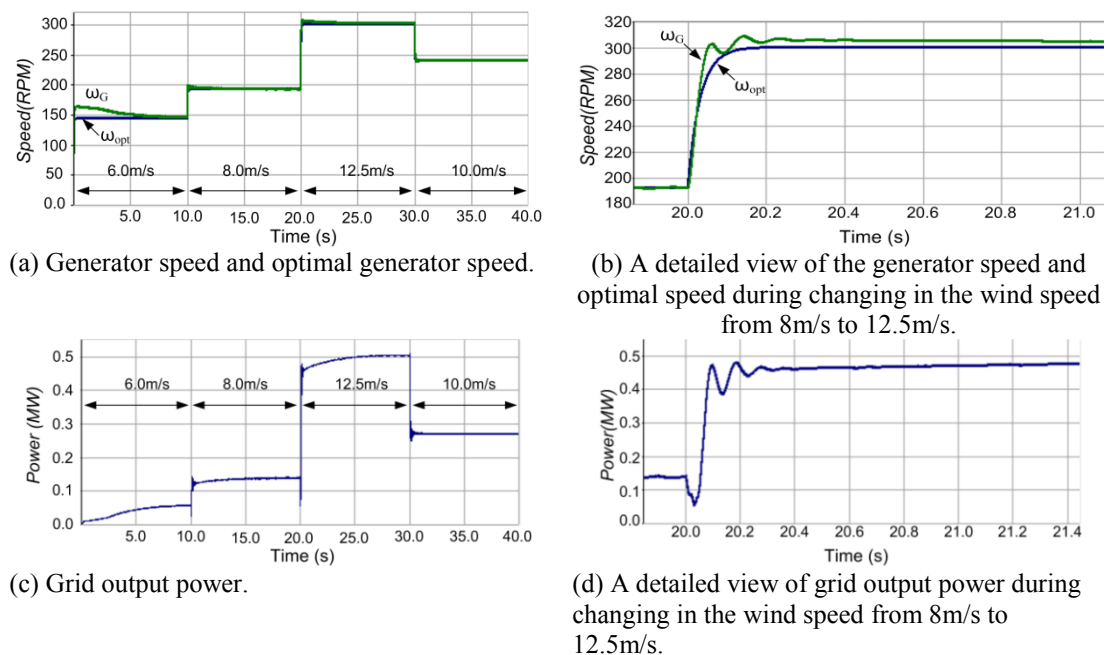


Figure 7.12 Simulation waveforms of generator speed and grid output power.

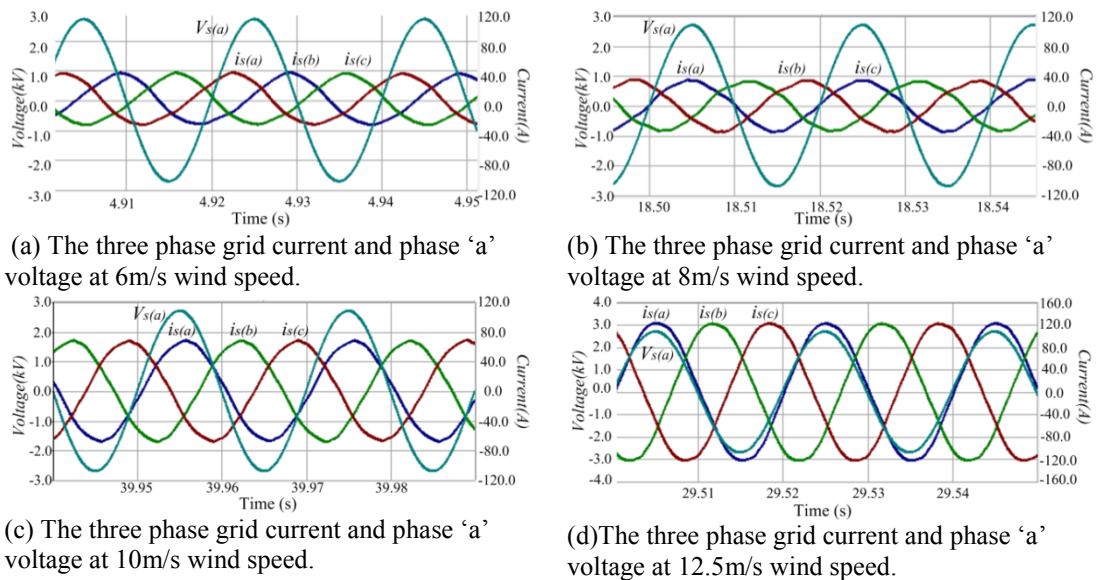


Figure 7.13 Simulation of grid current and phase 'a' voltage for the wind speed profile.

ii. Low voltage ride-through (LVRT) illustration

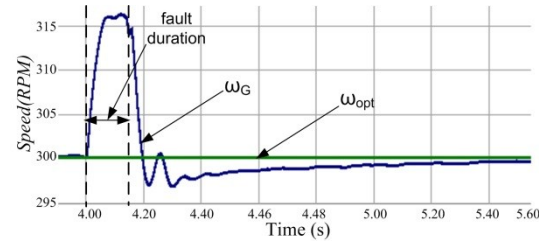
This subsection investigates the fault ride-through capability of the proposed WECS during an ac network fault. During the grid fault, the grid voltage collapses to 10% of its rated value. In most grid codes, such as the GB's, there is requirement that the wind turbine remains connected to the grid and supplies full reactive current[10]. As a result, the CSI cannot deliver to the grid the active power produced by the wind turbine. This will create a significant 'power imbalance between the CSI ac and dc sides that could cause a massive increase in the dc-link inductor current I_L . Such over-current may damage the CSI. Any pitch control will be too slow to be effective, and the excess energy results in a speed increase as excess energy is initially stored in the turbine inertia. Alternatively or additionally, in an attempt to improve the resiliency of the proposed WECS to such faults, the power dissipation mechanism consists of a resistor with a power electronics shunting switch, as shown in Figure 7.10. (A shunt dumping circuit parallel to L_{dc} is an alternative, with lower losses.) During normal operation switch (S_{damp}) is used to bypass the damping resistance R_{damp} . During grid short circuit, the WECS dissipates some energy in the damping resistor R_{damp} and temporary stores the rest in the turbine-generator mechanical system inertia, while the dc-link inductors current I_L is restrained by the following LVRT mechanism:

- In the charging mode, if the dc-link inductor current I_L reaches its maximum limit, the switch S_r (the pre-existing switch in the CSR) is turned off until the current I_L reaches the lower boundary of the charging current.
- In the discharge mode, if the dc-link inductor I_L reaches its upper limit, the switch S_{damp} is turned off to insert the resistor R_{damp} into the conduction path, preventing I_L from increasing, thus protecting the CSI from over current. Whence the system is protected.

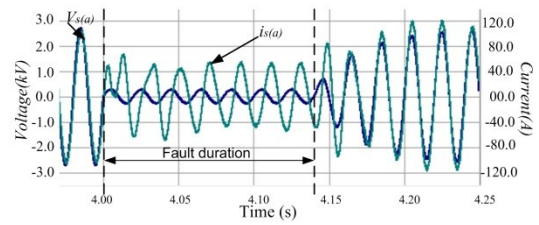
Although the proposed LVRT technique is simple, easy to implement, with high reliability and durability, it has the following drawbacks: extra hardware and continuous conduction losses in the switch S_{damp} under normal operation. Another solution is to control the dc-link current by controlling the grid side converter as shown in [11].

In this simulation section, the proposed LVRT technique is tested during a three-phase grid short circuit close to the PCC, with a 140ms fault duration. The proposed BTB will supply the grid with full rated reactive current. When the need for LVRT is detected, the control operation is modified as follows: 1) the upper and lower current limits for the switches S_r and S_{damp} are set to 0.37kA and 0.35kA. This allows control of the average dc-link inductor current to be coordinated between switches S_r and S_{damp} . 2) An additional controller is dedicated to adjusting the CSI modulation index and phase angle in order to regulate its reactive current injection into the grid during the short circuit (this controller operates only when a grid short circuit is detected). Figure 7.14(a) shows the temporary generator over-speed (5%) as the three-phase ac fault creates power imbalance between the ac and dc sides. The active power that cannot be transferred into ac side is absorbed by the mechanical inertia of the wind-turbine generator. As the grid voltage recovers when the fault is cleared, the controller slows the generator speed to the optimal speed. Figure 7.14(b) shows that the proposal WECS supplies the grid with full rated reactive current during the LVRT period and is able to redeliver controlled active power in a short time. Figure 7.14(c) shows that the wind turbine torque decreases when the generator speed increases during the grid fault. Figure 7.14(d) shows that the grid power drops to zero during the grid fault and build up when the grid recovers. Figure 7.15 shows

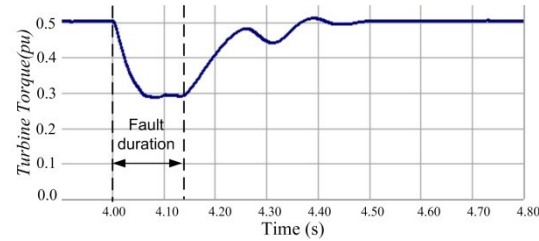
waveforms that summarize the performance of the proposed current limiter. From Figure 7.15(a), the proposal LVRT technique regulates the dc-link inductor current I_L within the desired limits during the grid fault. Figure 7.15(b) shows the current in the LVRT resistor. Figure 7.15(c) shows that the grid q-component current is increased to the rated value during the fault and decreases when the fault is cleared.



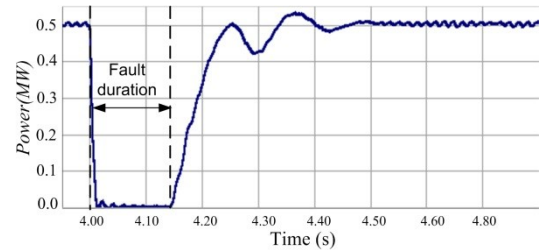
(a) Generator speed during grid fault and recovery.



(b) Grid phases 'a' voltage and current during grid fault and recovery.

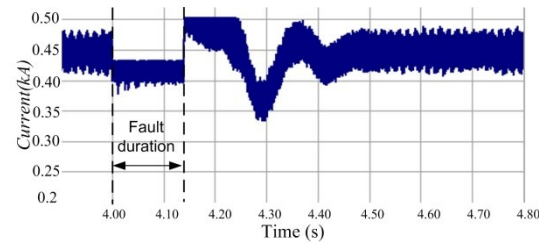


(c) Turbine torque during grid fault and recovery, pu.

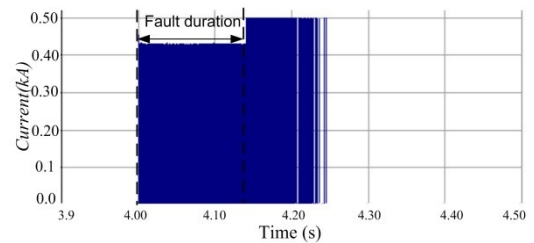


(d) Grid active power during grid fault and recovery.

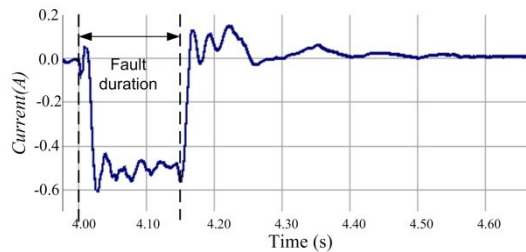
Figure 7.14 Performance waveforms of the proposed WECS during a LVRT condition.



(a) dc-link inductor current during the grid fault.



(b) LVRT resistor current during the grid fault.



(c) Grid q-component current during the grid fault

Figure 7.15 Waveforms of the dc-link current during a LVRT condition.

7.3.3 Experimental Results

This section presents experimental evaluation of the second WECS proposal, with emphasis on its steady state and dynamic performance. The ability to MPPT is assessed by varying the wind speed in four steps (6m/s, 10m/s, 8m/s and 9m/s), where each step is maintained for 40s. Figure 7.16 show the WECS test rig, which consists of five main parts.

1. Programmable dc supply: used to provide adjustable dc voltage to supply the dc motor, the reference dc voltage signal is received from the wind turbine emulator controller.
2. Motor generator set: consist of a separately excited dc motor acting as a prime mover for the three-phase synchronise generator, where the field current of the synchronous generator is fixed to make it operate as PMSG.
3. Grid connected transformer: to isolate the WECS from the grid.
4. Three-phase supply: provides an adjustable three-phase supply, representing the grid.
5. WTE controller: two functions, first: makes the dc motor behave like a real wind turbine, by detecting motor speed and current then applying the wind turbine equations to provide the reference voltage to the programmable dc supply. Second, it sends the wind speed to the BTB converter and controller.
6. BTB converter and controller: consists of the proposed BTB converter circuit shown in Figure 7.16 and the controller reads the grid current, grid voltage and wind speed then applies MPPT and reactive power control.

The results are displayed in Figure 7.17 to Figure 7.20. Figure 7.17(a) shows the optimal speed and generator speed, and active power the CSI delivers into the grid. The proposed controller tracks the optimal speed at different wind speeds, with minimum over/under shoot, and with smooth active power changes delivered to the grid as the wind speed varies. Figure 7.17(b) shows dc-link inductor current I_L , switch current I_S and CSI dc input current I_i , at 8m/s wind speed. The dc-link inductor current I_L is the switch current when the switch S_r in on and is the CSI input current I_i when the switch S_r in off. Figure 7.18 shows snapshots of the output grid current and phase 'a' voltage at different wind speeds, where Figure 7.18 and Figure

7.19 show that the proposed WECS supplies power to the grid, with high quality sinusoidal current, and the reactive power controller is able to regulate the reactive power injection into the grid, at zero. However, the power factor is less than unity in case in Figure 7.18(a) as the filter size used at the input of the CSI is extremely large and the active power from the turbine is low. Figure 7.20(c) and (d) show that the generator currents at 9m/s and 10m/s wind speed have different magnitudes and frequencies, as expected.

The simulation and experimental results presented in section 7.3.2 and 7.3.3 show that the proposed BTB topology is suitable for wind energy conversion systems, as it allows proper system operation with a fixed frequency at the grid side and variable frequency at the generator side.

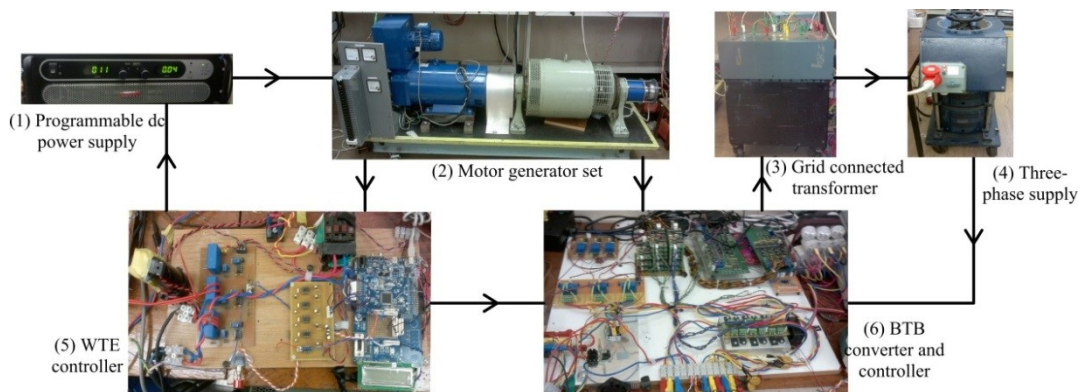


Figure 7.16 Second proposed WECS test rig

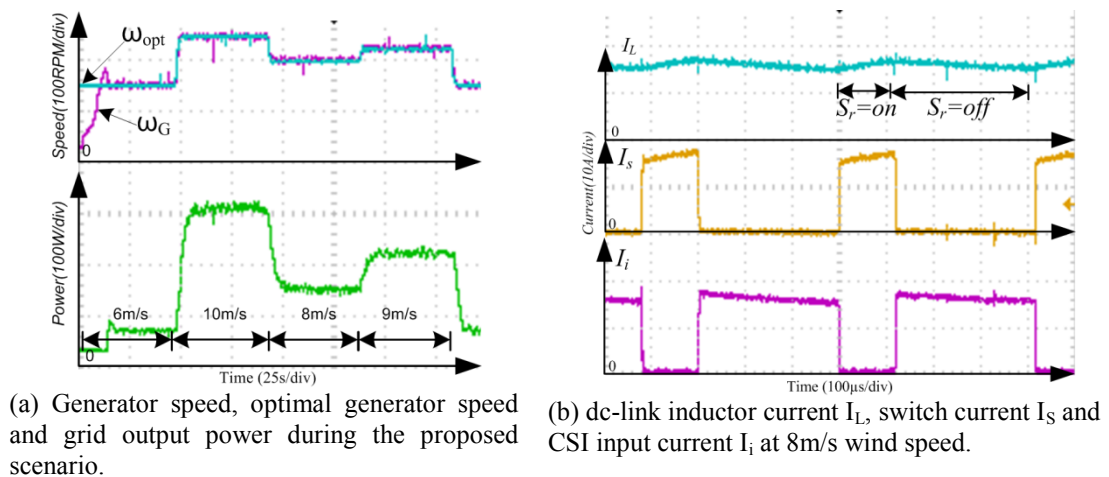
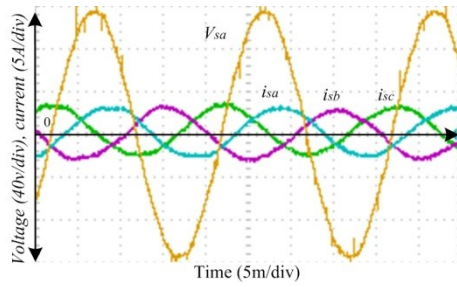
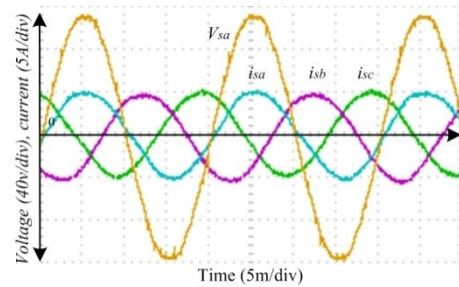


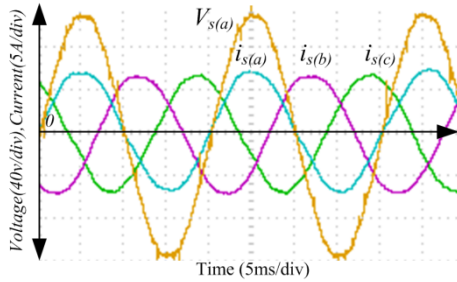
Figure 7.17 Waveforms of the overall performance of the second WECS proposed.



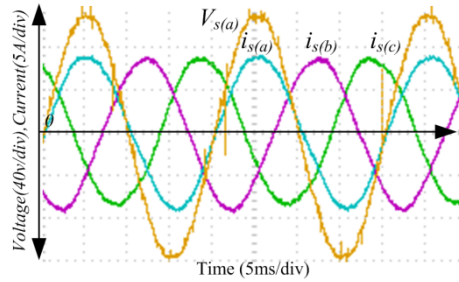
(a) Three phase grid current and phase 'a' voltage, at 6m/s wind speed.



(b) Three phase grid current and phase 'a' voltage, at 8m/s wind speed.

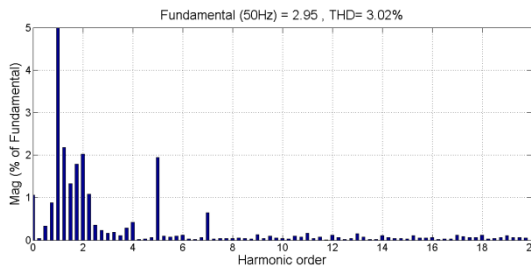


(c) Three phase grid current and phase 'a' voltage, at 9m/s wind speed.

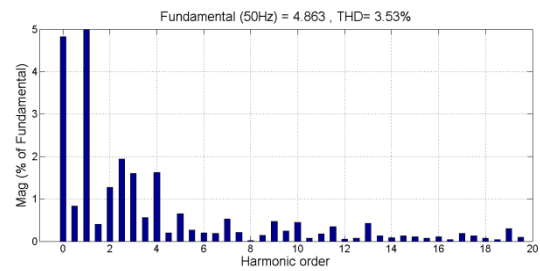


(d) Three phase grid current and phase 'a' voltage, at 10m/s wind speed.

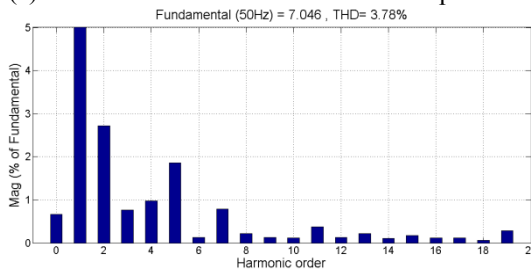
Figure 7.18 output grid current and phase 'a' voltage at different wind speed of the second WECS proposed.



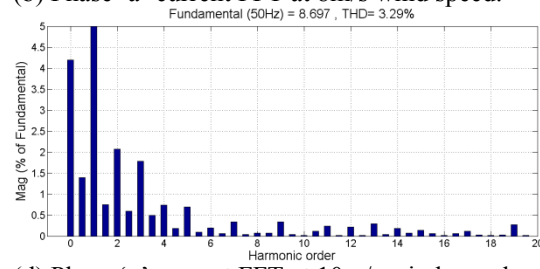
(a) Phase 'a' current FFT at 6m/s wind speed.



(b) Phase 'a' current FFT at 8m/s wind speed.

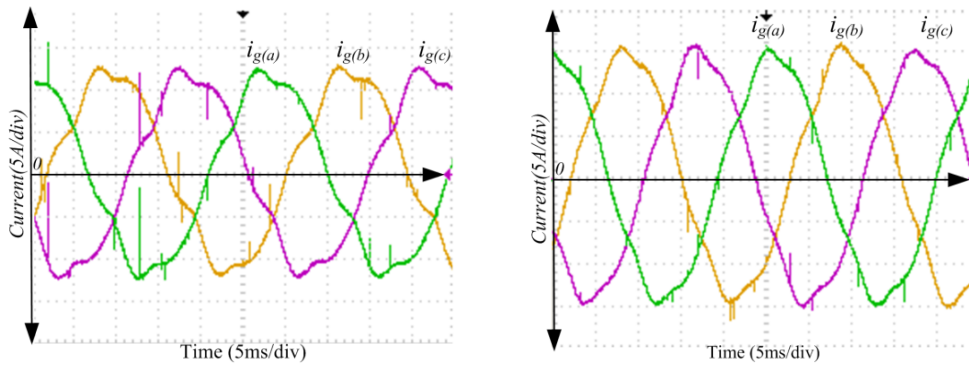


(c) Phase 'a' current FFT at 9m/s wind speed.



(d) Phase 'a' current FFT at 10m/s wind speed.

Figure 7.19 Waveforms shows the grid current fast fourrier transformation (FFT) and total harmonics distortion (THD) at different wind speed.



(a) Generator current at 9m/s wind speed.

(b) Generator current at 10m/s wind speed.

Figure 7.20 the generator current of the second WECS proposed.

7.4. Third WECS proposed (Dual three-phase PMSG and the proposed current source based dual three-phase BTB converter)

The WECS shown in Figure 7.21(a) consists of a wind turbine, a medium-speed drive gear box, a six-phase PMSG, a generator-side C-filter (C_{R1} and C_{R2}), the proposed BTB converter, and a grid-side C-filter (C_{i1} and C_{i2}), connected to the grid through a three-winding phase-shift transformer. As discussed in Chapter five the problem of high voltage stresses are partially solved by using two switching devices S_{r1} and S_{r2} to share the overall voltage stress, as shown in Figure 7.21(b).

The control strategy for the third WECS proposal is similar to that in the second proposed WECS.

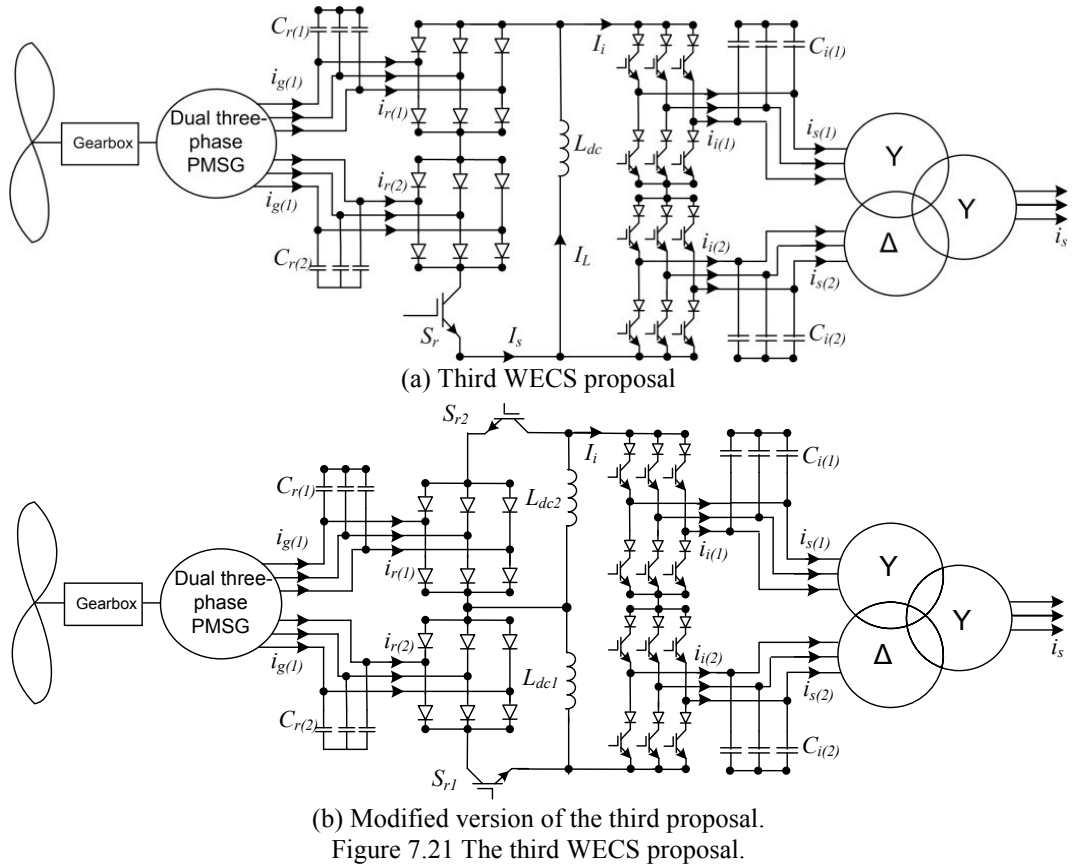
7.4.1 Magneto-motive forces produced by the harmonic currents drawn by the generator side converter

The magneto motive force (MMF) produced by the generator current in the air gap is:

$$MMF = NI \sin(\theta) \quad (7.26)$$

Where N is number of turns, I is stator current, and θ is the mechanical angle.

The analysis of the MMF produced by the generator side converter current harmonics is performed in two steps.



First step: Mathematically analyse the unwanted low frequency harmonics (fifth and seventh) generated by the switching process of switch S_r . Similarly to the three-phase configuration, the per phase-rectifier input current is the same as in Figure 7.11, and the peak of the rectifier input fundamental component I_{rp} is as in equation (7.22)

The carrier frequency harmonic components are obtained by setting $n=0$ in(7.21), yielding

$$I_{r(m0)} = A_{m0} + jB_{m0} = \frac{4\bar{I}_L}{3m\pi} \sin(\delta m\pi) \quad (7.27)$$

From(7.27), $A_{n0} = \frac{4\bar{I}_L}{3m\pi}$ and $B_{m0} = 0$. The peaks of the 1st and 2nd carrier frequency components can be obtained by setting $m=1$ and 2.

The sideband harmonics obtained by computing (7.21) for non-zero m and n are:

$$i_{r(mn)} = A_{mn} + jB_{mn} = \frac{j4\bar{I}_L}{nm\pi^2} \sin(\delta m\pi) \sin(\frac{1}{3}n\pi) e^{j\frac{1}{2}\pi(n+1)} \quad (7.28)$$

From(7.28), $A_{mn=0}$ and $B_{mn} = \frac{j4\bar{I}_L}{3m\pi} \sin(\delta m\pi) \sin\left(\frac{1}{3}n\pi\right) e^{j\frac{1}{2}\pi(n+1)}$ and from the double Fourier series, the rectifier input current i_r expressions are:

$$i_r(t) = \frac{1}{2} A_{00} + \sum_{n=1}^{\infty} (A_{0n} \cos n\omega_0 t + B_{0n} \sin n\omega_0 t) + \sum_{m=1}^{\infty} (A_{m0} \cos m\omega_c t + B_{m0} \sin m\omega_c t) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} (A_{mn} \cos((m\omega_c + n\omega_0)t) + B_{mn} \sin((m\omega_c + n\omega_0)t)) \quad (7.29)$$

$$i_r(t) = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin n\omega_0 t + \frac{4\bar{I}_L}{3\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sin(\delta m\pi) \cos m\omega_c t + \frac{4\bar{I}_L}{\pi^2} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{nm} \sin(\delta m\pi) \sin\left(\frac{1}{3}n\pi\right) e^{j\frac{1}{2}\pi(n+1)} \sin((m\omega_c + n\omega_0)t) \quad (7.30)$$

The first term in equation (7.29) represents the dc-offset where $n=m=0$. The first summation ($\sum_{n=1}^{\infty} \dots$) defines the fundamental low-frequency harmonics which include the low-order undesired harmonics. The second summation ($\sum_{m=1}^{\infty} \dots$) corresponds to the high-frequency carrier-wave harmonics. The third summation ($\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \dots$) refers to the sideband harmonics, which exist as groups around the carrier harmonic frequencies [9].

Equation (7.30) provides a theoretical solution for interpreting the ac harmonic distribution of the generator side converter current, including basebands, carrier frequency, and sidebands harmonics. In addition, (7.30) assists the filter design as it provides information about the location of the dominant low-order and switching frequencies to be eliminated. The fifth and seventh harmonic currents of Stator1 winding are expressed by substituting $n=5$ and 7 respectively in the first term of (7.30), as follows:

$$\left\{ \begin{array}{l} i_{ra(5,1)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{5} \sin 5\omega_0 t \\ i_{rb(5,1)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{5} \sin 5\left(\omega_0 t - \frac{2}{3}\pi\right) \\ i_{rc(5,1)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{5} \sin 5\left(\omega_0 t + \frac{2}{3}\pi\right) \end{array} \right. \quad (7.31)$$

$$\begin{cases} i_{ra(7,1)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{7} \sin 7\omega_0 t \\ i_{rb(7,1)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{7} \sin 7\left(\omega_0 t - \frac{2}{3}\pi\right) \\ i_{rc(7,1)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{7} \sin 7\left(\omega_0 t + \frac{2}{3}\pi\right) \end{cases} \quad (7.32)$$

Since the two sets of three-phase stator PMSG windings are shifted by 30° electrical, the fifth and seventh harmonic currents of the Stator2 winding are:

$$\begin{cases} i_{ra(5,2)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{5} \sin 5\left(\omega_0 t - \frac{1}{6}\pi\right) \\ i_{rb(5,2)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{5} \sin 5\left(\omega_0 t - \frac{2}{3}\pi - \frac{1}{6}\pi\right) \\ i_{rc(5,2)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{5} \sin 5\left(\omega_0 t + \frac{2}{3}\pi - \frac{1}{6}\pi\right) \end{cases} \quad (7.33)$$

$$\begin{cases} i_{ra(7,2)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{7} \sin 7\left(\omega_0 t - \frac{1}{6}\pi\right) \\ i_{rb(7,2)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{7} \sin 7\left(\omega_0 t - \frac{2}{3}\pi - \frac{1}{6}\pi\right) \\ i_{rc(7,2)} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \frac{1}{7} \sin 7\left(\omega_0 t + \frac{2}{3}\pi - \frac{1}{6}\pi\right) \end{cases} \quad (7.34)$$

Second step: Calculate the resultant *MMF* of the fifth and seventh harmonics in the air-gap.

The *MMF* produced by fifth harmonic current of the Stator1 winding is calculated by substituting equation (7.31) into (7.26) giving:

$$MMF_{(5,1)} = \frac{2\sqrt{3}\delta\bar{I}_L N}{\pi} \frac{1}{5} \left(\begin{aligned} &\sin 5\omega_0 t \sin \theta + \sin 5\left(\omega_0 t - \frac{2}{3}\pi\right) \sin\left(\theta - \frac{2}{3}\pi\right) \\ &+ \sin 5\left(\omega_0 t + \frac{2}{3}\pi\right) \sin\left(\theta + \frac{2}{3}\pi\right) \end{aligned} \right) \quad (7.35)$$

$$MMF_{(5,1)} = -\frac{2\sqrt{3}\delta\bar{I}_L N}{5\pi} \frac{3}{2} \cos(\theta + 5\omega_0 t) \quad (7.36)$$

Similarly $MMF_{(7,1)}$, $MMF_{(5,2)}$ and $MMF_{(7,2)}$:

$$MMF_{(7,1)} = \frac{2\sqrt{3}\delta \bar{I}_L N}{7\pi} \frac{3}{2} \cos(\theta - 7\omega_0 t) \quad (7.37)$$

$$MMF_{(5,2)} = \frac{2\sqrt{3}\delta \bar{I}_L N}{5\pi} \frac{3}{2} \cos(\theta + 5\omega_0 t) \quad (7.38)$$

$$MMF_{(7,2)} = -\frac{2\sqrt{3}\delta \bar{I}_L N}{7\pi} \frac{3}{2} \cos(\theta - 7\omega_0 t) \quad (7.39)$$

Equations (7.40) and (7.41) show the resultant MMF_5 and MMF_7 respectively, proving MMF cancellation, showing the desirable feature of using a multi-phase machine.

$$MMF_5 = MMF_{(5,1)} + MMF_{(5,2)} = 0 \quad (7.40)$$

$$MMF_7 = MMF_{(7,1)} + MMF_{(7,2)} = 0 \quad (7.41)$$

The first pulsating torque is from the eleventh harmonics current, which can be removed by the generator side C-filter.

7.4.2 Simulation results

i. Normal operating condition

The WECS in Figure 7.21 is simulated using PSCAD/EMTDC. The system parameters used in the simulation study are given in Table 7.3. To assess the steady state and dynamic performance of the proposed WECS, the system is simulated at several wind speeds conditions from 6.5m/s to rated wind speed, 12.5m/s. Figure 7.22 shows waveforms that summarize the overall performance of the proposed WECS. In Figure 7.22(a), the proposed WECS operates under optimal conditions, with minimum transients at the different wind speed steps and is able to track maximum power from the wind turbine. Figure 7.22(b) shows the changes in the active power delivered into the grid by the dual CSI, at different wind speeds. Figure 7.22(c) gives a detailed view of the active power delivered into grid as the wind speed changes from 10m/s to 12.5m/s. The proposed WECS decreases the power delivered to the grid; to decrease the electrometrical torque produce by the generator, to decrease the time needed to build up the turbine speed and reduce the transient time. Figure 7.22(c) shows that the average dc-link inductor current increases to compensate the increase the power delivered to the grid.

Figure 7.23(a) and (b) show the simulated grid currents and phase ‘a’ voltage at 12.5m/s and 10m/s wind speed, where the proposal BTB converter delivers to the grid, sinusoidal current with nearly unity power factor. Figure 7.23(c) and (d) shows the generator current of phases ‘a1’ and ‘a2’ at 12.5m/s and 10m/s wind speeds.

Table 7.3 The third WECS PSCAD/EMTDC setup parameters

Dual three-phase PMSG Parameters	
Rated power	5.2 MVA
Rated speed	180 rpm
Rated voltage	3.3 kV
Direct-axis inductance	0.0055 H
Quadrature-axis inductance	0.0055 H
Mutual inductance coefficient	0.001 H
Number of poles	34
Permanent magnetic flux	14 Wb
Wind Turbine Parameters	
Rated power	5.2 MW
Cut-in wind speed	4 m/s
Rated wind speed	12.5 m/s
Cut-out wind speed	25 m/s
Rotor diameter	108 m
Rotor area	9160 m ²
Gearbox ratio	1:10
Converter Parameters	
Generator side C-filter	280 μ F (Y connection)
DC side inductance	10 mH
Grid side C-filter	55 μ F (Δ connection)
Phase-shifted transformer rated power	5.2 MVA
Phase-shifted transformer rated voltage	3.3 kV
Switch Sr frequency	1.2kHz
Converter rated active power	5.5MW
Converter rated reactive power	3MVAr

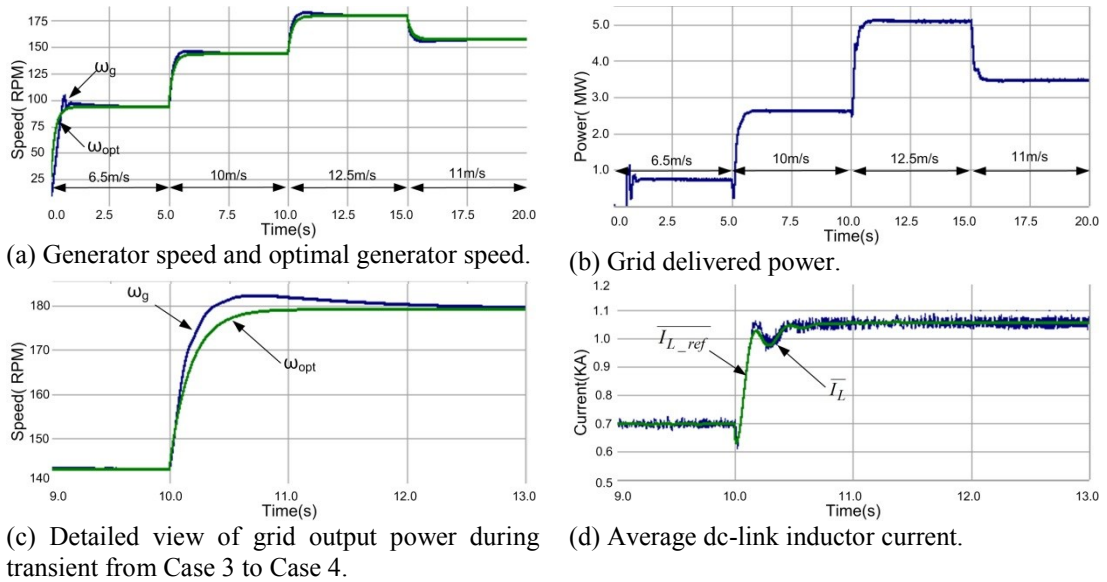


Figure 7.22 PSCAD/EMTD simulation waveforms of the third WECS proposed.

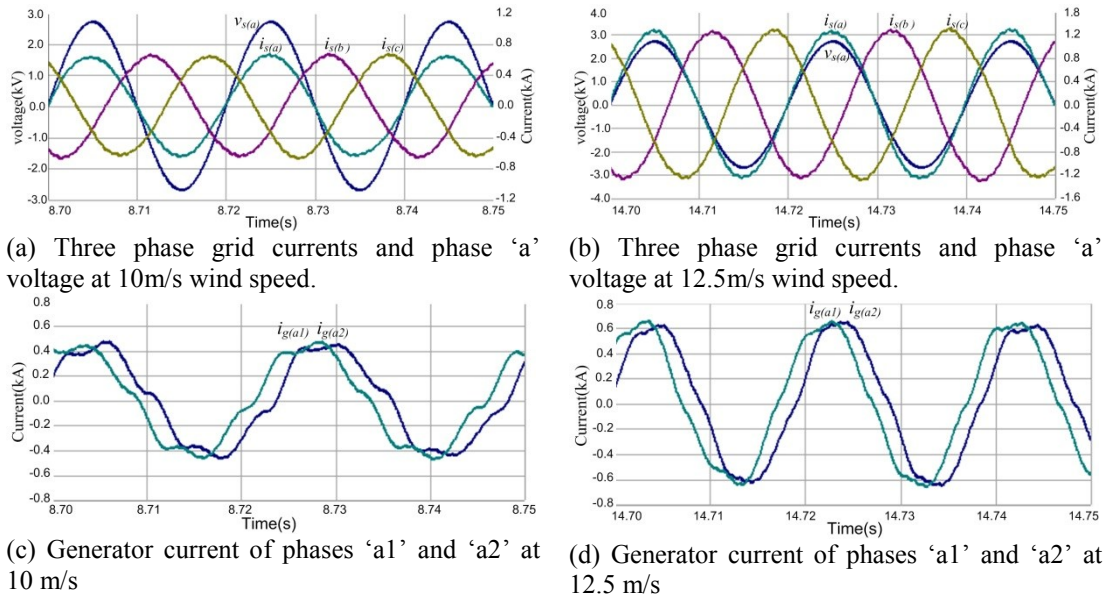


Figure 7.23 Simulation waveforms of the grid and generator currents at different wind speeds, of the third WECS proposed.

ii. LVRT

This section shows the performance of the third WECS under LVRT, using the LVRT technique previously discussed. In this simulation the grid voltage drops to 10% of its rated value for 140ms. Figure 7.28 shows waveforms that summarize the WECS overall performance. From Figure 7.28(a) the generator speed increases (9%) during the grid fault, due to the imbalance between the generated power and the grid delivered power, and when the grid recovers, the controller tracks the optimal speed again. Figure 7.28(b) shows the reactive current during LVRT. Figure 7.28(c) shows

that the grid delivered power reduces to zero during the LVRT and smoothly recovers when the fault clears. Figure 7.28(d) show the q-component of the grid delivered current that increases to the rated value during LVRT, and decreases to zero after the grid fault.

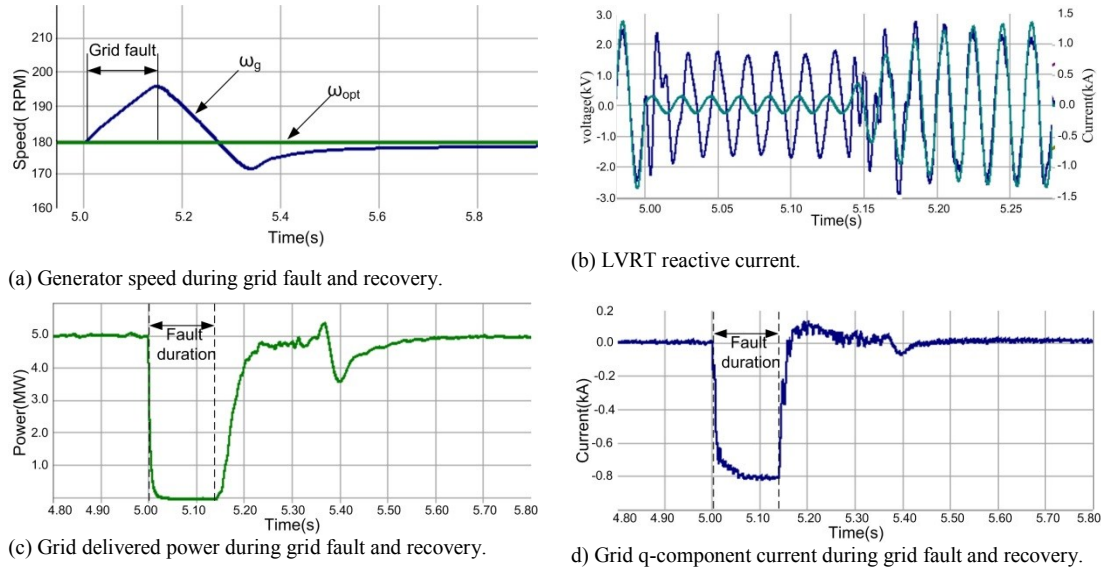


Figure 7.24 Waveforms of the third proposed WECS during a LVRT condition.

7.4.3 Experimental results

In this section, the performance of the proposed WECS shown in Figure 7.21 is experimentally evaluated, with different cases used to evaluate the dynamic performance of the proposed control schemes. Figure 7.25(a) shows the dual three-phase PMSG emulator, which consists of a three-phase synchronous generator connected to a phase-shift transformer. Figure 7.25(b) shows the experimental test rig rated at 2kVA. The experimental parameters are given in Table 7.4.

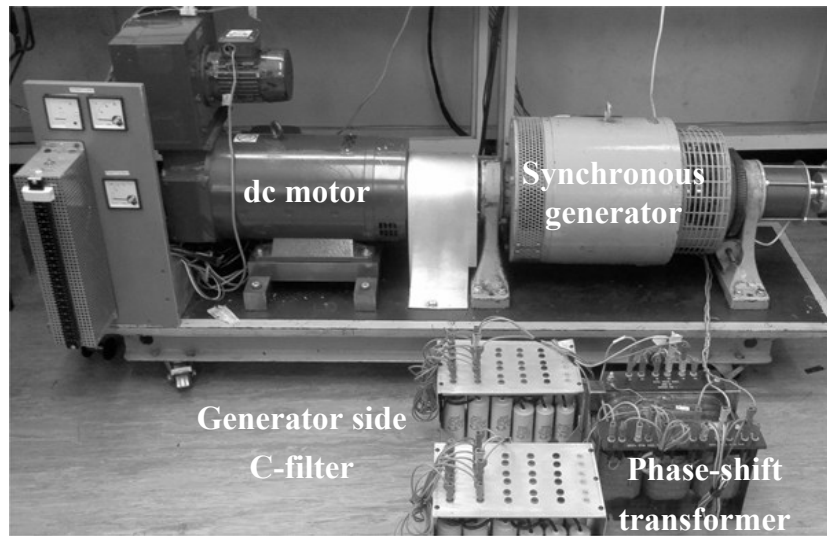
The WECS is tested at three different wind speeds each lasting 40 seconds: at initial wind speeds of 6m/s, which undergoes a step increase to 8m/s and then a step decrease to 7m/s. The sequence is repeated, thus enabling examination of the dynamic performance and stability of the proposed system. According to (7.1) and by multiplying by the gear box ratio, the optimal generator speeds at each wind speed are 600rpm, 800rpm and 700rpm respectively. Figure 7.26 and Figure 7.28 shows experimental results from the WECS converter in Figure 7.25. Figure 7.26(a) shows the generator tracks the optimal speed and produces the corresponding active power

is delivered to grid, at the different wind speeds. The proposal speed controller forces the generator to run at the optimal speed with minimum transient and oscillation at different wind speed condition. Also Figure 7.26(a) shows the change in the active power delivered to the grid changes smoothly with minimum oscillation. Figure 7.26(b) shows that the proposed speed controlled loop ensures soft started up. Figure 7.27(a) and (b) shows a snapshot of the output current injected into grid and phase 'a' voltage at 8m/s wind speed. The proposed WECS supplies the grid with high quality sinusoidal current, and the proposed reactive power controller adjusts the reactive power to zero, giving near unity power factor. Figure 7.28(a) shows in detail the dc-link inductor current I_L , dual CSI input current I_i and switch current I_s . From Figure 7.28(a) when the switch is on, the dc-link current rises the switch current I_s and the dual CSI input current I_i equals zero, while when the switch is off the dc-link inductor current I_L falls to the dual CSI input current I_i , and the switch current I_s is zero. Figure 7.28(b) show the dual CSI output currents ' i_{a1} ' and ' i_{a2} ', where the dual CSI converts the input current I_i to ac current. Figure 7.28(c) shows the generator side phase-shift transformer secondary currents and primary current at 8m/s.

Table 7.4 The third WECS experimental parameters

Wind Turbine Parameters	
Power at rated wind speed	4.6kW
Cut-in wind speed	4m/s
Rated wind speed	12.5m/s
Rotor diameter	3.2m
Rotor area	8.04m ²
Gearbox ratio	1:2.07
Dc motor Parameters	
Rated armature voltage	460 V
Rated speed	1500 rpm
Rated current	16A
Field current	1.2A
Armature resistance	2.5Ω
Torque constant K_m	2.47
Synchronous machine parameters	
Rated speed	1500rpm
Rated voltage	400V
Rated current	10A
Rated frequency	50Hz
Number of poles	4
Field current	0.5A
Generator voltage constant K_G	2.5
Armature resistance	1.2Ω
Armature inductance	36 mH

Generator side phase shift transformer parameters	
Rated power	2kVA
Primary rated voltage	415V (Δ connection)
Two secondary winding rated voltage	415V (Δ connection) 400V (Y connection)
Converter parameters	
Genrator side Cfilter	150 μ F(Y connection)
dc-link inductance	12.5mH
Grid side C-filter	55 μ F (Δ connection)
grid side phase shift transformer parameters	
Rated power	2kVA
Primary winding rated voltage	415V(Y connection)
Two secondary winding rated voltage	208V(Y connection) 208V(Δ connection)

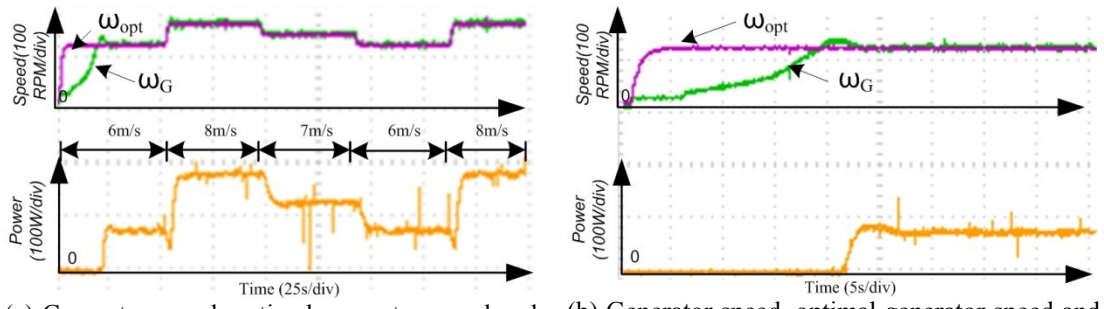


(a) Dual three-phase PMSG emulator.

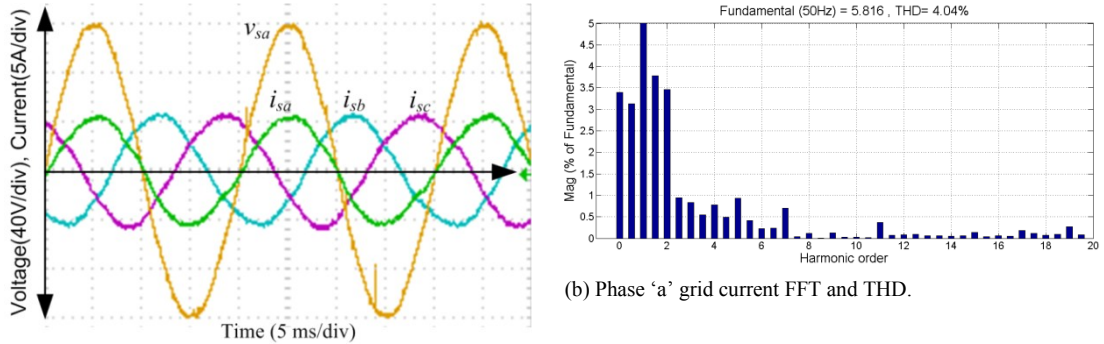


(b) Experimental test rig

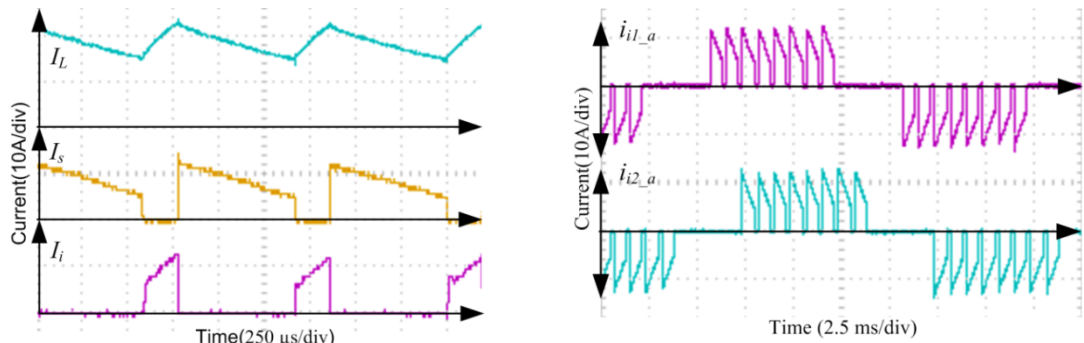
Figure 7.25 Third WECS experimental setup.



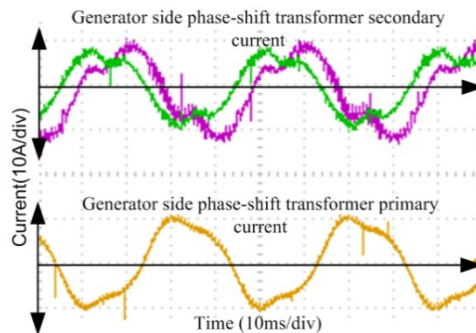
(a) Generator speed, optimal generator speed and grid output power during the proposed scenario. (b) Generator speed, optimal generator speed and grid output power during start-up.
 Figure 7.26 Waveforms showing the overall performance of the third proposed WECS.



(a) Three phase grid currents and phase 'a' voltage, at 8m/s. (b) Phase 'a' grid current FFT and THD.
 Figure 7.27 Waveforms show the grid current.



(a) dc-link inductor current I_L , switch current I_s and CSI input current I_i at 8m/s wind speed. (b) Dual CSI phase output current ' i_{i1_a} ' and ' i_{i2_a} ' at 8m/s.



(c) Generator side phase-shift transformer secondary current and primary current, at 8m/s wind speed
 Figure 7.28 Performance waveforms of the third proposed WECS, at 8m/s wind speed.

7.5. Summary

Three different WECS configurations are discussed in this chapter, based on the power electronics converters proposed in this thesis. The first WECS utilized a dual three-phase CSR and CSI to operate at low switching frequency. The configuration allows placing of the heavy equipment (grid-side transformer, CSI, and dc-link inductance) at the bottom of the wind turbine tower, for ease of installation and access. The second WECS utilized the three-phase BTB CSC proposed in Chapter five: this configuration is simple and easy to control with a low implementation cost. But the use of an uncontrolled diode rectifier limits the WECS rated power. The third WECS is suitable for multi-megawatt application due to using the dual three-phase BTB CSC proposed in Chapter five and MMF cancellation features which are inherent in a multi-phase machine.

The simulation and experimental results of the three proposed WECS, show tracking of wind turbine optimal speed with good dynamic performance, and stable ac grid output voltage and current waveforms over a wide wind speed range.

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Chapter 8. General chapters summaries and future research

8.1. General chapters summaries

This thesis presents new breeds of back-to-back (BTB) current source converters (CSCs) that may be applicable to variable-speed wind energy conversion system (WECS). These BTB converters employ current source inverters (CSI), current source rectifiers (CSR) and ac-dc buck-boost converters as interfacing converters. Chapter two of this thesis reviewed the modulation strategies for the voltage and current source converters, with illustrative simulations establishing the attributes and limitations of both converter types. The major findings of this chapter are presented as a comparison between the VSC and the CSC. The comparison showed that the CSC is suited for high-power medium-voltage WECS due to its low switching frequency per device, low dv/dt , and resilience to ac and dc short circuits. However, the voltage source converter (VSC) has faster dynamic response and higher efficiency. From wind energy prospective, fast dynamic response is irrelevant due to the large mechanical time constant of the wind turbine-generator system.

Chapter three presented modelling analysis for the CSC in island and grid modes (CSI and CSR), including a dual current source rectifier and inverter. All CSI and CSR models were developed in the $d-q$ synchronous reference frame to allow the use of conventional proportional-integral controllers, thereby ensuring zero steady-state error. The basic control objectives in this chapter are to allow the proposed CSC to meet grid code requirements and to be competitive to VSCs by offering features such as independent control of active and reactive powers; ac fault ride-through capability, and a low total harmonic distortion (THD) at reduced switching frequency per device.

Chapter four presented new single-stage, single-phase, three-phase and multi-phase ac-dc buck-boost converters, and discussed the operating principles and mathematical relationships governing each. The results shown that these converters have sinusoidal input current at nearly unity input power factor, and offer stable and adjustable output dc voltage (in buck and boost modes). The practicality of the

proposed ac-dc buck-boost converters is confirmed using simulations and experimentation.

Chapter five presented modified three-phase and dual three-phase back-to-back CSCs that offer several attractive features, such as soft start-up and shut-down capability; sinusoidal input and output currents; high input power factor; and controllable output reactive power; with zero switching losses at the inverter side. Simulation and experimental results showed that the proposed BTB converters are suitable for WECSs.

Chapter six reviewed and presented the mathematical model of a three-phase synchronous generator and dual three-phase permanent magnet synchronous generator model, in $dq0$ frame, where the phases of the two stator windings are shifted by 30° . This chapter also reviewed the wind turbine model, and outlined the wind turbine emulator that uses a PSoC microcontroller, programmable dc supply and a separately-excited dc motor, to mimic the operation of a variable speed wind turbine generator mechanical system.

Benefiting from the discussion in chapters three, four, five, and six, Chapter seven presented three different WECS configurations. The first WECS utilized the BTB dual current source converter arrangement presented in chapter, exploiting its low switching frequency. The second and third WECSs are based on the modified three-phase and dual three-phase BTB CSC proposed in chapter five. The second configuration that uses an uncontrolled diode rectifier with a single controllable switch, limits the rated power of the WECS to less than 1MW. While the third WECS configuration is suitable for multi-MW application; due to the magneto motive force cancellation feature of the multi-phase machine.

Based on the above discussion it can be concluded that the research objectives given in chapter one have been achieved. The simulation and experimental results shows that the proposed WECSs' satisfy most of the research motivation given in Chapter one; such as:

- Operating at variable speed with maximum power tracking.

- Transfer the power extracted from the wind turbine to the grid at fixed voltage and frequency, with high quality sinusoidal grid current.
- Supply reactive power to the grid during low voltage ride through.

The simulation and experimental work did not cover the entire grid code requirement like the frequency regulation support, and voltage regulation capability at the point of common coupling. Also the proposed WECSs are tested at rated wind speed no blade pitch angle ($\beta=0$) control considered. This important topic needs to be covered in future work; as will be shown in recommendation for future research section.

8.2. Author's contribution

The main contribution in this thesis is the three new current source based variable-speed WECSs. They offer the inherent features of existing systems based on VSCs such as: maximum power tracking; fault ride-through capability; provision of voltage and frequency support to ac grid; and inject a sinusoidal current is into grid with low harmonic content, but with increased reliability and improved ac side waveform quality; and independent control of active and reactive power. Most of these attributes have been validated using PSCAD/EMTDC simulations and substantiated on scaled down experimental prototypes. This thesis presented a comprehensive assessment of the steady-state and dynamic behaviour of the proposed WECSs, considering different operating conditions.

The main contributions of this thesis are:

- 1) Chapter two presented:
 - Online mapping technique that converts the gating signals of the VSC to those suitable for a CSC, without the need for the hardware based logic circuit mapping technique proposed by Espinoza.
 - Offline SHE modulation that can eliminate the 11th and 13th harmonics using one pattern with continuous pulse angle changes and with a fixed switching frequency. The proposed pattern addresses the drawback of the conventional SHE implementation that uses two patterns with two different switching frequencies.

2) Chapter four presented:

- New single-stage, ac-dc buck-boost converter and its control strategy. Its practicality is confirmed using simulations and experimentation. The proposed converter injects high-quality sinusoidal supply current, with near unity power factor over a wide operating range.
- Three-phase, single-switch ac-dc buck-boost converter, where the input capacitor operates under a continuous current mode with reduced switching frequency, in order of 1.2 kHz, to suit medium-voltage applications. Unlike the conventional CSC, the input capacitor has continuous current (thus, decreased voltage stress per device). Also the proposed ac side filter design ensures a high power factor at rated power, and low input current THD.
- Dual three-phase ac-dc buck-boost converter, with a three-winding phase-shifted transformer to achieve sinusoidal input currents, with relatively small ac filters. The proposed dual buck-boost converter has a better power factor profile, but its main drawback is that the switching devices are exposed to high-voltage stresses. A modified dual three-phase buck-boost configuration is proposed to partially solve this problem.
- Three-phase cascaded buck-boost converters that employ three single-phase converters, with their dc output terminals connected in series to generate high voltage. By using this approach, voltage stresses on the switching devices are reduced, and sinusoidal input currents with nearly unity power factor is achieved over the entire operating range, with small ac filters. The simulation and experimentation show that discontinuous conduction operation results in the lowest voltage stress per device, at the expense of increased discontinuous current peaks.

3) Chapter five presented new (three-phase and dual three-phase) current source based back-to-back converters, which have reduced circuit

complexity and simplified control, including a dedicated high frequency synchronization method that ensures zero CSI switching losses.

- 4) Chapter seven presented three new current source converter based variable-speed WECSs, including a method for low-voltage ride-through that uses a power dissipation mechanism that consists of a switched bleeding resistor in the dc input of the grid connected CSI. During normal operation, switch bypasses the bleeding resistor. During a grid fault, the proposal WECS dissipates some of the energy in the bleeding resistor and temporarily stores the rest in the turbine-generator mechanical inertia.

8.3. Recommendation for future research

- Design new ac-dc buck-boost converter configurations that have the advantage of both continuous conduction (low current stress on the switches) and the discontinuous conducting mode (lower voltage stress on the switches).
- Apply the proposed buck-boost converter and the modified current source back-to-back converter to different power electronics applications, such as uninterruptible power supplies.
- Investigate the viability of the WECSs under different grid conditions such as unbalanced grid operation.
- Study the performance of the WECS under high wind speed with blade pitch angle ($\beta \neq 0$) control consideration.

Appendix A Phase Lock Loop (PLL)

The phase angle and frequency information are used to transform the three-phase voltage and current from the abc frame to the dq frame, to detect the flow of active/reactive power. The zero crossing point of the grid voltages is the easiest way to obtain the phase information, but this method has slow dynamic performance since zero crossings occur once at every half cycle. Other techniques are based on low-pass filters (LPFs)[2-4], but using a LPF typically generates phase delay specially in the case of a step change in the phase angle or in the frequency or in both. This delay results in a sluggish response and causes any time-critical machine to malfunction. The weighted least-squares estimation (WLSE) can provide phase angle and frequency within a few sampling periods even when both the phase angle and amplitude begin to change in step manner[5].

A.1 Phase angle estimator

The single-phase grid voltage $v_s(t)$ is given by:

$$v_s = V_m \cos(\omega t + \theta) \quad (\text{A.1})$$

$$v_s = v_{sd} \cos \omega t - v_{sq} \sin \omega t \quad (\text{A.2})$$

where V_m : is the peak supply voltage, θ : is the phase angle, $v_{sd} = V_m \cos \theta$ and $v_{sq} = V_m \sin \theta$, at steady state θ , v_{sd} and v_{sq} are constant.

Using weighted least square (WLS) method, the cost function is chosen such that [6]:

$$J[x(t_i)] = \sum_{j=0}^i \lambda^{i-j} (y(t_j) - H(t_j)x(t_j))^2 \quad (\text{A.3})$$

where: $y(t_i) = v_s(t)$, $H(t_i) = [\cos \omega t_i \quad -\sin \omega t_i]$, $x(t_i) = [V_d(t_i) \quad V_q(t_i)]^T$, λ is the forgotten factor ($0 < \lambda < 1$).

The least-squares method is used to get $\hat{x}(t_i)$, to minimize the cost function is [5-8]:

$$\hat{x}(t_i) = \hat{x}(t_{i-1}) + k(t_i)(y(t_i) - H(t_i)\hat{x}(t_{i-1})) \quad (\text{A.4})$$

$$k(t_i) = P(t_{i-1})H(t_i)^T (1 + H(t_i)P(t_{i-1})H(t_i)^T)^{-1} \quad (\text{A.5})$$

$$P(t_i) = \lambda^{-1}P(t_{i-1}) - \lambda^{-1}K(t_i)H(t_i)P(t_{i-1}) \quad (\text{A.6})$$

The initial conditions can be set as: $\hat{x}(0) = 0$, $P(0) = \pi_0 I^{2 \times 2}$ and $\pi_0 > 0$ is the initial covariance constant.

From equation (A.4) the phase angle off-set θ and the line voltage angle $\hat{\theta}(t)$ can be calculated as follows:

$$\theta = \tan^{-1} \left(\frac{v_{sq}}{v_{sd}} \right) \quad (\text{A.7})$$

$$\hat{\theta}(t) = \omega t + \theta \quad (\text{A.8})$$

The step change in the phase angle θ or in the voltage amplitude, is recognized if the error magnitude $|y(t_i) - H(t_i)\hat{x}(t_{i-1})| > \varepsilon$ (ε is the heuristic guide line (20 ~ 40% of V_m)). Once recognized, the covariance P is reset to its initial value, this tends to increase the gain k, which increases the tracking speed in the case of phase angle jump.

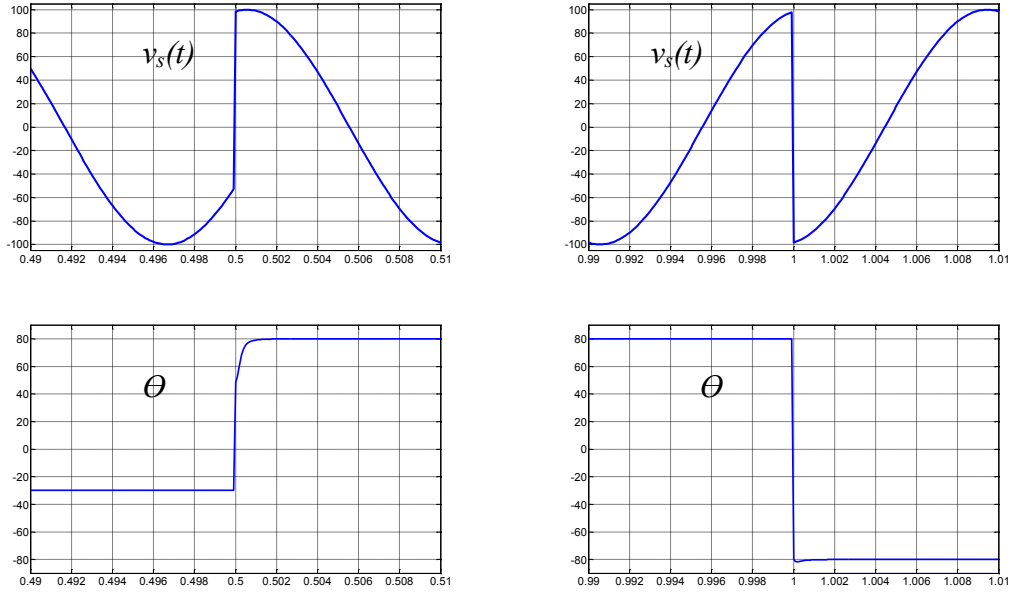
The WLSE for phase angle estimator is tested according to the following sequence. First the supply voltage waveform is shifted by -30° and then a step change of 80° is applied to phase angle, and after half a second it is changed to -80° .

Figure A. 1 Simulation result of the proposed estimation scheme with $\lambda = 0.98$.

(a) and (b) shows the simulation results of the WLSE phase angle estimator, where the sampling frequency is 10kHz, $\pi_0 = 300$ and $\lambda = 0.98$. The WLSE has succeeded in quickly tracking the phase angle change.

Figure A. 2 Experimental results of WLSE for phase angle estimator.

show experimental results of the grid phase 'a' and the line voltage angle $\hat{\theta}(t)$, where the presented WLSE tracks the grid voltage.



(a) Phase angle changed from -30 to 80.

(b) Phase angle changed from 80 to -80.

Figure A. 1 Simulation result of the proposed estimation scheme with $\lambda = 0.98$.

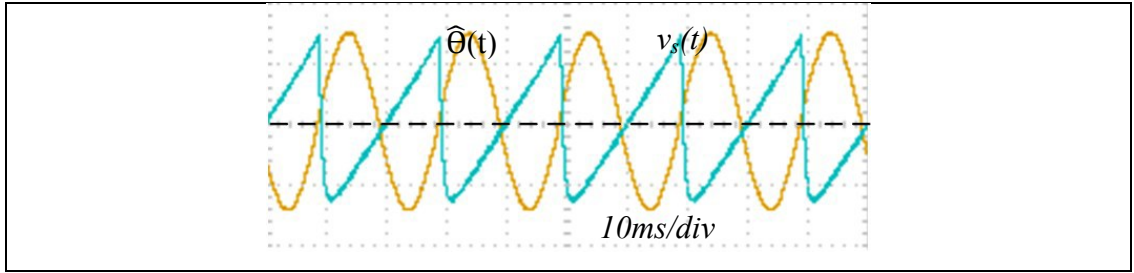


Figure A. 2 Experimental results of WLSE for phase angle estimator.

A.2 Frequency estimator

WLSE for frequency estimator is simple, and with low requires resources for implementation, because the estimated frequency is computed using the information provided from the supply[9].The voltage signal is digitized at the measurement location with a uniformly sampled at frequency $\omega = 2\pi/\Delta t$. Three consecutive samples of the signal ($v_s(i), v_s(i-1)$ and $v_s(i-2)$) are connected with the following equation[9, 10]:

$$\frac{v_s(i) - v_s(i-2)}{2} = v_s(i-1) \cos \omega \Delta t \quad (\text{A.9})$$

$$y(i) = z(i)x(i) \quad (\text{A.10})$$

here $y_{(i)} = \frac{v_{s(i)} - v_{s(i-2)}}{2}$, $z_{(i)} = v_{s(i-1)}$ and $x_{(i)} = \cos\omega\Delta t$

Equation (A.10) is over determined, since the number of equations is much larger than the number of variables, $x_{(i)}$ can be calculated using following formula [9, 10]:

$$x_{(i)} = \frac{\sum_{i=0}^k \lambda^{2(i-k)} z_i y_i}{\sum_{i=0}^k \lambda^{2(i-k)} z_{(i)}^2} = \frac{SumZY_{(i)}}{SumZZ_{(i)}} \quad (A.11)$$

$$SumZY_{(i)} = \lambda^2 SumZY_{(i-1)} + z_{(i)} y_{(i)} \quad (A.12)$$

$$SumZZ_{(i)} = \lambda^2 SumZZ_{(i-1)} + z_{(i)}^2 \quad (A.13)$$

$0 < \lambda < 1$ is the forgetting factor, which is introduced to give more impact to newer samples and weaken the impact of older data. Selecting the value of λ depends on the required estimator speed and the sensitivity to random noise, for λ near to one the accuracy is high but the frequency estimation speed is low vice versa [11]. it assumed that λ is constant value, The estimated frequency f_{est} can calculated as following:

$$f_{est} = \frac{\cos^{-1}(x_{(i)})}{2\pi\Delta t} \quad (A.14)$$

It can be noted that proposed WLSE for frequency estimation algorithm is very simple and easy to emblems. The forgetting factor can adapted according to the change in the signal frequency, to compromise between speed and accuracy. The residual error can be calculated as

$$e = y_{(i)} - z_{(i)} x_{(i)} \quad (A.15)$$

The covariance error as follows [9, 10]:

$$R_{(i)} = \lambda_{(i-1)}^2 R_{(i-1)} + [y_{(i)} - z_{(i)} x_{(i)}]^2 \quad (A.16)$$

Forgetting factor can be calculated as follow:

$$\lambda = \left(\frac{1}{1 + \left| \frac{R_{(i)}}{R_0} \right|} \right)^{\frac{1}{2}} \quad (\text{A.17})$$

where R_0 is chosen value.

Figure A. 3 show the simulation results of the frequency estimator, where the supply frequency step changed from 50Hz to 55Hz and $R_0=0.001$.

Figure A. 3 (a) show the simulation of the proposed WLSE for frequency estimation with constant forgetting factor, it can be observed the proposed frequency estimator succeed to accurately track the step change in the frequency in 0.025s, while

Figure A. 3 (b) show that using that the proposed adapted forgetting factor will increase the frequency estimation speed (0.002s) without effecting the accuracy.

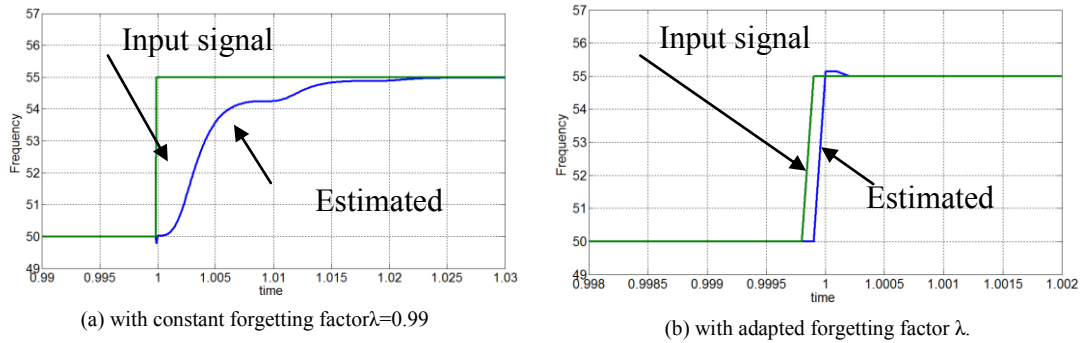


Figure A. 3 Simulation result of the WLSE for frequency estimator.

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Appendix B

Test Rigs Basic Components

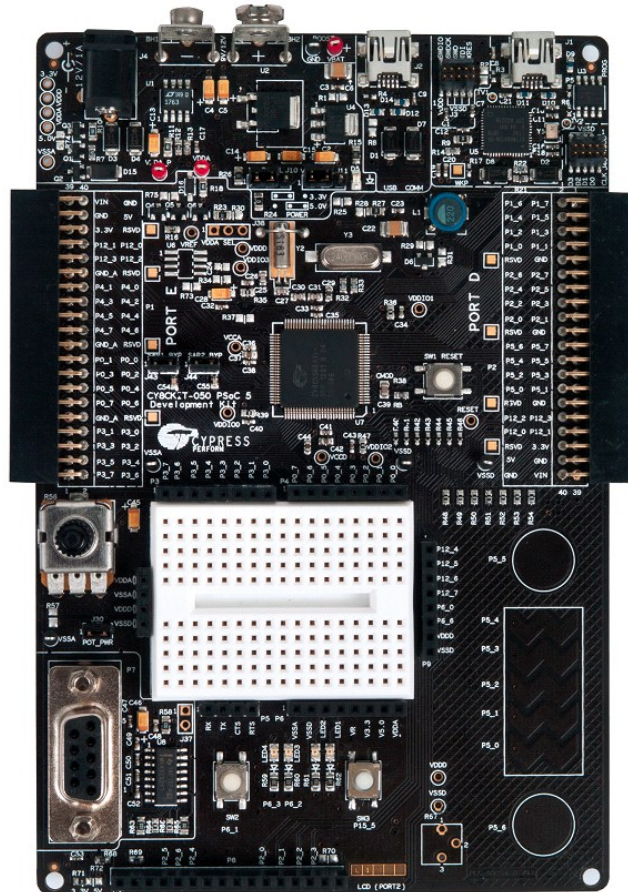
B.1 Controller

The purpose of the controller is to perform the control algorithm based on the feedback signals (voltage, current and speed) and take action by turning on/off the insulated gate bipolar transistors (IGBTs) in the proposed power electronics converters.

In this work two types of controller were used:

1. The Infineon 32-bit TriCore 1796B DSP is shown in Figure B. 1 .

Programmable system on chip (PSOC-5LP) is shown in



2. Figure B. 2

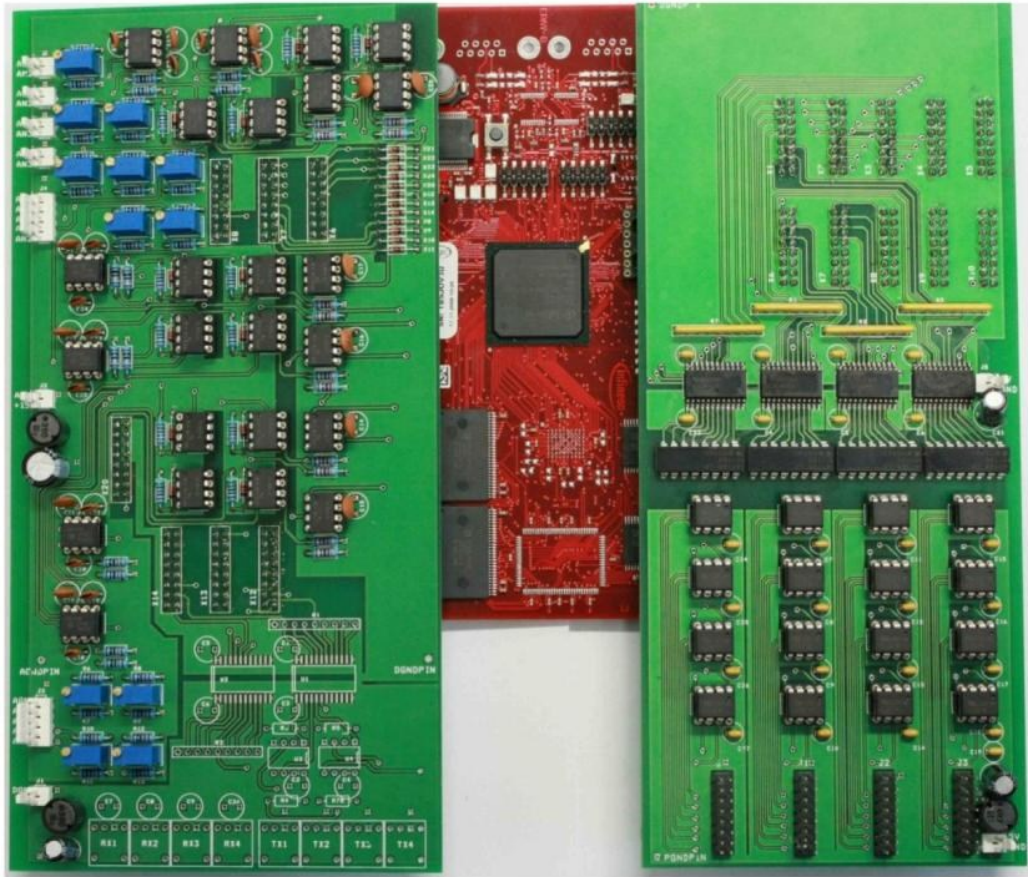


Figure B. 1 Infineon 32-bit TriCore 1796B DSP

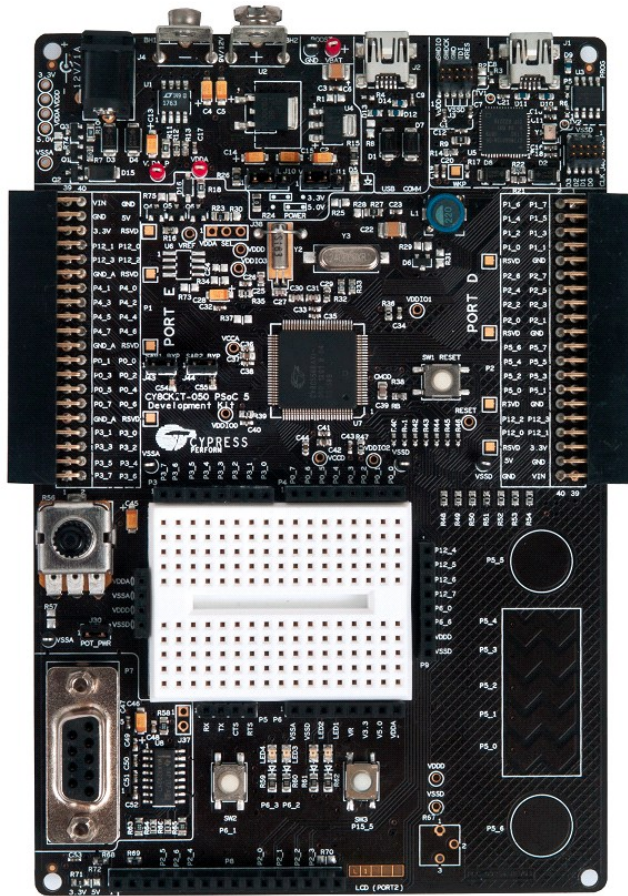


Figure B. 2 PSoC 5LP

B.2 IGBT gate drive

Figure B. 3 shows the used gate drive during this theses, the gate drive was used to insulate and amplifies the controller signal and make it suitable for the IGBTs.



Figure B. 3 Gate drive

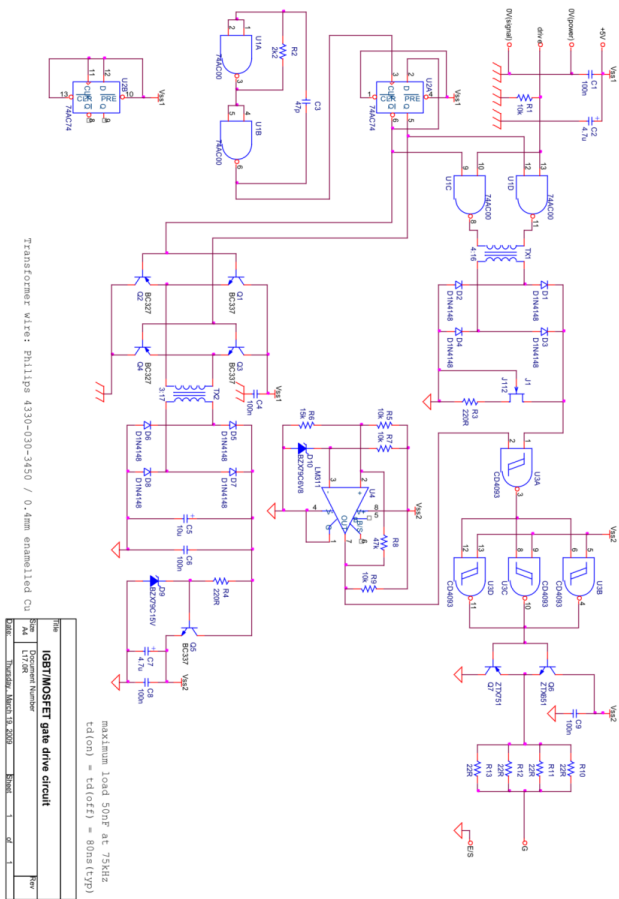
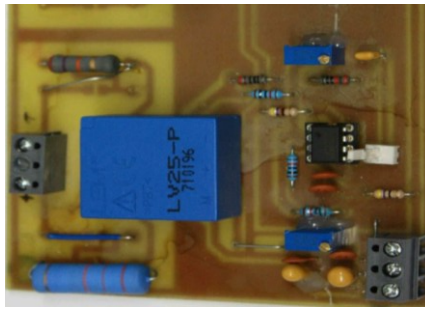


Figure B. 4 Gate drive schematic

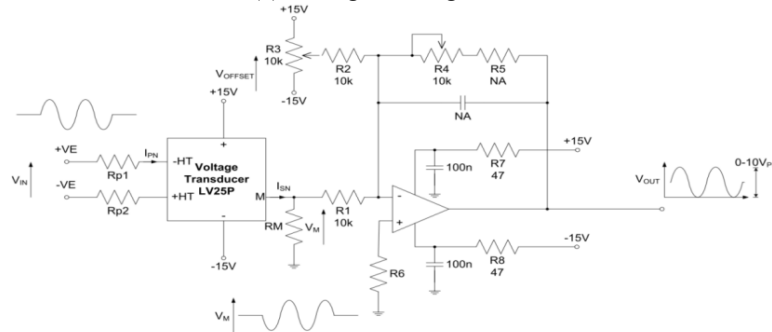
B.3 Voltage and current sensing circuit

Voltage and current measurements are required as feedback signals for the controller. The voltage transducer used LEM-LV25-P was used in the voltage sensing circuit which shown in Figure B.5(a). The voltage sensing schematic is given in Figure B.5(b).The LEM LA 55-P current transducer was used to electronically measure the ac and dc currents. The current sensing circuit and schematics are given in

Figure B. 6.

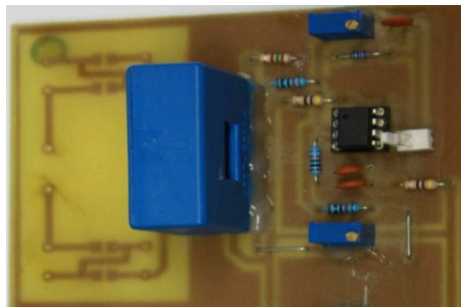


(a) Voltage sensing circuit

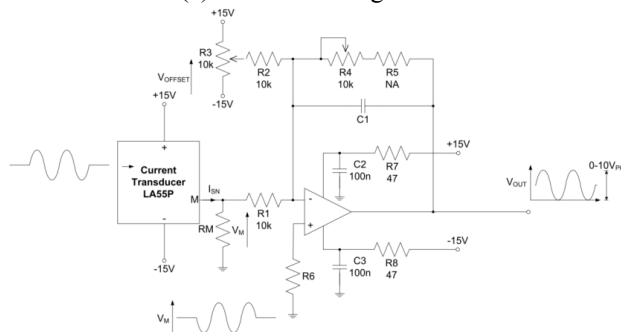


(b) Voltage sensing schematic

Figure B.5 Voltage sensing circuit and schematic



(a) Current sensing circuit



(b) Current sensing schematic

Figure B. 6 Current sensing circuit and schematic

B.4 Motor generator set

A separately excited dc motor was used as primary mover for the open winding three-phase synchronous generator, this motor generator set was used with the help of the micro-controller and the programmable dc power supply to build the wind turbine emulator. The motor generator set photo is given in Figure B. 7, and parameters are given in Table B.1.

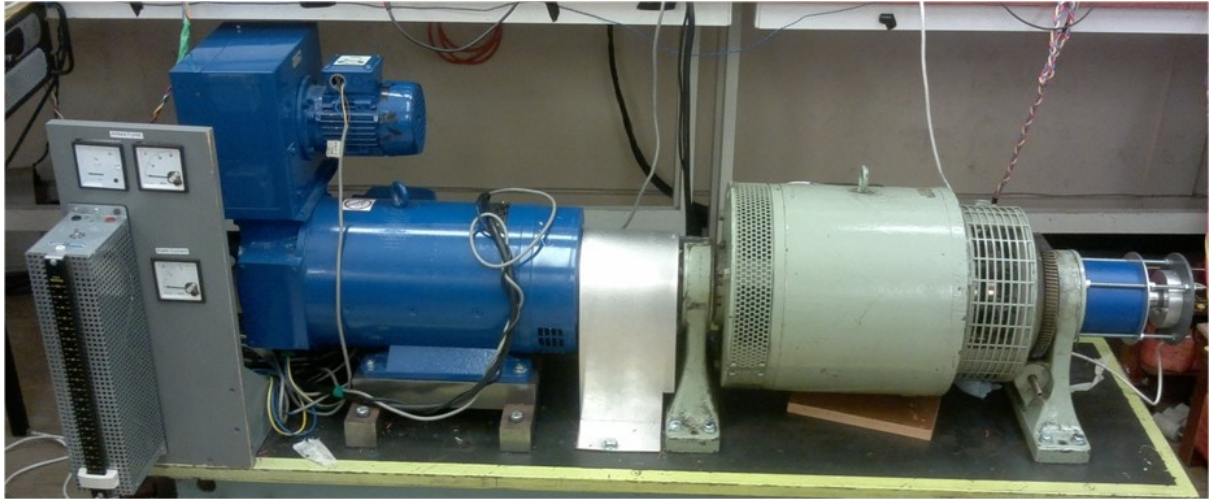


Figure B. 7 Motor generator set

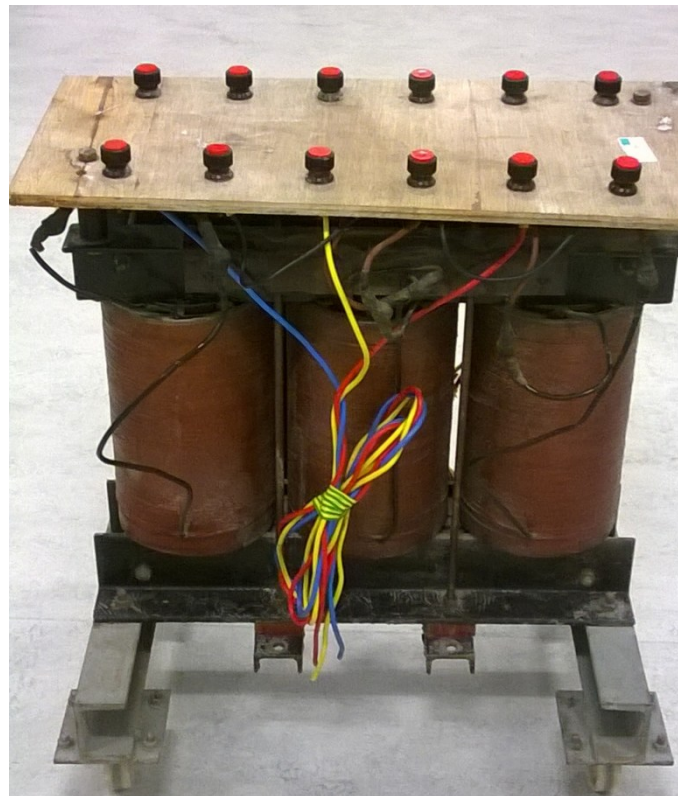
Table B.1 Motor generator set parameter

DC motor parameter	
Power rating	7.2kW
Speed	2500rpm
Armature voltage	460V
Armature current	18.5A
Field voltage	360V
Field current	1.9A
Synchronous generator parameter	
Rating	6.9kVA
Speed	1500rpm
Phase Voltage	400V
Phase current	10A
Power factor	0.8
Excitation voltage	140V
Excitation current	2.5A

B.5 Transformers

Two transformers are used during this research, first: three-phase shown Figure B. 8(a) its rated power 8kVA and phase voltage 460/230V. The second transformer is 2kVA phase shift transformer shown Figure B. 8(b) its, where it primary winding is

star connected (rate line voltage =415V), secondary and tertiary windings delta and star connected respectively (rated voltage=205V).



(a) three-phase transformer



(b) phase-shift transformer

Figure B. 8 transformer used

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Appendix D

Summary of Relevant Published Work by the Author

[1] I. Abdelsalam, G. Adam, D. Holliday, and B. Williams, "Assessment of a wind energy conversion system based on a six-phase permanent magnet synchronous generator with a twelve-pulse PWM current source converter," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, 2013, pp. 849-854.

Abstract –

The steady-state and dynamic performances of a new high-power variable speed wind-energy conversion system (WECS) that uses a six-phase permanent magnet synchronous generator (PMSG) with twelve-pulse back-to-back pulse width modulated current source converters is assessed. The proposed WECS inherently has all the features of existing systems based on voltage source converters, such as voltage control and fault ride-through capability, but with increased reliability and improved ac side waveform quality, benefiting from the three winding phase shifting transformer for further attenuation of the low-order harmonics. PSCAD/EMTDC simulation is used to assess the steady-state and dynamic behaviours of the proposed system under different operating conditions. Experimental results, obtained using a prototype grid side dual current source inverter (CSI), are presented to validate the proposed technique.

[2] I. Abdelsalam, G. Adam, D. Holliday, and B. Williams, "New back-to-back current source converter with soft start-up and shutdown capabilities," in *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on*, 2014, pp. 1-5.

Abstract –

Back-to-back voltage source and current source converters are key components of many power conversion systems. Various topologies have evolved around these conventional voltage and current source converters in an attempt to meet different design and reliability constraints. This paper proposes a new back-to-back current source converter that avoids the problem of excessive voltage stresses on the switching devices associated with the traditional current source converter. Its main features are reduced power circuit and control complexity, and sinusoidal ac currents with high power factor achieved at both ac sides at reduced switching frequency. Basic relationships that govern steady-state converter operation are established, and filter design is included. PSCAD/EMTDC simulations and experimentation are used

to demonstrate the practicality of the proposed power conversion system, and results show that the converter has good dynamic performance, with near unity input power factor over an extended operating range.

[3] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Single-stage, single-phase, ac–dc buck–boost converter for low-voltage applications," *IET Power Electronics*, vol. 7, pp. 2496-2505, 2014.

Abstract –

The suitability of a single-stage ac–dc buck–boost converter for low-voltage applications is investigated. In-depth discussion and analysis of the converter's operating principle, basic relationships that govern converter steady-state operation and details of the necessary control structures needed to comply with the grid code are provided. The validity of the proposed system is confirmed using power system computer aided design (PSCAD)/electromagnetic transients including DC (EMTDC) simulations, and is substantiated experimentally. The buck–boost converter under investigation has good dynamic performance in both buck and boosts modes, and ensures near unity input power factor over the full operating range, whilst having fewer devices and passive elements than other published versions of the buck–boost converter.

[4] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Modified back-to-back current source converter and its application to wind energy conversion systems," *IET Power Electronics*, vol. 8, pp. 103-111, 2014

Abstract –

The back-to-back (BTB) converter is used in power conversion applications such as machine drives, wind energy conversion systems (WECS), uninterruptible power supplies and high-voltage, direct current transmission systems. Various topologies have evolved around voltage source converters and current source converters (CSCs) in an attempt to meet various design and reliability constraints. This paper proposes a new CSC-based BTB converter suitable for WECS application. The proposed configuration addresses the main drawbacks of the conventional BTB CSCs, such as the over-voltage frequently experienced by switches during commutation. The inverter side converter has zero switching losses. The proposed WECS offers the following advantages: simple and easy control reduced switching frequency and maximum power point tracking with controllable grid active and reactive power. A low-voltage ride-through (LVRT) solution is also provided in the proposed WECS. PSCAD/EMTDC simulation is used to assess the steady-state and dynamic behaviours of the proposed system under different operating conditions and during LVRT. Experimental results allow steady-state and dynamic behaviour assessment of the proposed system under different operating conditions.

[5] I. Abdelsalam, G. P. Adam, D. Holliday, and B. W. Williams, "Three-phase ac–dc buck–boost converter with a reduced number of switches," *IET Renewable Power Generation*, 2015.

Abstract –

A single-switch, single-stage, three-phase ac–dc buck–boost converter suitable for medium-voltage applications is proposed. Basic relations that govern steady-state converter operation are established, confirmed using PSCAD/EMTDC simulations, and substantiated experimentally. Simulation and experimental results establish that the proposed converter has good dynamic performance in buck and boost modes, with near unity input power factor.

[6] G. Adam, I. A. Abdelsalam, K. H. Ahmed, and B. W. Williams, "Hybrid Multilevel Converter With Cascaded H-bridge Cells for HVDC Applications: Operating Principle and Scalability," *IEEE TRANSACTIONS ON POWER ELECTRONICS*, vol. 30, pp. 65-77, 2015.

Abstract –

Hybrid multilevel converters are contemplated in an attempt to optimize the performance of voltage source converters in terms of magnitude of semiconductor losses and converter footprint, and to achieve additional features such as dc short circuit proof, which is essential for a high integrity multi-terminal HVDC grid. Therefore, this paper considers an emerging hybrid cascaded converter that offers the dc side short circuit proof feature at reduced loss and footprint compared to the existing multilevel and other hybrid converters. Its operating principle, modulation and capacitor voltage balancing strategies are described in detail. Furthermore, hybrid converter scalability to high voltage applications is investigated. The validity of the modulation and capacitor voltage strategy presented are confirmed using simulation and experimentation. The hybrid cascaded converter is extendable to a large number of cells, making it applicable to high voltage applications, and operation is independent of modulation index and power factor. On these ground, the converter is expected to be applicable for both real and reactive power applications.

[7]G. Adam, I. Abdelsalam, S. Finney, D. Holliday, B. Williams, and J. Fletcher, "Comparison of two advanced modulation strategies for a hybrid cascaded converter," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, 2013, pp. 1334-1340.

Abstract –

This paper summarises an investigation into two modulation strategies that enable a hybrid cascaded multilevel converter to reduce on-state losses and extend the modulation index linear range independent of load power factor, and without capacitor voltage balancing problems. The first modulation strategy exploits

unconventional triplen harmonics in combination with a hybrid modulation strategy to optimally reduce the number H-bridge cells required to minimize semiconductor losses, and improve capacitor voltage balancing of the H-bridge cells. The second modulation strategy is based on level-shifted multilevel carriers and exploits 3rd harmonic subtraction to modify the modulating signals in order to extend the regions around zero voltage crossing where cell capacitor voltage balancing can be achieved, with a minimum number of cells. It is shown that both modulation strategies overcome the traditional limitations of hybrid cascaded converter such as dependency of the capacitor voltage balancing on modulation index and load power factor. Also they extend the modulation linear range virtually up to 1.27 in real power applications. Simulation and experimental results at several operating points are used to substantiate the strategies presented in this paper.