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Grid Integration of Renewable Power Generation

by

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of degree.

Signed: *S. Azmi*

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Abstract

This thesis considers the use of three-phase voltage and current source inverters as interfacing units for renewable power, specifically photovoltaic (PV) into the ac grid. This thesis presented two modulation strategies that offer the possibility of operating PV inverters in grid and islanding modes, with reduced switching losses. The first modulation strategy is for the voltage source inverter (VSI), and exploits 3rd harmonic injection with selective harmonic elimination (SHE) to improve performance at low and high modulation indices, where the traditional SHE implementation experiences difficulties due to pulse dropping. The simulations and experimentation presented show that the proposed SHE allows grid PV inverters to be operated with less than a 1kHz effective switching frequency per device. This is vital in power generation, especially in medium and high power applications. Pulse dropping is avoided as the proposed modified SHE spreads the switching angles over 90^{o}, in addition increasing the modulation index.

The second proposed modulation strategy, called direct regular sampled pulse width modulation (DRSPWM), is for the current source inverter (CSI). It exploits a combination of forced and natural commutation imposed by the co-existence of an insulated gate bipolar transistor in series with a diode in a three phase current source inverter, to determine device dwell times and switching sequence selection. The DRSPWM strategy reduces switching frequency per device in a CSI by suspending each phase for 60^{o}, similar to VSI dead-band, thus low switching losses are expected. Other benefits include simple digital platform implementation and more flexible switching sequence selection and pulse placement than with space vector modulation. The validity of the DRSPWM is confirmed using simulations and experimentation.

This thesis also presents a new dc current offset compensation technique used to facilitate islanding or grid operation of inverter based distributed generation, with a reduced number of interfacing transformers. The proposed technique will enable transformerless operation of all inverters within the solar farm, and uses only one power transformer at the point of common coupling. The validity of the presented modulation

strategies and dc current offset compensation technique are substantiated using simulations and experimentation.

List of Symbols

C_f, C_F	Filter capacitance (F)
f_{cr}	Carrier frequency (Hz)
f_{sw}	Switching frequency (Hz)
I_{dc}	dc-link current (A)
I_g	Grid current vector (A)
I_m	Peak phase current (A)
I_{pv}	Photovoltaic output current (A)
i_{ca}, i_{cb}, and i_{cc}	Instantaneous capacitor currents (A)
i_{ia}, i_{ib}, and i_{ic}	Instantaneous inverter currents (A)
i_{oa}, i_{ob}, and i_{oc}	Instantaneous output currents (A)
k_p, k_i	Proportional and integral control parameters
L_f, L_F	Filter inductance (H)
m, m_a	Modulation index
N	Transformer turns ratio
P	Active power (W)
Q	Reactive power (VAr)
R_f, R_F	Filter resistor (Ω)
T_s	Switching period (s)
V_{cr}, $\hat{V}_{cr}$	High frequency carrier voltage (V)
V_{dc}	dc-link voltage (V)
V_g	Grid voltage vector (V)
V_m, $\hat{V}_m$	Peak fundamental voltage (V)
V_{pv}	Photovoltaic output voltage (V)
v_{ca}, v_{cb}, and v_{cc}	Instantaneous capacitor voltages (V)
v_{cr}	High frequency carrier signal (V)
v_{ma}, v_{mb}, and v_{mc}	Modulating signals (V)
v_{oa}, v_{ob}, and v_{oc}	Instantaneous load voltages (V)
δ	Load angle (rad)
Φ	Phase angle (rad)

ω	Supply frequency (rad/s)

List of Abbreviations

CSI	Current source inverter
DG	Distributed generation
DRSPWM	Direct regular sampled pulse width modulation
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated gate bipolar transistor
MPPT	Maximum power point tracking
NPC	Neutral point clamping
PCC	Point of common coupling
PI	Proportional integral
PLL	Phase locked loop
PWM	Pulse width modulation
PR	Proportional resonance
PV	Photovoltaic
SHE	Selective harmonic elimination
SPWM	Sinusoidal pulse width modulation
STATCOM	Static synchronous compensator
SVM	Space vector modulation
THD	Total harmonic distortion
THIPWM	Third harmonic injection pulse width modulation
VSI	Voltage source inverter

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Chapter One

Introduction

1 Background and development of renewable energy systems

In the last two decades, environmental organizations have encouraged the power industry to use renewable power such as wind, photovoltaic, and tidal instead of fossil fuels, as a means to combat climate change. After years of research and development of hydroelectric, wind and photovoltaic (PV) energy sources, the economical and technical feasibility of these forms of power has extended to a large-scale level, but they remain expensive compared to fossil fuels[1.1-4]. Rethinking of the whole power industry approach to renewable power is on-going.

Renewable energy production rose from 4225.2TWh to 4447.5TWh between 2010 and 2011, representing a 20.2% share of the total global electricity production. Table 1.1 lists the global fraction of electricity production from various renewable sources in 2011. China ranks as the highest renewable energy producer with 785.9TWh, followed by the United States (555.6TWh), Brazil (450.8TWh), Canada (403TWh), and Russia (166.7TWh). The United Kingdom is placed 19th among the global producers of renewable energy production, with 37.6TWh [1.5, 6].

Table 1.1: Total electricity production from renewable sources in 2011.

Source	Electricity production (TWh)	Percentage relative to the total production (%)
Hydraulic	3579.5	80.5%
Wind	459.9	10.3%
Biomass	276.0	6.2%
Geothermal	69.9	1.6%
Solar	61.6	1.4%
Marine energies	0.5	0.01%
Total	4447.5	100%

The use of renewable energy resources, rather than fossil fuel and other non-renewable energy sources, led to positive consequences and impact on the climate and environment. These include low greenhouse gas emissions and polluting gases [1.7]. Among these renewable power sources, wind farms have raised several social and technical concerns. Examples of social concerns are the generated noise from the wind turbines and an unpleasant scenery, such that these concerns complicate the process of obtaining permission to build new onshore wind farms[1.8, 9]. Unlike wind energy, a photovoltaic system is a static device and does not produce noise or pollution; therefore it is suitable and safe for use in residential areas or large-scale onshore PV farms.

1.1 Development of renewable energy systems in the UK

Due to geographical location and unpredictable weather conditions, it is expected that photovoltaic systems are not suitable for the UK. However, with the advancement of the photovoltaic system, they can operate without the need of large amounts of sunlight. In 2007, the UK government agreed with the EU's target to increase the Union's portion of the total energy consumption from renewable energy sources to 15%by 2020. The Government's effort continues by introducing a system called Feed-In Tariff in April 2010 to support the usage of photovoltaic (roof-mounted or standalone), wind turbine (building mounted or free standing), hydroelectric, anaerobic digester, and micro combined heat and power (CHP). The system supports householders and communities in generating their own power with regular payment through their energy supplier. According to the Feed-In Tariff, there are approximately 174,988 photovoltaic sites in England with cumulative installed capacity of 573.3MW, 19,138 sites in Wales (46.3MW), 12,808 sites in Scotland (41.2MW), and 204 sites in Northern Ireland (0.7MW).As for onshore wind farms (dated construction finished by April 2013), Scotland holds the largest installed capacity of 1,845.9MW, followed by England (124.8MW), Wales (58.5MW) and North Ireland (54MW).Whilst, England is leading for operational offshore wind farms with a capacity of 2,969.2MW, this is followed by Scotland with 190MW and Wales with 150MW. The world's largest offshore wind farm is the London Array, located off-coast at Kent, England with a capacity of 630MW[1.10-12].

1.2 Application of distributed generation based renewable energy sources

Distributed generation is a form of decentralised electricity generation that permits a large number of medium-scale generating units, with a high concentration of inverter connected renewable energy based generation. This generation type is expected to be connected to the distribution network rather than a high voltage transmission network, or can be connected to form a so called micro-grid. The development of distributed generation based renewable energy systems has an important role in long term environmental targets. The main aims of such systems are to increase the network connection capacity by allowing more consumers and producer customers connections without creating new reinforcement costs, to enhance the reliability of the system, and to improve the overall supply quality with modern voltage control [1.13].

There are two major application modes that can be beneficial when using distributed generation system based renewable energy sources: island and grid connected modes. In the island mode of operation, the unit operates as an independent voltage source, without connection to the utility grid. Since this system is the source of power, it must be able to specify and control the voltage and frequency of its output. The dedicated control system in this mode must provide sufficient active and reactive power to match the connected loads whilst delivering output voltage with high power quality. The island mode based distributed generation isolates the user from the grid either by choice or circumstance, as in remote applications. The units are parallel connected to supply all the local loads. Power converters are designed to share the local loads and also to be controlled from a remote supervisory controller that can set the load contribution of each unit [1.14].

The grid is an integrated network of generation, high-voltage transmission, substations, and local distribution. Grid connected renewable energy systems (wind and photovoltaic) are designed to operate in parallel with the utility grid. The features of a grid connected mode include active and reactive power control with sufficient output current quality, good parallel load sharing operation, and establishment of frequency and voltage levels [1.15]. As the power generated by medium-scale renewable based

distributed generation is much smaller than that of the utility grid, there is no need to worry about the power balance.

1.3 Motivation

One of the main challenges in a distributed generation system is to connect hundreds or thousands of renewable energy systems to the utility/grid network. If the distributed energy sources are not properly connected, the grid can become unstable or even fail. This challenge is largely handled by power electronic converters.

Power electronic converters play an important role in distributed generation and in the integration of renewable energy sources into the electrical grid. They are widely used and rapidly expanding as these applications become more integrated with the grid-based systems. The main tasks of the power electronic converters are [1.16-18]:

- Maximum power transfer: on the input side (source), power electronics permit control and tracking of pre-defined power characteristic curves to maximize power extraction from the resources. Also, in the event of faults and sudden load variations, power electronics help to adjust the power extraction level and protects the sources.
- Active and reactive power control and power quality control: on the grid side, power converters must control active and reactive power injection into the grid, ensuring sinusoidal current is injected into grid, with low harmonic content, low electromagnetic interference, low leakage dc currents that meets grid codes and standard.

Although the power electronic converter is an efficient unit in the integration of distributed generation based renewable energy sources, it is the most susceptible unit to failure which may lead to major breakdown of a power plant. A statistic for wind power system failures, based on Swedish wind power plant in 2000 to 2004, shows that nearly 50% of the failures are caused by the power electronic converter[1.19]. Similarly in photovoltaic systems, for example, the Florida Solar Energy Center has recorded 213 failure events on 130 grid-connected PV systems from 1999 to 2003, where 65% of those failures are contributed by inverters[1.20, 21]. Thus, the issue of reliable and

efficient inverter design and inverter control systems are the main concerns for manufacturers, researchers and users when operating renewable energy systems.

Another issue related to massive penetration of distributed generation based renewable energy sources is the impact on grid stability [1.22, 23]. This issue has caused grid operators in many countries to upgrade their connection codes to ensure the safety and reliability of the network. In most countries, local regulations are imposed by the utility or the government. However, many organizations are working towards imposing grid requirement standards that can be adapted by most countries. The organizations are The Institute of Electrical and Electronic Engineers (IEEE) and International Electrotechnical Commission (IEC). Examples of IEEE and IEC standards, used as the main reference in this thesis, are IEEE-1547and IEC-61727. The IEEE-1547 standard deals with interconnecting distributed generation to the electric power system and the IEC-61727 standard is for Photovoltaic Systems-Characteristics of the Utility Interface [1.24, 25]. Table 1.2summarises some of the important issues listed in both the IEEE-1547 and IEC-61727 standards.

Table 1.2:Summary of some important issues in the IEEE1574 and IEC61727 standards.

Issues	IEEE1574	IEC61727
Nominal power	30 kW	10 kW
Harmonic current (order-h) limits	(2-10) 4.0% (11-16) 2.0% (17-22) 1.5% (23-34) 0.6% (>35) 0.3%	(3-9) 4.0% (11-15) 2.0% (17-21) 1.5% (23-33) 0.6%
	Even harmonics in these ranges shall be less than 25% of the odd harmonic limits listed.	
Maximum current THD	5.0%	
DC current injection	Less than 0.5% of rated output current	Less than 1.0% of rated output current
Frequency range for normal operation	59.3 Hz to 60.5 Hz	50±1 Hz

Grid connected inverters have to meet strict codes imposed by IEEE and IEC standards [1.26]. For example in Table 1.2, the current harmonic injection into the grid must not exceed 5%,with limitations imposed on individual harmonics as a percentage of the fundamental component. One widely used strategy to control the quality of injected output current into the grid, is the pulse width modulation technique. The modulation

technique is at the heart of the majority power electronic inverters with the target to reduce harmonic distortion and increased output magnitudes for a given switching frequency. Other performance criteria include minimization of switching losses and simple implementation, which are some of the challenges in selecting a suitable modulation technique[1.27].

DC current injection issues in grid connected inverters have been largely overlooked, despite growing concerns regarding the effect of dc current injection on distribution system components. The most severe problems that can be caused are saturation of the distribution transformers which results in waveform distortion, excessive losses, overheating and reduced lifespan [1.28]. The IEEE and IEC standards have been imposed to minimize the impact of dc current injection into the ac grid. The allowable limits range from 0.5% and 1% of the rated output current, as listed in Table 1.2 for low-voltage applications. However, these regulations and standards do not guarantee that the accumulative effect of numerous power converters connected to the grid remains acceptable, with no harmful effects to electric systems sensitive to dc components. Various methods have been proposed to prevent or minimize dc current injection into the ac grid, and have attract considerable interest and attention.

1.4 Objectives

In this thesis, three-phase voltage and current source inverters for grid integration are discussed, focusing on the following aspects: modulation strategies with the aim to ensure low inverter-semiconductor loss and guarantee acceptable power quality of the output voltage and current waveforms in accordance with the grid codes. In attempting to achieve these objectives, a number of new modulation strategies for low-loss, medium-voltage, three-phase current and voltage source inverters are proposed. These modulation strategies shown promising results, and other benefits such as simple implementation using digital platforms. Additionally, this thesis presents a new dc current offset compensation technique that may facilitate islanding or grid mode operation of distributed generation, with a reduced number of interfacing transformers. The proposed technique may have significant implication in the overall cost of medium-scale solar farms.

1.5 Methodology and scope of study

This thesis uses simulation and experimentation as the two main tools to assess and validate the technical viability of each modulation strategy and dc compensation techniques presented. The theoretical basis of each proposed strategy or technique is provided and supported with quantitative and qualitative analysis. Despite control not forming the main core of this thesis, significant effort has been devoted to the presentation of the control systems needed to facilitate safe operation of the simulation and experimental setups. Systematic derivation of the control structures and designs is presented appropriately to assist readers to replicate the material presented in this thesis. The level of details presented on the core power electronic device related topics such as modulation and control designs are kept within the appropriate level for a wide range of readers.

1.6 Thesis organization

The thesis is organized into eight chapters: Chapter One provides the general background to the drivers behind distributed generation in the context of grid and island modes, and highlights the challenges in grid interfacing of renewable power in generation, including PV systems. This chapter also presents some of the motivation, scope and methodology of this thesis.

Chapter Two provides a brief review and discussion of different voltage source inverter topologies, and articulates their suitability for PV systems.

As part of the contribution of thesis in the exploitation of converter modulation to reduce power loss and simplify digital implementation, Chapter Three discusses a number of existing pulse width modulation (PWM) techniques in general, with emphasis on the suitability of techniques for power generation in a harsh grid mode.

Chapter Four presents detailed discussion of the grid connected voltage source inverter with the implementation of existing modulation schemes and the proposed improved selective harmonic elimination (SHE) that exploits 3^{rd} harmonic elimination. Using

simulation and experimentation, this chapter demonstrates that the three-phase voltage source inverter can be operated in the grid mode when the effective switching frequency is less than 1kHz, without compromising control of the active and reactive powers.

Chapter Five discusses possible current source inverter topologies that can be used as a grid interfacing unit. A new modulation strategy, called direct regular-sampled pulse width modulation (DRSPWM), is proposed that offers distinctive features compared to existing modulation strategies. A thorough comparison of the proposed modulation strategy and existing modulation strategies for the three-phase current source inverter are presented. Simulation and experimentation are used to substantiate the outcomes of the comparisons.

Chapter Six discusses several methods claimed to be appropriate to compensate dc current offset injected by grid connected inverters. This thesis presents a dc current offset injection compensation technique that exploits a simple resonance controller, with possible incorporation of a proportional-integral controller to reduce capital cost of medium-scale solar farms. The proposed technique permits transformerless inverter operation within the solar farm, and uses a single transformer at the point of common coupling to the grid.

Chapter Seven demonstrates the viability of the proposed DRSPWM discussed in chapter five, when a current source inverter is operated in grid and island modes. This chapter also presents possible control structures that can be used to control a current source inverter in the grid mode. It is shown that the current source inverter has the potential to match the voltage source inverter over the entire operating range, including lagging, leading, and zero power factor.

Chapter Eight draws general conclusions, author contributions and some recommendations for future research.

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Chapter Two

Voltage Source Inverter Topologies

2.0. Introduction

This chapter discusses the different voltage source inverter (VSI) topologies commonly used in distributed generation systems, particularly in photovoltaic systems, and highlights the features of each topology. The suitability of each topology for grid-connected photovoltaic application is also discussed. Among the topologies discussed are: single-phase half and full bridge inverters, the three-phase two-level inverter, the neutral-point clamped (three-level diode clamped) inverter, the three-level flying capacitor inverter, the cascaded multilevel inverter with electrically isolated dc sources, and the modular multilevel inverter. However, of these topologies only the three-phase two-level VSI is deemed appropriate for subsequent chapters, which focus on grid integration of photovoltaic inverters.

2.1. Background

The power electronic interface is an important part of distributed generation units as it influences the overall system efficiency and performance. Since photovoltaic (PV) cells generate low voltage dc, normally dc-ac power converters are used to convert the generated dc power into ac, with suitable ac voltage that matches the ac utility. To maximize energy capture from such renewable energy sources, the converters also track the PV maximum power point (MPP)[2.1, 2]. Such power tracking systems are desirable because they speed up the investment return. At present, single-stage and two-stage arrangements are two competing solutions used for grid interfacing of PV systems [2.3]. In a single-stage grid-connected system, the PV system utilizes a single conversion unit (normally dc-ac power inverter) to track the MPP and to interface the PV system to the grid, as illustrated in Figure 0.1(a). Using this concept, the PV maximum power is delivered into the grid with high efficiency, small size and low cost. In order to be able to connect to the grid, such a topology requires either a step-up

transformer or a PV array with high dc voltage output, which can be realized using a string of series connected PV modules [2.4]. The disadvantages of these single stage solutions can be summarised as follows:

- A PV array with a large dc voltage increases control complexity and excites high leakage current between the panels and the system ground through parasitic capacitances. Also, this approach exacerbates partial shading problems.
- Using PV panels with low dc voltage and a step-up transformer to match the inverter output to the grid, increases inverter losses. This solution is also limited to small-scale applications. In addition, a 50/60Hz matching transformer is bulky.

For single-stage arrangements, different types of dc-ac inverters, such as single-phase half-bridge and full-bridge inverters, three-phase two-level inverters, and multilevel inverters, can be used. From these, there are two inverter topologies that are commonly used as grid interfacing unit of photovoltaic system; voltage source inverter and current source inverter. The use of current source inverter topologies will be discussed further in Chapter 5.

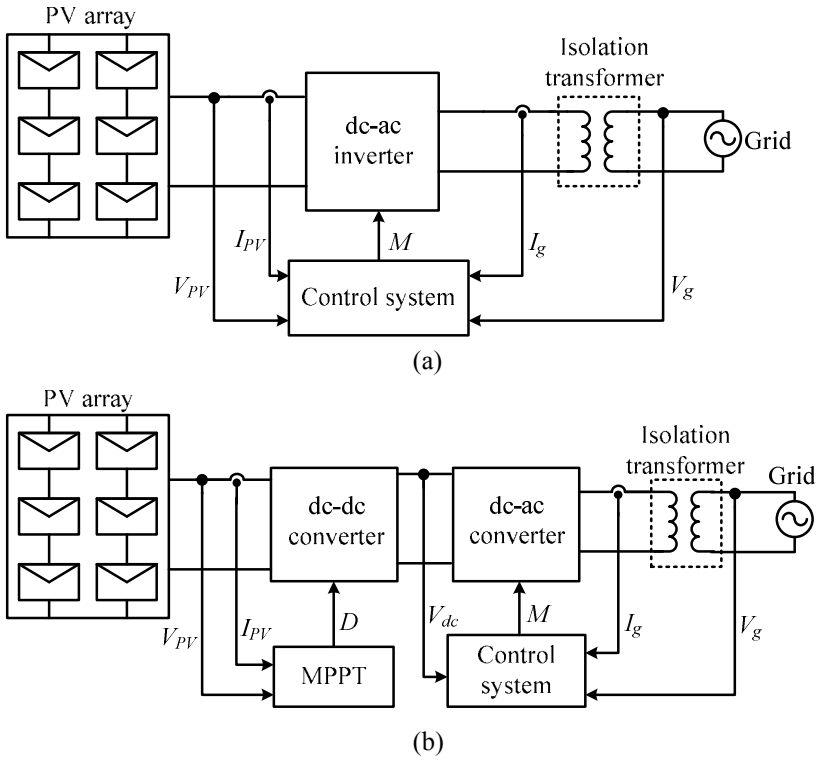

Figure 0.1: General block diagram of (a) single-stage arrangement grid connected PV system and (b) two-stage arrangement grid connected PV system.

For two-stage arrangements, a step-up dc-dc inverter can be used to boost the PV output voltage and perform maximum power tracking, while a dc-ac inverter is used to regulate the dc link voltage and provide a clean ac output current to the grid, as shown in Figure 0.1(b). The main advantage of this solution is the simplicity of the control structure since the control requirements are distributed between the two stages. Additionally, a PV array with a high dc voltage is not required, because the dc-dc converter boosts the voltage to the desired level. Since this topology consists of a two-stage arrangement, the system efficiency is expected to be lower and the cost is increased, compared to a single-stage arrangement [2.5].

2.2. DC-AC power inverter topologies

2.2.1. Single-phase half-bridge inverter

The topology of a half-bridge VSI is shown in Figure 0.2, where two dc capacitors are required to provide a return path for the load current, and ensure the inverter output voltage is modulated between $\pm\frac{1}{2}V_{dc}$. An additional benefit of having such capacitors is that the interfacing transformer no longer needs to be designed to block dc voltage stresses. Since the inverter output current does contain a significant dc offset, the voltage across these capacitors will remain virtually constant at $\frac{1}{2}V_{dc}$ (for an input dc voltage V_{dc}). Table 0.1 lists the two switch states and the corresponding output voltages of the single-phase half-bridge inverter. The switches S_1 and S_2 must not be turned on simultaneously to avoid a short circuit across the dc-link. Such a consideration is normally incorporated into the modulating technique in the form of dead time. This dead time guarantees complementary operation of switches S_1 and S_2. The same principle is applicable to other VSI topologies.

The VSI uses self-commutated switching devices, which must be able to conduct current in both directions to ensure bi-direction power flow capability. For this reason, a VSI uses insulated gate bipolar transistors (IGBTs) with inverse anti-parallel diodes.

The single-phase half-bridge inverter in Figure 0.2 can be controlled using selective harmonic elimination (SHE) or high-frequency carrier based pulse-width modulation. However, SHE is not suitable for single-phase inverters because all the low-order odd harmonics needed to be eliminated, including the triplen. By doing so, the dc link

voltage utilization is reduced (corresponding modulation index m_a=1), and the system may suffer from high switching losses. Therefore, carrier based pulse width modulation (PWM) is favoured [2.6]. The same principle is applicable to most VSIs, with some minor modifications.

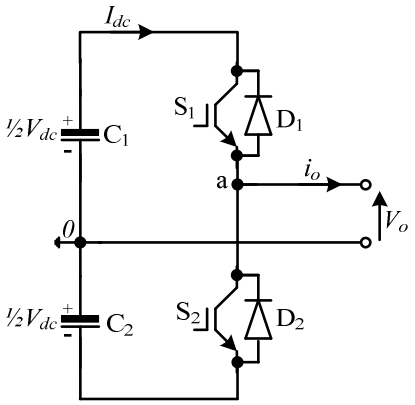

Figure 0.2: Topology of half-bridge single-phase VSI.

Table 0.1: Switch states and the outputs.

Output voltage	Switch states		Power path	
	S_1	S_2	$i_0>0$	$i_o<0$
$½V_{dc}$	ON	OFF	S_1C_1	D_1C_1
$-½V_{dc}$	OFF	ON	D_2C_2	S_2C_2

2.2.2 Single-phase full-bridge inverter

Figure 0.3 shows the schematic of a single-phase full-bridge inverter, which is also called an H-bridge, due to the arrangement of the power switches and the load. This inverter topology generates three voltage levels, $\pm V_{dc}$, and 0 at the inverter output. Table 2.2 summarises the switch combinations that can be utilized to generate the output voltage of the single-phase H-bridge inverter, assuming V_{dc} is the input dc voltage [2.6, 7].In single-phase inverter systems, the dc input current is pulsating, hence the power pulsates and a relatively large dc-link capacitor is required[2.8]. A pulsating input dc current may affect the lifetime of the PV arrays and the input filter capacitor. A single-phase topology is usually used with 50/60Hz transformer isolation as a grid-connected inverter for residential or small-scale PV systems, for powers between $1kW_{peak}$ and $6kW_{peak}$[2.4, 9-12].

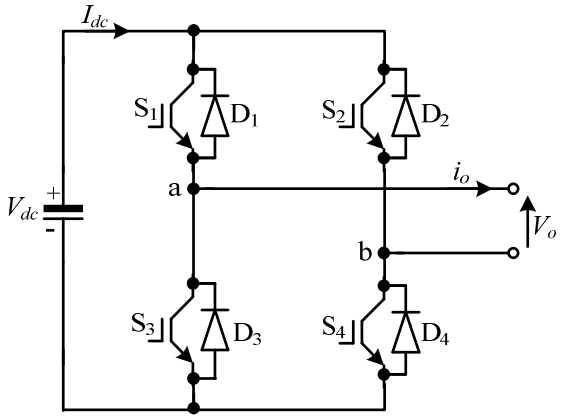

Figure 0.3: Topology of H-bridge single-phase VSI.

Table 0.2: Summary of the switch states of a single-phase H-bridge inverter that can be used to generate a three-level output voltage.

Output voltage	Switch states				Power path	
	S_1	S_2	S_3	S_4	$i_o>0$	$i_o<0$
V_{dc}	ON	OFF	OFF	ON	S_1S_4	D_1D_4
0	ON	ON	OFF	OFF	S_1D_2	S_2D_1
	OFF	OFF	ON	ON	S_4D_3	S_3D_4
$-V_{dc}$	OFF	ON	ON	OFF	D_2D_3	S_2S_3

2.3. Three-phase two-level voltage source inverter

The topology in Figure 0.4 is basically an extension of the half-bridge version of the single-phase inverter, by combining three legs to form a three-phase two-level VSI. Each phase of a three-phase two-level inverter generates two voltage levels, $\pm½V_{dc}$, as with the half-bridge version. The control strategy is similar to that of the single-phase inverter, except the reference signals for the different phase-legs are shifted 120^o from each other. The main advantages of this topology is that all triplen harmonics such as3^{rd}, 9^{th}, 15^{th}, etc. are eliminated in the line-to-line output voltage, so they will not appear in the currents in a three wire system [2.6, 13]. Since the sum of the currents in a balanced three-phase system is zero, the instantaneous ac output power is constant. Hence, dc input power and current are constant but also include some high switching frequency components that result from the modulation process. This means a relatively small dc capacitor is sufficient to filter these high switching frequency components. The constant dc input current is one of the features that make three-phase VSI an attractive interfacing option for PV systems (or any constant dc energy source)[2.14].

Three-phase two-level VSI has inherent features such as generation of leading and lagging reactive power, high power density (MVA per unit volume), fast dynamic response, and ability to operate under challenging conditions in medium and high-voltage applications[2.15]. These features make the three-phase two-level VSI the favourite candidate for medium and large scale solar farms [2.16-18]. The three-phase two-level inverter in such applications uses a relatively high switching frequency to minimize the ac filter size and to achieve a high dynamic response, but this can also be considered as its main disadvantage. This is because such a high switching frequency increases the *dv/dt* stresses on the interfacing transformers, hence imposing high insulation requirements to withstand switching of large voltage steps at high frequency (1kHz to 2kHz) [2.19].Since galvanic isolation is a requirement imposed by many grid codes for medium and large scale grid connected inverters, a transformerless solution is a viable option to reduce cost but only at a power level permitted by the grid code. In PV applications, the three-phase two-level VSI is the most commonly used interface unit between the PV panels and the ac grid, due to its simplicity and availability [2.3, 16, 18, 20-23].

The three-phase two-level VSI in Figure 0.4 can be controlled using most known modulation techniques, such as carrier based modulation techniques, as with the single-phase inverter and its derivatives (sinusoidal with some form for of 3rd harmonic injection), space vector modulation, and selective harmonic elimination. Details of these modulation strategies will be discussed in the subsequent chapters.

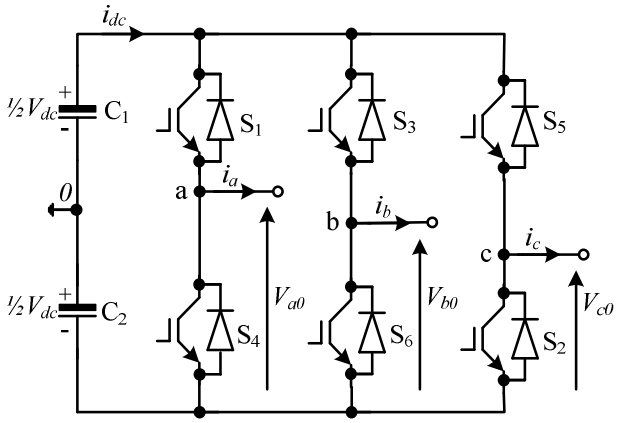

Figure 0.4: Topology of three phase two-level VSI.

2.4. Multilevel inverter

Recently, multilevel inverters have attracted attention because of their ability to overcome three-phase two-level VSI problems such as high voltage stress on the power switches and interfacing transformer, and high power losses due to a high switching frequency. Additionally, they offer lower THD (total harmonic distortion) due to a phase output voltage formation using small voltage steps with reduced switching frequency per device, low *dv/dt*, and a low common mode voltage [2.19, 24-26]. However, these advantages are achieved at the expense of increased power circuit complexity. Also a bulky transformer and an electrolytic capacitor are still required to meet galvanic isolation in a grid mode. A few multilevel inverter topologies are used in PV systems, namely the neutral-point clamped inverter, cascaded with electrically isolated inverter, and modular multilevel, which are briefly discussed in the following sections.

2.4.1. Neutral-point clamped inverter

Figure 0.5 show one phase of the neutral-point clamped inverter (also known as a three-level diode clamped inverter) that can generate three output levels $\pm\frac{1}{2}V_{dc}$ and 0 between phase '*a*' and reference point '0'. Table 0.3 lists the switch states of neutral-point clamped inverter and their corresponding output voltages. The voltage across each dc-link capacitor must be maintained at $\frac{1}{2}V_{dc}$ in order to ensure the voltage stress on each individual device is limited to $\frac{1}{2}V_{dc}$ [2.19, 27]. The use of high frequency PWM to control the switches of the neutral-point clamped inverter will suppress the voltage harmonics around and beyond the switching frequency components, and therefore allows the use of small ac output filters to attenuate these high frequency harmonics.

In the past there was expectation of extending the diode clamped inverter to generate more than three voltage levels. However, this did not materialise as dc link capacitance balancing proved to be impossible over the entire inverter operating range when the number of levels exceeded three. For this reason most of the practical applications of the diode clamped inverter are limited to the three-level inverter (NPC) and its derivative, the active neutral-point clamped (ANPC) inverter. The NPC or ANPC converter preserve the advantages of the two-level three-phase inverter, offer additional

benefits such as reduced switching losses and low *dv/dt*, and permit the use of relatively small ac filters [2.28, 29].

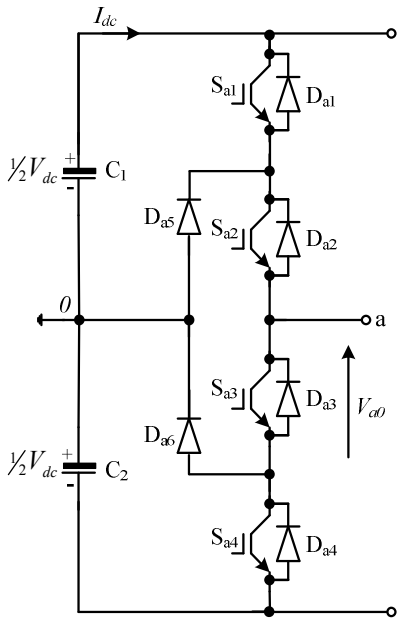

Figure 0.5: Topology of one-phase of neutral-point clamped inverter.

Table 0.3: Summary of the switch state combinations and their corresponding output voltage.

Output voltage level V_{a0}	Switch states				Current polarity	Current path
	S_{a1}	S_{a2}	S_{a3}	S_{a4}		
$+\frac{1}{2}V_{dc}$	ON	ON	OFF	OFF	$i_a>0$	S_{a1},S_{a2}
					$i_a<0$	D_{a1},D_{a2}
0	OFF	ON	ON	OFF	$i_a>0$	D_{a5},S_{a2}
					$i_a<0$	S_{a3},D_{a6}
$-\frac{1}{2}V_{dc}$	OFF	OFF	ON	ON	$i_a>0$	D_{a3},D_{a4}
					$i_a<0$	S_{a3},S_{a4}

2.4.2. Capacitor-clamped multilevel inverter

Figure 0.6 shows one phase of the three-phase flying capacitor multilevel inverter. The voltage across each capacitor must be maintained at $\frac{1}{2}V_{dc}$, therefore the maximum voltage stress on any switching device is limited to one capacitor voltage [2.24, 25, 30]. The inverter in Figure 0.6 provides a three-level output between ‘a’ and ‘0’ as listed in Table 2.4, which summarizes the switch states and corresponding inverter output voltages, in addition to the current paths. In this topology, the switch states that produce

the same phase voltage level are referred to as redundant switch states. This topology has several disadvantages which restrict its use. Converter initialization is a problem where the clamping capacitors of the flying capacitor multilevel inverter must be fully pre-charged before being modulated. This complicates the modulation process and hinders converter performance under ride-through conditions. Another problem concerns clamping capacitor ratings. Since these are rated at a large percentage of dc-bus voltage, these dc capacitor voltage ratings must be large compared to those of the diode-clamped inverter. Due to these limitations, there has been limited development of this topology, and it is not deemed suitable for PV applications [2.13]. Moreover, both the diode and flying capacitor clamped inverters exacerbate the problem of partial shading as they require a large number of series connected PV cells in order to build-up a relatively high dc voltage appropriate for medium-voltage applications [2.25, 31].

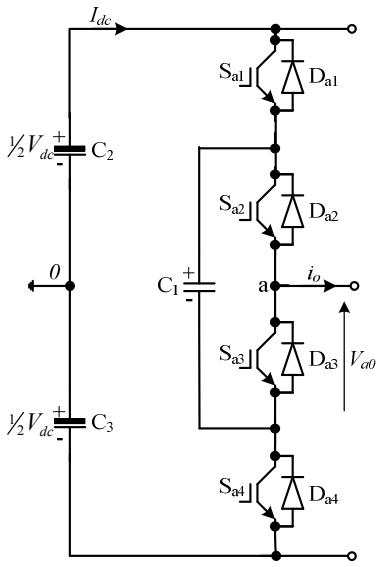

Figure 0.6: One phase of three-level flying capacitor (also known as capacitor clamped) inverter.

Table 0.4: Summary of the switch state combinations and their corresponding output voltages.

Output voltage level V_{a0}	Switch states				Current polarity	Current path
	S_{a1}	S_{a2}	S_{a3}	S_{a4}		
$+½V_{dc}$	ON	ON	OFF	OFF	$i_a>0$	S_{a1},S_{a2}
					$i_a<0$	D_{a1},D_{a2}
0	ON	OFF	ON	OFF	$i_a>0$	S_{a1},C_1,D_{a3}
					$i_a<0$	S_{a3},C_1,D_{a1}
	OFF	ON	OFF	ON	$i_a>0$	D_{a4},C_1,S_{a2}
					$i_a<0$	S_{a4},C_1,D_{a2}
$-½V_{dc}$	OFF	OFF	ON	ON	$i_a>0$	D_{a3},D_{a4}
					$i_a<0$	S_{a3},S_{a4}

2.4.3. Cascaded multilevel inverter

The cascaded multilevel inverter has received attention due to its simplicity and power stage modularity, which makes it scalable to medium voltage applications [2.32]. The cascaded multilevel inverter exploits series connection of single-phase H-bridge inverters with separate dc sources to build-up high output voltage using low voltage rated switching devices. Figure 0.7 shows the topology for one phase leg of a nine-level inverter with four cells in each phase [2.24, 33]. Exploiting bipolar voltage generation ability of each single-phase H-bridge cell, different voltage levels in the phase output voltage of the cascaded multilevel inverter are synthesized using the available switch combinations provided by the H-bridge cells. Each single-phase H-bridge inverter generates three voltage levels at its output: $\pm V_{dc}$ and 0, as stated in section 0. Thus, for example, a cascaded multilevel inverter with four cells per phase leg can generate a maximum of nine voltage levels that vary between $\pm 4V_{dc}$ and 0. This allows the production of a good sine-wave pre-filtered output voltage with staircase or pulse width modulation.

The cascaded inverter topology is attractive in PV applications because of its relative low voltage isolated dc sources, which can be replaced by PV arrays. These dc sources need not be of the same magnitude, and such a low voltage requirement of the H-bridge cells can be provided by fewer PV cells in series, hence the problem of partial shading is avoided. Since a PV array can be considered as an active dc source, capacitor voltage balancing is no longer required. Capacitive PV array currents to ground will be

problematic because the various arrays are not grounded and experience small progressive *dv/dt* steps.

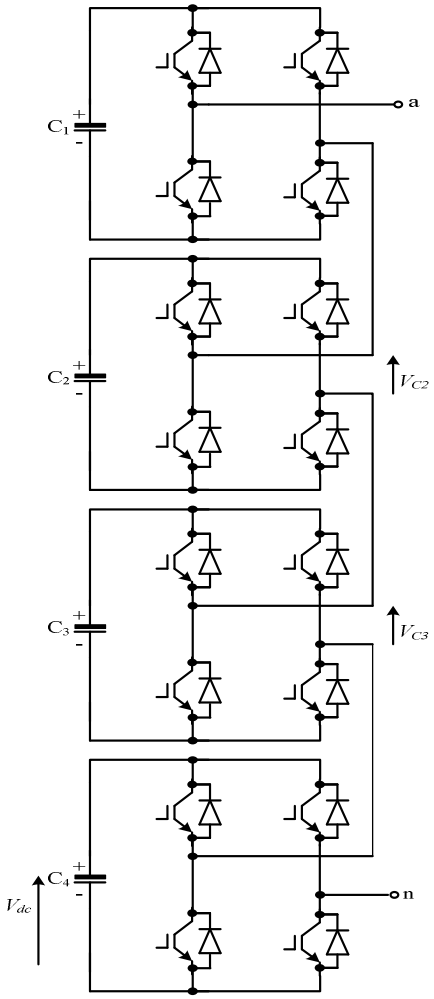

Figure 0.7: Power circuit of one phase leg of nine-level cascaded multilevel inverter.

2.4.4. Modular multilevel

Figure 0.8 shows one-phase of a three-level modular inverter which is composed of two groups of switches: the main switches areS_{a1}, S_{a2}, S_{a3} and S_{a4} and the auxiliary switches are S_{x1}, S_{x2}, S_{x3} and S_{x4}. There are four complementary switch pairs per phase (S_{a1}, S_{x1}), (S_{a2}, S_{x2}), (S_{a3}, S_{x3}) and (S_{a4}, S_{x4}) such that $S_{ai}+S_{xi}=1$ where i=1 to 4. Each capacitor in the circuit is maintained at $½V_{dc}$ and the voltage stress on each switching device is limited to one capacitor voltage [2.30, 34]. With reference to the supply midpoint 0 as in Figure 0.8, the three-level waveform between output phase ‘a’ and 0 can be synthesized as follows:

- For V_{a0}=½V_{dc}, the upper main switches ($S_{a1}$and S_{a2}) and lower auxiliary switches (S_{x3} and S_{x4}) are all turned on.
- For V_{a0}=0, there are four different switch combinations:
  i. S_{a1}, S_{a3}, S_{x2} and S_{x4} are turned on.
  ii. S_{a2}, S_{a3}, S_{x1} and S_{x4} are turned on.
  iii. S_{a2}, S_{a4}, S_{x1} and S_{x3} are turned on.
  iv. S_{a1}, S_{a4}, S_{x2} and S_{x3} are turned on.
- For V_{a0}=-½V_{dc}, the upper auxiliary switches (S_{x1} and S_{x2}) and lower main switches (S_{a3} and S_{a4}) are all turned on.

Table 0.5 summarizes the voltage levels and their corresponding switch states [2.26].
In the modular multilevel inverter, high frequency carrier based PWM is favoured over space vector modulation because it reduces the capacitor voltage balancing method complexity, and improves the capacitor voltage balancing method's robustness to different operating conditions, including unbalanced operating conditions and asymmetrical faults.

In a two-stage grid connected PV system, a modular multilevel inverter regulates the boost converter output voltage to be fixed and regulates the injected current into the grid to achieve unity power factor operation [2.34]. The modular multilevel inverter alleviates the disadvantages of conventional multilevel inverters such as the difficulty of capacitor voltage balancing with higher order levels, the need for ac output filtering and an interfacing transformer. Another advantage of the modular multilevel inverter is that it requires only one dc source and is able to synthesize intermediate voltage levels using its cell capacitors. Furthermore, it utilizes phase redundancy to balance the dc link capacitors regardless of number of levels, independent of power factor and modulation index. Also, it provides capability for fault management and fault ride-through [2.25, 27].

In order to realise these advantages, however, modular multilevel converters require a large number of active and passive components, and a robust capacitor voltage balancing strategy to control the voltage stress across each switching device. These requirements increase both the circuit and control complexity.

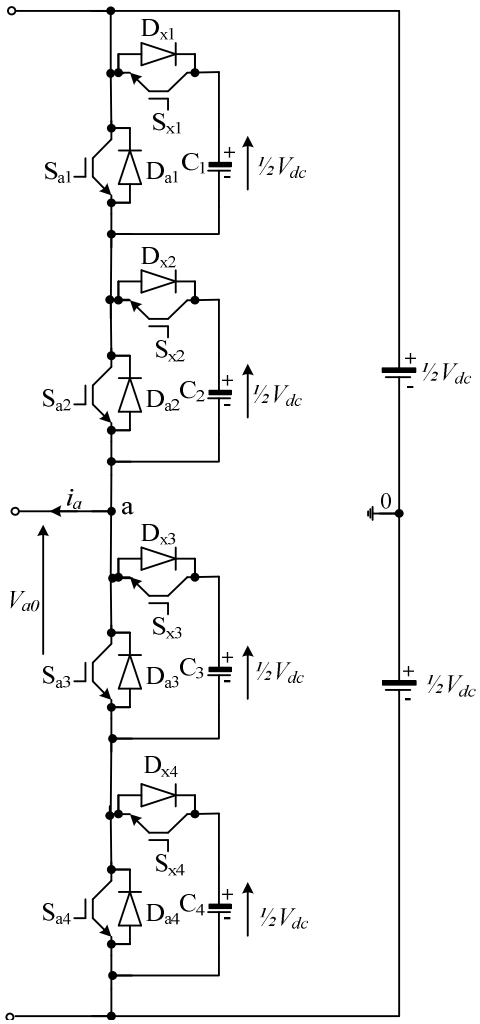

Figure 0.8: Power circuit of one phase leg of three-level modular inverter.

Table 0.5: Switch combinations for a three-level modular inverter.

Output voltage V_{a0}	Switch states								
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
$½V_{dc}$	ON	ON	OFF	OFF	OFF	OFF	ON	ON	
0	ON	OFF	ON	OFF	OFF	ON	OFF	ON	(i)
	OFF	ON	ON	OFF	ON	OFF	OFF	ON	(ii)
	OFF	ON	OFF	ON	ON	OFF	ON	OFF	(iii)
	ON	OFF	OFF	ON	OFF	ON	ON	OFF	(iv)
$-½V_{dc}$	OFF	OFF	ON	ON	ON	ON	OFF	OFF	

2.5. Summary

This chapter presented single-stage and two-stage converter arrangements as possible integration options for a grid-connected photovoltaic system. In both arrangements, the dc-to-ac inverter configurations, including single-phase, three-phase and multilevel, are discussed, and suitability and practicality of each topology for PV applications are highlighted. For simplicity and other features previously highlighted, the three-phase two-level VSI is selected as a suitable interfacing option to be used for the grid integration of the PV system in this thesis, which will be further discussed in subsequent chapters.

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Chapter Three

Modulation Techniques for the Voltage Source Inverter

3.0. Introduction

This chapter discusses a number of pulse width modulation (PWM) techniques used to generate gating signals for a three-phase two-level voltage source inverter (VSI). These modulation techniques, namely carrier-based sinusoidal pulse width modulation, third harmonic injection pulse width modulation, space vector modulation and selective harmonic elimination, are addressed and assessed in this chapter, and the features of each modulation technique are presented. A new implementation of the selective harmonic elimination (SHE) technique that exploits the 3^{rd} harmonic to improve performance at low and high modulation indices, is presented, and validated by simulation and experimentation.

3.1. Background

In principle, all two-level three-phase inverter modulation techniques create a train of pulses that have the same fundamental voltage as a target reference voltage. However, these pulse trains contain unwanted harmonic components which should be minimised. The duty cycles for the pulses must be calculated, and the best way to place these pulses within each switching cycle must be determined, taking into consideration minimisation of unwanted harmonics and other objectives such as low switching loss. A number of PWM techniques may be used to generate gating signals for the two-level three-phase VSI. In the literature, the most commonly discussed PWM techniques used to control a three-phase two-level VSI are carrier-based sinusoidal pulse width modulation (SPWM) [3.1-5], third harmonic injection pulse width modulation (THIPWM) [3.1, 6,7], space vector modulation (SVM) [3.7-12] and selective harmonic elimination (SHE) [3.13-23]. Since SHE is known for better harmonic performance than SVM and THIPWM but

poorer dc voltage utilization, like SPWM, this thesis proposes an improved SHE implementation with adjustment of third harmonic injection to preserve the advantage of standard SHE but with improved dc link utilization. The initial objective of third harmonic adjustment is to extend the maximum modulation index as the switching angle increases. The adjustment of the 3rd harmonic in SHE does not result in decoupling of the modulation index from the number of switching angles, however, it remains useful at high modulation indices where standard SHE tends to produce closely located switching angles (which cannot be realised practically). Thus, the proposed SHE results in wider separation of switching angles for the same modulation index as standard SHE, which leads to more viable practical realisation.

3.2. Carrier-based Sinusoidal Pulse Width Modulation

A circuit diagram of a three-phase two-level VSI that comprises six active switches, S_1 to S_6 with a free-wheeling diode in parallel with each switch, is shown in Figure 0.1.

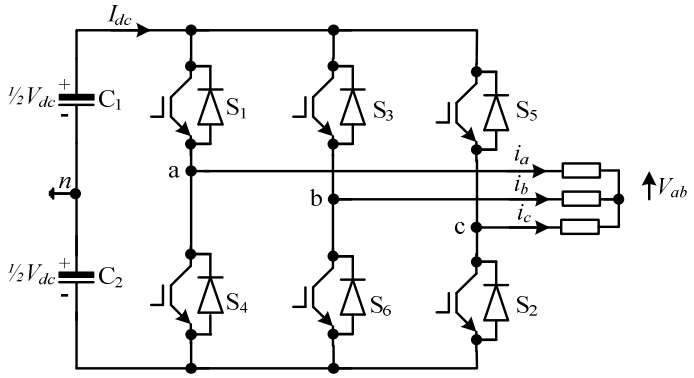


Figure 0.1: Topology of three phase two-level voltage source inverter.

Carrier-based sinusoidal pulse width modulation (SPWM) refers to the generation of PWM gating signals by comparing sinusoidal modulating signals (v_{ma}, v_{mb} and v_{mc}) to a high frequency carriers (v_{cr}) to generate the on and off periods of the PWM output signals, as shown in Figure 0.2(a) [3.24].

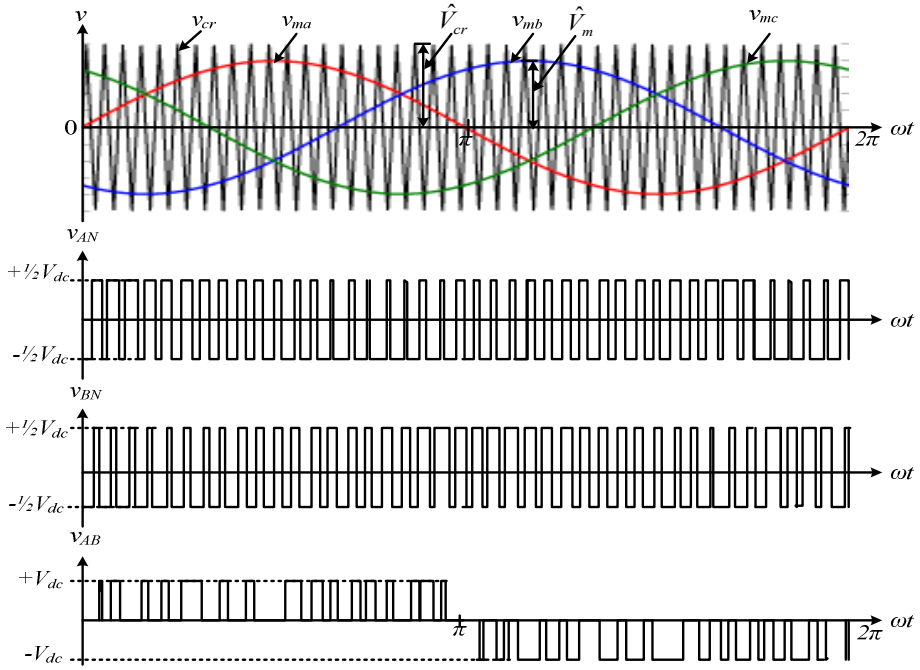
The fundamental-frequency component in the inverter output voltage can be determined by the amplitude modulation index, m_a

$$m_a = \frac{\hat{V}_m}{\hat{V}_{cr}} \tag{3.1}$$

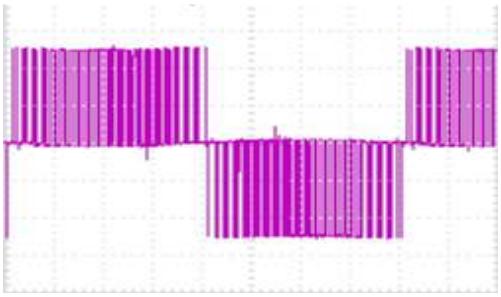
where $\hat{V}_m$ and $\hat{V}_{cr}$ are the peak values of the modulating and carrier signals respectively. The amplitude modulation index m_a is adjusted by varying $\hat{V}_m$ while $\hat{V}_{cr}$ is fixed. The frequency modulation index is defined by

$$m_f = \frac{f_{cr}}{f_m} \tag{3.2}$$

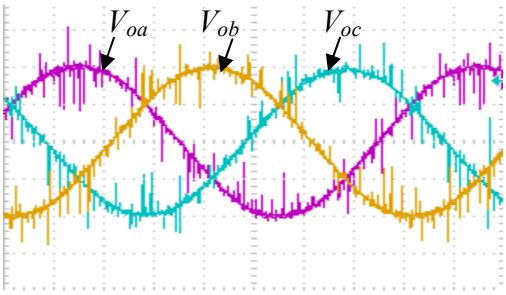
where f_m and f_{cr} are the frequencies of the modulating and carrier signals respectively. For instance, when $v_{ma} \geq v_{cr}$, the upper switch S_1 in leg '*a*' is turned on while the complimentary switch S_4 in the same leg is turned off, leading to the inverter voltage v_{AN} being equal to $+½V_{dc}$. When $v_{ma} \leq v_{cr}$, S_4 is on and S_1 is off leading to v_{AN} equalling to $-½V_{dc}$, as shown in Figure 0.2(a). These voltage signals (v_{AN} and v_{BN}) are defined with respect to the midpoint of the dc bus. The inverter line-to-line voltage, v_{AB} is determined by $v_{AB} = v_{AN} - v_{BN}$. The peak amplitude of the modulating signals, V_m, determines the amplitude modulation index m_a and in turn controls the rms value of the output line-to-line voltage, v_{AB}. The inverter switching frequency, f_{sw} is determined by the carrier frequency, f_{cr}. Figure 0.2(b) to (d) illustrates the experimental waveforms of the two-level three phase VSI line-to-line voltage, v_{AB}, load voltage, and current respectively. The main advantage of SPWM is its simple implementation, but it is unable to fully utilize the dc link voltage, therefore does not maximise the power density [3.25, 26].



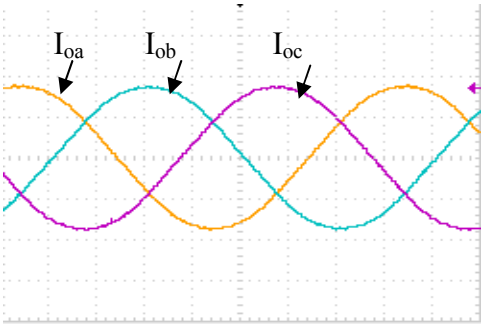
(a) SPWM for three-phase voltage source inverter



(b) Experimental line-to-line output voltage, v_{AB} waveform



(c) Sample of three phase load voltage



(d) Sample of three phase load current

Figure 0.2: Modulation of the three phase VSI using SPWM and sample of open-loop experimental waveforms (V_{dc}=100V, m_a=0.8 and f_{sw}=2000Hz).

3.3. Third Harmonic Injection Pulse Width Modulation (THIPWM)

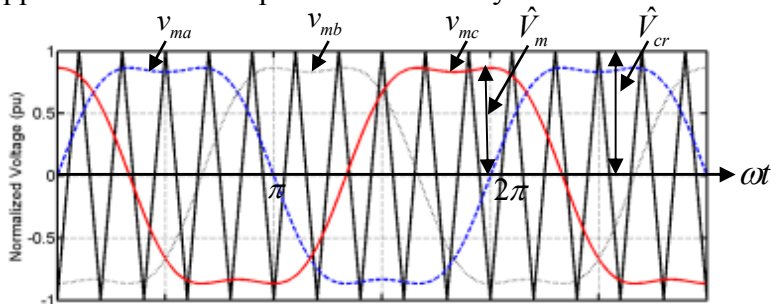
The modulating signal of THIPWM is generated by injecting selected harmonics into the reference signal of each leg. This technique provides a 15.5% higher fundamental amplitude than SPWM, which enables full utilisation of dc-link voltage. The modulating signal, v_{mx} is defined as [3.24]:

$$v_{mx} = m_a\left(\sin\left(\omega t + \phi\right) + \tfrac{1}{6}\sin 3\omega t\right) \tag{3.3}$$

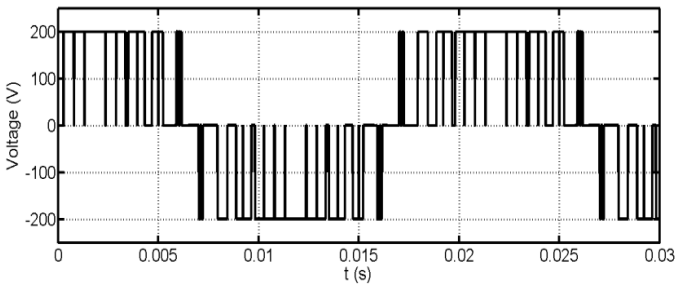
where m_a is the amplitude modulation index, $\phi = 0, \frac{2\pi}{3}, \frac{4\pi}{3}$, and $x = a$, b or c.

Figure 0.3(a) shows the modulating signals (v_{ma}, v_{mb} and v_{mc}) composed of the fundamental and third harmonic components, and highlights the flattened top of the modulating signals. As a result, the peak fundamental signal, V_m can be higher than the peak of the carrier signal, V_{cr} which boosts the fundamental line-to-line voltage, v_{AB}. A sample simulation result of the line-to-line voltage waveform v_{AB} with modulation index, m_a=0.8 and switching frequency, f_{sw}=2kHz, is illustrated in Figure 0.3(b).

Third harmonic injection does not affect the quality of the output voltage because the three-phase output does not contain triple harmonics [3.1]. The main advantage of this technique is simplicity in hardware and implementation. However, the disadvantage is that it is only applicable to a three-phase three-wire system.



(a) Modulating signals (v_{ma}, v_{mb} and v_{mc}) with third harmonic injection



(b) Line-to-line voltage, v_{ab} waveform with repsect to midpoint of the dc bus

Figure 0.3: Reference modulating and output voltage waveforms when the VSI is controlled with third harmonic injection PWM.

3.4. Space vector modulation (SVM)

Space vector modulation is based on eight possible switch state combinations for a three-phase VSI. A switch constraint for the VSI is that each leg contains two series switching devices operating in a complementary manner [3.7]. If the upper switch is turned on, the corresponding lower switch is off, and vice versa. The 'on' switch is represented by 1 and the 'off' switch is represented by 0, as stated in Table 0.1. The switched output voltage can be determined by the states of three upper switches S_1, S_3 and S_5 of phase '*a*', '*b*' and '*c*' respectively, as in Figure 0.1. The resultant output phase and line-to-line voltages are produced with respect to the corresponding 'on' and 'off' states of the three upper switches.

Table 0.1: Eight possible switch state combinations of a three-phase VSI.

S_1	S_3	S_5	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
0	0	0	0	0	0	0	0	0
1	0	0	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	V_{dc}	0	$-V_{dc}$
1	1	0	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	0	V_{dc}	$-V_{dc}$
0	1	0	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$-V_{dc}$	V_{dc}	0
0	1	1	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	$-V_{dc}$	0	V_{dc}
0	0	1	$-\frac{1}{3}V_{dc}$	$-\frac{1}{3}V_{dc}$	$\frac{2}{3}V_{dc}$	0	$-V_{dc}$	V_{dc}
1	0	1	$\frac{1}{3}V_{dc}$	$-\frac{2}{3}V_{dc}$	$\frac{1}{3}V_{dc}$	V_{dc}	$-V_{dc}$	0
1	1	1	V_{dc}	V_{dc}	V_{dc}	0	0	0

The relationship between the leg voltage, phase voltage and line-to-line voltage in a two-level three-phase VSI can be expressed as:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \text{ and } \begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \qquad (3.4)$$

The eight switch state combinations in Table 0.1can be represented in the stationary reference frame α-β by transforming the phase voltages from phase variables *a*, *b* and *c* to α and β using:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \tag{3.5}$$

where $V_{ref} = \sqrt{V_\alpha^2 + V_\beta^2}$ and $\theta = \tan^{-1} V_\beta / V_\alpha$

Based on this concept, the space vector diagram for a two-level inverter is shown in Figure 0.4. There are six stationery active vectors, namely $\overline{V}_1$ to $\overline{V}_6$, zero vector $\overline{V}_0$ and the reference vector, $\overline{V}_{ref}$ that rotate in space at an angular velocity of the fundamental frequency of the inverter voltage [3.26].

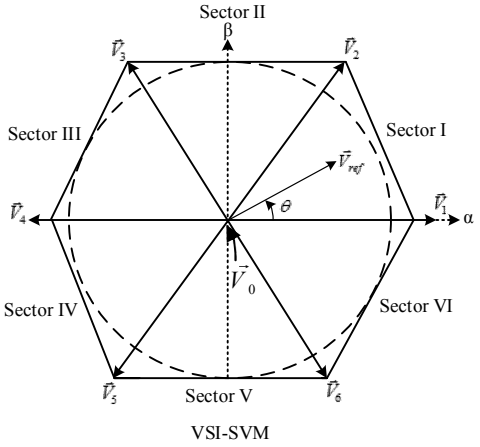


Figure 0.4: Space vector diagram for a two-level inverter.

The dwell times for the stationery vectors represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s for all six sectors that can be calculated as follows:

$$\begin{aligned} T_1 &= m_a T_s \sin\left(\frac{n\pi}{3} - \theta\right) \\ T_2 &= m_a T_s \sin\left(\theta - \frac{(n-1)\pi}{3}\right) \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{3.6}$$

where $m_a = {}^{2}\!/_{\sqrt{3}} \dfrac{V_{ref}}{V_{dc}}$ is amplitude modulation index and n is the sector number.

There are many switching sequences proposed for three-phase two-level VSI. Most are aimed at minimizing switching losses by reducing the number of commutations per switching cycle and use the redundant zero vectors in every sequence. Space vector modulation has the ability to transfer harmonic energy into the outer sideband harmonics and, to some extent, to the sidebands of the second carrier group [3.24]. It also offers flexibility in terms of pulse placement in any of the dedicated sectors and switching sequences. Furthermore, SVM increases dc link voltage by 15.5% and semiconductor utilization, improving the power density compared to sinusoidal PWM. It is not best suited for operating in medium-voltage distributed generation systems where the possibility of unbalanced operation and ac faults are high[3.27]. Digital implementation of these modulation strategies with grid connected PV inverters necessitates the use of relatively high switching frequencies for control purposes (the control period is equal to the reciprocal of switching frequency). Figure 0.5shows a simulation result of the line-to-line voltage, v_{AB} waveform with modulation index, m_a=0.8 and switching frequency, f_{sw}=2kHz.

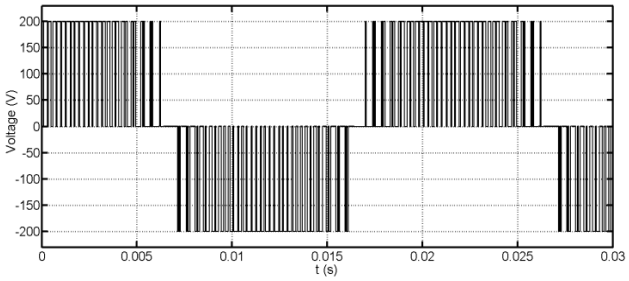


Figure 0.5: Line-to-line voltage, v_{AB} waveform relative to midpoint of the dc bus when the VSI is controlled by SVM.

3.5. Selective harmonic elimination

The selective harmonic elimination (SHE) technique, based on the idea of Fourier decomposition, is used to eliminate specific lower order harmonics in a switching waveform. SHE is considered useful for low baseband distortion in inverters with a low switching-to-fundamental frequency ratio[3.20].

The Fourier series expansion of the SHE-PWM waveform is given by:

$$V(\omega t) = \sum_{n=1}^{\infty} \left(a_n \cos\left(n\omega t\right) + b_n \sin\left(n\omega t\right) \right) \tag{3.7}$$

Owing to the PWM waveform characteristics of odd functions and quarter-wave symmetry, $a_n = 0$, for all *n*, and the output voltage reduces to:

$$V(\omega t) = \sum_{n=1}^{\infty} b_n \sin\left(n\omega t\right) \tag{3.8}$$

where ω is the radian frequency of the output voltage [3.16, 19].

There are two SHE solutions proposed based on the trajectories of chopping or switching angles over a ½π period. The switching angles for solution 1 are located between 0 and 60^o while for solution 2, the angles are located between 0 and 90^o. A generalized expression of b_n for any number of switching angles for both solutions is given by:

$b_n = \frac{2V_{dc}}{n\pi}\left[2\sum_{k=1}^{N} (-1)^{k-1} \cos n\alpha_k - 1 \right]$, in the case of the first arrangement that produces solution 1, and

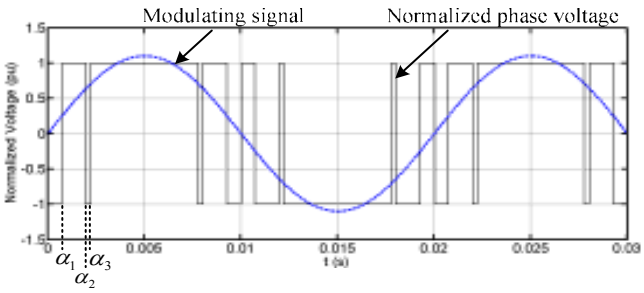
$b_n = \frac{2V_{dc}}{n\pi}\left[2\sum_{k=1}^{N} (-1)^{k} \cos n\alpha_k + 1 \right]$ in case of the second arrangement that produces solution 2, for odd values of *n*[3.20, 22, 23].

Figure 0.6(a) and (b) show the normalized(by ½V_{dc}) output voltage of two-level VSI relative to the supply mid-point, when SHE is used to control the inverter, with three notches (α_1, α_2 and α_3) for fundamental voltage adjustment and elimination of the 5th and 7th harmonics respectively. As previously mentioned, all switching angles for solution 1 in Figure 0.6(a) are located between 0 and 60^o as shown in Figure 0.6(c) (solid line). The maximum attainable modulation index for solution 1 is 1.1884. This maximum modulation index is achieved by solving an optimization problem that maximizes the modulation index. The solution uses equations for the elimination of the 5th and 7thharmonics as nonlinear constraints, and $\alpha_1 < \alpha_2$, $\alpha_2 < \alpha_3$ and $\alpha_3 \leq ½\pi$ as linear

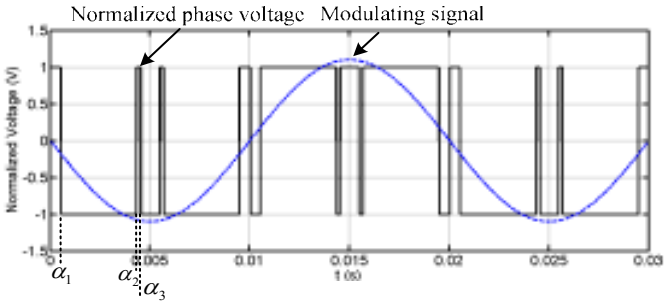
inequalities that maintain output voltage quarter wave symmetry [3.14-16]. The waveform of the line-to-line voltage v_{AB}, using solution 1, is shown in Figure 0.6(d).

Solution 2 (dotted line) in Figure 0.6(c) produces switching angles distributed over 90^o, with $\alpha_2 < \alpha_3$ located between 60^o and 90^o. The maximum modulation index with solution 2 is 1.16, which is lower than the modulation index produced by solution 1.

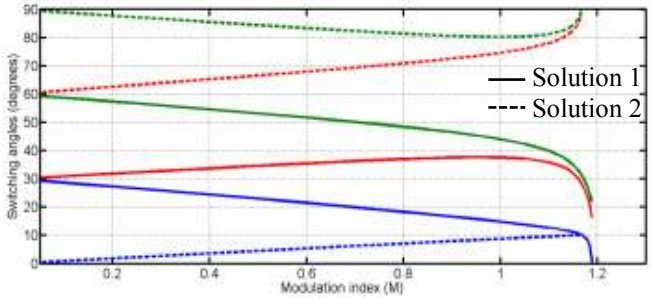
Additionally, it can be observed that solution 2 produces a fundamental voltage 180^o out of phase with that produced by solution 1, for the same fundamental voltage. This can be observed in Figure 0.6(b) as during most of the first half cycle, the inverter output phase is connected to the negative bus. This observation may be critical for SHE implementation in grid connected applications. The arrangement for solution 2 always produces a smaller modulation index and hence the fundamental voltage. Therefore, the choice between the arrangements may require careful attention to the fundamental voltage polarity.



(a) Waveforms illustrate phase voltage relative to supply mid-point when the 5th and 7th harmonics are eliminated and the modulation index is m_a=1.1 (solution 1)

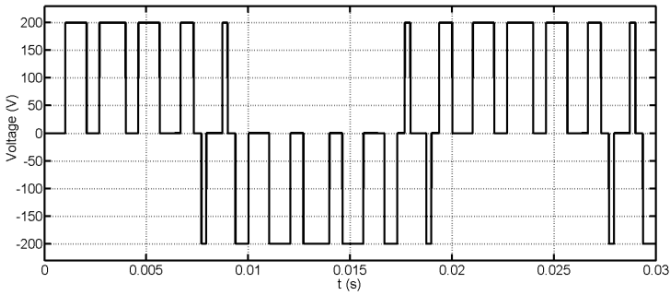


(b) Waveforms illustrate phase voltage relative to supply mid-point when the 5th and 7th harmonics are eliminated and the modulation index is m_a=1.1 (solution 2)



(c) Switching angle trajectories for solutions 1 and 2

(solid lines represent switching angles for solution 1 and dashed line for solution 2)



(d) Line-to-line voltage, v_{AB} waveform

Figure 0.6: SHE implementation using solution 1 and 2 when 5th and 7th harmonic components are eliminated.

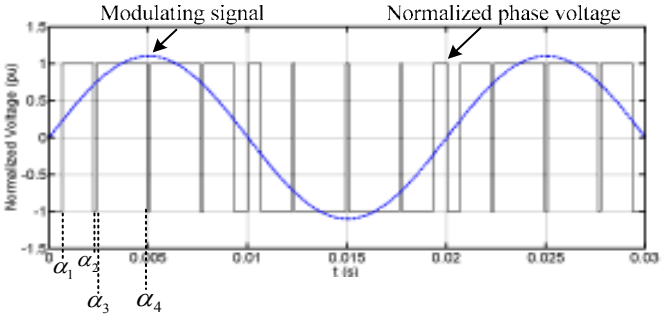
3.5.1. Improved selective harmonic elimination

Based on the previous discussion, with the intention of extending the modulation index as the switching angle increases, this thesis investigates adjustment of the third harmonic to decouple the maximum modulation index achievable from a given number of switching angles. When a fourth angle is added for 3rd harmonic adjustment, the maximum modulation index using solution 1 remains at 1.1884 as shown in Figure 0.8(a). This is obtained when the 3rd harmonic voltage magnitude changes from ⅙ to ⅕ of the fundamental voltage. As illustrated in Figure 0.7(a) and (b), control of 3rdharmonic injection results in the spreading of switching angles over one quarter of the fundamental cycle, i.e. 90o.

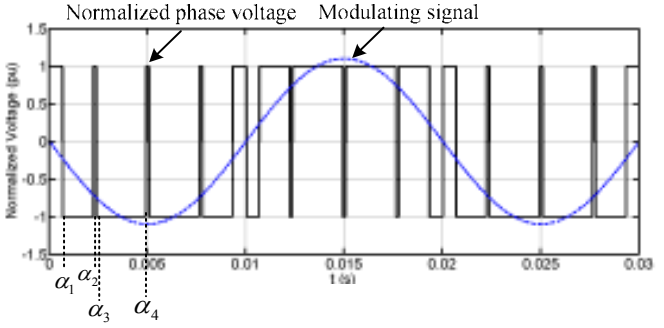
Adjustment of the 3rd harmonic in SHE does not result in decoupling of the modulation index from the number of switching angles, however it remains useful at high modulation indices where standard SHE tends to produce switching angles in a narrow range close to zero (which cannot be realized practically). Injection of the 3rd harmonic into arrangements 1 and 2 forces their switching angles to converge, for the same modulation index, thus practical realisation is now possible(see Figure 0.8(b))[3.27].

For further confirmation of the potential usefulness of 3rd harmonic adjustment, the case with five notches where the 5th, 7th, and 11th harmonics are eliminated, is presented in Figure 0.9(a). With adjustment of the 3rd harmonic, arrangements 1 and 2 produce one unique solution that satisfies quarter wave symmetry in the low modulation index range, $m_a<0.6$. Above this modulation index, the switching angles produced by solving the equations for arrangement 1 diverge from those produced by arrangement 2 (see Figure 0.9(a)). When the 5th,7th, 11th, and 13th harmonics are eliminated, the switching angles associated with the 7th, 11th and 13th remain the same for both solutions over the entire modulation index range, while those associated with 1st, 3rd and 5th diverge as modulation index increases, see Figure 0.9(b). The addition of the 3rd harmonic equation to the set of nonlinear transcendental equations contributes to simplification of the solution process as it is straightforward to find one set of initial guesses that can be used to produce the solutions for the entire modulation index linear range. A switching angle must be designated to control the third harmonic magnitude.

The modulation indices for the fundamental and 3rd harmonic voltages are defined as: $m_a = \frac{b_1}{\frac{1}{2}V_{dc}} = \frac{V_1}{\frac{1}{2}V_{dc}}$ and $m_3 = \frac{b_3}{\frac{1}{2}V_{dc}} = \frac{V_3}{\frac{1}{2}V_{dc}} = \frac{\gamma V_1}{\frac{1}{2}V_{dc}}$, where γ is a positive fraction used to describe the 3rd harmonic voltage component in terms of the fundamental.

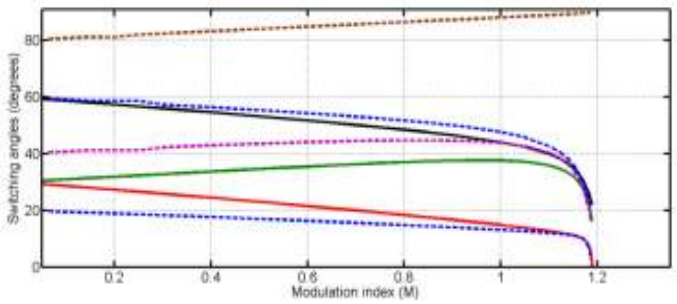


(a) Solution 1(0 to 60°)

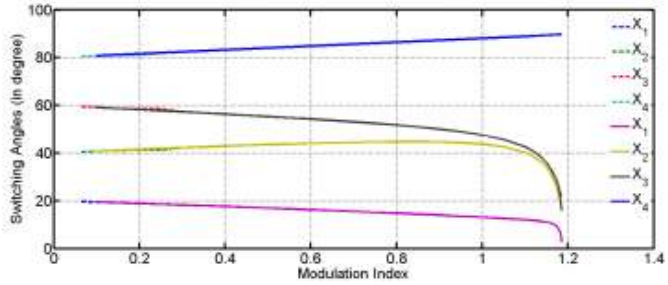


(b) Solution 2 (0 to 90°)

Figure 0.7: Waveform illustrate phase voltage relative to supply mid-point when the 5th and 7th harmonic are eliminated, m_a=1.1 and 3rd harmonic is m_3=m/5 for both SHE solutions.

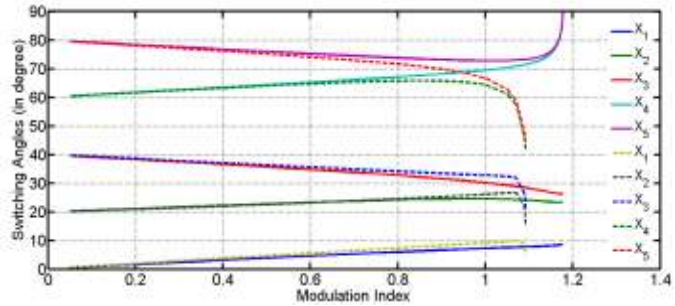


(a) The dotted and solid lines represent solution 1 with and without the addition of 3rd harmonic component respectively. The maximum attainable modulation index is 1.1884.

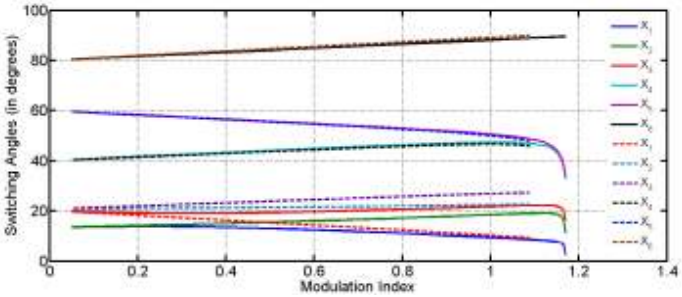


(b) The dashed and solid lines represent solutions 1 and 2 with the addition of 3rd harmonic component, maximum attainable modulation index for both solutions is 1.185.

Figure 0.8: Switching angle trajectories for solution 1 and 2 when 5th and 7th harmonics are eliminated.



(a) Maximum attainable modulation index for solutions 1 and 2 when 5th , 7th and 11th harmonics are eliminatedare 1.1773 and 1.092 respectively.

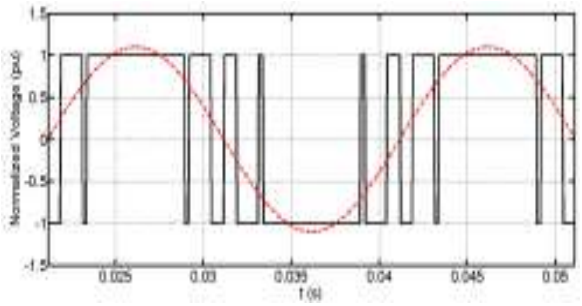


(b) Maximum attainable modulation index for solutions 1 and 2 when5th , 7th , 11th, and 13th harmonics are eliminatedare 1.170 and 1.088 respectively.

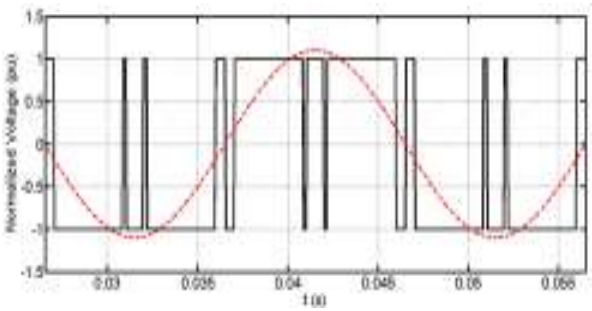
Figure 0.9: Switching angle trajectories for solution 1 and 2 with control of the 3rd harmonic component. Solid and dashed lines represent solution 1 and 2 respectively.

A. Open-loop validation of the proposed SHE

Figure 0.10 and 3.11 displays the two-level inverter output voltage and phase voltage waveforms obtained with SHE for solutions 1 and 2, with and without 3rd harmonic injection, using the DSP-hardware platform dSPACE1006. For simplicity of illustration, only two harmonics are eliminated (5th and 7th), with a modulation index m_a=1.1. Figure 0.10(b) shows that solution 2 fundamental voltage is 180° out of phase compared to solution 1 (see Figure 0.10(a)), for the same modulation index. This occurs because the switching angles for solution 2 are located in positions that result in the inverter output phase being connected to the negative bus during most of the first fundamental half cycle. Figure 0.11(a) to (b) display the output voltage waveforms for solutions 1 and 2 with adjustment of the 3rd harmonic ($m_3 = \frac{1}{5}m$). The switching instants in both waveforms are approximately identical, but the fundamental voltage produce by solution 2 remains 180° out of phase as compared to solution 1. The adjustment of the 3rd harmonic leads to a unique universal solution (switching angles) that can be used with both arrangements to achieve the desired fundamental voltage and eliminate the 5th and 7th, with both satisfying the quarterwave symmetry constraint.

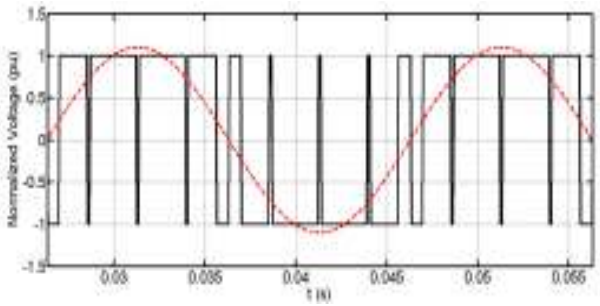


(a) Phase output voltage relative to supply mid-point (solution 1)

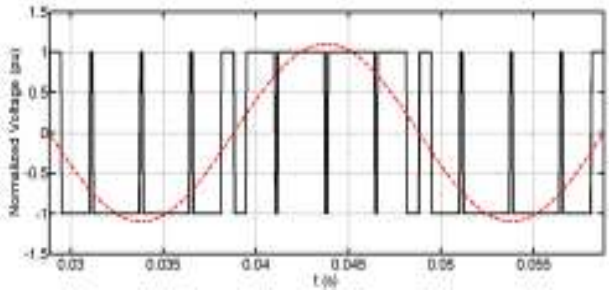


(b) Phase output voltage relative to dc supply mid-point (solution 2)

Figure 0.10: Experimental waveforms illustrating two-level inverter output voltage normalized by ½V_{dc} for solutions 1 and 2, when the 5th and 7th harmonics are eliminated without the adjustment of 3rd harmonic component.



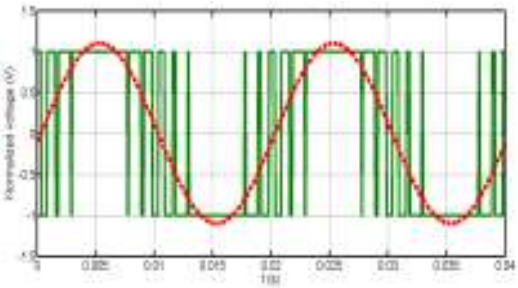
(a) Phase output voltage relative to supply mid-point (solution 1)



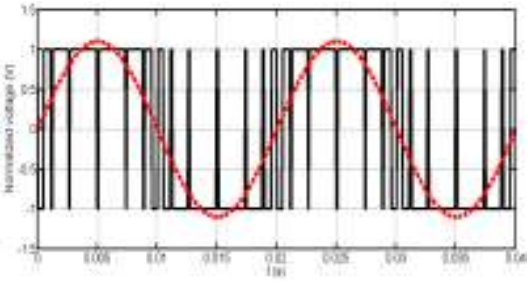
(b) Phase output voltage relative to dc supply mid-point (solution 2)

Figure 0.11: Experimental waveforms illustrating two-level inverter output voltage normalized by $½V_{dc}$ for solutions 1 and 2, when the 5th and 7th harmonics are eliminated, and including adjustment of the 3rd harmonic component.

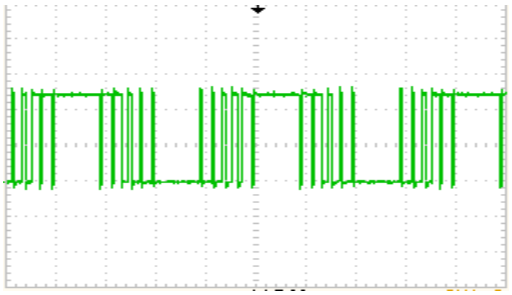
To further illustrate the usefulness of 3rd harmonic adjustment, Figure 0.12 shows the dSPACE1006 experimental results for voltage and current with elimination of the 5th, 7th, 11th and 13th harmonics using solution 1. These results are compared to standard SHE without 3rd harmonic component control. As more switching angles are added for both arrangements (standard and the proposed SHE), the quality of the line-to-line voltage and load current in Figure 0.12(f) and (h) are improved, compared to the waveforms in Figure 0.12(e) and (g) respectively. With a high modulation index of 1.1, the switching angles are increasingly wider using the proposed SHE (see Figure 0.12(b) and (d)), compared to standard SHE, as in Figure 0.12(a) and (c). A practical realisation is now possible without affecting the output quality.



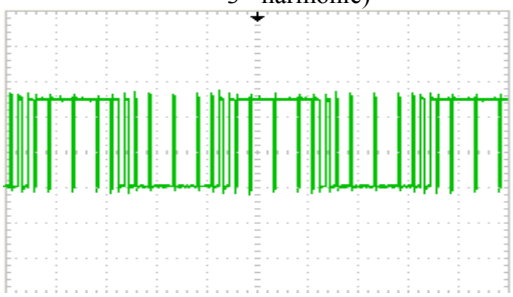
(a) Phase output voltage relative to dc supply mid-point (solution 1)



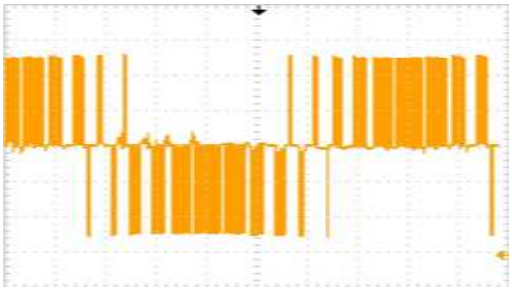
(b) Phase output voltage relative to dc supply mid-point (solution 1 with adjustment of 3rd harmonic)



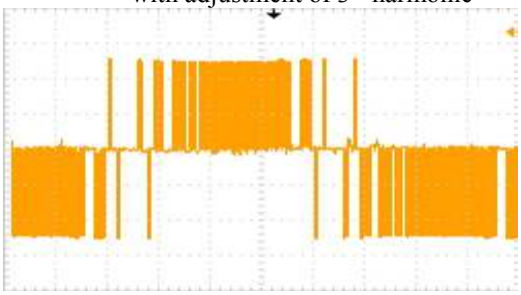
(c) Gating signal of switch S_1using solution 1



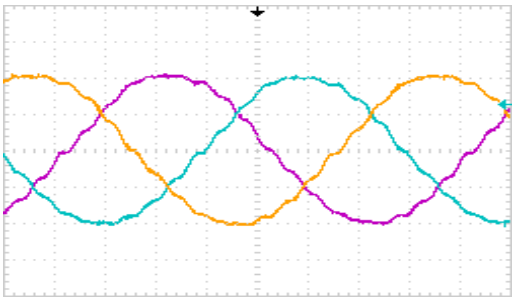
(d) Gating signal of switch S_1using solution 1 with adjustment of 3rd harmonic



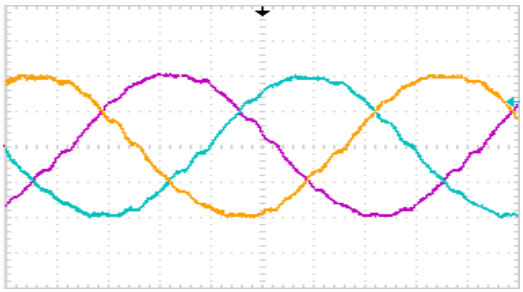
(e) Line-to-line voltage waveform using solution 1



(f) Line-to-line voltage waveform solution 1 with adjustment of 3rd harmonic



(g) Three phase load current using solution 1



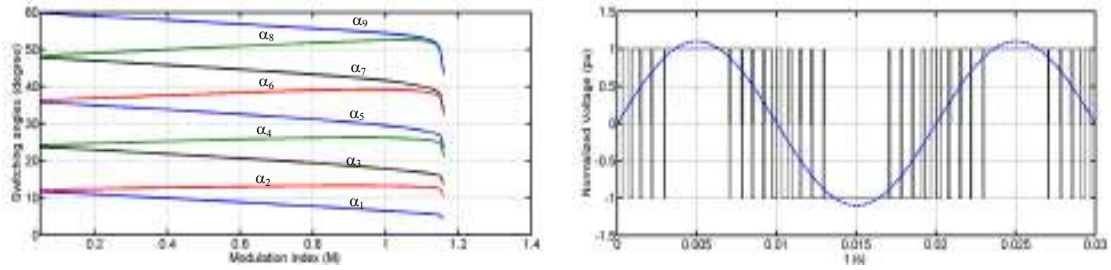
(h) Three phase load current solution 1 with adjustment of 3rd harmonic

Figure 0.12: Experimental voltage and current waveforms for two-level VSI using SHE solution 1, with and without adjustment of the 3rd harmonic component and 5th, 7th, 11th and 13thharmonics eliminated (m_a=1.1).

B. Open-loop validation of SHE with 9 angles

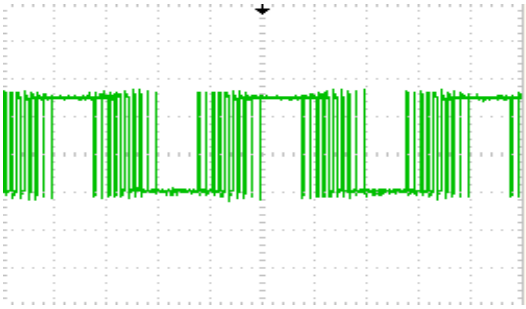
Figure 0.13(a) and (b) illustrate the switching angle trajectories with nine notches per quarter cycle and phase voltage(normalized by $½V_{dc}$) and its fundamental, for modulation m_a=1.1. The experimental waveforms of the voltage across switch S_1, line-to-line voltage v_{AB}, and three-phase load current are presented in Figure 0.14(a) to (c), which further illustrate the suitability of using SHE for a grid connected VSI.

As the switching angle increases, SHE approaches high frequency carrier based PWM and SVM in terms of output voltage quality, but with a reduced number of switching transitions compared to the counterparts. This is significant in multi-megawatt medium-voltage applications as nine notches per quarter cycle is equivalent to a 950Hz switching frequency, with relatively good output voltage and current waveform quality that cannot be achieved with carrier or space vector PWM with a similar switching frequency. The potential benefits of such an approach can be observed in terms of converter efficiency, which may not be significant in low power applications.

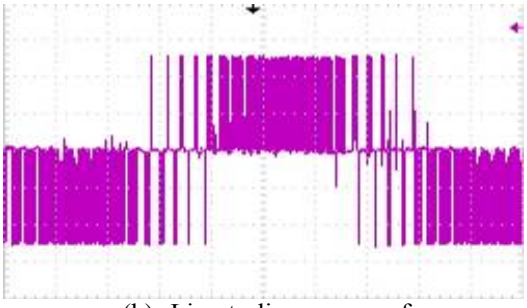


(a) Angles α_1 to α_9 per quarter cycle (b) Normalized PWM voltage waveform

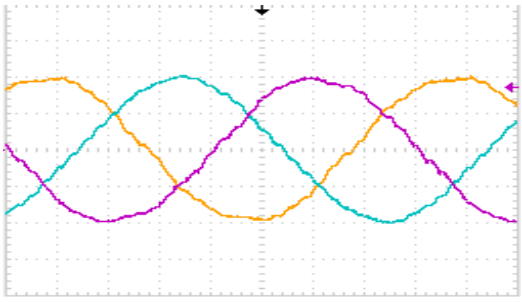
Figure 0.13: (a) Switching angle trajectories with nine notches per quarter fundamental cycle and (b) normalized PWM voltage waveform with reference to midpoint of dc bus.



(a) Voltage across switch S_1 waveform



(b) Line-to-line v_{AB} waveform



(c) Three phase load current

Figure 0.14: Open-loop experiment validation of VSI when SHE is used as the modulator (V_{dc}=100V, m_a=1.1, f_{sw}=950Hz, L_F=3mH and C_F=40μF).

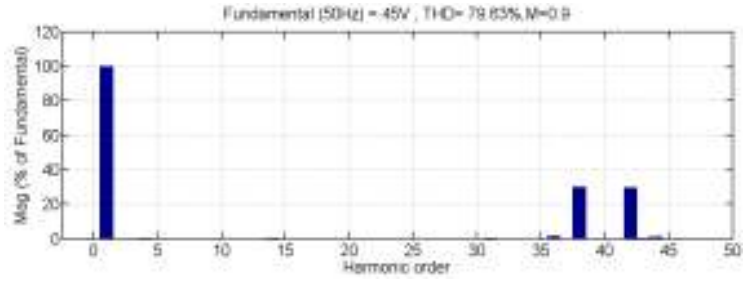
3.6. Assessment of PWM modulation techniques

Figure 0.15 presents the pre-filter voltage spectra for all the modulation techniques discussed in this chapter. All simulation results use f_{sw}=2kHz and a modulation index of 0.9. From these results, SPWM is able to eliminate all harmonics less than or equal to $2n\pm1$, where n is the number of pulses per half cycle of the sine wave. The inverter output voltage harmonics are pushed to the range around the carrier frequency and its odd multiples as shown in Figure 0.15(a). There are no low-order harmonics in the spectra. Both THIPWM and SVM contain similar harmonic distributions, as shown in Figure 0.15(b) and (c). The only exception is that SVM contains even-order harmonics such as the 2nd, 4th, 8th and 10th along with low-order odd-order harmonic contents. These even-order harmonics are not eliminated as they have very low magnitudes in the spectra, as illustrated in Figure 0.15(c). Most of the carrier harmonics and their sidebands in the phase voltage are suppressed around and beyond the second carrier component. Also THIPWM does not present low-order harmonics and the switching frequency component in the spectrum. Figure 0.15(d) shows SHE successfully eliminates the specified harmonics from the baseband (5th, 7th, 11th, 13th, 17th, 19th, 23rd and 25th). Whilst most of the harmonic energy is placed at the 29th and 31st, with the magnitude of

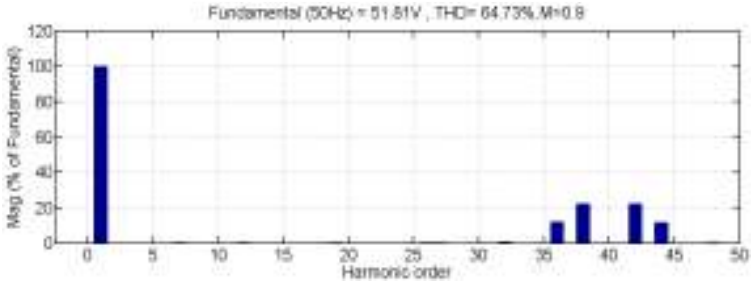
the 29th harmonic being 74% of the fundamental. Although SHE is the best choice in eliminating specific harmonic components, it has the highest percentage THD of all presented modulation techniques. Figure 0.15(e) shows that the adjustment of 3rd harmonic injection in SHE improves the fundamental phase voltage by 15.5%, compared to traditional SHE. This leads to similar dc utilization as with THIPWM and SVM. The low-order harmonics are present in the spectrum since only the 5th, 7th, 11th and 13th harmonics are eliminated, as presented in Figure 0.15(e).

Table 3.2 and 3.3 list the output voltage and current harmonic contents with modulation indices of 0.9 and 0.5 for all the discussed modulation techniques.

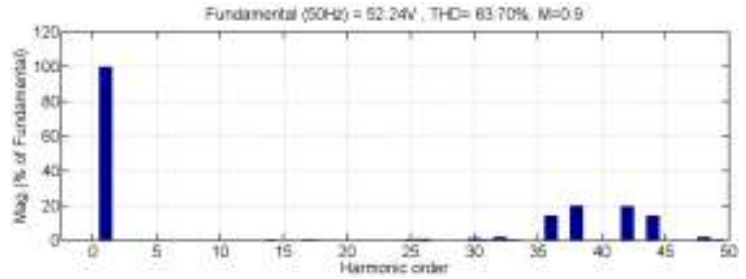
Figure 0.16(a) and (b) present the relationships between modulation index and attainable fundamental phase voltage (pre-filter), and THD for SPWM, THIPWM, SVM, SHE and the improved SHE. The improved SHE is able to almost match SVM and THIPWM over the entire modulation index range, where all three modulation techniques achieve a maximum fundamental phase voltage equal to $0.575V_{dc}$. SPWM and SHE with nine angles, are able to reach a maximum fundamental voltage of only $0.5V_{dc}$, see Figure 0.16(a). The plot of THD versus modulation index in Figure 0.16(b) shows that SVM and THIPWM have the lowest THD, while the proposed SHE almost matches the plot. This is mainly because only four harmonic components are eliminated, therefore the THD is slightly higher for SVM and THIPWM. Standard SHE with nine angles has the highest THD of all the techniques.



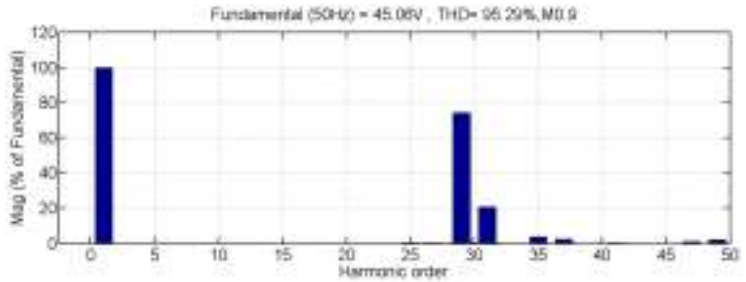
(a) SPWM



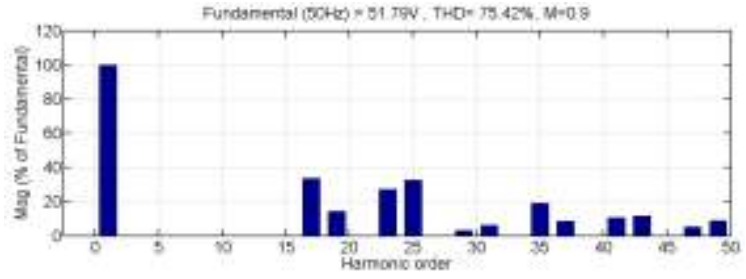
(b) THIPWM



(c) SVM



(d) SHE with 9 angles



(e) SHE with four angles and 3rd harmonic injection

Figure 0.15: Theoretical phase voltage harmonic spectrum of all PWM techniques.

Table 0.2 (a) Harmonic content in voltage for all discussed modulation techniques (m_a=0.9).

		Harmonics (% of fundamental)										
Order of the harmonics		1st	5th	7th	11th	13th	17th	19th	23rd	25th	27th	29th
Voltage	SPWM	100	0.09	0.26	0.12	0.04	0.19	0.11	0.25	0.15	0.18	0.21
	THIPWM	100	0.26	0.37	0.07	0.16	0.14	0.38	0.03	0.33	0.39	0.03
	SVM	100	0.25	0.32	0.22	0.15	0.53	0.14	0.44	0.17	0.39	0.36
	SHE	100	0.25	0.15	0.16	0.28	0.18	0.18	0.06	0.39	0.25	74.42
	Proposed SHE	100	0.31	0.22	0.12	0.28						

(b) Harmonic content in voltage for all discussed modulation techniques (m_a=0.5)

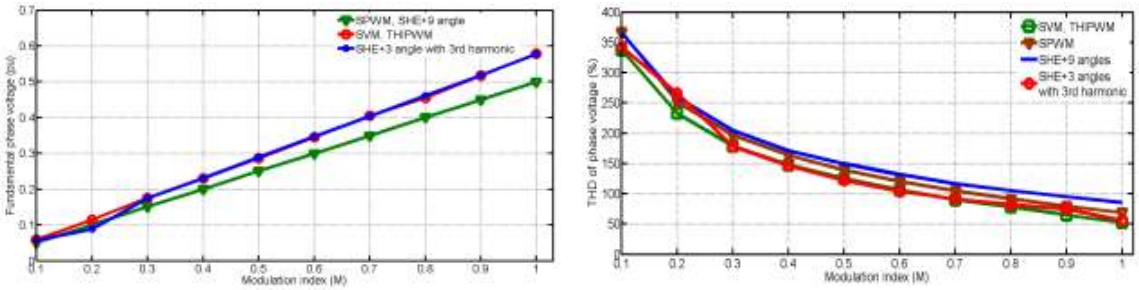
		Harmonics (% of fundamental)										
Order of the harmonics		1st	5th	7th	11th	13th	17th	19th	23rd	25th	27th	29th
Voltage	SPWM	100	0.3	0.5	0.18	0.71	0.32	0.39	0.14	0.34	0.28	0.8
	THIPWM	100	0.09	0.25	0.37	0.77	0.46	0.13	0.9	0.14	0.02	0.41
	SVM	100	0.33	0.23	0.39	0.34	0.28	0.63	0.29	0.44	0.09	1.06
	SHE	100	0.02	0	0.62	0.57	0.09	0.05	1.15	0.8	0.56	111.91
	Proposed SHE	100	0.05	0.41	0.43	0.06						

Table 0.3(a) Harmonic content in current for all discussed modulation techniques (m_a=0.9)

		Harmonics (% of fundamental)										
Order of the harmonics		1st	5th	7th	11th	13th	17th	19th	23rd	25th	27th	29th
Current	SPWM	100	0.05	0.44	0.05	0.01	0.05	0.02	0.05	0.03	0.03	0.03
	THIPWM	100	0.12	0.57	0.03	0.05	0.03	0.08	0.00	0.05	0.06	0.00
	SVM	100	0.12	0.5	0.1	0.05	0.13	0.03	0.08	0.03	0.06	0.05
	SHE	100	0.12	0.24	0.08	0.1	0.04	0.04	0.01	0.06	0.04	10.08
	Proposed SHE	100	0.56	0.19	0.05	0.09						

(b) Harmonic content in current for all discussed modulation techniques (m_a=0.5)

		Harmonics (% of fundamental)										
Order of the harmonics		1st	5th	7th	11th	13th	17th	19th	23rd	25th	27th	29th
Current	SPWM	100	0.14	0.81	0.09	0.25	0.08	0.08	0.02	0.05	0.04	0.11
	THIPWM	100	0.04	0.4	0.17	0.27	0.11	0.03	0.16	0.02	0	0.06
	SVM	100	0.09	0.35	0.09	0.06	0.17	0.18	0.09	0.07	0.04	0.11
	SHE	100	0.01	0.01	0.29	0.2	0.02	0.01	0.2	0.13	0.08	15.16
	Proposed SHE	100	0.08	0.36	0.17	0.05						



(a) (b)

Figure 0.16: Comparison of PWM strategies with varying modulation index for (a) per-unit fundamental pre-filter inverter current and (b) total harmonic distortion (%THD).

Table 0.4: Comparison summary of all presented modulation techniques.

	SPWM	THIPWM	SVM	SHE	Proposed SHE
DC voltage utilization, V_{phase}/V_{dc}	0.5	0.575	0.575	0.5	0.575
Harmonics	Medium	Medium	Worst	Low	Low
Digital implementation	Real-time	Real-time	Real-time	Look-up table	Look-up table

3.7. Summary of major findings

This chapter discussed a number of modulation techniques that can be used to generate a train of pulses that have the same fundamental voltage as the reference voltage for a three phase two-level VSI. Table 0.4 summarises a comparison between these modulation techniques, with reference to several important features, namely dc rail utilization, switching losses, harmonic performance, and digital implementation.

The use of sinusoidal PWM does not fully utilize dc link voltage as stated in Table 0.4, thus lowering the power density and is discarded for future investigation in subsequent chapters. The disadvantage of SPWM however can be reduced by using THIPWM, which enables a 15.5% dc utilization improvement and can be easily implemented in real-time. Similarly, SVM also increase the dc link voltage and semiconductor utilization and improves the power density, compared to sinusoidal PWM, but may have difficulties operating in medium-voltage distribution systems where the possibility of unbalanced operation and ac faults is high. Digital implementation of these modulation strategies with grid connected PV inverters necessitates the use of a relatively high

switching frequencies for control purposes (the control period must be equal to the reciprocal of switching frequency). For medium voltage applications, strict grid codes and the use of a suitable modulation technique are the main priorities, therefore it is sometimes favourable to use traditional modulation approaches such as SHE and carrier based PWM over space vector modulation.

The possibility of using SHE was investigated to control high-power PV inverters in an attempt to suppress switching losses (by adopting switching frequencies of less than 1kHz) and improve the dc link voltage utilization, despite the requirement of an offline look-up table. To achieve these objectives, a new SHE implementation with adjustment of the 3rd harmonic magnitude in the phase voltage was introduced. The control of 3rd harmonic results in spreading of switching angles over the quarter of fundamental cycle. This feature can be used to simplify pratical realization of SHE at high modulation indices when a large number of harmonics are eliminated.

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Chapter Four

Grid Interfacing of Voltage Source Inverter

4.0. Introduction

A low loss multi-megawatt medium-voltage voltage source inverter (VSI) for a grid connected photovoltaic system is presented in this chapter. The suitability of using selective harmonic elimination (SHE) as the modulation technique and ability of the proposed system to meet utilities regulations, IEEE and IEC standards, are investigated. In an attempt to illustrate the potential superiority of SHE over carrier based or space vector pulse width modulation (PWM), this chapter demonstrates SHE allows a grid connected inverter to be controlled using a switching frequency of less than 1kHz, while the inverter is able to provide other necessary operation features such as independent control of active and reactive powers and operation control simplicity. For system validation, experimental results with SHE are compared to a inverter controlled using third harmonic injection PWM, with a 2kHz switching frequency. Furthermore, this thesis proposes a new implementation for SHE that utilizes the 3^{rd} harmonics to spread the switching angles over 90^{o} instead of them being located in a narrow range as generated when using conventional techniques, along with increased linear modulation index. The advantages of the proposed technique include implementation simplicity and flexibility in PWM waveforms. Simulations and experimentation to demonstrate the viability of SHE for grid connected inverters, are presented and discussed.

4.1. Background

The use of voltage source inverters (VSIs) as interfacing units for grid integration of photovoltaic (PV) systems has been investigated intensively in the last decade. This includes the use of two-level and multilevel VSIs[4.1-3]. A multilevel VSI approach seems unsuitable for photovoltaic grid integration due to the following reason: multilevel inverters with a common dc link bus, such as diode and flying capacitor clamped inverters, exacerbate the problem of partial shading as they require a large number of series connected PV cells in order to build a relatively high dc voltage appropriate for medium-voltage applications[4.4-10].Although the modularity of a cascaded multilevel inverter is attractive for PV systems [4.11, 12], it exposes the PV cells to a low frequency ac current component, and hence reduces PV lifetime [4.12-15]. The two-level VSI is widely used for grid connected PV systems, regardless of disadvantages such as high switching losses and relatively low quality output voltage waveforms[4.16]. Most grid connected PV systems presented in the literature are inappropriate for high-power application due to the use of a high switching frequency which leads to high switching losses and increased voltage stresses (*dv/dt*) on phase interfacing reactors and the transformer.

The current source option for PV grid interfacing has been advocated recently as a means of improving the effectiveness of maximum power point tracking (MPPT), as the number of series connected PV in each string is reduced[4.17, 18]. This reduces the impact of partial shading, and increases system efficiency by using one conversion stage instead of two stages, therein benefiting from the voltage boost capability of the current source inverter (lower dc link voltage and higher ac side voltage)[4.19-24]. This approach may not be viable for high-power medium-voltage PV systems, since current source inverters (CSI) usually have higher semiconductor losses than voltage source inverters (VSI) of similar rating, switching frequency, and ac side voltage. This is because the CSI can have twice the semiconductors in the conduction path at any instant, compared to the VSI[4.25-27].

With regard to the modulation strategies discussed in chapter three and grid codes and standards requirements, medium-voltage applications tend to favour the use of traditional modulation approaches such as selective harmonic elimination (SHE) and

carrier based pulse width modulation, over space vector modulation [4.28-31]. This chapter explores the possibility of using SHE to control high-power PV inverters in an attempt to suppress switching losses (by adopting switching frequencies less than 1kHz), improved dc link voltage utilization, and reduced phase interfacing reactor *dv/dt* [4.29, 30, 32, 33]. To facilitate the inverter control process, the low frequency output voltage switching waveforms produced using SHE are constructed using a relatively high sampling frequency, which is exclusively determined by the time required to execute the control algorithm in a DSP. The outcome of this investigation is substantiated using simulation and experimentation. For further demonstration of SHE advantages, SHE simulation and experimental results are compared to the case where the inverter is controlled using third harmonic injection PWM (THIPWM) that permits increased dc link voltage utilization [4.34].

All the grid connected inverter experiments discussed in this chapter use nine switching angles in an attempt to meet harmonic requirements at the point-of-common-coupling. Eight angles are used to eliminate non-triplen harmonics up to the 25^{th} harmonic. An attractive feature that led to the adoption of SHE in this chapter is that the magnitude of non-triplen harmonics eliminated remain insignificant over the full modulation index linear range (0 to 1). Such a feature is not available in space-vector and carrier based PWM.

4.2. Operation of the VSI in island and grid modes

A standalone ac system may be described as one in which the entire ac power is delivered to the system through inverters. In island mode, there are no synchronous alternators present to provide a reference for the system frequency and voltage. All the system inverters need to be operated to provide a stable frequency and voltage in the presence of arbitrarily varying loads. Output voltage quality is the main factor to be considered for power quality.

On the other hand, in the grid connected mode, the system must control and handle disturbances from the network such as unbalanced or distorted grid voltages. The inverter module supplies the grid with the required controlled active and reactive

powers. The power quality is determined by the current quantity as the voltage is not controlled by the PV unit.

4.2.1 Control system

The main target of the control system in island mode operation is to maintain the voltage and frequency within the standard specification limits. The control system must provide sufficient active and reactive power to match the connected load, therein providing high power quality.

The main target for grid-connected mode is to achieve good tracking of the controlled variables with minimal phase error. The tracking accuracy is constrained by the maximum allowable inverter switching frequency, the dc link voltage and the converter output inductance. Current control for grid connected inverters controls both the harmonic content and the power injected into the grid. Three main voltage and current control algorithms for the three-phase two-level VSI are briefly introduced.

A. Stationary proportional-integral (PI) controller

Conventional PI control is simple and easy to implement. The transfer function is:

$$G(s) = K_P + \frac{K_I}{s} \qquad (4.1)$$

The control variable is forced to track a time domain reference. The PI controller can achieve fast response and good harmonic rejection, when combined with a high inverter switching frequency. A compromise between reference tracking and stability is required in applications with a low switching frequency. However, the disadvantages of this controller are an inability to track a sinusoidal reference with zero steady-state error and poor disturbance rejection capability.

B. Synchronous proportional-integral (PI) controller

Synchronous PI control is only applicable to three (multi) phase systems. The three-phase ac quantities are transformed into dc components in the synchronous reference frame to ensure zero steady-state error, unlike in the stationery reference frame. The control transfer function is also given by equation (4.1). In the synchronous frame, stability is improved at the expense of response time and harmonic rejection. The technique must be extended to achieve good performance under distorted or unbalanced mains conditions. The disadvantage of this controller is the requirement for a phase

looked loop (PLL) for transformations, hence the performance is dependent on the PLL characteristics.

C. Proportional resonance (PR) controller

Proportional resonance (PR) control introduces an infinite gain at the fundamental frequency, and hence achieves zero steady-state error. The system is in the stationary frame with independence between phases. It can be used in single and three phase systems and the controller transfer function is:

$$G(s) = K_P + \frac{K_I s}{s^2 + \omega_o^2} \tag{4.2}$$

An infinite gain at the resonant frequency is not achievable in a digital system. Also, any slight displacement between the reference signal frequency and the measured signal resonant frequency leads to performance degradation. A modified PR controller is used to solve this problem, with a transfer function given by:

$$G(s) = K_P + \frac{2K_I \omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{4.3}$$

where ω_c is the integrator low frequency cut-off.

For digital implementation, a discrete time transfer characteristic is obtained via a Tustin transformation. As with the synchronous controller, control is limited to the fundamental frequency component. Unlike synchronous frame control, the phases are individually controlled, which gives more robust performance in the presence of imbalance.

4.3. Analysis of AC dynamic equations for the three-phase two-level voltage source inverter in island mode

Figure 0.1 show the circuit diagram of three-phase two-level voltage source inverter operating in island mode. A proportional-resonance (PR) voltage regulator control loop is shown in Figure 0.2.

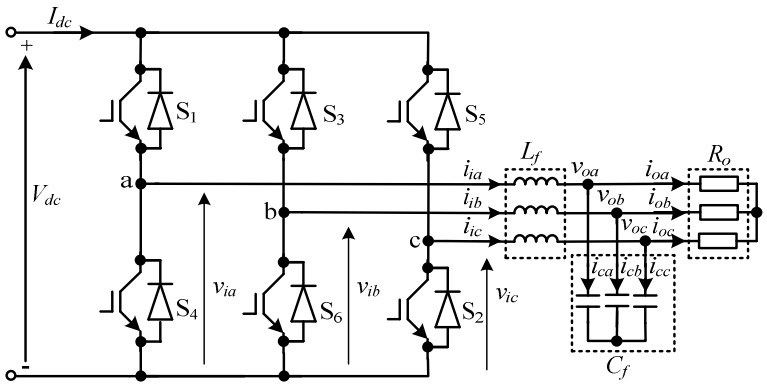


Figure 0.1: Circuit diagram of VSI in island mode.

A. Analysis of ac dynamic equations using proportional-resonance (PR) as a voltage regulator

Based on Figure 0.1, the dynamic equations that describe the VSI in the *abc* frame for island mode operation are:

$$i_{iabc} = i_{cabc} + i_{oabc} \tag{4.4}$$

$$\frac{dv_{oabc}}{dt} = \frac{1}{C_f}\left[i_{iabc} - \frac{v_{oabc}}{R_o} \right] \tag{4.5}$$

where v_{oabc} and $i_{iabc}=\gamma$ represent the output voltages and inverter currents, while L_f, C_f and R_o are the ac power filters and load respectively.

The proportional-resonance (PR) controller transfer function used in this chapter is expressed as:

$$y = k_{pv}e + k_{iv}\frac{es}{s^2 + \omega_o^2} \tag{4.6}$$

where k_{pv} is the proportional gain, k_{iv} is the integral gain, $e = v^*_{oabc} - v_{oabc}$ is the fundamental ac current error, and ω_o is the fundamental angular frequency.

The transfer function of the PR controller is digitized for DSP implementation using the following derivations.

Let

$$z = k_{iv} \frac{es}{s^2 + \omega_o^2} \tag{4.7}$$

Rearranging (4.7) to:

$$sz + \frac{\omega_o^2}{s} z = k_{iv} e \tag{4.8}$$

and

$$w = \frac{\omega_o^2}{s} z \tag{4.9}$$

By taking the derivative of (4.8)and (4.9):

$$\frac{dw}{dt} = \omega_o^2 z \tag{4.10}$$

$$\frac{dz}{dt} = k_{iv} e - w \tag{4.11}$$

where z and w are auxiliary control variables used to facilitate the control design. From (4.6), (4.10) and (4.11), the output of the PR controller can be rewritten as:

$$y = k_{pv} e + \int \left(k_{iv} e - \int \omega_o^2 z dt \right) dt \tag{4.12}$$

Replacing i_{iabc} in (4.4) with γ and from (4.5), including the output voltage error into the PR controller, the value of γ is obtained from (4.12):

$$\gamma = k_{pv} \left(v_{oabc}^* - v_{oabc} \right) + \int \left(k_{iv} \left(v_{oabc}^* - v_{oabc} \right) - \int \omega_o^2 z_v dt \right) dt \tag{4.13}$$

Substituting (4.13) into (4.5)

$$\frac{dv_{oabc}}{dt} = -\frac{\left(1 + R_o k_p\right)}{R_o C_f} v_{oabc} + \frac{k_p v_{oabc}^*}{C_f} + \frac{z_v}{C_f} \tag{4.14}$$

where

$$z_v = \int \left(k_{iv} \left(v_{abco}^* - v_{abco} \right) - w_v \right) dt \tag{4.15}$$

and

$$w_v = \int \omega_o^2 z_v dt \tag{4.16}$$

By taking the derivatives of (4.15) and (4.16)

$$\frac{dz_v}{dt} = k_{iv}\left(v^*_{abco} - v_{abco}\right) - w_v \tag{4.17}$$

$$\frac{dw_v}{dt} = \omega_o^2 z_v \tag{4.18}$$

From (4.14), (4.17) and (4.18), the state-space model of the voltage loop controller can be written in the form: $\frac{dx(t)}{dt} = Ax(t) + Bu(t)$

$$\frac{d}{dt}\begin{bmatrix} v_{oabc} \\ z_v \\ w_v \end{bmatrix} = \begin{bmatrix} -\frac{\left(1+R_o k_{pv}\right)}{R_o C_f} & \frac{1}{C_f} & 0 \\ -k_{iv} & 0 & -1 \\ 0 & \omega_o^2 & 0 \end{bmatrix} \begin{bmatrix} v_{oabc} \\ z_v \\ w_v \end{bmatrix} + \begin{bmatrix} \frac{k_{pv}}{C_f} \\ k_{iv} \\ 0 \end{bmatrix} v^*_{oabc} \tag{4.19}$$

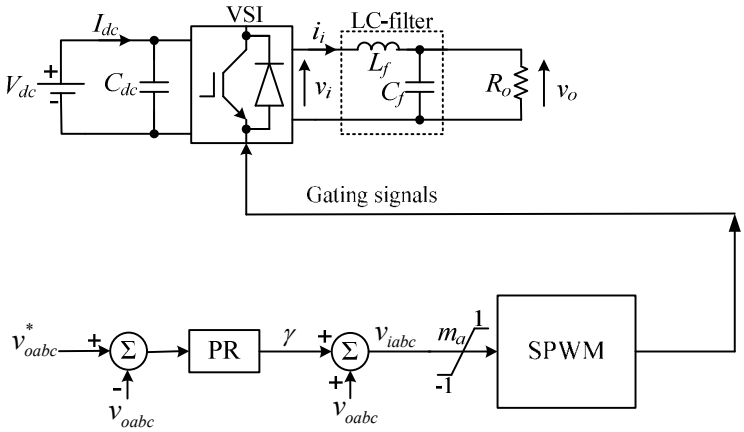


Figure 0.2: Schematic diagram of the voltage control loop using a PR controller.

B. Analysis of ac dynamic equations using proportional-integral (PI) as a voltage regulator

In the synchronous reference frame, the three-phase ac quantities are transformed into dc components to ensure any steady-state error is eliminated. Based on Figure 0.1, the inverter ac side dynamics in island mode can be expressed in the *d-q* axis reference frame as follows:

$$\frac{di_{cd}}{dt} = \frac{1}{L_f}\left[v_{id} + \omega L_f i_{oq} - v_{od}\right] \tag{4.20}$$

$$\frac{di_{cq}}{dt} = \frac{1}{L_f}\left[v_{iq} + \omega L_f i_{od} - v_{oq}\right] \tag{4.21}$$

$$\frac{dv_{od}}{dt} = \frac{1}{C_f}\left[i_{id} - \frac{v_{od}}{R_o} + \omega C_f v_{oq}\right] \tag{4.22}$$

$$\frac{dv_{oq}}{dt} = \frac{1}{C_f}\left[i_{iq} - \frac{v_{oq}}{R_o} - \omega C_f v_{od}\right] \tag{4.23}$$

Let $U_d = i_{id} + \omega C_f v_{oq}$ and $U_q = i_{iq} - \omega C_f v_{od}$, therefore (4.22) and (4.23) can be written as:

$$\frac{dv_{od}}{dt} = -\frac{v_{od}}{R_o C_f} + \frac{U_d}{C_f} \tag{4.24}$$

$$\frac{dv_{oq}}{dt} = -\frac{v_{oq}}{R_o C_f} + \frac{U_q}{C_f} \tag{4.25}$$

The variables U_d and U_q can be obtained from the proportional-integral (PI) controller as follows:

$$U_d = k_p\left(v_{od}^* - v_{od}\right) + k_i\int\left(v_{od}^* - v_{od}\right)dt \tag{4.26}$$

$$U_q = k_p\left(v_{oq}^* - v_{oq}\right) + k_i\int\left(v_{oq}^* - v_{oq}\right)dt \tag{4.27}$$

Replacing the integral parts of (4.26)and (4.27), with Z_d and Z_q, the following sets of equations are obtained:

$$U_d = k_p\left(v_{od}^* - v_{od}\right) + Z_d \tag{4.28}$$

$$U_q = k_p\left(v_{oq}^* - v_{oq}\right) + Z_q \tag{4.29}$$

$$\frac{dv_{od}}{dt} = -\frac{\left(1 + R_o k_p\right)}{R_o C_f} v_{od} + \frac{k_p v_{od}^*}{C_f} + \frac{Z_d}{C_f} \tag{4.30}$$

$$\frac{dv_{oq}}{dt} = -\frac{\left(1+R_o k_p\right)}{R_o C_f} v_{oq} + \frac{k_p v_{oq}^*}{C_f} + \frac{Z_q}{C_f} \tag{4.31}$$

$$\frac{dZ_d}{dt} = k_i \left(v_{od}^* - v_{od}\right) \tag{4.32}$$

$$\frac{dZ_q}{dt} = k_i \left(v_{oq}^* - v_{oq}\right) \tag{4.33}$$

Differential equations (4.30) to (4.33) can be written in state space form as:

$$\frac{d}{dt}\begin{bmatrix} v_{od} \\ v_{oq} \\ Z_d \\ Z_q \end{bmatrix} = \begin{bmatrix} -\frac{\left(1+R_o k_p\right)}{R_o C_f} & 0 & \frac{1}{C_f} & 0 \\ 0 & -\frac{\left(1+R_o k_p\right)}{R_o C_f} & 0 & \frac{1}{C_f} \\ -k_i & 0 & 0 & 0 \\ 0 & -k_i & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{od} \\ v_{oq} \\ Z_d \\ Z_q \end{bmatrix} + \begin{bmatrix} \frac{k_p}{C_f} & 0 \\ 0 & \frac{k_p}{C_f} \\ k_i & 0 \\ 0 & k_i \end{bmatrix} \begin{bmatrix} v_{od}^* \\ v_{oq}^* \end{bmatrix} \tag{4.34}$$

The voltage controller equations are:

$$i_{id} = U_d - \omega C_f v_{oq} = k_p \left(v_{od}^* - v_{od}\right) + k_i \int \left(v_{od}^* - v_{od}\right) dt - \omega C_f v_{oq} \tag{4.35}$$

$$i_{iq} = U_q + \omega C_f v_{od} = k_p \left(v_{oq}^* - v_{oq}\right) + k_i \int \left(v_{oq}^* - v_{oq}\right) dt + \omega C_f v_{od} \tag{4.36}$$

where the frequency ω is from the PLL and is treated as an input.

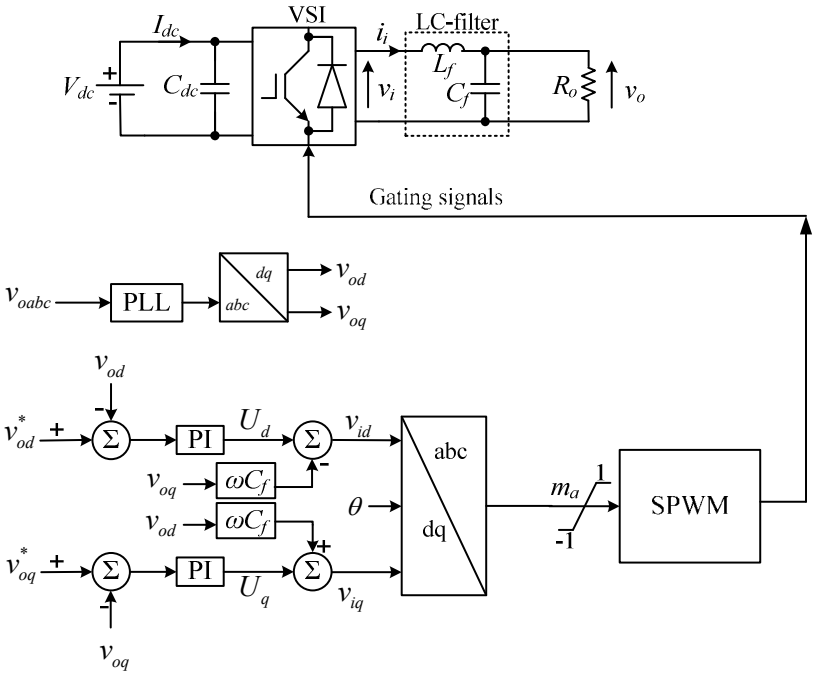


Figure 0.3: Control system of a VSI using PI control in the *dq*-frame.

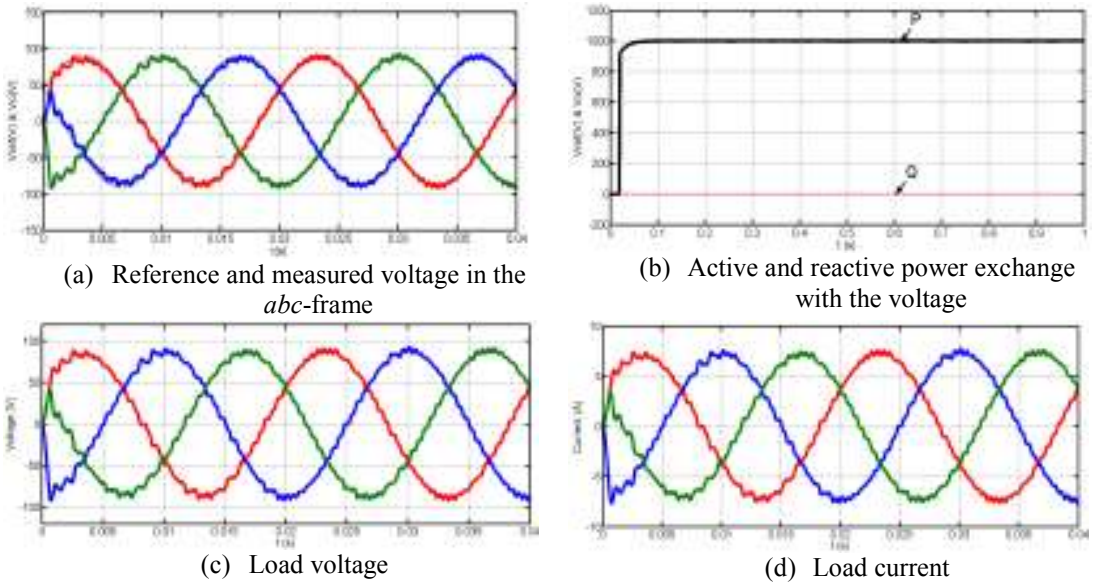
4.3.1. Simulation results of a three-phase VSI using PR control and PI control for island mode

The performance of a three-phase VSI using PR control and PI control for an island mode are investigated using Matlab/Simulink simulations. Both controllers are selected due to their ability to achieve zero steady-state error. The simulation results are based on the parameters in Table 0.1.

Table 0.1: System parameters.

Parameters		Values	
dc-link voltage	V_{dc}	200	V
Nominal frequency	f	50	Hz
Switching frequency	f_{sw}	2000	Hz
Filter inductance per phase	L_f	5	mH
Filter capacitance per phase	C_f	30	µF
PI controller proportional gain	k_p	0.5	
PI controller integral gain	k_i	300	
Resonant controller proportional gain	k_{pv}	10	
Resonant controller integral gain	k_{iv}	1200	

The VSI performances in island mode are investigated using a voltage-controlled PR controller and SPWM as the modulator, and are presented in Figure 0.4(a) to (d). The parameters used are listed in Table 0.1.



(a) Reference and measured voltage in the *abc*-frame

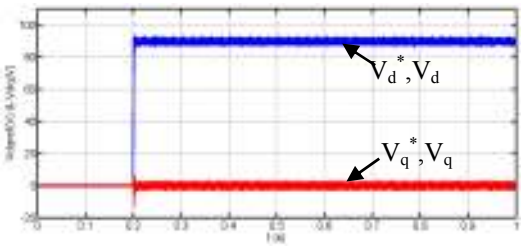
(b) Active and reactive power exchange with the voltage

(c) Load voltage

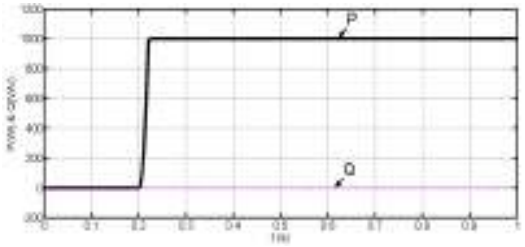
(d) Load current

Figure 0.4: Simulation waveforms illustrating three-phase VSI controlled by PR controller in island mode.

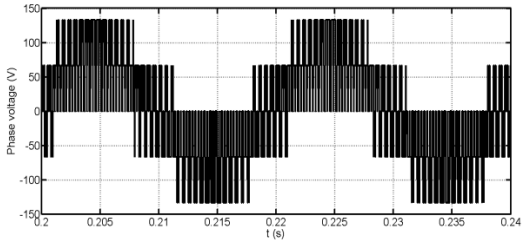
The three-phase VSI output voltage is controlled using PI control in the *dq*-frame, with the VSI supplying active and reactive power for a balanced load. The controller performance is assessed using a 1kW step balanced resistive load change at 0.2s. Figure 0.5(a) presents the ability of the measured output voltage, V_d, to track the reference while V_q is maintained at 0V. The output active and reactive powers are shown in Figure 0.5(b). Figure 0.5(c) to (e) show the phase voltage, line-to-line voltage, and sinusoidal output voltage waveforms in a steady-state condition. A disturbance exists during the output voltage transient, see Figure 0.5(e).A balanced, sinusoidal output current for the resistive load following a step change from no load is shown in Figure 0.5(f), while a modulation index of nearly 0.9 is achieved in Figure 0.5(g).All three phases are controlled independently, unlike with synchronous *dq*-frame control, which is expected to give more robust performance for both balanced and unbalanced loads. From the simulation results, both controllers achieve zero steady-state error and obtain balanced, sinusoidal output voltages and currents for a resistive load.



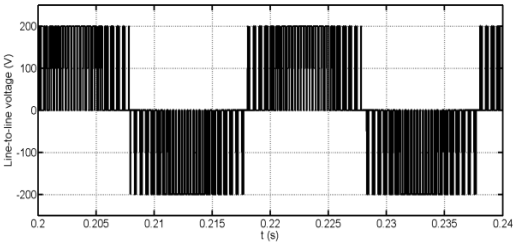
(a) Reference and measured voltage in *dq*-frame (step change in active voltage, V_d)



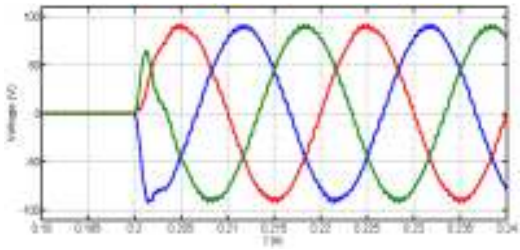
(b) Active and reactive power exchange with the load voltage



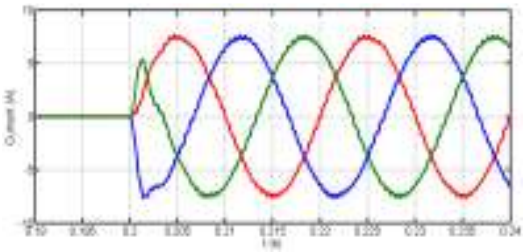
(c) Phase voltage



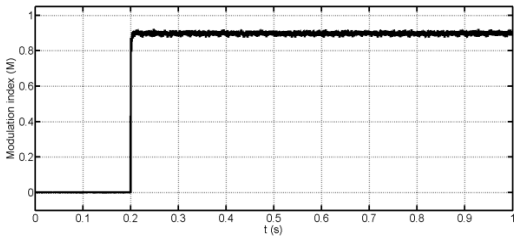
(d) Line-to-line voltage



(e) Load voltage



(f) Load current

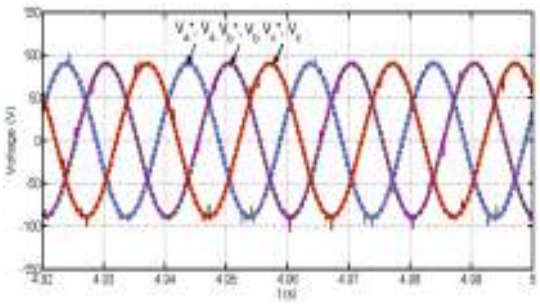


(g) Modulation index

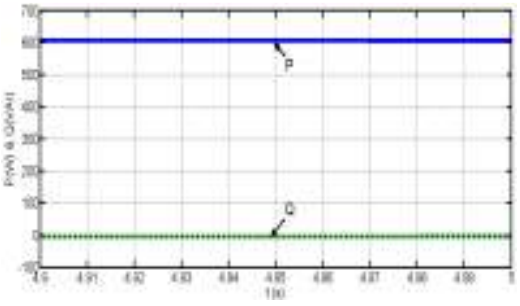
Figure 0.5: Simulation waveforms when three-phase VSI is controlled by synchronous frame PI controller and SPWM as the modulator is in island mode.

4.3.2. Experimental verification of three-phase VSI using PR control and PI control for island mode

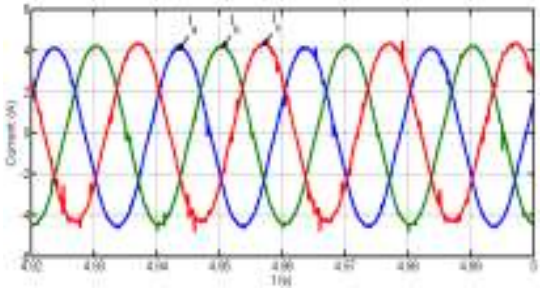
The corresponding experimental results using PR control in the *abc* and synchronous *dq*-frame PI control systems are shown in Figure 0.6 and 4.7 respectively. The reference output voltages, V_o are set to 90V and Figure 0.6(a) and 4.7(a) show that the measured voltages successfully track their respective references without any oscillatory and delay effects. In Figure 0.6(b) and 4.7(b), both controllers produce similar active and reactive power totals. The load currents and modulating signals for the VSIs operating in an island mode, using PR control, are shown in Figure 0.6(c) and (d). Figure 0.7(c) to (e) present the experimental output voltages, load currents and modulation index results when the VSI is controlled using PI control in the *dq*-reference frame.



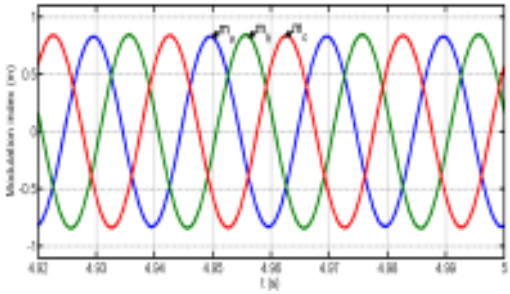
(a) Output voltages and their respective references



(b) Active and reactive power

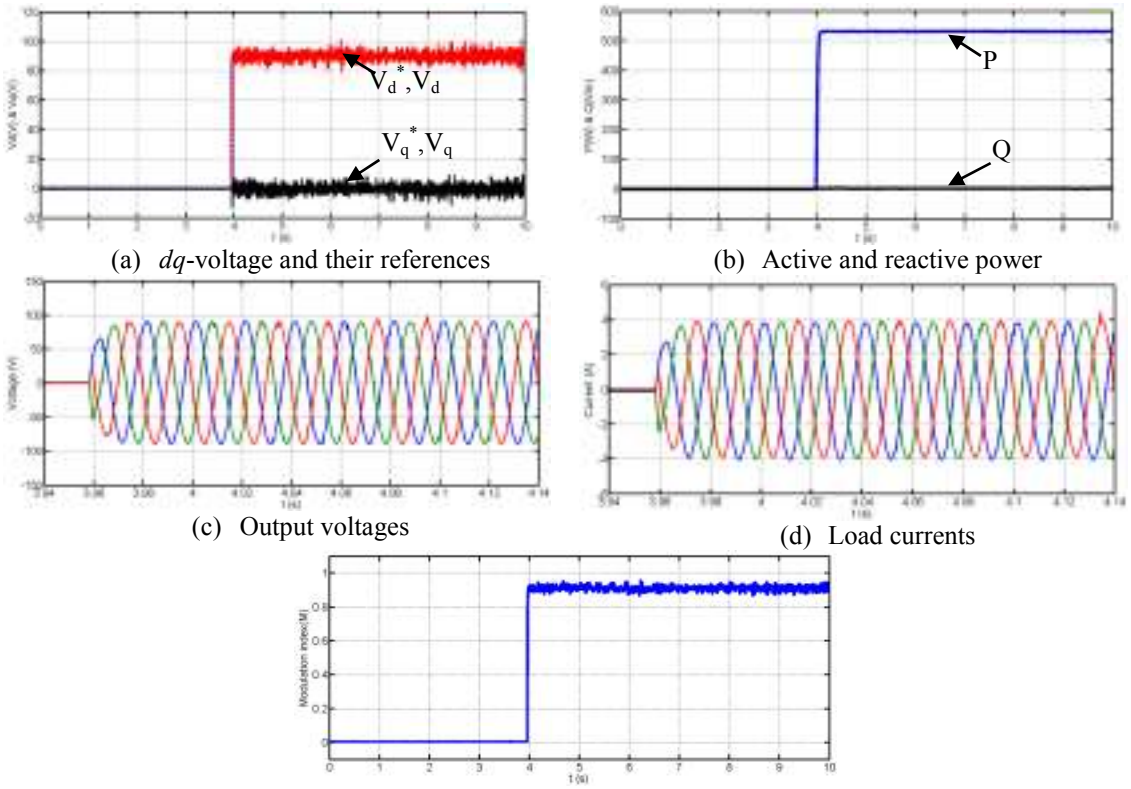


(c) Three-phase load currents



(d) Modulating signals

Figure 0.6:dSPACE 1006 control desk experimental results of the three-phase VSI scaled-prototype connected to balanced loads when controlled using a PR controller in an *abc* frame.



(a) *dq*-voltage and their references

(b) Active and reactive power

(c) Output voltages

(d) Load currents

(e) Modulation index

Figure 0.7: dSPACE 1006 control desk experimental results of a three-phase VSI scaled-prototype connected to balanced loads when it is controlled using a synchronous *dq*-frame PI controller.

4.4. Analysis of ac-side dynamic equations of grid connected VSI using proportional-resonance control in *abc* coordinates

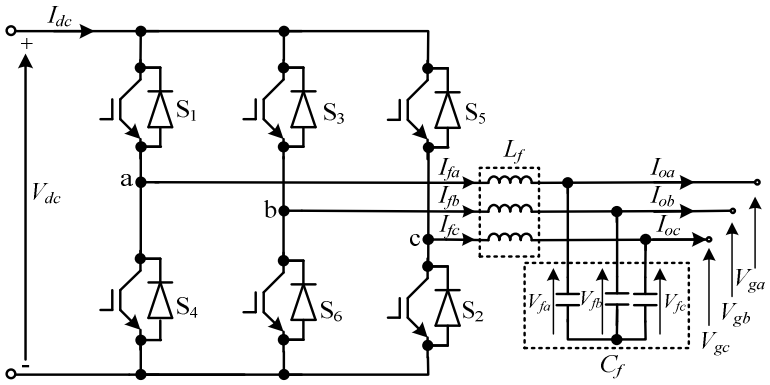


Figure 0.8: Schematic diagram of a grid-connected three-phase VSI.

Based on Figure 0.8, the differential equation describing the inverter ac-side dynamics, when considering only fundamental ac currents and voltages, is:

$$\frac{dI_{fabc}}{dt} = -\frac{R_f}{L_f} I_{fabc} + \frac{V_{con\_abc} - V_{fabc}}{L_f} \tag{4.37}$$

By setting $Y = V_{abc\_con} - V_{fabc}$, equation (4.37) can be written as:

$$\frac{dI_{fabc}}{dt} = -\frac{R_f}{L_f} I_{fabc} + \frac{Y}{L_f} \tag{4.38}$$

From (4.37)and (4.38), by feeding the grid current error to the PR controller, the value of Y is obtained from (4.12)

$$Y = K_{pi}\left(I^*_{fabc} - I_{fabc}\right) + \int\left(K_{ii}\left(I^*_{fabc} - I_{fabc}\right) - \int \omega_o^2 Z_i dt\right)dt \tag{4.39}$$

Substituting (4.39) and (4.37)

$$\frac{dI_f}{dt} = \frac{K_{pi} I^*_f}{L_f} - \frac{K_{pi} I_f}{L_f} - \frac{R_f I_f}{L_f} + \frac{Z_i}{L_f} \tag{4.40}$$

where

$$Z_i = \int\left(K_{ii}\left(I^*_f - I_f\right) - W_i\right)dt \tag{4.41}$$

and

$$W_i = \int \omega_o^2 Z_i dt \tag{4.42}$$

whereK_{pi} is the current controller proportional gain and K_{ii} is the current controller integral gain.

By taking the derivative of (4.41)and (4.42):

$$\frac{dZ_i}{dt} = K_{ii}\left(I_f^* - I_f\right) - W_i \tag{4.43}$$

$$\frac{dW_i}{dt} = \omega_o^2 Z_i \tag{4.44}$$

From (4.40), (4.43) and (4.44), the state-space model of the current loop controller is:

$$\frac{d}{dt}\begin{bmatrix} I_f \\ Z_i \\ W_i \end{bmatrix} = \begin{bmatrix} -\dfrac{\left(R_f + K_{pi}\right)}{L_f} & \dfrac{1}{L_f} & 0 \\ -K_{ii} & 0 & -1 \\ 0 & \omega_o^2 & 0 \end{bmatrix}\begin{bmatrix} I_f \\ Z_i \\ W_i \end{bmatrix} + \begin{bmatrix} \dfrac{K_{pi}}{L_f} \\ K_{ii} \\ 0 \end{bmatrix} I_f^* \tag{4.45}$$

From (4.45), the proportional-resonance control structure in *abc* coordinates used to regulate the output current and deliver the active and reactive powers into the ac grid, is illustrated in Figure 0.9.

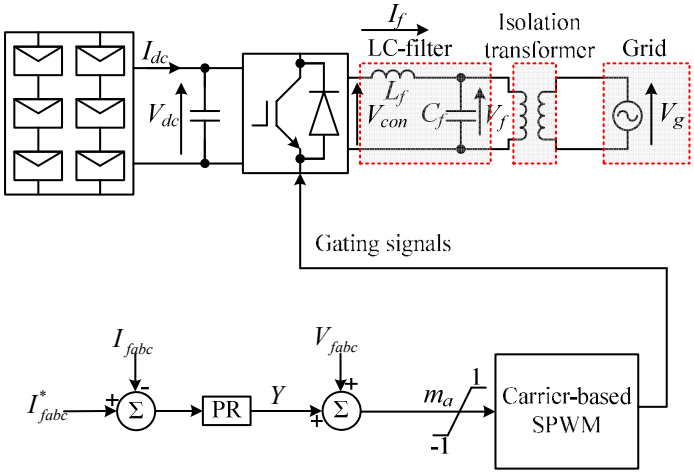
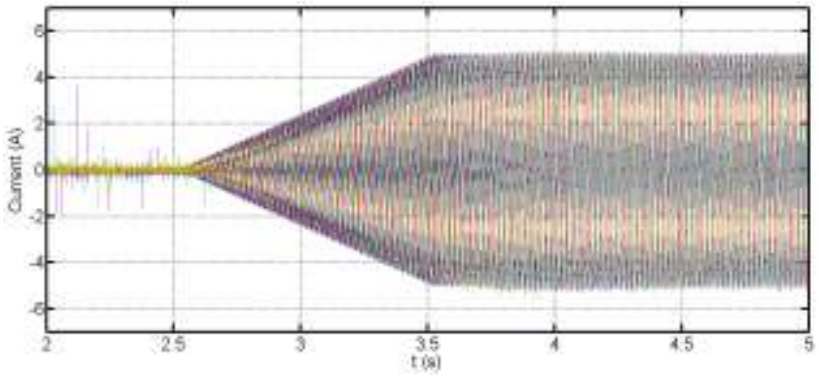
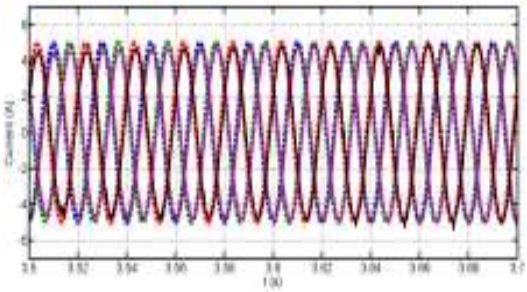


Figure 0.9: Schematic diagram consists of PR control system in *abc* coordinates that is used to control the output current of grid-connected VSI.

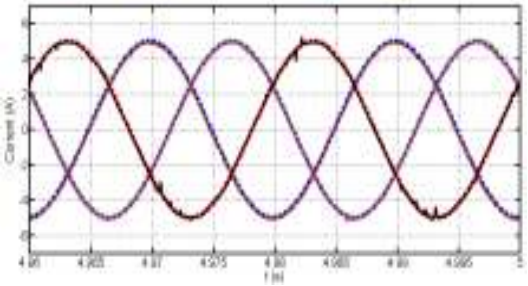
Figure 0.10 shows the experimental results from the dSPACE 1006 DSP platform for a grid-connected VSI using the PR control system in Figure 0.9. Figure 0.10(a) to (c) show the ability of the output currents to track the 5A references during transient and steady-state conditions. It is confirmed that the output currents successfully track the references while delivering active power of 600W at unity power factor, as demonstrated in Figure 0.10(d). The ac grid voltage is shown in Figure 0.10(e).



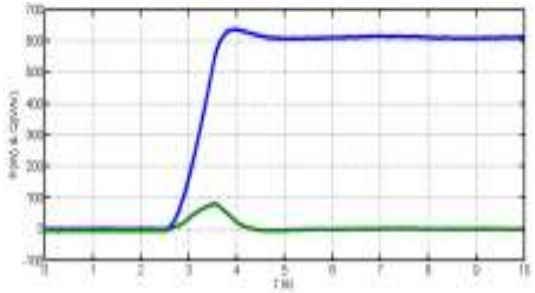
(a) Output phase current with their respective references



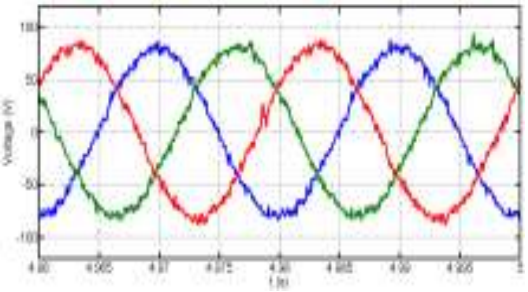
(b) Currents and their references during the transient



(c) Currents and their references during steady-state



(d) Active and reactive power exchange with grid voltage



(e) Grid voltage

Figure 0.10: Experimental results showing the performance of a VSI injecting current into the grid.

4.5. Analysis of AC side dynamic equation of a grid-connected VSI using proportional-integral control in the *dq*-frame

This section discusses the control systems of the grid connected inverter, and discusses the control variables that could be manipulated from a power electronic systems standpoint, including most of the possible physical limitations imposed by the ac side passive elements which are not well documented. A generic phasor diagram and P-Q envelope are presented that illustrate the operation of grid connected converters.

The active and reactive powers are regulated using direct power control, where the filter bus voltage is assumed constant. Inverter power injection into the grid is regulated in the synchronous reference frame, where the voltage magnitude at the filter bus is aligned with the *d*-axis (the reference for the whole system, in other words all measurements in the *d-q* axes will be relative to the filter bus voltage). Based on this principle and Figure 0.8, the inverter ac side dynamics can be expressed in the *d-q* axis reference frame as follows:

$$\frac{dI_{fd}}{dt} = -\frac{R_f}{L_f} I_{fd} + \frac{\left[V_{cd} - V_{fd} + \omega L_f I_{fq}\right]}{L_f} \tag{4.46}$$

$$\frac{dI_{fq}}{dt} = -\frac{R_f}{L_f} I_{fq} + \frac{\left[V_{cq} - V_{fq} - \omega L_f I_{fd}\right]}{L_f} \tag{4.47}$$

Let $Q_d = V_{cd} - V_{fd} + \omega L_f I_{fq}$ and $Q_q = V_{cq} - V_{fq} - \omega L_f I_{fd}$, therefore (4.46) and (4.47) can be written as:

$$\frac{dI_{fd}}{dt} = -\frac{R_f}{L_f} I_{fd} + \frac{Q_d}{L_f} \tag{4.48}$$

$$\frac{dI_{fq}}{dt} = -\frac{R_f}{L_f} I_{fq} + \frac{Q_q}{L_f} \tag{4.49}$$

Variables Q_d and Q_q can be obtained from the proportional-integral (PI) controller as follows:

$$Q_d = K_P(I^*_{fd} - I_{fd}) + K_I \int (I^*_{fd} - I_{fd})dt \tag{4.50}$$

$$Q_q = K_P(I^*_{fq} - I_{fq}) + K_I \int (I^*_{fq} - I_{fq})dt \tag{4.51}$$

Replacing the integral parts of (4.50) and (4.51) with W_1 and W_2, the following sets of equations are obtained:

$$Q_d = K_P(I^*_{fd} - I_{fd}) + W_1 \tag{4.52}$$

$$Q_q = K_P(I^*_{fq} - I_{fq}) + W_2 \tag{4.53}$$

$$\frac{dI_{fd}}{dt} = -\frac{\left(R_f + K_P\right)}{L_f} I_{fd} + \frac{W_1}{L_f} + \frac{K_P}{L} I^*_{fd} \tag{4.54}$$

$$\frac{dI_{fq}}{dt} = -\frac{\left(R_f + K_P\right)}{L_f} I_{fq} + \frac{W_2}{L_f} + \frac{K_P}{L} I^*_{fq} \tag{4.55}$$

$$\frac{dW_1}{dt} = K_I (I^*_{fd} - I_{fd}) \tag{4.56}$$

$$\frac{dW_2}{dt} = K_I (I^*_{fq} - I_{fq}) \tag{4.57}$$

Differential equations (4.54) to (4.57) can be written in state space form as:

$$\begin{bmatrix} \frac{dI_{fd}}{dt} \\ \frac{dI_{fq}}{dt} \\ \frac{dW_1}{dt} \\ \frac{dW_2}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{\left(R_f + K_P\right)}{L_f} & 0 & \frac{1}{L_f} & 0 \\ 0 & -\frac{\left(R_f + K_P\right)}{L_f} & 0 & \frac{1}{L_f} \\ -K_I & 0 & 0 & 0 \\ 0 & -K_I & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{fd} \\ I_{fq} \\ W_1 \\ W_2 \end{bmatrix} + \begin{bmatrix} \frac{K_P}{L_f} & 0 \\ 0 & \frac{K_P}{L_f} \\ K_I & 0 \\ 0 & K_I \end{bmatrix} \begin{bmatrix} I^*_{fd} \\ I^*_{fq} \end{bmatrix} \tag{4.58}$$

The Eigen-values of grid current controller is computed in (4.58). These Eigen-values represent the poles of the entire system with all controllers incorporated. It means that this approach take into account all the potential interaction between the cascaded loops. These Eigen-values hold important information such as damping factor, settling time, natural frequency and oscillation frequency. On this basis, all controller theoretical gains can be selected and adjusted accordingly to ensure all Eigen-values (poles) have negative parts, which an indication of stable system. The imaginary part of these Eigen-values represent the oscillation frequencies.

The *d-q* voltage components at the converter, which represent the voltage references to the modulator, can be estimated from the expressions for Q_d and Q_q, taking into account feed-forward terms as follows [4.35, 36]:

$$V_{cd} = Q_d + V_{fd} - \omega L_f I_{fq} \tag{4.59}$$

$$V_{cq} = Q_q + V_{fq} + \omega L_f I_{fd} \tag{4.60}$$

The current references are calculated directly from the desired active and reactive power set points as follows:

$$\begin{bmatrix} I_{fd}^{*} \\ I_{fq}^{*} \end{bmatrix} = \frac{2}{3} \frac{1}{V_{fd}^{2} + V_{fq}^{2}} \begin{bmatrix} V_{fd} & V_{fq} \\ V_{fq} & -V_{fd} \end{bmatrix} \begin{bmatrix} P^{*} \\ Q^{*} \end{bmatrix} \tag{4.61}$$

In PV applications, P^{*} can be obtained from the maximum power tracking error. A dc voltage controller that adjusts the PV cells operating point in order to maximize power extraction is used.

Figure 0.11 summarizes the grid connected inverter control systems used in this research, including the SHE implementation and THI pulse width modulation. Figure 0.12(a) shows the generic phasor diagram for the voltage source grid connected inverter. This phasor diagram illustrates the control principle of the VSI, including operating regions and boundaries in steady-state. When the voltage vector at the converter terminal $\vec{V}_c$ is in advance of the filter bus $\vec{V}_f$, the power flow is from the dc side to the ac network, and vice versa. When the voltage magnitude at converter terminal V_c is larger than at the filter bus V_f, where power injection into the grid is controlled, reactive power flows from the converter to the ac network (provision of leading VAr). Therefore converter active and reactive powers can be manipulated using the load angle δ and voltage magnitude at the converter terminal, V_c.

In VSIs, the phase interfacing inductor L_f is not only required for filtering and fault purposes, and is also necessary to provide phase shift δ to enable active power control. Also, it has to be sized appropriately not to limit the converter's ability to generate reactive power for a given dc link voltage. In this chapter the interfacing inductor L_f is sized so as to ensure the converter is able to provide its maximum design value of reactive power. The selection criterion for L_f is described as follows: as R_f is normally small compared to the reactance of the phase interfacing reactor-resistance can be neglected.

Therefore, the steady-state I_{fd} and I_{fq} can be obtained from equations (4.46) and (4.47) by setting the derivative terms to zero, and V_{fq}=0 since the voltage vector is aligned with the *d*-axis:

$$I_{fd} = \frac{V_{cq}}{\omega L_f} \tag{4.62}$$

$$I_{fq} = -\frac{(V_{cd} - V_{fd})}{\omega L_f} \tag{4.63}$$

Active and reactive powers *P* and *Q* at the filter bus can be expressed as:

$$P = \tfrac{3}{2} V_{fd} I_{fd} = \tfrac{3}{2} \frac{V_{cq} V_{fd}}{\omega L_f} \tag{4.64}$$

$$Q = -\tfrac{3}{2} V_{fd} I_{fq} = \tfrac{3}{2} \frac{V_{cd} V_{fd}}{\omega L_f} - \tfrac{3}{2} \frac{V_{fd}^2}{\omega L_f} \tag{4.65}$$

Equation (4.64)can be rewritten as shown in (4.66):

$$P + \tfrac{3}{2} \frac{V_{cd}^2}{\omega L_f} = \tfrac{3}{2} \frac{V_{cd} V_{fd}}{\omega L_f} \tag{4.66}$$

The converter active and reactive power capability curve (*P*-*Q* envelope) can be obtained by squaring, then adding, (4.66) and(4.65). The voltage at converter terminal is $V_c^2 = V_{cd}^2 + V_{cq}^2$:

$$P^2 + (Q + \tfrac{3}{2} \frac{V_d^2}{\omega L_f})^2 = (\tfrac{3}{2} \frac{V_c V_{fd}}{\omega L_f})^2 \tag{4.67}$$

Figure 0.12(b) depicts the converter's active and reactive power capability curve. The upper and lower of active-power axis (*P*) represent the over-excitation and under-excitation operating regions, where the converter releases and absorbs reactive energy to and from the ac grid. For medium-voltage where the PV inverter has to provide reactive power support to the ac network, L_f must be sized based on (4.67), assuming maximum active and reactive power capabilities. Therefore equation (4.67) can rewritten as:

$$X^2 P_{\max}^2 + (XQ_{\max} + \tfrac{3}{2} V_{fd}^2)^2 - (\tfrac{3}{2} V_c V_{fd})^2 = 0 \tag{4.68}$$

where $X = \omega L$.

For an inverter with V_{dc}=300V, P_{max}=1000W and Q_{max}=±663VAr, connected to a 110V ac network, the maximum interfacing inductance obtained after solving (4.68) for X is L_f≤36mH, assuming $V_c = \frac{1}{2} m_a V_{dc} = 0.575 V_{dc}$. For reactive power applications, such as a STATCOM [4.30], the phase interfacing inductor L_f can be selected based on maximum converter reactive power capability Q_{max} when P=0. Therefore, equation (4.67)reduces to:

$$Q_{\max} = \frac{3}{2} \frac{V_{fd}}{\omega L_f} (V_c - V_{fd}) \tag{4.69}$$

Assuming the same inverter parameters:

$$L_f \le \frac{3}{2} \frac{V_{fd}(V_c - V_{fd})}{\omega Q_{\max}} \le \frac{3}{2} \times \frac{155 \times (173 - 155)}{2 \times \pi \times 50 \times 663} \le 21\text{mH}. \tag{4.70}$$

This discussion is intended to show that sizing of the phase interfacing reactors for grid connected inverters is not merely based on filter design as found in many papers in the literature. Sizing has to take into consideration the converter capability curve as demonstrated in this chapter. The capacitor C_f is sized here to place the low-pass filter cut-off frequency between 150Hz and 200Hz. Despite this approach being commonly used for low power applications, it is not appreciated in high-power inverters that are connected to medium and high voltages. Instead, tuned filters target the significant switching frequency harmonic components and their sidebands that are not cancelled in the line-to-line voltage.

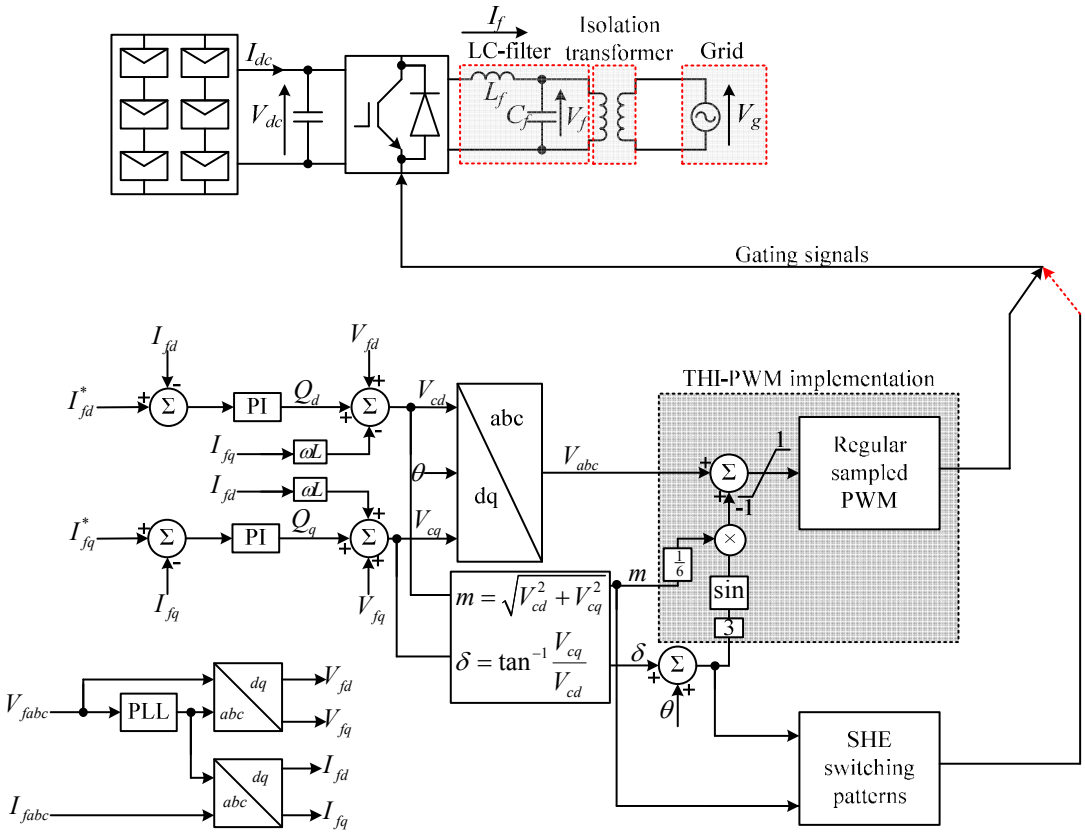
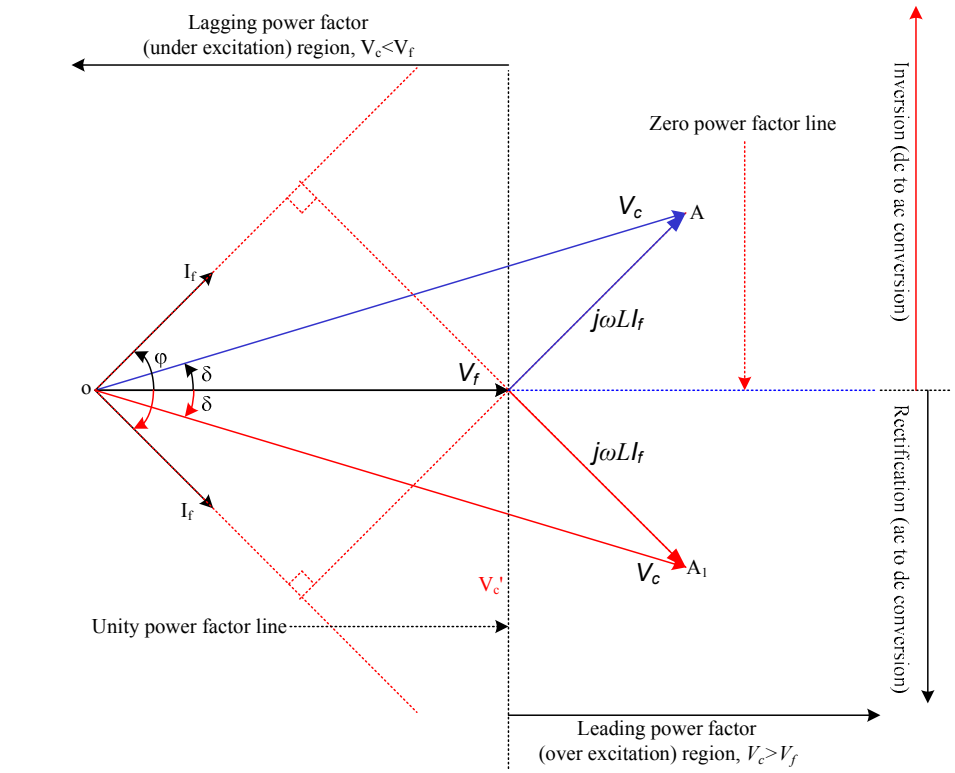
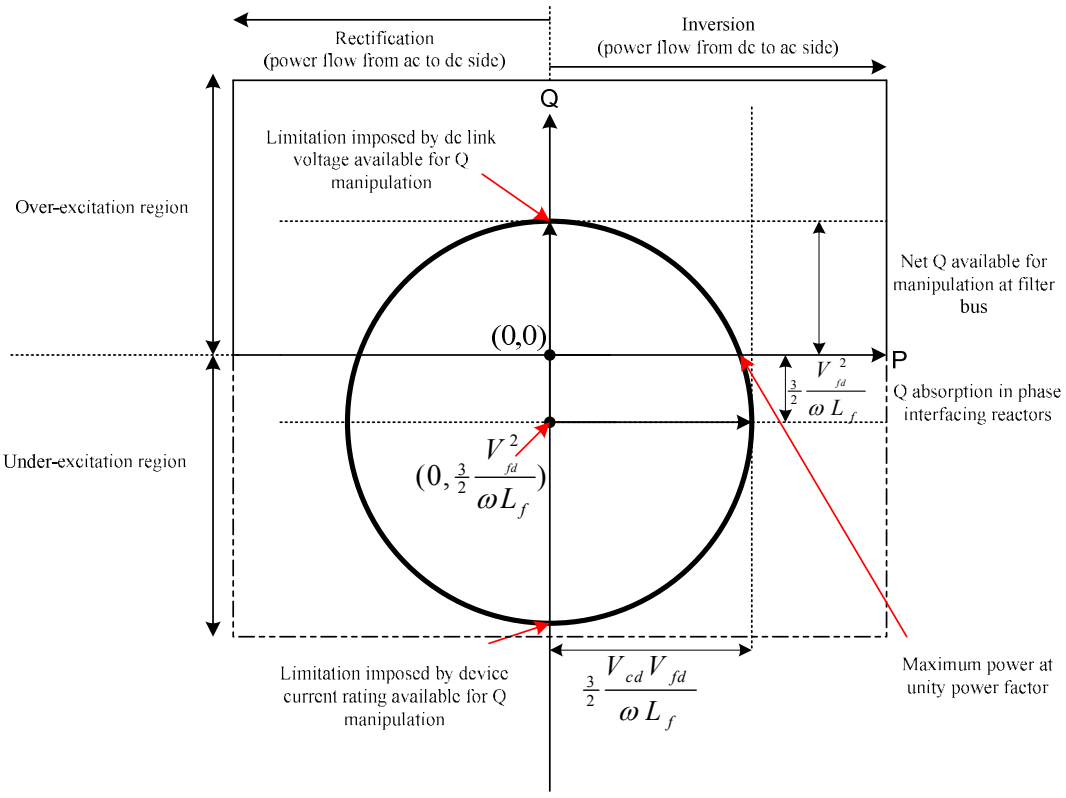


Figure 0.11: Schematic diagram of a grid connected PV inverter with SHE and THI-PWM using a dSPACE1006 hardware implementation.



(a)



(b)

Figure 0.12: Voltage source converter (a) generic phasor diagram and (b) theoretical capability curve.

4.6. Simulation results for a VSI in a medium voltage photovoltaic application

This section presents simulation results for a medium-voltage PV-inverter when controlled with SHE and sinusoidal PWM with triplen harmonic injection. These results aim to show that SHE can be used instead of carrier based PWM strategies to control grid connected PV inverters, whilst maintaining all of the control features achieved with carrier based strategies. Table 0.2 shows the simulation parameters used in this chapter. Figure 0.13 to Figure 0.17 show current, voltage and power waveforms obtained with SHE and THIPWM when exchanging active and reactive power. The results presented in Figure 0.13 and 4.8 are obtained when the active power current component I_d is varied from 0 to 1.0 pu (25MVA and 11kV based). SHE produces a similar performance to that of THIPWM at approximately half the switching frequency, including systems dynamics, and ac voltage and current waveform quality. Similar SHE performances are seen in Figure 0.15 and for THIPWM in Figure 0.16 when the inverter operates at full active power, 0.8 power factor lagging. VSI operation at zero power factor is presented in Figure 0.17. For further illustration of the potential reductions achievable in switching losses with SHE, Table 0.3 and 4.4 are presented. Table 0.3 presents the IGBT parameters used in the switching loss calculations, based on equations (4.71) and (4.72)[4.37, 38]:

$$\begin{aligned} P_{sw\_IGBT} &= \frac{f_{sw}}{4\pi}\int_{\varphi}^{\pi+\varphi}\left(\left(k_{on1}+k_{on2}\right)\cdot I_m \sin\left(\omega t-\varphi\right)+k_{off1}+k_{off2}\right)d\omega t \\ &= \frac{f_{sw}\left(k_{on1}+k_{on2}\right)\cdot I_m}{2\pi}+\frac{f_{sw}}{4}\left(k_{off1}+k_{off2}\right) \end{aligned} \tag{4.71}$$

$$\begin{aligned} P_{sw\_diode} &= \frac{f_{sw}}{4\pi}\int_{\varphi+\pi}^{2\pi+\varphi}\left(k_{D1}\cdot I_m \sin\left(\omega t-\varphi\right)+k_{D2}\right)d\omega t \\ &= \frac{f_{sw}\cdot k_{D1}\cdot I_m}{2\pi}+\frac{f_{sw}}{4}k_{D2} \end{aligned} \tag{4.72}$$

Table 0.4 summarises the inverter switching losses for three operating conditions. Based on these results it can be concluded that SHE produces lower losses than THIPWM, for similar operating conditions.

Table 0.2: Simulation parameters of a multi-megawatt PV inverter.

Parameters		Values
Converter power rating (MVA)		25
DC link voltage (kV)		20
AC voltage (line-to-line in kV)		11
Active power capability (MW)		20
Reactive power capability (MVAr)		15
Grid frequency (Hz)		50
Switching frequency (kHz)	THIPWM	2
	SHE	0.95
Current control proportional gain, K_p	THIPWM	70
	SHE	220
Current control integral gain, K_i	THIPWM	3000
	SHE	5000

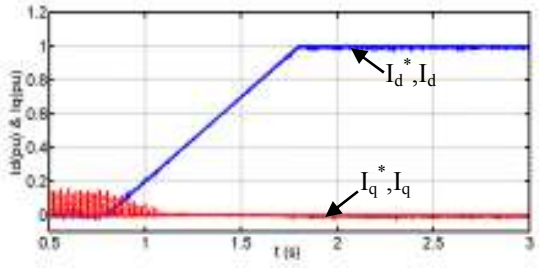
Table 0.3: Converter switching device data used for switching loss estimation, including turn-on, turn-off, and diode recovery losses, based on IGBT MG1200FXF1US53.

R_{on} (IGBT)	1.75mΩ	K_{on1}	0.0016J/A
R_{on} (diode)	1.64mΩ	K_{on2}	0.029J
V_0 (IGBT) or V_T	1.2V	K_{off1}	0.0017J/A
V_0 (diode) or V_F	1.05V	K_{off2}	0.35J
IGBT rating	3.3kV	K_{D1}	0.0006J/A
Number of series devices per arm	14	K_{D2}	0.398J

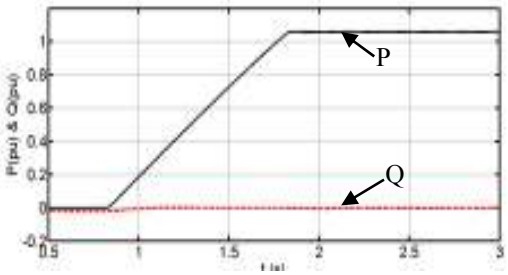
Table 0.4: Summary of switching losses with THIPWM and SHE modulation strategies for a 25MVA PV-inverter.

Operating condition	P=20MW at 0.8 power factor lagging	Q=15MVAr at zero power factor	20MW at unity power factor
SHE	190.6 kW	190.2kW	88.7kW
THIPWM	401.2kW	400.4kW	401.2kW

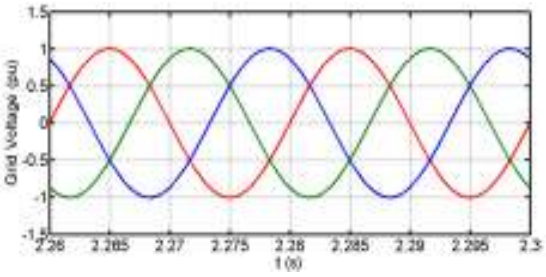
A. 20MW at unity power factor



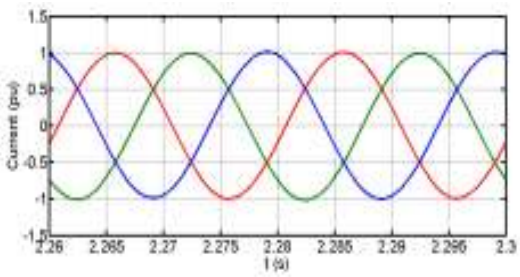
(a) Variation of active current, for PV inverter operating at full-load



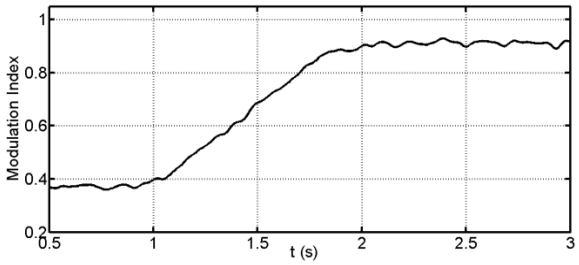
(b) Active and reactive power PV inverter exchanges with the grid



(c) Normalized grid voltage

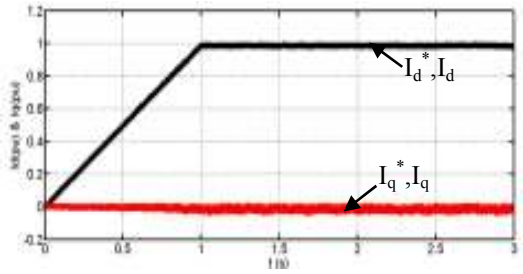


(d) Normalized current

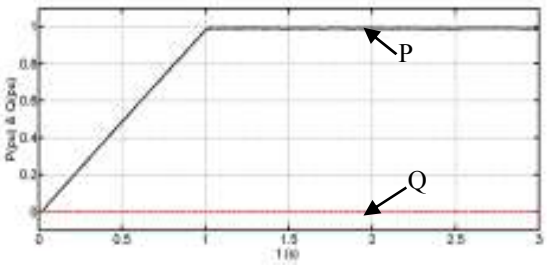


(e) Modulation index with variation of active power

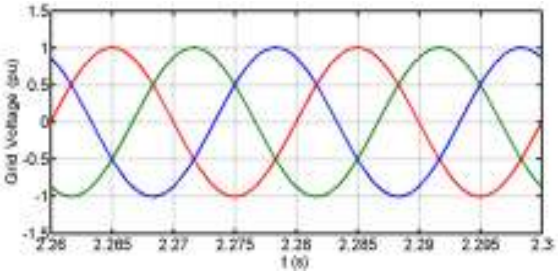
Figure 0.13: Simulation waveforms demonstrating operation of a high-power medium-voltage grid connected PV-inverter when controlled using SHE-PWM, with a 950Hz switching frequency, 20kV dc link voltage, and connected to a 11kV ac grid (step change in active power).



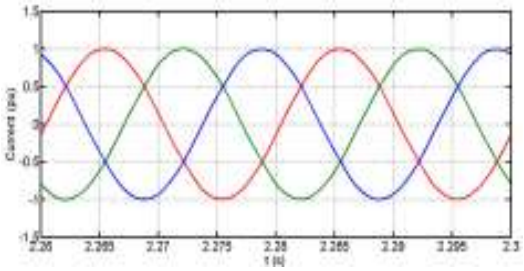
(a) Variation of active current when PV inverter operates at full-load



(b) Active and reactive power PV inverter exchanges with the grid



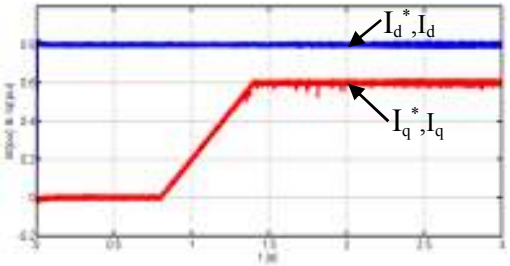
(c) Normalized grid voltage



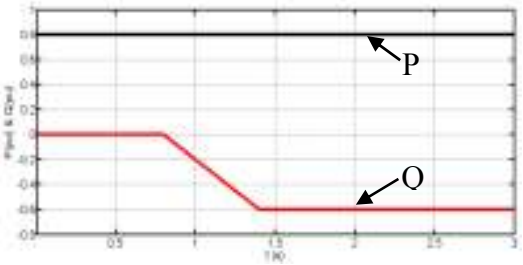
(d) Normalized output current

Figure 0.14: Simulation waveforms demonstrating operation of a high-power medium-voltage grid connected PV-inverter when controlled using THI-PWM, with a 2kHz switching frequency, 20kV dc link voltage, and connected to a 11kV ac grid (step change in active power).

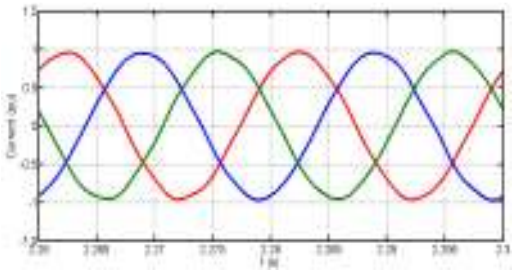
B. 20MW at 0.8 power factor lagging



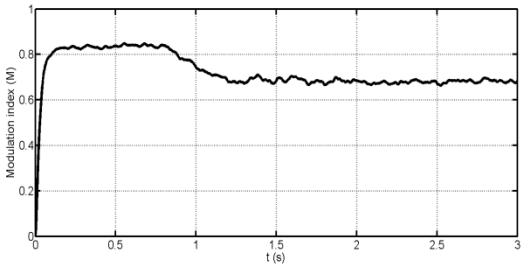
(a) Variation of reactive current when PV inverter operate at 0.8 power factor lagging



(b) Active and reactive power exchange with the grid voltage

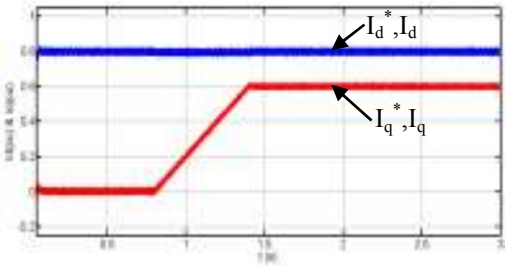


(c) Normalized output current

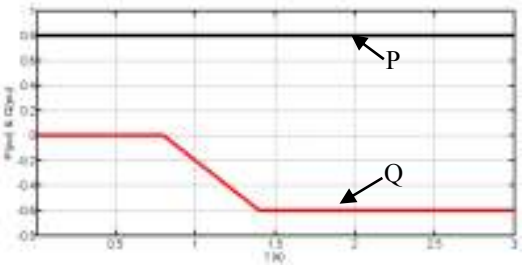


(d) Modulation index

Figure 0.15: Simulation waveforms demonstrating operation of grid connected PV-inverter when controlled using SHE-PWM during rated power of 20MW, 0.8 power factor lagging.

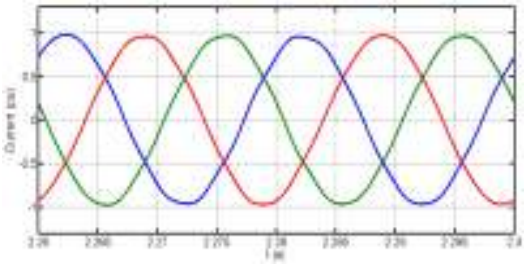


(a) Variation of reactive current when PV inverter operate at 0.8 lagging



(b) Active and reactive power PV inverter exchanges with the grid

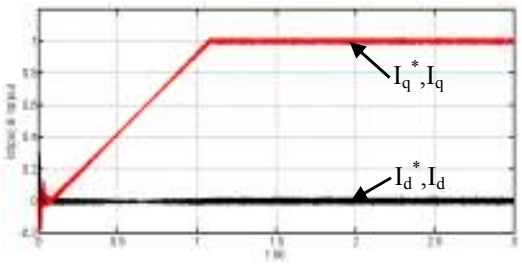
(c) Normalized grid voltage



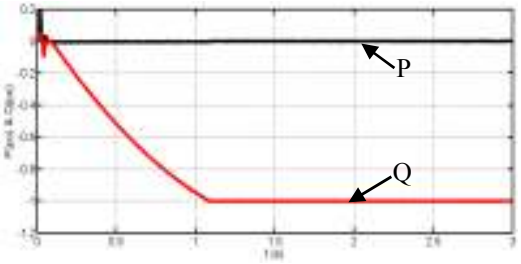
(d) Normalized output current

Figure 0.16: Simulation waveforms demonstrating operation of grid connected PV-inverter when controlled using THIPWM during rated power of 20MW, 0.8 power factor lagging.

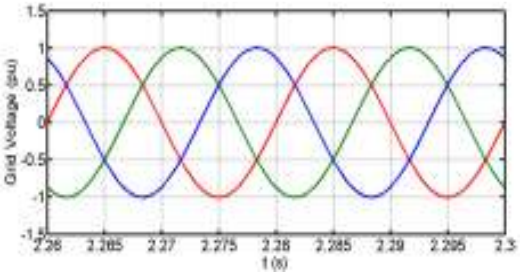
C. 15MVAr at zero power factor



(a) Variation of reactive current when PV operating at zero power factor



(b) Active and reactive power exchange with ac grid voltage



(c) Grid voltage

(d) Normalized output current

Figure 0.17: Simulation waveforms demonstrating operation of grid connected PV-inverter when controlled using THIPWM during rated power of 15MVAr, zero power factor lagging.

4.7. Experimental results of a low-loss grid-connected VSI

The experimental scaled-down test-rig results in this section aim to demonstrate the superiority of low switching frequency SHE over carrier based or space vector PWM strategies for grid connected two-level three phase VSIs. Third harmonic injection PWM is used as representative of high frequency carrier based and space vector PWM strategies. All the experimental results presented are based on parameters summarised in Table 4.5 and taken from the dSPACE1006 control desk.

Figure 4.18 and 4.19 summarises the practical implementation of the grid connected PV inverter using SHE and THIPWM. Modulation and control algorithms are implemented in dSPACE1006, which uses Matlab/Simulink and Real-Time Workshop as a front-end programming platform. The experimental results demonstrate the potential benefits of adopting SHE for PV inverters instead of commonly used carrier based PWM strategies in various grid mode conditions.

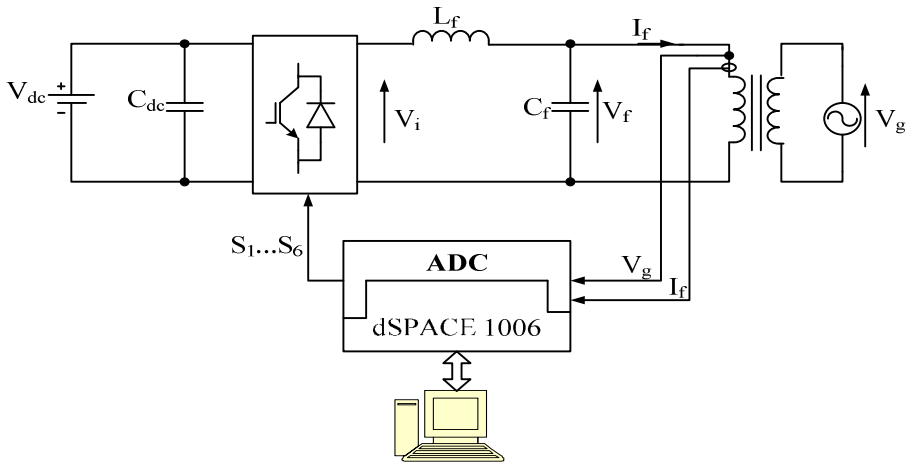


Figure 0.18: Hardware diagram of the test-rig

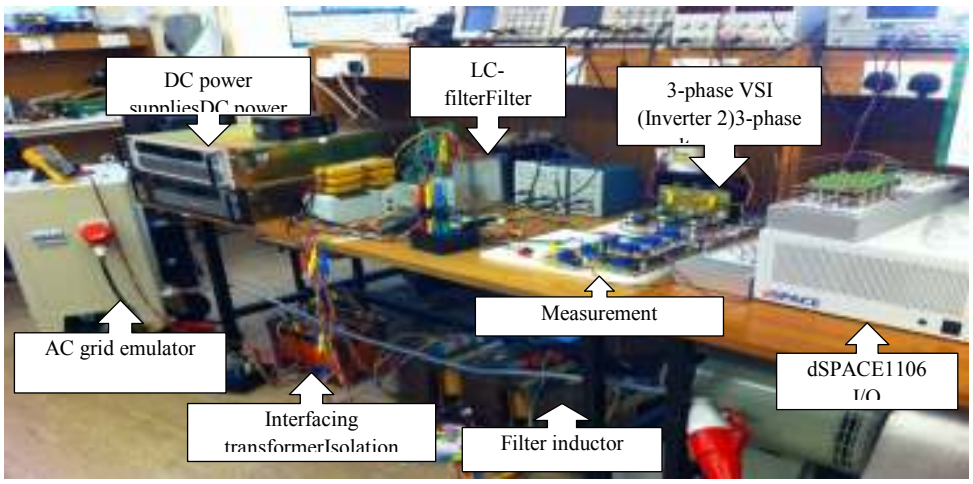


Figure 0.19: per-unit scaled-down test rig of a multi-megawatt PV inverter prototype.

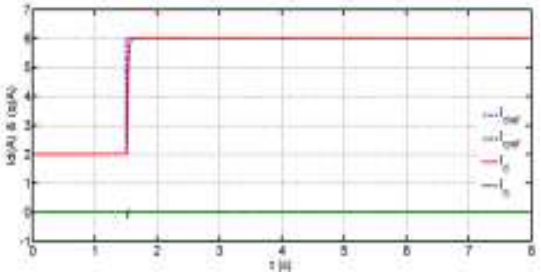
Table 0.5: Parameters of per-unit scaled-down test rig for prototype of megawatt PV inverter.

Parameter	THIPWM	SHE-PWM
Two-level converter rating (VA)	1200	1200
DC link voltage (V)	300	300
AC grid voltage per phase (V)	110	110
Active power capability (W)	1000	1000
Reactive power capability (VAr)	663	663
Interfacing inductor per phase (mH)	10	10
Filter capacitor (μF)	40	40
Grid frequency (Hz)	50	50
Switching frequency (kHz)	2	0.95
Proportional gain, K_P	4	120
Integral gain, K_I	1200	5000
Natural frequency, ω_n (rad/s)	346	707.1
Transformer turns ratio	1:1	1:1

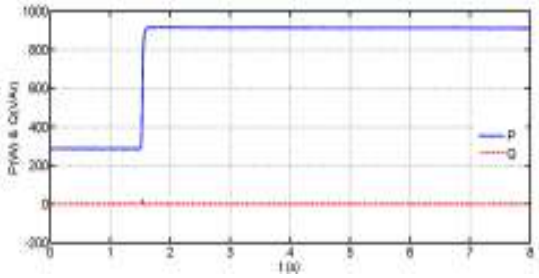
A. Step change in active power

Figure 0.20 illustrates the results when I_d is varied from 2A to 6A while I_q is zero in order to achieve unity power factor using sinusoidal PWM with triplen harmonic injection as the modulator. Figure 0.20(a) shows that the measured currents, I_d and I_q are able to track their respective reference currents with a short transient response time. In Figure 0.20(b), the active power demand exchanges from 300W to near rated power of 960W, with respect to the ac grid voltage. The quality of injected current into the grid in Figure 0.20(c) can be further improved by increasing the order of the ac power filter and increasing the witching frequency. Figure 0.20(d) presents an ac grid voltage where the measurement is taken at the filter bus (output) to the interfacing transformer. The in-

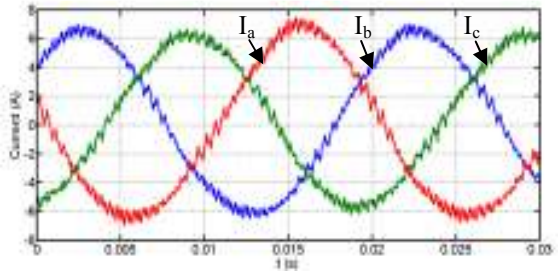
phase voltage and current waveforms in Figure 0.20(e) demonstrate unity power factor. In this application, the modulation index is varied from 0.85 to 0.95 following the variation of active and reactive currents when the PV inverter operates at full load.



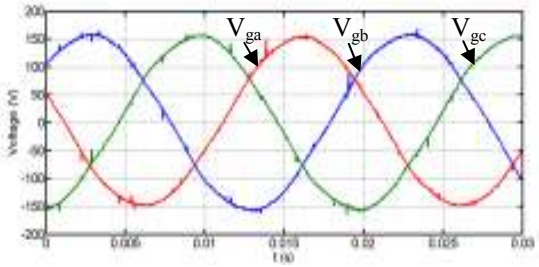
(a) Variation of active current components I_d when the PV inverter operates at full load



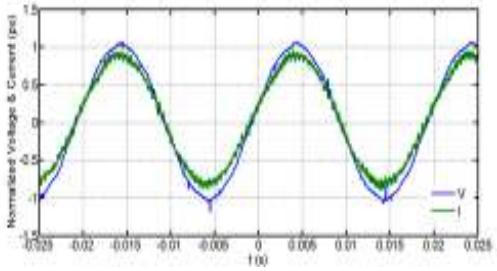
(b) Active and reactive power PV inverter exchanges with the grid measured at filter bus



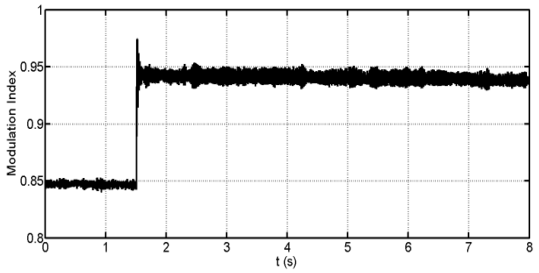
(c) Current waveforms when the PV inverter injects into grid



(d) Voltage waveforms the PV inverter presents to interfacing transfomer at the filter bus



(e) Normalized voltage and current at unity power factor

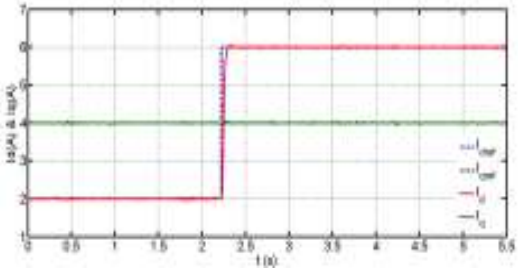


(f) Modulation index variation during active power change

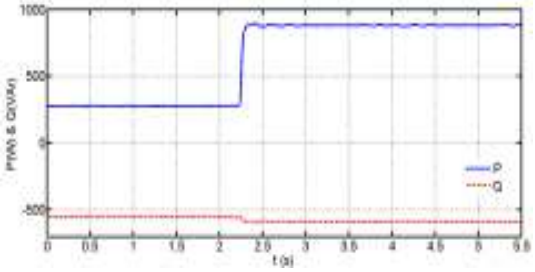
Figure 0.20: Waveforms demonstrating the operation of a PV inverter using sinusoidal PWM with triplen harmonic injection, when I_d is varied from 2A to 6A.

Figure 0.21 shows the experimental results when the grid connected inverter is controlled using SHE, with a reactive current component I_{qref}=4A, and a step change from 2A to 6A is applied to the active power current component I_{dref}. Figure 0.21(a) shows I_d and I_q are able to track their references when the inverter operates close to rated power, when SHE is used. Figure 0.21(b) shows active and reactive powers the inverter exchanges with the grid. Figure 0.21(c) and (d) show the good quality current

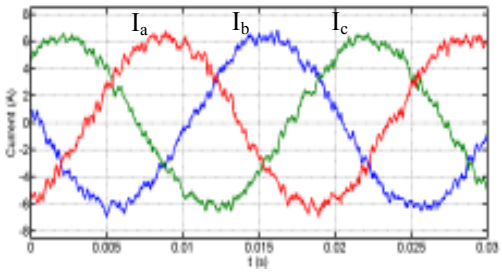
and voltage waveforms the inverter presents to the grid using SHE with a switching frequency of less than 1kHz. Figure 0.21(e) shows modulation index variation as I_{dref} is varied from 2A to 6A.



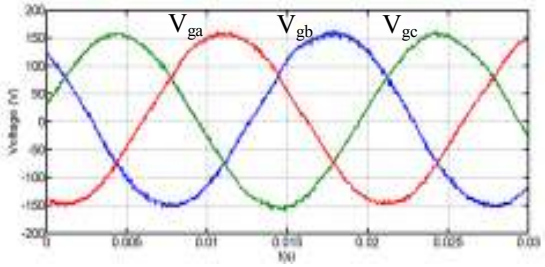
(a) Variation of active current component I_d from 2A to 6A when the PV inverter operates at near full load, exchanging considerable lagging reactive power with the grid



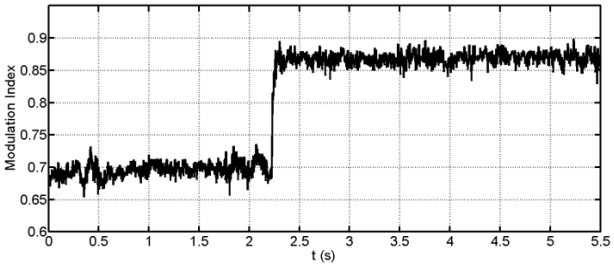
(b) The active and reactive power the PV inverter exchanges with the grid, measured at filter bus



(c) Current waveforms the PV inverter injects into grid at the filter bus



(d) Voltage waveforms the PV inverter presents to the interfacing transfomer at the filter bus

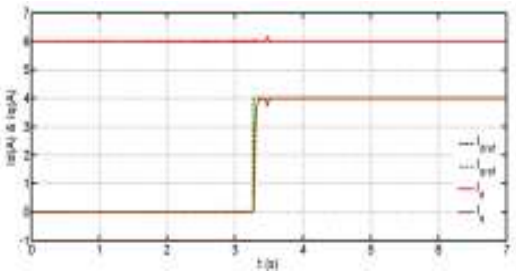


(e) Modulation index variation during active power change

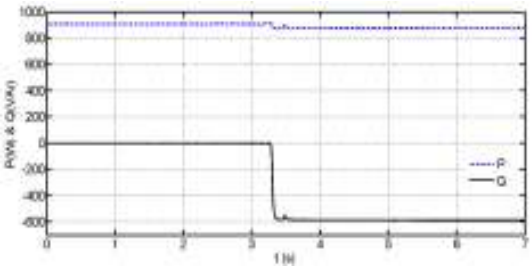
Figure 0.21: Experimental waveforms demonstrating operation of the grid connected inverter using SHE-PWM (step change in active power).

B. Step change in reactive power

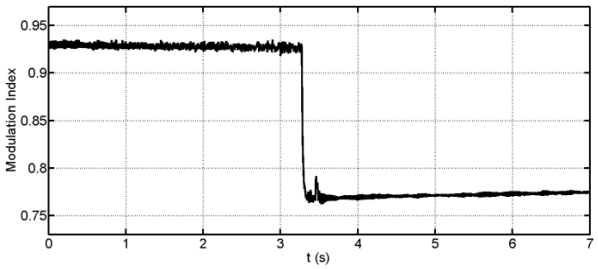
Similar results illustrating inverter operation when I_{qref} is varied from 0A to 4A and I_{dref} remains at 6A using THIPWM, are presented in Figure 0.22. The inverter is able to operate satisfactorily, with proper tracking of the set points as demonstrated in Figure 0.22(a). The active and reactive power exchanges with the ac grid voltage and variation of modulation index with respect to changes in reactive power are presented in Figure 0.22(b) and (c) respectively. Figure 0.23 shows the inverter operating results using SHE during variation of the reactive power.



(a) Variation of reactive current component I_q when the PV inverter operates at full load

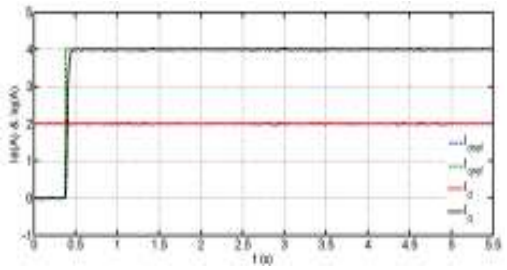


(b) Active and reactive power the PV inverter exchanges with the grid, measured at filter bus

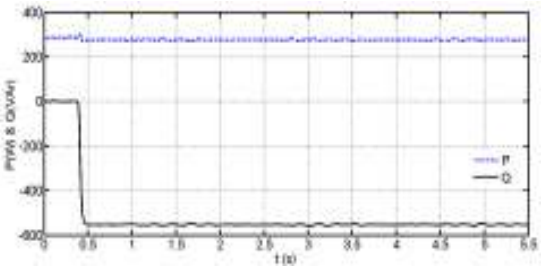


(c) Modulation index variation during reactive power change

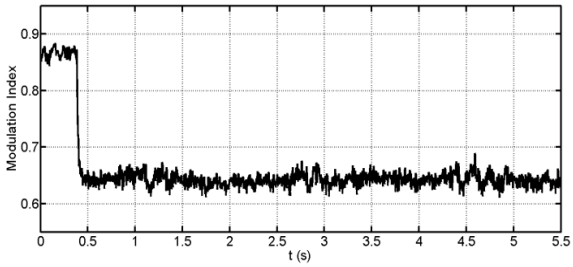
Figure 0.22: Experimental waveforms demonstrating PV inverter using sinusoidal PWM with triplen harmonic injection, when I_q is varied from 0 to 4A while I_d=2A.



(a) Variation of reactive current component, I_q varied from 0 to 4A while I_d= 2A



(b) Active and reactive power the PV inverter exchanges with the grid measured at filter bus during changes in I_q



(c) Modulation index variation, I_q changes from 0 to 4A

Figure 0.23: Experimental waveforms demonstrating operation of a grid connected inverter using SHE-PWM (step change in reactive power).

Figure 0.20 and 4.22 are for the case when the inverter is controlled using THI-PWM, with a 2kHz switching frequency, where I_{dref} is varied from 2A to 6A, and I_{qref} is varied from 0A to 4A. These results show the inverter under consideration stably exchanges active and reactive powers with the grid and presents high quality ac current and voltage waveforms at the point of common coupling (PCC). The output waveform quality in this case is similar to that obtained with SHE as demonstrated in Figure 0.21 and 4.23, despite THIPWM using a switching frequency approximately twice that used with SHE. Figure 0.20(f), 4.21(e), 4.22(c), and 4.23(c) confirm the variation of modulation index given in the generic phasor diagram for the voltage source converter in Figure 0.12(b), regarding increased modulation index margin for reactive power support.

Table 0.6 and 4.7 show the individual current and voltage harmonics for SHE and THI-PWM. Both modulation approaches are able to meet IEEE Standard 519-1922 and IEC 61000-3-6 for medium voltages [4.39, 40], and IEEE 1574 and IEC61727 for low voltage applications in terms of individual current and voltage harmonic limits. These results show SHE is able to meet strict harmonic requirements at the PCC, at a reduced switching frequency, such as 950Hz.

Table 0.8 and 4.9 present the switching device parameters used for the 1200VA pu scaled PV-inverter prototype and the estimated switching losses obtained for the two operating conditions. The switching losses are halved with SHE, compared to those with THIPWM. Based on these results it can be concluded that SHE can be considered for low loss large-scale PV inverters required for a sustainable low carbon economy as it is able to provide the flexibility of carrier based and space vector PWM strategies, including fast dynamic response at reduced losses. The SHE implementation for grid connected inverter is simple and exploits modern DSP floating point capabilities.

Table 0.6: Harmonic content in the experimental current for SHE-PWM and THI-PWM inverters.

		Harmonics (% of fundamental)								
Order of the harmonics		1st	5th	7th	11th	13th	17th	19th	23rd	25th
Current	SHE-PWM	100.00	0.3	0.3	0.2	0.15	0.01	0.1	0.03	0.01
	THI-PWM	100.00	0.35	0.38	0.16	0.19	0.02	0.09	0.06	0.02

Table 0.7: Harmonic content in the experimental voltage for SHE-PWM and THI-PWM inverters.

		Harmonics (% of fundamental)								
Order of the harmonics		1st	5th	7th	11th	13th	17th	19th	23rd	25th
Voltage	SHE-PWM	100.00	2.1	1.54	1.1	0.9	0.5	0.05	0.03	0.02
	THI-PWM	100.00	2	1.5	0.96	0.8	0.46	0.03	0.01	0.01

Table 0.8: Converter switching device data used for switching loss estimation, including turn-on, turn-off, and diode recovery losses, based on the IGBTIRG4PH50KDbF.

IGBT rating	1.2kV
K_1	0.44mJ/A
K_2	0

Table 0.9: Summary of switching losses with THIPWM and SHE modulation strategies for a 1200VA PV-inverter.

Operating condition	**P=878.6W and Q at 0.83 power factor lagging**	**P=913W at unity power factor**
SHE	18.1 W	15.04W
THI-PWM	38.1W	31.7W

4.8. Typical application of VSI for grid connection of PV arrays

This section presents a case study illustrating a typical VSI application for grid integration of PV arrays, when a maximum power tracking system is incorporated. In this mode, the inverter dc link voltage is adjusted as the weather changes in an attempt to ensure maximum power extraction. This has been simulated with the aid of a lookup table which contains a pre-defined PV *I-V* characteristic. Weather condition variation is simulated by variable current from the PV arrays, which is the assumed input signal to the lookup table. In this case study, the VSI dc voltage regulator is used to track the maximum power point (MPP), as previously described. For converter protection against over-current and to ensure sinusoidal output current, an inner current controller based on a synchronous reference frame PI controller is incorporated. Under this control mode, all the power generated by the PV will be injected into the ac grid, without creating active power imbalance between the inverter ac and dc sides [4.41-44]. Figure 0.24 summarises the typical control system of the PV inverter adopted in this chapter.

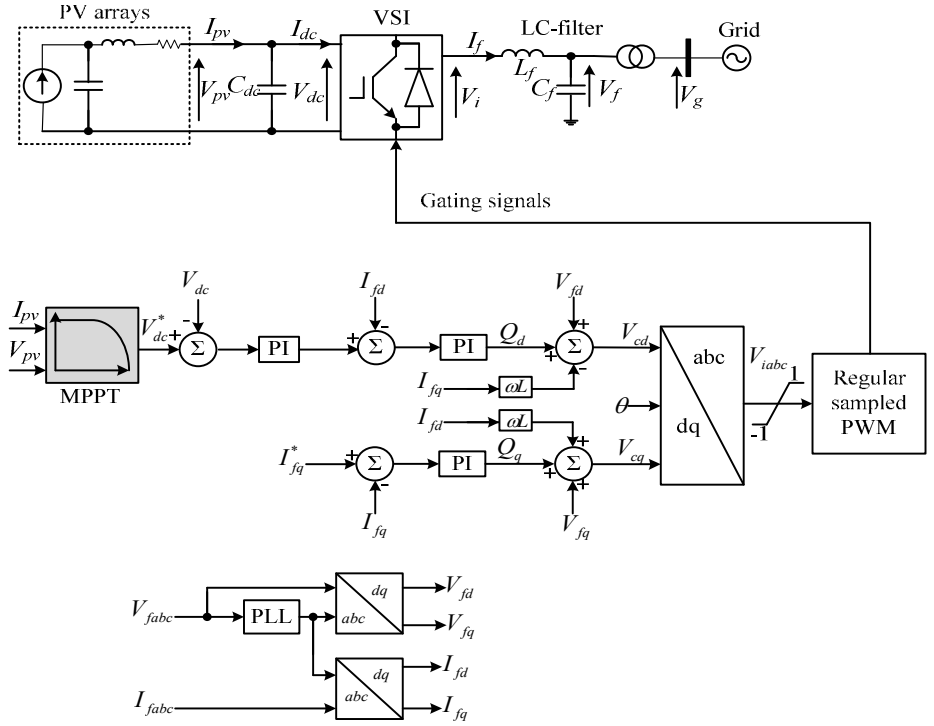
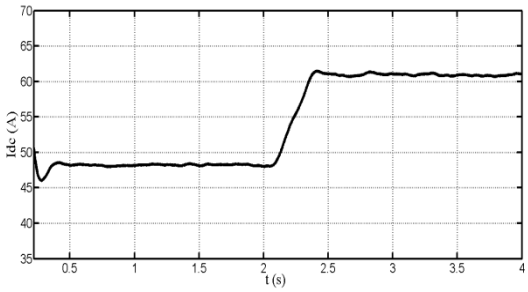


Figure 0.24: Schematic diagram representing the control structure which consists of a dc-link voltage regulator and an output current regulator.

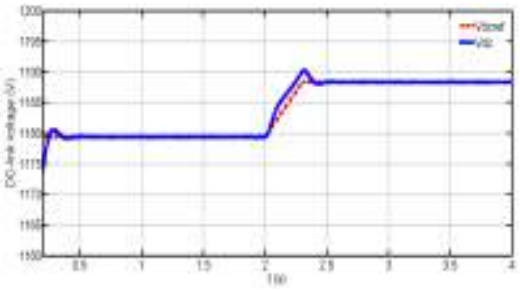
For performance demonstration of the grid-connected VSI under varying weather conditions, the test system shown in Figure 0.24 is simulated with the following parameters: the PV array is modelled as current source that varies its current injection (I_{pv}) with weather, and in this case I_{pv} is varied from 50A to 60A; dc-link capacitor=8mF; converter apparent rated power=100kVA; rated ac grid line voltage=380V; switching frequency=4kHz; and an LC-filter with 5mH and 40μF inductance and capacitance respectively.

Simulation results are displayed in Figure 0.25. The maximum power point tracker varies the inverter dc-link voltage from 1179V to 1188V as the PV array's output current I_{pv} varies with weather as shown in Figure 0.25 (a) and (b). A unity power factor is maintained by the VSI at the point of common coupling, as shown in Figure 0.25(d), independent of the PV operating point. The active and reactive powers the VSI exchanges with the grid are presented in Figure 0.25(e).

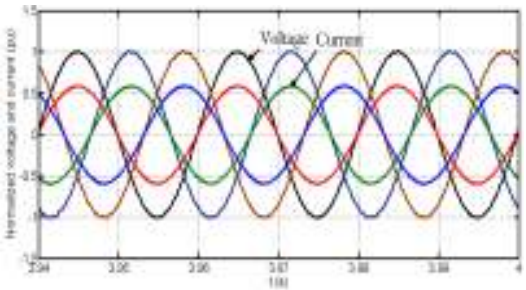
To further illustrate the possibility of the continual support to ac grid with low or no radiation from the sun, the PV array output power is reduced to near zero at t=1s while the VSI reactive power exchange with the ac grid is increased at t=2s. Results obtained are displayed in Figure 0.26. These results demonstrated that the PV inverter can inject active power into grid during the day and can operate as a typical static synchronous compensator during the night, providing reactive power support to the grid.



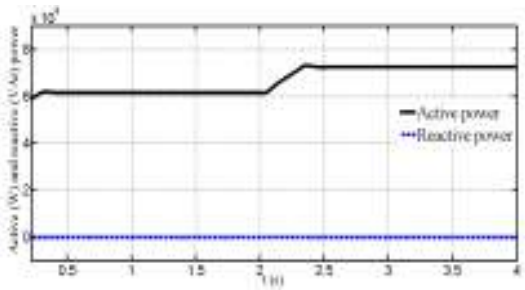
(a) dc-link current



(b) dc-link voltage with corresponding reference from MPPT

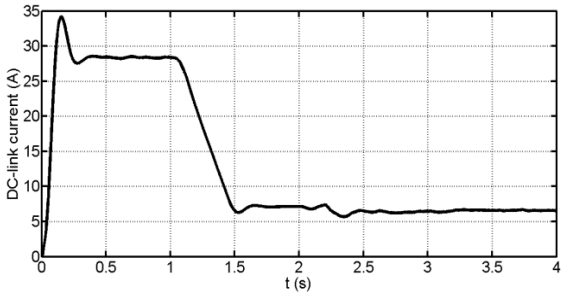


(c) Normalized grid voltage and current at unity power factor

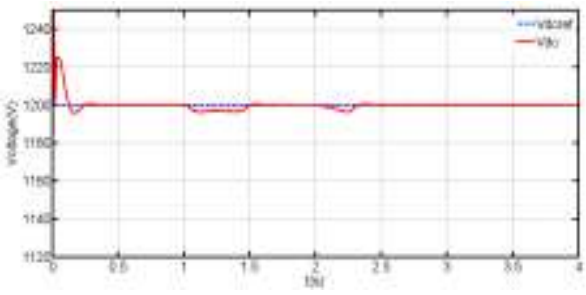


(d) Active and reactive power exchange with the ac grid (step change in active power)

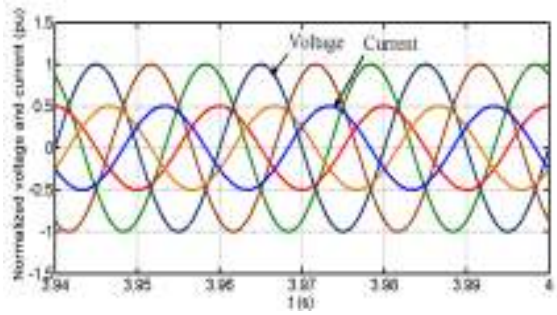
Figure 0.25: Simulation results of PV system behaviour in response to a step-change in PV arrays output current using three-phase voltage source inverter.



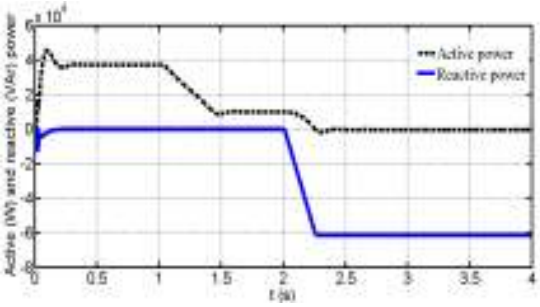
(a) dc-link current (I_{dc})



(b) dc-link voltage with respective reference from MPPT



(c) Normalized grid voltage and current at lagging power factor



(d) Active and reactive power exchange with the grid (step change in reactive power)

Figure 0.26: Simulation results showing the performance of the grid-connected photovoltaic VSI when there is low or no radiation from sun.

4.9. Summary

This chapter presents the analysis of the control systems used in a three-phase two-level VSI connected for island and grid mode operation. The discussed control systems are proportional-resonance (PR) and proportional-integral (PI) controllers. Proportional-integral (PI) control in the *dq*-frame was selected for further analysis, and itssuitability investigated for high-power medium-voltage grid connected inverters used as interfacing units for large-scale integration of renewable energy sources, when selective harmonic elimination is used. It has been demonstrated that the use of SHE does not compromise any grid connected inverter functionalites that are normally provided when controlled using carrier based PWM strategies. Additionally, this chapter established that contrary to traditional SHE implementation, adjustment of the 3rd harmonic magnitude leads to a universal solution for harmonic elimination equations that evolves switching angles that are better spread over 90^{o}. This feature can be used to simplify pratical realization of SHE at high modulation indices when a large number of harmonics are eliminated.The proposed system was verified in unity and lagging power

factor applications by simulation and experimentation. For completeness, an additional case study was presented that illustrates typical implementation of a PV inverter with maximum power point tracking.

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Chapter Five

Current Source Inverter for Photovoltaic Application

5.0. Introduction

This chapter discusses possible current source inverter (CSI) topologies worthy of attention for grid interfacing of photovoltaic systems. The suitable topologies are single-phase H-bridge, three-phase, and multilevel current source inverters are briefly discussed, taking into consideration the features suiting photovoltaic system requirements. A three-phase CSI is selected for grid integration in this thesis and further investigation in respect of the modulation strategies and control system are presented in this and subsequent chapters. Several modulation strategies, namely carrier-based sinusoidal PWM, selective harmonic elimination (SHE), space vector modulation, and twelve-step direct PWM, are discussed and compared to a new modulation technique termed direct regular-sampled pulse width modulation (DRSPWM). The theoretical basis of the proposed modulation technique is described in detail and includes dwell time calculations and switching sequence selection. The proposed DRSPWM technique is simple to implement digitally, and offers a degree of freedom and flexibility in switching sequence and pulse placement. The validity and suitability of the presented direct regular-sampled pulse width modulation technique is substantiated using simulations and experimentation.

5.1. Background

Though the voltage source inverter is the dominant topology in distributed generation (DG) applications, it has drawbacks such as short lifetime of the dc-link capacitor and inherent buck characteristics. Therefore, researchers and manufacturers continue their investigation into development of another efficient topology. The topology which has attracted considerable attention is the current source inverter due to its inherent boost

characteristics, longer lifetime of the energy storage unit, inherent fault protection capability, and direct control of the output current.

In photovoltaic applications, pulse width modulated CSIs are used for grid-interfacing between the photovoltaic system and ac main grid [5.1]. The current source option for PV grid interfacing has been advocated as a means of improving the effectiveness of maximum power point tracking (MPPT), as the number of series connected PV cells in each string is reduced [5.2, 3]. This reduces the impact of partial shading, and increases system efficiency by using one conversion stage instead of two stages, thereby benefiting from the voltage boost capability of the CSI [5.4-9]. Furthermore, PV system reliability is increased by replacing the shunt input electrolytic capacitor in the VSI with a series input inductor in the CSI.

5.2. Current source inverter topologies

This section presents current source inverter topologies being used in photovoltaic applications. The CSI has not been extensively investigated for grid-connected renewable energy systems. The CSI appears to be a feasible alternative to the VSI for grid connection of PV distributed generation, for the following reasons:

- The dc input current is continuous which is important for PV application.
- System reliability is increased by replacing the shunt input electrolytic capacitor with a series input inductor.
- The inherent CSI voltage boosting capability allows a low-voltage PV array to be grid interfaced without the need of a transformer or an additional boost stage.

5.2.1 Single-phase H-bridge current source inverter

A single-phase H-bridge current source inverter has four IGBT switches and four diodes, assigned as S_1 to S_4. Each diode is connected in series with an IGBT switch for reverse voltage blocking capability. A diagram of the single-phase H-bridge CSI topology is shown in Figure 0.1. A single-phase system has even harmonics on the dc side, which affect MPPT, reduce PV cell lifetime, and are associated with odd order

harmonics on the grid side [5.6, 10]. Therefore, eliminating the even harmonics on the dc side is essential when a single-phase H-bridge CSI is used.

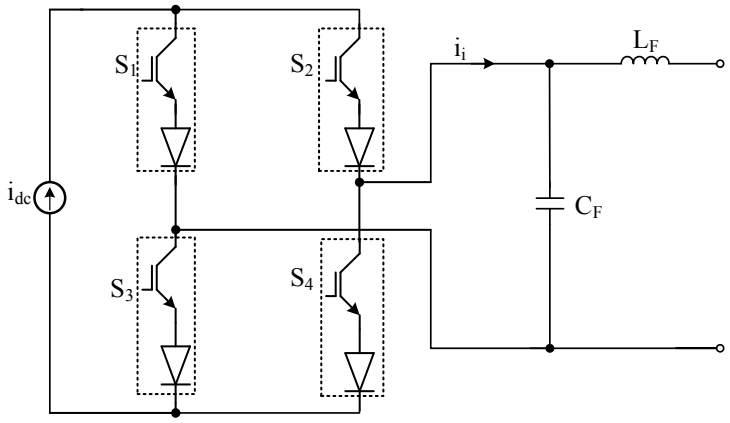


Figure 0.1: Topology of a single-phase H-bridge CSI.

Power fluctuation, caused by even harmonics on the dc-side in the single-phase single-stage PV application, affects the PV MPPT system, reduces PV lifetime, and reflects grid side 3rd harmonics[5.6, 10, 11].

5.2.2 Three-phase current source inverter

The three-phase CSI has six self-commutated unidirectional switches. The switches experience bipolar voltage stresses, with a maximum peak voltage equal to that of the ac output voltage. Similar to the single-phase H-bridge CSI, due to the low reverse voltage blocking capability of the IGBT, diodes have to be connected in-series with the switches. To eliminate the need for series diodes, symmetrical IGCTs may be an attractive alternative. The energy storage component at the dc-side is an inductor. The filter capacitor at the inverter output is used to attenuate high frequency harmonics associated with the modulation switching frequency. The CSI in Figure 0.2 generates three-level current output levels $\pm I_{dc}$ and 0. In each instant, one switch from the upper group (S_1, S_3 and S_5) and one from the lower group (S_4, S_6 and S_2) must be on. A zero current level at the output is achieved by turning on both switching devices in the phase leg. Unlike the single-phase system, the three-phase CSI does not contain even harmonics at the dc side or 3rd harmonics at the ac side of the system.

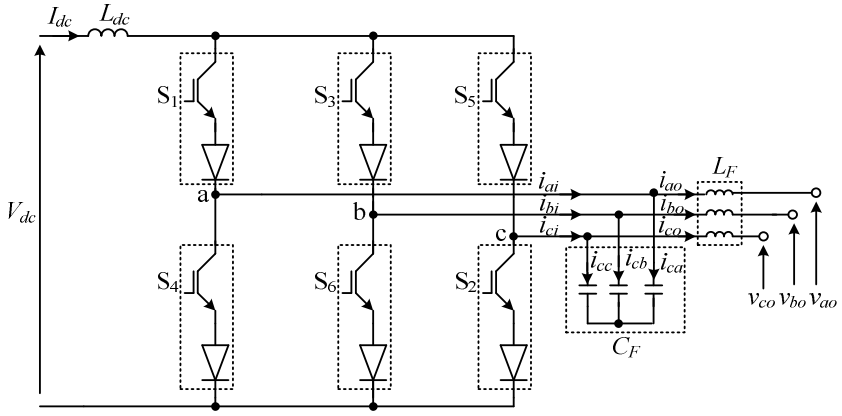


Figure 0.2: Topology of the two-level three-phase CSI.

5.2.3. Multilevel current source inverter

Multilevel current source inverters have gained attention in recent years and have been studied in high-voltage and high-power applications. By increasing the number of levels, the output currents in the case of a CSI are staircase current waveforms. With a large number of steps, the output current waveforms tend to sinusoidal waveforms, with a reduced THD and *di/dt*, and these can be achieved with a reduced switching frequency. Moreover, operation of a multilevel inverter at a low switching frequency results in lower switching loss and higher power transfer capability, compared to a standard three-phase inverter. For their advantageous features, multilevel CSIs have been adopted in distributed generation (DG) applications, particularly photovoltaic system.

Most of the multilevel CSIs reported in the literature are based on a single-phase cell [5.12-15], and are basically variations of the generalized multi-cell structure proposed in [5.16]. The generalized structured proposed in [5.17] has been extended to a three-phase topology in [5.13]. The topology proposed in [5.18] is a three-phase seven-level CSI that uses a phase-shifted trapezoidal PWM scheme for better harmonic performance with a low switching frequency. A modified three-phase multi-cell CSI topology proposed in [5.19] is different from the earlier proposed topologies in terms of the number of current levels. In [5.20], a three-phase multilevel CSI with 2(n+1) output current levels is introduced, with an associated closed-loop control strategy. Though a multilevel topology is able to overcome certain disadvantages of having single-stage CSIs, the advantages are achieved at the expense of a more complex PV system.

Furthermore, a bulky transformer and an electrolytic capacitor are required. Thus, the three-phase CSI is chosen for detailed analysis in a grid interfacing PV system while the H-bridge single phase and multilevel CSI are not discussed further in this chapter.

5.3. Modulation strategies for current source inverter

A number of pulse width modulation (PWM) strategies can be used to generate gating signals for three phase current source inverters, including those currently operational in grid mode. Examples of PWM strategies used to control a three-phase CSI are selective harmonic elimination (SHE) [5.21-29], carrier-based sinusoidal pulse width modulation (CSPWM) [5.15, 30], and space vector modulation (SVM) [5.31-44]. Two switching constraints must always be met to properly gate the power switches of the CSI. These are:

- The ac-side is mainly capacitive therefore it must not be short-circuited. This implies that at most one upper switch (S_1, S_3 and S_5) or one lower switch (S_4, S_6 and S_2) should be closed at any instant.
- The dc bus is a current-source type, therefore cannot become open-circuit and at least one top switch (S_1, S_3 and S_5) and one lower switch (S_4, S_6 and S_2) must be closed at every instant.

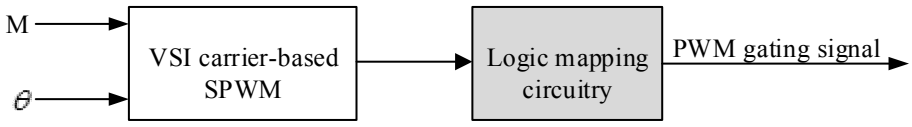
5.3.1. Carrier-based sinusoidal pulse width modulation

Carrier-based SPWM is simple to implement in a VSI and can be realized with a relatively low switching frequency. However, implementation of CSI carrier-based SPWM is not as straightforward as for the VSI case. The common approach used for the implementation of CSI carrier-based SPWM is to modify the gating signals of the VSI PWM using logic mapping circuitry as shown in Figure 0.3(a) [5.15, 30, 45]. Referring to Figure 0.3(b), the reference modulating signals (v_{ma}, v_{mb} and v_{mc}) are compared to high frequency carrier signals (v_{cr}), and with logic mapping circuitry, generate the CSI gating signals (S_1 to S_6) as illustrated in Figure 0.4(a). A sample of pre-filter inverter current (i_{ai}), and three-phase load current and voltage are shown in Figure 0.4(b) to (d) respectively.

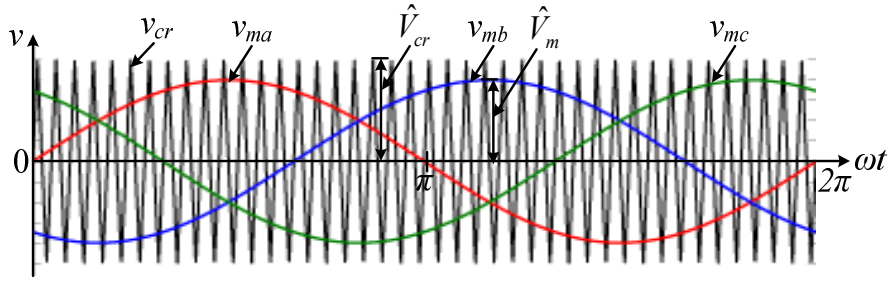
The fundamental inverter current magnitude, I_m in relation to the amplitude modulation index, m_a, for carrier-based SPWM, can be expressed as:

$$m_a = \frac{I_m}{I_{dc}} \tag{5.1}$$

Since the maximum achievable fundamental current magnitude with carrier-based SPWM is only $I_{m,\max} = m_a \frac{\sqrt{3}}{2} I_{dc} = 0.866 I_{dc}$ for m_a=1, carrier-based SPWM suffers from poor dc link current utilization. Furthermore, the use of logic mapping circuitry increases modulator complexity, and leads to suboptimal switching sequences from the switching loss viewpoint.

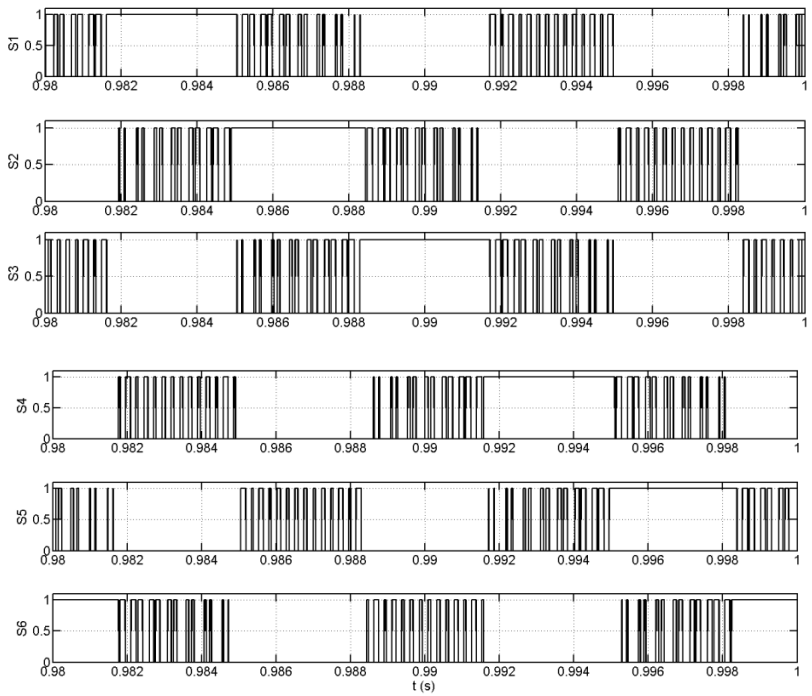


(a) Diagram of CSPWM gating signal generation

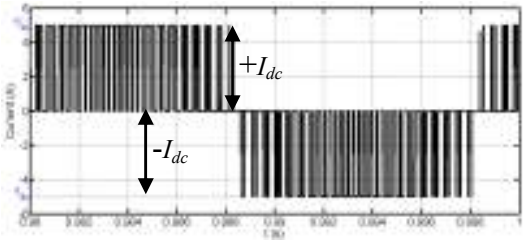


(b) Three phase reference and high-frequency carrier signals of VSI carrier-based SPWM before passing through logic mapping circuitry to generate CSI gating signals

Figure 0.3: Modulation process of the CSI using carrier-based SPWM

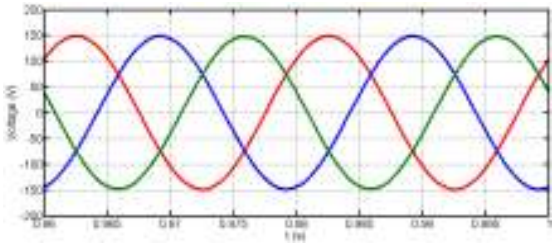


(a) CSI switching sequences of S_1 to S_6



(b) Inverter current, I_{ai} before ac filter

(c) Three phase load current (i_{ao}, i_{bo} and i_{co})



(d) Three phase load voltage (v_{ao}, v_{bo} and v_{co})

Figure 0.4: Sample CSI open-loop simulation waveforms using SPWM

5.3.2 Selective harmonic elimination

Generally, selective harmonic elimination is favoured over space vector and carrier based pulse width modulation in high-power medium-voltage CSI applications [5.28, 29]. This is due to its ability to synthesize high quality output current and voltage by

eliminating a number of pre-defined low-order harmonics, without a significant increase in switching frequency. There are two possible SHE implementations that can be used to generate gating signals for a CSI, as shown in Figure 0.5(a). One possible way is by direct calculation of the switching angles based on a pre-determined inverter phase current pattern to eliminate specific harmonics. An example of an inverter current waveform, i_i using SHE with two switching angles or notches over a ½πperiod to eliminate the 5th and 7th harmonics, is illustrated in Figure 0.5(b). The Fourier series expansion of the symmetric PWM waveform can be expressed as:

$$I_i(\omega t) = \sum_{n=1,3,5,..}^{\infty} \frac{4I_{dc}}{n\pi}\left(\cos(n\alpha_1) - \cos(n\alpha_2)... + \cos(n\alpha_n)\right)\sin(n\omega t) \qquad (5.2)$$

where n is the order of the harmonic and α_n is the n^{th} switching angle.

Based on(5.2), the following group of polynomial equations can be utilised to calculate n switching angles and realize the selective harmonic elimination of up to the m^{th} order:

$$\begin{aligned}
&\frac{4I_{dc}}{\pi}\left(\cos(\alpha_1) - \cos(\alpha_2)... + \cos(\alpha_n)\right) = I_i \\
&\cos(5\alpha_1) - \cos(5\alpha_2)... + \cos(5\alpha_n) = 0 \\
&\cos(7\alpha_1) - \cos(7\alpha_2)... + \cos(7\alpha_n) = 0 \qquad (5.3) \\
&... \\
&\cos(m\alpha_1) - \cos(m\alpha_2)... + \cos(m\alpha_n) = 0
\end{aligned}$$

In this equation group, the first equation is used to establish the magnitude of the fundamental component (I_i) and the other equations are utilised to ensure the elimination of the selected harmonics. Thus, by calculating the n switching angles, n-1 harmonics can be eliminated [5.24, 46, 47].

Alternatively, SHE can be realised by adapting the approaches presented in [5.21] and [5.25] that modify the chopping angles of a VSI using logic mapping circuitry to generate the gating signals for the CSI. The Fourier series expansion and related nonlinear equations for a VSI were discussed in chapter three.

The main disadvantage of SHE is that the output current waveform quality deteriorates as the modulation index decreases. This problem can be avoided at the expense of increased switching loss by increasing the number of notches per quarter fundamental cycle as the modulation decreases [5.22-24]. Another limitation of SHE is it does not ensure complete elimination of the selected harmonics over the full modulation index

linear range as the windows between adjacent switching angles tend to be small at low and high modulation indices, which is difficult to realise practically.

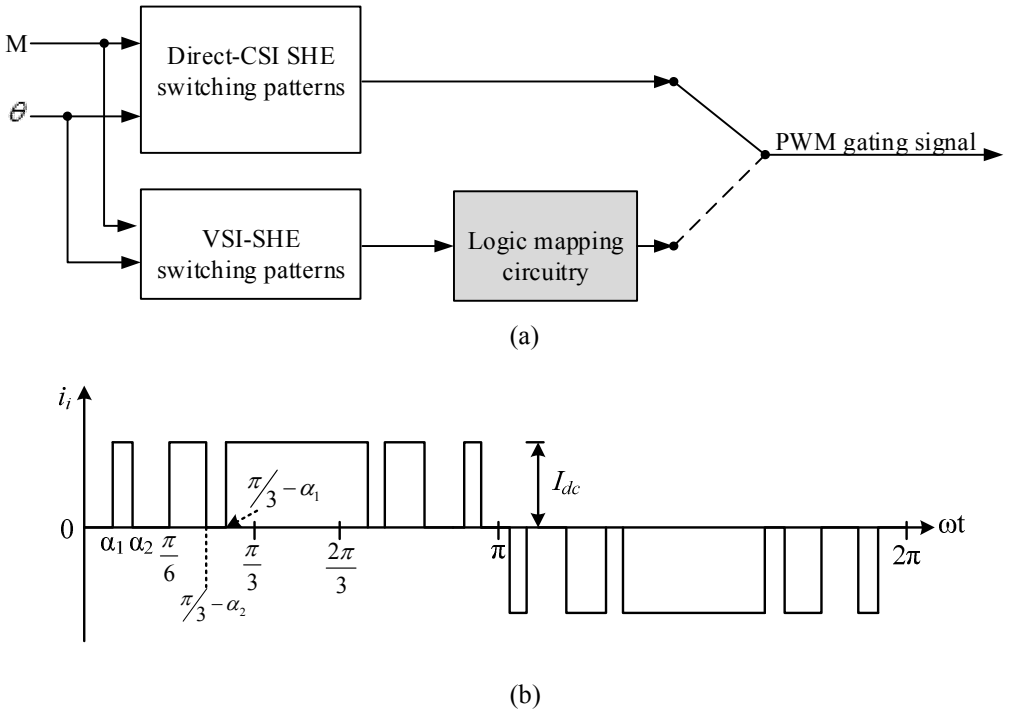


Figure 0.5: (a) Diagram of possible PWM gating signal generation using selective harmonic elimination and (b) typical inverter current waveform (i_i) relative to dc-link current ($\pm I_{dc}$).

5.4. Direct CSI space vector modulation

A version of space vector modulation that is specific to the CSI is shown in Figure 0.6, and is derived from transformation of the inverter phase currents into the *α-β* reference frame using Clark Transform, based on similar assumptions to those used for the VSI [5.35, 36]. This approach offers a higher degree of freedom and flexibility in terms of pulse placement and switching sequence selection.

To satisfy CSI switching constraints, there are nine switching states: three zero states and six active states, as listed in Table 0.1. One zero state [14] represents S_1 and S_4 in phase leg '*a*' being simultaneously on while the other four switches are off. The dc-link current bypasses the outputs, specifically $i_{ai}=i_{bi}=i_{ci}=0$. The active state [61] represents S_6 in phase leg '*b*' and S_1 in phase leg '*a*', being on. The dc-link current flow through S_6, the load, S_1, and then back to dc source resulting in $i_{ai}=I_{dc}$ and $i_{bi}=-I_{dc}$.

Table 0.1: Switch states and space vector.

State type	Switch state	On-switch state	Inverter current			Space vector
			i_{ai}	i_{bi}	i_{ci}	
Zero states	[14]	S_1, S_4	0	0	0	$\vec{I}_0$
	[36]	S_3, S_6				
	[52]	S_5, S_2				
Active states	[61]	S_6, S_1	I_{dc}	$-I_{dc}$	0	$\vec{I}_1$
	[12]	S_1, S_2	I_{dc}	0	$-I_{dc}$	$\vec{I}_2$
	[23]	S_2, S_3	0	I_{dc}	$-I_{dc}$	$\vec{I}_3$
	[34]	S_3, S_4	$-I_{dc}$	I_{dc}	0	$\vec{I}_4$
	[45]	S_4, S_5	$-I_{dc}$	0	I_{dc}	$\vec{I}_5$
	[56]	S_5, S_6	0	$-I_{dc}$	I_{dc}	$\vec{I}_6$

The space vector diagram for direct-CSI SVM is shown in Figure 0.6 where $\vec{I}_1$ to $\vec{I}_6$ are the active vectors and $\vec{I}_0$ is a zero vector located at the centre of the hexagon. As mentioned, using the Clark transformation, the inverter phase current is transformed to α-β reference:

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_{ai}(t) \\ i_{bi}(t) \\ i_{ci}(t) \end{bmatrix} \tag{5.4}$$

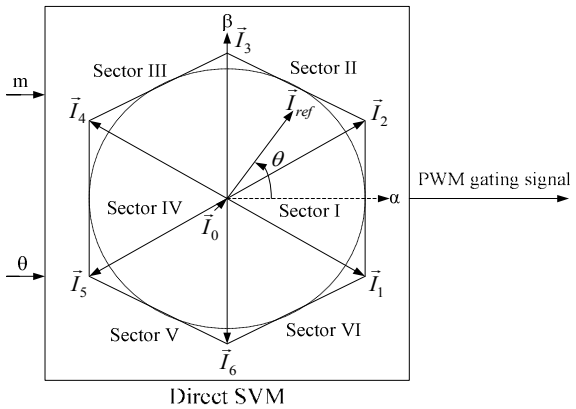


Figure 0.6: Diagram of PWM gating signal generation using direct SVM.

During one switch period T_s, PWM modulation can be summarized as:

$$\begin{aligned} \vec{I}_{ref} T_s &= \vec{I}_i T_1 + \vec{I}_{i+1} T_2 + \vec{I}_0 T_0 \\ T_s &= T_1 + T_2 + T_0 \end{aligned} \tag{5.5}$$

where T_1, T_2 and T_0 are the dwell times of the chosen switches and i= 0,1,2,...,6. The i value depends on the sector that $\vec{I}_{ref}$ lies in. An example of $\vec{I}_{ref}$ falling in sector I and synthesized by $\vec{I}_1$, $\vec{I}_2$ and $\vec{I}_0$ is illustrated in Figure 0.7.

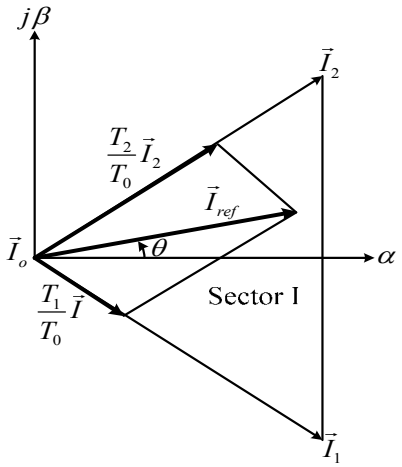


Figure 0.7: Synthesis of $\vec{I}_{ref}$ by $\vec{I}_1$, $\vec{I}_2$ and $\vec{I}_0$.

Equation (5.5) becomes

$$\begin{aligned} \vec{I}_{ref} T_s &= \vec{I}_1 T_1 + \vec{I}_2 T_2 + \vec{I}_0 T_0 \\ T_s &= T_1 + T_2 + T_0 \end{aligned} \tag{5.6}$$

$$\vec{I}_{ref} = I_{ref} e^{j\theta}, \vec{I}_1 = \tfrac{2}{\sqrt{3}} I_{dc} e^{-j\frac{\pi}{6}}, \vec{I}_2 = \tfrac{2}{\sqrt{3}} I_{dc} e^{j\frac{\pi}{6}} \text{ and } \vec{I}_0 = 0 \tag{5.7}$$

Substituting (5.7) into (5.6) yields dwell times (T_1, T_2 and T_0) for sector I as:

$$\begin{aligned} T_1 &= m_a \sin\left(\tfrac{\pi}{6} - \theta\right) T_s \\ T_2 &= m_a \sin\left(\tfrac{\pi}{6} + \theta\right) T_s \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{5.8}$$

where m_a is the modulation index given by $m_a = \frac{I_{ref}}{I_{dc}} = \frac{I_i}{I_{dc}}$ and I_i is the peak of fundamental component in i_i.

The selection of a zero vector sequence must ensure minimum switch transitions while maintaining switch utilization and losses. Table 0.2 lists zero vector sequences to satisfy the mentioned criterion.

Table 0.2: Selection of zero vector sequence in sector I to VI.

Sector	Initial state	Final state	Zero state
	I_i	I_{i+1}	I_z
I	$\vec{I}_1$=S$_1$, S$_2$	$\vec{I}_2$= S$_2$, S$_3$	$\vec{I}_0$= S$_5$, S$_2$
II	$\vec{I}_2$= S$_2$, S$_3$	$\vec{I}_3$= S$_3$, S$_4$	$\vec{I}_0$= S$_3$, S$_6$
III	$\vec{I}_3$= S$_3$, S$_4$	$\vec{I}_4$= S$_4$, S$_5$	$\vec{I}_0$= S$_1$, S$_4$
IV	$\vec{I}_4$= S$_4$, S$_5$	$\vec{I}_5$= S$_5$, S$_6$	$\vec{I}_0$= S$_5$, S$_2$
V	$\vec{I}_5$= S$_5$, S$_6$	$\vec{I}_6$= S$_6$, S$_1$	$\vec{I}_0$= S$_3$, S$_6$
VI	$\vec{I}_6$= S$_6$, S$_1$	$\vec{I}_1$= S$_1$, S$_2$	$\vec{I}_0$= S$_1$, S$_4$

The simulation results of gating signal generation (S_1 to S_6) with the associated sectors and phase '*a*' inverter current (i_{ai}) relative to I_{dc} for a three-phase CSI are presented in Figure 0.8. Direct-SVM is used in accordance with the switching sequence in Table 0.2, with modulation index of 0.8, I_{dc}=8A and switching frequency, f_{sw}=2.1kHz.

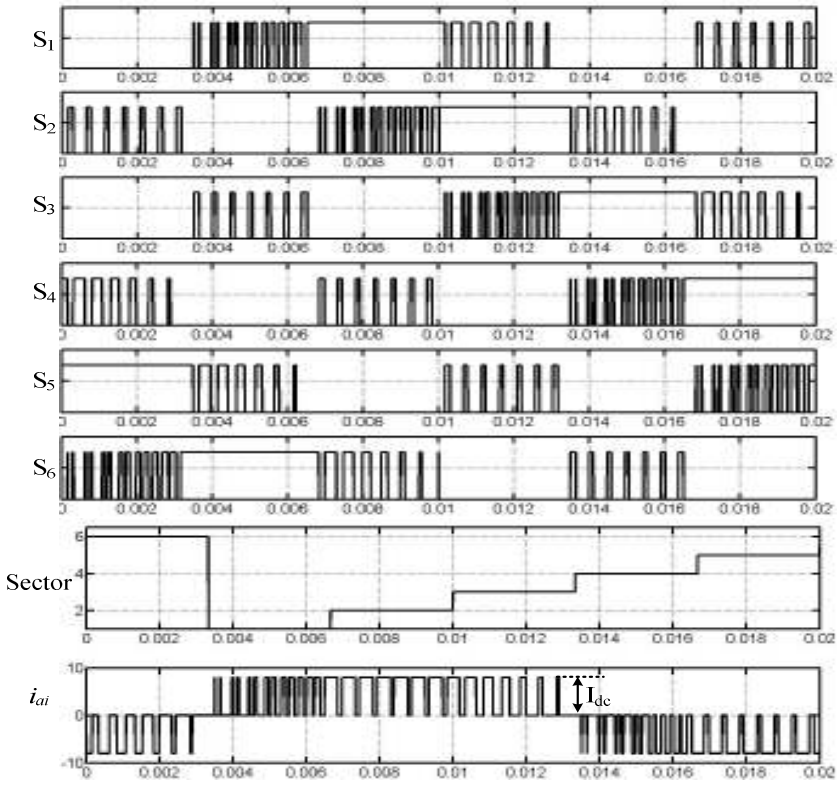


Figure 0.8: SVM switching sequence of a CSI over a fundamental cycle.

5.4.1. VSI-space vector modulation with logic mapping circuitry

The alternative approach, shown in Figure 0.9, is to use VSI space vector modulation to generate the gating signals which are then modified using logic mapping circuitry to suit the CSI [5.31, 32, 34]. The PWM modulation of VSI-SVM for a CSI is discussed in chapter three. The angles between the active space vectors for both the VSI and CSI are 60^o, however the CSI active vectors lead the VSI case by 30^o. This is one of disadvantages to be taken into account: a 30^o phase shift in output current compared to that of the VSI. The approach suffers from the same disadvantages as the CSPWM method when using logic mapping circuitry.

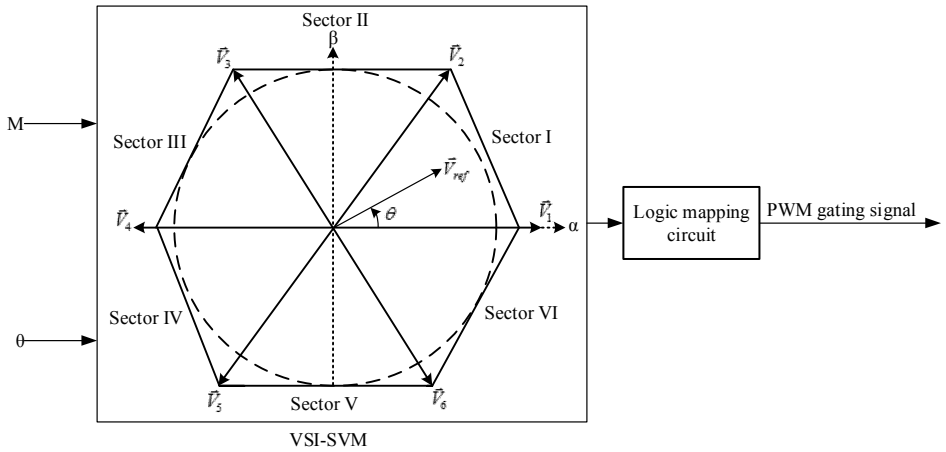


Figure 0.9: Diagram of VSI-SVM with logic mapping circuit used to generate CSI gating signals.

Both CSI SVM implementations are suitable for applications that use a relatively high switching frequency. In addition to the SVM discussion, there are several new SVM implementations aimed at achieving different objectives [5.33, 37, 38]. SVM is suited for digital implementation and real-time generation of the gating signals with different patterns, and offers the advantages of faster dynamics, controllability, and flexibility. The use of low switching frequency SVM may however, lead to the appearance low-order harmonics in the baseband [5.43]. In particular, the low-order harmonics, such as the 5^{th} and 7^{th}, may be close to the resonant frequency of the CSI output LC filter, which may excite LC resonance. Some attempts to exploit different SVM switching sequences and manipulate dwell times to minimize the magnitudes of the CSI 5^{th} and 7^{th} harmonics, have been achieved with relatively low switching frequency SVM [5.39-42, 44].

5.5. Twelve-Step Direct Pulse Width Modulation (TS-PWM)

In [5.48], a CSI PWM scheme is proposed that offers natural soft commutation, and a 50% reduced CSPWM switching frequency. The PWM scheme exploits the natural commutation in the Graetz converter to achieve natural commutation and low switching losses by using the grid voltages as modulating signals. However, the use of these reference compromises the basic features that make PWM CSIs competitive with respect to the VSI, such as black-start capability, and operation independent of the network short circuit ratio. In other words, such a scheme in its present form cannot be used to power a dead ac network that has no live ac voltage.

5.6. Proposed direct-regular sampled pulse width modulation

Because of the discussion on CSI modulation techniques, this thesis proposes a direct regular-sampled pulse width modulation (DRSPWM) technique that aims to simplify the CSI modulation process. The modulation strategy is suited for digital implementation and offers the flexibility of SVM in terms of pulse placement and switch sequence selection. The proposed modulation strategy exploits a combination of forced and natural commutation imposed by the co-existence of an insulated gate bi-polar transistor (IGBT) in series with a diode used in the CSI in Figure 0.2, to determine device dwell times and switching sequences.

5.6.1. Theoretical basis of the proposed DRSPWM

Figure 0.10 depicts a fundamental cycle of the target modulating signals divided into six sectors, designated I to VI. During the first sector, switches S_1 and S_5 operate alternatively with S_6 in order to synthesize non-zero output currents in the inverter phases. A zero current in the inverter output is achieved by selecting one of the following combinations: $S_1$and S_4 (1001000), S_3 and S_6 (001001), or S_5 and S_2 (010010). The CSI switch states in Figure 0.10 are expressed by $\prod_{j=1}^{6} S_j$, where S_j=1 and 0 represents the ‘ON’ and ‘OFF’ states respectively of switch S_j. The dwell time calculations for the respective sectors are listed in Table 0.3.

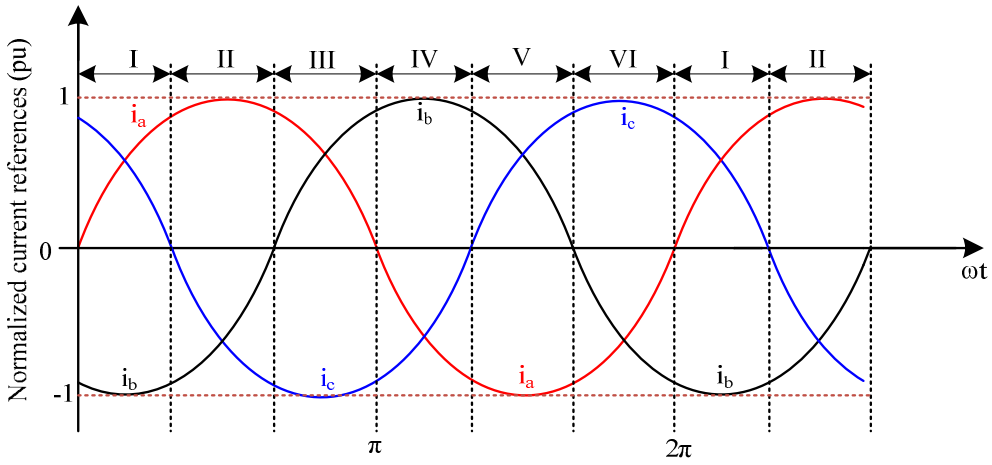


Figure 0.10: Reference modulating signal.

Table 0.3: Dwell times calculations for all sequences and sections identification.

Sector	Dwell times	Sector identification	Sector	Dwell times	Sector identification
I	$t_{000011} = m_a T_s \sin \omega t$ $t_{100001} = m_a T_s \sin(\omega t + \frac{2}{3}\pi)$ $t_{001001} = T_s - t_{000011} - t_{100001}$	$I_a > 0$ and $I_c > 0$	IV	$t_{011000} = -m_a T_s \sin(\omega t + \frac{2}{3}\pi)$ $t_{001100} = -m_a T_s \sin \omega t$ $t_{001001} = T_s - t_{011000} - t_{001100}$	$I_c < 0$ and $I_a < 0$
II	$t_{100001} = -m_a T_s \sin(\omega t + \frac{4}{3}\pi)$ $t_{110000} = -m_a T_s \sin(\omega t + \frac{2}{3}\pi)$ $t_{100100} = T_s - t_{100001} - t_{110000}$	$I_b < 0$ and $I_c < 0$	V	$t_{001100} = m_a T_s \sin(\omega t + \frac{4}{3}\pi)$ $t_{000110} = m_a T_s \sin(\omega t + \frac{2}{3}\pi)$ $t_{100100} = T_s - t_{001100} - t_{000110}$	$I_c > 0$ and $I_b > 0$
III	$t_{110000} = m_a T_s \sin \omega t$ $t_{011000} = m_a T_s \sin(\omega t + \frac{2}{3}\pi)$ $t_{010010} = T_s - t_{110000} - t_{011000}$	$I_b > 0$ and $I_a > 0$	VI	$t_{000110} = -m_a T_s \sin \omega t$ $t_{000011} = -m_a T_s \sin(\omega t + \frac{4}{3}\pi)$ $t_{010010} = T_s - t_{000110} - t_{000011}$	$I_b < 0$ and $I_a < 0$

Given $i_a + i_c = -i_b$ in a three-phase system, and assuming that within each switching cycle the dwell time associated with each active switch state is proportional to the phase current magnitude, then the dwell times associated with active states I-(ii) and I-(i) in first sector are:

$$I_{dc} \times t_{100001} = T_s \times i_a$$
$$I_{dc} \times t_{000011} = T_s \times i_c \qquad (5.9)$$

If the phase currents are expressed by: $i_a = I_m \sin(\omega t + \delta)$, $i_b = I_m \sin(\omega t + \delta + \frac{4}{3}\pi)$ and $i_c = I_m \sin(\omega t + \delta + \frac{2}{3}\pi)$, then the dwell times t_{100001} and t_{000011} can be expressed by[5.49]:

$$t_{100001} = m_a T_s \sin(\omega t + \delta)$$
$$t_{000011} = m_a T_s \sin(\omega t + \delta + \tfrac{2}{3}\pi) \quad (5.10)$$

where m_a is modulation index,

I_m is peak phase current, A;

T_s is switching period, s;

ω is supply frequency, rad/s; and

δ is the load angle, rad.

The amplitude modulation index, m_a is defined as:

$$m_a = \frac{I_m}{I_{dc}} \quad (5.11)$$

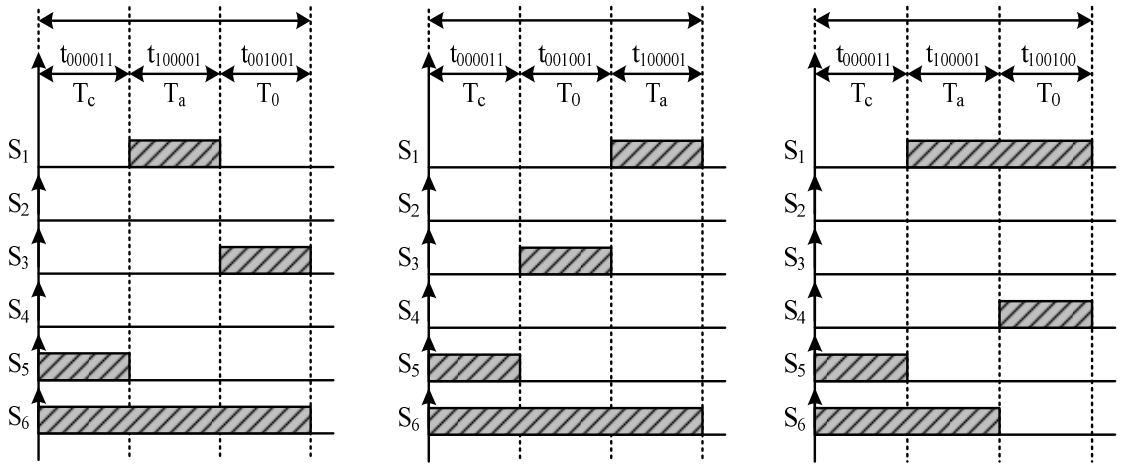
where $0 \le m_a \le 1$, and $m_f = \frac{f_{sw}}{f_o}$ is the ratio of switching frequency f_{sw} to fundamental frequency f_o.

The dwell time associated with a zero state is given by:

$$t_0 = T_s - t_{100001} - t_{000011} \quad (5.12)$$

There are several switching sequences that can be realized in each sector with the aim to minimize the number of switching transitions, including soft transitions between successive sectors. Table 5.4 lists all the possible switching sequences realizable over the full fundamental cycle. Figure 0.11 (a) to (c) show an example of the pulse placements for the switch sequences I, II and III in the first sector. Based on Figure 0.11 and Table 5.4, the switch sequences I and II operate the CSI as with typical VSI dead-band modulation [5.50] that suspends each inverter phase for 120°, and hence low switching loss is achieved. For example, for $30^o \le \omega t \le 150^o$ phase '*a*' is clamped to the positive rail by maintaining switch S_1 in the on-state, while switches S_2 and S_6 are switched on and off to synthesize the currents in phases *b* and *c*. During the periods when S_2 and S_6 alternatively operate, S_1 contributes to generate non-zero current in all the phases. With sequences I and II the switch states used to produce zero current in each phase change every 60°: for example, S_1 and S_4 correspond to 000101 in sector II for $60^o \le \omega t \le 120^o$.

For sequence III switching, the CSI phases over the entire fundamental period are observed in Figure 0.11(c). In this sequence, the switching frequency per device and switching loss are increased. In sequence III, the switch states that produce zero output phase currents are selected to avoid any one switch operating for the full sampling period, as shown in Figure 0.11(c). Period t_0, calculated using (5.12), is assigned to the dwell times of the zero switch states, for example, $t_{001001}=t_0$ in the first sector as shown in Table 5.4. The selection and placement of the zero switch state directly affects inverter switching loss and switching frequency per device. Sequences I and III can be realized by placing the switch states that produce zero current at the right or left, aligned within each switching cycle. Sequence III does not result in gating signals with 100 percent duty cycles, therefore it is suitable for low cost digital signal processor (DSPs) or microcontroller implementation. On this basis, the dwell times and switching sequences for the remaining sectors are determined.



(a) Sequence I (b) Sequence II (c) Sequence III

Figure 0.11: Examples of the possible switch sequences in sector I.

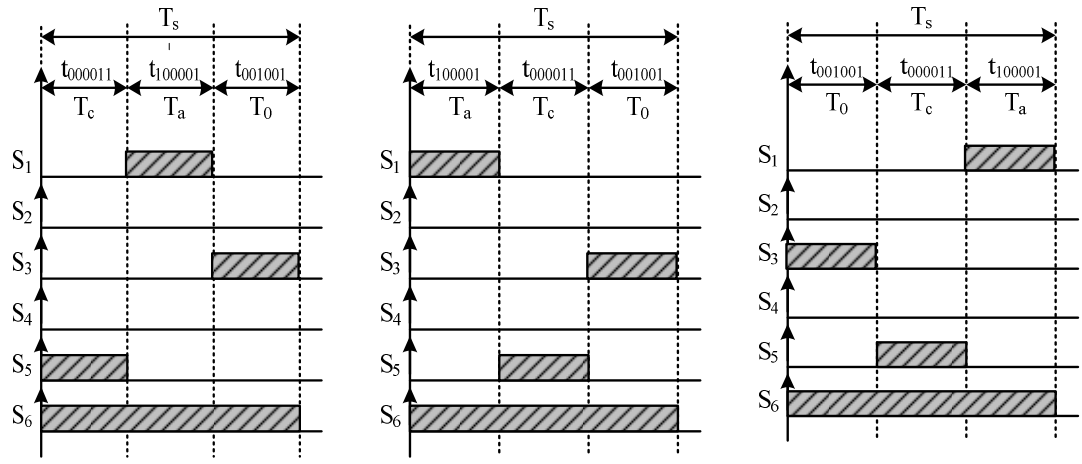
Table 0.4: Summary of the realizable switch sequences for the CSI.

(The symbol ⇆ links reversal switch states that could be re-ordered such that the second state could precede the first without affecting the modulation process; and symbols ↺ and ↻ represent re-ordering process that places the last switch state of the sequence at beginning, and first state to the end of the sequence, without affecting the modulation process)

Sector	**Active states**	**Zero states**	**Possible switching sequences**		
			I	**II**	**III**
I	(i) 000011 (ii) 100001	(a) 100100 ***(b) 001001*** (c) 010010	000011⇆100001 →***001001***↺	↻000011→***001001*** →100001↺	000011→100001 →***100100***
II	(i) 100001 (ii) 110000	***(a) 100100*** (b) 001001 (c) 010010	100001⇆110000 →***100100***↺	↻100001→***100100*** →110000↺	100001→110000 →***010010***
III	(i) 110000 (ii) 011000	(a) 100100 (b) 001001 ***(c) 010010***	110000⇆011000 →***010010***↺	↻110000→***010010*** →011000↺	110000→011000 →***001001***
IV	(i) 011000 (ii) 001100	(a) 100100 ***(b) 001001*** (c) 010010	011000⇆001100 →***001001***↺	↻011000→***001001*** →001100↺	011000→001100 →***100100***
V	(i) 001100 (ii) 000110	***(a) 100100*** (b) 001001 (c) 010010	001100⇆000110 →***100100***↺	↻001100→***100100*** →000110↺	001100→000110 →***010010***
VI	(i) 000110 (ii) 000011	(a) 100100 (b) 001001 ***(c) 010010***	000110⇆000011 →***010010***↺	↻000110→***010010*** →000011↺	000110→000011 →***001001***

After re-ordering the states of sequences I, II, and III, it is established that switching sequence III is unique and non-reversible (any re-ordering to its active or zero states produces switching sequences that cannot be realized practically). Switch sequence II however, permits re-ordering of the active states, but at the expense of fewer optimized switching sequences as the transitions between successive sectors necessitate switching of more than one inverter leg at the same time. The active and zero vectors of switch sequence I can be reordered as shown in Figure 0.12(a) to (c) and Table 5.4, without affecting the modulation process. Reordering of the active states in sequences I and II results in new realizable switching sequences belonging to the original groups (sequences I and II respectively). Also, positioning of the zero-current vector at the beginning or at the end of the switching period in sequence I produces new valid sequences belonging to the same group. Figure 0.12(a) to (c) show re-ordering of active and zero states of the sequence A (example of switch combinations belonging to

sequences I) that produces a new switching sequence belonging to the same group, with the turn-on order of the switching devices changed.



(a) Sequence A (000011→100001→001001)

(b) Reordering of active states in sequence A (100001→000011→001001)

(c)Reordering of zero state in sequence A (001001→000011→100001)

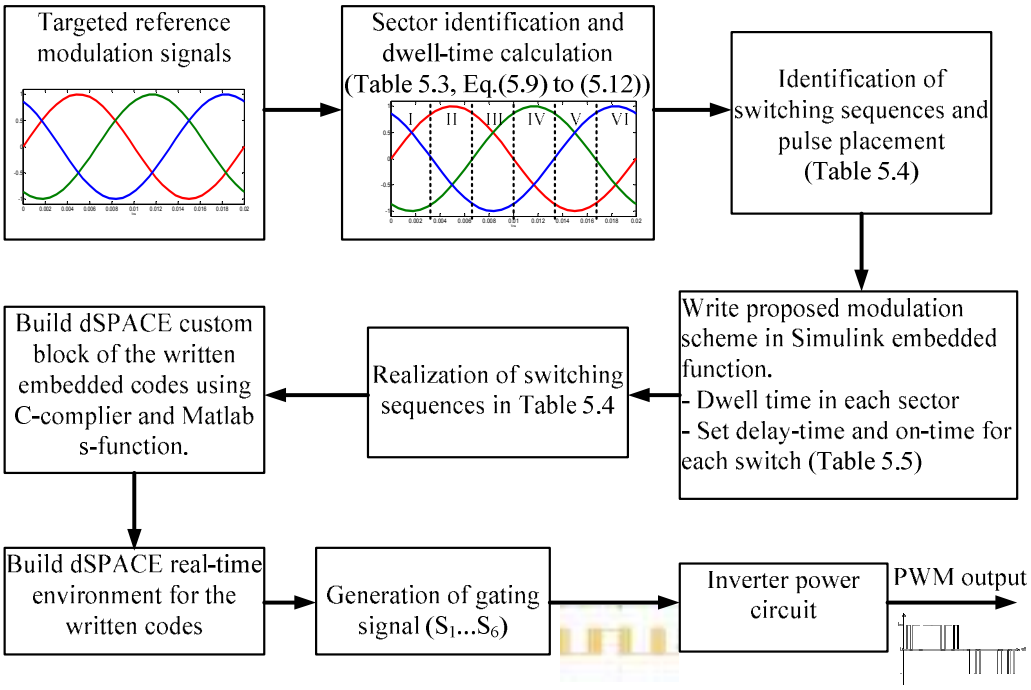
Figure 0.12: Pictorial representation of active states interchanged for sequence I.

5.6.2 Open-loop validation of the proposed DRSPM

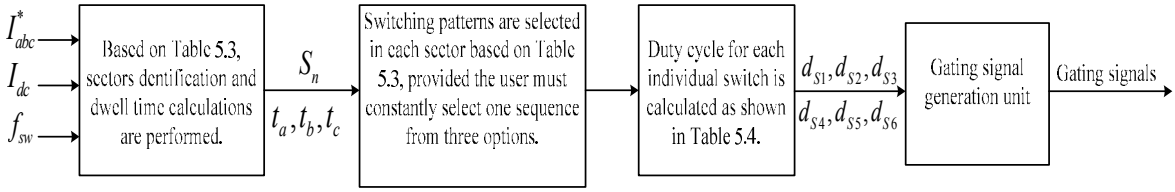
This section presents simulation and experimental results to validate the performance of DRSPWM when used to control a CSI. To further highlight the features of the proposed DRSPWM, CSPWM and SVM are compared in terms of switching frequency per device, harmonic distribution, fundamental inverter current, and total harmonic distortion (THD). The simulation and experimental results presented are obtained when the CSI feeds a resistive load of 22Ω through a CL filter, with capacitance C_F=40μF and inductance L_F=3mH, at a 2.1kHz switching frequency and a dc link inductance of 10mH. This test is necessary to isolate issues associated with the proposed modulation strategy from those of the control system. The dc link current is 5A and the modulation index is 0.8.

The proposed DRSPWM is implemented as an embedded function in Simulink, with all real-time restrictions implemented so that it can be used for simulation and experimentation using dSPACE1006, thereby benefiting from code generation facilities of the real-time workshop embedded coder. Block diagrams that summarise

dSPACE1006 and generic digital implementations of the proposed DRSPWM are shown in Figure 0.13.



(a) dSPACE implementation of the proposed DRSPWM



(b) Generic implementation on any general purpose DSP (digital signal processing) or microcontroller (d_{s1} to d_{s6} represent duty cycles of the switches S_1 to S_6)

Figure 0.13: dSPACE and generic block diagrams that summarise digital implementation of the proposed DRSPWM.

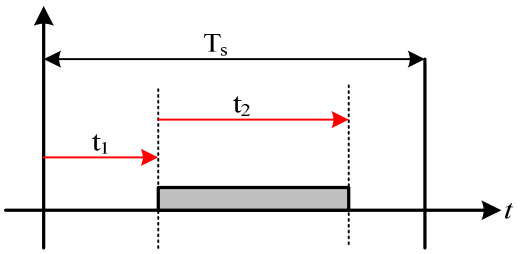


Figure 0.14: Illustration of arbitrary pulse generation.

Table 0.5: Example calculations of the gating pulses delay-time and on-time in the first sector.

Switches		Switches	
S_1	t_1=t_{000011} and t_2= t_{100001}	S_4	t_1=0 and t_2=0
S_2	t_1=0 and t_2=0	S_5	t_1=0 and t_2=t_{000011}
S_3	t_1= t_{000011}+ t_{100001} and t_2= t_0	S_6	t_1=0 and t_2=T_s

Detailed implementation is summarized as follows:

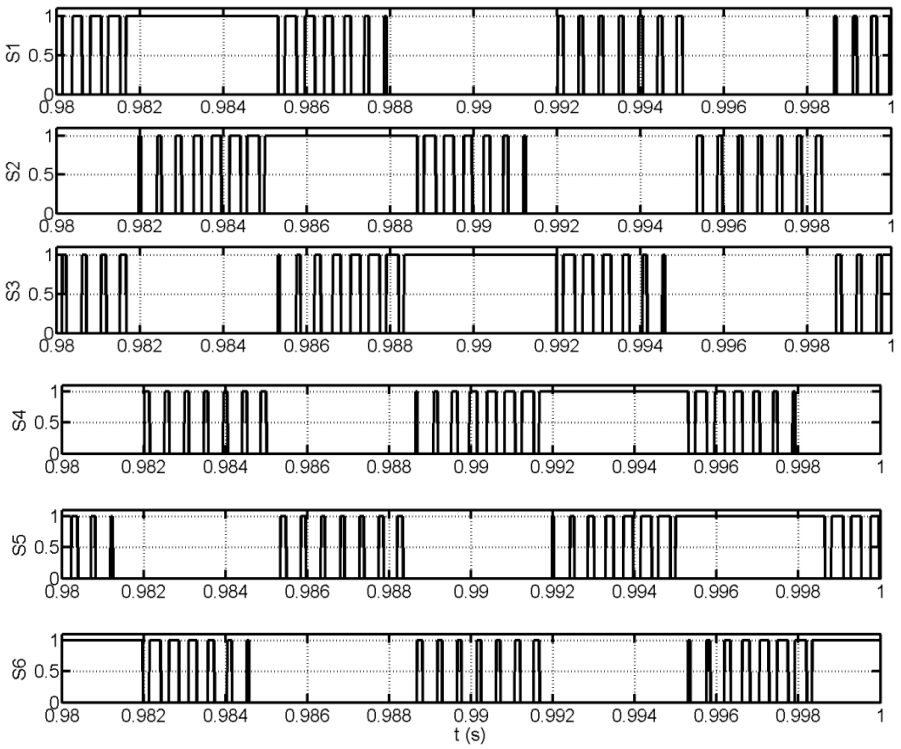
The custom block that permits arbitrary generation of pulse patterns in dSPACE1006 accepts two variables t_1 and t_2, in addition to the switching period, T_s, where t_1 represents pulse delay time, and t_2 is pulse on time (see Figure 0.14). A combination of assembly and low-level C code, and C-sfunction that communicates with the hardware in the dSPACE1006 its the custom block, are written and then integrated into Simulink to permit arbitrary signal generation. The inputs to the C-sfunction are switching period T_s, and t_1 and t_2 for each switch. The DRSPWM scheme is coded as an embedded function in the Simulink environment. The dwell times in each sector are calculated according to Table 0.3, and the delay-time and on-time for each switch in the CSI are set according to the example mapping in Table 5.5.

In this manner, all the proposed switching sequences I, II and III highlighted in Table 5.4 are realized. This explanation shows the suitability of the proposed DRSPWM for digital implementation, having the same flexibility as SVM in controlling switching sequence selection and pulse placement. These features are not available in CSPWM which uses hardware mapping or digital based mapping circuits, or in TS-PWM[5.48]. In this manner the gating pulses can be placed anywhere within the switching period.

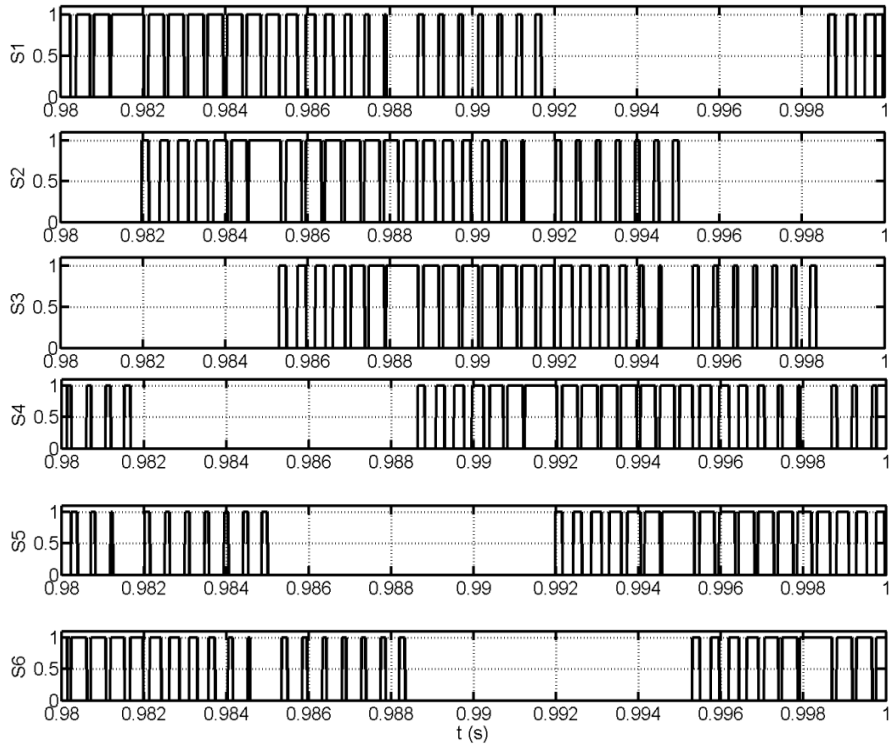
5.6.3. Simulation results

The open loop simulation results in Figure 0.15 illustrate the performance of the proposed DRSPWM at I_{dc}=5A, m_a=0.8 and a 2.1kHz switching frequency. The generated gating signal S_1 to S_6 using the proposed sequences (sequence I,II and III) are shown in Figure 0.15(a) and (b). The figure indicates that the number of switching transitions per fundamental cycle using sequences I and II is less than sequence III. The

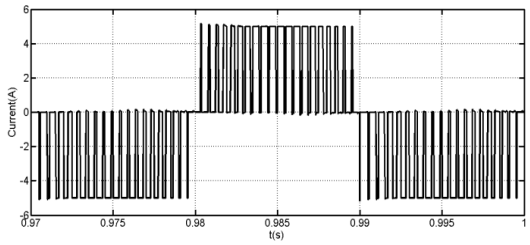
current and voltage waveforms displayed in Figure 0.15(c) to (f) confirm the effectiveness of the proposed DRSPWM in producing a good quality output without having a complex mapping circuit for PWM generation.



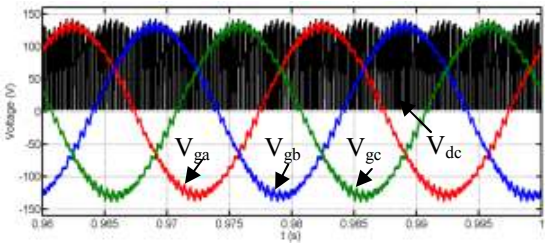
(a) Gating signal $S_1$to S_6 (sequence I and II)



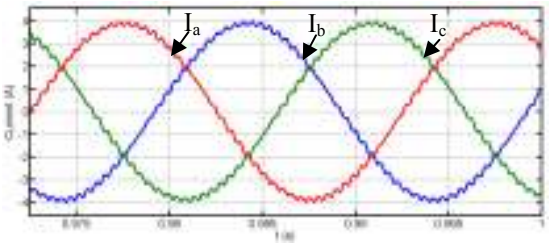
(b) Gating signal S_1 to S_6 (sequence III)



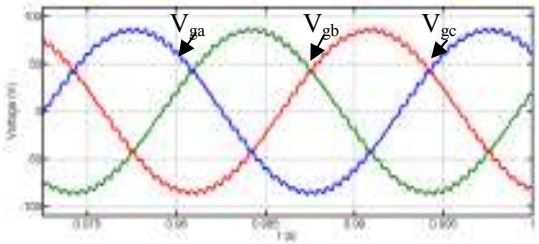
(c) Inverter current before filters with respect to $\pm I_{dc}$



(d) Capacitor voltage with respect to V_{dc}



(e) Three phase load currents



(f) Three phase load voltage

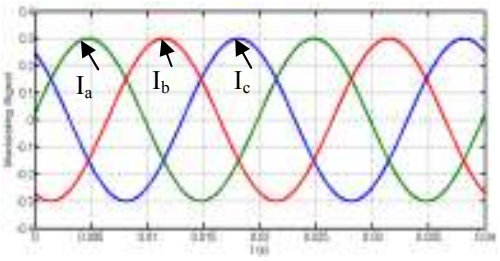
Figure 0.15: Open loop simulation waveforms illustrating the performance of the proposed DRSPWM at I_{dc}=5A, m_a=0.8 and a2.1kHz switching frequency.

5.6.4. Experimental verification of the proposed DRSPWM

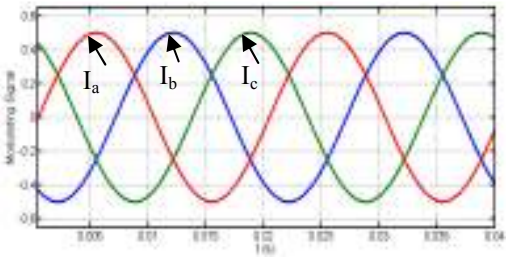
To illustrate the potential deterioration of output current waveform quality as the modulation index varies over the full linear range (0~1) for a fixed input filter (C_F=40μF and L_F=3mH), experimental waveforms for the modulating signals, and pre-filter and three-phase load currents obtained with 0.3, 0.5, 0.8 and 0.95 modulation indices, are presented in Figure 0.16 and 5.17. The load current quality remains virtually the same, except where the modulation index approaches unity. In this region, the pulse widths approach 100%, and dSPACE is unable to generate such pulses with sufficient accuracy. Pulse dropping introduces limited output current distortion. Therefore, the distortion shown at 0.95 modulation index is due to its implementation and this can be avoided using the Tri-Core Microcontroller TC1796 from Infineon.

Figure 0.18 present experimental results from a three-phase CSI having the same parameters and operating conditions as those in the simulations presented in Figure 0.15, with switching sequences I, II and III. The gating signal generation using the possible switching sequences are presented in Figure 0.18(a) and (b) while Figure 0.18(c) and (d) display the load voltage and current. The spectra of the pre-filter load current obtained with switching sequences I, II and III are displayed in Figure 0.19(a) to(c), with THDs of 59.13%, 58.65% and 59.27% respectively. Sequence II shows the lowest THD, with the magnitudes of low-order harmonics and lower sidebands being

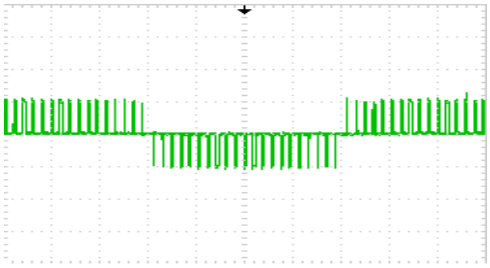
larger than those of sequences I and III, which is agreement with the simulation results. The low-order harmonics appearing in the baseband of sequences I and III are due to the implementation of the proposed DRSPWM in dSPACE1006 (inability to generate pulses with 0 and 100% duty cycle, even with custom coding). The viability of the proposed CSI DRSPWM in a grid mode is investigated in chapter seven.



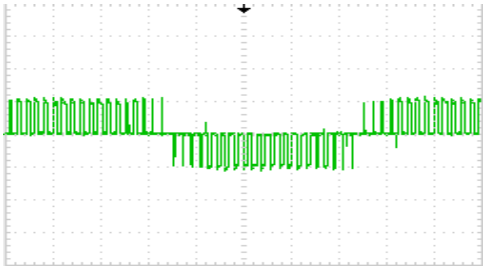
(a) Reference modulating signal, m_a=0.3 (from dSPACE control desk)



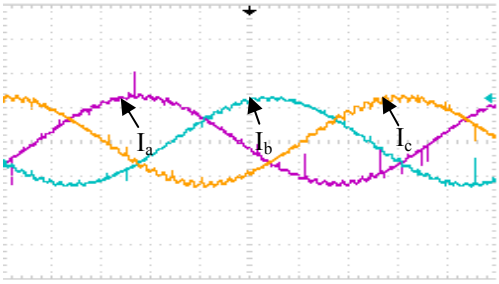
(b) Reference modulating signal, m_a=0.5 (from dSPACE control desk)



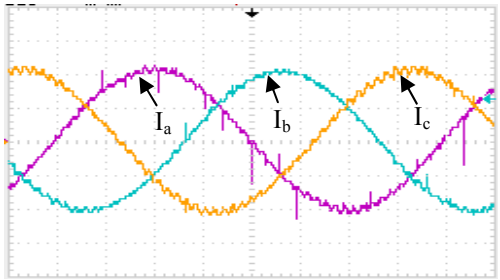
(c) Pre-filter inverter current with m_a=0.3 (5A/div, 2.5ms)



(d) Pre-filter inverter current with m_a=0.5 (5A/div, 2.5ms)

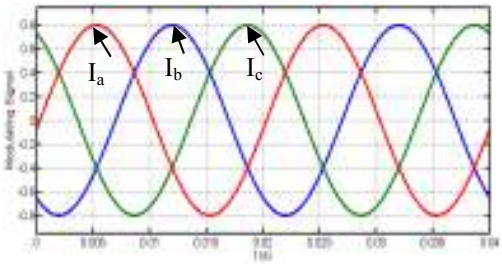


(e) Load current with m_a=0.3 (1A/div, 2.5ms)

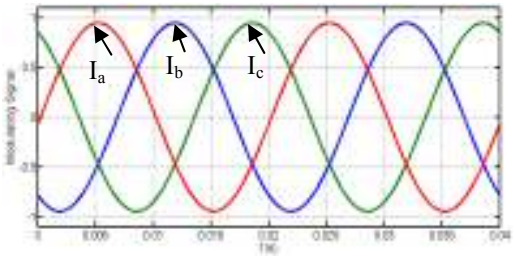


(f) Load current with m_a=0.5 (1A/div, 2.5ms)

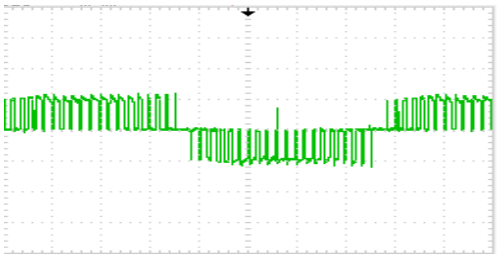
Figure 0.16: Experimental waveforms illustrating reference modulating signal, pre-filter inverter current and load current at m_a=0.3 and m_a=0.5 using the proposed DRSPWM.



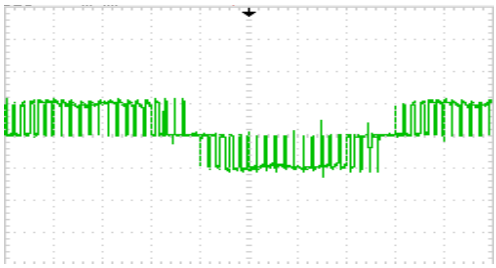
(a) Reference modulating signal, m_a=0.8 (from dSPACE control desk)



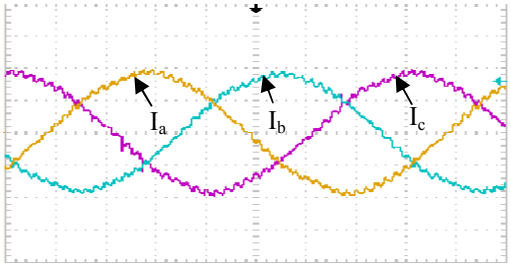
(b) Reference modulating signal, m_a=0.95 (from dSPACE control desk)



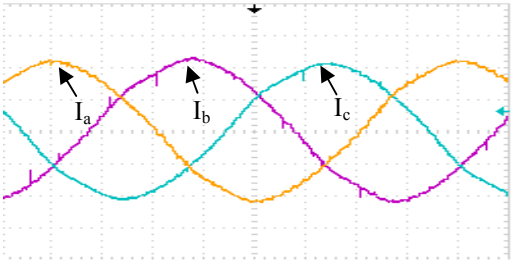
(c) Pre-filter inverter current with m_a=0.8 (5A/div, 2.5ms)



(d) Pre-filter inverter current with m_a=0.95 (5A/div, 2.5ms)

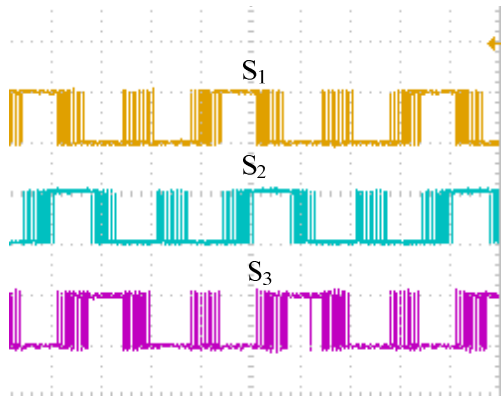


(e) Three-phase load currents with m_a=0.8 (2A/div, 2.5ms)

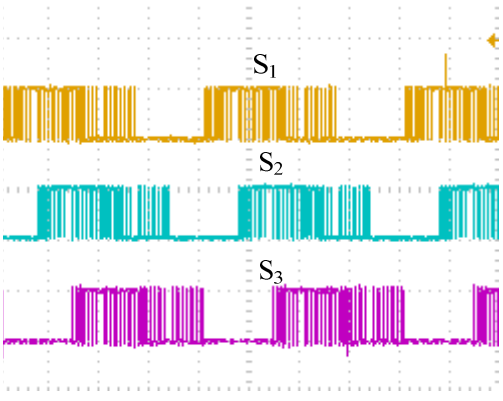


(f) Three-phase load current with m_a=0.95 (2A/div, 2.5ms)

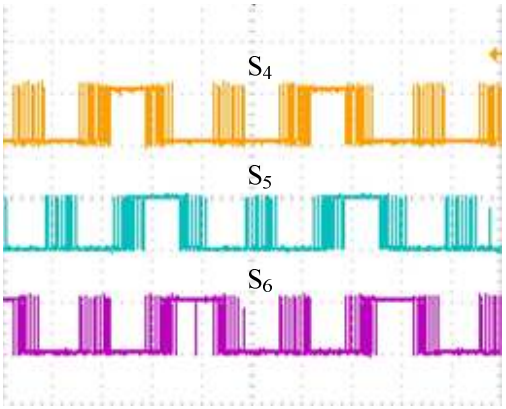
Figure 0.17: Experimental waveforms illustrating reference modulating signal, pre-filter inverter current and load current at m_a=0.8 and m_a=0.95 using the proposed DRSPWM.



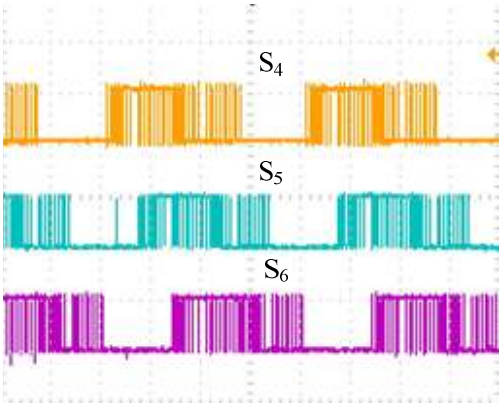
(a) Gating signal S_1 to S_6 (sequence I and II)



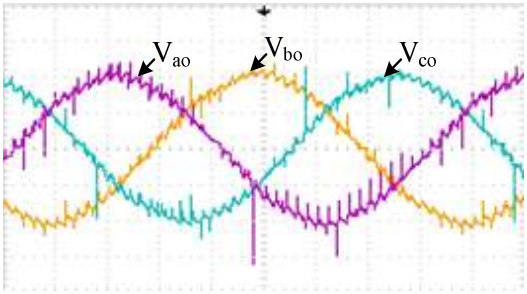
(b) Gating signal S_1 to S_6 (sequence III)



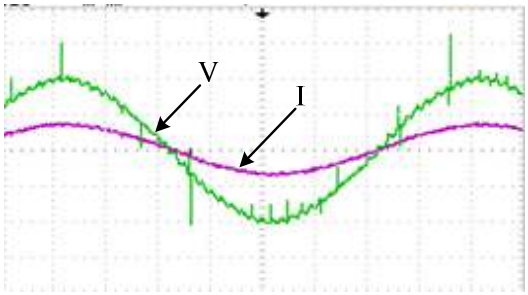
(a) Gating signal S_1 to S_6 (sequence I and II)



(b) Gating signal S_1 to S_6 (sequence III)

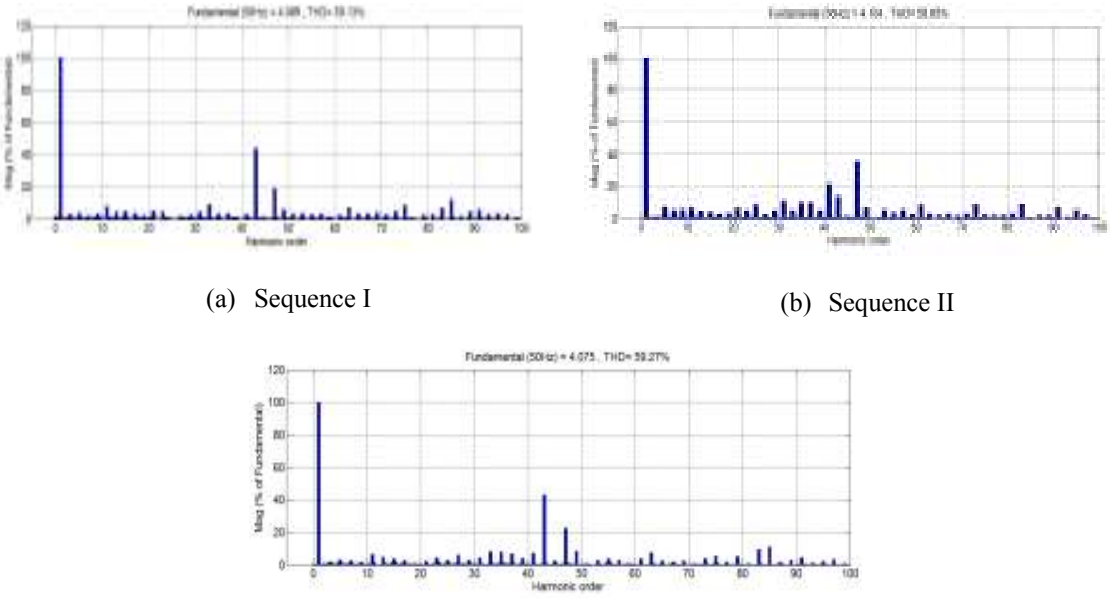


(c) Three-phase load voltages (40V/div, 2.5ms)



(d) Experimental spectrum of inverter current based on sequence I

Figure 0.18: Experimental waveforms illustrating the viability of the proposed RSPWM at m_a= 0.8, 2.1kHz switching frequency, and 70μF filter capacitor.



(a) Sequence I

(b) Sequence II

(c) Sequence III

Figure 0.19: Experimental harmonic spectrum of inverter current based on the proposed sequences I, II and III.

5.7. Assessment of PWM modulation techniques

A comparison between the proposed DRSPWM, the SVM and CSPWM strategies is presented. SVM and CSPWM are implemented using logic mapping circuits, all with a 2.1kHz switching frequency. Figure 0.20(a) to (d) display current waveforms in the switch S_1 when the CSI is controlled using the proposed DRSPWM with switching sequences I, II and III, CSPWM and SVM respectively. The proposed DRSPWM produces the lowest number of switching transitions per fundamental period. In DRSPWM with switching sequences I and II, each CSI switching device operates at half the assigned switching frequency, which is 21 pulses compared to 40 and 27 pulses for CSPWM, and SVM and DRSPWM with sequence III. This implies that the proposed technique has lower switching losses, making it promising for medium-voltage high-power applications. CSPWM has the highest switching rate.

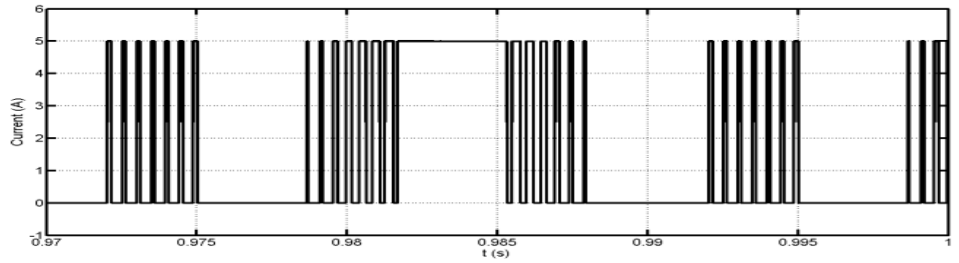
Figure 0.21(a) to (d) present experimental gating signals for switch S_1,for DRSPWM, CSPWM and SVM, to substantiate the simulation waveforms presented in Figure 0.20. The results in Figure 0.21(a) and (b) show that with the proposed DRSPWM sequences I and II, switch S_1 operates only at half switching frequency. Additionally, the experimental results in Figure 0.21(c) and (d) confirm that switch S_1 operates at 64%

and nearly 100% of the switching frequency when SVM and CSPWM are used respectively. This unequivocally shows DRSPWM with sequences I and III have lower switching losses, compared to SVM and CSPWM.

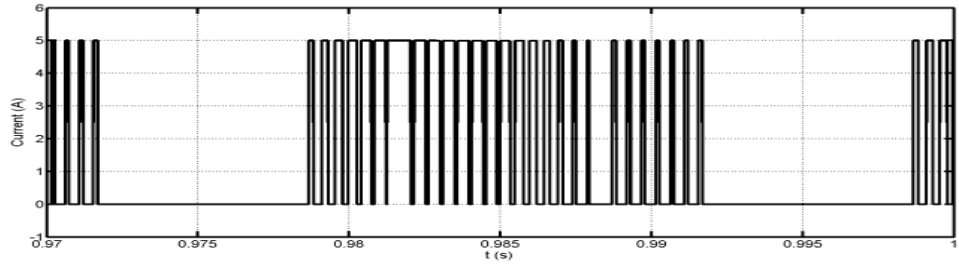
Simulation spectra in Figure 0.22(a) to (c) show that sequences I and III have no low-order harmonics in the baseband, with the sidebands located at lower frequencies than the switching frequency components, and with magnitudes which are much smaller than for CSPWM and SVM. Sequence II produces a significant number of low-order harmonics but has the lowest THD (72.37%) of all the discussed modulation techniques. Despite the difference in pulse placement within each switching cycle of sequences I and III, they have a similar harmonic distribution, including sideband harmonic magnitudes and similar THD (76.73% and 76.65% respectively). As the switching frequency increases, the magnitudes of the low-order harmonics produced by sequence II decrease rapidly. As a results, sequence II can be used for applications that use a high switching frequency. On the other hand, Figure 0.22(d) shows that CSPWM has low-order harmonics and its sideband placements are identical to that of a VSI, which are located at $mf_s \pm nf$, where n is even for odd-carrier frequencies ($m=2k+1$, $k=0,1,2\ldots$), and odd for even carrier frequencies ($m=2k$, $k=1,2,3\ldots$). The only exception is the absence of the carrier frequency components, which is expected in the CSI. Furthermore, CSPWM has the highest THD (91.12%). The SVM spectrum in Figure 0.22(e) shows that the sidebands around the first switching frequency component are widely spread, and that those located below the switching frequency component may behave as low-order harmonics. These may affect the ac filter design in a similar manner as low-order harmonics. Also, no switching frequency components are presence in the spectrum. The calculated THD for SVM is 76.55%.

Figure 0.23(a) and (b) present the relationships between modulation and attainable fundamental current magnitude (pre-filter), and THD for DRSPWM, CSPWM and SVM. The proposed DRSPWM matches SVM in the entire modulation index range, with both achieving a maximum fundamental current magnitude, $I_{m,max}$ equal to I_{dc} where $m_{a,max}=1$. The maximum achievable fundamental current magnitude with CSPWM is only $I_{m,\max} = m_a \frac{\sqrt{3}}{2} I_{dc} = 0.866 I_{dc}$ (see Figure 0.23(a)). The plot of THD

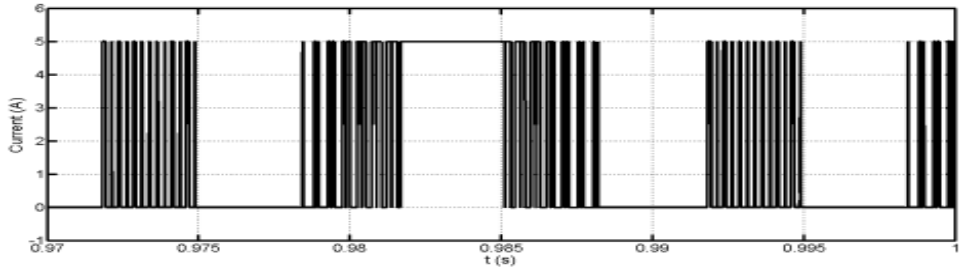
versus modulation index in Figure 0.23(b) shows that the proposed DRSPWM and SVM have lower THD than CSPWM.



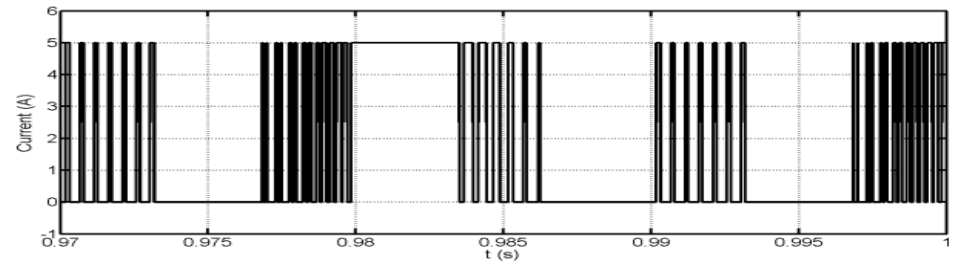
(a) Current waveform for switch S_1 (21 pulses per cycle for sequence I and II)



(b) Current waveform for switch S_1(27 pulses per cycle for sequence III)

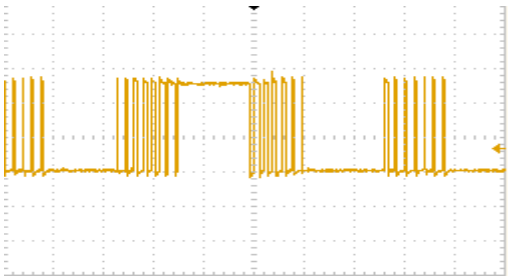


(c) Current waveform for switch S_1using CSPWM (40 pulses per cycle)

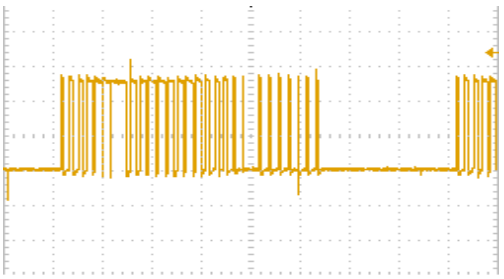


(d) Current waveform for switch S_1 using SVM (27 pulses per cycle)

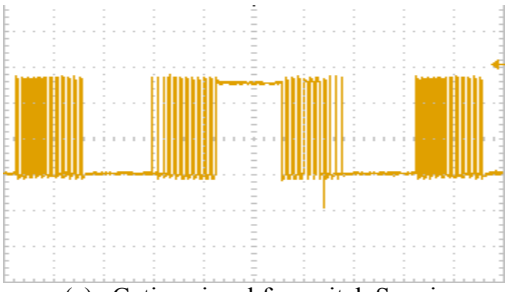
. Figure 0.20: Current waveforms for switch S_1 for the proposed DRSPWM technique, CSPWM and SVM, at I_{dc}=5A, m_a=0.8 and a 2.1kHz switching frequency.



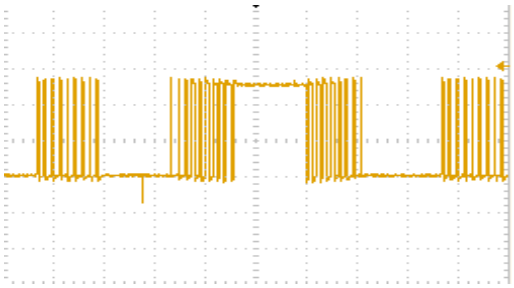
(a) Gating signal for switch S_1 using sequence I and II (2A/div,2.5ms), (21 pulses per cycle)



(b) Gating signal for switch S_1 using sequence III (2A/div,2.5ms),(27 pulses per cycle)

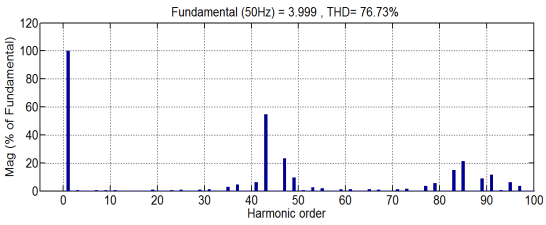


(c) Gating signal for switch S_1 using CSPWM (2A/div, 2.5ms), (40 pulses per cycle)

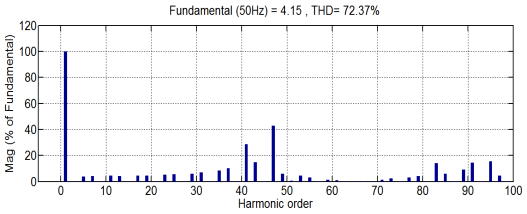


(d) Gating signal for switch S_1 using SVM (2A/div,2.5ms), (27 pulses per cycle)

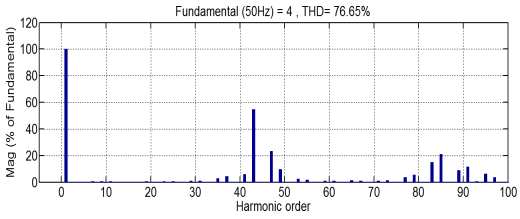
Figure 0.21: Experimental waveforms illustrating the gating signal for switch S_1 for the proposed DRSPWM technique, CSPWM and SVM at I_{dc}=5A and m_a=0.8.



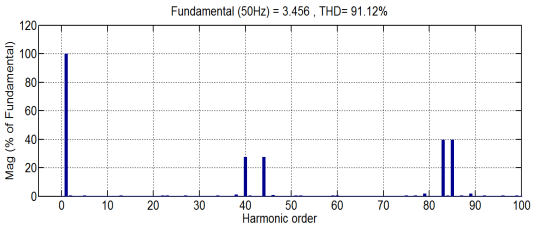
(a) DRSPWM (Sequence I)



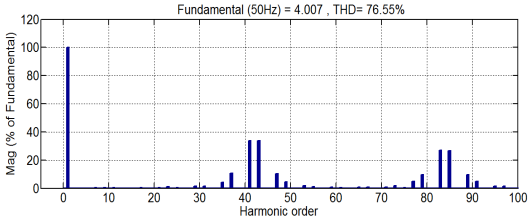
(b) DRSPWM (Sequence II)



(c) DRSPWM (Sequence III)

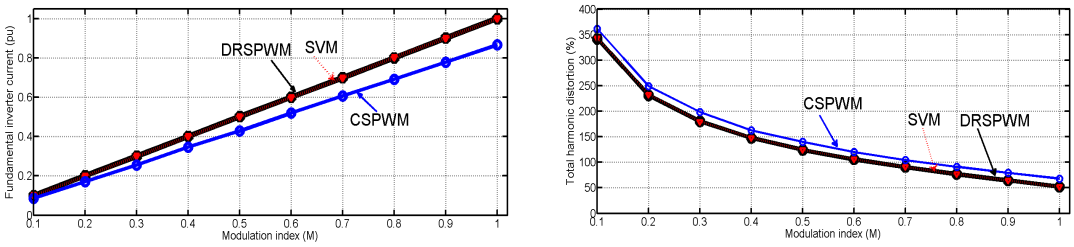


(d) CSPWM



(e) SVM

Figure 0.22: Theoretical spectrum of inverter current before ac filters.



(a) (b)

Figure 0.23: Comparison of PWM strategies with varying modulation index for (a) per-unit fundamental pre-filter inverter current and (b) total harmonic distortion (%THD), all at 2.1kHz switching frequency.

5.8. Summary

A new direct regular sampled pulse width modulation (DRSPWM) strategy for CSIs, including its theoretical basis, has been presented. The proposed DRSPWM is suitable for DSP and microcontroller digital implementation, and is simpler to implement than the other CSI modulation strategies presented in this chapter. It has been shown that some of the switch sequences of the proposed DRSPWM optimally operate the CSI from a switching loss prospective, in the same manner that dead-band modulation suspends operation of each VSI arm for 120^{o}. The viability of the presented DRSPWM strategy has been confirmed using simulations and experimentation.

It is concluded that the distinct features of the proposed DRSPWM are:

- Reduced complexity of CSI gate signal generation through elimination of logic mapping circuitry, hence implicit pulse pattern generation of the carrier based modulation is avoided.
- The same degree of freedom, flexibility and dc link utilization as space vector modulation, while expecting to maintain the robustness of the carrier based SPWM during unbalanced operation in a grid connected environment.
- Some of its switching sequences, such as I and II, halve the switching frequency per device, compared to carrier based SPWM, thus lower switching losses are anticipated.

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Chapter Six

DC Current Offset Compensation Technique for Grid Connected Inverters

7.0. Introduction

This chapter discusses dc current offset injection for integration of grid connected inverters which are applicable to medium-scale solar farms or any group of grid connected inverters confined within a relatively small area. DC current injection severely affects distribution system components such as isolation transformers, measurement units and protective relays. Several dc current offset compensation techniques claim to be appropriate to compensate dc current injected by grid connected inverters. This chapter presents a dc current offset compensation technique that exploits a simple resonance controller in combination with a proportional-integral controller to reduce capital cost of medium-scale solar farms. The proposed technique permits transformerless inverter operation within the solar farm, and uses only one large isolation transformer at the point of common coupling. Simulation and experimentation are used to demonstrate the practicability of the proposed system.

7.1. Background

Power quality is an important issue for the integration of grid connected inverters. The majority of research in the power quality area is commonly focused on active harmonics filtering techniques using active power filters and voltage sag compensation using series compensators, such as dynamic voltage restorers. Issues related to dc current injection in inverter based distributed generation have been generally overlooked, despite growing concerns regarding its effect on distribution system components. One of the most severe problems caused by dc currents is saturation of the distribution transformers, resulting in waveform distortion, excessive losses, overheating and

reduced lifespan. In addition, it also may cause inaccuracy in some of the measurement and protective relays systems [6.1-4].

A possible source of dc current injection into the grid arises from the semiconductor circuits in inverter systems. The appearance of unwanted dc current components in the output currents of such systems can be attributed to several factors including minor asymmetry in the pulse width modulation signals that may be caused by numerical truncated errors in the calculation of the switching instances, nonlinearity of the switching devices, and small errors and offset drift in the voltage and current measurement sensors used to provide feedback signals for the control systems [6.5, 6].

A number of guidelines and standards imposed are to minimize the impact of dc current injection into the ac grid [6.7]. Among these standards and recommendations are guidelines to limit the allowable amount of dc current injection into the distribution network. These are listed in Table 0.1, and vary from country to country. For example, British Standard G83/1 limits dc injection to 20mA for distributed generation with phase currents below $16A_{rms}$[6.8]. In IEEE standard 'IEEE 929-2000' the dc limit is 0.5% of the inverter rated current [6.9]. The dc current injection in the Australian standard AS4777.2 should not exceed 0.5% of the inverter rated output current or 5mA, whichever is the greater [6.10]. These standards, however, do not guarantee that the cumulative effect of numerous power converters connected to the grid remains within the permissible limit, without harmful effects on electric system components sensitive to dc current components. Various methods have been proposed to prevent or minimize dc current injection by grid-connected inverters in photovoltaic systems. These are discussed in detail in Section 6.2.

Table 0.1: Collection of general guidelines that impose limits on the allowable level of dc current injection into the grid by photovoltaic inverter systems.

Country	Standard	Maximum dc current permitted with transformer	Maximum dc current permitted without transformer
United Kingdom	ER G83/1	-	5mA
United States	IEEE 929-2000	½% of rated power inverter	½% of rated power inverter
Australia	AS 4777.2	½% of rated power inverter or 5mA (whichever greater)	½% of rated power inverter or 5mA (whichever greater)
Germany	DIN VDE 126	-	1000mA
Japan	Technical Guideline for the Grid Interconnection	1% of rated power inverter	1% of rated power inverter
Spain	RD 1663/2000	-	-

7.2. Review of dc current compensation techniques

This section provides insight into the existing methods that have been proposed in the literature to minimize dc current injection into the distribution network. These methods can be categorized as passive and active.

6.2.1. Passive methods

These methods use passive components, such as a coupling or isolation transformers and capacitors, to prevent dc current injection from the grid connected inverter.

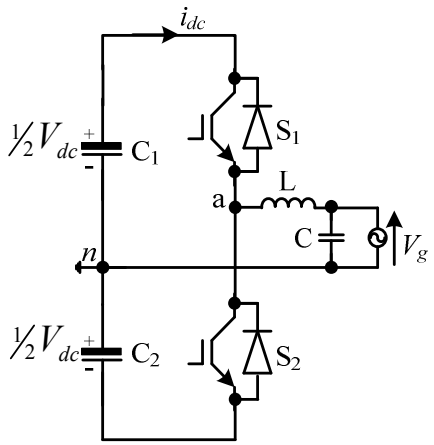
A. Isolation transformer

A line frequency isolation transformer is frequently employed at the inverter output to prevent penetration of unwanted dc currents into the grid. Also, it provides galvanic isolation between the photovoltaic system and the grid. However, a 50/60Hz transformer is large, heavy and is a substantial cost in grid connected inverter systems. Additionally, it contributes to system losses and footprint. Thus, transformerless systems have become attractive in the recent years. It has been claimed that adoption of a transformerless PV inverter system reduces the overall system costs by 25%, compared to the cost of a system that includes a transformer [6.11], and improves system efficiency by 1.5 to 2% [6.12, 13].

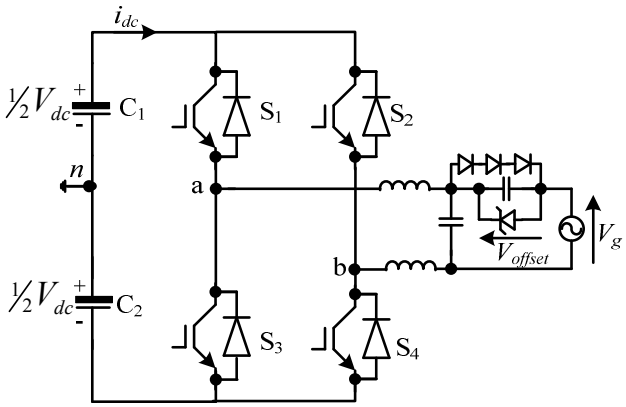
B. Blocking capacitors

Some researchers use dc and ac side capacitors to block dc current injection into the grid. For example, [6.14]present a transformerless single-phase half-bridge inverter with the neutral connected to the supply mid-point (dc node formed by connection of two dc side capacitors in series as shown in Figure 0.1(a). However, this approach is not readily extendable to three-phase inverter systems.

An alternative method that prevents dc current injection into the distribution network is to place an ac capacitor in series with the grid, with a diode network connected across the capacitor for over-voltage protection, as shown in Figure 0.1(b) [6.15]. However, this approach is risky as it may excite resonance with the ac grid and can potentially create harmonic current magnification, and hence worsen the power quality and degrade system stability.



(a) Single-phase half-bridge inverter with dc blocking capacitors



(b) Single-phase H-bridge inverter with ac blocking capacitor

Figure 0.1: Blocking capacitor circuits for single-phase grid connected inverters.

6.2.2. Active methods

Existing active methods for preventing dc current injection into the grid mainly rely on high precision current sensors in combination with some form of measurement or voltage transformer (VT) to control dc injection. However, the ability of a current sensor to detect a small dc component in a large ac current is expensive and challenging. These approaches are expensive to implement in medium to large scale solar farms as each inverter unit requires complex transformers and current sensors.

A. Current sensor and controller

A method of detecting and compensating dc offset injection in an H-bridge grid-connected inverter is proposed in [6.16]. The technique uses a voltage transformer (VT) with a 1:1 turns ratio, and an RC circuit. The primary side of the VT is connected across the grid while the secondary is connected in series with the RC circuit. With an assumption of a 1:1 turns ratio, the dc offset appears across the RC circuit capacitor and is fed back to a PI controller which in turn adjusts the inverter reference current as shown in Figure 0.2. The dc offset is eliminated, but there is no experimentation presented to validate the proposed technique. References [6.1, 17, 18] studied and verified the method introduced in [6.16], and a mathematical model-based controller with experimental validation is presented. However, the method adds cost and power loss, and increases the system footprint.

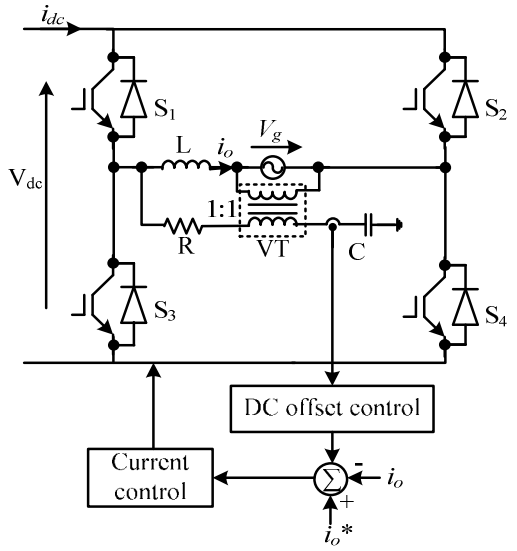


Figure 0.2: DC offset current control loop with a voltage transformer (VT).

In [6.6, 19], a method for dc current compensation in a transformerless full-bridge inverter is introduced. The method compensates the dc voltage in the inverter output, which is assumed to be proportional to the dc current offset that appears in the inverter output currents. The dc offset sensor is connected across the inverter terminals and consists of a magnetic circuit which is implemented using a low power toroidal transformer, as shown in Figure 0.3. The toroidal magnetic core is small, with winding resistance ranging from 30Ω to 80Ω. Operation depends on saturation of the reactor. When a dc voltage appears at the inverter output, in a closed-loop condition, distortion results in the reactor current. The experimental results show that this method is able to minimize the dc current component to less than 5mA for an injected grid current of $8A_{rms}$, which is within the IEEE standard limit.

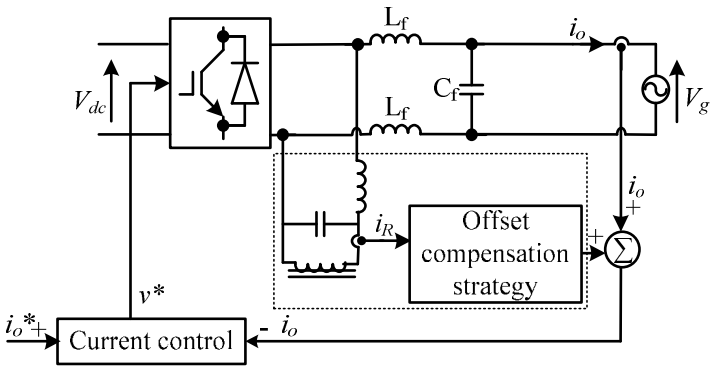


Figure 0.3: DC compensation technique using low power toroidal transformer as a dc offset sensor.

B. Auto-calibrating technique of dc link sensor and controller

Figure 0.4 shows dc compensation based on an auto-calibrating technique, where a current transducer is placed between the dc link capacitor and inverter switches to measure the dc current at the output, as proposed in [6.5]. This calibration technique is based on the operational state of the inverter. A connecting state is when output current flows to the load via the dc link sensor, and the freewheeling state where there no current flows in the sensor. During the freewheeling states, the current sensor output can be sampled and used to remove any offset current present in the inverter output current. The authors presented experimental results showing this auto-calibration technique is able to limit the dc current component to less than 8.63mA for a $10A_{rms}$fundamental current component in the inverter output. It is claimed that this method offers the possibility of operation in a transformerless mode of grid connected inverter systems.

In [6.20], two dc link current sensors are used to compensate the dc offset current in the three-level half-bridge inverter shown in Figure 0.5. The upper sensor is connected between the upper terminal of dc capacitor C_1 and the upper switch S_1 to measure the positive dc link current during the positive half of the mains cycle. The dc offset is calibrated during the negative half cycle, when the positive dc link current drops to zero. The lower sensor is coupled between the bottom terminal of dc capacitor C_2 and bottom switch S_4 to measure the negative dc link current during the negative half cycle. In this case, the dc offset is removed during the positive half cycle when the negative dc link current drops to zero during the positive half mains cycle. The proposed method is able to limit the dc component to 7.08mA in a $5A_{rms}$ inverter output current[6.14]. However, the claimed success of these methods is limited because the current sensors are placed where they measure discontinuous currents, which is impractical.

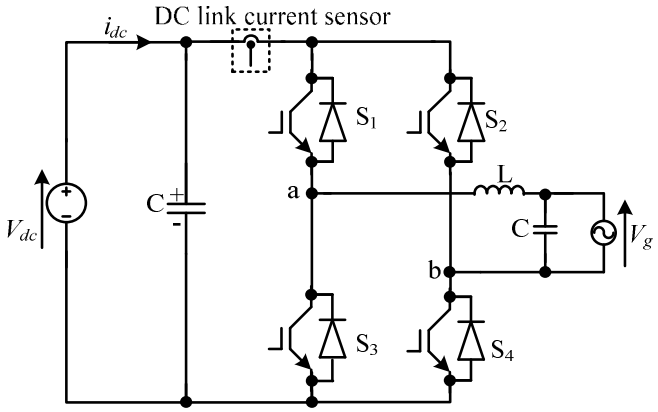


Figure 0.4: H-bridge inverter using dc-link current sensor to compensate dc current injection into the ac grid.

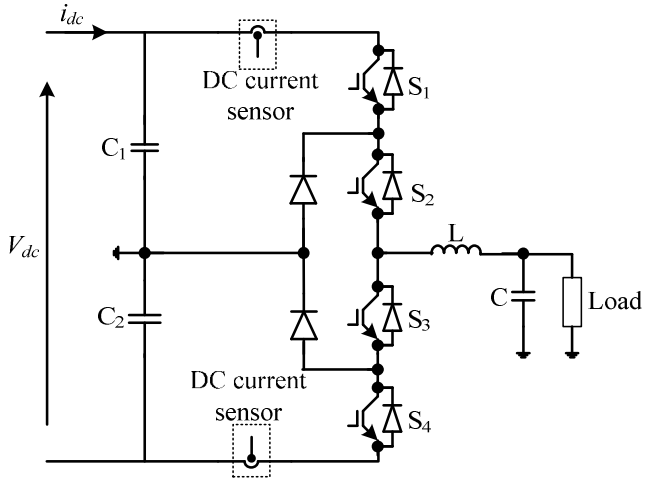


Figure 0.5: Three-level half bridge inverter using positive and negative dc current sensors to compensate dc current injection to the load.

7.3. Proposed dc current offset compensation technique for grid-connected inverters

This thesis proposes a viable technique to suppress dc current injection into the ac grid, which is applicable to medium-scale solar farms or any group of grid connected inverters confined within a relatively small area, as illustrated in Figure 0.6. The significance of this technique is that it does not rely on high-precision current measurement devices and does not use any form of complex transformer. Additionally, it allows transformerless operation of all inverters within the solar farm, and uses one power transformer rated at the full power of the solar farm. At least one inverter must be designated to perform dc offset compensation besides its basic function of active power interfacing into the ac grid. This inverter is required to compensate for all dc offsets that may exist in the total solar farm current before reaching the main interfacing transformer, and hence the risk of transformer saturation is avoided.

Referring to Figure 0.6, dc-link voltage of this inverter may come from PV panels with similar ratings as the other grid connected inverters if it is designed to perform dc offset compensation and active power interfacing into ac grid. However, a small rating of the inverter may require if it is designed to compensate dc offset only.

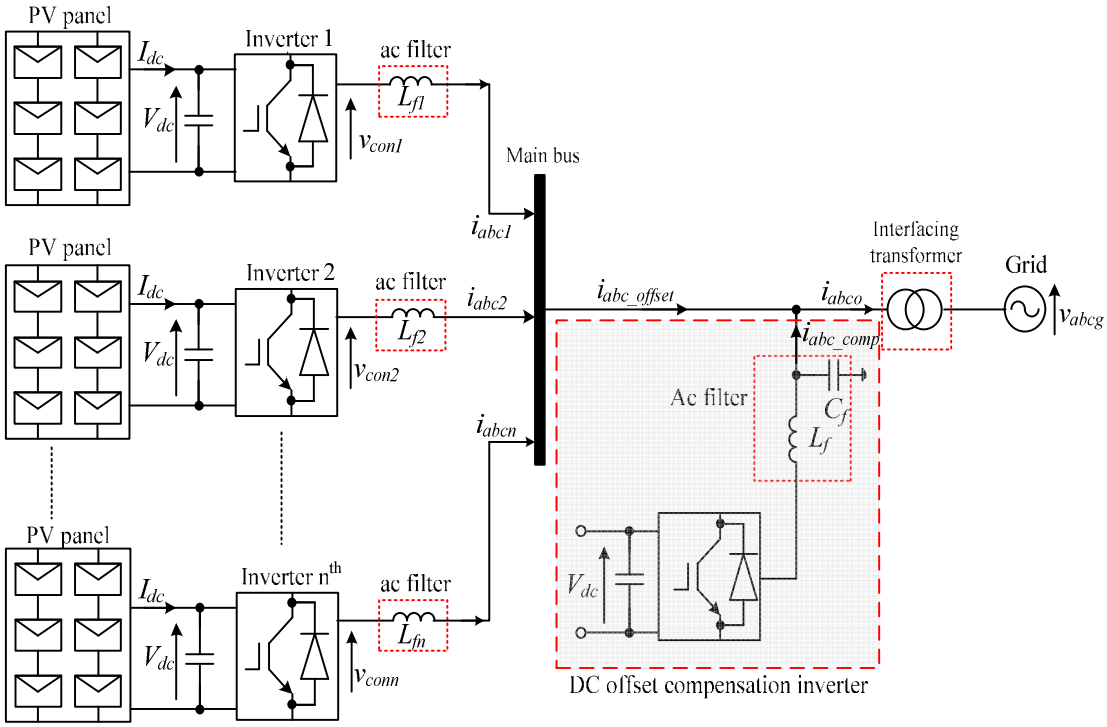
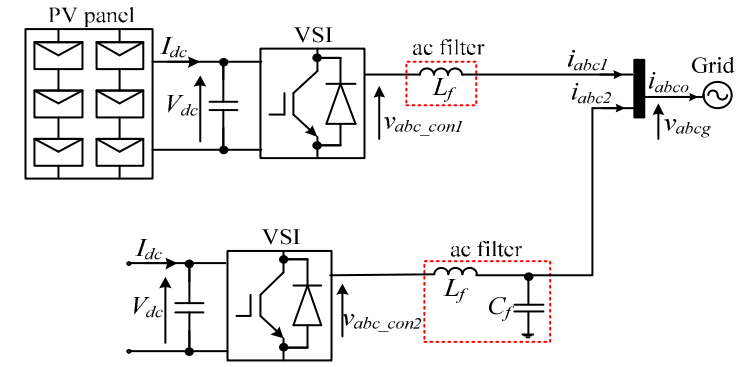
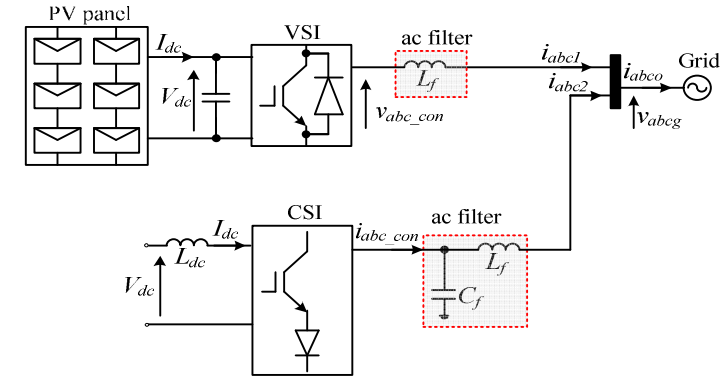


Figure 0.6: Generic diagram of grid connected inverters with dc offset compensation inverter in a solar farm.

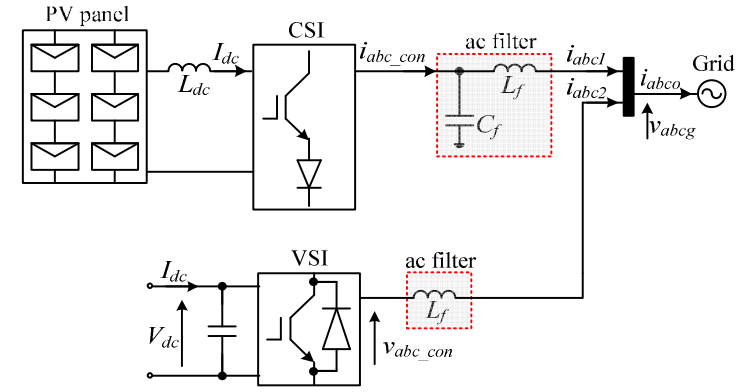
The approach estimates the dc offset in the total current (excluding the current of the inverter designated for dc offset compensation) by computing the mean current for each phase independently, and forces the dc offset in the total current to zero using combinations of proportional-integral (PI) and proportional resonance (PR) controllers using phase variables (*abc*). The proportional-integral (PI) or proportional (P) controller estimates the dc components needed in the modulating signal of each phase in order to counter the dc offsets in the total current. The resonance controller is used to control the fundamental currents needed for exchanging the active and reactive power with the ac grid. Figure 0.7(a) to (d) summarise the possibilities of using voltage and current source inverters for dc compensation.



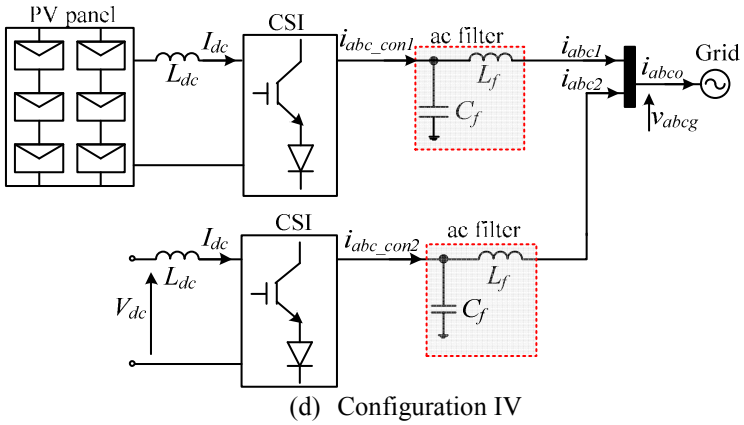
(a) Configuration I



(b) Configuration II



(c) Configuration III



(d) Configuration IV

Figure 0.7: Possible VSI and CSI configurations for the proposed dc offset compensation method.

The polluted phase current with dc offset for phase '*a*' can, for example, be expressed as:

$$i_a = I_{dc} + I_m \sin(\omega t + \varphi) \tag{6.13}$$

where I_{dc} represents the dc component of the phase current, I_m is the peak phase current, φ is the phase angle in radians, and ω is the system frequency in rad/s.

The mean or average current for phase '*a*' is:

$$\tilde{i}_a = \frac{1}{T}\sum_{k=0}^{N} i_a(k\omega T_s) = \frac{1}{T}\int_0^T i_a(\omega t)dt = \frac{1}{2\pi}\int_0^{2\pi}\left[I_{dc} + I_m \sin(\omega t + \varphi)\right]d\omega t = I_{dc} \tag{6.14}$$

In this manner, the dc offsets for the remaining phases are calculated, where T_s is the sampling period and N is the number of samples per fundamental period T.

The dc voltage component to be injected into the modulating signal of each phase of the designated inverter, in order to generate the dc current that will counter the existing dc component in the polluted phase currents, can be obtained from a proportional or proportional-integral controller as:

$$u_{dc\_abc} = k_{pdc}\left(I^*_{dc} - I_{dc\_abc}\right) + k_{idc}\int\left(I^*_{dc} - I_{dc\_abc}\right)dt \tag{6.15}$$

where I_{dc_abc} represents the vector of the dc offsets for the three phases.

The fundamental currents in response to the main active and reactive power exchange of the inverter additionally designated for dc current compensation, can be controlled using a PR controller tuned at fundamental frequency ω_0. The PR controller is favoured over a conventional PI controller because of its effectiveness in eliminating steady-state error in the *abc* instantaneous frame. The traditional PR controller transfer function used in this chapter is expressed as:

$$y = k_p e + k_i \frac{es}{s^2 + \omega_o^2} \tag{6.16}$$

where k_p is the proportional gain, k_i is the integral gain, $e = \tilde{i}^*_{abc} - \tilde{i}_{abc}$ is the error signals between the fundamental ac currents and their references, and ω_o is the fundamental angular frequency.

The PR controller transfer function in (6.16) is discretized using a forward Euler DSP implementation, with details of this discretization provided in Chapter 4 (equations 4.21

to 4.27). However, for general controller design, and with the aid of Figure 0.8, equation (6.16) has been transformed from the *s*-domain to the time-domain, to be incorporated into the inverter state space equations:

$$\tilde{y}(s) = \tilde{y}_1(s) + \tilde{y}_2(s) \tag{6.17}$$

$$\tilde{y}_1(s) = k_p e(s) = k_p \left(\tilde{i}^*_{abc}(s) - \tilde{i}_{abc}(s) \right) \tag{6.18}$$

$$\tilde{y}_2(s) = k_i \frac{s}{s^2 + \omega_0^2} e(s) = k_i \frac{1}{s + \frac{\omega_0^2}{s}} \left(\tilde{i}^*_{abc}(s) - \tilde{i}_{abc}(s) \right) \tag{6.19}$$

Equation (6.19) can be rewritten as:

$$s\tilde{y}_2(s) + \frac{1}{s}\omega_0^2 \tilde{y}_2(s) = k_i \left(\tilde{i}^*_{abc}(s) - \tilde{i}_{abc}(s) \right) \tag{6.20}$$

With a change of variable, $\tilde{y}_3(s) = \frac{1}{s}\tilde{y}_2(s)$, the following sets of first-order differential equations describe the resonance controller suitable for incorporation into to the inverter state space model:

$$\tilde{y}_1(t) = k_p \left(\tilde{i}^*_{abc}(t) - \tilde{i}_{abc}(t) \right) \tag{6.21}$$

$$\frac{d\tilde{y}_2(t)}{dt} + \tilde{y}_3(t) = k_i \left(\tilde{i}^*_{abc}(t) - \tilde{i}_{abc}(t) \right) \tag{6.22}$$

$$\frac{d\tilde{y}_3(t)}{dt} = \omega_0^2 \tilde{y}_2(t) \tag{6.23}$$

$$\tilde{y}(t) = \tilde{y}_1(t) + \tilde{y}_2(t) \tag{6.24}$$

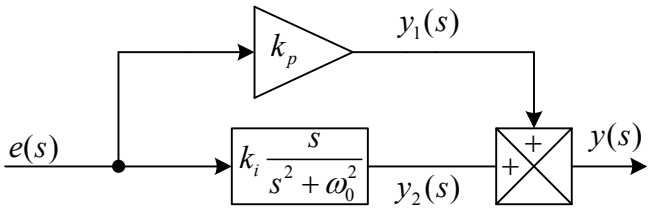


Figure 0.8: Block diagram that represents the proportional resonance controller.

The differential equation that describes inverter ac-side dynamics, when considering only the fundamental ac currents and voltages, is:

$$\frac{d\tilde{i}_{abc}}{dt} = -\frac{R_f}{L_f}\tilde{i}_{abc} + \frac{\tilde{v}_{abc\_con} - \tilde{v}_{abcg}}{L_f} \tag{6.25}$$

By setting $\tilde{y}_{abc} = \tilde{v}_{abc\_con} - \tilde{v}_{abcg}$, equation (6.25) can be written as:

$$\frac{d\tilde{i}_{abc}}{dt} = -\frac{R_f}{L_f}\tilde{i}_{abc} + \frac{\tilde{y}_{abc}}{L_f} \tag{6.26}$$

Variable $\tilde{y}_{abc}$ is the PR controller output in Figure 0.8. Therefore the normalized reference voltages provided to the modulator, taking into account the grid voltage as feed-forward are:

$$\tilde{v}^*_{abc} = \frac{2}{V_{dc}}\left(\tilde{y}_{abc} + \tilde{v}_{abcg}\right) \tag{6.27}$$

Substitute $\tilde{y}_{abc} = k_p\left(\tilde{i}^*_{abc}(t) - \tilde{i}_{abc}(t)\right) + \tilde{y}_2$ into (6.26), results in the following equation:

$$\frac{d\tilde{i}_{abc}}{dt} = -\frac{\left(R_f + k_p\right)}{L_f}\tilde{i}_{abc} + \frac{1}{L_f}\tilde{y}_2 + \frac{k_p}{L_f}\tilde{i}^*_{abc} \tag{6.28}$$

Differential equations (6.22), (6.23) and (6.28) can be merged into a single state space equation that can be used for selection of the PR controller gains, where the inverter internal dynamics are set by its passive components:

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_{abc}\\ \tilde{y}_2\\ \tilde{y}_3\end{bmatrix} = \begin{bmatrix}-\frac{(R_f + k_p)}{L_f} & \frac{1}{L_f} & 0\\ -k_i & 0 & -1\\ 0 & \omega_0^2 & 0\end{bmatrix}\begin{bmatrix}\tilde{i}_{abc}\\ \tilde{y}_2\\ \tilde{y}_3\end{bmatrix} + \begin{bmatrix}\frac{k_p}{L_f}\\ k_i\\ 0\end{bmatrix}\tilde{i}^*_{abc} \tag{6.29}$$

The current controller designs for the other inverters that are responsible only for active power injection into grid are similar.

Figure 0.9 summarises the control system for the inverter designated for dc current offset compensation. The control of fundamental current and dc offset can be performed with independent controllers as described, or both components can be controlled using a single PR controller, provided the proportional part of the PR controller is sufficient for suppressing the dc offsets to zero.

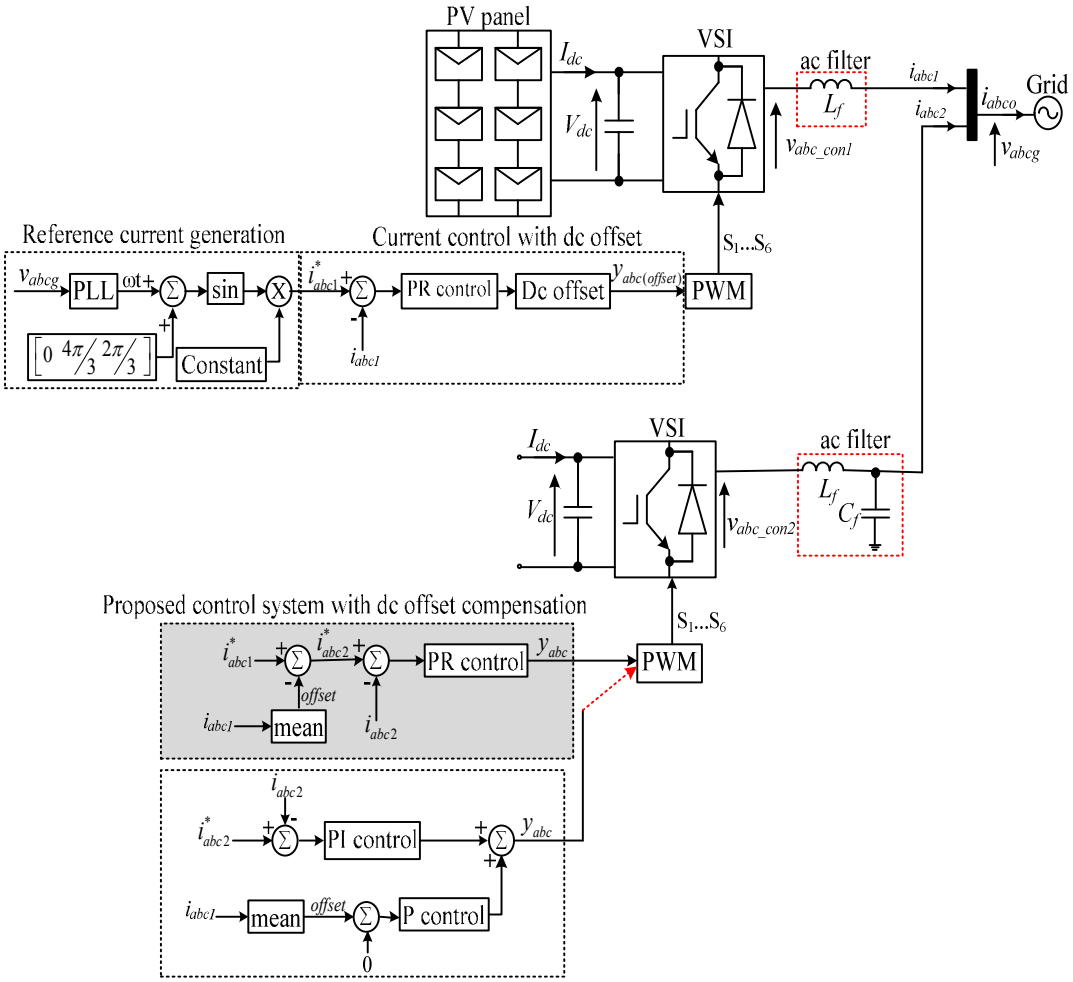


Figure 0.9: Proposed dc current offset compensation control system.

7.4. Simulation result

To demonstrate the effectiveness of the proposed dc current offset compensation technique presented in this thesis, the test system comprises of two grid-connected inverters (label'1' and '2') connected to the same bus as shown in Figure 0.9. Both inverters 1 and 2 are operated under current control mode, where inverter 1 mimics output currents of the solar farm that contains dc current component in either one or all of the phases. Injection of the dc offsets with unknown magnitudes into the output currents of inverter 1 is achieved by adding dc offsets to the modulating signals produced by the current controller. The output currents of inverter 1are used to extract the dc components in each phase that are used as feedback signals to the dc offset controller of inverter 2. The aim of the dc offset controller in inverter 2 is to suppress dc offset to zero in the output currents before entering the main interfacing transformer that

connects both inverters to the grid. The parameters used in the simulations are listed in Table 0.2. Two configurations have been simulated, while only one configuration has been used for experimental validation. The first configuration uses two voltage source inverters: one creates a dc offset and the second performs dc offset compensation. The second configuration uses the current source inverter for offset compensation. However, experimental validation is carried out for the first configuration only.

Table 0.2: Parameters used in the simulations.

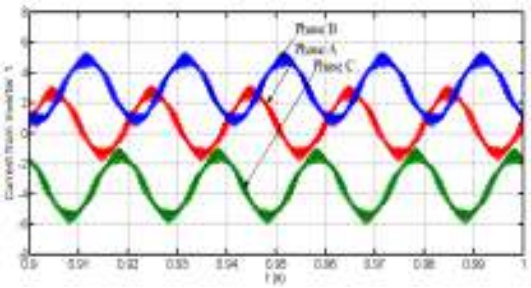
Parameters		Configuration I		Configuration II	
		Values			
DC-link voltage, V_{dc}	V	300	300	350	-
DC-link current, I_{dc}	A	-	-	-	10
Power capability, S	VA	1000	1000	1000	1000
Switching frequency, f_{sw}	Hz	2100	2100	2100	2100
Grid voltage per phase, V_g	V	110	110	110	110
Filter inductor of inverter 1, L_{f1}	mH	20	-	20	-
Filter capacitor of inverter 1, C_{f1}	µF	-	-	-	-
Filter inductor of inverter 2, L_{f2}	mH	-	10	-	3
Filter capacitor of inverter 2, C_{f2}	µF	-	70	-	150
Proportional gain of PR control, K_p	Ω	4	8	8	0.5
Integral gain of PR control, K_i	Ωs^{-1}	900	1200	650	50

6.4.1. Configuration I: Combination of VSIs

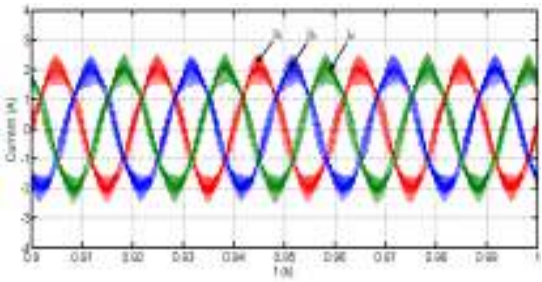
Figure 0.10 shows simulation results of inverter 1 when acting as an inverter that contains some dc current offset. The reference current, i^*_{abc1} is set at 2A with dc current offsets injected into each phase. The dc current offsets are 5%, 10% and -5% of the fundamental current, and are injected into phases *a*, *b* and *c* respectively. Figure 0.10(a) illustrates the phase current with injected dc current offsets. Figure 0.10(b) is the fundamental phase current and dc offset components are shown in Figure 0.10(c). The modulating signals of inverter 1 are shown in Figure 0.10(d).

The currents and voltages of inverter 2 are shown in Figure 0.11 (a) to (g). Using the proposed dc compensation strategy in Figure 0.9, the reference current in inverter 2, i^*_{abc2} is generated from i^*_{abc1} of inverter 1 adding the extracted dc offset from the output

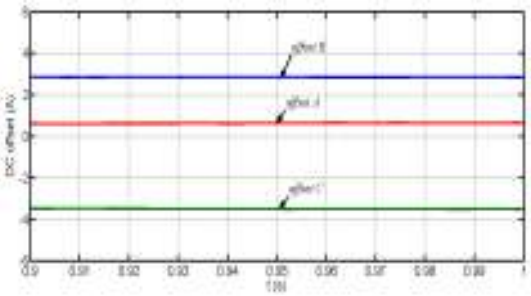
current of inverter 1, i_{abc1}. The output currents of inverter 2, i_{abc2} with their respective references, i^*_{abc2} are shown in Figure 0.11(a). Figure 0.11(b) to (d) compare the phase current of inverter 2 (i_{abc2}) with reference of i_{abc1}. i_{abc2} is the inverse of i_{abc1}, with the same amount of dc offset. Adding both i_{abc1} and i_{abc2} eliminates the dc offset, resulting in sinusoidal output current, i_{abco}. The modulating signals and the resultant output currents are shown in Figure 0.11(e) and (f) respectively while the grid voltage is illustrated in Figure 0.11(g).



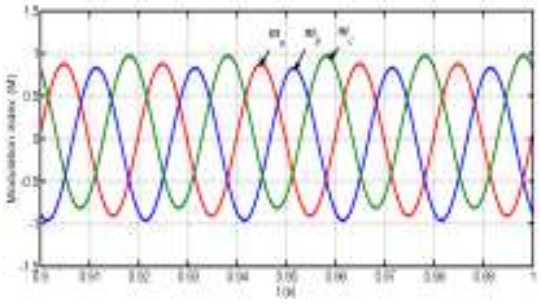
(a) Inverter 1three-phase output currents, including dc offsets



(b) Fundamental output current of inverter 1(when dc component is filtered)

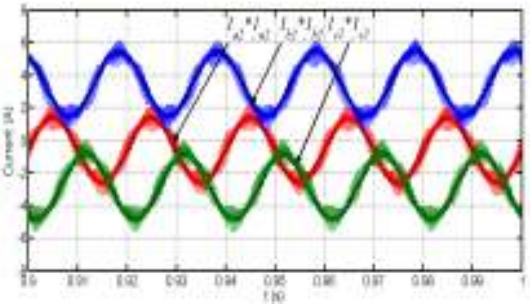


(c) DC offset components of the three phases

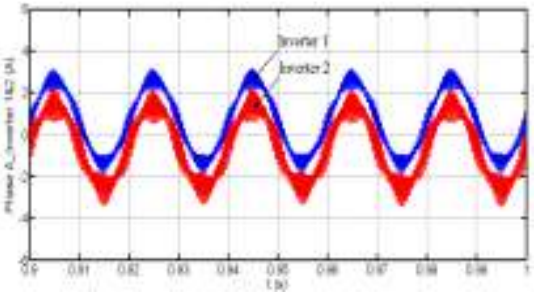


(d) Modulating signals of inverter 1 when dc offsets of 5%, 10% and -5% are injected

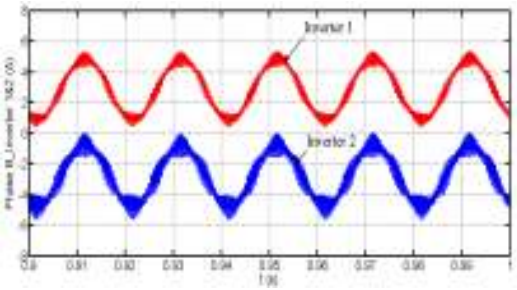
Figure 0.10: Simulation results of configuration I showing inverter 1 is mimicked an inverter that contains dc current offset components in its output current.



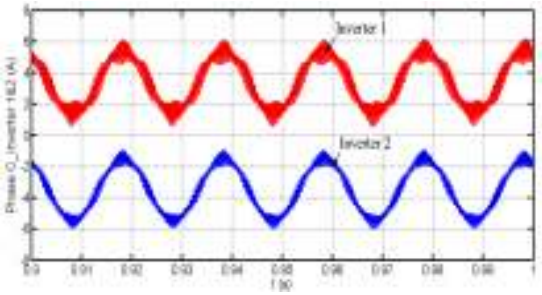
(a) Inverter 2 three-phase output currentsand their corresponding reference currents



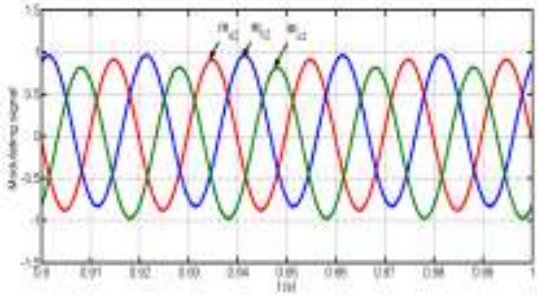
(b) Comparison of phase A current from inverters 1 and 2



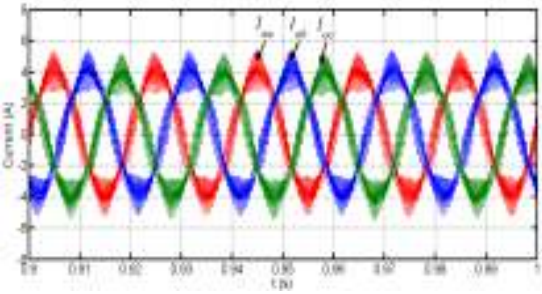
(c) Comparison of phase B current from inverter 1 and 2



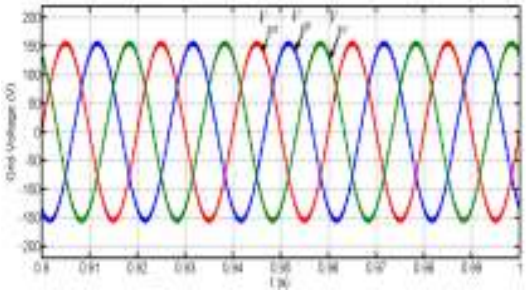
(d) Comparison of phase C current from inverter 1 and 2



(e) Modulating signals of inverter 2



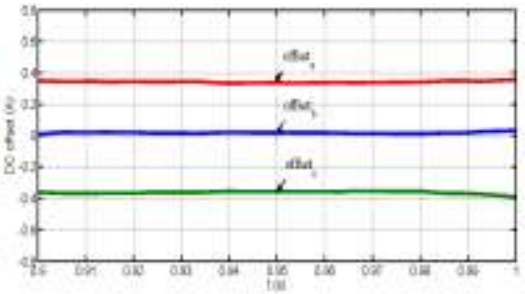
(f) Compensated three-phase output currents entering interfacing transformer



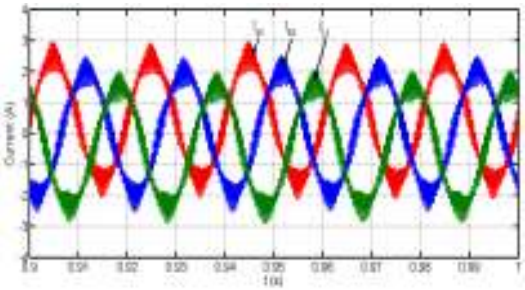
(g) Grid voltage

Figure 0.11: Simulation results of configuration I showing a VSI as a dc compensation inverter.

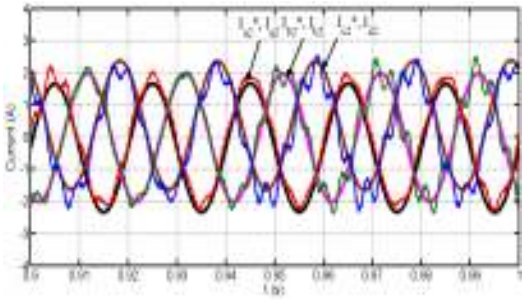
6.4.2. Configuration II: VSI and CSI combination



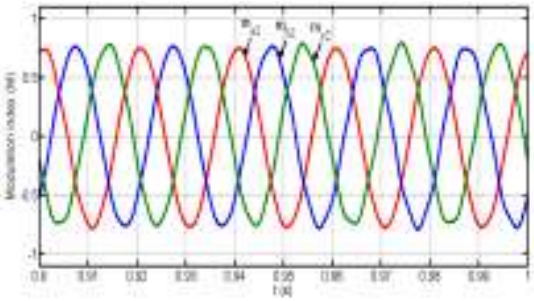
(a) DC offset componentof the three phases



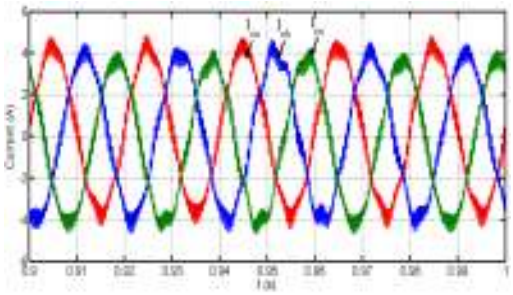
(b) Inverter 1 output current



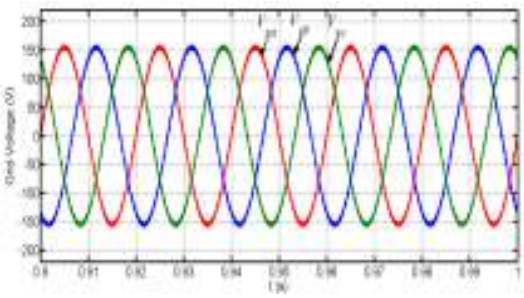
(c) Inverter 2 three-phase output currents and their respective reference currents



(d) Modulating signals of inverter 2

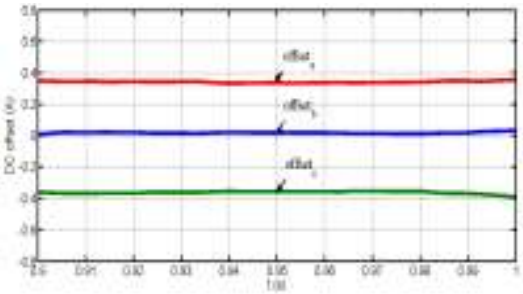


(e) Compensated three-phase output currents entering interfacing transformer

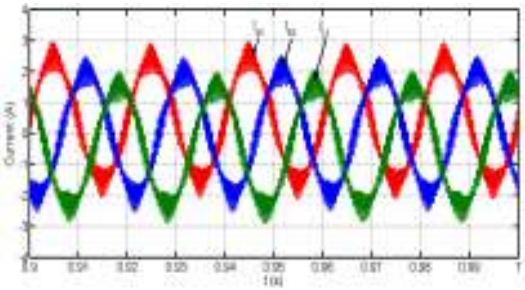


(f) Grid voltage

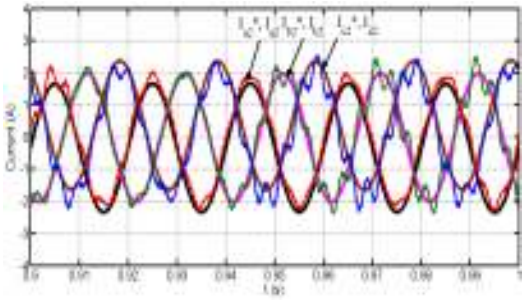
Figure 0.12(a) to (f) show simulation results for configuration II where the VSI mimics an inverter with a dc current offset component while the CSI is the dc current compensation inverter. The results shown in Figure 0.11 confirm that configuration I with a VSI as a dc current compensation inverter is superior, being able to compensate a higher level of dc offset while retaining balanced ac output currents. When a CSI is used as the dc compensation inverter, similar levels of dc offset as in Figure 0.10(c) are not achievable since instability and very poor dynamic performance results.



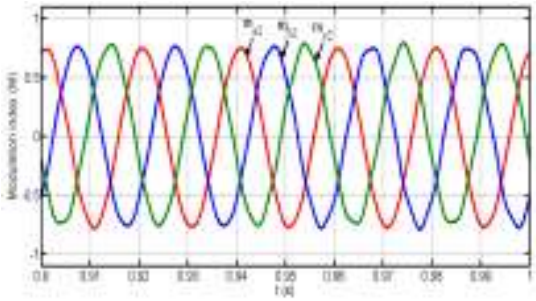
(g) DC offset componentof the three phases



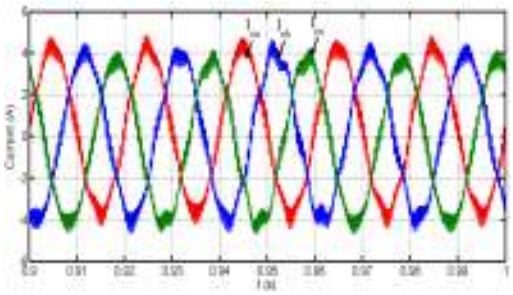
(h) Inverter 1 output current



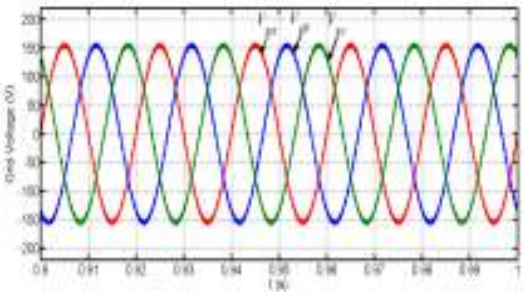
(i) Inverter 2 three-phase output currents and their respective reference currents



(j) Modulating signals of inverter 2



(k) Compensated three-phase output currents entering interfacing transformer



(l) Grid voltage

Figure 0.12: Simulation results for configuration II showing CSI as a dc compensation inverter.

7.5. Experimental verification

The parameters used in the experimental validation are listed in Table 0.3, and Figure 6.13 and 6.14 illustrate the practical implementation of the proposed dc compensation technique using configuration I.

Table 0.3: Experimental Parameters.

Parameters		Inverter 1	Inverter 2
		Values	
DC-link voltage, V_{dc}	V	200	200
Power capability, S	VA	1000	1000

Switching frequency, f_{sw}	Hz	4200	4200
Line-to-line grid voltage, V_g	V	86.6	86.6
Filter inductor of inverter 1, L_{f1}	mH	20	-
Filter capacitor of inverter 1, C_{f1}	μF	-	-
Filter inductor of inverter 2, L_{f2}	mH	-	10
Filter capacitor of inverter 2, C_{f2}	μF	-	70
Proportional gain of PR control, K_p	Ω	1.2	0.8
Integral gain of PR control, K_i	Ωs^{-1}	180	144

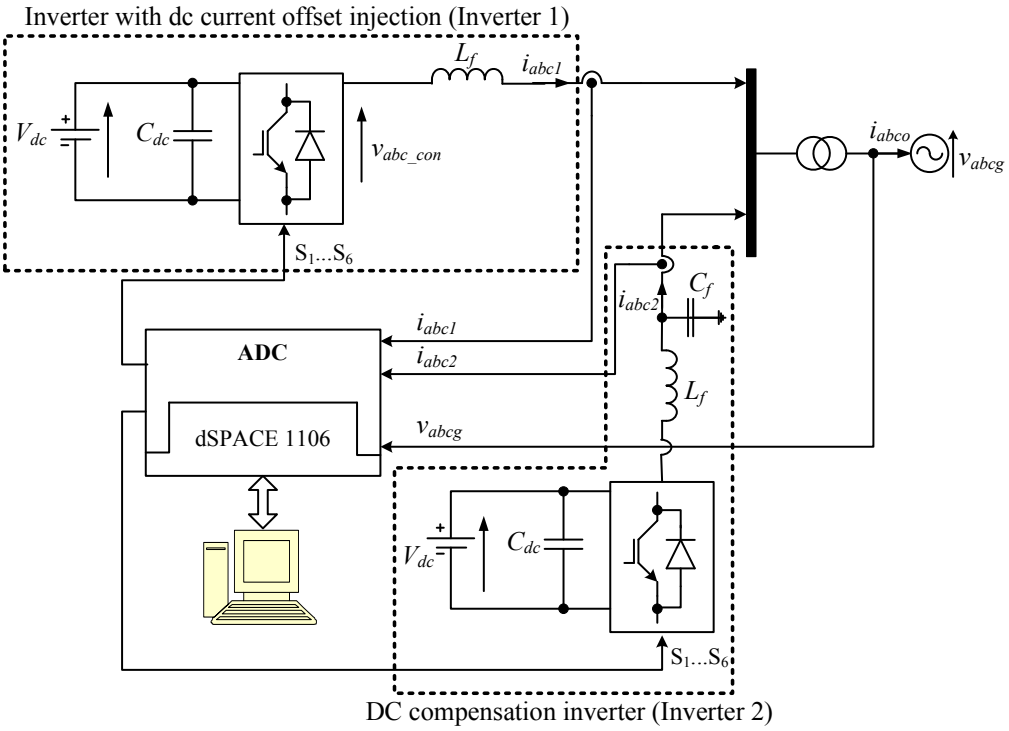


Figure 0.13: Hardware diagram of test-rig

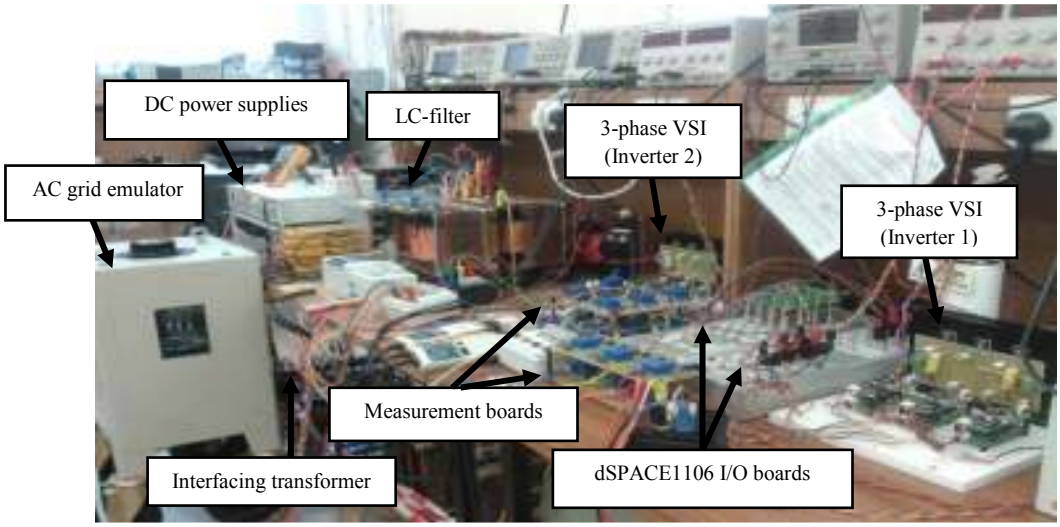
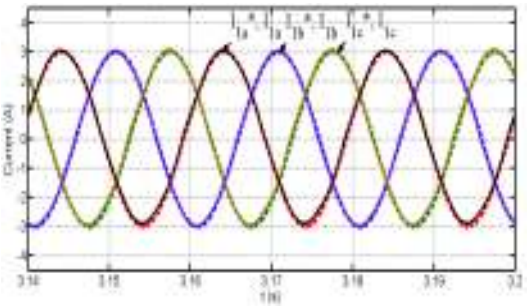


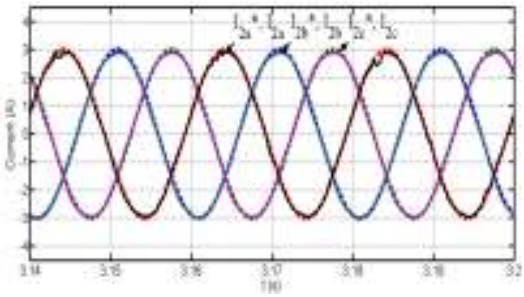
Figure 0.14: Experimental test rig setup of grid-connected inverters in parallel arrangement.

6.5.1. Experimental results: inverters 1 and 2 without dc offset injection

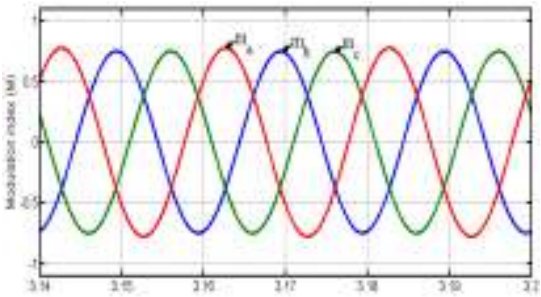
Figure 0.15(a) to (h) show the experimental results when inverters 1 and 2 operate in a parallel arrangement, with both injecting power into the grid, using one interfacing transformer. These results show that both inverters are able to operate satisfactorily and produce clean sinusoidal output currents. Figure 0.15(a) and (b) display inverters 1 and 2 output currents superimposed over their corresponding references currents, with currents of 3A per phase. The modulating signals for both inverters are stable as shown in Figure 0.15(c) and (d). Figure 0.15(e) and (f) show the three-phase output currents from inverters 1 and 2. The resultant three-phase output currents of the two inverters entering the interfacing transformer, and grid voltage are displayed in Figure 0.15(g) and (h) respectively.



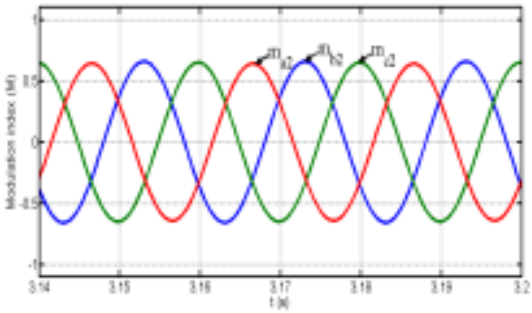
(a) Inverter 1currents with their corresponding references



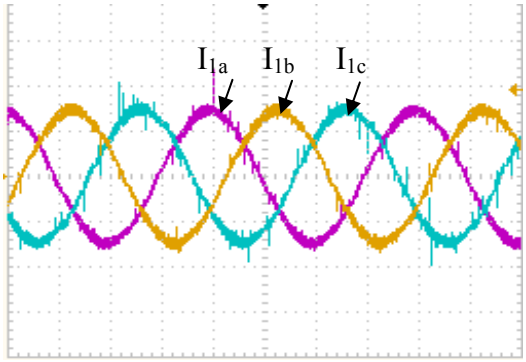
(b) Inverter 2 currents with their corresponding references



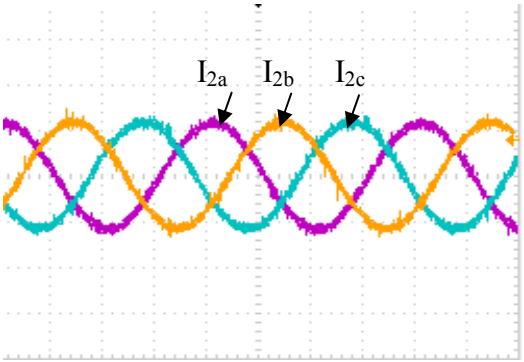
(c) Modulating signals of inverter 1



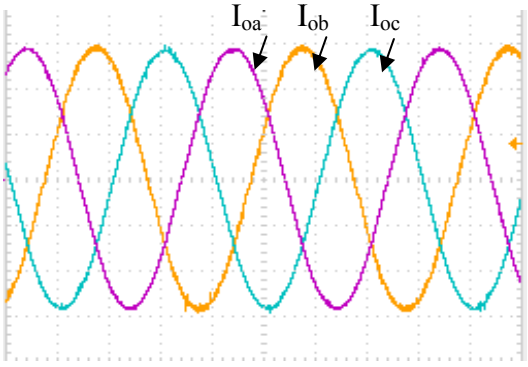
(d) Modulatingsignals of inverter 2



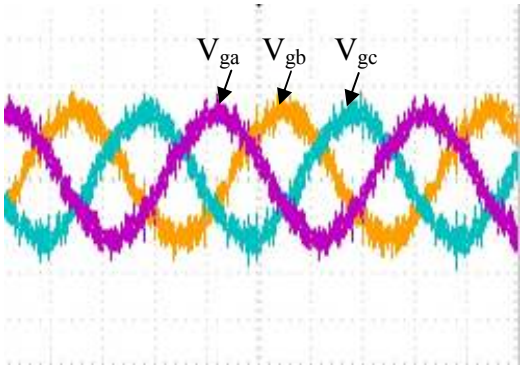
(e) Output phase current of inverter 1 (2A/div, 5ms)



(f) Output phase current of inverter 2 (2A/div, 5ms)



(g) Resultant output current (2A/div, 5ms)



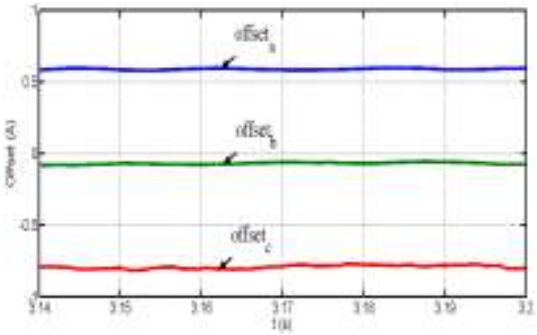
(h) Grid voltage (40V/div, 5ms)

Figure 0.15: Experimental results illustrating the current and voltage waveforms when two grid-connected VSIs exchange active and reactive power with the grid voltage without the introduction of dc current offset.

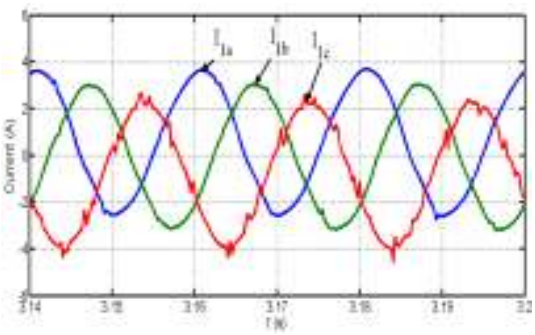
6.5.2. Experimental results: the proposed dc current compensation technique with different levels of dc current injected into the output of inverter 1

Figure 0.16 to 6.20 show the experimental results used to validate the proposed dc current compensation technique, with different current injection levels in the output of inverter 1. Inverter 2 performs the proposed dc compensation.

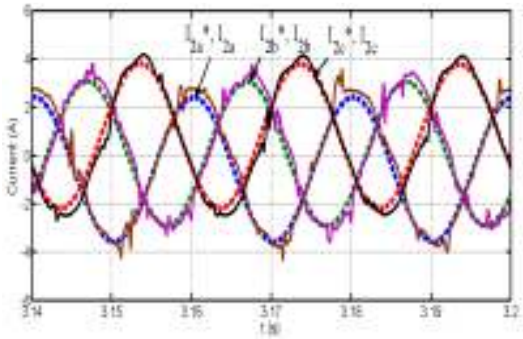
Figure 0.16 presents the experimental results when the dc components added into the modulating signals of the inverter 1 are adjusted randomly to give dc offsets of 19.6%, -2.67% and -26.67% in phases *a*, *b* and *c* (these percentage ratios are expressed with respect to a peak current of 3A). The results in Figure 0.16 (a) to (d) show the three-phase output currents of inverters 1 and 2, including the amount of dc offsets in the output currents of inverter 1 that need to be compensated, inverter 1 three-phase output currents, inverter 2 three-phase output currents superimposed on their reference currents, and the resultant output currents after compensation and seen by the coupling transformer. Figure 0.16(e) shows the grid voltage at the point of common coupling. These results show that the dc offsets in the output currents of inverter 1 are compensated by inverter 2, and results in sinusoidal output currents with near zero dc offset. These results are achieved despite a significant level of dc offset being injected into the output of inverter 1.



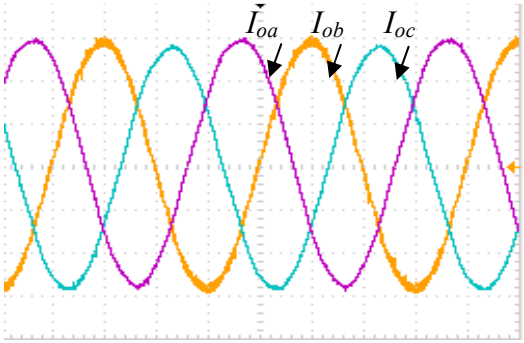
(a) DC current offset components of the three phases



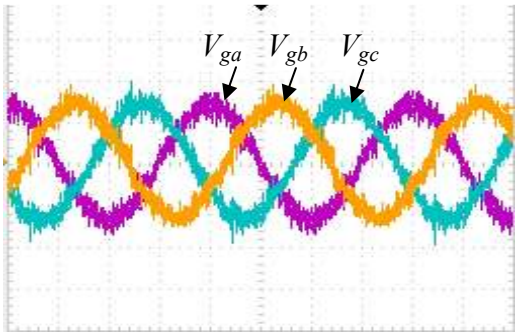
(b) Output phase current from inverter 1



(c) Output current from inverter 2 with their references

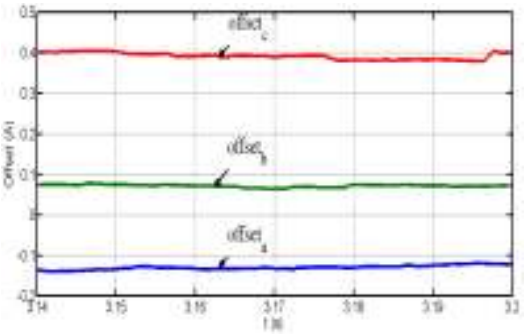


(d) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

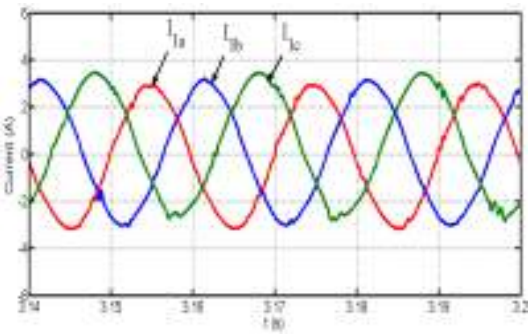


(e) Grid voltage (40V/div, 5ms)

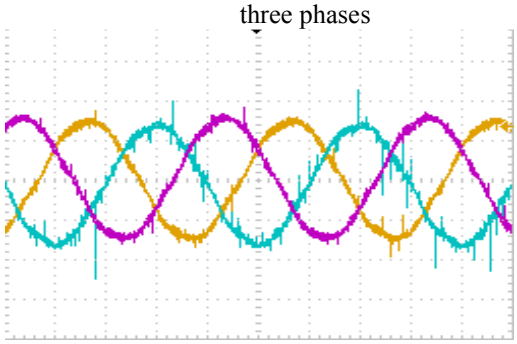
Figure 0.16: Experimental results demonstrating the practicability of the proposed dc offset compensation for grid connected inverters (Component of dc offsets injected relative to output current in each phase: *a*=0.59A, *b*=-0.08A and *c*=-0.8A).



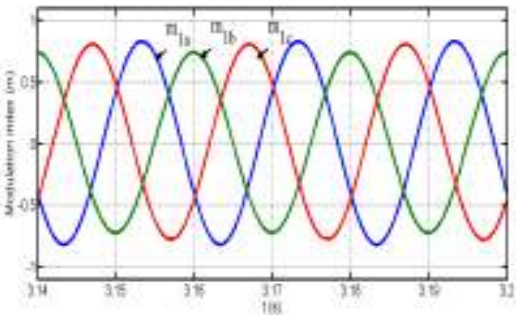
(a) DC current offset components of the three phases



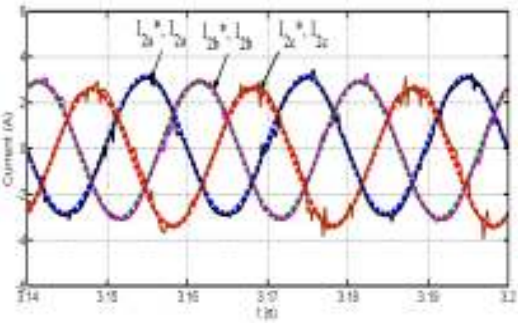
(b) Output phase current of inverter 1



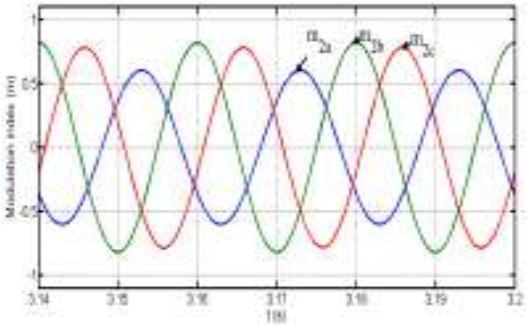
(c) Output phase current of inverter 1 (2A/div, 5ms)



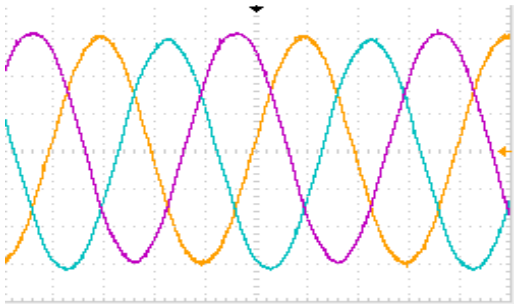
(d) Modulating signal of inverter 1



(e) Output current from inverter 2 with their references

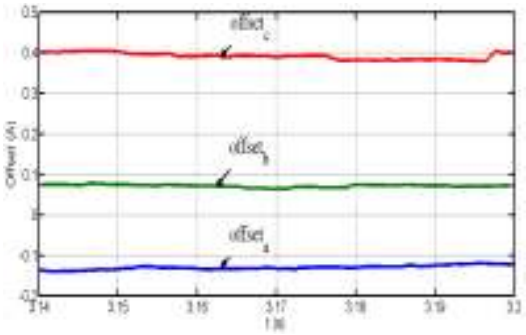


(f) Modulating signals of inverter 2

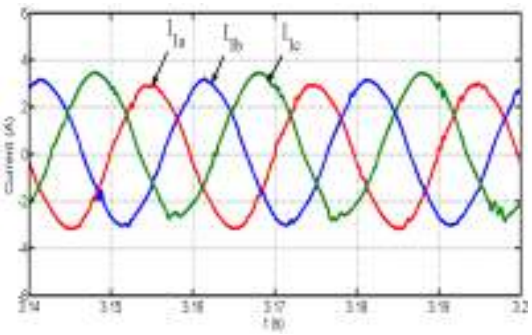


(g) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

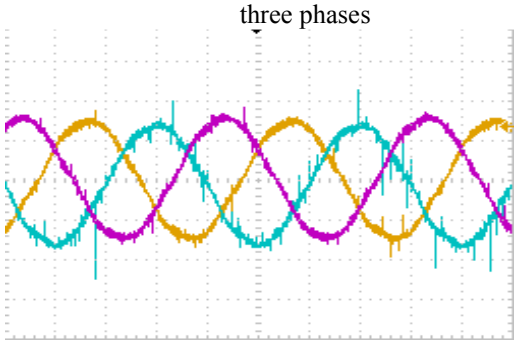
Figure 0.17 shows the experimental results when dc offsets of -4.7%, 2.3% and 13.3% relative to a peak phase current of 3A are injected into the output currents of inverter 1. These results are in agreement with the previous results presented in Figure 0.16 as inverter 2 is able to compensate the injected dc offsets.



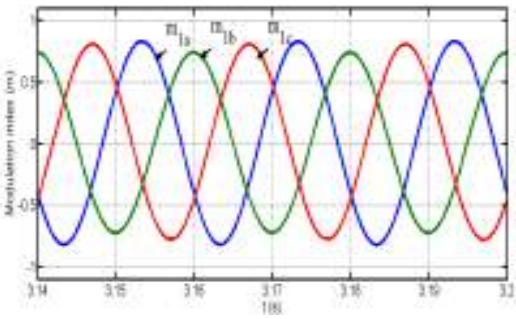
(h) DC current offset components of the three phases



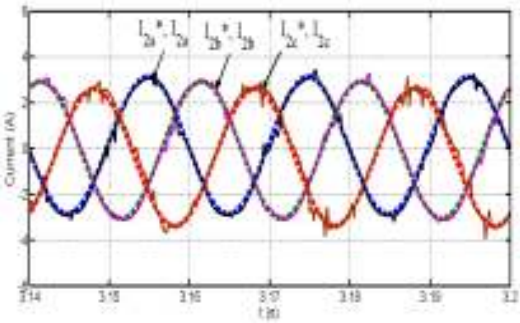
(i) Output phase current of inverter 1



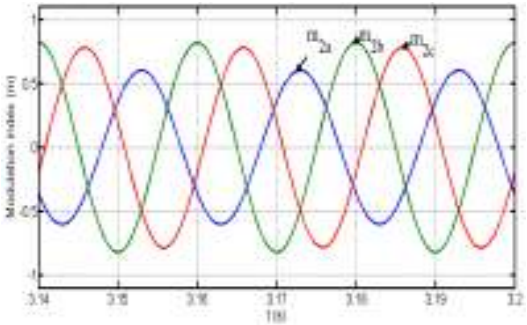
(j) Output phase current of inverter 1 (2A/div, 5ms)



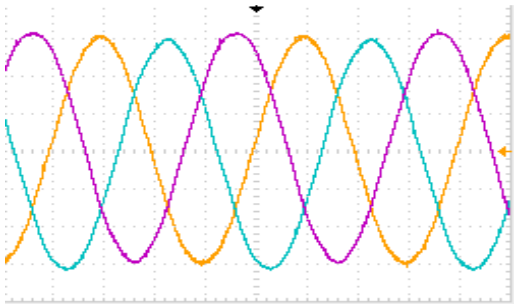
(k) Modulating signal of inverter 1



(l) Output current from inverter 2 with their references

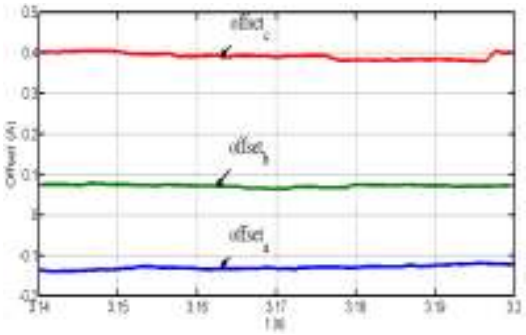


(m) Modulating signals of inverter 2

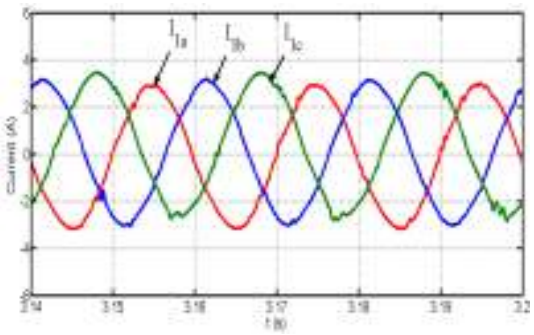


(n) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

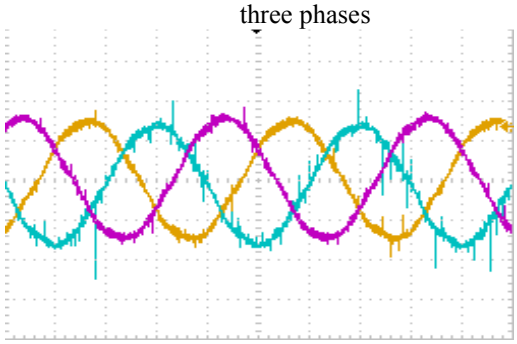
Figure 0.17 (d) shows that the modulating signals of inverter 1 contain the necessary dc component, while



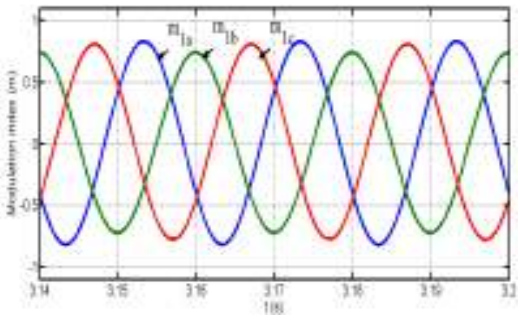
(o) DC current offset components of the three phases



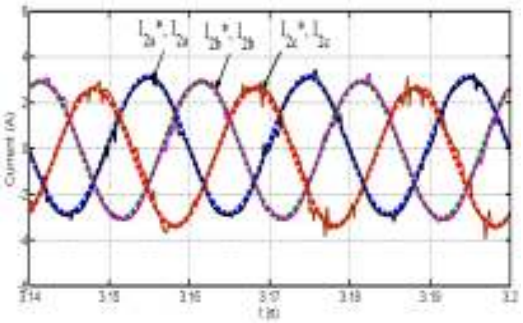
(p) Output phase current of inverter 1



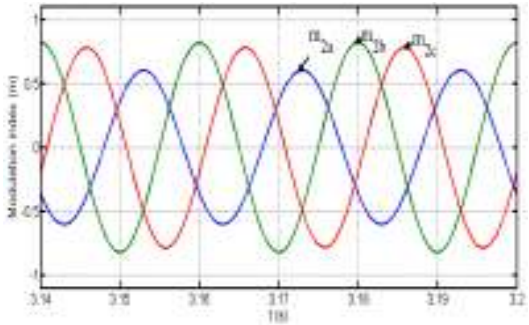
(q) Output phase current of inverter 1 (2A/div, 5ms)



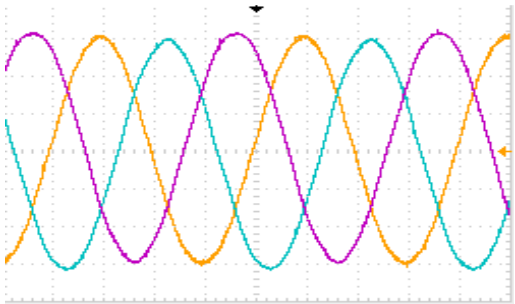
(r) Modulating signal of inverter 1



(s) Output current from inverter 2 with their references

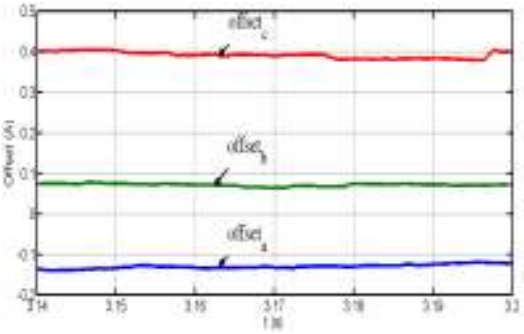


(t) Modulating signals of inverter 2

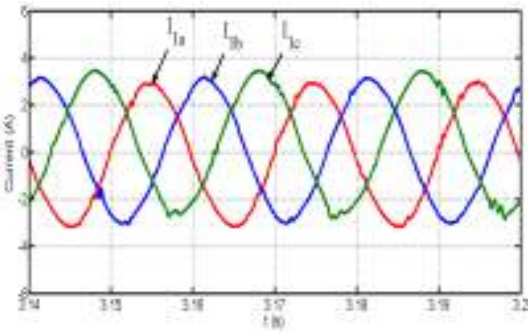


(u) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

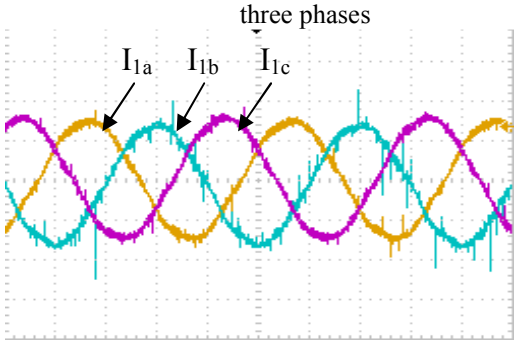
Figure 0.17(e) and (f) show the output current of inverter 2 used to counter the dc offset introduced by inverter 1 output. The resultant output phase currents entering the interfacing transformer are sinusoidal, meaning there is no risk of transformer dc saturation.



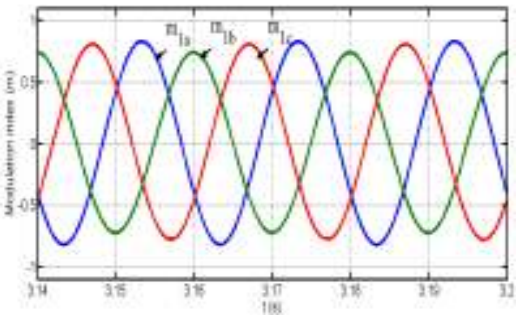
(v) DC current offset components of the three phases



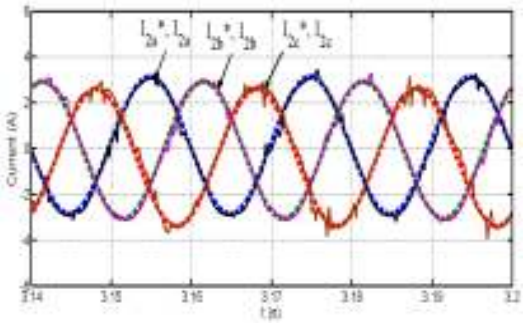
(w) Output phase current of inverter 1



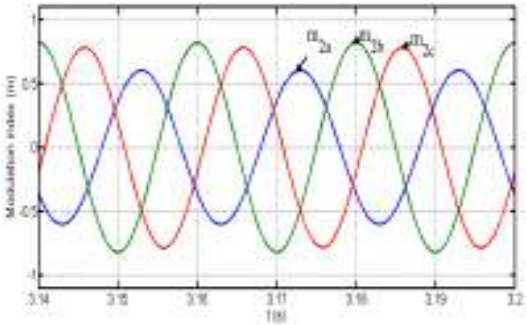
(x) Output phase current of inverter 1 (2A/div, 5ms)



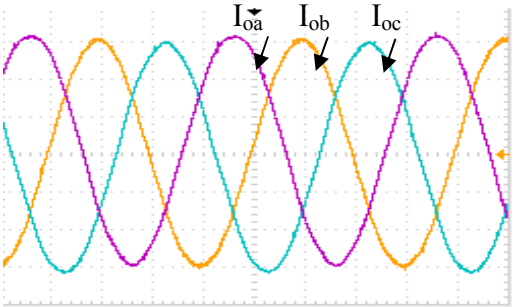
(y) Modulating signal of inverter 1



(z) Output current from inverter 2 with their references

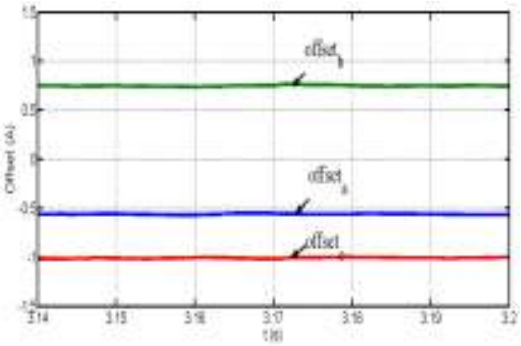


(aa) Modulating signals of inverter 2

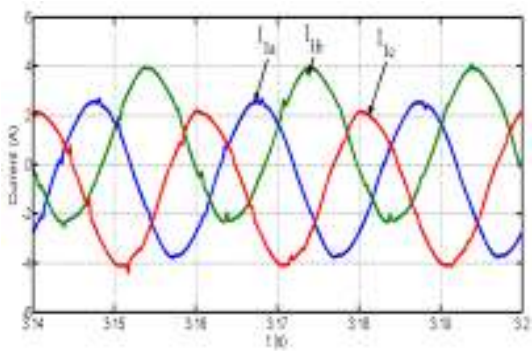


(bb) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

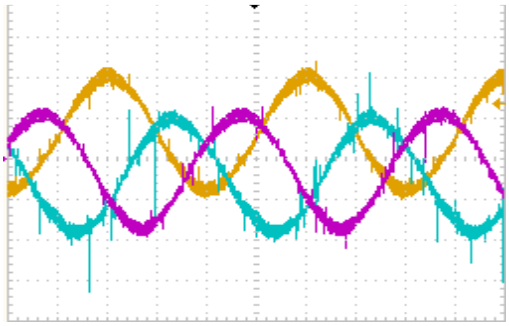
Figure 0.17: Experimental results demonstrating the practicability of the proposed dc offset compensation for grid connected inverters (Component of dc offsets injected relative to the output current in each phase: *a*=-0.14A, *b*=0.07A and *c*=0.4A).



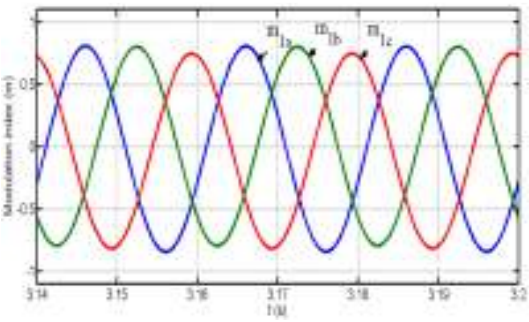
(a) dc current offset components of the three phases



(b) Output phase current from inverter 1

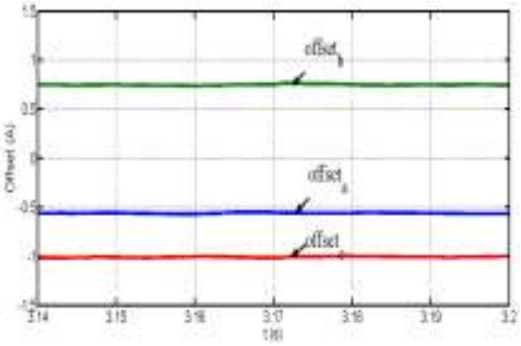


(c) Output phase current of inverter 1 (2A/div, 5ms)

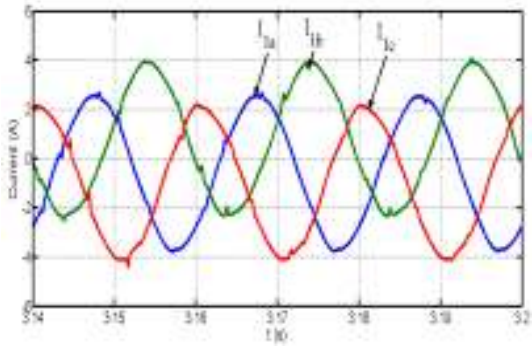


(d) Modulating signal of inverter 1

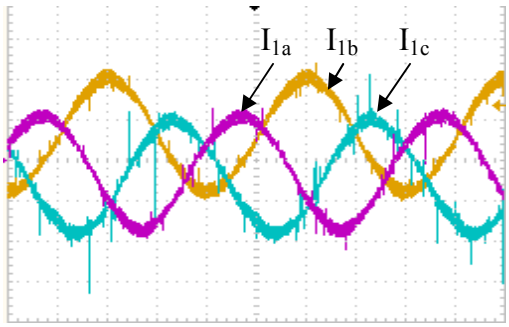
Figure 0.18 and 6.19 shows the results when relatively large dc current offsets are injected into the output phase currents of inverter 1 (-18.6%, 25% and -33.3% measured relative to the peak phase current of 3A). These results show that inverter 2 is able to compensate the high level of dc current injected into the output phase currents of inverter 1, as the resultant output phase currents entering the interfacing transformer become sinusoidal.



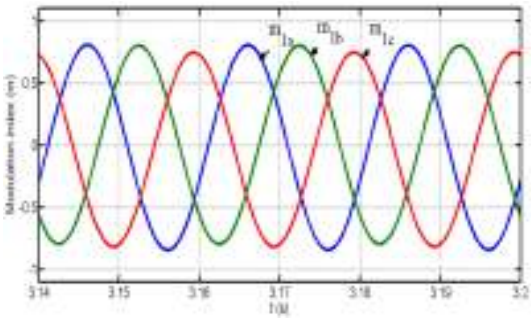
(e) dc current offset components of the three phases



(f) Output phase current from inverter 1

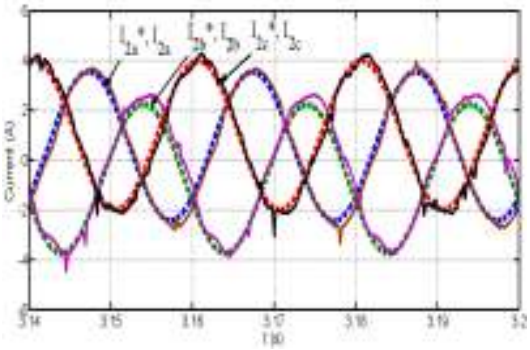


(g) Output phase current of inverter 1 (2A/div, 5ms)

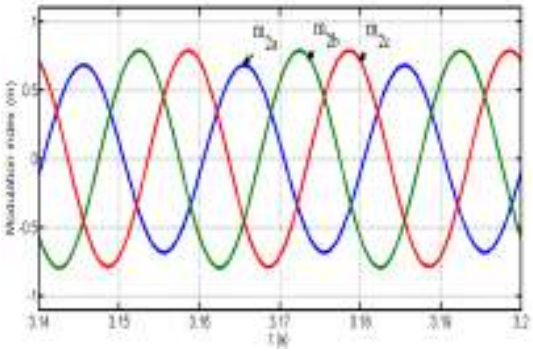


(h) Modulating signal of inverter 1

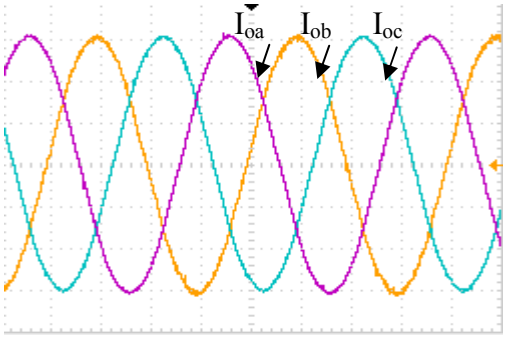
Figure 0.18: Experimental results demonstrating the practicability of the proposed dc offset compensation for grid connected inverters (Component of dc offsets injected relative to the output current in each phase: *a*=-0.56A, *b*=0.75A and *c*=-1A).



(a) Output current from inverter 2 with their references



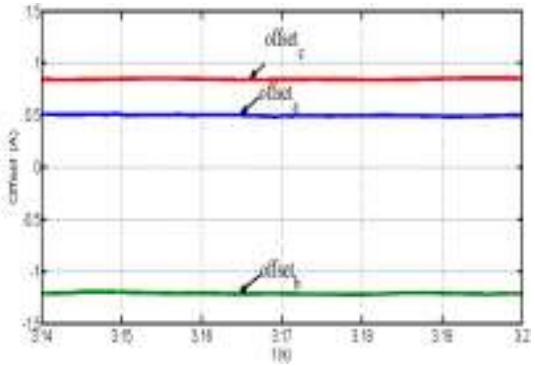
(b) Modulating signals of inverter 2



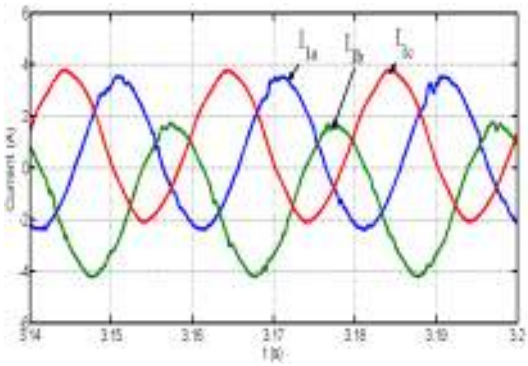
(c) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

Figure 0.19: Experimental results demonstrating the practicability of the proposed dc offset compensation for grid connected inverters (Component of dc offsets injected relative to the output current in each phase: *a*=-0.56A, *b*=0.75A and *c*=-1A).

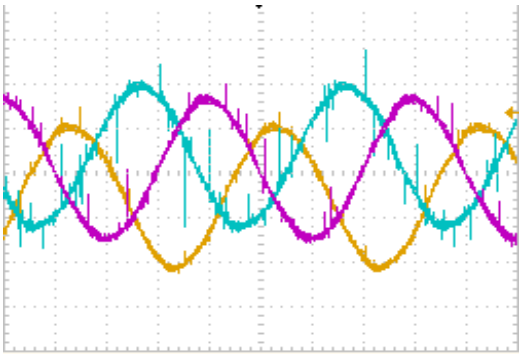
Experimental results with increasingly higher levels of dc injection (16.6%, -46.3% and 28.3% measured relative to the peak phase current of 3A) are shown in



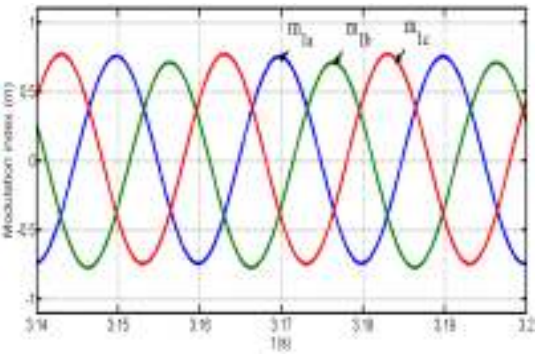
(a) dc offset components of the three phases



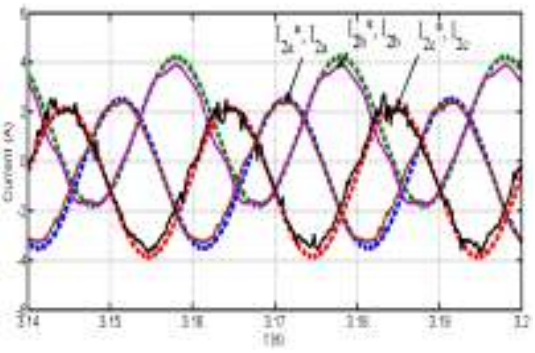
(b) Output phase current from inverter 1



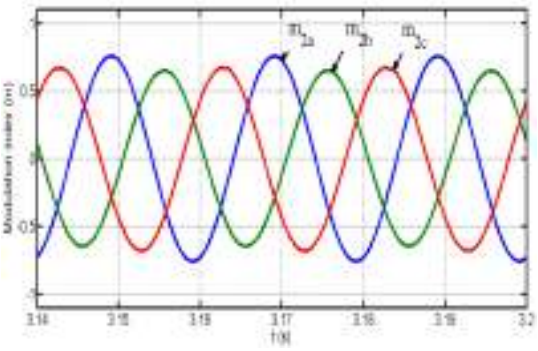
(c) Output phase current of inverter 1 (2A/div, 5ms)



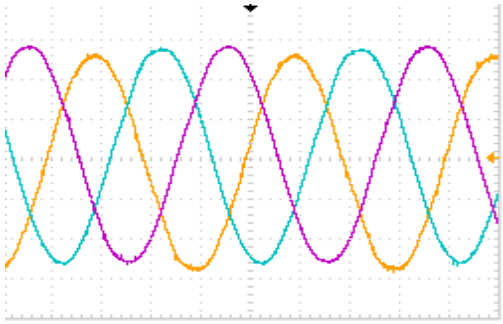
(d) Modulating signals of inverter 1



(e) Output phase current of inverter 2 with their corresponding references



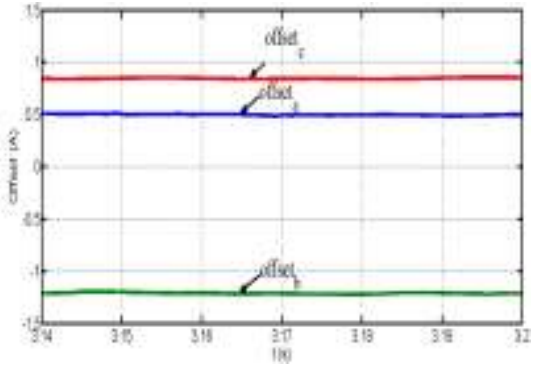
(f) Modulating signal of inverter 2



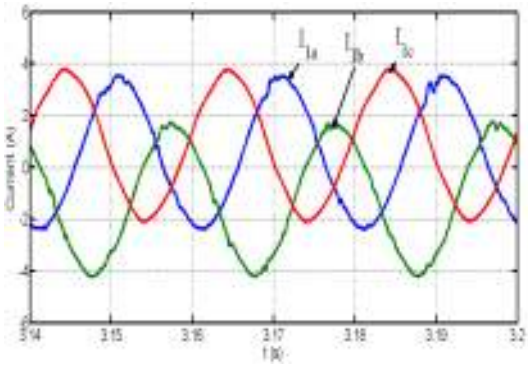
(g) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

Figure 0.20. These results show that the proposed technique is able to compensate such high levels of dc current in the output phases of inverter 1. The results in Figure 6.19 to

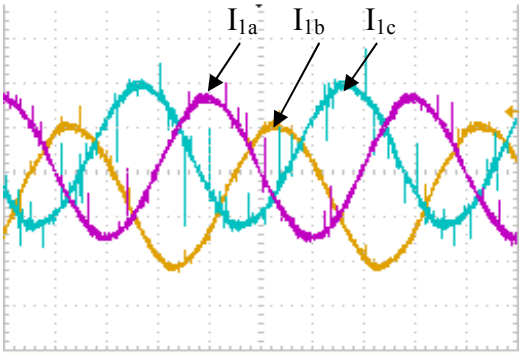
6.20 demonstrate the viability of the proposed technique, even in applications with relatively large dc components in the phase currents, as expected in a medium-scale solar farm with transformerless grid connected inverters.



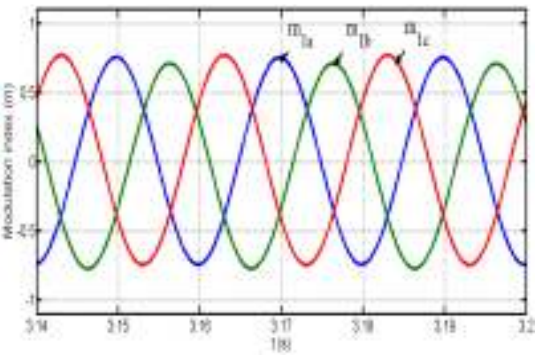
(h) dc offset components of the three phases



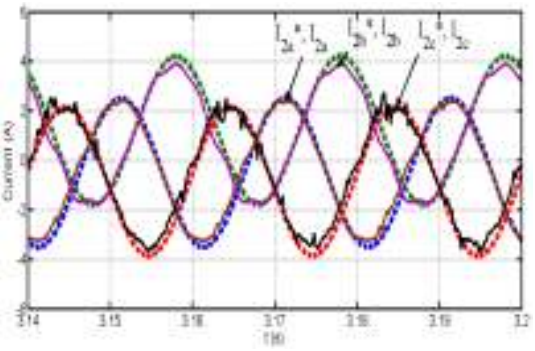
(i) Output phase current from inverter 1



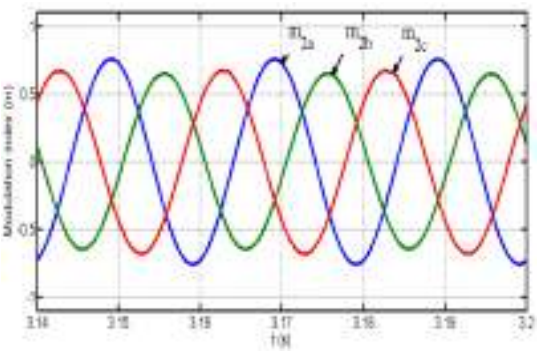
(j) Output phase current of inverter 1 (2A/div, 5ms)



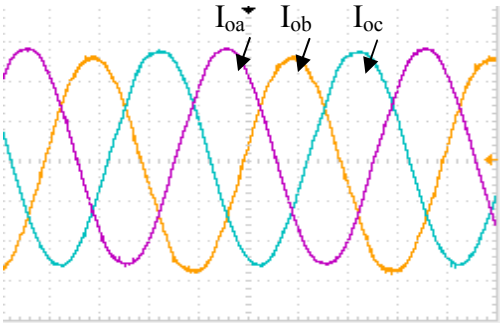
(k) Modulating signals of inverter 1



(l) Output phase current of inverter 2 with their corresponding references



(m) Modulating signal of inverter 2



(n) Compensated three-phase output currents entering interfacing transformer(2A/div, 5ms)

Figure 0.20: Experimental results demonstrating the practicability of the proposed dc offset compensation for grid connected inverters (Component of dc offsets injected relative to the output current in each phase: *a*=0.5A, *b*=-1.2A and *c*=0.85A).

7.6. Summary

This chapter discussed passive and active dc offset compensation techniques that claim to be applicable to minimize dc current injected into grid connected inverters. A new compensation technique is proposed which is applicable to medium-scale solar farms or any group of grid connected inverters confined within a relatively small area. This dc offset compensation technique exploits a simple proportional-resonance controller that aims to suppress dc offsets to zero in the output currents of grid-connected inverters before entering the main 50/60Hz interfacing transformer. At least one inverter is designated to perform dc offset compensation as well as its basic function of active power interfacing to the ac grid. The significance of this technique is it reduces the capital cost of a medium-scale solar farm since it enables transformerless operation of all inverters within the solar farm, and uses only one power transformer at the point of common coupling. Additionally, this technique does not rely on high-precision current measurement devices and does not use any form of complex transformer. To substantiate the proposed dc current compensation technique through simulation and experimentation, one inverter mimicked the output currents that contain dc current components in either one or all of the phases, while the second inverter performed the proposed dc compensation.

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Chapter Seven

Grid Integration of a Current Source Inverter

7.0. Introduction

The relevant attributes of the current source inverter for grid integration of photovoltaic systems are highlighted in chapter five, including discussions of their modulation techniques. This chapter presents the control structures needed to enable safe operation of current source inverters in grid mode, meeting all the relevant standards and grid code requirements. Additionally, the feasibility of the CSI to operate with a passive network with no generation, where the inverter needs to set the voltage (as in the case with the VSI and synchronous machines) during black-start is demonstrated. The discussion presented in this chapter shows that when a current source inverter is correctly controlled, it can provide all the flexibility needed for grid operation, including provision of leading and lagging reactive power needed for voltage support and survival during low-voltage ride-through. However, the issues related to low-voltage fault ride-through are not discussed in this chapter. This chapter also presents simulations and experimentation that demonstrates the suitability of the direct regular sample PWM as proposed in chapter five, for grid application.

7.1. Background

Distributed power generation based on renewable sources is experiencing fast growth and development worldwide, especially in countries such as China, United States, Germany and Japan [7.1]. Grid connected inverters play an important role in the integration of distribution generation onto ac grids. Such integration is governed by strict grid codes, which include the control of active and reactive power, permissible levels of harmonics, and other power quality aspects. Among two basic inverter technologies available, the current source inverter (CSI) is perceived to be suitable for grid integration of multi-megawatt wind turbines and photovoltaic systems [7.2, 4-7].

For example, the CSI provides a simple topological solution and satisfactory performance in grid mode, giving sinusoidal current, fully controlled power factor, and natural protection against dc side short-circuit faults.

Although, as yet, the CSI does not play a major role as a grid interfacing unit in distributed generation systems, it is a proven approach in high power, medium voltage ac drives systems with ac voltages of 2.3kV to 13.8kV [7.8, 9]. It is estimated that a minimum of 700 units of large CSI-fed drives are annually produced worldwide [7.10]. The features of a simple converter structure, low switch count, low *dv/dt* and reliable over-current/short circuit protection make the CSI competitive compared to the voltage source inverter (VSI) and the multilevel inverter.

In a photovoltaic system, the CSI has been advocated as a means of improving the effectiveness of maximum power-point tracking (MPPT), as the number of series connected PV in each string is reduced [7.11]. This reduces the impact of partial shading, and increases system efficiency by using one conversion stage instead of two, therein benefiting from the voltage boost capability of the CSI[7.12-18].

The single-phase CSI for photovoltaic grid integration is proposed in [7.11-14, 17, 18] which introduce various transformerless topologies to minimize the common-mode current that arises through the stray capacitance between the PV array and ground. Also, the proposed single-phase topologies need to cater for even harmonics on the dc side [7.17, 18]. These need to be eliminated since they affect MPPT, reduce PV inverter lifetime, and are associated with odd harmonics on the grid side.

It is advantageous to use a three-phase system instead of single-phase one because there are no even harmonics or 3rd harmonic on the grid side. Several applications of three-phase CSI in photovoltaic systems are proposed in [7.15, 16, 19, 20]. Analysis and modelling of a grid connected CSI, using PI control in the *dq*-frame and carrier-based SPWM, are presented in [7.15]. However, the controller only consists of a current control loop, which affects system reliability.

In [7.16], the proposed system consists of only one control loop for maximum power point tracking, and is claimed to produce an ac output current with a total harmonic distortion (THD) of 4.5%. However, with varying weather conditions, an output current control loop is important to limit the current and quickly recover the grid current variation. In [7.19], a modified carrier-based SPWM technique is proposed which adds a short-circuit pulse to the conventional SPWM to prevent an open-circuit CSI at any instant, and which is useful in adjustment of the PV-array voltage. Although a simple MPPT control structure is introduced, limited experimental results and information on the control system are presented [7.19].

In this chapter, a single-stage grid connected PV system based on a three-phase CSI is proposed. The control system uses the proposed direct regular-sampled pulse width modulation (DRSPWM) technique to regulate active and reactive power exchanges with the ac grid under various operating conditions, giving an ac output current with acceptable THD according to the IEEE 929-2000 standard for utility interfacing of photovoltaic systems [7.21].

7.2. Control system in island and grid modes

In principle, a CSI injects its output active and reactive power into the grid, assuming the grid is sufficiently large and able to absorb the injected powers without affecting its power balance [7.1, 22, 23]. In this mode, the grid dictates the ac voltage and frequency, while the CSI is seen as a slave that uses a phase locked loop to synchronize with the grid and manipulate its output currents relative to the grid voltage to achieve the desired active and reactive power exchange[7.24]. Whilst in an islanding mode, the CSI operates as a static synchronous generator that needs to set the ac frequency and gradually build-up its output voltage from 0 to rated voltage. It then establishes a stiff ac bus, where the loads are connected. During black start and operation in islanding mode, the CSI is controlled in a voltage mode where it sets the ac voltage.

7.2.1. Voltage control in island operation

The inverter voltage controller in island mode controls both the frequency and the quality of the output voltage supplied to the load. Two voltage control methods are considered for the three-phase CSI. These are proportional-resonant control in the *abc* frame, and proportional integral control in the synchronous reference *d-q* frame.

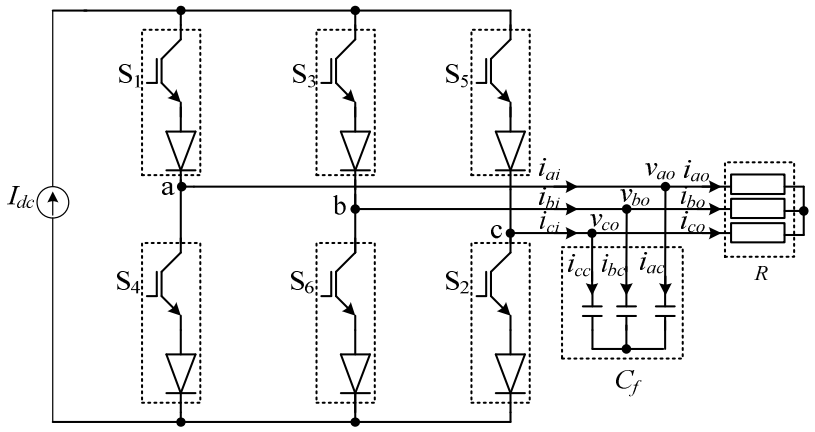


Figure 0.1: Circuit diagram of CSI in island mode.

A. Proportional-integral control in the abc frame

Figure 0.1illustrates a power circuit of a three-phase CSI connected to a passive load. From Figure 0.1, the dynamic equations that describe the CSI in the *abc* frame for island mode of operation are:

$$\frac{dv_{abco}}{dt} = \frac{i_{abci} - i_{abco}}{C_f} \tag{7.30}$$

$$v_{abco} = Ri_{abco} \tag{7.31}$$

Let

$$u = i_{abci} - i_{abco} \tag{7.32}$$

where v_{abco}, i_{abci} and i_{abco} represent the output voltages, inverter currents and load currents respectively, while C_f and R are the filter capacitance and the load resistance.

Figure 0.2 illustrates a proportional-resonant controller in the *abc* frame that is used to control the output voltage. The controlled variables are independent between phases, hence this controller can be applied to single and three phase systems.

The PR controller transfer function in (7.33) is discretized using a forward Euler method for DSP implementation, where discretization details are presented in chapter four (equations 4.21 to 4.27).

$$y = k_p e + \int \left(k_i e - \int \omega_o^2 z dt \right) dt \tag{7.33}$$

From (7.30) and (7.32), whilst including the output voltage error into the PR controller, u is obtained from (7.33):

$$u = k_{pv} \left(v_{abco}^* - v_{abco} \right) + \int \left(k_{iv} \left(v_{abco}^* - v_{abco} \right) - \int \omega_o^2 z_v dt \right) dt \tag{7.34}$$

Substituting (7.34) into (7.30)

$$\frac{dv_{abco}}{dt} = \frac{k_{pv} v_{abco}^*}{C_f} - \frac{k_{pv} v_{abco}}{C_f} + \frac{z_v}{C_f} \tag{7.35}$$

where

$$z_v = \int \left(k_{iv} \left(v_{abco}^* - v_{abco} \right) - w_v \right) dt \tag{7.36}$$

and

$$w_v = \int \omega_o^2 z_v dt \tag{7.37}$$

The derivatives of (7.36) and (7.37) are:

$$\frac{dz_v}{dt} = k_{iv} \left(v_{abco}^* - v_{abco} \right) - w_v \tag{7.38}$$

$$\frac{dw_v}{dt} = \omega_o^2 z_v \tag{7.39}$$

From (7.35), (7.38) and (7.39), the state space model of the voltage loop controller can be written in the form: $\frac{dx(t)}{dt} = Ax(t) + Bu(t)$

$$\frac{d}{dt}\begin{bmatrix} v_{abco} \\ z_v \\ w_v \end{bmatrix} = \begin{bmatrix} -\frac{k_{pv}}{C_f} & \frac{1}{C_f} & 0 \\ -k_{iv} & 0 & -1 \\ 0 & \omega_o^2 & 0 \end{bmatrix} \begin{bmatrix} v_{abco} \\ z_v \\ w_v \end{bmatrix} + \begin{bmatrix} \frac{k_{pv}}{C_f} \\ k_{iv} \\ 0 \end{bmatrix} v_{abco}^* \tag{7.40}$$

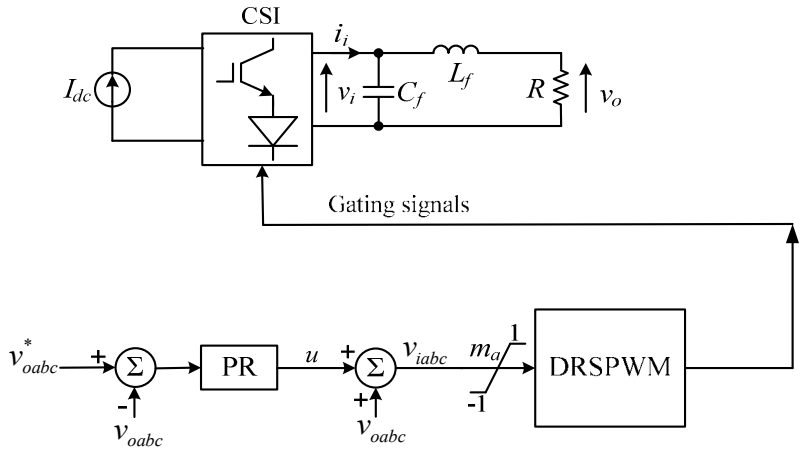


Figure 0.2: Control diagram of PR voltage controller for current source inverter.

B. Proportional-integral (PI) controller in island mode

The output voltage regulator is a PI controller in the synchronous rotating frame. The three-phase ac quantities are transformed into dc components in the *dq*-reference frame to eliminate steady-state error. This control system is illustrated in Figure 0.3. The stability is improved at the expense of response time and harmonic rejection. Referring to Figure 0.1, the dynamic equations in the *dq*-reference frame are:

$$\frac{dv_{od}}{dt} = \frac{1}{C_f}\left[i_{id} - i_{od} - \omega C_f v_{oq}\right] \tag{7.41}$$

$$\frac{dv_{oq}}{dt} = \frac{1}{C_f}\left[i_{iq} - i_{oq} + \omega C_f v_{od}\right] \tag{7.42}$$

To facilitate voltage regulator design, let

$$u_d = \frac{1}{C_f}\left(i_{id} - i_{od} - \omega C_f v_{oq}\right) \tag{7.43}$$

$$u_q = \frac{1}{C_f}\left(i_{iq} - i_{oq} + \omega C_f v_{od}\right) \tag{7.44}$$

The variables u_d and u_q can be obtained from the proportional-integral (PI) controller as follows:

$$u_d = k_p\left(v_{od}^* - v_{od}\right) + k_i \int \left(v_{od}^* - v_{od}\right)dt \tag{7.45}$$

$$u_q = k_p\left(v_{oq}^* - v_{oq}\right) + k_i \int \left(v_{oq}^* - v_{oq}\right)dt \tag{7.46}$$

where k_p and k_i are the proportional and integral gains of the voltage regulator in the d and q channels.

Replacing the integral parts in (7.45) and (7.46)with y_d and y_q, and substituting the resultant expressions(7.41) and (7.42), gives:

$$\frac{dv_{od}}{dt} = \frac{1}{C_f}\left[k_p v_{od}^* - k_p v_{od} + y_d\right] \tag{7.47}$$

$$\frac{dv_{oq}}{dt} = \frac{1}{C_f}\left[k_p v_{oq}^* - k_p v_{oq} + y_q\right] \tag{7.48}$$

$$\frac{dy_d}{dt} = k_i\left(v_{od}^* - v_{od}\right) \tag{7.49}$$

$$\frac{dy_q}{dt} = k_i\left(v_{oq}^* - v_{oq}\right) \tag{7.50}$$

Differential equations (7.47) to (7.50) can be re-arranged in state space form, $x'(t) = Ax(t) + Bu(t)$ as:

$$\frac{d}{dt}\begin{bmatrix} v_{od} \\ y_d \\ v_{oq} \\ y_q \end{bmatrix} = \begin{bmatrix} -\frac{k_p}{C_f} & \frac{1}{C_f} & 0 & 0 \\ -k_i & 0 & 0 & 0 \\ 0 & 0 & -\frac{k_p}{C_f} & \frac{1}{C_f} \\ 0 & 0 & -k_i & 0 \end{bmatrix} \begin{bmatrix} v_{od} \\ y_d \\ v_{oq} \\ y_q \end{bmatrix} + \begin{bmatrix} \frac{k_p}{C_f} & 0 \\ k_i & 0 \\ 0 & \frac{k_p}{C_f} \\ 0 & k_i \end{bmatrix} \begin{bmatrix} v_{od}^* \\ v_{oq}^* \end{bmatrix} \tag{7.51}$$

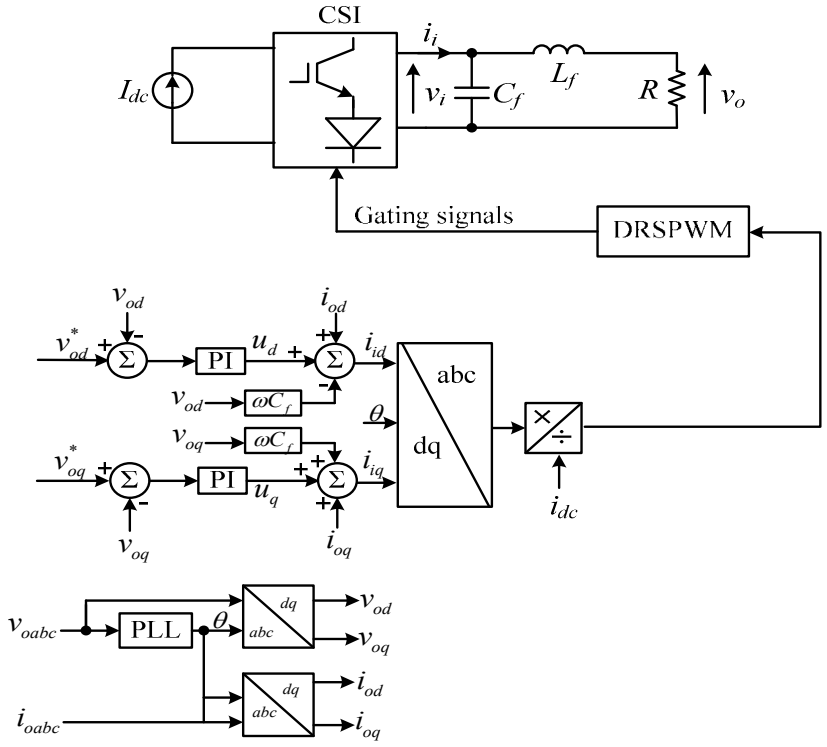


Figure 0.3: CSI control system in island mode using PI control in the*dq*-frame.

7.2.2. Simulation and experimental operational verification of the CSI in island mode

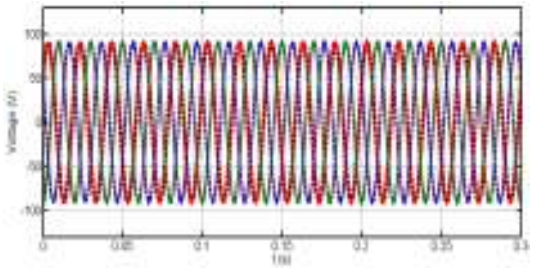
PR control in the *abc,* and PI control in the *dq*-frame for operation of a CSI in island mode are considered using simulation and experimentation analysis. The parameters used for simulation and experimental results are listed in Table 0.1.

Table 0.1: Parameters used in simulation and experimental investigation

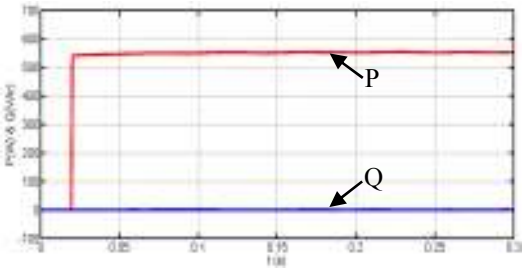
Parameters	Values
DC-link current (I_{dc})	8A
AC output voltage (V_o)	90V
Nominal frequency (f_o)	50Hz
Switching frequency (f_{sw})	2.1kHz
Capacitor filter (C_f)	70µF
Inductor filter (L_f)	3mH
Load (R)	22Ω

A. Simulation results

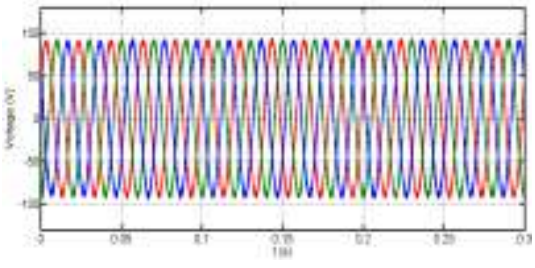
Figure 0.4 and 7.5 illustrate the voltage, power and current waveforms when a PR controller in the *abc* frame and a PI controller in the *dq*-frame, are used to control the CSI in island mode, respectively.



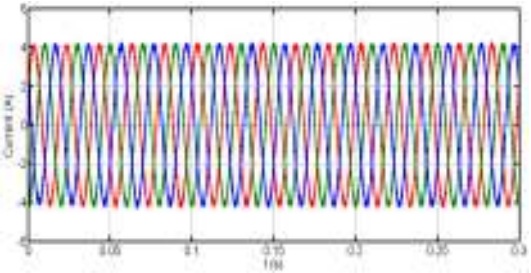
(a) Output voltages with their respective references



(b) Active and reactive power

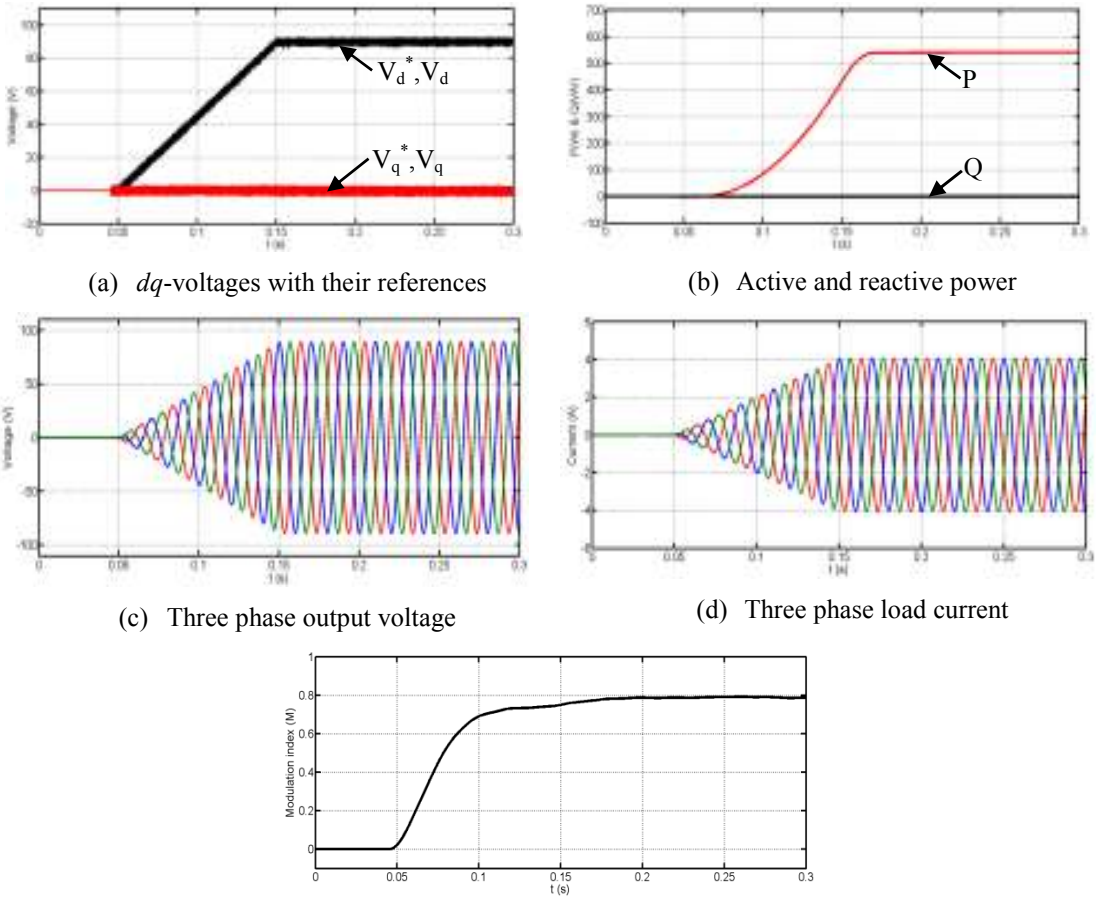


(c) Output voltage



(d) Load current

Figure 0.4: Simulation results illustrating a three-phase CSI in island mode using PR voltage-control in the *abc* frame.



(a) *dq*-voltages with their references

(b) Active and reactive power

(c) Three phase output voltage

(d) Three phase load current

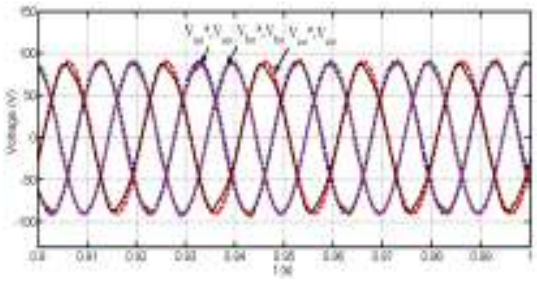
(e) Modulation index

Figure 0.5: Simulation results illustrating the three-phase CSI in island mode using *dq*-frame PI voltage-control.

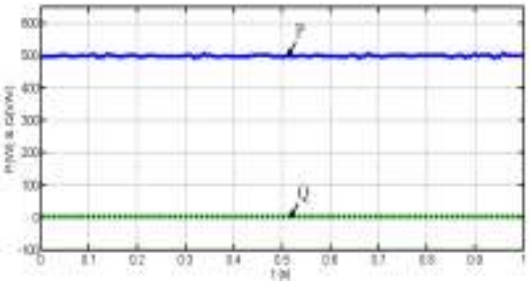
B. Experimental results

To verify the results in Figure 0.5, a laboratory test-rig with the parameters in Table 0.1 was implemented and the corresponding results are presented in Figure 0.6 to 7.8. Figure 0.6(a) to (c) are experimental results from the dSPACE1006 DSP-platform for the output voltages, active and reactive powers delivered to the load, and the respective modulating signals using the PR voltage controller in an *abc* frame. The output voltages using PI control in the *dq*-axes are compared to their corresponding references in Figure 0.7(a). With a dc-link current of 8A, the supplied active power to the load is nearly 500W while the reactive power is maintained at 0VAr, as demonstrated in Figure 0.7(b). Figure 0.8(a) and (c) show three-phase load voltages and currents and their respective magnification during transient and steady-state conditions. The modulation

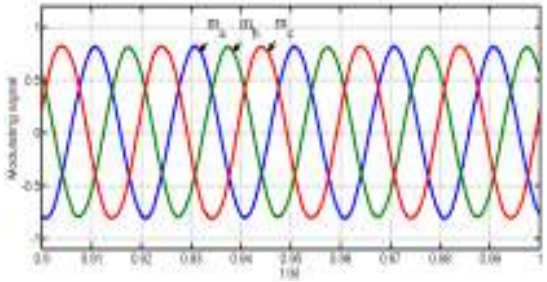
index plot is shown in Figure 0.8(c). Both controllers track their respective reference voltages and deliver the same active power to the load, with near unity power factor.



(a) Output voltages with their corresponding references

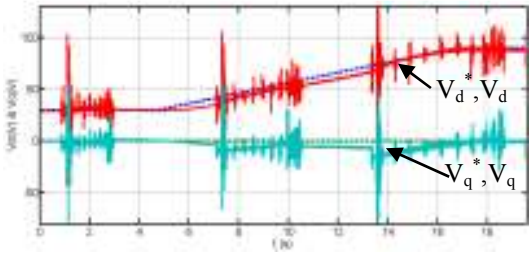


(b) Active and reactive power

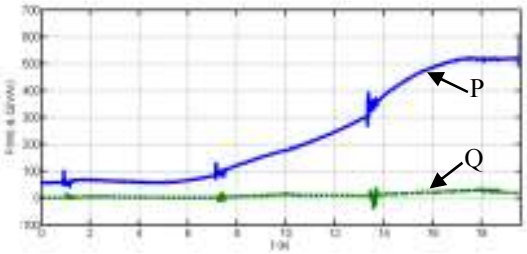


(c) Modulating signals

Figure 0.6: CSI experimental results in island mode using PR voltage control in an *abc* frame.

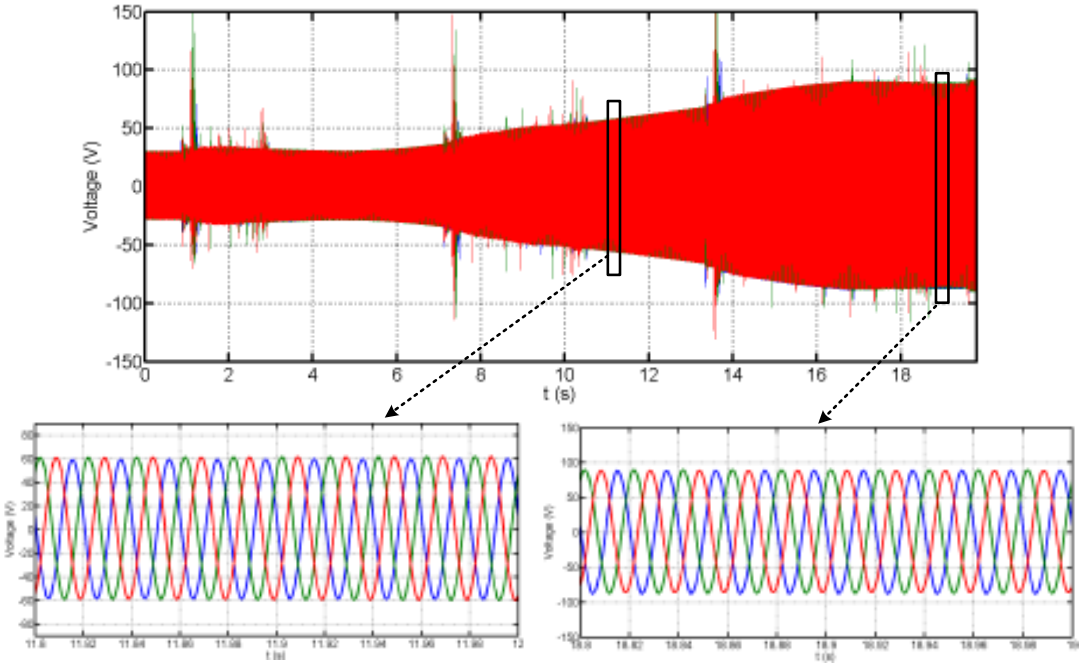


(a) *dq*-voltage with their references

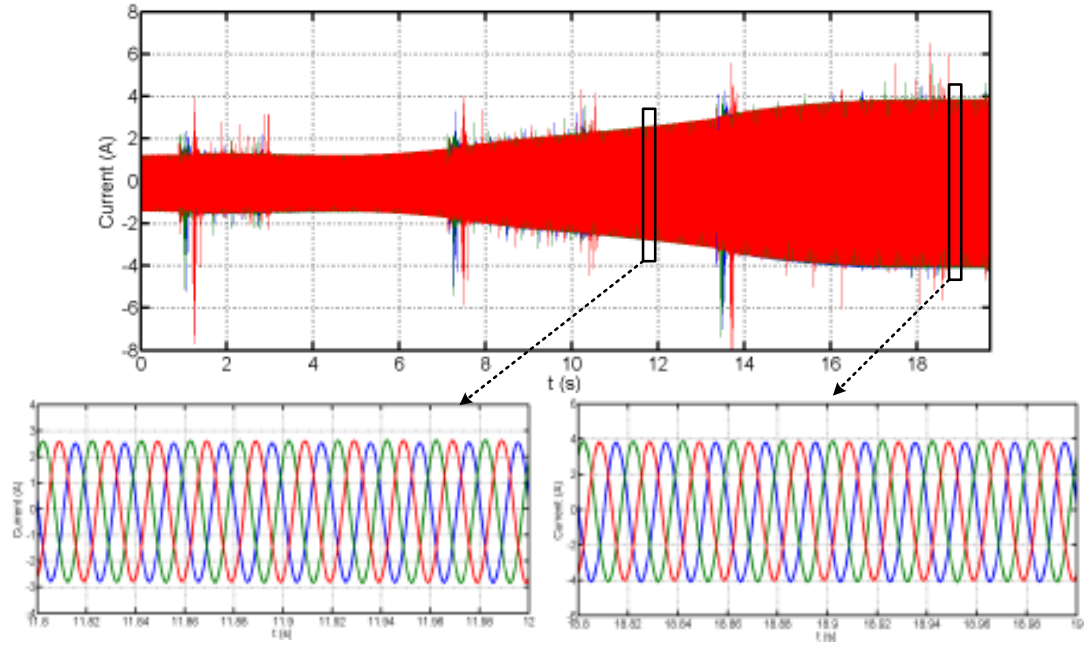


(b) Active and reactive powers

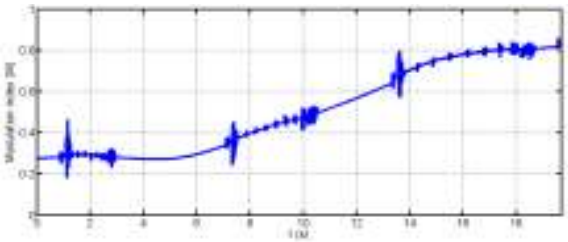
Figure 0.7:CSI experimental results in island mode using PI voltage control in the *dq*-frame (part a).



(a) Output voltage with exploded views



(b) Load current with exploded views



(c) Modulation index

Figure 0.8: CSI experimental results in island mode using PI voltage control in the *dq*-frame (part b).

7.3. Current control system for a grid-connected CSI

This section discusses the control systems used to assess the viability of the proposed DRSPWM technique for a grid connected CSI. Details are presented of the control variables manipulated in order to regulate active and reactive powers inverter exchanges with the ac grid.

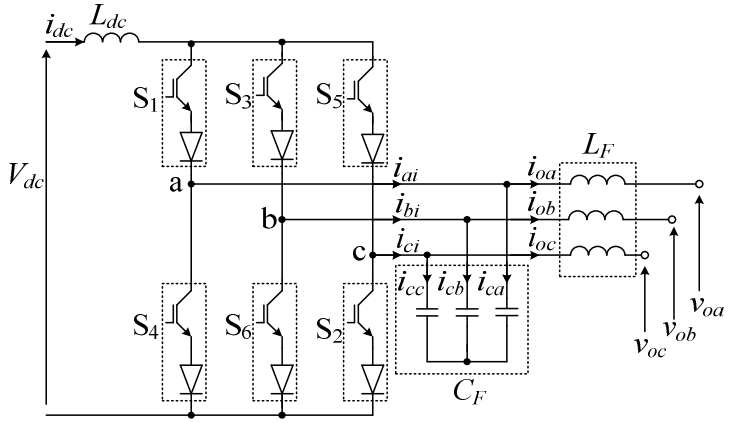


Figure 0.9: Schematic of grid-connected three-phase CSI.

From Figure 0.9, the dynamic equations describing the CSI in the *d-q* axes, where phase '*a*' of the grid voltage is aligned with the *d*-axis are:

$$\frac{di_{od}}{dt} = -\frac{R_F}{L_F} i_{od} + \frac{\left(v_{cd} - v_{od} + \omega L_F i_{oq}\right)}{L_F} \tag{7.52}$$

$$\frac{di_{oq}}{dt} = -\frac{R_F}{L_F} i_{oq} + \frac{\left(v_{cq} - v_{oq} - \omega L_F i_{od}\right)}{L_F} \tag{7.53}$$

$$\frac{dv_{cd}}{dt} = \frac{i_{id} - i_{od} + \omega C_F v_{cq}}{C_F} \tag{7.54}$$

$$\frac{dv_{cq}}{dt} = \frac{i_{iq} - i_{oq} - \omega C_F v_{cd}}{C_F} \tag{7.55}$$

Equations (7.52) and (7.53) describe the grid current dynamics in terms of the grid and filter capacitor voltages. Equations(7.54) and (7.55) express the capacitor voltage dynamics in terms of grid, filter capacitor and inverter currents where v_{od} and v_{oq}, and

v_{cd} and v_{cq} represent the *d-q* components of the grid and capacitor voltages; i_{od} and i_{oq}, and i_{id} and i_{iq} represent the *d-q* components of the grid and inverter currents; and R_F, L_F and C_F are the resistance, inductance and capacitance of the ac series and shunt filters.

7.3.1. Power control loop

The average power control method provides high quality sinusoidal output current and controls the average power flow. By assuming a fixed magnitude grid voltage, inverter active and reactive power exchange with the grid can be regulated directly by controlling the *d-q* components of the grid current. The reference currents the CSI needs to inject into the grid at voltage $v_o=v_{od}+jv_{oq}$ in order to exchange specific active and reactive powers can be expressed as:

$$\begin{bmatrix} i_{od}^* \\ i_{oq}^* \end{bmatrix} = \frac{2}{3} \frac{1}{v_{od}^2 + v_{oq}^2} \begin{bmatrix} v_{od} & v_{oq} \\ v_{oq} & -v_{od} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \tag{7.56}$$

7.3.2. Current control loop

Figure 0.10 presents the control system for grid-connected CSI which consists of a phase locked loop, outer current regulator, inner voltage regulator, and the proposed DRSPWM. The presented control structure in Figure 0.10uses several feedback loops with PI controllers in the synchronous frame, and feed-forward control to enhance the system's ability to reject disturbances. The proposed DRSPWM is used to generate the CSI switch gating signals. With this arrangement, system stability, dynamic response and response time are improved, with output harmonic elimination. To control the power flow, I_o is the outer control variable while for the inner loop, capacitor voltage, V_c enhances controller bandwidth.

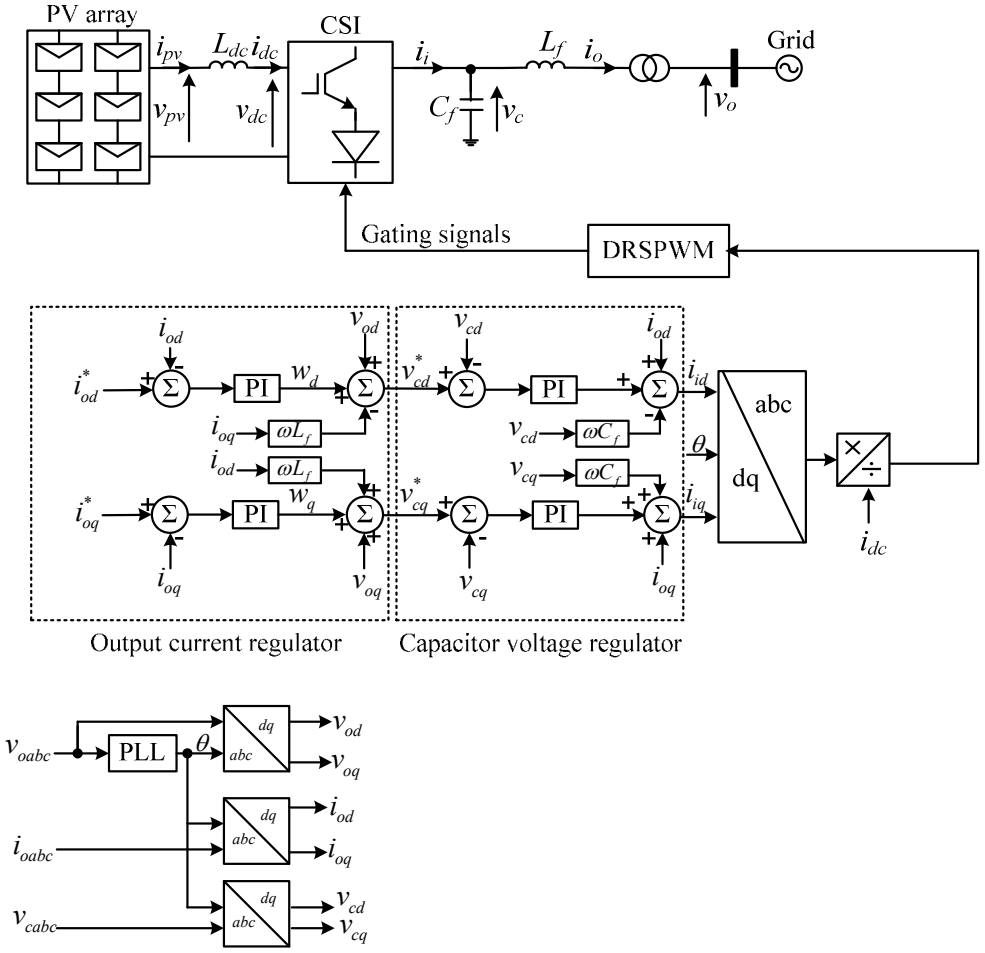


Figure 0.10: Block diagram of the control systems of a grid connected CSI.

The current regulator adjusts the magnitude and phase of the capacitor voltage relative to the grid voltage in order to fulfil the current commands in (7.56), designed based on equations (7.52) and (7.53). Thus the output current regulator autonomously provides a set-point to the inner loop that will be designed later based on (7.54) and (7.55). To facilitate current regulator design, let $w_d = v_{cd}^* - v_d + \omega L_F i_{oq}$ and $w_q = v_{cq}^* - v_q - \omega L_F i_{od}$, where the new variables w_d and w_q are obtained from the proportional-integral (PI) controller as follows:

$$w_d = k_{P1}\left(i_{od}^* - i_{od}\right) + k_{I1}\int\left(i_{od}^* - i_{od}\right)dt \tag{7.57}$$

$$w_q = k_{P1}\left(i_{oq}^* - i_{oq}\right) + k_{I1}\int\left(i_{oq}^* - i_{oq}\right)dt \tag{7.58}$$

where k_{P1} and k_{I1} are proportional and integral gains of the current regulators in the d and q channels.

Replacing the integral parts of (7.57) and (7.58) with z_d and z_q, and substituting the resultant expressions in (7.52) and (7.53), gives:

$$\frac{di_{od}}{dt} = -\frac{\left(R_F + k_{P1}\right)}{L_F} i_{od} + \frac{z_d}{L_F} + \frac{k_{P1}}{L_F} i_{od}^* \tag{7.59}$$

$$\frac{di_{oq}}{dt} = -\frac{\left(R_F + k_{P1}\right)}{L_F} i_{oq} + \frac{z_q}{L_F} + \frac{k_{P1}}{L_F} i_{oq}^* \tag{7.60}$$

$$\frac{dz_d}{dt} = k_{I1}\left(i_{od}^* - i_{od}\right) \tag{7.61}$$

$$\frac{dz_q}{dt} = k_{I1}\left(i_{oq}^* - i_{oq}\right) \tag{7.62}$$

Differential equations (7.59) to (7.62) can be re-arranged in state space form, $x'(t) = Ax(t) + Bu(t)$ as:

$$\frac{d}{dt}\begin{bmatrix} i_{od} \\ z_d \\ i_{oq} \\ z_q \end{bmatrix} = \begin{bmatrix} -\frac{(R_F + k_{P1})}{L_F} & \frac{1}{L_F} & 0 & 0 \\ -k_{I1} & 0 & 0 & 0 \\ 0 & 0 & -\frac{(R_F + k_{P1})}{L_F} & \frac{1}{L_F} \\ 0 & 0 & -k_{I1} & 0 \end{bmatrix} \begin{bmatrix} i_{od} \\ z_d \\ i_{oq} \\ z_q \end{bmatrix} + \begin{bmatrix} \frac{k_{P1}}{L_F} & 0 \\ k_{I1} & 0 \\ 0 & \frac{k_{P1}}{L_F} \\ 0 & k_{I1} \end{bmatrix} \begin{bmatrix} i_{od}^* \\ i_{oq}^* \end{bmatrix} \tag{7.63}$$

This arrangement shows the states related to the *d*-channel can be solved or controlled independent of the *q*-channel, hence decoupled control of active and reactive power is achieved.

Since w_d and w_q represent the outputs of the current regulator for the *d* and *q* channels, the *d*-*q* components of the reference capacitor voltage for the inner control loops can be estimated, taking into account feed-forward terms as follows:

$$v_{cd}^{*} = w_d + v_{od} - \omega L_F i_{oq} \tag{7.64}$$

$$v_{cq}^{*} = w_q + v_{oq} + \omega L_F i_{od} \tag{7.65}$$

As stated, the inner current loop is designed based on equations (7.64) and (7.65). The inner voltage controller adjusts the magnitude and phase of the fundamental component of the inverter currents (i_{ai}, i_{bi} and i_{ci}) and forces the capacitor voltages to follow the references provided by the current regulator. Therefore, similar procedures as those illustrated previously are required to facilitate controller design.

In (7.64) and (7.65), let $\lambda_d = i_{id} + \omega C v_{cq} - i_{od}$ and $\lambda_q = i_{iq} - \omega C v_{cd} - i_{oq}$, where the variables λ_d and λ_q are obtained from the proportional-integral (PI) controller as follows:

$$\lambda_d = k_{p2}\left(v_{cd}^{*} - v_{cd}\right) + k_{I2}\int (v_{cd}^{*} - v_{cd})dt \tag{7.66}$$

$$\lambda_q = k_{p2}\left(v_{cq}^{*} - v_{cq}\right) + k_{I2}\int (v_{cq}^{*} - v_{cq})dt \tag{7.67}$$

where k_{P2} and k_{I2} are the proportional and integral gains of the inner capacitor voltage regulator.

After replacing the integral parts of (7.66)and(7.67) with ψ_d and ψ_q, the following state space equations, of the form $x'(t) = Ax(t) + Bu(t)$, are obtained:

$$\frac{d}{dt}\begin{bmatrix} v_{cd} \\ \psi_d \\ v_{cq} \\ \psi_q \end{bmatrix} = \begin{bmatrix} -\frac{k_{P2}}{C_F} & \frac{1}{C_F} & 0 & 0 \\ -k_{I2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{k_{P2}}{C_F} & \frac{1}{C_F} \\ 0 & 0 & -k_{I2} & 0 \end{bmatrix} \begin{bmatrix} v_{cd} \\ \psi_d \\ v_{cq} \\ \psi_q \end{bmatrix} + \begin{bmatrix} \frac{k_{P2}}{C_F} & 0 \\ k_{I2} & 0 \\ 0 & \frac{k_{P2}}{C_F} \\ 0 & k_{I2} \end{bmatrix} \begin{bmatrix} v_{cd}^{*} \\ v_{cq}^{*} \end{bmatrix} \tag{7.68}$$

The reference inverter currents are obtained from the inner loop as:

$$i_{id}^{*} = \psi_d + i_{od} - \omega C_F v_{cq} \tag{7.69}$$

$$i_{id}^{*} = \psi_d + i_{od} + \omega C_F v_{cq} \tag{7.70}$$

The transfer functions that govern the grid current and capacitor voltage controllers can be obtained from (7.63) and (7.68). From these transfer functions, the theoretical gains for both controllers are obtained by assigning settling times and damping factors. The final controller gains used are obtained by fine-tuning based on Eigen-value analysis of the overall state matrix in (7.71).

The reference currents in (7.69) and (7.70) must be normalized by dc link current I_{dc} before passing them to the modulator. With the aid of (7.64) and (7.65), the state space equations in (7.63) can be combined with (7.68) to obtain the state equations for the overall system that account for possible interaction between the current and capacitor voltage loops.

$$\frac{d}{dt}\begin{bmatrix} i_{od} \\ z_d \\ v_{cd} \\ \psi_d \\ i_{oq} \\ z_q \\ v_{cq} \\ \psi_q \end{bmatrix} = \begin{bmatrix} -\frac{(R_f + k_{p1})}{L_f} & \frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & 0 \\ -k_{i1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{k_{p1}k_{p2}}{C_f} & \frac{k_{p2}}{C_f} & -\frac{k_{p2}}{C_f} & \frac{1}{C_f} & -\frac{k_{p2}\omega L_f}{C_f} & 0 & 0 & 0 \\ -k_{p1}k_{i2} & k_{i2} & -k_{i2} & 0 & -k_{i2}\omega L_f & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{(R_f + k_{p1})}{L_f} & \frac{1}{L_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & -k_{i1} & 0 & 0 & 0 \\ \frac{k_{p2}\omega L_f}{C_f} & 0 & 0 & 0 & -\frac{k_{p1}k_{p2}}{C_f} & \frac{k_{p2}}{C_f} & -\frac{k_{p2}}{C_f} & \frac{1}{C_f} \\ k_{i2}\omega L_f & 0 & 0 & 0 & -k_{p1}k_{i2} & k_{i2} & -k_{i2} & 0 \end{bmatrix} \begin{bmatrix} i_{od} \\ z_d \\ v_{cd} \\ \psi_d \\ i_{oq} \\ z_q \\ v_{cq} \\ \psi_q \end{bmatrix}$$
$$+ \begin{bmatrix} \frac{k_{p1}}{L_f} & 0 & 0 & 0 \\ k_{i1} & 0 & 0 & 0 \\ \frac{k_{p1}k_{p2}}{C_f} & \frac{k_{p2}}{C_f} & 0 & 0 \\ k_{p1}k_{i2} & k_{i2} & 0 & 0 \\ 0 & 0 & \frac{k_{p1}}{L_f} & 0 \\ 0 & 0 & k_{i1} & 0 \\ 0 & 0 & \frac{k_{p1}k_{p2}}{C_f} & \frac{k_{p2}}{C_f} \\ 0 & 0 & k_{p1}k_{i2} & k_{i2} \end{bmatrix} \begin{bmatrix} i_{od}^* \\ v_{od} \\ i_{oq}^* \\ v_{oq} \end{bmatrix} \tag{7.71}$$

The relationship that determines the ability of a CSI to exchange active and reactive power with the grid at voltage level V_{oabc} can be expressed as:

$$\left[\frac{P}{v_{od}} - \omega C_F v_{cq}\right]^2 + \left[\frac{Q}{v_{od}} - \omega C_F v_{cd}\right]^2 = i_{id}^2 + i_{iq}^2 \tag{7.72}$$

Given $i_{id}^2 + i_{iq}^2 = m^2 i_{dc}^2$, expression (7.72) can be rewritten as:

$$\left[\frac{P}{v_{od}} - \omega C_F v_{cq}\right]^2 + \left[\frac{Q}{v_{od}} - \omega C_F v_{cd}\right]^2 \leq m_{\max}^2 i_{dc}^2 \tag{7.73}$$

contribution to the fundamental current which may affect the dc current utilization. Inequality (7.73) shows that the ability of a CSI to exchange active and reactive powers with the grid is limited by the filter capacitance C_F, particularly when the inverter is sourcing lagging *VAr* (Q is negative). From (7.73) as $V_{cd} >> V_{cq}$, lagging reactive power tends to increase the modulation, and hence reduces the available modulation index margin for active power control. Operation with leading reactive power reduces the modulation index, and hence increases the margin for power control, for a fixed dc link current I_{dc}. Therefore, the relationship between *VAr* generation and modulation in a CSI is the opposite to that for a VSI. The equivalent relationship to (7.73) for a VSI is:

$$\left[\frac{\omega LP}{V_{do}}\right]^2 + \left[\frac{\omega LQ}{V_{do}} + V_{do}\right]^2 \leq \tfrac{1}{4} m_{\max}^2 V_{dc}^2 \tag{7.74}$$

where L is the total inductance of the phase interfacing reactors and transformer, neglecting resistance, V_{dc} is the VSI dc link voltage and P and Q are active and reactive power respectively.

This discussion has shown the CSI reactive power capabilities, and its possibilities for grid interfacing of renewable power where the inverter needs to meet strict requirements regarding sourcing of leading *VAr* and during low-voltage ride-through (LV-RT) conditions when attempting to support the grid voltage. Inequality (7.73) is useful for selecting the minimum dc link current required by the CSI in order to be able to exchange rated power at rated ac voltage for a given filter capacitance. The filter capacitor must be sized taking into account several factors: it must be sufficient for harmonic attenuation; a cut-off frequency of less than 200Hz to avoid control system conflict and LC filter resonance excitation due to the presence of low-order harmonics such as the 5^{th} and 7^{th}; and it must make a minimum

7.4. Simulation results

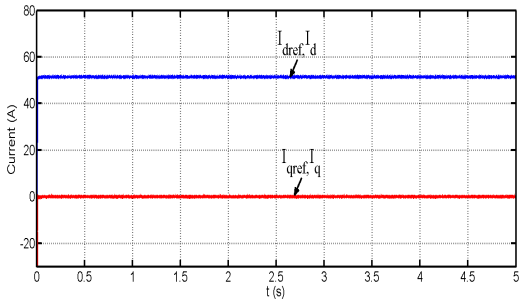
To further validate the proposed DRSPWM with a multi-loop control system, simulation results for the exchange of medium active and reactive powers are presented in this section. Table 0.2 lists the parameters used for the grid connected CSI.

Table 0.2: Parameters used in simulation for grid connected current source inverter

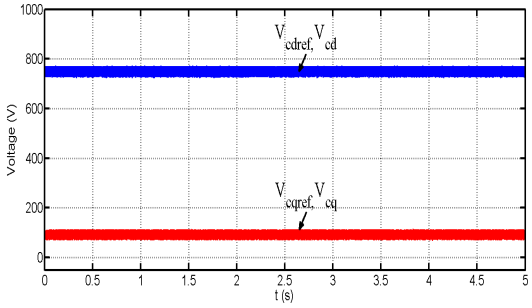
Parameters		Values	SI units
Maximum dc link current	I_{dc}	60	A
Switching frequency	f_s	2.1	kHz
Two-level converter rating	S	150	kVA
Active power capability	P	120	kW
Reactive power capability	Q	90	kVAr
Line-to-line ac voltage	V_{ac}	415	V
Filter capacitor	C_F	100	μF
Filter inductor	L_F	3	mH
Transformer turn ratio	N	1:1	
Current controller proportional gain	k_{P1}	25	Ω
Current controller integral gain	k_{I1}	3200	Ωs^{-1}
Capacitor voltage controller proportional gain	k_{P2}	1	Ω^{-1}
Capacitor voltage integral gain	k_{I2}	80	$\Omega^{-1}s^{-1}$

7.4.1. Unity power factor application

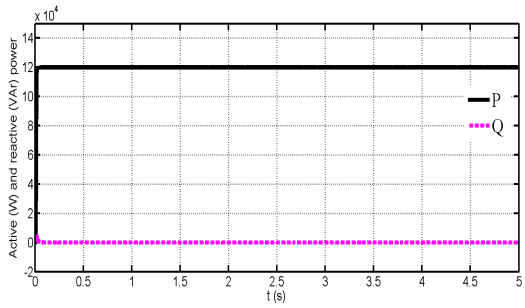
Reference active current, I_{dref} is set to 50A while reactive current reference, I_{qref} is 0A to achieve unity power factor. Figure 0.11(a) shows that I_d and I_q are able to track their references when the CSI is operated at rated power. Figure 0.11(b) show the performance of capacitor voltage used in the inner control loop regulator. The inverter operates at full medium active power as in Figure 0.11(c) with the exchange at $415V_{ac}$ grid voltage, shown in Figure 0.11(d). Output current is shown in Figure 0.11(e) while Figure 0.11(f) shows that the normalized grid voltage is in phase with the current in this unity power factor application.



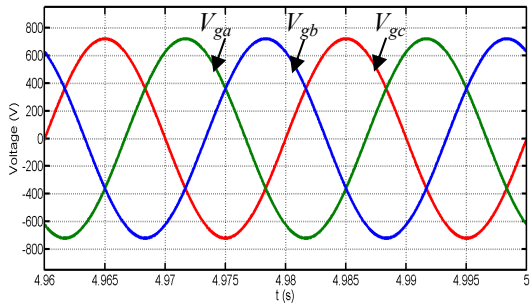
(a) *dq* output current with their references



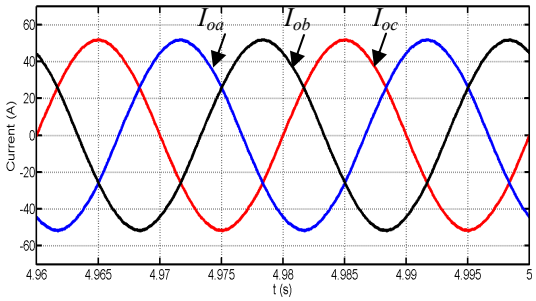
(b) *dq* capacitor voltage with their references



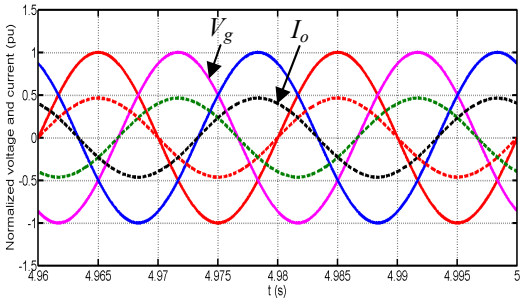
(c) Active and reactive power exchange with the grid



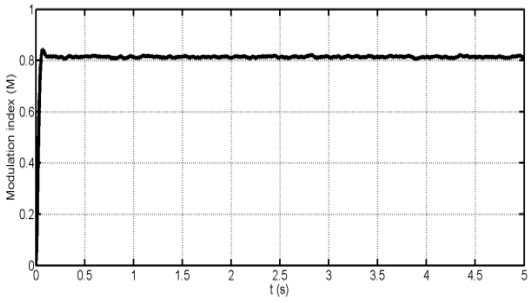
(d) Grid voltage



(e) Output current



(f) Normalized voltage and current in phase at unity power factor

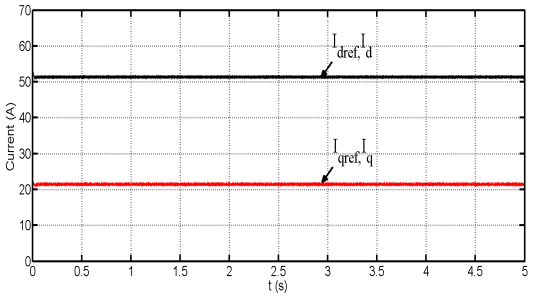


(g) Modulation index

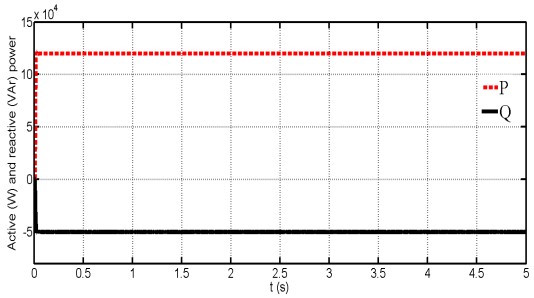
Figure 0.11: CSI simulation results operating with the proposed DRSPWM with unity power factor.

7.4.2. Lagging power factor

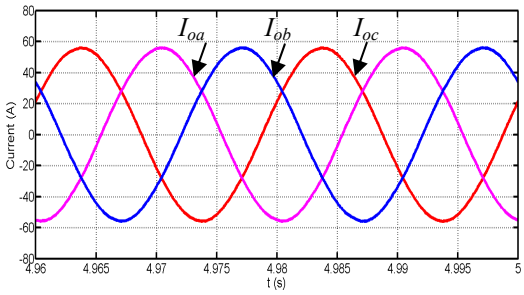
In a lagging power factor application, the active current I_d is remains at 50A while reactive current is changed to 20A as shown in Figure 0.12(a). The CSI operates at its active rated capability, 120kW, while the reactive power reaches approximately half its rating, -50kVAr, as illustrate in Figure 0.12(b). The output current and grid voltage for a lagging power factor are seen in Figure 0.12(c) and (d) respectively. Figure 0.12(e) shows the current waveform lags the voltage.



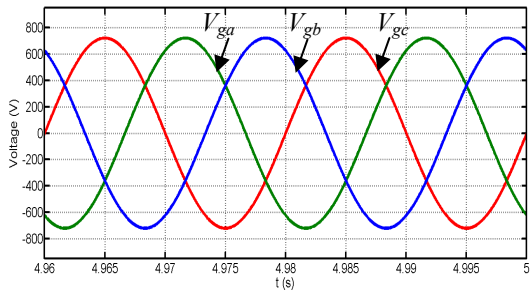
(a) *dq* output currents with their respective references



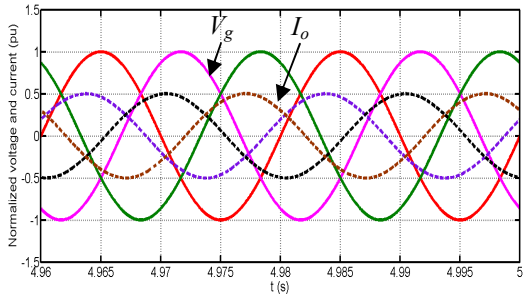
(b) Active and reactive power exchange with the grid



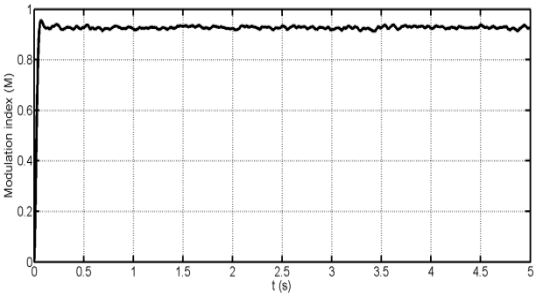
(c) Output current



(d) Grid voltage



(e) Current and voltage waveforms

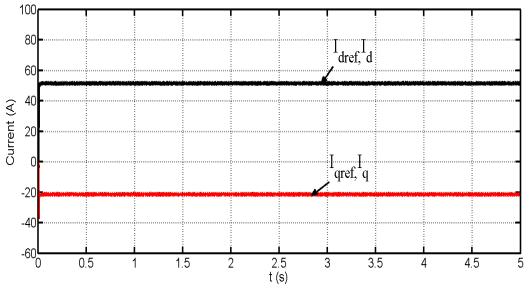


(f) Modulation index

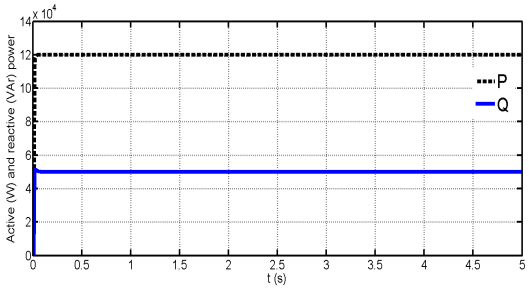
Figure 0.12: CSI simulation waveforms operating with the proposed DRSPWM with a lagging power factor.

7.4.3. Leading power factor

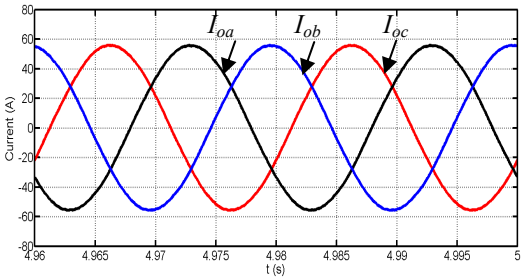
The reference reactive current, I_{qref} is set to -20A while I_{dref} is maintained at 50A to achieve a leading power factor. Figure 0.13(a) show the output current, I_d and I_q are able to track their references, producing medium active and reactive powers of 120kW and 50kVAr respectively, see Figure 0.13(b). The output current and grid voltage are shown in Figure 0.13(c) and (d) respectively. Figure 0.13(e) shows the current leads the voltage by 90°. The modulation index for lagging power factor is shown in Figure 0.13(f).



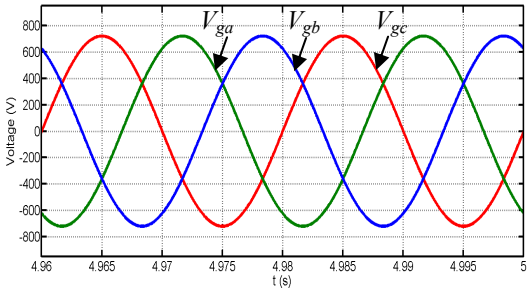
(a) *dq* output current and their references



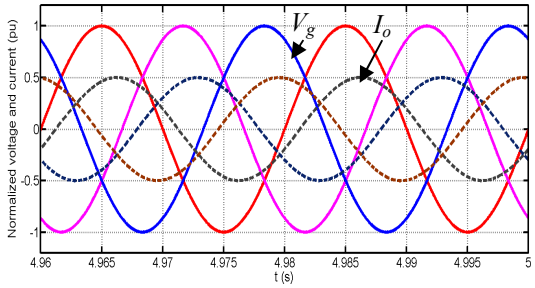
(b) Active and reactive power exchange with the grid voltage



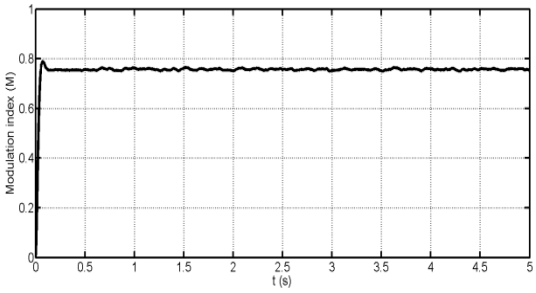
(c) Output current



(d) Grid voltage



(e) Current leads voltage by 90°

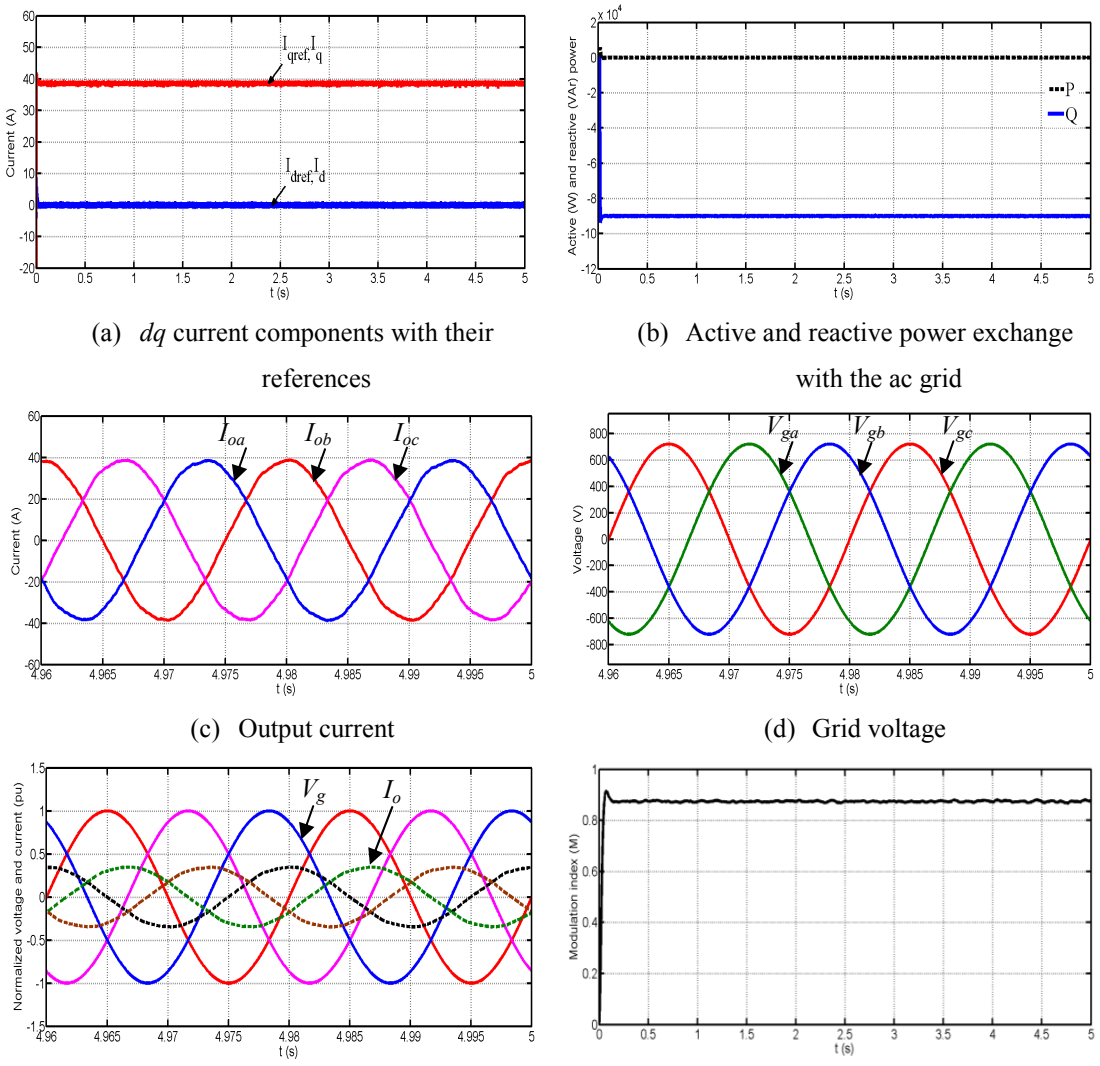


(f) Modulation index

Figure 0.13: CSI simulation results operating with the proposed DRSPWM with a leading power factor.

7.4.4. Zero power factor

In a zero power factor application, the inverter supplies reactive power and the active power is set to zero. The reactive current component, I_q is 40A and I_d is zero as shown in Figure 0.14(a), to produce rated reactive power of 90kVAr as shown in Figure 0.14(b). The output current and grid voltage are shown in Figure 0.14(c) and (d) respectively. The current and voltage phase conform with the conditions for zero power factor, as shown in Figure 0.14(e). The modulation index is maintained approximately 0.87 for this application, as shown in Figure 0.14(f).



(a) *dq* current components with their references

(b) Active and reactive power exchange with the ac grid

(c) Output current

(d) Grid voltage

(e) Normalized current and voltage waveforms

(f) Modulation index

Figure 0.14:CSI simulation results operating with the proposed DRSPWM at zero power factor.

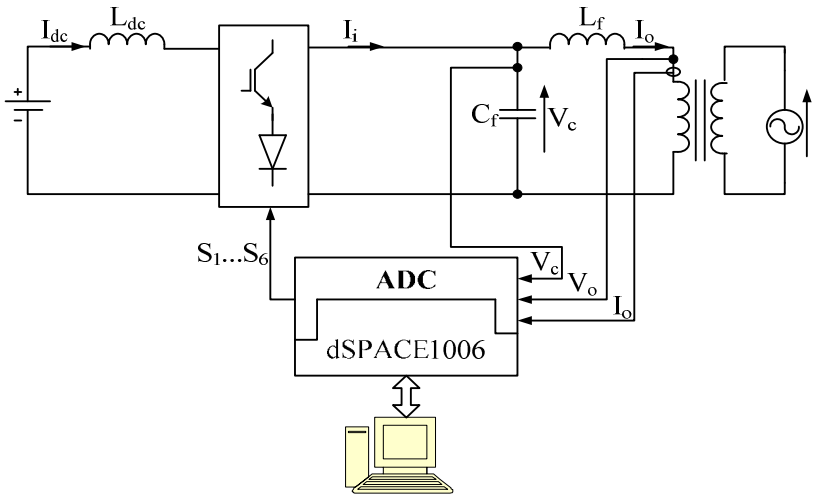
7.5. Experimental results of the proposed DRSPWM in a grid connected CSI

To investigate the viability of the proposed DRSPWM for a grid connected CSI, this section presents experimental results for a three-phase CSI connected to the grid, controlled using DRSPWM in conjunction with the control systems depicted in Figure 0.10. The experimental system parameters used are listed in Table 0.3. The hardware configuration is shown in Figure 0.15. The ac power filter parameters, C_F and L_F are selected so as to place the filter cut-off frequency at 200Hz, for reasons previously stated. With C_F<<200μF, the filter corner frequency is close to the control system bandwidth, resulting in system instability due to conflict between the filter and the control system. Also there is potential for low-order harmonics, such asthe 5th and 7th, to excite LC filter resonance.

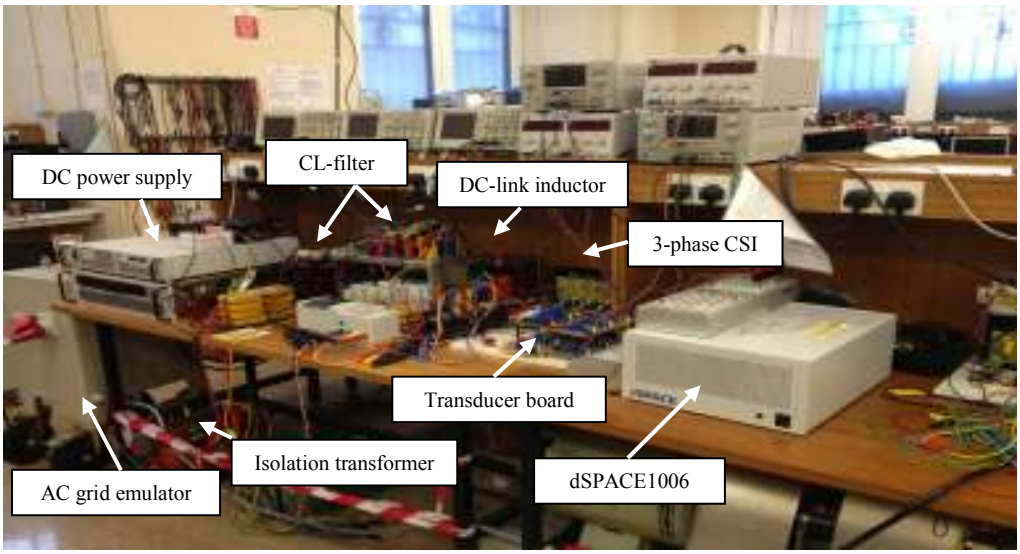
Table 0.3: Parameters used in the experiments

Parameters		Values	SI units
Maximum dc link current	I_{dc}	8	A
DC link inductor	L_{dc}	10	mH
Line-to-line ac side voltage	$V_{ac(rms)}$	√3×30	V
Switching frequency	f_s	4	kHz
Filter capacitor	C_F	200	μF
Filter inductor	L_F	3	mH
Transformer turn ratio	N	1:1	
Current controller proportional gain	k_{P1}	0.065	Ω
Current controller integral gain	k_{I1}	0.22	Ωs^{-1}
Capacitor voltage controller proportional gain	k_{P2}	0.015	Ω^{-1}
Capacitor voltage integral gain	k_{I2}	0.02	$\Omega^{-1}s^{-1}$

The results presented for the grid connected CSI are obtained when the inverter is fed from a dc source that mimics an ideal current source by varying the input dc voltage to maintain a constant dc link current of 8A. The viability of the proposed DRSPWM is investigated when the grid connected CSI is operated under various conditions.



(a)



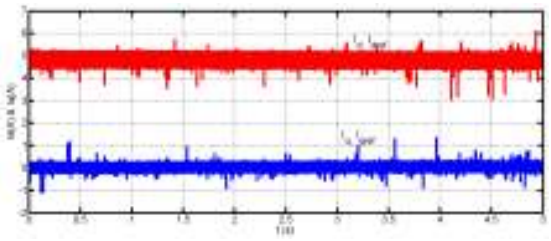
(b)

Figure 0.15: (a) Hardware diagram and (b) test-rig photograph.

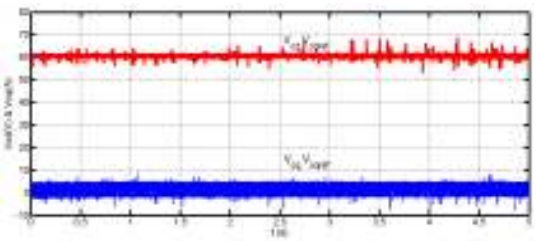
7.5.1. Unity power factor application

Figure 0.16 shows the results when the CSI injects active power into the grid at near unity power factor, with $i_{od}^{*} = 5A$ and $i_{oq}^{*} = 0$. Figure 0.16(a) shows the current controller successfully forces the active and reactive power current components i_{od} and i_{oq} to follow their references. Figure 0.16(b) also shows that the *d-q* components of the filter capacitor voltages (v_{cd} and v_{cq}) follow their references set by the current controller, and confirms the assumption made regarding $v_{cq} << v_{cd}$.

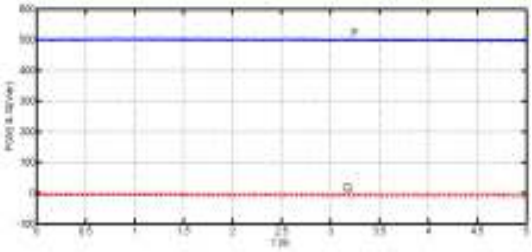
Figure 0.16(c) displays the actual active and reactive powers exchanged with the grid, and shows zero reactive power as expected. Figure 0.16(d) shows CSI voltage waveforms presented to the interfacing transformer that is used to provide galvanic isolation and voltage matching. The current waveform injected into the grid, monitored at the primary side of the transformer, is shown in Figure 0.16(e). Figure 0.16(f) confirms the phase voltage and current are in phase. Figure 0.16(g) shows the modulation index when the CSI is operated under the conditions stated. There is a small modulation index margin left that could be utilized for active or reactive power generation.



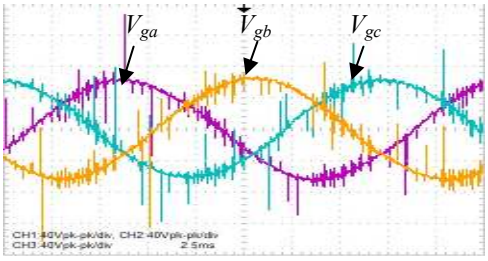
(a) *d-q* current components and their references



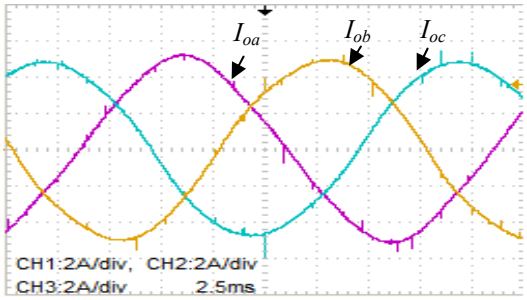
(b) *d-q* components of the capacitor voltage and their references



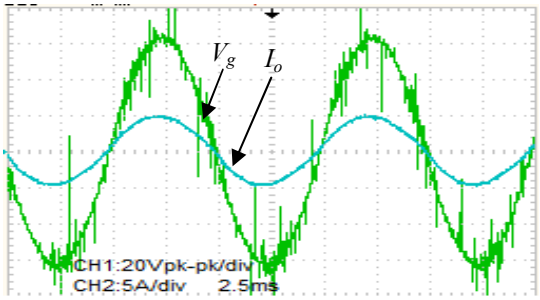
(c) Active and reactive power CSI injects into grid



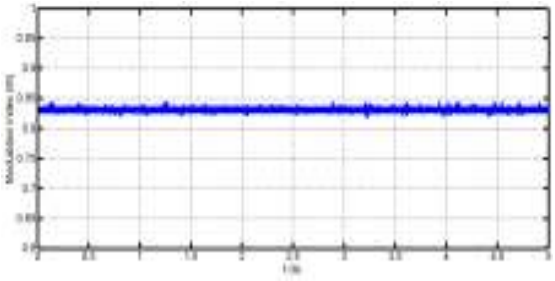
(d) Phase voltage CSI presents to interfacing transformer (40V/div, 2.5ms)



(e) Output current CSI injects to the grid (2A/div, 2.5ms)



(f) Phase voltage and current waveforms

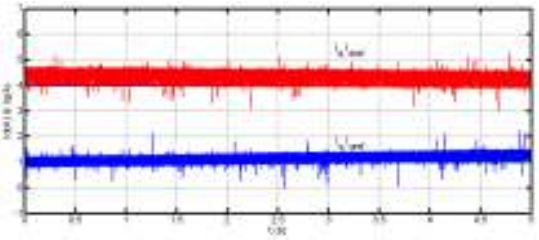


(g) Modulation Index

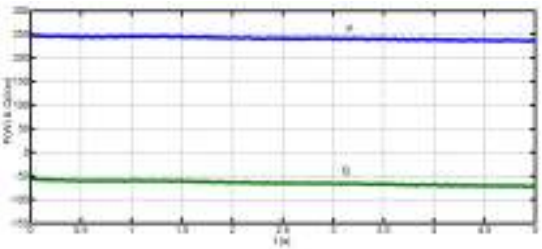
Figure 0.16:Waveforms of CSI operating with the proposed DRSPWM with near unity power factor (I_{dc}=8A, i_{od}= 5A, i_{oq}=0, V_{ac}=30V per phase).

7.5.2. Lagging power factor

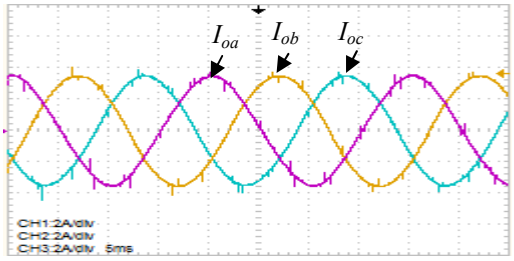
The experimental results in Figure 0.17 demonstrate successful CSI operation with the proposed DRSPWM when injecting active power and lagging reactive power at i_{od}=4A and i_{oq}=1A. Figure 0.17(a) shows the actual current tracks the reference current, and Figure 0.17(b) shows the active and reactive powers exchanged with the grid. Figure 0.17(c) and (d) show the voltage and current waveforms the CSI presents to the grid. Figure 0.17(e) shows phase voltage and current waveforms, again confirming that the phase current lags the voltage.



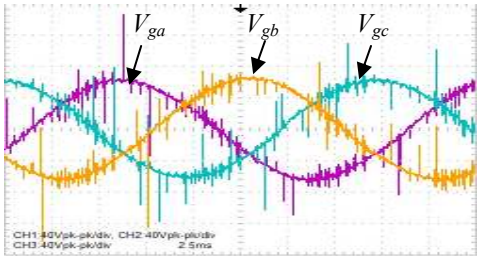
(a) *d-q* current components and their references



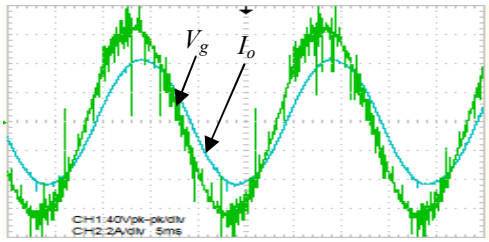
(b) Active and reactive powers CSI deliver to grid



(c) Output current CSI injects into grid (2A/div, 5ms)



(d) Phase voltage waveforms CSI present to interfacing transformer (40V/div, 2.5ms)

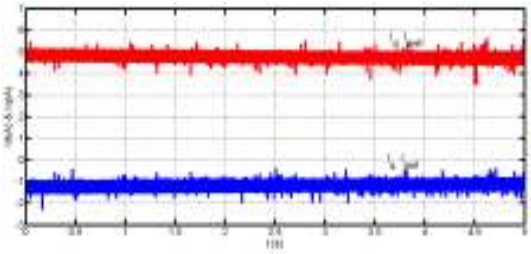


(e) Phase voltage and current waveforms

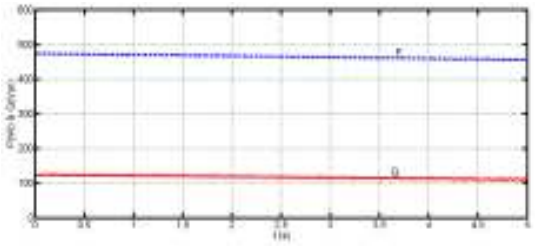
Figure 0.17: Waveforms demonstrating CSI operation with the proposed DRSPWM when delivering active power at lagging VAr (I_{dc}=8A, i_{od}=4A and i_{oq}= 1A).

7.5.2. Leading power factor

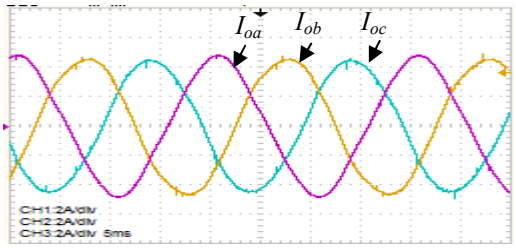
Figure 0.18 presents results when the CSI delivers active power with leading reactive power. Figure 0.18(a) shows the active and reactive power current components injected into the grid, confirming that the *d-q* currents follow their references, with i_{oq} negative for leading reactive power. Figure 0.18(b) shows the active and reactive powers injected into the grid at $i_{od}=5A$ and $i_{oq}=-1A$. Figure 0.18(c) and (d) show current and voltage waveforms as the CSI delivers active power at leading reactive power. Figure 0.18(e) shows that the modulation index reduces when active power is delivered into grid with leading reactive power and the same magnitude of i_{od}=5A. This is shown in equation (7.25) and articulated in the previous sections. Figure 0.18(f) further confirms leading reactive power generation, as the phase current leads the voltage.



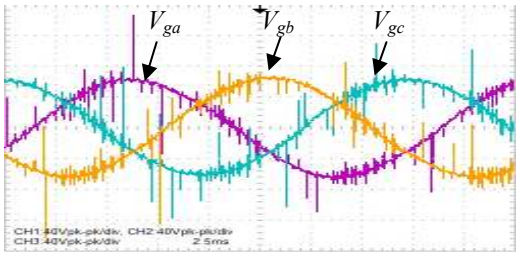
(a) *d-q* components of the inverter output current and their references



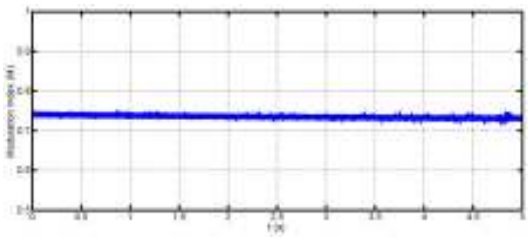
(b) Active and reactive power CSI exchanges with the grid



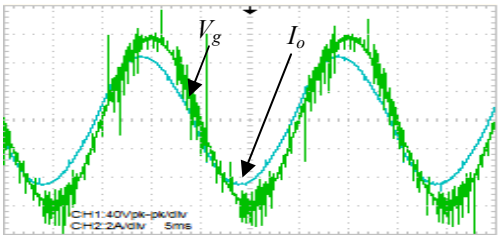
(c) Output current CSI injects into the grid (2A/div, 5ms)



(d) Phase voltage CSI presents to the interfacing transformer (40V/div, 2.5ms)



(e) Modulation index

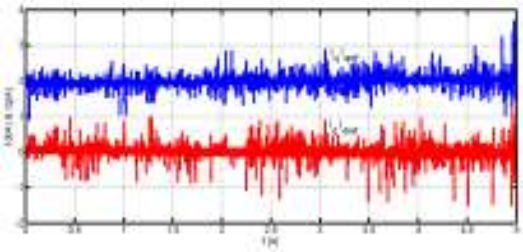


(f) Phase voltage and current waveforms

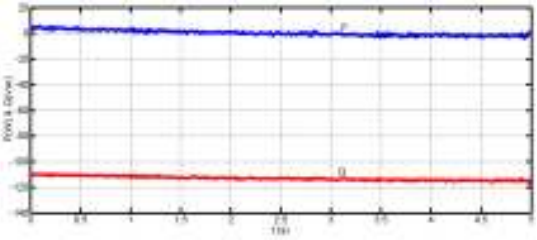
Figure 0.18: Waveforms demonstrating CSI operation with the proposed DRSPWM when delivering active power into grid with leading reactive power.

7.5.4. Zero power factor

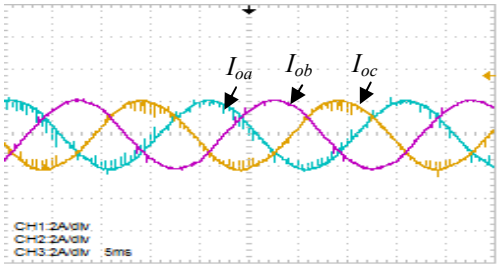
Figure 0.19 present results when the DRSPWM controlled CSI operates as a typical static synchronous compensator (STATCOM) with i_{od}=0 and i_{oq}=2A. Figure 0.19(a) and (b) demonstrate CSI operation at zero power with zero active power, as seen in the *d-q* current components and power plots. Figure 0.19(c) and (d) show that the current and voltage waveforms presented to grid at the transformer input remain sinusoidal. Figure 0.19(e) shows that the phase current lags the voltage by 90°. The proposed DRSPWM CSI is able to operate successfully over the entire operating range, including zero power factor. Based on the results presented in Figures 7.16, 7.17, 7.18 and 7.19, it can be concluded that the proposed DRSPWM controlled CSI is viable for a wide range of applications that use closed-loop control.



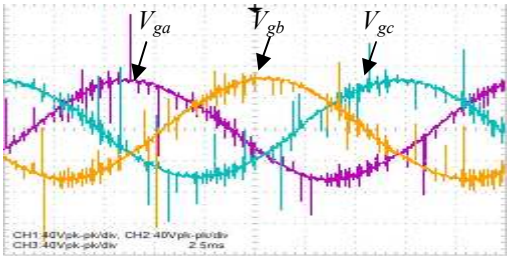
(a) *d-q* current components and their references



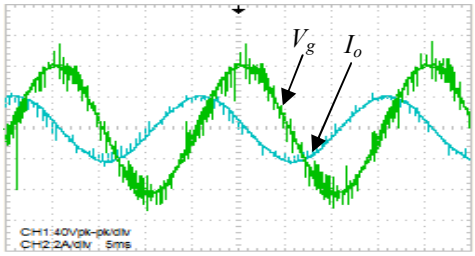
(b) Active and reactive power CSI exchanges with the grid



(c) Output current CSI injects into the grid (2A/div, 5ms)



(d) Phase voltage CSI presents to the interfacing transformer (40V/div, 2.5ms)



(e) Phase voltage and current waveforms

Figure 0.19: Waveforms demonstrating CSI operation with the proposed DRSPWM and zero power factor (typical reactive power applications).

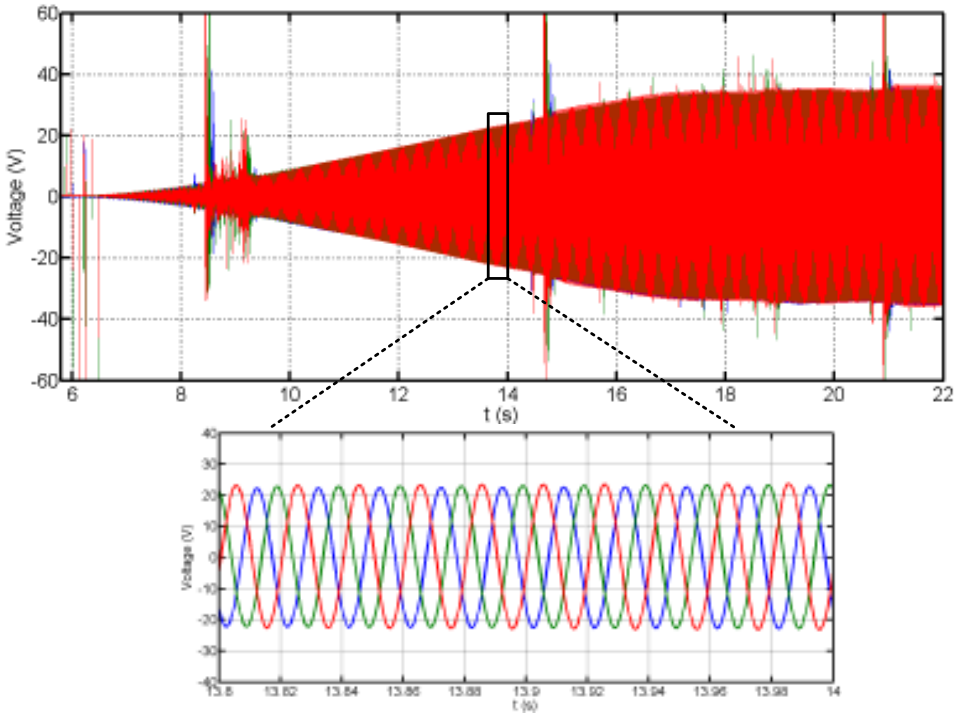
7.5.5. Black-start capability with the proposed DRSPWM

The UK National Grid, Grid Code Operating Code OC5.5.4 – Black Start Testing section defines a black start as the procedure to recover from a total or partial shutdown of the transmission system which has caused extensive loss of supplies. This entails isolated power stations being started individually and gradually being reconnected in order to form an interconnected system again [7.25]. During this situation, operation of a grid connected CSI is similar to an islanding mode where the CSI is voltage mode controlled. The inverter must be able to set the ac voltage for the grid and local load, with excellent harmonic rejection, as well as promoting a low-loss system.

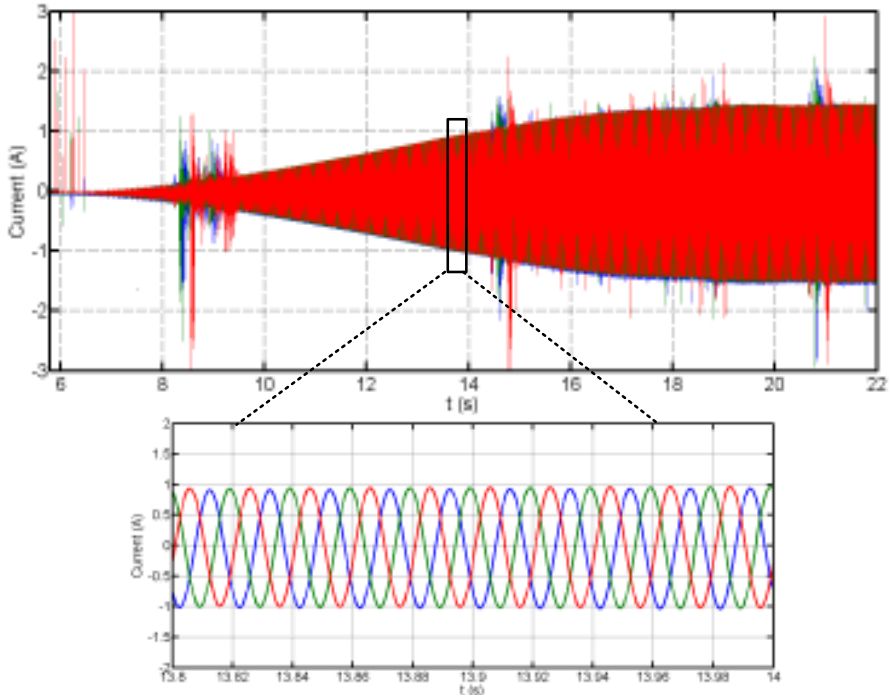
In [7.26], twelve-step PWM is introduced where the switching devices of the CSI operates at half the carrier frequency. This is an indication of low switching losses and offers the same feature as the new direct regular sampled PWM technique. However, the grid voltages are used as reference modulating signals that are compared with two saw-tooth unipolar carriers to generate the gating signals for the CSI switches. This compromises the basic features that make the PWM CSI competitive with respect to the VSI, such as black-start capability, and operation independent of the network short-circuit ratio. In other words, such a scheme cannot be used to power a dead ac network that has no live ac voltage.

Taking this aspect into consideration, the proposed new direct regular sampled PWM modulation technique does not use any carrier signals or reference voltages. Instead it divides the fundamental period into six sectors (60^{o}), and uses reference currents to determine the dwell times of the converter switches, assuming that within each switching cycle (T_s) the dwell time of the active state is proportional to the reference current magnitude. A CSI with the proposed modulation technique is able to operate without any abnormality during a black-start situation.

The experimental results in Figure 0.20 confirmed this feature by displaying the voltage and current waveforms, starting from 0A to a specified current level.



(a) Voltage (also magnified *13.8s<t<14s*) during black-start



(b) Current (also magnified *13.8s<t<14s*)during black-start

Figure 0.20: Experimental results confirming the capability of the proposed DRSPWM during black-start.

7.6. Typical application of a CSI for grid connection of PV arrays

The CSI is utilised to track the PV maximum power point and to interface the PV system to the grid. In order to achieve these requirements, three control loops are employed, namely dc-link voltage control, ac current control, and capacitor voltage control, as in Figure 0.21. The inverter dc link voltage is adjusted as the weather changes to ensure maximum power extraction all the times. This has been simulated with the aid of the lookup table that contains a pre-defined PV *I-V* characteristic. Weather condition variations are simulated by variable current from the PV arrays, which is assumed as the input signal to the lookup table.

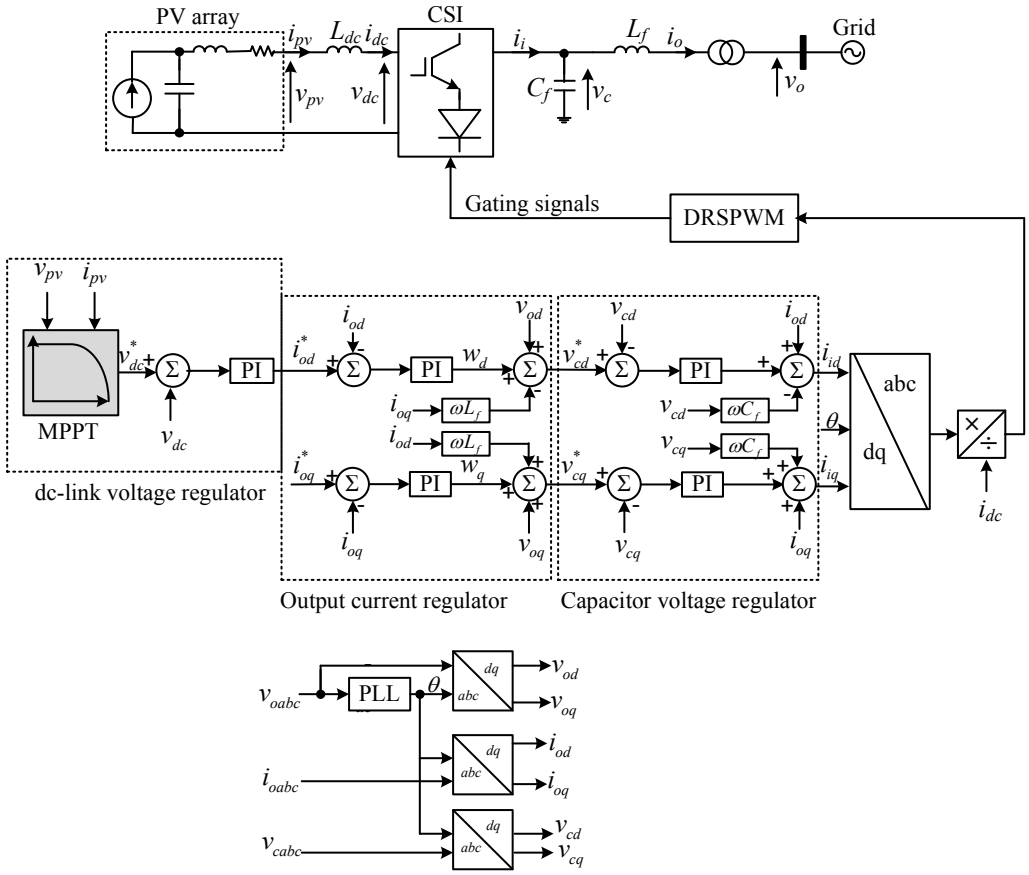


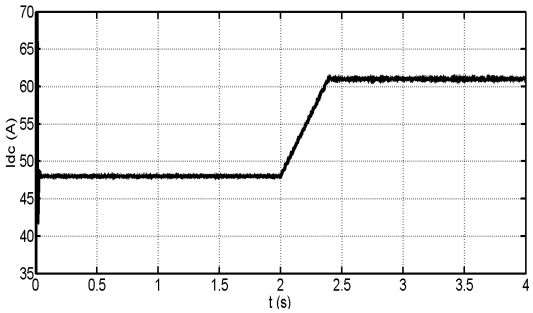
Figure 0.21: Test system of a grid-connected CSI for photovoltaic application.

Matlab/Simulink simulations demonstrate the performance of a single-stage grid-connected CSI when tracking the maximum power point and delivering active and reactive powers into the ac grid. For performance demonstration of the grid-connected

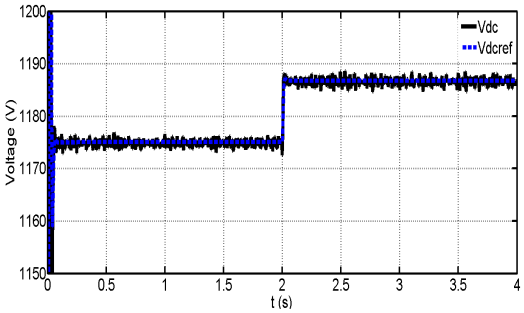
CSI under varying weather conditions, the test system shown in Figure 0.21is simulated with the following parameters: the PV array is modelled as a current source that varies its current injection (i_{pv}) with weather, and in this case i_{pv} is varied from 50A to 60A; dc-link inductor=40mH; converter rated apparent power=100kVA; rated ac grid line voltage=380V; switching frequency=2.1kHz; and an LC-filter with 3mH and 80μF inductance and capacitance respectively.

The simulation results of the CSI under varying weather conditions are shown in Figure 0.22. As PV array output current varies from 50A to 60A, dc-link current varies accordingly as shown in Figure 0.22(a). A new dc-link reference voltage is tracked by the MPPT, and using a typical proportional-integral dc-link voltage regulator, the measured dc-link voltage able to track the reference satisfactory. This is illustrated in Figure 0.22(b). The injected output currents are in phase with the voltage at the point of common coupling as required by the grid code and shown in Figure 0.22(c)and the active and reactive power exchanged with the grid is shown in Figure 0.22(d).

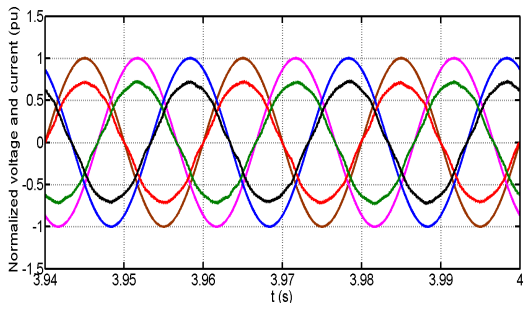
From these results, it can be inferred that PV grid integration using the CSI is satisfactory and can be relatively competitive with VSI PV grid integration in terms of simpler ac-filter design, and direct control of injected current (as compared to indirect output current control in a VSI).



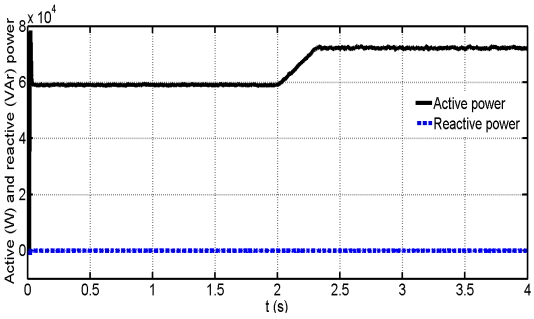
(a) dc-link current



(b) dc-link voltage with respect to reference from MPPT



(c) Normalized grid voltage and output current at unity power factor



(d) Grid active and reactive powers

Figure 0.22: Simulation results of PV system behaviour in response to a step-change in PV arrays output current using three-phase current source inverter.

7.7. Summary

This chapter presented the operation and control structures of a CSI in island and grid-connected modes. The control systems used in this chapter, namely proportional-resonance (PR) using phase variables and proportional-integral (PI) in the *dq*-frame, have been discussed and evaluated by simulation and experimentation. From these control systems, proportional-integral (PI) control in the *dq*-frame was selected for further investigation of the suitability of the proposed direct regular sample PWM (DRSPWM) technique in a grid-connected mode. The proposed system has been tested over the entire P-Q operating range, including lagging, leading and zero power factor. In addition, the feasibility of the proposed system to operate in a passive network with no generation where the inverter sets the voltage in the same way as a voltage source inverter and synchronous machines during black-start was demonstrated. This is one of the distinctive features of the proposed DRSPWM technique. For completeness, an additional case study was presented, illustrating typical PV CSI inverterimplemention, with maximum power point tracking.

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Chapter Eight

Conclusions

8.0. General conclusion

This thesis discussed grid integration of the medium-scale photovoltaic (PV) system using voltage and current source inverters. Its main focus is on modulation and control strategies that may facilitate low-loss operation of a PV system at low and medium voltage levels. To achieve this objective, six-pulse voltage and current source inverters were used as interfacing options throughout this thesis. Chapter two reviewed the most commonly used voltage source inverter (VSI) topologies that are normally used for interfacing of the PV system to the grid. The suitability of each topology for PV application (power loss, partial shading and number of conversion stages, etc.) was discussed. Based on the discussions presented in chapter two, the three-phase two-level VSI is selected as a suitable interfacing option to be used for the grid integration of the PV system in this thesis. This is due to simplicity of the two-level converter power circuit, and its applicability to medium power applications, with ac rated voltage ranging from 415V to 11kV (line-to-line).

Chapter three briefly reviewed the existing pulse width modulation (PWM) strategies for VSI, and highlighted their suitability for power generation in a harsh grid mode. Based on the discussion on this chapter, traditional space vector modulation that was developed on assumption of balanced three voltage vectors is abandoned in favour of selective harmonic elimination PWM and sinusoidal PWM with 3^{rd} harmonic injection. This is because the traditional space vector modulation technique with circular trajectory (and equal side hexagon) is valid only during balanced ac voltage, which cannot be guaranteed during operation at distribution level in grid mode. The use of modified space vector modulation with an elliptical trajectory is possible, but it increases the complexity of the implementation and dwell times calculations. The selected modulation strategies are justified on the grounds that they can match space vector modulation in terms of dc link utilization, and they offer robust performance during unbalanced network operation. As part of thesis contribution, this chapter

proposed a new selective harmonic elimination (SHE) strategy that expliots the 3rd harmonic magnitude in the phase voltage to preserve the improved dc link utilization over the full modulation index range by avoiding pulse dropping problems. An additional advantage is that it simplified the solution of the SHE equations (it is simple to find an initial set of angles that can be used to calculate the switching angles for the entire modulation index range). These features can be used to simplify pratical realization of SHE at high modulation indices when a large number of harmonics are eliminated.

In chapter four, several of control structures for islanding and grid operation of the voltage source inverter were presented, including their experimental substantiations. It has been demonstrated using a scale-down prototype that the proposed SHE with a synchronous frame PI control structure allows operation of the grid connected VSI, with an effective switching frequency of less than 1kHz. The use of SHE does not compromise any grid connected inverter functionalites that are normally provided when VSI is controlled using carrier based PWM strategies. Furthermore, the output voltage and current waveforms achieved with SHE are within allowable IEEE and IEC standards, and reduced conversion losses. Simulation and experimental results for the grid connected inverter presented in this chapter have shown that SHE with 950Hz effective switching frequency is able to match SPWM with 3rd harmonic injection that uses 2kHz switching frequency, in terms of waveforms quality, and control flexibility of the active and reactive powers. In the context of PV, this showed the potential usefulness of the proposed SHE in improving efficiency of PV inverters. Similar implementation can be extended to multilevel inverter topologies. This is,however, out of the scope of this thesis.

Chapter five presented a brief review of the current source inverter (CSI) topologies that suit PV applications, with the emphasis on the six-pulse bridge. Also, it reviewed CSI modulation strategies. Additionally, this chapter proposed a new direct-regular sampled pulse width modulation (DRSPWM) strategy with the advantage of simpler implementation than the existing CSI modulation strategies. Detailed comparison that shows the superiority of the proposed DRSPWM over SPWM, SVM and SHE was presented. This comparison has shown that the proposed DRSPWM has fewer

switching transitions than its counterparts, and this indicates lower switching loss. Simulation and experimental results were incorporated to assist this analysis.

Chapter six presented a dc current offset compensation technique that can be used to reduce the overall cost of the solar farm by allowing transformerless inverter operations within farm, and uses a single power transformer at the point of common coupling to the grid. The presented dc compensation technique can be implemented using voltage or current source inverters. However, it has been found that the CSI was inappropriate due to its slow dynamic response, and for this reason only the VSI option was considered in the experimental validation. It was demonstrated that the VSI incorporating with the proposed technique was able to suppress dc current offset to zero in the output phase currents that exist in grid connected parallel inverters within a solar farm before entering the main interfacing transformer to the ac grid. Hence, the risk of transformer saturation can be avoided. Furthermore, this permits transformerless inverter operation within the farm.

Grid integration of a current source inverter using the proposed modulation strategy and suitable control structures was discussed in chapter seven. It has been demonstrated that the grid connected CSI with the proposed DRSPWM was able to provide all the flexibility needed for grid operation, including provision of leading and lagging reactive power, and zero power factor. Additionally, the viability of the proposed DRSPWM for islanding mode was demonstrated using simulation and by experiment, including black start operation. From this chapter, it is possible to conclude that when a current source inverter is correctly controlled, it has the potential to match the performance of the voltage source inverter in a wide range of grid operations.

8.1. Author's contributions

Main contributions of this thesis are:

(a) A new implementation of selective harmonic elimination for voltage source inverters that exploits 3rd harmonic injection is proposed that has the following advantages:

- Switching losses are suppressed by adopting a switching frequency less than 1kHz.
- Improved dc-link voltage utilization and avoidance of pulse dropping at low and high modulation indices (injection of the 3rd harmonic in the phase voltage does not produce narrow pulses in conventional SHE implementation. Instead it redistributes the pulse evenly over quarter fundamental cycle). This is achieved despite the use of an offline look-up table.
- Simplified solutions of the SHE nonlinear transcendental equations, and in some cases production of a unique solution with extended modulation index range for both arrangements where the phase voltage starts for $-\frac{1}{2}V_{dc}$ or $\frac{1}{2}V_{dc}$.

(b) The proposed new direct-regular sampled pulse width modulation (DRSPWM) strategy for the current source inverter offers the following advantages:

- Reduces complexity of CSI gate signal generation by elimination of logic mapping circuitry, hence implicit pulse pattern generation of the carrier based modulation is avoided.
- Offers the same degree of freedom, flexibility and dc link utilization as space vector modulation, while expecting to maintain the robustness of the carrier based SPWM during unbalanced operation in a grid connected environment.
- Some of the proposed switching sequences in DRSPWM constitute half the switching frequency per device compared to carrier-based PWM, thus lower switching losses are anticipated.
- Feasible to operate in a passive network with no generation where the inverter sets the voltage like a voltage source inverter and synchronous machines during black-start.

(c) The proposed technique for suppression of dc current offset injection into ac grids is applicable to medium-scale solar farms or any group of grid connected inverters confined within relative small area. The proposed technique offers the following advantages:

- Does not rely on high-precision current measurement devices and does not use any form of complex transformer as discussed in the open literature.
- At least one inverter must be designated to perform dc offset compensation besides its basic function of active power interfacing to the ac grid. This inverter is required to compensate for all dc offsets that may exist in the total phase current before reaching the main interfacing transformer. The risk of transformer saturation is therefore avoided.
- Allows transformerless operation of all inverters within the solar farm, and uses one interfacing transformer at the point of common coupling to the grid to reduce the capital cost of a medium-scale solar farm.

8.2. Recommendations for future research

- Investigate the viability of the proposed DRSPWM during low-voltage ride-through and unbalanced operation of the grid connected current source inverters.
- Extension of the DRSPWM strategy to multilevel current source inverters.
- Investigate the possibility of extension of the modified SHE with 3^{rd} harmonic injection to multilevel voltage and current source inverters.

Appendix A

Real-time dSPACE processor board

A.1. dSPACEDS1006 DSP processor board

The DS1006 uses a single-core AMD Opteron™ processor as the real-time processor (RTP) to process real-time models. The RTP calculates real-time models and accesses the I/O boards via the PHS bus. The key features of DS1006 board are:

- X86 processor technology
- Fully programmable from Simulink
- High-speed connection to all dSPACE I/O boards via PHS bus
- Multiprocessor system of several DS1006 processor boards via fiber-optic connection (gigalinks).

Figure A.1 shows the DS1006 board that is used to interface and communicate between I/O boards and the MATLAB/SIMULINK simulation environment. The DS1006 processor board can be programmed via a real-time interface (RTI) in Simulink. Other useful features of this board in the Simulink environment are it is easy to access to the entire range of I/O boards and to alter simulation parameters such as solver options or simulation time as well as to generate C-codes.

Figure A.1: DS1006 real-time processor board

A.2. I/O board

The I/O boards that are designed in dSPACE are DS5101 Digital Waveform Output (DWO) and DS2002 ADC boards. The DS5101 Digital Waveform Output board is designated to generate complex, high-speed digital signals at high resolution. This board can generate various TTL pulse patterns on up to 16 channels with a time resolution of 25ns. The limitations of DS5101 are as follows:

- The minimum pulse length is 250ns.
- It is not possible to generate PWM signals or similar signals which are constantly low or high, for example, PWM signals with 0% or 100% duty cycle. There will always be a remaining pulse of at least 250ns length.

The DS2002 board provides an ADC unit featuring 2 parallel A/D converters (ADC1, ADC2) multiplexed to 16 channels each (signals VIN1 … VIN16 and VIN17 … VIN32). The A/D converters have the following characteristics:

- 4-, 8-, 12- or 16-bit resolution (selectable for each of the 2 A/D converters individually)
- ±5V or ±10V input voltage range (selectable for each of the 2 A/D converters individually)

Figure A.2 shows the I/O boards that are used for experimentation. Voltage and current feedback signals from transducer boards are connected to the DS2002 ADC channels while the DS5101 board is used for PWM generation foe the voltage and current source inverters.

Figure A.2: I/O DS5101 DWO and DS2002 ADC boards

A.3. dSPACE Control Desk 3.7

dSPACE Control Desk is an experimental software platform that provides all the functions to control, monitor and automate experiments and makes the development of controllers more effective. Figure A.3 illustrate an example of control desk layout that display the waveforms of controlled variables in real-time. The control variables can be run and stopped in real-time, and saved in comma separated values (.csv) format.

Figure A.3: Example of dSPACE control desk layout

Appendix B

Arbitrary custom pulse patterns code generation in dSPACEDS5101

B.1. Custom pulse pattern codes generation in DS5101 Digital Waveform Output

The implementation of a custom digital waveform output (DWO) application starts with writing the source file (.src).The source file is written in a plain ascii text file. Using DWO compiler (DWOCOMP), C-source (.c) and related files such as header file (.h), list file (.lst) and DWO simulator input file (.dat) are generated. The C-file contains the encoded DWO object code and a load routine for downloading the object code to the DS5101 by a master DSP. The header file contains address definitions for all timing parameters declared in the DWO source file and channel mask. These definitions allow easy access to individual timing parameters by the master DSP. All results and error messages are reported in a list file. These files are added to custom DWO program to be executed on the DS5101 board. Figure B.1 summarizes data flow compilation of customized codes in the DS5101 platform.

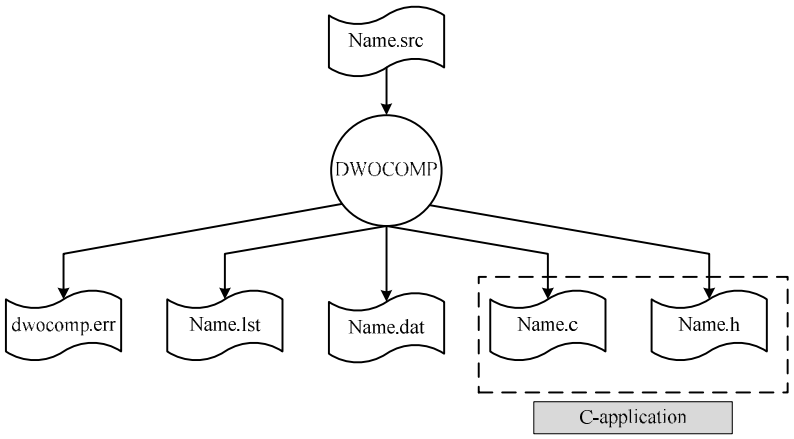

Figure B.1: Data flow compilation of customized codes in DS5101DWO

B.2. Sample of the custom source codes for PWM generation for a current source inverter

A sample of custom source code for pulse width modulation generation for a current source inverter is presented. There are six designated channels, namely channel 1, 3 and 5 for upper switches and channel 2, 4 and 6 for bottom switches. To synchronize the six output signals, a master clock is generated on an additional channel (channel 7). The high and low level durations can be adjusted independently through parameters ta1..ta4, tb1..tb4, or tc1..tc4 for the respective PWM phase. Since the DS5101is unable to generate PWM signals with duty cycle value of 0 and 1, there will be a high pulse of 250ns generated for duty cycle values near or equal to 0. For duty cycle values near or equal to 1, a high pulse of 800ns is generated.

```
# ========================================================================

unit ticks                # all delays given in 25ns ticks

delay t0  0               # PWM period / 2
delay t0a 0               # (PWM period / 2) - interruptshift
delay t0b 0               # interruptshift
delay ta1 0               # t_low/2,  phase A
delay ta2 0               # t_high,   phase A
delay ta3 0               # t_high/2, phase /A
delay ta4 0               # t_low,    phase /A
delay tb1 0               # t_low/2,  phase B
delay tb2 0               # t_high,   phase B
delay tb3 0               # t_high/2, phase /B
delay tb4 0               # t_low,    phase /B
delay tc1 0               # t_low/2,  phase C
delay tc2 0               # t_high,   phase C
delay tc3 0               # t_high/2, phase /C
delay tc4 0               # t_low,    phase /C

# ------------------------------------------------------------------------
#  PWM block 1 (channels 1..7)
# ------------------------------------------------------------------------

ch1                       # phase A
reset, wait;              # low after reset, wait for trigger
begin:
syncen,                   # use new data from DSP
nop, ta1;                 # delay t_low/2
set, ta2;                 # set output high, delay t_high
reset, wait,              # set output low, wait for trigger
goto begin;               # loop

ch2                       # phase /A
reset, wait;              # high after reset, wait for trigger
begin:
syncen,                   # use new data from DSP
nop, ta3;                 # delay t_high/2
```

```
set, ta4;               # set output low, delay t_low
reset, wait,              # set output high, wait for trigger
goto begin;             # loop

ch3                       # phase B
reset, wait;             # low after reset, wait for trigger
begin:
syncen,                   # use new data from DSP
nop, tb1;               # delay t_low/2
set, tb2;                 # set output high, delay t_high
reset, wait,              # set output low, wait for trigger
goto begin;      # loop

ch4                       # phase /B
reset, wait;            # high after reset, wait for trigger
begin:
syncen,                 # use new data from DSP
nop, tb3;                # delay t_high/2
set, tb4;               # set output low, delay t_low
reset, wait,              # set output high, wait for trigger
goto begin;             # loop

ch5                       # phase C
reset, wait;             # low after reset, wait for trigger
begin:
syncen,                  # use new data from DSP
nop, tc1;               # delay t_low/2
set, tc2;                # set output high, delay t_high
reset, wait,             # set output low, wait for trigger
goto begin;           # loop

ch6                       # phase /C
reset, wait;           # high after reset, wait for trigger
begin:
syncen,                  # use new data from DSP
nop, tc3;              # delay t_high/2
set, tc4;                # set output low, delay t_low
reset, wait,           # set output high, wait for trigger
goto begin;          # loop

ch7                       # master clock
reset, t0;              # low after reset
begin:
syncen,                 # use new data from DSP
   tr1, tr2, tr3,        # trigger channels 1..6
   tr4, tr5, tr6,
set, t0a;              # set output high, delay t0a
phsint,                # send interrupt to DSP
set, t0b;              # set output high, delay t0b
reset, t0,               # set output low, delay t0
goto begin;          # loop


updfunc all             # generate update function
g t0,  g t0a, g t0b
g ta1, g ta2, g ta3, g ta4,
g tb1, g tb2, g tb3, g tb4,
g tc1, g tc2  g tc3, g tc4;     # for all global delays
```

```
readfunc all             # generate read function
g t0,  g t0a, g t0b,
g ta1, g ta2, g ta3, g ta4,
g tb1, g tb2, g tb3, g tb4,
g tc1, g tc2  g tc3, g tc4;     # for all global delays
```

B.3. Simulink s-function template for DS5101DWO block

DS5101 RTI blockset provides DS5101DWO block to enable parameter updating of a custom DWO application in Simulink model. A simulink s-function template is serviced by RTI, where DWO C-source file, header file, and a number of parameters must be specified. A s-function template is edited and compiled using MATLAB command mex<file name>.c in the same working directory as C-source, header and other related files.

A sample of s-function template is presented as below.

```
#-------------------------------------------------------------------------------------------------#

#ifndef MATLAB_MEX_FILE
# include <ds5101.h>
# include <ap5101.h>
# include <rti_msg_access.h>
# include <rti_common_msg.h>
#endif

#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME pwm3_CSI
#ifndef MATLAB_MEX_FILE
#include "PWM3_INTSHIFT.h"
#include "PWM3_INTSHIFT.c"

#define NUM_DWOVARS 9

#define CHANNELMASK DS5101_PWM3_INTSHIFT_CHANNELS
#define DS5101_PWM3_INTSHIFT_GW_T0              0x000F0001
#define DS5101_PWM3_INTSHIFT_GR_T0              0x00010001
#define DS5101_PWM3_INTSHIFT_GW_T0A             0x000F0002
#define DS5101_PWM3_INTSHIFT_GR_T0A             0x00010002
#define DS5101_PWM3_INTSHIFT_GW_T0B             0x000F0003
#define DS5101_PWM3_INTSHIFT_GR_T0B             0x00010003
#define DS5101_PWM3_INTSHIFT_GW_TA1             0x000F0004
#define DS5101_PWM3_INTSHIFT_GR_TA1             0x00010004
#define DS5101_PWM3_INTSHIFT_GW_TA2             0x000F0005
#define DS5101_PWM3_INTSHIFT_GR_TA2             0x00010005
#define DS5101_PWM3_INTSHIFT_GW_TB1             0x000F0006
#define DS5101_PWM3_INTSHIFT_GR_TB1             0x00010006
#define DS5101_PWM3_INTSHIFT_GW_TB2             0x000F0007
#define DS5101_PWM3_INTSHIFT_GR_TB2             0x00010007
#define DS5101_PWM3_INTSHIFT_GW_TC1             0x000F0008
#define DS5101_PWM3_INTSHIFT_GR_TC1             0x00010008
#define DS5101_PWM3_INTSHIFT_GW_TC2             0x000F0009
```

```
#define DS5101_PWM3_INTSHIFT_GR_TC2             0x00010009
#define DS5101_PWM3_INTSHIFT_CHANNELS           0x0000000F

#define DS5101_LOAD() \
  ds5101_pwm3_intshift_load(boardBase, CHANNELMASK)

#define DS5101_INIT_ALL() /*\
  ds5101_pwm3_intshift_init_all(boardBase, 0.0, 0.0)*\

#define DS5101_UPDATE_ALL() \
  ds5101_pwm3_intshift_update_all(boardBase, u(0), u(1),u(2),u(3),u(4),u(5),u(6),u(7),u(8))

#endif
```

Appendix C

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Appendix D

Summary of relevant published work by the author

[1] S.A.Azmi, G.P.Adam, K.H.Ahmed, S.J.Finney, and B.W.Williams, "Grid Interfacing of Multimegawatt Photovoltaic Inverters," *Power Electronics, IEEE Transactions on,* vol. 28, pp. 2770-2784, 2013.

Abstract— This paper investigates the suitability of selective harmonic elimination (SHE) for low loss multi-megawatt grid connected photovoltaic (PV) inverters. The proposed system is able to meet utilities regulations, IEEE and IEC standards. In an attempt substantiate the potential superiority of SHE over carrier based or space vector pulse width modulation (PWM), this paper demonstrates SHE may allow grid connected PV inverters to be controlled using a switching frequency of less than 1kHz while the inverter is still able to provide necessary operation features such as independent control of active and reactive powers and operation control simplicity. For system validation, experimental results with SHE are compared to the case when the inverter is controlled using third harmonic injection PWM, with a 2kHz switching frequency. Furthermore, the paper proposes a new implementation technique for SHE that utilizes the 3^{rd} harmonics to spread the switching angles over 90^{o} instead of being located in a narrow range as generated when using conventional techniques, along with increases in modulation index. The advantages of the proposed technique include simplicity in implementation and flexibility in PWM waveforms. Simulation and experimentation demonstrate agreement, which validates the practicability of the proposed system.

[2] S.A.Azmi, G.P.Adam and B.W.Williams, "New Direct Regular Sampled PWM Applicable for Grid and Islanding Operation of Current Source Inverters," *Power Electronics, IET Transaction on*, pp.1-17,2013.(doi:10.1049/iet-pel.2013.0235)

Abstract—This paper presents new direct regular sampled pulse width modulation for grid connected three-phase current source inverters. The theoretical basis of the presented modulation strategy is described in detail and includes dwell time calculations and switching sequence selection. The modulation strategy is simple and suited for digital implementation, and has the flexibility and degree of freedoms of space vector modulation. This is because some switch sequences ensure a minimum number of switching transitions per fundamental cycle, unlike other methods presented in the literature. It is therefore applicable for high-power medium-voltage applications. The validity of the presented direct regular sampled pulse width modulation is confirmed using simulation and experimentation of a current source inverter, in open and closed loop operation.

[3] S.A.Azmi, K.H.Ahmed, S.J.Finney, and B.W.Williams, "Comparative Analysis between Voltage and Current Source Inverters in Grid-Connected Application", *Renewable Power Generation (RPG2011), IET International Conference on*, pp1-6, 2011.

Abstract—The voltage source inverter (VSI) is mainly used for grid interfacing of distributed generation systems. In order to boost the voltage of a renewable energy source to the required dc voltage level, a dc-dc converter is necessary even though the cost and complexity of the system are increased. Thus, in improving the cost and life expectancy of the power electronic interface, a current source inverter (CSI) is an alternative which offers short-circuit protection capabilities, implicit voltage boosting and a simple ac-side filter structure. However, it has attracted less research attention since it is purported to have drawbacks in term of high conduction losses and inefficient inductive energy storage on its dc-side. With reference to advantages and disadvantages of both inverter types, this paper presents a comprehensive comparative analysis with respect to the topological and operational features of the inverters. The comparison includes the power circuit, semiconductor constraints, cost, dc input filtering, steady-state, transient performance and power semiconductor losses. The analytical expectations of the systems are verified using MATLAB/ Simulink software package.

[4] S.A.Azmi, G.P.Adam and B.W.Williams, "New Modulation Strategy for Three-Phase Current Source Inverters", *Power Engineering, Energy and Electrical Drives (POWERENG 2013), 4th IEEE International Conference on*, pp1110-1115, 2013.

Abstract— This paper proposes a new regular sampled pulse width modulation (PWM) for three-phase current source inverters. The theoretical basis of the proposed modulation strategy is described, including dwell time calculations and switching sequence selection. This strategy is well suited for digital implementation, and enjoys all the flexibilities and degree of freedoms as in space vector modulation. In addition, it ensures a minimum number of switching transitions per fundamental cycle, unlike other PWM methods. It is therefore promising for high-power medium-voltage applications. The validity of the proposed modulation strategy has been confirmed using simulation and experimentation. To furthermore substantiate the superiority of the proposed modulation strategy against other PWM methods, its performance is compared to sinusoidal PWM, selective harmonic elimination, and space vector modulation.