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Pulsed MOSFET based Linear Transformer Driver

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Doctor of Philosophy

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DECLARATION OF AUTHENTICITY AND AUTHOR'S RIGHTS

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed:

Date:

Dedication

To my family

Abstract

Pulsed power flash radiography is a rapidly growing technology which involves the generation of intense and short bursts of electric pulses to generate high energy X-rays to inspect dense objects. The generation of fast transition, short width, repetitive pulses for effective output requires switching technology which has limitations. From the traditional slow switching gas trigger switches, switching technology has evolved to semiconductors which has led to improved switching characteristics and delivered pulse shapes. One such semiconductor which is of interest in flash radiography is a power MOSFET. Due to superior switching speeds, repetition rates and modularity, MOSFETs are a strong contender in future pulsed power applications. This thesis focuses on the design of a MOSFET based pulsed power system capable of generating 2.2kV, 200A pulses with turn on and turn off times of less than 10ns and 20ns respectively. In order to achieve the target specification, a high speed current source MOSFET gate driver design specific to the application is proposed. Further, an inductive voltage adder system which utilises multiple lower voltage pulse sources driven by MOSFETs and outputs a higher voltage which is the summation of the total number of voltage sources, is designed to be compatible with the proposed gate driver scheme. A compact high power density pulsed power prototype is demonstrated which provides a benchmark for future research into the development of a larger scale system for flash radiography.

Acknowledgment

I would like to express my deepest gratitude to my supervisors Professor Stephen Finney and Professor Barry Williams for their continuous guidance, advice and support throughout the PhD. Owing to their contribution it has been possible to give a well-defined direction to the project. Due to their encouragement, it was also possible to undertake a research visit to the pulsed power group at Fudan University, China and complete a two month research placement which gave me a wider experience in the research area of pulsed power as well as improving my research confidence.

My special thanks are given to Dr John Fletcher for introducing me to the interesting area of pulsed power and for offering me continuous guidance and support during the initial stages of my research. I acknowledge Dr T.C Lim for sharing his practical experiences and helping me through the technical aspects of the project. It has truly been a pleasure working alongside him. I give warm thanks to Mr Charles Croser for being the backbone of this project with regards to the physical design of the system, sourcing of components and being a friendly companion in the lab.

Funding from AWE Aldermaston is acknowledged. In particular, special thanks are due to Mark Sinclair of AWE for his input on pulsed power systems through regular meetings and at conferences.

Finally, I would like to thank my Parents, the lifelong friends I have made in Glasgow and the special person in my life, Indu Manoharan for giving me all the support through the good and bad times and helping me achieve my goals.

List of Abbreviations

AWE	Atomic Weapons Establishment;
BJT	Bipolar Junction Transistor;
DSRD	Drift Step Recovery Diode;
ESD	Electro Static Discharge;
FHCT	Fast High Current Thyristor;
FWHM	Full Width Half Maximum;
GTO	Gate Turn Off;
IGBT	Insulated Gate Bipolar Transistor;
IVA	Inductive Voltage Adder;
LTD	Linear Transformer Driver;
MITL	Magnetically Insulated Transmission Line;
MOSFET	Metal Oxide Semiconductor Field Effect Transistor;
MELF	Metal Electrode Leadless Face;
PIVA	Prototype Inductive Voltage Adder;
PFL	Pulse Forming Line;
PCSS	Photo Conductive Semiconductor Switch;
RP	Rod Pinch;
SG	Spark Gap;
SP	Self Pinch;
SMP	Self Magnetic Pinch;
SOS	Semiconductor Opening Switch;
SIThy	Silicon Induction Thyristor;
TVS	Transient Voltage Suppressor;

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Chapter 1

Introduction to pulsed power systems

1.1 Background

Pulsed power is high power, short duration pulse technology which deals with peak powers from hundreds of kilowatts to terawatt levels and pulse durations from nanoseconds to milliseconds [1]. In 1920, Erwin Marx developed a novel form of high voltage pulse generator for lightning testing of high voltage power transmission equipment and this represents the beginning of pulsed power. One of the earliest forms of pulse generation used a Marx generator, for which the circuit diagram is shown in Figure 1.1.

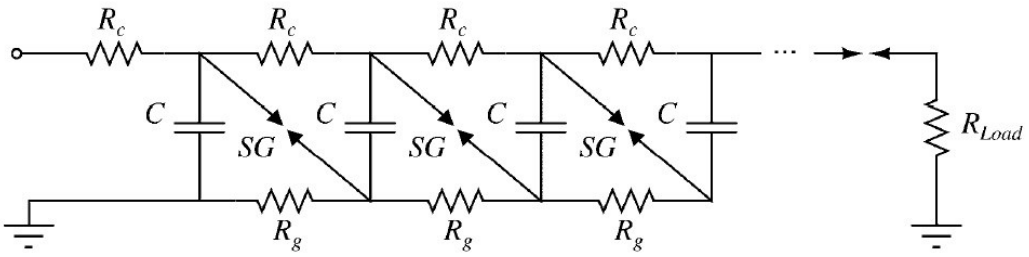


Figure 1.1: Schematic circuit of a Marx generator using spark gaps.

Initially, a set of N parallel connected capacitors are each charged to voltage V_{charge} in parallel. The capacitors are then connected in series to switch an output pulse voltage that is a multiple N of the charging voltage, V_{charge}. The series connection occurs due to the sequential over-voltage and breakdown of the spark gaps (SG) once the first gap breaks down. Spark gaps play an important role in pulse power systems.

Since its invention, the Marx generator has been widely researched and developed in both civil and military industries.

1.2 Application

Pulsed power can be used for various applications ranging from non-destructive inspection of metals, food processing, medical treatment, water treatment, exhaust gas treatment, ozone generation, particle acceleration, and X-ray generation. This thesis specifically focuses on the application of pulsed power in flash radiography and therefore most of the discussion will be related to the following application. J. C. Martin of the Atomic Weapons Establishment (AWE) proposed radiography as a diagnostic tool for explosively driven hydrodynamic experiments, providing essential data on the properties of materials placed under extreme conditions where shockwave pressures far exceeds those found in the earth's core [2]. Flash radiography is the production of intense X-ray beams of short-duration (10 to100 ns) which are a thousand times more powerful than medical X-rays. Figure 1.2 shows a typical X-ray configuration. X-ray imaging is used to measure high-speed dynamics of dense materials. The pulsed power requirement in large X-ray machines is of sub-microsecond pulses of 1MV to 10MV and approximately 1MA levels to drive the electron beam and produce X-rays by the bremsstrahlung mechanism. This mechanism is the generation of electromagnetic radiation by the deceleration of a charged particle when deflected by another charged particle. The pulse rise time should be 50ns to 100ns or less. These requirements led to the development of both fast rise time Marx banks with high voltage, high current and Pulse Forming Line

(PFL) techniques for the shaping of pulses and channelling the energy to the X-ray diode.

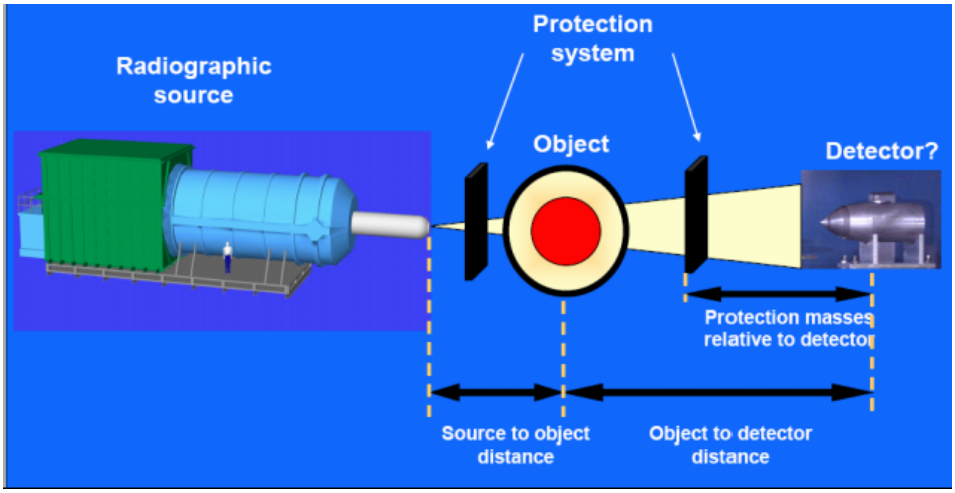


Figure 1.2: Typical X-ray system configuration [2].

1.2.1 X-ray generator

Figure 1.3 is a block diagram of a classical X-ray generator setup which includes a Marx generator, Blumlein Pulse Forming Line (PFL), Magnetic Insulation Transmission Line (MITL), and X-ray diode. The Marx bank charges a Blumlein PFL at the full operating voltage of the machine. One self-closing switch initiates the pulse forming action of the Blumlein. The PFL transmits a pulse of typically less than 100 ns duration to the e-beam diode to generate X-rays. Figure 1.4 shows a model of a Blumlein pulsed power machine used by AWE.

Figure 1.3: Block diagram of an X-ray generator.

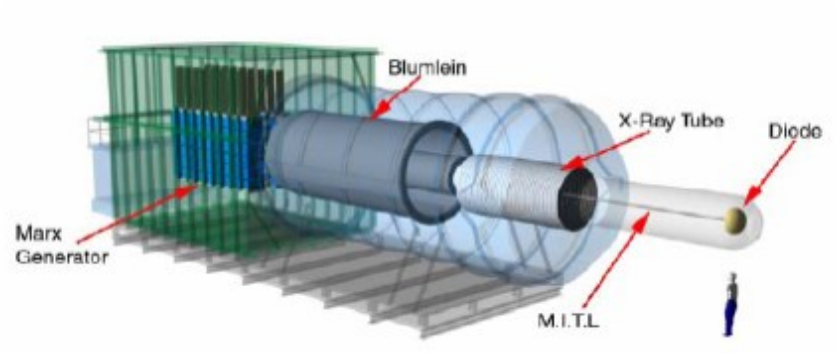
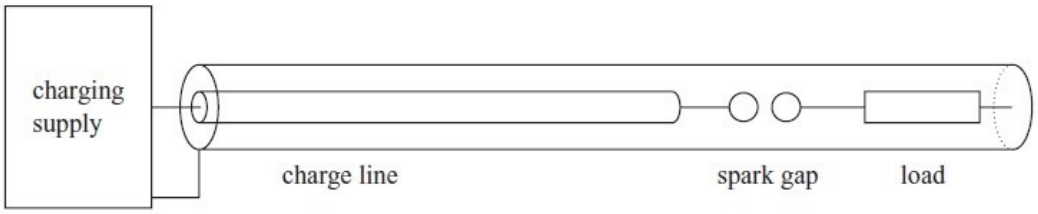


Figure 1.4: A typical X-ray generator setup [2].

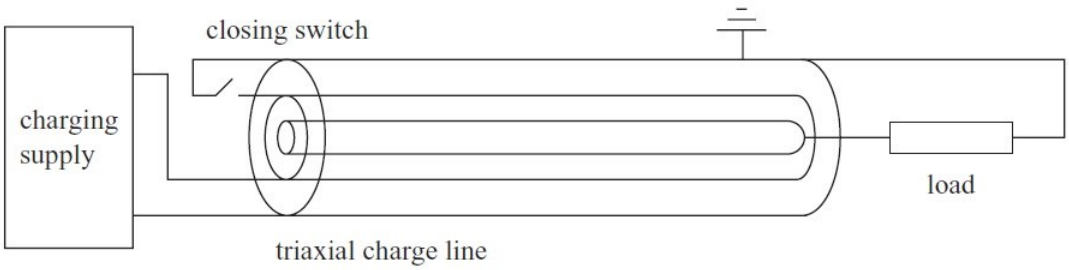
1.2.2 Pulse Forming Line (PFL)

The operational mechanism of the Marx generator has been described. A PFL uses circuit, switching, and transmission line techniques to achieve the pulse shape required by the load. There are two types of traditional PFL [1]. One is a standard PFL as shown in Figure 1.5(a) and the other is the Blumlein PFL as shown in Figure 1.5(b). In a standard PFL a length of cable or transmission line is charged to a DC voltage level V by a charging power supply. When the switch connecting the transmission line to the load is closed, the load begins to discharge the transmission line. The load pulse rise time is equivalent to the switching time. The values of voltage and current in the load may be found by solving the transmission line equations. In the case of a matched load, the load voltage is equal to half the charging voltage. A Blumlein PFL uses two charge lines with the load interposed as shown in Figure 1.5(b). For matched operation, the impedance of each of the charge lines should be one-half of the load impedance. The two lines are initially charged by a charging supply; the right-hand line charging path is through the load impedance. The closing switch is between the two plates (conductors) of the left-hand line. Closing the switch then launches a travelling wave into the left-hand line, and when

this wave reaches the load, the load voltage is developed. For matched operation, the magnitude of the load voltage impulse is equal to the charge voltage *V*. A disadvantage is that it produces greater pre-pulse as the stray capacitance prevents the two charge line conductors from being kept at exactly the same potential [4]. In addition, with the high MV requirements of pulsed power systems, the approach leads to large machines.



(a)



(b)

Figure 1.5: (a) Pulse Forming Line (PFL) and (b) Blumlein PFL [3] [4].

1.2.3 X-ray diodes

At the end of the X-ray machine, a diode is used to transfer the energy into a short pulse of Bremsstrahlung X-ray radiation. The diode's performance is judged by

the magnitude of the radiographic dose (rads) it produces and the size of the source (mm) from which the dose originates. The four most common diodes are the paraxial, self-pinched (SP), rod pinch (RP), and magnetically immersed [3].

A focusing cup is used to concentrate the stream of electrons to a small area of the target called the focal spot. The focal spot size is an important factor in the system's ability to produce a sharp image. The diode of interest to AWE is the self-magnetically pinched (SMP) diode. This diode is capable of producing a spot size of less than 3mm and 350 rads of X-rays at 1m [5]. The characteristic of interest to this particular project is its impedance, which varies between 65 to 40Ω.

1.2.4 Summary

The production of X-rays is characterised by the quality of the pulsed power source and the type of diode load. A SMP diode is a candidate for future flash radiography sources which can produce high radiation at small spot sizes. The quality of the pulsed power source is judged by the pulse shape it delivers which is a combination of fast rise and fall times and flat pulse top.

At present, AWE houses a number of pulsed power accelerators at the hydrodynamics facility in Aldermaston, UK. Based on the technology previously mentioned, the accelerators range in energy from 800kV to 10MV [6]. The machines are bulky in size, and single shot operated, and require oil insulation, and heavy maintenance. With time, these pulsed power machines are slowly being replaced by the newer and more flexible Inductive Voltage Adder (IVA) technology.

1.3 Inductive Voltage Adder technology

An alternative approach to using large Marx generators and pulse forming lines to achieve high voltages is to use the Inductive Voltage Adder (IVA) principle as illustrated in Figure 1.6 [7]. The *n* inductive cavities (cores) can be regarded as primary windings of a transformer. Each cavity is charged to an input voltage *V*, which is 1/*n* of the required output voltage. The inner stalk acts as the secondary windings of the transformer, which are connected in series to generate an output voltage. The output voltage is the summation of the voltages from each cavity, which in Figure 1.6 is *3V*.

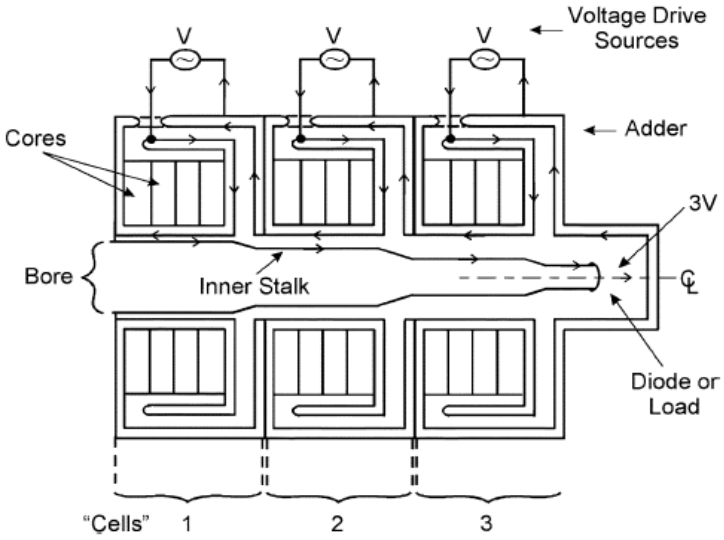
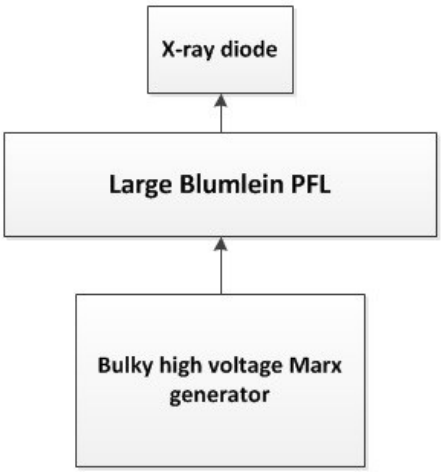


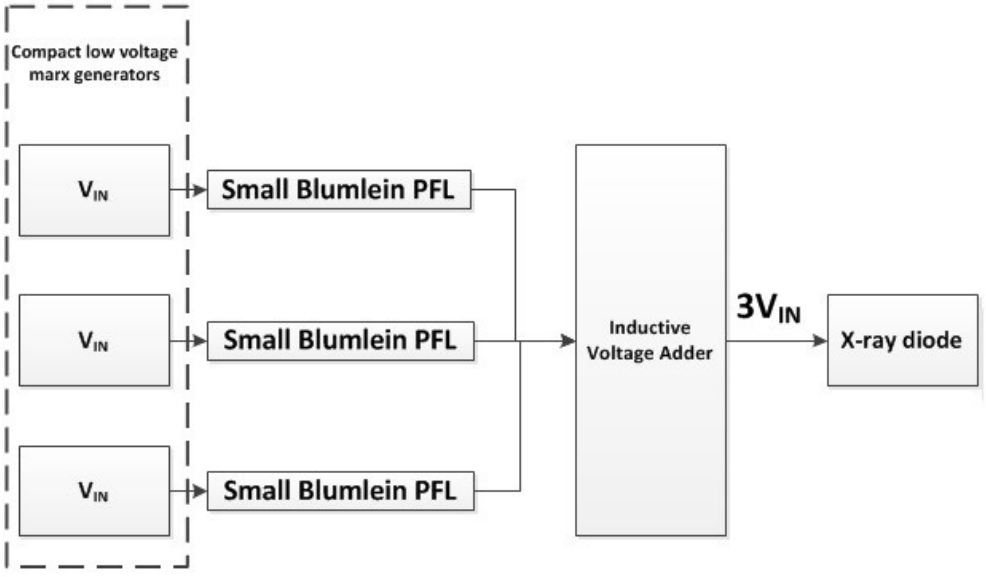
Figure 1.6: Inductive Voltage Adder (IVA) setup [7].

This offers unparalleled advantages over the conventional pulsed power architecture whereby increased flexibility, smaller size to weight ratio and higher output voltages can be achieved. Figures 1.7(a) and 1.7(b) illustrate the comparison between a conventional pulsed power system and an IVA.



Conventional pulse generator

(a)



Inductive Voltage Adder based pulse generator

(b)

Figure 1.7: Functional block diagram of (a) a conventional pulsed power system and (b) an IVA based pulsed power system.

A conventional system uses Marx generators and pulse forming lines which are rated at full output voltage. Therefore, significantly larger components are used. The high voltage isolation and insulation requirements are also higher. During maintenance periods, the whole system must be shut down. With an IVA configuration, smaller Marx generators and pulse forming lines can be used. This significantly reduces the size of each system. Consequently, its isolation and insulation requirements are also significantly reduced. If a fault condition develops in either of the smaller modules, it can be replaced with another. The machine can therefore be kept in operation. The modularity of the IVA gives increased flexibility, reduced maintenance costs, and reduced system size.

Figure 1.8 shows the configurations of a single IVA system and a 10-stage IVA flash radiography machine respectively. The 10-stage IVA machine is required to operate at 13 to 15MV and deliver a total current of 100kA. A possible configuration for this machine will be ten Marx generator driven water Blumlein PFLs of approximately 10Ω output impedance each feeding a single 1.5MV inductive cavity.

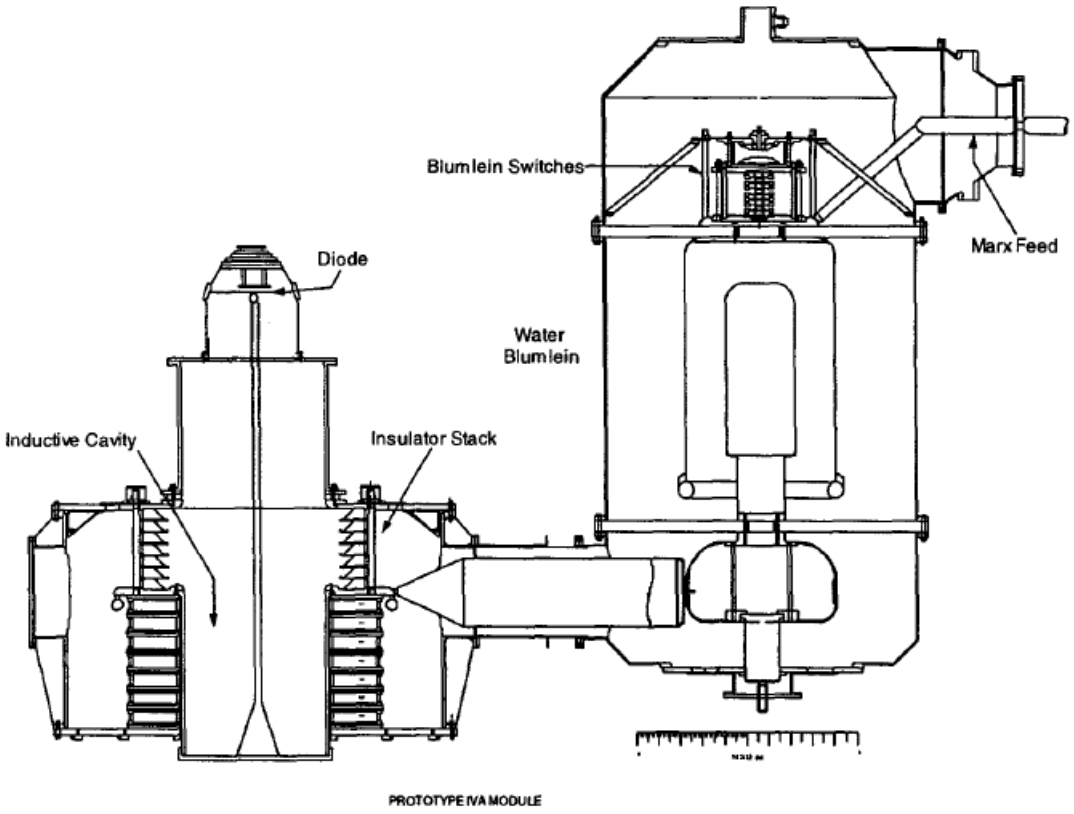


Figure 1.8: Prototype Inductive Voltage Adder (PIVA) [8].

Figure 1.9 shows a block diagram illustrating a Linear Transformer Driver (LTD) which is a variant of the original IVA technology, whereby the power source is formed from capacitors and switches surrounding the inductive cavity instead of an external power source such as a Marx generator.

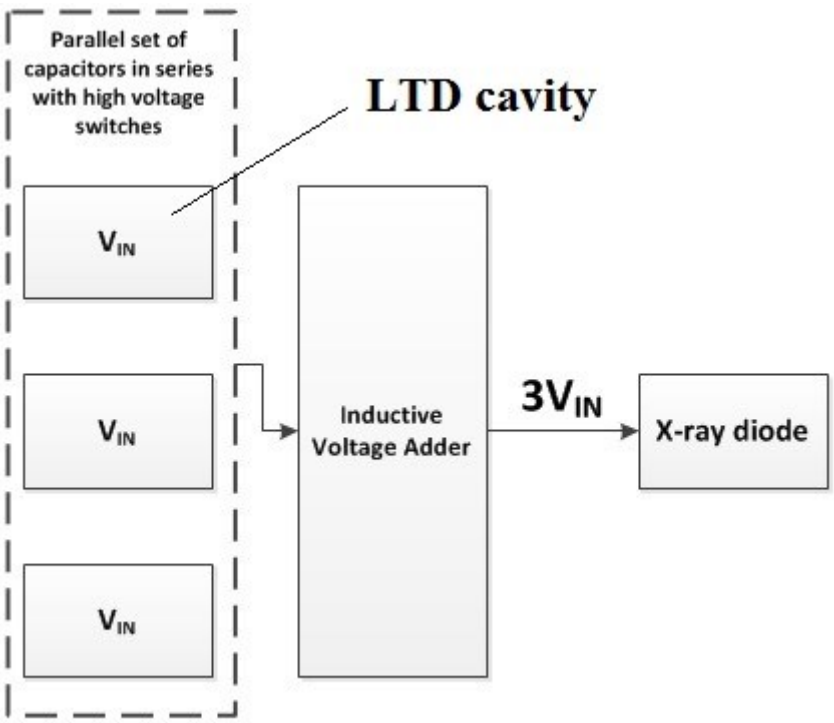


Figure 1.9: Functional block diagram of an LTD system.

An LTD cavity can be simplified to the equivalent circuit shown in Figure 1.10, which includes a switch, a charged capacitor, an inductor and a resistor. The switch represents all the cavity switches connected in parallel. The capacitance is equal to the sum of the capacitances of all the cavities. The inductance is equal to sum of all the inductances of the cavity and the resistance is equal to sum of the load resistance and cavity resistance. The salient feature of the approach is switching and inductively adding the pulses at low voltage through low inductance transfer and soft iron isolation. High currents can be obtained by feeding the cavity with many capacitors connected in parallel. High voltage can be achieved by inductively adding many stages in series. This is the working principle of LTD technology for pulsed power systems. The main advantage of LTD is elimination of Marx generator and Blumlein PFLs. Sandia National Laboratories is developing Linear Transformer Drivers as

shown in Figure 1.11 which is a technique for constructing high-current, high voltage pulses [9-11]. The LTD structure is compact, simple and flexible.

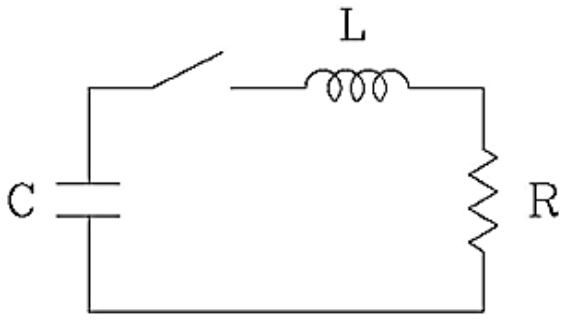


Figure 1.10: A simple LTD equivalent circuit.

Figure 1.11: The twenty parallel single-stage circuits in a single LTD cavity are triggered simultaneously to produce a 100kV, 0.5 MA, 60 ns pulse. [11]

1.4 Motivation for the thesis

Based on the aforementioned introduction to pulse power-driven flash radiography systems, such systems are characterised by high energy, high voltage, high-current, and pulse widths of less than 100ns. Currently, it is usual to adopt gas discharge tubes as the device to switch the Marx generators into the Blumlein PFL of the X-ray pulse power generator. With the demand for faster edge pulses, high reliability switches, and repetitive pulsing, conventional switching systems are presented with a difficulty satisfying the requirements for modern pulsed power systems.

The present challenges in pulsed power flash radiography are to improve pulse switching times, repetition rates and reproducibility, to lower maintenance, and to achieve an overall reduction in the system size. The transition to IVA based pulsed power systems is a significant step for AWE towards achieving higher quality pulses and a more flexible and reliable system. The LTD technology has shown further potential in eliminating the large Marx generator and Blumlein PFL and replacing them with capacitor and switch stacks surrounding the magnetic core. This has resulted in a significant improvement in switching speeds, reduced system size, better pulse shapes, increased system reliability, and lower costs. There is however further demand for improvement in all the mentioned areas. The modularity of an LTD presents an opportunity for high-voltage solid-state semiconductors such as MOSFETs, IGBTs, thyristors and GTOs as a replacement agent for gas/vacuum tubes of X-ray pulse power generators. AWE has focused its attention towards MOSFETs due to their distinctive capability in high speed repetitive switching,

modularity, and reliability. With rapid improvement in their power handling capabilities, they show applicability potential in small flash radiography systems.

The presented research study is motivated by the need to enhance the capability of pulsed power systems using Power MOSFET technology. Power MOSFETs of low power have demonstrated switching times in the order of 10ns using commercially available gate drivers. In order to achieve switching speeds of less than 10ns requires conceptual redesign of the MOSFET system using advanced gate drive techniques. The project aims to contribute to the area of high voltage pulsed power engineering by making use of the latest available MOSFET technology. The study aims to further advance the ability of MOSFET driven pulsed power systems towards high power applications which may be of potential use to AWE towards its goal of developing high speed repetitive pulsed power systems for flash radiography.

1.5 Work addressed in this thesis

The body of work described in this thesis takes the proven concept of solid-state Linear Transformer Driver (LTD) technology and enhances it through the design of new gate driver technology and a modified system layout adapted to the design.

1.5.1 Thesis structure

The thesis is presented as follows:

- Chapter 2 provides basic background theory on power electronic devices and surveys literature on solid state switching devices and LTD technology.

- Chapter 3 details the design and analysis of a high speed MOSFET gate driver for pulsed power applications.
- Chapter 4 discusses the design considerations for a pulse transformer, modular design of the LTD module, and experimental results for prototype two-stage and four-stage LTD systems. A simulation model is developed based on the experimental results, which is used to scale design a larger pulsed power system.
- Chapter 5 contains the conclusion and discussion of the overall thesis results while suggesting possible future research.

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Chapter 2

Literature Survey

2.1 Introduction

Currently, gas discharge switches are commonly used in pulsed power systems. System lifetime, efficiency and maintenance are however restricted due to the structure of the discharge gap [1]. In most pulsed power systems, the output pulse voltage, pulse repetition rate, and lifetime are determined by the capabilities of the switches. In the last 20 years, the evolution of pulsed power technology has largely relied on power switching device improvements. Rapid developments in the switching performance mark the evolution of pulsed power and its applications. By replacing conventional spark gaps with solid state switches, pulsed power system performance has been improved greatly. As a result, solid state switches have drawn particular attention due to their superior properties such as low cost, high efficiency, and flexibility. Recently, solid-state switching devices have increased in voltage and current rating, and *di/dt* and *dv/dt* rating. The power and frequency capabilities of different semiconductors are shown in Figure 2.1.

Chapter 1 introduced Flash radiography, the Inductive Voltage Adder (IVA), and Linear Transformer Driver (LTD) technology. The use of power MOSFETs in an LTD configuration is proposed as the research theme for this thesis. This chapter focuses on the power electronics and LTD related literature which justifies the use of

MOSFETs in the application and the advantages of an LTD system in comparison to other pulsed power generation techniques.

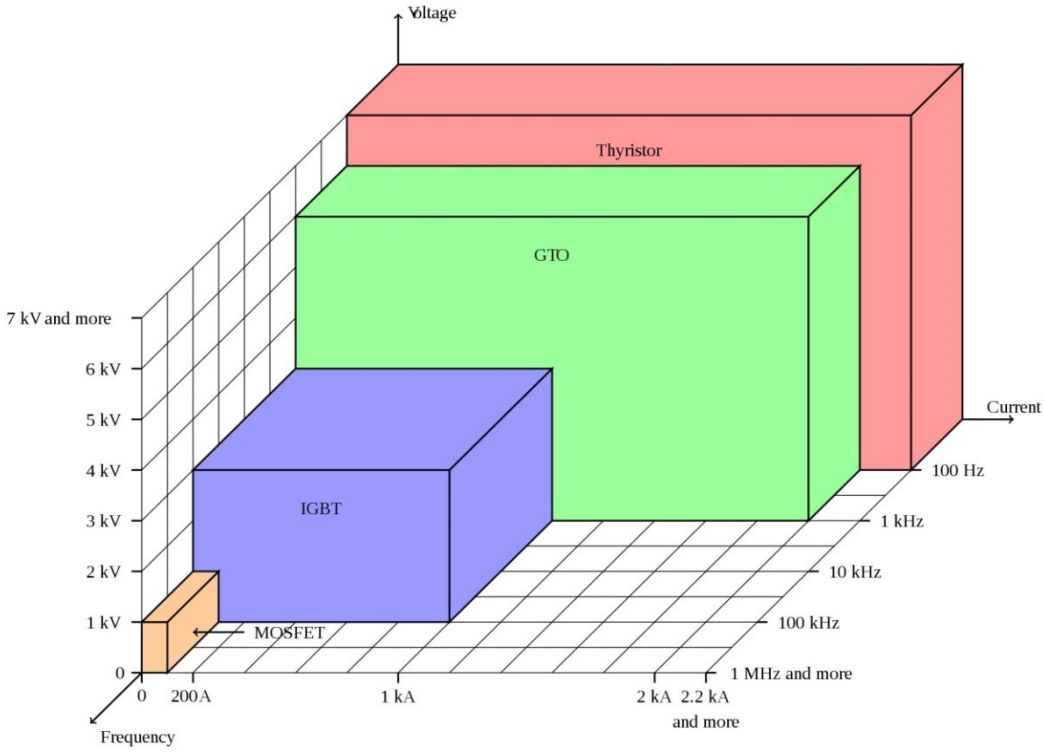

Figure 2.1: Power capability and operating frequency of different semiconductors [2].

2.2 Power electronics background

The following sub-sections give a brief overview of the common types of semiconductors used in pulsed power applications.

2.2.1 MOSFETs

A Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET), is a three terminal unipolar device with a vertically oriented four layer structure of alternate p-type and n-type doping as shown in Figure 2.2 (n-channel MOSFET). MOSFETs are devices that are simple to turn-on and turn-off. They have an insulated gate structure.

The device is turned on by applying a voltage to the gate (typically 15V for an N-channel MOSFET) and turned off by discharging the gate (usually to 0V). The gate structure looks capacitive. Whilst the gate capacitance is small; it takes finite time to charge and discharge. This affects the rate at which the device can be turned on and off. The MOSFET tends to be used in low voltage supplies (50-1000V) as the on-state resistance rises significantly as the blocking voltage requirement increases. In most switched-mode applications this additional loss generally means IGBTs are more efficient at voltages greater than 600 V. If on-state losses are not an issue then the MOSFET displays superior switching speeds to the IGBTs.

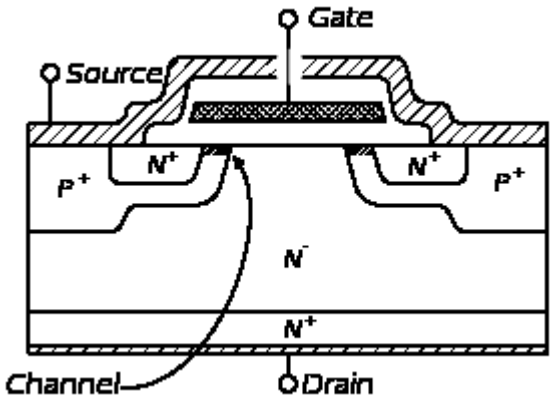

Figure 2.2: Cross section of a MOSFET.

2.2.2 IGBT

Insulated Gate Bipolar Junction Transistors (IGBTs), shown schematically in Figure 2.3, are now manufactured as modules with voltage ratings up to 6.5kV and current ratings to a few thousand Amperes. They display a MOSFET-like gate structure, and are therefore simple to drive on and off (in a similar manner to a MOSFET). The IGBT structure includes a bipolar-junction-transistor (BJT) which provides additional current conduction within the structure. The BJT structure

provides an almost constant voltage drop across the device (~2.4V in a power device). The on-state losses are less dependent on load current unlike in a MOSFET where on-state losses increase with the square of load current. One disadvantage of the IGBT is a current tail where current falls quickly in the device as the MOSFET structure turns off, but the BJT structure still has carriers in the base section that cannot be swept away. These free carriers contribute to a continued flow of current called a "tail" after the MOSFET section turns off. This current tails off in a few tens to hundreds of nanoseconds (the current tail duration depends on the device).

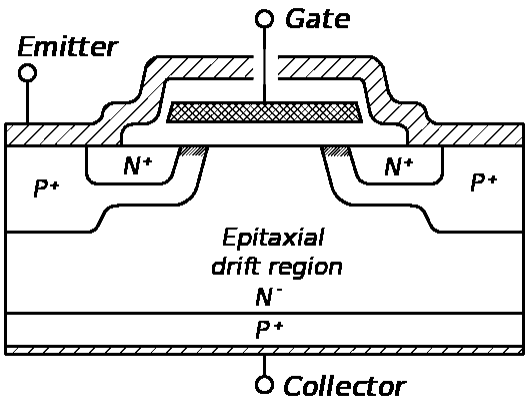

Figure 2.3: Cross section of an IGBT.

2.2.3 Thyristors

A Thyristor is a relatively simple to turn on device, but will turn off only when the conducted current falls to zero (turn off via the gate is possible but slow). Thyristors have voltage ratings up to tens of kV. Current ratings depend on the diameter of the thyristor wafer. A 150mm wafer in a pulsed-power application can conduct 8kA. Gate Turn-Off thyristors (GTOs) are structurally improved Thyristors which have a turn-off capability via the gate. Generally, GTOs are turned-off by

forcing a portion of the load current out through the gate. Somewhere in the region of 20% of conducted current which may be the order of kilo-amps needs to be diverted to force the device off. The commercial availability at high current and high blocking voltage of GTOs and Thyristors make this technology the current choice for pulsed-power applications where switching performance is not a concern.

Other lower power semiconductors used in pulsed power include Semiconductor Opening Switches (SOS) [3], Drift Step Recovery Diodes (DSRD) [4], and Photo Conductive Semiconductor Switches (PCSS) [5].

2.3 Pulsed power system based on solid-state devices

2.3.1 Pulsed power using MOSFETs and IGBTs

Typically, vendors' data sheets for solid state switches provide a starting point for selecting solid-state devices. However, most data sheets do not have sufficient information to determine the performance in a pulsed power application. B.Hickman *et al*. [6] presented a paper on testing MOSFETs and IGBTs to determine the rise time, fall time, and current handling capabilities. The switching evaluation is based on 1000V devices with a pulsed current of at least 25A and a pulse width of 100ns. Power MOSFETs have significantly faster turn-on and turn-off speed than IGBTs. MOSFETs however have lower current and voltage ratings than IGBTs. The experimental results are tabulated in Table 2.1 and the test circuit is shown in Figure 2.4. The author did not detail the gate driver circuit and the gate drive voltage for these tests.

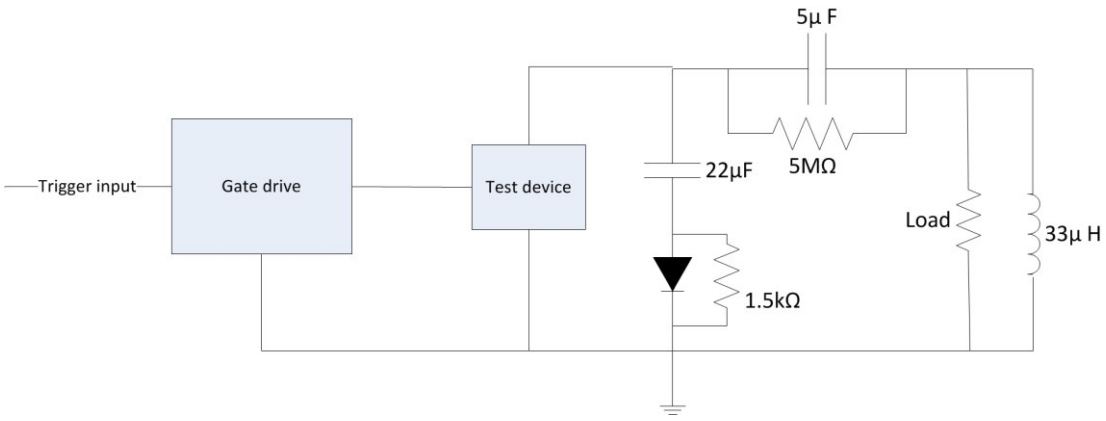

Figure 2.4: Test circuit diagram for the IGBT and MOSFET [6].

Table 2.1: Performance characteristics for the experimented devices [6].

Device	Rated Voltage	Rated Pulsed Current	Peak Measured Current	Turn-On Time	Turn-Off Time	Type
APT1001RBLC	1000V	44A	44A	19ns	13ns	MOSFET
APT1001RBVR	1000V	44A	47A	20ns	13ns	MOSFET
APT10086BLC	1000V	52A	56A	25ns	12ns	MOSFET
APT10050LVR	1000V	84A	76A	34ns	13ns	MOSFET
APT10053LNR	1000V	80A	85A	43ns	43ns	MOSFET
APT10040LVR	1000V	100A	95A	44ns	40ns	MOSFET
APT1201R5BVR	1200V	40A	40A	19ns	13ns	MOSFET
APT12080LVR	1200V	64A	65A	26ns	12ns	MOSFET
HGTG27N120BN	1200V	216A	56A	80ns	20ns	IGBT
IXBH40N160	1600V	40A	37A	60ns	20ns	IGBT
*IXGH45N120	1200V	180A	361A	226ns	681ns	IGBT
*IXSH35N120A	1200V	140A	172A	234ns	52ns	IGBT
*APT50GF120B2R	1200V	160A	167A	415ns	90ns	IGBT
*APT20GF120BDR	1200V	64A	60A	132ns	23ns	IGBT
*IXSH35N140A	1400V	140A	173A	217ns	257ns	IGBT
*APT15GF170BDR	1700V	50A	48A	121ns	19ns	IGBT
*IXBH42N170	1700V	180A	169A	133ns	61ns	IGBT

* Tested at 500ns or greater pulse widths to obtain peak current.

Alton Chaney *et al*. [7] presented a paper on the development of a 400V, 75ns pulse generator by employing an IXYS DE275-501N16A RF MOSFET with 500V, 16A rating and 6ns rise time. This pulse generator was used to drive a 50Ω resistive load. The overall system is shown in Figure 2.5. Its three stage design consists of an integrated variable frequency and variable duration pulse-width signal source, an inverter/driver stage and a power buffer consisting of a passively loaded single-ended

MOSFET. The experimental results of this device for the rise time (turn-on) and fall time (turn-off) are shown in Figures 2.6 & 2.7 respectively.

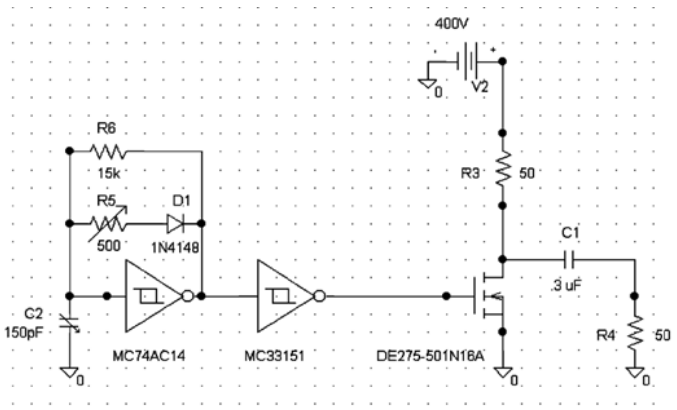

Figure 2.5: The overall pulse generating system using a MOSFET [7].

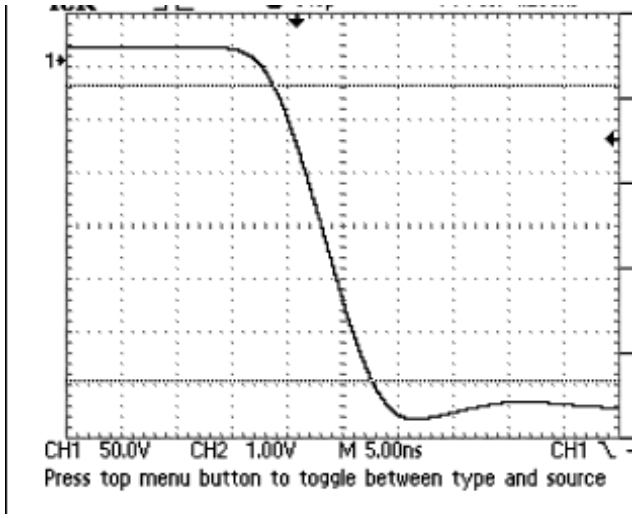

Figure 2.6: Drain-source voltage during turn-on transient for 400V with 50Ω load [7].

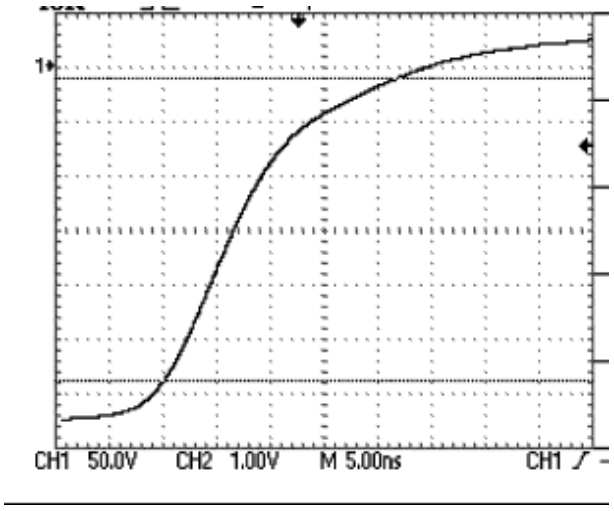

Figure 2.7: Drain-source voltage during turn-off transient for 350V with 50Ω load [7].

F.Wakeman *et al*., [8][9][10] presented papers on the application of pressure contact IGBTs [11] in pulse power systems, with some initial experimental results under short-pulse, high *di/dt* conditions as shown in Figure 2.8. The construction of these devices is totally free from wire and solder-bonds, which all but eliminate the problems of mechanical fatigue associated with conventional modules. Internal stray inductance in both the gate connections and emitter connections is vastly reduced when compared to conventional modules leading to improved ruggedness and short circuit behaviour. Pressure contacts IGBTs are therefore suitable for series connection in medium to high power applications. In the circuit, C1>>C2 and LI>>L3, and C2 and L3 are adjusted to obtain the required peak current and pulse duration. D3 is the free-wheeling diode. Four different experiments for an 1800V/400A device were carried out. From the experimental results, it was shown that peak currents greater than 3 times the collector-emitter current rating are possible and that the IGBT can be safely turned off from the gate with a peak current

more than twice the rated collector-emitter current. Employing the pressure contact IGBT, higher *di/dt* can be achieved.

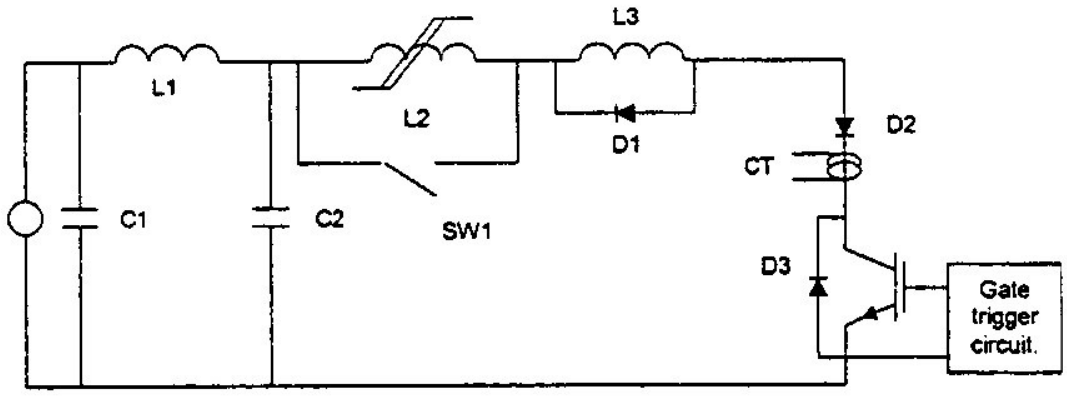

Figure 2.8: Test circuit diagram for IGBT [8].

In [12] S-R Jang did a comparative study of MOSFETs and IGBTs for high repetitive pulsed power modulators. For a 10kV system, the author obtained pulse rise times of 40 ns and 60 ns respectively using 18 MOSFETs and 12 IGBTs. It is concluded that due to the high switching loss and low conduction loss of the IGBT in comparison to MOSFETs, IGBTs are suitable for higher pulse width and high current applications which require lower repetition rates and slower switching speeds. Conversely, where high frequency switching is required, MOSFETs will be the favoured component choice. It is also shown that IGBTs can operate at arc currents up to five times the rated current.

2.3.2 Pulsed power system using SI-thyristors

R. Hironaka, *et al*., [13] presented a paper on a pulsed power system using one 5500V Static Induction Thyristor (SI-Thyristor) and a Blumlein line for pulse formation. A turn-on time of several tens of nanoseconds and a maximum output voltage rise rate of 96kV/μs was obtained. W Jiang [14] presented a paper on the

developments of SI Thyristor technology in repetitive pulsed power applications. A recently developed 3kV SIThy device (by NGK Insulators Ltd) has been tested with initial focus on the issue of switching speeds in comparison with MOSFET devices. The device is tested at 1MHz and 2kV. Figure 2.9 shows the test circuit, with rise and fall times of approximately 40ns and 100ns respectively.

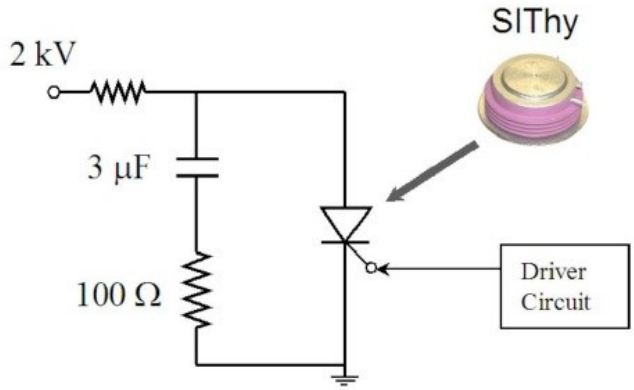

Figure 2.9: Test circuit for SI Thyristor [14].

The results shown in Figure 2.10 were obtained by R.Hironaka [14].

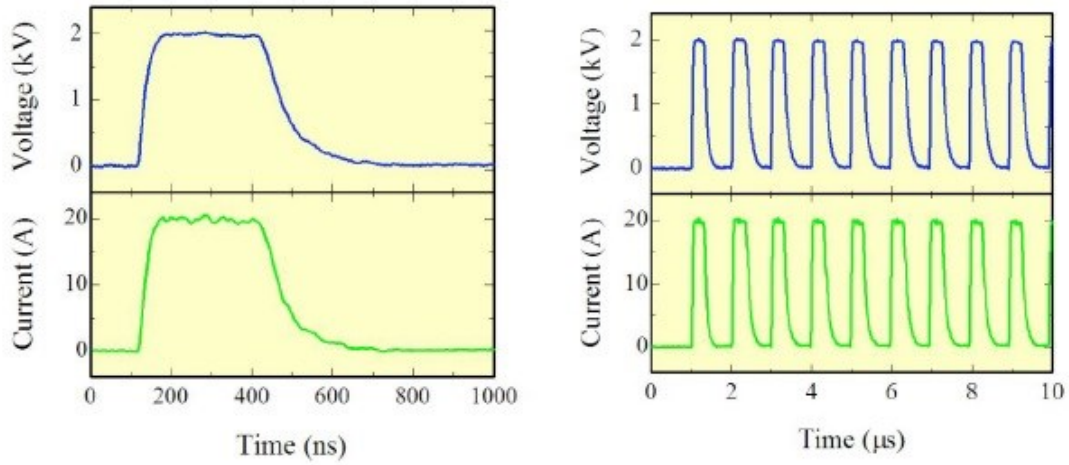

Figure 2.10: Output voltage and current waveforms [14].

F.J. Wakeman and M. Baker [15] presented a paper on the implementation of Gate-Turn-Off Thyristors (GTO) as high voltage turn-on switches for pulsed power application. Experiments on a symmetrical blocking 4.5kV, 66mm diameter silicon device showed that, the GTO has high peak current and *di/dt* capability [15]. J.Bonthond, *et al.* [16] presented a paper about high current, high *di/dt* switching with an optimised GTO Thyristor (Fast High current Thyristor, FHCT), which allows switching of tens of kA with a high rate of current rise from blocking voltages of several kilovolts. The author of [16] experimented on a symmetrical 4.5kV, 66mm un-shorted anode FHCT from Westcode with light gold doping which shows excellent turn-on characteristics. A *di/dt* of 20kA/μs for a half-sine wave current pulse of 32kA was achieved [16]. Table 2.2 summarises the test results.

Table 2.2: FHCT data measured in test circuit [16].

Test voltage	4.4	kV
Gate current rate of rise	200	A/μs
Gate current amplitude	240	A
Gate controlled turn-on delay time t_{gd} ($0.1 \bullet I_{gate}$ to $0.9 \bullet V_{anode}$)	550	ns
Gate controlled turn-on time t_{gt} ($0.1 \bullet I_{gate}$ to $0.1 \bullet V_{anode}$)	1.5	μs
Maximum di/dt	16	kA/μs
Maximum current	32	kA
Turn-on losses	4	Joules
Conduction losses (1-6 μs)	4	Joules

2.3.3 Discussion

From the previous literature survey, the commonly used semiconductors can be classified into different categories. Thyristors deliver very high power at wider pulse widths with slow rise and fall times. Their variants (SI thyristors and GTO thyristors) are more capable devices with significantly improved switching speeds and which can operate at tens of kilohertz. However, their switching times can be in

the range of several hundreds of nanoseconds, depending on the current rating of the device. They also have larger associated turn on delays. IGBTs are more suitable in medium power applications, and are capable of managing several kilovolts and hundreds of amperes. Generally, IGBTs have switching times greater than 20ns which increases as the current rating of the device increases. MOSFETs are suitable for high speed applications requiring switching speeds of less than 10ns, or high frequency applications which can range from several hundred kilohertz to megahertz. They however, have the lowest voltage and current ratings of all devices types. The capability to deliver near rectangular shape pulses, high repetition rate, and lower maintenance costs make the MOSFET a strong contender for pulsed power applications.

Due to the relatively higher switching delays and turn-on and turn-off times, IGBTs and Thyristors are not inherently suitable for operating in short pulse mode with widths less than 100ns. They are therefore suitable for wider pulse width applications or when used in conjunction with Pulse Forming Lines and magnetic pulse compression circuits. Therefore, they do not present a reasonable advancement to the existing IVA technology using gas trigger switches. It is in this regime where MOSFET technology leads the industry, with the capability to provide fast pulse edge transitions and short pulse widths. Consequently, the need for pulse compression circuits is eliminated, thereby showing potential to significantly reduce system size. For this reason, MOSFETs have been chosen as the preferred switching device type in this research project.

2.4 Pulsed power technology

In section 2.3, it was established that the MOSFET is the most suitable high speed switching technology for short pulse width generation and a potential new candidate for flash radiography application that is suitable to AWE. MOSFET technology can be used in different topologies to form a pulsed power system. In [17], S. Roche presented a paper which reviews solid-state pulsed power systems highlighting advantages and disadvantages of each topology. Further to this, three topologies, namely solid-state Marx, Solid-state IVA, and Series-switch topology, were further investigated. In the following subsections, a literature review for these topologies is presented.

2.4.1 Solid-state Marx

The operating principle of the Marx generator was discussed in Chapter 1. Solid state switches replace the spark gap switches and provide a higher switching speed and controllable on/off characteristics for the Marx system. Figure 2.11 shows the schematic diagram of a typical solid-state Marx circuit.

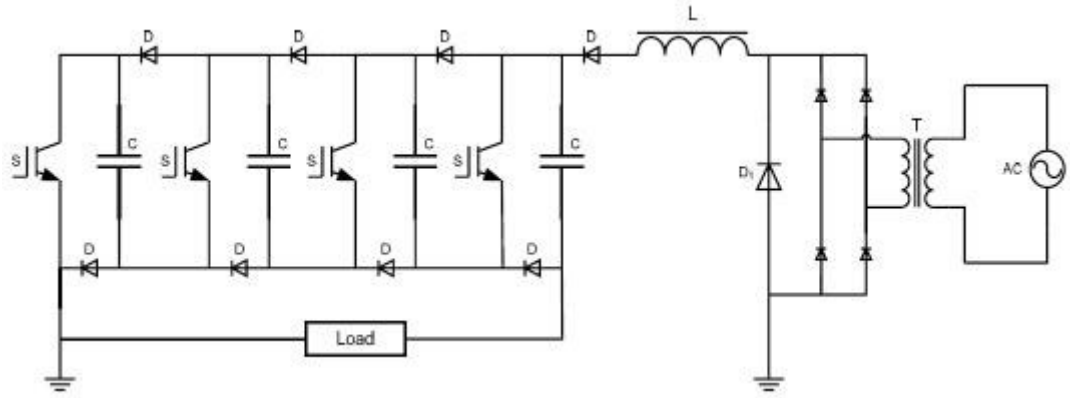

Figure 2.11: Schematic of a solid state Marx circuit [23].

Several papers have been presented on solid-state Marx generators [18-22], with most based on IGBTs. In [23] a 20 stage, 60 kV Marx generator uses IGBT switches rated at 3kV. The operating pulse widths range from 20μs to 100μs at a repetition rate which is variable between 50Hz and 500Hz. The rise time was measured to be 800ns. A MOSFET based pulse adder circuit is presented in [24]. The authors demonstrated a modified Marx generator topology with a resonant capacitor charging technique and an isolated multi-output gate drive transformer technique for synchronous triggering of the MOSFETs in the Marx circuit. Output voltages of 20kV at pulse widths of 3μs were obtained at a 20kHz repetition rate. Rise times of 150ns were obtained. The main disadvantage with a solid-state Marx generator is that the on-state losses are higher since the total on-state resistance increases with the number of MOSFET switching stages. The gate drive complexity is higher due to the need for isolating the MOSFETs operating at floating potentials. The total inductance of the stack increases with each stage and therefore, high speed switching becomes difficult. This is demonstrated in [25] where a MOSFET based Marx generator is presented. With a four stage Marx setup, rise times of 10ns to 15ns were demonstrated [25]. However, with a 25 stage Marx setup, the rise times increased to approximately 70ns.

2.4.2 Series switch topology

Series connecting a string of MOSFET or IGBT devices is possible. Two 3.3kV IGBTs connected in series should theoretically be able to support close to 6.6kV. However, it is imperative that the devices equally share the voltage. There has been much research effort expended on ensuring voltage sharing, particularly during the transient periods when turning on or off. The unequal voltage sharing shown

must be corrected using either passive or active means [26-30]. If not, as devices are pushed close to their operational limits, failure will result as the breakdown voltage of the device supporting the majority of the voltage will be exceeded. W.Jiang, *et al*. [31] presented a paper on stacked MOSFET switches. Each cell has 6 parallel-connected 900V, 8A MOSFETs. A string of 8 series-connected cells make up the modular system. The MOSFET is controlled by an optically coupled signal. The voltage and current ratings of the stacked switch are 5kV and 75A respectively. The rise time of the pulse with a width of 240ns is 33ns and the fall time 43ns. In [32], a 120kV, 70A switching system is presented which makes use of 100 series connected MOSFETs. RC snubbers are used for voltage balancing. Switching times are approximately 25ns.

Due to the requirement for voltage balancing between the series connected devices, active or passive voltage balancing techniques significantly increase the switching times of the semiconductors.

2.4.3 Solid-state IVA/ LTD

The principles of the IVA and LTD were discussed in Chapter 1. The salient feature is the ability to use low voltage and high current sources to add inductively and output a high power. Also, the low inductance arrangement using a 1:1 transformer ratio results in faster rise and fall times which are favourable for pulsed power systems. Solid-state LTDs have evolved from higher power LTD technologies [33-36] which deliver pulsed energy ranging from several megawatts to gigawatts. The switching technology used by these systems is pressurised air/gas closing switches which are rated at several hundred kilovolts. The high power output of an

LTD relies mainly upon the number of parallel connected capacitors and switches. MOSFETs with their high speed switching capability and ease of paralleling make them an ideal semiconductor to be used in an LTD configuration. One of the earliest MOSFET based IVA system was used by Lawrence Livermore National Laboratory, involving a solid state kicker pulser [37]. Figure 2.12 shows the schematic diagram of the Inductive Voltage Adder. Each adder stage board consists of 24 parallel connected MOSFETs and their corresponding gate driver circuit and capacitor bank, which connects to the primary winding of the transformer through sliding contacts. Output voltages of 20kV across a 50Ω load were obtained with pulse widths of 120ns and rise and fall times of approximately 12ns under single shot and burst mode operation.

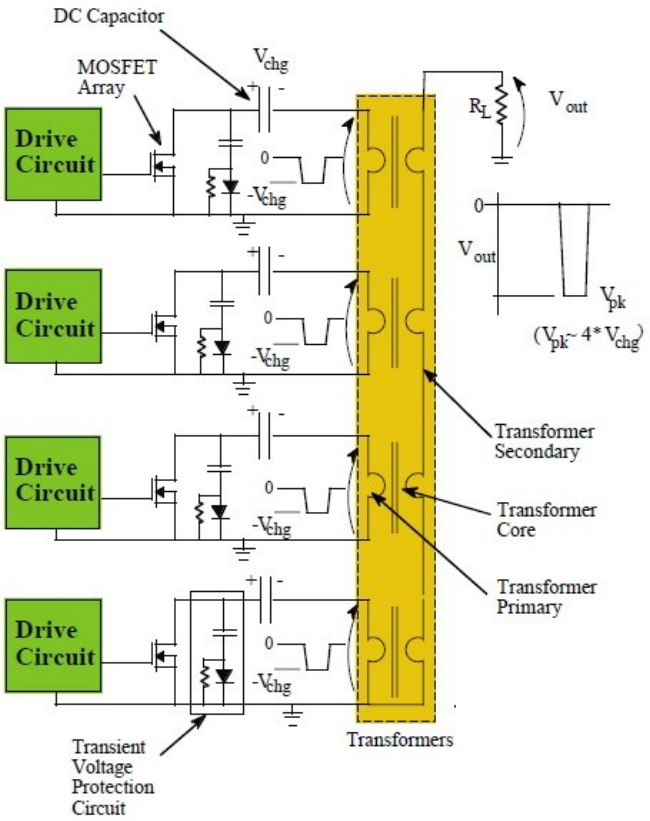

Figure 2.12: Schematic of the Inductive adder circuit [37].

In [38], W. Jiang presented a compact LTD system using ten adder stages of power MOSFETs. Each stage has 35 parallel connected MOSFETs with corresponding gate drivers and capacitor bank. Peak output voltages and currents of 9kV and 175A across a 50Ω load with flat top pulse width of approximately 42ns were obtained. Rise and fall times were reported to be 17ns and 22ns respectively.

2.5 Summary

From the previous discussion on three solid-state pulse generating technologies, it can be inferred that the Marx generator and series switching topologies are advantageous when the required peak current is lower and when turn on and turn off times are not a concern. Higher output voltages are readily obtained with the added complexity of floating gate driver and voltage balancing techniques. LTD technology uses several MOSFETs in parallel based around a transformer structure. This enables the distribution of the total current around the core. Higher output current per stack can thus be obtained along with high switching speeds due to a low inductance arrangement. Theoretically, the number of stacks that can be added to increase the output voltage is infinite. Therefore, this technology offers the best of high voltage and high current pulse generation capability. A MOSFET based LTD system is therefore the chosen topology for the approach in this thesis.

There is scope for improvement in the area of MOSFET based LTD systems to make them suitable for higher power applications. This requires research into improving technology from the fundamental level, which includes gate driver, pulse transformer, module, and system design. Chapter 3 focuses on the literature and design of a MOSFET gate driver circuit.

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Chapter 3

High-speed current-source MOSFET gate driver

3.1 Introduction

Over the last two decades, ultra-fast repetitive switching, compactness and portability have increasingly become attributes of pulsed power systems in both defence and non-defence sectors. Despite rating limits, solid-state switches are finding increasing applications in compact pulsed power systems. Principal solid-state pulsed power switches include thyristors, GTO thyristors, IGBTs and MOSFETs. These switches have the advantage that, when operated within their specifications, they will have a longer lifetime and have reduced maintenance than conventional gas switches. When high voltage, high current and fast rise times are needed, however, these switches have some limitations not yet overcome for practical applications. MOSFETs and IGBTs specifically, have drawn attention in high-speed or high-frequency applications. With relatively compact sizes and high repetition rate capability, they have a potential to overcome many of the challenges in pulsed power systems.

The proposed project is concerned with the application of MOSFETs in short-pulse, high-power pulse generation which are the desired characteristics in flash radiography. For high-power operation, there are two main problems with this

technology. The MOSFETs that are capable of ultra-fast switching come with a compromised lower power rating due to smaller die sizes and smaller input capacitances. This means that a larger array of these devices have to be connected in series/parallel combinations in order to develop a high power system. This adds to system cost and complexity and therefore is deemed impractical. Alternatively, MOSFETs with higher power ratings have a significantly larger die structure and therefore, higher input capacitance. Therefore, they exhibit slower switching and are not considered for short pulse width applications.

The key enabling technology behind the ultrafast operation of MOSFETs is the gate driver circuit. Many gate drive designs have been proposed in the literature and are commercially available. Some gate drivers facilitate low cost switching solution for devices, some offer improved switching speeds, and some with the ability to reduce the losses associated with repetitive switching [1-6]. Many of the commercially available high-speed drivers are rated for devices with an input capacitance of less than 2nF. For example, MOSFET driver EL7158 has a peak current drive of 12A and the specified rise and fall times are 12ns and 12.2ns respectively for a 2nF load capacitance. A more powerful driver DEIC515 has a peak drive current of 15A with specified rise and fall times of 4.1ns and 3.9ns respectively for a 2nF load capacitance. It must be highlighted that modern high-performance drivers also rely on the layout and proximity of the driver to the MOSFETs to achieve the specified rise and fall times. This is one of the disadvantages of voltage source drivers, where the loop inductance has a significant effect on switching performance. Higher power devices generally have an input capacitance greater than 5nF. For example, MOSFET IRFP4668 has a rating of 200V and 520A (pulse), with

an input capacitance of 10.7nF. Also, large devices come with inherently higher package inductances and input gate resistances. Therefore, generic drivers are not well suited to driving high-power MOSFETs at ultra-fast speeds. The fastest commercially available high-power MOSFET gate driver is the IXD630 with a peak current of 30A and specified rise and fall times of 35ns for a 5.6nF load capacitance.

There is a need for the design of a MOSFET gate driver which would be capable of driving high-capacitance MOSFETs and MOSFET arrays at ultra-fast speeds. This would enable high-power devices to switch at higher speeds. A high power density pulsed power system using MOSFETs can then be created using fewer devices for short pulse generation.

This chapter proposes a new current source gate driver scheme for ground referenced MOSFETs. The objective of the proposed gate driver is to enable ultra-fast switching of MOSFETs with higher input gate capacitances. Furthermore, the driver can synchronously drive multiple MOSFETs in parallel, without compromising the switching performance of each individual device. The driver is designed with the aim to maintain the simplicity, stability and compactness required for the development of a compact solid-state high power density pulsed power system.

In section 3.2, the proposed gate driver circuit and its operation are presented. A detailed analysis of the gate driver switching transients is presented in section 3.3. Section 3.4 discusses the effect of Miller capacitance on gate driver switching. The pulse generator logic circuit used to generate the gate trigger pulses is presented in section 3.5. Section 3.6 discusses the printed circuit board layout of the gate driver

which is critical to its performance. Experimental results are presented in section 3.7 followed by conclusions in section 3.8.

3.2 Proposed current source gate driver

The following sub-sections present the gate driver circuit and describe its operation.

3.2.1 Proposed circuit

The proposed current source gate driver is illustrated in Figure 3.1. It consists of two driver stage MOSFETs, S_1 and S_2 (n-channel), inductance L, an anti-parallel diode D_2 and resistor R_1. M_1 is the power MOSFET under test. The two driver stage MOSFETs are controlled and the diode D_1 is used to allow excess inductor current to be discharged via resistor R_1.

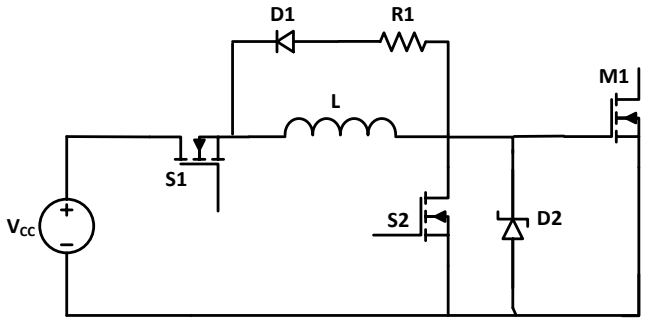


Figure 3.1: Simplified schematic of the gate driver circuit.

The gate waveforms of the two driver stage MOSFETs, S_1 and S_2, along with the inductor current, gate current and power MOSFET M_1 gate-to-source voltage are illustrated in Figure 3.2.

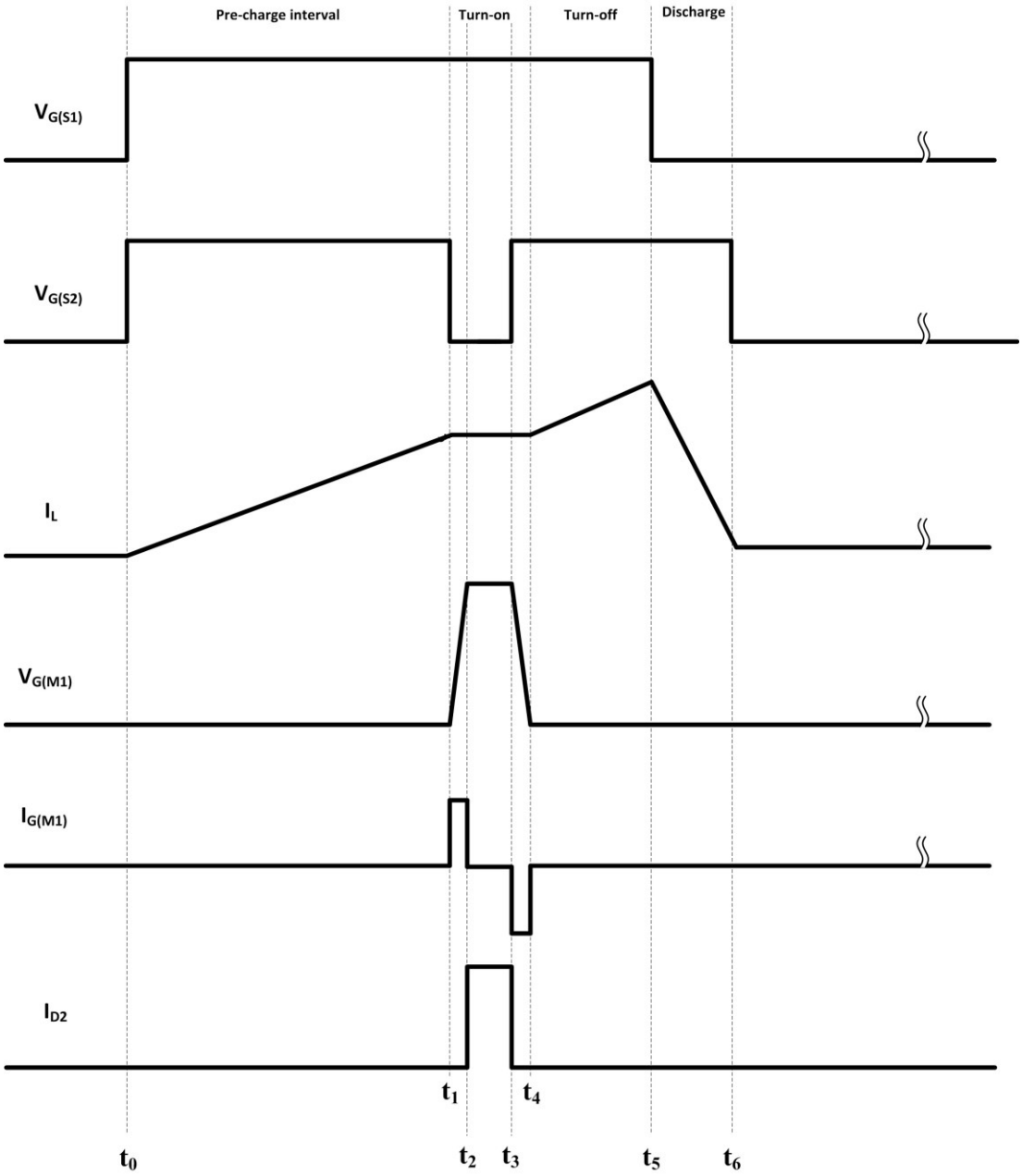


Figure 3.2: Switching waveforms for the proposed gate driver circuit.

3.2.2 Detailed operation at turn-on

It is assumed that the MOSFET M_1 is in the off state and the inductor current is zero before time t_0. The current paths during turn-on are illustrated in Figure 3.3.

For simplicity, the gate of power MOSFET M_1 is replaced with an equivalent capacitance C_G.

t_0-t_1: At t_0, switches S_1 and S_2 are turned on. The current begins to ramp up in the inductor. The current path during this interval is S_1-L-S_2. Since S_2 is in the on state, C_G is short circuited to ground via S_2 as shown in Figure 3.3 (a). The charging interval ends at time t_1 and is pre-determined by the user.

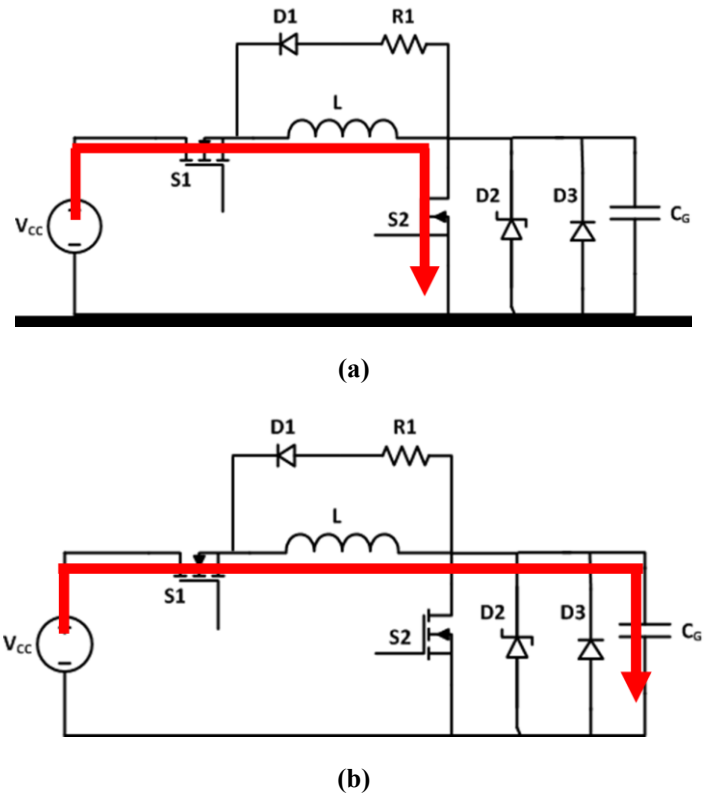


Figure 3.3: Current path during turn-on interval (a) t_0-t_1 (b) t_1-t_3.

t_1-t_3: At t_1, S_2 is turned off, forcing the inductor current to be diverted and begin to charge the power MOSFET gate as shown in Figure 3.3(b). The current path during this sequence is S_1-L-C_G. The gate voltage rises with a high dv/dt. At t_2 the power MOSFET gate is clamped at a desired safe gate voltage V_G. The clamping is undertaken by a Transient Voltage Suppressor (TVS) diode D_2. The current I_Z is

diverted through this diode while maintaining a fixed voltage at the power MOSFET gate. The TVS diode is in conduction between t_2 and t_3 until the gate voltage drops below the breakdown voltage of the diode. The turn-on interval ends at time t_4. The length of the interval is adjusted by the user to provide the desired pulse width.

3.2.3 *Detailed operation at turn-off*

At the beginning of this interval, the power MOSFET gate is charged to a gate voltage V_G and the inductor L is charged to a current I_L. The current paths during turn-off are illustrated in Figure 3.4.

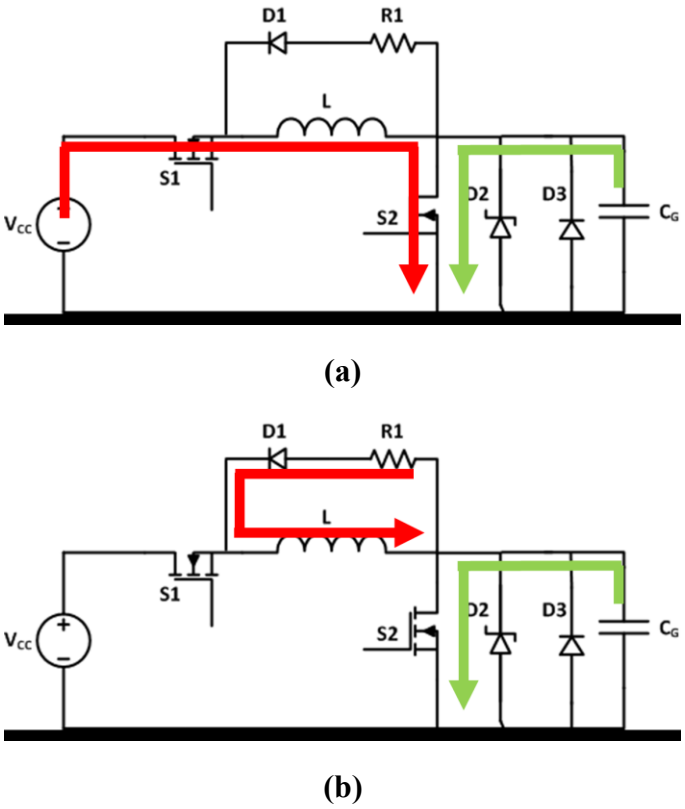


Figure 3.4: Current path during turn-off interval (a) t_3-t_5 (b) t_5-t_6.

t_3-t_5: At t_4, S_2 is turned on again. This enables the inductor current to be diverted away from the gate of the power MOSFET and initiates the turn-off process. The energy stored in the power MOSFET gate is discharged via the low impedance path

created by S_2 as shown in Figure 3.4(a). Simultaneously, the path created by S_1-L-S_2 results in further increase in the inductor current, which is not required. The interval ends at t_5. The voltage rating of the MOSFET S1 is influenced by the current flowing through the inductor and the value of discharge resistor.

$t_5 - t_6$: At t_5, S_1 is turned off, which isolates the inductor from the power supply and prevents further charging of the inductor. Remaining energy in the inductor is freewheeled and dissipated via resistor R_1 as illustrated in Figure 3.4(b).

3.3 Switching transient analysis

In high speed and short pulse width applications, parasitic inductances and capacitances dominate. These can significantly impede the slew rate as well as increase the output delay of the circuit. Thus, appropriate knowledge and awareness of the parasitic influences in the circuit will aid in gate driver performance optimisation.

The following sub-sections present a mathematical analysis of the switching transients associated with the proposed gate driver circuit. The analysis is split into two parts: a basic analysis that establishes the generic transient response of the gate driver, and a more detailed analysis in section 3.4 that considers the effects of parasitic Miller capacitances which influence MOSFET switching. Following the basic analysis, is discussion related to the design which identifies the key parameters and problems. This is followed by a proposed modification to the design.

3.3.1 *Pre-charge cycle*

The pre-charge cycle is between the time intervals t_0 and t_1. The current path is S_1-L-S_2 as stated in section 3.2.2. For analysis, Figure 3.1 can be simplified into the equivalent circuit shown in Figure 3.5. A voltage driven RL circuit is used to represent this condition where V_{CC} is the driver supply voltage, R_{ON} is the summation of the resistances around the current path which, in this case, is the on-state resistance of the driver MOSFETs R_{S1} and R_{S2}, and L is the loop stray inductance.

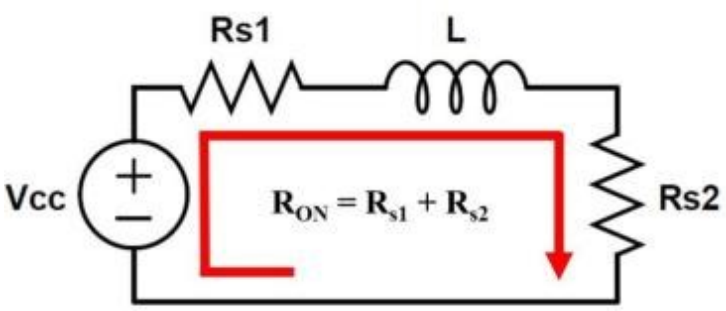


Figure 3.5: Gate driver equivalent circuit during the pre-charge interval.

During this time interval, current builds up in the inductor. The charging current I_L in the inductor L during the time interval t is:

$$I_L(t) = \frac{V_{CC}}{R_{ON}}(1 - e^{-\frac{R_{ON}}{L}t}) \qquad (3.1)$$

3.3.2 *Turn-on transient*

A basic MOSFET analysis can be performed by assuming the MOSFET gate capacitances as a single input capacitance. The turn-on of the power MOSFET is initiated at t_1 and occurs during the time interval t_1-t_4. With the inductor pre-charged to a current I_L, S_2 is turned off at t_1. Figure 3.6 shows the equivalent circuit during this time interval. A voltage driven RLC circuit is used to represent this condition,

where V_{CC} is the driver supply voltage, R_{IN} is the total input resistance in the gate path, L_L is the sum of the external inductance L and the stray loop inductance L_S of the path, and C_G is the total input gate capacitance of the power MOSFET M_1. This capacitance corresponds to the data sheet value of C_{ISS} (which is assumed constant, i.e. independent of voltage).

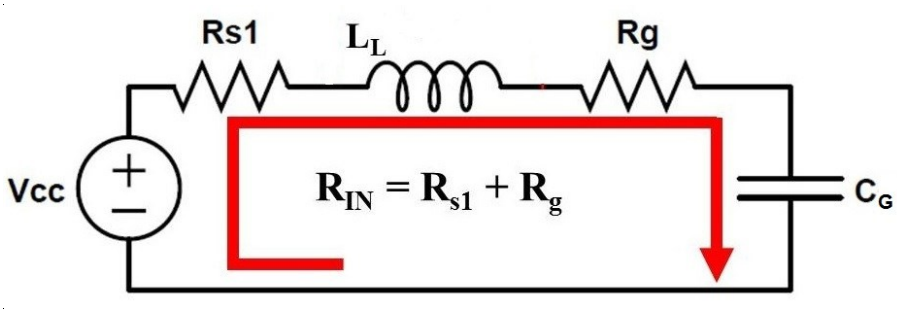


Figure 3.6: Gate driver equivalent circuit during the turn-on transient.

RLC circuits exhibit three types of dynamics, namely:

$\alpha < \omega_0$ => Under-damped dynamics;

$\alpha = \omega_0$ => Critically-damped dynamics;

$\alpha > \omega_0$ => Over-damped dynamics.

where

$$\alpha = \frac{R}{2L} \quad \text{(damping co-efficient)} \tag{3.2}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad \text{(resonant frequency)} \tag{3.3}$$

$$\omega_d = \sqrt{\alpha^2 - \omega_o^2} \quad \text{(ringing frequency)} \tag{3.4}$$

In a low impedance layout with no external resistance, the internal gate resistance of the MOSFET and the on-state resistance of S_2 are the main constituents, the values of which are very low. Under such conditions the circuit exhibits under-damped dynamics as $\alpha << \omega_o$. Using Euler's relation and a second order differential solution for a driven *RLC* circuit [7], the voltage on the gate capacitor V_C can be expressed as

$$V_C(t) = V_{IN} + A_1 e^{-\alpha t} \cos \omega_d t + A_2 e^{-\alpha t} \sin \omega_d t \tag{3.5}$$

where A_1 and A_2 are constants, dependent on the initial circuit conditions. The gate current $I_G(t) = I_L(t)$, can be calculated as:

$$I_L(t) = C_G \frac{dV}{dt} \tag{3.6}$$

Substituting equation (3.5) into (3.6)

$$I_L(t) = (\alpha C_G A_1 - \omega_d C_G A_2) e^{-\alpha t} \cos \omega_d t + (\omega_d C_G A_1 + \alpha C_G A_2) e^{-\alpha t} \sin \omega_d t \tag{3.7}$$

With known gate driver circuit initial conditions, $V_C(0) = 0$ and $I_L(0) = I_0$, where I_0 is the current in the inductor

$$V_C(0) = V_{in} + A_1 \tag{3.8}$$

and the current can be expressed as

$$I_L(0) = \alpha C_G A_1 - \omega_d C_G A_2 \tag{3.9}$$

Equating (3.8) and (3.9)

$$A_1 = V_C(0) - V_{in} \tag{3.10}$$

$$A_2 = \frac{-I_L(0) - C_G \alpha V_{in}}{C_G \omega_d} \tag{3.11}$$

Substituting (3.10) and (3.11) into the original equation (3.5), the peak capacitor voltage $V_C(t)$ can be expressed as

$$V_C(t) = V_{IN} + (V_C(0) - V_{IN}) e^{-\alpha t} \cos(\omega_d t) + \frac{-(I_L(0) + C_G \alpha V_{in})}{C_G \omega_d} e^{-\alpha t} \sin(\omega_d t) \tag{3.12}$$

Figure 3.7 shows the results of the simulation based on the equations with the effect of varying inductor current on gate capacitor voltage V_C. As expected, the rise time of V_C decreases as I_L increases.

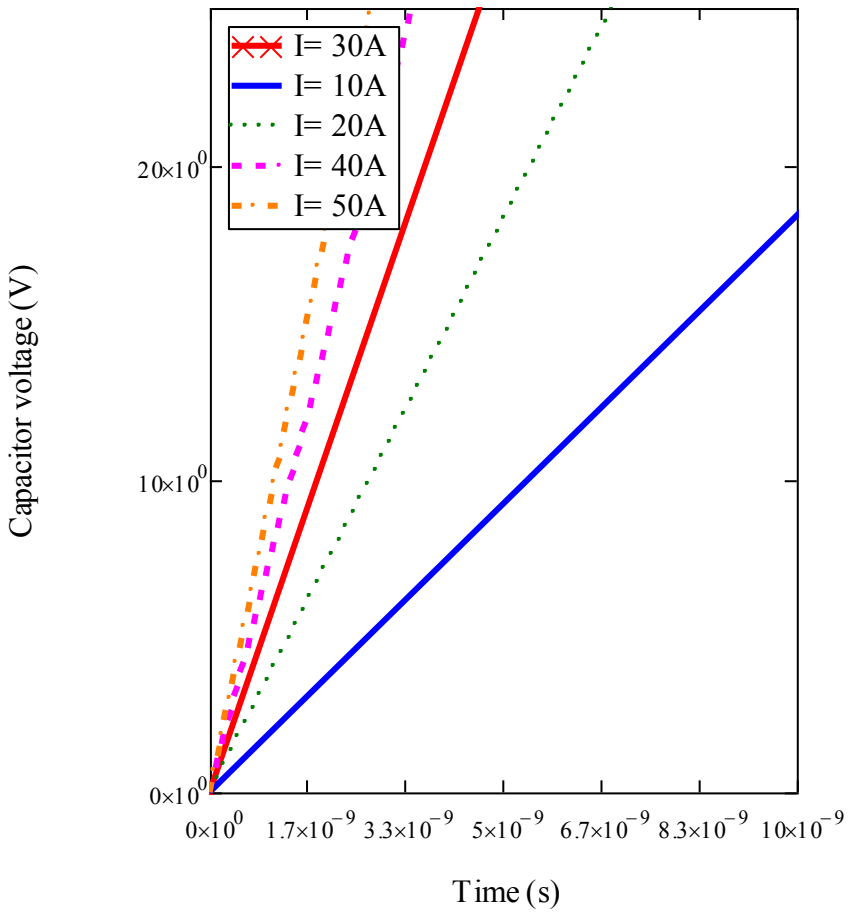


Figure 3.7: Effect of initial inductor current I_L on gate capacitor voltage.

3.3.3 *Turn-off transient*

Power MOSFET turn-off is initiated at time t_4, where the gate capacitor voltage is at the desired gate voltage V_G and the inductor current is maintained at I_L. Figure 3.8 shows the equivalent circuit during turn-off.

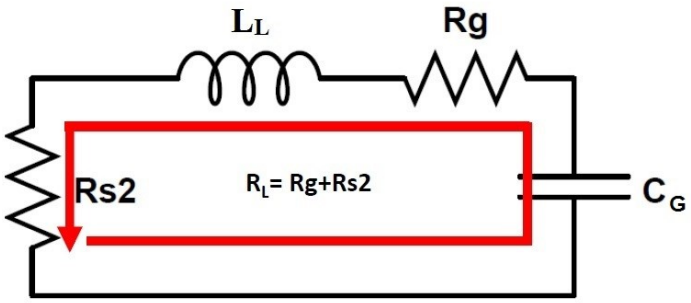


Figure 3.8: Equivalent circuit during MOSFET turn-off.

An undriven *RLC* circuit can be used to represent the turn-off process. The parameters are R_L which represents the sum of the internal gate resistance and the resistances around the path, which in this instance would be the S_2 on-state resistance. L_L is the total stray loop inductance around the path C_G-S_2 and C_G is the input gate capacitance of the device under test.

The capacitor voltage $V_C(t)$ in an undriven *RLC* circuit can be characterised by

$$V_C(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{3.13}$$

where A_1 and A_2 are constants dependent on the circuit initial conditions, s_1 and s_2 and the two roots of the characteristic equation of a second order circuit

$$s_1, s_2 = -\alpha \pm \sqrt{\alpha^2 - \omega_o^2} \tag{3.14}$$

Substituting (3.13) into (3.6), the inductor current can be expressed as

$$I_L(t) = -C_G\left[s_1 A_1 e^{s_1 t} + s_2 A_2 e^{s_2 t}\right] \tag{3.15}$$

During the off interval, the initial voltage on the gate capacitor $V_C(t) = V_G$ and the loop stray inductor current $I_L(0) = 0$. Therefore

$$V_C(0) = A_1 + A_2 \tag{3.16}$$

$$I_L(0) = -C_G(s_1 A_1 + s_1 A_2) \tag{3.17}$$

Equating (3.16) and (3.17)

$$A_1 = \frac{C_G s_2 V_C(0) + I_L(0)}{C_G(s_2 - s_1)} \tag{3.18}$$

$$A_2 = \frac{C_G s_1 V_C(0) + I_L(0)}{C_G(s_1 - s_2)} \tag{3.19}$$

Similar to turn-on, the turn-off equivalent circuit demonstrates under-damped dynamics and has complex roots with a damping co-efficient and ringing frequency which can be calculated using equations (3.2) to (3.4). The voltage on the gate capacitor $V_{G(M1)}$ during period t_3-t_4 can thus be expressed as

$$V_{G(M1)}(t) = V_{G(M1)}(0)e^{-\alpha t}\cos\omega_d t + \frac{\alpha C_G V_{G(M1)}(0) - I_L(0)}{C_G \omega_d} e^{-\alpha t}\sin\omega_d t \tag{3.20}$$

and the current can be expressed as

$$I_L(t) = I_L(0)e^{-\alpha t}\cos\omega_d t + \frac{V_{G(M1)}(0) - \alpha L_L I_L(0)}{L_L \omega_d} e^{-\alpha t}\sin\omega_d t \tag{3.21}$$

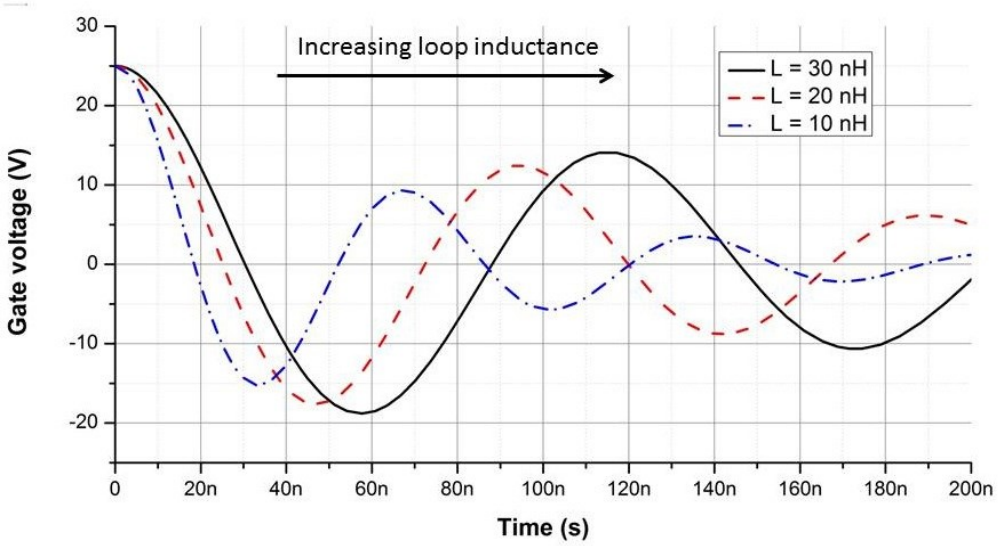


Figure 3.9: Effect of stray loop inductance on turn-off response.

Figure 3.9 shows the mathematical simulation result of the effect of increasing loop inductance on the turn-off gate capacitor voltage V_C. The ringing frequency decreases as the loop inductance increases. This results in an increase in the time taken for the capacitor voltage to fall to zero.

3.3.4 Discussion

The following points can be extracted from the basic analysis of the gate driver circuit:

1) A large peak gate current results in a fast gate voltage transition.
2) Higher gate current can be used to drive higher capacitive loads at similar speeds to devices with smaller gate capacitance.
3) The parasitic inductance L_S in the gate path has negligible effect on the turn-on performance. However, the peak output gate voltage and gate current vary due to the combined effect of parasitic inductance L_S along

with other parameters which include gate resistance R_G, gate capacitance C_G and external inductance L.

4) The parasitic inductance L_S has a significant effect on circuit turn-off delay. This is more prominent in devices with high input gate capacitance as the time constant increases. This can be a limiting factor in the design of short pulse generators using MOSFETs with high gate capacitance.
5) The voltage gain associated with this topology can be high due to high inductor current and low input capacitance.
6) The resonant voltage oscillation associated with MOSFET turn-off can result in false triggering of the gate signal.

From this summary, there are two main challenges with this topology. The first is the high voltage gain associated with turn-on, and the second is the resonant ringing during MOSFET turn-off which may result in false turn-on.

I. High voltage gain problem

MOSFETs are capable of managing $\pm 30V$ short gate voltage pulses. However, the high voltage gain associated with the proposed gate driver circuit poses a threat to safe operation of the MOSFET. Therefore, a clamping mechanism has to be implemented in order to operate the MOSFET within its safe voltage limits.

The gate voltage can be clamped using passive and active methods. Passive clamping uses fewer components whereas, active clamping uses feedback circuits and control logic to restrict the gate to a user defined voltage.

1) Passive voltage clamp

In [8] fast clamping diodes are described, which limit the gate voltage to a fixed, known value. This method can be used effectively by minimising the parasitic inductances in the current loop. An alternative to using a fast clamp diode is to use a Transient Voltage Suppressor (TVS) diode to clamp the voltage to a maximum. Traditionally, Zener and TVS diodes have been used for ESD and surge protection. These silicon junction devices, when used within their operating limits can also be used for effective voltage clamping. The disadvantage is that the losses are high as the excess inductor current is diverted through the TVS when the voltage clamping is in operation. Alternatively, both the fast clamp diode and TVS can be used together, with the TVS operating as a protection mechanism clamping any overshoot voltage. The effective gate capacitance of the test device is also slightly increased.

2) Active voltage clamp

MOSFET gate drivers have been proposed which use active control of the gate drive output stage to limit the peak gate voltage to a safe level. In [6], peak gate voltage is controlled by means of adjusting the relative on-time of the driver stage MOSFET. The design requires precise control of the delay between the complementary totem pole switches to limit the gate voltage. In [9] a voltage feedback method is described, where the energy supply is continuously adjusted to maintain a constant on-state gate voltage.

In a solid-state pulsed power system, an array of MOSFETs and their corresponding gate driver circuits are required to operate synchronously. The addition of complex relative switch timings and feedback circuits can severely

complicate the structure of the pulse power system. It is therefore, favourable to use a simple passive circuit design. Also, most of the techniques described have been designed for applications such as resonant converters, where ultra-fast rise and fall times are not critical.

Passive voltage clamping using fast clamp diodes and TVS diodes was chosen for the proposed gate driver design due to simplicity and ease of implementation. The losses associated with the TVS can be higher in comparison to a feedback controlled driver. However, these are negligible as the design is restricted to single and multiple burst mode pulses, where switching performance is the primary concern.

II. Turn-off oscillation problem

Parasitic inductances in the turn-off path appear in series with the internal resistance and the gate capacitance of the power MOSFET. This results in an under-damped oscillatory state of resonance. This oscillation presents a problem of an undesired turn-on voltage on the MOSFET gate. Three methods can be used to reduce the influence of these oscillations on the false triggering of the power MOSFET.

1) *Critical damping*

   Critical damping can be achieved by adding series resistance in the gate discharge path and establishing the dynamic condition where $\alpha = \omega_0$.

2) *Negative bias*

Adding a negative bias can improve the turn-off response. More importantly, it improves circuit noise immunity as the resonant oscillations are offset below the power MOSFET gate threshold voltage, towards the negative rail.

3) *Schottky/ TVS diode*

The TVS diode used for gate voltage clamping provides a low impedance return current path for the parasitic inductances, hereby clamping the oscillations. Alternatively, a Schottky diode with a low voltage drop can be connected in parallel with the input gate capacitance to create this path. Figure 3.10 illustrates the circuit arrangement with and without a shunting diode. The resonant energy built up in the stray inductor L during the discharge of the capacitor is circulated with the help of a diode, hereby preventing the capacitor negative voltage swing.

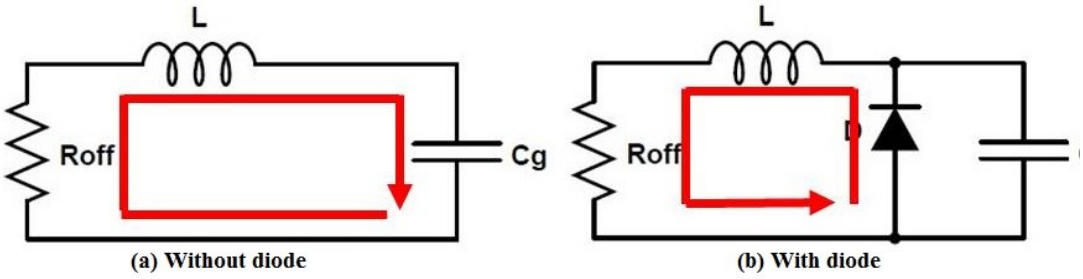


Figure 3.10: Equivalent gate driver circuit with and without a TVS/Schottky diode. The inductor current paths are shown just before resonance occurs.

Figure 3.11 shows the turn-off waveform of the gate voltage, in response to the three methods mentioned. The natural response of the turn-off circuit results in ringing and can cause false triggering when the gate voltage resonates to $+6V$, which exceeds the threshold turn-on voltage of the power MOSFET. With critical damping, the oscillations are damped. However, the turn-off delay of the circuit increases.

When a negative bias of -7V is applied to the circuit, the oscillations are offset towards the negative rail, thereby avoiding any false triggering. Furthermore, the turn-off response with the negative bias is faster than the natural response of the circuit. As expected with a TVS diode, the parasitic current finds a low impedance path, hereby reducing the oscillations.

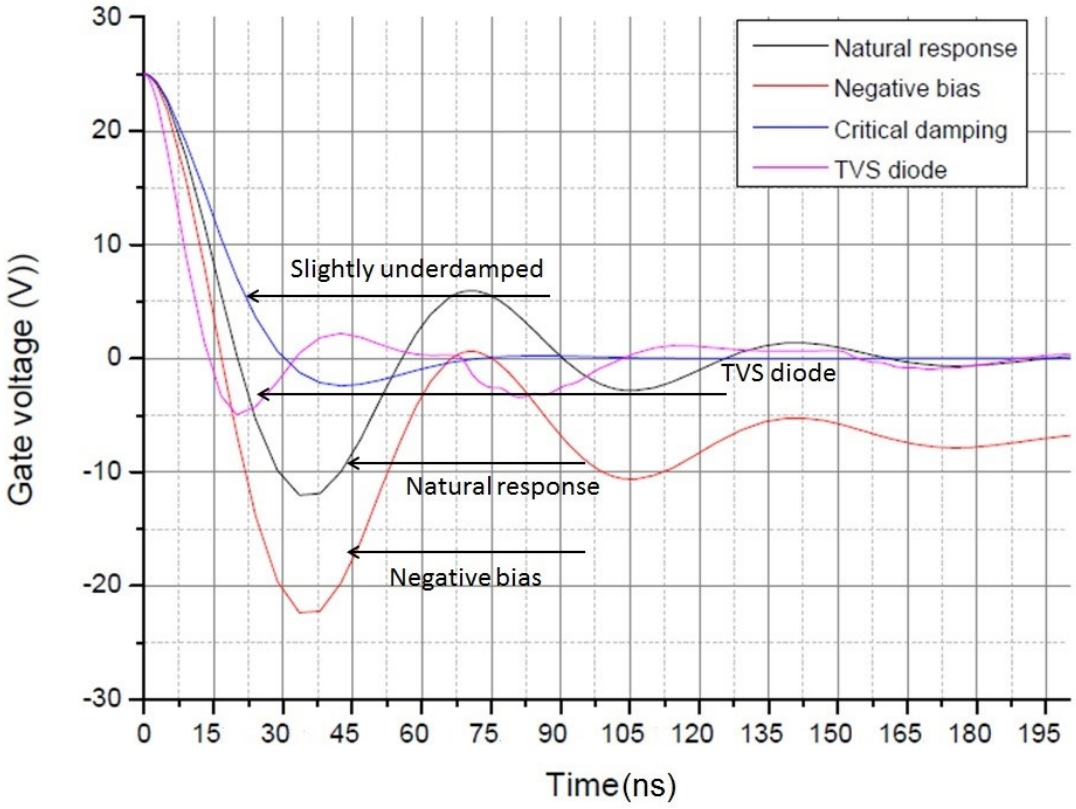


Figure 3.11: Simulated turn-off response waveforms for the three methods to control false-triggering gate driver signals.

A TVS diode is a critical component in the proposed gate driver circuit. Therefore, the turn-off oscillations are inevitably clamped. However, parasitic inductances between the TVS and the MOSFET gate die result in smaller amplitude but higher frequency oscillations. This can be suppressed by adding a small negative bias voltage to the circuit.

Based on the gate driver analysis, the gate driver circuit design was optimised. Figure 3.12 illustrates the modified gate driver circuit.

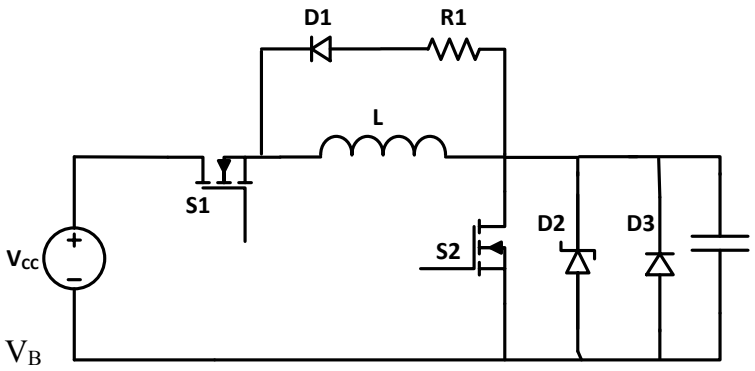


Figure 3.12: Modified gate driver circuit.

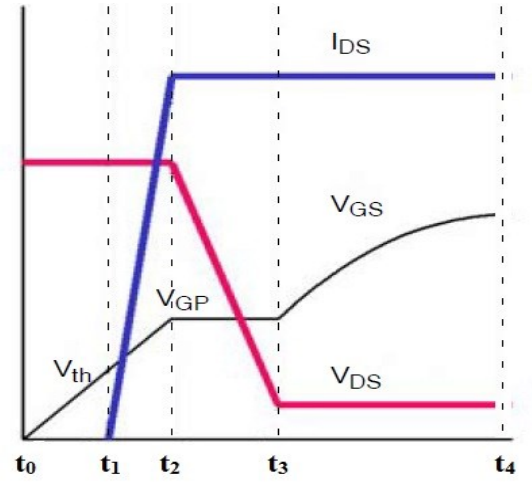
The main modification to the circuit is inclusion of a Schottky diode D3 in parallel with the TVS, which are placed very close to the gate terminals. The energy stored in the stray loop inductance is thus circulated through the diode reducing the effect of resonant oscillations during turn-off.

3.4 Effect of Miller capacitance on gate driver switching

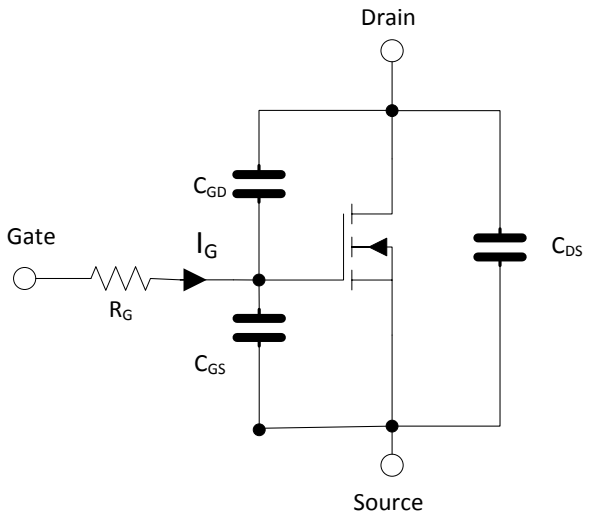
The basic analysis in section 3.3 helps identify system response and addresses key design conditions for optimising performance. However, in practice, MOSFET switching is not linear, as described earlier, due to the effects of non-linear parasitic capacitances within the physical parameters of the MOSFET. The specific analysis of the switching transient thus requires a fundamental understanding of MOSFET switching properties.

3.4.1 Turn-on

Figure 3.12(a) shows the typical switching waveforms at MOSFET turn-on where the turn-on transition can be separated into four periods. The switching delays and turn-on speed of the MOSFET are associated with two main parasitic capacitances, C_{GS} and C_{GD}, shown in the equivalent circuit in Figure 3.12(b).An approximate value of C_{GS} corresponds to the data sheet value of C_{ISS}, while an approximate value of C_{GD} corresponds to the data sheet value of C_{RSS}.



(a)



(b)

Figure 3.12: (a) MOSFET turn-on waveforms and (b) MOSFET equivalent circuit.

The gate voltage rise is brought about by charge changes in C_{GS} and C_{GD}. These capacitances vary as a function of the drain voltage V_{DS}, with C_{GD} having greater dependence due to the dV_{DS}/dt. During t_0-t_1, the gate voltage rises and there is no change in V_{DS}. Therefore, C_{GS} and C_{GD} can be assumed to be constant, with C_{GS} being significantly larger than C_{GD}. This can be verified by observing the capacitance curves from a typical MOSFET data sheet, as shown in Figure 3.13. Therefore, it can be assumed that a majority of the gate current is used in charging C_{GS}, which can be extracted from the data sheet as C_{ISS}. As the gate voltage begins to rise and approaches the threshold voltage at t_1, the MOSFET drain current begins to rise to the full load current and the Miller plateau voltage V_{GP} is reached at t_2.

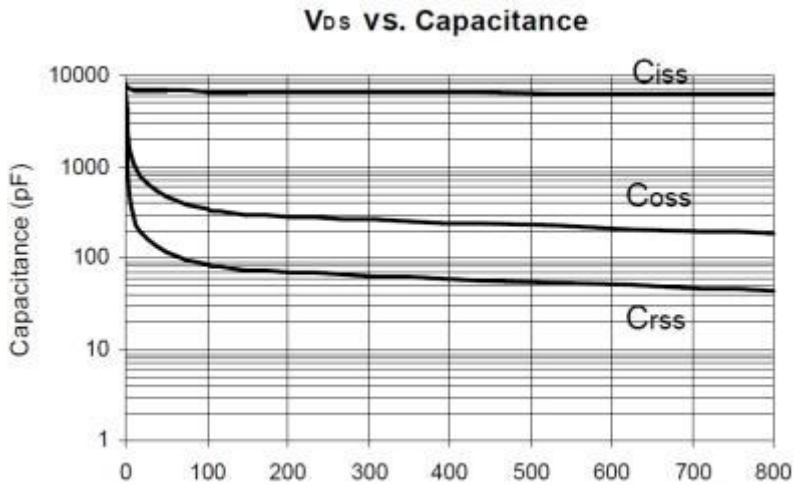


Figure 3.13: Typical capacitance curves extracted from MOSFET data sheet showing the variation in the parasitic capacitances with V_{DS}. [10].

The Miller plateau voltage V_{GP} is a function of the MOSFET trans-conductance and can be represented by [11]:

$$V_{GP} = V_{TH} + \frac{I_D}{g_{fs}} \tag{3.22}$$

V_{GP} is the Miller plateau voltage

V_{TH} is the MOSFET threshold voltage

I_D is the full load drain current

g_{fs} is the MOSFET transconductance

Alternatively, the value of V_{GP} can be estimated using the gate voltage versus gate charge curve specified on the MOSFET data sheet and similar to Figure 3.14.

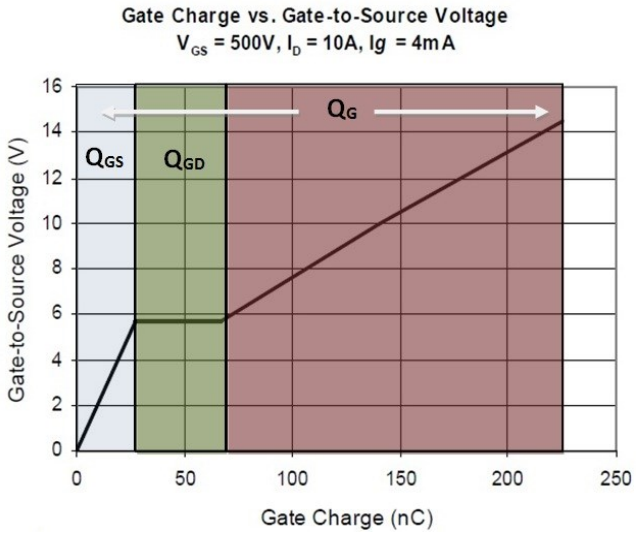


Figure 3.14: Typical Gate charge versus Gate voltage curve extracted from MOSFET data sheet [10]. The Miller plateau voltage specified for this specific device is approximately 6V.

For analysis, the circuit conditions can be assumed to be linear and can be represented as a voltage driven series RLC circuit as shown in Figure 3.15.

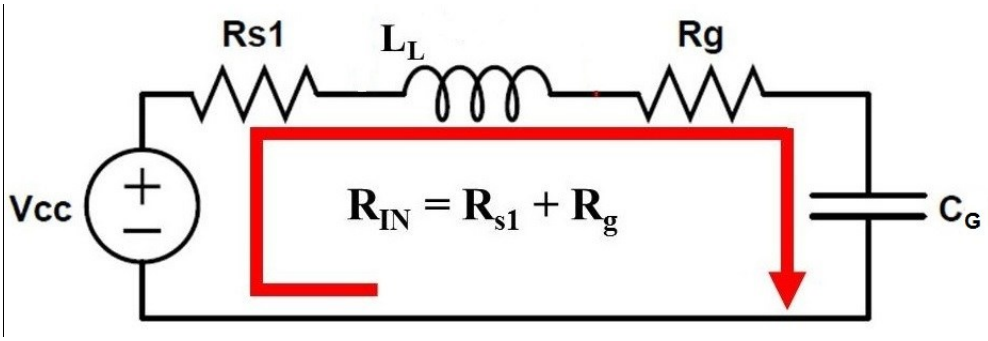


Figure 3.15: Equivalent circuit during turn-on.

The resistance R_{IN} corresponds to the total input gate resistance $(R_G + R_{SI})$, L_L corresponds to the sum of the external gate driver inductance and the parasitic inductances in the circuit and C_G=C_{ISS} is the input gate capacitance. The transient response during t_0-t_2 can be estimated using equations (3.2) to (3.12). Using equation (3.12), the Miller plateau voltage can be rewritten as

$$V_{GP} = V_{IN} - V_{IN}e^{-\alpha t}\cos(\omega_d t) + \frac{-(I_L(0) + C_G \alpha V_{in})}{C_G \omega_d} e^{-\alpha t}\sin(\omega_d t) \qquad (3.23)$$

where $V_C(t) = V_{GP}$ is the Miller plateau voltage at t_2

$C_G = C_{ISS}$ is the input gate capacitance

$t = t_2$-t_0 is the time taken to rise to V_{GP}

When the load current reaches its maximum, the voltage V_{DS} across the device starts to fall rapidly. During this transition there is a resultant increase in the Miller capacitance C_{GD} and in the gate capacitance C_{GS}, with the rise in C_{GD} being more significant, as shown in the capacitance curves in Figure 3.13. It is therefore assumed that a majority of the gate current is used to charge C_{GD}. The dV_{DS}/dt corresponds to the time it takes to charge the Miller capacitance. However, it is difficult to estimate this capacitance for the fall time of V_{DS}. Therefore, the data sheet value of Q_{GD} can be used and divided by the total voltage swing experienced on the drain connection. This gives a value of C_{GD} based on the data sheet transient [11].

The effective miller capacitance C_{GDeff} is

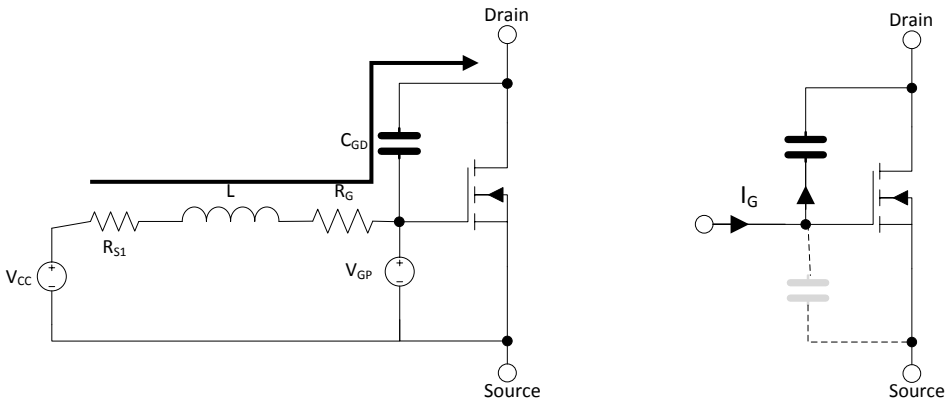
$$C_{GDeff} = \frac{Q_{GD}}{V_{DS} - V_F} \qquad (3.24)$$

where Q_{GD} is the gate-to-drain charge in the Miller region

$V_{DS} = V_{IN}$ is the supply voltage

$V_{DS\,(ON)}$ is the on-state forward voltage across the MOSFET

In the Miller plateau region, it is assumed that the voltage across C_{GS} is constant and that all current is diverted into charging the rapidly changing C_{GD}. The V_{GS} waveform during period t_2-t_3 is therefore relatively flat. Charging can be assumed to be linear and the circuit conditions during this period can be represented by the equivalent circuit shown in Figure 3.16(a). The gate-to-source capacitance C_{GS} is represented as a voltage source since it is charged to a voltage with a magnitude of V_{GP}. Assuming a constant inductor current, the equivalent circuit can be simplified for calculation as shown in Figure 3.16(b).



(a) **(b)**

Figure 3.16: Miller plateau MOSFET turn-on (a) equivalent circuit of gate driver and (b) simplified circuit.

The V_{DS} fall time t_{FV} corresponds to the Miller capacitance charging time and can be calculated as

$$t_{FV} = \frac{Q_{GD}}{i_G} \qquad \text{or } t_{FV} = \frac{C_{GDeff}(V_{DS} - V_F)}{i_G} \tag{3.25}$$

It is assumed that all current is diverted into C_{GD}. Therefore, a rise in V_{GS} in the Miller region is normally observed to be relatively flat. At t_3, V_{DS} has fallen to its on-state forward voltage V_F, and C_{GD} becomes constant and almost equivalent to C_{GS}. The MOSFET is on at this time, but the voltage has to increase further to enhance the conducting channel. The charge accumulated in the interval between t_3 and t_4, $Q_{G(ON)}$ is,

$$Q_{G(ON)} = Q_G - Q_{GS} - Q_{GD} \tag{3.26}$$

This can be correlated to the charge curve for a given MOSFET from the data sheet shown in Figure 3.14. Similar to the Miller charging time, the time taken to rise to the voltage V_{GS} is,

$$t_{VGS} = \frac{Q_{G(ON)}}{i_G} \tag{3.27}$$

3.4.2 Turn-off

Figure 3.17 shows the typical MOSFET turn-off waveforms where the characteristics are similar to those at turn-on. However, the turn-off process is largely influenced by the presence of path resistance and loop inductance in the circuit, as shown in the analysis in section 3.3. The switching transient can be analysed in a reverse order.

At t_5 the MOSFET gate is charged to an initial gate voltage V_{GS}. When the switch S2 is turned on, V_{GS} falls to the Miller plateau voltage V_{GP}. Since the total capacitance is unknown, the value of $Q_{G(ON)}$ is used to derive an equivalent

capacitance based on the voltage swing between V_{GS} and V_{GP}. The effective capacitance C_{Geff} between t_5-t_6 is [11]:

$$C_{Geff} = \frac{Q_{G(ON)}}{V_{GS} - V_{GP}} \tag{3.28}$$

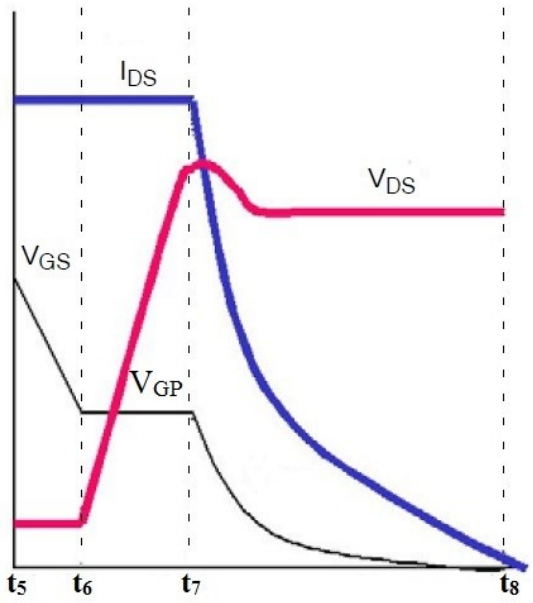


Figure 3.17: MOSFET turn-off waveform.

An equivalent circuit modelled during t_5-t_6 is shown in Figure 3.18. The circuit shows that the energy from the equivalent capacitance $C_G = C_{Geff}$ discharges through the loop inductance L_L and internal resistance R_L formed by the circuit. The voltage and current response can be estimated using equations (3.20) and (3.21).

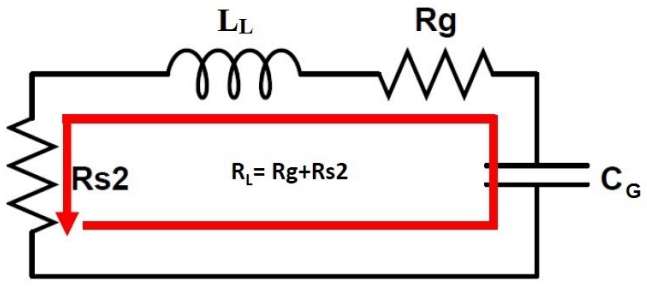


Figure 3.18: Equivalent circuit during turn off.

Similarly, during the Miller plateau region between t_6-t_7, the circuit can be modelled using Figure 3.18 where C_G=C_{GDeff} which is estimated using equation (3.24). Finally, the time taken for the gate voltage to fall to zero between t_7-t_8 is estimated by replacing C_{GDeff} with C_{ISS} in Figure 3.18. Common to both turn-on and turn-off is that the Miller region occurs during the drain voltage transition period.

3.4.3 Discussion

To calculate the actual response time of the gate driver is complicated. The analysis described aids understanding and more precisely estimates the varying MOSFET characteristics during the switching transients. The most relevant part of the analysis is the calculation of the switching time during the Miller plateau region, as this determines the time taken for the drain voltage to fall or rise. The charging and discharging of other parasitic capacitances has more effect on the input/output delay and the minimum achievable pulse widths with the device.

From the analysis, it can be deduced that the switching speed is dependent on the availability of the source current at the beginning of the Miller plateau region. It must be highlighted that the analysis using the current source driver presents a different switching characteristic in comparison to a voltage source driver. With the proposed gate driver topology, high current influences the speed of turn-on. During turn-off, however, a voltage source characteristic is exhibited. The proximity of the gate driver to the MOSFET has less influence during turn-on. However due to the voltage source characteristic during turn-off, the switching delay is influenced by the gate loop inductance. The proximity of the gate driver will depend on the minimum pulse width requirements for a specific design. For the proposed application, the

required minimum pulse width is approximately 70ns. Therefore, proximity i.e. low inductance design will be a key design parameter.

3.5 Pulse generator logic circuit

The logic circuit required to generate the gating signal for the two driver stage MOSFETs, S_1 and S_2 is simple. The circuit primarily consists of *RC* networks to generate delays, Schmitt triggers for inverted output logic and *XOR* gates to generate the output signals to the corresponding gate driver inputs for S_1 and S_2. The waveforms for the logic circuit and the circuit schematic are illustrated in Figures 3.19 and 3.20, respectively. The signals in Figure 3.19 correspond to the logic outputs shown in Figure 3.20.

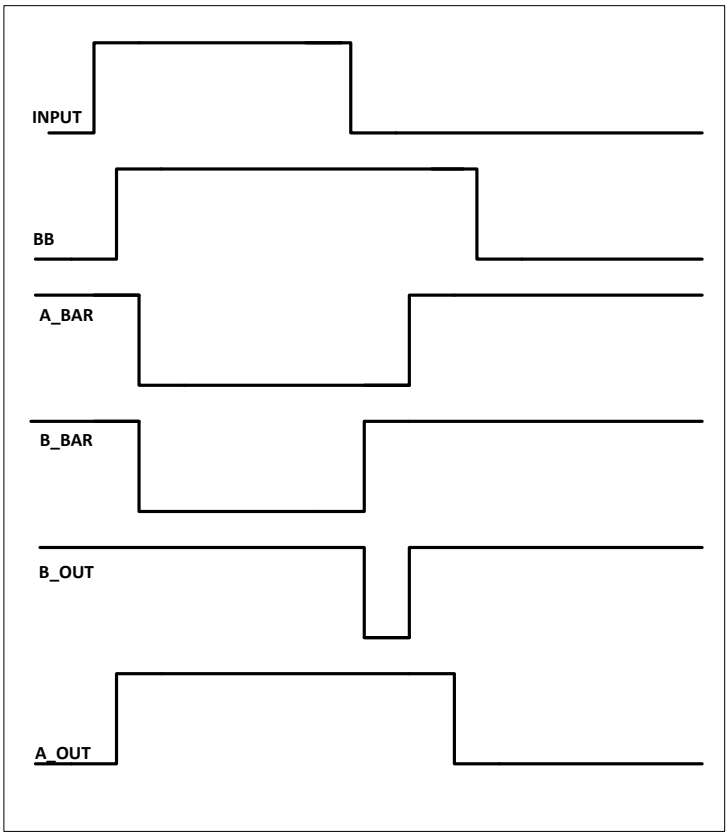


Figure 3.19: Logic circuit timing diagram.

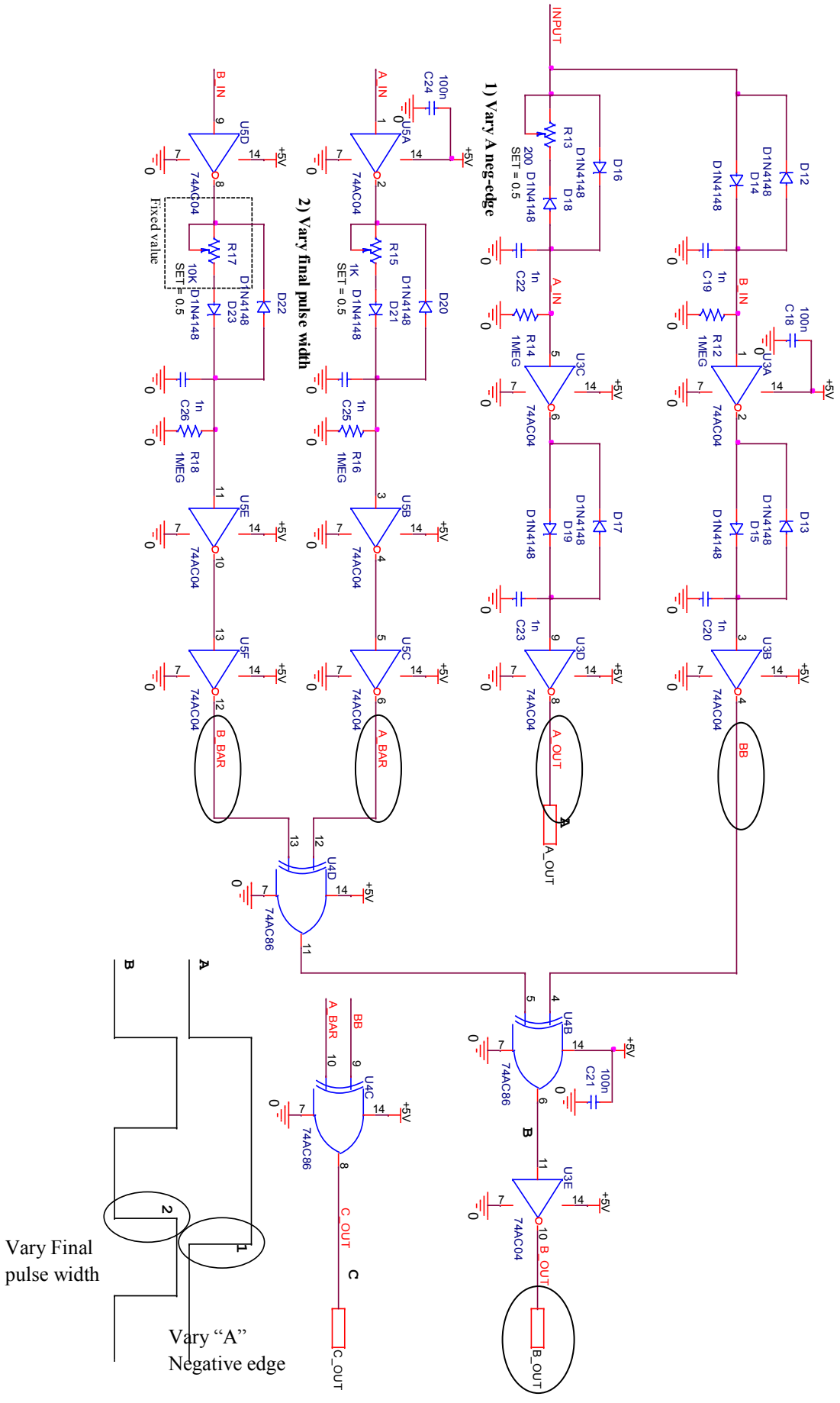


Figure 3.20: Detailed schematic of the pulse generator logic circuit

The waveform input signals correspond to the important logic output points which are highlighted in the logic circuit schematic of Figure 3.20. Signals *A_OUT* and *B_OUT* represent the input signals into the gate drivers for S_1 and S_2. *INPUT* corresponds to the input signal from the function generator. *BB, A_BAR* and *B_BAR* correspond to logic input signals into the *XOR* gates.

To illustrate the design of the pulse generator circuit, Table 3.1 summarises the design parameters which are based on actual values used in the gate driver. The on-time of *S2* determines the inductor charging time. *S1* is on for an extended period of time, until the output gate pulse is delivered. The function generator is programmed to output a 1μs signal. In order to convert this signal into the two input signals required for switches *S1* and *S2*, the processing described in section 3.5.1 and 3.5.2 occurs.

Table 3.1: Pulse generator specification.

Function generator output	1 μs
Input signal for S1 (schematic ref: A_OUT)	1.2 μs ON
Input signal for S2 (schematic ref: B-OUT)	1μs ON 50-100ns OFF
Pulse width	50 - 100ns
Repetition rate	Single/ Multi (up to 400 kHz)

3.5.1 Input signal for S1

In order to convert the input 1μs signal to 1.2μs, a trailing edge delay circuit was designed. Figure 3.21 shows the trailing edge delay circuit.

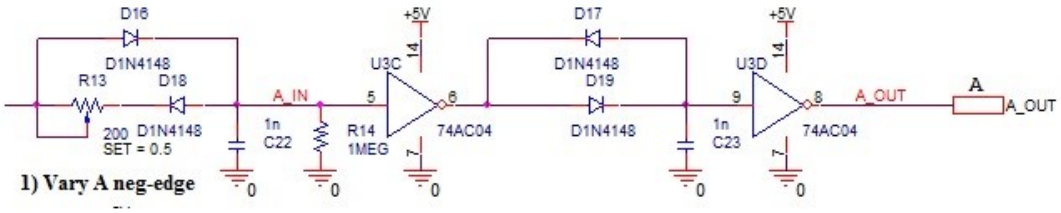


Figure 3.21: Trailing edge delay circuit.

In this circuit, the leading edge of the input pulse bypasses the delay circuit through the diode *D16* and into the input of the Schmitt trigger. During this time capacitor *C22* of value 1nF is charged to the input voltage. During pulse turn-off, the capacitor discharge path is blocked by *D16* and is therefore discharged through *D18* which has a series connected variable resistor, forming an RC delay circuit. With a variable resistance of 200Ω, the time constant is 200ns. The characteristic of a Schmitt trigger is that it outputs a high or a low signal when a threshold input voltage is reached. During the leading edge of the input signal, the threshold voltage is reached much faster than during the trailing edge. This increases the trailing output pulse width of the signal to 1.2µs. Figure 3.22 illustrates the switching diagram for the trailing edge delay circuit. Since the output of the Schmitt trigger is inverted, a second Schmitt trigger is used to invert the output signal to the original positive pulse.

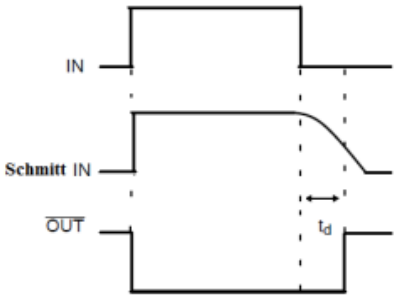


Figure 3.22: Timing diagram for trailing edge delay signal.

3.5.2 Input signal for S2

The signal requirements for *S2* are an ON-time of 1µs followed by an OFF-time of 50 to 200ns which is the required gate driver pulse width. In order to satisfy these design conditions, an XOR gate was used to generate the short pulse width. Two signals are fed into the inputs of the XOR gate. Each signal is inverted and the rising edge delay is increased using a delay circuit. The variable resistor in input A adjusts the pulse width to between 50ns and 200ns. This is compared with a fixed output from input *B* which is converted into a single output pulse using the XOR logic. The output pulse is a positive rising pulse, but the required signal for *S2* needs to be inverted. Therefore, the output is connected to another XOR gate and compared with the output from signal BB to generate the required input signal into *S2*.

3.6 Driver layout

Critical to gate driver performance is PCB layout. Shorter track loop area ensures lower parasitic inductances. The critical paths that require attention are highlighted in Figure 3.23.

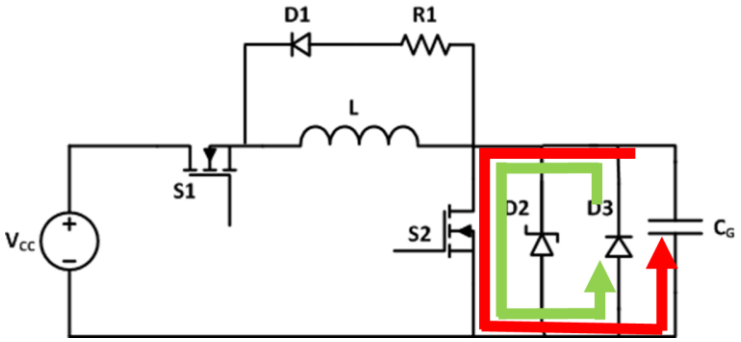


Figure 3.23: Critical current paths for layout optimization.

Path 1is critical to reducing the turn-off delay of the device under test, whereas Path 2 is critical to reducing the effect of resonant voltage ringing at the MOSFET gate

terminal. Path 1 complements path 2 by providing a lower path inductance. Path 2 is improved by placing the diode close to the gate terminal. A detailed PCB layout and technical information related to the layout design are discussed in Appendix B.

3.7 Experimental results

In this section, experimental results are presented for the proposed current source gate driver.

3.7.1 Driver and circuit parameters

Table 3.2 highlights the design specifications. This section outlines the component selection process for the gate driver circuit.

Table 3.2: Test conditions and performance specifications for gate driver test circuit.

Design parameters	**Value**
gate driver voltage **(V_{IN})**	20V
test circuit voltage **(V_{DC})**	50V
test load **(R_L)**	11Ω
turn-on/off time	< 10ns
pulse width	60ns - 100ns
test frequency	single shot, 400kHz burst

I. Driver stage MOSFETs

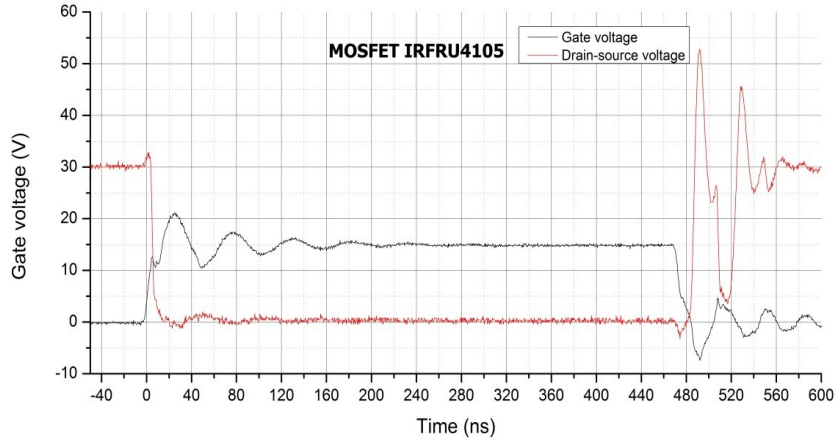
The driver stage MOSFETs comprise switches S_1 and S_2. S_1 is an isolation switch and does not need to have ultra-fast switching properties. It is driven by an opto-coupled gate driver (ACPL-H342-000E). S_2 however, requires high switching performance and lower on-state resistance. Three MOSFETs were considered for S_2, with characteristics highlighted in Table 3.3.

Table 3.3: Data sheet characteristics of the evaluated driver stage MOSFETs.

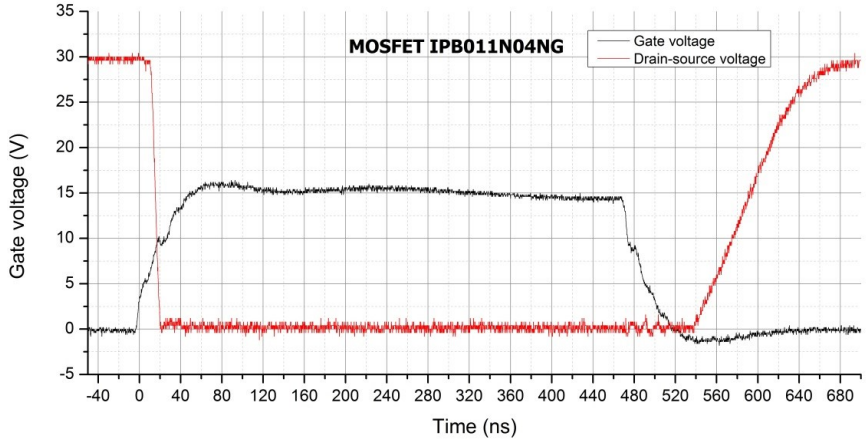
No.	MOSFET	$R_{DS\,(ON)}$ (mΩ)	C_G (pF)	BV_{DS} (V)	Data sheet turn on/off times (ns)
1	IRFRU4105	45	700	45 V	7/31
2	IPB011N04NG	1.1	16000	40 V	40/63
3	BSC047N08NS3G	4.7	3600	80 V	18/44

The MOSFETs are numbered for the discussion. The data specified in the manufacturers' data sheets are tested under different operating conditions and therefore do not give an accurate indication of relative performance. The switching delays and transition times are influenced by the selection of the controlling gate driver chip. Therefore, the performances of the three MOSFETs were experimentally verified using a high current gate driver *EL7158*. Figure 3.24 shows the waveforms of the gate voltage and the corresponding drain-source voltage of the three devices.

The advantage of MOSFET 1 is the low input capacitance, which facilitates faster switching using readily available MOSFET gate driver chips, as seen in Figure 3.24(a). However, it suffers from high on-state resistance, which translates into a high on-state voltage when conducting high currents. Moreover, this adds to the parasitic resistances in the turn-off path, which can increase the turn-off delay. MOSFET 2 has the advantage of an ultra-low $R_{DS(ON)}$. However it suffers higher turn-on and turn-off delays due to higher input and output capacitances. This can be seen in Figure 3.24(b). This can affect the minimum achievable pulse-widths and therefore is disadvantageous. MOSFET 3 has the distinctive advantage of a combination of low $R_{DS(ON)}$ and low input capacitance. Notably, MOSFET 3 offers performance that meets the design specifications. MOSFET 3 was therefore chosen for the proposed gate driver design.



(a)



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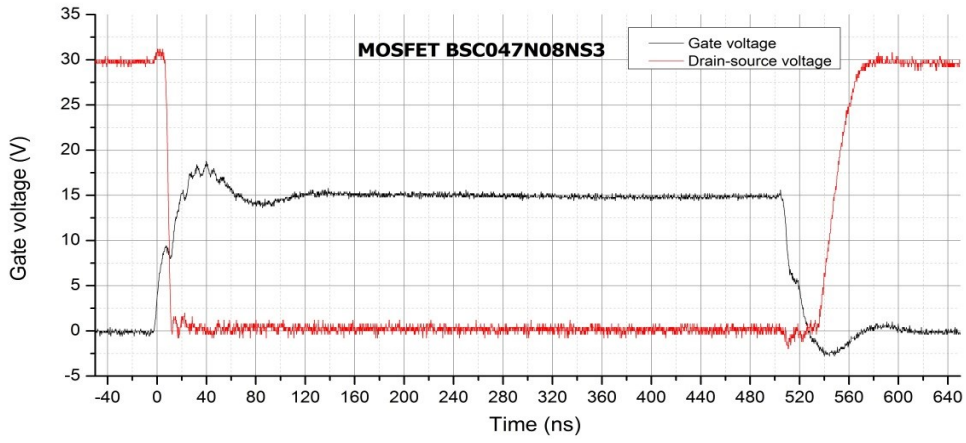


(c)

Figure 3.24: Waveforms for (a) MOSFET 1, (b) MOSFET 2, and (c) MOSFET 3.

II. TVS diodes

Generic TVS and Zener diodes are generally not used in high speed signalling applications. The presence of the p-n junctions results in an intrinsic parasitic capacitance. This capacitance is non-linear and decreases as the reverse bias voltage increases across the junction. It is therefore a common practice to use ultra-low capacitance Zener diodes in high-speed bus protection. However, the proposed gate driver circuit operates at high speeds and relatively higher power. From the gate driver analysis and through the selection of the driver MOSFETs, a drive current of 30A was chosen. The instantaneous power dissipation in a 20V Zener diode is therefore:

$$P_Z = V_Z I_G = 20 \times 30 = 600\text{W} \tag{3.29}$$

Therefore, a high pulse power TVS diode is required for protection. High power, low-voltage transient voltage suppressors are thin and have larger physical structure areas, and therefore have higher junction capacitance. Their nonlinear capacitance is relatively higher and therefore results in an increased turn-on delay. It is therefore essential to account for this in the gate driver design. To verify this, two 18V TVS diodes (*SMCJ18A* and *SMAJ18A*) were tested. Figure 3.25 highlights the junction capacitance curves for the two devices extracted from the manufacturer's data sheets.

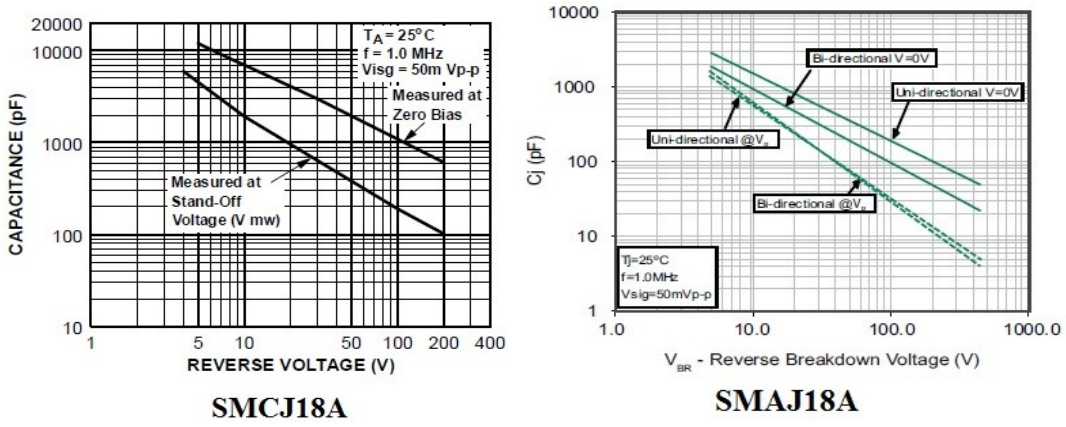


Figure 3.25: Junction capacitance curves for SMCJ18A and SMAJ18A [12].

The SMCJ18A is a higher power device with a 1500W pulse rating, whereas the SMAJ18A has a 400W rating. The junction capacitance curves show the nonlinear capacitance of the two devices. The higher power device has a variable capacitance between 10nF and 1nF at clamping voltage, whereas, the lower power device has a variable capacitance between 1500pF and 300pF. Figure 3.26 shows the experimental waveforms of the gate voltage for the two devices. There is a visible decrease in the turn-on delay of the gate pulse for SMAJ18A. Careful consideration must therefore be given to the choice of the protection diodes. The 400W pulse rated SMAJ18A therefore satisfies the power requirements for the proposed gate driver application.

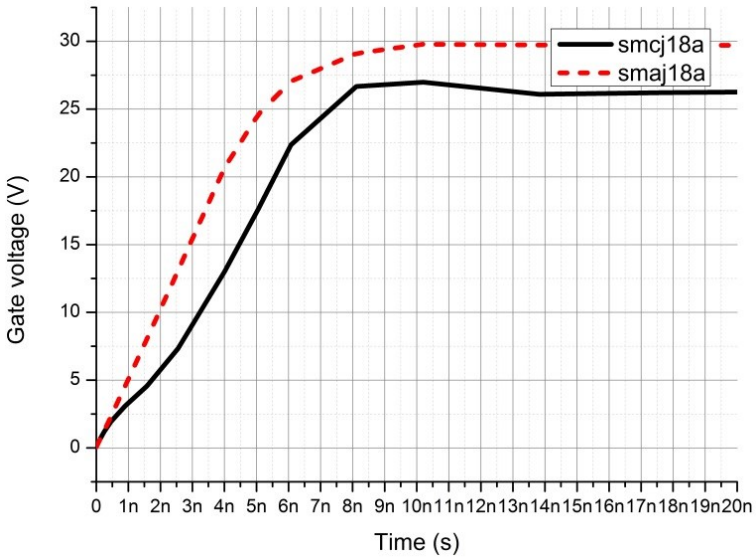


Figure 3.26: Gate voltage waveforms with different TVS diodes.

III. Driver inductor

The inductor is sized using the law of conservation of energy. The energy in the inductor E_L is,

$$E_L = \frac{1}{2} LI^2 \tag{3.21}$$

The energy in the gate capacitor E_C is,

$$E_C = \frac{1}{2} CV^2 \tag{3.22}$$

Using the law of conservation of energy, minimum energy required $E_C = E_L$. A safe operating margin can be established with energy in the inductor being twice as higher than the energy required by a capacitor.

For the proposed gate driver, a power inductor designed by Vishay Dale (IHLP6767GZERR47M01) with an inductance of 470nH (1.3mΩ, 123Adc

saturation) was chosen. The relatively large inductance simplifies the pulse generation process when using a basic function generator for experimentation.

3.7.2 Driver evaluation and device selection

Device evaluation is an important process in developing a high performance pulsed power system. It also forms the basis for the evaluation of the proposed gate driver. This section evaluates the performance of the gate driver and the device selection made for the pulsed power system.

In order to assess the performance of the gate driver, three high voltage MOSFETs were selected, each with different ratings and switching characteristics. Table 3.4 highlights the key specifications of the three devices. For presentation, the MOSFETs are numbered. Each MOSFET progressively has a higher current rating consequently, higher capacitance. MOSFETs 4 and 5 are of particular interest for the pulsed power system due to their higher voltage ratings and their performance characteristics. The choice of MOSFET 6 is purely to evaluate the capability of the gate driver to drive high capacitance MOSFETs. The quoted switching times are extracted from the vendor's data sheet.

Table 3.4: High voltage device data sheet characteristics for evaluation.

No.	**4**	**5**	**6**
Device	IXZ308N120	DE475102N20	IXFN180N20
Voltage rating	1200V	1000V	200V
Current rating	8A	24A	180A
Current rating (Pulse)	48A	144A	720A
$\mathbf{t_{on}/t_{off}}$	3ns/6ns	5ns/8ns	85ns/56ns
Input capacitance	2000pF	5500pF	22000pF
Output capacitance	59pF	200pF	3800pF
$\mathbf{R_{ds(on)}}$	2.1Ω	0.45Ω	10mΩ

The rise and fall times of the tested devices have a close relationship with the total loop inductance of the test circuit. Therefore, the inductance of the test circuit should be as low as possible. Figure 3.27 shows the experimental test circuit used to assess the semiconductor switches. The test voltage is 50V across an 11Ω resistive load. The load is formed of several parallel connected Metal Electrode Leadless Face (MELF) resistors. Figures 3.28 to 3.36 show the experimental switching waveforms for MOSFET 4, MOSFET5 and MOSFET 6.

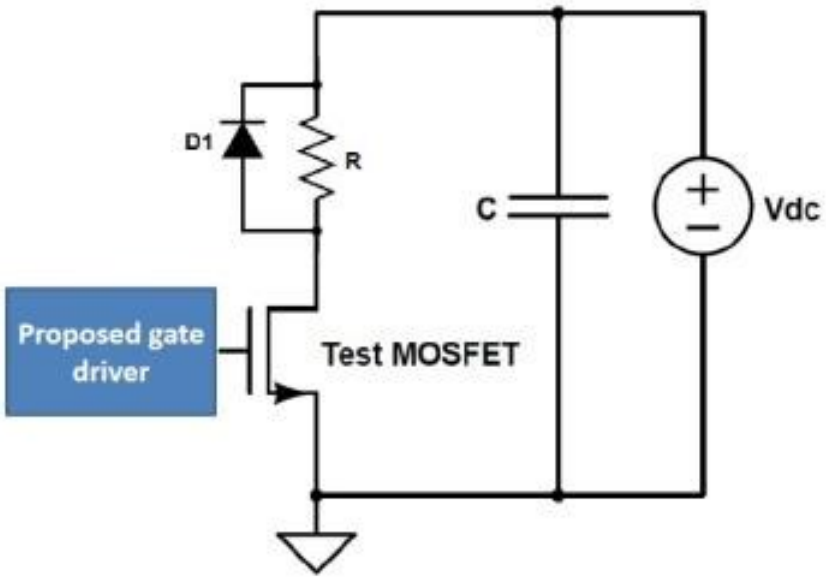


Figure 3.27: Power MOSFET test circuit.

I. Experimental results for MOSFET IXZ308N120

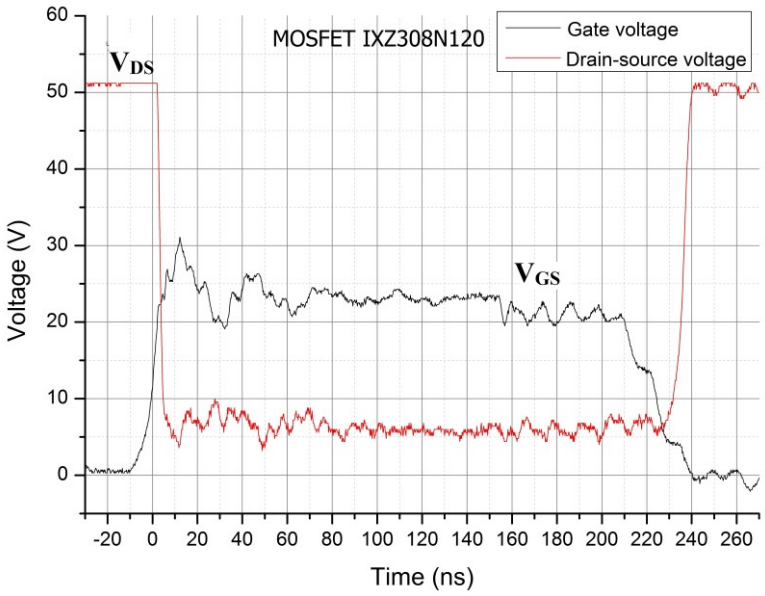


Figure 3.28: MOSFET 4 (V_G &V_{DS}).

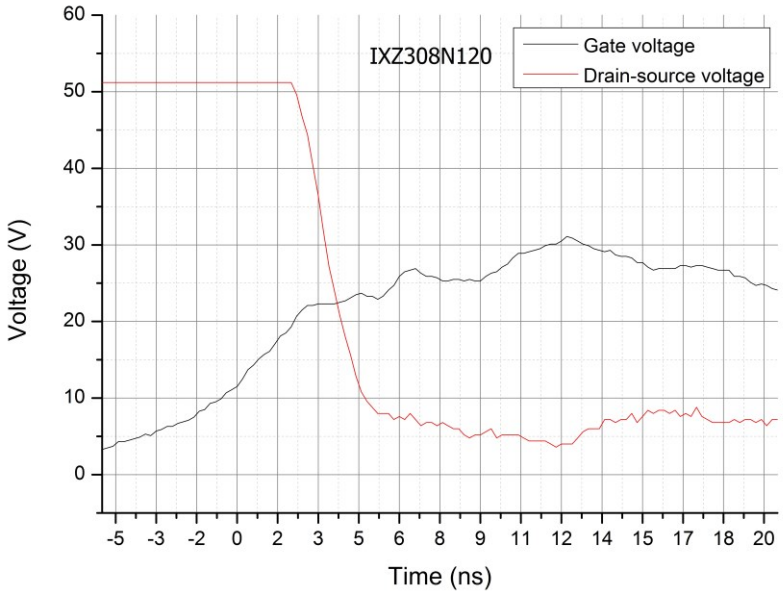


Figure 3.29: MOSFET 4 (V_{DS} fall time).

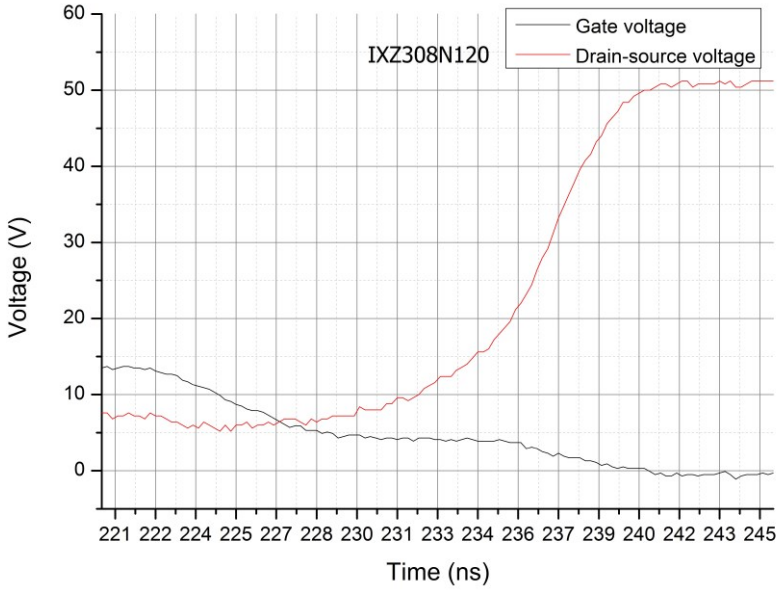


Figure 3.30: MOSFET 4 (V_{DS} fall time).

II. Experimental results for MOSFET DE475108N20

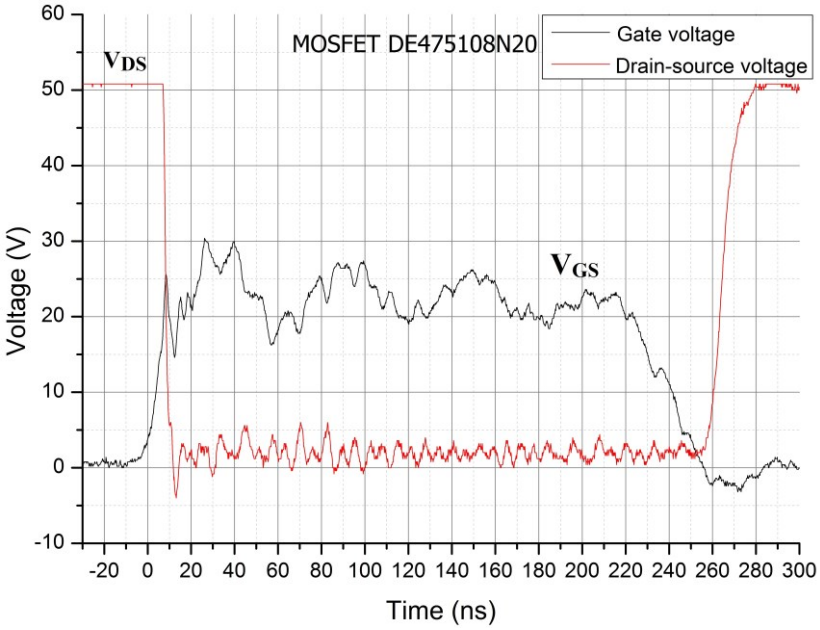


Figure 3.31: Waveforms for MOSFET 5 (V_G & V_{DS}).

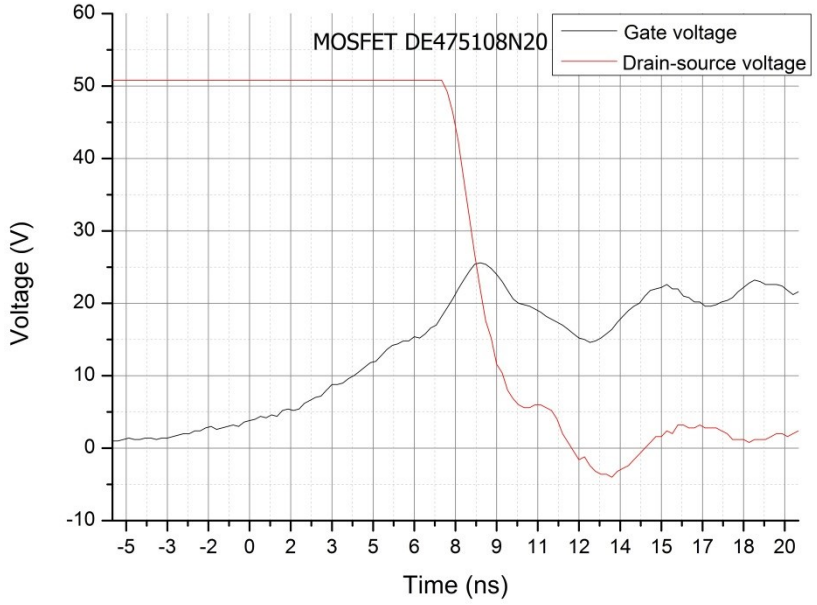
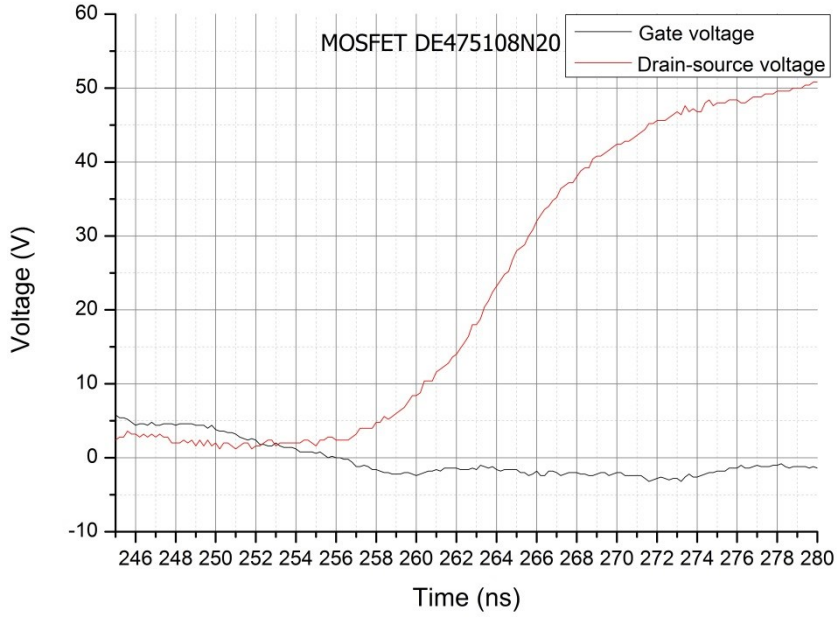


Figure 3.32: Waveforms for MOSFET 5 (V_{DS} fall time).



(c)

Figure 3.33: Waveforms for MOSFET 5 (V_{DS} rise time).

III. Experimental results for MOSFET IXFN180N20

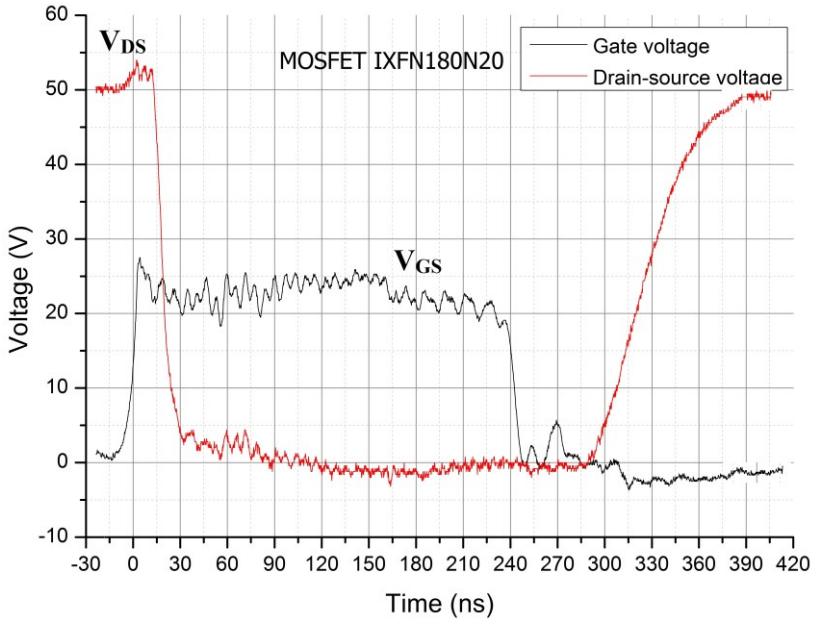


Figure 3.34: Waveforms for MOSFET 6 (V_G & V_{DS}).

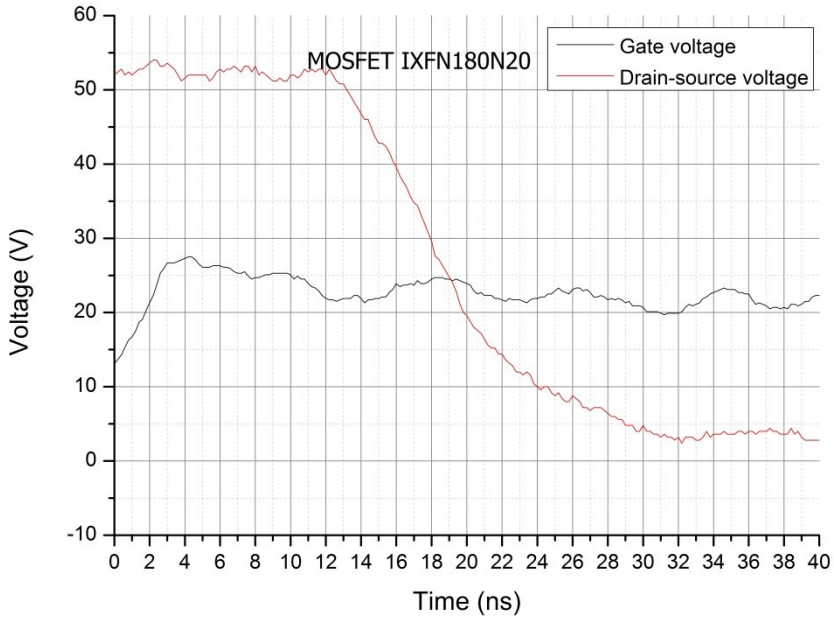


Figure 3.35: Waveforms for MOSFET 6 (V_{DS} fall time).

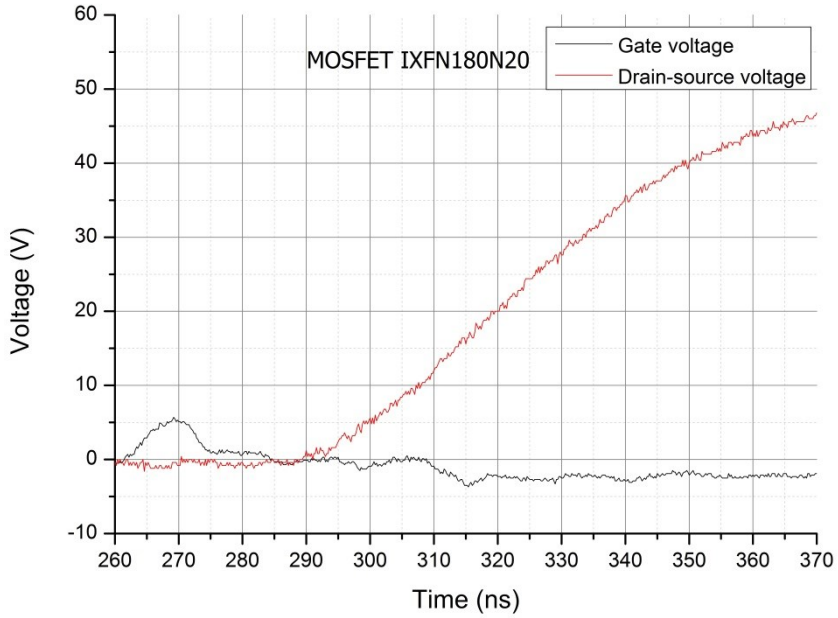


Figure 3.36: Waveforms for MOSFET 6 (V_{DS} rise time).

IV. Discussion

Table 3.5 summarises the turn-on and off times measured for the three devices. The switching times of all the three devices are enhanced at turn-on with the proposed gate driver in comparison to the manufacturer's specifications. The fastest switching is achieved using MOSFET 4 and MOSFET 5 with the rise times being 2.5ns and 3.5ns respectively. MOSFET 6 has the slowest turn-on characteristic as expected due to its significantly high input capacitance of 22nF in comparison to the other two devices which have an input capacitance of 2nF and 5.5nF respectively.

Table 3.5: Summary of measured device performances.

No.	**Device**	**test voltage**	turn-on time	turn-off time
4	IXZ308N120	50V	2.5ns	6ns
5	DE475108N20	50V	3.5ns	14ns
6	IXFN180N20	50V	14ns	60ns

The turn-off characteristic is governed by the load resistance, the parasitic inductance and the output capacitance of the MOSFETs. Similar to turn-on, MOSFET 6 shows the slowest turn-off characteristic due to its higher output capacitance. The turn-off transient can be improved by reducing the total parasitic inductance around the drain path. However, design restrictions often limit the minimum inductance that can be achieved with a specific device. This sets a limit to the device's performance. Also, MOSFETs 4 and 5 have significantly lower packaging inductance than MOSFET 6. Switching can thus also be improved by using die mounting techniques such as flip chip assembly [12], where wire bonding is removed and significantly lower package inductance is achieved.

MOSFETs 4 and 5 both demonstrate ultra-fast switching which complies with the design specifications for the pulsed power system. The advantage of MOSFET 4 is the higher voltage rating of 1200V. However, it has a high on-resistance of 2.1Ω, which translates into higher conduction losses at higher currents. An alternatively is to use a large array of parallel connected devices to reduce these losses. MOSFET 5 however, has lower voltage rating of 1000V, but has a much lower on-resistance of 0.45Ω. It is a better trade-off for lower losses, that is, a higher current rating of 144A. Fewer devices are therefore required to realise a high current module. MOSFET 5 is therefore chosen as the switching device for the proposed pulsed power system.

3.7.3 Parallel driven MOSFETs

Because of their positive $R_{DS(ON)}$ temperature co-efficient, MOSFETs can be readily connected in parallel. Conventionally, gate driver chips have been closely

located to each individual MOSFET. From the gate driver analysis and experimental results, it can be deduced that the proposed gate driver is capable of driving high capacitance devices at ultrafast switching speeds. This property can thus be manipulated to drive multiple parallel connected MOSFETs, where an array of parallel connected MOSFETs translates to an increase in the total gate capacitance. Since the proximity of the gate driver is not of concern during turn-on, the gate driver circuit can be placed at a symmetrical distance between multiple devices. Proximity, however, will have an effect on the turn-off delay. Figure 3.37 shows the experimental gate driver waveforms for different loop inductances, where a higher gate loop inductance results in a long turn off delay, thereby limiting the minimum achievable pulse width.

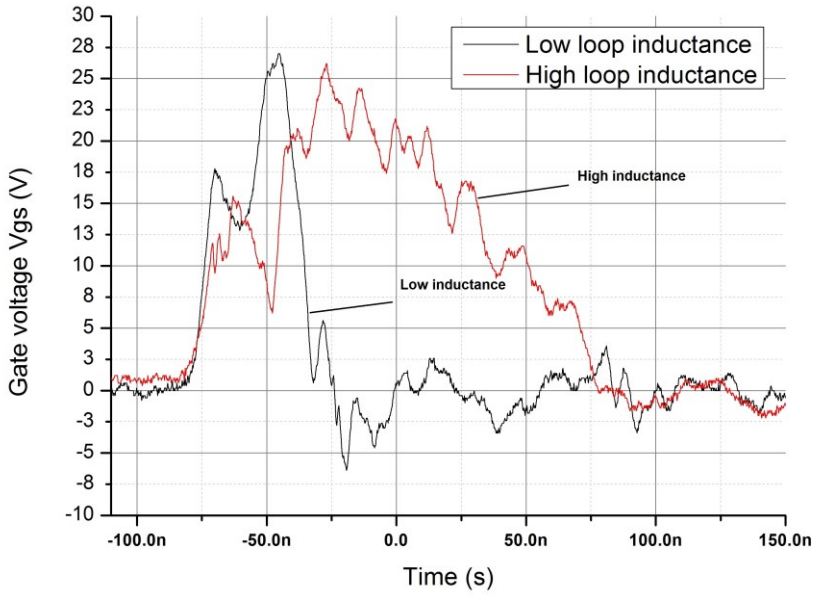


Figure 3.37: Gate voltage waveforms with different loop inductances.

For this particular example, four parallel MOSFETS were used. The shorter loop inductance was achieved by connecting coaxial wires between the gate driver and the MOSFET gate terminals whereas the larger inductance is inherent part of the layout

routing. The input pulse width for both signals is 50ns. The turn-off delay T_D is approximately 20ns for the short loop and 125ns for the larger loop. The total input capacitance C is approximately 22nF. Based on simple LC analysis:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3.23}$$

$$f_0 = \frac{1}{4T_D} \tag{3.24}$$

$$L = \frac{4T_D{}^2}{\pi^2 C} \tag{3.25}$$

Based on equations (3.23) to (3.25), the loop inductance for the short loop and the larger loop can be estimated to be 7.4nH and 288nH respectively. This puts a limitation on the proximity of the gate driver MOSFET to the device and consequently the number of devices that can be paralleled while maintaining the capability to deliver minimum pulse widths. Due to the physical dimensions of the MOSFET DE475108N20, a maximum of four devices were chosen per driver to maintain symmetry. Symmetry was achieved by placing two devices adjacent to each other on either sides of the board, as partially shown in Figure 3.38. The added benefit of this physical packaging is that the source terminals for the gate driver side have lower inductance which significantly reduces the negative feedback voltage between the source inductance terminals which can result in ringing and false turn-on of the MOSFET.

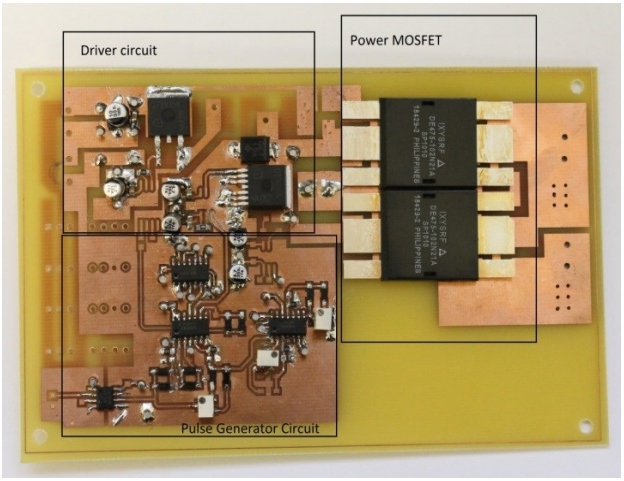
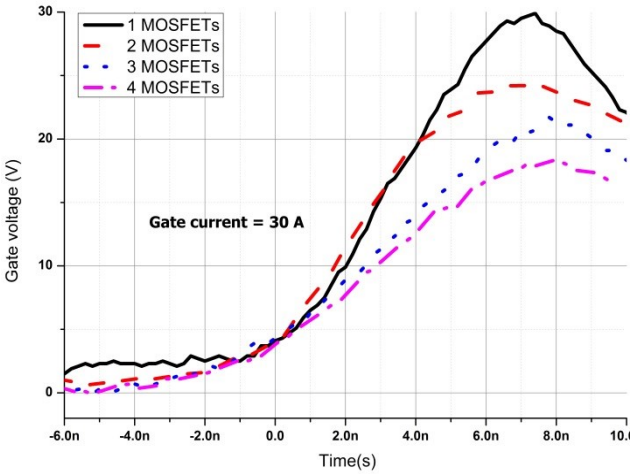


Figure 3.38: Gate driver circuit board.

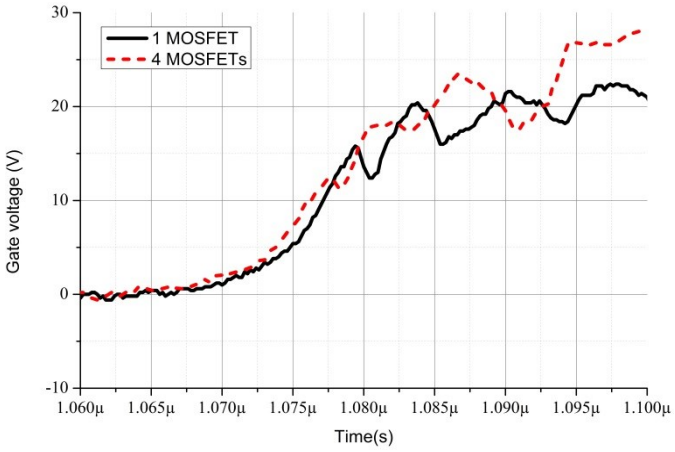
Figure 3.39(a) illustrates the gate voltage waveforms for a fixed gate current of 30A and varying number of parallel devices. As expected, the slew rate decreases as the number of devices increase. Therefore, higher gate current is required to improve switching with four parallel devices. Figure 3.39(b) compares the gate voltage for one MOSFET and four parallel driven MOSFETs. By increasing the gate current (by decreasing L), the switching speeds of the four MOSFETs can be matched to that of a single MOSFET.

3.7.4 High-voltage experiment

According to the design specifications, the pulsed power system must be capable of single shot and multi-pulse burst mode operation. Four MOSFETs were tested with the gate driver at a test voltage of 500V and a 10Ω load. The following subsections present the experimental waveforms for single shot, multi-pulse burst and variable pulse width operation.



(a)

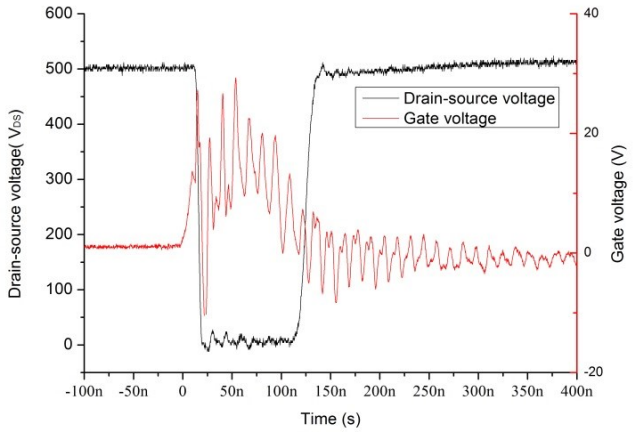


(b)

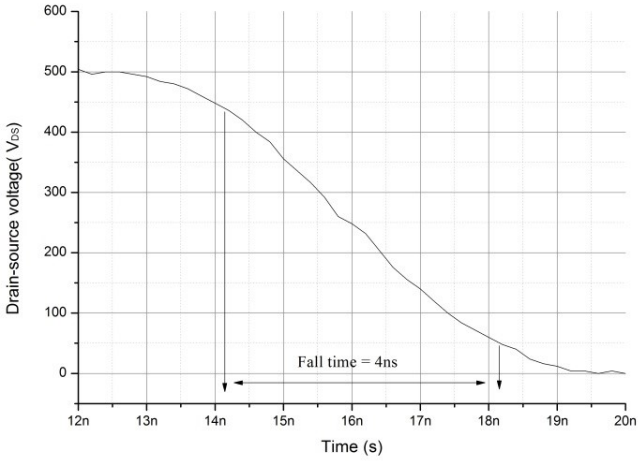
Figure 3.39: Gate voltage wave**forms (a) increasing number of devices and (b) matching switching speeds by increasing gate current.**

I. Single-shot experiment

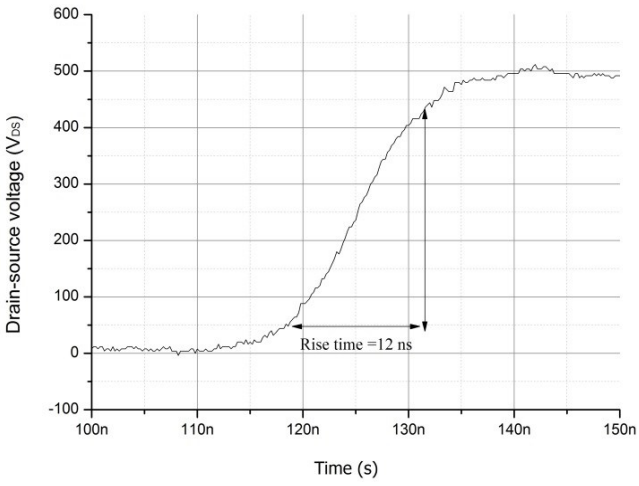
Figure 3.40 shows the gate voltage and drain-source voltage single-shot waveforms. Also shown is the expanded drain to source voltage fall and rise times. Pulse widths of 70ns with rise and fall times of 4ns and 12ns were measured across the four devices.



(a)



(b)



(c)

Figure 3.40: (a) Single shot V_{DS} & V_{GS} waveform, (b) V_{DS} fall time, and (c) V_{DS} rise time.

II. Multi-pulse experiment

Figure 3.41 shows the drain-source voltage waveform for multi-pulse operation. Pulse reproducibility at 400 kHz is demonstrated at 500V, 50A with ultra-fast switching times. The repetition rate is presently limited by the size and the charging time of the inductor. This can however be increased by using appropriate inductance and timing.

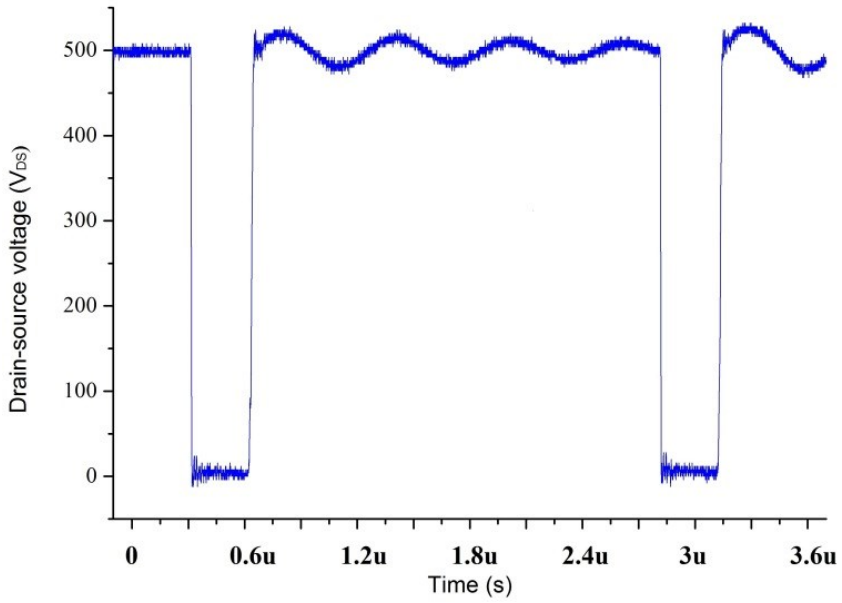


Figure 3.41: Multi-pulse switching waveforms of $V_{DS.}$

III. Variable pulse-widths experiment

The gate driver is flexible and can be used for various pulse widths. Figure 3.42 illustrates variable pulse widths between 70ns and 300ns.

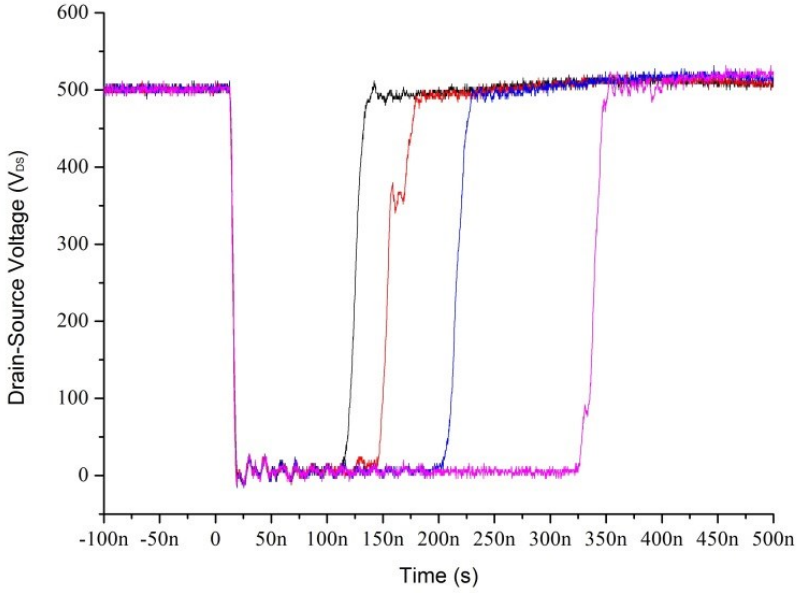


Figure 3.42: Switching waveform demonstration variable pulse widths.

3.8 Summary

A novel current source gate driver in the application area of pulsed power has been designed, analysed and experimentally verified for single-shot and multi-pulse burst mode. The analysis shows that with this topology, stray inductance has negligible effect on the pulse rise time. However, it is a key parameter affecting the MOSFET turn-off delay. This is more apparent in devices with higher gate capacitances. The analysis also demonstrates the driver's ability to switch multiple parallel connected MOSFETs synchronously without compromising switching speed. This is achieved by increasing the inductor current during the energising period.

Practical results demonstrate pulse rise and fall times of 4ns and 12ns respectively at a test voltage of 500V with a 10Ω resistive load. The results are based on the gate circuit driving four parallel MOSFETs with a total equivalent input capacitance of 22nF.

It is also shown that the intrinsic junction capacitance of TVS diodes increases significantly with power ratings. This results in an increase in the turn-on delay. Therefore, careful consideration must be given to the choice of protection diodes. This can be a limiting factor in the design performance. The performance of the gate driver sets a benchmark for the design of a pulsed power Linear Transformer Driver (LTD) which is discussed in the next chapter.

3.9 Proposed modifications to gate driver circuit for future research

In Chapter 3 during the analysis, it is identified that during turn-off, the gate driver dynamics are similar to that of a voltage source driver. The turn-off performance is thus limited due to the path inductance, resistance and the input gate capacitance. There is scope for improvement of the proposed gate drive circuit.

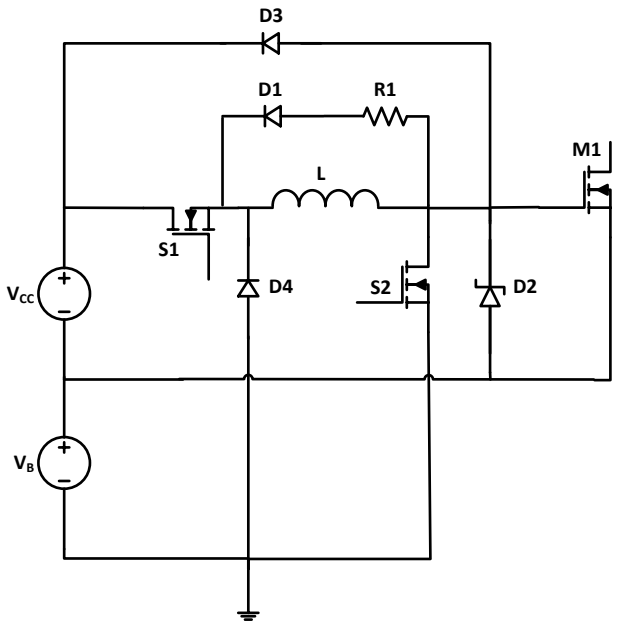


Figure 3.43: Proposed modified gate driver circuit.

Figure 3.43 shows the proposed modification to the gate driver circuit. The main modifications to the circuit are:

1) The addition of negative bias voltage and the connection of TVS between the gate of the power MOSFET and the circuit ground terminal,

2) Diodes D3 and D4 which facilitate the recovery of excess inductor energy when the gate voltage exceeds the input supply voltage.

Noise immunity will be improved with negative bias voltage. The feature of connecting the TVS diode from the gate-to-ground instead of conventionally being placed from gate-to-source terminals is that the gate voltage $V_{GS} = V_Z - V_B$, where V_Z is the TVS clamp voltage and V_B is the negative bias voltage. For example, an 18V TVS has a maximum clamping voltage V_Z of 31V at its peak operating current. With a negative bias voltage V_B of +7V applied to the gate driver circuit, the maximum gate-to-source voltage V_{GS} will be *(31-7=24V)*. This is better illustrated using the equivalent circuit shown in Figure 3.44.

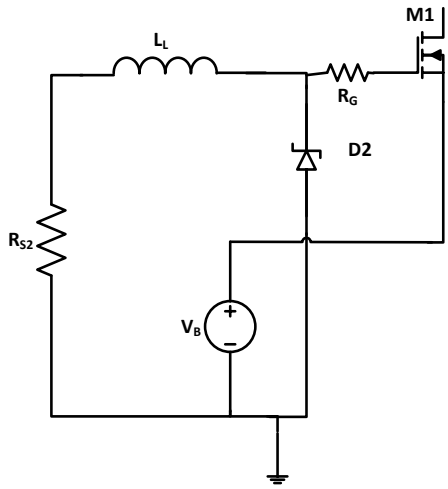


Figure 3.44: Equivalent circuit of the gate driver during turn-off.

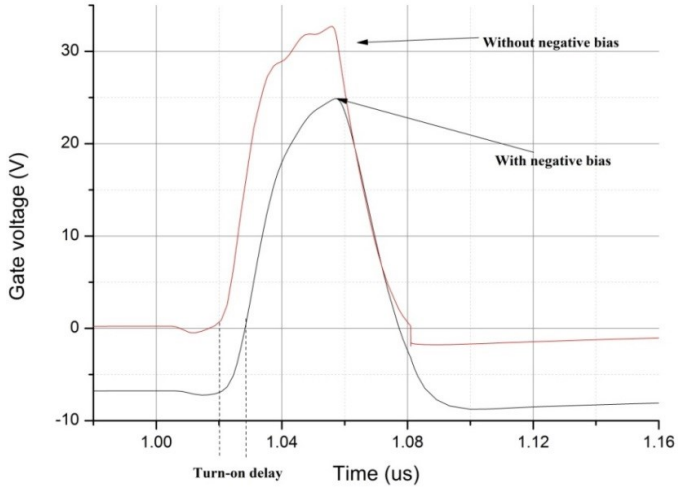


Figure 3.45: Simulated gate voltage waveforms with and without negative bias.

The trade-off with the negative voltage is the prolonged delay time at turn-on. The gate voltage must rise from the negative value to its threshold in comparison to the non-negative gate drive. This is illustrated in the simulated gate voltage waveforms in Figure 3.45. The energy recovery diodes are advantageous when operating the gate driver in repetitive pulse mode. Appropriate decoupling is required for effective voltage clamping using the energy recovery diodes.

References

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Chapter 4

Development of a Linear Transformer Driver

4.1 Introduction

Linear Transformer Driver (LTD) technology has enhanced pulsed power generation by providing high voltage output capability along with modularity, and a low inductance arrangement gives improved pulse shapes when using lower power sources. Chapter 2 surveyed the literature on power electronics based LTD and IVA systems. The demand for MOSFET based pulsed power system has significantly increased in the last decade. The LTD arrangement of MOSFETs has increased its capability to serve in low to medium-power systems. The associated complexity and increased number of components due to their lower power density, presently limits their applicability in high-power systems which can range up to several hundreds of megawatts. The gate driver design presented in Chapter 3 demonstrated rise and fall times of less than 10ns and its capability to drive multiple parallel connected MOSFETs at similar switching speeds. Using the high speed gate driver, larger and multiple power MOSFETs can be driven at high switching speeds. This technology therefore demonstrates the potential to reduce component count and increased power density per stack, which is favourable for developing higher power density pulse

generating systems suitable for future flash radiographic systems. The next step towards manipulating this technology is to develop an LTD system.

To develop an LTD system requires a pulse transformer design which is compatible with the proposed gate driver. A pulse transformer can be defined as a transformer designed specifically for handling voltage and current pulses with time durations in the order of sub-microseconds to several tens of microseconds.

The transformer is based on a basic principle that an applied time varying voltage V_P across the primary winding generates a magnetic field. The applied magnetic field drives the flux through the magnetic circuit path. The changing magnetic flux induces a voltage V_S in the secondary winding. Figure 4.1 shows the ideal transformer and its equivalent circuit. According to Faraday's law, an induced voltage is proportional to the rate of change of flux. The instantaneous voltage across the primary winding equals

$$V_P = N_1 \frac{d\phi_P}{dt} \tag{4.1}$$

Similarly, the voltage induced across the secondary equals

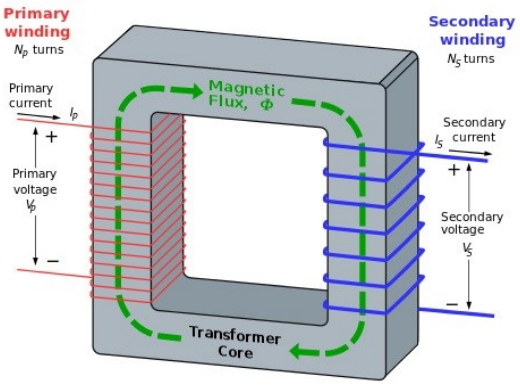
$$V_S = N_2 \frac{d\phi_S}{dt} \tag{4.2}$$

Where V_P is the voltage of the primary winding;

V_S is the voltage of the secondary winding;

N_1 *and* N_2 are the primary and secondary number of turns;

Φ_P *and* Φ_S are the primary and secondary magnetic fluxes.



(a)

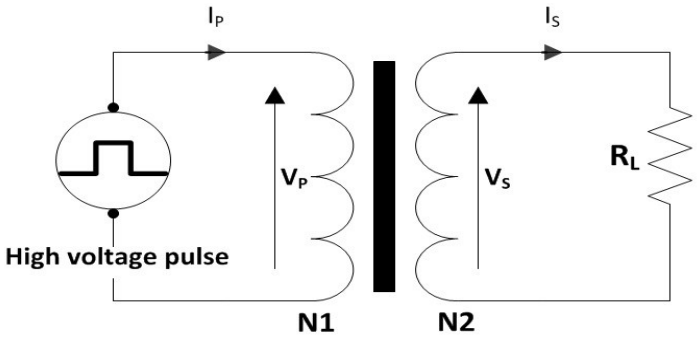


Figure 4.1: (a) Ideal transformer [1] and (b) ideal transformer equivalent circuit.

For a given magnetic core with a effective cross sectional area A_e, the magnetic flux density B_C is given by

$$B_C = \frac{\phi}{A_e} \tag{4.3}$$

where B_C is the maximum magnetic flux density of the core before it reaches saturation and the permeability of the material drops to that of an air core. Substituting (4.3) into (4.1) and (4.2) gives

$$V_P = N_1 A_e \frac{dB_C}{dt} \tag{4.4}$$

$$V_S = N_2 A_e \frac{dB_C}{dt} \tag{4.5}$$

The equations (4.4) and (4.5) imply that the available flux density limits the achievable pulse width at a given voltage. It also indicates that the voltage-time product is proportional to the number of winding turns. The output load voltage is the ratio of the primary and secondary turns which equals

$$V_S = \frac{N_2}{N_1} V_P \tag{4.6}$$

In contrast to conventional systems, modern pulsed power demands faster pulse switching times and the demand for the "ideal" rectangular pulse is constantly growing. The ideal transformer scenario applies where the flux induced by the primary winding ϕ_P is equal the flux experienced by the secondary winding ϕ_S. In this case with perfect coupling, no winding resistance, leakage inductance or parasitic capacitance, a rectangular pulse can be delivered to the load. In the context of flash radiography, faster pulse transitions lead to higher imaging quality at the required energy levels.

In practice, however, leakage reactance influences the pulse shape and achievable widths. The sources of leakage are poor magnetic flux coupling, stray wiring outside the transformer, and parasitic capacitance which exist within the transformer structure. In conventional high voltage transformers with large turn ratios, the output pulse rise time is limited by a combination of primary winding leakage inductance and secondary winding stray capacitance. [2].

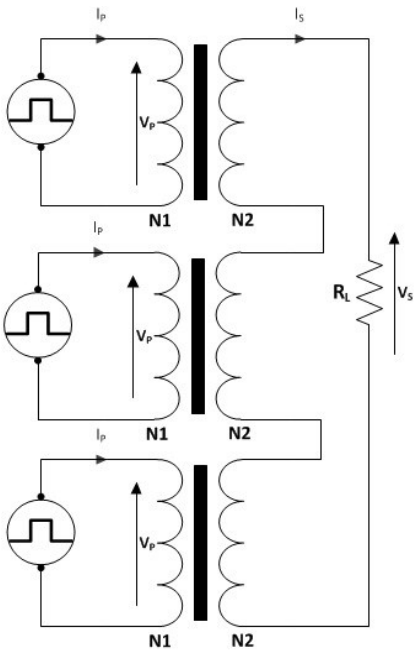


Figure 4.2: Linear Transformer Driver topology.

The Linear Transformer Driver (LTD) concept proposed in this research overcomes many major issues of the step-up pulse transformer circuit. The voltage adder topology essentially consists of switching modules each having the same circuit topology, as shown in Figure 4.2, in a low turn ratio configuration, usually 1:1. The secondary winding of each transformer is connected in series and the output load voltage is the sum of the outputs of each module.

This chapter investigates the design of a prototype LTD system for pulse widths of 100ns or less which are capable of single-shot and multi-pulse burst mode operation. The main objective is to establish pulse transformer action capable of achieving rise times less than 10ns, commensurate with a Linear Transformer Driver configuration using the proposed gate driver circuit.

Section 4.2 gives the background to the transformer model and its constituent elements. Section 4.3 characterises a useful transformer model based on the information presented in section 4.2. Section 4.4 discusses selection of the magnetic core for the application. In section 4.5, the sizing of the magnetic core and other components is considered. A prototype LTD system design is presented. Following this, section 4.6 presents the experimental results for a two-stage and a prototype four-stage LTD system for both single shot and multi-pulse burst mode operation. A system simulation model is presented in section 4.7 followed by discussion and a summary in section 4.8.

4.2 Transformer models

A standard equivalent circuit model for a pulse transformer is specified in the IEEE standards for pulse transformers [3]. This model is shown in Figure 4.3 and is more complex than the generic turn ratio controlled model of an ideal transformer.

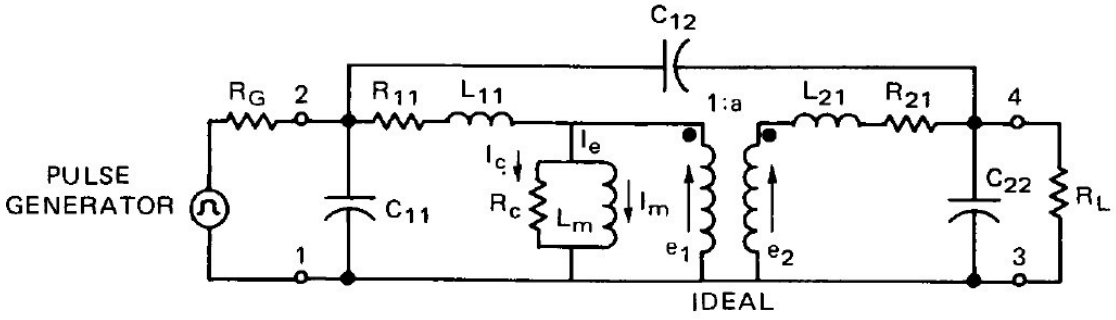


Figure 4.3: IEEE standards pulse transformer equivalent circuit [3].

The additional features which are shown in this model are the magnetising inductance L_m, leakage inductances L_{11}, L_{21}, core losses R_C, winding losses R_{11}, R_{21}, distributed capacitances C_{11}, C_{22} and coupling capacitance C_{12}.

4.2.1 Magnetising inductance

The ideal transformer model assumes a magnetic core with high permeability such that no current should flow in the primary winding when the secondary winding is open circuited. However, in reality the primary winding acts as an inductor wound on a core with finite permeability. This is the magnetising inductance which is represented as a shunt inductance in the equivalent circuit. The current used to magnetise the core is the magnetising current I_m. The magnetising inductance L_m is:

$$L_m = \frac{\mu_0 \mu_r N_1^2 A_e}{l_e} \tag{4.7}$$

where A_e is the effective cross sectional area of the core;

l_e is the effective path length of the core;

N_1 is the number of primary turns;

μ_r is the relative permeability of the core.

4.2.2 Leakage inductance

Leakage inductance is an indication of the number of primary flux lines which fail to couple to the secondary and vice versa. It is represented as an inductor in series with the transformer winding. The uncoupled inductance results in slower pulse edge transitions. Therefore, careful consideration has to be given during the design process to minimise this inductance.

4.2.3 Core losses

Core losses are shown in the IEEE standard transformer model as a shunt resistor R_C across the magnetising inductance L_m. This element is a result of the core's finite resistivity as well as the hysteresis losses in the material. The hysteresis losses are due to the B-H profiles of the core magnetization characteristics. The enclosed area in the magnetization curve is proportional to the energy lost over one cycle of the H field. So, the hysteresis losses are proportional to frequency as the loss is due to the procedure of magnetising and demagnetising each core. The core loss increases with core volume. The second type of core loss is the eddy current loss. The changing magnetic flux in the core induces eddy currents. At higher frequencies, the eddy current losses are dominant and result in higher power dissipation in the core. Selection of core material and lamination thickness play key roles in reducing these losses.

4.2.4 Parasitic capacitances

Parasitic capacitances exist between any two charge carrying conductors. Similarly in a transformer, capacitances exist between the turns of each winding as well as between the primary and secondary windings. Leakage inductance and parasitic capacitances influence each other. Increasing the separation distance between two windings decreases the parasitic capacitance. However, it leads to an increase in the leakage inductance and vice versa. Therefore, there is generally a trade-off during the design, where a compromise between leakage inductance and parasitic capacitance has to be established.

4.3 Forming a useful transformer model

Use of the full equivalent circuit is not always necessary and the circuit can be simplified for different operating conditions. For the analysis of the pulse transformer for short duration pulses with pulse widths of less than 100ns, the loss elements (shunt resistance R_C) can be ignored. It is assumed that a high permeability material and core size is chosen such that, the magnetising inductance L_m is significantly higher such that negligible amount magnetising current is flowing through the winding. The input current can be assumed to be effectively diverted into the load resistance R_L. The magnetising inductance L_m is therefore ignored during this period. In a 1:1 ratio LTD configuration, wide conductor casing is used which encloses the volume of the core. The effective series resistances R_{11} and R_{21} are therefore ignored. Figure 4.4 shows the simplified equivalent circuit which is applicable in short pulse conditions.

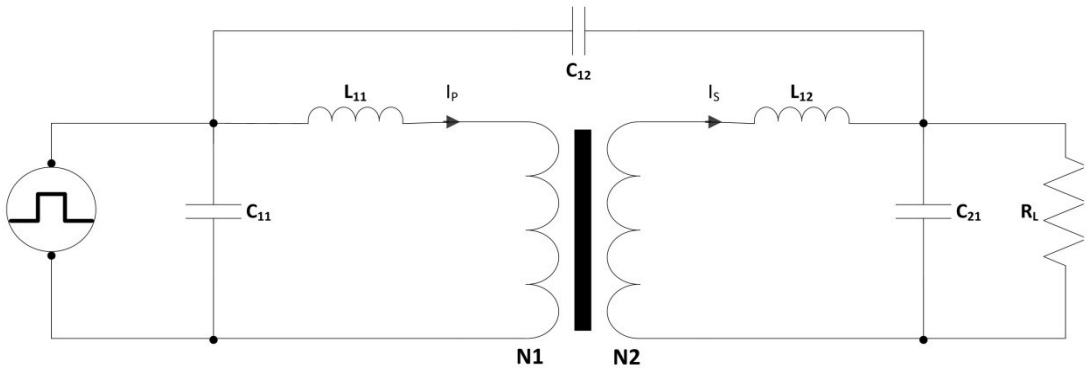


Figure 4.4: Simplified transformer equivalent circuit for short pulses.

4.4 Magnetic core considerations

The main function of a magnetic core in an LTD system is to provide galvanic isolation such that each individual pulse generator module can be grounded

in the voltage summing process [4]. The following subsections cover some of the considerations when selecting a core.

4.4.1 Core geometry

There are a number of possible choices for the core geometry in a transformer. However, the toroidal geometry is the preferred choice for the magnetic core in an LTD system. The shape enables the stacking of the power and switching components around the core to provide symmetrical high dv/dt switching. Other advantages of the toroid core are a well-defined flux path and low stray magnetic fields [5].

4.4.2 Material

The core in a pulsed power system should present relatively high impedance to the drive system such that the power from the MOSFET based pulsed power generator flows primarily into the load and not into the core magnetising region. The electromagnetic properties of a magnetic core are complicated to describe and to model. Their response is non-linear, exhibiting hysteresis and, rate dependent, as illustrated with the sample B-H curve shown in Figure 4.5.

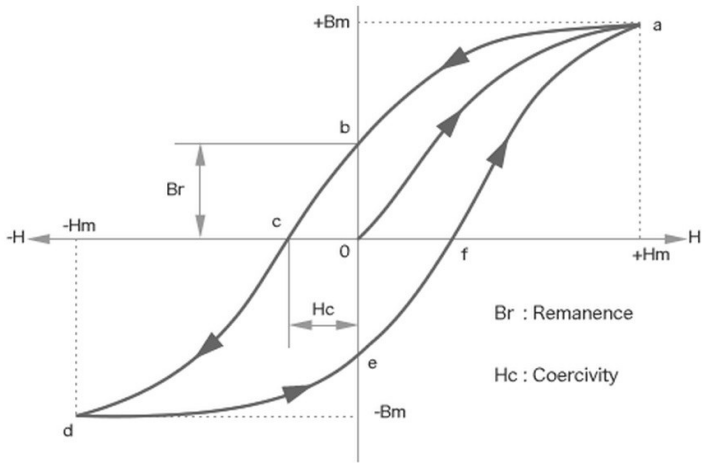


Figure 4.5: Illustration of a Non-linear B-H curve for a typical magnetic core going from saturation at $-B_m$ to saturation at $+B_m$. The trajectory depends on the applied magnetic field strength. The area within the loop represents hysteresis, adapted from [6]. B_r is the remnant flux density of the core.

From equation (4.5)

$$V_P = N_1 A_e \frac{dB}{dt} \tag{4.8}$$

Assuming that the core is reset to $-B_m$ the core demagnetises to $-B_r$. The total flux swing dB available is between $-B_r$ to $+B_m$. The main constraint on the choice of the magnetic material and the required volume of material depends on the requirement of the "voltage-time" product. Generally, a material with a high permeability would ensure that the magnetising inductance is sufficiently high such that a majority of the pulse generator power is delivered to the load. The second factor that influences the choice of material is maximum flux density. LTD systems, especially, operate in a 1:1 ratio single turn winding configuration. This means that the voltage per turn is much higher and the rate of change of flux is much quicker resulting in earlier core

saturation. Therefore, a material with a total flux swing ΔB higher than the product of the total pulse voltage and pulse length must be satisfied.

4.4.3 Core selection

Presently, ferrites and nanocrystalline cores are of particular interest in high frequency pulsed power systems [6]. Table 4.1 shows a comparison between a typical ferrite 4C65 (Ni-Zn) core and a nanocrystalline NANOPERM (Magnetec) core.

Table 4.1: Magnetic core characteristics.

	4C65 (Ni-Zn)	**Nanoperm (Fe(SiB))**
μ_i	125	30,000
B_{sat} (T)	0.38 T	1.2 T
ρ (Ω-m)	10^5	1.15 x 10^2

The advantage of a nanocrystalline core is its higher saturation flux density. The higher flux swing results in a reduction in the overall size of the transformer. Ferrites have the disadvantage of the lower saturation flux density, which translates to a larger system size to sustain a similar pulse stream.

Eddy current losses are significant at high frequencies of the order of hundreds of kilohertz. They are a result of the induced voltage due to the change in flux in the core. The resulting circulating current i_{eddy} causes heating of the core. The magnitude of the eddy current is limited by the path resistance R_{path} or the resistivity of the core ρ. Eddy current loss P_E can be estimated using an empirical equation [7] given by

$$P_E = \frac{\pi^2 f^2 B_m{}^2 \tau^2}{6\rho} \tag{4.9}$$

Here, f is the switching frequency, B_m is the maximum operating flux, τ is the material thickness, and ρ is the resistivity of the material. The equation indicates that the eddy current loss is directly proportional to the square of the switching frequency and inversely proportional to the resistivity of the magnetic core. By increasing the resistivity of the material, the eddy current losses can be reduced. Nickel-Zinc ferrites achieve this due to their significantly higher resistivity in comparison to other commonly used ferrites. For example, a typical Mn-Zn ferrite (3F45) has a resistivity of 10 Ω-m compared to Ni-Zn ferrite (4C65) with a resistivity of 10^5Ω-m. Due to its lower resistivity, 3F45 material is susceptible to higher eddy current losses at higher frequencies.

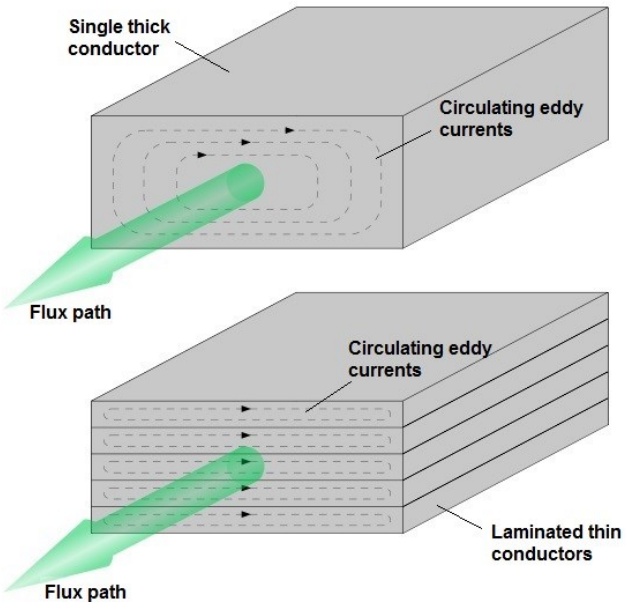


Figure 4.6: Diagram comparing the eddy currents in a thick conductor and in thin laminated conductor sheets. The current is distributed in the laminated sheets resulting in lower losses.

Equation 4.9 also indicates that the eddy current loss is directly proportional to the square of the thickness of the magnetic core. Figure 4.6 shows a diagram comparing the eddy currents between a thick conductor and thin laminated conductors. Nanocrystalline cores are manufactured as laminated sheets with different thicknesses. These laminations are electrically isolated and rolled into a core shape. In Figure 4.6, the distributed current circulates within the thin laminated structures resulting in significantly lower eddy current losses. For example Nanoperm, Metglas 2605SA1, and Metglas 2705M are manufactured as laminations with thicknesses of 17μm, 21μm and 22μm respectively. With increasing frequency, the skin depth decreases. Therefore, a Nanoperm core would have the lowest eddy current loss, compared to the Metglas cores due to its lower thickness.

4.5 Development of a prototype LTD system

This section describes the development of a prototype LTD system. The subsections individually look at the pulse transformer sizing, the module design and the experimental setup. Table 4.2 highlights the design specifications for a single LTD stage.

4.5.1 Determining core size

Based on the discussion in section 4.4, the characteristics of Ferrite (4C65) and nanocrystalline (Nanoperm) were considered during the selection process of the core size. The total "volt-second" product required by the core to sustain a stream of two pulses is:

$$V_C\, t = 2 \times 600 \times 80 \times 10^{-9} = 0.096 \times 10^{-3}\,\text{Vs} \qquad (4.10)$$

Table 4.2: Design specifications for a single LTD stage.

Input voltage	0-600V
Output voltage	0-600V
Load	11 Ω
Total load current	200 A
Pulse width	80ns
Pulse rise time	< 10ns
Pulse fall time	< 20ns
No. of pulses	Single
Droop voltage	10V

Assuming the maximum flux swing available after core reset ΔB= 0.7T for material 4C65, the minimum core area required to sustain the pulse stream can be calculated using equation (4.8). By substituting values for V_C, t, N and ΔB:

$$A_E = \frac{V_C t}{N \Delta B} = \frac{0.096 \times 10^{-3}}{1 \times 0.7} = 1.37 cm^2 \tag{4.11}$$

Similarly, assuming the maximum flux swing available after core reset ΔB= 1.2T for material Nanoperm, the minimum core area required is:

$$A_E = \frac{V_C t}{N \Delta B} = \frac{0.096 \times 10^{-3}}{1 \times 1.2} = 0.8 cm^2 \tag{4.12}$$

Comparing (4.11) and (4.12), the system size can be reduced by a factor of 1.7 when using a nanocrystalline core. Due to the significant achievable reduction in size, the Nanoperm core was selected. A toroid core with dimensions of 63mm x 50mm x 20mm and an effective core area of A_E 0.95 cm^2 was chosen.

Nanoperm cores are available with two different characteristics, having different values of permeability. Figure 4.7 shows the hysteresis curve for Nanoperm with the two different characteristics. For annotation, the materials with relative permeability of 30,000 and 80,000 will be addressed as Material 1 and Material 2 respectively. Comparing the two curves, the magnetic memory of Material 2 is more than that of Material 1.When a material with a stronger magnetic memory is reset to the negative axis, it enables a higher flux swing from $-B_r$ *to* $+B_s$. It is also obvious that the hysteresis loss in material 2 is higher and more energy is required to reset the core. Material 1 has a less steep curve and saturates at a higher magnetic field strength. It has a weak magnetic memory and the hysteresis losses are lower, making it more suitable for higher frequency applications. The disadvantage is that the maximum flux swing available after a full reset is limited to $0\text{-}B_S$, as opposed to $-B_r$ *to* $+B_s$ for a material with a square B-H loop.

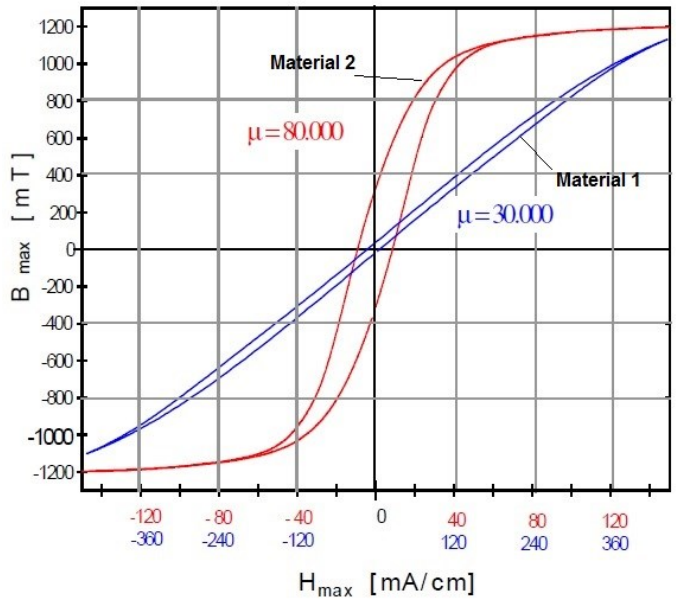


Figure 4.7: Hysteresis curve of Nanoperm core [8].

Table 4.3 highlights the advantages and disadvantages of materials 1 and 2. There is no significant advantage is using Material 2. Therefore, a core based on Material 1 was chosen for the application.

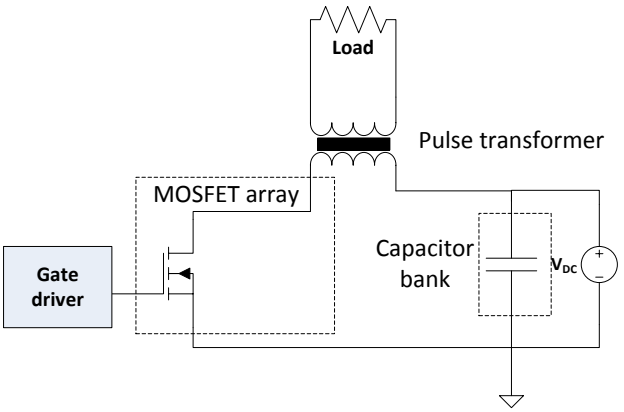
Table 4.3: Characteristics of Material 1 and Material 2.

	Advantage	**Disadvantage**
Material 1 (μ=30,000)	Low hysteresis loss High frequency operation Higher B_S	Flux swing after reset is approx. 0-B_S Larger core maybe required for wider pulse width operation Lower permeability
Material 2 (μ=80,000)	Higher permeability Higher flux swing $-B_r$ to B_S	Higher hysteresis losses Lower B_S

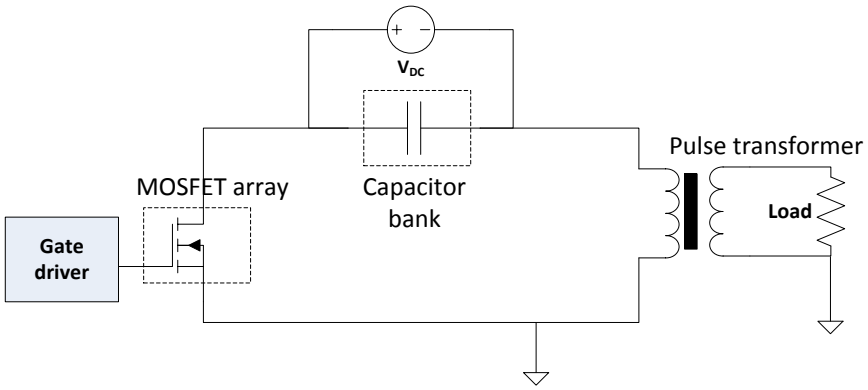
4.5.2 Module design

Two circuit topologies were investigated. Figures 4.8(a) and 4.8(b) show the schematic of the power side circuit of the pulsed transformer module using the two different topologies. For simplicity, the two topologies are named setup 1 and setup 2 respectively.

Setup 1 corresponds to the conventional arrangement of the capacitor bank, transformer, and the switching devices. The output of this arrangement is a positive output pulse. The disadvantage of this arrangement in an LTD system is that no part of the transformer winding is referenced to ground. During the stacking of each stage, achieving a shorter loop of the secondary stalk around the whole system becomes difficult and thus limits performance.



(a)

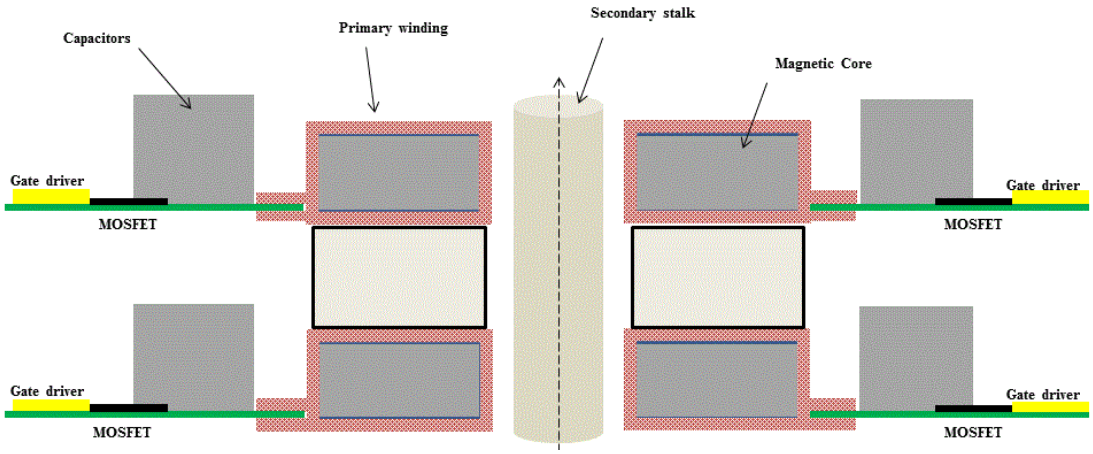


(b)

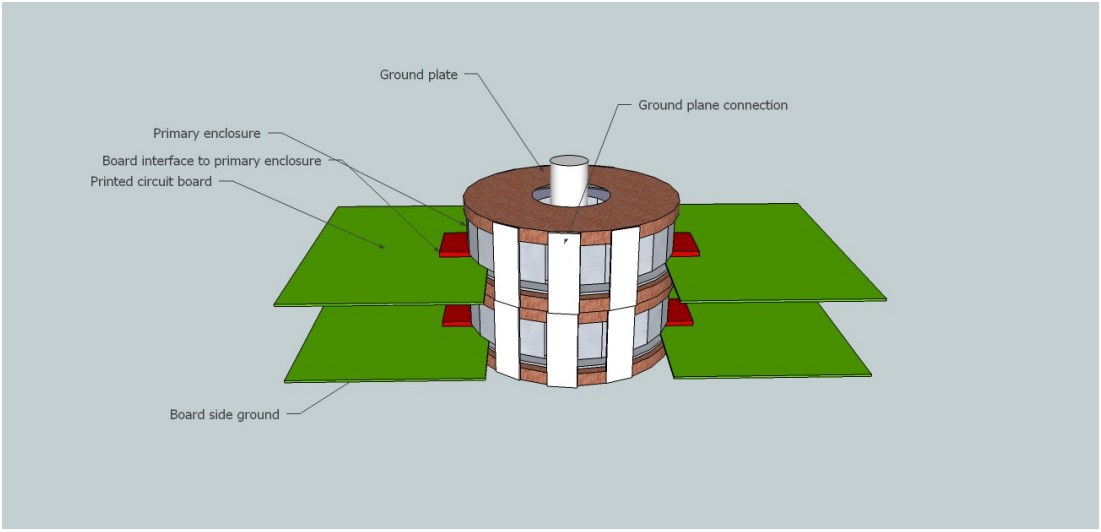
Figure 4.8: Schematic of (a) Setup 1 and (b) Setup 2.

Setup 2 is a modified arrangement where the one end of the transformer winding is referenced to ground. In this arrangement, the polarity of the capacitor is inverted and the high voltage power supply is at a floating potential. The output pulse in this arrangement is of negative polarity. The polarity of the output pulse can be changed by grounding either end of the secondary stalk. The advantage of this topology is easier layout and a significant reduction in the current loop formed by the secondary stalk. This topology was therefore chosen for the proposed design. The cylindrical shape of the LTD, with the centre secondary stalk acting as the inner conductor and outer cylinder being at ground potential, resembles a coaxial geometry

with impedance that can be changed by adjusting the stalk radius with respect to the outer cylinder radius [9]. A lengthy LTD system is in effect a transmission line and therefore, the stalk impedance has to be adjusted for impedance matching in order to achieve optimum pulse shape.



(a)



(b)

Figure 4.9: (a) Cross-sectional view diagram of the LTD module and (b) CAD model of the LTD module.

Figure 4.9(a) shows a cross sectional view of the proposed two stage LTD module. The diagram illustrates four driver boards with their respective array of MOSFETs and capacitors slotting into the magnetic core windings. A metallic housing completely encloses the toroid to form a single turn winding and affords low primary leakage inductance. The wide conducting paths facilitate the switching of high currents at high frequency with relatively lower inductance. The enclosure has one slot on either side of the core for the connection of the driver boards. The secondary is an aluminium rod which runs through the centre of the core with sufficient insulation spacing which is calculated based on the total output voltage. Figure 4.9(b) shows a CAD model of a two stage LTD system. In addition to the components shown in figure 4.9(a), the CAD model incorporates the outer ground cylindrical structure. The central stalk is connected to an aluminium disc at the bottom of the LTD system, which is at ground potential. Strips of copper are used to connect the bottom disc to the top disc, hereby creating a coaxial structure with low loop inductance. The resistive load is connected between the top of the central stalk and the top disc in a circular pattern for symmetrical distribution of inductance. An additional aluminium disc is inserted in the space between the two stages in order to facilitate a shorter average loop area for current flow.

In order to develop a compact LTD system, the gate driver board needs to complement a smaller LTD structure. The height of each modular stack will affect the size of the overall system. The height of each stack is restricted by two main components: 1) the magnetic core and 2) the capacitor bank. Generally speaking, nanocrystalline cores can be manufactured to various thicknesses. A higher volts/cm can be achieved by using thinner cores with an equivalent core area, A_E. However,

for this experiment a magnetic core with a thickness of 20mm was used due to its availability. Capacitor sizing increases with the power requirement. As the power rating increases, the minimum stack height is limited by the capacitor bank. For this specific application based on the design parameters in Table 4.2, the capacitance per stack can be calculated to be 3.2μF using the following empirical equation

$$C = \frac{i_L \Delta t_{pulse}}{\Delta V} \tag{4.13}$$

Here, C is the bulk capacitance, i_L is the load current, Δt_{pulse} is the pulse duration and ΔV is the acceptable voltage droop during the pulse. Several capacitor types were investigated including MKP and ceramic. The following section presents the experimental results for the LTD setup.

4.6 Experimental results

Figure 4.10 shows the block schematic of the LTD circuit. Two setups are described in this section. The first (Setup 1) is a two stage LTD to verify the working concept of the LTD. The second (Setup 2) is a four stage prototype LTD system. The latter uses four parallel connected MOSFETs per driver board.

4.6.1 Experimental setup 1

Figure 4.11 shows experimental Setup 1. The gate driver board layout is modified to be compatible with the LTD structure. The board slots into the gap between either ends of the winding and the copper strips come in contact with the top and bottom copper of the circuit board. In this setup two MKP capacitors are used in parallel between the MOSFETs and the top winding. Polypropylene Films (MKP)

use layers of metal and polypropylene dielectric films offering a higher breakdown voltage than polyester, and thus more suitable for high voltage applications such as switching power supplies. They also have low loss factors and good capacitance stability making them a good choice for high frequency applications. The main disadvantages are slightly higher cost and larger physical sizes over other film dielectric capacitors.

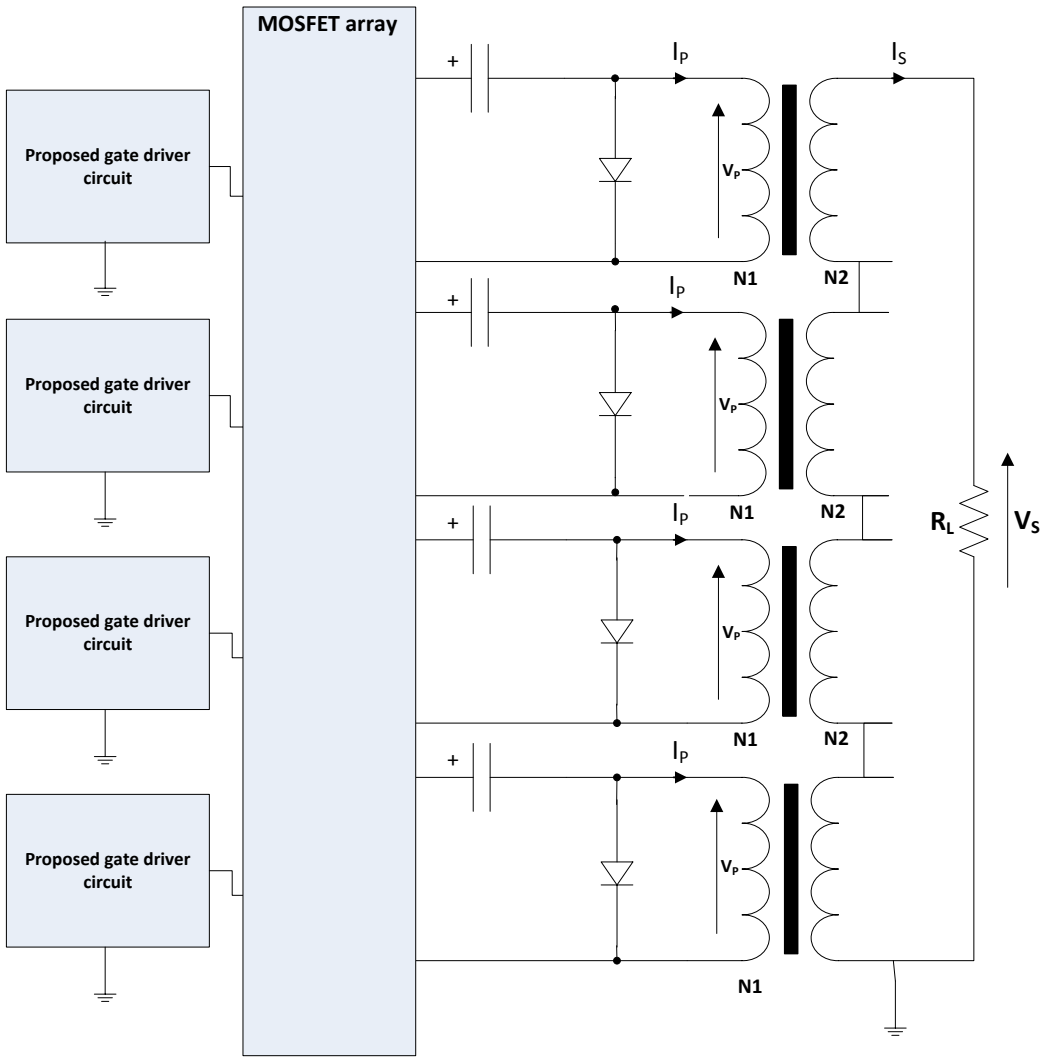


Figure 4.10: Block schematic of the proposed LTD system.

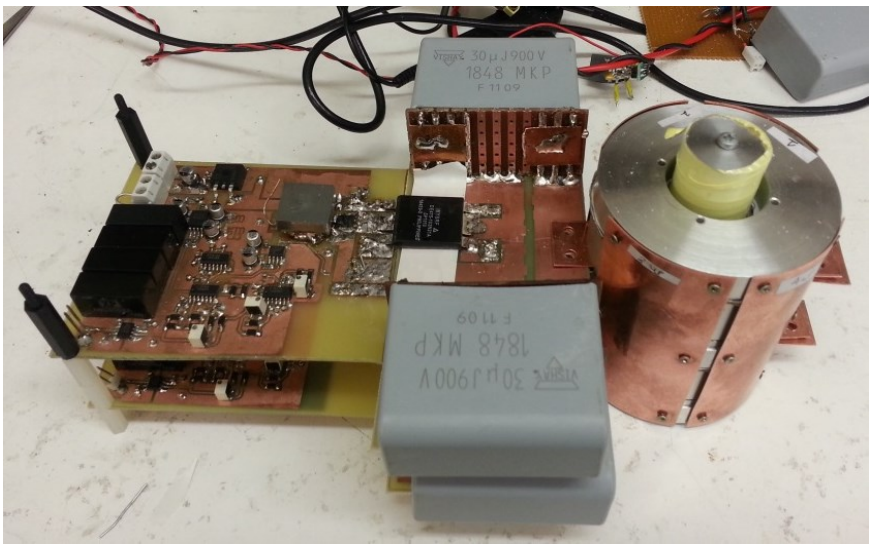


Figure 4.11: Experimental Setup 1.

One MOSFET is symmetrically mounted on each side of the board with vias connecting the gate, drain and source pins. The diameter and height of the transformer structure are 71mm and 75mm respectively. The diameter of the inner rod is 24mm. The output load is two 22Ω MELF high voltage resistors which are connected in parallel between the inner rod and the grounded aluminium disc on the top. Table 4.4 highlights the test specifications.

Table 4.4: Test specifications for Setup 1.

Input voltage	0-600 V
Output voltage per stage	0-600 V
Load	11 Ω
No. of stages	2
Total load current	100 A
Pulse width	80ns
Pulse rise time	< 10ns
Pulse fall time	< 20ns
No. of pulses	Single

I. Results

Figure 4.12 shows the load voltage waveform with a single powered stage across the load for an input voltage range between 100-400V. With a single stage, the output is thus between 100-400V.

Figure 4.13 shows the load voltage waveforms with two powered stages and an input voltage range of 100-600V. The output of each power stage is thus inductively added to give a total output voltage in the range of 200V to 1150V. The load current is approximately 104A at an output voltage of 1150V.

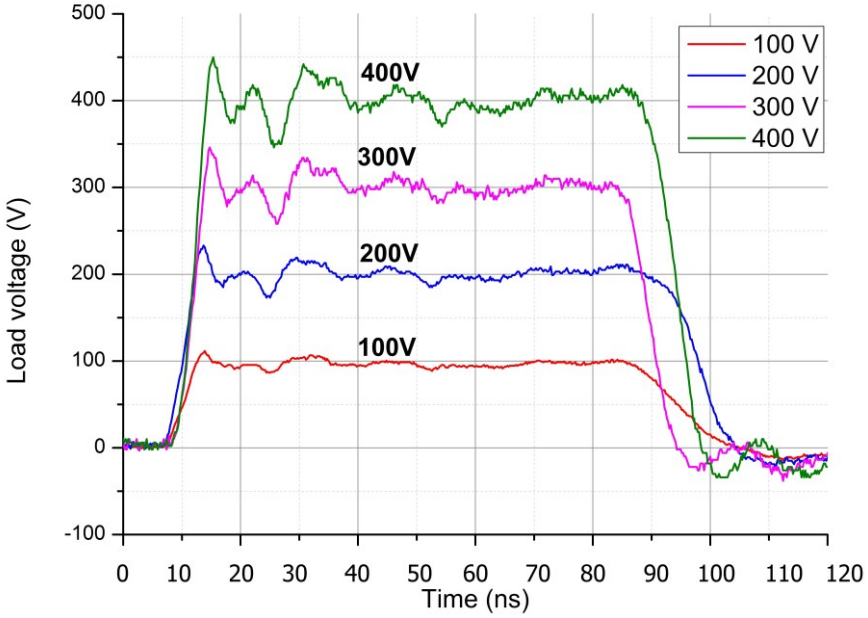


Figure 4.12: Single stage output load voltage waveforms for variable input voltage.

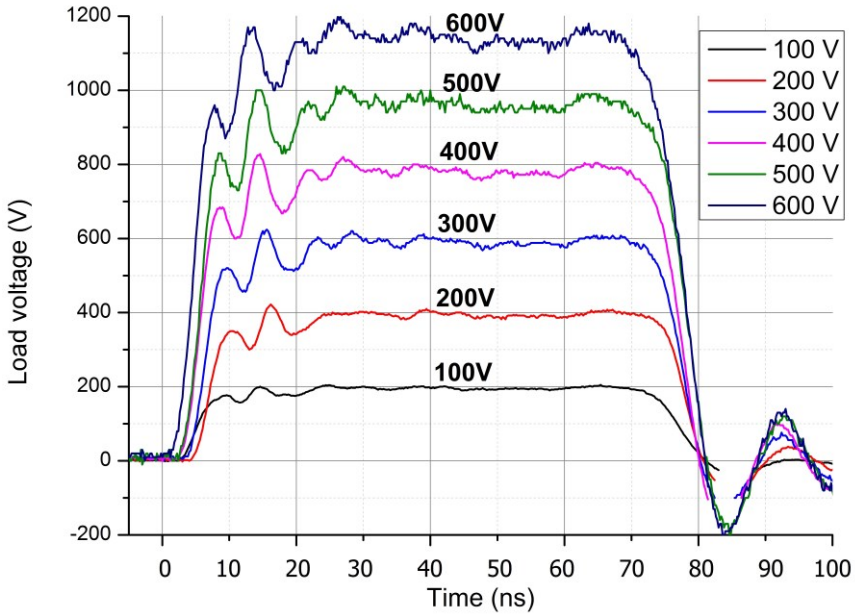
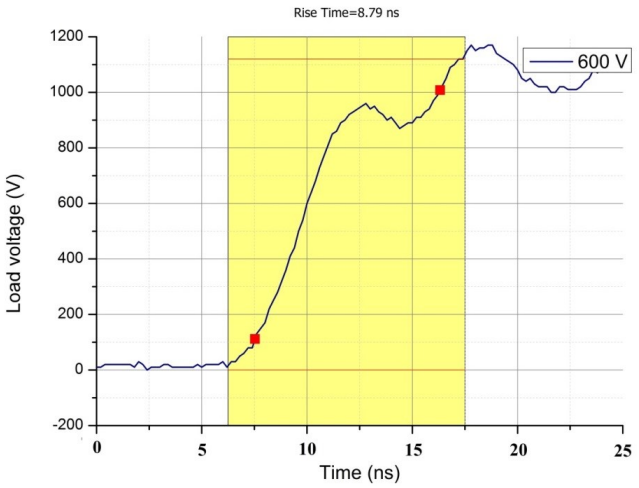
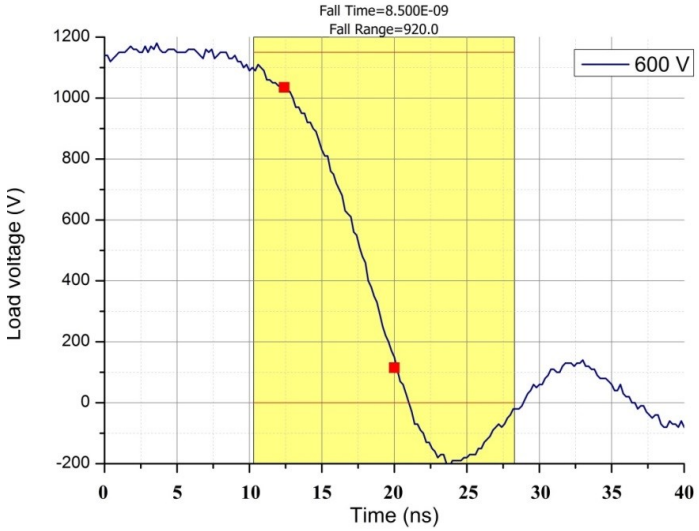


Figure 4.13: Two stage output load voltage waveforms for variable input voltage.

Figures 4.14(a) and 4.14(b) show rise (10% - 90%) and fall (90% -10%) times of the output voltage for the two stages operating at 600V. The flat top width of the pulse is 65ns. The full width at half maximum (FWHM) is measured to be approximately 75ns. The measured rise and fall times are 8.79ns and 8.5ns respectively. The 0-900V rising transient is significantly faster and takes approximately 5ns before the ripple is observed. This is associated with the leakage inductance of the test circuit. This is further discussed in section 4.7.



(a)



(b)

Figure 4.14: Two stage load voltage waveform (a) pulse rise time with 600V input, (b) pulse fall time with 600V input.

II. Discussion

Experimental setup 1 verifies the concept of an LTD using power MOSFETs. A two stage LTD setup achieved a 2x multiplication to the input voltage. Rise and fall times of less than 10ns were demonstrated which signifies its compatibility with

the design conditions for the pulsed power system. A total output voltage of 1.15kV and an instantaneous output power of 120kW are demonstrated. Due to the high di/dt transitions, small parasitic inductances have a significant effect on the pulse rise and fall times. The LTD design extensively minimises the leakage inductance. Furthermore reduction in the inductance requires the use of several MOSFETs in parallel surrounding the core to provide distributed path inductance.

Physically, the experimental setup has a height of 35mm per stack. This is dictated by the size of the MKP capacitors. The voltage to height ratio for an LTD system is stated in volts per centimetre which gives an indication of the power density and the compactness of the system. The ratio for experimental setup 1 is measured to be approximately 160V/cm.

The experiment provides a benchmark for the improvement of the proposed LTD system in terms of improving the output pulse response by reducing the path inductance as well as improving the design to increase the voltage to height ratio of the pulsed power system. The following section describes the results for a four stage LTD system.

4.6.2 Experimental setup 2

Figures 4.15(a) and 4.15(b) show the modified experimental setup 2. In this setup, four MOSFETs are used in parallel per gate driver board. Two MOSFETs are mounted next to each other symmetrically on either side of the board with their gate, drain and source terminals connected using vias.

(a)

(b)

Figure 4.15: Experimental setup 2; (a) top view and (b) side view.

The large MKP capacitors are replaced with 1kV, 100nF ceramic capacitors which are significantly smaller in size. Thirty two capacitors are connected in parallel per board to give an equivalent capacitance of 3.2μF. The minimum height of each stack is thus limited by the height of the toroid core, which is 20mm. The arrangement has four driver boards connected in an LTD configuration. A TTi 40MHz function generator is used to generate the input signals for the four boards. Four equal length

mini coaxial wires are used to connect to the input of each board. Two 11Ω resistors are connected in parallel between the inner stalk and the ground disc on the top. A low inductance arrangement is thus facilitated. Table 4.5 highlights the test specifications.

Table 4.5: Test specifications for experimental setup 2.

Input voltage	0-600V
Output voltage per stage	0-600V
Load	11Ω
Number of stages	4
Total load current	200A
Pulse width	80ns
Pulse rise time	< 10ns
Pulse fall time	< 20ns
No. of pulses	Single, 2 pulse burst mode

I. Module synchronisation

An increasing number of LTD stages accentuate the effect of propagation delays within each driver board, which can result in poorly synchronised pulses. This can affect the rising and falling edges of the output pulse. To compensate for these delays, a potentiometer is used to adjust the rising and falling pulse edges and synchronise the pulse adder stages. Figure 4.16 shows the gate voltage waveforms for the four stages. With the existing pulse generation circuit, the gate signals are synchronised to an accuracy of ±3ns.

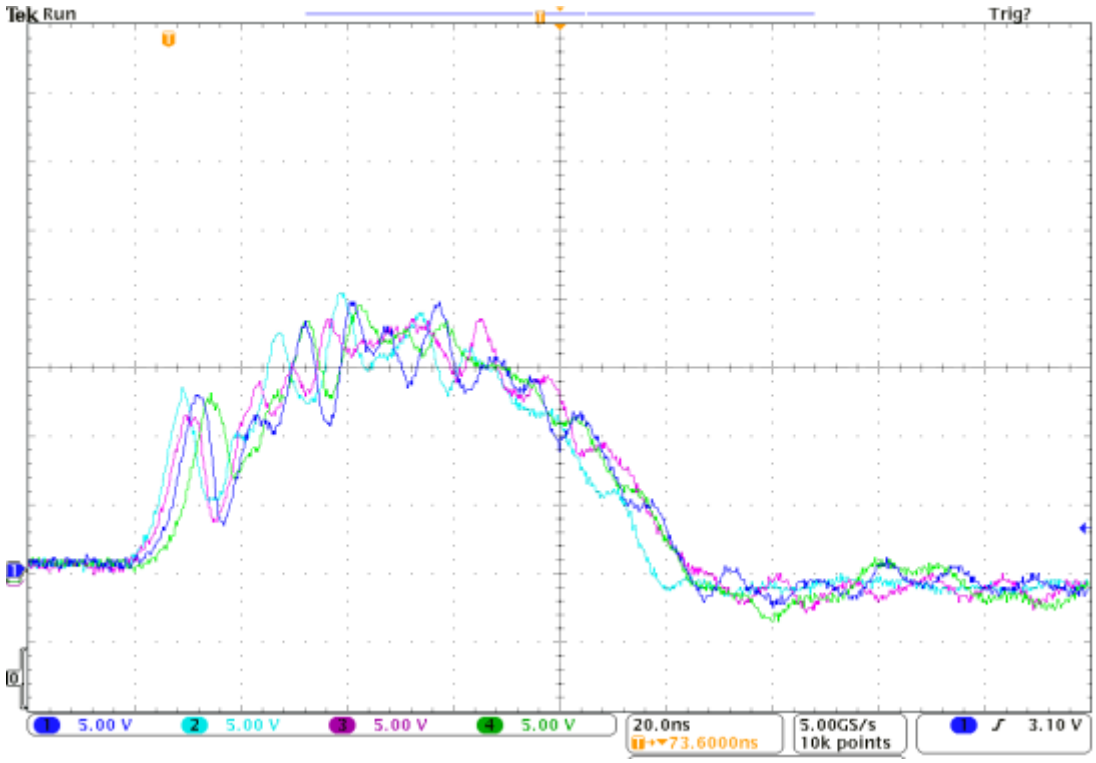


Figure 4.16: Gate voltage waveforms showing the synchronization of the four gate driver boards.

II. Results

This section presents the results for experimental setup 2. Three results are presented, 1) single-shot operation, 2) multi-pulse with a burst mode of 100 kHz, 3) multi pulse with a burst mode of 250kHz for varying input voltage between 150V and 550V.

(a) Single shot experiment

The function generator was set up for single-shot operation. Figure 4.17 shows the output load voltage waveform across the secondary stalk for varying input voltage between 150V-550V. As expected with a four stage voltage adder configuration the output voltage is measured to be between 600V and 2.1kV.

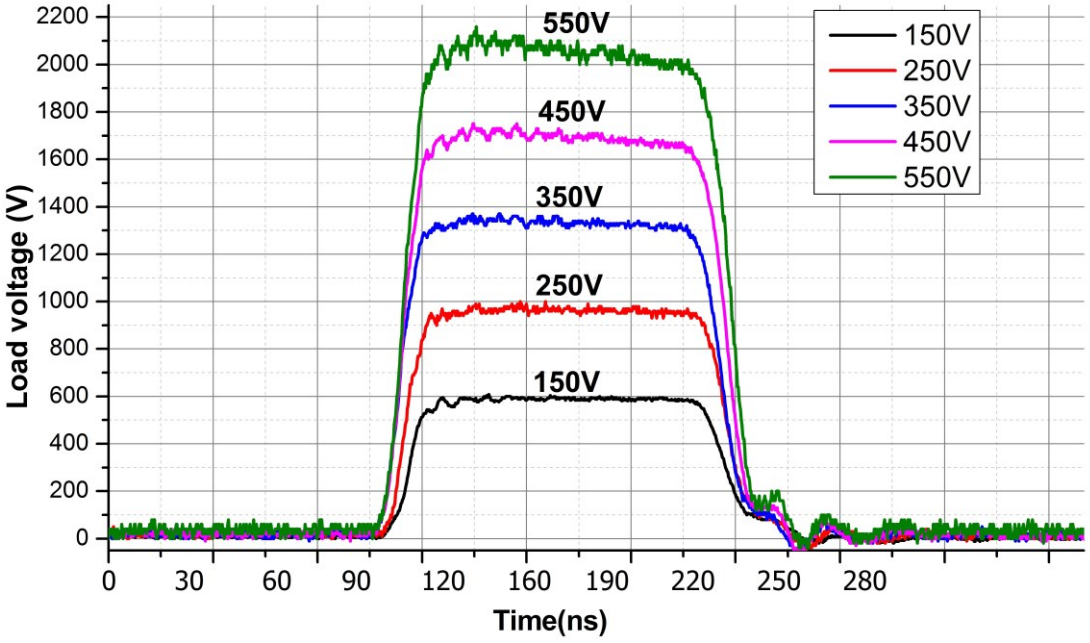
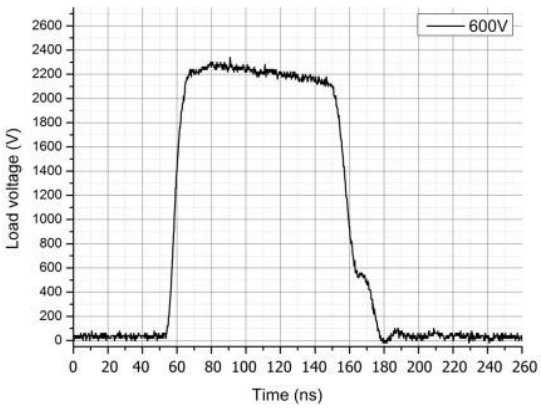
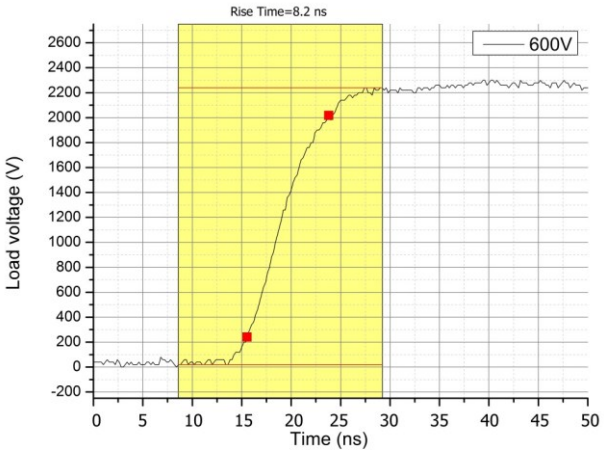


Figure 4.17: Four stage output load voltage waveform for varying input voltages.

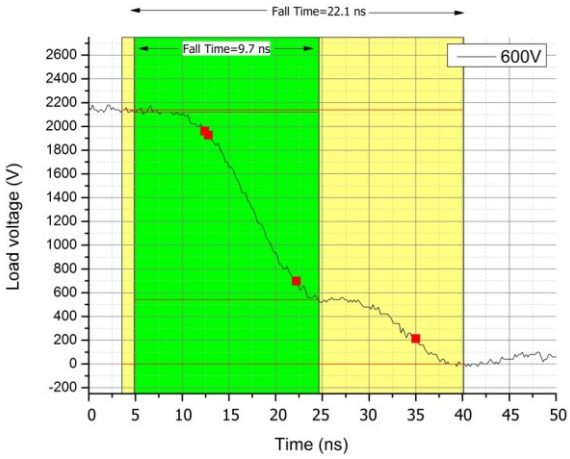
Figures 4.18(a) to 4.18(c) show the output pulse, pulse rise and pulse fall times respectively for an input voltage of 600V. The total output voltage is 2.25kV. The load current is approximately 200A. The flat top pulse width is 80ns and the Full Width at Half Maximum (FWHM) is 100ns. The droop voltage is approximately 40V which corresponds to the estimated capacitor voltage drop of ~ 10V per stage. The rise and fall times are measured to be 8.2ns and 22.1ns. The slower fall time can be associated with the delay in the turn off for one stage. This is clearly observed on Figure 4.18(c), where a single stage drops from 600 V to 0V after a ~8ns delay. Prior to this delay, the fall time between 2.25kV and 600V is measured to be 9.7ns which indicates that the fall time will be within the design specifications if synchronisation of the fourth board is improved. The expected output voltage with zero loss at 600V is 2.4kV. The voltage drop across the system is approximately 160V.



(a)



(b)



(c)

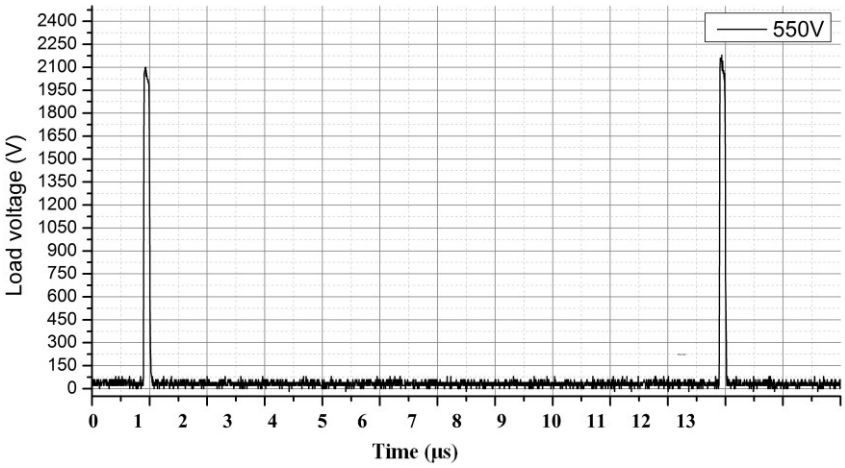
Figure 4.18: Four stage output load voltage waveform with 600V input (a) full pulse, (b) pulse rise time, and (c) pulse fall time.

The on-state resistance of each MOSFET is ~0.41Ω. The total on-state resistance per stage with four MOSFETs is ~0.1Ω which amounts to a voltage drop of 20V at a load current of 200A. The total voltage drop across the four stages is ~80V. The remaining 80V voltage drop can be attributed to the losses within the transformer and the secondary impedance.

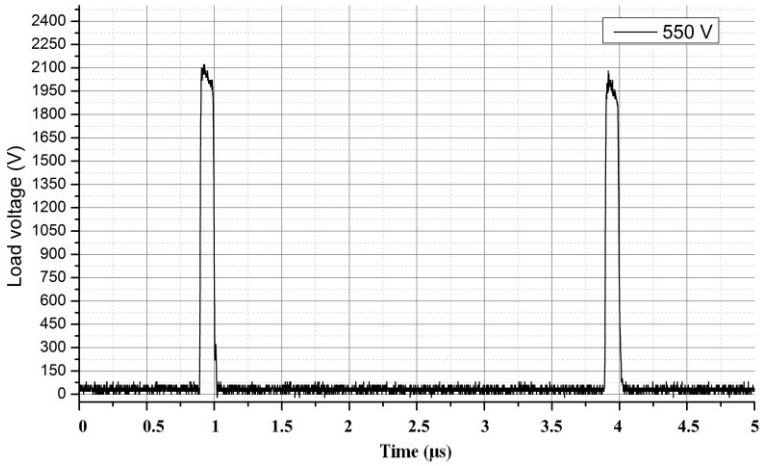
(b) Multi pulse experiment

One of the highlights of a MOSFET based pulsed power system is its ability to deliver multiple repetitive pulses at various frequencies to suit the needs of the application. Conventional large pulsed power systems are single-shot operated. When multi-shot experiments are required, multi-axis systems are used to deliver the separate pulses [10]. The arrangement is therefore bulkier than a single machine. Also, the radiographic image is produced from different directions. Therefore a system capable of generating pulses can deliver radiographic images from the same direction thereby providing higher quality radiographic results.

This section presents the experimental results for multi-pulse operation. The function generator is programmed for generating a burst of pulses. Two repetitive pulses are fired. Figures 4.19(a) and 4.19(b) show the output load voltage waveforms for repetition rates of 100 kHz and 333 kHz. The input voltage is 550V.



(a)



(b)

Figure 4.19: Multi shot four stage output voltage waveforms at (a) 100 kHz and (b) 333 kHz.

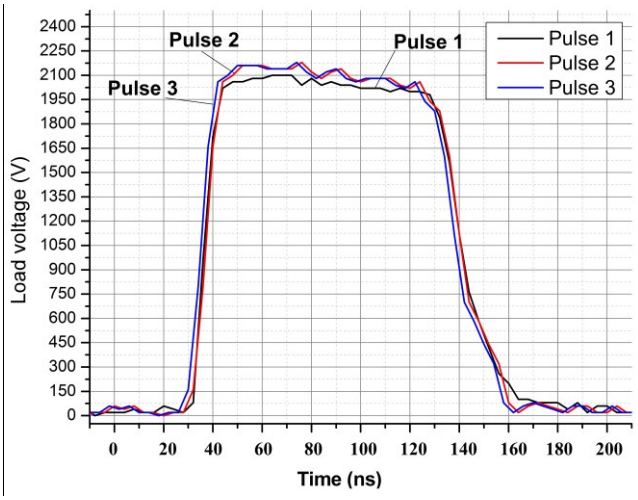


Figure 4.20: Four stage output voltage: Overlay of three consecutive pulses at 100 kHz repetition rate.

Another advantage of using a MOSFET based pulse generator is pulse reproducibility. Repetitive flash radiography with reproducible pulses further enhances the quality of the results. This is demonstrated in Figure 4.20, which shows an overlay of three consecutive pulses at a repetition rate of 100 kHz. The rise and fall times of all three pulses are matched.

4.6.3 Discussion

A compact prototype four stage LTD system is designed and presented which uses a low inductance structural design along with a high-speed gate driver circuit which delivers high current to the gate of the MOSFETs resulting in high speed pulses with rise and fall times of 8.2ns and 22ns respectively. Output voltages and currents of 2.25kV and 200A are demonstrated, which translate to an instantaneous output power of 450kW per pulse. The prototype demonstrates both single shot and multi-pulse operation for pulse widths less than 100ns. The design sets a benchmark for the future design of larger scale systems.

Physically, the experimental setup has a dimension of 25mm per stack. This is limited by the height of the toroid cores. The voltage to height ratio for experimental setup 2 is measured to be 225V/cm.

In order to estimate the performance of the system as the number of stages is increased, a simulation model has been derived from literature. The following section describes the development of the simulation model for the existing system and for a scaled higher voltage system.

4.7 Developing a simulation model

In section 4.3, Figure 4.4, a transformer model was presented. The main constituents of the model are primary and secondary leakage inductances, distributed capacitance and coupling capacitance. Generally, the primary leakage inductance L_{11} is minimal, owing to the configuration of the single turn primary. Similarly, because the primary encloses the core, the primary resistance R_{11} is low and can be neglected [11]. The parasitic elements in the secondary are dominated by the secondary stalk.

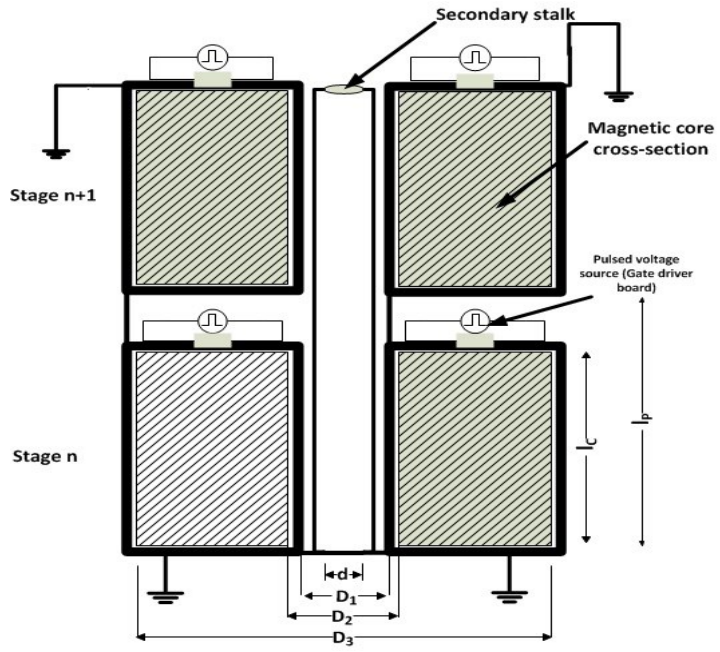


Figure 4.21: Illustration of two-stage inductive voltage adder system with input voltage sourced from the MOSFET based pulse generator.

D_3: outer diameter of magnetic core; D_2: inner radius of the magnetic core;

d: diameter of the secondary stalk; l_P: height of the cell; l_C: height of the core.

Owing to its cylindrical configuration, the LTD system can be modelled as a coaxial transmission line, where the outer cylinder is held at ground potential, and the secondary stalk, which is placed in the centre of the core, acts as the inner conductor. Figure 4.21 illustrates a two stage inductive adder setup and the relevant dimensions which form the basis for the calculation of the parasitic parameters.

The parasitic parameters thus are governed by the following empirical equations [12].

$$L_1 = (\frac{\mu_0 \mu_i l_p}{2\pi}) \ln(\frac{D_1}{d}) \qquad (4.14)$$

μ_i: permeability of the insulation (air), in H/m ; L_1:secondary stalk inductance, in H.

$$C_1 = \frac{2\pi\varepsilon_0\varepsilon_i l_P}{\ln(D_1 / d)} \tag{4.15}$$

C_1: secondary stalk capacitance; ε_i: permittivity of the insulator (air).

The stalk impedance Z_S is:

$$Z_S = \sqrt{\frac{L_1}{C_1}} \tag{4.16}$$

Table 4.6 summarises the dimensions of the proposed four stage LTD system. The diameters of each cell and the corresponding stalk diameters are consistent through each stage. The only variable is the stack height which increases with the number of stages n_1 to n_4. Using equations (4.14) to (4.16), the parasitic parameters are calculated and tabulated.

Table 4.6: Tabulated values of the calculated parasitic parameters.

Stage number	l_P **(mm)**	D_3 **(mm)**	D_2 **(mm)**	D_1 **(mm)**	d **(mm)**	L_1 **(nH)**	C_1 **(pF)**	Z_S **(Ω)**
n_1	25	63	50	30	24	1.11	1.44	27.8
n_1+n_2	50	63	50	30	24	2.23	2.88	27.8
$n_1+n_2+n_3$	75	63	50	30	24	3.35	4.32	27.8
$n_1+n_2+n_3+n_4$	100	63	50	30	24	4.46	5.76	27.8

A lumped element model has been developed to simulate the output voltage of the pulse adder system. Figure 4.22 shows the lumped element equivalent circuit model of a single LTD stage. The model is adapted from the Inductive Voltage Adder model presented in [13].

Here, S_1 represents the MOSFET stack which consists of four parallel connected MOSFETs, D_{S1} is the body diode of the MOSFETs, C_{S1} is the sum of the total output capacitance C_{OSS} of the MOSFETs, obtained from the data sheet, C_S is the energy storage capacitance, L_K is the primary leakage inductance, L_M is the magnetising

inductance, D_1 is the freewheeling diode, and L_1 and C_1 are the secondary stalk inductance and capacitance. The simulation parameters are tabulated in Table 4.7.

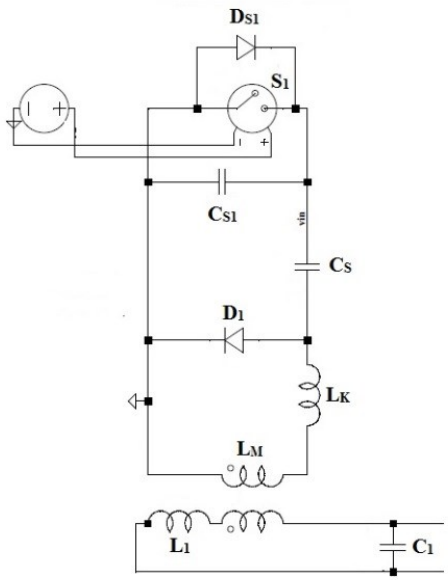


Figure 4.22: Simulation model of a single stage LTD.

Table 4.7: Simulation parameters.

Symbol	Parameter	Value
C_S	Storage capacitance	3.2μF
L_M	Magnetising inductance	27μH
L_K	Leakage inductance	12nH
L_1	Stalk inductance per cell	1.12nH
C_1	Stalk capacitance per cell	1.44pF
n	Number of stages	4
V_{IN}	Capacitor initial voltage	600V
R_L	Load resistance	11Ω
C_{S1}	Output capacitance per cell	800 pF

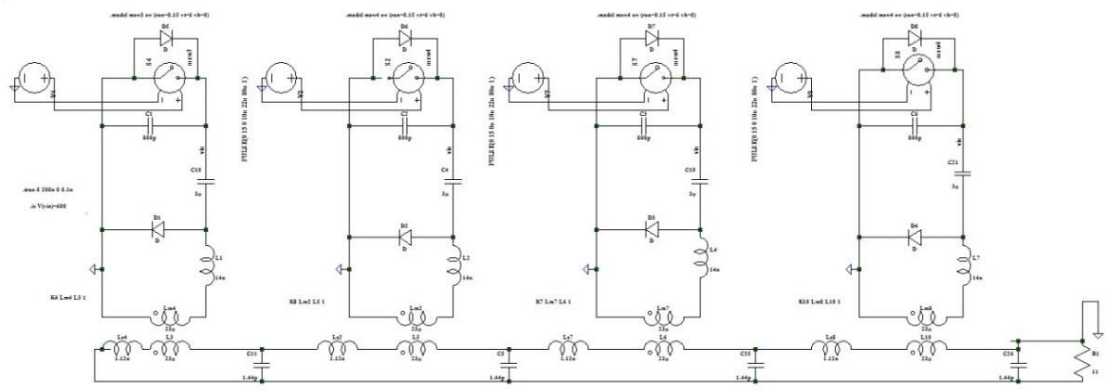


Figure 4.23: Simulation model of a four stage LTD system using the simulation parameters.

The output capacitance C_{OSS} of each MOSFET is 200pF. The total output capacitance C_{S1} of the four devices is therefore 800 pF per stage. The leakage inductance L_K was estimated by applying different values of L_K to the simulation and comparing it with the experimental results. Figure 4.23 shows the simulation model for a four stage LTD system. Figure 4.24 shows the simulated rise time for the pulse based on the listed parameters and with varying values of leakage inductance. Also shown is the experimental rise time waveform at an input voltage of 600V. From comparison, the leakage inductance can be estimated to be 12nH. While an effort has been made to synchronising all the four stages, the rise and fall times are also influenced by minor delays of ±2ns between each stage.

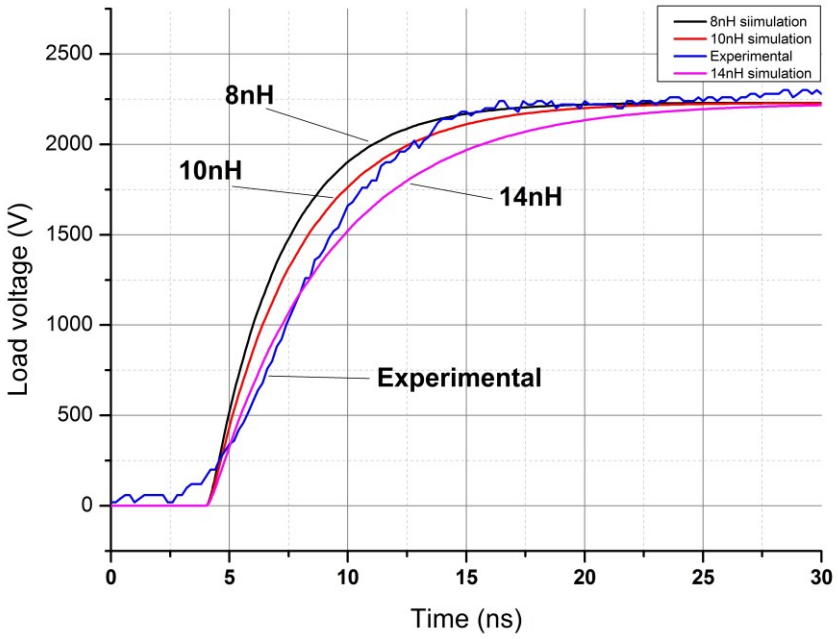


Figure 4.24: Comparison of simulated pulse rise time with experimental waveform.

Figures 4.25, 4.26 and 4.27 compare the simulation and experimental results for different values of load resistance.

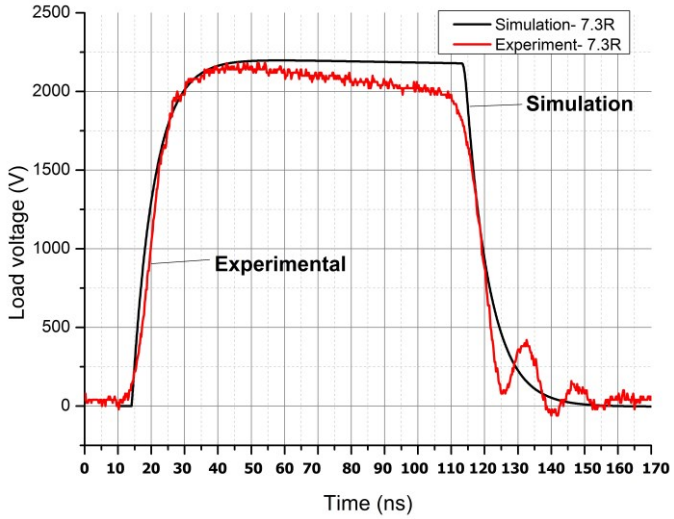


Figure 4.25: Comparison of simulated and experimental waveform for 7.3Ω load.

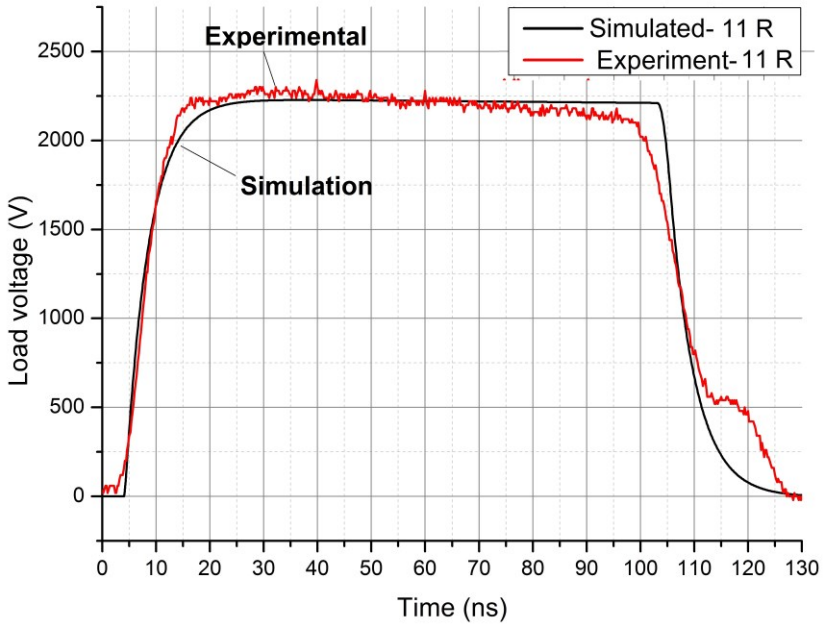


Figure 4.26: Comparison of simulated and experimental waveform for 11Ω load.

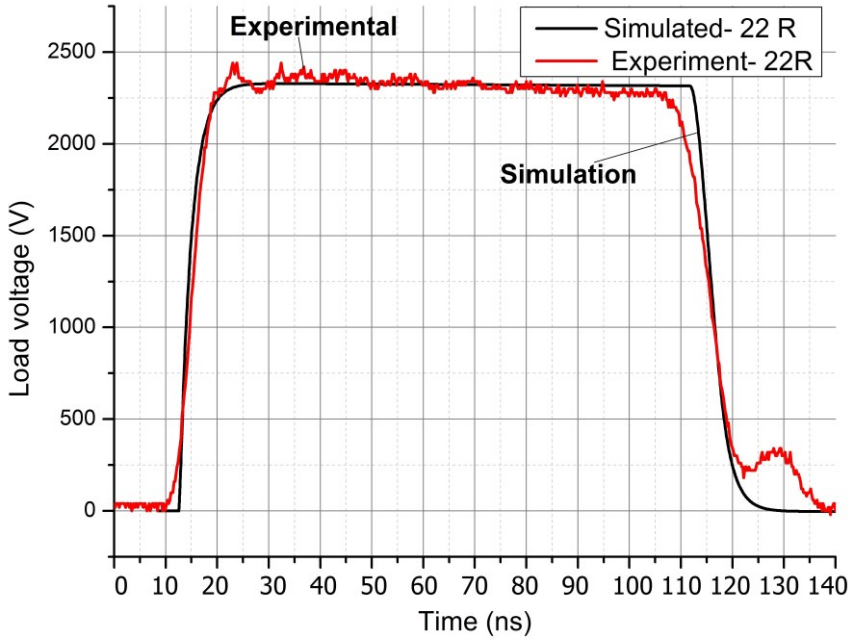


Figure 4.27: Comparison of simulated and experimental waveform for 22 Ω load.

The simulation waveforms match closely with the experimental waveforms. The variations observed in the pulse rise and fall times are influenced by two factors, *1)* The approximation of the value of leakage inductance, *2)* The timing delays between

each adder stage. Results show that the pulse top droop is higher when the load is increased to 7.3Ω. The load current is approximately 300 A. This is attributed to the increased capacitor voltage droop and a higher voltage drop across the stray inductance.

Using equation 4.16, the stalk impedance Z_S is estimated to be 27.8Ω. In an ideal transmission line circuit, the output impedance Z_O=Z_S. However, due to the presence of the leakage inductance L_K, the output impedance increases significantly.

$$Z_0 = \sqrt{\frac{L_K + L_1}{C_1}} \tag{4.17}$$

The total output impedance is thus estimated to be 95Ω. Previous modelling studies [14] have indicated that the output impedance should be matched to the load impedance for optimal pulse rise and fall times.

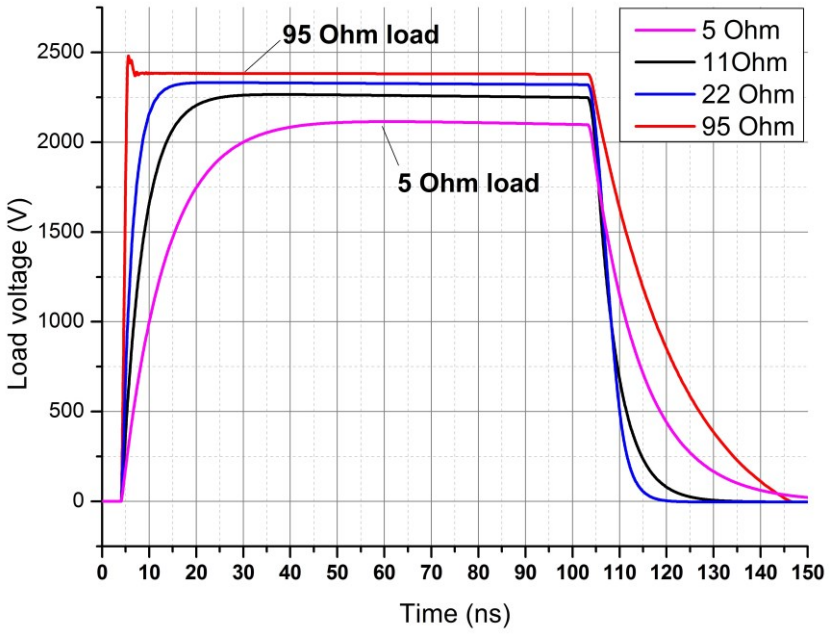


Figure 4.28: Output load voltage waveform simulation for different loads.

Figure 4.28 shows the simulated output voltage waveform for different load resistances. It can be seen that by matching the load impedance with the output impedance, the pulse rise time is significantly improved. This is also observed in Figures 4.25 to 4.27. However, for the proposed experiment, the load is fixed to 11Ω. One way of improving the rise time is by reducing the primary leakage inductance. For example, by reducing the L_K from 12nH to 5nH, Z_0 drops from 95Ω to 65Ω. Alternatively, the stalk impedance Z_S can be reduced by increasing the stalk diameter *d*.

The transformer model was used to scale a larger model. Figure 4.29 shows the results for a scaled 8 stage LTD system based on the described model. A rise time if less than 10ns is achievable with a 22Ω load. Peak output power of 0.92MW is achievable and within the design specification if the proposed system was scaled to eight stages.

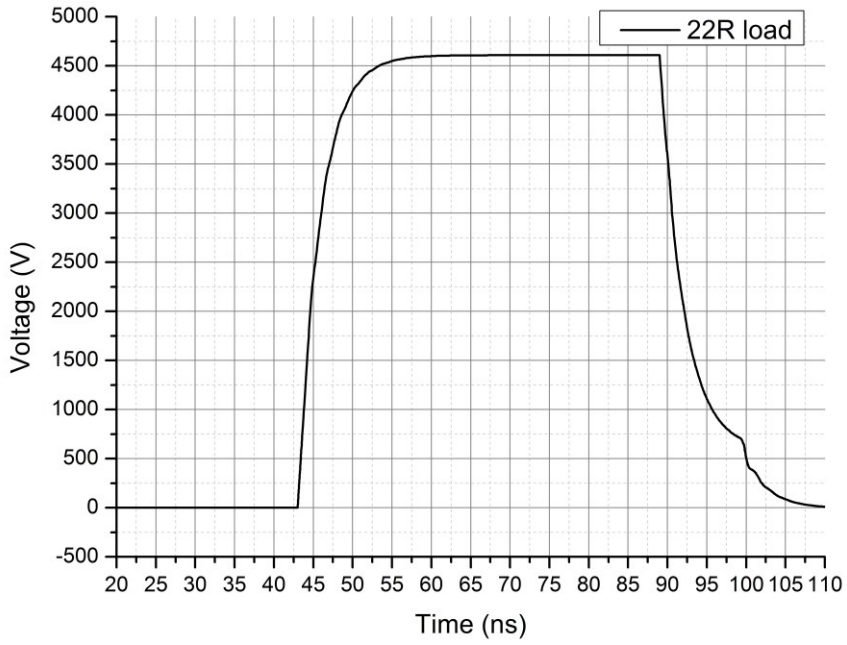


Figure 4.29: Simulated output voltage waveform for an 8 stage Linear Transformer Driver.

4.8 Summary

A compact prototype pulsed power system has been developed using power MOSFETs in an LTD configuration. The system is formed of four 600V adder stages to deliver a total peak voltage of 2.25kV with flat top pulse duration of 80ns and pulse rise and fall times of 8.2ns and 22ns respectively. Using only four parallel MOSFETs per adder stage, the system delivers a peak output power of 455kW. The proposed system demonstrates a significant improvement in the power density and switching performance in comparison to the literature presented in [15], where 35 parallel MOSFETs around the circumference of the core, and corresponding gate driver circuits, are used to deliver an output power of 157kW per stage. In comparison, the proposed system utilises one section of the core to deliver 112kW peak output power using four MOSFETs per stage.

From the experimental results of the four-stage LTD system, it is deduced that the primary and secondary leakage inductances ultimately limit the pulse rise and fall times. The MOSFETs switching speeds are enhanced by the current source gate driver and are capable of producing rise and fall times of approximately 4ns and 9ns as demonstrated in Chapter 3. In order to be able to match the output voltage rise and fall times to that of the MOSFET, the leakage inductance needs to be reduced. One method of reducing the primary leakage inductance is by distributing the layout of the MOSFETs around the circumference of the core. The current design incorporates four MOSFETs clustered on one side of the core. The presented arrangement is therefore optimised for currents up to 200A and satisfies the design requirements. If the design changes and the power requirements increase, several driver boards can then be stacked around the core to fulfil this requirement. For

example, if the current demand for each stage increases from 200A to 800A, four driver boards each with four parallel connected MOSFETs can be stacked around the circumference of the core. The leakage inductance and the load current remains the same for each board. Thus similar switching performance can be obtained at higher operating currents. Similarly, the output current loop of the secondary stalk will be distributed around the circumference of the core reducing the overall secondary leakage inductance, thereby improving system response.

A lumped element simulation model of the LTD system has been presented. The simulation results show a close relation with the practical results. By matching the stalk impedance with the load impedance, optimum rise and fall times can be obtained. The primary and secondary leakage inductances have a significant effect on the total output impedance seen by the load. This output impedance is estimated to be 95Ω for the proposed system. The load impedance is 11Ω. Although the load is not matched to the output impedance, the achieved output voltage rise and fall times fall within the design specifications, and therefore do not require further optimization. The response can however be improved by reducing the output impedance. This can be achieved by circular stacking of several parallel MOSFETs around the core, as well as by increasing the secondary stalk diameter. There are however limitations to this due to the minimum spacing requirements for high-voltage insulation. This imposes a limitation on the maximum permissible diameter for the stalk and ultimately the minimum achievable output impedance.

A scaled eight stage LTD was simulated to further demonstrate the performance of the system at higher voltages. It is shown that similar switching

performance can be achieved at higher output voltages using the proposed MOSFET based pulsed power system.

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Chapter 5

Conclusions

5.1 Conclusion

Pulsed power flash radiography technology requires the generation of high-voltage short pulses with very fast rise and fall times. From the literature survey it was realised that the characteristics of pulsed power systems are greatly dependent on the capability of the switches as well as a low inductance layout arrangement. This study focused on the effective utilisation of MOSFET switching technology since the majority carrier MOSFETs exhibits the fastest switching characteristics of available switching devices. Also, MOSFET characteristics allow parallel connection to increase the system power rating. These capabilities make MOSFETs the desired candidate for pulsed power switching technology. It is realised that the low power density of power MOSFETs presently limits their applicability in high power systems, such as flash radiography, due to increased complexity and component count. Available higher power density MOSFETs exhibit slow switching times when using commercially available MOSFET gate drivers. To meet the next generation requirements in pulsed power and to advance the applicability of MOSFETs in higher power applications, a novel gate drive has been proposed in this thesis.

5.1.1 High speed current-source MOSFET gate driver

The proposed novel contribution is a high-speed gate driver for high input capacitance power MOSFETs for pulsed power applications. The gate driver circuit

uses an inductor as a high-current source to rapidly charge the MOSFET gate capacitors thereby enhancing their turn-on switching speeds. The circuit uses a minimal number of active and passive components, making it suitable for single shot or burst mode pulse operation while maintaining simplicity and reduced component count. Using a DE475102N21A MOSFET, pulse rise and fall times of 4ns and 12ns were demonstrated at an operating voltage of 500V and a load resistance of 10Ω. The driver also demonstrated the ability to drive multiple MOSFETs connected in parallel. Test results demonstrate the performance of four parallel connected MOSFETs operated by a single gate driver.

The proposed gate driver design affords reduced component count by minimising the number of gate drivers required in a pulsed power system. In the proposed design four MOSFETs are used per gate driver board. Also, with high power density 1000V, 144A (pulse current) DE475102N21A MOSFET, the total number of MOSFETs required to deliver a given power reduces significantly.

Following the gate driver design and MOSFET selection, a pulse transformer was designed using a Nanoperm toroidal magnetic core encompassed in an aluminium enclosure to form a single primary turn wound core. This low inductance configuration was assembled in the form of a Linear Transformer Driver (LTD) configuration which is widely adopted in pulsed power systems due to its ability to deliver high voltage pulses using several lower voltage pulse sources in an inductive voltage adder configuration.

A prototype four stage LTD system using the proposed gate driver circuit was demonstrated at an operating input voltage of 600V for single-shot and burst-mode

operation. An output pulse voltage of 2.25kV with an 11Ω resistive load (200A) was demonstrated with pulse rise and fall times of 8.2ns and 22ns respectively. Multiple and reproducible high voltage and high speed pulses are a novel development which is demonstrated in this thesis. Variable burst mode repetition rates are demonstrated up to 333 kHz with a maximum of three consecutive pulses. The unit achieves the performance specifications and shows potential for future large repetitive pulse generator systems using Power MOSFETs.

A simulation model was developed based on the available literature and using the design parameters. Simulation results were compared with the experimental results for various load resistances. The results confirm good correlation with the experimental results and therefore can be used as a tool to predict system output using the specified equations and design parameters.

5.2 Future research

This section presents possible future research topics.

5.2.1 Current source MOSFET gate driver

The proposed current source driver in Chapter 3 has been implemented discretely. In order to be widely adopted into a large scale system, the drivers will need to be integrated into a single integrated circuit unit. The relative logic timing control of the gate drivers will be required to be controlled from a remote source such as a computer which is capable of high resolution timing adjustments of 0.5ns. A tighter layout will improve gate driver performance, allowing minimum achievable pulse widths.

The repetitive pulse frequency for the current design is limited by the charging and discharge time of the gate driver inductor. Modifying the logic timing signals will enable the use of the gate driver in repetitive pulse operation where the time between two consecutive pulses can range from several tens of nanoseconds to several hundreds of nanoseconds. This can be achieved by operating the gate driver inductor in continuous conduction mode.

5.2.2 LTD design and layout

Research into the characteristics of different magnetic cores, identifying more suitable magnetic core materials specific to this application, will ensure lower losses and effective use of the magnetic core. Closer attention needs to be given to a design with lower high-frequency losses. This would help reduce the metal housing cost of each transformer. Voltage to height ratio can be increased by using thinner and wider cores with the same effective core area.

When the system is scaled to higher voltages, the insulation requirements increase. Further research into using different insulation techniques will help reduce the spacing requirements between the stalk and the inner core radius.

As the height of the system increases, output pulse shapes will be affected by the pulse propagation time through the inner stalk. Detailed study into the effects of this delay and appropriate delay pulse circuitry will ensure synchronised firing of each stage.

Appendix A – Schematic of the proposed gate driver circuit

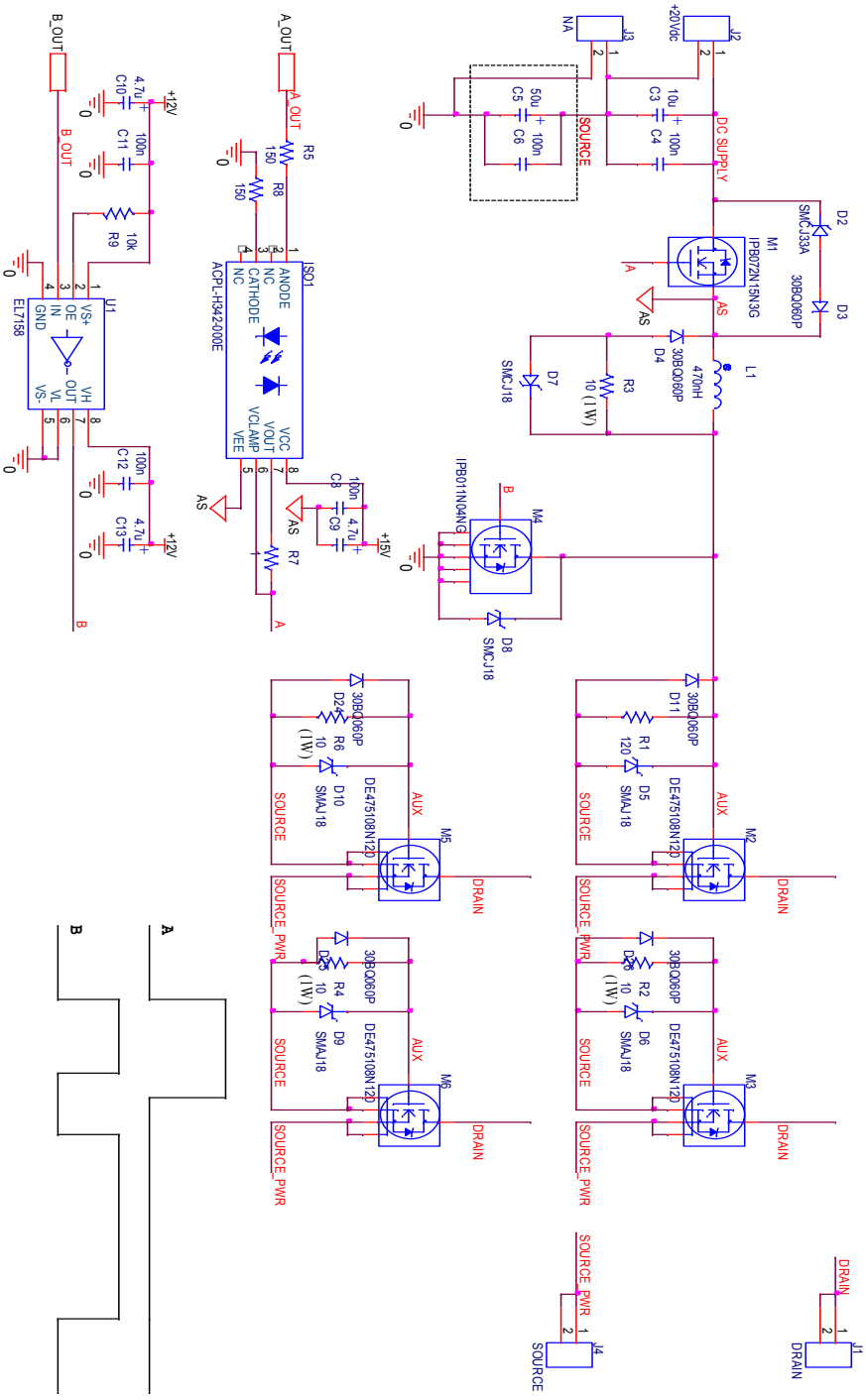

Figure A1: Schematic of the proposed gate driver circuit.

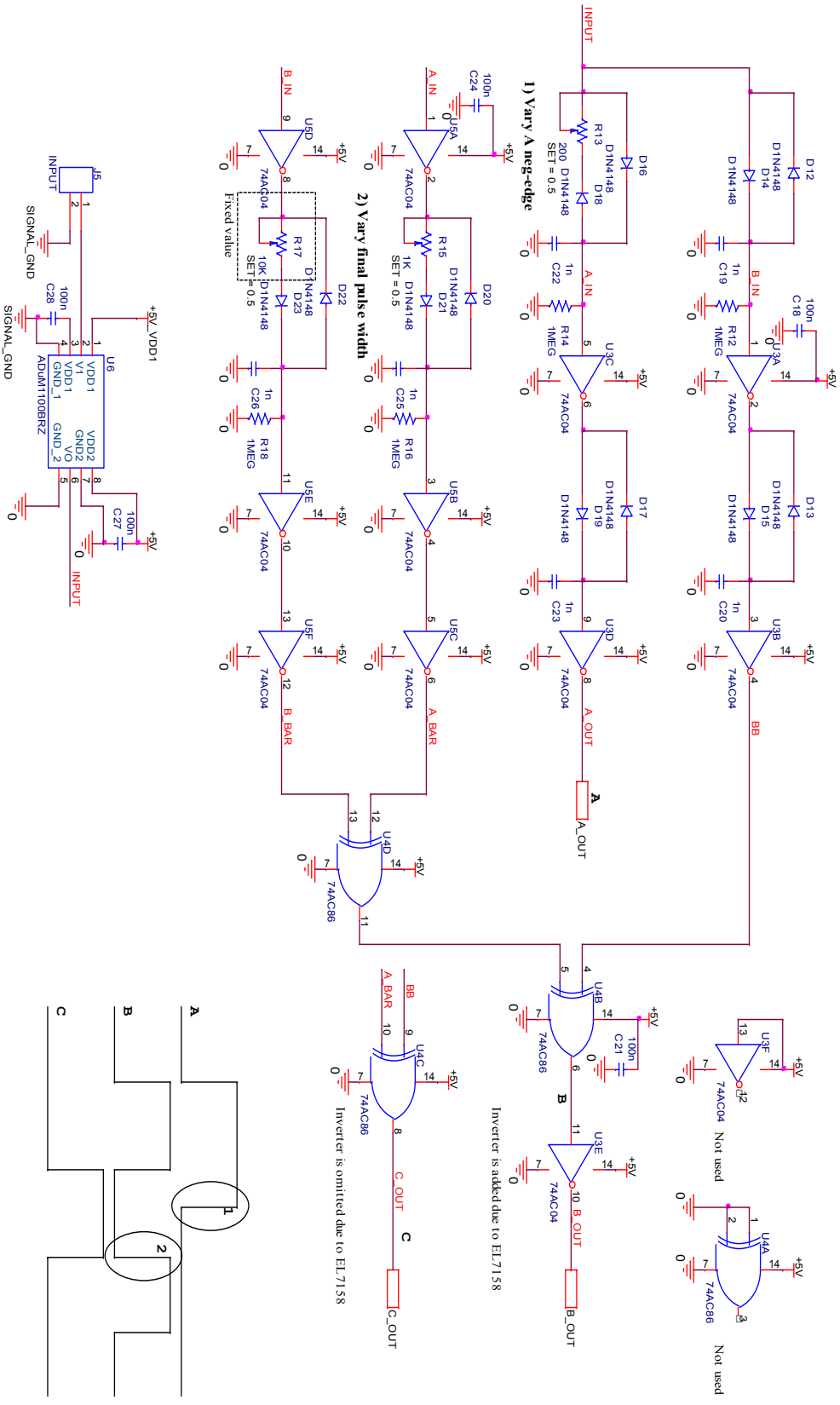

Figure A2: Schematic of the logic circuit for the proposed gate driver.

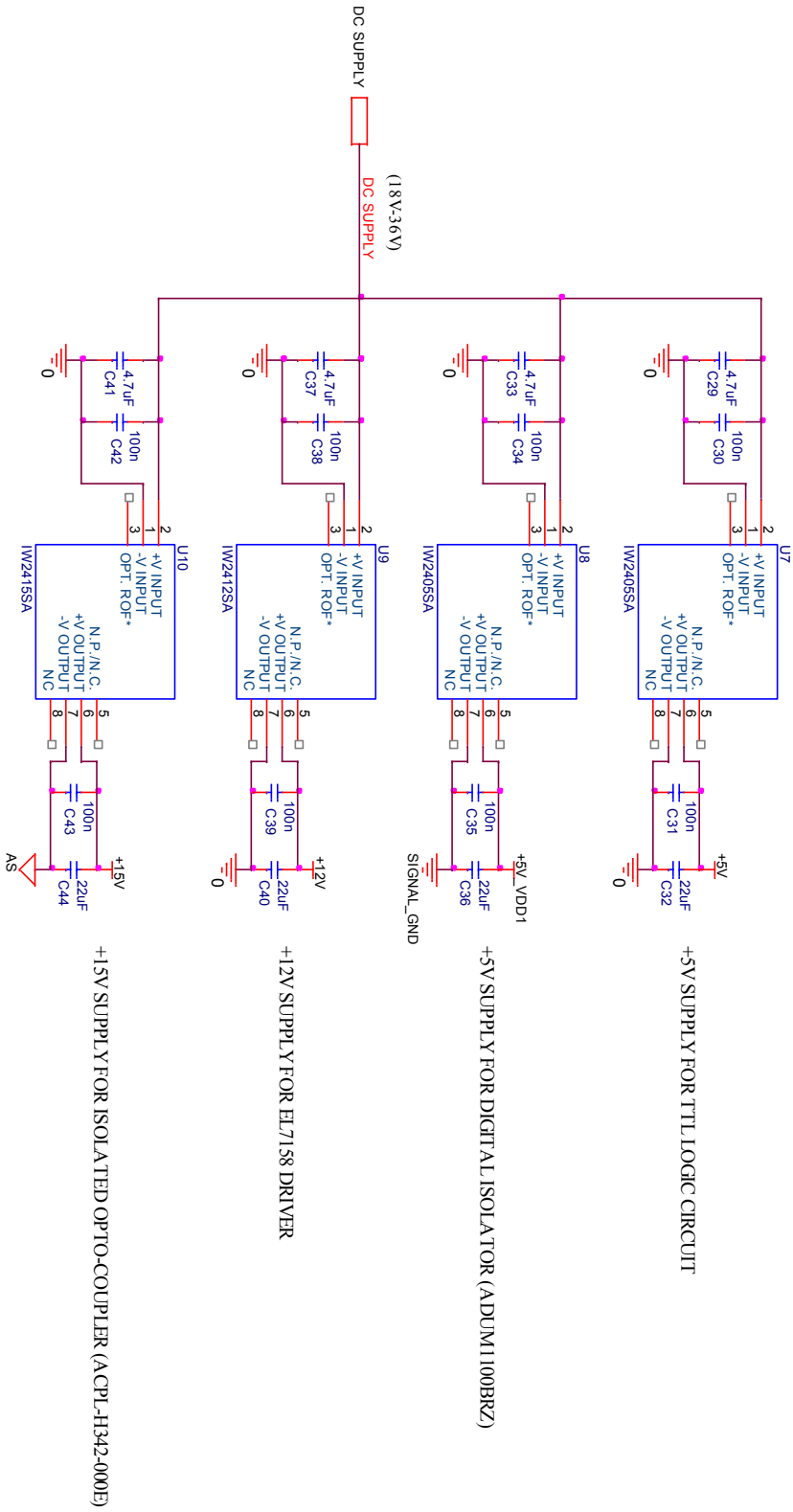

Figure A3: Schematic of power supply for the proposed gate driver.

Appendix B -PCB layout

This section presents the gate driver circuit PCB layout with power side circuit copper to slide into the pulse transformer.

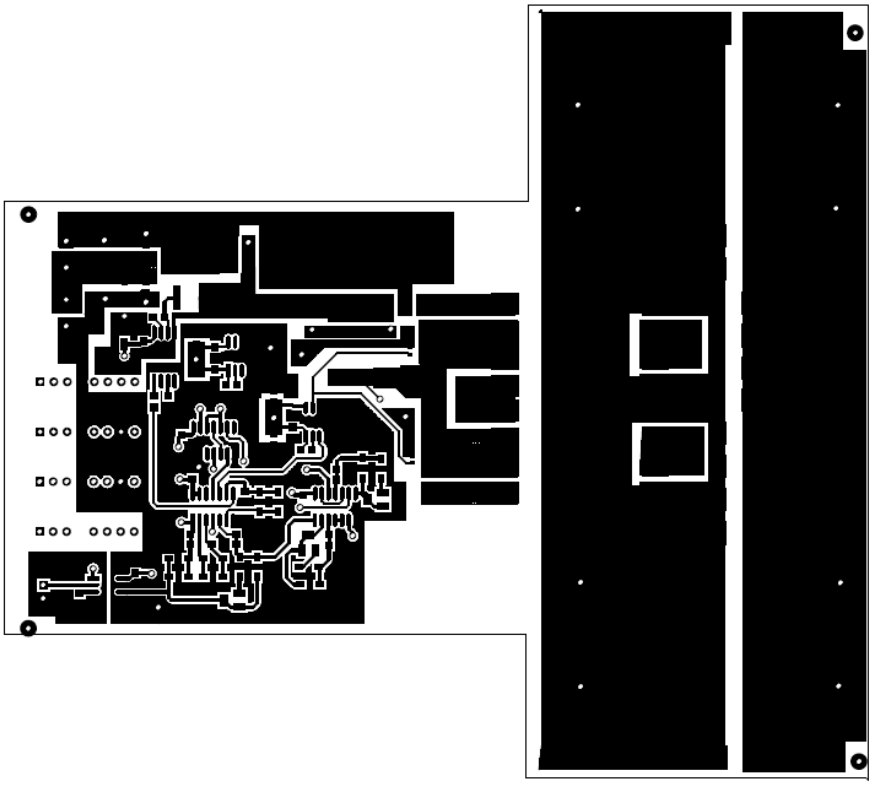

Figure B1: Gate driver circuit top layer PCB.

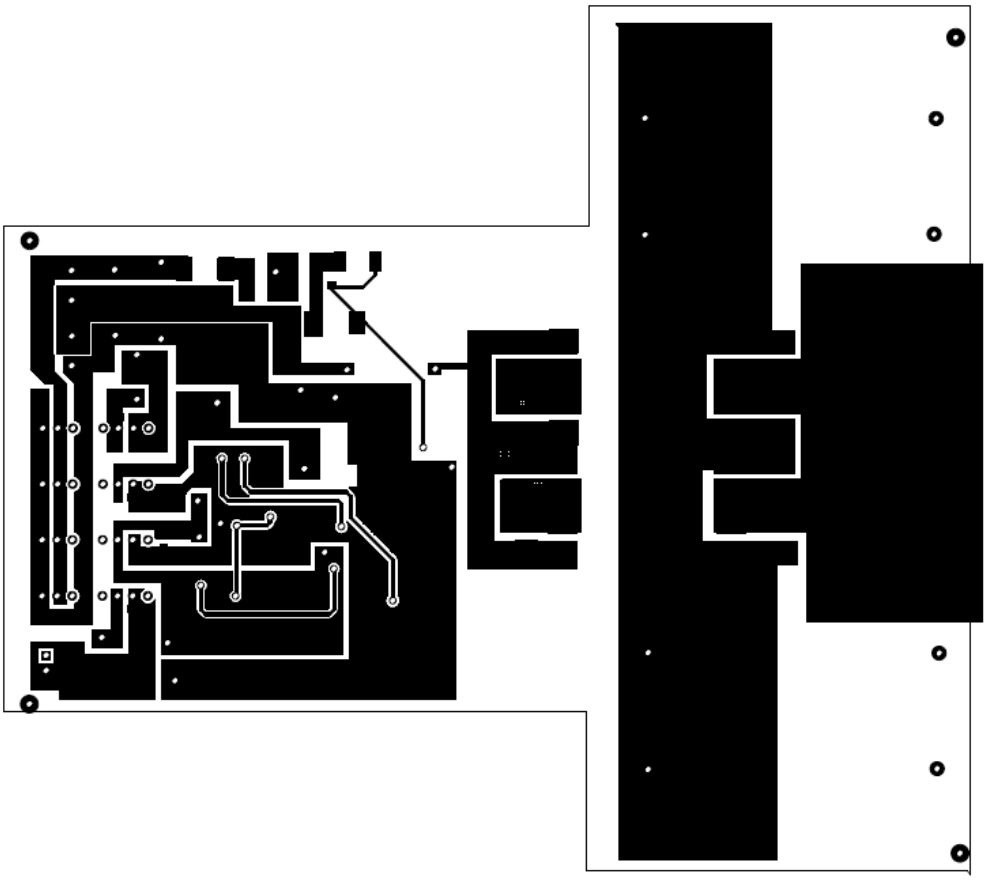

Figure B2: Gate driver circuit bottom layer PCB.

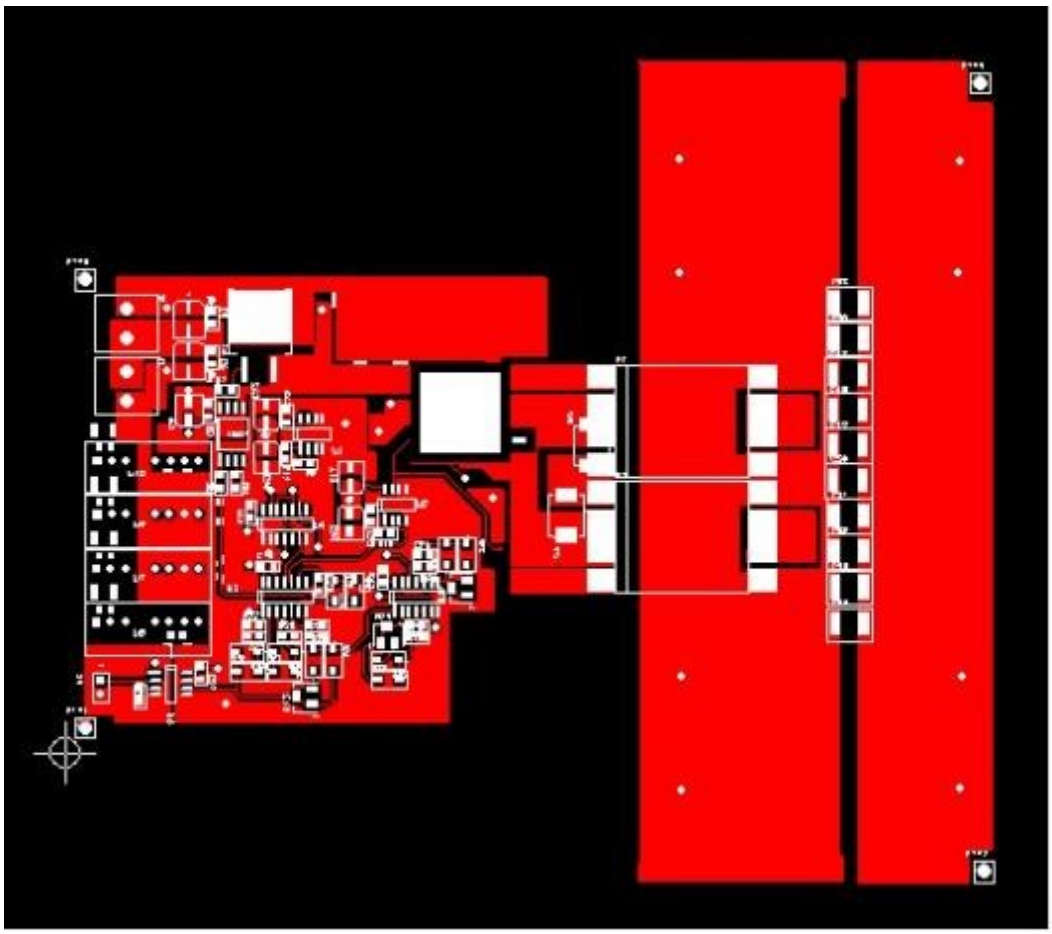

Figure B3: Gate driver circuit top silk.

Appendix C -Mechanical drawings

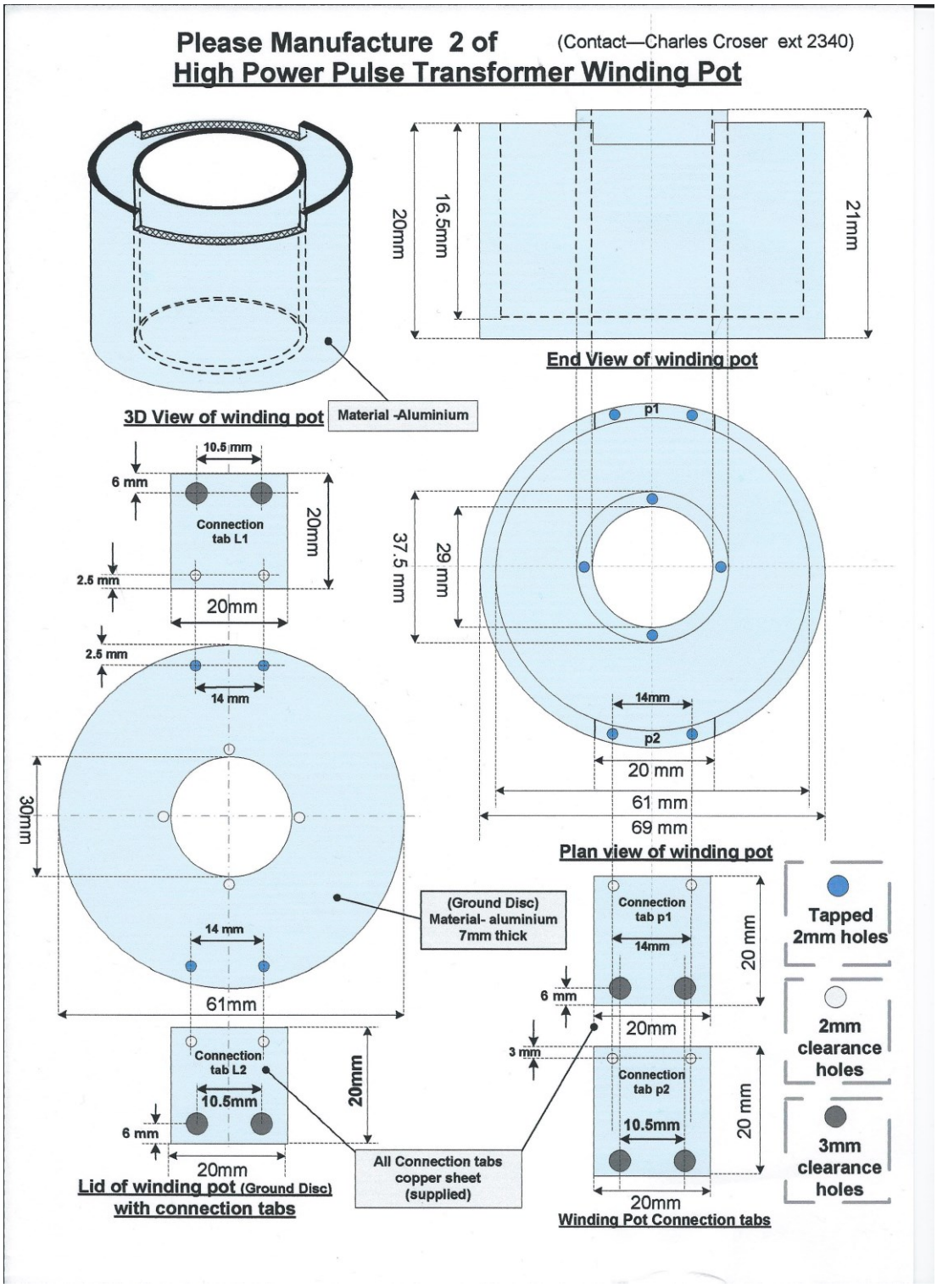

Figure C1: Magnetic core enclosure (Primary winding).

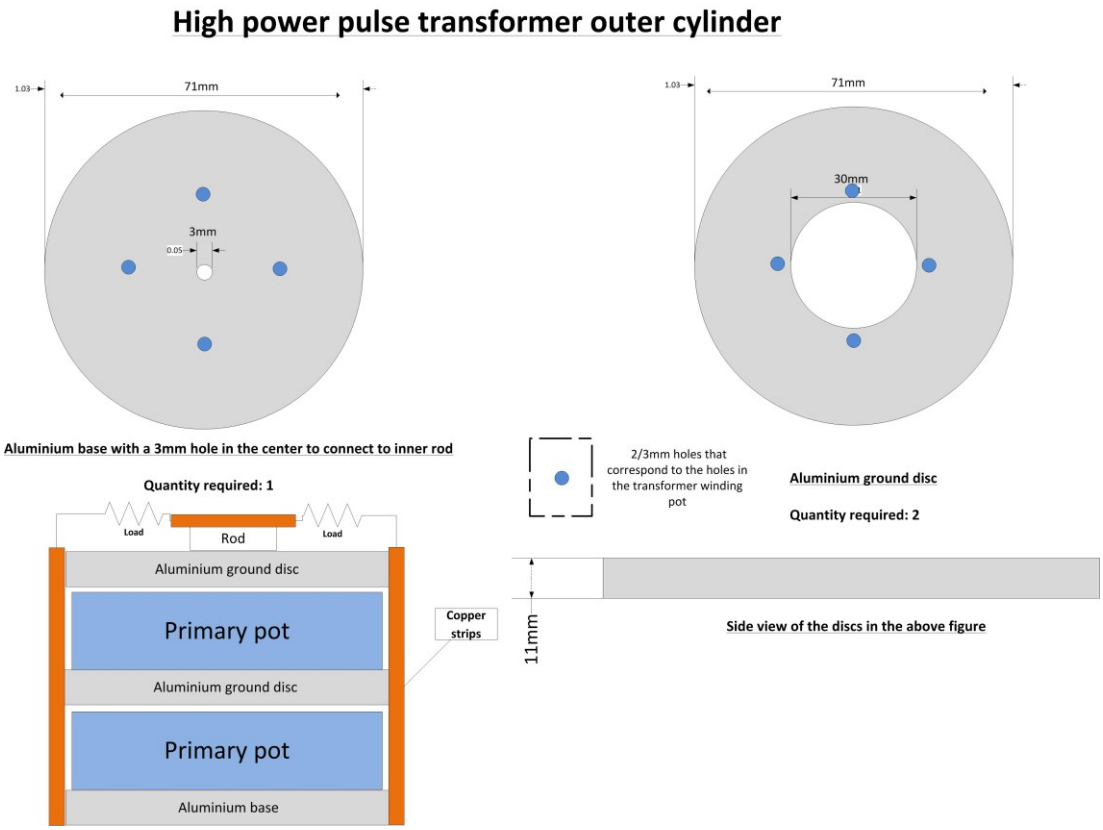

Figure C2: Outer cylinder dimensions.

Appendix D - Publications

Throughout the course of this study work was presented at international conferences including two oral presentations and two poster presentations. This has resulted in the publication of two conference papers and one journal paper with further scope of another journal paper in the June 2013 special issue of the IEEE transactions on plasma science. The details of these papers are given below.

Journal papers

1. P.Iyengar, T.C. Lim, S.J. Finney, B.W. Williams, M.A. Sinclair, "Design and analysis of an enhanced MOSFET gate driver for pulsed power applications,"

IEEE transactions on dielectrics and electrical insulation, Vol.20, no.4, August 2013, pp: 1136,1145.

Conference papers

1. P. Iyengar, T.C. Lim, S.J. Finney, B.W. Williams, M.A. Sinclair, "A 600V, 1KA compact LTD module using power MOSFETs," IEEE international power modulator and high voltage conference, June 2012, pp: 180-183.

2. P. Iyengar, J.E. Fletcher, D.J. Bittlestone, M.A. Sinclair, "Enhanced MOSFET gate driver for pulsed power IVA module," IEEE international pulsed power conference, 19-23 June 2011, pp: 1477-1481.

Appendix E- Table of Figures