

# Hardware tools for optogenetic neuroscience experimentation.

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# Declaration

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Signed:

Date:

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# List of abbreviations

$\mathbf{AC}$	Alternating current
BCI	Brain computer interface
BOE	Buffered oxide etchant
ChR2	Channel rhodopsin
CMOS	Complementary metal oxide
COTS	Commercial off the shelf
CVD	Chemical vapour deposition
DAC	Digital- analog converter
DBS	Deep brain stimulation
DC	Direct current
DMA	Direct memory access
DNA	Deoxyribonucleic acid
ECOG	Electrocorticography
EEG	Electroencephalogram
EEPROM	Electrically erasable, programmable read-only memory
EQE	External quantum efficiency
$\mathbf{FFT}$	Fast fourier transform
FDA	The United States Food and Drug Administration
FEA	Finite element analysis
FPGA	Field programmable gate array
FSCV	Fast scan cyclic voltammetry
GEAIs	Genetically encoded activity indicators
HMDS	Hexamethyldisilazane
I2C	Inter-Integrated Circuit
IC	Integrated circuit
ICP	Inductively coupled plasma
IQE	Internal quantum efficiency
IR	Infra-red
LD	Laser Diode
LDO	Low Drop-out (Regulator)
LED	Light emitting diode
LFP	Local field potentials
MISO	Master in slave out
MOSI	Master out slave in
MEA	Micro-electrode array
$\mu \text{LED}$	Micro Light emitting diode
MOVPE	Metalorganic vapour-phase epitaxy
OCD	Obsessive compulsive disorder
OOK	On-Off keying

PCB	Printed circuit board
PD	Parkinson's disease
PECVD	Plasma enhanced chemical vapour deposition
$\mathbf{PR}$	Photoresist
PSRR	Power Supply Rejection Ratio
PVD	Physical Vapour Deposition
PWM	Pulsewidth modulation
$\operatorname{RF}$	Radio Frequency
RIE	Reactive ion etching
RTA	Rapid thermal annealing
SEM	Scanning electron microscope
SPI	Serial Peripheral Interface
UV	Ultraviolet
VLC	Visible Light Communication

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# Abstract

Optogenetics confers the ability to precisely control the activity of neural populations with cell type specificity in response to illumination, providing a distinct advantage over the indiscriminate action of electrical stimulation. This added specificity offers considerable potential for advancement of experimental neuroscience, with applications ranging from improved understandings of neural circuits to the development of novel neuroprosthesis.

The work presented here focuses on the development of hardware tools for optogenetic experimentation; divided between the development of micro-LED neural probes, and electronic hardware for stimulation/recording control.

The development of neural probes with both optical stimulation and electrical recording sites (commonly known as optrodes), capable of providing illumination up to 100  $\text{mW/mm}^2$  is illustrated. A hybrid fabrication technique integrating micro-LEDs with monolithic probes was demonstrated; offering an attractive technique for the development of neural probes with multi-spectral stimulation capabilities.

To utilise such optoelectronic neural probes, a lightweight (sub 3g), low form factor ( $\approx$  18x15x10mm) wireless stimulation system was realised; offering individual control of up to 16 µLED channels. Microprocessor control enables flexible control of intensity, pulse width and repetition rate with a temporal resolution of 0.1ms; facilitating creation of diverse optical stimulation patterns. IR communication allows user selection of pre-uploaded stimulation protocols or direct uploading of stimulation protocols to the system's memory.

A bi-directional neural stimulation/recording system was created to harness the ability of optrode probes, allowing electrical/optical stimulation combined with recording of up to 16 channels at a sampling rate of 20kHz. These features were translated to a prototype wireless SD card based logger (permitting recording at 1kHz). Exemplar closed loop algorithms based on threshold crossing events were implemented on these systems.

## Chapter 1

# Introduction

### 1.1 Motivation

Neuroscience is turning science fiction into reality<sup>1</sup>. Electrical recording/stimulation of neurons have enabled humankind to directly interact with our own nervous systems for the treatment and alleviation of a widening range of clinical ailments. Successful interventional techniques have included: restoration of the senses through the auditory and visual pathways(2), alleviation of tremor in Parkinson's patients (3) and cortical control of brain computer interfaces (4),(5) to name a few. Successful adoption of neurotechnology in the clinic is only expected to increase as novel treatments and techniques are developed.

The importance and benefits of these techniques to society, and the necessity for further investigation, has been recognised outside the neuroscience and medical communities; large-scale government funded initiatives have spent multi-million figure sums on research into human neuroscience with key milestones for the development of interventional tools(6), (7). The gaze of industrial bodies has similarly shifted towards electroceuticals and bioelectronics as viable source for future revenue(8), (9); not only for clinical treatments but also for the adoption by the healthy patient(10).

The success of these techniques, however, is built on a vast body of neuroscience laboratory research. Significant improvement in neurotechnology can only be achieved through deeper understanding of the fundamental workings of the brain. This feat, however, is mired by the complexity of the human brain; there are approximately 86 billion neurons (11) which communicate over 100 trillion synapses. The enormity of this system and its intrinsic complexity requires multidisciplinary concerted actions to unravelling the brain's function; drawing input from varying fields including: neuroscience, biology, computing and engineering. However, despite these attempts the brain still holds many mysteries.

Electrical stimulation has long been one of the key tools to modulate neural activity; having found use in a neuroscience setting since the 1800s and from the 1950s onwards for various clinical treatments(12). Electrical stimulation has one major drawback; it indiscriminately stimulates neurons within its volume of influence. This lack of selectivity has held back our understanding of the brain. For example, despite the significant progress that has been made throughout its 50-year history; the exact mechanisms underpining deep brain stimulation's operation are still debated(13). Similarly, the efficacy of cochlear implants (perhaps the most ubiquitous neuroprosthesis) is held back by current spread in tissue(14). The ability to more accurately stimulate specific neural

<sup>&</sup>lt;sup>1</sup>The reader needs only to consider brain computer interfaces (BCI) to see that this is the case(1).

populations would convey the ability to understand neural circuits at a deeper level, the implications of which could eventually lead to enhancing the patient's quality of life.

Enter optogenetics, a relatively novel technique emerging in the early 2000s (15), which allows the genetic modification of neurons to light. The genetic modification component of this technique allows improved specificity in comparison to electrical stimulation. However, light is not natural within the body which brings us to the crux of this thesis. Optogenetics, as a new technique, requires the engineering of novel tools; this thesis details the development of one such tool, an optoelectronic system for combined optogenetic/electric stimulation and recording of neurons.



Figure 1.1: Components of a Neuromodulation System. This thesis covers the development of the hardware required for neuromodulation (outlined rectangle). The neural probe (Chapter 5,6) provides direct interaction with the neurons. This interface is supported by external hardware (Chapter 7,8) which handles data aquisition and provision of stimulation.

### 1.2 Thesis outline

This thesis details the development of hardware required for optogenetic neuroscience experiments. It is roughly split into two main bodies of interest; the first undertakes the creation of devices for the recording/perturbation of neurons and the second which focuses on the development of electronic hardware to properly harness these device capabilities. Chapters 2-4 describes the background required for the reader to appreciate this thesis: detailing the underlying issues these devices rely/operate on; comparing state of the art devices and providing context on the creation of microscale optoelectric devices. Chapter 5 details the fabrication and characterisation of a neural optrode, designed for multimodal use: optogenetic and electrical stimulation with simultaneous recording. Chapter 6 describes a hybrid technique incorporating both transfer printing techniques and monolithic fabrication, which is then demonstrated in the creation of a dual colour optogenetic stimulator. Having described these devices, the thesis switches focus to the creation of electronic hardware required for the usage of such devices; tackling two key challenges: stimulation and neural recording. **Chapter 7** reports on the creation of a wired stimulation system, capable of providing stimulation currents for either electrical or optical stimulation. This system is further enhanced to a low weight, miniature wireless neuro-stimulator for use in freely moving neuroscience experiments. **Chapter 8** sets out a wired multimodal system through the incorporation of neural recording capabilities. A wireless multimodal system is proposed. Simultaneous stimulation/recording capabilities open the doors to closed loop stimulation, and the hardware system is characterised in its ability to perform biomarker detection. **Chapter 9** concludes this thesis and offers guidelines for future work.

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### Chapter 2

# Background

### 2.1 Neurons

The brain is a complicated electrochemical system, whose varied and multi-faceted actions give rise to its behaviour. Like all other organs, the brain is composed of a variety of cells working in conjunction; namely neurons, astrocytes and glial cells. However, it is the neurons, which make up the functional building blocks of the brain and provide the focus for most research.

#### 2.1.1 Neuronal anatomy

Neurons are electrically excitable cells which exist in many forms, however, all share three anatomical characteristics; a cell body, dendrites and an axon (Fig 2.1). The neuron's cell body, referred to as the soma, is approximately 10 microns in diameter containing the nucleus of the cell. Branching appendages (dendrites and axons, collectively known as neurites) project from the soma forming connections with other neurons at regions known as synapses. The dendrites extend hundreds of micrometres into the extracellular matrix; the number and arrangement of these vary greatly ranging from single connections between neurons to vast collections of dense connections(1). The axon is the largest of all neural projections, and acts as a conduit to transmit the neuron's signal. The neuron only ever contains one axon, which may branch to numerous other neurons before termination. Some axons are coated in a myelin sheath, an insulating coating which improves the axons ability to propagate a signal. The neuron is not alone in its functioning and may synapse with thousands of neurons. The synapse is a tightly bound connection between neurons, which allows the propagation of one neuron's signal to another neuron. This synapse can be chemically mediated through the transferal of chemical messages known as neurotransmitters; or electrical through either gap junctions which permit a direct electrical connection between neurons or electric field propagation across the synapse(2).



Figure 2.1: Neurons Top) Anatomical structures of a neuron.

#### 2.1.2 Neural electrophysiology

The role of neurons is to process incoming electrochemical signals deriving from other neurons, or in the case of sensory neurons from an externally triggered stimuli. The neuron interprets this information, and under correct stimulus, produces its own signal which is transmitted to other neurons. One key component in this transmission is the action potential, a fast propagating electrical signal, which transmits the signal through the axon from the soma to the distant synapses. The neuron's cellular components and their underlying mechanisms are key in the development and spread of the action potential.

#### Transmembrane proteins and the resting neural potential

The cytosol of the neuron is separated from the extracellular fluid by the cellular membrane, a phospholipid bilayer structure, which is intrinsically impermeable to the flow of ions and polar molecules. Distributed across the cellular membrane are a variety of transport proteins; transmembrane proteins which regulate the ionic concentrations within the cell and facilitate transport of these substances across the membrane. The most notable of these of these are the Sodium channel, Potassium channel and the Sodium-Potassium pump. Together these transport proteins facilitate the generation and propagation of the action potential within neurons.

At rest these membrane proteins act to maintain the intracellular ionic concentrations such that the neuron's cytosol is potassium rich in comparison to the sodium and chlorine rich extracellular fluid. This difference between the ionic concentrations creates a separation of charge, with a negatively charged intracellular medium compared to the extracellular. This charge separation means the intracellular potential of a neuron lies at a different potential with respect to the extracellular fluid, this difference is known as the membrane potential. At rest the cell membrane potential is maintained at  $\approx$ -40-70mV with respect to the extracellular medium.

#### Action potential: The Hodgkin-Huxley model

However, when a neuron is activated the neuron produces an action potential: a fast transient change of the membrane potential distinguished by a sharp rise in cell potential (depolarisation)(fig 2.2, phase 1-3), followed by a slower return to resting potential (repolarisation) (fig 2.2, phase 3-5). The action potential initiates in the soma, and propagates through the axon to the synapse where the signal is passed onto further cells.



Figure 2.2: The action potential. The action potential is characterised by a transient change in cellular potential (top), which is determined by the opening and closing of various membrane proteins (lower).

This process was investigated by Hodgkin and Huxley in 1952(3) and described as

five distinct events, each of which is described by the actions of the membrane transport proteins and ion species mentioned in the previous segment:

- 1. An externally triggered event (e.g neurotransmitter release) causes an influx of sodium ions into the cell, locally increasing the potential (fig 2.2, stage 2).
- 2. If the area is sufficiently depolarised above a threshold ( $\approx$ -55mV), voltage sensitive sodium channels activate; drawing in more sodium ions. This new influx of sodium ions depolarises adjacent areas above threshold, opening more voltage sensitive sodium channels, creating a positive feedback loop which quickly spreads the depolarisation across the cell.
- 3. The increased potential activates voltage sensitive potassium channels; expelling potassium from the cell (fig 2.2, stage 3). The sodium channels close, and enter an inactive state whereby they are unable to open. The net effect of these two actions halts further depolarisation, and decreases cellular potential, returning the cell to the resting potential.
- 4. Potassium channels remain open, further reducing the cellular potential below the resting potential. This undershoot is known as hyperpolarisation.
- 5. Eventually the Na/K pump returns the concentration of the cells to their resting state (fig 2.2, stage 5).

The millisecond refractory period of the Na channel prevents reopening of recently opened channels, this ensures the orthodromic propagation of the action potential (i.e away from the soma). This of course is a simplified description of the mechanisms contributing to the neuron's action potential, and further mechanisms can influence this.

### 2.1.3 Neural encoding and populations

The neuron takes inputs from many sources and providing a single response signal (which may again be input to multiple neurons). This signal may then play excitatory or inhibitory roles in the synapsing with other neurons. The interplay of these neurons creates complex networks of interconnected neural populations, incorporating exquisite feedback systems. It is this distributed and coordinated activity which gives rise to the behaviour of the brain, however, this complexity which hinders understanding of the brains workings. Understanding the intricacies of the brain is an extraordinary demanding feat due to the incredible diversity and density of the neural circuits; yet, remarkably, improvements in neural recording and stimulation techniques have allowed the investigation of neural circuitry in ever increasing scale and precision.

#### 2.1.4 The mouse brain

Mice play a significant role in neuroscience research, which despite their differences to humans share enough morphological features to draw comparative conclusions including the main structures/systems that make up the brain and the sensory pathways (e.g. cortex, cerebellum, brainstem etc). The neural probes demonstrated later in this thesis were designed with the auditory pathway in mind (albeit not exclusively, these probes have been designed on a scale that they can access the majority of neural areas), and so to orientate the reader the salient features of this shall be briefly explained. First the mouse brain is dimensionally small (roughly a cuboid of dimensions approximately 15mm long x 11mm wide x 7.5mm thick). The brain is (structurally and functionally) split into multiple regions with a general gradient of increasing information complexity from the brainstem (the lower rear of the brain) to the cortex (the upper-frontal area of the brain). The central auditory pathway begins at the brainstem where it passes through the following brain regions before terminating in the auditory cortex (only those with \* shall be discussed in further detail, for further details please refer to (4) and (5)).

- 1. Cochlear nucleus.
- 2. Olivary complex.
- 3. Lateral lemniscal nuclei.
- 4. Inferior colliculus\*.
- 5. Medial geniculate body.
- 6. Auditory cortex\*.

The structure of the inferior colliculus and auditory cortex are both superficial regions on the upper region of the brain therefore facilitating more straightforward surgical access compared to the other deeper regions of the auditory pathway. These regions are both structured tonotopically (i.e. each auditory tone is attributed its own region of neurons); the inferior colliculus has a gradient of tones ranging from low frequencies in the surface to high frequencies in the deeper areas, while the auditory cortex these regions are arranged laterally. For these reasons both regions have been targets for interfacing with the auditory system as individual audio frequency bands can be recorded/stimulated.



Figure 2.3: Tonotopic mapping of Auditory pathway regions: Simplistic representations of tonotopic maps in the primary Auditory Cortex and central Inferior Colliculys nucleus. These are merely examples to show how gradients can be in different structures, and are not to-scale representations and do not incorporate non-linearities. Taken from (5) with permission.

### 2.2 Studying neural function

The study of neural function is an established yet still growing field, with many techniques for the observation of a neural population's activity available, the main techniques being electrophysiology recording, electrochemical recording and optical recording. These techniques operate under differing mechanism and so each offers distinct strengths and weaknesses in terms of spatiotemporal resolution, specificity and recording volume.

#### 2.2.1 Electrical recording

Electrophysiology is a technique which examines neural activity by recording the extracellular electric fields. Electrodes are utilised to detect the electric potential arising from the superposition of all ionic processes within its vicinity. Many processes contribute to the origin of these electric fields including; action potentials, calcium spikes (calcium channel mediated signals can produce long lasting, large amplitude potentials) and synaptic activity (inflow of  $Na^+/Ca^{2+}$  ions from the cytosol into cells during cellular excitation, and the resulting charge balancing return  $\operatorname{current}(6)$ . Extracellular action potential produces microvolt scale signals with high frequency components (up to 10KHz range see Fig 2.4). The electrical characteristics of neural tissue attenuates electrical signals with low pass filtering effects (modelling studies have suggested this low-pass filtering effect may originate from the intrinsic filtering effect of the neuron's structures (e.g. low pass filtering from dendrites(7), separation of the current  $\frac{1}{2}$  sink/source (8)) or as a result of an inhomogeneous extracellular medium(9)). The amplitude of the extracellular action potential has been approximated to attenuate with exponentially scaling factor  $e^{-r/r_0}$  (where  $r_0 \approx 18-28 \mu m (10)$ ))<sup>1</sup>, note these scaling factors are derived from measurements and so incorporate the filtering above. These factors mean the spatio-temporal resolution of recording electrodes is highly dependent on the distance of the neuron to the electrode, with close proximity recordings providing most detail.

Electroencephalogram (EEG) and electrocorticography (ECOG) recordings utilise large electrodes placed sparsely on top of the skull/brain, which are used to sense voltages from thousands to millions of neurons across a large volume. These provide information on the activity of neural ensembles, however, due to the poor signal transduction to recording sites, the individual neural information is lost. These techniques offer a non/minimally invasive approach to electrical recording and demonstrated clinical usage. However, to accurately determine the activity of individual neurons, invasive neural recording techniques (such as patch clamp and microelectrodes) are required. Patch clamping offer the gold standard of cellular electrical recording; precisely detailing the electrical state of the neuron. This technique uses hollow pipettes to directly record the intracellular potential, either through directly contact or penetration of the neuron cell membrane. Unfortunately, due to the complexity of this procedure it is not feasible for recording large numbers of neurons simultaneously; which, paired with inconsistent success rates(14), make patch clamp techniques unsuitable for wide-scale circuit analysis. Automation of patch clamp recording removes the necessity for manual operation(15) but is still met with low success rates ( $\approx 32.9\%$ )(16). Extracellular recording on the other hand offers rich detail of the electrical state of the local neu-

<sup>&</sup>lt;sup>1</sup>The extracellular action potential amplitude's decrease across the electrodes of a tetrode/electrode array was measured corresponding to a  $r_0$  of  $\approx 28\mu m$  - (11),  $\approx 28\mu m$  - (12). Measurement constrained modelling of extracellular action potential yielded an  $r_0 \approx 18\mu m$  (13).

rons in millisecond detail, while providing access to larger recording volumes and more straightforward experimental procedure.



Figure 2.4: **Recording electrodes.** Relative placements of recording electrodes and their typical properties of signal of interest. a) EEG scalp recording setup(17) b) ECOG array recording(18). c1) 10x10 Utah electrode array (19) c2) Multishank Michigan array(20). c3) wire electrode (not shown). Signal amplitude and bandwidth of neural signals graph derived from (21). Head outline derived from (22).

#### Electrical Recording: The electrode-tissue interface.

As mentioned prior, charge carriers in a neural tissue are the mobile ions in an aqueous medium, however, in the metal tracks of an electrode the charge carriers are electrons. When a metal electrode is inserted into neural tissue an electrode/electrode interface is created, arising from the difference of two phases of conduction. Electronic charge densities on the surface of the electrode are balanced by the distribution of oppositely charged ions from within the electrolyte.

The Helmholtz model describes the electrode-tissue at its simplest, interpreting the interface as a charged metal electrode interfacing with a layer of oppositely charged ions. Further interpretations (Gouy-Chapman model) incorporate the diffuse layer, a region where the charge density of the analyte is determined by the balance of electrostatic attraction of ions towards the electrode with the diffusion away from the electrode surface due. The Gouy-Chapman model was further improved by Stern, to account for the finite radius of the ions present. These models describe the interface with capacitive behaviour, storing energy in the electrostatic field between opposite charges. For further explanation on these three models see chapter 13 of (23).

The electrode-tissue interface has been represented by numerous electrical equivalent models which attempt to take into consideration the capacitive/resistive nature of the interface(24), (25). Such models share a common feature of a parallel capacitor and resistor pairing representative of the capacitive double layer and charge-transfer resistance. The charge transfer resistance is a material dependent resistivity. The implications of this circuit is that the electrode has a non-linear impedance, highest at low frequencies.

#### Electrical Recording: Advances in microelectrode technology

Extracellular recording using micro-electrode arrays (MEAs) is ubiquitous in neuroscience and was originally achieved using metal wire electrodes. However, the advent of semiconductor micromachining techniques provided the capability to develop highdensity MEAs; in particular two probes designs were developed, the Michigan probe (1970s) (26) and the Utah array (1980s)(27). These designs offered high density and high channel count recording sites with precise geometries which could be manufactured at scale; these became the dominant blueprint of most probe designs and both are commercially available. The Utah probe uses a "bed of nails" configuration whereas the Michigan probe utilises a linear array of electrodes along a single probe shank. Since the inception of these devices, recording sites have seen an increase probe site and density, with probes containing hundreds of recording sites becoming common. The high electrode densities ( $\leq 50 \mu m$  pitch) of microelectrode arrays have enabled the development of a technique known as spike sorting which allows the deconstruction of the ensemble activity into the activity of individual neurons. On top of increased electrode density and count, recent advances in recording probes have made significant strides in the following themes: flexible shanks, incorporation of active circuitry and multimodality.



Figure 2.5: State of the art extracellular microelectrode arrays. (clockwise from top left) Ultraflexible neural probes (scale bar 10  $\mu$ m)(28); "Sea of electrodes", 7272 electrode array(29);Neuropixels CMOS electrode array(30); Mesh electrodes (scale bar 100  $\mu$ m). (31), (32). Neuralink system featuring 3,072 electrodes, inset shows custom recording IC(33).

The increase in recording site number, requires a similar increase in size and complexity of supporting electronics. Many groups have utilised complementary metal– oxide– semiconductor (CMOS) technologies for the incorporations of active electronics, including amplification and digitisation into the probe shank and body(34), (35). In addition to reducing size, this has also shown a reduction in power consumption: the Neuropixel probe provides up to 384 recording channels while drawing only 18.84 mW(36), which for the same channel count using a commercial recording IC (Intan) would require approximately 20x power.

Many of the probes mentioned before have been microfabricated in silicon, however, this and other inorganic substrates have stiffnesses much higher than neural tissue (Young's modulus: Silicon - 160GPa(37), neural tissue - 0.1-16 kPa(38)). The resulting mechanical mismatch paired with micromotion of the probe causes untoward stresses in the neural tissue which is hypothesised to increased immune response thereby reducing signal quality. Compliant probes have shown reduced immune response for chronic use in comparison to stiff silicon probes(39). These probes may require stiffeners to accurately target volumes during implantation, resorbable materials offer an attractive approach to this(40). Mesh electrodes using flexible electrode principles allow high count 2D recording array. The Neuralink system demonstrates a high channel count flexible electrodes (up to 3,072 electrodes/array, 50um spacing), this also demonstrates a push from commercial bodies into the neural interfaces market(33).

Human-computer interfaces have been developed using implanted microelectrode arrays (Blackrock Neurotech's Utah array is currently the only FDA approved chronic, penetrating MEA). Research from the Braingate, has demonstrated restoration of communication in medical trials; user intention could be inferred from motor cortex recording, which was then used to control a Bluetooth linked tablet computer(41). Fast calibration

#### 2.2.2 Electrochemical recording

Electrochemical sensing techniques can be used to evaluate levels of neurotransmitter in extracellular fluid, a secondary indicator for neural activity(43)(44). A common technique is Fast Scan Cyclic Voltammetry (FSCV) which allows the measurement of neurotransmitter concentration. FSCV applies a cyclic ramping potential to an electrode, and the resulting current is observed; peaks in the current indicate presence of reduction and oxidation at the electrode surface, which can indicate the presence of an electroactive molecules (e.g. dopamine and serotonin). Surface treated electrodes can increase the range of substances detected by FSCV, including non-electrically active molecules (e.g. glutamate and glucose). FSCV is a relatively slow technique with scan rates of  $\approx 100$ ms, and high channel recording is seldom used in part due to the complexity in instrumentation required(45). Similar molecules (e.g. serotonin and dopamine) may produce similar results, reducing this techniques selectivity, limiting the effectiveness of the technique.

#### 2.2.3 Optical methods

Optical methods for mapping neural activity can provide widespread recording of neural activity over large volumes while providing high spatial resolution (sub-cellular ( $<2\mu m$ ) resolution across wide areas is frequently observed (46), (47). Many of these techniques rely upon activity indicators, (such as indicator chemical dyes or Genetically Encoded Activity Indicators (GEAIs)), whose optical properties change in response to cell activity; including intracellular calcium transients(48), synaptic neurotransmitter release, and membrane potential (49). Most GEIA's have activation/disactivation kinetics in the ms range(50), and so therefore changes in neural activity are only be observed at relatively low sampling rates (in comparison to the sub-millisecond resolution achievable with electrical readout methods)<sup>2</sup>. Efforts have been made to improve the temporal response of these methods, in response voltage indicators have been developed with fast on/off kinetics able to track single action potentials(51) and even pulse trains up to 100Hz(52). GEAIs are seeing increased use over their chemical counterparts, due to the longevity and selectivity for neural subtype(53)(54). Imaging with activity indicators commonly utilises a change in fluorescence, which requires an excitation source for imaging; high photon energy light (high frequency light) is required to excite the fluorescence, which can be from two or three photon sources for improved in resolution (however, this is limited to a penetration depth to  $\approx 1$  mm). Due to the size and complexity of the optics required, most optical readout systems operate head-fixed procedures. Fibre photometry offers a streamlined optical approach for the recording of bulk neural signals, using a single fibre optic for both transmission and reception of the excitatory/ optical signal, allowing for freely moving tethered procedures (55). A similar approach using photodetectors paired with a  $\mu$ LED source has enabled wireless observation of neural dynamics (56). Techniques such as skull thinning and cranial window techniques have enabled visualisation of deep neural activity without damaging the observed tissue, offering a less invasive option to microelectrode recording (57).

 $<sup>^{2}</sup>$ Readout setup can also hinder sampling rate, for example certain methodologies rely on scanning to target recording areas which will be limited by the speed of the focusing/scanning hardware(46).

### 2.3 Neural perturbation

The ability to examine a neural response gives invaluable insight into the workings of neural circuits which, when paired with the ability to influence these neurons, becomes a powerful tool for the investigation of neural circuits. Neurons communicate through electrochemical mechanisms: information is passed within the neuron electrically, mediated through the movement of ions. This electrical signal is then translated to chemical/electrical messaging at the synapse, through the action of neurotransmitters. To perturb the neurons, we can influence these two methods of signalling.

#### 2.3.1 Pharmacological stimulation

Pharmacological stimulation works by influencing the release/uptake of neurotransmitter or the blocking/exciting of membrane proteins to illicit certain responses (inhibition, excitation) within the neurons. Due to different neural subtypes, certain neurotransmitters or receptors can be blocked/released using chemicals, offering selectivity. Unfortunately chemical modulation has poor temporal kinetics, widespread effects, and poor spatial confinement(58), (59). Electrical stimulation on the other hand offers control of neural activity with temporal dynamics matching those of neural firing.

#### 2.3.2 Electrical stimulation

Electrical stimulation is one of the most prevalent methods of interacting with neurons, and uses electrodes to inject/extract charge thereby influencing the activity of neurons. Multiple electrodes are utilised, with at least one being a working electrode (the electrode that applies stimulation) and another being the return electrode (which is used to complete the circuit). The amount of charge transferred to neural tissue must be balanced to prevent irreversible faradaic reactions which can cause damage to both the tissue and electrode(60). Charge balancing is simple in current controlled stimulation systems, as the net charge is just the integration of stimulus amplitude with respect to the stimulus pulse duration; however, in voltage mode stimulation the total charge transfer is dependent on the impedance of the stimulation-return circuit and therefore hard to control(61).

Cathodic current stimulation has been found to be more efficacious than anodic stimulation for neural recruitment(62). A cathodal current draws positive ions to the electrode and supplies electrons the tissue. When a cathodic current is applied to the working electrode, a redistribution of charge occurs which acts to reduce the extracellular potential surrounding the electrode. As the extracellular potential reduces, the intracellular potential becomes less negative in comparison, depolarising the cell. If sufficiently stimulation is applied, this will elicit an action potential from the neuron.

As the distance (r) from the electrode increases the required current ( $I_{th}$ ) to invoke stimulation increases accordingly with the following relationship (63) (Equation 2.1). This relationship shows that even neurons in the immediate vicinity requires certain threshold for activation ( $I_0$ ). Both  $I_0$  and K are dependent on wide variety of factors including the electrical characteristics/geometries of the neuron, the neuron's orientation/position compared to the electrode(64) and can also be influenced by anisotropy/inhomogeneity of the conducting medium(65)<sup>3</sup>.

$$I_{th}(r) = I_0 + Kr^2 \tag{2.1}$$

<sup>&</sup>lt;sup>3</sup>A highly anisotropic/inhomegenous conducting medium will be expected given that the electrode will be surrounded by a matrix of interstitial fluid and membranes.

#### CHAPTER 2. BACKGROUND

Electrical stimulation is able to perturb neurons with high temporal (sub millisecond latency of stimulation to spiking(66), reversible effects. For this reason, electrical stimulation is readily adopted by neuroscience for the investigation of neural circuits. Electrical nerve stimulation is also seeing increased use outside the neuroscience laboratory setting; two of the most notable of which have been the cochlear implant and deep brain stimulation for treatment of Parkinson's disease (PD). The cochlear implant is the most widely adopted neuroprosthesis, with more than 300,000 patients worldwide (as of 2015); many of whom have been able to regain significant levels of hearing. Deep brain stimulation (DBS) has repeatedly shown tremendous success in the treatment of tremor in PD patients, indicating the viability of intracranial neurostimulation's role in a clinical setting. Indeed neuroprospheses are expected to play a greater clinical role in the future with neural stimulation showing promise for the treatment of neurological disorders (including OCD, depression and epilepsy) and restoration of senses (retinal implants, and inner-brain auditory implants). However, efforts to determine the exact mechanisms underpining many of these treatments are hampered by the varied actions of electrical stimulation.



Figure 2.6: The varied mechanisms of electrical stimulation. The diverse microenvironment of an electrode, paired with the spread of the electromagnetic field can produce varied responses to stimulation. Image from (67). AP refers to action potential.

Electrical stimulation alters the potential of the volume meaning any electrically excitable cell within this volume may be influenced (including non-targetted cells). Secondly the effect of this stimulation on a specific neuron is dependent on the electromagnetic field that this neuron experiences. Due to inhomogeneity of the neural microenvironment, electrical stimulation has a wide and varied action within this volume (fig 2.6) including(67): lack of cellular selectivity, high dependence on the cell's

position and orientation in the electric field and the cells size to name a few.

### 2.4 Optogenetic stimulation

Optogenetics is a relatively novel neuromodulation technique which is finding increasing use in neuroscience experimental procedure. The technique utilises genetic modification of cells to express light activated channels/pumps known as opsins which activate upon illumination; altering the cell potential to bring about excitation/inhibition with millisecond control(68), (69). The inclusion of a genetic modification component in this technique offers distinct advantages and disadvantages for neuroscientists over other stimulation methods. On the one hand, optogenetic's genetic targeting provides specificity while maintaining temporal resolution similar to neuronal firing; however, this comes at the cost of requiring viral transfection/creation of transgenic animal lines, not to mention the challenges which will need to be overcome before this technique can be translated to the clinic.

#### 2.4.1 Mechanism

Optogenetics relies on the introduction of an opsin into the host cells. Opsins are a super family of light responsive transmembrane proteins. As described before, an excitatory cell's transmembrane potential can be influenced by the influx or expulsion of ions through the membrane. Similarly, opsins pass ions across the membrane, however, unlike the native chemical/voltage dependence of our neuron's gates/channels, these are gated by light. Three significant families of opsins used in optogenetics are:

- Channelrhodopsin: a cation channel, the most notable variant of which is ChR2. When illuminated, this protein undergoes a conformational change and draws cations (H+/ Na+) into the cell, causing depolarisation and increasing the likelihood of neuronal firing.
- Halorhodopsin: is a chloride pump into the cellular membrane, which when illuminated hyperpolarises the cellular potential hereby decreasing the likelihood of neuronal firing.
- Archaerhodopsin: a proton pump which expels H+ during illumination. This hyperpolarises the neuron reducing firing rate.

The opsins that make up these families provide four major categories of action: fast excitation, fast inhibition, step function modulation, and intracellular neural signalling modulation, each with diverse range of characteristics (including activation wavelength, photocurrent and temporal kinetics)(70). Different opsins may be co-expressed, allowing both light activated inhibition and excitation of neurons(71), (72), however, the absorbance spectrum of these opsins are broad and may overlap creating crosstalk in two opsin systems.

These opsins however, are non-native to mammalian cells, originally identified in algae and require a method of introduction into the cells. Genetic modification alters the genetic code of the host cells to express the desired proteins. This technique begins by isolation of the target gene, which is then introduced into a vector. The vector infects the host cells, reprogramming the nucleus' DNA to produce the viral protein. Modified viruses have been developed for a variety of animal models; including mouse, non-human primates. This approach can be achieved by either injection of the altered virus into the host brain or creation of transgenic lineages by transduction of a fertilised nucleus. Genetic modification allows alteration of the viral protein to tailor the opsin expression towards preferred characteristics, e.g targeting proteins have been added which develop soma expressing opsins, reducing crosstalk from neurite presentation(73), (74).

#### 2.4.2 Light delivery

Optogenetics offers a variety of attractive benefits over conventional electrical stimulation however, light is not native to the brain, and thus in order to capitalise on these benefits instruments to illuminate the brain must be used. Surface illumination can be used to excite the outer layer of neurons; however, due to the attenuating and dispersive optical properties of tissue this technique is insufficient when targetting deeper volumes of neurons. Three distinct families of optogenetic stimulating techniques have been developed with the capabilities to illuminate *deep* areas of the brain; optical guiding, multi-photon illumination and optoelectronic probes. Each of these techniques has its own benefits and drawbacks associated with the technology.

#### **Optical Guiding**

This technique includes optical fibres and waveguides, and revolves around the idea that light can be transmitted from an external source through an optically constrained conduit to the target volume. Optical fibres are commonplace among neuroscience labs, aided by their relatively straight forward fabrication and experimental setup. Furthermore, the light wavelength is only limited by the external source, so it can be tailored to the opsin in use(75). The use of a distant light source means no active circuitry is inserted into the brain, benefiting chronic stimulation.

Multi-site illumination is not commonly achieved with optical fibre setups, due to the high volume displacement of multiple fibres. However, recently tapered fibres have been introduced, the reduction of fibre diameter causes out-coupling of higher order modes, offering some control of illumination depth(76) (this is demonstrated in fig 2.7 panel B; by changing the light's input angle from 6 degrees through to 35 degrees, the light outcouples from varying depths across the fibre taper). High channel multisite illumination has been demonstrated using a microfabricated glass needle array, modelled on the Utah MEA, allowing numerous optical stimulation sites, with both superficial and deep illumination(77). Microfabricated waveguide devices have enabled development of low cross-sectional area probes with the added benefits of microfabrication (scalability, bulk fabrication).



Figure 2.7: **Optical guiding optogenetic devices:**a) Penetrating optrode array (78) b) tapered fibre optic(76), c) integrated waveguide and electrode optrodes,(75) d) multifunction optical fibre with wave guiding, electrodes and micro-fluidic channels (79) e) wave-guiding glass Utah electrode (77).

Due to high propagation and coupling losses exhibited by some of these devices (Examples of high loss: 9.96 dB -(80),15.6dB - (81),  $\approx$ 22dB - (82), 13dB - (75)), optically guided approaches may require relatively high power light sources, the hardware of which is generally bulky and power consuming. Laser diodes and  $\mu$ LEDs have been incorporated into such devices to offer a compact solution, but electrical power required to drive such circuitry remains in the high tens of mW which will hinder wireless use and may pose issues with tissue heating (even though the power source is distant there heat is still transfered through the probe-shank (80)). Microfabrication techniques allow the straightforward pairing of waveguide probes with electrodes, and optical fibres have incorporated recording sites either through; coupling with a pre-made Utah/Michigan array or during fibre fabrication(79).
#### Multi-photon illumination

Single photon optical stimulation can be used from conventional light sources (e.g. arc-lamps), and is indeed used when surface stimulation is required. However, these methods may stimulate neurons outside of the focal point, two photon illumination offers restriction of optical excitement. When two photons of lower frequency are simultaneously incident they may provide enough energy to excite an opsin. This principle offers a great advantage as high wavelength light can be used to stimulate visible light opsins. Visible light has a high attenuation rate in neural tissue, however, near IR has a much lower attenuation and scattering coefficients; and so two photon techniques pass further through tissue. The conditions for two photon excitement are stringent, and only a small percentage of the incident photons are able to activate the opsins; this small excitation volume offering high spatial specificity. Furthermore multisite illumination systems can be developed using spatial light modulation, allowing arbitrary volumes of tissue to be selectively stimulated (83). This technique can be paired with activity indicators to develop all-optical systems capable of both recording and stimulation (84). Unfortunately, this technique is limited by the scattering of light in tissue, and optogenetic stimulation is only acheivable at depths up to a few hundred of microns(85).

#### **Optoelectronic Probes**

Unlike the other two techniques mentioned prior,  $\mu \text{LED}$  probes generate light at the point of stimulation. There are generally two approaches to this technique, monolithic  $\mu$ LED probes where the probe is developed using the LED substrate(86),(87),(88),(89) or transfer printed where the contact wires are microfabricated and a  $\mu$ LED is transferred onto the device(90), (91). Both approaches utilise  $\mu$ LEDs which can be arranged to create multiple illumination sites over widespread regions. Microfabrication techniques used in the manufacture of these devices allows the flexibility of probe design, providing: electrode incorporation, inclusion of temperature sensing elements and transfer printing of other active components (92).  $\mu$ LEDs produce light directly at the point of stimulation, and therefore do not experience significant propagation losses (excluding IR drops due to trace resistance) and benefit from low power requirements (to produce similar output irradiance a  $\mu \text{LED}(86)$  requires  $\approx 3.5 \text{mW}$  input electrical power in comparison to 120 mW for a LD driven waveguide(80)), facilitating wireless stimulation designs. However, this light generation causes device heating which can lead to tissue damage and restrict experimental protocols. Furthermore, inserting active circuitry into the brain (a notoriously difficult environment for electronics) means that impermeable passivation layers are imperative.



Figure 2.8: **Optoelectronic optogenetic devices:** (clockwise from top left) 96 channel high density  $\mu$ LED array (86); multichannel LED with incorporated electrodes(89); flexible  $\mu$ LED array(93); multi-function optrode with incorporated temperature sensor and photo-diode(92); schematic of a CMOS mini-LED optrode<sup>5</sup>(91).

#### 2.4.3 Limitations of light delivery

Unfortunately, transmitting light through neural tissue is constrained by physical limitations and unwanted physiological effects; frustrating current optogenetic techniques. The penetration depth of light in the brain is determined by the scattering and absorption of light within this material. Opsins' absorbance spectra are predominantly in the visible light spectrum which unfortunately exhibits strong scattering and absorption in neural tissue. This is further exacerbated by the emission profile of the light source; (e.g. due to the Lambertian emission profile of  $\mu$ LEDs, the intensity intrinsically reduces with increased distance from the source). Fast attenuation of illumination requires higher intensity illumination to ensure volumes are at/above threshold illumination; however, this may produce local tissue heating, impacting the stability of the neural tissue. Light induced temperature increases have been demonstrated to cause altered firing rates of non-opsin expressing neurons (94), (95) and higher temperature increases are known to damage neural tissue. This effect limits optogenetic experiments by restricting volume of illumination and stimulation durations. Simultaneous stimulation during recording can induce artifacts onto recording channels. These artifacts are generally much larger than the signal of interest, and may lead to signal loss and amplifier saturation. Artefact coupling on recording electrodes can occur during optogenetic stimulation due to multiple means:

• Electromagnetic crosstalk: This interference derives from the interaction between the electromagnetic fields of driven electrical circuits (e.g. LED/LD drivers) and

<sup>&</sup>lt;sup>5</sup>Classification of small scale LEDs is somewhat nebulous, in this publication miniLEDs are those with dimensions in the 100  $\mu$ m to 500 $\mu$ m range,  $\mu$ LEDs are sub 100 $\mu$ m range dimensions. Nanoleds are also being developed with sub-micron scales

recording circuitry.

• Photoelectric effects: The generation of a current/potential on an electrode in response to light.

Electromagnetic artefacts are proportional to the rise-time of the signal, which may limit the illumination protocol to low frequency stimulation patterns. Efforts have been made to reduce these artefacts, including shielding and pulse-shaping.

## 2.5 Optogenetic hardware

Penetrating optical neural probes (wave-guiding and  $\mu$ LED probes) require external electrical hardware for their operation. Laser coupled systems require complex driving circuitry; consequentially few custom laser driver ICs have been developed(96), the majority of laser coupled systems relying on commercial off the shelf (COTS) parts or benchtop systems. LEDs have much lower driving requirements and can be controlled by a variety of sources. COTS LED drivers are ubiquitous, however, most of these have been designed for the lighting/display industry and therefore offer the following disadvantages:

- Pulsewidth modulation (PWM) dimming instead of constant current.
- Low channel count.
- High (10mA-100mA) current source/sinking.

Programmable voltage/current DAC sources provide a strong contender for LED driving with COTS components as these offer high channel (>=16 channels), high resolution (>=12bits) electrical control (e.g. AD5767BCPZ-RL7). Custom CMOS integrated circuit have been developed for LED sources, with characteristics aligned with the needs of optogenetic stimulation with a small package. These ICs are mainly current sources with wide voltage swing to accommodate the exponential rise of the LEDs current/voltage (IV) characteristics. High current sourcing ICs have been developed with high illumination, LED coupled optical guiding probes in mind(97); both designs are PWM controlled and feature low channel count.  $\mu$ LED probes do not require as high driving capabilities, and as such custom ICs are mainly driven by high channel count and stimulation resolution (98), (99). CMOS fabrication is a powerful technique through which many silicon electrical circuits are manufactured, and many custom optogenetic stimulator ICs have incorporated multifunctional capabilities, including: recording, probe diagnosis(100). CMOS integration also enables dense packaging of electrical circuits, benefiting the translation of optogenetic hardware from benchtop systems to wireless.

## 2.6 Wireless Optogenetic systems

Tethers are common in optogenetic experiments: optical fibres providing illumination, wire providing electrical signals for stimulation power and recording signals. These tethers impose limitations on the experimental protocol: the animal must be habituated with the head stage, restriction of natural animal behaviour, expensive equipment such as commutators. Multiple wireless optogenetic systems have been developed, tackling these issues and offering freely behaving animal experiment.



Figure 2.9: Wireless optogenetic devices : (clockwise from top left)NFC powered wireless LED system (90); multimodal chemical and optogenetic stimulator (101); wireless recording/stimulation system with 32 optical and 32 readout channels (102); Plexon Helios system(103), (104); wireless LED stimulator (105) close loop wireless system (106).

Both optical guiding and micro-led probes have seen adaption into wireless designs. Two main neuroscience hardware suppliers offer wireless optogenetic headstages; the Helios from Plexon and the Teleopto from Teleopto, a similar system is available open source from Cerebro. These systems have similar operating principles: battery powered, optical fibre coupled with a laser diode/LED source and communication through IR. Numerous research groups have developed wireless systems with a wide spectrum of device characteristics. Powering wireless optogenetic devices provides one of the most difficult challenges faced during these designs, as the weight of the battery alone can be a significant percentage of a small animal's bodyweight. Batteries provide sufficient energy capacity to support complex wireless systems, capable of electrical recording and transmission, high channel count or multimodal neural perturbation. Gagnon-Turcotte and colleagues (102) presents one of the more complex wireless battery driven optogenetic systems featuring; 32 optical sites, electrical recording, compression and transmission of neural recordings of 32 channels and FPGA control (fig 2.9). Stimulation is achieved by LED coupled fibre optics powered by two CAT4016 LED drivers, capable of on/off control of a fixed illumination. The PCB board size required to accommodate a system is quite large, with dimensions 17x18x10 mm3 (without battery) and weighs 4.9g. The system is powered by a 3.7V, 110mAh LiPo battery, drawing 175mW during 10% duty cycle optical stimulation. Multiple battery-free wireless optogenetic devices have been demonstrated, wirelessly powered by inductive coupling or RF sources. The removal of the battery allows for significant reduction in weight and scale and removes the need for recharging, enabling full implantation of the system and chronic use. An example by Shin et al demonstrated flexible microfabricated systems with transfer printed  $\mu$ LEDs powered and controlled by inductive means (90). More

recent iterations from this group incorporated complicated electronics, including power regulation and a microcontroller for control of multiple  $\mu$ LEDs and amplitude control. There are drawbacks to reliance on wireless power supply, namely antenna size, tissue heating, sensitivity to alignment and low transmission distances from source. Wireless power transmitting in these devices is restricted to a few mW, sufficient for single  $\mu$ LED illumination, however, this restricts the system complexity and is unsuitable for high power illumination systems.

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## Chapter 3

# **Background: Device Physics**

#### 3.1 Microled Physics

The optoelectronic probes detailed further in this thesis are semiconductor devices, the underlying physics of which is extensively covered in literature. "CMOS Electronics How it works, how it fails" by Segura & Hawkins (1) offers a good introduction to semiconductor physics, including the origins of the semiconductor conduction and the p-n junction. "Light emitting diodes" by Schubert (2) provides depth on LED specific physics, namely recombination and efficiency, and information on their optical and electrical characteristics. "Nitride Semiconductor Light-Emitting Diodes (LEDs): Materials, Technologies, and Applications" by Huang, Kuo and Shen (3) offers detail into III-Nitride LEDs including the technologies used to develop these materials and improve efficiencies.



### **3.2** Solid state physics: band theory

Figure 3.1: **Band theory** Left) representation of development of the energy bands in multi-atom solid, right) energy band gaps in insulators, semiconductors and metals.

The orbital of the electron is linked to its energy; low energy electrons inhabit lower orbitals than high energy electrons. In a single atom the electrons exist at distinct orbitals, and therefore the atom's electrons exist at discreet energy levels. In two-atom systems, the exclusion principle prevents two electrons from inhabiting the same orbit; to accommodate this, the allowable energy level of the system's electrons separate. Continued accumulation of atoms causes further splitting of the energy states that the electrons may exist in. For this reason, unlike the single atom, electrons in solids may possess a range of allowable energy states known as energy bands.

Low energy bands are strongly attracted to the atom's nucleus and do not take part in interactions, and therefore the high energy bands (the valence band and the conduction band) are of most interest. The conduction band comprising of electrons with the highest energy states and is populated by electrons with sufficient energy and freedom to be mobile charge carriers. Electrons inhabiting the valence band also have high energy, however, these electrons are shared by atoms during bonding and are no longer free charge carriers.

The energy difference between the valence and conduction bands is known as the band gap, and this paired with abundance of electrons comprising these energy bands describes the electrical properties of solid state materials; which are divided into conductors, insulators and semiconductors. Conductors do not have a band gap, due to overlapping of the valence and conductance band; providing an abundance of free charge carriers and permitting the flow of current under an applied electric field. On the other hand, an insulator's band gap is sufficiently high that electrons cannot readily be excited from valence to conduction band. All electrons within an insulator inhabit the valence band and so these materials lack free charges; thereby restricting the flow of current in response to an electric field. Semiconductors have a smaller bandgap, and thermal energy alone is sufficient to excite some valence electrons to the conduction band.

When the electron leaves the valence band, an empty state is generated in the valence band. This empty state can be filled by a surrounding electron and in doing so will generate a further empty state. The empty state is known as a hole and will act as a positive charge carrier, moving in the opposite direction to the electron current. In intrinsic semi-conductors (i.e. pure semi-conductor crystal lattices) holes and electrons are generated simultaneously, therefore these materials have equal concentrations of holes and electrons

## 3.3 Semiconductor doping

Semiconductor carrier concentration can be modulated through the inclusion of impurities into the intrinsic semiconductor. Hole concentration can be increased by the inclusion of lower valence atoms, electron concentration can be increased through the inclusion of higher valence atoms. This is easily demonstrated on the doping of valence four semiconductors (such as Silicon); inclusion of valence 5 elements (e.g. Arsenic or Phosphorus) produces an excess of electrons in the area increasing the electron concentration, while inclusion of valence 3 (e.g. Boron) elements has the opposite effect increasing the hole concentration (see fig 3.2).



Figure 3.2: Semiconductor Doping a) representation of a valence four lattice (for example, Si which is the most ubiquitious semiconducting material), b) p-doped semiconductor, with hole from receiver atom, c) n-doped semiconductor with spare electron from donor atom.

## 3.4 PN Junction

The p-n junction is the fundamental basis of all semiconductor devices and arises when p- and n-type materials are joined. The joining of these materials develops a large density gradient of mobile charge carriers (electrons and holes). Diffusion of these charge carriers occurs; spreading electrons into the p-type material and holes to the n-type material. The mobile charges recombine creating a region which is devoid of free charges, known as the depletion region(1). Within this region, the dopant atoms having lost/gained electrons are now ionised, which in turn creates a charge separation. This charge separation develops an electric field. The intrinsic potential of the p-n junction, known as the built in voltage, acts as an energy barrier which opposes further diffusion across the p-n junction.



Figure 3.3: **The p-n junction.** Left) Creation of the p-n Junction: i) initial conditions (note in reality such a structure would not exist) ii) diffusion of mobile carriers iii) development of electric field and built in potential. Right) Electrical properties (Charge, electric field strength and potential) across p-n junction.

The depletion region, now devoid of free charge prevents the further flow of current. By forward biasing the pn junction (i.e providing a positive potential to the p-type material), the electrons are attracted and the positively charged holes are repelled, decreasing the width of the depletion region. With application of a sufficiently large potential, the electric field of the depletion region can be overcome, allowing current flow across the junction. Above this potential, the junction has low resistance; freely letting current flow. Alternatively, negative biasing the p-n junction causes the depletion region to widen, further preventing current flow.

The current-voltage (IV) characteristics of an ideal diode under forward biased conditions have been described by the Shockley equation(2):

$$I = I_s e^{\frac{e_V}{(n_{ideal}kT)}} \tag{3.1}$$

Where I is the current across a p-n junction for an applied voltage V.  $I_s$  is the saturation current (typically in the order of nA), e is the electron charge,  $n_{ideal}$  is the ideality factor, k is Boltzmann constant, T is the junction temperature. This relationship demonstrates the rectifying behaviour of the p-n junction i.e. under negative and low voltages there is very little current flow, but exponential current flow at positive voltages.

## 3.5 Recombination

During current flow across the p-n junction electrons and holes recombine and eliminate; releasing energy through radiative or non-radiative recombination processes. Radiative processes convert this energy to light with the generation of photons a phenomenon known as electroluminescence. The wavelength of light ( $\lambda$ ) produced is proportional to the energy released during the transition of the electron from conduction to valence bands (E):

$$E = hf = h\frac{c}{\lambda} \tag{3.2}$$

The radiative recombination rate is expectedly related to the availability of carriers, and is described in the following relationship(2):

$$R_{Radiative} = Bnp \tag{3.3}$$

where B is the bimolecular recombination coefficient, n is the electron concentration, and p is the hole concentration. However, not all hole-electron interactions produce light: non-radiative recombination may occur converting the electron's energy to phonons (quantized lattice vibrations). This process can occur through different mechanisms, including: recombination in deep level traps, Auger recombination (recombination energy is transferred from electron-electron or hole-hole without photon release) or carrier leakage (recombination outside of the active region)(2). These non-radiative processes compete with radiative processes for mobile carriers and the resulting inefficiency is non-ideal for LEDs. To maximise radiative recombination,  $\mu$ LEDs are made with "direct bandgap" materials (i.e those where the conduction and valence bands are aligned in k-space, and conservation of momentum can allow for recombination without the production of phonons).

## 3.6 Efficiency improving structures

The internal quantum efficiency of an LED (IQE) is determined by the competition of radiative processes (R <sub>Radiative</sub>) and non-radiative process (R <sub>Non-Radiative</sub>, including the Shockley-Reid-Hall recombination rate, Auger recombination, etc.), which can be summarised as(4):

$$IQE = \frac{R_{Radiative}}{(R_{Radiative} + R_{Non-Radiative})}$$
(3.4)

Therefore, the efficiency will be improved by increasing the radiative recombination rate and reducing the non-radiative recombination. Engineering of the layers which constitute the p-n junction can offer improvements in LED efficiency. In a homo-junction structure (i.e the p-n junction is made of differently doped regions of the same material), the charge carriers will diffuse far across the p-n junction; decreasing carrier concentration and therefore decreasing the radiative recombination rate. This diffusion can be restricted through the creation of heterojunction structures; p-n junction structures whose semiconductor composition changes abruptly over the length of the junction(5). Double hetero-structure heterojunctions confine charge carriers through the inclusion of a lower-bandgap material between the p-n junction, usually undoped creating a p-i-n region. At this region, both holes and electrons see a region of lower energy where they preferentially congregate. Another hetero-junction is the quantum well which provides a similar confinement of carriers, however, at a much smaller scale (nanometres). Higher band-gap layers inserted between the p-type/n-type layer and active regions may be used to further confine charge carriers. Electron blocking layers prevent carrier leakage of electrons into the p-type layer, and vice-versa for hole blocking layers.

## 3.7 III-V material LEDs

Compounds of three valence (Al,Ga,In) and five valence elements are commonly used to create semiconductors (known as III-V semiconductors). The LEDs demonstrated further are created using nitride compounds (AlN,GaN,InN) and their alloys. The IIInitride family of semiconductors supports a wide range of bandgaps from  $\approx 0.8$ eV (InN) to  $\approx 6.2 \text{eV}$  (AlN), spanning wavelengths from the near IR to extreme UV wavelengths(2) (for completeness GaN bandgap is  $\approx 3.4 \text{eV}$ ). Adjustment of the composition of these alloys, and therefore the active region's bandgap provides control of the LED's colour. The main III-V alloy of interest in this thesis is the InGaN alloy, whose spectrum of possible wavelengths extend from the near UV to the near IR, including the whole visible spectrum. Despite this range not all colours are equally straight-forward to realise; to date high efficiency blue and green InGaN  $\mu$ LEDs are widely produced however, higher wavelength LED fabrication requires increased In content and lower growth temperature which detrimentally effect crystal structure and ultimately efficiency deteriorates, frustrating red InGaN  $\mu$ LED development<sup>1</sup>(6).

LED semiconductor materials utilise a multilayer structure; grown using metalorganic vapour-phase epitaxy (MOVPE). However, MOVPE's high temperature operation limits the available substrates (silicon and sapphire being common examples, with sapphire being the most ubiquitous in industrial applications). Previous research has indicated that GaN on sapphire  $\mu$ LEDs are suitable for optogenetic stimulation(7), however, sapphire cannot be easily thinned to the desired thicknesses required for penetrating neural probes. Silicon on the other hand can be thinned to  $\approx 30\mu$ m, making it an ideal candidate for monolithic optogenetic probes. Unlike sapphire, silicon is opaque to visible wavelengths and manufactured LEDs must utilise top emission (i.e light is emitted through the top of the structure), necessitating optically transparent electrical contacts; commonly manufactured from: annealed Ni/Au, ITO and Ni/ITO.



Figure 3.4: Example GaN on Si LED structure. Adapted from (8).

MOVPE allows precise control of the optical/electrical/mechanical characteristics of each layer which are tuned to suit the requirements of that layer (an example stack for GaN on Si LEDs is demonstrated in fig 3.4)(8). Growing GaN on Si is advantageous (in that it can harness the power of silicon processing) but it is faced with challenges due to differing mechanical properties of the two materials. GaN's thermal expansion coefficient is lower than that of Si, which when cooled produces a tensile strain on the grown GaN; this strain can cause cracking or bowing of the wafers. Si has a cubic diamond crystal structure whereas GaN is a wurtzite structure, the lattice mismatch of

<sup>&</sup>lt;sup>1</sup>High efficiency red LEDs based on AlGaInP (the material used for the LEDs in Chapter 6) are well developed, however these suffer decreases in efficiency when scale is reduced.

these can further strain the epitaxal GaN. To reduce this strain several buffer layers are grown on the Si substrate prior to GaN growth, e.g. AlN which acts to help matching between the Si and GaN lattices(9).

## 3.8 AlGaInP based LEDs

While red III-V  $\mu$ LEDs are still in their infancy, red LEDs based on AlGaInP alloys are well developed. Together the binary structures of this material family (AlP,GaP,InP,GaAs) and their alloys have a bandgap ranging from 1.35eV to 2.45eV (corresponding to a spectrum ranging from green light to IR, across most of which there is a direct bandgap)(2). Typically AlGaInP LEDs are grown on GaAs substrates, which can be lattice matched to the grown semiconductor. AlGaInP LEDs suffers more from surface recombination (recombination at the edge/surface of the pixel, which does not contribute to emitted light) than the III-V materials shown above(10). This means that for AlGaInP LEDs the efficiency diminishes as the size decreases (as the surface area of the pixel becomes a larger relative to the pixel size). The AlGaInP LEDs discussed in Chapter 6 were acquired with the help of Dr. Erdan Gu through collaboration with a confidential company; therefore limited details of the epitaxial structure/fabrication of these  $\mu$ LEDs is provided.

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## Chapter 4

# **Background:** Microfabrication

## 4.1 Introduction

The creation of the micron-scale devices described throughout this thesis require precision which is only afforded to us by the use of various microfabrication techniques (described in this chapter). The microfabrication process relies on the development of stacked laminar features which are created through additive (deposition) or subtractive (etching) methods. To provide shape to these layers, photolithographic patterning is use to create a masking layer which prevents subsequent etching or deposition. Due to the nature of these device's small scale, most features are invisible to the naked eye and precise measurement tools are needed to validate manufacturing progress. Further reading on the techniques and processes involved in microfabrication can be found in (1), (2).

## 4.2 Photolithography

Photolithography is the method by which patterns are created in each layer of processing. This technique revolves around the use of a photosensitive chemical coating to mask areas from deposition or etching. The pattern is created by three main steps; resist coating, pattern exposure and development.

**Resist coating:** The sample is coated in a photosensitive chemical called photoresist. This is achieved normally through spin coating, dip coating or spray coating. Spin coating uses a rotating chuck to spread photoresist over the sample. The final photoresist thickness is determined by the viscosity of the photoresist and the rotational speed of the chuck. Baking of the resist coated sample helps remove solvent from the film prior to exposure. Photoresist adhesion can be improved through prior coating with adhesion promotors such as hexamethyldisilazane (HMDS), which can be spin-coated similar to photoresist.

**Exposure:** The second stage in photolithography is exposure where the pattern is transferred onto the photoresist by exposure to a UV light source. Masked photolithography (as is used in the processes below) illuminates the photoresist through a mask (a quartz glass sheet covered in metal according to the desired pattern). The mask's metal pattern shadows the underlying areas of photoresist, preventing their exposure to light. Alternative mask-less approaches can directly pattern the photoresist layers via a focused light source.



Figure 4.1: Key steps in the photolithography process. Samples are initially coated in photoresist using spin-coating. The samples are exposed to UV light using a mask aligner. The samples are developed revealing the desired pattern. Note the sidewall profile of the photoresist tones.

Two photoresist tones exist (positive and negative) contain photo-sensitive chemicals, which behave in opposite effects in response to light illumination:

- **Positive tone resists:** contain a photo-sensitive chemical which alters in response to illumination, becoming dissolvable in the developer. Thus shadowed areas in a mask are transferred during exposure. This resist produces inwardly side-profile after development.
- **Negative photoresist:** Upon illumination, the photo-sensitive chemical becomes insoluble. Therefore, in the negative tone resist, areas shadowed during exposure are unaffected and dissolve during development. The resist tones produce outwardly sloping photoresist walls.

The resolution of masked photolithography is limited by the wavelength of the light used and the separation of the sample and the mask. Improved resolution can be achieved through electron beam lithography or high resolution direct write lithography systems. Multi-pattern processes require alignment to ensure correct orientation of subsequent layers. To ensure the correct matching of subsequent stages, each mask uses alignment marks which allow for the positioning between the mask and sample features. This alignment can be achieved through a mask aligner (in this case the Karl Suss MA6); this machine coordinates the alignment and exposure process. Firstly, alignment of the sample to the mask is completed using a hand adjustable x/y/theta stage, the mask is brought into close contact with the sample and illuminated with a mercury lamp UV source. **Development:** After exposure, excess resist is removed by dissolution in a chemical developer. The development process can be controlled by a number of parameters including agitation, solution concentration and development time

#### 4.2.1 Lift-off

Photoresist can protect areas from etching or deposition. The process of protecting areas from deposition is called lift off, where an area is coated in photoresist to prevent subsequent material deposition. Later this photoresist is removed revealing an uncovered area. The inward sloping walls of positive tone photoresists are unsuitable for this technique as material deposition can completely cover such structures. Coverage of the photoresist can hinder lift-off quality by preventing solvent in-flow or creating vertical features of incompletely removed material, colloquially known as "rabbit ears". These defects can be detrimental to further processing; puncturing passivation layers, and can grow to larger defects during subsequent deposition processes. Special lift-off bilayer resists have been developed which improve lift-off through the development of re-entrant sidewalls. These profiles are created by a multi-layered photoresist method: an initial immiscible resist layer is deposited, on top of which the pattern-able PR layer is coated. During development this initial layer dissolves faster than the patterned PR, creating a re-entrant sidewall profile which is not covered during material deposition. Exposed photoresists facilitates the inflow of solvent, improving lift-off.



Figure 4.2: **Comparison of lift-off techniques.** Positive tones have inward sloping walls which can be completely covered during metalisation. This can lead to defects known as rabbit ears (ragged edges). The bilayer resist remedies this, by creating an overhang which prevents complete coverage by the metal. A SEM micrograph shows the overhanging profile of lift-off resists.

## 4.3 Etching

Etching is the process of removing material from a sample. Etching is facilitated by the chemical/physical interaction of the etchant with the specimen surface, and the removal of the subsequent reaction product. Key parameters in etching are:

- Etch rate: How much material is removed in a given time. High etch rates will allow material etching in user suitable timeframes, however the control over the removed thickness is lost. Low etch rates give great control over the total material removed however thick materials will require long manufacturing times.
- Selectivity: The ratio between etch rates of certain materials. Generally high selectivity between the etching material and other materials (e.g. masking layers) is desired.
- **Directionality:** Directionality is the extent of which the material is etched in certain directions, which helps determine the available aspect ratio. Isotropic etches have low directionality, etching in multiple dimensions (e.g. chemical etching of SiO<sub>2</sub> in buffered oxide etchant (BOE) is isotropic). Anisotropic etches preferentially remove material in one direction, providing etch profiles with steep sidewalls.

Etching can be split into two general terms; dry etching which relies on plasma to etch the target material and wet etching which uses wet chemicals (for common etch rates in these processes see (3), (4)).

#### 4.3.1 Dry Etching

Plasma etching uses plasmas to etch materials, the main dry etching methods used in this thesis rely on the same approximate process:

- 1. Reactive gasses are introduced into the vacuum chamber.
- 2. These gasses are excited to a plasma.
- 3. The plasma is driven to the substrate surface, the interactions between these etch the substrate material.
- 4. Etchant by-products are removed from the chamber.

Two main plasma etching techniques are utilised in this thesis; reactive ion etching (RIE) and inductively coupled plasma (ICP) etching (see (5) for further reading on dry etching).



Figure 4.3: **Plasma etching methodologies.** Comparison between the RIE and ICP apparatus.

#### **Reactive ion etching**

This etching technique uses reactive species to etch a target material and is the most frequently used etching process in the processes outlined ahead. Gas species are introduced into the vacuum chamber where they are ionised by a radio-frequency (RF) driven platen. The RF electromagnetic field excites the gas, creating a plasma containing reactive species (ions and free radicals). The plasma's free electrons are readily absorbed by the surroundings (due to the increased mobility of the electrons). The chamber walls are grounded; however, the sample platen is DC isolated using a blocking capacitor causing the platen to acquire a negative potential (V<sub>dc</sub>). The negatively charged platen repels electrons, creating a region known as the ion-sheath. Having lost electrons, the plasma takes on a net potential (V<sub>p</sub>). The potential difference between the plasma and the platen (V<sub>p</sub>-V<sub>dc</sub>) drives the reactive species from the plasma, across the ion sheath, into the target.

The etchant species must cross the ion sheath to etch the material; collisions within this sheath can determine the directionality of the etch, which in turn is effected by contributing factors such as ion sheath thickness and process pressure. These reactive species etch the target material through chemical reactions, physical etching via ion sputtering or ion-assisted etching (a combination of ion sputtering and chemical reactions which has improved etch rates than each individually). Chemical reactions occur when reactive agents adsorb onto the material surface, reacting with the surface material, the by-products of which are volatile in the chamber conditions and desorb from the wafer surface. Ion sputtering on the other hand is a purely physical process where material forcibly ejected by the impact of high energy ions colliding with the surface material.

#### Inductively coupled plasma etching

Similar to RIE, ICP etching utilises plasma to etch substrates. The ICP uses a coil driven by an RF source. The coils magnetic field inducts an electric field within the chamber, creating a plasma. This plasma is a much higher density than RIE, which paired with a reduced ion-sheath size can facilitate faster etch rates with increased anisotropy.

#### 4.3.2 Wet etching

Wet etching relies on chemical reactions to etch the material and therefore the etch properties are material and structural dependent. As a result, wet etches can provide high selectivity between different materials. Wet etches are generally isotropic etches, however certain etches result in directional etching (e.g. the preferred etching of the <100> crystal plane orientation during KOH chemical etching of Si). Wet etching has not been utilised significantly within the processes outlined later.

## 4.4 Deposition

Deposition techniques provide a method to create thin films on the surface of a sample. These techniques can be split between CVD (chemical vapour deposition) where the film derives from the reaction of chemically reactive precursors onto the surface, or by PVD (Physical Vapour Deposition) whereby the thin film is developed by transferral from the surface of a solid target material. The most common techniques used within the cleanroom are: PECVD for dielectric passivation layers, evaporation/sputter coating for metallisation and Parylene-C coating for conformal passivation layers.

#### 4.4.1 PECVD

Plasma enhanced chemical vapour deposition (PECVD) is a process whereby a thin film of material is developed on the substrate's surface from the reaction of volatile precursors. Precursor gasses are excited by RF fields creating a plasma. Driven to the substrate surface by an electric field, these volatile components adsorb onto the surface. The components react producing a solid phase and gaseous by-products which are removed under vacuum. PECVD within this thesis is mainly used for the creation of silicon dioxide passivation layers/hard masks; created by the decomposition and reaction of silane (SiH<sub>4</sub>) and nitrous oxide (N<sub>2</sub>O).

#### 4.4.2 Sputter deposition

Sputter deposition of a material is achieved by the accumulation of material released by ion bombardment onto a target material. Argon gas is ionised; the charged ions are driven towards a target material by an electric field. Material is ejected from the target surface, precipitating onto the substrate's surface (fig 4.4). The released material has a high energy and undergoes collision before settling, forming coatings with high coverage (the sputter tool used in this thesis, while not providing conformal coating provides very good coverage of surfaces; readily coating tall sidewalls and creeping under overhangs).

#### 4.4.3 Evaporation

This technique utilises the local heating of a focused electron beam to vaporise the surface of a target material. Under vacuum the vapour is transported to an overhead substrate's surface, where it precipitates (fig 4.4). Evaporation uses high vacuum which paired with the relatively low energy vapour results in few collisions of the released material; creating films with a slow deposition rate and low step coverage.



Figure 4.4: **Metallisation techniques** Sputtering of metal is achieved through the collision of Argon ions (black) onto a metal target, ejecting material onto the overhead sample. Ejected media has good step coverage. Evaporation relies on heating a target till the metal vapourises, precipitating onto the overhead sample with limited step coverage.

#### 4.4.4 Parylene C coating

Parylene coating is a common technique for the creation of conformal films used to prevent water ingress and ion diffusion. The technique is applied under vacuum beginning by heating a solid Parylene dimer till sublimation. In its gaseous form, the Parylene dimer is introduced to a furnace which cracks the dimer into its monomer constituents. The monomer is passed through to the deposition chamber, where it polymerises to a conformal solid.



Figure 4.5: **Parylene coating process.** The solid dimer sublimes in the vapouriser, where it is drawn into the furnace. High temperatures crack the parylene dimer into its monomer constituents. The parylene polymerises upon the sample on the deposition chamber. A cold trap is used to condense any remaining parylene, preventing its transport to the vacuum pump. Image derived from (6).

Since Parylene-C coating is initiated as a gaseous form, care must be made to prevent unwanted coating, as was the case regarding the circuit board connectors mentioned later. To prevent Parylene-C inflow, these connectors were tightly covered in Kapton tape and then painted over with multiple layers of aqueous latex (for the devices manufactured in this thesis, costume makeup aqueous latex was used). After Parylene coating these sacrificial layers can be carefully removed using scalpel and tweezers.

## 4.5 Additional fabrication methods

#### 4.5.1 Photoresist removal

Removal of un-damaged photoresist is trivial and can be completely removed using solvent baths. However, after treatment with plasma during etching, removal of these damaged layers can be more difficult. Two resist removal techniques were utilised during the following manufacturing processes:

- Oxygen plasma ashing: This method uses a heated platen in the presence of an oxygen plasma to strip resists. Various parameters (temperature, platen power, and time) can be controlled to control the aggressiveness of this removal. This is well paired with a subsequent soak in heated 1165 remover, the asher rapidly stripping the outer layer of photoresist allowing ingress of the 1165 photoresist remover.
- RCA 1 Clean: This chemical mixture aggressively removes organic materials and can etch some metals. It is created by the addition of hydrogen peroxide to a heated aqueous ammonia solution and soaking, into which the sample to be cleaned is soaked (≈5-30 mins depending on sample). It was shown to be very successful at removing stubborn photoresists layers (e.g. photoresist post Argon +

ICP etching). However due care should be taken given that this reaction produces oxygen (i.e. flammability), during which the solution will violently bubble which can be mechanically damaging to thin films.

#### 4.5.2 Thermal Annealing

Rapid thermal annealing (RTA) is used to anneal semiconductor contacts (e.g. the Ni/Au/pGaN contact). This relies on rapidly cycling the substrate temperature from room temperature to 1300°C and back, in a gaseous atmosphere (N2 and air atmospheres are common). The Jipelec RTA used provides heating with high intensity near-Infrared lamp sources, and allows user configuration of temperature ramping and hold steps and gas flows.

## 4.6 Measurement and analysis methods

Visual inspection using high magnification microscopes provide valuable insight into the success of various process steps, allowing examination of photoresist pattern transfer, defects, etc. However, the majority of process rely on the creation of nanometremicron scale features and validation of process operations is only achievable through measurement. Various tools are used throughout the fabrication process which permit deeper understanding into the mechanical or electrical properties of the sample under test.

#### 4.6.1 Profilometry

Profilometers are valuable tools for microfabrication; providing important information on the stack heights of various layers, key in determining deposition and etching rates during tool calibration and processing. These tools rely on a cantilever probe which is passed over the substrate; peaks/valleys in the topology produce deviations in the probe height which can be measured and communicated to the user. Two profilometers were utilised; a Veeco Dektak 3 profilometer suitable for line-scan measurement of profiles with a vertical range of  $65\mu$ m. Higher resolution measurements were available using an atomic force microscope (Park systems) suitable for 2D measurements with nanometre resolution.

#### 4.6.2 Optical thin film measurement

Light passing through two materials of different refractive index is partially reflected, the amount of reflected light is dependent a number of factors including the light's wavelength, the various layer thicknesses and the refractive indices of the layers. This property can be used to measure thin film thicknesses, as is provide with the Filmetrics F20; this apparatus shines white light onto the test sample and measures the reflectance spectrum, from which software determine the comprising layer thicknesses.

#### 4.6.3 Electric probe station

The electrical properties of a probed circuit can provide important information during fabrication and characterisation of semiconductor devices. The probe station allows the user to measure the current-potential (IV) characteristics between two probed points.

Nonlinear IVs are indicative of semiconductor circuits, linear IVs denote metallic circuits and noisy can denote open circuits or insulating materials. The ability to differentiate these differing states offers great benefit to the manufacturer as thin conducting layers may be optically indistinguishable but are easily discernable under electrical testing.

#### 4.6.4 Witness samples

Often it is not straighforward to measure directly the microfabricated structures, so witness samples can be included during the deposition/etch stage as a measurement proxy. An example of this would be the Au deposition/etch stage, during which a glass slide would be included in the same deposition and etch stages as the actual wafer. The glass slide would be tested for conductivity during etching to ensure that the Au was fully etched (any Au remaining on the glass would produce a linear IV instead of the glass' naturally insulating response).

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## Chapter 5

# **Optrode** Probes

## 5.1 Introduction

As previously mentioned, neural probes with integrated  $\mu$ LEDs have demonstrated their ability to provide optical stimulation. When paired with electrodes, these neural probes can become a powerful tool for examining neural circuits facilitating both optical stimulation and electrical stimulation/recording (multimodal stimulation provides a direct comparison between electrical/optical stimulation) This chapter describes the fabrication and characterisation of one such optrode. Modelling is performed to predict its ability to record and stimulate volumes of neural tissue.

## 5.2 Design Rationale

The design of a penetrating neural probe necessitates careful balancing of the requirements of the neuroscience experimentation and the restrictions of micro-fabricating such devices.

#### 5.2.1 Neurological Considerations

The main geometric concerns for the recording of neural activity via such probes are namely electrode spatial resolution, coverage and volume displacement.

- Electrophysiological constraints: The electrodes must be arranged to ensure the recording sites cover the vicinity of the desired neural populations; which in the case outlined here is recording from layers of the mouse cortex (approximately 1mm thick comprising of 6 layers between  $\approx 100-300 \mu m$  thick(1)).
- Volume displacement: The damage produced during insertion of the probe is linked with the total volume displaced by the neural probe, with larger volumes causing greater damage. Since these probes are penetrating, the most crucial factor is the cross sectional area of the probe, which should be minimised where possible.
- Surgery considerations: The mouse brain can be approximated as a cuboid with dimensions 15mm x 11mm x 7.5mm (l × w × h), with the neocortex covering the outer ≈1mm. Shank lengths of approximately 6-10mm allow for the majority of the mouse brain to be surgically accessible. The brain is accessed by removing a ≈5mm square portion of the skull over the region of interest, through which

multiple probes may need to be inserted. To tolerate this, the width of the probe and its associated PCB should be minimised.



Figure 5.1: **Surgical considerations** Left) schematic of surgery, showing surgical layout and size restrictions. Right) Key probe dimensions and aspect ratios.

#### 5.2.2 Microfabrication Considerations

Previous work by R.Scharf provided designs and a suggested fabrication process for high-density optrodes using a multi-layer design for LED and electrode tracks(2). Significant headway was made into the fabrication of these devices, however the geometries found in this design (stacked thin features extending multiple mm lengths) presented some difficulties in manufacture namely:

- Complete etching of the Ti/Au LED interconnects could not be fully achieved due to poor selectivity of the metal etch, leaving excess Ti/Au surrounding vertical features (e.g LEDs) (Fig 5.2 top). This paired with close proximity of features resulted in frequent shorting of LED wires.
- The etching of these LED wires created a highly textured substrate, over which it was difficult to pattern electrode wires (Fig 5.2, bottom).

Fabrication of these designs were brought to late stage; however, to ensure succesful manufacturability and maximise yied, a single layer (i.e. LED interconnects coplanar with electrode interconnects) design was adopted.



Figure 5.2: Bilayer design failure modes a) incomplete etching of LED interconnect material (yellow) leaves thin metal traces (red) on vertical features, b)which in turn caused shorting of LEDs through the proposed pathway (highlighted in orange) (Scale bar -  $25\mu$ m). c) Multilayer track configuration, d) created a rough substrate which was detrimental to patterning of fine  $2\mu$ m features (Scale bar -  $25\mu$ m).

The width of the probe shank is based on the number of traces and the width of the trace/inter-trace spacing, minimising these features ensures a thin probe width. With our current photolithography capabilities, the minimum feature size is  $\approx 2\mu$ m (limited by a variety of factors including wavelength of light used, photoresist feature aspect ratio and even user skill to name a few), however, to ensure robustness in design and reduce shorts, the minimum feature size and spacing was chosen as  $\approx 3\mu$ m.

## 5.3 Probe designs

Under these guidelines and with direct neuroscience input from Dr. Sakata (our close collaborator), optrode designs were created (Fig 5.3). The optrode is fabricated monolithically on a GaN on Si substrate featuring individually addressable  $\mu$ LEDs, with a common n-contact, paired with microelectrodes. With photolithography, numerous probe designs can be implemented on the same mask, allowing multiple probe styles to be fabricated simultaneously. Two styles of optrode probe shank designs were created: a linear array (collinear electrodes and  $\mu$ LEDs) and a tetrode design (incorporating three tetrodes (4 electrodes organised in a square geometry) surrounding a  $\mu$ LED). Double shank versions of these designs were developed, allowing coverage of a larger neural volume while demonstrating scalability of the design. Finally, a LED only probe based off previous designs was included.



Figure 5.3: **Optrode designs** Top) Schematic of single shank. Middle) Tetrode design. Bottom) Linear array. (Scale bars: Blue –  $100\mu$ m, black - $50\mu$ m). Green circles represent the  $25\mu$ m diameter LED pixel, black circles represent the  $5\mu$ m diameter electrodes openings.

The optrode shank designs had the following features

- Linear array optrode: this shank format featured 16 electrodes (5 $\mu$ m diameter) equally spaced 50 $\mu$ m along a range of 800 $\mu$ m, thereby allowing recording of most layers across a mouse cortex. This shank incorporated four 25 $\mu$ m diameter circular  $\mu$ LEDs in 200 $\mu$ m intervals.
- Tetrode array optrode: this design included three tetrodes (each electrode is  $5\mu$ m diameter) arranged at distances of  $300\mu$ m (centre to centre) and a single distant electrode. Each tetrode surrounded a  $25\mu$ m diameter circular ED with an inter-electrode spacing of  $50\mu$ m. This configuration provides recording capabilities for multiple layers and a distant electrode which could be used for either local field potential (LFP) recording or as a reference site for recording.

The salient points of each shank design are displayed in table 5.1. Mask designs were designed using Tanner L-EDIT CAD software and produced by Compugraphics.

	Tetrode Array	Linear Array	LED only
	shank	Shank	
Number of	3	4	16
LEDs/shank			
Number of	13	16	0
Electrodes/shank			
Shank Width	137	160	140
(measured at final taper width) ( $\mu$ m)			

Table 5.1: Optrode designs key features.

These probe designs facilitate recording and stimulating across most layers of the cortical column; other optrode designs following the Michigan probe style have lim-
ited spread of recording sites (3; 4), or are restricted in their ability to independently stimulate the comprising layers (5; 6; 7; 8; 9).

### 5.4 Probe Microfabrication

The following details the microfabrication stages used to develop the optrodes, which were developed using the techniques explained in the previous chapter. The recipes used for the deposition/etching processes can be found in Appendix A.

### **Probe Fabrication**









(10mins 150°C) followed by soaking in heated 1165. The wafer sample is then rinsed in water and dried using $N_2$ and hotplate.	
Step 11: Trench Etching –Pt2Patterning: A thick photoresist coating (~8um) was used to etch the trenches. Two step spinning was used to coat the wafer sample: First)300rpm for 15s, 200 ramp, Second) 2000rpm 120s, 200 ramp. Softbaked for 120s at 105°C. The wafer sample was exposed for 20s. Developed in a 1:1 solution of AZ developer/DI water for 120s. The wafer sample was rinsed in DI water and hardbaked.DRIE Etch: the wafer sample was etched to ~60um through the silicon.	



Figure 5.4: False colour SEM images demonstrating differing probe designs during fabrication (after step 9). Left) linear array design. Centre) Linear array design (Higher magnification). Right) Tetrode design.

Certain difficulties were experienced during probe fabrication, which could be improved with the following implementations:

- **n-Contact Patterning:** Lift-off removal sometimes proved challenging, (specifically of small features such as around  $\mu$ LEDs mesas); requiring ultrasonic agitation to clear samples. Increasing the area of these features may improve lift-off, and given the n-GaN's relatively high conductance this may have not have any significant detrimental effects on LED performance.
- Interconnect creation: The  $\mu$ LED/electrode wires were created using a SiO<sub>2</sub> hard mask; while this provided the high-resolution required it also involved multiple high-temperature cycles which may unnecessarily strain the devices. Secondly during creation of the hard-mask, a thin layer of unknown composition was occasionally created. This layer would peel from the hardmask, and was exceptionally resilient: surviving RCA 1 cleaning solution, Resist Stripper 1165 soaking, BOE etching and matrix ashing (see Fig 5.5, top).

To better this, it is proposed that wires are created through a 2 step lift-off process (see Fig 5.5, bottom). Firstly, high resolution features (wires) are created using lift off with a thin-resist, this step could be done using an evaporated metal layer to improve deposition directionality facilitating easier lift-off. A second metalisation layer is then used to bridge the mesa and wire layers (as lower resolution/high step coverage is required a sputter deposition would be suitable for this step). By removing the need for metal etching (and the necessary SiO<sub>2</sub> hard mask deposition/etching stages), it is hoped that this 2 step process would facilitate reliable creation of traces, by eliminating the risk created by the mask layer delamination above. Furthermore, the 2 step lift-off process would be performed without exposure to plasma environments, and under lower temperature thermal cycles which may also prevent damage to the device.



Figure 5.5: Fabrication difficulties a) Masking layer delamination during wire patterning. Scale bar = 100  $\mu$ m. b)Proposed 2-step lift off process. c) Example of lift off patterning of fine features.

### 5.5 Characterisation

Electrical and optical characterisation of the optrode was performed before singulation. Electrical characteristics were measured using semiconductor parameter analysers (Either HP4155A/Yokogawa), a voltage sweep of -1V to 6V was applied (0.1V steps), and the current draw was recorded. The  $\mu$ LED output optical power during a current sweep was measured with a Thorlab PM100A power meter. The LED's Lambertian emission profile prevents the power meter from capturing the total emitted power; to counter this a correction factor was first applied to the power measurements (See Appendix D).The  $\mu$ LED surface irradiance was then determined by dividing the corrected power by the LED active area (taken as the area of the LED mesa).



Figure 5.6: **Probe characterisation.** Top) Optical micrographs of illuminated LEDs under increasing load. Bottom left) IV characteristics of LEDs; dotted line- mean, shaded area mean $\pm$  standard deviation (Standard deviation is calculated with a normalisation factor of N-1). Right) Optical characteristics of an exemplar LED.

The  $\mu$ LEDs showed low turn-on voltages of 3.3V, which is approximately 0.6V higher than expected for the material (one would expect a turn-on voltage of  $\approx 2.7$ V considering the GaN/InN alloy's bandgap). The LEDs draw a current of  $0.54\pm 0.23$ mA (mean±std, n = 16) at 5V; exhibiting a leakage current of -0.15nA± 0.21nA (mean±std, n = 16) at -1V. The series resistance for these LEDs at 2.6kOhm ( $\approx 1.1$ kOhm of which is due to the interconnect) (Area =490  $\mu$ m<sup>2</sup>) is higher than reported values of similar LEDs ((10) R = 769  $\Omega$ , Area = 2500 $\mu$ m<sup>2</sup>; (11) R = 151 $\Omega$ , Area = 490  $\mu$ m<sup>2</sup>; (12) R=558  $\Omega$ , area = 400  $\mu$ m<sup>2</sup>). The low-leakage current indicates that discrepancies between measured properties and theoretical values/comparable devices are due to series parasitics (any parallel parasitics would expect to cause higher leakage current). This series parasitic is expected to be caused by the creation of a poor contact with the p-contact. The creation of the ohmic contact is dependent on the formation of a NiAu/p-GaN/O<sub>2</sub> compound created during annealing in air (13); the quality of this layer may have been disrupted by non-optimised process parameters (e.g. excess/insufficient deposition of metals, inclusion of contaminants such as residual hardmask, etc.).

Despite these series parasitics, irradiances of  $\approx 100 \text{mW/mm}^2$  were attained at 1mA drive currents. This equates to an external quantum efficiency (EQE) of 1.8%; (EQE is the ratio of photons which escape the LED per second to the number of electrons injected into the LED per second; an EQE of 2% means approximately 2 out of every 100 electrons which pass through the LED are converted to photons which escapes the LED). Due to the orientation of the unreleased neural probes on the wafer, attempts to align the optical power meter over the LEDs were hampered by the position of the current probes, and therefore the total number of optical measurements is small (n=4). The  $\mu$ LED fabrication attained a yield of 80% (n = 20) (i.e. LEDs which were not shorted, could be illuminated and achieved a current flow of 50 $\mu$ A by 4V). The neural

probes shown here demonstrate a proof of concept, further fabrication steps (backside thinning and passivation of devices) are required before in-vivo validation. As such no electrical characterisation of electrodes was completed.

### 5.6 Electrical/Optical simulation

The optrode allows close proximity of electrodes and an optical source, allowing simultaneous stimulation and recording from the same population of neurons. As the LED's irradiance increases, greater volumes of tissue can be stimulated, however, this introduced energy can cause local tissue heating. To prevent unnecessary tissue heating and reduce stimulation of neurons outside the recording region, it is appropriate to use the minimal irradiance required to excite a given volume.

To assess this, the overlap between the optical stimulation volume and the electric recording volume was modelled. A section of the neural probe was modelled at the base of a tissue cube (length: 400um, voxels 1um x 1um x 1um). The  $\mu$ LED emission profile is derived from prior work by the University of Strathclyde, which modelled an emission profile using a Monte-Carlo simulation, which considered the attenuation and scattering of light in tissue(2)(11), (the LEDs described here are of similar dimensions, allowing a direct comparison with this work). This model launches a fixed number of photons into a volume of neural tissue<sup>1</sup> (sub divided into voxels) with a Lambertian emission, each photon takes a random walk (where the distance and direction of each step is determined by the scattering co-efficient ( $\mu_{\rm s} = 117 \text{ cm}^{-1}$ ) and anisotropy factor (Henvey-Greenstein model, g = 0.88 which represents a higher likelihood for forward scattering) respectively). During this walk, the photon deposits a given amount of energy into the voxel (according to the Beers law,  $\mu_{\rm a} = 0.7 \text{ cm}^{-1}$ ) until the photon has depleted its initial energy or it has exited the volume. Similar models featuring a strong scattering coefficient, weak aborption coefficient (where  $\mu_a \leq \mu_s$ ) and a high anisotropy factor have shown to agree with measured light propogation through tissue(15). Two-dimensional isocurves of emission profiles were generated from given LED powers (see Fig1. panel f(11)), it is from these that the following simulations are derived. The optically stimulated volume based on a  $1 \,\mathrm{mW/mm^2}$  (threshold for ChR2(16)) for a given LED irradiance was derived by fitting an 8-point polynomial curve to the aforementioned 2D emission profile, which was revolved around the z-axis creating a 3D volume.

As mentioned prior (Chapter: Background, Section 2.1), the neural electric potential scales by an exponential decay with a decay constant of  $\approx 28 \mu m(17)$  and therefore the electrode's signal amplitude(V<sub>elec</sub>) in response to a distant neural signal (V<sub>neuron</sub>) can be modelled as a function of distance from the electrode (r).

$$V_{elec} = V_{neuron} * e^{(-r/r_0)}$$

$$(5.1)$$

In this simulation,  $V_{neuron}$  was set to 1mV representing the upper magnitude of an extracellularly recorded neuronal spike(18).

The electrode is not a perfect detector; noise sources limit the distinguishing of neural signals. The thermal noise of the electrode provides a measure of the electrode's limit

<sup>&</sup>lt;sup>1</sup>The scattering parameters used were those of human grey matter(14).

of detection (18), which is defined by

$$V_{noise} = \sqrt{(4 * R * k_B * T * BW)} \tag{5.2}$$

Where R is the resistance of the electrode,  $k_B$  is the Boltzmann constant, T is the temperature, and BW is the bandwidth of the signal. Given a bandwidth of 10kHz and electrode resistance of 500k $\Omega$ , the thermal noise at 37°C is approximately  $9\mu V(18)$ .



Figure 5.7: Simulation of emission coverage. a) The simulations examined a volume of  $200\mu \text{m} * 200\mu \text{m} * 250\mu \text{m}$  cuboid above the optrode surface, centred on the LED. b) Electrode coverage and stimulation volume as a function of irradiance. c) 2d comparison of optical stimulation volumes and recording limits at cut line a-a'. Recording limit of electrode given a  $9\mu \text{V}$  noise floor. Optically stimulated volumes of neurons under increasing power densities at the  $\mu \text{LED}$  surface are included (assuming a  $1\text{mW/mm}^2$  stimulation threshold).

The total number of voxels, which was both electrode detectable and stimulated was calculated for a range of irradiances between 10 and  $200 \text{mW}/\text{mm}^2$  (Fig 5.7). Irradiances up to  $80 \text{mW}/\text{mm}^2$  are sufficient to stimulate volumes up to  $\approx 2 \times 10-3 \text{mm}^2$ ,

while being completely covered by at least one electrode's region of detection. As the  $\mu$ LED's irradiance increases, the stimulation volume exceeds the bounds of the electrode's detectable volume. If stimulation and recording from a local neuron is the desired neuroscience protocol, it suggests that irradiances of  $\leq 80 \text{mW/mm}^2$  are sufficient for examining close neural circuits; irradiances higher than this activate neurons outside the detection limit and may cause unnecessary heating of tissue.

This irradiance bound suggested here provides guidance for designing neuroscience protocols, however, the realities of biological and hardware capabilities may alter this in practice. Opsin variability such as stimulation threshold or expression density will alter the optrodes coverage (e.g. low-threshold opsins, such as the step function family of opsins (19; 20), will require less stimulation intensity to fully stimulate the electrodes recording volume).

### 5.7 Electrical crosstalk

Crosstalk is the undesirable artefact imposed on a victim circuit due to electromagnetic interference from another aggressor circuit and can arise from inductive or capacitive means(21). Due to the close proximity of the LED and electrode interconnects, paired with the low magnitude of the signal of interest; the implications of crosstalk can be significant and should be considered.

Finite element analysis software (Comsol/Quickfield) was used to simulate the probe's electrostatic fields, to determine the mutual capacitance between the aggressor (LED) and victim (electrode) interconnects. Differing architectures were modelled to understand the implications of changing from a bilayer to monolayer probe architecture.

Capacitance (C) is the degree at which a system can store charge (Q) in response to an applied potential difference (V), and is defined by Eq 5.3.

$$Q = CV \tag{5.3}$$

For a system comprising of multiple conducting components, charge can build up between these components; the total charge on a conductor is the sum total of its capacitive interactions with other conductors (Eq 5.4).

$$Q_1 = C_{11}V_1 + C_{12}V_2 + \dots + C_{1n}V_n \tag{5.4}$$

Where  $C_{1n}$  is the mutual capacitance between the conductor<sub>1</sub> and conductor<sub>n</sub>. In a multi-conductor system of N conductors, the charge on each conductor is dependent on the mutual capacitances and the component's potential according to the capacitance matrix equation Eq 5.5(22):

$$\begin{bmatrix} Q_1 \\ Q_2 \\ \cdots \\ Q_n \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1n} \\ C_{21} & C_{22} & \cdots & C_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ C_{n1} & C_{n2} & \cdots & C_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \cdots \\ V_n \end{bmatrix}$$
(5.5)

It is this matrix that the finite element solver derives; initially by solving Poisson's equation for the electric field with electric potential as the dependent variable (Eqs 5.6,5.7) for electrostatics to determine the charge in the system under applied potentials.

$$\nabla(E) = \rho/\epsilon \tag{5.6}$$

$$E = -\nabla V \tag{5.7}$$

Where E is the electric field, V is the potential,  $\rho$  is the charge density, and  $\epsilon$  is the dielectric constant of the material.

Using this method, the energy within the system is calculated (integration of the energy density ( $W_e$ ) within a volume  $\Omega$ ) (Eqs 5.8,5.9) under differing load conditions, allowing the derivation of capacitance matrix components accordingly(23):

$$C_{ii} = \frac{2}{V_i^2} \int_{\Omega} W_e d\Omega \qquad V = \begin{cases} 0 & i \neq j \\ V_i & i = j \end{cases}$$
(5.8)

$$C_{ij} = \frac{1}{V_i V_j} \int_{\Omega} W_e d\Omega - \frac{1}{2} \left( \frac{V_i}{V_j} C_{ii} - \frac{V_j}{V_i} C_{jj} \right) \qquad V_k = \begin{cases} 0 & k \neq i, j \\ V_i & k = i \\ V_j & k = j \end{cases}$$
(5.9)

Simply put: a parameter sweep is applied to all conductors (applying a known load potential or grounding), the simulation is run, the total energy of the system is derived for each case, from these the capacitance matrix is calculated.

The neural probe was modelled as a 2D cross section, with a simplified geometry of a 7mm long shank portion embedded in a square faced cuboid of tissue (A=500 $\mu$ m x 500 $\mu$ m). Due to the close proximity of the driving and recording interconnects, the shank is expected to have the most dominant influence on capacitive coupling. Boundary conditions are applied to the model (external surroundings and n-contact (and connected Si/N-Gan) is grounded; conductive materials (interconnects/electrodes) are defined as terminals (i.e floating potential)) (Table 5.3). Relative permittivies are applied to the various dielectric materials (SiO<sub>2</sub> – 3.8 (24), tissue (modelled as water) - 80)(Table 5.2). The model is meshed with a density which increased around the interconnects.

Material	Relative Permitivity
SiO(2)	3.8
Tissue (modelled as water)	80

Table 5.2: Simulation material parameters

Boundary	Boundary Condition
External boundary	Grounded $(V = 0V)$
Probe substrate	Grounded $(V = 0V)$
Interconnects	Floating $V = V_0$

Table 5.3: Simulation boundary conditions



Figure 5.8: Mutual capacitance FEA modelling. Left to right) Probe architectures examined (geometries not to scale). Example Comsol 2d simulation geometries demonstrating probe shank embedded in tissue. Close up of probe meshing, demonstrating increased mesh density closer surrounding interconnects.

The capacitance matrix was derived for the probe style demonstrated above. The interconnects had an average capacitance to ground of  $2.3 \pm 0.001$  pF (mean $\pm$ std, n = 16), and a mutual capacitance with the nearest neighbouring interconnect of 0.07pF. As expected, the mutual capacitance decreases with higher order neighbours, a double exponential (Eq 5.10) was used to fit the results of the mono-layer design interconnect capacitances:

$$C_{1n} = 0.11e^{-0.97n} + 0.03e^{-0.18n} \tag{5.10}$$

where  $C_{1n}$  is the mutual capacitance between an interconnect and its n-th neighbour.



Figure 5.9: Mutual capacitance of driven line to nearest neighbour.

This process was repeated, calculating the capacitance matrix for the stacked architecture, which showed increased average capacitance between LED and electrode interconnects of  $1.1\pm 0.003$  pF (mean±std, n = 3); in agreement with previous measurements of this probe architecture's mutual capacitances (1-2pF). The mutual capacitance between a driven LED interconnect and the next electrode interconnect dropped off much faster (an order of magnitude) than in the mono-layer model, further neighbours however do not see improvement from the mono-layer design.

These results suggest that the monolayer design has improved electrical properties compared to the previous design (albeit only when considering only the first neighbouring electrode). To provide perspective to the results of these simulations, driving an LED (0-4V, 80ns rise time) will inject a current of  $3.5\mu$ A through a neighbouring electrode in a monolayer design, which when grounded through an electrode (Z =  $500k\Omega$ ) will briefly raise the amplifier front end potential by 1.75V. Already this may seem exceedingly large, however, it is preferable to a bilayer design which would inject  $55\mu$ A of current; which may raise the amplifier's potential to the saturation voltage.

The true mutual capacitances of these designs are presumably larger than this, as the shank only represents part of the total probe design (not to mention the PCB, connectors, etc.); to accurately describe this a 3D model would need simulated (which is too computationally intensive). However, such deep examination into the origins of interference sources and their mitigation has demonstrated its worth in significantly reducing electrical artefacts(4; 6). Further simulation would allow straightforward investigation into more artefact resistant topologies such as the inclusion of ground planes/guard traces or the substitution of SiO<sub>2</sub> for materials of a higher dielectric constant (e.g. Si<sub>3</sub>N<sub>4</sub>, SiC, Al<sub>2</sub>O<sub>3</sub>).

It should be noted that mutual inductance is also a cause of electrical artefacts; however, this was not examined in great detail as it is not expected to contribute as significantly as capacitive coupling (due to the I-V characteristics of the LED, the dI/dt is approximately three orders of magnitude greater than the dV/dt).

### 5.8 Conclusion

The optrode probes described here (albeit not singulated) demonstrate a process for fabricating neural probes capable of providing light power at ranges required for optogenetic stimulation. Single layer design architecture, while unfortunately reducing the density of the electrodes, significantly reduces capacitive coupling characteristics and ease of fabrication.

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## Chapter 6

# **Dual Colour Optical Stimulation**

### 6.1 Introduction

The following chapter discusses the development of a neural probe for use in multispectral optogenetic studies. This chapter shall briefly examine the need for multispectral opsin control and current efforts to provide such stimulation. An attractive solution for creating such probes based on transfer-printing techniques shall be introduced together with a generalised overview of this (as of yet not discussed) microfabrication technique. Finally the fabrication and characterisation of a dual colour neural probe developed using this technique shall be demonstrated. Following work completed in conjunction with Dr J C Carreira.

### 6.2 Background

The requirement for multi-spectrum stimulation capabilities is becoming more necessary for the optical control of neural circuits. Multispectral control has been used to enable independent inhibition & stimulation of differing neural populations expressing multiple spectrally distinct opsins. Klapoetke et al have demonstrated this capability, pairing the blue-green light activated Chronos (Spectral peak:  $\approx 490$  nm) with the redshifted Chrimson (Spectral peak: 590 nm), and were able to elicit colour dependent activity in differing neurons(1). Multicolour stimulation capabilities are necessary for step-function opsins whose activation is initiated by illumination of light of one wavelength and terminated by another wavelength(2) (e.g. SOUL which can be activated by 473nm light and deactivated with 589nm(3)). Optical stimulators which facilitate multispectral control remain relatively rare in the field and are generally achieved by fibre-optic methods

Miniaturised dual colour optogenetic stimulators have been realised using light-guiding neural probes (4; 5; 6). However, these architectures are dogged by the usual disadvantages facing waveguide optrodes (namely low illumination sites density and high power consumptions requirements). Transfer printed  $\mu$ LED probes provide an appealing alternative, allowing development of low-power, multisite, multi-colour stimulation capabilities (7; 8). Unfortunately, these lack the integration densities capable of monolithic neural probes. Monolithic probes are able to fabricate  $\mu$ LED probes at high densities(9; 10; 11). However the native semiconductor material is intrinsically monochromatic (without the need for more exotic semiconductor materials(12) or driving paradigms (13)). This dual colour optogenetic probe described here uses a hybrid of these fabrication approaches; aiming to pair the high resolution capabilities provided by monolithic integration with the material flexibility of transfer printing.

### 6.3 Transfer Printing

Transfer printing is an emerging microfabrication technique (developed in the mid-2000s (14)) which uses a stamp (typically an elastomer however, other carrier methods have been used (15)) to transfer structures from one substrate (donor substrate) to another (receiver substrate). This technique has permitted compact integration of materials and processes at scales which would previously have been incompatible using conventional microfabrication techniques (e.g. integration of semiconductors onto flexible substrates(16)/inclusion of non-foundry compatible materials onto CMOS ICs(17)/co-integration of different semiconductor materials). The versatility of this technique has led to the varied and widespread application of this technique; including development of flexible displays(18), silicon photonics(19), wireless data transfer(20) and of course neural probes (including transfer printing of  $\mu$ LEDs for optical stimulation but also transfer printing of photodetectors for sensing(21)).

#### Transfer printing process

Transfer printing follows the following (general) process (see also fig 6.1), for ease of description the case of transfer-printing  $\mu$ LEDs with an elastomer stamp shall be adopted:

- 1. Fabrication of the donor substrate: The  $\mu$ LEDs structures to be transferred are made using common microfabrication techniques (e.g. those above) with an additional step to remove the majority of the substrate material holding the structure. This is commonly achieved by under etching the  $\mu$ LED's wafer substrate; leaving  $\mu$ LEDs platelets suspended by small anchors (See Fig 6.1, left panel).
- 2. Release from the donor substrate: A microfabricated, polydimethysiloxane (PDMS) elastomer carrier stamp is brought into contact with the  $\mu$ LEDs and adheres to the top surface. The stamp is quickly retracted, and due to the viscoelastic behavior of the elastomer contact is maintained between the stamp and the  $\mu$ LEDs, releasing the  $\mu$ LEDs from the support structure.
- 3.  $\mu$ LED platelet transferal and alignment: The stamp and  $\mu$ LEDs are transported to above their desired location on the receiver substrate and aligned. High-magnification microscopes paired with high resolution control over stamp movement have enabled transfer printing with micron-scale accuracy and precision (the adapted NanoInk NLP 2000 used in the development of this optrode is capable of alighning to sub-micron accuracy and precision (22), however this is dependent on printing conditions and user capability).
- 4. Printing to receiver substrate: The stamp brings the  $\mu$ LED into contact with the receiver substrate. Slow retraction of the stamp relaxes the elastomer, leaving the  $\mu$ LED in situ. Once transferred the LEDs remain held in place by van der Wall's interactions and are ready for any further processing.

This general approach describes the transfer printing process, however extra steps may be required to maximise yield. For example in the following fabrication process, multiple pick-up/release stages were required to correct the  $\mu$ LED's orientation before final printing. Similarly extra adhesion layers (Parylene-C coatings) were required to overcome the rougness of the optrode tracks and ensure a good bond.



Figure 6.1: **Transfer printing process:** left)  $\mu$ LEDs suspended on donor substrate by anchors. right) Dual colour optrode transfer printing process; AlGaInP  $\mu$ LED platelets are retrieved from a donor substrate using a PDMS stamp, transported, aligned and printed onto the monolithic GaN on Si probe shank.

### 6.4 Transfer Printing Hardware

Transfer printing was achieved using a NanoInk NLP 2000 desktop dip pen nanolithography instrument adapted for use with the transfer printing method explained above. Originally this instrument would dip a tip into a donor ink resevoir, which would then be aligned onto the receiver surface using an X/Y/Z stage. The print head would be brought into contact with the receiver, releasing the ink from the head and facilitating dot/line arrays to be printed. This setup was augmented, with a elastomer stamp holder instead of a tip and donor substrate in place of the resevoirs.



Figure 6.2: **Transfer Printer:** Photograph of the adapted NanoInk NLP 2000 system for microtransfer printing, including key components. Image taken with permission from (20).

Elastomer stamps are created in-house using custom moulds (see Fig 6.3). The mould is microfabricated from Silicon, into which pyramid structures are etched at the location of the stamp corners (using wet-etch techniques to take advantage of the anisotropic etching of Si). The sidewalls of the mould are defined by a patterned thick layer of SU-8 photoresist. PDMS is poured into this mould and removed when set, creating a stamp with pyramidal tips on each corner.



Figure 6.3: Schematic drawing of the elastomer stamp fabrication process flow: (a) SiO2 deposition on a Si(100) wafer and definition of square openings; (b) definition of pyramidal protrusions by anisotropic wet etching; (c) SiO2 deposition; (d) definition of the body of the stamp using thick SU-8; (e) pouring of PDMS; (f) PDMS stamp after being peeled-away from the Si(100) mould. Taken with permission from (20).

For a more in-depth demonstration on the transfer printing process, hardware and stamp creation at Strathclyde University please refer to (20).

### 6.5 AlGaInP Red $\mu$ LEDs

AlGaInP red (630 nm) micro-LED platelets were acquired through a collaboration of Dr. Erdan Gu with a confidential company.  $\mu$ LEDs were microfabricated from AlGaInP on GaAs wafer, following a flip-chip LED approach. Initially the pixel area was defined by dry etching to reveal the n-layer. AuGe/Au and Ti/Al/Ti/Au was deposited to create the n and p contacts respectively. Next, the GaAs wafer was inverted and bonded to a temporary sapphire carrier, before removal of the GaAs substrate by wet etching. Finally the  $\mu$ LEDs were individualised through dry etching (producing the unreleased  $\mu$ LED platelets seen in Fig 6.1). mm<sup>2</sup>

Key AlGaInP red $\mu$ LED geometries		
Active area	$6.96 \mathrm{x} 10^{-4} \mathrm{mm}^2$	
Thickness	$3\mu\mathrm{m}$	

Table 6.1: AlGaInP Red  $\mu$ LEDs key geometries.

### 6.6 Probe design

The dual color probe was based on the linear array optrode from the previous chapter. The electrode sites offered locations for electrical contact for transfer printed AlGaInP  $\mu$ LED structures.



Figure 6.4: **Dual Colour optrode design** a) Top view schematic of neural probe tip, featuring multicolour stimulation sites and recording electrodes. b) Cross sectional schematic of final material layers, highlighting epitaxial structures of active elements. AlGaInP structure derived from (23).

### 6.7 Fabrication

Fabrication of this probe can be considered in two main steps: monolithic creation of the blue LEDs and neural probe shank using a GaN on Si substrate followed by transfer printing of AlGaInP  $\mu$ LEDs, after which the neural probes can be singulated and released from the substrate. The following fabrication description continues on from step 10 (Trench etching - Pt 1) in the preceeding chapter.







Figure 6.5: SEM images of the fabricated probes.

Through this fabrication technique 10  $\mu$ LEDs were transfer printed onto five monolithic probe structures, with a success rate of 50% (success rate was measured by the number of  $\mu$ LEDs which were successfully illuminated following the processing mentioned above. This success rate was spread across the differing probe structures - two probe structures had no functional red LEDs, two probe structures had both red LEDs functioning and one probe structure had both one working and one non-working red LED). The main failure mechanism was the creation of open circuits which is predicted to be due to incompletely cleared vias through the Parylene C layer. Further improvements in design and fabrication process are likely to result in increased yield.

### 6.8 Characterisation

The electrical and optical characterisation of the  $\mu$ LED devices was carried out in a similar manner to previous characterisation. The red LEDs operated at lower potentials to the Blue LEDs, with a turn on voltages of  $\approx 1.7$ V and  $\approx 3.3$ V respectively. At 4V the blue LEDs draw 0.3mA and compared to 0.82mA for the red LEDs. Both  $\mu$ LEDs provide sufficient illumination to excite opsins, capable of delivering  $\approx 100$ mW/mm2 illumination at 1mA. Each  $\mu$ LED is independently controllable, allowing single colour illumination or concurrent dual-colour stimulation. Electroluminescence spectra of the LEDs are displayed in figure 6.6, demonstrating the distinct peaks (blue LED - 452nm, red LED - 630nm) (Note the GaN spectrum is derived from historical measurements from similar LEDs of similar material).



Figure 6.6: **Dual color optrode performance.** Left top) Electrical and optical characterisation of  $\mu$ LEDs. Left bottom) Electroluminescence spectra of optrode  $\mu$ LEDs compared common opsin with absorbance spectra (ChR2 and Chrimson(1)). Right) Independent illumination capabilities (driving current 100 $\mu$ A)

### 6.9 Conclusion

This chapter details the development of a dual colour optrode probe. The fabrication method described offers a method for the integration of non-native materials (not limited to  $\mu$ LEDs) which lays the foundations for high-density dual colour optical stimulation.

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## Chapter 7

# Wireless stimulation

### 7.1 Introduction

 $\mu$ LEDs provide the ability to illuminate regions of neural tissue; such devices require electronic control to ensure accurate stimulation of these regions. Stimulation currents commonly rely on tethered setups to provide power and control, which may restrict experiment procedures and animal behaviour. Wireless stimulators have been developed by many groups (see Table 7.5 & futher comparison in appendices (Appendix E, Comparison of wireless optogenetic stimulation systems) ), however, these devices frequently; exhibit low channel count, lack subtle control over illumination or are made with custom ICs and thus are un-available for most users. The following chapter details the development of a wireless optogenetic stimulator tailored for the control of high channel count  $\mu$ LED devices. The device is coupled to a  $\mu$ LED probe (manufactured as a collaboration between University of Strathclyde and Neuronexus) manufactured similar to those previously detailed in Chapter 7 (i.e. same wafer materials, pixel geometries and pixel definition manufacturing steps), with the optical and electrical properties characterised through a series of benchtop experiments covered in section six of this chapter (see also figs 7.10, and 7.14).

### 7.2 Design Rationale

#### 7.2.1 Experimental procedure limitations

Wireless stimulators are most commonly head-mounted. An adult mouse only weighs  $\approx 30$ g, and any electronics can make up a significant fraction of the bodyweight. Guidelines suggest 10% of bodyweight ( $\approx 3$ g) can be head-mounted without significant adverse effects on the mouse's movements; although understandably this should be minimised where possible.

Neuroscience experiments typically run protocols lasting at least an hour, these are preceded by surgical procedures requiring an additional hour (at minimum) during which the optical stimulation will not be used. For this reason, the power supply should be capable of providing a minimum of 2 hours operating time and ideally up to 3-5 hours (these times should include an hour of stimulation protocol).

#### 7.2.2 Stimulation capabilities

Three main criteria are posed when evaluating a system's stimulation capabilities: update rate, stimulation amplitude control and multisite illumination capabilities.

- **Temporal control:** The ability to provide optical stimulation at neuron relevant time scales is important. The neuron's intrinsic action potential has a duration of approximately 1ms, however the fastest opsins currently available (e.g Chronos and Chrimson) have typical off time constants of approximately 2-4ms and can only follow stimulation pulse trains up to  $\approx 300$ Hz (1; 2). This frequency provides a lower bound for stimulation rate; however, to ensure future proofing for the development of ultra-fast opsins a temporal resolution of  $\approx 1$ kHz is desired.
- Amplitude control: The dynamic range of stimulation is of great importance as ultimately the volume of tissue stimulated is directly linked to the light intensity produced by the  $\mu$ LED. Lower light intensities (and therefore low driving currents) provide spatial confinement to the stimulation, which can be important during neural circuit analysis. Irradiances as low as approximately 0.4mW/mm<sup>2</sup> have been found to elicit robust spiking which can be recorded by nearby electrodes(3). Conversely high intensity stimulation can modulate greater volumes which may be required to elicit more widespread behavioural effects. Simulations detailed earlier suggest that irradiances of up 60mW/mm<sup>2</sup> are completely contained within the recording volume, thus offering a baseline for stimulation amplitude requirements. This corresponds to a driving current of  $\approx 0.5$ -1mA with a voltage compliance of  $\approx 5V$ . Step increments of approximately 8-10 $\mu$ A allow illumination resolution control of  $\approx 1$ mW/mm<sup>2</sup>.

Additionally, components of electrical crosstalk artefacts are proportional to the signal rise time; the ability to shape stimulation pulses to reduce crosstalk may prove useful. Kim et al. showed slower slew rates reduced artefacts(4). Mendrala demonstrated that pulse-shaping can attenuate the stimulation artefact; with Gaussian pulse shapes preferential over ramps and step increases in stimulation amplitude(5).

• Multisite Illumination: Simultaneous multisite electrical stimulation has proved useful in replicating neural function(6), which may extend to optical stimulation methods. High channel electrical recording systems are ubiquitous; this has not yet translated towards optogenetic stimulation, with relatively few wireless stimulators currently featuring greater than four independently controllable channels. To fully utilise the optical probe designs listed prior, the ability of provide independent stimulation of multiple channels (up to 16 channels simultaneously) is desired.

Parameter	Required Value
Weight	$\leq 3$ g
Update rate	$\geq 1 \mathrm{kHz}$
Max current source	$\geq 1 \mathrm{mA}$
Current step size	8-10uA
Voltage compliance	$\approx 5 V$
Waveform generation	Arbitrary, OOK(on off keying)
Battery life	$\geq 2hr$
Other	Independant multisite control

Table 7.1: Summary of the stimulation requirements for driving  $\mu$ LED-based neural probes.

### 7.3 Hardware

### 7.3.1 Stimulation/amplification circuitry

The Intan RHS2116 IC was chosen to drive the  $\mu$ LEDs as it has attractive features, namely simultaneous stimulation and recording capabilities across 16 channels(7). Electrical stimulation can be applied to each channel through a constant current sink/source DAC allowing each of the 16 channels to be used for LED driving (or alternatively electrical stimulation/recording). Stimulation currents can be sourced/sunk to  $\pm 2.55$ mA and the large voltage compliance of up to  $\pm 7$ V should provide sufficient voltage swing to drive the LEDs. The stimulation operates with 8-bit resolution, and a configurable step size (see Fig 7.2) supporting a wide dynamic range. Individual DAC trims allow compensation of stimulator output variance to within  $\pm 28\%$  of the nominal value. Recording of electrode potentials is achievable through low noise amplification and digitisation via analog to digital converters (ADCs). The Intan IC has two amplifiers: a 12bit DC amplifier (gain = 0.125) and a 16-bit AC amplifier (gain = 192), both of which can record from the channel simultaneously.

Stimulator Step Size	Full Scale Range
10nA	$\pm~2.55~\mu\mathrm{A}$
20nA	$\pm$ 5.10 $\mu {\rm A}$
50nA	$\pm$ 12.75 $\mu {\rm A}$
100nA	$\pm$ 25.5 $\mu {\rm A}$
20nA	$\pm$ 51.0 $\mu {\rm A}$
500 nA	$\pm$ 127.5 $\mu {\rm A}$
$1\mu A$	$\pm 255 \mu A$
$2\mu A$	$\pm$ 510 $\mu {\rm A}$
$5\mu A$	$\pm$ 1.275 mA
$10\mu A$	$\pm~2.55~\mathrm{mA}$

Table 7.2: Available stimulation ranges and step sizes



Figure 7.1: Intan IC key aspects. a) Simplified schematic of one channel's operation. b) Intan instructions are completed using the SPI protocol. Each instruction is made up of a command, the desired register and in the case of a write command, the desired values.

Memory registers within the Intan IC are used to configure different aspects of each channels stimulation including: stimulation activity (on/off), stimulation magnitude and stimulation polarity. Communication with the Intan RHS2116 IC is achieved by sending digital instructions using SPI (Serial Peripheral Interface) <sup>1</sup> protocol using a 4-byte instruction package (Fig 7.1). The commands allow for reading/writing of registers plus initiation of ADC aquisitions. Updating a channel's stimulation is achieved by setting the desired current magnitude and switching on the channel's DAC. These registers are latched, only updating once the "Update" bit of the command byte is enabled; this allows for the synchronisation of stimulation pulses across channels. The specifications of this IC meet the required criteria posed above. Furthermore, recording capabilities offer a venue for the creation of a multimodal (electrical/optical stimulation with recording) neural system. The feasibility of this IC to drive  $\mu$ LED systems wirelessly was evaluated under the following criteria:

- Can the RHS2116 provide sufficient power to suitably drive  $\mu$ LEDs?
- Can control be achieved by a microcontroller?

<sup>&</sup>lt;sup>1</sup>For a brief explanation on SPI and I2C (another communication protocol), see appendix F.

• Can the IC be powered by a single power source (i.e. a battery)?

### 7.4 Benchtop system

To assess the viability of this methodology, a benchtop system was developed consisting of an interface board and a headstage (Fig 7.2). Custom PCBs were created for each board, designed using Eagle EDA. The headstage housed the Intan IC whose electrode outputs were distributed to a breakout board for ease of characterisation. The interface board contained the microprocessor and power supply electronics and interfacing with the FT4222H using an off the shelf evaluation board. A breakout board was developed to provide access to the Intan IC's channels, allowing stimulation of external components.



Figure 7.2: **Wired system.** a) Representational block diagram of the benchtop system's communication chain. b) Image of benchtop system. c) Schematic of power delivery architecture.

### 7.4.1 Control logic and data transmission hardware

Control of the Intan IC was achieved using two ICs: an STM32 microcontroller, which directly interfaced with the Intan IC and an FT4222h USB to SPI interface which provided the communication between the microcontroller and the host computer (Fig 3.2a).

#### STM32L432KC Microcontroller

A microcontroller handles the timing and delivery of the Intan's instructions. Intan Technologies utilise FPGA controllers for hardware control, however a microcontroller was chosen to implement this due to their high versatility and shallower learning curve. The STM32L432KC microcontroller was adopted for this purpose due to its low power consumption and small form factor (5x5mm footprint) which will allow further translation to wireless use. These attributes are paired with the STM32L432KC built-in functionality which particularly lend themselves to the control of the Intan IC, namely:

- Serial Peripheral Interface (SPI) Communication: SPI communication allows for high rate data transmission between two devices. There are two SPI ports on the STM32L432KC which can be configured to clock speeds up to 25MHz in master mode.
- General Purpose Input/Output pins (GPIOs): GPIO pins provide the link between the microcontroller and the outer world. These pins offer the ability to set a pin to a digital output, digital input or alternate function. As digital outputs the pin voltage reflects the bit state of the GPIO registers; a binary 1 "pushes" the pin voltage to VDD and a binary 0 "pulls" the pin voltage to GND. The converse is correct with digital input pins (when the voltage on pin is approximately VDD, the register content is a binary 1, conversely a pin voltage at or near ground is represented as a binary 0). The alternate function configures GPIOs with special functions, (e.g providing the capability to communicate using interface standards (e.g SPI/I2C) or analog functionality).
- Timers: Build in timer functions allow the synchronisation of stimulation pulses.

### FT4222H USB 2.0 to Quad SPI / I2C Bridge IC

The FT4222H IC provides a USB to SPI bridge which was used to provide communication between the computer and the microcontroller. FTDI middleware libraries allow FT4222h to be controlled using LabVIEW; allowing the development of custom GUIs for stimulation control and recording of received data to hard disk. Further information on this IC's capabilities is presented in later chapters.

#### Power Supply

The STM32L4 microprocessor requires a 3.3V power supply (VDD\_STM) and the Intan IC requires three power supplies; a 3.3V source (VDD\_Intan) and two stimulation power supplies (V\_Stim\_-ve & V\_Stim\_+ve) which require ±3.3-9V. The FTDI chip's power requirements are provided by the evaluation board.

The USB supply provides a 5V DC power supply to the system with a maximum allowable current draw of 500mA, it was from this source that other supplies are derived (Fig 7.2). The VDD power supplies (VDD\_STM & VDD\_Intan) were created by regulating the 5V USB supply using a 3.3V Low Dropout (LDO) Voltage Regulator. LDO regulators are voltage regulators which produce a low noise output from a higher voltage input supply; dissipating any excess power through an internal resistor. These IC's require a supply overhead (the dropout voltage) to operate, meaning the 150mV dropout LD39015M33R requires at least 3.45V to produce a stable 3.3V output.

Stimulation supplies were created using an LTC3265 Low Noise Dual Supply IC. The

LTC3265's charge pumps convert the 5V USB supply into two bipolar supplies (+9V). To reduce power supply noise, these supplies were then regulated using high power supply rejection ratio (PSRR) Low Drop-out voltage regulators (LT3045, LT3094) to +5.5/-4.4V.

#### Software & Firmware

The STM32L4 microprocessor was programmed to receive protocol variables from a Labview user interface via the FT4222h USB-SPI bridge. These variables determined the stimulation current, pulse width, period of the stimulation pulse and number of pulses (if a pulse train is desired). A 20kHz timer was implemented on the microprocessor, allowing updating of the Intan IC's registers with a time resolution of  $50\mu$ s.

#### 7.4.2 Benchtop System Characterisation

The benchtop system was characterised for both amplitude and temporal control to determine its ability to provide stimulation protocols. Characterisation was performed electrically, using a  $1.96k\Omega$  resistor load in place of a LED, with the voltage drop across this resistor measured by a Saleae Signal analyser (sampling rate: 50MHz). To facilitate the measurement of this, a breakout board was developed using standard 2.54mm PCB sockets which allowed easy access to the Intan chips outputs (see Fig 7.3).



Figure 7.3: Benchtop system breakout board: Detail of the benchtop system breakout board (highlighted red box), the Omnetics connector (white connector) plugs into the Intan headstage thereby connecting the Intan's outputs to the 2.54mm PCB sockets (green connector). Please note this headstage is for an updated version of that seen in 7.2

#### Amplitude control

To assess linearity, the Intan IC's outputs was swept from 0-250 DAC Value (corresponding to a nominal current of 0 to 2.55mA) (Fig 7.4). The maximum current sourced was  $2.17\text{mA}\pm0.01\text{mA}$  of current (mean $\pm$ std for 7 channels), which corresponded with a voltage compliance of 4.25V. Linearity was achieved up to  $\approx 2\text{mA}$ , with the majority of channels outputs lying within 15% of the nominal current across this range (within the trim capabilities of the Intan sytem).


Figure 7.4: Characterisation: left) Linearity of system, right) Linearity error (Percentage difference between measured and nominal current). Each trace represents the output of a different stimulation channel (n=6).

#### **Temporal control**

The ability of the system to provide a temporally appropriate stimulation pulses was determined by a similar measure. A 20kHz update rate was used to update the Intan ICs stimulation registers. Figure 7.5 demonstrates the Intan IC's ability to provide on-off stimulation pulses at 1kHz, meeting the requirements outlined in Table 7.1. This was performed at step increments of 0.5mA nominal current. A 10kHz ripple was observed on the stimulation pulse, the peak-peak (pk-pk) difference of this ripple increased across the linear range (0-2mA), reaching a maximum of 68mV at 2.25mA.



Figure 7.5: Stimulation characterisation a) 1kHz pulse stimulation at increased nominal current, note the overshoot during stimulation onset. b) Stimulation pulse ripple of 0.5mA (blue) and 2.5mA (red) pulses. c) Stimulation ripple as a function of nominal current.

An overshoot was present at the onset of stimulation which would reach compliance before settling; this is believed to be the artefact mentioned in the "Intan Stimulation/Recording Controller User Guide" which is caused by "an imperfection due to the current source circuitry"(8). This overshoot lasts  $\approx 0.25\mu$ s, and is settled by  $\approx 0.5\mu$ s, and is therefore not expected to cause any significant issues during stimulation (fig 7.6) (firstly the turn on kinetics of opsins are orders of magnitude greater than this (generally in the order of 1ms); secondly the recording bandwidth is at maximum only 20kHz and thus any artifact from this overshoot will be heavily filtered). The offset of stimulation, however, sees no under/overshoot, again settling by  $\approx 0.25\mu$ s. This overshoot is likely to be observed with a similar increase in the  $\mu$ LEDs optical power however the optical power was only measured with a long integration time so this cannot be confirmed.



Figure 7.6: Onset (left) and offset (right) of stimulation pulses of differing nominal current.

The firmware allowed for diverse stimulation protocols, (exemplar stimulation waveforms demonstrated in fig 7.7), including: synchronous multi-channel activation, pulse trains (e.g triplets, quintets), and channel-independent stimulation (i.e. each channel can be controlled individually and independently as they are not multiplexed).



Figure 7.7: Exemplar pulses, (top) showing constant frequency pulses, bottom) quintuplet pulses.

# 7.5 Wireless stimulator system

The wired stimulator system outlined above, demonstrated that the component parts have the capability to meet the desired criteria for a wireless system. A wireless system was then developed through an iterative process, which produced 3 versions. Each iteration improved thanks to the involvement and consultation with members of SIBPS Neuroscience group (Dr Aimee Bias, Dr Amisha Patel and Dr Mirna Merkler).

## 7.5.1 Version 1

To develop a wireless design, the system demonstrated above was miniaturised (fig 7.8). However, the buck converter's (LTC3265) foot print was too large, and was replaced with an inverting switching regulator (LT1611) which enabled inversion of the input power supply. The system successfully illuminated a off the shelf SMD LED, demonstrating that the Intan System could be reliably controlled wirelessly, using a 3.7V battery (rather than the 5V USB supply). However, consultation with neuroscientists raised concerns that this design's form factor was too bulky, furthermore the device's weight (3.9g without battery) was prohibitive. The connector used in this design (Omnetics Nano strip connector), was chosen as it is a de-facto industrial standard; however, their excessive lead time (approximately 6-8weeks) and high cost (approximately £100 per connector pair) provided sufficient cause to exchange.



Figure 7.8: Wireless stimulator: Version 1 (Scale = 10mm). left) wireless stimulator. right) PCB designs indicating key circuits.

# 7.5.2 Version 2

With respect to the feedback provided a second design iteration was developed (fig 7.9), with the circuit board layout completed by Svetoslav Stoyanov under my direction. This design incorporated the following changes:

- Reduction of system to a single board: Condensing the design to one board gave significant improvements in weight and size.
- Power supply change: the single board design necessitated a smaller footprint power system; to enable this the Intan's stimulation supplies was changed to a 5V output step-up DC-DC converter (TPS61240) followed by a dual LDO regulator (LM27762) which inverted and regulated the supply to create the positive and negative supply rails(+4.7V/-3.8V).
- Change of connector: A Molex Slimstack board to board connector replaced the Omnetics connector, this replacement was chosen for its reliable sourcing, low cost and high-density connections.

Under these changes a second version of the system was constructed (shown in fig 7.9); reducing the system to a motherboard (containing the Intan IC, control and power circuits) and a daughter board onto which the LED probes are affixed and wirebonded. Wireless communication was achieved utilising an IR wireless protocol (covered later), which allowed the user to select pre-programmed protocols. A red SMD LED was included to indicate optical stimulation and reception of user commands. A 3D printed battery case was designed using Autodesk Inventor based on imported PCB dimensions. The total weight of this system was 2.52g including a 40mAh 3.7V LiPo battery.



Figure 7.9: Wireless stimulator: Version 2 (Scale = 10mm). a) wireless stimulator illuminating neural probe. Blue LED is the neural probe; red LED is the indicator LED. b) PCB designs indicating key circuits. c) Irradiance response of  $\mu$ LED to sweep of the DAC, showing a maximum irradiance of 160mW/mm2. d) architecture of V2 power supply.

The wireless system was able to successfully drive  $\mu$ LEDs to irradiances up to  $160 \text{mW/mm}^2$ , suitable for optogenetic stimulation. Diverse illumination protocols could be created by the system including: sweeps across channels, multiple simultaneous channels and amplitude modulation of channels. The idle current draw (i.e system awake but no stimulation) was 13.7mA (at 3.7V supply), which could be reduced to 11.2mA during sleep mode by setting the microcontroller into a low power mode. This allowed a run time of approximately 3 hours using a 40mAh LiPo battery; sufficient for a one-hour surgery followed by a 1.5-hour protocol. This design was prepared for in-vivo experiments however, due to the probe shanks breaking, did not conclude with any successful experiments.

# 7.5.3 Version 3

The final version of the wireless stimulator is displayed in fig 7.10, showing minimal dimensions and weight (2.8 g).



Figure 7.10: Wireless stimulator: Version 3 a): Render of principle components forming the wireless system. b) Image of wireless device. c) Example of illumination patterns capable. d) Weight breakdown of key system components.

The wireless system's design was further refined from V2 to resolve three key criteria: improved ease of mating connection, reduced power consumption and inclusion of non-volatile memory.

# Improved mating connection

The Molex Slimstack utilised in V2, while suitable in size and weight, was difficult to mate for un-practised users and required extra mechanical support to prevent detachment. Justifiably this component was exchanged for a new connector of similar footprint (Molex floating series connector). The Molex's floating features (the header is slightly moveable) facilitate easy pairing of connectors without requirements for high alignment accuracy.

#### Power supply

Long battery life is important for two reasons: firstly, it enables longer experiment protocols, however secondly it reduces the urgency to complete surgery. Increasing battery performance can be achieved by either:

• Increasing the capacity of the battery.

• Reducing the power drawn by the system.

Given the battery adds significant weight, the former is dependent upon manufacturers, and so efforts must be made to reduce power consumption. In version 3, two techniques were applied to reduce the quiescent power consumption during idleness:

- The microcontroller was set to low power modes.
- The power supply was altered to switch off the Intan chip between the experiment protocols.

The power supply was split between two supplies, one for the microcontroller and the other for the Intan IC. The microcontroller supply was passed directly from the battery source through 3.3V LDO voltage regulator (LD39015M33R) an LDO from the battery source.



Figure 7.11: Block diagram of wireless power supply. Blue lines indicate control lines from microcontroller.

The power supplies were altered from the previous versions (fig 7.11). The Intan VDD supply was achieved using a second LD39015M33R. The Intan Stimulation power supplies were generated similar to the previous version; i.e by firstly converting the 3.7V battery supply to 5V then generating bipolar supply using the LM27762DSSR Dual LDO. The DC/DC 3.7V-5V conversion was replaced with a Boost Converter (MAX17220) which had improved efficiency ( $\approx 95\%$  vs  $\approx 83\%$ ) and a true-shutdown mode which, when enabled, reduces the quiescent current to only 300nA. The Intan IC's power supply "output enable" pins were connected to the STM32 microcontroller; supporting controlled shut down of these supplies when the Intan IC was not used. This power control system allows reduces the quiescent current draw from 10.1mA (at idle) to 0.59mA (at sleep).

Characterisation of the power draw of the system was determined using a Keithley source meter, providing a voltage source (3.7V) and measuring current. An output from the Intan system was delivered through a  $1k\Omega$  resistor. The current draw of the system was measured during 4 points: turn-on and initialisation, idle state, DAC sweep and sleeping (salient points are provided in table 7.3 and fig 7.12).



Figure 7.12: System Power requirements: a) Current draw during various running modes. The plot shows current draw during 1) initialisation, 2) idle, 3) pulsetrain of ramped stimulation intensity and 4) sleep mode. Inset shows the current draw during initialisation: 1a) significant inrush current due to microcontroller/power source switch on, 1b) microcontroller idling, 1c) Intan IC turn-on, 1d) Intan Initialisation. b) Current draw during sweep of stimulation currents. Left axis shows total system consumption during current stimulation. Right axis shows additional current required to provide stimulation current (i.e. system current draw subtracting system idle current). Piecewise breakdown of current draw during idle (c) and sleep modes(d).

	$\fbox{Current draw at 3.7V (mean \pm std) (mA)}$				
Configuration	V2	V3			
Idle	$13.7 \pm 1.35$	$10.1 {\pm} 0.05$			
0.5mA Nominal source	$13.7 {\pm} 0.57$	$11.3 {\pm} 0.05$			
1.0mA Nominal source	$15.5 \pm 1.26$	$12.7 {\pm} 0.02$			
1.5mA Nominal source	$16.3 {\pm} 0.97$	$13.9 {\pm} 0.07$			
2.0 mA Nominal source	$18.4{\pm}1.11$	$14.7 {\pm} 0.07$			
Asleep	$11.2 \pm 1.42$	$0.59 \pm 0.002$			

Table 7.3: Current draw for wireless systems (Version 2 & Version 3) under various load conditions.

During turn-on and initialisation, there is an initial surge of current (max = 35mA), which quickly settles (fig 7.12). During initialisation, the STM32's clock speed is reduced which reduces the current draw. The Intan IC is powered up and initialised according to the manufacturer guidelines. Turn on and initialisation of the Intan IC brings the current draw to its steady state idle current draw of 10.1mA, (not shown is that this can be reduced to  $\approx$ 9mA by turning off the Intan amplifiers). A breakdown of the idle current draw (fig 7.12) was determined based on the system component's data sheets. The "Other" category represents current draw without a known origin; which is expected to comprise of leakage currents, inefficiencies of the power system and unknown current draws within the Intan/microcontroller. Actual current draw of each component can be determined but would require a larger PCB created, adding additional measurement locations in series to each component for current measurement. The "Other" category makes up approximately 30% of the power draw, and therefore significant improvements to battery consumption could be made by the targetted reduction of this category (if indeed any further reductions are possible).

During the DAC sweep, the Intan DAC register was swept from 5-250 in increments of 5. The additional supply current required to source the DAC's outputs was approximately 2x the nominal stimulation current; greater than the Intan data sheet's submitted factor (1.38xnominal current), which may infact be linked to the inefficiencies seen in Fig 7.12.

The sleep function powers down the Intan IC according to the sequence in table 7.4. Disabling the SPI communication before shutting down the Intan power supplies ensures that the microcontroller's pins do not short VDD and ground. Finally, the microcontroller enters the low power "Stop" mode; disabling internal high speed clocks, while retaining register values. The microcontroller is brought out of this Stop mode by an external GPIO interrupt, which in this system's case is the reception of a new IR instruction.

Power Up Sequence	Power Down sequence
Turn on Intan V stim supply	Disable Intan Stimulation pin
Turn on Intan VDD supply	Disable SPI communication
Enable SPI communicatione	Turn off Intan VDD stim supply
Enable Intan Stimulation pin	Turn off Intan V stim supply
Initialise Intan IC	

Table 7.4: Power on and power down sequence

Given this power draw, it is expected that the system fitted with a 40mAh battery could run for approximately 2 hours of total stimulation protocol (one led, 10% duty cycle, 2mA stimulation pulse) with 32hours standby: enabling multi-day experimentation.

#### Non-Volatile Memory

Non-volatile, electrically erasable, programmable read-only memory (EEPROM) was included to the design. Currently the experimental protocols are coded in the devices firmware, which requires re-flashing to enact each update/change in protocol/change in neural probe<sup>2</sup>. However, the ability to permanently store variables could allow the re-

<sup>&</sup>lt;sup>2</sup>This approach requires a user with understanding of the inner workings of the code/firmware upload process and increases the manual handling of these devices which increases the risk of damage (e.g. by incorrect setup).

uploading of the device remotely. The storage capacity is not significant (only 128kbits) and the  $I^2C$  communication interface prevents high speed writing of data, however its inclusion vastly increases the potential functionality of the device by allowing:

- Selective device control: Currently the IR remote will broadcast a command, which will be non-selectively interpreted by any device in the IR remotes range of operation (somewhat akin to electrical stimulation). To allow individual device to respond; identifiers, unique to each device, could be stored on the devices non-volatile memory. The IR remote's command structure could be reconfigured to incorporate a "device select" preamble, multiple devices would recieve the transmitted command however only those with matching identifiers would be programmed to respond. This would enabling multiple wireless devices to be operating simultaneously, each using differing protocols.
- Storage of characterisation values: As mentioned previously the Intan IC's outputs are not exactly the nominal output (Fig 7.4), which can be corrected using the current trim registers (which offer adjustment of the output  $\pm 28\%$ ). The required correction factors could be stored in ROM and loaded when required. Calibration of devices to remove variability would allow interchangeability between devices.
- Storage of stimulation protocols: The microcontroller has limited memory for protocols, and so the device benefits from increasing this storage capacity. Stimulation protocols could also be wirelessly uploaded onto the device, stored on non-volatile memory and retrieved later.

# 7.6 System control

#### **IR** Communication Protocol

Communication with the system is achieved using an IR remote, and transmission is received by a Vishay IR Receiver module. IR communication is an attractive solution for wireless control; mainly due to its simplicity, low pin requirements (only one microcontroller pin is required) and good coverage when using a strong IR source (due to the reflection of transmitted IR on surfaces). The IR remote transmits a NEC protocol encoded command which is modulated at 38kHz. This signal is received by the Vishay receiver, demodulated and then provided to the microcontroller using on-off keying. The NEC protocol begins by transmitting a header which pulls the output pin of the Vishay IR sensor low for 4.5ms. This is followed by the command which is represented by a bitstream of high pulses of  $562.5\mu$ s duration followed by a low period of variable length ( $562.5\mu$ s for binary 0, 1.6875ms for binary 1). This equates to a data transmission rate in the single digit kilobits/second (depending on the bit pattern transmitted), which is relatively slow compared to other wireless methods (Bluetooth - Mbps range, NFC - 500 kbps range). This message can be decoded by measuring the time taken between rising pulses. This is realised in the microcontroller firmware by pairing a 10kHz timer (which provides a counter of  $100\mu$ s resolution) and a GPIO interrupt, which acts to reset the counter upon receiving a rising input. Windowing and timeouts are included in the IR protocol to prevent artefacts creating spurious commands (necessary as given the slow data rate of IR, transmission of long protocols may take seconds - increasing the likelihood of bit error). The reception of a correct command is indicated by the illumination of the red user LED.

#### Finite State Machine

The user's choices are decoded and enact pre-programmed protocols. The microcontroller firmware operates a finite state machine (fig 7.13); a coding architecture performs certain functions depending on the current state variable. Upon power-up the microcontroller initialises variables, peripherals and establishes communication modalities; completion of initialisation is signalled by the turning off of the status LED. The microcontroller remains in an idle state until the user selects by IR remote, whereupon the microcontroller will complete one of 3 options:

- Sleep: This ceases stimulation, and turns off the Intan IC power supplies. The microcontroller resets variables and goes into a low-power mode. These actions reduce the power draw significantly, and is beneficial to perform upon startup once initialisation is complete. During this mode the wireless system is unresponsive (even to re-programming requests from the debugger) and must be woken up before any further actions.
- **Run Protocol:** This selection runs one of the pre-programmed protocols. This turns on the Intan power supplies and initialises the Intan's registers according the user guide. The protocol runs until completion, where the device will return to the idle state, or can be immediately cancelled by sending the device to sleep.
- Current Sweep: This performs a current sweep, which can be used to determine the irradiances range of each  $\mu$ LED.

The finite state machine firmware was further enhanced to incorporate the external non-volatile memory for storage of protocols, (albeit only demonstrated in firmware, results not shown). Extra states where included allowing the transferal of a protocol to the external non-volatile memory, which could then be immediately ran or stored for future experiments. To facilitate the transferal of large data-streams, a custom IR remote was created which interfaced with a Labview program (a Labview program sent a command bitstream to a microcontroller, which then modulated an IR LED using two transistors (one of which controlled toggled the LED according to the carrier frequency and the second provided the amplitude modulated signal)). A cyclic-redundancy check (CRC) was included within the transfer which allowed the identification of incorrect data transfer.



Figure 7.13: Implemented state machine.

#### **Current Sweep**

The irradiance of  $\mu$ LEDs during a current sweep (measured by a Thorlab power meter and corrected for Lambertian emission) is displayed in fig 7.14. Most LEDs can be successfully driven to irradiances of at least 60mW/mm<sup>2</sup>. Most Irradiance-DAC bit curves exhibited a knee point, after which the increase of irradiance plateaued. Each of these knee point was characterised and compared to the LED's IV, corresponding to an average nominal current of 0.93 ±0.13 mA, and voltage of 4.62 ±0.12V. This is proposed to be due to the output's voltage reaching near the compliance level(≈4.7V). Conversely LEDs with less resistive IV characteristics showed the ability to be driven to higher irradiances, with no distinguishable knee points.



Figure 7.14: Irradiance response of  $\mu$ LEDs to sweep of stimulation DAC values. Each trace represents an individual  $\mu$ LED's irradiance.

#### Stimulation protocol control

The microcontroller enables the development of complicated protocols; variance of pulsewidth, amplitude and multichannel stimulation is demonstrated (fig 7.15). Such protocols are created by updating the Intan registers based on a pre-composed array of protocol values.



Figure 7.15: **Examples of stimulation protocols achievable:**(Left) Sweeps across channels with varying direction/pulsewidth with fixed stimulation amplitude (each trace represents a single channel's output). (Middle) Simultaneous fixed amplitude activation of multiple channels (each trace represents a single channel's output). (Right) Amplitude modulation of a single channel.

In a similar manner shaping of the pulse-rise time is achievable; the creation of sine, exponential, and trapezoidal rising/falling pulses are displayed in fig 7.16. This capability is of great interest in future work (incorporation of recording capabilities) as the reduced onset/offset signal differential can reduce crosstalk artefacts in recording channels (see following chapters). Completely arbritary waveforms can also be generated, as demonstrated by signal devised from a random number generator (fig 7.16 lower right panel).



Figure 7.16: Varied pulse-shaping can be created, including: sinusoid, exponential, trapezoidal and random pulses.

The downside of such approaches is the demand this puts on the microcontroller's memory; the STM32L432KC only has 64kB of SRAM, and a 700 pulse on-off keyed protocol can take up 2.7kB (if the protocol values are stored as a 4-byte word). Adding extra complexity (e.g. varying both pulsewidth and channel number), or using pulse-shaping can quickly increase the memory required. Currently this limits the number of protocols which can be stored on the microcontroller.

This can be countered by parameterising the protocols; by storing the parameters which make up the protocol instead of the individual commands. The following algorithm uses nested loops to create a repeating On-Off keyed stimulation protocol from only three key parameters per LED (Pulsewidth, Stimulation period, and Counter).

```
while Protocol Running do

for i=1:Number of \mu LEDs do

if Counter[i]=Pulsewidth[i] then

| Turn off \mu LEDs[i]

end

if Counter[i]=Stimulation Period[i] then

| Turn on \mu LEDs[i]

| Reset Counter[i]

end

Increment Counter[i]

end

end
```

Algorithm 1: Algorithm for parameterised control of LEDs.

The temporal resolution of this loop can be determined using one of the STM32's Timers. Such an algorithm provides control over all LEDs with on-off keying, describing the behaviour of 16 LEDs using only 49 variables. More complex protocol elements such as: pulse shaping, pulse trains and refractory periods could be incorporated into such

algorithms.

# 7.7 System Evaluation

This chapter demonstrated the successful creation of a wireless stimulator with capabilities to drive  $\mu$ LED probes. The system meets the majority of the design criteria, albeit the positive stimulation power supply should be increased to meet these specifications. At the present voltage compliance, the LED is in the steep exponential IV region and even small improvements (0.3V) would allow much higher current flows; facilitating greater coverage of the LED operational ranges.

The main strength of this wireless system is the successful pairing of the versatile and capable Intan stimulator and the flexibility of processing afforded by the microcontroller. The wide-dynamic range of the Intan system provides great control over the stimulation volume and correction of discrepancies between LED uniformity. Electronic control of stimulation amplitude (over external current limiting resistors), allows easy user adjustment without the need for circuit board modification.

The microcontroller enables diverse generation of user protocols (on-off keying/variable waveforms, multisite stimulation), complexity which is generally not afforded by other wireless stimulators [see table 7.5]. Furthermore, the microcontroller's firmware is re-configurable, allowing for the inclusion of new features through software improvements.

	(9)	(10)	(11)		(12)	(13)	(14)	(15)	This work
Wireless (?)	Y	Y	Y		Y	Y	Y	N	Y
Stimulation channels	32	4	1	4	1	4	3	12	16
Weight (g)	2.8 (w/o battery)	3	0.075	0.06	2.8	3.1	2.4	1.9	2.8
Amplitude control	Fixed	Fixed	User definable	Fixed	Fixed	User Definable	Fixed	User Definable	User Definable
Stimulation control	ООК	OOK	OOI	K	OOK	ООК	OOK	OOK, Pulse -shaping	OOK, Pulse -shaping
Power consumption w/o stim (mW)	160	21	?		?	?	?	?	At Idle: 37.4 At Sleep: 2.2
Recording channels	32	10	n/a		n/a	n/a	n/a	32	n/a

Table 7.5: Comparison between relevent stimulator systems

This system fares well in comparison to other wireless stimulators [table 7.5], although it is hard to make direct parallels between these devices as each inhabits its own niche. The most comparable system in terms of versatility is the wired headstage produced by Mendrela and colleagues(15). This headstage has impressive capabilities demonstrating 12 channels of arbitrary waveform stimulation with an 11.72kHz update rate. However, already weighing 1.9g (excluding power supply, battery and control electronics) is likely to be restrictively heavy should it translate into a wireless system. Furthermore, this custom IC is unavailable to most research groups.

The wireless stimulator/recorder developed by Gagnon-Turcotte and colleagues was created using commercial of the shelf components(9). This system features the highest (to my knowledge) stimulation channel count of any wireless system (32 channels of both stimulation and recording). However, the high channel count is reflected in the devices prohibitively high weight (2.9g without battery so will be  $\approx$ 4.1g with 40mAh battery) and high power consumption (estimated less than 45 minutes runtime on a 40mAh battery). Furthermore, this stimulator lacks the ability to alter stimulation

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intensity, relying on PWM (pulse-width modulation).

The system demonstrated in this chapter lies between these two devices; providing fine stimulation control while commercial off the shelf parts, without sacrificing weight or run-time.

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# Chapter 8

# Neural Recording and closed loop

# 8.1 Introduction

In addition to stimulating neurons, it is beneficial to acquire the neuron's biopotentials. The Intan IC offers a strong foundation to achieve both these roles, however, the requirement to store such retrieved neural data requires significant alterations. Over the course of multiple iterations, the stimulation system described earlier was improved to demonstrate combined stimulation and recording capabilities. This chapter describes the key steps established to enable such a system; the functionality of this system is characterised in respect to the noise and data loss. Artefact suppression methods were demonstrated and evaluated. A wireless alternative system is proposed, and preliminary work is demonstrated. Finally closed-loop control modalities are examined.

# 8.2 System Requirements

Two key extracellular biopotentials are action potentials (AP), also referred to as spiking, and local field potentials. These signals inhabit different spectral ranges; LFPs occupy low frequencies (0.05-500Hz) and action potentials incorporate higher frequency components (up to  $\approx 10$ kHz). Nyquist theorem requires an acquisition rate of at least double the highest frequency component necessitating a sample rate of at least 1kHz and 20kHz for LFPs and APs respectively. These bio-potentials have signal amplitudes ranging from  $10\mu$ V-1mV, and so to accurately capture these signals, the noise floor must be below this value.

To guarantee retrieval of these potentials, the electronic hardware should be capable of transferring data to the host computer at a rate equal to or higher than incoming data. Each of the Intan's ADC conversion returns a 32bit response which consists of both the AC and DC amplifiers result. Recording 16 channels at a sampling rate of 20kHz requires a throughput of 10.24Mbps, which rises to 12.8Mbps if the stimulation commands are also to be logged.

# 8.3 Recording system architecture

# 8.3.1 Recording specific challenges

There are specific challenges that occur when recording is introduced which are not an issue in stimulation only systems; external noise can introduce cause artefacts onto the recording channels, high sampling rates/channel counts require a high volume of data to be transferred to the computer, and data communication with the Intan IC is no longer unidirectional. These issues and the hardware/methods used to overcome them are described here. The amplification and acquisition of bio-potentials using the Intan RHS2116 is discussed in further detail and two data communication concepts are introduced: external RAM buffering and bidirectional error-free data communication.

# 8.3.2 Hardware overview

To provide contextualisation for the following discussion, it is beneficial to offer an overview of the developed system. The recording system was based on the previously described benchtop stimulator system (described in Chapter 7, section 4) and features the same general characteristics (i.e. a headstage board which houses the Intan IC and connects to the optrode, and an interface board which houses the components required for data transfer and the power supplies). The main difference between these boards is the introduction of external RAM buffers and an LVDS (low voltage differential signal) converter (the reasons for these inclusions are discussed in further detail later within this chapter). In an ideal world, the PC would be able to directly interact with the Intan IC, however this is not the case so a chain of communication connecting the optrode output to the storage within the computer must be set up, where each component in the chain is required to account for the difference between the ideal case and reality (see fig 8.1 for a block diagram of the recording system).

This chain of communication begins with the Intan IC digitising the electrical signal at the electrode. This digital value must be read periodically with temporally accurate intervals at a timeframe and synchronicity which is possible directly from the PC, and so an intermediatory processor must handle communication with the Intan IC (which in this case is the microprocessor, an FPGA could also be used however as mentioned in Section 7.4.1 the learning curve for these was deemed too steep). The common signalling approach used between the microprocessor and the Intan IC is unfortunately succeptible to errors when transmitted at high data rates and over distance and so a LVDS converter acts to counter this converting the electrical signal into a more robust format. Having retrieved the digitised signal, the microprocessor must pass this data onto the PC which is facilitated by the FT4222H USB Bridge IC introduced in the previous chapter. On paper, these IC's are capable of achieving the required data transfer rates, however in practice the asynchronous manner in which this data is produced (e.g. the microprocessor may be ready to transmit data, but the PC is unable to retrieve) can cause loss of data, and so to remedy this an external RAM buffering system was included.



Figure 8.1: Block diagram of Stim/Recording system. The key elements of the stimulation recording system are shown. Arrows between the boxes demonstrate the communication protocols between devices. Power conversion begins with the 5V from the USB which is brought into the interface board by the FT4222H USB Bridge IC; this is then converted to the various IC supplies.

# 8.3.3 Intan RHS2116 signal acquisition

The Intan RHS2116 has two amplifiers which connect to the recording channel input; a high gain AC coupled amplifier and a low gain DC coupled amplifier, the signals of which can be acquired simultaneously(1). The AC coupled amplifier is used for the capture of neural bio-potentials, the capacitively coupled front ends reject DC signals and the high gain (x192) enables acquisition of these low-amplitude neural signals. Filters on the amplifier provide a bandpass filter with programmable low and high cutoff frequencies (Low pass filter 0.1-20kHz 3rd order butterworth, single pole highpass 0.1-1000Hz filter). The amplified signal is then digitised through a multiplexed 16-bit ADC. The exact configuration of these amplifiers is unknown, however the IC designer (Reid Harrison) has written on amplifier design which suggests it utilises an operational transconductance amplifier with pseudo-resistors to control filter frequencies(2). The low gain (x0.125) DC coupled amplifier directly measures the input channel and is generally used for monitoring electrode potential after stimulation. This is beneficial in the development of an optrode as it can provide a direct measurement of the LEDs potential, therefore allowing direct monitoring of the LEDs quality (e.g. if the LED has failed).



Figure 8.2: Electrical interference of the Stim/Recording system. Electrical interference of the recording channel is anticipated as a key source of recording noise, which will occur at both the optrode and also from within the stimulation/recording hardware. Two pathways for this interference are expected to be via capacitive coupling (highlighted in red). Please note there will be further noise pathways than those shown in the above image.

Artefacts can prevent the faithful recording of neural recordings; these are caused by the introduction of potentials to the amplifier input. Two noise sources which are anticipated to create artefacts (see fig 8.2 for the anticipated electrical interference paths):

- Optrode sourced artefacts: These artefacts can be separated into optically(3) and electrically derived sources(4), (5). The electrical artefacts are mainly caused by mutual capacitance between the recording and stimulating traces, in which changing potentials (i.e at onset and offset of stimulation) inflicts a current in the recording line. The amplifiers have very high input impedance ( $61M\Omega$ ) and so the inflicted current is discharged through the relatively high impedance electrode/tissue interface; where the resulting potential is sampled as an artefact on the recording channel (please note that this is only a proposed hypothesis for the artefact potential). Optically introduced artefacts (bequerel/photovoltaic) are more complicated and depend heavily on probe geometry, materials and the intensity of illumination.
- Recording system noise: The Intan IC has input protection circuitry which prevents damage to the susceptible amplifier inputs from electrostatic discharge. To provide this protection, diodes connect the amplifier inputs to the stimulation power supplies providing a safe route to bleed off charge. Unfortunately, the capacitance of these diodes is sufficient to allow noise from the power lines to capacitively couple to the amplifier inputs. Capacitive coupling will inject noise based on the differential of the voltage signal and so to minimise any artefacts, stable, low noise power supplies should be used. LDO (low dropout) voltage regulators with high PSRR (power-supply rejection ratio, a measure of how immune

the power supply output is to noise in the inputs) were used to provide low noise power supplies; the PSRR is the regulators ability to produce a noise free output from a noisy input.

The Intan IC has methods for artefact removal which may help remove the stimulation locked optrode artefacts:

- Charge recovery: Two charge recovery methods are available, the first is a charge recovery switch connecting the electrode to ground. The second is a charge recovery circuit which uses a programmable current to bring the electrode voltage to a set potential.
- Fast settling function: This feature "reset the amplifiers if a large input signal causes the output signals to saturate" by closing "a switch in an AC high-gain amplifier that drives its analog output to the baseline "zero" level."
- Low-Frequency Cut-off setting: the amplifier recovery time is in part controlled by their frequency response. This feature allows brief increases of the high-pass cut-off frequency, hereby helping the amplifier recover in response to "slow" artefacts.

These artefact reducing features were influential during in the choice of the hardware, as having synchronised control of the stimulation and artefact had potential to create artefact free/reduced recordings.

# 8.3.4 External Ram Buffering

To completely capture the incoming samples at 20kHz, the recording system must be capable of continuously transmitting 12Mbps (Sampling rate\*number of instructions\*size of instruction = 20000Hz\*20 instructions\*32bit per instructions = 12Mbps<sup>1</sup>). This rate can be handled reliably by a microcontroller, however the bottleneck is transmitting to and storing on a computer's hard drive.

A computer using the Windows operating system will occasionally run background tasks which will introduces latencies of 100ms, during which transmitted data may be lost. To counter this, data can be buffered on the microcontroller and retrieved when the host computer is available. Unfortunately, the microcontroller has relatively small amounts of RAM which limits this approach. The microcontroller used was the STM32L432KC, as in the previous chapter, which only contains 64Kbytes of memory equating to 40ms of data recording (more recently advanced microcontrollers (STM32H7 line) have been developed with 1.2MB equivalent 740ms of recording). Evidently this microcontroller has insufficient storage to robustly buffer incoming data, so further storage capabilities are required.

External ram chips (IS65WVS2568GBLL) with a storage capacity of 4Mb each were incorporated onto the design to provide extra buffering. These utilised Quad SPI communication (4 data lines) with a maximum data transmission rate of 45MHz, sufficient for data transmission. However, this memory is only able to communicate with one master at a time; switches were used to facilitate communication with both the microcontroller and the FTDI chip. Low on resistance switches (SN74CB3T3384) were chosen as the low resistance ensures no distortion of the Quad-SPI control signals. This

<sup>&</sup>lt;sup>1</sup>20 instructions are sent to the Intan IC each cycle, 16 ADC conversion requests and 4 stimulation commands. Each of these instructions is 32bits long.

microcontroller acts as the arbiter of these switches, dictating the order of communication.



Coloured switching groups close simultaneously

Figure 8.3: External buffering structure. External ram chips mediate communication between the microcontroller and the FTDI USB-SPI converter. The microcontroller opens/closes switches to coordinate reading/writing of each RAM chip.

## 8.3.5 Bidirectional error-free data communication

Head-fixed neuroscience experiments are carried out in enclosures which may have large number of auxiliary equipment (microscopes, webcams, micromanipulators etc.). To allow for flexibility of experimental setup (especially around the brain) recording systems are generally configured as a small form factor headstage which is then cabled to the control hardware (usually outside the recording enclosure). This cabling needs to be long enough to be practically useful (>50cm). High speed data transferal is trivial when transmitting over short distances on a PCB, however signal integrity can decrease when transferred over long cable distances due to two causes: propagation delays and interference.

Propagation delays occur due to the finite speed of signal transmission through a conductor (5ns/m); as the distance increases, the time delay between a master sending a signal and the slave receiving this signal increases. At low frequencies the effects of propagation delay are negligible; both the transmitter and receiver will experience the same signal at any one time. However, at higher frequencies (where propagation delays are a significant fraction of the signal period) at any given time the transmitter may be seeing a different signal than the receiver.

For synchronous communication protocols (e.g. I2C, SPI etc.) between two systems this can be disastrous. In a uni-directional system (as is the case with the stimulation only system) this communication method is generally immune to propagation delays as the clock and data lines are delayed by the same amount. However, if data is expected to return from the slave, propagation delays will desynchronise the returning data line which manifests as right shifting of the data (See Fig 8.4). In SPI communication, only the MISO line is disrupted as the MOSI is inherently synchronised with the clock line. FPGA circuits can delay sampling of the MISO line to counter this, however this feature is unavailable in microcontrollers. Desynchronisation was overcome by returning the clock signal with the MISO line, creating a clock and data which are synchronised (fig 8.4). A separate SPI port, configured as slave, received the returning data with DMA (Direct Memory Allocation, a feature which allows memory transfer to occur without processor input) to ensure that the received data is immediately buffered without extra

CPU input.



Figure 8.4: **Propagation delays problems and solutions.** Left) Due to propagation delays, incoming MISO lines are desynchronised with the clock; leading to right shifted results. Right) By returning the clock signal with the MISO line, incoming data is returned in synchrony with a clock signal. This can be read in a separate SPI port configured as a slave.

To ensure the data was transmitted without interference, Low Voltage Differential Signalling (LVDS) was used. The microcontroller utilises CMOS logic levels; a binary 1 is represented by a "high" voltage of between 2-3.3V, and a binary 0 is represented by a voltage between 0-0.8V. This transmission modality is not immune to the influence of noise, and deviations of the signal can lead to bit error.

On the other hand, LVDS communicates using two data lines, where the signal is represented by the difference between these lines. It is through this differential that common noise on the signal is rejected; allowing the resolution of correct data from noisy signal lines. To further enhance the common noise rejection, LVDS signals are commonly transmitted in shielded twisted pair cabling. The drawback of this methodology is namely that more hardware is necessary to encode/decode the signals, and secondly that each signal requires twice the number of wires to transmit (flexible high channel count wires can be difficult to source).

#### 8.3.6 Firmware

Two important features which enable the seamless recording of data are: Direct Memory Access (DMA) and double buffering. Without these the required data processing would be too much for the microcontroller's processor to handle.

• **Double buffering:** Digitised recordings are continuously returning to the microcontroller, where it is stored in the microcontroller's SRAM. At the same time, previously retrieved data needs to be sent to the computer for storage. To ensure that outgoing data isn't overwritten during this process, a technique called double buffering is used. Double buffering uses two banks of memory to store/transmit data. As one buffer of data is being retrieved, the second is being transmitted.

Once the first bank of data is full, these buffer's roles swap; this process continues. As long as the second buffer can be transmitted before the first buffer is full, data logging shall occur seamlessly without packet losses.



Figure 8.5: **Double buffering of data.** Two buffers are used which are interleaved between receiving data and transmitting data.

There are two sets of double buffers within the recording system. The primary double buffer occurs within the microcontroller's SRAM; one buffer is used to store incoming data and the second is used to send the buffered data to the external RAM. A secondary double buffer occurs between the two RAM chips, one RAM chip retrieves data from the microcontroller while the second is used for transmission to the computer via the FT4222h.

• Direct Memory Allocation (DMA): DMA allows direct transferral of data between the microcontroller's internal memory and peripheral registers. This is used within the microcontroller to coordinate the reception and transmission of data, without CPU usage. This allows the CPU to focus on ensuring that the correct Intan recording and stimulation commands are updated and transmitted at the correct sampling rate. Two DMA streams are used, the first is used to store all returning digitised samples in the microcontroller's SRAM, the second is used to transmit the buffered data to the external RAM chips.

The data acquisition firmware is founded on these two features, and uses the following process to gather data (displayed graphically in fig 8.6):

- 1. A timer is created at the sampling rate, which is set to produce an interrupt at the given sampling rate.
- 2. Upon receiving a timer interrupt, new digital commands are sent to the Intan Chip using SPI, and the results are buffered in the microcontrollers internal memory using DMA. The digital instruction packet is 20 commands long (4 bytes/command) comprising of 16 ADC conversion requests and 4 instructions to update stimulation registers.
- 3. Every 300 interrupts (equating to reception of 24000bytes), the microcontroller's double buffering swap; previously buffered data is transmitted to the external RAM and a fresh buffer begins collecting data from the Intan chip.
- 4. Every 6000 interrupts, the external RAM double buffering is swapped. The microcontroller configures the switches to the second RAM chips, and raises a GPIO flag to alert the FTDI chip of new data. This flag is recognised by the Labview program, and the FTDI retrieves data from the external ram.
- 5. Every 12000 cycles these cycles return to their initial state.



Figure 8.6: **Graphical interpretations of software cycles:** Left) Cyclical double buffering of data acquisition. Right) Software cycle of Labview program during collection of data.

# 8.3.7 Labview User Interface

A Labview user interface controls communication with the microcontroller via the FTDI USB-SPI bridge. Libraries from FTDI provide communication with this device through device drivers which can be integrated into LABVIEW. This interface allows the user to develop stimulation protocols with control over timing, polarity and magnitude of an individual electrode's stimulation. The protocol is loaded onto the microcontroller (via the intermediator RAM chips). Raising of the FTDIO GPIO pins alerts the microcontroller that the protocol is ready to load. The microcontroller loads the protocol and begins recording from the Intan IC. The Labview program idles until reception of an GPIO flag indicating that a RAM buffer is ready for retrieval. The memory contents are read and the acquired data is presented live to the user, and stored in the hard drive. Two files are created from this program: a binary file of retrieved ADC data and a file denoting the received packet numbers. The packet number is a monotonically increasing 16 bit counter, which provides clarity on packet loss. The user can cease recording, whereupon the FTDI chip will provide an interrupt to the microcontroller and recording will end, reinitialising the Intan IC and microcontroller.

# 8.4 System characterisation

An example recording of a test signal is displayed in figure 8.7. A DAC output (STM32-L49ZG microcontroller source) producing a 1V pk-pk sinusoidal signal (f  $\approx$ 1kHz) which was reduced  $\approx$ 1000 fold through a voltage divider, the resulting signal was recorded on the electrode channel.



Figure 8.7: Sample recording of 1kHZ signal.

Further characterisation of the system was performed to determine the system's noise floor and packet loss ratio.



#### 8.4.1 System noise

Figure 8.8: Noise characteristics of signal. Left) Sampling of the system noise floor with various timeframes. Right) Spectral power of noise floor, inset switching noise spikes (first harmonic at 66Hz).

The recording system's noise was characterised to determine the noise floor and was achieved by grounding the electrodes. A 30 second sample of the acquired signal, recorded in a faraday cage is displayed in figure 8.8; the signal wanders between approximately  $\pm 10\mu$ V interspersed with single sample pulses of up to  $30\mu$ V amplitude.

Test	Packet loss incidents	Total packets lost	Package loss rate
1	0	n/a	n/a
2	1	8	7.00E-04
3	0	n/a	n/a
4	0	n/a	n/a
5	0	n/a	n/a

Table 8.1: **Packet Loss**: Packet loss results for 5 one hour long recordings (12000 packets - each packet is 0.3s of recording). Packet loss was quantified under two conditions: the number of loss events (i.e the frequency of a data packet being missed) and the total data lost.

The RMS noise was calculated to be  $2.7\mu$ V slightly higher the Intan recording IC's specifications(1). These higher amplitude pulses are only single samples and may be removable in post-processing. An example algorithm would be one which windows the recorded samples checking for single sample deviations greater than 3 standard deviations the window's mean and upon detection these could be replaced with the average of the neighbouring values.

These artefacts are suspected to be due to switching noise arising from the control and data transfer systems. The activity of the control system's GPIOs (i.e multiple signals with large and synchronised di/dt or dV/dt components) interferes with the Intan IC's power supply which injects artefacts into the amplifiers inputs through capacitive coupling(see Intan datasheet(1)). Frequency analysis (FFT) of the signal identified noise peaks at 66Hz and its harmonics, supporting the proposition that the external data transfer is the origin of the noise components (the microcontroller writes to the external RAM at periods of 15ms: f=66Hz). This was confirmed by increasing the slew rate of these GPIOs, which resulted in an increase in amplitude of these artefacts (data not shown). The high amplitude amplifier noise is thought to originate from the interface board PCB's design, and it is hoped that by improving this layout would eradicate this switching noise. Examples of principles to improve layout would be:

- **Reference planes**: The return current of a signal generally travels across the reference plane, directly beneath the signal interconnect. Gaps/breaks in this reference plane interrupt the flow of the return current; increasing the inductance of the transmission line. Therefore, increasing noise injected into the system by high di/dt switching events. The guideline here is to ensure that reference planes are as uninterrupted as possible, especially under interconnects.
- Return currents: Shared return paths cause crosstalk; to reduce the influence of this placement of components should prevent/minimise sharing of return paths. In the case above, the power supplies shared return path with the high di/dt digital signals.

# 8.4.2 Packet loss

A counter was appended to each data package sent to the host computer; packet loss could be determined by the observing discrepancies within this counter. The package loss rate was quantified over multiple one hour tests (12000 packets) (see table 8.1); package losses were quantified under two conditions: the number of loss events (i.e the frequency of a data being missed) and the total data lost. The recording system was shown to exhibit packet loss, however this was at a low and unpredictable rate.

Fortunately, the packet counter highlights loss events and by recording the stimulation commands, the log of stimulation is inherently synchronised. The recording system operates in an open-loop configuration and the microcontroller is unaware of the host computers ability to receive data. It is suspected that this is the origin of package losses, as the host computer may be unable to service the USB transfer request, causing a buffer overflow and lost data.

# 8.5 Diagnostic Capabilities

The Intan's onboard DC amplifiers allow monitoring of the LED channel potential, which can be used as a diagnostic measurement of the  $\mu$ LEDs. The IV characteristics of the devices can be derived by applying a ramping current and simultaneously recording the potential; deviations from the standard operation could be indicative of  $\mu$ LED degradation (e.g shorting, open circuits and efficiency changes). This capability is demonstrated in figure 8.9, which compares the exponential IV characteristic response of an off the shelf through-hole mounted LED and the linear IV of a resistive short. This feature could be of particular use for continuous monitoring of  $\mu$ LED health during chronic experimentation. Similar diagnostic functions have been developed on CMOS  $\mu$ LED probes(6).



Figure 8.9: **Diagnostic capabilities of the recording system.** The linear response of resistive shorts can be distinguished from the non-linear behaviour of LEDs. (Step size  $10\mu$ A).

# 8.6 Stimulation artefact suppression

Artefacts distort neural recordings, which can have negative impacts on analysis techniques. Artefact suppression can be achieved by nullifying the artefact before acquisition (front end artefact suppression) or by removing it during post processing (back end artefact suppression) (for further detail on both methods, refer to (7)). Front end techniques focus on preventing amplifier saturation and its subsequent signal loss, or fast recovery methods. Back end artefact suppressing techniques generally rely on signal processing to remove the artefact which is generally processor and memory intensive. For these reasons, front end suppression systems will likely see increased use as the neuroscience field increased adoption of closed-loop and wireless neural control.

The Intan IC has a multiple front end artefact suppression techniques available: electrode grounding, fast settling of amplifiers and frequency switching. These techniques together with pulse-shaping shall be examined for their ability to reject artefacts. The neural probes have not been released and so a complete characterisation of the optical and electrical artefacts is not feasible. However, it is possible to examine the system's response to capacitive coupled artefacts, allowing prediction of optrode operation.

# 8.6.1 Capacitive Coupled Artefacts



Figure 8.10: Capacitive Coupled Artefacts. Left) Circuit used for evaluating artefact in response to stimulation. In neurological experiments, the electrode will be connected to the reference ground through a frequency dependendent impedance (Z), which was simplified to a 200kOhm resistor. Right) measured artefact in response to 1mA pulse.

As stated previously, capacitive coupling between the LED drive lines and the nearby recording electrodes is expected to be the dominant source of electrical crosstalk. The circuit in fig 8.10 was used to examine capacitive crosstalk; a red LNG21LRKR LED was used as in place of a  $\mu$ LED, a 1pF capacitor representative of optrode's intertrack capacitance was included and a 200kOhm resistor was represented electrodetissue interface's impedance. It is recognised that a purely resistive electrode fails to faithfully capture the response a capacitive electrode would provide; however, it offers a point of reference for future use. The capacitive artefact was measured in response to a 1mA current pulse (300ms period, 50ms pulsewidth) shown in fig 8.10 . The predicted artefact at the onset/offset of stimulation is visible, expressing peaks of 1.8mV, which is followed by a low-frequency return to baseline.

#### Electrode grounding

The Intan IC has programmable internal switches which when activated connect the channel to stimulation ground. By grounding the recording channel during onset of stimulation, current bypasses the electrode. This grounding can be brief, only during onset and offset periods. The recording channel can be returned to normalcy during stimulation. This method was tested by switching the Intan's amplifiers to ground for a duration before and after stimulation onset/offset.

The grounding circuitry was able to successfully remove the switching artefact during onset and offset of stimulation (see fig 8.11). Unfortunately, after deactivation of the switch, the potential rebounds producing a large negatively deflecting signal with a duration of 3 samples (0.15ms). Further investigation (not shown) found that this behaviour was independent of stimulation, producing a consistently negative "spike" upon reopening of the switch.



Figure 8.11: **Input Grounding:** Top) Average artefact waveform in response to stimulation. Lower) close up of onset/offset artefacts. Red area is stimulation duration; blue area is grounding duration. The purple region is where both stimulation and grounding overlap operations.

Modelling of the stimulation circuit (LTSpice) suggested this method would be a suitable approach to quickly removing capacitive artefacts. However, in practice it produces similar artefacts to the capacitive crosstalk. This feature may still prove useful under further investigation: systems utilising stimulus switches which hold the amplifier at a given potential during stimulation have demonstrated success in reducing stimulation artefacts(8), (9). However, these designs incorporate further switches which remove contact between the amplifier and electrode.

#### Fast settling of amplifiers

The fast settling feature of the Intan IC "allows users to clamp the output" of the high gain amplifier at baseline(1), work by the amplifier designer suggests that this shorts the amplifier feedback loop(10). This was found to block the artefact, again producing a rebound after cessation of fast settling similar to grounding (see fig 8.12). This method was able to produce a steady baseline during the stimulation pulse, not featuring the low frequency baseline shift of the previous methods.



Figure 8.12: **Fast settling:** Top) Artefact waveform in response to stimulation. Lower) close up of onset/offset artefacts. Red area is stimulation duration; blue area is grounding duration.

#### **Frequency switching**

This method briefly swaps the high pass filter to a higher cut-off frequency (in this case from 5Hz to 1kHz) this allows the greater rejection of the artefacts low frequency artefacts. This feature was applied for a window of 6 samples during onset/offset. As seen by the response in fig 8.13, the amplitude of the artefact is unchanged (since only low frequencies are filtered), however the post onset/offset potential settles to baseline significantly faster than otherwise. Since low frequency artefacts are quickly settled, this rejection method may be of interest during LFP recording.



Figure 8.13: **Frequency switching:** Left) Average artefact waveform in response to stimulation. Red area is stimulation duration; blue area is grounding duration. Right) Comparison of artefacts with and without frequency switching enabled.

#### Pulseshaping

A distinct problem when using a current source  $\mu$ LED stimulator is that due to the LED's non-linear IV response, before the turn on voltage, small changes in current can lead to abrupt voltage changes. This abrupt potential change can further intensify the crosstalk artefacts. One technique of mitigating these effects is through shaping of the stimulation pulse to slow the potential change has been shown to reduce these artefacts(5).



Figure 8.14: Stimulation Artefacts. Recording artefacts in response to ramped stimulation. DAC instruction was ramped to its extents (0 -255b) during a 5ms period (Ramp-onset to Ramp off). An offset was applied to traces for clarity - see legend.

The ability of the system, demonstrated here, to utilise pulse shaping was investigated using the circuit shown in fig 8.10. The stimulation current was ramped through the complete range over a 5ms time period, and the resulting stimulation artefact was recorded in the recording electrode. This was repeated for a variety of step sizes. As expected the artefact size scales with step size; at larger step sizes the largest voltage increase occurs within one step, and thus reduction of artefact is not possible. However, at lower current steps, the voltage increase is spread across more bit-values, and as such the capacitive crosstalk can be mitigated. The 10nA step size offered greatest resolution and so had most control over the final waveform.

As the system is capable of generating arbitrary waveforms, differing pulse shapes (step, ramp, sine and two exponentials) were investigated (Fig 8.15) under a 10nA step size. Again the demonstrating that a slowed increase in current can indeed reduce crosstalk. The most effective shape tested was a slow exponential rise from 50nA to  $2.55\mu$ A.



Figure 8.15: **Pulseshaping** (a-e) (top) Commands for shaped pulse (bottom) Artefact in response to shaped pulse. f) Comparison between greatest and lowest artefact. Signals averaged over 20 pulses.

The traces following the stimulation artefact "spike" are of interest as it demonstrates that there is not a significant rise in potential after the initial turn on. This is well indicated in the exponential pulse which shows that the fast rise in current after turn-on doesn't inflict a strong electrical artefact.

These findings are to be expected considering the LED's IV non-linear response and provide guidelines for the development of two-phase pulse shaping regimes:

• **Phase 1:** To reduce the stimulation artefact, the current should be slowly ramped to the turn-on voltage.

• **Phase 2:** Having passed the most abrupt potential increase, the supply current can now be increased at a greater rate till the desired current is achieved.

To achieve this control while maintaining high illumination capabilities, higher resolution DACs would be required, as pulse shaping was only achievable at nano-amp step sizes. A range of 2.55mA with step size of 10nA would require at least 18bit resolution (which is currently not common for DACs and especially not for high channel count systems). Alternative methods for pulseshaping could be to use

- Voltage/Current controlled DACs: A voltage source could control the initial pulse section, offering better control for less resolution (e.g 10mV steps) which switches to current source to offer greater control over the final stimulation illumination (Hottowy et al demonstrate such a voltage/current DAC(11)).
- Delta-Sigma ( $\Delta\Sigma$ ) Modulation: Mendrela achieved pulse shaping utilising a custom IC, this used a 10 bit DAC utilised a  $\Delta\Sigma$  modulator to dither the output signal (effectively increasing the resolution of the stimulation)(12). Pulse shaping using this system was able to reduce stimulation artefacts from 0.6mV to less than 0.1mV.

# 8.7 Wireless recording

The previous chapter demonstrated that a stimulating system could be achieved using wireless power and control, suggesting that wireless readout is also attainable. A prototype system was created, where the acquired data was transmitted to a micro-SD card.

The electronics of the wireless recording system are similar to the stimulation system; however, the microcontroller was upgraded to a STM32F411RE to enable SDIO communication. Preliminary firmware was developed similar in architecture to the recording system, however, instead of transferring data to a host computer the buffered data is sent to the SD card using a file allocation system (FATFS) to handle file storage.


Figure 8.16: Wireless recording system. Left) block diagram of key operational components. Right) PCB of wireless recording design, scale bar is 1cm.

The prototype PCB was designed and fabricated (see fig 8.16), the extra components expecting to add approximately 0.5g to the total weight. Experience with the wired recording system suggests that robust full frequency band recording of neural signals may not be achievable with a wireless system. SD cards are also susceptible to latencies and are the weakest point in the data acquisition chain.

To mitigate the risk of data loss, a relatively low sampling rate of 1kHz was chosen, allowing recording of LFPs. The reduced demand on the recording system necessitates infrequent writing to the SD card (every 350ms). Preliminary firmware was tested on a microcontroller development board and was shown to be capable of recording data at this data rate.

The power requirements for such a device are expected to be significantly higher than the stimulation alone due to the inclusion of the micro-SD card; writing to the memory card requires up to 100mA current during writes but only  $\approx 0.35$ mA during idleness(13) (the included reference is to a hobbyist data logger blog, which for the interested reader may provide some useful details into the development of low power data logging). The duty cycle of write periods will ultimately dictate the average power consumption, which underpins the feasibility of this device. The duty cycle of write-times is dependent on two factors: the SDIO clock frequency and total data transferred. Currently the clock frequency is configured to 2MHz and requires a throughput of 625kbps (with file writing overheads this duty cycle is just over 50% predicting an average current draw of  $\approx$ 50mA). Improvements could be made by increasing the clock speed (Certain micro-SD cards can be clocked up to 40 MHz, suggesting an average current draw of 2.5mA), however, this may negatively impact the noise characteristics of the recordings. This could be further reduced by only sampling the AC amplifiers, thereby discarding the DC amplifier recordings and halving the required throughput. To provide perspective an increase of 2.5mA current draw on the previous wireless stimulators conditions would still allow recording lasting at least an hour. The prevalence of micro-SD based

neurologgers suggests that the high power consumption during micro-SD card write periods is not a significant obstacle(14), (15).

### 8.8 Closed-loop operation

With the ability to both stimulate and record, the performance of this system in perform closed-loop control mode is of interest. Close-loop control of neurons utilises decision algorithms to apply real-time perturbations to the neural circuitry. This has widespread use in both neuroscience and medical applications. The ability of close-loop stimulation to created cell-specific activity/behaviour linked perturbations is valuable in determining neural function (16), (17). Closed-loop neural stimulation shows potential for the treatment of neurological disorders(18). Little et al demonstrated closed loop treatment of Parkinson's disease associated tremor(19); providing stimulation in response to increased beta wave LFP activity with improved efficacy in comparison to open-loop stimulation. Adaptive stimulation methods have been shown to recognise abnormal ECOG activity and provide on-demand stimulation for seizure prevention in epileptic patients(20). Optogenetic stimulation has already demonstrated successful closed-loop control of central(21), (22) and peripheral(23) targeted treatments in animal models of disease. Further discussion on optogenetic close loop applications is discussed in Grosenick et al(24) and see Edwards et al for a discussion on recent closed-loop optogenetic systems (25).

To investigate the system's closed-loop capabilities, two control algorithms were developed and investigated under benchtop test conditions. Firstly, a simple one-channel thresholding closed loop algorithm was developed (utilising a previous iteration of the recording circuitry), which uses an on/off trigger-able protocol. This protocol detects above-threshold potentials on a single recording channel, and applies stimulation to another channel. An exponentially weighted moving average was incorporated to smooth incoming electrode recordings, thereby preventing single event threshold crossings (noise related events) from triggering the feedback protocol.

The closed loop system was evaluated by measuring the stimulation response to a dummy signal. A wire was attached to a recording channel and dipped into saline. The dummy waveform representing a neural spike was generated by a DAC (NI USB-6259, National Instruments, Texas) was passed through a platinum wire into the saline. The responding electrode current (stimulation of  $1\mu$ A) was driven through a 1M $\Omega$  resistor, and the potential across this electrode was recorded. For this test the amplitude threshold was set at  $-200\mu$ V. The stimulation response was measured using the internal ADCs of the Intan chip.



Figure 8.17: Closed-loop control. Left) Experimental setup. Right) demonstration of close loop capability. The stimulation (red trace) is applied within  $150\mu$ s of the recording signal (blue trace) crossing the  $-200\mu$ V threshold.

The algorithm responds to threshold crossing event within  $150\mu$ s, less than the timeframe of the neurons action potential. Since the processing is carried out by the microcontroller itself, the latency is significantly lower than those of computer based closed-loop systems (the data transfer process can introduce latencies in the order of milliseconds).

Such a close-loop protocols on their own is not particularly indicative of a neural biomarker, and the algorithm is susceptible to false positives from noise sources. This example is more indicative of the microcontroller's ability (and that of the system) to provide externally evoked stimulation in a quick manner. Better use of such an algorithm would be for behavioural experiments involving binary choices e.g. lick-test, a GPIO from the microcontroller could be attached to an external light gate and provide stimulation in response to a correct lick test.

High throughput data transfer (20kHz recording) can be computationally expensive for the STM32L432KC microcontroller, and so it is difficult to run more complicated close-loop algorithms while ensuring the temporal periodicity of recordings. With a reduced CPU load, more complex control can be achieved. The wireless recording system records at 1kHz; this low CPU load allows the incorporation of more complicated protocols; specifically, frequency analysis of the incoming LFPs.

The ability of the wireless recording system to detect frequency spectral powers was demonstrated as a proof of concept. Two microcontrollers were used in this demonstration, one running the proposed wireless firmware and a second which acted as a mock Intan chip providing simulated data of a 1mV pk-pk signal of varying 3Hz/5Hz signal. The simulated signal was acquired by the microcontroller, subsampled to 500Hz and appended to a moving window buffer. A discrete Fourier transform running an FFT algorithm was completed on one channel of recorded data. The FFT was calculated in real time and the results of the 3Hz and 5Hz frequency bins was stored on a micro-SD card alongside the recorded input data. Post processing of the recorded signal in Matlab provided a gold standard showing close comparison to the microcontroller's FFT (Fig 8.18).



Figure 8.18: **Spectral power detection.** The spectral composition of a test signal (alternating 3/5Hz) was calculated using an FFT. Lower graphs compare the micro-controller's attempts with a MATLAB gold standard (Red traces – 5Hz, Blue traces – 3Hz).

The microcontroller was shown to be in close compliance with the Matlab gold standard suggesting that the real time frequency detection was viable. Thresholds can be applied to multiple frequency bins, allowing frequency dependent variation of the Intan's stimulation (fig 8.18). The frequencies demonstrated here are arbitrary and could be extended to more useful bands.

### 8.9 Conclusion

The development of neural recording systems has been discussed. This system was able to record from up to 16 channels at 20kHz, with low data loss. The capability of this system to perform diagnostic and artefact reducing features was evaluated. Pulse shaping proved to be a feasible method to reduce the capactively coupled artefact, however this feature was not viable for use due to the lack of stimulation range. The system was adaptable for wireless recording, and showed promise for future wireless close loop control.

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### Chapter 9

### Conclusions and further work.

### 9.1 Conclusion

The work presented in this thesis details the development of hardware for bidirectional optogenetic experimentation. Neural probes suitable for simultaneous neural stimulation and recording have been, designed, fabricated and characterised. These probes pair optical and electrical stimulation capabilities facilitating the direct comparison of these methods for perturbation of neural circuits which can be validated through on probe recording electrodes. Light output was produced up to  $\approx 100 \text{mW/mm}^2$ ; simulations suggest this is sufficient to correctly stimulate the electrodes recordable volume. A fabrication method for the creation of multi-colour optogenetic stimulators was developed and demonstrated. Red/blue optrodes have been demonstrated, however, this technique could be extended to the whole spectra of  $\mu \text{LED}$  wavelengths; complementing the increasing diversity of opsins. These probes only require singulation through backside grinding and passivation through Parylene coating before their use in neurological experiments.

The stimulation system demonstrated its capability to provide complex and diverse stimulation patterns for both optical and electrical stimulation. Control of up to 16 stimulation sites was achieved with independent control of illumination intensity, pulsewidth and frequency with an update rate of 10kHz. The ability to individually stimulate multiple channels further enhances the stimulation capabilities. This system was successfully transferred to a low-weight wireless stimulator whose low weight (sub 3g) and small scale is suitable for use in freely roaming experimentation. Low power features were implemented, maximising experimental battery life and enabling a run time of over 2 hours. Furthermore, this system has been developed using off the shelf components with common hardware development techniques; both of which lend themselves to be fabricated by an experienced hardware engineer permitting wider dissemination possibilities.

A neural potential recording system was developed, allowing bidirectional interaction with neurons. This hardware was capable of recording from up to 16 channels at 20kHz but ultimately showed intermittent data package loss. A wireless readout prototype was demonstrated with the capability to perform frequency analysis in real time, which could be used for close loop neural control.

### 9.2 Further work

### 9.2.1 Optrodes

Modelling suggested that an optimised design could be created using a guard plane between the electrodes and LED interconnects. A grounded guard layer between electrodes and the driven LEDs is able to restrict the electric field, shielding the electrodes. If the manufacturing challenges posed by this scheme were overcome, this topology would offer significant reductions in the probe's mutual capacitance while maintaining high resolution.

The Intan IC offers bi-phasic stimulation capabilities, which could be harnessed to drive multiple, oppositely biased LEDs with a single trace. This could be advantageous in either reducing the number of traces for a given LED: thereby allowing the development of thinner probes to reduce insertion damage or to utilise in multiplexing efforts to increase channel count. With these guidelines an optrode design has been suggested (fig 9.1), this uses oppositely biased LEDs with a ground plane between electrodes and LED wires. The reduced number of traces allows for wider traces, which may be easier to pattern thin wires onto.



Figure 9.1: **Proposed new neural probe design.**a) probe tip design, featuring 16 LEDs and 16 recording sites. Black scale bar is  $100\mu$ m. b) cross section of probe. c) closeup of tip, green rectangles are p-contact, gold areas are electrode traces. Blue scale bar is  $20\mu$ m. d) proposed operation scheme.

This design may have further improvement on current shielding probes, by bringing the GND plane into electrical contact with the Silicon substrate. Charge carrier creation in the electrically floating substrate is proposed to be a contributor to artefacts(1). However, by defining the potential of these layers it may be possible to reduce the induced artefact.

### 9.2.2 Wireless stimulation/recording

Both wireless system's designs could see immediate improvements in four main areas (in order of importance): communication, stimulation range, power consumption, and size.

- Stimulation Range: The voltage supply range should be increased to facilitate complete coverage of most LEDs for the 0-2.55mA range. This could be achieved by inclusion of new hardware (e.g. The MAX5025/6 variable step-up converter could replace the MAX17220).
- Power consumption: The current draw of both the idle and active stages can be reduced. The sleep current draw is 0.59mA at present, of which 0.35mA is the Vishay IR receiver. This could be significantly reduced, by adding a MOSFET to the IR receiver's power supply lines under the microcontroller's control. While asleep, the IR receiver would be periodically woken up by the microcontroller, check for a "WAKE" command (e.g. a continuous on-off cycle) and then either wake-up completely or continue the deep sleep. A 100ms period of searching for a wake signal every 3s would reduce the total average sleep current by more than half. The current draw of the active stage could possibly be reduced through optimisation of the firmware. The STM32 CPU current consumption is 84  $\mu$ A/MHz and is presently operating at 16MHz, however, the firmware operates at a 10kHz cycle so there are likely redundant clock cycles which can lead to significant reductions. There are also a significant portion of the power consumption which is presently not accounted for, determining where this derives from could provide opportunities to significantly reduce the power draw.
- Size: Smaller footprint components offer significant reductions in system size (WLCSP packaged microcontrollers are available in a  $\frac{1}{4}$  of the area as QFN package microcontrollers). Such savings in size opens the door to two routes. Small package size can lead to reduced weight and bulk devices. Alternatively, the free space could be utilised for the incorporation of extra hardware such as on-board battery charging or FPGAs (see later).

The longer term improvements involve incorporation of wireless power transfer and wireless data transfer and the adoption of new operation techniques.

Wireless power supply: Wirelessly powered optogenetic stimulators have been developed which can operate for extended periods of time due to the continuous wireless power transferal. Such energy harvesting techniques allow battery free use or can be used in conjunction with energy storage components which operation during lapses of power. The wireless system demonstrated above requires at least ≈ 50mW for stimulation and is sensitive to lapses in power; based on other wirelessly powered devices, achieving such power requirements wirelessly is difficult (2), (3)(an exception is the Enercage system, which can provide 122 mW of power, however the additional weight and bulk of this would be prohibitive(4)). An attractive opportunity is the incorporation of wireless power transfer to the wireless system; an additional coil antenna for inductive power transfer could power and recharge the system via additional electronics (proposed block diagram fig 9.2). Recharging could occur between experimental procedures, permitting multi-day chronic experimentation.



Figure 9.2: **Proposed wireless power scheme.**The ST25DV04K is a NFC reader chip with energy harvesting capabilities. Energy harvested power is converted to 5V with the boost converter. This 5V supply is used with the STBC15 which handles system power and battery charging.

- Wireless data transfer: Currently readout from the wireless systems is configured as a micro-SD based data logger. As a data logger, there is no method to see how the recording is in real-time; real time visualisation of recorded potentials would be of specific use for close loop experimentation as it would allow the neuroscientist user to alter stimulation parameters (e.g target power thresholds) on the fly. Wireless communication methods such as Bluetooth Low Energy (BLE) and Visible Light Communication (VLC) would offer viable alternatives/supplements to micro-SD logging. Bluetooth low energy offers a data transfer rate of 2MBits/s, exceeding requirements for 1kHz recording of neural signals, with a power draw of 10mW. VLC has demonstrated GBps data transfer rates. Such systems have been incorporated onto other Intan based wireless neural recording systems, which suggests it would be viable with minimal alteration to the current system(5).
- Operation techniques: Optically stimulating neural probes are being developed with increasing channel count. While this enables diverse neurological experimentation it massively increases the requirements of the stimulator. Multiplexing of the LED interconnects would provide increased efficiency in terms of reducing hardware requirements. The Intan systems biphasic stimulation capabilities could be paired with the microcontrollers GPIO's tri-state operation (Pin state = VDD/GND/High-Z) to achieve control over a significant number of LEDs. An example of multiplexing utilising the Intan IC outputs and the microcontroller GPIO pins is demonstrated in fig 9.3. This method of course requires particular attention to design and fabrication as any shorts could be detrimental to multiple LEDs. This could be minimised using high resolution photolithography techniques; probes individual p and n interconnects could be fabricated and the multiplexing achieved on the PCB.



Number of LEDS = Number of stimulation channels\*2\*Number of GPIOs

Figure 9.3: Channel multiplexing. This multiplexing arrangement provides the control of a large number of LEDs. Individual red group LEDs are turned on by applying a positive current and setting the desired GPIO LOW (all other GPIOs to High-Z). Blue group LEDs are turned on by setting the GPIO to low state (all other GPIOs to High-Z) and applying a negative current. The colour coding is intentional; the configuration above gives red group a voltage swing up from GND to Vstim +ve, while the blue group has a voltage swing of Vstim –ve to +3V). This higher voltage swing would be more suitable for high bandgap LEDs (blue GaN LEDs) and the lower voltage swing would be more suitable for lower bandgap LEDs (red AlGaN LEDs).

### 9.2.3 Wired Stimulation/Recording

The wired recording will likely be held back by the poor processing capabilities of the STM32L432KC and should be upgraded to a more powerful microcontroller/FPGA (e.g the STM32H7 series microcontrollers, these have dual core processors capable of clocking up to 480 MHz, a six-fold increase on the STM32L4 series). Higher performance microcontroller systems may enable the development of a more robust data retrieval systems through advanced features. One feature being flexible memory controller (FMC) which allows the microcontroller to interface with high capacity external memory, allowing up to 512 Mbyte SDRAM (512x the current memory capabilities). Dual core microcontrollers provide an option for one processor core to handle control of data acquisition and stimulation, and the second microcontroller could operate closedloop algorithms on incoming data. A possible new framework is described in fig 9.4. For wired systems where weight and space are not at a premium, it may be beneficial to shift from using the Intan RHS2116 to a DAC (e.g TI DAC81416 – 16bit 16 channel voltage DAC) and a RHD2116 Digital Amplifier. This would offer a 16 stimulation channels and 32 recording channels. Higher resolution DAC under independent control from the recording (currently the DAC is updated at the sampling rate, it may be more beneficial to have this operating faster) may allow for better control of the pulse shaping. On the other hand, this setup would require more hardware and some features would be lost (e.g. electrical stimulation).



Figure 9.4: **Proposed STM32H7 based stim/record architecture.** This system utilises the dual-core processors. Processor 1's CPU handles the delivery of instructions to the Intan IC. DMA is used to buffer incoming data and return it to the host computer. The second processor could be used for the completion of close loop algorithms, the results of which can be used to determine the Intan's instructions.

### 9.2.4 Closed loop

The closed loop examples are in preliminary stages and require characterisation to ensure their robustness in use. The initial approach for this would be to upload previously recorded LFP signals into the "mock" Intan, and see if the closed-loop algorithm provided adequate detection and stimulation.

Other biosignals could be examined; however, to ensure robust recognition by the microcontroller, the biosignal should be straightforward to detect (e.g. the QRS complex detection for cardiac optogenetics(6)). For more complex detection of bio-signals, FP-GAs could be introduced to handle processing. There is a variety of FPGA based spike sorting systems which have enabled spike sorting on hardware(7)–(8) which could possibly be achieved for wireless sorting through the use of low power FPGAs such as ICE40 or IGLOO nano range.

### 9.3 Other Comments

The work shown here demonstrates some exciting outcomes which prove that high performance systems can be developed based on accessible hardware. A lot of the work presented here has been facilitated by the current trends in electronics; e.g. increased miniaturisation and adoption of low power schemes for use in IOT and wearables. The interested reader should look to these trends as there may be direct benefits for neurotechnology; for example, edge based AI systems are being developed which allow the local processing of AI algorithms on a hardware device (e.g. Google Coral TPU), may provide new frameworks for closed-loop systems.

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### Appendices

Appendix A

### Microfabrication recipes

### A.1 PECVD recipes

Recipe	Oxide200.rec
Gasses (Flow rate in sccm)	SiH4 (170) N2O (710) He (16)
Power (W)	70
Pressure (T)	1
Deposition rate (nm/min)	3
Temperature	300C

Table A.1: Oxide200: Silicon Dioxide deposition recipe.

### A.2 Etch recipes

### A.2.1 RIE1 - Dielectric etches

Recipe	mlesio2.rec
Gasses	CHF3 $(5)$
(Flow rate in sccm)	Ar $(15)$
Power (W)	120
Pressure (mT)	30
Etch rate (nm/min)	3

Table A.2: SiO2 etch

### A.2.2 RIE2 - Metal etches

Posino	Parmetal.rec				
necipe	Step 1 (Gold etch)	Step 2 (Ti Etch)			
Gasses	$\Lambda r(40)$	Ar()			
(Flow rate in sccm)	AI(40)	SF6()			
Power	200	200			
(W)	300	200			
Pressure	45	45			
(mT)	40				
Etch rate	2	3			
(nm/min)	J				

Table A.3: Parmetal etch used for the etching of Ti/Au tracks

### APPENDIX A. MICROFABRICATION RECIPES

Recipe	NiAutest.rec
Gasses	Ar (40)
(Flow rate in sccm)	O2(4)
Power (W)	300
Pressure (mT)	45
Etch rate (nm/min)	3

### A.3 ICP recipes

Recipe	KHSGan4.rec					
Gasses	Ar (10)					
(Flow rate in sccm)	Cl(30)					
Power (W)	200					
Pressure (mT)	5					
Etch rate (nm/min)	$GaN \approx 450 \text{ SiO}2 \approx 50$					

Table A.5: Etch recipes for ICP etching of GaN semiconductor

Appendix B

### Wireless Optogenetic Stimulator Schematics



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Appendix C

### **Recording/Stimulating system**

### FT4222h

	GND	FT_QUAD_103	FT_QUAD_IO2	GND	FT_QUAD_IO0	FT_QUAD_IO1	FT_QUAD_CLK	GND		GND
P\$1 P\$2	P\$3	P\$4	P\$5	P\$6	P\$7	P\$8	P\$9	P\$10	P\$11	P\$12
VCCIO V_OUT_3V3	GND	103	102	GND	MOSVID0	MISO/I01	CLK	GND	P\$11	GND
V_BUS VCC	GND	GPI00	GPI01	GPI02	GPI03	GND	SSIO	P\$15	SS	GND
P\$24 P\$23	P\$22	P\$21	P\$20	P\$19	P\$18	P\$17	NSS P\$16	P\$15	P\$14	P\$13
V_5V	GND		GPI01	GPI02	GPI03	GND	FT_QUAL			GND

### Microcontroller



# RAM & Switches













## Power Supplies



# LVDS tranciever





# **HDMI** Connector



### **Microcontroller Firmware Code**

```
/**
* @file
               : main.c
* @brief
               : Main program body
** This notice applies to any and all portions of this file
* that are not between comment pairs USER CODE BEGIN and
* USER CODE END. Other portions of this file, whether
* inserted by the user or by software development tools
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* DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT HOLDER OR CONTRIBUTORS BE LIABLE
* FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL
* DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR
* SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER
* CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY,
* OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE
* OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
*/
                       -----*/
/* Includes -----
#include "main.h"
#include "stm3214xx hal.h"
/* USER CODE BEGIN Includes */
#include "State Machine definitions.h"
/* USER CODE END Includes */
/* Private variables -----*/
QSPI HandleTypeDef hqspi;
static DMA HandleTypeDef hdma;
static DMA_HandleTypeDef hdma2;
/* USER CODE BEGIN PV */
/* Defines
```

```
*/
//GPIO Pins for selecting memory banks
#define BANK_SELECT1 LL_GPI0_PIN_5
#define BANK_SELECT2 LL_GPI0_PIN_8
/* Private variables ------*/
uint16_t Data_Size= 12000;
static volatile uint16_t Data[400];
//Internal Double_Buffers
static volatile uint16_t Data1[12000];
static volatile uint16_t Data2[12000];
static volatile uint16 t DataRx[240];
//Variables used to develop the stimulation pulse
static volatile uint16_t Stim_Counter[16];
static volatile uint16 t Stim Pos Amp[16];
static volatile uint16 t Stim Neg Amp[16];
static volatile uint16 t Stim Pos Limit[16];
static volatile uint16_t Stim_Neg_Limit[16];
static volatile uint16 t Stim Off Limit[16];
static volatile uint16 t Stim Mask;
static volatile uint16_t Stim_On_Off;
static volatile uint16_t Stim_Pol;
static volatile uint16_t Pulse_Count[16];
static volatile uint16_t Pulse_Number[16];
static volatile uint16_t Stim_Bit ;
static volatile uint16_t Refractory_Num[16];
static volatile uint16_t Refractory_Count[16];
static volatile uint16_t Refractory_Bit ;
//variables used to define the IV characteristics
static volatile uint16 t IV Loop i;
static volatile uint8_t IV_Loop_j;
//variables used in the transmission of data to the host computer
static volatile uint8_t Transmit_State = Transfer_Idle;
static volatile uint32_t Transmit_Address = 0;
static volatile
                   uint8_t Transmit_Switch = 2;
static volatile uint8_t Test1 ;
static volatile uint8_t dat;
static volatile uint16_t Counter;
static volatile uint16_t Counter2;
static volatile uint8_t Record_Choice = 0;
static volatile
                   uint8_t State = Initial;
static volatile uint8_t Program_Choice = 0;
static volatile uint8_t Restart = 1;
static volatile uint8_t pRD =0;
static volatile uint8_t Reset_Flag = 0;
static volatile
                   uint16_t Temp_1;
```

uint8\_t dummy;

```
static volatile uint16_t Transmit_Counter = 0;
static volatile uint8_t qq = 0;
```

```
static volatile uint16_t Temporary_Var;
static volatile uint32_t tmp_32;
static volatile uint16_t Recovery_Switch = 0;
```

//Intan\_Initialisation Commands

uint16\_t Commands[62] =

{49407,49407,49407,49407,32800,32801,32806,27136,32768,32769,32770,32771,32772,32773, 32774,32775,32776,40970,40972,32802,32803,32804,32805,41002,41004,41006,41008,41024,4 1025,41026,41027,41028,41029,41030,41031,41032,41033,41034,41035,41036,41037,41038,41 039,41056,41057,41058,41059,41060,41061,41062,41063,41064,41065,41066,41067,41068,410 69,41070,41071,32800,32801,53503}; uint16 t Registers[62] =

```
uint16_t test1,test2;
/* USER CODE END PV */
```

/\* Private function prototypes -----\*/ void SystemClock\_Config(void); static void MX\_GPI0\_Init(void); static void MX\_QUADSPI\_Init(void); static void MX\_SPI1\_Init(void); static void MX\_SPI3\_Init(void); static void Config\_Memory\_Banks(void); static void MX\_TIM1\_Init(void); static void Select\_Program(void); static void Intan com(void); static void Initialise Intan(void); static void Test\_IV(void); static void Initialise\_All(void); static void Read\_Protocol(void); /\* USER CODE BEGIN PFP \*/ /\* Private function prototypes -----\*/ /\* USER CODE END PFP \*/ /\* USER CODE BEGIN 0 \*/

```
//Timer interrupt, this sets the state machine to "Timer event", bringing the state
machine out of the idle state
extern void TIM2_IRQHandler()
{
    if(((TIM2->SR & TIM_SR_UIF) == TIM_SR_UIF))
    {
        /* Clear the update interrupt flag*/
```

```
(TIM2->SR = ~TIM_SR_UIF);
```

}

```
State = Timer_Event;
}
//External GPIO interrupt, this sets the reset flag high to reset the firmware.
extern void EXTI15_10_IRQHandler(void)
{
      if ((READ_BIT(EXTI->PR1, EXTI_IMR1_IM10) == (EXTI_IMR1_IM10))!=RESET)
      {
            Reset_Flag = 1;
            //Clear the EXTI pending bits
            WRITE_REG(EXTI->PR1, EXTI_IMR1_IM10);
      }
}
/* USER CODE END 0 */
/**
* @brief The application entry point.
*
* @retval None
*/
int main(void)
{
      /* USER CODE BEGIN 1 */
      /* USER CODE END 1 */
      /* MCU Configuration-----
                                                   -----
                                                              */
      /* Reset of all peripherals, Initializes the Flash interface and the Systick.
*/
      HAL Init();
      HAL Delay(50);
      /* USER CODE BEGIN Init */
      /* USER CODE END Init */
      /* Configure the system clock */
      SystemClock_Config();
      /* USER CODE BEGIN SysInit */
      /* USER CODE END SysInit */
      Data[0] = 1;
      Data[2] = 1;
      /* USER CODE END 2 */
      /* Infinite loop */
      /* USER CODE BEGIN WHILE */
      //select stm32 as writer to bank 1
```

```
//Runs initialisation registers for the the Intan system and returns variables
to their initial values
      Initialise All();
      //Sets the program state to "program select" here it will await a program
selection from the user.
      //After this it will run that program till it the reset pin is toggled
      State = Program_Select;
      while (1)
      {
             /* USER CODE END WHILE */
             /* USER CODE BEGIN 3 */
             switch (State)
             {
             case Idle:
                    if (Reset Flag == 1){
                          Reset Flag = 0;
                          //turn off timer
                          CLEAR_BIT (TIM2->CR1,TIM_CR1_CEN);
                          State = Reinitialise;
                          //State = Program_Select;
                          //set state to reinit.
                    }
                    break;
             case Initial:
                   11
                                              GPIOA->BSRR = GPIO_BSRR_BS2;
                    //
                                              GPIOA->BSRR = GPIO_BSRR_BR2;
                    State = Timer_Event;
                    break;
             case IV_INIT:
                    Test IV();
                    State = Idle;
                    break;
             case Record Init:
                    //turn on the correct memory bank
                    SET_BIT(GPIOA->BSRR, BANK_SELECT1);
                    SET_BIT(GPIOA->BRR, BANK_SELECT2);
                    while (((GPIOB->IDR & LL_GPIO_PIN_7) == 0)){
                    }
                    SET_BIT(GPIOA->BRR, BANK_SELECT1);
                    SET_BIT(GPIOA->BSRR, BANK_SELECT2);
                    //read protocol from memory bank into DataRx
                    Read_Protocol();
                    //return memory bank to initial convention
                    SET_BIT(GPIOA->BRR, BANK_SELECT1);
                    SET_BIT(GPIOA->BSRR, BANK_SELECT2);
                    SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
                    SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
                    //Set up the DMA for recording: set memory to peripheral
                    SET_BIT(DMA1->IFCR, DMA_IFCR_CTCIF5|DMA_IFCR_CHTIF5);
                    DMA1_Channel5->CCR &= ~DMA_CCR_EN;
```

```
tmp_32 = DMA1_Channel5->CCR;
                    tmp_32 &= (uint32_t)~(DMA_CCR_DIR);
                    tmp_32 |= DMA_MEMORY_TO_PERIPH;
                    DMA1 Channel5->CCR = tmp_32;
                    SET_BIT(GPIOB->BSRR, LL_GPIO_PIN_6);
                    HAL_Delay(1);
                    HAL_Delay(500);
                    while (((GPIOB->IDR & LL_GPIO_PIN_7) == 0)){
                    }
                    //deconstruct the data packet
                    //DataRX[1] = Which Stimulation channels are to be used.
                    Stim_Bit = (0xFFFF & (DataRx[1]));
                    Stim_Mask = Stim_Bit;
                    //DataRX[1] = Which Stimulation channels have a refractory
period.
                    Refractory Bit = (0xFFFF & (DataRx[2]));
                    uint8 t iii;
                    //DataRx[3]-DataRx[114] are the various protocol values
                    for (iii = 0;iii<15;iii++){</pre>
                           Stim_Pos_Amp[iii]=(DataRx[(uint16_t)((iii*7)+3)]);
                           Stim_Neg_Amp[iii]= (DataRx[(uint16_t)((iii*7)+4)]);
                           Stim_Off_Limit[iii]= (DataRx[(uint16_t)((iii*7)+5)]);
                           Stim_Pos_Limit[iii] =(DataRx[(uint16_t)((iii*7)+6)]);
                           Stim_Neg_Limit[iii] = (DataRx[(uint16_t)((iii*7)+7)]) ;
                           Pulse_Number[iii] = (DataRx[(uint16_t)((iii*7)+8)]) ;
                           Refractory_Num[iii] = (DataRx[(uint16_t)((iii*7)+9)]);
                    }
                    //set Step polarity to positive current for all channels.
                    SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
                    Temporary Var = (uint16 t) ((1 << 15) + (44));
                    SPI1->DR = Temporary Var;
                    while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
                    }:
                    Temporary_Var = (uint16_t)255;
                    SPI1->DR = Temporary Var;
                    while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
                    };
                    SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
                    //Update channels
                    SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
                    Temporary_Var = (uint16_t)57599;
                    SPI1->DR = Temporary_Var;
                    while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
                    };
                    Temporary_Var = (uint16_t)0;
                    SPI1 \rightarrow DR = 0;
                    while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
                    };
                    SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
```

```
HAL_Delay(1);
                    while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
                    };
                    SET BIT(GPIOA->BSRR, LL GPIO PIN 4);
                    //Update Positive and negative current amplitudes for each
channel
                    for (iii = 0;iii<15;iii++){</pre>
                           //Toggle pin low;
                           SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
                           Temporary_Var = (uint16_t) ((32768)+(96+(iii)));
                           SPI1->DR = Temporary_Var;
                           while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
                           };
                           Temporary_Var =
(uint16_t)((uint16_t)(128<<8)|(uint16_t)(Stim_Pos_Amp[iii]));</pre>
                           SPI1->DR = Temporary_Var;
                           while ((LL SPI IsActiveFlag BSY(SPI1) == 1)){
                           };
                           SET BIT(GPIOA->BSRR, LL GPIO PIN 4);
                           //Toggle pin high
                           //Toggle pin low;
                           SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
                           Temporary_Var = (uint16_t) ((32768)+(64+(iii)));
                           SPI1->DR = Temporary_Var;
                           while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
                           };
                           Temporary_Var =
(uint16_t)((uint16_t)(128<<8)|(uint16_t)(Stim_Neg_Amp[iii]));</pre>
                           SPI1->DR = Temporary_Var;
                           while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
                           };
                           SET BIT(GPIOA->BSRR, LL GPIO PIN 4);
                           //Toggle pin high
                    }
                    //Initialise the timer, which shoul begin recording.
                    MX_TIM1_Init();
                    State = Idle;
                    break;
                    //This selects the various programs and is the start of where any
additional features should be included
             case Program_Select:
                    switch (Program_Choice){
                    case IV:
                           State = IV_INIT;
                           break;
                    case Record:
                           State = Record_Init;
                           break;
                    default:
                           State = Idle;
                           break;
```

} break; //Reinitialises all variable on reset. **case** Reinitialise: Reset\_Flag = 0; SET\_BIT(GPIOA->BRR, LL\_GPIO\_PIN\_9); Initialise\_All(); State = Program\_Select; break; // On a timer event it will request ADC conversions from the Intan IC case Timer\_Event: Intan\_com(); State = Transmit Data; break; //Transmit data determines if and how the data should be transmitted back to the host computer. // The Counter variable determines which external RAM bank the data is sent to and which memory address // This also handles the flags to the FT4222h which inform it to retrieve new data case Transmit\_Data: switch(Counter){ case 0: if (Transmit\_Address >478144 ){ Transmit\_Address = 0; if (Transmit\_Switch > 1){ Transmit\_State = Transfer\_Check2; Transmit\_Switch = 1; }else{ Transmit\_State = Transfer\_Check3; Transmit\_Switch = 2; } } break; case 1: if (Transmit Address == 240000 ){ Transmit Address = 262144; SET\_BIT(GPIOA->BRR, LL\_GPIO\_PIN\_9); } break; case 298: Transmit\_Counter++; if (Transmit\_Counter == 20){ Counter2++; Transmit\_Counter =0; } break; case 299: WRITE\_REG(QUADSPI->FCR, (QSPI\_FLAG\_TE | QSPI\_FLAG\_TC)); //Turn off DMA DMA1\_Channel5->CCR &= ~DMA\_CCR\_EN;
```
DMA1_Channel5->CNDTR = (uint32_t)24000;
                                 DMA1_Channel5->CPAR = (uint32_t)&(QUADSPI->DR);
                                 WRITE_REG(QUADSPI->DLR, (( sizeof(Data2) )-1));
                                 MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE,
0x00000000);
                                 MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_INSTRUCTION,
0x02);
                                 break;
                          case 300:
                                 Transmit_State = Transmit;
                                 CLEAR_BIT(DMA2->ISR, DMA_ISR_TCIF1);
                                 CLEAR_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
                                 Data2[0]=Counter2;
                                 CLEAR_BIT(DMA1_Channel5->CCR, DMA_CCR_EN);
                                 DMA1_Channel5->CMAR = (uint32_t)&Data2;
                                 DMA2_Channel1->CMAR = (uint32_t)&Data1;
                                 DMA2_Channel1->CNDTR = (uint32_t)12000;
                                 DMA2_Channel1->CPAR = (uint32_t)&(SPI3->DR);
                                 SET BIT(DMA2 Channel1->CCR, DMA CCR EN);
                                 //Counter2++;
                                 break;
                          case 301:
                                 if (Transmit_Address >478144 ){
                                        Transmit Address = 0;
                                        if (Transmit_Switch > 1){
                                               Transmit_State = Transfer_Check2;
                                               Transmit_Switch = 1;
                                        }else{
                                               Transmit_State = Transfer_Check3;
                                              Transmit_Switch = 2;
                                        }
                                 }
                                 break;
                          case 302:
                                 if (Transmit Address == 240000 ){
                                        Transmit Address = 262144;
                                        SET_BIT(GPIOA->BRR, LL_GPIO_PIN_9);
                                 }
                                 break;
                          case 598:
                                 Transmit_Counter++;
                                 if (Transmit_Counter == 20){
                                        Counter2++;
                                        Transmit_Counter =0;
                                 }
                                 break;
                          case 599:
                                 WRITE_REG(QUADSPI->FCR, (QSPI_FLAG_TE |
QSPI_FLAG_TC));
                                 //Turn off DMA
                                 DMA1_Channel5->CCR &= ~DMA_CCR_EN;
                                 DMA1 Channel5->CNDTR = (uint32 t)24000;
                                 DMA1 Channel5->CPAR = (uint32 t)&(QUADSPI->DR);
                                 WRITE_REG(QUADSPI->DLR, (( sizeof(Data2) )-1));
```

```
MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE,
0x00000000);
                                 MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_INSTRUCTION,
0x02);
                                 break;
                          case 600:
                                 Transmit_State = Transmit;
                                 while(((READ_BIT(DMA2->ISR, DMA_ISR_TCIF1) ==
(DMA_ISR_TCIF1)) ? 1UL : 0UL)==0){
                                 CLEAR_BIT(DMA2->ISR, DMA_ISR_TCIF1);
                                 CLEAR_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
                                 Data1[0]=Counter2;
                                 CLEAR_BIT(DMA1_Channel5->CCR, DMA_CCR_EN);
                                 DMA1_Channel5->CMAR = (uint32_t)&Data1;
                                 DMA2_Channel1->CMAR = (uint32_t)&Data2;
                                 DMA2_Channel1->CNDTR = (uint32_t)12000;
                                 DMA2_Channel1->CPAR = (uint32_t)&(SPI3->DR);
                                 SET BIT(DMA2 Channel1->CCR, DMA CCR EN);
                                 //Counter = 0;
                                 //Counter2++;
                                 //comment
                                 Counter = 0;
                                 //comment
                                 break;
                          default:
                                 break;
                          }
                          switch(Transmit_State){
                          case Transmit:
                                 WRITE_REG(QUADSPI->AR, (uint32_t)Transmit_Address);
                                 DMA1_Channel5->CCR |= DMA_CCR_EN;
                                 QUADSPI->CR |= QUADSPI CR DMAEN;
                                 Transmit State = Transfer Check;
                                 Transmit_Address = Transmit_Address + 24000;
                                 break;
                          case (Transfer_Check):
                                                     if(((READ_BIT(DMA1->ISR,
DMA_ISR_TCIF5) == (DMA_ISR_TCIF5)) ? 1UL : 0UL)==1)
                                                     {
                                                            SET_BIT(DMA1->IFCR,
DMA_IFCR_CTCIF5|DMA_IFCR_CHTIF5);
                                                            Transmit_State =
Transfer_Idle;
```

break;

break; case (Transfer\_Check2):

```
if(((READ_BIT(DMA1->ISR, DMA_ISR_TCIF5) ==
(DMA_ISR_TCIF5)) ? 1UL : 0UL)==1){
```

```
SET_BIT(DMA1->IFCR,
DMA_IFCR_CTCIF5|DMA_IFCR_CHTIF5);
```

SET\_BIT(GPIOA->BSRR, BANK\_SELECT1);

SET\_BIT(GPIOA->BRR, BANK\_SELECT2);

SET\_BIT(GPIOA->BSRR, LL\_GPIO\_PIN\_9);

Transmit\_State = Transfer\_Idle;

}

}
break;
case (Transfer\_Check3):

```
if(((READ_BIT(DMA1->ISR, DMA_ISR_TCIF5) ==
(DMA_ISR_TCIF5)) ? 1UL : 0UL)==1){
```

SET\_BIT(DMA1->IFCR, DMA\_IFCR\_CTCIF5|DMA\_IFCR\_CHTIF5);

SET\_BIT(GPIOA->BRR, BANK\_SELECT1);

SET\_BIT(GPIOA->BSRR, BANK\_SELECT2);

SET\_BIT(GPIOA->BSRR, LL\_GPIO\_PIN\_9);

Transmit\_State = Transfer\_Idle;

```
}
                          break;
                          case (Transfer_Idle):
                                                                                break;
                          }
                          State = Idle;
                          break;
             }
      }
      /* USER CODE END 3 */
}
/**
 * @brief System Clock Configuration
 * @retval None
 */
void SystemClock_Config(void)
{
      RCC_OscInitTypeDef RCC_OscInitStruct = {0};
      RCC_ClkInitTypeDef RCC_ClkInitStruct = {0};
      /** Initializes the CPU, AHB and APB busses clocks
       */
      RCC OscInitStruct.OscillatorType = RCC OSCILLATORTYPE HSI;
      RCC OscInitStruct.HSIState = RCC HSI ON;
      RCC_OscInitStruct.HSICalibrationValue = RCC_HSICALIBRATION_DEFAULT;
      RCC_OscInitStruct.PLL.PLLState = RCC_PLL_ON;
      RCC_OscInitStruct.PLL.PLLSource = RCC_PLLSOURCE_HSI;
      RCC_OscInitStruct.PLL.PLLM = 1;
      RCC_OscInitStruct.PLL.PLLN = 10;
      RCC_OscInitStruct.PLL.PLLP = RCC_PLLP_DIV7;
      RCC_OscInitStruct.PLL.PLLQ = RCC_PLLQ_DIV2;
      RCC_OscInitStruct.PLL.PLLR = RCC_PLLR_DIV2;
      if (HAL_RCC_OscConfig(&RCC_OscInitStruct) != HAL_OK)
      {
             // Error_Handler();
      }
      /** Initializes the CPU, AHB and APB busses clocks
       */
      RCC_ClkInitStruct.ClockType = RCC_CLOCKTYPE_HCLK|RCC_CLOCKTYPE_SYSCLK
                    |RCC_CLOCKTYPE_PCLK1|RCC_CLOCKTYPE_PCLK2;
      RCC ClkInitStruct.SYSCLKSource = RCC SYSCLKSOURCE PLLCLK;
      RCC_ClkInitStruct.AHBCLKDivider = RCC_SYSCLK_DIV1;
```

```
RCC_ClkInitStruct.APB1CLKDivider = RCC_HCLK_DIV1;
      RCC_ClkInitStruct.APB2CLKDivider = RCC_HCLK_DIV1;
      if (HAL_RCC_ClockConfig(&RCC_ClkInitStruct, FLASH_LATENCY_4) != HAL_OK)
      {
             //Error_Handler();
      }
      /** Configure the main internal regulator output voltage
       */
      if (HAL PWREx ControlVoltageScaling(PWR REGULATOR VOLTAGE SCALE1) != HAL OK)
      {
             //Error_Handler();
      }
}
/* QUADSPI init function */
static void MX_QUADSPI_Init(void)
{
      HAL RCC QSPI CLK ENABLE();
      /* GPIO Ports Clock Enable */
      LL_AHB2_GRP1_EnableClock(LL_AHB2_GRP1_PERIPH_GPIOA);
      LL_AHB2_GRP1_EnableClock(LL_AHB2_GRP1_PERIPH_GPIOB);
      //Quad SPI GPIO
      LL_GPI0_InitTypeDef GPI0_InitStruct;
      //PA2 - NSS
      //PA3 - QUADSPI_CLK
      //PA6 - QUADSPI_BK1_IO3
      //PA7 - QUADSPI_BK1_IO2
      //PB0 QUADSPI_BK1_I01
      //PB1 QUADSPI_BK1_IO0
      GPI0_InitStruct.Pin = LL_GPI0_PIN_2;
      GPIO InitStruct.Mode = LL GPIO MODE ALTERNATE;
      GPIO InitStruct.Speed = LL GPIO SPEED FREQ MEDIUM;
      GPIO InitStruct.OutputType = LL GPIO OUTPUT PUSHPULL;
      GPIO InitStruct.Pull = LL GPIO PULL NO;
      GPIO InitStruct.Alternate = LL GPIO AF 10;
      LL GPIO Init(GPIOA, &GPIO InitStruct);
      GPIO_InitStruct.Pin = LL_GPIO_PIN_3|LL_GPIO_PIN_6|LL_GPIO_PIN_7;
      GPI0_InitStruct.Mode = LL_GPI0_MODE_ALTERNATE;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
      GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
      GPI0_InitStruct.Pull = LL_GPI0_PULL_NO;
      GPI0_InitStruct.Alternate = LL_GPI0_AF_10;
      LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
      GPI0_InitStruct.Pin = LL_GPI0_PIN_0|LL_GPI0_PIN_1;
      GPI0_InitStruct.Mode = LL_GPI0_MODE_ALTERNATE;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
      GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
      GPIO InitStruct.Pull = LL GPIO PULL NO;
      GPIO InitStruct.Alternate = LL GPIO AF 10;
      LL_GPI0_Init(GPI0B, &GPI0_InitStruct);
```

```
/* QUADSPI parameter configuration*/
      hqspi.Instance = QUADSPI;
      hqspi.Init.ClockPrescaler = 2;
      hqspi.Init.FifoThreshold = 1;
      hqspi.Init.SampleShifting = QSPI_SAMPLE_SHIFTING_NONE;
      hqspi.Init.FlashSize = 30;
      hqspi.Init.ChipSelectHighTime = QSPI_CS_HIGH_TIME_1 CYCLE;
      hqspi.Init.ClockMode = QSPI_CLOCK_MODE_0;
      hqspi.Init.FlashID = QSPI_FLASH_ID_1;
      hqspi.Init.DualFlash = QSPI_DUALFLASH_DISABLE;
      if (HAL_QSPI_Init(&hqspi) != HAL_OK)
      {
             _Error_Handler(__FILE__, __LINE__);
      }
        HAL_RCC_DMA1_CLK_ENABLE();
      hdma.Instance = DMA1_Channel5;
      hdma.Init.Request = DMA REQUEST 5;
      hdma.Init.Direction = DMA MEMORY TO PERIPH;
      hdma.Init.PeriphInc = DMA PINC DISABLE;
      hdma.Init.MemInc = DMA MINC ENABLE;
      hdma.Init.PeriphDataAlignment = DMA PDATAALIGN BYTE;
      hdma.Init.MemDataAlignment = DMA_MDATAALIGN_BYTE;
      hdma.Init.Mode = DMA NORMAL;
      hdma.Init.Priority = DMA_PRIORITY_HIGH;
        _HAL_LINKDMA(&hqspi,hdma,hdma);
      HAL_DMA_Init(&hdma);
      HAL_NVIC_SetPriority(DMA1_Channel5_IRQn, 0, 0);
      HAL_NVIC_EnableIRQ(DMA1_Channel5_IRQn);
      //__HAL_DMA_ENABLE(&hdma);
      ((QUADSPI->CR) |= (QUADSPI CR EN));
/* SPI1 init function */
static void MX SPI1 Init(void)
      LL_SPI_InitTypeDef SPI_InitStruct;
      LL_GPI0_InitTypeDef GPI0_InitStruct;
      /* Peripheral clock enable */
      LL_APB2_GRP1_EnableClock(LL_APB2_GRP1_PERIPH_SPI1);
      /**SPI1 GPIO Configuration
 PA1 ----> SPI1_SCK
 PA4 ----> SPI1 NSS
 PA11 ----> SPI1_MISO
 PA12 ----> SPI1_MOSI
       */
      GPI0_InitStruct.Pin = LL_GPI0_PIN_4;
```

```
GPIO_InitStruct.Mode = LL_GPIO_MODE_OUTPUT;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
      GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
      GPIO InitStruct.Pull = LL GPIO PULL NO;
      GPIO InitStruct.Alternate = LL GPIO AF 5;
      LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
      GPIO_InitStruct.Pin = LL_GPIO_PIN_1|LL_GPIO_PIN_11|LL_GPIO_PIN_12;
      GPI0_InitStruct.Mode = LL_GPI0_MODE_ALTERNATE;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
      GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
      GPI0_InitStruct.Pull = LL_GPI0_PULL_NO;
      GPI0_InitStruct.Alternate = LL_GPI0_AF_5;
      LL GPIO Init(GPIOA, &GPIO InitStruct);
      /* SPI1 parameter configuration*/
      SPI InitStruct.TransferDirection = LL SPI FULL DUPLEX;
      SPI_InitStruct.Mode = LL_SPI_MODE_MASTER;
      SPI InitStruct.DataWidth = LL SPI DATAWIDTH 16BIT;
      SPI InitStruct.ClockPolarity = LL SPI POLARITY LOW;
      SPI InitStruct.ClockPhase = LL SPI PHASE 1EDGE;
      SPI_InitStruct.NSS = LL_SPI_NSS_SOFT;
      SPI InitStruct.BaudRate = LL SPI BAUDRATEPRESCALER DIV4;
      SPI_InitStruct.BitOrder = LL_SPI_MSB_FIRST;
      SPI_InitStruct.CRCCalculation = LL_SPI_CRCCALCULATION_DISABLE;
      SPI_InitStruct.CRCPoly = 7;
      LL_SPI_Init(SPI1, &SPI_InitStruct);
      LL_SPI_SetStandard(SPI1, LL_SPI_PROTOCOL_MOTOROLA);
      LL_SPI_EnableNSSPulseMgt(SPI1);
      LL_SPI_Enable(SPI1);
/* SPI3 init function */
static void MX SPI3 Init(void)
      LL SPI InitTypeDef SPI InitStruct;
      LL GPI0_InitTypeDef GPI0_InitStruct;
      /* Peripheral clock enable */
      LL_APB1_GRP1_EnableClock(LL_APB1_GRP1_PERIPH_SPI3);
      LL_APB1_GRP1_EnableClock(LL_APB1_GRP1_PERIPH_SPI3);
      /**SPI3 GPIO Configuration
 PA15 (JTDI) ----> SPI3_NSS
 PB3 (JTDO-TRACESWO) ----> SPI3_SCK
 PB4 (NJTRST) ----> SPI3 MISO
 PB5
       ----> SPI3_MOSI
       */
      GPIO InitStruct.Pin = LL GPIO PIN 15;
      GPIO InitStruct.Mode = LL GPIO MODE ALTERNATE;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
```

```
GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
GPI0_InitStruct.Pull = LL_GPI0_PULL_N0;
GPI0_InitStruct.Alternate = LL_GPI0_AF_6;
LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
```

```
GPI0_InitStruct.Pin = LL_GPI0_PIN_4;
GPI0_InitStruct.Mode = LL_GPI0_MODE_INPUT;
GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
GPI0_InitStruct.Pull = LL_GPI0_PULL_N0;
GPI0_InitStruct.Alternate = LL_GPI0_AF_6;
LL_GPI0_Init(GPI0B, &GPI0_InitStruct);
```

```
GPI0_InitStruct.Pin = LL_GPI0_PIN_3|LL_GPI0_PIN_5;
GPI0_InitStruct.Mode = LL_GPI0_MODE_ALTERNATE;
GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_MEDIUM;
GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
GPI0_InitStruct.Pull = LL_GPI0_PULL_NO;
GPI0_InitStruct.Alternate = LL_GPI0_AF_6;
LL_GPI0_Init(GPI0B, &GPI0_InitStruct);
```

```
/* SPI3 parameter configuration*/
SPI_InitStruct.TransferDirection = LL_SPI_FULL_DUPLEX;
SPI_InitStruct.Mode = LL_SPI_MODE_SLAVE;
SPI_InitStruct.DataWidth = LL_SPI_DATAWIDTH_16BIT;
SPI_InitStruct.ClockPolarity = LL_SPI_POLARITY_LOW;
SPI_InitStruct.ClockPhase = LL_SPI_PHASE_1EDGE;
SPI_InitStruct.NSS = LL_SPI_NSS_SOFT;
SPI_InitStruct.BitOrder = LL_SPI_MSB_FIRST;
SPI_InitStruct.CRCCalculation = LL_SPI_CRCCALCULATION_DISABLE;
SPI_InitStruct.CRCPoly = 7;
LL_SPI_Init(SPI3, &SPI_InitStruct);
```

LL\_SPI\_SetStandard(SPI3, LL\_SPI\_PROTOCOL\_MOTOROLA);

LL\_SPI\_DisableNSSPulseMgt(SPI3); SPI3->CR1 &= ~(1 << SPI\_CR1\_SSI\_Pos);</pre>

```
__HAL_RCC_DMA2_CLK_ENABLE();
CLEAR_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
hdma2.Instance = DMA2_Channel1;
hdma2.Init.Request = DMA_REQUEST_3;
hdma2.Init.Direction = DMA_PERIPH_TO_MEMORY;
hdma2.Init.PeriphInc = DMA_PINC_DISABLE;
hdma2.Init.MemInc = DMA_MINC_ENABLE;
hdma2.Init.PeriphDataAlignment = DMA_PDATAALIGN_HALFWORD;
hdma2.Init.MemDataAlignment = DMA_MDATAALIGN_HALFWORD;
hdma2.Init.Mode = DMA_NORMAL;
hdma2.Init.Priority = DMA_PRIORITY_HIGH;
SET_BIT(SPI3->CR2, SPI_CR2_RXDMAEN);
HAL_DMA_Init(&hdma2);
CLEAR_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
```

```
DMA2_Channel1->CMAR = (uint32_t)&Data1;
DMA2_Channel1->CNDTR = (uint32_t)12000;
```

```
DMA2_Channel1->CPAR = (uint32_t)&(SPI3->DR);
      SET_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
      //while(LL DMA IsActiveFlag TC4(DMA2)==0){
      //}
      //LL_DMA_ClearFlag_TC4(DMA2);
      LL_SPI_Enable(SPI3);
      SPI3->CR1 &= ~(1 << SPI_CR1_SSI_Pos);</pre>
/** Configure pins as
 * Analog
 * Input
 * Output
 * EVENT_OUT
 * EXTI
*/
static void MX_GPI0_Init(void)
      LL_GPI0_InitTypeDef GPI0_InitStruct;
      /* GPIO Ports Clock Enable */
      LL_AHB2_GRP1_EnableClock(LL_AHB2_GRP1_PERIPH_GPIOA);
      LL_AHB2_GRP1_EnableClock(LL_AHB2_GRP1_PERIPH_GPIOB);
      /**/
      LL_GPI0_ResetOutputPin(GPI0A, LL_GPI0_PIN_0);
      /**/
      GPIO InitStruct.Pin = LL GPIO PIN 0;
      GPIO InitStruct.Mode = LL GPIO MODE OUTPUT;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_LOW;
      GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
      GPIO InitStruct.Pull = LL GPIO PULL NO;
      LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
      GPI0_InitStruct.Pin = LL_GPI0_PIN_9;
      GPI0_InitStruct.Mode = LL_GPI0_MODE_OUTPUT;
      GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_LOW;
      GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
      GPI0_InitStruct.Pull = LL_GPI0_PULL_NO;
      LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
      LL_GPI0_ResetOutputPin(GPI0B, LL_GPI0_PIN_9);
      LL_GPI0_ResetOutputPin(GPI0B, LL_GPI0_PIN_6);
```

/\*\*/ GPI0\_InitStruct.Pin = LL\_GPI0\_PIN\_6; GPI0\_InitStruct.Mode = LL\_GPI0\_MODE\_OUTPUT; GPIO InitStruct.Speed = LL GPIO SPEED FREQ LOW; GPIO InitStruct.OutputType = LL GPIO OUTPUT PUSHPULL; GPI0\_InitStruct.Pull = LL\_GPI0\_PULL\_NO; LL\_GPI0\_Init(GPI0B, &GPI0\_InitStruct); LL\_GPI0\_ResetOutputPin(GPI0B, LL\_GPI0\_PIN\_6); //LL GPIO SetOutputPin(GPIOB, LL GPIO PIN 6); LL GPIO ResetOutputPin(GPIOB, LL GPIO PIN 7); 11 // /\*\*/ 11 GPI0\_InitStruct.Pin = LL\_GPI0\_PIN\_7; GPIO InitStruct.Mode = LL GPIO MODE INPUT; GPI0\_InitStruct.Speed = LL\_GPI0\_SPEED\_FREQ\_LOW; GPI0\_InitStruct.OutputType = LL\_GPI0\_OUTPUT\_PUSHPULL; GPIO InitStruct.Pull = LL GPIO PULL NO; LL GPIO Init(GPIOB, &GPIO InitStruct); GPIO InitStruct.Pin = LL GPIO PIN 10;

```
GPIO_InitStruct.Mode = LL_GPIO_MODE_INPUT;
GPIO_InitStruct.Speed = LL_GPIO_SPEED_FREQ_LOW;
GPIO_InitStruct.OutputType = LL_GPIO_OUTPUT_PUSHPULL;
GPIO_InitStruct.Pull = LL_GPIO_PULL_DOWN;
LL_GPIO_Init(GPIOA, &GPIO_InitStruct);
```

```
SYSCFG->EXTICR[2] = SYSCFG_EXTICR3_EXTI10_PA;
EXTI->IMR1 |= (1<<10);
EXTI->EMR1 |=(1<<10); //Unmask interrupt line 15
EXTI->RTSR1 |= (1<<10); //falling edge line 15
NVIC_ClearPendingIRQ(EXTI15_10_IRQn);
NVIC_EnableIRQ(EXTI15_10_IRQn);
__NVIC_SetPriority(EXTI15_10_IRQn,0);
```

//LL\_GPI0\_SetOutputPin(GPI0B, LL\_GPI0\_PIN\_7);

```
GPI0_InitStruct.Pin = LL_GPI0_PIN_5;
GPI0_InitStruct.Mode = LL_GPI0_MODE_OUTPUT;
GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_LOW;
GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
GPI0_InitStruct.Pull = LL_GPI0_PULL_N0;
LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
```

```
LL_GPI0_ResetOutputPin(GPI0A, LL_GPI0_PIN_5);
```

```
GPI0_InitStruct.Pin = LL_GPI0_PIN_8;
GPI0_InitStruct.Mode = LL_GPI0_MODE_OUTPUT;
GPI0_InitStruct.Speed = LL_GPI0_SPEED_FREQ_LOW;
GPI0_InitStruct.OutputType = LL_GPI0_OUTPUT_PUSHPULL;
GPI0_InitStruct.Pull = LL_GPI0_PULL_N0;
LL_GPI0_Init(GPI0A, &GPI0_InitStruct);
```

```
LL_GPI0_ResetOutputPin(GPI0A, LL_GPI0_PIN_8);
}
/* USER CODE BEGIN 4 */
//This reads the stimulation protocol from memory. This is achieved throguh DMA,
which reads protocol into DataRx
void Read_Protocol(void)
{
      DMA1_Channel5->CCR &= ~DMA_CCR_EN;
      MODIFY_REG(DMA1_Channel5->CCR, DMA_CCR_DIR, DMA_PERIPH_TO_MEMORY);
      while(((READ_BIT(QUADSPI->SR, QUADSPI_SR_BUSY) == (QUADSPI_SR_BUSY)) ? 1UL :
0UL)==1){
             //SET BIT(GPIOA->BRR, LL GPIO PIN 0);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, QUADSPI_CCR_FMODE_0);
      DMA1 Channel5->CMAR = (uint32 t)&DataRx;
      DMA1 Channel5->CNDTR = (uint32 t)230;
      DMA1 Channel5->CPAR = (uint32 t)&(QUADSPI->DR);
      WRITE_REG(QUADSPI->DLR, 229);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_INSTRUCTION, 0x03);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_ABMODE,
(QUADSPI CCR ABMODE 0 QUADSPI CCR ABMODE 1));
      MODIFY REG(QUADSPI->CCR, QUADSPI CCR ABSIZE, 0x00);
      WRITE_REG(QUADSPI->AR,0);
      DMA1_Channel5->CCR |= DMA_CCR_EN;
      QUADSPI->CR |= QUADSPI_CR_DMAEN;
      while(((READ_BIT(DMA1->ISR, DMA_ISR_TCIF5) == (DMA_ISR_TCIF5)) ? 1UL :
0UL)==0){
             //SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      SET BIT(DMA1->IFCR, DMA IFCR CTCIF5|DMA IFCR CHTIF5);
      //SET BIT(GPIOA->BSRR, LL GPIO PIN 9);
      //hqspi.Lock = HAL UNLOCKED;
      HAL Delay(2);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_ABMODE, 0x00);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_ABSIZE, QUADSPI_CCR_ABSIZE_0);
      DMA1 Channel5->CCR &= ~DMA CCR EN;
      MODIFY_REG(DMA1_Channel5->CCR, DMA_CCR_DIR, DMA_PERIPH_TO_MEMORY);
}
void MX_TIM1_Init(void)
{ //Enable Clocks
      SET_BIT(RCC->APB1ENR1,RCC_APB1ENR1_TIM2EN);
      uint32_t Pre_Tim_2 = 0;
      TIM2 \rightarrow PSC = 0;
      uint32 t Reload Tim 2 = 4000;
      TIM2->ARR = Reload Tim 2;
      TIM2->DIER |= TIM_DIER_UIE;
```

```
NVIC_EnableIRQ(TIM2_IRQn);
      NVIC_SetPriority(TIM2_IRQn,1);
      TIM2->CR1|=(TIM_CR1_CEN);
}
//This handles the configuration of the external memory, setting them into Quad-SPI
mode from single line SPI mode
static void Config_Memory_Banks(void){
      QSPI CommandTypeDef sCommand;
      sCommand.InstructionMode = QSPI_INSTRUCTION_NONE;
      sCommand.Instruction = 0x02; // Write ID
      sCommand.AddressMode = QSPI ADDRESS 4 LINES;
      sCommand.Address = 0xFF;
      sCommand.AddressSize = QSPI ADDRESS 8 BITS;
      sCommand.AlternateByteMode = QSPI_ALTERNATE_BYTES NONE;
      sCommand.DataMode = QSPI_DATA_NONE;
      sCommand.DummyCycles = 0x00 ;
      sCommand.AlternateBytesSize = QSPI ALTERNATE BYTES 8 BITS;
      sCommand.AlternateBytes = 0x00;
      sCommand.DdrMode = QSPI DDR MODE DISABLE;
      sCommand.DdrHoldHalfCycle = QSPI DDR HHC ANALOG DELAY;
      sCommand.SIOOMode = QSPI_SIOO_INST_EVERY_CMD;
      sCommand.NbData = sizeof(Data);
      HAL_QSPI_Command(&hqspi, &sCommand, 1);
      /* Read memory mode from memory address from memory banks
       * Send 0x05 to memory and read the result
       */
      sCommand.InstructionMode = QSPI_INSTRUCTION_NONE;
      sCommand.Instruction = 0x05; // Write ID
      sCommand.AddressMode = QSPI_ADDRESS_1_LINE;
      sCommand.Address = 0x05;
      sCommand.AddressSize = QSPI ADDRESS 8 BITS;
      sCommand.AlternateByteMode = QSPI ALTERNATE BYTES NONE;
      sCommand.DataMode = QSPI DATA 1 LINE;
      sCommand.DummyCycles = 0 ;
      sCommand.AlternateBytesSize = QSPI ALTERNATE BYTES 8 BITS;
      sCommand.AlternateBytes = 0x00;
      sCommand.DdrMode = QSPI_DDR_MODE_DISABLE;
      sCommand.DdrHoldHalfCycle = QSPI_DDR_HHC_ANALOG_DELAY;
      sCommand.SIOOMode = QSPI_SIOO_INST_EVERY_CMD;
      sCommand.NbData = 1;
      HAL_QSPI_Command(&hqspi, &sCommand, 1);
      /* Configure QSPI: CCR register with functional as indirect read */
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, QUADSPI_CCR_FMODE_0);
      /* Start the transfer by re-writing the address in AR register */
      WRITE_REG(QUADSPI->AR, 0x05);
      Test1 = QUADSPI->DR;
      while(((READ BIT(QUADSPI->SR, QUADSPI SR BUSY) == (QUADSPI SR BUSY)) ? 1UL :
0UL)==1){
```

```
//SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
```

```
MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, 0);
      //HAL_QSPI_Receive(&hqspi,Test1,HAL_QPSI_TIMEOUT_DEFAULT_VALUE);
      11
             while(((READ BIT(QUADSPI->SR, QUADSPI SR BUSY) == (QUADSPI SR BUSY)) ?
1UL : 0UL)==1){
      11
                    //SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      //
             }
      //
             MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, 0);
      //
      /*
       *
       */
                                 = QSPI INSTRUCTION 1 LINE;
      sCommand.InstructionMode
      sCommand.Instruction
                                  = (uint8 t) 2;
      sCommand.AddressMode
                                  = QSPI ADDRESS 1 LINE;
      sCommand.AddressSize = QSPI_ADDRESS_24_BITS;
      sCommand.Address= 1;
      sCommand.AlternateByteMode = QSPI ALTERNATE BYTES NONE;
      sCommand.DataMode
                                  = QSPI DATA 1 LINE;
                                 = 0;
      sCommand.DummyCycles
      sCommand.DdrMode
                                  = QSPI DDR MODE DISABLE;
      sCommand.DdrHoldHalfCycle = QSPI_DDR_HHC_ANALOG_DELAY;
      sCommand.SIOOMode
                                  = QSPI_SIOO_INST_EVERY_CMD;
      sCommand.NbData = 1;
      HAL_QSPI_Command(&hqspi, &sCommand, HAL_QPSI_TIMEOUT_DEFAULT_VALUE);
      QUADSPI - >DR = 77;
      while(((READ_BIT(QUADSPI->SR, QUADSPI_SR_BUSY) == (QUADSPI_SR_BUSY)) ? 1UL :
0UL)==1){
             //SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      }
      sCommand.InstructionMode
                                 = QSPI_INSTRUCTION_1_LINE;
      sCommand.Instruction
                                  = (uint8 t) 3;
                                  = QSPI_ADDRESS_1_LINE;
      sCommand.AddressMode
      sCommand.AddressSize = QSPI ADDRESS 24 BITS;
      sCommand.Address= 0;
      sCommand.AlternateByteMode = QSPI ALTERNATE BYTES 1 LINE;
      sCommand.AlternateBytesSize = QSPI ALTERNATE BYTES 8 BITS;
      sCommand.AlternateBytes = 0;
      sCommand.DataMode
                                  = QSPI_DATA_1_LINE;
      sCommand.DummyCycles
                                  = 0;
                                  = QSPI_DDR_MODE_DISABLE;
      sCommand.DdrMode
      sCommand.DdrHoldHalfCycle = QSPI_DDR_HHC_ANALOG_DELAY;
      sCommand.SIOOMode
                                  = QSPI_SIOO_INST_EVERY_CMD;
      sCommand.NbData = 1;
      HAL_QSPI_Command(&hqspi, &sCommand, HAL_QPSI_TIMEOUT_DEFAULT_VALUE);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, QUADSPI_CCR_FMODE_0);
      WRITE_REG(QUADSPI->AR, 0x01);
      Test1 = QUADSPI->DR;
      while(((READ_BIT(QUADSPI->SR, QUADSPI_SR_BUSY) == (QUADSPI_SR_BUSY)) ? 1UL :
0UL)==1){
             //SET BIT(GPIOA->BRR, LL GPIO PIN 0);
      }
```

```
MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, 0);
      /* Set memory to quad mode
       *
       */
      sCommand.InstructionMode = QSPI_INSTRUCTION NONE;
      sCommand.Instruction
                                 = (uint8_t) 56;
                                 = QSPI_ADDRESS_1_LINE;
      sCommand.AddressMode
      sCommand.AddressSize = QSPI_ADDRESS_8_BITS;
      sCommand.Address = 56;
      sCommand.AlternateByteMode = QSPI_ALTERNATE_BYTES_NONE;
      sCommand.DataMode
                                 = QSPI DATA NONE;
      sCommand.DummyCycles
                                 = 0;
                                 = QSPI DDR MODE DISABLE;
      sCommand.DdrMode
      sCommand.DdrHoldHalfCycle = QSPI DDR HHC ANALOG DELAY;
      sCommand.SIOOMode
                                 = QSPI_SIOO_INST_EVERY_CMD;
      HAL_QSPI_Command(&hqspi, &sCommand, HAL_QPSI_TIMEOUT_DEFAULT_VALUE);
      //WRITE REG(QUADSPI->AR, 56);
      while(((READ BIT(QUADSPI->SR, QUADSPI SR BUSY) == (QUADSPI SR BUSY)) ? 1UL :
0UL)==1){
             //SET BIT(GPIOA->BRR, LL GPIO PIN 0);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, 0);
      sCommand.InstructionMode = QSPI_INSTRUCTION_4_LINES;
      sCommand.Instruction = 0x02; // Write ID
      sCommand.AddressMode = QSPI_ADDRESS_4_LINES;
      sCommand.Address = 0x00;
      sCommand.AddressSize = QSPI_ADDRESS_24_BITS;
      sCommand.AlternateByteMode = QSPI_ALTERNATE_BYTES_NONE;
      sCommand.DataMode = QSPI DATA 4 LINES;
      sCommand.DummyCycles = 0x00 ;
      sCommand.AlternateBytesSize = QSPI ALTERNATE BYTES 8 BITS;
      sCommand.AlternateBytes = 0x00;
      sCommand.DdrMode = QSPI DDR MODE DISABLE;
      sCommand.DdrHoldHalfCycle = QSPI DDR HHC ANALOG DELAY;
      sCommand.SIOOMode = QSPI SIOO INST EVERY CMD;
      sCommand.NbData = 1;
      HAL_QSPI_Command(&hqspi, &sCommand, HAL_QPSI_TIMEOUT_DEFAULT_VALUE);
      QUADSPI - > DR = 77;
      while(((READ BIT(QUADSPI->SR, QUADSPI SR BUSY) == (QUADSPI SR BUSY)) ? 1UL :
0UL)==1){
             //SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      }
      sCommand.InstructionMode = QSPI INSTRUCTION 4 LINES;
      sCommand.Instruction = 0x03; // Write ID
      sCommand.AddressMode = QSPI_ADDRESS_4_LINES;
      sCommand.Address = 0x00;
      sCommand.AddressSize = QSPI ADDRESS 24 BITS;
      sCommand.AlternateByteMode = QSPI ALTERNATE BYTES 4 LINES;
      sCommand.DataMode = QSPI_DATA_4_LINES;
```

```
sCommand.DummyCycles = 0x00 ;
      sCommand.AlternateBytesSize = QSPI_ALTERNATE_BYTES_8_BITS;
      sCommand.AlternateBytes = 0x00;
      sCommand.DdrMode = QSPI DDR MODE DISABLE;
      sCommand.DdrHoldHalfCycle = QSPI DDR HHC ANALOG DELAY;
      sCommand.SIOOMode = QSPI_SIOO_INST_EVERY_CMD;
      sCommand.NbData = 1;
      HAL_QSPI_Command(&hqspi, &sCommand, HAL_QPSI_TIMEOUT_DEFAULT_VALUE);
      MODIFY REG(QUADSPI->CCR, QUADSPI CCR FMODE, QUADSPI CCR FMODE 0);
      WRITE REG(QUADSPI->AR, 0x01);
      Test1 = QUADSPI->DR;
      /* Read Id register ----- */
      sCommand.InstructionMode = QSPI_INSTRUCTION_4_LINES;
      sCommand.Instruction = 0x02; // Write ID
      sCommand.AddressMode = QSPI_ADDRESS_4_LINES;
      sCommand.Address = 0 \times 00;
      sCommand.AddressSize = QSPI ADDRESS 24 BITS;
      sCommand.AlternateByteMode = QSPI ALTERNATE BYTES 4 LINES;
      sCommand.DataMode = QSPI_DATA_4_LINES;
      sCommand.DummyCycles = 0x00 ;
      sCommand.AlternateBytesSize = QSPI_ALTERNATE_BYTES_8_BITS;
      sCommand.AlternateBytes = 0x00;
      sCommand.DdrMode = QSPI_DDR_MODE_DISABLE;
      sCommand.DdrHoldHalfCycle = QSPI_DDR_HHC_ANALOG_DELAY;
      sCommand.SIOOMode = QSPI_SIOO_INST_EVERY_CMD;
      sCommand.NbData = sizeof(Data);
      HAL_QSPI_Command(&hqspi, &sCommand, 1);
//This sets out the initialisation code to the intan IC as suggested in the IC's data
sheet
static void Initialise_Intan(void)
      for(qq=0;qq<62;qq++){
             LL GPIO ResetOutputPin(GPIOA,LL GPIO PIN 4);
             SPI1->DR = (Commands[qq]);
             while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
             };
             test1 = (uint16_t)(READ_REG(SPI1->DR));
             SPI1->DR = (Registers [qq]);
             while ((LL_SPI_IsActiveFlag_BSY(SPI1)== 1)){
             };
             LL_GPI0_SetOutputPin(GPI0A,LL_GPI0_PIN_4);
             test2 = (uint16_t)(READ_REG(SPI1->DR));
      }
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      //The Following lines set up the current step size, set to 10uA. This should
be changed to allow for user selectable sizes.
```

```
SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
```

```
SPI1->DR = ( uint16_t) (160<<8) |(uint16_t)34;</pre>
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      SPI1 \rightarrow DR = (uint16 t)(15);
      while ((LL_SPI_IsActiveFlag_BSY(SPI1)== 1)){
      };
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      SPI1->DR = ( uint16_t) (160<<8) |(uint16_t)35;</pre>
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      SPI1 \rightarrow DR = (uint16 t)(255);
      while ((LL_SPI_IsActiveFlag_BSY(SPI1)== 1)){
      };
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      SET BIT(GPIOA->BRR, LL GPIO PIN 4);
      SPI1 - DR = (uint16 t) (160 < 8) | (uint16 t)44;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      SPI1->DR = ( uint16 t) 255;;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1)== 1)){
      };
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
}
//This reads the users program choice from the external ram
static void Select_Program(void){
      //disable DMA1
      // set direction periph to memory
      //wait till quad spi not busy
      // change to read
      //set data rx
      //dma 2 bytes
      //data length = 1 (2-1)
      //instructuion
      DMA1 Channel5->CCR &= ~DMA CCR EN;
      MODIFY_REG(DMA1_Channel5->CCR, DMA_CCR_DIR, DMA_PERIPH_TO_MEMORY);
      while(((READ_BIT(QUADSPI->SR, QUADSPI_SR_BUSY) == (QUADSPI_SR_BUSY)) ? 1UL :
0UL)==1){
             //SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      }
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, QUADSPI_CCR_FMODE_0);
      DMA1_Channel5->CMAR = (uint32_t)&DataRx;
      DMA1_Channel5->CNDTR = (uint32_t)2;
      DMA1_Channel5->CPAR = (uint32_t)&(QUADSPI->DR);
      WRITE_REG(QUADSPI->DLR, 1);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_INSTRUCTION, 0x03);
      MODIFY REG(QUADSPI->CCR, QUADSPI CCR ABMODE,
(QUADSPI CCR ABMODE 0 QUADSPI CCR ABMODE 1));
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_ABSIZE, 0x00);
```

```
WRITE_REG(QUADSPI->AR,0);
      DMA1_Channel5->CCR |= DMA_CCR_EN;
      QUADSPI->CR |= QUADSPI_CR_DMAEN;
      while(((READ BIT(DMA1->ISR, DMA ISR TCIF5) == (DMA ISR TCIF5)) ? 1UL :
0UL)==0){
             //SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      }
      SET_BIT(DMA1->IFCR, DMA_IFCR_CTCIF5|DMA_IFCR_CHTIF5);
      //SET BIT(GPIOA->BSRR, LL GPIO PIN 9);
      HAL_Delay(2);
      Program_Choice = DataRx[0];
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_ABMODE, 0x00);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_ABSIZE, QUADSPI_CCR_ABSIZE_0);
      DMA1 Channel5->CCR &= ~DMA CCR EN;
      MODIFY_REG(DMA1_Channel5->CCR, DMA_CCR_DIR, DMA_PERIPH_TO_MEMORY);
      State = Program_Select;
}
//This performs ADC requests on each channel.
//The Stimulation parameters are checked for each channel
//The channel is turned on/off depending on how it is working
//The channels polarity is switched depending on how it is configured
static void Intan_com(void)
{
      uint16_t Temp_1 = 49407;
      uint16_t Temp_2 = 0;
      uint16_t Temp_3 = 57599;
      uint16_t Stim_On_Address = 32810;
      uint16_t Stim_Pol_Address = 32812;
      uint16_t Stim_On_Off_Temp = 0;
      uint16 t Stim Pol Temp = 0;
      uint16 t Results1;
      uint16 t Results2;
      uint16_t Temp_4 = 32780;
      uint16_t Temp_5 = 57599;
      uint8_t ii;
      Stim_On_Off_Temp = Stim_On_Off;
      Stim_Pol_Temp = Stim_Pol;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      //Toggle pin high
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      //Toggle pin low;
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      SPI1 \rightarrow DR = (uint16 t) 2048;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
```

```
};
SPI1->DR = (uint16_t) 0;
for (ii = 0; ii<15;ii++){</pre>
       if ((READ_BIT(Stim_Bit, ((uint16_t)(1<<ii))) == (((uint16_t)(1<<ii))))</pre>
              if(Stim_Counter[ii]==Stim_Pos_Limit[ii]){
                     //set negative
                     Stim Pol Temp &= ~(uint16 t)(1<<ii);</pre>
              if(Stim_Counter[ii]==Stim_Neg_Limit[ii]){
                     //increase pulse count and turn off
                     Stim_On_Off_Temp &= ~((uint16_t)(1<<ii));</pre>
                     Pulse_Count[ii] = Pulse_Count[ii]+1;
              Stim_Counter[ii]=Stim_Counter[ii]+1;
       }else{
              Refractory Count[ii] = Refractory Count[ii] +1;
       }
       while ((LL SPI IsActiveFlag BSY(SPI1) == 1)){
       };
       //Toggle pin high
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
       //Toggle pin low;
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      SPI1->DR = (uint16_t)2111;
       if(Stim_Counter[ii]==Stim_Off_Limit[ii]){
              Stim_Counter[ii] = 0;
              Stim Pol Temp |= (uint16 t)(1<<ii);</pre>
              Stim On Off Temp |= (uint16 t)(1<<ii);</pre>
       if ((READ_BIT(Refractory_Bit,(uint16_t)1<<ii))==((uint16_t)1<<ii)){</pre>
              if(Pulse_Count[ii]==Pulse_Number[ii]){
                     Pulse_Count[ii] = 0;
                     Stim_Bit &= ~(uint16_t)(1<<ii);</pre>
              if (Refractory_Count[ii] == Refractory_Num[ii]){
                     Stim_Bit |=(uint16_t)(1<<ii);</pre>
                     Refractory_Count[ii] = 0;
                     Stim_Pol_Temp |= (uint16_t)(1<<ii);</pre>
                     Stim_On_Off_Temp |= (uint16_t)(1<<ii);</pre>
                     Stim_Counter[ii] = 0;
       }else{
              Stim_Bit |=(uint16_t)(1<<ii);</pre>
       }
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
       };
```

){

```
SPI1 \rightarrow DR = (uint16_t) 0;
}
if (((Stim_Bit) & ((uint16_t)1<<15))==((uint16_t)1<<15)){</pre>
       if(Stim_Counter[15]==Stim_Pos_Limit[15]){
              //set negative
              Stim_Pol_Temp &=~ (uint16_t)1<<15;</pre>
       }else if(Stim_Counter[15]==Stim_Neg_Limit[15]){
              //increase pulse count and turn off
              Stim_On_Off_Temp &=~ ((uint16_t)(1<<ii));</pre>
             Pulse_Count[15] = Pulse_Count[15]+1;
       Stim_Counter[15]=Stim_Counter[15]+1;
}else{
       Refractory_Count[15] = Refractory_Count[15] +1;
if(Pulse_Count[15]==Pulse_Number[15]){
      Pulse Count[15] = 0;
       Stim Bit &=~ (uint16 t)(1<<15);</pre>
}
while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
};
//Toggle pin high
SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
//Toggle pin low;
SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
SPI1->DR = (uint16_t)Temp_1;
if (((Refractory_Bit) & ((uint16_t)(1<<15)))==((uint16_t)(1<<15))){</pre>
       if(Stim_Counter[15]==Stim_Off_Limit[15]){
              Stim Counter [15] = 0;
              Stim Pol Temp |= (uint16 t)(1<<15);</pre>
              Stim_On_Off_Temp |= (uint16_t)(1<<15);</pre>
       }
       if (Refractory_Count[15] = Refractory_Num[15]){
              Stim Bit |=(uint16 t)(1<<15);</pre>
              Refractory_Count[ii] = 0;
              Stim_Pol_Temp |= (uint16_t)(1<<15);</pre>
              Stim_On_Off_Temp |= (uint16_t)(1<<15);</pre>
              Stim_Counter[15] = 0;
       }
}
while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
};
SPI1->DR =(uint16_t) 0;
while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
};
//Toggle pin high
SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
```

```
//Toggle pin low;
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      SPI1->DR = Stim_Pol_Address;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
      };
      SPI1->DR = (uint16_t)Stim_Pol_Temp;
      Stim_Pol = Stim_Pol_Temp;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      //Toggle pin high
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      //Toggle pin low;
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      SPI1->DR = Stim On Address;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
      };
      SPI1->DR =(uint16_t)(Stim_On_Off_Temp & Stim_Mask);
      Stim On Off = Stim On Off Temp ;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      //Toggle pin high
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      //Toggle pin low;
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      SPI1->DR = Temp_5;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
      };
      SPI1->DR = 0;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      SET BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      Counter++;
//This ramps up all the currents on each channel, performing an IV sweep
static void Test_IV(void){
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      Temp_1 = (uint16_t) ((1<<15)+(44));</pre>
      SPI1->DR = Temp_1;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
      };
      Temp_1 = (uint16_t)255;
      SPI1->DR = Temp_1;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      Temp_1 = (uint16_t)57599;
      SPI1->DR = Temp 1;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
      };
```

```
Temp_1 = (uint16_t)0;
SPI1 \rightarrow DR = 0;
while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
};
SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
HAL_Delay(1);
for(IV_Loop_i = 0;IV_Loop_i<16;IV_Loop_i++)</pre>
{
       CLEAR_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
      DMA2_Channel1->CMAR = (uint32_t)&Data1;
      DMA2_Channel1->CNDTR = (uint32_t)2048;
      DMA2 Channel1->CPAR = (uint32 t)&(SPI3->DR);
       SET_BIT(DMA2_Channel1->CCR, DMA_CCR_EN)
       for(IV_Loop_j = 0;IV_Loop_j<255;IV_Loop_j++){</pre>
             //turn on LED
              //Toggle pin high
              SET BIT(GPIOA->BRR, LL GPIO PIN 4);
              Temp_1 = (uint16_t) ((32810));
              SPI1->DR = Temp 1;
              while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
              };
              Temp_1 = 0;
              Temp_1 |= (uint16_t)(1<<IV_Loop_i);</pre>
              SPI1->DR = Temp_1;
             while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
              };
              SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
              //update current
              //Toggle pin low;
              SET BIT(GPIOA->BRR, LL GPIO PIN 4);
              Temp 1 = (uint16 t) ((32768)+(96+(IV Loop i)));
              SPI1->DR = Temp 1;
              while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
             };
              Temp_1 = (uint16_t)((uint16_t)(128<<8)|(uint16_t)(IV_Loop_j));</pre>
              SPI1->DR = Temp 1;
             while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
              };
              SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
              //Toggle pin high
              //update reg
              //Toggle pin low;
              SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
              Temp_1 = (uint16_t)57599;
              SPI1->DR = Temp_1;
              while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
              };
              Temp_1 = (uint16_t)((uint16_t)(128<<8)|(uint16_t)(IV_Loop_j));</pre>
              SPI1 \rightarrow DR = 0;
              while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
```

```
};
              SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
             HAL_Delay(1);
              //read adc
              SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
              Temp_1 = (uint16_t) (2048+(IV_Loop_i));
              SPI1->DR = Temp_1;
             while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
              };
              SPI1 \rightarrow DR = 0;
             while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
              };
              SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
       }
      HAL_Delay(3);
      CLEAR_BIT(DMA2->ISR, DMA_ISR_TCIF1);
      CLEAR_BIT(DMA2_Channel1->CCR, DMA_CCR_EN);
      CLEAR BIT(DMA1 Channel5->CCR, DMA CCR EN);
      SET BIT(GPIOA->BRR, BANK SELECT1);
      SET_BIT(GPIOA->BSRR, BANK_SELECT2);
      WRITE_REG(QUADSPI->FCR, (QSPI_FLAG_TE | QSPI_FLAG_TC));
       //Turn off DMA
      DMA1_Channel5->CCR &= ~DMA_CCR_EN;
      DMA1_Channel5->CMAR = (uint32_t)&Data1;
      DMA1_Channel5->CNDTR = (uint32_t)4096;
      DMA1_Channel5->CPAR = (uint32_t)&(QUADSPI->DR);
      WRITE_REG(QUADSPI->DLR, (( 4096)-1));
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_FMODE, 0x000000000);
      MODIFY_REG(QUADSPI->CCR, QUADSPI_CCR_INSTRUCTION, 0x02);
      WRITE_REG(QUADSPI->AR, (uint32_t)IV_Loop_i*4096);
DMA1_Channel5->CCR |= DMA_CCR_EN;
      QUADSPI->CR |= QUADSPI CR DMAEN;
}
HAL Delay(1000);
SET_BIT(DMA1->IFCR, DMA_IFCR_CTCIF5|DMA_IFCR_CHTIF5);
SET_BIT(GPIOA->BSRR, BANK_SELECT1);
SET_BIT(GPIOA->BRR, BANK_SELECT2);
SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_9);
HAL_Delay(3000);
HAL_Delay(1);
SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
Temp_1 = (uint16_t) (1<<15)+(42);</pre>
SPI1->DR = Temp_1;
while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
};
Temp_1 = (uint16_t)(0);
SPI1->DR = Temp_1;
while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
};
SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
```

```
SET_BIT(GPIOA->BRR, LL_GPIO_PIN_4);
      Temp_1 = (uint16_t)57599;
      SPI1->DR = Temp_1;
      while ((LL_SPI_IsActiveFlag_TXE(SPI1) == 0)){
      };
      SPI1 \rightarrow DR = 0;
      while ((LL_SPI_IsActiveFlag_BSY(SPI1) == 1)){
      };
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
}
//This sets the variables to their initial value prior to
static void Initialise_All(void)
{
      Counter = 0;
      Counter2 = 0;
      IV_Loop_i = 0;
      IV\_Loop\_j = 0;
      Temp 1 = 0;
      MX GPIO Init();
      MX_QUADSPI_Init();
      MX_SPI1_Init();
      MX_SPI3_Init();
      SET_BIT(GPIOB->BRR, LL_GPIO_PIN_6);
      uint16_t reinit;
      for (reinit=0;reinit<12000;reinit++){</pre>
             Data1[reinit] = 0;
             Data2[reinit] = 0;
      for (reinit=0;reinit<400;reinit++){</pre>
             Data[reinit] = 0;
       for (reinit=0;reinit<200;reinit++){</pre>
             DataRx[reinit] = 0;
      }
      HAL_Delay(10);
       SET_BIT(GPIOA->BRR, BANK_SELECT1);
      SET_BIT(GPIOA->BSRR, BANK_SELECT2);
      HAL_Delay(10);
      Config_Memory_Banks();
      //memset(reg, 0, sizeof(reg));
      uint32_t tmp;
      SET_BIT(GPIOA->BSRR, BANK_SELECT1);
      SET_BIT(GPIOA->BRR, BANK_SELECT2);
      HAL_Delay(10);
      Config_Memory_Banks();
      HAL_Delay(5000);
      //commented to allow XXX
      while (((GPIOB->IDR & LL_GPIO_PIN_7) == 0)){
```

```
}
      HAL_Delay(20);
      SET_BIT(GPIOA->BRR, BANK_SELECT1);
      SET_BIT(GPIOA->BSRR, BANK_SELECT2);
      Select_Program();
      SET_BIT(GPIOA->BRR, BANK_SELECT1);
      SET_BIT(GPIOA->BSRR, BANK_SELECT2);
              while(((READ BIT(GPIOB->IDR, LL GPIO PIN 7) == (LL GPIO PIN 7)) ? OUL :
      11
1UL)==0){
      //
      11
                          }
      SET_BIT(GPIOA->BRR, LL_GPIO_PIN_0);
      SET_BIT(GPIOA->BSRR, LL_GPIO_PIN_4);
      SET_BIT(DMA1->IFCR, DMA_IFCR_CTCIF5|DMA_IFCR_CHTIF5);
      DMA1_Channel5->CCR &= ~DMA_CCR_EN;
      tmp = DMA1_Channel5->CCR;
      tmp &= (uint32 t)~(DMA CCR DIR);
      tmp |= DMA MEMORY TO PERIPH;
      DMA1 Channel5->CCR = tmp;
      SET_BIT(GPIOB->BSRR, LL_GPIO_PIN_6);
      HAL_Delay(1);
      Initialise_Intan();
      Reset_Flag = 0;
}
/* USER CODE END 4 */
/**
* @brief This function is executed in case of error occurrence.
* @param file: The file name as string.
 * @param line: The line in file as a number.
 * @retval None
 */
void _Error_Handler(char *file, int line)
{
      /* USER CODE BEGIN Error Handler Debug */
      /* User can add his own implementation to report the HAL error return state */
      while(1)
      {
      }
      /* USER CODE END Error Handler Debug */
}
#ifdef USE_FULL_ASSERT
/**
* @brief Reports the name of the source file and the source line number
*
          where the assert_param error has occurred.
* @param file: pointer to the source file name
 * @param line: assert_param error line source number
 * @retval None
*/
void assert_failed(uint8_t* file, uint32_t line)
{
```

#### Stimulation/Record system User Software

**Step 1:** Attach the Stim/Record system to the Intan headstage using the micro-HDMI cable. Plug in Stim/Record system to a USB 3 port (blue USB port).



Step 2: Open the recording Labview program.

Menu 1. Users start menu.

**Step 3a:** Select Record, this brings up the menu 2. The user can change the stimulation protocol of the LEDs/electrodes. Clicking on a stimulation site will bring up a pop-up (Popup 1).



Menu 2. Protocol Creation.

**Step 3b:** The protocol for each electrode can be altered in the popup window, press update protocol once complete.



Popup 1. Individual channel protocol creation.

Step 3c: Once the protocol is complete press "Create Protocol".

**Step 4:** In the display acquisition window, recording can be started and stopped by pressing the "Start Recording" and "Stop Recording" buttons. Stopping recording will bring the system back to its initial values, it may be wise for future changes to individually allow independent displaying/recording capabilities.



Data Acquisition display.

### Matlab Data Import Code

```
8888
%This code can be used to import acquired data from the Stim/Record system
%It opens a dat file, and converts the values into uV for AC amplifier vals
and mV for DC amplifier vals
8888
clc
clear
%Amount of time of recording
Time = 10;
%% Number of samples within given time
num = 20*20000*Time;
%File ID
FID = fopen('Test SPI Master1.dat','r');
f=fread(FID, [4, num]);
fclose(FID);
%%Calculate AC and DC values
AC Channels=0.195*((f(1,:)+256*f(2,:))-32768);
DC Channels=-19.23*((f(3,:)+256*mod(f(4,:),16))-512);
%%Separate AC conversions into different channels
Channel1=AC Channels(4:20:end);
Channel2=AC Channels (5:20:end);
Channel3=AC_Channels(6:20:end);
Channel4=AC_Channels(7:20:end);
Channel5=AC_Channels(8:20:end);
Channel6=AC_Channels(9:20:end);
Channel7=AC_Channels(10:20:end);
Channel8=AC_Channels(11:20:end);
Channel9=AC_Channels(12:20:end);
Channel10=AC_Channels(13:20:end);
Channel11=AC_Channels(14:20:end);
Channel12=AC_Channels(15:20:end);
Channel13=AC_Channels(16:20:end);
Channel14=AC_Channels(17:20:end);
Channel15=AC_Channels(18:20:end);
Channel16=AC Channels(19:20:end);
%%Separate DC conversions into different channels
Channel1_DC=DC_Channels(4:20:end);
Channel2_DC=DC_Channels(5:20:end);
Channel3_DC=DC_Channels(6:20:end);
Channel4_DC=DC_Channels(7:20:end);
Channel5_DC=DC_Channels(8:20:end);
Channel6_DC=DC_Channels(9:20:end);
Channel7_DC=DC_Channels(10:20:end);
Channel8_DC=DC_Channels(11:20:end);
Channel9_DC=DC_Channels(12:20:end);
Channel10 DC=DC Channels(13:20:end);
Channel11 DC=DC Channels (14:20:end);
Channel12 DC=DC Channels (15:20:end);
Channel13 DC=DC Channels (16:20:end);
Channel14 DC=DC Channels (17:20:end);
Channel15 DC=DC Channels (18:20:end);
Channel16 DC=DC Channels (19:20:end);
```

### Appendix D

## **Power Correction factor**

The light emitted from the LED follows a Lambertian emission profile; therefore, the intensity decreases as a function of distance (and viewing angle albeit the following assumes a centred, top down view). Therefore, the proportion of the light captured by the power meter is dependent on its separation from the emitter. To account for this a correction factor was applied to the power meter readings; this correction uses simple geometry to calculate the power meter's solid angle and therefore to estimate the percentage of light captured.

As a lambertian emmitter the intensity of the LED ( $I_e$ )-(i.e. the radiant flux emitted( $\Phi_E$ ) by a surface per unit area ( $A_{LED}$ ), is proportional to the radiance of the emitter (L) accordingly:

$$M_{\rm e} = \pi L = \Phi_{\rm E} / A_{\rm LED} \tag{D.1}$$

Where L is the radiant flux  $(\Phi_R)$  - (power recieved at the power meter) recieved by a surface per unit solid angle  $(\Omega)$  per unit projected area (A - Area of LED).

$$L = \Phi_{\rm R} / (\Omega A_{\rm LED}) \tag{D.2}$$

Bringing eq D.2 into eq D.1 we get

$$\pi \Phi_{\rm R} / (\Omega A_{\rm LED}) = \Phi_{\rm E} / A_{\rm LED} \tag{D.3}$$

leading to

$$\Phi_{\rm R}/\Phi_{\rm E} = \Omega/\pi \tag{D.4}$$

The ratio of collected power by the power meter is shown below (as a percentage value), (solid angle is calculated with simple geometry using the distance of the detector to probe, and also the detector diameter).



Appendix E

# Comparison of wireless optogenetic stimulation systems

Reference	Light source	# of optical	Colour	# of recording	Weight(g)	Power source	Amplitude Control	Control	Notes
		sites		sites		Source			
[1]	μILED	2	Blue	0	0.11	RF harvesting	Fixed	On/off	Electrical stimulation,
									RF Communication,
									Protocol selection
[2]	LED	1	Blue	0	0.016	RF harvesting	Fixed	On/Off	
[3]	$\mu$ ILED	4*	Blue	1	0.7	RF harvesting	Fixed	On/Off	Temp sensing, $\mu$ IPD
[4]	Optical fiber	2	Blue	2	7	Battery	Fixed	On/Off	RF Communication
	(LED source)	¥							
[5]	μILED	4*	Blue	0	0.07	RF/PV	Fixed	On/Off	
[6]	Optical fiber	$16^{*}$	Blue/yellow	4	1.13	Battery	?	?	
[]			**		(w/o batt)	- 1	0 /0 7	<u> </u>	
	µLED	1	Variable	0	0.03	Inductive	On/Off	On/Off	
[8]	LED	3	Blue	0	2.4	battery	On/Off	On/Off	
[9]	µLED	1	Blue	0	0.02	RF	?	?	
	LED	2	Blue	0	2.9	Battery	User selectable	On/Off	
	LED	8	Blue	0	2	RF	fixed amplitude	On/Off	
[12]	(LD source)	1	Blue	0	6.8	Battery	User selectable"	On/Off	BLE communication
[13]	Optical fiber	1	Blue	0	$\approx 1.6$	Battery	User selectable	On/Off	MCU controllable
	(LED source)								protocols with RF trigger.
[14]	$\mu$ ILED	2	green	0	?	Inductive	On/Off	On/Off pulse	Close loop operation
									based on strain gauge.
[15]	$\mu \text{LED}$	1	Blue	0	0.3	Inductive	fixed amplitude	On/Off	RF communication,
			D / C / D					0 /0 <b>m</b>	microfluidic drug delivery
[16]	Optical fiber	1	R/G/B	0	2.8	Battery	User selectable	On/Off	IR Communication,
	(LED source)	201	DI		0	T 1		0.40 m	Open source.
[17]	Waveguide	32†	Blue	32  11	:	Inductive	User selectable	On/Off	
[10]	$(\mu \text{LED source})$	0	Dlass	C A	41.97	Dattant	2	2	Designed for one in prime to studies
[10]		2	Diue Diue/Orango	04	41.57	Battery	fired amplitude	$\frac{1}{\frac{1}{2}}$	Designed for use in primate studies
[19]		2	Diue/Orange	0	2	Dattery	inxed amplitude		solative control of multiple devices
									microfluidic drug delivery
[20]	<i>u</i> ILED	4	Blue	0	1.8	Battery	fixed amplitude	On/Off	IB communication
[20]	μΠΠΕΡ	1	Diac	0	1.0	Dattery			Microfluidic drug delivery
[21]	<i>µ</i> ILED	1	Blue	0	0.02	Inductive	On/Off	On/Off	
[22]	LED	1	Blue	0	2	Battery	Programmable	Programmable	Electrochemical detection
						· ·	output	output	
[23]	$\mu$ LED	4	Blue	8	4.1	Battery			Close loop
[24]	$\mu$ LED	10	Blue	0	6.5	Battery			On board sound processing
							output	output	stimulation.

\*Note these optical sites are not individually controllable. \*\*Paper demonstrates multiple coulour across different devices. \*\*\*Multiplexed †Multiplexed from 4 sources. ††Wired recording.

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Appendix F

# **Communication protocols**

#### F.1 Communication formats

Multiple electrical communication formats are used within this thesis, the following sections hope to provide a small introduction for those who may need it. All formats described here are synchronous communication formats, that is the input/output data is synchronised to a clock (i.e. the logical HIGH/LOW value of the data line at the rising/falling edge of the clock determines the binary value). These formats use a Master-Slave architecture, where one device (the master) handles the initiation of data transfer requests/timing to the slave device. For an in-depth description, please look the following guides- For SPI (1), For I<sup>2</sup>C (2).

### F.2 Serial Peripheral Interface

Serial Peripheral Interface (SPI) transmits data between a master and a slave using the following signal lines.

- **CS**: Chip select the master uses this signal to indicate which slave the device is communicate with. Usually this is an active low signal i.e. the line is pulled low to select a specific chip.
- SCLK: Clock line, this is the clock signal through which data is synchronised to. Data can be sampled on the rising or falling edge (This protocol is denoted as CPHA -0 and CPHA - 1 respectively). The clock line can idle at either low or high logic levels (Denoted as CPOL - 0 and CPOL - 1 respectively).
- **MOSI Master Out Slave In**: The MOSI line is used for data transferal from the master to the slave. This is generated at the same time as the SCLK signal, so is generally unlikely to exhibit de-synchronisation.
- MISO Master In Slave Out: The MOSI line is used for data transferal from the slave to the master. This is generated only after the slave device has received the clock signal, so this may exhibit de-synchronisation.

When communicating using SPI, the master device will indicate on the CS line that a certain peripheral is to be communicated with. The clock line will then toggle between HIGH and LOW states, and the master device will shift data out on the MOSI line lines (toggling the data line to send the binary message according to the clock state). The peripheral device will receive this clocked signal, decoding the binary message as it arrives, simultaneously the response will be shifted out on the MISO line by the peripheral. Generally communication between both devices is simultaneous, responses will generally be delayed (i.e. the master may request a response but this will only be returned a few requests later, as is the case with the Intan IC where when given an ADC request the Intan AC will only provide this on the 3rd message). SPI communication generally occurs at high clock rates (in the MHz) range, and so this is ideal for mass data transfer.

Single master, multi-peripheral architectures can be created where all peripherals share common SCLK/MOSI/MISO lines but with an individual CS line to each peripheral. When the master wishes to communicate with an individual peripheral, that peripheral's CS line is brought low (while others remain high) therefore allowing the direct communication between one master/peripheral pairing at once. This has the unfortunate downside of requiring n+3 signal lines (where n is the number of peripherals), and so for large peripheral counts this is un-ideal for low pin microcontrollers.

#### F.3 Inter-Integrated Circuit

Inter-Integrated Circuit  $(I^2C)$  is a protocol well suited for communication between a master device and multiple slave peripherals, which transmits data using 2 signal lines:

- **SCL**: Clock line, this is the clock signal through which data is synchronised to, it is initiated by the master device.
- SDA: Data line, both master and slave transmit data across this line.

Within the I<sup>2</sup>C, each peripheral has its own address to which it responds to. Data transferal begins with a start condition (the SDA line is brought low by the master while the SCL is high). The intended chip will then be indicated, by the writing of the I<sup>2</sup>C address to the data line, followed by a Read/Write bit value. If the peripheral is ready to communicate, it will respond by an acknowledgement response (ACK bit). After this data will be transmitted across the data line, ending in a stop condition (the SDA line is brought high by the master while the SCL is high). Writing/Reading from peripheral registers involves initially sending the address of the peripheral's memory to be accessed, followed by the data being written/read.

## Bibliography

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