MOSFET-based MMC for Low-voltage DC Distribution Networks

Yanni Zhong

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Power Electronics, Drives and Energy Conversion (PEDEC) Group
Institute of Energy and Environment
Department of Electronic and Electrical Engineering
University of Strathclyde
Glasgow, UK

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Signed: Date:

Dedicated to my family

Abstract

The increased load demand and the development of distributed generation technologies present challenges to the existing low-voltage power distribution networks. In particular, numbers of high-capacity power electronic interfaces, such as electric vehicle (EV) chargers and embedded photovoltaic (PV) generation, have increased significantly. In comparison with conventional AC systems, low-voltage DC (LVDC) systems offer several potential benefits, including improved utilisation of cable voltage ratings, and elimination of reactive current and skin effect issues. LVDC distribution also complements the growth of power electronic loads having an implicit DC stage as part of their grid interface. However the DC-AC conversion stage at the customer end is one of the main challenges for LVDC distribution due to the widespread existence of AC loads.

To overcome this limit, a high-performance modular multilevel converter (MMC) with parallel-connected MOSFETs is proposed in this thesis. It allows the converter to operate at relatively high voltage with low harmonic content, without the use of large AC filters. MMC also has low switching frequency, and facilitates the use of MOSFETs with the feature of synchronous rectification which provide lower conduction loss and allows parallel-connection to further reduce the losses.

Power losses are calculated to show that the efficiency of MMC can exceed that of a conventional 2-level converter. Comparative analysis was carried out for a conventional 2-level converter, a SiC MOSFET 2-level converter, a Si MOSFET MMC and a GaN HEMT MMC, in terms of power loss, power quality, converter cost, and heat sink size. The analysis suggests that the 5-level MMC with parallel-connected Si MOSFETs may be an efficient alternative for this LVDC application. The optimal number of parallel-connected MOSFETs was then investigated. In addition, thermal measurement was developed to verify the loss calculation. A detailed converter design was conducted with current control methods to eliminate circulating current distortion for single-phase MOSFET MMC. Then a single-phase 5-level MMC prototype was built to validate the control methods proposed.

Acknowledgement

I would like to express my sincere gratitude to my supervisors Prof Stephen Finney and Dr Derrick Holliday. Prof Finney has always been able to explain the technical issues clearly, support me with new ideas and encourage me throughout my PhD study. Dr Holliday has always been patient in reviewing my papers, giving me confidence and providing valuable advices.

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List of Abbreviations & Symbols

The following are the abbreviations and symbols used throughout this thesis.

Abbreviations

CDSM	Clamped Doubled Submodule
DG	Distributed Generations
DSP	Digital Signal Processor
EV	Electric Vehicle
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FBSM	Full-bridge Submodule
FFT	Fast Fourier Transform
GaN	Gallium Nitride
HBSM	Half-bridge Submodule
HEMT	High Electron Mobility Transistors
HVDC	High-voltage DC
IGBT	Insulated Gate Bipolar Transistor
LVDC	Low-voltage DC
MMC	Modular Multilevel Converter
MOSFET	Metal–oxide–semiconductor Field Effect Transistor
NLC	Nearest Level Control
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PF	Power Factor
PI	Proportional Integral
PR	Proportional Resonant
PWM	Pulse Width Modulation
PV	Photovoltaic

RMS	Root Mean Square
SiC	Silicon Carbide
SPWM	Sinusoidal Pulse Width Modulation
SR	Synchronous Rectification
THD	Total Harmonic Distortion
VSI	Voltage Source Inverters

Symbols

i_{al}	Lower arm current in the MMC
E_{on}	Energy loss during turn-on transient
E_{off}	Energy loss during turn-off transient
i_{al}	Lower arm current in the MMC
i_{au}	Upper arm current in the MMC
i_{diff}	Circulating current in the MMC
I_{DS}	Drain-to-source current of MOSFET
L_{arm}	Arm inductance of MMC
M	Modulation index
$\boldsymbol{n}$	Number of submodules in one arm
Q_{rr}	Reverse recovery charge of MOSFET
R_G	Gate resistance of power switches
R_{on}	On-state resistance of power switches
R_Θ	Thermal resistance
T_J	Operating junction temperature of power switches
V_{al}	Lower arm voltage of series connected submodules in the MMC
V_{au}	Upper arm voltages of series connected submodules in the MMC
V_{CE}	On-state collector-emitter voltage of IGBT
φ	Lagging phase angle

1. Introduction

1.1 Background of the Thesis

At the end of 19th century, there was a 'battle of currents' which happened between Thomas Edison and George Westinghouse [1]. The first DC distribution system was built for lighting by Edison in 1882, which was operated with a fixed low voltage of 100 V or 110 V [2]. Due to the lack of power converters, the DC step-up and step-down conversions were very difficult. In 1891, Westinghouse made history by installing a 4 kV AC transmission line [3]. It was made possible by the development of poly-phase AC motors, generators and transformers by Nikola Tesla, which readily allowed voltage to be increased for transmission and reduced again for distribution. This ability paved the way for long distance transmission with low loss but relied on AC.

The trends of load growth, the electrification of heating and vehicle transport, and the development of distributed generations (DG) put significant strain on the existing AC distribution networks as they already operate close to their capacity limits in some cases [4]. In the UK, statistics show that full penetration of heat pumps (HPs) and electric vehicles (EVs) could increase the total electricity consumption by approximately 50% [5]. The installation of more cables or replacing existing cables with higher capacity ones is costly. Considering the average cost of replacing the existing buried low voltage (LV) cable is £98,400 per km, and the total length of underground cables is 328,038 km in the UK [6], it would be highly expensive and unrealistic to renew the entire distribution network.

In the UK, there is a legal commitment to have an 80% reduction in greenhouse gas (GHG) emissions by 2050 [7]. In order to reduce the GHG emissions from conventional fossil fuel power generation, there is a greater emphasis on the growth of renewable generations. In 2015, the total electricity generated from renewable energy sources have increased to 24.7%, from 19.1% in 2014 [8]. Figure 1.1 shows six main types of renewable energy sources in the UK, amongst which, wind power

(onshore and offshore) provides the largest amounts of generation. For wind turbines, there are AC-DC and DC-AC conversions before connected to the main grid. It can be seen in Figure 1.1 that solar photovoltaic (PV) has the highest absolute increase, from 1.5 TWh in the second quarter (Q2) of 2014 to 3.2 TWh in Q2 2015 [9]. It was reported that in the LV network, PV is the most common DG source [10]. As PV generates DC power, a DC-AC converter is required to integrate to the main grid, shown in Figure 1.2. Before connecting to any consumer electronics such as a mobile phone charger, printer or a computer, the AC electricity needs to be converted to DC. These additional conversion stages are unavoidable in the current AC networks, which potentially results in 1/3 of the energy generated from solar PV being lost at the point of use [11].

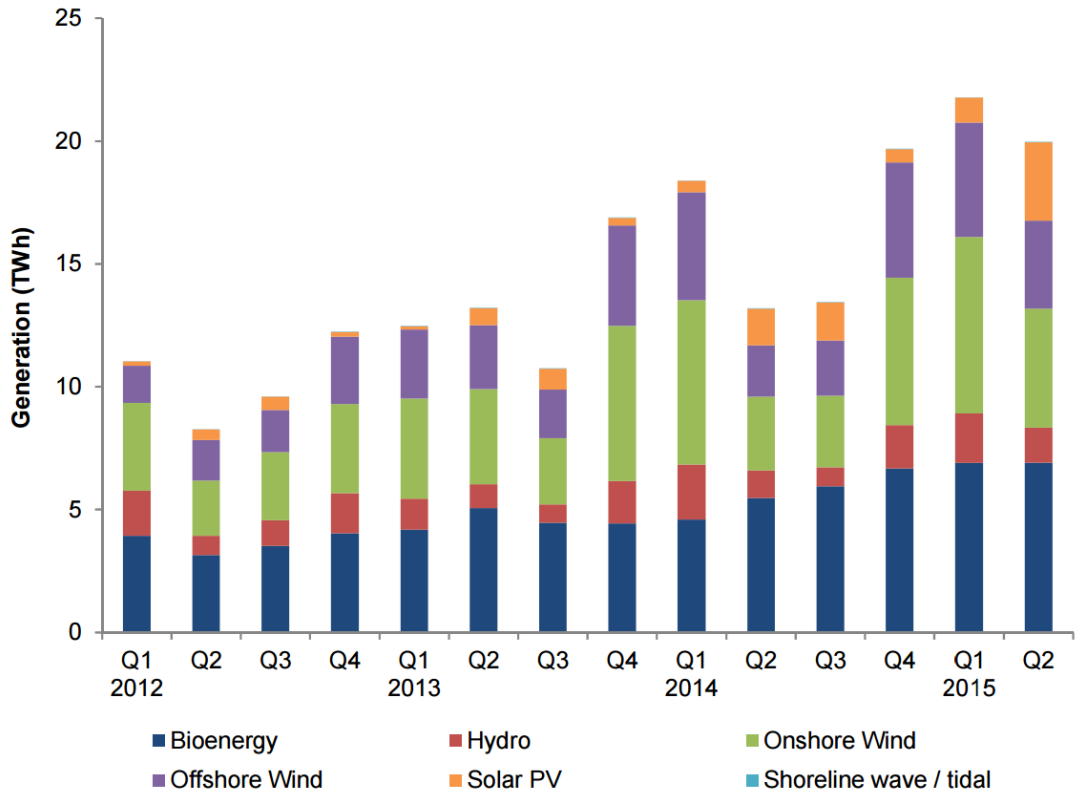


Figure 1.1 UK Renewable electricity generation (Q refers to one quarter of a year)[9]

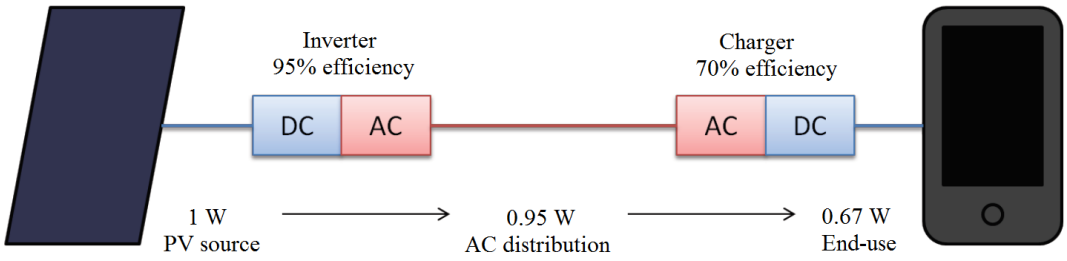


Figure 1.2 Conversion of 1 W power from PV panel (left) delivers 0.67 W of usable electricity to consumer electronics (right)

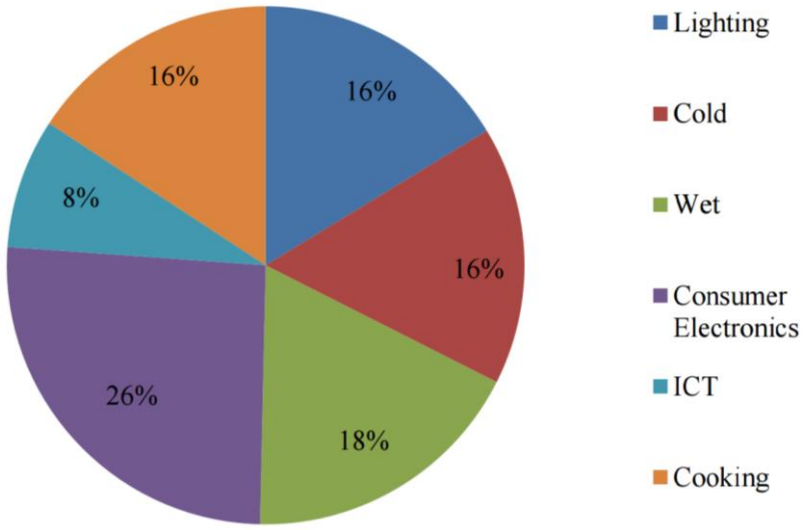


Figure 1.3 Detailed domestic electrical energy use by different sectors [12]
Note: **'Cold'** - freezers and refrigerators; **'Wet'** - washing machine, dryers and dishwashers; **'ICT'** - laptops, PCs and printers; **'Consumer electronics'** - TV, set-top box, DVD/VCR etc

Figure 1.3 illustrates the electrical energy consumption in residential area in the UK. Other references [13, 14] define the 'consumer electronics' as electronic or digital equipment for everyday use which is also include in the category 'ICT' shown in Figure 1.3. Irrespective of the categorisation of the 'ICT' devices, the electrical characteristics are similar – they are DC operated. A transformer and an AC-DC rectifier are usually installed in the adapters of those devices, which then introduce standby losses and harmonics. Current 'cold' and 'wet' appliances usually adopt variable frequency control to improve their efficiency, this includes an internal DC

stage as part of their grid interface. As a result, part of the energy will be wasted when transforming from AC mains to the internal DC stage.

Through the development of semiconductors, the step-up/step-down power electronics converters are no longer considered as a constraint for the distribution networks. Additionally, a higher DC distribution voltage can be used to release a large amount of additional power capacity without having to dig up existing cables. However, majority of the local loads still operate in AC. An extra DC-AC stage will be required to supply an AC load at the point of use in LVDC distribution networks, and reduced cable loss or increased capacity must be traded against conversion loss at the substation and the point of use. The conventional 2-level converter suffers from high switching losses, electromagnetic compatibility (EMC) issue, and requires a bulky output filter and an input filter when connected to a single-phase load. It is therefore important to develop a high-efficiency high-performance inverter for DC networks.

In summary, the existing LVAC distribution systems face significant challenges due to the increased electrical energy demand, the constraints of distributed generation and the rise of DC-operated loads. In the last mile of the electricity networks, LVDC distribution network presents a promising solution to improve the efficiency of distribution system. This thesis investigates the potential of developing high-efficiency, high-performance inverter to ensure that the extra DC-AC conversion stage will not negate the potential benefits of LVDC networks.

1.2 Aims of the Research Work

In this thesis, the potential of using low voltage DC distribution in the range of 500 V - 1.5 kV to replace the conventional three-phase 415 V AC distribution system is investigated. As described in Section 1.1, existing LVAC distribution system faces challenges from increased load demand, high power losses when connected to loads with an internal DC stage and having to accommodate new technologies such as PV and EVs. LVDC distribution networks present a promising solution, but they

introduce an extra DC-AC stage when connecting to AC loads. To overcome this limit, a DC-AC customer end converter needs to be designed in order to reduce the power losses as well as improving the power quality.

The main aims of this research work are to:

- Investigate the potential benefits of LVDC distribution, identify potential network configurations and appropriate network voltage. The associated increases in power capacity are then assessed.
- Investigate DC-AC converter topologies and control schemes for LVDC application. Evaluate the benefits of MOSFET-based MMC.
- Conduct a power loss calculation for different types of converters and develop thermal measurement to verify the loss calculation.
- Compare the power losses and cost of conventional 2-level IGBT converters and different levels of Si MOSFET MMC. Choose the appropriate number of levels for MMC in an LVDC application. Then compare with GaN HEMT MMC and SiC MOSFET 2-level converter in terms of power loss, power quality and heat sink size in order to determine an appropriate converter configuration.
- Design a high efficiency DC-AC converter based on capacitor and inductor sizing. Develop control strategies to minimise harmonic components of the circulating currents, as well as establishing voltage control to stabilise the output voltage under varying load conditions.
- Develop an experimental hardware prototype to test the current control strategies. Programme TI DSP to control the circuit.

1.3 Outline of the Thesis

The structure of the thesis is organised as follows:

Chapter 2 – The Concept of LVDC Distribution Systems

This chapter reviews the background of LVDC distributions system, where the benefits of DC distribution networks over the existing AC networks are evaluated.

The configuration of LVDC distribution system is presented based on the published literature. According to the existing cable voltage rating, the DC voltage level for LVDC network is proposed.

Chapter 3 – Investigation of High Efficiency DC-AC Converter

This chapter introduces DC-AC converter topologies for the application of LVDC distribution. Features of different converters are discussed and compared. The low voltage Si MOSFET MMC topology is proposed and its operational fundamentals are described. The feasibility of using parallel-connected MOSFETs is investigated experimentally.

Chapter 4 – Converter Design of MOSFET MMC

The process of the converter design of MOSFET MMC is described in this chapter, which includes the submodule capacitor sizing, arm inductor sizing and the output filter design of MMC. Two circulating current suppression control methods are proposed, along with the closed-loop control to stabilise the output voltage for varying load condition. A hardware prototype is developed for the verification of current control strategies.

Chapter 5 – Power Loss Calculation

This chapter presents semiconductor conduction and switching losses calculation methods for IGBT, MOSFET and wide band gap devices including SiC MOSFET and GaN HEMT. Input capacitor power loss for 2-level converter and submodule capacitor loss for MMC are analysed. In addition, inductor power loss and the relationship of modulation index and transformer turns-ratio are described. A comparison of experimental results for different types of converters are presented.

Chapter 6 – Thermal Design and Thermal Measurement Verification

In this chapter, the thermal analysis is presented and heat sink sizing is given. A thermal measurement method was designed to verify the power loss calculation presented in Chapter 5. The synchronous rectification and power loss reduction by parallel-connected MOSFETs were also validated through thermal measurement.

Due to the poor performance of the body diode of MOSFET, the necessity of using parallel-connected shottky diodes was tested.

Chapter 7 – Conclusions and Future work

This chapter draws the conclusion from this PhD thesis and proposes future research ideas.

2. The Concept of LVDC Distribution Systems

2.1 Introduction

The structure of power grid is changing. Electricity networks face the problem of increasing power capacity and achieving a low-carbon economy whilst maintaining an uninterrupted power supply. The standard EN50160 defines the voltage range of LV distribution is +10%, -6% in the UK [15]. It has been noted by many Distribution Network Operators (DNOs) that, typically, the voltage limit of the line is exceeded before the thermal limit of the cable is reached [16]. The voltage drop is caused by the line resistance and inductive reactance. To compensate this, and release additional capacity up to the cable thermal limit, extra equipment, in the form of reactive power compensation, would be required.

The capacity of low voltage AC distribution systems may be increased by upgrading existing cables or installing additional ones. This can be highly expensive and can take several months for DNOs to get permission, since it causes significant disruption to the local community [16]. A viable solution is to convert the existing distribution network to DC.

The development of high capacity power electronic devices has led to high efficiency with high reliability rectifiers and inverters, which can be utilised in LVDC. By adopting an LVDC distribution system, additional capacity can be released from existing cables. It also has the ability to accommodate the connection of new technologies such as embedded generation, energy storage and electrical EV charging. The advantages and challenges will be discussed in the following sections. Several proposed topologies, connections and groundings are presented.

2.2 The Benefits of LVDC Systems

Electric power grids are moving towards smart grids, features of which include distributed resources, communications and control, improved reliability and energy efficiency [17]. In this section, the benefits of adopting LVDC distribution and how LVDC networks can adapt to the new trend will be discussed. Current load characteristics of the distribution network will be presented, and the transfer capacity will be analysed. Also, the effect of new technology on the distribution networks will be discussed.

2.2.1 Load Characteristics

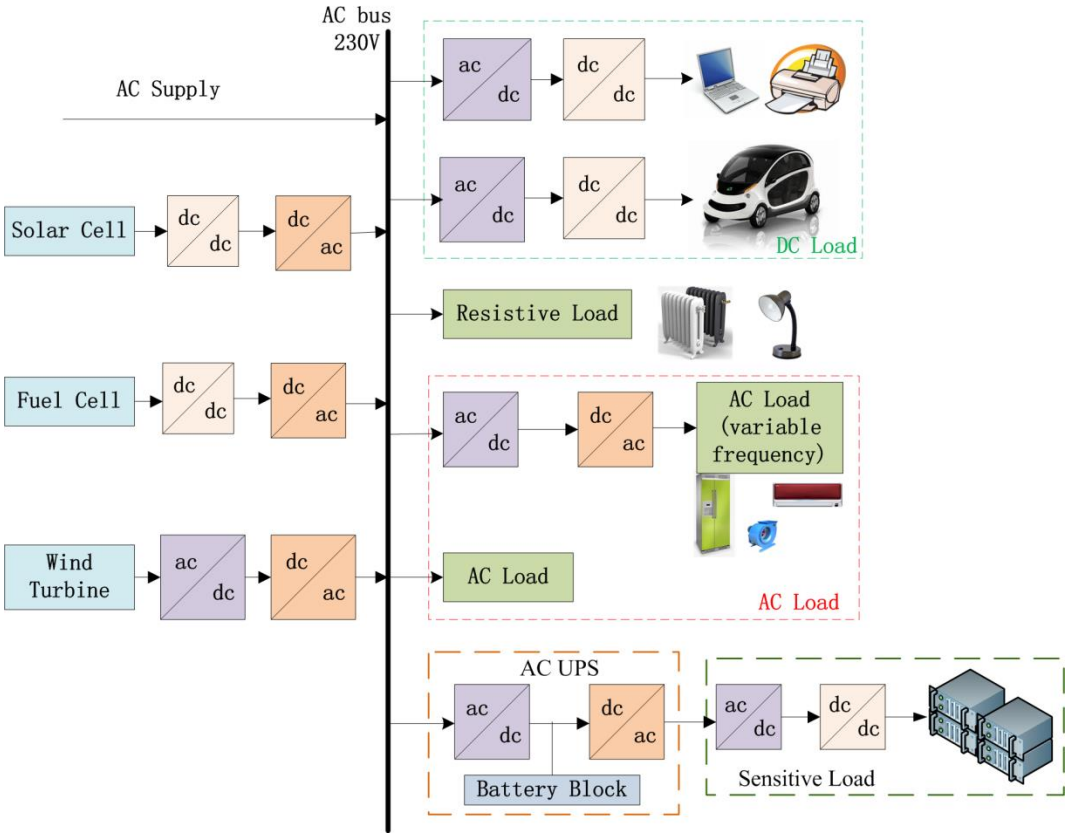
Today's load profile is very different from a century ago when lighting, heating and AC machines dominated. With the development of semiconductors and digital devices, the percentage of power electronic loads are increasing dramatically [2]. Those power electronic loads are DC-operated. The existing AC distribution system would face limitations in the improvement of efficiency.

Even though the household electronic appliances are designed to run with AC, many can be operated with DC directly. Electronic loads such as LED lighting, TVs, DVDs, personal computers, laptop, printers etc. operate internally on DC. As shown in Figure 2.1, the use of rectifiers in front of those DC loads will give rise to extra loss. The average efficiency of linear power supply is about 40-50% [18]. The rectifiers also introduce harmonic distortion which is unwelcome to the power system. In addition, electronic appliances operated on a low voltage need a step down transformer which consumes energy, even when the appliances are performing in standby mode. It is estimated that input transformers inside the adaptors of electronic loads lead to approximately 52 TWh/year standby losses in the EU-27 countries [19].

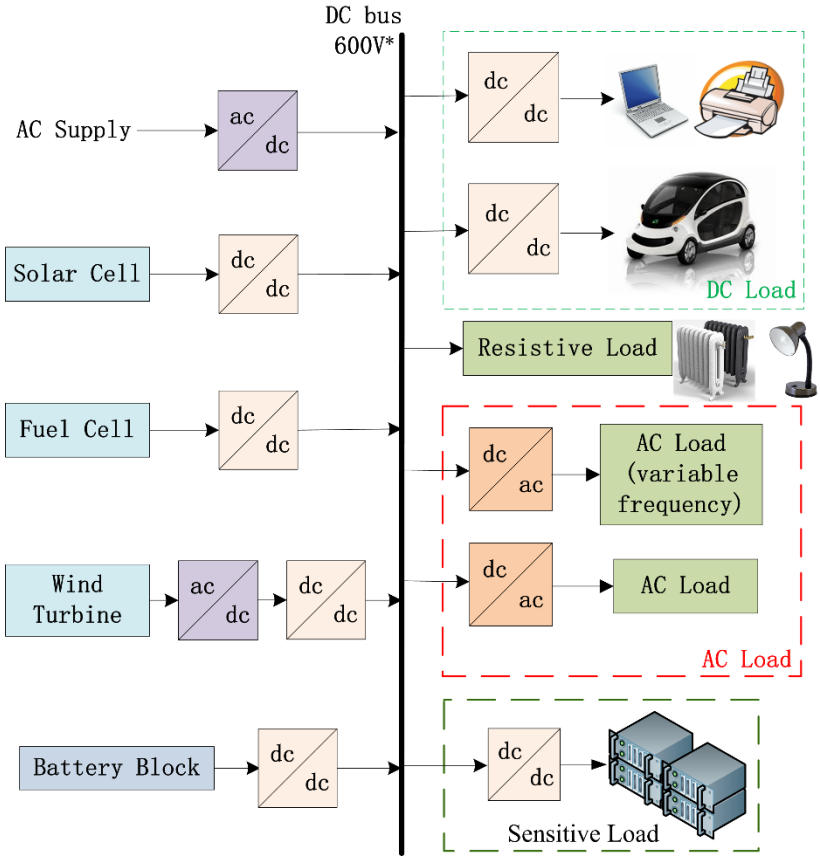
Some appliances with machine drives such as refrigerators and air conditioners need a variable output frequency. They convert AC to DC and DC to variable frequency AC by power electronics converters [20]. This requires two conversion stages, which increases energy losses.

Resistive loads like heating, incandescent lamps and stoves, can operate with both AC and DC, and the output power is equal if the RMS values are the same.

In summary, it is illustrated in Figure 2.1 that many conversion steps can be avoided by employing LVDC networks. Since each step causes losses and decreases the reliability of the system [21], LVDC distribution is a better choice from this point of view.



(a) Existing LV AC Distribution System



(b) Proposed LV DC Distribution system

Figure 2.1 Comparison of existing LVAC and proposed LVDC distribution schemes

2.2.2 Transfer Capacity and Cable Losses

Because of the higher voltage rating and higher RMS value of DC voltage, the transmission capacity of a low-voltage DC system is higher than that with corresponding low-voltage AC system [22]. The directive of EU low voltage (LVD 72/23/EEC) defines the range of low voltage is between 75 and 1500 V [23]. According to [24], the maximum transmission capacity of a unipolar 1500 V DC system can be 4 times more than the traditional AC system with the same 3-phase cables and transmission distance. The high transmission capacity also enable the LVDC network to substitute a part of MV networks [25]. A detailed case study of transfer capacity of LVDC networks will be presented in Section.2.3.4.

For same amount of power, the cable losses of DC systems can be lower than that of traditional AC system, since DC network can be operated at a higher voltage. It will lead to a lower current and the cable loss is proportion to the square of cable current. As presented in Section.2.3.4, the cable loss also depends on the DC voltage level, as well as the configuration of distribution systems.

2.2.3 Distributed Generation Units and Energy Storage

If a blackout occurs in the MV network, the islanding operation of the LVDC network would be possible if the LVDC network contains distributed generation (DG) units and energy storage units. Also, the reliability of the medium-voltage (MV) network increases since the LVDC network forms its own protection area.

The voltage level regulation can be improved by the use of DC networks. For instance, the output power of PV generation is unpredictable, and can lead to reverse power flow from LV side to MV side, which can influence voltage levels and cause power losses [26]. DC allows bi-directional power flow, as well as avoids phase imbalances which presents in AC system. The absence of reactive power in DC system also contributes to the stability of voltage levels [27].

DG units and energy reserves would be easier to connect to DC than AC in the LV network, because there are no problems with the frequency synchronization. Some of the DG technologies, like PV systems, generate DC power and the conversion stages can be reduced from 2 to 1 stage when connecting to DC network [28]. Wind turbines usually operate with variable speed to obtain maximum power, as do tidal generators. Therefore, AC-DC-AC back to back converters are used to synchronize the output to the grid [2]. However, a simpler and cheaper solution would be to connect to DC grid through an AC-DC converter. Storage systems, such as batteries and electric vehicles, could be more readily coupled with the LVDC network. The energy storage systems also play an important role to enhance the power quality [29].

Banks and datacentres contain sensitive loads, i.e. critical computers which are required to operate 24/7. In the existing AC network, numbers of online uninterruptible power supplies (UPS) are used to protect the sensitive loads from outages and transients of the utility grid [30]. As demonstrated in Figure 2.1 (a), The AC UPS is composed of an AC/DC converter, a battery block and a DC/AC converter [2]. Because the datacentres are DC-operated, adaptors consist of AC/DC and DC/DC converters are required [30]. In DC systems, however, a big battery block can be employed to provide uninterruptible power [21]. As shown in Figure 2.1 (b), DC networks help by removing a lot of small converters when connected to sensitive loads.

In summary, the use of LVDC distribution networks will increase the efficiency and reduce the cost because of a decreased number of AC/DC conversion stages [31]. In different types of electronic systems, all power electronic converters used can give rise to harmonic disturbances by injecting harmonic currents directly into the grid [32]. Therefore, by using DC network instead of AC, the harmonic disturbance would be reduced as well.

2.3 Layout of LVDC Distribution System

In this section, the cables, network connection and grounding of existing LVAC distribution networks are presented. Then the proposed topology, connection and grounding of DC networks is introduced. The suggested DC voltage level is given based on the existing cables, and the transfer capacity and cable losses are compared with the existing AC distribution system.

2.3.1 Existing LVAC Networks

In the UK LV distribution networks, there are four types of cables in terms of the core numbers, which are listed in Table 2.1.

Table 2.1 Four types of cables in the UK LV distribution networks

Cable type	The arrangement of conductors
5-core	Three phases + Street light + N*
4-core	Three phases + N
3-core	Two phases + N
2-core	One phase + N

*N denotes neutral

Before the 1970s the most common cable installed in the UK were the BS 480 and the BS 6480 4-core paper insulated lead covered (PILC) cables [27]. Their rated RMS voltage are 660/1100V and 600/1000V (phase to ground / phase to phase) respectively. Since 1970s, 4-core and 3-core cross-linked polyethylene (XLPE) insulated cables have generally been installed. The 4-core XLPE cables are used to replace the old PILC cables, and 3-core cables are used in extensions and new circuits. These cables are generally regarded as 'main' cables, which form the backbone of distribution networks.

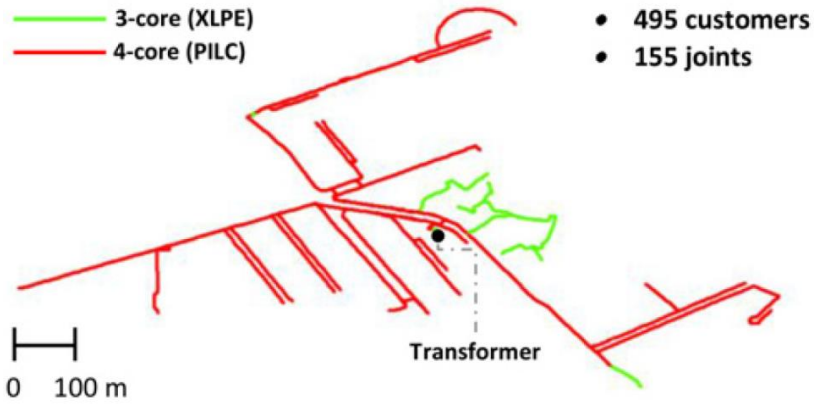


Figure 2.2 A typical UK distribution network, geographic information systems data provided by Electricity North West [27]

Figure 2.2 demonstrates the main cables in a typical UK distribution network. It shows the majority cable types are still PILC cables. In UK LV distribution networks, there are both three-phase 4-core cables and 3-core cables which are carrying two phases and one neutral. The connection of 3-core cables to customers is shown Figure 2.3, where 3-core cables are demonstrated in black. The illustration of cable

connections from 3-core cable to 4-core cable is presented in Figure 2.4, where the 2-core ‘service’ cable connects customers to the network.

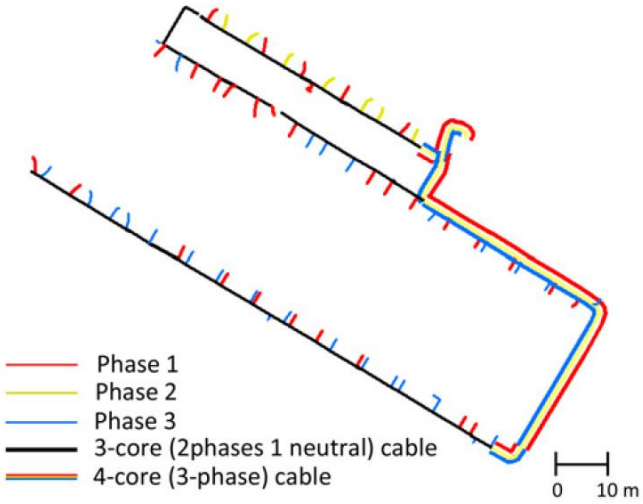


Figure 2.3 3-core cables in a real UK distribution network [27]

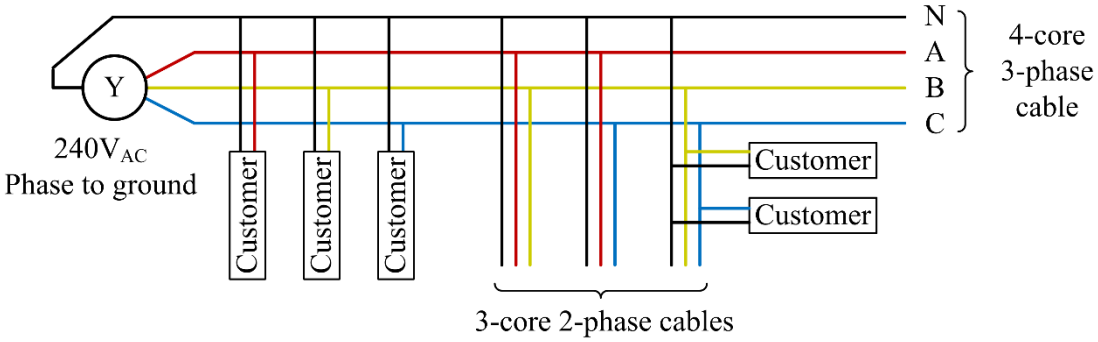


Figure 2.4 The connection of 3-core cable to 4-core cable in a distribution network

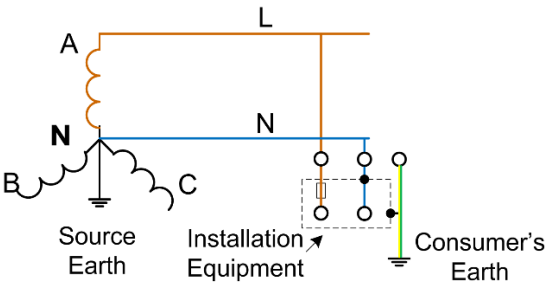
BS 7671 defines 5 types of earthing systems: TT, TN-S, TN-C-S, TN-C and IT. The meaning of each letter(s) is listed in Table 2.2.

Table 2.2 Meaning of letters in earthing system

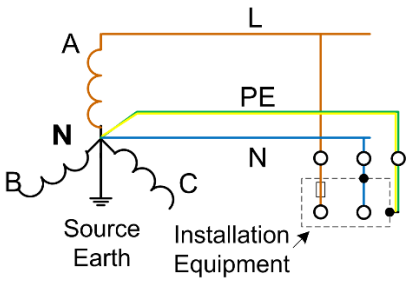
T	Earth (from the French word ‘Terre’)
N	Neutral
S	Separate
C	Combined
I	Isolated (or through a deliberately introduced impedance)
PE	Protective conductors
PEN	Combined neutral and protective conductor

In the UK, there are only three types of earthing system between a low voltage supply distribution tansformer and the consumer: TT, TN-S and TN-C-S. TN-C type is not allowed because it requires an exemption from the Electricity Safety, Quality and Continuity Regrulations, while the unearthed IT system is not permitted for a LV public supply in the UK [33].

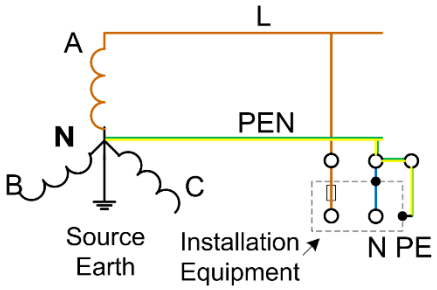
The three types of earthing configurations are shown in Figure 2.5. The TT system is usually used in an overhead line. The equipment at the consumer side is earthed through an electrode which is buried directly into the ground. The most common system connection in the UK is TN-S system, which consists of an earthed suppply conductor providing an earth connection to the consumer. TN-C-S system, where the neutral is served as a combined neutral and protective conductor, is employed for newly installed system in the UK [34].



(a) TT system



(b) TN-S system



(C) TN-C-S system

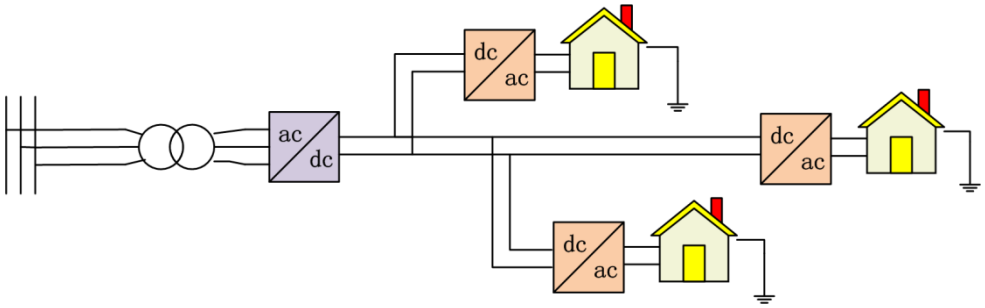
Figure 2.5 System earthing configurations

2.3.2 Topologies and Connections of LVDC Networks

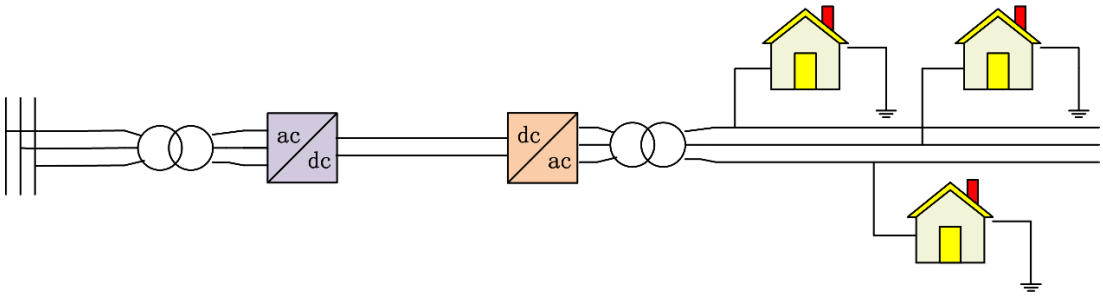
LVDC distribution networks consist of power converters and DC links between the converters. There are different kinds of topologies for an LVDC distribution system. One common point is that AC/DC conversion is located next to an MV line, if the

transmission network is using AC. The DC/AC conversion, however, can be located either at each customer end or served as an integrated DC/AC inverter right in the end of the main DC line. Depending on the location, reference [35] divides the LVDC system to two types – a wide LVDC distribution and a HVDC-link-type distribution.

In comparison to the topology of existing LVAC system, the wide LVDC distribution network has multiple branches and does not have to separate into 3-phase. In this case, the LVDC distribution system will not face the problem of unbalanced loading. Example of basic implementation of an LVDC distribution system is shown in Figure 2.6.



(a) Topology of a wide LVDC distribution system



(b) Topology of an HVDC-link-type distribution system

Figure 2.6 Topology schematic of LVDC distribution networks

The HVDC-link-type LVDC topology is composed of one DC line interconnecting two separate AC networks. In this kind of network, customers are connected to a 3-phase AC network which is similar to the existing LVAC network. A transformer is required to be connected between the DC link and the customer networks to ensure the compatibility with the existing AC system [35]. Figure 2.6 (b) presents an example of an HVDC-link-type distribution system.

The connections of LVDC distribution system can be divided into two types: unipolar and bipolar. The difference is how many voltage levels the system has. The unipolar system transmits energy at one voltage level. All the customers are connected to this one voltage level, as shown in Figure 2.6.

The bipolar system is constituted by two series-connected unipolar systems, as illustrated in Figure 2.7. The loads in the bipolar system can be connected between 3 voltage levels in multiple ways, such as (a) between one current conductor (either positive or negative) and the zero conductor, (b) directly between the positive and negative conductors and (c) between the positive and negative conductors with neutral connection. Case (a) will face the unsymmetrical loading problems. In this situation, there will be a continuous current flow in the neutral line. For case (b) and (c), the cost of power electronic devices will increase due to the higher voltage rating [36].

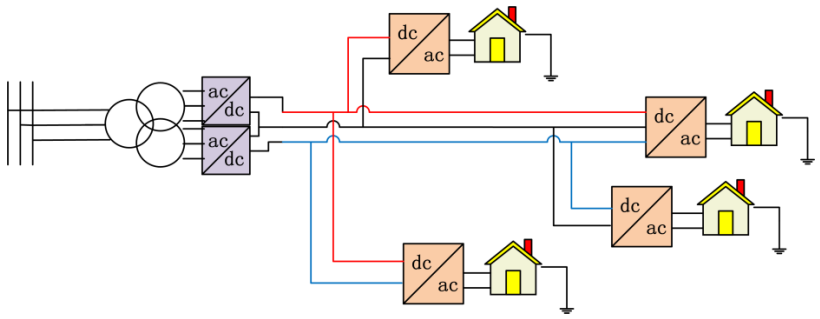


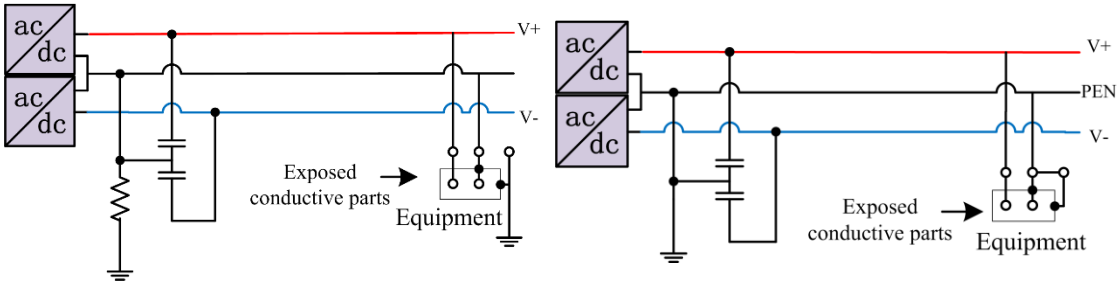
Figure 2.7 A bipolar LVDC distribution system

2.3.3 Grounding of DC Networks

Grounding is a major issue of an electrical power system since it affects its safety, survivability and power availability [37]. When selecting grounding methods, two opposing requirements need to be considered: (1) minimizing DC stray current, and (2) maximizing personnel and equipment safety [38]. For a DC system, the benefits of grounding include: easy to detect the ground faults, limiting voltage stress under transient fault conditions and disconnecting faulty equipment under steady-state fault [37]. During ground faults, however, it will give rise to a large ground current

and DC link voltage transient. Ungrounded DC systems on the other hand provide small stray-current and voltage-transient during ground faults [39]. However, it's hard to detect the fault due to the small value of ground fault current [40].

Figure 2.8 presents two grounding topologies for a bipolar LVDC system. Figure 2.8 (a) shows the ungrounded IT system, where the positive and negative conductors are connected to the neutral line by capacitors. The neutral line is grounded though earth impedance and the exposed conductive parts of equipment are grounded. Figure 2.8 (b) illustrates the grounded TN system, where the neutral line is grounded and the exposed enclosure of equipment is connected to the PEN [40].



(a) IT DC system (b) TN DC system

Figure 2.8 Different grounding systems for LVDC networks

2.3.4 DC Voltage Level and Cables

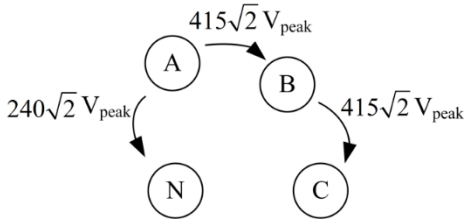
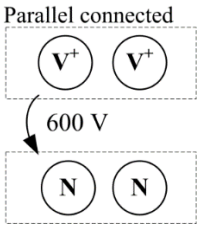
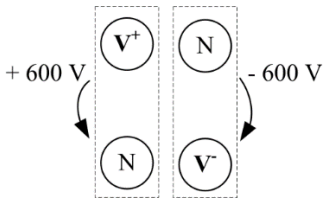
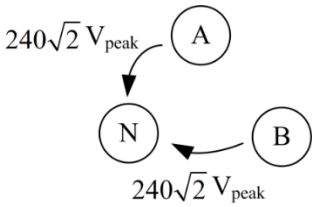
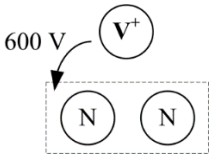
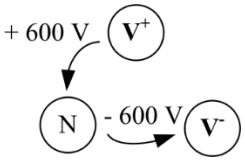
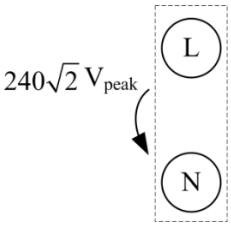
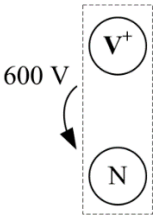
Study show that, for the same thermal limit and the voltage drop of the cable, more power can be transmitted with a DC distribution system than in an identical AC system. This will be enhanced further by the increase of voltage level [36]. Therefore, ±750 V are chosen to be the DC bus voltage for the Finnish LVDC test network [41, 42], which reaches the maximum value of low DC voltage.

As mentioned in Section 2.3.1, the existing 'main' cables are mainly 4-core and 5-core cables [35]. PILC 4-core BS 6480 is the most common cable, which is rated at 600/1000 V (phase to neutral and phase to phase RMS value) [43]. In this thesis 600 Vdc is chosen to be the DC distribution voltage. The phase to phase voltage in a bipolar DC system would be 1200 V, which is lower than the peak voltage 1414 V

for the BS 6480 cables. Voltage can be chosen at a higher value which is still within the existing cables' thermal and isolation limits. However, 600 V is chosen because there are a wide variety of power devices available in this voltage range. It also provides the network with redundancy for up to 17% over-voltage.

Examples of cable connections for unipolar and bipolar DC systems are given in Table 2.3. For unipolar DC systems, the conductors can be parallel-connected to take advantage of all cable wires.

Table 2.3 Cable connections for AC and DC networks

	AC	DC	
		Unipolar	Bipolar
4-core			
3-core			
2-core			

A. Power transfer capability comparison of the AC and DC networks

To compare the AC and DC network power transfer capability, a few assumptions should be made. There are two constraints for the maximum current that can flow in a cable, the thermal limits and the maximum voltage drop [44]. Below a certain cable length, the thermal limit is the main constrain. Therefore, the following assumptions are made:

- The current rating of 3 types of cables (4-core, 3-core and 2-core) is chosen to be 265 A per core, which is derived from cable standards [27, 45].
- The power factor is assumed to be 0.95 for AC networks.
- Voltage drop is not taken in to consideration in this calculation.

The transmission capacity calculation results for different cable configurations are listed in Table 2.4 and demonstrated in Figure 2.9, which shows in 4-core cases, the transfer capacity of DC network is 1.75 times that of 3-phase AC network. The unipolar and bipolar configurations have an impact on the transfer capacity for DC networks, but both types can transfer larger power capacity than 3-core AC network. For 2-core service cables, the power transferred by DC is 2.63 times that of AC system. From this point of view, DC is superior to AC since it can release a large amount of power capacity without replacing the buried cables.

Table 2.4 Transfer capacity comparison of different cable configurations

		AC	DC	
			Unipolar	Bipolar
4-core	V_{RMS} (V)	240	600	1200
	I_{RMS} (A)	265	530	265
	P (kW)	181.3	318	318
3-core	V_{RMS} (V)	240	600	1200
	I_{RMS} (A)	265	265	265
	P (kW)	120.8	159	318
2-core	V_{RMS} (V)	240	600	
	I_{RMS} (A)	265	265	
	P (kW)	60.4	159	

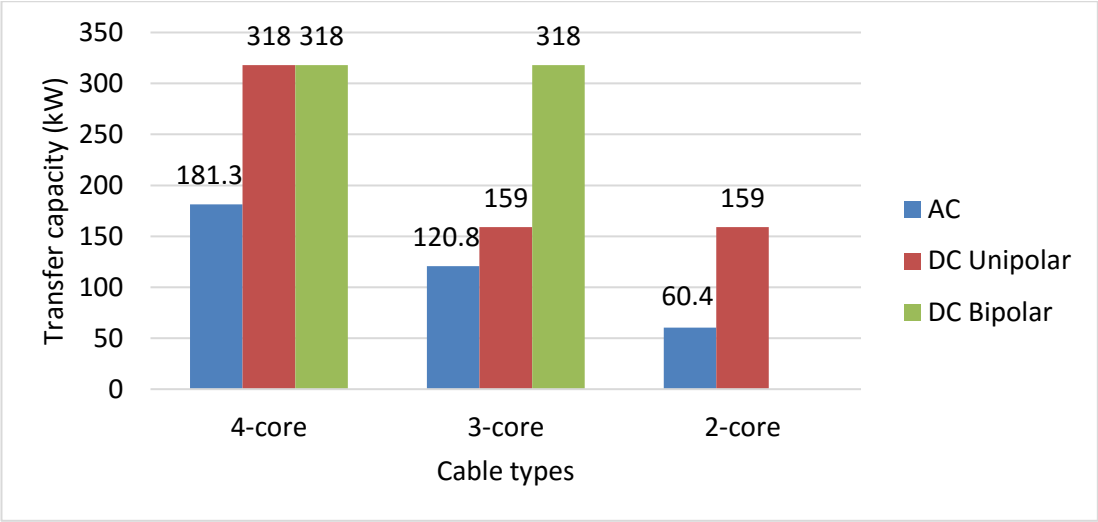


Figure 2.9 Transfer capacity comparison of different cable configurations, at 0.95 PF

B. Cable loss comparison when delivering the same amount of power

When delivering the same amount of power, the cable losses will be compared in the following paragraphs. Table 2.5 shows the symbols definition used in this comparison.

Table 2.5 Symbols definition for cable loss calculation

Symbol	Definition
P	Load power consumption
r	Cable resistance per unit length
l	Cable length
$\cos\phi$	Power factor
V_{ac}	AC phase to ground RMS voltage (240 V)
V_{dc}	DC bus voltage (600 V)
$I_{ac,2}$	RMS current of an AC system with 2-core cables
$\Delta P_{ac,2}$	Power losses of an AC system with 2-core cables
$I_{dc,2}$	Current of a DC system with 2-core cables
$\Delta P_{dc,2}$	Power losses of a DC system with 2-core cables
$I_{ac,4}$	RMS current of a 3-phase AC system with 4-core cables
$\Delta P_{ac,4}$	Power losses of a 3-phase AC system with 4-core cables
$R_{\Delta P}$	Cable loss ratio of DC network over AC network

1) 2-core cables

For single-phase feeders (2-core cables) in LVAC systems, power losses on the cables are given by (2-1) and (2-2) [21].

$$I_{ac,2} = \frac{P}{V_{ac} \cdot cos\varphi} \tag{2-1}$$

$$\Delta P_{ac,2} = 2 \cdot rl \cdot I_{ac,2}^2 = 2 \cdot \frac{rL}{cos^2\varphi} \cdot \frac{P^2}{{V_{ac}}^2} \tag{2-2}$$

In a DC system only active power is present. For the same load power consumption *P* and the same length 2-core cables, current and power losses in the DC system are expressed in (2-3) and (2-4) [46].

$$I_{dc,2} = \frac{P}{V_{dc}} \tag{2-3}$$

$$\Delta P_{dc,2} = 2 \cdot rl \cdot I_{dc,2}^2 = 2 \cdot rl \cdot \frac{P^2}{V_{dc}^2} \tag{2-4}$$

The DC-AC power loss ratio is presented in (2-5).

$$R_{\Delta P} = \frac{\Delta P_{dc,2}}{\Delta P_{ac,2}} = \frac{I_{dc,2}^2}{I_{ac,2}^2} = \frac{{V_{ac}}^2}{V_{dc}^2} \cdot cos^2\varphi = 0.16\, cos^2\varphi \tag{2-5}$$

Equation (2-1) and (2-3) demonstrate that the current in single-phase is always lower than in the existing LVAC feeder when delivering same amount of active power. Therefore, the cable losses of DC network is lower, as illustrated in Table 2.6.

Table 2.6 Cable losses of LVDC networks with 2-core cables

	Per phase current	Cable loss	Power ratio $R_{\Delta P}$
DC network	$\frac{P}{V_{dc}}$	$2 \cdot rL \cdot \frac{P^2}{V_{dc}^2}$	$0.16\, cos^2\varphi$

2) 4-core cables

Similarly, for a three-phase AC load (4-core cables), (2-6) and (2-7) can be obtained.

$$I_{ac,4} = \frac{P}{3 \cdot V_{ac} \cdot cos\varphi} \tag{2-6}$$

$$\Delta P_{ac,4} = 3 \cdot rl \cdot I_{ac,4}^2 = \frac{1}{3} \cdot \frac{rl}{cos^2\varphi} \cdot \frac{P^2}{V_{ac}^2} \tag{2-7}$$

Table 2.7 summarises the relative power loss of a 4-core cable energised under unipolar and bipolar DC. $R_{\Delta P}$ represents the ratio of DC to AC power loss, for a fixed power transmission.

Table 2.7 Cable losses of unipolar and bipolar LVDC networks with 4-core cables

DC network	Per phase current	Cable loss	Power ratio $R_{\Delta P}$
Unipolar	$\frac{P}{V_{dc}}$	$2 \cdot rL \cdot \frac{P^2}{V_{dc}^2}$	$0.96\ cos^2\varphi$
Bipolar	$\frac{P}{2V_{dc}}$	$rL \cdot \frac{P^2}{V_{dc}^2}$	$0.48\ cos^2\varphi$

For 4-core cables, the unipolar cable configuration sees a larger cable loss when compare to a bipolar configuration. The reason is that the load current in unipolar configuration is higher because the same power is carried by two conductors. However, the power loss of unipolar network is still lower than AC system because the AC system has power losses in three cables while the unipolar DC system only has two.

If the DC link voltage is designed higher, the power losses in DC networks will becomes much lower. In summary, when deliver the same amount of power, LVDC distribution system sees a lower cable loss.

2.4 Challenges of LVDC Distribution systems

As discussed in Section 2.2, the LVDC distribution systems have many benefits, such as higher transfer capacity and higher efficiency, when connected to DC-operated loads. There are no skin effect and reactive power issues related to DC networks.

However, the LVDC network faces electrical safety challenges. The AC power distribution system has mature safety and protection technologies since it has been developed for decades [47]. The design of AC circuit breakers is aided by the occurrence of naturally occurring current zeros. In DC systems these do not occur

and must be generated artificially by the breaker, making their design challenging. One solution is to create a longer distance between the contacts in the circuit breaker, generating an increased voltage [30]. Another is to use a breaker together with a resonant circuit which will create a voltage zero [48]. Detailed protection analysis for LVDC distribution systems can be found in [41, 49].

Another challenge is at the customer end DC-AC stage, since there are many existing AC loads. The DC-AC interface must achieve high efficiency whilst meeting user power quality requirements. For conventional two-level converters, choice of high switching-frequency reduces filter size and provides improved power quality. However, this results in higher losses and EMC issues. Therefore, a new kind of high-performance high-efficiency inverter which has multiple levels, lower switching frequency and reduced harmonic content is investigated in this thesis.

2.5 Summary

This chapter evaluated the benefit of LVDC over the existing LVAC distribution system. Compared to the conventional AC distribution system, DC distribution provides better utilisation of conductor voltage rating, thereby increasing the power transmission capacities. In this thesis, DC voltage level is chosen to be 600 V in consistency with the existing cable rating, as well as improving the transfer capacity. A case study of transmission capacity shows 1.75 times more capacity can be released by adopting 600 V unipolar or ±600 V bipolar LVDC without replacing the buried cables for the 4-core main cables. For the existing 2-core service cables the LVDC transfer capacity can achieve 2.63 times more power than the 240 V single-phase AC networks.

The use of power electronics to provide point-of-use regulation of AC supplies can eliminate reactive and harmonic power flows whilst maintaining the customer power quality. The number of DC-operated appliances have increased dramatically. LVDC networks can potentially provide higher efficiency since many conversion steps are avoided. Distributed resources are a main feature of smart grids, many of which are

naturally DC power sources or require a DC stage as part of the power conversion process. DC distribution is a promising solution to accommodate those changes.

However, the DC networks are more complex than the AC networks. The electrical safety is one of the great challenges to the DC networks. Protection methods have been investigated and analysed by many researchers, but are not the topic of this study.

Although there is a growing trend for DC compatible loads many traditional AC loads will remain on the distribution network. The presence of these AC loads will require an extra DC-AC conversion stage and incur additional losses. Where large numbers of AC loads are present conversion loss may compromise the efficiency of DC distribution networks. Therefore, the development of a high efficiency high performance DC-AC converter is another major challenge to the LVDC networks. This study mainly focuses on the DC-AC converter design for LVDC applications.

3. Investigation of High Efficiency DC-AC Converter

3.1 Introduction

As mentioned in Section 2.4, the DC-AC power conversion stage is one of the major challenges for LVDC distribution networks. The aim of this thesis is to investigate a high efficiency and high performance inverter, so that the extra DC-AC stage will not negate all the benefits of LVDC network. This chapter compares the conventional 2-level converter with multilevel converters, discusses briefly about different multilevel converter topologies and proposes a low voltage MOSFET-based MMC to be the promising choice for LVDC applications.

In addition, the topologies and benefits of commonly used MMC are discussed. The modulation techniques and capacitor voltage balancing control are then analysed. The potential for MOSFET-based MMC for low voltage applications is discussed. It is demonstrated that the parallel-connection of MOSFETs can reduce the conduction loss dramatically. The limits of MOSFETs parallel connection are then investigated, evaluated and tested.

3.2 Voltage Source Inverters

There are two basic configuration types for DC-AC conversion, Current Source Inverters (CSI) and Voltage Source Inverters (VSI). In comparison with CSI, the VSI has proven to be more reliable with higher efficiency and faster dynamic response [50]. Therefore, different kinds of VSI will be discussed in this section. For VSI, the DC input voltage is usually constant, while the amplitude of the AC output voltage can be controlled by certain modulation techniques [51].

3.2.1 Two-level and Commonly Used Multilevel VSI

According to the levels of output voltage, VSI can be divided into two categories: two-level and multilevel. Figure 3.1 shows a typical 2-level IGBT-based VSI. Each leg has two IGBTs which are connected in series, where the voltage stress for each IGBT is the same as the DC link voltage. The switching frequency of each IGBT equals to the carrier switching frequency.

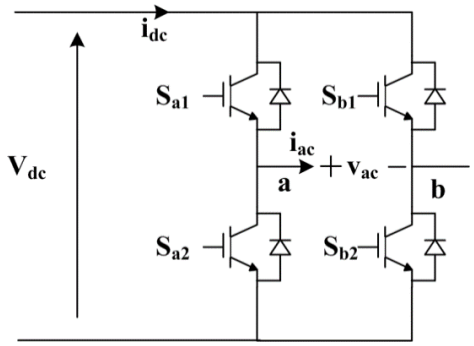


Figure 3.1 2-level inverter

There are many commonly used multilevel converters topologies. Three-level diode clamped converter is also called neutral point clamped (NPC) multilevel converter, as shown in Figure 3.2. Requirements for tolerable voltage ripple at the neutral point may dictate the use of increased capacitance, whilst additional inverter control may be required to ensure that the neutral point remains balanced. For the NPC converter, the power losses are not equally distributed among the semiconductors [52]. The switching frequency and rating current is limited by the power loss in the most stressed semiconductor device [53]. For more than three levels, the diode clamped converter cannot maintain balance of the cell capacitors without compromising power quality or adding additional voltage balance circuits [54, 55]. The physical layout with more than five levels can become impractical due to the large number of diodes. It can also limit the effectiveness of the voltage clamping circuit. The difficulties associated with capacitor voltage balance makes the generalized diode clamped converter unsuited for the application under consideration.

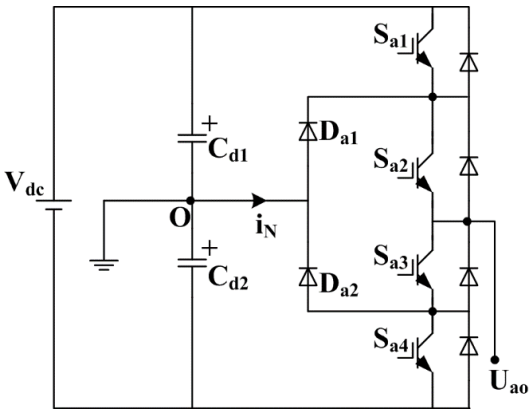


Figure 3.2 One phase of NPC

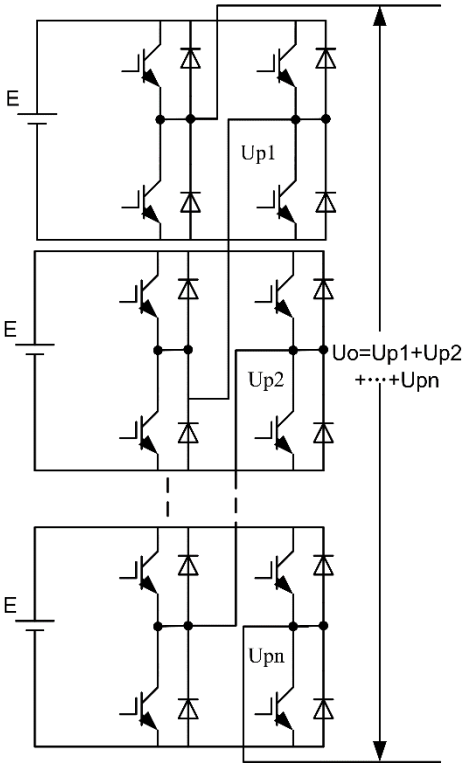


Figure 3.3 Cascaded H-bridge multilevel converter

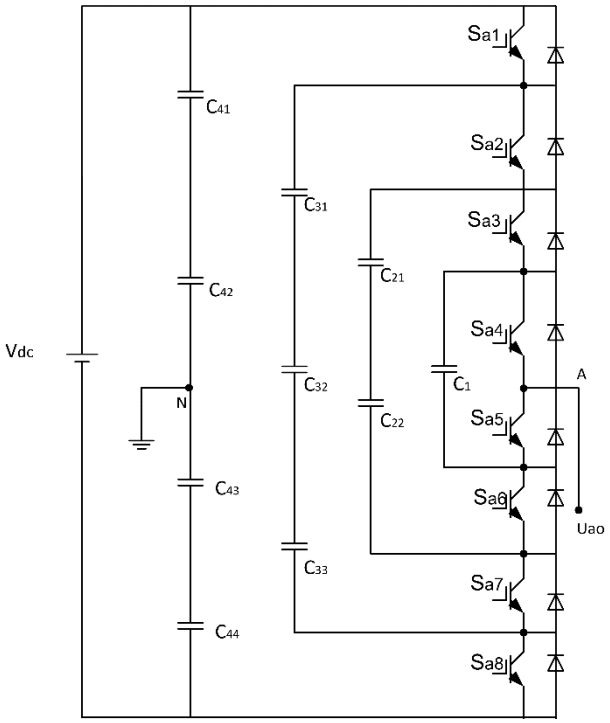


Figure 3.4 5-level flying capacitor converter

As presented in Figure 3.3, the cascaded H-bridge multilevel converter requires numerous isolated DC sources, and the absence of a common DC link also makes this topology unsuited to this project [56]. The flying capacitor converter, shown in Figure 3.4, is limited by the relative complexity of the circuit topology and the large number of capacitors required. The inherent capacitor location makes clamping voltage transients across the device difficult to achieve. Converter control is

complicated by the need to maintain capacitor voltage balance, and this may tend to increase device switching frequency and switching losses will therefore also increase [57].

3.2.2 Modular Multilevel Converter

The modular multilevel converter (MMC) was first introduced in 2003 by Marquardt for high-voltage applications [58] and has since become the most commonly used voltage-source converter (VSC) for high-voltage direct current (HVDC) transmission applications. Figure 3.5 shows the topology of a single-phase MMC. ***n*** cascaded submodules in series with arm inductors constitute one arm and two arms form one phase leg. The presence of arm inductors is a fundamental feature of MMC, two major functions of which are to limit DC fault currents and circulating currents [59]. A given number of cell submodules may be used to generate the desired AC output. MMC processes high efficiency with high power quality and as such is a potential topology for use in low voltage applications

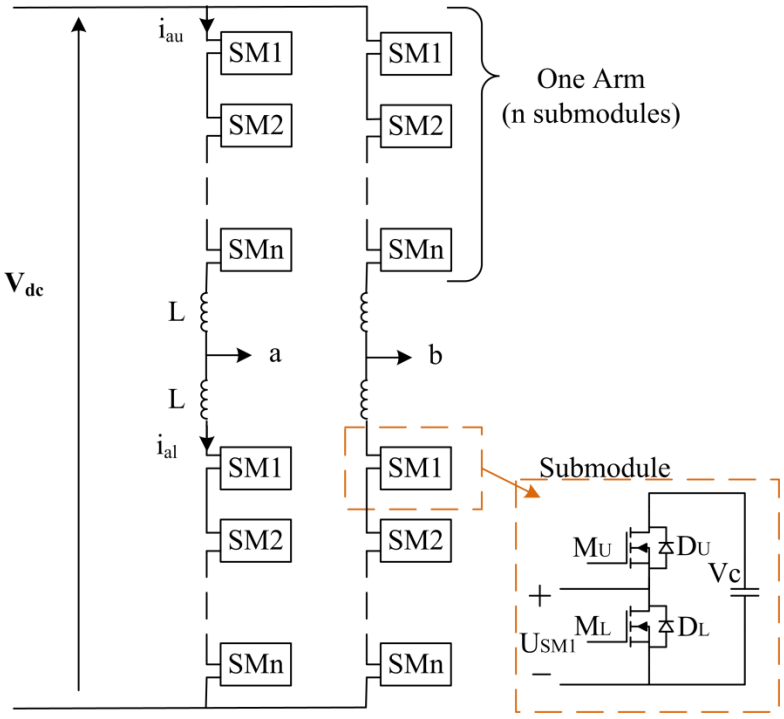
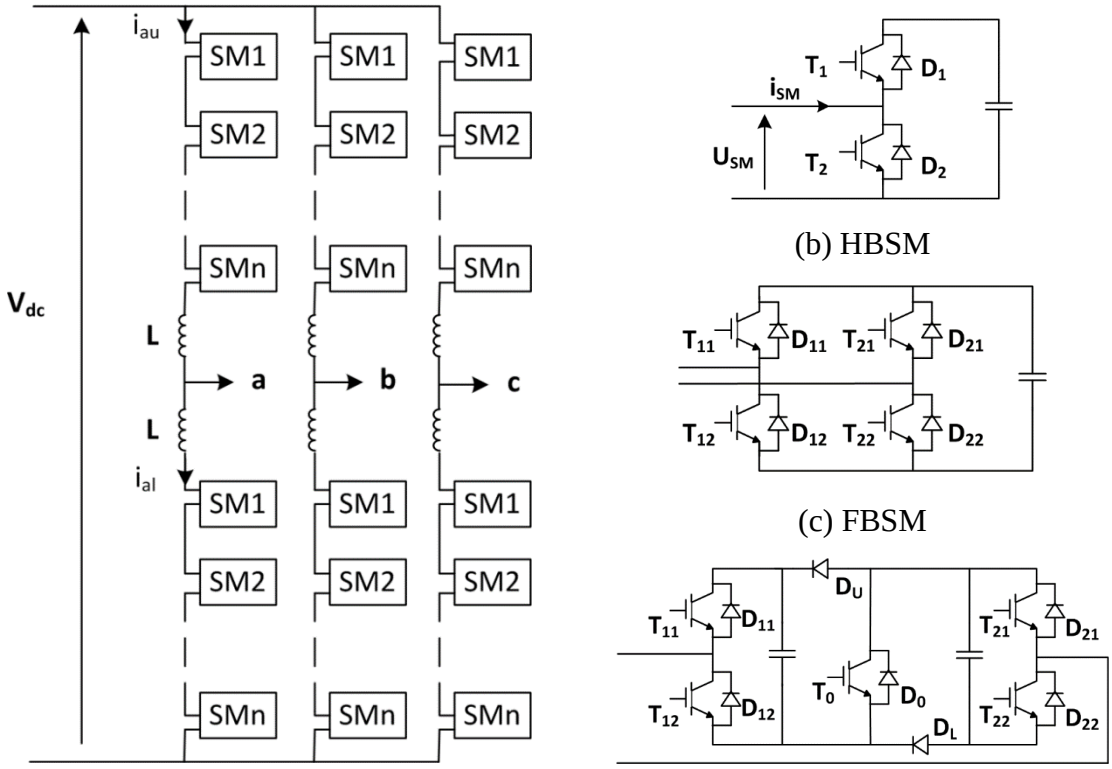


Figure 3.5 Single-phase MOSFET-based (n+1) level MMC

A. Topologies of MMC

The basic building-blocks of the MMC are the half-bridge submodule (HBSM) and full-bridge submodule (FBSM). Alternative submodule structures and hybrid multilevel converter topologies are presented in [60]-[62], giving improved converter efficiency when compared with FBSM-based MMC, DC fault blocking and voltage clamping functionality.

1) Submodule Structures



(a) Three-phase MMC (b) HBSM (c) FBSM (d) CDSM

Figure 3.6 Topology of MMC and 3 common structures of submodules

- Half-bridge submodule

Figure 3.6 (b) presents the half-bridge submodule (HBSM), which gives the lowest losses and cost in comparison to other multi-level topologies [58,63]. However, HBSM-based MMC cannot block fault current that occurs when the DC side voltage drops below the peak AC side voltage, i.e. the AC-side reverse current. As the HBSM can only generates unipolar voltages (Table 3.1) and operates in two quadrants [64]. It does not possess the ability to block AC-side reverse current.

Table 3.1 Switching States of one HBSM

	T_1	T_2	U_{SM}	$i_{SM}>0$	$i_{SM}<0$
Normal Mode	1	0	U_C	D_1	T_1
	0	1	0	T_2	D_2

Note: '1' means the switch is under on-state, while '0' means off-state. U_{SM} denotes the output voltage of the submodule and i_{SM} stands for the input submodule current.

- Full-bridge submodule

The structure of full-bridge submodule (FBSM) is illustrated in Figure 3.6 (c). As shown in Table 3.2, FBSM can generate bipolar voltages. Therefore, it has the reverse-blocking capability and maintains the power control ability during a large DC-bus voltage drop [60, 61]. Since the number of semiconductors is doubled, the implementation of FBSM will lead to a higher cost and power losses.

Table 3.2 Switching States of one FBSM

	T_{11}	T_{12}	T_{21}	T_{22}	U_{SM}	$i_{SM}>0$	$i_{SM}<0$
Normal Mode	1	0	0	1	U_C	D_{11}, D_{22}	T_{11}, T_{22}
	1	0	1	0	0	D_{11}, T_{21}	T_{11}, D_{21}
	0	1	0	1	0	T_{12}, D_{22}	D_{12}, T_{22}
	0	1	1	0	$-U_C$	T_{12}, T_{21}	D_{12}, D_{21}
Block Mode	0	0	0	0	U_C	D_{11}, D_{22}	--
	0	0	0	0	$-U_C$	--	D_{12}, D_{21}

- Clamped doubled submodule

Clamped doubled submodule (CDSM, Figure 3.6 (c)) provides fault blocking capability but with a lower device count than the FBSM. Power losses from conduction are increased slightly due to the presence of T_0 in comparison to the HBSM. In comparison with FBSM, however, the power losses are significantly reduced. Table 3.3 indicates that in normal operation mode, the CDSM can operate in three quadrants [65].

Table 3.3 Switching States of one CDSM

	T_{11}	T_{12}	T_{21}	T_{22}	T_0	U_{SM}	$i_{SM}>0$	$i_{SM}<0$
Normal Mode	1	0	0	1	1	$2U_C$	D_{11}, D_0, D_{22}	T_{11}, T_0, T_{22}
	1	0	1	0	1	U_C	D_{11}, D_0, T_{21}	T_{11}, T_0, D_{21}
	0	1	0	1	1	U_C	T_{12}, D_0, D_{22}	D_{12}, T_0, T_{22}
	0	1	1	0	1	0	T_{12}, D_0, T_{21}	D_{12}, T_0, D_{21}
Block Mode	0	0	0	0	0	$2U_C$	D_{11}, D_0, D_{22}	--
	0	0	0	0	0	$-U_C$	--	D_{12}, D_L, D_U, D_{21}

- Other alternative submodules

A variety of other submodule topologies are possible, such as Three-level Submodules, Asymmetrical Double Submodule, Cross- or Parallel-connected Submodule, Flying Capacitor Submodule and NPC-Type Submodule [64, 66]. A comparison on different submodule structures was conducted by Nami in [64], which considered number of output voltage levels, voltage blocking ability, bipolar operation, design and control complexity. It concludes that there is a trade-off between submodule complexity, functionality, and the optimum topology should be chosen based on specific application.

2) Hybrid Multilevel Converter

In this section, a converter that has a mix of HBSM, FBSM and also 2-level switches are introduced as hybrid multilevel converters. Those topologies all have the DC fault blocking functionality but with fewer semiconductors than FBSM based MMC.

- Hybrid MMC with mixed submodules

A hybrid MMC presented in [62] contains mixed submodules of HBSM and FBSM (shown in Figure 3.7). The FBSM can be used to generate a negative voltage for DC fault control but with increased complexity in submodule voltage and energy control.

- Hybrid 2-level with AC side cascaded FBSM multilevel converter

Figure 3.8 indicates one phase of a $4\boldsymbol{n}+1$ level converter which contains series-connected IGBTs and $\boldsymbol{n}$ cascaded FBSMs in the AC side. The 2-level VSC controls

the fundamental voltage at 50 Hz or 150 Hz (when selective harmonic elimination PWM is applied) switching frequency. The FBSMs are served as active power filter to improve the output voltage harmonic performance [67]. However, the active switching devices of the 2-level VSC must withstand voltage stress equivalent to the full DC side. Short circuits on the DC side will result in the DC side capacitors discharging and an inrush current from the AC grid. The FBSM in Figure 3.8 can be used to block this inrush AC fault current.

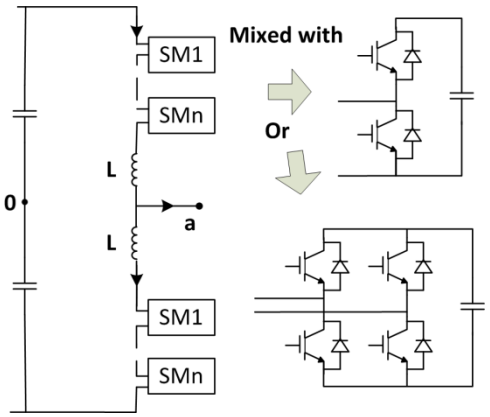


Figure 3.7 Hybrid MMC

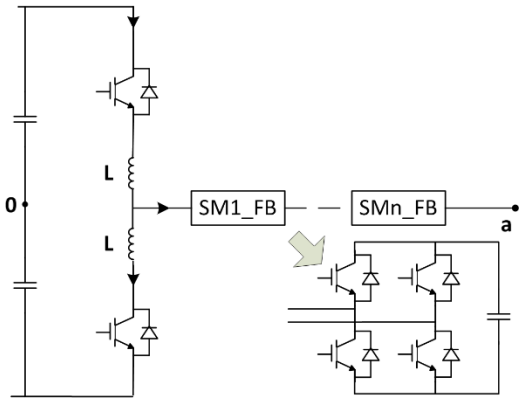


Figure 3.8 Hybrid 2-level with AC side cascaded FBSMs

- Alternate Arm Converter

A hybrid multilevel converter proposed in [68] is Alternate Arm Converter (AAC), as shown in Figure 3.9. In AAC, a stack of FBSM, a string of IGBT (the director switch) and an arm inductor compose one arm and two arms form one phase leg. The function of FBSM is to generate multistep voltage and the director switch to decide which arm will conduct. With upper arm for the construction of positive half period of the AC sinewave and the lower arm for the negative half period, the stack of FBSM in one arm is only required to produce half of the DC link voltage. Therefore, the minimum number of FBSM it requires is only half of the FBSM-based MMC. By generating negative voltage in the FBSM the AAC is capable of blocking DC faults. It is capable of achieving soft-switching during the cross-over between the two arms of one leg [68]. The series connection of IGBTs still requires nearly identical switching characteristics and dynamic voltage sharing [66]. The DC-side filter is also required.

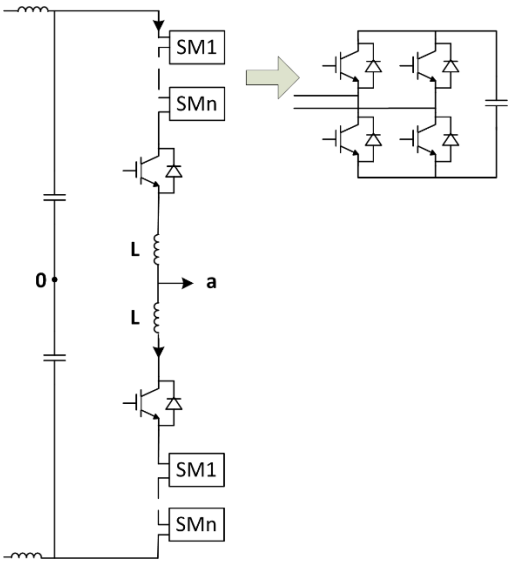


Figure 3.9 Topology of AAC

There are various other kinds of hybrid multilevel converter which are introduced and summarized in [64]. When choosing the optimum topology for a specific application, a trade-off between power density, cost, efficiency and functionality needs to be considered.

B. Benefits of MMC

In comparison with two-level converters and conventional multilevel converters, MMC possesses a number of attractive features.

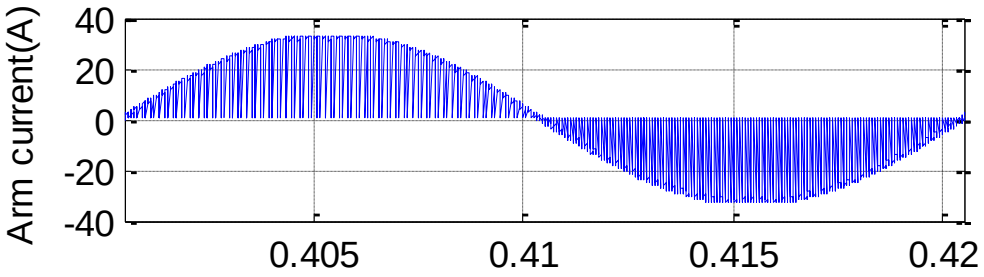
1) Low Slope di/dt of the Arm Currents

Because the existence of stray inductances, high slopes di/dt of the arm currents would cause unwanted electromagnetic interference (EMI) problems. As shown in Figure 3.10, the arm current waveforms of 2-level converter is discontinuous while it's continuous and has a much lower di/dt in MMC.

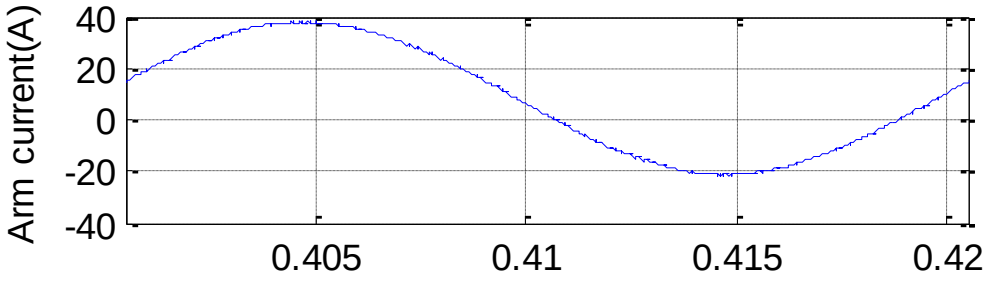
2) Low Voltage Stress on each Power Device

Two level converters suffer from high du/dt during switching. Voltage across the devices changes rapidly from zero to the full DC voltage in short switching periods. This can cause problems in parasitic capacitances in interface transformers, gate drive transformers etc. In MMC the voltage steps are much smaller as each device's

voltage is limited to the size of one sub-module, which in itself is only a fraction of the DC voltage. The potential for interference is much lower and stress on other system components is reduced.

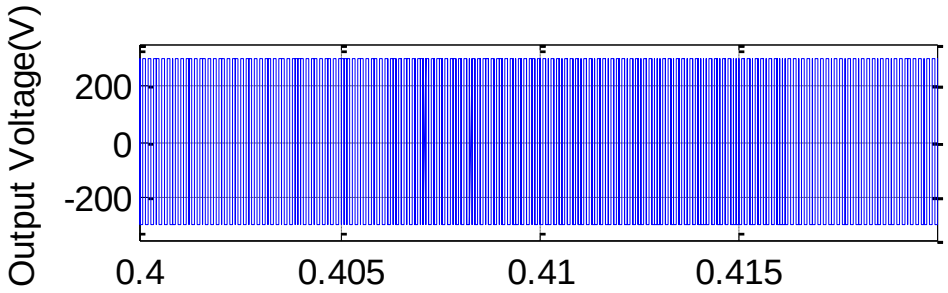


(a) Arm current of a 2-level converter

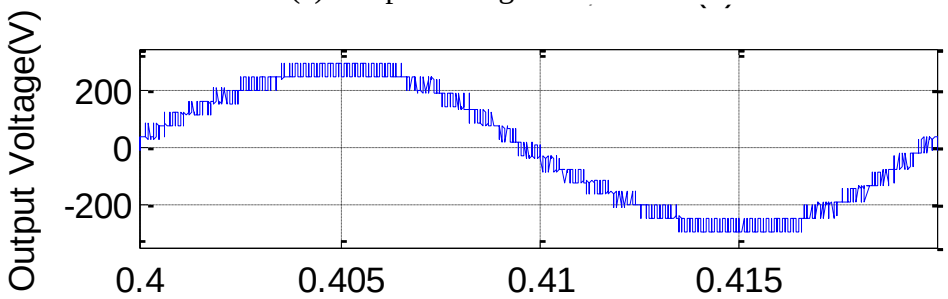


(b) Arm current of MMC

Figure 3.10 Arm currents waveform comparison (switching frequency 10 kHz)



(a) Output voltage of 2-level converter



(b) Output voltage of a 13-level MMC

Figure 3.11 AC output voltages waveform comparison (switching frequency 10 kHz)

As illustrated in Figure 3.11, when the input DC voltage is ±300 V, devices in 2-level converter will face 600 V, while it's only 50 V for devices in a 13-level MMC. Therefore, each power device sees a lower stress and lower du/dt is presented in MMC, which gives rise to a better EMC performance as well as low total harmonic distortion (THD).

3) Modular Construction

Within each module, the voltage level is clamped and may be set to a level compatible with each device's voltage rating. The identical modular provides scalability to different power and voltage levels. Redundant modules may be included to allow continued operation during failures by short-circuiting faulty sub-modules [58].

4) Distributed Energy Stored in Each Submodule Capacitor

No DC-link capacitors are required, which would otherwise result in extremely high surge currents under semiconductor and gating failures and DC faults [63, 69]. The elimination of DC-link capacitors also makes it feasible to control the DC-current directly, without intermediate passive filters [65].

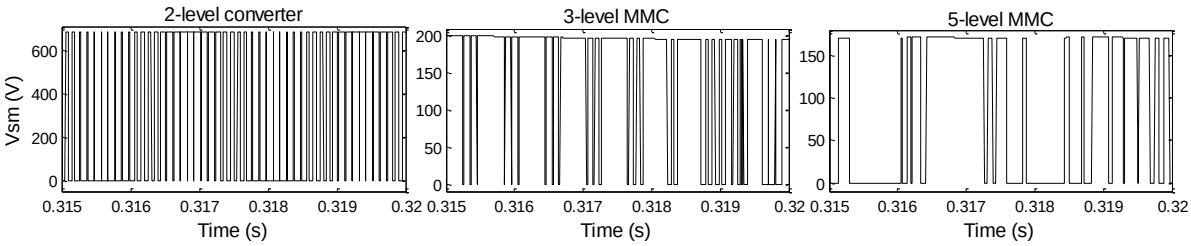
5) Smaller AC Filters

With increased voltage levels, harmonic filter size can be decreased or even eliminated, lending to a significant cost reduction.

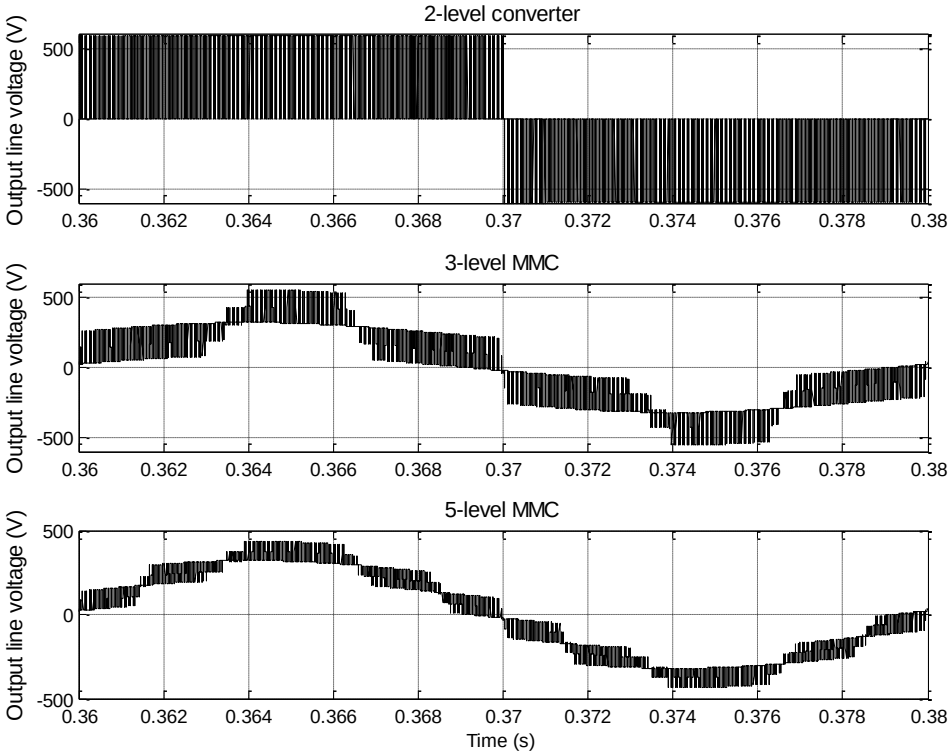
6) Low Switching Frequency and Switching Power Losses

The switching frequency of each power device is approximately 1/***n*** of the overall frequency of the converter, where '***n***' is the number of submodules per arm. In this way, the switching power loss is significantly reduced.

Figure 3.12 (a) demonstrates the simulated submodule voltage (U_{SM1} in Figure 3.5) waveforms for 2, 3 and 5-level MMC. It indicates that the switching frequency decreases significantly with the increased voltage level. The output line voltages of these three converters are presented in Figure 3.12 (b). THD analysis of the output waveforms are listed in Table 3.4, which show that the increased number of levels can bring improved THD at the output.



(a) Simulated submodule voltage waveforms



(b) Simulated output line voltage waveforms

Figure 3.12 Simulated waveforms for 2-level converter, 3- and 5-level MMC

Table 3.4 THD analysis of output voltage for 2-level converter, 3 and 5-level MMC (10 kW, 10 kHz, 600 Vdc / 240 Vac, 0.95 PF)

Converter Type	**THD V_{line_out}**
2-level Converter	111.70%
3-level MMC	31.53%
5-level MMC	16.05%

7) The Ability to Prevent Capacitor Discharging Current

There are two kinds of DC fault currents, the discharging currents from the DC side converter's capacitors and cable capacitance, and the AC networks contribution through converter's free-wheeling diodes [70, 71]. For customer-end converters in LVDC distribution system, there is no active source in the AC side. Hence when a DC fault occurs, only the capacitor discharging currents need to be blocked. Traditionally DC or AC circuit breakers are required to disconnect the converters, or the fault currents may damage the semiconductors and the converters [66]. However, all of the MMC topologies introduced in Section 3.2.2 A have the ability to block the capacitor discharging currents by simply turning off all of the switches [68]. During DC fault condition, the arm inductor serves as a protection choke to limit the fault current [60].

In conclusion, with all the benefits discussed, MMC has the potential to serve as high efficiency and high performance inverter for LVDC applications.

3.3 Fundamentals of MMC

The modulation techniques and operation principles of MMC will be further discussed in this section.

3.3.1 Modulation Techniques

Pulse width modulation (PWM) is one of the most widely utilized strategies for controlling the AC output of power electronic converters. It varies the duty cycle of the switches at a high switching frequency to achieve an average voltage or current of a low-frequency output [72]. It can be easily adopted by MMC applications. Space-vector modulation (SVM) scheme has also been applied to MMC [58]. Along with carrier-based PWM, both of these require high switching frequency. Therefore, they are suitable to low number of levels, and medium and low power applications [73]. Compared with carrier-based PWM, SVM is much more complicated to be implemented [74].

For high numbers of SMs, low switching frequency modulation schemes are desired to reduce switching losses. Reference [64] listed three low switching frequency schemes: selective harmonic elimination (SHE), nearest vector control (NVC) and nearest level control (NLC). SHE-based modulation requires numerical algorithms which consist of tables and interpolation. Therefore, SHE method is not suitable for high dynamic performance and limited to low-bandwidth or open-loop applications [73, 75, 76].

NVC was proposed in [77] to improve the dynamic performance of SHE, which approximates the reference value to the nearest vector in the α-β plane without the time average calculation of the reference. However, for multilevel converters with less than seven levels the NVC introduces high levels of low-order harmonic currents and voltage distortion [78]. Moreover, implementation of NVC is not straightforward due to the requirement for the numerical algorithm to locate the nearest vector [73]. In comparison with NVC, NLC is simpler to apply as finding the nearest level is much easier than finding the nearest vector. Therefore, NLC is regarded to be the most reasonable modulation methods for MMC with high number of levels [65, 76].

In summary, the multicarrier PWM is a good option for lower number of levels MMC, and NLC for high number of levels MMC. Both types of modulation techniques will be discussed in further details.

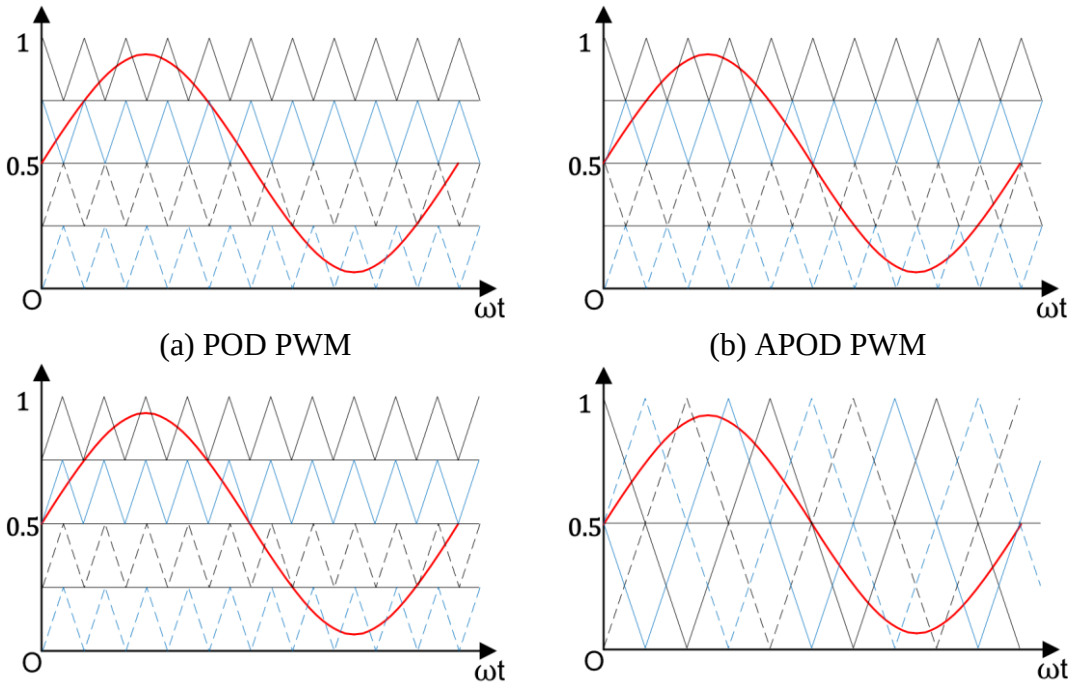
A. Multicarrier PWM

According to the number of levels and phase-angle difference, multicarrier PWM can be classified into two categories: level-shifted and phase-shifted PWM. For both schemes, an ***n+1*** level MMC requires ***n*** triangular carriers, with the same frequency and amplitude. A sinusoidal reference waveform (with triplen if desired) is compared to the carrier waveforms and the gate signal to each device is determined by the comparison results. If the modulating wave is greater than the carrier signal, then the corresponding switch is turned on. In the reverse situation, if the modulating wave is lower than the carrier signal, then the device corresponding to that carrier is switched off.

1) Level-shifted PWM

For an ***n+1*** level MMC, the ***n*** triangular carriers are disposed vertically with contiguous bands [55]. Figure 3.13 (a) – (b) shows the three different schemes of level-shifted PWM.

- Phase opposition disposition (POD): the upper half carrier waveforms are in phase, while they have a 180° phase shift with carriers in the lower half. In lower modulation indices, this scheme has a better harmonic performances compared to PD PWM [74].
- Alternative phase opposition disposition (APOD): Each carrier has a 180° phase shift with the contiguous carrier. This scheme is similar with POD, but with improved line voltage THD.
- Phase disposition (PD): All the carriers are in phase. Compared to other level-shifted PWM, it is generally accepted that this scheme leads to the lowest harmonic distortion under higher modulation index condition [74]. However, this modulation scheme is not feasible for separate voltage control of upper and lower arm which will be adopted in this application.



(a) POD PWM (b) APOD PWM

(c) PD PWM (d) PhS PWM

Figure 3.13 Multicarrier PWM for 5-level MMC

2) Phase-shifted (PhS) PWM

For the phase-shifted carrier strategy, each carrier waveform is shifted by Θ_{PhS} from the adjacent carrier. The shifted angle is given by (3-1)

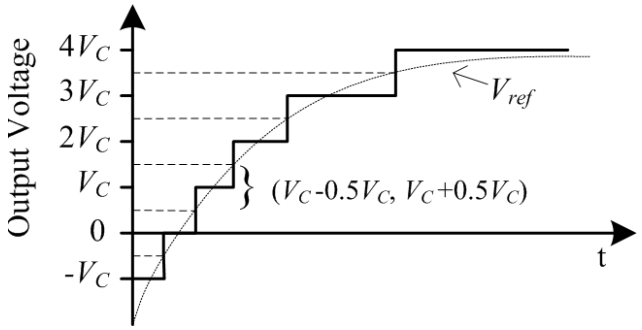
$$\theta_{PhS} = \frac{360^\circ}{n} \tag{3-1}$$

In comparison with other multicarrier PWM methods, research shows that PhS PWM results in the lowest distortion factors in the output voltage in the whole range of modulation indices [79].

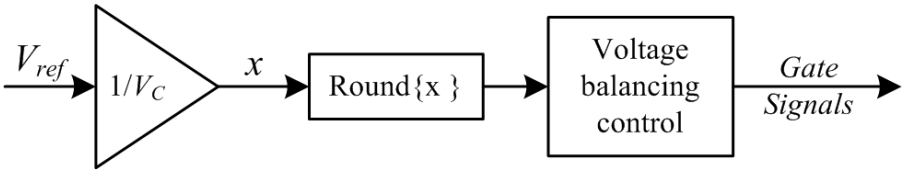
A main feature of PhS PWM is that it is capable of modulating each submodule independently [80]. Therefore, it can realize the individual voltage balancing control [81, 82].

B. Nearest Level Control (NLC)

The principle of NLC is to select the nearest level that the inverter can generate. The output voltage level is selected by comparing the reference voltage (V_{ref} in Figure 3.14) versus the nominal capacitor voltage (V_C). As illustrated in Figure 3.14 (b), x is the result of V_{ref} over V_C. The round function generates the closest integer to *x*. And *Round {x}* denotes the number of inserted submodules in one arm. For example, if V_{ref} is a value between (V_C *-0.5*V_C, V_C *+0.5*V_C), then *Round {x}* =1, which indicates one submodule in the arm will be inserted.



(a) Operating waveform illustration



(b) Control block of the NLC method

Figure 3.14 Operating principle of NLC

3.3.2 Capacitor Voltage Balancing Algorithm

Capacitor voltage imbalance can generate a common mode voltage, resulting in undesirable circulating currents. In order to keep the submodule capacitor voltages balanced, a balancing algorithm has to be implemented. In this section, two main algorithms are introduced. The first is the sorting algorithm and the second is based on the individual and average PI control.

A. Sorting Algorithm

The sorting algorithm was introduced in 2003 [58, 64], and is based on the level-shifted PWM. This method is easy to be implemented.

First all the submodule capacitor voltages and arm currents are measured. Then the capacitor voltages in each arm are sorted by the controller. When the arm current is positive, the submodules with lower voltage will be inserted so that their capacitors can be charged. During negative arm current the submodules with higher voltage will be inserted so that they can be discharged. Additionally, the stored energy between each arm should be kept equal.

B. Individual and Average PI control

Based on the phase-shifted PWM, the individual and average PI control for voltage balancing was introduced by [83] and [84]. The MMC circuit graph is presented in Figure 3.5.

This voltage balancing method includes two main control: average control and individual balancing control. An arm-balancing control can also be introduced to enable a stable operation under all the load conditions [81].

(1) The average control forces the average submodule capacitor voltage in one phase (v_{C_av}) to follow the command signal v_C*, as shown in Figure 3.15. The average submodule capacitor voltage can be obtained by using the sum of submodule capacitor voltages in one phase divided by *2n*, where *n* is the number of submodules in one arm. The average submodule capacitor voltage error is fed into a PI controller. The output is the command signal for the circulating current i_{diff}, which is defined by (3-2). The function of current minor loop is to control the circulating current i_{diff}.

(2) The individual balancing control (P controller) makes sure the each capacitor voltage follow the command signal v_C*. The polarity of the voltage demand generated from the individual balancing control depends on the arm current direction [83].

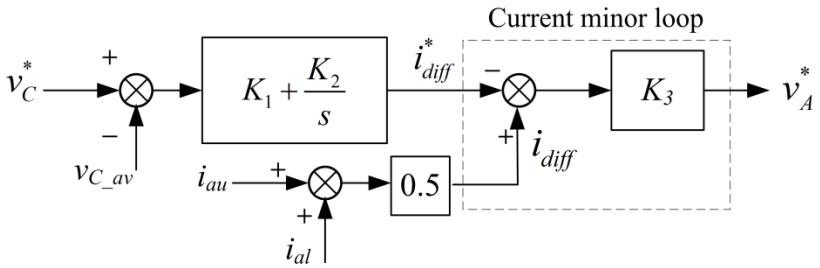


Figure 3.15 Average PI control for voltage balancing

$$i_{diff} = \frac{i_{au}+i_{al}}{2} \tag{3-2}$$

In this study, the sorting capacitor voltage balancing method is adopted because it is easy to be implemented. Accordingly, the level-shifted PWM is recommended since the number of levels is typically low for LVDC application. Both POD and APOD have symmetrical carrier waveforms besides the '*y=0.5*' line in Figure 3.13, which means both of them can provide separate voltage control of upper and lower arms. POD is used in this study due to the fact that it is easier to be programmed inside DSP.

3.4 Proposed Low Voltage Si MOSFET MMC

Established designs for a two-level converter operating at 600 Vdc input would require 1.2 kV IGBTs. The limiting factor of 2-level IGBT-based converter is that switching loss is relatively high and conduction loss is set by the threshold voltage and a resistive voltage drop [85].

Although Si MOSFET are available with voltage rated of 1.2 kV [86], these devices are limited by high on-state resistance (R_{on}) and poor body diode characteristics. This negates the benefits in switching frequency that might be gained from using Si MOSFETs instead of IGBTs.

There are 1.2 kV rated Silicon Carbide (SiC) MOSFETs available, which are promising since they can achieve low R_{on}. The body diodes of SiC MOSFETs also have ultralow reverse recovery loss. However, the fast switching necessary for high switching frequency may bring EMC issues.

The challenge is to provide a high efficiency DC-AC interface that can supply the necessary power quality without large output filters. Increasing switching frequency can improve THD and reduce filter size for two level converters. However, increased switching frequency means higher power losses. MMC provides a method that decoupling switching frequency from power quality.

The modular structure of MMC clamps the submodule voltage to a lower value, which enable the use of low voltage rating Si MOSFET. The benefits of adopting low voltage MOSFETs are discussed in this section. Experimental results will be presented to back up the theory.

3.4.1 Benefits of MOSFET MMC

1) MOSFET Low On-State Resistance

Although the MMC has more semiconductor devices than a conventional 2-level IGBT-based converter, the modular structure of MMC enables the use of lower rated MOSFETs which have much lower on-state resistance.

2) Synchronous Rectification

The MOSFET has a lower on-state voltage drop than its body diode. As shown in Figure 3.16 (a) when S_U=1, S_L=0, and Figure 3.16 (b) when S_U=0, S_L=1, the MOSFET is controlled to operate in the third quadrant, thereby reducing power losses [87, 88]. The diodes only conduct during dead times, i.e. where S_U=0, S_L=0.

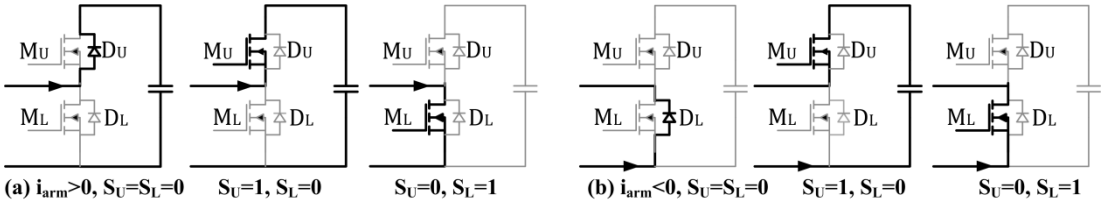


Figure 3.16 Current paths in one MOSFET-based MMC submodule (S_U=upper switch, S_L=lower switch and 0/1=off/on)

3) Parallel-connected MOSFETs

The positive temperature coefficient exhibited by MOSFETs facilitates their parallel connection. The low submodule switching frequency, a product of the MMC, reduces the importance of dynamic current loading and allows parallel-connected MOSFETs to share currents equally. Parallel connection further reduces conduction losses, which helps to reduce the size of heat sink.

In comparison, the current sharing for IGBTs is a problem, particularly when the switching frequency is relatively high for a 2-level converter. Also, the parallel connection of IGBT will not significantly reduce the conduction loss due to the existence of saturation voltage at zero current.

3.4.2 Parallel Connection of MOSFETs

The paralleling connection of MOSFETs reduces conduction losses significantly. The switching losses, however, will remain the same or even increase due to the slight unbalanced current sharing between the paralleled switches.

In this section, the feasibility and current sharing of MOSFETs in parallel connection are investigated. Factors that affect parallel-connection of MOSFETs are discussed,

which include four major parts: circuit layout, gate circuitry, current and temperature unbalance. Gate resistance will influence the dynamic performance of current sharing. Therefore, different gate resistances are tested in this study.

With the increased number of paralleled devices, the parasitic track resistance (R_{DSi} in Figure 3.18) becomes significant [89]. The study performed in [90] concludes that an MMC with four Si MOSFETs in parallel is a suitable choice for LVDC applications. Therefore, one submodule with four parallel-connected MOSFETs measured using a Rogowski coil under 0.5 duty cycle, 3 kHz switching frequency and 16 A load current is investigated in this section.

A. Layout Considerations

Non-symmetrical layouts will lead to the current imbalance at switching transients, resulting in unbalanced switching losses [91]. The circuit layout used in this study is shown in Figure 3.17, where a small 2-layer PCB symmetrically connects the four MOSFETs. On the top layer lies the drain connection, while on the bottom layer is the gate and source connections.

According to KVL, the paralleled switches should share the same voltage. Under switching transient, however, the individual stray inductance (L_{Di} and L_{Si} in Figure 3.18) can lead to the unequal drain-source voltages. The di/dt at switching transients will generate a voltage across L_{Si}. This voltage will counteract the applied gate voltage and leads to the unbalance of the source currents [91, 92]. Therefore, the main circuit design consideration is to match the individual stray inductances, which requires a symmetrical layout of the drain connection and source connections. The gate connections are not designed symmetrically due to the space limitation of a 2-layer PCB board. However, the same connection track lengths are guaranteed. Also, the relatively low switching frequency for each submodule in MMC ensures that it is not a problem for current sharing.

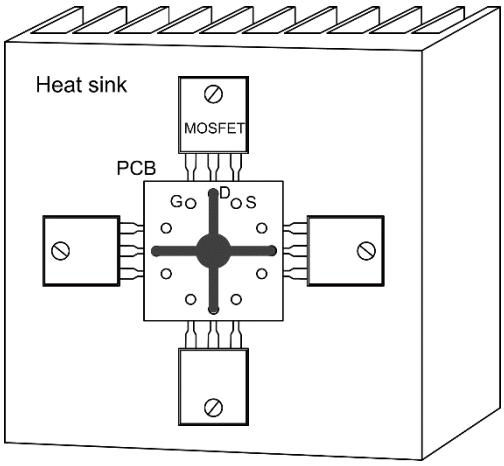


Figure 3.17 Layout of four parallel-connected MOSFETs

Keeping the junction temperature (T_j) difference minimal allows all the parallel-connected MOSFETs to be operated around the maximum T_j and hence provides a minimum value of total resistance. To achieve this, the MOSFETs should be closely thermally coupled, which means they should be mounted on the same heat sink [91].

B. Gate Oscillations

There is a common low impedance path among parallel-connected MOSFETs, which tends to cause parasitic self-oscillations [91, 92]. Hence, a small gate resistance (R_{Gi}) is required for individual MOSFETs to provide gate decoupling and damping. The additional gate resistance will slow down the turn-on speed. The EMC issue, however, will be improved with a large R_{Gi}.

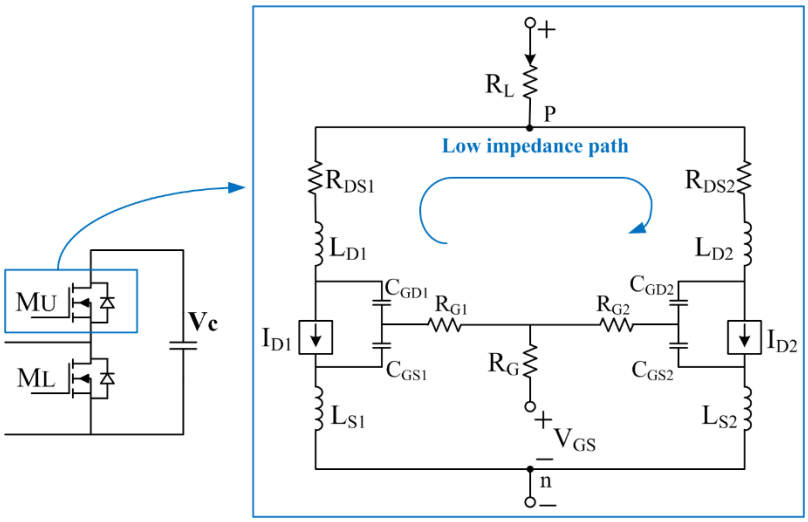


Figure 3.18 Parallel-connection of 2 MOSFETs in a submodule

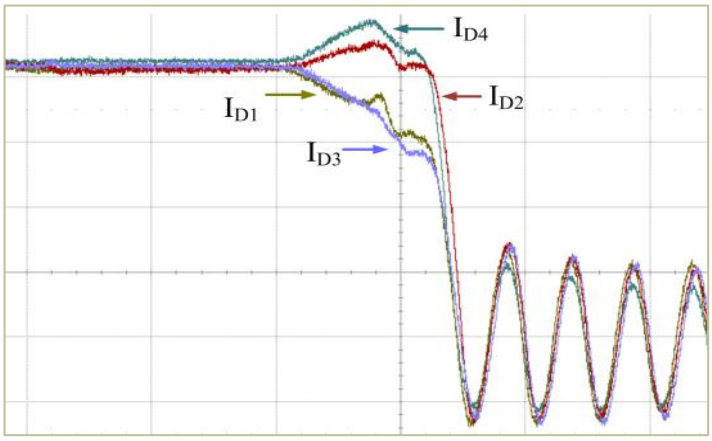
C. Current Sharing

As previously indicated in [89], a gate drive with a reduced speed can be employed to address EMC concerns in Si MOSFET-based MMC. Therefore, in this section dynamic sharing was tested under normal (R_{Gi} = 1 Ω) and slowed (R_{Gi} = 100 Ω) switching.

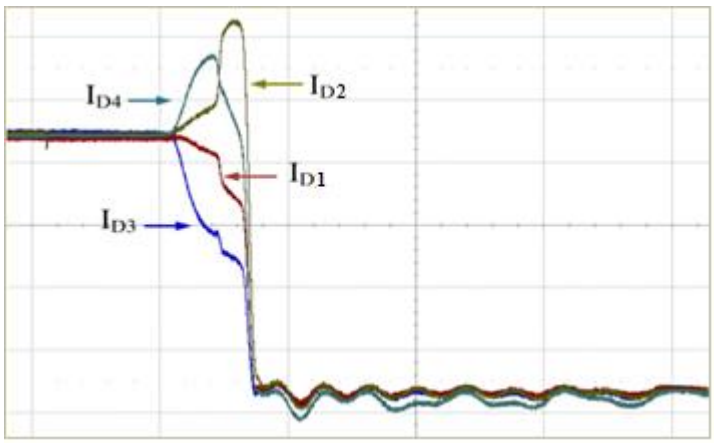
1) Dynamic Sharing at Turn-off Transient

Figure 3.19 shows with larger gate resistances, oscillation at turn-off are significantly attenuated, reducing electromagnetic emissions. With slowed switching, however, dynamic current unbalance is enlarged at turn-off (Figure 3.19) due to the increase in *R-C* time constant (gate resistance and miller capacitors).

Because of relatively low submodule switching frequency, dynamic unbalance between the four parallel-connected MOSFETs has no appreciable effect on either the overall or individual device loss. It is also not sufficient to exceed pulse power rating of any individual device.



(a) With R_{Gi} = 1 Ω, i = 1-4 [current: 1 A/div, time: 200 ns/div]



(b) With R_{Gi} = 100 Ω, i = 1-4 [current: 1 A/div, time: 2 μs/div]

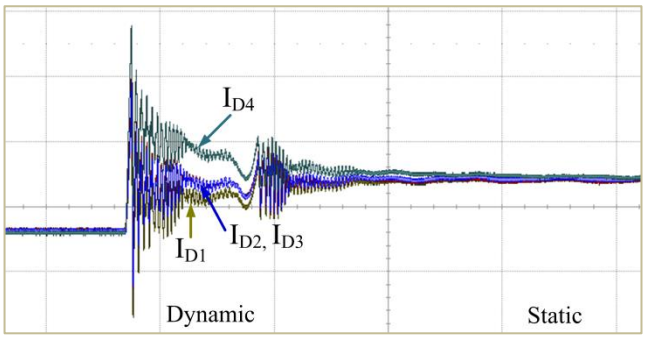
Figure 3.19 Experimental results of current sharing between four paralleled MOSFETs at turn-off

2) Dynamic Sharing at Turn-on Transient

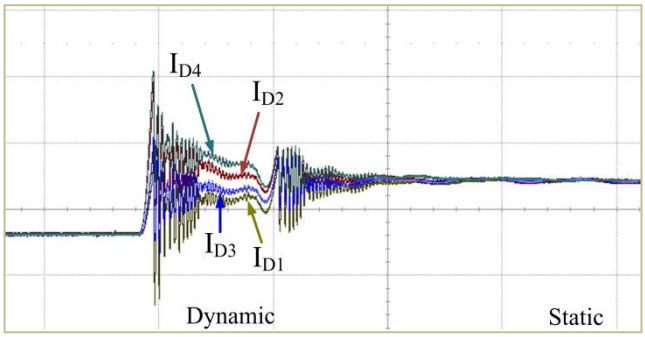
The difference of individual device transconductances and threshold voltages gives rise to varying switching rates as shown in Figure 3.20. With the lowest threshold voltage, MOSFET4 turns on first. The Miller effect of MOSFET4 then lowers the rate of rise in the drive voltage applied on the other 3 devices. At turn-on transient, MOSFET4 takes a slight larger current than other MOSFETs. The large current overshoot is due to reverse recovery of the intrinsic diode.

There is no significant difference in the overshoot at turn-on for different gate resistance. The parasitic oscillations and dynamic current unbalance are similar in Figure 3.20 (a) and (b).

They are also caused by the collective effects of the gate and drain resistances ($R_{G,}$ R_{DS} in Figure 3.18), the source and drain inductances (L_S, L_D in Figure 3.18), the drain-source capacitance and the gate-source capacitance (C_{GS} in Figure 3.18) [91, 92]. With so many components affecting switching performance, it is concluded in [91] that matching MOSFET switching transients is practically impossible. However, the correct selection of passive components and design layout can reduce the imbalances between devices.



(a) With R_{Gi} = 1 Ω, i = 1-4 [current: 5 A/div, time: 2 µs/div]



(b) With R_{Gi} = 100 Ω, i = 1-4 [current: 5 A/div, time: 2 µs/div]

Figure 3.20 Experimental results of current sharing between four paralleled MOSFETs at turn-on

3) Static Current Sharing

The major cause of static junction temperature difference and current unbalance is R_{on} mismatch. Figure 3.20 shows the experimental results of current sharing between four MOSFETs. R_{on} increases with junction temperature due to the reduction in carrier mobility [93]. This will lead to an automatic equal current sharing between parallel-connected devices. The results show that the four MOSFETs share current well during the static state (Figure 3.20).

3.5 Summary

In this chapter, two-level VSI and commonly used multilevel converters are presented. The two-level VSI is the easiest to be implemented. However, it suffers from high di/dt and high voltage stress on each semiconductor devices. Also high switching frequency and bulky filters are required to provide a better waveform quality. While at the same time, it introduces high switching loss and EMI issues. The limits of using flying capacitor converter are the complexity of the circuit

topology and the large number of capacitors required. Additional inverter control may be required to ensure that the neutral point remains balanced for NPC. The power losses are not equally distributed in NPC, which lead to the fact that the rating current is limited by the power loss in the most stressed semiconductor device.

MMC is a promising topology since it has many benefits (Section 3.2.2) such as continuous arm currents, a reduced *du/dt*, modular construction, no need of an input filter, allowing the use of smaller AC filters, low switching losses, better output waveform quality and the ability to block DC faults. MMC also provides redundancy for failure management. The modular structure of MMC allows lower voltage devices to be used. MOSFETs may be used in place of IGBTs and the R_{dson} may be reduced through parallel connection. The synchronous rectification of MOSFETs further reduces conduction loss.

Then different submodule structures of MMC were analysed. HBSM is the simplest, benefiting from the lowest power losses and cost but cannot block the AC-side reverse current. FBSM is able to block DC fault current, however the cost and power losses are the highest. CDSM possesses the ability to block DC fault without a significant increase in power losses and cost.

Three hybrid multilevel converter topologies with fault blocking capability were introduced. The hybrid MMC increases the complexity of control submodule capacitor voltage balancing. The AAC topology requires a DC side filter and series connection of devices can prove challenging. The series connected devices of the 2-level and hybrid 2-level converter suffer high voltage stress and the DC side capacitor can lead to a high inrush current.

The modulation techniques are analysed in Section 3.3. For small number of levels MMC, multicarrier PWM can provide an improved waveform quality and a reduction in harmonics, at the expense of increased losses. For high number of levels NLC is more suitable due to its simplicity and improved performance. Level-shifted PWM with sorting voltage balancing algorithm is easier to adopt and is therefore selected for this study.

Due to the fact that the paralleling connection of MOSFETs can significantly reduce the conduction losses of MMC, Section 3.4.2 investigated the issues related to MOSFETs parallel-connection. The track resistance and the difference of individual switches may give rise to the unbalance of current sharing in static status. However, the positive temperature coefficient of MOSFETs results in convergence in sharing between the devices. Experimental results demonstrated that the static currents are well balanced between four parallel-connected MOSFETs. The circuit layout, stray inductances and parasitic capacitances result in dynamic imbalance. Due to the relatively low switching frequency of MMC, the dynamic current sharing is not a major problem.

In summary, the MMC with parallel connected MOSFETs is a potential and feasible topology for low-voltage application.

4. Converter Design of MOSFET MMC

4.1 Introduction

In Chapter 3, the benefits of MOSFET-based MMC for low voltage application were discussed. The converter design of MOSFET-based MMC will be presented in this chapter. Capacitor sizing and arm inductor sizing methods are introduced to meet the submodule capacitor voltage and circulating current requirements. Since typically a reduced voltage levels of MMC is needed for low voltage applications, a small AC output filter would be required to maintain the output waveform quality. In Section 4.5, the filter design is presented and discussed.

A circulating current will be drawn from the DC side in single-phase MMC, which will introduce power losses in both the DC transmission network and power devices. Increased power losses might damage the power devices. Circulating current suppression control schemes is then introduced and validated with both simulation and experimental results. In addition, closed-loop voltage regulation to stabilise the output voltage when the load changes is designed in Section 4.6.3.

4.2 Steady State Mathematical Analysis

In this section a mathematical analysis of the MMC is performed. Figure 3.5 and Figure 4.1 show the topology and average model of a single phase MMC. In each arm, R represents the parasitic ohmic losses, which mainly generated by the power semiconductor devices [94, 95].

In this analysis the following assumptions are used.

1. Assume that current suppression control eliminates all harmonics and remaining the circulating current (i_{diff}) only has a DC component I_{dc}.
2. All the capacitors and switches are identical.
3. Submodule capacitor voltages are assumed to be instantaneously balanced.

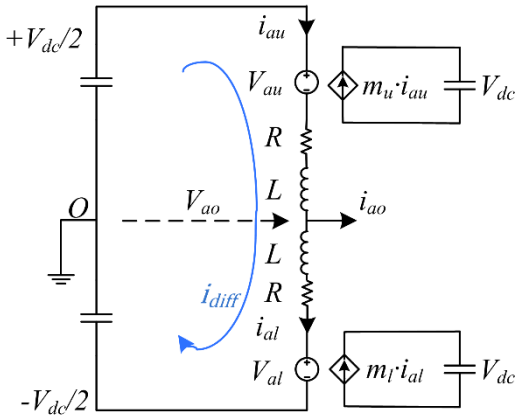


Figure 4.1 Average model of MMC

As shown in Figure 4.1, the cumulative upper and lower arm voltages of series connected submodules are V_{au} and V_{al} respectively and i_{au} and i_{al} stand for upper and lower arm currents. The output voltage V_{ao} and current i_{ao} are assumed sinusoidal with lagging phase angle φ and given by (4-1) and (4-2), where M is the modulation index.

$$V_{ao} = M \cdot \sin \omega t \cdot \frac{V_{dc}}{2} \tag{4-1}$$

$$i_{ao} = I_{ao} \sin(\omega t - \varphi) \tag{4-2}$$

According to [96] and Assumption 1, the arm currents can be expressed as (4-3) and (4-4), where I_{dc} is the DC component of i_{diff}.

$$i_{au} = i_{diff} + \frac{i_{ao}}{2} = I_{dc} + \frac{i_{ao}}{2} \tag{4-3}$$

$$i_{al} = i_{diff} - \frac{i_{ao}}{2} = I_{dc} - \frac{i_{ao}}{2} \tag{4-4}$$

The switching action is described by m_u and m_l, which represents on average, how many submodules are connected in the upper and lower arm respectively. The definitions of m_u and m_l are given by (4-5) and (4-6).

$$m_u = \frac{1}{2} - \frac{1}{2} M \cdot \sin \omega t \tag{4-5}$$

$$m_l = \frac{1}{2} + \frac{1}{2} M \cdot \sin \omega t \tag{4-6}$$

In the average model, the capacitor current in each submodule can be estimated by the production of switching action and arm currents i_{au}, i_{al}. The capacitor currents in upper and lower arm (i_{cu} and i_{cl}) are given by (4-7) and (4-8).

$$i_{cu}(t) = i_{au} \cdot m_u = (I_{dc} + \frac{I_{ao}}{2}\sin(\omega t - \varphi)) \cdot \left(\frac{1}{2} - \frac{1}{2}M \cdot \sin \omega t\right) \quad (4\text{-}7)$$

$$i_{cl}(t) = i_{al} \cdot m_l = (I_{dc} - \frac{I_{ao}}{2}\sin(\omega t - \varphi)) \cdot \left(\frac{1}{2} + \frac{1}{2}M \cdot \sin \omega t\right) \quad (4\text{-}8)$$

By solving (4-7), (4-9) can be obtained, which shows that i_{cu} can be expanded to DC, fundamental and second harmonics of the grid frequency.

$$i_{cu}(t) = \frac{1}{2}\left(I_{dc} - \frac{\mathrm{M}}{4}I_{ao}\cos\varphi\right) - \left[\frac{M}{2}I_{dc} \cdot \sin \omega t - \frac{1}{4}I_{ao}\sin(\omega t - \varphi)\right] + \frac{\mathrm{M}}{8}I_{ao}\cos(2\omega t + \varphi) \quad (4\text{-}9)$$

Similarly, i_{cl} can be expressed by (4-10).

$$i_{cl}(t) = \frac{1}{2}\left(I_{dc} - \frac{M}{4}I_{ao}cos\varphi\right) + \left[\frac{M}{2}I_{dc} \cdot sin\omega t - \frac{1}{4}I_{ao}\sin(\omega t - \varphi)\right] + \frac{M}{8}I_{ao}\cos(2\omega t + \varphi) \quad (4\text{-}10)$$

Under steady state, the DC component of the capacitor current should be zero, which reflects the power balance between the AC-side and the DC-link [94]. Therefore the relationship between input DC current and output current can be presented in (4-11).

$$I_{dc} = \frac{1}{4}I_{ao}M\cos\varphi \quad (4\text{-}11)$$

4.3 Submodule Capacitor Sizing

MMC relies on charged submodule capacitors to build up the output AC voltage. Due to the bulky size and large numbers of the capacitors, the capacitances should be minimised, whilst maintaining the voltage fluctuation within ±10% of the nominal value limit [97].

The submodule capacitor is sized based on its maximum energy deviation in this section. The symbols used in the analysis are defined as follows: V_C the average submodule capacitor voltage; V_{C_nom} represent the nominal submodule capacitor voltage and ΔV_{max} the maximum voltage difference in p.u.

4.3.1 For Single-phase MMC

The average model (Figure 4.1) is used for analysis in this section, considering with 2-phase-leg topology. Level-shifted SPWM modulation, specifically phase opposition disposition (POD), is exploited to generate a sinusoidal output waveform. The upper and lower arm voltage can be expressed as (4-12) and (4-13) respectively.

$$V_{au} = m_u \cdot V_{dc} = \left(\frac{1}{2} - \frac{1}{2}M \cdot \sin \omega t\right) \cdot V_{dc} \tag{4-12}$$

$$V_{al} = m_l \cdot V_{dc} = \left(\frac{1}{2} + \frac{1}{2}M \cdot \sin \omega t\right) \cdot V_{dc} \tag{4-13}$$

The average energy stored in one arm is given by (4-14).

$$E_{arm} = \frac{n}{2} \cdot C_{sub} \cdot {V_C}^2 \tag{4-14}$$

The peak to peak energy deviation can be expressed as (4-15) [97].

$$\Delta E_{arm} = \frac{n}{2} \cdot C_{sub} \cdot \left[V_{C\_nom}(1 + \Delta V_{max})\right]^2 - \frac{n}{2} \cdot C_{sub} \cdot [V_{C\_nom}(1 - \Delta V_{max})]^2 \tag{4-15}$$

Therefore, the minimal submodule capacitance can be derived as (4-16).

$$C_{sub} = \frac{\Delta E_{arm}}{2n \cdot {V_{C\_nom}}^2 \cdot \Delta V_{max}} = \frac{n \cdot \Delta E_{arm}}{2{V_{dc}}^2 \cdot \Delta V_{max}} \tag{4-16}$$

The energy deviation can be obtained from the power transfer capacity and AC and DC side voltages [98].

The apparent power can be expressed as (4-17). Two times I_{dc} is because there are two phase legs and I_{dc} indicates the DC component in the circulating current in one phase leg.

$$|\bar{S}| = \frac{P}{\cos \varphi} = \frac{V_{dc} \cdot 2I_{dc}}{\cos \varphi} \tag{4-17}$$

The instantaneous power flowed in to the upper arm can be calculated by combining (4-12), (4-3) and (4-17) (Figure 4.2), which is given by (4-18).

$$\begin{aligned} p_{arm\_up}(t) &= V_{a1}(t) \cdot i_{au}(t) = \left[\frac{1}{2}V_{dc} - V_{ao}(t)\right] \cdot \left[I_{dc} + \frac{1}{2}i_{ao}(\mathrm{t})\right] \\ &= |\bar{S}| \frac{1}{4M}(1 - M \sin \omega t) \cdot [M \cos \varphi + 2 \sin(\omega t - \varphi)] \end{aligned} \tag{4-18}$$

Energy stored in one arm (Figure 4.3) can be obtained from integrating the power with respect to time. The peak to peak energy variation can be calculated from the integration of $P_{arm\_up}(t)$ between *t1* and *t2*, where *t1* and *t2* are the zero crossing points of P_{arm_up}. The symbolic solution for ΔE_{arm} is given by (4-21). Its non-linear part can be defined as normalised peak to peak energy variation k_E which is scaled by the power and frequency, as shown in (4-22).

$$t1 = \frac{1}{\omega}[\varphi - \sin^{-1}(0.5M\cos\varphi)] \tag{4-19}$$

$$t2 = \frac{1}{\omega}[\pi + \varphi + \sin^{-1}(0.5M\cos\varphi)] \tag{4-20}$$

$$\Delta E_{arm} = \int_{t1}^{t2} P_{arm_{up}}(t)\,dt = \frac{|\bar{S}|}{\omega}\cdot\frac{1}{M}\left(1-\frac{1}{4}M^2\cos^2\varphi\right)^{1.5} \tag{4-21}$$

$$k_E = \frac{1}{M}\left(1-\frac{1}{4}M^2\cos^2\varphi\right)^{1.5} \tag{4-22}$$

From (4-21), the maximum ΔE_{arm} occurs when $\cos\varphi$=0, when real power is zero. Also, lower *M* would lead to a higher energy deviation.

$$\Delta E_{arm\_max} = \frac{|\bar{S}|}{\omega}\cdot\frac{1}{M} \tag{4-23}$$

Therefore, the minimum cell capacitance required for single-phase MMC is given by

$$C_{sub} = \frac{n\cdot|\bar{S}|}{2\omega\cdot M\cdot {V_{dc}}^2\cdot\Delta V_{max}} \tag{4-24}$$

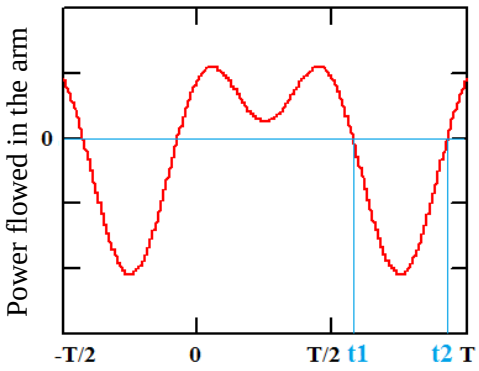


Figure 4.2 Power flow through the arm

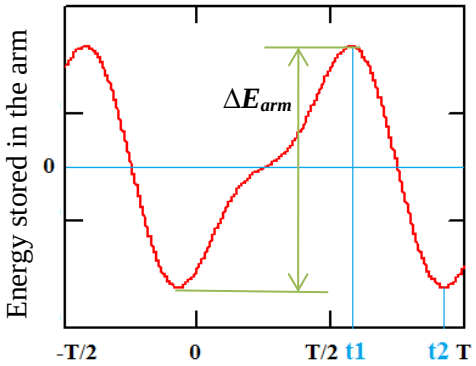


Figure 4.3 Energy stored in the arm

Case Study: when peak magnitude of output voltage $\hat{V}_a$ equals to $0.5V_{dc}$

In this study, the effects of *M* and phase angle φ on the submodule capacitor sizing are investigated to ensure the capacitor voltage remain within the distortion limit at any load condition.

The AC voltage magnitude (V_{ao}) varies between 0.9 – 1.1 times its nominal voltage $\hat{V}_{a\_nom}$, which meets the ±10% fluctuation requirement regulated by network operators [99]. Peak magnitude ($\hat{V}_a$) must remain less than $0.5V_{dc}$ (when M=1) as the arm is unable to generate negative voltage. Assuming the maximum magnitude of AC peak voltage is $0.5V_{dc}$, (4-25) can be obtained.

$$1.1 \cdot \hat{V}_{a_{nom}} = 1.1 \cdot M_{nom} \cdot \frac{V_{dc}}{2} = \frac{V_{dc}}{2} \tag{4-25}$$

The nominal and minimal modulation indexes M_{nom} and M_{min} can be obtained by (4-26) and (4-27) respectively.

$$\hat{V}_{a_{nom}} = M_{nom} \cdot \frac{V_{dc}}{2} \tag{4-26}$$

$$M_{min} \cdot \frac{V_{dc}}{2} = 0.9 \cdot \hat{V}_{a_{nom}} = 0.9 \cdot M_{nom} \cdot \frac{V_{dc}}{2} \tag{4-27}$$

Therefore,

$$M_{nom} = \frac{1}{1.1} = 0.91 \tag{4-28}$$

$$M_{min} = \frac{0.9}{1.1} = 0.82 \tag{4-29}$$

Figure 4.4 shows that the energy deviation reaches the maximum $1.22\frac{|\bar{S}|}{\omega}$ when M=0.82 and φ=90°C (reactive power only). Therefore, by substituting ΔE_{arm} with $1.22\frac{|\bar{S}|}{\omega}$ in (4-16), the submodule capacitance can be sized by (4-30). It shows that submodule capacitance will increase with the number of levels of MMC.

$$C_{sub} = \frac{1.22 \cdot n \cdot |\bar{S}|}{2\omega \cdot {V_{dc}}^2 \cdot \Delta V_{max}} \tag{4-30}$$

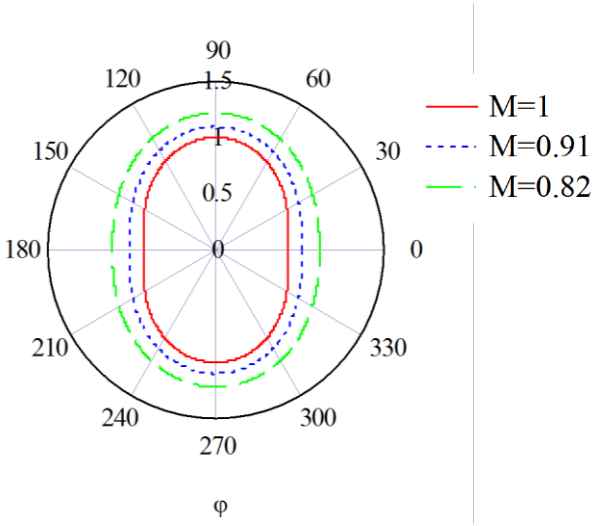


Figure 4.4 Normalised energy deviation k_E for different M

4.3.2 For Three-phase MMC

For three-phase MMC, the calculations are the same, while the apparent power is different.

$$|\bar{S}| = \frac{P}{\cos\varphi} = \frac{V_{dc} \cdot 3I_{dc}}{\cos\varphi} \tag{4-31}$$

Similar with single-MMC, the instantaneous power flowed in to the upper arm can be given by (4-32).

$$P_{arm\_up}(t) = |\bar{S}|\frac{1}{6M}(1 - M\sin\omega t) \cdot [M\cos\varphi + 2\sin(\omega t - \varphi)] \tag{4-32}$$

The maximum peak to peak energy variation ΔE_{arm_max} can be expressed as (4-33).

$$\Delta E_{arm\_max} = \frac{2|\bar{S}|}{3\omega} \cdot \frac{1}{M} \tag{4-33}$$

Therefore, combining (4-33) and (4-16), the submodule capacitance can be derived as (4-34).

$$C_{sub} = \frac{n \cdot |\bar{S}|}{3\omega \cdot M \cdot {V_{dc}}^2 \cdot \Delta V_{max}} \tag{4-34}$$

Simulation results of capacitor voltages for a single-phase 5-level MMC

According to the capacitor sizing calculation, (4-24), the required capacitor for 5-level 2-phase-leg 10 kW 600 Vdc / 240 Vac MMC is 3.18 mF. Therefore 3.3 mF capacitor is chosen due to the market availabilities The Matlab simulation shows that the 8 submodule capacitor voltages in one phase leg are well balanced (Figure 4.5), and the voltage ripple is ±7.5%, which is within the ±10% distortion limit.

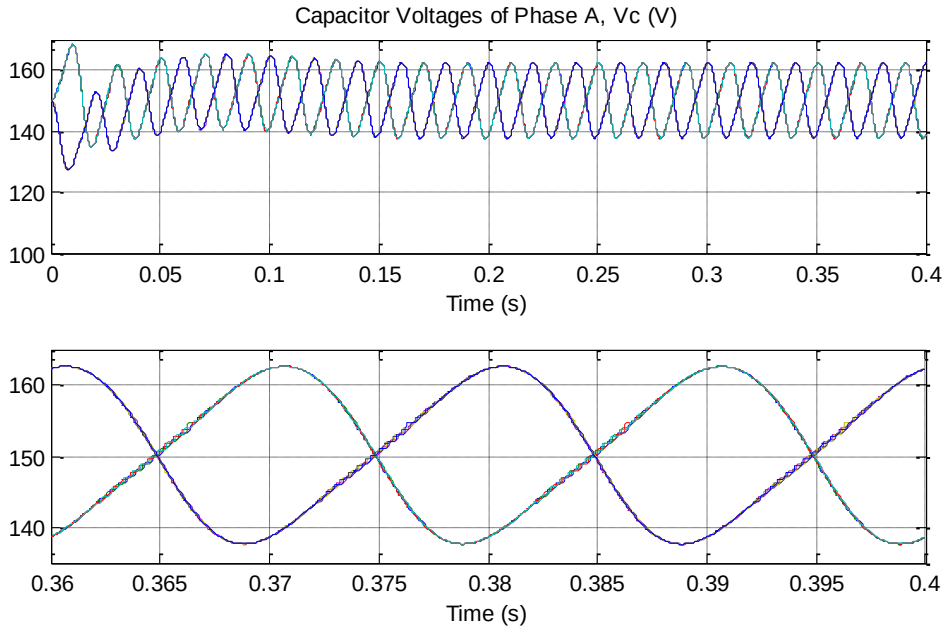


Figure 4.5 Capacitor voltages of 4 submodules per arm in a 5-level 2-phase-leg MMC with 3.3 mF submodule capacitance

4.4 Arm Inductor Sizing

In MMC, arm inductors are placed in series with submodules in each arm. The function of arm inductors is to limit the circulating current which results from the voltage difference between the DC side voltage and the voltage in one phase leg. In some applications such as HVDC system, arm inductor is also a key component to limit the DC fault current [78]. While in this study, the main consideration is the circulating current constraint.

The current suppression control can effectively reduce the 2nd harmonic distortion, which will be introduced in Section 4.6.2. For circulating currents at switching frequency, however, it can only be suppressed by the arm inductors, because the high switching frequency is out of the controller's bandwidth [100]. As a result, the arm inductor is sized in order to limit switching frequency circulating current.

In this section, the arm currents are assumed to consist of only DC and fundamental components, as indicated in (4-3) and (4-4). The voltage difference between phase leg and the DC voltage gives rise to the circulating current. According to [94], the voltage difference u_{diff} can be given by (4-35). Its maximum value can be derived as (4-36) accordingly.

$$\begin{aligned} u_{diff} &= \frac{V_{dc}-(v_{au}+v_{al})}{2} \\ &= \frac{n}{8C_{sub}}\left\{-\frac{3}{4\omega}M \cdot I_{ac} \cdot \sin(2\omega t-\varphi)+\frac{1}{\omega}M^2 I_{dc} \cdot \sin(2\omega t)\right\} \end{aligned} \tag{4-35}$$

$$u_{diff\_max} = \frac{n \cdot I_{dc}}{8\omega C_{sub}} \cdot \sqrt{(M^2-3)^2+9\tan^2\varphi} \cdot \sin(2\omega t-\theta) \tag{4-36}$$

where $\theta = \tan^{-1}(\frac{3\tan\varphi}{M^2-3})$.

$$u_{diff\_max} = \frac{n \cdot I_{dc}}{8\omega C_{sub}} \cdot \sqrt{(M^2-3)^2+9\tan^2\varphi} \tag{4-37}$$

The peak to peak value of the circulating current at the switching frequency can be given by (4-38).

$$I_{pp} = \frac{u_{diff}}{L_{arm}} \cdot \Delta T \tag{4-38}$$

Since the largest ΔT would be T_S, the largest I_{pp} can be expressed as (4-39).

$$I_{pp\_max} = \frac{u_{diff\_max}}{L_{arm}} \cdot T_S = \frac{n \cdot I_{dc} \cdot T_S}{8\omega L_{arm} C_{sub}} \cdot \sqrt{(M^2-3)^2+9\tan^2\varphi} \tag{4-39}$$

At the time of writing, there is no specific limitation about the DC side current distortion. However, in this study I_{pp_max} is limited into 5% of DC side current I_{dc}.

$$I_{pp\_max} = 5\% \cdot I_{dc} = 5\% \cdot 2I_{dc} = 0.1I_{dc} \tag{4-40}$$

Given this, the arm inductor's minimum size should be:

$$L_{arm} = \frac{5n}{4\omega C_{sub} f_s} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2\varphi} \tag{4-41}$$

Therefore, when *M=1, φ=0,* the smallest arm inductance is given by (4-42), which is inverse proportional to the switching frequency.

$$L_{arm} = \frac{5n}{2\omega C_{sub} f_s} \tag{4-42}$$

By substituting (4-24) into (4-42), it can be concluded that the arm inductance is not affected by the number of levels.

$$L_{arm} = \frac{5 \cdot M \cdot {V_{dc}}^2 \cdot \Delta V_{max}}{f_s \cdot |\bar{S}|} \tag{4-43}$$

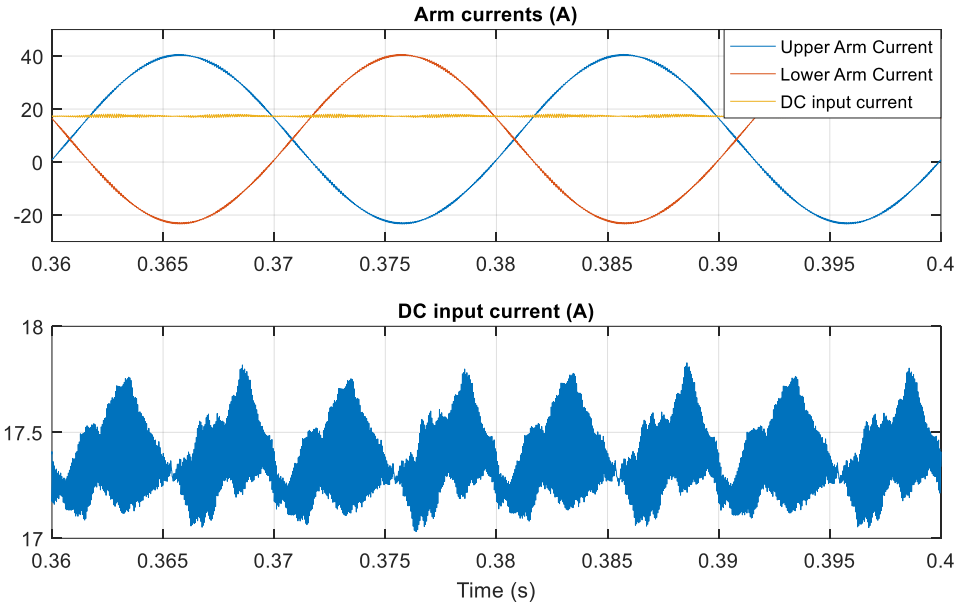


Figure 4.6 Simulation results of arm currents and circulating current of 2-phase-leg 5-level MMC (V_{dc}=600 V, V_{out}=240 V, 10 kW, L_{arm}=1.5 mH)

By using (4-41), 1.5 mH arm inductance is required for 10 kW 2-phase-leg 5-level MMC with 600 Vdc and 240 Vac. The MATLAB simulation results of arm currents and DC input current is presented in Figure 4.6. It shows that the DC current ripple is 4.7% which meets the current limitation.

4.5 Output Filter Design of MMC

For high voltage application, usually MMC is composed of hundreds of submodules. The output waveform is nearly sinusoidal and a filter is generally not required. For LVDC applications, however, the number of levels tends to be lower, due to the increased cost and complexity. As shown in Table 4.1, for 10 kW 600 Vdc / 240 Vac 10 kHz applications, a small output filter is required when less than 13 levels are used, in order to meet the 5% distortion limit.

Table 4.1 THD analysis of output voltage and current for different number of levels MMC, (10 kW, 10 kHz, 600 Vdc / 240 Vac, 0.95 power factor)

THD	I_{out}	V_{line_out}
5-level	0.48%	16.05%
7-level	0.65%	10.39%
9-level	0.59%	7.72%
11-level	0.59%	5.78%
13-level	0.45%	4.47%

The transfer function of a passive LC filter (Figure 4.7(a)) is given by (4-44). Equation (4-45) denotes the cut-off frequency.

$$G_{LC} = \frac{V_o}{V_{in}} = \frac{1/sC}{sL+1/sC} = \frac{1}{s^2LC+1} \tag{4-44}$$

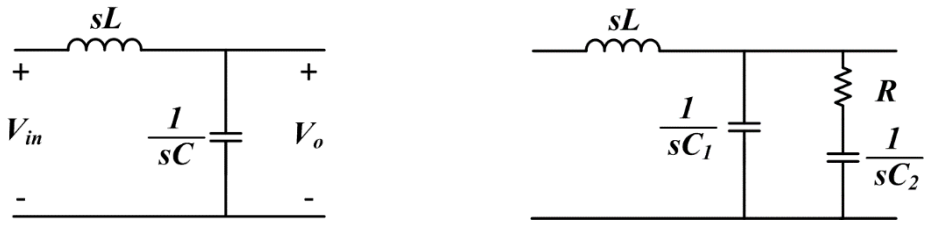
$$\omega_n = \frac{1}{\sqrt{LC}} \tag{4-45}$$

A large *L* would increase the converter volume and cost significantly, while a large *C* would draw large current from the converter which puts more stress on switching devices. Therefore, it is a trade-off when choosing *L* and *C* values.

The gain of passive LC filter at ω_n is infinite, as presented in Figure 4.8(a). In the parallel damped filter shown in Figure 4.7 (b), series-connected resistor *R* and capacitor C_2 are connected in parallel with capacitor C_1. The purpose of resistor *R* is to reduce the output peak impedance of the filter at the cut-off frequency. Capacitor C_2 blocks the low frequency component of the input voltage and prevents power dissipation in the filter resistance [101].

Equation (4-46) demonstrates the transfer function for the parallel damped filter. The cut-off frequency is the same as (4-45).

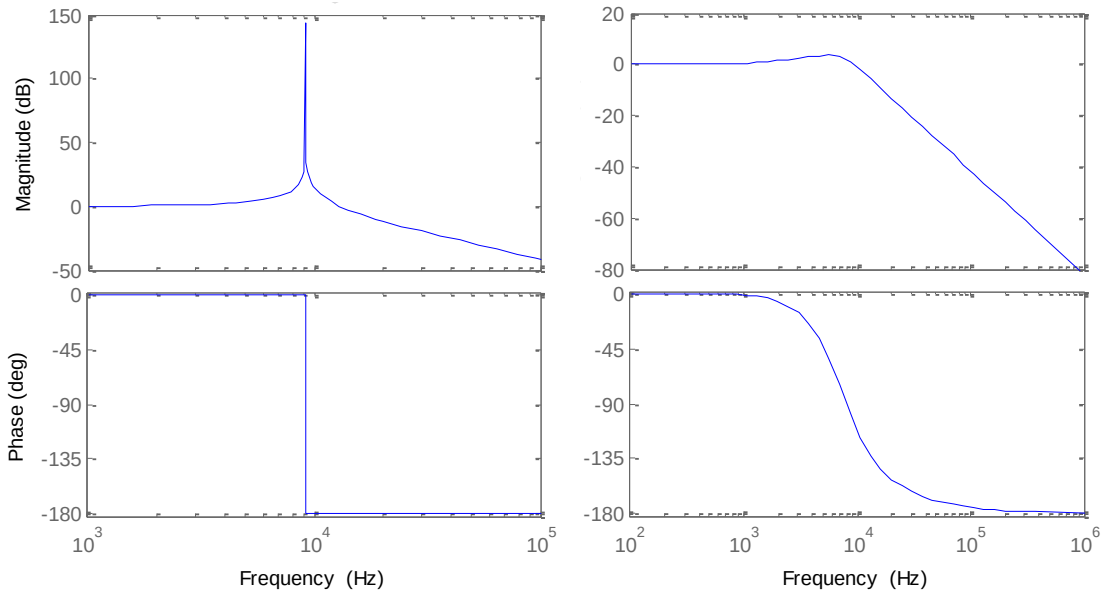
$$G_{dmp} = \frac{C_2Rs+1}{C_1C_2LRs^2+(C_1+C_2)Ls^2+C_2Rs+1} \tag{4-46}$$



(a) Passive LC filter (b) Parallel damped filter

Figure 4.7 Topologies of passive LC filter and parallel damped filter

From the Bode plot of the parallel damped filter shown in Figure 4.8 (b), the gain at the cut-off frequency is significantly damped. Therefore, in this study, the parallel damped filter is adopted.



(a) Bode plot of a passive LC filter (b) Bode plot of a parallel damped filter

Figure 4.8 Bode plots of passive LC filter and parallel damped filter

From an AC perspective, the arm inductances in one phase can be regarded as connected in parallel, and serve as part of the output filter (Figure 4.9). Hence for low voltage MMC, only capacitor is needed as the output filter. For example, the

output voltage THD for a 10 kHz, 5-level MMC (with parameters listed in Table 4.2) is 16.05%, as shown in Figure 4.10(a). The FFT analysis indicates the high distortions appear as sidebands, centered around the multiples of the switching frequency. Therefore, the cutoff frequency of the filter needs to be lower than the switching frequency. According to [101], the impedance of capacitor C_{f2} should be lower than R_f at the resonant frequency, while its capacitance should be higher than C_{f1} so that the cutoff frequency of the main filter will not be affected.

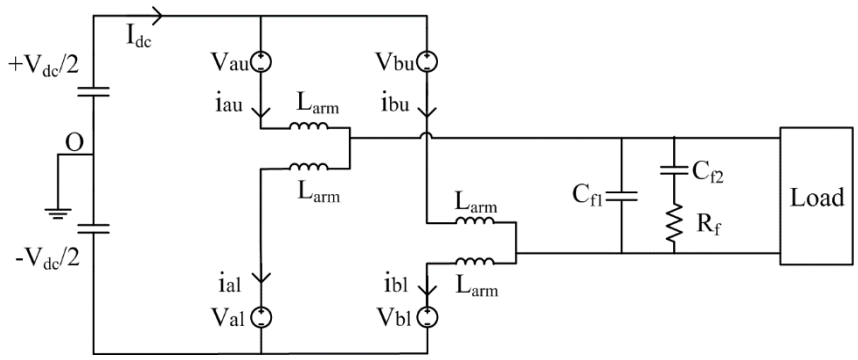


Figure 4.9 Equivalent circuit of two-phase-leg MMC with parallel damped filter

As shown in Figure 4.10(a), the FFT analysis suggests 20 kHz harmonic dominates. By setting the cutoff frequency equal to 10% of 20 kHz and applying (4-45), a parallel damped filter with C_{f1}=200 nF can be selected. According to [101], the optimum damping resistance R_f and capacitance value and C_{f2} are given by (4-47) and (4-48).

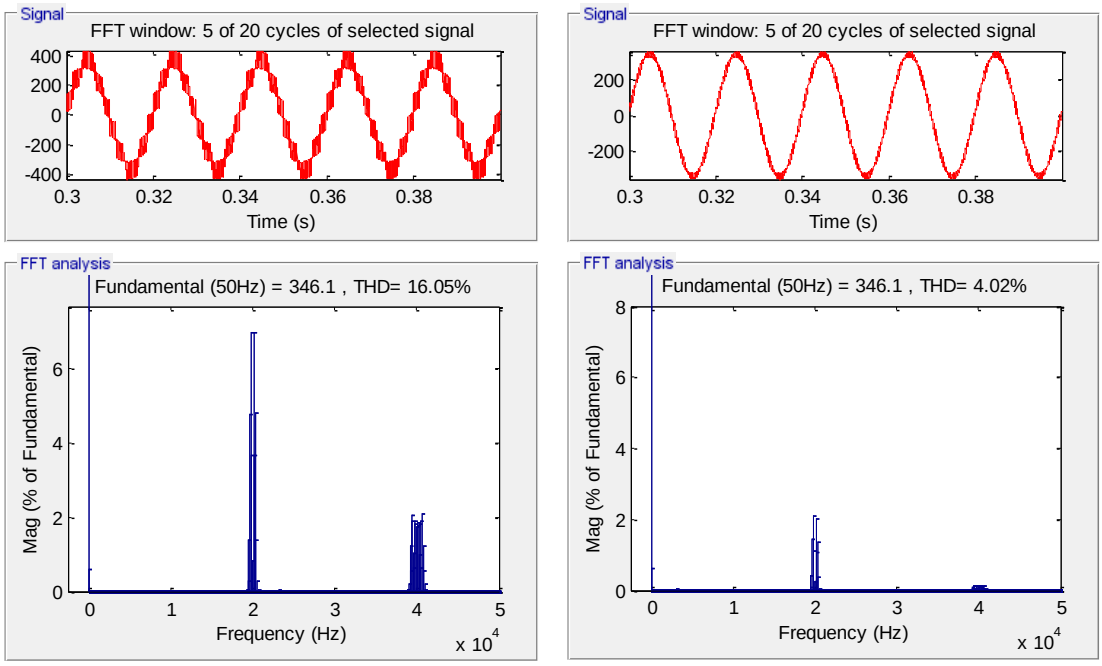
$$R_f = \sqrt{\frac{L_{arm}}{C_{f1}}} \tag{4-47}$$

$$C_{f2} = 4C \tag{4-48}$$

Therefore, C_{f2}=800 nF, R_f=86.6 Ω is designed. The output spectrum shown in Figure 4.10 (b) indicates that the filter can meet the 5% distortion factor.

Table 4.2 Circuit parameters for two-phase-leg 5-level MMC

Input Voltage (V_{dc})	600 V	Output Voltage (V_o)	240 V
Modulation Index (*M*)	0.57	Output Current (RMS)	43.86 A
Arm Inductance	1.5 mH	Submodule Capacitance	3.3 mF
Power Factor	0.95	I_{dc}	16.67 A
Real Power	10 kW	Load R_L	5.19 Ω
Switching Frequency	10 kHz	Load L_L	5.46 mH



(a) without output filter (b) with parallel damped filter

Figure 4.10 FFT analysis of output line voltage of 5-level two-phase-leg MMC

4.6 Control Strategies of MMC

This section analyses why the circulating current is a serious problem for single phase converters. For 2-level converter, the only way to eliminate it is by adding an input filter. For MMC, the capacitance is distributed in each submodule. Therefore, circulating current suppression control can be employed to compensate the common mode voltage by inserting and bypassing the required number of submodules. Closed-loop voltage regulation is also designed to maintain the output voltage value during changing load condition.

4.6.1 Second-order Harmonic Circulating Current

A. 2-level Converter

Single phase converter faces significant second harmonic issues. A simple analysis is given by equalling the input and output power of the converter (Figure 3.1).

$$\begin{aligned} P_{ac} = i_{ac} \cdot v_{ac} &= \hat{I}_{ac} \sin(\omega t + \varphi) \cdot M V_{dc} \sin(\omega t) \\ &= \frac{1}{2} M \hat{I}_{ac} V_{dc} [\cos\varphi - \cos(2\omega t + \varphi)] \end{aligned} \tag{4-49}$$

$$i_{dc} = \frac{P_{dc}}{V_{dc}} = \frac{P_{ac}}{V_{dc}} = \frac{1}{2} M \hat{I}_{ac} [\cos\varphi - \cos(2\omega t + \varphi)] \tag{4-50}$$

where P_{ac} denotes the AC side power, i_{ac} is the AC side current, v_{ac} is the output line voltage, $\hat{I}_{ac}$ is the peak amplitude of i_{ac}, the φ is the phase angle and M is the modulation index.

The AC output power consists of DC and 2nd harmonic component, as illustrated in (4-49). Assuming there is no power loss within the converter, and V_{dc} is constant, (4-50) can be obtained, demonstrating that a large amount of 2nd harmonic current is presented on the DC side.

B. Single-phase and Three-phase MMC

From (4-7) and (4-9), the average upper arm capacitor current can be expressed as the sum of fundamental-frequency and 2nd harmonic components.

$$i_{cu} = -i_c^{(1)}(t) + i_c^{(2)}(t) \tag{4-51}$$

where $i_c^{(1)}(t) = \frac{M}{2} I_{dc} \cdot sin\omega t - \frac{1}{4} I_{ao} \sin(\omega t + \varphi)$,

and $i_c^{(2)}(t) = \frac{M}{8} I_{ao} \cos(2\omega t + \varphi)$.

And the average lower arm capacitor current is given by (4-52).

$$i_{cl} = i_c^{(1)}(t) + i_c^{(2)}(t) \tag{4-52}$$

The n^{th} capacitor ripple voltage can be obtained by multiplying the corresponding capacitor reactance and the n^{th} harmonic capacitor current.

$$\Delta u_C^{(n)}(t) = \frac{i_c^{(n)}(t)}{jn\omega C} \rightarrow V_n \sin n\omega t \tag{4-53}$$

where $\Delta u_C^{(n)}(t)$ denotes the n^{th} harmonic capacity voltage and can be represented by $V_n \sin n\omega t$ for short.

Hence the total capacitor ripple voltage of upper and lower cells can be indicated as ΔV_{cu} and ΔV_{cl} respectively.

$$\Delta V_{cu} = -V_1 \sin \omega t + V_2 \sin 2\omega t \tag{4-54}$$

$$\Delta V_{cl} = V_1 \sin \omega t + V_2 \sin 2\omega t \tag{4-55}$$

Therefore, the ripple voltage of the submodule terminal is:

$$\Delta V_{au} = m_u \cdot \Delta V_{cu} = (\frac{1}{2} - \frac{M}{2} \cdot \sin \omega t) \cdot (-V_1 \sin \omega t + V_2 \sin 2\omega t) \tag{4-56}$$

$$\Delta V_{al} = m_l \cdot \Delta V_{cl} = (\frac{1}{2} + \frac{M}{2} \cdot \sin \omega t) \cdot (V_1 \sin \omega t + V_2 \sin 2\omega t) \tag{4-57}$$

Ripple voltage across the phase

$$\Delta V_a = \Delta V_{au} + \Delta V_{al} = 2 \cdot (\frac{M}{2} \cdot \sin \omega t \cdot V_1 \sin \omega t + \frac{1}{2} V_2 \sin 2\omega t) \tag{4-58}$$

This means there is only 2nd harmonic component as the ripple voltage across the phase. The 2nd harmonic component in the phase ripple voltage can produce a circulation current which has a double line-frequency in the converter arms. Therefore, the circulating current can be expressed as (4-59).

$$i_{diff} = I_{diff} \sin(2\omega t + \theta) \tag{4-59}$$

In a 3-phase condition, assuming a balanced load, the DC side ripple current is given by (4-60).

$$\begin{aligned} \Delta I_{dc_{3ph}} &= i_{diff_a} + i_{diff_b} + i_{diff_c} = I_{diff_a} \sin(2\omega t + \theta) + \\ &\quad I_{diff_b} \sin(2(\omega t + 120^o) + \theta) + I_{diff_c} \sin(2(\omega t + 240^o) + \theta) \\ &= I_{diff_a} \sin(2\omega t + \theta) + I_{diff_b} \sin(2\omega t + \theta + 240^o) \\ &\quad + I_{diff_c} \sin(2\omega t + \theta + 120^o) \end{aligned} \tag{4-60}$$

If the load is well balanced $I_{diff_a} = I_{diff_b} = I_{diff_c}$, the current in DC side will not have a 2nd harmonic component, as indicated in (4-61).

$$\Delta I_{dc_{3ph}} = I_{diff_a}[\sin(2\omega t + \theta) + \sin(2\omega t + \theta + 240^o) + \sin(2\omega t + \theta + 120^o)] = 0 \quad (4\text{-}61)$$

For an H-bridge inverter, however, instead of cancelling each other, the 2nd harmonic component will be enhanced in the DC side current, as shown in (4-62).

$$\begin{aligned} \Delta I_{dc_H} &= i_{diff_a} + i_{diff_b} \\ &= I_{diff_a}\sin(2\omega t + \theta) + I_{diff_b}\sin(2(\omega t + 180^o) + \theta) \\ &= 2I_{diff_a}\sin(2\omega t + \theta) \end{aligned} \quad (4\text{-}62)$$

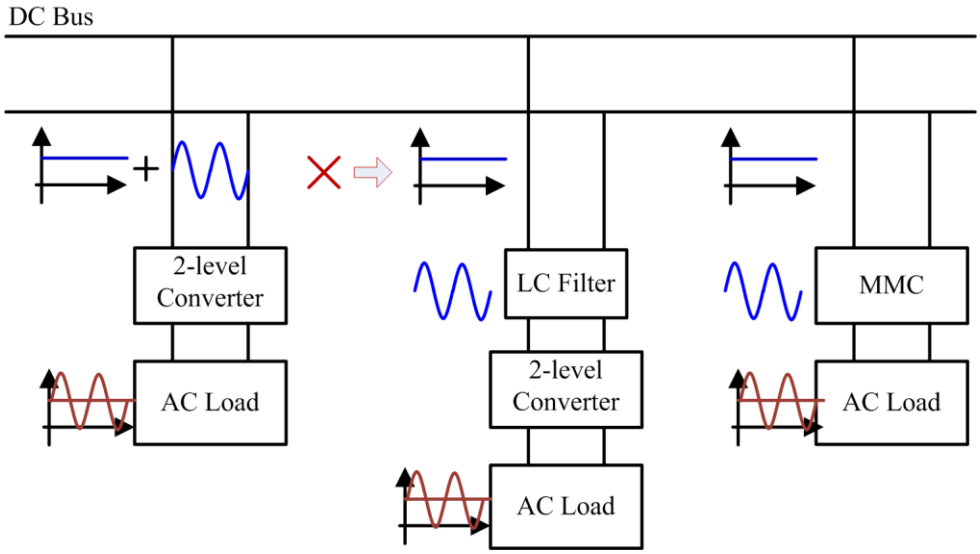


Figure 4.11 Inverters for DC distribution network

The harmonics in DC side current will increase transmission power losses and could potentially lead to the DC network malfunction. The current circulating between phases will increase the semiconductor power losses, which may damage the switches. Therefore, as shown in Figure 4.11, for conventional 2-level converter, an input filter is often required, which stops the 2nd harmonic energy from being transmitted to the DC side. For MMC, however, since the DC capacitors are distributed in the converter, they can be controlled to store the second harmonic energy without the requirement of a bulky input filter. The circulating current suppression control will be designed in Section 4.6.2.

4.6.2 Circulating Current Suppression Control

A. Mechanism of Harmonics in the Circulating Current

In this section, the circulating current suppression control for single phase MMC is developed. Assumption 1 in Section 4.2 is not applicable since there are even harmonic components in the circulating current i_{diff} [94, 102]. Therefore, upper and lower arm currents ((4-3) and (4-4)) are expressed in (4-63) and (4-64), and i_{diff} can be derived in (4-65).

$$i_{au} = i_{diff} + \frac{i_{ao}}{2} \tag{4-63}$$

$$i_{al} = i_{diff} - \frac{i_{ao}}{2} \tag{4-64}$$

$$i_{diff} = \frac{i_{au}+i_{al}}{2} \tag{4-65}$$

As illustrated in Figure 4.1, (4-66) and (4-67) can be obtained according to KVL, where R represents the parasitic ohmic losses.

$$\frac{V_{dc}}{2} - v_{au} - Ri_{au} - L\frac{di_{au}}{dt} - v_{ao} = 0 \tag{4-66}$$

$$\frac{V_{dc}}{2} + v_{ao} - Ri_{al} - L\frac{di_{al}}{dt} - v_{al} = 0 \tag{4-67}$$

The difference of (4-66) and (4-67) is given by (4-68).

$$v_{ao} = \frac{-v_{au}+v_{al}}{2} + \frac{1}{2}Ri_{ao} + \frac{L}{2}\frac{di_{ao}}{dt} \tag{4-68}$$

The differential mode component of arm voltages is defined as e_a.

$$e_a = \frac{-v_{au}+v_{al}}{2} \tag{4-69}$$

It illustrates that e_a controls the output current i_{ao} directly, i.e. controls the output power.

By adding (4-66) and (4-67) together, and combining (4-65), (4-70) can be derived.

$$V_{dc} - (v_{au} + v_{al}) = 2Ri_{diff} + 2L\frac{di_{diff}}{dt} \tag{4-70}$$

Define half of the voltage difference between DC side voltage and the sum of upper and lower arm voltage is u_{diff}.

$$u_{diff} = \frac{V_{dc}-(v_{au}+v_{al})}{2} = Ri_{diff} + L\frac{di_{diff}}{dt} \quad (4\text{-}71)$$

Equation (4-71) implies that u_{diff} gives rise to the circulating current, as illustrated in Figure 4.12. Therefore, the control of i_{diff} can be realised by regulating the common mode arm voltages [103]. The current control block diagram is shown in Figure 4.13.

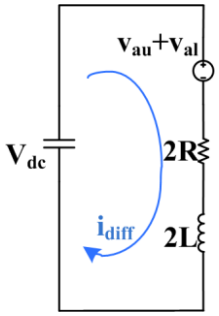


Figure 4.12 Equivalent circuit of circulating current

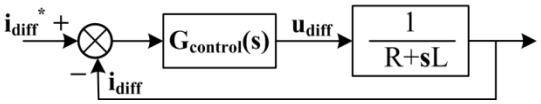


Figure 4.13 Current suppression control block diagram

By substituting (4-69) into (4-71), the references of arm voltage can be given by (4-72) and (4-73) [104].

$$v_{au}^{*} = \frac{V_{dc}}{2} - e_a - u_{diff} \quad (4\text{-}72)$$

$$v_{al}^{*} = \frac{V_{dc}}{2} + e_a - u_{diff} \quad (4\text{-}73)$$

e_a is generated by the main PWM controller to control the output voltage and power. u_{diff} is the voltage difference generated by the inner current suppression controller to suppress the circulating current.

In the following Section B and Section C, two types of circulating current suppression controller will be introduced.

B. Proportional Resonant (PR) Control

The standard proportional integral (PI) controller functions adequately for DC quantities. For single-phase AC, however, a PI controller introduces a residual

constant error [105]. A PR controller can achieve zero steady-state error at certain operation frequency [106], due to its infinite gain, as shown in Figure 4.14. Also, PR controller has a very narrow bandwidth, which ensures the controller only affect circulating current at a certain frequency. In addition, it has been concluded in Section 4.6.1 that the second harmonic dominates. Therefore, a PR controller at 100 Hz is adopted in this section.

The transfer function of PR controller is shown in (4-74).

$$G_{PR}(s) = K_P + \frac{K_r s}{s^2+\omega_n{}^2} \tag{4-74}$$

where K_P and K_r are the proportional and resonant gains respectively, and ω_n is the resonant frequency.

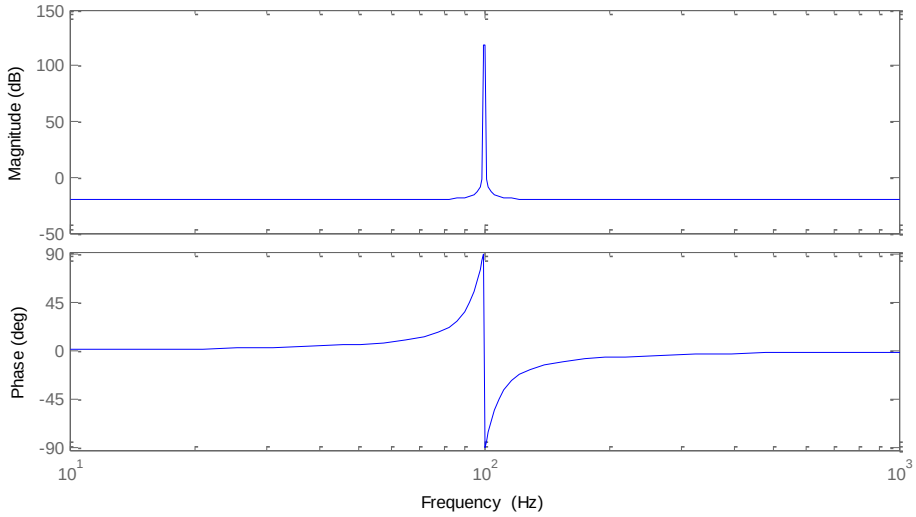


Figure 4.14 Bode plot of PR controller at 100 Hz resonant frequency

As shown in Figure 4.15, the circulating current i_{diff} can be obtained by halving the sum of arm currents. Then the high pass filter (5 Hz cut-off frequency) filters out the DC component. Therefore only harmonics (i_{diff_ac}) would be left, among which the second harmonic dominates. The 2nd order harmonic current reference ($i^*_{diff\_ac}$) is set as zero and compared with i_{diff_ac}. Their difference is feed into a PR controller, which will generate an infinite gain and achieve zero-steady state error at 100 Hz. The output u_{diff} is then subtracted from the arm voltage modulation references in (4-72) and (4-73) in order to compensate the voltage variations of submodule capacitors.

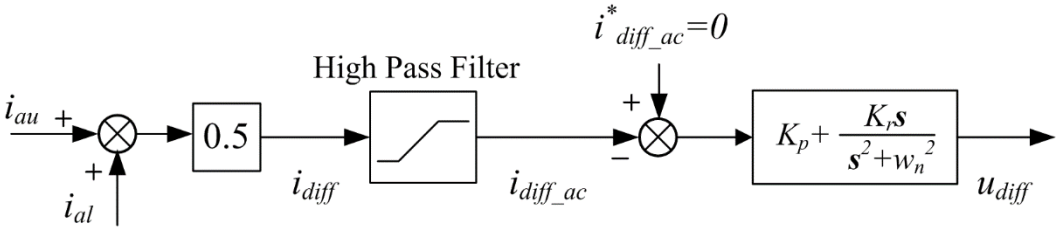


Figure 4.15 PR control block for circulating current suppression

Simulation results for a 10 kW 5-level 2-phase-leg Si MOSFET MMC are shown in Figure 4.16. It shows with PR controller, the 2nd harmonic in the circulating current is almost eliminated and the arm currents are composed of a 50 Hz sine wave with a DC offset. With 1.5 mH arm inductance, the input DC current ripple is 4.2% which is within the 5% current distortion limit.

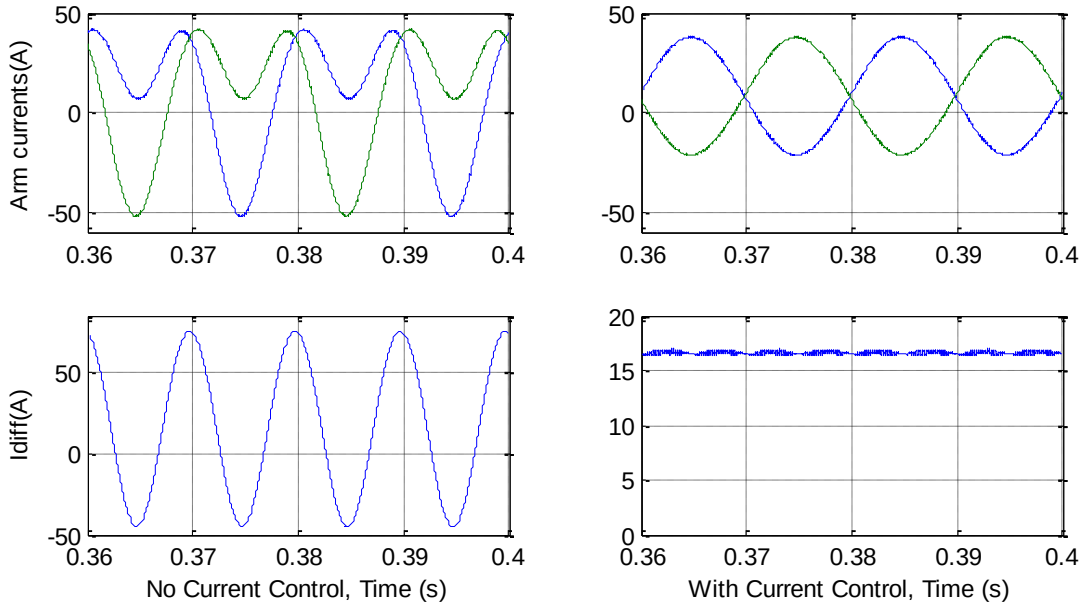


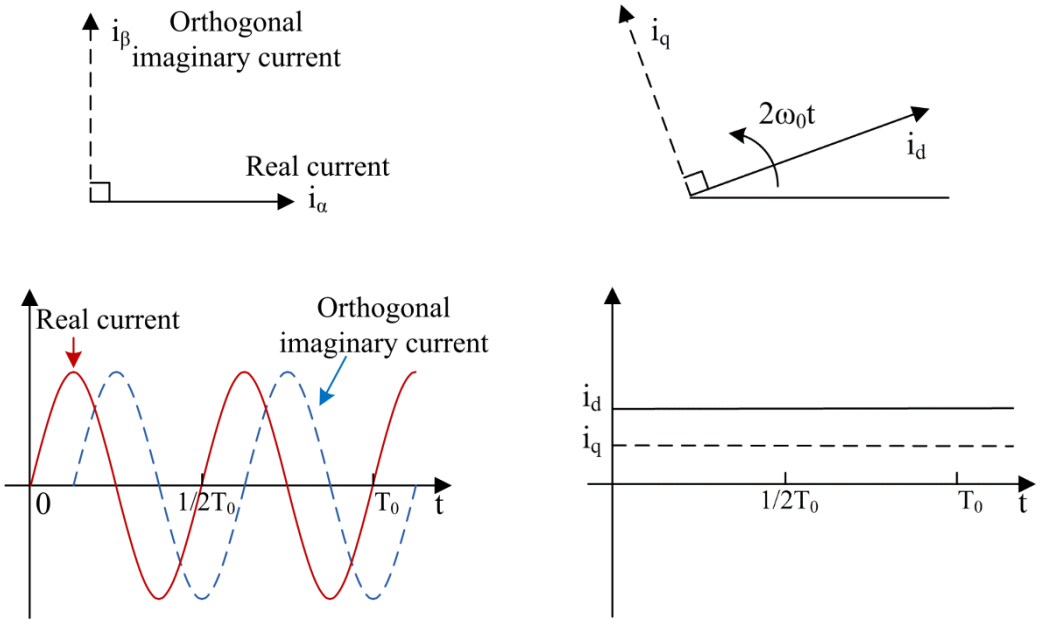
Figure 4.16 Simulation results of arm currents and circulating current of 5-level 2-phase-leg Si MOSFET MMC, without and with PR current control. (V_{dc}=600 V, V_{out}=240 V, 10 kW, L_{arm}=1.5 mH)

C. Proportional Integral (PI) Control with Orthogonal Imaginary Axis

DQ transformation is commonly used in three-phase system, where AC signals are transformed into two-axis, stationary (αβ) frame, then into rotating (dq) reference

frame to become DC quantities. Thereby, a PI controller can be adopted to achieve zero steady-state error. However, for a single-phase system, in order to apply DQ transformation and achieve zero steady-state error, a fictitious phase must be created to generate an orthogonal plane [107]. There are many ways to generate the virtual axis from a single-phase signal, such as shifting the AC signal by 90°C [108], applying a first-order, all-pass filter phase shifter [109] and second-order generalised integrator [110].

In this study, the orthogonal axis is generated by delaying 90°C of the real signal, as illustrated in Figure 4.17 (a). The real current is the i_{diff} after the high pass filter, in which the second harmonic dominates. The stationary αβ coordinate can be transformed to the rotary dq coordinate through the Park Transformation (4-75).



(a) Two phase stationary (αβ) frame (b) Two phase rotary (dq) frame

Figure 4.17 Reference frames for Park Transformation, T_0 is the fundamental time period, the real current is the second harmonic component

As shown in the control block diagram (Figure 4.18), after the Park Transformation, two DC quantities i_d/i_q are generated. The reference signals (i^*_d/i^*_q) are set to zero because the input harmonic signal should be eliminated. PI controller is then applied to ensure a zero steady-state error. Although i_q is imaginary and does not exist

practically, the PI control action has been done in the dq frame. The compensation, however, is only made on the real signal, i.e. only u_{diff} will be adopted for the use of (4-72) and (4-73).

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4-75}$$

where $\omega t=2(2\pi/T_0)t$ in this application.

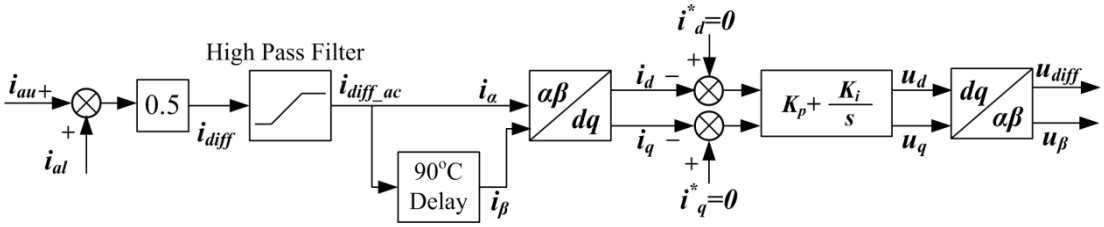


Figure 4.18 PI current suppression control block diagram with imaginary orthogonal axis

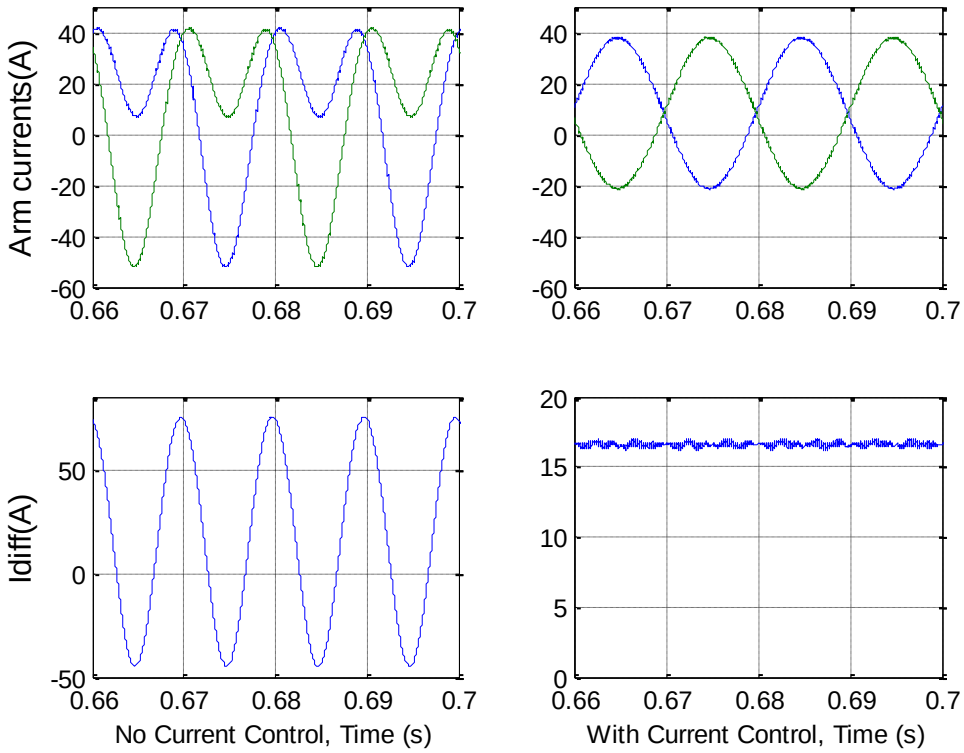


Figure 4.19 Simulation results of arm currents and circulating current of 5-level 2-phase-leg Si MOSFET MMC, without and with PI current control. (V_{dc}=600 V, V_{out}=240 V, 1.5 kW, L_{arm}=1.5 mH)

Simulation results for a 10 kW 5-level 2-phase-leg Si MOSFET MMC are shown in Figure 4.19. With PI controller, the 2nd harmonic in the circulating current is almost

eliminated. It has similar results with PR controller that the input DC current ripple is 4.2%.

4.6.3 Output Voltage Regulation

The voltage regulation is designed to stabilise the output voltage for varying load condition. When the load current changes, voltage drop on the arm inductors and filter will change, which gives rise to an error between the output voltage vo and the output voltage reference v* (Figure 4.20). For single-phase AC, a PR controller with 50 Hz resonant frequency is adopted because it can provide zero steady-state error [105]. The definition of parameters for the overall control schematic blocks shown in Figure 4.20 is listed in Table 4.3.

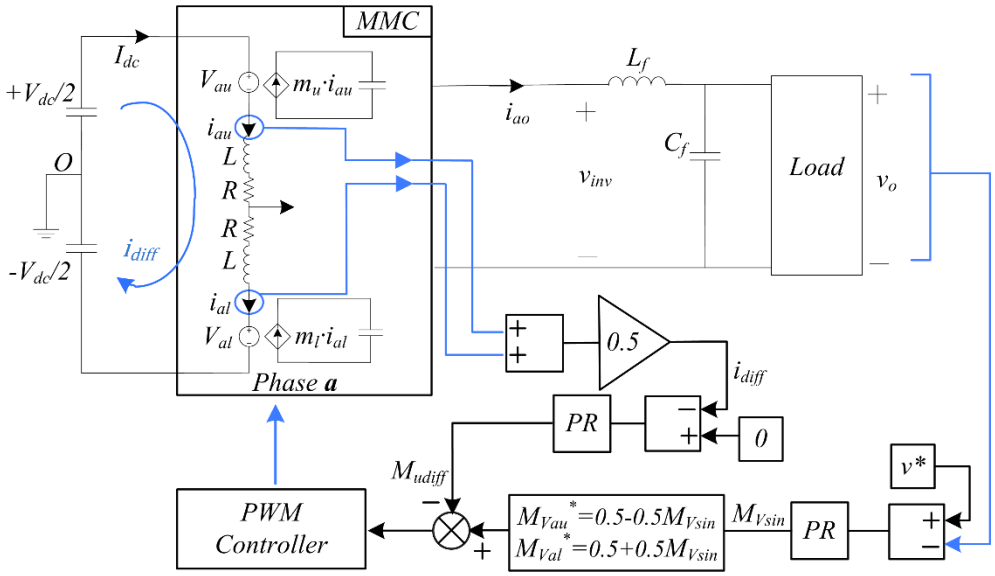


Figure 4.20 Overall control schematic blocks of MMC

Table 4.3 Definition of parameters for the MMC overall control schematic blocks

v_o	The output load voltage	v_{inv}	Inverter output
v^*	The output voltage reference	Z_L	Load impedance
M_{Vsin}	Output modulation signal of voltage controller		
M_{Vau}	Modulation signal of upper arm		
M_{Val}	Modulation signal of lower arm		
M_{udiff}	Compensating signal of circulating current suppression control		

The PR controller generates the 50 Hz fundamental control signal for MMC. For example, (4-76) shows the relationship of inverter output v_{inv} and DC side voltage in a single-phase-leg MMC, where M and Θ are generated by the PR controller according to the arm inductance, filter impendence and the error between v_o and v^*. To simplify the mathematics, the filter is assumed to be a passive LC filter.

$$V_{inv} = M_{Vsin} \cdot V_{dc} = M \sin(\omega t + \theta)\, V_{dc} \tag{4-76}$$

Based on Figure 4.20, the impedance of C_f in parallel with Z_L is expressed by (4-77). The inductance is the sum of half arm inductance ($L_{arm}/2$) and filter inductance. Hence equation relating v_o and v_{inv} is given by (4-78).

$$Z_o = C_f // Z_L = \frac{Z_L}{1 + j\omega C_f Z_L} \tag{4-77}$$

$$v_o = \frac{Z_o}{j\omega\left(\frac{L_{arm}}{2} + L_f\right) + Z_o} \cdot v_{inv} = |Z| e^{ir} v_{inv} \tag{4-78}$$

By substituting (4-76) into (4-78), (4-79) can be obtained. By equalising amplitude and phase angle of (4-79), M and Θ are given by (4-80) and (4-81) respectively.

$$\hat{V}_o \sin \omega t = |Z| \cdot M \cdot \sin(\omega t + \theta + \gamma) \cdot V_{dc} \tag{4-79}$$

$$\mathrm{M} = \frac{\hat{V}_o}{|Z| \cdot V_{dc}} \tag{4-80}$$

$$\theta = -\gamma = \tan^{-1} \frac{\omega R_L \left(\frac{L_{arm}}{2} + L_f\right)}{F \cdot |Z_L|^2 + \omega X_L \left(\frac{L_{arm}}{2} + L_f\right)} \tag{4-81}$$

where $\hat{V}_o$ is the peak value of output voltage; $Z_L = R_L + jX_L$ is the load impedance; F is a factor relating to the arm inductance and filter parameters:

$$F = 1 - \omega^2 C_f \left(\frac{L_{arm}}{2} + L_f\right) \tag{4-82}$$

and Z refers to the impedance proportion that defines the voltage sharing:

$$Z = \frac{F \cdot |Z_L|^2 + \omega X_L \left(\frac{L_{arm}}{2} + L_f\right) - j\omega R_L \left(\frac{L_{arm}}{2} + L_f\right)}{F^2 \cdot |Z_L|^2 + 2\omega X_L \left(\frac{L_{arm}}{2} + L_f\right) \cdot F + \omega^2 \left(\frac{L_{arm}}{2} + L_f\right)^2} \tag{4-83}$$

Instead of carrying out those complicated mathematics, PR controller is able to generate M and Θ automatically to compensate the output voltage error.

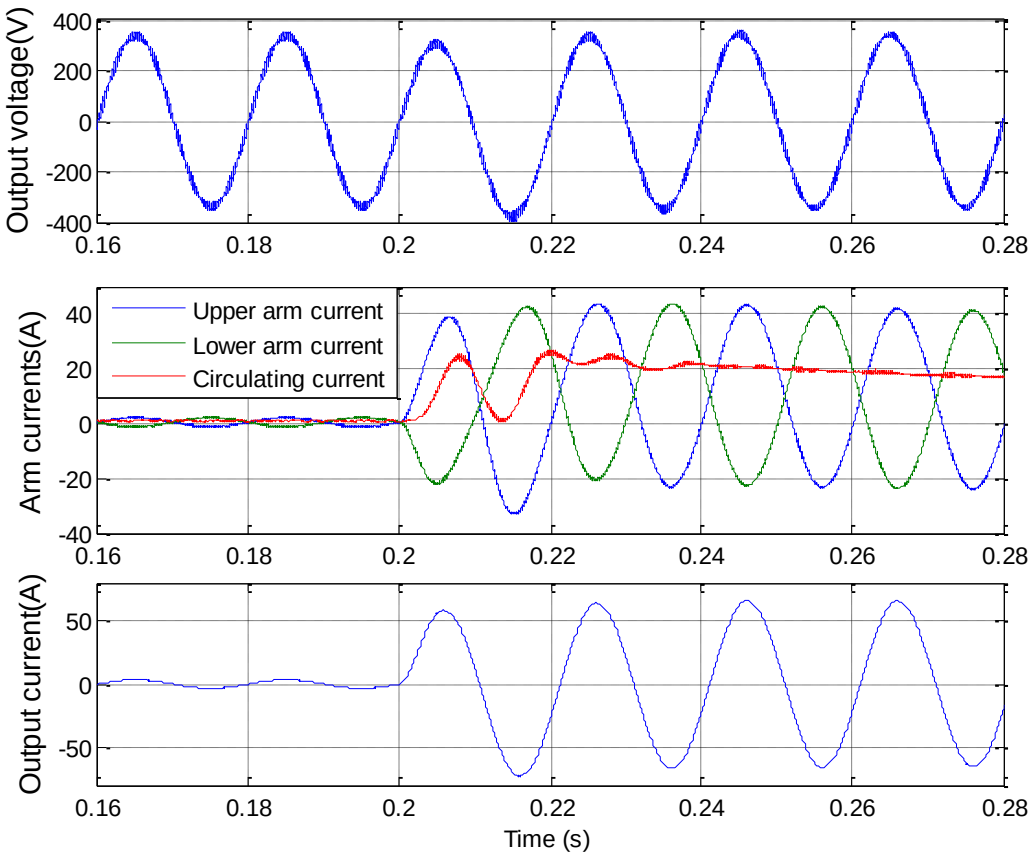


Figure 4.21 Voltage and currents waveforms of a 10 kW two-phase-leg 5-level MMC when the load is increased at 0.2 s

Figure 4.21 shows the simulation results for a 5-level H-bridge MMC, where the output power changes from 500 W to 10 kW at t=0.2 s. The results indicate that the output voltage v_o can be stabilised during the transition from almost no load to the full-load condition. Arm currents and output current undergo a sudden increase at t=0.2 s, and the arm currents are stable and free from 2nd harmonic distortion. The FFT analysis shows that the total harmonic distortions (THD) of the output voltage and current are 3.98% and 0.46% respectively, indicating a very high quality output power.

4.7 Experimental Verification

In this section, test rig of MOSFET-based single-phase-leg 5-level MMC with 4 submodules in one arm is built to verify the current suppression control methods which are introduced in Section 4.6.

4.7.1 Hardware Setup

A. Test Rig Layout

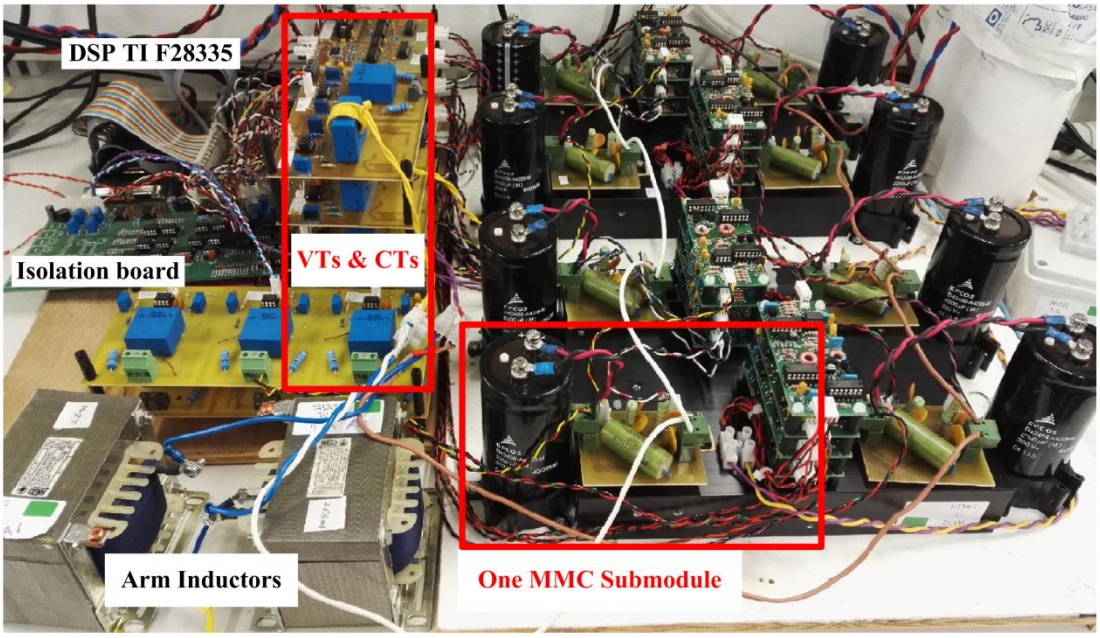
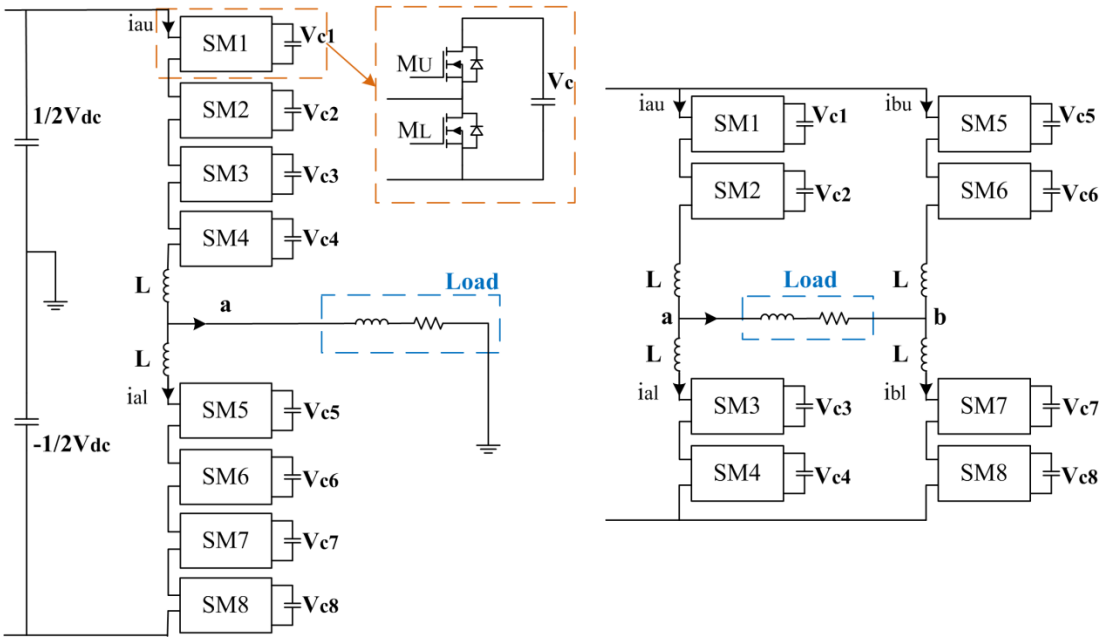


Figure 4.22 5-level MMC prototype

The MMC prototype consists of 8 MMC submodules in total, a TI F28335 digital signal processor (DSP) and voltage and current transducers, as shown in Figure 4.22. The 8 submodules can be either connected as a 5-level single-phase-leg MMC or as a 3-level two-phase-leg MMC, as shown in Figure 4.23.

Figure 4.24 presents the signal process loop of a 5-level single-phase-leg MMC. Eight submodule capacitor voltage signals and two currents signals are detected by the voltage and current transducers. The 10 feedback signals from transducers are sent to the interface circuits, which have the function of isolation. Then signals are sampled at each interruption of the DSP (10 kHz). The current suppression control is

implemented by DSP. Then eight PWM signals are generated to control the submodules. Complimentary boards are employed to create complimentary signals from these eight signals with a 2 μs dead-time. In the end, 16 signals are sent to gate drivers to drive power MOSFETs.



(a) 5-level single-phase-leg MMC (b) 3-level two-phase-leg MMC

Figure 4.23 Test rig topologies: 5-level single-phase-leg MMC and 3-level two-phase-leg MMC

The circuit details (schematic diagrams) of voltage and current transducers, interface circuits, DSP, complimentary board and gate driver are presented in Appendix A.

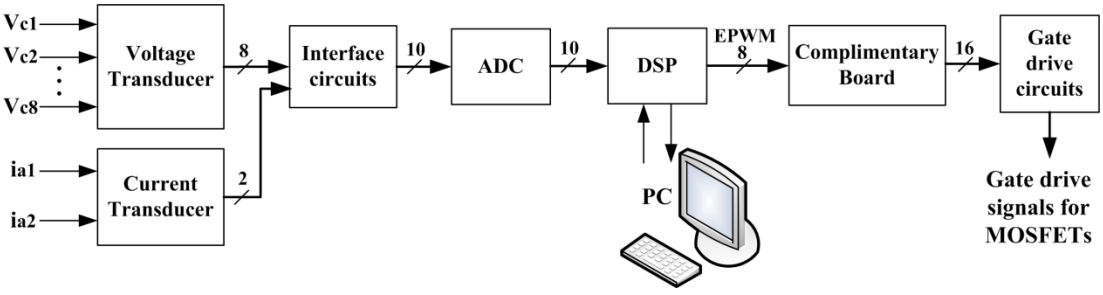


Figure 4.24 Schematic diagram of 5-level single-phase-leg MMC prototype

B. Main Circuit and Snubber Circuit Design

One MMC submodule is shown in Figure 4.25. The 150 V varistor is paralleled besides each MOSFET to protect it from over voltage. A 2.2 μF film capacitor is connected directly across the two MOSFETs serving as a high-frequency bypass capacitor. An RC snubber circuit is designed to suppress the turn-off voltage overshoot caused by the stray inductance.

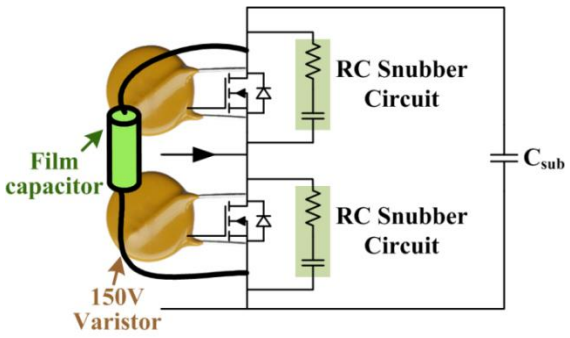


Figure 4.25 One MMC submodule schematic of the test rig

The circuit of Figure 4.26 shows the submodule's parasitic inductances (L_{stray}) and capacitance (C_{par}). L_{stray1}/L_{stray2} is composed of drain/source bonding and lead inductances of MOSFET and drain/source copper trace stray inductances of the printed circuit board (PCB) [111]. C_{par} is mainly the output capacitance of MOSFET. The EMI will be introduced by the unwanted coupling of signals through the parasitic impedances. The parasitic inductances will cause the voltage oscillation during the MOSFET turn-off transient (Figure 4.27(a)). If the amplitude of voltage overshoot exceeds the maximum rated voltage of MOSFET, it may damage the device. The conducted EMI generated by the ringing could also result in problems for adjacent ICs.

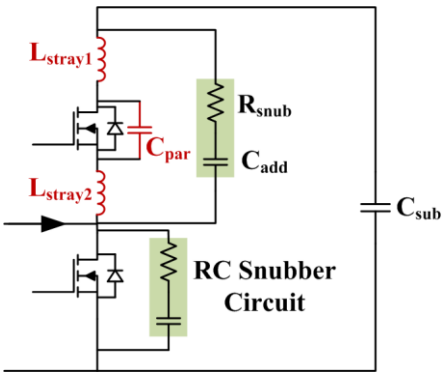
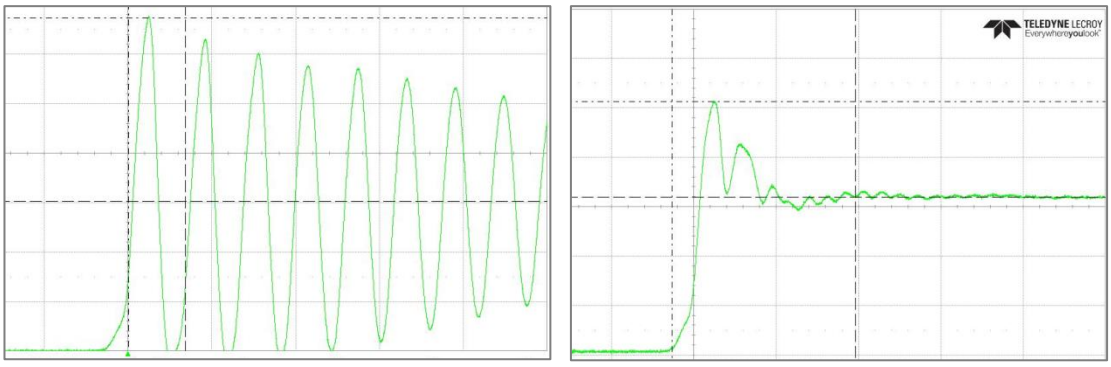


Figure 4.26 One MMC submodule schematic with snubber circuit

Figure 4.27 shows the scope plots of MOSFET turn-off voltage. The drain-to-source voltage V_{ds} is clamped to 60 V. The peak amplitude of the voltage oscillation, however, reached 134.2 V (Figure 4.27(a)). In comparison, Figure 4.27(b) shows the snubber circuit suppressed the overshoot voltage and damped the ringing, by providing an alternative path for the high frequency current which flows through the stray inductances.



(a) without snubber circuit, ΔV=74.2 V (b) with snubber circuit, ΔV=38.6 V

Figure 4.27 MOSFET turn-off voltage waveforms, 60 V *Vds* (20 V/div, 100 ns/div)

The frequency of the ringing caused by L_{stray1}, L_{stray2} and C_{par} can be determined from the scope plot in (Figure 4.27(a)), which is given by (4-84).

$$f_0 = \frac{1}{2\pi\sqrt{L_{\sum stray}C_{par}}} \tag{4-84}$$

where $L_{\sum stray}$ denotes the total parasitic inductance.

The ringing frequency can be reduced by half with certain amount capacitance (C_{add}) added in parallel with the MOSFET. Since the resonant frequency of an LC circuit is

given by (4-85), the relationship of snubber capacitor (C_{add}) and the parasitic capacitor can be expressed as (4-86).

$$f_{new} = \frac{1}{2} f_0 = \frac{1}{2\pi\sqrt{L_{\sum stray}(C_{par}+C_{add})}} \tag{4-85}$$

$$C_{add} = 3C_{par} \tag{4-86}$$

Rearranging (4-84), the total parasitic inductance can be obtained. The snubber resistance can then be given by (4-86).

$$L_{\sum stray} = \frac{1}{\frac{C_{add}}{3}(2\pi f_0)^2} \tag{4-87}$$

$$R_{snub} = \sqrt{\frac{L_{\sum stray}}{C_{par}}} \tag{4-88}$$

The experiment result (Figure 4.27(b)) shows the overshoot voltage is 38.6 V for 60V *Vds*. When the *Vds* increases to 100 V, result in Figure 4.28 shows the overshoot voltage doesn't increase. In this case, it is safe to use 200 V rated MOSFET IRFP4668PbF for the application of 600 *Vdc* (150 V for each submodule) application.

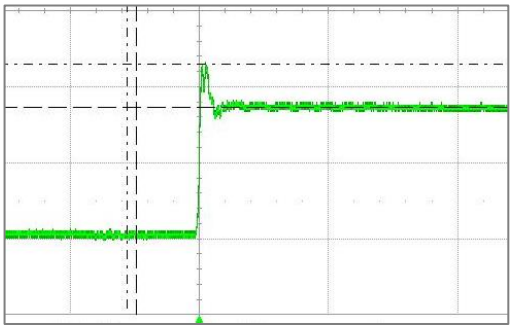
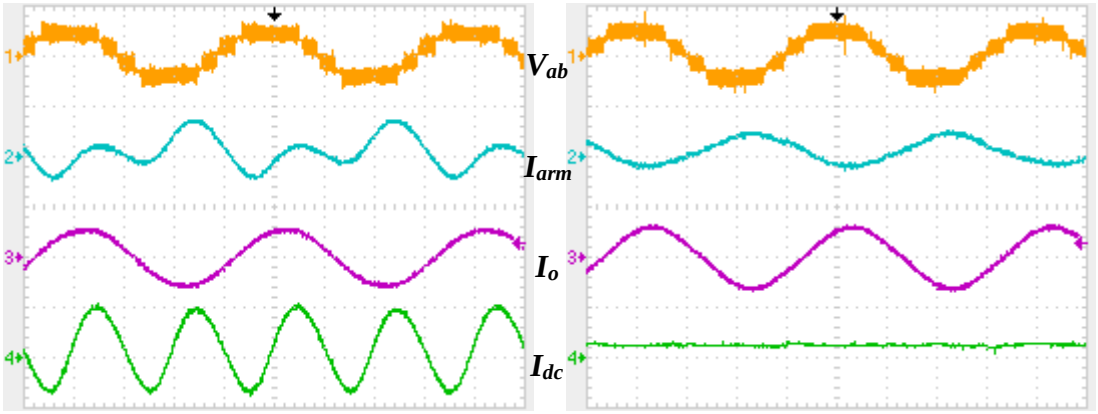


Figure 4.28 MOSFET turn-off voltage waveforms with snubber circuit, 100 V *Vds*, ΔV=28 V (50 V/div, 1 μs/div)

4.7.2 Case 1: Two-phase-leg 3-level MMC

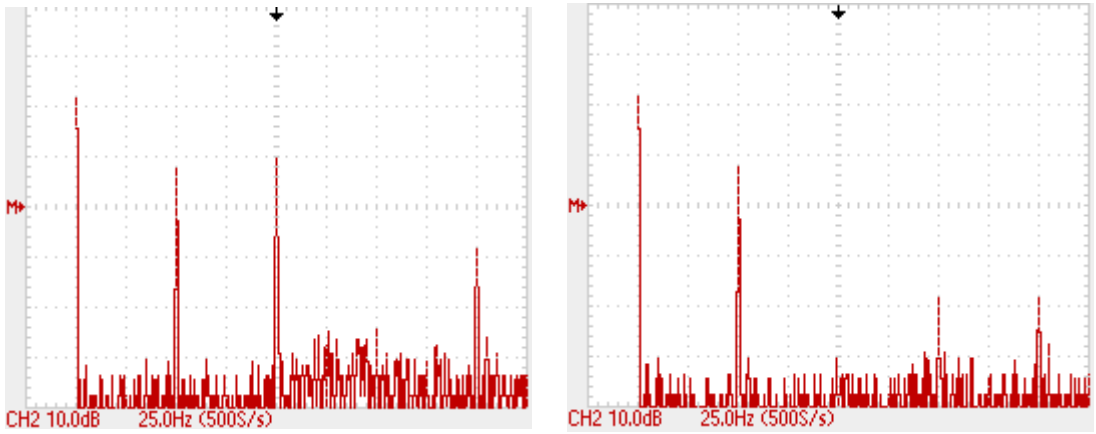
In this study, the test rig is connected to form a two-phase-leg 3-level MMC, as shown in Figure 4.23 (b). A PR controller is adopted to suppress the 2nd harmonic circulating current. Experimental results are presented in Figure 4.29, which

demonstrates that the 2nd harmonic in the input DC current is almost eliminated with PR control. In a result, the ripple of output voltage waveform is smaller with current suppression control. Figure 4.30 shows the FFT analysis of arm current. It demonstrates that the PR controller eliminates the 100 Hz harmonics.



(a) No current suppression control (b) With current suppression control

Figure 4.29 Waveforms of two-phase-leg 3-level MMC, without and with current suppression control (V_{ab}: 100 V/div; Currents: 5 A/div)



(a) No current suppression control (b) With current suppression control

Figure 4.30 FFT analysis of arm current, with and without current suppression control. (10 dB/div, time 25 Hz/div)

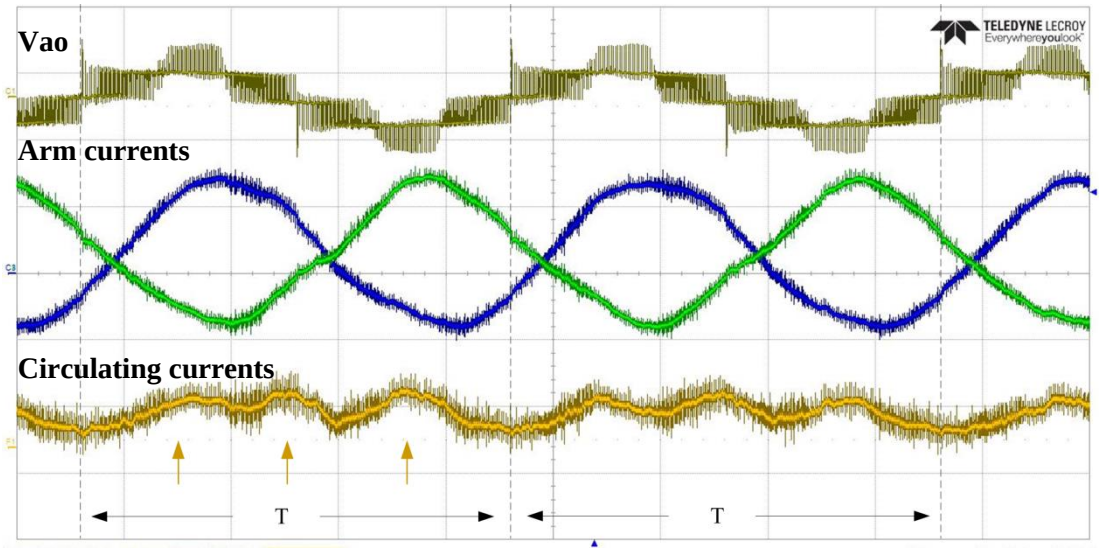
4.7.3 Case 2: Single-phase-leg 5-level MMC

The topology for the second case study is shown in Figure 4.23(a), which is a single-phase-leg 5-level MMC. Experimental parameters are listed in Table 4.4. Two

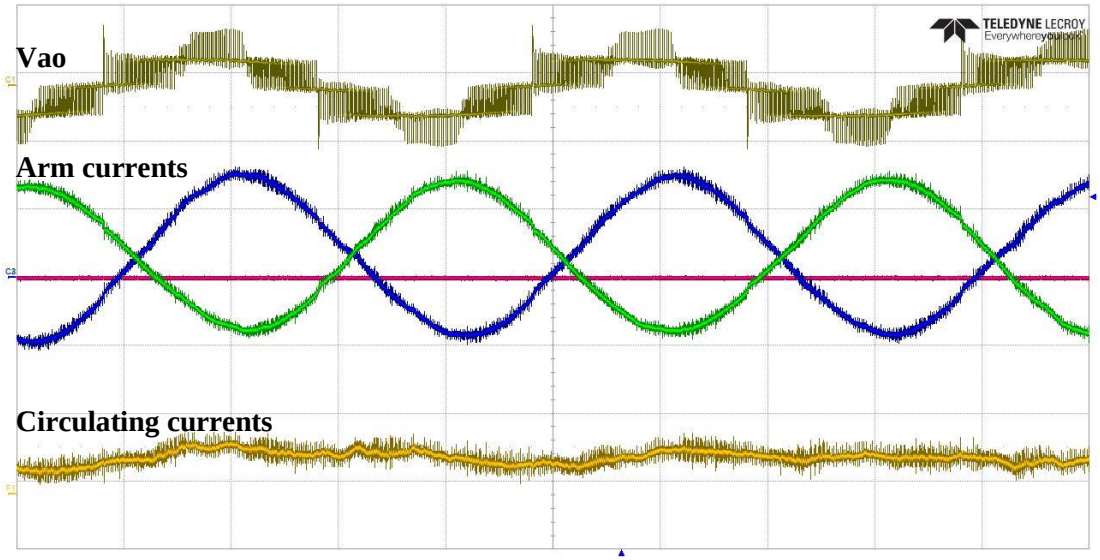
different current suppression control strategies – PR control and PI control with orthogonal imaginary axis are applied and results are shown in Figure 4.31.

Table 4.4 Experimental parameters of a single-phase-leg 5-level MMC

Submodule capacitance	3.3 mF	Arm inductance	1.5 mH
Snubber capacitance	5.6 nF	Snubber resistance	3.3 Ω
Switching frequency	10 kHz	Input DC voltage	150 V
Load resistance	8.9 Ω	Load inductance	12.5 mH



(a) With PR current suppression control



(b) With PI current suppression control

Figure 4.31 Experimental waveforms for single-phase-leg 5-level MMC
(V_{ao}: 100 V/div; Currents: 2 A/div)

Simulation results for the two current suppression controllers are similar, as shown in Figure 4.16 and Figure 4.19. The experimental result of PI current suppression control, however, is better than that of PR control. Figure 4.31 (a) shows that with PR controller the circulating current contains third harmonics.

The following paragraphs will explain why the experimental results contain odd harmonics.

In the MATLAB simulation, all the submodules are identical. However, in the test rig there are individual differences among the submodule capacitors. In this case, the n^{th} harmonic capacity voltage $\Delta u_C^{(n)}(t)$ in (4-53) will not be the same for upper and lower arms. Therefore, (4-54) - (4-58) should be rewritten as (4-89) - (4-93).

The total submodule capacitor ripple voltages in upper and lower arm are given by (4-89) and (4-90).

$$\Delta V_{cu} = -V_{1u}\sin\omega t + V_{2u}\sin 2\omega t \tag{4-89}$$

$$\Delta V_{cl} = V_{1l}\sin\omega t + V_{2l}\sin 2\omega t \tag{4-90}$$

The ripple voltage of the submodule terminal is:

$$\Delta V_{au} = m_u \cdot \Delta V_{cu} = (\frac{1}{2} - \frac{M}{2}\cdot \sin\omega t)\cdot(-V_{1u}\sin\omega t + V_{2u}\sin 2\omega t) \tag{4-91}$$

$$\Delta V_{al} = m_l \cdot \Delta V_{cl} = (\frac{1}{2} + \frac{M}{2}\cdot \sin\omega t)\cdot(V_{1l}\sin\omega t + V_{2l}\sin 2\omega t) \tag{4-92}$$

Ripple voltage across the phase

$$\Delta V_a = \Delta V_{au} + \Delta V_{al} = \frac{1}{2}(V_{1l} - V_{1u})\sin\omega t + \frac{1}{2}\cdot[M(V_{1u} + V_{1l})\sin^2\omega t + (V_{2u} + V_{2l})\sin 2\omega t] + \frac{M}{2}\cdot(V_{2l} - V_{2u})\sin\omega t\sin 2\omega t \tag{4-93}$$

From (4-93), there are fundamental and 3rd harmonics in the ripple voltage across one phase. Those components will give rise to the even harmonics in the circulating current. Figure 4.32 shows the simulation results of circulating current suppression controller when the capacitors are not identical. From the FFT analysis of circulating current, the 2nd harmonic is almost eliminated, while the fundamental, 3rd (17.1%) and 4th (26.14%) harmonics are presented.

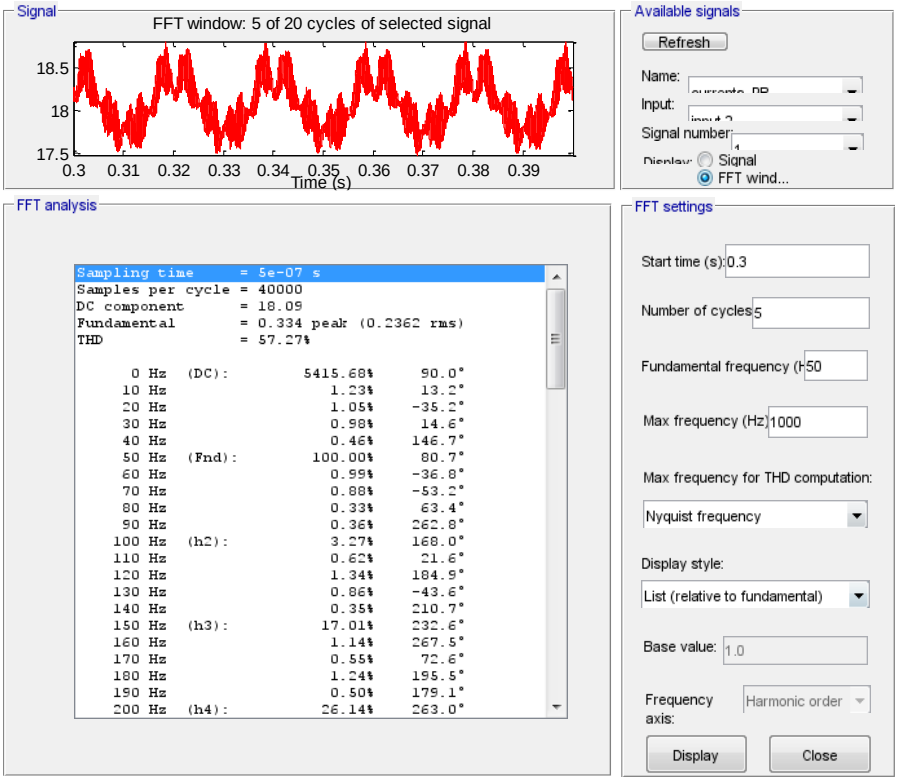


Figure 4.32 FFT analysis of circulating current with PR controller under unbalanced capacitors (1 mF difference between total upper and lower arm capacitance)

There are two possible reasons why the PI controller provides a better performance than PR controller. It might because PI controller has a larger bandwidth. For example, after the Park Transformation at 100 Hz, the third harmonic signal is converted into 50 Hz or 250 Hz. The PI controller may still has certain gains at these two harmonics which might help to suppress these harmonics.

In addition, the difference between these two controllers might be caused by the discretization method when implement the controller into DSP. Zero-Order Hold (ZOH) is employed for both controllers. For systems with time delays in feedback loops, the ZOH method leads to an approximate discretization rather than an exact discretization [112]. PR is a second order controller and the implementation of PR controller requires a relatively high sampling frequency. It is therefore sensitive to the discretization errors. However, for PI controller which is a first order controller, ZOH method is able to provide a better accuracy [113].

In conclusion, for practical single-phase low voltage MMC, PI controllers are better suited and easier to be implemented.

4.8 Summary

This chapter presented the overall converter design of MMC with experimental results for validation. In Section 4.3, submodule capacitor sizing method which is based on the peak to peak energy deviation is introduced. A case study concluded that the highest energy deviation happens when there is only the reactive power. Submodule capacitors can be sized according to this highest energy deviation. Calculation results illustrated that the required submodule capacitance is proportional to the number of levels if the power and load conditions are the same. MATLAB simulation results show that the capacitor voltages of a two-phase-leg 5-level MMC are well balanced and the voltage fluctuation is within ±10% limit, based on the sizing method used.

The arm inductor sizing method introduced in Section 4.4 is based on the limitation of circulating current at the switching frequency, since the 2^{nd} harmonic can be effectively eliminated by the current suppression controller. Results show that the required arm inductance is inversely proportional to the switching frequency and will not be influenced by the number of levels of MMC.

In order to meet the distortion limit, simulation results show that a small output AC filter is required for the low voltage MMC with less than 13 levels. The arm inductance can serve as part of the output filter. In Section 4.5, a parallel damped filter is designed for a 10 kHz two-phase-leg 5-level MMC.

Section 4.6 explains how switching action of submodule devices causes 2^{nd} harmonics to be generated, which were found to be doubled in two-phase-leg converters. A PR and PI with orthogonal imaginary axis current controllers were developed to eliminate the circulating current distortion. Simulation results presented a similar effect of both controllers since all the capacitors are identical. In addition, a closed-loop PR control was introduced to stabilise the output voltage during load changing transient. In Section 4.7, experimental results of PI controller are better

than that of PR controller. The reason might because PI controller has a larger bandwidth, or it might because of the discretization method when implement the controller into DSP. PR is a second order controller and is more sensitive to the discretization errors than the first order PI controller. The odd harmonics in the circulating current are caused by the parameter mismatch of different capacitors.

5. Power Loss Calculation

5.1 Introduction

As described in Chapter 3, MMC enjoys many benefits when compared with conventional 2-level converter, such as a reduced switching frequency, low *dv/dt* and reduced output harmonics which decreases the size of AC filters significantly. The converter whole-lifecycle cost is one of the major part in transmission and distribution applications, and it is dominated by power loss during normal operation. Therefore, this chapter evaluates the power loss performance for 2-level power converters and MMCs.

The emerging wide bandgap devices such as the silicon carbide (SiC) MOSFET and Gallium Nitride (GaN) high electron mobility transistors (HEMT) are attractive to LVDC applications due to their low power loss and high switching performance. In this chapter, comparative analysis is carried out among conventional 2-level IGBT converter, 2-level SiC MOSFET converter and Si MOSFET MMC and GaN HEMT MMC.

The comparison is first conducted between conventional 2-level converter and different levels of MOSFET MMC. The most favourable and practical levels of Si MOSFET MMC is determined in terms of losses and converter cost. In addition, the 2-level SiC converter, GaN HEMT MMC and Si MOSFET MMC with parallel-connected switches are discussed and compared. The optimal converter system is then chosen mainly from the perspective of efficiency and power quality.

The loss calculation of power converter is a complex procedure, including semiconductors' conduction and switching losses, input filter power losses for 2-level converters, and submodule capacitor losses for MMC. Conduction loss is affected by the junction temperature which should be taken into account. During parallel connection, the circuit track resistance must be considered. The inductor losses in MMC and conventional converters are discussed in Section 5.5.1. The

modulation index has a dramatic impact on the power loss, which will be discuss in Section 5.5.2.

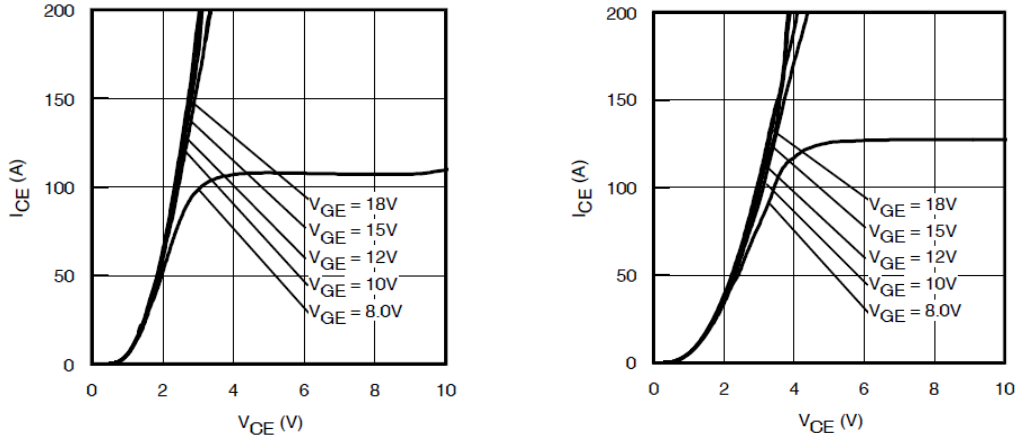
5.1.1 Conduction Losses

Due to the voltage drop across switching devices, the instantaneous power dissipation during conduction is the product of the on-state voltage and the on-state current:

$$P = V_{on} \cdot i_o \tag{5-1}$$

The device voltage is a function of the current and will be changed with junction temperature. The output characteristics of switching devices are given by the datasheet.

A. Conduction Loss for IGBT



(a) T_J=25 °C; t_P=30 µs (b) T_J=150 °C; t_P=30 µs

Figure 5.1 Typical IGBT Output Characteristics, *IRG7PSH50UDPbF (1.2 kV, 50 A)* [114]

Figure 5.1 shows the output characteristics of IGBT, where T_J denotes the operating junction temperature. Curve fitting is used to obtain the on-state voltage V_{CE} as a function of collector-emitter current I_{CE} at 25 °C and 150 °C (Equation (5-2) and (5-3)).

$$V_{on\_IGBT\_25} = V_{CE0} + I_{CE} \cdot R_{on\_25} \tag{5-2}$$

$$V_{on\_IGBT\_150} = V_{CE0} + I_{CE} \cdot R_{on\_150} \tag{5-3}$$

where R_{on} is the forward resistance of the device and V_{CE0} is the on-state collector-emitter voltage at zero current [115].

Assuming the R_{on} varies linearly with T_J between 25 °C and 150 °C, the on-state voltage can be expressed as (5-5) for any junction temperature T_J.

$$V_{on\_IGBT} = V_{CE0} + I_{CE} \cdot R_{on} \tag{5-4}$$

$$R_{on} = (R_{on\_150} - R_{on\_25}) \cdot \frac{T_J - 25}{150 - 25} + R_{on\_25} \tag{5-5}$$

The conduction loss of IGBT can be expressed as:

$$P_{con\_IGBT} = \frac{1}{T}\int_0^T V_{on}(t) \cdot i_{CE}(t)dt = \frac{1}{T}\int_0^T (V_{CE0} + i_{CE}(t) \cdot R_{on}) \cdot i_{CE}(t)dt \tag{5-6}$$

where T is the fundamental period.

B. Conduction Loss for MOSFET

The on-state voltage of MOSFET is given by (5-7).

$$V_{on\_MOSFET} = I_{DS} \cdot R_{on} \tag{5-7}$$

where I_{DS} is the drain-to-source current of MOSFET.

As shown in Figure 5.2, R_{on} increases with temperature because of the decreasing carrier mobility [93]. The on-resistance for T_J is given by (5-8), which is obtained from the Normalized On-Resistance vs. Temperature curve [116].

$$R_{on} = R_{on\_25} + k_{Ron} \cdot (T_j - 25) \tag{5-8}$$

where k_{Ron} is the temperature coefficient obtained from the curve and R_{on_25} is the on-resistance at 25°C.

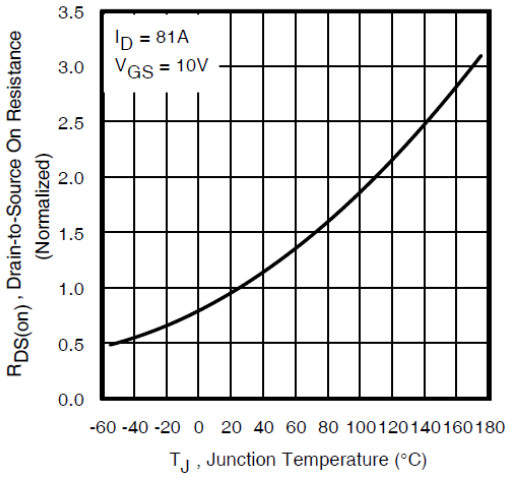


Figure 5.2 Normalized R_{on} vs. Temperature, *IRFP4668PbF (200 V, 130 A, 8 mΩ)* [117]

The conduction loss of MOSFET:

$$P_{con\_MOSFET} = \frac{1}{T}\int_0^T (i_{DS}(t) \cdot R_{on}) \cdot i_{DS}(t)dt \quad (5\text{-}9)$$

C. Conduction Loss for Diode

Diode I-V characteristics are similar to those of the IGBT and a linear approximation of an on-state voltage and resistance may be used. The on-state voltage of diode can be expressed as (5-10), where V_{F0} is the forward voltage drop across the diode with no load, and I_F is the diode forward current.

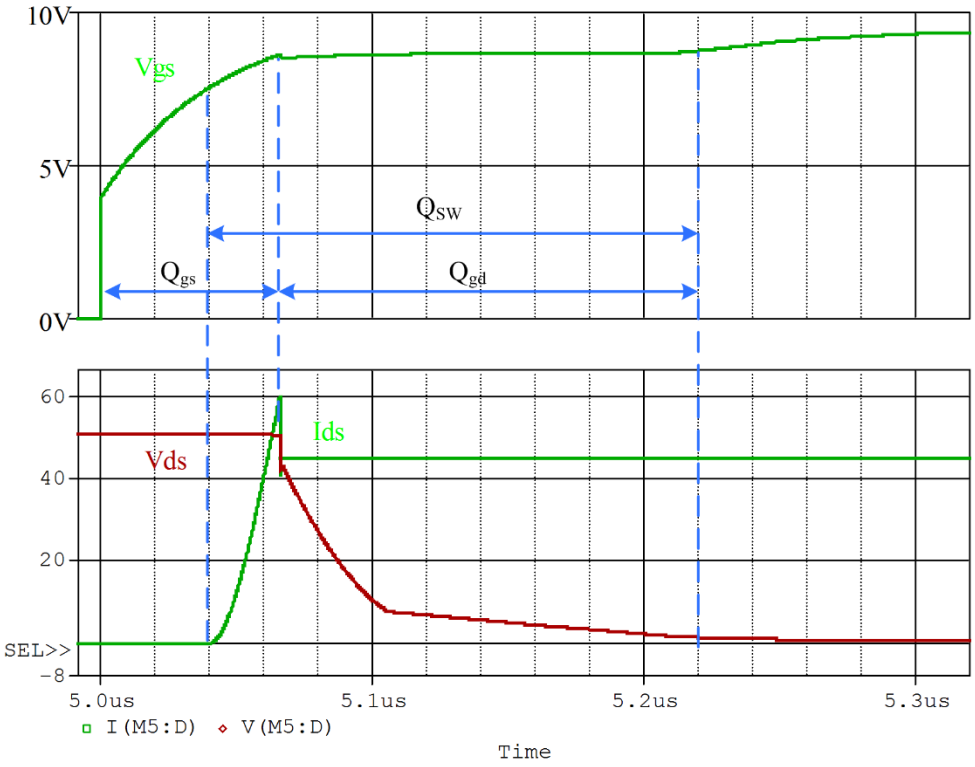
$$V_F = V_{F0} + I_F \cdot R_{on\_D} \quad (5\text{-}10)$$

Diode conduction losses can therefore be given by (5-11).

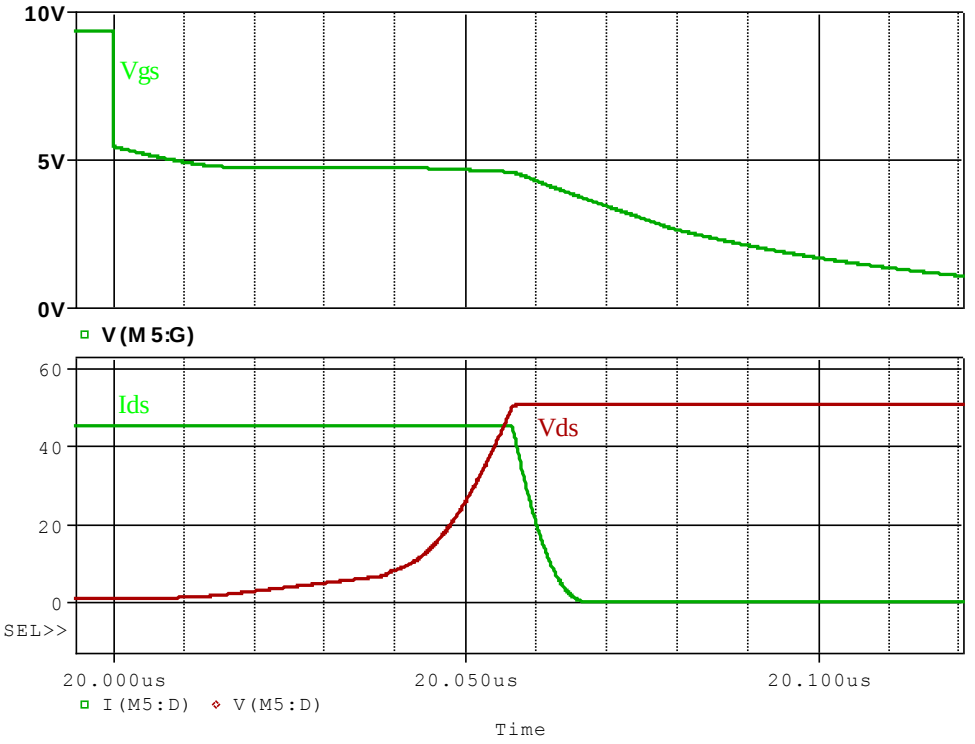
$$P_{con\_Diode} = \frac{1}{T}\int_0^T (V_{F0} + i_F(t) \cdot R_{on}) \cdot i_F(t)dt \quad (5\text{-}11)$$

5.1.2 Switching Losses

Switching loss is the power dissipation during turn-on and turn-off switching transitions. The most accurate method for switching loss calculation is to perform a time-integral of the instantaneous power dissipation during switching transitions, which is the product of current through and voltage across the devices. Typical plots of the drain current and drain-source voltage waveforms are shown in Figure 5.3, which can be used for this purpose. To simplify the calculation, however, the switching energy can be used for the estimation of IGBT switching power losses and switching gate charge for that of MOSFET switching power losses, since they can easily be obtained from manufacture datasheets. Curve fitting will be adopted to describe the changing of switching energy/charge with device current.



(a) Turn-on transient



(b) Turn-off transient

Figure 5.3 Pspice simulation result of MOSFET turn-on and turn-off transient

A. Switching Loss for IGBT

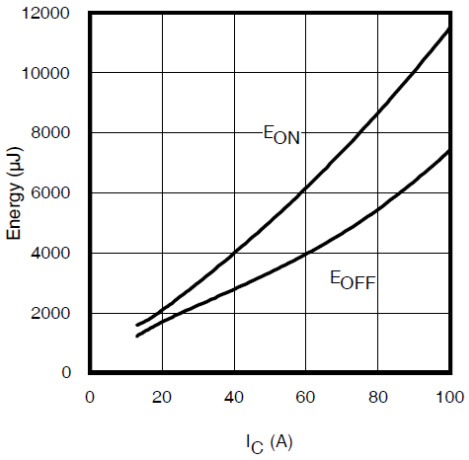


Figure 5.4 Typ. Energy loss vs. I_C
T_J = 150 °C; L = 200 µH; V_{CE} = 600 V,
R_G = 5.0 Ω. *IRG7PSH50UDPbF* [114]

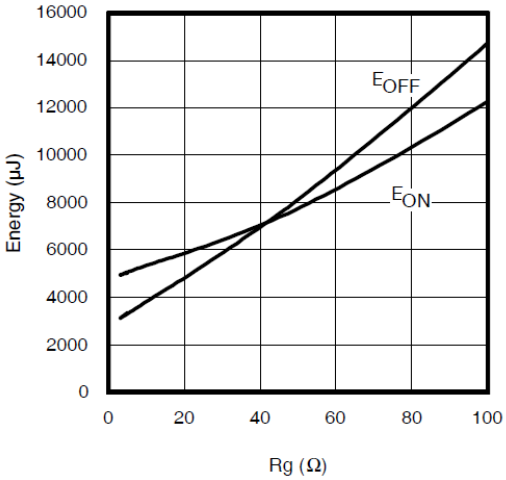


Figure 5.5 Typ. Energy loss vs. R_G
T_J = 150 °C; L = 200 µH; V_{CE} = 600 V,
I_{CE} = 50 A; V_{GE} = 15 V. *IRG7PSH50UDPbF*

The switching loss for IGBTs can be calculated by the product of energy loss and switching frequency. As shown in Figure 5.4, a curve fit is used to obtain the energy losses as a function of collector current. The energy loss can be given by (5-12) and (5-13).

$$E_{on} = K_{on\_0} + K_{on} \cdot I_{CE} \tag{5-12}$$

$$E_{off} = K_{off\_0} + K_{off} \cdot I_{CE} \tag{5-13}$$

where K_{on_0} and K_{off_0} are the offsets, K_{on} and K_{off} are the gradients obtained from the curve fitting of the E_{on} and E_{off} respectively.

The switching energy losses also vary with the gate resistance, as indicated in Figure 5.5. If R_G is not 5 Ω, the energy loss needs to be modified accordingly.

$$\begin{aligned} P_{SW_{IGBT}} &= \left(E_{on} + E_{off}\right) \cdot f_s \\ &= \frac{1}{T}\int_0^T \left[\left(K_{on\_0} + K_{off\_0}\right) + \left(K_{on} + K_{off}\right) \cdot i_{CE}(t)\right] \cdot f_s dt \end{aligned} \tag{5-14}$$

B. Switching Loss for MOSFET

MOSFET switching losses can be simply expressed as (5-15) [118].

$$P_{SW\_MOSFET} = \frac{1}{2} I_{DS} V_{DS} \left(t_{off} + t_{on}\right) f_s \tag{5-15}$$

where t_{on} and t_{off} are the turn-on and turn-off time respectively, which can be obtained from (5-16) and (5-17)

$$t_{on} = t_{off} = \frac{Q_{SW}}{I_{GS}} \tag{5-16}$$

$$Q_{SW} = Q_{gs2} + Q_{gd} = \frac{V_{gs(pl)} - V_{gs(th)}}{V_{gs(pl)}} Q_{gs} + Q_{gd} \tag{5-17}$$

where Q_{SW} is the switching gate charge increment required as gate voltage increases from its threshold value to the end of its plateau level [119], as shown in Figure 5.3 (a), and I_{GS} is the average gate current. As illustrated in Figure 5.6, Q_{gs} is the gate to source charge, Q_{gd} is the gate to drain 'Miller' charge, $V_{gs(pl)}$ is the gate plateau voltage, and $V_{gs(th)}$ is the gate threshold voltage

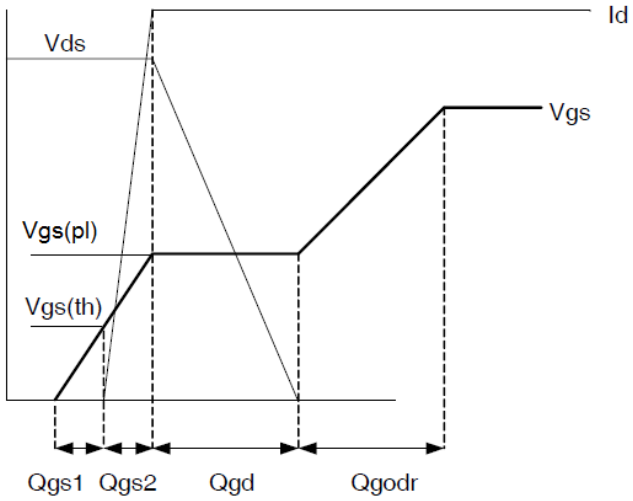


Figure 5.6 Si MOSFET Gate Charge Waveform

The Miller plateau gate current is used to approximate the average gate current I_{GS}, which is given by (5-18), where V_{GS} is the applied gate drive voltage, and R_g is the total gate resistance.

$$I_{GS} = \frac{V_{GS} - V_{gs(pl)}}{R_g} \tag{5-18}$$

Switching parameters provided by the datasheet are measured under certain voltage V_{test} and current I_{test}. Assuming gate charge parameters change linearly with the drain-source voltage and current, the switching loss can be expressed as (5-19).

$$P_{SW\_MOSFET} = \frac{1}{T}\int_0^T {V_{DS}}^2 \cdot {i_{DS}}^2 \cdot \left(\frac{Q_{SW}/I_{GS}}{I_{test} \cdot V_{test}}\right) \cdot f_s \, dt \tag{5-19}$$

C. Switching Loss for Diode

The diode can be considered as an ideal switch at turn-on, since it turns on rapidly compared to the self-commutated switches. The switching loss of the diode can be attributed to the reverse-recovery power loss. For datasheets which provide the diode reverse recovery energy loss curve (Figure 5.7), curve fitting can be applied to get the average energy loss (5-20).

$$P_{SW\_D} = E_{rr} \cdot f_s = \frac{1}{T}\int_0^T \left(K_{rr\_0} + K_{rr} \cdot i_F(t)\right) \cdot f_s dt \tag{5-20}$$

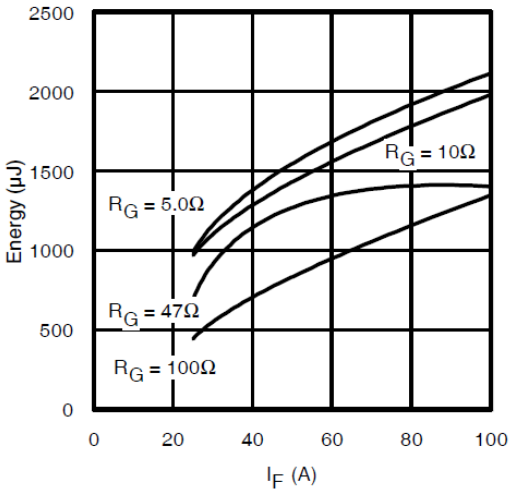


Figure 5.7 Diode E_{RR} vs. I_F, T_J=150 °C, *IRG7PSH50UDPbF(1.2 kV, 50 A)* [114]

There is no reverse recovery energy loss curve provided for the body diode of the MOSFET. Hence the reverse recovery charge Q_{rr} is used to calculate the loss (5-21).

$$P_{rr\_D} = \frac{1}{T}\int_0^T \frac{Q_{rr}}{I_{test} \cdot V_{test}} \cdot {V_{DS}}^2 \cdot i_F \cdot f_s dt \quad (5\text{-}21)$$

5.1.3 Comparison Setup

Typically, consumer-end converters require single phase, 240 Vac, 10 kW per household [120]. The DC link voltage is selected to be 600 V in Chapter 2. Single-phase-leg converter can only provide an output voltage up to 212 Vrms, unless third harmonic injection is applied. Therefore, the 2-phase-leg converters are adopted to provide increased voltage output. The topologies are either MMC with HBSM or 2-level converter. Parameters for the power loss calculation are summarized in Table 5.1.

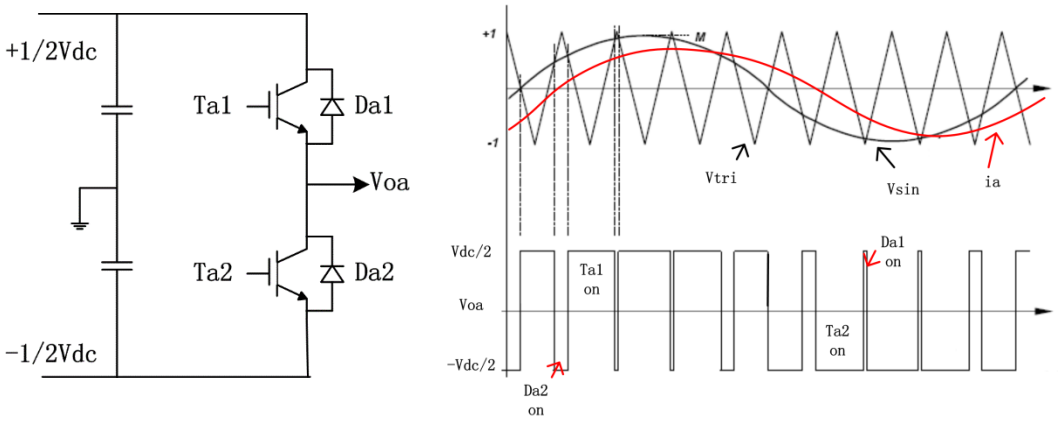
Table 5.1 Parameters for 10 kW customer-end converters

Input Voltage (Vdc)	600 V	Output Voltage (Vo)	240 V
Modulation Index (*M*)	0.57	Iapk	58.9 A
Power Factor	1	Idc (one phase)	8.33 A
Output Power	10 kW	R	5.76 Ω

5.2 Power Losses of Conventional 2-level Converter

5.2.1 Operating Principle

Figure 5.8 shows the topology for one phase of a conventional, IGBT-based 2-level converter. Sinusoidal-pulse-width-modulation (SPWM) is used to control the magnitude and frequency of the output. As illustrated in Figure 5.8 (b), a control signal v_{sin} is compared with a triangular waveform v_{tri} which determines the switching frequency to generate the switching signals. In this way, the duty cycle of each switch can be modulated, resulting in a controlled average output voltage.



(a) Half-bridge of a 2-level Converter (b) PWM control for 2-level converter

Figure 5.8 Topology and PWM control of half-bridge 2-level converter

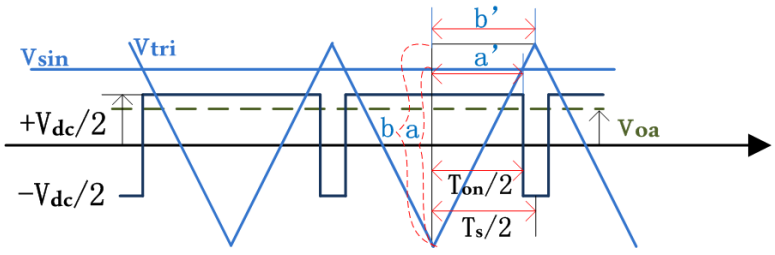


Figure 5.9 Sinusoidal PWM

Assuming that the carrier is a triangle wave from -1 to 1, and the modulation signal and load current are defined as (5-22) and (5-23) respectively.

$$v_{sin} = M \cdot \sin \omega t \tag{5-22}$$

$$i_a = I_o \sin(\omega t - \varphi) \tag{5-23}$$

where M is the amplitude modulation index, defined as the ratio of the peak amplitude of the modulation signal v_{sin} divided by the peak amplitude of v_{tri}.

Switches T_{a1} and T_{a2} are operated in a complementary manner and the output voltage v_{oa} fluctuates between $+\frac{1}{2}Vdc$ and $-\frac{1}{2}Vdc$. Assuming the switching frequency is much faster than the fundamental frequency, the modulation signal v_{sin} can be treated as a constant value over one switching period as shown in Figure 5.9. The duty ratio of switch T_{a1} and T_{a2} can be deduced as (5-25) and (5-26).

$$\frac{T_{on}}{T} = \frac{a'}{b'} = \frac{a}{b} = \frac{v_{sin}+1}{2} = \frac{1}{2} + \frac{1}{2}M \cdot \sin \omega t \tag{5-24}$$

$$d_{a1} = \frac{1}{2} - \frac{1}{2}M \cdot \sin \omega t \tag{5-25}$$

$$d_{a2} = \frac{1}{2} + \frac{1}{2}M \cdot \sin \omega t \tag{5-26}$$

The output voltage is therefore given by

$$v_{oa} = \frac{V_d}{2} - d_{a1} \cdot \frac{V_d}{2} = \frac{T_{on}}{T}V_d - \frac{V_d}{2} = \frac{1}{2}M \cdot \sin \omega t \cdot V_d \tag{5-27}$$

The conduction time for switch T_{a1} and T_{a2} over the carrier period T_s is $d_{a1} \cdot T_s$ and $(1 - d_{a1}) \cdot T_s$ respectively.

5.2.2 Conduction Loss

As shown in Figure 5.8 (b),

when $i_a>0$ ($\phi \leq \omega t < \pi+\phi$), T_{a1} and D_{a2} conducts;
when $i_a<0$ ($\pi+\phi \leq \omega t < 2\pi+\phi$), D_{a1} and T_{a2} conducts.

Based on (5-6) and (5-11), the average conduction losses for the IGBT and diode can be estimated by (5-28) to (5-31).

$$\bar{P}_{cond\_Ta1} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} d_{a1} \cdot (i_a^2 \cdot R_{on} + V_{CE0} \cdot i_a) d(\omega t) \quad (5\text{-}28)$$

$$\bar{P}_{cond\_Da1} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} d_{a1} \cdot (i_a^2 \cdot R_{on\_D} + V_{f0} \cdot i_a) d(\omega t) \quad (5\text{-}29)$$

$$\bar{P}_{cond\_Ta2} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} d_{a2} \cdot (i_a^2 \cdot R_{on} + V_{CE0} \cdot i_a) d(\omega t) \quad (5\text{-}30)$$

$$\bar{P}_{cond\_Da2} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} d_{a2} \cdot \left(i_a^2 \cdot R_{on\_D} + V_{f0} \cdot i_a\right) d(\omega t) \quad (5\text{-}31)$$

5.2.3 Switching Loss

According to (5-14) and (5-20), the switching losses of T_{a1} and D_{a1} are given by (5-32) and (5-33) respectively.

$$\begin{aligned} P_{SW_{Ta1}} &= P_{SW_{Ta2}} \\ &= \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} \left[\left(K_{on\_0} + K_{off\_0}\right) + \left(K_{on} + K_{off}\right) \cdot i_a\right] \cdot f_s d(\omega t) \end{aligned} \quad (5\text{-}32)$$

$$P_{SW\_Da1} = P_{SW\_Da2} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} \left(K_{rr\_0} + K_{rr} \cdot i_a\right) \cdot f_s d(\omega t) \quad (5\text{-}33)$$

5.2.4 Input DC Capacitor Power Losses

For 10 kW H-bridge converter, a DC input capacitor is required. The average energy stored in the input capacitor is expressed in (5-34) , where V_{dc} is the nominal voltage.

$$E_{dc} = C_{dc} \cdot V_{dc}^2 \quad (5\text{-}34)$$

The peak to peak energy deviation is given by (5-35)

$$\Delta E_{dc} = C_{dc} \cdot [V_{dc}(1 + \Delta V_{max})]^2 - C_{dc} \cdot [V_{dc}(1 - \Delta V_{max})]^2 \quad (5\text{-}35)$$

Therefore, the minimal submodule capacitance can be derived as (5-36).

$$C_{dc} = \frac{\Delta E_{dc}}{4{V_{dc}}^2 \cdot \Delta V_{max}} \quad (5\text{-}36)$$

The upper arm current arm current can be obtained from (5-37).

$$i_{up} = \left(\frac{1}{2} + \frac{1}{2}M \cdot \sin\omega t\right) \cdot I_a \sin(\omega t - \varphi) \quad (5\text{-}37)$$
$$= \frac{1}{4}MI_a \cos\varphi + \frac{1}{2}I_a \sin(\omega t - \varphi) - \frac{1}{4}MI_a \cos(2\omega t - \varphi)$$

Assuming all AC components are drawn from the capacitor, the capacitor current is expressed as (5-38).

$$i_{Cdc} = \frac{1}{2}I_a \sin(\omega t - \varphi) - \frac{1}{4}MI_a \cos(2\omega t - \varphi) \quad (5\text{-}38)$$

The DC side current is expressed as (5-39).

$$I_{dc} = \frac{1}{4}MI_a \cos\varphi \quad (5\text{-}39)$$

The capacitor power is given by (5-40), where S denotes the converter apparent power, $S=P/\cos\varphi=V_{dc}I_{dc}/\cos\varphi$.

$$P_{Cdc}(t) = V_{dc} \cdot i_{Cdc} = \frac{2|S|}{M}\left[\sin(\omega t - \varphi) - \frac{M}{2}\cos(2\omega t - \varphi)\right] \quad (5\text{-}40)$$

Energy stored in the DC link capacitor can be calculated by the integral of P_{Cdc} and time, which is given by (5-41)

$$E_{dc} = \int P_{Cdc}(t)\,dt = \frac{|S|}{2\omega M}[M \cdot \sin(\varphi - 2\omega t) - 4\cos(\varphi - \omega t)] \quad (5\text{-}41)$$

For the customer-end converter described in Section 5.1.3, when M=0.57, the change of capacitor energy in one fundamental period can be plotted in Figure 5.10. It shows that the peak to peak energy deviation ΔE_{dc} doesn't change much with load angle (φ).

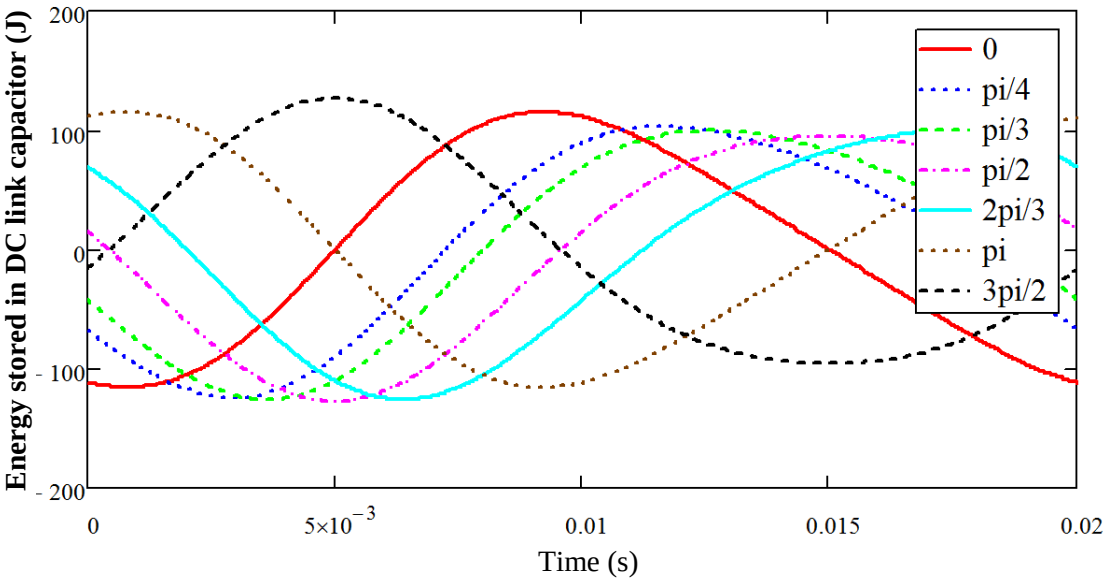


Figure 5.10 The energy stored in the DC link capacitor, with 50 Hz, S=10VA, *M=0.57*, and φ changing from *0* to *1.5π*.

Assuming *M*=0.57 and $\varphi=0$, ΔE_{dc} can be obtained by integrating P_{Cdc} from *t1* to *t2*, where *t1* and *t2* are the crossing 0 points of P_{Cdc}.

$$\Delta E_{dc} = \int_{t1}^{t2} P_{Cdc}(t)\, dt = \frac{2|S|}{0.57} \cdot 6.6 \cdot 10^{-3} = 232J \tag{5-42}$$

According to [121] and Matlab simulation results, to meet 5% current ripple limitation, 65 mH input inductor is required when $\Delta V_{max}=0.1$ *p.u.*, while 6.5mH input inductor is required when $\Delta V_{max}=0.01$ *p.u.*. It means when the DC ripple is smaller, the required input inductance is smaller. Therefore, ΔV_{max} is set to be 0.01 p.u. in this study to avoid a bulky input inductance. The required capacitance can be obtained by using (5-36).

$$C_{dc} = \frac{\Delta E_{dc}}{4{V_{dc}}^2 \cdot \Delta V_{max}} = 16mF \tag{5-43}$$

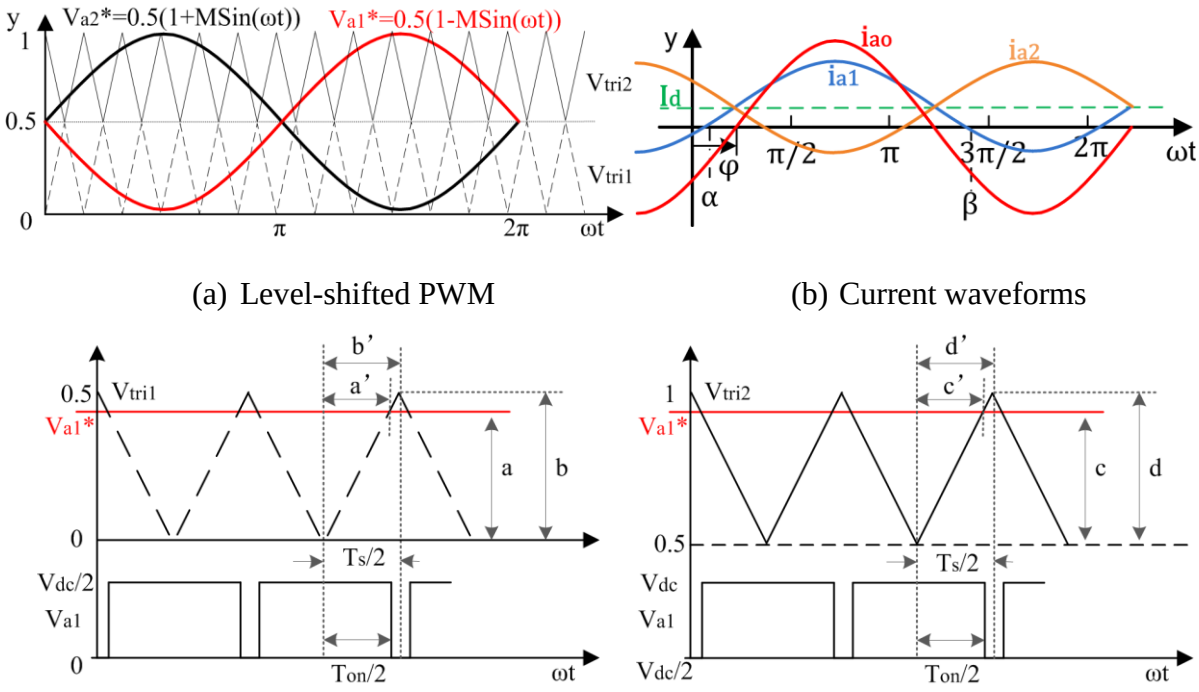
Power dissipated in the submodule capacitor can be estimated by the product of equivalent series resistance (ESR) and the square of charging current [122]. DC link capacitor power loss is given by (5-44), where R_{ESR} is the ESR of submodule capacitor.

$$\bar{P}_{cap} = \frac{1}{2\pi}\int_0^{2\pi} i_{Cdc}^2 \cdot R_{ESR} d(\omega t) \tag{5-44}$$

5.3 Power Losses of MOSFET-based MMC

5.3.1 Duty Cycle Calculation

To calculate the power losses of each device, it is very important to know the duty cycle for each switch first. In this section, the level-shifted PWM (Figure 5.11 (a)) is applied and all capacitor voltages are assumed to be balanced. 3-level MMC (Figure 5.12) is employed to explain the duty cycle calculation.



(a) Level-shifted PWM (b) Current waveforms

(c) $0 \leq \omega t < \pi$, upper arm (d) $\pi \leq \omega t < 2\pi$, upper arm

Figure 5.11 Level-shifted PWM control for 3-level MMC converter

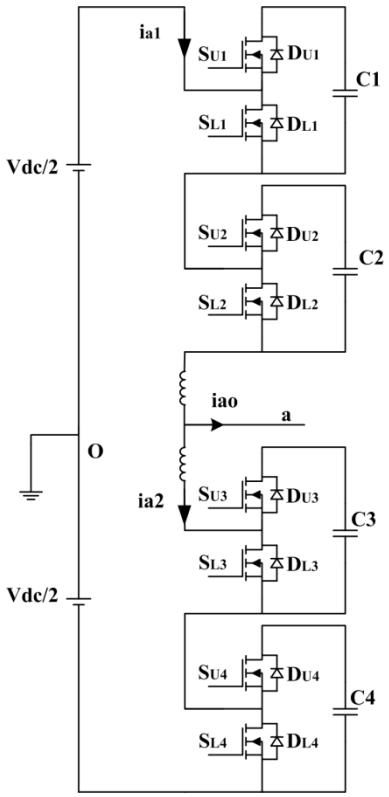


Figure 5.12 One phase leg of 3-level MMC

With 2 submodules in one arm, the arm voltages have 3 output levels: *0, $V_{dc}/2$* or *V_{dc}*, which are summarized in Table 5.2.

Table 5.2 Submodule Status

V_{a1}	**Duty Ratio***	**Submodule Status**	**Gate Signal for S_{U1} (or S_{U2})**	**Possibility for S_{U1} (or S_{U2}) to be '1'**
0	d_0	Both are bypassed	Both are '0'	$C_{SU0} = 0$
$V_{dc}/2$	d_1	One is inserted and one is bypassed	One is '0' and one is '1'	$C_{SU1} = 1/2$
V_{dc}	d_2	Both are inserted	Both are '1'	$C_{SU2} = 1$

*Duty ratio relating to the corresponding arm voltage value.

As illustrated in Figure 5.11 (c), the upper arm voltage V_{a1} has two states (*0* or $V_{dc}/2$) during the interval $0 \le \omega t < \pi$. The duty ratio d_1 and d_0 relating to state $V_{dc}/2$ and *0* respectively can be deduced as (5-45) and (5-46), where T_S is the switching period.

$$d_1 = \frac{T_{on}/2}{T_s/2} = \frac{a'}{b'} = \frac{a}{b} = \frac{V_{a1}^*}{V_{tri1}} = \frac{0.5 - 0.5 \cdot M \cdot \sin \omega t}{0.5} = 1 - M \cdot \sin \omega t \qquad (5\text{-}45)$$

$$d_0 = 1 - d_1 = M \cdot \sin \omega t \qquad (5\text{-}46)$$

According to Table 5.2, only one submodule is inserted when $V_{a1}= V_{dc}/2$. The probability for SM1 to be chosen is given by (5-47).

$$C_{SU1} = \frac{1}{C_1^2} = \frac{1}{2} \tag{5-47}$$

where C_x^m is the number of possible combinations of x items chosen from a set of m items at a time without repetition.

Therefore, during $0 \leq \omega t < \pi$, the duty cycle of switch S_{U1} (or S_{U2}) is expressed as (5-48).

$$d_{SU} = C_{SU0} \cdot d_0 + C_{SU1} \cdot d_1 = \frac{1}{2}(1 - M \cdot \sin \omega t), \quad 0 \leq \omega t < \pi \tag{5-48}$$

Similarly, the upper arm voltage V_{a1} has two states (V_{dc} and $V_{dc}/2$) during the interval $\pi \leq \omega t < 2\pi$. Duty ratios $d2$ and $d1$ relating to states V_{dc} and $V_{dc}/2$ are provided by (5-49) and (5-50) respectively.

$$d_2 = \frac{T_{on}/2}{T_s/2} = \frac{c'}{d'} = \frac{c}{d} = \frac{V_{a2}{}^* - 0.5}{V_{tri2}} = \frac{0.5 - 0.5 \cdot M \cdot \sin \omega t - 0.5}{0.5} = -M \cdot \sin \omega t \tag{5-49}$$

$$d_1 = 1 - d_2 = 1 + M \cdot \sin \omega t \tag{5-50}$$

The duty cycle of switch $S_{U1/2}$ during $\pi \leq \omega t < 2\pi$ is therefore can be deduced as (5-51).

$$d_{SU} = C_{SU1} \cdot d_1 + C_{SU2} \cdot d_2 = \frac{1}{2}(1 - M \cdot \sin \omega t), \quad \pi \leq \omega t < 2\pi \tag{5-51}$$

In summary, the duty cycles for switch S_{U1} (or S_{U2}) and S_{L1} (or S_{L2}) are given by (5-52) and (5-53).

$$d_{SU} = \frac{1}{2}(1 - M \cdot \sin \omega t) \tag{5-52}$$

$$d_{SL} = 1 - d_{SU} = \frac{1}{2}(1 + M \cdot \sin \omega t) \tag{5-53}$$

Where more than three levels are used, duty cycles for switches S_U and S_L in one cell are the same. Switch S_{Ui} is on means the corresponding submodule is inserted. Therefore, d_{SU} is the same as the modulation signal for the arm V_{a1}*, which is shown in (4-5).

5.3.2 Conduction and Switching Loss

As illustrated in Section 3.4.1, due to the synchronous rectification, MOSFETs conduct the whole period except dead times when the body diodes conduct. Since the dead time is only 2% of the switching period, the diode conduction loss can be ignored. As shown in Figure 5.11 (b), D_{U12} would be switched on and off at dead times when $i_{a1}>0$ $(\omega t: \alpha \rightarrow \beta)$, while D_{L12} would be switched on and off at dead times when $i_{a1}<0$ $(\omega t: \beta \rightarrow 2\pi+\alpha)$. The power losses of one submodule MMC can be given by (5-54) - (5-59).

$$\bar{P}_{cond\_MU} = \frac{1}{2\pi}\int_0^{2\pi} d_{SU} \cdot (i_{a1}^2 \cdot R_{on\_M}) d(\omega t) \tag{5-54}$$

$$\bar{P}_{cond\_ML} = \frac{1}{2\pi}\int_0^{2\pi} d_{SL} \cdot (i_{a1}^2 \cdot R_{on\_M}) d(\omega t) \tag{5-55}$$

$$\bar{P}_{sw\_DU} = \frac{1}{2\pi}\int_\alpha^\beta \frac{Q_{rr}}{I_{test} \cdot V_{test}} \cdot {V_C}^2 \cdot i_{a1} \cdot f_s \, d(\omega t) \tag{5-56}$$

$$\bar{P}_{sw\_DL} = \frac{1}{2\pi}\int_\beta^{2\pi+\alpha} \frac{Q_{rr}}{I_{test} \cdot V_{test}} \cdot {V_C}^2 \cdot i_{a1} \cdot f_s \, d(\omega t) \tag{5-57}$$

$$\bar{P}_{sw\_MU} = \frac{1}{2\pi}\int_0^{2\pi} {V_C}^2 \cdot {i_{a1}}^2 \cdot \left(\frac{Q_{SW}/I_{GS}}{I_{test} \cdot V_{test}}\right) \cdot f_s \, d(\omega t) \tag{5-58}$$

$$\bar{P}_{sw\_ML} = \bar{P}_{sw\_MU} \tag{5-59}$$

5.3.3 Capacitor Power Loss

In high voltage applications, film power capacitors are often used as the benefit from low dissipation factor (DF). The low equivalent series resistance (ESR) allows high AC currents without significant increases in temperature. For lower voltage applications, in the range of several hundred voltes, electrolytic capacitors are another option. In comparison, the ESR of electrolytic power capacitors is much higher, but the volume and weight are significantly smaller than that of film capacitors.

The film capacitors in the market are usually for DC link applications which can stand high power, like the last two examples in Table 5.3. For 2 mF capacitors, the film capacitors are approximately 6 times heavier and 7 times larger than electrolytic capacitor. There are no products available in the market for lower power rating which is suitable for the low-voltage MMC application. The capacitor value in

second row is estimated by capacitor company *API capacitors*. Even in this estimated case, the weight and volume of film capacitors are still twice of the electrolytic one. However, ESR of film capacitors is about 30 times smaller than that of electrolytic capacitor.

Table 5.3 Comparison between electrolytic and film capacitors

	Capacitance(μF)	**Voltage (V)**	**Weight (g)**	**Volume (cc)**	**ESR (mΩ)**	**Part number**
Electrolytic	2200	350	280	221	28	B43456A4228M000
Film	2300	250	370	420	0.8	Estimated by *API capacitors**
	2400	450	1985	1613	0.2	DCHCH07240JH00KS00
	2030	600	1760	1480	1.6	DCP6I07203ER00

*There is no product for sale. These values are estimated by API capacitors company [123].

Power dissipated in the submodule capacitor can be estimated in the similar way as MOSFET conduction loss. Capacitor power losses in upper and lower arm are given by (5-61) and (5-61) respectively, where R_{ESR} is the ESR of submodule capacitor.

$$\bar{P}_{cap\_U} = \frac{1}{2\pi}\int_0^{2\pi} d_{SU} \cdot (i_{a1}^2 \cdot R_{ESR}) d(\omega t) \tag{5-60}$$

$$\bar{P}_{cap\_L} = \frac{1}{2\pi}\int_0^{2\pi} d_{SL} \cdot (i_{a2}^2 \cdot R_{ESR}) d(\omega t) \tag{5-61}$$

5.3.4 With Paralleling MOSFETs

Section 3.4.2 demonstrated that the currents among parallel-connected devices can be shared equally in static state. Therefore, when calculating the power losses, the expression for R_{on} (Equation (5-41)) can be modified accordingly by dividing by m, where m is the number of parallel-connected devices. The parasitic resistance of track and solder joints must be considered as well, especially for very low R_{on}.

In [89], it is estimated that parasitic track resistance is composed of two parts: 0.2 mΩ (R_{DS}) for individual device drain connecting to the p joint and source to the n joints in Figure 3.18, and 0.4 mΩ (R_L) from p and n joints to the main bus. Therefore, the total on-state resistance including track resistance can be given by (5-62).

$$R_{on} = 0.4 + \frac{1}{m}\left(R_{on_{25}} + k_{Ron} \cdot \left(T_j - 25\right) + 0.2\right)\ \text{m}\Omega \qquad (5\text{-}62)$$

5.3.5 Loss Comparison between Different Levels of Si MOSFET MMC

The loss comparison in this section includes the semiconductor losses and capacitor losses. The devices are chosen to meet the voltage and power rating, whilst minimising R_{on} as the conduction losses dominate in MMC power loss. Table 5.4 summarizes the devices parameters for different levels of converters. It shows the R_{on} of MOSFETs increases significantly with junction temperature T_j. The switching loss of MOSFETs is affected by T_j as well. In addition, Table 5.4 shows that R_{on} of 400 V MOSFET is significantly larger than those equal or under 200 V MOSFETs. Calculation results indicate that power loss of 3-level MOSFET-based MMC is higher than that of conventional 2-level converter. Therefore, in the following analysis, the 3-level MOSFET-based MMC would not be taken into consideration.

As presented in Equation (5-43), the required DC side capacitance for 2-level converter is 16 mF. Therefore, 18 mF capacitors are chosen for 2-level IGBT converter. According to (4-24), the required submodule capacitances for different levels of 2-phase-leg MMC at M=0.57 (240 V output) are summarized in Table 5.5.

Table 5.4 IGBT and MOSFET Parameters for different levels of converters

No. of Levels	**2-level**	**No. of Levels**	**3-level**	**5-level**	**7-level**	**9-level**
Device	IRG7PSH50 UDPbF	**Device**	IRFP360	IRFP4668	IRFP4568	IRFP4110
V_{CES}[a]	1200 V	V_{DSS}[b]	400 V	200 V	150 V	100 V
V_{CE0}@25°C	1.06 V	R_{on} @25°C	200 mΩ	8 mΩ	4.8 mΩ	3.7 mΩ
R_{on}[a] @25°C	13.5 mΩ	R_{on} @80°C	320 mΩ	12.8 mΩ	7.44 mΩ	4.9 mΩ
V_{CE0}@150°C	1.35 V	R_{on} @125°C	450 mΩ	17.6 mΩ	10.1 mΩ	6.9 mΩ
R_{on}[a] @150°C	15.5 mΩ	Q_{rr}[c]@25°C	5600 nC	633 nC	515 nC	94 nC
		Q_{rr} @125°C	--	944 nC	758 nC	140 nC

[a] V_{CES}: IGBT Maximum Collector-to-Emitter Voltage
[b] V_{DSS}: MOSFET Maximum Drain-to-Source Voltage
[c] Q_{rr}: MOSFET anti-parallel diode reverse recovery charge

Table 5.5 Comparison of capacitance requirements for different levels of converter

No. of Levels	Required Input C_{dc}(mF)	Capacitance (mF)	Manufacturer Part No	ESR (mΩ)	Capacitor Loss (W)*
2-level	16	18	B43456A4189M000	5	2.3
	Required C_{sub}				
3-level	1.6	2.2	B43456A4228M000	28	20.4
5-level	3.1	3.3	B43456A4338M000	20	29.2
7-level	4.7	4.7	B43456A4478M000	15	32.8
9-level	6.2	6.8	B43456A4688M000	12	35

*Capacitor loss for 2-phase-leg converter

Table 5.6 Comparison of semiconductor and capacitor cost of different 10 kW 2-phase-leg converters

No. of Levels	Manufacturer Part No Capacitor	Quantity	Price (£)	Manufacturer Part No Devices	Quantity	Price (£)	Total price (£)
2-level	B43456A4189M000	4	622.28	IRG7PSH50UDPbF	4	27.72	650.0
5-level	B43458A9338M	16	749.6	IRFP4668	32	116.8	866.4
	With 2 parallel-connected MOSFETs				64	233.6	983.2
7-level	B43456A4478M000	24	1043.3	IRFP4568	48	224.2	1267.4
	With 2 parallel-connected MOSFETs				96	343	1386.3
9-level	B43456A4688M000	32	3,096	IRFP4110	64	132.5	3228.5
	With 2 parallel-connected MOSFETs				128	235.5	3332.0

According to the calculation methods introduced in Section 5.2, power losses of a conventional 2-level IGBT converter and Si MOSFET MMCs with different numbers of levels are presented in Figure 5.13 and Table 5.5. It illustrates that with increasing number of levels, capacitor power losses in MMC are almost constant, while conduction and switching losses decrease gradually. In particular, with parallel-connection (Figure 3.18) of 2 MOSFETs the conduction loss reduces dramatically. Therefore, the potential performance improvements and practicalities of parallel-connected MOSFETs are to be investigated.

Table 5.6 shows the capacitor and semiconductor devices cost for different levels of converters. For 2-level converter, 2 capacitors are needed to be connected in series to

build up the DC voltage. The capacitance will reduce to half of its original value accordingly. Therefor another two capacitors are connected in parallel to increase the total capacitance. Hence 4 capacitors are required for the conventional 2-level converter.

Figure 5.13 shows that the cost of converters rises dramatically with the increased converter levels. In particular the capacitor cost increases significantly and dominates the overall cost as shown in Table 5.6. The control complexity and volume will be increased as well. In addition, capacitor loss is becoming the dominate factor among the overall power loss. Therefore, increasing the number of levels is not a promising way to improve the efficiency. For further studies, a 5-level MMC with parallel-connected Si MOSFETs is considered because it provides a good balance between control complexity, losses and cost.

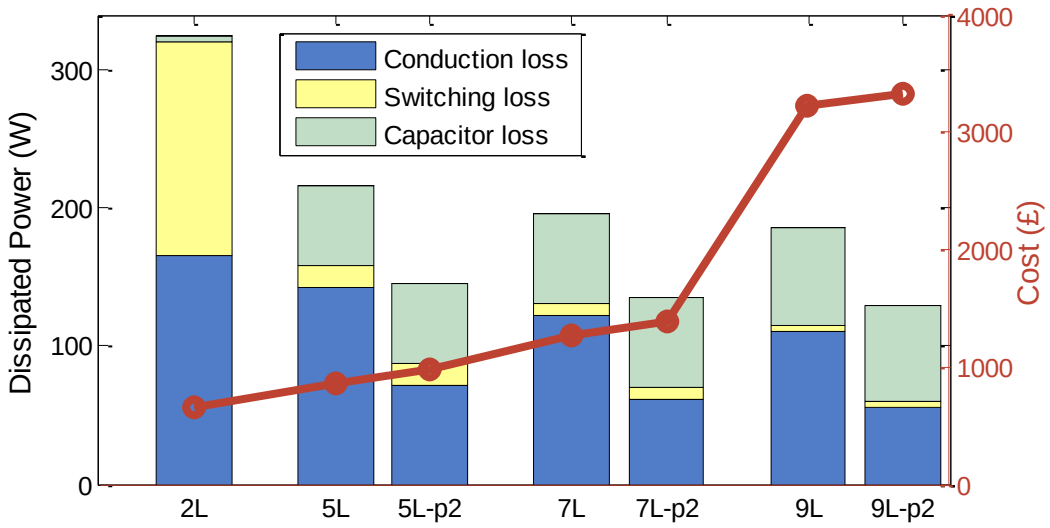


Figure 5.13 Power loss and cost comparison for H-bridge 2-level IGBT converter and different levels of Si MOSFET MMC at M=0.57, 10 kHz, 10 kW and unity power factor. 2L=2 level IGBT; 5L/7L/9L= 5/7/9 level MMC without parallel connection; 5L-p2/7L-p2/9L-p2= 5/7/9 level MMC with 2 parallel-connected devices

5.4 Wide Bandgap Devices Based Converters

Silicon carbide (SiC) and gallium nitride (GaN) are from the family of materials known as wide bandgap semiconductors. The crystal bonds of these are stronger than

that of silicon and a larger energy is required for electrons to cross the bandgap. These, therefore have a much smaller leakage current and can withstand much higher temperatures than the silicon devices [124].

5.4.1 SiC MOSFET 2-level Converter

Comparing with Si devices, the drift-layer resistance of SiC devices is much lower. Therefore, SiC devices can achieve a low R_{on} which mitigates the conduction loss. Unlike IGBTs, MOSFETs feature no tail current, which reduces turn-off switching loss. In comparison with Si MOSFETs, the body diode of SiC MOSFETs has an ultralow reverse recovery loss as the body diode is a PN junction diode, which has short minority carrier lifetime. The recovery current is primarily to discharge the junction capacitance, again helping to reduce losses [124].

Among the available choices of SiC MOSFETs in the market, the R_{on} and devices' conduction loss do not reduce at lower voltage rating. For LVDC application at 600 Vdc, 2-level SiC MOSFET converter (Figure 5.14) has the lowest loss. The 1.7 kV Cree CAS300M17BM2 is used rather than 1.2 kV SiC MOSFET devices because of its lower R_{on} [125].

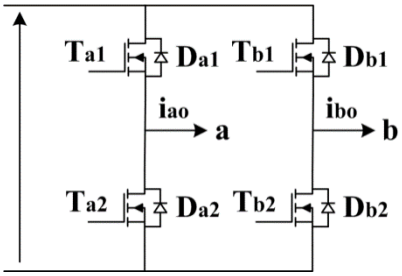


Figure 5.14 SiC MOSFET-based 2-level converter

The conduction losses can be calculated by Equations (5-63) - (5-66). And the duty cycles are the same as 2-level IGBT converters, which are given by (5-25) and (5-26).

$$\bar{P}_{cond\_Ta1} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} d_{a1} \cdot i_a^2 \cdot R_{on} d(\omega t) \tag{5-63}$$

$$\bar{P}_{cond\_Da1} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} d_{a1} \cdot (i_a^2 \cdot R_{on\_D} + V_{f0} \cdot i_a) d(\omega t) \tag{5-64}$$

$$\bar{P}_{cond\_Ta2} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} d_{a2} \cdot i_a^2 \cdot R_{on} d(\omega t) \tag{5-65}$$

$$\bar{P}_{cond\_Da2} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} d_{a2} \cdot \left(i_a^2 \cdot R_{on\_D} + V_{f0} \cdot i_a\right) d(\omega t) \tag{5-66}$$

The turn-on and turn-off switching energies are provided by manufacture datasheet. Therefore, curve fitting is used to estimate the switching loss. Similar to IGBTs, the switching loss can be calculated by Equation (5-32) and (5-33).

5.4.2 GaN HEMT 3-level MMC

Compared with existing switching power devices GaN devices have a smaller size, which reduces the parasitic parameters. The absence of wire bones allows ultra-low inductance and provides high manufacturing reliability. Figure 5.15 shows the comparison between the package of top-side cooled GaN and TO-220. The compact layout lowers the drain voltage overshoot. No body diodes are required as the reverse conduction is an intrinsic operational capability of GaN devices. These features contribute to a significant low switching loss [126]. The thick redistribution layer (RDL) and top copper of GaN package allows a low R_{on}.

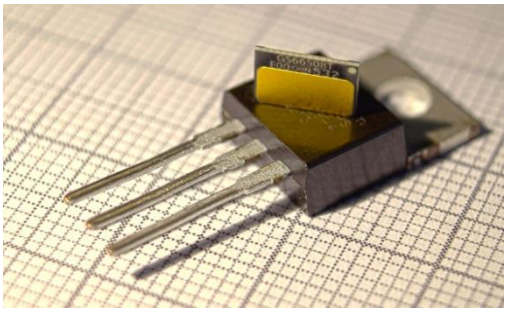


Figure 5.15 The package of top-side cooled GaN device in comparison with TO-220 (from GaN System)

Based on the availability of GaN 650 V rated and 100 V rated devices, 3-level and 9-level GaN MMC can be used in a 600 Vdc LVDC application. Considering that conduction losses dominate the losses of MOSFET MMCs, R_{on} is the main factor that dictates the choice of device and topology [90]. For a 9-level MMC application, the 100 V rated GS61008T GaN HEMT (R_{on}=7.4 mΩ) yields no benefit comparing with the IRFP4110PbF Si MOSFET (R_{on}=3.7 mΩ). Hence a GaN 3-level MMC (Figure 5.16) using 650 V GaN GS66516T devices is proposed.

The calculation of GaN MMC conduction losses and switching losses follows the same method as the Si MOSFET MMC, except that there is no body diode switching loss for GaN devices.

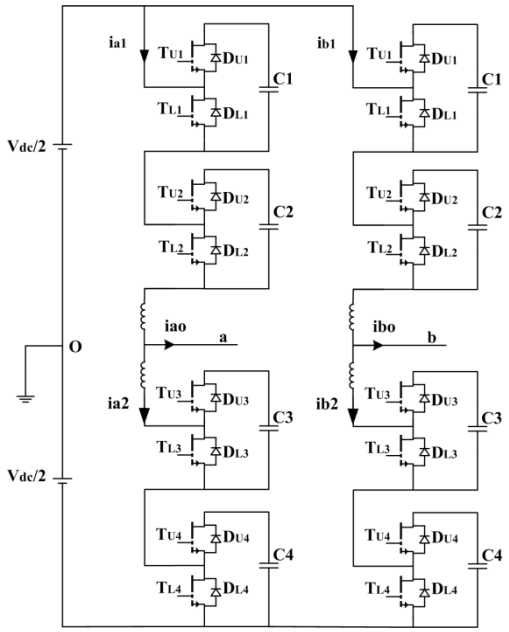


Figure 5.16 Topology of a GaN 3-level MMC

5.5 Loss Comparison

Section 5.3 proposed 5-level to be the most practical number for MOSFET MMC, and the parallel-connection of MOSFETs is very attractive for the improvement of efficiency. Section 5.4 proposed another two wide bandgap devices based converters for LVDC applications, SiC MOSFET 2-level and GaN HEMT 3-level converters. In this section, the three types of converter will be compared in terms of power losses. The optimal number of devices for parallel connection will be investigated as well. In addition, the inductor losses and the use of transformer will be discussed.

5.5.1 Discussion about Inductor Loss

Inductor losses depend on material and manufacturing techniques and therefore estimates for losses are hard to provide. Instead, the value of inductance required for each of the topologies is compared to indicate the relative losses of each.

Inductors are placed in series with submodules in each arm and cause additional power losses including core loss, AC winding loss and DC resistance loss in MMC. To meet the harmonics requirements, inductors are needed for conventional 2-level converters in both input and output filters as well.

For a simple comparison, the requirement for input DC current distortion is set to be 5% with 600 Vdc input, 10 kW output power, 10 kHz switching frequency, M=0.57 and unity power factor.

Table 5.7 Comparison of Inductance requirements and harmonic distortions for different levels of converter

No. of Levels	**Input filter L_{fin}**	**Output filter L_{fo}**	**Input current ripple**	**Output THD**
2-level	6.5 mH	3 mH	5%	1.62%
	Required L_{arm}		**Input current ripple**	**Output THD**
5-level	1.5 mH		4.7%	1.42%
7-level	1.5 mH		4.5%	1.17%
9-level	1.5 mH		4.1%	1.05%
11-level	1.5 mH		3.7%	1%

Table 5.7 shows the simulation results of the required inductor values for a 2-level converter and MMCs with various numbers of levels. Results show that the sum of arm inductors in two-phase-leg MMC is approximately twice the value of output filter inductance in 2-level converter. The AC value of arm current in MMC, however, is half the value of output AC current, as shown in Equation (4-3) and (4-4). Also, the harmonic content before the output filter in 2-level converter are larger, which would increase the core losses. It's difficult to tell if the arm inductors in MMC lead to more power losses than the 2-level converter by simply comparing with output filter inductor. But to eliminate 2nd harmonic current in the DC side, usually a bulky input filter is required for 2-level converters. Based on the calculation method presented in [121], the inductance required for the input filter of a conventional two-level converter needs to be approximately 6.5 mH to meet the 5% input current requirement. In this case, the arm inductors might not introduce more power dissipation than conventional 2-level converters.

5.5.2 Discussion about Modulation Index and Transformer

Due to the fact that 600 Vdc is chosen for LVDC networks in this study (Section 2.2.3), to generate a 240 Vac output, the modulation index is relatively low for an H-bridge converter. This would lead to an increased current for the same amount of power and the power losses of the converter would increase accordingly. To use a higher modulation index requires an interface transformer. Hence, there is a trade-off between converter loss and transformer loss. In this section, the relationship between modulation index *M* and transformer duty ratio will be deduced.

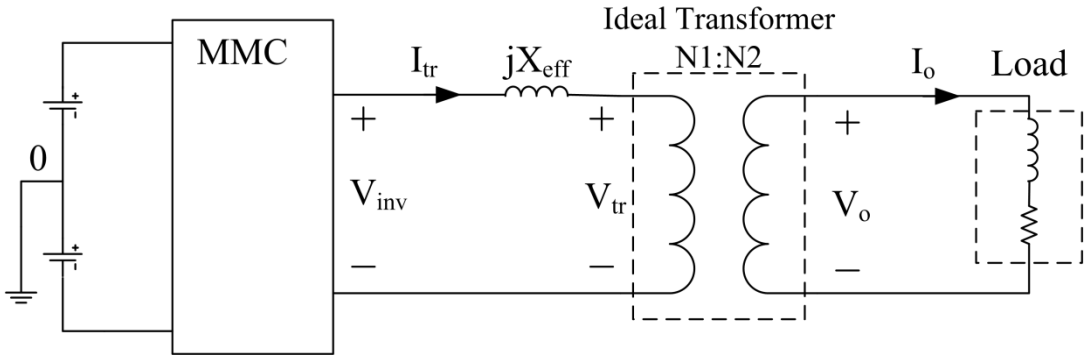


Figure 5.17 MMC circuit with a transformer

Figure 5.17 demonstrates the MMC circuit connects to loads through a transformer. The effective reactance X_{eff} combines the arm inductance and transformer reactance. The RMS value of MMC output voltage V_{inv} is given by (5-67).

$$|V_{inv}| = M \cdot V_{dc}/\sqrt{2} \tag{5-67}$$

Assuming the transformer is ideal with N1:N2 turn ratio, Equation (5-68) can be obtained.

$$\frac{V_{tr}}{V_o} = \frac{N1}{N2}, \qquad \frac{I_{tr}}{I_o} = \frac{N2}{N1} \tag{5-68}$$

Based on KVL, the relationship between V_{inv} and V_{tr} can be given by.

$$V_{inv} = I_{tr} \cdot jX_{eff} + V_{tr} \tag{5-69}$$

Assume *S, P, Q, PF* and X_{pu} denotes the apparent power, active power, reactive power, power factor, and per unit impedance respectively. Equations (5-70) to (5-73) can be derived.

$$P = S \cdot PF \tag{5-70}$$

$$Q = S \cdot \sin(\arccos PF) \tag{5-71}$$

$$I_o = I_d + jI_q = \frac{P}{V_o} + j\frac{Q}{V_o} \tag{5-72}$$

$$X_{eff} = X_{pu}\frac{V_o^2}{S} \tag{5-73}$$

where I_o is the RMS of output load current, I_d and I_q are the real and reactive current components of I_o respectively.

By substituting (5-70) and (5-71) into (5-72), I_o can be expressed by (5-74).

$$I_o = \frac{S}{V_o}[PF + j\sin(\arccos PF)] \tag{5-74}$$

By combining (5-67), (5-68), (5-69), (5-73) and (5-74), the relationship between *M* and transformer duty ratio can be given by

$$M = \frac{\sqrt{2}V_o}{V_{dc}}\sqrt{\left(\frac{N2}{N1}X_{pu}\right)^2 + \left(\frac{N1}{N2}\right)^2 - 2X_{pu}\sin(\arccos PF)} \tag{5-75}$$

Simulations of a 5-level MMC were performed to assess how the converter efficiency changes when an interface transformer is used. The turn ratio of the transformer and modulation index was adjusted so that the output voltage remained at 240 V RMS for a 600 Vdc input. And the highest transformer duty ratio is N1:N2=1.7 to make sure that M is not exceeding 1. As the turn ratio increases the voltage on the converter side of the transformer must do also by way of an increased modulation index. The higher voltage requires less current for the same power flow and thus decreases i^2r loss and increases efficiency.

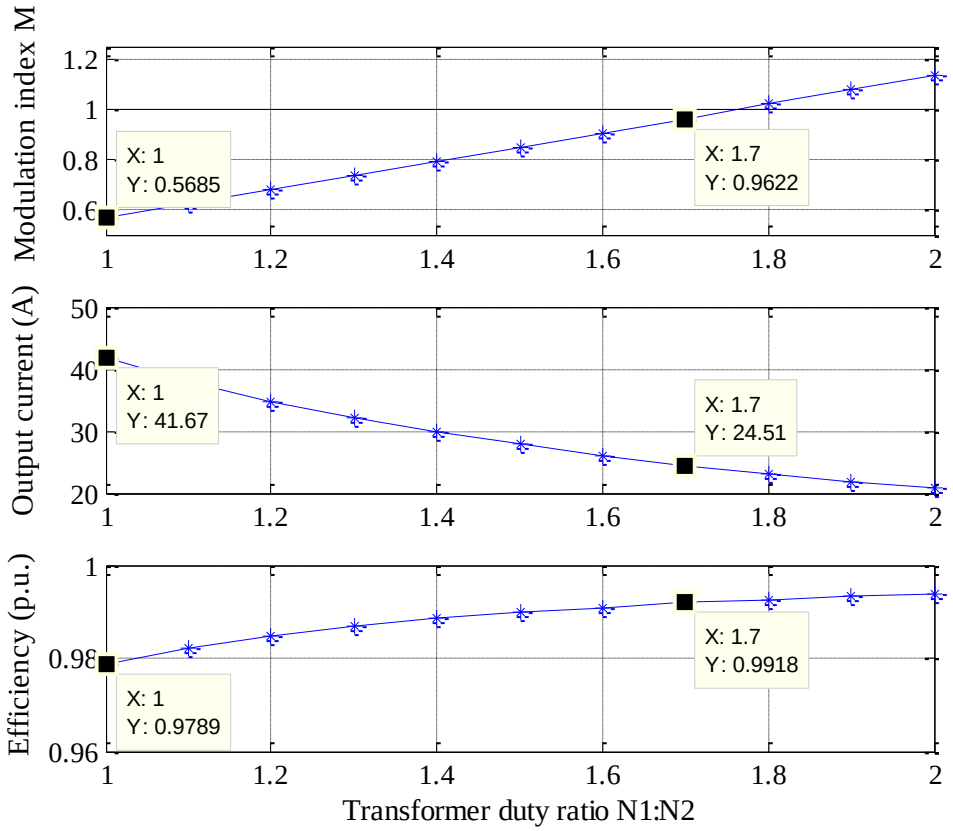


Figure 5.18 Modulation index required for different transformer duty ratio, the corresponding output rms current values and converter efficiency for 5-level Si MOSFET MMC at 10kW, 10kHz, X_{pu}=0.1 and unity power factor

Results in Figure 5.18 show that by using an interface transformer and matching the output characteristics of the converter so that it can operate with unity modulation index, the output current is significantly reduced. The corresponding efficiency of 5-level MMC is increased from 97.89% to 99.18%.

Table 5.8 Comparison of capacitance requirements for different levels of converters M=1, 10 kHz, 10 kW

No. of Levels	**Required Input C_{dc}**(mF)	**Capacitance** (mF)	**Manufacturer Part No**	**ESR** (mΩ)	**Capacitor Loss** (W)
2-level	9.7	10	B43740A5109M000	8	1.4
MMC	**Required C_{sub}**				
3-level	0.9	1.5	B43456A4158M000	47	6.5
5-level	1.8	2.2	B43456A4228M000	28	7.8
7-level	2.7	3.3	B43456A4338M000	20	8.3
9-level	3.5	3.9	B43456A4398M000	17	9.4

For a detailed comparison, when M=1, the submodule capacitance requirements are summarized in Table 5.5, which shows that MMC requires smaller submodule capacitance than that for M=0.57 (Table 5.4). According to new parameters, the power losses for different levels of MMCs are re-calculated and plotted in Figure 5.19. In comparison with M=0.57 (Figure 5.13), the capacitor losses and conduction losses are significantly reduced for M=1. The power loss of 5-level MMC with 2 parallel-connected MOSFETs reduced 72% over 2-level converter, while for M=0.57, the reduction is 57%. The transformer inductance can serve as the output filter to generate a better output waveform quality, as well as providing electrical isolation. However, including a transformer adds cost and volume to the system.

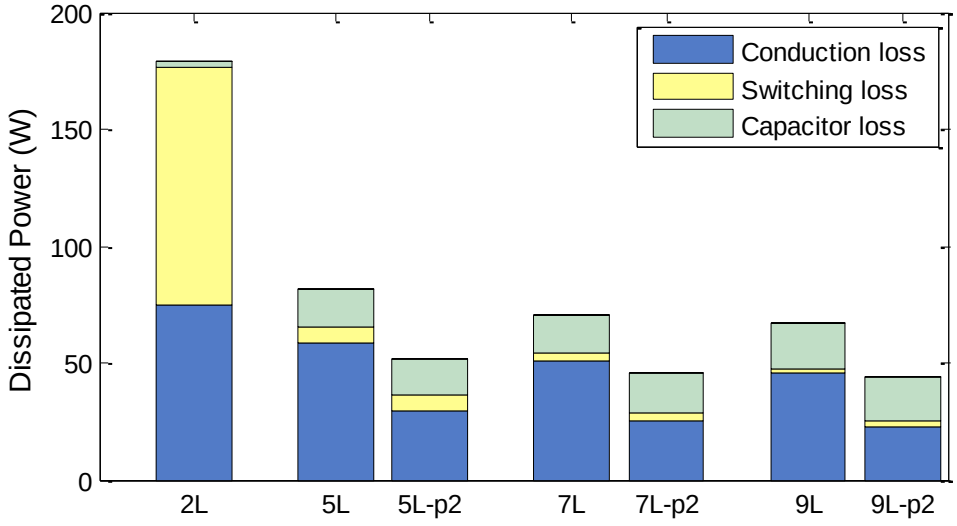


Figure 5.19 Loss comparison for H-bridge 2-level IGBT converter and different levels of Si MOSFET MMC at 10 kHz, 10 kW, M=1 and unity power factor. 2L=2 level IGBT; 5L/7L/9L= 5/7/9 level MMC without parallel connection; 5L_p2/7L_p2/9L_p2= 5/7/9 level MMC with 2 parallel-connected devices

5.5.3 Comparison of Loss with Parallel-connected Devices

When the number of paralleled devices becomes high, the effect of track resistance would become significant. Therefore, there will be a point when it becomes unattractive to keep increasing the number of devices. This section discusses the optimal number in parallel. The comparison of loss in three proposed converters, SiC MOSFET 2-level, GaN HEMT 3-level and Si MOSFET 5-level MMC are presented and the most practical topology for LVDC application is investigated.

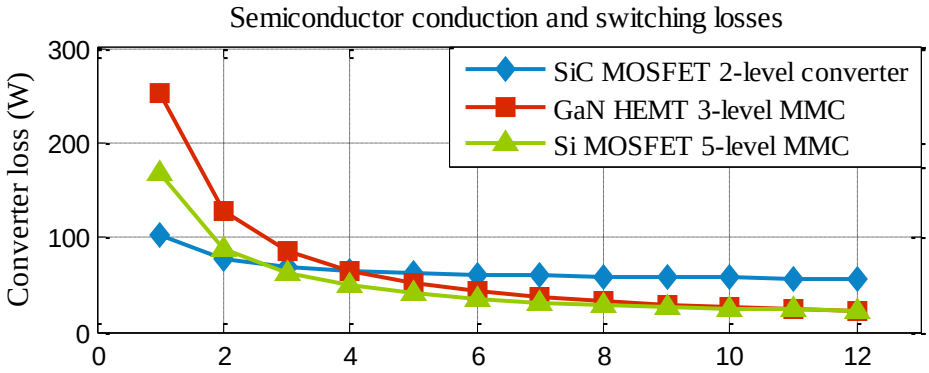
Table 5.9 explains the reason why the three types of semiconductors are not compared in the same topology. Since the conduction loss dominates, the optimal converter topology for each type of semiconductors is selected based on the available devices in the market and a low R_{on}. The 1.7 kV Cree CAS300M17BM2 is used rather than 1.2 kV SiC MOSFET devices because of its lower R_{on}. For a 9-level MMC application, the 100 V rated GaN HEMT (R_{on}=7.4 mΩ) yields no benefit comparing with the Si MOSFET (R_{on}=3.7 mΩ). Hence a GaN 3-level MMC using 650 V GaN GS66516T devices is proposed. As discussed in Section 5.3, a Si MOSFET 5-level MMC is proposed considering the power loss and converter cost.

Table 5.9 Parameter comparison between different types of devices

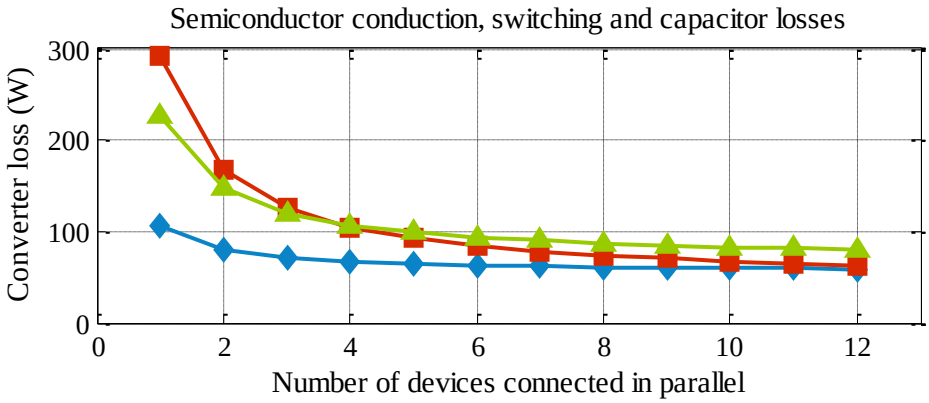
	SiC MOSFET		GaN HEMT		Si MOSFET		
Available voltage ratings	1.7 kV	1.2 kV	650 V	100 V	400 V	200 V	100 V
No. of Levels	2-level	2-level	3-level	9-level	3-level	5-level	9-level
Device	CAS300M 17BM2	C2M00251 20D	GS66516T	GS61008T	IRFP360	IRFP46 68	IRFP411 0
R_{on}	8 mΩ	25 mΩ	27 mΩ	7.4 mΩ	200 mΩ	8 mΩ	3.7 mΩ

Figure 5.20 (a) shows the comparison of semiconductor conduction and switching power losses between these converters. It indicates that there are diminishing returns in terms of converter loss after more than four devices are connected in parallel. At this point the Si MMC 5-level topology has the lowest loss among the three studied.

When capacitor losses are included (Figure 5.20 (b)), SiC 2-level converter has the lowest power losses when the number of paralleled devices is four. The output power quality of SiC 2-level converter, however, is the worst (Table 3.4). It therefore requires a bulky output filter.



(a)



(b)

Figure 5.20 Loss comparison for two phase-leg Si MOSFET 5-level MMC, SiC 2-level, and GaN 3-level MMC converters at 10 kW, 10 kHz, 600 Vdc, M=0.57 and unity power factor

The switches in SiC 2-level converter see the highest switching frequency (10 kHz for 2-level, 5 kHz for 3-level, 2.5 kHz for 5-level MMC), which would introduce high EMI issue. Figure 5.21 further analysed the portion of each type of power losses in each type of converters. It can be observed that the switching loss of SiC MOSFET 2-level converter is high and becomes the dominate factor with the increased number of parallel-connected devices. The conduction loss of GaN HEMT 3-level MMC is extremely large at first, while it's reduced dramatically with the

parallel-connection. For Si MOSFET 5-level MMC, the capacitor loss becomes the dominate factor when the number of parallel-connected devices exceeds 3.

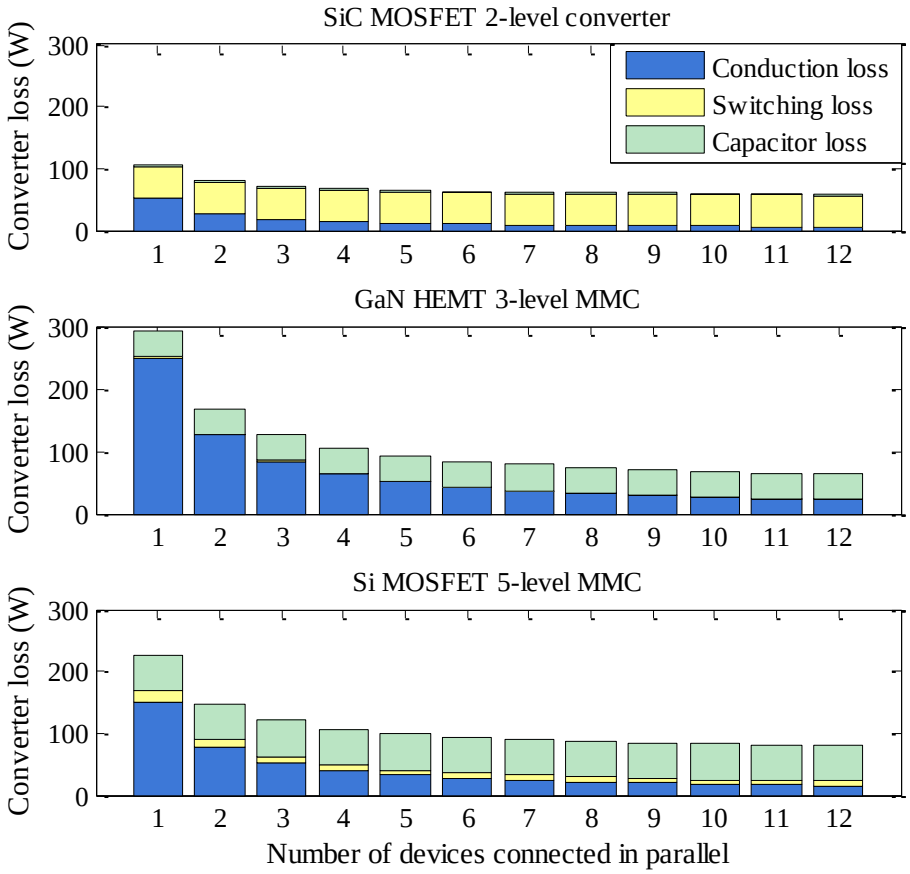


Figure 5.21 Bar chats of converter loss with devices connected in parallel for SiC MOSFET 2-level converter, GaN HEMT 3-level and Si MOSFET 5-level MMC. The capacitor power losses are assumed to be the same for all 12 cases.

In summary, the Si MOSFET 5-level MMC with 4 parallel-connected MOSFETs is the most potential topology proposed for 10 kW LVDC application to deliver high-efficiency and power quality without undue complexity.

5.6 Summary

This chapter evaluates the power losses of different converters for LVDC application. The curve fitting method is used to estimate the semiconductor power losses according to the datasheet provided by the manufacturer. When calculating the conduction loss, especially for MOSFETs, the junction temperature is considered. The switching gate charge and reverse recovery charge are adopted to calculate the MOSFETs switching and body diode switching losses.

Power losses are compared among different levels of converters. Results presented that the capacitor power losses in MMC are almost the same, whilst the conduction and switching losses decrease with the increased number of levels of MMC. The parallel-connection of MOSFETs can reduce the conduction loss significantly. With an increased number of levels the capacitor power losses becomes a dominate factor, and the complexity, volume and cost increased. It was proposed that a 5-level MMC with MOSFETs connected in parallel is suitable for LVDC applications.

Electrolytic capacitors are used in this study because of the small volume. These do, however, introduce a relatively large capacitor loss. Alternatively, film capacitors can be used if the volume is not a problem, which will almost eliminate the capacitor power loss. The inductor loss is difficult to calculate because the losses vary significantly depending on the material and manufacturing techniques. The input inductor is sized according to the 5% input current distortion requirement. Results show that the arm inductance of MMC may not introduce more power dissipation than that of conventional 2-level converter.

To generate a 240 Vac from 600 Vdc the modulation is very low (0.57) for a 2-phase-leg converter. This corresponds to a high current and high loss. For a high modulation index, current through the switches may be decreased and losses reduced with the requirement of an interface transformer. Therefore, the improved efficiency must be traded against the additional component which adds cost and volume.

SiC MOSFET 2-level converter and GaN HEMT 3-level MMC are two other feasible converter types for LVDC application. Section 5.4 analysed the power losses

of these two wide bandgap devices based converters. The comparison results in Section 5.5 show that a converter with 4 parallel-connected devices is the most favourable number due to diminishing returns in of efficiency gains because of track resistance. The Si MOSFET 5-level MMC with 4 MOSFETs in parallel is the most promising topology considering its relative low cost, high efficiency and waveform quality.

6. Thermal Design and Thermal Measurement Verification

6.1 Introduction

Thermal design is critical because excessive junction temperature is detrimental for power semiconductor devices [127]. Temperature rise is determined by the dissipated power and thermal resistance. Thermal resistance is a factor to describe how easer the generated heat can be transferred. There are three mechanisms of heat transfer: conduction, convection and radiation. The transfer of heat from the junction of power devices to a heat sink is by means of conduction. In this chapter, the heat energy flow by conduction is analysed and the heat sink is sized for different kinds of converters mentioned in Chapter 5. Thermal measurement is designed in this chapter, and hardware is set up to verify the loss calculation proposed in Chapter 5.

6.2 Thermal Analysis

Power dissipation in the semiconductors will result in the rise of junction temperature. Where temperature exceeds the maximum temperature specified on the datasheet the reliability and performance of semiconductors will not be guaranteed. A thermal calculation is therefore conducted to avoid the excessive junction temperatures.

Thermal resistance is an intrinsic property used to describe the thermal conductivity of an object, which is denoted by (6-1), where ΔT is the temperature difference between the high and low temperature ends, P_{cond} is the dissipated power through this object.

$$R_\theta = \frac{\Delta T}{P_{cond}} \tag{6-1}$$

Figure 6.1 shows the heat flow of a MOSFET, which is mounted on a heat sink through an electrical insulating washer. The heat flows from the high temperature

end (MOSFET junction) to the low temperature end (heat sink). Because different layers have different surface areas, thickness and thermal conductivity their thermal resistances are different. The total thermal resistance from junction to ambient is given by (6-2).

$$R_\theta = R_{\theta(J-C)} + R_{\theta(C-S)} + R_{\theta Ins} + R_{\theta(S-A)} \tag{6-2}$$

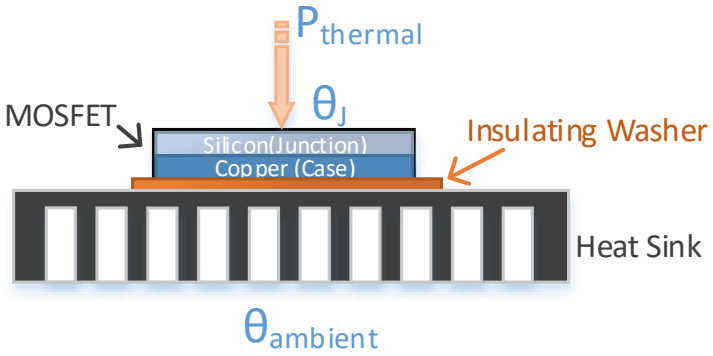


Figure 6.1 Heat flow of MOSFET mounted on a heat sink

Example 1: Maximum MOSFET Power Dissipation

Once the device parameters are specified, the maximum power dissipation can be calculated to make sure it is within the safe temperature range. Table 6.1 summarizes the thermal resistances of MOSFET(IRFB4127PbF) [128], thermal pad (Sil-Pad K-10) [129] and heat sink (47DC) [130].

Table 6.1 Thermal resistances

Devices		Thermal resistances
MOSFET (IRFB4127PbF)	Junction-to-Case	$R_{\Theta J\text{-}C}$ =0.4 ˚C/W
	Case-to-Heatsink	$R_{\Theta C\text{-}S}$ =0.5 ˚C/W
Thermal Insulator (Sil-Pad K-10) Thermal Pad (@50 psi)		$R_{\Theta Ins}$ =2.01 ˚C/W
Heat Sink (47DN)	Heat Sink-to-Ambient	$R_{\Theta S\text{-}A}$ =1.7 ˚C/W

The maximum junction temperature for MOSFET IRFB4127 is 175˚C.

$$\theta_{J\_max} = 175℃ \tag{6-3}$$

Assuming the ambient temperature is 30°C, the maximum temperature rise in the MOSFET is given by (6-4).

$$\Delta\theta_M = \theta_J - \theta_{ambient} = 175 - 25 = 150℃ \quad (6\text{-}4)$$

For MOSFETs, the temperature difference between junction and ambience is

$$\Delta\theta_M = P_{loss} \cdot R_\theta = P_{loss} \cdot (R_{\theta(J-C)} + R_{\theta(C-S)} + R_{\theta Ins} + R_{\theta(S-A)}) \quad (6\text{-}5)$$

Therefore, the maximum power dissipated in the MOSFET is expressed in (6-6).

$$P_{loss\_max} = \frac{\theta_{J\_max} - \theta_{ambient}}{R_{\theta(J-C)} + R_{\theta(C-S)} + R_{\theta Ins} + R_{\theta(S-A)}} = \frac{150}{0.4+0.5+2.01+1.7} = 32.54\ W \quad (6\text{-}6)$$

Example 2: Thermal calculation of parallel-connected MOSFETs and IGBT

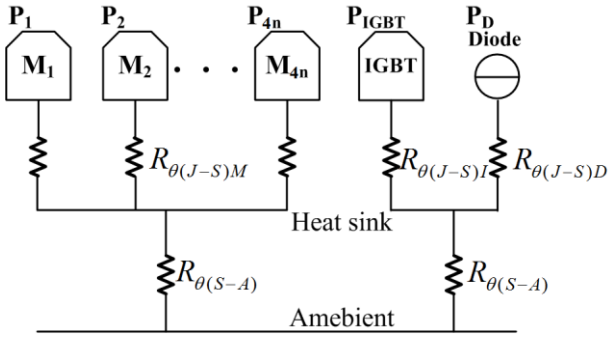


Figure 6.2 Thermal equivalent circuit of parallel-connected MOSFETs and IGBT

Chapter 5 concluded that MOSFETs in parallel connection would reduce the power losses significantly. This part will analyse the thermal design for 4 parallel-connected MOSFET *(n+1)*-level MMC and 2-level IGBT converter. As shown in Figure 6.2, $R_{\Theta(J\text{-}S)}$ denotes the thermal resistance between junction and heat sink, which is given by (6-7).

$$R_{\theta(J-S)} = R_{\theta(J-C)} + R_{\theta(C-S)} \quad (6\text{-}7)$$

The temperature differences between junction and ambient for MOSFET MMC and IGBT converter are given by (6-8) and (6-9) respectively, where $R_{\Theta(S\text{-}A)}$ is the heat sink-to-ambient thermal resistance and P_i is the power loss for MOSFET M_i.

$$T_J - T_{amb} = \sum_1^{4n} P_i \cdot (R_{\theta(J-S)} + R_{\theta(S-A)}) \quad (6\text{-}8)$$

$$T_J - T_{amb} = P_{IGBT} \cdot \left(R_{\theta(J-S)IGBT} + R_{\theta(S-A)}\right) + P_D \cdot (R_{\theta(J-S)D} + R_{\theta(S-A)}) \quad (6\text{-}9)$$

Example 3: Capacitor Cooling and Useful Life

Since the electrolytic capacitor loss is relative high in MMC converter, especially at a high current (low modulation index), the capacitor cooling is assessed here. For a Si MOSFET 5-level MMC, there will be 8 capacitors (B43456A4228M000) in one phase. Each capacitor dissipated approximately 3.65 W in a 10 kW converter [131]. TDK EPCOS states the thermal resistance for capacitor used in the experiment as approximately 5.5 °C/W [132]. According to (6-1), the temperature differential is 20 °C. Assuming the ambient temperature is 25 °C, the hot spot temperature rise is 55 °C which is below the 85 °C limit. According to the useful life calculation tool [132], the capacitor operating useful life would be greater than 250000 hours. Therefore, there is no need to consider the capacitor cooling for the 10 kW LVDC application studied here.

For higher current condition, base cooling with 2 overlapping thermal pads can be used [131]. The capacitor base connected to a heat sink would provide an efficient cooling since a large amount of heat dissipation is through the case base [133].

6.3 Heat Sink Sizing

Once the converter topology and devices are selected, dissipated power can be calculated. By using (6-8) for MOSFET MMC or (6-9) for two-level IGBT converter, required heat sink thermal resistance can be calculated for a certain junction temperatures.

In this section, the heat sink is sized for 10 kW IGBT 2-level, SiC MOSFET 2-level, GaN HEMT 3-level MMC and Si MOSFET 5-level MMC converters. The junction temperature and ambient temperature are assumed to be 125 °C and 25 °C respectively. Section 5.5.3 concludes that 4 parallel-connected devices are the most favourable option. Therefore, heat sink sizing for converters with 4 devices are analysed in Part B, C and D.

6.3.1 Heat Sink Sizing for Different Converters

A. Heat Sink Sizing for IGBT 2-level converter

According to Section 5.2 and 5.3.5, power losses of IGBTs and Diodes in one arm at 0.57 modulation index are listed in Table 6.2. By using (6-9), required $R_{\theta(S-A)}$ can be given by (6-10). The heat sink is thereby selected to meet the requirement with the smallest volume. The parameters are listed in Table 6.2.

$$R_{\theta(S-A)} = \frac{T_J - T_{amb} - P_{IGBT} \cdot R_{\theta(J-S)IGBT} - P_D \cdot R_{\theta(J-S)D}}{P_{IGBT} + P_D} \quad (6\text{-}10)$$

Table 6.2 Heat sink sizing for each arm of IGBT 2-level converter

	Parm (W)	$R_{\theta(J-S)}$	Required $R_{\theta(S-A)}$ (°C/W)
IGBT	59.2	0.51	
Diode	21	0.61	0.71
Heat sink	height x width x length (mm)	Volume (cm^3)	Heat sink $R_{\theta(S-A)}$ (°C/W)
FISCHER ELEKTRONIK SK 47/100 SA	40x200x100	800	0.7

B. Heat sink sizing for SiC MOSFET 2-level converter

According to Section 5.4.1, 1.7 kV SiC MOSFET CAS300M17BM2 is selected due to its low R_{dson}. $R_{\theta(J-C)}$ is provided by the datasheet, but not $R_{\theta(C-S)}$ [134]. $R_{\theta(C-S)}$ is also called contact thermal resistance, which is determined by the contact area size and how good the contact between the package and heat sink [135].

The surfaces of package cases and heat sink surfaces are not perfectly flat. There will be an air gap between them which is a good thermal insulator. The contact force will enhance the contact; however, it's not the research area that this thesis will investigate. In this study, the assumption is made that the contact between SiC MOSFET module and heat sink is similar as the contact between Si MOSFET and heat sink. Since case-to-sink thermal resistance has an inverse relationship with the contact area, $R_{\theta(C-S)}$ can be estimated by (6-11).

$$R_{\theta(C-S)SiC} = \frac{A_{Si}}{A_{SiC}} R_{\theta(C-S)Si} \quad (6\text{-}11)$$

where A_{Si} and A_{SiC} are the contact areas for Si MOSFET and SiC MOSFET module, $R_{\theta(C\text{-}S)Si}$ is the Si MOSFET case-to-sink thermal resistance which is provided by datasheet [117].

Once the junction to heat sink thermal resistances is defined, the required $R_{\theta S\text{-}A}$ can be calculated by using (6-8).

C. Heat sink sizing for GaN HEMT 3-level MMC

There are two kinds of package of GaN HEMT provided by GaN Systems - Top-side cooled and Bottom-side cooled. As shown in Figure 6.3, top-side cooled device has a larger metal contact area and typically used in a higher power system than the bottom-side cooled transistor. In LVDC application, the top-side cooled device is chosen because of the demand for a better thermal solution. Usually, a pedestal copper block would be required when mounting the GaN transistor to a heat sink [136]. Thermal resistance of the copper block can be calculated by (6-12).

$$R_\theta = \frac{d}{\lambda A} \tag{6-12}$$

where d is the length in m, A is the contact area in m^2, and $\boldsymbol{\lambda}$ is the material thermal conductivity in W/m°C

(a) Top-side cooled (b) Bottom-side cooled

Figure 6.3 Package of GaN HEMT devices, from GaN Systems

Assuming 4 parallel-connected GaN transistors are mounted to a pedestal copper block (30mmx30mm, 3mm height), the thermal resistance is given by (6-13).

$$R_{\theta\_copper} = \frac{0.003}{385*(0.03*0.03)} = 0.009°C/W \tag{6-13}$$

The resistance is so small that can be ignored. Similar with SiC MOSFET module, only $R_{\theta(J-C)}$ is provided by the manufacturer. $R_{\theta(C-S)}$ can be estimated by comparing the contact areas.

D. Heat sink sizing for Si MOSFET 5-level MMC

Heat sink sizing for Si MOSFET 5-level MMC is relatively easy, since both the $R_{\theta(J-C)}$ and $R_{\theta(C-S)}$ are given by the manufacturer. The required $R_{\theta(S-A)}$ can be obtained by solving (6-8).

6.3.2 Heat Sink Sizing Comparison

Power losses and the required $R_{\theta(S-A)}$ are listed in Table 6.3 for B, C and D converters. The heat sinks are selected according to the required $R_{\theta(S-A)}$. By comparing volumes, it shows that the Si MOSFET 5-level MMC heat sink has half the volume of that for top side cooled GaN HEMT devices. Even though power loss of GaN 3-level MMC is smaller than SiC MOSFET 2-level converter, the package of GaN transistor is tiny which leads to a large $R_{\theta(C-S)}$. The heat sink volume required for a conventional IGBT 2-level converter is 1600 cm^3 for one-phase-leg. In comparison with IGBT 2-level converter, the heat sink volume required for the three types of converter (B, C and D) is reduced more than 10 times.

Table 6.3: Heat sink Comparison between 3 types of converters with 4 devices in parallel-connection (losses and heat sinks are for one-phase-leg);
Heat sink manufacturer: FISCHER ELEKTRONIK

Converter Type	Ploss (W)	$R_{\theta(J-S)}$	Required $R_{\theta(S-A)}$	Heatsink Part No.	$R_{\theta(S-A)}$	Volume (cm^3)
SiC MOSFET 2-level	33.1	0.072 °C/W	2.95 °C/W	SK 81/ 75 SA	2.5 °C/W	112.5
GaN 3-level MMC	32.1	0.68 °C/W	2.44 °C/W	SK 81/ 100 SA	2.1 °C/W	150
Si MOSFET 5-level MMC	24.4	0.53 °C/W	3.57 °C/W	SK 81/ 50 SA	3.0 °C/W	75

6.4 Methodology of Thermal Measurement

MMC is capable of achieving an efficiency in the range of 98-99% [137]. Therefore, to assess the efficiency of the converter to a reasonable degree of accuracy measurements should be accurate to within 0.1%. There are many ways to assess the efficiency and verify the loss calculation. It can be conducted by measuring the input and output power, i.e. by using power analyser or voltage/current multimeter with precision high capacity resistor. Alternatively, a double-cased temperature-controlled chamber can be used to detect the temperature rise of the mass flow and obtain the power loss. Up to 2 kW, an accuracy of up to ±0.4% can be reached by the calorimetric direct power method [138, 139].

The size of the MMC converter means that the measurements using the calorimetric double-cased chamber loss measurement is not feasible in the laboratory. In this section, an alternative thermal measurement method is proposed because it is impervious to harmonics and EMI generated by switching actions. One submodule of MMC is test to verify the loss calculation.

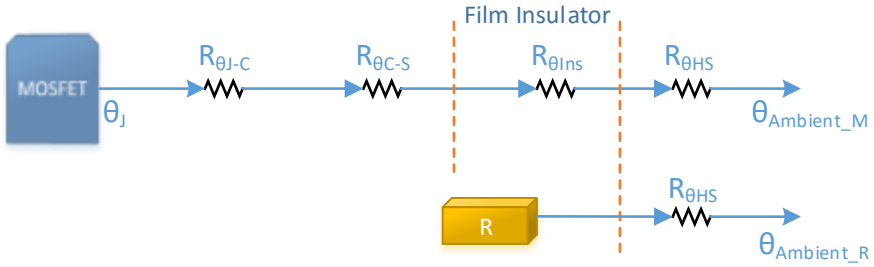


Figure 6.4 Heat flow of MOFST and resistor mounted on heat sinks

As shown in Figure 6.4, the power dissipated by both the MOSFET and resistor will flow through heat sink. Equation (6-1) illustrated that if the heat sinks (47DN) are the same, then the same amount of temperature rise means same associated power loss. Therefore, a thermocouple (Pico Tech) is used to record the temperature rise. Before the measurement, the 'power loss v.s. heat sink temperature rise' curve is calibrated by mounting two TO220 package resistors on the heat sink at the same position (Figure 6.5). Since the package type, position of devices and measurement positions are exactly the same; the thermal distribution won't be an issue in this measurement.

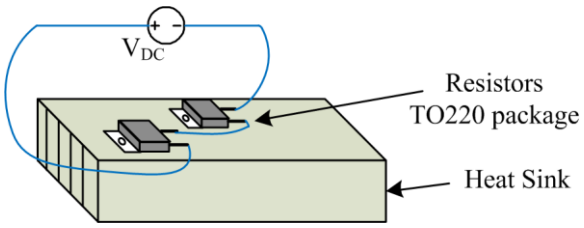


Figure 6.5 Resistors (TO220 package) mounted on a heat sink

6.4.1 Heat Sink Pre-calibrated Curve

The thermal resistance the material used in 47DN is 1.7 ˚C/W. Based on the power loss calculation for one MMC submodule, input power level will not exceed 11 W. Thermocouples are used to measure the temperature rise for 1 hour under each voltage value listed in Table 6.4.

Table 6.4 Data for heat sink pre-calibration curve

V_{dc}	I	P	ΔΘ/°C	V_{dc}	I	P	ΔΘ/°C
1	0.21	0.21	1.02	5.4	1.15	6.20	14.92
2	0.43	0.85	3	5.8	1.23	7.16	16.63
2.5	0.53	1.33	4.31	6	1.28	7.66	17.37
3	0.64	1.91	5.86	6.2	1.32	8.18	18.35
3.5	0.74	2.61	7.56	6.4	1.36	8.71	19.69
4	0.85	3.40	9.05	6.7	1.43	9.55	21.19
4.4	0.94	4.12	10.85	7	1.49	10.43	22.69
4.7	1.00	4.70	11.89	7.2	1.53	11.03	23.38
5	1.06	5.32	13.21				

'Heat sink temperature rise ($\Delta\theta$) v.s. power dissipation (P)' curve is drawn in Figure 6.6. The coefficient of determination (R^2) shows quadratic polynomial curve matches the data better than the linear curve. Therefore, the relationship of heat sink temperature rise Δθ and power loss P_{loss} is given by (6-14).

$$P_{loss} = 0.0069 \cdot \Delta\theta^2 + 0.3088 \cdot \Delta\theta \tag{6-14}$$

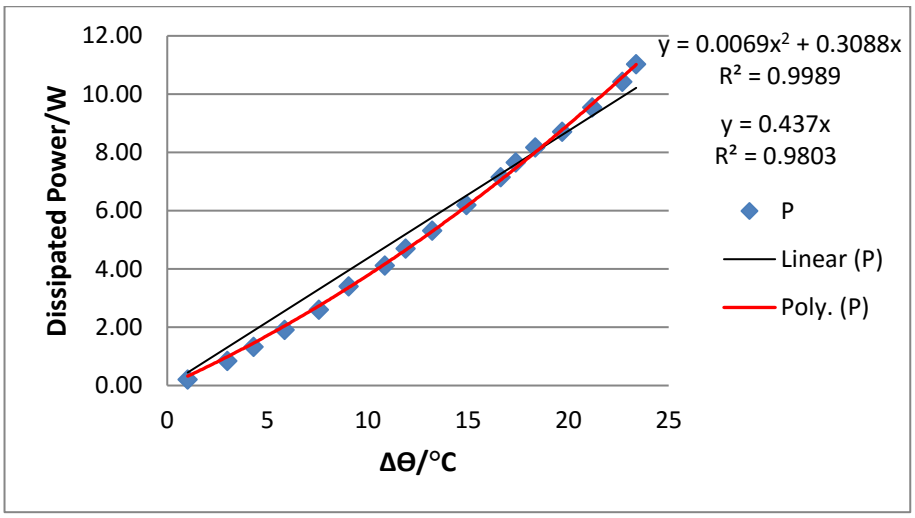


Figure 6.6 Heat sink pre-calibrated curve

6.4.2 MMC Submodule Thermal Test

The experimental test rig is shown in Figure 6.7 to measure the power losses and module switching behavior. It's composed of a single Si MOSFET MMC module operated as a DC-chopper and an R-L load. The MOSFET tested in this circuit is IRFB4127PbF. The max DC side voltage is 100 V. The range of DC side current I_{dc} is from 1 A to 20 A. The theoretical analysis predicts a power dissipation is from 0.3 W (I_{dc}=1 A) to 10.2 W (I_{dc}=20 A).

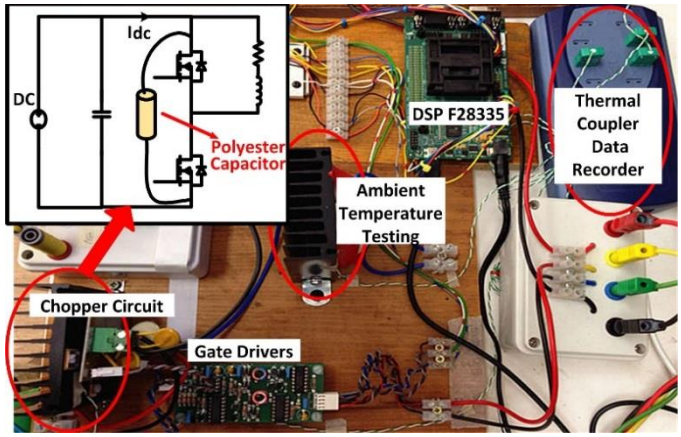


Figure 6.7 Experimental test rig for power loss measurement

The module is mounted on the same heat sink, which has been pre-calibrated against known power dissipation. As long as the module heat sink temperature rise is

measured, the associated device losses can be read from Figure 6.6. Test results are given in Table 6.5 shows, where $\Delta\Theta$ indicates the increased temperature of heat sink; *Difference* means the increased percentage of measured loss. It shows that the measured power losses are higher than calculated losses. There are two main reasons for this. One is because of the track resistance [89]. The second is because of the poor reverse recovery performance of MOSFET body diode which leads to extra power losses.

Table 6.5 Measured power losses of one MMC submodule

V_{dc}/V	I_{dc} /A	$\Delta\Theta$/°C	Measured loss/W	Calculated loss/W
37.8	3.02	6.84	2.43	2.13
44.1	3.52	7.69	2.78	2.56
50	4.2	10.08	3.81	3.18
62.7	5.03	12.78	5.07	4
74.4	5.95	14.20	5.78	4.97
80.4	6.42	16.33	6.88	5.5
86.7	6.99	16.94	7.21	6.17
92	7.41	18.45	8.05	6.69

6.5 Measurement Results

In this Section, the thermal measurement results are compared with the calculated results. Thermal measurement is also applied to verify the MOSFET synchronous rectification. Power losses of one MMC submodule with 2 parallel-connected MOSFETs are tested by thermal measurement in this section. The schottky diode in parallel with MOSFET is investigated.

6.5.1 Synchronous Rectification Verification

Figure 6.8 shows the estimated and measured power dissipation for synchronous and non-synchronous rectification, for a range of currents. It highlights the reduced loss synchronous rectification can bring over normal chopper operation for a MMC submodule. Track resistance power losses are included to compensate the measured results difference in Table 6.5 [89]. Some of the heat dissipated in the tracks and

joints would act to increase heat sink temperature; some of it would be radiated to the air. Thereby half of the calculated losses for parasitic track resistance are included. Figure 6.8 shows the measured and calculated losses closely agree with each other. It also indicates that the calculated loss is slightly lower than the measured value for non-synchronous rectification case. This might be caused by the bad performance of MOSFET's body diode.

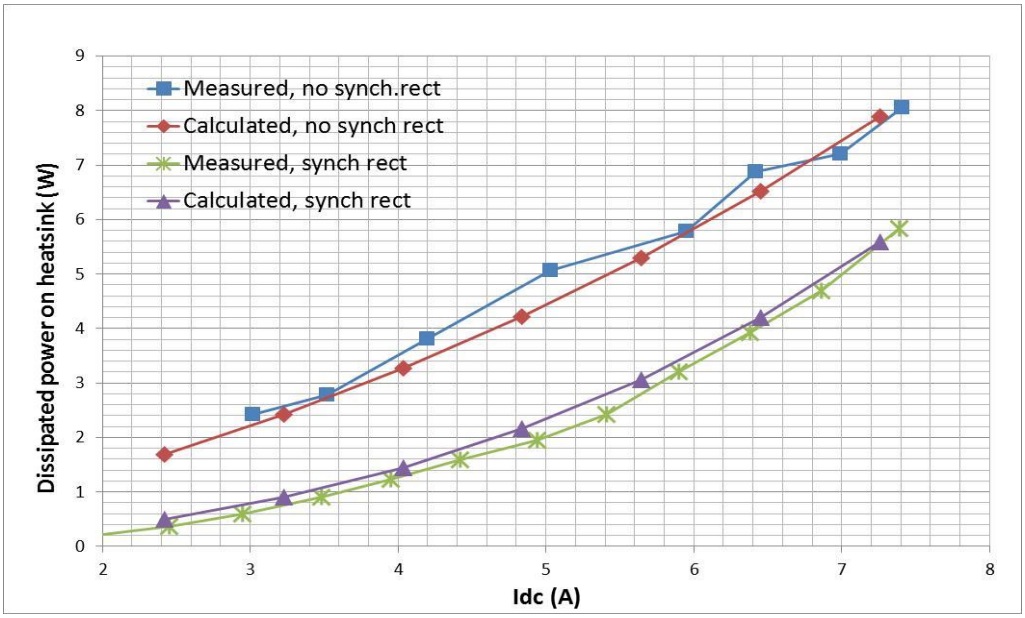


Figure 6.8 Heat dissipation for one MMC submodule with and without synchronous rectification, track resistance is included in the calculated power loss

Figure 6.9 shows the calculated efficiency for specific junction temperatures, T_j. The experimental results lie within the range 25 °C < T_j < 125 °C. According to the thermal analysis, T_j = 60 °C is the predicted junction temperature, which shows a good agreement with the measured results. Figure 6.9 also reflects that with synchronous rectification, the circuit is able to achieve a high efficiency even at low power input.

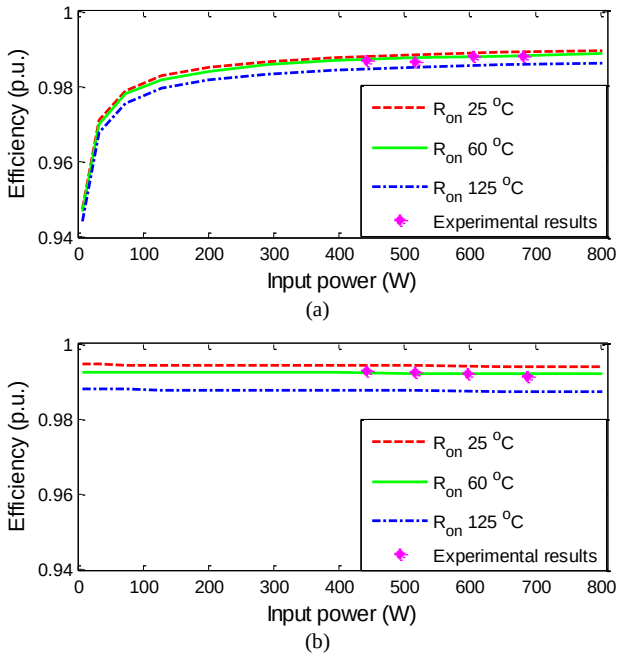


Figure 6.9 Efficiency curves of (a) normal operation and (b) synchronous rectification

6.5.2 Power Losses of Two Parallel-connected MOSFETs

Section 3.4.2 concluded that static current can be shared equally between parallel-connected MOSFETs due to their positive temperature coefficient. In this test, the heat dissipated on the heat sink of one MMC submodule with two MOSFETs (Figure 6.10) in parallel is measured. The schematic circuit is shown in Figure 3.18, where the individual gate resistance for parallel connection (R_{G1} and R_{G2}) is 1 Ω in this test.

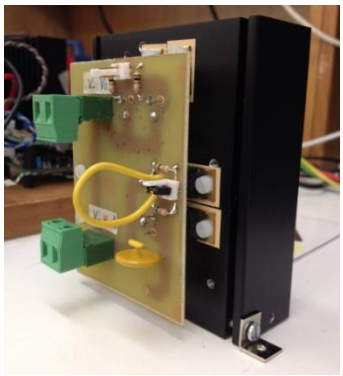


Figure 6.10 One MMC submodule with 2 paralleled MOSFETs

Table 6.6 shows the measured results of paralleled two MOSFETs and without paralleling MOSFETs circuits, which indicates a huge power loss reduction in the former case. Experiment is conducted in a normal chopper operation mode without synchronous rectification.

Table 6.6 Measured results of paralleled MOSFETs circuit

Normal				current /A	Parallel 2 MOSFETs			
efficiency	V_{dc} /V	power loss/W	ΔΘ/°C		ΔΘ/°C	power loss/W	V_{dc} /V	efficiency
97.92%	51	6.38	15.37	6	12.14	4.77	49	98.38%
98.03%	59	8.14	18.62	7	14.68	6.02	57	98.49%
98.09%	68	10.40	22.43	8	18.29	7.96	65	98.47%

6.5.3 Performance with Schottky Diode

The poor reverse recovery performance of MOSFET body diodes draws a lot of concerns. Usually, a Schottky diode can be used to replace the body diode. The performances of one submodule MMC with/without Schottky diode are compared, and the circuit used for this test is illustrated in Figure 6.11. The parameters of MOSFET body diode and Schottky diode are listed in Table 6.7, which indicates that both dynamic and static parameters are improved by Schottky diode.

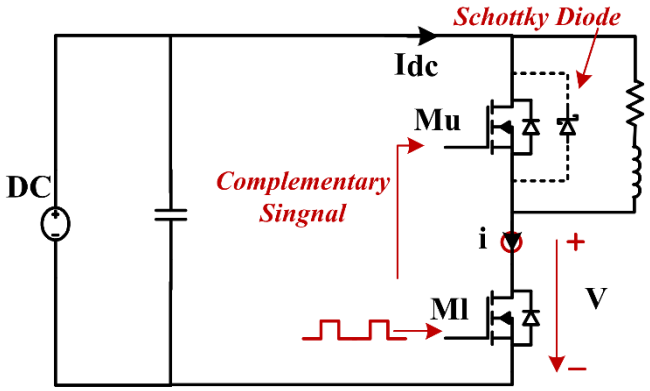


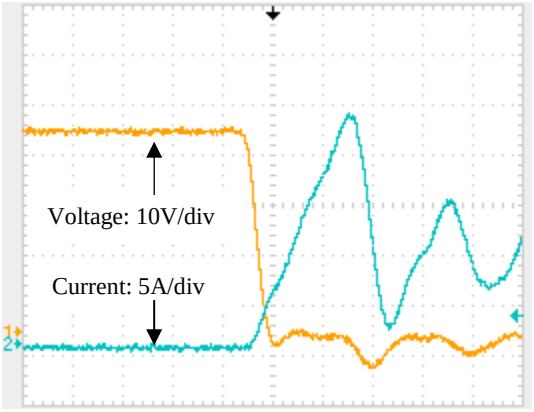
Figure 6.11 One MMC submodule circuit for Schottky diode performance test

Table 6.7 Parameters of MOSFET body diode and Schottky diode

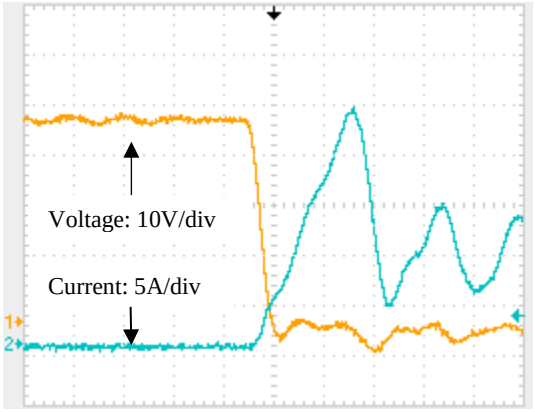
Symbol	Parameter	MOSFET body diode IRFP4668PbF		Schottky Diode APT60S20B	
V_R	Repetitive Reverse Voltage (V)	200	**Conditions***	200	**Conditions***
I_F	Forward Current (A)	130		75	
V_{SD}	Diode Forward Voltage (V)	1.3		0.83	
t_{rr}	Reverse Recovery Time (ns)	130	V_R = 100 V, I_F = 81 A, di/dt = 100 A/μs	55	V_R = 133 V, I_F = 60 A, di/dt = 200 A/μs
Q_{rr}	Reverse Recovery Charge (nC)	633		160	
I_{RRM}	Reverse Recovery Current (A)	8.7		5	

*Tested at 25 °C junction temperature

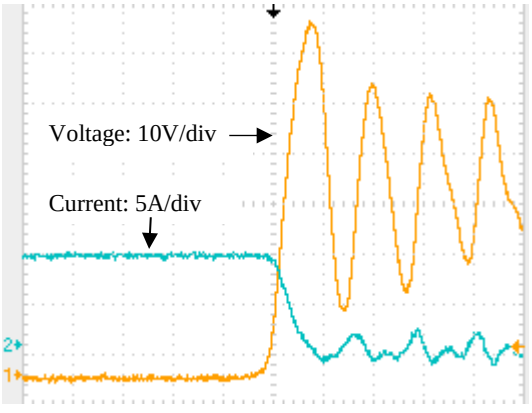
The turn-on current overshoot is mainly caused by the diode reverse recovery, while the turn-off voltage overshoot primarily results from the di/dt of stray inductances. As shown in Figure 6.12, the switching performance of the circuit with a Schottky diode is slightly better than that without one, although the difference is small.



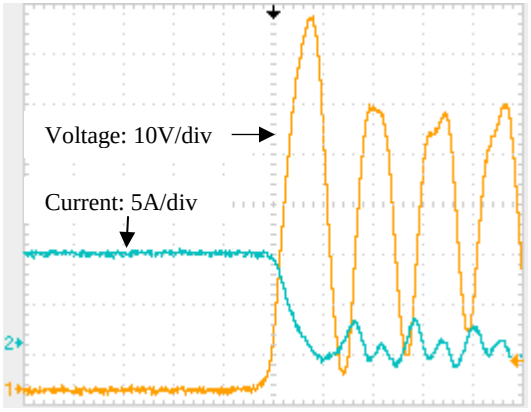
(a) Turn-on transient, with Schottky diode



(a) Turn-on transient, without Schottky diode



(c) Turn-off transient, with Schottky diode



(d) Turn-off transient, without Schottky diode

Figure 6.12 Experimental results of witching transients of MOSFET circuit with/without Schottky diode

The thermal measurement is shown in Figure 6.13. The green line indicates the ambient temperature. The red and blue lines represent with and without Schottky diode in the circuit. The input power is increased every 5000 s (1 h 23 mins). Once the input power has risen, power dissipated in chopper circuit increases; thereby the temperature of heat sink goes up.

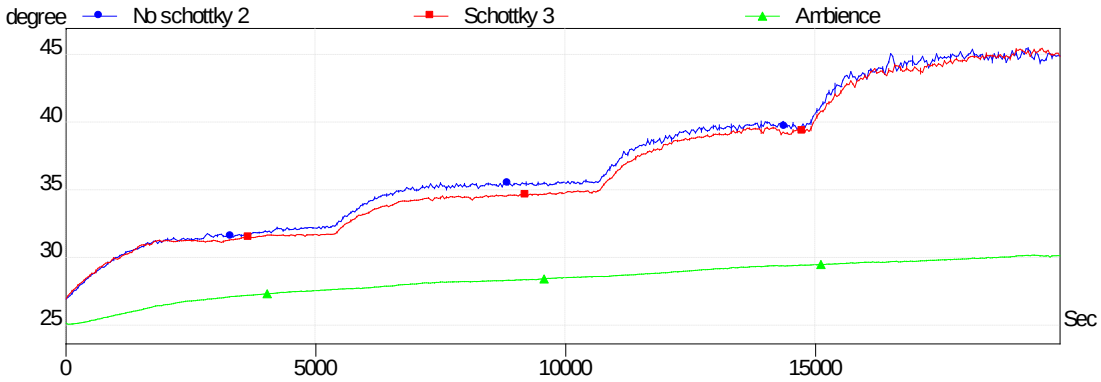


Figure 6.13 The heat sink temperature waveforms of 2 chopper circuits (with and without Schottky diode)

Due to synchronous rectification, the conduction losses of both circuits are similar. Because the switching loss is only a small part of the total losses, especially when current reaches a high level, the power losses of these two circuits are almost the same, as shown in Figure 6.13. Figure 6.12 indicates that the dynamic switching transients are not improved much by adopting Schottky, while RC snubber circuit results in Section 4.7.1 B presents a much better improvement. Therefore, an extra Schottky diode for each MOSFET is not necessary, but the RC snubber circuits are included to improve the switching performance.

6.6 Summary

In this chapter, thermal analysis is conduct to estimate the junction temperature and size the heat sink. Results show that the heat sink is approximately ten times smaller when four devices are connected in parallel for the three types of converters proposed than that of conventional IGBT 2-level converter. Si MOSFET 5-level MMC has the smallest heat sink size, which is half the volume of GaN 3-level MMC.

The package of GaN transistor is much smaller than that of SiC MOSFET module, which leads to an increased $R_{\theta(C\text{-}S)}$ and heat sink size.

The thermal measurement method proposed in this chapter was used to verify the power loss calculation. Thermocouples are used to measure the temperature rise of heat sink and compared with the pre-calibrated '$\Delta\theta$-P' curve to estimate the power loss. The loss of a single MMC submodule circuit has a good agreement with calculated results, especially when the track path resistance are included and the junction temperature is estimated. Thermal measurements show a significant reduction of power loss under synchronous operation than under the normal condition. Losses decreased dramatically when two MOSFETs were connected in parallel. The performance of circuit with schottky diode is investigated, including switching transients' performance and thermal measurement. Results concluded that the MOSFET body diode reverse recovery could be accommodated without the need for a schottky diode, and due to synchronous rectification there was a minimal difference in power loss

7. Conclusions and Future Work

7.1 General Conclusions

In this thesis, research investigations were carried out for the potential use of 600 V DC distribution systems to replace existing three-phase 415 V AC systems. Analysis shows that energisation of 4-core main cables using DC results in power capacity 1.75 times higher than using AC. For 2-core service cables, power throughput 2.63 times higher than AC can be achieved. In addition, there are no reactive power and skin effect issues for DC network. The ever increasing use of DC-operated appliances and LVDC networks have the potential to achieve lower power loss, considering the number of conversion stages is reduced. In the short term, however, many local loads will still require AC connection and an additional DC-AC converter is needed, which would introduce additional DC-AC conversion loss. Therefore, an optimal design of a consumer-end DC-AC converter was carried out in this thesis for the application of LVDC distribution system.

Two-level VSI and commonly used multilevel converters were introduced in Chapter 3. Conventional two-level VSI can be easily implemented. However, each power device suffers from high di/dt and high-voltage stress. In addition, a high switching frequency is required to provide an adequate output quality, which would introduce high switching loss and high EMC issues at the same time. The flying capacitor multilevel converter topology is complex and the number of capacitors required limit its usage. The NPC topology requires additional control to ensure that the neutral point remains balanced. Unequal distribution of power loss can result in the rated current being limited by the power loss in the most stressed semiconductor device. MMC is a promising topology since it benefits from modular construction, reduced size of AC filters, low switching losses, better output waveform quality and the ability to prevent capacitor discharging current. MOSFET based MMC was then proposed for this application thanks to its modular construction. With the feature of SR, it enjoys low conduction losses. In addition, parallel-connection of MOSFETs

can further reduce the conduction loss. The feasibility of parallel-connection is verified by the experimental work in Section 3.4.2.

After the topology is selected to be MOSFET MMC, a detailed converter design was presented in Chapter 4. The submodule capacitor sizing method was introduced, which is based on the peak to peak energy deviation. It demonstrated that the required value of capacitance increases with the increased number of levels. The arm inductor is sized to limit the switching frequency circulating current. Results show that the required arm inductance is inversely proportional to the switching frequency and will not be affected by the number of levels of MMC for a fixed DC voltage. A small output AC filter is required in order to meet the distortion limit when less than thirteen levels are used. The filter design was presented and a parallel damped filter was selected in this study.

Single-phase converters suffer from 2^{nd} harmonic currents in the DC side. A PR and PI with orthogonal imaginary axis current controllers are developed to eliminate the circulating current distortion. For both controllers, simulation results present similar results to each other. To stabilise the output voltage during load change transient, a closed-loop PR controller is introduced. Then a single-phase 5-level MMC prototype is built to evaluate the control strategies. In Section 4.7, the experimental investigation shows that PI controller has comparably better results than that of PR control. The difference might be due to PI controller's larger bandwidth. Another reason might be caused by discretization method when implement the controller into DSP. PR is a second order controller and is therefore sensitive to the discretization errors. There are odd harmonics, 3^{rd} for example, showing in the experimental results. They are resulted from the parameter mismatch of different capacitors.

Power loss calculations based on the converter parameter design were carried out in Chapter 5. The loss calculation was based on a curve fitting method using the data provided by manufacturers' datasheets to provide an estimation. Since the parameters will change with temperature, the junction temperature was taken into consideration. The track resistance of the PCB boards was considered for converters with parallel-connected devices. Results show that the number of modules has little impact on capacitor power losses, while the conduction and the switching losses decrease with

increased number of levels of MMC. However, the converter cost, in particularly the capacitor cost will rise dramatically as well as the volume and control complexity. Based on given constraints, a 5-level MMC was proposed and investigated in this thesis.

Electrolytic capacitors were chosen in this study due to the smaller volume in comparison with film capacitors. However, the ESR is much higher than that of film capacitor, which will introduce larger power losses. The modulation index to generate 240 Vac from 600 Vdc input is relatively low, which will generate a high current and lead to a high loss when transfer the same amount of power as in a high modulation index situation. However a high modulation index will require a transformer, which increases cost and size.

Wide bandgap devices are promising for low voltage applications due to their low power losses. Based on the available devices in the market, SiC MOSFET 2-level converter and GaN HEMT 3-level MMC were proposed and compared with Si MOSFET 5-level MMC. The number of devices in parallel was investigated and the results in Section 5.5 indicate that 4 parallel-connected devices provide the more favourable results due to the existence of track resistance. The Si MOSFET 5-level MMC with 4 MOSFETs in parallel as a topology has the most potential amongst the three types of converters to deliver higher efficiency and better waveform quality without undue cost and complexity.

Thermal analysis was conduct in Chapter 6 and results show that the heat sink size is approximately ten times smaller when four devices are connected in parallel for the three proposed types of converters in comparison to conventional IGBT 2-level converter. The investigation from this work shows that Si MOSFET 5-level MMC has the smallest heat sink size.

In Chapter 6, a thermal measurement was proposed for the purpose of validating the loss calculation. This method based on the idea that the dissipated power will correlate to the temperature rise of the heat sink. Measured results show a good match with the calculated power loss, especially when the track path resistance and the junction temperature are taken into account. It also proves the reduction of power

loss under synchronous operation when compare to the normal condition. Thermal measurement results concluded that the MOSFET body diode reverse recovery could be accommodated without the need of a schottky diode.

7.2 Thesis Contribution

The main contribution of the thesis is the optimal design of a consumer-end DC-AC converter for LVDC distribution applications. To achieve high efficiency and high reliability without undue cost and complexity, MMC topology was chosen with the optimal devices selection and the development of suitable control strategies. Thermal design was also carried out to optimize converter performance. The thesis contributions can be summarised into four points:

- A high-efficiency MOSFET-based MMC has been designed to address the identified weak points of LVDC networks at DC-AC conversion stage, which includes submodule capacitor sizing, arm inductor sizing and output filter design. Study shows a 5-level MMC with 4 MOSFET in parallel connection is a promising alternative topology to replace the conventional 2-level IGBT-based converter. Because the converter efficiency can be improved from 96.8% to 99% for 600 Vdc and 240 Vac application with 10 kW power rating. Also the heatsink sizing shows that the volume can be reduced to 20 times smaller. In addition, MMC provides a better power quality with improved EMC features, which requires a reduced output filter size.
- A thermal measurement technique was developed to validate the power loss calculation. The measured and calculated results are comparable. This technique was also adopted to verify that the MOSFET body diode reverse recovery could be accommodated without the need for a schottky diode.
- PR controller has been designed to eliminate circulating current distortion for single-phase MOSFET MMC. The second order harmonic has been suppressed effectively, but there is third harmonic circulating current shown in the experimental results of a 5-level MOSFET MMC prototype, which is resulted from the parameter mismatch of individual capacitors. The third

contribution is the development of PI control with orthogonal imaginary. Experimental results present a good performance of the circulating current suppression.

- Wide bandgap devices were considered in the process of choosing an appropriate converter topology for LVDC application. Power losses, power quality and heat sink size were compared between SiC MOSFET 2-level converter, GaN HEMT 3-level MMC and Si MOSFET 5-level MMC. The Si MOSFET 5-level MMC was selected based on a comparative analysis on the aforementioned factors. Power loss calculation indicates that four MOSFETs in parallel is the diminishing return point. The factor that affects the parallel-connection of MOSFETs in this study is mainly the track resistance. This is the fourth contribution. Then a circuit with four parallel-connected MOSFETs was tested and the balanced static current sharing has been verified experimentally.

7.3 Recommendations for Future Work

Based on what has been achieved in this research work, the following recommendations are outlined for potential extension of the existing work.

- The protection of LVDC is considered as one of the major problems and the HBSM-based MMC topology adopted in this study cannot block fault current contributions from the AC side during a DC side fault. However, other SM topology and hybrid MMCs possess this capability. Optimal MMC topology for the use of LVDC protection should be investigated.
- Volume and cost of different types of topology can be further investigated. In this study, the cost was compared between IGBT 2-level converter and different levels of Si MOSFET MMC with only semiconductors and capacitors taken into consideration. For a detailed comparison, the cost of filters, heat sinks and gate drivers should also be considered.

- The accuracy and tolerance of any further thermal measurement can be improved by setting up a calorimeter.
- EMC is one of the major concerns for applications such as aircraft distribution systems. Therefore, the effect of EMC on Si MOSFET 5-level MMC should be further investigated.
- This research work showed that the volume and loss trade-off of submodule capacitors were major concerns for the MMC topology to be used in low-voltage application. However, the advances in capacitor technology would make this approach significantly more attractive. The investigation of capacitors with small volume and low ESR are very valuable to realise this application.

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Appendix A. Experimental Configuration

In this section, the details of the practical implementation for the 5-level MMC prototype (Figure 4.22) are presented. As shown in Figure 4.24, the test rig is composed of Digital Signal Processor (DSP), voltage and current transducers, interfacing circuits, complimentary board and gate driver. The schematic circuits and main features of those components will be presented in this section.

A.1 Digital Signal Processor

The main purpose of the digital signal processor (DSP) is to convert the data from analogue to digital, process the data digitally, and then generate the demand switching signals (i.e. PWM signals) for power switches like MOSFETs. The high-performance 32-Bit TMS320C28335 DSP is employed in this study, which is shown in Figure A.1.

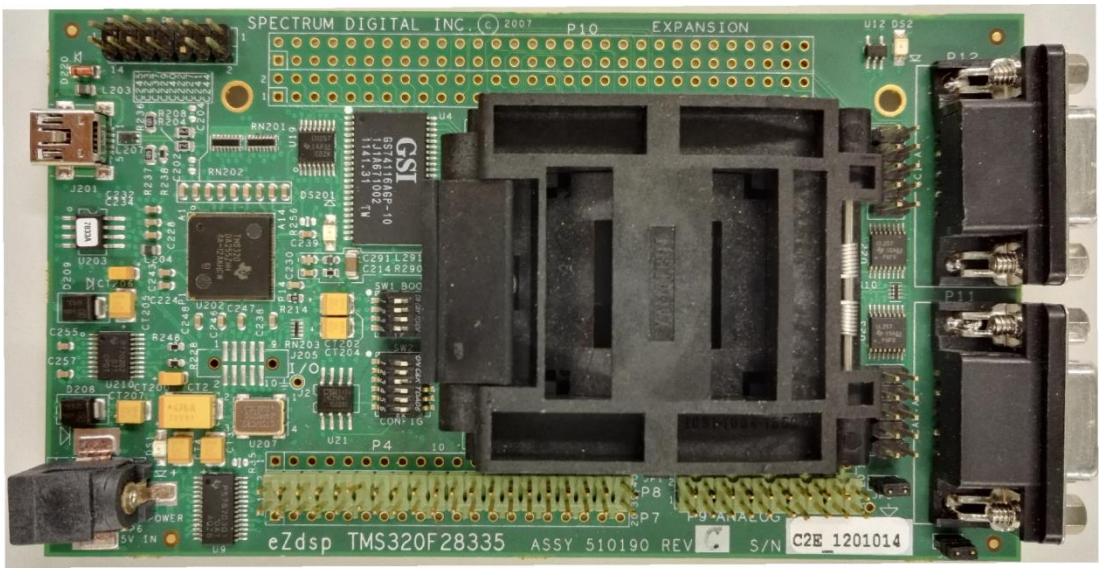

Figure A.1 TMS320F28235 Digital Signal Controller

The related main features are listed as follows:

- High-Performance Static CMOS Technology
  - – Up to 150 MHz (6.67-ns Cycle Time)
  - – 1.9-V/1.8-V Core, 3.3-V I/O Design
- Enhanced Control Peripherals

– Up to 18 PWM Outputs

– Up to 9 16-Bit Timers (6 for ePWMs and 3 XINTCTRs)

- High-Performance 32-Bit CPU (TMS320C28x)

  – IEEE-754 Single-Precision Floating-Point Unit (FPU) (F2833x only)

  – 16 x 16 Dual MAC (6 for eCAPs and 2 for eQEPs)

  – Harvard Bus Architecture

  – Fast Interrupt Response and Processing

  – Unified Memory Programming Model

  – Code-Efficient (in C/C++ and Assembly)
- Three 32-Bit CPU Timers
- Six-Channel DMA Controller (for ADC, McBSP, ePWM, XINTF, and SARAM)
- On-Chip Memory

  –256K x 16 Flash, 34K x 16 SARAM
- GPIO0 to GPIO63 Pins Can Be Connected to one of the Eight External Core Interrupts
- 12-Bit ADC, 16 Channels

  – 80-ns Conversion Rate

  – 2 x 8 Channel Input Multiplexer

  – Two Sample-and-Hold

  – Single/Simultaneous Conversions

  – Internal or External Reference
- Up to 88 Individually Programmable, Multiplexed GPIO Pins with Input Filtering

A.2 Voltage and Current Transducers

Accurate voltage and current data are required for the controller. The voltage transducer shown in Figure A.2 with Hall effect sensing device *LEM LV 25-P* is employed to measure the voltage signal with the voltage range from 0 to 500 V. The measurement resistance R_M has to be in the range of 100 to 350 Ω for a DC circuit supply of ±15 V. As shown in Figure A.3, if the primary current is taken as 10mA

then the value of the input resistors can be calculated from $V\text{-}HT*10^3/10$ Ω. Positions are available from both input terminals for suitable power resistors. Normally a 3watt type is enough. The gain resistor is chosen to suit circuit following the amplifier (NE5534) or AD convertor of microcontroller which may be 5 V or 3.3 V.

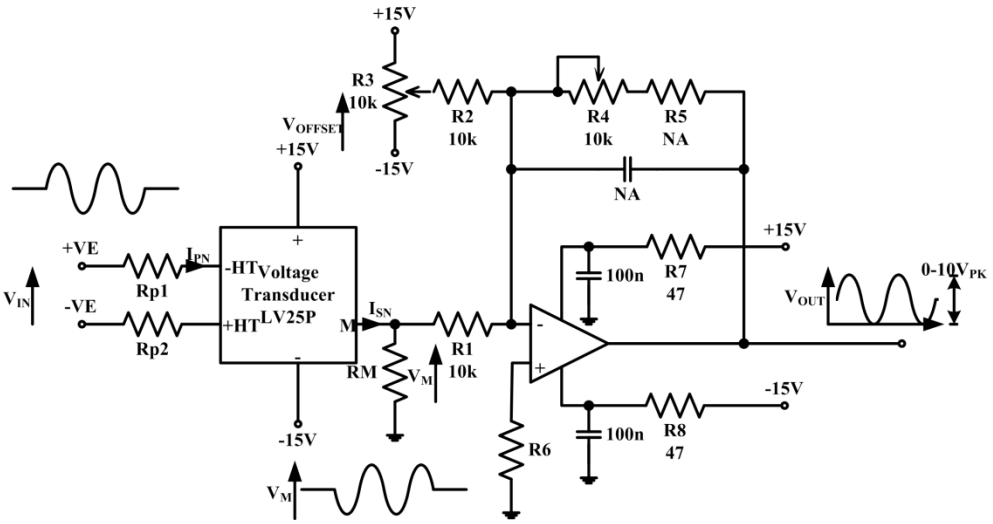

Figure A.2 Circuit schematic of voltage transducer

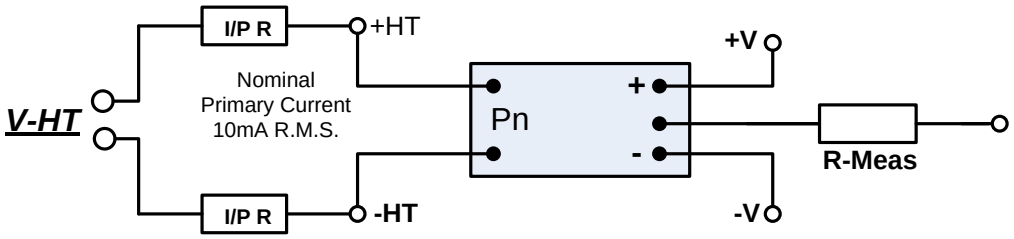

Figure A.3 Voltage transducer minimal circuit

The current transducer circuit presented in Figure A.4 with current sensing device *LEM LA 55-P* is used to measure the AC or DC current with the current range from 0 to 50 A. The measurement resistance R_M has to be in the range of 50 to 150 Ω for a ±15 V DC circuit supply. Nominal current range for one turn primary is 50 A. This can be reduced by winding a number of turns through the transducer window as long as the turns are kept to the top limb for best magnetic coupling. Figure A.6 presents the photo of voltage and current transducers on the same board. There are 6 turns of windings through the current transducer window.

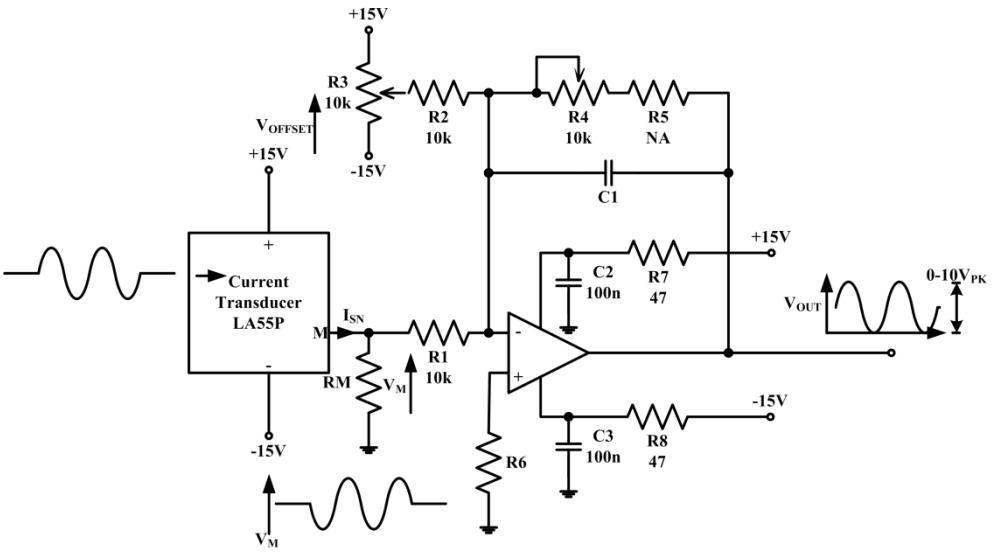

Figure A.4 Circuit schematic of current transducer

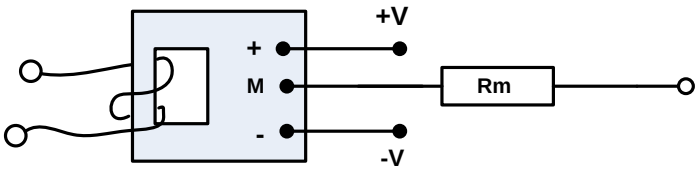

Figure A.5 Current transducer minimal circuit

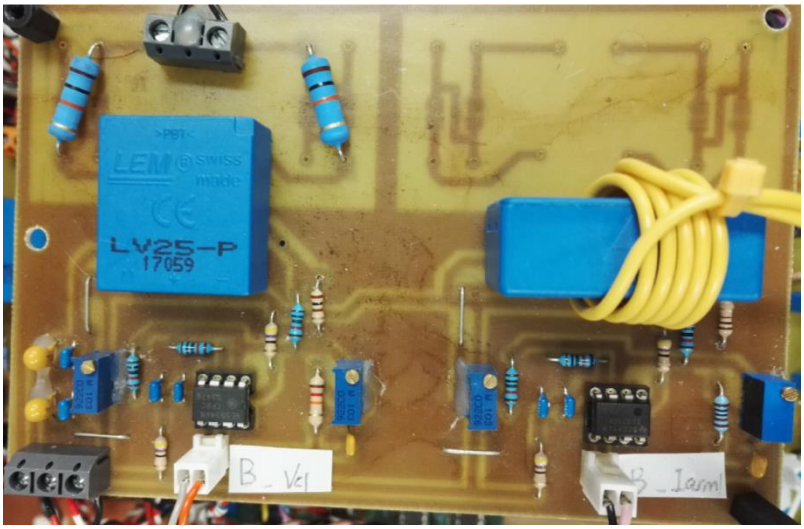

Figure A.6 Photo of voltage and current transducers

A.3 Interfacing Circuits

The interface board implemented in this circuit is given in Figure A.7. Main purpose of this circuit is to isolate the ADC channels of the DSP controller from the voltage and current transducer circuits. Its circuit schematic is given in Figure A.8.

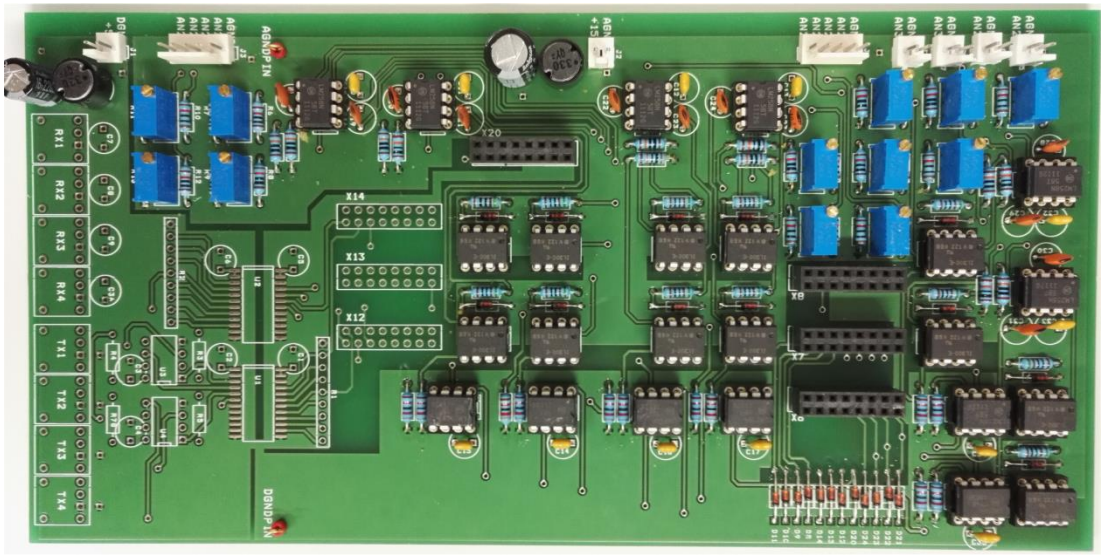

Figure A.7 Photo of interface circuit board

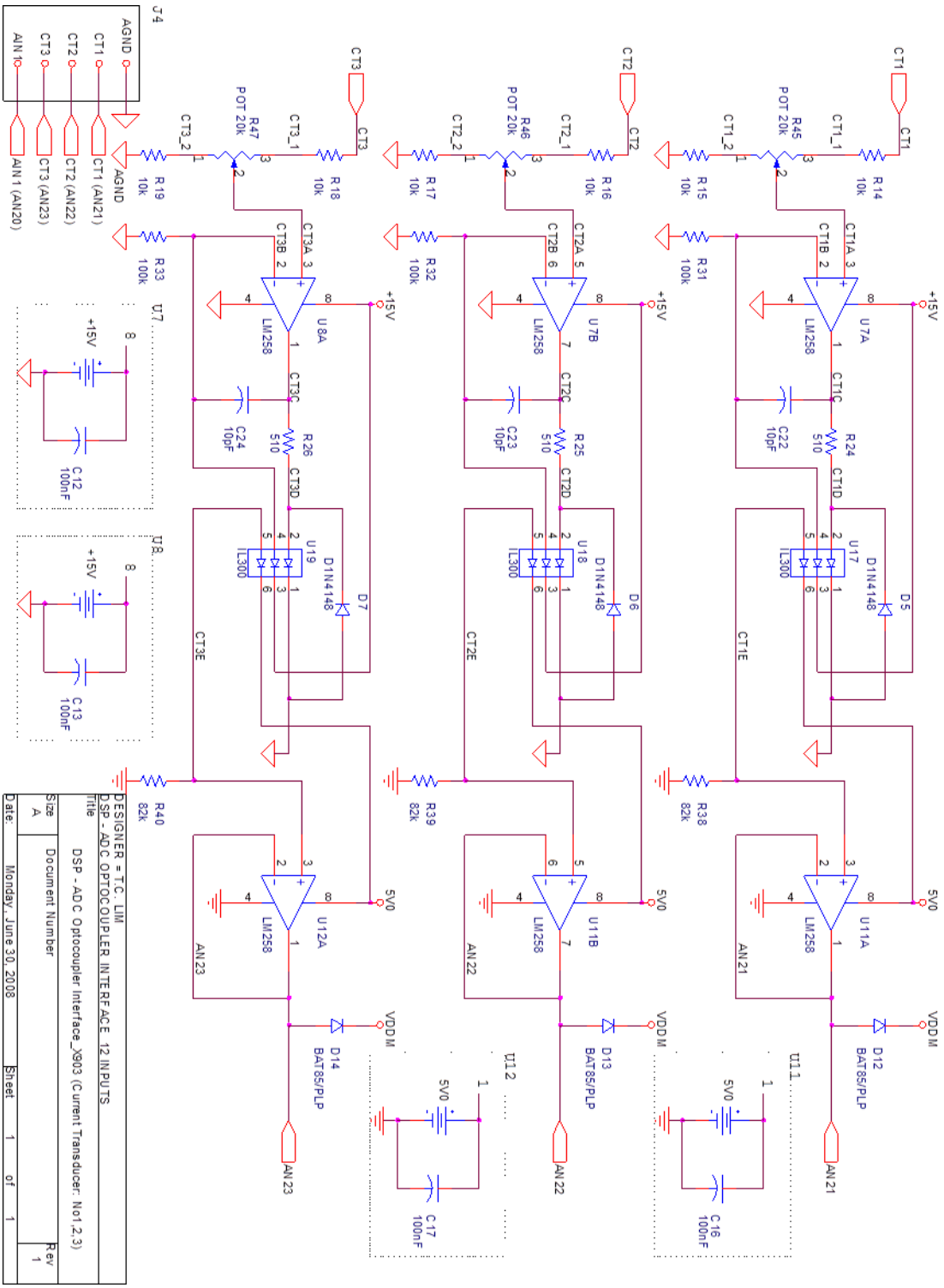

Figure A.8 Interfacing circuit schematic of the ADC channels

A.4 Complimentary Board

The function of complementary signal generating boards is to generate complementary signals for two MOSFETs in the same submodule with 2μs dead time. The circuit photo and schematic are shown in Figure A.9 and Figure A.10 respectively.

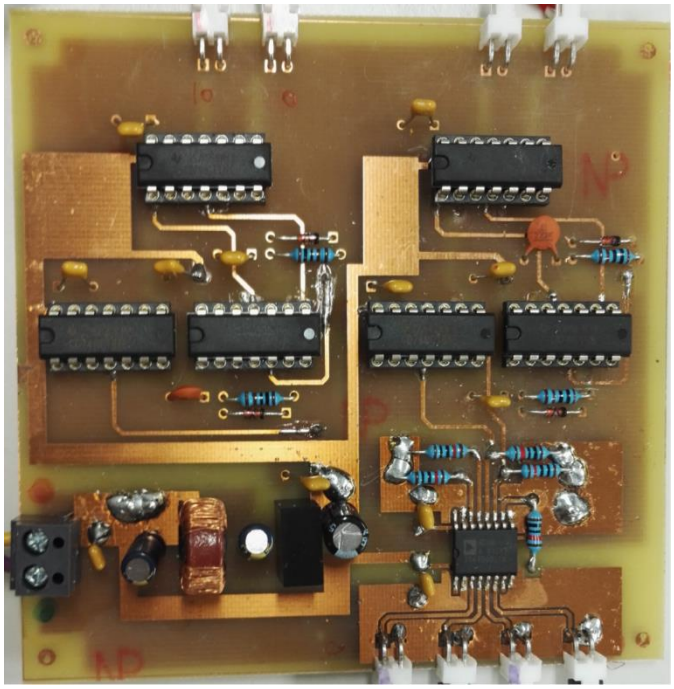

Figure A.9 Photo of complementary signal generating board

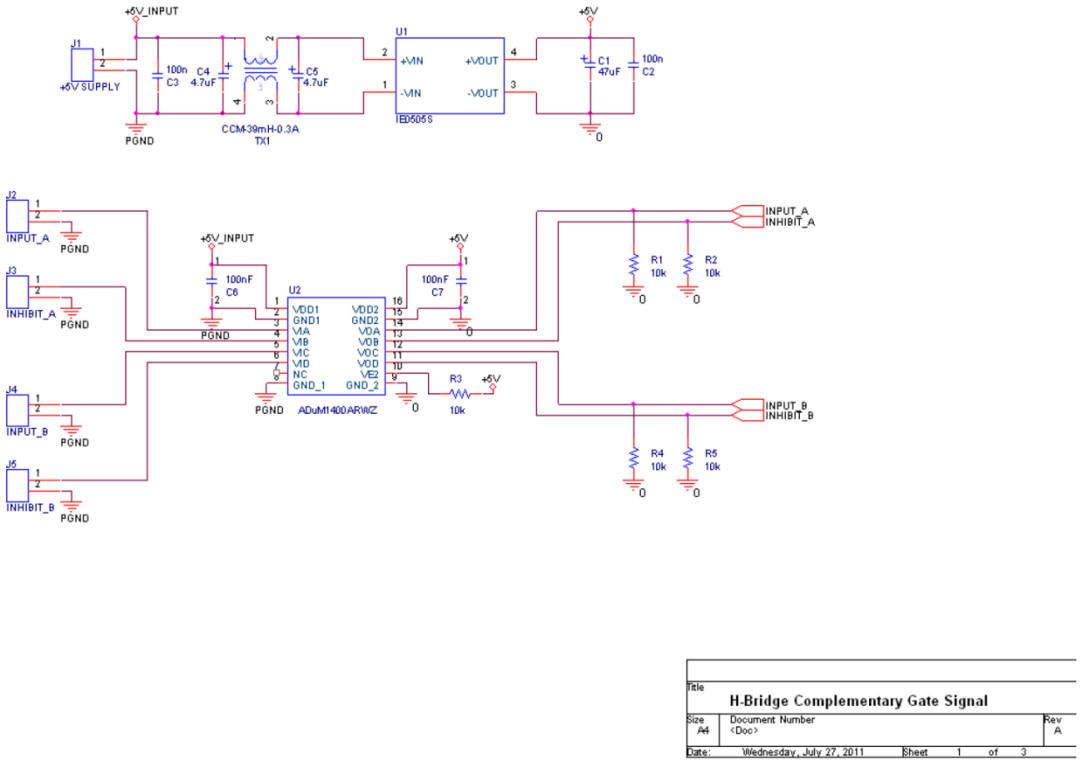

Figure A.10 Complementary gate signal generating board circuit schematic

A.5 Gate Driver

Figure A.11 shows the gate drive circuit implemented in this test rig and the circuit schematic is shown in Figure A.12. The gate drive circuit is used to provide electrical isolation between the PWM interface circuit and gate drive circuits, amplify the 3.3 V PWM signal output from the DSP EPWM output to 15 V for the power MOSFETs to be turned on.

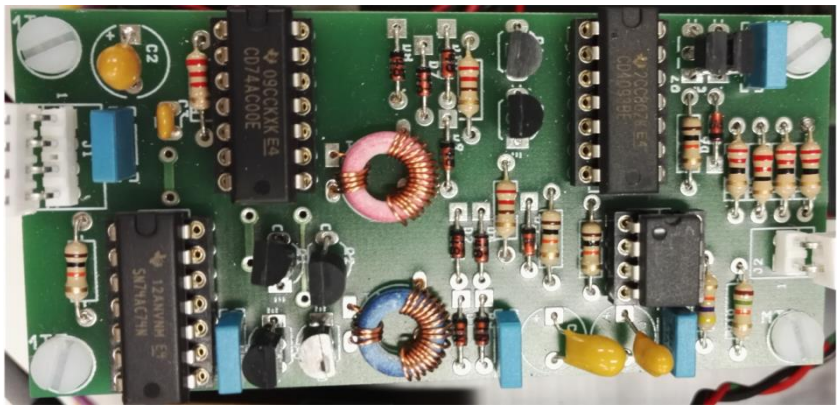

Figure A.11 Photo of a gate drive circuit

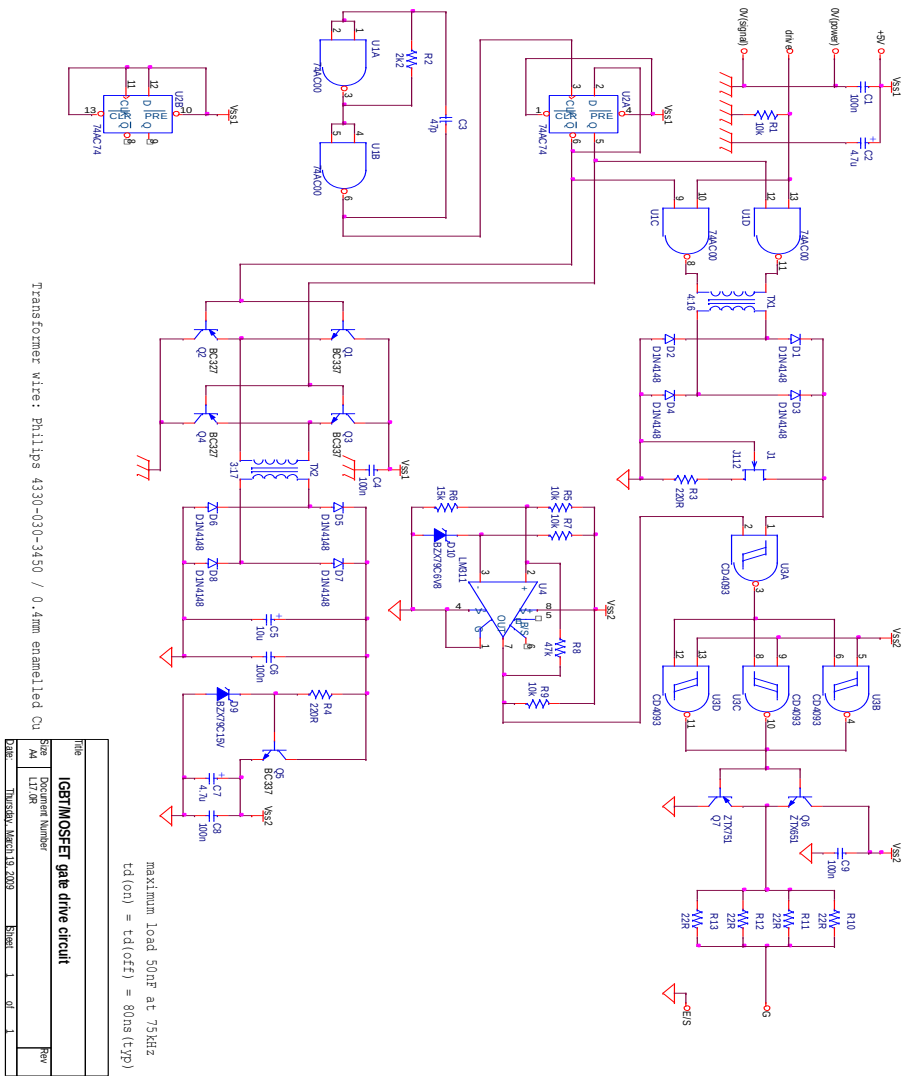

Figure A.12 Gate drive circuit schematic

Appendix B. Matlab Simulation Code

The following shows the Matlab simulation code for a five-level H-bridge MMC with PR control to supress the circulating current.

```
function [sa,flg,va1,va2]=
fcn(Vc,yc,va,ia1,ia2,sa0,flag0,Ucmd)
num=4;% num is the number of cells in one arm
sa=zeros(num*2,1);
flg=zeros(1,2);
var flg;
var tep;

va1=0.5-0.5*va-Ucmd;
va2=0.5+0.5*va-Ucmd;

if (va1>=yc(1))
    flg(1,1)=1;
elseif (va1>=yc(2)&&va1<yc(1))
    flg(1,1)=2;
elseif (va1>=yc(3)&&va1<yc(2))
    flg(1,1)=3;
elseif (va1>yc(4)&&va1<yc(3))
    flg(1,1)=4;
else %va<=yc(num)
    flg(1,1)=5;
end

if (flg(1,1)==flag0(1,1))
    for i=1:num
    sa(i)=sa0(i);
    end
else

vc1=Vc(1:num);
seq1=linspace(1,num,num);

for i=1:num-1
    for j=1:num-i
        if(vc1(j)>vc1(j+1))
            tep=vc1(j);
            vc1(j)=vc1(j+1);
            vc1(j+1)=tep;
            tep=seq1(j);
            seq1(j)=seq1(j+1);
            seq1(j+1)=tep;
```

```
        end
    end
end


if(flg(1,1)==1)% va>=yc(1)
    %+Vdc/2
    for II=1:num
            sa(II)=1;
    end
elseif(flg(1,1)==5)%va<=yc(num)
    %-Vdc/2
    for II=1:num
            sa(II)=0;
    end
elseif(flg(1,1)==2)%va>=yc(2)&&va<yc(1)
    %+Vdc/4
    %upper arm
    if(ia1>=0)% one large by-pass(0)
        for II=1:num
            if(II==seq1(num))
                sa(II)=0;
            else
                sa(II)=1;
            end
        end
    else
        %ia<0 one small by-pass(0)
        for II=1:num
            if(II==seq1(1))
                sa(II)=0;
            else
                sa(II)=1;
            end
        end
    end

elseif(flg(1,1)==4)%va>yc(4)&&va<yc(3)
    %-Vdc/4
    %upper arm
    if(ia1>=0)% 1 small charge/insert(1)
        for II=1:num
            if(II==seq1(1))
                sa(II)=1;
            else
                sa(II)=0;
            end
        end
    else
```

```
        %ia<0 1 large insert(1)
        for II=1:num
            if(II==seq1(num))
                sa(II)=1;
            else
                sa(II)=0;
            end
        end
    end

else%0
    %upper arm
    if(ia1>=0)%two small charge/insert(1)
        for II=1:num
            if(II==seq1(1)||II==seq1(2))
                sa(II)=1;
            else
                sa(II)=0;
            end
        end
    else
        %ia<0  two large discharge/insert(1)
        for II=1:num
            if(II==seq1(3)||II==seq1(4))
                sa(II)=1;
            else
                sa(II)=0;
            end
        end
    end
end
end

%lower arm
if (va2>=yc(1))
    flg(1,2)=1;
elseif (va2>=yc(2)&&va2<yc(1))
    flg(1,2)=2;
elseif (va2>=yc(3)&&va2<yc(2))
    flg(1,2)=3;
elseif (va2>yc(4)&&va2<yc(3))
    flg(1,2)=4;
else %va<=yc(num)
    flg(1,2)=5;
end

if (flg(1,2)==flag0(1,2))
    for i=1:num
    sa(i+num)=sa0(i+num);
```

```
    end
else
vc2=Vc(num+1:num*2);
seq2=linspace(1,num,num);

for i=1:num-1
    for j=1:num-i
         if(vc2(j)>vc2(j+1))
            tep=vc2(j);
            vc2(j)=vc2(j+1);
            vc2(j+1)=tep;
            tep=seq2(j);
            seq2(j)=seq2(j+1);
            seq2(j+1)=tep;
         end
    end
end

if(flg(1,2)==1)% va>=yc(1)
    %+Vdc/2
    for II=1:num
        sa(II+num)=1;
    end
elseif(flg(1,2)==5)%va<=yc(num)
    %-Vdc/2
    for II=1:num
        sa(II+num)=0;
    end
elseif(flg(1,2)==2)%va>=yc(2)&&va<yc(1)
    %+Vdc/4
    %lower arm
    if(ia2>=0)% one large by-pass(0)
        for II=1:num
            JJ=II+num;
            if(II==seq2(num))
                sa(JJ)=0;
            else
                sa(JJ)=1;
            end
        end
    else   %ia<0 one small by-pass(0)
        for II=1:num
            JJ=II+num;
            if(II==seq2(1))
                sa(JJ)=0;
            else
                sa(JJ)=1;
            end
        end
```

```
    end
elseif(flg(1,2)==4)%va>yc(4)&&va<yc(3)
    %-Vdc/4
    %lower arm
    if(ia2>=0)% one small charge/insert(1)
        for II=1:num
            JJ=II+num;
            if(II==seq2(1))
                sa(JJ)=1;
            else
                sa(JJ)=0;
            end
        end
    else    %ia<0 one large discharge/insert(1)
        for II=1:num
            JJ=II+num;
            if(II==seq2(num))
                sa(JJ)=1;
            else
                sa(JJ)=0;
            end
        end
    end
else%0
    %lower arm
    if(ia2>=0)%two small charge/insert(1)
        for II=1:num
            JJ=II+num;
            if(II==seq2(1)||II==seq2(2))
                sa(JJ)=1;
            else
                sa(JJ)=0;
            end
        end
    else  %ia<0  two large discharge/insert(1)
        for II=1:num
            JJ=II+num;
            if(II==seq2(3)||II==seq2(4))
                sa(JJ)=1;
            else
                sa(JJ)=0;
            end
        end
    end
end
```

Appendix C. Relevant Published Work

1. Y. Zhong, S. Finney, and D. Holliday, "An investigation of high efficiency DC-AC converters for LVDC distribution networks", in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD)*, Manchester, 8-10 April 2014, pp. 1-6.

   Abstract:

   Low voltage DC (LVDC) distribution systems offer improved efficiency and reliability in smart grids. A major challenge facing LVDC systems is DC-AC conversion. A study of an effective low voltage DC-AC converter is therefore presented. Modular Multilevel Converter (MMC) performance (in particular power loss) is compared with a conventional IGBT-based 2-level converter and its advantages highlighted. A phase-shifted sinusoidal PWM based individual voltage balancing strategy for the MMC is presented. A proportional-resonant controller is introduced to eliminate the 2nd harmonic circulating current in the H-bridge MMC converter.

2. Y. Zhong, H. Derrick, and S. J. Finney, "High-efficiency MOSFET-based MMC for LVDC Distribution System", in IEEE Energy Conversion Congress and Expo (ECCE) Montreal, Spet. 20-24, 2015, May 2015.

   Abstract:

   Low-voltage DC (LVDC) systems offer a promising means for improving distribution system efficiency and reliability. The DC-AC conversion stage, however, is one of the main challenges for LVDC networks. A low-voltage modular multilevel converter (MMC) for LVDC distribution systems is proposed in this paper. Analysis is presented to show that its efficiency can exceed that of a conventional 2-level converter. The low voltage rating of each MMC submodule enables MOSFETs to be used in place of IGBTs to reduce power losses. The application of synchronous rectification (SR) further reduces

conduction losses. It is shown that device switching frequency reduces as the number of MMC levels is increased. MMC power losses, for different numbers of levels, are compared with those of a conventional 2-level converter. Simulation and experimental results are presented to confirm the mathematical analysis.

3. N.M. Roscoe, Y. Zhong, and S. J. Finney, "Comparing SiC MOSFET, IGBT and Si MOSFET in LV distribution inverters", in 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, Japan, 2015.

Abstract:
Efficiency, power quality and EMI are three crucial performance drivers in LVDC applications such as electrical supply, EV charging or DC aerospace. Recent developments in SiC MOSFETs and MMC for LVDC promise two significant improvements in LVDC inverter performance. However, the designer is left with many combinations of technology and inverter level to choose from. This paper aims to clarify this choice by identifying one optimum Si design and one optimum SiC design, using detailed loss calculations. An IGBT inverter is included as a baseline. Loss calculations estimate the effects of Si MOSFET switching loss and all parasitic interconnection loss. The validity of the loss estimations are verified using careful experiments on a Si MOSFET cell. Close agreement indicates that the modelling approach is valid for extension to many cells in series, and to the parallel connection of many devices. Despite the lower EMI inherent in MMC inverters, Si MOSFETs risk worse EMI, due to poor reverse recovery characteristic. Slowed device gate switching experimentally demonstrates the reduction in switching noise, promising very low EMI. This initial study has therefore identified two promising candidate SiC and Si MOSFET inverters which will be fully constructed in future work, in order to aid designers in choosing the optimum semiconductor technology and topology for LVDC inverters.

4. Y. Zhong, N. M. Roscoe, D. Holliday, and S. J. Finney, " MMC with Parallel-connected MOSFETs for LVDC Distribution", in The 8th IET International Conference on Power Electronics, Machines and Drives, Glasgow, UK, 2016.

Abstract:

A highly efficient DC-AC converter is key to the success of low-voltage DC (LVDC) distribution networks. Calculated power losses in a conventional IGBT 2-level converter, a SiC MOSFET 2-level converter, a Si MOSFET modular multilevel converter (MMC) and a GaN HEMT MMC are compared. Calculations suggest that the parallel-connected Si MOSFET MMC may be the most efficient topology for this LVDC application. In this paper, the current unbalance limits for the parallel-connected MOSFETs and the optimal number of parallel-connected MOSFETs for MMC are investigated. Experimental results are presented for current sharing in parallel-connected MOSFETs and for the verification of power loss in a single Si MMC module.