Advanced Transfer Printing:

Tools and Applications

PhD Thesis

S. P. Bommer

Institute of Photonics

Department of Physics

University of Strathclyde, Glasgow

October 2, 2025

Dedication

I dedicate this thesis to my parents, my family and my soon to be wife Hayley.

To my Mother, I want to thank you for all the support you have given me and my siblings. You have always said you want to provide an even better life for your children than you had. I believe you have achieved this, you have made sure that every one of your children had the opportunity they desired available to them. I cannot think of an instance where you have prevented me from doing what I loved, except if it was dangerous or short sighted. For that I am grateful.

To my Father, you passed on to me a curiosity about how things work and the motivation to make the things you want. Your passion for tools and DIY have directly translated into core skills that I use daily. I believe those days in the house watching "How Its Made" and "Mythbusters" is what started my interest in Physics and Engineering. Without that foundation I wouldn't be where I am now.

To my future wife Hayley, without your encouragement I may not have enrolled in university at all. The support you have given me to push myself out of my comfort zone was instrumental to developing me in to who I am today. I look forward to marrying you and I hope we can continue to help each other grow.

Declaration

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Acknowledgements

I would like to thank my first supervisor, Prof Michael Strain. The guidance he has provided over the 8 years I have been under his tutelage has helped me grow as a researcher. The atmosphere he brings to the IoP inspires personal development. He has provided me both the scope to pursue my interests, but also the guidance needed for me to get things done. For this I am truly grateful.

I would also like to extend my thanks to Dr Benoit Guilhabert, despite not being so on paper, he became my de facto second supervisor. Working together on TP2 was an incredible experience, and him providing me the room to contribute to such a critical system is the reason I have a thesis at all. I look forward to working with him in the future.

I would like to thank the colleagues that started the PhD in IoP alongside me, Dr. Nils Wessling and Dr. Eleni Margariti. I don't think I could have asked for a better cohort to begin the project with. We were able to push each other from the very beginning. Without that sense of friendly competitiveness I am not convinced I would have achieved half the things I have in this project.

I would like to thank the post-docs directly above me also, Dr. John McPhillimy, Dr. Jack Smith and Dr. Dimitars Jevtics. Your willingness to share your knowledge with anyone that is ready to put the effort in is substantial. I can only imagine the how much longer this thesis would have taken if not for your contributions.

I would like to extend a wider thanks to the rest of the IoP, everyone of you is so open and friendly that it makes working here not feel like work.

Contents

Chapter 1

Introduction

1.1 Introduction

Photonic integrated circuits (PICs) are often compared to integrated circuits (ICs), and for good reason. Several decades after their invention in the late 1940s, ICs revolutionized industry by solving "the tyranny of numbers" [1]. Before their development, complex systems required hundreds or thousands of individual vacuum tube components, connected by intricate networks of wiring. This system was costly to maintain, as the interconnects (rather than the replaceable vacuum tubes themselves) became the primary source of expense for industries. This expensive maintenance would have resulted in a plateau of innovation and scale, as any benefit gained by more complex systems would have been counteracted by their operational costs. That was until the invention of the integrated circuit.

Integration of components onto a single substrate enabled the reliability of electronic devices to be greatly increased, at the expense of more complex and costly fabrication and a reduction in repairability. However, this approach was easier to justify to industry. A large initial investment could be warranted by the prospect of a long operational lifespan, allowing companies to recover costs over time. Once a system reached the end of its life and became irreparable, it was simply replaced with the latest model from the manufacturer—thus perpetuating a cycle of generational improvements. This enabled quick development of IC technology over the course of decades and as the technology

continued to advance, the infrastructure to support its manufacture also improved to match it. This enabled the devices to become cheaper overall, further accelerating this cycle of development. By the year 2000 the field of ICs had advanced to the point that Jack Kilby of Texas Instruments was awarded the Nobel Prize in Physics for his contributions to its invention [2].

PICs emerged in the 1980s as a solution for high-speed data transmission and optical communication. Just as with electronics, researchers aimed to shrink and integrate multiple components onto one substrate, such as lasers [3], modulators [4] and detectors [5]. Unlike with ICs, no one material platform became dominant in the photonics space, with early development being driven by gallium arsenide (GaAs) for manipulation of photons and indium phosphide (InP) for their generation. Now it is common to see inclusion of silicon (Si) PICs due to its prevalence in electronic foundries and its compatibility with complementary metal-oxide-semiconductor (CMOS) processes.

As with electronics, PICs have seen benefits when moving to an integrated platform in terms of size, weight, power and cost (SWaP-C). A typical free-space optical setup can be measured on the meter-scale whereas a PIC is typically on the centimetre-scale [6]. By dramatically reducing the size of the system, improvement can be seen in temperature stability due to the reduction of material mass and variation of thermal expansions [7, 8]. Improvements in power efficiency are also present, particularly for non-linear applications due to their reduction of modal volumes.

The reason no particular material dominated the manufacturing of PICs in the same way silicon did for ICs is because of the diverse set of optical functions needed for their operation. For ICs, the building block of most components is the transistor, functioning as an electronic switch allowing low current logic to control high current circuitry. This one component can be found in nearly every circuit device, from microprocessors [9], amplifiers [10] and displays [11]. For PICs no such component exists that perform as diverse a selection of functions as a transistor. As such, a diverse set of material types are necessary for PICs to compete with their IC equivalents. These materials can be split into three classifications of operations as shown in Table 1.1, which is a non-exhaustive sample of such.

Category	Material
Generation	Indium Phosphide [12], Gallium Arsenide [13], Gallium Nitride [14]
Routing + Manipulation	Silicon [15], Silicon Nitride [16], Lithium Niobate [17], Polymers [18]
Detection	Germanium [19], Indium Gallium Arsenide [20], Silicon [21]

Table 1.1: **Photonic material types and their function.**

As seen in the table each material platform has strengths in one or two categories, but falls short in the other(s), as such no monolithic device can facilitate the breadth of applications needed for telecommunications [22], quantum computing [23] and sensing [24]. This is further complicated by the operational bandwidths of materials. For example silicon absorbs light $< 1\,\mu m$ in wavelength making it useful for routing at $> 1\,\mu m$ and detection at $< 1\,\mu m$ but not both simultaneously. Additional complications arise when looking at non-linear applications where different materials have different non-linear coefficients. For example, Lithium Niobate ($LiNbO_3$) has a high $\chi^{(2)}$ non-linearity making it useful for second harmonic generation [25] and in optical parametric oscillators [26], however it has a lower $\chi^{(3)}$ non-linearity compared to Aluminium Gallium Arsenide (AlGaAs), thus making AlGaAs the preferred choice for photon-pair generation [27] and super continuum generation [28].

The variation in optical properties required to perform for any given task in photonics necessitates multi-material integration techniques for integrated photonics. This is why heterogeneous integration techniques have a large focus placed on them in research.

1.2 Overview

The work detailed in this Thesis discuss the development of new transfer print technologies, and how transfer printing as a technique is suited to tackle several challenges in the integrated photonics sector. Discussed also in this work are the current road-

blocks preventing integration of more advanced materials. In this chapter the reader will be shown the all the context required to understand both the advantages and the limitations to delve into the level of detail provided in the later chapters.

1.3 Monolithic Photonic Integrated Circuits

Before discussing methods of multi-material integrated PICs, its best to first provide a description of monolithic circuits, as the underlying functional principles for both remain the same. For integrated photonic circuits light is confined within waveguide structures, forcing the electromagnetic fields into discrete transverse modes. These guiding geometries can be fabricated using various combinations of lithographic patterning, etching and deposition on semiconductor material, which will be discussed later. These guiding structures serve as the building block of many PIC devices, from routing structures, resonators [29], interferometers [30] and on-chip lasers [31] etc. These transverse modes represent a stable field distribution within the guiding structure and are determined by a combination of its geometry and refractive index (RI).

The RI of a material, or more specifically the ratio of the refractive index of the guiding medium to the surrounding cladding layer, given as the refractive index contrast (RIC) given in Eq. (1.1) determines the level of confinement of a propagating mode.

$$RIC = RI_{guide} : RI_{cladding} \tag{1.1}$$

In free-space optics it is common for $RI_{cladding} = RI_{air} = 1$ due to a lack of an additional cladding layer around the optics. However, for integrated photonics it is common for waveguides to be clad in materials with a variety of RIs, as seen in Fig. 1.1. The RIC of any waveguide gives an indication of how tightly confined a mode can be within a guiding structure. A high RIC allows for a small waveguide cross-sectional area, which is advantageous for some non-linear processes as it allows the intensity of mode to be high whilst using nominally low injection power.

As a mode propagates through the waveguide, coupled mode theory indicates that a small portion of that field propagates in the area directly surrounding the waveg-

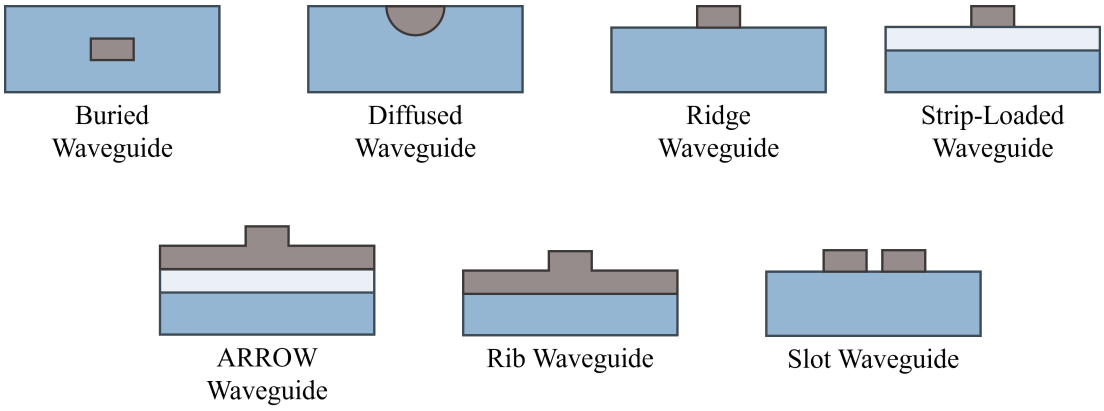

Figure 1.1: **Examples of different waveguide structures**

uide [32]. This is referred to as the evanescent tail of the mode, and is sensitive to perturbations of the surrounding environment. As such, it is responsible for scattering losses caused by the surface roughness of guiding structures [33], or sharp changes in RIC of the surrounding area. The evanescent tail is also what allows coupling between photonic structures.

As the evanescent tail of one guiding structure overlaps the geometry of another guide, a portion of the propagating mode transfers into the secondary structure. The amount of light coupled is proportionate to several parameters, such as the geometry and composition, their separation and the length of the coupling region. By tuning each of these parameters it is possible to control the amount of light coupled into the secondary structure, This forms the basis for various devices such as resonators [29] and couplers [34].

Many hybrid/heterogenous devices rely on evanescent coupling to facilitate connections between integrated devices as it allows for the coupling of light without the need for a mating structure between components. This allows hybrid devices to be compact in footprint as well as providing a level of standardisation between different types of structures as coupling parameters can be tuned by simply changing the spacing between the coupled geometries. Decisions like this can be made during the design process of the fabrication workflow, before the fabrication and packaging stages.

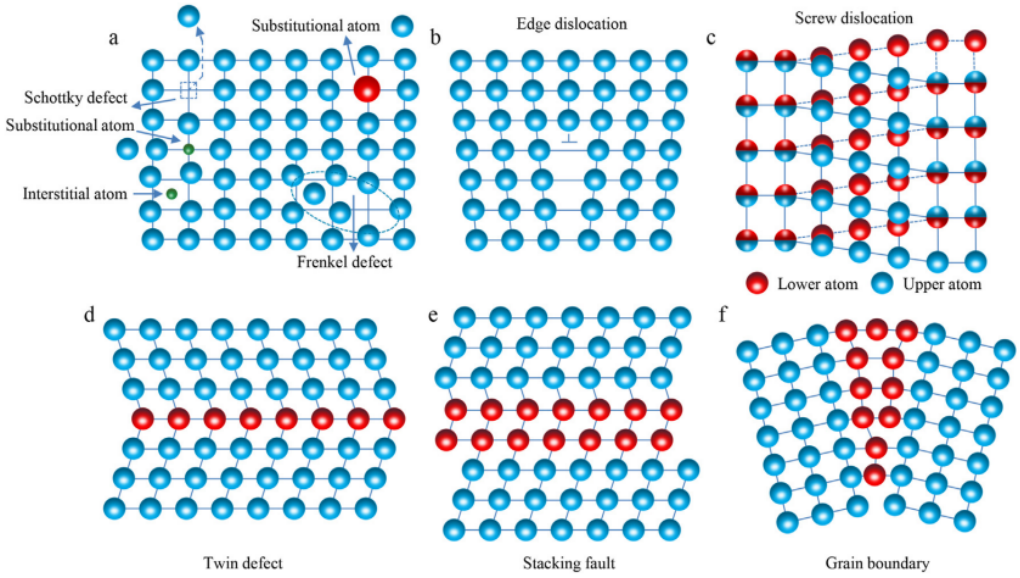

Figure 1.2: **Schematic illustrations for the different types of crystal defects.** (a) Point defects include doping and vacancies. Line defects include (b) edge dislocation and (c) screw dislocation. Plane defects include (d) twin, (e) stacking dislocation, and (f) grain boundaries. [38]

1.4 Chip-Scale Integration

The underlying crystal lattice mismatch between various semiconductor materials is a major challenge for hybrid integration of PICs as it prevents their combination during the growth stage via techniques like molecular beam epitaxy (MBE) [35] or metalorganic vapor phase epitaxy (MOVPE) [36]. The mismatch between lattice constants result in the generation of crystal dislocations amongst other flaws in the crystal structure [37]. Intermediate growth layers that provide a gradient region between the material layers can improve this, but result in a large spatial separation between layers as the transition layer is much thicker than the device layers. An example of this can be seen in Fig. 1.2.

For many PICs, even if the transition layer wasn't needed, the inability to pattern lower layers with devices would severely limit the flexibility and density that could be achieved with PICs. As such many research institutes and industries focus instead on multi-material combination after the growth stage.

Hybrid integration techniques [1] are a method of stacking layers of different semiconductor material together after the initial growth stage on the wafer to device level. An example of this is wafer bonding, in which wafer stacks can be fused together with high temperature and pressure by thermal compression bonding (TCB) [39] or by use of optical grade adhesives. Both wafers can be fully or partially patterned beforehand, necessitating the need for wafer-scale alignment techniques [40]. It is not uncommon to remove the donor wafer's substrate layer, such that only the device layers are left as an inverted stack on the receiving wafer. This allows additional patterning to be defined on this device layer, increasing the complexity achievable compared to a single wafer.

Hybrid integration techniques are an excellent method to enable large-scale integration of multi material structures, particularly in terms of the capability of supporting parallel fabrication arrays of circuits by use of dicing techniques at the final step with no additional investment in fabrication time [41]. However, a downside with full wafer hybrid integration techniques is that if any further patterning of the wafer stack is required, then compatibility between the different material layers and their respective etch chemistries becomes a factor. When more than one material is present, then the whole wafer needs to be processed multiple times. This can be extremely challenging to achieve whilst avoiding damage to previously integrated layers/devices. The motivation of multi-material integration is to combine various optical properties onto one platform, the variety of optical properties come from the composition of the different semiconductors.

In either case, there are downsides to the workflow of wafer-scale hybrid integration techniques as the devices are repeatedly exposed to damaging etching steps. Kinetic etching processes, require use of sacrificial cladding layers to protect device structures [42]. Otherwise a global decrease in the surface quality can be seen leading to higher optical losses. The cladding can then be selectively removed via chemical-etching processes. Chemical etching can be tailored towards removing only the target material layers, however if the other layers in the wafer stack contain a similar composition it

[1] In literature it is common to see Heterogeneous and Hybrid integration used interchangeably. For this work Hybrid refers to wafer-scale integration techniques, whereas Heterogeneous integration focuses on the smaller device-scale integration.

is likely that unwanted etching of these layers will also be seen, albeit at a different etch rate. This can lead to instances where even though material stacks can feasibly be integrated together, their patterning processes become overly complex or impossible, preventing fabrication into a useful device. This problem only becomes more complex once more than 2 material stacks are required, which can severely limit the complexity achievable for PICs.

1.5 Device Level Integration

Similar to hybrid integration, heterogenous integration enables merging of semiconductor material by stacking layers on top of one another, however heterogeneous integration focuses on the transfer of device-scale components rather than entire wafers. This enables the assembly of multi-materials as a back-end process, in that complete components can be assembled together as pieces of a complete PIC with no additional patterning stages required. By assembling only completed components, the damaging etch processes can be grouped to the relevant material, reducing the overall number of processes that any circuit component is exposed to.

Some examples of heterogeneous integration are flip-chip printing, where after fabrication the component is inverted and adhered to the substrate by means of reflow soldering [43] or thermal compression bonding enabling the connection of on-chip lasers or detectors onto silicon substrates [44]. Typically flip-chip techniques are utilised for components on the millimetre-scale. Another example is through use of self assembly techniques, by utilising surface tension [45] or capillary action [46] it is possible to align μ-components onto substrates. Typical applications of self-assembly are in the construction of quantum dots and nanowire arrays [47] where parallel assembly of components can be achieved. This enables transfer of components that would otherwise be challenging due to their footprint being $< 10 \times 10\,\mu m^2$.

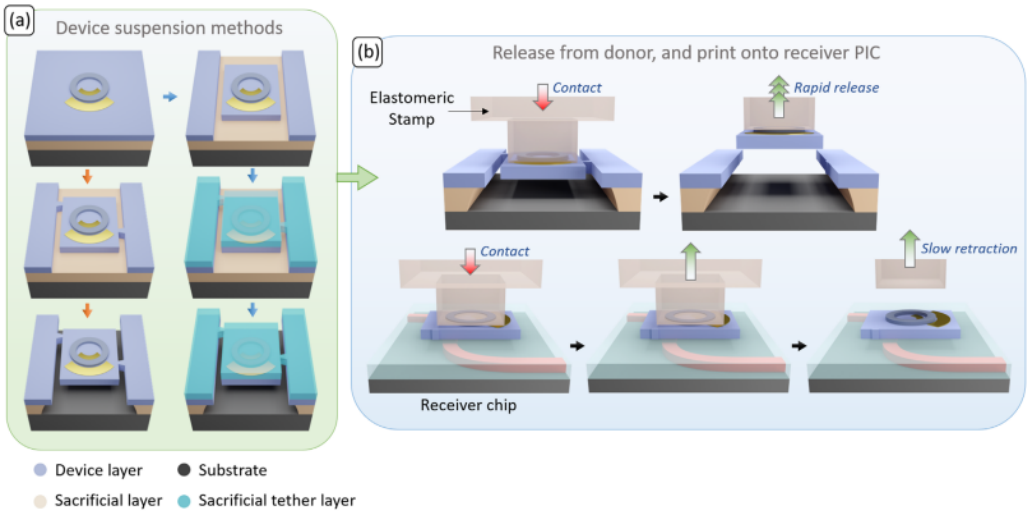

Figure 1.3: **Generalized schematic of the transfer-printing of membrane photonic devices.** (a) Two processes by which suspended membranes may be fabricated, with tethers either monolithically fabricated in the same layer as the devices, or patterned in a sacrificial resist layer to which the top surface of the membrane adheres after the under-etch of the substrate. (b) Simplified demonstration of the process of retrieving from the donor and printing onto the receiver PIC, using an elastomeric stamp. [51]

1.6 Transfer Printing

A further technique, and the focus of this thesis, is transfer printing. This is a μ-assembly technique that is capable of integrating a diverse set of materials and components on the $10^0 - 10^3$ micron length scale. This is achieved by use of a soft elastomeric stamp, typically made from polydimethylsiloxane (PDMS), to pick and place prefabricated device coupons like μ-LEDs [48], lasers [49] and sensors [50]. This process is compatible with both a diverse range of membrane devices and substrates. The pick and place mechanism relies on the reversible adhesion properties of PDMS to enable preferential transfer to the receiver substrate. This removes the need for the high temperatures seen in processes requiring solder reflow and thermal compression bonding, making it compatible with flexible devices and complex PICs.

Transfer printing emerged in the early 2000s as a promising technique for heterogeneous integration, enabling high precision integration of component coupons of diverse materials. Initially being developed for flexible electronics and bio-integrated

devices [52–54], the method quickly gained attention in the photonics field due to its level of compatibility with different material types and sizes. A significant milestone in transfer printing's history was from the work of John Bowers group at University of California, Santa Barbara (UCSB). They demonstrated successful transfer of high performance III-V lasers directly onto silicon photonic circuits [55], overcoming the technical hurdle that was silicon's poor light-emission properties. At which point interest in the technique spiked with several institutes incorporating it into their fabrication flows in the following years.

Within the Institute of Photonics (IoP) at the University of Strathclyde (UoS) several sub categories of transfer printing have been explored. Serial printing is where the singular devices are transferred in a deterministic manner, this is what is most commonly thought of when transfer printing is mentioned and represents a significant portion of the work done within the group. Serial printing allows the most control over the transfer process by operating on the component-level. This allows users to pre-characterise devices on the donor chip and downselect the ones to be transferred. This is particularly useful for donor devices where the spectral characteristics cannot be controlled during the design process, such as nano-wires and quantum dots. For these devices the fabrication process results in scattered distributions of donor components making them incompatible with multi-device transfer techniques.

Parallel transfer printing is the process where periodic arrays of devices can be picked from the donor substrate in sets of 2 or more and transferred to the receiver substrate, with their device pitch maintained throughout [56]. This method is typically faster than serial printing when used on matured material platforms, but provides many of the same benefits in terms of absolute alignment accuracy. Here the pitch and layout of donor devices must be complimentary to that of the receiver as it cannot be adapted during the print process. This method is ideal for when arrays of devices are required, such as pixel displays [57] and solar cells [58]. Schematics of serial and parallel transfer printing can be seen in Fig. 1.4.

Lastly, mass transfer techniques help bridge the gap between wafer-scale hybrid methods and transfer printing by enabling the simultaneous printing of entire arrays

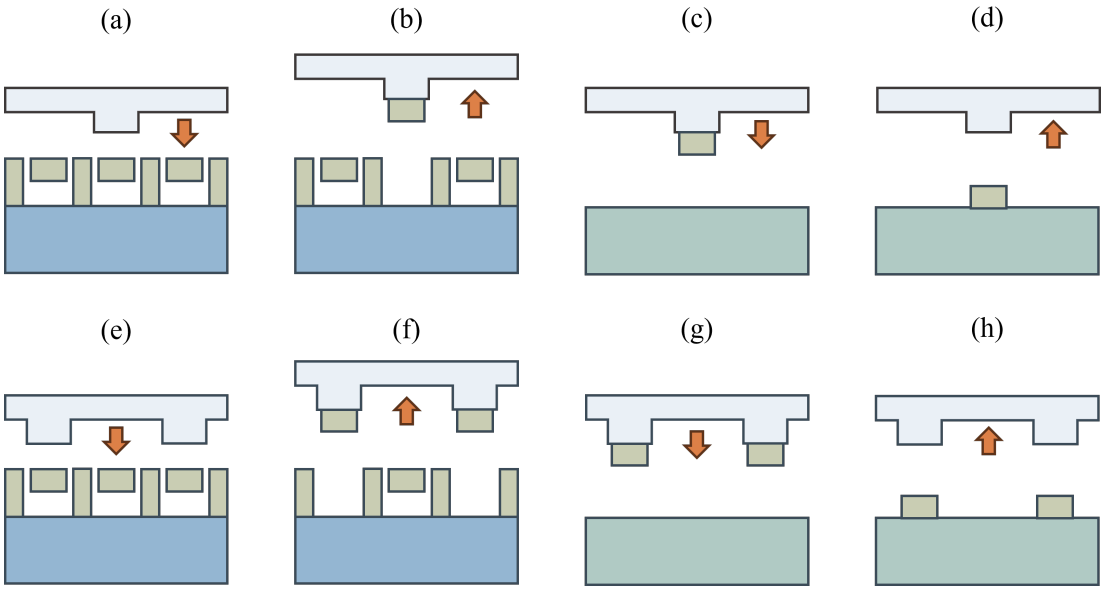

Figure 1.4: **Serial and Parallel Printing.** (a-d) Process of pick up and release for serial printing, as one device is printed at a time the pitch between devices can be controlled. (e-h) Parallel printing enables printing of more devices at once, with the pitch of devices remaining fixed within a batch.

of donor devices. Within the IoP this is implemented using a continuous roller system, where samples are moved under a roller coated with adhesive elastomer. The roller facilitates continuous device pickup and release, driven by the same linear stage that the donor and receiver chips are mounted. While alignment accuracy may be sacrificed due to the lack of through-stamp imaging, this system has demonstrated printing of over 75,000 devices in just 10 seconds [59], offering significant improvement in throughput compared to serial and parallel techniques.

Both parallel and mass transfer techniques are aimed towards typical industrial foundry applications where turnaround time and yield are significant factors. This is great for many devices such as μ-LEDs for high resolution displays [60], flexible-electronics for smart wearables [61] and μ -lenses for advanced imaging systems [62]. However, the most adaptable of these techniques is serial printing by allowing tailored printing strategies of devices on a device-to-device basis. This is particularly useful during process development, as the majority of transfer prints process flows are "discovered" by empirical testing in the lab.

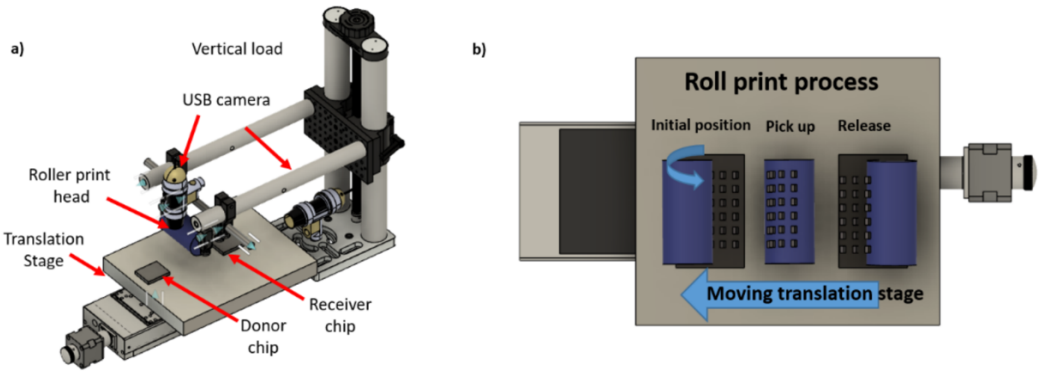

Figure 1.5: **Roller Printing.** (a) Schematic representation of the roll printing setup. (b) Printing process (left to right), devices are released from a donor onto the roller print head and then released onto a receiver chip. [59]

1.7 Serial Transfer Printing

As mentioned earlier, serial transfer printing (TP) enables high accuracy printing of individual devices in a deterministic manner. This enables flexibility in the selection of devices as their position on the donor substrate is decoupled from their position on the receiver substrate. This enables devices to be easily characterised before assembly and sorted e.g. by wavelength or Q-factor, during the assembly stage [63] as well as variations in the spatial density between donors and printed devices. An example of this will be discussed in-depth in Chapter 4 of this thesis. This flexibility in device selection also enables TP demonstrations of novel material platforms where fabrication issues have limited the yield of donor coupons, and example of which can be seen in Fig. 1.6.

TP is capable of precision printing where accuracies less than $0.1\,\mu m$ have been achieved [64], a particular practical demonstration within IoP of this printing accuracy was demonstrated in work by Dr John McPhillimy [65] where an AlGaAs disk resonator was printed with increasing overlap to an underlying waveguide, this change in overlap allowed selective coupling to higher order modes within the disk highlighting how the performance of a PIC can be controlled at the printing stage. More recent demonstrations have also highlighted the capability of TP based integration onto novel substrates,

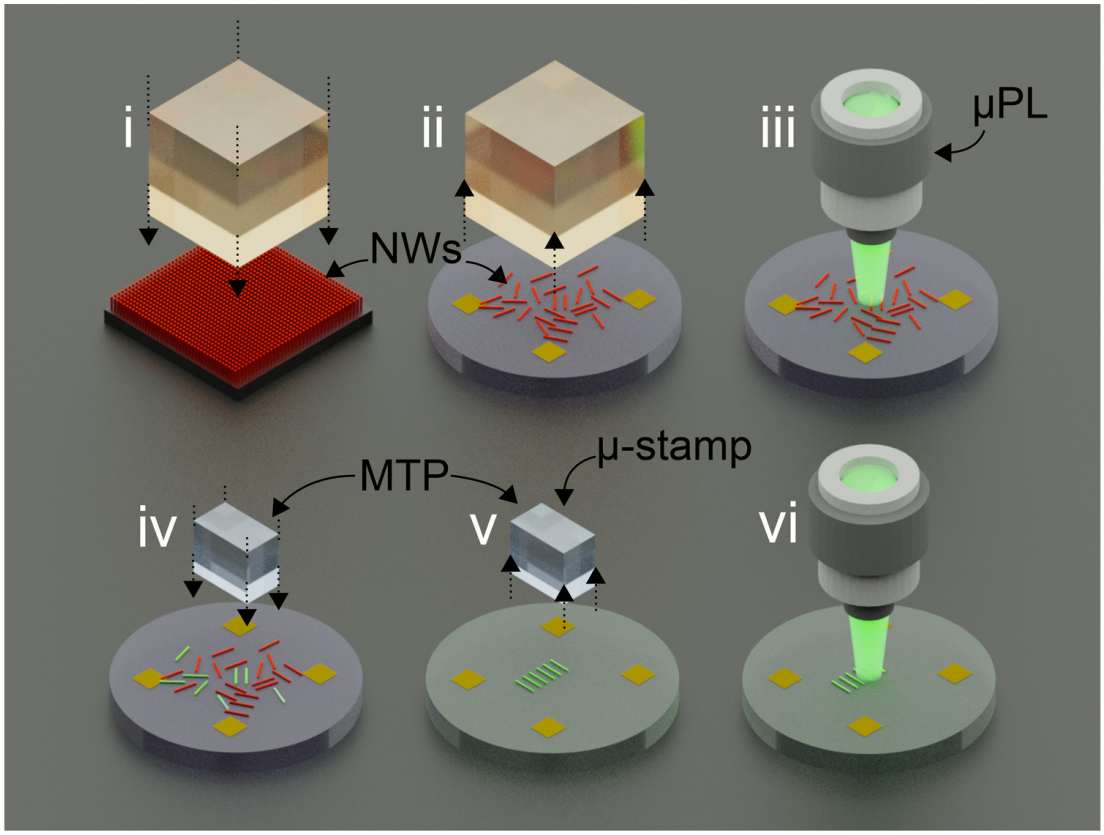

Figure 1.6: **Deterministic Sorting of Nanowires.** (i) NW lasers on their growth substrate are released using a large PDMS block, (ii) transferred onto a target quartz disk, and randomly distributed on the surface. (iii) Device populations are characterized using an automated scanning microscopy system and binned by threshold. (iv) Selected NW devices are individually picked using a PDMS μ-stamp and (v) printed onto a second substrate in regular arrays. (vi) Target devices are recharacterized with the system. [63]

for example several articles highlight the integration of photonic devices onto fibres and waveguide facets [62, 66]. An example of printing a μ-lens structure onto the end of fibre facet will be discussed in Chapter 3.

The dynamic adhesion characteristics of PDMS is what enables serial TP, in particular its dependence on velocity [67, 68]. When PDMS is brought into contact with the surface of a device, the stamp can conform around the surface of the structure. This promotes formation of Van der Waals (VdW) interactions [69] allowing adhesion to the surface of the stamp. By applying a fast retraction of the stamp, a large force can be applied to the sacrificial support structure of the coupon causing it to break and release the device. Detailed discussion on designing coupons for TP can be found in Chapter Chapter 4. The fracture occurs in a time frame shorter than the relaxation period of the PDMS allowing the coupon to remain adhered to the stamp. After this, the coupon can then be bought into contact with the receiver where VdW forces can form with the underside of the coupon. The slow retraction speeds then allow the stamp to gently peel off the surface of the coupon resulting in stamp to component adhesion being less than the component to substrate adhesion.

The mechanical relaxation behavior of PDMS is determined by the density of cross-linking between its polymer chains. When the bulk material is deformed, the chains attempt to move, but cross-linked regions restrain this motion, increasing relaxation times and making the material more elastic. The PDMS used in this work (Sylgard 184, supplied by Sigma-Aldrich) is typically prepared at a 10:1 ratio of base polymer to curing agent, a mixture that provides reliable curing and favourable mechanical properties for high-resolution casting. The base polymer consists of long PDMS chains with vinyl end groups, while the curing agent contains silane cross-linkers and a platinum catalyst to drive the reaction.

PDMS is generally chemically inert and hydrophobic, which leads to poor adhesion to most surfaces. However, Van der Waals forces from the methyl groups along the chains are sufficient to enable transfer printing applications. The ratio of base to curing agent directly tunes the cross-link density and therefore the rigidity of the material: increasing the proportion of base yields softer, more compliant PDMS that can better

conform to the surface of a device, while increasing the proportion of curing agent produces stiffer, more brittle PDMS that adheres less effectively. Ratios above 15:1 (base:curing agent) result in incomplete curing, while ratios below 5:1 yield a glass-like, brittle polymer.

It is possible to increase the dynamic range of stamp adhesion of any one stamp by implementing additional geometries such as pyramid structures at the corner of the stamps [42]. This enables printing onto more challenging substrates where the VdW forces of the substrate are not as high due to factors such as surface finish and composition. The inclusion of pyramid structures enabled flip-chip style integration of a GaN LED [66]. This was achieved by control of the pyramid geometries of two stamps, allow stamp-to-stamp transfer of the LED structure before a final printing stage. Different methods of dynamically changing the adhesion force during printing exist [70,71]. Typically they will limit some other aspect of the printing process, usually visibility through the stamp.

PDMS being transparent is one of the key enablers for high accuracy printing, as many of other integration techniques require the contact stage to be done "blind". This means that device alignment then relies on a calibration step and various assumptions during the integration process. When operating at print tolerances of $\approx$ 100 nm a blind process becomes sensitive to any and all sources of error within the system. With optically clear stamps it is possible to see the printed devices during the entirety of the printing process enabling verification of alignment at any stage of the process as seen in Fig. 1.7. This also enables implementation of machine vision based strategies for high precision integration, as the donor and receiver substrates are visible during the integration process also [64].

The primary transfer printer setup is shown in Fig. 1.7, and referred to internally as TP1. Multiple demonstrations of advanced printed strategies have been made on this machine, in-particular in machine vision assisted printing. TP1 one was created from a modified NLP2000 Dip Pen Nano-lithography system from Nanoink. Designed originally to deposit micro droplets of inks and various biomaterials for bio-organic and microfluidic applications [72]. This system was shared many of the specifications

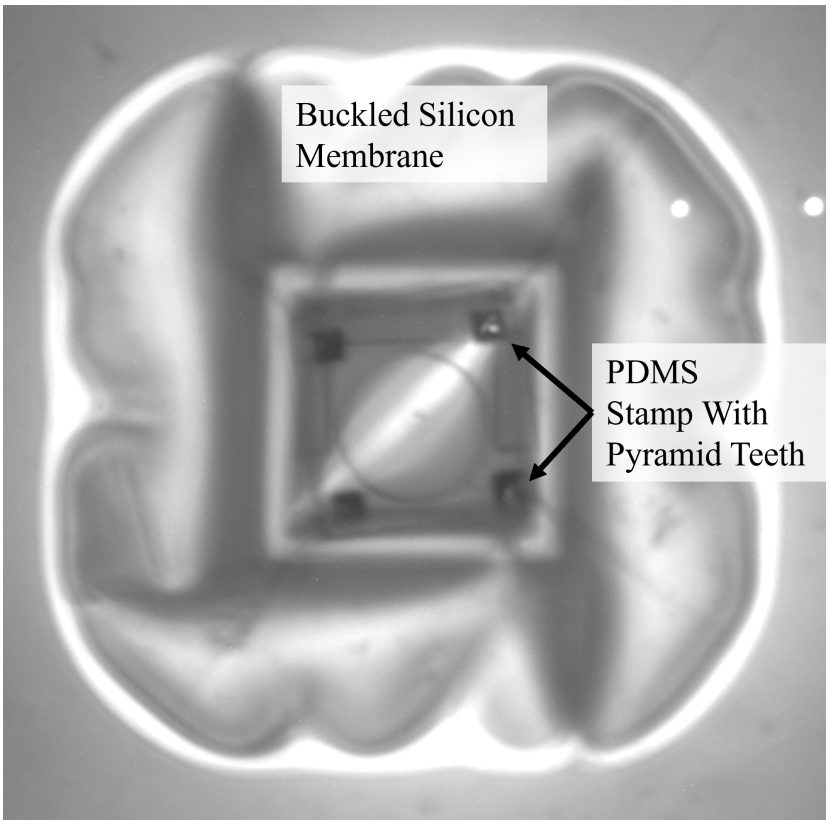

Figure 1.7: **Through stamp imaging.** Photograph from transfer print system imaging through PDMS stamp. Edges of stamp structures appear opaque, as well as pyramid structures. Any faces that are parallel to imaging plane appear transparent.

needed for a transfer printer, it is capable of impressive motion precision of ±5nm with a minimum step size of 100 ± 25nm. The built-in high resolution microscope enables imaging with a resolution down to 300 nm. The system was kept much the same as the stock machine, but with the inclusion of a rotation stage for control of the θ_Z axis. The μ-pipette system was swapped for a PDMS stamp holders.

1.7.1 Current state-of-the-art

Recent advances in transfer printing have enabled the integration of diverse materials onto various substrates with high precision. For instance, researchers have successfully integrated centimetre-long thin-film LiNb devices onto silicon nitride platforms using micro-transfer printing, achieving propagation losses of approximately 0.9 dB/cm and transition losses of 1.8 dB per facet [73]. Additionally, programmable micro-transfer printing systems utilizing sharp phase-changing polymers and μ-heater arrays have demonstrated dynamic selectivity, facilitating the transfer of materials ranging from micro-scale coupons to nanometre-thick films [70].

Advancements in transfer printing have also focused on the integration of pre-characterized devices to ensure optimal performance in heterogeneous systems. For example, the IoP have developed methods to characterize nanowire laser populations using automated optical microscopy, followed by high-accuracy transfer printing with automatic device spatial registration. This process allows for the selection and integration of nanowire lasers based on their performance metrics, facilitating the assembly of high-quality photonic systems [63, 74].

While numerous "hero" demonstrations have showcased the potential of transfer printing, there is a growing need for ensemble demonstrations that address scalability and manufacturability. Future research should focus on developing high-throughput processes capable of integrating large arrays of devices with consistent performance. This includes refining techniques to ensure uniformity across transferred devices and developing robust methods for yield management during large-scale manufacturing [59].

In the industrial sector, transfer printing has been employed for the heterogeneous integration of μ-scale compound semiconductor devices onto silicon substrates, offer-

ing a cost-competitive path to commercialization. Micro-transfer printing has been demonstrated for several compound semiconductor applications, providing practical methodologies for large-scale integration. Additionally, advancements in transfer printing techniques have facilitated the development of flexible electronics, enabling the fabrication of devices on flexible substrates with complex surface morphologies [75, 76], for applications in wearable devices and robotic sensing.

1.8 Limitations of Transfer Printing

To discuss advancements in transfer printing, it is useful to clarify the metrics the advances are being gauged against. Several metrics are prioritised in research, such as transfer yield, the number of devices mechanically transferred from the donor substrate onto the receiver versus the amount "lost". This is usually measured on large sample sets where statistical techniques can be used. A common industry standard is a 6σ process, corresponding to a yield of 99.99966%. Another metric is the printing accuracy, how small is the print window, the area in which a coupon can be guaranteed to reside within, and its standard deviation. If a process has a large print window, then that enables freedom with respect to receiver design and device density. small print windows tend to be limited to "hero" devices [65] or those that facilitate alignment tolerant designs. The metric that was focused on in this project was the yield of functioning devices. This is decoupled from transfer yield and accuracy as it inherently factors in the device to device variations caused by the fabrication process. In some cases a functioning device could perform poorly in terms of print accuracy such as Fig. 1.8. In this figure the coupon was intended to be printed at a 45°angle with respect to the waveguide such that the optical mode would only interact with the shallow etched portion of the coupon and the ring resonator, minimising unwanted perturbations. During the release process a rotation was introduced, causing a small portion of the coupon edge to overlap the underlying waveguide. The area overlapping was measured to be of negligible consequence to the circuit's optical performance. This combined with the ring resonator being inherently resilient to rotational misalignment due its circular

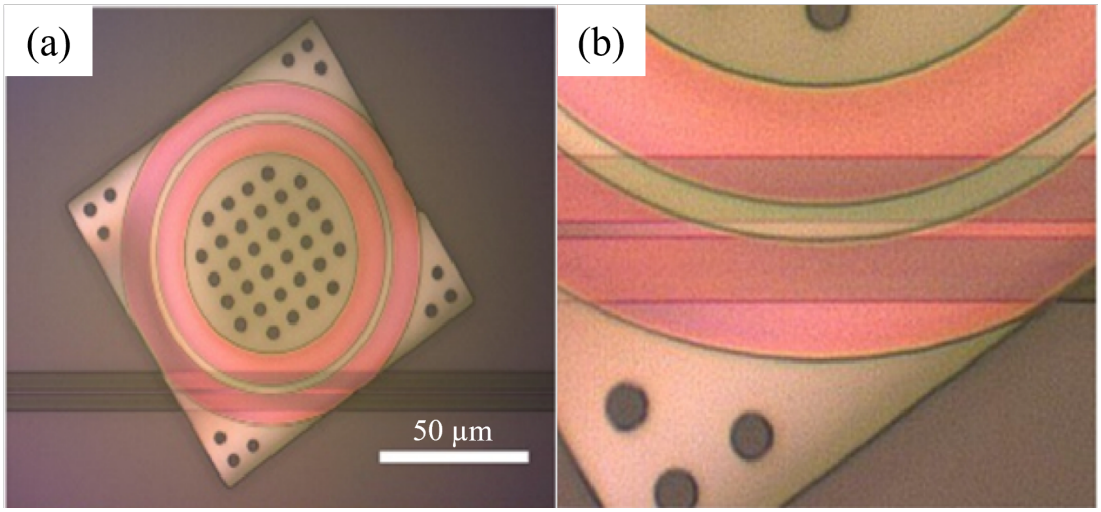

Figure 1.8: **LiNb membrane ring on SiN waveguide.** (a) Microscope image of a transfer printed lithium niobate ring resonator overlapping a silicon nitride waveguide device. Membrane was intended to be rotated to a 45° angle to the waveguide to avoid corners of coupon overlapping the waveguide. (b) Shows magnified view of waveguide overlapping region.

profile, allowed the device to function as intended despite being out of alignment.

Placement errors typically arise from the conformal properties of the stamp head, which deforms to match the device structure. While this compliance allows for better contact, it also limits the accuracy of the printing process when alignment features are used. The transfer relies on reversible adhesion forces between the stamp and device, and the operator has no direct way to measure these interacting forces. Experience can help mitigate errors through consistent printing strategies. As will be discussed in Chapter 2, the inclusion of high precision stages such as the SmarAct system can improve precision. However, errors will still persist due to factors like vision system resolution, device fabrication, and stamp compliance.

1.8.1 Optical Injection and High-Accuracy Transfer Printing

A significant challenge faced when integrating high quality photonic components on chip is verifying their performance either before or during the integration process. For waveguiding devices in particular this is a challenge as the typical method of coupling light into the component is via overlapping their evanescent fields with an already active

waveguide. This can typically only be achieved once the device is already integrated onto the receiving structure. This can cause a significant waste in time and materials as the testing process occurs near the end of production. However, where electrical circuits typically need all contacts to be connected for current to flow in the circuit, photonic circuits can be optically driven even when components are not yet integrated. This opens up the opportunity monitor the optical performance of the whole circuit during the assembly stage to determine the quality of components as they are being integrated, as well as compensating for variations in performance due to fabrication variations. Small variations in device performance due to surface roughness can often be compensated for by minor adjustments to the device placement at on the receiver. If the circuit can be monitored during the assembly stage, the device performance can be identified before the final device contact with the receiver. This would ensure consistency between batches of printed devices. At the start of this PhD project, no such system existed that facilitate both high precision placement of transfer printable devices as well and optical measurements for device verification.

1.8.2 Standardisation and Tooling for Thin-Film Membrane Devices

The integration of thin-film semiconductor membranes via transfer printing presents a second critical challenge: the lack of standardisation and design tools tailored for sub-500 nm devices. These ultra-thin membranes are essential for enabling monolithic and heterogeneous photonic integration, particularly in single-mode optical applications. However, to maintain single-mode operation and sufficient mode confinement, the printed membranes—and often their etched features—must reside in regimes below 100 nm. At this scale, mechanical fragility becomes a serious concern, and the absence of specialized design and simulation tools makes intelligent device layout cumbersome and imprecise. Without proper design environments, the field struggles to establish reproducible processes for sacrificial layer release and membrane handling, which impedes efforts to standardize fabrication flows. This issue becomes especially critical as photonics continues to diverge from electronics in its demand multi-material integration at the device-level. (A more in-depth exploration of these limitations and proposed

solutions is included in Chapter 4.)

1.8.3 Suspended Devices and Throughput Constraints

The fabrication of suspended photonic devices through transfer printing is essential for achieving high-Q resonators, yet presents a multifaceted challenge. Traditional TP demonstrations often rely on full or partial contact between the printed device and the substrate, which inherently limits the refractive index contrast and thus the confinement needed for single-mode, low-loss performance. In contrast, suspended devices—surrounded by an air cladding—enable not only higher Q-factors but also improved modal purity, and open up functionalities like evanescent field sensing. However, transferring these structures is inherently difficult due to TP's dependence on contact area, making suspended geometries mechanically unstable during pick-and-place operations. This challenge is further compounded when integrating ensembles of devices, as Q-factor performance is highly sensitive to nanoscopic fabrication variations, necessitating pre-characterization and selective printing, which slows down throughput. Addressing this bottleneck will require innovations in both process stability and integration strategies that allow in-situ testing prior to release or detachment.

1.9 Thesis Outline

In this thesis, solutions to some of these challenges will be presented. A short background on photonic fabrication technology will be given in Chapter 2 and is intended to get the reader familiar with the relevant technology and terminology used in the rest of this Thesis.

In Chapter 3, an introduction will be given to the custom-built transfer print system within the IoP cleanroom. Details on the design of the system is given with a focus on the modularity of the platform. This modularity is then utilised in the development of an optical measurement system capable of in-situ monitoring of photonic integrated circuits. The techniques and considerations used during the development of the setup will be discussed. An application of transfer printing μ-lens structures onto a single

core fibre facet with alignment achieved via a targeted illumination strategy is discussed enabling marker free accurate alignment. Several additional demonstrations will be given to highlight the versatility and the types of integration the system can achieve.

Following this, Chapter 4 will discuss a methodology developed in this project for the design of suspended membrane structures in the form of a Python package. This methodology allows convenient generation of membrane photomasks with a selection of layout and design tools. This package is also compatible with any foundry library that utilises Shapely for its back-end, such as GDShelpers, GDSfactory and Nazca [77–79]. Integrated in this library is a method for the generation of conformal layouts of etching holes to mitigate issues in fabrication of thin-film isotropic material. To support this, analytical tools were developed to be able to evaluate the etch characteristics of structures during the design stage. This enables the co-fabrication of various membrane designs on one chip that otherwise would have been prohibitively challenging.

The final results chapter will return to the injection system developing it further to include a cross-polarised microscopy setup. Allowing for in-situ spectral measurements of photonic crystal cavities (PhCCs) during the integration process. This enables unique insights into the transfer process that have been immeasurable in prior work up until now. This development allows for wavelength sorted transfer of 119 devices without need for post fabrication trimming. Highlighting the versatility of in-situ measurement technologies, not only in reducing fabrication time but also in improving the quality of fabricated devices.

The thesis will conclude with an overview of the work carried out over the course of this PhD and its implications on the field of transfer printing as a whole. An outlook to the future will be provided, highlighting what can be done with the developments presented to continue pushing this technique towards the cutting edge of heterogeneous photonic integration technology.

Chapter 2

Background

2.1 Device Processing

In the manufacture of PICs, every devices goes through a process flow to take it from device conceptualisation to a finished device. Each process flow is broken down into a sequence of steps, some of which can be shared across various devices to allow parallel fabrication. The number and specifics of each process step can vary widely, making it challenging to discuss device progression across devices. As such, it is useful to split these steps into broad stages of design, front-end and back-end to enable comparison.

These stages are followed in sequence with design coming first. In which the geometry of the device is generated with the use of design tools such as KLayout [80] and GDSfactory [78]. Often simulation tools are used in this stage to test the geometries virtually, such as Lumerical [81] or Tidy3D [82]. Following this is the front-end Stage, consisting mostly of lithography, etching and deposition steps. Often metrology measurements will be included between these steps to ensure fabrication is progressing as intended. Finally, back-end process are done to take the device to its packaged form. This includes steps such as wafer dicing, wire bonding of electrical contacts and embedding devices in protective housings etc. Device testing can occur at either the front-end or back-end stage, to validate the device's performance as it progresses through the process flow.

These categories are separated in such a way that a step in one stage does not affect

any steps in another stage. For example, the fabrication of red, green and blue light emitting diodes (LEDs) requires a unique set of front-end processes for each separate channel. However, the back-end process of wiring and packaging in a transparent housing remains the same [83]. A brief description of key front-end and back-end processed can be found in the following sections. For a discussion on the Design stage, please see Chapter 4.

2.1.1 Front-end

2.1.1.1 Lithography

Lithography is a method transferring geometry onto the surface of a wafer, typically by ultra-violet (UV) light patterning of photo-curable polymer called photoresist. This resist can be deposited onto the surface of a wafer by conformal spray coating [84] or resist spinning techniques [85] to precisely control the thickness of the deposited layer. This can then be exposed to structured UV light, by mask-based projection, digital light processing (DLP) projection or direct-write laser-lithography amongst others [86]. The spatial structure of the light is determined by the design of the PIC device, resulting in a binary image determining where material is kept and where it is removed. For positive tone photoresist, regions exposed to UV light have their polymer bonds broken due to the light-matter interaction. These broken polymers are then susceptible to chemical developing solutions, allowing exposed regions to be selectively washed away. For negative-tone resists, the exposed regions instead undergo a curing process, becoming rigid from exposure to the UV. The unexposed regions can then be selectively removed by use of a solvent rinse. This allows for straightforward transfer of device patterns onto the photoresist, which can then be transferred to the semiconductor material via etching steps.

2.1.1.2 Etching

Etching is the process of eroding away the layers of the wafer to transfer the patterns created in the photoresist into the semiconductor material, falling into broadly into

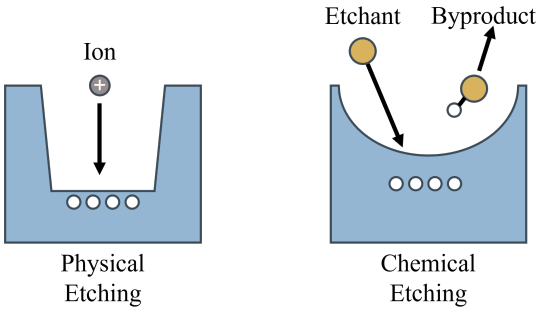

Figure 2.1: **Kinetic and chemical etching.**

categories of dry and wet etching. Both dry and wet etching procedures use tailored "recipes" for the selective removal of material layers, with the methodology broadly falling into two categories of kinetic and chemical etching and seen in Fig. 2.1.

Kinetic etching is a physical method of removing material, high-energy ions bombard the surface of the semiconductor and break away sections of the crystal lattice. Noble gases are used in this process due to their large size and inertness, such as Argon, Krypton and Xenon [87]. Acceleration of these ions occur in reactive ion etching tools (RIEs) where a plasma cloud is created in a vacuum above the semiconductor target. Kinetic etches tend to be more agnostic to the material being etched compared to their chemical counterpart. Chemical etching can occur in dry process tools such as an RIE, or via wet-etching techniques in solution [88]. In either case, a reactive ion or molecule is used that contains dangling bonds, these bonds then preferentially attach to the atoms in the semiconductor lattice, where the atom-to-atom attraction of the etchant is stronger than that of the lattice. The now inert etchant can then be removed after the etching process. Chemical etches tend to be more material selective than their kinetic counterpart.

2.1.1.3 Deposition

Deposition techniques allow formation of additional layers of material onto the surface of the wafer, typical techniques use chemical vapour deposition (CVD) and plasma-enhanced chemical vapour deposition (PECVD), in both cases the wafer is loaded into a vacuum chamber where a gas shower head introduces precursor gases such as

silane (SiH_4), ammonia (NH_3) and oxygen (O_2) etc. For CVD a temperature range of $600°C - 1100°C$ is used to cause a chemical reaction between the wafer and the precursors [89]. This generates a thin layer of material on the surface as well as by products that are pumped away. For PECVD lower temperatures $100°C - 400°C$ can be used as an RF power source is instead used to ionise the precursor gases into a plasma, making it more susceptible to chemical reactions at the wafer surface.

2.1.2 Back-end

2.1.2.1 Metallisation

Metallization in photonic fabrication is a critical back-end process that involves depositing and patterning metal layers to enable electrical interfacing with active photonic devices such as modulators, photodetectors, and thermal tuners. Metals like aluminum, gold, titanium, and platinum are commonly used, depending on the required conductivity, adhesion, and compatibility with subsequent packaging steps. The process typically begins with a thin film metal deposition using techniques such as sputtering, evaporation, or electroplating. After deposition, photolithography is used to define the metal pattern, followed by either lift-off or etching to remove unwanted areas. In some cases, a thermal annealing step is performed to improve contact resistance or to form metal-silicide junctions. Proper metallization ensures low-loss electrical routing and is essential for high-speed and high-density integration of photonic-electronic systems.

2.1.2.2 Planarization

Planarization is the process of flattening the wafer surface to create a uniform and smooth topology, which is especially important in multilayer photonic integration. As various material layers are deposited and etched throughout the fabrication process, surface topography can become highly uneven, causing issues with lithography focus, alignment, and layer stacking. Chemical Mechanical Polishing (CMP) is the most widely used planarization method, combining mechanical abrasion with chemical etching through a rotating pad and slurry. This technique is typically applied after the

deposition of dielectric materials like silicon dioxide or after metal filling in holes to prepare the surface for further processing. Effective planarization minimizes dishing, erosion, and other surface defects, enabling precise layering and reliable performance of complex photonic circuits [90].

2.1.2.3 Dicing and Packaging

Dicing and packaging represent the final steps in photonic chip fabrication, where individual dies are separated and integrated into usable modules. Dicing involves cutting the processed wafer into discrete chips using diamond saws or laser-based methods, with care taken to avoid damaging sensitive photonic structures, particularly waveguide facets used for optical coupling. After dicing, each die is mounted into a package that provides mechanical support, environmental protection, and electrical and optical connectivity. Optical packaging may include alignment and attachment of optical fibers to on-chip grating couplers or edge couplers, often using active alignment techniques to minimize coupling losses. Electrical connections are made via wire bonding or flip-chip bonding to interface the chip with external circuits. Thermal management components such as heat sinks or thermoelectric coolers are also integrated when needed. High-quality packaging ensures the chip performs reliably in real-world applications while protecting it from mechanical and environmental stress.

Chapter 3

Transfer Print Instrument Build

3.1 Introduction

Transfer printing is a highly precise technique for integrating heterogenous devices, enabling both in-plane [91] where light propagates along the bounds of the chip and out-of-plane assemblies [62] where light is emitted or absorbed perpendicular to the chip. In-plane integration often benefits from existing structural features such as waveguides, ring resonators, electrodes, or heating pads, which serve as spatial references during the alignment process. These features are typically an order of magnitude larger than the printing window, allowing machine vision techniques [92] to achieve sub-pixel alignment with high accuracy.

For out-of-plane structures, similar alignment strategies can sometimes be applied [93]. However, the features surrounding the emission or detection points are generally much smaller than those in in-plane configurations, making machine vision alignment more challenging. This issue is further exacerbated in vertical passive structures, where the absence of well-defined reference features around the printing window limits the effectiveness of conventional alignment methods. As discussed in the previous chapter, Transfer printing is uniquely capable of compensating for a range of printing challenges due to both its simplicity in the integration process and its device level processing.

To aid in the development of new transfer print technologies a custom-built transfer printing tool was developed that functions not only as a system for high accuracy

transfer printing, but one that can operate additional tools in parallel to the printing processes. The modularity of the system enables tool modules to be actively developed and prototyped within an transfer printing environment, unlocking new potential technologies for transfer printing. The first module developed was designed to aid in the alignment of passive out-of-plane optical structures, as well as other applications discussed later in this chapter.

The first module provides a methodology for vertically injecting light through the microscope system and is discussed in this chapter. The injected light appears as a tightly focussed spot within the transfer printer's vision system, and allows relative positioning of the spot to allow coupling of light into various optical structures. This allows a light source to always be present and controllable during the transfer printing stage, opening up opportunity for optical performance based print alignment verification.

The development process of the both the transfer printer and the optical injection setup are discussed in detail within this chapter, including design criteria, optics, electronics and software. A experimental example is also given in the form of printing a μ-lens onto a fibre facet. Several other applications for such a system are discussed near the end of this chapter.

3.2 Acknowledgements

In this chapter, I would like to acknowledge the contributions from my colleague Dr. Benoit Guilhabert to my project via the construction and design of the transfer print system which will be discussed in the following section. I would also like to thank my colleague Dr. Nils Wessling for the development of transfer printable GaN μ-lens, which will be used as a demonstrator for the injection system later in this chapter.

3.3 Base System

The transfer printer used in this work, known internally as "TP2", is a custom-built system designed as an upgrade to the previous system, which was adapted from a

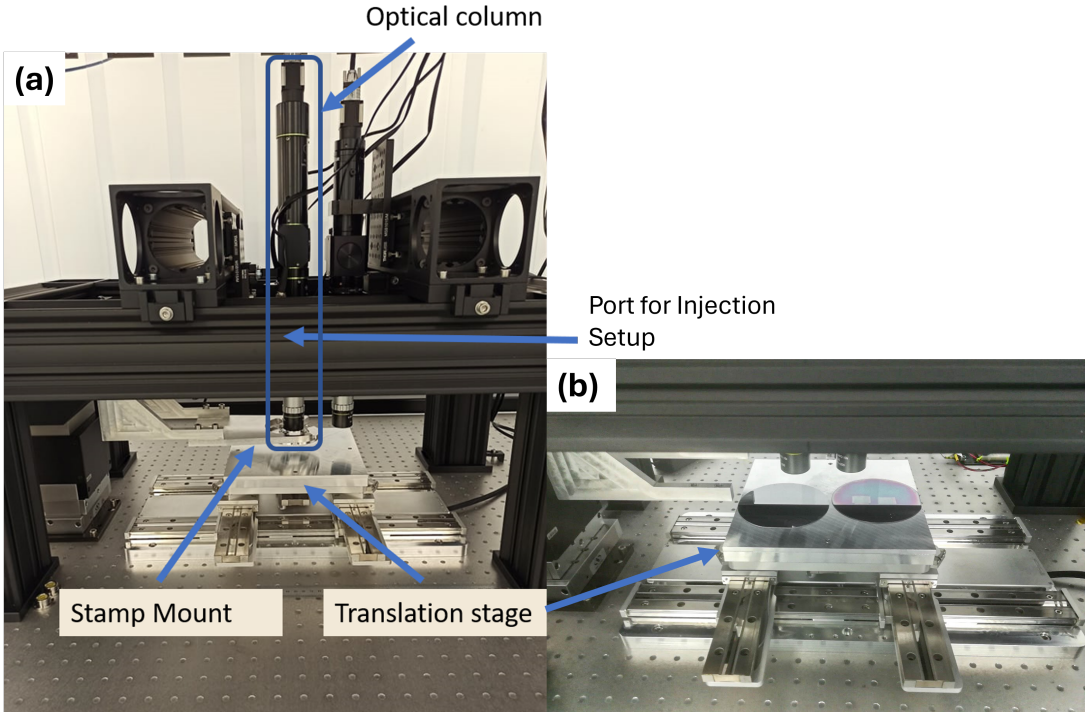

Figure 3.1: **Base Transfer Print Setup.** (a) Overview of custom built transfer print system. Frame is constructed from Thorlabs 95mm optical rails, providing a modular platform to the rest of the system. Translation stage is a high precision 6-axis motion system driven by piezo stick slip motors, built custom for this machine by SmarAct. The stamp mount is attached to an independent 3-axis translation stage to enable alignment of the stamp head to the microscope column. Optical column outlined in blue, with location in port for light injection annotated, which is obscured by the optical rail. (b) View of the translation stage with 2 4-inch silicon wafers mounted. The entire surface of both wafers can be scanned under the vision system enabling transfer printing of large device numbers comparible with industry requirements.

NLP2000 NanoInk Dip-Pen lithography tool. The construction of this system is shown in Fig. 3.1 and consists of the four main components of any transfer printer: the frame, the translation stage, the stamp system, and the vision system.

As can be seen in Figure 3.1 the printer's frame is constructed from 95 mm aluminium rails supplied by Thorlabs, providing structural rigidity while offering a range of mounting options that make the setup highly modular. This modularity has been utilised both in this chapter and throughout the work. The frame is designed to accommodate two different microscope configurations, allowing them to operate in tandem. One microscope, with low magnification and a wide field of view (FOV) is used for

coarse global alignment of wafers. While the other, a high-magnification system, enables precise local alignment of suspended devices. Either of these optical columns can be easily swapped out for another subsystem to support different transfer-print-based integration strategies.

The most significant improvement between the previous transfer printer and this revised version is the inclusion of a six-axis translation stage from SmarAct, seen in Figure 3.1(b). This stage offers nanometric precision and accuracy and is capable of mounting two 4-inch semiconductor wafers for large-scale integration experiments. It provides movement over a $200\,mm^2$ area with speed control ranging from $0.1\,\mu ms^{-1}$ to $10000\,\mu ms^{-1}$, offering a broad dynamic range of forces that can be applied during the pick-up and release stages of printing. Additionally, the stage supports several kilograms of load, allowing for the integration of various hardware components, including temperature control systems and mounts for novel substrates.

The stamp holder operates independently of the translation stage and accommodates larger-form-factor PDMS stamps mounted on 1-inch diameter glass slides. These stamps can be vacuum-mounted to the holder, ensuring a flatter and more stable positioning relative to the stage than mechanically mounted solutions. The vacuum chuck also allows transparent substrates to function as "stamps," enabling high-precision, flip-chip-like processes. Furthermore, the system maintains backward compatibility with stamps from the previous setup through the use of a 3D-printed adapter. The relative positioning of the stamp with respect to the microscope is controlled via a three-axis translation stage.

The primary microscope in TP2 is based on the Optem Fusion microscope system from Qioptiq, a modular platform that can be customised for a range of applications. This configuration includes motorised zoom and focus modules, enabling the automation of critical steps in the transfer process. During each stage of the print process, the stamp may be positioned several millimetres away from the substrate to prevent accidental collisions. At this distance, the stamp's geometry is no longer visible in the microscope's FOV, necessitating frequent focus adjustments to verify successful device pick-ups and to monitor the initial contact between the stamp and the substrate

surface. The automated zoom functionality allows the system to accommodate a wide range of suspended membrane footprints while maintaining consistent performance with standardised alignment markers [94].

3.4 Vertical Injection Setup

3.5 Optics

The primary microscope of the transfer print system features an additional port for adding secondary imaging systems or light sources. The injection setup is mounted to this interface and consists of a reflective collimator which produces a beam spot approximately 1.8 mm wide. This coupled to a 2-axis galvanometer then emits a steerable collimated beam. This then couples into a two lens telescope functioning as a beam expander, consisting of an $f_1 = 40mm$ and $f_2 = 150$ mm best form lenses in a 4f configuration [95]. This ensures the beam returns to collimated after the 3.75X expansion in beam size. This is then fed through the injection port of the microscope setup to the back aperture of the objective lens which is 6 mm wide, so the beam overfills the opening by 12.5 % which ensures a diffraction limited spot at the point of focus on the sample. A schematic view of the system can be seen in Fig. 3.2.

The module was intended to be compatible with as many photonics platforms as possible, meaning that operation from visible to short wave infrared wavelengths was essential [96, 97]. As such certain material choices were made to support this, such as the galvanometer mirrors being coated in silver and the telescope lenses are uncoated N-BK7 glass. The lenses are also of the "best form" type, where the flat back surface of a plano-convex lens is shaped such that it mitigates spherical aberrations. This helps minimise distortion of the beam shape when using the beam-steering functionality. These choices enable the injection system to be relatively agnostic to the particular wavelength source used. However through testing of different wavelengths it was found that the system is sensitive to chromatic aberrations which would result in the focal range of the injection setup not matching that of the imaging system. To combat this,

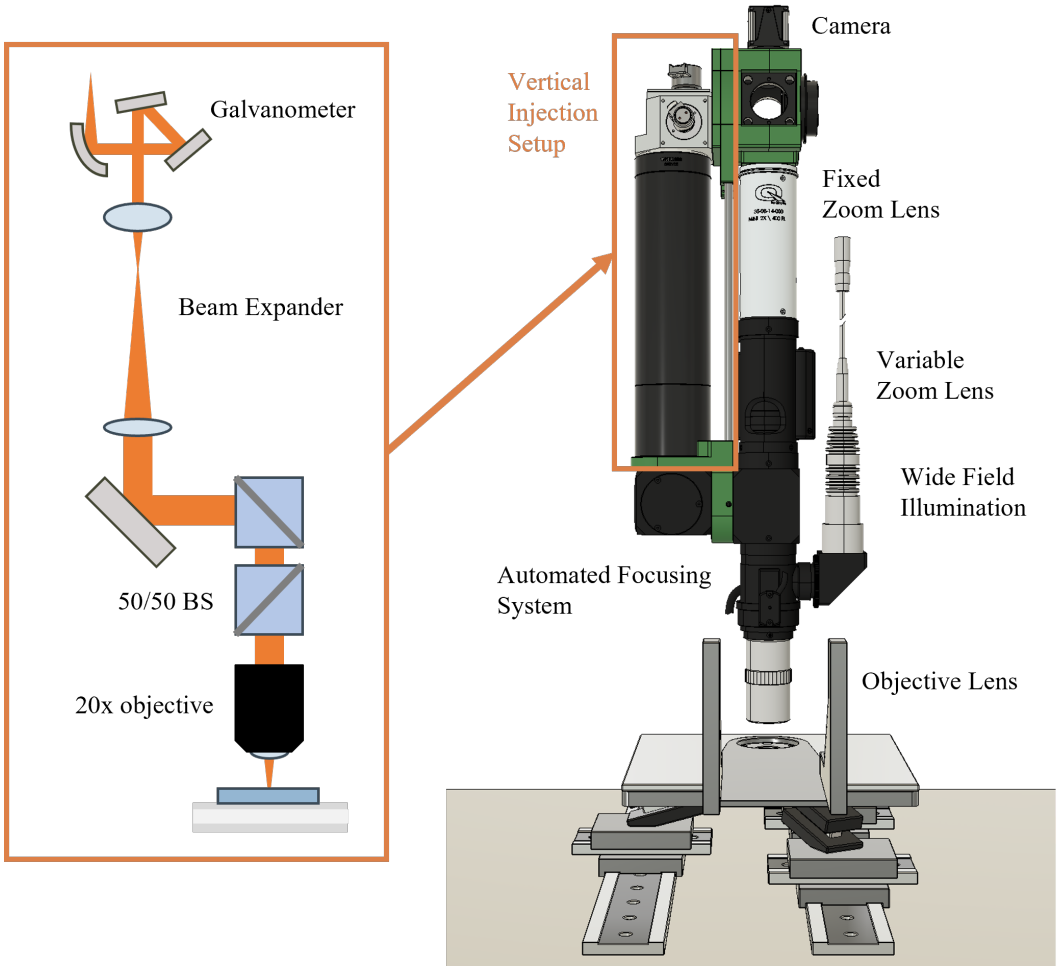

Figure 3.2: **Schematic view of setup.** View of the optical injection path highlighted in orange. Full view of system shown on the right, highlighting how the injection module fits within the vision system.

the inclusion of a large z translation mount for the f_2 lens was made, which offers 29.5 mm of travel, this allows the user to manually calibrate the focus of the injected beam after the source has been swapped.

3.6 Specifications

Among the core components of a transfer printer, the optical microscope is the most critical for this work, as it serves as the primary interface for the injection system, both optically and mechanically. The microscope's performance defines key metrics that inform the design of the injection system, which are detailed in Table 3.1.

Property	Low Magnification	High Magnification
Magnification Value	8.4x	58x
Field of View	0.72mm x 0.54mm	0.10mm x 0.07mm
Working Distance	34mm	34mm
Resolution	354 lp/mm	900 lp/mm
Depth of Field	0.041mm	0.0063mm
Numerical Aperture	0.12	0.30

Table 3.1: Specification for imaging optics on transfer printer.

Two of these properties were prioritised during the development of this system: resolution and field of view. The resolution, measured in line pairs per millimetre, refers to standardised reference patterns consisting of periodic line structures with a duty cycle of 50%, examples of which can be seen in Fig. 3.3.

As the period of these structures decrease it becomes more challenging for an imaging system to resolve their features accurately, as can be seen in Fig. 3.3 (b). The period of $8\,\mu m$ can be resolved accurately showing the correct number of lines and their overall shape is accurate. For a period of $4\,\mu m$ and $2\,\mu m$ inconsistencies in the widths of each line can be seen, however the correct number of lines are still visible. In the final set with a period of $1\,\mu m$ issues arise with the shape of the lines and the total number visible, with some of the lines now being absent. In this example the imaging system would be classified as accurate to a line pair period of $2\,\mu m$ (500 lp/mm). In high magnification mode, the microscope can resolve 900 lp/mm, which corresponds

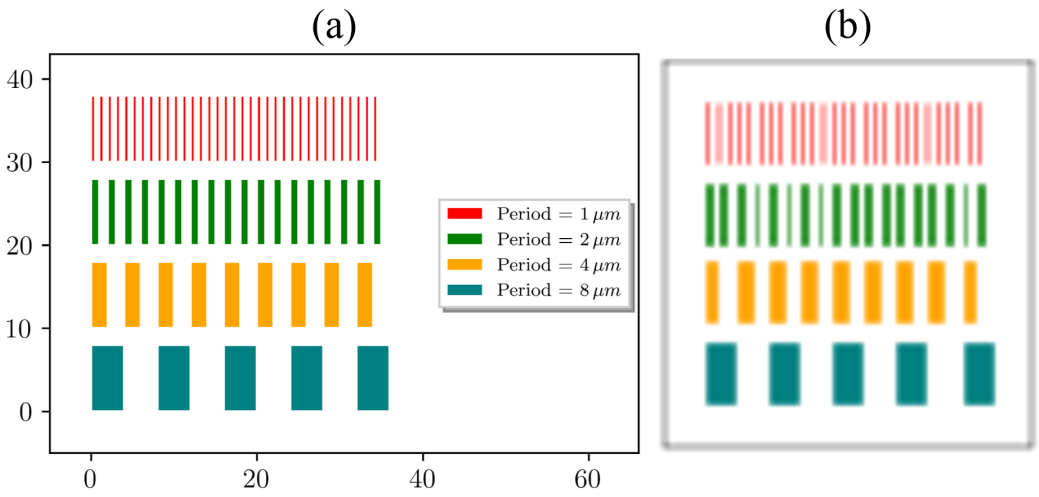

Figure 3.3: **Visual example of line pairs.** (a) Set of periodic line structures with increasing period length. (b) Intentionally low resolution duplicated of line pairs to represent the effect of imaging system not being able to fully resolve image. If (a) and (b) look indistinguishable, it is recommended that the reader refer to the digital copy.

to a line pair period of 1.11 μm which can also be represented as a sampling density of 1800 samples/mm. Using conservative estimations of the Nyquist limit, leads to a pratical sampling density of 1800/3 = 600 samples/mm, or 1 sample per 1.67 μm. As a target, the XY translation resolution of injection system was chosen to be half this line pair period to ensure that the beam steering could operate at the same resolution or higher than the imaging system, and was measured empirically to be $\approx 0.5\,\mu m$.

The latter property of the field of view corresponds to how much of the object can be visible at once and is inversely correlated to the image magnification. This provides a metric for the amount of XY travel the system needs to be able to target any structure on screen, examples of differently sized travel windows can be seen in Fig. 3.4.

Three differently sized travel windows are shown overlaid on top of the microscope field of view (FOV). The red window represents a case where the travel window is smaller than the FOV, limiting where the injection system can target on the chip. The orange window indicates a travel window that is the exact size of the FOV. While this may be suitable, it leaves no margin for error when aligning the injection setup to the microscope, making the system more susceptible to long-term mechanical drifts. The

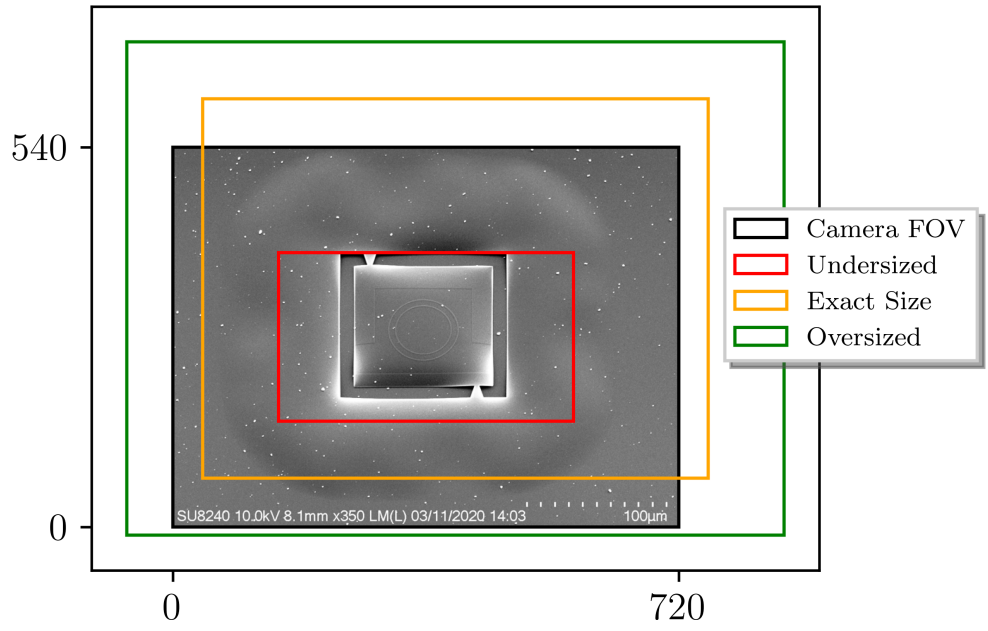

Figure 3.4: **Comparison of camera FOV and different XY travel windows.** Outlined in black is an SEM image of a suspended silicon membrane device to represent the FOV of the microscope. Differently sized travel windows are overlaid on the image to represent issues with their varying sizes.

green window represents the ideal case, where the Galvo travel window exceeds the microscope's FOV, allowing the excess motion to compensate for any misalignment of the setup. Due to the optical path of the microscope, the Galvo travel window does not change dynamically with changes in magnification. Therefore, the travel window should slightly exceed the largest FOV to ensure the system is compatible with as many PICs as possible. The design of the optical path and control electronics enabled this.

3.7 Beam Spatial Control System

The galvanometer consists of 2 rotatable mirrors orientated complementary to each other such that one mirror corresponds to X-axis motion and the other the Y-axis. To control the angle of the galvanometer mirrors, their driver boards need to be provided with an analogue signal, the voltage of this signal is then compared to ground to determine the deflection angle of each mirror. The driver boards support 3 control voltage ranges, 5, 12, and 15V which determine what signal is required to achieve their maximum rotation range of $\pm 12.5°$. It is recommended to use a digital to analogue convertor (DAC) which can approximate an analogue signal to a certain resolution dependant on its bit number, as seen in Fig. 3.5. A DAC functions by using a resistor ladder configuration [98], where various rungs of the ladder can be switched on and off to create different combinations of voltages in a manner similar to binary sequences [99]. The resolution of a DAC follows 2^n where n represents the bit number, such that a DAC with 8 bits can produce 256 voltages between 0V and its max operating range. Typically higher resolution DACs require higher operating voltages to work, as otherwise the minimum voltage step will be equal to or less that the noise floor of the power supply. This would make the produced signal inconsistent and result in the galvanometer oscillating when trying to hold a fixed position. Typically the max resolution of a 5V DAC will be 12-bit, corresponding to a voltage step of 0.0012V. Various combinations of control voltage, step modes and bit numbers are presented in Table 3.2. As the galvanometer couples into a sequence of relay optics, the perimeters of the max travel range cause the beam to be incident on the mounting hardware for

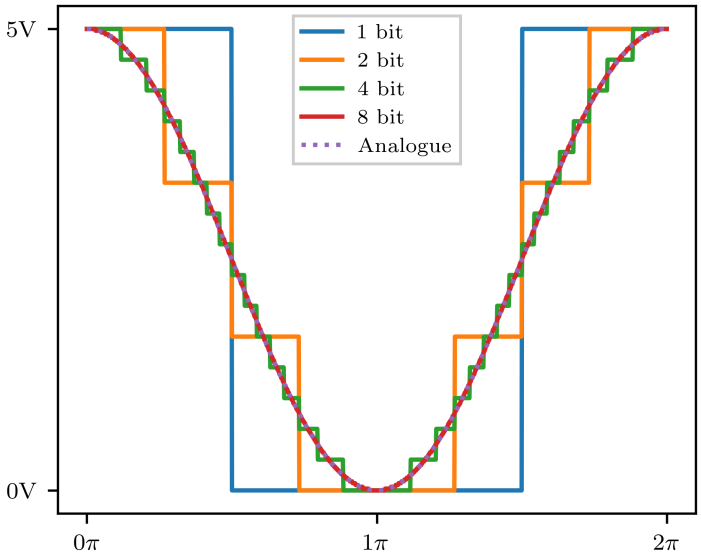

Figure 3.5: **Representation of a DAC signal.** Analogue signal shown as a purple dotted line, other colours show how the accuracy that the signal can be recreated is affected by the bit value of the DAC.

Control Voltage (V)	Step Mode (V/°)	Operating Range (°)	Bit Number (Resolution)	Voltage Step (V)
5	0.5	**10.0**	12 (4,096)	**0.0012**
	1.0	**5.0**	13 (8,192)	**0.0006**
	1.2	**4.2**	16 (65,536)	**0.0001**
12	0.5	**12.5**	12 (4,096)	**0.0029**
	1.0	**12.0**	13 (8,192)	**0.0015**
	1.2	**10.0**	16 (65,536)	**0.0002**
15	0.5	**12.5**	12 (4,096)	**0.0037**
	1.0	**12.5**	13 (8,192)	**0.0018**
	1.2	**12.5**	16 (65,536)	**0.0002**

Table 3.2: Key parameters when selecting control electronics for Thorlabs Inc. 2 axis galvanometer system. The module supports 3 separate step modes that correlate with 5V, 12V and 15V logic systems respectively. Combinations of different configurations are shown, A 16 bit DAC is recommended when used for high speed scanning operations, 12 and 13 bit configurations are discussed for point and click operation in this paper. Values in bold are a result of combining the previous column values

the optics and lost to scattering. As such it was found empirically that the full FOV of the system can be traversed when using a control voltage of 5V and a step mode of

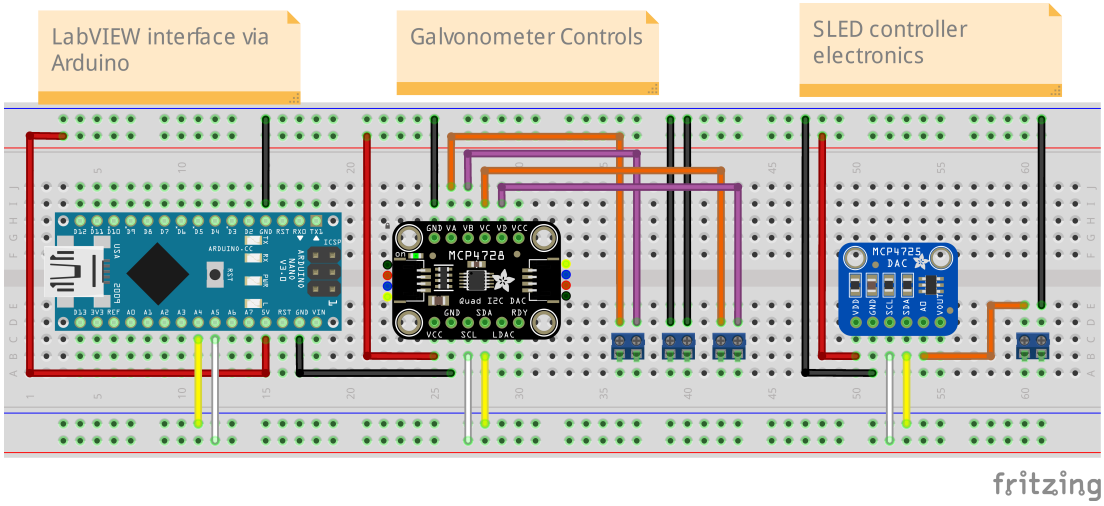

Figure 3.6: **Breadboard view of control circuit.** Visual layout of breadboard components assembled for the control of the injection setup. The quad channel DAC is shown in black and is connected to the 2-axis galvanometer. A second DAC board is shown on the right in blue, and can be connected to various light sources that support analogue signals to control output intensity.

1.2 V/°. This low voltage operating voltage requirement simplified the design of the control electronics.

The Arduino family of microcontrollers is a well-known 5V hardware architecture that is affordable and widely supported. It provides a range of general-purpose input and output (GPIO) pins and supports various communication protocols. One such protocol used in this work is I^2C, which allows for the daisy-chaining of multiple modules and can be controlled in an addressable manner [100]. This enables the use of external DAC modules, as, at the time of writing, no Arduino product had an in-built DAC with a resolution higher than 8 bits. The MCP4728 module from Adafruit supports four individually controllable 12-bit analogue outputs, allowing for two channels per galvanometer, as shown in Fig. 3.6.

Each galvanometer has 3 electrical connections positive (+ve), negative (-ve) and ground (gnd), typically the gnd and -ve terminals would be tied together allowing the rotation of the mirrors to be controlled entirely by modifying the analogue signal going to the +ve terminal. To maximise the effective resolution of this system, an alternate configuration was used where the both the +ve and -ve terminal where connected to

an output channel of the DAC. This allowed for 12-bit resolution for each half of the travel range, and an effective 13-bit over the whole travel range, but requires a software check when transitioning from a negative to positive rotation angle.

LabVIEW was chosen as the interface between the user and the control system because it is an industry-standard software platform that supports an extensive range of external libraries. A unique aspect of LabVIEW is that it allows for the parallel development of both the user interface and the computational logic. By utilising draggable blocks that can be wired together, LabVIEW enables one of the fastest methods for controlling multiple pieces of hardware in tandem with a user-friendly interface. At the time of writing, LabVIEW supports the LINX library, which facilitates direct communication with Arduino boards, allowing for the full operation of the microcontrollers within LabVIEW itself.

State machine architecture [101] was used in the development of the interface that allows for a responsive interface that is robust to errors and scalable development for when additional features from the system are required. One state in the machine is when the mirrors are transitioning past the 0° angle, during this transition the output tied to controlling the mirror is swapped to the other in the pair, whilst the opposing one is clamped to 0V. If both channels where driven above 0V, this would cause an error in the positioning system and give an inconsistent result. An image of the control panel for the injection setup can be seen in Fig. 3.7

3.8 3D Printing

As the microscope uses a proprietary connection system and the injection system was built from ThorLabs components, it was necessary to design custom parts to facilitate the interfacing of these two platforms. Since the system needed to be tested at various stages of development, rapid prototyping technology was employed to create mounting components for the setup, with the intention of replacing them with machined parts once the system was finalised. However, during testing, it was found that with proper design and material selection, 3D-printed components were suitable for the final revi-

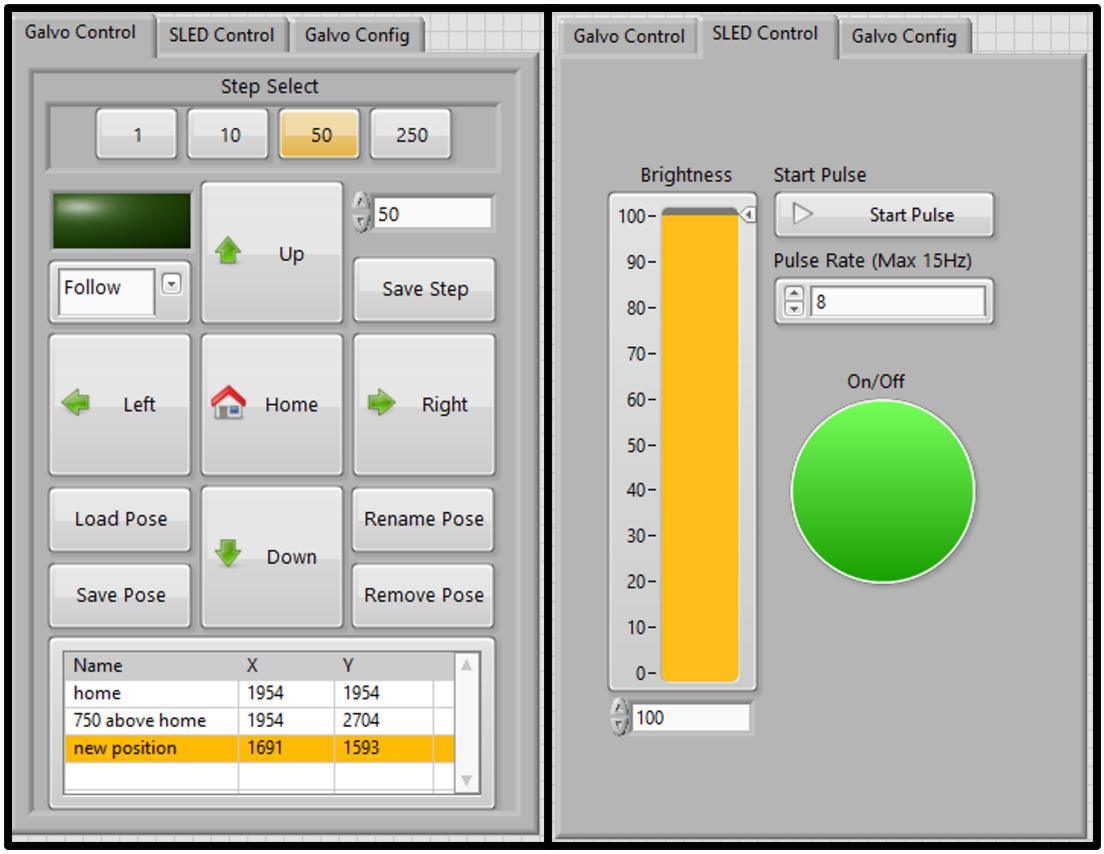

Figure 3.7: **LabVIEW Interface for Vertical Injection System.**

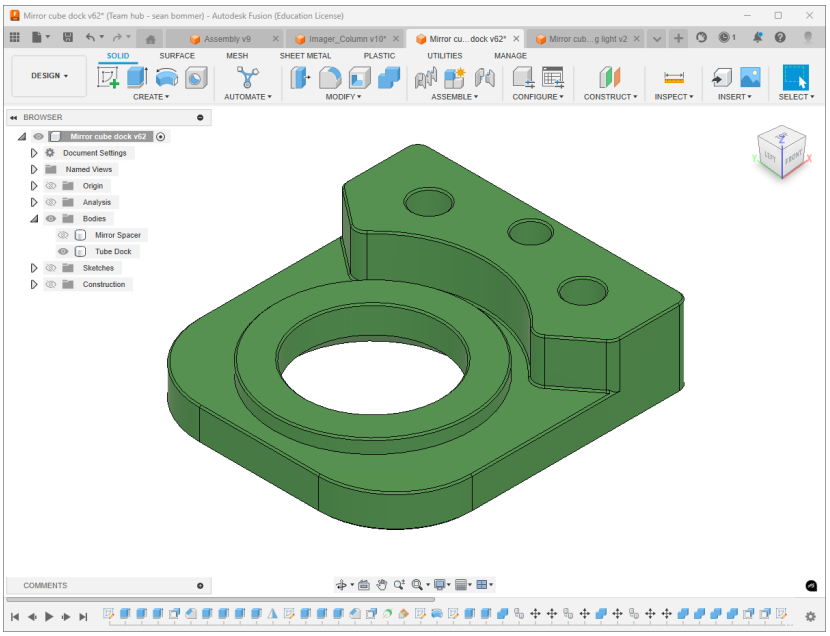

Figure 3.8: **Injection System Dock.** Image of the 3D printed Qioptiq to Thorlabs adapter within Fusion 360. The timeline visible at the bottom shows all the commands used to model the part, and can be "scrubbed" through to revert to a previous state for ease of editing.

sion. Most consumer-grade machines are able to reliably achieve print tolerances of 0.2 mm when printing with the standard nozzle diameter of 0.4 mm. This can be improved further to 0.05 mm in some instances based on material choice and tuning of print parameters to that specific material.

To design a part for 3D printing, a computer-aided design (CAD) package is used to generate a digital representation of the object. The CAD package used in this work is Fusion 360 which is a cloud-based service provided by Autodesk. Several mounts were designed and prototyped over the course of this project, one such part is the interface piece of between the Qioptiq column and the injection setup seen in Fig. 3.8. Fusion 360 allows definition of both dimensions and constraints, which enabled the precise modelling needed to ensure all mating pieces of the setup connected properly.

Once a CAD model is created, it must be processed using a software package called a "slicer" and the one used for this project is the open-soure "PrusaSlicer". The slicer converts the model into a format suitable for 3D printing by breaking it into layers of a

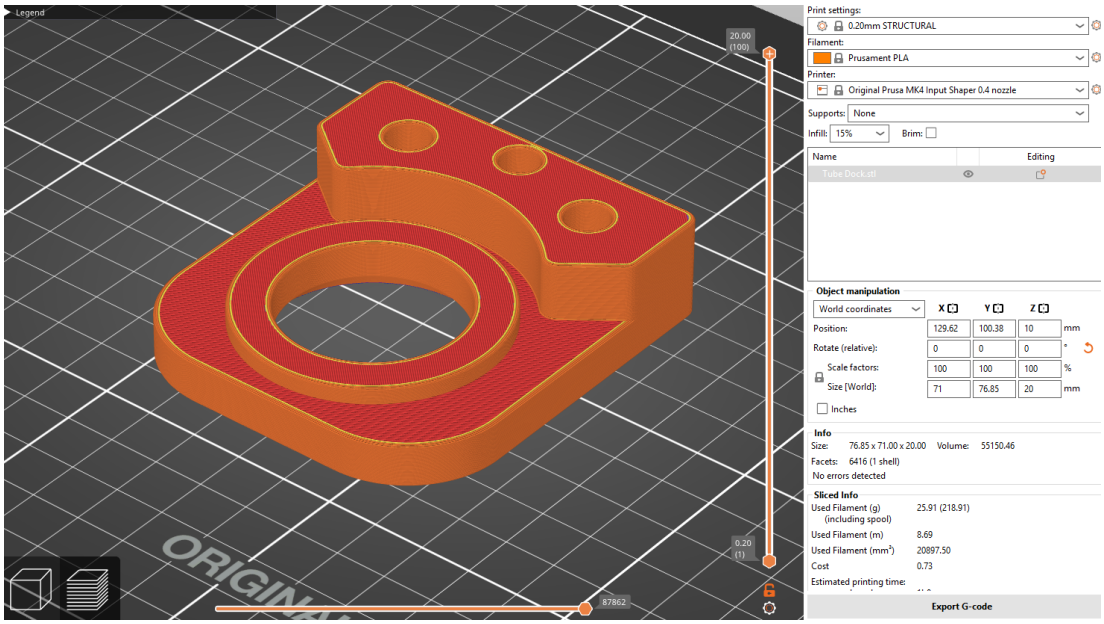

Figure 3.9: **Interface piece converted to GCode in Prusaslicer**

determined height and generating a sequence of tool paths, known as GCode. GCode is a standard communication format for toolhead-based motion systems, such as CNC machines, laser cutters, and 3D printers. The slicer determines how the printer will build the object by defining perimeters, infill patterns, and support structures. Modern slicers offer over 200 settings to fine-tune print behavior based on material properties. Pre-configured profiles are available to simplify the process, enabling users to create complex geometries such as curved holes, internal flexures, print-in-place hinges, and single-piece assemblies that would be difficult or costly to manufacture using traditional subtractive techniques. The adapter piece can be seen in Fig. 3.9 where it has been broken down into a series of tool paths.

Fused Filament Fabrication (FFF) 3D printers construct objects by depositing layers of molten plastic sequentially. The plastic filament is fed through an extruder system that grips and advances it into a heater block, referred to as the "hot end." The hot end raises the plastic's temperature just above its glass transition point, allowing it to flow smoothly through the nozzle—typically around 220°C for polylactic acid (PLA). As the molten plastic is extruded, the nozzle geometry ensures compression into the layer below while creating a smooth top surface for subsequent layers. To maintain

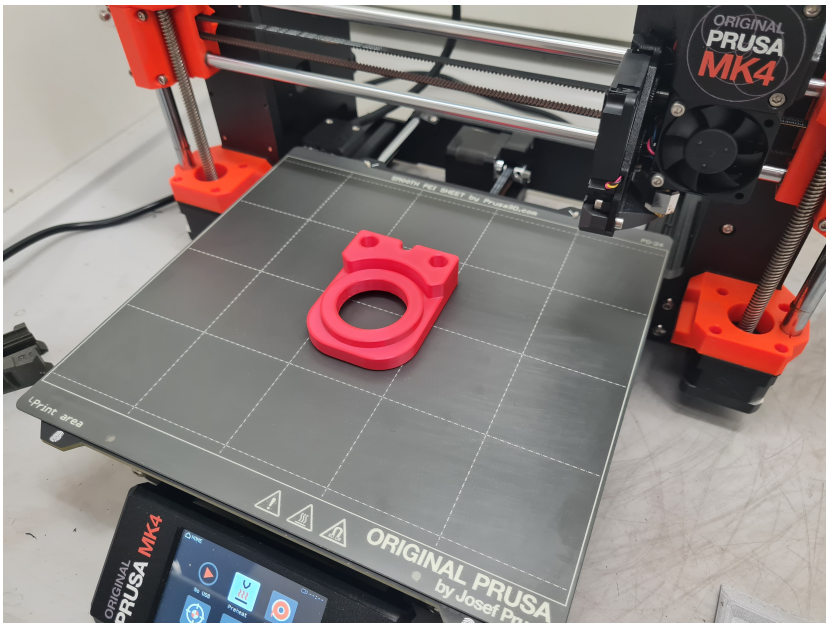

Figure 3.10: **Interface Piece printed on Prusa MK4 3D printer**

precision, an auxiliary fan rapidly cools the plastic, solidifying it before the next layer is applied. The printer follows a sequence of GCode commands created by the slicer to control the nozzle's movement relative to the print surface, enabling the creation of a 3D object. The adapter part can be seen on the print bed of Fig. 3.10.

3.9 Early Prototype

The combination of low cost electronics, 3D printing technologies along with an initial investment of equipment from ThorLabs enabled the iterative development of this system over the course of this project. This was particularly useful during the two year period of the Covid-19 pandemic, when the majority of the development took place. This enable the majority of the system to be developed in the home lab, as consumer 3D printers had become both affordable and reliable by that time and many electronic suppliers where still shipping products. An early version of the setup can be seen in Fig. 3.11

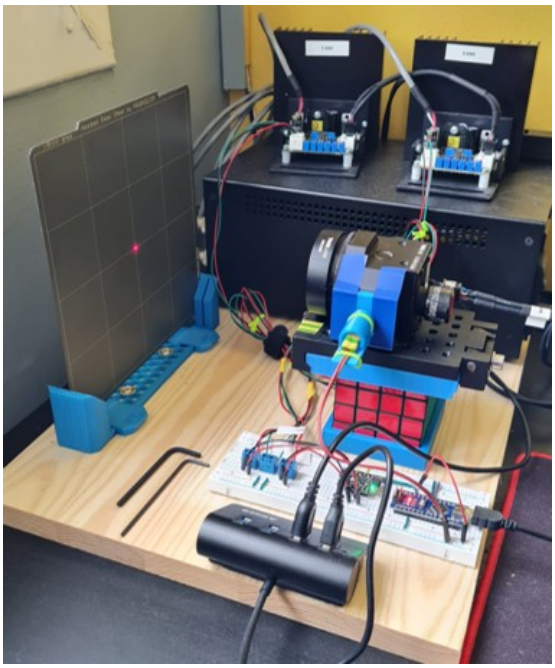

Figure 3.11: **Early test bench setup.** Laser source is a deconstructed red diode laser pen. Galvo system is mounted on a 4x4x4 Rubiks cube, which enable coarse rotation to target in 1-axis. Arduino circuit with quad channel DAC can be seen below. Alignment target is a build plate from a Prusa Mini+ 3D printer.

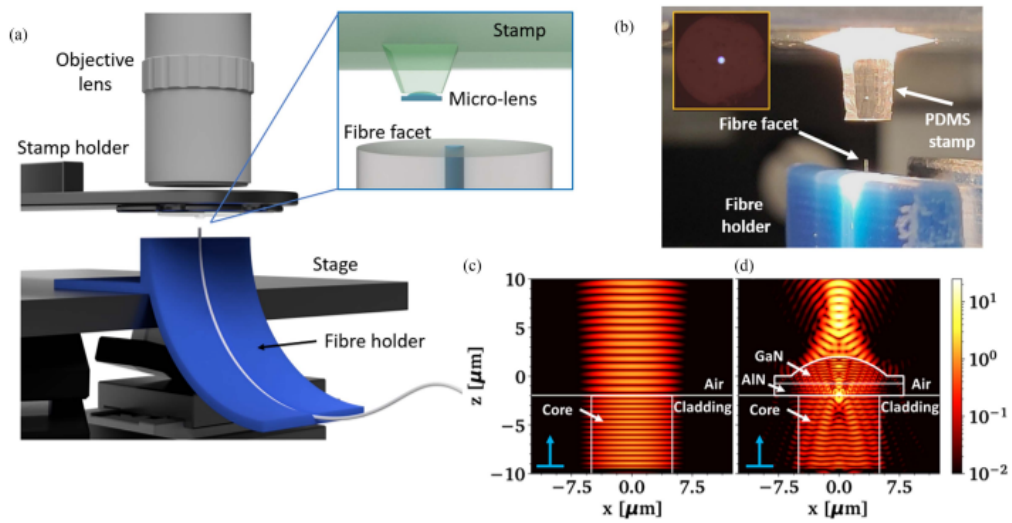

Figure 3.12: **Transfer Print Setup for Fibre Printing.** (a) Schematic view of the setup. (b) Photograph of system during print integration. (c-d) Lumerical simulations of light emission from fibre, before and after integration of GaN lens.

3.10 Micro Lens Printing

To highlight the capabilities of this injection system, a demonstrator experiment was developed in which a GaN μ-lens would be transfer printed onto the end of a single-mode optical fibre. The fibre would then simulate the alignment of membrane devices to both an "emitter" and a "detector" device for comparison. In both cases, the alignment is to a substrate where no markers are present, and the core of the fibre is not visible in the setup due to the low refractive index contrast between the core and the cladding layers [102].

A 3D printed jig was fabricated to mount the fibre at the appropriate height in the TP system whilst maintaining a safe bend radius in the fibre. A schematic representation of the fibre mounting system within the transfer printing tool is provided in Fig. 3.12 (a), along with a close up photograph in Fig. 3.12 (b). For the emitter scenario, the opposing end of the fibre can simply be connected to a light source to illuminate the core, as can be seen in the inset of Fig. 3.12 (b) and provides a reference feature in which the lens can be aligned to. As the core could remain illuminated during the whole print process, the alignment could be verified both during and immediately

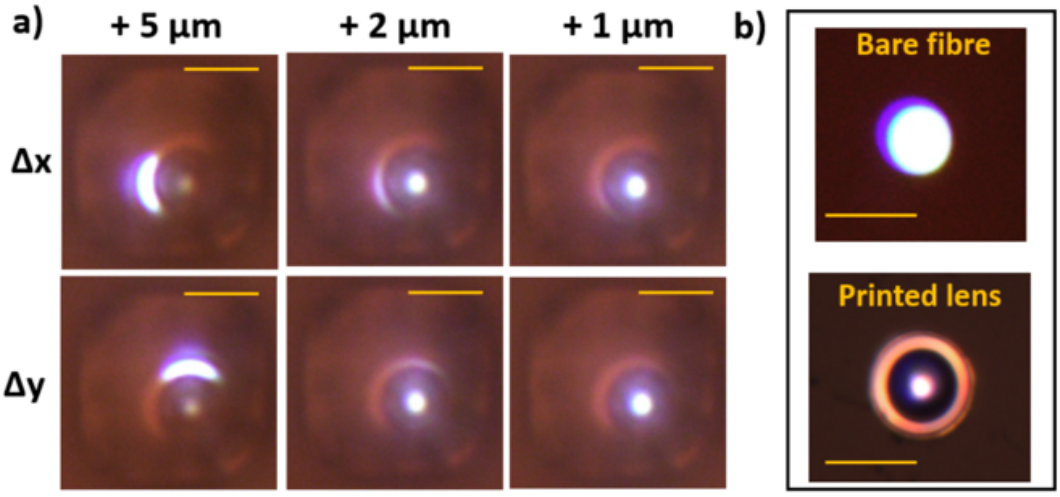

Figure 3.13: **Alignment of GaN μ-lens to white light illuminated fibre facet.** (a) μ-lens fixed in position and suspended on transfer stamp, with various stage offsets in X and Y shown to show contrast between aligned and misaligned lens. (b) Microscope image of fibre facet emission before (top) and after (bottom) printing of μ-lens membrane. All scale bars represent 15 μm.

following the print process as seen in Fig. 3.13 where good alignment to the fibre core was achieved.

In Fig. 3.13 (a) The effect of translating the μ-lens away from the centre of the core can be seen. For lower offsets, an change in spot intensity is visible during the alignment process. For larger offsets, an additional change in the beam spot shape is measurable. Fig. 3.13 (b) was taken that the same focal position, showing the effect of the μ-lens altering the emission of the fibre facet.

To demonstrate the use case of aligning to a detector device, the white light source was disconnected from the opposing fibre end and instead replaced with a visible wavelength photodetector, this allows the fibre core position to be determined by injecting light through the transmission setup and inferring that the highest measured power corresponds to the best alignment to the fibre core. As this detected position can be sensitive to the relative injection angle of the red SLED, a calibration process was carried out before the printing stage.

The floating mount of the injection system allows for minor adjustments to the mounting angle via two XY linear stages mounted to the TP2 frame. This, in conjunc-

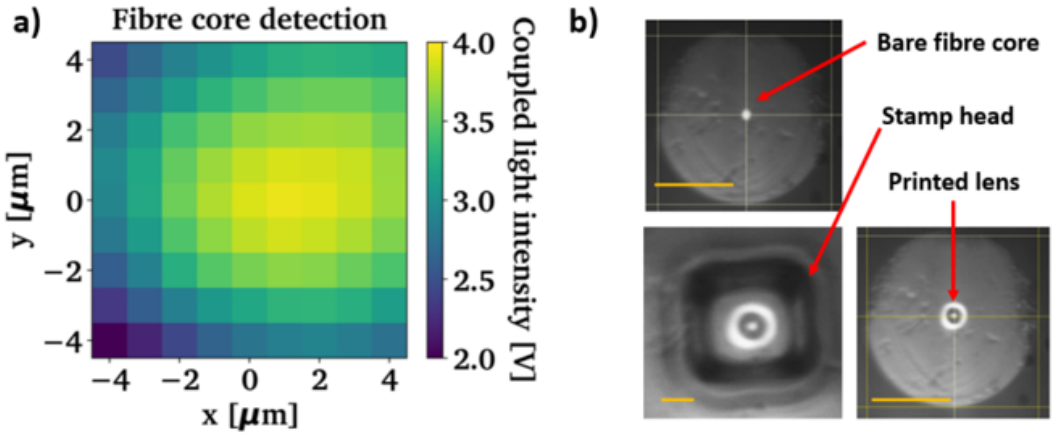

Figure 3.14: **μ-lens aligned to detector device.** (a) Map of measured voltage from Si photodetector via injected light. (b) Camera view on TP2 of showing stages of the transfer print process.

tion with the beam steering enabled by the galvanometers, facilitates the convenient alignment of the injection source relative to a sample surface. The beam was positioned such that it aligned with the radial axis of the objective lens, minimising any aberration effects [103], and was focused onto a mirror surface. Once the spatial position was roughly achieved, the beam was defocused by translating the stage in the z-direction, causing an Airy disk pattern to form on the camera feed. When misaligned, these disks exhibited a non-uniform intensity distribution, with one side of the disk appearing larger, indicating the need for alignment. By adjusting the stages and galvo mirrors in the opposite direction of the disk deformation, the resulting pattern became more balanced. The stage could then be returned to the focus position to verify alignment with the centre of the FOV. To compensate for any tilt in the fibre facet, the stamp can be brought into contact with the surface at various points to determine the z-height at which the stamp starts to deform. This information can then be fed back to the stage controller, allowing compensation for the tilt and saving the fibre position as the pivot point for printing. The stage is capable of repeatable positioning within a 10 nm range. Meaning errors in positioning due to mechanical backlash are negligible.

By implementing a raster scanning technique, the fibre facet can be mapped out with respect to measured intensity as seen in Fig. 3.14 (a). The point of highest

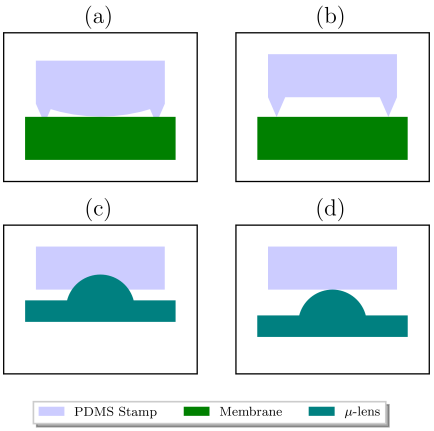

Figure 3.15: **Visualisation of reversible adhesion promoters.** (a) Flat stamp with pyramids conforming to surface of membrane. (b) Flat stamp peeled off from membrane surface due to pyramid protrusions providing a peeling force. (c) Lens structure of membrane embedded into body of flat stamp. (d) Only tip of lens in contact with stamp due to curve protruding geometry providing a peeling force against the stamp.

intensity can then be taken at the print location and marked with a virtual marker in software. The device can then be brought into alignment to the virtual marker and transferred in an aligned position. In this instance a raster scan process of $1\,\mu m$ steps was used over an $8 \times 8\,\mu m$ area with the peak intensity measured at (1, 0). The centre of this area was determined by estimation from the boundary of the cladding region, indicating that the fibre core and cladding layer are not collinear at the surface of the facet. This detection method allowed for printing accuracy equivalent to the emitter case $\pm 0.5 \mu m$, with the step size of the raster scan being the main source of error.

3.10.1 Reversible Adhesion

As the fibre was constructed from silica, the adhesion force between the back surface of the lens and the fibre facet was low enough to allow reprinting of the lens cavity. Typically, this would lead to a situation where the membrane device would be difficult to release accurately, as the adhesion between the stamp and the membrane would be stronger than that between the membrane and the substrate. However, the geometry of the lens structure helps mitigate this issue, allowing for effective release and reprinting

without compromising the integrity of the membrane device.

In prior works, the inclusion of protruding structures on the stamp allowed for a larger difference in adhesive forces during the pick-up and release stages of transfer printing [42]. These protrusions create a larger contact area between the stamp and the membrane during the fast retraction stage, due to their deformable structures, as shown in Fig. 3.15 (a). When idle, the protrusions relax, providing a "peeling" force at the base of the stamp, leaving only the tips of the protrusions in contact with the membrane. This results in a significant reduction in contact area, making transfer onto the substrate easier, as seen in Fig. 3.15 (b).

A similar effect is achieved with the μ-lens structure. A flat stamp is able to conform to the dome of the lens, increasing the contact area during pick-up, as shown in Fig. 3.15 (c), causing the lens to become embedded in the stamp. When idle, the internal stresses of the stamp eject the lens structure until an equilibrium point is reached, where elastic forces balance the adhesion of the stamp. This results in a low contact area, as seen in Fig. 3.15 (d).

3.11 Application Demonstrators

The vertical injection setup developed in this chapter was designed with the intention of developing a multi-purpose system. Throughout its development, several use cases emerged that highlight the potential future applications of the system, which are summarised in this section as proofs of concepts. A more detailed and in-depth exploration of an additional use case can be found in Chapter 4, while the examples presented here serve more as viability studies for further development. Included in this are In-situ detection of changes in coupling conditions, fully vertical injection of light into PICs, sample height detection via a soft contact method and traditional optical coupling to grating structures.

3.11.1 In-situ print detection of buckled Si membrane on SiN, via grating couplers.

The original concept for this system was to provide an alternative to fiducial markers for high-accuracy printing. When transfer printing a photonic component on-chip, the goal is often to spatially align the two devices within a given tolerance [65]. While the precise location for printing can be determined through theory and simulations, these often make assumptions regarding the presence of defects, sidewall roughness, etc., which can affect the coupling characteristics between the receiving substrate and the transferred device. This can lead to issues where even the most accurately placed component performs below specifications due to fabrication noise, which is challenging to measure beforehand. If the device's performance could be measured during the printing process rather than after, it might be possible to increase the yield of high-performance devices within a single print session by optimising the print position based on the target device characteristics.

The initial technical challenge for this work was to determine whether the vertical injection setup could be actively used during the printing process, where the injected beam propagates through the stamp during the measurement phase. Despite PDMS being transparent in the visible range [104–107] , it can still act as a diffractive element when placed in-line with the microscope system. This diffractive effect could hinder the beam quality when injecting light into a photonic system, as well as diffuse any reflected signal intended for measurement, making it challenging to achieve reliable outcomes.

A proof of concept demonstration was developed, in which a silicon membrane device was printed on top of a waveguide SiN structure with grating couplers terminating both ends. The injection system would couple a red SLED source into the first coupler, and the microscope's camera would monitor the intensity of the output coupler. The membrane would be printed directly on top of the waveguide, as seen in Fig. 3.17, to act as a source of optical loss. This setup would allow a basic "on" and "off" signal to be detected during the recording of the printing process. The membrane device used was a legacy silicon membrane device with 400 nm of silica deposited on top after the device was under-etched, causing the membrane to adopt a convex geometry as seen

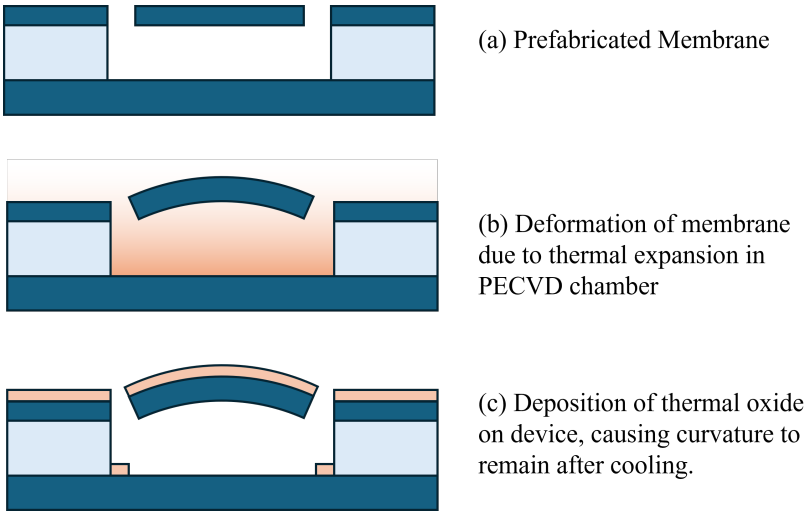

Figure 3.16: **Fabrication of Buckled Membrane device.** Step by step process of how silicon on insulator membrane device was fabricated to created a buckled membrane. Dark blue represents silicon, light blue represents silica and orange represents thermally deposited oxide.

in Figure 3.16. This allowed the membrane to be depressed onto the surface of the receiver, making full contact with the SiN waveguide, and then spring back off the surface once the stamp was retracted. This created a "button-like" effect, where pressing the membrane would switch off the output grating coupler.

As seen in Fig. 3.17, when the membrane is depressed onto the surface of the waveguide, the output grating coupler decreases in brightness towards an off-state. When pressure is removed from the membrane, it returns to its convex shape, creating an air gap around the waveguide that allows the injected mode to propagate again, switching the output grating back to an on-state. This experiment is repeated across four combinations of two variables. First, the membrane is placed either on top of the guide or on a featureless area. Second, a detection window is used on the output coupler or on a featureless area away from the output, with the window area remaining fixed for all measurements. This setup allows for the monitoring of potential changes to the measured intensity that are not directly related to the loss induced by the membrane.

Changes in measured brightness during the print cycle can be observed in all combinations tested. However, for the "on guide on grating" variation, there is an order of magnitude difference in the relative change in output brightness, confirming that the

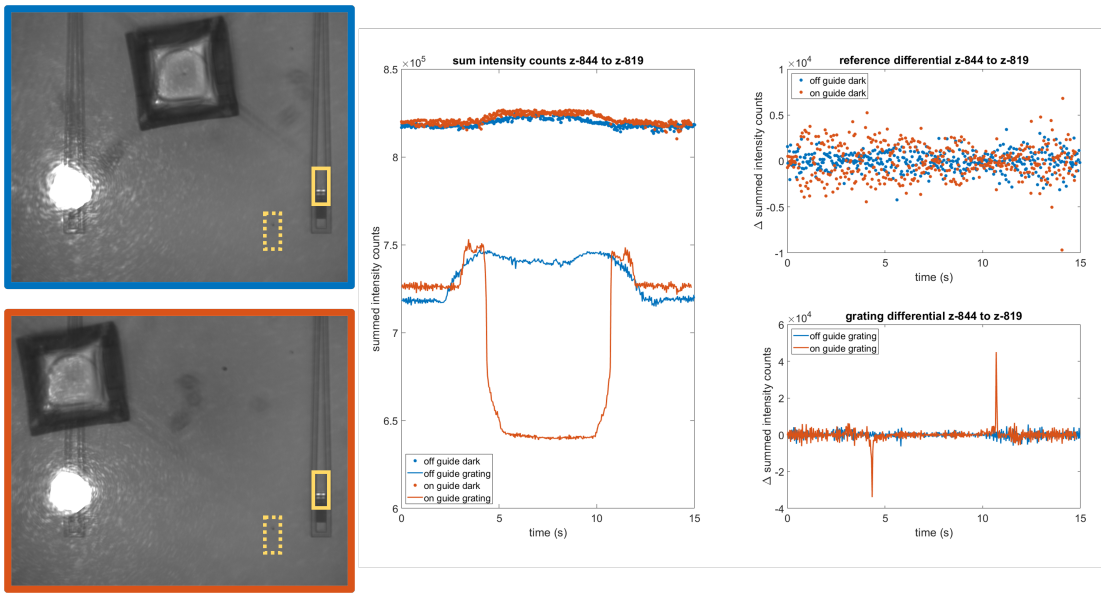

Figure 3.17: Buckled Si membrane devices were printed onto a u-bend SiN waveguide terminated with grating couplers. Two spatial windows were monitored, highlighted in yellow, one on the grating output and the other in a reference dark area, referred to as grating and dark respectively. The summed intensity of these windows were monitored for two 15 second print events, where the buckled membrane was fully depressed to be flat with the SiN surface. An off-guide measurement was taken as a reference (shown as blue) to show general effect cause by depression of the stamp. Then a membrane was printed onto the waveguide (shown as orange). When the bulk Si of the membrane came into contact with the waveguide, as detectable drop in output intensity was observed and could be detected as a triggered event using a basic differential analysis.

optical loss induced by printing the silicon membrane was detectable. This validates the initial steps needed for more advanced in-situ measurements, such as the ability to couple into photonic structures for through-stamp testing. The next technical challenge to overcome would be integrating the ability to obtain optical spectra during measurement, allowing alignment to be optimised by measuring parameters like the Q-factor.

3.11.2 Vertical injection through mirror couplers

Vertical coupling mechanisms for photonic integrated circuit (PIC) devices are predominantly based on grating couplers [108] due to their fabrication simplicity and tunable wavelength operation [109]. However, a major drawback of these structures is that they

emit and receive light at an angle θ relative to the surface normal of the chip. This limitation restricts their use in more complex multilayer systems, where they could serve as optical interconnects, and reduces the efficiency of vertical injection setups.

Alternative methods capable of true vertical emission are currently being developed, including nano-3D printed couplers [110] and etched structures [111] that exploit the geometry of the semiconductor crystal lattice. However, these approaches introduce additional challenges, such as the need for expensive fabrication equipment and material-specific constraints. As part of this work, a technique was developed to fabricate vertically emitting polymer structures using standard cleanroom equipment.

In parallel, my colleague Ross Cassells developed a method for fabricating polymer waveguide mirrors on glass. This technique employs grayscale patterning to create smooth, angled surfaces in SU-8 photoresist. Once the dosage steps are calibrated, it can reliably produce 45-degree surfaces at the ends of waveguides [112]. These surfaces can then be coated with metal to enhance their reflectivity, enabling true vertical light injection and emission on-chip. Device testing has demonstrated the broadband capability of these structures [96], showcasing their potential for a wide range of applications across different material platforms.

These coupling structures are particularly well-suited for the vertical injection setup, as they enable efficient coupling into waveguiding structures, as seen in Fig. 3.18, while minimizing the scattering losses typically associated with grating structures when injecting light parallel to the surface normal of the photonic chip [113]. As a result, these structures open up new possibilities for innovative integration schemes in conjunction with vertical injection setups.

Currently, the system has been used solely for validating fabrication process flows. To advance this work, the key technical challenge lies in developing a unique integration method that leverages the advantages of these systems. For instance, since fabricating these couplers does not require an etching process, they could be seamlessly integrated onto suspended membrane structures without significantly affecting device quality factors. Additionally, SU-8 can serve as a mode converter for high-index materials [114], suggesting the possibility of fabricating a mirror-coupler mode-converter structure di-

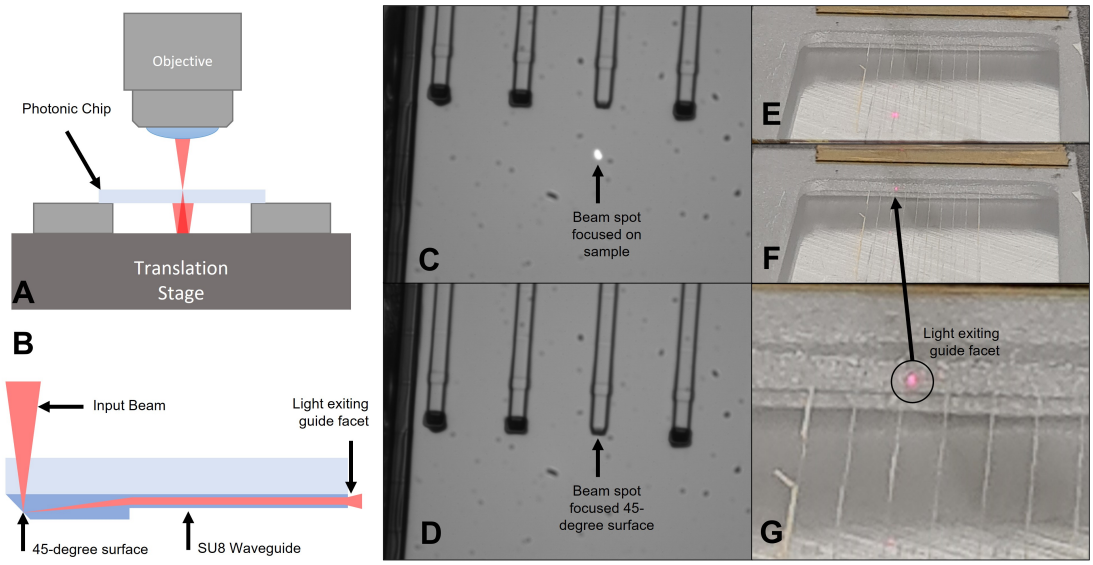

Figure 3.18: 633nm light source coupling to SU8 polymer waveguides via greyscale patterned waveguides. (a-b) Schematic view of setup, transparent photonic chip is suspended such that the light focuses through the glass substrate onto the patterned mirror surface. (c) microscope view of beam spot misaligned from mirror coupler input port. (d) beam spot focused on mirror coupler disappears due to all light being reflected into waveguide. (e) external view of light misaligned from coupler. (f-g) external view of light aligned to coupler, light scatters out from the waveguide end facet.

rectly onto a waveguiding membrane. This could enable active spectral measurements during the device printing process, facilitating real-time optimisation of alignment and device performance.

3.11.3 Stamp height detection, via PDMS pyramid

For transfer printing, and in-fact, all CNC-like systems, spatial referencing is critical to enable active alignment and automated processes [64,115]. As transfer printers view PICs from a top-down perspective, machine vision techniques can be used to detect lateral features across the chip [116,117]. This allows for alignment of the X, Y linear and Zθ rotational axes using industry-standard techniques. To measure the z-height of devices loaded on the transfer printer, typically a touch-off technique is used with the stamp head. The stamp is brought slowly into contact with the PIC surface, then when a visual distortion in the image is observed it is assumed that the stamp has

deformed slightly due to compression against the PIC surface, the height this occurs is then recorded as the z-height of the PIC. This process is only accurate to sub-micron precision as it dependant on many factors, such as PDMS thickness and mixing ratio as well as the reflectivity of the PIC surface. The method also relies on a well illuminated FOV to be able to detect the subtle distortion of the image which leaves a level of ambiguity to detect when the stamp is in contact. A better method would allow a change in signal, which is "on" when in contact and "off" otherwise.

A method to achieve this is to leverage the vertical injection system and an advanced stamp design already used to promote reversible adhesion [42]. Pyramid teeth can be included on the surface of the PDMS stamp by utilising KOH wet etching processes on the silicon mould, this etch process exposes the crystalline planes of the silicon wafer that result in a pyramidal structure with an apex angle of 51.7° [111]. The angle of these facets prevent light from from reflecting back through the microscope, and instead cause them to be lost to scattering. This functions as the "off" condition for when the stamp is no longer in contact with the PIC surface, when the tip of the pyramid comes into contact with the surface of the PIC it then deforms to a flat surface as seen in Fig. 3.19 and in turn acts as a mirrored surface allowing light to be transmitted back through the microscope. This results in an "on" condition for when the stamp comes into contact with the PIC.

From initial testing this method is accurate to at least 100 nm, however more in-depth analysis is needed, this is due to the more efficient use of the camera's dynamic range. With the touch-off method fluctuations in intensity between contact and no contact could be estimated to be lower than 30% of the sensors dynamic range, whereas for this technique, as the geometry of the stamp head prevents any back reflection, a beam intensity can be used that would normally push the camera sensor well above saturation. When the apex of the pyramid is deformed to a flat with area < pixel area, a fully saturated spot will be detected.

The next technical challenge for this work is to integrate the machine vision process required to detect the on/off illumination of the stamp pyramids, which would enable automatic height mapping of PIC surface from within the transfer printer, advanced

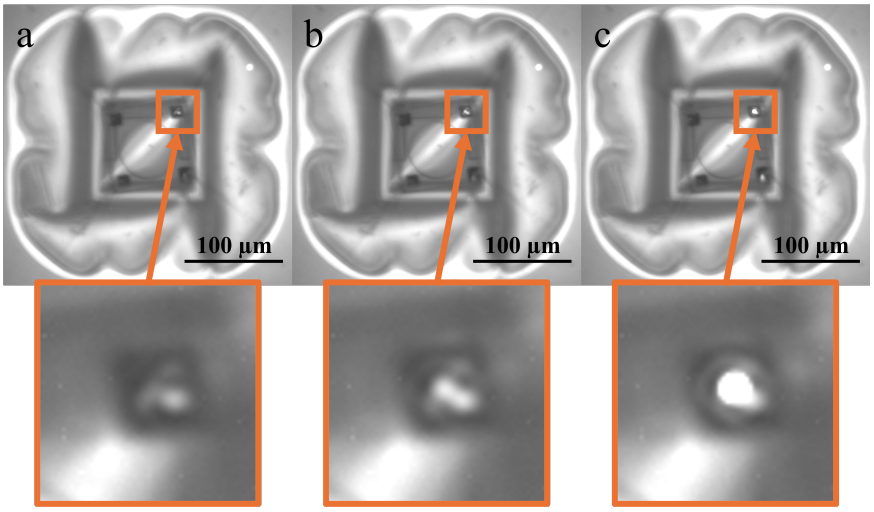

Figure 3.19: In-situ detection of stamp contact. (a) laser is focussed on pyramid head of PDMS stamp, only a small portion of light is reflected back to the camera due to the pyramid geometry. (b) stamp comes into initial contact with the device below, causing the tip of the stamp to flatten and increasing the light reflected back to the camera. (c) stamp is lowered a further 500nm and shows a significant increase in reflected light due to a large flat area of the forming at the beam focus position.

integration into non-planar substrates and in-situ curing processes. The ability of the PDMS pyramids to scatter light when incident on the facets opens up opportunities for unique coupling integrated into transfer print stamp heads similar the mirror coupler discussed earlier.

3.11.4 Off-axis monitoring via grating couplers

Grating couplers are an industry-standard method of coupling light onto a chip [108], so although alternatives are being developed that can offer better performance for certain applications [118], it is unlikely that grating couplers will be fully replaced by an alternate technology. This is due to their simplicity in fabrication and the continued research into their optimisation [119]. As this is the case, compatibility for non-vertical monitoring was added to the transfer print setup.

The easiest method to achieve this would be the inclusion of an off-axis detector or camera that is configurable and aligned to the grating coupler output angle, while still providing clearance for the stamp holder required for the printing process. Despite

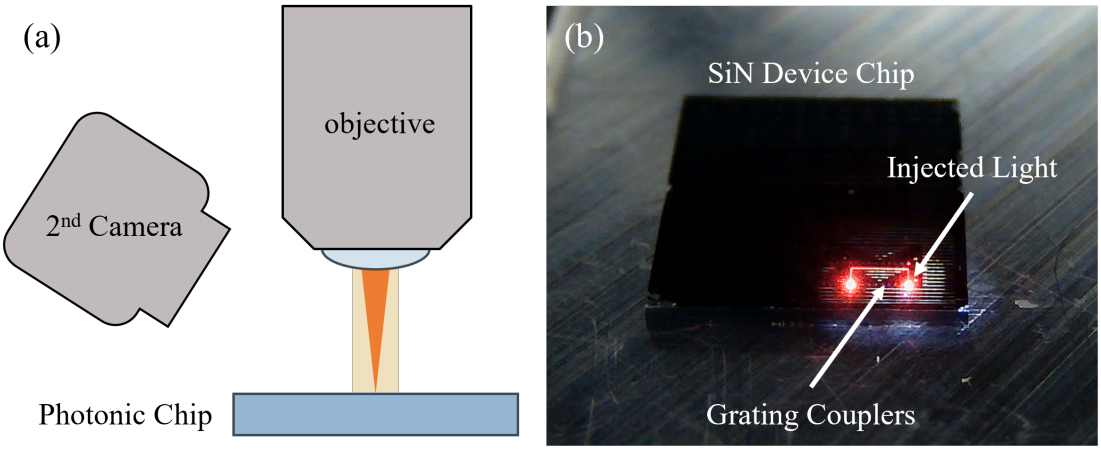

Figure 3.20: (a) Schematic view of secondary camera setup for off-axis monitoring of grating coupler devices. (b) Demonstration of on-chip coupling to SiN device, waveguides optimised for 1550 nm operation causes visible scattering when injecting 632 nm.

being designed to operate at a specific angle, grating couplers present a slowly varying envelope with emission angle. The efficiency of the coupling gradually drops off as the coupling angle increases in deviation from the designed angle. Since the transfer printer is intended to aid in the integration of heterogenous materials on-chip, a reduction in coupling efficiency can be tolerated, as it is not intended to be the final packaging of the PIC. This would allow the vertical injection setup from this chapter to still be used, provided the light source is powerful enough to compensate for the losses. A conceptual version of this setup was tested, demonstrating the feasibility of this approach.

As seen in figure Fig. 3.20 a secondary camera was setup at an angle matching a SiN chip with grating coupler devices. The gratings were designed for 1550 nm operation with a grating input/output angle of $\approx$ 20°. For ease of testing 632 nm source was used for visibility, which lead to multimode operation of the waveguides producing the scattering losses that highlight the geometry of the guide in Fig. 3.20 (b). Two large spots can be seen at the end of the guide structures, the rightmost corresponds to the scattering losses caused by injecting light vertically into the chip. The left corresponds to the output coupler that contains only light that has propagated through the guide.

This serves as a minimal proof of concept that an off-axis system could be included as a module for the transfer printer. The next technical challenge to overcome is running

this system in-tandem with a printing process. The first half of this is a mechanical challenge as the design of the PIC and mounting setup for the stamp could limit the clearance needed to align the module. The second is the inclusion of a method to obtain spectral information during the printing process, the main applications of this type of module would be to enable target coupling criteria of passive resonator structures. For this reason, being able to measure device spectra in-situ is required.

3.12 Conclusion

This work has demonstrated the development and implementation of an advanced transfer printing system tailored for precise heterogenous integration of photonic devices. By leveraging a custom-built six-axis translation stage, a modular optical setup, and an innovative vertical injection system, we have achieved high-precision alignment and transfer capabilities. The incorporation of machine vision, targeted illumination strategies, and adaptive control systems has enabled reliable device placement, even in challenging out-of-plane configurations.

The integration of 3D printing for rapid prototyping and the use of low-cost electronics further enhanced the flexibility and accessibility of the system, allowing for iterative improvements throughout the project. A key demonstration of the system's capabilities was the successful alignment and transfer printing of GaN micro-lenses onto optical fiber facets, showcasing the potential for advanced photonic device fabrication with sub-micron accuracy.

Beyond the specific applications explored in this work, the methodologies developed here offer broader implications for the field of transfer printing, particularly in areas requiring precise optical alignment and integration. Future efforts could focus on refining the automation processes, expanding the range of compatible substrates, and exploring novel materials to further improve transfer reliability and efficiency.

Ultimately, this research contributes to the advancement of scalable and high-precision transfer printing technologies, paving the way for new possibilities in integrated photonics and μ-fabrication.

Chapter 4

Python Package for Rapid Prototyping of Transfer Printable Coupons

4.1 Introduction

Transfer printing is a heterogenous assembly technique that is growing in popularity within the scientific community [120], with many factors playing a role in its adoption. Firstly, transfer printing fundamentally allows access to functions not natively accessible on single material chips, allowing construction of integrated systems with best in class performance. [121–123]. Secondly, due to its relative youth compared to other heterogenous techniques such as flip-chip integration [124] and wafer-scale heterogeneous integration [125], there are many publications where the novelty of research lies in being the first demonstration of material X on material Y [126], which can be achieved with even rudimentary setups, as discussed in the previous chapter. Thirdly, due to the underlying similarity to large-scale pick-and-place systems such as those seen in printed circuit board (PCB) foundries, it is easy to extrapolate the value proposition of a transfer print system for photonic integrated circuits (PICs) to industry. As such, we can see growing interest in adoption of transfer printing within companies like

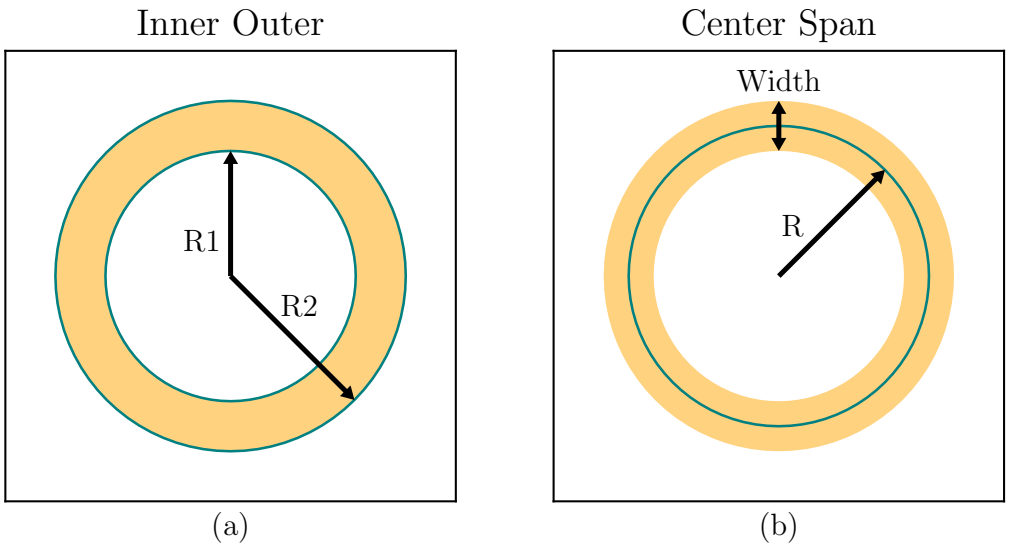

Figure 4.1: **Ring Resonator parametrised two ways.** (a) inner radius and outer radius. (b) waveguide width and effective radius.

X-Celliprint [127] who are pushing to develop commercial systems.

To achieve this goal, transfer printing needs to mature as a whole. Not only the machine itself but the tools around it that support its use. A printable membrane device can be thought of as the overlap between integrated photonics and micro-electromechanical systems (MEMS) [128]. Currently the focus has been on the development of the former optical performance. This is because heterogenous integration is well placed to tackle the challenges faced by monolithic platforms [129] and once the device is printed the mechanical features that maintain the device's suspension on the donor are intentionally broken. As such they serve no role post-integration. Because the optimisation of the support anchors are often overlooked, the capability of the technique is restricted as the pick-up and release characteristics of each batch of devices is inconsistent. This keeps the device yield low and the skill level of the integration process high. This can be in-part due to the immaturity of the tools available for the design of such structures, placing comprehensive studies of mechanical performance outside the overlap of the Venn diagram of difficult to achieve and novel to publish. We can start to shift this position by developing tools that lower this difficulty threshold and build on the knowledge obtained thus far in the field, starting with the design tools.

As lithographic techniques improve and evolve, so do the graphic design system (GDS) editors that support them. Rudimentary pattern generators have developed into sophisticated systems with integrated design rule checks, layout and schematic comparisons and even in-built simulation capabilities. A trivial example of this development would be to look at a ring resonator where the outer and inner perimeter define the physical structure of the device, within modern design tools this structure is contextualised to use the parameters of waveguide width and effective radius of the propagating mode. Despite being the same structure, the route to producing it has changed to conform to the theory of device itself. A more comprehensive example of this is the part development kits provided by PIC foundries, where a platform of components have been developed in-house and provided to the customer fully parametrised and tailored to their material platform. The former provides the building blocks to the latter. As the focus has been on the optical elements, no such PDK or design tool has been developed (at time of writing) that focuses on the generation of micro transfer printable structures.

In this chapter, a custom built GDS design tool for suspended membrane structures will be presented. Arguments for development choices will be provided where relevant, such as why the reasons for choosing Python as the back end for the package. The composition of a suspended membrane structure will be broken into a component level basis with the most interesting highlighted for extended discussion later. The design process will be established to provide the reader with the background required to understand the intricacy of certain processes and the implementation of certain solutions within the design package. Design metrics produced within this tool and their application to a more mature design process will also be discussed.

4.1.1 Why use Python?

The Python programming language has seen mass adoption across nearly every technical field, becoming one of the most popular and widely used programming languages since its creation by Guido van Rossum in 1991 [130] as a project for his Christmas holiday. His intention was to make an open-source, general purpose code interpreter that built upon his experience working with the ABC programming language. This project was received well and quickly became the 2^{nd} most popular coding language in industry. The first being JavaScript which is responsible for the majority of website architecture today. There are many reasons for this popularity, but the ones that translate well into a academic research setting are:

Legibility: Python is a high-level language, meaning that complex aspects of programming, such as memory management, are handled automatically by the interpreter instead of by the user. This lowers the verbosity of python scripts by removing these background processes, allowing users to focus just on the task at hand. The coding syntax that remains was also chosen to feel familiar to written English by curation of key words and relying heavily on indentation rather than brackets for code blocking. In academic settings this is invaluable, as it provides a lower barrier to entry for new researchers and allows the act of writing code to "get out of the way" of coding.

Versatility: Python was developed as a general purpose language, meaning it has applications in many fields from data analysis to scientific computing to system automation. This is built upon by the vast amount of high quality open source libraries that enable new functionality and features. This is incredibly valuable in an academic setting as their is often a element of time pressure in any given project. As python is so versatile, it allows nearly any task to be done within its ecosystem. This allows users to save valuable research time by learning only one programming language instead of several to achieve the same task.

Development Speed: Python was built to have a short development time from idea conception to implementable solution, sacrificing computational speed in some applications for this trade off. This makes it great for rapid prototyping workflows, allowing it to quickly adapt to on the fly modifications to optical setups, data formats

or device designs often seen in research. Certain key processes can be passed off to computationally faster languages [131] to mitigate issues with runtime speed where applicable and is a common feature of popular libraries.

Because of the above benefits and more [132], various GDS design tools such as GDShelpers, GDSfactory, and Nazca have been developed within the Python ecosystem [77,77,79]. Each library offers an extensive collection of photonic components and tools for under-etching device geometries. However, none (at the time of writing) include tools tailored to the design of μ-transfer printable membrane structures. This means users need to develop custom solutions leading to a lack of standards across the transfer printing field.

Most of these libraries are built upon a well-established and popular geometry library called Shapely [133], which provides a comprehensive toolkit for geometric design and manipulation with tools for construction, set operations, geometric transforms and more. Shapely has been taken as the foundation for these packages, with the contextualisation to PIC design built on top to allow features such as GDS cell construction and waveguide routing. By building the membrane design package on this same foundation, it not only follows a clearly laid path, but it ensures compatibility with these tools and their continued development.

4.1.2 What Should It Do?

Optimising a design for transfer printing requires an iterative approach as there are many interlinked parameters that can result in non-successful transfer. Despite the transfer printer itself being conceptually simple in its operation, the inverse can be said for the development of transfer printable coupons. as many parameters are interlinked to one another. The dimension of the coupon informs the size and quantity of the anchors. First due to the length of material needing supported but also the contactable area for the stamp, resulting in different forces during the pickup stage. The geometry of the device determines the minimum etch time required, and thus the amount of holes required on the coupon. Several more relationships between parameters are bound to be discovered as transfer printing technology matures, particularly in regards to material

properties.

To make optimising the design straight forward typically parameter sweeps are carried out, in the context of device design a sweep is simply and array of identical designs where key parameters are varied across each entry in the array, such as the number of anchors and the size of the coupon. These designs can then be made on a small sample of the chosen material and tested for viability with a transfer print system by attempting to print each one. The best design can then be used to make large arrays of the functional device with the confidence that an optimum design has been chosen. The tool discussed in this chapter was created to facilitate this process. A typical design process would look similar to Figure 4.2. Highlighted in orange are some of the design questions that need answered when making a new membrane design, and the tool presented in this chapter is designed to facilitate answering them.

4.1.3 Suspended Membrane Structures

An already extensive range of suspended membrane devices have been demonstrated in literature [66, 76, 134, 135], and any new package for this field should look at what designs have already been tested and proven to ensure it can not only accommodate them, but make it more convenient to generate them. To achieve this, this package splits a membrane structure into several core components that can be used in a modular fashion to construct a range of complex designs from simple pieces. These components include:

- **Coupon:** The part of the membrane intended for transfer, providing the surface to adhere to for both the picking and placing processes as well as defining the overall footprint for the printed component. The desired photonic device can be embedded within the coupon in various ways to facilitate transfer.
- **Border:** The support structure surrounding the coupon. Its geometry determines the leverage available to the μ-transfer printing system for mechanical pickup, as it defines the length of the anchor geometries.
- **Anchors:** Mechanical tethers that connect the coupon to the surrounding border.

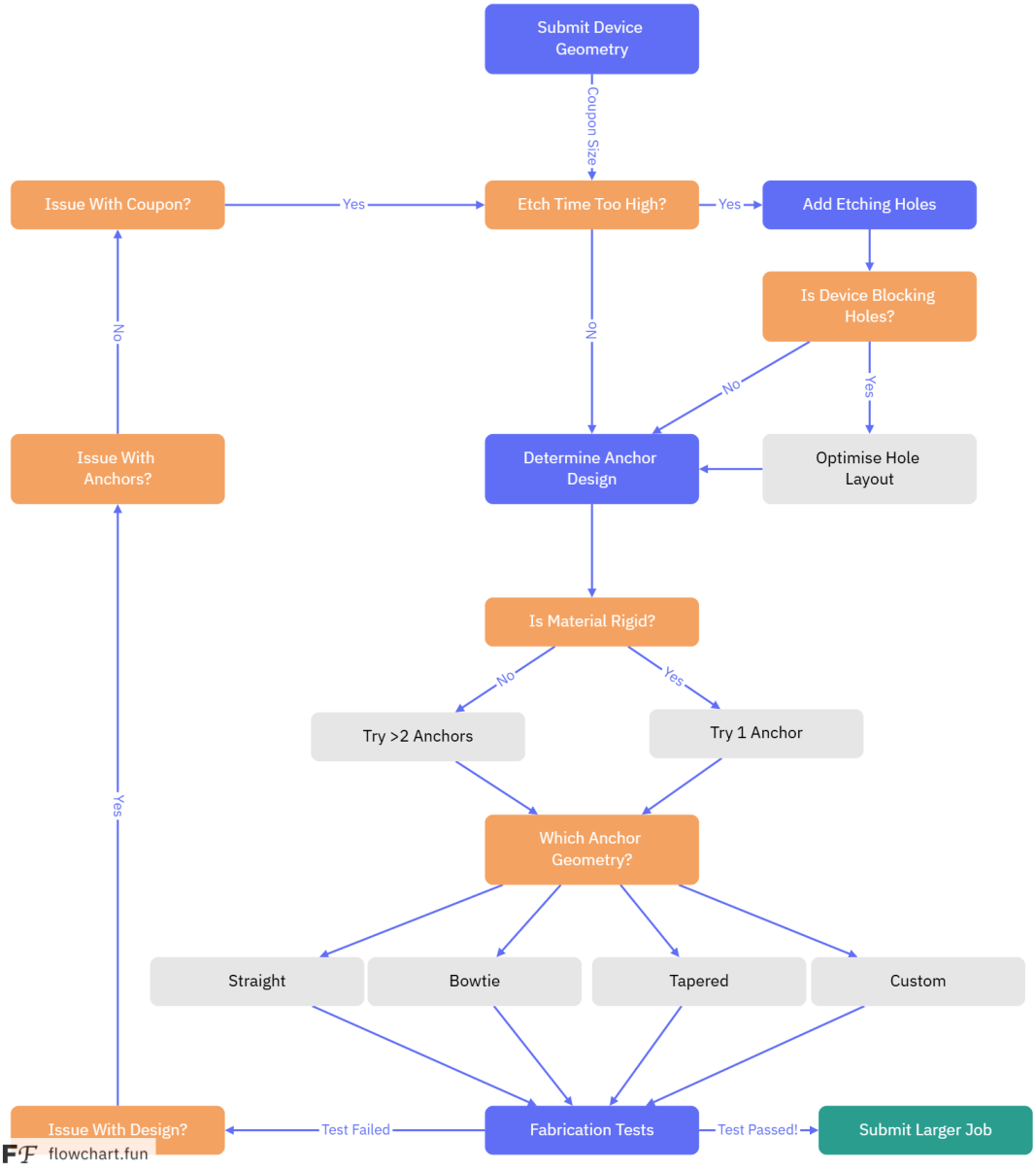

Figure 4.2: **Flowchart for basic design process of suspended membrane structures.** The tree is simplified to give an overview of the process of creating new transfer printable designs. Additional considerations also need to be given for different material types.

These sacrificial structures prevent the coupon from dispersing across the surface during the release stages but are designed to break away during the stamp pickup process.

- **Devices:** The photonic components designed into the coupon, which may be shallow-etched for waveguiding applications such as ring resonators or punched through the entire structure, as in the case of photonic crystal cavities.

- **Holes:** Features to facilitate faster under etch times and improve flatness of coupon underside. These provide additional routes for liquid etchants to flow underneath the coupon to remove the sacrificial layer more effectively.

- **Panels:** Components that allow arrays of membrane designs to be created and organised as part of a larger photomask design, facilitating common tasks such as device parameter sweeps and labelling. The former of which allows variations to be tested across one panel, such as anchor widths varying from 1 μm to 5 μm. the Latter allows text labels to be aligned with rows and columns of the panel, making identification of devices easier when printing.

Each of the core elements is highlighted in Figure Fig. 4.4 with a negative tone mask for clarity. Typically positive resist patterns will be produced where UV light will expose sections of the resist to be removed, whereas negative patterns expose the areas to remain post development process. For direct-write systems such as laser lithography tools positive resists have the benefit of limiting the minimum feature sizes possible to the resolution of the motion system. For negative resists the minimum feature size is limited by the beam size of the laser which is typically diffraction limited to $300\,nm$ whereas it is possible to achieve $\leq 100\,nm$ with many motion systems. Positive resist is also more convenient for processing as the developed mask can be stripped even after development, by solvent cleaning and matrix ashing processes [136].

Defaulting to positive tone resists also has the benefit of slightly reducing computational time. The GDS file format doesn't support polygons with holes, which the importance of will be discussed later in this chapter. So, in any instance where a hole is

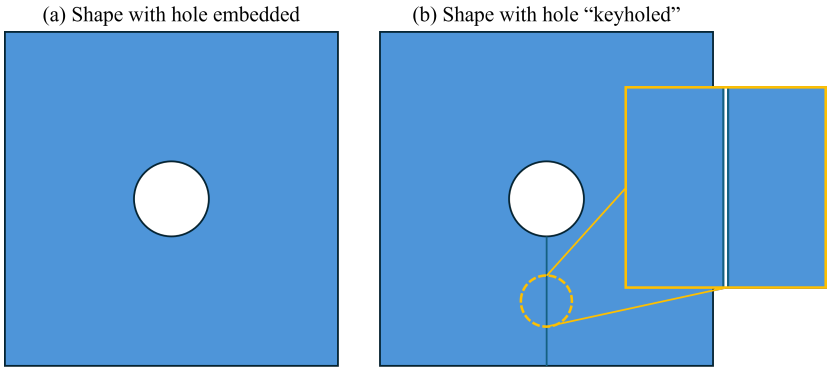

Figure 4.3: **Process of Applying a Keyhole to a Polygon.** (a) Polygon containing a hole. (b) Polygon and hole now merged to one object by subtraction of a thin rectangle.

required the polygon needs to be “key holed”. This is when two parallel lines which are separated by a distance smaller than the lithographic resolution, are added to the design that connects the exterior of the polygon to the exterior of the hole. This connects the two geometries into one to create an equivalent geometry that is GDS compatible and can be seen in Figure 4.3. This has the downside of adding four additional points per hole in each design, as well as the computational overhead required to calculate where those points should be. During the development of these tools, it was found empirically that positive resist patterns tend to have significantly less polygons containing holes than their negative counterparts.

The modular design of the membrane package allows users to focus on the components most relevant to their process at any given time. By breaking down the design into distinct, manageable parts, users can easily isolate and modify individual elements without needing to navigate the entire structure. This enables researchers to concentrate on optimising specific aspects of their design, such as the geometry of the coupon or the configuration of the anchors knowing that the rest of the structure will remain as intended.

As an example of this focused design approach, Fig. 4.5 demonstrates the flexibility of the membrane design package when only a single component is varied. Coupon designs that go beyond what is typically seen in the literature are easily achievable within this library. This is important because it is hard to predict what functionality will be

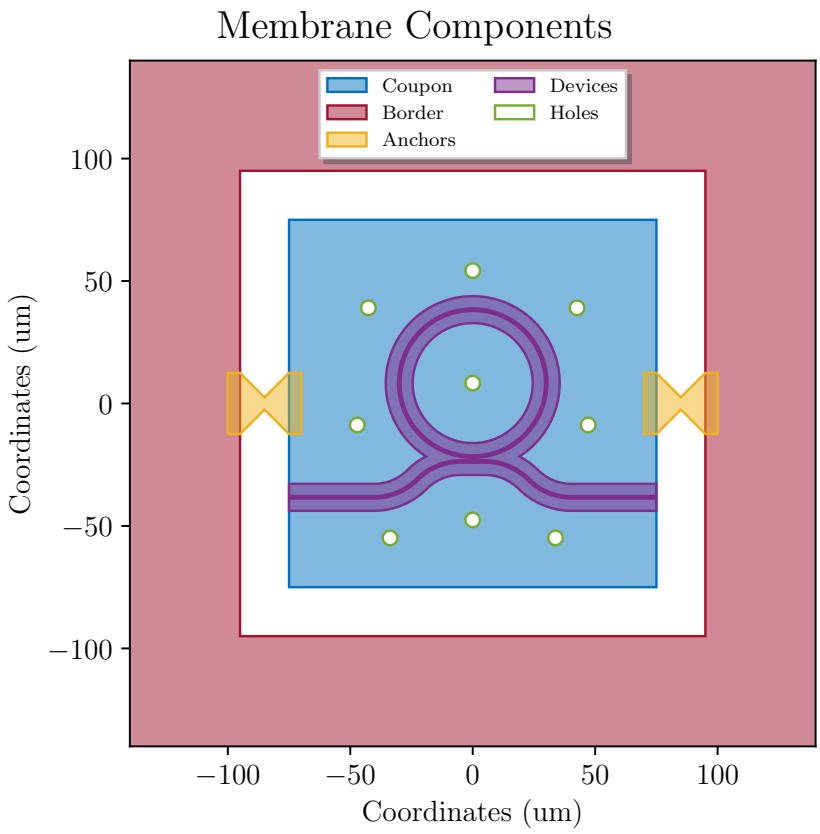

Figure 4.4: **Geometry of a shallow-etched ring resonator suspended membrane structure.** All core components can be seen highlighted within this diagram and were generated using the package described in this chapter.

needed in the future, so to avoid as many arbitrary limitations as possible code flexibility should be considered at each step. As the package matures in capability additional components can be introduced that serve different roles in the fabrication process or provide alternative implementations of the same components, entirely replacing them.

- **Irregular:** Both regular and irregular polygons can be generated using the *create_coupon*() method by specifying different values for the *side_lengths* parameter.
- **Circular:** Circular coupons can be generated by increasing the *num_sides* parameter to the desired number of vertices. This could be utilised in ring resonator geometries where it is desirable to have the waveguide edge follow the perimeter of the coupon.

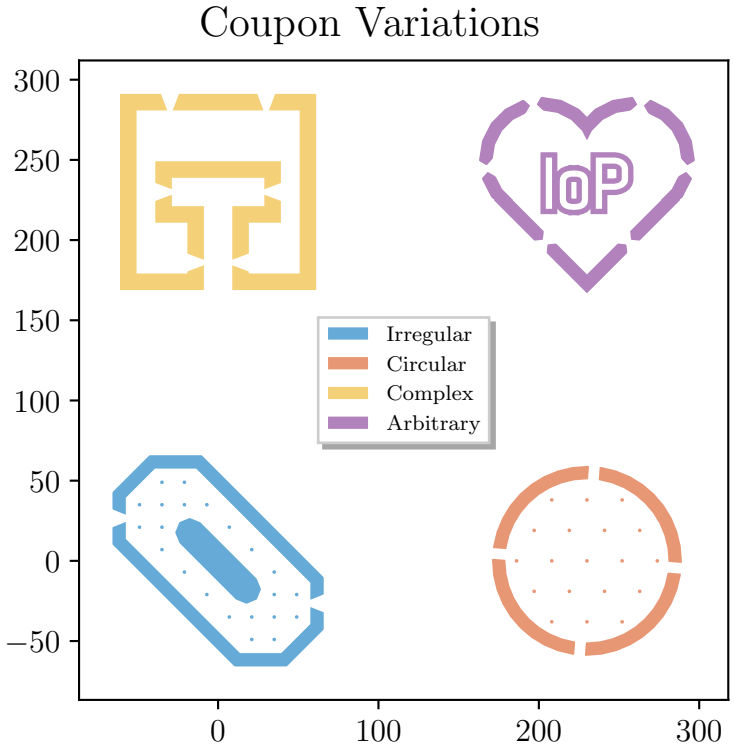

Figure 4.5: **Examples of various membrane geometries supported using default library functions.**

- **Complex:** Simple geometries can be generated and later modified using boolean operations to form complex geometries.
- **Arbitrary:** The geometry generation methods can be bypassed entirely, allowing any polygon object to be converted into a Coupon component.

4.1.4 Component Based Design Hierarchy

The membrane design package is structured around a Membrane class that contains methods for generating each component. Each component, such as Coupon, Border, Anchors, Devices, Holes, and Panels, are also defined as separate classes. This object-oriented approach allows the context of one component to be seamlessly passed onto the next when generating the overall structure. For example, the Coupon class can provide the necessary geometric information required by the anchors to ensure proper alignment and connectivity.

Certain components of the membrane, such as anchors, devices, and holes, can exist multiple times as part of the design. For these components, an additional "Multi" class is provided to facilitate the creation of sets of components seen in Fig. 4.6. For example, the Hole class defines the radius, length, and angle of a single hole component, while the MultiHole class generates grids of coordinates where duplicates of the Hole class are translated. Similarly, the Anchor class generates a tether geometry along the length of a line, whereas the MultiAnchor class duplicates the anchors and updates each anchor with a new anchor line to follow. This approach allows for efficient generation and manipulation of multiple components.

To allow arrays of membrane designs, the Membrane class can be passed into a sub_panel object contained within a Panel class seen in the top of Fig. 4.6. Each membrane within a sub_panel is identical and can be placed based on a desired pitch or spacing. However, each sub_panel within a Panel can contain unique membrane structures, facilitating device arrays and parameter sweeps. This hierarchical approach allows for efficient organisation and manipulation of multiple membrane designs, making it easier to conduct systematic studies and optimise designs via parameter sweeps whilst still allowing groupings of particular designs.

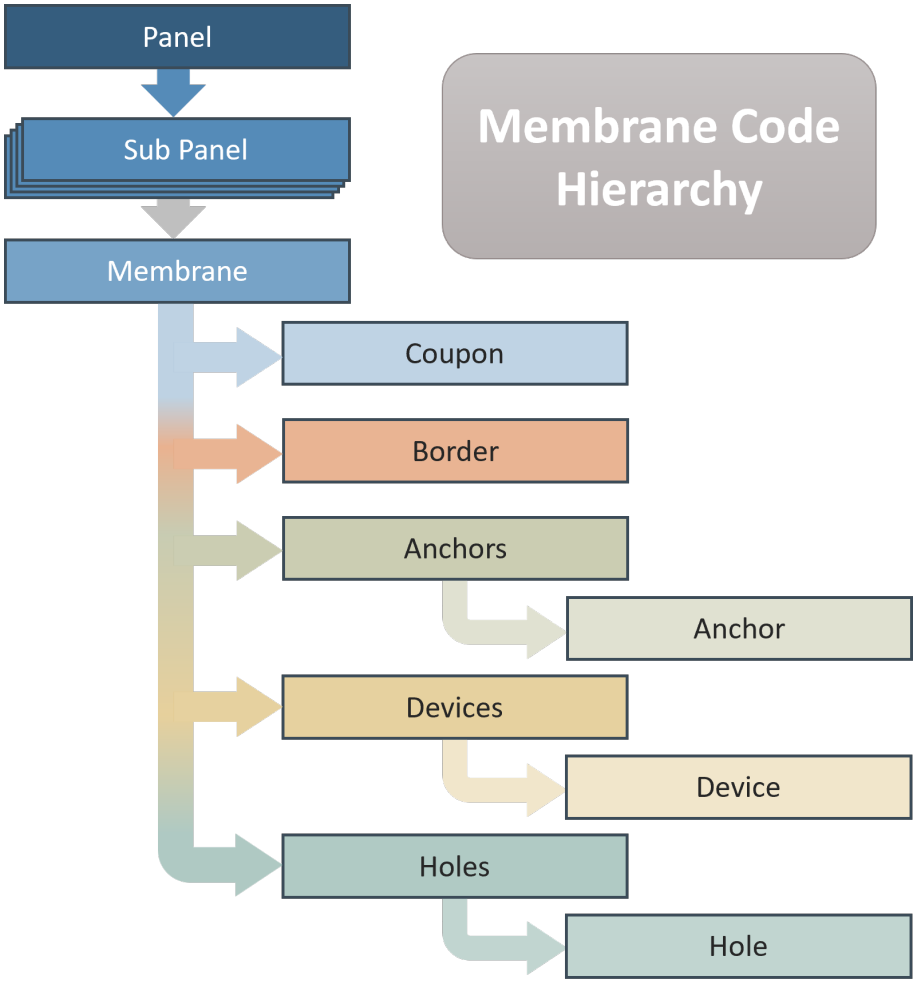

Figure 4.6: **Diagram of component hierarchy.** General generation and manipulation can be carried out through the Membrane class. Lower level operations can be performed by accessing the individual components within the Membrane class.

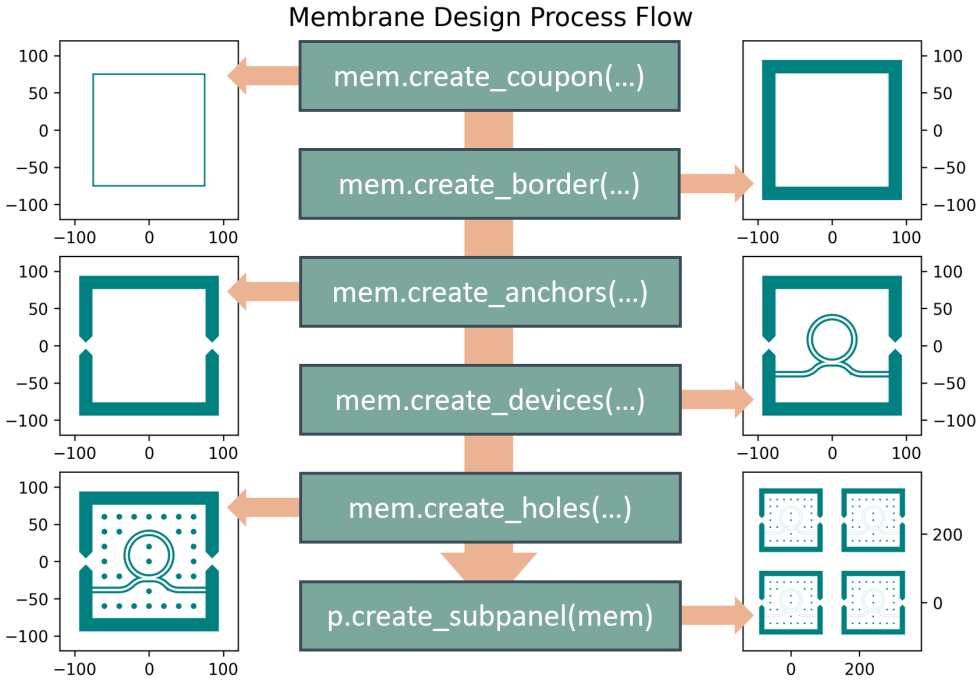

Figure 4.7: **Membrane design process flow.** In the centre, the Python commands used to generate each component, left and right arrows point to visualisations of each command. Downward arrow indicates order in which commands are typically run.

The typical process flow for generating a new Membrane design is illustrated in Fig. 4.7. These six steps cover all the necessary geometry needed to create the majority of designs seen in the literature. Not every step is mandatory; for instance, the creation of etching holes and device geometries can be omitted to allow for simpler membrane designs. Certain components, such as devices and anchors, can be repeated to introduce variations within a single membrane design, to create more complex structures. As printing requirements become more sophisticated, this process can serve as an initial template where more advanced designs are achieved by editing the component classes of the template.

By constructing the membrane in a step-by-step process, conducting design case studies for new wafer materials becomes straightforward. The Membrane class passes the context of each component to the next method call, ensuring that the design updates in a predictable manner. This predictability is crucial for efficiently generating design parameter sweeps, as it reduces time spent troubleshooting. Consequently, users

can instead focus more on design optimisation, leading to more effective and efficient development cycles.

For example, when working with thin semiconductor materials in the sub-500nm range, it is crucial to consider the mechanical properties of the material. The forces applied by the transfer stamp can be high enough to damage the membrane during pickup. By tuning the anchor geometries, we can lower the breaking force required for pickup to below the damage threshold of the coupon. For instance, decreasing the anchor widths can reduce the pickup force. However, this approach has limitations: the lithography systems may not be able to resolve such small features, and overly narrow anchors may not support the coupon adequately during under-etching, leading to premature breakage and collapse. Conversely, anchors that are too wide can cause excessive force during pickup leading to fractures.

Predicting the ideal geometry beforehand is often non-trivial, so it is often more efficient to run a case study with a range of anchor geometries to empirically determine the best solution. An example of this approach is shown in Fig. 4.8, where various anchor parameters, such as width, position, and quantity, are systematically varied.

4.2 Complex Anchors

Transfer printing excels at heterogenous material integration, uniquely enabling the dense integration of multiple materials. To fully leverage this flexibility, it is essential to move beyond demonstrations of "hero" devices and develop designs that can consistently achieve good device yield. One way to achieve this is by utilising more complex anchor designs, which provide better control over the release procedure.

Various anchor geometries have been explored in literature, including straight, tapered, and bow tie variants [42, 51, 59]. Bow tie and taper anchors, in particular, offer better tolerance to variations in material properties, such as strength and thickness, and help ensure consistent material cleaving by focusing the mechanical stress at the narrowest points of their geometry. A design tool should provide an in-built method for the generation of these geometries to fully utilise these advantageous properties.

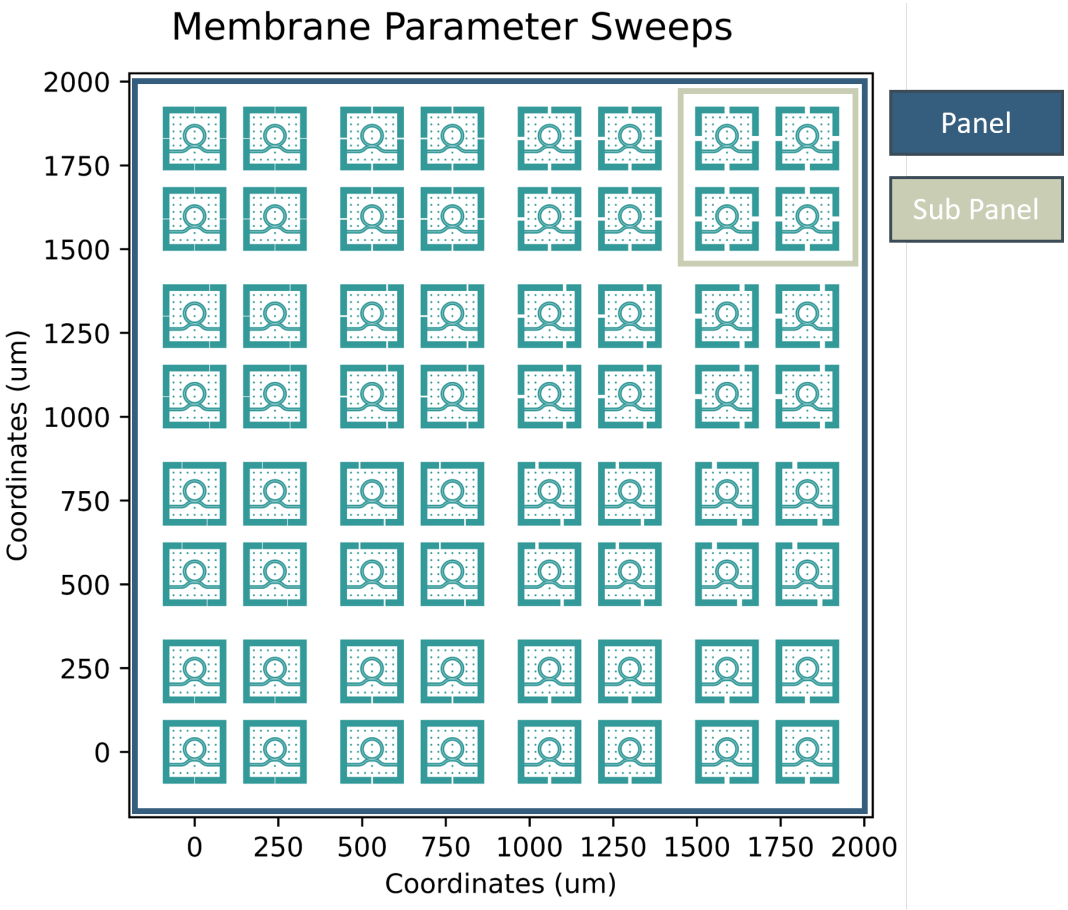

Figure 4.8: **Membrane parameter sweep** Panel containing a membrane design parameter sweep, where anchor widths are varied from left to right, and anchor positions and quantities are varied from bottom to top. The 2x2 *sub_panels* layout allows for the collection of statistical information for each design variant.

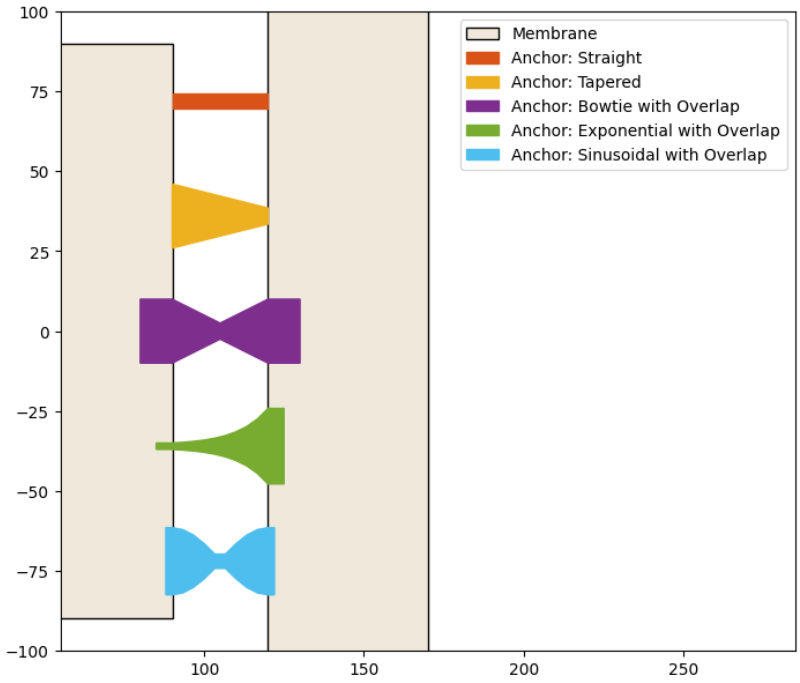

Figure 4.9: **Examples of various anchor geometries that can be produced easily with the Anchor class.**

Creating a unique anchor component for each variation is one solution for this, but would become cumbersome and complex as new design metas emerge. Therefore, a more efficient solution is to develop a universal method that can conveniently generate a large variety of design variations. This approach simplifies the design process and allows for greater flexibility in adapting to new and evolving requirements.

In the next section, a detailed explanation will be provided on how the method for generating anchor geometries, capable of producing the designs shown in Fig. 4.9, is implemented. While similar sections could be written for each component, covering the extensive considerations made for all of them would make for a tedious read. The anchor geometries were chosen as an interesting example because their flexibility and benefits have been well-documented in the literature. This section will therefore highlight the unique challenges and solutions associated with anchor design, providing insights that are also broadly applicable to other components.

4.2.1 Generating Anchors

The anchor generation method must meet several critical requirements to support the diverse needs of advanced photonic device design. First, it must offer flexibility in geometry to accommodate various anchor profile designs. Second, the method should allow precise control over dimensions and placement, enabling accurate alignment and uniformity across multiple devices, which is essential for ensuring high device yield. Third, the method should facilitate efficient computation and utilise existing tools from the Shapely library to enable quick iterations and adjustments.

To meet the first requirement, a geometry generation method similar to mathematical plotting functions was implemented. This begins by creating a line formed from two points on neighbouring geometries, such as the coupon and border, to construct a Shapely *LineString* object, effectively functioning as the x-axis for the design and defined as the *anchor_line* within the library. An array of widths is then passed to the anchor method, plotted symmetrically against the anchor line using a combination of the Shapely *project* and *interpolate* functions. This technique also allows for the easy definition of overlap regions, as shown in Fig. 4.4, which is useful in applications where the membrane anchors are made of a secondary sacrificial material [74].

The second requirement is addressed by imposing a specific design restriction: the anchor must always travel along the shortest path between two geometries. This restriction simplifies the positioning of anchor geometries, ensuring that the anchor is always oriented perpendicular to the edge of the coupon to which it is attached, when using the process as demonstrated in Fig. 4.7. This approach eliminates the need for trigonometric calculations, instead relying on the efficient back end of the Shapely library. The placement of the anchor is determined by selecting one of the edges of the polygon, indexed from 0 to n, where n is the number of edges. The position along that edge is then specified using the Shapely *interpolate* command, which by default returns a normalised position between 0 and 1 for relative control of position but optionally, distances using the base unit of the chosen file format.

The third requirement is met through a comprehensive understanding of the Shapely library, which this package is built upon. This understanding allows for the implemen-

tation of more advanced techniques for generating polygons, using the context of previously defined geometries to our advantage. A graphical representation of this technique is shown in Fig. 4.10, with further details of implementation.

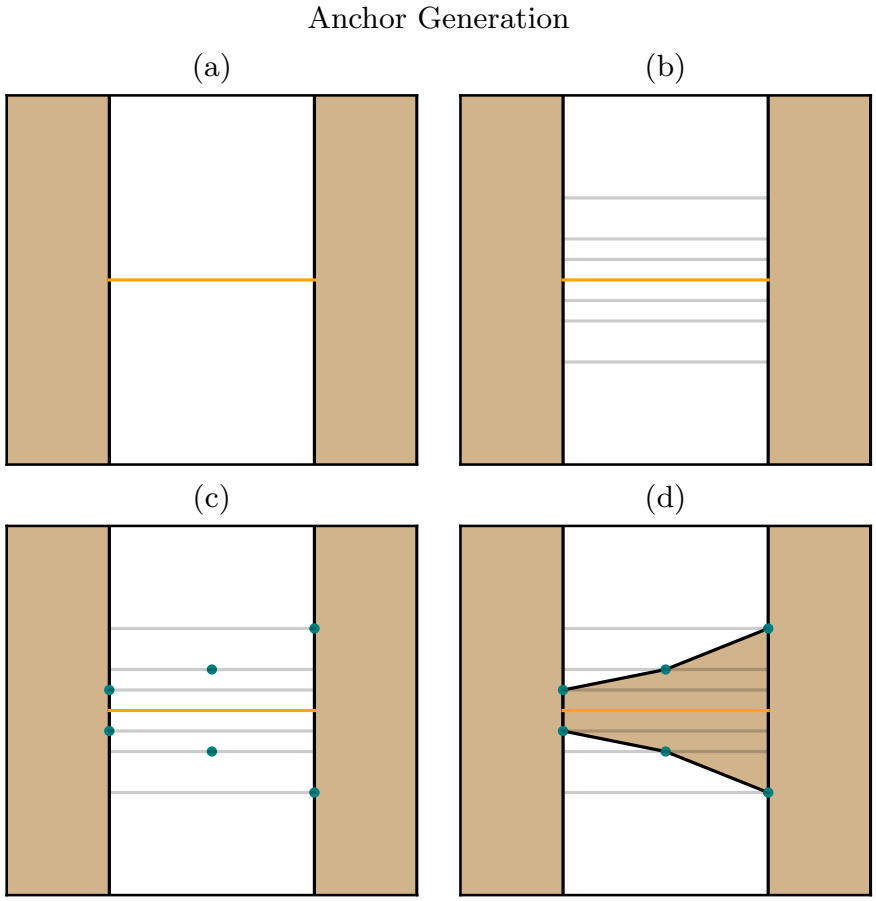

Figure 4.10: **Graphical representation of anchor geometry generation.** (a) A line is constructed between the coupon and the border, the starting point is defined by the user as a relative position on the coupon exterior. (b) Additional lines are generated at offsets determined by the anchor widths, which are parallel to the main line. (c) Points are interpolated onto the respective lines to create the outer profile. (d) Points are combined to generate the final geometry. This method ensures the anchor is always perpendicular to the edge of the coupon it is attached to.

This particular implementation of the anchor component was reached via iteration, through feedback from collaborative working. The initial attempt was the hard coded method discussed earlier. Originally it would only work for rectangular coupons and only predetermined anchor positions were available based on the quantity of anchors

used. Since then the implementation has become inherently more flexible as personal experience with nanofabrication and code development grew over the course of this project. This is also one key benefit of developing these software solutions in-house, as they allow rapid iteration of features to tailor towards personal use cases.

4.3 Membrane under etching

To facilitate the mechanical transfer of the coupon, a sacrificial etch layer (SEL) beneath the membrane is removed, leaving the coupon suspended solely by the anchors. In this state, the transfer print tool head can attach to the coupon's surface and apply a mechanical lifting force that cleaves the supporting anchors. Various etching techniques can be used, such as vapour etching [137] and wet etching techniques [42]. However, wet etching processes are typically used, where the wafer is fully submerged in a liquid etchant solution for a set period dependant on the size of the membrane being released. After this time, the wafer is removed and submerged in a neutralising solution to prevent residual etching or oxidation of etchants on the surface. The sample then undergoes a gentle washing and drying process, producing a usable transfer print donor chip.

Different etch behaviours are observed depending on the specific chemistry of the chosen etchant, the SEL and the rest of the wafer stack. These behaviours range from highly isotropic to highly anisotropic, with the primary contributing factor being the differences between the underlying crystal structure and the epitaxial layers (epi-layers) of the wafer stack. It is typically best practice to run a test geometry when trialling a new combination of etchant and wafer stack so that parameters such as side-wall roughness, etching time and etch isotropy can be measured empirically.

For a highly anisotropic processes such in Fig. 4.11(a) the etch front propagates in a purely linear fashion, such that the shape of the etch front is maintained throughout the process. This directionality occurs due to the underlying crystal structure of the SEL where particular planes that bi-sect the crystal have higher or lower densities of atoms, making it quicker for the etchant to propagate in particular directions. For highly isotropic etches, such as Fig. 4.11(b) there is no preferred direction for the etch

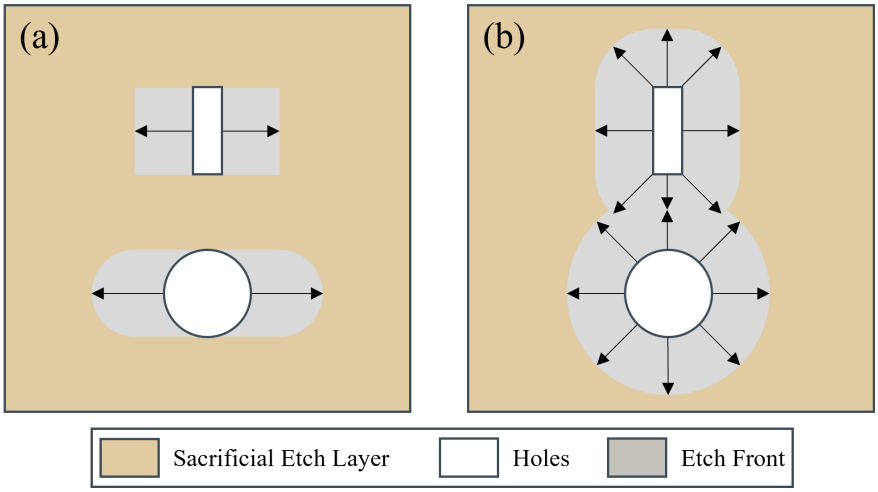

Figure 4.11: **Comparison between etching behaviours** (a) Example schematic of a horizontal anisotropic etch. (b) Example schematic of an isotropic etch

front to propagate, and instead it extends in all directions uniformly.

When fabricating panels of membrane devices it is undesirable to under-etch all of the SEL, as that can cause the entirety of the device layer to collapse onto the substrate causing catastrophic breaks. As such, the density of devices should be considered when designing membrane panels. Anisotropic etches can be exploited to enable high density arrays by orientating the border and anchor geometry such that they run complementarily to the etch fronts, it is possible to create arrays where only the anchors and coupon are suspended as in Fig. 4.12 (a & c). This allows the suspension length (SL) to be as short as possible, which helps to keep the rigidity of the suspended device high.

The scenario depicted in Fig. 4.12 (b) often presents more challenges during process development, as the uniform etching profile also attacks the area beneath the supporting border structure. This causes the SL to exceed twice the shortest length of the coupon. The large SL can cause the device to deflect downwards towards the substrate. Given that a typical thickness of the sacrificial layer can be $< 2\mu m$, this can be sufficient to cause the underside of the membrane to touch the substrate. As the SEL is often chosen for its low surface roughness, this contact can result in the membrane bonding to the substrate via Van der Waals forces, preventing the device from being transfer printed and reducing the yield of the donor chip.

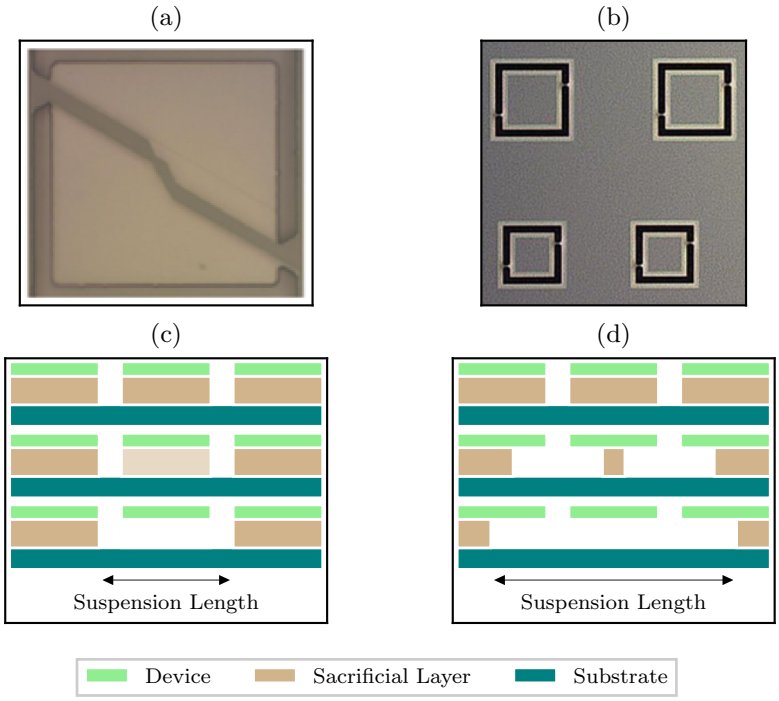

Figure 4.12: **Comparison of Etching Behaviours** (a) Anisotropic etching profile of membrane LED, courtesy of Eleni Margariti (b) Near isotropic etching of blank AlGaAs membrane devices, courtesy of Elise Burns. (c-d) Schematic view of suspension length for anisotropic etch and isotropic etch, respectively.

These challenges limit the transfer print-based heterogenous integration of III-V semiconductor materials, particularly in waveguiding applications where their tunable non-linear refractive indices can be used as printable cladding layers for quantum applications [73, 120] or as independent waveguide features that are shallow etched [74]. For these applications, thin-film devices are required to be $\leq 500\,nm$ in thickness to allow single-mode operation, making them particularly vulnerable to the aforementioned issues owed to their reduced rigidity. The remainder of this chapter discusses the techniques and metrics integrated into this package to facilitate the integration of such devices.

4.4 Etching Holes

To address the issues of membrane collapse, holes can be added to the surface of the coupon to expedite the etching process. These holes penetrate the same portion of the layer stack as the gap region, allowing the etchant greater access to the SEL beneath the coupon. These holes provide multiple entry points, dramatically accelerating the under-etching process and reduce the SL. For a perfectly isotropic etch with a circular dilation pattern, the SL is nearly halved by placing a single hole at the centre of a square coupon. Given that waveguide devices occupy a relatively small area of the coupon, multiple holes can be included to enhance this improvement.

When creating a distribution of holes the user has control over the several key parameters such as hole radius, hole spacing, and distance from the coupon edge. The collection of holes is aligned to the centre of the coupon by default. To analyse the benefit of increasing the amount of etching holes we can introduce a metric which we can use to measure the etching performance, for example the membrane etch length (MEL). The MEL represents the minimum lateral length the etchant is required to traverse for a geometric region to be fully underetched. For identically spaced holes this can easily be determined using geometry and the assumption of an isotropic etch. For a square grid this is calculated as the hypotenuse of a right-angle triangle with side lengths equal to half the hole pitch. The impact of increasing hole count using this metric is illustrated in Figure 4.13 (b).

As seen in the figure, increasing the hole count by reducing hole spacing provides a linear benefit in reducing the MEL, thereby shortening the SL. However diminishing returns are observed as the decrease in MEL is linear but the hole count increases as $N_H \propto \Delta P^2_{H(x,y)}$, where N_H is the number of holes, and ΔP_H is the hole pitch. Second to this, too many holes on the coupon will compromise its function in transfer printing by removing too much area from the coupon. The coupon serves to provide contact area both for the print head to mechanically pick up the device, as well as to offer enough surface area for Van der Waals forces to bond the device to the receiver substrate. Both of these are critical for a successful transfer print, so the coupon's integrity should be

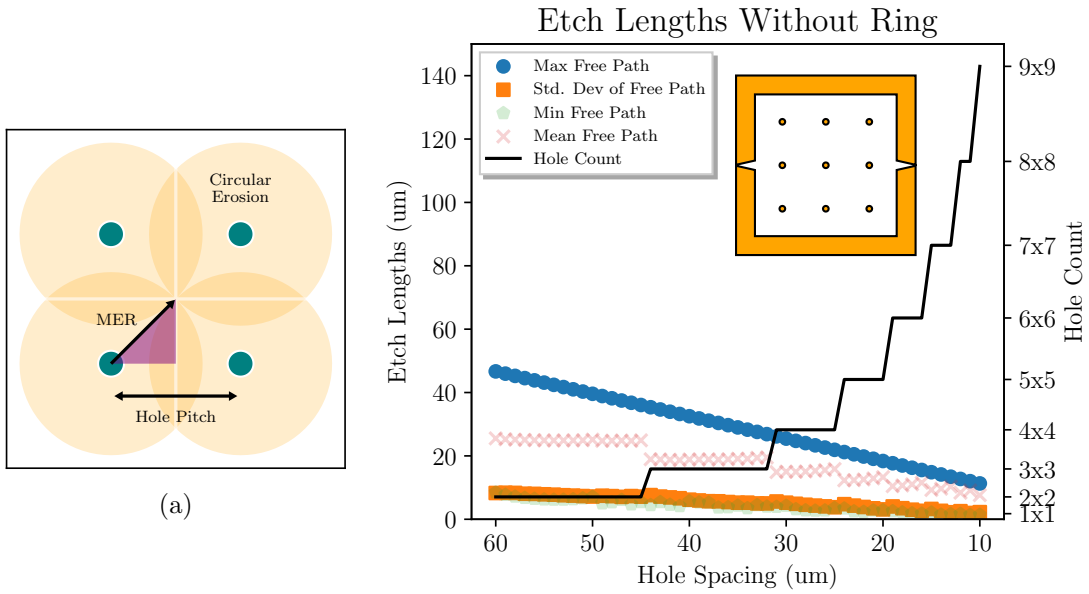

Figure 4.13: **Membrane Etch Length versus Hole Count** (a) Schematic drawing showing how Maximum Free Path is calculated, assuming circular etch front and rectilinear hole arrangements. (b) Trend of MEL versus Hole spacing, a linear decrease in MEL can be seen while hole count increases in a step-like fashion, proportional to the square of the hole spacing. This figure ignores contribution to etch performance from the Membrane gap region.

prioritised.

Using sparse arrays of holes on the coupon surface is ideal for reducing MEL in blank membrane devices, thus addressing issues related to large SLs. However, this technique is hard to apply to membranes for waveguiding applications as despite their small feature sizes, their variability in design can regularly lead to features overlapping with holes. This variability necessitates the development of unique hole spacing for each design, consuming development time and hindering parallel fabrication restricting applications to "hero" devices. The next section describes this issue in more detail and the solutions that have been implemented within this design package.

4.5 Conformal Placement Around Devices

As an optical mode propagates through a waveguide structure the majority of the light is confined within the physical structure of the waveguide, assuming the guide has been designed for low loss single mode operation. However, a small percentage of this light propagates outside the waveguide structure as part of the evanescent tail [32], this amount can interact with the external environment to modify properties of the mode. This proximity based effect is what allows vertical waveguide coupling to transfer printed devices [65, 74] amongst other applications [138, 139] by providing optical structures that can perturb the mode. Whilst this proximity effect can be useful, unintended use is undesirable. The etching holes can act as a perturbation source as they are pockets of low index material (air) surrounded by high index material (device layer), as the mode propagates through the device the evanescent tail can interact with these index step changes and perturb the mode. To avoid these issues the etching holes are often placed several microns away from any guiding geometry as a minimum, this effectively creates a virtual increase in device footprint on the coupon.

To avoid interference with the optical device by either the proximity effect or breaking the device geometry, the offending holes are selectively removed from the surface of the coupon introducing two problems. Firstly, the etching performance of the design is significantly decreased as there are sections where the hole pitch is now N times the target pitch, based on the number of consecutive holes deleted from the design. Secondly the MEL metric implemented previously breaks as the hole array is no longer identically spaced. Starting with the latter we require a more robust method of determining the MEL that can handle not only the irregular layouts as a consequence of the device component, but also the flexibility of the coupon coupon geometry demonstrated earlier.

4.5.1 Robust MEL

As every optical or mechanical component within this package represents some form of polygon, line, path, or array, we can use a variety of geometric operations to our

advantage outside simple trigonometry. To produce a robust method for the MEL we need to first look at dividing the coupon into discrete contiguous regions defined by the layout of the etchant entry points, with this defined we can evaluate the MEL based on the whether the etchant progresses from a line source such as the gap region, or a point source like an etching hole.

An array of etch regions can be generated by means of a Voronoi diagram, which is a method of dividing a plane into regions based on the distribution of seed points. It is the mathematical equivalent of allowing circular etch fronts to propagate from a provided set of seed locations, where the region boundaries are defined as every location where points on neighbouring regions collide [140]. The technique is indifferent to the distribution of the seed points, so the pseudo-random position of the etching holes can be used. To properly account for the contribution from the gap region the coordinate positions from the coupon perimeter can be included, however to simulate the effects of a line source, additional points are interpolated along the coupon perimeter of a spacing an order of magnitude less than the initial pitch of the etching holes. An example of this Voronoi diagram can be seen in Fig. 4.14 (b).

After defining these regions the MEL can be calculated using one of two methods, if the region was defined by a line source like the gap region or a large feature embedded in the coupon we can use the longest distance perpendicular to the edge of the feature to the opposite side of the etch region. For a point source like the etching hole we can use the Hausdorff distance measurement which is defined as the longest of the shortest distances between two polygons [141]. Each point on the first polygon is compared to all the points on the second polygon, with the shortest combination recorded. Once repeated for each point, the largest of these shortest distances is taken as the Hausdorff distance. Using a square grid of holes, this approximation is equivalent to the MEL implementation discussed earlier but is now able to adapt to various device geometries as well as any missing holes. With a robust method of monitoring the MEL for any distribution of etching features, the correlation between hole count and etching time can be measured as in Section 4.5.1.

The under etch process is limited by the longest MEL. By removing the overlapping

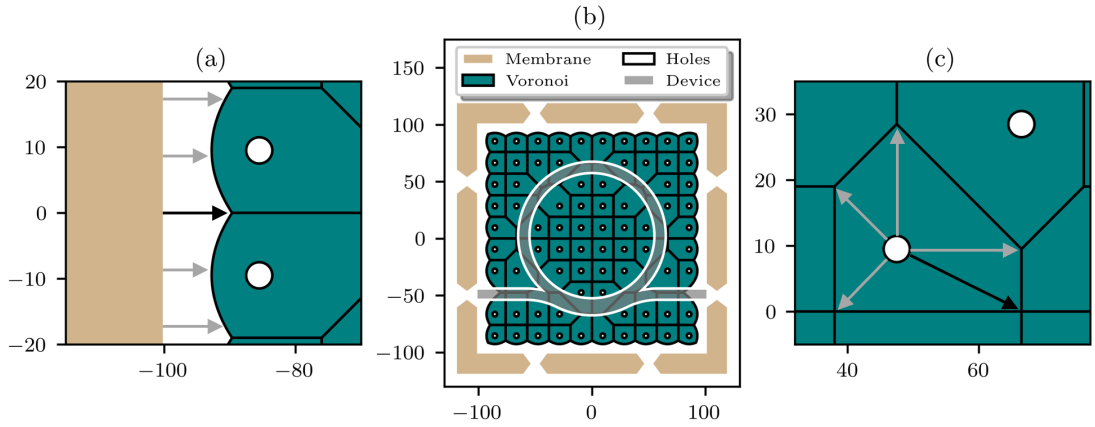

Figure 4.14: **Voronoi diagram and minimum etch length** (a) Minimum etch length calculated as from a line source, the coupon edge, shown in black. (b) A Voronoi diagram calculated from the layout of etching holes. (c) Minimum etch length calculated from a point source, the etching hole, shown in black.

holes, it has the same overall effect as doubling the hole pitch. This is a particular issue as this creates localised areas where the release process is longer, which is often adjacent to the device region of the membrane. This can lead to significant stress points forming during processing due to the rest of the membrane being suspended, free to mechanically flex. As seen in Fig. 4.16. These problems can be mitigated somewhat by varying the hole spacing or increasing the size of the coupon but this wouldn't always be ideal. As the purpose of this package is to be a design tool for Membrane devices, it should provide a robust solution for these issues.

4.6 Device avoidance

An intelligent way to mitigate the issue of overlapping hole geometries, would be to avoid removing them altogether and instead shift their positions slightly so they avoid any optical structures. This will still decrease their effectiveness as the holes will no longer be uniformly distributed, however the impact of this is much less that if the hole

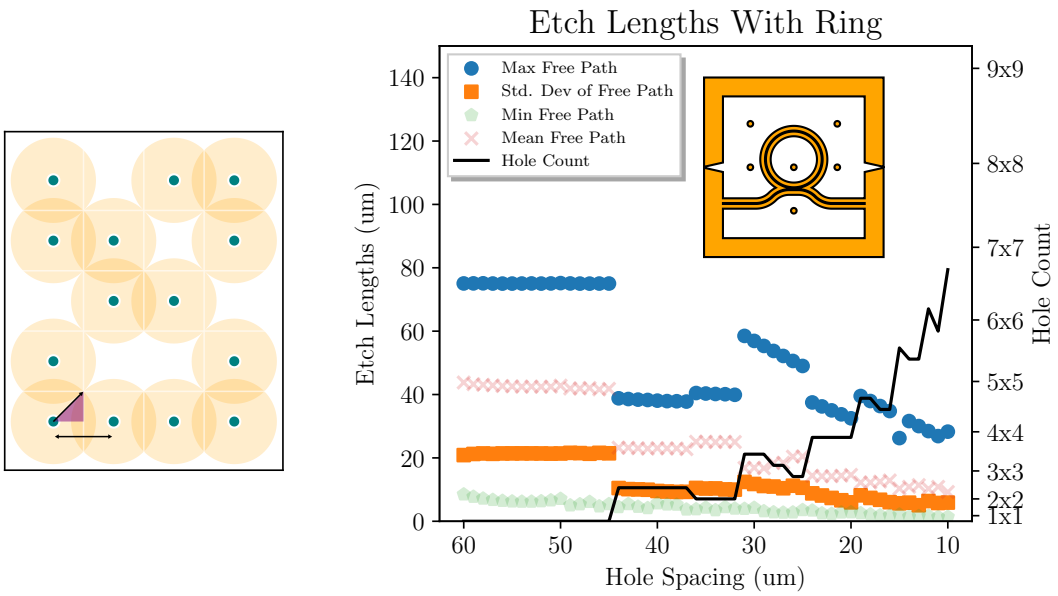

Figure 4.15: **Membrane Etch Length versus Hole Count with Device** (a) Schematic drawing showing effect of device presence on the layout of etching holes. (b) Trend of MEL versus Hole spacing, an erradic behaviour can be seen as the hole spacing decreases due to different hole configurations nesting around the device more uniformly than others. This figure ignores contribution to etch performance from the Membrane gap region.

was removed entirely.

Within the package the holes are designed as their own component contained within an a multi class, This allows various affine transforms to be applied to the geometry to modify the distribution of the array. From simple methods such as moving to a set position or by a set amount to more advance manipulations such as displacing along the path of a geometry and 'snapping' to a particular structure. These facilitate a range of manipulations to be carried out based on what the context deems most suitable. However, manual manipulation of these etching components can quickly reach a level of tedium that would inhibit their day to day use as each membrane design would need to be individually defined. Instead we can reuse the Voronoi diagram used to calculate the MEL to provide the translation direction required for each hole component.

The implementation device avoidance here is fairly straightforward, and provided as an optional input parameter for the user. First the tessellation is constructed using

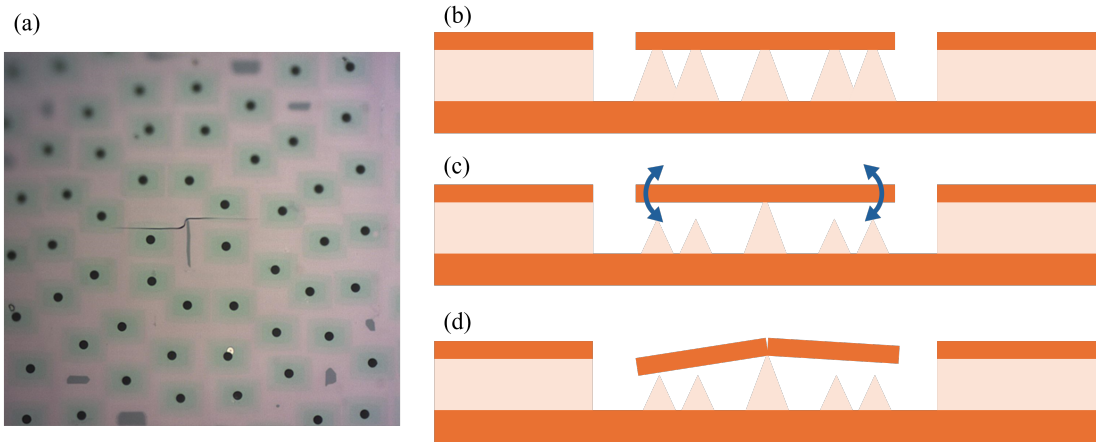

Figure 4.16: **Example of membrane fracture.** (a)Fracture due to sacrificial layer etching non-uniformly forming sharp ridge underneath membrane surface. **Image courtesy of Elise Burns.** (b) Schematic view of under etch behaviour, pointed "tent" shaped structures form underneath the device layer of the membrane. (c) Uneven hole placement results in pivot point where membrane can flex during the under etch process. (d) eventual snapping of membrane around the fulcrum point.

the origins of the etching holes as the seed points, before any that overlap with the device are removed. Any that would be removed instead have the boolean difference of the protected device area taken from their etch region. We can refer to the leftover area as the protected etch region (PER). The hole is then translated to the centroid of this PER region, where the via can still contribute significantly to the etching process. The implementation of this technique provides no significant increase in computational time compared to the default method ensuring convenient use in real world applications.

4.7 Lloyd's algorithm

Lloyd's algorithm belongs to a family of relaxation algorithms, mathematical models that take a given data set and modifies it in a step wise process, until a condition is met. Lloyd's algorithm is a spatial relaxation algorithm that takes a random distribution of points within a constrained area, such as the membrane coupon, and attempts to shift their position such that its adjacent neighbours are all an equal distance from one another. Lloyd's algorithm can be used to conform the distribution of etching holes around the device geometry to mitigate scenarios where the area under the device is

etched last, as this can lead to stress points forming where the membrane is most fragile.

The typical implementation of a Lloyd algorithm is as follows, a set of 2 dimensional points are provided as the seed for a Voronoi tessellation. The centroid is found for each region of the tessellation and is taken as a seed point for the next iteration. This loops until the amount any given point is shifted falls below a threshold condition. Once met, the Voronoi pattern is considered to have reached equilibrium. If we apply this to the distribution of holes for an isotropic etch, this should result in every region of the final Voronoi pattern etching within the same period of time due to their uniform distribution.

The implementation within this package is slightly modified as it has to also avoid the device geometry. Typically a Lloyd algorithm will be implemented within a closed geometry that is empty, that allows the algorithm to manipulate the position of each point without risk of overlapping any internal structures. However, in this instance overlapping the device should be entirely avoided. This is where the the device avoidance method described earlier is utilised, after each iteration of the algorithm, the avoidance method is utilised to make sure that no holes overlap the device geometry within a specified radius.

When implemented as part of the Lloyd algorithm, there is an edge case to the device avoidance that should be considered. It is possible that when the device geometry is subtracted from the hole etch region, that the PER generated is split into N smaller regions. For this work, the largest of N regions is used whilst the rest are discarded. However, generating a hole for each additional region was also tested, but resulted in runaway conditions, particularly in acute corners that would endlessly "spawn" new holes. This behaviour was undesirable as it would result in cases where panels of devices would not etch uniformly due to a variation in hole densities caused by design variations. By generating holes only at the largest region, the total number of holes would remain the same at the end of the algorithm. This increases the predictability of any one design enabling easier development of device panels with a range of transfer printable PIC modules. This improved predictability can be seen in Fig. 4.18

In this figure we can see that the etching time plateaus for each increase in hole

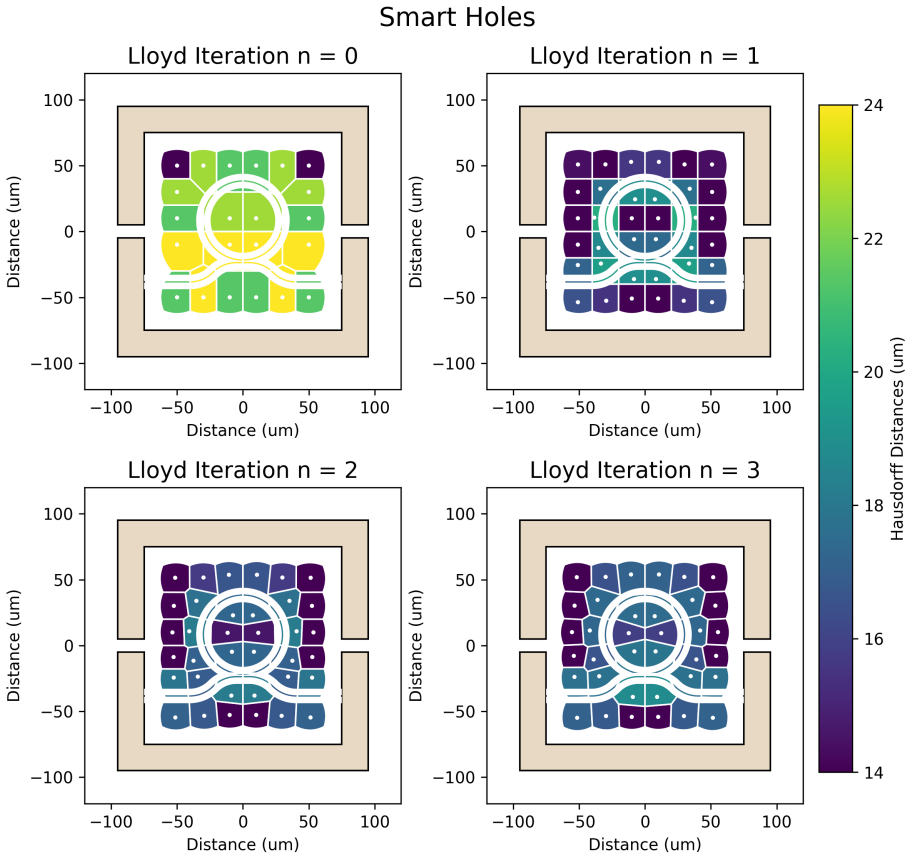

Figure 4.17: **Visual representation of Lloyd algorithm progressing in a stepwise fashion.** For $n = 1$ the device avoidance implementation is activated. For $n > 1$ all holes begin to redistribute themselves around the device.

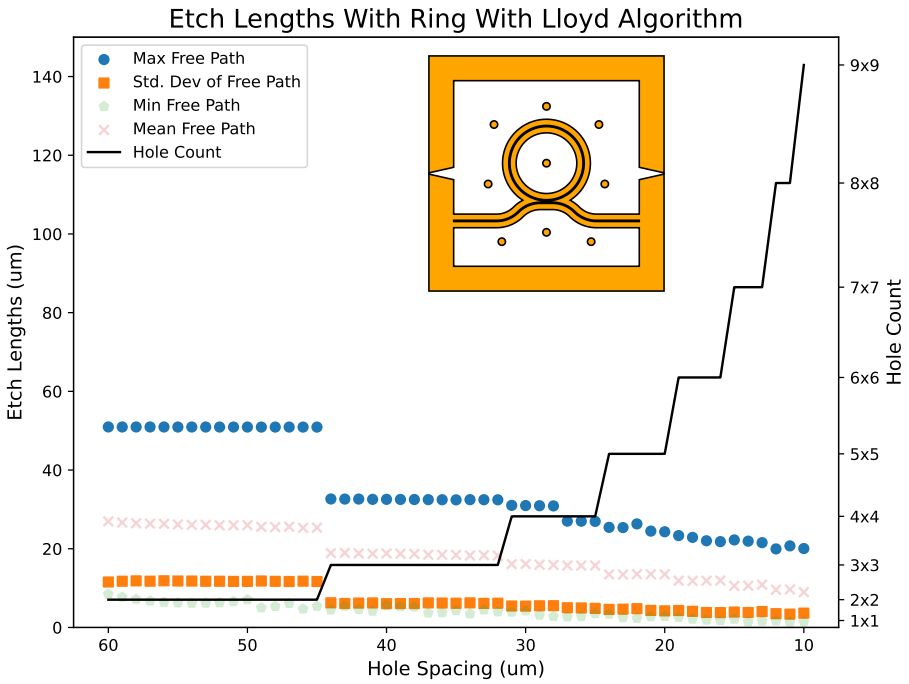

Figure 4.18: **Membrane Etch Length versus Hole Count with Lloyd Algorithm** A predictable decrease in MEL can be seen where the DEL plateaus with each increase in hole density. This figure ignores the contribution to etch performance from the membrane gap region.

count, due to the etching holes finding their uniform distribution across the membrane. This means that the hole spacing defined by the user isn't necessarily the hole spacing of the final result after utilising Lloyd's algorithm. As such it is included within the *create_holes*() method to provide an upper limit to the iteration count using the 'order' parameter. An order of 0 is the default and results in identically spaced holes with overlapping holes removed, an order of 1 enables the device avoidance functionality. an order of 2 or more runs the Lloyd algorithm as described. For weakly isotropic etching processes, such as shown in Fig. 4.16 where the etch fronts progress in a rectangular fashion, low order numbers are recommended as they maintain an overall grid-like distribution.

4.8 Device Etch Length

Thanks to the implementation of smart holes, a key development in scaling the membrane device fabrication to industry is now available. Typically large membranes require a longer etching time compared to smaller membranes, this is due to the MEL being defined by the coupon dimensions. If combined in a set, the largest MEL would define the etching time for the rest of the designs. This could lead the smaller membranes to have an SL many times larger than the length of their coupon. This would make them prone to collapse or difficult to pick up. For waveguiding devices this can be mitigated by the smart placement of etching features, which then switches the MEL's dependency on coupon dimension to the etching hole spacing, which is independent of any other membrane geometry. Being able to fabricate multiple device footprints on the one chip would allow foundries to provide lower minimum order quantities and allow customers more parameter spaces for designs affordably.

However, even with intelligent hole placement algorithms it is sometimes impossible for two device designs to etch within the same period if the target time is too short. Such as the case shown in Fig. 4.19. In this figure, it is clear to see that even though each design is of a ring resonator of matching radius and mesa width, the presence of a coupling waveguide can have a significant impact on the device etch length (DEL).

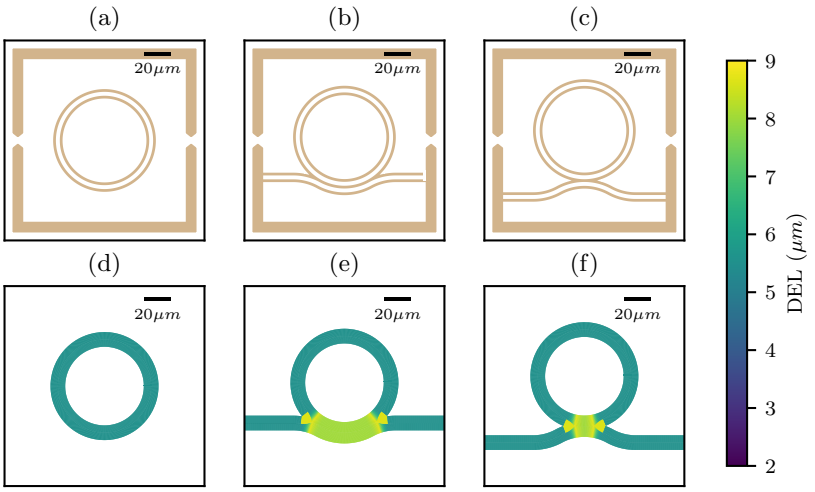

Figure 4.19: **Variations of ring resonator device embedded on a membrane** (a-c) Membrane ring resonator variations. (a) With no coupling guide. (b) With coupling guide and large coupling region. (c) With coupling guide and small coupling region. (d-f) Representations of device etch length, where etch starts a distance away from the mesa region equal to the edge gap.

In many instances the user can have an intuition on which variations would have the same DEL, but it isn't always obvious. As such, it is important to be able to quantify this parameter as it provides the lower limit to the etching time for any device.

When the user defines the device geometry, the there are 3 main parameters: the device itself, the width of the mesa region and gap left around the mesa that determines the allowed proximity of any etching holes. When defining the device, the object is converted to its Shapely equivalent structure inside a Device object. This conversion means that any GDS library that is built on Shapely is directly compatible with this tool, it also allows control of the absolute positioning of the device relative to the coupon. The mesa width determines the region that is shallow etched onto the coupon that defines guiding structure, when a mesa width of 0 is given a negative resist tone device is returned. A schematic view of these 3 parameters can be seen in Fig. 4.20.

To be able to retrieve the device's etch length, we can again utilise a Voronoi diagram as we did with the etching holes. However, instead of providing a uniform distribution

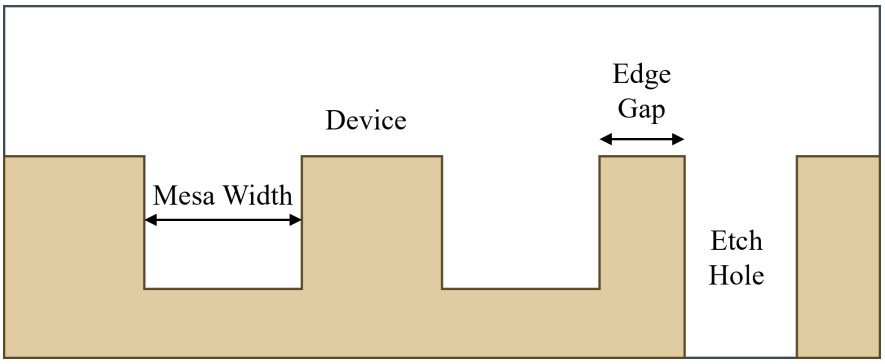

Figure 4.20: **Schematic view of coupon cross section with shallow etched device.** Annotated regions can be set by the user during the design stage.

of points, we pass the perimeter of the device geometry, after it has been broken into segments of a maximum length, as the seed. The segmenting technique ensures that every existing point on the perimeter is preserved, to ensure accurate recreation of the device regardless of the maximum length chosen. These points are then grouped with the regions they spawned during the tessellation and are stored within the devices class instance.

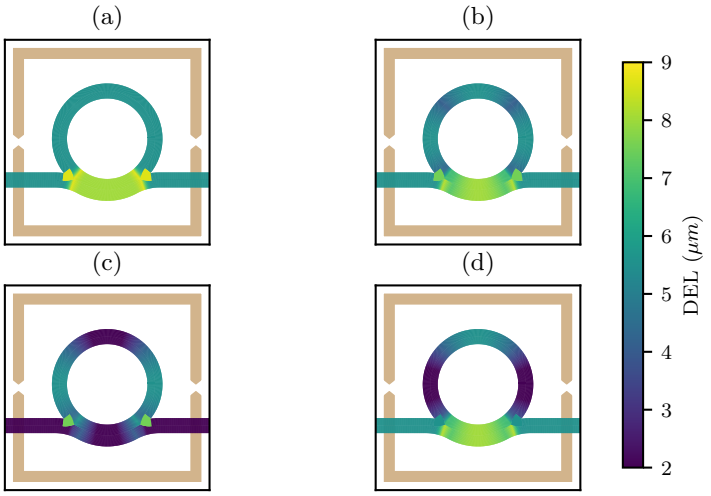

Figure 4.21: **Comparison of various etch metrics** (a) Hausdorff Distance (b) Cardinal Distance (c) Horizontal Distance (d) Vertical Distance

Once the etch regions have been calculated, they are paired with their respective

seed points and stored in a list within the device class. This allows various metrics to be measured after the Voronoi diagram has been constructed, such as Hausdorff distance as well as an additional metric created in this work termed the cardinal distance. This takes the longest X or Y component of the Hausdorrf distance between the seed point and the region's bounding box. This allows a more rectilinear etch front to be approximated as seen in Fig. 4.12 (b), and can highlight which devices will be harder to under etch than others.

The implementation for the DEL is such that the generation of the device etch map can be done within a few minutes and often much less dependant on device complexity. This allows users to iterate based on its output regularly, for a rapid prototyping cycle. The etch maps of various devices can also be collected easily to allow comparisons to evaluate which devices could potentially be batched together within the one chip.

4.9 Fabrication

To validate that this design methodology works in practice, a pattern was constructed to compare the performance of the standard method of placing etching holes versus the smart algorithm implemented in this chapter. A spiral waveguide structure was chosen for this demonstration as it highlights the challenge of placing holes within tight spaces. The majority of the spiral footprint is in close proximity to itself, when superimposed with a uniform grid of holes it results in many sections where the holes initially overlap the structure.

The AlGaAs wafer stack consisted of a GaAs substrate, a $2\,\mu m$ SEL of low aluminium content AlGaAs and $0.5\,\mu m$ device layer consisting of high aluminium content AlGaAs. The SEL was removed using a citric acid underetch process and can be seen monitored in 50 minute increments in Fig. 4.22. It can be seen clearly that a large portion of the holes are missing in the standard method due to the device overlap. The smart hole method results in a uniform distribution of holes across the coupon despite the large footprint structure embedded. Despite the underetch process showing anisotropic properties with a rectilinear etch progression there is still a substantial

benefit to etching time observed between (d) and (h). This is important as most under etch processes aren't fully isotropic as in the ideal case discussed in the modelling.

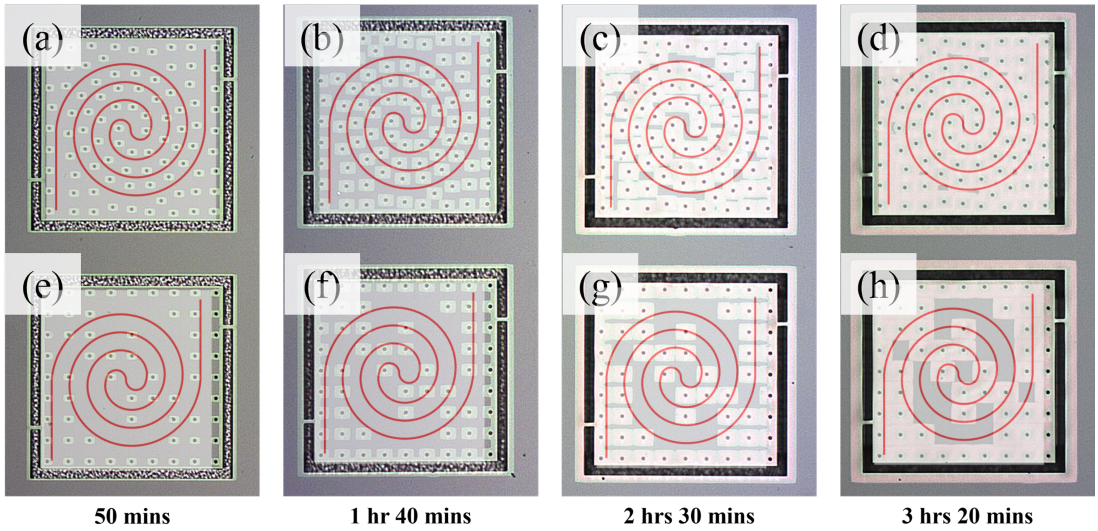

Figure 4.22: **Demonstration of smart etching holes.** Suspended membrane structures with designed to contain a spiral shaped waveguide (highlighted in red) with etching holes placed surrounding the structure. (a-d) Holes placed conformally around the structure using a Lloyd's algorithm of order 5. (e-h) Standard method of hole placement where overlapping holes are removed. Etch lateral etch progression can be seen in steps of 50 minutes from (a) to (d) and (e) to (h) respectively.

4.10 Conclusion

A method for the design of membrane format devices was developed to enable easy development of masks for suspended membrane structures that at the time of writing have not been publicly available before. A focus was placed during the development on flexibility and modularity to ensure it could adapt to a variety of membrane structures including those demonstrated previously in literature as well as more advanced structures needed as transfer printing technology matures. A component based approach was taken to divide the membrane into key parts, that act as building blocks for one another. This facilitates regular activities such as parameter sweeps to determine the best geometry to ensure high device yield. Care was taken to develop each component of a membrane structure to enable not only the functionalities needed in a membrane

device, but also to remove the challenges associated with learning to design structures within a programming language. By developing a component hierarchy designs can be developed in a stepwise manner, this lowers the complexity needed for any particular design.

Different etching regimes were discussed in terms of isotropic and anisotropic wet etching, with a focus on the former and its effect on the membrane suspension length. The inclusion of etching holes was described, and their effect of speeding up the under etch process as well as the diminishing returns as hole density increases. Following its introduction, device avoidance strategies were discussed in the form of a modified Lloyd's algorithm, to enable automatic conformal placement of etching holes around a device to enable efficient under etch processes. Following this, two related design metrics were introduced as a feature of this library.

Methods for calculating the Membrane Etch Length (MEL) and the Device Etch Length (DEL) were provided to allow the user a planar view of etching behaviour, allowing identification of challenging structures before a timely fabrication process. This enables an easier path to make "smarter" membrane designs, enabling deterministic transfer printing of challenging structures such as thin-film III-V semiconductors, or large form factor structures.

Fabrication results were shown for smart holes placed conformally around a spiral waveguide membrane device, and then discussed in detail. A substantial decrease in etching time was observed even despite the anisotropic etch process of the AlGaAs membrane, showing that this implementation of smart holes could be applicable to many material platforms.

This package is a stepping stone towards enabling transfer print friendly designs of photonic structures by providing tools that allow the creation of GDS mask geometries with the context that is relevant to the design of suspended membrane structures. This provides a stepping stone for the technique of transfer printing to become more mature by supporting all aspects of the fabrication process.

4.11 Future Work:

4.11.1 Weighted Stippling

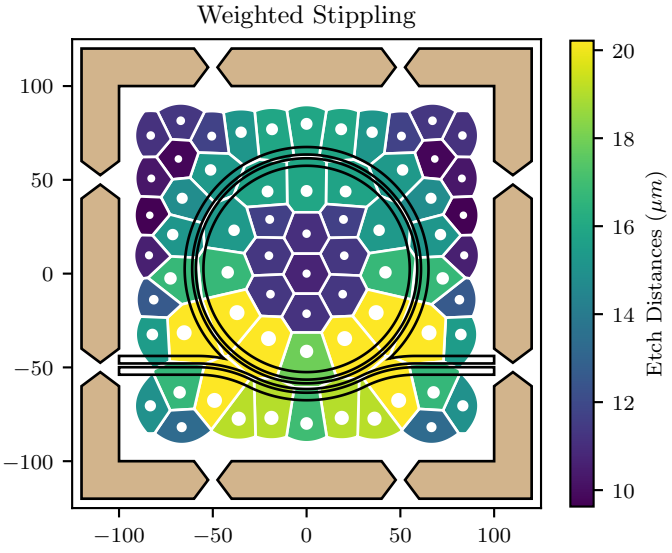

Figure 4.23: **Concept implementation of weighted stippling.** The radius of the etching holes is determined by the size of the etching region. This could potentially decrease the standard deviation of the membranes wet etching characteristics, leading to more uniform and controllable etches.

Weighted Stippling refers to the deterministic placement of dots of varying sizes to create shading effects in artwork. In this context, it involves varying the etching hole diameter or geometry based on the measured Hausdorff distance. This method aims to reduce the standard deviation of Mean Free Paths (MELs) for a given design, ensuring more uniform and predictable etch behaviour. The technical challenge lies in preventing the etching holes from encroaching on the device region, whilst avoiding the need for computationally intensive design checks.

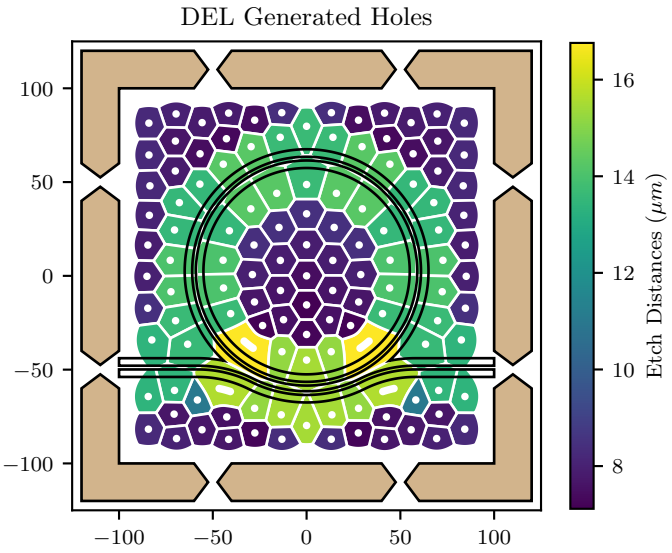

Figure 4.24: **Concept implementation of DEL generated holes.** Regions where the DEL is above a certain threshold are taken as the locations to generate additional holes to provide a more direct hole optimisation technique.

4.11.2 Generation of Holes at High DEL Locations

The total etch time of a membrane is significantly influenced by the DEL. Automatically placing additional holes in critical areas could optimise the etching process. Regions identified by the Voronoi diagram as having high DELs can be targeted for additional hole generation. The technical challenge here is to provide controllable threshold conditions for consistent behaviour.

4.11.3 Support Pillars

Non-uniform etching can lead to structural issues, such as device fractures, caused by high DEL regions acting as stress points while the rest of the membrane is fully released. Selectively displacing the etching vias around strategic locations on the membrane could mitigate these issues. This approach allows for more precise control over the under-etch

process, such as creating sacrificial material pillars at membrane corners that last long enough for high MET regions to etch fully, thus preventing turbulent shaking during processing. The technical challenge involves implementing a tuneable displacement of the hole geometries.

4.11.4 Anchor Dimension Study and Simulations

While this chapter demonstrates a comprehensive design tool for generating anchor designs, a detailed study on which geometries are optimal for specific configurations has not yet been conducted. The primary challenge is the volume of testing required for a thorough study. A potential solution is to combine small-scale studies with integrated simulation tools. Python's extensive library includes Finite Element Modelling (FEM) simulation suites that can be integrated into this package, enabling a series of standardised simulations based on material strength and anchor geometry.

Chapter 5

Integration of Photonic Crystal Cavities with In-Situ Monitoring

5.1 Introduction

Two dimensional photonic crystal cavities (PhCCs) allow high spatial confinement of light within solid state materials. With high resonant Q-factors that can exceed 10^6 in common materials such as silicon [142, 143] they allow significant enhancement of the light-matter effects necessary for sensing [144, 145], non-linear optics [146, 147], ultra compact lasers [148, 149] and coupling to single photon emitters [150–152]. Optimum performance can be achieved using a suspended device geometry where the upper and lower bounds of the cavity are air clad, causing the optical mode to be strongly confined to the semiconductor material. Modal confinement is then provided by arrays of etched through holes in the plane of the cavity, providing an effective air-cladding for the cavity in the lateral direction. Control of the hole tiling patterns and material thickness allows tuning of the cavity resonances [143, 153] with typical hole diameters and membrane thicknesses of $150\,nm$ and $220\,nm$ respectively to ensure a single supported optical mode in the vertical direction.

The same properties that make these devices appealing for sensing and non-linear applications also make them highly-susceptible to fabrication variations. PhCCS have

been demonstrated using deep UV lithography methods [154–156], however the highest resolution available for definition of their small feature sizes is through electron-beam lithography, where typical fabrication variances are in the few nanometre range after lithography, dry etching and wet etching steps are completed [157,158]. These processes impart stochastic noise from each technique into the final geometry of each device, that subsequently leads to variations of cavity resonant wavelength on the order of a few nanometres when targeting a $1550\,nm$ operation. For high Q-factor devices, this can be two-orders of magnitude larger than any one cavity line-width making it statistically challenging to produce spatial clusters of nominally identical devices. This limits applications to the use of a single resonator or identification of "hero" performance. However, PhCCs are beginning to be applied in cases where ensembles [159] or coupling between co-resonant cavities is required, it is essential to move beyond the limitations of the as-fabricated platform. Post fabrication tuning of devices has been demonstrated using mechanical [152, 160], cladding refractive index [161, 162], thermal [163] and electronic [164] tuning mechanisms, however routes to scaling these for dense arrays of cavities are challenging. One recent approach employed the use of laser enhanced selective oxidation of an array of cavities after initial spectral characterisation to align the resonant wavelength of 64 PhCCs to within a standard deviation of 2.5pm [159]. This actively monitored process allowed an ensemble of devices to operate on a single optical pump beam for high speed spatial light modulation.

In this chapter a physical transfer method will be presented where rather than tuning cavities in a fixed spatial arrangement, the individual devices are fabricated as mechanically separable pixels which can then be characterised, binned and physically rearranged onto a new substrate. This tackles two major challenges in the creation of arrays fabricated from single pixel devices. Firstly, the PhCC pixel devices must be detachable from their native substrate and transferred onto a receiver substrate, whilst maintaining a suspended geometry to preserve their optical characteristics. Secondly, the process of optically characterising the devices needs to be carried out within the same system as the transfer process to enable high-throughput device binning and assembly. This latter point is critical as the majority of high-accuracy transfer techniques

rely on physically shuttling samples between characterisation and micro-assembly systems. Here, by integrating both measurement and transfer assembly processes into a single system, we not only enable the deterministic selection and transfer of 119 devices in a single session, but also unlock the possibility of measuring dynamic changes in device performance during the printing process that are inaccessible using traditional serial integration and measurement methods.

Here I will show the measurement and subsequent transfer of 119 silicon PhCC devices to an array sorted by resonant wavelength. Experiments showing the repeatability of the printing will be discussed along with the specifics of the process that allowed re-printing of single devices up to 5 times before resonant wavelength shifts greater than a line width occurred. A variation of the setup from Chapter 2 is used in conjunction with a swept wavelength laser and camera based intensity detection setup to allow in-situ characterisation of PhCC devices during the printing process. Dynamic effects on the cavity resonances induced by the printing process are measured in the seconds to hours timescale, uncovering elastic effects as well as new insights that will inform future print process development.

5.2 Acknowledgements

The work demonstrated in this chapter is the result of a collaborative effort between University of Strathclyde (UoS) and the Massachusetts Institute of Technology (MIT). Fabrication of the PhCC devices was carried out by Dr. Christopher Panuski (MIT). Fabrication of the Silica frames was carried out by Zhongyi Xia (Strathclyde) for the sorted array and Dr. Eleni Margariti (Strathclyde) for the dense integration set. Final extraction of resonant wavelength and Q-factors were carried out by Dr. Jack Smith. Scanning Electron Microscope images were taken by Elise Burns.

5.3 Photonic Crystal Cavities

Two-dimensional PhCCs are passive resonator devices that utilise both total internal reflection (TIR) and photonic bandgap (PBG) effects to confine light into a small modal

volume to promote constructive interference and non-linear effects. The resonant wavelength of the cavities can be determined by a combination of the material thickness and the refractive index, a common combination is 220 nm of silicon for a target wavelength of 1550 nm corresponding to a refractive index of ≈ 3.5. The top and bottom side of the cavity are often air-clad [159, 165] to achieve a high index contrast, allowing the surfaces to act as mirrors aligned to the longitudinal axis of the trapped light.

Transverse confinement of the mode is provided by a periodic structure of holes or pillars with a lattice constant proportional to the target wavelength [143], for this work a triangular lattice of holes with a constant of 400 nm was used. This periodic structure creates a frequency range in which light cannot propagate by the PBG effect [143, 166, 167]. This allows light to be trapped transversely by incorporating a defect into the lattice structure by either removing or shifting holes allowing precise control of where the resonant device will emit from. For this work L3 cavities were used [159], where a line of 3 holes are removed from the centre of the cavity to act as the crystal defect.

The performance of these devices can be further enhanced by modifying the position and size of the holes directly surrounding the defect region, to improve group velocity dispersion (GVD) and Q-factors for target applications. A common method for implementing these changes it so use inverse design principles where a target mode geometry is defined and an iterative algorithm modifies lattice properties until it is reached [168]. These methods aren't dissimilar to Lloyd's algorithm presented in Section 4.7, except the target metric is a desired mode shape rather than an etch length. Inverse design procedures were used for these cavities to improve their Q-factor whilst keeping the mode volume small.

Integration of these devices into a deterministic array provide applications in many arrays, one of the conceptually most straightforward is that of parallel and multiplexing applications. The ratio of Q-factor to device footprint of these devices are very high, making them ideal for use as compact refractive index sensing devices and their size allows them to be packed densely together as will be discussed in Figure 5.11. This would enable parallel sensing of multiple parameters such as temperature, humidity,

air-quality etc. to happen within a compact device, such as embedded on the end of a fibre.

Another application is in the introduction of gain material to the PhCC by means of nanowires or quantum dots, allowing the PhCC device to function as a nano-laser. Again, the high modal confinement of the cavity would allow the laser to have a low pump threshold. This combined with deterministic assembly process discussed in this chapter could potentially enable hybrid mode applications, where beam steering and frequency conversion are possible in a compact form factor. Transfer printing would also prove very cost effective in this application due to it efficient use of materials.

5.4 Fabrication

5.4.1 Photonic Crystal Cavities

The PhCCs used in this work were fabricated on a native 220 nm core thickness Silicon-on-Insulator (SOI) platform, with a 2 μm buried oxide layer between the core and silicon substrate, following the design of cavities from references [159, 169]. The PhCC cavities were defined on releasable pixels, where the PhCC was surrounded by a 1 μm wide planar silicon area and a concentric trench area with a width of 1 μm. The pixel geometry is shown in Fig. 5.1. The PhCCs were suspended, and released from the substrate using a chemical HF acid etch to selectively remove the buried oxide layer. They were anchored to the surrounding core area during under-etching using a tapered section of silicon core that supported the pixels in a cantilever geometry during suspension. The transfer printing process cleaved this anchor during pick-up to release the PhCCs from their native substrate.

5.4.2 Silica Suspension Frames

The receiver substrate for the transfer print based integration of PhCCs required a geometry matching the lateral overlap dimensions of the PhCC pixels and a vertical suspension over a substrate. To match the donor geometry of silicon membranes suspended above a silicon substrate, a silicon substrate was selected as a receiver. The

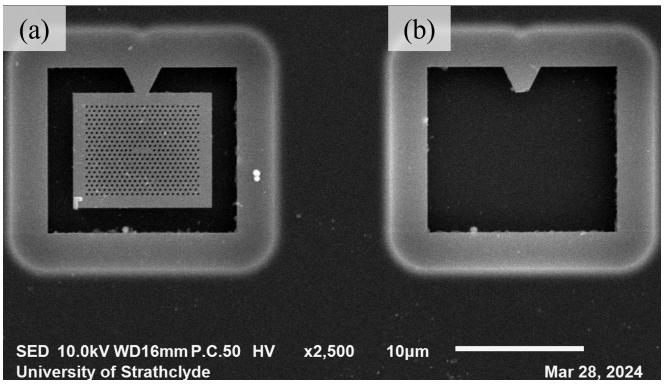

Figure 5.1: **SEM image of suspended silicon PhCC structure.** Silicon PhCC suspended on donor chip anchor tapering to 2 μm. (a) As-fabricated device. (b) Border area after device pickup on right.

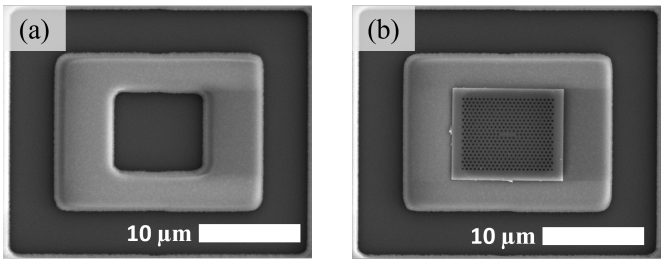

Figure 5.2: **SEM of silica receiver frames.** Receiver frames were fabricated to be complimentary in dimension to the PhCC devices. (a) Empty as-fabricated frame. (b) Silica frame with PhCC device printed on top.

suspension geometries were fabricated in silica that resemble the shape of a photo frame, a rectangular border with an empty rectangular region in the centre at a height of 1.55 μm. The silica layer was deposited onto the silicon substrate using a Plasma Enhanced Chemical Vapor Deposition (PECVD) process. The suspension frames were then defined using direct write laser lithography into a photoresist layer spin-coated onto the silica, then transferred to the silica using CHF_3 Reactive Ion Etching (RIE). Finally, the photoresist layer was removed using organic solvents and a short oxygen plasma ash. These frames enable both the top and bottom side of the PhCC to be air-clad enabling high modal confinement by increasing the refractive index contrast on both sides of the device. Analysis of the overlap of these devices is given in Section 5.8.6.

5.5 System

5.5.1 Transfer printer

The transfer printing system was a custom built instrument comprising a 6-axis motion control stage, rigidly fixed stamp holder, polymer (PDMS) stamp pick-up head, optical microscopy system and custom control and alignment software. Details of this system can be found in reference [66]. The donor and receiver samples were mounted on the motion control stage and their positions measured using the optical microscopy systems and on-chip alignment markers.

Figure 5.3: **Configuration of Transfer Printer for in-situ PhCC measurements.** Overview of transfer printer setup. (a) Inset of showing the dual column setup of microscope for print alignment and cross-polarised measurement system for device testing. (b) Wide-view showing swept laser system and PC control interface.

5.5.2 In-situ optical measurement system

The injection module from Chapter 3 was repurposed for this work, swapping out the input fibre from a 632 nm super luminescent diode (SLED) to the Agilent 8614B short-wave infrared (SWIR) swept laser via a polarisation maintaining fibre. An IR compatible microscope was constructed as an alternative to the visible column used in

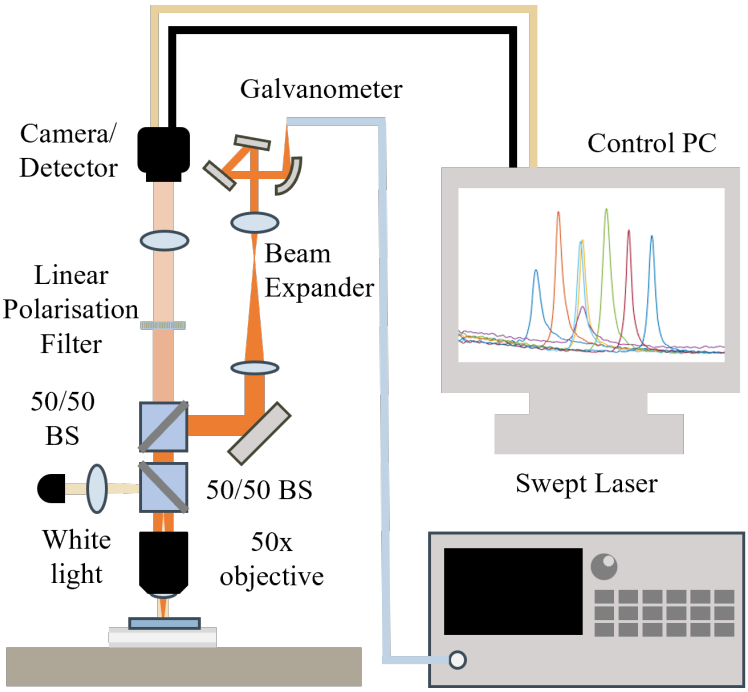

Figure 5.4: **Schematic of the optical measurement system.** The system comprises tuneable laser source and broadband white light illumination, galvo beam steering, microscope column, polarisation filter, and camera detection system.

Chapter 3 as it was deemed unsuitable for testing during the development stages of this work due to interference effects caused by the beam splitting components within the column causeing periodic signals as the swept laser system scanned across a wavelength range. This is believed to have been caused by the optical coatings being optimised for visible wavelengths.

The IR column includes a linear grid mesh polariser aligned at a 45° angle to the edge of the PhCC donor chip and silica frame receiver chip providing 20 dB of extinction. The injection fibre is aligned such that its polarisation is at an angle of −45° to the cavity and 90° to the polarising filter. This allows the specular background from light incident on the substrate to be suppressed significantly. Light that couples with the PhCC becomes aligned in polarisation to the cavity, such that when it is reflected back through the filter, the reduction in intensity is half that of the background noise. This results in overall less light being measured during the scanning process, but provides a large improvement in the signal-to-noise ratio (SNR), making it easier to

detect resonances. An InGaAs array used for detection is housed inside a Lucid Vision Triton Global Shutter camera, the bandgap of the sensor has been optimised to extend the sensitivity down to visible wavelengths, facilitating a broad mesurement range of 400 - 1700 nm. This allows co-alignment of the wide field illuminated device structures to the injected tuneable IR beam using the same sensor. The laser system provided a controllable trigger pulse rate based on a set wavelength step over a continuous sweep. This would allow the camera to consistently acquire a frame at the same points in every sweep. Similar experimental setups have been demonstrated [170] where light was collected in transmission and a pulse laser source used instead. The setup described hear more closely resembles that shown in [171] with some additional convenience features to aid in its integration within a transfer print system.

5.6 Measurements

5.6.1 Optical Spectra and Measurement Method

Spectral measurements of PhCCs were performed using a swept tunable laser (Agilent 8164A) in continuous sweep mode over a 10 nm range around 1550 nm at 0.5 nm/s with a laser linewidth of 100kHz. The reflected signal was captured by an InGaAs camera at 833.3 fps triggered by the laser, providing a measurement resolution of 0.6 pm limited by the max frame rate of the camera. The camera gain was adjusted to prevent saturation, and a fixed region of interest (ROI) was used to sum the reflected intensity across frames. This ROI remained the same across all measurements in this work.

For array measurements, the laser scanned over 10 nm in 20 s, enabling analysis of cavity resonances. Peak search and resonance fitting routines determined cavity wavelength and Q-factor at the end of each scan. For dynamic measurements on pre-characterized devices, the scan range was reduced to 2.5 nm, Shortening the measurement time to 5 s and total analysis time to under 10 s. Higher Q-factor cavities could be analysed with improved resolution by reducing the laser sweep speed.

5.6.2 Extraction of resonant wavelength and cavity Q-factor

The resonance wavelength and linewidth were evaluated by fitting the measured reflectivity spectra data around a resonance to an analytical model. Following common practice in literature, we have used a Fano resonance model for fitting our photonic crystal cavity spectra [171–174]. After removing the low frequency background modulation from the signal, we fit the reflected intensity, $I(\lambda)$, with the Fano equation [174] shown in Eq.[5.1]. The fitting was carried out using a nonlinear regression method in MATLAB, fitting to the analytical function Eq. (5.1).

$$I(\lambda) = A + B\frac{(cot(\delta) + 2(\lambda - \lambda_R)/\gamma)^2}{1 + (2(\lambda - \lambda_R)/\gamma)^2} \tag{5.1}$$

Here, λ_R is the resonant wavelength, γ is the resonance width, and A and B are constants relating to the background and peak height respectively. The parameter controlling the deviation from Lorentzian lineshape is δ, which refers to the phase shift from the coupling of a discrete resonant mode to a continuum band of states [174]. It is related to the Fano parameter, q, through $q = cot\delta$, and it can be shown that for $q \to 0$ or $q \to \pm\infty$ Lorentzian lineshapes are recovered. The Q factors are measured as $Q = \lambda_R/\gamma$.

5.7 Printing Process

The general method used to transfer print objects using a polymeric stamp is well covered in literature [51,175–177] and was also discussed in detail in an earlier chapter. Velocity control is shown to play a key role in terms of controlling the relative adhesion of the stamp to devices during the print process [67]. For devices where the material thickness is greater than $1\,\mu m$ or with high stiffness, it is possible to use a variation of the stamp geometry that include protrusions that can dynamically relax during the printing process resulting in a dynamic change of contact area of a picked device [178]. However due to the small device footprint and material thickness of $220\,nm$, geometric variations of the stamp geometry isn't suitable for the transfer of these PhCC devices and instead require the use of a flat stamp surface to ensure minimal deformation during

transfer [179]. It has been shown that control of the Polydimethylsiloxane (PDMS) composition can be used to tune the dynamic range of surface adhesion to promote transfer in the direction of donor to receiver [179].

In this work, a PDMS composition of 10:1 (monomer:curing agent) mixture was used, and is the recommended ratio from the manufacturer. Lower concentrations of monomer result in a more rigid and less tacky stamp whereas higher concentrations result in a more adhesive stamp. The mould for the stamp was created by etching a into a Silicon on insulator wafer (SOI) to create the 10 $\mu m \times$ 30 μm wide portion of the stamp. The base of the stamp was patterned using SU-8 polymer from Kayaku.

The anchor geometry of PhCCs tapered to a dimension of 2 μm at the membrane edge and required the flat face of the stamp to fully cover the surface of the cavity device in order to apply enough force to break it. Due to the limited contact area of the silica receiver frames, the force of the device to frame adhesion was insufficient to overcome the device to stamp adhesion when using traditional printing methods. Introducing a lateral shear into the print process allowed the use of friction between the frame and the device to force the cavity off the stamp surface. This resulted in two issues to overcome, alignment to the silica frame was difficult to achieve and the additional release forces had the potential to plastically deform the cavity resulting in detuning of its resonant wavelength (discussed later). To combat the former, a print stage was introduced where the cavity was printed onto an intermediate frame before printing on the target location. This allowed the device to be re-picked from the intermediate frame where approximately only a quarter of the device was in contact with the stamp. This, in combination with slow release speeds, allowed the device to be aligned to the final silica frame with negligible misalignment observed. The latter issue of plastic deformation was handled by introducing a characterisation step whilst the device was on the intermediate frame, and to determine its position in the sorted set by this resonance. A detailed view of the whole print process is shown in Fig. 5.5 along with microscope images of the PhCC cavity on the surface of the stamp.

For the initial release from the donor chip, The flat stamp surface was brought into contact with the PhCC surface, ensuring no stamp contact with the tether area. Once

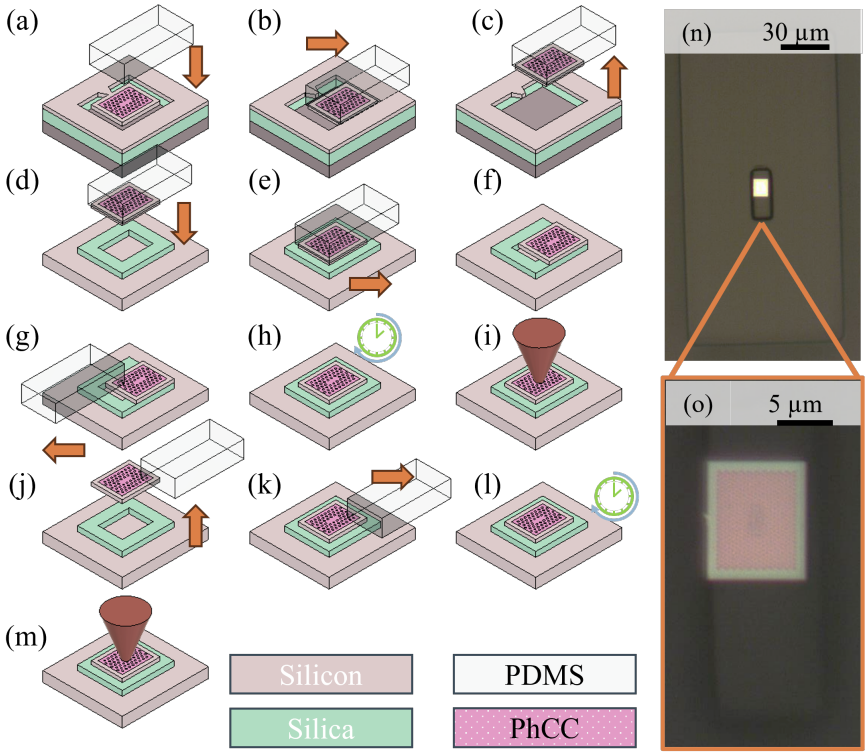

Figure 5.5: μ **-transfer print process for suspended photonic crystal cavities.** (a) The stamp is aligned to the donor device. (b) A lateral motion at a velocity of $8000\mu ms^{-1}$ is used to break the device anchor. (c) The device is removed from the donor chip. (d) The picked device is aligned to the intermediate silica frame on the receiver. (e) Device is released onto the receiver frame using a combined sheer motion at a velocity of $0.5\mu ms^{-1}$. (f) The stamp is removed from the device to ensure device is printed. (g) The stamp comes into partial contact to provide a sheer at $0.5\mu ms^{-1}$ to align the cavity to the frame. (h) Cavity is left for several hours to allow detuning effects to subside. (i) Swept laser system characterises device on to determine its new position (j) Device is picked with only a quarter in contact with the stamp. (k) Device is aligned to final frame and released using a sheer at $0.05\mu ms^{-1}$ to maintain alignment. (l) Cavity is left for several hours to allow detuning effects to subside. (m) Cavity resonance is reverified with a final measurement. (n-o) Microscope view of transfer print stamp with printed device.

in contact a lateral shear motion of $\approx 1\,\mu m$ was applied to fracture the tether at a velocity of $\approx 8000\,\mu m s^{-1}$, Fig. 5.5(a). The PhCC on the stamp is then aligned to the receiver chip suspension frame, centring the PhCC on the air void of the frame. The PhCC is brought into contact with the silica suspension frame, then released from the stamp surface using a combined shear and vertical motion at a velocity of $\approx 0.05 \mu m s^{-1}$. This is then repeated for the subsequent reprinting of the cavities, exchanging the initial high speed lateral sheer step for a lower velocity vertical pickup with a reduced contact area. This process allowed release of the PhCC into its target position with a yield of 100% for the 448 prints carried out for this work, i.e. 238 prints of the main cavity set, 90 prints of the repeatability tests, and 120 prints for the dense integration set. The tapered anchor successfully cleaved at the edge of the PhCC with no detectable damage to the cavity for all 249 devices presented in this work. Only one during the beginning of this study became stuck on the base of the stamp, making it irrecoverable, resulting in an overall yield of 99.78% for the print integration process.

5.8 Results

5.8.1 Spatial ordering of PhCC array by resonant wavelength

A schematic of the transfer print system with optical measurement module is presented in Figure 5.6. The transfer printing system comprises an optical microscope column, fixed transfer stamp holder and a high-accuracy 6-axis translation stage with Peltier coolers, on which the donor and receiver samples are mounted [66]. The Peltier elements are held a few degrees below the cleanroom laboratory temperature at a constant 19.6^{o}C with closed loop feedback to ensure stable operation of the PhCCs. In addition to the wide-field optical imaging function of the microscope column, the system also incorporates an optical injection line for the swept-wavelength tuneable laser characterisation system. The signal reflected from a targeted PhCC is coupled back through the microscope objective to a camera system for assessment of the spatial mode and measurement of the reflectivity spectrum under swept wavelength operation.

Figure 5.7 shows a reflectivity spectrum measurement from a representative PhCC

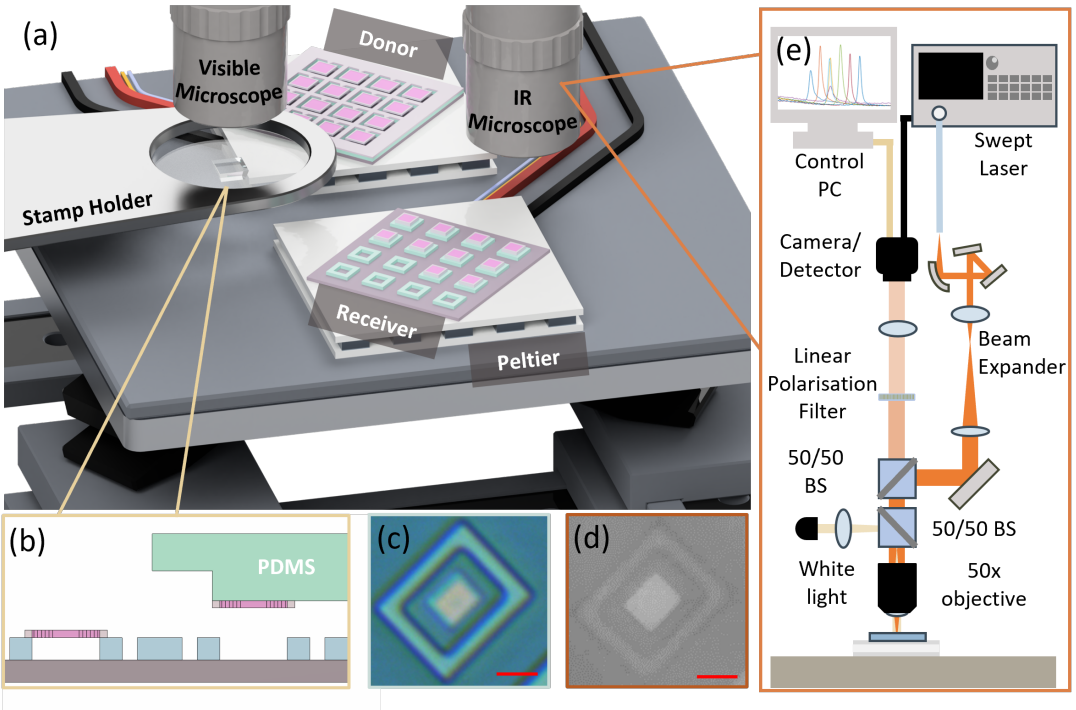

Figure 5.6: **Accurate transfer printing system with in-situ reflectivity spectrum measurement capability.** (a) Schematic transfer printing system and optical measurement rig incorporating high-accuracy 6-axis stage, fixed stamp holder, Peltier mounted donor and receiver samples and optical microscope objective lenses. (b) Schematic of the pixel printing process using a PDMS stamp. (c) and (d) show images of a printed PhCC pixel in the visible and IR systems respectively. (e) Schematic detail of the optical injection and measurement system embedded in the transfer printing tool.

device captured using the in-situ scanning laser measurement system in the transfer print tool. The central resonant wavelength, linewidth and Q-factor of the resonator can be extracted from this swept laser measurement in real-time, with single pass sweeps taking only a few seconds to complete. For the PhCCs' in this work, the resonant wavelengths were in a range around $\sim 1551\,\text{nm}$, with cavity linewidths of $\sim 15\,\text{pm}$ and Q-factors in the 10^5 range.

To enable spatial ordering of an as-fabricated PhCC array, 120 devices were first measured on their native substrate, and the resultant map of PhCC pixel resonant wavelengths is shown in Figure 5.8(a). As expected, the measured cavity wavelengths span across a range of a few nanometres in wavelength, corresponding to the variations

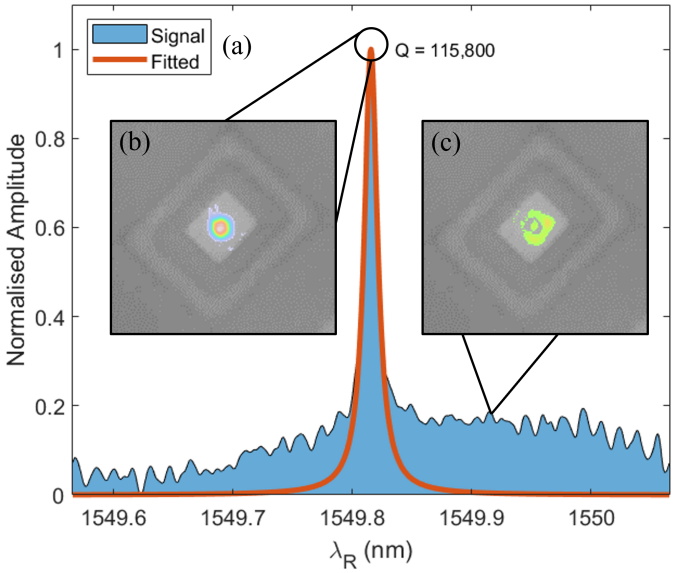

Figure 5.7: **Spectral measurement of PhCC in the transfer system.** (a) Measured reflectivity spectrum from a PhCC captured using the in-situ measurement system. The PhCC is printed on a receiver substrate silica suspension frame. Insets show the spatial mode images captured by the InGaAs camera at two points in the tuneable wavelength sweep corresponding to on-resonance (b) and off-resonance (c) conditions.

in cavity geometry induced by nano-fabrication geometry tolerances. The blank spots in the figure correspond to PhCCs where no spectral measurements could be obtained, likely due to partial collapse of the pixels onto the exposed substrate during the undercut process. One pixel could not be released from the donor chip, so all further results correspond to the remaining 119 pixels that could be transferred. The resonant wavelengths are distributed across the array without any clear spatial pattern, as shown in Figure 5.8(a). The devices were then numerically sorted by resonant wavelength and printed onto receiver substrate following the spectral ordering.

Figure 5.8(b) shows a map of the printed pixels' resonant wavelengths on a first receiver substrate. From the first print it is obvious that the spectral ordering has been frustrated and again the cavities form a disordered array, although all transferred pixels are now visible, recovering the previously unmeasureable cases from the donor substrate. The measurements on receiver 1 were then used to create an ordered array, through selective placement during an additional transfer step onto a second receiver,

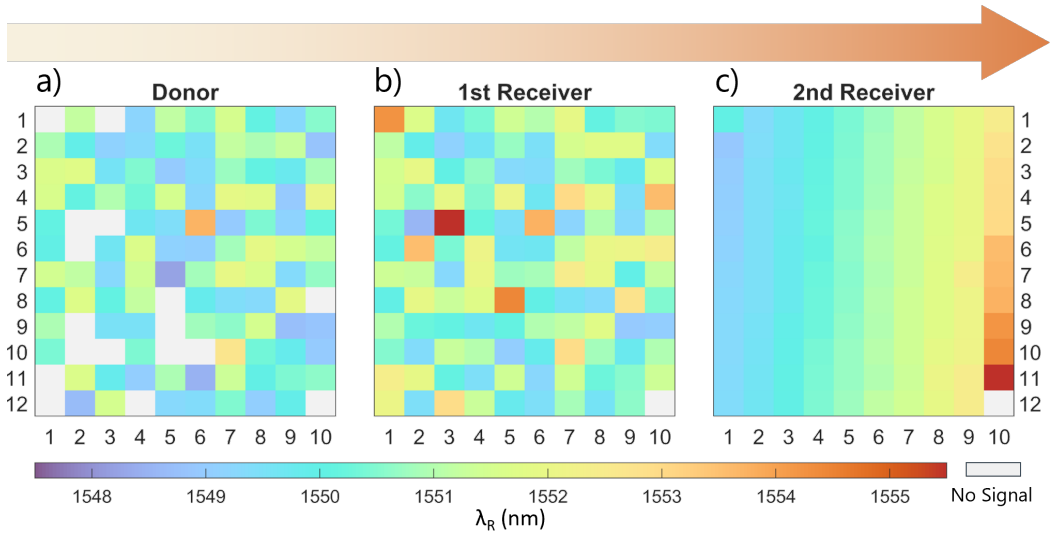

Figure 5.8: **Spatial ordering of PhCC arrays by resonant wavelength.** Measured resonant wavelengths of the PhCCs on (a) donor substrate, (b) 1st receiver and (c) 2nd receiver substrate.

the measured results of which are presented in Figure 5.8(c).The wavelength ordering was preserved faithfully in this transfer, indicating that the process of cleaving the silicon tethers during the first print likely induced a plastic shift in the cavity resonant wavelengths. Figure 5.9(a) and (b) show the wavelength shifts of individual PhCCs for the first and second prints, with a clear improvement in the second print case. For the first print, the mean wavelength shift of $\pm 0.426\,\text{nm}$ and standard deviation across the array of $\pm 0.438\,\text{nm}$, clearly shows the effect of the release from the donor substrate on the cavities where the spectral ordering has been frustrated by the initial release process. The second print however shows a mean wavelength shift of $\pm 0.025\,\text{nm}$ and standard deviation of $\pm 0.139\,\text{nm}$, demonstrating stable performance of the PhCCs before and after. The two outlier values of wavelength shift in the second print array correspond to two cases where mechanical effects during printing caused larger deviations of the resonant wavelength. Device 1 was printed as a calibration step for the force being applied during the print release stage and a higher than necessary value appeared to cause a residual plastic shift in resonant wavelength. The second outlier device was accidentally printed onto a rigid area of the sample before being moved to its target receiver location, again exhibiting a larger deviation of the resonant wave-

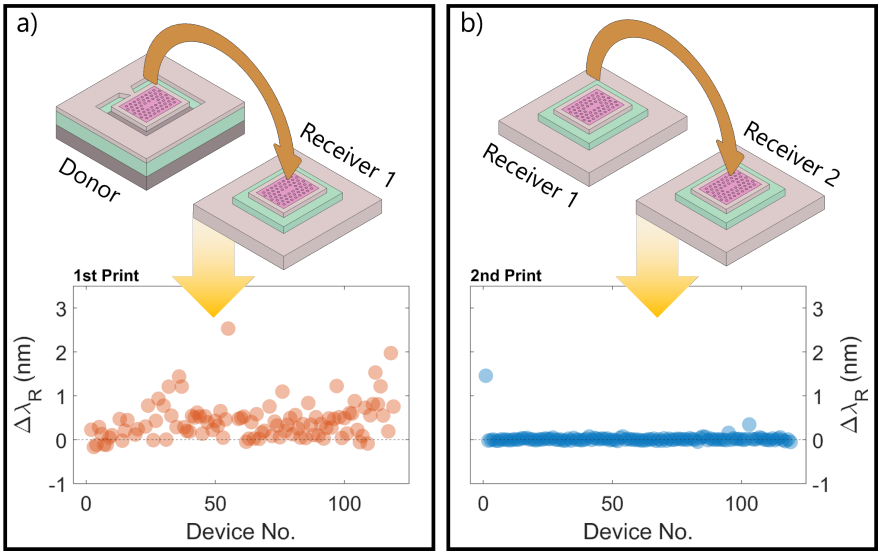

Figure 5.9: **Printing induced resonant wavelength shift.** Measured resonant wavelength shifts of individual PhCCs after (a) 1st print, and (b) 2nd print

length. Removing these outliers in the second print gives mean and standard deviation wavelength shifts of ± 0.007 nm and ± 0.021 nm respectively. This consistency in performance is comparable an order of magnitude larger than what has been achieved with post-fabrication tuning [180]. However, this could be improved with a larger set of donor devices and can occur during the heterogenous integration stage without additional processing. By spatially ordering the devices, local clusters of PhCCs were identified with resonant wavelength spread within a cavity linewidth, highlighting the potential of this technique when used with a higher number of donor devices. Other potential devices that could benefit from this type of integration include nanowires [63] and quantum dot devices [181].

5.8.2 Spatial clusters of cavity resonances within ordered arrays

The ordered arrays of devices maintained the overall standard deviation of resonant wavelength, λ_R, from the as-fabricated PhCC devices. The ordering allows for local spatial clusters of devices with closely spaced resonant wavelengths to be assessed. The average cavity linewidth of ~ 0.015 nm was taken as a first approximation of the maximum deviation between individual cavity resonant wavelengths that would allow

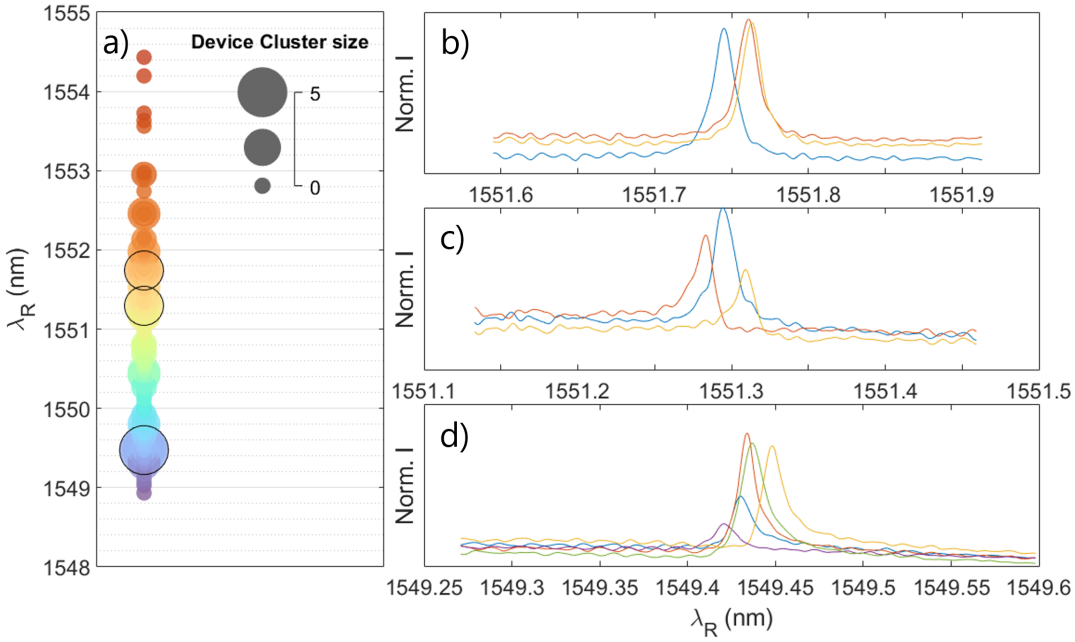

Figure 5.10: **Cavity Clustering.** (a) A bubble chart showing resonant wavelength ordered on the y-axis, spatial position by colour and number of devices within a standard deviation of 0.015 nm by bubble size. (b-d) Selected groupings of devices outlined in black in (a) are shown as reflectivity spectra to show the spectral overlap between devices.

them to interact with a single narrow linewidth laser source. Fig. 5.10 (a) shows the distribution of PhCC clusters across the range of measured resonant wavelengths. The bubble size is related to the number of devices with resonant wavelengths within the average cavity linewidth from one another. There are a number of groupings on the order of 5-6 cavities, showing that even without post-fabrication tuning device selection and spatial binning can be achieved even within a set of only 119 devices. Fig. 5.10(b-d) shows examples of cavity resonance clusters around a wavelength of $1550nm$.

The wavelength ordered set of PhCCs presented above was printed with minimum pitch of $50\,\mu m$ in both the x and y directions. In order to demonstrate the potential of this integration method for producing densely packed arrays, we transferred an additional 120 devices onto an 8×15 spatial array of support frames with a pitch of 18 and $16\,\mu m$ in the x and y directions resulting in a minimum edge to edge separation of $7\,\mu m$ in both directions, as shown in Fig. 5.11.

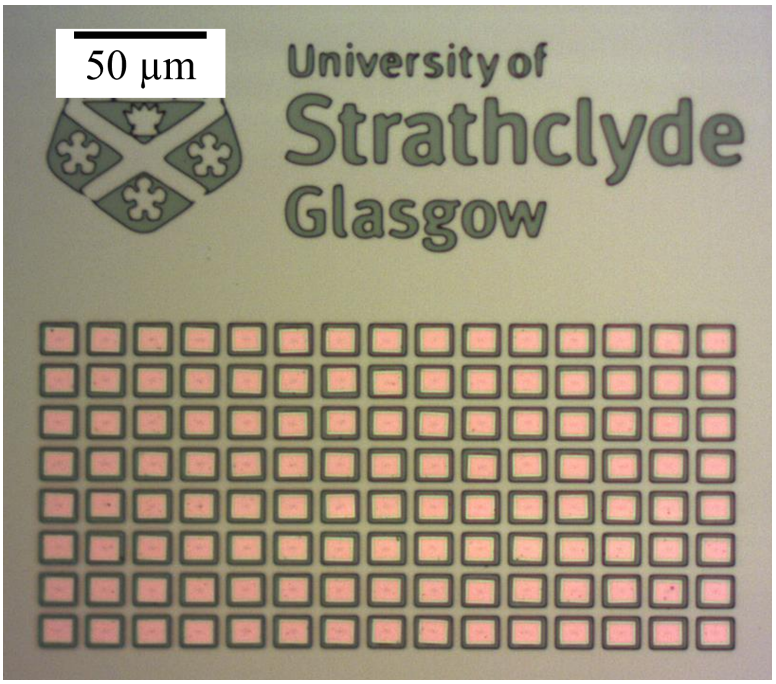

Figure 5.11: **Densely printed array.** Optical microscopy image of an an array of 120 PhCC devices printed with edge to edge spacing of 7 μm in both directions.)

5.8.3 Dynamic cavity response measured in-situ

As detailed in the previous section, the release of the silicon PhCC pixels from their native substrate results in a permanent shift in their cavity resonant wavelength. Since the spectral measurements of the PhCCs are carried out in-situ in the transfer printing system, dynamic effects can be monitored. Limited only by the timescale of the swept laser spectral measurement system and the short travel movements needed to obtain optical alignment. The inset to Fig. 5.12 shows the time varying cavity reflectivity spectrum for a single PhCC cavity over a few tens of seconds just after the initial printing, showing a clear shift of the spectrum with time. The main decay curve presented in Fig. 5.12 shows the results of spectral measurements of 2 different PhCCs on the same substrate measured concurrently over the course of 200 minutes, plotting the measured resonant wavelength shift relative to the pre-printed steady-state value. The printing process shows a clear red-shift in cavity resonant wavelength immediately after release onto the receiver substrate, followed by a relaxation back towards the

steady state value on a timescale of around 200 minutes.

This decay could be the result of several factors, but the exact source is unknown currently. The first theory is that the relaxations are dependant on the mechanical properties of the silicon material, such that larger of the exponential terms is resultant of a mechanical stretching in the XY plane of the cavity, and the smaller term corresponds to a "sagging" of the cavity over suspension frame, providing a Z-component to the detuning. A second theory is that their is a combination of mechanical effects combined with a relative humidity change at the surface of the cavity due to coming into contact with the PDMS stamp head. The water deposits on the surface then evaporate off returning the cavity resonance to its original value.

The results of the multiple print cycles show that steady-state cavity resonances are preserved for up to 5 cycles, demonstrating that the print process does not leave measurable material deposits on the cavity, which would induce a red-shift of the resonance wavelength due to increasing local cladding refractive index. The dynamic relaxation of resonant wavelengths rather suggests a strain based effect induced by the contact printing that then relaxes as the free-standing PhCCs are left on the suspension frames with no restraining force beyond the local forces between their surfaces. Furthermore, the relaxation curves can be fitted to a double exponential function, with two characteristic relaxation time constants originating from potentially distinct physical processes.

5.8.4 Multiprinting

An additional set of 10 PhCCs were selected from the donor chip, with resonances around $1550\,nm$ to test the effects of multiple print cycles on the cavity response. For each device resonant wavelength and Q-factor were measured prior to each print. Two print cycles were carried out each day over a period of 5 days, based on Fig. 5.12 a minimum of 5 hours was left between a print cycle and measurement to ensure the dynamic detuning effects would be negligible. In Fig. 5.13 the distribution of wavelengths for the 10 devices is shown in blue for each print cycle, and the relative wavelength shift is shown in red. All print cycles are numbered after the initial "0" from the donor to receiver to avoid inclusion of plastic shift effects. It can be seen that

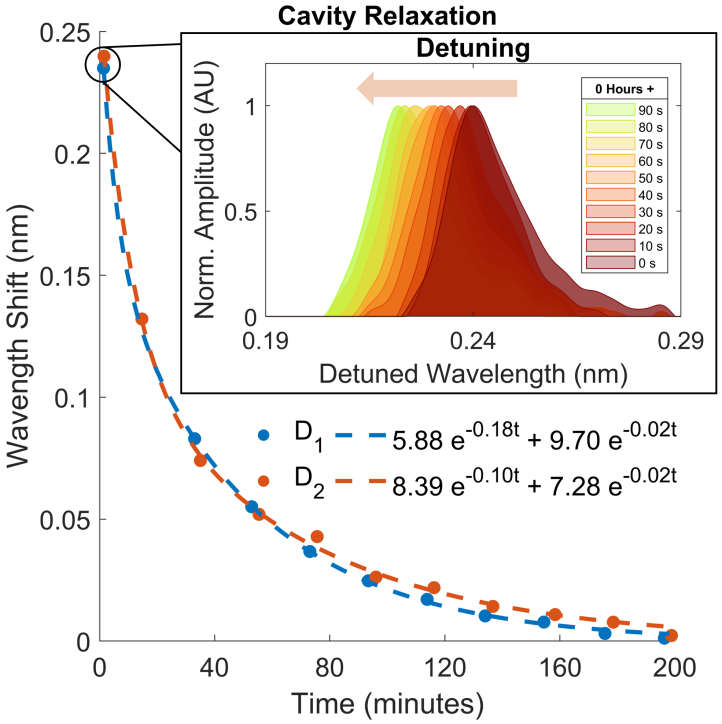

Figure 5.12: **Dynamic effects of printing on the cavity optical response.** Cavity resonance wavelength for 2 separate PhCCs measured over a 200 minute period after initial printing. The inset shows the fast relaxation of the cavity resonance just after printing, as captured by the in-situ measurement and the stable steady state response after relaxation.

for up to 5 print cycles that negligible shifts in wavelength are present. For >5 print cycles the stability of the device wavelength degrades becoming comparable with the as-fabricated array. This detuning is could be caused by effects of surface contamination from the environment or the stamp itself.

5.8.5 Cavity Q-factors effects

When observing the Q-factors of each device the measured Q factors remained within the range of 10^5 with individual devices showing variations in the 10^4 range. The full set of 10 devices remain within a consistent operating range and even recover some performance during 6-8th print cycles indicating cumulative damage to the cavity is an unlikely source to the cavity detuning. An increase in device contamination could still be possible if the Q-factor increase is indicative of the stamp being able to clean

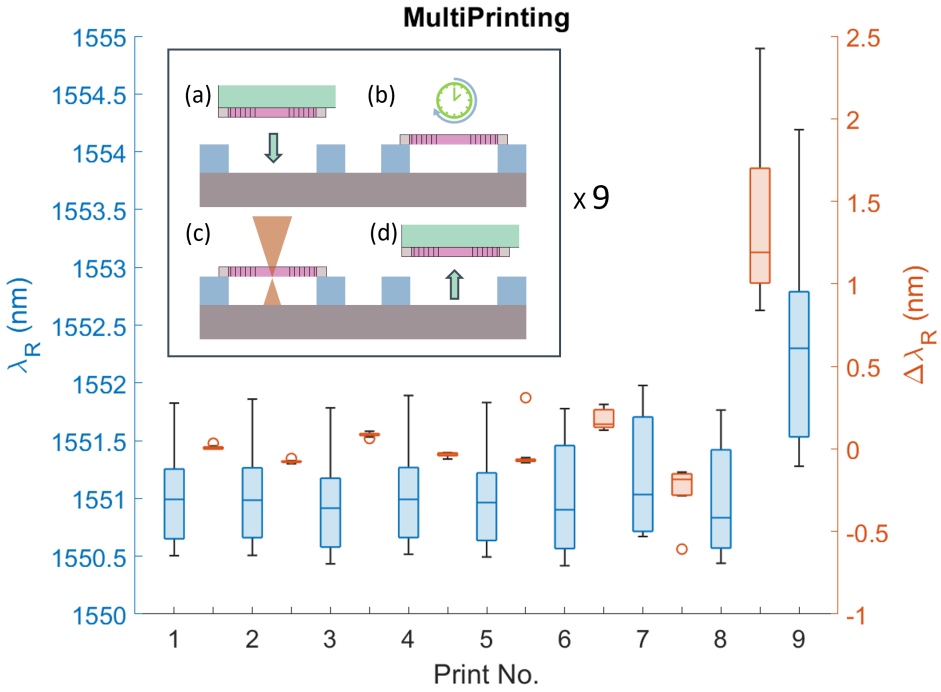

Figure 5.13: **Repeated print cycles.** Measured cavity wavelength sets after each printing cycle for a set of 10 PhCC devices, showing absolute cavity resonant wavelength (blue) and relative resonance shift between each print location (red). (Inset illustrates the print and measurement cycle.)

devices under certain conditions to regain performance.

A third potential factor is the alignment of the cavities to the silica frames, there is a small margin of tolerance designed into the two structures that allow the cavity to be misaligned slightly. It is possible this margin is not large enough to prevent the holes of the PhCC from overlapping the receiver frame structure, reducing the device performance by modifying the refractive index contrast.

5.8.6 Contact area measurements

To quantify the extent of the spatial overlap between the printed PhCC devices and support frames, a frame was imaged in a scanning electron microscope before and after printing of the PhCC, as shown in Fig. 5.15. The internal dimensions of the support frame were measured as $8.5 \times 7.5\,\mu m$ prior to the PhCC printing. The PhCC device was measured with external dimensions of $11 \times 9\,\mu m$, and by image overlap analysis of

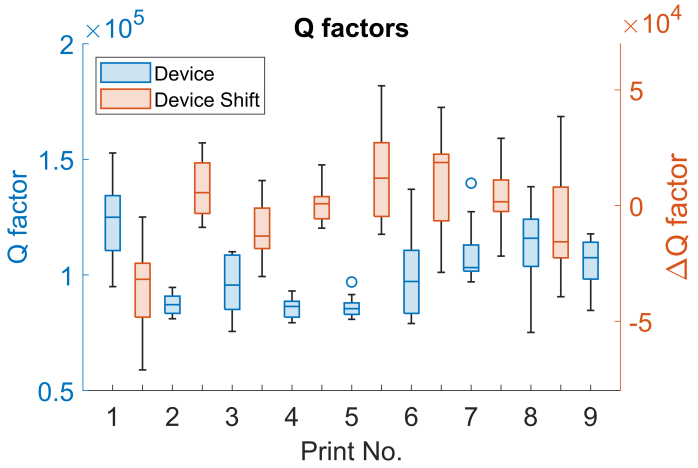

Figure 5.14: **Q-factor variation as a function of repeated print cycle** Q-factor variation as a function of repeated print cycle for a set of 10 PhCC devices. Absolute Q-factor value for the 10 device set is presented along with the device specific Q-factor variation associated with each print cycle. the box plots indicate median value (middle line), 25th, 75th percentile (box) and 5th and 95th percentile (whiskers) as well as outliers (single points).

the pre- and post-printing images the mean overlap lengths between PhCC and support frame were $1.21, 1.24, 0.49, 1.05\,\mu m$ for the left, right, top and bottom edges respectively resulting in an average overlap of $1.00\mu m$. The edge detection was performed within Python using standard techniques within the OpenCV package, using the following process. A Gaussian blur was used to de-noise the image, following a morphological close operation to remove pixel islands that were unattached to the target structures. Finally, an adaptive threshold was used to binarize the image. An averaged line profile was taken for each edge of the imaged structures, in both the horizontal and vertical directions. This was then passed through a peak detection algorithm from the SciPy library to find the locations of each edge with the errors taken as the FWHM of each detected edge.

An average overlap of $1\,\mu m$ was measured for the printed device. The device is shown to be centred well in the horizontal direction as the difference in the left to right overlap is only $30\,nm$ whereas a skew is observed in the vertical direction with an overlap difference of $560\,nm$. The internal geometry of the frame was intended to be $9 \times 7\mu m$ to result in an equal amount of overlap for both the horizontal and vertical directions.

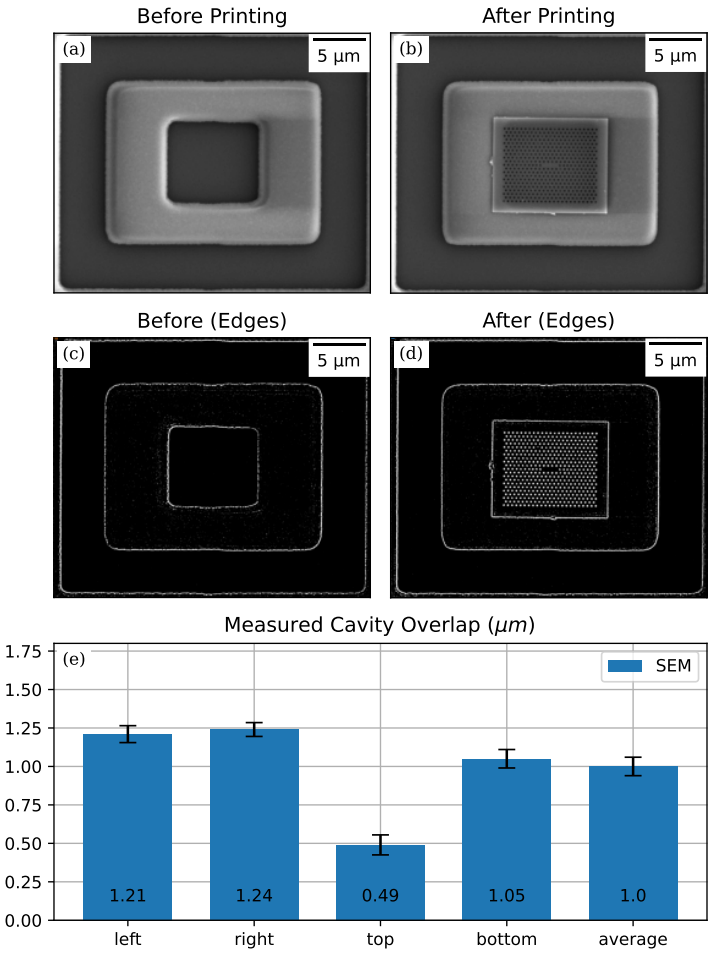

Figure 5.15: **SEM analysis of Cavity Overlap** (a-b) SEM images of silica support frame before and after printing of PhCC device. (c-d) Post edge detection process for before and after printing. (e) Measured overlap of each cavity edge, error bars represents the combined FWHMs of the average line profile of (c) and (d).

However, it is apparent that a distortion of the internal geometries is present as the measured geometry is $8.5 \times 7.5 \mu m$ The source of this error could be multiple effects resist exposure and etching processes. This particular sample was fabricated using a direct-write lithography tool from Heidelberg instruments that has been known to have calibrations issue following its installation during the course of this project. However any comment on this is purely speculative. The optical resolution of the microscope when operating in high resolution mode is 900 lp/mm which corresponds to being able to resolve one line pair every 1.1 μm. This combined with the inaccuracy in the final

frame geometry pushes the print tolerances of the final devices to the upper limit of what the transfer print system is currently capable of. If this study were to be reattempted, it would be beneficial to generate a hard mask from a industry supplier to be used with a mask aligner system to mitigate inconsistencies between pattern exposures. A larger border area around the crystal cavities would allow the internal window of the frame to be larger also, resulting in a larger print tolerance to ease the print requirements. The lp/mm could also be increased by improving the vision system, such as a higher quality camera sensor or high maginification objective lens. This should also improve the print accuracy of the printer as the resolution of the motion system is two-orders of magnitude larger than that of the microscope.

5.9 Discussion

The integration of spectral measurement and transfer print integration into a single system not only benefits the throughput, yield and selectivity of the device integration process, but has also enabled measurement of transient effects in device performance that were not possible in separate integration and measurement systems. Furthermore, the integration of high quality factor, air clad, photonic crystal cavities provides an extremely sensitive optical measurement tool for observing these transient effects. As noted above, there are two measurable effects of the PhCC integration process on the cavity resonances. The first is a permanent shift in the cavity resonant wavelength during the release from the donor substrate, and the second is a transient resonant wavelength shift during subsequent prints that relaxes to a consistent, steady-state value. Although full exploration of the physical mechanisms underlying these effects is beyond the scope of this work, their magnitude and potential sources can be outlined. A shift of PhCC resonant wavelength measured after a print cycle can be due to change of cavity effective refractive index, or mechanical deformation of the cavity. In this work we have used nominally identical L3 photonic crystal cavities that can have measured resonant wavelengths with a standard deviation in the order of 1 nm (around the 1550 nm region). In reference [143] the authors show that a wavelength

dispersion of this order corresponds to a randomised variation in hole radius and position of $\approx 0.0014a$, where a is the lattice constant of the photonic crystal. This in turn would correspond to a variation in real space of $\approx 0.56\,\text{nm}$ (for a lattice constant of 400 nm) for our devices. Thus, in accordance with perturbation theory [182], a uniform expansion of the PhCC lattice by 0.56 nm would lead to a redshift of cavity wavelength greater than 1 nm. Similarly, given the near-unity energy confinement of our L3 cavity modes in silicon, perturbation theory also dictates that a 1 nm redshift in wavelength corresponds to a change in effective index of a factor of ≈ 0.0014, assuming no mechanical deformation of the cavity. In reference [159] oxidation of silicon PhCC's show resonant wavelength blueshifts of a few nanometres, through oxide formation of nanometric scales. Thus, effective refractive index changes of this order correspond to nanometric material refractive index changes. We are unable to measure any deposition of stamp material on the cavity via direct imaging (optical or electron beam) that would show such nanometric depositions. In the case of the transient resonance shifts from one suspended position to another, the cavity response relaxes to a consistent steady state, within a linewidth of the original resonance. This suggests a small stress is induced in the cavity cause by the print process, that then relaxes. This relaxation can occur even during the surface to surface contact between the membrane and support structures.

The sub-nanometre wavelength shifts of all cavity steady-state resonances observed after 5 sequential printing cycles demonstrates the ability to preserve all physical properties of the device (lattice constant, refractive index, etc.) to better than one part in 1000 making suitable for the assembly of spatial light modulators. The preservation of resonant cavity wavelength allows for the selection of specific cavities to be integrated into pre-defined spatial locations, overcoming the existing variance in nominally identical devices as-fabricated on their native substrate. This deterministic post-measurement selection of cavities will enable single device selection for integration into photonic integrated circuits, or on fibre tips, as high-quality factor filters and non-linear resonators with absolute control over target wavelength. Importantly, the spatial ordering of these devices enables construction of cavity arrays with well-defined wavelength

characteristics. For example, cavity arrays can be designed with wavelength gradients across the array to enable passive beam steering at high speeds [183]. Uniform arrays can also be assembled for applications as spatial light modulators [159]. In this case the yield of cavity responses within the linewidth scale is important and is related to the variance of cavity wavelength from nanofabrication tolerances. In this work we show that groupings of ≈ 5 PhCCs can be extracted within the range of a linewidth from an initial set of 120 devices. Full details are presented in the supplementary material. This gives a nominal down selection factor of ≈ 0.042, meaning that for a uniform 10x10 cavity array, an initial donor set of around 2380 devices is needed. When fabricating donor arrays at large scale, multiple uniform arrays can be assembled from a single fabrication run.

5.10 Conclusion

I have demonstrated a post-fabrication integration method that allows the spectral measurement, binning and spatial arrangement of high Q-factor Photonic Crystal Cavity (PhCC) devices into ordered arrays, with precision beyond what is achievable in as-fabricated device arrays. The transfer printing integration of 119 PhCC pixels demonstrated handling of devices with dimensions in the few micrometre range, onto suspension frames on receiver substrates with physical contact limited to 1 μm in overlap. SEM imaging was used to characterise the physical overlap of the PhCCs and support frames. The printing process preserved cavity resonant wavelengths within their linewidth range after a first permanent shift induced by the print release from the donor substrate. Furthermore, the printing process preserved cavity performance over multiple cycles, allowing for reconfiguration or rework of samples using this method. The in-situ optical measurement of cavities enabled study of the printing dynamics in the seconds to hours timescale, exhibiting elastic relaxation effects in the cavities after printing that would not have been easily measurable in standard integration and measurement system combinations. The ability to directly measure micron scale device response and subsequently integrate large numbers of devices onto host chips breaks

the dependence on fabrication limited integrated optical systems and paves the way for future, high performance optical systems-on-a-chip.

Chapter 6

Conclusion

6.1 Conclusion

Presented in this thesis were the efforts made to mature transfer printing as a integration platform. Having already proven itself as capable method for heterogenous material integration [51, 63, 66] and as a technique that can enable high performance photonic circuitry to the point of adoption into foundry ecosystems. This highlights the importance to mature the technology as a whole, moving away from demonstrations of "hero" devices or one-time fabrication runs. To a point where it can produce a consistent output on a daily basis.

To enable this, the aspects of what sets apart integrated circuits (ICs) and a photonic integrated circuits (PICs) were looked at. In particular, the mechanisms that allow mass integration of electronics via PnP tools that are not present in transfer print systems. To combat this, the functional principle behind the operation of PICs was analysed and evaluated to determine how these limitations could be overcome. One such solution was to enable in-situ testing of PICs to enable alignment free assembly of high performant circuits.

Chapter 2 outlines the construction of a vertical optical injection system integrated into a custom-built transfer printer. The system is capable of optically coupling into photonic structures during transfer print integration. The design decisions, from the coatings of the optics and the electrical hardware to the software implementation were

all discussed in detail highlighting technical priorities in each. 3D printing techniques were introduced and their role in the rapid development such systems.

A technical demonstration on the benefits of such a system was provided by demonstration of alignment of a GaN μ-lens to a single core fibre. Two alignment mechanisms were provided for comparison. First where the fibre was illuminated with a red wavelength light source such that the position of the core was visible. This allowed active alignment of the lens by monitoring the spot shape as the lens approached the surface of the fibre facet. This is equivalent to printing onto other vertical emitter structures found commonly in PIC systems. The second acted as a representation of aligning to a detector device. The opposing end of the fibre was connected to a photodetector and the red light source was then connected to the vertical injection setup. By implementation of a raster scan of the light across the fibre surface a voltage map was constructed, the central peak of which corresponds to the centre of the fibre core. Both instances resulted in good alignment to the fibre core within $\pm 0.5\,\mu m$ of the core position.

Several technical demonstrations where also given, such as active monitoring of coupling conditions during the print process. Coupling light into state of the art greyscale patterned on-chip mirror couplers, as well as industry standard grating couplers with off-axis monitoring. These three provide a supporting toolset for the future of optically monitored transfer print integration. Height mapping of PICs was also explored utilising pre-existing features of the PDMS stamp, opening avenues for integrated metrology methods as another back-end process integrated into the transfer printer. This system will be invaluable in the development of future transfer print technology and techniques, allowing tailoring of processes towards photonic circuitry.

Chapter 3 presented work on the μ-fabrication of suspended membrane devices, in particular efforts made towards standardising the fabrication process. Challenges in the design of suspended membrane structures is discussed, with a focus on issues caused by the lack of tools to aid in the design process. These are addressed by the development of a python based GDS package. The reason why Python was used compared to other alternatives was discussed, particularly focusing on benefits in ease of use and compatibility with other industry packages that utilise a shared geometry library, such

as Nazca, GDShelpers and GDSfactory. Detail on the hierarchical structure of the python library was given, with discussion on how it enabled modularity in the design by dividing the membrane footprint into core components based on their function, enabling standardisation of the design process of membrane structure that has not existed previously.

This package was then utilised to tackle challenges faced with the fabrication of thin-film membrane devices, in particular, those which are $< 500\,nm$ in thickness. Design metrics where introduced such as the suspension length and membrane etch length, which were used to aid analysis of the under etching process. The difference between suspension lengths was highlighted for when the under etch process is isotropic versus anisotropic. To address this, a method of including etching features was included, with analysis on the effect on etching time and number of etching holes provided. Issues with the diverse nature of photonic structures was discussed, highlighting how basic layouts techniques struggled to provide predictable etch behaviour.

To resolve this a Lloyd algorithm based layout method was introduced, that allows for uniform conformal placement of holes around photonic structures. The implementation uses an iterative approach which is useful for weakly isotropic etches with a low number of iterations. Higher iterations are useful for complex structures with a strongly isotropic etch. This integration enabled predictable etching behaviour across multiple devices. As such, additional metrics were introduced with the device etch length, photonic structures with similar DELs have the potential to be fabricated together on the same chip. Visualisation tools where provided that allowed comparison of etching behaviour across membrane designs allowing them to be fabricated together. To provide an example, such a design was provided on an AlGaAs wafer. This library acts as a building block for future intelligent designs of transfer printable photonic structures, which will enable the integration of high efficiency heterogeneous waveguide devices.

Chapter 4 tackled several technical challenges with transfer printing, utilising the injection system developed earlier in this work to push the capabilities of what is achievable with transfer print integration. The first challenge addressed was the transfer printing of suspended structures. It is critical to achieve air-clad devices for het-

erogenous integration of high-Q factor devices such as photonic crystal cavities. The air-cladding surrounding the cavity enables a high index contrast between the mode of the cavity and its surroundings. This is critical for high-Q factor systems and non-linear devices. The air-cladding necessity introduces challenges in the printing process when attempting dense integration of device ensembles, as the contact area between the device and the receiving substrate is greatly reduced. By use of the sub-nm precision stage with velocities ranging from $0.05\,\mu ms^{-1}$ to $8000\,\mu ms^{-1}$, it was demonstrated that functional devices could be assembled atop a suspended silica frame structure. This work demonstrated > 400 prints of Silicon PhCCs with a nominal overlap of only $1\,\mu m$, demonstrating a novel new capability for scalable transfer printing.

The second challenge was the in-situ measurement of photonic devices during the print integration process to facilitate deterministic transfer of devices. As discussed in the introduction of this thesis, serial transfer printing allows for the greatest control of the integration process of all the printing processes, at the expense of increasing integration time. By integrating the measurement setup into the print system we can decrease the overall integration time by consolidating back-end process into one step. In this chapter the construction of a cross-polarised microscope was discussed as an additional module for TP2. After combining the in-situ injection setup in chapter 2, with a tuneable swept wavelength laser, operating in the short wavelength infra-red region. This module enabled in-situ characterisation of PhCC devices allowing an array of 119 devices to be printed in wavelength ascending order in a period of ≈ 3 hours.

The capability enabled by having the module integrated into the transfer printer allowed for unique insights into the transfer process that were previously immeasurable. Two detuning effects were detected in the printing process due to a delay of ≈ 10 seconds between the release of the cavity onto the frame and its subsequent measurement. The first was a large permanent red-shift in resonance corresponding to the mechanical fracture of the anchor from the donor chip. The second was also a detuning effect to longer wavelengths, that would relax over a period of hours that corresponded to mechanical stresses during the release process. The ability to detect these changes allowed an empirical development of a printing process that enabled a repeatable printing pro-

cedure. A subset of 10 devices were re-printed 9 times after release from the donor with a permanent detuning measured only after the 5th reprint. The print procedure developed for this work was then repeated for an additional 120 devices, where a device to device spacing of only $7\,\mu m$ was achieved showing the capability of this combination of systems for deterministic integration of dense suspended ensembles.

The integration of photonic crystal cavities by optically monitored transfer printing has provided potentially the most sensitive measurements of mechanical stresses during the transfer print process to date. An upper bound of $0.3\,nm$ was found for the average detuning experienced by the process of printing, which corresponds to a physical deformation of the cavity of only $0.17\,nm$. A deformation on this scale would typically only be measurable by scanning electron microscope or similar, highlighting how the printing of PhCC devices could unlock further developments in transfer print integration.

The work demonstrated in this thesis represents a multi-faceted approach to advance transfer print technology towards an industry scale technique. A critical approach was taken in every aspect to develop either systems, techniques or methods that capitalised on prior knowledge of the integrated photonics space. Careful thought was taken in each stage to allow for continuous development and adaptability where possible, such as the modularity of the transfer print system or the component based structure of the membrane design tool or the modification of printing procedure based on measured results. It is critical to develop each of these tools in parallel to one another to ensure interoperability to provide a comprehensive suite of tools that can address new challenges in the fabrication process. This is essential to take full advantage of its applications in telecommunications, quantum optics, machine learning and more. These tools represent a solid foundation in which the future of transfer printing can be built upon for the integration of advanced materials and devices.

Bibliography

[1] G. Freeman, "Who invented the integrated circuit?" *IEEE Annals of the History of Computing*, vol. 42, no. 3, pp. 75–83, 2020.

[2] The Nobel Prize, "Jack Kilby: Facts," https://www.nobelprize.org/prizes/physics/2000/kilby/facts/, 2025, accessed: 2025-04-18.

[3] J. J. G. M. van der Tol, Y. S. Oei, U. Khalique, R. Nötzel, and M. K. Smit, "InP-based photonic circuits: Comparison of monolithic integration techniques," *Progress in Quantum Electronics*, vol. 34, no. 4, pp. 135–172, Jul. 2010. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0079672710000091

[4] L. A. Eldada, M. Levy, R. Scarmozzino, and R. M. O. Jr, "Laser rapid prototyping of photonic integrated circuits," in *Nanofabrication Technologies and Device Integration*, vol. 2213. SPIE, Jul. 1994, pp. 36–47. [Online]. Available: https://proceedings.spiedigitallibrary.org/conference-proceedings-of-spie/2213/0000/Laser-rapid-prototyping-of-photonic-integrated-circuits/10.1117/12.180981.full

[5] A. Dentai, R. Kuchibhotla, J. Campbell, C. Tsai, and C. Lei, "High quantum efficiency, long wavelength InP/InGaAs microcavity photodiode," *Electronics Letters*, vol. 27, no. 23, pp. 2125–2127, Nov. 1991, publisher: The Institution of Engineering and Technology. [Online]. Available: https://digital-library.theiet.org/doi/10.1049/el:19911316

[6] E.-H. Lee and S. H. Song, "Three-dimensional planar-integrated optics: a comparative view with free-space optics," in *Optoelectronic Integrated*

Circuits IV, vol. 3950. SPIE, Apr. 2000, pp. 194–200. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/3950/0000/Three-dimensional-planar-integrated-optics--a-comparative-view-with/10.1117/12.382162.full

[7] S. Kyatam, D. Mukherjee, H. Neto, and J. Mendes, "Thermal management of photonic integrated circuits: impact of holder material and epoxies," *Applied Optics*, vol. 58, pp. 6126–6135, Jul. 2019.

[8] M. Badás Aldecocea, P. Piron, J. Bouwmeester, L. Jerome, H. Kuiper, and E. Gill, "Opto-thermo-mechanical phenomena in satellite free-space optical communications: survey and challenges," *Optical Engineering*, vol. 63, Oct. 2023.

[9] J. Liu, M. Beals, J. Michel, and L. Kimerling, "Light up the Future of Silicon Microprocessors," *ECS Transactions*, vol. 19, no. 1, p. 17, May 2009, publisher: IOP Publishing. [Online]. Available: https://iopscience.iop.org/article/10.1149/1.3118927/meta

[10] S. Liu and A. Khope, "Latest advances in high-performance light sources and optical amplifiers on silicon," *Journal of Semiconductors*, vol. 42, no. 4, p. 041307, Apr. 2021, publisher: Chinese Institute of Electronics. [Online]. Available: https://dx.doi.org/10.1088/1674-4926/42/4/041307

[11] T. Kamins, *Polycrystalline silicon for integrated circuits and displays*. Springer, 2012.

[12] S. Wang, Y. Li, J. Chen, O. Lin, W. Niu, C. Yang, and A. Tang, "Development and challenges of indium phosphide-based quantum-dot light-emitting diodes," *Journal of Photochemistry and Photobiology C: Photochemistry Reviews*, vol. 55, p. 100588, Jun. 2023. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1389556723000199

[13] G. Granger, M. Bailly, H. Delahaye, C. Jimenez, I. Tiliouine, Y. Leventoux, J.-C. Orlianges, V. Couderc, B. Gérard, R. Becheker, S. Idlahcen, T. Godin,

A. Hideur, A. Grisard, E. Lallier, and S. Février, "GaAs-chip-based mid-infrared supercontinuum generation," *Light: Science & Applications*, vol. 12, no. 1, p. 252, Oct. 2023, publisher: Nature Publishing Group. [Online]. Available: https://www.nature.com/articles/s41377-023-01299-9

[14] S. Rajbhandari, J. J. D. McKendry, J. Herrnsdorf, H. Chun, G. Faulkner, H. Haas, I. M. Watson, D. O'Brien, and M. D. Dawson, "A review of gallium nitride LEDs for multi-gigabit-per-second visible light data communications," *Semiconductor Science and Technology*, vol. 32, no. 2, p. 023001, Feb. 2017. [Online]. Available: https://iopscience.iop.org/article/10.1088/1361-6641/32/2/023001

[15] A. Annoni, E. Guglielmi, M. Carminati, S. Grillanda, P. Ciccarella, G. Ferrari, M. Sorel, M. J. Strain, M. Sampietro, A. Melloni, and F. Morichetti, "Automated Routing and Control of Silicon Photonic Switch Fabrics," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 22, no. 6, pp. 169–176, Nov. 2016. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/7450148

[16] C. Xiang, W. Jin, and J. E. Bowers, "Silicon nitride passive and active photonic integrated circuits: trends and prospects," *Photonics Research*, vol. 10, no. 6, pp. A82–A96, Jun. 2022, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/prj/abstract.cfm?uri=prj-10-6-A82

[17] Y. Qi and Y. Li, "Integrated lithium niobate photonics," *Nanophotonics*, vol. 9, no. 6, pp. 1287–1320, Jun. 2020, publisher: De Gruyter Section: Nanophotonics. [Online]. Available: https://www.degruyterbrill.com/document/doi/10.1515/nanoph-2020-0013/html

[18] H. Ma, A. K. Jen, and L. R. Dalton, "Polymer-based optical waveguides: Materials, processing, and devices," *Advanced Materials*, vol. 14, no. 19, pp. 1339–1365, 2002.

[19] K. Vetter, "Recent Developments in the Fabrication and Operation of Germanium Detectors," *Annual Review of Nuclear and Particle Science*, vol. 57, no. Volume 57, 2007, pp. 363–404, Nov. 2007, publisher: Annual Reviews.

[Online]. Available: https://www.annualreviews.org/content/journals/10.1146/annurev.nucl.56.080805.140525

[20] J. Kaniewski, J. Muszalski, and J. Piotrowski, "Recent advances in InGaAs detector technology," *physica status solidi (a)*, vol. 201, no. 10, pp. 2281–2287, 2004. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.200404819

[21] Z. Fang and C. Z. Zhao, "Recent Progress in Silicon Photonics: A Review," *International Scholarly Research Notices*, vol. 2012, no. 1, p. 428690, 2012. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.5402/2012/428690

[22] C. R. Doerr, "Silicon photonic integration in telecommunications," *Frontiers in Physics*, vol. 3, Aug. 2015, publisher: Frontiers. [Online]. Available: https://www.frontiersin.orghttps://www.frontiersin.org/journals/physics/articles/10.3389/fphy.2015.00037/full

[23] M. AbuGhanem, "Photonic Quantum Computers," Sep. 2024, arXiv:2409.08229 [quant-ph]. [Online]. Available: http://arxiv.org/abs/2409.08229

[24] M. A. Butt, N. L. Kazanskiy, S. N. Khonina, G. S. Voronkov, E. P. Grakhova, and R. V. Kutluyarov, "A Review on Photonic Sensing Technologies: Status and Outlook," *Biosensors*, vol. 13, no. 5, p. 568, May 2023. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC10216520/

[25] C. Wang, X. Xiong, N. Andrade, V. Venkataraman, X.-F. Ren, G.-C. Guo, and M. Lončar, "Second harmonic generation in nano-structured thin-film lithium niobate waveguides," *Optics Express*, vol. 25, no. 6, p. 6963, Mar. 2017. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=oe-25-6-6963

[26] L. Ledezma, A. Roy, L. Costa, R. Sekine, R. Gray, Q. Guo, R. Nehra, R. M. Briggs, and A. Marandi, "Octave-spanning tunable parametric oscillation in nanophotonics," *arXiv*, 2022. [Online]. Available: https://arxiv.org/abs/2203.11482

[27] H. Mahmudlu, S. May, A. Angulo, M. Sorel, and M. Kues, "AlGaAs-on-insulator waveguide for highly efficient photon-pair generation via spontaneous four-wave mixing," *Optics Letters*, vol. 46, no. 5, pp. 1061–1064, Mar. 2021, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/ol/abstract.cfm?uri=ol-46-5-1061

[28] S. May, M. Clerici, and M. Sorel, "Supercontinuum generation in dispersion engineered AlGaAs-on-insulator waveguides," *Scientific Reports*, vol. 11, no. 1, p. 2052, Jan. 2021, publisher: Nature Publishing Group. [Online]. Available: https://www.nature.com/articles/s41598-021-81555-3

[29] ScienceDirect, "Ring resonator," 2025, https://www.sciencedirect.com/topics/computer-science/ring-resonator (Last Accessed 2025-04-18).

[30] H. Saghaei, P. Elyasi, and R. Karimzadeh, "Design, fabrication, and characterization of Mach–Zehnder interferometers," *Photonics and Nanostructures - Fundamentals and Applications*, vol. 37, p. 100733, Dec. 2019. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S156944101930149X

[31] K. Liu, N. Chauhan, J. Wang, A. Isichenko, G. M. Brodnik, P. A. Morton, R. O. Behunin, S. B. Papp, and D. J. Blumenthal, "36 Hz integral linewidth laser based on a photonic integrated 4.0 m coil resonator," *Optica*, vol. 9, no. 7, pp. 770–775, Jul. 2022, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/optica/abstract.cfm?uri=optica-9-7-770

[32] H. A. Haus, W. P. Huang, N. A. Whitaker, and S. Kawakami, "Coupled-mode theory of optical waveguides," *Journal of Lightwave Technology*, vol. 5, p. 16, Jan. 1987. [Online]. Available: https://ui.adsabs.harvard.edu/abs/1987JLwT...5...16H

[33] Y. Shi, L. Ma, Y. Zhuang, and Z. He, "Investigation on roughness-induced scattering loss of small-core polymer waveguides for single-mode optical interconnect applications," *Optics Express*, vol. 28, no. 26, pp. 38 733–

38 744, Dec. 2020, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/oe/abstract.cfm?uri=oe-28-26-38733

[34] R. A. Vicencio, D. Román-Cortés, M. Rubio-Saldías, P. Vildoso, and L. E. F. Foa Torres, "Nonsymmetric evanescent coupling in photonics," *Physical Review A*, vol. 111, no. 4, p. 043510, Apr. 2025. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevA.111.043510

[35] P. Frigeri, L. Seravalli, G. Trevisi, and S. Franchi, "Molecular Beam Epitaxy: An Overview," in *Comprehensive Semiconductor Science and Technology*. Elsevier, 2011, pp. 480–522. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/B9780444531537000997

[36] A. G. Thompson, "MOCVD Technology for Semiconductors," *Materials Letters*, vol. 30, no. 4, pp. 255–263, Mar. 1997. [Online]. Available: https://doi.org/10.1016/S0167-577X(96)00215-7

[37] H. Klapper, "Generation and propagation of dislocations during crystal growth," *Materials Chemistry and Physics*, vol. 66, no. 2, pp. 101–109, Oct. 2000. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0254058400003424

[38] J. Wang, X. Zhao, G. Zou, L. Zhang, S. Han, Y. Li, D. Liu, C. Fernandez, L. Li, L. Ren, and Q. Peng, "Crystal-defect engineering of electrode materials for energy storage and conversion," *Materials Today Nano*, vol. 22, p. 100336, Jun. 2023. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2588842023000354

[39] "Thermocompression Bonding - an overview | ScienceDirect Topics." [Online]. Available: https://www.sciencedirect.com/topics/engineering/thermocompression-bonding

[40] Y. Grauer, A. Miller, D. C. L. Tulipe, A. Manassen, S. Eisenbach, O. Bachar, and R. Gronheid, "Overlay challenges in 3D heterogeneous

integration," in *Metrology, Inspection, and Process Control XXXVI*, vol. 12053. SPIE, May 2022, pp. 113–129. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/12053/120530D/Overlay-challenges-in-3D-heterogeneous-integration/10.1117/12.2608319.full

[41] M. R. Marks, K. Y. Cheong, and Z. Hassan, "A review of laser ablation and dicing of Si wafers," *Precision Engineering*, vol. 73, pp. 377–408, Jan. 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0141635921002464

[42] G. Chappell, B. Guilhabert, T. Garcia, K. Zhao, I. Watson, M. Dawson, M. Tamargo, and J. Hastie, "Suspension and transfer printing of ZnCdMgSe membranes from an InP substrate," *Optical Materials Express*, vol. 10, pp. 3328–3341, Nov. 2020.

[43] D. Sparks, G. Queen, R. Weston, G. Woodward, M. Putty, L. Jordan, S. Zarabadi, and K. Jayakar, "Wafer-to-wafer bonding of nonplanarized MEMS surfaces using solder," *Journal of Micromechanics and Microengineering*, vol. 11, p. 630, Sep. 2001.

[44] H. K. Charles, "Microelectronic Packaging: Electrical Interconnections," in *Encyclopedia of Materials: Science and Technology*, K. H. J. Buschow, R. W. Cahn, M. C. Flemings, B. Ilschner, E. J. Kramer, S. Mahajan, and P. Veyssière, Eds. Oxford: Elsevier, Jan. 2001, pp. 5616–5635. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B0080431526009815

[45] S. Biswas, M. Mozafari, T. Stauden, and H. O. Jacobs, "Surface Tension Directed Fluidic Self-Assembly of Semiconductor Chips across Length Scales and Material Boundaries," *Micromachines*, vol. 7, no. 4, p. 54, Apr. 2016, number: 4 Publisher: Multidisciplinary Digital Publishing Institute. [Online]. Available: https://www.mdpi.com/2072-666X/7/4/54

[46] M. Barelli, C. Vidal, S. Fiorito, A. Myslovska, D. Cielecki, V. Aglieri, I. Moreels, R. Sapienza, and F. Di Stasio, "Single-Photon Emitting

Arrays by Capillary Assembly of Colloidal Semiconductor CdSe/CdS/SiO2 Nanocrystals," *ACS Photonics*, vol. 10, no. 5, pp. 1662–1670, May 2023, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acsphotonics.3c00351

[47] Z. He, J.-L. Wang, S.-M. Chen, J.-W. Liu, and S.-H. Yu, "Self-Assembly of Nanowires: From Dynamic Monitoring to Precision Control," *Accounts of Chemical Research*, vol. 55, no. 11, pp. 1480–1491, Jun. 2022, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acs.accounts.2c00052

[48] J. F. C. Carreira, "Hybrid micro-LED devices enabled by elastomeric micro-transfer printing," 2020.

[49] S. Ghosh, J. O'Callaghan, O. Moynihan, D. Huang, H. Frish, H. Rong, K. Thomas, E. Pelucchi, and B. Corbett, "Scalable transfer printing approach to heterogeneous integration of InP lasers on silicon-on-insulator waveguide platform," *Applied Physics Letters*, vol. 125, no. 8, p. 081104, Aug. 2024. [Online]. Available: https://doi.org/10.1063/5.0223167

[50] G. Chen, J. Goyvaerts, S. Kumari, J. V. Kerrebrouck, M. Muneeb, S. Uvin, Y. Yu, and G. Roelkens, "Integration of high-speed GaAs metal-semiconductor-metal photodetectors by means of transfer printing for 850 nm wavelength photonic interposers," *Optics Express*, vol. 26, no. 5, pp. 6351–6359, Mar. 2018, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/oe/abstract.cfm?uri=oe-26-5-6351

[51] J. A. Smith, D. Jevtics, B. Guilhabert, M. D. Dawson, and M. J. Strain, "Hybrid integration of chipscale photonic devices using accurate transfer printing methods," *Applied Physics Reviews*, vol. 9, no. 4, p. 041317, Dec. 2022.

[52] L. B. Goetting, T. Deng, and G. M. Whitesides, "Microcontact Printing of Alkanephosphonic Acids on Aluminum: Pattern Transfer by Wet Chemical

Etching," *Langmuir*, vol. 15, no. 4, pp. 1182–1191, Feb. 1999. [Online]. Available: https://pubs.acs.org/doi/10.1021/la981094h

[53] K. J. Lee, M. J. Motala, M. A. Meitl, W. R. Childs, E. Menard, A. K. Shim, J. A. Rogers, and R. G. Nuzzo, "Large-Area, Selective Transfer of Microstructured Silicon: A Printing- Based Approach to High-Performance Thin-Film Transistors Supported on Flexible Substrates," *Advanced Materials*, vol. 17, no. 19, pp. 2332–2336, 2005, _eprint: https://advanced.onlinelibrary.wiley.com/doi/pdf/10.1002/adma.200500578. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.200500578

[54] S. A. Lange, V. Benes, D. P. Kern, J. K. H. Hörber, and A. Bernard, "Microcontact Printing of DNA Molecules," *Analytical Chemistry*, vol. 76, no. 6, pp. 1641–1647, Mar. 2004, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/ac035127w

[55] J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, and B. Corbett, "Wafer-scale integration of group III–V lasers on silicon using transfer printing of epitaxial layers," *Nature Photonics*, vol. 6, no. 9, pp. 610–614, Sep. 2012, publisher: Nature Publishing Group. [Online]. Available: https://www.nature.com/articles/nphoton.2012.204

[56] C. A. Bower, E. Menard, and P. E. Garrou, "Transfer printing: An approach for massively parallel assembly of microscale devices," in *2008 58th Electronic Components and Technology Conference*, May 2008, pp. 1105–1109, iSSN: 2377-5726. [Online]. Available: https://ieeexplore.ieee.org/document/4550113

[57] C. A. Bower, M. A. Meitl, B. Raymond, E. Radauscher, R. Cok, S. Bonafede, D. Gomez, T. Moore, C. Prevatte, B. Fisher, R. Rotzoll, G. A. Melnik, A. Fecioru, and A. J. Trindade, "Emissive displays with transfer-printed assemblies of 8m×15m inorganic light-emitting diodes," *Photonics Research*,

vol. 5, no. 2, pp. A23–A29, Apr. 2017, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/prj/abstract.cfm?uri=prj-5-2-A23

[58] S. Jung, U. J. Yang, J. Oh, S. Jeong, Y. Cho, G. H. Lee, M. K. Choi, and C. Yang, "Transfer Printing of Photoactive Layer Enabling Efficient, Wearable, and Dual-Function Organic Solar Cell Modules for a Wireless Healthcare Monitoring System," *Advanced Functional Materials*, vol. 34, no. 41, p. 2406200, 2024, _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/adfm.202406200. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adfm.202406200

[59] E. Margariti, G. Quinn, D. Jevtics, B. Guilhabert, M. D. Dawson, and M. J. Strain, "Continuous roller transfer-printing and automated metrology of >75,000 micro-LED pixels in a single shot," *Optical Materials Express*, vol. 13, no. 8, p. 2236, Aug. 2023. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=ome-13-8-2236

[60] C. Linghu, S. Zhang, C. Wang, H. Luo, and J. Song, "Chapter Eight - Mass transfer for Micro-LED display: Transfer printing techniques," in *Semiconductors and Semimetals*, ser. Micro LEDs, H. Jiang and J. Lin, Eds. Elsevier, Jan. 2021, vol. 106, pp. 253–280. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0080878420300636

[61] Z. Chen, C. Zhang, and Z. Zheng, "Advancements in transfer printing techniques for flexible electronics: adjusting interfaces and promoting versatility," *International Journal of Extreme Manufacturing*, vol. 6, no. 5, p. 052005, Jun. 2024, publisher: IOP Publishing. [Online]. Available: https://dx.doi.org/10.1088/2631-7990/ad5391

[62] N. K. Wessling, S. Ghosh, B. Guilhabert, M. Kappers, A. M. Hinz, M. Toon, R. A. Oliver, M. D. Dawson, and M. J. Strain, "Fabrication and transfer printing based integration of free-standing GaN membrane micro-lenses onto semiconductor chips," *Optical Materials Express*, vol. 12, no. 12, p. 4606, Dec. 2022.

[63] D. Jevtics, J. McPhillimy, B. Guilhabert, J. A. Alanis, H. H. Tan, C. Jagadish, M. D. Dawson, A. Hurtado, P. Parkinson, and M. J. Strain, "Characterization, Selection, and Microassembly of Nanowire Laser Systems," *Nano Letters*, vol. 20, no. 3, pp. 1862–1868, Mar. 2020, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acs.nanolett.9b05078

[64] J. McPhillimy, D. Jevtics, B. J. E. Guilhabert, C. Klitis, A. Hurtado, M. Sorel, M. D. Dawson, and M. J. Strain, "Automated Nanoscale Absolute Accuracy Alignment System for Transfer Printing," *ACS Applied Nano Materials*, vol. 3, no. 10, pp. 10 326–10 332, Oct. 2020, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acsanm.0c02224

[65] J. McPhillimy, S. May, C. Klitis, B. Guilhabert, M. D. Dawson, M. Sorel, and M. J. Strain, "Transfer printing of AlGaAs-on-SOI microdisk resonators for selective mode coupling and low-power nonlinear processes," *Optics Letters*, vol. 45, no. 4, p. 881, Feb. 2020. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=ol-45-4-881

[66] B. Guilhabert, S. P. Bommer, N. K. Wessling, D. Jevtics, J. A. Smith, Z. Xia, S. Ghosh, M. Kappers, I. M. Watson, R. A. Oliver, M. D. Dawson, and M. J. Strain, "Advanced Transfer Printing With In-Situ Optical Monitoring for the Integration of Micron-Scale Devices," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 29, no. 3: Photon. Elec. Co-Inte. and Adv. Trans. Print., pp. 1–11, May 2023.

[67] X. Feng, M. A. Meitl, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Competing fracture in kinetically controlled transfer printing," *Langmuir*, vol. 23, no. 25, p. 12555–12560, Dec. 2007.

[68] G. Violano, A. Chateauminois, and L. Afferrante, "Rate-dependent adhesion of viscoelastic contacts, Part I: Contact area and contact line velocity within model randomly rough surfaces," *Mechanics of Materials*, vol. 160, p. 103926,

Sep. 2021. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0167663621001708

[69] X. Zhou, P. Tian, C.-W. Sher, J. Wu, H. Liu, R. Liu, and H.-C. Kuo, "Growth, transfer printing and colour conversion techniques towards full-colour micro-LED display," *Progress in Quantum Electronics*, vol. 71, p. 100263, May 2020. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0079672720300173

[70] Q. Guo, L. Yang, Y. Gan, J. Zhang, J. Zhang, J. Jiang, W. Lin, K. Chen, C. Zhang, and Y. Wang, "Advancing Electronics Manufacturing Using Dynamically Programmable Micro-Transfer Printing System," Mar. 2025, arXiv:2503.11109 [physics]. [Online]. Available: http://arxiv.org/abs/2503.11109

[71] H. Luo, C. Wang, C. Linghu, K. Yu, C. Wang, and J. Song, "Laser-driven programmable non-contact transfer printing of objects onto arbitrary receivers via an active elastomeric microstructured stamp," *National Science Review*, vol. 7, no. 2, pp. 296–304, Feb. 2020. [Online]. Available: https://doi.org/10.1093/nsr/nwz109

[72] J.-W. Jang, A. Smetana, and P. Stiles, "Multiplexed Dip Pen Nanolithography patterning by simple desktop nanolithography platform," in *Microfluidics, BioMEMS, and Medical Microsystems VIII*, vol. 7593. SPIE, Feb. 2010, pp. 261–268. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/7593/75930Y/Multiplexed-Dip-Pen-Nanolithography-patterning-by-simple-desktop-nanolithography-platform/10.1117/12.845214.full

[73] M. Niels, T. Vanackere, T. Vandekerckhove, S. Poelman, T. Reep, G. Roelkens, M. Billet, and B. Kuyken, "Centimetre-Scale Micro-Transfer Printing to enable Heterogeneous Integration of Thin Film Lithium Niobate with Silicon Photonics," Feb. 2025, arXiv:2412.15157 [physics]. [Online]. Available: http://arxiv.org/abs/2412.15157

[74] Z. Li, J. Smith, M. Scullion, N. Wessling, L. McKnight, M. Dawson, and M. Strain, *Photonic integration of lithium niobate micro-ring resonators onto silicon nitride waveguide chips by transfer-printing*, Aug. 2022.

[75] A. Ghaffari, A. Hosseini, X. Xu, D. Kwong, H. Subbaraman, and R. T. Chen, "Transfer of micro and nano-photonic silicon nanomembrane waveguide devices on flexible substrates." *Optics express*, vol. 18, pp. 20 086–95, 9 2010.

[76] K. H. Lee, S. Zhang, Y. Gu, T. P. Lodge, and C. D. Frisbie, "Transfer Printing of Thermoreversible Ion Gels for Flexible Electronics," *ACS Applied Materials & Interfaces*, vol. 5, no. 19, pp. 9522–9527, Oct. 2013, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/am402200n

[77] "Gdshelpers," https://gdshelpers.readthedocs.io/en/latest/ (Last Accessed 2025-04-18).

[78] "GDSFactory," https://gdsfactory.github.io/gdsfactory/index.html (Last Accessed 2025-04-18).

[79] "Nazca," https://nazca-design.org/ (Last Accessed 2025-04-18).

[80] "Klayout," https://www.klayout.de/ (Last Accessed 2025-04-18).

[81] "Ansys Lumerical," https://www.ansys.com/products/optics/fdtd (Last Accessed 2025-04-18).

[82] "Tidy3d Flexcompute," https://www.flexcompute.com/tidy3d/solver/ (Last Accessed 2025-04-18).

[83] D.-S. Lee and S. H. Kim, "Chapter Eleven - Monolithic integration of AlGaInP red and InGaN blue/green LEDs," in *Semiconductors and Semimetals*, ser. Micro LEDs, H. Jiang and J. Lin, Eds. Elsevier, Jan. 2021, vol. 106, pp. 345–387. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0080878421000041

[84] N. P. Pham, T. L. M. Scholtes, R. Klerk, B. Wieder, P. M. Sarro, and J. N. Burghartz, "Direct spray coating of photoresist for MEMS applications," in *Micromachining and Microfabrication Process Technology VII*, vol. 4557. SPIE, Sep. 2001, pp. 312–319. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/4557/0000/Direct-spray-coating-of-photoresist-for-MEMS-applications/10.1117/12.442960.full

[85] F.-C. Chou, M.-W. Wang, S.-C. Gong, and Z.-G. Yang, "Reduction of photoresist usage during spin coating," *Journal of Electronic Materials*, vol. 30, no. 4, pp. 432–438, Apr. 2001. [Online]. Available: https://doi.org/10.1007/s11664-001-0055-6

[86] E. Sharma, R. Rathi, J. Misharwal, B. Sinhmar, S. Kumari, J. Dalal, and A. Kumar, "Evolution in Lithography Techniques: Microlithography to Nanolithography," *Nanomaterials*, vol. 12, no. 16, p. 2754, Jan. 2022, number: 16 Publisher: Multidisciplinary Digital Publishing Institute. [Online]. Available: https://www.mdpi.com/2079-4991/12/16/2754

[87] K. Racka-Szmidt, B. Stonio, J. Żelazko, M. Filipiak, and M. Sochacki, "A Review: Inductively Coupled Plasma Reactive Ion Etching of Silicon Carbide," *Materials*, vol. 15, no. 1, p. 123, Dec. 2021. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC8745874/

[88] W. P. Gomes, "Chapter 6 - Wet etching of III–V semiconductors," in *Handbook of Advanced Electronic and Photonic Materials and Devices*, H. Singh Nalwa, Ed. Burlington: Academic Press, Jan. 2001, pp. 221–256. [Online]. Available: https://www.sciencedirect.com/science/article/pii/B9780125137454500184

[89] F. G. Aras, A. Yilmaz, H. G. Tasdelen, A. Ozden, F. Ay, N. K. Perkgoz, and A. Yeltik, "A review on recent advances of chemical vapor deposition technique for monolayer transition metal dichalcogenides (MX2: Mo, W; S, Se, Te)," *Materials Science in Semiconductor Processing*, vol. 148, p. 106829,

Sep. 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1369800122003687

[90] J.-F. Zheng, P. J. Hanberg, H. V. Demir, V. A. Sabnis, O. Fidaner, J. S. H. Jr, and D. A. B. Miller, "Novel planarization and passivation in the integration of III-V semiconductor devices," in *Optoelectronic Integrated Circuits VI*, vol. 5356. SPIE, Jun. 2004, pp. 81–91. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/5356/0000/Novel-planarization-and-passivation-in-the-integration-of-III-V/10.1117/12.529696.full

[91] J. A. Smith, D. Jevtics, B. Guilhabert, M. D. Dawson, and M. J. Strain, "Hybrid integration of chipscale photonic devices using accurate transfer printing methods," *Applied Physics Reviews*, vol. 9, no. 4, p. 041317, Dec. 2022.

[92] J. McPhillimy, D. Jevtics, B. J. Guilhabert, C. Klitis, A. Hurtado, M. Sorel, and M. D. Dawson, "Automated nanoscale absolute accuracy alignment system for transfer printing," *ACS Applied Nano Materials*, vol. 3, no. 10, pp. 10 326–10 332, oct 2020.

[93] E. Perez, G. Moille, X. Lu, D. Westly, and K. Srinivasan, "Automated on-axis direct laser writing of coupling elements for photonic chips," *Optics express*, vol. 28, no. 26, pp. 39 340–39 353, Dec. 2020. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC8482346/

[94] B. Guilhabert, S. P. Bommer, N. K. Wessling, D. Jevtics, J. A. Smith, Z. Xia, S. Ghosh, M. Kappers, I. M. Watson, R. A. Oliver, M. D. Dawson, and M. J. Strain, "Advanced transfer printing with in-situ optical monitoring for the integration of micron-scale devices," *IEEE Journal of Selected Topics in Quantum Electronics*, pp. 1–12, 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9973343/

[95] "How to Build a Beam Expander." [Online]. Available: https://www.newport.com/n/how-to-build-a-beam-expander

[96] R. Cassells, J. A. Smith, C. Hu, S. P. Bommer, B. Guilhabert, M. D. Dawson, and M. J. Strain, "Planar waveguide to vertical mode couplers covering the visible to IR spectral range," *Optics Express*, vol. 32, no. 22, p. 38128, Oct. 2024. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=oe-32-22-38128

[97] K. A. Buzaverov, A. S. Baburin, E. V. Sergeev, S. S. Avdeev, E. S. Lotkov, S. V. Bukatin, I. A. Stepanov, A. B. Kramarenko, A. S. Amiraslanov, D. V. Kushnev, I. A. Ryzhikov, and I. A. Rodionov, "Silicon Nitride Integrated Photonics from Visible to Mid-Infrared Spectra," *Laser & Photonics Reviews*, vol. 18, no. 12, p. 2400508, 2024.

[98] "Resistor ladder," https://en.wikipedia.org/w/index.php?title=Resistor_ladder&oldid=1276969588 (Last Accessed 2025-04-18).

[99] "Binary number," https://en.wikipedia.org/w/index.php?title=Binary_number&oldid=1283245201 (Last Accessed 2025-04-18).

[100] "I²C," https://en.wikipedia.org/w/index.php?title=I%C2%B2C&oldid=1279068511 (Last Accessed 2025-04-18).

[101] "Finite state machine," https://en.wikipedia.org/w/index.php?title=Finite-state_machine&oldid=1285525354 (Last Accessed 2025-04-18).

[102] J. M. Stone, H. A. C. Wood, K. Harrington, and T. A. Birks, "Low index contrast imaging fibers," *Optics Letters*, vol. 42, no. 8, p. 1484, Apr. 2017. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=ol-42-8-1484

[103] "Distortion (optics)," https://en.wikipedia.org/w/index.php?title=Distortion_(optics)&oldid=1282377909 (Last Accessed 2025-04-18).

[104] T. Eder, A. Mautner, Y. Xu, M. R. Reithofer, A. Bismarck, and J. M. Chin, "Transparent PDMS Surfaces with Covalently Attached Lubricants for Enhanced Anti-adhesion Performance," *ACS Applied Materials & Interfaces*, vol. 16, no. 8, pp. 10 942–10 952, Feb. 2024, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acsami.3c17110

[105] Z. Cai, W. Qiu, G. Shao, and W. Wang, "A new fabrication method for all-PDMS waveguides," *Sensors and Actuators A: Physical*, vol. 204, pp. 44–47, Dec. 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0924424713004640

[106] J. C. McDonald, D. C. Duffy, J. R. Anderson, D. T. Chiu, H. Wu, O. J. A. Schueller, and G. M. Whitesides, "Fabrication of microfluidic systems in poly(dimethylsiloxane)," *ELECTROPHORESIS*, vol. 21, no. 1, pp. 27–40, 2000, _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/%28SICI%291522-2683%2820000101%2921%3A1%3C27%3A%3AAID-ELPS27%3E3.0.CO%3B2-C. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/%28SICI%291522-2683%2820000101%2921%3A1%3C27%3A%3AAID-ELPS27%3E3.0.CO%3B2-C

[107] J. C. McDonald and G. M. Whitesides, "Poly(dimethylsiloxane) as a Material for Fabricating Microfluidic Devices," *Accounts of Chemical Research*, vol. 35, no. 7, pp. 491–499, Jul. 2002, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/ar010110q

[108] L. Cheng, S. Mao, Z. Li, Y. Han, and H. Y. Fu, "Grating Couplers on Silicon Photonics: Design Principles, Emerging Trends and Practical Issues," *Micromachines*, vol. 11, no. 7, p. 666, Jul. 2020, number: 7 Publisher: Multidisciplinary Digital Publishing Institute. [Online]. Available: https://www.mdpi.com/2072-666X/11/7/666

[109] A. Bozzola, L. Carroll, D. Gerace, I. Cristiani, and L. C. Andreani, "Optimising apodized grating couplers in a pure SOI platform to 0.5 dB coupling efficiency," *Optics Express*, vol. 23, no. 12, pp. 16 289–16 304, Jun. 2015, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/oe/abstract.cfm?uri=oe-23-12-16289

[110] H.-W. Rhee, J. Shim, J.-Y. Kim, D. J. Bang, H. Yoon, M. Kim, C. C. Kim, J.-B. You, and H.-H. Park, "Direct optical wire bonding through open-to-air

polymerization for silicon photonic chips," *Optics Letters*, vol. 47, no. 3, pp. 714–717, Feb. 2022, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/ol/abstract.cfm?uri=ol-47-3-714

[111] K. P. Rola, K. Ptasiński, A. Zakrzewski, and I. Zubel, "Silicon 45° micromirrors fabricated by etching in alkaline solutions with organic additives," *Microsystem Technologies*, vol. 20, no. 2, pp. 221–226, Feb. 2014. [Online]. Available: https://doi.org/10.1007/s00542-013-1859-z

[112] R. Cassells, J. Smith, C. Hu, S. Bommer, B. Guilhabert, M. D. Dawson, and M. J. Strain, "Waveguide vertical couplers covering the visible to IR spectral range: IEEE Photonics Conference 2024," *2024 IEEE Photonics Conference (IPC)*, pp. 1–2, Dec. 2024, publisher: IEEE.

[113] Z. Cai, "Loss analysis of a grating coupler for single-mode fiber coupling into an SOI waveguide," *Applied Optics*, vol. 63, no. 14, pp. 3763–3769, May 2024, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/ao/abstract.cfm?uri=ao-63-14-3763

[114] D. Li, D. Yang, M. Xiang, Z. Chen, Z. Song, and Y. Wang, "A spot-size converter designed with a SU8 polymer cladding for LNOI waveguide," in *Eighth Symposium on Novel Photoelectronic Detection Technology and Applications*, vol. 12169. SPIE, Mar. 2022, pp. 1877–1882. [Online]. Available: https://www.spiedigitallibrary.org/conference-proceedings-of-spie/12169/121697O/A-spot-size-converter-designed-with-a-SU8-polymer-cladding/10.1117/12.2625049.full

[115] Q. Liu, J. Jiang, W. Xiu, Z. Ming, B. Cui, L. Zheng, J. Wang, and L. Qi, "Research Progress on Precision Tool Alignment Technology in Machining," *Micromachines*, vol. 15, no. 10, p. 1202, Oct. 2024, number: 10 Publisher: Multidisciplinary Digital Publishing Institute. [Online]. Available: https://www.mdpi.com/2072-666X/15/10/1202

[116] J. McPhillimy, D. Jevtics, B. J. E. Guilhabert, C. Klitis, A. Hurtado, M. Sorel, M. D. Dawson, and M. J. Strain, "Automated Nanoscale Absolute Accuracy Alignment System for Transfer Printing," *ACS Applied Nano Materials*, vol. 3, no. 10, pp. 10 326–10 332, Oct. 2020.

[117] P. Sitthi-Amorn, J. E. Ramos, Y. Wangy, J. Kwan, J. Lan, W. Wang, and W. Matusik, "MultiFab: a machine vision assisted platform for multi-material 3D printing," *ACM Trans. Graph.*, vol. 34, no. 4, pp. 129:1–129:11, Jul. 2015. [Online]. Available: https://dl.acm.org/doi/10.1145/2766962

[118] L. Wang, J. Qiu, Z. Dong, Y. Chen, L. Wu, H. Guo, and J. Wu, "Single-etched fiber-chip coupler with a metal mirror on a 220-nm silicon-on-insulator platform for perfectly vertical coupling," *Optics Letters*, vol. 49, no. 11, pp. 2974–2977, Jun. 2024, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/ol/abstract.cfm?uri=ol-49-11-2974

[119] C.-C. Lin, A. Na, Y.-K. Wu, L. Wang, and N. Na, "Optimization of Grating Coupler over Single-Mode Silicon-on-Insulator Waveguide to Reach $<$ 1 dB Loss through Deep-Learning-Based Inverse Design," *Photonics*, vol. 11, no. 3, p. 267, Mar. 2024, number: 3 Publisher: Multidisciplinary Digital Publishing Institute. [Online]. Available: https://www.mdpi.com/2304-6732/11/3/267

[120] G. Roelkens, J. Zhang, L. Bogaert, E. Soltanian, M. Billet, A. Uzun, B. Pan, Y. Liu, E. Delli, D. Wang, V. B. Oliva, L. T. Ngoc Tran, X. Guo, H. Li, S. Qin, K. Akritidis, Y. Chen, Y. Xue, M. Niels, D. Maes, M. Kiewiet, T. Reep, T. Vanackere, T. Vandekerckhove, I. L. Lufungula, J. De Witte, L. Reis, S. Poelman, Y. Tan, H. Deng, W. Bogaerts, G. Morthier, D. Van Thourhout, and B. Kuyken, "Present and future of micro-transfer printing for heterogeneous photonic integrated circuits," *APL Photonics*, vol. 9, no. 1, p. 010901, Jan. 2024. [Online]. Available: https://doi.org/10.1063/5.0181099

[121] T.-W. Lu, Y.-C. Lin, and P.-T. Lee, "Highly Accurate Docking of a Photonic Crystal Nanolaser to a SiNx Waveguide by Transfer Printing," *ACS Photonics*,

vol. 10, no. 8, pp. 2679–2687, Aug. 2023, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acsphotonics.3c00411

[122] I. Mathews, D. Quinn, J. Justice, A. Gocalinska, E. Pelucchi, R. Loi, J. O. Callaghan, and B. Corbett, "Micro-transfer printing high-efficiency GaAs photovoltaic cells onto silicon for wireless power applications," May 2020, arXiv:2006.12223 [physics]. [Online]. Available: http://arxiv.org/abs/2006.12223

[123] A. Osada, Y. Ota, R. Katsumi, K. Watanabe, S. Iwamoto, and Y. Arakawa, "Transfer-printed quantum-dot nanolasers on a silicon photonic circuit," *Applied Physics Express*, vol. 11, no. 7, p. 072002, Jul. 2018, arXiv:1803.11552 [physics]. [Online]. Available: http://arxiv.org/abs/1803.11552

[124] M. Theurer, M. Moehrle, A. Sigmund, K.-O. Velthaus, R. M. Oldenbeuving, L. Wevers, F. M. Postma, R. Mateman, F. Schreuder, D. Geskus, K. Wörhoff, R. Dekker, R. G. Heideman, and M. Schell, "Flip-Chip Integration of InP to SiN Photonic Integrated Circuits," *Journal of Lightwave Technology*, vol. 38, no. 9, pp. 2630–2636, May 2020. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/8985330

[125] S. Ghosh, S. Yegnanarayanan, D. Kharas, M. Ricci, J. J. Plant, and P. W. Juodawlkis, "Wafer-scale heterogeneous integration of thin film lithium niobate on silicon-nitride photonic integrated circuits with low loss bonding interfaces," *Optics Express*, vol. 31, no. 7, pp. 12 005–12 015, Mar. 2023, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/oe/abstract.cfm?uri=oe-31-7-12005

[126] T. Vanackere, T. Vandekerckhove, L. Bogaert, M. Billet, S. Poelman, S. Cuyvers, J. Van Kerrebrouck, A. Moerman, O. Caytan, N. Singh, S. Lemey, G. Torfs, P. Ossieur, G. Roelkens, S. Clemmen, and B. Kuyken, "Heterogeneous integration of a high-speed lithium niobate modulator on silicon nitride using micro-transfer printing," *APL Photonics*, vol. 8, no. 8, p. 086102,

Aug. 2023. [Online]. Available: https://pubs.aip.org/app/article/8/8/086102/2905003/Heterogeneous-integration-of-a-high-speed-lithium

[127] "Heterogeneous integration starts here," https://x-celeprint.com/ (Last Accessed 2025-04-18).

[128] M. K. Mishra, V. Dubey, P. M. Mishra, and I. Khan, "MEMS Technology: A Review," *Journal of Engineering Research and Reports*, pp. 1–24, Feb. 2019. [Online]. Available: https://journaljerr.com/index.php/JERR/article/view/76

[129] V. Stojanović, R. J. Ram, M. Popović, S. Lin, S. Moazeni, M. Wade, C. Sun, L. Alloatti, A. Atabaki, F. Pavanello, N. Mehta, and P. Bhargava, "Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes [Invited]," *Optics Express*, vol. 26, no. 10, p. 13106, May 2018. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=oe-26-10-13106

[130] "Guido van rossum," https://en.wikipedia.org/w/index.php?title=Guido_van_Rossum&oldid=1285749495 (Last Accessed 2025-04-18).

[131] "A Review of Existing Approaches to Increase the Computational Speed of the Python Language," *International Journal of Research in Engineering, Science and Management*.

[132] A. N. Ziogas, T. Schneider, T. Ben-Nun, A. Calotoiu, T. D. Matteis, J. d. F. Licht, L. Lavarini, and T. Hoefler, "Productivity, Portability, Performance: Data-Centric Python," *ACM Computing Surveys*, p. 1122445.1122456, Mar. 2022, arXiv:2107.00555 [cs]. [Online]. Available: http://arxiv.org/abs/2107.00555

[133] "Shapely," https://shapely.readthedocs.io/en/stable/index.html (Last Accessed 2025-04-18).

[134] C. Wang, C. Linghu, S. Nie, C. Li, Q. Lei, X. Tao, Y. Zeng, Y. Du, S. Zhang, K. Yu, H. Jin, W. Chen, and J. Song, "Programmable and scalable transfer printing with high reliability and efficiency for flexible inorganic electronics,"

Science Advances, vol. 6, no. 25, p. eabb2393, Jun. 2020. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC7299632/

[135] H. Zhou, W. Qin, Q. Yu, H. Cheng, X. Yu, and H. Wu, "Transfer Printing and its Applications in Flexible Electronic Devices," *Nanomaterials*, vol. 9, no. 2, p. 283, Feb. 2019, number: 2 Publisher: Multidisciplinary Digital Publishing Institute. [Online]. Available: https://www.mdpi.com/2079-4991/9/2/283

[136] "MEGAPOSIT™ SPR™220 SERIES i-LINE PHOTORESISTS," *Semiconductor Technologies*, no. 889, 2014.

[137] W. Kubota, R. Yamaoka, T. Utsunomiya, T. Ichii, and H. Sugimura, "Vapor-Phase Chemical Etching of Silicon Assisted by Graphene Oxide for Microfabrication and Microcontact Printing," *ACS Applied Nano Materials*, vol. 5, no. 8, pp. 11 707–11 714, Aug. 2022, publisher: American Chemical Society. [Online]. Available: https://doi.org/10.1021/acsanm.2c02690

[138] R. Orghici, U. Willer, M. Gierszewska, S. Waldvogel, and W. Schade, "Fiber optic evanescent field sensor for detection of explosives and CO2 dissolved in water," *Applied Physics B*, vol. 90, no. 2, pp. 355–360, Feb. 2008. [Online]. Available: https://doi.org/10.1007/s00340-008-2932-7

[139] A. M. Hutchinson, "Evanescent wave biosensors. Real-time analysis of biomolecular interactions," *Molecular Biotechnology*, vol. 3, no. 1, pp. 47–54, Feb. 1995.

[140] F. Aurenhammer, "Voronoi diagrams—a survey of a fundamental geometric data structure," *ACM Computing Surveys*, vol. 23, no. 3, pp. 345–405, Sep. 1991. [Online]. Available: https://dl.acm.org/doi/10.1145/116873.116880

[141] A. A. Taha and A. Hanbury, "An Efficient Algorithm for Calculating the Exact Hausdorff Distance," *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. 37, no. 11, pp. 2153–2163, Nov. 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7053955/

[142] T. Asano and S. Noda, "Photonic crystal devices in silicon photonics," *Proceedings of the IEEE*, vol. 106, no. 12, p. 2183–2195, Dec. 2018.

[143] Y. Lai, S. Pirotta, G. Urbinati, D. Gerace, M. Minkov, V. Savona, A. Badolato, and M. Galli, "Genetically designed l3 photonic crystal nanocavities with measured quality factor exceeding one million," *Applied Physics Letters*, vol. 104, no. 24, p. 241101, Jun. 2014.

[144] K. Deasy, K. N. Sediq, S. Brittle, T. Wang, F. Davis, T. H. Richardson, and D. G. Lidzey, "A chemical sensor based on a photonic-crystal l3 nanocavity defined in a silicon-nitride membrane," *Journal of Materials Chemistry C*, vol. 2, pp. 8700–8706, 10 2014.

[145] L. Picelli, A. V. Klinken, G. Lindgren, K. D. Hakkel, F. Pagliano, N. Fiaschi, I. Sersic-Vollenbroek, P. J. V. Veldhoven, R. W. V. D. Heijden, and A. Fiore, "Scalable wafer-to-fiber transfer method for lab-on-fiber sensing," *Applied Physics Letters*, vol. 117, 10 2020.

[146] G. Marty, S. Combrié, F. Raineri, and A. De Rossi, "Photonic crystal optical parametric oscillator," *Nature Photonics*, vol. 15, no. 1, p. 53–58, Jan. 2021.

[147] A. Chopin, A. Barone, I. Ghorbel, S. Combrié, D. Bajoni, F. Raineri, M. Galli, and A. De Rossi, "Ultra-efficient generation of time-energy entangled photon pairs in an InGaP photonic crystal cavity," *Communications Physics*, vol. 6, no. 1, pp. 1–9, Apr. 2023.

[148] S. Noda, K. Kitamura, T. Okino, D. Yasuda, and Y. Tanaka, "Photonic-crystal surface-emitting lasers: Review and introduction of modulated-photonic crystals," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 23, no. 6, p. 1–7, Nov. 2017.

[149] E. Dimopoulos, A. Sakanas, A. Marchevsky, M. Xiong, Y. Yu, E. Semenova, J. Mørk, and K. Yvind, "Electrically-driven photonic crystal lasers with ultra-low threshold," *Laser & Photonics Reviews*, vol. 16, no. 11, p. 2200109, 2022.

[150] K. Kuruma, Y. Ota, M. Kakuda, S. Iwamoto, and Y. Arakawa, "Surface-passivated high-q gaas photonic crystal nanocavity with quantum dots," *APL Photonics*, vol. 5, no. 4, p. 046106, Apr. 2020.

[151] C. L. Phillips, A. J. Brash, M. Godsland, N. J. Martin, A. Foster, A. Tomlinson, R. Dost, N. Babazadeh, E. M. Sala, L. Wilson, J. Heffernan, M. S. Skolnick, and A. M. Fox, "Purcell-enhanced single photons at telecom wavelengths from a quantum dot in a photonic crystal cavity," *Scientific Reports*, vol. 14, no. 1, p. 4450, Feb. 2024.

[152] M. Petruzzella, F. M. Pagliano, Zobenica, S. Birindelli, M. Cotrufo, F. W. V. Otten, R. W. V. D. Heijden, and A. Fiore, "Electrically driven quantum light emission in electromechanically tuneable photonic crystal cavities," *Applied Physics Letters*, vol. 111, p. 251101, 12 2017.

[153] S. Iadanza, G. C. R. Devarapu, A. Blake, P. A. Alba, J.-M. Pedini, and L. O'Faolain, "Polycrystalline silicon PhC cavities for CMOS on-chip integration," *Scientific Reports*, vol. 12, no. 1, p. 17097, Oct. 2022.

[154] M. Settle, M. Salib, A. Michaeli, and T. F. Krauss, "Low loss silicon on insulator photonic crystal waveguides made by 193nm optical lithography," *Optics Express*, vol. 14, no. 6, p. 2440–2445, Mar. 2006.

[155] Y. Xiao, F. Wang, D. Mao, T. Kananen, T. Li, H. Lee, Z. Wang, and T. Gu, "Scalable photonic crystal waveguides with 2 db component loss," *IEEE Photonics Technology Letters*, vol. 34, no. 12, p. 637–640, Jun. 2022.

[156] Y. Ooka, T. Tetsumoto, A. Fushimi, W. Yoshiki, and T. Tanabe, "Cmos compatible high-q photonic crystal nanocavity fabricated with photolithography on silicon photonic platform," *Scientific Reports 2015 5:1*, vol. 5, pp. 1–9, 6 2015.

[157] A. Samarelli, D. S. Macintyre, M. J. Strain, R. M. D. L. Rue, M. Sorel, and S. Thoms, "Optical characterization of a hydrogen silsesquioxane lithography process," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures*, vol. 26, pp. 2290–2294, 2008.

[158] N. L. Thomas, Z. Diao, H. Zhang, and R. Houdré, "Statistical analysis of sub-nanometer residual disorder in photonic crystal waveguides: Correlation between slow light properties and structural properties," *Journal of Vacuum Science and Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 29, 9 2011.

[159] C. L. Panuski, I. Christen, M. Minkov, C. J. Brabec, S. Trajtenberg-Mills, A. D. Griffiths, J. J. D. McKendry, G. L. Leake, D. J. Coleman, C. Tran, J. St Louis, J. Mucci, C. Horvath, J. N. Westwood-Bachman, S. F. Preble, M. D. Dawson, M. J. Strain, M. L. Fanto, and D. R. Englund, "A full degree-of-freedom spatiotemporal light modulator," *Nature Photonics*, vol. 16, no. 12, p. 834–842, Dec. 2022.

[160] L. Midolo, P. J. van Veldhoven, M. A. Dündar, R. Nötzel, and A. Fiore, "Electromechanical wavelength tuning of double-membrane photonic crystal cavities," *Applied Physics Letters*, vol. 98, no. 21, p. 211120, May 2011.

[161] C. Grillet, C. Monat, C. Smith, M. Lee, S. Tomljenovic-Hanic, C. Karnutsch, and B. Eggleton, "Reconfigurable photonic crystal circuits," *Laser & Photonics Reviews*, vol. 4, no. 2, p. 192–204, 2010.

[162] F. S. F. Brossard, V. Pecunia, A. J. Ramsay, J. P. Griffiths, M. Hugues, H. F. S. S. F. Brossard, A. J. Ramsay, V. Pecunia, J. P. Griffiths, H. Sirringhaus, and M. Hugues, "Inkjet-printed nanocavities on a photonic crystal template," *Advanced Materials*, vol. 29, p. 1704425, 12 2017.

[163] H. Chong and R. De La Rue, "Tuning of photonic crystal waveguide microcavity by thermooptic effect," *IEEE Photonics Technology Letters*, vol. 16, no. 6, pp. 1528–1530, Jun. 2004.

[164] C. Husko, A. De Rossi, S. Combrié, Q. V. Tran, F. Raineri, and C. W. Wong, "Ultrafast all-optical modulation in GaAs photonic crystal cavities," *Applied Physics Letters*, vol. 94, no. 2, p. 021111, Jan. 2009.

[165] J. Jágerská, H. Zhang, Z. Diao, N. L. Thomas, and R. Houdré, "Refractive index sensing with an air-slot photonic crystal nanocavity," *Optics Letters*, vol. 35, no. 15, pp. 2523–2525, Aug. 2010, publisher: Optica Publishing Group. [Online]. Available: https://opg.optica.org/ol/abstract.cfm?uri=ol-35-15-2523

[166] E. Yablonovitch, "Inhibited Spontaneous Emission in Solid-State Physics and Electronics," *Physical Review Letters*, vol. 58, no. 20, pp. 2059–2062, May 1987. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRevLett.58.2059

[167] W. L. Vos and L. A. Woldering, "Cavity quantum electrodynamics with three-dimensional photonic bandgap crystals," Apr. 2015, arXiv:1504.06803 [quant-ph]. [Online]. Available: http://arxiv.org/abs/1504.06803

[168] D. P. Bourne and S. M. Roper, "Centroidal Power Diagrams, Lloyd's Algorithm, and Applications to Optimal Location Problems," *SIAM Journal on Numerical Analysis*, vol. 53, no. 6, pp. 2545–2569, Jan. 2015.

[169] M. Minkov, V. Savona, and D. Gerace, "Photonic crystal slab cavity simultaneously optimized for ultra-high Q/V and vertical radiation coupling," *Appl. Phys. Lett*, vol. 111, p. 131104, 2017.

[170] M. W. McCutcheon, G. W. Rieger, I. W. Cheung, J. F. Young, D. Dalacu, S. Frédérick, P. J. Poole, G. C. Aers, and R. L. Williams, "Resonant scattering and second-harmonic spectroscopy of planar photonic crystal microcavities," *Applied Physics Letters*, vol. 87, no. 22, p. 221110, Nov. 2005. [Online]. Available: https://pubs.aip.org/apl/article/87/22/221110/325795/Resonant-scattering-and-second-harmonic

[171] M. Galli, S. Portalupi, M. Belotti, L. Andreani, L. O'Faolain, and T. Krauss, "Light scattering and fano resonances in high-q photonic crystal nanocavities," *Applied Physics Letters*, vol. 94, no. 7, 2009.

[172] C. Wu, N. Arju, G. Kelp, J. A. Fan, J. Dominguez, E. Gonzales, E. Tutuc, I. Brener, and G. Shvets, "Spectrally selective chiral silicon metasurfaces based on infrared fano resonances," *Nature communications*, vol. 5, no. 1, p. 3892, 2014.

[173] Y. Yang, I. I. Kravchenko, D. P. Briggs, and J. Valentine, "All-dielectric metasurface analogue of electromagnetically induced transparency," *Nature communications*, vol. 5, no. 1, p. 5753, 2014.

[174] M. F. Limonov, M. V. Rybin, A. N. Poddubny, and Y. S. Kivshar, "Fano resonances in photonics," *Nature photonics*, vol. 11, no. 9, pp. 543–554, 2017.

[175] A. Carlson, S. Wang, P. Elvikis, P. M. Ferreira, Y. Huang, and J. A. Rogers, "Active, programmable elastomeric surfaces with tunable adhesion for deterministic assembly by transfer printing," *Advanced Functional Materials*, vol. 22, no. 21, pp. 4476–4484, 2012.

[176] A. Carlson, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Transfer printing techniques for materials assembly and micro/nanodevice fabrication," *Advanced Materials*, vol. 24, pp. 5284–5318, 2012.

[177] B. Corbett, R. Loi, W. Zhou, D. Liu, and Z. Ma, "Transfer print techniques for heterogeneous integration of photonic components," *Progress in Quantum Electronics*, vol. 52, pp. 1–17, mar 2017.

[178] S. Kim, J. Wu, A. Carlson, S. H. Jin, A. Kovalsky, P. Glass, Z. Liu, N. Ahmed, S. L. Elgan, W. Chen, P. M. Ferreira, M. Sitti, Y. Huang, and J. A. Rogers, "Microstructured elastomeric surfaces with reversible adhesion and examples of their use in deterministic assembly by transfer printing," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 107, no. 40, p. 17095–17100, Oct. 2010.

[179] D. Jevtics, J. A. Smith, J. McPhillimy, B. Guilhabert, P. Hill, C. Klitis, A. Hurtado, M. Sorel, H. Hoe Tan, C. Jagadish, M. D. Dawson, and M. J. Strain, "Spatially dense integration of micron-scale devices from multiple materials on a single chip via transfer-printing," *Optical Materials Express*, vol. 11, no. 10, p. 3567, Oct. 2021.

[180] C. L. Panuski, I. Christen, M. Minkov, C. J. Brabec, S. Trajtenberg-Mills, A. D. Griffiths, J. J. D. McKendry, G. L. Leake, D. J. Coleman, C. Tran, J. St Louis,

J. Mucci, C. Horvath, J. N. Westwood-Bachman, S. F. Preble, M. D. Dawson, M. J. Strain, M. L. Fanto, and D. R. Englund, "A full degree-of-freedom spatiotemporal light modulator," *Nature Photonics*, vol. 16, no. 12, pp. 834–842, Dec. 2022, number: 12 Publisher: Nature Publishing Group. [Online]. Available: https://www.nature.com/articles/s41566-022-01086-9

[181] J. Yoo, K. Lee, U. J. Yang, H. H. Song, J. H. Jang, G. H. Lee, M. S. Bootharaju, J. H. Kim, K. Kim, S. I. Park, J. D. Seo, S. Li, W. S. Yu, J. I. Kwon, M. H. Song, T. Hyeon, J. Yang, and M. K. Choi, "Highly efficient printed quantum dot light-emitting diodes through ultrahigh-definition double-layer transfer printing," *Nature Photonics*, vol. 18, no. 10, pp. 1105–1112, Oct. 2024.

[182] D. J. John, D. Joannopoulos, J. N. Winn, and R. D. Meade, "Photonic crystals: molding the flow of light," *InPrinceton University of Press: Princeton, NJ, USA*, 2008.

[183] A. M. Shaltout, K. G. Lagoudakis, J. van de Groep, S. J. Kim, J. Vučković, V. M. Shalaev, and M. L. Brongersma, "Spatiotemporal light control with frequency-gradient metasurfaces," *Science*, vol. 365, no. 6451, p. 374–377, 2019.