Aluminium Oxide Prepared By UV/ozone Exposure For Low-Voltage Organic Thin-Film Transistors

by

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DECLARATION

This thesis is a result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of the degree.

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ABSTRACT

The novelty of this research lies in the development of a dry, ultra-thin gate dielectric based on an inorganic/organic bi-layer with a total thickness of up to ~ 20 nm. The inorganic layer is aluminium oxide formed by UV/ozone exposure of aluminium layers. The organic layer is 1-octylphosphonic acid prepared by vacuum evaporation. A fully-dry fabrication process has been developed and the low-voltage OTFT operation has been demonstrated. In addition, the preparation of the aluminium oxide has been optimized through its implementation into p-channel thin-film transistors based on thermally evaporated pentacene.

Results demonstrate that the UV/ozone exposure time primarily affects the threshold voltage of the transistors and the bias-stress induced shift in the threshold voltage. Both parameters improve when longer UV/ozone exposure times are implemented. Except for the lower field-effect mobility, the resultant transistor parameters are comparable to similar transistor structures reported to date using mixed wet-and-dry processes.

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LIST OF SYMBOLS AND ABBREVATIONS

AlO_x	Aluminium oxide
Al_2O_3	Aluminium (III) oxide
$BaTiO_3$	Barium titanate
BCB	Benzocyclobutene
BGBC	Bottom Gate Bottom Contact
BGTC	Bottom Gate Top Contact
BZT	Barium zirconate titanate
2C8-BTBT	2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene
C_{10}-DNTT	2,9-didecyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene
C_{13}-BTBT	2-tridecyl[1]benzothieno[3,2-b][1]-benzothiophene
$C_{22}H_{14}$	Pentacene
C_{60}	Fullerene
CDT-BTZ	Cyclopentadithiophene−benzothiadiazole
C_i	Capacitance per unit area
CuPc	Copper pthalocyanine
d	Dielectric thickness
DFHCO-4T	Carbonyl-functionalized quaterthiophene
diF-TEG ADT	Triethylgermylethynyl-substituted anthradithiophene
diF-TES ADT	2,8-difluoro 5,11-triethylsilylethynyl anthradithiophene
DNTT	Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene
DPP-DTT	N-alkyl diketopyrrolo-pyrrole:dithienylthieno[3,2-b]thiophene
DPP-PDVT	Poly[2,5-bis(alkyl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione-alt-5,5′-di(thiophen-2-yl)-2,2′-(E)-2-(2-(thiophen-2-yl)vinyl)

	thiophene]
$F_{16}CuPc$	Copper hexadecafluorophthalocyanine
HfO_2	Hafnium oxide
HMDS	Hexamethyldisilazane
HOMO	Highest Occupied Molecular Orbital
I_d	Drain current
I_g	Gate current
I_{on}	On-current
I_{off}	Off -current
I_{on}/I_{off}	On/off current ratio
IDT-BT	Indacenodithiophene benzothiadiazole
k	Relative permittivity (dielectric constant)
L	Channel length
$LaAlO_3$	Lanthanum aluminate
LUMO	Lowest Unoccupied Molecular Orbital
MIM	Metal Insulator Metal
n	Number of 15-Å thick aluminium layers
n-type	Electron carrier
NDI-$DTYM_2$	Naphthalene diimides fused with 2-(1,3-dithiol-2-ylidene)malononitrile groups
NDTs	Naphthodithiophene-based polymers
o-MeO-DMBI	2-(2-methoxyphenyl)-1,3-dimethyl-1H-benzoimidazol-3-ium iodide
8PA	1-octylphosphonic acid

ODPA	1-octadecylphosphonic acid
OTFT	Organic Thin-Film Transistor
OTS	Octadecyltrichlorosilane
p-type	Hole carrier
P_3HT	Poly(3-hexylthiophene)
PDBT-co-TT	Poly{2,2'-[(2,5-bis(2-octyldodecyl)-3,6-dioxo-2,3,5,6-tetrahydropyrrolo[3,4-c]pyrrole-1,4-diyl)]dithiophene- 5,5'-diyl-alt-thieno[3,2-b]thiophen-2,5-diyl}
PDMS	Polydimethylsiloxane
PF-TAA	poly(triarylamine)
PhO-OTS	(18-phenoxyoctadecyl)trichlorosilane
PMMA	Poly(methyl methacrylate)
PPO/PS	Polyphenyleneoxide/Polystyrene
PS	Polystyrene
PVP	Poly(vinyl phenol)
S	Subthreshold slope
SAM	Self-Assembled Monolayer
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
SZN	Strontium zirconate nickelate
t	Time (UV/ozone exposure or bias stress time)
Ta_2O_5	Tantalum pentoxide
TiO_2	Titanium dioxide
TGBC	Top Gate Bottom Contact

TGTC	Top Gate Top Contact
TIPS-PEN	6,13-bis(triisopropylsilylethynyl)pentacene
V_{ds}	Drain-source voltage
V_{gs}	Gate-source voltage
V_t	Threshold voltage
W	Channel width
YO_x	Yttrium oxide
ε_0	Vacuum permittivity
μ_p	Hole mobility

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PUBLICATIONS AND OUTPUTS

Patent application

1. Methods for Forming an Organic Layer on a Substrate. Inventors: University of Strathclyde (H. Gleskova, K. C. Chinnam and S. Gupta), WO2013021149A3.

Journal papers

1. **K.C. Chinnam**, S. Gupta, H. Gleskova, Aluminium Oxide Prepared by UV/ozone Exposure for Low-Voltage Organic Thin-Film Transistors, J. Non-Cryst. Solids **258** (2012), pp. 2512-2515. Presented at the 24th International Conference on Amorphous and Nanocrystalline Semiconductors (ICANS 24), Nara, Japan August 21-26, 2011.

2. **K.C. Chinnam**, H. Gleskova, Effect of Heat Treatment in Aluminium Oxide Preparation by UV/ozone Oxidation for Organic Thin-Film Transistors, Journal of Nanoscience and Nanotechnology **13** (2013), pp. 5182-5185. Presented at the European Materials Research Society (E-MRS) Spring Meeting, Strasbourg, France, 14-18 May 2012.

Conference proceeding

1. S. Gupta, **K.C. Chinnam**, M. Zelzer, R. Ulijn, H. Gleskova, Optimizing Pentacene Growth in Low-Voltage Organic Thin-Film Transistors Prepared by Dry Fabrication Techniques, Mat. Res. Soc. Symp. Proc. **1435** (2012), 6 p.

Invited talk

1. H. Gleskova, **K.C. Chinnam**, S. Gupta, Ultra-Thin, Inorganic-Organic Dielectric Bi-layers as Gate Dielectrics in Organic Thin-Film Transistors, International Conference on Progress in Applied Surface, Interface and Thin Film Science III, 14-18 May 2012, Florence, Italy.

Conference talk

1. H. Gleskova, **K.C. Chinnam**, S. Gupta, Gate Dielectric for Low-Voltage Organic Thin-Film Transistors, 24th International Conference on Amorphous and Nano-crystalline Semiconductors, 21–26 August 2011, Nara, Japan.

Conference posters

1. **K.C. Chinnam**, S. Gupta and H. Gleskova, Effect of UV/ozone Treatment Time on Pentacene Thin-Film Transistors, 10th International Summer School on Physics at Nanoscale, Devet Skal, Czech Republic, 30 May - 4 June 2011.
2. S. Gupta, **K.C. Chinnam**, M. Zelzer, R. Ulijn, H. Gleskova, Optimizing Pentacene Growth in Low-Voltage Organic Thin-Film Transistors Prepared by Dry Fabrication Techniques, Mat. Res. Soc. Spring Meeting, San Francisco, USA, 9-13 April 2012.
3. **K.C. Chinnam**, H. Gleskova, UV/ozone Formation of Gate Dielectric in Organic Thin-Film Transistors, European Materials Research Society (E-MRS) Spring Meeting, Strasbourg, France, 14-18 May 2012.

1 INTRODUCTION

1.1 OVERVIEW OF THE ORGANIC ELECTRONICS

Constructing the basic building blocks of complex electronic circuits with organic materials is referred to as organic electronics or plastic electronics or printed electronics. Electronics based on organic materials is often associated with attributes like flexible or stretchable, and large-area, printable or roll-to-roll fabrication. Consequently, organic electronics has been transforming the field of electronics that used to rely on rigid and inelastic electronic devices. It has been replacing these with lightweight, flexible and stretchable circuits fabricated at a much lower cost. Due to its ability to produce electronic devices with novel form factors and to tune various electronic properties, the field of organic electronics has progressed tremendously in the past two decades [1–20]. Compatibility of organic materials with a wide range of flexible substrates led to novel device applications. These range from electronic paper (i.e. flexible, paper-like display) and organic light-emitting displays to large-area solar cells, disposable electronics, sensors and RFID tags.

Organic materials, such as small molecules and polymers, are carbon and hydrogen based materials that are naturally compatible with existing plastic substrates. Organic materials can be synthesized and functionalised to provide conducting, semiconducting and insulating materials. In the last few decades

scientists have studied the electrical properties of various organic materials and explored their usage as functional materials in numerous electronic devices. These materials have been catalysing the field of organic electronics. These new materials have also urged researchers to develop new and cost effective fabrication techniques and revolutionize the device fabrication. Techniques such as printing, stamping, and molecular self-assembly are used to deposit a wide range of materials. Device fabrication on flexible substrates leads to roll-to-roll processing, which has been a backbone of the printing industry for printing high quality newspapers and magazines. Roll-to-roll processing of plastic electronics can employ printing or vacuum deposition techniques. This technology is entirely changing the fabrication of electronics in terms of production volume and cost.

The development of reliable organic electronic devices requires a better understanding of the material properties as well as comprehensive device studies and process optimization. Such combined studies enabled researchers to engineer materials with better optoelectronic properties and to fabricate electronic devices and circuits with improved performance characteristics [19]. Though there is a wider scope of innovation in device applications of the organic functional materials, these materials also have limitations. Device life time, durability and stability are lower for the organic devices when compared to their inorganic counterparts. Device degradation is mostly a result of the atmospheric, thermal and electrical effects applied during the device fabrication and operation.

Intensive research is on-going to develop materials for device encapsulation. Researchers are developing new, room-temperature material deposition techniques to reduce the thermal stress during the fabrication process as well as to develop efficient

encapsulants. Researchers have also been developing organic devices that require low operating voltages for portable, battery-powered applications. These low-voltage devices require downscaling of the implemented materials with no impairment to their properties.

Smart colour TVs and smart displays have emerged after voluminous cathode ray tubes (CRTs) were replaced by the flat panel displays. They were made possible by adding new functionality to the existing flat panel displays. Recently, this technology is being transferred to flexible plastic foils using electronic circuits made of organic materials [18], [21–24]. These ‘plastic’ displays are like sheets of plastic paper.

The depletion of the existing resources of fossil fuels and the carbon footprint generated by their usage has led scientists to develop alternative means of power generation and to introduce so called green technologies. Solar cells which harvest the light energy from the sun and convert it to electricity represent one of the most researched alternative methods. Large-area solar cells with high efficiency are of imminent interest. Here, organic materials play an increasingly important role. That is a result of rising solar cell efficiency, reduced production cost, ability to produce large-area devices, and a possibility to mount them on the walls and roof tops of the self-sustained buildings [25–30].

The field of medicine has progressed to newer heights after the electronic sensors and drug delivery devices have been introduced to monitor living tissues. Nowadays, the devices can be produced to manipulate or monitor the tiniest cells in the living organisms using the cutting edge technology. These devices need to be inexpensive and compatible with the living tissue. Organic materials [3], [31], [32]

naturally lend themselves for such biocompatible devices. Their low cost also allows producing disposable devices, i.e. they can be disposed of after the usage.

Sensors are the key components that monitor our surroundings to keep us safe in our day-to-day activities. If sensors can be produced in bulk at a low cost, their applications can be substantially broadened. Organic materials are an inexpensive substitute for the inorganic materials [33–39]. They could also be made into flexible or stretchable products which enables the mounting of the sensor arrays onto non-planar surfaces and into less accessible locations. RFID tagging is a technology most predominantly used for the identification and tracking in supermarkets, livestock, etc. The implementation of organic materials into these RFID tags leads to lighter and flexible tags produced at a lower cost [40–45].

To summarize, organic materials have changed the field of electronics by introducing new manufacturing approaches, novel devices and unusual form factors.

1.2 RESEARCH AIM OF THIS THESIS

A broad objective of this thesis was to develop low-voltage organic thin-film transistors (OTFTs) using dry fabrication techniques. The developed process should not use wet fabrication steps and should employ low-temperature processes compatible with plastic substrates and roll-to-roll processing. To fabricate transistors with low operating voltages, reliable, ultra-thin dielectrics are needed. This thesis presents low-voltage OTFTs based on pentacene and a dry, bi-layer gate dielectric consisting of aluminium oxide and 1-octylphosphonic acid. The preparation of the aluminium oxide by UV/ozone oxidation of an aluminium metal has been explored in depth and the process was optimized. To date, the ultra-thin aluminium oxide was

prepared by exposing aluminium metal to oxygen plasma. The results presented in this thesis show that UV/ozone oxidation provides an alternative path to plasma oxidation.

1.3 OUTLINE OF THE THESIS

This thesis presents the optimisation procedure of aluminium oxide prepared by UV/ozone oxidation. Chapter 1 introduces the field of organic electronics and presents the aim of this thesis and the thesis outline. Chapter 2 gives a detailed discussion of the state of the art of the OTFT technology – introducing the conjugated organic semiconductors, listing different OTFT structures and materials, explaining the OTFT operation, and discussing various OTFT fabrication techniques. From Section 2.4 onward, the focus is shifted to low-voltage OTFTs, describing the dielectric materials and fabrication techniques used to date. The aspect of OTFT electrical and environmental stability is reviewed in Section 2.5. Finally, Section 2.6 summarises the main objectives of this research.

Chapter 3 is devoted to the research methodology. Section 3.1 describes the deposition techniques and materials employed in the fabrication of metal-insulator-metal (MIM) and transistor structures. Section 3.2 explains the design of the shadow masks for the transistor fabrication. Section 3.3 describes the fabrication of the capacitor and OTFT structures, while Section 3.4 focuses on the electrical characterisation of these structures. Section 3.5 describes the extraction of various OTFT and capacitor parameters from current-voltage and capacitance measurements.

Chapter 4 presents various experiments related to the optimization of the aluminium oxide. It summarizes the results of various MIM structures implementing

aluminium oxide prepared by UV/ozone oxidation. Chapter 5 discusses the effect of UV/ozone exposure time on OTFT performance, while chapter 6 studies the role of thermal annealing during UV/ozonation of the aluminium. Chapter 7 describes the effect of the transistor channel length and channel width on the OTFT performance and chapter 8 presents the OTFT bias-induced instability as a function of the gate bias voltage. Finally, chapter 9 summarises the experimental findings and provides direction for the future research.

1.4 CONTRIBUTIONS

The main contributions of this research are:

- Design and demonstration of a fully dry fabrication process for low-voltage organic thin-film transistors with inorganic/organic dielectric bilayer.
- Development of gate dielectric based on aluminium oxide and 1-octyl phosphonic acid with thickness ranging from ~ 10 to ~ 20 nm.
- First demonstration and comprehensive optimization of UV/ozone oxidation of aluminium for low-voltage OTFTs.
- Study of the bias-induced instability of low-voltage OTFTs under very high gate-source/drain electric fields.

2 BACKGROUND

2.1 CONJUGATED ORGANIC SEMICONDUCTORS

The electronic configuration of carbon is $1s^2\ 2s^2\ 2p_x^1\ 2p_y^1\ 2p_z^0$. Every carbon atom forms three sp^2 hybridized orbitals. The p_z orbital is lying in the plane perpendicular to the plane of the sp^2 orbitals as shown in Figure 2.1a.

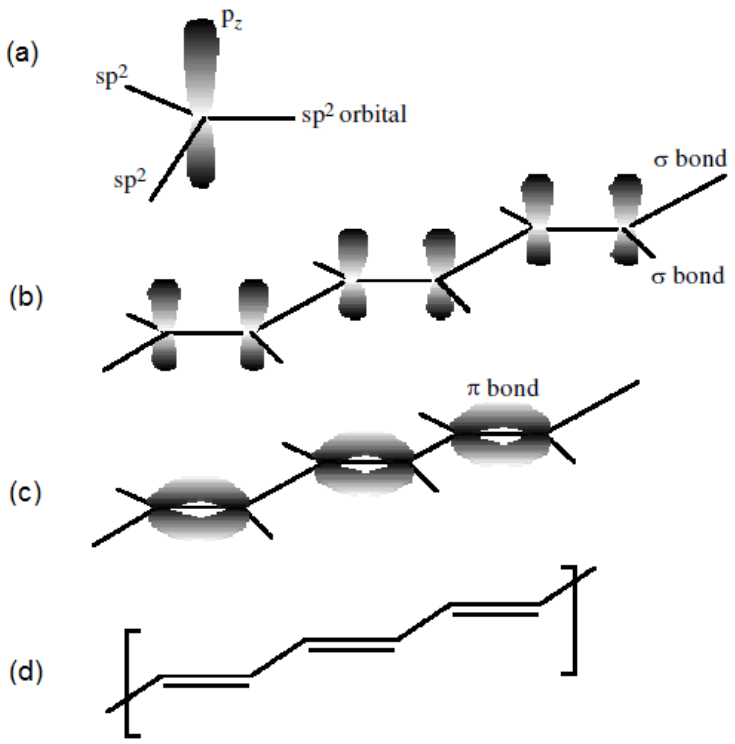

Figure 2.1. sp^2 and p_z orbitals in carbon atom (a), σ-bond with the adjacent carbon atoms in the molecular chain (b), π-bond formation (c), and conjugated structure of polyacetylene (d) [46].

Each sp^2 orbital can form a strong covalent bond with the sp^2 orbital of the adjacent carbon atom or with the s orbital of hydrogen atom. This is called σ-bond and it is shown in Figure 2.1b. The p_z orbital forms a weak π bond with the p_z orbital of the adjacent carbon atom, as shown in Figure 2.1c. This π bond creates π-bonding and π*-antibonding orbitals. The electron densities of these orbitals are located above and below the plane of the molecule and they are delocalized over the entire molecule, as shown in Figure 2.2 for a simple case of benzene.

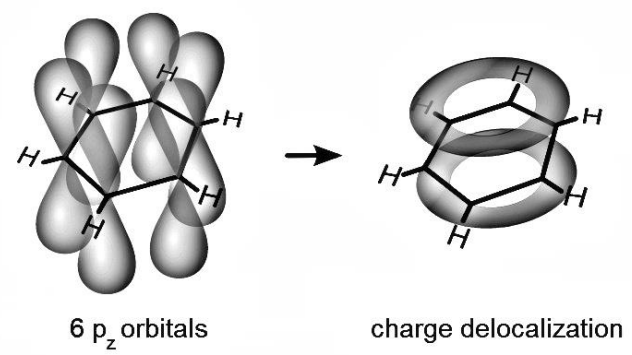

Figure 2.2. Charge delocalization above and below the plane of benzene.

Once all atoms in the molecule are bonded, they form a chain-like structure with alternating single and double bonds. The single bond is the σ bond and the double bond depicts the σ bond and the delocalized π bond, as shown in Figure 2.1d. The single bonds form the back bone of the molecular chains giving them the mechanical strength. Molecules having this type of alternating single and double bond chain structure are called conjugated molecules.

According to the Huckel's approximation of the molecular orbitals, only interactions between p_z orbitals of the nearest neighbours are considered. The electron-electron interactions are neglected and the molecular geometry and

symmetry are defined by the σ bonds. Using this approximation and the Pauli's exclusion principle the energy levels of the molecular π-orbitals can be calculated.

HOMO level is the Highest Occupied Molecular Orbital and LUMO level is the Lowest Unoccupied Molecular Orbital. As the number of carbon atoms in the molecular chain increases, the number of π-orbitals and the number of possible energy levels increases, leading to a decreased energy difference between the HOMO and LUMO levels. A perfect and infinitely long conjugated molecule should therefore have a partially-filled, one-dimensional energy band. However, Peirel's distortion breaks the symmetry of the system, lowers the overall energy and creates a gap between the HOMO and LUMO levels at the Fermi level. The band gap of the conjugated materials typically lies between 2 and 3.5 eV and their optical band gap lies in the visible spectrum.

The conjugated materials can be tailored for specific optical or electrical applications by altering their chain lengths and the side groups. Moderate mobility of the charge carriers allows their implementation in the field-effect transistors, their high-yield photoluminescence and electroluminescence make them attractive for light-emitting diodes, and their strong photon absorption in the visible part of the light spectrum is exploited in photovoltaic cells. Although the charge carrier mobility of these conjugated semiconductors is lower than that of crystalline silicon, they offer other advantages, e.g. compatibility with the plastic foils.

2.2 ORGANIC THIN-FILM TRANSISTORS

Organic thin-film transistors are the basic building blocks of any organic electronic circuit. Figure 2.3 shows an example of a unipolar, 3-terminal (source,

drain, and gate) structure of the organic thin-film transistor. Current flowing between the source and drain terminals of an OTFT can be modulated by the voltage applied across the isolated gate terminal. OTFT works on a similar principle as a parallel plate capacitor. However, compared to the parallel plate capacitor the OTFTs have an extra organic semiconducting layer between the plan-parallel source and drain contacts. This organic semiconductor layer leads to the formation of a conducting channel under the condition of charge carrier accumulation that enables conduction between the source and drain terminals. Depending upon the type of the semiconducting material used, the OTFTs can be p-type (hole-conducting) or n-type (electron-conducting).

OTFTs are used to switch, amplify and modulate the electrical signals. OTFTs have been implemented in the backplanes of flexible displays [21–24], sensors [33–39], RFID tags [40–45], and complementary logic circuits [47–49].

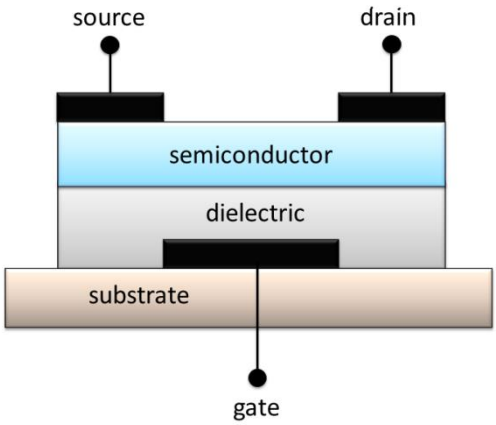

Figure 2.3. Organic thin-film transistor structure.

The following review papers depict the progress and the state-of-the-art of the OTFTs since they were first discovered [6], [24], [50–62]. OTFTs have emerged from amorphous silicon thin-film transistor technology in 1980s after the discovery of the organic semiconducting materials. Approximately within a decade organic

transistors with higher field-effect mobilities than amorphous silicon [63] were achieved. Initially OTFTs were not commercially interesting due to the instability and lower field-effect mobility. Consequently, a quest to find new organic semiconducting materials with better field-effect mobilities has started. References [49–61] discuss different materials and fabrication techniques developed for the OTFTs. In general, OTFTs can be divided into small molecule and polymer OTFTs, based on the type of the implemented conjugated semiconductor. Overall, small molecule OTFTs have shown better performance when compared to the polymer OTFTs. On the other hand, the polymers tend to be solution deposited, while the small molecule semiconductors are mostly vacuum deposited. Recently, the blends of small molecules and polymers and donor-acceptor polymers were introduced. More information about these is given in Section 2.2.2.

The key elements that hinder the OTFT performance are the defects at the interface between the semiconductor and the dielectric, the leakage current through the dielectric and the material work function mismatch. In the semiconductor layer the charge carriers are scattered and trapped due to the existing electronic traps, grain boundaries, etc. The growth of the semiconductor layer is controlled by the surface energy and the surface roughness of the underlying surface. The smoother the surface, the better is the film growth with well-defined grain boundaries. The dielectric material has to be very uniform with low leakage current, high breakdown voltage and high capacitance. Finally, the work function of the source/drain contacts should be matched to the HOMO (LUMO) of the organic semiconductor. Implementation of a new organic semiconductor or a dielectric material often requires complete re-optimization of the fabrication process.

This thesis focuses on the development of low-voltage, p-channel organic thin-film transistors with ultra-thin, dry, organic/inorganic bilayer gate dielectric. Current section briefly summarises the up-to-date progress in the field of OTFTs.

2.2.1 OTFT structure

Organic thin-film transistors are fabricated by depositing thin films of different materials on a substrate. The transistor structure comprises of insulating, semiconducting and conducting thin films that are sequentially deposited on a chosen substrate. Depending on the fabrication layer sequence, the organic thin-film transistors are classified as bottom gate, top contacts (BGTC), bottom gate, bottom contacts (BGBC), top gate, top contacts (TGTC) and top gate, bottom contacts (TGBC).

Since the organic semiconducting layers are soft and fragile, they are often deposited on the insulating layers. Their deposition the other way around is more difficult to perform and often results in transistors with lower carrier mobility. Many insulating materials (dielectric layers) form smooth surfaces which enables better grain formation in vacuum-deposited, organic semiconducting layers. A BGTC structure (Figure 2.4a) comprises of source and drain contacts deposited on top of the semiconducting layer, while the gate terminal is on the bottom of the structure and separated by the gate dielectric. This structure is relatively easy to fabricate as the top source and drain contacts can be created using shadow mask evaporation. In the case of the BGBC configuration (Figure 2.4b) the source and drain contacts are deposited on the dielectric layer. If the dielectric was inorganic then lithographic techniques could be employed to pattern the source and drain contacts, but it becomes more

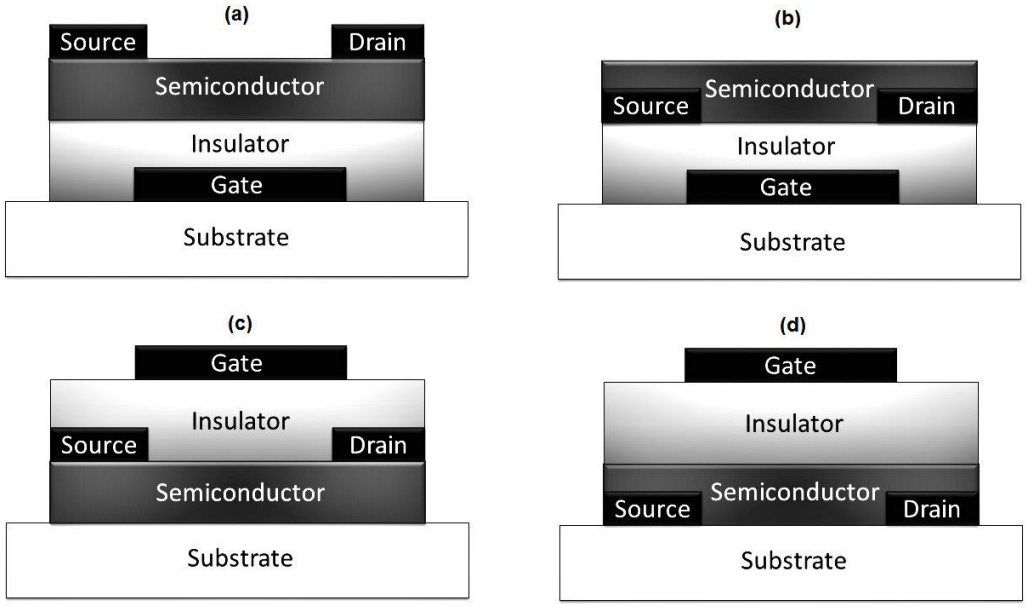

Figure 2.4. Organic thin-film transistor structures: bottom gate, top contacts – BGTC (a), bottom gate, bottom contacts – BGBC (b), top gate, top contacts – TGTC (c), and top gate, bottom contacts – TGBC (d).

challenging when organic dielectrics are employed because the solvents used during source/drain contact preparation can react with the underlying dielectric layer. TGTC configuration (Figure 2.4c) is an inverted structure of the BGBC configuration. In TGTC structure the gate electrode is deposited last on the top of the dielectric and the source and drain contacts are on top of the semiconductor. Finally, the TGBC structure is an inverted BGTC one. TGBC structure allows using the standard lithography (photo or e-beam) for forming the source/drain contacts and it is often used for OTFTs with short channel. In all four structures the source and drain contacts must be well aligned with the gate electrode.

BGBC and TGBC configurations create complications for the growth of the organic semiconductor. The source and drain contacts create surface topography and disrupt the grain formation of the growing organic semiconductor. BGTC structures are the most commonly used OTFT structures due to lesser complexity in laying

different layers on top of each other. This structure is also used in this project because the inorganic part of the bi-layer dielectric is prepared by a UV/ozone exposure of the gate metal (aluminium).

2.2.2 Semiconductor materials

Organic semiconductors exhibit conjugation as discussed in Section 2.1. Organic materials with high electron affinity typically function as n-type semiconductors and materials with high ionization potential function as p-type semiconductors. However, ambipolar conduction was also demonstrated in several organic semiconductors. Figure 2.5 shows the molecular structure of the common p- and n-type OTFT materials. These materials are often insoluble and chemically unstable. Functional end groups are added to their chemical structures to improve their solubility and stability. This ability to tailor the molecules through the addition of the groups is the key advantage of organic semiconducting materials. Table 1 lists several organic semiconductors and the corresponding OTFT field-effect mobilities. Since there are many organic semiconductor materials available, the quest to find materials with better environmental stability and higher charge carrier mobility is on-going.

Many different organic semiconductor materials are currently available [50], [53-54], [64–73], which can be broadly classified into: vacuum deposited small molecules, solution processed polymers, solution processed small molecules, single crystals, blends of polymers and small molecules, and donor-acceptor semiconductors. Solution processed polymers and vacuum deposited small molecules are the most common choice in the OTFTs. Historically the vacuum deposited

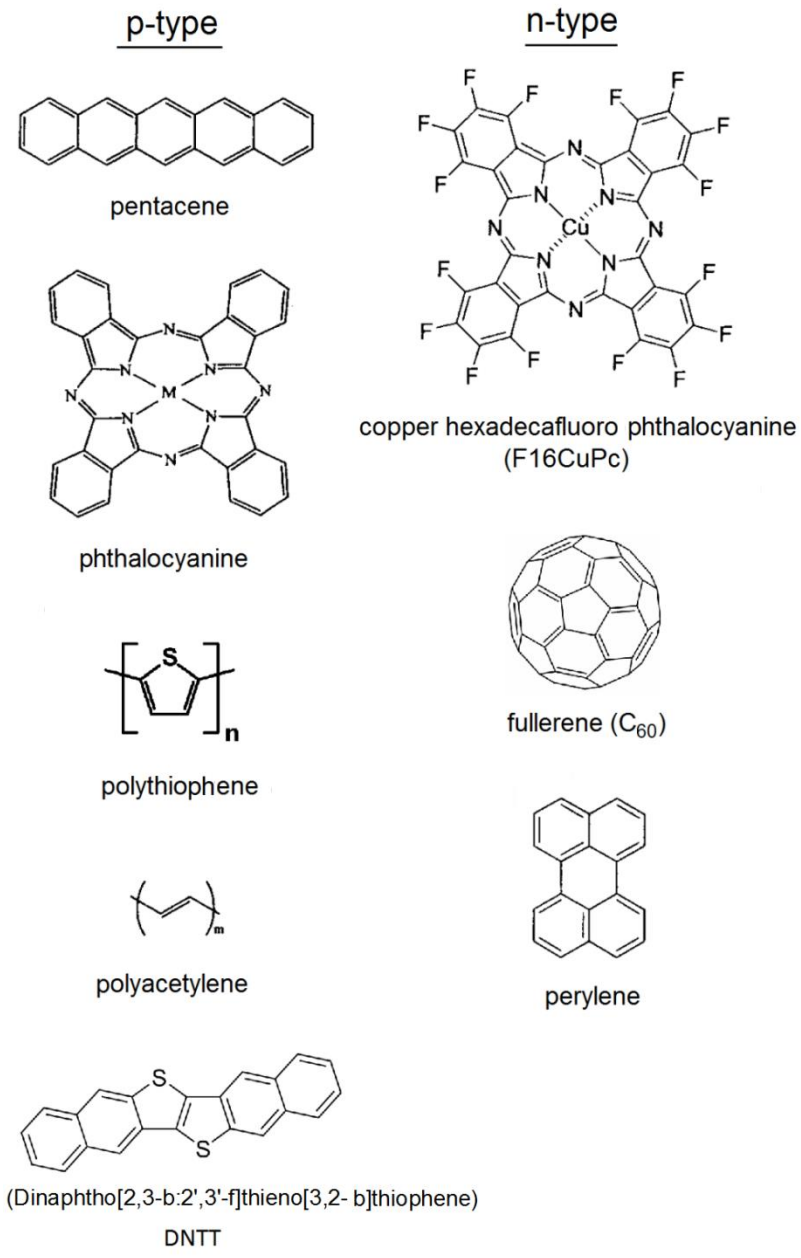

Figure 2.5. Common p- and n-type organic semiconductors.

small molecules have always led to OTFTs with higher field-effect mobility, when compared to solution deposited polymers. Consequently, polymer-small-molecule blends have been developed to take advantage of the field-effect mobility of small molecules and mechanical strength of the polymers. Ambipolar organic semiconductor materials based on the donor-acceptor copolymers were also

developed. These chemically engineered materials have reported relatively high field-effect mobilities for both p and n-channel OTFTs.

Table 1 summarizes the best OTFT field-effect mobilities achieved for different types of organic semiconductors. Vapour-deposited pentacene is the most studied small-molecule semiconductor in OTFTs, exhibiting the highest field-effect mobility of 23.2 cm^2/Vs [74]. Cyclopentadithiophenebenzothiadiazole copolymer is an example of the polymeric semiconductor reaching OTFT mobility of 1.4 cm^2/Vs [80]. Solution processed C_{10}-DNTT (2,9-didecyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene) reached the highest field-effect mobility of 11 cm^2/Vs [86] among all solution processed small molecule materials.

Single-crystal organic semiconductors are also available but they are more difficult to handle. Mobility of up to 40 cm^2/Vs [88] has been achieved for rubrene single crystals. Blend of polymer 2-(2-methoxyphenyl)-1,3-dimethyl-1H-benzo-imidazol-3-ium iodide and small molecule TIPS pentacene has the highest reported n-channel field-effect mobility 6.81 cm^2/Vs [93] among the polymer-small molecule blends. Among the donor-acceptor polymers n-alkyl diketopyrrolo-pyrrole: dithienylthieno[3,2-b]thiophene (DPP-DTT) exhibits the best p-channel field-effect mobility of 10.5 cm^2/Vs [97].

Table 2 lists the on/off current ratio, field-effect mobility, threshold voltage and subthreshold slope obtained for the OTFTs that have been fabricated using different organic semiconductors. It also lists how the semiconductor material was deposited and what OTFT structure was employed.

Figure 2.6 shows how the field-effect mobility of the p-channel and n-channel OTFTs has been improved in the recent years by introducing new materials

Table 1. Organic semiconductors and the corresponding OTFT mobility.

Organic Semiconductor	Mobility $cm^2/V\text{-}s$	Carrier type	Dielectric	Ref
Vacuum deposited small molecules				
Pentacene ($C_{22}H_{14}$)	23.2	p	silk fibroin	[74]
C_{13}-BTBT (2-tridecyl[1]benzothieno[3,2-b][1]- benzothiophene)	17.2	p	AlO_x/C_{14}-PA	[75]
DNTT (2,9-di-decyl-dinaphtho-[2,3-b:2′,3′-f]-thieno-[3,2-b]-thiophene)	8.5	p	$SiO_2/AlO_x/C_{14}$-PA	[76]
DFHCO-4T (carbonyl-functionalized quaterthiophene)	4.6	n	SiO_2/PαMS	[77]
CuPc (copper pthalocyanine)	0.5	p	CaF_2	[78]
F_{16}CuPc (copper hexadecafluorophthalocyanine)	0.2	n	SiO_2	[79]
Solution processed polymers				
CDT-BTZ (cyclopentadithiophenebenzothiadiazole copolymer)	1.4	p	SiO_2/PTES	[80]
IDT-BT (indacenodithiophene benzothiadiazole)	1.2	p	CYTOP	[81]
PDBT-co-TT Poly{2,2'-[(2,5-bis(2-octyldodecyl)-3,6-dioxo-2,3,5,6-tetrahydropyrrolo[3,4-c]pyrrole-1,4-diyl)]dithiophene-5,5'-diyl-alt-thieno[3,2-b]thiophen-2,5-diyl}	0.94	p	SiO_2/OTS	[82]
NDTs (naphthodithiophene-based polymers)	0.77	p	SiO_2/OTS	[83]
Tetrathienoacene copolymers	0.33	p	SiO_2/HMDS	[84]
P_3HT (poly(3-hexylthiophene))	0.2	p	SiO_2	[85]
Solution processed small molecules				
C_{10}-DNTT (2,9-didecyl-dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene)	11	p	SiO_2	[86]
TIPS-PEN (6,13-bis(triisopropylsilylethynyl)pentacene)	1.8	p	SiO_2/HMDS	[87]
Single crystal semiconductors				
Rubrene	40	p	SiO_2/silane	[88]
Pentacene	35	p	-	[89]
2C_8-BTBT (2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene)	31.3	p	SiO_2/parylene	[90]
Fullerene (C_{60})	11	n	SiO_2/BCB	[91]
TIPS-PEN (6,13-bis(triisopropylsilylethynyl)pentacene)	4.6	p	SiO_2/OTS	[92]
Polymer-small molecule blends				
o-MeO-DMBI 2-(2-methoxyphenyl)-1,3-dimethyl-1H-benzoimidazol-3-ium iodide) + TIPS PEN	6.81	n	SiO_2/BCB	[93]
diF-TES ADT:PF-TAA poly(triarylamine), poly(fluorene-co-triarylamine)	>5.5	p	CYTOP	[94]
diF-TEG ADT (Triethylgermylethynyl-substituted anthradithiophene)	5.4	p	SiO_2	[95]
diF-TES ADT (triethylsilylethynyl-substituted anthradithiophene)	1.5	p	SiO_2	[96]
Donor-acceptor polymers				
DPP-DTT (Diketopyrrolopyrrole (DBT)+Thieno[3,2-b]thiophene(TT))	10.5	p	SiO_2/silane	[97]
DPP-PDVT (poly[2,5-bis(alkyl)pyrrolo[3,4-c]pyrrole-1,4(2H, 5H)-dione- alt -5,5′-di(thiophen-2-yl)-2,2′-(E)-2-(2-(thiophen-2-yl)vinyl)thiophene]	8.2	p	SiO_2/OTS	[98]
NDI-DTYM2 naphthalene diimides fused with 2-(1,3-dithiol-2-ylidene)malononitrile groups	3.5	n	CYTOP	[99]
CDT-BTZ (Cyclopentadithiophene–benzothiadiazole)	3.3	p	SiO_2/HDMS	[100]

Table 2. Mobility and on-off current ratio (I_{on}/I_{off}) of OTFTs with various organic semiconductors. V stands for vapour deposition and S for solution processing.

Organic Semiconductor	(W/L)	μ ($cm^2/V.s$)	I_{ON}/I_{OFF}	V_t (V)	S V/dec	Dep	OTFT Structure	Ref
			Vacuum deposited small molecules					
Pentacene	12	23.2	3×10^4	-0.8	0.17	V	BGTC	[74]
C_{13}-BTBT	2	17.2	1.6×10^7	-2.7		V	BGTC	[75]
DNTT		8.5	10^7			V	BGTC	[76]
DFHCO-4T	15	4.6				V	BGTC	[77]
CuPc	50	0.5	2×10^2	-15	4	V	TGBC	[78]
F_{16}CuPc	35	0.2	6×10^4	5.5	1.1	V	BGTC	[79]
			Solution processed polymers					
CDT-BTZ	11	1.4	~10^5	10		S	BGTC	[80]
IDT-BT	33	1.2	~10^4	-25		S	TGBC	[81]
PDBT-co-TT	10	0.94	~10^6	-25		S	BGTC	[82]
NDTs	30	1.5	10^7			S	TGBC	[83]
Tetrathienoacenes		0.33	>10^5	-15		S	BGTC	[84]
P_3HT	200	0.2	4×10^2	-37		S	BGBC	[85]
			Solution processed small molecules					
C_{10}-DNTT	3	11	3×10^6			S	BGTC	[86]
TIPS-PEN		1.8	>10^7	-3.4	0.3	S	BGBC	[87]
			Single crystals					
Rubrene	5	40				V	BGBC	[88]
Pentacene		35						[89]
$2C_8$-BTBT	1	31.3	10^7	-10	2	S	TGTC	[90]
Fullerene	20	11	2×10^6	28		S	BGTC	[91]
TIPS-PEN	20	4.6	10^7	-20		S	BGTC	[92]
			Polymer-small molecule blends					
o -MeO-DMBI + TIPS-PEN	20	6.8	~10^6	55		S	BGTC	[93]
diF-TES ADT:PF-TAA	14	>5.5	> 10^6	-5	2	S	TGBC	[94]
diF-TEG ADT	40	5.4	10^6			S	BGBC	[95]
diF-TES ADT	22	1.5	>10^6	-20	0.4	S	BGBC	[96]
			Donor-acceptor polymers					
DPP-DTT	28	10.5	≥10^6	-6	1	S	BGBC	[97]
DPP-PDVT	28	8.2	~10^7	-5	0.5	S	BGBC	[98]
NDI-DTYM2	110	3.5	8×10^8	2		S	BGBC	[99]
CDT-BTZ	70	3.3	10^6	-15		S	BGBC	[100]

and fabrication techniques. Charge carrier mobility is the most important electrical property of the semiconductors with respect to OTFTs.

Not counting the single-crystal materials, the vacuum grown p-type small-molecule organic semiconductors exhibit the highest charge-carrier mobility reported

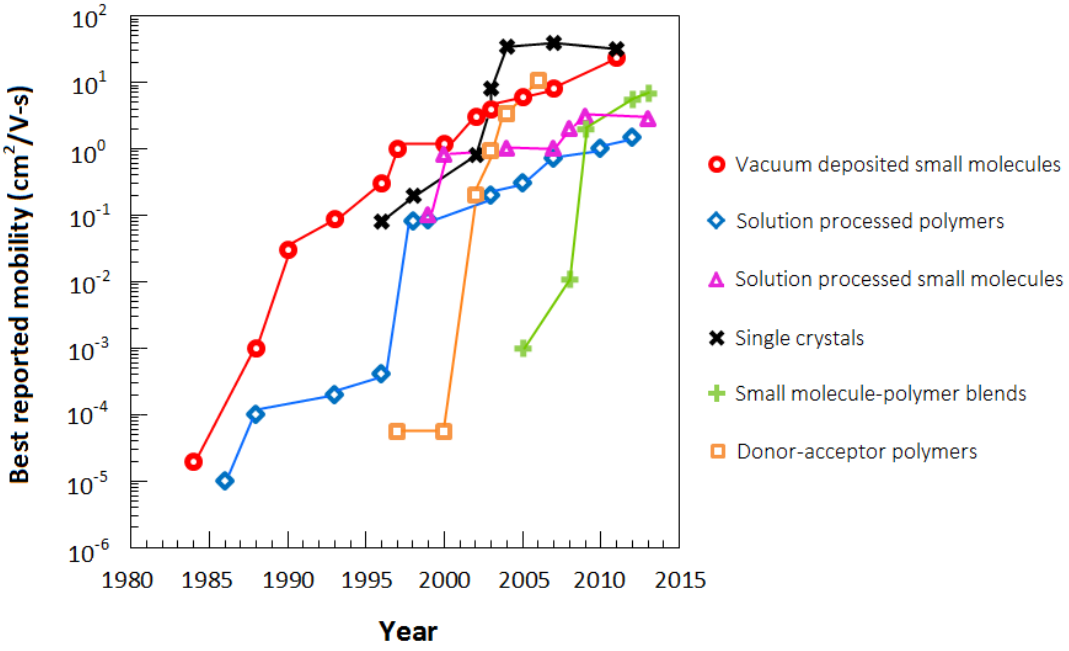

Figure 2.6. Evolution of the charge carrier mobility of different types of organic semiconductors [50], [74-100].

to date for organic semiconductors. The field-effect mobility of pentacene is 23.2 cm^2/Vs [74], which is higher than the field-effect mobility of 0.1 to 1 cm^2/Vs achieved for amorphous silicon transistors. Consequently, pentacene is the most widely used organic semiconductor in OTFTs and OTFT applications. The OTFTs studied in this thesis are based on pentacene due to its commercial availability, high mobility and vacuum deposition technique. The disadvantage of pentacene is its degradation in the air caused by the oxidation of its middle benzene ring. This has been overcome by adding side chains to the middle ring (e.g. TIPS-pentacene) or replacing it with two thiophenes (e.g. DNTT).

The performance of the OTFTs is controlled by the first few monolayers of the semiconductor layer at the semiconductor/dielectric interface. This region has to be trap and defect-free. To minimize the density of these electronic traps, suitable combination of the semiconductor and dielectric as a well as smooth and uniform dielectric layer are required [101].

2.2.3 Gate dielectric materials

Gate dielectric materials are as important as the semiconductors for the OTFTs. Low leakage current, high breakdown voltage and high capacitance are the main criteria of an ideal gate dielectric. Leakage current is the current that passes through the dielectric material along the defects and localized states. No dielectric material is a perfect electrical insulator and there is always some current flowing through the dielectric – this current must be as low as possible. Breakdown voltage (electric field) is the voltage (electric field) at which the dielectric undergoes an irreversible failure and loses its electrically insulating properties. Parallel-plate capacitance of the dielectric is higher if the dielectric is thinner and/or its relative permittivity (dielectric constant) is higher. Bearing these requirements in mind, several dielectrics have been tested in OTFTs while often compromising some of these requirements. The gate dielectric materials implemented in OTFTs to date can be divided into inorganic or organic dielectrics, self-assembled monolayers (SAMs), and multilayer dielectrics. A detailed discussion of the dielectric materials in OTFTs has been presented in several review articles [55, 102-104].

Inorganic dielectrics are typically oxides or nitrides of inorganic elements, such as silicon dioxide, silicon nitride, aluminium oxide, etc. Since single-crystal silicon wafers are readily available, many OTFTs employed thermally grown silicon dioxide as the gate dielectric. Although low-temperature deposition processes for silicon dioxide, e.g. ion-beam sputtering and chemical vapour deposition, exist, the disadvantage of the silicon dioxide is its low relative permittivity of 3.9. Highest OTFT field-effect mobility of ~ 10 $cm^2/V.s$ was reported for pentacene OTFTs when strontium zirconate nickelate (SZN) dielectric was prepared by sol-gel technique.

[105]. Table 3 lists the inorganic dielectric materials employed for OTFTs including their preparation, the highest field-effect mobility, on/off current ratio and organic semiconductor. The table also lists the thickness (*d*), capacitance per unit area (C_i), relative permittivity (*k*) and the electric breakdown field (E_B) for each dielectric (where available).

Table 3. Inorganic dielectrics.

Dielectric	Method	d (nm)	C_i (nF/cm^2)	*k*	E_b (MV/cm)	Semicond.	μ cm^2/V.s	I_{on}/I_{off}	Ref
Inorganic									
SZN	sol-gel	120	59.30	8.05		Pentacene	10.04	~10^4	[105]
$BaTiO_3$	Spin coat	250	55.12	15.57		Pentacene	8.85	>10^3	[106]
BZT	Spin coat	180	58.30	11.85		Pentacene	7.31	10^5	[107]
SiO_2	Sol-gel	104	67.26	7.5		Pentacene	6.3	>10^5	[108]
HfO_2	Sol-gel	190	52	11		Pentacene	3.8	10^2	[109]
$LaAlO_3$	PLD	330		15	6	Pentacene	1.4	10^7	[110]
AlO_x	PLD	330		9	7	Pentacene	0.6	10^4	[110]
Si_3N_4	sputt.	100	66				~0.6		[111]
Ta_2O_5	e-beam		245			Pentacene	0.45	~10^2	[112]
TiO_2	anodiz.	30	676			Pentacene	0.15		[113]

Organic/polymer dielectrics are a cost effective substitute for inorganic dielectrics due to their simpler deposition techniques like spin coating, spray coating, printing and polymerisation. To date most organic dielectrics have been solution processed (spin coated or ink-jet printed); a few have been vacuum deposited. Polymer dielectrics for OTFTs should be smooth, chemically compatible with other OTFT materials and stable. Some of the common examples of polymer dielectrics are poly(methyl methacrylate) (PMMA), polyimide, poly(vinyl alcohol) (PVA), and polyvinyl phenol (PVP). Table 4 lists some of the most common organic/polymeric dielectrics employed in OTFTs. However, the major drawback of many polymer dielectrics is either their low relative permittivity or low electric breakdown field.

The highest field-effect mobility 23.2 $cm^2/V.s$ was reported for pentacene OTFT's with spin coated silk fibroin dielectric.

Table 4. Organic dielectrics. SC stands for spin-coated.

Dielectric	Method	d (nm)	C_i (nF/cm^2)	*k*	E_b (MV/cm)	Semicond.	μ $cm^2/V.s$	I_{on}/I_{off}	Ref
Organic/polymeric									
Silk fibroin	SC	420	17.5	6.1		Pentacene	23.2	3×10^4	[74]
CYTOP						diF-TES ADT: PF-TAA	>5.5	$>10^6$	[94]
PPO/PS		30					3.6		[114]
Cross-linked PVP	SC	260		3.6		Pentacene	3	10^5	[115]
Copolymer PVP	SC	380		4		Pentacene	2.9	10^5	[115]
Polyimide	SC	600					2.4	10^7	[116]
PVA	SC	860		8.3			1.48	$\sim10^4$	[117]
PVP Photo patterned	SC					Pentacene	1.23	10^7	[118]
PS	SC	~700		2.5		P(NDI2OD-T2)	~0.3	$\sim10^8$	[119]
PMMA	SC	560	5.06	3.2		Pentacene	0.153	$\sim10^4$	[120]
PVP	SC	440		4.2		Pentacene	0.1	10^3	[121]

While several inorganic dielectrics have high relative permittivity and low leakage current, their preparation requires higher growth temperature and patterning techniques based on photolithography. Their growth on plastic foils is also challenging. In addition, their surface is hydrophilic with high surface energies. This affects the morphology of the growing organic semiconductor in the bottom gate OTFTs. The organic dielectrics, on the other hand, employ low temperature deposition methods and offer natural compatibility with plastic foils. Their relative permittivity and surface energy vary. Consequently, they are an attractive substitute for the inorganic counterparts.

Hybrid dielectrics are a combination of organic and inorganic dielectrics which aim to exploit the best of both types of materials, e.g. high dielectric constant and compatibility with the organic semiconductor. This category of dielectrics can be

sub-divided into polymer-nanoparticle composites and inorganic/organic bilayer dielectrics. Table 5 lists the hybrid dielectrics which reported the best OTFT field-effect mobility until date. The highest OTFT field-effect mobility of 1.3 $cm^2/V.s$ was reported for pentacene-based OTFTs with PS-TiO_2 polymer nano-composite dielectric [122] and 10.5 $cm^2/V.s$ was reported for DPP-DTT based OTFTs with SiO_2/OTS inorganic/organic bilayer dielectric [97].

Table 5. Hybrid dielectrics.

Dielectric	Method	d (nm)	C_i (nF/cm^2)	*k*	E_b (MV/cm)	Semicond.	μ $cm^2/V.s$	I_{on}/I_{off}	Ref
Polymer-Nanoparticle Composite									
PS-TiO_2	SC	~1200		8.2		Pentacene	1.3	10^3	[122]
Polyimide-Ta_2O_5	SC			5.5			0.38	10^5	[123]
SM-Al_2O_3 +PVP	SC	290		7.2		Pentacene	~0.25	~10^3	[124]
cross-link PVP +TiO_2	SC	700		5.4		Pentacene	0.24	10^3	[125]
SM-TiO2 +polyimide	SC	~500		~4		Pentacene	~0.18	6×10^5	[126]
SM-$BaTiO_3$ +PVP	SC	406	31	14		Pentacene	0.04	6×10^4	[127]
Inorganic/Organic Bilayer									
SiO_2/OTS	Thermal/ SC					DPP-DTT	10.5	10^5	[97]
Al_2O_3/CEP	ALD/SC	160+5	85	9/14		Pentacene	5.02	>10^5	[128]
AlOx/14PA	O_2 plasma /DC	3.6+1.7	800			C_{10}-DNTT	4.3	10^8	[129]
Al_2O_3/ cross-link BCB	ALD/SC	100	50		>3	C_{60}	~2.5	~10^6	[130]
HfO_2/8PA	sol-gel/DC	8+1	583			Pentacene	~1.8	~10^6	[131]
PVP/YO_x		45+50	70.8	3.7/14.6	~2	Pentacene	1.74	10^4	[132]
PhO-OTS		2.5	900		14	Pentacene	1.0	~10^4	[133]
Ta_2O_5/PMMA	e-beam/ SC	80+37	63.5			Pentacene	0.68	~10^6	[134]
Al_2O_3/PMMA	anodi./SC	60+160	11.2			Pentacene	0.31	~10^6	[135]
HfO_2/ODPA	sol-gel	3.1	560			C_{60}	0.28	~10^5	[136]
SiO_2/ cross-link PVA	PECVD/SC	950+350				Pentacene	0.12	~10^6	[137]

Multilayer dielectrics with highest OTFT field-effect mobility are presented in Table 6. Thickness of the multilayer dielectrics can be scaled depending on the device requirement. Multilayers are prepared by depositing stacked ultra-thin layers of organic or inorganic materials, or by a combination of several organic dielectric materials. The highest field-effect mobility 3.6 $cm^2/V.s$ was reported for DHFCO-4TCO-based OTFTs with SAND/SiO_x multilayer dielectric [138].

Table 6. Multilayer dielectrics.

Dielectric	Method	d (nm)	C_i (nF/cm^2)	*k*	E_b (MV/cm)	Semicond.	μ $cm^2/V.s$	I_{on}/I_{off}	Ref
Multilayers(Organic-Organic/Inorganic)									
v-SAND/SiO_X	VSA/VD	25.4	185	10.1/3.9		DHFCO-4TCO	3.6	10^4	[138]
Silane/TiO_2	MLD/ALD	100		17		Pentacene	1.3	>500	[139]
SAMT-III	SP	5.5	390		6-7	DH-6T	0.06	~10^3	[140]

2.2.4 Electrode materials

Three OTFT electrodes perform different functions in the transistor. While the gate electrode serves to form a conducting channel at the semiconductor/ dielectric interface through a capacitive charge accumulation, the source electrode injects charge into one side of the channel and the drain electrode collects this charge on the other side of the channel. Therefore, the choice of material for the source/drain contacts and a reduction of the contact resistance between the semiconductor and the source/drain electrodes become crucial. Consequently, to minimize the energy barrier between the metal and the semiconductor, metals having work function close to the HOMO level of the semiconductor are used for p-type semiconductors and metals with work function matching the LUMO levels are used for n-type organic semiconductors.

Gold is the most common source/drain electrode material used to date due to its work function matching the energy levels of many organic semiconductors. In addition, gold has high electrical conductivity and it does not oxidize. The only drawback of gold is its price. Other high work function materials like palladium [141] and indium tin oxide [142] have been implemented in p-channel OTFTs. In BGBC and TGBC transistors structures the gold electrodes are sometimes function-

alized with self-assembled monolayers to improve the charge injection into the organic semiconductor [143]. Silver can be used as a cost effective replacement for gold but its conductivity is lower and the material is prone to oxidation. Transitional metal oxides like copper oxide and molybdenum oxide have been implemented in OTFTs and they reported reasonably good transistor performance [144]. These materials could replace gold in the near future to reduce OTFT production cost. Low-cost solution-processed gold or silver nanoparticles thermally cured at 200°C were also implemented in OTFTs. Carbon nanotubes and conducting polymers provide another path for the electrode formation in OTFTs.

Transistors presented in this thesis use gold for the source and drain contacts and aluminium as the gate electrode. Gold was selected due to its compatibility with pentacene which is the chosen semiconductor in our OTFTs.

2.2.5 OTFT operation

Organic thin-film transistors are three-terminal electronic devices. As shown in Figure 2.7 when voltage is applied to the gate electrode of an OTFT, charges of the opposite polarity are induced in the semiconductor layer near the semiconductor/dielectric interface. This is called charge accumulation. The accumulated charge forms a narrow conducting channel between the source and drain electrodes. When the voltage is applied between the source and drain terminals, the current flows between them.

The current flowing from the source to the drain can be controlled by the voltage applied on the gate terminal. Figure 2.7 represents the operation of a typical

p-channel OTFT. The n-channel OTFT works on the same principle. In this case, however, positive voltage is applied to the gate and drain electrodes, leading to an electron accumulation in the transistor channel.

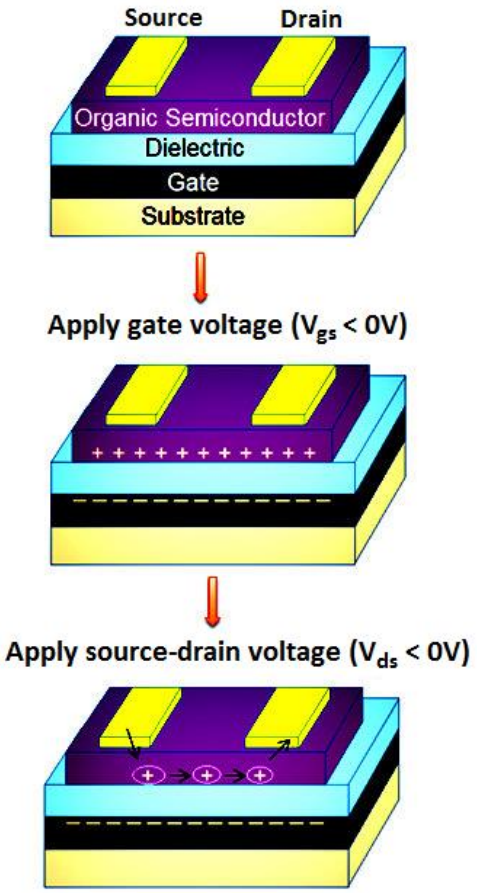

Figure 2.7. Schematic representation of OTFT operation.

Figure 2.8 represents the energy level diagram of the dielectric/semiconductor interface when large enough gate voltage is applied. Positive charge is accumulated close to the HOMO level of the semiconductor when negative gate-source voltage is applied to p-channel OTFT. Negative charge is accumulated close to the LUMO level of the semiconductor for n-channel OTFT when positive gate-source voltage is applied. Figure 2.9 represents the energy level diagram along the conducting channel of the OTFT. The picture shows how the positive charge flows from the

source terminal through the semiconductor (in the vicinity of the HOMO level) into the drain for p-channel OTFT and a negative drain-source voltage. There is a large energy barrier for the negative charge to flow in the vicinity of the LUMO level. For the n-channel OTFT the negative charge flows from the source electrode, near the LUMO level of the semiconductor, and into the drain when positive drain-source voltage is applied. Due to the large energy barrier between the Fermi level of the drain contact and the HOMO level of the semiconductor layer the mobility of the positive charge is restricted.

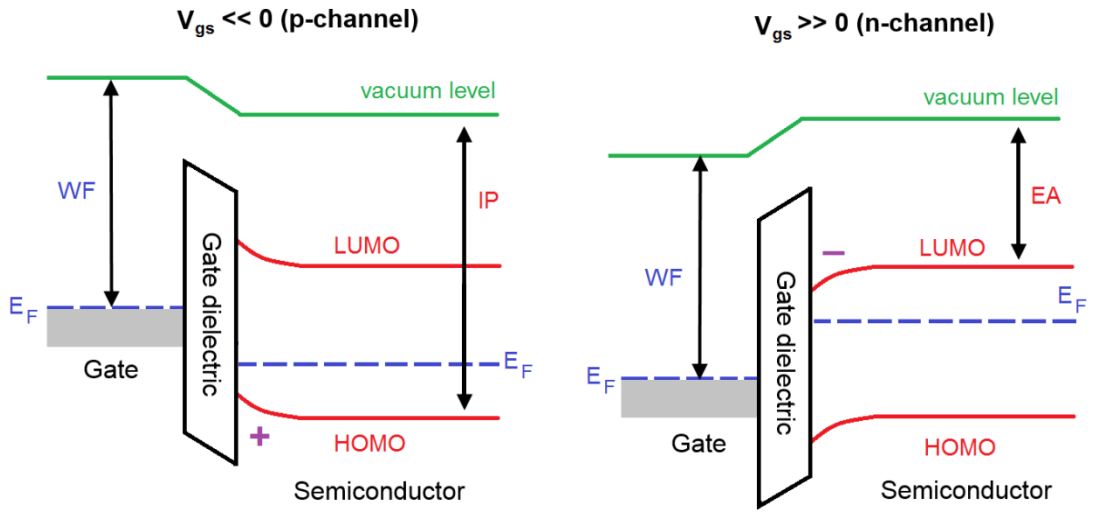

Figure 2.8. Energy level diagram of a dielectric-semiconductor interface of p-type and n-type OTFTs. E_F is the Fermi level, WF is the metal work function, EA is the electron affinity and IP is the ionization potential [50].

Figure 2.10 shows an example of output and transfer characteristics of low-voltage p-channel OTFT. When $V_{gs} \geq 0$, the drain current is very small and the transistor is in the OFF state. When $V_{gs} \leq 0$ is applied on the gate terminal and V_{ds} of −1.5 V is applied to the drain terminal, the current increases by many orders of magnitude and the transistor is turned ON. When $|V_{ds}| < |V_{gs} - V_t|$ where V_t is the threshold (turn-on) voltage of the transistor, the transistor is said to be in the linear regime. When $|V_{ds}| > |V_{gs} - V_t|$ the channel is pinched off near the drain contact

and the drain current reaches saturation. The linear and the saturation regimes are clearly visible in the transistor output characteristics.

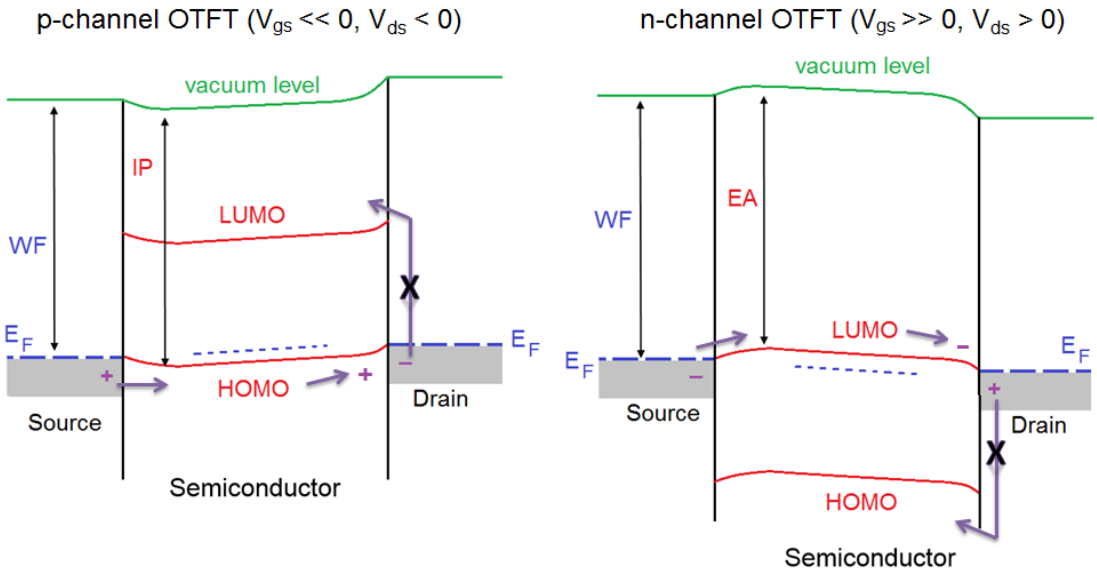

Figure 2.9. Energy level diagram along the channel of p-type and n-type OTFTs [50].

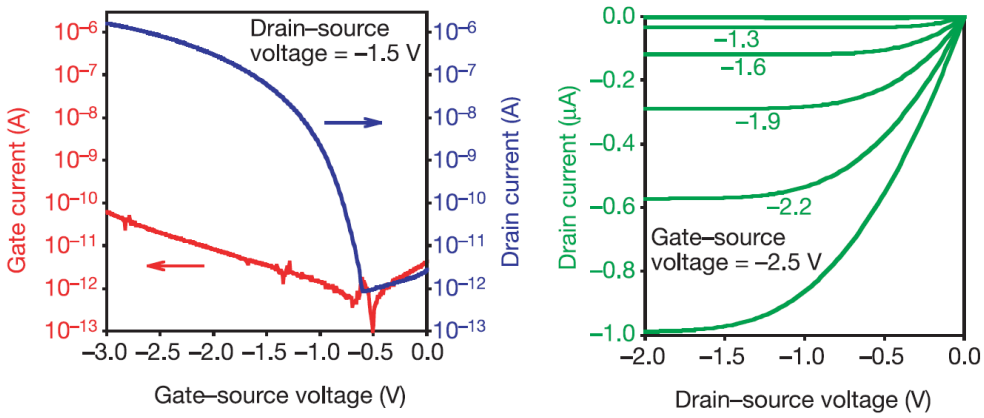

Figure 2.10. OTFT transfer (left) and output (right) characteristics [133].

High semiconductor field-effect mobility, high ON/OFF drain current ratios, low threshold voltages, low dielectric leakage currents, sharp subthreshold slopes and low contact resistance are the major requirements for OTFTs. As mentioned before, semiconducting materials with high carrier mobility are desired because they lead to faster transistors.

The current-voltage behaviour of OTFTs is typically described by MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) equations, even though organic thin-film transistors operate slightly differently when compared to the traditional, crystalline silicon transistors. In silicon transistors charge inversion leads to the channel formation whereas charge accumulation is responsible for the channel formation in organic thin-film transistors. In organic thin-film transistors the type of channel formed (electron-rich or hole-rich) depends on the semiconductor layer and the work function of the source-drain metal.

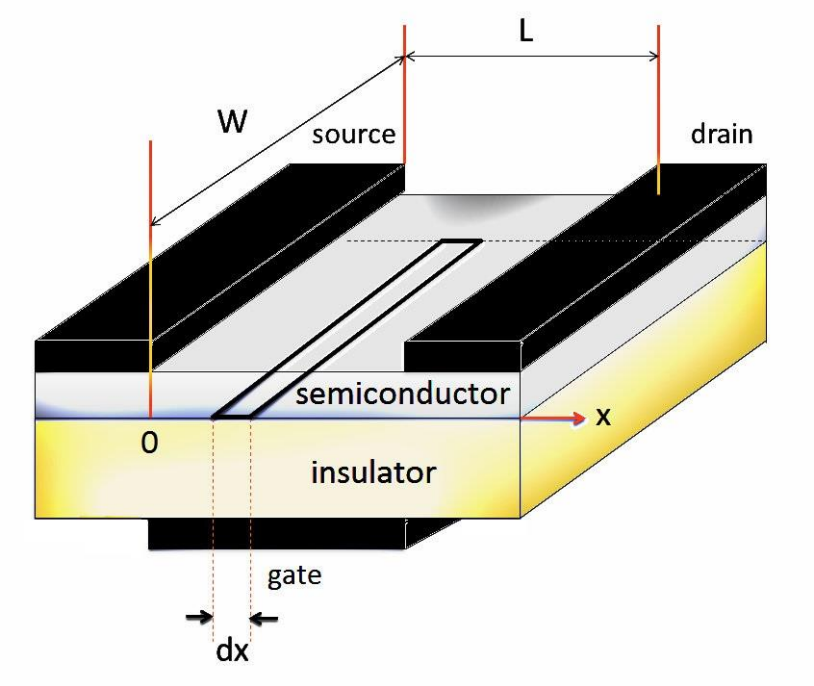

Figure 2.11. OTFT dimensions.

An application of the gate-source voltage higher than the threshold voltage causes charge accumulation in the channel region of the OTFT. This accumulated charge manifests itself as a measurable drain current upon the application of the drain-source voltage. This drain current can be derived by estimating the charge induced in the channel region of the OTFT. In Figure 2.11 the charge dq induced by

gate voltage V_{gs} in an elemental strip of width dx located at a distance x from the source is:

$$dq = 0 \quad \text{for } |V_{gs}| < |V_t|$$

$$dq = -C_i \left[V_{gs} - V_t - V(x)\right] W dx \quad \text{for } |V_{gs}| > |V_t| \tag{1}$$

where W is the channel width, C_i is the capacitance per unit area of the gate dielectric ($C_i = \frac{\varepsilon_0 k}{d}$, where ε_0 is the permittivity of vacuum, and k and d is the relative permittivity and thickness of the gate dielectric, respectively), Wdx is the area of the elemental strip, V_t is the threshold voltage and $V(x)$ is the potential in the channel at a position x induced by the drain bias voltage. $V(x)$ = 0 at the source and $V(x)$ = V_{ds} at the drain. The negative sign indicates that the charge accumulated in the channel region is of the opposite sign to the applied gate voltage. Drain current I_d arises due to the flow of charges from source to drain electrodes. In the case of the elemental strip shown in Figure 2.12 the drain current is given as:

$$I_d = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt} \tag{2}$$

Charge carrier mobility μ is defined as the ratio of the mean velocity $v = dx/dt$ of the carriers to the electric field $E = -dV/dx$ in which the carriers move. By substituting $dx/dt = -\mu(dV/dx)$ in Equation (1) one gets:

$$I_d\, dx = W\, C_i\, \mu \left[V_{gs} - V_t - V(x)\right] dV \tag{3}$$

To obtain the drain current along the entire channel of the OTFT, Equation (3) is integrated from source (x=0, $V(x) = 0$) to drain (x= L, $V(x) = V_{ds}$), while assuming constant mobility and a linear increase in V_{ds} from the source to the drain:

$$\int_0^L I_d \, dx \; = \int_0^{V_{ds}} W \, C_i \, \mu \left[V_{gs} - \, V_t - V(x) \right] dV \qquad (4)$$

These assumptions are reasonable in the linear regime where $|V_{ds}| < |V_{gs} - \, V_t|$. Equation (4) leads to the following expression for the transistor drain current in the linear regime of the operation.

$$I_d \; = \frac{W}{L} \, C_i \, \mu \left(V_{gs} - \, V_t - \frac{V_{ds}}{2} \right) V_{ds} \qquad (5)$$

If $\frac{V_{ds}}{2} \ll V_{gs} - \, V_t$, Equation (5) can be rewritten into the more familiar repression:

$$I_d \; = \frac{W}{L} \, C_i \, \mu \left(V_{gs} - \, V_t \right) V_{ds} \qquad (6)$$

showing a linear increase in the drain current with increasing drain voltage.

As V_{ds} increases further, dq next to the drain becomes gradually smaller (see Equation (1)). When $V_{ds} = \, V_{gs} - \, V_t$, dq becomes zero. This is called the pinch off point of the OTFT. Further increase in the V_{ds} shifts the pinch off point towards the source. Since the potential at the pinch off point remains constant at $V_{gs} - \, V_t$, the drain current becomes independent of drain voltage. Therefore any further increase in V_{ds} beyond $V_{gs} - \, V_t$ does not affect the drain current of the OTFT and the OTFT is in the saturation regime. The drain current in the saturation regime is obtained by substituting $V_{ds} = \, V_{gs} - \, V_t$ in equation (5), leading to a quadratic expression:

$$I_d \; = \frac{W}{2L} \, C_i \, \mu \left(V_{gs} - \, V_t \right)^2 \qquad (7)$$

The current-voltage characteristics of the OTFT are obtained by measuring the transfer and output characteristics which show the effect of V_{gs} and V_{ds} on the OTFT

drain currents (see Figure 2.10). Equations (6) and (7) are used to extract the OTFT parameters in the linear and saturation regimes as demonstrated in the Section 3.5.

2.3 OTFT FABRICATION

OTFTs are fabricated by a sequential deposition of different functional materials onto a substrate. Organic materials, especially semiconductors used in OTFTs, have very different properties, e.g. solubility and melting point, when compared to inorganic materials. Initially, many OTFTs have been prepared on silicon substrates using conventional fabrication techniques like photolithography and thermal oxidation. But these processes are not compatible with the low melting point of plastic substrates. To fabricate OTFTs on flexible substrates new material deposition techniques had to be developed. The processes employed to fabricate OTFTs are broadly divided into wet and dry. Historically, wet and dry processes have been mixed during the OTFT fabrication. As mentioned above, organic semiconductors are broadly divided into polymers and small molecule materials. Polymers possess good solubility and therefore are often wet/solution processed. Small molecule materials on the other hand are mostly vacuum deposited. The deposition methods of the other OTFT layers are often chosen based on the established procedures, existing equipment, and material compatibility. Depending on the desired OTFT channel geometries, the electrodes can be prepared by shadow mask evaporation, patterning using lithography or by various printing techniques. The dielectric layers are either solution or dry processed; the selected method often depends on the chosen material. The following papers present a detailed overview of the OTFT fabrication methods [24], [54], [56], [58].

2.3.1 Printing/wet processing

OTFTs employing polymer semiconductors take advantage of wet processing techniques such as spin coating [145], drop casting [146], inkjet printing [147], screen printing [148], micro contact printing [149] and photolithography [150]. Spin coating requires covering the substrate with a few drops of a liquid material and applying a centripetal force to attain a desired thickness of the film. Spin coating is a simple method that produces uniform films with good reproducibility. Its disadvantage is material waste, difficulty to cover large areas and a limited control of the layer thickness and device geometry. Drop casting relies on the application of a few drops of the liquid material onto a substrate and a subsequent evaporation of the solvent to produce thin film. Such films, although produced in desired locations, suffer from thickness non-uniformity and a possible phase separation of the deposited material. The surface energy of the underlying surface also affects the grain formation in the drop-casted films.

Inkjet printing is a computer controlled printing technique where the functional liquid material becomes an ink in the electronic printer. Inkjet printing is mostly used to print OTFTs with a restricted space resolution of 20-50 μm due to the ink spreading issues. Nevertheless, if compared to drop casting, inkjet printing can produce smaller droplets of reproducible size. The ink spreading can be overcome by forming hydrophobic/hydrophilic areas on the surface before the application of the ink. Sirringhaus demonstrated an all-polymer OTFT with 5-μm channel length using direct inkjet printing technique [151].

Screen printing is another commonly used printing technique for OTFTs. Screen printing utilizes a stencil mask with the desired dimensions and an ink paste

that is pressed with a squeegee through the stencil. Space resolution of 35-100 µm can be achieved with this technique. However, thin films are difficult to produce.

Micro contact printing uses the polymethylsiloxane (PDMS) stamps to pattern the self-assembled monolayers from solutions. Micro contact printing can achieve a resolution of 2 µm. However, micro contact printing is difficult to apply to large areas or large features.

Photolithography is a mature technique used in the fabrication of integrated circuits. Photosensitive polymer is first spun on the substrate and dried. It is then selectively exposed to the UV light and developed to provide patterned features. These features act as a mask during the wet/dry etching of the underlying layer. After the underlying layer is etched, the masking polymer is removed. This procedure is the standard of the semiconductor industry for inorganic materials. Each patterning step requires the use of specific chemical solutions (developers, strippers) and an elevated temperature. Because the commercial photosensitive polymers have very similar chemical properties to those of the organic materials used in the organic electronics, standard photolithography is not used to pattern organic materials.

2.3.2 Dry processing

OTFTs based on small molecule organic semiconductor materials employ the following most common dry deposition techniques: vacuum thermal evaporation [152], organic vapour phase deposition [153], organic molecular beam deposition [154], thermal imaging [155] and laser evaporation [156]. Vacuum sublimation or vacuum thermal evaporation is the most widely used deposition technique for small

molecule materials due to its simplicity and an existence of mature, commercially available equipment. This deposition is performed in a vacuum chamber. The source material is placed into a boat or crucible and is heated to cause its evaporation or sublimation. Shadow masks are typically used to assure that the material is deposited in the desired locations only. This process has a good control of the thickness as well as the uniformity of the deposited film. The main advantage of this technique is that layers of different materials can be sequentially deposited in high vacuum. This process is also compatible with roll-to-roll processing. The main disadvantages of this technique are its limitation to materials with low melting or sublimation temperature and the waste of the material.

In the organic vapour phase deposition technique the vapour of the desired material is generated in a hot-walled reactor vessel. The vapour is then delivered onto a cooled substrate using a stream of inert gas. This process was developed to overcome the difficulties of the vacuum sublimation technique and it allows the use of liquid organic sources. Organic molecular beam deposition technique provides thin films of high quality with well controlled thickness in ultra-high vacuum conditions. Few results were reported based on this deposition technique due to the low OTFT field effect mobility.

Thermal imaging or laser-induced thermal imaging is a deposition technique where the organic thin-film material is deposited onto a substrate by laser ablation. To do that, the desired organic film is first produced on a donor carrier that is then brought into contact with the receiving substrate. Thermal heating or laser ablation transfer the organic material from the carrier to the receiving substrate. This

technique produces devices with inferior performance, but it is very handy in developing microelectronic circuits.

Laser evaporation which is widely used for inorganic materials is also being used to evaporate organic materials. In this technique the organic material is evaporated by using a pulsed ultraviolet laser. The evaporated material condenses on the substrate maintained at low temperature. This technique produces high quality thin films which show similar morphologies and device performance as the ones prepared by thermal evaporation.

An all-dry fabrication technique was implemented to fabricate OTFTs in 2011 [157]. Pentacene OTFTs were fabricated on highly conductive silicon substrates. An acrylate polymer dielectric (crosslinked tripropyleneglycol diacrylate) was deposited by flash evaporation on silicon substrate and the remaining OTFT layers were deposited by thermal evaporation in vacuum. These OTFTs reported a field-effect mobility of 0.09cm^2/V-s, the threshold voltage of 10 V and on-off current ratio of 1.3×10^3.

Historically, OTFTs fabricated using dry processes reported better performance due to better molecular ordering and packing in different layers. The major drawback of the dry deposition techniques is their higher cost.

2.4 LOW-VOLTAGE OTFTs

Low power consumption is the main requirement for all modern-day electronic devices. Consequently, electronic devices with low operating voltages are necessary. The operating voltages of the early-day OTFTs were 20 V to 40 V. This was caused by the use of silicon wafers and a thick thermally-grown silicon dioxide

to suppress the leakage current through the dielectric. These voltages were very high when compared to the inorganic TFTs. Even though the compatibility of OTFTs with flexible plastic foils is very attractive, these silicon-wafer-based OTFTs were neither compatible with plastics nor suitable for low-voltage operation. Therefore, much effort was focused on OTFTs with low operating voltages produced on glass or plastic substrates.

OTFT drain current is directly proportional to the capacitance per unit area C_i, as shown by Eqs (6) and (7). Therefore, higher capacitance per unit area leads to a larger amount of accumulated charge for the given gate voltage and a lower threshold voltage. Consequently, such OTFTs would give similar drain current at low voltages as the high-voltage OTFTs at much higher voltages.

Capacitance C is defined as the ratio of magnitude of charge q on the capacitor electrodes to the potential difference ΔV across the electrodes and is given as $C = q/\Delta V$. Farad (F) is the SI unit for capacitance. OTFT structure involves a specific type of capacitor, a parallel plate capacitor. In this case the capacitance is proportional to the area A of the electrodes and inversely proportional to the distance d between them, namely $C = \varepsilon_0 A\left(\frac{k}{d}\right)$. The transistor Eqs. (6) and (7) involve the capacitance per unit area expressed as $C_i = \varepsilon_0\left(\frac{k}{d}\right)$ [158]. Here ε_0 is the permittivity of vacuum and k is the relative permittivity or dielectric constant of the gate dielectric. Consequently, to achieve high capacitance per unit area the low-voltage OTFTs must employ thin and/or high-k dielectrics. Taking this approach several low-voltage OTFTs have been reported. They implemented ultra-thin dielectrics [159], self-assembled monolayers [47] and high-k dielectric materials [160].

2.4.1 Dielectric materials and their fabrication

Silicon dioxide (SiO_2) is the most common dielectric in OTFTs. The typical thickness of SiO_2 is 200 nm to 400 nm. When this thickness is reduced to 2 nm, the leakage current increases by few orders of magnitude as a result of increased carrier tunnelling [161]. Increased leakage current and low relative permittivity ($k \sim 3.9$) make SiO_2 less attractive for low-voltage OTFTs. Many other existing dielectrics that were tested in OTFTs exhibited either low k or high leakage currents when their thickness was reduced. This led to the development of new dielectric materials with high relative permittivity, reduced thickness and low-temperature deposition method.

The dielectric materials implemented into low-voltage OTFTs can be broadly divided into high-k inorganic dielectrics, organic dielectrics and hybrid dielectrics [158][162]. Different dielectric groups possess different mechanical properties and are deposited by different techniques. Inorganic dielectrics are most commonly deposited by sputtering [163], anodization [164], plasma-enhanced chemical vapour deposition [165], atomic layer deposition [166], thermal or e-beam evaporation [167], and sol-gel deposition [168].

Organic dielectrics are deposited mainly by wet techniques like spin-coating [169], drop casting [170], jet, gravure or screen printing [171], and surface-initiated polymerization [172]. As mentioned in the previous section, most of these result in large thickness that is not suitable for low-voltage operation.

Hybrid dielectrics tested for low-voltage OTFT operation are polymer-nanoparticle composites and inorganic-organic bilayer dielectrics. Polymer-nanoparticle dielectrics were deposited by spin coating [173] and doctor blading [174] techniques. Inorganic-organic bilayer dielectrics were deposited by combining

the inorganic and organic dielectric deposition techniques. Anodization/spin coating [175], e-beam evaporation/spin coating [176], sol-gel technique [177], atomic layer deposition/spin coating [178], etc., are some of the inorganic-organic bilayer deposition techniques employed in low-voltage OTFT fabrication.

2.4.2 Inorganic dielectrics

Low-cost fabrication and low-voltage OTFT operation requirements have displaced the conventional dielectrics like SiO_2 by inorganic, high-k dielectrics like aluminium oxide, tantalum oxide, titanium dioxide, hafnium dioxide, zirconium dioxide and cerium dioxide [158]. Their thickness ranges from 6 to 200 nm.

Tantalum oxide (Ta_2O_5) with a dielectric constant of ~ 23 has been prepared by anodization, e-beam evaporation and magnetron sputtering. Ta_2O_5-based OTFTs exhibited threshold voltages of ~ 1.1 V [179]. Titanium dioxide (TiO_2) with relative permittivity of ~ 41 was prepared by sol-gel and spin coating. It is suitable for fabricating low-voltage printed OTFTs. TiO_2-based OTFTs have reported operating voltages > 1 V [180]. OTFTs based on hafnium dioxide (HfO_2) (relative permittivity of ~ 22) prepared by anodization and sol-gel techniques have reported very low operating voltages of ~0.75 V. Zirconium dioxide (ZrO_2) with a relative permittivity of ~ 25 prepared by atomic layer deposition is not a good candidate for OTFTs due to device degradation and higher operating voltages [181]. Cerium dioxide (CeO_2) with relative permittivity of ~ 23 has been implemented in OTFTs and the OTFT performance was poor due to its polycrystalline structure with high leakage currents [182].

Aluminium oxide with its relative permittivity of ~ 8 is the most commonly used dielectric for low-voltage OTFTs. The capacitance per unit area of Al_2O_3 layers deposited at room temperature is higher than that of the thermally grown SiO_2 films. The dielectric properties of reactively sputtered Al_2O_3 have been studied by varying the film thickness [183]. Electrical properties of Al_2O_3 deposited by rf magnetron sputtering have been studied and implemented in OTFTs [184]. Thin layers of Al_2O_3 fabricated by molecular beam epitaxy led to very low leakage currents [185]. Pentacene OTFTs have been fabricated using atomic layer deposited Al_2O_3 films [186]. AFM study confirmed that pentacene film formed a well ordered films with large grains and the OTFTs had hole mobilities of 1.5 ± 0.2 cm^2/Vs. Plasma-assisted atomic layer growth of Al_2O_3 films also produced dielectric films with relatively low leakage currents and it was indicated that post oxygen plasma annealing of Al_2O_3 films improved their electrical properties [187]. Anodised Al_2O_3 with n-octyltrichlorosilane SAM was used as a dielectric to prepare low-voltage non-volatile memory elements based on pentacene [188].

The major drawback of very thin Al_2O_3 layers is their high leakage current and possibly high surface energy. To reduce that, Al_2O_3 has been coated with thin polymer layers or self-assembled monolayers (SAMs), as discussed in Section 2.4.4.

2.4.2.1 Ozone and UV/ozone oxidation

Ozone oxidation is a low temperature substitute to conventional oxidation techniques used to oxidise metal films to create high-k dielectric materials. Ozone oxidation was introduced to oxidise different materials like silicon [189], hafnium [190], zirconium [190] and these dielectrics had enhanced dielectric properties when

compared to conventionally oxidised dielectrics of similar thicknesses. To improve the corrosion properties of aluminium, some work has been done on ozone oxidation of aluminium [191-192] but such layers have not been previously tested in transistors.

UV/ozone exposure provides an alternative path for the metal oxidation to prepare high-k dielectrics. UV/ozone cleaners have been used in semiconductor device fabrication for surface cleaning, namely to decompose and eliminate organic contaminants [193-194]. They have also been used for surface modification of thin films to improve surface wettability. UV/ozone oxidation has been used to prepare high-k dielectrics such as zirconia [195], hafnia [196–198], hafnium silicon oxynitride (HfSiON) [199] and hafnium aluminium oxynitride (HfAlON) [200]. These UV/ozone oxidised high-k dielectrics have been implemented into MOSFETs for CMOS. This project, for the first time, prepared aluminium oxide by UV/ozone oxidation of aluminium metal and implemented it into low-voltage OTFTs based on pentacene.

2.4.3 Organic dielectrics

Organic dielectrics tested in low-voltage OTFTs are inkjet-printed, spin-coated or cross-linked poly-4-vinyl phenol (PVP), preimidized polyimide, crosslinked blends of poly(methyl methacrylate) (PMMA), poly(perfluorobutenyl-vinylether) (CYTOP)®, and poly(vinyl cinnamate) with thermally crosslinked silane agent. Their typical thicknesses are 50 to 300 nm. When implemented in OTFTs, they led to OTFT operating voltage of less than 5 V [162].

Self-assembled monolayers and multilayers are another category of organic dielectric materials. Self-assembled nanodielectrics (SANDs) were also proposed and tested in low-voltage OTFTs [138].

2.4.4 Hybrid dielectrics

Inorganic dielectrics are widely used in OTFTs but due to their brittle nature organic dielectrics are preferred for applications where flexibility and stretchability is desired. However, most organic dielectrics possess low relative permittivity which is a disadvantage for low-voltage OTFTs. Therefore, the inorganic/organic hybrids have been developed to harvest the best properties of both materials. Here, the inorganic part provides the high relative permittivity, while the organic material provides the desired surface energy and low surface roughness. Hybrid dielectrics are either polymers with embedded inorganic nanoparticles or inorganic-organic bilayer dielectrics [89].

The polymer-nanoparticle composites (e.g. polystyrene with TiO_2 nanoparticles, cross-linked PVP with TiO_2 nanoparticles, and PMMA-PVC blends with silica powder) led to large leakage current density even when thicknesses in excess of 290 nm were used, and as such are not suitable for low-voltage operation. To overcome this, the inorganic-organic bilayer dielectrics were proposed by Deman and Tardy [134]. Such dielectric consists of two sequentially deposited thin films; one inorganic and the other organic. Some examples of the inorganic-organic bilayer dielectrics implemented in low-voltage OTFTs are PMMA/Ta_2O_5 bilayer [134], PMMA/Al_2O_3 bilayer [135], SiO_2/PVA bilayer [137], Al_2O_3/BCB bilayer [130], and Al_2O_3/phosphonic acid bilayer [129]. The thickness of these dielectrics varies from ~

10 nm to ~ 200 nm. To date, these hybrid dielectrics were deposited by a combination of dry (inorganic) and wet (organic) deposition techniques.

The self-assembled monolayers (SAMs) represent another possibility of organic layer formation. SAMs are usually linear oligomers with strong chemical anisotropy. The chemically active end group bonds to the surface of the underlying oxide and leads to almost vertical arrangement of the organic molecules with respect to the surface of the oxide [201]. SAMs also improve the dielectric properties of oxides such as Al_2O_3 [129] and HfO_2 [131]. Introduction of the self-assembled monolayers has reduced the density of the charge trapping states at the semiconductor-dielectric interface and improved the subthreshold slope and the threshold voltage in the pentacene OTFTs [202]. Solution-processed alkyl phosphonic acid SAMs were used to obtain a mobility of 0.6 $cm^2/V{\cdot}s$ for p-channel and 0.02 $cm^2/V{\cdot}s$ for n-channel organic thin-film transistors for implementation into logic circuits [47].

Different types of self-assembled monolayers and multilayers were reported for OTFTs [203]. Alkyl phosphonic acids have strong affinity for Al_2O_3 [47, 204–206] and, therefore, are the preferred choice for Al_2O_3. Al_2O_3 functionalized with phosphonic acids led to low-voltage pentacene OTFTs with high gate dielectric capacitance per unit area and the gate leakage current density supressed by ~ 2 orders of magnitude [207]. Alkyl phosphonic acids also lower the surface energy of Al_2O_3, leading to higher field-effect mobility and good on/off current ratio for pentacene OTFTs [208]. Some studies reported that alkyl phosphonic acids in combination with Al_2O_3 have formed organic multilayers instead of monolayers which helped in the crystallographic film formation of the semiconductor layer [205].

In all of the above cases the SAMs were deposited from solutions. However, in such a case, traces of the solvents may be left in the deposited layer and may affect the device performance. The development of a dry process would eliminate such issue. Therefore, this thesis explores the vacuum growth of 1-octylphosphonic acid monolayer and combines it with an ultra-thin aluminium oxide to form an inorganic-organic bilayer in low-voltage OTFTs.

2.5 OTFT STABILITY

Stability is a major issue with the OTFTs because many organic materials tend to degrade (change their chemical composition) when exposed to UV light, oxygen or moisture. In addition, prolonged application of the electrical bias changes the transistor performance. Both effects can lead to the reduced field-effect mobility and change in the OTFT threshold voltage and sub-threshold slope. Implementation of OTFTs into circuits requires good bias and environmental stability. Electrical and environmental instability studies have been performed by many research groups [165, 209–221]. While the environmental stability is understood in some materials like pentacene, a comprehensive theory to explain the bias instability is still lacking.

2.5.1 Instability induced by electrical bias

Instability induced by electrical bias is not unique to OTFTs. Bias instability in amorphous silicon transistors is well understood [222, 223] and these transistors find wide-spread commercial application in liquid-crystal displays and electronic readers. Though OTFTs offer prospect for large-area and flexible device

applications, their bias instability must be understood and addressed. Therefore, OTFT fabrication processes, material selections and operating voltages must be tested to provide OTFTs with stable and reliable performance.

Bias stress may cause variations in the OTFT parameters such as the threshold voltage, subthreshold slope, field-effect mobility, and the on- and off-currents. However, well optimized OTFTs typically exhibit change in the threshold voltage only. Mobile ion migration, bipolaron formation in the organic semiconductor and the defect generation at the dielectric/semiconductor interface have been proposed to cause the bias instability [211] in the OTFTs. Bias stress causes the threshold voltage to shift to higher negative values in the case of p-channel OTFTs and to higher positive values in the case of n-channel OTFTs. This threshold voltage shift is caused by the prolonged biasing of the gate electrode, leading to charge accumulation at the dielectric/semiconductor interface. Smaller shift in the threshold voltage was observed when both the gate and the drain electrodes were biased.

In OTFTs the bias instability arises due to the gate-bias induced charge carriers trapped at the dielectric/semiconductor interface, injected into the gate dielectric or trapped in the conduction channel. Carrier trapping increases when the devices are biased for longer periods of time or with higher voltage, causing a larger shift in the threshold voltage and a decrease in the drain current.

The time-dependent shift in the threshold voltage, ΔV_t, during the bias stress is described by a stretched exponential function [209]. This stretch-exponential behaviour, as opposed to simple exponential behaviour, is a result of an energy distribution of the carrier traps and is described by

$$\Delta V_t(t) = [V_t(\infty) - V_t(0)] \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}} \right] \quad (8)$$

here $V_t(\infty)$ is the equilibrium threshold voltage after the prolonged electrical bias, $V_t(0)$ is the initial threshold voltage before the application of the electrical bias, τ is a time constant and β is the stretching parameter ($0 < \beta \leq 1$).

2.5.2 Instability induced by ambient environment

Organic OTFTs are stable in vacuum but their performance degrades over time when they are exposed to UV light, oxygen, or moisture. Defects can be induced in the organic semiconductors when they are exposed to the light. Organic molecules do not react with the oxygen in the ground state. Upon exposure to the light, the oxygen becomes photoexcited and more reactive. Oxidation results in a deformation of the conjugated system, leading to a larger HOMO-LUMO gap and a reduction in the field-effect mobility [219]. In addition, deeper defect states are formed in the organic semiconductors, leading to the change in the subthreshold slope of the OTFTs [210].

Moisture or water absorption also degrades the OTFT performance as deeper trap states are created in the semiconductor material. Defects are also created if solvents are used to fabricate the OTFTs, leading to the OTFT degradation. Not much research has been done on the environmental stability of the OTFTs because this issue can be resolved by using proper encapsulation and the devices can be fabricated in a controlled environment. However, the sensitivity of organic materials to various gases was exploited in gas sensing applications.

2.6 SUMMARY AND OBJECTIVES

This chapter discussed conjugated organic semiconductors, the structure and operation of organic thin-film transistors and materials and fabrication processes involved in OTFT fabrication process. Since the focus of this thesis is the development of low-voltage OTFTs, an overview of the materials and fabrication techniques employed to fabricate such transistors has been presented as well. Finally, the OTFT instability arising from the bias stress and exposure to ambient environment has been discussed.

Transistors that require low operating voltages are highly desirable in many circuit applications, for example in flexible displays, electronic readers and RF identification tags. In such a transistor the gate dielectric layer is one of the crucial layers. It controls the turn-on voltage of the transistor, the current of the transistor in its on-state, the leakage current from the gate electrode, and the growth of the subsequent transistor layers. Thicker dielectrics lead to lower leakage currents but higher operating voltages. While the operating voltage of the transistor decreases and the on-current increases when the thickness of the gate dielectric is reduced, the leakage current also increases. Consequently, organic thin-film transistors typically employ thicker dielectric layers to suppress the unwanted leakage current. The challenge of the project was to develop an ultra-thin gate dielectric for low-voltage OTFTs that would lead to a negligible gate current when compared to the drain current.

The main objectives of this research were: i) to develop a low-temperature, dry fabrication process for low-voltage OTFTs, (ii) to develop an ultra-thin, dry, organic/inorganic bilayer dielectric based on aluminium oxide and alkyl phosphonic

acid, (iii) to study the preparation of the aluminium oxide by UV/ozone exposure, and (iv) to investigate the stability of these low-voltage OTFTs. Vacuum evaporation was employed to deposit various transistor layers with the aim to obtain transistor performance comparable to that of organic transistors prepared with mixed wet and dry techniques. Such a process would open path for introduction of a wider range of plastic substrates with more stringent thermal and chemical constraints.

3 EXPERIMENTAL PROCEDURES

3.1 SELECTION OF MATERIALS

OTFTs are prepared by depositing thin films of different functional materials on a substrate. Although a large variety of materials for OTFT fabrication is available, only some materials are compatible with the dry fabrication and low-voltage device operation. Since this research could not build on any previous research results obtained within the group, the growth of all chosen functional materials had to be pre-optimized. Therefore, to reduce the complexity of the optimization process and to study the effect of the aluminium oxide preparation on the OTFT performance, well-studied organic semiconductor and electrode materials were selected.

This section gives a brief description of the materials and the deposition techniques employed to fabricate the OTFTs. The approach is based on the implementation of a dry, ultra-thin gate dielectric with the thickness smaller than 20 nm and a moderate relative permittivity. The remaining materials, i.e. the organic semiconductor and the source-drain electrodes, were chosen based on the OTFT results reported in the literature.

3.1.1 Gate dielectric

To obtain OTFT with high field-effect mobility it is crucial to have the best organic semiconductor layer in terms of growth and grain formation. Semiconductor layer formation is controlled by the layer over which it is grown [125]. Therefore, to obtain good crystalline morphology of the semiconductor layer in the BGTC transistor geometry, the surface roughness and the surface energy of the gate dielectric need to be controlled. The conducting channel is formed above this dielectric layer in the organic semiconductor and, therefore, the properties of this dielectric/semiconductor interface are also very important [125].

This project developed a dry, ultra-thin dielectric composed of aluminium oxide and a monolayer of 1-octylphosphonic acid. For the first time the aluminium oxide was prepared by UV/ozone oxidation of aluminium metal and the 1-octylphosphonic acid was deposited in vacuum. The following sections discuss the details of these processes.

3.1.1.1 UV/ozone oxidation of aluminium

This section describes the preparation of the AlO_x that formed the inorganic part of the inorganic-organic bilayer gate dielectric in pentacene-based low-voltage OTFTs.

Figure 3.1 is a pictorial representation of AlO_x formation by UV/ozone oxidation of aluminium. The gate electrode, a 30-nm-thick Al, was thermally evaporated through a shadow mask (gate electrode) onto a glass substrate (Eagle 2000). A 20-nm-thick Au film was thermally evaporated on one end of all gate lines

through a shadow mask to prevent their oxidation. Aluminium was then exposed to UV/ozone in a commercial UV/ozone cleaner for a fixed length of time. This led to the formation of a thin layer of AlO_x on the surface of aluminium. Afterwards, a 15 Å-thick layer of aluminium was deposited on top of the created AlO_x and UV/ozone oxidized for the same time as the gate electrode. Additional 15 Å-thick aluminium

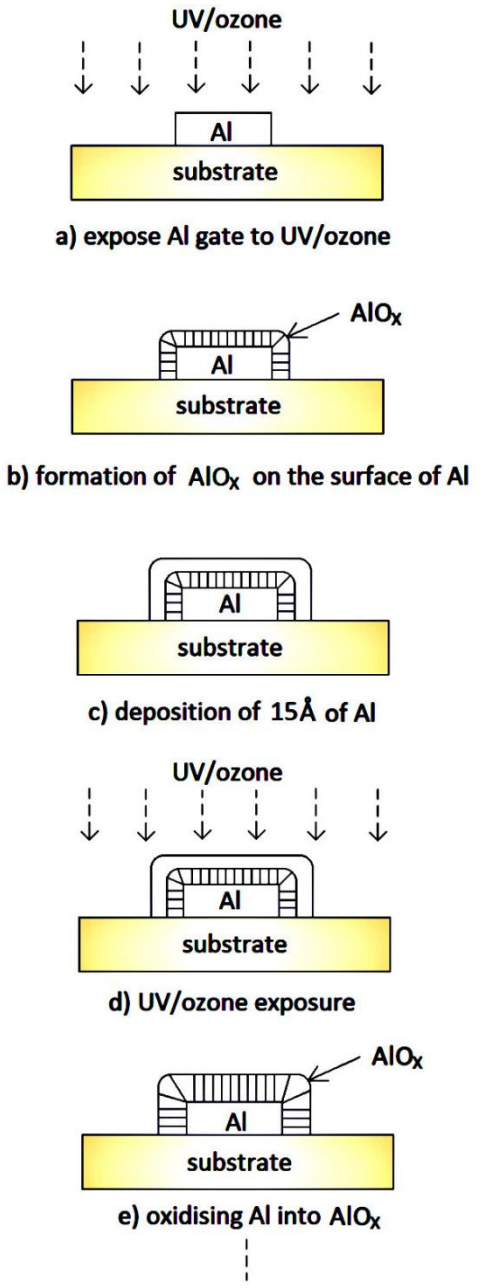

Figure 3.1. UV/ozone treatment procedure for AlO_x formation.

layers were sequentially deposited and oxidized to increase the AlO_x thickness. The number of these 15 Å-thick layers of aluminium was varied from 0 to *n* where *n* was as high as 6. Different AlO_x layers were prepared in different experiments. In some experiments the UV/ozone exposure time was varied, while the AlO_x thickness was kept constant. In other experiments, the UV/ozone exposure time was kept constant while the AlO_x thickness was varied. In all cases, AlO_x was prepared by exposing the aluminium to UV/ozone in ambient atmosphere. To prevent the contamination of the oxidizing surface, the UV/ozone cleaner was enclosed under a Hepa filter.

The essential part of a UV/ozone cleaner is a high-pressure mercury lamp that emits UV light at 184.9 and 253.7 nm. Molecular oxygen absorbs the 184.9 nm wavelength and converts to ozone. The higher UV wavelength does not generate ozone; on the contrary, it causes its dissociation into atomic oxygen. Consequently, the ozone is continuously generated and destroyed in the UV/ozone cleaner. The generated ozone and/or atomic oxygen reacted with aluminium to form aluminium oxide. In addition, the UV light was absorbed by the glass substrate, leading to a temperature rise of the sample to ~ 100°C. This temperature, set by the light intensity of the flat mercury lamp at the surface of UV-absorbing glass substrates placed at a fixed distance underneath the lamp, was determined experimentally. Consequently, the growing AlO_x layer may have been annealed as it was formed.

3.1.1.2 1-octylphosphonic acid

The organic part of the inorganic-organic bilayer dielectric is a short-chain alkyl phosphonic acid, namely 1-octylphosphonic acid, chemically represented as $C_8H_{19}O_3P$. Figure 3.2 shows the molecular structure of 1-octylphosphonic acid

comprising of a phosphonate group and an alkyl chain. 1-octylphosphonic acid was selected because it was commercially available with the highest purity.

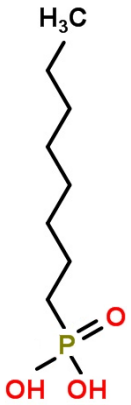

Figure 3.2. 1-octylphosphonic acid molecular structure.

99%-pure 1-octylphosphonic acid was purchased from Sigma-Aldrich and thermally evaporated through a shadow mask (gate dielectric) in high vacuum (~ 1×10^{-7} mbar) on UV/ozone oxidized AlO_x. The substrate holder was kept at room temperature during the growth and it was heated to ~ 135°C for 1 hour after the deposition. The optimization of the 1-octylphosphonic acid growth was not part of this project and the same recipe was used in all transistor and metal-insulator-metal (capacitor) structures. It was however confirmed through the capacitance measurements that the resulting thickness was approximately equal to the length of the molecule (cca 1 nm).

3.1.2 Organic semiconductor and electrodes

Pentacene, a p-type small molecule organic semiconductor, was used in this project. Pentacene is well studied and the most understood vacuum deposited organic

semiconductor whose incorporation into OTFTs often leads to high field-effect mobility. Figure 3.3 shows pentacene ($C_{22}H_{14}$) with its 5 benzene rings forming a linear molecular structure.

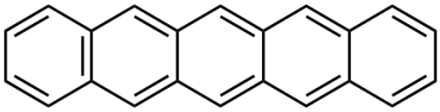

Figure 3.3. Pentacene molecular structure.

Three-times purified pentacene was purchased from Sigma-Aldrich and used as purchased. It was vacuum deposited through a shadow mask (semiconductor) onto the 1-octylphosphonic acid layer. A 50-nm-thick pentacene layer was used in the OTFTs. The deposition was performed at room temperature at a rate of 0.16 Å/s and pressure of ~ 1×10^{-7} mbar. The same recipe was used in all OTFTs.

As discussed above, aluminium with 99.999% purity was used for the gate electrode. When exposed to UV/ozone, its surface was converted into aluminium oxide. Other advantages of Al are its low cost and good electrical conductivity. Thermal evaporation of aluminium was performed at a pressure of ~ 1×10^{-6} mbar.

To obtain an effective charge injection from the source electrode into the transistor channel, the work function of the material chosen for the source and drain electrodes must match the HOMO level of pentacene.

Figure 3.4 shows that the work function of gold of ~ 5.1 eV is well aligned with the HOMO level of the pentacene lying at ~ 4.9 eV [54]. In fact, Au has been the material of choice for the majority of pentacene OTFTs. In this project the 99.99% gold was deposited by thermal evaporation trough a shadow mask (source/drain electrodes) at a pressure of ~ 1×10^{-6} mbar.

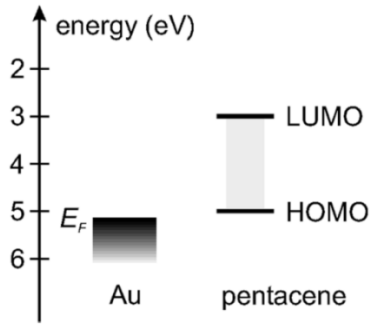

Figure 3.4. Alignment of pentacene energy levels and the work function of gold [53].

3.2 DEVICE STRUCTURES

This section describes the general design layout of the OTFT samples and the transistor structure. The design layout aimed to obtain as many devices as possible in one fabrication run and to provide some data on the yield and uniformity of the fabricated devices. This section discusses the design of the transistor shadow masks. Although later in the project a new source/drain mask was designed to accommodate the changed requirements, the general device layout was maintained.

3.2.1 Mask design

The transistor shadow masks were designed using AutoCAD design software. Figure 3.5 represents the design layout of the OTFTs. On a 76×76 mm^2 substrate each transistor was allocated an area of 5×5 mm^2. There are 6 identical transistor sections, each containing 4×4=16 OTFTs with variable channel length and channel width. 9-mm side spacing is provided for the alignment marks. 2-mm spacing is provided between the transistor sections and they are 6 mm away from the top and bottom edges of the substrate.

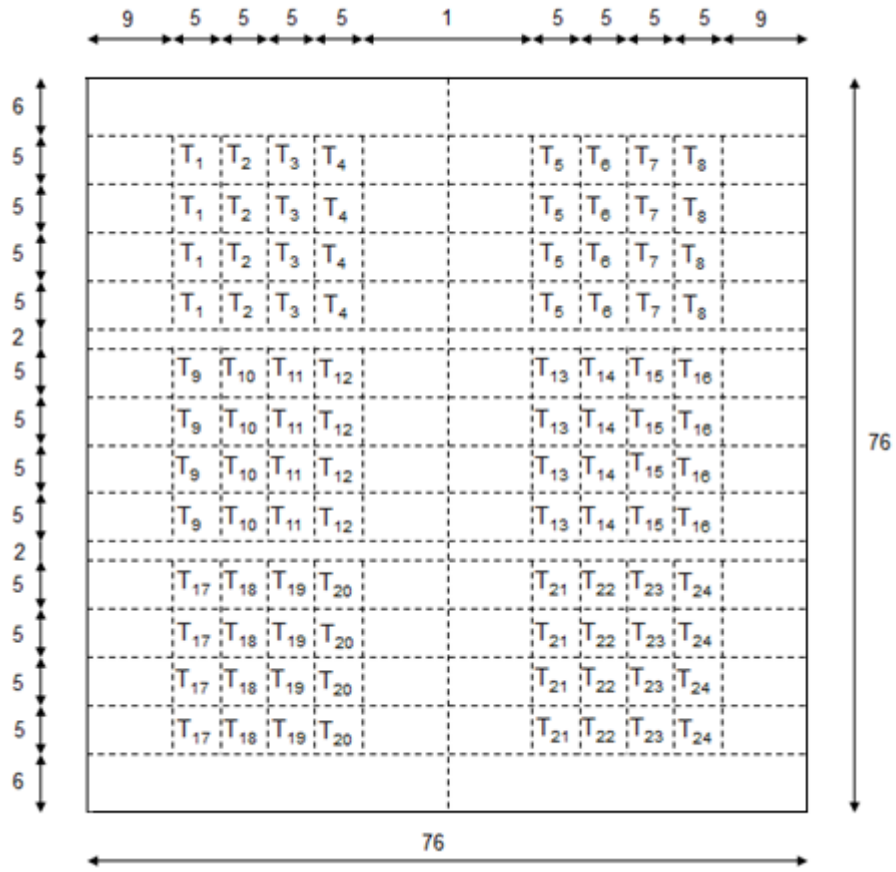

Fig 3.5. Design layout for OTFTs.

Table 6 lists the different channel lengths and channel widths implemented in the OTFT design. As shown in Figure 3.5, a single section of transistors has 16 OTFTs. Four vertical transistors in each set have the same channel length and channel width. Similarly, transistors in the next column have common dimensions.

Shadow masks for the semiconductor island, gate dielectric, and the partial coverage of the gate lines with Au were fabricated using a CAD controlled drill bit. These masks were made of 1.2-mm thick aluminium sheet. After machining, the metal masks were polished and cleaned with acetone and methanol and dried with nitrogen gun. The source-drain and gate masks were made by laser cutting of Kapton substrate. These masks were fabricated by CADiLAC Laser and cleaned with acetone and methanol and dried with the nitrogen gun. The mask layout is shown in Appendix 1.

Table 7. OTFT channel lengths (*L*) and channel widths (*W*).

Transistor	Channel Length L (μm)	Channel Width W (μm)
T1	20	200
T2	30	200
T3	40	200
T4	50	200
T5	60	200
T6	70	200
T7	80	200
T8	100	200
T9	20	500
T10	30	500
T11	40	500
T12	50	500
T13	75	500
T14	100	500
T15	125	500
T16	150	500
T17	20	1000
T18	30	1000
T19	40	1000
T20	50	1000
T21	75	1000
T22	100	1000
T23	125	1000
T24	150	1000

3.2.2 Capacitor structures

Metal-insulator-metal (MIM) structures (or capacitors) with AlO_x and AlO_x coated with 1-octylphosphonic acid monolayer were fabricated using various AlO_x

thicknesses and UV/ozone exposure times. Figure 3.6.a shows the cross-sectional view of the AlO_x capacitors and Figure 3.6.b shows the cross section of capacitors with AlO_x coated with a monolayer of 1-octylphosphonic acid.

Two different capacitor structures are shown in Figure 3.7. Figure 3.7.a shows the crossover type and Figure 3.7.b depicts the planar structure. The patterned Al lines in Figure 3.7.a as opposed to Figure 3.7.b require that the bilayer dielectric covers the vertical surfaces as well. Therefore the comparison of these two structures allows evaluating the step coverage of Al electrode by the dielectric bi-layer.

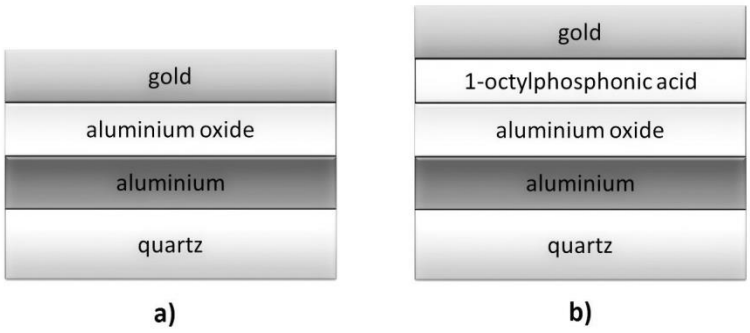

Figure 3.6. Cross section of capacitors with AlO_x (a) and AlO_x coated with 1-octylphosphonic acid (b).

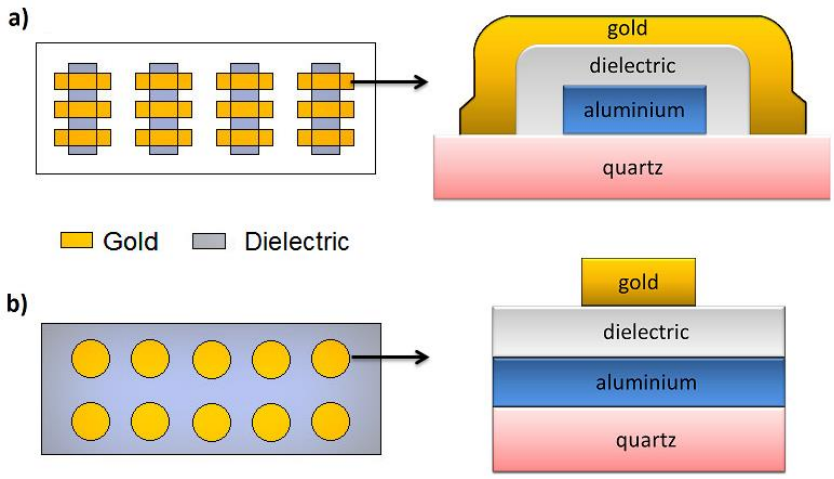

Figure 3.7.Top and cross-sectional view of capacitor structures: (a) cross-over and (b) planar.

3.2.3 OTFT structure

All OTFTs fabricated in this project have the bottom gate and top contact (BGTC) structure as shown in the Figure 3.8. Since the AlO_x is prepared by the UV/ozone oxidation of the aluminium metal, choosing aluminium as a gate electrode simplifies the fabrication process.

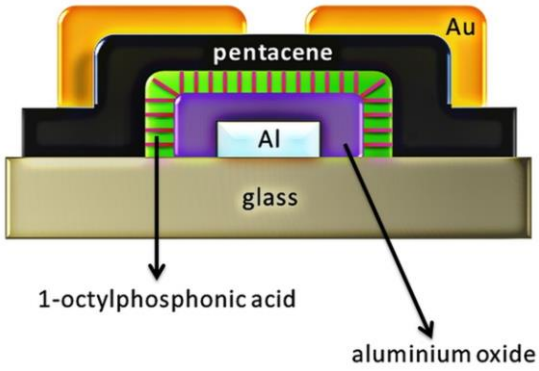

Figure 3.8. Cross-sectional view of the organic thin-film transistor.

3.3 DEVICE FABRICATION

All devices (transistors, capacitors) are fabricated by dry fabrication steps. This section discusses the details of the device fabrication procedures.

3.3.1. Capacitor fabrication

Capacitors with AlO_x and AlO_x coated with 1-octylphosphonic acid were fabricated on clean quartz wafers. Pairs of capacitors with and without 1-octylphosphonic acid (see Figure 3.6) were fabricated side by side in some experiments. Crossover capacitors depicted in Figure 3.7.a were fabricated by

thermal evaporation of aluminium through a shadow mask containing rectangular slits of 500 μm by 5 mm. The aluminium was then exposed to UV/ozone for different times. After the dielectric layer was formed, a 50-nm-thick gold layer was thermally evaporated at a pressure of ~ 1×10^{-6} mbar through a shadow mask with rectangular openings of 750 μm by 2 mm.

The planar capacitors were fabricated in a similar manner. In this case, however, the aluminium formed a continuous layer. After the dielectric layer was formed, a 50-nm-thick layer of gold was deposited by vacuum deposition at a pressure of ~ 1×10^{-6} mbar using shadow masks with holes of various diameters.

Planar and cross-over capacitors were fabricated with and without phosphonic acid, side by side. The thickness of the 1-octylphosphonic acid layer was approximately 1 nm. The fabricated capacitors were stored in nitrogen atmosphere during the whole fabrication process and they had very minimal exposure to the normal atmospheric conditions. Initially, batches of capacitors were fabricated to study the effect of the UV/ozone exposure on their properties. Later the capacitors were fabricated alongside of each transistor set. These were used to obtain the dielectric capacitance, leakage current density and the electric breakdown voltage.

3.3.2. Transistor fabrication

All fabricated OTFTs have the bottom gate and top source-drain contact structure as shown in Figure 3.8. The materials used for fabrication (see Figure 3.8) are: glass Eagle 2000 as substrate, aluminium as gate contact, aluminium oxide coated with approximately a monolayer of 1-octylphosphonic acid as the gate

dielectric, pentacene as the semiconductor and gold as source and drain contacts. The fabrication details are given in Section 3.1.

Aside from the UV/ozone oxidation, all TFT layers were grown under high vacuum condition (~1×10^{-7}–1×10^{-6} mbar) in a computer-controlled thermal evaporator (Minispectros, Kurt J Lesker) enclosed in a nitrogen glove box. Each transistor set typically contained 6 different samples; samples within each set were prepared side by side. Each sample contained 12 transistors with channel width of 1 mm and 4 different channel lengths of 30, 50, 70, and 90 μm, and four corresponding capacitor structures, total of 16 devices.

With the aim to optimize the preparation of aluminium oxide via UV/ozone exposure initially three sets of transistors (A, B, and C) were fabricated. Set A and C were fabricated to investigate the effect of UV/ozone exposure time for the fixed dielectric thickness. In set B the AlO_x thickness was varied while the UV/ozone exposure time was held at 60 minutes. In addition, the AlO_x thickness of sets A and C correspond to the lowest and the highest thickness in set B, respectively. AlO_x in set A was fabricated by exposing the aluminium gate to UV/ozone for t = 2, 5, 10, 20, 40 or 60 minutes. Afterwards, a 15-Å-thick layer of aluminium was deposited on top of the created AlO_x and UV/ozone oxidized for the same time as the gate electrode. Additional 15 Å-thick aluminium layers were sequentially deposited and oxidized to increase the AlO_x thickness in sets B and C. The number of 15 Å-thick aluminium layers is n. n=1 for set A and n=6 for set C. In set B n is varied from 1 to 6 while the UV/ozone exposure time t is fixed at 60 minutes. Except AlO_x all other TFT layers in all three sets were prepared in the same manner.

To study the effect of thermal heating of AlO_x during the UV/ozone oxidation process two sets of transistors (D and E) were fabricated. In set D different UV/ozone exposure times of 2, 5, 10, 20, 40 and 60 min were used to prepare the AlO_x in the OTFTs. The UV/ozone exposure of AlO_x was followed by an annealing in a vacuum oven at 100°C for 58, 55, 50, 40, 20 and 0 min, respectively. The rest of the layers were prepared according to the standard recipe. In the set E the AlO_x layers were prepared by UV/ozone exposure of Al for 2, 5, 10, 20, 40 and 60 min. Afterwards these layers were annealed in a vacuum oven for 24 hours at 140°C. The remaining transistor layers were prepared according to the recipe mentioned above.

We also studied the effect of OTFT dimensions (*W* and *L*) on the transistor performance. OTFT set F was fabricated for this purpose. Standard fabrication procedure was followed with AlO_x prepared by 60-min UV/ozone exposure.

3.4 DEVICE MEASUREMENT

All device measurements were performed in ambient atmosphere in the dark using Agilent B1500A semiconductor parameter analyser. The measurement unit was equipped with a capacitance module that allows switching between the current-voltage and capacitance measurements.

3.4.1 Capacitor leakage current density

All dielectric materials pass small current upon application of voltage. The current results from pinholes or defects that allow charge carriers to move across. Ideally this current should be very small. The leakage current was measured by

sweeping the voltage on the Au electrode while grounding the Al one. The voltage was raised in 10 mV increments. Example of a current-voltage (I-V) measurement is shown in Figure 3.9. To obtain the leakage current density in A/cm^2, the current is divided by the area of the parallel-plate capacitor.

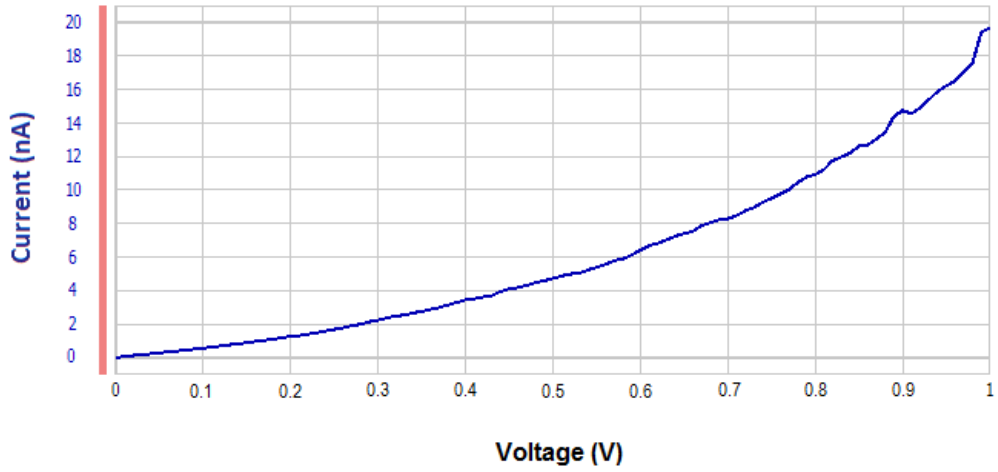

Figure 3.9. Current-voltage measurement of a capacitor.

Breakdown voltage is the maximum voltage that a dielectric can withstand without losing its insulating properties. Upon breakdown, large current suddenly flows through the dielectric and creates a permanent current path. Example of such irreversible change is shown in Figure 3.10. In this case the dielectric lost its resistance and became highly conducting at the breakdown voltage of ~ 5.5 V. We define the breakdown voltage as the voltage at which the current of 100 µA is reached. The breakdown voltage depends on the thickness of the dielectric; the breakdown voltage increases with the increasing thickness of the dielectric. Therefore, for the reason of easy comparison, it is better to define the electric breakdown field (typically given in MV/cm), obtained by dividing the breakdown voltage with the thickness of the dielectric. Good dielectrics typically achieve values in excess of 5 MV/cm.

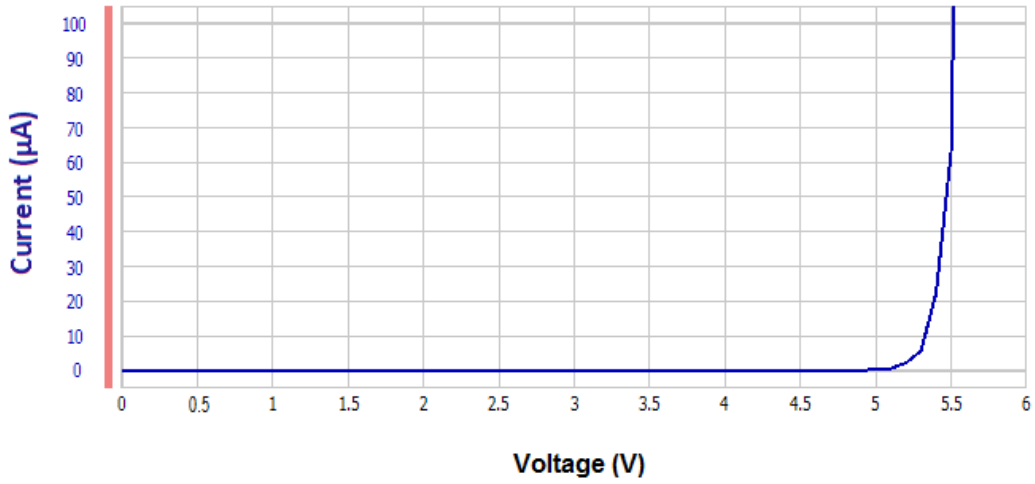

Figure 3.10. I-V measurement to obtain the dielectric breakdown voltage.

3.4.2 Gate dielectric capacitance

The dielectric capacitance was measured as a function of a.c. frequency (see Figure 3.11) from 1 kHz to 5 MHz with a d.c. bias of 1 V and an a.c. oscillation of 50 mV. This measurement was done in the same configuration as the leakage current measurement. Both the parallel and series equivalent models were fitted to the measured data. Capacitance values extracted at the frequency of 1 MHz were used in the transistor calculations.

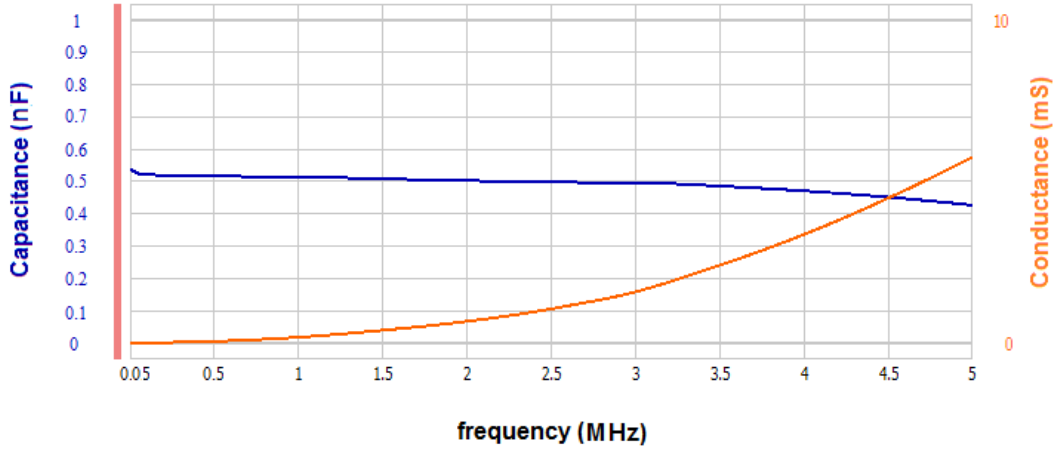

Figure 3.11.Gate dielectric capacitance measurement.

The capacitance module of B1500A can measure the conductance and admittance of the capacitor. Capacitance was then calculated by fitting the measured data to the parallel and series models. Parallel and series resistances, impedance, and the phase angle were calculated as well. Capacitors with conductance < 1 mS exhibited large parallel resistance, small series resistance, the phase angle of ~ −90° and the capacitance values calculated using the series and parallel models were similar. As can be seen from Figure 3.11, this behaviour was well satisfied at the chosen frequency of 1 MHz.

3.4.3 Transistor characteristics

The transistor transfer characteristics were obtained by applying a voltage sweep on the gate electrode from 1 V to –3 V and measuring the drain current while applying two different drain voltages of –0.1 V and –3 V, as shown in Figure 3.12. The gate voltage was decreased in 40-mV increments.

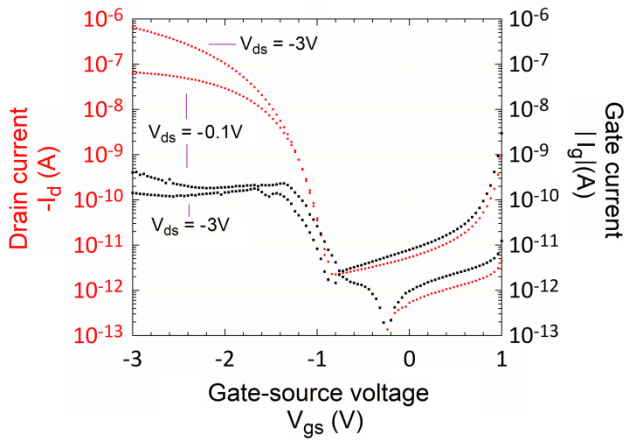

Figure 3.12. OTFT transfer and gate current characteristics.

Figure 3.13 shows an example of the OTFT output characteristics. They are obtained by applying a voltage sweep on the drain electrode from 0 V to –3 V and

measuring the drain current at different gate voltages of 0, –0.5, –1, –1.5, –2, –2.5 and –3 V. The drain voltage was decreased in 30-mV increments.

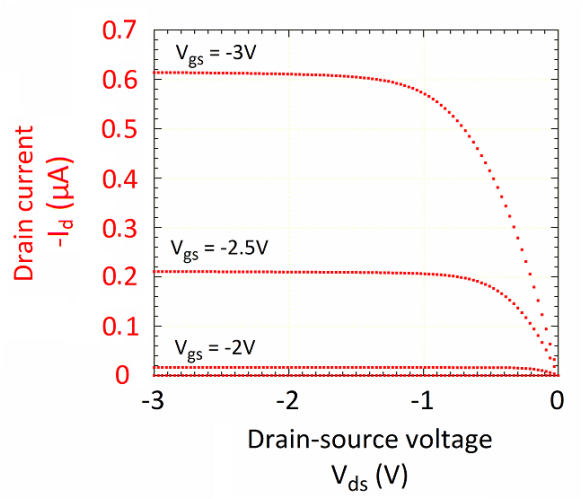

Figure 3.13. OTFT output characteristics.

3.4.4 Bias stress of transistors

Bias stress measurements were performed on various transistor sets to study the effect of the preparation conditions of the aluminium oxide. During the bias stress measurements the bias was applied to the gate electrode and the source and drain electrodes were grounded. This configuration leads to a larger shift in the threshold voltage than biasing the drain and gate electrodes simultaneously.

Before the bias stress commenced, the transfer characteristic of the virgin transistor was measured. Afterwards, the voltage was applied across the gate terminal for a total time of 5000 s. The bias stress was regularly interrupted and the transistor transfer characteristic was measured. Measurements were taken after 10, 30, 70, 100, 200, 600, 1000, 2000 and 5000 seconds.

Two types of bias stress measurements were performed. First measurement involved studying the effect of UV/ozone exposure time of AlO_x on the bias stress

instability at a constant gate bias of –4 V. The second measurement involved studying the effect of different gate biases of –3, –3.5, –4, –4.5 and –5 V on the bias stress instability of OTFTs prepared with 60-min-UV/ozone-exposed AlO_x. For the bias stress measurements the transfer characteristic at the drain voltage of –3 V was measured. These measurements were performed quickly to minimize the pause in the bias stress experiment and not to allow the recovery of the OTFT. The standard transistor parameters were extracted from the transfer characteristics as discussed in the following section.

3.5 TRANSISTOR PARAMETER EXTRACTION

This section describes the extraction of various OTFT parameters. To allow comparative studies of the OTFTs prepared in different experiments, all transistors had similar history and they were measured using the same protocol. OTFTs were evaluated using the general MOSFET equations in linear and saturation regimes to calculate the field-effect mobilities and threshold voltages in linear and saturation regimes and the inverse sub-threshold slope. The MOSFET equations were derived in Section 2.2.5.

3.5.1 Field-effect mobility and threshold voltage in the linear regime

The current-voltage relationship in the linear regime of the transistor is expressed by Equation (6) (see Section 2.2.5). For V_{ds} = –0.1 V the transistor is in the linear regime and the slope of the I_d versus V_{gs} is given by:

$$Slope = \left(\frac{W}{L}\right) \mu_p \, C_i \, V_{ds} \qquad (9)$$

Figure 3.14 shows the transfer characteristic at V_{ds} = –0.1 V plotted on a linear-linear scale and the linear fit used to calculate the field-effect mobility and the threshold voltage.

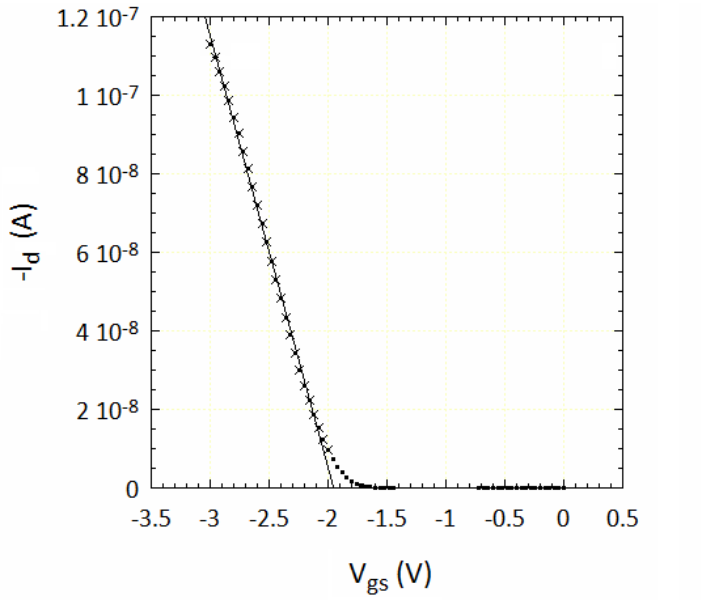

Figure 3.14. Mobility and threshold voltage extraction in the linear regime.

The linear section of the I_d versus V_{gs} characteristic is fitted with a straight line. The intercept of this line on the voltage axis determines the threshold voltage V_t, while its slope is used to calculate the field-effect mobility in linear regime using Equation (9). To calculate the mobility, W and L were measured for each transistor and C_i was calculated as the mean of the capacitance determined experimentally from the corresponding capacitor structures.

3.5.2 Field-effect mobility and threshold voltage in the saturation regime

The current in the saturation regime is represented by Equation (7). For V_{ds} = –3 V the transistor is in the saturation regime. Plotting $\sqrt{I_d}$ versus V_{gs} leads to a linear dependence with the following slope:

$$Slope = \sqrt{\left(\frac{W}{2L}\right) \mu_p C_i} \tag{10}$$

The square root of the drain current I_d for V_{ds} = –3 V is plotted as a function of V_{gs} on a linear-linear scale. Straight line is fitted to the linear section as shown in Figure 3.15. Similarly to the linear regime, the slope of this line is used to obtain the field-effect mobility and the intercept on the x-axis to obtain the threshold voltage V_t (see Figure 3.15).

3.5.3 On-, off- and gate-leakage currents and inverse subthreshold slope

Transistor on- and off-currents are extracted directly from the measured transfer characteristics. The on-current of the OTFT is the drain current at V_{gs} = –3 V

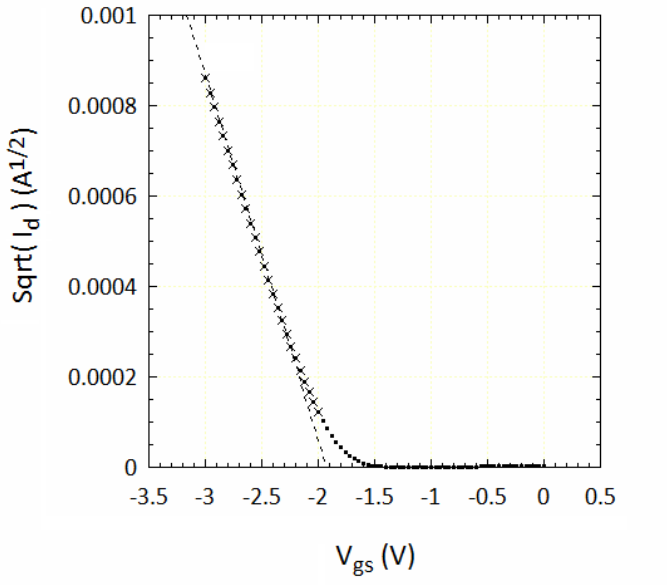

Figure 3.15. Mobility and threshold voltage extraction in the saturation regime.

and V_{ds} = –3 V. The off-current is the minimum drain current obtained in the transfer characteristic for V_{ds} = –3 V. The gate-leakage currents are also measured while measuring the OTFT transfer characteristics. The gate-leakage current is the gate current at V_{gs} = –3 V and V_{ds} = –3 V.

Subthreshold slope is an important parameter of the OTFT. The exponential rise on the transfer characteristic for V_{ds} = –3 V is used to determine the inverse subthreshold slope in mV/decade defined as $[\partial \log_{10}(I_d)/\partial V_{gs}]^{-1}$. This section of the curve is re-plotted in Figure 3.16 and an exponential curve is fitted through these data points.

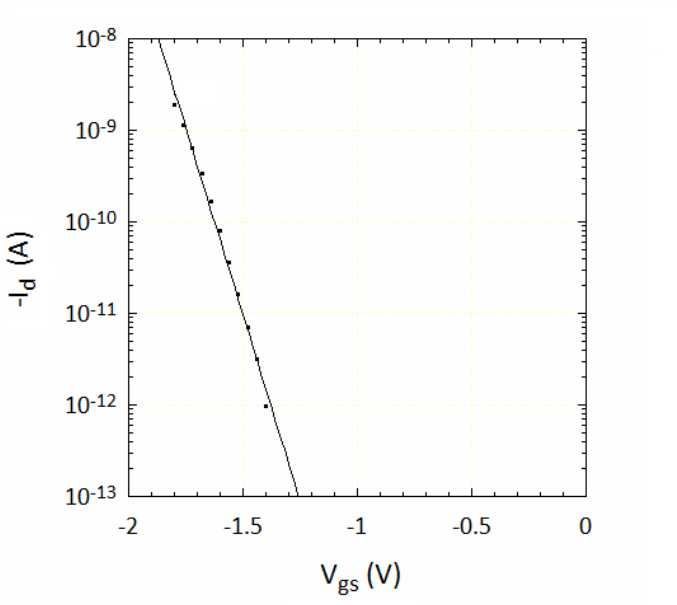

Figure 3.16. Extraction of the subthreshold slope.

In summary, this chapter discussed the selection of the materials, mask design, fabrication of the transistor and capacitor structures, device measurements including the bias stress, and the transistor parameter extraction.

4 GATE DIELECTRIC OPTIMIZATION

4.1 INTRODUCTION

This thesis focuses on the preparation and optimization of AlO_X dielectric layer produced by UV/ozone oxidation of aluminium metal to obtain the gate dielectric material suitable for OTFTs with low operating voltages. Chapter 4 summarizes the results of a study of metal-insulator-metal (MIM) structures that incorporate AlO_X dielectric layer prepared by UV/ozone oxidation of aluminium. These structures were investigated and optimized with the aim to produce the dielectric for low-voltage OTFTs. The dielectric layer suitable for low-voltage OTFTs should be very thin with high relative permittivity, leading to high capacitance and consequently to an increase in the charge carrier density accumulated in the channel of the OTFT for a given gate voltage. At the same time, the leakage current flowing through the dielectric layer should be very low and the electric breakdown field should be high. Since the UV/ozone oxidation technique has never been used to produce AlO_X gate dielectrics in thin-film transistors, a comprehensive process optimization was carried out.

To create the AlO_X layer, aluminum was exposed to the UV/ozone for varied amount of time with the aim to achieve the above mentioned dielectric properties.

Several batches of metal-insulator-metal (MIM) structures with different contact area, layer structure, topography, and UV/ozone exposure time were fabricated. These structures were characterized by measuring the capacitance as a function of a.c. frequency and the current-voltage characteristics. In addition, batches of complementary MIM structures with similar AlO_X layers and added monolayer of 1-octylphosphonic acid were fabricated by adding the alkyl phosphonic acid on top of the UV/ozone oxidized AlO_X. Leakage currents, electric breakdown voltages and capacitances as functions of frequency of these MIM structures with inorganic/organic dielectric bilayer were measured to make a comparative study.

Sections 4.2, 4.3 and 4.4 summarize the experimental results of the MIM structures with AlO_X layers prepared by a single UV/ozone exposure of aluminium. Structures with and without 1-octylphosphonic acid monolayer are compared.

Section 4.5 describes how an additional suppression of the leakage current could be achieved when thicker UV/ozone oxidized AlO_X is used. Since the oxidation is a self-limiting process, an increase in the UV/ozone oxidation time beyond about an hour is not a practical solution for producing thicker oxide. Therefore, an alternative pathway was suggested and described in Section 3.1.1. This procedure relies on the deposition of additional ultra-thin layer(s) of aluminium on top of the already formed AlO_X dielectric and their subsequent conversion into AlO_X using UV/ozone oxidation. Batches of MIM structures with varied AlO_X thicknesses were fabricated using this procedure. The leakage currents of these thicker MIM structures were investigated to understand the effect of AlO_X thickness on this parameter.

Section 4.6 explains how the MIM structures studied in Section 4.5 also could be used to estimate the relative permittivity of the UV/ozone oxidized AlO_X. To do this, capacitance as a function of frequency was measured for a large number of MIM (capacitor) structures with different AlO_X thicknesses. These AlO_X layers were made thick enough to allow measurement of their thicknesses with Dektak profilometer. The relative permittivity was calculated from the known capacitance and the layer thickness.

Section 4.7 explains how the thickness of AlO_X layer produced on the surface of aluminium metal by a single UV/ozone oxidation step can be extracted. The determination of this thickness typically requires spectroscopic ellipsometry. In this experiment several batches of MIM structures with varied AlO_X thickness were fabricated. Capacitance of these structures was measured and using the relative permittivity from the above experiment the AlO_X thicknesses were extracted. Then the data was extrapolated to obtain the AlO_X thickness formed on the surface of aluminium after a single 60-minute UV/ozone exposure step.

Finally, Section 4.8 summarizes and discusses the experimental findings of the Section 4.1.

4.2 LEAKAGE CURRENT DENSITY

Figure 4.1 shows the leakage current densities of MIM (capacitor) structures (see Section 3.4.1) with AlO_X prepared using different UV/ozone exposure times. In these experiments the bottom aluminium metal was exposed once to the UV/ozone to produce AlO_X on its surface. In some structures, a monolayer of 1-octylphosphonic

acid was thermally evaporated on top of AlO_X before the top Au electrode was formed. The figure shows three different capacitor areas and two different MIM topographies. The leakage current density is reported at a voltage of 1 V. The triangular points represent the leakage current densities of AlO_X capacitors and the circular points indicate the leakage current densities of AlO_X/1-octylphosphonic acid capacitors. Three graphs correspond to three different capacitor areas to understand the effect of the capacitor area and the topography on the current flowing through the dielectric. Each point on the graph represents an average of 5 capacitor measurements and the error bars are the standard deviations.

Figure 4.1.a represents the leakage current densities of the planar capacitors with an area of 0.023 mm^2, which were the smallest fabricated capacitors. The leakage current densities of AlO_X capacitors were in the order of $(2\text{-}8)\times10^{-5}$ A/cm^2 and the complementary AlO_X/1-octylphosphonic acid capacitors had a current density of $(1\text{-}8)\times10^{-6}$ A/cm^2. When a monolayer of 1-octylphosphonic acid was added on top of AlO_X, the leakage current densities were suppressed approximately by one order of magnitude. At the same time, the UV/ozone exposure time did not have significant effect on the leakage current densities.

Figure 4.1.b depicts the leakage current densities of the planar capacitors with an area of 0.28 mm^2. This area is one order of magnitude bigger than the area of the capacitors shown in Figure 4.1.a. In this case the leakage current densities of AlO_X capacitors were in the order of (8-15) A/cm^2 and the corresponding AlO_X/ 1-octylphosphonic acid capacitors had current density of $(2\text{-}6)\times10^{-6}$ A/cm^2. The data shows that the leakage current density was decreased by 6 to 7 orders of magnitude by adding the alkyl phosphonic acid.

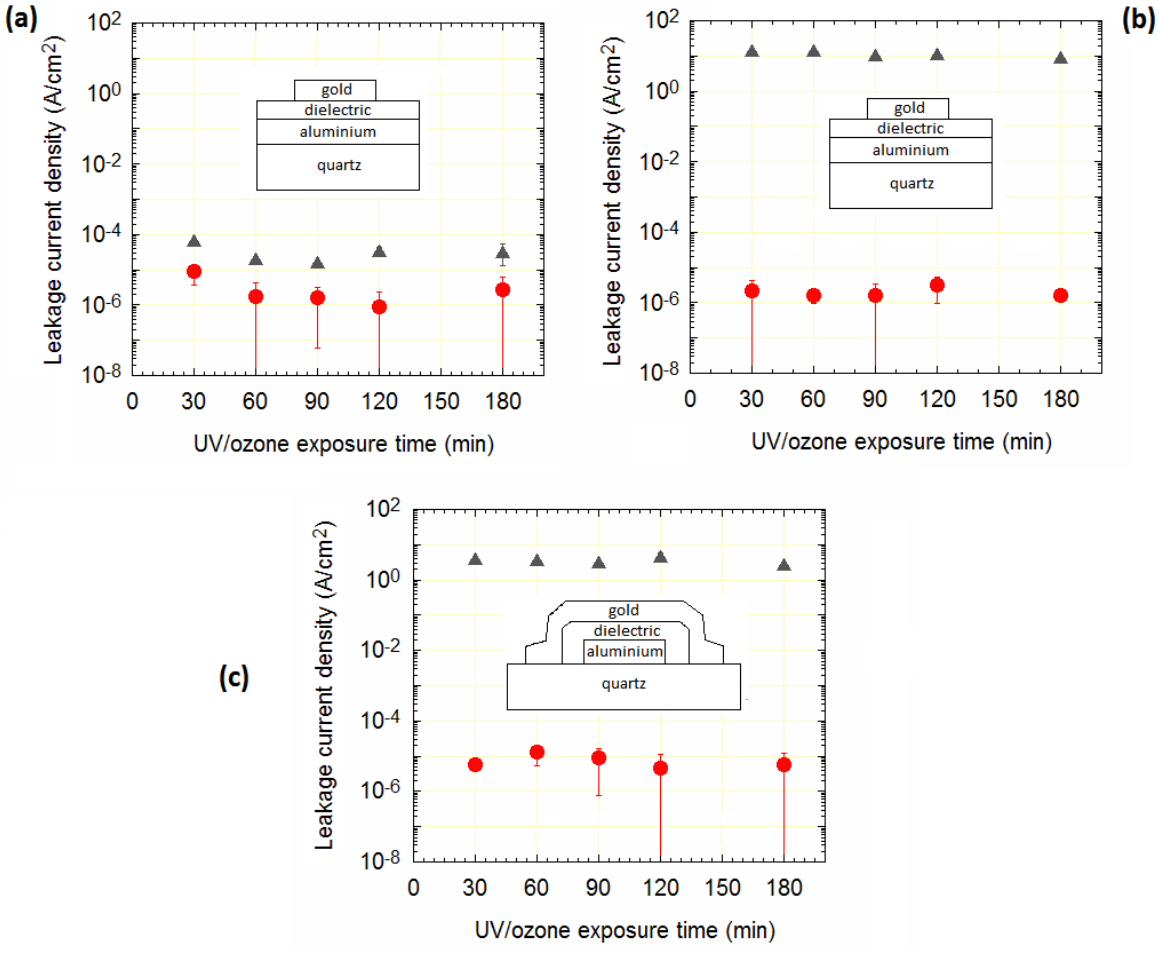

Figure 4.1. Leakage current densities of AlO_X (▲) and AlO_X coated with 1-octylphosphonic acid (●) capacitors where AlO_X is prepared by using different UV/ozone exposure times. Capacitor area: (a) 0.023mm^2 (b) 0.28 mm^2 (c) 0.39 mm^2

Figure 4.1.c shows the current densities of the cross-over capacitors with an area of 0.39 mm^2. In addition to a different topography, the area of these capacitors is slightly larger than that of capacitors shown in Figure 4.1.b. The leakage current densities of AlO_X capacitors are (3-8) A/cm^2 and the AlO_X/1-octylphosphonic acid capacitors exhibit current densities of (8-11)×10^{-6} A/cm^2. The leakage current densities have decreased by 6 orders of magnitude by adding the monolayer of alkyl phosphonic acid, which is similar to the data shown in Figure 4.1.b.

The results show that the area of the capacitor has large effect on its leakage current density. The leakage current density of AlO_X capacitors is reduced by many

orders of magnitude for the smallest area. This may be an indication of low-density pin-holes and/or formation of defects that provide easy passage for charge carriers. However, the ability of 1-octylphosphonic acid to suppress the leakage current density is exceptional.

The increasing UV/ozone exposure time does not have much influence on the leakage current densities of capacitors with large area. For the smallest AlO_X and AlO_X/1-octylphosphonic acid capacitors the leakage current density is highest for the 30-minute oxidation and somewhat reduced for longer oxidation times. This is likely a result of increased AlO_X thickness with rising oxidation time. Finally, the capacitors with aluminium exposed to UV/ozone for less than 60 minutes exhibited low yield and were often shorted.

4.3 CAPACITANCE

Figure 4.2 summarizes the capacitance measurements of the MIM structures described in Section 4.2. As mentioned in the previous chapter, the capacitances have been measured by varying the frequency from 1 kHz to 5 MHz with a d.c. bias of 1 V and an a.c. oscillation amplitude of 50 mV. An example of such measurements is shown in Figure 3.11. One should note that the capacitance measurements of AlO_X capacitors were disturbed by high leakage currents and in most cases it was not possible to obtain any values. The two data points shown in Figure 4.2.a serve mostly as evidence for the presence of the alkyl phosphonic monolayer in some MIM structures, since structures with added alkyl phosphonic acid exhibit capacitance that is about a factor of two to three lower than that of structures with AlO_X only.

The measured capacitances indicate that the topography of the capacitor has only minor effect on the capacitance because both structures provide comparable capacitances. By adding the monolayer of 1-octylphosphonic acid the leakage current was suppressed by many orders of magnitude and allowed the measurement of capacitance as a function of frequency. We did not see any significant changes in the capacitance as a function of the UV/ozone exposure time for structures that include alkyl phosphonic acid. Similar capacitance values indicate that the ratio of the relative permittivity and the thickness of the AlO_X remains approximately constant with increasing UV/ozone exposure time. It could also mean that the increase in the AlO_X thickness between 30- and 180-minute oxidation is small. Finally, the yield of the fabricated capacitors was high when UV/ozone exposure time of at least 60 minutes was used.

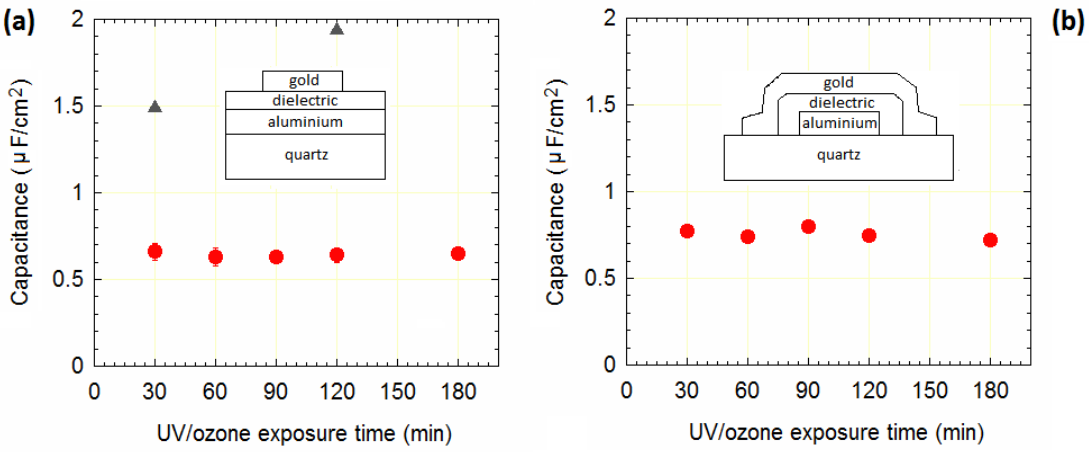

Figure 4.2. Capacitance of AlO_X (▲) and AlO_X coated with 1-octylphosphonic acid (●) capacitors where AlO_X is prepared by using different UV/ozone exposure times.
Capacitor area: (a) 0.028mm^2 (b) 0.39 mm^2

4.4 BREAKDOWN VOLTAGE

Figure 4.3 represents the electrical breakdown voltage measurements of the fabricated capacitors. Breakdown voltage is the voltage at which the dielectric

develops an irreversible electrical short. An example of such measurement is given in Figure 3.10.

The breakdown voltage of AlO_X capacitors increases slightly with rising oxidation time. This may be due to thicker or improved AlO_X with prolonged UV/ozone exposure. The breakdown voltages of AlO_X/1-octylphosphonic acid capacitors are not affected much by the area of the capacitors or their structure. However, the breakdown voltage is improved significantly from (2-3) V to (4.6-4.8) V when 1-octylphosphonic acid is added on top of AlO_X.

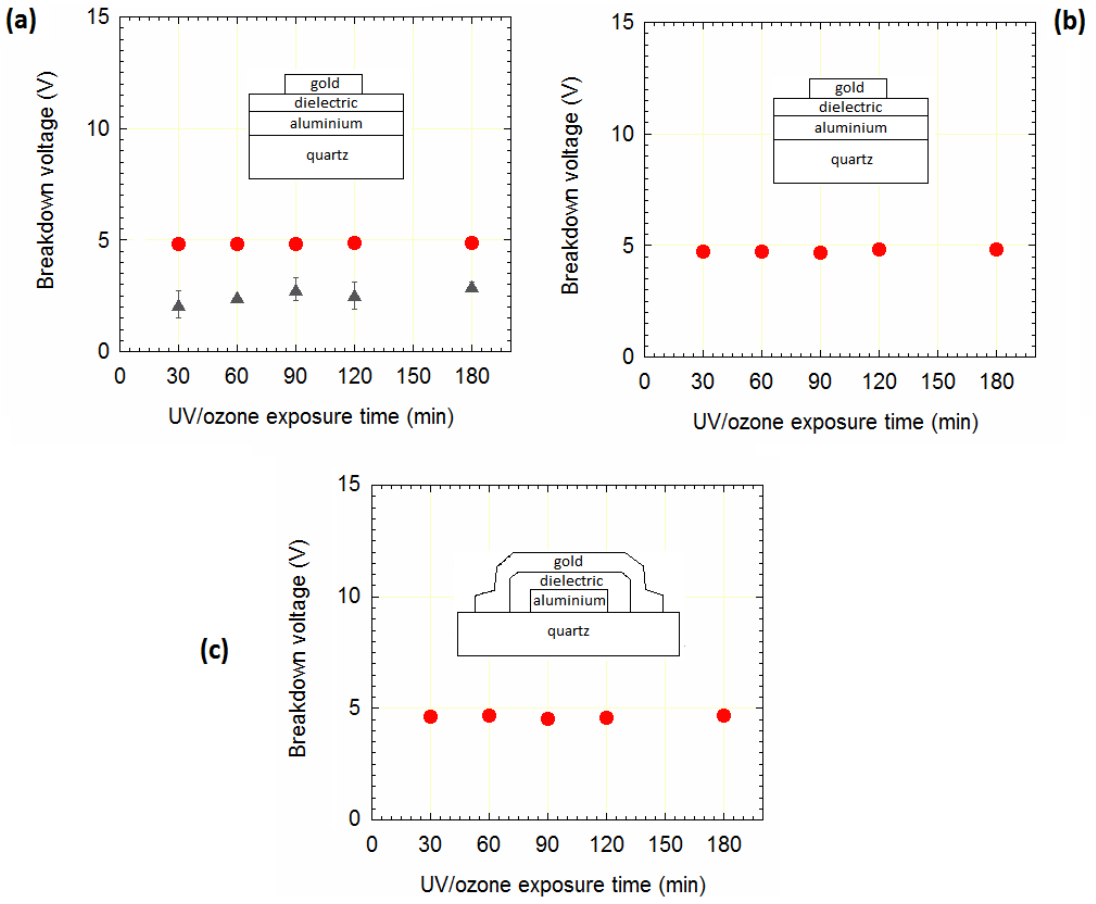

Figure 4.3. Breakdown voltages of AlO_X (▲) and AlO_X coated with 1-octylphosphonic acid (●) capacitors where AlO_X is prepared by using different UV/ozone exposure times. Capacitor area: (a) 0.023mm^2 (b) 0.28 mm^2 (c) 0.39 mm^2

It was not possible to extract any data from the AlO_X capacitors with larger area because they were very leaky and often behaved as ideal resistors. As can be seen from the figure, the UV/ozone exposure time has almost no effect on the breakdown voltage when 1-octylphosphonic acid is added. In addition, comparable values of the breakdown voltages in Figure 4.3.b and 4.3.c suggest good step coverage of the AlO_X by the vacuum deposited 1-octylphosphonic acid which would become important in the OTFT structures.

4.5 AlO_x LEAKAGE CURRENT SUPPRESSION

This section explains how the leakage current density can be suppressed by implementing thicker AlO_X in the MIM structures. The thicker AlO_X is achieved by gradually increasing its thickness using the procedure described in Section 3.1.1. As explained before, thick AlO_X layers were prepared by sequential evaporation of 15 Å-thick layers of aluminium and their oxidation by UV/ozone for 60 minutes. Four different sets of MIM structures with gold electrodes on both sides of AlO_X were fabricated. To vary the AlO_X thickness, 8, 10, 14 and 18 15-Å-thick aluminium layers were sequentially deposited and UV/ozone exposed for 60 minutes. The fabricated capacitors were characterized by measuring their leakage current densities, capacitances and the thickness of AlO_X. As the AlO_X layer becomes thicker, the charge flow is restricted, leading to more resistive AlO_X layers. As expected, the resistance of the AlO_X layer increased with increasing AlO_X thickness. Figure 4.4 shows the leakage current densities of the Au/AlO_X/Au MIM structures where the AlO_X dielectric was built from 8, 10, 14 and 18 15-Å-thick aluminium layers. The corresponding mean AlO_X thicknesses measured with Dektak were 180, 243, 347,

and 438 Å respectively. It is clearly visible that the thinner the dielectric the higher is the leakage current for voltages between 0 and ~ 3 V which is the typical range of operating voltages for low-voltage OTFTs. By increasing the AlO_X thickness from 180 to 438 Å the leakage current density was suppressed by about one order of magnitude. We ascribe the random, sudden increase in the current density occurring around 2 V to the contamination of the samples during lengthy UV/ozone oxidation process. This behaviour is not seen in the OTFTs.

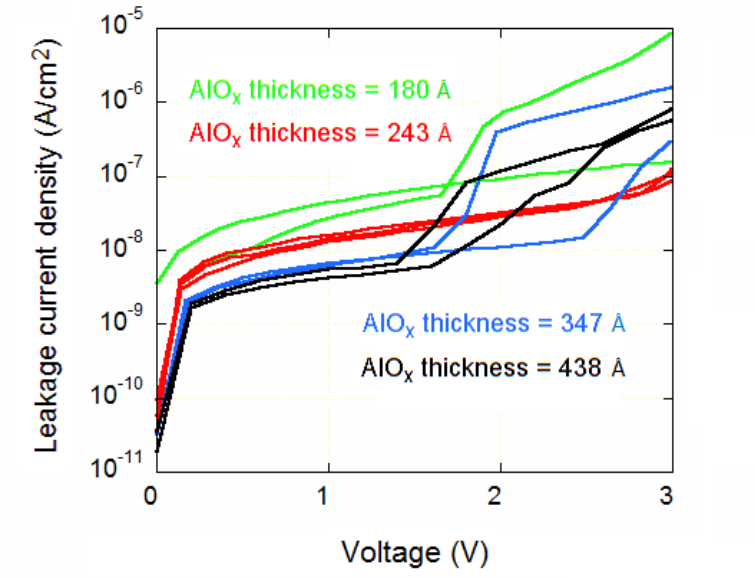

Figure 4.4. Leakage current densities of Au/AlO_X/Au MIM structures with different AlO_X thicknesses. Measurements from 2-3 samples for each AlO_X thickness are shown.

4.6 RELATIVE PERMITTIVITY OF AlO_X PREPARED BY 60-MINUTE UV/OZONE EXPOSURE STEPS

Four Au/AlO_X/Au MIM structures described in the above section were also used to determine the relative permittivity of AlO_X. The AlO_X thickness of each sample was measured using Dektak profilometer. The samples had AlO_X thicknesses of 180, 243, 347, and 438 Å corresponding to the total thickness of aluminium of

120, 150, 210, and 270Å, respectively. This is shown in Figure 4.5 together with a linear fit of the data. This fit must pass through the origin of the coordinate system and can be expressed as y = 1.6305x, where y is the AlO_X thickness and x is the total Al thickness converted to AlO_X through 60-minute UV/ozone oxidations.

The capacitance of the Au/AlO_X/Au MIM structures with different AlO_X thicknesses is shown in Figure 4.6. The plot of $1/C_i$ is also shown to investigate if the relative permittivity k changes with increasing thickness. The more or less linear increase of $1/C_i$ with AlO_X thickness suggests that k is independent of AlO_X thickness.

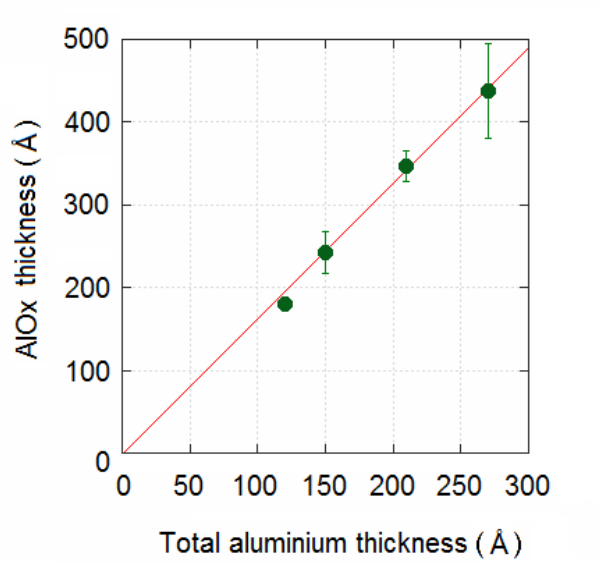

Figure 4.5. AlO_X thickness versus the total thickness of evaporated aluminium. Each data point represents a mean of 10 measurements. Line equation: y = 1.6305x, R^2= 0.99816

Finally, the capacitance and the thickness measurements allowed calculation of the relative permittivity of AlO_X leading to a mean value of 6.80 and a standard deviation of 0.34, as shown in the Figure 4.7. This value is in agreement with a value obtained on Au/AlO_X/1-octylphosphonic acid/Au MIM structures prepared in a similar way [154]. MIM cross-over and planar structures prepared for [154], however, included 1-octylphosphonic acid on top of AlO_X. This led to lower MIM

leakage currents and less challenging capacitance measurements. The relative permittivity obtained from these structures was 6.7 ± 0.4 [154]. These values are slightly lower than the relative permittivity of Al_2O_3 cited in the literature, which indicates that the composition of our AlO_X is not precisely stochiometric. The relative permittivity of Al_2O_3 ranges from ~8 to 11.0 depending on the crystalline form and crystallographic orientation.

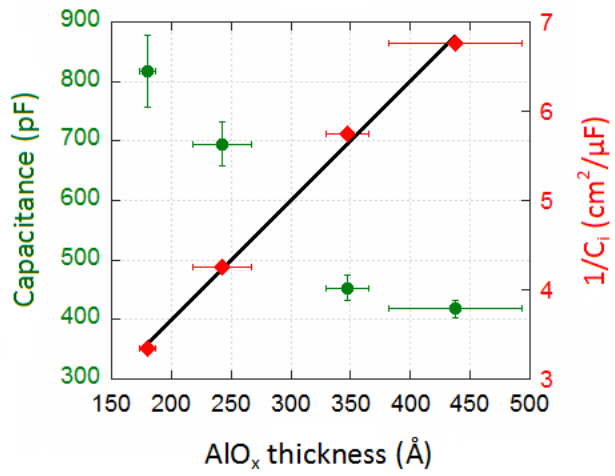

Figure 4.6. Capacitance and inverse capacitance of Au/AlO_X/Au MIM structures. Each data point represents the mean of 10 measurements.

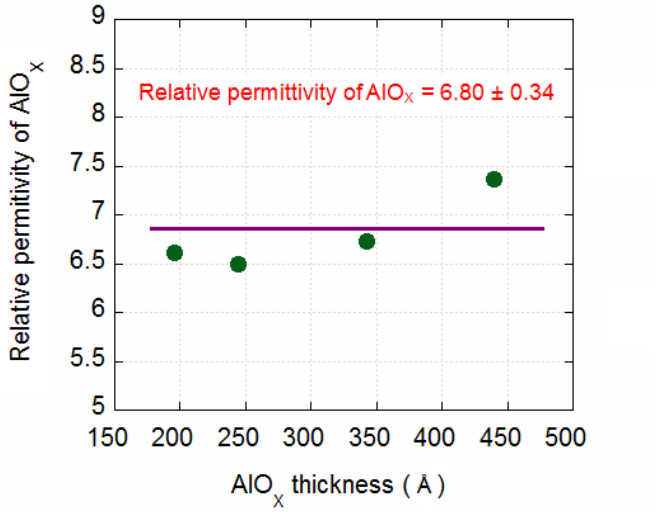

Figure 4.7. Extraction of relative permittivity of AlO_X prepared by 60-minute UV/ozone exposures of thin aluminium layers.

4.7 DETERMINING AlO_x THICKNESS FORMED ON SURFACE OF Al IN A SINGLE UV/OZONE EXPOSURE STEP

When aluminium metal is exposed to the UV/ozone, its surface oxidizes. The oxide is very thin and its thickness is typically determined by spectroscopic ellipsometry. This section describes how one may extract this thickness in a different way. A series of MIM structures with increasing AlO_X thickness is used for this purpose. These structures use Al as the bottom and gold as the top electrode.

In each MIM structure the bottom aluminium metal was first exposed to UV/ozone for 60 minutes. Afterwards, one to six 15-Å-thick Al layers were sequentially deposited and UV/ozone exposed for 60 minutes to increase the AlO_X thickness. This procedure was described in a greater detail in Section 3.1.1.

Capacitance of these MIM structures was measured and the corresponding thicknesses were calculated using the dielectric permittivity obtained in the previous section. Figure 4.8 shows the calculated AlO_X thickness plotted against the number of 15 Å-thick aluminium evaporations. The least-square fit of the data is extrapolated to '0' aluminium evaporations and it allows extraction of the thickness of AlO_X that was formed by oxidizing the bottom aluminium electrode of the MIM structures. As can be seen from the figure, the thickness of AlO_X formed on top of 30-nm-thick aluminium electrode after 60-minute UV/ozone exposure is ~ 70 Å. This value is larger than the ~ 40 Å-thick aluminium oxide obtained by a 5-minute plasma oxidation of aluminium [47]. This is reasonable because we use longer exposure time and the UV/ozone is more reactive than the oxygen plasma itself.

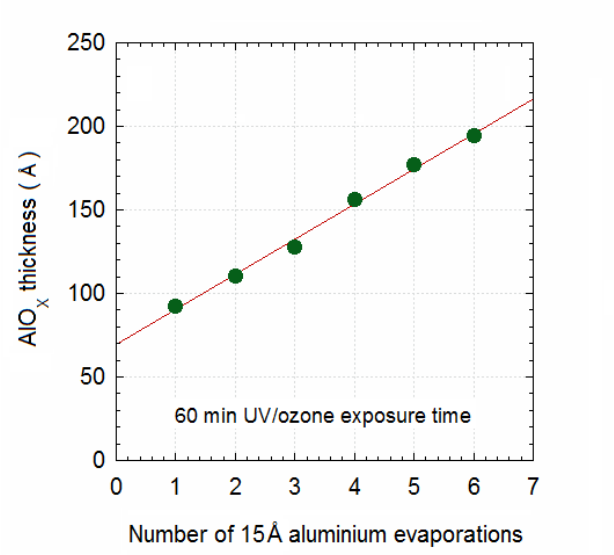

Figure 4.8. AlO_X thickness extraction. Line equation: y = 69.391 + 21.059x, R = 0.99732

Comparing this result with the fit obtained in Figure 4.5, the value of the last point in Figure 4.8 should be 69.391 Å + 1.6305 × 90 Å = 216.1 Å. The measured experimental point shown in Figure 4.8 is 10% lower and confirms good agreement between these two experiments. The main contribution to this error is likely to come from the thickness measurement of the AlO_X layers thinner than 20 nm.

However, the extrapolated thickness of 69.4 Å may be overestimated. If one assumes that the thickness of the AlO_x produced by UV/ozone oxidation increases as a function of the square root of time (similar to SiO_2 growth on Si), then the single, 60-minute UV oxidation leads to oxide thickness that is $\sqrt{120}/\sqrt{60}$ = 1.41 times smaller than the one produced by a 120-minute oxidation.

4.8 Discussion

A dry, inorganic/organic bilayer dielectric of AlO_X functionalized with 1-octylphosphonic acid monolayer has been demonstrated in this Chapter. AlO_X

preparation by UV/ozone exposure has been investigated systematically by measuring the capacitance, breakdown voltage and current density of various AlO_X and AlO_X/8PA MIM structures as function of oxidation time and structure topography. The relative permittivity of the AlO_X prepared by sequential UV-ozone exposure of 15-Å-thick Al layers has been extracted. Finally, an attempt has been made to extrapolate the AlO_X thickness obtained in a single 60-minute oxidation step. As mentioned above, this extrapolated thickness is likely to be an upper limit of the actual AlO_X thickness.

The properties of AlO_X prepared by UV/ozone oxidation in ambient air presented in this chapter are in a reasonable agreement with those obtained for AlO_X prepared by other techniques, as summarized in Table 8. The relative permittivity of 6.8 obtained in this chapter is lower than that achieved by pulsed or atomic layer deposition and short oxygen plasma exposure. It is higher though than the one obtained by mild air plasma or longer oxygen plasma. On the other hand, the UV/ozone oxidation leads to high electric breakdown field surpassed only by the pulsed layer deposition. Among the sub-100-Å oxides, the UV/ozone oxidation leads to slightly higher leakage current density if compared to oxygen plasma oxidation but it surpasses the mild air plasma oxidation by 3 orders of magnitude. Based on these results the UV/ozone oxidation seems reasonably attractive for low-voltage OTFTs.

When 1-octylphosphonic acid is deposited on AlO_X prepared by UV/ozone oxidation, the total dielectric thickness is increased to ~80 Å and the measured capacitance is 0.64 $\mu F/cm^2$. On adding approximately a monolayer of 1-octyl phosphonic acid the leakage currents are reduced by an order of magnitude for small-

area capacitors and by 6 orders of magnitude for large-area MIM structures, indicating the presence of defects in the AlO_X layer.

Table 8. Comparison of AlO_x presented in this Chapter and AlO_x prepared by other methods.

AlO_x preparation	AlO_x thickness (Å)	k_{AlOx}	Time (min)	Electric breakdown field (MV/cm)	Leakage current density (A/cm^2)	Ref
UV/ozone exposure	~69	6.8±0.34	60	3.6	2×10^{-5} @ 1 V	This work
Oxygen plasma	50	6.2	10	3	1×10^{-7}@ 1 V	[224]
Oxygen plasma	36	9	2	1.22	~4×10^{-7}@ 1 V	[225]
Mild air plasma	36	5	2	1.11	~2×10^{-2}@ 1 V	[225]
Rf magnetron Sputtering	1900	~7	60	~3		[226]
Pulsed layer deposition	3300	9		~7	6×10^{-8}@33 V	[227]
Atomic layer deposition	590	10.3				[228]
Anodization	85			1.54		[229]

When compared to the work done by Jedaa et al. [225] (see Table 9) it is clear that the 'dry' 1-octylphosphonic monolayer is quite effective in supressing the leakage current when compared to 'wet' 1-octadecylphosphonic acid, even though it is ~ 50% shorter. The capacitance and the breakdown voltages of the 'dry' AlO_X/8PA MIM structures reported in this work are comparable to those obtained for 3.6-nm-thick AlO_X prepared by oxygen plasma and functionalized with a monolayer of 1-octadecylphosphonic acid.

Table 9. Comparison of AlO_x/SAM presented in this Chapter and the results obtained in [225].

AlO_x preparation	SAM	SAM preparation	Total thickness (Å)	Capacitance /area ($\mu F/cm^2$)	Electric breakdown field (MV/cm)	Leakage current density (A/cm^2)
UV/ozone exposure	1-octyl phosphonic acid	thermal evaporation	~69+10	0.64	4.8	2×10^{-6} @ 1V
Oxygen plasma	1-octadecyl phosphonic acid	dip coating	36+24.4	0.67	5	5×10^{-7}@ 1V
Mild air plasma	1-octadecyl phosphonic acid	dip coating	36+24.4	0.38	4	2×10^{-6}@ 1V

4.9 CONCLUSION

Preparation of ultra-thin dielectric layers consisting of AlO_X and a monolayer of 1-octylphosphonic acid was studied. AlO_X dielectrics were prepared by UV/ozone treatment of aluminium electrodes. Since the oxidation is a 'self-limiting' process, thicker AlO_X layers were produced by a sequential deposition and UV/ozone oxidation of 15 Å-thick aluminium layers. Surface modification of AlO_X was achieved with a monolayer of 1-octylphosphonic acid applied by vacuum deposition. The addition of 1-octylphosphonic acid led to a dramatic reduction in the leakage current density and an increase in the breakdown voltage. The measurements indicated that the capacitors have better yield if the UV/ozone exposure was at least 60 minutes. Results also showed that the AlO_X capacitors became very leaky when their area increased. This indicated the existence of 'pin hole' defects in the AlO_X

layer. When a monolayer of 1-octylphosphonic acid was added on top of AlO_X or when the AlO_X thickness was increased by depositing and oxidizing additional 15-Å-thick aluminium layer(s), these pin holes were covered up, leading to a major decrease in the leakage current and a substantial increase in the device yield. By comparing our work to [47] we can conclude that the combination of AlO_X dielectric prepared by UV/ozone exposure and vacuum deposited 1-octylphosphonic acid exhibits similar capacitance and leakage current density as the AlO_X dielectric prepared by oxygen plasma treatment and combined with 1-octadecylphosphonic acid self-assembled from a solution. The relative permittivity of the UV/ozone oxidised AlO_X was 6.80 ± 0.34. The extracted thickness of the aluminium oxide formed by 60-minute UV/ozone exposure of bare aluminium metal was approximately 70 Å. The leakage current density and the capacitance could be controlled by adjusting the thickness of AlO_X layer. However, there was a trade-off between the capacitance and the leakage current density.

5 EFFECT OF UV/OZONE TIME AND AlO_x THICKNESS ON OTFT PERFORMANCE

5.1 INTRODUCTION

Chapter 4 explained the optimization of AlO_X layer prepared by UV/ozone oxidation of aluminium by incorporating it into MIM structures. Chapter 5 presents the results of a similar approach to AlO_X formation; however, the UV/ozone oxidized AlO_X is now implemented as a gate dielectric into the OTFTs. Three sets of transistors were fabricated with the same bottom-gate, top-source-drain structure discussed in Section 3.3.2. Except for the AlO_X layer prepared using different UV/ozone oxidation procedures, all other layers were identical in all transistor sets. Capacitor structures were fabricated alongside the transistors.

Set A and C were fabricated to investigate the effect of UV/ozone exposure time for 'fixed' dielectric thickness. In set B the AlO_X thickness was varied while the UV/ozone exposure time was held at 60 minutes. In addition, the AlO_X thickness

of sets A and C correspond to the lowest and the highest thickness in set B, respectively. Section 3.3.2 provides additional details.

Section 5.2 presents the breakdown voltages and the capacitances of the three sets of transistors obtained from the capacitor structures. Section 5.3 provides results of the detailed evaluation of these OTFTs and summarizes the threshold voltages, inverse subthreshold slopes, field-effect mobilities, and transistor on- and off-currents as functions of UV/ozone exposure time and increasing AlO_X layer thickness. Finally, the transistor results are summarized in Section 5.4.

5.2 CAPACITANCE AND THE BREAKDOWN VOLTAGE OF THE GATE DIELECTRIC

The capacitance and the gate dielectric breakdown voltages were measured using the capacitor structures fabricated alongside the OTFTs. In some cases we calculated the thicknesses of the aluminium oxide layers from the capacitance measurements by using the relative permittivity of AlO_X, k = 6.8, determined previously. All transistors shared the same history. Although the variation in the transistor performance was not studied, they exhibited high yield and similar performance.

Figure 5.1.a shows the gate dielectric capacitance as a function of UV/ozone exposure time for set A. In this case the AlO_X layer consists of oxidized aluminium gate plus one additional oxidized 15-Å-thick Al layer. Figure 4.9.b shows the capacitance as a function of AlO_X thickness produced by 60-minute UV/ozone exposures for set B. Here the number of oxidized 15-Å-thick Al layers is varied

from 1 to 6. Figure 5.1.c shows the capacitance as a function of UV/ozone exposure for set C. This set is similar to set A except the thickness of AlO_X is approximately double of that of set A. The capacitance of set A is about 0.45 μF/cm^2 and there is a very slight decrease in capacitance with increasing UV/ozone exposure time.

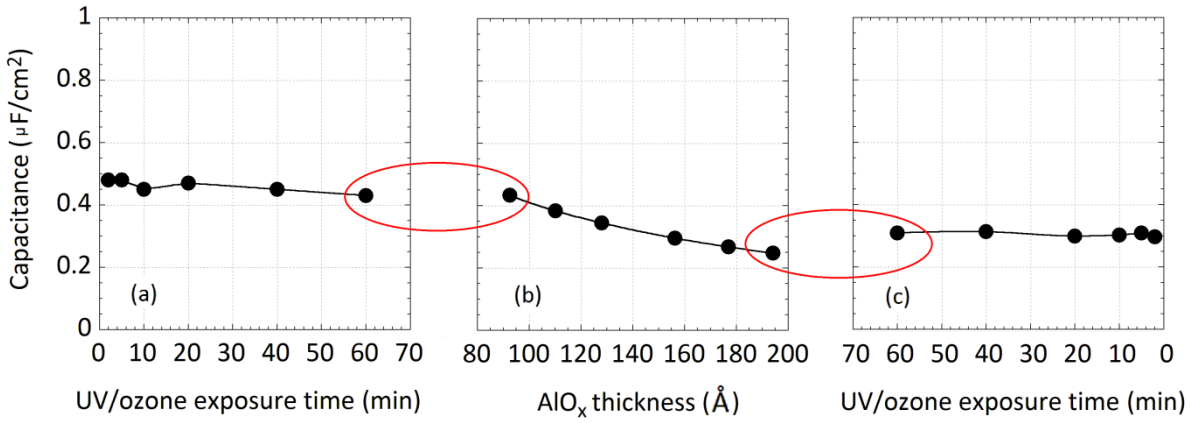

Figure 5.1. Gate dielectric capacitance for sets A (a), B (b) and C (c). Note the reversed x-scale in (c).

From Figure 5.1.b we can see that, as expected, as the thickness of AlO_X layer is increased the capacitance is decreased. The change in capacitance also indicates that the AlO_X thickness is increasing in approximately equal increments from sample to sample. Figure 5.1.c depicts the capacitance of set C. In this case the capacitance is around 0.30 μF/cm^2 and independent of UV/ozone exposure time. The average gate dielectric capacitance of set C is smaller than that of set A because the AlO_X thickness is bigger. Samples within set A (Figure 5.1.a) have approximately the same AlO_X thickness as the sample with the thinnest AlO_X layer in set B (the left-most data point in Figure 5.1.b), also indicated by similar capacitance values. Similarly, the thickness of AlO_X in set C (Figure 5.1.c) is similar to the sample with the thickest AlO_X layer in set B (the right-most data point in Figure 5.1.b). In addition, the samples represented by the right-most data point in Figure 5.1.a and the left-most data point in Figure 5.1.b were prepared according to the same exact

fabrication recipe at different times. Similarly the samples represented by the right-most data point in Figure 5.1.b and the left-most data point in Figure 5.1.c were prepared at different times following the same fabrication procedure. Small changes in the capacitance are seen in set A. In general, there is a decrease in capacitance with rising UV/ozone exposure time which indicates increased AlO_X thickness. For practical applications lower exposure time would be desirable as it would shorten the overall fabrication time.

Figure 5.2 represents the gate dielectric breakdown voltage of three sets of MIM structures. The breakdown voltage does not change much with increasing UV/ozone exposure time, although it reaches slightly higher values for longer UV/ozone times (see Figures 5.2.a and 5.2.c). For set C 20-minute UV/ozone exposure of aluminium leads to the same breakdown voltage as for all longer exposures. Consequently, the 20-minute UV/ozone exposure time is sufficient to form a dielectric with improved electrical breakdown characteristics. Figure 5.2.b shows a gradual increase in the breakdown voltage with increasing AlO_X thickness. The breakdown voltage rises from 5 to 12 V as the AlO_X thickness increases from 93 Å to 194 Å. As mentioned previously, the right-most point in Figure 5.2.b and the

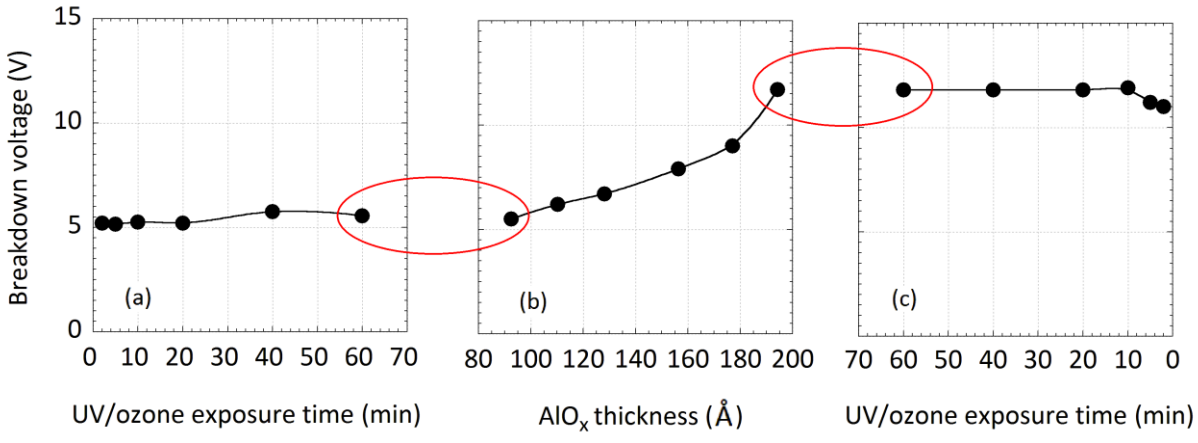

Figure 5.2. Gate dielectric breakdown voltage for sets A (a), B (b) and C (c). Note the reversed x-scale in (c).

left-most point in Figure 5.2.c correspond to capacitor samples prepared according to the same recipe. Similarly, the right-most point in Figure 5.2.a and the left-most point in Figure 5.2.b corresponds to transistor samples prepared using the same recipe. Similar values indicate good reproducibility of the gate dielectric preparation between different growth runs. In all cases the electric breakdown field is at least 5 MV/cm.

5.3 TRANSISTOR PERFORMANCE

The transfer characteristics of one OTFT are shown in Figure 3.12. The output characteristics are shown in Figure 3.13 (see Section 3.4.3). This OTFT had the following performance: charge carrier mobility $\mu_p \approx 0.08$ cm^2/Vs, the threshold voltage $V_t \approx -1.9$ V, subthreshold slope $S \approx 120$ mV/decade, on-off current ratio $\approx 1\times10^6$ and the off-current ≈ 1 pA.

Figure 5.3 represents the threshold voltages calculated using the MOSFET equation in the saturation regime for sets A, B and C. The figure includes data for OTFTs with all nominal channel lengths of L = 30, 50, 70, and 90 µm. W = 1000 µm in all transistors. Figure 5.3.a (set A) shows that as the UV/ozone exposure time increases the threshold voltage decreases and this behaviour is independent of the channel length of the transistor. The decrease in the threshold voltage is faster for shorter exposure times and reduces after ~ 20-minute UV/ozone exposure time. Figure 5.3.b (set B) gives the threshold voltage as a function of AlO_X thickness for different channel lengths. There is a slight decrease in the threshold voltage as the exposure time increases, dropping from ~ –1.45 V to ~ –1.35 V. Different channel

lengths of the transistors show approximately the same behaviour. Figure 5.3.c represents the threshold voltages for thickest AlO_X layer as a function of UV/ozone exposure time. Here the UV/ozone exposure time has similar effect on the threshold voltage of the transistors as in Figure 5.3.a. However, the data points are shifted downward by ~ 0.2 V. The right-most data points in Figure 5.3.a and the left-most data points in Figure 5.3.b correspond to samples prepared according to the same recipe at different times. Similarly, the right-most data points in Figure 5.3.b and the left-most data points in Figure 5.3.c correspond to samples prepared according to the same recipe at different times. This indicates good reproducibility of our fabrication process.

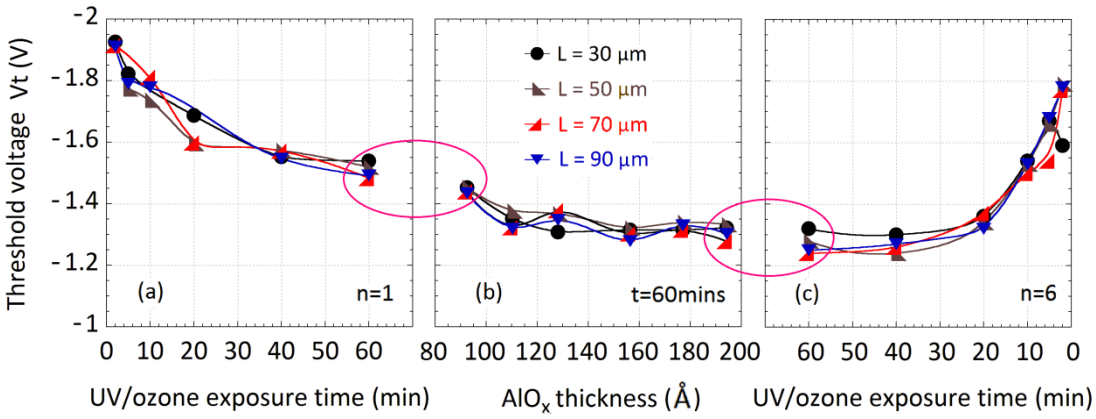

Figure 5.3. OTFT threshold voltage of sets A (a), B (b) and C (c) calculated from the saturation regime. Note the reversed x-scale in (c).

To summarize, the threshold voltage varies between ~ –1.2 V and ~ –2 V as a function of the AlO_X preparation conditions. A fixed positive charge in the AlO_X layer would lead to more negative threshold voltage and may explain the higher $|V_t|$ for short UV/ozone oxidation. Lower operating threshold voltages are desirable for implementation of the transistors in the circuits, indicating that longer exposure times and thicker AlO_X layers would be needed. On the other hand, shorter oxidation times would lead to faster fabrication process and therefore be of interest.

Figure 5.4 summarizes the inverse subthreshold slopes for all three transistor sets. There seems to be a spread in the data and the values of inverse subthreshold slope vary from ~ 100 mV/decade to ~ 250 mV/decade. From Figure 5.4.b we can see that the subthreshold slope is slightly higher for thicker AlO_X, while the UV/ozone exposure does not have much effect (Figures 5.4.a and 5.4.b). Overall, the lowest values are obtained for the thinner AlO_X layer with shorter UV/ozone exposure time. Since the subthreshold slope is controlled by the interface between the 1-octylphosphonic acid and pentacene, one would not expect change in its value with changing AlO_X preparation conditions.

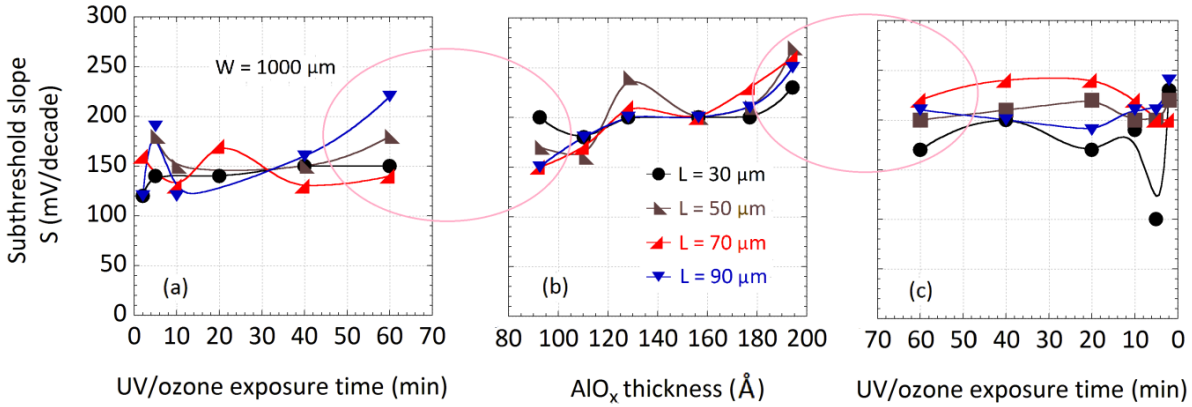

Figure 5.4. OTFT inverse subthreshold slope of sets A (a), B (b) and C (c). Note the reversed x-scale in (c).

Figure 5.5 depicts the field-effect mobilities calculated from the saturation regime of the three transistor sets. In set A (Figure 5.5.a, thinnest AlO_X layer) transistors with the shortest UV/ozone exposure time of 2 minutes exhibit the highest mobility of up to $\approx 0.084 cm^2/Vs$. When the thickness of the gate dielectric is increased (Figure 5.5.b, 60-minute UV/ozone exposure time) the mobility remains more-or-less unchanged. Similarly, for thicker AlO_X layer the UV/ozone time does not have much effect on the hole mobility. The values are more scattered for

UV/ozone exposure times less than 20 minutes. Based on Figure 5.5 there is no clear correlation between the hole mobility and the channel length.

The OTFT mobility is primarily controlled by the pentacene grain size and the interface between 1-octylphosphonic acid and pentacene. Therefore, changes among various transistors with similar *L* are not expected. However, if the contact resistance between the source/drain contacts and the channel is high, compared to the channel resistance, one may observe a decrease in the mobility with decreasing channel length. Even though Figure 5.5.b seems to suggest such behaviour, Figures 5.5.a and 5.5.c do not. Consequently, the variation in the mobility is likely a result of the non-optimized growth of 1-octylphosphonic acid monolayer.

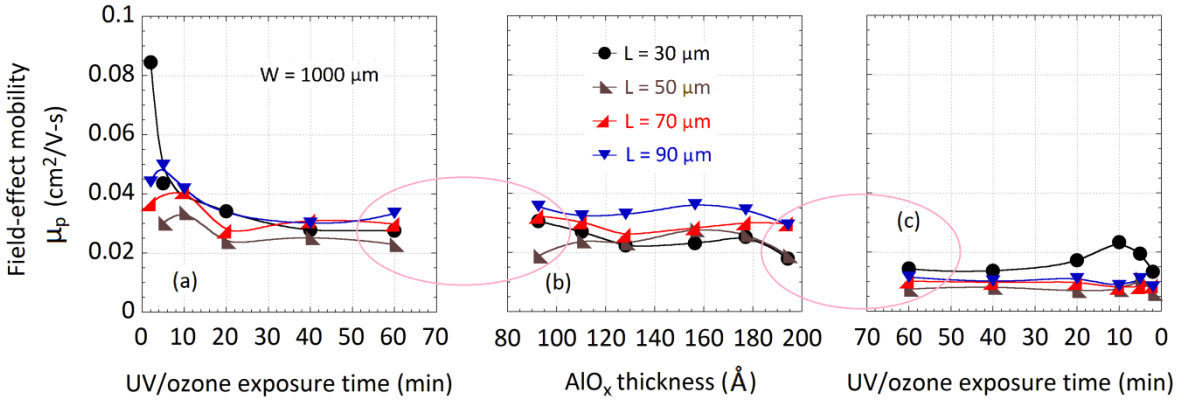

Figure 5.5. OTFT field-effect mobility of sets A (a), B (b) and C (c) calculated from the saturation regime. Note the reversed x-scale in (c).

Figure 5.6 shows the off-currents of the three sets of transistors. There is a larger spread in the values of the off-currents for samples with thinner AlO_X layer (Figure 5.6.a) as compared to the thicker one (Figures 5.6.b and 5.6.c). Shorter UV/ozone exposure times have a similar effect but to a lesser degree (see Figure 5.6.c). As expected, the AlO_X thickness does not affect the off-currents of the OTFTs (see Figure 5.6.b). In addition, Figure 5.6.c suggests that thicker AlO_X layer

might lead to better transistor uniformity. As shown in Figure 5.2, thicker AlO_X layer also leads to higher breakdown voltage of the transistors.

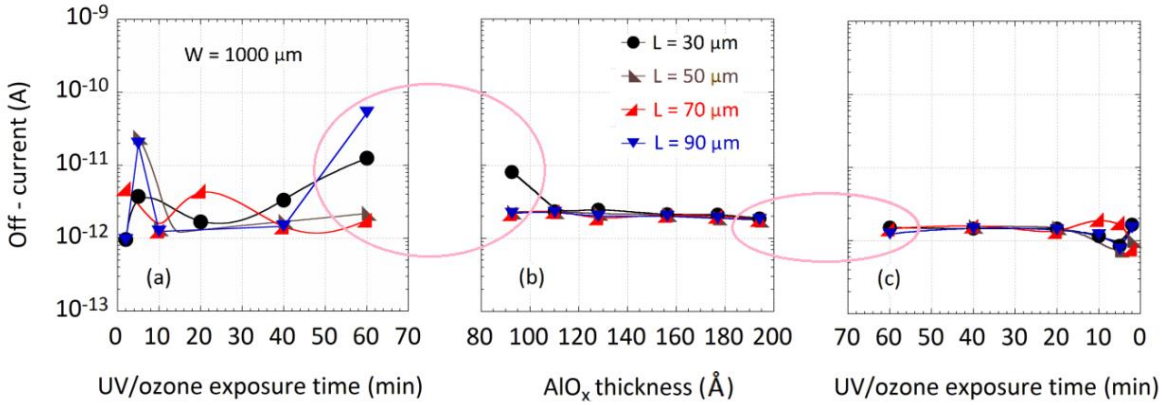

Figure 5.6. Transistor off-current for sets A (a), B (b) and C (c). Note the reversed x-scale in (c).

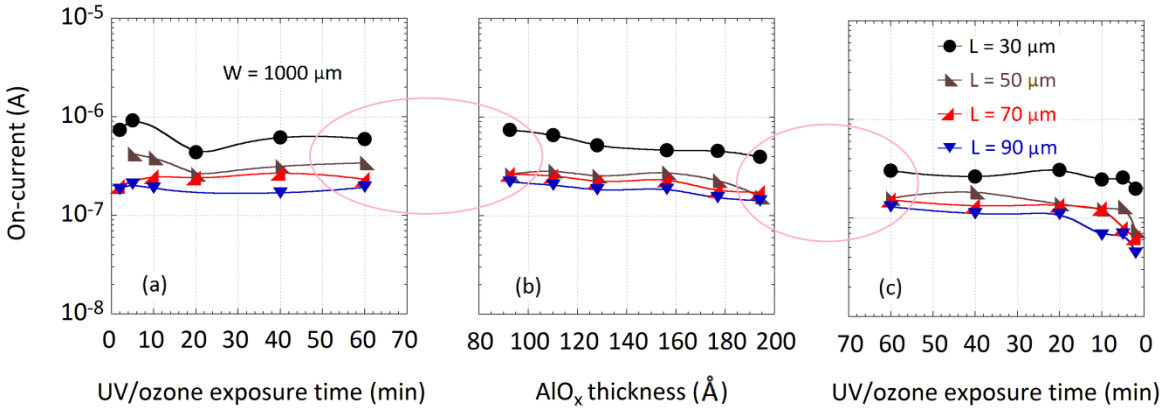

Figure 5.7. Transistor on-current for sets A (a), B (b) and C (c). Note the reversed x-scale in (c).

Figure 5.7 represents the transistor on-currents. The on-currents are defined as the drain current for V_{ds} = –3 V and V_{gs} = –3 V. From Figure 5.7 it is clearly evident that the OTFTs with channel lengths of 30 µm have the highest transistor on-currents. As expected, the on-current decreases as the channel length increases. The increase in the AlO_X thickness also decreases the transistor on-current because the gate dielectric capacitance decreases as the dielectric thickness increases (see Figure

5.7.b). We also note the reproducibility of the on-currents by comparing similar transistors fabricated at different times and marked with an oval.

5.4 DISCUSSION

Table 10 compares the performance of pentacene OTFTs based on AlO_X/8PA bilayer dielectric presented in this chapter to OTFTs, fabricated by others, that utilize dielectric of a similar thickness and composition.

Table 10. Comparison of OTFTs presented in this Chapter to transistors with similar dielectrics.

Dielectric	d (Å)	C_i ($\mu F/cm^2$)	μ_p ($cm^2/V\text{-}s$)	V_t (V)	S (mV/decade)	On/Off ratio	Ref
AlO_x/8PA	90/10	0.43	0.02–0.04	-1.43– -1.54	140–222	$(1–4)\times10^5$	This work
AlO_x/10PA	50/12		0.54	-0.22		6×10^4	[206]
AlO_x/6PA	50/8		0.40	-0.02		2×10^4	[206]
AlO_x/10PA	36/12	0.86	0.15			2×10^6	[225]
AlO_x/6PA	36/8	1	0.05			2×10^4	[225]
AlO_x/10PA	36/12	0.78	0.03			5×10^3	[225]
SiO_2/8PA	100/10		1.2	-0.75	500		[208]
HfO_2/8PA	105/10	0.6	0.74	-0.58	110	1×10^6	[131]

The capacitance of the developed dry bi-layer dielectric is the lowest among the reported values, even though the OTFTs with SiO_2/8PA dielectric are expected to exhibit even lower capacitance due to the lower relative permittivity of SiO_2. The field-effect mobility achieved in this project is almost an order of magnitude lower

than that obtained by Fukuda and Hill and comparable to OTFTs with AlO_X/6PA and AlO_x/10PA in [225]. This may be a result of better pentacene optimization (purity, growth) in the case of [206] and [208]. The threshold voltage is higher by ~ −1 V, while the subthreshold slope and on/off current ratio lie in the middle of the reported range. The subthreshold slopes are close to those obtained for hafnia dielectric which indicates comparable properties of the semiconductor/dielectric interface. The on/off current ratio is also comparable to that obtained by Klauk and Hill and this value can be improved once all the OTFT layers are properly optimised. As shown in [229-231] these transistor parameters are affected by the growth of octylphosphonic acid and pentacene that were not optimised in this study. Their optimization leads to lower threshold voltage and subthreshold slope and increased field-effect mobility and on/off current ratio.

Completely dry pentacene OTFT process was also reported by Abbas et al. Compared to their work, the OTFTs presented in this Chapter exhibit similar field effect mobility, substantially lower subthreshold slope and lower threshold voltage that results from the ultra-thin dielectric developed in this project.

5.5 CONCLUSION

This section reported the performance of low-voltage pentacene transistors (and corresponding capacitors) with 18 different AlO_X recipes to study the effect of AlO_X thickness and UV/ozone exposure time on transistor performance. The total thickness of the inorganic/organic bi-layer gate dielectric was varied between ~10 and ~20 nm. Out of that, the thickness of the vacuum deposited 1-octylphosphonic

acid is approximately 1 nm. Since the AlO_X does not form an interface with the organic semiconductor, it was expected that the variation in the AlO_X preparation would mainly affect the leakage current, capacitance and breakdown voltage of the gate dielectric. In addition, the transistor threshold voltage could be affected via immobile charge in the AlO_X prepared using various recipes. Finally, the transistor on-current would be proportional to the capacitance of the gate dielectric and therefore affected by AlO_X preparation.

Indeed, the gate dielectric capacitance decreased from ~ 0.5 to ~ 0.25 $\mu F/cm^2$, the breakdown voltage increased from 5 to 12 V and the gate-source leakage current decreased by a factor of 10 as the gate dielectric thickness increased. The results also demonstrate that the threshold voltage depends primarily on the UV/ozone time and it decreases with increasing UV/ozone exposure time. The threshold voltage varies by ~ 0.7 V as a function of aluminium oxide preparation. The behaviour of the inverse subthreshold slope and the field-effect mobility is not clearly correlated with the AlO_X preparation and the slightly lower mobility achieved for thicker AlO_X and/or longer UV/ozone exposure times may be a consequence of increased surface roughness of the AlO_X layer affecting the growth of the organic monolayer. The lower gate dielectric breakdown voltage and the higher transistor threshold voltage achieved for shorter UV/ozone exposure times indicate insufficient oxidation process, most likely associated with the presence of immobile positive charge in the AlO_X layer. In addition, the transistor yield, uniformity, and reproducibility improve when longer UV/ozone exposure time and/or thicker AlO_X layers are used.

6 EFFECT OF THERMAL ANNEALING OF AlO_X ON OTFT PERFORMANCE

6.1 INTRODUCTION

As discussed before, commercial UV/ozone cleaner is used to convert aluminium into aluminium oxide (AlO_X) for use as gate dielectric in low-voltage organic thin-film transistors based on pentacene. During the oxidation process, the substrate is exposed to ozone, UV light and thermal heating (100°C) caused by the absorption of the UV light. This section describes the results of experiments whose aim was to understand the role of this thermal heating during AlO_X formation, namely, whether the heating itself (without UV/ozone) could provide a beneficial annealing effect and thus improve the transistor performance.

When glass substrates coated with aluminium metal are exposed to UV/ozone, their temperature quickly rises to 100°C due to the UV light absorption by the glass. This elevated temperature may or may not be beneficial to the growing AlO_X layer and, consequently, to the transistor. Therefore, the experiments described

in this section investigate if such heating could improve the quality of the gate dielectric as well as the overall transistor performance.

Since the heating cannot be 'turned off' during the UV/ozone oxidation to provide a comparative study at 100°C and 20°C, transistor set D with six different transistor samples was fabricated. The AlO_X was prepared by applying six different UV/ozone times – 2, 5, 10, 20, 40 and 60 minutes. In addition, each sample underwent a subsequent heating step at 100°C up to a total time of 1 hour. Therefore, the UV/ozone exposure times were 2, 5, 10, 20, 40 and 60 minutes and the additional 100°C annealing steps were 58, 55, 50, 40, 20 and 0 minutes, respectively. To replicate the environment in the UV/ozone cleaner without the UV/ozone, the samples were annealed in a conventional oven in ambient atmosphere.

Section 6.2.1 compares the transistor performance of set D to that of set A from Chapter 5. In set A the UV/ozone oxidation time was 2, 5, 10, 20, 40 and 60 minutes with no additional heating. Gate dielectric breakdown voltages and leakage current densities and OTFT threshold voltages are compared between sets A and D.

In the transistor set D the 100ºC-anneal was fixed at 60 min and the UV/ozone exposure time was varied from 2 to 60 minutes. Transistor set E was prepared to complement set D and the results of set E are discussed in Section 6.2.2. In set E the UV/ozone exposure time was fixed at 60 minutes and the subsequent 140ºC-anneal was varied from 1 to 24 hours. In this case the annealing temperature was raised to 140ºC and the anneal was performed in a vacuum oven for 0, 1, 2, 5, 10 and 24 hours, respectively. All remaining transistor layers in set E were identical.

Summary of both annealing experiments is given in Section 6.3.

6.2 TRANSISTOR RESULTS

6.2.1 OTFT results: AlO_x anneal time fixed, UV/ozone time varied

The gate dielectric capacitance values of sets A and D were quite similar and they did not depend on UV/ozone time or duration of 100°C annealing. Measurement of all 12 different AlO_X recipes (sets A plus D) led to a mean value of 0.49 $\mu F/cm^2$ and a standard deviation of $\pm$ 0.04 $\mu F/cm^2$.

Figure 6.1 shows the gate dielectric breakdown voltage plotted against UV/ozone exposure time for sets A and D. The red triangles represent the breakdown voltage of the capacitors where AlO_X was prepared by UV/ozone exposure followed by annealing at 100°C up to a total time of 60 minutes. The 60-minute UV/ozone treated sample did not undergo additional annealing as it was already heated by the UV light for 60 minutes. The blue circles represent the breakdown voltages of the capacitors where AlO_X was prepared purely by UV/ozone exposure without the additional heating step. Each data point in the graph represents an average of four capacitors and the error bars are the corresponding standard deviations. The data in Figure 6.1 show a slight increase in the breakdown voltage with increasing UV/ozone exposure time for both sample sets. This indicates that the annealing itself neither improves nor impedes the quality of the dielectric with respect to its electrical breakdown. When the variation between alike samples is very small, the standard deviations are not visible in the graph. Finally, the electric

breakdwn field is larger than 5 MV/cm for all AlO_X layers regardless of their preparation.

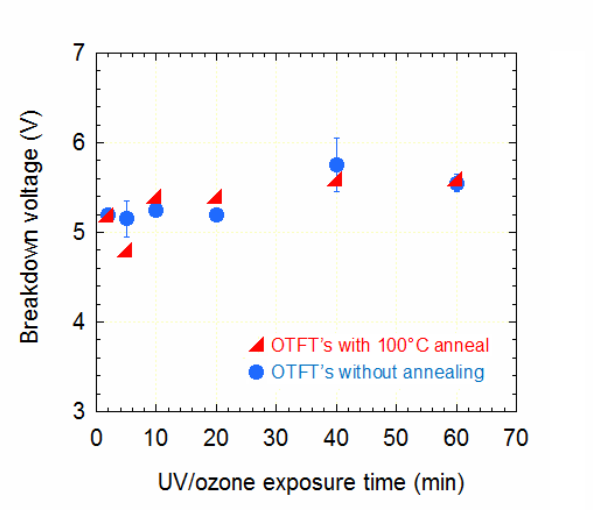

Figure 6.1. Gate dielectric breakdown voltage versus UV/ozone exposure time. OTFTs with (set D) and without (set A) 100°C anneal are shown for comparison.

Figure 6.2 represents the threshold voltages of two sets of transistors. Every data point on the graph is a mean of four OTFTs with different channel lengths. The error bars are the standard deviations. The blue circles represent OTFTs with UV/ozone exposure only, while the red triangles correspond to OTFTs with the same UV/ozone exposure and additional annealing at 100°C. The threshold voltage of the OTFTs in which AlO_X was prepared by UV/ozone exposure without additional heating step decreases with increasing exposure time. OTFTs with AlO_X exposed for 2 minutes have V_t of ~ −1.9 V, while the OTFTs with AlO_X exposed for 60 minutes have V_t of ~ −1.5 V. The OTFTs that underwent additional heating step have a slightly different behavior. Their V_t is ~ −1.72 V for UV/ozone times up to 20 minutes. After 20 minutes, their V_t is similar to that of transistors in set A (no additional heating step). Therefore, the additional 100°C heating step provided slight benefit to OTFTs with AlO_X prepared by short UV/ozone exposure time.

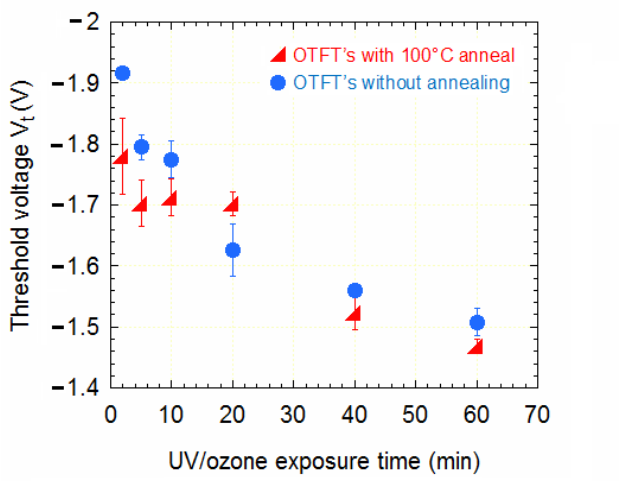

Figure 6.2. OTFT threshold voltages versus UV/ozone exposure time. OTFTs with (set D) and without (set A) 100°C anneal are shown for comparison.

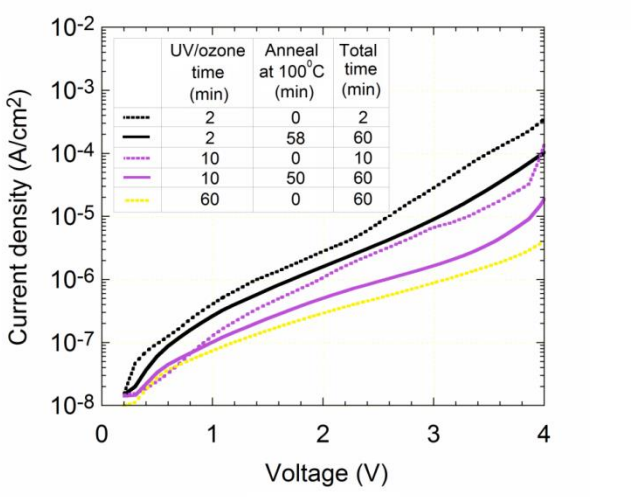

Figure 6.3. Current-voltage dependence of capacitors with AlO_x/1-octylphosphonic acid dielectric. AlO_x was prepared by UV/ozone oxidation (dashed curves) or by UV/ozone oxidation followed by annealing at 100°C (solid curves).

Figure 6.3 shows the current-voltage measurement of capacitors with AlO_x/ 1-octylphosphonic acid dielectric. For samples that underwent UV/ozone treatment only (dashed curves) the leakage current decreases with increasing UV/ozone time. The leakage current density of the capacitors that contain 2-minute-oxidized AlO_x is about 1 order of magnitude higher than that of capacitors that contain 60 minute-oxidized AlO_x. This is a consequence of increasing AlO_x thickness with increasing oxidation time. The solid curves correspond to capacitors in which the AlO_x layer

underwent additional heating. Compared to the non-annealed samples, the added heating step supressed the leakage current density for shorter UV/ozone times.

The remaining transistor parameters, namely the field-effect mobility, off-current, and the subthreshold slope are controlled by the organic semiconductor (pentacene) and the interface between 1-octylphosphonic acid and pentacene No improvement in these parameters was observed when additional annealing was applied.

6.2.2 OTFT results: AlO_x anneal time varied, UV/ozone time fixed

This section discusses the results of an experiment in which the OTFTs were prepared by annealing the 60-minute UV/ozone oxidised AlO_x at 140ºC at 6 different annealing times – 0, 1, 2, 5, 10 and 24 hours, prior to phosphonic acid deposition. The higher annealing temperature and longer annealing times were selected because slight improvement in the threshold voltage was seen in transistor set D for short UV/ozone exposure times.

The first point on all the graphs represents OTFTs which were fabricated without any additional anneal. These OTFTs are similar to the transistors in set D where AlO_x was prepared by 60-minute UV/ozone exposure and they serve as a reference.

Figure 6.4 shows the capacitance per unit area of the MIM strutures that were fabricated side by side with the OTFTs to extract the capacitances and breakdown voltages of the gate dielectric. The data in Figure 6.4 suggest an increase in the

capacitance with increasing annealing time, which would indicate that either the thickness or the relative permittivity of AlO_x has changed. Since it is unlikely that the 140ºC anneal would lead to reduced AlO_x thickness, additional verification was sought to confirm whether the relative permittivity is increased. To test this, the MIM structures discussed in Section 4.5 were annealed for 24 hours at 140ºC and the capacitance was remeasured. The capacitance values before and after the anneal were the same, within the error of measurement, indicating that the 140ºC anneal did not affect the relative permittivity of the AlO_x layer. Consequently, it was concluded that the 140ºC anneal does not affect the capacitance of the gate dielectric.

Figure 6.5 represents the breakdown voltages of the MIM structures. As can be seen from the figure, the breakdown voltage increases slightly after the annealing. The increase in the breakdown voltage is observed already after one hour of annealing and the prolonged annealing does not lead to additional noticeable improvement. Consequently, one can conclude that the 140ºC anneal leads to improved electrical breakdown characteristic of the gate dielecric. Similar increase in the breakdown voltage was observed on capacitor structures of Section 4.5 after their 24-hour anneal at 140ºC in vacuum.

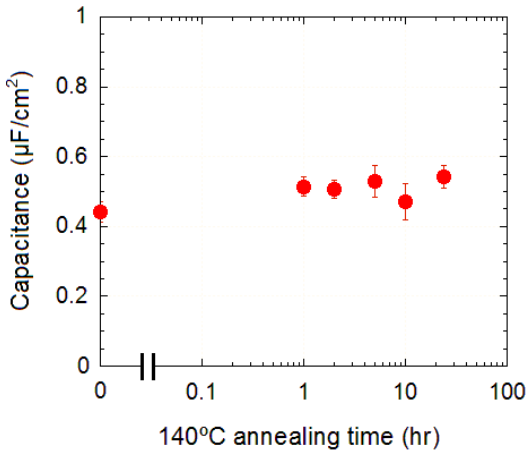

Figure 6.4. Gate dielectric capacitance as a function of 140ºC annealing time.

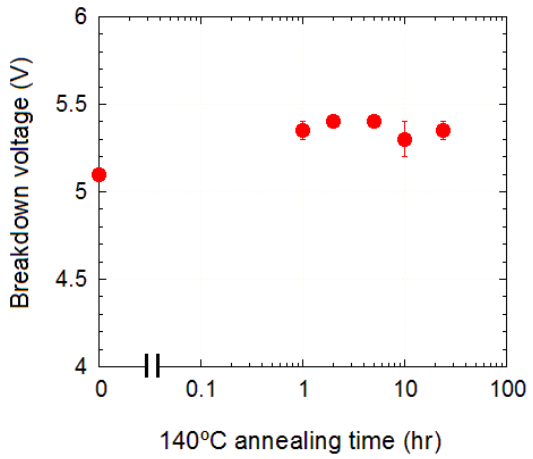

Figure 6.5. Dielectric breakdown voltage versus 140ºC annealing time.

Figure 6.6 depicts the gate current densities as a function of 140ºC anneal duration. These currents are not affected by annealing; they remain the same within the error of measurment. However, they are slightly higher than the leakage currents of set D. This could be the result of a marginally thinner gate dielectric, as indicated by slightly higher capacitance values.

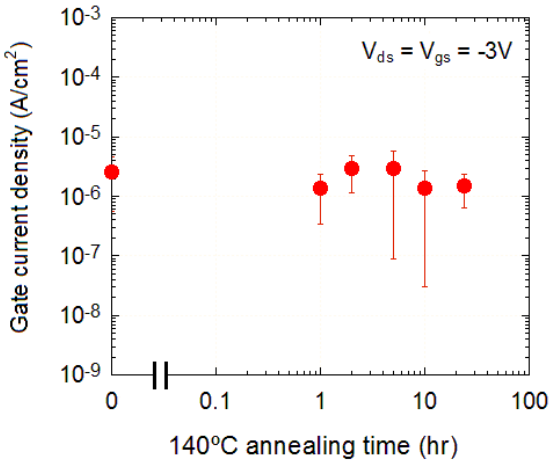

Figure 6.6. Gate current density versus 140ºC annealing time.

Figure 6.7 represents the threshold voltages of the OTFTs. Within the error of measurement the threshold voltages are unaffected by the 140ºC anneal.

Consequently, the 140ºC anneal following the 60-minute UV/ozone oxidation does not provide any additional benefit for the transistor turn-on voltage.

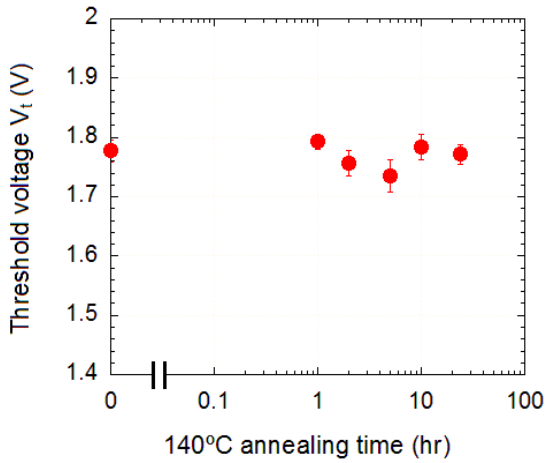

Figure 6.7. OTFT threshold voltage versus 140ºC annealing time.

Figure 6.8 represents the field effect mobility of the OTFTs for different 140ºC anneal times. The mobility exhibits a slight decrease when the annealing step is introduced. This might be because of the changes in the dielectric structure, e.g. surface roughness, which would influence the growth of 1-octylphosphonic acid and the subsequent pentacene grain growth. Consequently, the mobility of the charge carriers in the channel region may be affected. Therefore the 140°C-anneal of 60-minute oxidized AlO_x is not beneficial for the OTFT mobility.

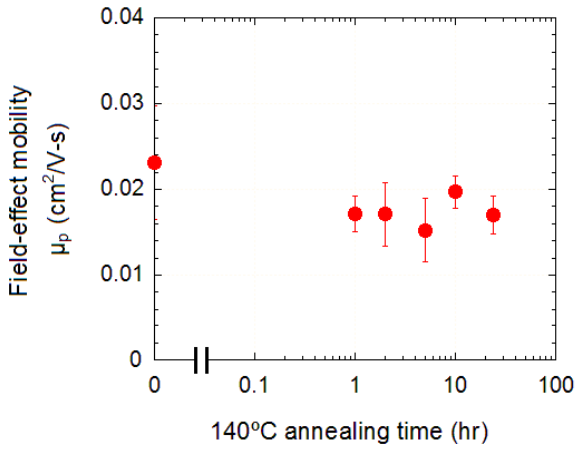

Figure 6.8. OTFT saturation mobility versus 140ºC annealing time.

Figure 6.9 represents the subthreshold slope of the OTFTs. Within the error of measurement it remains the same for different annealing times except the sample where AlO_x was annealed for 24 hours. At present time it is not clear why would the annealing of AlO_x affect the subthreshold slope, unless the morphology of AlO_x was altered by the annealing.

Figure 6.10 represents the OTFT on- and off-currents. On-currents do not change with annealing, but the off-currents are slightly decreased after 2 hours of annealing. This change is not significant.

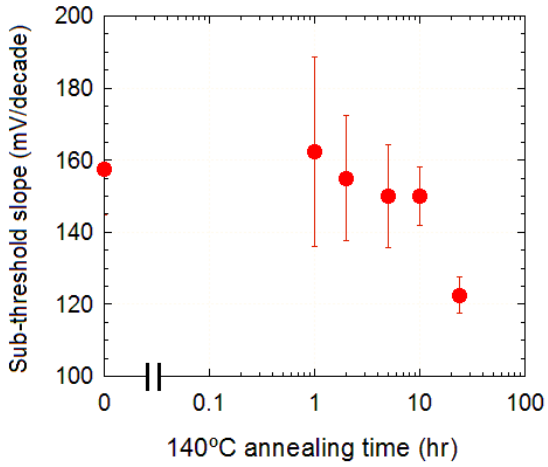

Figure 6.9. OTFT sub-threshold slope versus 140ºC annealing time.

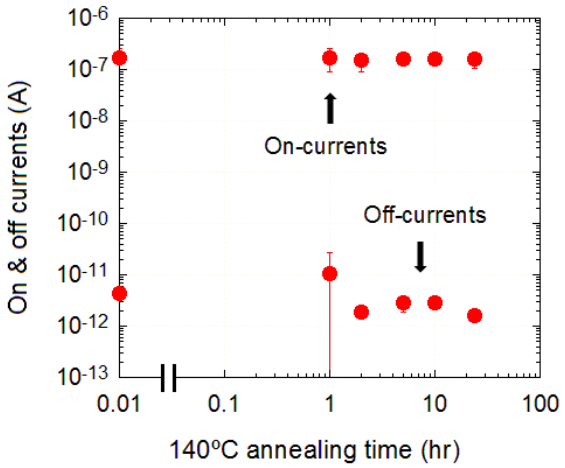

Figure 6.10. OTFT on- and off-currents as functions of 140ºC annealing time.

Figure 6.11 represents the OTFT on/off current ratios. On/off ratios increase with increasing annealing time which is a consequence of the reduced off-currents, as shown in Figure 6.10. But this improvement is quite small and probably would not justify the extra 140ºC-anneal step in the OTFT fabrication process.

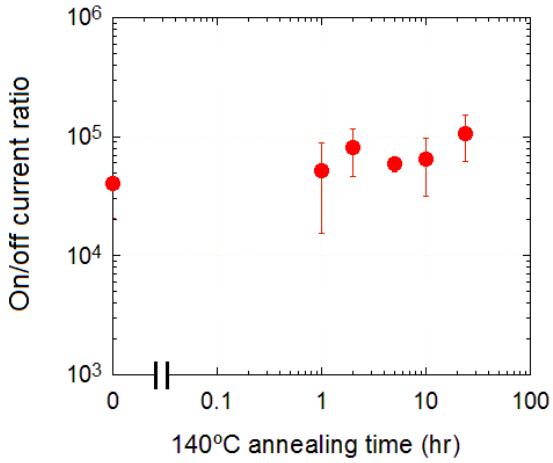

Figure 6.11. OTFT on/off current ratio versus 140ºC annealing time.

6.3 Discussion

The evaluation of the fabricated capacitors and transistors presented in this Chapter showed that while the 100°C anneal improved the gate dielectric leakage current and V_t of the transistors in which the UV/ozone exposure time was up to 10 minutes, the combination of 60-minute UV/ozone exposure and 140°C anneal did not improve these parameters. However, minor improvement in the electrical breakdown voltage was observed for the latter AlO_X/8PA MIM structures.

OTFTs respond to the fixed and/or mobile charge in the gate dielectric and as such provide additional information. The increase in the OTFT threshold voltage with decreasing UV/ozone oxidation time indicates presence of positive charge in the

gate dielectric. This charge must be associated with AlO_X because all transistors share the same alkyl phosphonic layer. Shorter UV/ozone oxidation time during AlO_X preparation leads to a larger amount of positive charge that is reduced by subsequent thermal treatment. However, the thermal treatment performed at 140°C (up to 24 hours) on OTFTs with 60-minute oxidized AlO_x does not provide similar benefit.

The process of aluminium oxidation involves insertion of O atoms into Al network. Experiments with crystalline Al in ultra-high vacuum revealed that when the surface of Al is exposed to ozone, faster oxidation kinetics and thicker oxide layers are produced [232]. This is ascribed to the high reactivity of ozone that decomposes into molecular and atomic oxygen. Oxygen vacancy is a common defect in many oxides and AlO_X with sub-stochiometric oxygen content exhibits greater number of oxygen vacancies [233]. If the oxygen vacancy loses an electron, it becomes positively charged. Short UV/ozone exposure times likely lead to AlO_X with sub-stochiometric oxygen content and hence to a higher density of oxygen vacancies that cause higher transistor threshold voltage. The subsequent thermal treatment reduces the density of these vacancies resulting in lower transistor threshold voltage. One would infer that this effect is localized because the temperature is too low for any significant diffusion of oxygen and/or change in the thickness or morphology of the film. Since the oxygen vacancies are known to provide passage for the electric charge, the reduction in their density after the 100°C anneal would be accompanied by a reduction in the gate dielectric leakage current, as observed in Figure 6.3.

6.4 CONCLUSION

During the oxidation process utilizing commercial UV/ozone cleaners the substrate is exposed to ozone, UV light and thermal heating (100°C) caused by the absorption of the UV light. Since annealing (heating) steps are an established method in the fabrication of various electronic devices to improve their performance, it was expected that the elevated temperature during the UV/ozone oxidation process would not have any detrimental effect on the quality of the formed oxide. On the contrary, based on the wealth of experience gained in the fabrication of silicon-based devices, one might expect an improvement in the device parameters with optimized annealing procedure. The experimental results confirmed that this is the case indeed. In fact, the transistor data showed that the additional 100°C heating step provided slight benefit to OTFTs with AlO_X prepared by short UV/ozone exposure time. Transistors in which AlO_X was prepared by a 2-minute UV/ozone treatment followed by a 58-minute annealing at 100°C exhibited ~ 8% lower threshold voltage than OTFTs employing a 2-minute UV/ozone treatment only; and ~ 12% higher threshold voltage than the transistors with 60-minute UV/ozone exposure and no additional heating step. Therefore, while the 100°C anneal improved the OTFT threshold voltage, the UV/ozone oxidation cannot be shortened and replaced with a heating step to gain the same transistor performance.

From Section 6.2.2 we can summarize that the OTFTs exhibited improvement in the off-currents, the on/off current ratios and the dielectric breakdown voltages after annealing of up to 24 hours. The breakdown voltage increased by 0.3 V after 1 hour of annealing, indicating some improvement in the UV/ozone oxidized AlO_x. This result is in agreement with the breakdown voltage

results discussed in 6.2.1. The origin of the higher capacitance is not clear at the present time, but it leads to slightly reduced field-effect mobilities, as determined by applying MOSFET equations.

In summary, the additional heating step of 100ºC provides slight benefit to OTFTs with short UV/ozone exposure time, while the threshold voltage of both transistor sets exhibits similar behaviour for UV/ozone exposure times of 20 minutes or longer. The annealing step at 140ºC provides slight benefit to the OTFT off-currents and on/off current ratios. Even though the performed heating steps provided some transistor improvement, the UV/ozone oxidation cannot be shortened and replaced with a heating step to gain the same transistor performance.

7 EFFECT OF *W* AND *L* ON OTFT PERFORMANCE

7.1 INTRODUCTION

This section provides results of a study of the effect of transistor dimensions, namely the channel length *L* and channel width *W*, on the OTFT performance. We have fabricated three sets of transistors with different channel widths 200, 500 and 1000 μm. The transistor dimensions are listed in Table 7. The preparation of aluminium oxide was the same in all transistor samples, encompassing 60-minute UV/ozone exposure and no annealing. Complete fabrication process is explained in Chapter 3.

Section 7.2 presents the results obtained from electrical characterization of all fabricated OTFTs. Results include the transfer characteristic of a typical OTFT including the hysteresis, followed by a summary of various transistor parameters. Results have been analysed in several ways to unlock the effect of *W* and *L* on the transistor performance. This includes a few normalization procedures with respect to channel width *W*, channel length *L* and their ratio *W/L*. Consequently, OTFT

parameters like the on- and off-currents and the field-effect mobility were found to depend on the ratio of channel width and channel length. Finally, Section 7.3 summarizes the findings.

7.2 OTFT RESULTS

Figure 7.1 presents the typical transfer characteristics of an OTFT with W = 520 µm and L = 27 µm. This OTFT had the following performance: charge carrier mobility $\mu_p \approx 0.06$ cm^2/Vs, the threshold voltage $V_t \approx -1.4$ V, sub-threshold slope $S \approx 130$ mV/decade, on-off current ratio $\approx 1.5\times10^5$ and the off-current ≈ 7 pA.

Figure 7.2 shows the hysteresis in the measurement of the transfer characteristics of the OTFT whose transfer characteristics have been shown in Figure 7.1. The hysteresis was obtained by varying the gate-source voltage V_{gs} from 1 V to –3 V and back for drain-source voltage V_{ds} = –3 V.

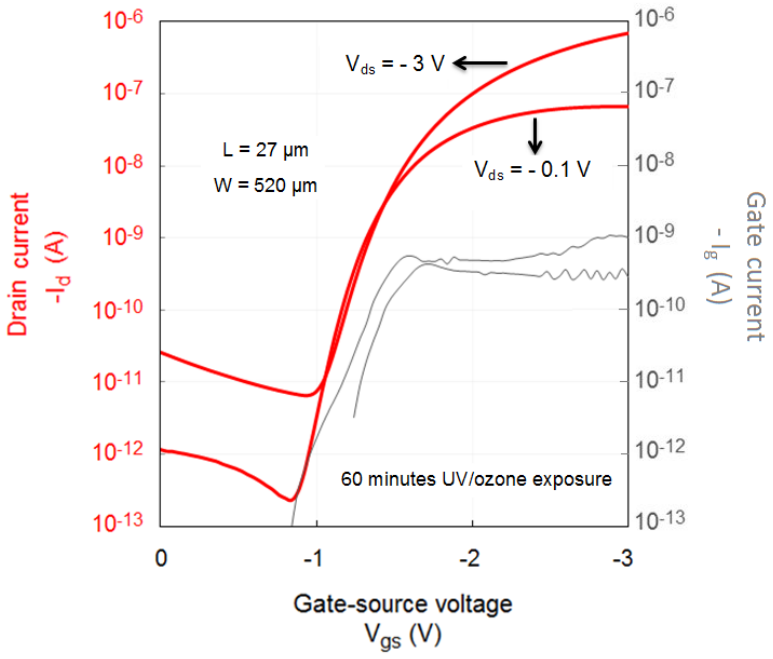

Figure 7.1. OTFT transfer characteristics.

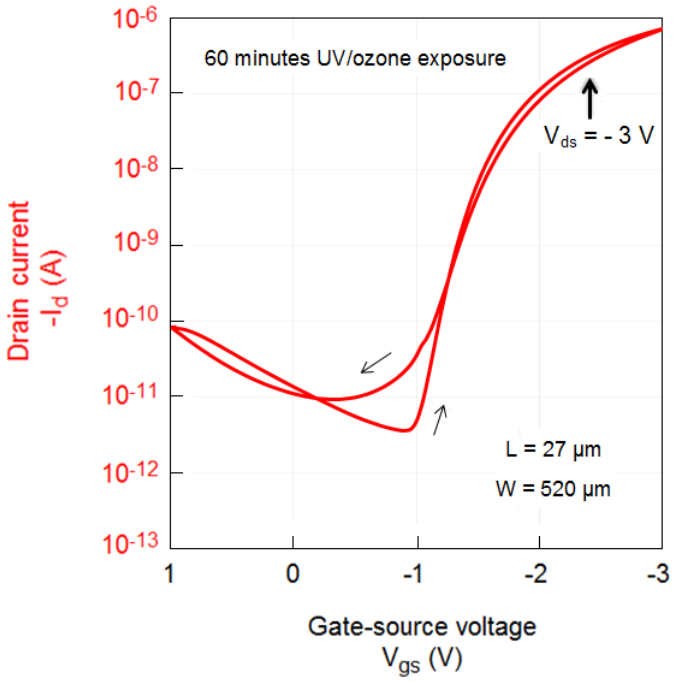

Figure 7.2. OTFT hysteresis.

The hysteresis is small and the drain current followed almost the same path when V_{gs} was swept from 1 V to –3 V and back. In the transistor on-state the depletion-accumulation sweeping direction leads to a slightly higher current when compared to the accumulation-depletion direction. This behaviour is reversed in the subthreshold region and near the off-state. This is a result of charge trapping near the semiconductor-dielectric interface.

Figure 7.3 shows the field-effect mobilities of the OTFTs fabricated with different channel widths and channel lengths. One can see from the graph that the mobilities are higher for the OTFTs with W = 200 µm and they decrease as the channel widths of the OTFTs increase. In addition, for the given channel width the mobility increases as the channel length increases. As mentioned previously, this dependence of mobility on L indicates relatively high source-drain contact resistance. The variation in the mobilities is smallest for OTFTs with W = 1000 µm and largest

for those with W = 200 µm. It is not immediately obvious why that should be the case and, therefore, this data will be discussed again later in this section.

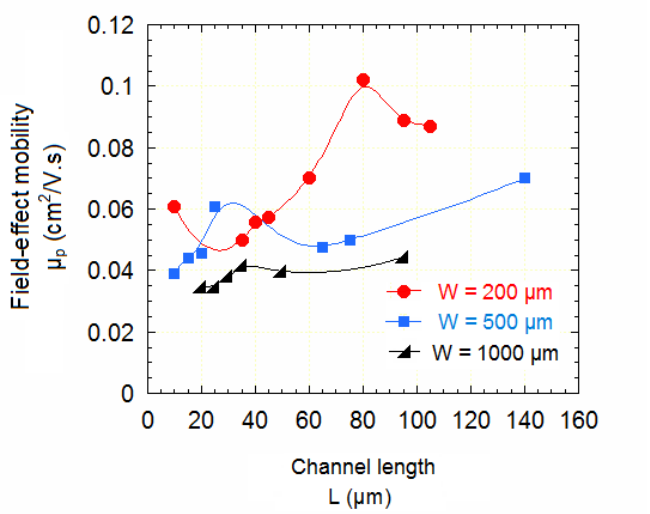

Figure 7.3. OTFT field-effect mobility versus OTFT channel length.

Figure 7.4 depicts the threshold voltages of the OTFTs. The threshold voltages are not affected by transistor dimensions. This is not surprising since the threshold voltage should be primarily controlled by the vertical electric field across the gate dielectric. Minor variations are seen for OTFTs with W = 200 and 500µm, while OTFTs with channel width of 1000 µm exhibit threshold voltage independent of the channel length. This likely reflects the small variations between the OTFTs.

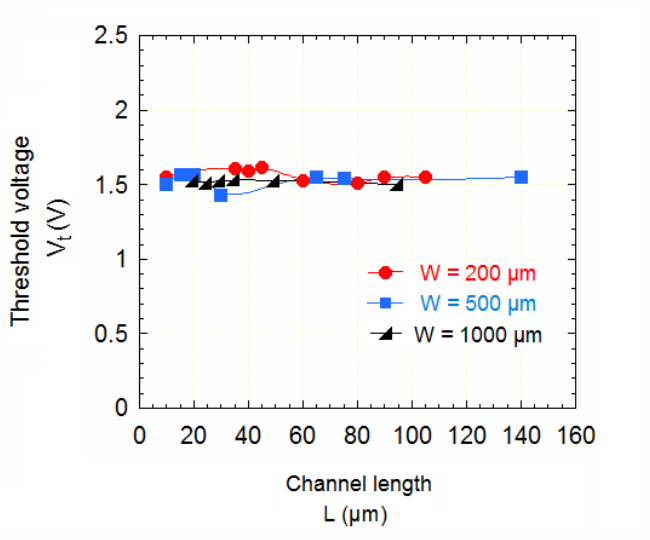

Figure 7.4. OTFT threshold voltage versus OTFT channel length.

Figure 7.5 presents the OTFT subthreshold slopes. OTFTs with W = 1000 µm exhibit lower subthreshold slopes for different OTFT channel lengths, while OTFTs with W of 200 or 500 µm exhibit higher values with a larger scatter. Figure 7.5 suggests that the OTFT dimensions, especially the channel width W, may affect the subthreshold slope values. The larger is the channel width the lower the subthreshold slope; with the latter being desirable.

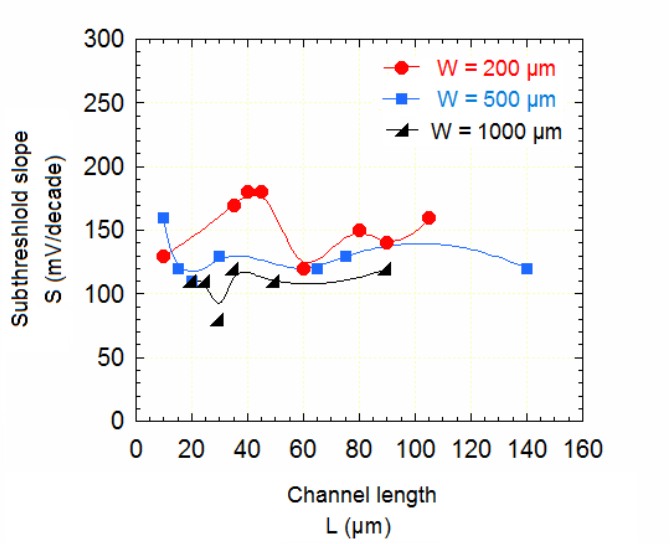

Figure 7.5. OTFT sub threshold slope versus OTFT channel length.

Figure 7.6 shows the OTFT on- and off-currents as functions of channel width and channel length. As expected, the on-currents are the highest for OTFTs with channel width W = 1000 µm and smallest for W = 200 µm.

For any given channel width the OTFT on-currents decrease as the channel length increases. This is because as the distance between the source and the drain terminals increases the channel resistance increases. The off-currents of the OTFTs seem lower for W = 1000 µm when compared to OTFTs with smaller channel widths. At the same time the off-currents do not change much with increasing channel length.

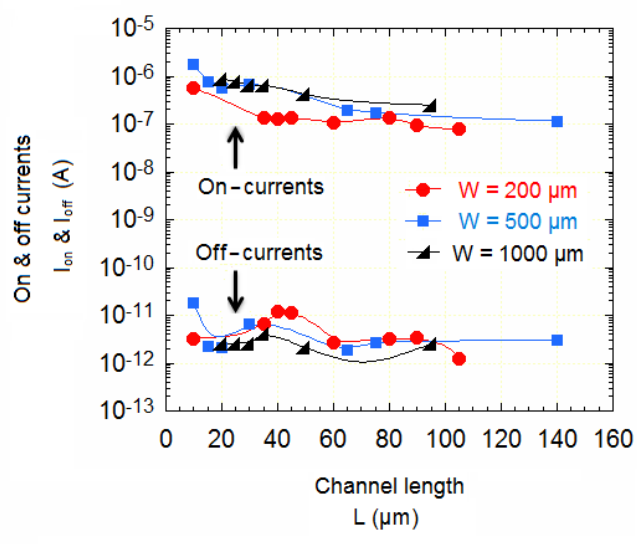

Figure 7.6. OTFT on and off-currents versus the channel length.

Since *W* and *L* influence the on/off-currents of the transistor, all currents were normalized by multiplying them with a factor of *L/W*. Figure 7.7 shows these normalized on/off-currents as function of channel length. This normalization procedure brought all on-current values closer together and, as expected, made them independent of *L*. This behaviour, however, is not observed for the OTFT off-currents. One can clearly see that the channel width affects the off-currents, with *W* = 1000 µm leading to the lowest values and *W* = 200 µm leading to the highest.

Figure 7.8 represents the normalized on- and off-currents (shown in Figure 7.8) replotted against the ratio of channel width to channel length, *W/L*. In this case all on-currents (as well as off-currents) are superimposed on top of each other and they both decrease with increasing *W/L*. As the *W/L* increases from ≈ 1.5 to ≈ 50, the normalized on-current decreases from ≈ 5×10^{-8} A to ≈ 2×10^{-8} A and the normalized off-current decreases from ≈ 1×10^{-12} A to ≈ 5×10^{-14} A.

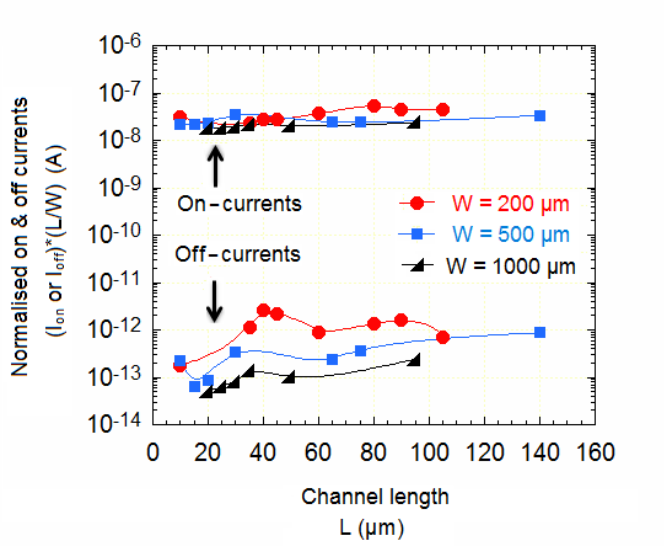

Figure 7.7. Normalized on- and off-currents versus OTFT channel length.

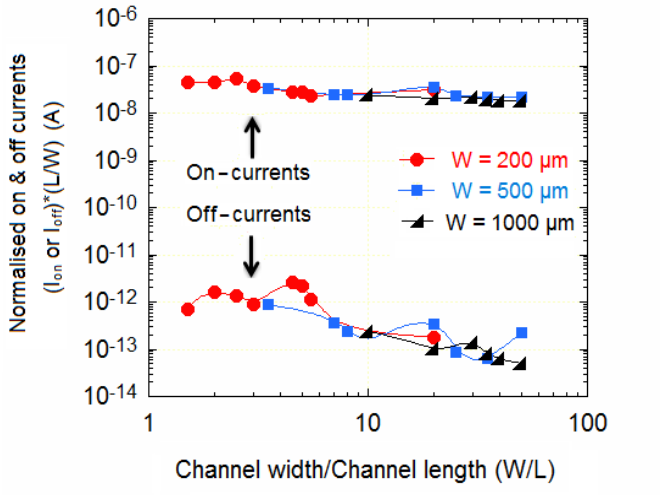

Figure 7.8. Normalized on- and off-currents versus the ratio of channel width to channel length.

Figure 7.9 shows the field-effect mobilities of the OTFTs for different *W/L* ratios. In this case the data plotted in figure 7.3 is replotted as a function of *W/L*. While the mobility data presented in figure 7.3 showed no clear dependence on the channel length, its dependence on *W/L* becomes quite clear. As the *W/L* increases from ≈ 1.5 to ≈ 50, the field-effect mobility decreases from ≈ 0.1 to ≈ 0.04 cm^2/Vs. When the *W/L* reaches 10, the change in mobility with increasing *W/L* becomes negligible. One can see that if the transistor dimensions are not carefully selected,

the value of the field-effect mobility can be grossly overestimated. In this particular case, the mobility calculated for small *W/L* is overestimated by a factor of 3.

The mobility calculation assumes that the charge accumulation occurs within the transistor area of *W*×*L*. In reality, the charge accumulation occurs wherever the organic semiconductor resides above the gate electrode. Consequently, the charge outside of *W*×*L* area will contribute to the drain current and inflate the calculated mobility. If the extension of the organic semiconductor beyond *W*×*L* region could be prevented, this mobility overestimate would be eliminated.

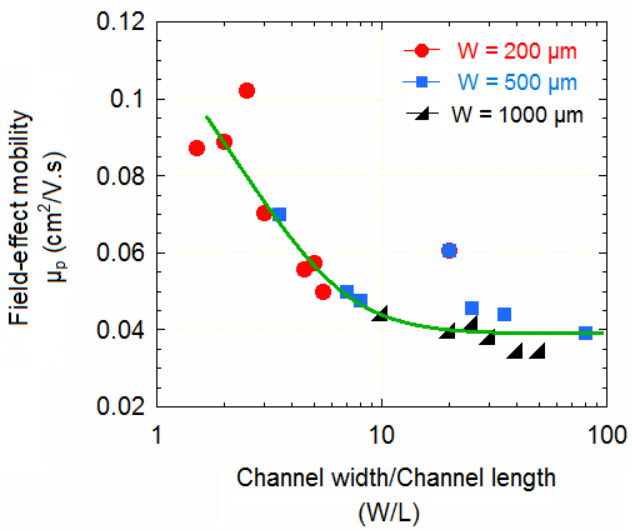

Figure 7.9. OTFT field-effect mobility versus ratio of OTFT channel widths and channel lengths.

In summary, the normalized on- and off-currents and the mobility show good correlation with *W/L*. Since the pentacene island is substantially wider than the channel width, the vertical electric field of the gate electrode affects the dielectric/semiconductor interface wherever the semiconductor resides above the gate electrode. Consequently, larger drain current is measured for transistors with smaller *W/L* due to a larger relative contribution from parasitic currents. The data also shows that *W/L* of our transistor design should be at least 10 to eliminate the

overestimate in the calculated field-effect mobility. However, if the size of the transistor island (semiconductor area) is reduced down to *W*, this value would gradually decrease.

7.3 DISCUSSION

One can find very few past research articles that discuss the effect of channel dimensions on the transistor performance [234-240]. Kwon studied the effect of channel width on TIPS-pentacene OTFTs. In that case the threshold voltage and drain current increased and the field-effect mobility decreased with increasing channel width. In addition, the field-effect mobility was dependent on the threshold voltage [240]. These results were in agreement with those obtained for TFTs with nanowire channels [237] and a bilayer amorphous/nanocrystalline silicon [239]. The results presented in this Chapter show lower field-effect mobility for OTFTs with larger channel width, while the threshold voltage is not affected. As expected, the on-currents are also higher for OTFTs with larger channel width. These results are in agreement with experimental observations reported previously. The only difference is in the behaviour of the threshold voltage that could be ascribed to different materials and transistor operating voltages.

Similar changes in the field-effect mobility when plotted against *W*/*L* were observed by Hatzopoulos [239] and Zan et al [236]. Based on their observations the mobility decreased with increasing *W*/*L* and levelled off when the ratio was greater than 10.

An increase in the subthreshold slope was observed with increasing channel width [235, 236]. The OTFTs presented here exhibit the opposite. When comparing the subthreshold slope of OTFTs with similar *L* and increasing *W*, lower slopes were obtained for larger *W*. However, the subthreshold slope strongly depends on the particular semiconductor/dielectric interface and therefore, it is difficult to compare different material systems.

OTFT off-current decreased with increasing channel width (see Figures 7.6 and 7.7). This is attributed to parasitic currents that increase with decreasing W/L (see Figure 7.8).

Finally, OTFT performance obtained in this chapter for transistors with $W/L \geq 10$ is comparable to low-voltage OTFTs with organic/inorganic bilayer dielectric implementing short alkyl phosphonic acid monolayers (C6 – C10) and similar *W/L* reported by Fukuda [206] and Acton [131] (see Table 9).

7.4 CONCLUSION

Several batches of OTFTs with varied channel width and channel length were fabricated to study the effect of OTFT dimensions on transistor performance. The data presented in Section 7.2 demonstrate that the OTFTs have negligible hysteresis in their transfer characteristics. Reliable transistor performance has been observed for the OTFTs with larger channel widths of $W = 1000$ µm. The field-effect mobilities are overestimated for OTFTs with *W/L* ratio less than 10. Similarly, the transistor on- and off-currents exhibit correlation with *W/L*. Threshold voltages and sub-threshold slopes are not significantly affected by varying channel width and channel

length. Therefore, to obtain more accurate values for various transistor parameters, transistors with $W/L > 10$ should be used.

8 BIAS-STRESS-INDUCED OTFT INSTABILITY

8.1 INTRODUCTION

This section discusses results of the bias-induced instability in the low-voltage OTFTs fabricated and presented in the previous sections. Ideally, the OTFT performance should not deteriorate when the device is turned ON/OFF many times or when it is kept under electrical bias for prolonged time. OTFT stability is the fundamental constraint that determines transistor suitability in various circuit applications. Device stability is typically investigated by subjecting the OTFT to an electrical bias for a long period of time and recording the changes in the device performance during that time. A circuit designer is more concerned with the changes in the OTFT on-current due to bias stress, while the device engineer or physicist aims to understand the physical mechanism that controls the observed deterioration in the OTFT performance when subjected to electrical bias. This section presents the bias stress data of the OTFT from both points of view.

Bias-induced degradation is not unique to OTFTs. In fact, other thin-film transistor technologies developed for flexible device applications, e.g. hydrogenated amorphous silicon, exhibit similar deterioration. OTFTs present a unique challenge

in this case due to many available OTFT materials, device geometries and fabrication procedures (wet or dry).

In low-voltage OTFTs the typical gate operating voltages lead to a large electric field applied across the gate dielectric. The dielectric strength and the homogeneity of the gate dielectric play an important role during the bias stress experiment. Few groups reported the effect of the gate bias stress on the low-voltage OTFTs but in all the cases the gate voltage was kept below 3 V. In addition, both the gate and drain electrodes were biased, leading to a lesser transistor degradation. This section presents the bias-stress data for OTFTs with high gate voltage (3 V $\leq |V_{gs}| \leq$ 5 V) and source/drain electrodes grounded. The first part studies the transistor bias-induced instability as a function of the gate bias, while the second part investigates how the UV/ozone exposure time during the AlO_X preparation affects the gate-bias induced transistor instability.

8.2 OTFT INSTABILITY: EFFECT OF THE GATE BIAS

This experiment has been performed on freshly fabricated devices with the same device geometries (W = 1000 μm and L = 30 μm) and device fabrication conditions. These devices are similar to those reported in Section 7.2. The details of the bias stress experiment are given in Section 3.4.4.

Figure 8.1 shows the transfer characteristics of the OTFT after 10, 100 and 1000 seconds of a bias stress at V_{gs} = –3 and –5 V. The transfer characteristics shift in the direction of the applied voltage, leading to more negative threshold voltage. When V_{gs} = –3 V, the slope in the subthreshold regime remains unchanged for stress

times up to 100 seconds and a small increase is noticeable after 1000 seconds. The on-current decreases with the increasing bias stress time, while the off-current does not change much between 10 and 1000 seconds. When V_{gs} = –5 V, a much larger shift of the transfer characteristic in the direction of the applied voltage occurs, indicating a larger shift of the threshold voltage. The slope in the subthreshold region increases early on and continues to rise with increasing bias stress time. The on-current decreases and the off-current increases with the increasing stress time. This proceeds at a faster rate when high electric field between the source/drain and gate electrodes is applied.

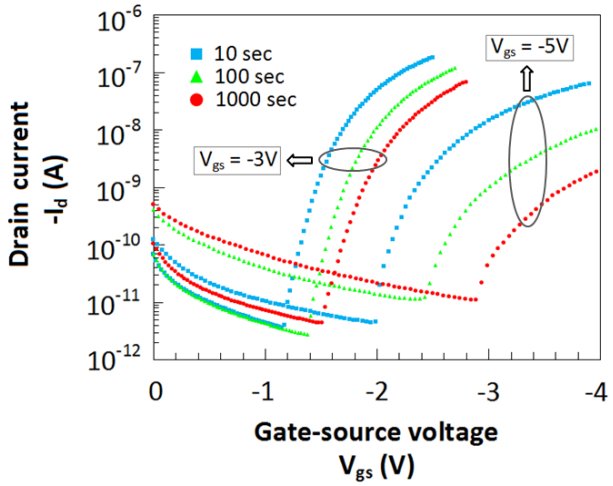

Figure 8.1 OTFT transfer characteristic as a function of bias stress time for gate stress voltages of –3 and –5 V. The source and drain electrodes were grounded.

Figure 8.2 represents the changes in the threshold voltage of 5 similar OTFTs when subjected to 5 different gate bias voltages of –3, –3.5, –4, –4.5 and –5 V for up to 5000 seconds. One can see that after 5000 seconds the threshold voltage of the OTFT has risen to –2.06 V for V_{gs} = –3 V, –2.12 V for V_{gs} = –3.5 V, –2.43 V for V_{gs} = –4 V, –2.98 V for V_{gs} = –4.5 V and to –3.36 V for V_{gs} = –5 V. In addition, for V_{gs} = –5 V the threshold voltage reaches saturation at t ~ 1000 seconds.

The solid curves represent the least-square fits of the data points to the stretched-exponential function given by Eq. (8). However, this equation is modified to $|V_t(t)| = |V_t(\infty)| - [\,|V_t(\infty)| - |V_t(0)|\,] \cdot e^{-\left(\frac{t}{\tau_{Vt}}\right)^{\beta_{Vt}}}$ to reflect the changes in $|V_t|$ instead of $|\Delta V_t|$. These transistors were subsequently bias stressed for 5000 seconds by applying positive gate bias voltages of +3, +3.5, +4, +4.5 and +5 V to the corresponding OTFTs. This, however, had only minor effect on the value of the threshold voltage and did not lead to its recovery to the original value.

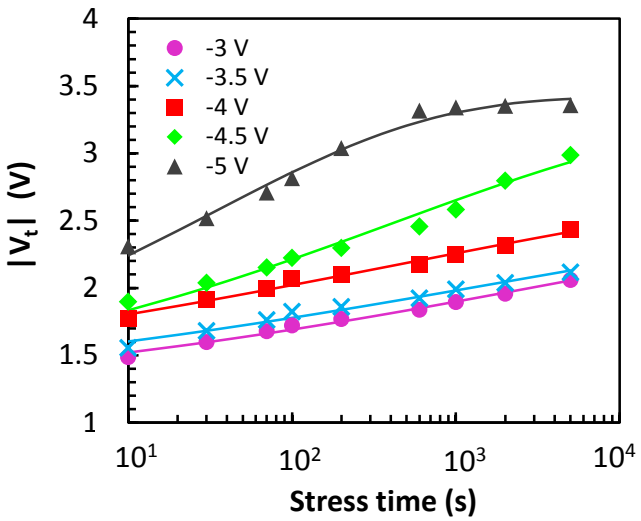

Figure 8.2. OTFT threshold voltage versus stress time for different gate bias voltages.

Figure 8.3 represents the normalised OTFT field-effect mobility as a function of the bias stress time for 5 different gate bias voltages. The mobilities were normalized with respect to the field-effect mobilities before the bias stress. The mobility decreases with increasing stress time for all gate biases. For very high source-gate electric field the effect saturates, as can be seen for V_{gs} = –5 V and t ~ 1000 seconds. The mobility reduces by almost 2 orders of magnitude when the gate-source electric field of approximately 4 MV/cm is applied. Similar to the threshold voltage, the drop in the normalized field-effect mobility as a function of time can be

described by a stretched-exponential function $\frac{\mu(t)}{\mu(0)} = \frac{\mu(\infty)}{\mu(0)} + \left[1 - \frac{\mu(\infty)}{\mu(0)}\right] . e^{-(t/\tau_\mu)^{\beta_\mu}}$.

The solid lines in Figure 8.3 show such least-square fits. Finally, the OTFT mobility did not recover on applying the positive gate bias for 5000 seconds.

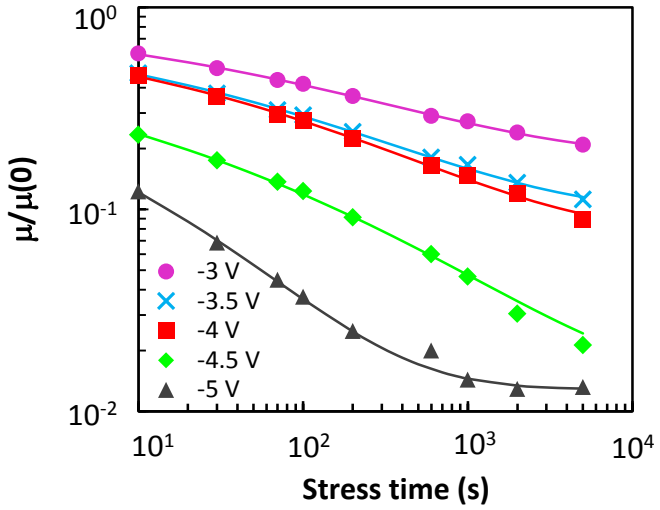

Figure 8.3. Normalised field-effect mobility versus bias stress time for 5 different gate bias voltages. Source and drain contacts were grounded.

Figure 8.4 represents the change in the subthreshold slope with increasing bias stress time for different gate bias voltages. The initial subthreshold slope was ~100 mV/decade. One can observe that after 5000 seconds of bias stress the subthreshold slope increased by 63 mV/decade for V_{gs} = –3 V, 104 mV/decade for V_{gs} = –3.5V, 223 mV/decade for V_{gs} = –4 V, 280 mV/decade for V_{gs} = –4.5 V and 303 mV/decade for V_{gs} = –5 V. The change in the subthreshold slope is relatively small for V_{gs} = –3 V and –3.5 V and becomes much larger for $|V_{gs}| \geq 4$ V. There is an indication that the subthreshold slope starts to saturate for V_{gs} = –5 V and t > 2000 seconds. The solid curves represent the least-square fits of the data to the stretched-exponential function $\Delta S(t) = S(t) - S(0) = (S(\infty) - S(0))\left[1 - e^{-(t/\tau_S)^{\beta_S}}\right]$. Finally,

the subthreshold slopes were not recovered upon biasing the OTFTs with respective positive gate voltages for 5000 seconds.

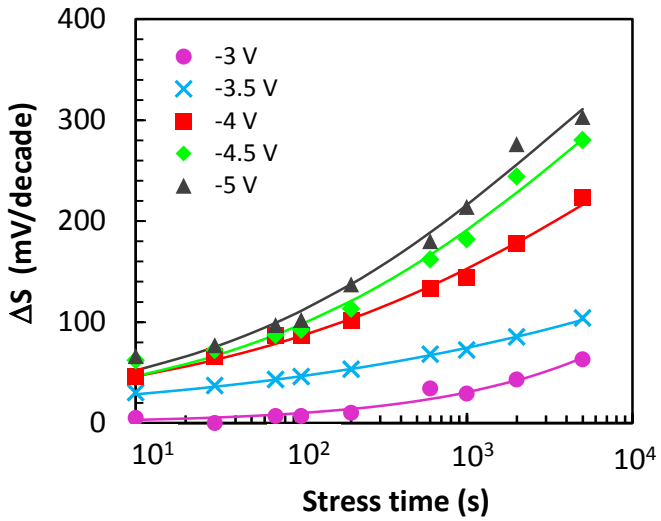

Figure 8.4. OTFT subthreshold slope versus bias stress time for 5 different gate bias voltages. Source and drain contacts were grounded.

Figure 8.5 represents the normalised OTFT on-current measured as a function of bias stress time for different gate bias voltages. The on-current is defined as the drain-source current at V_{gs} = –3 V and V_{ds} = –3 V. On-currents have been normalised with respect to the initial on-current of the unstressed OTFTs. The on-currents are decreasing by an order of magnitude when the OTFT is bias stressed at –3 V for 5000 seconds, more than an order of magnitude when bias stressed at –3.5 V, two orders of magnitude at –4 V and ~ 4 orders of magnitude at –4.5 and –5 V. The solid curves represent the least-square fits of the data to the stretched-exponential function $\frac{I_{ON}(t)}{I_{ON}(0)} = \frac{I_{ON}(\infty)}{I_{ON}(0)} + \left[1 - \frac{I_{ON}(\infty)}{I_{ON}(0)}\right].e^{-(t/\tau_{ION})^{\beta_{ION}}}$.

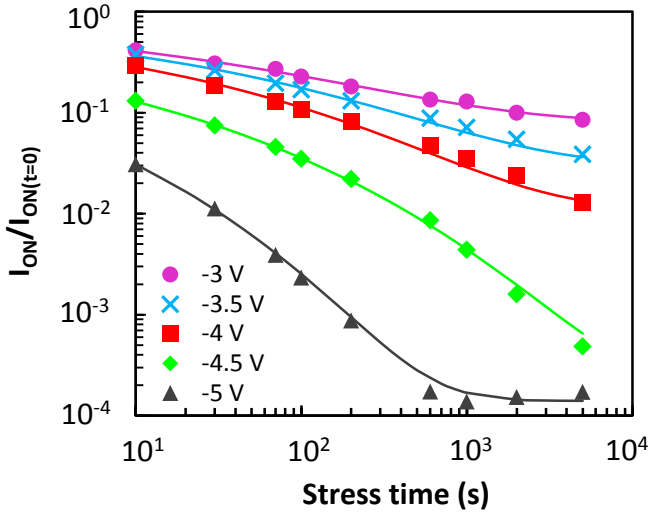

Figure 8.5. OTFT normalised on-current versus stress time at different gate bias voltages. I_{on} is recorded for V_{gs} = V_{ds} = –3 V.

Table 11 lists the stretching parameters and time constants obtained from Figures 8.2-8.5. The stretching parameters for the threshold voltage are about 0.17 and they are increasing for $|V_t| > 4$ V. The stretching parameters for the mobility are about 0.24 with the exception of a slightly lower value for $V_t = -4.5$ V. The stretching parameters for the subthreshold slope generally increase with the gate bias voltage. However, β_S for $V_t = -3$ V does not follow this rule and reaches the highest value of 0.50. Finally, the stretching parameters for the on-current are about 0.24 with the exception of a slightly lower value for $V_t = -4.5$ V. All time constants are decreasing with increasing bias stress voltage, confirming that the degradation of all transistor parameters proceeds at a faster rate.

Table 11. Time constants and stretching parameters obtained from Figures 8.2-8.5.

Gate Bias (V)	β_{Vth}	τ_{Vth} (s)	β_μ	τ_μ (s)	β_S	τ_S (s)	β_{ION}	τ_{ION} (s)
-3	0.18	3.4×10^{3}	0.25	3.9×10^{1}	0.50	1.7×10^{5}	0.24	8.8×10^{1}
-3.5	0.17	1.8×10^{3}	0.24	1.6×10^{1}	0.22	1.4×10^{6}	0.25	7.7×10^{1}
-4	0.16	4.8×10^{2}	0.24	1.6×10^{1}	0.30	1.3×10^{4}	0.25	3.6×10^{1}
-4.5	0.24	4.3×10^{2}	0.18	1.1×10^{0}	0.35	5.6×10^{3}	0.21	3.5×10^{-1}
-5	0.32	3.4×10^{1}	0.23	3.3×10^{-1}	0.36	3.3×10^{3}	0.24	5.4×10^{-2}

8.3 OTFT INSTABILITY: EFFECT OF UV/OZONE EXPOSURE

This section investigates how the UV/ozone exposure time during the AlO_X preparation affects the gate-bias induced OTFT instability. These OTFTs correspond to the 'set A' of Chapter 5. Six identical OTFTs with W = 1000 µm and L = 30 µm were investigated. The only difference between the transistors was the length of the UV/ozone exposure during AlO_x preparation that was 2, 5, 10, 20, 40 and 60 minutes. These transistors were stored in low vacuum at a pressure of ~ 5×10^{-1} mbar for six months after the fabrication before the bias stress was performed. All transistors were bias-stressed at V_{gs} = –4 V for 10, 30, 70, 100, 200, 600, 1000, 2000 and 5000 seconds while keeping the source and drain electrodes grounded. Other details of the bias stress experiment are given in Section 3.4.4.

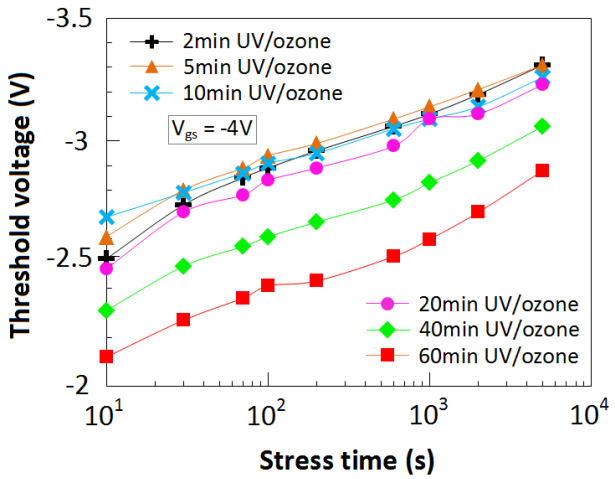

Figure 8.6. OTFT threshold voltage versus bias stress time for six different UV/ozone exposures. UV/ozone was used to convert Al into AlO_X and create the inorganic part of the bi-layer gate dielectric.

Figure 8.6 presents the changes in the threshold voltage of the transistors when V_{gs} = –4 V source-to-gate bias is applied to six OTFTs whose AlO_X layers

were prepared by implementing different UV/ozone exposure times. After 5000 seconds of bias stress the threshold voltage rises to –3.31, –3.31 , –3.26, –3.23, –3.06 and –2.88 V for transistors implementing a 2-, 5-, 10-, 20-, 40- and 60-minute UV/ozone exposure, respectively. A large shift in the threshold voltage is observed at t = 10 seconds for short UV/ozone exposure times. After this initial rise, further increase in the threshold voltage is similar, irrespective of the UV/ozone exposure time. Overall, the OTFTs using shorter UV/ozone exposure time exhibit larger shift in the threshold voltages after 5000 seconds, indicating an inferior AlO_X quality. As the UV/ozone exposure time increases, the overall shift in the threshold voltage decreases. During the subsequent application of the positive gate bias voltage for t = 5000 seconds a minor change in the threshold voltages was observed, but a complete recovery did not occur.

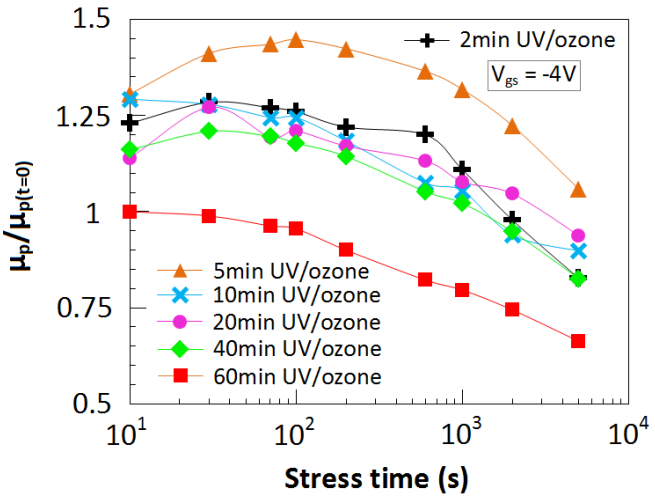

Figure 8.7. Normalised field-effect mobility versus bias stress time for OTFTs with different UV/ozone exposure times.

Figure 8.7 presents the normalised OTFT field-effect mobility as a function of the bias stress time for OTFTs shown in Figure 8.6. The mobilities were normalised with respect to the field-effect mobilities before the bias stress. With the

exception of the 60-minute UV/ozone exposure, the mobility increases in the beginning of the bias stress sequence and decreases afterwards. This abnormal behaviour that does not follow a stretched-exponential behaviour is not observed for OTFTs where AlO_X was prepared by 60-minute UV/ozone exposure. In such a case the decrease in the mobility follows a similar dependence on the stress time as observed in Section 8.2. However, the absolute decrease in the relative mobility is smaller than that observed in Section 8.2. This is most likely caused by the fact that the OTFTs underwent environmental mobility degradation during the 6-month storage time. The OTFT field-effect mobilities did not recover upon application of the positive gate bias voltage for t = 5000 seconds.

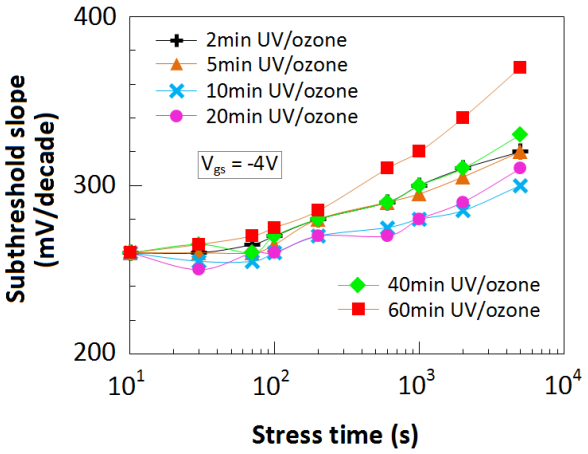

Figure 8.8. Subthreshold slope versus the bias stress time for OTFTs shown in Figures 8.7 and 8.8.

Figure 8.8 shows the change in the subthreshold slope with increasing bias stress time for OTFTs shown in Figures 8.6 and 8.7. When V_{gs} = –4 V is applied for t = 10 seconds, a jump in the subthreshold slope is observed. After 5000 seconds of the bias stress, the subthreshold slopes rises to 320, 310, 300, 310, 330 and 370 mV/decade for OTFTs with AlO_X prepared by a 2-, 5-, 10-, 20-, 40-, and 60-minute UV/ozone exposure. Even though the subthreshold slope increases for all UV/ozone

exposure times, this behaviour is somewhat different from that observed in Section 8.2. This difference might be ascribed to the environmental degradation of the transistors prior to the bias stress experiment. Finally, the subthreshold slopes did not recover to their original values when positive gate bias stress was applied for t = 5000 seconds.

8.4 DISCUSSION

When negative gate bias is applied to OTFT, charge carriers are accumulated in the semiconductor near the semiconductor/dielectric interface. These charge carriers can be injected into the existing traps in the gate dielectric, or new charge carrier traps could be formed in the dielectric or near the dielectric/semiconductor interface. These would manifest themselves as changes in the threshold voltage and possibly field-effect mobility and subthreshold slope. When a positive charge is injected into the gate dielectric, which is likely at high source-gate electric field, the injected charge effectively screens the electric field induced by the gate electrode and the threshold voltage shifts to a more negative value. One would expect this charge injection to occur for high V_{gs} and diminish as the threshold voltage approaches the gate bias voltage, as seen for V_{gs} = −5 V in figure 8.2. In the beginning of any bias stress experiment the accumulated charge density in the channel is at its maximum and, consequently, the injection of the charge into the gate dielectric has the highest probability.

Bias stress degradation of similar OTFTs has been studied by Gupta et al. [231] by varying the post-deposition annealing of 1-octylphosphonic acid layer. As

the bias stress time increased from 10 to 5000 s, the threshold voltage increased by ~ −0.3 V for shorter and ~ −0.6 V for longer 8PA anneal times [231]. The lowest curve in Figure 8.2 corresponding to V_{gs} = −3 V could be compared to the shorter annealing times presented in [231], although the growth conditions of the 8PA and pentacene layers were not identical. Figure 8.2 shows that V_t increased by ~ −0.5 V between the stress time of 10 and 5000 s for V_{gs} = −3 V. This value falls into the range of values observed in [231]. The time constant and stretching parameter extracted for V_{gs} = −3 V in this chapter are comparable to [231]. The time constant decreased from 3.3×10^6 to 7.5×10^2 s and the stretching parameter increased from 0.15 to 0.28 with increasing annealing time [231] while τ_{Vt} = 3.4×10^3 s and β_{Vt} = 0.18 for V_{gs} = −3 V in this Chapter.

Bias stress effect of low-voltage OTFTs with similar material/transistor architecture and different drain bias voltages has been reported by Zschieschang et al [209]. It was observed that the threshold voltage shifted by ~ −0.9 V after 5000 s of bias stress. The degradation was also studied as a function of drain-source bias voltage up to −2 V and the degradation proceeded faster for lower drain-source voltages. The time constant decreased from 1.76×10^7 to 4.82×10^3 and the stretching parameter increased from 0.3 to 0.4 with the increasing drain voltage [209]. For pentacene OTFTs Gu et al. [241] extracted stretching parameters in the range from 0.40 to 0.42 while Han et al. [242] obtained a value of 0.28. High threshold voltage shift was observed for OTFTs with short-chain phosphonic acid [206] which is comparable to the shift in the threshold voltage presented in this Chapter. Finally, the bias stress conditions presented in this Chapter represent the most severe bias stress applied to such transistors to date.

A decrease in the mobility with increasing bias stress time is more difficult to analyse, since some degradation is due to the presence of oxygen and moisture in the ambient environment. Whatever the origin of the mobility degradation might be, the mobility degradation increases with increasing gate bias and time. The mobility degradation stops eventually, as seen in Figure 8.3 for the highest gate bias stress. The field-effect mobility decreased by more than an order of magnitude for higher gate bias voltages and the degradation was lower for smaller voltages. The mobility degradation for $V_{gs} = -3$ V is about 50% faster than that reported in [231] for similar OTFT structures. This may result from different 8PA and pentacene growth between these two experiments. The mobility stretching parameters are in the range of 0.18 to 0.25, while they are ranging from 0.61 to 0.65 in reference [231]. However, in both cases the stretching parameters are not affected by the varied transistor/bias properties, suggesting that the controlling factor may be the environmental degradation.

The change in the subthreshold slope means changing dielectric/semiconductor interface. Additional charge carrier traps are created at or near the dielectric/semiconductor interface due to the bias stress. For example, hole traps may appear above the HOMO level of pentacene. Subthreshold slope degrades faster at higher gate bias (see Fig. 8.4). Higher gate bias results in higher density of accumulated charge in the channel and, consequently, generation of a larger number of traps at the interface. The subthreshold slope increased by ~ 50 meV for $V_{gs} = -3$ V and stress time of 5000 s, while it increased by ~110 meV for comparable OTFTs in [231]. The stretching parameter (see Table 11) varies from 0.22 to 0.50, while it increased from 0.35 to 0.72 upon extending the 8PA anneal [231]. The

subthreshold slope time constant decreased with increasing gate bias voltage (Table 11) and increased with increasing annealing time [231].

The decay in the OTFT on-current as a function of the bias time is a combined effect of the threshold voltage shift, mobility drop and an increase in the subthreshold slope. The on-currents can also decay if the band gap of the semiconductor changes due to its oxidation or when the source/drain contact resistance increases, especially for OTFTs with short channel length. The on-current stretching parameter varies between 0.21 and 0.25 and is not much affected by the applied gate bias. A value of 0.29 was obtained for comparable OTFT in [231]. The time constant increased with increasing V_{gs}. A value smaller than 100 s was obtained for $V_{gs} = -3$ V while a value of ~ 300 is reported in [231] for comparable OTFTs.

8.5 CONCLUSION

Prolonged gate bias stress was applied to OTFTs and a change in the transistor parameters was studied as a function of the gate bias stress voltage. The gate bias voltages were chosen to create large gate-source electric field that far exceeds the normal transistor operating conditions. Degradation in the threshold voltage, field-effect mobility and the subthreshold slope was observed with increasing gate bias. The threshold voltage and the subthreshold slope increased with the increasing stress time and gate bias. The field-effect mobility decreased. The change in the OTFT parameters followed a stretched-exponential dependence. The degradation of the OTFT performance reaches saturation for the gate bias stress of −5 V and stress time higher than 200 seconds. The transistor degradation occurs as

a result of the charge injection into the existing traps in the gate dielectric and the formation of new charge carrier traps in the dielectric or near the dielectric/semiconductor interface.

The second experiment studied the effect of the UV/ozone exposure time during the AlO_X preparation on the bias-induced transistor instability. Since these transistors underwent some environmental degradation before the bias stress experiment, the change in their threshold voltage, field-effect mobility and subtheshold slope followed slightly different time behaviour when compared to the as-fabricated OTFTs. Nevertheless, degradation in all OTFT parameters was observed, confirming that the short UV/ozone exposure time leads to aluminium oxide of inferior quality. This manifested itself as a large increase in the threshold voltage in the early stage of the degradation process and unusual degradation kinetics of the field-effect mobility.

9 SUMMARY AND FUTURE WORK

9.1 SUMMARY

A completely dry fabrication process has been proposed for low-voltage OTFTs. An ultra-thin, inorganic/organic dielectric bilayer consisting of aluminium oxide prepared by UV/ozone oxidation and a vacuum-deposited 1-octylphosphonic acid was implemented in OTFTs based on pentacene. Although this is the first demonstration of a vacuum-grown alkyl phosphonic acid used in OTFTs, this thesis focused on the preparation of the aluminium oxide using UV/ozone oxidation.

The preparation of the aluminium oxide was optimized with respect to the OTFT performance. The experimental results show that the quality of the AlO_X layer primarily affects the transistor threshold voltage. Longer UV/ozone exposure times yield lower threshold voltage, confirming that the exposure of at least 60 minutes is required for the proper oxidation. On the other hand, thicker aluminium oxide prepared by sequential evaporation and UV/ozone exposure of thin aluminium layers exhibited only minor effect on the transistor threshold voltage. An elevated temperature applied after or during the UV/ozone oxidation process aids in the initial

stage of the AlO_X formation, leading to the leakage current density suppression. Similar effect is not observed when post-annealing step is applied to AlO_X prepared by a 60-minute UV/ozone exposure. Instead, a slight improvement in the transistor off-current, on/off current ratio and the dielectric breakdown voltage is seen.

OTFT geometry (*W* and *L*) has minor effect on the transistor performance, but to obtain accurate field-effect mobility, the *W/L* ratio should be greater than 10. The results show that a 3-fold overestimate in the field-effect mobility can be obtained when the channel length and channel width become comparable.

Finally, the bias-induced instability of the OTFTs has been investigated by applying gate bias voltages that far exceed the normal transistor operation. These were chosen to accelerate the transistor degradation process. The stretched-exponential degradation in the threshold voltage, subthreshold slope and field-effect mobility was observed. This degradation increased for longer stress time and higher gate bias, as observed in other thin-film transistors. The UV/ozone exposure time used during the AlO_X preparation also affected the transistor instability, confirming that short oxidation times lead to inferior oxide quality.

9.2 FUTURE WORK

Completely dry fabrication process for low-voltage OTFTs has been demonstrated and an optimization of one of the transistor layers, namely the aluminium oxide prepared by UV/ozone exposure, was performed. Although this dry process yields transistors that have comparable parameter values to similar devices obtained by mixture of wet and dry processing, their field-effect mobility

needs to be improved. This can be achieved through additional optimization of the existing transistor, namely the improvement of the interface between the alkyl phosphonic acid and the organic semiconductor. Lower mobility also could be a sign of a larger resistance between the source-drain contacts and pentacene. Therefore, the future transistor optimization process should include the following:

- Optimization of the semiconductor layer growth by varying its thickness, deposition rate and growth temperature.
- Optimization of the growth of 1-octylphosphonic acid that would lead to a compact, well-ordered monolayer.
- Optimization of the source and drain contacts to provide good charge carrier injection into the transistor channel.
- Separation of the bias-induced and environmentally-induced transistor degradation processes with the aim to understand and control them.
- Development of n-channel OTFT by implementing an n-type organic semiconductor.
- Transfer of the transistor fabrication process onto plastic substrate.

Additional experiments might also be performed with respect to the UV/ozone oxidation process. This thesis studied the UV/ozone oxidation in depth, but other methods of ozone generation exist. These can be used instead of or in combination with the existing method. In addition, the use of dry air or pure oxygen would lead to higher concentration of the generated ozone and this may affect the rate of oxide formation as well as its quality. Additional material characterization techniques, such as X-ray reflection, X-ray diffraction, X-ray photoelectron spectroscopy, and atomic force microscopy could be implemented in the future to

provide additional information about the structure and surface roughness of these oxides.

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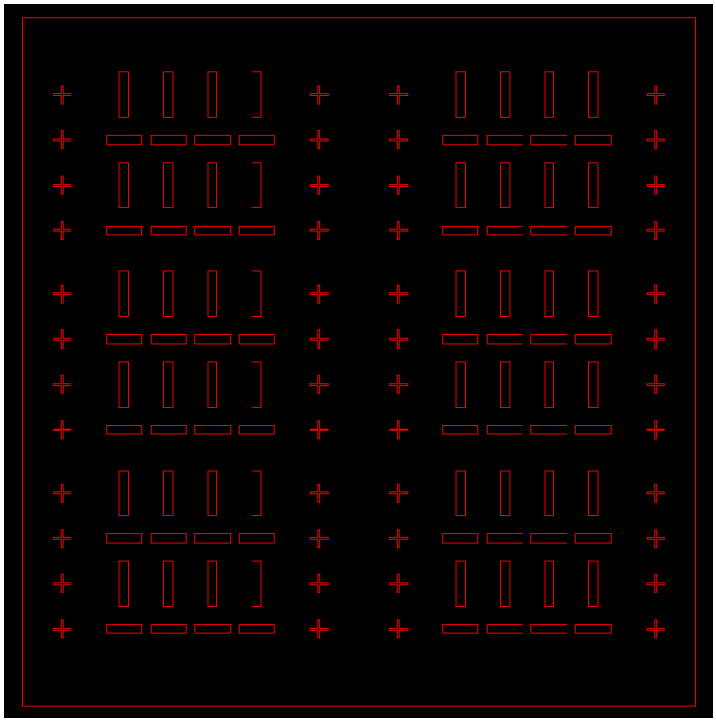
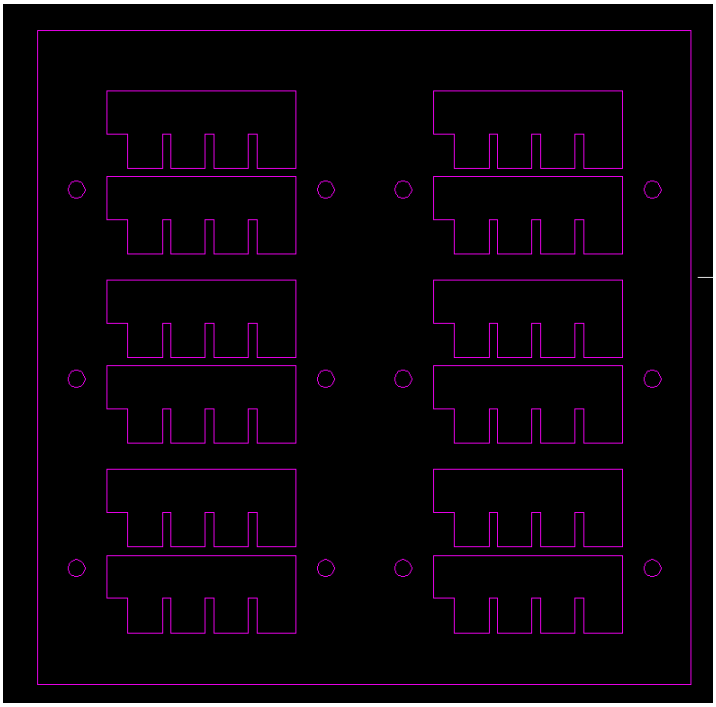
APPENDIX

A1 OTFT MASKS

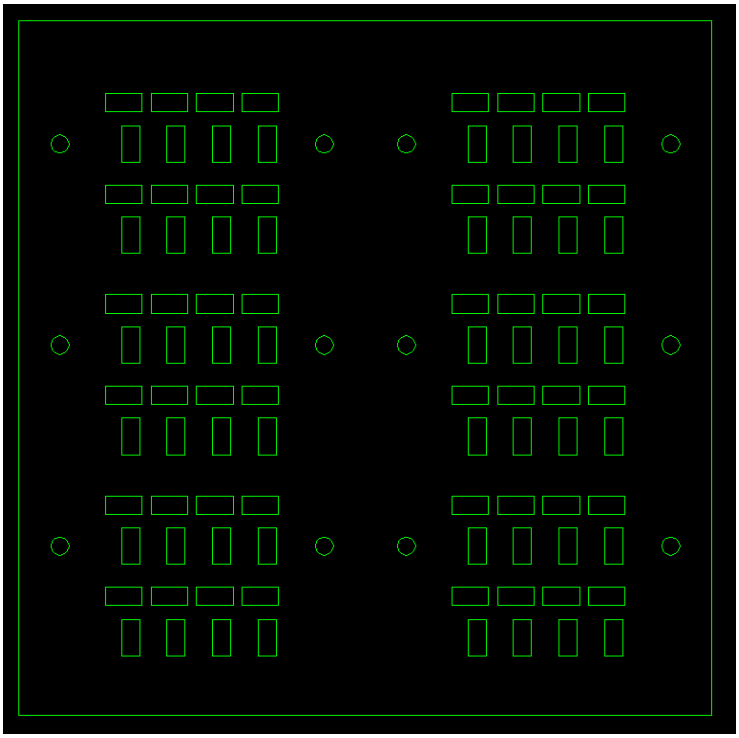


(a)



(b)

(c)



(d)

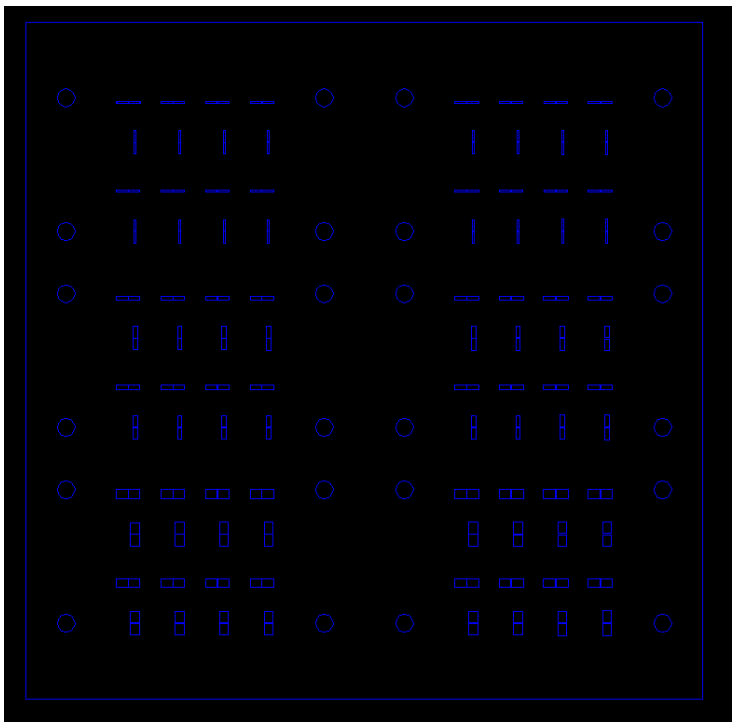


Figure A1. AutoCAD mask design: (a) gate electrode, (b) gate dielectric, (c) semiconductor and (d) source-drain electrodes design.