Stability and Accuracy Enhancement of Power Hardware-in-the-Loop Simulation

PhD Thesis

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

Driven by the target of decarbonization through eliminating carbon emissions and developing a renewable and sustainable energy schemes, the modern power industry has been experiencing a remarkable transition. To support this, Power Hardware-in-the-Loop (PHIL) simulation, an advanced and efficient method incorporating physical power apparatus and emulated power network into a real-time testing configuration, has been leveraged for the prototyping of power components, the verification of novel control paradigms, and dynamic modelling of renewable energy systems under broad-spectrum testing scenarios.

The power amplifier, sensors, and signal conversion units based power interface bridges the hardware and real-time simulation platform into PHIL closed-loop setup. However, the dynamics and non-ideal characteristics stemming from the power interface (e.g., time delay, limited bandwidth, noise perturbation, and signal distortion) pose significant challenges to the PHIL closed-loop simulation regarding its stability and accuracy. From the perspective of system performance, these challenges associated with unstable system operation, protective apparatus tripping, and accuracy deterioration issues have been intriguing many academic researchers and industrial engineers and remained to be resolved. In this thesis, research efforts have been devoted to developing novel compensation schemes to improve the stability and accuracy of PHIL simulation and thus enabling a more robust simulation environment that is extendable and re-configurable for future real-time testing of complex power systems and power apparatus.

This thesis works towards the development of novel PHIL system compensation methods, designed specifically to mitigate the detrimental impact of the power interface on the stability and accuracy of PHIL closed-loop systems. Firstly, a compensation scheme comprising a Smith predictor compensator is proposed to mitigate the stability deteriorating impact stemming from the time delay. Furthermore, an online system impedance identification technique is leveraged to enhance the robustness of the proposed compensator and facilitate this compensation scheme with adaptivity to PHIL system impedance variation. Secondly, the sliding discrete Fourier transform based interfacing signal manipulation in conjunction with the phase shift addition method is proposed to compensate for the time delay on a harmonic-by-harmonic basis. Based on the proposed time delay compensation method, an optimal compensation filter is designed to compensate for the non-ideal power interface by maximising its bandwidth, maintaining its unity-gain characteristic, and compensating for its phase-shift over the frequencies of interest. This compensation scheme is crucial for improving the power signal synchronisation accuracy and the power transfer transparency. Thirdly, a novel scheme for sensitivity analysis of PHIL setups is proposed to facilitate quantitatively analysing and assessing the impact of external disturbances stemming from the sensor noise, switching harmonics, or quantization noise on the power interface. In addition, the inherent relationship between sensitivity transfer functions and stability criteria is elaborated along with theoretical and experimental validation. Based on this concept, accuracy assessment methods are employed in this scheme to quantify generic sensitivity criteria. Finally, a comprehensive assessment of the PHIL interfaces regarding their suitability, stability, and applicability for incorporating a grid-forming converter with black-start capability into PHIL closed-loop simulations is presented, and the current-type interfacing method with compensation and scaling scheme is proposed to interface a grid-forming converter with soft black-start capability into a PHIL setup.

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Last but not least, I would like to thank my parents, and sister for their unconditional support and encouragement that guided me throughout my PhD. This thesis is dedicated to them and my wife and children in the future.

Contents

List of Figures

List of Tables

List of Tables

Abbreviations

AC	Alternating Current
ADC	Analogue-to-Digital Converter
DAC	Digital-to-Analogue Converter
DC	Direct Current
DERs	Distributed Energy Resources
DFT	Discrete Fourier Transform
DG	Distributed Generation
DIM	Damping Impedance Method
DPSL	Dynamic Power System Laboratory
DRTS	Digital Real-Time Simulator
FFT	Fast Fourier Transform
GFC	Grid-Forming Converter
GM	Gain Margin
GSDFT	Goertzel Algorithm-Based Sliding DFT
GTAI	Giga-Transceiver Analogue Input
GTAO	Giga-Transceiver Analogue Output
HuT	Hardware under Test
HVDC	High-Voltage Direct Current

IAs	Interface Algorithms
IIR	Infinite Impulse Response
IR	Impedance Ratio
ITM	Ideal Transformer Model
I-ITM	Current-Type ITM
LHP	Left Half-Plane
LL	Line-to-Line
LPF	Low-pass Filter
MIPTE	Maximum Instantaneous Power Tracking Error
MV	Medimum Voltage
MW	Mega-Watt
PA	Power Amplifier
PCC	Point of Common Coupling
PCD	Partial Circuit Duplication
PF	Power Factor
PHIL	Power Hardware-in-the-Loop
PI	Power Interface
PLL	Phase-Locked Loop
PM	Phase Margin
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
RMS	Root Mean Square
RTDS	Real-Time Digital Simulator^{TM}

SDFT	Sliding Discrete Fourier Transform
SG	Synchronous Generator
SISO	Single-Input Single-Output
SNR	Signal to Noise Ratio
SoI	System of Interest
SP	Smith Predictor
THD+N	Total Harmonic Distortion Plus Noise
TLM	Transmission Line Model
UK	United Kingdom
V-ITM	Voltage-Type ITM
VM	Vector Margin
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
VSM	Virtual Synchronous Machine

Chapter 1

Introduction

1.1 Research Context

Driven by the target of decarbonization through eliminating the carbon emissions of primary energy resources and developing a renewable and sustainable energy utilisation scheme, the modern power industry has been experiencing remarkable transition in the past decades [1–7]. Thanks to the advancement of emerging state-of-the-art power conversion techniques, the power network has been witnessing increasingly high penetration of Distributed Generation (DG), which integrates various Renewable Energy Sources (RES) into the conventional power grid through dedicated interfacing power converters [3–7]. These converters, operating in grid-following mode or grid-forming mode, not only play a significant role in incorporating a wider-scale Distributed Energy Resources (DERs) into the power grid but also result in more complex interconnections between DERs and power grid [4, 7]. These interactions inevitably introduce unexpected and unstable dynamics to power converters and power grid, drastically expose the vulnerabilities of the power grid, and pose significant threat to the reliability and security of the converter-dominated power network.

Consequently, a comprehensive and in-depth investigation of the power con-

verter and its tightly coupled interactions with the power network under various operating conditions is crucial before its final-stage systematic deployment. In terms of the testing and investigation of the candidate power apparatus and its interactions with the power systems, the most straightforward approach is using the pure-hardware experiments. However, due to the limited flexibility and power capacity and high expense of the pure-hardware experiment, it is always infeasible and inefficient to carry out repeated testing and in-depth investigation of the Hardware under Test (HuT) in a cost-effective and de-risking manner. Based on the advanced mathematical modelling of the power system [8, 9], offline digital simulations are employed to emulate small-scale power system and to test physical HuT before its final-stage deployment [10,11]. However, the large-scale power network with increasing penetration of the power electronics and distributed generations requires high-fidelity mathematical modelling and remarkably high computation, which pose significant challenges to the off-line digital simulation. On the other hand, a mathematical modelling-based digital simulation cannot thoroughly represent the dynamic behaviour of the physical HuT neither to carry out the investigation of its interconnections with the emulated power systems.

To make up for the deficiencies of aforementioned testing approaches, the real-time power hardware-in-the-loop (PHIL) simulation, a state-of-the-art testing technique combining Digital Real-Time Simulator (DRTS) and hardware experiments into a closed-loop testing environment [12–14], is exploited as an effective way to narrow the gap between computation-based digital simulation and pure analogue hardware laboratory testing. Advanced real-time simulation platforms, such as Real-Time Digital Simulator$^{\text{TM}}$ (RTDS), OPAL-RT$^{\text{TM}}$, and Speedgoat$^{\text{TM}}$ performance real-time target machine, etc., facilitate the simulation capability of PHIL, which enable large scale power systems to be replicated accurately in the real-time simulation environment and provides an effective way to carry out non-destructive and repeated investigation of the interdisciplinary system

simulation and candidate apparatus prototype under broad-spectrum operating conditions, in particular for the extreme scenarios [13, 15, 16]. It significantly de-risks the entire testing and degrades the expense and time-to-market of research and development in the modern power industry. Above all, the PHIL real-time simulation paved a new pathway in investigating the interactions between the physical power components under test and the real-time emulated power grid in a closed-loop configuration, which has been extensively employed in the testing and prototyping of power apparatus [16–19], laboratory-based power system education [19], validation of novel control strategies [20], geographically distributed real-time co-simulation [21, 22], black start testing of grid-forming converter [23, 24], and dynamic modelling and prototyping of renewable energy systems involving variable-speed wind turbines [25], photovoltaic cell [26,27], and energy storage resources [28, 29].

For a typical PHIL system, the power amplifier, sensors, and signal conversion units-based power interface bridges the hardware and real-time simulation platform into PHIL closed-loop setup. However, the dynamics and non-ideal characteristics (e.g., time delay, limited bandwidth, noise perturbation, and signal distortion) stemming from the Power Interface (PI) pose significant challenges to the PHIL closed-loop simulation regarding its stability and accuracy. For laboratory-based or industrial applications, if a real-world PHIL experimental validation enters an unstable state, the system's voltage and current can become divergent, resulting in significant oscillations. These may lead to over-current protective tripping of the interfacing power amplifier, or in some cases, cause irreparable damage to the HuT. Such occurrences can lead to substantial economic losses and jeopardize personal safety. On the other hand, the accuracy issue arising from the time delay and signal distortion can lead to unsynchronised power signals and power mismatches between the DRTS and HuT sides. Consequently, this can result in inaccurate dynamic behaviours being applied to the HuT and

can also lead to a deterioration in the HuT associated control performance. From the perspective of system performance, these challenges and issues associated with stability and accuracy have been intriguing many academic researchers and industrial engineers and remains to be tackled.

Despite the technological advancements of the real-time computing technique and the novel power amplifier promoted the extensive utilisation of PHIL real-time simulation technique, the stability and accuracy issues arising from the power interface need to be resolved in order to establish a robust and stable PHIL testing with high-fidelity and re-configurability, which are of great significance in the wide extension and application of PHIL system for real-time testing of complex power system and power apparatus in the future. The research work conducted in this thesis focuses on the development of novel compensation schemes to enhance the stability and accuracy of PHIL simulation setups.

1.2 Research Motivation

PHIL system is defined as a closed-loop system consisting of a digital real-time simulation platform interfacing with the hardware under test (HuT) through a dedicated power interface (PI), which facilitates the conservation of instantaneous power transfer as existed in the real-world system through natural coupling. As illustrated in Figure 1.1, the power interface comprising a Power Amplifier (PA), voltage and current sensors, signal conversion cards (i.e., Analogue-to-Digital Converter (ADC) and Digital-to-Analogue Converter (DAC)), and low-pass filters employed for noise mitigation, inevitably introduces non-ideal characteristics and dynamics such as time delay, noise, or signal magnitude distortion to the PHIL closed-loop simulation system. From the perspective of system modelling and operation, these non-idealities play a crucial role in determining the stability and in deteriorating the system accuracy. Stability and accuracy are regarded

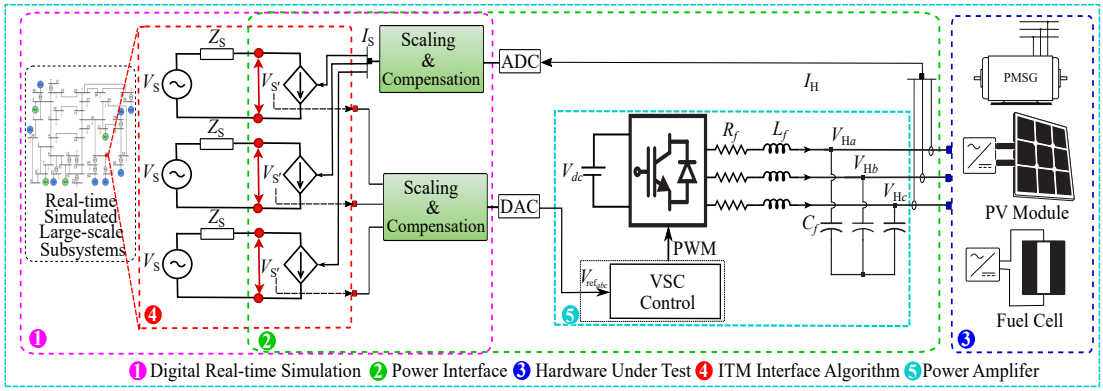

Figure 1.1: A typical PHIL setup and a conceptual representation of its topology.

as the utmost important factors for a well-established PHIL simulation setup. The stability and accuracy issues arising from the non-ideal characteristics and dynamics of the power interface and the closed-loop system are elaborated as follows:

- **Time delay stemming from the power interface**

  Owing to the splitting of the original System of Interest (SoI) into a digital real-time simulation and physical power hardware that are interconnected by a power interface, the digital processing of DRTS platform, the signal conversion cards (i.e.,ADC and DAC), and the digital control of the power amplifier all inevitably introduce time delays to the PHIL closed-loop configuration and these has been further characterized in [30]. From the system modelling and control point of view, the aggregated time delay in the PHIL closed-loop system results in negative phase response and consequently deteriorates the system stability margins. As presented in [31], the PHIL closed-loop system reaches an unstable state once the time delay exceeds a threshold value leading to the system phase response breaches its stability margin. On the other hand, as reported in [32], the time delay deteriorates the accuracy of power signal synchronisation and the transparency of power transfer within the PHIL setup.

- **Impedance ratio and system impedance variation**

  Apart from the degraded PHIL closed-loop system phase margin arising from the time delay, the impedance ratio between the digital real-time simulation side and hardware component side is another key determinant of the PHIL closed-loop system gain margin. As demonstrated in [33–35], the PHIL stability is strictly constrained by the impedance ratio between the simulation side and hardware side. Such a stringent impedance ratio constraint is not always ensured in practice due to the impedance variations of the emulated power network and hardware components during an experimental scenario run. Consequently, the existing PHIL interface may no longer be suitable for guaranteeing the stability of a PHIL system with inherent impedance variation. In light of this, there are new chances to develop novel compensation techniques to fill the identified research gaps between the PHIL stability and the inherent variable impedance characteristic of the PHIL system.

- **Limited bandwidth and non-unity gain characteristic of PA**

  Despite a power amplifier with ideal characteristics (i.e., infinite bandwidth and unity gain) being expected in the PHIL system [33,36], the actual power amplifier, which is modelled as time delay and a low-pass filter in [30,37–39], presents non-ideal characteristics (i.e., limited bandwidth, non-unity gain, and resonance of the passive output filter). These characteristics result from its digital control strategies and the passive output filters that are employed to limit the output voltage ripple stemming from high-frequency pulsating modulation and realise accurate power signal replication. These non-ideal characteristics lead to power signal magnitude distortion and limit the applicability of PHIL simulation with only a limited harmonics can be replicated accurately in one PHIL experiment.

- **Non-zero phase shift and non-unity magnitude response of PA output filter**

  The power amplifier output filter introduces a non-zero phase shift that can have similar effects as the loop phase lag resulting from time delays caused by multiple stages in the PHIL closed-loop system [30]. These effects include reducing the system stability margin, deteriorating the power signal synchronisation accuracy, and degrading the transparency of power transfer between DRTS and HuT in a PHIL closed-loop setup [30, 31, 33]. In addition, the non-unity magnitude response of this output filter at the frequency of interest leads to the attenuation or amplification of the reference signal to be replicated by PA, which can result in further deterioration of the accuracy of power signal synchronization and a degradation of the transparency of power transfer between the DRTS and HuT in a PHIL closed-loop setup.

- **Disturbance and deteriorated performance**

  Due to the implementation of the non-ideal power interface, external disturbances are inevitably injected into the PHIL setup and are mainly stemmed from (i) Offset noise in the measurement units, (ii) Quantization error/noise in the ADC card, (iii) Sensor measurement noise (typically high-frequency), and (iv) Switching harmonics stemming from high-frequency pulsating modulation. From an application point of view, a comprehensive sensitivity analysis and assessment of the impact of these disturbances on system operation is crucial for a high-fidelity and robust PHIL simulation. In contrast to the well-presented schemes for PHIL system stability analysis and accuracy assessment in the literature, no sensitivity analysis scheme has been developed within the PHIL community.

- **Stability issue arising from the lack of power signal synchronisation in the PHIL interface dedicated to the testing of grid-forming**

converter with black-start capabilities

Grid-Forming Converter (GFC) establishes a stable and controllable voltage at its output terminal without requiring external angle reference, which enables the GFC to be a candidate for providing black-start services. The application of PHIL simulation for GFC testing has attracted significant interest from academic researchers and industrial engineers. The voltage-type PHIL setup has been extensively employed for the real-time testing of grid-following converter, which regulates its voltage angle to be synchronised with that of the interfacing voltage-type power amplifier (i.e., a grid simulator) by employing a dedicated synchronisation unit (e.g., Phase-Locked Loop (PLL)) [20, 27, 29, 40, 41]. However, the voltage-type interface is not capable of incorporating a GFC in the PHIL setup for black-start testing. This is because GFC regulates output voltage by using the angular frequency reference generated by its internal dedicated unit. The direct coupling of the GFC and interfacing power amplifier may lead to stability issues arising from their independent and inherent voltage regulation and the lack of voltage angle synchronisation at their coupling point. This results in new research opportunity to develop new power interface that is dedicated to the testing of GFC with black-start capability, thus addressing the limitation of conventional voltage-type interfacing method.

Motivated by addressing these research challenges, the research efforts in this thesis have been devoted to developing novel PHIL compensation and interfacing methodologies. These are underpinned by identifying, assessing and analysing the limitation of the existing schemes proposed for improving the stability, accuracy, and applicability of PHIL system in the literature. Subsequently, novel compensation and interfacing techniques are proposed to establish a more robust PHIL system with higher fidelity than the conventional one.

1.3 Research Contributions

This thesis contributes the following aspects toward the existing body of knowledge:

- Detailed modelling of the PHIL setup with its state-of-the-art highlighted along with its key attributes including the closed-loop system stability and accuracy, in particular the power signal synchronisation accuracy and power transfer transparency. A comprehensive comparison and assessment of the existing PHIL stability stabilisation schemes are presented in conjunction with an in-depth analysis of their advantages and key limitations. More details of these aspects are elaborated in Chapter 2.

- A Smith Predictor (SP) criterion inspired compensator is designed to mitigate the negative impact of the time delay on the PHIL closed-loop stability. Although a passive approach, this passive compensator introduces a buffer in variability of the impedances and enables a stable PHIL experiment over a wider range of scenarios. Robustness analysis of the passive compensator against the modelling error stemming from system impedance variation is presented and the stability constraint of the passive compensator-based PHIL system is defined. Detailed analysis, assessment, and experimental validation of this proposed compensator are presented in Chapter 3.

- To further enhance the robustness of Smith predictor compensator and overcome the limitation of its passive attribute, an adaptive Smith predictor based on a computationally efficient online impedance parameter identification technique is proposed. The accurate impedance identification allows for the parameters of the Smith predictor being adapted in real-time to ensure seamless operation catering to any variations in impedance during the experimental run. A real-world PHIL experiment involving passive

load bank and power converter is employed to verify the effectiveness and demonstrate the applicability of the proposed compensation scheme. This contribution and its associated details are presented in Chapter 3.

- Investigation and assessment of the existing time delay compensation methods from the perspective of improving the PHIL system accuracy. On the other hand, the limitations of the conventional time delay compensation methods including the phase lead compensator and Fast Fourier Transform (FFT) based frequency domain phase lag compensation algorithm are presented. A computation-efficient Sliding Discrete Fourier Transform (SDFT) based time delay compensation method is proposed to compensate for the time delay on a harmonic-by-harmonic basis. This proposed time delay compensation scheme is further presented in Chapter 4.

- Design and development of a compensation scheme for the open-loop controlled Voltage Source Converter (VSC) power amplifier to enable more accurate power signal synchronisation and power transfer within the PHIL closed-loop simulation. This compensation method is designed to maximise the bandwidth of the power interface, preserve unity-gain over a wider frequency range, and compensate for the phase lag in the PHIL closed-loop via optimal tuning of the proposed compensator. In addition, it compensates for the phase lag on a harmonic-by-harmonic basis. An analytical assessment and a comprehensive comparison of the proposed compensator over the compensation techniques (e.g., lead-lag filter, notch filter) published in the literature are presented from the perspective of their frequency response characteristics and closed-loop stability of the compensation scheme-based PHIL setup. The effectiveness of this compensation method has been evaluated via the proposed accuracy metrics and simulation results. The design criteria and validation of this method are presented in Chapter 4.

- A scheme for sensitivity analysis of PHIL setups is developed by using transfer functions describing the dynamic behaviour of forward and feedback paths. The inherent relationships between stability, accuracy and sensitivity are elaborated and verified by the scheme and allow for a precise estimation of PHIL system properties prior to experimental testing. Based on this scheme, accuracy assessment methods are employed to quantify generic sensitivity criteria. A converter-based PHIL setup is employed to demonstrate the applicability of the proposed scheme. From an application point of view, the proposed scheme is crucial for facilitating the quantitative analysis and assessment of the impact of external disturbances on PHIL simulation systems. This contributes to the design and implementation of a high-fidelity and robust PHIL simulation. In-depth explanation and verification of this proposed scheme are presented in Chapter 5.

- A current-type interfacing method is proposed to interface a grid-forming converter with soft black-start capability into a PHIL setup. Scaling and compensation schemes are developed for a robust and high-fidelity PHIL simulation guaranteeing an accurate replication of the dynamics of the emulated power network at the physical GFC interfacing point. To support its adoption, stability analysis of this PHIL setup is presented. On the other hand, a comprehensive assessment and evaluation of the voltage-type, current-type, and partial circuit duplication method based PHIL interfaces regarding their suitability and applicability for incorporating grid-forming converter with black-start capability into PHIL closed-loop simulation are presented. These offer meaningful insights for selecting proper interfacing method. Analytical assessment and experimental validation involving interfacing a 90 kVA power converter implemented with grid-forming control scheme are presented to verify the proposed methodology. Detailed analysis and experimental validation of this interface are presented in Chapter 6.

1.4 Thesis Overview

An overview of the chapters within this thesis is presented as follows:

Chapter 2: This chapter presents the state-of-the-art of real-time PHIL system along with its key technical challenges to be tackled. Emphasis is placed on the detailed modelling of the PHIL system from the perspective of its architecture, interface algorithms, and mathematical modelling of its subsystems. Based on the detailed system modelling, the key determinants (i.e., time delay and impedance variation) for the PHIL stability are identified along with a frequency domain assessment of their impacts on the PHIL stability. Following on from this, the novel compensation schemes that are dedicated to improving the PHIL stability in the literature are comprehensively reviewed. The design criteria, functionality, advantages and the main limitation of these advanced PHIL stabilisation schemes are summarised. On the other hand, the deteriorated PHIL system accuracy stemming from the time delay and non-ideal power interface is further investigated from the aspect of power signal synchronisation and power transfer transparency. Accuracy metrics are proposed to quantitatively assess the PHIL power signal synchronisation and power transfer transparency in transient and steady-state.

Chapter 3: Having identified the detrimental impact of the time delay and impedance variation on the PHIL system stability, this chapter focuses on the development of PHIL stabilisation scheme. To address the limitation of existing PHIL system stabilisation methodologies as presented in Chapter 2, this chapter presents an adaptive Smith predictor based PHIL stability enhancement scheme. The proposed Smith predictor compensation scheme is presented with emphasis placed on its design criteria, operational principle, and assessment of Smith predictor based PHIL system stability. Moreover, with the system impedance inherent variation characteristics taken into account, the robustness of Smith predictor

is analysed and the stability constraints of the PHIL system is further identified. To facilitate the Smith predictor with adaptivity to the system impedance variation, the online SDFT and vector fitting algorithm based impedance identification method is developed. Finally, analytical assessments of the proposed adaptive Smith predictor compensation scheme are presented along with pure simulations and a real-world PHIL experimental validation.

Chapter 4: This chapter presents an interface compensation method that enables more accurate power signal synchronisation and power transfer within a PHIL setup, which is based on an open-loop controlled voltage source converter power amplifier. Detailed modelling of the PHIL system with an open-loop controlled voltage source converter power amplifier is presented along with an assessment of the impact of power amplifier on PHIL system stability and accuracy. These are followed by a comprehensive assessment of the compensation techniques (e.g., lead-lag filters, notch filter) published in the literature from the perspective of compensating for the power amplifier non-unity characteristics. To address the limitation of these compensation methods, an optimal filter tuning based method is further presented to maximise the bandwidth of power interface, preserve unity-gain over a wider frequency range. The effectiveness of proposed compensator in maximising the bandwidth of the power interface is demonstrated by frequency-domain assessment. To mitigate the detrimental impact of time delay on the PHIL accuracy, SDFT based time delay compensation method is employed in conjunction with the proposed optimal filter tuning based method. Furthermore, the performance of proposed method regarding its capability in improving the power signal synchronisation and enhancing the power transfer transparency in the PHIL closed-loop configuration is validated and demonstrated via the proposed accuracy metrics and PHIL simulation results.

Chapter 5: This chapter presents the proposed scheme for sensitivity analysis of the PHIL system. Firstly, the originations of the external disturbance within the

PHIL setup are summarised and the detailed modelling of the current-type power interface is presented. Following these, the principles of sensitivity analysis are explained followed by the derivation of sensitivity analysis metrics for PHIL simulation setups. Based on the proposed sensitivity analysis scheme, the inherent relationship between sensitivity transfer functions and stability criteria is elaborated along with analytical assessment. Furthermore, the accuracy assessment methods employed in the proposed scheme to quantify generic sensitivity criteria are presented. Moreover, a converter-based current-type PHIL experiment is leveraged for the evaluation of sensitivity analysis scheme, and experimental results are presented to characterize and demonstrate the applicability of the proposed scheme.

Chapter 6: This chapter presents the design and development of a current-type interface that is dedicated to the PHIL testing of grid-forming converter with black-start capability. The novel grid-forming control principles and the key attributes for enabling grid-forming converter to be a candidate for providing black-start provision service are presented. Following this, the interfacing coupling point voltage stability issue of the conventional voltage-type PHIL interface is analysed and further demonstrated by simulation results. The applicability of proposed current-type interface for grid-forming converter testing and the proposed scaling and delay compensation are presented along with its detailed system modelling. Based on this, the stability analysis and analytical stability assessment of the proposed current-type interface is presented. Finally, simulation results of a real-world PHIL experiment incorporating a Triphase 90 kVA power converter that is implemented with grid-forming control scheme are presented to validate the proposed PHIL interface.

Chapter 7: This chapter concludes the thesis by summarising the scopes of research outputs, highlighting the principle contributions, and identifying several potential directions that are worthy of being explored as future work.

1.5 List of Publications

The key publications resulting from this thesis are summarised as follows:

1.5.1 Journal Articles

- **Feng Z**, Pena Alzola R, Syed M, Norman P & Burt G. "Adaptive Smith Predictor for Enhanced Stability of Power Hardware-in-the-Loop Setups," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 10, pp. 10204-10214, 2023, doi: 10.1109/TIE.2022.3224196.

- Alassi A, **Feng Z**, Ahmed K, Syed M, Egea-Alvarez A & Foote C. "Grid-Forming VSM Control for Black-Start Applications with Experimental PHiL Validation," in *International Journal of Electrical Power & Energy Systems*, vol. 151, pp. 109119, 2023, doi: 10.1016/j.ijepes.2023.109119.

- Paspatis A, Kontou A, **Feng Z**[1], Syed M, Lauss G, Burt G, Kotsampopoulos, P & Hatziargyriou, N. "Virtual Shifting Impedance Method for Extended Range High-Fidelity PHIL Testing," in *IEEE Transactions on Industrial Electronics*, early access, April, 2023, doi: 10.1109/TIE.2023.3269467.

- Lauss G, **Feng Z**, Syed M, Kontou A, De Paola A, Paspatis A & Kotsampopoulos, P. "A Framework for Sensitivity Analysis of Real-Time Power Hardware-in-the-Loop (PHIL) Systems". in *IEEE Access*, vol. 10, pp. 101305-101318, 2022, doi: 10.1109/ACCESS.2022.3206780.

- Han J, Hong Q, **Feng Z**, Syed M, Burt G & Booth C. "Design and Implementation of a Real-Time Hardware-in-the-Loop Platform for Prototyping and Testing Digital Twins of Distributed Energy Resources," in *Energies*. 2022 Sep 10; 15(18). 6629. doi: 10.3390/en15186629.

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1.5.2 Conference Papers

- Zaman T, **Feng Z**, Syed M, Pilscheur B, Flynn D, & Burt G. "Multimode synchronous resonance detection in converters dominated power system using synchro-waveforms," in *CIRED 2023 - The 27th International Conference and Exhibition on Electricity Distribution.* IET, accepted/in press, April, 2023.

- **Feng Z**[2], Alassi A., Syed M, Pena Alzola R., Ahmed K., & Burt G. "Current-type power hardware-in-the-loop interface for black-start testing of grid-forming converter," in *IECON 2022, The 48th Annual Conference of the IEEE Industrial Electronics Society.* Piscataway, N.J.: IEEE. 2022. pp. 1-7, doi: 10.1109/IECON49645.2022.9968517.

- **Feng Z**, Pena Alzola R, Seisopoulos P, Syed M, Guillo-Sansano E, Norman P & Burt G. "Interface compensation for more accurate power transfer and signal synchronisation within power hardware-in-the-loop simulation," in *IECON 2021 – The 47th Annual Conference of the IEEE Industrial Electronics Society.* Piscataway, N.J.: IEEE. 2021. pp. 1-8, doi: 10.1109/IECON48115.2021.9589158.

- **Feng Z**, Pena Alzola R, Seisopoulos P, Guillo Sansano E, Syed M, Norman P & Burt G. "A scheme to improve the stability and accuracy of power hardware-in-the-loop simulation," in *IECON 2020, The 46th Annual Conference of the IEEE Industrial Electronics Society.* Piscataway, N.J.: IEEE. 2020. pp. 5027-5032, doi: 10.1109/IECON43393.2020.9254407.

[2] This paper was awarded with the IEEE Industrial Electronics Society Young Professional & Student Paper Assistance Award.

1.5.3 Technical Reports

- Alassi A, **Feng Z**, Syed M, Egea-Alvarez A, Ahmed K & Burt G. "Distributed ReStart: Non-Conventional Black-Start Resources: RTDS Based Network Energization from Grid Forming Converters: Part 2," *National Grid*, Warwick, 14, Jul, 2022. 14 p.

  https:// www.nationalgrideso.com/document/268201/download

  https://pureportal.strath.ac.uk/en/publications/distributed-restart-non conventional-blackstart-resources-rtds-bas

- Alassi A, **Feng Z**, Avras A, Syed M, Egea-Àlvarez A & Ahmed K. "Distributed ReStart: Non-Conventional Black-Start Resources: RTDS Based Network Energization from Grid Forming Converters: Part 1," *National Grid*, Warwick, 23, Nov, 2021. 20 p.

  https://www.nationalgrideso.com/document/226951/download

  https://pureportal.strath.ac.uk/en/publications/distributed-restart-non-conventional-black-start-resources-rtds-b

Chapter 2

Power Hardware-in-the-Loop (PHIL) Simulation Techniques

This chapter presents the literature review of the PHIL simulation techniques along with their generic modelling and identified key attributes. The remainder of this chapter is organized as follows: Section 2.1 presents the state-of-the-art PHIL techniques. In Section 2.2, the detailed system modellings from the perspective of PHIL configuration, interfacing topology, and the mathematical modelling of power interface and system components are presented. Section 2.3 presents the PHIL stability attribute, the principles for determining the stability, along with a comprehensive evaluation of the stabilisation schemes in the literature. Section 2.4 presents the PHIL accuracy analysis, the criteria derivation for PHIL power transfer transparency studies, and the proposed accuracy assessment methods. Section 2.5 concludes this chapter[1].

[1] The mathematical modelling and theoretical derivations in this chapter are extended from the conference publications [31, 32] and journal publications [42, 43].

2.1 State-of-the-Art of PHIL

The real-time power hardware-in-the-loop simulation, a state-of-the-art simulation technique that combines real-time digital simulation and hardware experiments into a closed-loop testing environment, is exploited as an effective way to narrow the gap between computation-based digital simulation and pure analogue hardware experiment in a controlled laboratory setup [11–13, 33, 38]. Emerging novel computation technology facilitates the capability of the power hardware-in-the-loop simulation to carry out comprehensive and in-depth investigation of large-scale complex power systems and candidate power apparatus or control paradigms under broad-spectrum operation conditions before their final deployment as well as systemic application [12, 13, 15–17]. This plays a significant role in accelerating the research and development of the emerging novel power technologies by enabling repeated and non-destructive real-time testing under a broad range of scenarios and a variety of grid configurations [13, 15, 16, 19, 20, 23, 25, 26, 44–46]. On the other hand, with the real-time digital simulated system and pure power hardware comprised in a closed-loop testing environment, the interaction between the power apparatus and the real-time simulated power network can be thoroughly investigated without the expense and risk of field trials. This advanced real-time testing methodology has been extensively leveraged for the in-depth modelling and assessment of renewable energy technologies including photovoltaic system [26, 44], energy storage system [45], variable-speed wind turbines [25], etc., prototyping of power apparatus [16, 17, 19, 46], verification of control strategies [20], the geographically distributed real-time co-simulation [21], black start testing of grid-forming converter [23], and power system education [19], etc.

In spite of the extensive and widely utilisation of the PHIL simulation technique, PHIL is not a plug-and-play setup that just leverages an off-the-shelf real-

time digital simulator and power hardware. A dedicated power interface consisting of power amplifier, signal conversion cards, and voltage or current sensors bridges the real-time simulation side and hardware. However, this power interface naturally comprises inherent time delay (as characterised in [30]) stemming from the power amplifier digital control, sensors, signal conversion stages and signal distortion arising from the power amplifier filters. From the perspective of system performance, these characteristics that are not exist in the real-world system of interest pose significant threat to the stability and accuracy of PHIL system. To ensure the PHIL experimental results to be precise and representative of the real-world SoI, the power interface that bridges the software side and hardware side should be well designed and implemented to enable stable and accurate PHIL operation.

The PHIL stability and accuracy issues arising from the non-ideal power interface have been remaining to be addressed and many research efforts have been devoted to this research area. To tackle these issues, a comprehensive and representative system modelling and in-depth analysis of the key determinants for these issues are important and will be the core sections in this chapter.

2.2 PHIL System Modelling

This section describes the architecture of PHIL setup and presents a comprehensive assessment of the interfacing methodologies. Detailed PHIL system component modelling is presented along with the system transfer functions.

2.2.1 PHIL Configuration and Interfacing Methods

PHIL simulation combines the physical power component with real-time emulated system into a closed-loop testing configuration that mimics the original system of interest (SoI). Figure 2.1 illustrates the SoI and its corresponding PHIL simula-

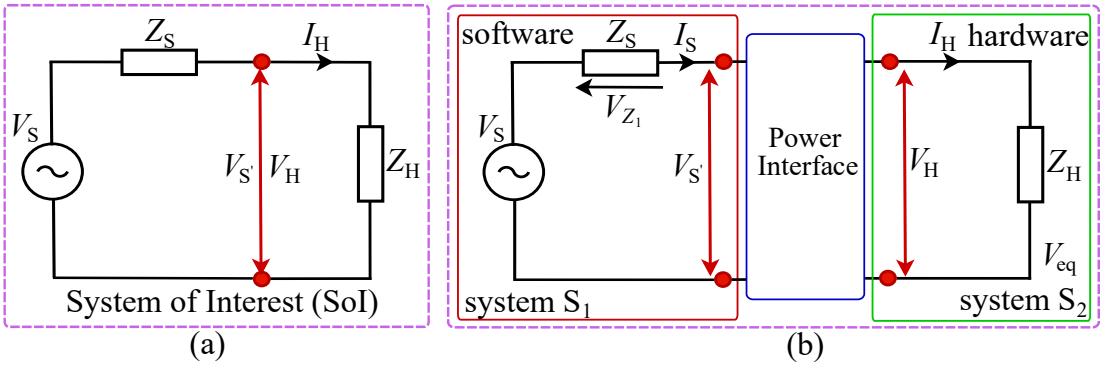

Figure 2.1: Principle topology of (a) system of interest (SoI) and (b) the corresponding PHIL simulation system.

tion system. The original SoI is expressed by a lumped voltage divider topology comprising two series-connected Thévenin equivalent circuits S_1 and S_2, respectively. S_1 represents the real-time emulated power network in DRTS referred to as software side and S_2 represents the real-world HuT referred to as hardware side. System S_1 comprises a voltage source V_S in series with an equivalent impedance Z_S of the simulated system in the software side and system S_2 comprises the hardware side equivalent impedance Z_H. As illustrated in Figure 2.1(b), these two subsystems are coupled through a power interface (PI) in the PHIL setup.

A typical power interface comprises a power amplifier, signal conversion cards and voltage or current sensors. Two signal conversion cards are typically employed - a digital-to-analogue converter (DAC) card and an analogue-to-digital converter (ADC) card. The ADC card incorporates a low-pass filter in series to eliminate high frequency noise components within the analogue signal. The configuration of these components and the manner in which the power is transferred between the DRTS and the HuT are defined by the Interface Algorithms (IAs) [33]. Interface algorithms such as the Ideal Transformer Model (ITM), the Damping Impedance Method (DIM), the Partial Circuit Duplication (PCD), and Transmission Line Model (TLM) have been discussed and evaluated in literature [13, 33, 38, 47–49].

Table 2.1: Comparison of the interface algorithms regarding stability, accuracy, and ease of implementation.

Interface algorithms [13, 33, 49]	**Stability**	**Accuracy**	**Ease of Implementation**
Ideal transformer model (ITM)	Low	Medium	High
Damping impedance method (DIM)	Medium	High	Medium
Partial circuit duplication (PCD)	High	High	Medium
Transmission line model (TLM)	High	Low	Low

Depending on the level of stability and accuracy performance and the ease of implementation of the aforementioned IAs, the criteria Low/Medium/High were leveraged to assess these IAs. Consequently, a comparative summary of these IAs is presented in Table 2.1. Note that ease of implementation refers to the level of complexity involved in putting the relevant interface algorithm into practice, while taking into account the amount of the availability of laboratory resources and the computation resources, time and expertise required.

As shown in Table 2.1, among these mentioned interfacing methods, ITM is the most straightforward way as a result of its ease of implementation and relatively high and acceptable stability and accuracy performance. In spite of the complex structure, DIM, as a combination of ITM and PCD, can provide the best trade-off between stability and accuracy under the circumstance that the damping impedance can ideally match with the impedance of HuT [13,33,47,49]. Even though PCD interface presents remarkably high stability, its accuracy is determined by the system converging speed and the relatively large linking impedance and small HuT impedance, which are always not practical and infeasible in the real world [33, 49]. As a result of the passive linking impedance, the TLM interface algorithm presents high stability, which is at the expense of the accuracy under the assumption that the transmission time constant is equal to the time step [33, 49]. Moreover, this method is limited by its difficulty for practical implementation and the high requirement of linking impedance.

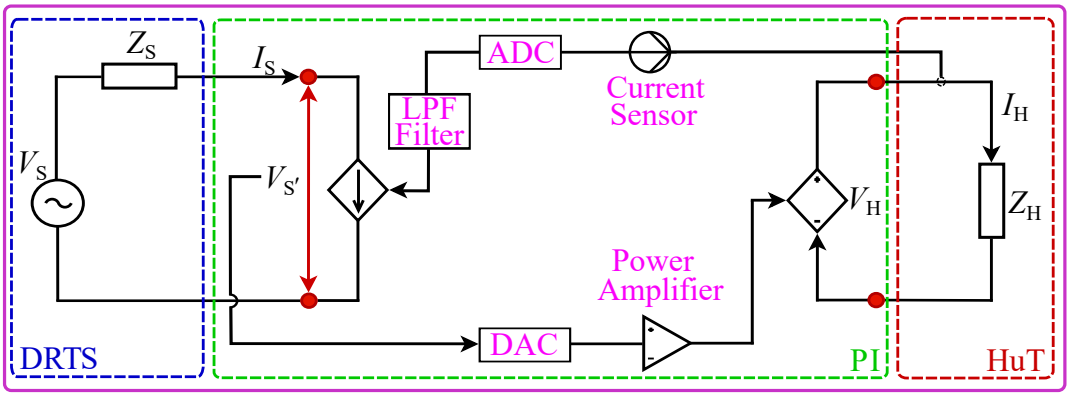

Figure 2.2: Equivalent model of the PHIL system with voltage-type ITM interface.

2.2.2 ITM-Based Interface Modelling

Among the interfacing methods dedicated to the PHIL setup, the ITM interface is widely adopted because of its simple implementing structure and shows a good performance with respect to stability and accuracy properties. Depending on the type of power amplification and the controllable power sources implemented in the DRTS and hardware side, ITM can be categorized as voltage-type or current-type. Owing to the availability of the off-the-shelf voltage-type power amplifier, Voltage-Type ITM (V-ITM) interface has been extensively leveraged for the real-time testing of grid-following converter and other power apparatus [20, 27, 29, 40, 41]. This interface will be utilised throughout the chapter.

As shown in Figure 2.2, the V-ITM is configured as a controllable voltage source in hardware side and a controllable current source in DRTS side. The voltage source is controlled by a voltage-type power amplifier that regulates its output voltage by following the command signal that are measured at the coupling point in the simulation side and transmitted through a DAC card. On the other hand, the hardware side current is measured by the current sensor and further processed by a Low-pass Filter (LPF) unit, whose output injects into the emulated network by a controlled current source and thus closing the simulation loop. From the system modelling point of view, the PHIL system is represented

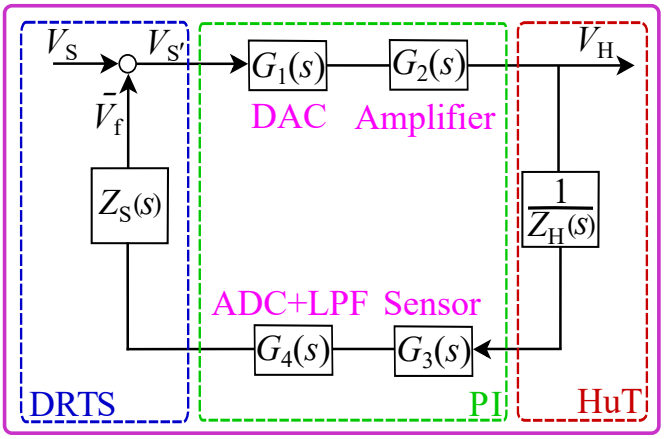

Figure 2.3: Equivalent block diagram of the V-ITM based PHIL system in Fig. 2.2.

in the form of a Single-Input Single-Output (SISO) closed-loop system and the respective equivalent block diagram with all key components and interface signals are presented in Figure 2.3. The open-loop transfer function of this PHIL system is represented as,

$$T_O(s) = \underbrace{G_1(s)G_2(s)G_3(s)G_4(s)}_{G_{PI}(s)} \frac{Z_S(s)}{Z_H(s)}, \tag{2.1}$$

where Z_S and Z_H are the equivalent impedance of the power network within the DRTS platform and the HuT, respectively. $G_{PI}(s)$ is the transfer function of the power interface comprising the transfer functions of DAC card $G_1(s)$, power amplifier $G_2(s)$, current sensor $G_3(s)$, and ADC card in series with a LPF $G_4(s)$.

As summarised in [30], the following processes and units all inevitably introduce time delay (in microsecond scale) to the PHIL closed-loop configuration:

- Digital processing of DRTS platform (50 µs to 100 µs).
- Digital control of the power amplifier (50 µs to 550 µs).
- ADC and DAC signal conversion cards (100 µs to 200 µs).
- Communication latency between different platforms (50 µs to 100 µs).

With the time delay τ in the PHIL closed-loop expressed by its equivalent Laplace transformer ($e^{-s\tau}$) [50], the components in Eq. (2.1) are modelled as,

$$\begin{cases} G_1(s) = k_1 e^{-sT_{\mathrm{d1}}}, & G_2(s) = k_2 \dfrac{1}{\frac{s}{2\pi f_{c2}} + 1} e^{-sT_{\mathrm{d2}}}, \\ G_3(s) = e^{-sT_{\mathrm{d3}}}, & G_4(s) = \dfrac{1}{\frac{s}{2\pi f_{c4}} + 1} e^{-sT_{\mathrm{d4}}}, \end{cases} \tag{2.2}$$

where k_1 and k_2 are the scaling factor of DAC card and power amplifier, respectively. T_{d1} and T_{d4} represent the one time-step delay of DRTS, T_{d2} and T_{d3} are the time delay of the power amplifier and sensor, respectively. f_{c2} is the cut-off frequency of the power amplifier and f_{c4} is the equivalent cut-off frequency of the ADC anti-aliasing filter and LPF. Representing the total time delay in the feed-forward path as $T_{\mathrm{d-ff}}$ and in the feedback path as $T_{\mathrm{d-fb}}$, the aggregated time delay (in microsecond scale) in the open-loop is given by,

$$T_{\mathrm{d}} = \underbrace{T_{\mathrm{d1}} + T_{\mathrm{d2}}}_{T_{\mathrm{d-ff}}} + \underbrace{T_{\mathrm{d3}} + T_{\mathrm{d4}}}_{T_{\mathrm{d-fb}}}. \tag{2.3}$$

The open-loop transfer function Eq. (2.1) is further expressed as,

$$T_{\mathrm{O}}(s) = \underbrace{G^*_{\mathrm{PI}}(s) e^{-sT_{\mathrm{d}}}}_{G_{\mathrm{PI}}(s)} \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)} = \underbrace{G^*_{\mathrm{PI}}(s) \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)}}_{T^*_{\mathrm{O}}(s)} e^{-sT_{\mathrm{d}}}, \tag{2.4}$$

where $G^*_{\mathrm{PI}}(s)$ and $T^*_{\mathrm{O}}(s)$ represent the delay-free part of interface $G_{\mathrm{PI}}(s)$ and open loop system $T_{\mathrm{O}}(s)$, respectively.

For analytical assessment and frequency-domain analysis, the time delay expressed in its equivalent Laplace transformer $e^{-sT_{\mathrm{d}}}$ can be further approximated by a rational model with Pade approximation formula [50]. Considering the trade-off between the ease of implementation and approximation accuracy, second-order

Pade approximation is employed in this chapter,

$$e^{-sT_\mathrm{d}} = \frac{\frac{{T_\mathrm{d}}^2}{12}s^2 - \frac{T_\mathrm{d}}{2}s + 1}{\frac{{T_\mathrm{d}}^2}{12}s^2 + \frac{T_\mathrm{d}}{2}s + 1}. \tag{2.5}$$

For digital implementation, continuous-time delay is expressed by delaying the uniformly sampled signal z^{-1} in the order of D [51] and the z-domain transfer function is in the form of,

$$H_\mathrm{d}(z) = z^{-D}, \tag{2.6a}$$

$$D = \frac{T_\mathrm{d}}{T_\mathrm{s}} = Int(D) + F, \tag{2.6b}$$

where D is the division of time delay T_d and sampling time T_s and can be expressed by the sum of integer part $Int(D)$ and fractional part F.

Based on the recursive duplication of linear Lagrange interpolation techniques, all-pass fractional delay Thiran filter [52] is utilised for the approximation of fractional delay F. Depending on the value of F, the transfer function of Thiran all-pass filter can be further expressed by,

$$H_\mathrm{d}(z) = \begin{cases} z^{-1}, & \text{if } Int(D) = 0, \quad F > 0, \\ z^{-D}, & \text{if } Int(D) \in R^+, F = 0, \\ \dfrac{\sum\limits_{k=0}^{N} h_k z^{-(N-k)}}{\sum\limits_{k=0}^{N} h_k z^{-k}}, & \text{if } Int(D) \in R^+, F > 0, \end{cases} \tag{2.7a}$$

$$h_{k(k=0,1,2,\ldots N)} = (-1)^k \binom{N}{k} \prod_{n=0}^{N} \frac{D - N + n}{D - N + k + n}, \tag{2.7b}$$

where N ($N = ceil(D)$) is the order of Thiran all-pass filter.

2.3 PHIL Stability

This section presents the PHIL system stability criteria and identifies the key determinants for the PHIL closed-loop stability. These are followed by analytical assessment of the identified PHIL stability determinants and a comprehensive and in-depth assessment of the PHIL stabilisation schemes in the literature.

2.3.1 Stability Criteria and Determinants

Based on the open-loop transfer function $T_{\mathrm{O}}(s)$ of the SISO closed-loop system in Figure 2.3, the system stability can be assessed by applying suitable stability criteria such as the Nyquist or the Routh–Hurwitz criterion [50] to the closed-loop system characteristic equation that is given by,

$$1 + T_{\mathrm{O}}(s) = 0. \tag{2.8}$$

As shown in Eq. (2.4) and Eq. (2.8), the closed-loop characteristic polynomial $(1 + T_{\mathrm{O}}(s))$ consists of the impedance, time delay and the delay-free power interface $G^{*}_{\mathrm{PI}}(s)$. The Gain Margin (GM) and Phase Margin (PM) are employed to determine the closed-loop stability from the open-loop transfer function [50]. Under the circumstance that GM and PM are positive, the PHIL stability is guaranteed provided that the magnitude and phase responses of the open-loop transfer function $T_{\mathrm{O}}(s)$ satisfy the following criteria,

$$\begin{cases} \mathrm{GM} &= 0 - 20log(|T_{\mathrm{O}}(j\omega_{\mathrm{cp}})|), \quad \mathrm{GM} > 0 \\ \mathrm{PM} &= \angle T_{\mathrm{O}}(j\omega_{\mathrm{cg}}) - (-180^{\circ}), \quad \mathrm{PM} > 0 \end{cases} \tag{2.9}$$

where ω_{cg} is the gain crossover frequency at which the magnitude of $T_{\mathrm{O}}(s)$ is 0 dB, ω_{cp} is the phase crossover frequency at which the phase of $T_{\mathrm{O}}(s)$ crosses -180°.

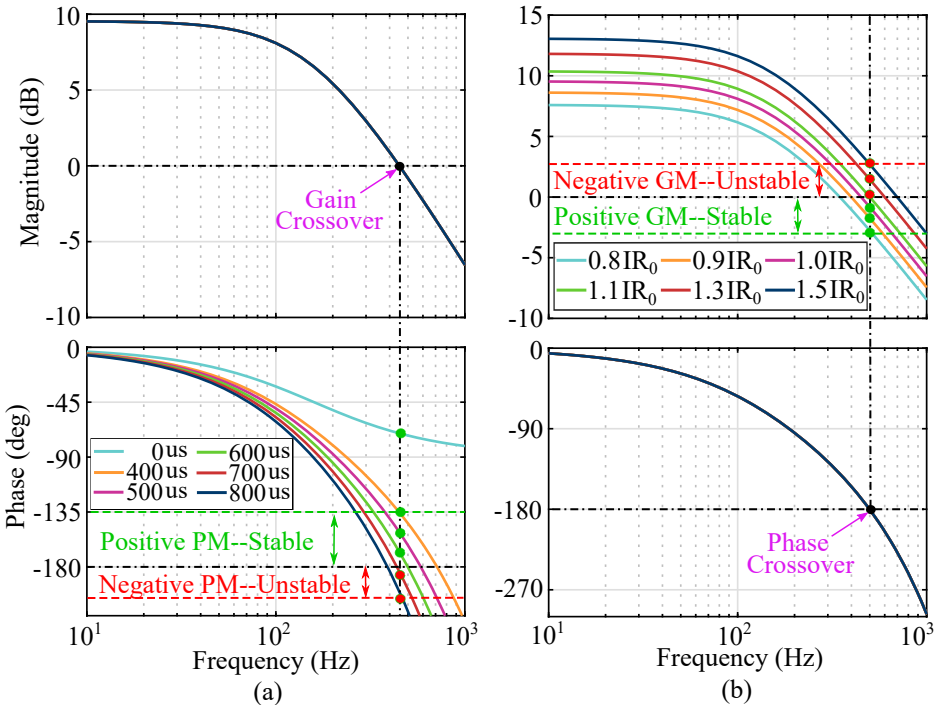

Figure 2.4: Bode plots of the open-loop transfer functions of PHIL system with unity $G^*_{\mathrm{PI}}(s)$ and (a) fixed IR ($\mathrm{IR}_0 = 3/(0.001s+1)$) and variable time delay, (b) fixed time delay ($T_{\mathrm{d}} = 600us$) and variable IR.

The delay-free power interface $G^*_{\mathrm{PI}}(s)$, aggregated time delay, and the equivalent impedance of the simulation and hardware side in Eq. (2.4) and Eq. (2.8) are the key determinants in guaranteeing the stability criteria in Eq. (2.9). The impact of these key determinants on the PHIL system stability are elaborated as follows:

- Delay-free power interface $G^*_{\mathrm{PI}}(s)$

  With more advanced power amplifiers being made available in the market, the precise modelling of the off-the-shelf power amplifier comprising subsystems (as in Eq. (2.2)) and the signal conversion cards (i.e., ADC and DAC) is feasible in a laboratory environment. Correspondingly, the delay-free part $G^*_{\mathrm{PI}}(s)$ in the power interface (as in Eq. (2.4)) serves as an invariant part in determining the PHIL stability.

- Time delay

  As shown in Figure 2.4(a), the frequency response of the time delay presents unity magnitude but introduces additional phase lag. Phase margin (PM) measures the system stability tolerance to the time delay and the stability can only be guaranteed provided that PM is large than zero and the corresponding phase response should satisfy the following criteria,

$$\begin{cases} \text{GM} = \left| G^*_{\text{PI}}(jw_{cg}) \frac{Z_{\text{S}}(jw_{cg})}{Z_{\text{H}}(jw_{cg})} e^{-jw_{cg}T_{\text{d}}} \right| = 1, \\ \text{PM} = \angle \left[G^*_{\text{PI}}(jw_{cg}) \frac{Z_{\text{S}}(jw_{cg})}{Z_{\text{H}}(jw_{cg})} e^{-jw_{cg}T_{\text{d}}} \right] + 180^\circ > 0, \end{cases} \tag{2.10}$$

  where w_{cg} is the gain crossover frequency at which the magnitude of open-loop transfer function is equal to 1 (0 dB).

  Since time delay has no effect on the magnitude of the input signal so does the gain crossover frequency [50]. However, as shown in Eq. (2.10), the phase lag caused by the time delay significantly degrades system stability as a result of the reduced phase margin. Accordingly, given that the PHIL system with fixed impedance, the time delay destabilises the PHIL system once it exceeds a critical limit T_{dc}, which is defined as,

$$\text{PM} = \angle \left[G^*_{\text{PI}}(jw_{cg}) \frac{Z_{\text{S}}(jw_{cg})}{Z_{\text{H}}(jw_{cg})} e^{-jw_{cg}T_{\text{dc}}} \right] + 180^\circ = 0. \tag{2.11}$$

- Software and hardware side impedance

  Due to the phase lag introduced by the time delay, the PHIL system stability is more susceptible to the system impedance variance than that of a delay-free PHIL system. Even when the time delay is within the critical limit as identified in Eq. (2.11), as shown in Figure 2.4(b), the closed-loop stability can only be maintained for certain Impedance Ratio (IR), where IR = $\frac{Z_{\text{S}}}{Z_{\text{H}}}$. The smaller the magnitude ratio is, the more stable the system will

be. On the other hand, the gain margin of the PHIL system is a factor by which the impedance ratio can be raised before breaching the system stability. Accordingly, given that the PHIL system with fixed time delay, the impedance ratio destabilises the PHIL system once it exceeds a critical limit $\mathrm{IR_C}$ ($\mathrm{IR_C} = \frac{Z_\mathrm{S}(jw_{cp})}{Z_\mathrm{H}(jw_{cp})}$), which is defined as,

$$\mathrm{GM} = \left| G^*_\mathrm{PI}(jw_{cp}) \frac{Z_\mathrm{S}(jw_{cp})}{Z_\mathrm{H}(jw_{cp})} e^{-jw_{cp}T_\mathrm{d}} \right| = 1. \tag{2.12}$$

This rigorous impedance ratio constraint in maintaining a stable PHIL system presents a significant limitation in the realisation of PHIL setups as in real-world applications the impedances in the simulation and hardware sides witness significant variations.

The above identified key determinants including the delay-free power interface $G^*_\mathrm{PI}(s)$ and time delay that are not exist in original system of interest and the impedance ratio between the software and hardware side play a significant role in determining the PHIL system stability.

2.3.2 PHIL Stability Enhancement Scheme

To mitigate the destabilisation impact of the identified key determinants on the PHIL closed-loop stability, many research efforts have been devoted to improving the stability of a PHIL system either by decreasing the impedance ratio between the software and hardware side or by improving the system stability margin through augmenting the power interface with compensation schemes.

The stabilisation scheme involving decreasing the impedance ratio between the software and hardware side includes advanced ideal transformer method [53], impedance shifting method [54], and hardware inductance addition method [55, 56]. The design principles, advantages and limitation of these stability en-

hancement schemes are summarised as follows:

- Advanced ideal transformer method [53].

  The advanced ideal transformer method was designed by connecting compensation capacitance in parallel with the controllable current source (as shown in Figure 2.2) in the simulation side. This decreases the equivalent impedance in the simulation side and the impedance ratio between the simulation and hardware side, thus improving the PHIL closed-loop stability margin. Owing to the implementation of compensation shunt capacitance, a proper compensation for the controlled current source is required to guarantee the voltage output of the DRTS platform is equivalent to that of the original PHIL system.

- Impedance shifting method [54].

  To degrade the impedance ratio between the simulation side and hardware side, the impedance shifting method was implemented by reducing part of the simulation side impedance and shifting this to the hardware side by inserting a physical impedance. From the control point of view, this shifted impedance changes the zero and pole locations of the transfer function in Eq. (2.4) with the former being much further from the imaginary axis and the later being much closer to the imaginary axis in the Left Half-Plane (LHP). However, by doing so, the accuracy of the experiment is significantly deteriorated as it is not equivalent to the original SoI. Furthermore, this compensation scheme requires additional physical inductance, which increases the overall testing expense.

- Hardware inductance addition method [55, 56].

  Motivated by decreasing the impedance ratio between the software and hardware side, this method was proposed to increase the equivalent hard-

ware side impedance through inserting additional cascaded inductance to the HuT. However, by doing so, the PHIL system stability margin is improved at the expense of distorting the original PHIL topology, which leads to inaccurate simulation. Furthermore, this compensation scheme requires additional physical inductance, which increases the overall testing expense.

On the other hand, the PHIL stability enhancement schemes realised by improving system stability margin without changing system impedance include the feedback current filtering [56, 57], multi-rate partitioning interface [56, 58], Bergeron transmission line model based multi-time-step interface [27], open-loop inverter based interface [32, 59], spectrum assignment based interface [34], and robust data-driven controller [60]. The design principles, merits and limitations of these PHIL stability enhancement schemes are summarised as follows:

- Feedback current filtering method [56, 57].

  As illustrated in Figure 2.2, a first-order low-pass filter can be deployed in PHIL feedback path to mitigate the high-frequency noise of current measurement. On the other hand, the implementation of this filter with a low cut-off frequency extends the stability margins to the PHIL closed-loop system. However, setting the cut-off frequency of the low-pass filter is a trade-off between realising improved stability margin whilst minimizing the deterioration of accuracy. The low-pass filter also significantly limits the PHIL system bandwidth if a relatively low cut-off frequency is selected to stabilise a marginally unstable or absolutely unstable PHIL system.

- Multi-rate partitioning (multi-time-step) interface [27, 56, 58].

  Thanks to the remarkable computation capability of modern real-time computation platforms, multi-rate partitioning interface was proposed to divide the original PHIL system into some dedicated fast subsystems with small

time-steps. The introduction of multiple fast subsystems with multi-time-step can not only extend the system bandwidth but also improve the system stability significantly by reducing the equivalent time delay in the PHIL system. However, this method requires advanced multi-core real-time simulation platforms, and the fidelity depends on the dynamic coupling and clock synchronisation between all subsystems.

- Open-loop inverter based interface [32, 59].

  An open-loop controlled Voltage Source Inverter (VSI) without output filter was proposed for being the power amplifier in a PHIL setup. Compared with the conventional closed-loop controlled voltage source converter, the proposed open-loop VSI presents less time delay associated with sampling and computation. The eliminated time delay can improve the stability margin, as demonstrated in Figure 2.4(a), and enhance the PHIL stability. Even this open-loop VSI based power amplifier improves the PHIL stability, offers higher bandwidth than the closed-loop controlled power amplifier, its only applicable for the significantly inductive HuT.

- Spectrum assignment based interface [34].

  A delay differential equations based stability analysis method was proposed in [34], based on which spectrum assignment was leveraged to enhance the ITM-based PHIL setup. The spectrum assignment was achieved by implementing a system state feedback of the hardware side voltage to manipulates the input of power interface. The adjunctive state feedback voltage to the controlled input voltage source of power interface add its derivative to the system state, which paved a new pathway to shift certain critical spectrum's infinite roots to the left half complex plane. This enables the PHIL system being equivalent to a delay-free system and stability enhancement can be achieved without full knowledge of the hardware impedance.

Table 2.2: Comparison of PHIL stabilisation schemes regarding stability, accuracy, and ease of implementation.

Stabilisation scheme	**Stability**	**Accuracy**	**Ease of Implementation**
Advanced ITM interface [53]	Low	Medium	High
Impedance shifting method [54]	High	Medium	Medium
Hardware inductance addition [55, 56]	High	Low	Low
Feedback-path current filtering [56, 57]	Medium	Medium	High
Spectrum assignment based interface [34]	High	Medium	Medium
Open-loop inverter based interface [32, 59]	Medium	High	Medium
Multi-rate partitioning Interface [27, 56, 58]	High	High	Low
Robust data-driven controller compensation [60]	Medium	Medium	Medium

- Robust data-driven controller compensation method [60].

  A data-driven controller design methodology utilising convex optimisation criteria was employed to tune the PHIL feedback current low-pass filter such that the PHIL system stability enhancement is achieved. With the norms of the difference between controller based interface and ideal unity interface accounted as the objective function to be optimized, the filter is designed in discrete-time domain and tuned by optimizing the objective function with the pre-defined PHIL stability constraints were satisfied. This data-driven based filter design method can enhance the PHIL stability without requiring a full knowledge of the hardware parameters and also offers the PHIL system with enhanced accuracy and disturbance rejection capability.

In summary, the proposed methods in literature realise stable PHIL setups by redefining the impedance ratio at the point of common coupling, by manipulation of interface signals, or by using novel interfacing components and compensation schemes. Apart from their design principles, merits and limitations, their performances regarding the stability, accuracy, and ease of implementation are given in Table 2.2 by using the predefined criteria Low/Medium/High in Chapter 2.2.1.

2.4 PHIL Accuracy

This section presents an analysis of the PHIL system accuracy from the aspects of the deviation between PHIL system and original SoI, the power signal synchronisation and power transfer transparency within the PHIL closed-loop setup. Furthermore, accuracy metrics are developed for the transient and steady-state accuracy assessment.

2.4.1 PHIL Accuracy Analysis

An ideal ITM interface is delay-free and has transparent power amplification with unity-gain and infinite bandwidth. Under such conditions, the PHIL system is equivalent to the system of interest (SoI) as duplicated in Figure 2.1(a) and the closed-loop transfer function between the hardware side voltage $V_{\mathrm{H}}(s)$ and the equivalent software side voltage source $V_{\mathrm{S}}(s)$ of such an ideal PHIL setup is,

$$T_{\mathrm{C}}^{\mathrm{id}}(s) = \frac{V_{\mathrm{H}}}{V_{\mathrm{S}}} = \frac{Z_{\mathrm{H}}(s)}{Z_{\mathrm{S}}(s) + Z_{\mathrm{H}}(s)}. \tag{2.13}$$

However, the closed-loop transfer function that is related to the hardware side voltage $V_{\mathrm{H}}(s)$ and the software side voltage $V_{\mathrm{S}}(s)$ of the actual PHIL setup with non-ideal interface is given by,

$$T_{\mathrm{C}}(s) = \frac{V_{\mathrm{H}}}{V_{\mathrm{S}}} = \frac{G_1(s)G_2(s)}{1 + T_{\mathrm{O}}(s)}. \tag{2.14}$$

For a given signal (e.g., $V_{\mathrm{H}}(s)$), its accuracy can be quantitatively analysed by assessing the deviation between the closed-loop transfer functions of the ideal PHIL and the actual PHIL through the relative error $\epsilon(s)$ defined as,

$$\epsilon(s) = \left| \frac{T_{\mathrm{C}}(s) - T_{\mathrm{C}}^{\mathrm{id}}(s)}{T_{\mathrm{C}}^{\mathrm{id}}(s)} \right|. \tag{2.15}$$

Based on the detailed modelling of SoI system and PHIL system, the accuracy of PHIL system can be analytically assessed in a quantitative manner through employing the relative error $\epsilon(s)$. This is critical for the system operator to design and tune the PHIL system prior to its final deployment.

On the other hand, owing to the non-unity magnitude of the power interface component and the phase lag arising from the aggregated time delay as defined in Eq. (2.3), the phase and magnitude relationship between V_{S} and V_{H} of the actual PHIL system are not aligned with that defined in Eq. (2.13). This discrepancy not only leads to the inaccurate power signal synchronisation between the simulation side and hardware side, but also deteriorates the current response at the simulation side and hardware side. Being proportional to the frequency of input power signal, the phase shift stemming from the time delay and the non-unity magnitude characteristic of the power interface distorts the phase relationship between the voltage and current. Consequently, this leads to deteriorated Power Factor (PF) angle and inaccurate power transfer between DRTS platform and hardware.

Provided a PHIL interface is an ideal one that presents unity magnitude and zero phase lag, the apparent power transferred between the simulation side ($S_{\mathrm{S}'}$) and hardware (S_{H}) over a certain frequency w_k are,

$$\begin{cases} S_{\mathrm{S}'} = & |V_{\mathrm{S}'} I_{\mathrm{S}}| \angle\theta_{\mathrm{S}'} & = & P_{\mathrm{S}'} + jQ_{\mathrm{S}'}, \\ S_{\mathrm{H}} = & |V_{\mathrm{H}} I_{\mathrm{H}}| \angle\theta_{\mathrm{H}} & = & P_{\mathrm{H}} + jQ_{\mathrm{H}}, \\ = & |V_{\mathrm{S}'} I_{\mathrm{S}}| \angle\theta_{\mathrm{H}} & = & P_{\mathrm{S}'} + jQ_{\mathrm{S}'}, \end{cases} \tag{2.16}$$

where $\theta_{\mathrm{S}'}$ is PF angle at the simulation side (i.e., $\angle V_{\mathrm{S}'} - \angle I_{\mathrm{S}}$), θ_{H} is PF angle at the hardware side (i.e., $\angle V_{\mathrm{H}} - \angle I_{\mathrm{H}}$), and $\theta_{\mathrm{S}'} = \theta_{\mathrm{H}}$.

For an actual PHIL interface with a variety of interfacing components as presented in Figure 2.2, it presents non-unity magnitude and negative phase char-

acteristics over a certain frequency w_k, the actual voltage $\hat{V}_{\mathrm{H}}$ and current $\hat{I}_{\mathrm{H}}$ at hardware side with respect to the actual voltage $\hat{V}_{\mathrm{S}'}$ and current $\hat{I}_{\mathrm{S}}$ at simulation side are,

$$\begin{cases} \hat{V}_{\mathrm{H}}(w_k) = G_1(w_k)G_2(w_k)\hat{V}_{\mathrm{S}'}(w_k) = |G_1(w_k)G_2(w_k)| \left|\hat{V}_{\mathrm{S}'}(w_k)\right| \angle\alpha, \\ \hat{I}_{\mathrm{H}}(w_k) = G_3(w_k)G_4(w_k)\hat{I}_{\mathrm{S}}(w_k) = |G_3(w_k)G_4(w_k)| \left|\hat{I}_{\mathrm{S}}(w_k)\right| \angle\beta, \end{cases} \tag{2.17a}$$

$$\begin{cases} \angle\hat{V}_{\mathrm{H}} = \angle\alpha = \angle[G_1(w_k)G_2(w_k)] + \angle\hat{V}_{\mathrm{S}'}, \\ \angle\hat{I}_{\mathrm{H}} = \angle\beta = \angle[G_3(w_k)G_4(w_k)] + \angle\hat{I}_{\mathrm{S}}. \end{cases} \tag{2.17b}$$

Substituting Eq. (2.2) and Eq. (2.3) into Eq. (2.17b), the phase angles in Eq. (2.17) are further expressed as,

$$\begin{cases} \angle\hat{V}_{\mathrm{H}} = \angle[G_1(w_k)G_2(w_k)] + \angle\hat{V}_{\mathrm{S}'} = \angle(\frac{1}{\frac{jw_k}{2\pi f_{c2}}+1}) - w_k T_{\mathrm{d-ff}} + \angle\hat{V}_{\mathrm{S}'}, \\ \angle\hat{I}_{\mathrm{H}} = \angle[G_3(w_k)G_4(w_k)] + \angle\hat{I}_{\mathrm{S}} = \angle(\frac{1}{\frac{jw_k}{2\pi f_{c4}}+1}) - w_k T_{\mathrm{d-fb}} + \angle\hat{I}_{\mathrm{S}}. \end{cases} \tag{2.18}$$

The difference ($\angle\varphi$) between the power factor angle at the hardware (i.e., $\hat{\theta}_{\mathrm{H}} = \angle\hat{V}_{\mathrm{H}} - \angle\hat{I}_{\mathrm{H}}$) and the power factor angle at the simulation side (i.e., $\hat{\theta}_{\mathrm{S}'} = \angle\hat{V}_{\mathrm{S}'} - \angle\hat{I}_{\mathrm{S}}$) is given by,

$$\angle\varphi = \hat{\theta}_{\mathrm{H}} - \hat{\theta}_{\mathrm{S}'} = (\angle\hat{V}_{\mathrm{H}} - \angle\hat{V}_{\mathrm{S}'}) + (\angle\hat{I}_{\mathrm{S}} - \angle\hat{I}_{\mathrm{H}}). \tag{2.19}$$

Substituting Eq. (2.18) into Eq. (2.19), the power factor angle difference $\angle\varphi$ is further expressed as,

$$\angle\varphi = \angle(\frac{1}{\frac{jw_k}{2\pi f_{c2}}+1}) - \angle(\frac{1}{\frac{jw_k}{2\pi f_{c4}}+1}) - w_k(T_{\mathrm{d-ff}} - T_{\mathrm{d-fb}}). \tag{2.20}$$

The apparent power at simulation side and hardware side are expressed as,

$$\begin{cases} \hat{S}_{\mathrm{S}'} = \left|\hat{V}_{\mathrm{S}'}\hat{I}_{\mathrm{S}}\right| \angle\hat{\theta}_{\mathrm{S}'} = \hat{P}_{\mathrm{S}'} + j\hat{Q}_{\mathrm{S}'}, \\ \hat{S}_{\mathrm{H}} = \left|\hat{V}_{\mathrm{H}}\hat{I}_{\mathrm{H}}\right| \angle\hat{\theta}_{\mathrm{H}} = \hat{P}_{\mathrm{H}} + j\hat{Q}_{\mathrm{H}}. \end{cases} \tag{2.21}$$

Substituting Eq. (2.17a) into Eq. (2.21), the apparent power at simulation side and hardware side are further expressed as,

$$\begin{cases} \hat{S}_{\mathrm{S}'} = \left|\hat{V}_{\mathrm{S}'}(w_k)\right| \left|\hat{I}_{\mathrm{S}}(w_k)\right| \angle\hat{\theta}_{\mathrm{S}'} = \hat{P}_{\mathrm{S}'} + j\hat{Q}_{\mathrm{S}'}, \\ \hat{S}_{\mathrm{H}} = \underbrace{|G_1(w_k)G_2(w_k)G_3(w_k)G_4(w_k)|}_{|G_{\mathrm{PI}}(s)|} \left|\hat{V}_{\mathrm{S}'}(w_k)\right| \left|\hat{I}_{\mathrm{S}}(w_k)\right| \angle\hat{\theta}_{\mathrm{H}} = \hat{P}_{\mathrm{H}} + j\hat{Q}_{\mathrm{H}}. \end{cases} \tag{2.22}$$

Substituting Eq. (2.19) into Eq. (2.22), the active and reactive power at the hardware side can be further expressed as,

$$\begin{cases} \hat{P}_{\mathrm{H}} = |G_{\mathrm{PI}}(s)|(\hat{P}_{\mathrm{S}'}cos\varphi - \hat{Q}_{\mathrm{S}'}sin\varphi), \\ \hat{Q}_{\mathrm{H}} = |G_{\mathrm{PI}}(s)|(\hat{Q}_{\mathrm{S}'}cos\varphi + \hat{P}_{\mathrm{S}'}sin\varphi). \end{cases} \tag{2.23}$$

It is evident from Eq. (2.23) that the actual power transfer within the PHIL setup is not aligned with the power transfer defined in Eq. (2.16). This difference results from the non-unity magnitude $|G_{\mathrm{PI}}(w_k)|$ and the phase lag φ stemming from the power amplifier output filter, the signal processing unit (i.e., low-pass filter), and the aggregated loop time delay. These distort the transparent power transfer between the simulation side and hardware side.

2.4.2 PHIL Accuracy Assessment Metrics

Beyond the PHIL interface optimisation and stabilisation stage, rigorous accuracy assessment of final-stage PHIL experimental results is of great significance. Having identified the impact of power interface non-idealities on PHIL system signal synchronisation and power transfer transparency, appreciate metrics are essential for quantifying these PHIL accuracy properties. The following two metrics are proposed to quantify the steady-state and transient PHIL accuracy.

- **Steady-state accuracy metrics**

  The simulation side voltage signal $\hat{V}_{\mathrm{S}'}$ that is to be amplified by the power amplifier, the voltage signal $\hat{V}_{\mathrm{H}}$ at the hardware side, the power factor angle ($\hat{\theta}_{\mathrm{S}'}$ and $\hat{\theta}_{\mathrm{H}}$) at simulation side and hardware side, the active power ($\hat{P}_{\mathrm{S}'}$ and $\hat{P}_{\mathrm{H}}$) and reactive power ($\hat{Q}_{\mathrm{S}'}$ and $\hat{Q}_{\mathrm{H}}$) at simulation and hardware side are employed to assess the PHIL system accuracy. Accuracy metrics are defined by the relative average error η to quantify the discrepancy between the power signal of the PHIL setup with respect to that of original system of interest. The relative error is given by,

$$\eta_x = \frac{\epsilon_x}{|x_{\mathrm{ref}}|} = \frac{|\hat{x} - x_{\mathrm{ref}}|}{|x_{\mathrm{ref}}|}, \tag{2.24}$$

  where $\hat{x}$ is the power signal within the PHIL setup, x_{ref} is the reference power signal in the system of interest. x refers to the voltage signal, power factor angles, active and reactive power within the PHIL setup and original system of interest.

  On the other hand, the power signal tracking error metrics are proposed to quantitatively assess the power signal distortion and the power transfer transparency between simulation side and hardware side at steady-state.

The power signal tracking error metrics are given by,

$$\begin{cases} \text{Voltage tracking error} \quad \eta_{VT} = \frac{\left|\hat{V}_{\mathrm{H}} - \hat{V}_{\mathrm{S}'}\right|}{\left|\hat{V}_{\mathrm{S}'}\right|}, \\ \text{Active power tracking error} \quad \eta_{PT} = \frac{\left|\hat{P}_{\mathrm{H}} - \hat{P}_{\mathrm{S}'}\right|}{\left|\hat{P}_{\mathrm{S}'}\right|}, \\ \text{Reactive power tracking error} \quad \eta_{QT} = \frac{\left|\hat{Q}_{\mathrm{H}} - \hat{Q}_{\mathrm{S}'}\right|}{\left|\hat{Q}_{\mathrm{S}'}\right|}, \\ \text{Power factor angle tracking error} \quad \eta_{\theta T} = \frac{\left|\hat{\theta}_{\mathrm{H}} - \hat{\theta}_{\mathrm{S}'}\right|}{\left|\hat{\theta}_{\mathrm{S}'}\right|}. \end{cases} \tag{2.25}$$

- **Transient state accuracy metrics**

  Maximum Instantaneous Power Tracking Error (MIPTE): The maximum instantaneous active and reactive power are measured at the Point of Common Coupling (PCC) once the PHIL feedback loop is completed. This metric will therefore take all the dynamics of power interface and the delays from the feed forward and feedback loops into account. The MIPTE metrics are defined as maximum deviation between the measured power at the PCC of the actual PHIL system and that of the monolithic system of interest and are given by,

$$\begin{cases} \mathrm{MIPTE}_{\mathrm{P}_{\mathrm{S}'}} = \max\left(\frac{P_{\mathrm{S}'}(t) - P'_{\mathrm{S}'}(t)}{[P_{\mathrm{S}'}(t)]_{\mathrm{RMS}}}\right), \\ \mathrm{MIPTE}_{\mathrm{Q}_{\mathrm{S}'}} = \max\left(\frac{Q_{\mathrm{S}'}(t) - Q'_{\mathrm{S}'}(t)}{[Q_{\mathrm{S}'}(t)]_{\mathrm{RMS}}}\right), \end{cases} \tag{2.26}$$

  where $P_{\mathrm{S}'}(t)$ and $Q_{\mathrm{S}'}(t)$ are the active power and reactive power of the monolithic system of interest, respectively. $P'_{\mathrm{S}'}(t)$ and $Q'_{\mathrm{S}'}(t)$ are the active power and reactive power of the actual PHIL system, respectively.

These accuracy metrics are crucial for PHIL accuracy assessment and will be further leveraged for the compensation schemes validation in the rest chapters.

2.5 Summary

This chapter presented the state-of-the-art of PHIL systems and identified the key challenges in realising a stable PHIL closed-loop simulation with high fidelity. These are followed by detailed PHIL system modelling regarding its architecture, interface algorithm, mathematical modelling of key components and equivalent system transfer functions.

Significant emphasis has been placed on the analysis of PHIL closed-loop stability. The key determinants for PHIL closed-loop stability have been identified and their impacts on PHIL stability have been analytically assessed. Following on this, the novel PHIL stability enhancement schemes involving modifying the impedance ratio between simulation side and hardware side and implementing compensation schemes to improve system stability margins have been reviewed. The review of a variety of PHIL stabilisation schemes in relevant literature along with their design principles, advantages and limitations reveal that there are ongoing research activities towards bridging the research gap in developing state-of-the-art compensation schemes for enhancing the PHIL closed-loop stability without deteriorating its accuracy.

In addition, the detrimental impact of PHIL interface on the signal synchronisation and power transfer transparency has been analysed. This justifies the development of compensation scheme for improving PHIL accuracy as one of the main contributions of this thesis. Accuracy metrics were proposed for quantitatively assessing PHIL accuracy and verifying the proposed compensation methodologies in the following chapters. These are of great value in providing a means to quantify simulation accuracy on a common basis for the PHIL community.

The detailed modelling and PHIL stability and accuracy analysis in this chapter will contribute to the development of PHIL stability and accuracy enhancement schemes in this thesis by establishing theoretical foundations.

Chapter 3

Adaptive Smith Predictor for PHIL Stability Enhancement

The stability and accuracy of power hardware-in-the-loop (PHIL) setups are sensitive to and deteriorated by the dynamics and non-ideal characteristics of their power interfaces, such as time delay, noise perturbation, and signal distortion. As analysed in Chapter 2.3, from the control point of view, the PHIL closed-loop stability is mainly determined by the time delay stemming from the power interface and the equivalent impedance ratio between software and hardware side. The impact of varying impedance ratio between simulation side and hardware side on the PHIL stability has been well-analysed and assessed in [33–35, 61, 62] and the PHIL stability is strictly constrained by this impedance ratio. Such a stringent impedance ratio constraint is not always ensured in practice due to the impedance variations of the emulated power network and hardware components during an experimental scenario run.

The literature review of the PHIL stabilisation schemes in Chapter 2.3 has revealed that there is a growing tendency for developing novel stabilisation scheme to mitigate the impact of non-ideal power interface on PHIL stability without deteriorating the simulation accuracy. Although the proposed stabilisation methods

(as summarised in Chapter 2.3) in the literature realise stable PHIL setups by re-defining the impedance ratio at the point of common coupling or by manipulating the interface signals. These method are either limited by the availability of proper physical impedance [54, 56] and the deteriorated simulation accuracy [53–56], or their performances are deteriorated by the limited bandwidth [56,57], or depended on the dynamic coupling and clock synchronisation between subsystems with different time-steps [27, 56, 58]. Furthermore, these methods are passive, i.e., only applicable to the setup for which they are designed and any hardware or software impedance variation may lead the system to instability.

Considering the aforementioned limitations, inspired by the Smith predictor criterion applied in [31, 63–66], this chapter presents an adaptive Smith predictor based PHIL stabilisation scheme that presents high robustness to the variations of system impedance. The main contributions of this proposed method are summarised as follows,

1. A Smith predictor criterion inspired compensator is designed to mitigate the negative impact of the time delay on PHIL closed-loop stability. Although a passive approach, this passive compensator introduces a buffer in the variability of impedance and enables a stable PHIL experiment over a wider range of scenarios.

2. Robustness analysis of the passive compensator against the modelling error stemming from system impedance variation is presented and the stability constraint of the passive compensator-based PHIL system is defined.

3. To enhance the robustness of compensator and overcome the limitation of passive approaches, an adaptive Smith predictor compensator based on a computationally efficient online impedance parameter identification technique is proposed. The accurate impedance identification allows the parameters of Smith predictor compensator being adapted in real-time to

ensure seamless operation catering to any variations in impedance during the experimental run.

The remainder of this chapter is organized as follows: Section 3.1 presents the in-depth design criteria of the Smith predictor compensator along with its robustness analysis and stability constraints definition. In Section 3.2, the online SDFT and vector-fitting based impedance identification method are presented and its functionality in equipping the proposed compensator with adaptivity to system impedance variation is elaborated. Analytical assessments of the proposed compensation scheme are presented in Section 3.3, followed by its experimental validation in Section 3.4. In-depth discussions are presented in Section 3.5. Section 3.6 concludes the chapter[1].

3.1 Smith Predictor Based Stability Enhancement Scheme

This section describes the design criterion and the functionality of Smith predictor compensator, analyses the impact of modelling errors on the robustness of proposed Smith predictor compensator, and defines the stability constraints of the Smith predictor aided PHIL setups.

3.1.1 Smith Predictor Design Criteria

Smith predictor based predictive control, an effective time-delay compensation scheme, has been extensively employed for power system control [63, 67], power converters control [64, 65], microgrid hierarchical control [66], etc. As shown in Figure 3.1, inspired by the Smith predictor design criterion in [63–67], a model based compensator $C_{eq}(s)$ is designed and implemented in the feed forward path

[1] This chapter is an extension of a conference publication [31] and journal publication [42].

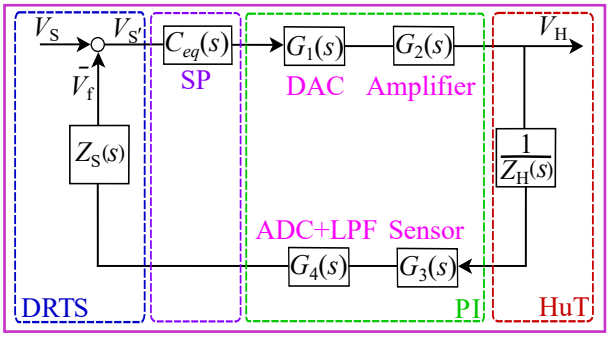

Figure 3.1: Equivalent PHIL diagram with Smith predictor compensator.

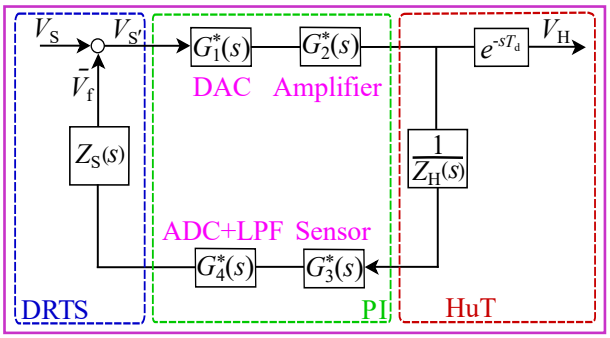

Figure 3.2: Equivalent PHIL system with shifted time delay in the open-loop.

in the PHIL closed-loop setup, whose closed-loop transfer function is given by,

$$T_{\mathrm{C}}^{1}(s) = \frac{C_{eq}(s)G_1(s)G_2(s)}{1 + C_{eq}(s)G_1(s)G_2(s)G_3(s)G_4(s)\frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)}}. \tag{3.1}$$

Substituting Eq. (2.4) into Eq. (3.1), the closed-loop transfer function of the Smith predictor-based PHIL setup in Figure 3.1 is further expressed as,

$$T_{\mathrm{C}}^{1}(s) = \frac{C_{eq}(s)G_1(s)G_2(s)}{1 + C_{eq}(s)T_{\mathrm{O}}^{*}(s)e^{-sT_{\mathrm{d}}}}. \tag{3.2}$$

Figure 3.2 presents the equivalent PHIL diagram with time delay shifted in the open-loop, whose closed-loop transfer function is,

$$T_{\mathrm{C}}^{2}(s) = \frac{G_1^*(s)G_2^*(s)}{1 + G_1^*(s)G_2^*(s)G_3^*(s)G_4^*(s)}e^{-sT_{\mathrm{d}}} = \frac{G_1^*(s)G_2^*(s)}{1 + T_{\mathrm{O}}^{*}(s)}e^{-sT_{\mathrm{d}}}. \tag{3.3}$$

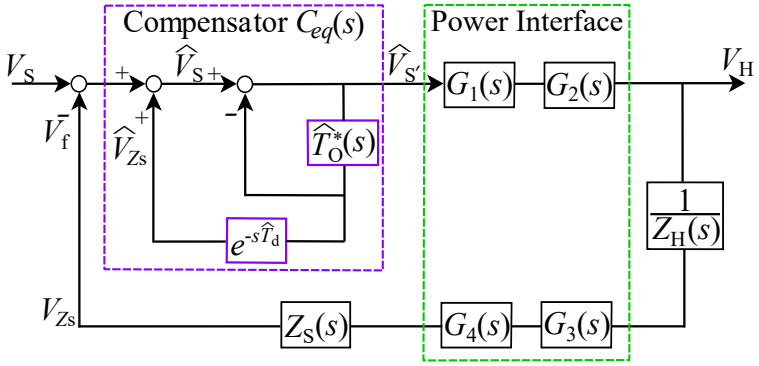

Figure 3.3: Equivalent PHIL diagram with detailed structure of Smith predictor compensator.

The transfer function of Smith predictor compensator is derived by setting the equivalence between the systems in Figure 3.1 and Figure 3.2 (i.e., $T_C^1(s)$=$T_C^2(s)$), which yields,

$$C_{eq}(s) = \frac{1}{1 + \widehat{T}_O^*(s)(1 - e^{-s\widehat{T}_d})}, \tag{3.4}$$

where $\widehat{T}_O^*(s)$ and $\widehat{T}_d$ are the estimation of the nominal delay-free model $T_O^*(s)$ and the aggregated delay T_d, respectively. As presented in [30], the time delay within the PHIL setup presents a relatively small variation with respect to its average value. Note that, the maximum time delay is used when designing the Smith predictor to ensure its effectiveness in fully mitigating time delay.

An illustration of the Smith predictor compensator is enclosed in the dashed block (purple) in Figure 3.3, the Smith predictor compensator is implemented at the point of common coupling in the feed-forward path to process the output signal from DRTS before it is amplified by the power amplifier. By implementing this compensator, the closed-loop transfer function between V_S and V_H is,

$$T_C(s) = \frac{G_1(s)G_2(s)}{1 + \left[T_O^*(s)e^{-sT_d} + \widehat{T}_O^*(s)(1 - e^{-s\widehat{T}_d})\right]}. \tag{3.5}$$

Assuming the time delay and the system model are estimated precisely, namely

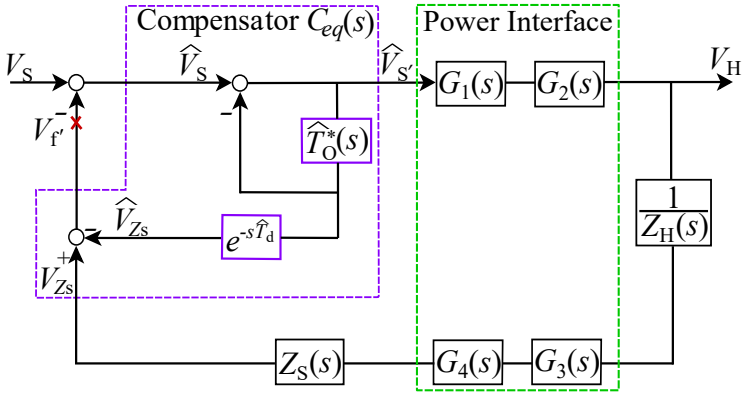

Figure 3.4: Theoretical equivalence of the diagram in Figure 3.3.

$\widehat{T}_d = T_d$ and $\widehat{T}_O^*(s) = T_O^*(s)$, the closed-loop transfer function in Eq. (3.5) is the same as that in Eq. (3.3). It is clear from Eq. (3.3) that the characteristic equation of the Smith predictor compensator-based PHIL setup excludes the time delay, thereby enhancing the system stability. Note that with accurate estimations of $\widehat{T}_O^*(s)$ and $\widehat{T}_d$, as shown in Figure 3.4, the estimated output $\widehat{V}_{Z_S}$ of the Smith predictor is equal to the actual feedback signal V_f (i.e., the actual voltage drop V_{Z_S} of the impedance Z_S). The voltage signal $\widehat{V}_S$ applied to the inner loop of the Smith predictor and the actual voltage $\widehat{V}_{S'}$ applied to the power interface are,

$$\begin{cases} \widehat{V}_S = V_S + \widehat{V}_{Z_S} - V_f = V_S, \\ \widehat{V}_{S'} = \frac{\widehat{V}_S}{1+T_O^*(s)} = \frac{V_S}{1+T_O^*(s)}. \end{cases} \tag{3.6}$$

Accordingly, the compensator outputs a delay-free signal $\widehat{V}_{S'}$ to the power interface. Figure 3.4 presents the equivalent diagram of Figure 3.3, from the control point of view, the estimated output $\widehat{V}_{Z_S}$ of the compensator counteracts the actual voltage drop V_{Z_S} of the impedance Z_S and results in a virtual zero feedback signal $V_{f'}$. This enables an equivalent open-loop system operation through injecting a delay-free input to the power interface, thus mitigating the simulation error and destabilisation impact stemming from the time delay.

3.1.2 Robustness Analysis of Smith Predictor

Assuming $\delta T_{\mathrm{O}}^{*}(s)$ as the error between the estimation $\widehat{T}_{\mathrm{O}}^{*}(s)$ and the actual $T_{\mathrm{O}}^{*}(s)$, the estimation model is represented as,

$$\widehat{T}_{\mathrm{O}}^{*}(s) = T_{\mathrm{O}}^{*}(s) + \delta T_{\mathrm{O}}^{*}(s). \tag{3.7}$$

The error in estimation is attributed to the imprecise modelling of the power interface and the variations in the HuT and DRTS impedances. Substituting Eq. (3.7) into Eq. (3.5), the closed-loop transfer function of the PHIL setup can be written as,

$$T_{\mathrm{C}}(s) = \frac{V_{\mathrm{H}}(s)}{V_{\mathrm{S}}(s)} = \frac{G_1(s)G_2(s)}{1 + T_{\mathrm{O}}^{*}(s) + \delta T_{\mathrm{O}}^{*}(s)(1 - e^{-sT_{\mathrm{d}}})}. \tag{3.8}$$

Accordingly, the system characteristic equation is given by,

$$1 + T_{\mathrm{O}}^{*}(s) + \delta T_{\mathrm{O}}^{*}(s)(1 - e^{-sT_{\mathrm{d}}}) = 0. \tag{3.9}$$

As the modelling error is part of the system characteristic equation, the system stability is susceptible to this modelling error. As illustrated in the Nyquist diagram in Figure 3.5, the minimum system stability margin is the shortest distance between $T_{\mathrm{O}}^{*}(jw)$ and the critical point (-1,0) in the polar diagram. The condition for the PHIL closed-loop to maintain stability is that this minimum stability margin is always greater than the magnitude of $\left|\delta T_{\mathrm{O}}^{*}(jw)(1 - e^{-jwT_{\mathrm{d}}})\right|$ for all the frequencies, which yields,

$$\left|\delta T_{\mathrm{O}}^{*}(jw)(1 - e^{-jwT_{\mathrm{d}}})\right| < \left|-1 - T_{\mathrm{O}}^{*}(jw)\right|, \ \forall w > 0. \tag{3.10}$$

The limit of the modelling error at which the overall PHIL closed-loop can

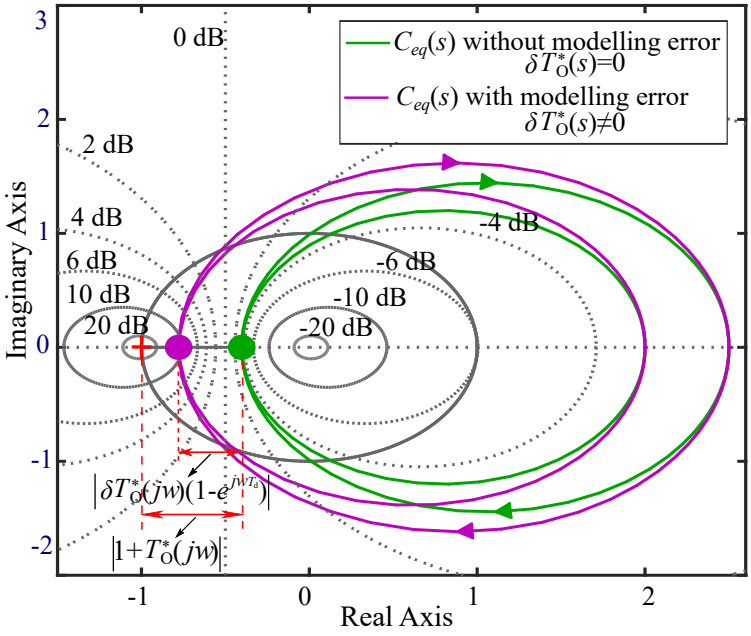

Figure 3.5: Polar diagram of the Smith predictor compensator based PHIL system with and without modelling error in the compensator.

maintain stability is given by,

$$|\delta T^*_{\mathrm{O}}(jw)| < \frac{|1+T^*_{\mathrm{O}}(jw)|}{|1-e^{-jwT_{\mathrm{d}}}|}, \quad \forall w > 0. \tag{3.11}$$

The robustness of Smith predictor is quantitatively defined by the criteria derived in Eq. (3.10) and Eq. (3.11). With more advanced power amplifiers being made available in the market, the precise modelling of the power amplifier comprising subsystems (as in Eq. (2.2)) is feasible in a laboratory environment. Therefore, the error in model estimation stems from the impedance variations during the real-time testing. For a Smith predictor compensator designed for a system with impedance ratio IR_0, variations in impedance ratio can be accommodated to ensure a stable system until the inequality relationship in Eq. (3.10) fails. The value of impedance ratio at which the inequality in Eq. (3.11) is no longer valid is defined as the critical impedance ratio IR_{c}, which serves as the buffer for variability in the impedance ratio guaranteeing PHIL system stability.

3.2 Impedance Identification Aided Adaptive Smith Predictor

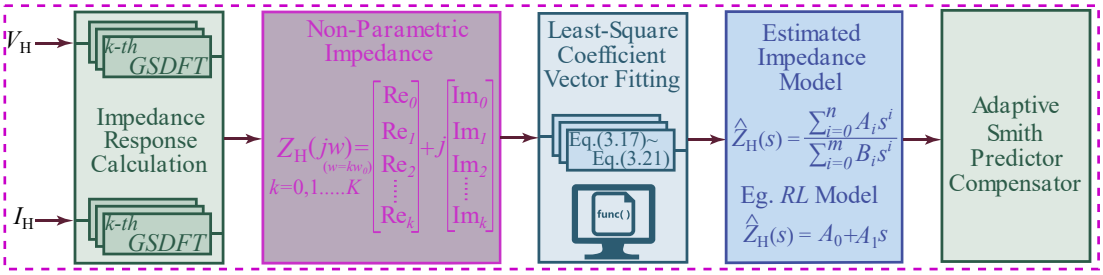

Figure 3.6: Block diagram of GSDFT-based HuT impedance identification aided adaptive Smith predictor.

If the impedance of the system can be estimated in real-time, the model of Smith predictor based compensator adopted for a PHIL setup can be updated to ensure stability with varying impedance. This is the principle adopted for the development of adaptive Smith predictor in this chapter.

As shown in Figure 3.6, the impedance model identification involves applying the Goertzel Algorithm-Based Sliding DFT (GSDFT) to process the externally injected excitation voltage signals and the corresponding current signals for frequency-domain impedance responses calculation. The responses are successively processed by the least-square vector fitting algorithm to get the rational impedance model that is employed to update the adaptive Smith predictor. The following two sub-sections elaborate on these steps in more detail.

3.2.1 Impedance Frequency Response Calculation

In real-time application, the frequency-domain data must be processed frequently and promptly. SDFT is deduced from the Discrete Fourier Transform (DFT) circular shift property [68] with the time-domain sequence circularly shifted by one sample through multiplying $e^{j\frac{2\pi k}{N}}$ and the signal spectral being updated on a

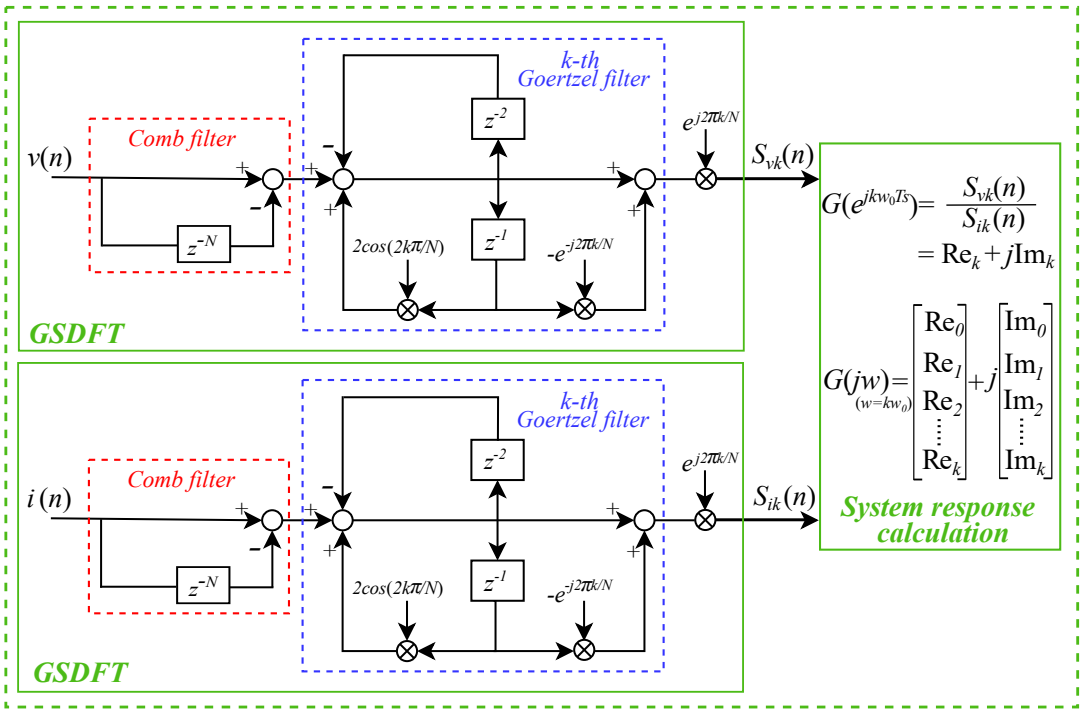

Figure 3.7: GSDFT-based frequency-domain response calculation.

sample-by-sample basis [68, 69]. This attribute enables SDFT to present higher computation efficiency and low computation cost than FFT in processing signals with selective frequencies [68, 70]. Deduced from the frequency sampling theorem as given in Eq. (3.12a), SDFT can be represented as a comb filter in series with complex resonator banks [51] and be written as,

$$S_k(n) = e^{j\frac{2\pi k}{N}}[S_k(n-1) + x(n) - x(n-N)], \tag{3.12a}$$

$$H_{\text{SDFT}}(z) = \frac{S_k(n)}{x(n)} = \underbrace{(1-z^{-N})}_{\text{Comb filter}} \underbrace{\frac{e^{j\frac{2\pi k}{N}}}{1-e^{j\frac{2\pi k}{N}}z^{-1}}}_{\text{complex resonator}}, \tag{3.12b}$$

where $N\,(N = \frac{f_s}{f_0})$ is the window size, f_s is the sampling frequency, f_0 is the fundamental frequency, and $k\,(k = 1, 2, 3, \cdots, N)$ represents the order of recursive filter.

To further reduce the computation complexities of SDFT for its real-time

application, Goertzel algorithm [68–71] is applied to SDFT by multiplying the numerator and denominator of Eq. (3.12b) with $(1-e^{-j\frac{2\pi k}{N}}z^{-1})$. Accordingly, the transfer function of GSDFT consists of real-only coefficients in its denominator and is given by,

$$H_{\text{GSDFT}}(z) = \underbrace{(1-z^{-N})}_{\text{Comb filter}} \underbrace{\frac{(1-e^{-j\frac{2\pi k}{N}}z^{-1})}{1-2\cos(\frac{2\pi k}{N})z^{-1}+z^{-2}}}_{k\text{-th Goertzel filter}} e^{j\frac{2\pi k}{N}}. \tag{3.13}$$

As shown in Figure 3.7, the structure of a GSDFT corresponds to the cascading of a comb filter, a Goertzel filter in second-order Infinite Impulse Response (IIR) form, and a phase shift factor $e^{j\frac{2\pi k}{N}}$. This structure enhances its ease of implementation for frequency-domain response calculation in real-time application.

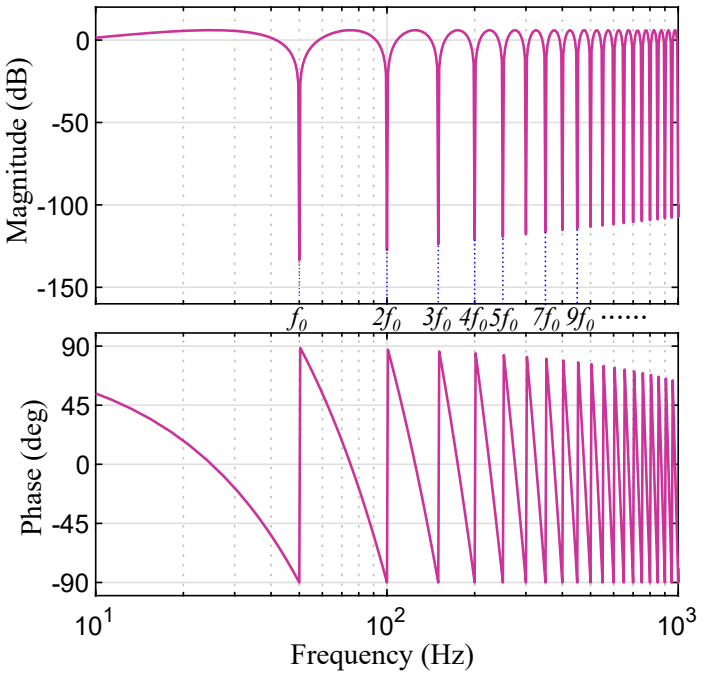

Figure 3.8: Frequency response of the N^{th} order comb filter for a selective set of harmonics.

Figure 3.8 illustrates the frequency response characteristic of comb filter over

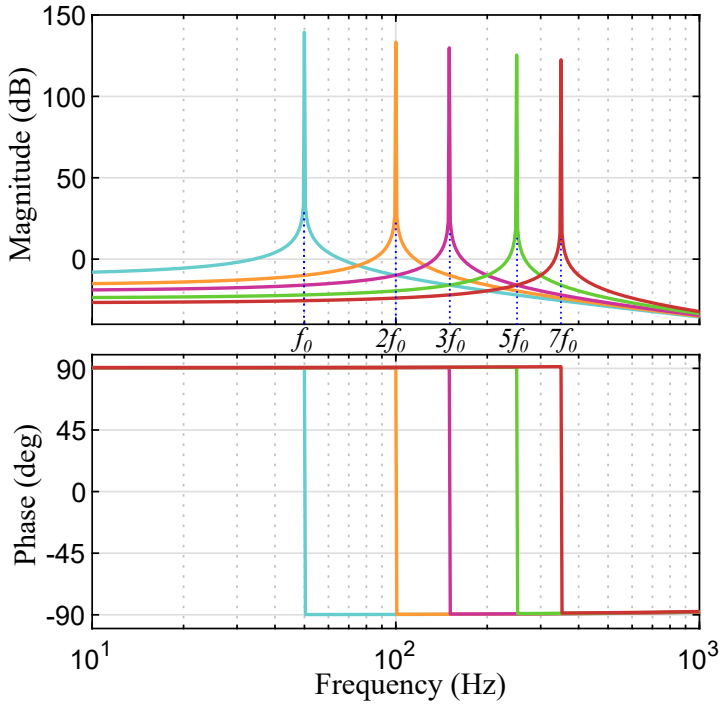

Figure 3.9: Frequency response of complex resonator for a selective set of harmonics.

a set of harmonics. Being widely employed for power system and power converter harmonic extraction and harmonic mitigation [67, 72–74], as shown in Figure 3.8, the comb filter can be envisioned as a notch filter with notches periodically spaced at fundamental and harmonic frequencies. This presents the same characteristic as narrow band-pass filter and enables the attenuation of the input signal with notch frequencies to an extremely low level. As presented in Figure 3.9, the k-th order IIR Goertzel filter is equivalent to a band-pass filter centred at the frequency kf_0 with a sharp cut-off amplitude, which enable it selectively amplifies the corresponding signal component.

It is evident from the frequency response characteristic of the GSDFT filters presented in Figure 3.10, the GSDFT with k-th order Goertzel filter presents unity gain and zero phase shift characteristics at the frequency of concern. Thus the implementation of GSDFT with k-th order Goertzel filter enables the selective signal extraction at a certain frequency of interest without magnitude distortion

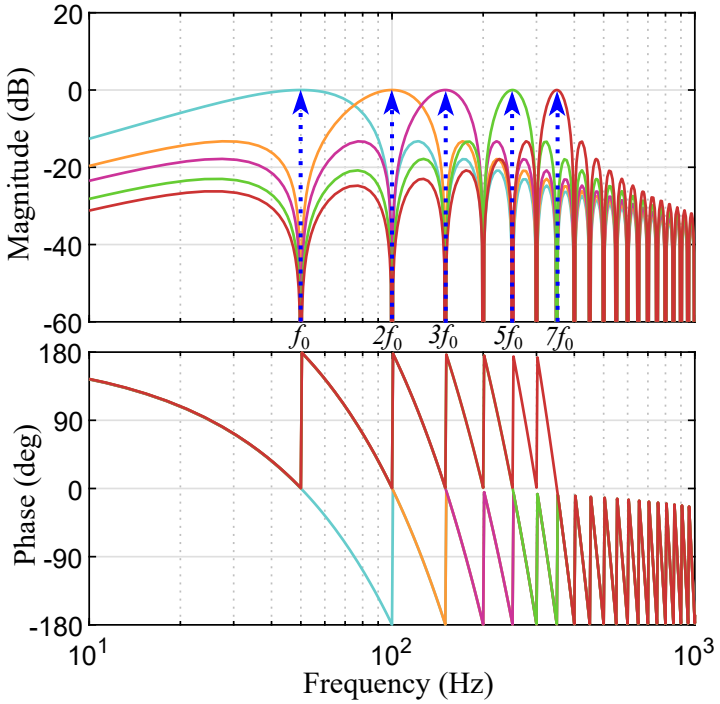

Figure 3.10: Frequency response of the GSDFT with Goertzel filters designed for a selected set of frequencies.

and phase shift. Based on the selective signal processing attribute of GSDFT, the frequency-domain HuT impedance response with respect to an externally injected signal with frequency kw_0 is give by[2],

$$Z_{\mathrm{H}}(e^{jkw_0T_s}) = \frac{S_{vk}(n)}{S_{ik}(n)} = \mathrm{Re}_k + j\mathrm{Im}_k. \tag{3.14}$$

Owing to the sample-by-sample signal processing properties of GSDFT, the HuT impedance frequency response calculation that is based on the GSDFT filters presents higher computation efficiency and higher speed than the conventional FFT-based frequency response calculation over a selective set of frequencies. The frequency-domain HuT impedance data calculated in Eq. (3.14) will be further processed to identify the equivalent HuT model in the following section.

[2] Re and Im denote the real part and imaginary part of a complex number, respectively.

3.2.2 HuT Impedance Parameters Calculation

As shown in Figure 3.6, the multiple sinusoidal voltage excitation signals with predefined frequencies w_k, $(k = 1, \cdots, K)$ are injected via the power amplifier and the corresponding frequency-domain system response data is calculated by GSDFT. The response data is further processed by exploiting the vector fitting algorithm in a least-square sense.

The rational transfer function of the impedance, a continuous-time linear time-invariant (LTI) system, is,

$$\widehat{Z}_{\mathrm{H}}(s) = \frac{A(s)}{B(s)} = \frac{\sum_{i=0}^{n} a_i s^i}{1 + \sum_{i=1}^{m} b_i s^i}, \tag{3.15}$$

where n and m are the order of the numerator and denominator, respectively. a_i and b_i represent the coefficients of the transfer function to be estimated.

The frequency response data calculated by GSDFT over the predefined frequencies, namely $|w_0, Kw_0|$, are expressed as,

$$Z_{\mathrm{H}}(jw_k) = \mathrm{Re}_k + j\mathrm{Im}_k, \;\; k = (1, \cdots, K)\;, \tag{3.16}$$

where K represents the number of the frequency components to be injected.

ϵ_k represents the numerical difference between the measured $Z_{\mathrm{H}}(jw_k)$ and the frequency response of the estimated $\widehat{Z}_{\mathrm{H}}(jw_k)$ at frequency w_k and is given by,

$$\epsilon_k = (\mathrm{Re}_k + j\mathrm{Im}_k) - \frac{A(jw_k)}{B(jw_k)}, \tag{3.17}$$

where

$$A(jw_k) = \sum_{i=0}^{n} a_i (jw_k)^i, \;\; B(jw_k) = 1 + \sum_{i=1}^{m} b_i (jw_k)^i. \tag{3.18}$$

Exploiting the residual ϵ_k as a scalar to assess the estimation error, the weighted error $\bar{\epsilon}_k$ is calculated by multiplying the residual ϵ_k with weighting function $B(jw_k)$, which yields,

$$\bar{\epsilon}_k = \epsilon_k B(jw_k) = (\mathrm{Re}_k + j\mathrm{Im}_k)B(jw_k) - A(jw_k). \tag{3.19}$$

Quadratic cost function is further defined as the summed square of the weighted error $\bar{\epsilon}_k$ over the experimentally-observed frequency-domain data, namely,

$$\jmath_{(\mathbf{A},\mathbf{B})} = \arg\min_{\mathbf{A},\mathbf{B}} \sum_{k=1}^{K} \left|\bar{\epsilon}_k\right|^2. \tag{3.20}$$

Coefficient matrices $\mathbf{A}$ and $\mathbf{B}$ are calculated by minimizing the quadratic cost function through differentiating it with respect to unknown coefficients (i.e., a_i and b_i), that is,

$$\begin{cases} \frac{\partial \jmath_{(\mathbf{A},\mathbf{B})}}{\partial a_i} = 0, \quad \mathbf{A} = [a_0, a_1, a_2, \cdots a_n]^T, \\ \frac{\partial \jmath_{(\mathbf{A},\mathbf{B})}}{\partial b_i} = 0, \quad \mathbf{B} = [1, b_1, b_2, \cdots b_m]^T. \end{cases} \tag{3.21}$$

The vector fitting linearisation method as elaborated in [75, 76] is applied to the non-linear matrices in Eq. (3.21) to converter it into a set of linear algebraic equations. Based on these, the numerical values of the coefficient matrices $\mathbf{A}$ and $\mathbf{B}$ are further calculated by solving the corresponding linear algebraic equations. The details of this method and its examples are presented in Appendix A.

The main advantage of this method is that the impedance measurement is based on GSDFT calculations over a selected set of frequencies with high-speed computation and low complexity. The compensator is updated based on the online impedance measurement without a requirement of prior knowledge of the parameters of system to be tested, which is well-suited for PHIL simulation.

Table 3.1: Parameters for the analytical assessment and simulation.

Setup	k_1	k_2	f_{c2}	f_{c4}	T_{d1}	T_{d2}	T_{d3}	T_{d4}	T_{d}
Unit	–	–	kHz	kHz	µs	µs	µs	µs	µs
Value	0.2	5	8	8	50	450	50	50	600

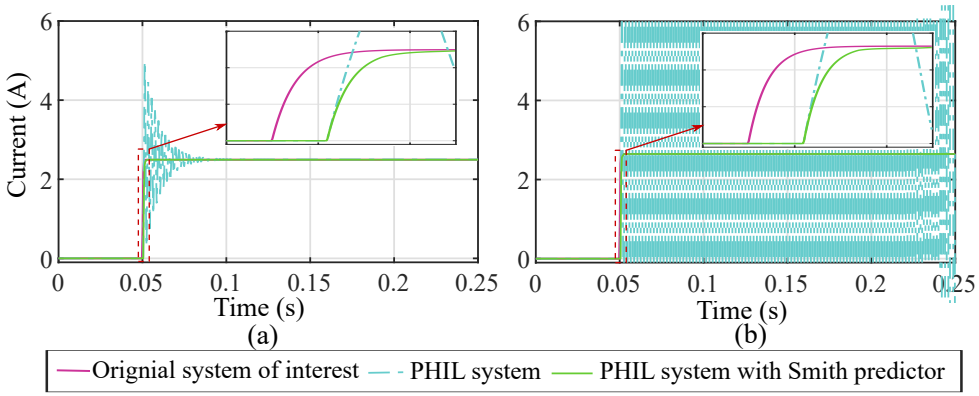

Figure 3.11: Current behaviour of the PHIL systems with (a) $Z_{\mathrm{H}} = (1\mathrm{e}^{-3}s + 1)\Omega$ and (b) $Z_{\mathrm{H}} = (7.692\mathrm{e}^{-4}s + 0.769)\Omega$.

3.3 Analytical Assessment and Simulation

This section presents the analytical assessment and evaluation of Smith predictor in improving the PHIL stability through simulation undertaken in Matlab/Simulink. The PHIL interface parameters (as in Eq. (2.2)) are given in Table 3.1. The software side impedance is chosen as $Z_{\mathrm{S}} = 3\,\Omega$ (Note that, as the Smith predictor is designed according to the system impedance, the effectiveness validation of proposed approach is not limited by the choice of the impedance of the system under consideration) and the simulation side voltage is emulated as a 10 V step voltage signal in the cases presented in subsections 3.3.1 and 3.3.2.

3.3.1 Stability Enhancement by Smith Predictor

The first case involves a PHIL system with hardware impedance $Z_{\mathrm{H}} = (1\mathrm{e}^{-3}s + 1)\Omega$ and the impedance ratio IR is the same as IR_0, for which the analytical stabil-

ity assessment is presented in Figure 2.4. The hardware side current is presented in Figure 3.11(a). For the PHIL system without a compensator, the current reaches a stable state after some oscillations and is consistent with that of the SoI at the steady state. As for the PHIL with Smith predictor compensator, the current oscillations stemming from the time delay are mitigated as the time delay has been equivalently shifted out of the PHIL closed-loop by the compensator.

Figure 3.11(b) presents the current behaviour of a PHIL system with hardware impedance $Z_{\mathrm{H}} = (7.692\mathrm{e}^{-3}s + 0.769)\Omega$ and an impedance ratio as $1.3\,\mathrm{IR}_0$. As analysed in Figure 2.4, this impedance ratio exceeds the critical ratio limit and the closed-loop system is unstable. Correspondingly, the current of such a PHIL system without a compensator is not convergent in nature. While the current of the PHIL system with a compensator converges and is aligned with that of the SoI at steady state.

Comparing these two cases, the variation in system impedance can lead to instability if the variation exceeds the critical IR boundary as shown in Figure 2.4. The incorporation of Smith predictor compensator stabilises the closed-loop system and also extends the range of impedance ratios over which the PHIL simulation can remain stable.

3.3.2 Robustness Assessment of Smith Predictor

Although the passive Smith predictor can ensure the stability of PHIL setups over an extended impedance range, the system can tend towards instability if the modelling error between estimated model and actual model breaches the stability criterion defined by Eq. (3.10) and Eq. (3.11). Consider a PHIL system with impedance ($Z_{\mathrm{S}} = 3\,\Omega$, $Z_{\mathrm{H}} = (1\mathrm{e}^{-3}s + 1)\Omega$). A Smith predictor compensator is designed for the example PHIL system. Figure 3.12 presents the inequalities in Eq. (3.10) against the variable impedance ratio as a result of hardware side impedance variations. Critical impedance ratio IR_{c} is obtained as $\mathrm{IR}_{\mathrm{c}} = 2.88\mathrm{IR}_0$

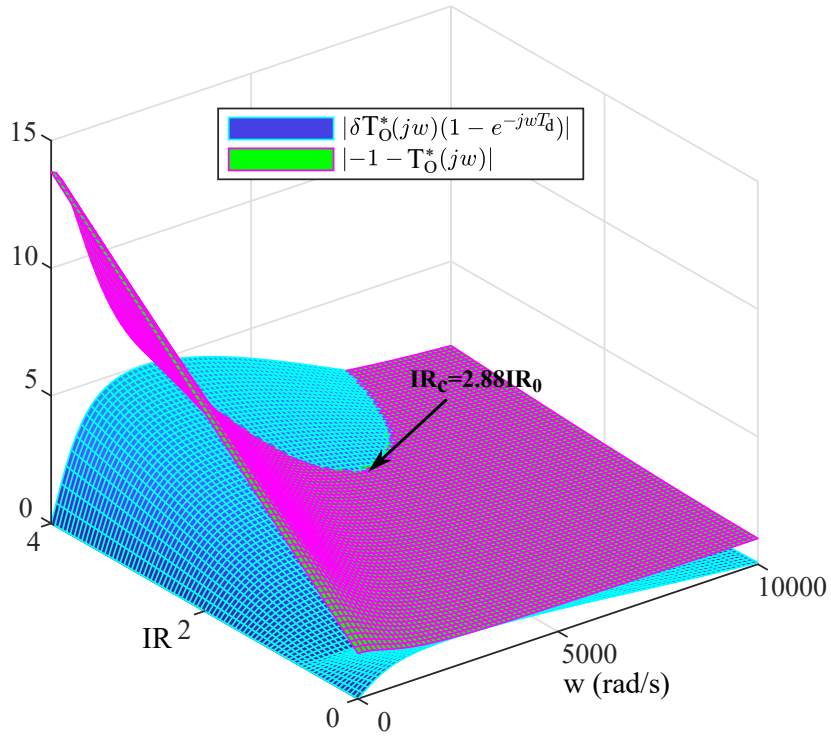

Figure 3.12: Magnitude of the inequalities in Eq. (3.10).

Table 3.2: Hardware-side impedance and impedance ratio.

Cases	**Case A**		**Case B**	
$Z_{\mathrm{H}}\,(\Omega)$	$t \leq 0.15s$	$t > 0.15s$	$t \leq 0.15s$	$t > 0.15s$
	$1\mathrm{e}^{-3}s+1$	$7.692\mathrm{e}^{-4}s+0.769$	$1\mathrm{e}^{-3}s+1$	$3.448\mathrm{e}^{-4}s+0.345$
IR	IR_0	$1.33\,\mathrm{IR}_0$	IR_0	$2.90\,\mathrm{IR}_0$

from the boundary of the two terms in Eq. (3.10). Provided the compensator is not updated according to the impedance variation, the PHIL system is unstable once the impedance ratio exceeds $\mathrm{IR_c}$, otherwise, the system is stable but inaccurate due to the modelling error between the estimated model and the actual model.

This is further demonstrated in simulation where a passive Smith predictor is designed according to the impedance ($Z_{\mathrm{S}} = 3\,\Omega$, $Z_{\mathrm{H}} = (1\mathrm{e}^{-3}s+1)\Omega$) and hardware side impedance variation is emulated at $t = 0.15s$ for the two cases

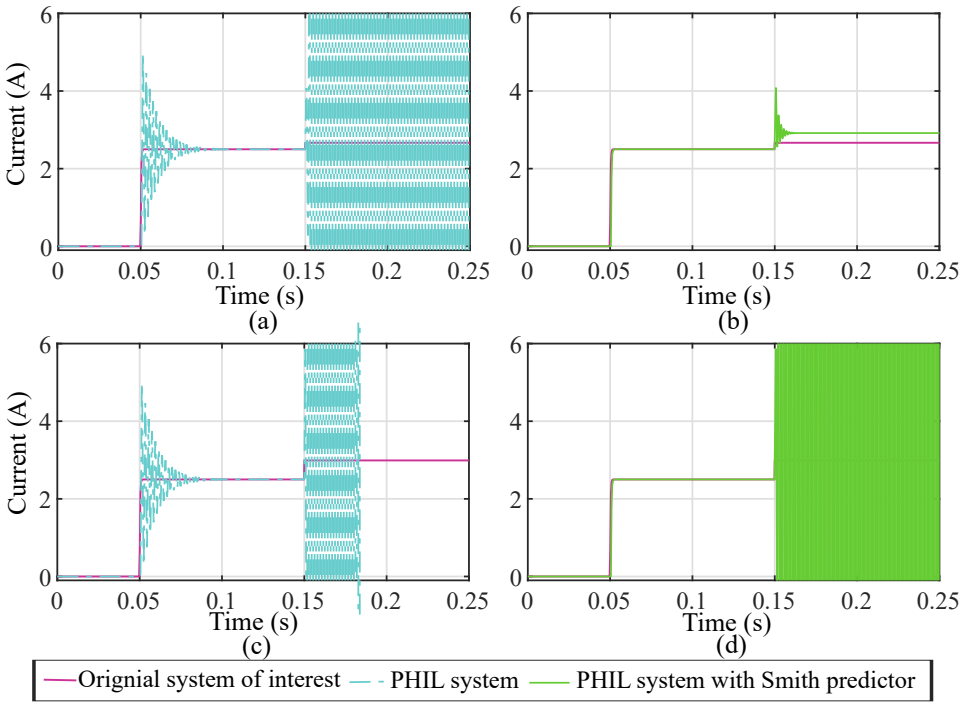

Figure 3.13: Current behaviour of the PHIL systems with impedance variations: (a), (b): Case a, (c), (d): Case b.

listed in Table 3.2. For Case A, as shown in Figure 3.13(a), the PHIL system with impedance ratio as IR_0 is stable before impedance change and becomes unstable after impedance change. Before the impedance change, as shown in Figure 3.13(b), the PHIL with compensator is stable and its current is consistent with that of the SoI. After impedance change, the compensator still stabilises the PHIL system as the impedance ratio is within the critical impedance ratio in Figure 3.12, but the current deviates from that of the SoI. In terms of Case B, as shown in Figure 3.13(c), the PHIL system without a compensator is stable before impedance change but becomes unstable after impedance change. For the PHIL system with a compensator, since the impedance ratio exceeds IR_c after the impedance change, the compensator is not able to maintain the stability criterion defined in Eq. (3.10). At this point, as shown in Figure 3.13(d), the current is divergent and tends to instability and the PHIL system reaches an unstable state.

Table 3.3: Hardware-side impedance variation.

Parameters	R_1	R_2	L_1	L_2	C
Value	1.000 Ω	0.500 Ω	1.000 mH	0.333 mH	250.000 µF

Impedance	**Element**	**Reference**	**Estimation**
Z_{H1}	$R_1 + L_1$	$R_1 + sL_1$	$1.005\mathrm{e}^{-3}s + 1$
Z_{H2}	$R_2 + L_2$	$R_2 + sL_2$	$3.334\mathrm{e}^{-4}s + 0.5$
Z_{H3}	$(R_1 + C)//L_1$	$\frac{R_1L_1Cs^2+L_1s}{L_1Cs^2+R_1Cs+1}$	$\frac{2.505\mathrm{e}^{-7}s^2+9.856\mathrm{e}^{-4}s+1.245\mathrm{e}^{-4}}{2.521\mathrm{e}^{-7}s^2+2.469\mathrm{e}^{-4}s+1}$

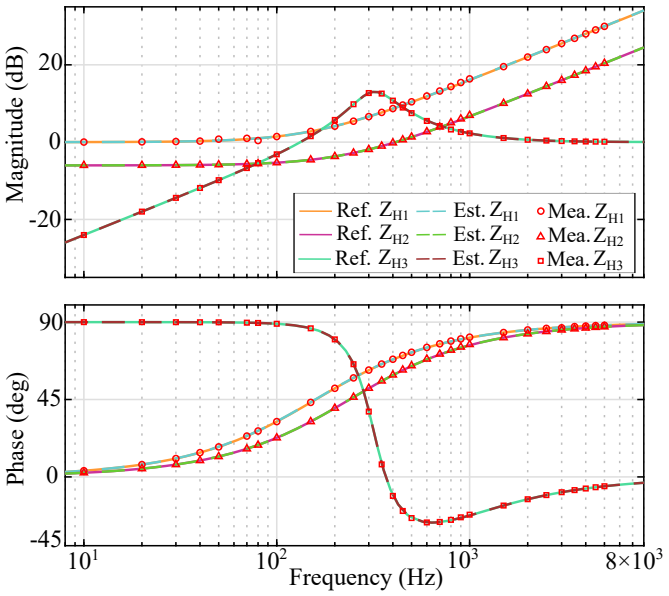

Figure 3.14: Frequency response of the impedance model.

3.3.3 Assessment of Real-Time Adaptive Smith Predictor

For the evaluation of adaptive Smith predictor, a single-phase Alternating Current (AC) voltage source V_{S} rated at 230 V and 50 Hz and three hardware impedances (combination of resistive-inductive and resistive-inductive-capacitive) are chosen as presented Table 3.3. The simulation begins with hardware side impedance as Z_{H1} for which the Smith predictor is accordingly designed. Two cases are presented where impedance is varied at $t = 0.15s$, first from Z_{H1} to Z_{H2}, and

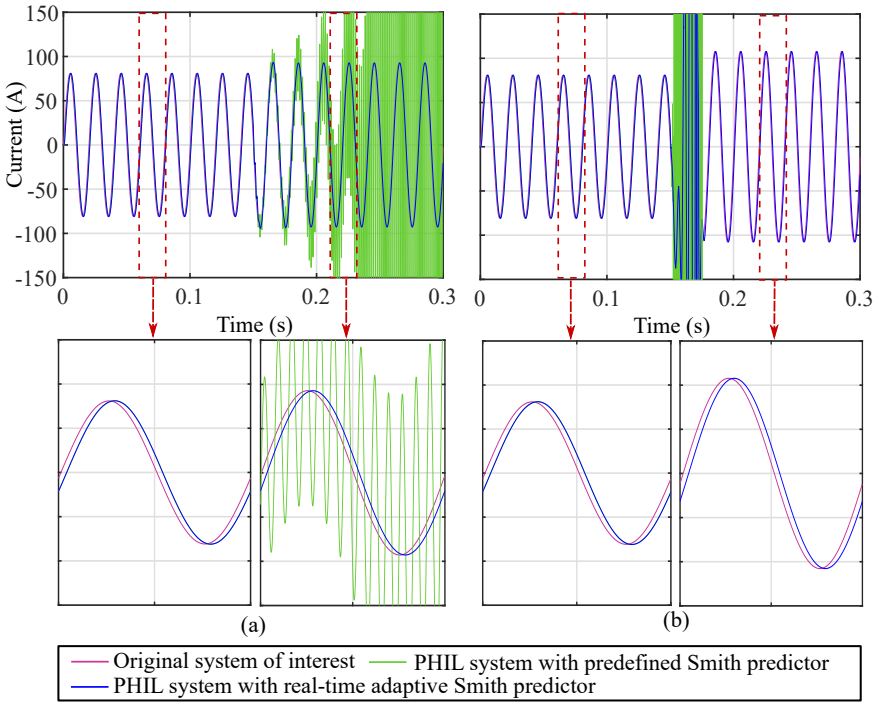

Figure 3.15: Current behaviour of the PHIL systems with impedance variations: (a) Z_{H1} to Z_{H2} (b) Z_{H1} to Z_{H3}.

second from Z_{H1} to Z_{H3}.

As presented in Section 3.2, the adaptive Smith predictor is dependent upon accurate estimation of the impedance change. Figure 3.14 presents the GSDFT experimental measurement over the selected set of frequencies ranging from 10 Hz to 5 kHz and the frequency response of the reference model and estimated model identified by the impedance identification units as presented in Figure 3.6. Although there are some slight deviations between the experimental measurement data and the reference model, most frequency-domain measurement data are well-fitted to the reference model. Good agreement between the estimated impedance transfer function and the reference impedance transfer function has been achieved.

Figure 3.15 shows the hardware side currents of the original SoI, PHIL system with passive compensator or with adaptive compensator. Before the impedance change, the PHIL systems implemented with these compensators are stable and their currents lag the SoI current by T_{d}. However, after the impedance change,

the PHIL system with a passive compensator is unstable. On the contrary, the PHIL system with real-time adaptive compensator is stable and the short-period oscillations after the impedance change are suppressed.

3.4 Experimental Validation

This section is dedicated to the experimental validation of the proposed PHIL stability enhancement scheme. The experiment was undertaken in the Dynamic Power System Laboratory (DPSL) at the University of Strathclyde. Figure 3.16 shows the experimental setup. An equivalent voltage source and a low X/R ratio grid impedance, as listed in Table 3.4, are employed to emulate a low-voltage grid within the DRTS. A 256-step passive load bank is incorporated within the PHIL simulation by a Triphase 90 kVA voltage source back-to-back converter (TP90 kVA) acting as the power amplifier. The signal conversion between DRTS and TP90 kVA are achieved by employing two signal conversion cards (i.e., Giga-Transceiver Analogue Output (GTAO) card and Giga-Transceiver Analogue Input (GTAI) card). The remainder of the parameters for this PHIL setup[3] are presented in Table 3.4.

Table 3.4: Parameters of the PHIL experimental setup.

Description	**Symbol**	**Unit**	**Value**
Software side voltage source	$V_{\mathrm{S,LL}}$	V	400
System fundamental frequency	f_0	Hz	50
Total time delay	T_d	µs	250
Software impedance	Z_{S}	Ω	12
Hardware system impedance	Z_{He1}	Ω	$5\mathrm{e}^{-4}s + 12$
as identified in Figure 3.19	Z_{He2}	Ω	$1\mathrm{e}^{-3}s + 10$
Power amplifier (TP90 kVA)	$G_2(s)$	-	$\dfrac{1}{2.350\mathrm{e}^{-9}s^2 + 2.923\mathrm{e}^{-5}s + 1}$

[3] This experimental setup and power equipment are further utilised in the following chapters.

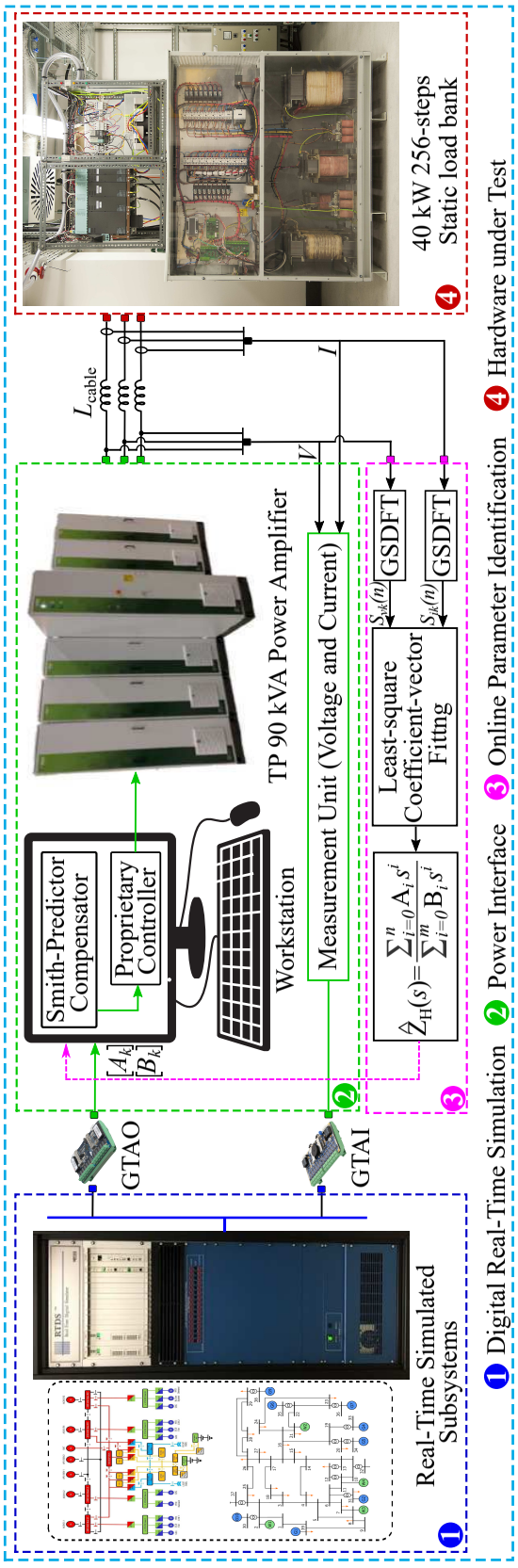

Figure 3.16: Power hardware-in-the-loop experimental setup.

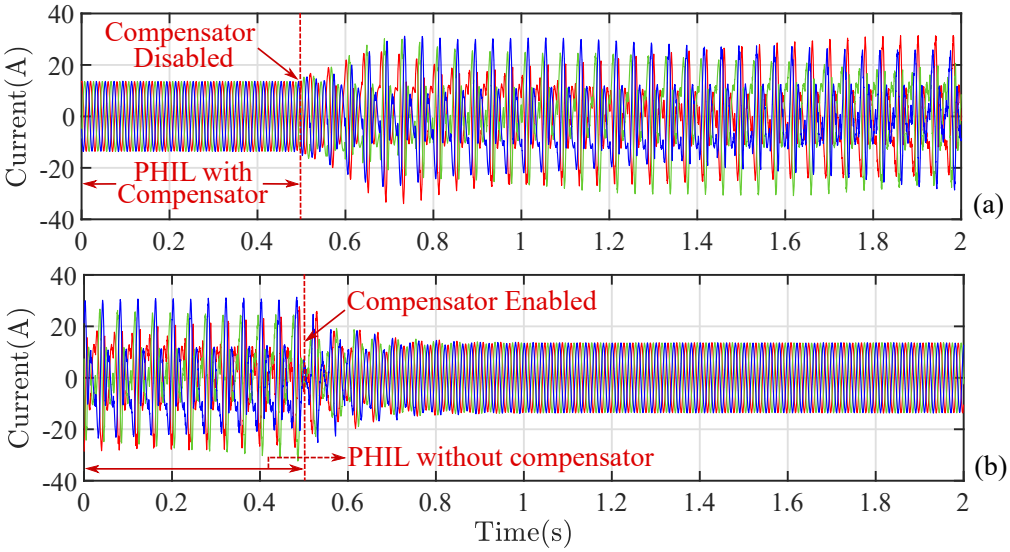

Figure 3.17: Hardware current of the PHIL system with impedance Z_{He1}: (a) without and (b) with Smith predictor compensator.

The digital voltage signal $V_{S'}$ measured from the point of common coupling of the equivalent network is transmitted to TP90 kVA as its command signal, which is processed by the proposed compensator. The passive load bank is coupled with the output terminal of TP90 kVA. The current response of the passive load bank I_{H} is measured and transmitted to DRTS as the command signal for the controllable current source. The analogue signals V_{H} and I_{H}, and the impedance measurement are recorded by the Triphase datalogger with a sampling rate of 16 kHz and are replotted by Matlab.

3.4.1 Experimental Evaluation of Smith Predictor

Figure 3.17 presents the hardware current signal of the PHIL setup with hardware impedance Z_{He1}. For the PHIL system without a compensator, as shown in Figure 3.17(a), the hardware current diverges once the compensator is disabled and the closed-loop system tends to instability. This is aligned with the stability assessment as presented in Figure 3.18(a). Once the compensator is enabled, the hardware current converges and reaches a stable state as in Figure 3.17(b). This

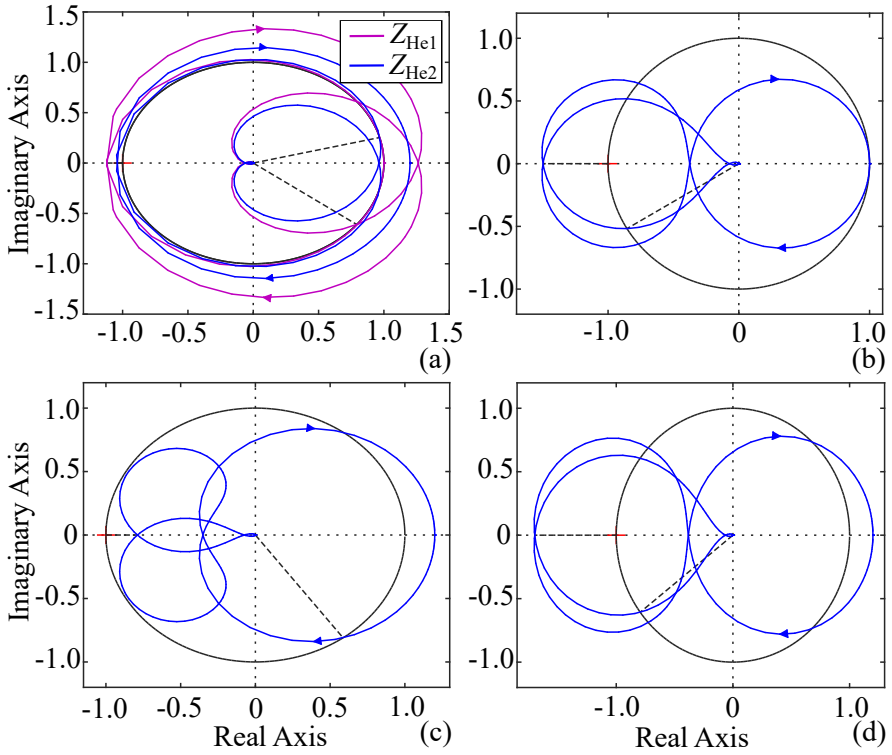

Figure 3.18: Nyquist diagram of the open-loop transfer function of a PHIL system with (a) Z_{He1} and Z_{He2}, (b) SP (based on Z_{He1}) and Z_{He1}, (c) SP (based on Z_{He1}) and Z_{He2}, (d) SP (based on Z_{He2}) and Z_{He2}.

is in agreement with the stability assessment of the open-loop transfer function of the Smith predictor based PHIL system in Figure 3.18(b).

3.4.2 Experimental Robustness Assessment of the Adaptive Smith Predictor

The robustness of the Smith predictor compensator is assessed by implementing an impedance variation in the passive load bank. Figure 3.19(b) and Figure 3.19(c) show the impedance measured by the GSDFT-based impedance identification unit. As shown in Figure 3.19(a), the hardware side current presents significant oscillations and reaches an unstable state after the impedance varies from Z_{He1} to Z_{He2}. Corresponding to the stability assessment as presented in Figure 3.18(c), the compensator that is initially designed for the hardware impedance

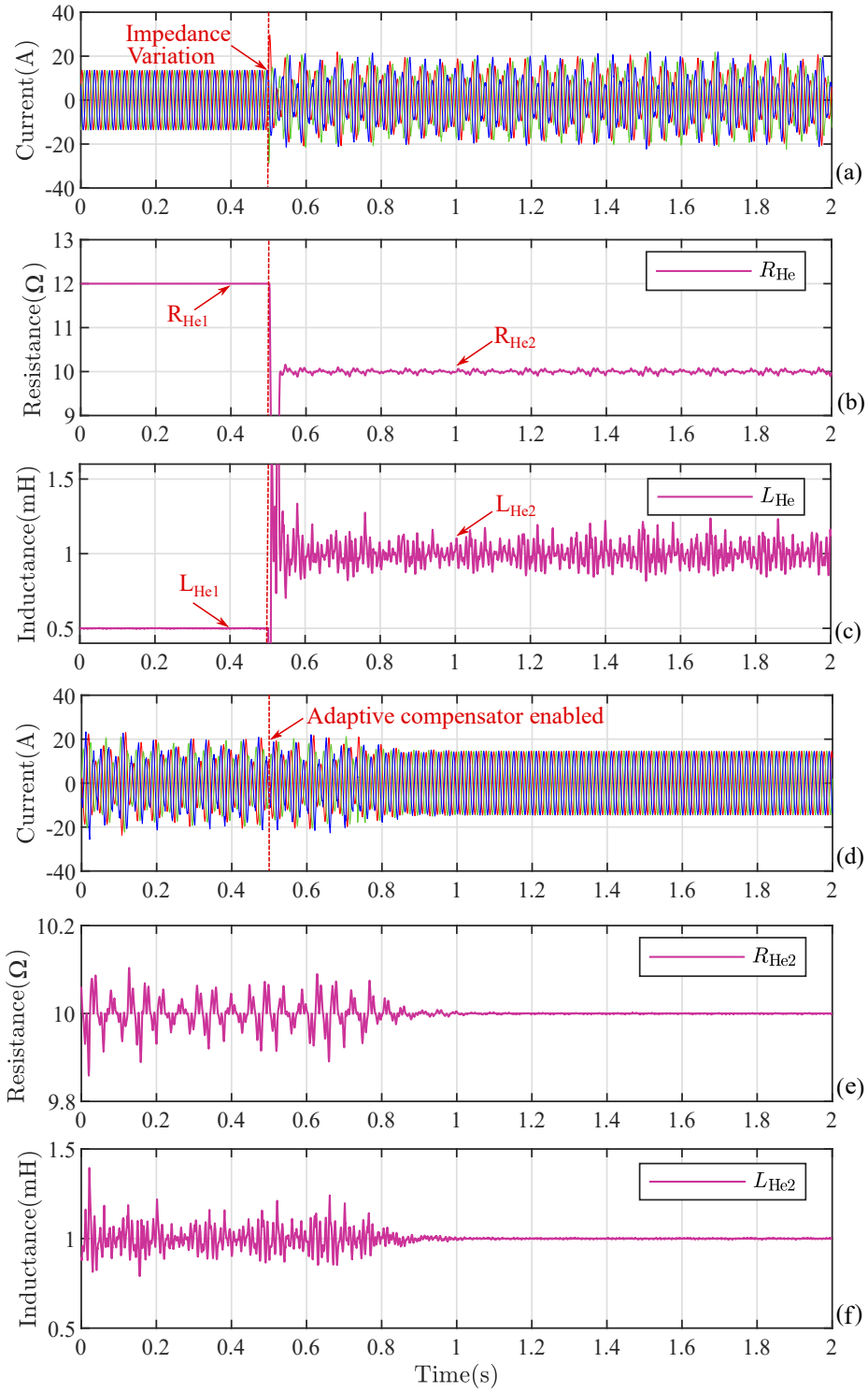

Figure 3.19: Hardware current of PHIL system with passive SP (based on Z_{He1}) and impedance vary from Z_{He1} to Z_{He2}: (a), (b), (c), and Hardware current of PHIL system with impedance Z_{He2} and adaptive SP that is initially based on Z_{He1} and is updated according to the online impedance measurement: (d), (e), (f).

Z_{He1} is no longer capable to stabilise the PHIL closed system as the stability criterion defined in Eq. (3.10) is not maintained. Upon activation of the adaptive compensator, the current converges to a stable state and the GSDFT-based impedance measurement presents more accurate results due to the stabilisation of the online updated adaptive compensator as shown in Figure 3.19(e). This is consistent with the stability assessment in Figure 3.18(d).

3.5 Discussion

The performance of the passive Smith predictor and the distinct advantage offered by the adaptive Smith predictor have been demonstrated by analytical assessment, simulation and experimental results. This section presents a brief discussion on the applicability and limitation of the proposed approach.

As demonstrated in the above sections, the proposed adaptive Smith predictor scheme stabilises the PHIL system with inherent impedance variation. Although the applicability of the approach in this chapter has been limited to passive loads for the purpose of proof of concept demonstration, the approach is extendable and applicable in theory for a stable PHIL system incorporating parallel connected power converters, active or passive loads, of which the equivalent impedance may witness variation when single or multiple power apparatus plugged in or out. This can be explored in frame of future research.

The Smith predictor based PHIL system presents accurate simulation results as that of the original system of interest when it reaches a steady state. In terms of the transient state performance, as demonstrated in Figure 3.11, the Smith predictor based PHIL system presents less oscillations than that of the PHIL system without Smith predictor when the system is subject to a step change in voltage. The improved transient performance of the Smith predictor based PHIL system is achieved by the mitigation of time delay that degrades the system

convergence speed as a result of deteriorated system stability margin.

Even though the Smith predictor contributes to improved transient and steady state performance, its online impedance identification approach presents a limitation for its applicability to fast changes in impedances. As shown in Figure 3.15(b), the adaptive Smith predictor stabilises the PHIL system 0.02 s after a step change in impedance is applied. This arises from the natural circular signal processing attribute of the GSDFT based online impedance identification scheme that requires one-cycle processing time (i.e., 0.02 s) for calculating the impedance parameters and updating the Smith predictor. This limitation does not deteriorate the performance of the proposed Smith predictor in stabilizing the PHIL system with inherent impedance variation that could challenge the closed-loop stability as demonstrated by the simulation results and the experimental results. Development of faster online impedance parameters identification schemes can enhance the applicability of the proposed methodology for the faster impedance change scenarios and their associated transient studies. This forms an interesting direction for future research.

3.6 Summary

In an effort to mitigate the stability deteriorating impact stemming from the time delay and impedance variation, while at the same time enabling a stable PHIL setup over a wider range of scenarios, this chapter proposed a PHIL closed-loop stability enhancement scheme involving the Smith predictor compensator and GSDFT-based impedance identification techniques. The adoption of Smith predictor compensator is motivated by its functionality in equivalently shifting the inherent time delay out of the PHIL closed-loop, thus enabling a virtually delay-free operation with improved stability margin. Consequently, the improved stability margin extends the constraint of impedance ratio that can be raised

before breaching the system stability, and thus enabling stable PHIL operation over a wider impedance range than that possible without the proposed Smith predictor compensator.

Although the Smith predictor compensator offers remarkable avenues for improving PHIL stability over an extended impedance range, the PHIL system that is based on this passive compensation method can tend towards instability once the modelling error between the estimated model in the compensator and the actual model breaches the stability criterion defined in the compensator robustness analysis section. Subsequently, the GSDFT-based impedance identification method is adopted to enhance the robustness of the proposed compensator and equip it with adaptivity to system impedance variation.

By employing the GSDFT-based impedance identification, good agreement between the estimated impedance transfer function and the reference impedance transfer function has been achieved. This enhances the robustness of the Smith predictor compensator and the consequent PHIL stability, which has been validated by experimental results. Furthermore, the effectiveness and robustness of the proposed adaptive Smith predictor compensator based stabilisation scheme have been analysed and assessed by pure simulation and real-world PHIL experiment. Moreover, the simulation and experimental results reveal that the proposed adaptive Smith predictor enables a stable PHIL system over a wider range of impedance ratios, allowing for a broader range of scenarios being investigated at one experimental run than that of the PHIL system without the proposed compensator. This is critical for a stable and well-established robust PHIL experimental assessment of the candidate hardware systems with inherently variable impedance. This scheme could be extendable and applicable for a stable PHIL incorporating multiple parallel power converters or physical power network with inherent impedance variation on a common basis and will play a significant role in the experimental validation of the emerging novel power techniques.

Chapter 4

Compensation for High-Fidelity PHIL Interfaces

As presented in Chapter 2, PHIL is not a plug-and-play simulation tool that just leverages an off-the-shelf real-time digital simulator and power hardware. As a result of splitting the real-world SoI into DRTS-based simulation and physical HuT, the power interface that bridges these two systems inevitably introduces non-ideal characteristics (e.g., time delay, signal distortion, and limited bandwidth) to the PHIL closed-loop setup. As analysed in Chapter 2.3 and Chapter 2.4, from the standpoint of PHIL system performance, these non-ideal characteristics pose significant threat to system stability, play a detrimental role in the PHIL power signal synchronisation and power transfer transparency, and limit the order of harmonics being replicated by the PHIL setup.

Power amplifier (e.g., switched-mode, generator, linear amplifier) bridges DRTS and HuT [19–21, 25, 39, 77–81]. For medium and high voltage PHIL applications, the switched-mode VSC power amplifier is widely employed as a power source or sink for the HuT due to its advantages of cost, efficiency, controllability [19–21, 25, 39, 77]. The voltage tracking capability of VSC with closed-loop control is achieved at the expense of a resultant low bandwidth, which limits its

capability of replicating the high-frequency reference signal that includes certain harmonics in the PHIL simulation with different testing objectives. As presented in [59], the VSC-based power amplifier with open-loop control is efficient to replicate high-frequency transients within PHIL and introduces less time delay than the VSC with closed-loop control. However, without proper compensation strategies applied to the open-loop controlled VSC-based power amplification stage, the actual PHIL system response presents significant discrepancies when compared with that of the original SoI due to the following key determinants:

1. Despite a power amplifier with ideal characteristics (i.e., infinite bandwidth and unity gain) is expected in the PHIL system and is assumed to be idealised in some research works [33, 36], the actual power amplifier, which is modelled as a time delay in series with a low-pass filter in [30, 37–39], presents remarkable non-ideal characteristics (i.e., limited bandwidth, non-unity gain, and resonance of the passive output filter). These characteristics are attributed to its digital control and the passive output filters that are employed to limit the output voltage ripple stemming from high-frequency pulsating modulation and to realise accurate power signal replication.

2. The non-zero phase shift introduced by the power amplifier output filter presents the same effects as the loop phase lag that results from the time delay introduced by multiple stages within the PHIL closed-loop [30], on reducing the system stability margin, deteriorating the power signal synchronisation accuracy, and degrading the transparency of power transfer between DRTS and HuT [30, 31, 33].

To avoid significant simulation errors and potential damage to the apparatus in the closed-loop simulation configuration, many research efforts have been devoted to compensating for the non-ideal power interface via mitigating the effects of the dynamics and non-ideal characteristics mentioned above. In [37],

notch filter and low-pass feedback filter were utilised to compensate for the parasitic resonance of the passive output filter and the phase lag within the PHIL closed-loop, respectively. However, the cancellation of resonance cannot guarantee the unity-gain of the compensated power interface and introduces additional phase lag to be compensated. The feedback filter-based compensation is achieved at the expense of lower bandwidth and presents non-unity gain characteristic if high-order frequency components are taken into consideration. Phase-lead compensator was employed to compensate for the magnitude attenuation and the phase lag of the power interface in [38]. While the frequency response of the compensated power interface is much closer to unity, as discussed in Section 4.3, the non-unity gain and phase-lag over a certain frequency range still degrade the stability and accuracy of PHIL simulation.

To tackle the stability and accuracy issue arising from the non-ideal power interface characteristics and address the limitations of the compensation methods in the literature, this chapter presents a compensation method compensating for the non-ideal power interface by maximising its bandwidth, maintaining its unity-gain characteristic, and compensating for the phase-shift over the frequencies of interest. This contributes towards a robust PHIL setup with high-fidelity interface and enhanced accuracy.

Figure 4.1 shows a conceptual representation of the proposals stated in this chapter. The rest of the chapter is structured in the subsequent manner: Section 4.1 provides the details of PHIL system modelling. Section 4.2 presents the analysis of PHIL system regarding its stability, accuracy, and power transfer transparency. In Section 4.3, the details of the proposed compensation method are elaborated. Subsequently, in Section 4.4, case studies are carried out to validate the effectiveness of the proposed compensation method. Section 4.5 makes a conclusion and summarises the scopes of the proposed method[1].

[1] This chapter is an extension of conference publications [31, 32]

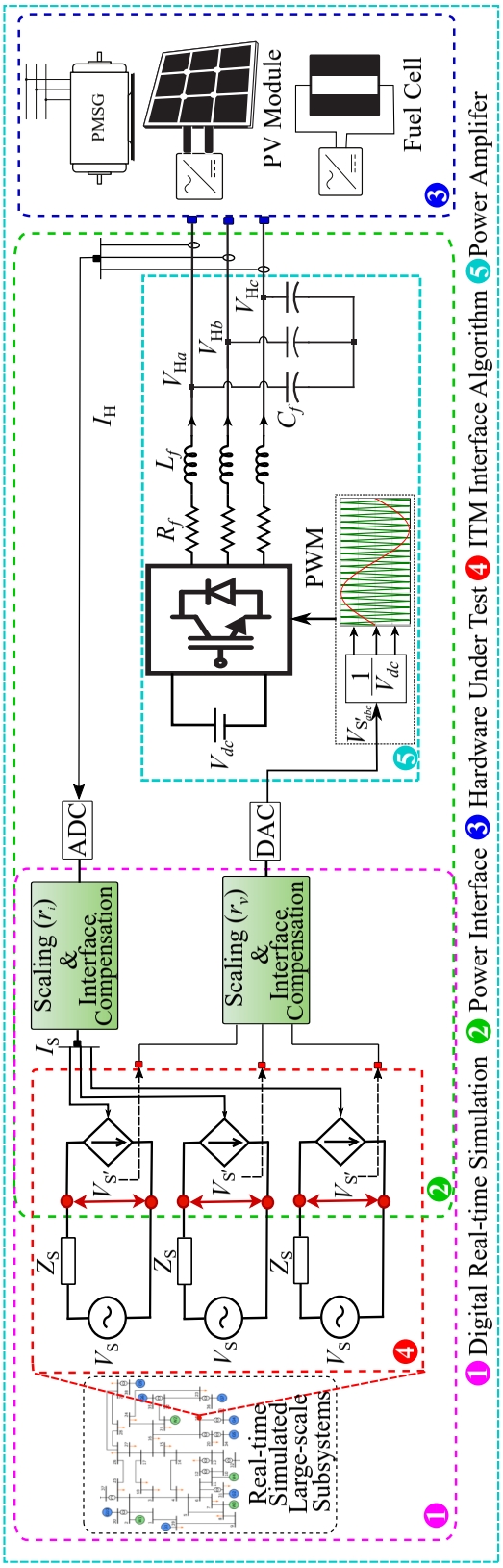

Figure 4.1: A conceptual representation of the PHIL topology and the proposed compensation scheme in this chapter.

4.1 Modelling of PHIL System with Open-Loop Controlled VSC-Based Power Amplifier

This section presents the detailed modelling of the open-loop controlled switched-mode VSC-based PHIL system along with an in-depth analysis of its accuracy with the proposed power signal scaling ratio taken into account.

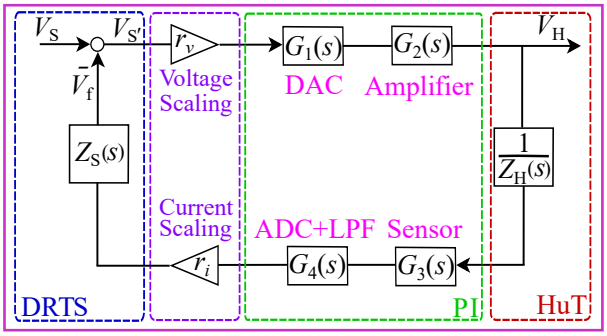

Figure 4.2: Equivalent block diagram of the V-ITM based PHIL system in Fig. 4.1.

Figure 4.2 presents the equivalent block diagram of the PHIL system presented in Figure 4.1. Being different from the generic modelling as presented in Chapter 2.2, power signal scaling ratio and open-loop controlled VSC power amplifier are incorporated into this PHIL setup. These additive blocks within this diagram are modelled as follows:

4.1.1 Voltage and Current Scaling Ratio

The voltage level and power capacity of the real-time emulated power network is much higher than that of the power amplifier and physical HuT in the laboratory. Consequently, a voltage scaling ratio is introduced to facilitate the capability of a power amplifier by scaling down the PCC command voltage $V_{S'}$ under the rated voltage of the power amplifier and HuT. On the other hand, for the purpose of representing the power components that are emulated in DRTS with higher

power rating than that of the physical HuT, current scaling ratio is employed to scale up the hardware side current before it is sent to DRTS side. The voltage and current scaling ratios are given by,

$$r_v = \frac{V_{\text{Hnom}}}{V_{\text{S}'\text{nom}}}, \tag{4.1a}$$

$$r_i = \frac{I_{\text{S}'\text{nom}}}{I_{\text{Hnom}}} = \frac{S_{\text{S}'\text{nom}}/V_{\text{S}'\text{nom}}}{S_{\text{Hnom}}/V_{\text{Hnom}}}, \tag{4.1b}$$

where V_{Hnom} is the nominal voltage of the physical HuT, $V_{\text{S}'\text{nom}}$ is the nominal voltage of the emulated HuT at the simulation side, S_{Hnom} is the nominal power rating of the physical HuT, and $S_{\text{S}'\text{nom}}$ represents the nominal power rating of the emulated power component in the simulation side.

4.1.2 Switched-Mode Power Amplifier with LC Filter

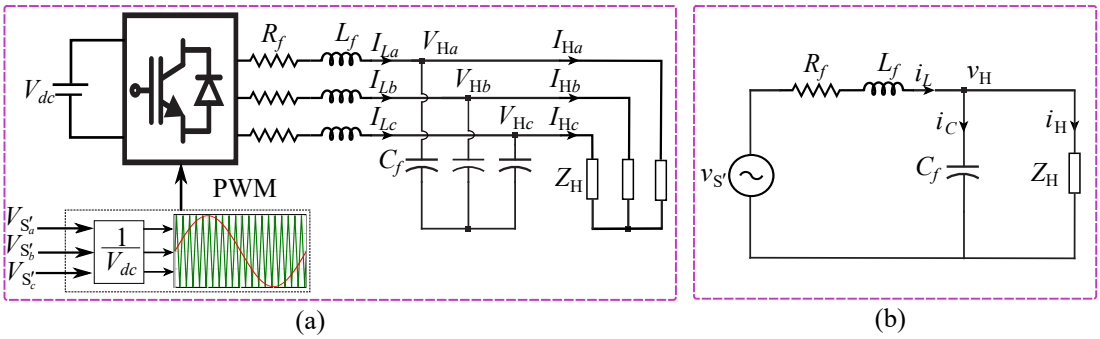

Figure 4.3: (a) Switched-mode VSC with open-loop control and LC output filter, and (b) its small-signal equivalent per-phase schematic.

Figure 4.3(a) represents the open-loop controlled switched-mode VSC-based power amplifier (Cell 5 within Figure 4.1), which is modelled as a voltage source converter with passive output filters and controlled via Pulse Width Modulation (PWM). The LC output filters are implemented to eliminate high-frequency switching harmonics stemming from high-frequency pulsating modulation, and its cut-off frequency should be tuned to be at least a decade lower than the

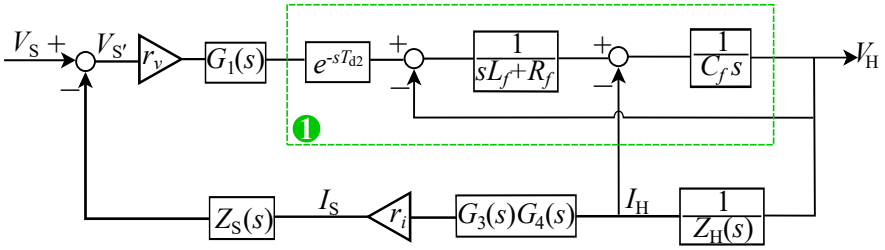

Figure 4.4: Equivalent block diagram of the PHIL system in a single-phase basis.

switching frequency. Figure 4.3(b) illustrates the small-signal equivalent single-phase diagram of the VSC coupled with the physical HuT. Correspondingly, the equivalent block diagram of the open-loop controlled switched-mode power amplifier with LC filter is shown in the cell 1 within Figure 4.4 and its transfer function is given by,

$$G_2'(s) = \frac{V_{\mathrm{H}}}{V_{\mathrm{S}''}} = e^{sT_{\mathrm{d2}}} G_f(s), \tag{4.2}$$

where T_{d2} (i.e., 1.5 times the sampling period of VSC control) is the equivalent time delay of the PWM modulation and its computation, $G_f(s)$ represents the equivalent transfer function of output filter and HuT impedance and is given by,

$$G_f(s) = \frac{1}{L_f C_f s^2 + (R_f C_f + \frac{L_f}{Z_{\mathrm{H}}})s + (1 + \frac{R_f}{Z_{\mathrm{H}}})}, \tag{4.3}$$

where R_f is the parasitic resistance of inductor, L_f and C_f are the inductance and capacitance of output filter respectively, and Z_{H} is the equivalent HuT impedance.

Multiplying the numerator and denominator of Eq. (4.3) with Z_{H}, it is further expressed as,

$$G_f(s) = \frac{Z_{\mathrm{H}}}{L_f C_f Z_{\mathrm{H}} s^2 + (R_f C_f Z_{\mathrm{H}} + L_f)s + (Z_{\mathrm{H}} + R_f)}, \tag{4.4a}$$

$$G_f(s) = K\frac{\prod_{i=1}^{m}(s - z_i)}{\prod_{i=1}^{n}(s - p_i)},\ m = n - 2\ , \tag{4.4b}$$

where K is the transfer function gain.

Some typical examples of the equivalent transfer functions as in Eq. (4.4a) with different HuT impedance are presented in Appendix B. Convert the numerator-denominator polynomials in Eq. (4.4a) to a rational transfer function in a factored zero-pole form as given by Eq. (4.4b). Apparently, the numerators of Eq. (4.4a) and its equivalent in Eq. (4.4b) are two order less than their denominators.

It is evident from Eq. (4.2) and Eq. (4.4a) that the output voltage V_{H} is affected by the filter characteristics and the HuT impedance under different load scenarios as shown in Appendix B. A compensation strategy as elaborated in the following section is required to ensure high-precision power signal amplification.

4.2 Analysis of PHIL System with Open-Loop Controlled VSC-Based Power Amplifier

This section explains the effects of the power amplifier and the loop time delay on the stability, the signal synchronisation accuracy, and the transparency of power transfer of the PHIL simulation. It is worth noting that the remaining components in Figure 4.2 are modelled by analogy with these presented in Eq. (2.2) in Chapter 2.2.

4.2.1 PHIL System Stability

As the power signal scaling ratios are applied to the PHIL setup, the open-loop transfer function of the PHIL setup as presented in Figure 4.2 is represented as,

$$T_{\mathrm{O}}^{'}(s) = \underbrace{r_v r_i G_1(s) G_2^{'}(s) G_3(s) G_4(s)}_{G_{\mathrm{PI}}^{'}(s)} \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)} = \underbrace{G_{\mathrm{PI}}^{'*}(s) e^{-sT_{\mathrm{d}}}}_{G_{\mathrm{PI}}^{'}(s)} \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)}, \tag{4.5}$$

where $G_1(s)$, $G_3(s)$, and $G_4(s)$ are the equivalent transfer functions of the interfacing components as defined in Eq. (2.1), $G_2^{'}(s)$ is the transfer function of the open-loop controlled power amplifier as given in Eq. (4.2), T_{d} is the aggregated loop time delay given by Eq. (2.3), and $G_{\mathrm{PI}}^{'*}(s)$ represents the delay-free part of the power interface $G_{\mathrm{PI}}^{'}(s)$.

Applying the stability criterion as presented in Chapter 2.3.1 to the closed-loop system characteristic equation that is given by,

$$1 + G_{\mathrm{PI}}^{'}(s) \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)} = 1 + G_{\mathrm{PI}}^{'*}(s) e^{-sT_{\mathrm{d}}} \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)} = 0. \tag{4.6}$$

The PHIL system closed-loop stability can be determined by assessing the gain margin (GM) and phase margin (PM) as elaborated in Chapter 2.3.1. The closed-loop stability is guaranteed under the condition that the open-loop transfer function satisfies the following criteria,

$$\begin{cases} \mathrm{GM} = 0 - 20log(\left| G_{\mathrm{PI}}^{'*}(j\omega_{\mathrm{cp}}^{'}) e^{-j\omega_{\mathrm{cp}}^{'} T_{\mathrm{d}}} \frac{Z_{\mathrm{S}}(j\omega_{\mathrm{cp}}^{'})}{Z_{\mathrm{H}}(j\omega_{\mathrm{cp}}^{'})} \right|), & \exists\, \mathrm{GM} > 0, \\ \mathrm{PM} = \angle \left[G_{\mathrm{PI}}^{'*}(j\omega_{\mathrm{cg}}^{'}) \frac{Z_{\mathrm{S}}(j\omega_{\mathrm{cg}}^{'})}{Z_{\mathrm{H}}(j\omega_{\mathrm{cg}}^{'})} \right] - \angle(\omega_{\mathrm{cg}}^{'} T_{\mathrm{d}}) - (-180^{\circ}), & \exists\, \mathrm{PM} > 0, \end{cases} \tag{4.7}$$

where $\omega_{\mathrm{cg}}^{'}$ is the gain crossover frequency at which the magnitude of $T_{\mathrm{O}}^{'}(s)$ is 0 dB, $\omega_{\mathrm{cp}}^{'}$ is the phase crossover frequency at which the phase of $T_{\mathrm{O}}^{'}(s)$ crosses -180°.

As the time delay presents unity magnitude, the gain crossover frequency w_{cg} and the gain margin that defines the upper limit of the system magnitude variance before it raises above unity, are determined by the magnitude of power signal scaling ratio (r_v and r_i) and delay-free part of the power interface $\left| G_{\mathrm{PI}}^{'}(s) \right|$.

As shown in Eq. (4.7), the phase lag stemming from the power amplifier output filter, the signal processing units (as given in Eq. (2.1)), and the loop time delay degrades the PHIL system stability margin as a result of the reduced phase margin, a factor that indicates the system stability tolerance to phase lag [50].

4.2.2 PHIL Signal Synchronisation Accuracy Analysis

With the power signal scaling ratios taken into account, the closed-loop transfer function between the hardware side voltage $V_{\mathrm{H}}(s)$ and the equivalent software side voltage source $V_{\mathrm{S}}(s)$ of a delay-free ideal PHIL setup with unity-gain and infinite bandwidth is given by,

$$T_{\mathrm{C}}^{\mathrm{id}'}(s) = \frac{V_{\mathrm{H}}}{V_{\mathrm{S}}} = \frac{r_v Z_{\mathrm{H}}(s)}{r_v r_i Z_{\mathrm{S}}(s) + Z_{\mathrm{H}}(s)}. \tag{4.8}$$

However, the closed-loop transfer function between the hardware side voltage $V_{\mathrm{H}}(s)$ and software side voltage $V_{\mathrm{S}}(s)$ of the PHIL setup as in Figure 4.2 is

$$T_{\mathrm{C}}'(s) = \frac{V_{\mathrm{H}}}{V_{\mathrm{S}}} = \frac{r_v G_1(s) G_2'(s)}{1 + T_{\mathrm{O}}'(s)}. \tag{4.9}$$

Due to the non-unity magnitude and the phase lag arising from the interfacing components, the phase and magnitude relationship between V_{H} and V_{S} are not aligned with that defined in Eq. (4.8). With accurate modelling of the system components as defined in Eq. (2.2) and Eq. (4.2), the accuracy of PHIL setup in this chapter can be quantitatively analysed by employing the relative error $\epsilon(s)$ that is given by Eq. (2.15).

On the other hand, being proportional to the frequency of input power signal, the phase shift caused by the loop time delay and power amplifier filter, and the non-unity magnitude characteristic of the passive output filter distort the phase relationship between the voltage and current, and deteriorate the power transfer

between DRTS platform and HuT.

By applying the power signal scaling ratios to the PHIL setup that presents unity magnitude and zero phase lag in Chapter 2.4.2, the apparent power transferred between the simulation side ($S_{\mathrm{S}'}$) and hardware (S_{H}) over a certain frequency w_k in Eq. (2.16) can be further expressed as,

$$\begin{cases} S_{\mathrm{S}'} = & |V_{\mathrm{S}'} I_{\mathrm{S}}| \angle\theta_{\mathrm{S}'} & = & P_{\mathrm{S}'} + jQ_{\mathrm{S}'}, \\ S_{\mathrm{H}} = & |V_{\mathrm{H}} I_{\mathrm{H}}| \angle\theta_{\mathrm{H}} & = & P_{\mathrm{H}} + jQ_{\mathrm{H}}, \\ = & r_v r_i^{-1} |V_{\mathrm{S}'} I_{\mathrm{S}}| \angle\theta_{\mathrm{H}} & = & r_v r_i^{-1}(P_{\mathrm{S}'} + jQ_{\mathrm{S}'}), \end{cases} \tag{4.10}$$

where $\theta_{\mathrm{S}'}$ is power factor angle at the simulation side (i.e., $\angle V_{\mathrm{S}'} - \angle I_{\mathrm{S}}$), θ_{H} is power factor angle at the hardware side (i.e., $\angle V_{\mathrm{H}} - \angle I_{\mathrm{H}}$), and $\theta_{\mathrm{S}'} = \theta_{\mathrm{H}}$.

Applying the same derivation procedures given by Eq. (2.17) to Eq. (2.22), the active and reactive power at the hardware side of the PHIL setup in this chapter can be further expressed as,

$$\begin{cases} \hat{P}_{\mathrm{H}} = & r_v r_i^{-1} \left| G'_{\mathrm{PI}}(s) \right| (\hat{P}_{\mathrm{S}'} cos\varphi - \hat{Q}_{\mathrm{S}'} sin\varphi), \\ \hat{Q}_{\mathrm{H}} = & r_v r_i^{-1} \left| G'_{\mathrm{PI}}(s) \right| (\hat{Q}_{\mathrm{S}'} cos\varphi + \hat{P}_{\mathrm{S}'} sin\varphi), \end{cases} \tag{4.11}$$

where $\angle\varphi$ represents the difference between the power factor angle at the hardware side (i.e., $\hat{\theta}_{\mathrm{H}} = \angle\hat{V}_{\mathrm{H}} - \angle\hat{I}_{\mathrm{H}}$) and the power factor angle at the simulation side (i.e., $\hat{\theta}_{\mathrm{S}'} = \angle\hat{V}_{\mathrm{S}'} - \angle\hat{I}_{\mathrm{S}}$).

It is obvious from Eq. (4.11) that the actual power transfer within the PHIL setup is not aligned with the power transfer defined in Eq. (4.10). This difference results from the non-unity magnitude $\left| G'_{\mathrm{PI}}(w_k) \right|$ and the phase lag φ stemming from the power amplifier output filter, the signal processing unit (i.e., low-pass filter), and the aggregated loop time delay. These lead to distorted power transfer transparency between the simulation side and hardware side.

4.3 PHIL Interface Compensation Schemes

This section presents a comprehensive assessment of the interface compensation methods that are proposed in the literature. This is followed by an in-depth explanation of the proposed compensation method from the aspects of power amplifier non-unity characteristic compensation and the loop phase lag compensation.

4.3.1 Power Amplifier Compensator

As discussed in Section 4.2, the non-ideal power interface, in particular the power amplifier output filters and the loop time delay, distort the transparent power transfer between the simulation side and hardware side. The high reconfigurability of the software within PHIL enables the flexibility to implement compensation blocks at the PCC in simulation platform. As shown in Figure 4.1, the compensation units can be implemented in the software side to process the voltage and current signals before they are applied in the feed-forward and feedback paths of the PHIL closed-loop.

For most scenarios, the passive elements within the power interface and the HuT provide sufficient damping to mitigate the resonance of the output filter. On the contrary, for the passive filter in Eq. (4.4a) whose poles are lightly damped, the notch filter is an option to compensate for the resonance by placing additional zeros near the resonate poles, thereby cancelling the associated resonant transient [50]. The notch filter is given by,

$$G_{notch} = \frac{s^2 + 2r\zeta_n w_n s + w_n^2}{s^2 + 2\zeta_n w_n s + w_n^2}, \tag{4.12}$$

where w_n is the centre notch frequency, ζ_n is the damping ratio of the notch filter that determines the sharpness of notch filter response and its notch width, and r is the filter gain at the notch frequency that determines the notch depth.

The resonant peak in Eq. (4.4a) is compensated by tuning the notch frequency w_n to be equal to the resonant frequency w_r of the output filter, and tuning the filter gain r to be the same as that of the output filter in Eq. (4.4a) at w_r to cancel the resonant peak. As shown in Figure 4.5, the compensation for the resonance peak is achieved at the expense of more phase lag in the compensated filter, and the unity-gain of the compensated filter is only maintained over a certain frequency range that may not in the range of all the frequencies of interest for some typical PHIL testing scenarios.

The transfer functions of the lead-lag filters are given by,

$$\begin{cases} G_{lead}(s) &= \frac{\frac{\lambda s}{w_r}+1}{\frac{s}{\lambda w_r}+1}, \quad \lambda > 1, \\ G_{lag}(s) &= \frac{\frac{\lambda s}{w_r}+1}{\frac{s}{\lambda w_r}+1}, \quad 0 < \lambda < 1, \end{cases} \tag{4.13}$$

where w_r is the resonant frequency in Eq. (4.4a).

Lead or lag filters are both candidates to compensate for the non-ideal power interface in Eq. (4.4a). It is obvious from Figure 4.5 that the lead filter compensates for the phase lag by introducing a positive phase shift to the power amplifier while resulting in a higher resonant peak that deteriorates the closed-loop stability. The lag filter suppresses the resonant peak by degrading the gain of the passive filter, which is achieved at the expense of a larger phase lag to be compensated and reduce the overall bandwidth of the compensated filter. For both scenarios, the unity-gain magnitude response of the compensated filter is achieved only over a certain narrow frequency range.

In this chapter, a compensator $G_f^{comp}(s)$ is designed to compensate for the non-unity characteristics of the output filter over its bandwidth by inverting the denominator in Eq. (4.3) to the numerator of the proposed compensator $G_f^{comp}(s)$. Because the degree of the denominator is two times higher than that of the numerator in Eq. (4.4), a second-order denominator that has two poles is required

in $G_f^{comp}(s)$ to cancel the additional two zeros of the numerator in $G_f^{comp}(s)$. This not only enables the numerator and denominator of the compensated filter are of equal order but also makes the compensation block physically realisable. So the compensator $G_f^{comp}(s)$ is the inverse of $G_f(s)$ augmented with a second-order low-pass filter to ensure it is a proper transfer function, that is,

$$\begin{aligned} G_f^{comp}(s) = & \frac{G_f^{-1}(s)}{\frac{s^2}{(kw_r)^2}+2\frac{\zeta_{op}}{kw_r}s+1}, \\ = & \frac{L_fC_fs^2+(R_fC_f+\frac{L_f}{Z_H})s+(1+\frac{R_f}{Z_H})}{\frac{s^2}{(kw_r)^2}+2\frac{\zeta_{op}}{kw_r}s+1}, \end{aligned} \tag{4.14}$$

where k represents the ratio between the resonant frequency in the compensator to that of the transfer function in Eq. (4.3), ζ_{op} is the optimum damping ratio to be tuned in the compensator.

The transfer function of the equivalently compensated output filter can be further expressed as,

$$G_f^{'}(s) = G_f(s)G_f^{comp}(s) = \frac{1}{\frac{s^2}{(kw_r)^2}+2\frac{\zeta_{op}}{kw_r}s+1}. \tag{4.15}$$

In order to tune the compensated filter $G_f^{'}(s)$ to behave like a well-known second-order Butterworth filter with maximally flat magnitude response [50, 82], ζ_{op} is tuned as the optimal value $\frac{\sqrt{2}}{2}$ as in [82, 83], such that the bandwidth of $G_f^{'}(s)$ is k times the resonant frequency w_n. To make the compensated filter $G_f^{'}(s)$ with wider bandwidth than that of the uncompensated filter $G_f(s)$, k is tuned to be 3 in this chapter.

Figure 4.5 presents the frequency response of the compensator in Eq. (4.14) and the compensated output filter in Eq. (4.15). The compensated filter implemented with the compensator in Eq. (4.14) presents unity magnitude characteristic over a wider frequency range than that of the uncompensated filter. The power amplifier compensated by Eq. (4.14) presents a wider bandwidth than that

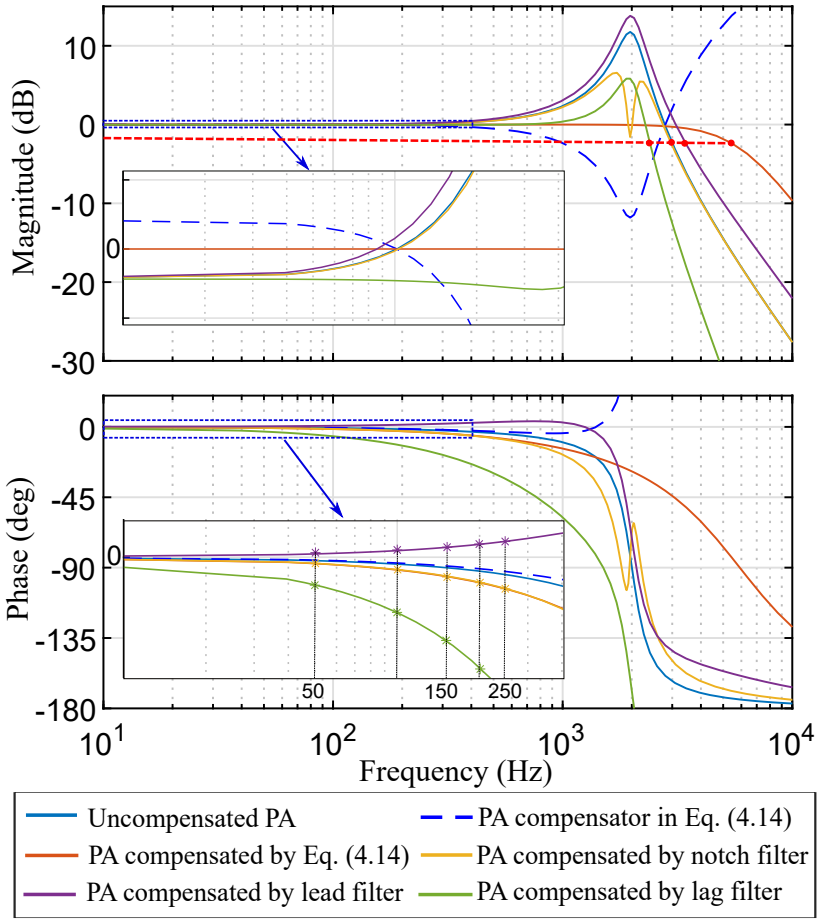

Figure 4.5: The frequency response of the uncompensated filter $G_f(s)$, compensator $G_f^{comp}(s)$ in Eq. (4.14), and the compensated filter $G_f'(s)$.

of the power amplifier compensated by a notch filter or lead-lag compensators. Note that, the implementation of the compensator in Eq. (4.14) is under the assumption that the parameters of the LC filter and the HuT impedance are known exactly, which is achievable by employing the system identification techniques as presented in Chapter 3.2 in the controlled and laboratory-based PHIL environment. However, if system's parameter information is not available or the filter in Eq. (4.3) has lightly damped complex poles whose locations cannot be estimated precisely, the conventional notch filter in Eq. (4.12) is an option to suppress the resonance and cancel the corresponding resonant transient.

Even though the compensated $G_f^{'}(s)$ presents a unity-magnitude characteristic over a wide range of frequencies, the phase lag introduced by this compensated filter is,

$$\angle G_f^{'}(s = jw) = tan^{-1}(\frac{\frac{2\zeta_{op} w}{kw_r}}{1 - \frac{w^2}{(kw_r)^2}}). \tag{4.16}$$

The phase lag significantly distorts the power signal and power transfer as discussed in Section 4.2. The compensation of these phase lags and the loop delay on a harmonic-by-harmonic basis is presented in the following section.

4.3.2 Loop Phase Lag Compensation

As analysed in Section 3.2.1, SDFT that is defined in Eq. (3.12b) can be envisioned as a N^{th} order comb filter in series with parallelised complex resonators. The frequency response of the comb-filter as illustrated in Figure 3.8 reveals its equivalence to the notch filter with notches periodically spaced at the fundamental and harmonic frequencies. It is evident from Figure 3.9, the single complex resonator designed for a specific frequency kf_0 is equivalent to a band-pass filter centred at the frequency kf_0 with a sharp cut-off amplitude, which enables it selectively amplifies the corresponding signal component. Consequently, as presented in Figure 3.10, the SDFT filter presents a linear phase and steep cut-off amplitude characteristics, which enable the selective update of the signal phase and amplitude characteristics over a wide range of frequencies without magnitude distortion and phase shift. This attribute paves a new pathway for compensating the time delay in the PHIL setup on a harmonics-by-harmonics basis by processing the power signal with multiple complex resonators based SDFT.

To guarantee the stability of SDFT in processing the power signal within the PHIL setup, the damping factor r is applied to the SDFT filter as given by

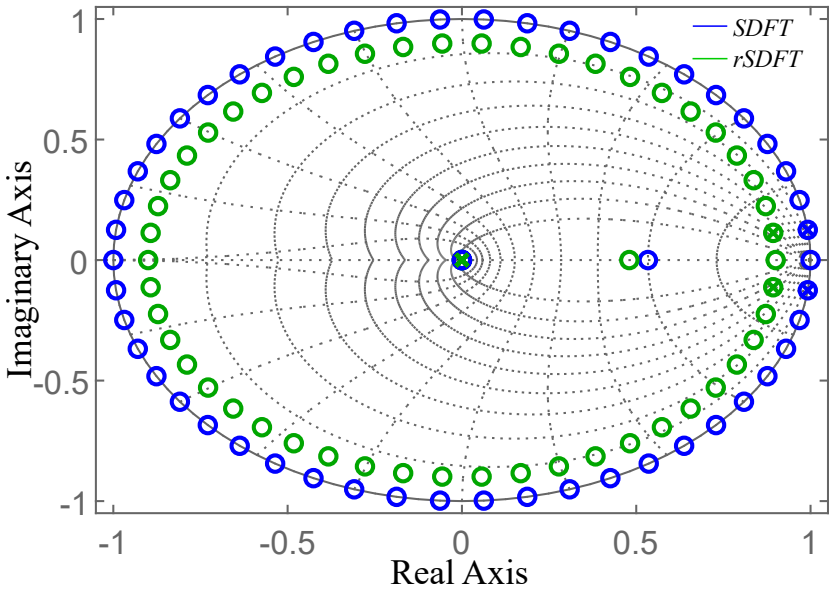

Figure 4.6: Zero-Pole maps of SDFT and rSDFT with damping factor r, $(r = 1 - \varepsilon)$.

Eq. (3.12b) [68, 70]. The stability-enhanced SDFT filter is given by,

$$H_{\mathrm{rSDFT}}(z) = \underbrace{(1 - r^N z^{-N})}_{\text{Comb filter}} \underbrace{\sum_{k=1}^{N} \frac{e^{j\frac{2\pi k}{N}}}{1 - r z^{-1} e^{j\frac{2\pi k}{N}}}}_{\text{Complex resonators}}, \tag{4.17}$$

where $N\,(N = \frac{f_s}{f_0})$ is the window size, f_s is the sampling frequency, f_0 is the fundamental frequency, and $k\,(k = 1, 2, 3, \cdots, N)$ represents the order of the resonators.

As shown in Figure 4.6, the damping factor r that is given by $(r = 1 - \varepsilon)$, where ε is an infinitesimally small positive quantity, forces the zeros or poles of rSDFT to be located within the unity circle with radius r.

Based on the rSDFT filter with multiple parallelised complex resonators designed for the frequencies of interest, a scaling factor $\frac{1}{N}$ is implemented at the output of each single resonator to mitigate the overflow error and maintain the unity gain of the rSDFT filter, of which the phase of each harmonic updates over every sampling period.

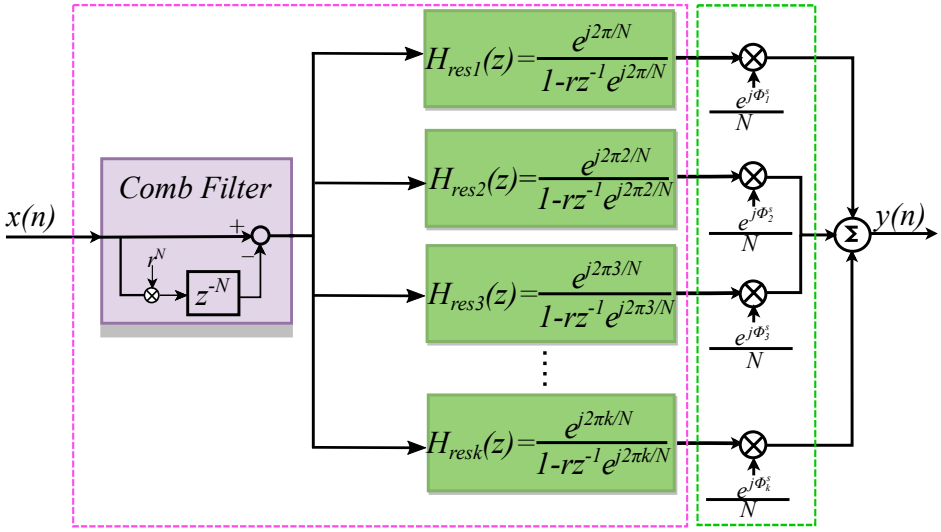

Figure 4.7: The block diagram of the rSDFT with complex resonator banks and harmonic-by-harmonic time delay compensations.

Figure 4.7 presents the block diagram of the rSDFT-based phase lag compensation filters. To compensate for the phase lags of the compensated filter in Eq. (4.16) and the aggregated loop time delay, an additional phase shift Φ_k^s is implemented at the output of the resonator with resonant frequency kw_0. The rSDFT filter implemented with additional phase shift can be expressed as,

$$H_{\text{rSDFT}}^{comp}(z) = (1 - r^N z^{-N}) \frac{1}{N} \sum_{k=1}^{N} \frac{e^{j\frac{2\pi k}{N}} e^{j\Phi_k^s}}{1 - rz^{-1} e^{j\frac{2\pi k}{N}}}, \tag{4.18}$$

where

$$\Phi_k^s = kw_0 T_{dff} + \angle G_f'(kw_0). \tag{4.19}$$

The phase addition method that is applied to the output of each single complex resonator enables phase lag compensation without signal magnitude distortion on a harmonic-by-harmonics basis. This can mitigate the detrimental impact of the time delay on the power transfer transparency and enable accurate replication of the HuT dynamics in DRTS side.

4.4 Case Study and Simulation Results

This section presents an analytical frequency-domain assessment of the interface compensation methods that are proposed in the literature and the proposed compensation schemes in this chapter. This is followed by the validation of the proposed interface compensation scheme and the time delay compensation method regarding their functionalities in improving the power signal synchronisation accuracy and the power transfer transparency of the PHIL setup.

Matlab/Simulink simulation models are utilised to verify the effectiveness of the proposed compensation method. Table 4.1 tabulates the parameters of the PHIL setup in Figure 4.1. A voltage source inverter with ideal semiconductor switches is employed as the power amplifier. The LC filters parameters are calculated by tuning their cut-off frequency to be equal to $f_{sw}/10$. The voltage divider topology is emulated in DRTS side and the HuT is emulated as an inductive hardware component.

The scaled voltage signal $r_v\hat{V}_{\mathrm{S}'}$ that is to be amplified by the power amplifier, the voltage signal $\hat{V}_{\mathrm{H}}$ at the HuT side, the power factor angle θ, the scaled active power and scaled reactive power at both of the simulation and hardware side are employed to assess the performance of the compensation method. Accuracy metrics that are defined by the relative average error η and the signal tracking error in Eq. (2.24) and Eq. (2.25) are leveraged to quantify the accuracy of power signal amplification and the transparency of power transfer between the simulation side and the HuT side at steady-state.

4.4.1 Evaluation of Different Compensation Strategies

This section compares the performances of the compensation schemes presented in Section 4.3.1 from the perspective of their frequency response characteristics and the closed-loop stability of the compensation schemes-based PHIL setups.

Table 4.1: PHIL system parameters for analysis and simulations.

Description	**Symbol**	**Value**
PHIL setup		
Nominal HuT resistance	R_{H}	$2\,\Omega$
Nominal HuT inductance	L_{H}	1 mH
Naturally coupled DRTS resistance	R_{S}	$0.5\,\Omega$
Naturally coupled DRTS equivalent voltage	V_{S}	4.26 kV
Naturally coupled DRTS inductance	L_{S}	2 mH
PHIL system fundamental frequency	f_0	50 Hz
PHIL system feed-forward path time delay	T_{dff}	450 µs
PHIL system feed-back path time delay	T_{dfb}	50 µs
Nominal power rating of the emulated HuT	$S_{\mathrm{S}'nom}$	62.5MVA
Nominal power rating of the physical HuT	$S_{\mathrm{H}nom}$	100kVA
Nominal voltage of the emulated HuT	$V_{\mathrm{S}'nom}$	15 kV
Nominal voltage of the physical HuT	$V_{\mathrm{H}nom}$	600 V
Voltage scaling ratio	r_v	0.04
Current scaling ratio	r_i	25
Power amplifier		
Direct Current (DC) voltage	V_{DC}	1000 V
Switching frequency	f_{sw}	20 kHz
Sampling frequency	f_s	40 kHz
Filter inductance	L_f	0.054 mH
Filter parasitic resistance	R_f	6.8 mΩ
Filter capacitor	C_f	117 µF

Table 4.2: Magnitude (in abs), phase (in deg), and bandwidth (in Hz) of the uncompensated output filter and the output filter compensated by the proposed compensator, notch filter, lead filter, and lag filter.

Compensator	**Filter in Eq. (4.3)**	**Compensator in Eq. (4.14)**	**Notch filter**	**Lead filter**	**Lag filter**
Mag at f_0	0.9944	1.0000	0.9943	0.9946	0.9941
Phase at f_0	-0.2744	-0.6707	-0.7687	0.4368	-1.5547
Mag at $5f_0$	1.0030	1.0000	1.0020	1.0088	0.9955
Phase at $5f_0$	-0.2402	-3.3556	-2.7473	3.2852	-6.6068
Bandwidth	3118.2	6033.1	3049.5	3561.3	2729.5

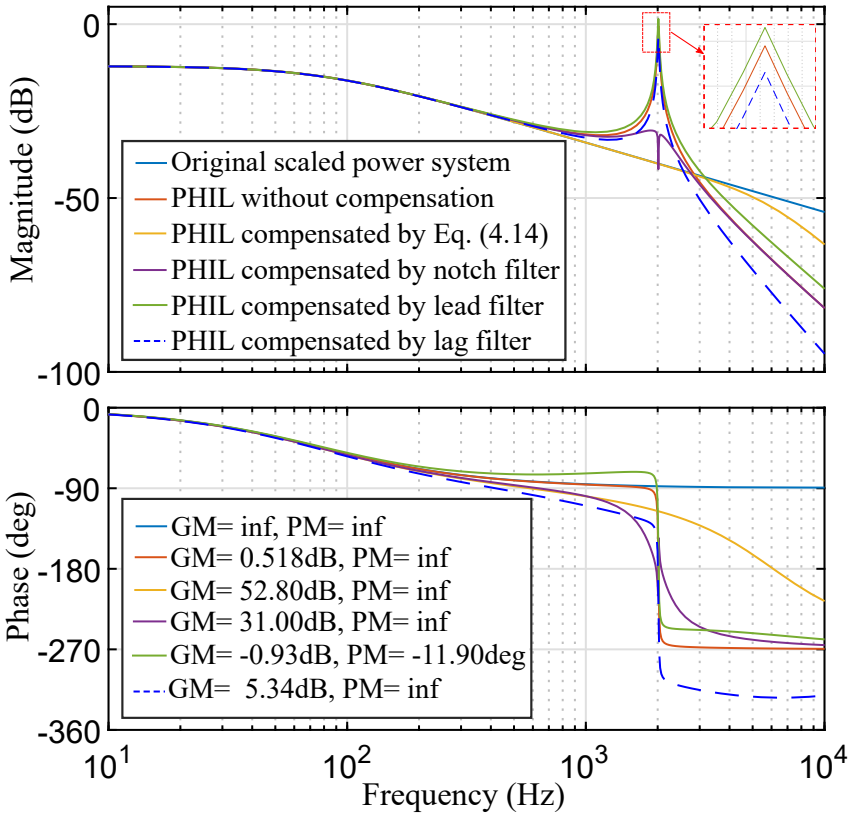

Figure 4.8: Bode plot of the open-loop transfer functions of the original scaled power system, uncompensated PHIL system, and the PHIL system compensated by the compensators as shown in the legend.

Table 4.2 presents the frequency responses of the original uncompensated power amplifier filter and that of the power amplifiers that are compensated by different compensators. The non-unity magnitude of the power amplifier output filter in Eq. (4.3) is compensated to be unity by implementing the proposed compensator in Eq. (4.14) in this chapter over the fundamental frequency and other harmonics components. This results from the optimal setting of the damping factor in Eq. (4.14) to make the compensated filter present a flat unity magnitude response over a wide range of frequencies. However, the magnitudes of the power amplifier compensated by the notch filter, lead filter, and lag filter are non-unity at the fundamental frequency and other harmonic components, which inevitably distort the reference power signal to be amplified. Note that the phase lags of the

power amplifier compensated by notch filter, lag filter, and the proposed compensator in Eq. (4.14) are much larger than that of the original uncompensated power amplifier. The bandwidth of power amplifier compensated by Eq. (4.14) is higher than that of the uncompensated power amplifier and the power amplifier compensated by notch filter, lead filter, and lag filter. This is attributed to the optimal tuning of the ratio factor k in Eq. (4.14).

Figure 4.8 presents the frequency responses of the open-loop transfer function of the uncompensated and compensated PHIL systems. The resonance of uncompensated PHIL system is compensated by implementing the compensator in Eq. (4.14). Notice that the magnitude characteristic of the PHIL system compensated by Eq. (4.14) is aligned with that of the original scaled power system because the compensated power amplifier presents unity gain over a certain frequency range. The notch filter and lag filter are also effective in suppressing the resonance of PHIL system, of which the stability margins are lower than that of the PHIL system compensated by Eq. (4.14). Even though the lead filter compensates for phase lag to some extent, it can destabilise the PHIL system, in particular the marginally stable PHIL system or the PHIL system with low stability margins. This is because the lead filter causes the magnitude of the compensated PHIL system to exceed unity and the resonance frequency to be greater than the gain-crossover frequency w_{cg} as defined in Eq. (4.7).

4.4.2 Accuracy Evaluation of the Proposed Compensation Method

This section evaluates the performance of the proposed method regarding its capability in improving the power signal synchronisation and enhancing the power transfer transparency in the PHIL closed-loop configuration. Accuracy metrics are employed to evaluate the following cases:

1. Original scaled SoI.
2. PHIL system without compensation.
3. PHIL system with loop time delay compensation only.
4. PHIL system with compensation proposed in this chapter.

Table 4.3 presents the power signal tracking error metrics. Due to the non-unity gain of the power amplifier as described in Table 4.2, the loop time delay, and the phase lag of power amplifier output filter, the Root Mean Square (RMS) voltage and power factor angle tracking errors are significant for the PHIL system without proper compensation in Case 2 and Case 3. Notice that even the loop delay is compensated in Case 3, there still exists a power factor angle tracking error due to the phase lag of the power amplifier output filter in Eq. (4.16). Because the compensation method proposed in this chapter maintains the unity gain of the power amplifier and takes both the loop time delay and the phase lag of the power amplifier output filter into consideration, as shown in Case 4, the PHIL system compensated by the proposed method presents remarkably improved power signal tracking capabilities regarding the RMS voltage, power factor angle, and the active power and reactive power.

Table 4.3: Power signal tracking error metrics of different cases at the fundamental frequency f_0.

Case	$\hat{V}_{\mathrm{H}}$ ($\mathrm{V_{RMS}}$)	$r_v\hat{V}_{\mathrm{S}'}$ ($\mathrm{V_{RMS}}$)	η_{VT}	$\hat{\theta}_{\mathrm{H}}$ (deg)	$\hat{\theta}_{\mathrm{S}'}$ (deg)	$\eta_{\theta T}$	$\hat{P}_{\mathrm{H}}$ (kW)	$r_v r_i^{-1}\hat{P}_{\mathrm{S}'}$ (kW)	η_{PT}	$\hat{Q}_{\mathrm{H}}$ (kvar)	$r_v r_i^{-1}\hat{Q}_{\mathrm{S}'}$ (kvar)	η_{QT}
1	143.84	143.84	0.00%	32.14	32.14	0.00%	7.417	7.417	0.00%	4.660	4.660	0.00%
2	145.47	146.29	0.56%	32.14	42.09	23.64%	7.586	6.686	13.46%	4.766	6.039	21.08%
3	143.35	144.17	0.57%	32.14	33.10	2.99%	7.367	7.331	0.49%	4.629	4.777	3.10%
4	143.84	143.84	0.00%	32.14	32.14	0.00%	7.417	7.417	0.00%	4.660	4.660	0.00%

Table 4.4: PHIL power signal to reference power signal error metrics of different cases at the fundamental frequency f_0.

Case	$\hat{V}_{\mathrm{H}}$ ($\mathrm{V_{RMS}}$)	$\eta_{V_{\mathrm{H}}}$	$r_v\hat{V}_{S'}$ ($\mathrm{V_{RMS}}$)	$\eta_{V_{\mathrm{S}'}}$	$\hat{\theta}_{\mathrm{S}'}$ (deg)	$\eta_{\theta_{\mathrm{S}'}}$	$\hat{P}_{\mathrm{H}}$ (kW)	$\eta_{P_{\mathrm{H}}}$	$r_v r_i^{-1}\hat{P}_{\mathrm{S}'}$ (kW)	$\eta_{P_{\mathrm{S}'}}$	$\hat{Q}_{\mathrm{H}}$ (kvar)	$\eta_{Q_{\mathrm{H}}}$	$r_v r_i^{-1}\hat{Q}_{\mathrm{S}'}$ (kvar)	$\eta_{Q_{\mathrm{S}'}}$
1	143.84	0.00%	143.84	0.00%	32.14	0.00%	7.417	0.00%	7.417	0.00%	4.660	0.00%	4.660	0.00%
2	145.47	1.13%	146.29	1.70%	42.09	30.96%	7.586	2.28%	6.686	9.86%	4.766	2.27%	6.039	29.59%
3	143.35	0.34%	144.17	0.23%	33.10	2.99%	7.367	0.67%	7.331	1.16%	4.629	0.67%	4.777	2.51%
4	143.84	0.00%	143.84	0.00%	32.14	0.00%	7.417	0.00%	7.417	0.00%	4.660	0.00%	4.660	0.00%

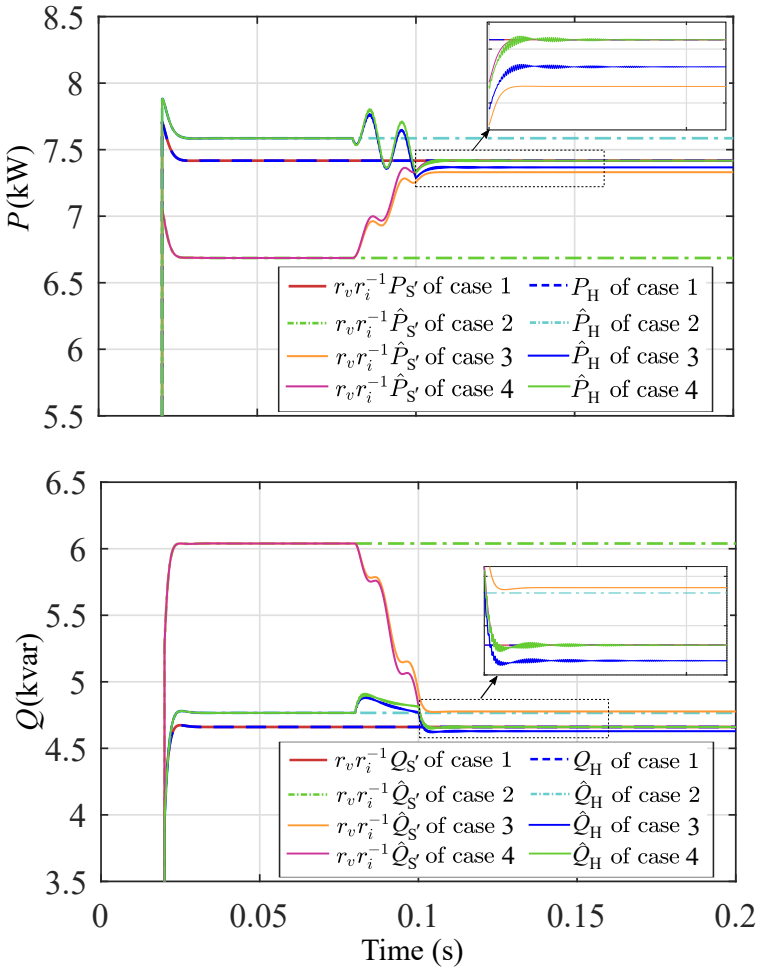

Figure 4.9: Active power and reactive power at the simulation and HuT side of the scaled voltage divider system and PHIL system.

Table 4.4 and Figure 4.9 present the steady-state PHIL power signal to reference signal error metrics and the active and reactive power behaviours under the pre-defined cases, respectively. The compensation blocks are implemented at $t = 0.08$s in Case 3 and Case 4. As a result of the non-unity magnitude of power amplifier and the phase lags in the closed-loop, the errors of the voltage and power factor angle between the PHIL system and the original scaled power system are also remarkable in Case 2 and Case 3. As shown in Figure 4.9, there are significant mismatches between the power signal at the simulation and hard-

ware sides (i.e., $\hat{P}_{\mathrm{H}} > r_v r_i^{-1} \hat{P}_{\mathrm{S}'}$ and $\hat{Q}_{\mathrm{H}} < r_v r_i^{-1} \hat{Q}_{\mathrm{S}'}$) for the PHIL system without compensation. These mismatches result from the loop phase lag and the non-unity magnitude of the power amplifier as explained in Eq. (4.11). Note that the active and reactive power differences between the PHIL system in Case 3 and the original scaled power system are also remarkable even when the loop time delay is compensated. After implementing the proposed compensation method, the active power and reactive power of the PHIL system in Case 4 are aligned with that of the reference power system and the power transfer within this PHIL system is as transparent as that of the reference SoI system in Case 1.

4.5 Summary

To mitigate the deteriorating impact of time delay and non-unity power interface on the PHIL accuracy and to extend the bandwidth of the power interface, this chapter presents a compensation scheme for the open-loop controlled VSC-based power amplifier that enables more accurate power signal synchronisation and power transfer within the PHIL closed-loop simulation. This compensation method is designed to maintain the unity gain of the power amplifier over a wider range of frequencies via optimal tuning of the proposed compensator. In addition, the SDFT-based time delay compensation scheme compensates for the phase lag on a harmonic-by-harmonic basis. The advantages of this compensation method over the compensation techniques published in the literature have been demonstrated via frequency-domain analysis. The effectiveness of this compensation method has been evaluated and demonstrated via the proposed accuracy metrics and the simulation results. The PHIL simulation that is based on the proposed compensation method presents high power signal tracking capability, which is of great significance for a high-fidelity PHIL simulation.

Chapter 5

A Novel Scheme for Sensitivity Analysis of PHIL Setups

As presented in Chapter 2, PHIL setups are modelled as closed-loop systems consisting of a digital real-time simulator interfacing with the real-world hardware under test through a dedicated PI, which facilitates the conservation of instantaneous power as exists in the real-world system through natural coupling. A conventional PI that is typically comprised by a power amplifier, sensors, signal conversion cards, and filters, inevitably introduces non-ideal characteristics such as time delay, signal distortion, limited bandwidth, and external disturbances that are not existent in SoI to the PHIL simulation. From a system operation perspective, these non-ideal characteristics play crucial roles in PHIL system with respect to its stability and accuracy, while leading to the system performance being more susceptible to these non-ideal characteristics, in particular the external disturbances.

The impact of these non-ideal characteristics and the dynamics stemming from the PI on the PHIL system stability and accuracy has been extensively discussed in Chapter 2. Many research efforts have been devoted to improve the stability and accuracy of the PHIL simulation as summarised and assessed in Chapter 2.3

and Chapter 2.4. Detailed modelling principles, block diagrams, stability criteria, and accuracy metrics have been developed for the assessment of system properties involving the stability and accuracy.

Apart from the conventional stability and accuracy assessments of the PHIL simulation, a comprehensive analysis and assessment of the impact of external disturbances on the PHIL simulation is an important factor in PHIL setups before their final-stage deployment. Due to the implementation of the non-ideal PI, external disturbances are inevitably injected into the PHIL setup and are mainly stemmed from,

- Offset noise in the measurement units
- Quantisation error/noise in the ADC card
- Sensor measurement noise (typically high-frequency)
- Switching harmonics stemming from high-frequency pulsating modulation.

From an application point of view, comprehensive sensitivity analysis and assessment are crucial for a high-fidelity and robust PHIL simulation. In contrast to the well-presented schemes for stability and accuracy analysis and assessment in the literature, no sensitivity analysis scheme has been developed within the PHIL community. In this chapter, to facilitate quantitatively analysing and assessing the impact of external disturbances on PHIL simulation systems, a novel scheme for sensitivity analysis of the PHIL setups has been proposed for quantifying the sensitivity criteria. The main contributions of this chapter are summarised as follows,

1. A scheme based on detailed modelling was developed for the sensitivity analysis of PHIL setups using transfer functions describing the dynamic behaviours of SoI and the interfacing components within the PHIL setup.

2. The inherent relationship between stability, accuracy and sensitivity was elaborated and verified by the scheme through analytical assessment and experimental validation. This allows for a precise estimation of PHIL system properties prior to its deployment for experimental testing.

3. In conjunction with the sensitivity analysis criteria, practical accuracy assessment methods involving the Signal to Noise Ratio (SNR) and the Total Harmonic Distortion Plus Noise (THD+N) are presented to quantify the sensitivity, which can be easily and extensively applied to the practical PHIL experiments.

4. Based on the current-type ITM interface, the proposed scheme for sensitivity analysis was characterised and verified by experimental PHIL setups at the Dynamic Power Systems Laboratory at the University of Strathclyde, demonstrating its applicability for either simplified or complex power system and components testing.

The remainder of this chapter is structured as follows: Section 5.1 presents the detailed modelling of the PHIL system with V-ITM and Current-Type ITM (I-ITM) interfaces. Section 5.2 provides the in-depth details of the sensitivity analysis scheme from the aspects of modelling principles, sensitivity analysis metrics, and the inherent relationship between the sensitivity analysis metrics and the stability and accuracy of a PHIL setup. Analytical assessments of the proposed sensitivity analysis scheme and its key attributes are presented in Section 5.3, followed by a comprehensive experimental validation in Section 5.4. Section 5.5 summarises this chapter[1].

[1] This chapter is an extension of conference publications [23,32] and journal publication [43]

5.1 PHIL ITM Interfacing Methods

This section presents the state-of-the-art of voltage-type and current-type ITM interfacing methods with emphasis placed on the detailed modelling of the current-type ITM interface along with an in-depth explanation of its properties.

As analysed and assessed in Chapter 2.2.1, among the novel PHIL interfacing methods as tabulated in Table 2.1, the ITM interface is extensively adopted in the PHIL community because of its simplified implementing structure and its relatively good performance with respect to the stability and accuracy. Even though the proposed sensitivity analysis scheme could be extendable and applicable to other interface methods, the ITM interface will be utilised for the development of sensitivity analysis scheme throughout the chapter.

Determined by the type of power amplification and the controllable power sources implemented in DRTS and HuT side, ITM interface can be categorised as voltage-type (V-ITM) or current-type (I-ITM). Detailed modelling of these ITM interfaces are given in the following sections.

5.1.1 Voltage-Type ITM (V-ITM) Interface

As presented in Figure 2.2, the V-ITM is configured as a controlled voltage source in HuT side and a controlled current source in DRTS side, which are controlled by a voltage-type PA and current sensor, respectively. With the interfacing components, equivalent impedance in DRTS and HuT side, and interface signals represented in the form of a SISO closed-loop system, the equivalent V-ITM block diagram is presented in Figure 2.3. To support the development of the sensitivity analysis scheme, the V-ITM open-loop transfer function given by Eq. (2.1) is further expressed as,

$$T_{\mathrm{O}}^{\mathrm{v}}(s) = \underbrace{G_1^{\mathrm{v}}(s)G_2^{\mathrm{v}}(s)}_{C_{\mathrm{v}}(s)} \frac{Z_{\mathrm{S}}(s)}{Z_{\mathrm{H}}(s)} \underbrace{G_3^{\mathrm{v}}(s)G_4^{\mathrm{v}}(s)}_{P_{\mathrm{v}}(s)}, \tag{5.1}$$

where $Z_{\mathrm{S}}(s)$ and $Z_{\mathrm{H}}(s)$ are the equivalent impedance of the power network within the DRTS platform and the HuT, respectively. $C_{\mathrm{v}}(s)$ is the transfer function of the power interface in feed-forward path comprising the transfer functions of DAC card $G_1^{\mathrm{v}}(s)$ and voltage-type power amplifier $G_2^{\mathrm{v}}(s)$. $P_{\mathrm{v}}(s)$ is the transfer function of the power interface in feedback path comprising the transfer functions of current sensor $G_3^{\mathrm{v}}(s)$ and ADC card in series with LPF $G_4^{\mathrm{v}}(s)$.

5.1.2 Current-Type ITM (I-ITM) Interface

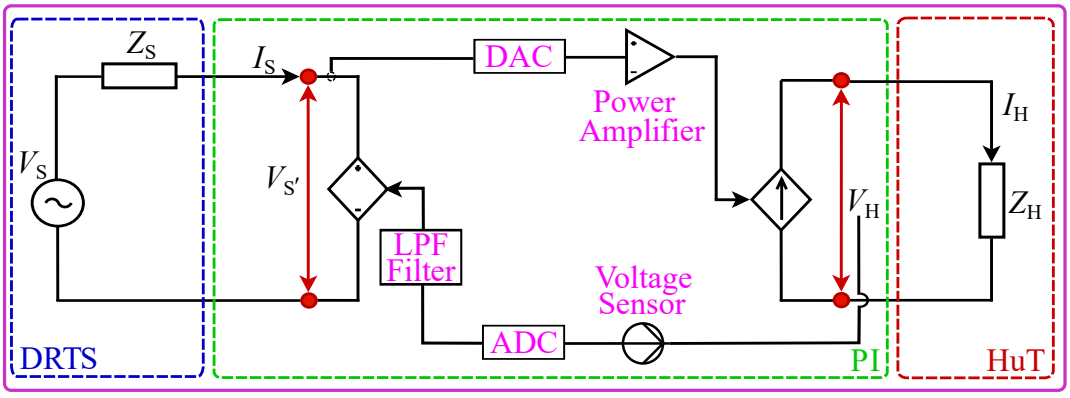

Figure 5.1: Equivalent model of the PHIL system with current-type ITM interface.

In contrast to the V-ITM interface, as illustrated in Figure 5.1, the I-ITM interface is configured as a controlled current source on the HuT side and a controlled voltage source on the DRTS side, which are controlled by a current-type PA and a voltage sensor, respectively. Figure 5.2 presents the equivalent SISO closed-loop block diagram of the I-ITM interface, whose open-loop transfer function $T_{\mathrm{O}}^{\mathrm{i}}(s)$ is given by,

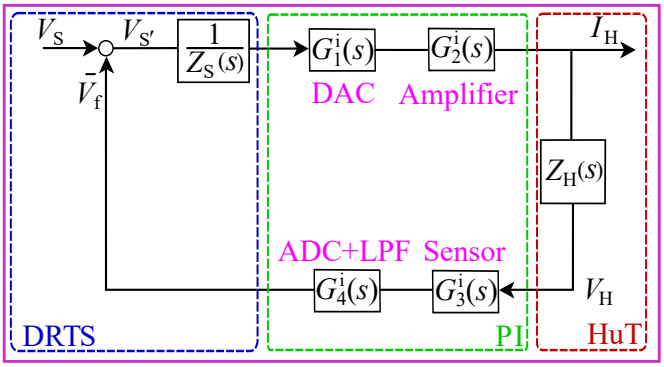

Figure 5.2: Equivalent block diagram of the I-ITM based PHIL system in Figure 5.1.

$$T_O^i(s) = \underbrace{G_1^i(s)G_2^i(s)}_{C_i(s)} \frac{Z_H(s)}{Z_S(s)} \underbrace{G_3^i(s)G_4^i(s)}_{P_i(s)}, \tag{5.2}$$

where $Z_S(s)$ and $Z_H(s)$ are the equivalent impedance of the power network within the DRTS platform and the HuT, respectively. $C_i(s)$ is the transfer function of the power interface in feed-forward path comprising the transfer functions of DAC card $G_1^i(s)$ and current-type power amplifier $G_2^i(s)$. $P_i(s)$ is the transfer function of the power interface in feedback path comprising the transfer functions of voltage sensor $G_3^i(s)$ and ADC card in series with LPF $G_4^i(s)$.

Based on the detailed modelling of the I-ITM interface and the open-loop transfer function of its equivalent SISO closed-loop system, the stability assessment criteria as presented in Chapter 2.3.1 and the stability margin assessment method as given by Eq. (2.9) can be applied to the open-loop transfer function defined in Eq. (5.2). The stability of I-ITM PHIL setup is constrained by the time delay and the impedance ratio between HuT side and DRTS side IR $= \frac{Z_H}{Z_S}$. Note that, in contrast to the V-ITM interface, the greater the impedance ratio between DRTS side and HuT side is, the more stable the system is. In terms of the accuracy assessment, the analytical accuracy assessment criteria defined in Eq. (2.15) as well as the accuracy metrics presented in Chapter 2.4.2 can be applied to the I-ITM interface through proper modifications.

5.2 Sensitivity Analysis Method for PHIL Setup

This section presents the proposed scheme for sensitivity analysis of PHIL setup. Initially, the modelling principles of PHIL system sensitivity analysis are explained followed by the derivations of sensitivity analysis metrics for V-ITM and I-ITM based PHIL setups. Eventually, the inherent relationships between the sensitivity analysis metrics of the proposed scheme and the stability and accuracy of PHIL setups are presented.

5.2.1 Modelling Principles for Sensitivity Analysis

A comprehensive sensitivity analysis of the external disturbances arising from the power interface of the PHIL systems is based on the derivation of sensitivity analysis metrics, which define the relationship between a specific disturbance and the signal of interest in frequency domain. The characteristics of sensitivity analysis metrics indicate the magnitude attenuation or amplification of the external disturbance over any frequency of interest and its respective phase shift. The disturbances stemming from the non-ideal PI within the PHIL setup affect the digital signals $V_{S'}$ and I_S as well as the analogue signals V_H and I_H on the interface. As shown in Figure 5.3 and Figure 5.4, the disturbance is identified according to its associated signal of interest and is denoted by the symbol δ as a prefix.

The generic definition of the sensitivity function $S_1(s)$ that is used to describe the relationship between the signal of interest (i.e., $V(s)$ or $I(s)$) and its associated local disturbances (i.e., $\delta V(s)$ or $\delta I(s)$) is given by,

$$S_1(s) = \begin{cases} \dfrac{V_{S'}(s)}{\delta V_{S'}(s)} = \dfrac{1}{1+T_O(s)}, \\ \dfrac{V_H(s)}{\delta V_H(s)} = \dfrac{1}{1+T_O(s)}, \\ \dfrac{I_S(s)}{\delta I_S(s)} = \dfrac{1}{1+T_O(s)}, \\ \dfrac{I_H(s)}{\delta I_H(s)} = \dfrac{1}{1+T_O(s)}. \end{cases} \tag{5.3}$$

Regardless of the type of signal of interest and the type of ITM interface, sensitivity analysis metric $S_1(s)$ are equivalent. In terms of the sensitivity function for other disturbances with respect to a specific signal, it can be derived in a similar manner as sensitivity analysis metric $S_1(s)$. The following sub-sections present the sensitivity analysis metrics for the voltage-type and current-type ITM interfaces.

5.2.2 Sensitivity Analysis Metrics for V-ITM PHIL Setup

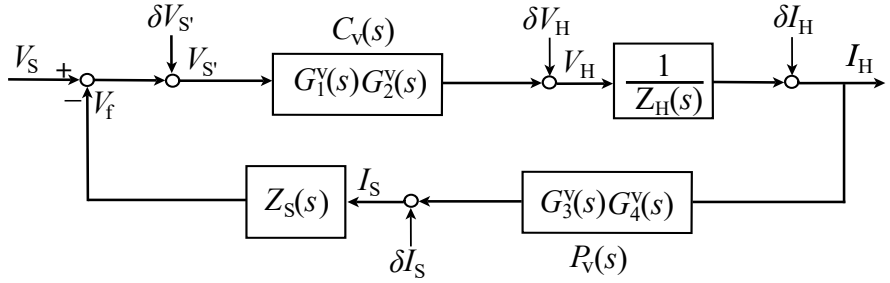

Figure 5.3: Block diagram of PHIL with V-ITM interface and disturbances arising from PI in a SISO closed-loop manner.

With the aforementioned disturbances incorporated into the PHIL closed-loop, Figure 5.3 presents the an extended representation of the equivalent block diagram of the V-ITM interface based PHIL setup in Figure 2.3. The hardware

side current response I_{H} that is fed back from HuT to DRTS is of great significance for investigating the characteristics of HuT and the interactions between HuT and DRTS. This represents the signal of interest of V-ITM interface and thus being employed for the sensitivity analysis. The sensitivity metrics for assessing the impact of various identified disturbances on the signal of interest I_{H} are defined as,

$$\begin{cases} S_1^{\mathrm{v}}(s) = \dfrac{I_{\mathrm{H}}(s)}{\delta I_{\mathrm{H}}(s)} = \dfrac{1}{1+T_{\mathrm{O}}^{\mathrm{v}}(s)}, \\ S_2^{\mathrm{v}}(s) = \dfrac{I_{\mathrm{H}}(s)}{\delta V_{\mathrm{H}}(s)} = \dfrac{1/Z_{\mathrm{H}}(s)}{1+T_{\mathrm{O}}^{\mathrm{v}}(s)}, \\ S_3^{\mathrm{v}}(s) = \dfrac{I_{\mathrm{H}}(s)}{\delta V_{\mathrm{S}'}(s)} = \dfrac{C_{\mathrm{v}}(s)/Z_{\mathrm{H}}(s)}{1+T_{\mathrm{O}}^{\mathrm{v}}(s)}, \\ S_4^{\mathrm{v}}(s) = \dfrac{I_{\mathrm{H}}(s)}{\delta I_{\mathrm{S}}(s)} = \dfrac{-C_{\mathrm{v}}(s)Z_{\mathrm{S}}(s)/Z_{\mathrm{H}}(s)}{1+T_{\mathrm{O}}^{\mathrm{v}}(s)}. \end{cases} \tag{5.4}$$

5.2.3 Sensitivity Analysis Metrics for I-ITM PHIL Setup

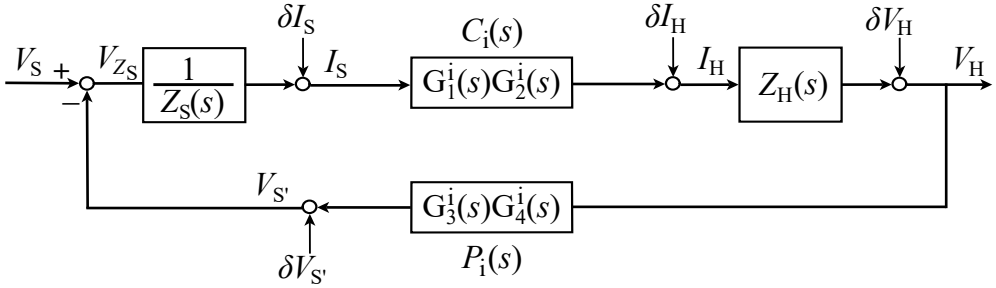

Figure 5.4: Block diagram of PHIL with I-ITM interface and disturbances arising from PI in a SISO closed-loop manner.

The equivalent block diagram of the I-ITM interface based PHIL setup with its relevant identified disturbances can be drawn by analogy with the one shown in Figure 5.3. Correspondingly, the block diagram is illustrated in Figure 5.4. The

HuT voltage V_{H} that is measured and fed back from HuT to DRTS represents the dynamics of HuT and thus being regarded as the signal of interest for the development of sensitivity analysis scheme for I-ITM interface. The sensitivity metrics for assessing the impact of the identified disturbances arising from the PI on the HuT voltage V_{H} can be derived in analogy to Eq. (5.4). On the other hand, the analysis of the impact of the disturbance associated with the signal of interest on all the interface signals within the PHIL setup is of great significance. For the disturbance δV_{H} that is associated with the signal of interest V_{H}, the sensitivity metrics for analysing its impact on all the interfacing signals are defined as,

$$\begin{cases} S_1^{\mathrm{i}}(s) &= \dfrac{V_{\mathrm{H}}(s)}{\delta V_{\mathrm{H}}(s)} = \dfrac{1}{1+T_{\mathrm{O}}^{\mathrm{i}}(s)}, \\ S_2^{\mathrm{i}}(s) &= \dfrac{V_{\mathrm{S}'}(s)}{\delta V_{\mathrm{H}}(s)} = \dfrac{P_{\mathrm{i}}(s)}{1+T_{\mathrm{O}}^{\mathrm{i}}(s)}, \\ S_3^{\mathrm{i}}(s) &= \dfrac{I_{\mathrm{H}}(s)}{\delta V_{\mathrm{H}}(s)} = \dfrac{-P_{\mathrm{i}}(s)/Z_{\mathrm{S}}(s)}{1+T_{\mathrm{O}}^{\mathrm{i}}(s)}, \\ S_4^{\mathrm{i}}(s) &= \dfrac{I_{\mathrm{H}}(s)}{\delta V_{\mathrm{H}}(s)} = \dfrac{-C_{\mathrm{i}}(s)P_{\mathrm{i}}(s)/Z_{\mathrm{S}}(s)}{1+T_{\mathrm{O}}^{\mathrm{i}}(s)}. \end{cases} \tag{5.5}$$

These sensitivity metrics define the relationship between the signal of interest and its associated disturbance or external disturbances. These play an important role in facilitating the quantitative analysis and assessment of the impact of external disturbances on PHIL simulation systems. The inherent relationship between these sensitivity metrics and stability criteria is also an indicator of the PHIL system stability and will be further elaborated in the following section. On the other hand, accuracy assessment methods are further proposed to bridge the generic sensitivity criteria in this scheme with the quantification of PHIL accuracy in the following section.

5.2.4 Sensitivity Analysis and Stability

In terms of a disturbance with given frequency ω, the magnitude of the sensitivity function $S_1(j\omega)$ defined in Eq. (5.3) is given by,

$$|S_1(j\omega)| = \left| \frac{1}{1 + T_{\mathrm{O}}^{\mathrm{v,i}}(j\omega)} \right|. \tag{5.6}$$

$|S_1(j\omega)|$ represents the reciprocal of the distance between the Nyquist curve of the open-loop transfer function $T_{\mathrm{O}}^{\mathrm{v,i}}(s)$ and the Nyquist point (-1, 0) at the given frequency ω [50]. As presented in Figure 5.5, the Vector Margin (VM) is defined by the shortest distance between the Nyquist curve and the Nyquist point. The maximum magnitude of the sensitivity function in Eq. (5.3) is achieved at this point and is calculated as $|S_1(j\omega)|_{max}$. The greater the magnitude of $|S_1(j\omega)|_{max}$ is, the closer the Nyquist curve is to the Nyquist point (-1, 0). Consequently, the PHIL system is less robust and tends to be unstable. Correspondingly, the maximum magnitude of the sensitivity function given by $|S_1(j\omega)|_{max}$ indicates the robustness of overall PHIL stability and is given by,

$$|S_1(j\omega)|_{max} = \left| \frac{1}{1 + T_{\mathrm{O}}(j\omega_0)} \right|_{max}, \tag{5.7}$$

Correspondingly, VM is expressed as,

$$\mathrm{VM} = \frac{1}{|S_1(j\omega)|_{max}}. \tag{5.8}$$

Figure 5.5 illustrates the relationship between the gain margin (GM), phase margin (PM), and the vector margin (VM). To avoid the Nyquist curve encircling the critical point, as shown in Figure 5.5, the following inequality between the stability margins can be derived as,

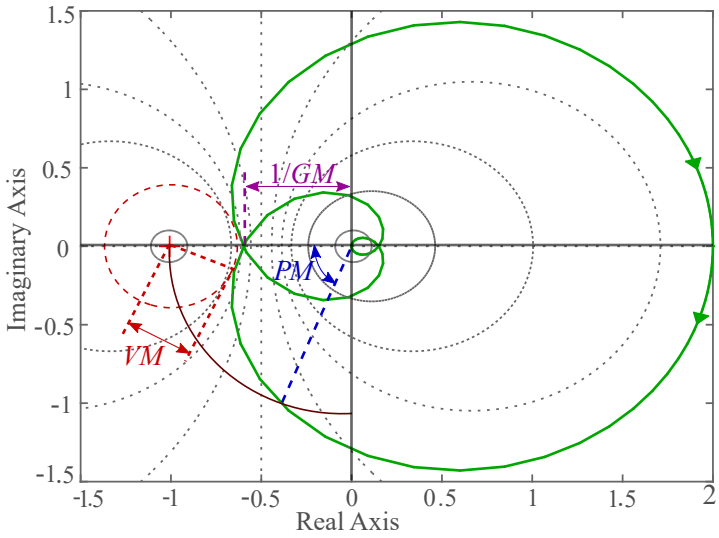

Figure 5.5: Nyquist diagram of an open-loop transfer function $T_{\mathrm{O}}(s)$ with gain margin, phase margin, and vector margin.

$$\begin{cases} \mathrm{VM} + \dfrac{1}{\mathrm{GM}} & \leq 1, \\ \mathrm{VM} & \leq sin(\mathrm{PM}). \end{cases} \tag{5.9}$$

Substituting Eq. (5.8) into Eq. (5.9), the inequalities between sensitivity function $S_1(j\omega)$ and gain margin and phase margin are given by,

$$\begin{cases} \dfrac{1}{|S_1(j\omega)|} & \leq \dfrac{\mathrm{GM}-1}{\mathrm{GM}}, \quad \forall\omega > 0, \\ \dfrac{1}{|S_1(j\omega)|} & \leq sin(\mathrm{PM}), \quad \forall\omega > 0. \end{cases} \tag{5.10}$$

Even a PHIL system with GM and PM satisfying the stability criteria defined in Eq. (2.10), the system may fail to met the criteria defined in Eq. (5.9). The inequality defined between the sensitivity function $S_1(j\omega)$ and GM and PM in Eq. (5.10) provides a critical criteria for a robust PHIL stability assessment, which will be further analytically assessed in the following section.

5.2.5 Sensitivity Analysis and Accuracy

The magnitude of sensitivity function determines the extent to which the external disturbance distorts the signal of interest and deteriorates the PHIL simulation accuracy, while the phase response characteristics indicate the corresponding phase shift of the system response with respect to the signal of interest. Based on the sensitivity metrics in Eq. (5.4) and Eq. (5.5), the impact of the various identified external disturbances on the system response can be quantified in an analytical manner. For the continuous-time domain PHIL accuracy assessment and the quantification of the extent to which the disturbances distort the PHIL accuracy, the following methods are utilised in this scheme:

- THD+N: DFT-based signal decomposition and calculation of the weighted function of the magnitude of signal with the frequency of interest (i.e., V_1) and the aggregated magnitude of signals excluding the frequency of interest, this yields,

$$\text{THD} + \text{N} = \frac{\sqrt{\sum_{i=2}^{n} V_i^2 + V_{\text{noise}}^2}}{V_1} \times 100\%, \tag{5.11}$$

  where V_i is the RMS value of the i-th harmonic voltage, V_{noise} is the RMS value of noise signal, and V_1 is the RMS value of voltage signal with frequency of interest.

- Signal to noise ratio (SNR): The SNR is calculated by,

$$\text{SNR}\,(\text{dB}) = 10log\Big(\frac{P_{\text{s}}}{P_{\text{n}}}\Big), \tag{5.12}$$

  where P_{s} is the power of signal with frequency of interest only and P_{n} is the power of signal excluding the frequency of interest.

5.3 Frequency-Domain Assessment of Sensitivity Analysis Scheme

This section presents an analytical assessment of the sensitivity analysis metrics that are developed for the V-ITM and I-ITM interfaces in frequency-domain. Following from this, the relationship between sensitivity analysis metrics and stability margins is further verified.

5.3.1 Sensitivity analysis of V-ITM Interface

The sensitivity analysis of V-ITM interface is based on the block diagram presented in Figure 5.3. According to the sensitivity metrics defined in Eq. (5.4), the impact of the identified disturbances on the signal of interest (i.e., the HuT current response I_{H}) is investigated. The parameters of the interfacing components of the V-ITM based PHIL setup are given in Table C.1 in Appendix C.

According to the parameters of the PHIL setup tabulated in Table C.1, the PHIL system open-loop transfer function as defined in Eq. (5.1) is given by,

$$T_{\mathrm{O}}^{\mathrm{v}}(s) = \frac{32.58\,\mathrm{e}^{-s\,1.03\mathrm{e}^{-4}}}{s^3\,2.64e^{-13} + s^2\,8.0e^{-7} + s + 2199}. \tag{5.13}$$

To ensure linearity and thus making the system amenable for analysis, Padé approximation as given in Eq. (2.5) is employed to represent the time delays in the transfer function. Based on this approximation, the Bode diagrams of $T_{\mathrm{O}}^{\mathrm{v}}(s)$ and $S_{2,3,4}^{\mathrm{v}}(s)$ is shown in Figure 5.6. The frequency response of the sensitivity analysis metrics reveal the impact of identified disturbances on the signal of interest in the PHIL setup from the perspectives of magnitude and phase shift.

Taking the disturbance $\delta V_{\mathrm{S}'}$ and its impact on the HuT current response I_{H} as an instance, the frequency response of $S_3^{\mathrm{v}}(s)$, as defined in Eq. (5.4), corresponds to the cyan curve in Figure 5.6. It is evident that the magnitude response presents

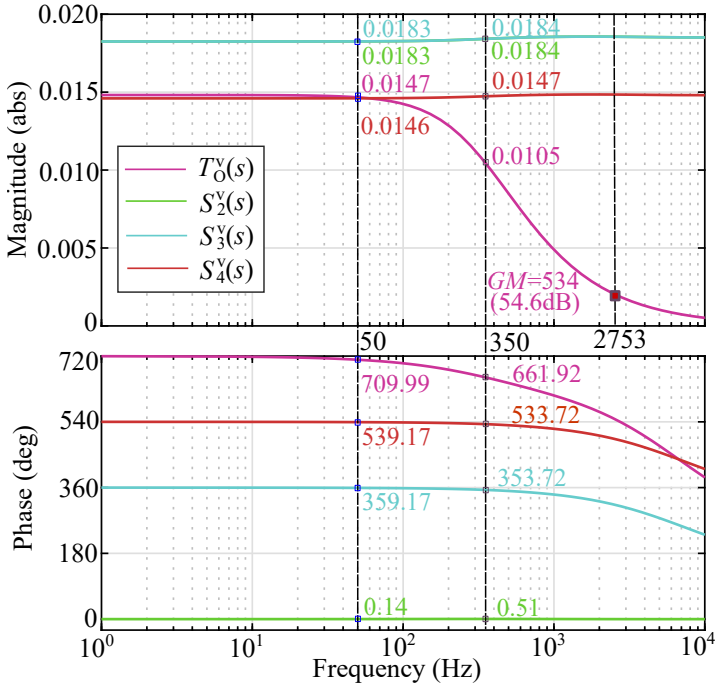

Figure 5.6: Frequency response of the open-loop transfer function $T_O^v(s)$ and sensitivity analysis metrics $S_{2,3,4}^v(s)$ in Eq. (5.4).

negligible variation and rates at 0.0184 with frequencies up to 10 kHz. In terms of the phase response, the phase shift is negligible at the frequency of interest and certain harmonics up to 350 Hz, beyond which the phase shift witnesses significant variations.

5.3.2 Sensitivity analysis of I-ITM Interface

The stability and sensitivity analysis has also been performed for the I-ITM interface, considering the block diagram in Figure 5.4. The parameters of the interfacing components of the I-ITM based PHIL setup are given in Table C.2 in Appendix C. The sensitivity analysis of I-ITM interface refers to a typical case representing a realistic scenario that is further employed for experimental validation in Chapter 5.4.

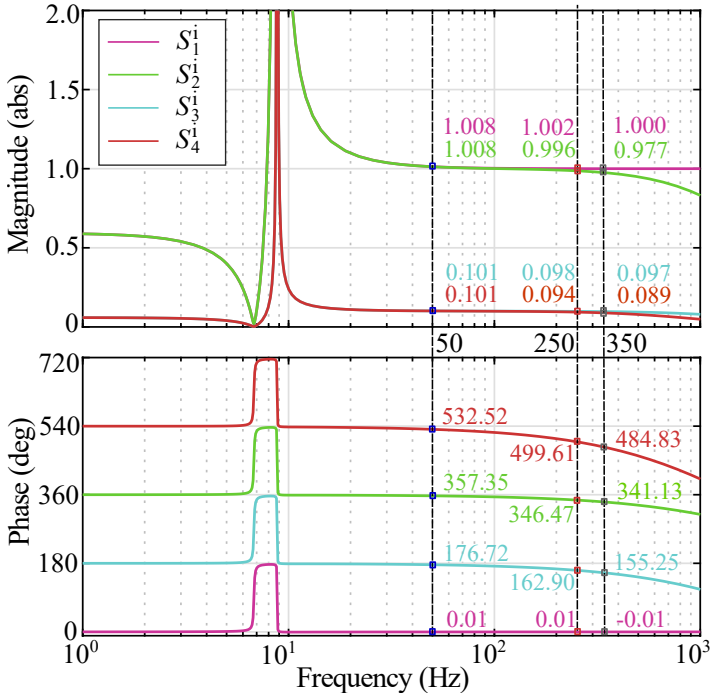

Figure 5.7: Frequency response of the I-ITM interface sensitivity transfer functions $S^{\mathrm{i}}_{1,2,3,4}(s)$ in Eq. (5.5).

In this case, the sensitivity analysis has focused on the impact of the output voltage disturbance δV_{H} of the power converter, stemming from the measurement noise and the switching of power converter operating as HuT, on the interfacing signals of the PHIL setup as highlighted in Figure 5.4. For a given disturbance with frequency ω, the frequency-dependant magnitude and phase response of the interfacing signals can be derived from the sensitivity metrics in Eq. (5.5) for further analysis. For the disturbance δV_{H}, the magnitude and phase response of the interface signals $V_{\mathrm{H}}, V_{\mathrm{S}'}, I_{\mathrm{S}}$, and I_{H} over certain frequencies of interest are highlighted in Figure 5.7.

For the analytical assessment of the sensitivity and stability criteria defined in Section 5.2.4, a case study involving different DRTS side impedance as given in Table 5.1 is presented. Figure 5.8 presents the frequency response of the open-loop transfer functions $T^{\mathrm{i}}_{\mathrm{O}2,3,4}(s)$ and their corresponding sensitivity analysis met-

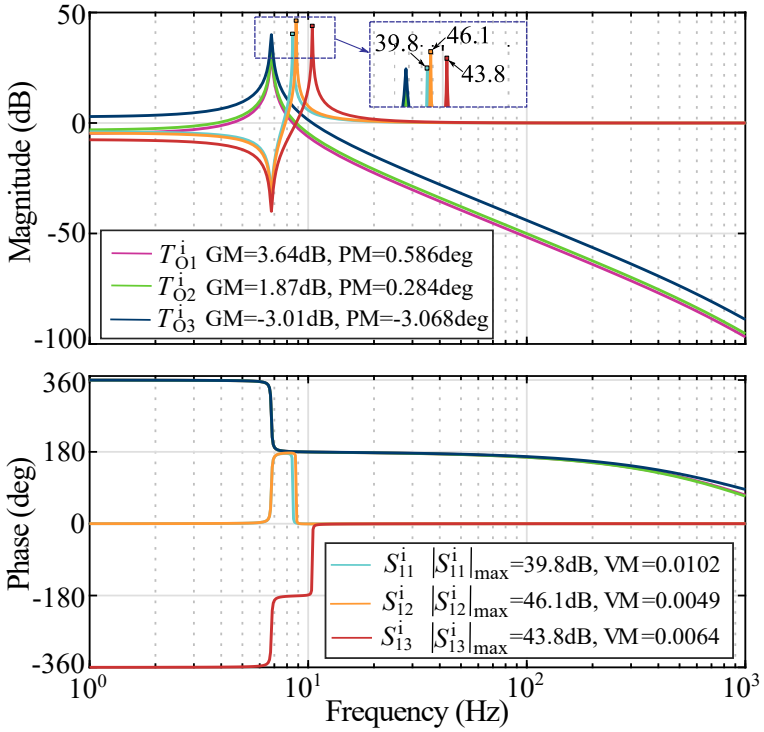

Figure 5.8: Bode diagram of open-loop and sensitivity transfer functions $T^{i}_{O1,2,3}(s)$ and $S^{i}_{11,12,13}(s)$.

Table 5.1: Stability margins of the I-ITM open-loop transfer functions $T^{i}_{O1,2,3}(s)$.

Transfer Function	Software Impedance (Ω)		**GM** (abs)	**PM** (deg)	**VM** (abs)
$T^{i}_{O1}(s)$	$Z_{11}(s)$	$12 + s4.775e^{-4}$	1.5205	0.586	0.0102
$T^{i}_{O2}(s)$	$Z_{12}(s)$	$10 + s4.775e^{-4}$	1.2402	0.284	0.0049
$T^{i}_{O3}(s)$	$Z_{13}(s)$	$5 + s4.775e^{-4}$	0.7071	-3.0680	0.0064

rics $S^{i}_{11,12,13}(s)$, of which the stability margins and the maximum magnitude are given in Table 5.1. Gain margin and phase margin of $T^{i}_{O1}(s)$ and $T^{i}_{O2}(s)$ as well as the maximum magnitude of the sensitivity analysis metrics $S^{i}_{11}(s)$ and $S^{i}_{12}(s)$ satisfy the inequality criteria defined in Eq. (5.9) and Eq. (5.10). Therefore, these

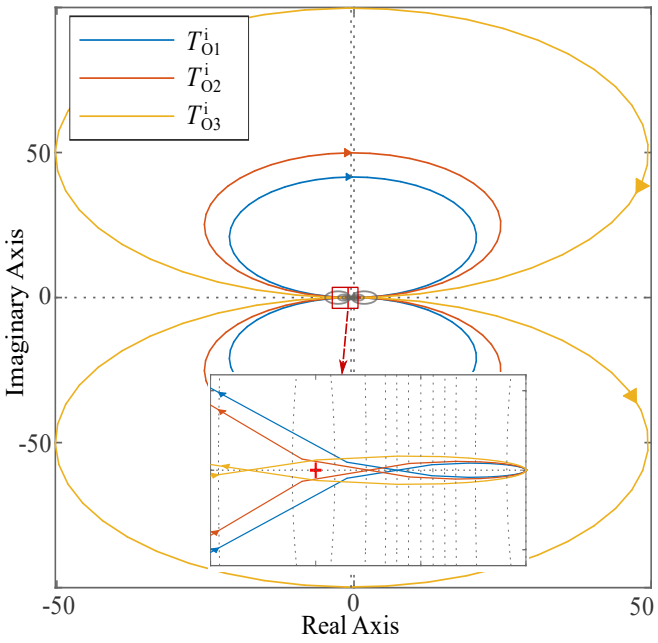

Figure 5.9: Nyquist plot of open-loop transfer functions $T^{i}_{O1,2,3}(s)$.

systems are stable, which is consistent with the stability status as indicated in the Nyquist plot in Figure 5.9. However, the gain margin and phase margin of $T^{i}_{O3}(s)$ as well as the maximum magnitude of the sensitivity function $S^{i}_{13}(s)$ do not satisfy the inequality criteria defined in Eq. (5.9) and Eq. (5.10) and therefore, the corresponding PHIL setup is unstable. This is further verified by the Nyquist plot in Figure 5.9. This case study will be further experimentally validated in Section 5.4.4 through employing a real-world PHIL experiment setup with variable DRTS side impedance as given in Table 5.1.

5.4 Experimental Verification of the Sensitivity Analysis Scheme

For a comprehensive validation of the proposed sensitivity analysis scheme and its associated stability and accuracy criteria, an I-ITM interface based PHIL experiment comprising a 90 kVA power converter as HuT and a 15 kVA power converter operating as a current-mode power amplifier is employed for experimental validation. The experimental results are compared with the analytical assessment results as presented in Chapter 5.3.2.

5.4.1 Experimental Setup

This case study involves incorporating a voltage source back-to-back converter into a PHIL simulation setup by applying the I-ITM interface. Figure 5.10 illustrates the setup for this PHIL experimental test[2]. The current signal I_{S} measured from the real-time network hosted in DRTS is transmitted to Triphase 15 kVA (TP15 kVA) current-type PA as its command signal to regulate its output current I_{H}. The output terminal of TP15 kVA converter is coupled with that of Triphase 90 kVA (TP90 kVA) power converter with the former sourcing or sinking current to the latter. The output voltage V_{H} of TP90 kVA converter is measured and transmitted to DRTS as the command voltage signal $V_{\mathrm{S}'}$ for the controllable voltage source. For the modelling process, the parameters of the interfacing components in this PHIL setup is shown in Table C.2 in Appendix C. This PHIL setup is consistent with the one used for analytical assessment in Chapter 5.3.2 and thereby allowing for a direct comparison of the experimental results with the analytical ones.

[2] The power equipment (i.e., RTDS and Triphase 90 kVA power converter) utilised in this setup are the same as the ones utilised in Chapter 3.

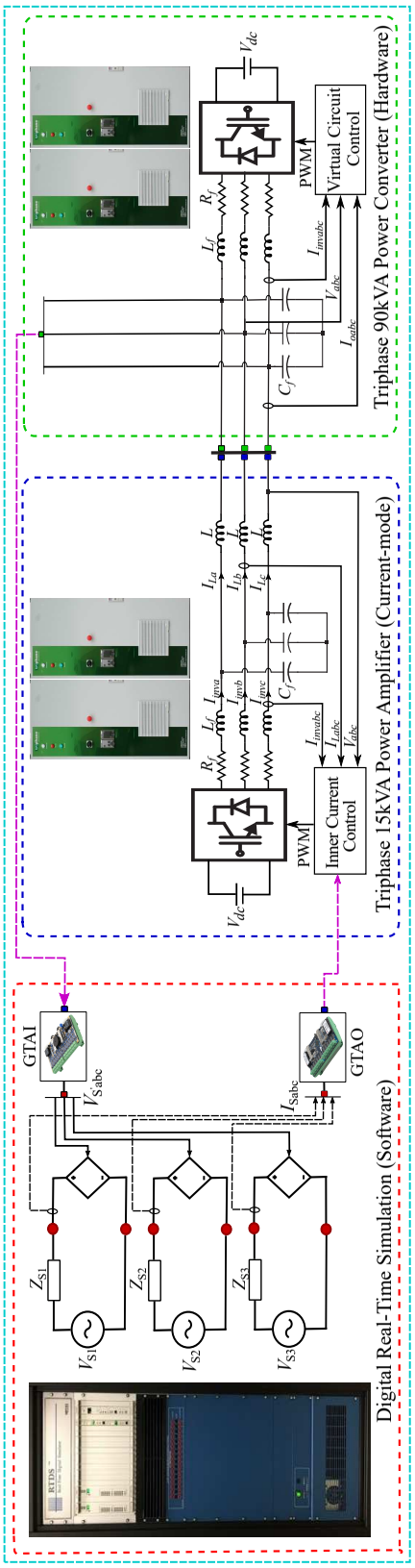

Figure 5.10: Experimental setup of the implemented PHIL simulation system with applied I-ITM interface.

An equivalent voltage source with a nominal Line-to-Line (LL) AC voltage $V_{\mathrm{S,LL}}$ of 0.4 kV, and the fundamental frequency f_0 of 50 Hz emulates a low-voltage grid. A low X/R ratio grid impedance, as listed in Table C.2 in Appendix C, emulates a strong grid. The output voltage of TP90 kVA power converter was regulated at a LL AC voltage of 260 V, 50 Hz. The DRTS side signals $V_{\mathrm{S}'}$ and I_{S} are recorded at a sampling rate of 20 kHz and the HuT side signals V_{H} and I_{H} are recorded at a sampling rate of 16 kHz by Triphase datalogger, a dedicated data acquisition unit of TP90 kVA.

5.4.2 PHIL Setup without External Disturbance Injection

Figure 5.11 presents the waveforms of interfacing signals of the PHIL setup and their single-sided amplitude spectrums. The output signal V_{H} of TP90 kVA power converter is distorted by the harmonics and high-frequency noise introduced by the pulsating modulation of the converter. Owing to the implementation of a low-pass filter with a cut-off frequency at 1500 Hz, the DRTS side voltage $V_{\mathrm{S}'}$ for the controlled voltage source presents higher SNR and lower THD+N than that of the hardware converter output voltage V_{H} and is less noisy. The SNR and THD+N of the digital current I_{S} are approximately equal to that of the voltage $V_{\mathrm{S}'}$. However, the amplitude of most frequency components of the current-mode power amplifier output current I_{H} are greater than that of the reference signal I_{S} and correspondingly I_{H} presents a lower SNR and higher THD+N than that of the current I_{S}. The inherent disturbances stemming from the aforementioned signal conversions and high-frequency pulsating modulation at each stage deteriorate the interfacing signals within the PHIL closed-loop setup.

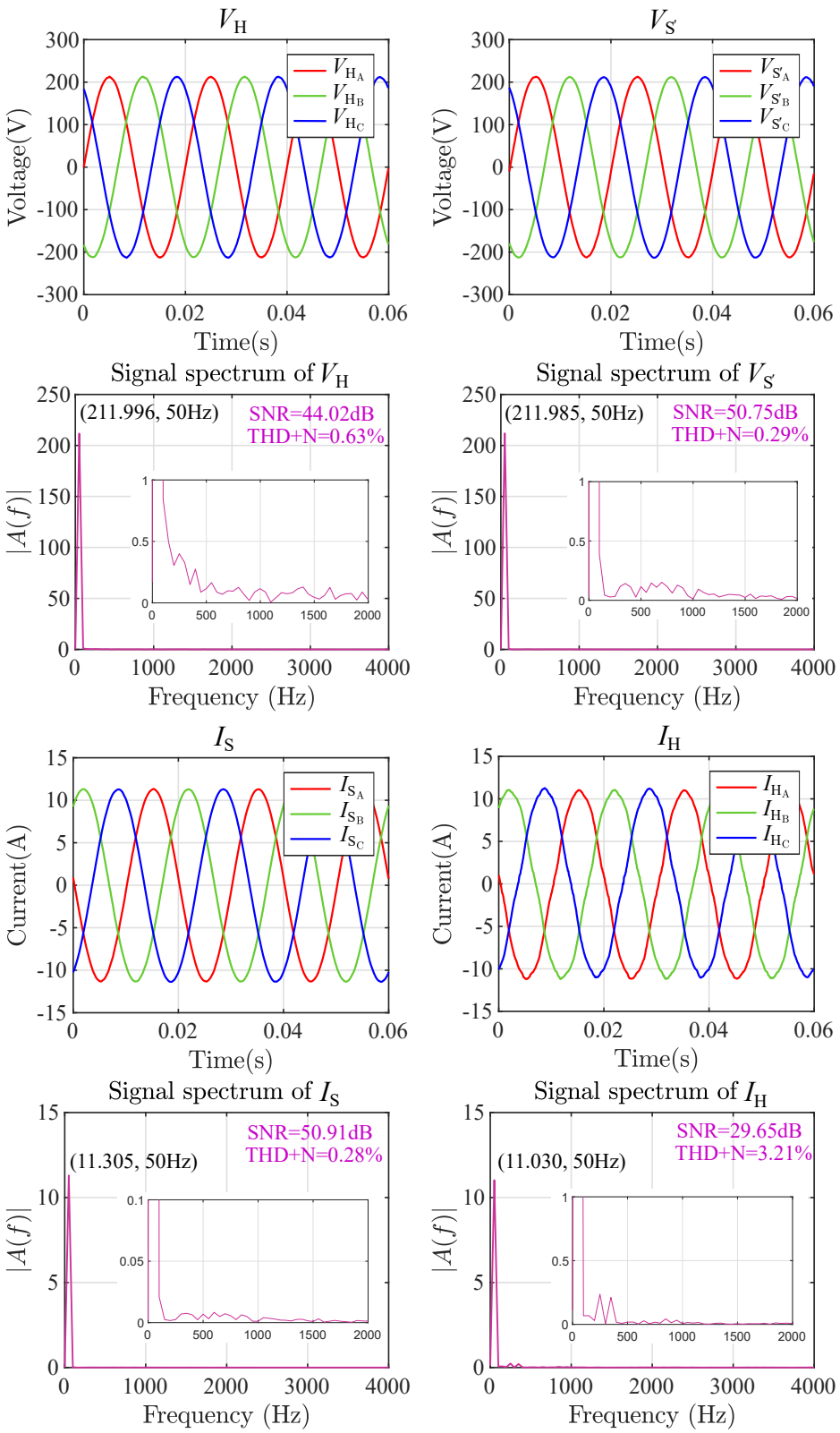

Figure 5.11: Waveforms and corresponding signal spectrums of interface signals without external harmonics injection.

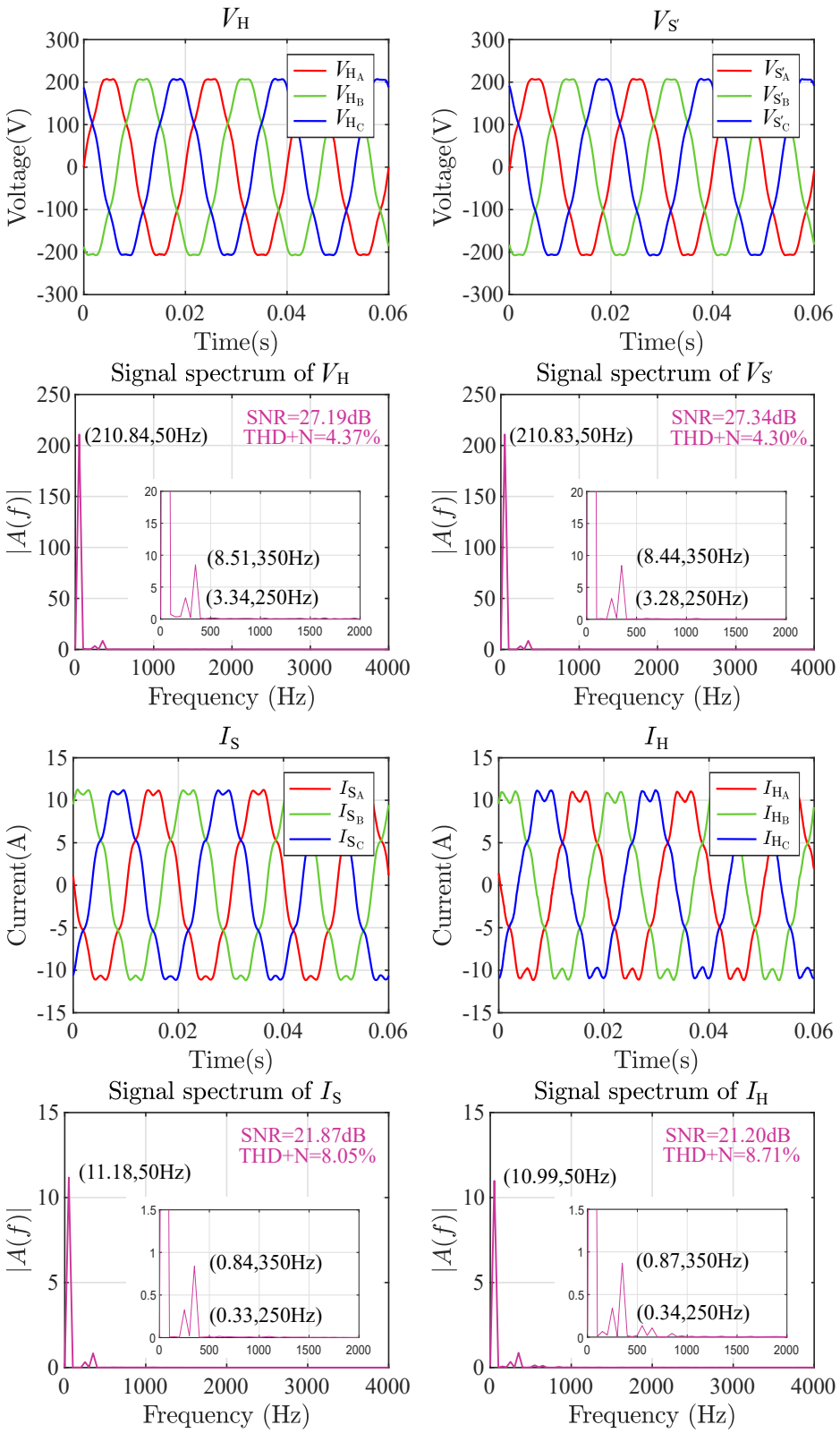

Figure 5.12: Waveforms and corresponding signal spectrums of interface signals with fifth and seventh harmonics injection.

5.4.3 PHIL Setup with External Disturbance Injection

Figure 5.12 presents the waveforms of interfacing signals of the PHIL setup and their single-sided amplitude spectrums for the PHIL testing scenarios with external disturbance injection. To demonstrate the impact of the disturbance δV_{H} on the interfacing signals, the fifth (0.015 p.u.) and seventh (0.04 p.u.) harmonics are injected in the output voltage of TP90 kVA power converter. All interface signals show lower SNR and higher THD+N than those of the scenario without external harmonics injection. Due to the magnitude attenuation and phase shift of the amplifier, significant discrepancy between the DRTS side current I_{S} and the current-mode power amplifier output current I_{H} are existent throughout the entire range of frequencies of interest as shown in Figure 5.12. Apart from the frequencies of interest, the amplitude spectrum of TP15 kVA power converter output current I_{H} presents higher portion of harmonics than its command signal as a result of the high-frequency modulation of power converter.

Sensitivity can be assessed through the signal spectrum of interface signals and the phase response of dedicated interface signals over the frequency of interest. As illustrated in the frequency spectrum in Figure 5.12, the magnitude responses of the interface signals (i.e., $V_{\mathrm{S}'}$, I_{S}, I_{H}) with respect to an externally injected harmonic signal (δV_{H}) over the frequency of interest are consistent with the magnitude responses of sensitivity metrics (i.e., $S_2^{\mathrm{i}}(s)$, $S_3^{\mathrm{i}}(s)$, $S_4^{\mathrm{i}}(s)$) in Figure 5.7. In terms of the phase response assessment of the sensitivity metrics, taking the voltage signal V_{H} and current signal I_{S} as examples, the phase shifts of the interface signal I_{S} against the externally injected voltage signal V_{H} with a fix harmonic can be directly revealed from their phase response. Figure 5.13(a) presents the phase response of I_{S} and V_{H} over the fundamental frequency. Based on these phase responses, the phase difference between these two interface signals is calculated and illustrated in Figure 5.13(b) and Figure 5.13(c). This phase difference slightly deviates from the constant value 176.72 deg (cyan line) that

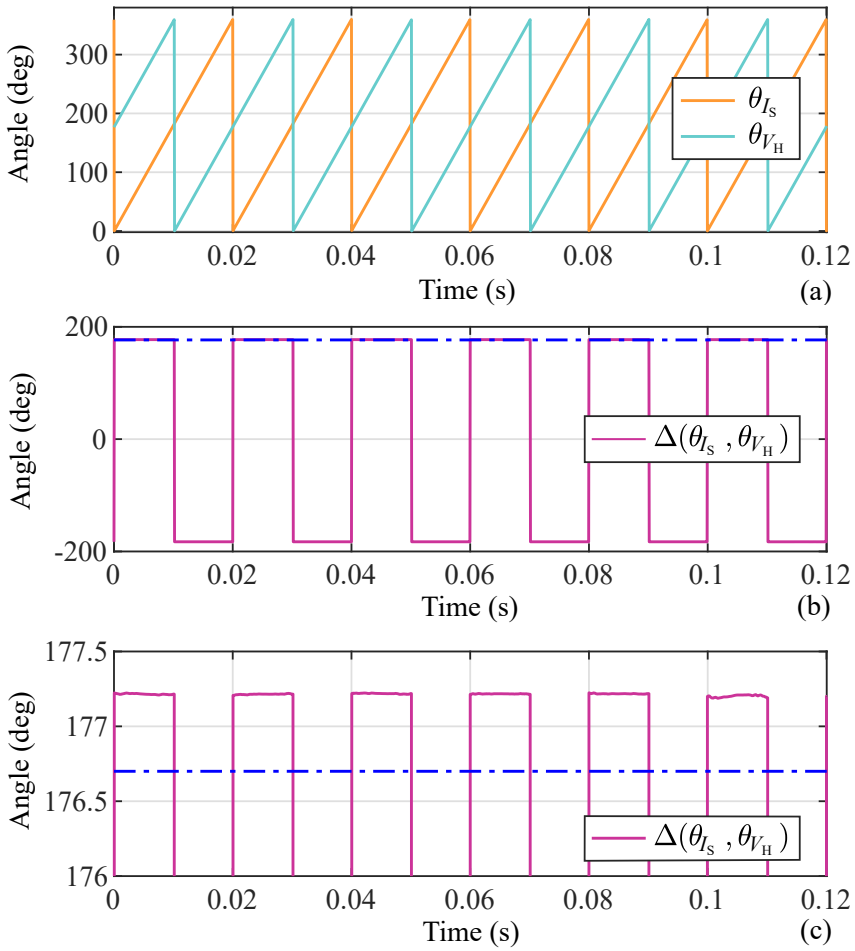

Figure 5.13: I-ITM setup: (a) phase angle of I_S and V_H with fundamental frequency (50 Hz), (b) phase difference between I_S and V_H, (c) zoomed-in version of (b).

corresponds to the phase response of the sensitivity metric ($S_3^i(s)$) at the fundamental frequency in Figure 5.7. Furthermore, the phase response of I_S and V_H over the seventh harmonic is presented in Figure 5.14(a) along with their phase difference as presented in Figure 5.14(b) and Figure 5.14(c). Once again, this phase difference deviates from the phase response (155.25 deg) of the sensitivity metric ($S_3^i(s)$) at 350 Hz in Figure 5.7. The discrepancy between the experimental phase shift and the phase shift of the analytical sensitivity metric may arise from the additional time delay stemming from the current or voltage measurement units, and the variable time delay in power amplifier.

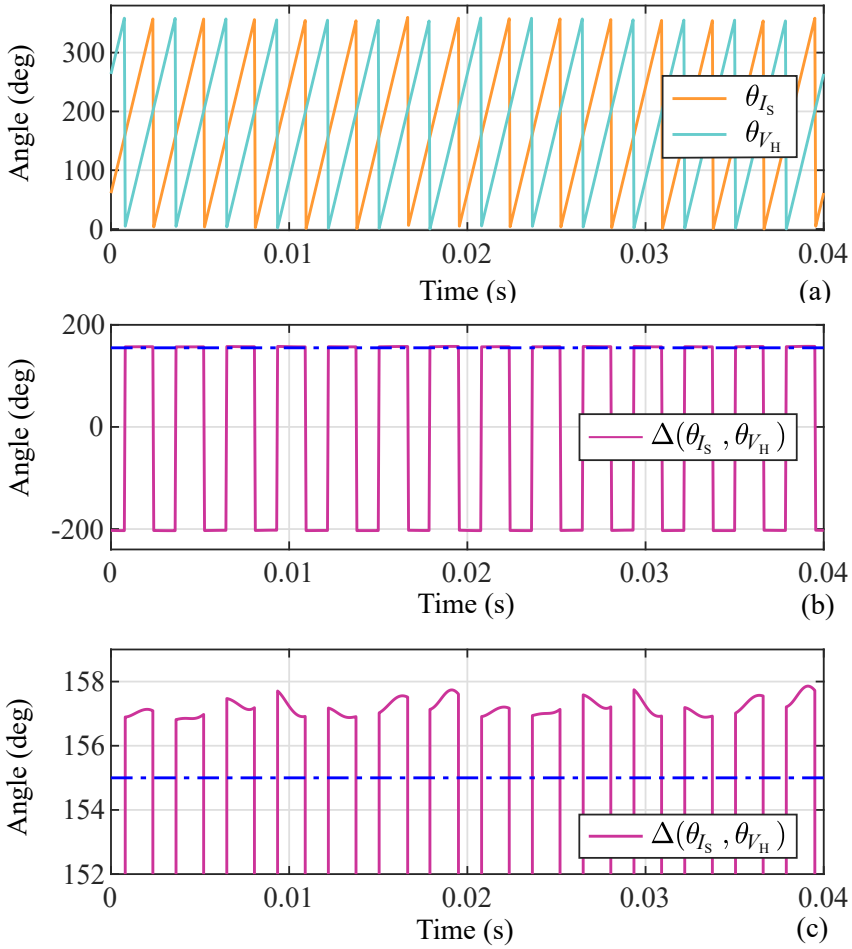

Figure 5.14: I-ITM setup: (a) phase angle of I_S and V_H with seventh harmonic (350 Hz), (b) phase difference between I_S and V_H, (c) zoomed-in version of (b).

5.4.4 PHIL Setup Stability Experimental Assessment

Based on the I-ITM PHIL setup, grid side impedance variations are emulated to verify the stability and sensitivity criteria that are defined in Chapter 5.2.4. Impedance variation from $Z_{12}(s)$ to $Z_{13}(s)$ is implemented at $t = 0.2\,\text{s}$, as given in Table 5.1, and the interface signals within the PHIL setup are shown in Figure 5.15. After the impedance change, the interface signals are divergent and present significant oscillations. The PHIL system is unstable. This is consistent with the analytical stability analysis in Chapter 5.2.4. As given in Table 5.1, the

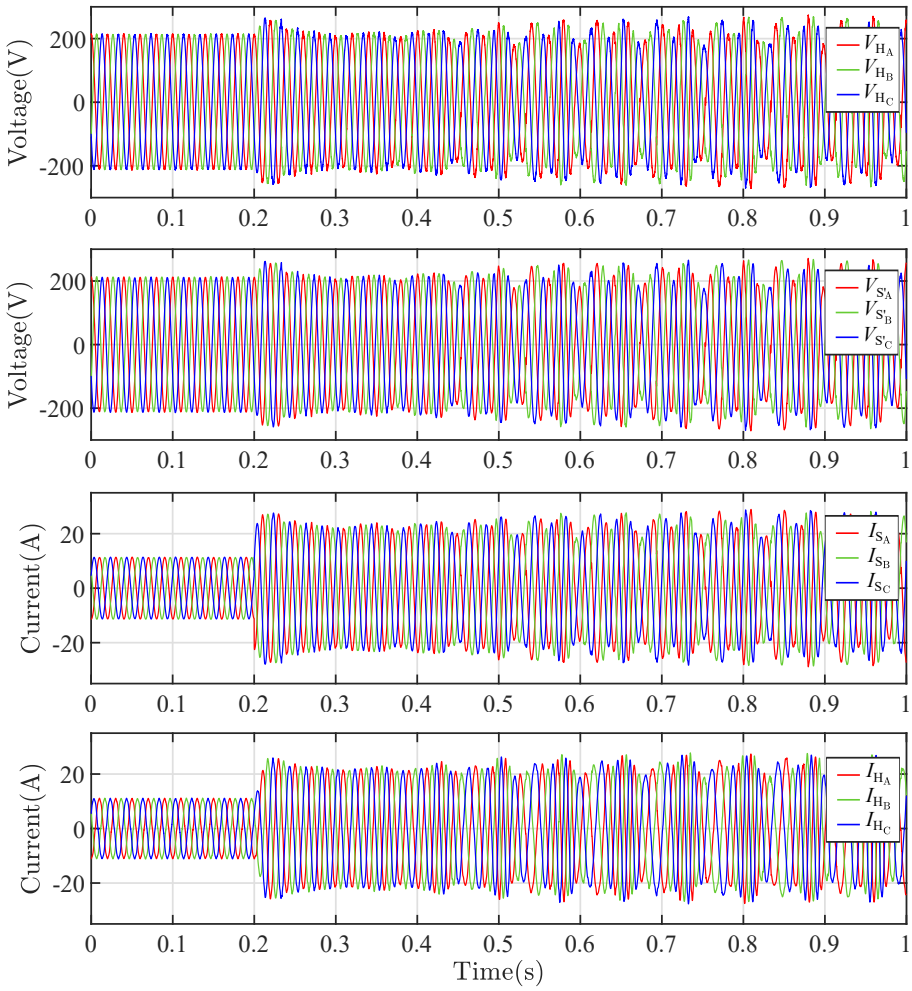

Figure 5.15: Interface signals of the I-ITM PHIL setup with varying grid impedance $Z_{12}(s)$ and $Z_{13}(s)$ as given in Table 5.1.

stability margin decreases as a result of the grid side impedance decrement. When the grid side impedance witness a variation from $Z_{12}(s)$ to $Z_{13}(s)$, the inequalities between gain margin, phase margin and vector margin defined in Eq. (5.9) and Eq. (5.10) are no longer guaranteed and the system reaches an unstable state.

5.5 Summary

This chapter presents a structured and novel scheme developed for the sensitivity analysis of PHIL simulation systems.

Firstly, depending on the interfacing methodologies, analytical modelling of PHIL systems with particular reference to potential disturbances causing sensitivity issues was presented. Based on the detailed PHIL system modelling, PHIL sensitivity transfer functions with respect to the voltage-type and current-type interfaces were introduced. The proposed sensitivity analysis metrics were of great importance for evaluating the robustness or enhanced stability properties of PHIL setups with various interfacing topologies.

On the other hand, the inherent relationships between the proposed sensitivity transfer functions and the stability criteria were explained along with theoretical and experimental validations. Moreover, based on the generic sensitivity criteria, accuracy assessment methods were employed in this proposed scheme to quantify the PHIL accuracy according to the generic sensitivity criteria. Furthermore, the experimental results of a 90 kVA power converter based PHIL setup were presented to characterise and demonstrate the applicability of the proposed sensitivity analysis scheme.

The analytical assessment and experimental validation demonstrated that the adoption of the proposed sensitivity analysis scheme enables the sensitivity behaviour and system properties, such as stability or accuracy, being determined in a reproducible and accurate manner. The proposed scheme was introduced as a guideline for the PHIL research community by providing high-value information regarding the system disturbance assessment, accuracy quantification, and system stability analysis. This fills the research gap whereby a structured analysis and evaluation has not been previously possible for assessing the impact of external disturbances on PHIL simulation performance.

Chapter 6

PHIL Interface for Black-Start Testing of Grid Forming Converters

6.1 Introduction

Power converters used for the grid-connection of key DERs, such as solar photovoltaic, wind turbines and battery systems, are typically operated in grid-following mode. The converter in this case latches to a strong grid voltage using a PLL and acts as a current source exchanging active and reactive power [84]. That said, the increasing DERs penetration is necessitating a review of this classical paradigm to exploit the power converters grid-support and restoration capabilities. The use of grid-forming converters (GFC) is gaining increasingly-high research and industrial traction due to the wide range of associated benefits [85–87]. One of the key benefits of operating converters in grid-forming mode stems from the name, i.e., due to its ability to 'form' a grid by generating its own AC voltage without the need of a PLL that synchronises it with the coupled grid. Consequently, a GFC establishes a stable and controllable voltage at its output terminal

without requiring external angular reference, which enables it to be a candidate for providing black-start services. This makes GFC an attractive option to participate in black-start applications [88–91].

Comprehensive and in-depth investigations of the dynamic limitations of candidate GFC control schemes designed for black-start service provision under a broad spectrum of operating conditions are crucial prior to their final deployment and systemic application in the power industry. For this reason, the application of PHIL simulation for GFC testing has attracted significant interest from academic researchers and industrial engineers. PHIL incorporates a real-time emulated network and hardware power converter into a closed-loop setup, which enables repeated and non-destructive testing of the candidate power converter and its associated control strategies. This can be adopted for the GFC testing to address the computation limitations of pure software simulation and de-risk the hardware experiments in a more realistic and cost-effective manner.

The voltage-type PHIL simulation setup has been extensively employed for the real-time testing of grid-following converters. The grid-following converters regulate their voltage angle to be synchronised with that of the interfacing voltage-type power amplifier (i.e., a grid simulator mimicking the real-time emulated power grid in DRTS) by employing a dedicated synchronisation unit (e.g., a PLL) [20, 27, 29, 40, 41]. However, the voltage-type interface is not capable of incorporating a GFC in the PHIL setup for black-start testing. GFC regulates output voltage by using the angular frequency reference generated by its internal dedicated unit. The direct coupling of GFC and interfacing power amplifier may lead to stability issues arising from their independent and inherent voltage regulation and the lack of voltage angle synchronisation at their coupling point. To address this issue, a physical linking impedance insertion and a digital-twin emulated impedance-based interfacing method was proposed in [92]. The applicability of this method is limited by the availability of physical impedance and

the necessity of precise power measurement before enabling the closure of a physical contactor. Furthermore, the accuracy of this setup is highly dependent on the consistency between the physically inserted linking impedance and the emulated impedance on the simulation side and is remarkably prone to the linking impedance mismatches.

To address these limitations of the conventional voltage-type interfacing method and the interfacing method developed in [92], the current-type interfacing method is proposed to incorporate a GFC into PHIL setup for black-start testing. The scaling and compensation schemes that are proposed in Chapter 4 are optimised and applied for a robust and high-fidelity PHIL simulation guaranteeing an accurate replication of the dynamics of the emulated power network at the physical GFC interfacing point. To support its adoption, a comprehensive stability analysis and assessment of this PHIL interface along with the proposed PHIL compensation techniques are presented.

The rest of this chapter is structured in the subsequent manner: Section 6.2 presents an overview of GFC control techniques to support black-start service provision. The proposed current-type PHIL setup is presented in Section 6.3, detailing the applicability of ITM interface for black-start testing of GFC, system modelling, scaling, delay compensation, and stability analysis. In Section 6.4, analytical assessment and simulation results are presented to verify the proposed interfacing method. In Section 6.5, experimental results involving interfacing a 90 kVA power converter implemented with grid-forming control are presented to demonstrate the applicability of the interfacing method. Section 6.6 summarise this chapter[1].

[1] This chapter is an extension of conference publications [23, 32], journal publication [24], and technical reports [93, 94].

6.2 GFC Control and Black-Start Techniques

Black-start application, an ancillary service that can be offered by VSC for the High-Voltage Direct Current (HVDC) network [95], has been under research spotlight in the category of Medimum Voltage (MV) distribution network. A typical testing of this ancillary service in MV network on an industrial scale is the Distributed ReStart project in the United Kingdom (UK), where a live trail of GFC for black-start application on a Mega-Watt (MW) scale has been carried out in Scottish power network [96, 97].

For VSC aided black-start application, an anchor black-start source is required to energise network segments, connect to loads, and in some cases synchronise to neighbouring networks for seamless transition to grid-connected mode. Network restoration typically involves power transformers energisation, a process that can lead to very high inrush currents, up to 7-10 times of the transformer rating current [98]. On the other hand, power converters are also known for their limited over-current capabilities. Using GFCs for large transformers energisation should thus be combined with inrush current mitigation techniques as reported in [99].

Given the GFCs voltage control flexibility, soft transformer energisation technique can be integrated into the voltage control loop. This can be achieved through the adjustment of voltage reference to a ramp between 0 and 1 pu within a suitable duration that results in inrush current mitigation [90, 99]. A sample scenario incorporating voltage ramp for black-start using a voltage source converter is shown in Figure 6.1. The various GFC control paradigms involving the droop control, power synchronising control, Virtual Synchronous Machine (VSM), and matching control are comprehensive evaluated in [88] regarding their soft black-start capabilities. Among these control methods, VSM control presents more flexibility as a result of its tunable virtual inertia. The corresponding GFC control diagram based on the VSM control method is illustrated in Figure 6.2.

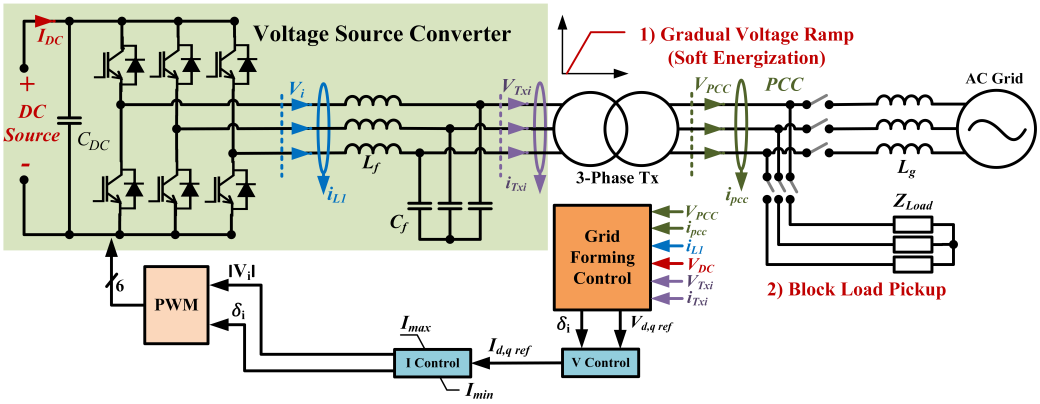

Figure 6.1: Simplified network used for preliminary grid-forming control validation and black-start steps.

This control technique emulates the swing equation of a synchronous machine as in [100],

$$J\frac{d\omega}{dt} = \frac{1}{\omega_{ref}}(P_{ref} - P) + D_p(\omega_{ref} - \omega), \tag{6.1}$$

where J is the virtual inertia, D_p is the damping factor, ω_{ref} and ω are reference and measured angular frequencies, with similar analogy for the active power P.

The VSM voltage loop is inspired by the Synchronous Generator (SG) analogy [100, 101] and yields to,

$$|V| = \frac{\omega}{K_v s}(D_q \Delta|V| + \Delta Q), \tag{6.2}$$

where $1/K_v$ is the integrator gain, D_q is the voltage damping factor, $\Delta|V|$ and ΔQ are the voltage magnitude and reactive power errors, respectively.

Finally, when soft energisation is used, the voltage reference is defined as,

$$|V_{ref}| = \begin{cases} \frac{t}{T_{ramp}}|V_{nom}|, & t < T_{ramp}, \\ |V_{nom}|, & t \geq T_{ramp}, \end{cases} \tag{6.3}$$

where T_{ramp} is the ramping duration, t is the elapsed time since ramping initialisation, and V_{nom} is the desired steady-state voltage amplitude.

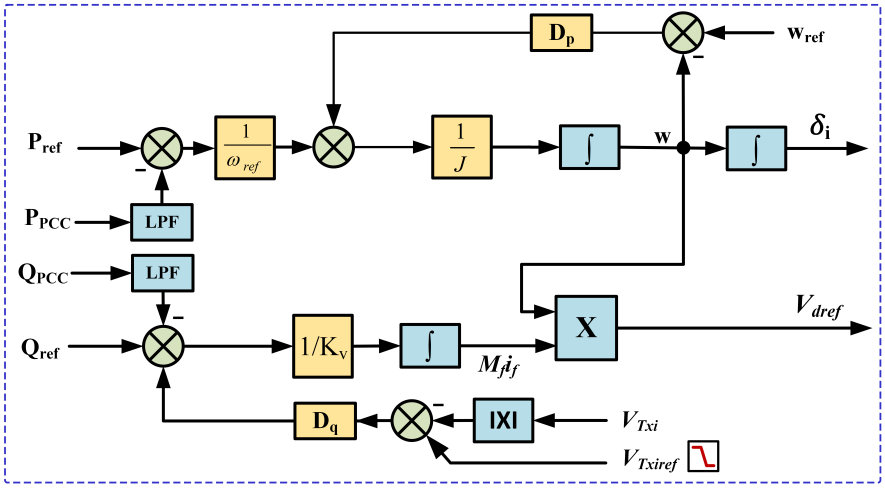

Figure 6.2: Virtual synchronous machine (VSM) control diagram.

The ramping voltage reference of GFC defined in Eq. (6.3) mitigates the transformer inrush current and limits it under the strict GFC current constraint, and thereby enabling a smoothing transformer energising process.

Loads connected at PCC can be energised with the same voltage ramp, or after a 1 pu voltage is established at the PCC. The former technique is applied in this chapter while taking into account the sensitivity of some load types to a ramped voltage startup as reported in [89]. Overall, robust system response to disturbances and transients is crucial for a successful black-start process. During the network energisation sequence, the GFC output voltage is controlled by following the amplitude reference as defined in Eq. (6.3) and the angular frequency setpoint generated by the grid-forming control loop as presented in Figure 6.2. Consequently, GFC establishes a stable and controllable voltage at its output terminal without requiring external angular reference. This attribute poses significant challenges to the V-ITM interface, which incorporates the physical power converter by regulating its voltage angle to be synchronised with that of an interfacing PA mimicking the real-time emulated power grid. The lack of voltage synchronisation at the coupling point of GFC and PA leads to instability, which will be further explained in the following sections.

6.3 PHIL Interface for Black-Start Testing of GFC

This section initially presents a comparative analysis of the applicability of V-ITM and I-ITM interfaces for incorporating a GFC with black-start capability into a PHIL closed-loop setup. This is followed by a comprehensive modelling of the PHIL setup with I-ITM interface in conjunction with an explanation of the scaling ratio, stability analysis, and time delay compensation method.

6.3.1 Applicability of ITM Interface for Black-Start Testing of GFC

The simplified power network with GFC in Figure 6.1 can be represented as a monolithic system (i.e., SoI) in the form of a lumped voltage divider topology as in Figure 6.3(a). As illustrated in Figure 6.3(b), the monolithic SoI is divided into two cascaded subsystems S_1 and S_2. System S_1 represents the emulated power network in DRTS and comprises a Thévenin equivalent voltage source V_S cascaded with an equivalent impedance Z_S. System S_2 represents the grid-forming converter that is modelled as a voltage source in series with an output impedance Z_H. As discussed in Chapter 2 and Chapter 5, a dedicated ITM based power interface bridges subsystems S_1 and S_2. Distinguished by the power amplification mode and the types of the controllable power source in DRTS side, ITM interface can be classified into voltage-type (V-ITM) and current-type (I-ITM).

As shown in Figure 6.4, a V-ITM interface is configured as a voltage-mode power amplifier that is coupled with hardware and a controllable current source on the software side. This setup has been extensively employed for grid-following converter testing, where the converter under test regulates its current to be synchronised with the power amplifier output voltage [20, 29]. However, owing to the

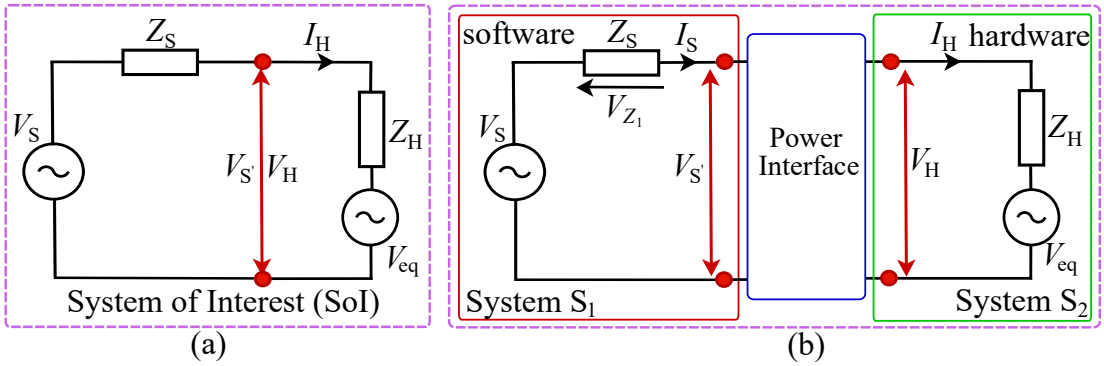

Figure 6.3: Principle topology of (a) SoI with equivalent emulated DRTS network and GFC modelling and (b) the corresponding PHIL simulation system.

inherent voltage amplitude and angular frequency regulation of GFC, this setup is not suitable for interfacing GFC into a PHIL setup for black-start testing. The direct coupling of GFC and voltage-mode power amplifier leads to instability stemming from the lack of voltage synchronisation at their coupling point.

On the contrary, an I-ITM interface is configured as a current-mode power amplifier sinking or sourcing current to the coupled hardware and a controllable voltage source on the software side. Figure 6.5 illustrates the equivalent circuit diagram of the PHIL setup comprising a real-time emulated power network, current-mode power amplifier, and power converter implemented with grid-forming control. The inductive filter of the current-mode power converter tackles the voltage synchronisation issue of the V-ITM interface and the dynamics in the simulated power network can be replicated to the GFC under test through the current-mode power amplifier. Despite the feasibility of this interface to incorporate GFC in a PHIL setup, its practical implementation is constrained by the limited capability of the power amplifier in terms of its power rating, and by the stability and accuracy issues arising from the loop time delay. From an application point of view, comprehensive system modelling, optimised design (e.g., proper scaling), stability assessment, and time delay compensation are crucial for accurate replication of the behaviours of physical GFC in the emulated grid.

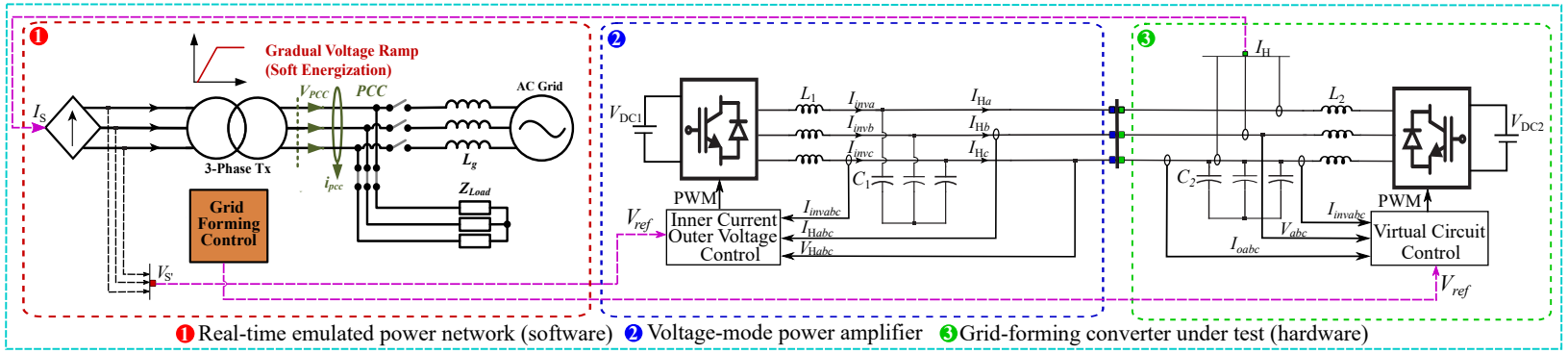

Figure 6.4: A representation of the equivalent circuit diagram of a voltage-type PHIL system with physical grid-forming converter.

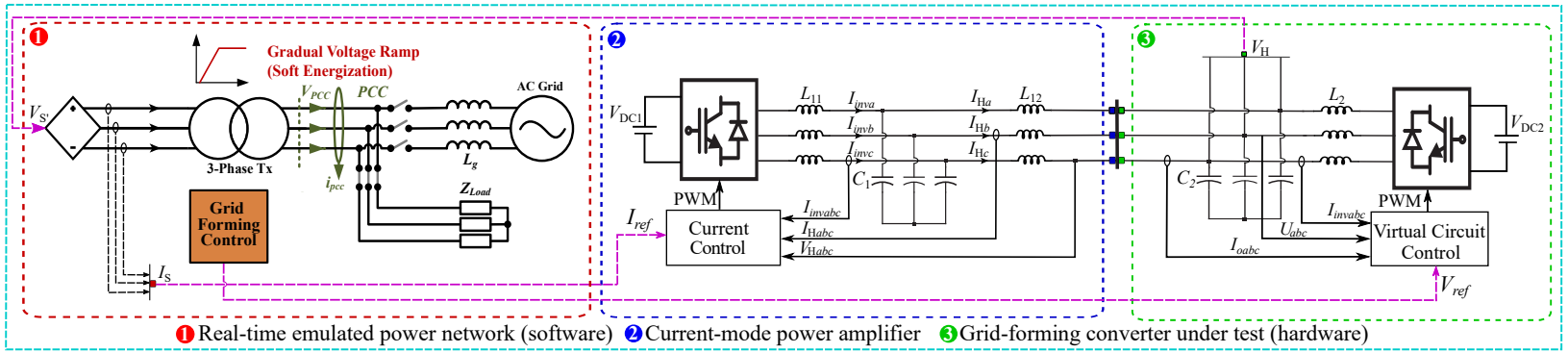

Figure 6.5: A representation of the equivalent circuit diagram of a current-type PHIL system with physical grid-forming converter.

6.3.2 Interface Design and Modelling

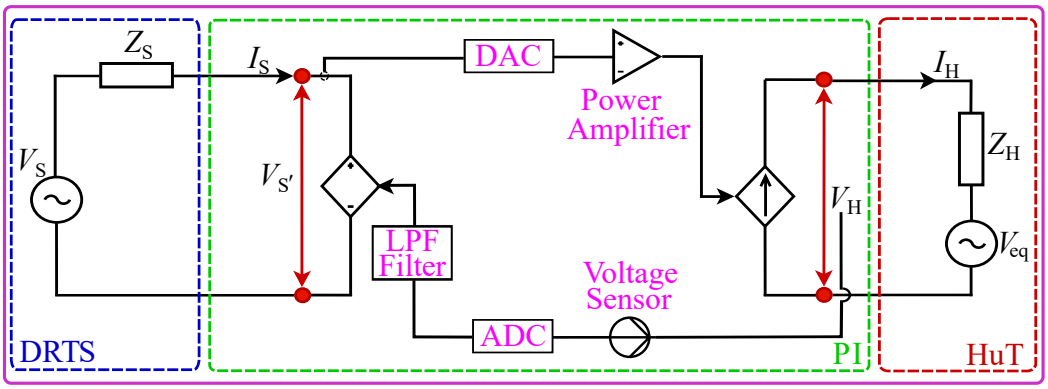

Figure 6.6: Equivalent model of the PHIL system with I-ITM interface and GFC.

The equivalent model of the PHIL setup in Figure 6.5 is presented in Figure 6.6, of which the equivalent block diagram is presented in Figure 6.7. As shown in Figure 6.7, the interface components, equivalent impedance, and interface signals are represented in the equivalent block diagram as a SISO closed-loop system. The scaling ratio design and the interfacing component modelling are presented as follows:

(1) Voltage and Current Scaling Ratio

The power capacity and voltage level of the network to be energised in the black-start sequence is higher than that of the candidate GFC power converter in the laboratory, and the current in energised network is much higher than the current constraint of the current-mode power amplifier. Voltage scaling ratio r_v is introduced to scale up the output voltage (V_{H}) of the physical GFC to a higher voltage ($V_{\mathrm{S}'}$) in the emulated power network that is hosted in DRTS. Current ratio r_i is utilised to scale the digital current (I_{S}) in the power network down to a lower command for regulating the output current (I_{H}) of the power amplifier. The voltage scaling ratio and current scaling ratio are given by,

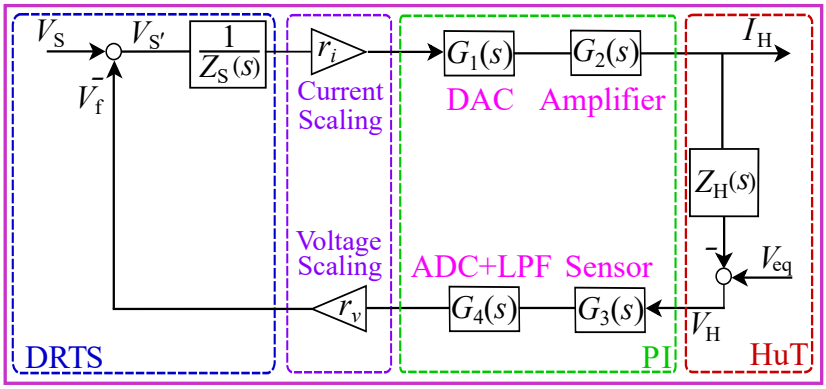

Figure 6.7: Equivalent block diagram of the I-ITM based PHIL system in Figure 6.6.

$$r_v = \frac{V_{S'\text{nom}}}{V_{\text{Hnom}}},\ r_i = \frac{I_{\text{Hnom}}}{I_{\text{Snom}}},\ \frac{S_S}{S_H} = \frac{r_v}{r_i}, \tag{6.4}$$

where V_{Hnom} and $V_{S'\text{nom}}$ are the nominal voltage of the physical GFC and emulated GFC on DRTS side, respectively. I_{Hnom} and I_{Snom} are the nominal current of the power amplifier and the rated current of the emulated power network on DRTS side, respectively. S_H and S_S are the power rating of the physical GFC and emulated GFC on DRTS side, respectively.

(2) Current-Mode Power Amplifier

The cell 2 of Figure 6.5 represents the circuit diagram of the switched-mode power converter with LCL output filter. Figure 6.8 presents the grid side current feedback control diagram of this three-phase current-mode VSC. The system open-loop transfer function is give by,

$$T_{\text{OCA}}(s) = \frac{i_e}{i_a} = \frac{(k_p s + k_i) K_{\text{PWM}} e^{-sT_{\text{d-PA}}}}{L_{11}L_{12}C_1 s^4 + (L_{11} + L_{12})s^2}, \tag{6.5}$$

where k_p and k_i are the proportional gain and integral gain of the current controller, respectively. K_{PWM} is the gain (i.e., half of the DC-link voltage) of PWM converter and $T_{\text{d-PA}}$ is the PWM control delay that is a sum of one time step T_s

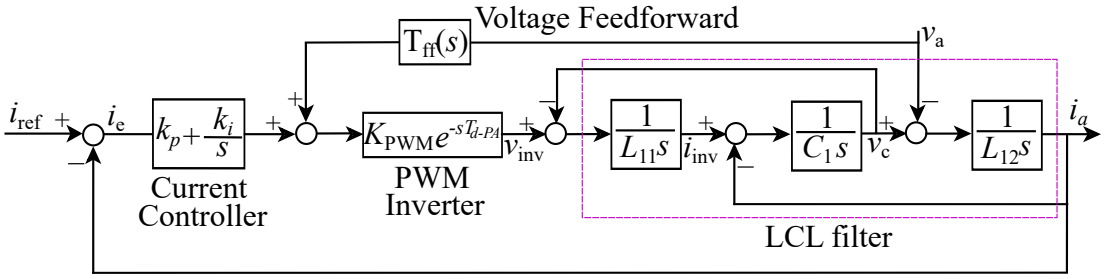

Figure 6.8: Block diagram of the current feedback control of the current-mode power amplifier.

for computation and half time step for PWM generation.

Applying the Taylor series expansion, the PWM control delay is approximated as,

$$e^{-sT_{\mathrm{d-PA}}} = e^{-s1.5T_s} \approx \frac{1}{1+1.5T_s s}. \tag{6.6}$$

Grid-side voltage feed-forward is implemented to mitigate the impact of GFC output voltage on the grid-side current regulation. The voltage feed-forward term $T_{ff}(s)$ is given by,

$$T_{ff}(s) = \frac{1}{K_{\mathrm{PWM}}e^{-sT_{\mathrm{d-PA}}}}(L_{11}C_1 s^2 + 1). \tag{6.7}$$

Substituting Eq. (6.6) into Eq. (6.5) and taking the voltage feedforward term into account, the closed-loop transfer function of the current-mode power amplifier is obtained as,

$$G_2(s) = \frac{(k_p s + k_i)K_{\mathrm{PWM}}}{1.5T_s L_{11}L_{12}C_1 s^5 + 1.5T_s(L_{11}+L_{12})s^3 + (k_p s + k_i)K_{\mathrm{PWM}}}. \tag{6.8}$$

Note that, the rest of interfacing components in Figure 6.7 are modelled in analogy to the generic modelling as presented in Eq. (2.2) in Chapter 2.2.

6.3.3 PHIL System Stability Assessment

Based on the interface modelling, the open-loop transfer function of the SISO closed-loop PHIL system in Figure 6.7 is defined as,

$$T_{\mathrm{O}}(s) = r_v r_i G_1(s) G_2(s) G_3(s) G_4(s) \frac{Z_{\mathrm{H}}(s)}{Z_{\mathrm{S}}(s)}. \tag{6.9}$$

The closed-loop stability is determined by the time delay, the non-ideal power amplifier and signal processing unit in the power interface, and the variable impedance at different black-start stages on the simulation side. Nyquist stability criteria can be applied to determine the closed-loop system stability by assessing the eigenvalues of the system characteristic equation $(1 + T_{\mathrm{O}}(s) = 0)$. Correspondingly, the system stability margins (e.g., GM and PM) defined in Eq. (2.9) can be adopted to quantitatively assess this PHIL closed-loop stability.

6.3.4 Time Delay Compensation for Accuracy Improvement

As demonstrated in Chapter 2.4, the time delay stemming from the signal conversion units (e.g., GTAO and GTAI cards) and the digital control of the power amplifier inevitably introduces phase offsets between the power signals transmitted within the closed-loop setup and deteriorates the power transfer transparency between the software and hardware side. Since the VSM control is dependent on accurate voltage signal synchronisation and power measurement that are susceptible to the phase mismatch between the hardware GFC and the equivalent virtual GFC on DRTS side, time delay compensation is crucial for a high-fidelity replication of the emulated grid behaviours to hardware GFC.

The SDFT based time delay compensation scheme as presented in Chapter 4.3.2 is employed to compensate for the time delay in the PHIL setup by

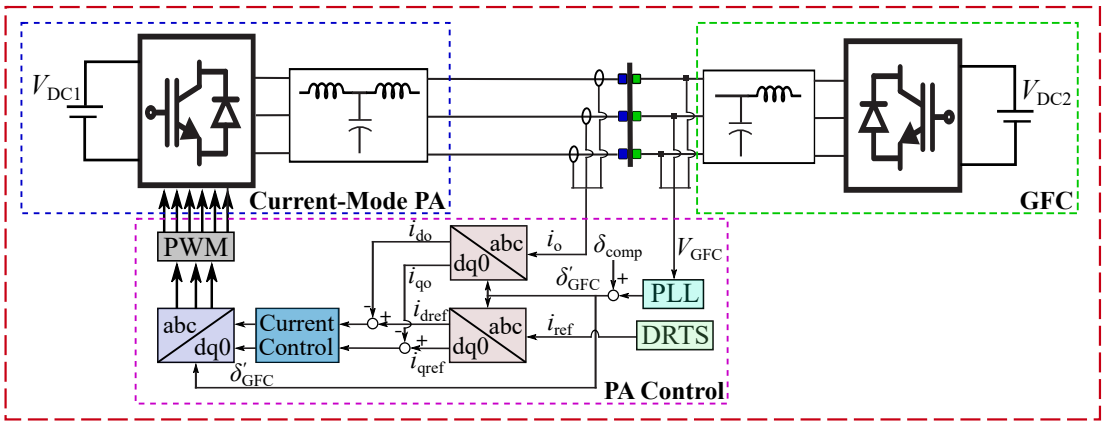

Figure 6.9: Block diagram of phase-lag compensation.

adding an additional phase shift to the command signal of the current-mode power amplifier and the measured hardware voltage signal at the fundamental frequency. On the other hand, the time delay compensation of the current-mode power amplifier can be achieved by adding an additional phase shift (δ_{comp}) to the hardware GFC output voltage phase angle (δ_{GFC}) that is extracted by a PLL from GFC output voltage. This is given by,

$$\delta'_{\text{GFC}} = \delta_{\text{GFC}} + \delta_{\text{comp}}. \tag{6.10}$$

The phase shifted GFC voltage angle (δ'_{GFC}) is further utilised to convert the current control loop output component (in dq frame) to the modulating signal of the current-mode power converter, thereby compensating for the time delay arising from the current-mode power amplifier and aligning the output current of current-mode power amplifier with its current reference received from DRTS.

By doing so, accurate voltage or current signal synchronisation and transparent power transfer between the real-time emulated power network and the hardware GFC can be achieved.

6.4 Analytical Assessment and Simulation

This section presents a comparison between the voltage-type and current-type PHIL interfaces regarding their feasibility and capability of incorporating GFC into a PHIL setup. Finally, analytical assessment of the current-type PHIL stability is presented.

Table 6.1: PHIL setup parameters in Figure 6.5.

Description	**Symbol**	**Value**
PHIL setup		
Voltage scaling ratio	r_v	27.5
Current scaling ratio	r_i	0.0133
Cut-off frequency of $G_4(s)$ in Eq. (6.9)	f_{c4}	500 Hz
Transformer power rating (3 phase)	S_{Tx}	53MVA
Transformer turns ratio (kV_{LL_P}/kV_{LL_S})	TR	11/33
Equivalent load in emulated power network	Z_{load}	54 Ω
Real-time digital simulator time step	τ_s	50 µs
Current-type power amplifier (TP15 kVA)		
DC voltage	V_{DC1}	650 V
Switching frequency	f_{sw1}	6.4 kHz
Sampling frequency	f_{s1}	6.4 kHz
Inverter side filter inductance	L_{11}	2.3 mH
Grid side filter inductance	L_{12}	0.93 mH
Filter capacitance	C_1	8.8 µF
PI controller proportional gain	k_p	11
PI controller integral gain	k_i	12.5
Hardware converter under test (TP90 kVA)		
DC voltage	V_{DC2}	700 V
Switching frequency	f_{sw2}	16 kHz
Sampling frequency	f_{s2}	16 kHz
Inverter side filter inductance	L_2	0.5 mH
Filter capacitance	C_2	47 µF
Emulated virtual resistance [102]	R_e	6.8417 Ω
Emulated virtual inductance [102]	L_e	0.05 mH

6.4.1 Voltage-Type PHIL for Interfacing GFC

For the black-start application, a grid-forming converter has its internal control loop to regulate voltage and frequency to energise the power network. Since the direct coupling of GFC and voltage-mode power amplifier leads to instability and potential damage to the physical apparatus, Matlab/Simulink simulation is employed to assess this setup. The emulated voltage-mode power amplifier and hardware GFC are based on the parameters of TP90 kVA in Table 6.1, which includes the parameters of the remainder PHIL setup in Figure 6.5.

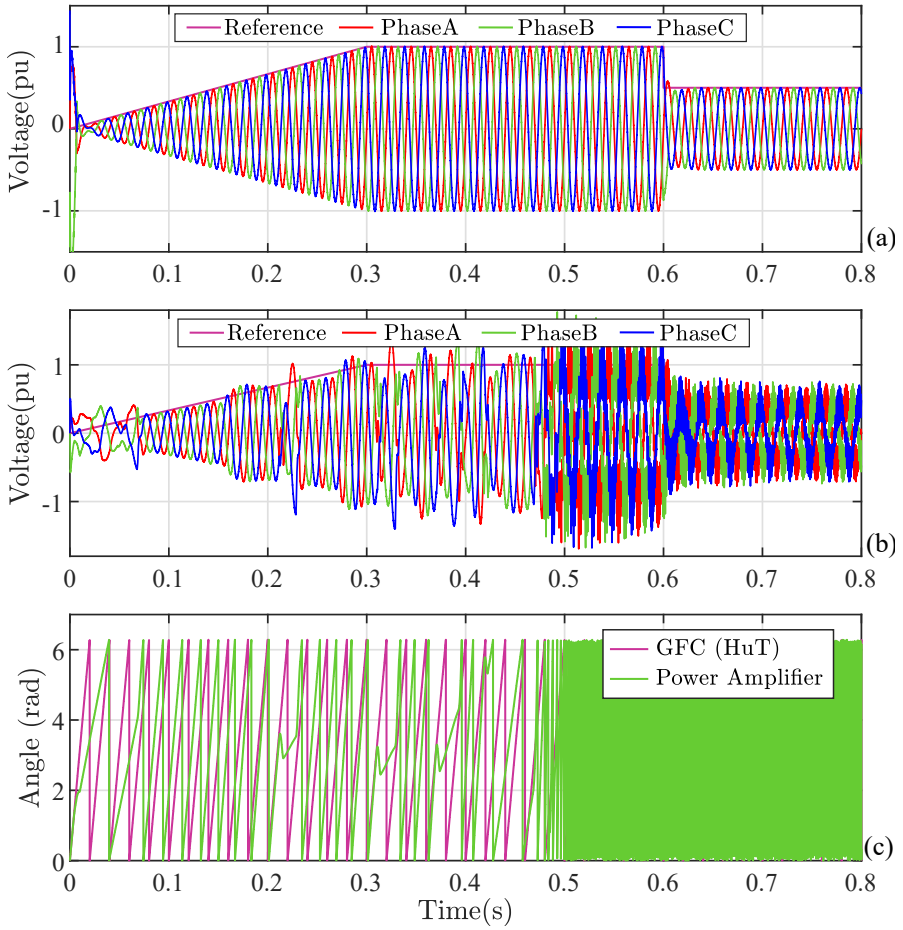

Figure 6.10: (a) GFC voltage of monolithic SoI, (b) GFC voltage of voltage-type PHIL, and (c) voltage angle of voltage-type PHIL.

In the monolithic SoI, a GFC is directly coupled with the power network without an interfacing power amplifier. Figure 6.10(a) presents the GFC output voltage. A voltage reference with a ramp-up between 0-0.3s and a step-down at t=0.6s is emulated and the GFC output voltage presents good tracking performance.

In terms of the voltage-type PHIL setup as presented in Figure 6.4, GFC regulates its output voltage by following its inherent angle while the power amplifier regulates its output voltage by following the reference signal from DRTS. These attributes lead to angle mismatch at the coupling point between GFC and power amplifier. As shown in Figure 6.10(b), the GFC output voltage (i.e., the voltage at the coupling point between GFC and power amplifier) presents significant oscillations. It is evident in Figure 6.10(c) that the voltage angle of GFC presents significant discrepancies from that of the power amplifier.

6.4.2 Stability Assessment of Current-Type PHIL Interface

According to the virtual circuit control theory as presented in [102], the output impedance of TP90 kVA is given by,

$$Z_{\mathrm{H}}(s) = \frac{s5.5\mathrm{e}^{-4} + 6.842}{s^2 5.5\mathrm{e}^{-4} + s3.216\mathrm{e}^{-4} + 1}. \tag{6.11}$$

The system open-loop transfer function in Eq. (6.9) can be calculated by utilising the system parameters tabulated in Table 6.1 and its corresponding frequency response is shown in Figure 6.11. The open-loop transfer function of the current-type PHIL setup with parameters in Table 6.1 has positive GM and PM and the closed-loop setup is stable. The impact of the scaling ratios that are employed to facilitate the hardware GFC power rating and to limit the power amplifier current reference on the PHIL closed-loop stability is assessed. A higher power

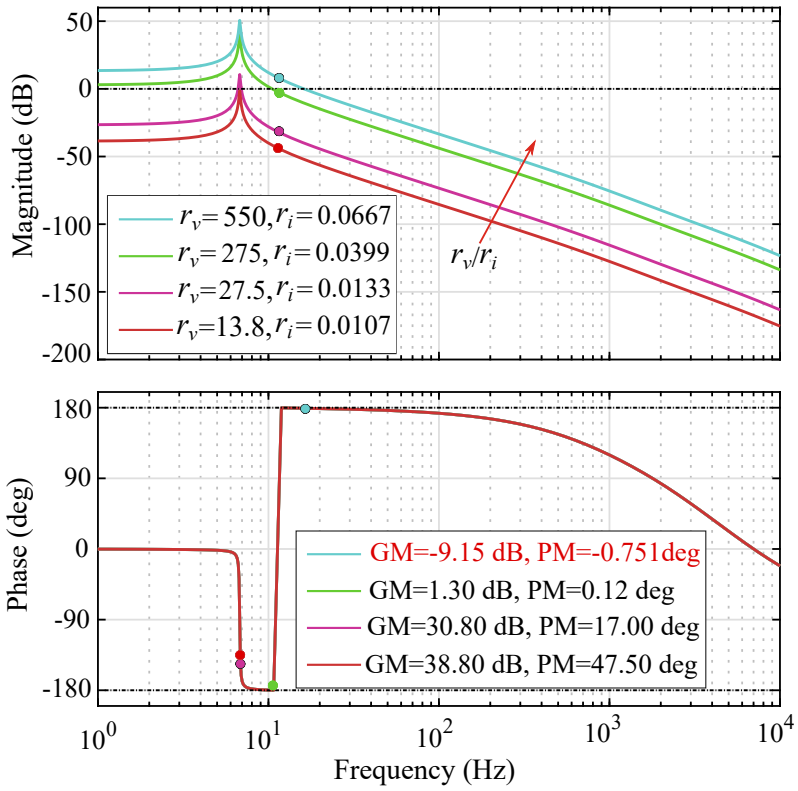

Figure 6.11: Bode diagram of the open-loop transfer function of current-type PHIL setup.

rating of the emulated GFC on the real-time simulation side can be achieved by implementing a high voltage scaling ratio. However, as illustrated in Figure 6.11, such a PHIL system can be unstable as the increment of the voltage scaling ratio degrades the system gain margin. The cyan curve represents the PHIL system with the highest voltage scaling ratio and power rating among the given systems, this PHIL system is unstable and presents negative GM and PM. The gain margin of the PHIL system is a factor by which the scaling ratio can be raised before breaching the system stability. A stability assessment of the PHIL system with pre-designed scaling ratios is crucial prior to the final-stage system implementation.

6.5 Experimental Validation

This section is dedicated to the experimental validation of the current-type PHIL interface regarding its capability to incorporate GFCs with black-start capabilities into a PHIL setup.

Figure 6.12 illustrates the experimental setup, the cells of which are corresponding to those presented in Figure 6.13. The simplified power network model is emulated in RTDS and Triphase 90 kVA (TP90 kVA) power converter operates in grid-forming mode. These are coupled by a Triphase 15 kVA (TP15 kVA) power converter acting as a current-type power amplifier that sinks or sources current to the TP90 kVA converter, thus enabling the PHIL closed-loop configuration and mimicking the relative power behaviors in the emulated power network. The parameters of the emulated power network, power amplifier, and power converter are given in Table 6.1. The scaling ratio r_v and r_i as tabulated in Table 6.1 are employed to represent the power converter that is emulated in RTDS with higher power rating and voltage levels than that of the actual GFC (TP90 kVA) and to scale down the RTDS reference current signal within the current constraint of TP15 kVA power converter, respectively. By doing so, the power rating of the emulated GFC on RTDS side is 2062 (r_v/r_i) times that of TP90 kVA.

To validate the effectiveness of the current-type PHIL interface in realising a stable and accurate testing of the hardware GFC integration throughout the black-start process, voltage-mode VSM control with a 5-second ramping time of the hardware GFC is utilised to realise a soft energisation of the power transformer together with the load connected at the PCC point in the emulated power network. The voltage and current at the interfacing point in RTDS, the output voltage of TP90 kVA, and the command and output current of TP15 kVA are recorded by RTDS and Triphase datalogger, respectively, and are replotted by Matlab.

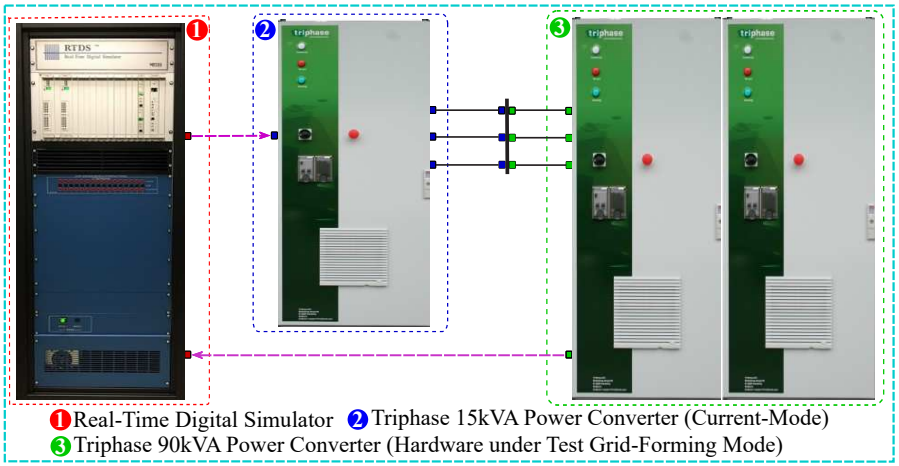

Figure 6.12: A representation of the experimental PHIL setup with physical grid-forming converter.

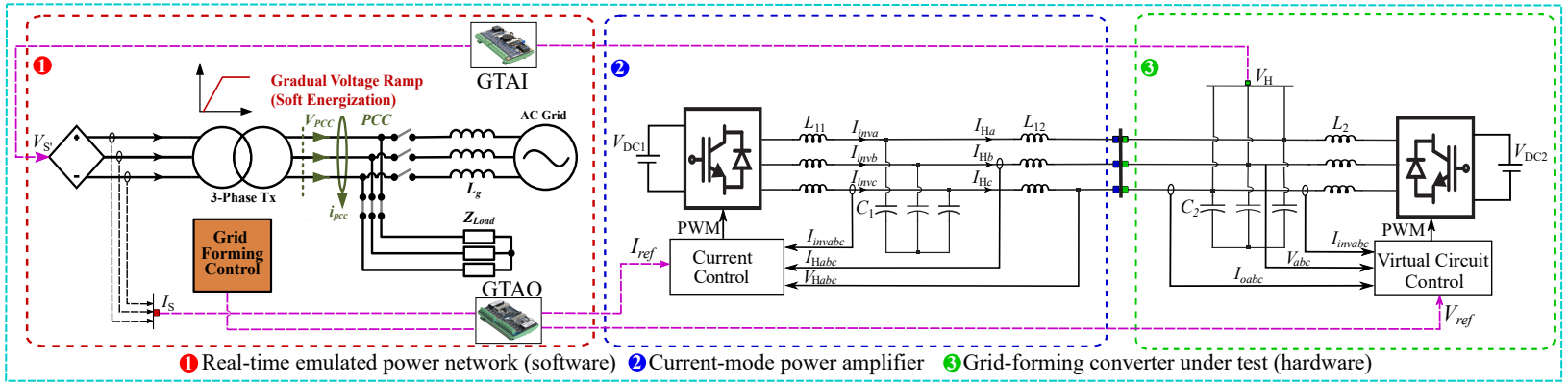

Figure 6.13: Equivalent circuit diagram and interface as implemented in Figure 6.12

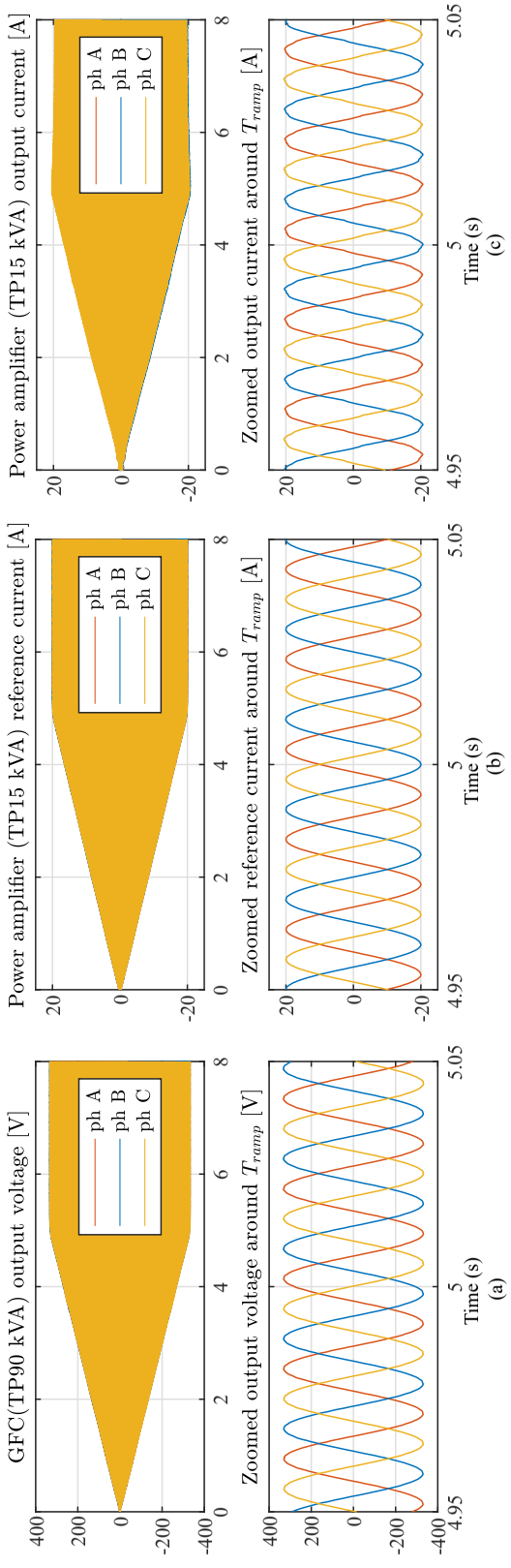

Figure 6.14: Experimental results of the voltage and current of the power amplifier and GFC power converter within the PHIL setup.

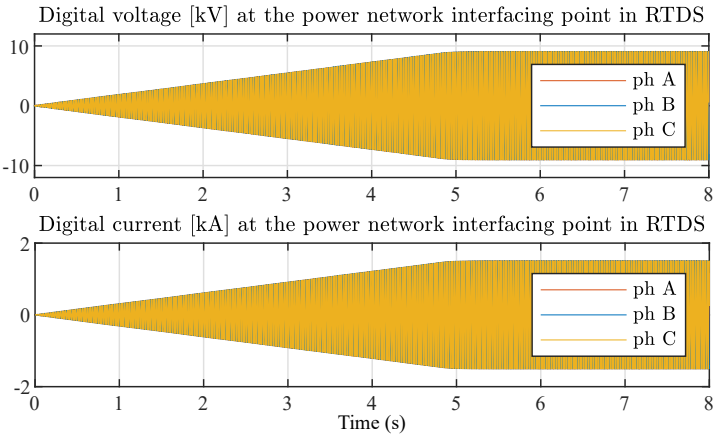

Figure 6.15: Experimental results of the voltage and current at the interfacing point within the real-time emulated power network.

The voltage at the hardware GFC power converter output terminal is presented in Figure 6.14(a) with a zoomed section around the end of ramping time. This illustrates a successful hardware GFC output voltage tracking from 0 to the rated value without any measurable delay during the voltage ramp period. Correspondingly, the voltage at the interfacing point of the real-time emulated power network in RTDS is illustrated in Figure 6.15. The scaled-up voltage at the interfacing point presents the same trend as the hardware GFC during the soft energisation within the voltage ramp period. Through the implementation of the time delay compensation and power signal scaling, the hardware GFC voltage behaviour is replicated in the emulated power network.

The current at the interfacing point of the real-time emulated power network that is hosted in RTDS, as shown in Figure 6.15, is transmitted to the current-mode power amplifier as its command signal through proper scaling. Figure 6.14(b) and Figure 6.14(c) present the command signal received from RTDS and the output current of TP15 kVA power converter, respectively. The scaled-down ($r_i = 0.0133$) three-phase current is accurately transmitted to TP15 kVA and is well-tracked by the output current of TP15 kVA. As shown in the zoomed version of the command and output current around the end of the ramping time,

the actual output current is more harmonic-rich than the command signal. Despite the minor distortion of the output current, the phase of the power amplifier output current is aligned with that of the command signal. This is achieved by implementing the delay compensation method as presented in Section 6.3.4, through which the current behaviour in the emulated power network can be replicated by the power amplifier and be applied to the hardware GFC.

Through proper scaling and delay compensation, a stable and accurate simulation can be achieved by applying the current-type interface to incorporate a hardware GFC into a PHIL closed-loop. This can effectively tackle the stability issue of the voltage-type interface as presented in Section 6.4.1.

6.6 Summary

This chapter presents a novel interfacing method along with its associated optimisation and compensation schemes that enable the incorporation of GFC with black-start capability into a PHIL closed-loop setup.

Firstly, a comprehensive assessment and evaluation of the voltage-type PHIL interface regarding its suitability and applicability for incorporating GFC with black-start capability into PHIL closed-loop simulation were presented. The theoretical analysis and simulation results revealed the stability issue arising from the lack of voltage synchronisation at the coupling point between GFC and power amplifier in a voltage-type interface. Moreover, the limitation of partial circuit duplication method based interface in incorporating GFC with black-start capability into PHIL setup has been highlighted. These analyses have revealed the necessity for a robust PHIL interface with high-fidelity to effectively test GFC with black-start capability.

Secondly, to address the limitations and stability issues of the voltage-type PHIL interface, a current-type interfacing method was proposed to interface a

GFC with soft black-start capability into a PHIL setup. The in-depth modelling of the current-type PHIL interface has been presented along with stability analysis. In addition, interface optimisation including proper scaling and time delay compensation have been proposed to facilitate the testing capability and to improve the simulation accuracy. Furthermore, the proposed scaling method has been validated by the stability criteria defined in Chapter 2.

Finally, the experimental results involving the employment of a 90 kVA hardware GFC to energise a power network with a ramping voltage reference for the VSM control loop were illustrated. These outcomes demonstrated its effectiveness in tackling the stability issue arising from the lack of voltage synchronisation at the coupling point of GFC and interfacing power amplifier, and indicate the suitability and applicability of a current-type interface in incorporating hardware GFC into a PHIL setup.

Overall, this chapter presents a novel current-type interface that paves a new pathway for testing GFC with black-start capabilities in a PHIL setup. Furthermore, the proposed optimisation and scaling schemes support the adoption of this technique for further experimental validation of GFC over extended testing scenarios. This is of great significance in facilitating the integration of renewable energy sources into modern power networks.

Chapter 7

Conclusions and Future Work

PHIL techniques pave a new pathway in facilitating the real-time testing and rapid prototyping of novel power apparatus and in investigating the interactions between the candidate apparatus and their associated control schemes with the large-scale complex power grid, while offering a variety of attractive attributes involving the flexibility, redundancy, high-configurability, repeatability, and cost effectiveness of non-destructive real-time closed-loop testing. This is of great significance in promoting the research and development of novel power apparatus and accelerating the transition of modern power grid. However, in analogy to other emerging technologies, PHIL technique is accompanied by challenges and limitations in realising a robust and high-fidelity real-time simulation, with the mitigation of detrimental behaviours arising from the interfacing components and system impedance variations being the most prominent.

This thesis focused on the development of compensation methodologies for mitigating the detrimental impact of non-ideal power interface characteristics (e.g., time delay, limited bandwidth, signal distortion) and system impedance variation, thereby enhancing the stability and accuracy of PHIL simulation. These proposed methodologies include:

- A real-time impedance aided Smith predictor compensator with adaptivity to system impedance variation for enhanced PHIL stability.
- An optimal filter tuning based method for maximising the bandwidth and preserving unity-gain characteristics of the power interface over a wider frequency range.
- Sliding DFT based time delay compensation on a harmonic-by-harmonic basis for more accurate power synchronisation and power transfer within the PHIL setup.
- A scheme for sensitivity analysis of the PHIL setup for quantitatively analysing the impact of external disturbance on PHIL interfacing signals and their associated stability and accuracy assessment.
- A current-type interface with proposed scaling ratio and time delay compensation for incorporating GFCs with black-start capabilities into a PHIL setup with enhanced stability and accuracy.

The following sections conclude this thesis by summarising the general research findings, outlining the scope of research outputs, and highlighting the principle novel contributions. These are followed by identifying several potential directions that are worth being undertaken as future work.

7.1 Conclusions

From the research point of view, the contributions stemming from the research work undertaken throughout this thesis can be attributed to the following distinct key knowledge streams, which are subsequently presented in detail in the following subsections.

7.1.1 Methodology to Extend the Operating Boundaries of PHIL with Enhanced Stability

A comprehensive review and in-depth analysis of the PHIL stabilisation schemes have been performed in Chapter 2 from the perspective of the effectiveness in enhancing PHIL stability, the impact on simulation accuracy along with the ease of implementation of these schemes. This review and analysis in conjunction with the assessment of the impact of time delay and variable system impedance ratio on PHIL stability have provided valuable insights for the PHIL community. This includes identifying the key determinants for PHIL stability and developing a novel compensation methodology for achieving a stable and robust PHIL simulation by compensating for these identified determinants.

The mechanism by which the time delay and inherent variable PHIL system impedance ratio deteriorates the PHIL closed-loop stability has been identified in Chapter 2. This revealed that the PHIL stability can only be maintained within a stringent impedance ratio range, thereby the PHIL operating boundaries are constrained in one experimental scenario run. Most of the reviewed PHIL stabilisation schemes in the literature were designed without taking the inherent impedance variation characteristic and the stringent impedance ratio boundary into account. However, the real-world PHIL may witness significant impedance variation when single or multiple power apparatus are connected and disconnected. To fill this research gap between the enhanced PHIL stability and the inherent variable impedance characteristic of the PHIL system, the Smith predictor criterion inspired and system impedance identification aided adaptive compensator was proposed to enhance the PHIL stability and to enable a robust PHIL operation over extended operating boundaries.

Through the studies and assessment of the proposed adaptive Smith predictor compensator in Chapter 3, the following conclusions have been drawn:

- The theoretical analysis revealed that the proposed compensator mitigates the deteriorating impact of the time delay on PHIL closed-loop stability by virtually shifting it to the open-loop. Consequently, this enables a delay-free closed-loop system with an improved stability margin.

- The improved stability margin extends the impedance ratio that can be raised before breaching the system stability, thereby introducing a buffer in the variability of impedances, extending the operating boundaries of PHIL experiment, and enabling a stable PHIL experiment over a wider range of scenarios. This has been validated by both simulation and experiment, which demonstrated that the compensator aided example PHIL setup maintains stability with an extended impedance ratio from IR_0 to $1.3\,\mathrm{IR}_0$.

- The stability boundary and its associated critical impedance ratio for the passive SP compensator have been defined and demonstrated by analytical assessment. This provides the compensator designer with an efficient tool to quantitatively assess the extent to which the modelling error between the estimated model in the compensator and the actual model can be tolerated before the modelling error breaches the stability criterion. This has been validated by analytical assessment and simulation, which demonstrated that the passive compensator-based example PHIL setup can only maintain stability up to a critical impedance ratio IR_C as $2.88\,\mathrm{IR}_0$, beyond which the interfacing signals are divergent and the system reaches an unstable state.

- Having identified the limitation of passive SP compensator, a computationally efficient SDFT based on-line impedance identification method was proposed to enhance the robustness of SP compensator. The effectiveness of this online impedance measurement technique has been validated by simulation and experimental results, of which strong agreement between the estimated impedance transfer function and the reference impedance transfer

function has been achieved.

- This impedance identification technique allows the estimated model of the Smith predictor to be adapted in real-time and equips the compensator with adaptivity to impedance variation, thereby ensuring seamless operation catering to impedance variation during the experimental run. This further extends the operating boundaries of a PHIL setup with enhanced stability and allows for undertaking PHIL experimental validation over wider testing scenarios.

- A comparative assessment of the passive compensator and impedance-aided adaptive compensator have been performed by employing a real-world PHIL experiment involving passive load bank and a 90 kVA back-to-back power converter. The experimental results have demonstrated the effectiveness of online impedance identification units and the merits of the proposed adaptive compensator over the passive compensator in extending the PHIL operating boundaries with guaranteed stability.

To sum up, the analytical assessment, simulation and experimental results have demonstrated that the proposed adaptive SP compensator enables a stable PHIL system over a wider range of impedance ratios, allowing for a broader range of scenarios being investigated at one experimental run than that of a PHIL system without the proposed compensator. Although the applicability of the proposed adaptive SP compensator in this thesis has only been shown with passive loads for the purpose of proof of concept demonstration, this methodology possesses the potential for being extended to a stable PHIL setup incorporating multiple parallel power converters or physical power networks that present inherent impedance variation on a common basis. This will push beyond the existing limits of PHIL simulation towards a more stable operation that enables a more robust PHIL experimental validation over extended operating boundaries.

7.1.2 Optimisation and Compensation for a High-Fidelity PHIL Interface

An analytical assessment of the impact of non-ideal interface characteristics involving the time delay, signal distortion, and limited bandwidth on the power signal synchronisation and power transfer transparency within the PHIL setup has been performed in Chapter 2. Acknowledging the importance of power signal synchronisation and transparent power transfer for the accurate replication of the HuT dynamics on the emulated power network hosted in DRTS, this thesis developed optimisation and compensation approaches for realising a high-fidelity PHIL interface. The proposed optimisation and compensation approaches enable an extended bandwidth of the compensated power interface and preserve unity gain over a wider frequency range than that of the uncompensated interface, while also compensating for the phase lag arising from the inherent time delay on a harmonic-by-harmonics basis. These proposed approaches and their associated optimised characteristics enable enhanced accuracy in a PHIL setup. The following sections will conclude each proposed approach in detail.

(1) Open-Loop Controlled VSC Amplifier and Optimal Filter Tuning

An optimal filter tuning based method was proposed to compensate for the output filter of the open-loop controlled VSC-based interfacing power amplifier, which presents less time delay associated with sampling and computation than the closed-loop controlled VSC. Through the optimal tuning of the optimum damping ratio ζ_{op} to be $\frac{\sqrt{2}}{2}$ of the proposed compensator, the compensated filter is equivalent to a second-order Butterworth filter with maximally flat magnitude response over an extended frequency range and presents the following characteristics:

- **Unity gain over a wider frequency range**: The analytical assessment presented in Chapter 3 has demonstrated that the compensated PA output

filter preserves unity gain over a wider frequency range (0 Hz-830 Hz) than that of the uncompensated output filter (98.7 Hz-100.2 Hz). This ensures the magnitude of the power amplifier output voltage remains consistent with that of its reference voltage over an extended frequency range, thereby ensuring an accurate power signal replication, mitigating the impact of non-unity power amplifier magnitude on the power transfer transparency.

- **Improved bandwidth**: By implementing the proposed compensator with the ratio between the resonant frequency of the proposed compensator and that of the power amplifier output filter tuned to be 3, the bandwidth (5300 Hz) of the equivalent compensated power amplifier output filter presents a remarkable increase by around 2.6 times of the bandwidth (2000 Hz) of the uncompensated output filter. The improved bandwidth enhanced the PHIL capability for more accurate replication of high-frequency reference signal that includes certain harmonics in the PHIL simulation with different testing objectives.

(2) SDFT Based Time Delay Compensation

Having enabled the unity gain of power interface, SDFT based time delay compensation method is further proposed to compensate for the phase lag by manipulating the reference signal and adding an additional phase shift. The analysis of SDFT frequency response revealed that it can selectively update the reference signal at frequencies of interest without magnitude distortion, thereby enabling time delay compensation on a harmonic-by-harmonic basis.

The effectiveness of the proposed optimal filter tuning in conjunction with the delay compensation has been validated by the proposed accuracy metrics in a quantitative manner. The proposed compensation aided power interface presents less power signal tracking error and reduced power signal to reference power signal error than the uncompensated power interface. On the other hand,

the simulation results demonstrated that the proposed compensation approaches based interface presents consistent power measurement on DRTS and HuT side. These provide high-level confidence that the proposed compensation method is efficient for improving the signal synchronisation accuracy and enhancing the power transfer transparency, which are critical for designing a high-fidelity PHIL interface.

7.1.3 A Novel Scheme for Sensitivity Analysis of PHIL Setups

A sensitivity analysis scheme has been developed to fill the research gap whereby a structured analysis and evaluation has not been previously possible for assessing the impact of external disturbances on PHIL performance. Through the analytical assessment and experimental validation of the proposed sensitivity analysis scheme in Chapter 5, the following conclusions have been drawn:

- A sensitivity metrics based scheme has been proposed for the purpose of PHIL sensitivity analysis and assessment of PHIL robustness and performance with respect to the potential disturbances stemming from the power interface. The proposed sensitivity metrics have been validated by their frequency domain analytical assessment and an I-ITM based PHIL experimental validation, for which strong agreement between the sensitivity metrics frequency response and PHIL experimental results regarding the interfacing phase shift and magnitude response has been achieved. These demonstrate the applicability of the proposed sensitivity analysis scheme.

- The inherent relationships between the proposed sensitivity analysis scheme and the stability criterion have been theoretically defined by a set of criteria. The system stability performance of a PHIL experimental validation

involving grid side impedance change was aligned with the analytical assessment of the defined criterion. This is important for evaluating the enhanced PHIL stability properties prior to its deployment.

- Accuracy assessment methods involving SNR and THD+N were employed to quantify the generic sensitivity criteria. These accuracy criteria have been applied to the PHIL experimental validation for accuracy evaluation in a reproducible manner. From an application point of view, the proposed scheme is crucial for facilitating the quantitative analysis and assessment of the impact of external disturbances on PHIL performance.

Overall, the analytical assessment along with the power converter based PHIL experimental validation demonstrate the applicability of the proposed sensitivity analysis scheme for PHIL setups. The proposed scheme is introduced as a guideline for the PHIL research community by providing high-value information regarding the system disturbance assessment, accuracy quantification, and system stability analysis. So the design and implementation of a high-fidelity and robust PHIL setup are consequently supported.

7.1.4 Approach for Incorporating GFC with Black-Start Capability into PHIL Setups

For the purpose of addressing the limitation of the extensively utilised voltage-type PHIL interface, a current-type interfacing method was proposed to interface a GFC with soft black-start capability into a PHIL setup. Based on the research findings as presented in Chapter 6, the following conclusions have been drawn:

- The suitability and applicability of the voltage-type PHIL interface for incorporating a GFC with black-start capability has been theoretically analysed along with a simulation-based verification, which demonstrates the stability issue arising from the lack of voltage synchronisation at the coupling

point between GFC and power amplifier. On the other hand, the limitation of partial circuit duplication method based interface has been highlighted. These offer meaningful insights for the PHIL users on selecting a proper interface for GFC testing, in particular for black-start applications.

- To address the identified limitation of the voltage-type interface, a current-type interface was proposed to incorporate a GFC with black-start capability into a PHIL setup. Detailed system modelling was presented along with scaling and compensation schemes, which were proposed for enabling a robust and high-fidelity PHIL simulation, facilitating the testing capability, and guaranteeing an accurate replication of the dynamics of emulated power network at the physical GFC interfacing point.

- Stability analysis has been presented by utilising the stability criteria defined in Chapter 2 to support the selection of the proposed scaling ratio. This is of great importance to support the adoption of the proposed interface prior to its deployment.

- A PHIL experiment involving the employment of a hardware GFC to energise a DRTS-hosted power network with a ramping voltage reference for the VSM control loop has been presented. The experimental results demonstrated that a robust and high-fidelity PHIL testing of GFC can be achieved by applying the current-type PHIL interface in conjunction with the proposed interface compensation methods. This further verified the applicability of the current-type interface for GFC testing with black-start capability and provided high-level confidence in the adoption of this technique for further experimental validation of GFC over extended testing scenarios. The experiment gave valuable insight regarding the integration of a new GFC controller for UK black start services.

7.2 Future Work

Based on the findings, discussions and conclusions of the accomplished research work, this section presents the following topics that are identified as potential research directions to be explored in the future.

7.2.1 Enhanced Smith Predictor with Advanced Impedance Identification Methods

As discussed in Chapter 3.5, despite the proposed adaptive Smith predictor contributing to enhanced stability and improved transient or steady-state performance, its online impedance identification approach limits its applicability when the PHIL system witnesses fast impedance change. This arises from the natural circular signal processing attribute of GSDFT based online impedance identification scheme that requires one-cycle processing time (i.e., 0.02 s) for calculating the impedance parameters and updating the Smith predictor.

To facilitate the applicability of the proposed methodology, the development of faster online impedance parameter identification schemes (e.g., Luenberger observer [103], Kalman filters [104]) can enhance the applicability of the proposed methodology for faster impedance change scenario. Even though these require a more complex implementation than the proposed one, they indeed present the potential in improving the applicability of this proposed methodology for transient studies by tackling the one-cycle processing issue of SDFT. This forms an interesting direction for future research.

7.2.2 Smith Predictor with Extended Testing Scenarios

As demonstrated in Chapter 3, the proposed adaptive Smith predictor scheme stabilises the PHIL system with inherent impedance variation. Even though the applicability of the proposed approach in this chapter has been limited to

passive loads for the purpose of proof of concept demonstration, this approach is extendable and applicable in theory for a stable PHIL system incorporating parallel connected power converters, active or passive loads, or even a power network, of which the equivalent impedance may witness variation when single or multiple power apparatus are connected and disconnected. This can be explored in the frame of future research.

7.2.3 Modified Smith Predictor for Enhanced PHIL Disturbance Rejection Capability

Acknowledging that the inherent disturbances stemming from the power interface play a significant role in deteriorating PHIL simulation accuracy as demonstrated in Chapter 5, a compensation technique that equips the PHIL setup with disturbance rejection capability is desired for further enhancing its fidelity. The online impedance identification aided adaptive Smith predictor compensator not only enhances the PHIL closed-loop stability but also possesses potential in enhancing the PHIL disturbance rejection capability. This could be achieved by implementing a buffer to the estimated system model in the Smith predictor for attenuating the disturbance signal to a very low level. This forms an interesting direction for further refining the proposed Smith predictor for enhancing the PHIL disturbance rejection capability.

7.2.4 Comprehensive Assessment of Various PHIL Interface Algorithms for Black-Start Testing of GFCs

In this thesis, the V-ITM and I-ITM interfaces have been well assessed from the perspective of their capability in incorporating GFC with black-start capability into a PHIL setup. However, the interface algorithms as listed in Chapter 2 and their extended ones may have a better performance than the proposed method.

From a research and application point of view, a comprehensive analysis and assessment of these interface algorithms regarding their suitability, applicability, and capability for testing GFC are of great value. Based on this, modifications and optimisation of these interface algorithms can be carried out to facilitate the application of novel PHIL techniques for GFC testing in the future.

7.2.5 Applying PHIL for Testing GFC with Black-Start Capability over Wider Scenarios

The experiment in Chapter 6 is limited to the VSM-based soft voltage ramp-up for the purpose of proof of concept demonstration and preliminary validation of the applicability of current-type interface and its associated compensation techniques. Recommended future work includes expanding the testing of current-type interface to cover all the black-start scenarios (e.g., load pickup, grid synchronisation, etc.). Correspondingly, stability analysis of this interface with the variable impedance over each black-start stage should be taken into account for further assessment of this interface. On the other hand, incorporating multiple GFCs as HuT into the PHIL setup also forms an interesting research direction to explore. This will mainly involve the investigation of the impact of multiple GFCs and their coordinated operation on the PHIL stability and accuracy performance.

Appendix A

Impedance Coefficients Calculation Method in Chapter 3

This section presents the detailed method that is applied to calculate the impedance transfer function based on the frequency-domain measurement. Furthermore, the example impedance calculation that is associated with Chapter 3.3.3 is presented.

A.1 Impedance Calculation Linearisation

The vector fitting linearisation method as elaborated in [75, 76] is applied to the non-linear matrices in Eq. (3.21) to converter it into a set of linear algebraic equations, which can be expressed as,

$$\mathbf{PC} = \mathbf{Q}\,, \tag{A.1}$$

where $\mathbf{P}$, $\mathbf{C}$, and $\mathbf{Q}$ are given by,

$$\begin{cases} \mathbf{C} &= [a_0, a_1, a_2, a_3, \cdots, b_1, b_2, b_3, b_4, \cdots]^T, \\ \mathbf{Q} &= [R_0, I_1, R_2, I_3, \cdots, 0, M_2, 0, M_4, \cdots]^T, \end{cases} \tag{A.2}$$

$$\mathbf{P} = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & 0 & \lambda_4 & \cdots & I_1 & R_2 & -I_3 & R_4 & \cdots \\ 0 & \lambda_2 & 0 & -\lambda_4 & 0 & \cdots & -R_2 & I_3 & R_4 & -I_5 & \cdots \\ \lambda_2 & 0 & -\lambda_4 & 0 & \lambda_6 & \cdots & I_3 & R_4 & -I_5 & -R_6 & \cdots \\ 0 & \lambda_4 & 0 & -\lambda_6 & 0 & \cdots & -R_4 & I_5 & R_6 & -I_7 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \\ I_1 & -R_2 & -I_3 & R_4 & I_5 & \cdots & M_2 & 0 & -M_4 & 0 & \cdots \\ R_2 & I_3 & -R_4 & -I_5 & R_6 & \cdots & 0 & M_4 & 0 & M_6 & \cdots \\ I_3 & -R_4 & -I_5 & R_6 & I_7 & \cdots & M_4 & 0 & -M_6 & 0 & \cdots \\ R_4 & I_5 & -R_6 & -I_7 & R_8 & \cdots & 0 & M_6 & 0 & -M_8 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \end{bmatrix}. \quad \text{(A.3)}$$

According to the vector fitting linearisation method in [75, 76], the elements in matrices $\mathbf{P}$ and $\mathbf{Q}$ are defined by GSDFT output frequency-domain data in Eq. (3.16) and are given by,

$$\begin{cases} \lambda_h &= \sum_{k=1}^{K} {w_k}^h, \\ R_h &= \sum_{k=1}^{K} {w_k}^h \mathrm{Re}_k, \\ I_h &= \sum_{k=1}^{K} {w_k}^h \mathrm{Im}_k, \\ M_h &= \sum_{k=1}^{K} {w_k}^h ({\mathrm{Re}_k}^2 + {\mathrm{Im}_k}^2). \end{cases} \quad \text{(A.4)}$$

Based on Eq. (A.1), matrix $\mathbf{C}$ that is comprised by the numerical values of the coefficient matrices $\mathbf{A}$ and $\mathbf{B}$ are further calculated by,

$$\mathbf{C} = \mathbf{P}^{-1}\mathbf{Q}. \quad \text{(A.5)}$$

By doing so, the coefficients of the estimated impedance transfer function in Eq. (3.21) are obtained.

A.2 Impedance Calculation Example

Taking the identification of impedance Z_{H3} in Table 3.3 as an example, based on the externally injected excitation signals, the GSDFT output frequency-domain data is given by,

Table A.1: Frequency-domain impedance (Z_{H3}) response data

k	w_k(rad)	Re_k	Im_k	Mag(dB)	Phase(deg)
1	314.16	$6.183\,e^{-4}$	0.322	-9.84	89.89
2	628.32	0.012	0.695	-3.15	89.04
3	942.48	0.075	1.190	1.53	86.40
4	1256.62	0.338	1.907	5.74	79.96
5	1570.80	1.280	2.812	9.80	65.53
6	1885.02	3.401	2.656	12.70	37.99
7	2199.16	4.212	0.538	12.56	7.27
8	2513.32	3.376	-0.659	10.73	-11.05
9	2827.46	2.633	-0.949	8.94	-19.81
10	3141.59	2.168	-0.962	7.50	-23.93
11	3769.87	1.682	-0.838	5.48	-26.48
12	4398.20	1.450	-0.713	4.17	-26.20
13	5026.53	1.320	-0.615	3.26	-24.99
14	5654.87	1.240	-0.539	2.62	-23.50

Table 3.3 presents the frequency-domain transfer function of Z_{H3}, a RLC impedance that can be represented as an inductor in parallel with a cascaded resistor and capacitor. Accordingly, the matrices $\mathbf{A}$ and $\mathbf{B}$ are expressed as,

$$\mathbf{A} = [a_0, a_1, a_2]^T,\ \mathbf{B} = [1, b_1, b_2]^T. \tag{A.6}$$

According to the vector fitting linearisation method, the matrices $\mathbf{P}$, $\mathbf{C}$, and $\mathbf{Q}$ in Eq. (A.2) and Eq. (A.3) are further given by,

$$\begin{cases} \mathbf{C} &= [a_0, a_1, a_2, b_1, b_2]^T, \\ \mathbf{Q} &= [R_0, I_1, R_2, 0, M_2]^T, \end{cases} \tag{A.7}$$

$$\mathbf{P} = \begin{bmatrix} \lambda_0 & 0 & -\lambda_2 & I_1 & R_2 \\ 0 & \lambda_2 & 0 & -R_2 & I_3 \\ \lambda_2 & 0 & -\lambda_4 & I_3 & R_4 \\ I_1 & -R_2 & -I_3 & M_2 & 0 \\ R_2 & I_3 & -R_4 & 0 & M_4 \end{bmatrix}. \tag{A.8}$$

Substituting the frequency domain data in Table A.1 into Eq. (A.4), the elements in matrices $\mathbf{P}$ and $\mathbf{Q}$ are calculated as,

$$\begin{cases} \lambda_0 = \sum_{k=1}^{14} {w_k}^0 = 14, & R_0 = \sum_{k=1}^{14} {w_k}^0 \mathrm{Re}_k = 23.185, \\ \lambda_2 = \sum_{k=1}^{14} {w_k}^2 = 1.288\, e^8, & R_2 = \sum_{k=1}^{14} {w_k}^2 \mathrm{Re}_k = 2.249\, e^8, \\ \lambda_4 = \sum_{k=1}^{14} {w_k}^4 = 2.484\, e^{15}, & R_4 = \sum_{k=1}^{14} {w_k}^4 \mathrm{Re}_k = 3.657\, e^{15}, \\ I_1 = \sum_{k=1}^{14} {w_k}^1 \mathrm{Im}_k = -5.134\, e^3, & M_2 = \sum_{k=1}^{14} {w_k}^2 ({\mathrm{Re}_k}^2 + {\mathrm{Im}_k}^2) = 5.898\, e^4, \\ I_3 = \sum_{k=1}^{14} {w_k}^3 \mathrm{Im}_k = -3.035\, e^{11}, & M_4 = \sum_{k=1}^{14} {w_k}^4 ({\mathrm{Re}_k}^2 + {\mathrm{Im}_k}^2) = 7.158\, e^{15}. \end{cases} \tag{A.9}$$

Substituting the numerical value in Eq. (A.9) into Eq. (A.7) and Eq. (A.8), and utilising Eq. (A.5), matrix $\mathbf{C}$ is calculated as,

$$\mathbf{C} = \mathbf{P}^{-1}\mathbf{Q} = [1.245\, e^{-4}, 9.856\, e^{-4}, 2.505\, e^{-7}, 2.469\, e^{-4}, 2.521\, e^{-7}]^T. \tag{A.10}$$

Consequently, matrices $\mathbf{A}$ and $\mathbf{B}$ are obtained as,

$$\mathbf{A} = [1.245\, e^{-4}, 9.856\, e^{-4}, 2.505\, e^{-7}]^T,\ \mathbf{B} = [1, 2.469\, e^{-4}, 2.521\, e^{-7}]^T. \tag{A.11}$$

$\mathbf{A}$ and $\mathbf{B}$ are further expressed into a transfer function form as in Table 3.3.

Appendix B

Examples of VSC Output Filter and HuT Impedance

Depending on the type of the HuT load (Z_{H}), the equivalent transfer function of output filter and HuT impedance in Eq. (4.3) can be expressed as,

Infinite load ($Z_{\mathrm{H}} = \infty$)

$$\begin{aligned} G_f(s) &= \frac{1}{L_f C_f s^2 + R_f C_f s + 1}, \\ &= \frac{1}{\frac{s^2}{(w_0)^2} + 2\frac{\xi}{w_0} s + 1}, \end{aligned} \tag{B.1a}$$

$$w_0 = \frac{1}{\sqrt{L_f C_f}},\ \xi = \frac{R_f}{2}\sqrt{\frac{C_f}{L_f}}\,, \tag{B.1b}$$

where w_0 is the natural frequency, ξ is the damping ratio, and the resonant frequency w_r ($w_r = w_0\sqrt{1-2\xi^2}$).

Resistive HuT ($Z_{\mathrm{H}} = R_{\mathrm{H}}$)

$$\begin{aligned} G_f(s) &= \frac{1}{L_f C_f s^2 + (R_f C_f + \frac{L_f}{R_{\mathrm{H}}})s + (1 + \frac{R_f}{R_{\mathrm{H}}})}, \\ &= \frac{1}{\frac{s^2}{(w_0)^2} + 2\frac{\xi}{w_0}s + (1 + \frac{R_f}{R_{\mathrm{H}}})}, \end{aligned} \tag{B.2a}$$

$$w_0 = \frac{1}{\sqrt{L_f C_f}},\ \xi = \frac{R_f C_f + L_f/R_{\mathrm{H}}}{2}\sqrt{\frac{1}{L_f C_f}}\ , \tag{B.2b}$$

where w_0 is the natural frequency, ξ is the damping ratio, and the resonant frequency w_r ($w_r = w_0\sqrt{1 + \frac{R_f}{Z_{\mathrm{H}} - 2\xi^2}}$).

Inductive HuT ($Z_{\mathrm{H}} = R_{\mathrm{H}} + sL_{\mathrm{H}}$)

$$G_f(s) = \frac{sL_{\mathrm{H}} + R_{\mathrm{H}}}{\mathrm{A}s^3 + \mathrm{B}s^2 + \mathrm{C}s + \mathrm{D}}, \tag{B.3a}$$

where

$$\begin{bmatrix} \mathrm{A} & \mathrm{B} \\ \mathrm{C} & \mathrm{D} \end{bmatrix} = \begin{bmatrix} L_f C_f L_{\mathrm{H}} & L_f C_f R_{\mathrm{H}} + R_f C_f L_{\mathrm{H}} \\ R_f C_f R_{\mathrm{H}} + L_f + L_{\mathrm{H}} & R_f + R_{\mathrm{H}} \end{bmatrix}. \tag{B.3b}$$

Appendix C

PHIL Setup Parameters Used in Chapter 5

The parameters of V-ITM interface based PHIL setup in Chapter 5 are tabulated in Table C.1. Note that the signal processing card (i.e., GTAO card) $G_1^{\mathrm{v}}(s)$ is assumed to be ideal, whereas the modelling of the voltage amplifier includes a delay of 3.1 µs characterized as an exponential function in $G_2^{\mathrm{v}}(s)$. For the feedback loop, the current sensor is considered to be ideal with $G_3^{\mathrm{v}}(s) = 1$, while the GTAI card in series with the low-pass filter are modelled as in Eq. (2.2) with a cut-off frequency of 350 Hz.

PHIL experimental setup parameters used for the analysis of I-ITM interface in Chapter 5 are given in Table C.2. For this setup, the time step size and the fundamental frequency are set as 50 µs and 50 Hz, respectively and the line-to-line software side voltage is 400 V. The forward signal processing (i.e., GTAO card) and the feedback voltage measurement are assumed to be ideal, thus respective transfer functions $G_1^{\mathrm{i}}(s)$ and $G_3^{\mathrm{i}}(s)$ are equal to 1. The current-type PA shows a low-pass behaviour with a cut-off frequency of 768 Hz. The cut-off frequency of $G_4^{\mathrm{i}}(s)$ is 1500 Hz. DRTS and HuT system impedances including grid impedance properties as well as the converter output impedance are shown in Table C.2.

Table C.1: Model parameters of the PHIL setup with V-ITM interface

Description	**Symbol**	**Unit**	**Value**
RTDS time step	-	µs	50
Software side voltage source	$V_{\mathrm{S,LN}}$	V	230
Fundamental frequency	f_0	Hz	50
Software system impedance	$Z_{\mathrm{S}}(s)$	Ω	0.8
Hardware system impedance	$Z_{\mathrm{H}}(s)$	Ω	54
Voltage-type PA-Equivalent delay and filter as identified in [54]	$G_2^{\mathrm{v}}(s)$	-	$\frac{\mathrm{e}^{-s3.1\mathrm{e}^{-6}}}{s^2 2.642\mathrm{e}^{-13} + s0.8\mathrm{e}^{-6} + 1}$
Current measurement	$G_3^{\mathrm{v}}(s)$	-	1
Feedforward GTAO card	$G_1^{\mathrm{v}}(s)$	-	1
Feedback GTAI card + low-pass filter	$G_4^{\mathrm{v}}(s)$	-	$\frac{1}{(1/2\pi 350)s + 1}$

Table C.2: Model parameters of the PHIL setup with I-ITM interface

Description	**Symbol**	**Unit**	**Value**
RTDS time step	-	µs	50
Software side voltage source	$V_{\mathrm{S,LL}}$	V	400
Fundamental frequency	f_0	Hz	50
Software system impedance Emulated grid impedance	$Z_{\mathrm{S}}(s)$	Ω	$10 + s4.775\mathrm{e}^{-4}$
Hardware system impedance Converter output impedance [102]	$Z_{\mathrm{H}}(s)$	Ω	$\frac{s5.5\mathrm{e}^{-4} + 6.842}{s^2 5.5\mathrm{e}^{-4} + s3.216\mathrm{e}^{-4} + 1}$
Current-type PA Current control transfer function with delay compensation [32]	$G_2^{\mathrm{i}}(s)$	-	$\frac{1}{(1/2\pi 768)s + 1}$
Voltage measurement	$G_3^{\mathrm{i}}(s)$	-	1
Feedforward GTAO card	$G_1^{\mathrm{i}}(s)$	-	1
Feedback GTAI card + low-pass filter	$G_4^{\mathrm{i}}(s)$	-	$\frac{1}{(1/2\pi 1500)s + 1}$

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