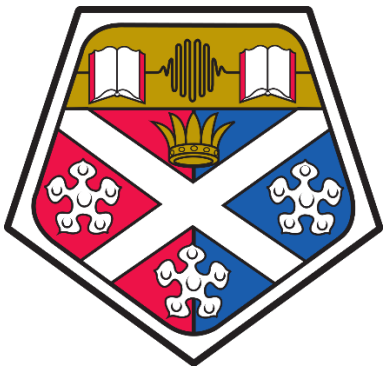

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Analysis and Design of the Modular Multilevel Converter for Secure Systems

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B.Sc. (*honours*), M.Sc. (*honours*)

A thesis presented in fulfilment of the requirements for the degree of Doctor of Philosophy

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To my family

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Abstract

This thesis investigates the operation, dynamics and design of modular multilevel converters (MMCs) for stable and reliable operation.

The internal dynamics and control schemes of the conventional MMC is analysed with consideration of passive component tolerances. Detail qualitative and quantitative analysis of MMC internal dynamics with different control strategies, is performed. Inter-arm passive component tolerances lead to fundamental and higher odd-order harmonics in the common-mode loop, which may cause external oscillation in the dc-link.

Considering the technical characteristics of the half-bridge SM (HB-SM) and full-bridge SM (FB-SM), a T-type MMC (T-MMC) consisting of two SM-based stages is proposed in this research. The first stage of the T-MMC is a conventional MMC; and the second stage is a series-connected flexible AC transmission system (FACTS) device. The reliability and stability of the converter are significantly increased, whereas flexible operation with various modes is attained. Also, converter ac and dc fault-tolerant capabilities become feasible. Two bypassing approaches are presented to reduce the conduction losses of the FB-SMs; therefore, the converter normal mode operation efficiency becomes similar to that of the conventional MMC.

The T-MMC integrated with energy storage elements (ESEs) is studied, and it is found that the T-MMC based energy storage system (ESS) can not only isolate faults but maintain continuous power for the normal side, which greatly improves stability and reliability of the connected systems. A T-MMC based multi-terminal high voltage dc (HVDC) network is studied, indicating the effectiveness of the T-MMC in power system scenarios.

The presented investigation and design are supported by theoretical analysis, simulation, and experimentation.

List of Abbreviations

ADC	Analog-digital conversion
DMA	Direct memory access
ESS	Energy storage system
FB	Full bridge
HB	Half bridge
HVDC	High voltage direct current
LCC	Line-commutated converter
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristor
MMC	Modular multilevel converter
MVDC	Medium voltage direct current
NLC	Nearest level control
PCC	Point of common coupling
PI	Proportional integral
PR	Proportional resonance
SM	Submodule
STATCOM	Static synchronous compensator
T-MMC	T-Type modular multilevel converter
TSG	Thyristor-SM group
UFBS	Ultra-Fast bypass switch
USG	UFBS-SM group
VSC	Voltage source converter

List of Symbols

V_{dc}	DC-Link voltage
I_{dc}	DC-Link current
v_{ac2}	AC grid voltage
v_{io}	Converter output voltage of one phase
C_{SM}	Submodule capacitance
V_{cijk}	Capacitor voltage of the specific SM
V_{cijk}^{*}	Specific SM capacitor voltage reference
Kb_{ijk}	Proportional gain of V_{cijk} controller
N	SM number per MMC arm
I_{icm}	MMC common-mode current
ω	First-Order angular velocity
v_{ac}	Converter output voltage
v_{g}	Grid (PCC) voltage
$v_{g'}$	Referred grid (PCC) voltage
C_{HB}	HB-SM capacitance
C_{FB}	FB-SM capacitance
P	Active power
Q	Reactive power
M	TSG/USG number per phase
N'	FB-SM number for Stage-II
P_{dc}	DC power
P_{ESE}	Energy storage element power
T_{ESS}	ESS operating duration

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Chapter 1

Introduction

This chapter introduces background and motivation of the presented research. Also, the research objectives and thesis organization are outlined.

1.1 Background

Electric power generation, transmission and distribution require high reliability, resiliency and security; therefore, power electronic solutions are in high demand, especially in bulk and critical electric power applications such as medium to high voltage direct current (MVDC/HVDC) systems, medium-voltage motor drives, and flexible ac transmission systems (FACTS) [1]-[4].

The terms voltage source and current source are generally used to classify power converters [5]. Current source converters (CSCs) have been historically used as solutions for line-commutated converters (LCCs) in HVDC systems [6] and CSC fed drives for electric motors [7], for example. However, the drawbacks are obvious, such as the limited controllability, vulnerability to commutation failure, etc. [5]-[8]. The voltage source converter (VSC) is now the preferred technology, as it offers more flexibility, such as independent control of active and reactive power, higher power quality, no minimum dc power flow, resilience to ac network disturbances and faults, etc. [9]-[13].

Among many VSC topologies for high power applications, the modular multilevel converter (MMC) has drawn considerable attention since it was proposed [10]. It is the preferable choice to overcome the voltage limitation of mainstream semiconductors [11]. Also, based on the concept of submodules (SMs) for scalability and modularity, MMCs exhibit other advantageous features, such as high reliability, high-quality ac/dc output waveforms, low semiconductor switching frequency, etc. [12]. These feature are especially attractive for medium and high voltage applications, and MMC-based systems have been widely implemented [13].

There are two typical MMC SM circuit configurations, namely, the half-bridge SM (HB-SM) and the full-bridge SM (FB-SM), which are shown in Fig. 1-1(a) and (b). The HB-SM offers simpler structure and lower losses, whereas the FB-SM provides a larger (bipolar) output voltage range. With the utilization and combination of different SMs, the MMC has different operational merits and drawbacks, which have been well-established [12]. Based on the HB-SM, half-bridge MMC (HB-MMC) is the most popular and fundamental topology, as shown in Fig. 1-2(a).

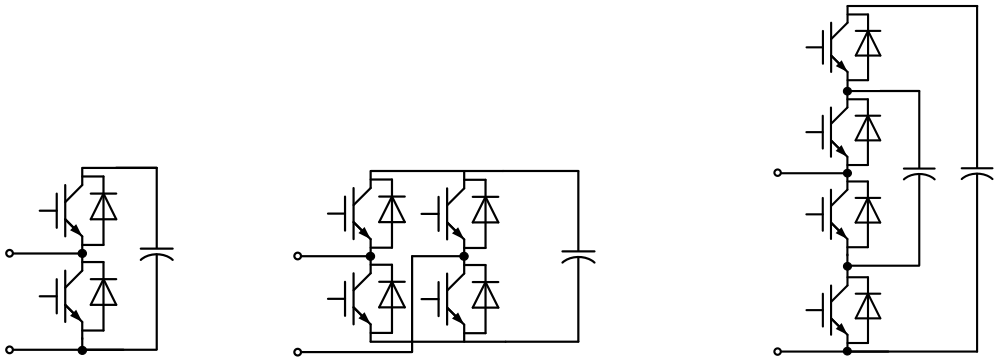

Fig. 1-1. Typical SM configurations: (a) HB-SM, (b) FB-SM, and (c) FC-SM.

The MMC control system is complex as the use of floating distributed capacitors in multilevel converters results in complex dynamics, which necessitates the adoption of a complex multi-layer control system for both the internal and external parts [11]. For example, the inner SM capacitor voltages affect the ac side voltage synthesis in terms of both differential and common mode ac voltage. To reduce undesirable internal and external coupling and maintain satisfactory performance, many control methods have been developed to suppress the circulating current, and regulate capacitor voltages to be independent of the dc-link voltage [14]-[16]. In terms of the MMC internal control system, SMs, arms and legs can be treated as three internal control layers from both topology and function points of view. MMC common-mode current, which consists of dc and harmonics, acts as a link between the energy of the dc side and submodule (SM) capacitors, which can be used to regulate the internal dynamics. SM capacitor voltage balancing is essential for both semiconductor safety and arm and leg level performance. To manage the voltage differences between SMs within each arm, SM voltage balancing algorithms based on either centralized or individual measures are employed [17], [18]. Research effort has been invested into higher-level controllers

(arm and leg level capacitor sum characteristics) [19], [20]. Although a large number of SMs may reduce the adverse effects of capacitance tolerance, component tolerance issues still exist; therefore, parametric uncertainty due to passive component tolerances should be taken into account during MMC design and maintenance [21]-[24]. The adverse effects on ac output voltage caused by MMC asymmetrical capacitance with three-level flying capacitor SMs (shown in Fig. 1-1(c)) are analysed when an energy-based balancing approach is adopted [22]. The existence of fundamental frequency ripple in the dc-link, due to asymmetrical arm inductances is highlighted and a voltage-based active control method is suggested in [23]. Thus, investigating the impact of MMC passive components and the effect of control system on both internal dynamics and external performance are required to achieve the desirable operation. This is also a demand of building secure MMC-based systems.

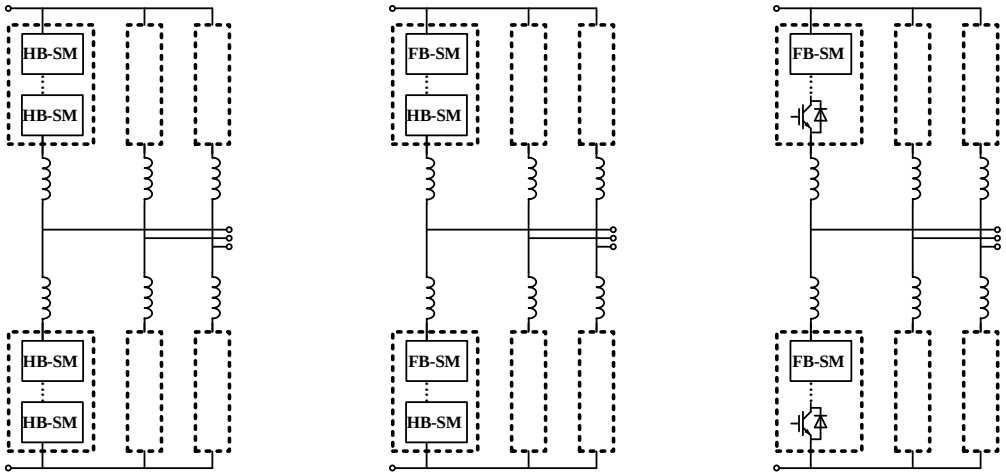

Fig. 1-2. Analysed topologies: (a) HB-MMC, (b) mixed-cell MMC, and (c) AAC.

From the topology point of view, the MMC basic topology can also be optimized for various requirements, to gain merits such as dc fault ride-through capability, smaller capacitor sizing or higher efficiency. In general, unipolar or bipolar voltage generation ability of SMs (HB-SM and FB-SM are representatives) determines the dc fault blocking competency of a converter [11], [12]. However, SMs with reverse-voltage blocking ability increase the number of switches in the main conduction path, impairing the high-efficiency feature of the overall converter. As a result, any design has to evaluate its constructed SMs and the trade-off between a larger arm operational range (indicating dc fault resilience) and lower semiconductor losses [24], [25].

Consequently, mixed-cell MMC types (shown in Fig. 1-2(b)) based on the combination of conventional HB-SM and other SMs (such as FB-SMs or degraded FB-SMs) have attracted attention as they balance efficiency and dc fault tolerance capability [26]-[30]. The alternate arm converter (AAC, as shown in Fig. 1-2(c)) based on director switches and FB-SMs has a compact size and dc fault isolation capability, but manipulation for waveform synthesis is difficult due to the hybrid use of director switches and FB-SMs within one arm [29]. An MMC based on unidirectional current FB-SMs is proposed with much lower IGBT usage and dc fault blocking capability; however, specific control systems and application scenarios are needed [30]. Another MMC construction deploys series-connected SMs in the ac side. These topologies, with a specific harmonic elimination modulation, were proposed to optimize the conventional two-level converter in terms of ac output quality, switching losses, and dc fault blocking ability [31]-[33]. Three-phase series and parallel hybrid MMCs were subsequently proposed based on the same director-switch concept [34]. However, the high *dv*/*dt* stress on the director switches is the main problem for high voltage applications, and although the series-connected configuration distributes the dc-link voltage into three levels, balancing capacitor voltages needs intricate control, especially during unbalanced grid faults. Then, topologies with sufficient FB-SMs were proposed in [35] and [36] to gain dc fault ride-through capability in HVDC applications, and the MMC behaves as a two-level converter using a quasi two-level modulation technique [37]. Aimed at connecting large wind turbines into the grid with the high-quality ac output, a hybrid MMC combines an HB-MMC with an FB-SM, as proposed in [38]. However, ac-side FB links of such designs are always in operation; thus, the mentioned trade-off is not overcome. Attracted by the salient conducting features of thyristors, researchers have integrated thyristor-based switches into VSCs. Four hybrid topologies combining SMs with line-commutated converters (LCCs) were reviewed in terms of active and reactive power capabilities [39]. With the design concept inherited from LCCs, various VSC configurations based on FB-SMs and thyristor strings have been investigated [40]-[43]. However, different from the conventional LCC implementation, the series-connection of thyristors requires higher-performance voltage-balancing and signal-synchronizing techniques for thyristor forced-commutation approaches, and sophisticated and lengthy turn-on/off processes

occur at the fundamental frequency, which may result in voltage-balancing or thyristor commutation failure. A novel dc-fault tolerant MMC was proposed, with fully-controllable thyristors (IGCTs or GTOs) adopted for switching action; nevertheless, the major issue is that thyristor high voltage and current capabilities are not fully utilized [44]. It can be concluded that an MMC with dc fault isolation functionality and without jeopardizing normal operation is required when constructing secure systems. Also, secure systems may require not only protective measures but smooth operation under various conditions. This additional requirement is basically in line with present circumstances. For example, power system inertia is reducing generally as the penetration of converter-interfaced generation decreases intrinsic energy storage ability, which indicates that inherent tolerance capability to power disruption is decreasing [45]. Also, the developing but intermittent energy sources tend to threaten system stable operation; while power consumption and sudden system faults in either the dc or ac side of an ac/dc converter may induce undesirable power variations. These issues pose challenges for secure systems. So, achieving power support in contingencies is also required to maintain safe and stable system operation; and integrating energy storage systems (ESSs) into different systems, in short, medium and/or long terms, becomes a necessity for security and management [46].

1.2 Motivation and Objectives

The core motivation of this research is to improve the security of MMC-based systems. From the MMC control perspective, no comprehensive analysis of the internal and external coupling effects due to capacitance and inductance tolerances has been investigated. Therefore, this thesis presents a comprehensive analytical assessments of different control methods to control MMC internal dynamics, namely, the voltage and energy based controllers and their variants, with consideration of passive component tolerances. In an effort to further increase reliability of related systems, this research proposes and elaborates a T-type MMC (T-MMC) based on a dual-stage structure (HB-MMC based and FB-SM based stages), which offers salient operational benefits. Also, the T-MMC based energy storage system and its constructed dc system are investigated and presented. The proposed T-MMC may be considered a conventional MMC converter compensated with a series energy storage FACTS device that provides various ac and dc side functions and support.

The main research objectives are summarized as:

- MMC internal control schemes and the adverse effects of passive component tolerances on both the dc and ac sides are considered;
- A comprehensive assessment of the internal/external coupling effects due to the passive component tolerances within one phase-leg is presented;
- A novel modular multilevel converter topology, which affords attractive features such as ac-side voltage enlargement and dc/ac fault ride-through, is proposed;
- Reduced operational losses of the proposed converter under normal conditions, utilization of thyristors and disconnectors in the converter is presented; and
- Energy storage integration into the proposed converter is investigated. Also, the security, stability and reliability of T-MMC based dc systems can be enhanced.

1.3 Thesis Organization

This thesis is organized into six chapters.

Chapter 1 introduces the background of modular multilevel converters and their major technical characteristics. Research motivation and objectives are outlined.

Chapter 2 presents a brief review of the fundamentals of the modular multilevel converter and describes a number of control schemes used to regulate MMC internal dynamics. The mechanism that internal and external are coupling, as a result of different component tolerances between the upper and lower arms of the same phase-leg, is studied. Simulation evaluation and experimental results of the different control schemes are presented.

Chapter 3 proposes the T-MMC for reliable and flexible ac/dc conversion applications. The structure and basic characteristics of the proposed T-MMC are described, whereas the loss-reduction approaches and converter control system are presented. Simulation and experimentation confirm the effectiveness of converter performance.

Chapter 4 investigates the T-MMC based ESS and its additional features. Energy storage sizing and relevant converter control are discussed. Simulation and experimentation establish the technical feasibility and critical functions.

Chapter 5 analyses the T-MMC applications in a dc system, wherein the operation features are highlighted. Simulation results of a three-terminal dc grid with ESS integration are presented to demonstrate system performance.

Chapter 6 draws the conclusions and contributions; recommendations for future research are presented.

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Chapter 2

Modular Multilevel Converter and its Internal Control

The half-bridge modular multilevel converter (HB-MMC), which is the most common topology in the MMC family, is studied in this chapter. Topology, parameters (such as capacitance, inductance, etc.), operation principles and control schemes are presented. Specifically, this chapter comprehensively reviews and assesses of a number of existing internal controllers that manage HB-MMC horizontal/vertical dynamics and balancing, including internal and external coupling characteristics.

2.1 Typical Topologies and Operation Principles

To break through the voltage rating limits of the available semiconductors, the MMC with the utilization of series-connected submodules (SMs) was proposed [1]. The MMC serves as a VSC and can achieve ac/dc power conversion with smoother ac voltage waveforms and independent *P*-*Q* control [1]. Based on MMC schematics, various SM topologies (such as half-bridge and full-bridge) can be used to obtain different operational features, whereas MMC operation principles and key parameter design are well-established in the literature [2], [3].

As a typical MMC, the HB-MMC is widely studied and applied in bulk power conversion applications; and MMC implies HB-MMC within this chapter [1]-[3]. Fig. 2-1 shows a conventional topology, where a three-phase MMC is connected to an ac grid (v_{ac2}) via a Δ-Y interfacing transformer. The output phase voltage measured relative to ground at the ac pole of each phase is v_{io}, and V_{dc} and I_{dc} are the dc link voltage and current respectively. Each MMC arm incorporates an arm inductor L and N series-connected SMs. In general, each SM is composed of semiconductor switches and a capacitor with the nominal capacitance C_{SM}.

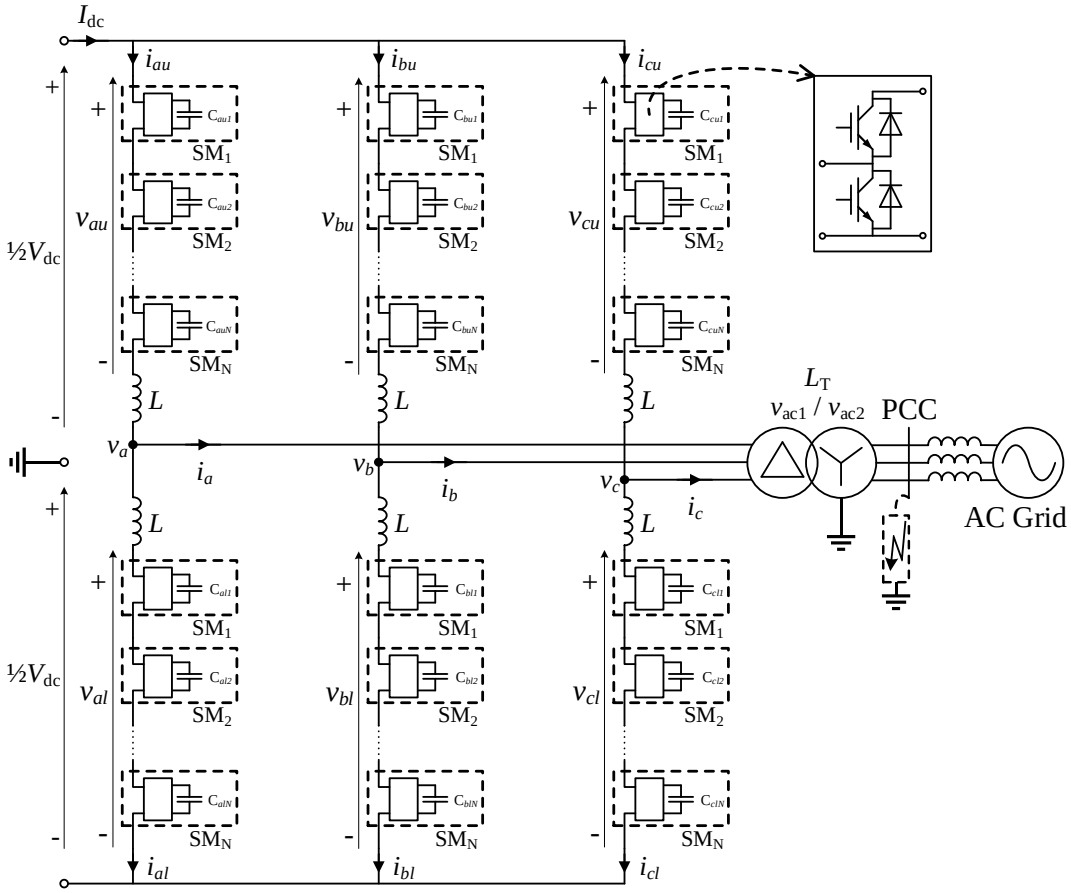


Fig. 2-1. MMC topology (with HB-SM).

With the positive direction arm currents i_{ij} (where i: a, b, c, are the three phase-legs and j: u, l, indicate the upper and lower arms respectively) and ac output current i_i as indicated in Fig. 2-1, the common and differential mode currents i_{icm} and i_{idiff} of an arbitrary phase-leg i are respectively defined as [4]:

$$i_{icm} = ½(i_{iu}+i_{il}) \tag{2.1}$$

$$i_{idiff} = i_{io} = i_{iu}-i_{il} \tag{2.2}$$

The common-mode current refers to the arm current component which is shared between the upper and lower arms of the leg, and consists of a dc component due to dc power transfer and an ac component which is predominantly 2nd order harmonics. For the i^{th} leg, V_{cijk} represents the capacitor voltage of the k^{th} SM in the j^{th} arm and V_{cij} is the sum of the SM capacitor voltages of the j^{th} arm of the i^{th} phase-leg, where k = 1-N. The voltage developed across an MMC arm v_{ij} can therefore be approximated by

the product of modulation or insertion function m_{ij} (normally $0 \leq m_{ij} \leq 1$) and its respective SM capacitor voltage sum V_{cij} [5]:

$$v_{ij}(t) = m_{ij}(t) \times V_{cij}(t) \tag{2.3}$$

With these assumptions, the differential-mode voltage and current of each phase resemble the output phase voltage v_{io} and current, that is, $v_{io}(t) = v_{idiff}(t) = v_{iu}(t)\text{-}v_{il}(t)$, which is mainly explored for ac voltage generation.

The common and differential modes of the upper and lower arm capacitor voltage sums are defined as:

$$\Sigma V_{ci} = V_{ciu} + V_{cil} \tag{2.4}$$

$$\Delta V_{ci} = V_{ciu} - V_{cil} \tag{2.5}$$

Then, the common-mode capacitor voltage sum $\sum V_{ci}$ is mostly comprised of a dc component and a small ac component that drives the circulating current in each arm, when counter harmonics are not injected into the common-mode voltage of each leg. The differential-mode capacitor voltage sum ΔV_{ci} of each leg is mainly comprised of the fundamental ac voltage, provided the upper and lower arm capacitor voltage sums have the same dc components.

Various established modulation techniques, such as pulse-width modulation (PWM) and nearest-level modulation, can be used [6]-[16]. From the voltage balancing perspective, the modulation process can either be integrated with SM-level voltage balancing or separated, leading to a new classification method. Specifically, there are two SM capacitor voltage balancing approaches, depending on the employed modulation method. The first approach calculates the number of SMs to be inserted into the conduction path and bypassed from each arm using nearest voltage level modulation [6], [7] or pulse width modulation with various carrier arrangements such as Phase-Shifted Carrier PWM (PSC-PWM) [8], [9] or phase disposition PWM (PD-PWM) [10], [11]. The SM number to be inserted and bypassed, and the sorted order of SM capacitor voltages for each arm, are fed to the SM selection algorithm. The second approach assigns the PSC-PWM and a dedicated modulating signal to each SM, with SM capacitor voltage being controlled individually by additional components injected into the main modulation signal of the arms [12]-[16]. These two

approaches may lead to different internal control schemes; therefore, integration into the control structure will be investigated later. As both balancing algorithms usually operate at high frequency, it can be reasonably assumed that the SM level voltage differences are minor, and the impact of SM capacitance differences at the SM level is mitigated by the capacitor voltage balancing. This is the basis for the following higher-level control analysis.

In general, the MMC requires a number of high and low level controllers to regulate its output ac and dc voltages, as well as active and reactive power exchanged with the ac grid. With the high modularity of the MMC circuit topology, there are many distributed passive voltage sources or energy tanks facilitating the use of low-voltage rated switching devices, for suppression of electromagnetic interference (EMI), and for providing fault-tolerant operation. The use of distributed floating capacitors in the MMC results in a converter with complex external dynamics (ac and dc side output performance) and internal dynamics (between SMs of the same arm, upper and lower arms of the same leg, and different legs); thus, a complex system requires extensive information for the controller to regulate overall operation [2]-[5]. Also, MMC capacitor voltages affect the synthesis of the common and differential mode arm voltages that create common and differential mode currents respectively [17]. Normally, the common-mode current within the MMC leg consists of dc and even harmonic currents, and its dc component helps transfer power between the dc side and the MMC arms, while the ac component (usually referred to as circulating current) increases capacitor voltage ripple and semiconductor losses.

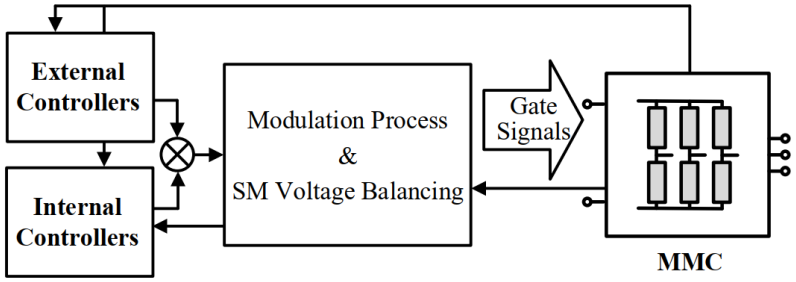


Fig. 2-2. MMC Control System Structure.

An overall control structure is shown in Fig. 2-2, where, based on sampling results, external and internal controllers operate co-ordinately and provide references for the

modulation stage. Also, the SM voltage balancing algorithm is usually aligned with the modulation process, as previously discussed. Once the MMC internal dynamics are controlled, its overall performance under normal and abnormal ac grid conditions, particularly its dynamic response due to the decoupling of SM capacitor voltage from the dc link voltage, are improved [17].

2.2 Internal Dynamics and Parameters

2.2.1 General Description

Fundamental plus higher-order harmonics which appear as capacitor voltage ripple are unavoidable due to the unique operation of the MMC. Both inner and outer arm SM-based circuits contribute to arm currents flowing through the SM capacitors, and therefore these currents cause capacitor voltage ripple which is out of phase in the upper and lower arms of each leg. The main variables that influence the internal dynamics are SM, arm and leg voltages, representing three coupled control hierarchies within the MMC that could be exploited to enhance its performance independent of operating conditions. Detailed analysis of different internal control schemes will be discussed later.

Most research generally assumes symmetrical MMC element values such as SM capacitance and arm inductance. This practice is reasonable and acceptable in most cases [18]-[20]. However, component tolerances exist. The impact of unequal arm inductances on MMC performance is investigated in [21], where, importantly, the use of additional controllers (proportional resonant based) is recommended to prevent a dc component developing in the ac side output and to suppress fundamental oscillation in the dc link. Although the negative effects of SM capacitor voltage difference can be eliminated by voltage balancing algorithms at the SM level, the differences in SM capacitances due to tolerances cannot be handled adequately by the inner-arm balancing within each arm. That is, as the ac output controller selects different SMs during operation with a fixed number of inserted and bypassed SMs, capacitance asymmetry may appear as variable capacitance in each phase-leg (upper plus lower arms), rather than fixed capacitance C_{SM}/N. The same rule can also be applied to the arm inductors. Thus, when it comes to the practical design, it is necessary to account for the passive component tolerances for the following reasons:

- Each SM must be regulated correctly to ensure that the voltage stresses on each SM capacitor and switching devices do not exceed their rated voltage;
- Although the majority of publications assume identical SM capacitance, the inherent SM capacitance tolerances have noticeable adverse impact in terms of stored energy variation;
- Given the SM capacitors and arm inductors play fundamental roles in the synthesis of the ac and dc output voltages and power transfer between the ac and dc sides, differences in their values may lead to unbalanced fundamental arm currents, which could affect the common-mode and dc link currents, as will be elaborated later; and
- The assumption of identical SM capacitance leads to performance deterioration of some control methods when hardware implemented, which appears as voltage imbalance between the arms of the same or different legs, etc.

Accurate theoretical quantification of the impact of SM capacitance tolerance on MMC performance is difficult as it involves a large number of components with highly complex dynamics that operate as part of a variable structure system, with structure variability influenced by several controllers. The study of the potential impact of the capacitance tolerance is divided into three parts:

- Capacitance tolerance impacts on the pattern and rate of the capacitor voltage variation at the SM level within each arm (this effect is expected to be mitigated by SM level capacitor voltage balancing);
- Vertical asymmetry (the upper and lower arms of the same phase-legs present different total capacitances) may lead to unequal voltage or energy distribution between the upper and lower arms; and
- Horizontal asymmetry (the phase-legs reflect different equivalent capacitances) may cause unequal energy distribution and excessive circulating currents between legs.

Thus, regulation of MMC inner dynamics requires horizontal balancing (leg *a*, *b* and *c*) and vertical balancing (upper and lower arms of the same leg, *iu* and *il*).

For the horizontal balancing, a satisfactory case is that the common-mode capacitor voltage sum of the three legs is controlled to be the same and constant. Such control ensures satisfactory operation over the full range and with fast dynamic response at both the ac and dc sides. This is because of the reduced coupling between the principal ac and dc variables involved in the power transfer and synthesis of the output voltages and currents.

Concerning vertical balancing, unbalanced voltage between the upper and lower arms of the same leg appears not to cause dc offset or even harmonics in the ac output voltage. But this observation is true only when the MMC operates at relatively low modulation indices (where it does not need to insert or bypass all the SMs in its arms to satisfy output voltage requirements) [7]-[11]. Failure to nullify the errors between the mean value of upper and lower arm capacitor voltage sums (basically differential capacitor voltage sum) may introduce dc offsets into the ac output voltages and currents when MMC operation requires all SMs. However, the potential problems of dc offsets and even harmonics in the output waveforms can be avoided by using redundant SMs in each MMC arm or by regulating the capacitor voltage sum of each arm to be higher than the actual dc link voltage (thus, appearing to have redundant SMs). As stated, when the upper and lower arms of the same phase-leg have different capacitances, uncontrolled fundamental current appears in the common-mode current of each phase-leg, and also in the dc link current. This problem could be typically avoided, however, if the dc components of the differential-mode capacitor voltage sums of the upper and lower arms of all three phase-legs are nullified (or forced to zero).

2.2.2 Effects of Arm Capacitance Asymmetry

To show the basic internal and external coupling effects due to arm capacitance asymmetry, the MATLAB/Simulink based model as shown in Fig. 2-1 is used to clarify issues due to the potential mismatch of MMC capacitance. This following illustrates basic behaviour with and without capacitance tolerances in leg B, assuming inverter mode operation, with MMC parameters in Table 2-1 feeding a passive load.

Table 2-1. Simulation parameters of the 40MVA MMC.

Rated power	40MVA
DC voltage	40kV
AC grid line voltage	33kV
AC grid frequency	50Hz
Transformer leakage inductance	0.18pu
Transformer ratio	20/33kV
Arm inductance	6.1mH(0.2pu)
Numbers of SMs per arm	20
SM capacitance	6.7mF(40kJ/MVA)
Modulation carrier frequency	1.0kHz

Fig. 2-3 show simulation waveforms of the output ac voltages, dc link current, common-mode currents, and differential-mode capacitor voltage sums, when 0 and ±10% tolerances are applied to SM capacitances of the arms in leg B, and without active vertical control (no inter-arm control). The plots in Fig. 2-3-I show that the mean differential-mode capacitor voltage sums of the three legs are near zero with zero SM capacitance tolerance. Fig. 2-3-I and II (a) show the same stiff ac grid voltage, and the dc link current and common-mode currents do not exhibit any low frequency oscillation. However, when ±10% SM capacitance tolerance is incorporated, Fig. 2-3-II shows the common-mode currents contain noticeable unbalanced ac components (more than 100A in amplitude, approximately), with significant 50Hz components in both the common-mode and dc link currents [cf Fig. 2-3-II(b) and (c)]. Also, the pre-filtered and post-filtered differential-mode capacitor voltage sums become unbalanced and deviate from zero, respectively [cf Fig. 2-3-II(d) and (e)]. Thus, it can be concluded that the simulated waveforms in Fig. 2-3 verify the previous mathematical analysis.

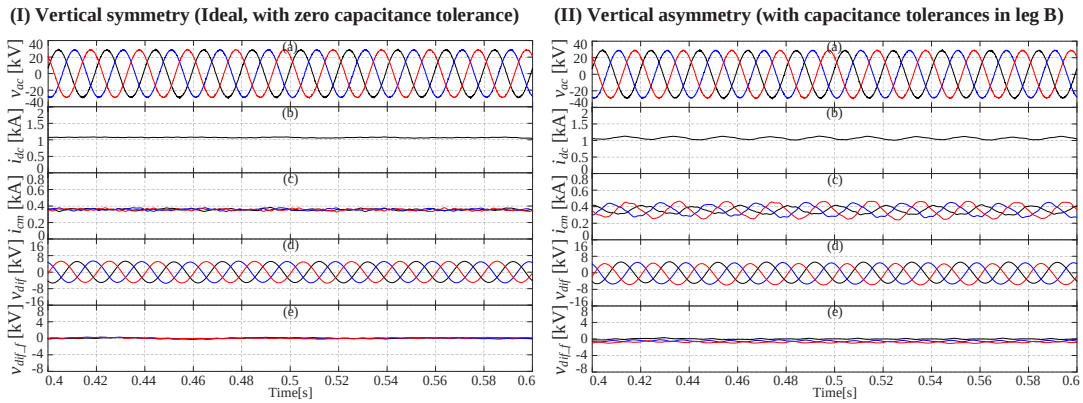


Fig. 2-3. MMC waveforms in vertically symmetric and asymmetric cases: (a) ac output voltage v_{ac}, (b) dc link current i_{dc}, (c) common-mode current i_{cm}, (d) differential-mode capacitor voltage sum v_{diff}, and (e) 50Hz-notch filtered differential-mode capacitor voltage sum v_{diff_f}.

From the internal dynamics perspective, many control strategies have been developed to suppress the circulating current and capacitor voltage ripple, and these strategies broadly exploit injection of appropriate harmonics into the common-mode voltage or arm currents.

To illustrate the potential effects of internal dynamics on the ac output, three sets of simulation cases are presented, namely, without vertical balancing, and with voltage and energy based vertical balancing methods, where the dc link voltage remains 40kV, modulation index is fixed at 95%, and two set points common-mode capacitor voltage sums, namely, 80kV (V_c = 1pu) and 88kV (V_c = 1.1pu). Fig. 2-4 summarizes the normalized arm voltages of leg B and their corresponding upper and lower arm capacitor voltage sums, with vertical SM capacitance asymmetry of ±10%.

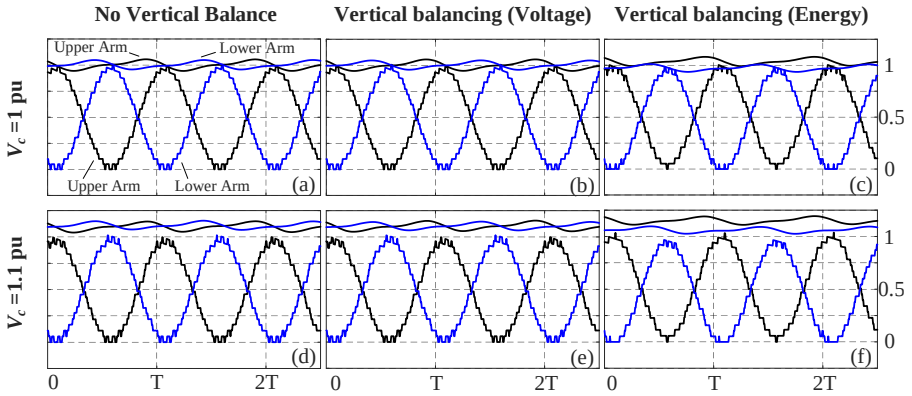


Fig. 2-4. Normalized arm terminal voltages and common-mode capacitor voltages of methods in asymmetric case.

Fig. 2-4(a) and (d), and (b) and (e) show that without vertical balancing and with voltage-based vertical balancing the drift of the differential-mode capacitor voltage sums from zero remain small for both set points of the common-mode capacitor voltage sums of 1pu and 1.1pu; thus both arms are able to synthesize the correct arm voltages. In contrast, Fig. 2-4(c) and (f) show that with the energy-based vertical balancing the drift of the differential-mode capacitor voltage sums from zero becomes large as the set point of the common-mode capacitor voltage sums increases from 1pu to 1.1pu; thus making the arm with lower voltage unable to synthesize the correct arm voltages. This problem would be exacerbated if the MMC operates at higher modulation indices that approach unity for SPWM and 1.155 with SPWM plus 3rd harmonics. Fig. 2-4(f) shows even though the modulation index or upper and lower voltages do not hit the limits, the dc components of the capacitor voltage sums of the upper and lower arms become unequal, and this may cause dc-offset in the output ac voltages if not mitigated.

2.2.3 Analysis of Arm Capacitance Asymmetry Impacts

To substantiate the observed phenomenon mathematically, approximate analysis is used to explain the influence of asymmetric arm capacitance, assuming:

- Modulation signals are continuous and harmonic free;
- Switching frequency is sufficiently high, so the output and arm currents and voltages can be assumed constant within each switching period;
- The capacitance tolerances between the SMs of each arm are taken into account, but for simplicity these tolerances are reflected to the mean or equivalent capacitance of each arm;
- The SM capacitor voltages within one arm are balanced; and
- Common-mode capacitor voltage sum (SM average) controllers are effective among three legs.

Taking phase-leg *i* as an example, the upper and lower arm currents are:

$$i_{iu}(t) = \tfrac{1}{2} i_i(t) + i_{icm}(t) = \tfrac{\sqrt{2}}{2} I_i \sin(\omega t + \varphi_i) + I_{icm} \tag{2.6}$$

$$i_{il}(t) = -\tfrac{1}{2} i_i(t) + i_{icm}(t) = -\tfrac{\sqrt{2}}{2} I_i \sin(\omega t + \varphi_i) + I_{icm} \tag{2.7}$$

where I_i and φ_i are the rms and phase angle of fundamental output current respectively, and i_{icm} only consists of dc component I_{icm}. For simplicity, the MMC inherent second and higher even order harmonic circulating currents are suppressed.

Independent of the modulation method, the switching functions that describe or define the number of SMs to be inserted from the arms of each leg can be approximated by the followings average and normalized insertion functions:

$$S_{iu}(t) = \tfrac{1}{2} - \tfrac{1}{2} M_i \sin(\omega t + \varphi_s) + M_{icm} \tag{2.8}$$

$$S_{il}(t) = \tfrac{1}{2} + \tfrac{1}{2} M_i \sin(\omega t + \varphi_s) + M_{icm} \tag{2.9}$$

where M_i and φ_s are the amplitude and phase angle of the modulation index respectively, M_{icm} is the output of common-mode controller, $0 \le M_i \le 1$ and $0 \le M_{icm} \le 1$.

The upper and lower SM average capacitor currents can be approximated as:

$$\begin{aligned} i_{cu}(t) = {} & I_{icm}(\tfrac{1}{2} + M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) \\ & - \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) + \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_i) \\ & + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) \end{aligned} \tag{2.10}$$

$$\begin{aligned} i_{cl}(t) = {} & I_{icm}(\tfrac{1}{2} + M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) \\ & + \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) - \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2} + M_{icm}) \sin(\omega t + \varphi_i) \\ & + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) \end{aligned} \tag{2.11}$$

where dc components control the mean SM voltages and fundamental and second-order harmonics constitute SM voltage ripple. By integrating the average capacitor currents in (2.10) and (2.11), the upper and lower arm capacitor voltage sums are:

$$\begin{aligned} v_{cu}(t) &= v_{cu}{}^{0} + \frac{1}{C_u} \int i_{cu}{}^{\omega, 2\omega} dt \\ &= V_{cu} + A_u \cos(\omega t + \varphi_s) - B_u \cos(\omega t + \varphi_i) + D_u \sin(2\omega t + \varphi_s + \varphi_i) \end{aligned} \tag{2.12}$$

$$\begin{aligned} v_{cl}(t) &= v_{cl}{}^{0} + \frac{1}{C_l} \int i_{cl}{}^{\omega, 2\omega} dt \\ &= V_{cl} - A_l \cos(\omega t + \varphi_s) + B_l \cos(\omega t + \varphi_i) + D_l \sin(2\omega t + \varphi_s + \varphi_i) \end{aligned} \tag{2.13}$$

where $A_u = \frac{I_{icm}M_i}{2\omega C_u}$, $B_u = \frac{\sqrt{2}I_i}{2\omega C_u}(\frac{1}{2} + M_{icm})$, $D_u = \frac{\sqrt{2}I_iM_i}{16\omega C_u}$, $A_l = \frac{I_{icm}M_i}{2\omega C_l}$, $B_l = \frac{\sqrt{2}I_i}{2\omega C_l}(\frac{1}{2} + M_{icm})$, $D_l = \frac{\sqrt{2}I_iM_i}{16\omega C_l}$, and C_u and C_l represent the equivalent capacitances of the upper and lower arms respectively. DC components of capacitor voltages v_{cu}^0 and v_{cl}^0 represent the settling points for the upper and lower arm capacitor voltage sums. Switching action then reflects SM voltage back to the ac terminals and the common-mode voltage of each phase-leg is described by:

$$v_{icm}(t) = v_{iu}(t) + v_{il}(t) = NS_{iu}(t)v_{cu}(t) + NS_{il}(t)v_{cl}(t) \tag{2.14}$$

where S_{iu} and S_{il} remain unchanged as (2.8) and (2.9) because no new component is added into the switching functions. Similarly, as the dc component of the mean common-mode capacitor voltage sum is controlled to $2N \times V_c$*, only ac components are considered.

Based on (2.8), (2.9), (2.12), (2.13) and (2.14), the ac components (frequency at ω, 2ω and 3ω) of the leg common-mode voltages are:

$$\begin{aligned} v_{icm}(t)^{(\omega)} &= v_{iu}(t)^{(\omega)} + v_{il}(t)^{(\omega)} \\ &= N(\tfrac{1}{2} + M_{icm})(A_u - A_l)\cos(\omega t + \varphi_s) \\ &\quad - N\left[(\tfrac{1}{2} + M_{icm})(B_u - B_l) + \tfrac{1}{4}M_i(D_u - D_l)\right]\cos(\omega t + \varphi_i) \\ &\quad - \tfrac{1}{2}M_i(V_{cu} - V_{cl})\sin(\omega t + \varphi_s) \end{aligned} \tag{2.15}$$

$$\begin{aligned} v_{icm}(t)^{(2\omega)} &= v_{iu}(t)^{(2\omega)} + v_{il}(t)^{(2\omega)} \\ &= -N\tfrac{1}{4}M_i(A_u + A_l)\sin(2\omega t + 2\varphi_s) \\ &\quad + N\left[\tfrac{1}{4}M_i(B_u + B_l) + (\tfrac{1}{2} + M_{icm})(D_u + D_l)\right]\sin(2\omega t + \varphi_s + \varphi_i) \end{aligned} \tag{2.16}$$

$$v_{icm}(t)^{(3\omega)} = v_{iu}(t)^{(3\omega)} + v_{il}(t)^{(3\omega)} = \tfrac{1}{4}NM_i(D_u - D_l)\cos(3\omega t + 2\varphi_s + \varphi_i) \tag{2.17}$$

where the voltage ripple at ω, 2ω, and 3ω generates corresponding common-mode ac currents. Equation (2.15) indicates that unequal capacitances of the upper and lower arms of the same leg can lead to the appearance of fundamental voltage in the common-mode capacitor voltage sum which would drive fundamental current in the common-mode loop of each phase-leg. Equation (2.16) represents the component of the common-mode voltage that would drive 2nd order harmonic current in each phase-leg, which will be eliminated. Any resistance in the common-mode circuit loop is neglected for simplicity, thus only total inductance of the common-mode loop is considered. The

amplitude of the 3ω components is small compared to that at ω, so the common-mode current (due to the fundamental voltage ripple) is:

$$\begin{aligned} i_{icm}(t)^{(\omega)} &= \frac{1}{L_u + L_l}\int v_{icm}(t)^{(\omega)}dt = K_1 \sin(\omega t + \varphi_s) - K_2 \sin(\omega t + \varphi_i) + K_3 \cos(\omega t + \varphi_s) \\ &= \sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 - 2K_2\sqrt{K_1{}^2 + K_3{}^2}\cos(2\varphi_s - \varphi_k)} \\ &\times \sin\left[\omega t + \arctan\left(\frac{\sqrt{K_1{}^2 + K_3{}^2}\sin(\varphi_s + \varphi_k) - K_2 \sin\varphi_s}{\sqrt{K_1{}^2 + K_3{}^2}\cos(\varphi_s + \varphi_k) - K_2\cos\varphi_s}\right)\right] \end{aligned} \tag{2.18}$$

where L_u and L_l are the upper and lower arm inductances respectively, and $\varphi_k = \arctan\left(\frac{K_3}{K_1}\right)$, $K_1 = N\frac{(\frac{1}{2} + M_{icm})(A_u - A_l)}{\omega(L_u + L_l)}$, $K_2 = N\frac{(\frac{1}{2} + M_{icm})(B_u - B_l) + \frac{1}{4}M_i(D_u - D_l)}{\omega(L_u + L_l)}$, and $K_3 = \frac{M_i(V_{cu} - V_{cl})}{2\omega(L_u + L_l)}$.

The amplitude range of the fundamental common-mode current has a range:

$$\begin{aligned} &\sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 - 2K_2\sqrt{K_1{}^2 + K_3{}^2}} \\ \le &\sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 - 2K_2\sqrt{K_1{}^2 + K_3{}^2}\cos(2\varphi_s - \varphi_k)} \le \\ &\sqrt{K_1{}^2 + K_2{}^2 + K_3{}^2 + 2K_2\sqrt{K_1{}^2 + K_3{}^2}} \end{aligned} \tag{2.19}$$

Considering the range of modulation indices M_i and M_{icm}, and the definitions of K_1, K_2 and K_3 above, $C_u \neq C_l$ the fundamental frequency current in (2.18) has a non-zero amplitude and exists in the common-mode current. Also, the fundamental arm currents interact with switching functions, resulting in dc and 2ω voltage deviation of the upper and lower arms. The following mathematical derivation establishes the generation mechanism of the dc and 2ω components in the common-mode current. Additional fundamental current is added into the ideal arm currents in (2.6) and (2.7):

$$\begin{aligned} i_{iu}{}'(t) &= \tfrac{1}{2}i_i(t) + i_{icm}(t) \\ &= \tfrac{\sqrt{2}}{2}I_i \sin(\omega t + \varphi_i) + I_{icm} + \sqrt{2}I_{icm\omega}\sin(\omega t + \varphi_{icm\omega}) \end{aligned} \tag{2.20}$$

$$\begin{aligned} i_{il}{}'(t) &= -\tfrac{1}{2}i_i(t) + i_{icm}(t) \\ &= -\tfrac{\sqrt{2}}{2}I_i \sin(\omega t + \varphi_i) + I_{icm} + \sqrt{2}I_{icm\omega}\sin(\omega t + \varphi_{icm\omega}) \end{aligned} \tag{2.21}$$

where $I_{icm\omega}$ and $\varphi_{icm\omega}$ are the rms and phase angle of the fundamental common-mode current respectively. If no active controller is designed for the fundamental oscillation, the switching functions remain as (2.8) and (2.9). The SM mean capacitor currents are:

$$\begin{aligned} i_{cu}{}'(t) = {} & I_{icm}(\tfrac{1}{2}+M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) - \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(\varphi_s - \varphi_{icm\omega}) \\ & - \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) + \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2}+M_{icm}) \sin(\omega t + \varphi_i) \\ & + \sqrt{2} I_{icm\omega} (\tfrac{1}{2}+M_{icm}) \sin(\omega t + \varphi_{icm\omega}) \\ & + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) + \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(2\omega t + \varphi_s + \varphi_{icm\omega}) \end{aligned} \tag{2.22}$$

$$\begin{aligned} i_{cl}{}'(t) = {} & I_{icm}(\tfrac{1}{2}+M_{icm}) - \tfrac{\sqrt{2}}{8} I_i M_i \cos(\varphi_s - \varphi_i) + \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(\varphi_s - \varphi_{icm\omega}) \\ & + \tfrac{1}{2} I_{icm} M_i \sin(\omega t + \varphi_s) - \tfrac{\sqrt{2}}{2} I_i (\tfrac{1}{2}+M_{icm}) \sin(\omega t + \varphi_i) \\ & + \sqrt{2} I_{icm\omega} (\tfrac{1}{2}+M_{icm}) \sin(\omega t + \varphi_{icm\omega}) \\ & + \tfrac{\sqrt{2}}{8} I_i M_i \cos(2\omega t + \varphi_s + \varphi_i) - \tfrac{\sqrt{2}}{4} I_{icm\omega} M_i \cos(2\omega t + \varphi_s + \varphi_{icm\omega}) \end{aligned} \tag{2.23}$$

where the dc and 2ω ac components in (2.22) each contain a term related to the amplitude of fundamental frequency common-mode current $\sqrt{2}\, I_{icm\omega}$ which has the opposite sign to the corresponding term in (2.23). Charging and discharging SMs with the currents in (2.22) and (2.23) causes dc, ω and 2ω differences between the upper and lower arms. Also, both dc and 2ω frequency voltage differences are introduced by the non-zero fundamental frequency common-mode current.

Accordingly, for one MMC leg, capacitance asymmetry leads to odd harmonic components in common-mode current (mainly a fundamental frequency component), and its amplitude, depending on various variables, increases proportionally with the capacitance difference. For MMC operation, asymmetric capacitance in one leg results in two major effects:

- As the asymmetry is random among the legs, the amplitude and phase angle of the fundamental common-mode currents of the three legs would be unbalanced, causing unbalanced fundamental current to feed into the dc link current; and
- Such additional fundamental arm currents may interact with switching functions, resulting in dc and 2ω voltage deviation of the upper and lower arms.

Furthermore, the voltage differences contribute to the common-mode loop current ripple through the coefficient K_3 in (2.19), leading to MMC inner-leg interaction. Also, this analysis initially assumed the output of the common-mode capacitor voltage sum controller to be a pure dc component to maintain the constant SM average dc voltage. However, the fundamental fluctuations will induce small corresponding components into the PI controllers, depending on bandwidth and phase-shift characteristics. Therefore, both dc and ω frequency voltage deviation continues until reaching equilibrium in terms of phase angle and magnitude change. The mathematically analysis assumed an ideal MMC dc power supply. Long distance cables introduce parasitic parameters and as a result, the fundamental oscillation in one leg influences other legs through the weak dc terminal voltage, actuating fundamental oscillations and arm voltage differences. This phenomenon could be considered as power circulating among three legs to compensate for the stored energy of different arms, which is an inter-leg interaction. Based on the previous discussion on such a complicated system, an accurate calculation of the amplitude of the fundamental frequency dc link current ripple caused by passive component tolerances is tedious, with much uncertainty that cannot be accounted for readily, such as collective action of various internal controllers. Therefore, the presented analysis is an attempt to explain the mechanism of the inducement of fundamental current ripple and its potential causes, rather than a precise quantification of its magnitude. Fortunately, there are various internal control schemes that are able to (or intend to) suppress such ripple, facilitating MMC internal and external decoupling.

For unbalanced grid analysis, most approaches in the literature focus on eliminating the 2ω power component, which causes the dc voltage and/or dc current oscillation [22]. However, unlike the 2ω components only occurring during output unbalanced conditions, oscillation at ω always exists due to MMC charging and discharging with unequal arm capacitances in the same leg. Similarly, the tolerances of arm inductance within one leg can cause the same current oscillation as the energy stored in the arm inductors and the ac voltage drops they present are no longer balanced. Therefore, additional controllers are needed to regulate the inherent fundamental current difference between arms and energy differences caused by passive component tolerances. This discussion shows that a vertical balancing controller that minimizes

the differential-mode capacitor voltage sum is effective for correct MMC operation when passive components tolerances are significant. Also, in the asymmetry case, the incorporation of a dedicated controller to directly eliminate the fundamental current from the common-mode current of each leg, may aid suppression of fundamental frequency oscillation of the dc link current, but cannot eliminate the differential-mode capacitor voltage sum.

2.3 Internal Control Schemes

In light of the mentioned observations, proper designed MMC internal controllers are necessary parts for desirable operation. This section reviews the internal control schemes proposed and studied in the literature, especially arm and leg level balancing schemes. As stated, the adopted control scheme should function for both internally balancing and internal-external decoupling.

As the fundamental condition, voltage control of each SM capacitor is essential for ensuring switching device safety and good performance of higher hierarchies. Different methods for managing voltage differences amongst SMs of the same arm caused by different charging/discharging times and non-ideal parameters are discussed in the literature, including SM voltage control algorithms based on either centralized or individual schemes [23]-[28].

Many focus on control of higher hierarchies such as arm and leg capacitor voltages, and arm and leg energy (power integral), considering both normal and abnormal cases. The importance of controlling MMC arm voltage was first recognized in [29] where internal voltage regulation was implemented based on an individual SM voltage balancing method with Phase-Shifted Carrier Pulse Width Modulation (PSC-PWM). The individual SM balancing method was improved in [30]-[37] by direct control of the MMC arm voltages, which is realized through manipulation of the active power of the upper and lower arms of each phase-leg in order to estimate the appropriate fundamental current to be injected into the common-mode current of each leg. Early studies identified the importance of controlling the MMC internal stored capacitive energy for safe and proper operation [38], [39]. Subsequently, a comprehensive study of MMC capacitive energy variation during asymmetric ac faults was presented, considering three control objectives (suppression of negative currents to zero, balanced

active power or balanced reactive power) [40]. The study concluded that the control objective which eliminates reactive power oscillation offers clear advantage over maintaining balanced output phase current or oscillation free active power, particularly, in terms of capacitor energy and voltage ripple for reactive power loadings, ranging from unity to zero power factor. In [41]-[47], methods of balancing the arm voltage (or energy) using the concept of equivalent arm capacitance was proposed, and was assessed considering a single-phase to ground fault with a number of control objectives. However, some claims, regarding the relationship between the ability to suppress circulating currents and injection of negative sequence current into the ac grid, need additional considerations in more cases. But generally, the methods discussed in [41]-[47] show satisfactory MMC operation during normal and abnormal conditions.

From the modulation and SM voltage balancing point of view, the control methods are divided into two broad categories. Methods that use dedicated SM controllers to regulate individual SM capacitor voltage without employing capacitor voltage sorting, are classified as Method-I (with such methods, capacitor voltage balancing and modulation represent two successive stages or layers). Whereas methods that insert or bypass SMs based on the combined outcomes of modulation and a capacitor voltage sorting algorithm, are classified as methods II to IV (in these cases, capacitor voltage balancing and the modulation process are inseparable).

Fig. 2-5 and Fig. 2-6 depict generic control structures for the methods I and II respectively, with both employing a output controller for regulating the output ac currents and active and reactive power (or dc voltage) [41]-[43]. Usually, both methods employ a positive and negative separation stage (based on phase-lock loop) that decomposes the three-phase voltages and currents into positive and negative sequence components to be used by the inner current controller to compute the modulating signals [45]-[47].

Because the common-mode arm voltage or common-mode capacitor voltage sum only influences the common-mode current in each leg, its exploitation to regulate arm or leg voltage or energy will not affect the differential ac output current or voltage of the MMC, provided any modification is applied to both the upper and lower arm voltage

commands and the modulation functions remain within the linear range (no saturation). All the methods investigated include a dedicated controller for MMC internal dynamics regulation, and a proportional-resonant controller tuned at 2ω for circulating current suppression in each leg. To minimize the adverse impact of cross-modulation due to undesirable SM capacitor voltage dynamics on the output voltage and current waveforms, a dedicated PI controller is used on each leg to regulate the common-mode capacitor voltage sum independent of the dc link voltage. Thus SM capacitor voltage dynamics and regulation are decoupled from the dc link voltage. From observation of the active power of the upper and lower arms and literature review, injection of a small fundamental current into the common-mode current of each leg improves vertical balance, specifically, equalizing SM capacitor voltages or energy sum of the upper and lower arms of the same leg.

2.3.1 Method-I: Voltage Control Based on Individual SM Voltage Balancing

This method does not employ a sorting-based SM capacitor voltage balancing algorithm in the inner layer as originally envisioned by Marquardt. Rather it uses a simple proportional controller at each SM level to regulate the capacitor voltage in an isolated manner. The SM capacitor voltage controller estimates the adjustment to be introduced to the main modulation signal of each arm in order to synthesize the modulating signal to be compared with the dedicated PSC of each SM. A depiction of Method-I in Fig. 2-5 shows that the main modulation signal of the arm or leg is modified by an amount that represents the output of the capacitor voltage controller multiplied by the polarity of the arm current ($Kb_{ijk} \times (V_{cijk}^{*} - V_{cijk}) \times \text{sign}(i_{ij})$, where Kb_{ijk} represents the proportional gain of the SM capacitor voltage controller). The main attribute of this method over a sorting-based method is that the average switching frequency of the SM switches is constant and equal to the assigned carrier frequency, independent of modulation depth. Therefore, this method ensures even thermal distribution, whence simpler heat management system design.

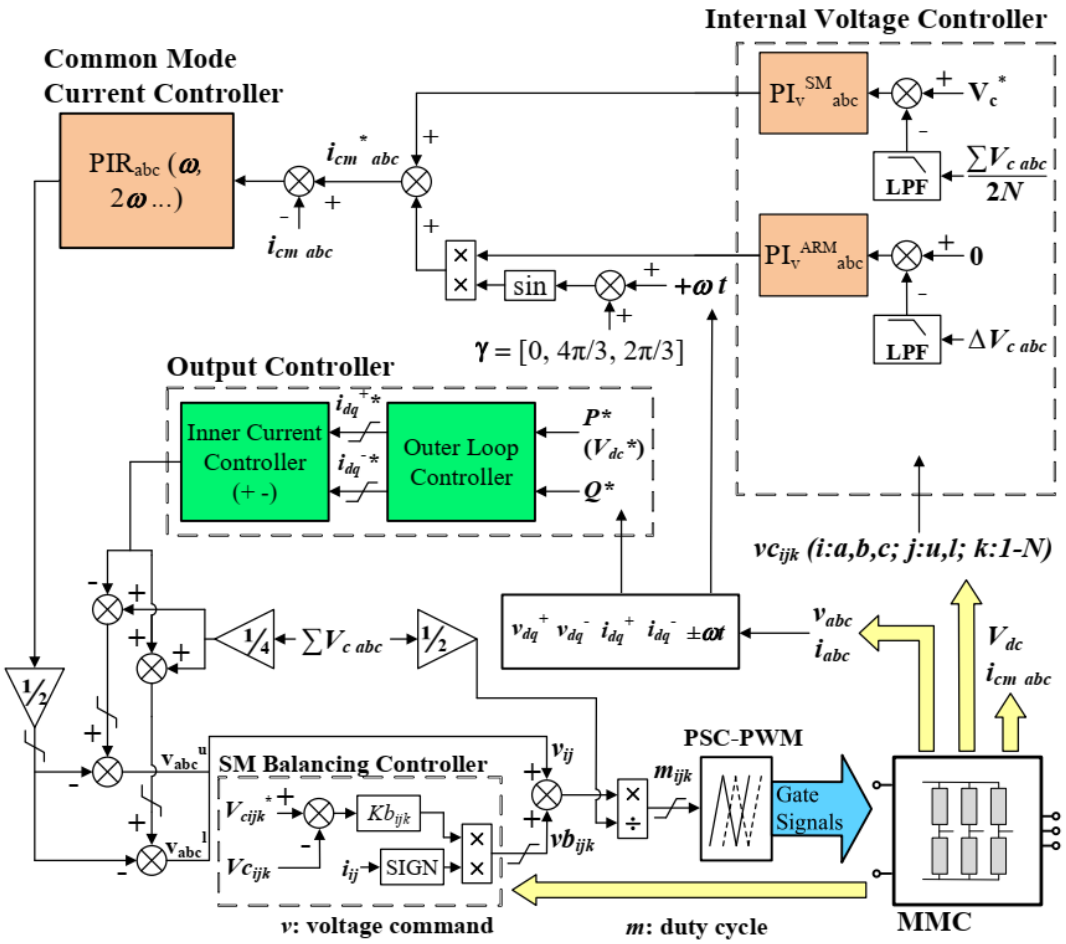


Fig. 2-5. Schematic diagram of Method-I.

Two ways to implement Method-I have emerged, and the main difference is the choice of reference V_{cijk}* used by each SM capacitor voltage controller that ensures capacitor voltage balancing. The first implementation sets the reference voltage for each SM capacitor constant (dc) or equal to the average of the common-mode capacitor voltage sum per leg, excluding the ripple (V_{cijk}* = ½$\sum V_{ci}/N$) [48]-[51]. The initial premise of this implementation is that, if the common-mode capacitor voltage sum is tightly controlled and the individual SM capacitor voltages in the entire leg are also controlled to balance, the upper and lower arm capacitor voltage sums of the same leg will be the same, which means vertical balancing is eventually achieved. Low pass filters are needed to prevent introducing SM voltage ripple into the control loops. A more common implementation uses the SM arithmetical average voltage of each arm as a reference, balancing SM voltage within one arm, which shows good dynamic response and has low parameter sensitivity [23], [30]-[34].

For management of internal arm-level dynamics, Method-I in Fig. 2-5 uses both average SM capacitor voltage control and arm voltage balancing control. The average SM voltage controller ensures the SM average capacitor voltage of each leg is controlled and independent of the dc link voltage. This is achieved through manipulation of the common-mode current of each leg, whilst the arm voltage balancing controller aims to eliminate any error between the dc components of the capacitor voltage sum of the upper and lower arms of the same leg. This is facilitated by manipulation of the active-power difference between the upper and lower arms of the same leg, through injection of a small fundamental current into the common-mode current which is predominantly dc with a remnant of the circulating current [30]-[36], [51]. As shown in Fig. 2-5, SM voltage and arm balancing controllers PI_v^{SM} and PI_v^{ARM} control the common and differential mode capacitor voltage sums respectively, with the ac components of the measured capacitor voltages low-pass filtered (LPFs in Fig. 2-5). In previous studies, both common and differential mode controllers use only proportional terms, benefiting from the MMC natural ability to balance its arm capacitor voltages. Hence the integral terms only accelerate convergence toward the desired settling points with zero steady-state error.

Accordingly, common and differential mode mean capacitor voltage sum control are achieved, therefore, horizontal and vertical balance are ensured with decoupled capacitor voltages. As a well-designed SM balancing scheme can isolate SM-level manipulation and higher-level control, the direct higher level voltage control scheme can naturally be applied to the sorting algorithm, as to be discussed.

2.3.2 Method-II: Voltage Control Based on Sorting Algorithm

The conventional MMC control system has a similar structure to that of the two-level converter with minor controller modifications to account for circulating currents. This approach is known for its simplicity and stability, but its main drawback is that the SM capacitor voltages are directly coupled to (or track) the MMC dc link voltage. This means any change in active power set-point necessitates dc link voltage change of the power controlling converter. The SM capacitor voltages and their corresponding energy levels are also changed. As a result, such a controlled MMC tends to suffer from slow dynamic response and is subject to strict and slow power ramp rates.

Therefore, Method-II with an additional control stage to manage the MMC internal dynamics and decouple the common-mode SM capacitor voltage sum from the dc link voltage in order to improve dynamic response, was proposed. As shown in Fig. 2-6, Method-II adopts similar common and differential mode capacitor voltage sum controllers, PI_v^{Σ} and PI_v^{Δ}, respectively, as proposed by Akagi *et al*. [32], implemented with Method-I to regulate MMC internal dynamics.

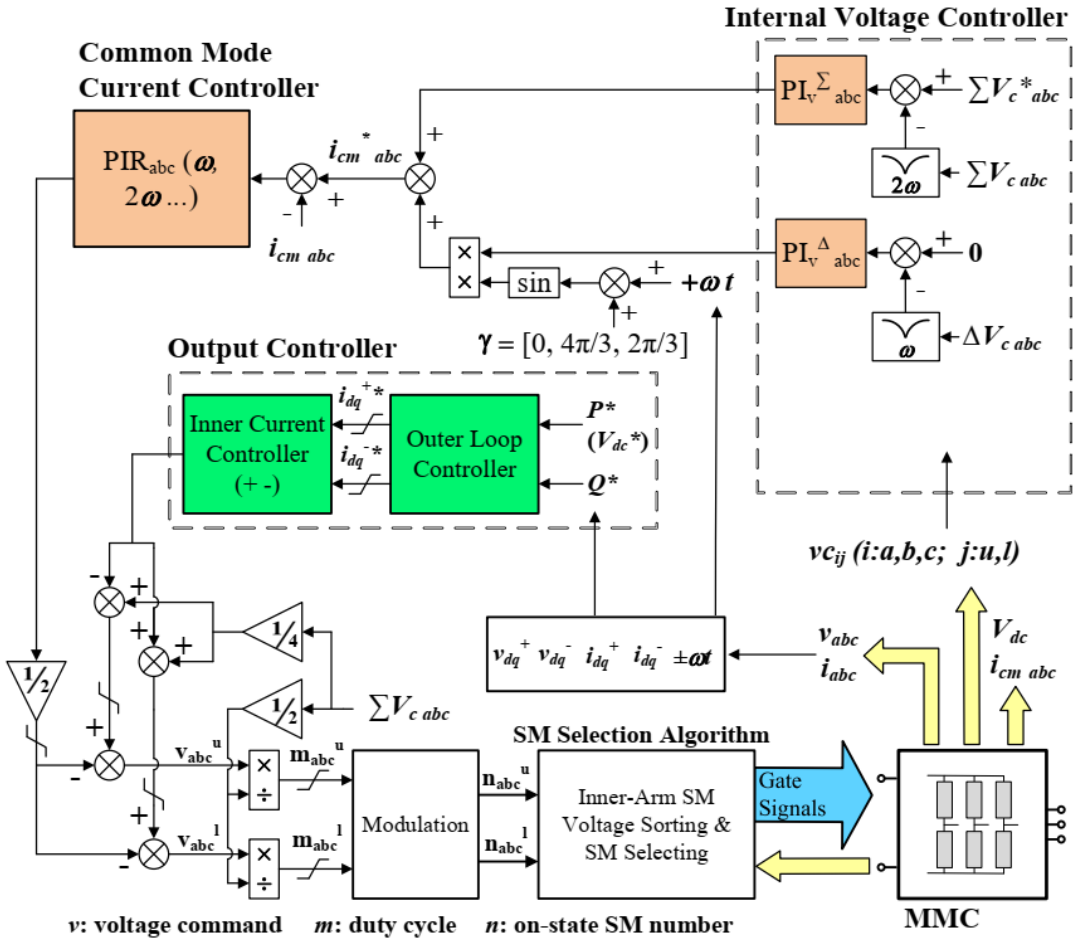


Fig. 2-6. Schematic diagram of Method-II.

The MMC leg common and differential mode capacitor voltage sums contain ac components, predominantly 2nd and 1st harmonics respectively; therefore, a number of notch filters tuned at 2ω and ω suppress these ac components in Fig. 2-6.

2.3.3 Method-III: Conventional Energy Control

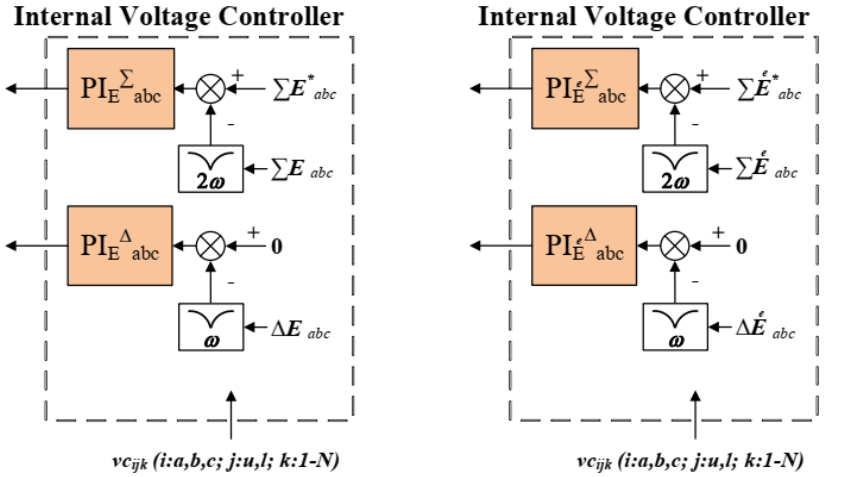
MMC internal dynamics regulation using energy-based controllers, as shown in Fig. 2-7(a), is referred to as Method-III in this chapter. The control structure is similar to

Method-II, but it regulates the dc components of the common and differential mode energy of the upper and lower arms of each leg to be constant and zero respectively [41], [45], [47]. The common and differential mode capacitor energy sums of each leg are:

$$\Sigma E_i = \frac{1}{2}\left(\sum_{k=1}^{N} C_{iuk} \times {V_{ciuk}}^2 + \sum_{k=1}^{N} C_{ilk} \times {V_{cilk}}^2\right) \tag{2.24}$$

$$\Delta E_i = \frac{1}{2}\left(\sum_{k=1}^{N} C_{iuk} \times {V_{ciuk}}^2 - \sum_{k=1}^{N} C_{ilk} \times {V_{cilk}}^2\right) \tag{2.25}$$

where the capacitance and voltage of each SM are incorporated into the calculation. Studies have shown that the common and differential mode capacitor energy sums of each leg oscillate or contain the same dominant frequencies as in the common and differential mode capacitor voltage sums respectively, that is, 2ω and ω, where ω represents fundamental angular frequency [41]-[47]. Therefore, notch filters tuned at 2ω and ω are adopted respectively to obtain the corresponding dc components. Most (if not all) previous research that has studied the conventional energy-based controller ignores SM capacitance tolerance.



(a) Conventional Energy Controller of Method-III

(b) Equivalent Energy Controller of Method-IV

Fig. 2-7. Arm controller schematic diagrams of methods III and IV.

Assuming that all SM capacitances are equal, results in the dc components of the common and differential mode energy sums being constant and zero respectively, representing sufficient and necessary conditions for balanced arm capacitor voltage sums. Mathematically, forcing the dc component of the total energy of the upper and

lower arms to be equal does not ensure that the upper and lower arms have the same dc voltage components. And its adverse implication remains unobserved in most previous studies, as the MMC operates away from its maximum modulation index range where all SM capacitors of each arm are inserted or bypassed in order to synthesize the output ac voltage. With unequal capacitance in the upper and lower arms, uncontrolled and unequal fundamental currents are induced into the leg common-mode currents, which can potentially result in a dc output voltage bias.

2.3.4 Method-IV: Equivalent Energy Control

The energy calculation in Method-IV neglects SM capacitance tolerance and assumes each arm has an equivalent capacitance [41], [45], and is thus termed 'Equivalent Energy Control'. The method can be viewed as an alternative implementation of the conventional energy-based controller, but equal SM capacitance assumption means it can be viewed as another implementation of Method-II using the difference and sum of two arm voltages squared instead of direct control of common and differential mode capacitor voltage sums. Assuming the ideal case of equal SM capacitance, leg common and differential mode capacitor voltage sums are:

$$\Sigma \overset{e}{E}_i = \tfrac{1}{2} C_{arm} \times (V_{ciu}{}^2 + V_{cil}{}^2) \tag{2.26}$$

$$\Delta \overset{e}{E}_i = \tfrac{1}{2} C_{arm} \times (V_{ciu}{}^2 - V_{cil}{}^2) \tag{2.27}$$

where C_{arm} represents the equivalent capacitance of the arm and superscript '*e*' refers to the equivalent energy (or energy calculated based on the equal equivalent capacitance). The reference of common-mode capacitor energy sum for a generic leg is:

$$\Sigma \overset{e}{E}_i{}^* = 2 \times \tfrac{1}{2} C_{arm} (N \times V_c{}^*)^2 = 2N \times \tfrac{1}{2} C_{SM} (V_c{}^*)^2 \tag{2.28}$$

where C_{SM} represents the capacitance of each SM and V_c* refers to the SM voltage reference as in Fig. 2-5. Similarly, the controllers are shown in Fig. 2-7(b) and the control objectives of the internal arm controller using Method-IV are to achieve energy balance both among legs and between upper and lower arms within each leg. When these objectives are satisfied, the following equations hold:

$$\tfrac{1}{2}C_{arm}\times(V_{ciu}{}^{2}+V_{cil}{}^{2})=\tfrac{1}{2}C_{arm}\times 2(N\times V_{c}^{*})^{2} \quad (2.29)$$

$$\tfrac{1}{2}C_{arm}\times(V_{ciu}{}^{2}-V_{cil}{}^{2})=0 \quad (2.30)$$

Solving (2.29) and (2.30), yields

$$V_{ciu}{}^{2}=V_{cil}{}^{2}=(N\times V_{c}^{*})^{2}\Rightarrow V_{ciu}=V_{cil}=N\times V_{c}^{*} \quad (2.31)$$

Practically, in the equivalent energy method, the controllers manipulate the sum and difference of squares of the arm voltage sum, where the term ½C_{arm} can be treated as a coefficient lumped into the PI controller gains. Therefore, such an equivalent energy control method is voltage-based and is able to regulate arm SM voltage sum theoretically and practically in most cases [17], [41], [45].

2.3.5 Method-V: Direct Control of Fundamental Frequency Current

Considering the induced fundamental frequency ripple in the common-mode current (and even dc link current), an alternative method is proposed to directly suppress the fundamental components from common-mode currents when significant vertical asymmetry presents. The control system diagram is shown in Fig. 2-8. Instead of dedicated voltage or energy-based differential-mode controllers, a PR controller tuned at 50Hz is used to suppress the ω component in the common-mode currents. This means a zero-magnitude fundamental component is adopted as the reference for the 50Hz band, rather than the differential-mode capacitor voltage sum controllers PI_v^{Δ}.

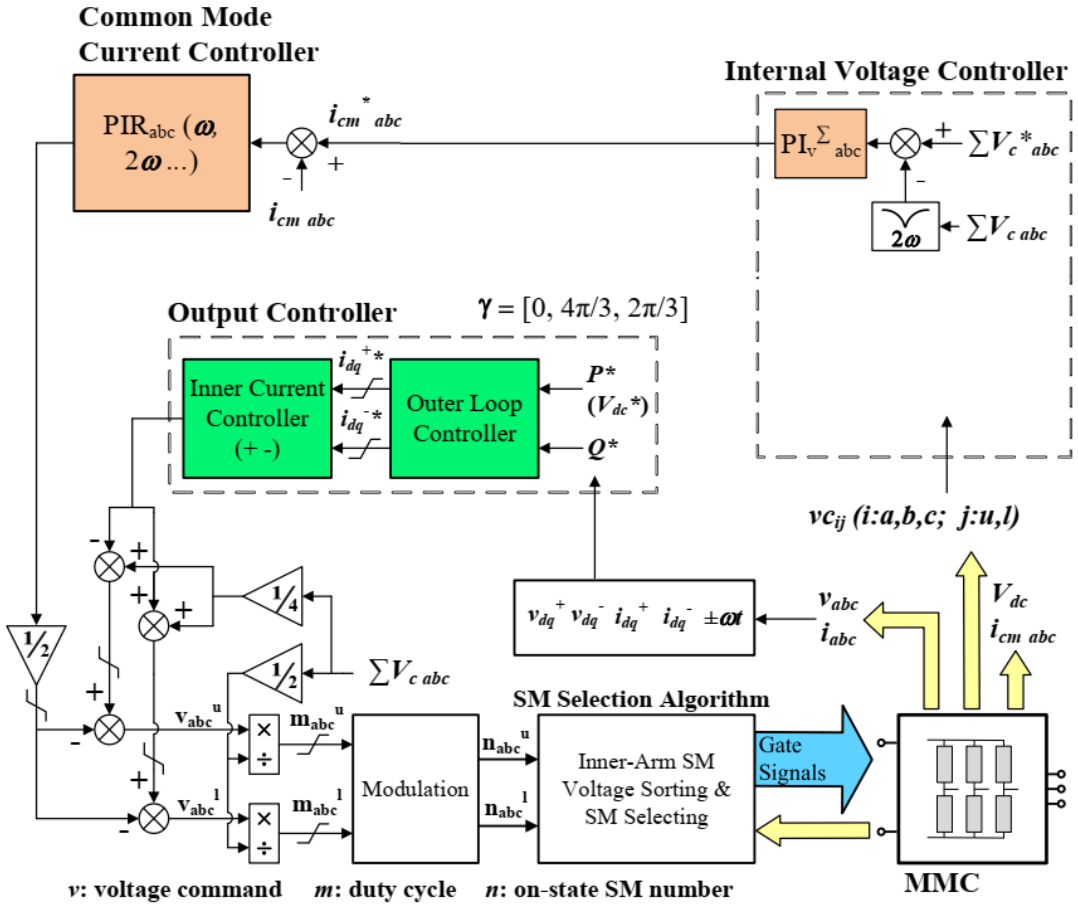


Fig. 2-8. Schematic diagram of the direct elimination method.

2.4 Internal Balancing Assessment Based on Simulation

This section assesses the performance of different internal control methods previously described when the MMC is connected to an ac grid as shown in Fig. 2-9, with simulation parameters in Table 2-1, and with and without considering SM capacitance tolerances.

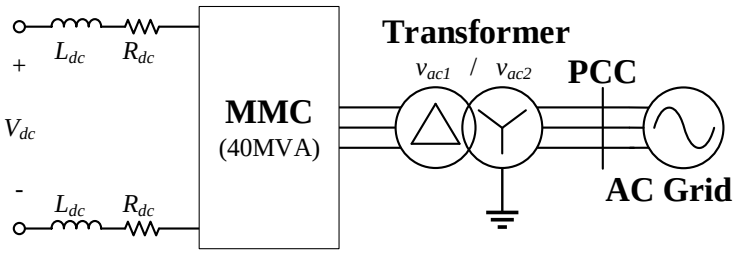


Fig. 2-9. Illustrative 40MW MMC for HVDC transmission system.

Initially, the MMC is controlled to inject 40MW into an ac grid and regulates its average SM capacitor voltage at 2kV (common-mode capacitor voltage sum is 80kV). At t = 0.6s, a step change is applied to the active power output references to reverse the power flow from 40MW to -40MW. At t = 1.2s, a step change is applied to the common-mode capacitor voltage sums to increase the average common-mode capacitor voltage sums (SM average capacitor voltage) by 0.1pu. At t = 1.8s, a single-line-to-ground (SLG) fault is applied at the point of common coupling of phase A. The reactive power output is controlled to be zero. During the SLG fault, the positive-sequence over-current limit is set to 1.1pu and the negative-sequence current is suppressed to zero.

Since the steady-state and dynamics of the output quantities with different inner control schemes are the same, only three-phase phase voltages and currents at the PCC, MMC ac current at the low-voltage side of the interfacing transformer, and average active power are given in Fig. 2-10.

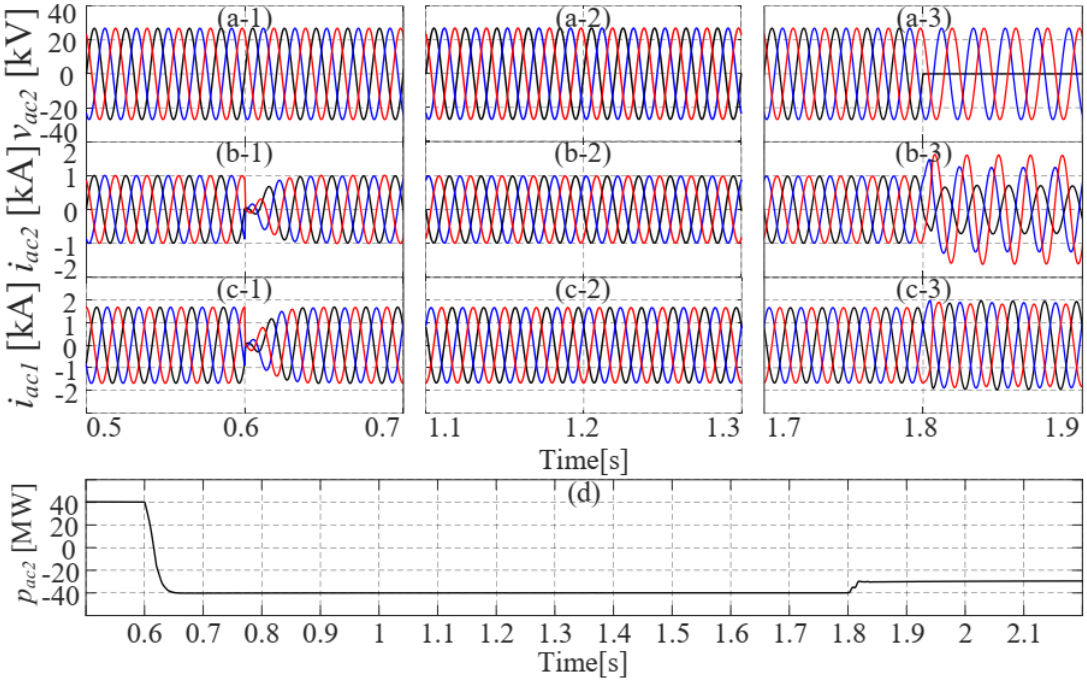


Fig. 2-10. AC output performance: (a) grid phase voltage v_{ac2}, (b) grid current i_{ac2}, (c) MMC side current i_{ac1}, and (d) mean active power p_{ac2}.

Fig. 2-10(a-1), (b-1) and (c-1), and (a-2), (b-2) and (c-2), and (a-3), (b-3) and (c-3) show the voltages and currents at the PCC and currents at the converter side, zoomed

around t = 0.6s (instant of active power reversal), t = 1.2s (application of step change to reference of common-mode capacitor voltage sums) and t = 1.8s (initiation of single-phase ac fault) respectively. These simulation waveforms show the MMC exhibits quick dynamic response during power reversal, presents high quality ac side waveforms to the ac grid, and the magnitude increases of the common-mode capacitor voltage sums do not lead to any noticeable changes in ac current waveforms (which indicates good decoupling of the external dynamics). Also, during the solid single-phase ac fault, the converter ac side currents remain balanced as expected (because of negative sequence current suppression). Fig. 2-10(d) shows active power the MMC injects into PCC over the entire simulation period. The plots shown in Fig. 2-10 confirm the simulated MMC operates correctly, and are similar for all methods being compared.

2.4.1 Performance of Control Schemes in the Symmetrical Case

Fig. 2-11 shows waveforms when only the common-mode capacitor voltage sum (SM average voltage) controller is used with symmetric capacitance. The power reversal at 0.6s triggers a brief damped oscillation period. When the step change is applied to the reference common-mode capacitor voltage sum (to vary its mean from 80kV to 88kV) at 1.2s, the differential-mode capacitor voltage and energy sums exhibit fluctuations. Fig. 2-11(c) and (d) show that the common-mode capacitor voltage sums follow the reference commands, hence horizontal capacitor voltage balance is maintained. As expected, the common-mode capacitor energy sum increases with the common-mode capacitor voltage sum [cf Fig. 2-11(e) and (f)]. In the pre-fault condition, the dc link current is equally distributed between the three legs, which results in balanced common-mode currents; but during the SLG fault, the dc component of the common-mode currents are not equal as expected [cf Fig. 2-11(b)].

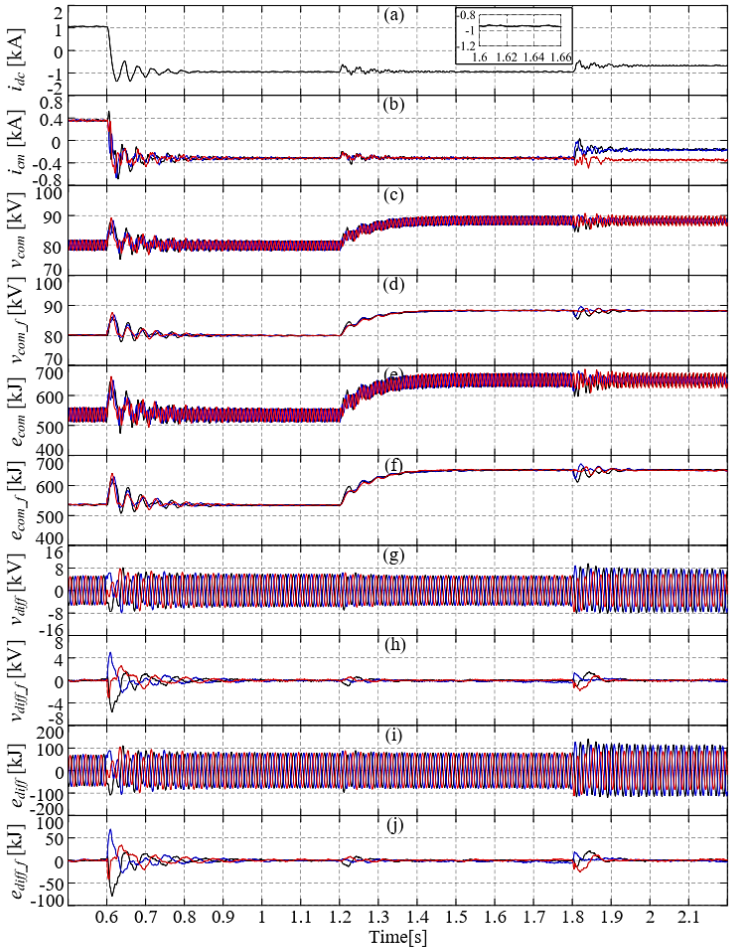


Fig. 2-11. Waveforms of average voltage controller in symmetric case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) common-mode capacitor voltage sum v_{com}, (d) filtered common-mode capacitor voltage sum v_{com_f}, (e) common-mode capacitor energy sum e_{com}, (f) filtered common-mode capacitor energy sum e_{com_f}, (g) differential-mode capacitor voltage sum v_{diff}, (h) filtered differential-mode capacitor voltage sum v_{diff_f}, (i) differential-mode capacitor energy sum e_{diff}, and (j) filtered differential-mode capacitor energy sum e_{diff_f}.

The performance of methods I to IV with zero capacitance tolerance is examined (only the filtered waveforms of the capacitor voltage and energy sums are presented) and system operating conditions remain the same as previously outlined. Parts (a) and (b) in Fig. 2-12-I to IV show that all the control methods maintain the same quality dc link current and common-mode currents in the symmetrical case. Horizontal leg energy and voltage balance are achieved, with dc link current equally distributed among the three legs. During the SLG fault, the common-mode mean currents become unequal, with the average SM voltage unchanged, thus, the three common-mode capacitor energy sums (leg power integral) are unchanged [cf (c)-(f) in Fig. 2-12-I to IV]. For vertical balance of the symmetric legs, the mean voltage (energy) difference of the

arms remains zero [cf (e) and (f) in Fig. 2-12-I to IV]. It is concluded that the analysed control methods basically show the same performance, with both horizontal and vertical voltage/energy balance with symmetrical capacitance.

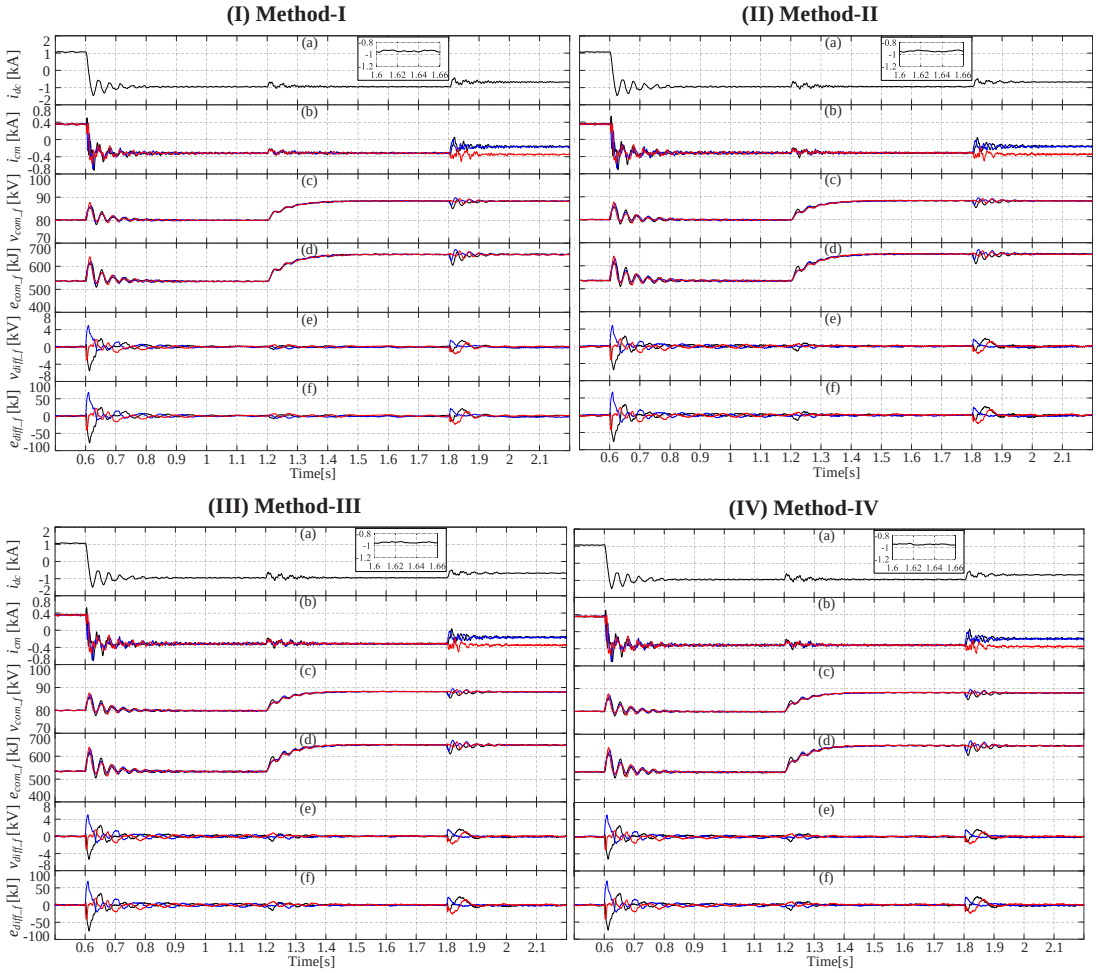


Fig. 2-12. Waveforms of methods I to IV in the symmetrical case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, and (f) filtered differential-mode capacitor energy sum e_{diff_f}.

2.4.2 Performance of Control Schemes with Horizontal Capacitance Asymmetry

Each leg B SM capacitance is assumed to be $0.9C_{SM}$, while that of legs A and C are C_{SM}. Fig. 2-13 shows the waveforms when only a common-mode capacitor voltage sum controller is used.

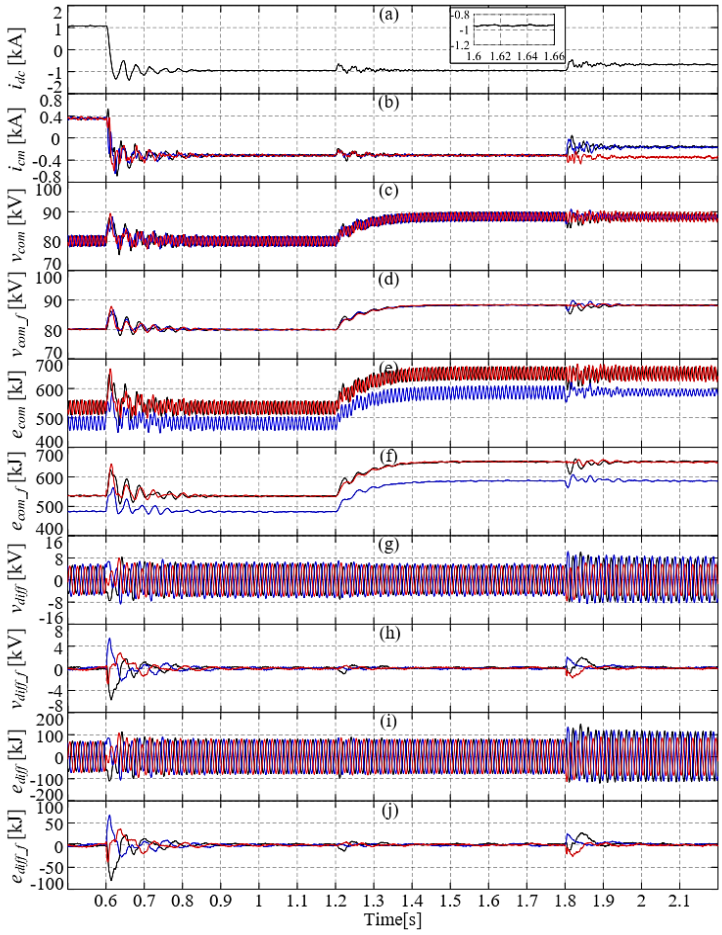


Fig. 2-13. Waveforms of average voltage controller in horizontal asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) common-mode capacitor voltage sum v_{com}, (d) filtered common-mode capacitor voltage sum v_{com_f}, (e) common-mode capacitor energy sum e_{com}, (f) filtered common-mode capacitor energy sum e_{com_f}, (g) differential-mode capacitor voltage sum v_{diff}, (h) filtered differential-mode capacitor voltage sum v_{diff_f}, (i) differential-mode capacitor energy sum e_{diff}, and (j) filtered differential-mode capacitor energy sum e_{diff_f}.

Because the common-mode capacitor voltage sums are horizontally balanced, the average common-mode capacitor energy sum of leg B is lower than those in legs A and C [cf Fig. 2-13(c)-(f)]. In the horizontal asymmetry case, without vertical balancing (differential-mode capacitor voltage/energy sum) control, there is no obvious oscillation in the dc link current and common-mode currents [cf (a) and (b) in Fig. 2-13].

The effectiveness of control methods I to IV with horizontal asymmetry can be assessed from the simulation waveforms in Fig. 2-14 (only the filtered waveforms of the capacitor voltage and energy sums are presented).

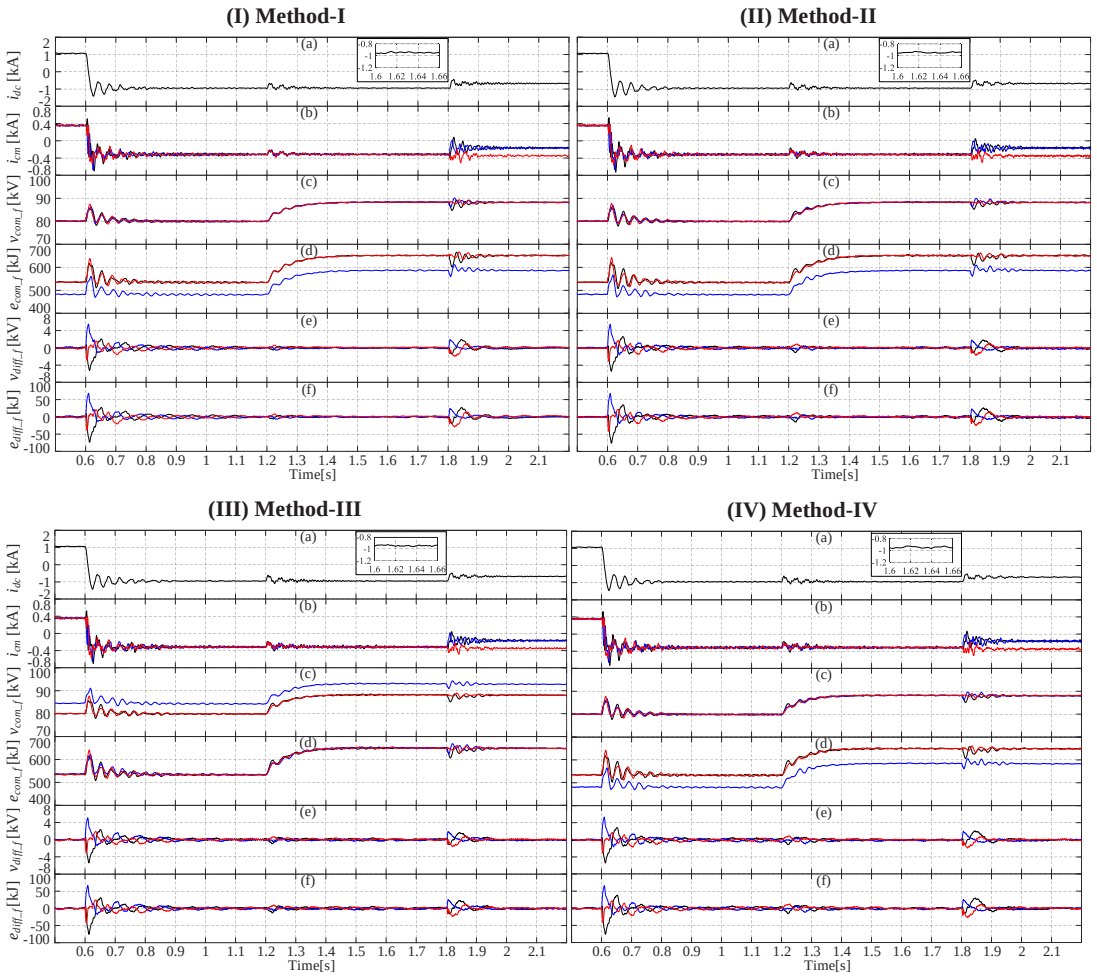


Fig. 2-14. Waveforms of methods I to IV in horizontal asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, and (f) filtered differential-mode capacitor energy sum e_{diff_f}.

When horizontal voltage balance is accomplished by methods I and II, the common-mode capacitor energy sum stored in leg B is lower than symmetrical legs A and C because of lower capacitance during steady-state and remain unchanged during dynamic conditions. This indicates the three legs exchange zero energy (active power integral) with the ac grid [cf (c) and (d) in Fig. 2-14-I and II]. Without vertical capacitance asymmetry, dc link current, common-mode current shows normal characteristics without ripple [cf (a), (b), (e) and (f) in Fig. 2-14-I and II]. Similar performance is seen in Fig. 2-14-IV for Method-IV that purports to control energy through equal equivalent capacitance and square of voltage sum. Fig. 2-14-III(c) and (d) based on Method-III show that with balanced common and differential mode capacitor energy sums, the capacitor voltage sum of leg B is higher than the other legs

with horizontal asymmetrical capacitance (when capacitances of both arms of leg B are deliberately set different from those of legs A and C). There is no noticeable ripple in the dc link current and common-mode currents; and the differential-mode characteristics are acceptable [cf Fig. 2-14-III(a), (b), (e) and (f)].

2.4.3 Performance of Control Schemes with Vertical Capacitance Asymmetry

For the vertical asymmetry case of leg B, each SM capacitance of the upper arm is assumed to be $0.9C_{SM}$, while those of the lower arm are $1.1C_{SM}$.

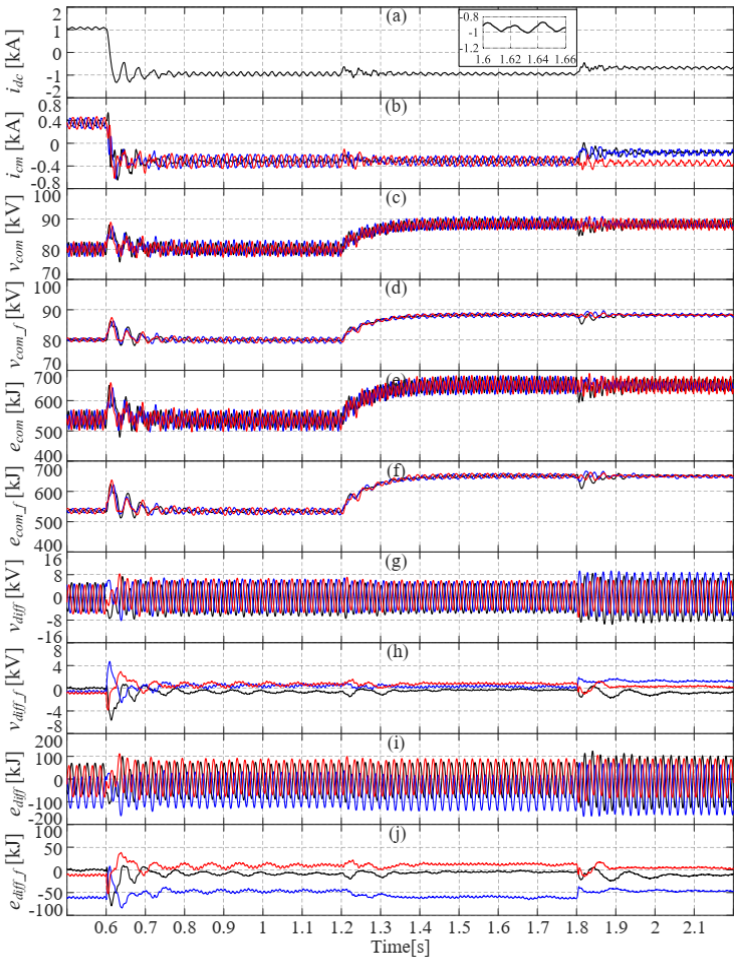


Fig. 2-15. Waveforms of average voltage controller in vertical asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) common-mode capacitor voltage sum v_{com}, (d) filtered common-mode capacitor voltage sum v_{com_f}, (e) common-mode capacitor energy sum e_{com}, (f) filtered common-mode capacitor energy sum e_{com_f}, (g) differential-mode capacitor voltage sum v_{diff}, (h) filtered differential-mode capacitor voltage sum v_{diff_f}, (i) differential-mode capacitor energy sum e_{diff}, and (j) filtered differential-mode capacitor energy sum e_{diff_f}.

Fig. 2-15 shows the waveforms when only common-mode capacitor voltage sum control is used. The mean values of common-mode capacitor voltage and energy sums

of the three legs are basically the same [cf Fig. 2-15(c)-(f)]. However, without vertical symmetry, the deviations observed in the differential-mode capacitor voltage and energy sums indicate that neither vertical voltage balance nor vertical energy balance is achieved, especially in leg B [cf Fig. 2-15(g)-(j)]. Also, the dc link and common-mode currents exhibit 50Hz oscillation [cf Fig. 2-15(a) and (b)]. This 50Hz oscillation in the common-mode currents of the legs with symmetrical capacitances (legs A and C) is caused by coupling interaction through the shared dc bus terminal. Fundamental components of the common-mode currents further actuate small dc voltage deviations in the differential-mode capacitor voltage sum of legs A and C. Provided the dc voltage deviation between the upper and lower arms remains small, and the output ac voltages being synthesized do not require the modulation index to reach its maximum limit [cf Fig. 2-15(g) and (h)], the MMC output ac voltage is not affected.

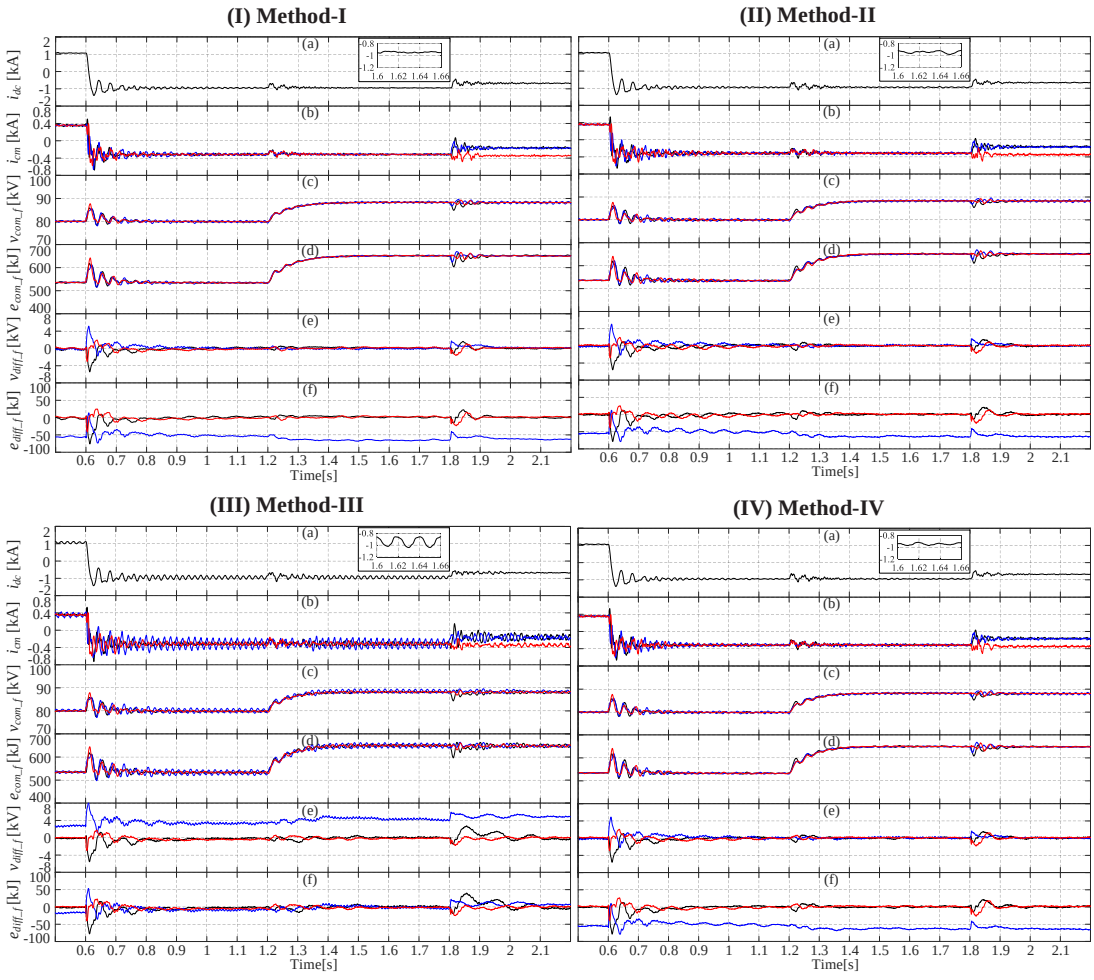


Fig. 2-16. Waveforms of methods I to IV in vertical asymmetry case: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered

common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, and (f) filtered differential-mode capacitor energy sum e_{diff_f}.

MMC internal dynamic regulation performance results for methods I to IV during vertical asymmetry are given in Fig. 2-16. For the voltage-based control schemes in Fig. 2-16-I and II (c) and (d), horizontal voltage balance is maintained, with the mean values of the common-mode capacitor energy sums controlled to be equal and constant. Also, the vertical voltage balance controllers have reduced the deviation of the mean differential-mode capacitor voltage sum to zero, achieving equalization of the total dc capacitor voltage sum across both arms of each leg under normal and fault conditions [cf (e) in Fig. 2-16-I and II]. However, the capacitor energy sums of each arm remain unequal as predicted [cf (f) in Fig. 2-16-I and II]. With these voltage-based methods that include both horizontal and vertical controllers, the positive and negative sequence fundamental currents which appear as unbalanced ac components in the common-mode currents, are significantly reduced, with the 50Hz negative sequence current that appears as oscillation in the dc link current being suppressed [cf (a) and (b) in Fig. 2-16-I and II]. Also, the results of Method-IV (capacitor voltage sum squared as the control variable instead of the actual energy), indicate that its performance under normal and abnormal conditions is similar to that of the methods I and II [cf Fig. 2-16-IV]. In contrast, the results of Method-III that exploits the actual energy as control variables, show that the horizontal balancing indicators such as the common-mode capacitor energy and voltage sums remain balanced during vertical asymmetry [cf Fig. 2-16-III(c) and (d)]. The differential-mode capacitor energy sums of all three legs are, however, nullified after an extended oscillation period (which indicates vertical arm energy balance is ensured), under both normal and fault conditions [cf Fig. 2-16-III(f)]. However, ensuring vertical energy balance in Method-III increases the deviation of the mean differential-mode capacitor voltage sums from zero, which leads to failure of arm vertical voltage balance in the case of vertical asymmetry [cf Fig. 2-16-III(e)]. This phenomenon increases the magnitudes of unbalanced 50Hz components in the common-mode currents and common-mode capacitor voltage, which reflect into the dc link current [cf Fig. 2-16-III(a)-(d)]. As Method-III fails to ensure arm voltage balance, the mean capacitor voltage sum of leg B lower arm is approximately 38kV and 42kV, respectively, before and after the

application of the step change to the common-mode capacitor voltage sum at 1.2s. This indicates that the dc voltage across the lower arm remains below 40kV and 44kV, respectively, before and after 1.2s, but high enough and sufficient to synthesize the required MMC output ac voltage amplitude. Thus, no distortion is observed in the output ac voltage [cf Fig. 2-10(c) and Fig. 2-16-III(e)].

2.4.4 Performance of the Direct Fundamental Ripple Suppression Method

The effectiveness of Method-V (for fundamental ripple suppression) is assessed in this simulation section (Fig. 2-17). As this method is specific for suppressing the fundamental ripple caused by upper and lower arm asymmetry, results are presented in two typical cases, namely, with and without capacitance tolerances in leg B.

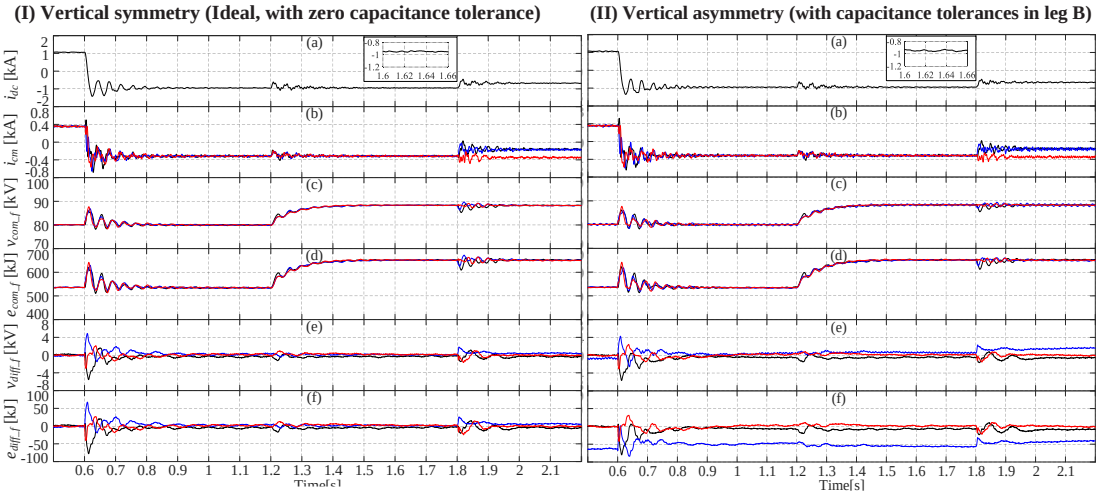


Fig. 2-17. Waveforms of the direct fundamental oscillation elimination method in symmetry and vertical asymmetry cases: (a) dc link current i_{dc}, (b) common-mode current i_{cm}, (c) filtered common-mode capacitor voltage sum v_{com_f}, (d) filtered common-mode capacitor energy sum e_{com_f}, (e) filtered differential-mode capacitor voltage sum v_{diff_f}, and (f) filtered differential-mode capacitor energy sum e_{diff_f}.

Simulation waveforms with zero and ±10% vertical capacitance tolerances are presented in Fig. 2-17-I and II respectively. These results show that with the common-mode capacitor voltage sum being controlled, horizontal capacitor voltage balance is achieved [cf (c) in Fig. 2-17-I and II]. When vertical capacitance tolerance asymmetry is considered, the 50Hz oscillation in the common-mode currents of the three legs and dc link current are suppressed [cf Fig. 2-17-II(a) and (b)]. The 50Hz fundamental oscillation of the common-mode capacitor voltage is cancelled by injecting the appropriate fundamental frequency voltage into the modulating signals in order to

produce the needed fundamental current to neutralize the 50Hz component [cf Fig. 2-17-II(c)]. However, the proposed fundamental current elimination method is unable to nullify the mean differential capacitor voltage sums with vertical capacitance asymmetry (both arm capacitor voltages remain unbalanced) [cf Fig. 2-17-II(d) and (e)]. This may limit the maximum attainable modulation index as the arms with the lower dc voltages would be unable to synthesize the needed arm voltages at high modulation indices.

2.5 Overall Comparison Based on Simulation

Iterative simulations of methods for a range of SM capacitance and arm inductance tolerances show the overall relationship between passive component tolerances and normalized fundamental frequency dc link current ripple magnitude with different voltage levels, in Fig. 2-18 and Fig. 2-19 respectively. The base of ripple magnitude normalization is the mean dc link current.

Based on the parameters in Table 2-1, the overall relationship between vertical capacitance and inductance asymmetry (different capacitance and inductance tolerances between upper and lower arms of the same leg) and normalized magnitude of fundamental frequency dc link current ripple are shown in Fig. 2-18-I and Fig. 2-18-II respectively, based on the different control methods being examined. Under these simulated conditions, the fundamental ripple magnitude is generally below 5% with all control methods, for SM capacitance and arm inductance tolerances ranging from 0 to 10%. Without a vertical balancing controller, no fundamental current appears in the dc link when SM capacitance and arm inductance tolerances are zero (ideal or vertical symmetry), but the 50Hz oscillation magnitude in the dc link current increases linearly with MMC passive component tolerance. This study also shows that as capacitance asymmetry increases, control methods I, II, IV and the direct fundamental frequency current elimination method remain capable of suppressing the dc link fundamental current ripple. Method-III, however, leads to the fundamental frequency current ripple magnitudes increasing with increasing SM capacitance tolerance. The conclusions drawn from this discussion of Fig. 2-18 are in accordance with the approximate theoretical analysis articulated mathematically.

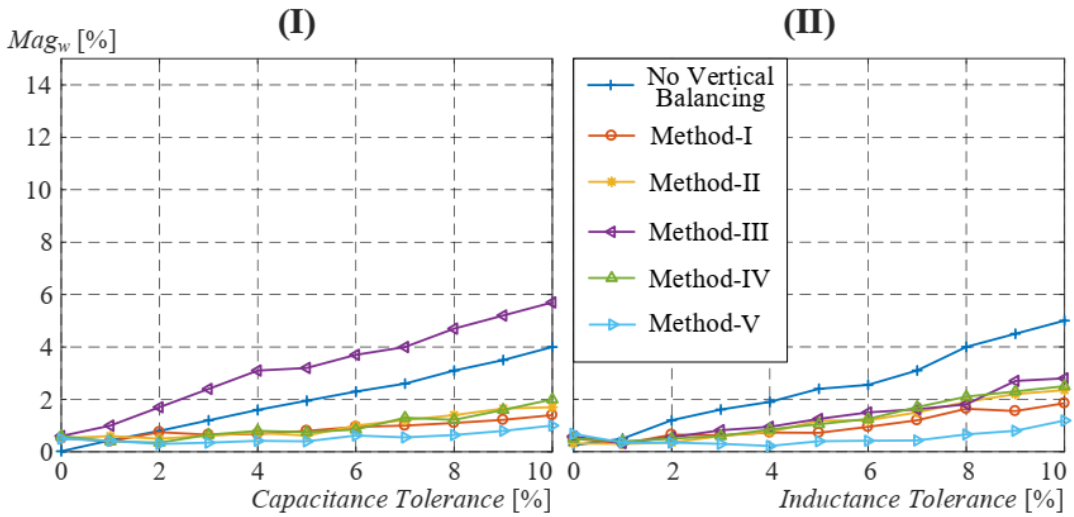


Fig. 2-18. Relationship between normalized dc link current ripple magnitude and passive component tolerances, with different control methods (Table 2-1).

To further illustrate the impact of the switching voltage step (voltage per SM) on dc power quality, the same MMC system and control methods with different parameters, as listed in Table 2-2, is investigated.

Table 2-2. Simulation parameters of the 100MVA MMC.

Rated power	100MVA
DC voltage	100kV
AC grid line voltage	66kV
AC grid frequency	50Hz
Transformer leakage inductance	0.18pu
Transformer ratio	50/66kV
Arm inductance	15.3mH(0.2pu)
Numbers of SMs per arm	20
SM capacitance	2.7mF(40kJ/MVA)
Modulation carrier frequency	1.0kHz

The plots in Fig. 2-19 for the 100kV dc link voltage MMC with an SM voltage of 5kV show a similar trend to the counterparts in Fig. 2-18 when the dc link voltage is 40kV and SM voltage is 2kV. In addition to the generally increased fundamental current ripple due to capacitance and inductance tolerances, Fig. 2-18 and Fig. 2-19 show further increase of the current ripple with the dc link voltage, meaning that the ripple amplitude is exacerbated by the increased average SM capacitor voltage (or switching voltage).

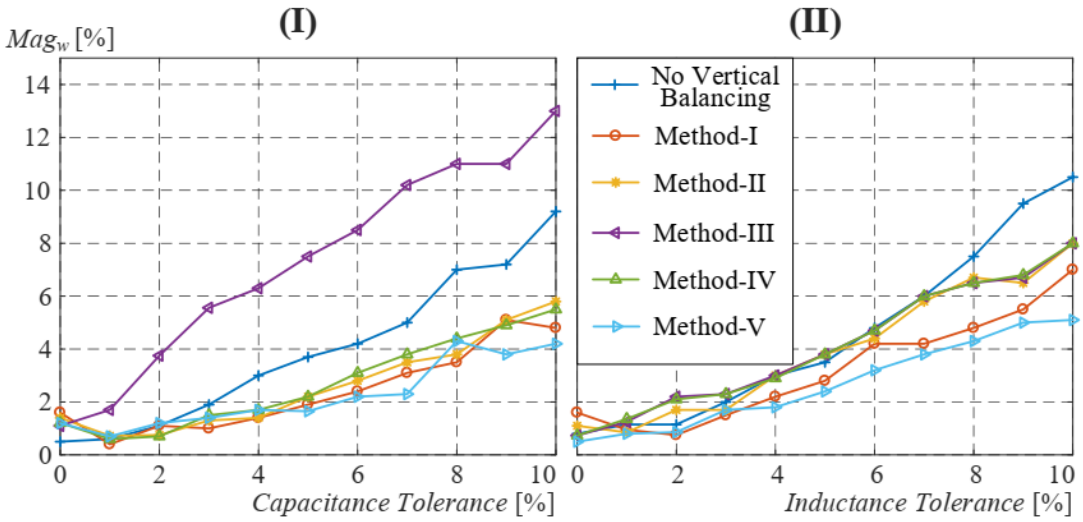


Fig. 2-19. The relationship between normalized dc link current ripple magnitude and passive component tolerances, with different control methods (Table 2-2).

Vertical passive component tolerances tend to cause drift of the differential-mode capacitor voltage sum from zero and fundamental frequency dc link current ripple for an MMC system, as indicated by the mathematical expressions. Voltage-based vertical balancing controllers (methods I, II and IV) can eliminate the differential-mode capacitor voltage sum. The proposed control method (Method-V), which directly suppresses fundamental components of the common-mode current regardless of arm voltage balance, shows superior performance in terms of dc link fundamental current ripple suppression. These observations indicate that none of the previously discussed methods can eliminate the fundamental current ripple completely although some could be adopted to obtain a lower magnitude; implementing hardware-based balanced component value maintenance should be considered under feasible conditions.

A more practical simulation study is presented to assess the performance of selected internal and external decoupling control methods when passive component tolerances are considered. An MMC-based HVDC transmission station with a 40km dc cable is simulated with the control methods in the previous parts and parameters listed in Table 2-3. Given the previous observation, four control methods are considered in these parametric studies in terms of MMC internal dynamics regulation. The methods are: Method-II with no vertical balance, Method-II, Method-III and the direct fundamental current ripple suppression approach.

Table 2-3. New simulation parameters of the 100MVA MMC station.

DC voltage	100kV
AC grid line to line voltage	66kV
Transformer ratio	50/66kV
Transformer leakage-inductance	0.2pu
Numbers of SMs per arm	50
Expected arm inductance value	0.18pu
Expected SM capacitance value	6.7mF
Cable resistance per km	10mΩ/km
Cable inductance per km	1.4mH/km
Cable capacitance per km	0.1μF/km

Fig. 2-20 and Fig. 2-21 depict detailed quantitative comparison of the fundamental frequency ripple in the dc current normalized by the mean value and attainable modulation range versus passive component tolerances, for the four methods.

Fig. 2-20-I to Fig. 2-20-IV show that certain combinations of passive component tolerances exhibit larger fundamental frequency ripple in the dc current. Fig. 2-20-II and Fig. 2-20-III reveal that Method-II exhibits better fundamental ripple suppression than Method-III. Also, Fig. 2-20-IV displays the smallest fundamental frequency ripple among all methods.

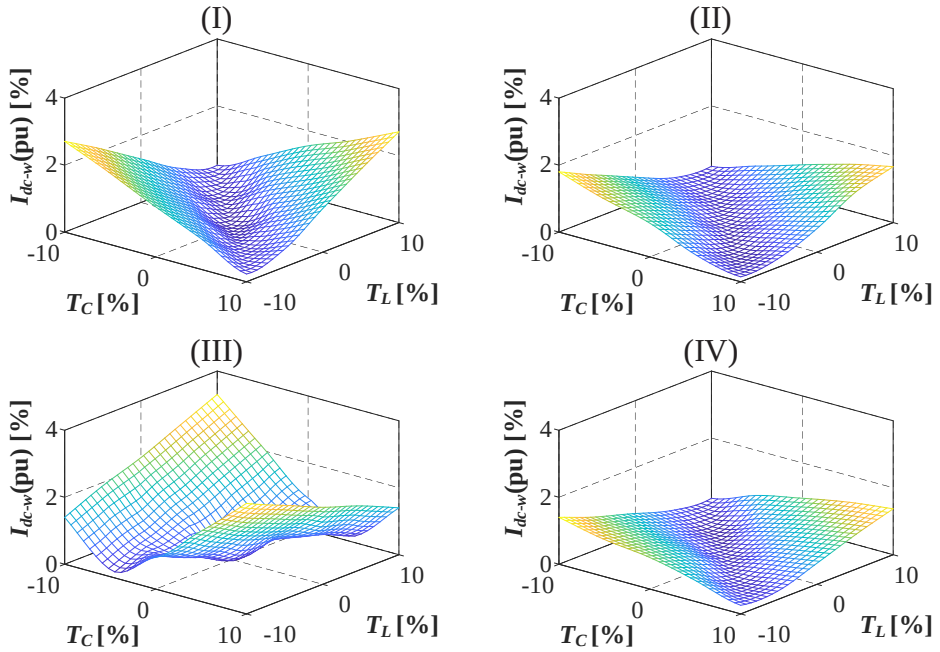


Fig. 2-20. Variation of fundamental frequency dc-link current ripple magnitude (pu) with SM capacitance tolerances T_C and arm inductor tolerances T_L: (I) Method-II with no vertical balance, (II) Method-II, and (III) Method-III, (IV) Method-V.

Fig. 2-21-I and IV show that with Method-II with no vertical balance and direct fundamental current ripple suppression, the component tolerances reduce the linear modulation index range by 2% approximately, whilst Method-II retains maximum and nearly constant modulation index range for all tolerances (Fig. 2-21-II). Fig. 2-21-III shows the modulation index range of Method-III deteriorates rapidly and mainly with capacitance tolerance. Also, Fig. 2-21-IV shows that the direct fundamental current ripple suppression method offers the best performance in term of fundamental frequency ripple suppression at the expense of a small linear modulation range reduction.

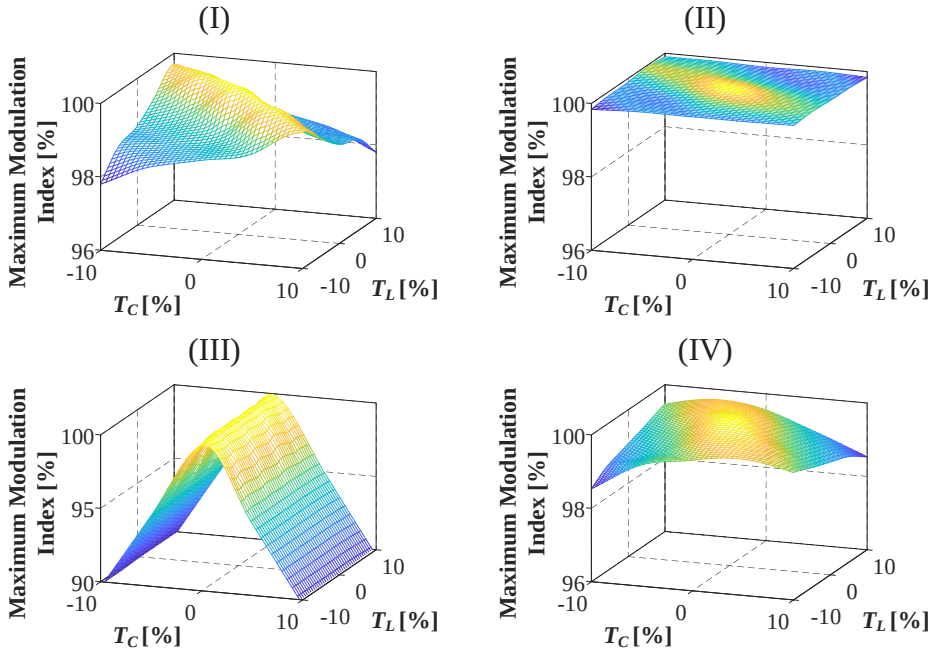
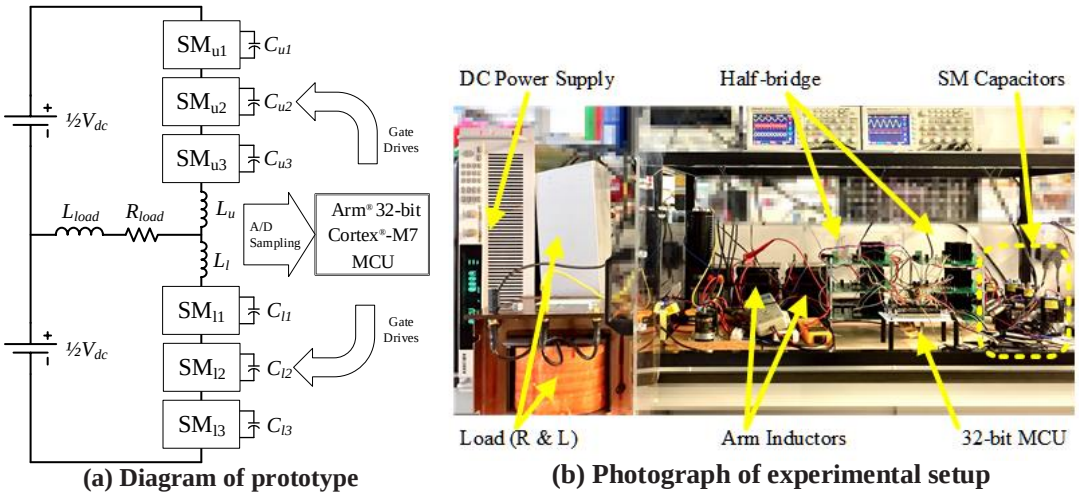


Fig. 2-21. Variation of maximum modulation index with SM capacitance tolerances T_C and arm inductor tolerances T_L: (I) Method-II with no vertical balance, (II) Method-II, (III) Method-III, and (IV) Method-V.

2.6 Inter-Arm Control Study Using Experimentation

A single-phase MMC prototype is built in the laboratory as shown in Fig. 2-22, with parameters in Table 2-4 and Table 2-5. This section uses the prototype to validate the previously presented analysis and simulations, particularly, with regard to the relationship between passive parameter mismatch, differential-mode capacitor voltage sum, and induced fundamental circulating current.



(a) Diagram of prototype **(b) Photograph of experimental setup**

Fig. 2-22. Schematic diagram and photograph of the prototype scale-down single-phase MMC with three SMs per arm.

Table 2-4. Parameters of the single-phase MMC prototype.

Rated power	1kW
DC voltage V_{dc}	300V
Load resistance R_{load}	5Ω
Load inductance L_{load}	12.5mH
Nominal arm inductance L_{arm}	5mH
Numbers of SMs per arm	3
Nominal SM capacitance C_{SM}	1.8mF
Modulation index	0.8
Modulation carrier frequency	2.0kHz

Table 2-5. Values of the passive components (for both symmetry and asymmetry cases).

	Symmetry	**Asymmetry**
C_{u1}	1.84mF	
C_{u2}	1.80mF	
C_{u3}	1.78mF	
C_{l1}	1.82mF	
C_{l2}	1.74mF	1.62mF
C_{l3}	1.79mF	1.66mF
L_u	5.5mH	
L_l	5.7mH	

As part of the validation process, a number of experimental scenarios are presented, namely, no vertical balancing, and scenarios with Method-II (voltage-based vertical balancing), Method-III (energy-based vertical balancing) and the proposed direct fundamental circulating current elimination method. Table 2-5 shows SM capacitances

and inductances of the experimental test rig, with vertical symmetrical and asymmetrical capacitances. Besides capacitor voltage balancing, the horizontal voltage balancing controller that regulates the mean common-mode capacitor voltage sum of the phase-leg at rated dc link voltage (300V), is implemented in all scenarios. The sorting-based inner arm SM voltage balancing method with PD-PWM modulation is adopted.

Fig. 2-23 shows experimental waveforms with no vertical balancing, voltage-based vertical balancing, energy-based vertical balancing, and the proposed direct fundamental circulating elimination method, when the SM capacitors are near matched in order to reflect the ideal case of vertical symmetry. The fundamental circulating current magnitude of the method without vertical balancing is smallest in the symmetrical case because no active injected current is present. The magnitude of fundamental circulating currents that exist in the common-mode current are practically the same for the cases with voltage-based vertical balancing and energy-based vertical balancing, cf Fig. 2-23-II and III. While the proposed direct elimination of fundamental current exhibits a reduction compared with that of voltage/energy balancing methods, which can be seen in Fig. 2-23-IV, but with the penalty of creating substantial arm voltage imbalance, with the error in the dc offset of the differential mode capacitor voltage sum V_{armdif} amounting to 9V (equivalent to SM capacitor voltage deviations of ±1.5% from their respective nominal values). With small SM capacitance value errors plus randomness of the unquantified errors introduced by semiconductor voltage drops, switching characteristics and other nonlinearities, the cases with no vertical balancing and energy-based vertical control show modest drift or error between the capacitor voltage sums across the upper and lower arms (cf Fig. 2-23-I and III), while the voltage-based vertical balancing in Fig. 2-23-II shows the smallest dc voltage error between the upper and lower arms. The differences in the quality of the output voltage and current waveforms between these methods are small (worst-case output phase voltage and current total harmonic distortion of 20.3% and 0.4% respectively).

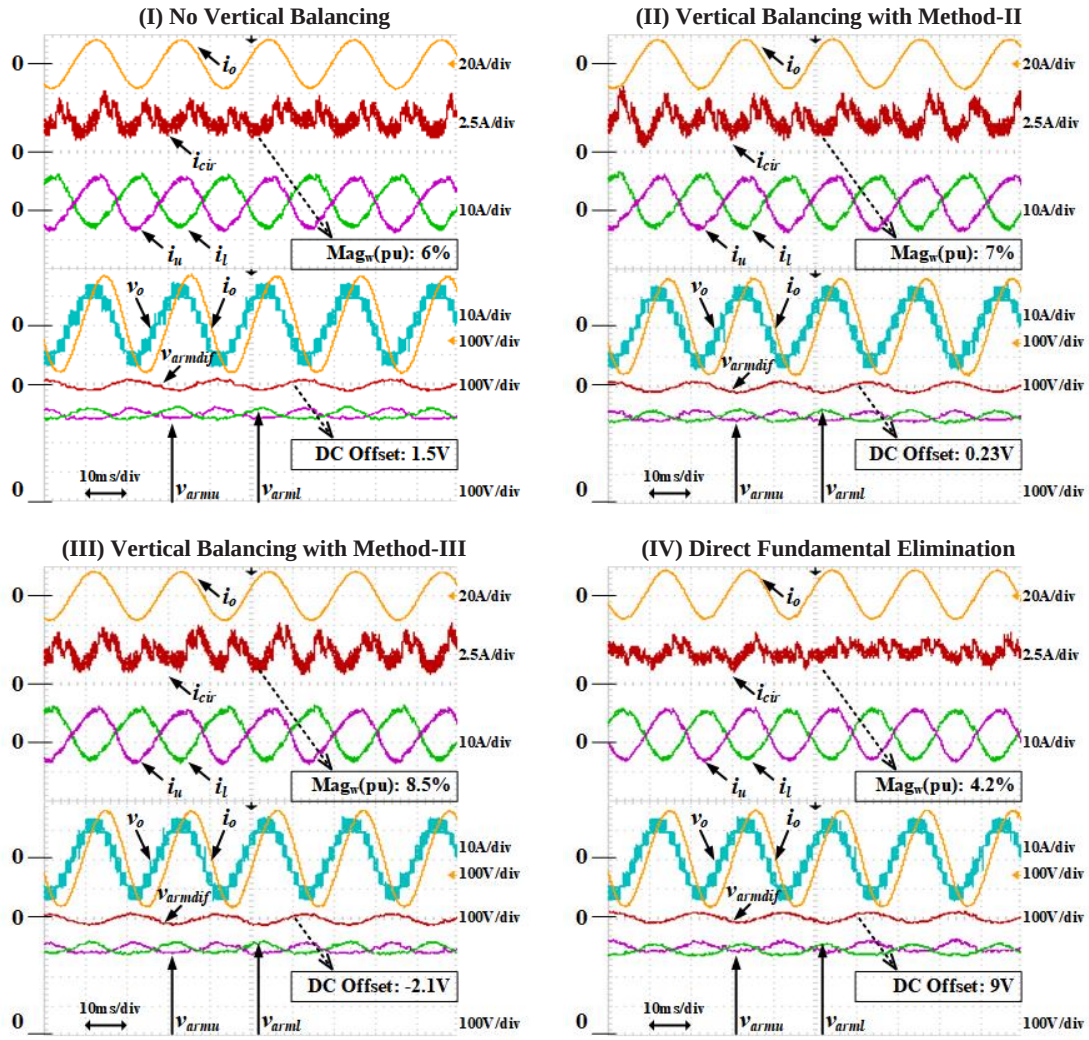


Fig. 2-23. Waveforms of no vertical balancing, Method-II, Method-III and the direct elimination method in vertical symmetry case.

In contrast, Fig. 2-24 shows experimental waveforms for the considered methods with the asymmetrical capacitance shown in Table 2-5. The fundamental circulating current magnitudes increase for all methods, and cases without vertical balancing and with the energy-based vertical balancing exhibit larger fundamental circulating currents and larger errors in the differential-mode capacitor voltage sums (large degree of voltage imbalance between upper and lower arms), cf Fig. 2-24-I and III. The fundamental frequency circulating current magnitude is suppressed by the proposed direct elimination method, but creates a voltage imbalance between the upper and lower arms, cf Fig. 2-24-IV. Thus, capacitor voltages exhibit deviations of ±3V for each SM (±3% from their respective nominal values). The voltage-based vertical balancing method in Fig. 2-24-II shows the best overall performance in terms of compromise

between fundamental circulating current magnitude and arm voltage imbalance. The results in Fig. 2-23 and Fig. 2-24 confirm the theoretical analysis and discussion presented. The differences in the quality of the output voltage and current waveforms between the methods are small (THD = 21.1% and 0.49% respectively).

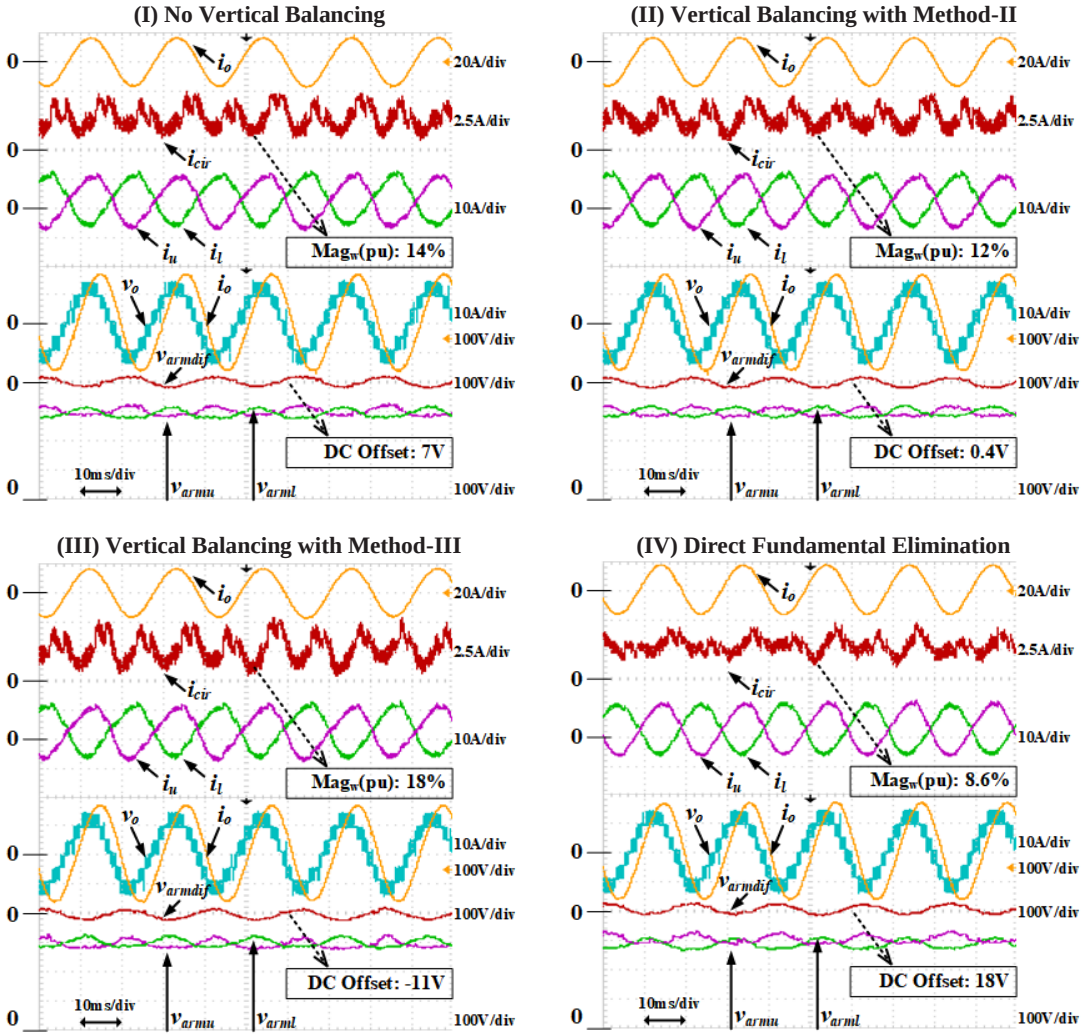


Fig. 2-24. Waveforms without vertical balancing, Method-II, Method-III and the direct elimination method in vertical asymmetry case.

In summary, the presented experimental waveforms corroborate the detailed theoretical analysis. It can be argued that for an MMC with passive component tolerances, the voltage and equivalent energy based vertical controllers estimate an appropriate amount of fundamental voltage to be injected into the common-mode voltage of each phase-leg in order to force the differential-mode capacitor voltage sums to be zero, therefore, the fundamental current ripple in the common-mode and

dc currents are by-products. The proposed method estimates a suitable fundamental voltage to be injected into the common-mode loop of each phase-leg in order to directly eliminate the fundamental components from the common-mode and dc link currents, with the differential-mode capacitor voltage sum deviations being the by-product.

2.7 Summary

Table 2-6 summarizes the main attributes and limitations of the different methods of managing the MMC internal dynamics investigated in this chapter.

Table 2-6. Summarized features of the assessed internal control schemes.

	Method-I	**Method-II**	**Method-III**	**Method-IV**	**Method-V**
SM-Level Performance	Able to equally distribute the total arm voltage across SM capacitors.				
	All switching devices operate at a fixed frequency.	Switching devices operate at a frequency that varies within a limited range.			
Arm-Level (Vertical) Balancing	Able to suppress capacitor voltage difference between upper and lower arms of each phase-leg to near zero even when passive components have significant tolerance.	Able to suppress capacitor voltage difference between upper and lower arms of each phase-leg to near zero even when passive components have significant tolerance.	The capacitor voltage difference between upper and lower arms of one phase-leg increases rapidly with capacitance tolerance.	Able to suppress capacitor voltage difference between upper and lower arms of each phase-leg to near zero even when passive components have significant tolerance.	Cannot ensure capacitor voltage difference between upper and lower arms of one phase-leg to be zero when passive components have significant tolerance.
AC Side Performance	Minimizes risk of dc offsets in ac output voltages and currents, due to vertical balancing capability.	Minimizes risk of dc offsets in ac output voltages and currents, due to vertical balancing capability.	Imposes potential risk of dc offsets in ac output voltages and currents due to inferior vertical balancing performance.	Minimizes risk of dc offsets in ac output voltages and currents, due to vertical balancing capability.	Imposes potential risk of dc offsets in ac output voltages and currents due to lack of actively vertical balancing capability.
DC Side Performance	Able to reduce fundamental frequency ripple in dc link current in practical systems with vertically passive component tolerances.	Able to reduce fundamental frequency ripple in dc link current in practical systems with vertically passive component tolerances.	Unable to reduce fundamental frequency ripple in dc link current in practical systems with vertical capacitance tolerances.	Able to reduce fundamental frequency ripple in dc link current in practical systems with vertically passive component tolerances.	Exhibits superior capacity of suppressing fundamental frequency ripple in dc link current in practical systems with vertically passive components tolerances.

Leg-Level (Horizontal) Balancing	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during operation near maximum modulation index.	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during operation near maximum modulation index.	Creates unbalanced common-mode capacitor voltage sums across the phase-legs in practical systems with horizontal passive component tolerances. The risk of curtailing synthesis of maximum ac output voltage increases in phase-leg that possess larger equivalent capacitance. The phase-leg that possess smaller equivalent capacitance may experience over-voltage.	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during operation near maximum modulation index.	Maintains common-mode capacitor voltage sums of phase-legs to be practically balanced, avoiding the risk of momentary inrush currents during operation near maximum modulation index.

The findings of this section can be applied to optimize and predict MMC internal dynamics and internal/external decoupling, and scenarios when the submodule fault management is activated to bypass faulted submodules. The difference of distributed and non-distributed submodule capacitor voltage balancing (inner arm balancing) on the performance of horizontal and vertical balancing controllers is also taken into account. Simulations under a number of severe test scenarios (such as unrestrained step change in the reference active power and average capacitor voltage per leg, and single-phase-to-ground ac fault) and experimental results for different vertical balancing methods were presented. The main contribution and significance of the research presented in this section beyond those previously explored in the literature are as follows:

- The presented theoretical analysis, simulations and experimentation show that submodule capacitance and arm inductance tolerances can lead to MMC performance deterioration, namely, in the quality of ac and dc voltage and current waveforms, and voltage stress distribution between the upper and lower arms will be compromised;

- Only vertical asymmetry of the submodule capacitances and arm inductances give rise to induced fundamental frequency ripple in the common-mode and dc link currents, and unequal dc voltage sharing between MMC upper and lower arms, which can lead to dc offsets in the output phase currents and voltages. The presented detailed parametric studies revealed that these problems are acute for an MMC with larger switching voltages (voltage per SM capacitor). The horizontal asymmetry of the SM capacitances and arm inductances does not induce fundamental ripple in the common-mode and dc link currents or imbalance between upper and lower MMC arms of one phase-leg. Besides substantial differences in the energy storage of the three phase-legs, horizontal asymmetry leads to significant differences in control effort, which may affect utilization of the phase-legs (arm with larger or lower dc modulation index may suffer from under-utilization as its ability to synthesize ac voltage is curtailed);
- Detailed investigation revealed that energy-based vertical and horizontal controllers may exacerbate deterioration of dc current waveform quality and the problem of voltage imbalance between MMC upper and lower arms when passive component tolerances are significant;
- Detailed theoretical investigation on the mechanism by which the fundamental current is induced in the MMC common-mode and dc side has led to the development of a new direct fundamental component elimination method. The effectiveness of proposed method for suppressing the fundamental ripple in the common-mode and dc currents was confirmed using simulation and corroborated experimentally. But this improved performance is achieved at the expense of increased dc voltage imbalance between the upper and lower arms; and
- Detailed quantitative and qualitative comparisons of several methods reveal that the voltage-based vertical and horizontal balancing methods offer the best overall practical compromises between suppression of fundamental ripple in the dc current and dc voltage imbalance between MMC upper and lower arms.

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Chapter 3

T-Type Modular Multilevel Converter (T-MMC)

Generally, any MMC topology design has to evaluate the performance of its SMs and faces a trade-off between a larger arm operational range (usually indicating the dc fault resilient capability) and lower semiconductor losses (which are mainly caused by the added controllable semiconductors in the major current paths). In light of such a challenge, this chapter proposes a novel MMC, named 'T-type MMC' (T-MMC), for more reliable, controllable and efficient performance in power conversion applications. The topology provides various features such as dc fault tolerance, high normal operation efficiency, increased ac-side output range, and feasible energy storage integration. Circuitry configurations and control structures are presented, with respect to its fundamental functions. The T-MMC topology consists of two power stages (Stage-I and Stage-II), which are coordinated for ac and dc fault tolerance, increased ac-side voltage synthesis, etc. A thyristor or disconnector based bypassing technique minimizes the conduction losses of Stage-II; thus T-MMC normal mode operation losses can be equivalent to those of the conventional HB-MMC. Simulation and experimentation demonstrate T-MMC performance.

3.1 T-MMC Circuitry Configurations

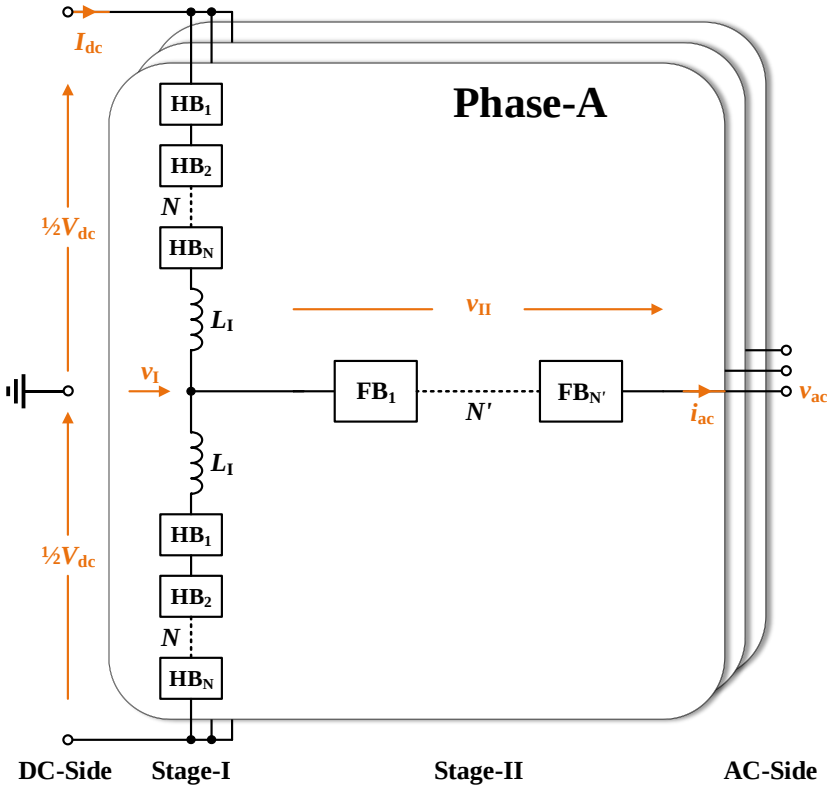
3.1.1 Basic Topology

Fig. 3-1 shows the basic stage topologies, and constructed HB and FB SMs of the proposed T-MMC. One T-MMC phase consists of three star-connected modular arms, with their ends as dc positive, dc negative and ac nodes respectively, resembling the letter 'T'.

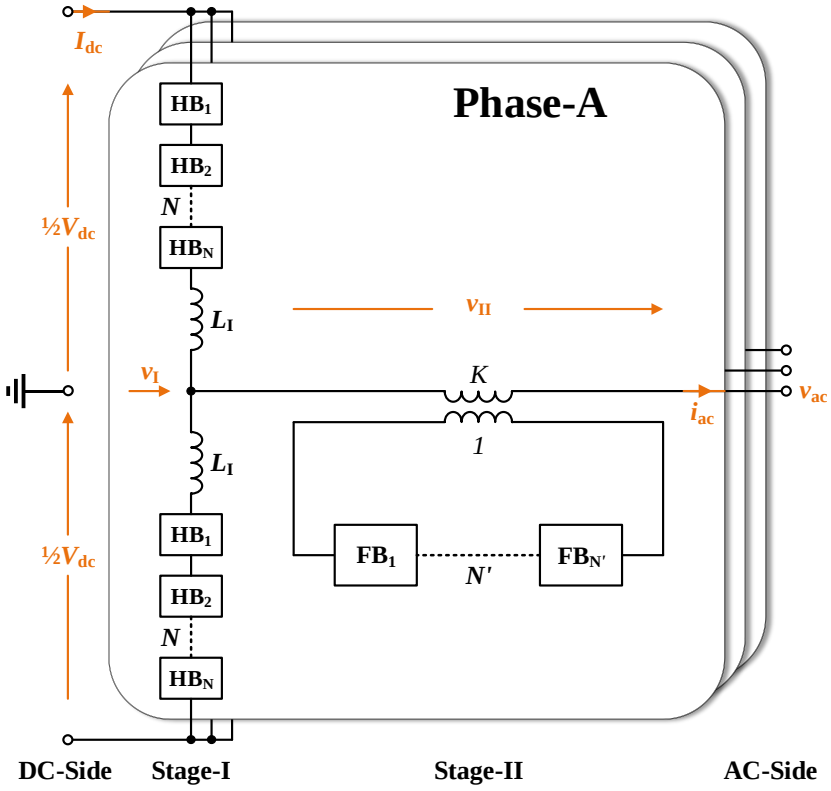
The dc-side power interface (Stage-I) has upper and lower arms, where each consists of N HB-SMs and an arm inductor L_{I}, as that of a conventional HB-MMC. Stage-I can also be other MMC types. The ac-side power interface (Stage-II) can be one arm

composed of N' FB-SMs, as shown in Fig. 3-1(a), or with an interfacing transformer to provide galvanic isolation, as shown in Fig. 3-1(b).

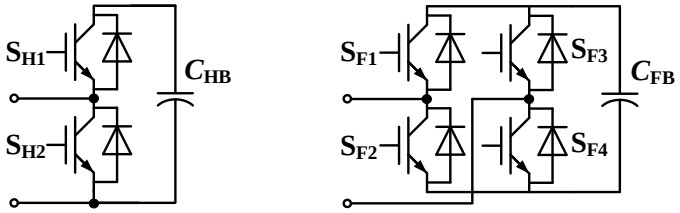
Auxiliary circuits such as the snubbers and any protective SM parallel-connected thyristors are not illustrated.



(a)



(b)



(c) (d)

Fig. 3-1. The T-MMC basic circuit configurations: (a) topology diagram, (b) topology diagram with transformer, (c) HB-SM, and (d) FB-SM.

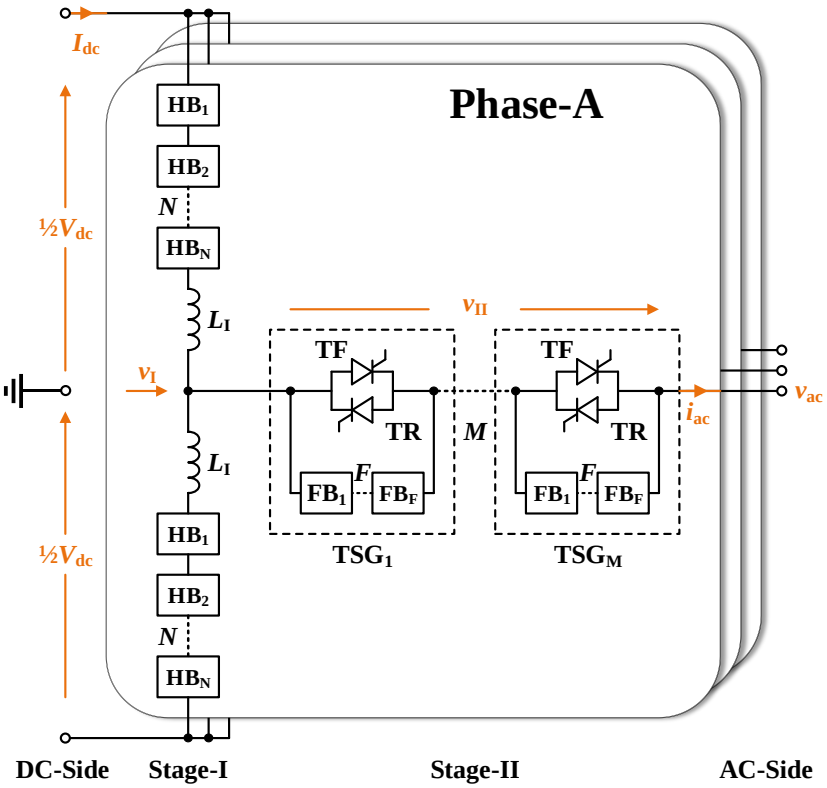
In terms of functionality, as the topology has more degrees of freedom due to the added stage, the T-MMC has more operation modes. Assuming Stage-I HB-SMs and Stage-II FB-SMs have the same rated voltage, the number of IGBTs employed for active power conversion in the proposed structure is equal to a FB-MMC, provided both systems operate with identical rated ac and dc voltages. But the proposed structure of separating the capacitors from HB-MMC adds features, such as easier voltage levelling and independent operation of stages I and II. However, the conduction losses of the overall converter are relatively high because the Stage-II FB-SMs introduce a large number of semiconductor switches into the main conduction path. To resolve the reduced-efficiency issue of the T-MMC basic topology, practically acceptable

topologies are presented. Two bypassing mechanisms, using thyristors and disconnectors respectively, are proposed.

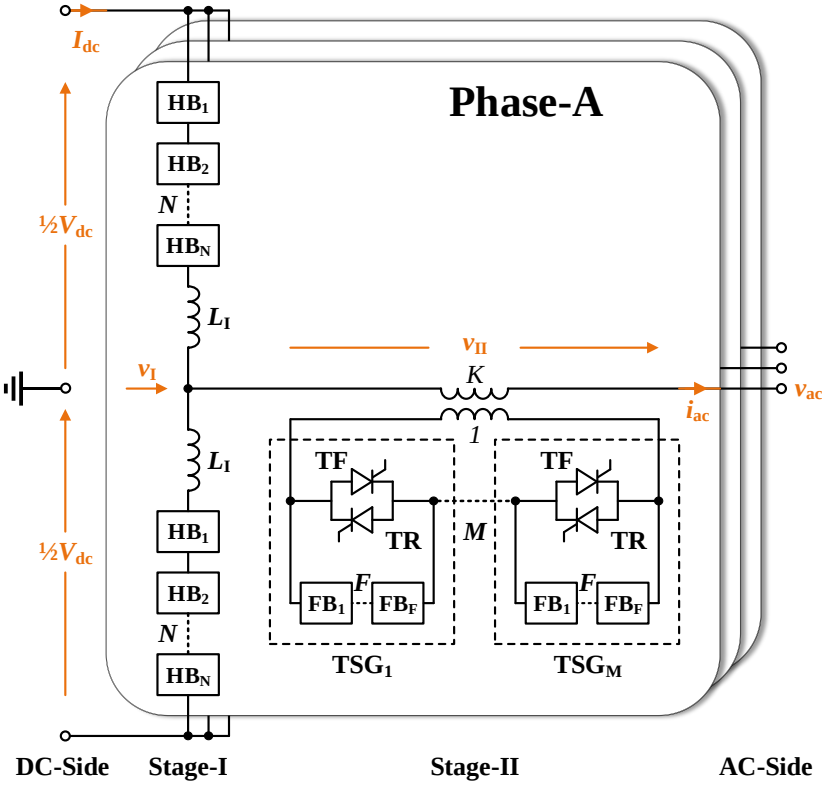
3.1.2 The TSG-Based T-MMC Topology

In the first T-MMC variant, the ac-side power interface (Stage-II) is one arm composed of *M* thyristor-SM groups (TSGs). As shown in Fig. 3-2(a), within one TSG, a pair of antiparallel-connected symmetric (reverse blocking) thyristors (TF//TR) and *F* series-connected FB-SMs form two parallel current paths, both of which are suitable for ac/bidirectional current flow. Also, the number of FB-SM N' equals $M \times F$, for consistency.

From the topology feature perspective, the TSG-based T-MMC is a VSC with modularity and scalability. Within each stage, equal voltage distribution can be achieved between IGBTs and thyristors respectively, as long as HB and FB SM capacitor voltages are maintained balanced. The shunt TF//TRs of Stage-II are on during normal operation; thus, taking advantage of thyristor features (high voltage and power capabilities), minimal voltage drop and low conduction loss are incurred by Stage-II. The proposed TSG can also ensure thyristor-commutation, which will be presented later.



(a)

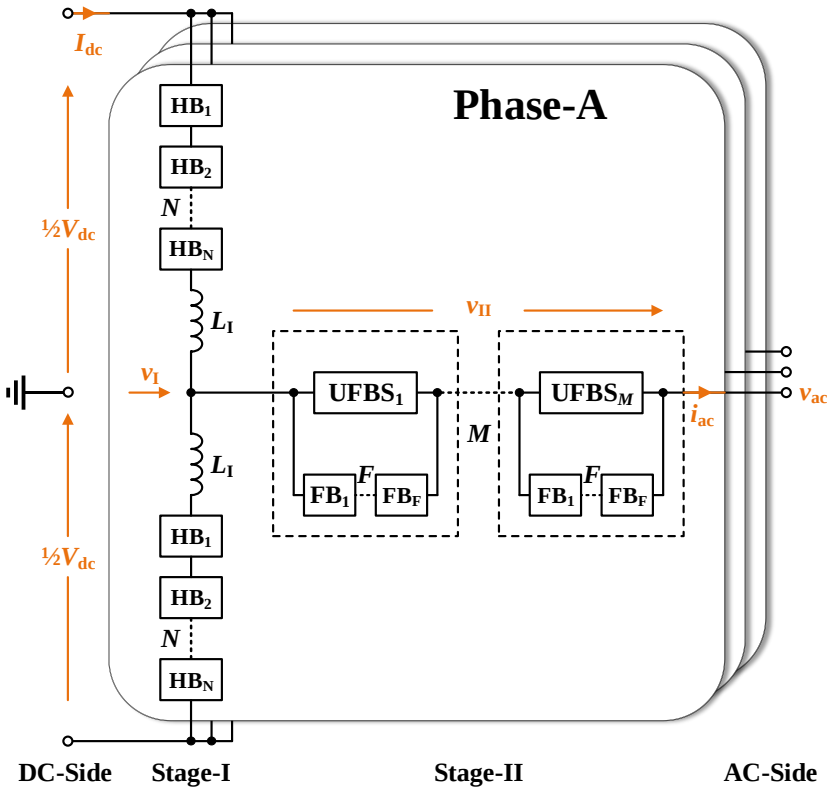


(b)

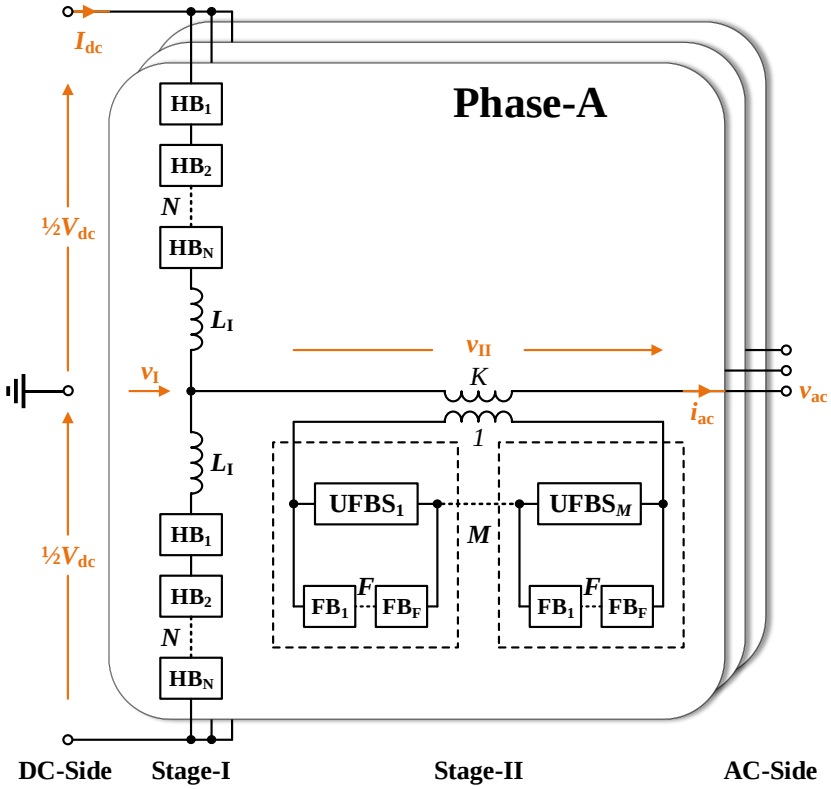
Fig. 3-2. The thyristor-based practical T-MMC circuit configurations: (a) Topology diagram, and (b) Isolated variant.

3.1.3 The USG-Based T-MMC Topology

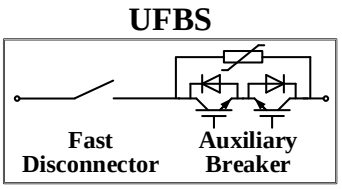
Another practical T-MMC type uses a specific circuit breaker, namely, the ultra-fast bypass switch (UFBS), as shown in Fig. 3-3, where the ac-side power interface (Stage-II) is one arm composed of *M* UFBS-SM groups (USGs). Within one USG, a parallel-connected UFBS and *F* series-connected FB-SMs form two parallel current paths, both of which are designed for bidirectional current flow. The on-demand ESS is divided into *M* modular units for faster activation and deactivation times (inserting and bypassing) of the FB-SMs.



(a)



(b)



(c)

Fig. 3-3. The circuit breaker based practical T-MMC circuit configurations: (a) topology diagram, (b) isolated variant, and (c) UFBS.

Such modular topological connection is beneficial for UFBSs voltage balancing. As a result, each phase of the on-demand ESS resembles a hybrid dc circuit breaker [1], [2]. The difference is that the circuit breakers of the T-MMC operate in the ac side. During normal operation, the FB-SMs can be bypassed by the UFBSs, thus avoiding semiconductor switching and conduction losses. With the reduced resistance and on-state voltage drop in the bypass path (mechanical disconnectors, a few IGBTs, and the transformer for the isolated variant, if configured), the efficiency of the circuit breaker based practical T-MMC is marginally different from that of a conventional HB-MMC.

3.2 T-MMC Design Principles and Operation Modes

Like a conventional HB-MMC, the HB-SM voltage rating of Stage-I is V_{dc}/N, and Stage-I can synthesize a sinusoidal voltage $v_I = V_I \sin(\omega t+\varphi_I)$. Assuming all Stage-II thyristors/UFBSs are off, and FB-SM capacitor voltages are equal and constant, Stage-II is able to synthesize a sinusoidal voltage $v_{II} = V_{II} \sin(\omega t+\varphi_{II})$. Then the voltage ratings of the TF//TRs and FB-SMs, namely, V_T and V_{FB}, are V_{II}/M and $V_{II}/(M\times F)$, respectively.

Galvanic isolated topology variants are shown in Fig. 3-2(b) and Fig. 3-3(b), where the TSG/USG voltage levels can also be flexibly changed by the transformer turns ratio K. Accordingly, V_T and V_{FB} are $V_{II}/(M\times K)$ and $V_{II}/(M\times F\times K)$, respectively. The transformer bandwidth must be commensurate with the highest frequency of the required compensating harmonics.

To be able to achieve the desired functions regarding voltage synthesis, fault isolation, etc., the Stage-II is sized such that its maximum attainable ac voltage is the same as that of the Stage-I. Also, with appropriate modulation methods, the following voltage expression holds:

$$v_I + v_{II} = v_{ac} \tag{3.1}$$

where v_I, v_{II} and v_{ac} are the synthesized voltages of Stage-I, Stage-II, and the overall converter, respectively.

The T-MMC can be applied in various power system and motor drive scenarios. In generic grid-connected applications, the T-MMC ac-side terminal is connected to the ac grid point of common coupling (PCC) through a grid-interfacing transformer, as shown in Fig. 3-4(a), where T-MMC is employed as a bidirectional ac/dc converter station. Thus, the T-MMC can be modelled as series-connected ac voltage sources, as shown for one phase in Fig. 3-4(b), where L and R represent the ac bus impedance. Different operational modes can be achieved by manipulating the two stages.

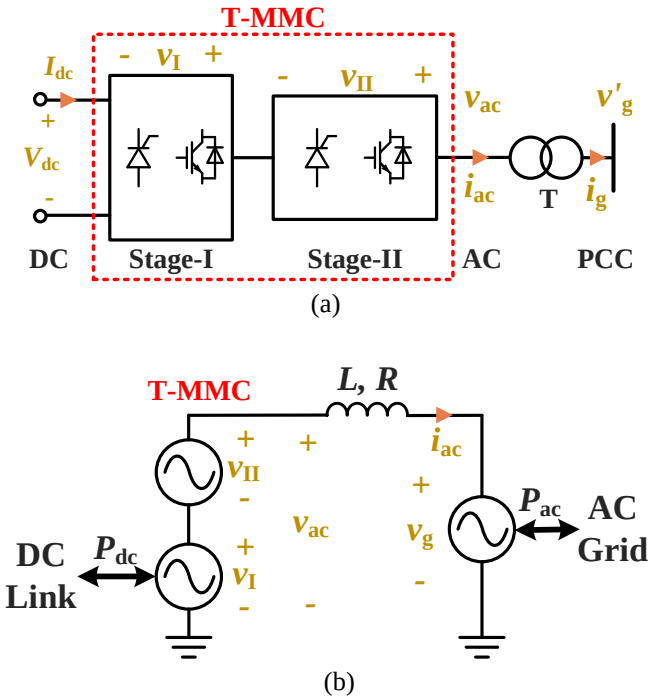


Fig. 3-4. T-MMC in grid-connected applications: (a) schematics and (b) simplified model.

Also, for the isolated versions, the galvanic isolated transformer can be used to reduce the insulation level and to establish bespoke trade-offs between FB-SM voltage and current ratings when compact design is not a priority. The additional leakage reactance introduced by the transformer impacts system performance, therefore, must be considered when designing the control system.

In general, for the given ac network impedances L and R, the active and reactive powers of the station ac grid (P_g and Q_g) are controlled through the ac grid current, which can be regulated by modifying the phase and magnitude of the station output ac voltage v_{ac} based on:

$$v_{ac} + L\frac{di_{ac}}{dt} + Ri_{ac} = v_g \tag{3.2}$$

where i_{ac} is the converter side ac current.

Considering the Stage-I HB-MMC internal model, the overall equivalent circuit of the proposed station converter structure is shown in Fig. 3-5, where L' and R' are the leakage inductance and resistance of the interfacing transformer (plus the series

transformer, if configured) respectively and v_g' is the PCC ac voltage referred through the grid-interfacing transformer.

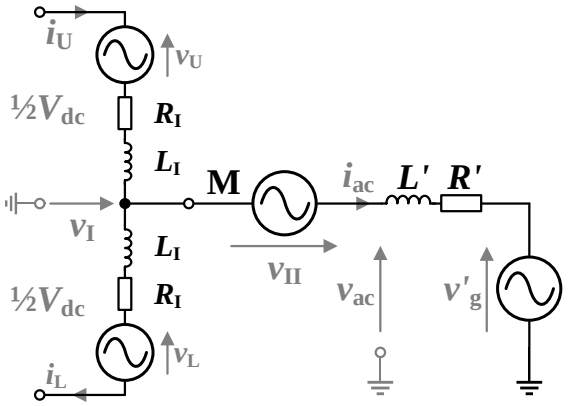


Fig. 3-5. T-MMC analytical model (including stages I and II) in grid-connected applications.

According to Fig. 3-5, the ac and dc circuit loops of one phase-leg of the HB-MMC have the following relationships:

$$\frac{L'}{2}\frac{di_{ac}}{dt}+\frac{R'}{2}i_{ac}+v_I=\frac{(v_L-v_U)}{2} \tag{3.3}$$

$$2L_I\frac{di_{CM}}{dt}+2R_Ii_{CM}=V_{dc}-(v_U+v_L) \tag{3.4}$$

where, as usual, $i_{ac} = i_U - i_L$, $i_{CM} = ½(i_U + i_L)$ and i_{CM} is the common-mode current of one phase-leg.

The dual-stage structure of the T-MMC provides operation flexibility. By manipulating the major parts of stages I and II, different operation modes can be achieved; therefore, different operational functions can be obtained, including normal efficient operation, faults isolation, and other supportive functions.

Fig. 3-6 illustrates conceptual waveforms of the four fundamental modes (modes 1 to 4) of the T-MMC (one phase) under network normal and fault conditions.

- *Mode 1:* By operating Stage-I as a conventional HB-MMC, and with bypass paths (either thyristors or UFBSs) on, the T-MMC functions in the 'normal' mode (mode 1). As shown in Fig. 3-6(a), Stage-I is responsible for generating the ac-side voltage required by the grid-connected controllers. To avoid short

circuit, the FB-SMs of Stage-II are not allowed to actively generate voltages in this mode. The conducting capability of thyristors/UFBSs compared to that of IGBTs minimizes Stage-II losses. Accordingly, T-MMC affords similar operation efficiency to a conventional HB MMC (Stage-I). The voltage drop across Stage-II is neglected in the conceptual waveforms in Fig. 3-6(a). Also, the converter equivalent circuit during normal operation reveals that for the HB-MMC ac loop model, $R = ½R_I + R'$ and $L = ½L_I + L'$.

- *Mode 2:* Because of the extra ac voltage offered by the series-connected Stage-II, simultaneous operation of the stages can increase the maximum ac voltage that the converter station can generate, which is attractive for the host ac grid. Thus, when the reactive power (voltage) support is needed by the ac grid, T-MMC is able to increase the ac-side voltage amplitude, thereby avoiding Stage-I over-modulation. T-MMC behaviour during ac-side *Q* support is illustrated in Fig. 3-6(b), where both stages contribute to generating the ac-side voltage v_{ac} (the vector sum). As PCC active power is still provided by Stage-I, the dc-side power remains at 1pu. In this mode, all Stage-II bypass paths must be off so that the FB-SM string of Stage-II acts as a series-connected cascaded H-bridge STATCOM. Theoretically, the operation of the two stages is not independent; therefore Stage-II voltage and current vectors are controlled to be orthogonal for steady-state energy balance.
- *Mode 3:* AC fault ride-through techniques with VSCs have been extensively investigated. When a worst-case solid ac-side fault occurs, T-MMC Stage-I reduces its ac output voltage to limit the fault current, similar to the behaviour of a conventional HB MMC. Illustrative waveforms are shown in Fig. 3-6(c), where Stage-I controls reactive current and Stage-II is bypassed (v_{II} is assumed to be zero). In terms of a three-phase system, negative sequence current elimination is also feasible in asymmetrical ac fault cases.
- *Mode 4:* Fig. 3-6(d) illustrates T-MMC dc fault isolation capability under the worst dc-side fault condition. Stage-I upper and lower arms are bypassed; thus v_I is negligible. With the same voltage rating as Stage-I, Stage-II can safely isolate the dc and ac sides by the FB-SM string barrier (all thyristors

and IGBTs are off). Then no ac-side current can sink into the dc side. Stage-II can also operate as a STATCOM to provide supportive *Q* for the tied grid.

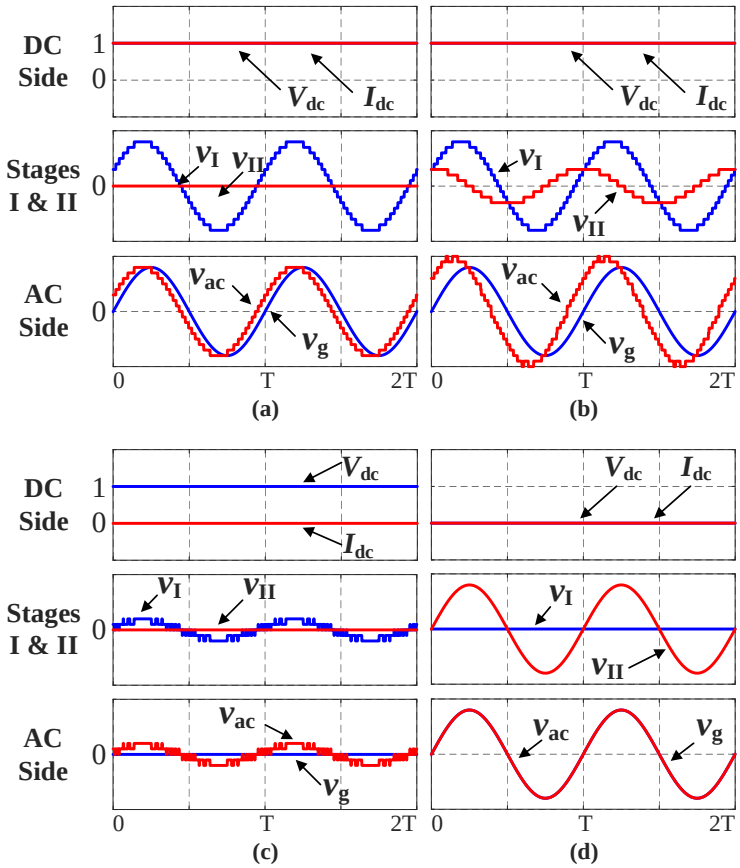


Fig. 3-6. T-MMC conceptual waveforms (in pu) in normal and faulty network cases: (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

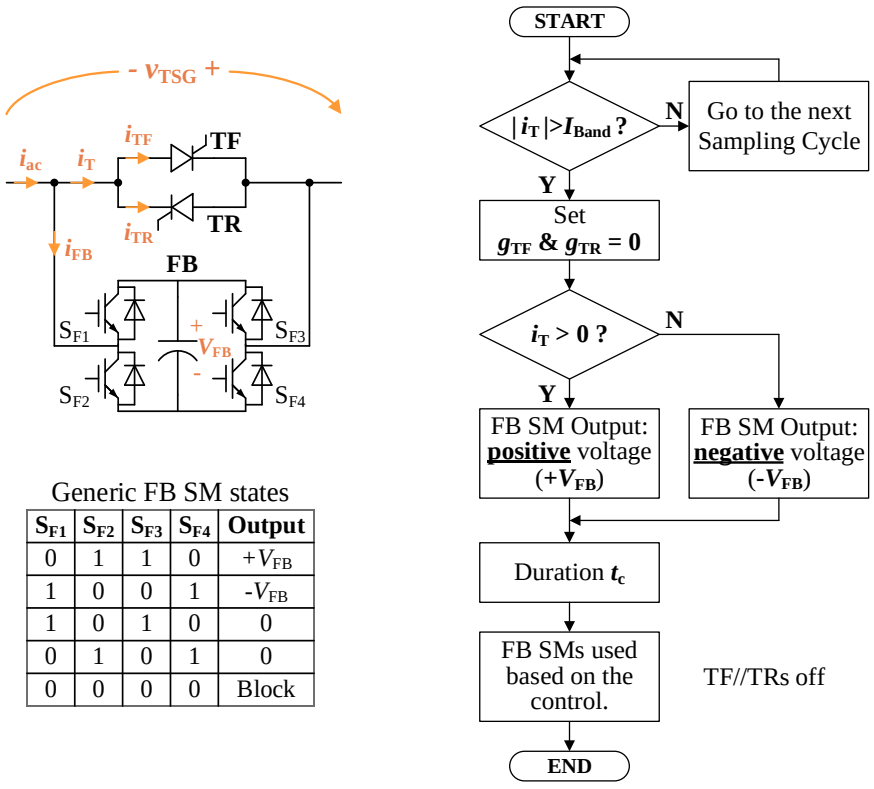
3.3 TSGs and USGs

Greatly reducing the conduction losses during the normal operation, TSGs and UFBSs are critically important for the thyristor and circuit breaker based T-MMCs, respectively.

For the thyristor-based T-MMC, various natural and forced commutation methods exist to turn off thyristors, and here the parallel voltage forced-commutation is implemented within each TSG, where the FB-SMs can be configured as parallel commutating voltage sources [3].

An illustrative TSG schematic with one FB-SM (F = 1) is depicted in Fig. 3-7(a). Thyristor forced-commutation is achieved by the manipulation of the FB-SM and thyristors, as in the procedure shown in Fig. 3-7(b).

The essential condition is a reverse voltage applied to the on-state thyristor. By providing the FB-SM path with lower impedance (a parallel voltage), the ac current is transferred from the thyristor path to the FB-SM path. Given a thyristor turn-off time t_q, a parallel voltage duration t_c longer than t_q is required. Practically, to avoid incorrect detection of the ac current zero-crossing point, a dead-band (I_{Band}, larger than the current measurement tolerance) is used.



Generic FB SM states

S_{F1}	S_{F2}	S_{F3}	S_{F4}	Output
0	1	1	0	$+V_{FB}$
1	0	0	1	$-V_{FB}$
1	0	1	0	0
0	1	0	1	0
0	0	0	0	Block

(a) **(b)**

Fig. 3-7. TSG-commutation illustration: (a) schematics of the TSG (F = 1) and generic FB-SM states and (b) forced-commutation procedure flow chart.

Forced-commutation process waveforms are illustrated in Fig. 3-8, where the duration t_c is exaggerated for illustration, and g_{TF} and g_{TR} are the triggering signals of TF and TR respectively. Enabled g_{TF} and g_{TR} indicate that the gate drivers are turned on to provide gate currents, whereas disabled g_{TF} and g_{TR} indicate zero gate current.

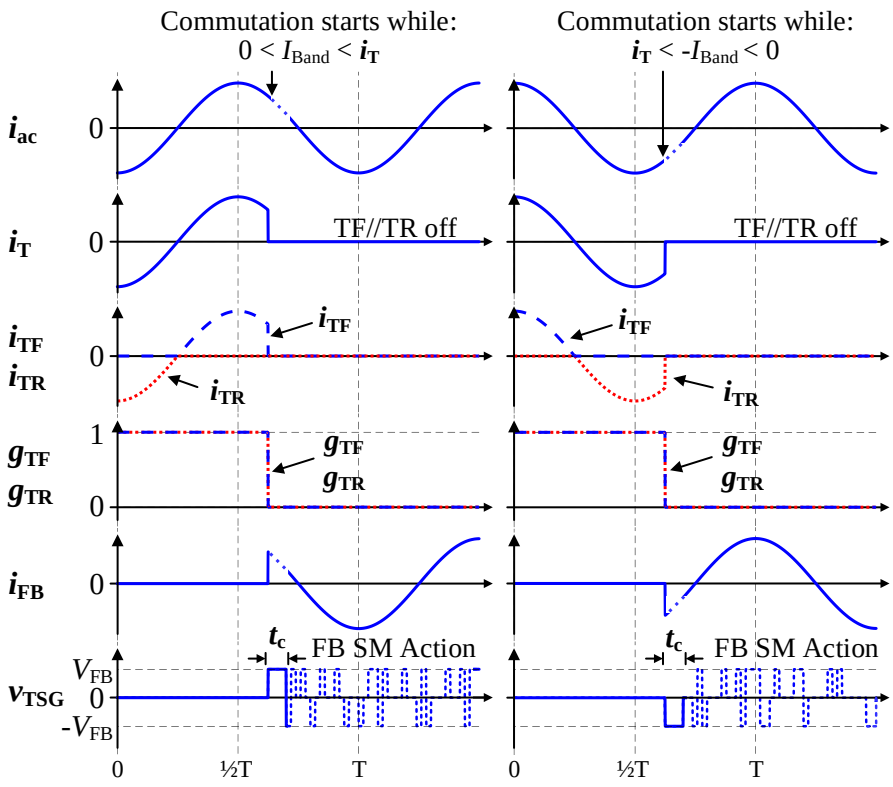


Fig. 3-8. Descriptive waveforms (in pu) of the thyristor-commutation process.

As the FB-SM capacitor is discharging during the interval t_c, with ideal switches (zero conduction and switching losses), the capacitor voltage variation is:

$$C_{FB} \times \Delta V_{FB} = \int_{t}^{t+t_c} i_{ac}(t)dt \tag{3.5}$$

where ΔV_{FB} is the capacitor voltage variation due to the commutation process and $i_{ac}(t)$ is the instantaneous ac current.

Available high-power converter grade thyristors have significant re-applied *dv*/*dt* capabilities (kV/μs), and maintaining circuit parameters under limits is not difficult. Additionally, RCD snubber circuits can be used to avoid the erroneous thyristor reactivation caused by the *dv*/*dt*. Using partial SMs or a specific SM within a TSG for commutation is also feasible. Thyristors have high turn-on and on-state *di*/*dt* ratings (kA/μs), which are sufficient for dynamic performance.

For the generic grid-connected scenario in Fig. 3-4, the instantaneous *di*/*dt* of the turned-on thyristors within Stage-II is:

$$\frac{di}{dt} = \frac{v_{\mathrm{I}} - Ri_{\mathrm{ac}} - v_{\mathrm{g}}}{L} \tag{3.6}$$

During commutation, the ac current is temporarily not controlled, with a maximum possible deviation of:

$$\left|\Delta I_{\mathrm{ac}}\right|_{\max} = t_{\mathrm{c}} \frac{V_{\mathrm{II}} + RI_{\mathrm{ac}}}{L} \tag{3.7}$$

where I_{ac} is the ac current magnitude. Fortunately, the current control variable trajectory is only slightly influenced due to the short duration t_{c} and inductive impedance of the ac bus (in both the internal arms and external load).

For the USG-based T-MMC, the previously mentioned bypassing mechanism (using UFBSs) is incorporated into the Stage-II as well, to reduce the continuous operational losses. Thus, within each USG, the commutation process would occur between the FB-SM string and the UFBS. Successful current commutation from the UFBS path to the FB-SM path is critical for activation of the Stage-II FB-SM based converter. For generic sake, the opening duration of the UFBS (which is highly depending on the mechanical characteristics of the disconnector,) is t_{o}.

An illustrative USG schematic with one FB-SM (F = 1) is depicted in Fig. 3-9(a). Commutation is achieved by the manipulation of the FB-SM and UFBS, with the forced-commutation procedure shown in Fig. 3-9(b).

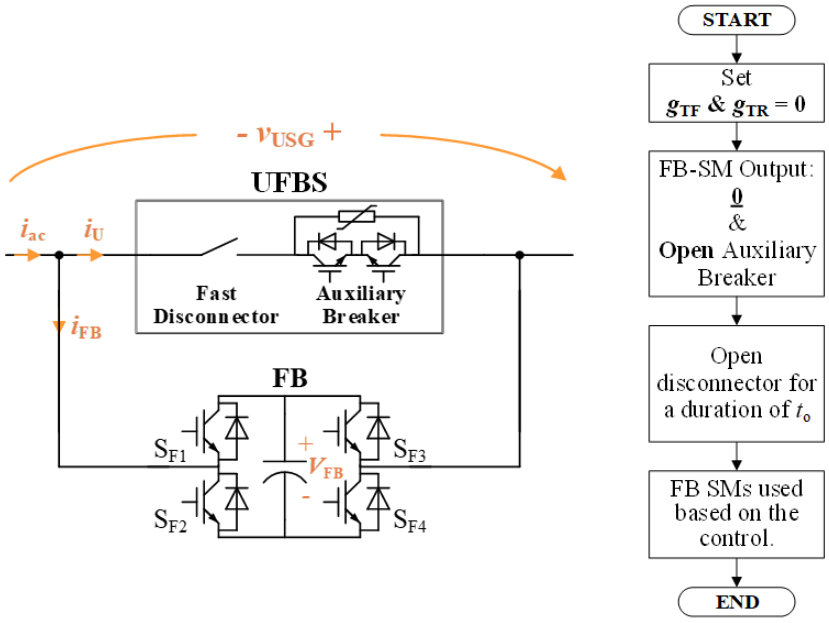


Fig. 3-9. USG-commutation illustration: (a) schematics of the USG (F = 1) and generic FB-SM states and (b) forced-commutation procedure flow chart.

Fig. 3-10 shows T-MMC status for each of the four modes. AC-side reactive power support and dc fault isolation rely on active operation of Stage-II, and their transitions involve prompt commutation of the TSGs/USGs.

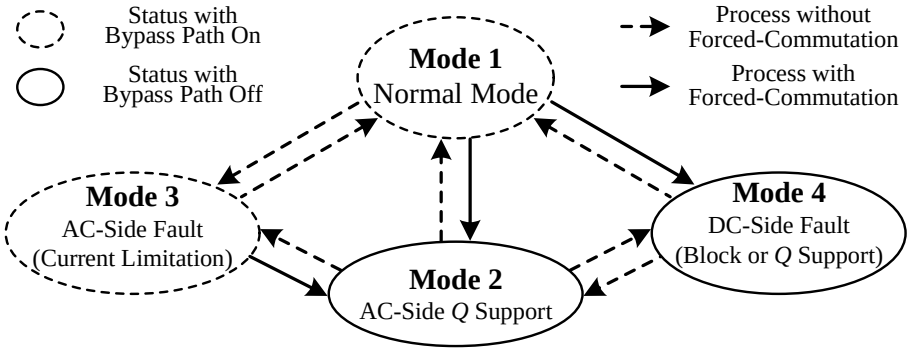


Fig. 3-10. T-MMC status diagram of fundamental modes.

3.4 Control System

Due to T-MMC topology complexity, a hierarchical control system is suggested, including output control (for dc and/or ac sides), stage-level control, and inner-stage control. The inner-stage control for Stage-I includes MMC circulating current control and leg, arm and SM level control, whereas Stage-II internal control involves phase and SM level control.

A typical control diagram for a grid-connection application is shown in Fig. 3-11, where the output controllers, ac-side controllers, stage internal controller, and modulation process are the major parts to generate the semiconductor gate signals. Usually, the output controllers control the ac grid active and reactive powers (extra dc-side voltage control loop is based on the active power regulation). Various VSC grid-forming or grid-following control schemes are applicable for different scenarios due to the VSC nature of the T-MMC. The three-phase output voltage reference v_{ac}^* is obtained finally [4], [5].

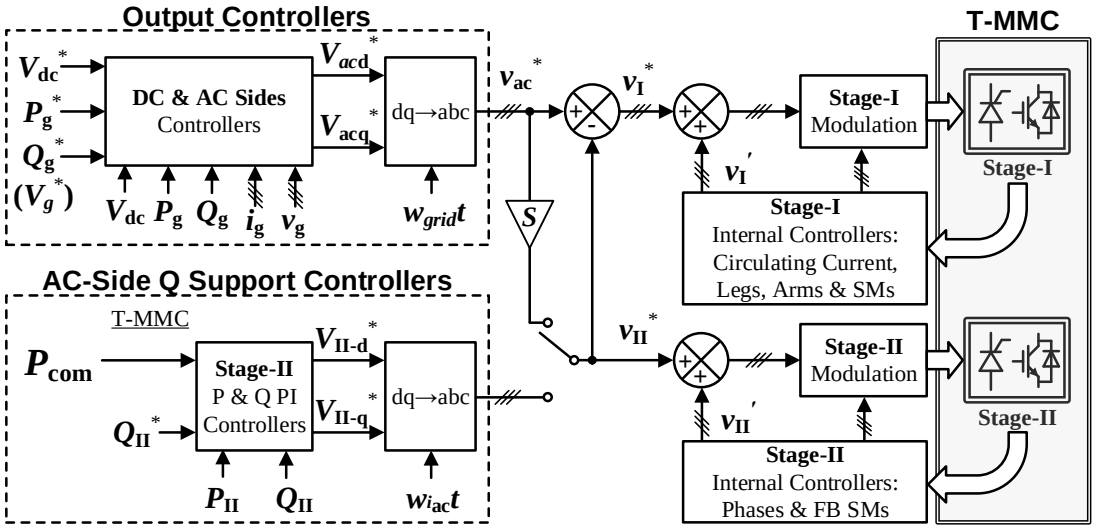


Fig. 3-11. Overall control diagram of the T-MMC for a grid-connected application.

Stage-level control coordinates the operation of the two stages, and therefore takes responsibility to tackle abnormal cases. In Fig. 3-11, variable *S* is assigned to be '0' (no dc fault) or '1' (dc pole-to-pole fault), reflecting the dc network health status. Further functions, including pole-to-ground fault detection or power-sharing between stages, are also feasible. Normally, Stage-I ac voltage reference v_I^* equals v_{ac}^*, whereas that of the Stage-II, v_{II}^*, is zero (hardware-wise, bypass path are turned on), indicating the normal mode. In general, when a dc fault occurs (S = 1), Stage-II can either block the dc/ac sides or generate the ac voltage (using v_{ac}^*) under regulation of the ac-side output controllers. As the ESEs are integrated into Stage-II, ac grid active power can be maintained. The ac-side *Q* support controllers are enabled and selected when ac-side support (including energy compensation and ancillary services) is required. As shown in Fig. 3-11, Q_{II}^* can be used to make Stage-II contribute to voltage support,

whereas P_{com} (to compensate power losses) is for Stage-II average capacitor voltage control.

Fig. 3-12 shows the Stage-II average capacitor voltage controller, which is used to adjust the average voltage of the FB-SM capacitors. The average voltage of all the capacitors is calculated and compared with the reference set, which is usually the rated value, and a PI controller is used to regulate absorbed power of the Stage-II. With the active power being regulated, stored energy within Stage-II capacitors is controlled.

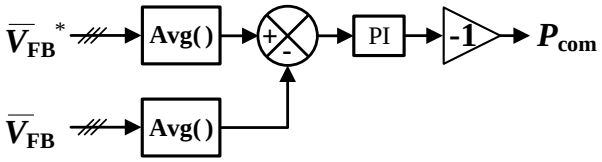


Fig. 3-12. Average capacitor voltage controller for Stage-II.

An inter-phase voltage balancing controller is shown in Fig. 3-13, where notch filters are adopted to suppress potential second-order harmonics without delay, and fundamental frequency voltage injection ensures active power (voltage) regulation.

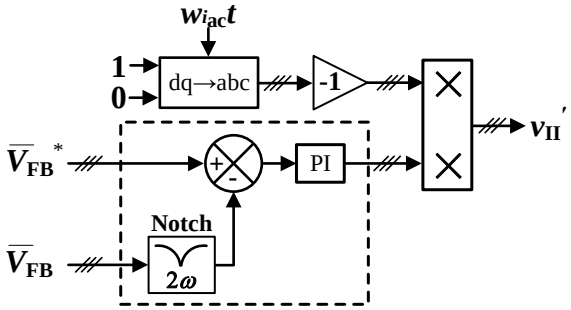


Fig. 3-13. Capacitor voltage balancing controller for Stage-II.

Modulation methods for modular multilevel converters have been extensively investigated in the literature. Briefly, the modulation methods for Stage-I are the same as those for the HB-MMC, whereas the modulation methods for Stage-II can be inherited from techniques for cascaded H-bridge (CHB) converter.

3.5 Converter Characteristics

Generally, as a bidirectional voltage source converter, the T-MMC can be used in a variety of ac/dc conversion applications. Due to the inherent scalability of both stages,

suitable voltage/power levels can range from low to high, whereas the current ratings are mainly dependent on semiconductors. On the other hand, as a member of the MMC family, the T-MMC inherits many other merits, including modularity, high-quality output (ac and dc side) waveforms, and internal submodule fault tolerance [6]-[8].

In particular, the T-MMC is more suitable and applicable in the applications where both reliability and efficiency are highly sought, such as medium and high voltage systems with bulk power conversion. With respect to other conventional topologies, although operation efficiency is high, the HB-MMC has difficulties in tolerating dc-side faults. In contrast, mixed-cell and FB-MMCs can achieve both ac and dc fault protection, but the conduction losses increase due to more semiconductors in the main conduction path. Thus, in these applications, there is a challenging design trade-off between larger output voltage ranges (related to the ac and dc side conditions) and lower semiconductor losses for the conventional topologies. The proposed approach establishes a feasible methodology to avoid the apparently unavoidable trade-off, achieving high fault resiliency and operation efficiency simultaneously.

A comparative table of different typical MMCs (including HB-MMC, mixed-cell MMCs and FB-MMC) is given in Table 3-1 considering semiconductor usage, quantitative losses, critical features, etc.

Table 3-1. A quantitative comparison of various typical MMCs.

	HB MMC	Mixed-Cell MMC (HB:FB = 1:1)	Mixed-Cell MMC (HB:FB = 1:2)	FB MMC	**T-MMC (TSG-Based)**
DC voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
SM No. per phase	$2N$	$2N$	$2N$	$2N$	$2N$ (Stage-I); MF (Stage-II)
SM rated voltage	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N	V_{dc}/N (Stage-I); $½V_{dc}/(MF)$ (Stage-II) [1]
IGBT/ Diode No. per phase	$4N$	$6N$	$20N/3$	$8N$	$8N$ (if $MF = N$) [2]
Thyristor No. per phase for current conduction	-	-	-	-	$2M$
IGBT/Diode No. in current path	$2N$	$3N$	$10N/3$	$4N$	$2N$
Thyristor No. in ac current path	0	0	0	0	M
Maximum converter ac voltage	$½V_{dc}$	$½V_{dc}$ [3]	$½V_{dc}$ [3]	$½V_{dc}$ [3]	V_{dc} [4]
DC fault isolation	No	Yes	Yes	Yes	Yes
AC-Side Q-support during dc fault	No	Yes	Yes	Yes	Yes

[1]: Assuming $V_I = V_{II}$; thus, ac voltage synthesis and Stage-II ESE integration becomes more flexible.
[2]: Assuming $V_I = V_{II}$ and $MF = N$.
[3]: More SMs are required for a higher ac voltage.
[4]: Assuming $V_I = V_{II}$. This is achieved by operating stages I and II simultaneously.

3.6 Simulation

In order to verify the proposed topologies and approaches, a typical grid-connection application scenario is configured and the T-MMC model is simulated as shown in this section. The typical illustration with the ac and dc links in this section is to show the main operating modes and features of the T-MMC, especially the double-side fault tolerant capability, in a straightforward manner.

A T-MMC, with its dc side connected to a voltage-controlled dc link through a short cable and its ac side connected to a stiff ac grid through a Δ-Y interfacing transformer, is simulated using MATLAB/Simulink, with parameters listed in Table 3-2. Both TSG and USG based T-MMCs are studied.

Table 3-2. Simulation parameters.

	Parameters	**Rating**
DC side	DC-link voltage	40kV
	DC cable distance	10km
	DC cable (T-model) inductance	150uH/km
	DC cable (T-model) resistance	11mΩ/km
	DC cable (T-model) capacitance	200nF/km
AC side	AC grid frequency	50Hz
	AC grid voltage	33kV
	Transformer ratio	20/33kV
	Transformer leakage inductance	0.18pu
Stage-I	HB-SM number per arm N	20
	HB-SM rated voltage	2kV
	HB-SM capacitance C_{HB}	6.7mF
	Arm inductance L_I	0.2pu
Stage-II	TSG/USG number per phase M	10
	FB-SM number per TSG/USG F	4
	FB-SM rated voltage	0.55kV
	Commutation time for TSGs (t_q = 500us)	700us
	Commutation time for USGs (t_o = 2ms)	2ms
	FB-SM capacitance C_{FB}	18mF

A conventional grid-connected control structure, with inner vector current loops, outer *P*-*Q* loops and PLL, is adopted. In the normal case, the Stage-I is controlled to inject 40MW active power into the PCC at unity power factor, and Stage-II bypass paths (either TSGs or USGs) are on. In this section, T-MMC performance for ac-side reactive power support and dc fault ride-through are presented.

3.6.1 AC-Grid Support Case

Fig. 3-14-I to IV show TSG-based T-MMC ac-grid support performance. Fig. 3-14-I shows the performance on dc and ac sides. After thyristor-commutation at t = 0.7s, the output and activated ac-side Q support controllers of the T-MMC operate together from 0.72s, and the PCC reactive power ramps up to 48MVAr approximately, as shown in Fig. 3-14-I(e). With a constant PCC voltage, the three-phase currents are increased due to the increased Q, whereas the dc and active powers are slightly influenced, as shown in Fig. 3-14-II(a)-(e). The voltage contribution of each stage is shown in Fig. 3-14-II(b) and (c), whereas Stage-II increases ac voltage synthesis while

Stage-I maintains the original ac-side voltage amplitude (without over-modulation). Also, both stages contribute to reactive power support of the ac-side, as shown in Fig. 3-14-II(d) and (e). Stage-I arm currents and HB-SM voltage ripple increase, as displayed in Fig. 3-14-III(a) and (b). Also, Stage-II capacitor voltages are controlled and balanced, as shown in Fig. 3-14-III(c)-(e). The fluctuation of the active power of stages is due to the regulation of Stage-II capacitor voltages. As shown in Fig. 3-14-IV(a)-(e), Stage-II ac current is commutated from the thyristor paths to the FB-SM paths after 0.7s (700μs thyristor commutation duration is required). Due to thyristor forced-commutation, the ac current is temporarily uncontrolled, with a small deviation; see Fig. 3-14-IV(c)-(e).

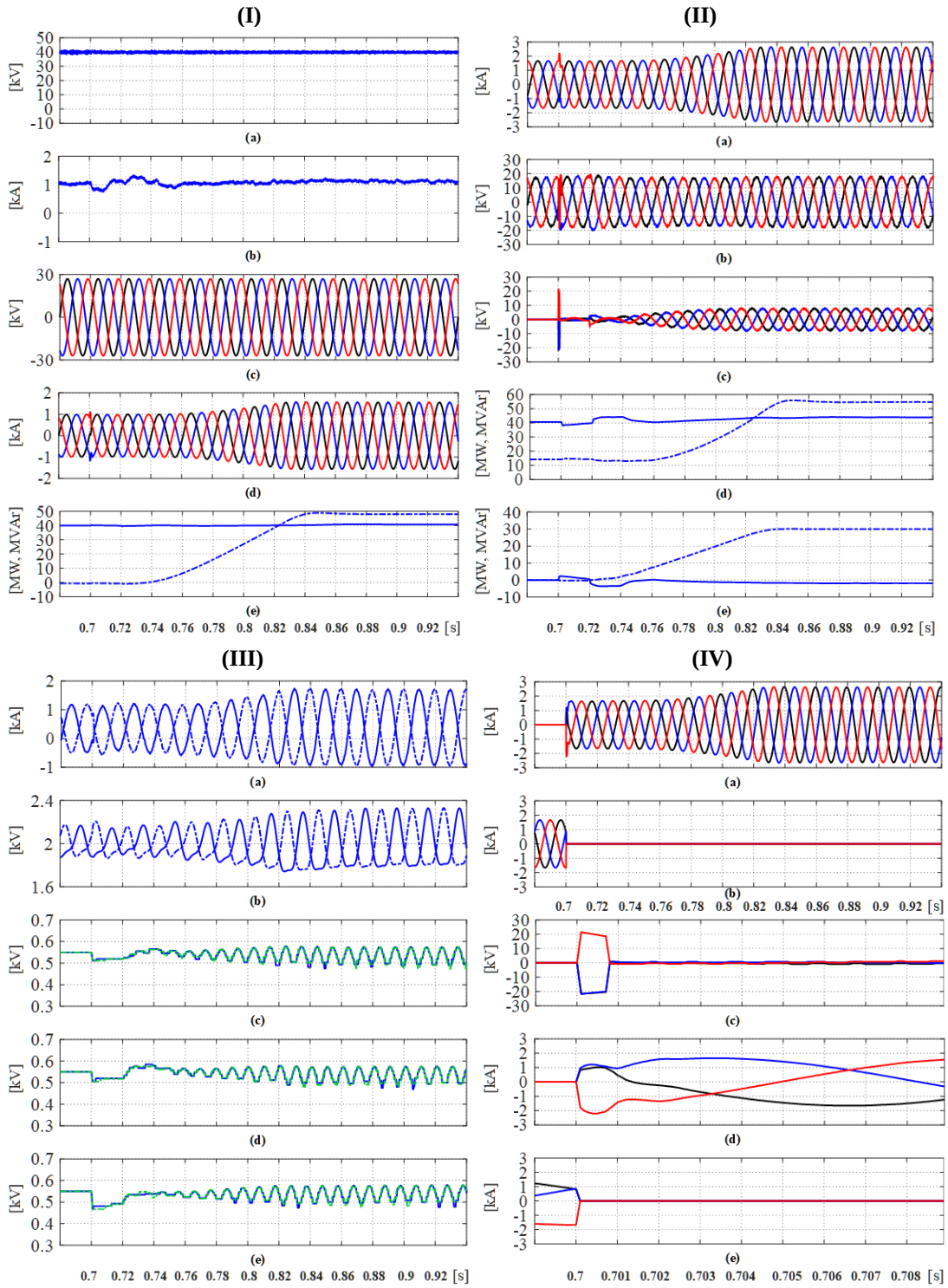


Fig. 3-14. TSG-based T-MMC waveforms in ac-grid support case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

Fig. 3-15-I to IV show ac-grid support performance of the USG-based T-MMC. Fig. 3-15-I shows performance on the dc and ac sides. After UFBS-commutation at 0.7s, the output and activated ac-side *Q* support controllers of the T-MMC operate together from 0.72s, and the PCC reactive power ramps up to 48MVAr approximately, as shown in Fig. 3-15-I(e). With a constant PCC voltage, the three-phase currents are increased due to the increased *Q*, whereas the dc and active powers are slightly influenced, as shown in Fig. 3-15-II(a)-(e). The voltage contribution of each stage is shown in Fig. 3-15-II(b) and (c), where Stage-II increases ac voltage synthesis while Stage-I maintains the original ac-side voltage amplitude (without over-modulation). Both stages contribute to reactive power support for the ac-side, as shown in Fig. 3-15-II(d) and (e). Stage-I arm currents and HB-SM voltage ripple increase, as displayed in Fig. 3-15-III(a) and (b). Also, Stage-II capacitor voltages are controlled and balanced, as shown in Fig. 3-15-III(c)-(e). As shown in Fig. 3-15-IV(a)-(e), Stage-II ac current is commutated from the UFBS paths to the FB-SM paths after 0.7s.

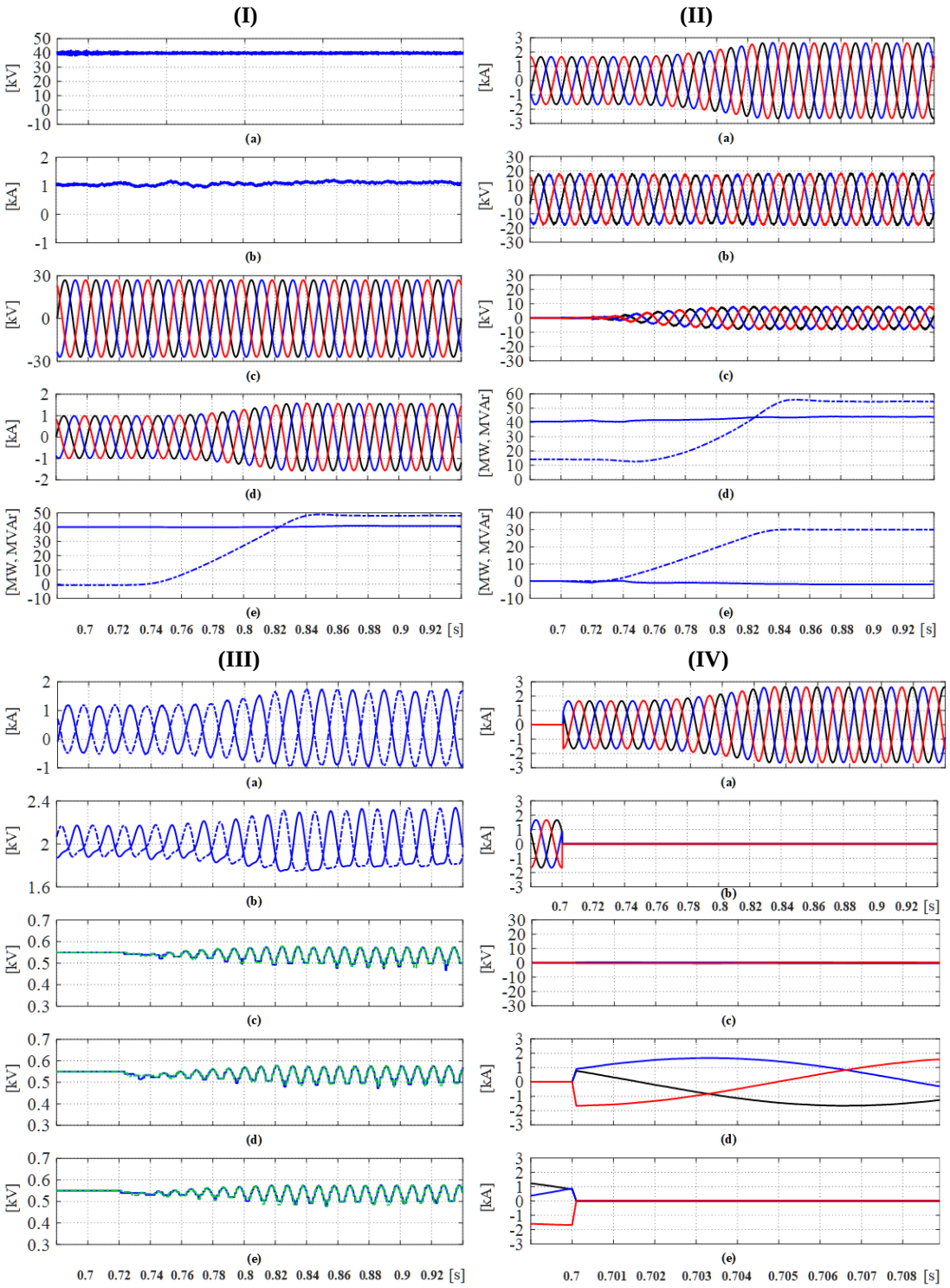


Fig. 3-15. USG-based T-MMC waveforms in ac-grid support case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

3.6.2 DC Fault Blocking Case

Simulation results in Fig. 3-16-I to IV show the dc fault blocking capability of TSG-based T-MMC. A pole-to-pole solid short-circuit dc fault is applied at 0.7s and cleared after 140ms, whence the voltage and current of T-MMC dc-side terminal fall to zero, as depicted in Fig. 3-16-I(a) and (b). Also, PCC voltage is in the normal case, whereas the PCC current is blocked, see Fig. 3-16-I(b) to (d). During the dc fault, Stage-II blocks the fault. Thus, with the assistance of T-MMC Stage-II, inrush current from the ac side into dc side is prevented, and the ac-side voltage stress transfers to Stage-II, see Fig. 3-16-II(a)-(e). Fig. 3-16-III shows selected internal variables of the stages during the fault. Stage-I SMs are blocked, as shown in Fig. 3-16-III(a) and (b), and Stage-II SMs are blocked, as shown in Fig. 3-16-III(c)-(e). Fig. 3-16-IV depicts the thyristor-commutation process (700μs thyristor commutation duration is required). After 0.7s, thyristor and FB-SM paths of Stage-II are turned-off and blocked respectively, see Fig. 3-16-IV (c) to (e).

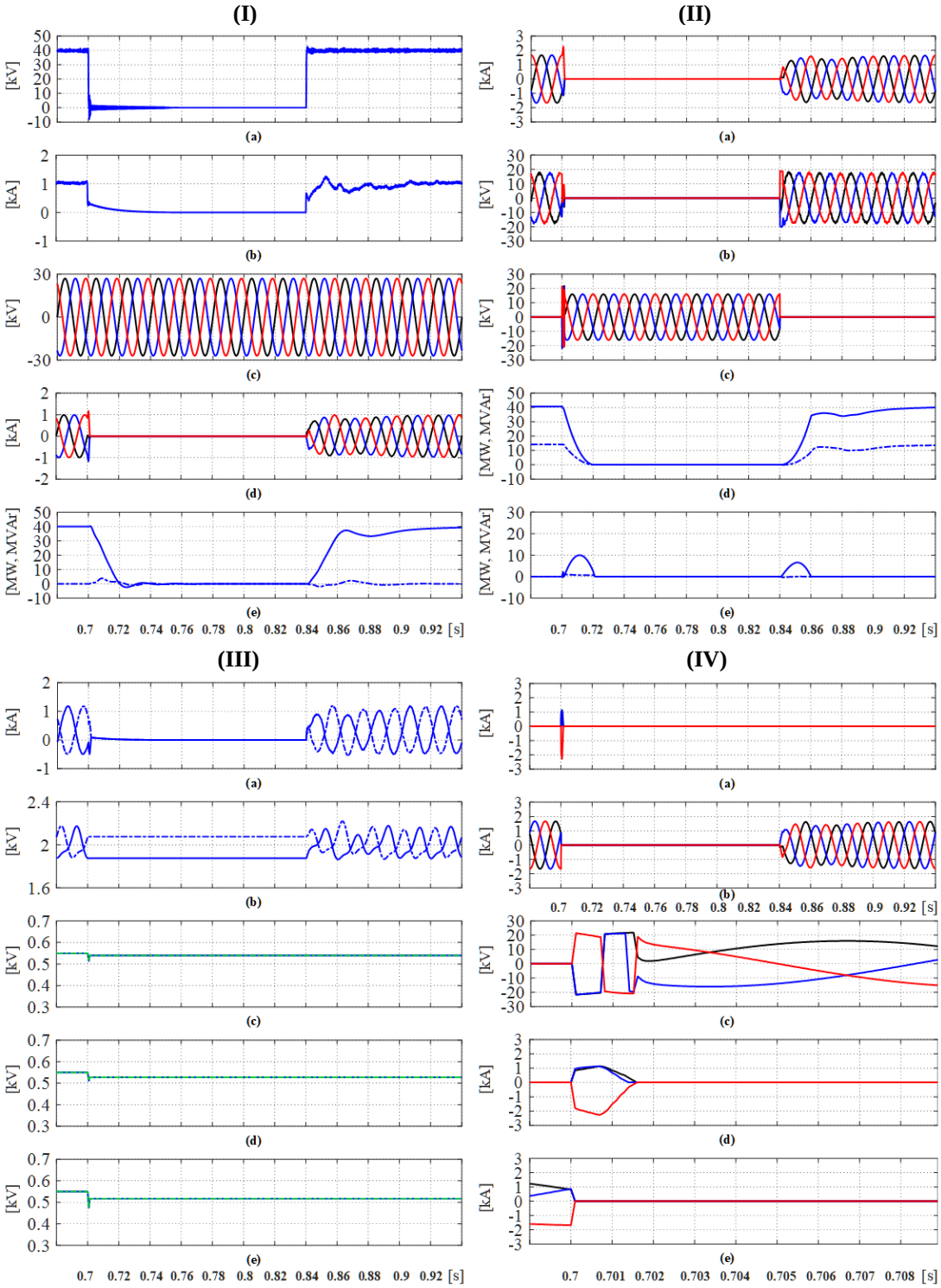


Fig. 3-16. TSG-based T-MMC waveforms in dc fault blocking case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

Simulation results in Fig. 3-17-I to IV show the dc fault blocking capability of USG-based T-MMC. A pole-to-pole solid short-circuit dc fault is applied at 0.7s and cleared after 140ms, whence voltage and current of T-MMC dc-side terminal fall to zero, as depicted in Fig. 3-17-I(a) and (b). Also, PCC voltage is as in the normal case, whereas the PCC current is blocked, see Fig. 3-17-I(c) to (e). During the dc fault, Stage-II blocks the fault. Thus, with the assistance of T-MMC Stage-II, inrush current from the ac side into dc side is prevented, and ac-side voltage stress transfers to Stage-II, see Fig. 3-17-II(a)-(e). Fig. 3-17-III shows selected internal variables of the stages during the fault. Stage-I SMs are blocked, as shown in Fig. 3-17-III(a) and (b), and Stage-II SMs are blocked, as shown in Fig. 3-17-III(c)-(e). Fig. 3-17-IV depicts the UFBS-commutation process (2ms duration is required). After 0.7s, UFBS and FB-SM paths of Stage-II are turned-off and blocked respectively, as shown in Fig. 3-17-IV(d) and (f).

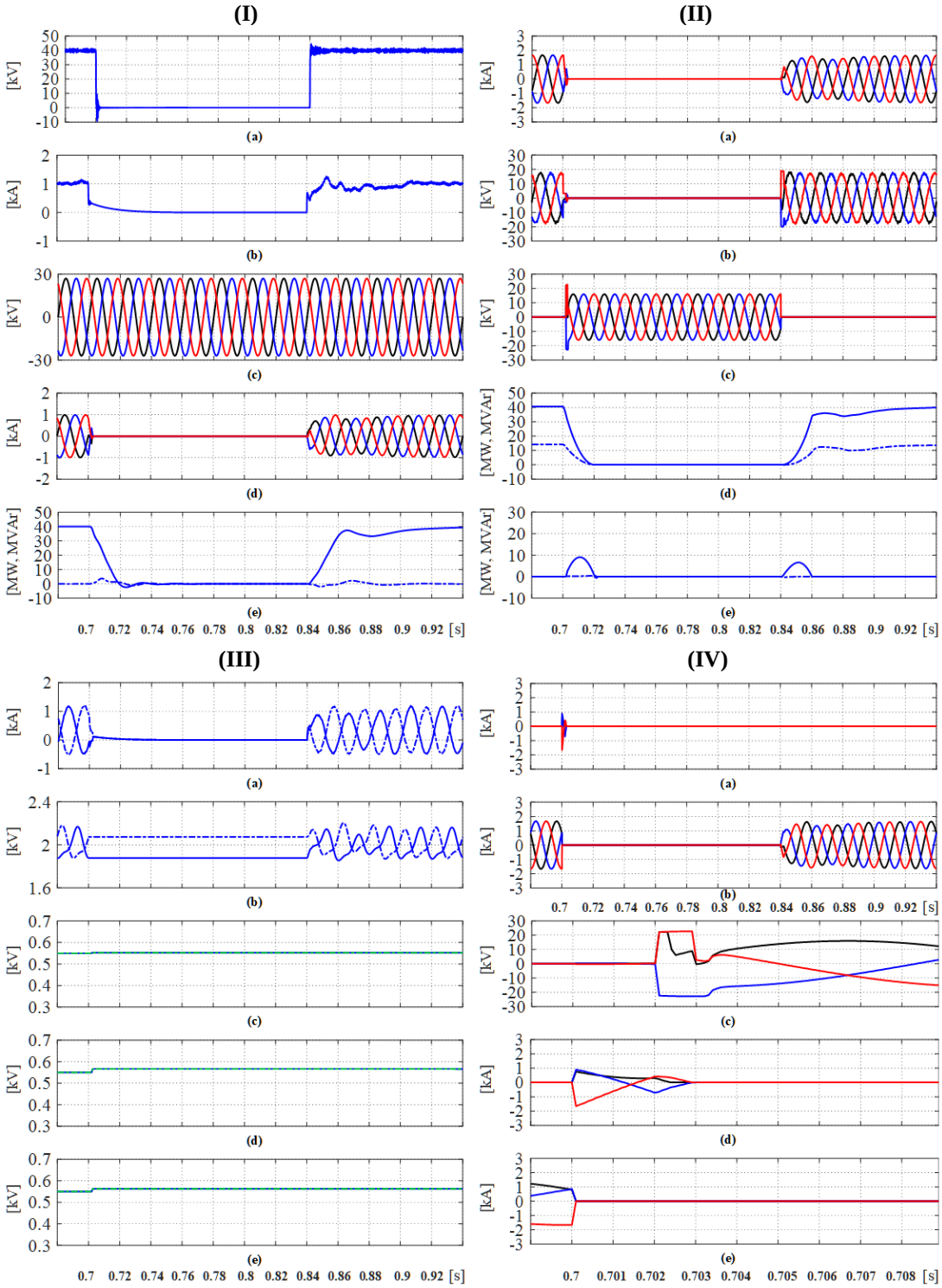


Fig. 3-17. USG-based T-MMC waveforms in dc fault blocking case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

3.6.3 DC Fault with *Q*-support Case

Fig. 3-18-I to IV demonstrate the reactive power support function of the TSG-based T-MMC during the dc fault. With the previous dc fault condition, the simulation waveforms in Fig. 3-18-I(a)-(e) show that the T-MMC can still provide reactive power (PCC reactive power equals 20MVAr) for the ac grid during the dc fault. After thyristor-commutation, the T-MMC (Stage-II, specifically) generates ac voltage to support the ac side (more that 20MVAr, to compensate the ac bus impedance as well), rather than eradicate ac current, as shown in Fig. 3-18-II. Fig. 3-18-III shows that Stage-I bypassed arms become part of the ac bus while its SMs remain blocked. Also, Stage-II operates as a STATCOM connected to the PCC, where the active power exchange regulates the capacitor voltages, and reactive power output is utilized for PCC *Q*-support. Fig. 3-18-IV shows the thyristor-commutation process (700μs duration is required), whereas Stage-II FB-SMs change from the bypassed mode to the active mode.

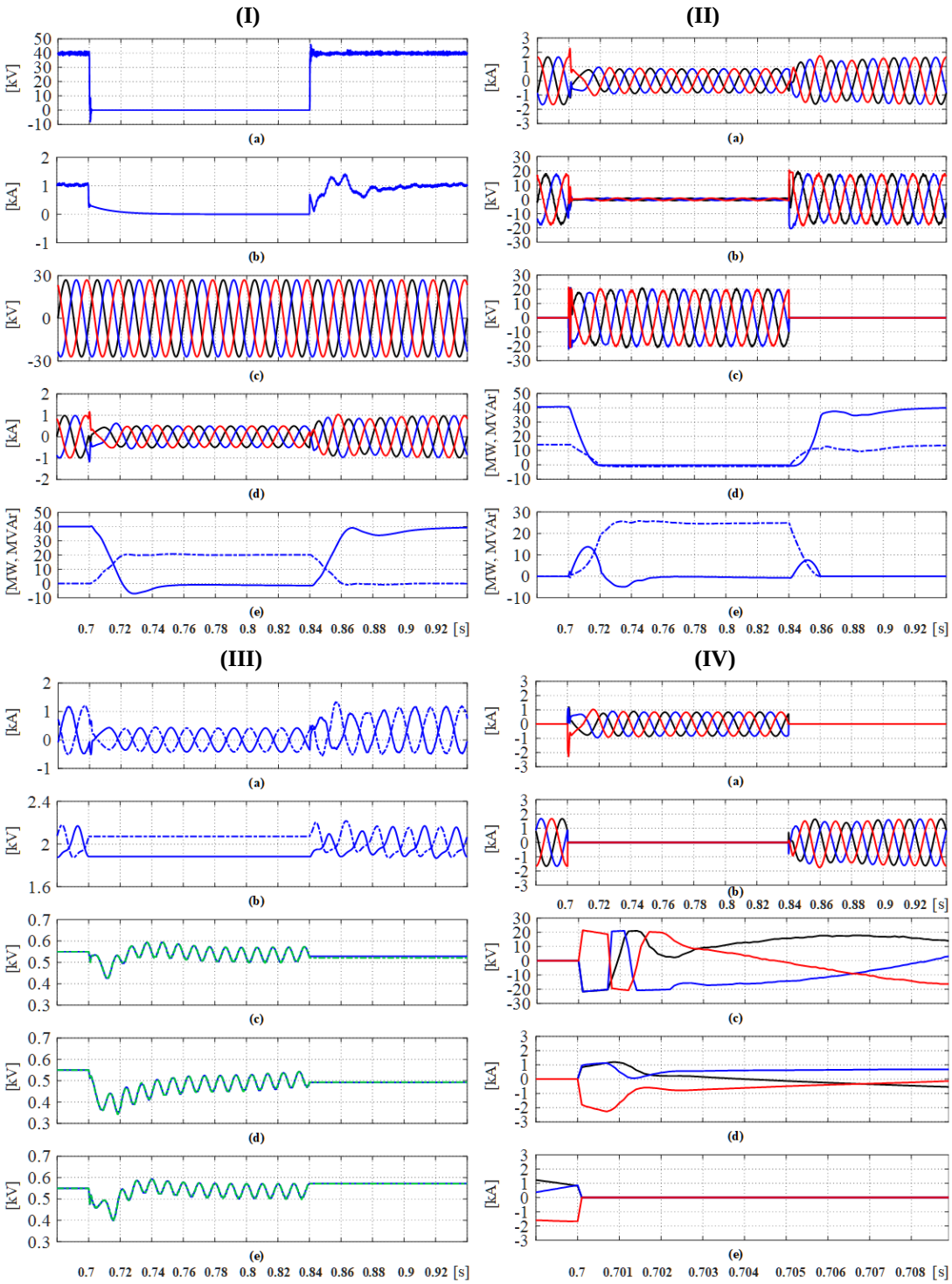


Fig. 3-18. TSG-based T-MMC waveforms in dc fault with *Q*-support case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

Fig. 3-19-I to IV demonstrate the reactive power support function of the USG-based T-MMC during the dc fault. Simulation waveforms in Fig. 3-19-I(a)-(e) show that the T-MMC can still provide reactive power (PCC reactive power equals 20MVAr) for the ac grid during the dc fault. After UFBS-commutation, the T-MMC (Stage-II, specifically) generates ac voltage to support the ac side (more that 20MVAr, to compensate the ac bus impedance as well), rather than eradicate ac current, as shown in Fig. 3-19-II. Fig. 3-19-III shows that Stage-I bypassed arms become part of the ac bus while its SMs remain blocked. Also, Stage-II operates as a STATCOM connected to the PCC, where the active power exchange regulates the capacitor voltages, and reactive power output is utilized for PCC *Q*-support. Fig. 3-19-IV shows the UFBS-commutation process (2ms duration is required), whereas the Stage-II FB-SMs change from the bypassed mode to the active mode.

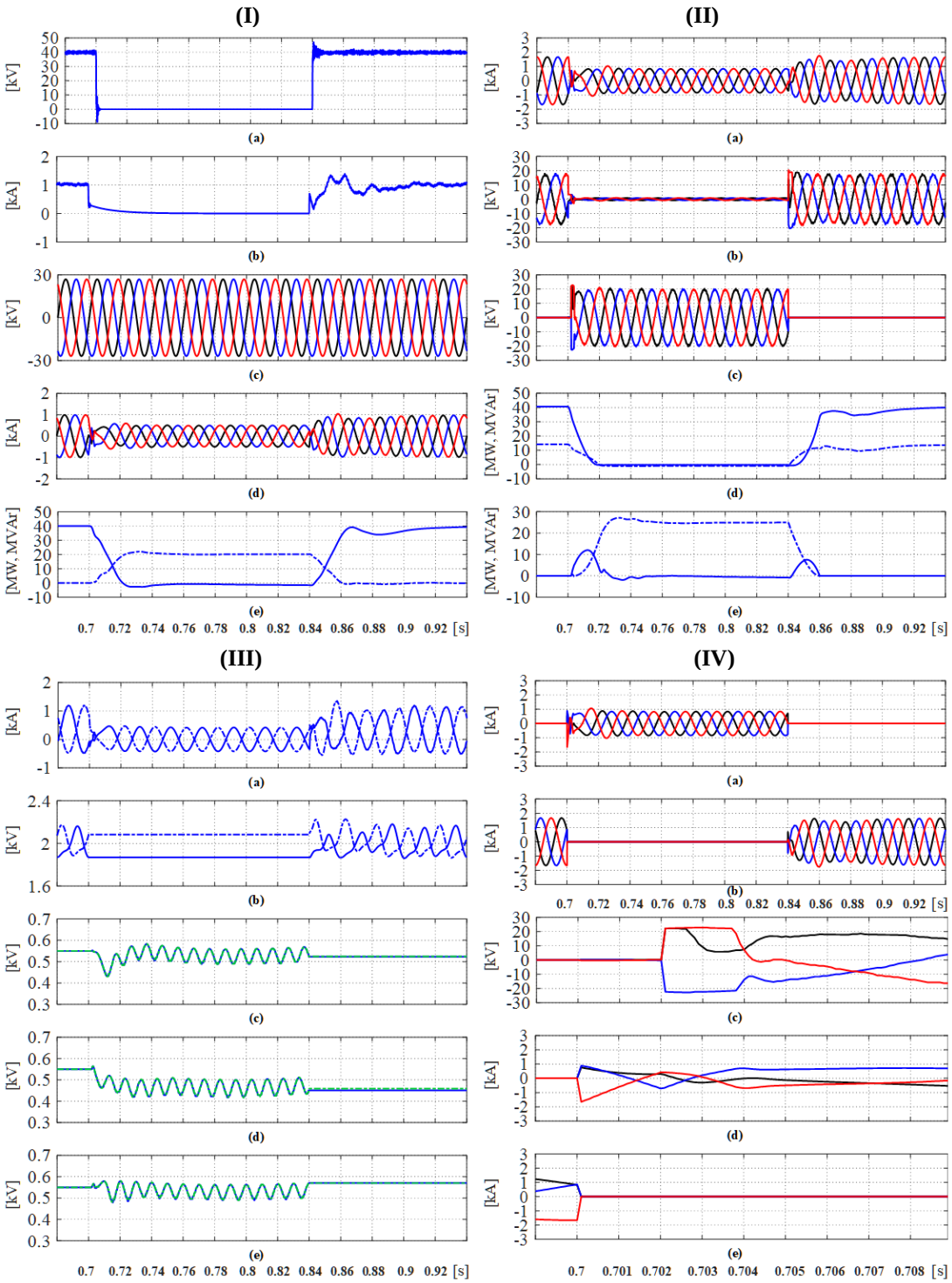
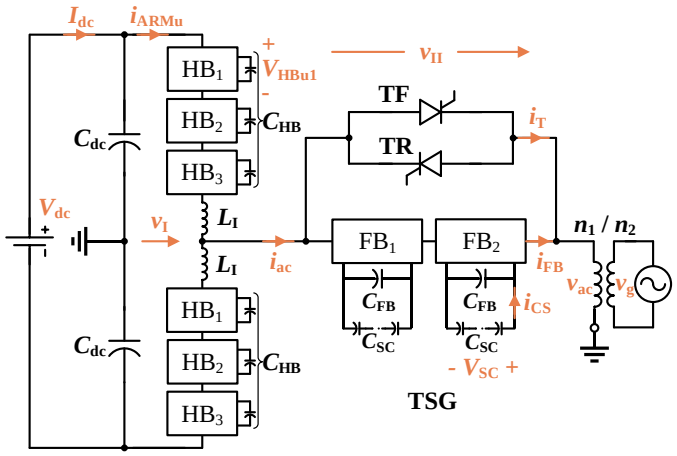


Fig. 3-19. USG-based T-MMC waveforms in dc fault with *Q*-support case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

In these simulation cases, the TSG-based bypassing method may need less commutation time than the USG based case. But the commutation durations are highly depended on the turn-off time of the adopted technologies. Also, the previous commutation process waveforms show that both methods for the Stage-II are able to switch between the bypassed efficient state and the FB-SM based active state, depending on the converter mode requirement. However, compared with the FB and mixed-cell MMCs, the T-MMC avoids improving the dc fault tolerance ability by simply inserting FB-SMs into the main conduction path. The T-MMC retains dc fault ride-through capability without compromising normal operation efficiency; thereby, providing an effective solution to the trade-off between fault-blocking competency and converter operating efficiency.

3.7 Experimentation

A single-phase prototype is used to verify the main functions of the proposed TSG-based T-MMC, with the hardware schematics, photograph and parameters shown in Fig. 3-20 and Table 3-3. Voltage and current variables for the waveforms are measured as indicated in Fig. 3-20.



(a)

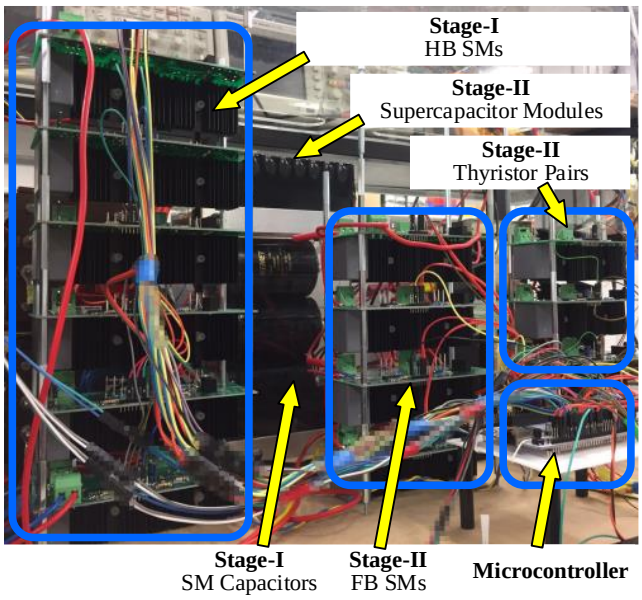


Fig. 3-20. Experimental prototype of the proposed T-MMC integrated with SCs: (a) schematics and (b) photograph.

Table 3-3. Hardware parameters.

	Parameters	**Rating**
DC/AC Sides	Rated Power	500W
	DC-Side voltage V_{dc}	120V
	DC link capacitance C_{dc}	6.8mF
	AC grid rms voltage v_g	240V
	AC transformer leakage	250uH
	AC transformer ratio n_1/n_2	36/240
Microcontroller	Modulation type	PWM-PD
	Switching frequency	2kHz
	Sampling frequency	10kHz
Stage-I	HB-SM rated voltage	40V
	HB-SM capacitance C_{HB}	3.8mF
	HB-SM IGBT type	IRG7PH35UD1-EP
	Arm inductance L_I	3mH
Stage-II	FB-SM rated voltage	32V
	FB-SM capacitance C_{FB}	2mF
	FB-SM IGBT type	IRG7PH35UD1-EP
	Thyristor (TF//TR) type	TM8050H-8W
	Commutation duration t_c	300us
	SC cell type	BCAP0100
	Series cell No. per module N_S	18
	Parallel cell No. per module N_P	1

The converter is controlled to transfer rated power from the dc to ac side, while the control system is executed by an Arm Cortex-M7 processor, including the sorting-

based algorithm for the SM voltage balancing. In this chapter, the energy storage function of the integrated supercapacitors is not utilized.

3.7.1 Normal Operation Case

Fig. 3-21 shows T-MMC waveforms during the normal operation.

In Fig. 3-21(a)-(d), the converter ac-side current (amplitude 20A) is near sinusoidal and in phase with the grid voltage, injecting rated power at unity power factor. Stage-I takes over ac-side voltage generation (with most switching harmonics suppressed by the ac bus inductive impedance), while the thyristors (TF and TR) are maintained on to bypass the IGBT-based FB-SMs, see Fig. 3-21(e)-(h). With the voltage drop across Stage-II being about 1V (due to the superior conducting characteristics of thyristors), Stage-II conduction losses are minimized in this normal mode, see Fig. 3-21(f)-(h). The upper arm current and HB_1 SM capacitor voltage of Stage-I are shown in Fig. 3-21(i) and (k), indicating the circulating current is suppressed and SM voltages are controlled by the inner-stage controllers. As expected, this operation mode is observed being similar to that of a conventional HB-MMC.

As the FB-SMs of Stage-II are bypassed, SC current is zero; hence the SC voltage is constant, see Fig. 3-21(j) and (l).

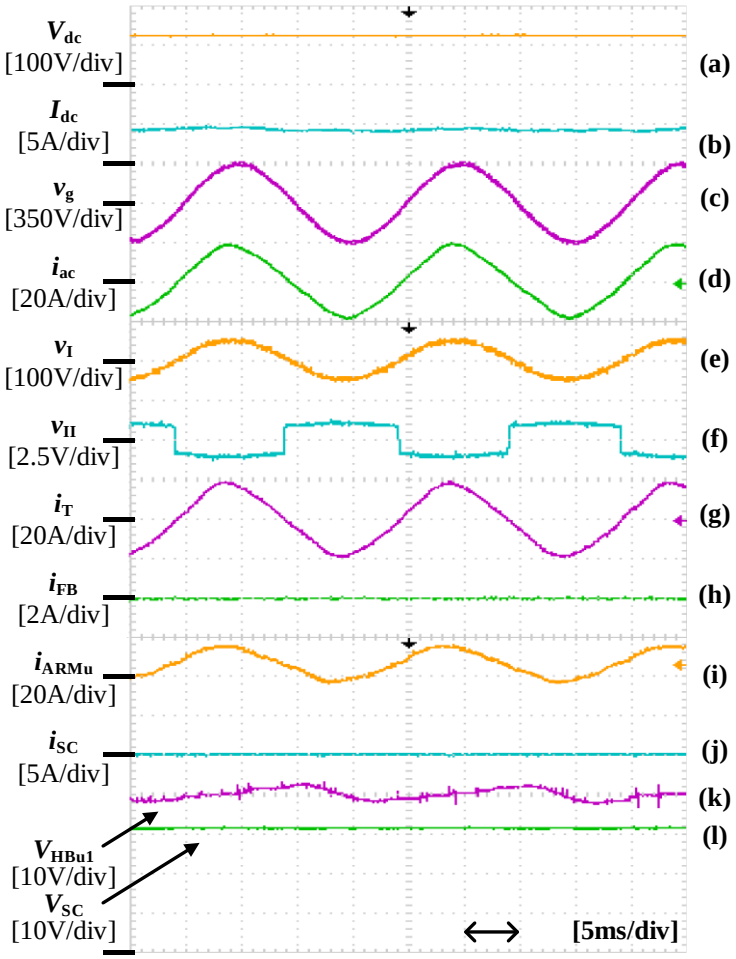


Fig. 3-21. T-MMC waveforms in the normal mode.

3.7.2 AC-Side Voltage Boost Case

In order to verify the ac-side voltage boost ability of the proposed T-MMC, a significantly increased interfacing inductance, which would require an extra inductive *Q*, is used as illustrated in Fig. 3-22.

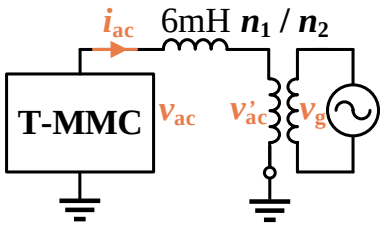


Fig. 3-22. Schematics for the ac-side voltage boost case.

The experimental waveforms in Fig. 3-23(a)-(e) show that the T-MMC (Stage-I) maintains active power conversion, while both stages are activated, contributing to

generation of the increased ac-side voltage, see Fig. 3-23(f)-(j). As a result, an enlarged ac-side output voltage ($v_{ac} = v_I + v_{II}$) is synthesized (approximately, 100V + 80V = 180V peak-to-peak), while both stages operate without over-modulation. Stage-I upper arm current and HB_1 SM capacitor voltage, which are regulated, are shown in Fig. 3-23(k) and (n).

As stage-II only provides reactive power, the mean SC charging current is zero and the SC voltage remains in steady-state (with minor ripple due to the SC internal resistance), see Fig. 3-23(l) and (m).

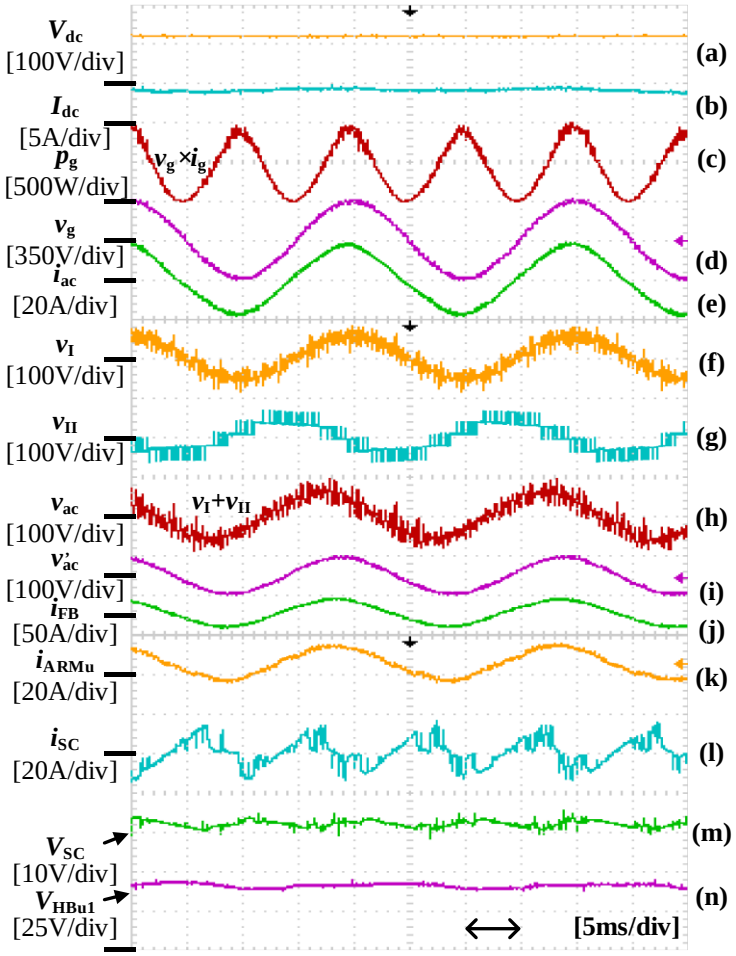


Fig. 3-23. T-MMC waveforms in an enlarged inductance case.

3.7.3 Thyristor Forced-Commutation

Fig. 3-24 demonstrates the thyristor-commutation process of the TSG in Stage-II. The TSG-based T-MMC is to verify the thyristor forced-commutation method, which is more intricate than that of the UFBS as discussed.

When the ac current is positive (conducted by TF), forced-commutation is achieved when the FB-SM generates a positive voltage for a duration t_c. Then, with TF turned-off, the ac current commutates from the thyristor path to the FB-SM path. The process for TR commutation is shown for the negative i_{ac} case. The ac current deviates slightly during the commutation process, after which full control recovers; and when the process is complete, FB-SMs are able to respond to control system demands. The results confirm the analysis articulated.

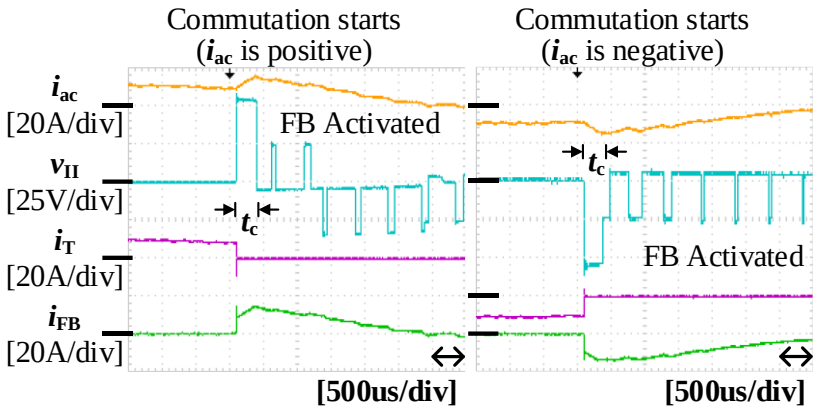


Fig. 3-24. Stage-II TSG thyristor-commutation process waveforms.

3.8 Summary

A T-type MMC referred to as T-MMC has been proposed in this chapter. Flexible operation based on the dual-stage topology can perform ac/dc side protective and supportive functions, such as ac/dc fault isolation, reactive power enlargement, etc. Also, ESS integration into the converter is feasible.

Novel thyristor-SM grouping and UFBS-SM grouping for the Stage-II have been presented, with the commutation mechanism and converter-level merits elaborated. As a result, both high efficiency and tolerance capability are achieved by the T-MMC, which was highlighted by comparing it with other typical MMCs.

The effectiveness of the proposed T-MMC was demonstrated through simulation and experimentation.

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Chapter 4

T-MMC Based Energy Storage Systems

Energy storage elements can be integrated into the SMs of the T-MMC; therefore, the T-MMC can perform as a flexible ESS, enabling regular energy storage, advanced grid ancillary services provision, and dc/active power support during system intermittency and faults. Taking the advantages of controllability and flexibility of the independent stages, a decoupled power relationship between the ac and dc sides of the T-MMC based ESS is achieved, which is important for enhancing ac and dc fault performance. Operation of the proposed ESS under normal conditions and during ac and dc faults is investigated, with the control system presented. Simulation and experimentation confirm the enhanced performance, including continuous operation during ac and dc faults with negligible power transfer disruption.

4.1 Motivation and Background of Energy Storage Integration into MMCs

With the development of power electronic dominant systems, integrating energy storage systems is an effective approach to increase system inertia and associated stability and security. Also, energy storage systems can facilitate system power flow management. Currently, both energy storage technologies and ESS integration approaches have technical limitations and practical challenges in medium and high voltage applications, which impede their exploitation [1], [2]. Among various electrical energy storage technologies, battery and supercapacitor are two types which offer high energy and power density features. As MMC SMs can perform flexible control and management in terms of voltage balancing, state-of-charge (SoC), health, etc., the distributed deployment of rechargeable batteries and/or supercapacitors (SCs) is applicable [3], [4]. Thus, integrating batteries or supercapacitors into the MMC is a promising approach as such ESSs are suitable for distributed utilization and the converter can perform as a battery/supercapacitor management system. However, the difference between the rated voltage of high voltage applied MMC SMs (typically

ranging from 1.6kV to 2.8kV) and the battery or supercapacitor stacks (typically ranging from 400V to 850V) presents a technical restriction of integrating energy modules (EMs) into HVDC converters, which is limiting deployment. To overcome this issue, hard and soft switching dc/dc converters are proposed to meet the high voltage requirements and reduce ESS current ripple, but system complexity and conversion losses are increased [5]-[7].

An MMC-based ESS would be especially critical for secure systems when considering fault cases [6]. For example, in critical ac/dc conversion applications such as HVDC, multi-terminal dc grids, and shipboard power systems, regulating the dc-side power is essential for system safe operation when an ac grid fault occurs. Also, mitigating the influence of any temporary power transfer loss, due to major disturbances in other parts of the asynchronous power system or dc grid faults, on the stability of connected ac grids, is a necessity to be realized. A number of solutions that employ the shunt-connected ESS in the ac or dc side, or integrating EMs of supercapacitors or batteries into MMC SMs, have been proposed, particularly, to enhance system inertial response and frequency stability.

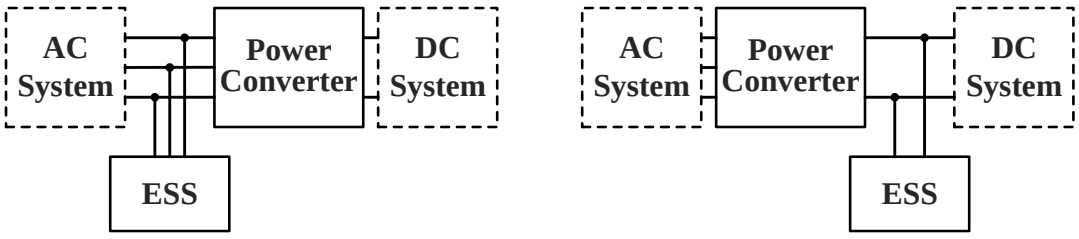

Fig. 4-1. Shunt-Connected ESSs: (a) in the ac side and (b) in the dc side.

The shunt-connected ESS in the ac side, as shown in Fig. 4-1(a), is effective for smoothing short-duration active (and reactive) power variations of the host ac grid as a result of disturbances in remote asynchronous ac grids. However, it is unable to prevent over/under voltage on the dc side during nearby solid short circuit ac faults. Conversely, the shunt-connected ESS in the dc side, as shown in Fig. 4-1(b), can prevent the dc side over/under voltage during severe ac faults, but it is unable to support ac grids during dc faults; especially during sub-transient periods. As power exchanging capability of conventional ESS is impaired when the parallel-connected network has a fault, two sets of shunt-connected ESSs are needed for both ac and dc

side power flow smoothing. An HB-MMC integrated with batteries was investigated to minimize SM capacitance and regulate the dc voltage during ac low-voltage ride-through operation in [6]. In [7] and [9], HB-MMCs with batteries or supercapacitors were investigated as pure ESS for dc transmission. However, the use of HB-SMs compromises dc fault withstanding ability. With the advantage of FB-SMs and the integrated battery EMs, a control method of the hybrid MMC is proposed to regulate power flow continuously in normal and ac/dc fault modes [10]. During the dc fault, ac grid active power is controlled to exchange with the upper and lower arms, which operate as shunt-connected ESSs, where arm voltages and currents have zero offset, while dc current is nullified gradually as the common-mode current of each phase-leg is zero. However, the battery transient current rating is limited in high power applications, and normal-mode operation efficiency is similar to that of the mixed-cell MMC. Also, this implementation (based on either FB-MMCs or hybrid MMCs) may be impeded in HVDC applications, as the transient discharge current (caused by the distributed parameters of the dc side long-distance overhead line or cable plus the ac current associated with the regulated active power being exchanged with the ac grid) may pose significant risks to the converter semiconductor switches. Additionally, the degraded special dc/dc converters formed by FB-SMs in the ac fault mode are unable to inject reactive power into the ac grid, which is essential from the ac grid protection point of view.

In the light of these factors, the T-MMC based ESS is presented in this chapter, with discussion on operational modes and additional functions. Simulation and experimentation results shows advantageous features for both sides of the converter, establishing the effectiveness and benefits.

4.2 Configurations and Features of the T-MMC based ESS

Integrating SC or battery based EMs into the T-MMC can be implemented by connecting the EMs with the SM dc-side, as shown in Fig. 4-2 for the MMC SMs.

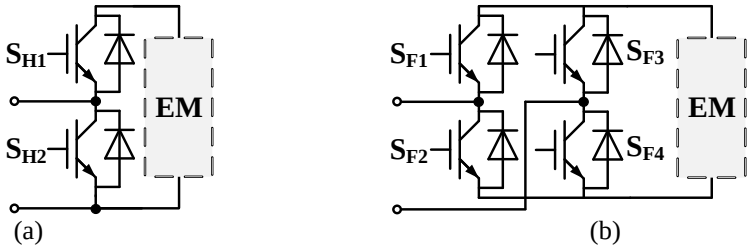

Fig. 4-2. SMs with EM integration: (a) HB-SM and (b) FB-SM.

Although, from the system inertia aspect, it is desirable to equip the converter with as much EMs as possible; integrating EMs into the Stage-I is not necessary for the fulfilment of enhanced fault ride-through capabilities. Thus, integrating proper EMs into the Stage-II is essential for advanced functions, and the proposed Stage-II is amenable to splitting EM integration. The FB-SMs voltage level V_{FB} can be adjusted by N' (and K) to suit commercially available ESEs, of which the voltage level is usually obtained by series-connection of small cells. Despite an increased cost and size, the T-MMC topology allows EM galvanic isolation.

The T-MMC integrated with energy storage elements (ESEs) can provide additional security features for the connected systems. For grid-connected applications, the grid-connected system model in Fig. 4-3 shows a power path to the ESEs. With added energy storage, Stage-II can partake in active power exchange. The T-MMC based ESS is able to simultaneously provide enlarged P-Q support for the ac side due to the independent Stage-II. As a result, flexible power flow management is achieved, which can improve converter resilience against ac/dc faults and other severe disturbances. Also, the tied power systems may suffer from sudden power changes during ac network faults or consumption/generation fluctuation. With appropriately sized ESEs, the power relationship between the dc and ac sides can be decoupled by the converter, leading to an increased system security margin.

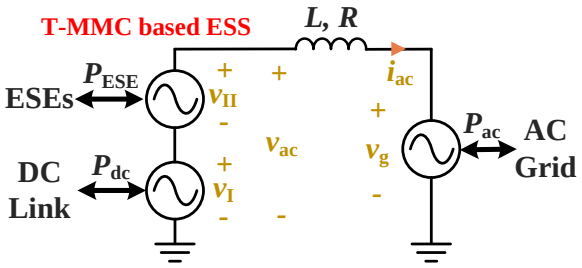

Fig. 4-3. Analytical model of a grid-connected system with T-MMC based ESS.

Generally, the most severe fault case is that one side completely loses its power due to a solid fault. If the ESEs within Stage-II has sufficient power/energy rating, any power pause in the dc/ac side caused by the ac/dc side fault can be eliminated. Single-phase conceptual waveforms are shown in Fig. 4-4. When a worst-case solid ac-side fault occurs, the T-MMC ac-side output voltage v_{ac} is reduced under control. In Fig. 4-4(a) Stage-I maintains its original power conversion (P_{dc} is maintained), whereas Stage-II operates to exchange power with Stage-I ($P_{ESE} = P_{dc}$). This is a special case of ac-side power support. Under the worst dc-side fault condition, Stage-I upper and lower arms are bypassed, and Stage-II generates ac voltage to provide *P*-*Q* support ($P_{ESE} = P_{ac}$), as shown in Fig. 4-4(b).

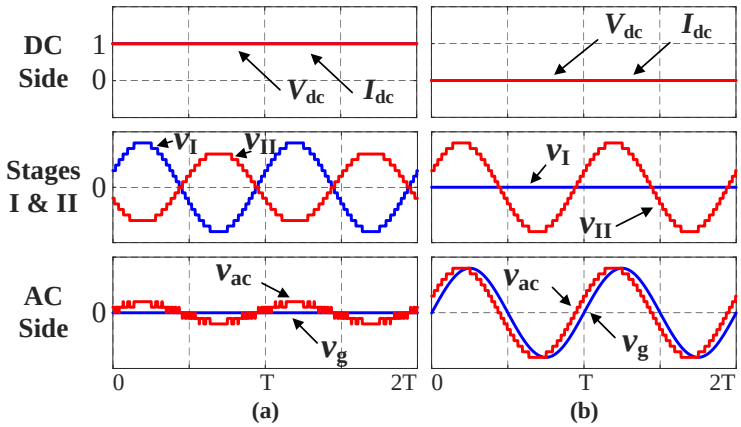

Fig. 4-4. T-MMC conceptual waveforms (in pu) with sufficient ESEs: (a) Mode 3 and (b) Mode 4.

In detail, when an ac short circuit fault occurs, successful activation of the on-demand Stage-II based ESS enables its FB-SMs to generate an ac voltage with appropriate phase and magnitude relative to those of Stage-I and the ac grid to facilitate controlled generation or absorption of the active (and reactive) power that cannot be exchanged with the ac grid due to voltage collapse, with the Stage-I seeing the Stage-II as a

replacement of the normal ac grid. In this way, the dc power flow P_{dc} is uninterrupted, while the station is also able to provide reactive power support to the ac grid. When a dc short circuit fault occurs, Stage-I SMs are bypassed by the back-to-back connected protective thyristors, while the on-demand Stage-II based ESS is activated after successful current commutation. Thus, the arm inductors and transformer leakages are part of the system impedance. Long distance dc line inductance and resistance between the dc fault point and the station can also be included. Due to FB-SM bipolar output and the energy stored inside the EMs, the activated Stage-II based ESS replaces Stage-I, sourcing or sinking active (and reactive) power during the dc fault period, and the phase and magnitude of the Stage-II ac voltage must be adjusted relative to that of the ac grid and Stage-I. Thus, during a dc fault, Stage-II takes control over the ac current, including the ac current components that flow through Stage-I. As a result, full control over active and reactive power exchanged with the ac grid is retained. As the upper and lower arm currents of Stage-I (HB-MMC) sum to zero at the positive and negative dc nodes, the absence of dc components in HB-MMC arm currents leads to rapid fall of the dc fault current after bypassing the HB-MMC and activating Stage-II.

From an energy flow aspect, Stage-I SM capacitors ideally exchange zero net dc/active power with the dc/ac grid during normal operation. Accordingly, when converters are assumed to be lossless, the dc power P_{dc} will be transferred to the ac-side P_{ac}. Thus, the ESEs within Stage-II act as a power buffer (P_{ESE}) between P_{dc} and P_{ac}.

4.3 Energy Storage Elements for the T-MMC

Various existing energy storage technologies, such as Lithium-ion batteries and supercapacitors, can be used in the T-MMC EMs due to their suitability for burst power applications. Generically, for fault ride-through applications, ESE sizing includes estimates of the active power rating, stored energy capability, and net energy exchanged for a given charge/discharge depth. For the uninterrupted active power transfer (sinking or sourcing) within a finite duration, each EM must be rated at:

$$P_{EM} = \tfrac{1}{3}P_{ESE}/N' \tag{4-1}$$

where P_{EM} is the EM rated active power. Hence, the EM rated current is:

$$I_{EM} = P_{EM}/V_{EM} \tag{4-2}$$

where V_{EM} is the EM rated voltage.

The minimum EM energy capability is calculated based on worst-case scenarios such as a three-phase solid ac fault and a pole-to-pole solid dc fault, in which the ESE is required to provide rated power support for an ESS operating duration of T_{ESS} ($T_{ESS} = T_2 - T_1$, and must be selected larger than the fault critical times). Therefore, the stored energy per EM E_{EM} is quantified as:

$$\begin{aligned} &\frac{dE_{EM}}{dt} = P_{EM} \\ &\Rightarrow \int_{E_{EM1}}^{E_{EM2}} dE_{EM} = \int_{T_1}^{T_2} P_{EM} dt \Rightarrow E_{EM2} - E_{EM1} = P_{EM}(T_2 - T_1) = P_{EM} T_{ESS} \end{aligned} \tag{4-3}$$

where E_{EM1} and E_{EM2} are EM energy levels at arbitrary instances T_1 and T_2 respectively, and E_{EM1} and E_{EM2} are associated with EM voltages V_{EM1} and V_{EM2} respectively. If the initial EM voltage V_{EM1} is assumed to be rated voltage, the voltage V_{EM2} will define the maximum voltage stress on the EM and FB-SM components, and the minimum voltage level to synthesize the required Stage-II ac output voltage. Thus, assuming $E_{EM2} = kE_{EM1}$ (k is selected depending on the allowable charge/discharge depth), the initial stored energy estimate within each EM is:

$$|1-k| E_{EM1} = P_{EM} T_{ESS} \Rightarrow E_{EM1} = \frac{P_{EM} T_{ESS}}{|1-k|} \tag{4-4}$$

Other practical factors may vary from one energy storage technology to another; therefore, the presented EM energy storage estimate should be adjusted with technology-dependent considerations such as permissible current capability, current and voltage ripple requirements for extended lifetime, etc. Then, the corrected energy storage can be used to quantify and optimize the ESS scale and its capital cost. For the proposed structure, the deliberate use of low-rated FB-SM voltages within the ESS permits direct connection of the EM across the FB-SM.

Stage-II performance depends on the integrated ESE characteristics, while the SC is currently an especially attractive choice due to high power capability and long lifetime; an example used in this study is shown in Fig. 4-5, where the FB-SM is equipped with

an SC module of N_S series and N_P parallel connected SC cells. Usually, due to the intrinsic SC time constant, a shunt connection with conventional electrolytic and/or film/paper capacitors (with the lower ESR and longer lifetime) results in an efficient configuration [11].

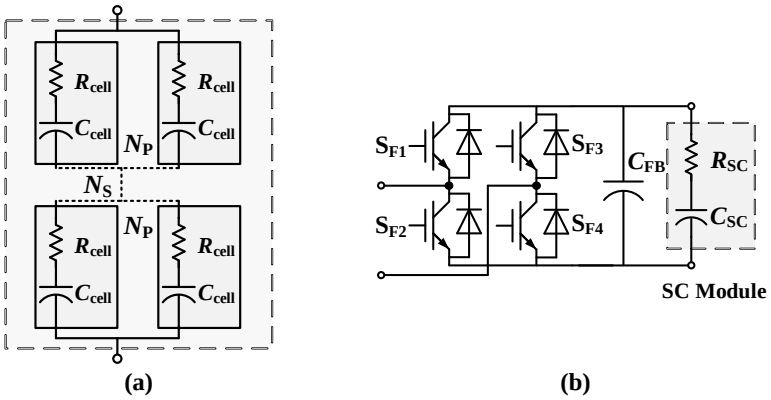

Fig. 4-5. EM example: (a) Simplified model of an SC module and (b) FB-SM with an SC module.

The SC sizing of the Stage-II ESE can be evaluated, assuming:

- *SC modules:* All Stage-II $3\times N'$ FB-SMs are integrated with the same rated SC modules;
- *SC cells:* Cells inside the SC module are balanced in terms of voltages and currents, while the capacitance and ESR of cells (C_{cell} and R_{cell} respectively) are equal and constant; and
- *Conventional capacitors:* The ESR and stored energy of conventional capacitors are negligible compared with those of SC, whereas the current pulse due to switching action is sourced by conventional capacitors.

Thus, there are some design factors to be considered:

- *Rated voltage:* The minimum number of series-connected cells within one SC module N_S is determined by:

$$N_S \geq V_{FB}/V_{cell} \tag{4-5}$$

where V_{FB} is the steady-state voltage set point of the FB-SM and V_{cell} is the SC cell rated voltage.

- *Available energy and absolute maximum voltage:* The number of parallel-connected cells within one SC module is:

$$N_{\mathrm{P}(1)} \geq \frac{2P_{\mathrm{ESE}}T_{\mathrm{ESS}}}{3N^{'}N_{\mathrm{S}}C_{\mathrm{cell}}V_{\mathrm{cell}}^{2}[1-(1-\delta)^{2}]} \tag{4-6}$$

  where T_{ESS} is the ESS full-power operation duration in the constant P_{ESE} power rating, and δ is the SC maximum charge/discharge depth, which for safety should be restricted to:

$$\delta \leq \hat{V}_{\mathrm{cell}}/V_{\mathrm{cell}} - 1 \tag{4-7}$$

  where $\hat{V}_{\mathrm{cell}}$ is the SC cell absolute maximum voltage.

- *Absolute maximum current:* From an over-current protection perspective, another boundary is:

$$N_{\mathrm{P}(2)} \geq KI_{\mathrm{ac}}/\hat{I}_{\mathrm{cell}} \tag{4-8}$$

  where K = 1 or the transformer turns ratio, depending on the topology, and $\hat{I}_{\mathrm{cell}}$ is the SC cell absolute maximum current.

- *SM voltage drop:* The SC ESR and SM semiconductors lead to voltage drops, which may affect Stage-II output waveform synthesis. Hence, assuming a fixed on-state semiconductor voltage drop $V_{\mathrm{SEMI\text{-}FB}}$, N_{P} should also satisfy:

$$N_{\mathrm{P}(3)} \geq \frac{KI_{\mathrm{ac}}R_{\mathrm{cell}}N_{\mathrm{S}}}{V_{\mathrm{FB}} - V_{\mathrm{FB}}' - 2V_{\mathrm{SEMI-FB}}} \tag{4-9}$$

  where V_{FB}' is the acceptably minimum value of the FB-SM positive output voltage.

Based on constraints (4-6), (4-8) and (4-9), the minimum number of parallel-connected cells within one SC module N_{P} is:

$$N_{\mathrm{P}} = \max(N_{\mathrm{P}(1)}, N_{\mathrm{P}(2)}, N_{\mathrm{P}(3)}) \tag{4-10}$$

With the determined N_{S} and N_{P}, Stage-II ESE energy capability E_{ESE} can be calculated as:

$$E_{ESE} = 1.5\, N' N_S N_P C_{cell} V^2_{cell} \quad (4\text{-}11)$$

Related variables such as T_{ESS} and P_{ESE} can be adjusted for long-term energy storage applications.

4.4 Commutation and Control

With ESE integrated into Stage-II, the corresponding operation modes can offer additional functions. Thus, the status of T-MMC based ESS are slightly changed, as shown in Fig. 4-6, where the Stage-II bypass path is off in modes 2 to 4 to allow FB-SM active operation.

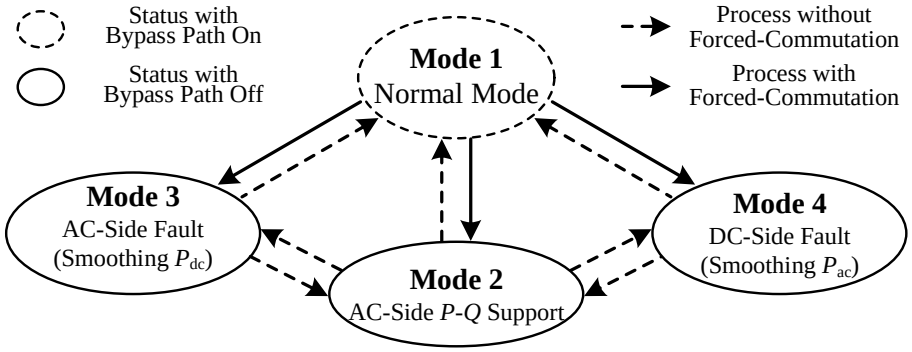

Fig. 4-6. Status diagram of the T-MMC based ESS with additional functions.

Also, with additional features, the T-MMC based ESS control structure should be modified to achieve desirable performance, as shown in Fig. 4-7.

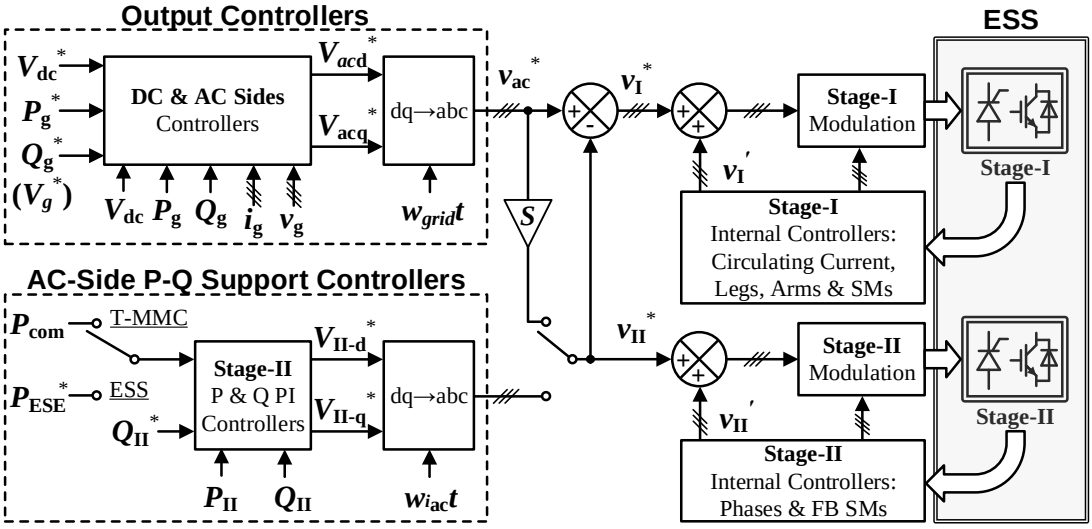

Fig. 4-7. Overall control diagram of the T-MMC based ESS for a grid-connected application.

The stage-level control coordinates operation of two stages, and therefore takes responsibility to tackle abnormal cases. Normally, the Stage-I ac voltage reference (v_{I}^{*}) equals v_{ac}^{*}, whereas that of the Stage-II (v_{II}^{*}) is zero (hardware-wise, bypassing paths are turned on), indicating the normal mode. Similarly, when a dc fault occurs (S = 1), Stage-II can either block the dc/ac sides or generate the ac voltage (using v_{ac}^{*}) under regulation of the ac-side output controllers. The ac-side P-Q support controllers are enabled and selected when ac-side support (including active power support and ancillary services) is required. Stage-II stored energy management is achieved by choosing the T-MMC selection, whereas the ac-side power support is achieved by using the determined power reference (P_{ESE}^{*}, with the ESS selection). Also, Q_{II}^{*} can be used to make Stage-II contribute to ac-side voltage support.

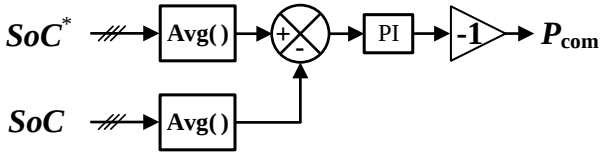

Fig. 4-8. EM average SoC controller for Stage-II.

The variable P_{com} (to manage energy storage/usage) is for Stage-II EM average SoC control, whereas Fig. 4-8 shows the Stage-II EM average SoC controller, which is used to adjust the average SoC of the integrated EMs within Stage-II. The core method is to control the active power of the Stage-II and therefore the stored energy will be regulated.

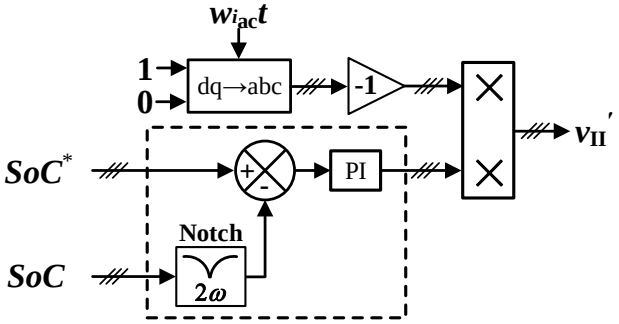

Fig. 4-9. EM SoC balancing controller for Stage-II.

Also, an inter-phase voltage balancing controller is needed, as shown in Fig. 4-9, where notch filters are adopted to suppress potential second-order harmonics (although

smaller due to the integrated EMs) without delay, and fundamental frequency voltage injection ensures active power (energy) regulation.

The relevant modulation techniques are the same as the regular T-MMC.

4.5 Simulation

In order to verify the T-MMC based ESS, the same grid-connection application scenario as for the T-MMC in chapter three is configured. The T-MMC based ESS, with its dc side connected to a voltage-controlled dc link through a short cable and its ac side connected to a stiff ac grid through a Δ-Y interfacing transformer, is simulated using MATLAB/Simulink, with the parameters listed in Table 4-1.

Table 4-1. Simulation parameters.

	Parameters	**Rating**
DC side	DC-link voltage	40kV
	DC cable distance	10km
	DC cable (T-model) inductance	150uH/km
	DC cable (T-model) resistance	11mΩ/km
	DC cable (T-model) capacitance	200nF/km
AC side	AC grid frequency	50Hz
	AC grid voltage	33kV
	Transformer ratio	20/33kV
	Transformer leakage inductance	0.18pu
Stage-I	HB-SM number per arm N	20
	HB-SM rated voltage	2kV
	HB-SM capacitance C_{HB}	6.7mF
	Arm inductance L_I	0.2pu
Stage-II (ESS)	TSG/USG number per phase M	10
	FB-SM number per TSG/USG F	4
	FB-SM rated voltage	0.55kV
	Commutation time for TSGs (t_q = 500us)	700us
	Commutation time for USGs (t_o = 2ms)	2ms
	FB-SM capacitance C_{FB}	3mF
	SC cell type	BCAP0310
	Series cell number per module N_S	204
	Parallel cell number per module N_P	8
	SC module capacitance C_{SC}	12.15F
	SC module ESR R_{SC}	56.1mΩ

The conventional grid-connected control structure, with inner vector current loops, outer *P*-*Q* loops and PLL, is adopted. In the normal case, Stage-I is controlled to inject 40MW active power into the PCC at unity power factor, and Stage-II bypass paths (either TSGs or USGs) are on.

In this section, the simulated behaviour of the T-MMC based ESS, in dc and ac fault cases, are presented.

4.5.1 DC Fault Case

Fig. 4-10-I to IV demonstrate TSG-based T-MMC performance with energy storage system integration, during a dc fault. With a pole-to-pole solid short-circuit dc fault from t = 0.7s to 0.84s (140ms duration), the T-MMC based ESS controls the ac-grid current, and maintains continuous active power injection, as shown in Fig. 4-10-I. During the dc fault, Stage-I is bypassed with minor reactive power consumption due to the arm inductors, see Fig. 4-10-II(a), (b) and (d). Continuous current control is achieved by the energy storage integrated Stage-II, which is able to synthesize ac voltage and exchange active power with the PCC, see Fig. 4-10-II(a), (c) and (e). Also, Stage-II also generates reactive power to compensate the ac bus impedance as shown in Fig. 4-10-II(e). During the dc fault, Stage-I common-mode currents are reduced to zero and the HB-SMs block, as shown in Fig. 4-10-III(a) and (b). Stage-II SCs discharge to provide power, as shown in Fig. 4-10-III(c)-(e). The Stage-II thyristor turn-off process, which needs a 700μs duration, is illustrated in Fig. 4-10-IV(a)-(e).

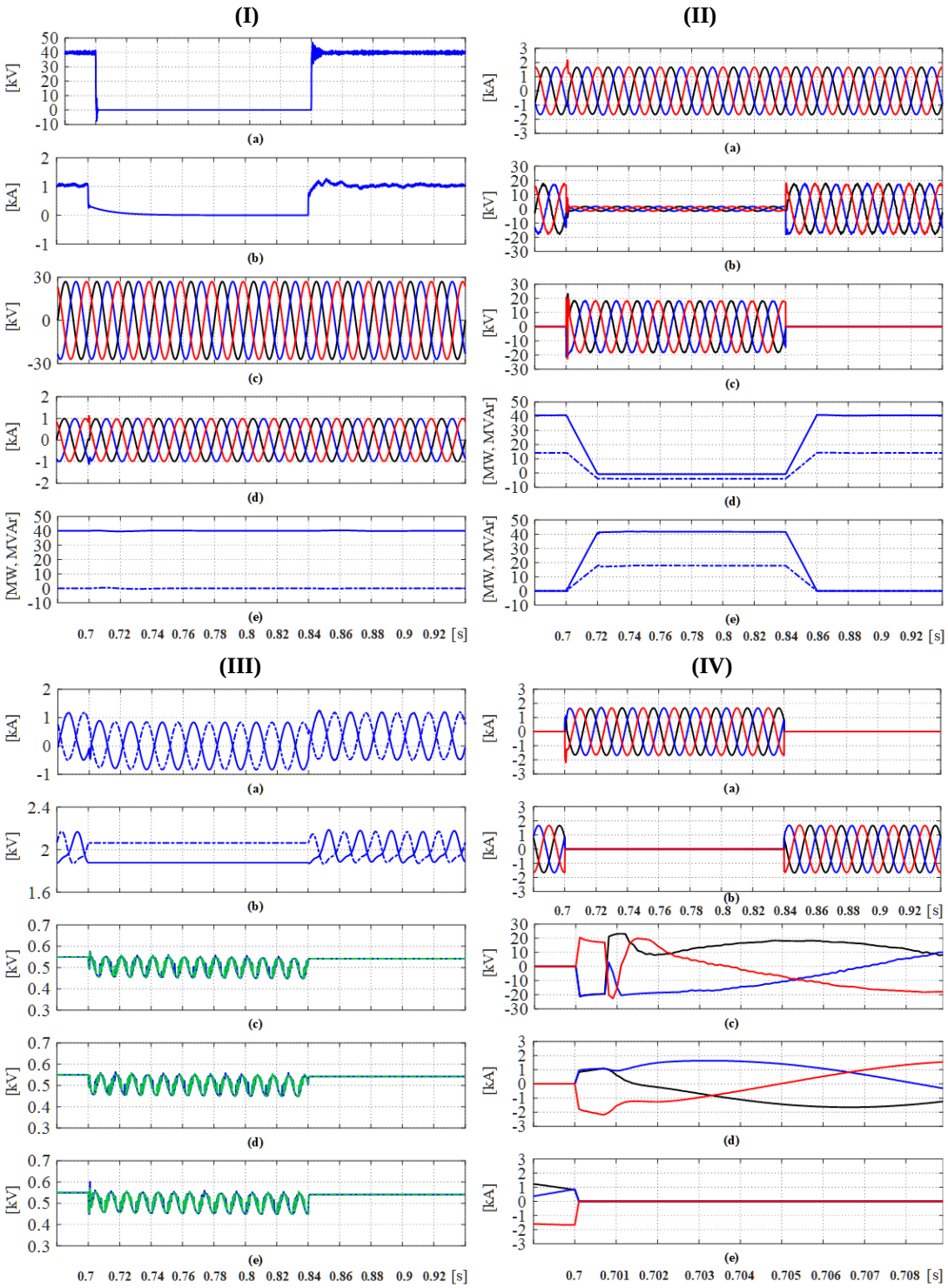

Fig. 4-10. TSG-based T-MMC with energy storage integration in the dc fault case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

Fig. 4-11-I to IV demonstrate USG-based T-MMC performance with energy storage system integration during a dc fault. During the dc fault, Stage-I is bypassed with minor reactive power consumption due to the arm inductors. Continuous current control is achieved by the energy storage integrated Stage-II, which is able to synthesize ac voltage and exchange active power with the PCC, see Fig. 4-11-I(a)-(d). Stage-II also generates reactive power to compensate the ac bus impedance as shown in Fig. 4-11-I(e). With a pole-to-pole solid short-circuit dc fault from 0.7s to 0.84s (140ms duration), the T-MMC based ESS controls ac-grid current, and maintains continuous active power injection, as shown in Fig. 4-11-II(a)-(e). During the dc fault, Stage-I common-mode currents are reduced to zero and the HB-SMs block, as shown in Fig. 4-11-III(a) and (b). Stage-II SCs discharge to provide power, as shown in Fig. 4-11-III(c)-(e). The Stage-II UFBS turn-off process, which necessitates a 2ms duration, is illustrated in Fig. 4-11-IV.

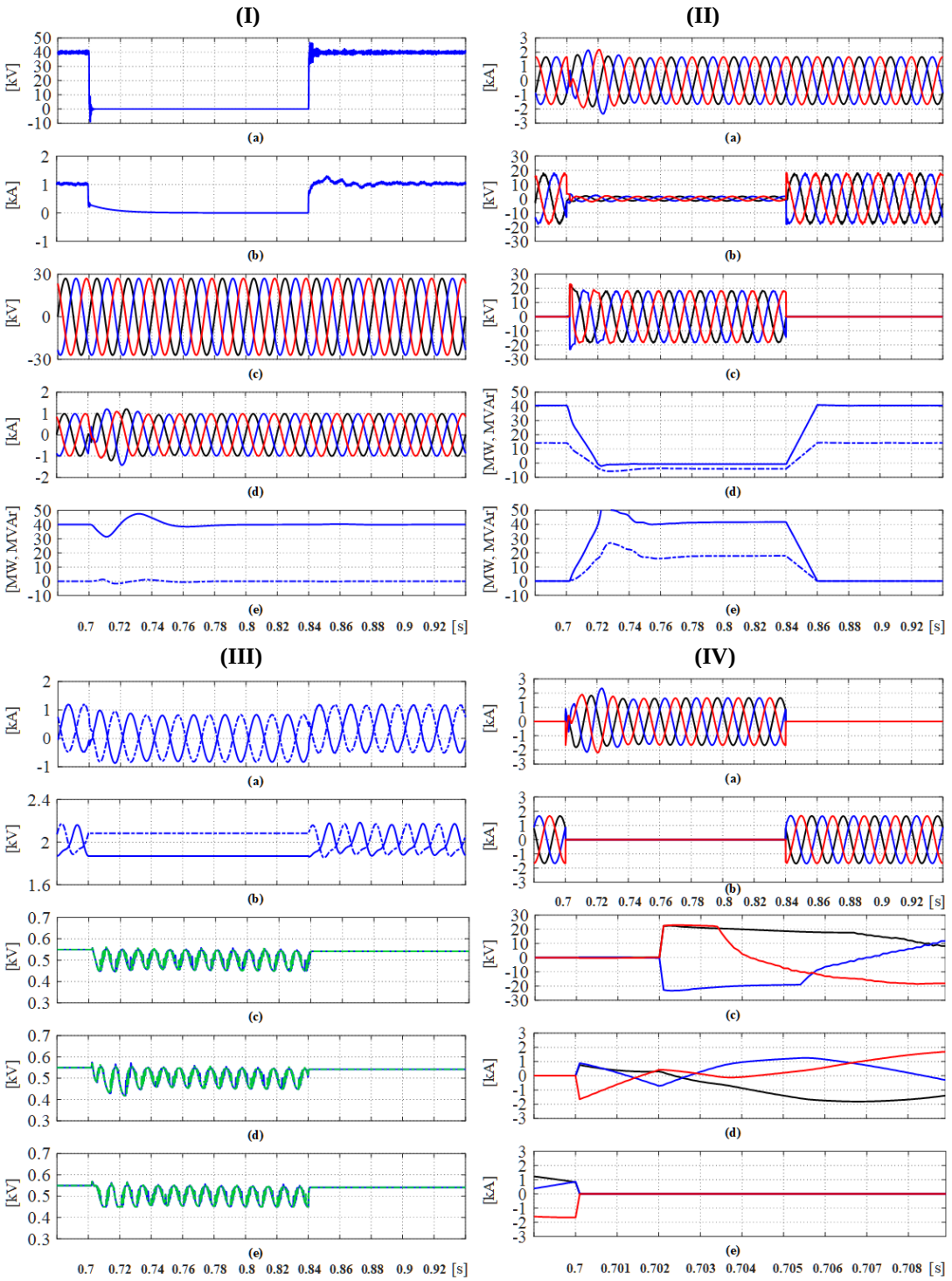

Fig. 4-11. USG-based T-MMC with energy storage integration in the dc fault case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

4.5.2 AC Fault Case

Fig. 4-12-I to IV demonstrate the performance of the TSG-based T-MMC with energy storage system integration, during an ac fault. A solid short-circuit ac fault (phases A and B) occurs at 0.7s, and the T-MMC based ESS eliminates the PCC negative sequence current components and smooths the dc power, as shown in Fig. 4-12-I(a)-(e). Stages I and II operate simultaneously, and Stage-II absorbs a portion of the active power from Stage-I to match the power imbalance, see Fig. 4-12-II. Stage-I arm currents increase with the ac bus current, whereas the SCs within the Stage-II FB-SMs charge to store the dc power, as shown in Fig. 4-12-III. Fig. 4-12-IV shows the thyristor-commutation process (700μs duration is required), whereas Stage-II FB-SMs change from the bypassed mode to the active mode.

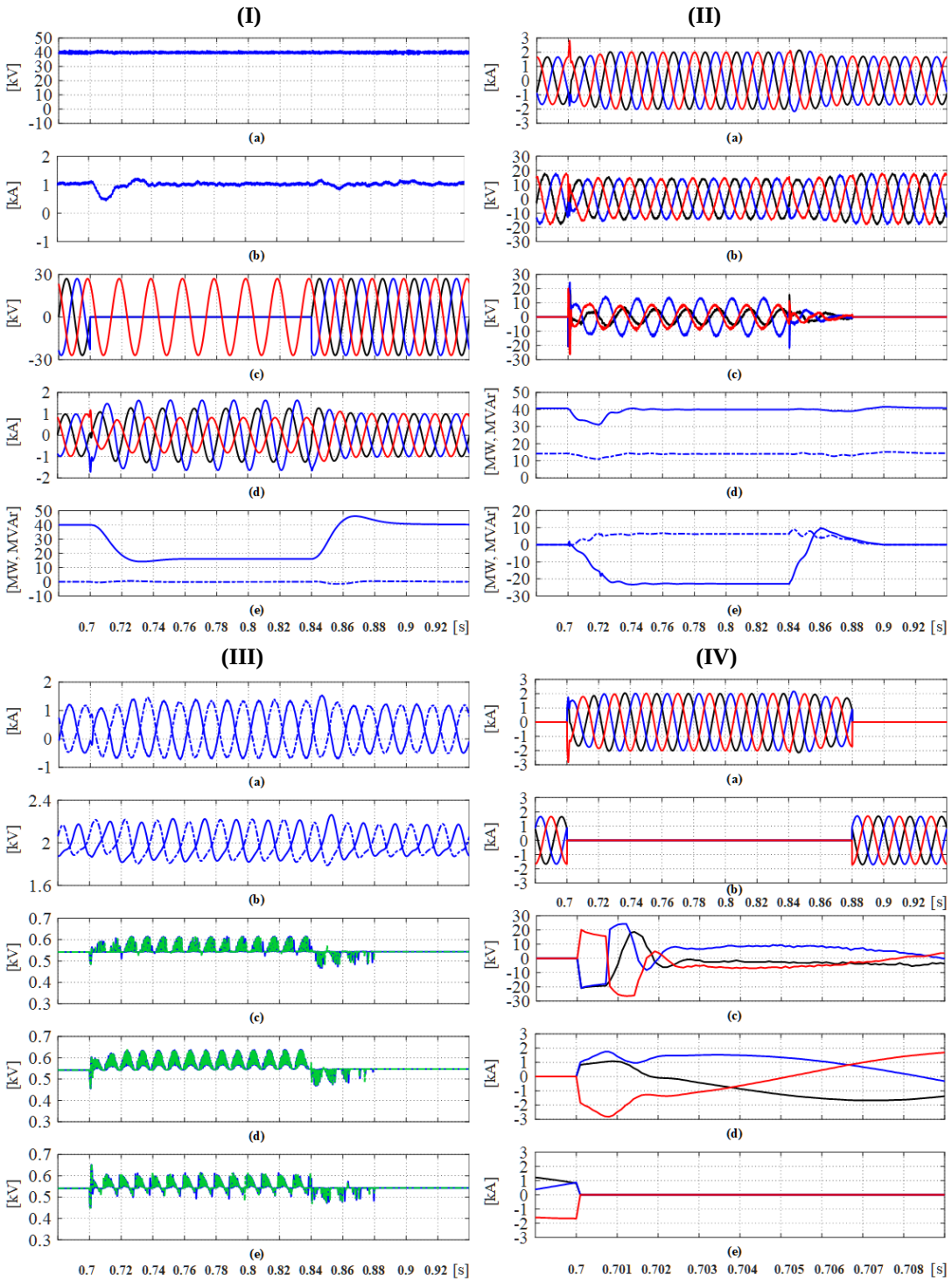

Fig. 4-12. TSG-based T-MMC with energy storage integration in the ac fault case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

Fig. 4-13-I to IV demonstrate the performance of the USG-based T-MMC with energy storage system integration, during an ac fault. A solid short-circuit ac fault (phases A and B) occurs at 0.7s, and the T-MMC based ESS eliminates the PCC negative sequence current components and smooth the dc power, as shown in Fig. 4-13-I(a)-(e). Stages I and II operate simultaneously, and Stage-II absorbs a portion of the active power from Stage-I to match the power imbalance, see Fig. 4-13-II. Stage-I arm currents increase with the ac bus current, whereas the SCs within the Stage-II FB-SMs charge to store dc power, as shown in Fig. 4-13-III. Fig. 4-13-IV shows the UFBS-commutation process (2ms duration is required), whereas the Stage-II FB-SMs change from the bypassed mode to the active mode.

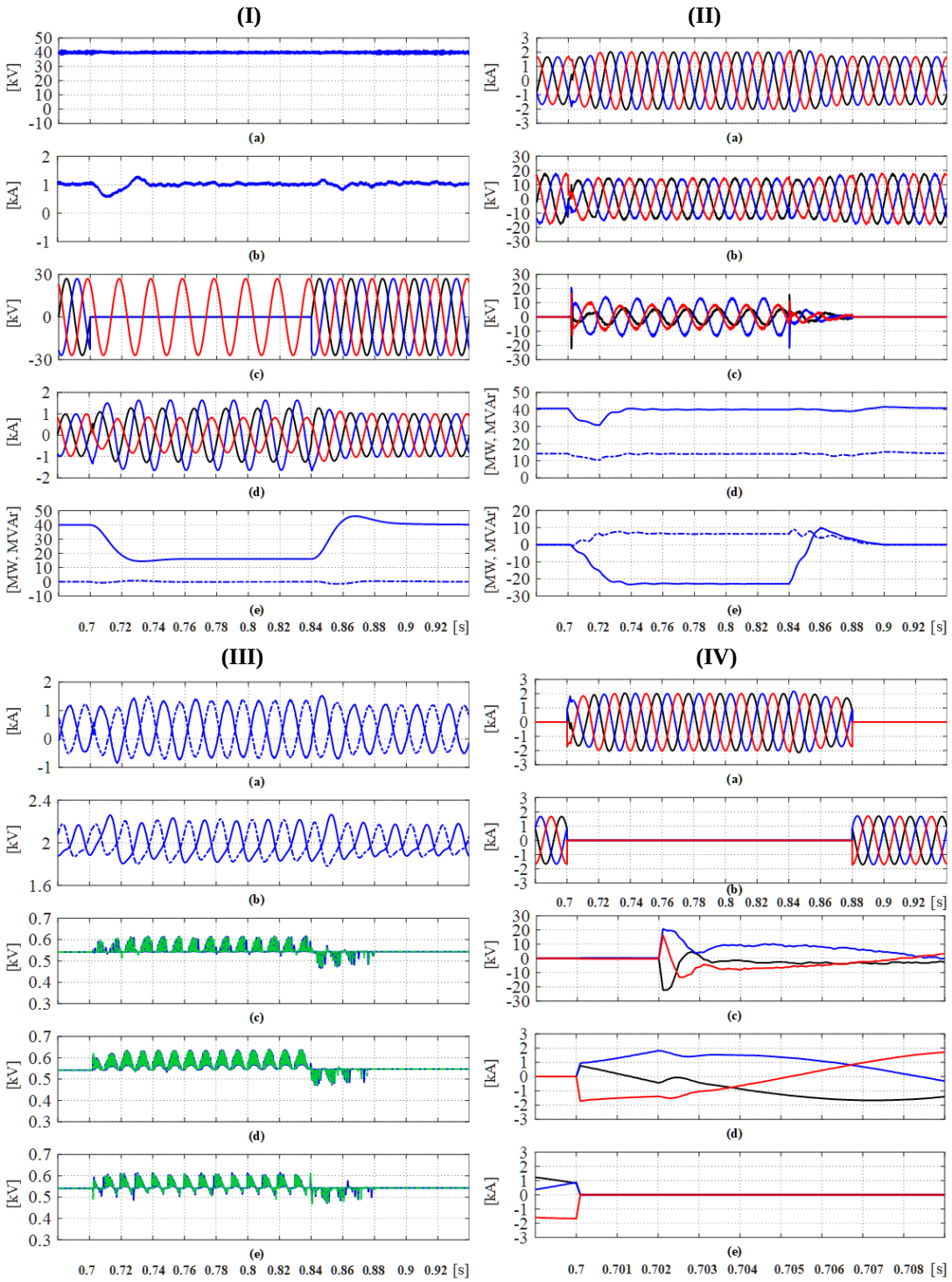

Fig. 4-13. USG-based T-MMC with energy storage integration in the ac fault case: (I-a) T-MMC dc-side voltage, (I-b) T-MMC dc-side current, (I-c) PCC voltage, (I-d) PCC current, (I-e) PCC *P* and *Q* in solid and dash lines respectively, (II-a) T-MMC ac-side current, (II-b) Stage-I ac-side voltage, (II-c) Stage-II output voltage, (II-d) Stage-I *P* and *Q* in solid and dash lines respectively, (II-e) Stage-II *P* and *Q* in solid and dash lines respectively, (III-a) Phase-A Stage-I arm currents, (III-b) Phase-A Stage-I arm average capacitor voltages, (III-c) Phase-A Stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-d) Phase-B stage-II FB-$SM_{1\&2}$ capacitor voltages, (III-e) Phase-C stage-II FB-$SM_{1\&2}$ capacitor voltages, (IV-a) Stage-II FB-SM path current, (IV-b) Stage-II bypass path current, (IV-c) Stage-II output voltage, (IV-d) Stage-II FB-SM path current, and (IV-e) Stage-II bypass path current.

4.6 Experimentation

The prototype of the TSG-based T-MMC with energy storage integration in chapter three establishes the advanced features of active/dc power support in dc/ac fault cases.

4.6.1 DC Fault Case

Before the dc fault occurs, the T-MMC operates in the normal mode with Stage-II bypassed by thyristors for higher efficiency, see Fig. 4-14(e)-(h). The dynamics in Fig. 4-14(a)-(d) illustrate that ac-side active power injection continues when the dc voltage collapses.

In Fig. 4-14(e)-(h), Stage-II is activated and starts generating ac voltage after the commutation process, whereas Stage-I arms are bypassed with only reactive power consumption. During the dc fault, no dc offset exists within the Stage-I arm current, and the HB-SMs are bypassed, with constant capacitor voltages, see Fig. 4-14(i) and (l). Also, the integrated SCs partially discharge, to provide the required ac side power, see Fig. 4-14(j) and (k).

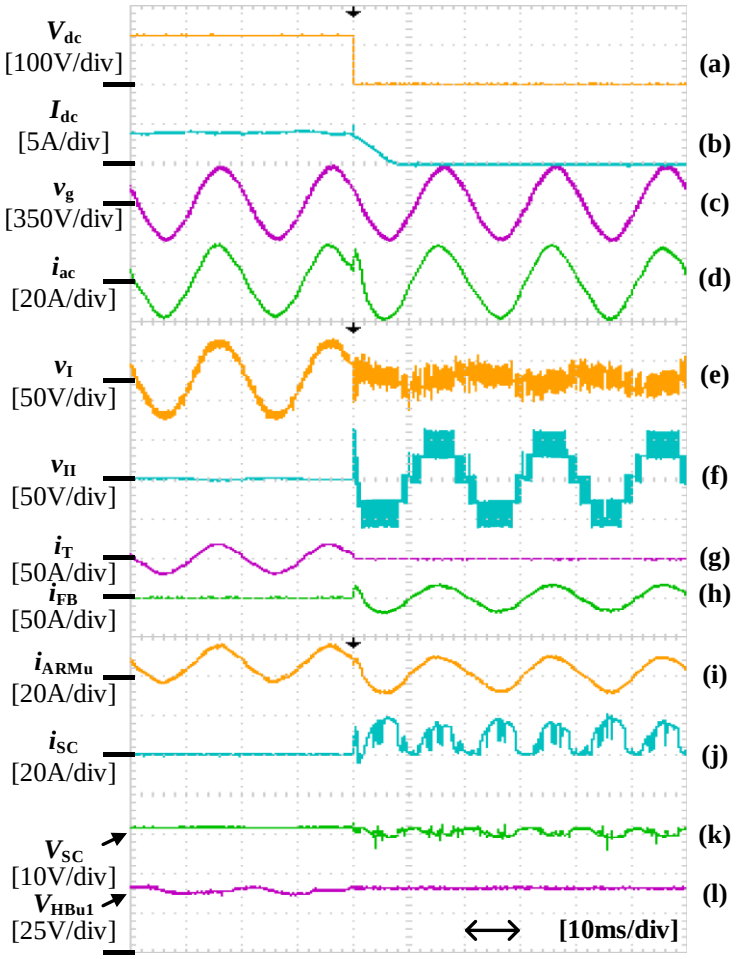

Fig. 4-14. Waveforms of T-MMC based ESS in the dc fault case.

4.6.2 AC Fault Case

The T-MMC shifts from the normal mode (Stage-II is bypassed) to a double stage active mode when the ac fault occurs, see Fig. 4-15(e)-(h).

After successful commutation, Stage-II generates ac voltage and compensates the active power from Stage-I. DC power remains after a transient period despite the faulty ac grid, see Fig. 4-15(a)-(d). Stage-I continues operating, with upper arm current and an SM voltage shown in Fig. 4-15(i) and (l). Also, the integrated SCs within Stage-II FB-SMs charge during the ac fault, absorbing the active power, see Fig. 4-15(j) and (k).

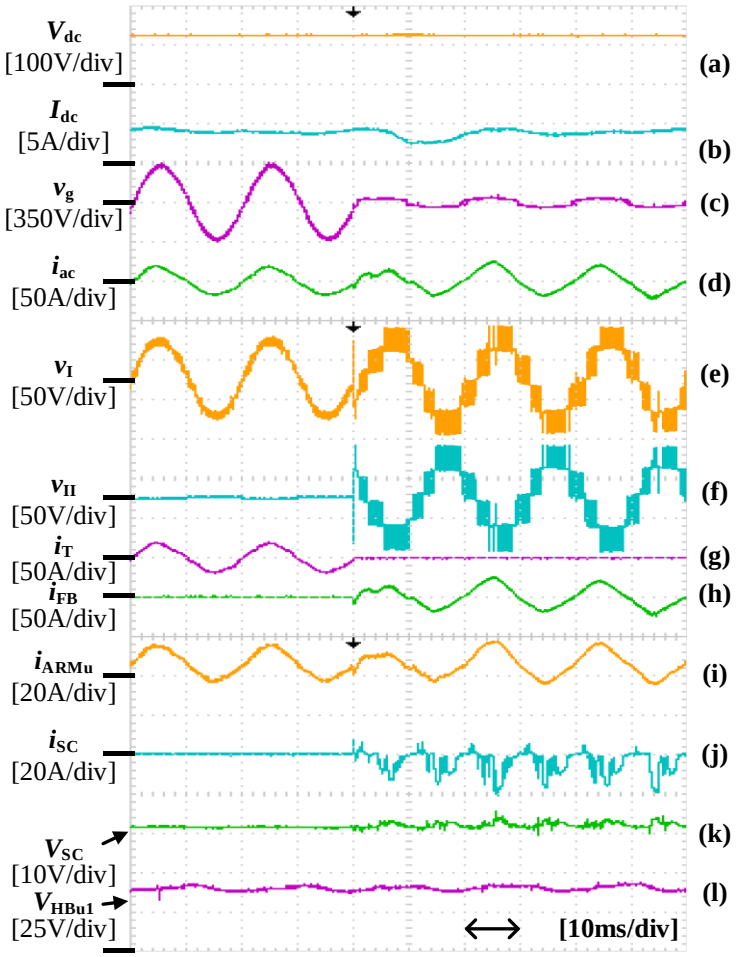

Fig. 4-15. Waveforms of T-MMC based ESS in the ac fault case.

4.7 Summary

This chapter investigated energy storage integration into the T-MMC, mainly in an effort to minimize the power disruption between a dc grid and ac grids that host power converters during ac and dc network faults. The T-MMC based energy storage system can not only increase converter inertia but can maintain continuous power transmission during faults. Functions and performance were elaborated in this chapter, with simulation and experimental verification.

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Chapter 5

T-MMC Based Multi-Terminal DC System

In this chapter, a multi-terminal dc system (MTDC) based on the T-MMC is studied. Background of the current dc network is discussed, and characteristics of the T-MMC based dc system (with and without ESS integration) during ac and dc faults are elaborated. Taking advantage of the high reliability and flexibility of the T-MMC (with energy storage integration), enhanced system ac and dc fault ride-through performance can be realized. Simulation results of a multi-terminal HVDC system confirm its feasibility, therein illustrating the desirable features of the T-MMC based dc system.

5.1 Background

The controllability and cost-effectiveness that multi-terminal MVDC and HVDC transmission systems offer to future power systems (particularly, for large power exchange and maximum utilization of renewable energy reserves over wide geographical areas) are the main drivers that attract research interest in all aspects of voltage-source converters (VSCs) [1]. Considering its significant advantages, the modular multilevel converter (MMC) has become the topology of choice in MVDC and HVDC applications [2]-[3]. However, resiliency to ac and dc faults remains important for reliable MTDC network operation.

MMCs are known for the resilience to symmetrical and asymmetrical ac faults, but the collapse of power transfer with the ac grid during ac faults can create significant disturbances on the dc side, viz., over/under voltage and transient power flow. Such over/under voltage could lead to the unintended triggering of station protection systems. Some solutions such as the telecommunication-based protection, frequency modulation techniques, and the installation of dc choppers have been investigated to mitigate the impact of ac faults on the dc side [4]. But none fully addresses the mentioned technical challenges.

Generally, dc fault impact present major technical barriers that hinder dc system interconnection and penetration of MTDC grids into critical and backbone power corridors of large power systems. The use of unipolar cells makes the HB-MMC vulnerable to dc faults. Therefore, additional measures (such as protective thyristors to divert some of the fault currents from the freewheeling diodes) are used to extend the time the dc fault can be sustained before dc circuit breaker isolation [5]. The FB-MMC and its variants (such as the mixed-cell MMC) have the ability to stop or control fault currents during the dc fault [2], [6]-[8]. Other converters such as the alternate arm converter (AAC) [9] and hybrid cascaded MMC [10], [11] and its two-level version [12], are proposed to block the dc fault. However, as mentioned, these converters suffer from either relatively high semiconductor conduction losses or arm current commutation issues, which hinders their adoption in practical systems. Another attractive protection approach with lower losses is dc breakers to interrupt the dc current and isolate the fault point within a few milliseconds [13]-[15]. Generally, converter and breaker topologies, which offer dc fault blocking and fault current control, prioritize converter semiconductor switch protection and provision of ac grid reactive power support during dc faults.

Also, such approaches could lead to zero dc/active power transfer between the dc and ac grid throughout the fault duration. And the impact of active power mismatch due to sudden dc power transfer drop on the frequency and first swing angular stability of connected ac power systems will be exacerbated by declining system inertia, as a large number of synchronous generators are deemed to be displaced by converter-based renewable energy generation. Thus, the ESS, which are able to balance the power across systems, is increasingly required by robust dc systems for the sake of reliability and security. As articulated in the previous chapters, the T-MMC and the T-MMC based ESS are especially applicable for system development due to their attractive features. Thus, a system-level solution based on such, are presented herein.

5.2 System Configurations and Features

In order to provide a global solution, this chapter proposes a T-MMC (with ESS) based MTDC grids to achieve enhanced ac and dc fault ride-through capabilities. Both isolation of the fault side and uninterruptable power flow of the normal side can be

achieved. Thus, the major motivation is to incorporate T-MMC based ESS into a dc system, to act as a fault isolator and power buffer. Fault isolators are for fault cases, whereas power buffers can provide/absorb active powers to/from the connected ac grids when the dc voltage collapses during a dc fault; and sink/source dc powers when one or more host ac grid is subjected to an ac fault. Thus, the negative impact of an ac/dc fault on the transient stability of connected dc/ac grids, particularly, sudden power mismatch, is avoided.

Depending on the adopted configuration for each station, the T-MMC based system offers one or more of the following features:

- *Resiliency against dc faults:* Each station within the system is capable of preventing the ac grid from contributing fault current to the fault dc side;
- *Resiliency against ac faults:* Each station can provide reactive power support during solid symmetrical and asymmetrical ac faults as expected in all grid codes;
- *Uninterruptable power transmission:* With the T-MMC based ESS, the dc power and ac active power are decoupled. As a result, stability and reliability of the connected ac/dc grids are improved as the loss of dc/active power due to dc/ac faults do not lead to power transmission interruption or attenuation;
- *Flexible implementation of ESS integration:* The separation of EMs from the HB-MMC SMs and the introduction of the independent Stage-II make integrating the ESS into MVDC and HVDC systems easier, without extra circuitry for voltage matching. Additionally, grounding of the ESS becomes feasible;
- *High efficiency:* The on-demand feature of the T-MMC Stage-II is technically attractive as the station is basically as efficient as a conventional HB-MMC during normal operation; and
- *AC grid support:* The structure is able to greatly enhance frequency and voltage support for the host ac grid by operating the T-MMC Stages simultaneously.

5.3 Autonomous Control for System Operation

For T-MMC based stations, autonomous operation is needed to facilitate seamless transition between normal and fault modes within the dc system. All T-MMC stations are equipped with active and reactive power control loops. The active and reactive power controllers generate direct and quadrature reference currents for the positive sequence inner current controller that define the references for the positive sequence modulation signals. The negative sequence current controller suppresses the negative sequence current to zero and generates the negative sequence modulation signals. An extra dc voltage controller is added as the outer loop of the station that controls the system dc link voltage. To facilitate seamless transition between the various control modes, anti-windup and power limitations are incorporated. Thus, for different operating modes, the control system manipulates the stages seamlessly, facilitating ac/dc fault ride-through, uninterruptable power transmission, and boost operation (extended active and reactive power control range).

Hereafter, the major operation cases and control considerations are:

- *Normal Mode:* During normal operation, Stage-II remains in an idle state with all FB-SMs bypassed to increase station efficiency. This mode is similar to conventional HB-MMC station operation, which achieves ac/dc power exchange;
- *AC Fault Mode:* When an ac fault is detected for a tied ac system, Stage-I of the relevant T-MMC retains its active power demand unchanged to minimize the transient dc power flow in the system dc side. After current commutation, the on-demand ESS is activated to limit the ac current contribution to the ac fault and participate in power balancing between Stage-I and ac grid (and suppresses the negative sequence current in asymmetrical fault cases). As a result, HB-MMC control is modified to basic load-angle control, and the ESS compensates the depressed grid voltage to exchange active power with Stage-I and ac grid. Also, simultaneous operation can be utilized for long-term reactive power boost for ac voltage support and short-term active power boost for inertial response and primary frequency support;

- *DC Fault Mode:* When a dc fault is detected, the HB-SMs of Stage-I are blocked and bypassed as described previously. After ac current commutation, Stage-II is activated to take control of the PCC current and exchange active and reactive power with the ac grid. Thus, the ac side does not experience noticeable active and reactive power imbalance. Also, the dc fault current diminishes rapidly in the dc side. During the dc fault, all T-MMC stations of the MTDC system must be switched to the dc fault mode to avoid interruption of the active and reactive power exchanged with their host ac grids; and
- *Higher-Level Energy Management:* As the ESS charges/discharges (depending on the station operation mode) during the ac/dc fault, to ensure sufficient power support duration in fault cases, ac/dc fault probability information from the power system operators is needed to optimize the on-demand stored energy of the ESS.

5.4 Simulation Study

Fig. 5-1 shows a dc grid with three T-MMC based terminals (I, II and III), used to assess the technical viability of the proposed system structure, with the system parameters displayed in Table 5-1. The symmetrical monopole interconnection is adopted with the lumped parameter model of dc lines. The converter station of terminals I, II and III are modelled by UTG-based T-MMCs. Terminal I regulates the dc voltage V_{dc} at 80kV, while II and III control their active powers exchanged with ac grids II and III respectively. The positive direction of active and reactive power is assumed to be from the dc side to ac sides. All three terminals maintain rated capacitive reactive power references. Quantitative substantiation of the beneficial claims, with regard to boost operation and uninterruptable active/dc power in ac and dc fault cases, is presented based on MATLAB/Simulink time-domain simulations.

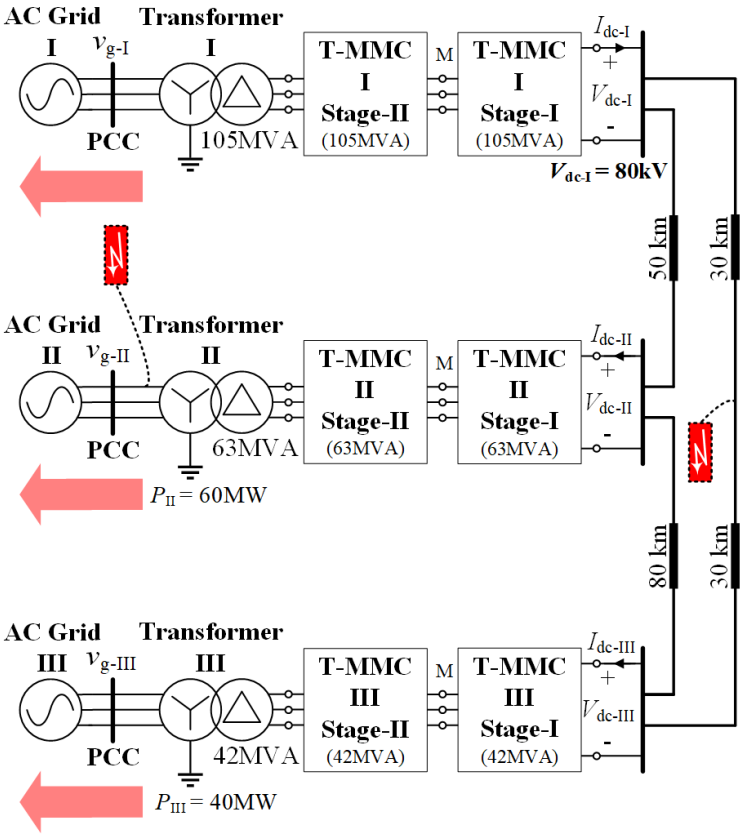


Fig. 5-1. Simulated three-terminal dc grid.

Table 5-1. Simulation parameters.

	Parameters	Rating
DC side	DC line inductance (uH/km)	11
	DC line resistance (mΩ/km)	220
	DC line capacitance (nF/km)	11
AC side	L-L rms voltage v_g (kV)	66
	Transformer ratio	40/66
	Frequency (Hz)	50
	Transformer leakage (pu)	0.18
	Transformer resistance (pu)	0.01
Stage-I	SM number per arm N_{HB}	40
	Arm inductance (pu)	0.19
	HB-SM capacitance-I (mF)	8.3
	HB-SM capacitance-II (mF)	5
	HB-SM capacitance-III (mF)	3.3
Stage-II (ESS)	SM number per UTG F	10
	UTG number per leg M	4
	Transformer turning ratio K	1:2
	Transformer leakage (pu)	0.18
	Nominal voltage of EMs (V)	600
	Storage capacity I (kWh)	161
	Storage capacity II (kWh)	97
	Storage capacity III (kWh)	64
	EM I internal resistance (mΩ)	42
	EM II internal resistance (mΩ)	71
	EM III internal resistance (mΩ)	106

5.4.1 AC Grid *Q*-Support Case

This subsection demonstrates ac grid support capability of the proposed system, in which station II exploits the reactive power capabilities of both stages by ramping up its reactive power output beyond the possible range of the conventional HB-MMC. The maximum capacitive reactive power limit of station II is established by increasing the reactive power outputs until the ac current limit (1.2pu) is reached. Simulation results with station II operating in this boost mode are presented in Fig. 5-2 and Fig. 5-3.

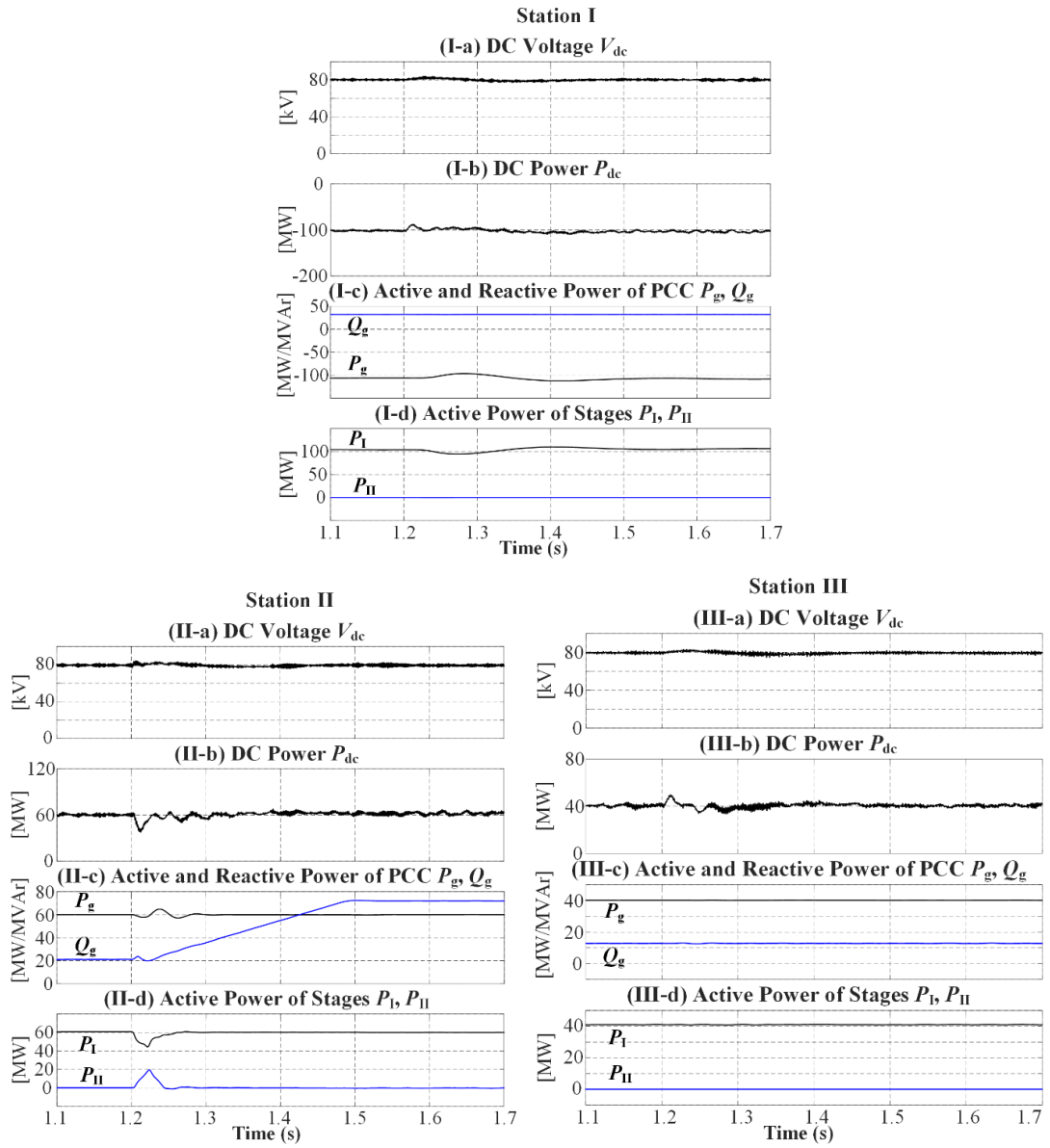


Fig. 5-2. Simulation waveforms of the station I-III with station II in ac grid *Q*-support mode.

Fig. 5-2 II (a)-(d) show that station II starts increasing its grid reactive power at t = 1.2s from 20MVAr until the ac current hits the limit, where the reactive power output reaches the maximum of +75MVAr approximately, whereas its rated active power is unchanged. Waveforms in Fig. 5-2 I and III show that except for a minor disturbance for a short period after boost mode initiation, operation of stations I and III remains unaffected.

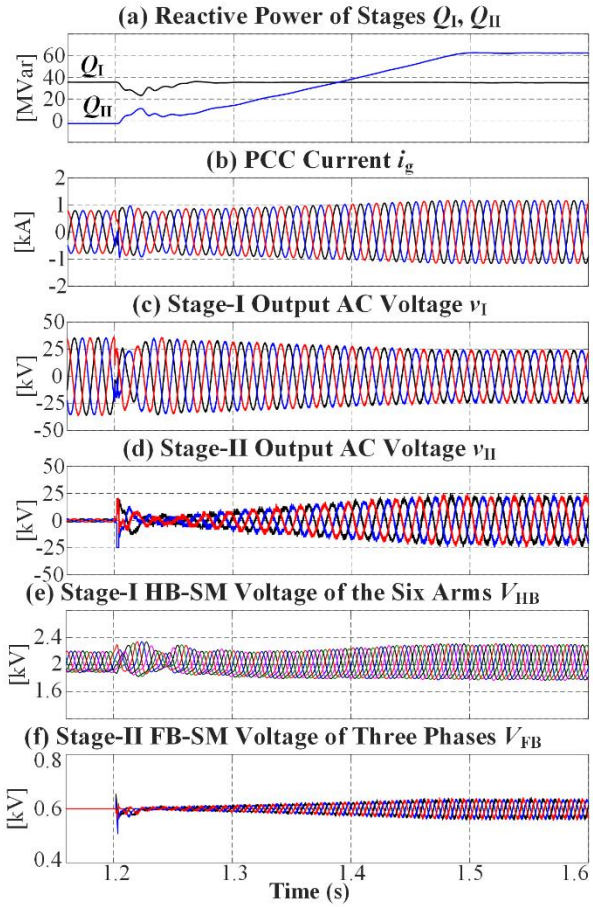


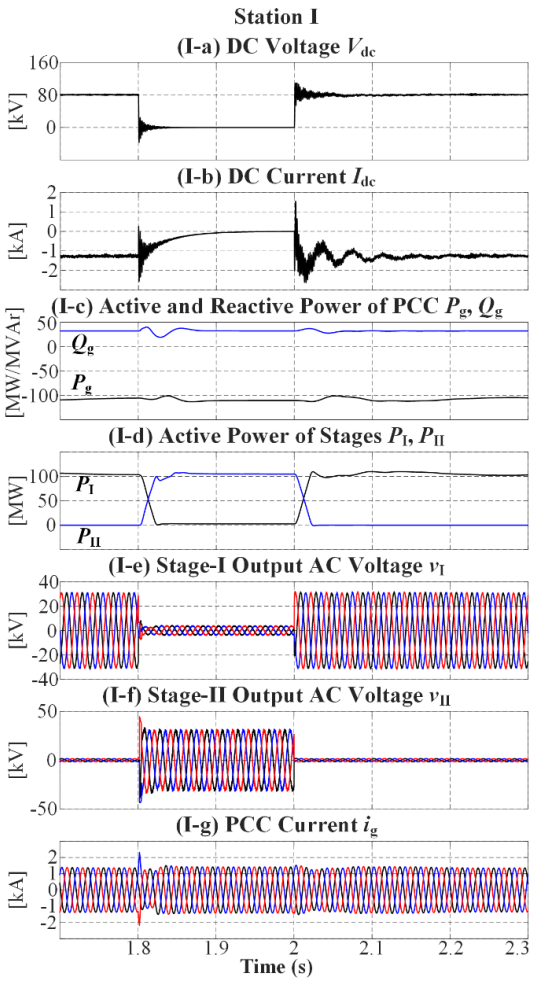
Fig. 5-3. Other waveforms of the station II with station II in boost mode.

Fig. 5-2 II (c) and (d) and Fig. 5-3(a) indicate that before initiation of the boost mode, Stage-I of station II contributes the entire reactive power exchanged with ac grid II (Q_g) plus the reactive power consumption of the transformers. Fig. 5-3(a) shows the reactive power contributions from the stages of station II, revealing that significant ac voltage boost is facilitated by Stage-II. Fig. 5-3(b)-(d) show the PCC current and ac voltages of the stages. The grid current reaches its limit while significant modulation index margin remains unexploited for both stages. Also, voltage stresses on the switching devices and EMs of station II remain controlled, see Fig. 5-3(e) and (f). As the Stage-II contributes zero active power while boosting the reactive power capability of the proposed structure, this operation is not time-limited.

5.4.2 DC Fault Case

Fig. 5-4 displays simulation results for a temporary solid pole-to-pole dc short circuit fault between terminals I and III as indicated in Fig. 5-1.

The dc fault is initiated at t = 1.8s and cleared at 2.0s. Waveforms (a) and (b) in Fig. 5-4 show the dc-side voltages and currents of stations I, II and III respectively. Waveforms (c) and (d) in Fig. 5-4 present the net active and reactive power exchanged with their respective ac grids, and active powers of stations I-III stages, respectively. These results show that the stations are capable of riding-through a pole-to-pole dc short circuit fault, without interrupting the active/reactive power exchanged with their ac grids. The dc current in Fig. 5-4(b) for stations I, II and III and Stage-I arm currents in Fig. 5-4(h) for stations I, II and III confirm the dc fault current drops to zero within 5 fundamental cycles. Waveforms (c) and (d) of I, II and III in Fig. 5-4 show that the active and reactive power that converter stations exchange with their respective ac grids are unaffected by the dc fault, with the ESSs compensating for the lost dc/active powers from/into Stage-Is. Waveforms (e) and (f) in Fig. 5-4 show the sudden collapse of HB-MMC ac voltages as a result of the dc fault and the subsequent action of bypassing HB-SMs, and then converter station output ac voltages are compensated by Stage-II ac voltages. As a result, the Stage-IIs take over the control of ac grid currents and active/reactive powers, see (c)-(g) of I, II and III in Fig. 5-4.


Station I
(I-a) DC Voltage V_{dc}
160
80
0
[kV]
(I-b) DC Current I_{dc}
2
1
0
-1
-2
[kA]
(I-c) Active and Reactive Power of PCC P_g, Q_g
50
0
-50
-100
Q_g
P_g
[MW/MVAr]
(I-d) Active Power of Stages P_I, P_{II}
100
50
0
P_I
P_{II}
[MW]
(I-e) Stage-I Output AC Voltage v_I
40
20
0
-20
-40
[kV]
(I-f) Stage-II Output AC Voltage v_{II}
50
0
-50
[kV]
(I-g) PCC Current i_g
2
1
0
-1
-2
[kA]
1.8
1.9
2
2.1
2.2
2.3
Time (s)

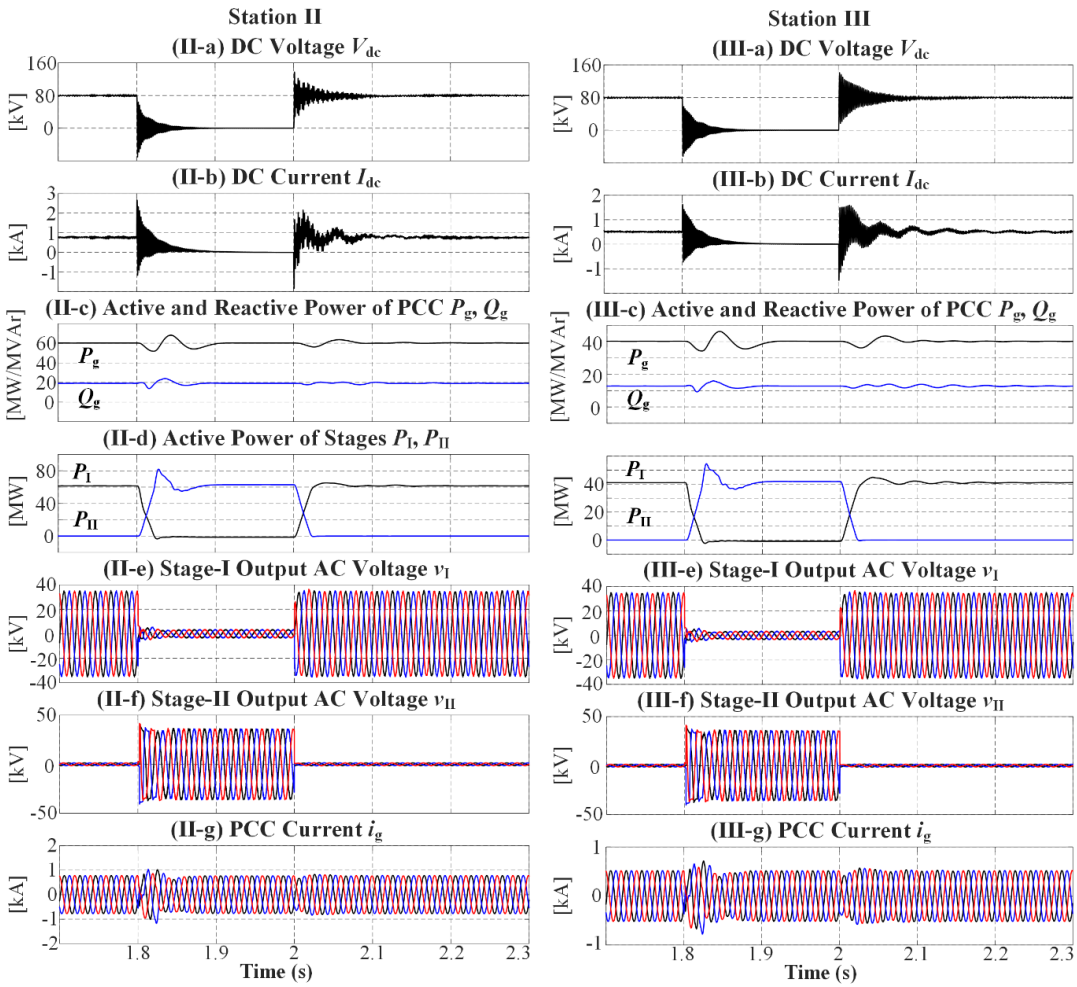


Fig. 5-4. Simulation waveforms of the station I-III with station II in the pole-to-pole dc short circuit fault case.

Thus, this dc fault case simulation reveals that T-MMCs relax dc fault requirements in a multi-terminal dc grid, through replacing conventional dc circuit breakers with dc disconnectors, without disrupting the active/reactive power exchanged with the host ac grids.

5.4.3 AC Fault Cases

This subsection examines the system resiliency against symmetrical and asymmetrical ac faults.

A temporary solid symmetrical three-phase to ground ac fault is applied at the PCC of ac grid II at t = 1.2s and cleared at 1.4s. Simulation results are presented in Fig. 5-5 and Fig. 5-6.

Waveforms (a) and (b) in Fig. 5-5 show that during the ac fault the sudden active power drop of terminal II from 60MW to 0 limits impact on the dc grid power flow, with the dc voltages and powers of terminals I, II and III exhibiting minor disturbance at fault inception and clearance instances. Waveforms (c) and (d) in Fig. 5-5 present the net active and reactive power exchanged with the ac grids, and active powers of stages of stations I, II and III. In this ac fault case, stations I and III continue in normal mode operation, where their Stage-IIs are bypassed in the idle state. Waveforms (c) and (d) of II in Fig. 5-5 show that the ESS facilitates orderly diversion of the dc power P_{dc} (or active power) of which station II is unable to inject into ac grid II due to the ac fault.

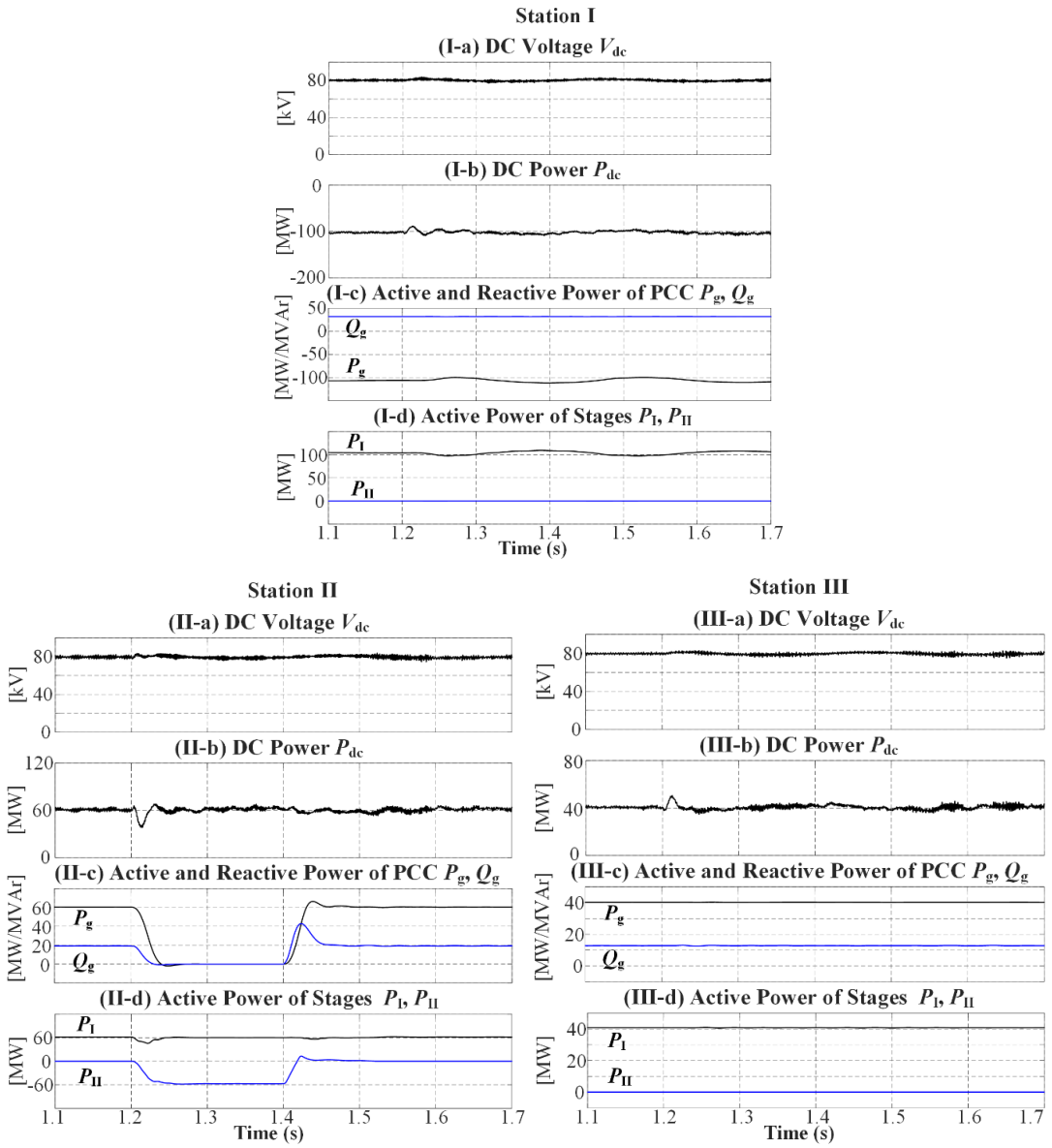


Fig. 5-5. Simulation waveforms of the station I-III with station II in three-phase short circuit solid ac fault case.

Fig. 5-6(a)-(d) show simulation waveforms of the PCC voltage and current, and ac voltages contributed by station II stages. This simulation assumes that the maximum over-current capability of each station is limited to 1.2pu. Fig. 5-6(a) and (b) show that the converter station with the proposed concept is capable of injecting maximum current into the fault ac grid as expected, with a 2ms commutation process after the ac fault at t = 1.2s. Fig. 5-6(c) and (d) reveal that Stage-II is idle, and its ac voltage and active/reactive power contributions start at fault inception and gradually cease after fault clearance. Thus, the ESS is able to sink rated active power during the ac fault,

while limiting the ac current contribution to the fault grid as expected from any VSC, without excessive over-voltage in the dc network. Also, voltage stresses on converter switches, passive components and EMs remain regulated, see Fig. 5-6(e) and (f). To ensure seamless transition from the ac fault to post-fault, Stage-II bypass after fault clearance is delayed by 5 cycles (100ms) to enable natural reduction to its contribution to the total output ac voltage and active/reactive power, as shown in Fig. 5-6(c), (d) and (f).

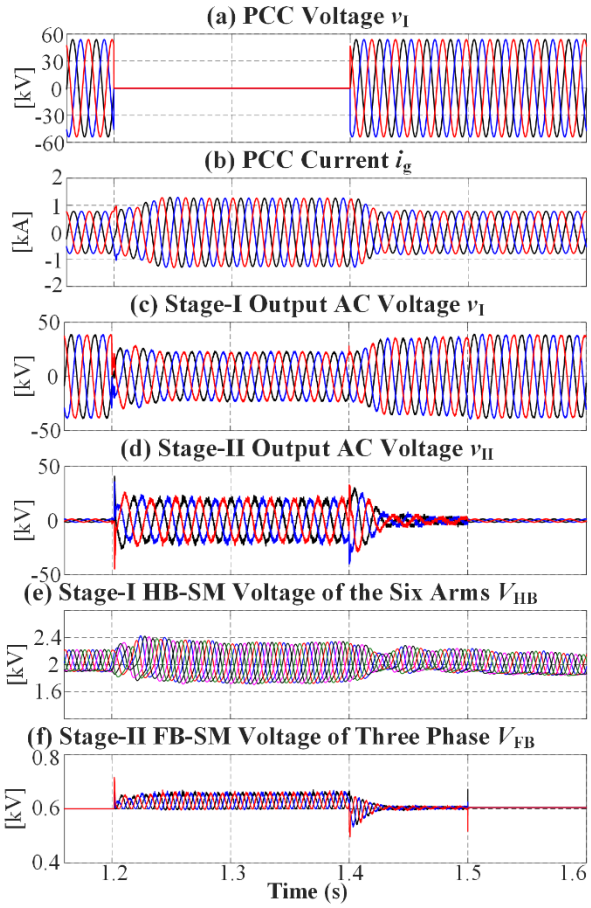


Fig. 5-6. Other waveforms of the station II with station II in three-phase short circuit solid ac fault case.

System resiliency to the asymmetrical ac fault is further examined, where station II is subjected to a temporary solid single-phase to ground ac fault at the PCC of ac grid II at t = 1.2s and cleared at 1.4s. Simulation results are presented in Fig. 5-7 and Fig. 5-8.

Waveforms (a) and (b) of I, II and III in Fig. 5-7 show that during the ac fault, station II active power drops from 60MW to 48MW, whereas the dc voltages and powers of

terminals I, II and III have small disturbance at fault inception and clearance instances. Waveforms (c) and (d) in Fig. 5-7 present the active and reactive power exchanged with the tied ac grids, and active powers of stations I, II and III stages. In this ac fault case, stations I and III continue operation with Stage-IIs bypassed in the idle state. Station II ESS absorbs a portion of the dc power P_{dc} (or active power) that station II cannot inject into ac grid II due to the fault, see Fig. 5-7 II (c) and (d).

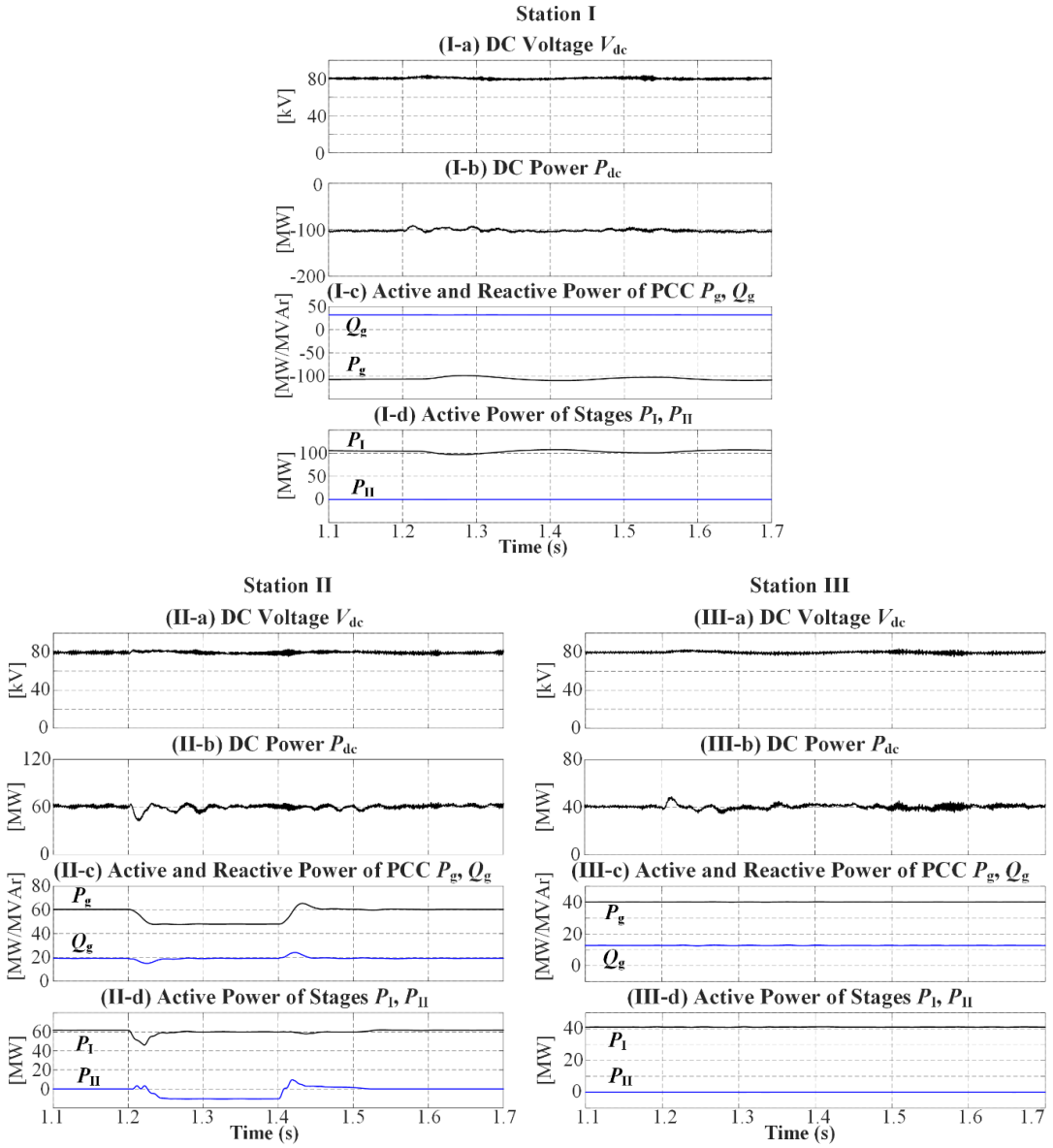


Fig. 5-7. Simulation waveforms of the station I-III with station II in single-phase short circuit solid ac fault case.

Fig. 5-8(a)-(d) show simulation waveforms of the PCC voltage and current, and ac voltages contributed by the stages of station II. Fig. 5-8(a) and (b) show that station II

suppresses the negative sequence current, with a 2ms commutation process after the ac fault inception. Fig. 5-8(c) and (d) reveal that Stage-II remains idle during the pre-fault period, contributing near zero ac voltage and power. Its ac voltage and active/reactive power contributions start at fault inception and gradually cease after fault clearance. Participation of station II ESS to sink active power during the single-phase ac fault prevents substantial disturbance in dc power flow. In addition to active or dc power balancing, Fig. 5-8(b)-(d) show that the ESS functions as a series active power filter that injects negative sequence voltage, to suppress the negative sequence current and present balanced three-phase ac voltage to the Stage-I. Also, voltage stresses on converter switches, passive components and EMs remain regulated, see Fig. 5-8(e) and (f). Seamless transition from the ac fault to the post-fault condition is realized by delaying Stage-II bypass to enable natural diminishing of its contribution to the synthesis of the total output ac voltage and the active/reactive power, as shown in Fig. 5-8(c), (d) and (f).

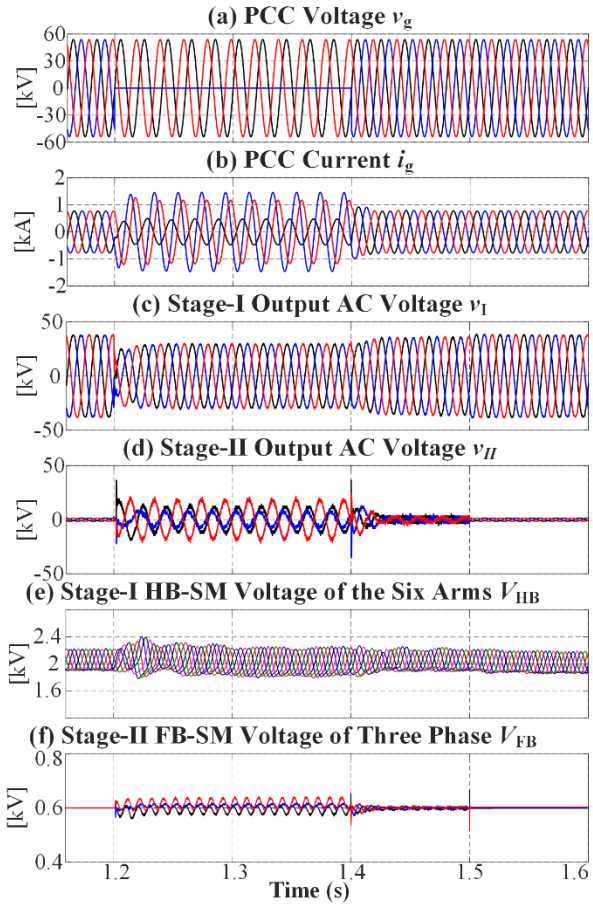


Fig. 5-8. Other waveforms of the station II with station II in single-phase short circuit solid ac fault case.

In summary, the ac fault case simulation indicates that the multi-terminal dc grid can minimize the impact of an ac fault on the dc side, including, elimination of dc link voltage variations and minimization of transient dc power flow.

5.5 Summary

This chapter has presented the T-MMC based station that employs energy storage system technology to improve ac and dc fault ride-through performance in a multi-terminal HVDC grid. Operating philosophies of the proposed structure were explained, with the effectiveness in ac and dc fault cases validated on a three-terminal HVDC system, using time-domain simulation. The proposed structure helps decouple the active power at the point of common coupling from the dc power. The occurrence of a dc fault will not lead to noticeable disruption of active/reactive power exchanged with the ac grids. Also, the concept minimizes the dc power transient within the dc

grid during ac faults; therefore, no significant transient dc voltage or power flow is observed in the dc link.

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Chapter 6

Conclusion

This chapter draws conclusion from the research, summarizes the major contributions of this research, and the envisaged research expectation on the topic of this thesis.

6.1 General Conclusions

The research focused on the design and analysis of a modular multilevel converter (MMC) for secure systems in ac/dc conversion applications; whereas various technical aspects including configuration, operation and control were discussed with simulation and experimentation substantiation.

Firstly, this study reviewed the MMC technical background and characteristics. Mainstream topologies, typical submodules, and operating principles were presented; while attributes and limitations were analysed.

Chapter 2 presented comprehensive analysis and assessment of different proportional resonant (PR)-based control schemes proposed to regulate the internal dynamics, with the consideration of passive component tolerances, different energy and voltage based control schemes under various conditions were analysed. It was observed that without vertical voltage balance control unequal passive component values in the upper and lower arms of the same phase-leg may cause unbalanced fundamental currents in the arms, unequal dc voltage across the arms, and fundamental oscillation in the common-mode currents that lead to fundamental frequency ripple in the dc link current. Simulation supported the statement and theoretical analysis explained the mechanism; hence, the control scheme is necessary for the nullification of arm voltage difference and/or suppression of oscillation caused by capacitive/inductive asymmetry between arms of the same phase-leg. Different voltage and energy based control schemes were assessed; and two SM-level capacitor voltage balancing approaches were considered. A specific method for directly suppressing the fundamental oscillation in the common-

mode and dc link current was proposed. Simulation results showed the effects of different control schemes, and supported the effectiveness of proposed method in suppressing the fundamental current ripple caused by tolerances of upper and lower arm passive elements. Experimental results from a single-phase MMC prototype confirmed the presented theoretical discussion and simulation.

Albeit offering desirable features and significant advantages, different MMC topologies have their limitations, and these were analysed in this study. In light of the analysed weaknesses of existing MMCs, a novel T-type MMC (T-MMC) was proposed in Chapter 3. This converter showed a new set of features suitable for ac/dc conversion application and secure system construction. The features include dc fault tolerance, high normal operation efficiency, increased ac-side output range, and feasible energy storage integration. T-MMC topologies, including basic and practical versions, were introduced; basically, the T-MMC consists of two stages, namely Stage-I (an HB-MMC) and Stage-II (an FB-SM chain-link). Design principles and fundamental operation modes were analysed. In order to minimise normal operation losses, the Stage-II bypass mechanism uses thyristor-SM groups (TSGs) and UFBS-SM groups (USGs). The necessary commutation approaches were considered. Control system for the operation of stages and regulation of the internal variables was given. The characteristics of the proposed converter compared with other mainstream MMC topologies were presented: the T-MMC offers some attractive features over other MMCs, such as an increased ac voltage and dc fault tolerant capability. The T-MMC involves a larger number of component especially the Stage-II. Simulation and experimental results of various operation cases established the effectiveness of the proposed T-MMC in terms of fault tolerance and reactive power support. Furthermore, motivation and background of integrating energy storage into MMCs were presented in this study, and it was observed that the feasible energy storage integration feature of the T-MMC can provide benefits to secure systems. Hence, Chapter 4 presented T-MMC based energy storage systems (ESSs), which can provide reliable active (and reactive) power support to the connected ac and dc side systems, especially in certain fault cases. Topological configurations of the energy storage integrated T-MMC and the attractive features in different additional operation modes were presented. In addition, this chapter provided sizing and other practical considerations of the

integrated energy storage elements (ESEs). The commutation schemes and control approaches were illustrated and discussed for active power (stage-of-charge) regulation of ESEs. Simulation and experimentation showed that the T-MMC based ESS can operate to compensate power in both ac and dc fault cases. This advantage of the proposed T-MMC significantly increases the security of its connected systems.

Technical background of multi-terminal dc (MTDC) networks was introduced; as the major issue preventing the development of MTDC networks is dc fault. Given the dc fault tolerant capability and uninterrupted power support of the T-MMC (integrated with ESEs), Chapter 5 investigated the T-MMC based dc network. Firstly, the T-MMC based system was studied in terms of configuration and features in the MTDC scenarios. With energy storage integration, the dc system can present desirable operation characteristics, while autonomous control of the converter station was proposed. A developed three-terminal dc system simulation model was used to demonstrate operational features. It was shown that the T-MMC based terminal station can be used in a dc network, where both dc and ac faults can be tolerated and overall system security is improved.

6.2 Author's Contribution

The contributions and significance presented in this thesis can be summarised as:

- It has been established that unequal SM capacitance in the upper and lower arms of the same phase-leg (vertical asymmetry) introduces negative sequence currents into the MMC arms and appears as fundamental current in the common-mode currents; thus, causing excessive voltage ripple in the common-mode voltage, with negative sequence fundamental current tending to leak into the dc link current;
- Detailed investigation of internal control schemes reveals that a vertical voltage-based balancing controller might help suppress fundamental oscillation in the common-mode currents and dc link current in the case of vertical asymmetry of SM capacitances and arm inductances;
- A direct method for suppressing the fundamental circulating current is effective in ensuring MMC dc link current quality with worst-case passive

component asymmetry, at the expense of a marginal reduction in the modulation index control range;

- To address the trade-off between dc fault tolerance capability and high operation efficiency, a new topology named T-MMC was proposed;
- A dual-stage topology is used to allow flexible operation and provide larger output range. Thus, the T-MMC can achieve fault blocking and reactive power support during a dc fault. Also, enlarged reactive power support can be generated;
- Taking advantages of the thyristors and mechanical disconnectors, two bypassing mechanisms are integrated into the T-MMC, thereby obtaining high normal-mode operation efficiency;
- With energy storage integration, the T-MMC based ESSs can be used to provide active/dc power support and smooth sudden power changes, which is especially attractive during faults. Thus, converter fault resiliency can be increased; and
- The T-MMC can be applied in critical system scenarios, such as the development of multi-terminal dc systems. With the T-MMC (can be integrated with ESEs), grid fault ride-through capabilities are improved, while system reliability is enhanced.

6.3 Future Research Expectation

Some recommendations for future research are:

- More detailed modelling considering of the MMC internal control scheme is suggested to improve MMC internal dynamics, where small signal analysis or impedance analysis is recommended and stability aspects of the MMC with different internal control schemes are expected;
- Various applications with specific component parameters may lead to different MMC operating results. Effects of different component parameters (including internal and ac/dc side ones) on MMC internal dynamics (such as SM capacitor voltages) and external dynamics (such as magnitude of the fundamental frequency ripple) are suggested to be further investigated;

- The proposed T-MMC involves two stages, which need different control systems. Although a hierarchical control system has been proposed in this study, more precise and advanced control strategies are expected to improve the dynamics and performance of the T-MMC;
- Cost evaluation of the T-MMC is expected, based on precise T-MMC configuration and design, and practical engineering; and
- Operation efficiency of the T-MMC should be evaluated, based on adopted configuration and parameters of the selected components (such as switches, passive elements, bypassing paths, etc.).

Appendices

Appendix A. Test Rig Hardware Configurations

The components of the utilized hardware are microcontroller, HB and FB SMs, voltage and current sensors, inductors, grid-interfacing transformer, etc. Two main components are introduced.

- *Microcontroller:* The ST STM32F767ZI microcontroller, which is shown in Fig. A-0-1, is used in the experimentation. The microcontroller is designed to be responsible for sampling variables, processing algorithms, and generating gate drive signals.

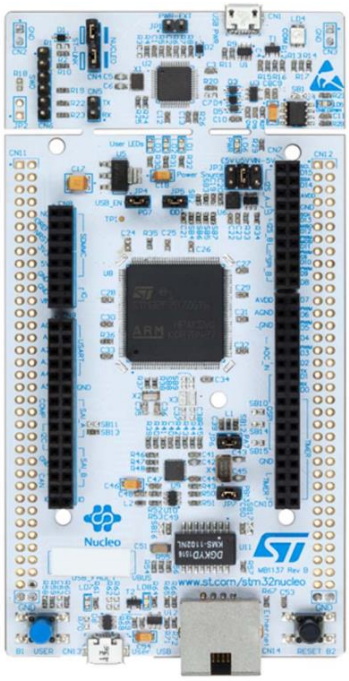

Fig. A-0-1. ST STM32 Nucleo-144 board.

The ST STM32F767ZI microcontroller has the following features:

- Core: Arm® 32-bit Cortex®-M7 CPU with DPFPU, ART Accelerator™ and L1-cache: 16 Kbytes I/D cache, allowing 0-wait state execution from embedded Flash and external memories, up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions;
- Up to 2 Mbytes of Flash memory organized into two banks allowing read-while-write;
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels;
- 2×12-bit D/A converters;
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support;
- Up to 18 timers: up to thirteen 16-bit and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input;
- All 15 timers running up to 216 MHz.

- *HB and FB SMs:* The MMC SMs are important parts as discussed. The HB-SM used in the test rig is shown as in Fig. A-0-2, where IGBTs and the gate drivers, SM capacitor voltage and SM current measurement are integrated. The FB-SM can be built similarly.

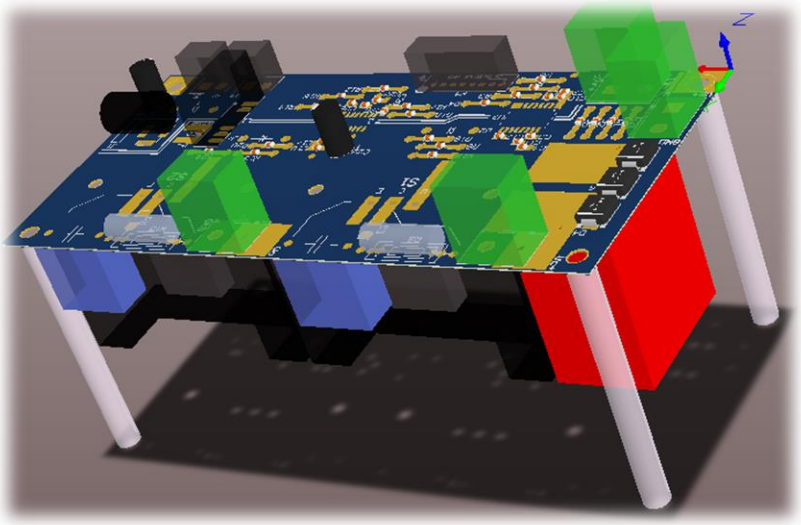

Fig. A-0-2. HB-SM PCB board 3-D model.

The part number of the used IGBT (International Rectifier) is IRG7PH35UD1PBF-EP, which has the following features:

- Low $V_{CE\ (ON)}$ trench IGBT Technology;
- Low Switching Losses;
- Square RBSOA;
- Ultra-Low V_F Diode;
- 1300V_{pk} Repetitive Transient Capacity.

Appendix B. Sample Code for Microcontroller

- MMC internal control function:

```
void MMCInternalControl(void)
{
 Vdc = 120;
 VarmRef = Vdc*2*1024*10/40/33; // 3*Vc[V]*2[V]/40[V]*1024/3.3[V]
 /* V arm*/
 Varm_1U = Vc_1U[0] + Vc_1U[1] + Vc_1U[2];
 Varm_1L = Vc_1L[0] + Vc_1L[1] + Vc_1L[2];
 /* V sum */
 Notch_Filter_2w_In[0] = Varm_1U + Varm_1L;
 Notch_Filter_2w(Notch_Filter_2w_In, Notch_Filter_2w_Out, 0, 1024*5);
 VarmSum = Notch_Filter_2w_Out[0];
 /* V dif */
 Notch_Filter_w_In[0] = Varm_1U - Varm_1L;
 Notch_Filter_w(Notch_Filter_w_In, Notch_Filter_w_Out, -N*1024, N*1024);
 VarmDif = Notch_Filter_w_Out[0];
 /* Circulating Current Suppression 100Hz */
 if(1)
  {
   PR_Icir_2w_In[0] = 0 - ((Iarm_1U + Iarm_1L)>>1);
   PR_Icir_2w(PR_Icir_2w_In, PR_Icir_2w_Out, -400, 400);
   PR_Icir_Out = PR_Icir_2w_Out[0];
  }
 /* Internal Balancing */
 uint16_t InternalControlMode = 1;    /*  0: Icir Suppression
 if(InternalControlMode == 0)
  {
   PIR_Icir_CommonMode = PR_Icir_Out;
  }
 if(InternalControlMode == 1)
  {
   /* Vsum Controller */
   V_Sum_In[0] = 2*VarmRef - VarmSum;
   V_Sum(V_Sum_In, V_Sum_Out, -(400<<2), (400<<2));
   PIR_Icir_CommonMode = (V_Sum_Out[0]>>2) + PR_Icir_Out;
  }
 if(InternalControlMode == 2)
  {
   /* Vsum Controller */
   V_Sum_In[0] = 2*VarmRef - VarmSum;
   V_Sum(V_Sum_In, V_Sum_Out, -(400<<2), (400<<2));
   /* Vdif Controller */
   V_Dif_In[0] = 0*2*1024*10/40/33 - VarmDif;
   V_Dif(V_Dif_In, V_Dif_Out, -200, 200);
   PIR_Icir_CommonMode = ((V_Sum_Out[0] - V_Dif_Out[0]*VmmcSin/400)>>2) +
PR_Icir_Out;
  }
 if(InternalControlMode == 3)
  {
   /* Vsum Controller */
   V_Sum_In[0] = 2*VarmRef - VarmSum;
   V_Sum(V_Sum_In, V_Sum_Out, -(400<<2), (400<<2));
   /* Vdif Controller */
   V_Dif_In[0] = 4*2*1024*10/40/33 - VarmDif;
   V_Dif(V_Dif_In, V_Dif_Out, -200, 200);
```

```
   PIR_Icir_CommonMode = ((V_Sum_Out[0] - V_Dif_Out[0]*VmmcSin/400)>>2) +
PR_Icir_Out;
  }
 if(InternalControlMode == 4)
  {
   /* Vsum Controller */
   V_Sum_In[0] = 2*VarmRef - VarmSum;
   V_Sum(V_Sum_In, V_Sum_Out, -(400<<2), (400<<2));
   /* w E */
   PR_Icir_w_In[0] = 0 - ((Iarm_1U + Iarm_1L)>>1);
   PR_Icir_w(PR_Icir_w_In, PR_Icir_w_Out, -200, 200);
   PIR_Icir_CommonMode = V_Sum_Out[0] + PR_Icir_w_Out[0] + PR_Icir_Out;
  }
 /* Limit */
 if(PIR_Icir_CommonMode>=400)PIR_Icir_CommonMode = 400;
 if(PIR_Icir_CommonMode<=-400)PIR_Icir_CommonMode = -400;
}
```

- Sorting-Based SM capacitor voltage balancing function:

```
void Sorting(uint16_t *Vc, uint16_t Length, uint16_t *IncInd)
{
 uint16_t i,j, temp1, temp2;
 uint16_t VcTemp[3];
 VcTemp[0] = Vc[0];VcTemp[1] = Vc[1];VcTemp[2] = Vc[2];
 for(j=0; j<Length; j++)
 for(i=0; i<Length-1-j; i++)
 if(VcTemp[i] > VcTemp[i+1])
  {
   temp1 = VcTemp[i];
   VcTemp[i] = VcTemp[i+1];
   VcTemp[i+1] = temp1;
   temp2 = IncInd[i];
   IncInd[i] = IncInd[i+1];
   IncInd[i+1] = temp2;
  }
}
```

- Modulation and limitation:

```
/* MMMC Modulation -- Injecting Common-mode Component & Limitation */
if((Ref_1U_Sin - (PIR_Icir_CommonMode/2)) <= 0) Ref_1U = 1;
else if((Ref_1U_Sin - (PIR_Icir_CommonMode/2)) >= 120*354/50) Ref_1U =
T_Carrier*N;
else Ref_1U = (Ref_1U_Sin -
(PIR_Icir_CommonMode/2))*(T_Carrier*N)/(120*354/50);

if((Ref_1L_Sin - (PIR_Icir_CommonMode/2)) <= 0) Ref_1L = 1;
else if((Ref_1L_Sin - (PIR_Icir_CommonMode/2)) >= 120*354/50) Ref_1L =
T_Carrier*N;
else Ref_1L = (Ref_1L_Sin -
(PIR_Icir_CommonMode/2))*(T_Carrier*N)/(120*354/50);

/* ESS Modulation -- Direct AC Output */
if((Ref_2_Sin + ESS_CommonMode) <= 0) Ref_2 = 1;
else if((Ref_2_Sin + ESS_CommonMode) >= (120*354/50)) Ref_2 =
T_Carrier*N2time2-1;
else Ref_2 = (Ref_2_Sin +
ESS_CommonMode)*(T_Carrier*N2time2)/(120*354/50);
```

- PD-PWM example for one timer (Timer 8):

```
void TIM8_CC_IRQHandler(void)
{
 /* USER CODE BEGIN TIM8_CC_IRQn 0 */
 /* PWM-PD */
  if(((TIM8->CR1&(1<<4))>>4) == 1)   //Counter is downcounter
   {
    OnNum_1L = OnNum_Done_1L + 1;
   }
  else                               //Counter is upcounter
   {
    OnNum_1L = OnNum_Done_1L;
   }
  if(OnNum_1L > N)OnNum_1L = N;

  for(uint16_t i=0;i<N;i++)
   {
    SMState_1L[i] = 0;
   }

  if(SortingGoing == 1)
   {
    if(Iarm_1L >= 0)
    {
     for(uint16_t i=0;i<OnNum_1L;i++)
      {
       SMState_1L[IncInd_1L_Old[i]] = 1;
      }
    }
    else
    {
     for(uint16_t i=0;i<OnNum_1L;i++)
      {
       SMState_1L[IncInd_1L_Old[N-1-i]] = 1;
      }
    }
   }
   else
    {
     if(Iarm_1L >= 0)
      {
       for(uint16_t i=0;i<OnNum_1L;i++)
        {
         SMState_1L[IncInd_1L[i]] = 1;
        }
      }
     else
      {
       for(uint16_t i=0;i<OnNum_1L;i++)
        {
         SMState_1L[IncInd_1L[N-1-i]] = 1;
        }
      }
    }

 /* GPIO Signals */
  if(VmmcModEN==1)
   {
    if(SMState_1L[0] == 1)  {HAL_GPIO_WritePin(GPIOD, GPIO_PIN_5,
GPIO_PIN_SET);}
```

```
    else            {HAL_GPIO_WritePin(GPIOD, GPIO_PIN_5,
GPIO_PIN_RESET);}
    if(SMState_1L[1] == 1)  {HAL_GPIO_WritePin(GPIOD, GPIO_PIN_6,
GPIO_PIN_SET);}
    else            {HAL_GPIO_WritePin(GPIOD, GPIO_PIN_6,
GPIO_PIN_RESET);}
    if(SMState_1L[2] == 1)  {HAL_GPIO_WritePin(GPIOD, GPIO_PIN_8,
GPIO_PIN_SET);}
     else            {HAL_GPIO_WritePin(GPIOD, GPIO_PIN_8,
GPIO_PIN_RESET);}
   }

 /* DutyCycle Update */
  if(((TIM8->CR1&(1<<4))>>4) == 0)  //Counter is upcounter, Which means
One Cycle is Finished.
   {
    OnNum_Done_1L = Ref_1L / T_Carrier;

    if((Ref_1L - OnNum_Done_1L*T_Carrier) < MinDutyCycle)TIM8->CCR1 =
MinDutyCycle;
    else if ((Ref_1L - OnNum_Done_1L*T_Carrier) > MaxDutyCycle )TIM8->CCR1
= MaxDutyCycle;
    else TIM8->CCR1 = (Ref_1L - OnNum_Done_1L*T_Carrier);
   }


 /* USER CODE END TIM8_CC_IRQn 0 */
 HAL_TIM_IRQHandler(&htim8);
 /* USER CODE BEGIN TIM8_CC_IRQn 1 */

 /* USER CODE END TIM8_CC_IRQn 1 */
}
```

Appendix C. List of Figures

Appendix D. List of Tables

Appendix E. Author's Publications

- **Shuren Wang**, Grain P. Adam, Ahmed M. Massoud, Derrick Holliday and Barry W. Williams, "Analysis and Assessment of Modular Multilevel Converter Internal Control Schemes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Volume: 8, Issue: 1, March 2020.

  Abstract - Adoption of distributed submodule (SM) capacitors in a modular multilevel converter (MMC) necessitates complex controllers to ensure the stability of its internal dynamics. This paper presents comprehensive analysis and assessment of different proportional resonant (PR)-based control schemes proposed to stabilize the internal dynamics and ensure ac and dc sides power quality of the MMC within a dc transmission system. With the consideration of passive component tolerances, different energy- and voltage-based control schemes under various conditions are analysed. It has been established that without vertical voltage balance control, unequal passive component values in the upper and lower arms of the same phase leg may cause: unbalanced fundamental currents in the arms, unequal dc voltage across the arms, and fundamental oscillations in the common-mode currents that lead to fundamental frequency ripple in the dc-link current. The theoretical analysis that explains this mechanism is presented, and is used to show that vertical voltage balancing is necessary for the nullification of arm voltage difference and suppression of odd oscillations caused by capacitive/inductive asymmetry between arms of the same phase leg. Simulations support the theoretical analysis and the effectiveness of voltage balancing in ensuring correct operation, independent of tolerances of the MMC passive elements, and operating conditions. A new direct method for elimination of fundamental oscillations in the common-mode and dc-link current is proposed. Experimental results from a single-phase MMC prototype validate the presented theoretical discussions and simulations.

- **Shuren Wang**, Grain P. Adam, Ahmed M. Massoud, Derrick Holliday and Barry W. Williams, "Strategies for Decoupling Internal and External Dynamics Resulting From Inter-Arm Passive Component Tolerances in HVDC-MMC," in *IEEE ECCE-2019*, Sep. 2019.

  Abstract - Modular Multilevel Converter (MMC) performance may be adversely affected by passive component tolerances, such as submodule capacitance and arm inductance variations. Depending on control strategies, the differences in equivalent capacitances and/or inductances of the upper and lower arms of one phase-leg can cause unequal power distribution between upper and lower arms. Assuming passive component tolerances ranging between ±10%, this paper presents a comprehensive assessment of the internal/external coupling effects due to the passive component tolerances within one phase-leg, under the control of common MMC balancing methods. A novel control strategy is proposed to suppress the fundamental component that arises in the dc-link current due to such tolerances, and its effectiveness is demonstrated via simulation and experimentation. The investigation shows that voltage-based common and differential mode balancing control provides effective ac offset suppression while the proposed method offers superior performance in terms of dc-link fundamental current ripple suppression.

- **Shuren Wang**, Khaled H. Ahmed, Grain P. Adam, Ahmed M. Massoud and Barry W. Williams, "A Novel Converter Station Structure for Improving Multi-Terminal HVDC System Resiliency against AC and DC Faults," *IEEE Trans. Industrial Electronics*, Volume: 67, Issue: 6, June 2020.

  Abstract - In an effort to minimize the power disruption between a dc grid and ac grids that host power converters during ac and dc network faults, this paper proposes a novel converter station structure to improve ac and dc fault ride-through performance of the multi-terminal HVdc grid. The proposed structure consists of two independent ac and dc interfacing circuits, which are a half-bridge modular multilevel converter and a cascaded H-bridge

(CHB) based energy storage system. Taking the advantages of high controllability and flexibility of the independent CHB converter and ease of integrating energy modules, a decoupled power relationship between the ac and dc sides is achieved, which is important for enhancing ac and dc fault performance. Operation of the proposed converter station under normal conditions and during ac and dc faults is explained, with the control system presented. Simulation validation of the proposed structure on a three-terminal HVdc grid confirms the enhanced performance, including the continuous operation during ac and dc faults with negligible power transfer disruption.

- Abdel-Aziz A. A., Khaled H. Ahmed, **Shuren Wang**, Ahmed M. Massoud and Barry W. Williams, "A Neutral-Point Diode-Clamped Converter with Inherent Voltage-Boosting for A Four-Phase SRM Drive," *IEEE Trans. Industrial Electronics*, Volume: 67, Issue: 7, July 2020.

  Abstract - This paper proposes a new asymmetric neutral-point diode-clamped (NPC) multilevel converter for a four-phase switched reluctance motor drive. The inbuilt NPC clamping capacitors are used for both voltage level clamping and also as dc rail voltage-boosting capacitors to increase the output power of the motor, particularly for high-speed electric vehicle applications. The new converter allows regenerative energy to be recovered back to the dc supply for rapid machine braking, thus increasing overall drive efficiency. Analysis of the different modes of converter operation, along with design equations for sizing the voltage-boosting capacitors, are detailed. The effect of capacitance on boost voltage and increased motor base speed is presented. Simulation and experimental results confirm the effectiveness of the proposed converter.

- **Shuren Wang**, Ahmed M. Massoud and Barry W. Williams, “A T-Type Modular Multilevel Converter,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019. (Early access).

  Abstract - This paper proposes a novel modular multilevel converter (MMC) named ‘T-type MMC’ (T-MMC) for reliable, controllable and efficient performance in energy conversion applications. Circuitry configurations and control structures are presented, with respect to fundamental and additional functions. The T-MMC topology consists of two solid-state power stages (Stage-I and Stage-II), which are coordinated for ac and dc fault tolerance, increased ac-side voltage synthesis, etc. Energy storage elements can be integrated into the submodules. As a result, the T-MMC based energy storage system can not only increase system inertia but maintain continuous power transmission during faults. A thyristor forced-commutation technique facilitates actively-controlled utilization of symmetrical thyristors in the conduction path; thus T-MMC normal-mode operation losses can be equivalent to those of the conventional half-bridge MMC. Simulation and experimentation demonstrate the performance of the T-MMC.