

**High yield and accuracy transfer printing of
micron-scale opto-electronic devices for volume
manufacturing**

PhD Thesis

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Abstract

Increasing demands on the performance and scale of opto-electronic systems for displays and on-chip photonics require the integration of a diverse range of photonic materials at micron scales. The primary goal of this thesis is to develop and test a novel transfer printing technique for the large-scale micro-assembly of integrated optoelectronic devices, with a particular focus on microLED displays. Initial work involved designing and fabricating large arrays of membrane devices in a cleanroom laboratory, emphasizing the necessity for these devices to be suspended to facilitate the transfer printing process. The fabrication steps for both miniLED ($100 \times 100 \mu m^2$) and microLED ($30 \times 30 \mu m^2$) arrays are detailed, followed by the introduction of a new automated transfer method based on continuous roll transfer printing. The experimental setup, along with critical process parameters, is analysed comprehensively, showing how this continuous process enables the parallel transfer of thousands of devices in less than 30 seconds. A new membrane device design compatible with the roller process is introduced. In order to test this new method, as well as to inspect the individual position of thousands of devices, an automated assessment method is developed. High accuracy and throughput in the automated spatial registration of micron-scale devices on planar chips are demonstrated, utilizing simple optical microscopy tools to assess yield, spatial pitch, and rotation. By using this method, an entire chip of 1 *cm* size consisting of 4,000 devices in total, was imaged with 94 *nm* pixel resolution and mean value of $0.06 \pm 0.26 \mu m$. Following this, the continuous, single-shot roller transfer printing process was used for the large-scale hybrid integration of over 75,000 microLED devices with sub-micron relative position accuracy, maintaining array geometry with less than 1 μm deviation. This work shows the potential for hybrid materials device integration at scale, com-

patible with the well-established infrastructure and semiconductor processes developed in industrial foundry manufacturing. Additionally, a novel method for inducing and maintaining strain in silicon through physical bending is proposed. Controlled bending generates strain levels up to 0.4% that persist after removing external stress. This phenomenon is explored through a finite element mechanical model, analytical analysis and experimentally verified using electron backscatter diffraction measurements. The fabrication of the thin film silicon membranes, as well as the results of each method are presented and explained. The findings suggest significant potential for strain engineering in high-performance silicon-based technologies without the need for complex fabrication techniques.

Publications

- Margariti E., Bruckbauer J., Winkelmann A., Guilhabert B., Kumar N., Trager-Cowan C., Martin R., Strain MJ. Strain-induced modifications of thin film silicon membranes by physical bending (under review process)
- Margariti E, Quinn G, Jevtics D, Guilhabert B, Dawson MD, Strain MJ. Continuous roller transfer-printing and automated metrology of >75,000 micro-LED pixels in a single shot. *Optical Materials Express*. 2023 Aug 1;13(8):2236-50. (The paper was highlighted in the news release in Optica)
- Margariti E, Guilhabert B, Quinn G, Jevtics D, Dawson MD, Strain MJ. Continuous roller transfer-printing of QVGA semiconductor micro-pixel arrays. In 2022 IEEE Photonics Conference (IPC) 2022 Nov 13 (pp. 1-2). IEEE.
- Margariti E, Guilhabert B, Jevtics D, Dawson MD, Strain MJ. Sub-micron-accuracy automated position and rotation registration method for transferred devices. In 2021 IEEE Photonics Conference (IPC) 2021 Oct 18 (pp. 1-2). IEEE. (The paper was shortlisted for best student paper 2021)

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List of Abbreviations

μ TP	micro Transfer Printing
CF_4	Carbon Tetrafluoride
CHF_3	Trifluoromethane
Cl_2	Chlorine
N_2	Nitrogen
N_2O	Nitrous Oxide
SF_6	Sulfur Hexafluoride
SiH_4	Silane
SiO_2	Silicon Dioxide
AFM	Atomic Force Microscope
AOM	Acousto-optic Modulator
AR	Augmented Reality
BOE	Buffered Oxide Etch
BOX	Burried Oxide
CMOS	Complementary Metal Oxide Semiconductor
CRT	Cathode Ray Tube

List of Abbreviations

EBSD	Electron Back-Scatter Diffraction
FEA	Finite Element Analysis
FOV	Field Of View
GaN	Gallium Nitride
HDR	High Dynamic Range
HiSiD	Heterogeneous integration System in Display
HUD	Heads-up Display
ICP	Inductively Coupled Plasma
KOH	Pottasium Hydroxide
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MFC	Mass Flow Controller
OLED	Organic Light Emitting Diode
PDMS	Polydimethylsiloxane
PECVD	Plasma Enhanced Chemical Vapor Deposition
QVGA	Quarter Video Graphics Array
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscopy
Si	Silicon
SOI	Silicon-on-Insulator
TP	Transfer printing
VR	Virtual Reality

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In loving memory of Xristina Margariti (26-12-2021) and Nikolaos
Kessisoglou (19-05-2023). Your presence continues to inspire and guide me
every day. Forever remembered.

Chapter 0.

Chapter 1

Introduction

The thesis concentrates on developing a new transfer printing method based on continuous roll-transfer printing for the parallel transfer of thousands of devices, targeting large-scale applications such as micro-LED displays. Hence, Chapter 1 briefly describes the evolution of displays over the past years and the need for next-generation display technology. It introduces Micro-LED display technology and highlights the mass transfer challenge that currently hinders their commercialization. Competitive mass transfer methods that are currently under development are also discussed, outlining the strengths and limitations of each method.

Chapter 2 focuses on the fabrication of suspended mini and micro LED devices and the specific requirements for roll transfer. The new continuous roll-transfer printing method and experimental setup are presented. Chapter 3 introduces the development of an automated image processing inspection method for characterizing large array devices. The method is used on non-printed devices after fabrication for validation and then is applied to assess the roll-printed mini and micro LED devices for yield, positional, and rotational assessment. Chapter 4 presents another important aspect addressed in this thesis, which is the strain induced by mechanically bending thin film material, particularly focusing on strain engineering on silicon and its benefits. A method of inducing and maintaining strain on silicon membranes by physically bending them is presented. A detailed analysis is provided, including theoretical calculations, simulations, and experiments. The influence of strain on the band gap of silicon is

discussed. Finally, Chapter 5 summarizes the key findings of this thesis and proposes future work based on this research.

1.1 Heterogeneous integration for display technologies

The development of displays has been significantly influenced by the concept of heterogeneous integration, which involves the combination of dissimilar devices to enable advanced functionalities. This evolution has been driven by the need for next-generation electronics, where sensors, actuators, and display pixels interact with the local environment, leading to the development of high-performance, cost-effective, and reliable display solutions [1]. The integration of diverse materials and devices onto a single chip has demonstrated higher yield, scalability, robustness, efficiency, and manufacturability, thus revolutionizing display technologies. Furthermore, the successful realization of monolithic polychromatic emission has the potential to accelerate the development of phosphor-free white light sources, chip-scale color microLED displays, and other GaN-based optoelectronic systems and platforms [2]. An example of an heterogeneous integrated system in display can be seen in Figure 1.1, where the integration of micro displays units, computing units, storage units, sensing units and radio frequency (Rf) units is shown. Additionally, the integration of inorganic LEDs on a single wafer has the potential to overcome the current limitations of large format displays with low resolution, thus opening up new possibilities for display technology [3].

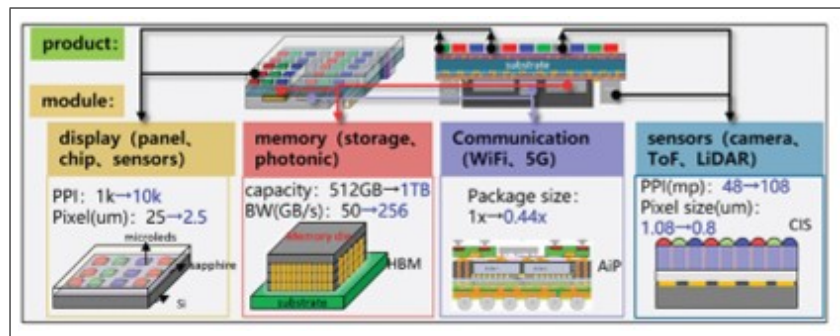


Figure 1.1: Heterogeneous integration system in display [4]

Heterogeneous integration offers a pathway to revolutionize display technologies by

enabling advanced functionalities, scalability, and enhanced performance. The integration of diverse materials and devices not only enhances the efficiency and manufacturability of displays but also opens up new possibilities for creating innovative and high-quality display solutions.

1.2 Display evolution

In recent decades, display technologies have become embedded in a myriad of devices and common applications, appearing in various forms such as televisions, tablets, smart devices, and billboards, impacting both social production activities and individuals' daily routines [5]. The evolution of display technology from cathode ray tube (CRT) to microLED displays has been a remarkable journey marked by significant advances. Initially, CRT displays were the primary means of presenting electronic information and images, revolutionizing the computer, network, and digital technology landscape [6]. The transition from CRT to microLED displays signifies a paradigm shift in display technology, offering enhanced image quality, higher contrast, wider color gamut, faster response time, and lower power consumption [7]. This evolution has been facilitated by the development of innovative technologies such as carbon nanotube-based field-emission cathodes, which have found applications in field emission displays and electron guns, contributing to the progression of display technology [8].

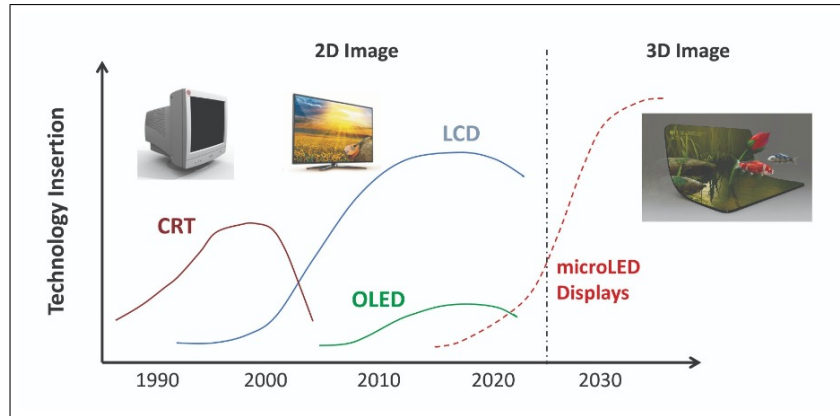


Figure 1.2: Display evolution and future expectations [9]

Figure 1.2 presents a chronological diagram of the display technology during time.

The rapid adoption of microLED technology has opened new frontiers in emission-based displays, offering unprecedented image quality and energy efficiency, thereby shaping the future of display technology [10]. As microLED displays continue to advance, the integration of artificial intelligence applications and the promise of future technological integration further underscore the dynamic and evolving nature of display technology [11]. Moreover, the realization of microLED displays has necessitated high-yield mass transfer processes for the rapid assembly of micron-scale devices onto non-native display substrates, underscoring the technological challenges and innovations associated with microLED displays [12], [13]. While LCD and OLED are displacing traditional displays, they are also opening up new applications, such as wearable devices etc. The transition has been marked by advancements in materials science, nanotechnology, and enzyme engineering, reflecting the interdisciplinary and dynamic nature of display technology evolution [14], [15], [16], [17], [18]. Here, a very brief introduction of the dominant and most important display technologies are presented.

1.2.1 Cathode Ray Tube

Initially, cathode ray tube (CRT) display technology pioneered video displays and held a dominant market position from the 1950s until the turn of the century [19]. Invented in the late 1890s, the CRT paved the way for the development of various display devices such as oscilloscopes, televisions in the 1930s, and monitors [20]. The CRT was widely used in offices and homes, serving as the platform on which the personal computer and graphical user interface were developed [21].

A cathode ray tube (CRT) display and its operation principal is presented in Figure 1.3. A CRT display operates by using an electron beam inside the tube to scan a raster of pixels line by line from left to right, starting with the uppermost line. The electron beam is emitted from the cathode, which is a crucial component of the CRT technology. The CRT display functions as an emissive display, where the electron beam excites phosphors on the screen, causing them to emit light and create the visual display. This technology has been fundamental in the development of various applications, including televisions, monitors, and oscilloscopes. The electron beam scanning process in a CRT

display is essential for creating the images on the screen. The beam is controlled by magnetic fields to move it accurately across the screen, illuminating the phosphor dots that make up the pixels of the display. The interaction between the electron beam and the phosphor coating on the screen results in the emission of light, which forms the images visible to the viewer [22]. This process allows for the rapid and precise display of information, making CRT displays suitable for a wide range of applications.

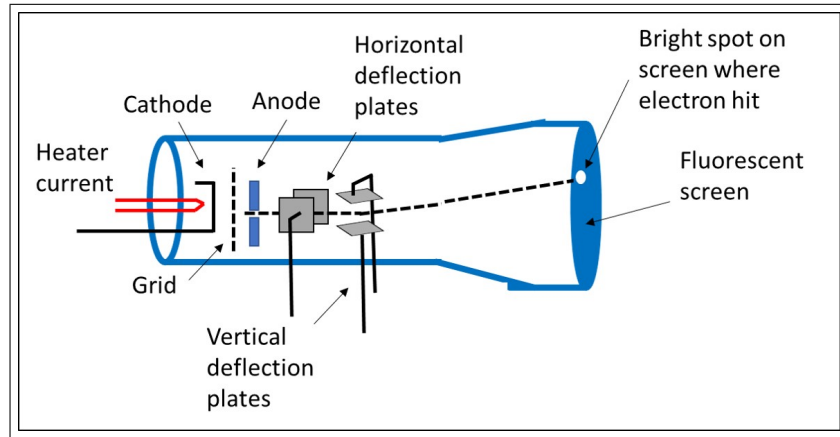


Figure 1.3: Operation principal of CRT display.

Despite the historical significance and widespread use of CRT displays, advancements in display technology have led to the decline of CRTs in favor of lighter, more energy-efficient alternatives such as liquid crystal displays (LCDs) and light-emitting diodes (LEDs). However, the principles of operation of CRT displays have paved the way for the development of modern display technologies, contributing to the evolution of visual display systems [23].

1.2.2 Liquid Crystal Display

Liquid crystal displays (LCDs) operate by manipulating the orientation of liquid crystal molecules through the application of electric currents, resulting in the modulation of light transmission. A typical cross section schematic of LCD displays can be seen in Figure 1.4. LCD technology has been pivotal in various applications, from smartphones to large TVs, due to its lightweight nature, high resolution, good color performance, and low power consumption [24].

Liquid Crystal Display (LCD) technology functions by manipulating light at the pixel level. Each LCD screen comprises a layer of liquid crystals sandwiched between two glass layers, with polarizing filters attached to each glass layer. These filters are aligned perpendicularly to each other, polarizing light in a specific direction as it passes through them. The liquid crystal molecules in an LCD are arranged in a specific manner, influenced by factors such as orientation materials and pretilt angles, which impact the display quality [25].

The pixels on an LCD screen are composed of three subpixels: red, green, and blue, arranged in a grid pattern. When an electric current is applied to a specific pixel, it affects the alignment of the liquid crystals in that pixel. These liquid crystals twist and change their orientation based on the voltage applied. As the liquid crystals twist, they either allow light to pass through or block it, depending on their orientation. This modulation of light passing through the liquid crystal layer determines the color and intensity of each pixel. By varying the intensity of the electric current applied to each subpixel, different colors can be achieved.

Most LCD screens also feature a backlight behind the liquid crystal layer to illuminate the display. The backlight emits white light, which passes through the liquid crystals and is modulated to produce the desired colors. A display controller receives digital image data and converts it into signals that control the electric currents applied to each pixel. This controller ensures that the correct colors and intensities are displayed at each pixel location. Overall, LCD technology relies on the manipulation of light and liquid crystals to create the images and colors displayed on the screen.

LCDs have also been integrated with metasurfaces for applications like information encryption, leveraging the expertise from the LCD display industry [26]. Additionally, LCD technology has been utilized in the development of heads-up displays (HUDs) for generating images with high brightness and clarity [27]. The versatility of LCDs extends to applications in virtual reality (VR) and augmented reality (AR) headsets, showcasing the adaptability of liquid crystal technology in display systems [28].

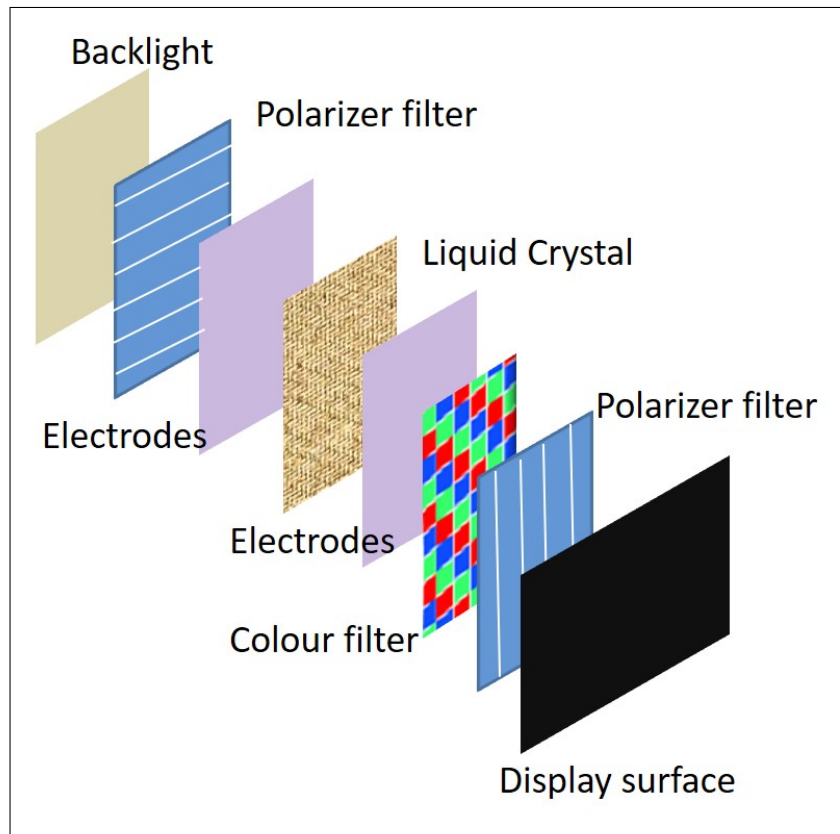


Figure 1.4: Liquid Crystal Display cross section schematic

1.2.3 Organic Light Emitting Diodes (OLED)

LED technology has evolved significantly over the past century, starting with Henry Joseph Round's observation of light emission from carborundum crystals in 1907. This initial discovery laid the groundwork for further exploration into electroluminescence, notably by Oleg Vladimirovich Losev in 1927 [29].

Throughout their history, LEDs have transitioned from costly laboratory equipment to indispensable lighting solutions, driven by innovation and sustainability. As LED technology continues to advance, its potential to shape the future of lighting remains substantial [30].

Organic light-emitting diodes (OLEDs) are a type of light-emitting diode where the emissive electroluminescent layer is a film of organic compound that emits light in response to an electric current [31]. A schematic of the fundamental structure of

OLEDs can be seen in Figure 1.5. They comprise multiple organic layers enclosed between two electrodes, typically made of glass or plastic. These layers consist of the emissive layer, conductive layers, and a substrate. The organic layers are designed to facilitate the injection and transport of charge carriers, leading to the recombination of electrons and holes in the emissive layer, resulting in the emission of light [32]. The use of different materials in the various layers of OLEDs allows for the tuning of emission spectra and the achievement of full-color displays [33]. The emissive layer is where light generation occurs, with electrons and electron holes recombining upon the passage of an electric current, releasing energy in the form of photons. This process of light emission is what produces the display's visuals. Conductive layers, such as the electron transport layer and hole transport layer, aid in the movement of electrons and electron holes to the emissive layer, ensuring efficient light emission.

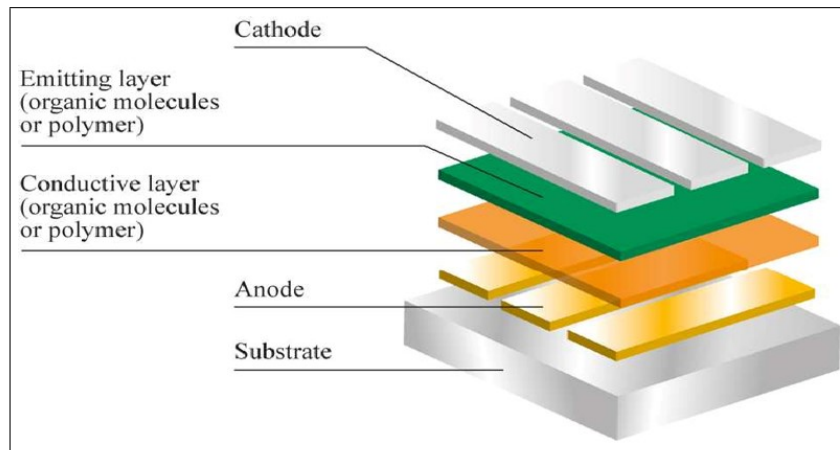


Figure 1.5: Fundamental Principle of Organic Light Emitting Displays [34]

The substrate provides structural support for the OLED layers and may include additional components like thin-film transistors (TFTs) for pixel control. OLED displays are composed of individual pixels, each containing red, green, and blue subpixels. These subpixels emit light independently, enabling precise control over color and brightness. By adjusting the intensity of the electric current passing through each subpixel, OLED displays can produce a wide range of colors. Their ability to emit their own light at the pixel level allows OLED displays to achieve vibrant colors, high contrast ratios, and wide viewing angles without requiring a separate backlight layer. The emissive behavior

of OLEDs makes them suitable for bright environments and wide-angle viewing, and they have been identified as a next-generation illumination light source due to their lightweight, flexibility, and surface illuminant properties [35], [36].

Moreover, OLED displays offer the advantage of being thin and flexible due to their inherent design. Unlike traditional LCD displays, which rely on a backlight, OLED displays do not need this additional layer, allowing for thinner and more flexible designs. This flexibility opens up possibilities for curved or even rollable display designs, expanding the range of applications for OLED technology.

The development of OLEDs has seen significant progress due to improved materials and device design. The emissive layer in OLEDs can be doped with phosphorescent materials to achieve highly efficient emission [37]. Phosphorescent OLEDs have been shown to have high theoretical quantum efficiency, making them suitable for display and lighting applications [38]. Additionally, the use of composite organic materials in OLEDs has been found to enhance performance efficiency and extend the device's lifetime [39].

1.2.4 Micro-LEDs as the next generation display

MicroLED, short for micro light-emitting diode, is an emerging display technology that is expected to revolutionize the display industry due to its numerous advantages. MicroLED technology is anticipated to be utilized in next-generation displays and various other applications due to its high luminous efficiency, high color saturation, high contrast, self-illumination, low energy consumption, long service life, and wide color gamut [40]. It is recognized as the ultimate display technology and is one of the fastest-growing technologies in the world, with applications ranging from large flat panel displays, televisions, wearable displays, virtual reality displays, to light sources for neural interfaces and optogenetics [41]. MicroLEDs are also attractive for other applications such as visible light communication, bio-imaging, and sensors [42]. MicroLED arrays, with pixel sizes less than 10 microns, are envisioned for wearable display applications, such as smartwatches, with the promise of offering high dynamic range (HDR) and high power efficiency [43].

The technology is based on Gallium Nitride (GaN) chiplets, offering exceptionally high luminance, high luminous efficiency, and a long operating lifetime compared to competing approaches such as organic light-emitting diodes [44]. High-density and fully integrated microLEDs can be used for microdisplays with sizes of 1 cm^2 and below in augmented reality applications, where high efficiency, high brightness, robustness, and degree of integration are key requirements [45]. Realizing cost-effective microLED displays requires the integration of varied processes on semiconductor wafers and display substrates, including fabrication, assembly, and interconnection of tiny components [46]. An emerging application for microLED technology is on expandable large LED screens, called tiled displays [47]. MicroLED arrays are also capable of controlling neural activity and are increasingly used in optogenetics technology [48]. Furthermore, microLEDs have the same potential for self-luminousness and the same perfect black level as OLEDs [49].

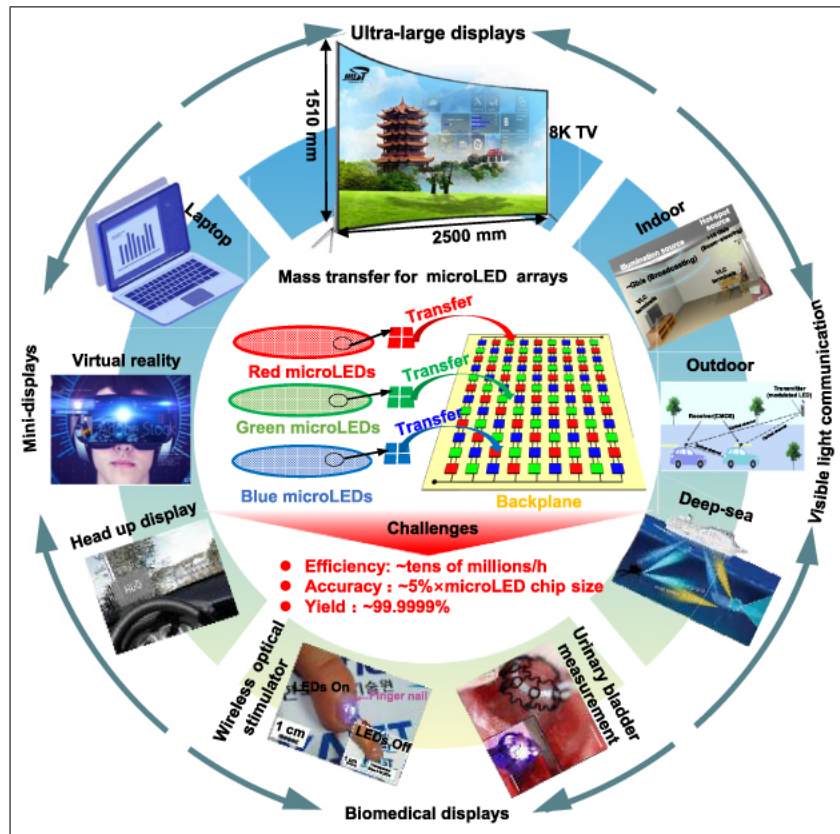


Figure 1.6: Manufacturing process of microLED displays and representative examples of the applications microLED displays [50]

MicroLED technology is considered a promising next-generation display technology due to its numerous advantages over traditional display technologies such as LCD and OLED [51], [40]. They have the potential to significantly enhance the dynamic range of LCDs and provide sunlight-readable emissive displays [52].

Compared to OLED or LCD displays, MicroLED flat panel displays offer unmatched performance advantages, leading to a growing industry consensus that MicroLED will become a significant flat panel display category [53]. Inorganic-based MicroLEDs have demonstrated significant improvements in display and biomedical applications, potentially revolutionizing future optoelectronic systems [54]. MicroLED technology is garnering strong interest as a means to achieve superior displays supported by bright, long-lasting, and efficient emitters across various applications [55].

While challenges exist in commercializing MicroLED displays, leveraging existing expertise and equipment from related industries can expedite the industrialization of MicroLED technology [56]. MicroLED arrays, with pixel sizes smaller than 10 microns, are envisioned for wearable display applications, offering high dynamic range and power efficiency [43]. The potential for MicroLED displays to integrate more complex sensors due to their smaller emitter size relative to the display's pixel area opens up possibilities for advanced functionalities [57].

Beyond entertainment and consumer electronics, microLED technology finds applications in medical sensors for monitoring physical and psychological conditions and treating diseases. Additionally, microLED-based visible light communication (VLC) systems facilitate high-speed data transmission ($\geq 10\text{ Gbps}$) and modulation bandwidths ($\geq 100\text{ MHz}$) [58], enabling deep-sea communication. Figure 1.6 illustrates the manufacturing challenges of microLED displays and some representative examples of their applications.

1.3 Micro-LED displays on the market

Since the advent of microLED, there has been a surge in interest and investment from both investors and companies seeking to develop micro LED display technology. Figure 1.7 shows two representative examples of the first demonstrated microLED TVs by

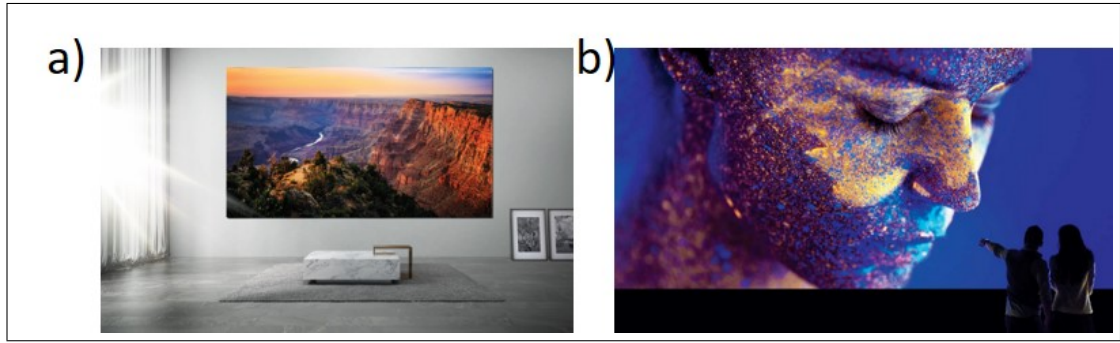


Figure 1.7: Two representative examples of the first demonstrated microLED TVs. a) Samsung "The Wall" (Credit: Samsung) and b) "Sony microLED Cleidis" (Credit: Sony)

Samsung and Sony and Figure 1.8 presents a chronological diagram of all the demonstrated microLED products and their corresponding mass transfer process up to 2020. Some highlights of the microLED prototypes are briefly mentioned in this paragraph. In 2012, Sony launched its first 55-inch full HD Micro LED TV with over 6 million Micro LED chips. Compared to Sony LCD and plasma TVs of the same era, this TV has a contrast ratio of $3.5\times$ higher, color reproduction rate of $1.4\times$ higher, and response speed of $10\times$ higher. In 2014, Apple Inc. acquired LuxVue, demonstrating its commitment to developing micro LED displays for future products such as the iWatch, iPhone, and iMac and significantly increasing the popularity of micro LED display technology. In 2017, the French laboratory CEA-LETI presented a prototype of a wide $10\ \mu\text{m}$ pixel pitch video graphics microdisplay based on a patterned array of monochromatic gallium nitride microLEDs integrated with CMOS circuitry. In 2018, Sony unveiled its impressive 16K resolution Micro-LED display "CLEDIS", and Taiwan-based PlayNitride showed off two prototypes of its full-color Micro-LED display panels. AUO Corporation, also from Taiwan, has launched a 12.1-inch full-color Micro LED display with amazing performance. US-based X-Celeprint demonstrated the versatility of its technology in 2018 by launching a 5.1-inch full-color Micro LED display comprised of red, green, and blue LEDs. In the same year, Samsung launched The Wall, a 146-inch micro LED display. In 2019, Chinese companies Ledman, Konka, Leyard, and others launched impressive 8K Micro-LED screens ranging from 135 to 324 inches.

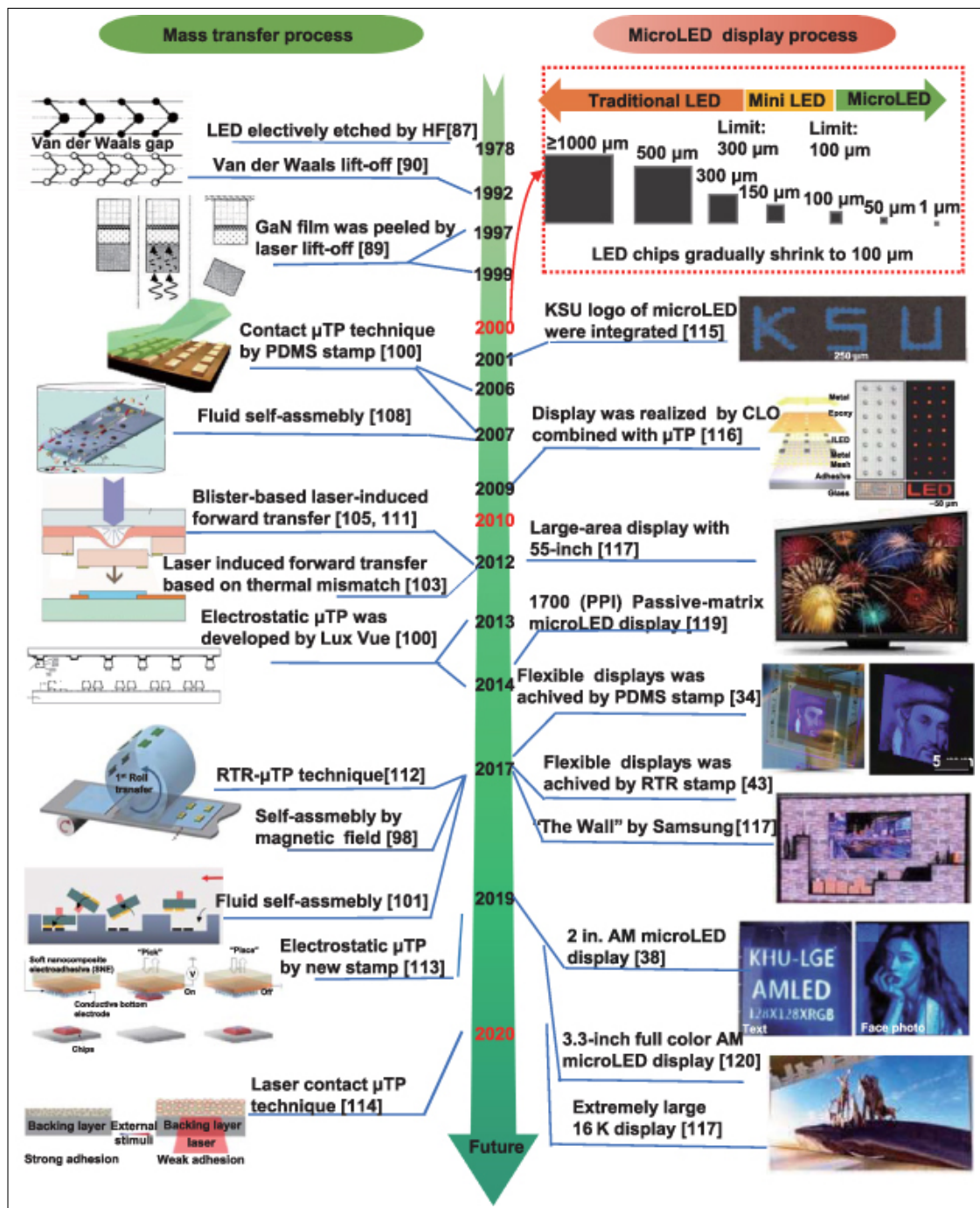


Figure 1.8: Schematic diagram of a brief chronology of the development of microLED displays and mass transfer techniques. [50]

In 2022, Seoul Viosys demonstrated additional potential for large-scale applications by introducing 54-inch and 81.5-inch micro LED displays with pixel spacing suitable for

producing 4K display screens ranging in size from 100 inches to 200 inches. Several companies, including Lumiode, Jade Bird Display, and Plessey, have announced upcoming new product launches in 2025, highlighting widespread expectations for micro LED technology. These achievements highlight the promising trajectory of microLED as a next-generation display technology. Its applications are expected to expand beyond flat panel displays to include spatial displays, wearable/implantable optoelectronic devices, visible/deep-ultraviolet sunblind communications, biomedical sensing, and many other fields. The proliferation of new micro LED displays in recent years is closely related to the development of mass transfer technology. However, high production costs continue to hinder the widespread adoption of microLED displays [59].

1.4 Mass transfer challenges

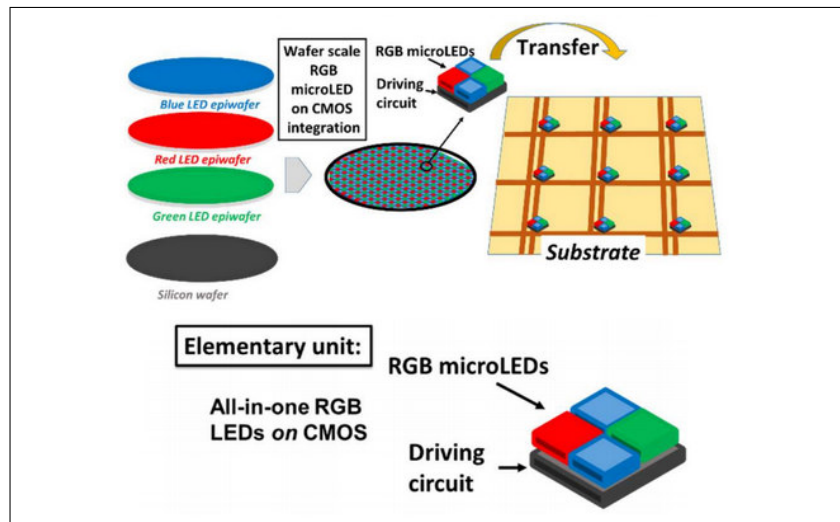


Figure 1.9: Schematic of the fabrication of a full colour microLED display [60]

The development of microLED displays is based on millions of multi-colored self-luminous elements consisting of red, green, and blue (RGB) micro LEDs. However, growing RGB microLEDs simultaneously on a single epitaxial wafer is difficult because wafer size is limited to approximately 8 inches. Therefore, it is necessary to deterministically assemble microLED chips from various growth/donor substrates. This can be illustrated in Figure 1.9. Moreover, Gallium Nitride (GaN) is commonly grown on

sapphire substrates due to lattice matching and its optical transparency, which is beneficial for optoelectronic applications [61]. Sapphire wafers are typically restricted to a maximum size of 6 inches [62]. In contrast, low-cost silicon (Si) substrates are available in sizes up to 12 inches in diameter, which is important for real scaling of microLEDs production [63]. Moreover, GaN on Si technology offers the advantages of being compatible with standard silicon processing technologies and equipment [64]. However, Si is an indirect bandgap material and absorbs a significant portion of visible light. When micro-LEDs are fabricated on a silicon wafer, the emitted light can be absorbed by the silicon, which dramatically reduces its efficiency [65]. To achieve high efficiency and brightness, micro-LEDs need to be transferred to a substrate that either reflects light or is transparent to the emitted wavelengths. Thus, micron scale device transfer at 12 inches scale is needed [66]. The challenges associated with mass transfer of microLED displays are multifaceted and include the need for high-throughput processes, cost-effective methods, and precise assembly of display substrate for final applications, e.g flat panel display. One of the key challenges is to achieve high-throughput mass transfer processes that can rapidly assemble millions of micron-sized devices onto non-native display substrates. [12]. This challenge is further compounded by the need for full-color operation, reduced external quantum efficiency (EQE), and low mass transfer efficiency and yield. Moving microLEDs to large-area TFT backplanes represents a major challenge as it is a significant technology step missing in current display technologies. [13] Additionally, the high production costs associated with mass transfer make microLEDs an excellent candidate for future display technologies [67]. Achieving micro LED display performance and cost goals requires uniform, low-defect epitaxial stacks and high-performance, low-cost wafer-to-backplane mass transfer. [68]. Efforts to develop microLED technology for displays have increased attention to the importance of mass transfer micro-assemblies. [55]. Research is ongoing into more cost-effective mass transfer methods, which will be a key factor in the popularity of microLED displays. Addressing these issues is critical to the successful commercialization and widespread adoption of microLED display technology

Despite their diminutive size ($<100\text{ }\mu\text{m}$), microLED chips pose significant fabrica-

tion challenges. Three primary hurdles must be overcome [69]:

1. Achieving extreme transfer efficiency (tens of millions per hour (h^{-1}) is crucial due to the immense number of chips required for high-resolution displays. Traditional pick-and-place techniques are inadequate for transferring over 100 million pixels onto the receiver substrate, essential for an 8K display.
2. Ensuring extreme placement accuracy (approximately 5% of the microLED chip size) is critical. The transfer error of a $10\ \mu m$ -sized microLED chip should be smaller than $0.5\ \mu m$, far beyond the accuracy of traditional transfer techniques.
3. Ensuring extreme reliability (around 99.9999%) is essential to prevent thousands of dead pixels resulting from even a 0.01% failure rate.

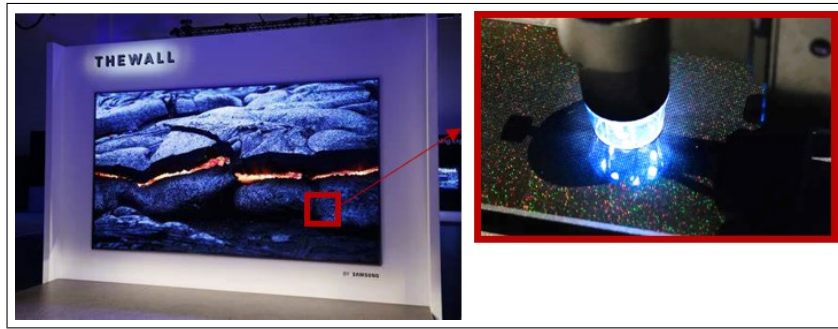


Figure 1.10: Example of Samsung ‘The Wall’ 960×540 microLEDs with a close up of the individual pixels across a small area. Source: Samsung, CES Global Stage of Innovation 2018

These requirements are related to the pixel density and resolution, color and brightness uniformity, electrical connectivity, scalability and consistency. Traditional assembly methods prove impractical for microLEDs, necessitating innovative approaches to address these challenges. The development of efficient and cost-effective assembly concepts and processes for large-scale and high-density microLED arrays is paramount to unlocking the full potential of microLED technology across various applications.

Conventional mechanical transfer equipment falls short in meeting the demands for transferring Micro-LED chips in the millions required for mass production. One of the

primary issues is the need for high-yield mass transfer processes that can rapidly assemble millions of micron-scale devices onto non-native display substrates [12]. This process necessitates an exceptionally high transfer rate, alignment accuracy, bonding strength, and reliability. For instance, to manufacture a 4K ultra-high-definition (UHD) color TV, approximately 25 million Micro-LED chips need to be transferred. In order to understand this example better, Figure 1.10 presents an example of the first demonstrated micro-printed LED TV presented by Samsung in 2018, including an inset of individual pixels across a small area. According to traditional transfer equipment and technology, this process would take more than two months, clearly falling short of mass production requirements [5]. The transfer of microLEDs onto the large area TFT backplane, which is a critical technical step, does not exist in present display technologies, posing a significant challenge for conventional transfer methods [70]. The challenges associated with mass transfer in manufacturing and the efficient fabrication of low-current, micron-scale optoelectronic devices have historically impeded the commercialization of microLED displays, making conventional methods inadequate for addressing these challenges [53]. Consequently, there is a critical need for mass transfer technology to meet these production demands. Conventional methods, such as wafer dicing and pick-and-place techniques, are not suitable for devices with the thicknesses and dimensions in the range of microLEDs due to challenges associated with wafer utilization, device fragility, and size [71]. Additionally, the conventional method of fabricating microLED displays from red, green, and blue (R/G/B) LED wafers involves multiple steps with multiple interposers, making the process complex and less suitable for high-throughput mass transfer [72].

Moreover, the success of microLED display insertion hinges on its cost competitiveness against conventional LCD/OLED displays. However, at the time of writing, cost competitiveness is not yet realistic, indicating that conventional transfer methods may not be suitable for achieving the cost targets required for mass production of microLED displays [73].

1.5 Mass transfer printing methods

Pick-and-place techniques in mass transfer can be categorized into four main types based on the relative position of the transfer medium and receiving substrate and the technical means that they use.

1.5.1 Self-assembly mass transfer

Self-assembly of Micro LEDs is a technology that allows cost-effective and rapid integration of large numbers of functional components onto non-traditional substrates. [74] This method is used for MicroLED display assembly, combining LED wafers and provides a practical micro-assembly technology that acts as a bridge between display panels [75]. Companies such as Sharp and Foxconn have used transfer self-assembly technology to assemble MicroLED displays, demonstrating practical application in industry [76]. Self-assembly methods demonstrate their versatility by providing a way to integrate optoelectronics into objects that are incompatible with traditional semiconductor manufacturing processes.

Using a self-assembly method represents a more efficient approach to the complex task of deploying microLEDs compared to traditional bulk assembly methods. Unlike multi-step processes, self-assembly simplifies the procedure by requiring only one step: placing the microLED chip in a special liquid environment. This environment recognizes the shape of the chips and manipulates physical forces to help align and position them. By leveraging these features, self-assembly technology can greatly improve the transmission efficiency of [77].

One type of self-assembly method is fluid-based, which uses the properties of a liquid medium to guide the microLED chip to the desired location. In this process, a specially designed substrate is dipped into a self-assembly solution at a specific angle (typically around 30°) to allow the chip to move smoothly under gravity. Because the micro LED chips float in a liquid environment, they are free to move until they come into contact with the molten alloy at a predetermined location, forming a stable bond. A schematic, representing the self assembly fluid transfer, can be seen in Figure

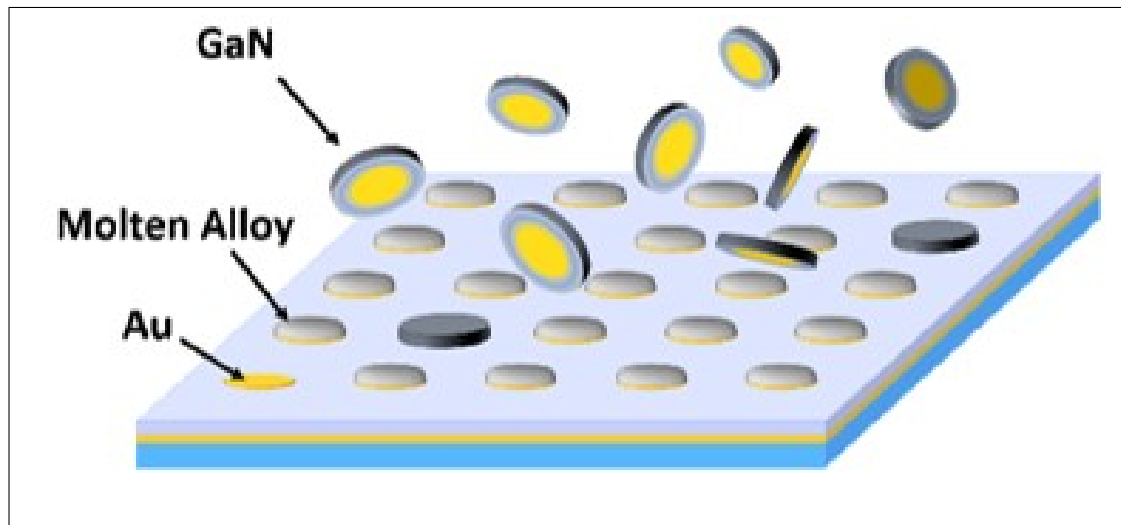


Figure 1.11: a) Schematic representation of self assembly fluid transfer [78]

1.11. Positioning and alignment of microLEDs during liquid-based self-assembly relies on two main mechanisms: shape sensing and surface tension-based alignment. Shape recognition involves matching complementary shapes (indentations) on the substrate, ensuring that only microLEDs of a specific shape, such as a $100\ \mu\text{m}$ square shape, are suitable for recognition. In contrast, alignment by surface tension utilizes the capillary forces of the molten alloy on the substrate. Initially, confined liquid droplets (molten alloy) are placed in a given pattern, forming a meniscus shape due to capillary forces, which helps align the chip to the desired position [79], [80]. Liquid-based self-assembly has shown remarkable performance in microLED alignment, achieving transfer efficiencies of up to 97% with self-assembly rates of 40,000 units per hour for $100\ \mu\text{m}$ parts, with an emphasis on mechanical positioning without electrical connections. However, obstacles remain, including limitations related to chip materials and shapes, as well as the risk of damage due to elevated interface temperatures. Fluid-based self-assembly can also use magnetic [81] or electric forces [82], [83] to facilitate movement and positioning of the chip at designated receptor sites. Numerous technical obstacles must be overcome to minimize the occurrence of missing chips. Therefore, a thorough study of the impact of process parameters on alignment accuracy, covering factors such as magnetic/electrostatic field strength, chip-to-pad distance and orientation, chip size

and configuration, and magnetization/static level, is important. Additional research is needed to address these issues and improve processes to improve efficiency and reliability.

1.5.2 Elastomeric and roll-transfer printing

Elastomer stamp transfer is a promising mass transfer method for microLEDs with unique properties suitable for high-throughput manufacturing processes. X-celprint uses this process which involves capturing microLEDs from a source substrate and transferring them to a receiver substrate using an elastomeric stamp, typically made of a material such as polydimethylsiloxane (PDMS) [84]. Elastomer stamps can be easily adhere to microLEDs due to their unique properties, such as adhesiveness and ductility, and then transferred to receiving substrates using high transfer coefficients. This feature is particularly useful for achieving high transmission rates and maintaining the integrity of transmitted micro LEDs. [67]. The elastomer die transfer process involves several key steps. Figure 1.12 a) shows a diagram of the four steps involved in the process. First, the elastomer stamp is brought into contact with the mother substrate containing the micro LED. The stamp attaches to the microLED via van der Waals interactions, allowing efficient and accurate device selection. The stamp is then brought into contact with a receiving substrate and the micro LEDs are transferred to the new substrate, forming the desired pattern or array. Thanks to the convenient stamp shape, the micro LEDs are positioned precisely on the receiver board, contributing to high transmission efficiency and process accuracy [53].

One limitation of the elastomer stamp transfer method is that the range of adhesion control can be limited, making it difficult to achieve high transfer rates on certain substrates without adhesion promoting layers. Additionally, the scalability and productivity of the elastomer die transfer process are important factors for commercialization, which affect the efficiency and cost-effectiveness of mass production [85].

Roll-to-roll transfer is an innovative approach developed for high-volume transfer of microLEDs, offering unique advantages for high-throughput and high-throughput manufacturing processes. This method was developed by the Korea Institute of Machinery

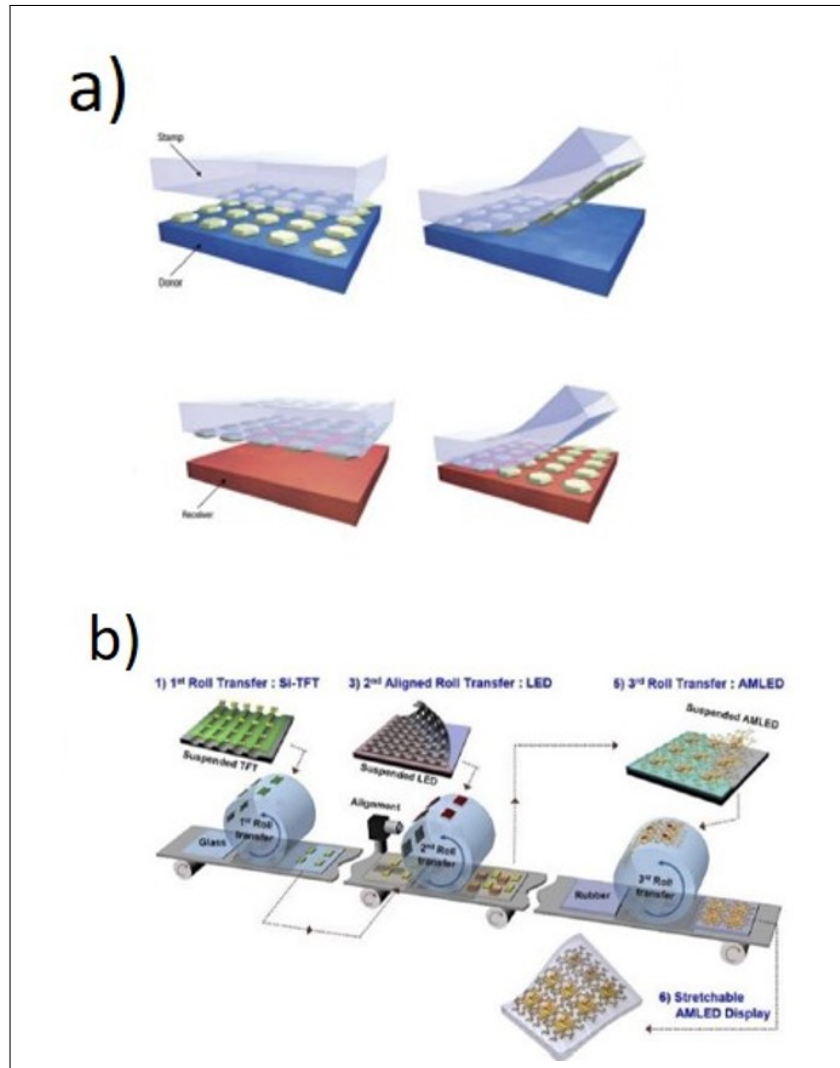


Figure 1.12: a) Schematic representation of elastomeric transfer and b) roll transfer printing [86]

and Materials (KIMM) and has shown promise in solving problems associated with bulk transfer of micro LEDs [87], [88]. The roll-to-roll transfer process involves using continuous rolls of flexible substrate material from which the microLEDs are transferred from the original substrate, as it can be seen in Figure 1.12 b). The continuous nature of the roll-to-roll printing process enables high-speed continuous transfer of microLEDs, enabling efficient mass production. This method is particularly advantageous for achieving high transmission rates and maintaining the integrity of transmitted microLEDs. In the roll-to-roll transfer process, a flexible substrate is fed through a series

of rollers to transfer the microLEDs to the substrate at high throughput. This continuous, automated process ensures fast and accurate transmission of microLEDs, providing high transmission throughput and process efficiency.

One of the main advantages of roll-to-roll transfer is that it allows for scalability and mass production. The rolling nature of the process allows large-scale production of microLED displays, making them suitable for commercial applications. However, this technique is still not in scale and it faces some challenges, especially regarding the chip size, alignment and devices damage.

1.5.3 Electrostatic/Electromagnetic Contact μ TP technique

Another approach to contact μ TP involves electrostatic or electromagnetic forces. In this technique, special stamps capable of generating switchable electric or magnetic forces are utilized. Figure 1.13 presents a schematic of the two processes. Apple's company, LuxVue, uses electrostatic transfer technology to replace the head with an electrode layer and the dielectric layer with a substrate. The size of the electrostatic switching head array is very close to the range of the device. The gap must be the same size as the Micro-LED chip gap to ensure correct switching. This transfer method uses electrostatic attraction and repulsion to select and place and can transfer multiple Micro-LED sheets simultaneously. [89].

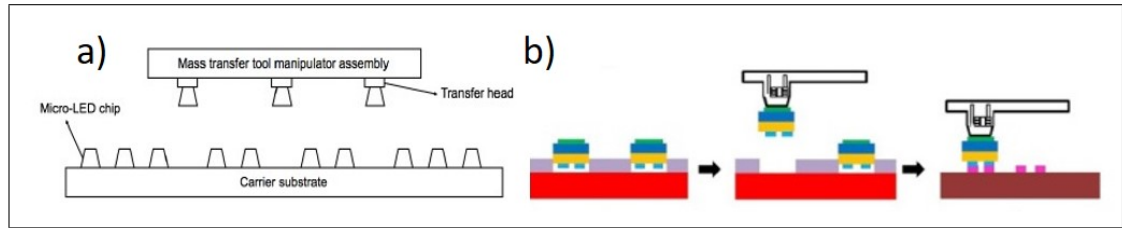


Figure 1.13: a) Schematic representation of electrostatic transfer and b) electromagnetic transfer printing [86]

In contrast to the electrostatic contact μ TP technique, the electromagnetic contact μ TP technique requires microLED chips with an additional magnetically sensitive layer to generate magnetic force. Industrial Technology Research Institute (ITRI) and other integrated units combine iron, cobalt, nickel and other magnetic materials into Micro-

LED chips, making them magnetic and then harnessing the energized energy coils as head for transmission. Electromagnetic forces can be controlled using programmable electromagnetic modules [90]. The complexity of this technology lies in the consistency of the magnetic dopant material and the complexity of the electromagnetic module design. Both electrostatic and electromagnetic contact μ TP techniques offer a promising approach for integrating extremely small objects. However, mass transferring tiny chips with predefined patterns remains a significant challenge, primarily due to the preparation and patterning of the stamp. Moreover, applying voltage to the head during electrostatic induction can lead to a charging effect that may harm the micro devices.

1.5.4 Laser assisted Transfer Printing

Laser-assisted transfer techniques, used by US QMAT, Uniquarta and Sony companies, have emerged as a critical enabler for the mass production and commercialization of MicroLED displays. The precision, scalability, and versatility of laser-assisted transfer methods offer promising solutions for addressing the challenges of large-scale manufacturing and integration of MicroLED technology into diverse applications. As research and technological advancements continue, laser-assisted transfer of MicroLEDs is poised to play a pivotal role in shaping the future of display technology, offering high-performance, energy-efficient, and visually immersive display solutions. Laser lift-off (LLO) and Laser-Induced Forward Transfer (LIFT) are two prominent processes used for the mass transfer of microLEDs, each with its unique characteristics and applications. These techniques have demonstrated high precision and large-scale mass transfer processes, enabling the transfer of microLEDs with high throughput and yield [91], [92]. A schematic representation of both laser assisted transfer techniques can be seen in Figure 1.14.

Laser lift-off (LLO) is a technique that has been demonstrated to successfully separate GaN thin films from sapphire substrates using a laser. The process involves the use of a high-powered laser beam to vaporize the interface between GaN and sapphire, allowing for the detachment of the thin film. LLO has been widely used to separate LED devices from sapphire substrates, and it has shown promise in achieving high

precision and large-scale mass transfer processes. The third harmonic of a Q-switched Nd:yttrium-aluminum-garnet (YAG) laser has been utilized for successful LLO, and deep-UV LLO has been identified as the only proven way of separating GaN from sapphire substrates that are deep-UV transparent [93], [94], [95].

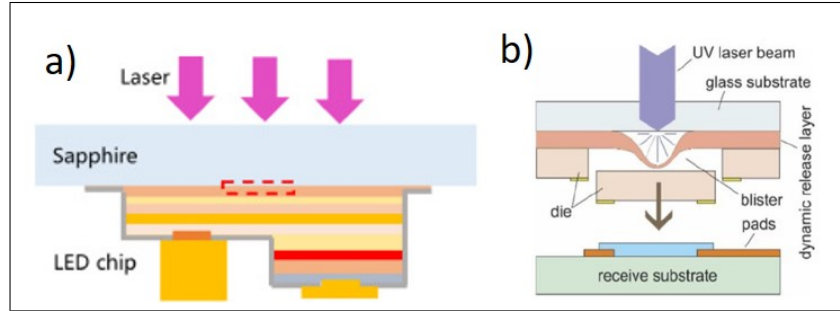


Figure 1.14: Schematic representation of laser-assisted transfer. a)LLO [96]and b)LIFT [86]

On the other hand, Laser-Induced Forward Transfer (LIFT) is a technique that involves the use of a laser to transfer a thin film of material from a donor substrate to a receiver substrate. This process enables the precise transfer of microscale light-emitting diodes (LEDs) to unusual substrates by spontaneously formed vertical tethers during chemical lift-off. LIFT has been applied to the mass transfer of microscale LEDs and has shown potential for achieving high-density microLED arrays. Additionally, LIFT has been used for the detachment of thin InGaN/GaN LEDs from their original sapphire substrates by applying an ultrafast laser [97], [98], [99].

Both LLO and LIFT processes have been instrumental in addressing the challenges associated with mass transferring microLEDs. LLO has been particularly effective in separating LED devices from sapphire substrates, while LIFT has shown promise in achieving high-density microLED arrays and the detachment of thin LED films from their original substrates. Although these methods satisfy the yield and accuracy requirements, the cost and complexity of the laser system, as well as the risk of damage of the devices from the laser source, still need to be addressed.

1.6 Mass commercialization of microLED products

To encourage widespread adoption of microLED displays, efforts are underway to find cost-effective mass transfer methods based on highest efficiency, productivity, and precision. These efforts highlight the importance of developing transfer methods that can efficiently process millions of microLED pixels with minimal material loss and high success rates. Achieving this efficiency and precision in high-volume transfer processes is critical to reducing manufacturing costs and increasing the commercial viability of microLED displays. As advances in this direction continue, the implementation of more cost-effective material delivery methods is becoming a critical factor in popularizing microLED displays across a variety of applications and industries. There have been significant changes in the commercial landscape for microLED products in recent years. Several companies specializing in GaN-on-Si LED devices have already begun selling their technology and products, including Lattice Power, Osram, BridgeLux, and Plessey [100]. These companies have proven the advancement and commercialization of microLED technology by taking the lead in bringing microLED products to the market. Additionally, the quality and variety of microLED display prototypes is growing rapidly as the first commercial products hit the market. This represents a significant change in the availability of microLED products and marks a turning point in the commercialization of this technology. MicroLED display products have not been commercially available in the past due to serious technical issues, but recent developments have led to the launch of commercial products. [101].

Current limitations of microLED mass transfer methods, such as laser transfer methods, elastic die transfer techniques, and roll-to-roll transfer methods, pose serious challenges to commercialization. These limitations are preventing widespread adoption of microLED displays in mainstream consumer applications. One of the main limitations is the high cost associated with these advanced bulk transfer methods. The labor intensity and high cost of these methods make them insufficient for commercial purposes, making them difficult to scale up for mass production of micro LED displays. Additionally, complexity and technical challenges have historically hindered the com-

mercialization of microLED displays, particularly those associated with the production of low-current, micron-scale optoelectronic devices and mass mobilization in efficient production. Moreover, the critical technological step of moving micro LEDs to large-area TFT backplanes does not exist in current display technologies, presenting great challenges to commercialization. Mass production of low-cost consumer TVs is also limited by the need to process millions of individual chips, highlighting a significant limitation in the mass production of microLED displays. Figure 1.15 presents a table that summarizes all the mass transfer techniques presented in this section.

Transfer method companies	Performance	Advantages	Disadvantages	Special requirement	Chip size	Used by
Laser-based	Transfer yield 99.99% Transfer rate 100millions/hour	No impurities transfer on substrate surface	Laser source can damage their transfer stability	Need to be placed in a transparent substrate to laser source	>1 μm	Optovate/Uniqarta
Electrostatic transfer	1 million/hour	Flexible and perfect repeatability	Charges are induced which can degrade device performance	Suspension	1-100 μm	Apple/LuxVue
Fluidic based transfer	Transfer yield 65% Transfer rate 50millions/hour	Economical, easy to operate	Inefficient, high probability of pixel damage	Liquid suspension	>20 μm	Foxconn/eLux
Elastomeric transfer	Transfer yield 99.99% Transfer rate 1 million/hour	Efficient and economical transfer	Poor repeatability	Suspension	>10 μm	X-Celeprint
Roll to roll transfer	Transfer yield 99.99% Transfer rate 10.000 /second	High efficiency, economical and high throughput	High probability of device damages	Suspension	100 μm	KIMM

Figure 1.15: Table of comparison between mass transfer techniques for micro-LEDs [77]

Despite the advantages in the field of transfer printing, several challenges remain for mass transfer, particularly concerning cost, yield, and chip size. These issues need to be addressed to achieve a dominant market position. Depending on the application and the number of devices, different techniques may be preferred. Among the existing methods, roll-to-roll printing is the most attractive due to its high transfer rate, lack of

Chapter 1. Introduction

reliance on external forces, and its roller-based system, which is common in high-volume manufacturing industries. However, this technique still faces issues with placement accuracy and chip size.

This thesis introduces a transfer printing method based on the roll-to-roll technique, aiming to achieve a similar transfer yield (99.9%) for tens of chips, with a placement accuracy of $1\ \mu\text{m}$ and a pixel size as small as $30\ \mu\text{m}^2$.

1.7 Thesis outline

Chapter 1 has given an overall introduction of current technology and challenges and how heterogeneous integration technology helps with these challenges. The evolution of display technology was presented briefly, ending up to the next generation display technology, the microLED displays. The challenges for the commercialization of these displays were presented, focusing on the mass transfer. The mass transfer techniques that are currently under development were discussed and the limitations of these. In Chapter 2, the fabrication for high yield large scale devices will be presented. The new development of a method based on continuous roll-transfer printing will be introduced, highlighting its potential for large scale transfer devices. Chapter 3 introduces a new custom made automated image based inspection method for large array transfer devices with less than $1\ \mu\text{m}$ accuracy. The results of a roll-transfer printed miniLEDs and microLEDs will be presented and analyzed by using this method. Chapter 4 describes the ability of inducing strain in thin film silicon membranes by physically bending them. The results combine theoretical analysis, simulation and experimental results. Finally, Chapter 5 concludes the presented thesis and achievements and discusses the future work.

Chapter 2

Fabrication of large membrane device arrays and roll-transfer printing

2.1 Micro-fabrication processes

In this section, a brief description of the methods and processes used during the fabrication of membrane device arrays and characterization will be presented. All the equipment used for this work is located in the Strathclyde cleanroom laboratory. A cleanroom laboratory is a controlled environment designed to minimize and control temperature, humidity, airborne particles, pollutants, and other contaminants that could adversely impact sensitive processes, such as semiconductor manufacturing or biotechnology research [102]. These specialized facilities adhere to stringent cleanliness standards, typically specified by the ISO class system, with lower class numbers indicating cleaner environments. Cleanrooms are characterized by high-efficiency particulate air (HEPA) or ultra-low penetration air (ULPA) filtration systems that continuously filter and circulate air to maintain low particle counts [103]. Personnel in cleanrooms often wear specialized garments such as cleanroom suits, gloves, and masks to prevent the introduction of contaminants. Access to cleanrooms is usually restricted, and protocols for entering and exiting are strictly enforced to ensure the maintenance of



Figure 2.1: Part of the dry process room in the cleanroom located in TIC.

cleanliness. Cleanroom laboratories are vital for industries where even minute particles can impact product quality or the outcome of delicate scientific experiments. Due to the small size of the chip and the step by step processes that involve deposition or removal of layers of materials, airborne dust particles can severely affect the process yield. The clean room located in the Technology and Innovation building, where all the experiments were conducted, is commissioned with class 10,000 (ISO 7) meaning 10,000 particles/cubic foot of size $>0.5 \mu m$ are permitted after ISO norm [104]. A part of the cleanroom can be seen in Figure 2.1 The section describes the standard procedure of micro-fabrication processes, starting with the necessary preparation and cleaning of the sample. Each machine and recipe used in this thesis is introduced. To ensure the success of each process, a range of characterization techniques have been used and are briefly described. Finally, the process of fabricating suspended mini/micro LEDs is presented. A flow chart of the whole fabrication process is presented in Figure 2.2, however, the full details of each process are described in the following subsections.

2.1.1 Preparation of the sample.

The 6-inch (15.24 *cm*) GaN-on-Si wafers, measuring 1 *mm* in thickness, were received in quarters, with the Si [110] crystal direction indicated by a notch. This notch serves as a guide for a potassium hydroxide wet etch, which laterally removes Si at a rate of approximately 1 $\mu m/min$. The wafers were initially cut into regular 15x19 mm^2 dies, with the longer direction to be the one perpendicular to the notch, by using the 'DAD3220 Disco Automatic Wafer Saw' dicer. Figure 2.3 represents the size of the wafer and the corresponding dicing size. In the next section, the importance of cutting



Figure 2.2: Flow chart of the fabrication of suspended membrane arrays

the chips in larger pieces will be presented, as well as its contribution to the roll-printing process and the uniformity of the printing devices. Prior to any fabrication process, a standard cleaning preparation for all the wafers used is essential. The standard cleaning preparation for a wafer before any fabrication involves a series of meticulously controlled steps to ensure a pristine substrate surface [105].

Typically, the process begins with a solvent clean, where the wafer is immersed in organic solvents like acetone or isopropanol to remove any organic surface contaminants. These contaminants may include residues from handling, oils, or other organic substances that could interfere with subsequent fabrication processes. The solvent clean is typically performed in a controlled environment to minimize the risk of recontamination. After the wafer is immersed in the solvent, it is often subjected to ultrasonic agitation to enhance the removal of particulate matter. Following the solvent exposure, a thorough rinse with deionized water is usually performed to ensure the complete removal of the solvents, particles, organic residues and any remaining contaminants. This initial cleaning step is essential for achieving a pristine substrate surface and is typi-

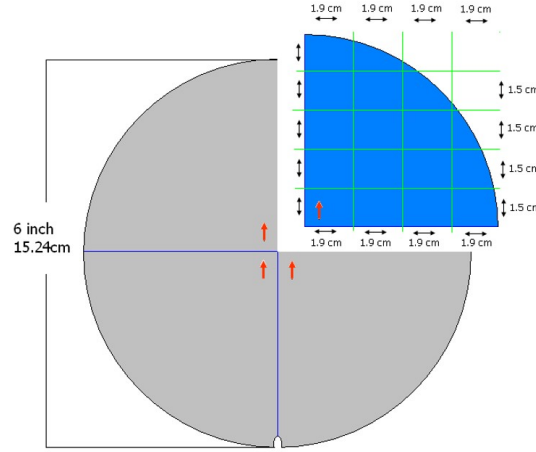


Figure 2.3: Representation of the regular dicing size

cally followed by additional cleaning processes, such as the oxygen plasma treatment, to further prepare the wafer for semiconductor manufacturing. This is followed by a rinse with deionized water. Thorough cleaning process is essential for creating a clean and uniform starting surface for subsequent fabrication steps, ensuring the success and reliability of semiconductor manufacturing processes on the wafer. The sample is then dried under pressurised N_2 flow. For samples intended for spin coating, a subsequent step involves placing the sample on a hotplate at a temperature exceeding 100°C for 10 minutes. This aids in evaporating water residues to enhance resist adhesion to the surface. The same standard solvent clean can be employed for removing photoresist after dry etching. The 'Matrix 105 Plasma Asher Descum' is a useful tool for enhancing cleaning [106]. It operates by creating an oxygen plasma discharge, with reactive radical species diffusing to the target wafer or die, removing organic resists at rates of around $1\ \mu\text{m}/\text{min}$. The process conditions include a pressure of $3.75\ \text{Torr}$, Mass Flow Controller (MFC) at 35%, 500 W RF power, and a substrate temperature of 200°C . This process is applicable for both photoresist removal and general cleaning purposes.

2.1.2 Photolithography patterning and development

Photolithography is a fundamental process in semiconductor manufacturing, essential for creating intricate patterns and features on substrate wafers [107]. The process be-

gins with a clean wafer being coated with a photosensitive material called photoresist. This photoresist is applied as a thin film and is sensitive to ultraviolet (UV) light. The wafer is then pre-baked to evaporate any solvent in the photoresist, ensuring a uniform coating. Next, a photomask, containing the desired pattern, is placed in proximity to the wafer. The photomask is typically made of glass and has a patterned metal film that allows or blocks the passage of UV light. The entire system is then exposed to UV light, and the photoresist undergoes a chemical change, becoming either more soluble (positive photoresist) or less soluble (negative photoresist) in a developer solution. After exposure, the wafer undergoes a post-exposure bake to further stabilize the pattern. In the development step, the exposed photoresist is selectively removed, revealing the underlying wafer surface. The exposed or unexposed areas now serve as a mask for subsequent processing steps. For positive photoresists, the areas exposed to UV light are removed during development, leaving the unexposed regions on the wafer. Conversely, in the negative photoresist, the exposed areas remain after development [108]. The wafer is then subjected to various processing steps such as etching or deposition, where the exposed or unexposed regions dictate the pattern transfer onto the silicon. This photolithography process is repeated for each layer of the semiconductor device, enabling the creation of complex and layered structures necessary for the functionality of integrated circuits and other microelectronic devices. The precision and repeatability of photolithography are critical for achieving the nanoscale features required in modern semiconductor fabrication [109].

Laser lithography is a high-precision technique used in the fabrication of semiconductor devices and microelectronics [110]. The process begins with a substrate coated with a light-sensitive material. Unlike traditional photolithography which uses a broad spectrum of light, laser lithography employs a focused laser beam to directly write the desired pattern onto the photoresist. The laser beam is directed by a system of mirrors and lenses, allowing for precise control over the exposure and spot size. Another important feature of laser lithography is its maskless operation, compared to traditional lithography where a physical mask is needed. The photoresist undergoes a chemical change upon exposure to the laser, becoming either more or less soluble depending

on the specific type of photoresist used. After exposure, the substrate undergoes a development process to selectively remove the exposed or unexposed areas of the photoresist. Laser lithography offers advantages such as higher resolution and the ability to create intricate patterns on a smaller scale down to 300 nm , compared to conventional photolithography. This method is particularly valuable in the production of advanced semiconductor devices with nanoscale features.

UV Mask lithography

The primary lithography employed in this study utilizes a Karl Suss MA6 mask aligner, which can be seen in Figure 2.4a). In this type of mask aligner, a 4-inch squared glass substrate is patterned with a thin-film chromium mask and brought into close proximity to the sample surface within micrometer range. The chromium layer shields portions of the resist, while the corresponding areas are illuminated by a high-pressure short-arc mercury lamp, emitting ultraviolet light in the wavelength range of 365 nm to 436 nm (Hg UV400-type). This system allows for a minimum feature size as low as $1\text{ }\mu\text{m}$, depending on resist thickness and substrate flatness. To ensure an even optical power density distribution in the exposed area of the mask, optical elements collimate the UV beam. Translation stages are employed for precise adjustment of x, y, z positioning, and rotation. The accurate alignment of sequential exposures is crucial for optimal development. A gap of more than $15\text{ }\mu\text{m}$ between the mask and the samples is necessary to enable free movement beneath the exposing pattern, a configuration known as proximity lithography. The initiation of pattern exposure involves determining parameters such as dosage, time, and exposure gap, based on the photosensitive material properties and thickness. The parameters used in this thesis are stated in Table 2.1. Similarly, the development of the photoresist pattern employs a PR-specific developer, with adjustments in developer dilution and exposure time based on material characteristics, allowing for specific thicknesses or sidewall shaping. While photolithography is a valuable tool for defining patterns on surfaces, it alone cannot make these patterns permanent. To achieve permanence, various etching methods (both wet and dry), as described subsequently, can be utilized to engrave these patterns permanently into the

Process	Parameters
Spin coating	3.8 krpm/60 sec
Soft baking	1min at 115 °C
Exposure settings	contact/2.8 sec
Development time	35 sec

Table 2.1: Process parameters used with Mask aligner



(a) Karl Suss MA6 mask aligner.



(b) DWL66+ laser lithography system

Figure 2.4: Photolithography machines used in this thesis.

processed materials [111].

Maskless laser lithography

The ‘DWL66+’ laser lithography system, manufactured by ‘Heidelberg Instruments, presented in Figure 2.4b) was also used, especially for the study of tethers design for roll transfer printed devices, as it will be presented in the following section. This tool utilizes a 375 nm UV laser, automatically focused into the coated resist thin film with the assistance of a red interferometer laser that does not expose the resist. The write head objective, which focuses on both lasers, is laterally scanned above the surface while continuously maintaining the objective-substrate distance using the interferometer laser. The photomask is digitally defined and applied by modulating the laser intensity with an acousto-optic modulator (AOM), synchronized with the beam position. This feature facilitates rapid prototyping through design alterations from run to run, allowing the fabrication of large arrays of devices with controllable shape and dimensions. In this process, the exposure parameters include the laser focus, the laser

Process	Parameters
Spin coating	3.8 krpm/60 sec
Soft baking	1min at 115 °C
Exposure settings	Focus -5/Intensity 100%/Power 30mW
Development time	35 sec

Table 2.2: Process parameters used with Laser lithography

intensity and the laser power. After careful optimization, all the parameters used for the laser exposure are mentioned in Table 2.2.

The final step in the photolithography process involves the development of the photoresist. Here, the UV-exposed pattern is transferred into the photoresist film by selectively removing the exposed or unexposed parts of the resist due to light-induced changes in solubility. For a positive photoresist, light exposure locally increases resist solubility, while for a negative resist, the polymer is crosslinked and less soluble in the developer solution. The development recipe used for the following experiments is detailed in Table 2.1 and Table 2.2 for both Mask aligner and Laser lithography patterning, respectively.

2.1.3 Plasma etching and deposition

Plasma-based dry etching and deposition techniques are fundamental processes in semiconductor manufacturing and materials engineering. [112] In plasma-based dry etching, a vacuum chamber is employed to create a low-pressure environment, and reactive gases, often fluorine-based, are introduced. Radiofrequency (RF) power is applied to generate a plasma, which consists of ions, electrons, and radicals. This highly reactive plasma selectively removes material from a substrate by chemical reactions and physical ion etching, allowing for precise and controlled etching of patterns or structures. Conversely, in plasma-based deposition, such as Plasma Enhanced Chemical Vapor Deposition (PECVD), precursor gases are introduced into the chamber and activated by the plasma. The energetic species in the plasma facilitate the chemical reactions necessary for depositing thin films onto a substrate surface. These techniques offer advantages such as high precision, anisotropy, and the ability to operate at lower temperatures

Etching material	Gases	RF Power	Process pressure
Silicon dioxide	5 sccm CHF_3 , 15 sccm Ar	200 W	0.03 Torr
Silicon	10 sccm Ar, 10 sccm O_2 , 60 sccm SF_6	300 W	0.05 Torr

Table 2.3: Process recipes used for etching silicon dioxide and silicon

compared to wet etching or deposition methods. They are crucial in the fabrication of microelectronics, enabling the creation of intricate patterns and functional layers in the production of integrated circuits and other advanced electronic devices [111].

Reactive Ion Etching

Reactive Ion Etching (RIE) is a precision technique employed for selectively etching materials with high anisotropy [113]. When etching silicon dioxide (SiO_2) using RIE, the process involves setting up a vacuum chamber with radiofrequency (RF) power and introducing fluorine-based gases such as SF_6 or CF_4 to enhance reactivity. Prior to the etching, proper masking of undesired areas on the sample is crucial. Once loaded into the chamber, the introduction of reactive gases, application of RF power to create a plasma, and subsequent attack of silicon dioxide by reactive ions occur. The resulting volatile byproducts are pumped away, leaving behind the etched features. Control over gas flow rates and the monitoring of the process, including endpoint detection for achieving the desired etch depth, are essential. Adjusting parameters like temperature can further optimize the process. Following completion, unloading the sample and a post-process cleaning step ensures the removal of any residues. For all the experiments used in this thesis, the following parameters in Table 2.3 for etching silica were used, resulting in an etching rate of 40 nm/min.

To etch silicon using RIE, a vacuum chamber equipped with radiofrequency (RF) power is utilized. Silicon wafers, often coated with a layer of silicon dioxide or a photoresist mask, are loaded into the chamber. Reactive gases, such as SF_6 or Cl_2 , are introduced into the chamber, creating a plasma when subjected to RF power. The reactive ions in the plasma selectively attack the silicon, forming volatile silicon compounds that are pumped away, leaving behind precisely etched features on the silicon surface. Control over gas composition, flow rates, RF power, and other parameters is crucial

Etching material	Gases	RF Power	Process pressure
Gallium Nitride	5 sccm Cl_2 , 10 sccm Ar	200 W	0.02 Torr

Table 2.4: Process recipe used for etching gallium nitride

for achieving desired etch rates and selectivity. Endpoint detection techniques, such as interferometric depth monitoring, help determine when the etching process reaches the desired depth. Post-etch cleaning may be necessary to remove any residues. The specific conditions for silicon etching using RIE depend on the equipment used, the characteristics of the silicon substrate, and the desired outcome, necessitating careful optimization for each application. For all the experiments used in this thesis, the following parameters in Table 2.3 for etching silicon were used, resulting in an etching rate of 580 nm/min for silicon and 125 nm/min for silicon dioxide.

Inductively coupled plasma reactive ion etching

The STPS Multiplex system, an example of an inductively coupled plasma reactive ion etching (ICP-RIE) tool, is designed for precision etching processes, such as those involving Gallium Nitride (GaN) in semiconductor fabrication. [114] In the vacuum chamber of the tool, reactive gases, tailored for GaN etching like Cl_2 , BCl_3 , or SF_6 , are introduced. GaN substrates, often coated with a masking material, are loaded into the chamber. Applying radiofrequency (RF) power to inductive coils generates a high-energy plasma containing reactive ions and radicals. The energetic ions bombard the GaN surface, chemically reacting and forming volatile byproducts that are subsequently evacuated. Temperature control, gas flow regulation, and pressure adjustment are employed to optimize the etching process while monitoring tools aid in endpoint detection, where the slope of the intensity of the wavelength changes indicating the stop of the process at the interface of the different layers. The parameters used in this thesis for etching gallium nitride are presented in Table 2.4. The resulting etched patterns on the GaN surface can be finely controlled, making the STPS Multiplex system a valuable tool for semiconductor manufacturing. All the etching machines that were used in this work as shown in Figure 2.5.

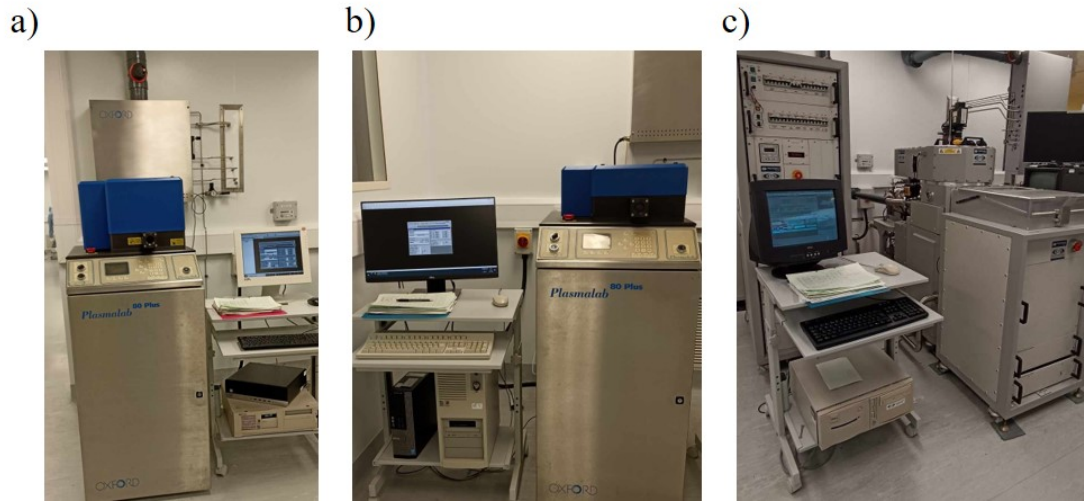


Figure 2.5: Etching machines used in this thesis: a) RIE for silica etching, b) RIE for silicon etching and c) ICP for gallium nitride etching

Plasma Enhanced Chemical Vapor Deposition

Plasma Enhanced Chemical Vapor Deposition (PECVD) is a technique utilized for the deposition of thin films, such as silicon dioxide, onto substrates in a controlled and precise manner [115]. PECVD is widely employed in semiconductor manufacturing and microelectronics for its ability to produce conformal and electrically insulating layers, crucial for the fabrication of integrated circuits and other advanced electronic devices. In the PECVD process for depositing silicon dioxide, a vacuum chamber is employed, and precursor gases, typically silane (SiH_4), nitrous (N_2O) and oxygen (O_2), are introduced into the chamber. Radiofrequency (RF) power is then applied to create a plasma within the gas mixture. The energetic species in the plasma facilitate the dissociation of the precursor gases, promoting chemical reactions that result in the deposition of silicon dioxide on the substrate surface. The deposition occurs at relatively low temperatures, making PECVD suitable for sensitive materials. In this work, the PECVD tool ‘Oxford Plasmalab 80 Plus’ is used which is based on a capacitively coupled RF (13.56 MHz) plasma in a vacuum chamber (parallel plate style), completely analogue to the used RIE etching tools and is presented in Figure 2.6. The process parameters, including gas flow rates, RF power, and chamber pressure, are carefully

Depositing material	Gases	RF Power	Process pressure
Silicon Dioxide (SiO_2)	170 sccm SiH_4 , 710 sccm N_2O	70 W	1 Torr

Table 2.5: Process parameters used for oxide deposition

controlled to achieve the desired film thickness, uniformity, and quality. The parameters used in this work are shown in Table 2.5



Figure 2.6: Plasma Enhanced Chemical Deposition machine used in this thesis.

2.1.4 Suspension of the devices

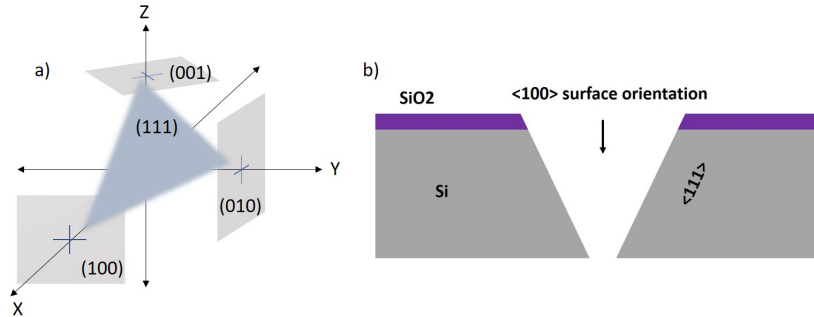


Figure 2.7: a) Silicon cubic crystal directions and b) anisotropic etching of Silicon.

Wet etching methods are known for their faster processing compared to dry etching methods, even though they offer less control over etch rates. Dry methods are advantageous for ensuring isotropy in etching progress, typically resulting in vertical profile sidewalls. On the other hand, wet methods, as demonstrated in this section,

exhibit anisotropic effects, particularly on specially-oriented Si wafer planes [116]. The crucial parameter influencing orientation-dependent Silicon etching is the atomic crystallographic structure and available bonds in the crystal plane. In this work, Si $\langle 111 \rangle$ wafers were used for the underetching procedure, leveraging the high anisotropy during exposure to KOH wet etch to fabricate suspended, releasable material layers. Figure 2.7a) shows the silicon cubic crystal directions and Figure 2.7b) represents this anisotropic etching. This approach simplifies fabrication, enabling a higher device density not achievable with isotropic etching. A deep RIE etch is employed to expose a significant portion of the underlying material, aiding the etch progress and ensuring smooth backside surfaces. An anisotropic wet potassium hydroxide (KOH) etch is crucial for the lateral removal of Si, with standard process conditions involving KOH dissolution in water at $85 \pm 3^\circ\text{C}$. The lateral etch rate along the $\langle 110 \rangle$ crystal direction of Si $\langle 111 \rangle$ substrates is exploited to create suspended GaN membranes [117]. Figure 2.8 shows the impact of KOH solution on the undercut of GaN membranes in steps at different times. It is also important to highlight the importance of this process for achieving specific device structures and discusses protective measures, such as SiO_2 layers, against the KOH solution's impact on GaN membranes [118].

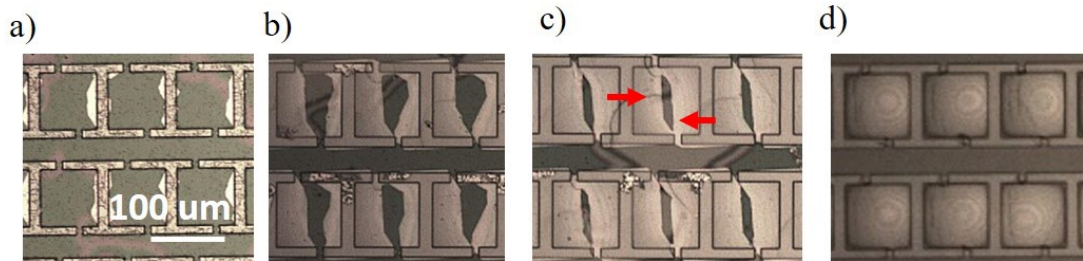


Figure 2.8: $100 \times 100 \text{ } \mu\text{m}^2$ GaN membranes on Si substrate after KOH etching on different times: a) After 10 minutes, b) after 30 minutes, c) after 45 minutes, and d) after 60 minutes

2.2 Characterization techniques

Characterization and metrology techniques are indispensable in microfabrication. These methods, such as scanning electron microscopy and atomic force microscopy, enable

quality control by assessing the dimensions, surface characteristics, and overall morphology of microfabricated features, ensuring they meet design specifications [119]. Additionally, these techniques play a pivotal role in optimizing microfabrication processes, offering insights into how different parameters impact the final product. Detecting faults, identifying defects, and analyzing material composition are facilitated by these techniques, contributing to the reliability and functionality of microfabricated devices. In this subsection, we briefly describe the method used in this thesis, and highlight their importance for the work.

2.2.1 Imaging

Optical microscope

An optical microscope is a vital tool in the characterization of microfabricated structures, offering invaluable insights into their morphology and dimensional features. Optical microscopes utilize visible light to magnify and observe microscale details, providing a non-destructive means of examining the surface characteristics of fabricated components. With high-resolution lenses and advanced imaging capabilities, optical microscopes enable precise visualization of microfabricated features, such as patterns, layers, and defects. This characterization aids in quality control by assessing the uniformity, alignment, and integrity of structures, ensuring they adhere to design specifications. Additionally, optical microscopes are instrumental in identifying surface irregularities, cracks, or other imperfections that may impact the functionality and reliability of microfabricated devices. The real-time, non-invasive nature of optical microscopy makes it a versatile and efficient tool for researchers and engineers engaged in the intricate processes of microfabrication, contributing to the optimization and quality assurance of microscale structures. A ‘Leica DMR’ optical microscope is used to collect images of samples at different stages of the micro-fabrication process with 5-50x magnification using a Thorlabs color camera with resolution 1440 x 1080 Pixel (1.6 MP), illustrated in Figure 2.9 a).

Scanning Electron Microscopy

A scanning electron microscope (SEM) operates by scanning a focused electron beam over the surface of a specimen, generating high-resolution images of its topography and morphology. In microfabrication characterization, SEM plays a pivotal role due to its ability to provide detailed imaging at nanoscale levels. When the electron beam interacts with the specimen, various signals are produced, including secondary electrons, backscattered electrons, and characteristic X-rays. These signals carry information about the surface structure, composition, and topography of microfabricated features. SEM's exceptional spatial resolution allows for precise examination of intricate details, such as patterns, particle sizes, and surface roughness. This information is crucial for quality control, enabling the identification of defects, irregularities, or variations in microscale structures. The 'Hitachi S-3000N' scanning electron microscope is used to obtain quasi-3D images with 10's to 100's of *nm* resolution of the created microstructures. Figure 2.9 b) shows the SEM system used in this thesis. This SEM employs a lower quality thermal tungsten filament as an electron source which limits the resolution in comparison to field emission sources. A strength of this particular SEM is the quick pumping time. A huge strength of SEM imaging is the large depth of focus. For the imaging of the fabricated devices, a voltage between 15-30 *keV* was used.



(a) Optical Microscope.



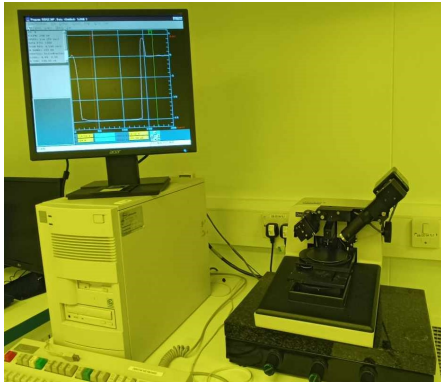
(b) Scanning Electron Microscopy

Figure 2.9: Imaging machines used in this thesis.

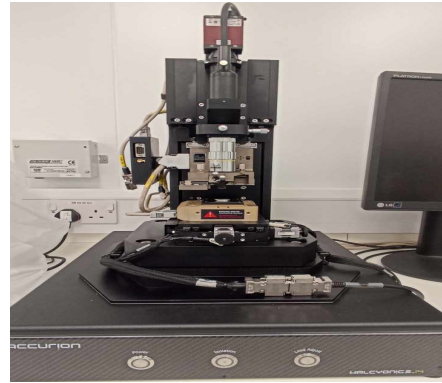
2.2.2 Profilometer

A profilometer is a metrology instrument used to measure the surface topography of materials at the microscale level. The device operates by gently scanning a stylus or a non-contact probe along the surface of the specimen. As the stylus moves, it detects variations in height, producing a height profile that represents the surface features. In contact profilometers, the stylus physically touches the surface, while non-contact profilometers use optical or acoustic methods to measure surface features without direct contact. The collected data allows the profilometer to generate a detailed three-dimensional map of the surface, revealing information about features such as roughness, step heights, and surface irregularities.

Stylus profilometers utilize a pointed, typically conical probe tip to evaluate the topography of a sample. This tip makes contact with the sample surface by applying a specified force and is then moved linearly while monitoring changes in the tip holder angle differentially to reconstruct a one-dimensional height profile. The feedback on height measurement can be achieved through various methods, such as laser reflection from the deflecting tip holder or alternative techniques like inductive transducers or piezoelectric elements, which convert position changes into electrical signals.



(a) Dektak Stylus Profilometer



(b) Atomic Force Microscope

Figure 2.10: Profilometers used in this thesis

Atomic Force Microscope

An Atomic Force Microscope (AFM) operates on the principle of scanning the surface of a sample with a sharp tip at the atomic or molecular scale to detect forces between the tip and the sample surface, allowing for three-dimensional imaging and manipulation of individual atoms. The evaluation of 3D surface topology with high measurement precision is conducted using a vibration-shielded atomic force microscope (AFM) from 'Park Systems.' This application is particularly relevant for assessing the root-mean-square (r.m.s.) roughness of significant surfaces, as well as topology. Within this AFM apparatus, a silicon cantilever equipped with a sharp tip is systematically scanned over the sample surface, employing a piezo controller for vertical movements. The resulting 2D force landscape, generated by probing the surface, serves as a key indicator of the surface topology. Both profilometers used in this thesis are presented in Figure 2.10

White light reflectometer

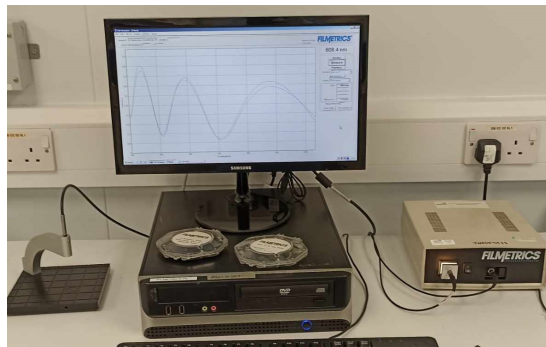


Figure 2.11: White light reflectometer used in this thesis

A white light reflectometer is an optical instrument designed for precise thickness measurements of thin films and coatings on a variety of substrates. The principle behind its operation is based on the interference of white light reflected from the surface of the film. When white light illuminates a thin film, some of it is reflected at the film's upper surface, while the rest penetrates and reflects off the substrate. These multiple reflections create interference patterns that are dependent on the thickness of the film. The reflectometer captures the reflected light spectrum and analyzes it to determine

the thickness of the film. By comparing the interference patterns with a reference, often obtained from a known standard, the instrument can accurately calculate the thickness of the thin film. White light reflectometers are widely used in industries such as semiconductor manufacturing, optics, and coatings, providing a non-destructive and highly precise method for thickness measurement in nanometer-scale applications. The ‘Filmetrics F20’ white light reflectometer measures the reflection spectrum of a sample with respect to a Si wafer calibration reference and is shown in Figure 2.11.

2.2.3 Fabrication process for large arrays of membrane devices

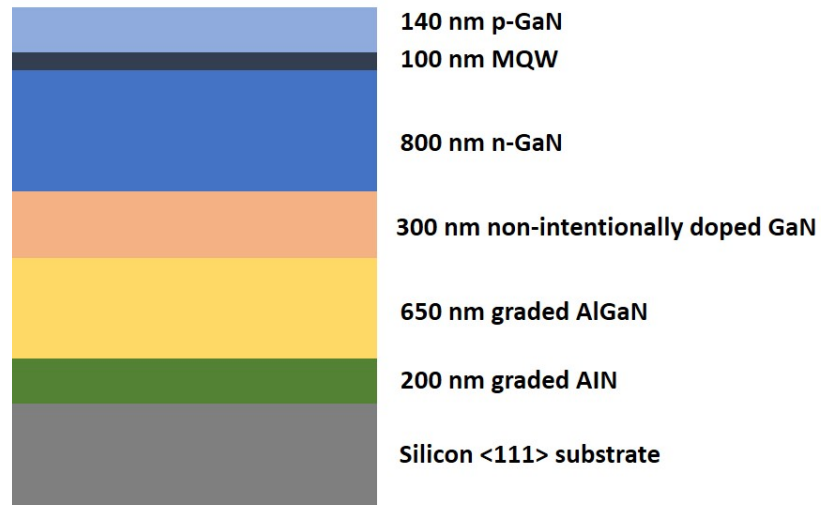


Figure 2.12: LED epi-structure of the wafer used in this work.

The process of transferring LED pixels from their growth wafer to a host substrate involves the physical release of these devices from their native wafer. In this study, III-N (III-nitride) optoelectronic devices are grown on silicon substrates, offering a convenient mechanism for selectively suspending epitaxial layers over the silicon substrate [120]. The LED epi-structure of the wafer used in this work is presented in Figure 2.12. The suspended pixels discussed in this work are part of an III-N-on-Silicon material platform widely employed for LED devices emitting at a wavelength of 450 nm. The fabrication process for creating these suspended pixel devices is detailed in [121].

For efficiency and a quicker turnaround in iterative optimization cycles, this work focused on mechanically suspended pixels, thereby reducing the number of steps re-

quired for sample production. A schematic of the fabrication process of suspended GaN membranes is presented in Figure 2.13. While active LED devices on this material would involve additional steps for electronic contacts and insulation layers, these do not impact the mass transfer process under consideration.

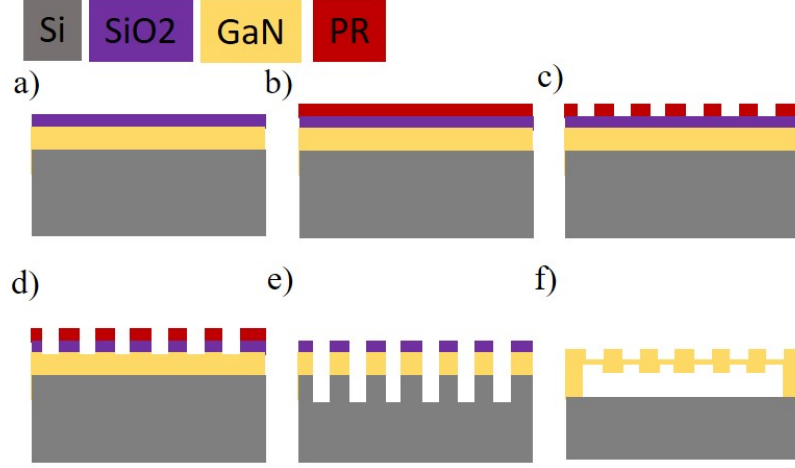


Figure 2.13: Schematic representation of the fabrication process of suspended GaN membranes: a) After PECVD, b) after spin coating, c) after photolithography, d) after RIE for silica, e) after ICP and RIE for silicon and f) after KOH for devices suspension.

To create the suspended pixels, a SiO_2 hard mask is deposited on the III-N material, followed by spin coating with a positive-tone photoresist. The suspended membrane pixel patterns are then exposed in the photoresist mask using a direct-write laser lithography system, facilitating rapid prototyping of various tether geometries. However, these device geometries remain compatible with standard photomask processing. The photoresist mask is subsequently transferred into the silica hard mask using a CHF_3 reactive ion etch. Finally, the pattern is transferred into the semiconductor layers using an Diargon and Chlorine gas ($Ar_2 : Cl_2$) inductively coupled plasma reactive ion etch (ICP-RIE). The Si layer is anisotropically underetched using potassium hydroxide (KOH), resulting in voids in the Si material under the III-N pixels. The impact of each process step on the fabrication of the membranes is shown in Figure 2.14

The resulting suspended membranes are supported by two anchors to surrounding support material, allowing for fracture during the pick-up process to release the mem-

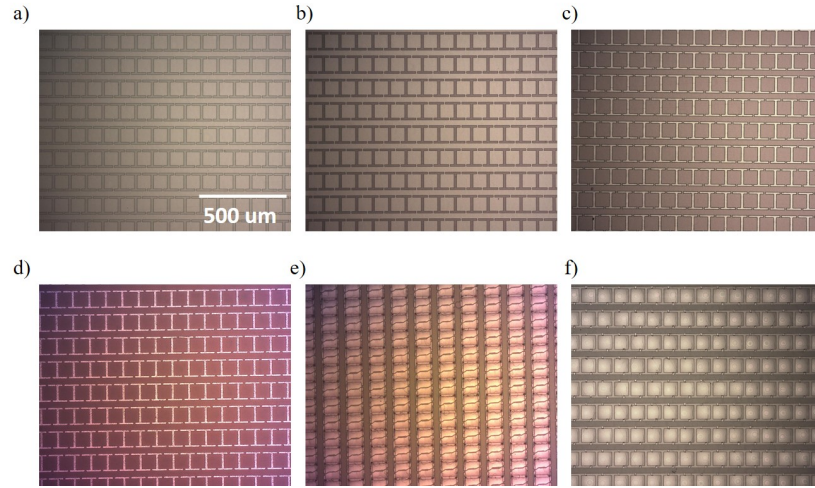


Figure 2.14: Microscope 10x magnification images after fabrication steps (same scale for all the images): a) after patterning of the photoresist, b) after transferring the pattern down to silicon dioxide, c) after transferring the pattern down to gallium nitride, d) after transferring the pattern down to silicon, e) half way of the underetching of the membranes and f) final suspended membranes.

brane, as it can be seen in Figure 2.15. This detailed process ensures the controlled and precise creation of suspended III-N pixels for subsequent integration into the desired host substrate. Example of fabricated arrays of micro-LEDs and mini-LEDs are shown in Figure 2.16

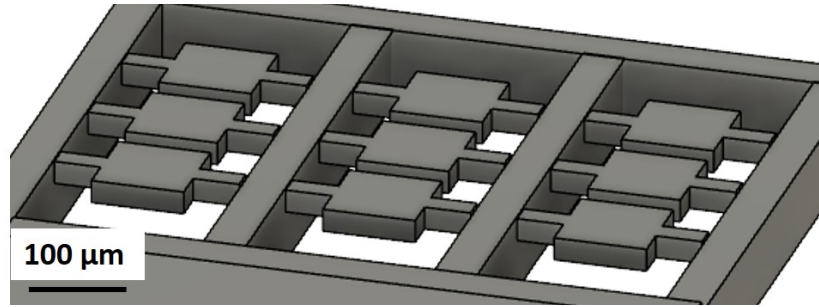


Figure 2.15: Schematic of the suspended membranes supported by two anchors

2.3 Continuous roll-transfer printing

Transfer printing is a highly advantageous technology for membrane devices, enabling the seamless integration of components from various material platforms onto a single

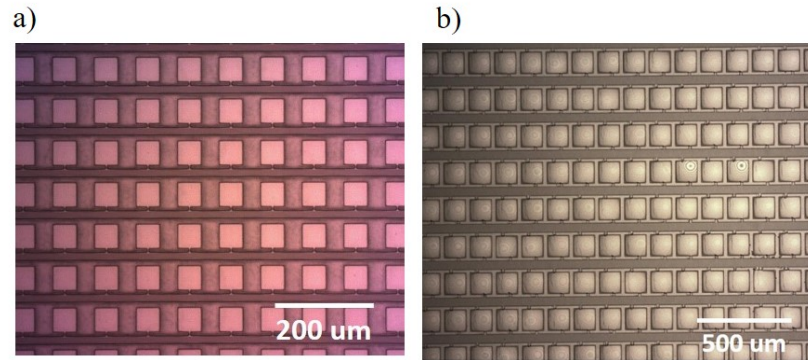


Figure 2.16: Final fabricated arrays of suspended devices: a) micro-LEDs and b) mini-LEDs

substrate. This technology has gained significant traction in the display industry, both for large and small devices, through hybrid integration methods. Among the various techniques for transfer printing, the polymer stamp-based pick-and-place method is the most prevalent. This approach employs a viscoelastic material, typically a PDMS stamp, to lift devices from a donor substrate and transfer them to a receiver substrate. The process relies on the adhesion properties of PDMS and the bond between the materials being transferred, utilizing van der Waals forces or a surface adhesive layer.

Despite several successful demonstrations, scaling up production using this technology remains a significant challenge. To address this, a continuous roller transfer printing method has been developed, capable of printing tens of thousands of devices simultaneously with high throughput. Roll transfer printing offers several advantages over other techniques. It eliminates the need for generating external forces (such as magnetic, electric, or optical fields) and does not require challenging environmental conditions. Additionally, as a continuous process that does not require to disengage the roller, it allows for the simultaneous printing of multiple devices, making it highly efficient for large-scale production.

The key benefit of roll-to-roll transfer printing over traditional pick-and-place flat transfer printing lies in its pseudo-one-dimensional contact area. Flat dies, which require precise planar alignment, are difficult to scale over large areas. In contrast, roller dies have a contact surface that can be aligned parallel to the roller axis. By mov-

ing this one-dimensional contact area across the substrate, the entire substrate can be processed in a single continuous pass, thus facilitating the scalability of this method for future applications. In the following subsections, the details of the continuous roll transfer printing experimental setup and process is presented.

2.3.1 Experimental setup

Figure 2.17 illustrates the 3D schematic of the custom-designed setup used in this study. The single-shot roller printing technique was employed with a specialized configuration centered around a commercially available silicone rubber compound roller. This roller has dimensions of 40 *mm* in diameter and 60 *mm* in axial length, providing a lightweight and compact design that facilitates bidirectional device pick-up. To control the height of the roller in relation to the stage surface and regulate the applied pressure on the donor and receiver chips, a high vertical load translation stage was incorporated. Specifically, the Thorlabs' Long Travel Vertical Translation Stage was utilized for its ability to accurately position optomechanical systems. This stage can handle moments as high as 16.9 *Nm* with a recommended maximum load of 23 *kg*. Constructed using dynamically damped Ø1.5" posts to minimize mechanical vibration and ringing, these stages are well-suited for alignment-sensitive applications. The Vertical Stages allow for a translation of 254 *mm*, and the fine adjustment knob on the top of each stage can be operated by hand or with a 5 *mm* hex key or balldriver, resulting in a motion of 1.27 *mm* per revolution. It's important to note that the torque required for the fine adjustment knob increases with the load on the stage. For coarse adjustment over an extensive travel range, the stage features a quick-release button. Holding down the button disengages the stage from the lead screw, enabling manual adjustment of the mounting plate position. A pin attached to the back of the stage, connected by a ball chain, can be employed to lock the quick-release mechanism, preventing inadvertent use of the coarse adjustment feature. To minimize potential damage during coarse adjustment, two bumpers on the base plate of the stage provide additional protection. Once the desired stage height is achieved, two included C15QR handles can be utilized to secure the post clamps holding the mounting plate, ensuring extra stability.

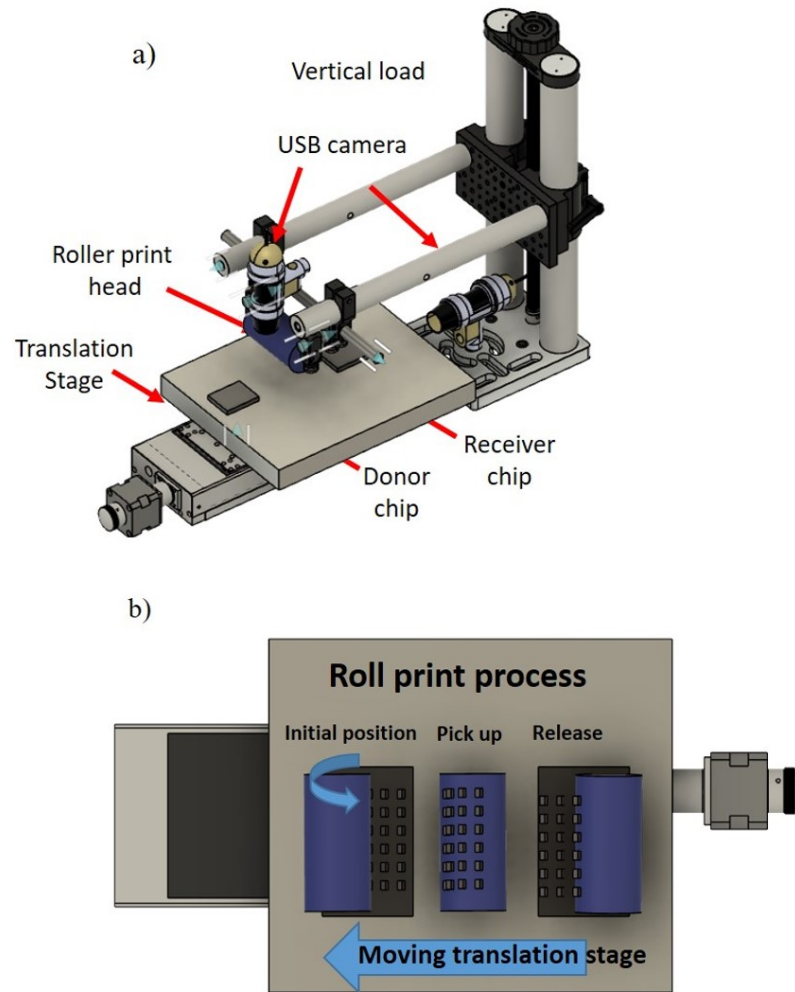


Figure 2.17: Schematic representation of the roll printing setup. (b) Printing process (left to right), devices are released from a donor onto the roller print head and then released onto a receiver chip

To ensure smooth rotation of the roller during stage translation, the system was operated at the minimum of vertical load, as excessive load can deform the roller's surface from its intended cylindrical shape [122], [123]. The roller is mounted on ball bearing hubs to minimize axial friction, with these bearings being designed and 3D printed to precisely match the roller's sides (internal hole) and the diameter of the post clamp, as it can be seen in Figure 2.18. The translation stage employed in this system

is an automated setup with a $2\text{ }\mu\text{m}$ on-axis accuracy, a travel range of 150 mm , and a maximum speed of 30 mm/s . This Linear Positioning Stage is optimized for applications demanding both high load capacity and high resolution, such as measurement and inspection tasks. It provides 150 mm of linear travel for loads up to 20 kg when mounted horizontally. Each stage features a typical on-axis accuracy of $2.0\text{ }\mu\text{m}$ ($5.0\text{ }\mu\text{m}$ Max) when using the included calibration files with Thorlabs' Kinesis® or APT™ software. The lead screw, directly driven by a two-phase stepper motor capable of 409,600 microsteps per revolution, ensures smooth translation with a theoretical positional resolution of less than 100 nm . Notably, the platform position remains fixed when no power is supplied to the stage, a feature absent in DC servo motor translation stages. The primary platform is supported by four recirculating ball carrier bearings mounted on precisely aligned linear guide rails. The specially designed stepper motor, optimized for microstepping applications, allows for smaller and smoother low-speed motion with significantly reduced vibrational noise compared to DC servo motors. To drive this 150 mm translation stage, one of Thorlabs' benchtop stepper motor controllers is required. These controllers are compatible with Kinesis and APT™ software, providing out-of-the-box stage control from a PC and supporting common programming interfaces such as LabVIEW, LabWindows™, and ActiveX. In this specific setup, the Kinesis software is employed.

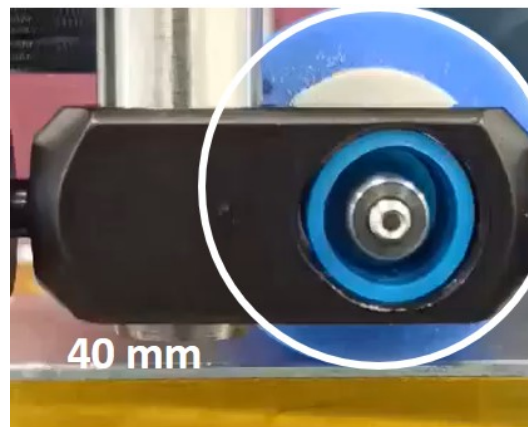


Figure 2.18: Side picture of the roller, illustrating the side mounting of the roller and the bearings used to minimize side friction.

The experimental arrangement includes two microscope cameras properly positioned for comprehensive observation of the printing process. One camera is situated directly above the roller, while the other is oriented perpendicular to the leading edge of the roller, as shown in Figure 2.17. These digital microscopes are equipped with achromatic objective lenses, offering a maximum magnification capability of 1,000x. Each microscope features eight built-in LED lights, weighing 0.23 *kg*. These digital microscopes are designed with practicality in mind, incorporating two adjusting knobs on the side to facilitate changes in both focus and brightness. With a real angle of view of 120 degrees, these microscopes operate at 5 Volts and support 4K (3840x2160) picture snapshots and video recording. Notably, the microscopes offer the convenience of wired connectivity, ensuring fast and reliable data transmission. In comparison to WiFi microscopes, where pixel compression is often required for WiFi transmission, these USB microscopes with 2K resolution can effortlessly transmit 3.7 million high-definition images through the data cable. This allows for seamless integration with mobile phones and computers, providing rapid data transfer in a matter of seconds. The decision to opt for a wired connection not only ensures fast data transmission but also enhances the overall reliability of the imaging system.

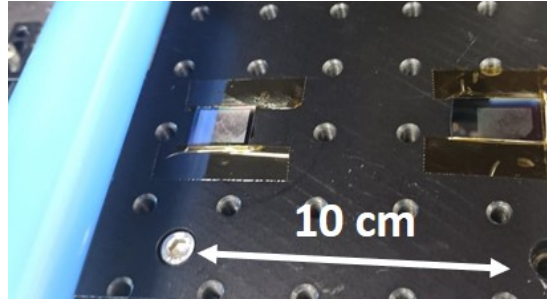


Figure 2.19: Illustration of the one-roll printing

The experiment involves securing the donor and receiver chips on a translation stage, positioned a few centimeters apart to facilitate a one-roll printing process, as depicted in Figure 2.19. To anchor the chips in place, a thin tape is employed along the edges, ensuring stability during the printing procedure. The detailed designs of the donor and receiver chips are elucidated in Section 3. The single-shot roller printing process sequence can be summarized as : (1) The donor and receiver chips are carefully

positioned on the translation stage, maintaining a separation equivalent to the circumference of the roller. (2) The roller surface is brought into contact with the translation stage, applying sufficient vertical load to initiate rotational motion without any mechanical slippage between the roller and stage surface. (3) The translation stage is set in motion at a constant velocity of 1 mm/s, causing the donor chip to traverse under the roller. During this phase, the devices are released from their suspended positions and adhere to the roller's surface. (4) The roller completes a full rotation driven by the translation stage until it comes into contact with the receiver chip. (5) Subsequently, the devices on the roller surface establish contact with the receiver chip, facilitating the transfer of the devices onto the receiver's surface. This process ensures precision and controlled movement, essential for the successful execution of the single-shot roller printing technique.

2.3.2 Roller print head surface

To achieve a large-scale, high-yield transfer, the surface properties of the roller transfer head are pivotal, particularly at the micron scale. The investigation is focus on silicone rollers commonly used in surface cleaning applications, comparing three variants based on their surface roughness. Past studies have highlighted the potential for non-uniformities in roller printing due to deviations in the cylindrical profile of the roller [124]. While applying pressure to the roller can address longer-range non-uniformities, local surface roughness remains a challenge.

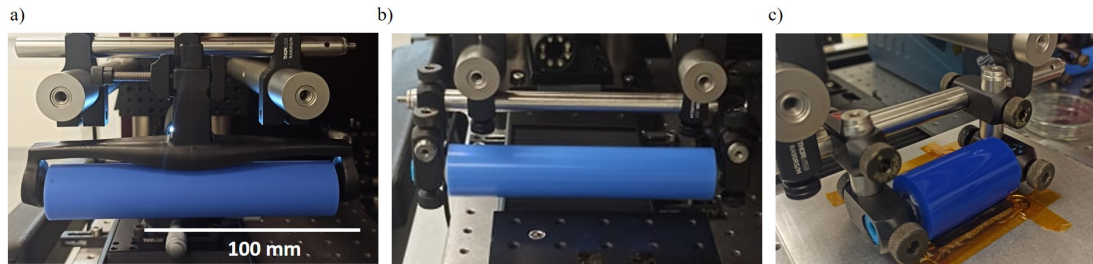


Figure 2.20: The three different rollers used in this thesis: a) Roller with high roughness, b) roller with medium roughness and c) roller with low roughness

In the study, nominally identical donor and receiver chips were employed with three

silicone rollers characterized by low, medium, and high surface roughness, respectively and the rollers used can be seen in Figure 2.20. Surface roughness was assessed by excising small portions of each roller’s material and imaging them using an atomic force microscope (AFM), as illustrated in Figure 2.21. The large-scale peak-to-peak surface roughness for the three rollers was measured at approximately $18\ \mu m$, $1.4\ \mu m$, and $0.3\ \mu m$, respectively. Figure 2.21 also presents the outcomes of test printing pixel arrays with each roller. Notably, rollers with higher roughness values exhibited device transfer, but with a significant loss of devices and positional shifts from the uniform array. Conversely, the roller with $0.3\ \mu m$ surface roughness demonstrated faithful device transfer, showcasing optimal transfer output and minimal spatial deviations from the as-fabricated uniform array grid arrangement. This observation aligns with the expectation that, given the small size of the devices, minimizing surface roughness enhances the contact area between the roller and the pixel, resulting in better printing quality for the device array. For both the demonstration of an 80×80 device array mini-LED with individual elements measuring $100 \times 100\ \mu m^2$, spaced at $170\ \mu m$ with a $120\ \mu m$ center-to-center arrangement (179 dpi), as well as for the demonstration of the full 320×240 pixel array transfer, featuring elements of $30 \times 30\ \mu m^2$ and a center-to-center spacing of $50\ \mu m$ (549 dpi), the roller with $0.3\ \mu m$ surface roughness was selected. Detailed presentation and analysis of the printed devices will be provided in Chapter 3.

Following the aforementioned results, additional insights pertaining to the roller specifically refer to the variant with $0.3\ \mu m$ surface roughness, chosen for the final configuration.

The roller, made of silicone rubber, features a surface with low relative roughness, moderate viscosity, lightweight composition, and particle sizes less than $2\ \mu m$. While detailed technical specifications are limited due to its commercial availability, the basic properties of silicone rubber are well understood. Composed mainly of siloxane (Si–O) bonds, exhibits molecular structures where siloxane bonds have a higher bond energy ($106.0\ kcal/mol$) compared to carbon bonds (C–C) which have $84.9\ kcal/mol$. This indicates that siloxane bonds offer greater capacity and stability [125], [126]. Conse-

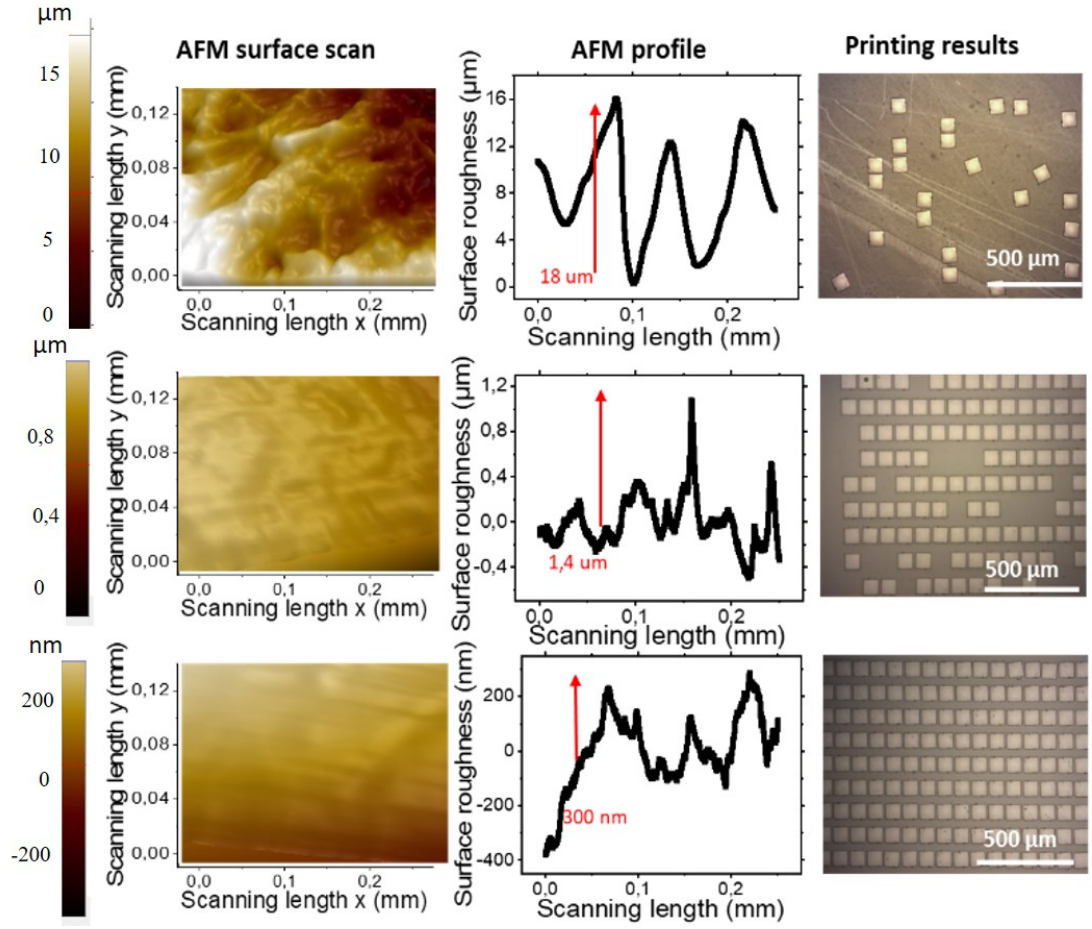


Figure 2.21: . Illustration of the effects of roller surface roughness on transfer printing process. Left hand side and center columns show AFM surface and profile scans respectively for three roller print heads with different surface roughness. The red arrow on AFM profiles indicates the ‘peak-to-peak’ values. The right hand side column shows optical microscope images of the roller transfer printing results from nominally identical donor chips using the respective rollers

quently, silicone rubber demonstrates superior heat resistance, electrical conductivity, and chemical stability compared to other conventional organic rubbers [127]. Typically, silicone rubber is characterized by low surface energy, potentially up to 30 mJ/m^2 depending on the manufacturing process, although surface or curing modifications can render it sticky [128], [129]. One of its most notable properties is heat resistance. Silicone rubber can withstand continuous use for over 10,000 hours at 200°C , and for shorter durations, it can endure temperatures up to 300°C . While the embrittlement

point for most organic rubbers ranges between -20°C to -30°C , silicone rubber maintains flexibility down to -60°C to -70°C . The tear strength of standard silicone rubber is approximately 9.8 kN/m , with high-strength variants achieving tear strengths between 29.4 and 49.0 kN/m through polymer modification and careful selection of fillers and cross-linkers. Silicone rubber also boasts flex fatigue resistance—its ability to endure continuous flexing and bending without cracking—is 8–20 times higher than that of conventional products [130]. Silicone rubber exhibits exceptional weatherability. Unlike most organic rubbers that deteriorate rapidly when exposed to ozone produced by corona discharge, silicone rubber remains unaffected. It can also withstand prolonged exposure to wind, rain, and UV rays without significant changes to its physical properties. Furthermore, it absorbs only 1% moisture even after prolonged water exposure, maintaining its mechanical strength [131]. After each full roll process, the roller is cleaned either by adhesive pads commonly used for roller cleaning or by rinsing under clean, warm water. The wet roller surface becomes slippery, aiding in the removal of excess dirt or dust accumulated during the rolling process. When dry, the roller retains its initial sticky properties due to its water resistance and hydrophobic nature.

2.3.3 Membrane device design for high yield roll-transfer printing

The comprehensive fabrication process for a large array of devices is outlined in Section 2.2. Within this section, we conduct a parametric study focusing on the design of the device. Specifically, we varied the shape, position, and dimensions of the anchors in III/V on Si test structures to evaluate their compatibility with the roller printing process. In comparison to standard planar pick-and-place transfer printing methods [86], [132], the roller printing method introduces two distinctive aspects in the contact between the devices to be transferred and the pick-up head. Firstly, contact with the devices is not simultaneous across their entire surface; instead, the array is picked up in a serial, row-by-row manner. Secondly, the curved surface of the roller and the directionality of the contact progression can induce torsion of the membranes. The effects of these factors are contingent on the membrane size and the roller’s radius of curvature (ROC). Larger ROC rollers and smaller membranes are less likely to be

affected by torsional effects, as the surface-to-surface contact becomes more uniform during the printing process.

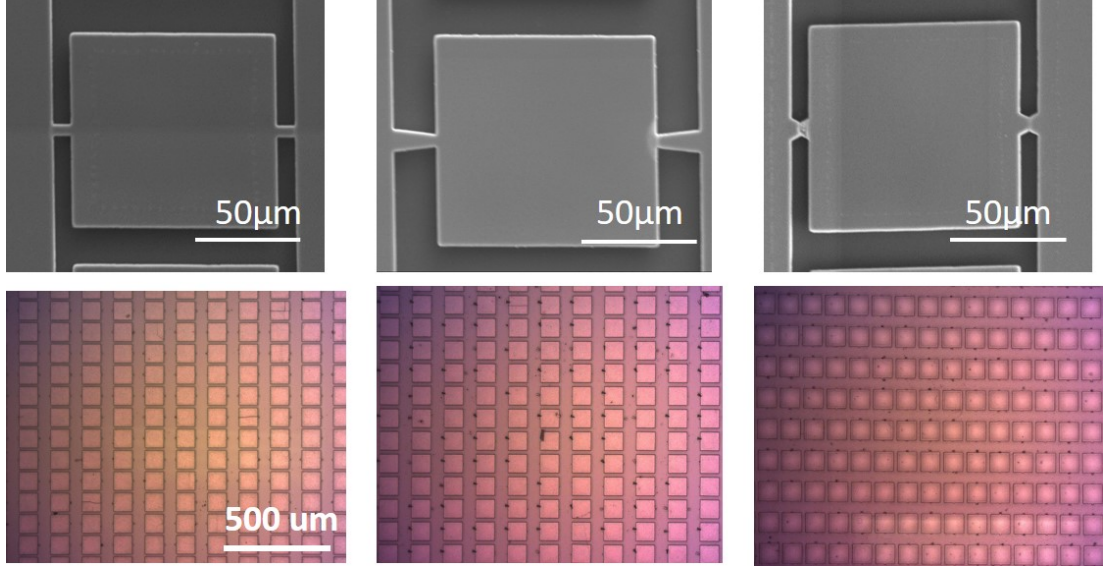


Figure 2.22: Plan view of SEM images of three pixel anchor designs and corresponding printed arrays, from left to right: rectangular, triangular, bow-tie

To investigate the mechanical effects of anchor geometries on printing yield, test membranes with dimensions of $100 \times 100 \mu m^2$ were fabricated, incorporating variations in tether shape and relative position to the membrane structure. Three main anchor geometries were tested: rectangular, tapered, and bow-tie shaped, as illustrated in Figure 2.22. Each shape corresponds to different breaking points during the pick-up process, with critical dimensions ranging between 2-10 μm . For repeatable tether cleaving and membrane stability, the following anchor dimensions were determined: i) $10 \times 5 \mu m^2$ for rectangular shape, ii) 7 μm long and 10 - 5 μm in width for the tapered geometry, and iii) 10 μm long, 4 μm major dimension width, and 2 μm minimum width for the bow-tie shaped anchors. Figure 2.22 showcases scanning electron microscopy (SEM) images of the selected anchor designs after suspension on their native silicon substrate. Notably, each of these designs performed equally well in printing trials.

In addition to tether geometry, we explored the placement of tether supports relative to the membrane layout. While planar transfer printing processes often utilize tethers arranged asymmetrically around the membrane's central axis, the roller printing

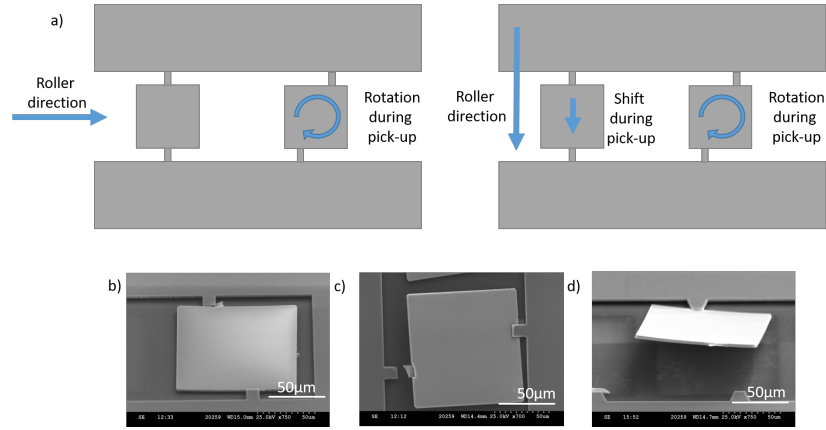


Figure 2.23: a) Plan view schematic of the various effects during membrane pick-up dependent on the anchor location geometry and roller translation direction. SEM images of examples of b) collapsed membrane c) shifted membrane trapped by anchor support, and d) rotated and partially released membrane.

method necessitates a different approach due to the previously mentioned torsional effects. Asymmetrical tether positions, in this case, can induce rotation of the membrane around an axis normal to its center of surface area, as the roller's surface-to-membrane contact is non-uniform and varies during pick-up and release processes. The rotation is also influenced by the direction of travel of the roller in relation to the tethers, as depicted in Figure 2.23a). Figure 2.23 b),c) and d) provide examples of failed membrane pick-up resulting from these rotational effects, wherein devices may fail to release, collapse onto the substrate, or slide under the mechanical support structures surrounding the pick-up area, depending on the direction of roller travel. Figure 2.24 presents some representative results of the donor after roll-printing, as well as the corresponding printed devices in the case that asymmetrical tethers were used. This figure summarizes all the defects that can encounter in this case.

For smaller pixel dimensions, a single tether geometry may suffice. For the demonstration of single-shot roller printing, membrane pixels with dimensions of $30 \times 30 \mu m^2$ and a center-to-center pitch of $50 \mu m$ were fabricated (549 dpi). An array of 320×240 such pixels was used, corresponding to a quarter video graphics array (QVGA) with a total of 76,800 individual pixels. The silicon receiver chips were coated with a thin adhesive layer of fast-cured adhesive optical polymer (Norland NOA 81) to aid device

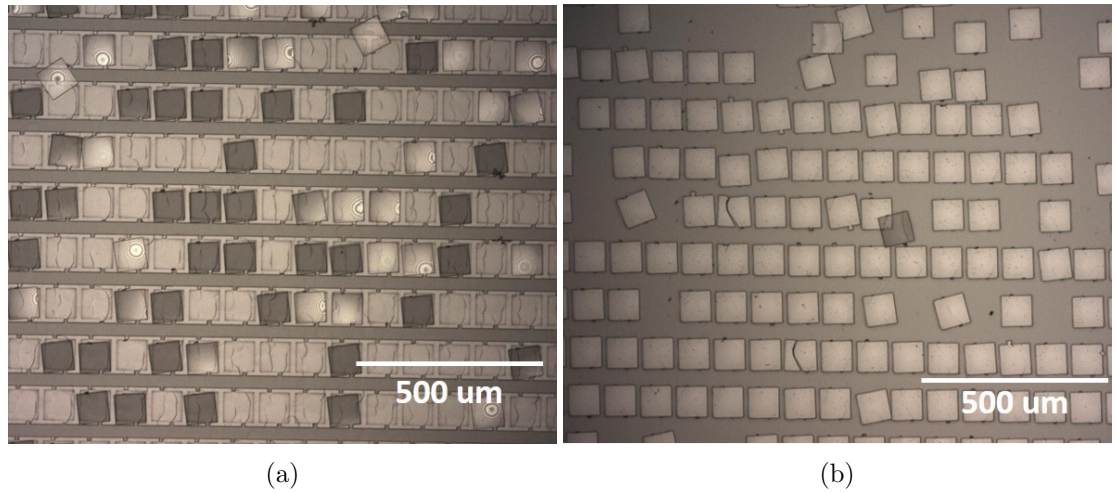


Figure 2.24: Representative results of asymmetrical tethers positioning: a) donor after roll-printing and b) resulted printed array.

release from the roller transfer head.

Norland NOA 81 is an optical adhesive coating with exceptional optical clarity and adhesion properties. Its low viscosity allows for easy application, providing a uniform and thin coating on various surfaces [133]. This coating possesses excellent light transmission characteristics, making it suitable for optical devices. Importantly, NOA 81 is engineered to be non-conductive, ensuring it does not interfere with the electrical performance of coated devices. Furthermore, its refractive index closely matches that of glass, minimizing optical distortions and reflections. Its stability over a broad temperature range and resistance to yellowing make it a durable choice for optical applications.

2.3.4 Chip size and edge effects

In this research, the focus is on transferring a substantial number of devices, highlighting the criticality of ensuring the successful fabrication of micropixels across the entire chip. To optimize the fabrication process, a larger dicing size than the standard chip dicing size, as discussed in the preceding section, needs to be employed, as the entire area of the QVGA aligns with the dimensions of the chip. The new dicing size to avoid this issue is $24 \times 20 \text{ mm}^2$. Figure 2.25a) shows the new diced wafer and Figure 2.25b) shows the differences in the size on the diced chips.

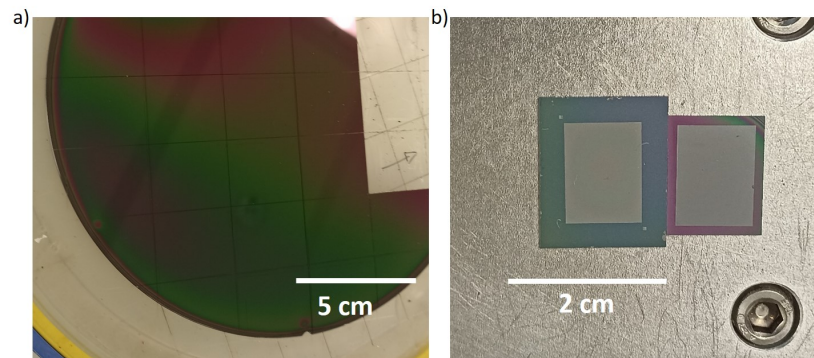


Figure 2.25: a) New diced wafer and b) comparison between the two different dices used in this thesis

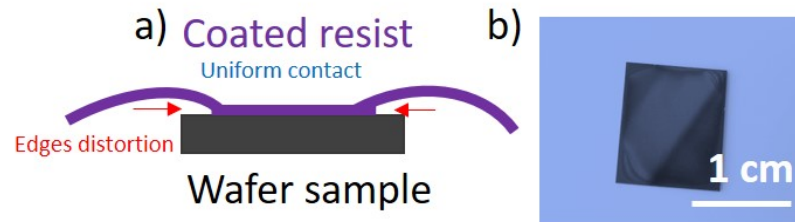


Figure 2.26: Edge effect of spin coating. a) Schematic illustration and b) example of a spin coated sample

This change has notable implications for the fabrication workflow, especially during the spinning phase, as challenges can arise, particularly concerning edge uniformity. The centrifugal force involved in the spin coating process may cause a thickness gradient across the substrate, resulting in a thicker center compared to the edges, especially notable in larger substrates. Figure 2.26 a) presents a schematic of this effect while Figure 2.26 b) shows a real example of a spin coated sample, where the fringes at the edges represent the small gap between the resist and the surface. Additionally, edge exclusion effects can lead to different coating dynamics at the substrate periphery. Researchers often address these edge issues by carefully optimizing spin speed, duration, and other parameters, and by considering alternative coating techniques, such as spray coating [134]. Despite its efficacy, achieving uniformity across the entire chip surface remains a critical consideration in spin coating applications. The non-uniformity resulting from spin coating can have wide-ranging implications for subsequent fabrication steps. Challenges arise in processes like photolithography and etching, where uneven

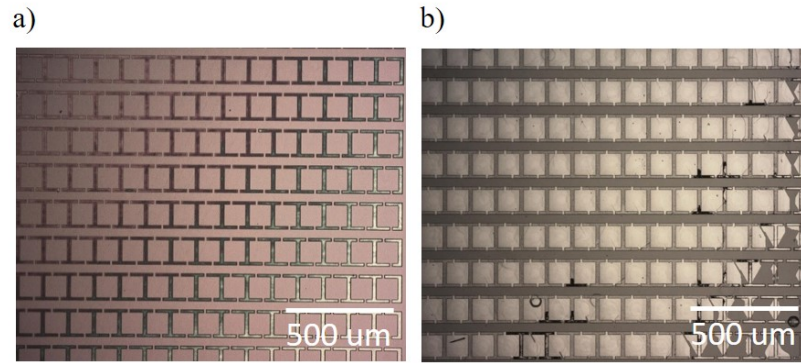


Figure 2.27: Representative examples of fabrication issues on the edges of the chip: a) After ICP and b) after KOH

film thickness complicates pattern transfer, potentially causing defects. Non-uniformity may lead to uneven etching rates, affecting the precision of features and potentially causing defects in the final device. In the pursuit of high yield and consistency, non-uniform spin coating introduces a higher risk of defects, reducing overall production reliability. In this work, achieving high yield and consistency in device fabrication is critical. The uniformity of plasma-enhanced chemical vapor deposition (PECVD) deposited silica across a semiconductor chip can be an issue as well. Side effects, such as non-uniform film thickness, can arise due to factors like the size of the wafer and its topography, experiencing edge effects and variations in plasma distribution. The design of the gas distribution system within the PECVD chamber also plays a role, impacting the distribution of precursor gases and, consequently, the uniformity of the deposited silica layer. Maintaining a uniform temperature across the wafer is critical to preventing variations in film thickness. However, edge exclusion effects, similar to those seen in other deposition methods, may lead to differences in film thickness near the wafer edges compared to the center. Figure 2.27 presents some representative examples of fabrication issues that can arise from the reasons mentioned above in the next fabrication steps. In Figure 2.27a), the non-uniformity on the etching process of GaN is optically noticeable from the different colors in the areas of interest, while in Figure 2.27b), the undercut of the membranes revealed the inappropriate patterning on the sides.

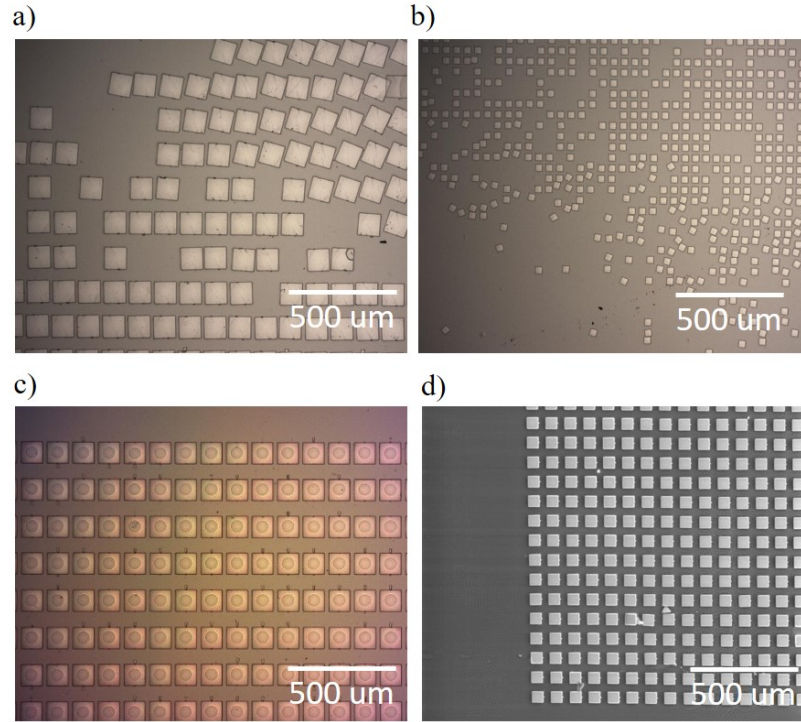


Figure 2.28: Roll-printed arrays, showing the edge effect issues and resolved results by changing the chip size for a),c) mini-LEDs and b),d) microLEDs.

The crucial factor arises during the roll printing process, where the roller's uniformity is compromised when in contact with the array columns situated on the sides. This inconsistency is attributed to a step between the device and the translation stage. Because the devices are positioned in close proximity to this step, the roller exhibits discontinuous areas. While this local mismatch facilitates the pickup of devices, it leads to the transfer of printed devices with unintended rotation as it can be seen in Figure 2.28 a) and b). By dicing the wafer in larger pieces, the side issue was eliminated and the results of these can be seen in Figure 2.28c) and d) for mini-LEDs and micro-LEDs, respectively.

2.3.5 Chapter summary

In this chapter, the complete fabrication process for large arrays of membrane devices was detailed. Each step of the fabrication was described, with an emphasis on the spe-

Chapter 2. Fabrication of large membrane device arrays and roll-transfer printing

cific requirements for making the membranes suspended, allowing them to be released from their substrate for transfer printing. A novel transfer printing method based on continuous roll-transfer printing was introduced, with both the mechanical setup and the physical mechanisms involved being outlined. Additionally, the fabrication challenges that can impact the roll-printing process and their effects on achieving high-yield fabricated arrays were discussed. The chapter concludes with solutions to these issues, underscoring the importance of fabrication yield in the roll-transfer printing process.

Chapter 3

Automated inspection method for large array devices and analysis

In this chapter, a new method to characterize and analyse large arrays of planar optoelectronic devices will be introduced. This will be divided into two main parts. One is the high throughput optical microscopy system and setup, and the second the computational analysis method based on image processing and cross correlation. To validate the accuracy and the precision of this method, a detailed analysis of photolithographically patterned devices will be presented, after fabrication and prior to any printing process. Finally, the method will be used in order to characterize mini-LED arrays and a whole quarter VGA (Video Graphics Array) printed by the roll-transfer method that was described in Chapter 2. The full inspection of the printed chip will be presented, including transfer yield and positional accuracy, showing 99.9% local yield and less than 1 μm positional accuracy for more than 75,000 devices.

3.1 Automated sub-micron accuracy inspection method

In the mass production of hybrid opto-electronic devices, a critical challenge lies in swiftly determining the precise positions of numerous devices with an accuracy reaching

the 100 *nm* range [135]. This assessment must be rapid and feasible with straightforward process to seamlessly integrate into the manufacturing process.

To meet this challenge, a computational image processing method has been developed for the analysis of extensive areas containing printed devices, employing low-magnification optics. Through an image processing analysis based on a cross-correlation method, individual device central coordinates and rotational orientation can be determined with sub-micron accuracy. This holds true even when the minimum optical resolution of the microscopy system is within the micron range. Consequently, large arrays of devices can be characterized using a single high-resolution image that covers the entire chip, with the resolution's importance lying in the fact that accuracy is limited to the pixel resolution of the image [136]. Utilizing a high-resolution image allows for sub-micron accuracy for thousands of devices. Another noteworthy aspect of this method is the ability to select the required accuracy for a specific application. Generally, there exists a trade-off between accuracy and the time required for scanning analysis. Depending on the precision needed for a given application, this balance can be adjusted accordingly. This renders the method particularly efficient for micron-accuracy printing. The subsequent sections aim to illustrate the maximum resolution achievable with this method, with a focus on the discussion of sub-micron accuracy analysis.

3.1.1 High-Throughput Optical Microscopy

In the case of inspecting a large array of devices, handling a substantial amount of data, particularly in imaging where accuracy is tied to pixel resolution is crucial. Different magnifications can be achieved using various optical objectives, leading to distinct effective pixel resolutions. However, increasing resolution also reduces the field of view, posing challenges when imaging an entire millimeter scale chip. Imaging an area of 10^{-2} square meters (1 cm^2) with an accuracy of 10^{-6} ($1\text{ }\mu\text{m}$) is challenging primarily due to the four orders of magnitude difference between the total area and the desired resolution. This means the imaging system must resolve details that are 10,000 times smaller than the overall area being imaged, necessitating extremely precise and sta-

ble equipment. High-resolution imaging systems must maintain consistent micron-level accuracy across centimeter-scale areas, which is challenging due to the limitations of optical lenses that can introduce aberrations and mechanical stages that must move with sub-micron precision without causing vibrations or drift. Additionally, maintaining such high accuracy over a large field of view requires rigorous calibration and environmental control to mitigate the effects of temperature changes, air currents, and other external factors that can cause minute shifts. The vast scale difference also complicates data acquisition and processing, as capturing detailed images at this resolution generates enormous amounts of data that require efficient handling and analysis. Thus, the challenge lies in bridging the gap between these vastly different scales while maintaining precision and stability. An automated process is necessary to assess the yield of the transfer process and detect distortions in the spatial pixel arrangement of over 75,000 devices.

In response, the development of both hardware and software tailored for the automated analysis of extensive membrane arrays is proposed. To assess a large ensemble of devices, we used a custom-built scanning system based on a commercial microscope (LEICA DM2700M) [137]. The system includes a high-precision, computer-controlled piezo translation stage (SmarAct SOM-MS-8080) with a high-resolution sensor, offering an accuracy of approximately 4 *nm* as specified in the datasheet [138]. Coupled with a CMOS camera (Thorlabs, DCC1645C [139]), this setup enabled the scanning of target samples, saving and processing captured images, and combining them into large collages for further analysis. Figure 3.1 shows this custom-made optical microscopy system, highlighting the sample holder on top of the nanometer precision translation stage. The automated microscopy system is equipped with various optical objectives, ranging from 5x to 100x magnification, which were used for both coarse and fine scanning of the samples. This system was employed to measure the yield and accuracy of the presented roller-printing method by scanning samples containing over 75,000 individual pixels. Optical microscope images were captured using a commercial CMOS camera 1.3 MP (1280 x 1024 pixels) with a nanometre accuracy translation stage as the sample holder. Automated scanning measurements were precisely stitched together, forming

Magnification	Pixel size (μm)	Field of view (mm^2)
5x	0.91	1.08540723
10x	0.45	0.2654208
20x	0.23	0.069337088
50x	0.094	0.0115815219
100x	0.047	0.0028953805

Table 3.1: Microscope camera magnification with corresponding pixel resolution and field of view

large effective field-of-view images. The low stage drift and rapid acquisition minimize stitching errors to the nanometer range.



Figure 3.1: High throughput optical microscopy system with a close up section of the nanometer stage sample holder

The system was built by a colleague in our group for scanning and analyzing samples containing large arrays of devices at high resolution. By selecting specific optical objectives on the microscope, we can switch between different magnifications and adjust the field of view accordingly. For further analysis, the relative pixel size was measured, which can be see in Table 3.1, using an image processing script in Matlab, which will be described in the following sections.

For our device analysis, two imaging configurations were employed: Firstly, a 50X magnification objective lens was used, resulting in a pixel size of approximately 94 nm . However, this configuration reduced the field of view to 0.0116 mm^2 , requiring more images and thus significantly increasing scanning time and dataset size. Thus, a 10X

magnification objective lens was also used, with a pixel size of 452 nm and field of view 0.265 mm^2 . This configuration was particularly beneficial for evaluating complete 320×240 device arrays and confirming the transfer yield.

By taking 10,000 images and averaging the time, it was estimated that each scanning step takes approximately one second, meaning it takes one second to move the stage and save the image. This relatively slow speed is largely due to the bandwidth limitations of the CMOS camera (Thorlabs, DCC1645C) using USB 2.0.

In general, three main factors affect the processing time. The first factor is the physical movement of the stage. The microscope stages from SmarAct used in this work can achieve a velocity of 8 mm per second in open-loop mode. For this work, the velocity was set to 2 mm per second, the standard velocity for closed-loop scanning. The second factor is the time it takes to capture and store an image on a computer. When building the scanning state machine (scanning algorithm) for this work, the main emphasis was on ensuring stability, especially during long tasks. Consequently, sub-second delays were introduced between individual states to ensure each step is fully complete and to avoid potential software crashes. During the scanning process, images are stored on a local hard drive rather than in RAM to prevent overflow.

The third factor is the state change in the scanning state machine, i.e., the delays associated with the computer moving the stage and then capturing and storing the image on a drive. The camera used for image acquisition, the Thorlabs DCC1645C USB 2.0 CMOS Camera, takes significantly longer to save 1.3-megapixel resolution images compared to higher-speed USB 3.0 cameras. Replacing the camera would therefore significantly impact acquisition and processing times.

The individual images are then processed using a Matlab script, which crops and stitches them into a collage. The image stitching time typically takes a few seconds to a few minutes depending on the number of images. The entire process rarely produces errors during scanning, allowing the system to operate unattended overnight.

To ensure accurate image scanning, the image formed on the CMOS camera must align with the scanning direction to avoid any rotational offsets, as shown in Figure 3.2. Before scanning printed devices, the system is characterized using a reference

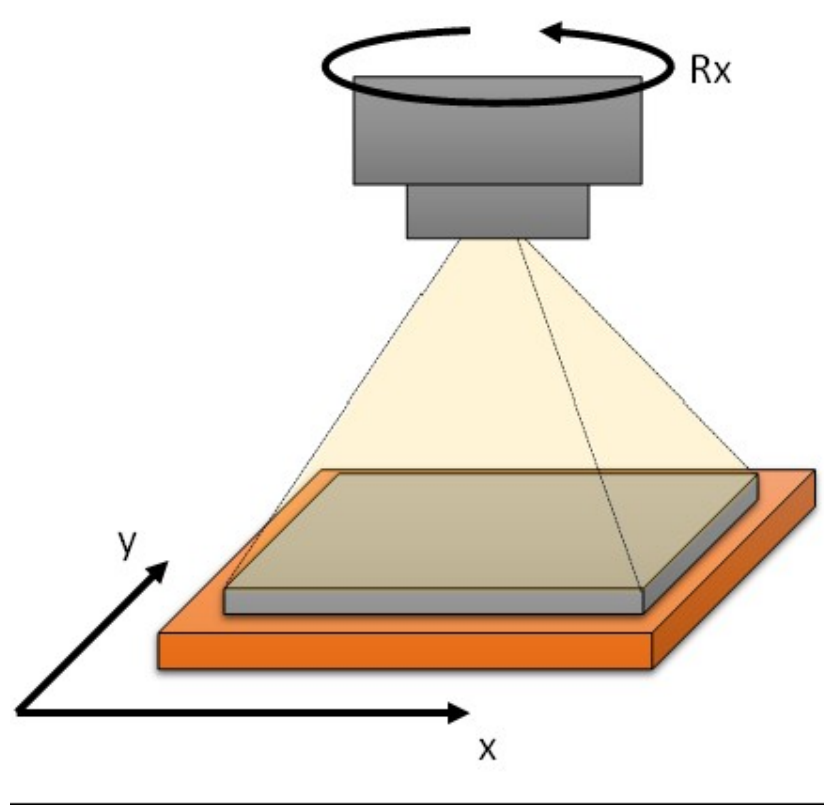


Figure 3.2: Schematic representation of the rotational alignment of the camera with the sample for adjustment

sample to confirm suitable stitching accuracy. Consequently, after each alignment, the system should be benchmarked to verify its stitching accuracy. The way that this was done was again by using the image processing method that is shown in the next section. Finally, some backlashes were occasionally noticed, though the source has not yet been identified. However, during the analysis stage, the errors produced by these backlashes are averaged out, so the overall accuracy of the proposed analysis method is not significantly affected.

To illustrate, Figure 3.3 presents a complete effective field-of-view image of a micro-LED Quarter Video Graphics Array (QVGA), along with a zoomed-in view of stitched sub-fields. The resulting calibrated image acts as input for the developed image processing method that is described in the next subsection, facilitating the comprehensive characterization of the entire chip.

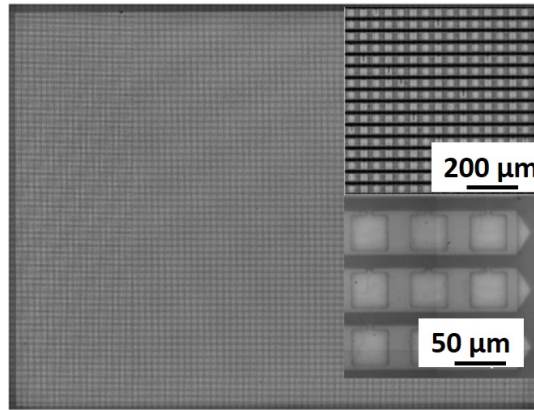


Figure 3.3: Quarter VGA micro-LED device (320x240 elements) with a close up snapshot of the stitched elements

3.1.2 Automated image processing analysis and characterization

The automated system was devised to assess both the yield of the transfer process, focusing on identifying missing membrane devices in a printed array, and the relative positional accuracy of the print. This involves evaluating the device-to-device pitch in comparison to the as-fabricated array. The image analysis was executed using Matlab and relied on standard tools within the image processing and statistical pattern recognition toolboxes [140], [141]. This section will present the results of several images during the code development process. After assessing the strengths and challenges of each method, the final code will be introduced.

The initial investigations commenced with an image featuring 12 dot-shaped objects of silver microparticles paste of varying diameter sizes, between 100-200 μm . At this stage, the focus was on image processing to identify the number of objects and the central position of each one. A fundamental image processing approach was employed, beginning with the conversion of the 3-color image to grayscale, followed by binarization. Binarization involves transforming data features into binary numbers to enhance the efficiency of classifier algorithms and is commonly utilized in image processing [142]. In this context, the threshold for binarization was automatically adapted and defined based on the dynamic range of the raw image. After the binarization process, the complementary of the image is taken, in order to convert the black regions to white and

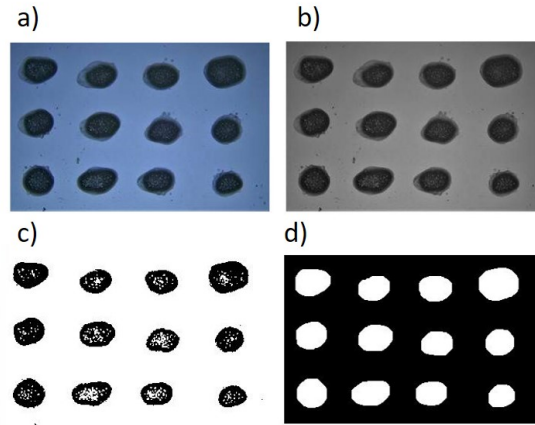


Figure 3.4: Basic initial image processing. a) Initial image, b) conversion to gray scale, c) binarized format and d) complementary image

vice-versa. That will help in identification of the objects in the following steps. The initial image as well as the different processing steps of the same image are presented in Figure 3.4 a)-d), respectively. For convenience, from now on, all the complementary images are been referred as binarized. Additional tests were conducted by analyzing the image using different RGB filters, performing individual binarization for each filter, and summing the results as Figure 3.5 illustrates. However, no significant difference was observed in the outcomes. The same results processing was implemented to an image including square shaped devices presented in Figure 3.6 a), which match the shape of the pixels. As a proof that the same process can be carried out with any shape, the resulted binarized image can be seen in Figure 3.6 b).

Moving forward, the subsequent stage involves pinpointing the centers of each square. At this point, a built-in Matlab function was employed, which essentially identifies all the white objects in the image as points of interest. The function then determines the center of the resulting white object based on its shape after binarization. While this method offers a quick and rough inspection, its accuracy is notably low. The limitation arises from the strong dependence on the quality of the resulting binarized image. In situations where there is low contrast in the image, the binarization may not be adequate, leading to limited accuracy in detection. Figure 3.7 provides an example of this issue, illustrating how the central location can be misinterpreted due

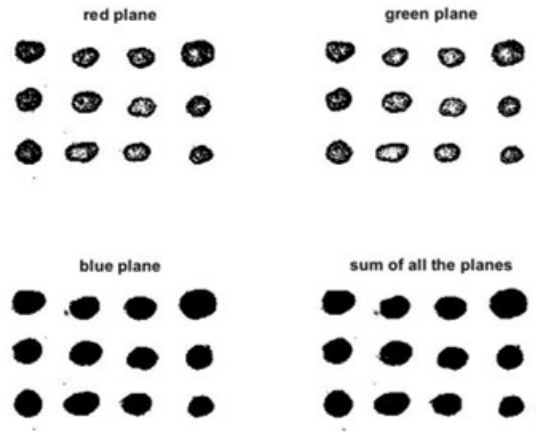


Figure 3.5: Binarization of the each filter of the image and the final summation for all the filters

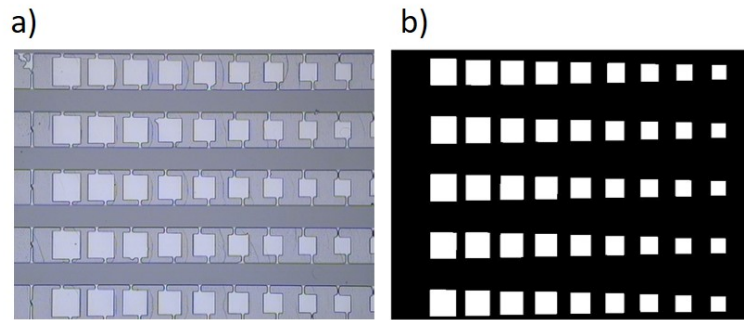


Figure 3.6: Example of the binarization of squares in different sizes. a) Initial image and b) Binarized image

to the constraints of binarization. While in this image, where the number of objects is low, it is easy to identify the error, in the case of inspecting images that contain hundreds of objects, the process becomes challenging.

For our specific case, where the accuracy of our method needs to be in the order of nanometers, this technique proves insufficient. The subsequent paragraph will introduce the cross-correlation method, accompanied by various examples used during the code development, showcasing improvements that can be implemented.

Before proceeding, additional image processing steps are necessary to enhance the accuracy of detection. Small objects and spatial defects were removed from the image using an inbuilt Matlab function called 'morphological opening' tool, which conducts a shape and scale-based thresholding operation. Essentially, what this tool does, is

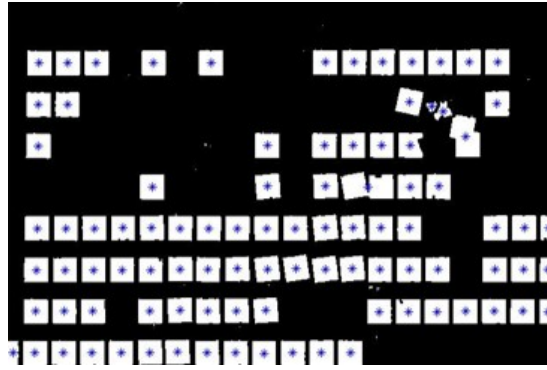


Figure 3.7: Example of a poor center detection due to the binarized , detecting two centers in one object (top right) and one center between two objects (middle right)

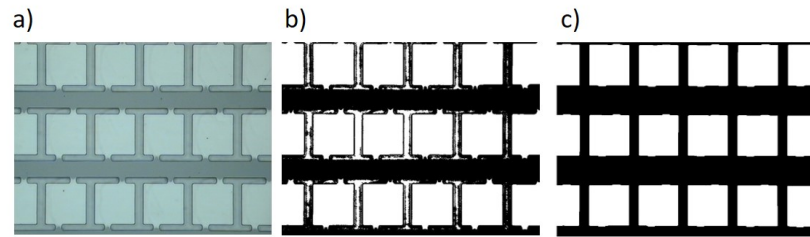


Figure 3.8: Example of different processing of the same image. a) initial image, (b) image after binarization and (c) image after morphological opening and object recognition processing

that uses a pre-defined pixel size shape and removes all the objects within the image that are less than that size. Subsequently, an object recognition tool was employed to identify approximately square objects within the image. An example of the differences between the initial image, after binarization and after morphological opening and object recognition processing can be seen in Figure 3.8 a), b) and c), respectively. For each identified device, a kernel convolution matrix was applied for edge detection. Edge detection involves various mathematical methods aiming to identify abrupt changes in brightness, or edges, in a digital image [143]. The matrix used for edge detection should be symmetric for optimal results, with its dimensions linked to the desired thickness of the detected edges. An example of applied edge detection method on squared objects can be seen in Figure 3.9a) for lower density array and Figure 3.9 b) for high density array. This step is crucial since, in some instances, the edges of devices post-binarization may appear non-continuous or have low contrast with the background image, making

it challenging to detect centers using conventional techniques.

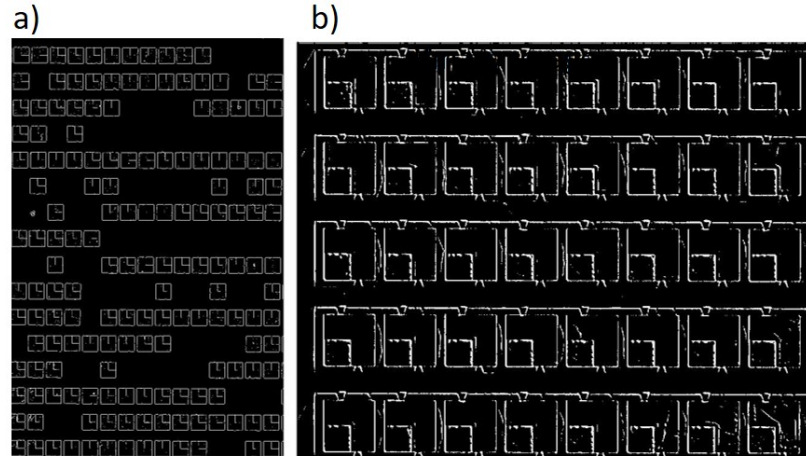


Figure 3.9: Example of edge detection on squares. a) Lower dense array and b) high dense array

The center points of the objects were then extracted through a cross-correlation operation with an idealized prototype of the membrane edge representation, within the range of $\pm 50 \mu m$ around the point of interest. This approach, similar to the one presented in [135], is particularly essential for accurate center detection, especially when the edges of devices exhibit non-continuous or low-contrast characteristics after binarization.

Cross correlation

Cross-correlation is a crucial mathematical technique in signal processing and image analysis, employed to qualify the similarity between two signals or datasets as they vary temporally or spatially [144]. Its primary utility lies in uncovering patterns, similarities, or relationships inherent in different signals. When applied to time-series data, the cross-correlation process entails sliding one signal, often termed the “reference” or “template” signal, across another, known as the “input” signal in delay space. At each point of overlap, the similarity between the two signals is calculated, generating what is known as the cross-correlation function [145]. This function provides insights into how well the reference signal aligns with the input signal at various time lags.

In the realm of image analysis, cross-correlation serves to compare two images by

systematically shifting one image (considered the template) over another (the source image) and evaluating the similarity between the pixel values at each spatial position [146]. This application proves valuable in diverse tasks, including object detection, template matching, and image registration [147]. Essentially, cross-correlation acts as a powerful tool for unveiling meaningful relationships and patterns in both temporal and spatial domains, contributing significantly to signal processing and image analysis methodologies. The formula for discrete cross-correlation of two signals x and y at a given lag k is:

$$[k] = \sum x[n]y[n + k] \quad (3.1)$$

Where:

- $x[n]$ is the value of the reference signal at time (or position) n .
- $y[n+k]$ is the value of the input signal at time (or position) $n+k$.
- k is the lag, which determines the time shift (or spatial shift in the case of images) between the two signals.

The resulting cross-correlation function provides information about how well the two signals match at each lag k . Peaks in the cross-correlation function indicate strong similarities between the two signals. Cross-correlation is widely used in various fields such as signal processing [148], image analysis [149], audio processing [150], and geophysics [151] for tasks like finding echoes in sonar signals, aligning images, tracking objects, and more.

One common application of cross-correlation in image processing is template matching [152], which is very similar to the one that it is used in this code. It refers to the process of having a smaller image (template) and trying to detect it within a larger image (source image). The goal is to find the region in the source image that best matches the template. At first, the template is translated (or moved) across the source image at different positions. At each discrete position displacement, the cross-correlation between the template and the corresponding region of the source image is calculated. At

each position, the cross-correlation value is computed by comparing the pixel values of the template and the corresponding region in the source image using the cross-correlation formula. The positions with highest cross-correlation values indicate better matches between the template and the source image. Peaks in the cross-correlation map indicate potential locations of the template within the source image.

Another application is image registration [153], which involves aligning two or more images of the same scene taken from different perspectives, at different times, or under different conditions. Cross-correlation can be used to determine the transformation that best aligns the images. This is particularly useful in medical imaging, remote sensing, and computer vision. In cases where images are only shifted (translated), cross-correlation can help find the translation that best aligns the images. The peak of the cross-correlation function corresponds to the translation that aligns the images. Cross-correlation can also be used to estimate more complex transformations, such as rotations, scaling, and shearing, by considering different transformations at each position of the template.

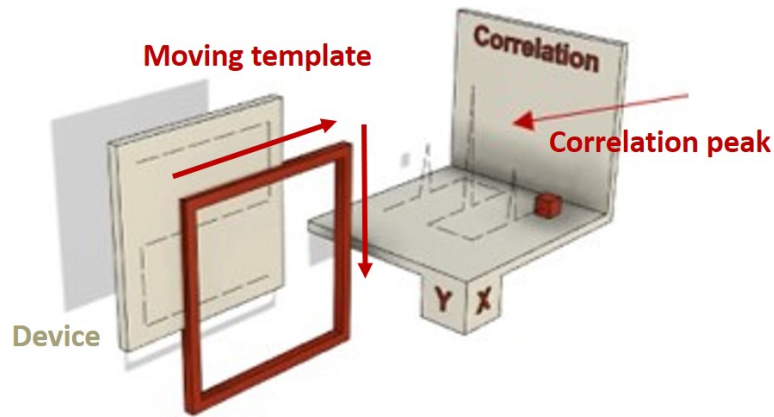


Figure 3.10: Representation of the cross correlation technique

This thesis employs a cross-correlation technique in its image processing method to detect the center location and rotation of membrane devices. The process necessitates a pre-defined template of the device geometry. This template is realized through the creation of a correlator, represented by an adequately sized matrix. This matrix mirrors the dimensions of the devices targeted for detection. The underlying concept involves

generating a digital rendition of the devices and cross-correlating it with the image, as illustrated in Figure 3.10. The matrix is structured with zero values except for the first and last row and column, where the values are set to 1, representing in this way the edges of the square-shaped template. The number of rows and columns with ones can be adjusted, and this adjustment is correlated with the thickness of the edges represented after the kernel convolution for edge detection. The result of this correlation is an $m \times n$ matrix, with m and n being the image resolution, encompassing various values indicative of the similarities between the image and the matrix. These values are normalized within the range of 0 to 1, with zero denoting non-similarities and one indicating identical matches. The highest values within this matrix correspond to the centers of the square-shaped devices, providing a robust method for precise detection in the context of device center localization and rotation assessment.

To identify devices or areas with abnormal orientations resulting from the printing process within the analyzed array, the previously discussed cross-correlation with angle detection was implemented. This involved rotating the correlator matrix within a range of ± 20 degrees at each scan position, with a step size of 1° . The outcome was the determination of the maximum correlation for each angle at specific pinpointed locations.

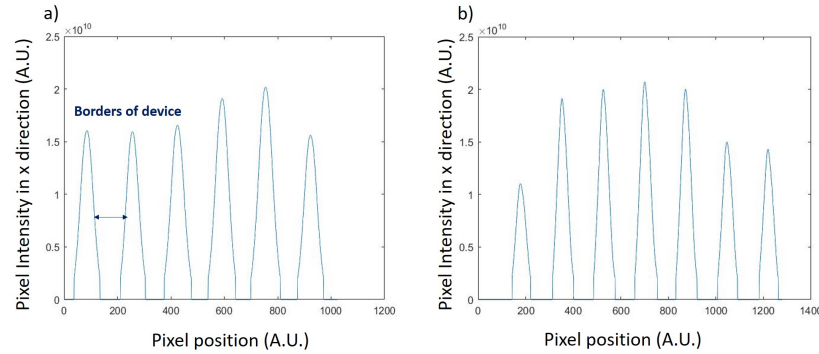


Figure 3.11: Correlation for an array of membrane devices, indicating the evenly distance between the devices that enables the clustering and the intensity values, with the peak of the graph being the maximum value of the correlation . a) in x-direction and b) in y-direction.

To find the angle at which the maximum correlation is achieved for each individual

device, a clustering approach was employed. This process automatically defined the borders of each object within the array. Various methods exist for clustering, and the one proposed here relies on a function that sums all the pixels in the x and y directions, respectively. When these results are plotted, the peaks in the corresponding graph indicate the intensity of the pixels, as it can be seen in Figure 3.11 a) and b) for the x and y direction, respectively. Utilizing a built-in MATLAB function to detect peaks and measure the distance between them allowed for the precise definition of the borders of each device. This approach is particularly effective because the devices are evenly spaced apart on the chip, as illustrated in Figure 3.11, which displays the resulting graphs. This clustering method ensures that the process has been accurately executed for all the examples used, while detecting the maximum correlation for all the angles and providing a robust means of detecting abnormal orientations in devices within the analyzed array induced by the printing process.

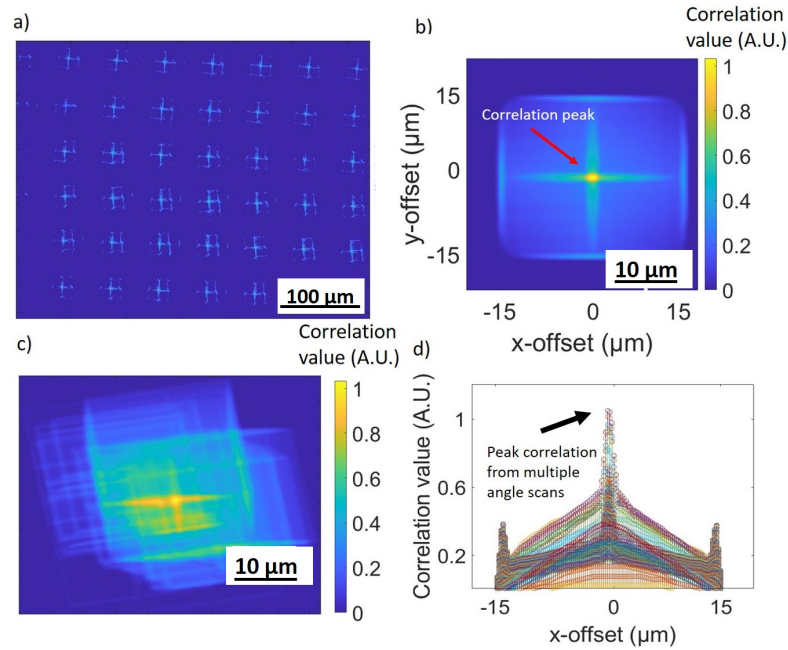


Figure 3.12: Correlation graphs. a) Pixel intensity reconstructive array of devices, b) close up of a reconstructed device (translation), c) close up of a reconstructed device for multiple angles (rotation) and d) Cross correlation curves as a function of angles

In Figure 3.12 a), a reconstruction of the imaged array post-correlation is presented, accompanied by a close-up view of a device for two different cases, as shown in Figures

3.12 b) and c), illustrating translation and rotation assessments, respectively. The yellow color in both figures represents the highest correlation value, indicating the point where the template perfectly aligns with the devices. This enables the accurate determination of the central position of large arrays of devices, overcoming the limitations associated with edge detection. The peak of the local cross-correlation corresponds to the extracted device center point within the camera pixel resolution. The angular rotation of the object is calculated in a similar fashion where the cross-correlation is calculated as a function of the relative rotation of the prototype object within the range of ± 10 degrees of rotation. Figure 3.12d) shows calculated cross-correlation curves as a function of angle, the maximum of the central peaks.

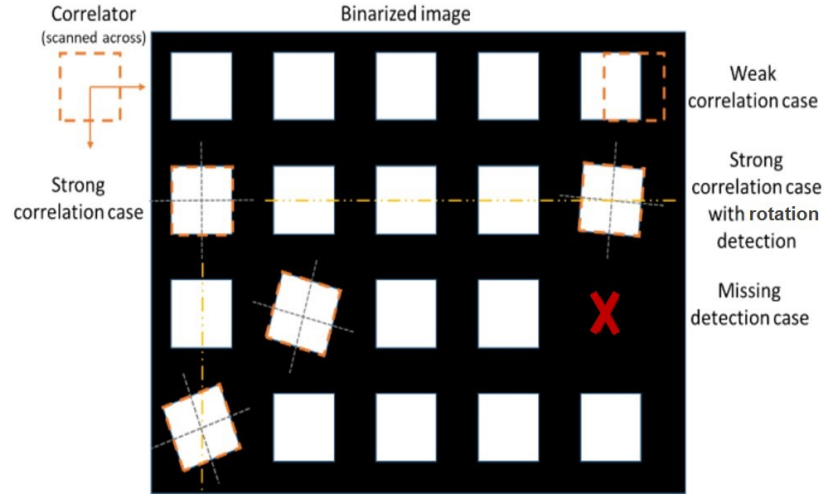


Figure 3.13: Schematic representation of the cross correlation

Figure 3.13 provides a comprehensive summary of the different cases encountered after the correlation process. In instances where the correlator precisely matches the device, termed a strong correlation case, the highest accuracy in detection is achieved. Conversely, in weak correlation cases where some similarities are detected but not the exact origin pattern of the correlator, the results are obtained by taking the maximum correlation, thereby ignoring less significant values. In cases where there is no commonality between the correlator and the image, the script recognizes this as a missing detection case. Leveraging the consistency of the array, this also allows for an assessment of the printing process yield by identifying potential devices that may not have

been successfully printed. Furthermore, the use of the rotated correlated matrix enables the detection of strong correlation for tilted devices, corresponding to the appropriate angle of rotation. This versatile approach adds robustness to the assessment, allowing for a comprehensive analysis of translation, rotation, and printing yield in large arrays of devices.

The metrology system compiles a list of spatial positions corresponding to each recognized device and their local rotation, and the total number of missing devices. Yield is simply calculated from the missing device numbers, and can be calculated for sub-sections of the full array using the extracted local spatial coordinates. The measured pitch values between each device and its 4 adjacent neighbors are calculated using a loop which corrects for any missing devices. The final results of the analysis are used to produce statistical distributions of center-to-center pitch values, rotation angles and number of missing pixels, all of which can be assessed over local or global areas.

3.2 Analysis of the photolithographically patterned devices

We applied our methodology to an as-fabricated chip before initiating any printing processes for validation. To facilitate comparison, we present two examples of our analysis: one utilizing a conventional microscope camera and another using the dynamic microscopy system previously described. In the former case, we successfully imaged an array of 6×6 devices at a resolution of $0.625 \mu\text{m}/\text{pixel}$, as can be seen in Figure 3.14a). Meanwhile, in the latter case, we achieved imaging of an entire QVGA device with an impressive resolution of $0.094 \mu\text{m}/\text{pixel}$, as presented in Figure 3.14b).

The initial evaluation of the automated analysis method involved examining a QVGA format pixel donor chip, which served as the reference sample. This chip's geometric characteristics were extracted and directly compared with the intended square array pitch specified in the photolithography mask design. In Figure 3.15, the initial image of the QVGA patterned devices on a silicon substrate is presented.

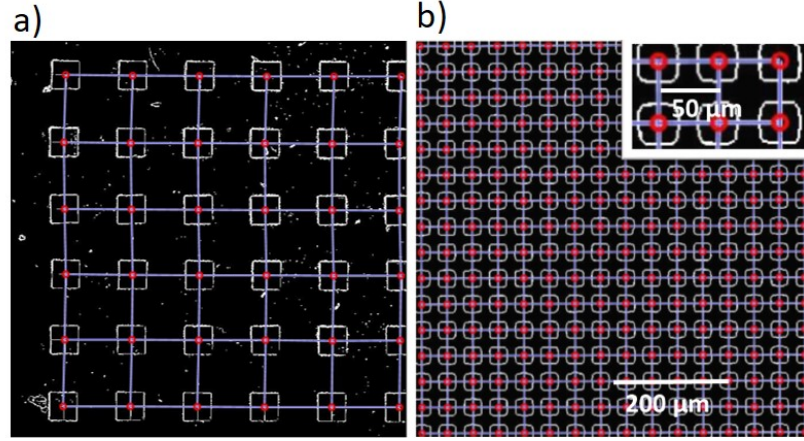


Figure 3.14: Center detection and pitch values. a) micro-LED by conventional microscope and b) sub-section of QVGA imaged array by dynamic microscopy system

To explore the method’s limitations, we opted for the highest magnification objective available in our microscopy system—a 50X infinity corrected lens, providing a pixel resolution of 94 nm/pixel at the camera image plane. To optimize scanning time, a sub-section of the array containing 900 devices was chosen for analysis. The histogram in Figure 3.16 illustrates the errors in the extracted pitch values, where pitch error is defined as the deviation between the extracted pitch value of neighboring devices and the as-designed value. Given that the device pitch is identical in both the x and y directions, the pitch between nearest neighbors in both dimensions is reported in a unified dataset. It is important to note that, in this case, no trend of x versus y direction was observed.

For the measured devices in this set, the mean pitch error is $\pm 120\text{ nm}$, with a standard deviation of 830 nm , according to the results from Figure 3.16. The mean value reference to the offset of the centre of Gaussian distribution from 0. Notably, this value closely aligns with the pixel resolution of the imaging system. However, the standard deviation is almost an order of magnitude larger than the pixel resolution. It is important to note that the device positional accuracy should theoretically be defined by the lithographic precision of the fabrication process. Therefore, the 830 nm standard deviation serves as a conservative estimate for the accuracy of the measurement technique. Additionally, our analysis did not detect any measurable rotation of devices

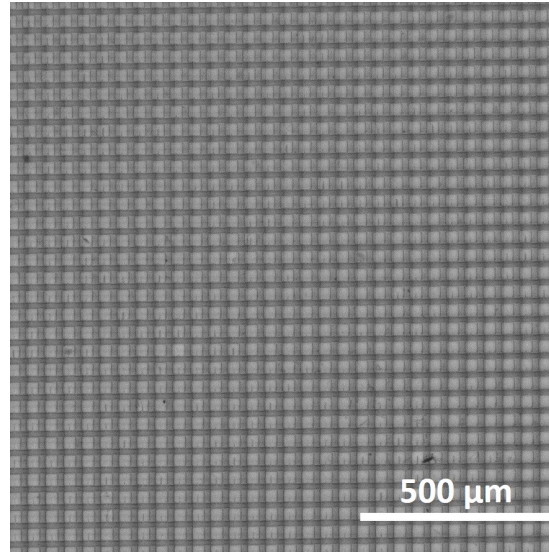


Figure 3.15: Subsection of the stitched image of the QVGA donor by using 50X magnification

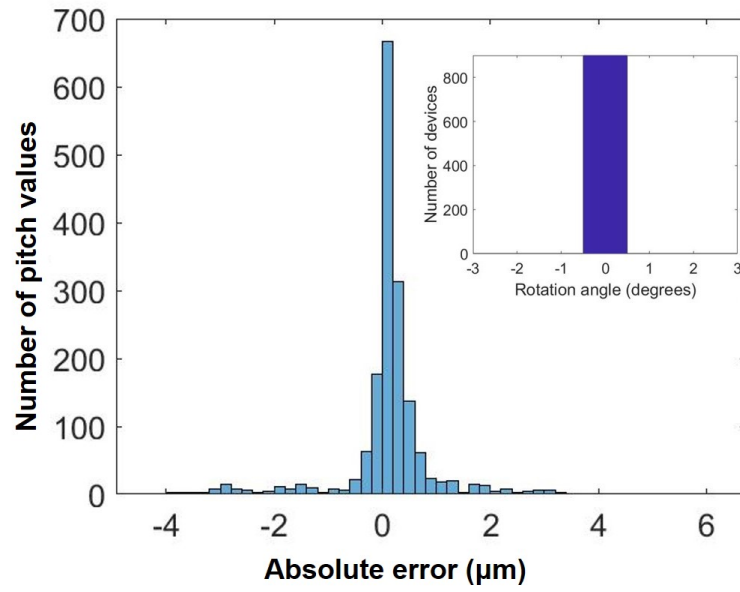


Figure 3.16: Extracted histogram in both x and y directions of the relative pitch error in the as-fabricated pixel array donor chip (Inset: histogram of the extracted pixel rotation error)

from their nominally ideal position, with the automated scan achieving a resolution of 1° .

3.3 Analysis of continuous roll-transfer printed devices

An analysis of the roll-transfer printed chips was carried out. The devices analyzed here consists of an array of suspended mini and micro-LED transfer printed over a polymer coated flexible receiver substrate. The roll-transfer printing method that was described in Chapter 2 was used for the transfer printing of both mini-LED devices and QVGA devices. In the first subsection, the analysis of the printing of a low quality fabricated chip is presented for yield assessment purposes, following by the analysis of roll-printed mini and micro-LED arrays.

3.3.1 Low quality fabricated chip for yield assesment

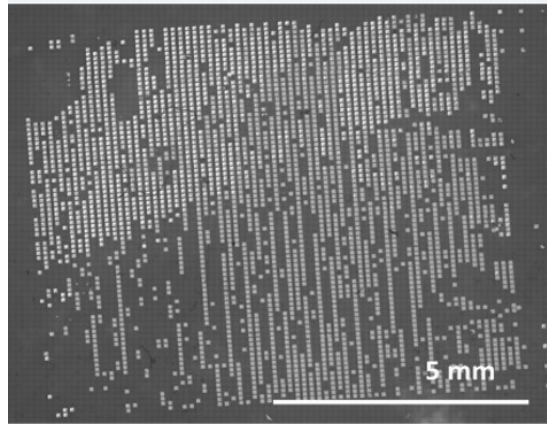


Figure 3.17: Full array of the printed devices (order of cm)

To verify the accuracy of our yield assessment, we conducted a test print using a donor chip deliberately engineered to have a significant number of defects, resulting in a low yield print outcome. In Figure 3.17, the full mini-LED array of the printed devices which consist of 4,000 devices and it is in the order of cm is presented, while in Figure 3.18, a portion of the processed microscopy image is displayed. The vacant grid sites, indicative of defects, are clearly discernible in the processed image and are marked with an 'x' at the expected location of the pixel center. It is essential to note that the extracted pixel pitch values (depicted by blue lines) are specifically defined between nearest neighbor pixels. This approach, as designed, eliminates distances that may

encompass missing device elements. The successfully transferred pixels are identified by red circles, representing their extracted center positions in the image.

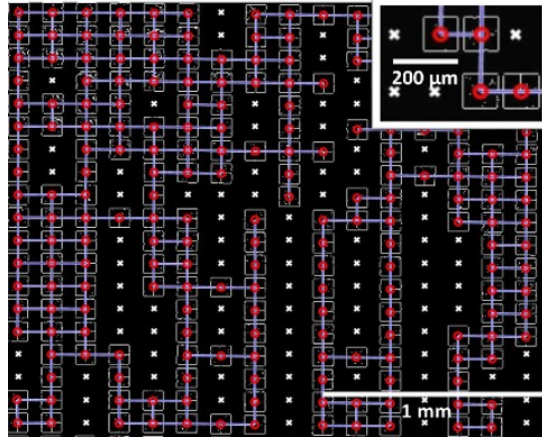


Figure 3.18: Full array of the printed devices (order of *cm*)

In a manner similar to the previous scenario, we conducted a comparative analysis of pitch values against the design specifications, assessing positional grid errors in both Δx and Δy dimensions. Across the x direction, a mean value of $-0.69 \mu m$ with a standard deviation of $0.69 \mu m$ is presented, while in the y direction, a mean value of $2.60 \mu m$ with a standard deviation of $1.62 \mu m$ is calculated. Graphs in Figure 3.19 depicting Gaussian fits of these values illustrate a noteworthy observation: a broader error distribution in Δy , attributed to the specific chip transfer method employed. This observation provides useful information about the mechanics and precision of the transfer method. Specifically, it highlights a problem or a characteristic of the printing method and the equipment setup used in the experiment. The roller, which is supposed to transfer the chips precisely, is not perfectly aligned in the y direction. This misalignment can cause the chips to be placed inaccurately along that axis. Because of this misalignment, the chips might be shifted more than expected in the y direction, leading to a broader error distribution. This means that the placement of chips varies more widely in this direction compared to a well-aligned system. Recognizing this issue can lead to adjustments in the setup, such as re-calibrating the roller alignment or refining the transfer method to reduce the error. Understanding the source of the error helps in improving the precision and accuracy of the chip transfer process, which is

critical in high-precision manufacturing

Furthermore, we observe larger mean deviation values compared to the as-fabricated chip, indicative of printing effects. Our measurement technique operates at a scale that allows for the quantification of these deviations. Additionally, through a count of missing devices on the chip, we assess the process yield, revealing an 80 % success rate in this particular case.

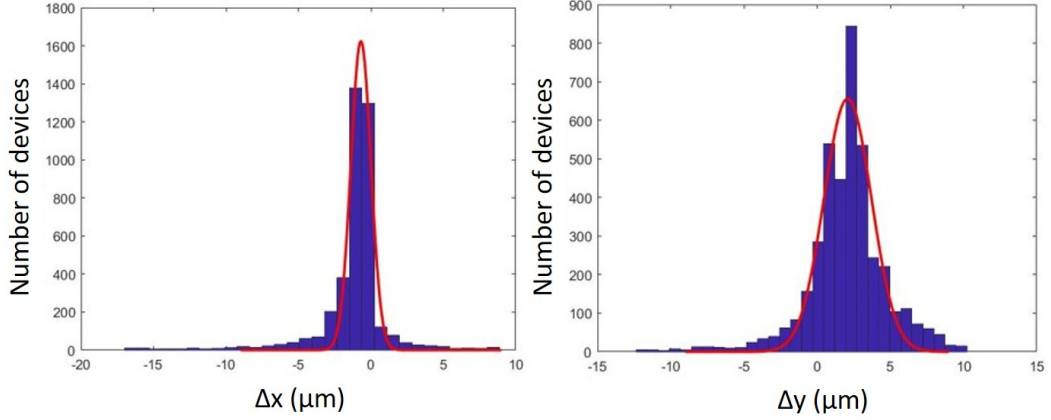


Figure 3.19: Histogram of the error Δx and Δy , respectively with Gaussian fitting

3.3.2 Mini-LEDs

Figure 3.20a), we present the initial image of a segment containing roll-printed mini-LEDs. Subsequently, in Figure 3.20b), the results of cross-correlation are displayed within a cropped area, revealing detected device centers marked with red dots and their corresponding center-to-center distances.

Similar to non-printed devices, errors or defects arising from the transfer printing process are computed by comparing the results with the GDSII file of the mask utilized in the lithography process. The GDSII file provides a known distance between consecutive devices, which, in this case, is $170 \mu m$ in the x-direction and $120 \mu m$ in the y-direction. The error distribution of pitch values, calculated from the script, and the assessed distribution of device rotation are depicted in Figure 3.21a) and b), respectively.

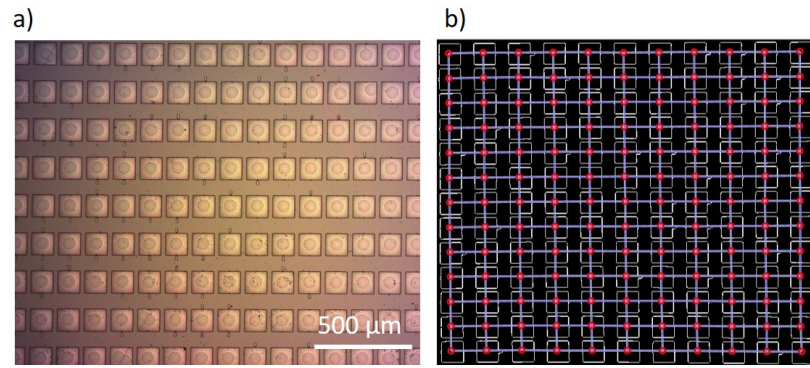


Figure 3.20: Roll-transfer printed mini-LEDs a) microscope image and b) snapshot of the analyzed image

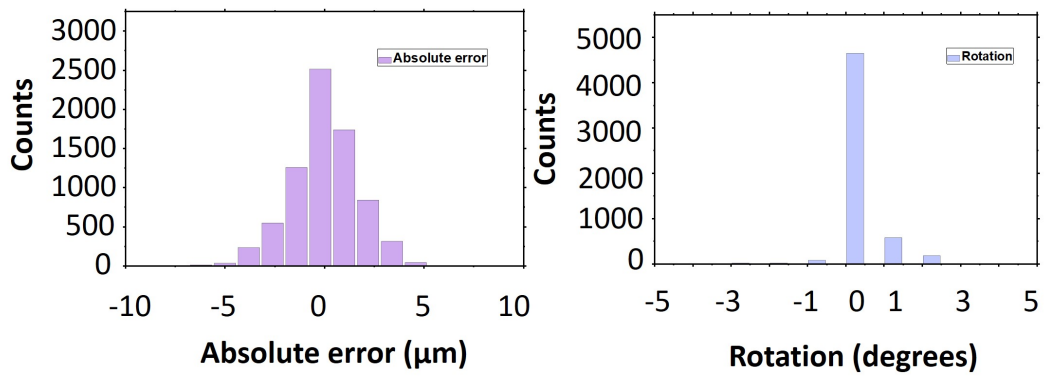


Figure 3.21: Statistical analysis of roll-transfer printed mini-LED array

A comprehensive analysis of the printed array was conducted using the automated metrology tool, yielding a transfer success rate of 95 %.

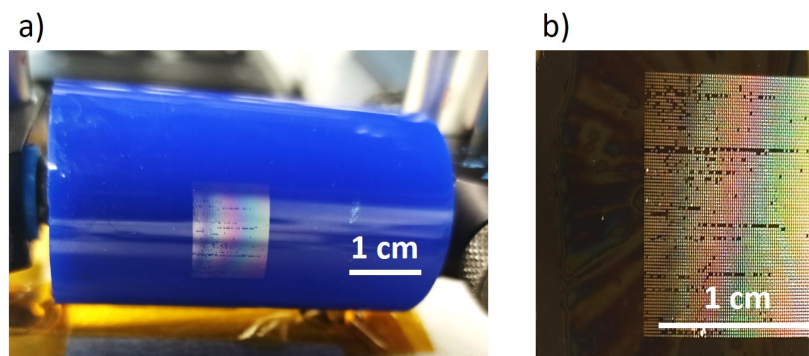


Figure 3.22: Roll-transfer printed chip with mini-LEDs

The full roll-transfer printed chip picked from the donor chip, as well as the printed

mini-LED pixels are presented in Figure 3.22a) and b), respectively. The inter-pixel pitch in both the x and y directions was extracted, with a measurement resolution limit of 720 nm . Across the full pixel array a mean pixel pitch error of 26 nm is found, with a standard deviation of $1.43\text{ }\mu\text{m}$ [154].

3.3.3 Quarter Video Graphics Array

The continuous roll printing process was then carried out on a full QVGA pixel array. Figure 3.23 a) shows the pixel array after pick-up by the roller print head, during the continuous roller transfer stage. Figure 3.23 b) and c) respectively show optical microscope and SEM images of a sub-section of the printed array.

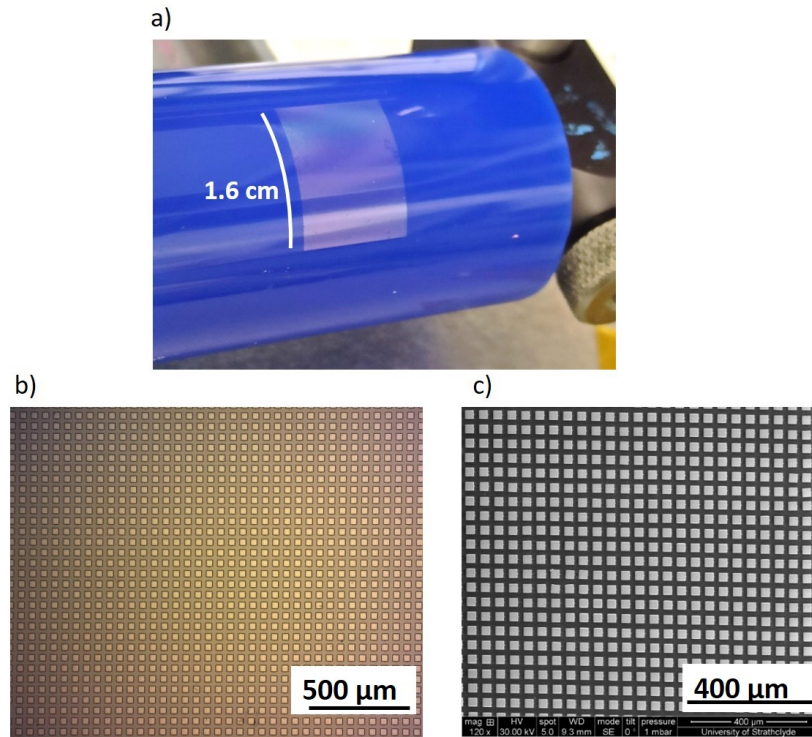


Figure 3.23: a) Image of the roller print head mid-way through the process with the QVGA pixel array visible on the surface. b) Optical microscope and c) SEM images of sub-sections of the transfer printed pixel array

A sub-section of the full printed array was imaged using the 50X objective scanning optical microscopy system, and processed with the automated metrology system. As before, the pixel pitch values are reported as an error value from the designed value

of $50\ \mu\text{m}$ in both x and y dimensions, as shown in Figure 3.24a) and b). This high resolution sub array produced mean offset and standard deviation values of 120 and 730 nm, respectively, for the full dataset. As these values are of the same order of magnitude as the measured values from the as-fabricated device we can be confident they represent the effects of the printing process and are not measurement limited.

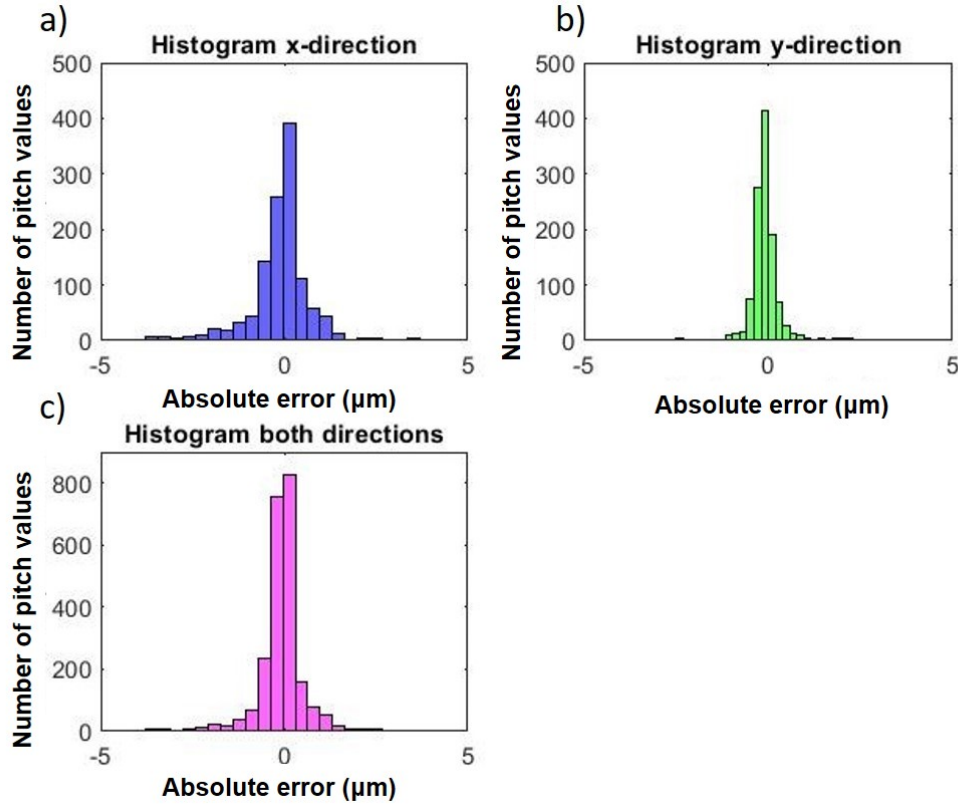


Figure 3.24: Extracted histograms of the relative pitch error in a sub-section of the printed pixel array receiver chip, using a 50X optical microscope objective. Histograms for (a) x and (b) y directions are presented individually and (c) as a combined data set

The scanning microscopy was then carried out over the full array using a 10X magnification objective lens to reduce throughput time. The 10X objective setup has a spatial resolution of $720\ \text{nm}/\text{pixel}$ at the image plane. The full QVGA area of $12 \times 15\text{mm}^2$ takes 160 minutes with the 10X objective and 1800 minutes with the 50X objective. The scanning time of the system is limited by the current implementation of the electronic interfacing between the camera, stage controller and computer. By

optimizing the data connection rates and removing communications latencies the scan time could be improved by around two orders of magnitude. Figure 3.25 shows the histogram of extracted pitch error across both x and y dimensions. The mean pixel pitch error is 430 nm , with a standard deviation of 980 nm . These figures are comparable with the high-resolution sub-section measurements. The distribution of pitch error across the array as a function of spatial location was assessed and did not demonstrate any local trends, giving confidence in the uniformity of the process over relatively large areas. The analysis of pixel rotation showed negligible rotation effects to within the 1° accuracy of the method.

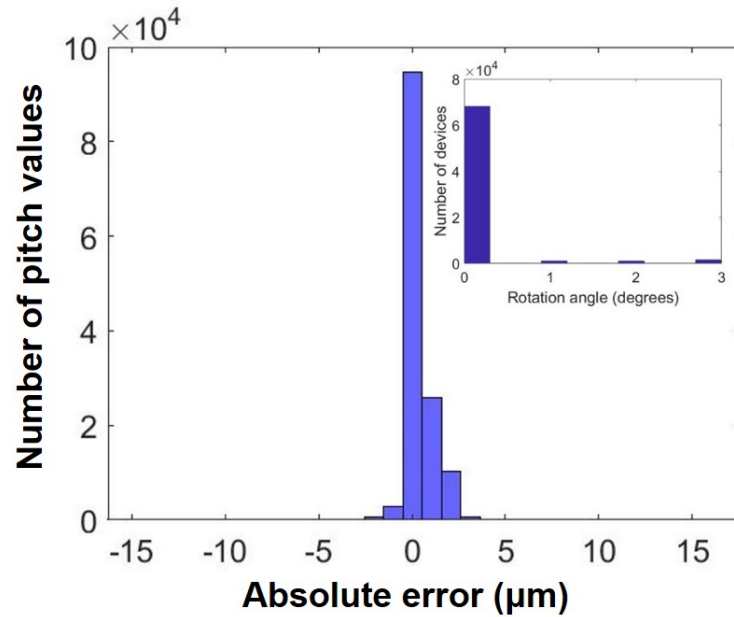


Figure 3.25: Histogram of pitch offset error for the full roller transfer printed QVGA pixel array (Inset: histogram of the rotation).

By calculating the ratio of the missing devices over the centres of the devices and the missing devices, the transfer yield can be determined. The absolute yield of the array printing process was 98%, however, the defects were spatially localized within two small areas with yields of $\sim 80\%$. As mentioned previously, a significant advantage of our method is that the position, rotation and yield results are associated with coordinate locations in the grid, allowing for spatially resolved analysis of the results. Figure 3.26a) shows a heat map of the calculated transfer yield for the whole chip divided into

10×10 local sub-areas, each of these representing 32×24 devices in column and row, respectively, on a color scale.

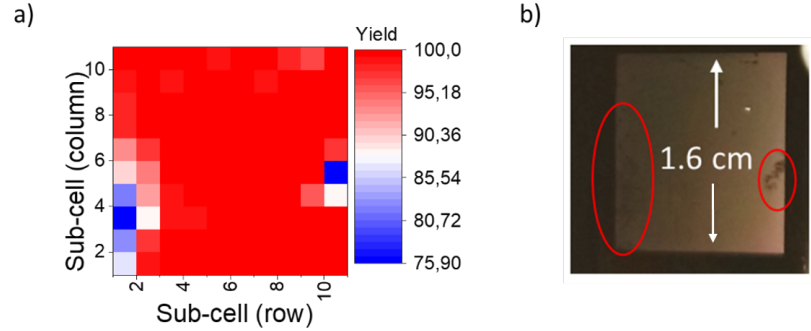


Figure 3.26: a) Local area process yield map. b) Photograph of the printed device array, highlighting areas of local yield issues corresponding to (a).

Two clear areas of low process yield are apparent in this analysis, while the majority of the chip approaches unity yield. Figure 3.26 b) shows a large FOV image of the printed array where the local, low yield areas of the array are obvious, highlighted by the red bounding ellipses. The donor chip for this process was re-assessed using optical microscopy after the printing stage to correlate defects in the printed array with the remaining donor pixel sites. The areas of low yield on the receiver corresponded to areas on the donor where the pixels had not been released and were still in-place. Inspection showed that these pixels were not fully-fabricated as membranes, potentially due to their proximity to the chip edges causing issues with a lithography step, as mentioned in Chapter 2. The same explanation of the localized low yield is applied to miniLEDs as well. Attempts to print these membranes from both chips using a standard planar single device transfer printing method [155] were unsuccessful highlighting the failure of membrane release. Figure 3.27 shows parts of the fabricated donor prior to any printing processes, illustrating the small areas in the donor where the fabrication yield was low. In Figure 3.27a) the black lines in the middle of the device shows clearly that this area in the device is not fully underetched, thus it cannot be releasable during the transfer printing process, while Figure 3.27b) presents a line of devices that have been removed from the donor, matching the lines missing from the printed arrays. By using the same analysis code in the remaining devices in the donor, the number and position

of the non printed devices can be determined.

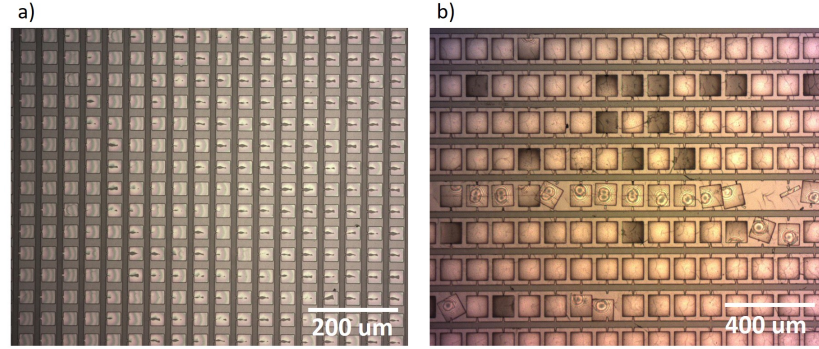


Figure 3.27: Parts of the fabricated donors with low fabrication yield before the printing process. a) QVGA donor showing devices that are not fully underetched and b) miniLEDs donor showing missing and detached devices from the chip

The areas of lower yield are therefore attributed to donor processing issues, rather than the printing process itself, resulting to a roll-transfer printing yield of more than 99.9%.. [156].

3.4 Chapter summary

In this chapter, the development of a new automated sub-micron inspection method was introduced in order to evaluate continuous roll-transfer printing method in terms of positional accuracy, rotation and yield. This method was used for both the analysis of an as-fabricated donor chip for validation and the resultant roll printed arrays. The as-fabricated chip analysis showed a measurement limited performance, with a standard deviation of the pixel pitch error of 830 nm . The roll-printed mini-LEDs array with 4000 pixels in total showed a mean pitch error of 26 nm and a standard deviation of $1.43\text{ }\mu\text{m}$, while the fully transferred QVGA array of $>75,000$ devices presented a mean pitch error of 430 nm and a standard deviation of 980 nm . The full array yield of 95% and 98% for miniLEDs and microLEDs respectively, was shown to be spatially dependent with the majority of the chip area yield $>99.9\%$ and defects dominated by small areas where the donor chip processing had failed. This work shows the potential for hybrid materials device integration at scale, compatible with the well-established infrastructure

Chapter 3. Automated inspection method for large array devices and analysis
and semiconductor processes developed in industrial foundry manufacturing.

Chapter 4

Mechanical deformation of thin film silicon

In this chapter, a simple method for inducing and permanently maintaining strain in silicon through physical mechanical bending is presented. By subjecting the silicon substrate to a controlled bending process, the generation of strain levels that persist even after the removal of external stress is demonstrated. This opens up new avenues for enhancing the performance of silicon devices without resorting to complex and expensive fabrication techniques. A comprehensive study of the mechanics behind the phenomenon is presented, along with a detailed characterisation of the strain induced. These findings showcase the potential of this approach in improving strain engineering and fostering the development of high-performance silicon-based technologies.

4.1 Introduction

4.1.1 Heterogeneous integration for strain engineering on Silicon

One significant aspect of heterogeneous integration is the use of strained silicon, which has shown remarkable potential for enhancing the performance of electronic devices, particularly metal-oxide-semiconductor field-effect transistors (MOSFETs). Strained silicon-on-insulator (SSOI) substrates have been developed to leverage the benefits of strained silicon and silicon-on-insulator technologies, combining the properties of both

materials [157]. The incorporation of strained silicon technology has led to impressive improvements in the performance of MOSFETs over the past decade [158]. The piezoresistive effect in biaxially strained silicon has been studied, demonstrating the engineering of piezoresistivity in strained silicon, which is crucial for understanding the behavior of strained silicon under mechanical stress [159]. Furthermore, the stability of strain in nanoscale patterned strained silicon-on-insulator has been investigated, highlighting the potential for integrating strained silicon into nanoscale devices. These findings underscore the significance of strained silicon in heterogeneous integration, particularly in enhancing the performance of electronic devices and enabling the development of advanced materials and systems.

4.1.2 Changes in the atomic structure of silicon

Changes in atomic arrangement in strained silicon can lead to changes in electronic band structure. The effect of elastic strain on changing electronic properties has been demonstrated through low-temperature measurements of the longitudinal Hall effect in strained silicon quantum wells before and after emission [160]. The strain change in the band structure can be explained by the overlap of atomic orbitals, which leads to the band change in the allowed energy levels [161]. Additionally, the effect of subband structure modification on the mobility of modern MOSFETs using strained ultrathin silicon films has been investigated, revealing the impact of strain on the electronic properties of silicon [162]. In addition, the possibility of improving device performance by modifying the band structure of silicon has been widely studied, highlighting the importance of modification technology in nanomaterials [163]. The presence of strain in silicon nanomaterials can control the bandgap size and change the properties of the bandgap indirectly or directly, demonstrating the significant impact of strain on the electronic properties of silicon [164]. Moreover, the strain effect is based on differences in reactivity depending on the atomic arrangement (including compressed or expanded arrangement) of the surface atoms, which further highlights the role of atomic arrangement in determining the electronic band structure [165]. A schematic of the induced changes on the crystal lattice by strain is presented in Figure 4.1. Strain also changes

the band structure of the semiconductor, indicating that strain has a direct effect on the electronic properties of silicon [166].

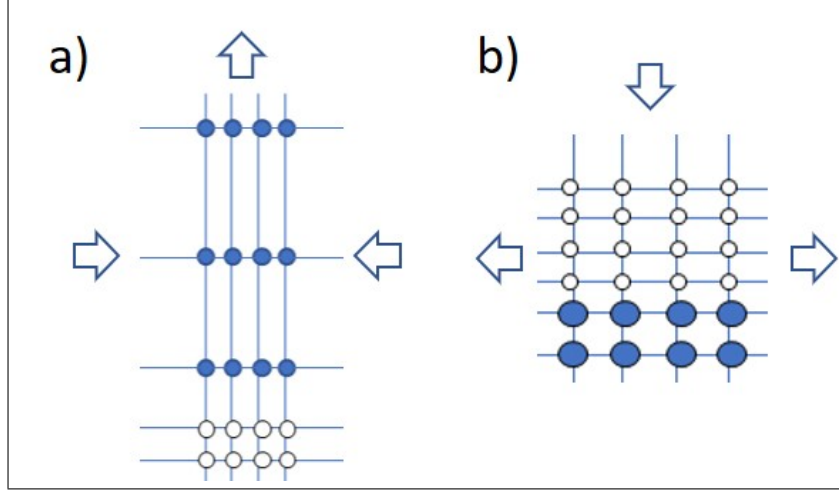


Figure 4.1: Schematic of layers under in-plane a) compressive and b) tensile strain

The generation of second-order nonlinear optical effects in silicon due to strain modification has become the subject of extensive research. It is theoretically believed that symmetry breaking due to deformation of crystalline silicon results in a large number of non-zero components of the second-order nonlinear sensitivity tensor $\chi(2)$ [167]. This is important because the presence of inversion symmetry in the Si crystal structure prevents the use of second-order optical nonlinearities, and the generation of strain gradients in Si by stressed materials can be considered a way to overcome this limitation [168]. Strained silicon waveguides have been proposed to break silicon centrosymmetry, suppressing second-order nonlinearities and producing second-order nonlinear optical effects [169]. Strain-induced second-order nonlinearities in silicon ($\chi(2)$ effect) have been investigated, and studies focusing on the induced Pockels effect have explored the possibility that strain induces large nonlinear optical effects through changes in wave function symmetry. [170], [171] Additionally, strain-induced band splitting and quantum confinement effects in ultra-thin silicon have been identified as bandgap engineering mechanisms that can produce second-order nonlinear optical effects [172]. Exploitation of strain-induced second-order nonlinear optical effects in silicon impacts silicon photonics by paving the way to exploit other second-order nonlinear processes

and alter the fundamental optical properties of the material. [173]

4.1.3 Silicon crystal lattice

The silicon crystal lattice is a three-dimensional arrangement of silicon atoms bonded together in a regular, repeating pattern. The lattice structure of silicon is a key factor that determines its electrical properties. In its unstrained state, silicon has a diamond faced center cubic (FCC) cubic crystal structure, with each silicon atom covalently bonded to four neighbouring silicon atoms. This regular arrangement of atoms gives silicon its crystalline structure and electrical properties. Each silicon atom forms covalent bonds with four neighboring silicon atoms, resulting in a tetrahedral structure. Figure 4.2 shows the lattice structure of silicon. This crystal lattice structure confers several advantages such as high thermal conductivity [174], structural stability [175], optical applications [176] and photonic-electronic integration potential [177]. However, one of the biggest limitations is that the centrosymmetric diamond lattice of silicon inhibits efficient second-order nonlinear optical processes, limiting its optical functionalities [178]. When silicon is subjected to strain, whether it is compressive or tensile, the lattice structure is modified. The strain changes the interatomic distances and bond angles, altering the arrangement of atoms within the crystal lattice. This modification of the lattice structure affects the electronic properties of silicon, particularly the mobility of charge carriers, making it a valuable tool for the development of advanced semiconductor devices

The amount of strain required to induce specific modifications depends on the desired effect. When considering strain-induced improvements in carrier mobility and transistor performance, moderate levels of strain in the range of 1% to 2% are often targeted. This range of strain can lead to significant enhancements in carrier mobility and thus improve the speed and efficiency of transistors [158]. On the other hand, when aiming to induce second-order harmonic properties or nonlinear optical effects in silicon, the strain levels required are typically lower. Strain levels ranging from 0.1% to 0.3% in tensile or compressive strain have been investigated for achieving efficient second-harmonic generation in strained silicon waveguides and nanostructures [180]. Achieving

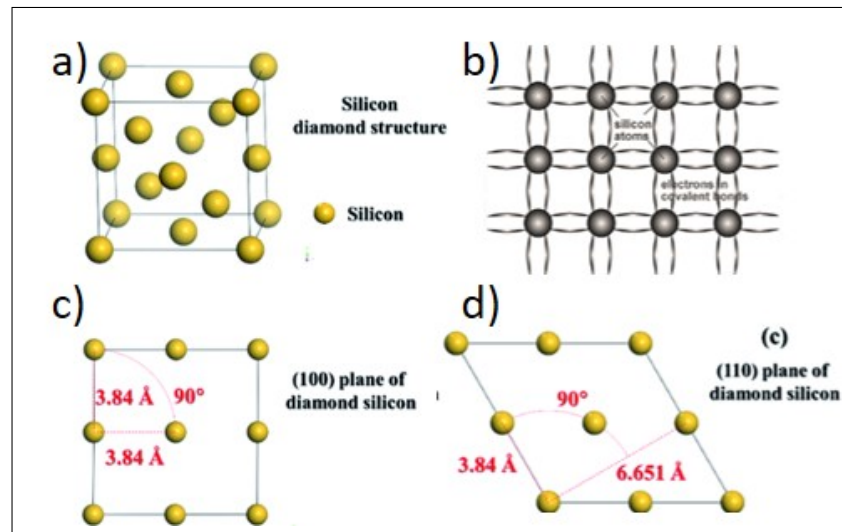


Figure 4.2: Silicon crystal lattice structure a) cubic silicon diamond structure, b) silicon atoms with covalent bonds, c) (100) plane and d) (110) plane of silicon [179]

and controlling strain in silicon can be a complex process, as strain can interact with various factors, such as the device geometry, the integration of strain-inducing layers or structures, and the overall device architecture.

The importance of strain engineering in semiconductor materials has increased in recent years [181] as the demand for faster, more efficient and high quality heterostructure electronic and photonic devices has grown [182]. Strain engineering can help to improve the performance of devices in a number of ways [183] [184] [185], including single photon emitters [186], increased carrier mobility [187] [188], enhanced transistor performance and improved device speed [189] [190], reduced parasitic capacitance [191], changes in the bandgap [192] [193], refractive index [194] and improved signal propagation [195]. The benefits of strain engineering, combined with its compatibility with existing manufacturing processes, make it a promising technology for improving the performance of devices [196].

Traditional methods of inducing strain involve complex and costly processes such as epitaxial growth in planar materials [197], ion implantation [198], exploiting the mismatch between hetero-epitaxial layers, as the silicon and germanium lattices [199] which impose limitations on device scalability and integration. Additionally, these strain induction methods often suffer from limited controllability and the tendency of strain

to relax over time, limiting their long-term effectiveness. More recently, semiconductor nanomembranes (NMs) have emerged as a promising materials platform for strain engineering [200]. This platform offers unique opportunities for strain manipulation, both through spontaneous elastic strain upon NM release, and through the application of external mechanical stress [201].

Here, a simple approach to induce and maintain strain in silicon is proposed by physically bending thin silicon membranes. The controllable bending of the thin film membranes is achieved by using simple topological features on the substrate and printing the membranes across these features, using micro-transfer printing method. To verify the results from the simulation, we transfer-printed two membranes across a micron-scale ridge with $h=1.15\ \mu m$ and $h=1.50\ \mu m$, respectively, and analysed them with electron backscatter diffraction (EBSD) measurements. All the electron backscatter measurements were occurred in collaboration with the Physics Department of University of Strathclyde. The silicon membranes have been fabricated by using standard nanofabrication techniques and transfer printed on ridges by using elastomeric transfer printing. The printed membrane conforms on top of the ridge, resulting in physical bending. This simple model can be directly compared with a full finite element mechanical model. Simple modelling of the induced stress in membranes can be achieved by treating the as cantilevers with fixed boundary conditions. By using experimental and theoretical analysis, a maximum normal and shear strain of 0.6% and 0.3% respectively was achieved, giving the potential for future silicon-based device designs, where strain engineering can be efficiently integrated into existing fabrication processes, paving the way for a new era of high-performance and energy-efficient electronic devices.

4.2 Device fabrication and transfer printing.

We performed experimentally two printed cases applying Si membranes to ridge features with height $1.15\ \mu m$ and $h=1.50\ \mu m$, respectively. The silicon membrane has been fabricated by using standard nanofabrication techniques and transfer printed on ridges by using elastomeric transfer printing. The printed membrane conforms on top of the ridge, resulting in physical bending.

4.2.1 Fabrication of thin-film silicon membranes.

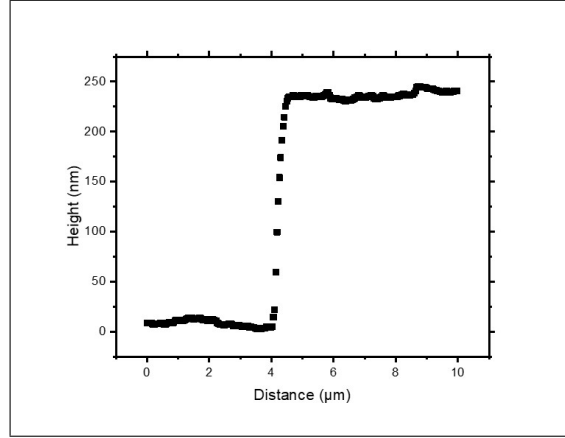


Figure 4.3: AFM measurement of the final thickness of the silicon membrane

A Silicon-on-Insulator (SOI) wafer was used with Silicon thickness $1.5 \mu\text{m}$ and buried oxide (BOX) $5 \mu\text{m}$. A blanket etch was performed on the top silicon layer by using reactive ion etching in order to define the desired thickness of the membrane (in this case, 220 nm thickness) as it can be seen in Figure 4.3. By using standard lithography and chemical etching processes, the square shape of the membranes was achieved resulting in $100 \times 100 \mu\text{m}^2$ size, as shown in Figure 4.4 (a). The process parameters used for etching Si and SiO_2 , as well as the exposure parameters for S1805, are the same mentioned in the fabrication steps in Chapter 2. In order to make the membranes releasable from their native substrate, an under-etching process is required for etching the Buried Oxide (BOX) underneath the Si membranes. In this work, acid etch was used by using 7:1 ratio Buffered Oxide Etch (BOE). BOE etches silicon dioxide isotropically with a theoretical rate of 80 nm/min . In order to protect the top side of the membranes from BOE attack, a photoresist mask was used. Studies have shown that BOE has the capability to selectively etch SiO_2 while maintaining the integrity of the photoresist mask [202]. The photoresist s1818 was spin coated on 3000rpm speed and 100 rpm/s acceleration for 60 seconds and was developed for 45 seconds with a 1:1 ratio developer-DI water. solution. The exposure parameters used for the laser lithography were 15 mW , 25 % filter, 35 % intensity and 30% focus. Figure 4.4 (b) shows the resulted array with the reflowed photoresist mask and Figure 4.4 (c)-(f) show the BOE

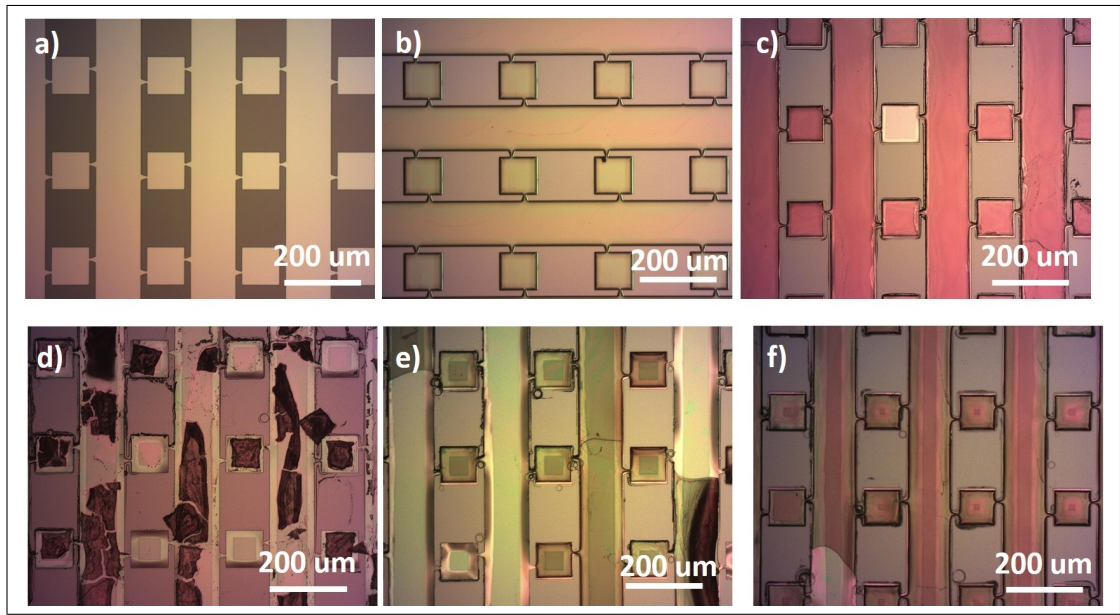


Figure 4.4: a) Fabricated array of silicon membranes before suspension and b) after applying photoresist mask and reflow, c) after 2 hours of BOE, d) after 4 hours, e) after 7 hours and f) after 10 hours

etching process at different time steps. It can be noticed that after 4 hours, the photoresist mask starts breaking and getting removed from the top of the devices. After the final fabrication step, the membranes are now suspended to facilitate the pick-up and place process. An example of the array of the suspended membranes with a close up of a suspended device can be seen in Figure 4.5 (a) and (b), respectively. [203], [204].

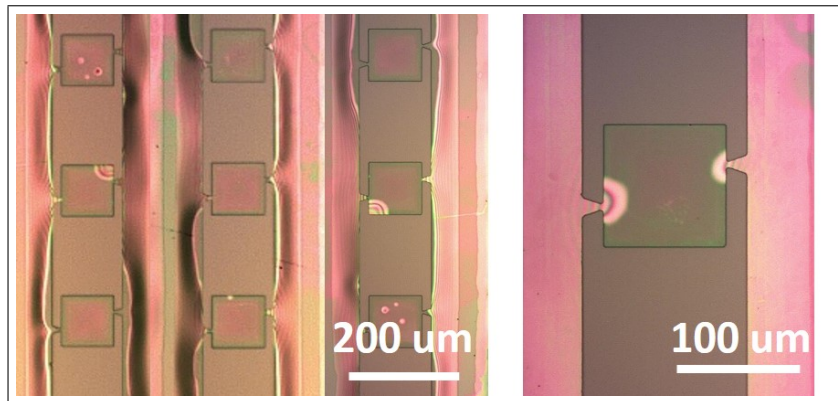


Figure 4.5: a) Suspended devices array and b) close up of a suspended device

4.2.2 Fabrication of the elastomeric stamp.

The transfer printing process uses an elastomeric stamp, commonly Polydimethylsiloxane (PDMS) material, as a means to pick up the material from its native substrate (donor) and place it to the target substrate (receiver). The tackiness of the stamp is related to the ratio used in the fabrication. In this case, a 10:1 ratio stamp was used. For better adhesion between the stamp and the membrane, the stamp has the same cross sectional dimensions as the membrane and a thickness of $100\ \mu m$. For better release, a four-square pyramid pattern on the sides of the stamps was used with height $7\ \mu m$ [205]. The stamp mold was fabricated on Silicon wafer by standard lithography and etching process and the pyramid shape was achieved by using anisotropic KOH wet etching. The PDMS was poured in the mold and cured for 24 hours at room temperature and then 1 hour on a hot plate at $150^{\circ}C$. After the curing process, the elastomeric material is released from the mold and mounted on the transfer printing system [205], [206], [207].

4.2.3 Fabrication of ridges

The ridges are made of SU8 negative tone photoresist and were fabricated on silicon substrate by using laser lithography. By adjusting the laser parameters, the height and width can vary and the one used in this study resulting to ridge of $h=1.15\ \mu m$ and $w=3.5\ \mu m$ and $h=1.50\ \mu m$ and $w=4.5\ \mu m$, respectively.

4.2.4 Transfer printing of Silicon membranes

The fabricated silicon membranes were picked up from the donor and printed on the silicon substrate over the ridge by using elastomeric transfer printing. The process is well documented in previous publications [203], [209], [210], [211]. The whole process relies on the competitive adhesion between different materials, bringing them into contact through Van der Waals forces. This process is rate sensitive, which means that we can enhance the pick-up and printing by adjusting the speed of the process and the criterion of this is illustrated in Figure 4.6 [208]. The membrane was picked up with high speed from its donor and transfer printed with low speed in the middle of the

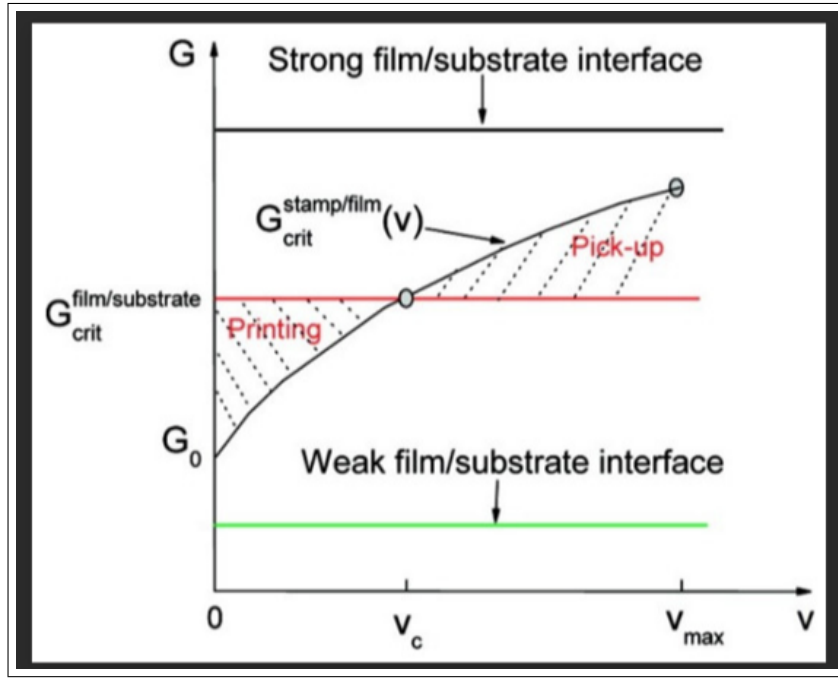


Figure 4.6: Schematic diagram of critical energy release rates (G) for the film/substrate interface and for the stamp/film interface as a function of speed (v), indicating maximum speed (v_{max}) and critical velocity (v_c) [208]

ridge with micrometer accuracy. An illustration of the process can be seen in Figure 4.7. The stamp is brought in close contact with the membrane and by quickly pulling it, due to the preferable adhesion, the membrane is attached on the stamp. The stamp is moved on top of the receiver substrate and brought in contact with the ridge. By slowly removing the stamp, the membrane is finally printed on top of the ridge. Figure 4.8 shows a microscope top view and an SEM 35° image of the printed membrane on top of the ridge for the $h=1.15 \mu\text{m}$ and $h=1.50 \mu\text{m}$ cases.

The printed membrane shows clear conformation to the ridge it is printed over, hence a mechanical deformation that is permanent once the stamp has released the membrane in place. In the optical micrographs of Figure 4.8, optical fringes are easily identifiable. They originate from optical interference of the illumination light due to the gap between the backside of the membrane and the substrate. In addition, the width of these fringes is increasing with the distance away from the top of the ridge indicating a non-uniform gap i.e. a curvature of the membrane. This will be analyzed in more

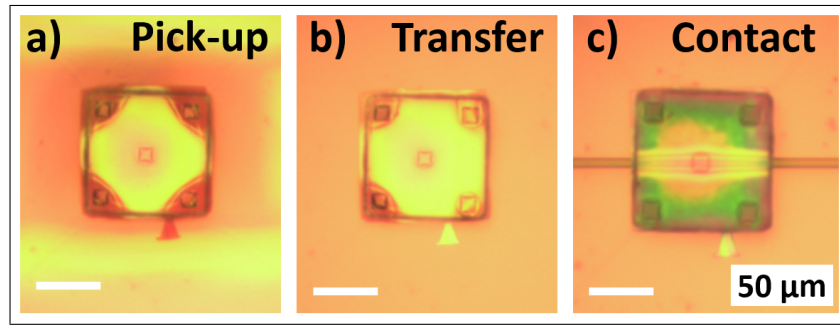


Figure 4.7: Optical images presenting the stamp transfer printing. a) The membrane is picked from the host substrate b) The membrane is attached on the stamp and transferred to the receiver substrate and c) The membrane is brought in contact with the ridge

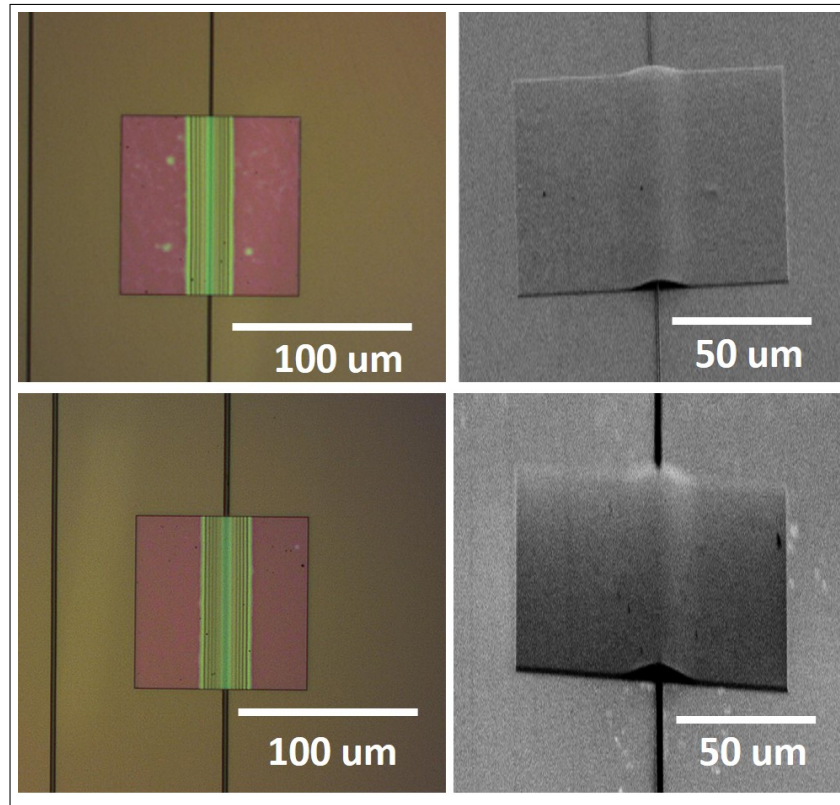


Figure 4.8: a microscope top view and an SEM 35° image of the printed membrane on top of the ridge Top images for the $h=1.50 \mu m$ and bottom for $h=1.15 \mu m$

details in section 4.3.5. The areas on both sides of the membrane, where there are no fringes, correspond to a full contact to the receiving substrate. Knowing the distance per pixel calibration of the imaging setup, the contact length can thus be estimated

at $39\ \mu\text{m}$ and $35\ \mu\text{m}$ for $h=1.15\ \mu\text{m}$ and $h=1.50\ \mu\text{m}$, respectively. The tilted SEM imaging in Figure 4.8 visually confirms the previous description, namely an s-shape conformation behaviour.

4.3 Analytical analysis of the s-shape cantilever beam

Deformation

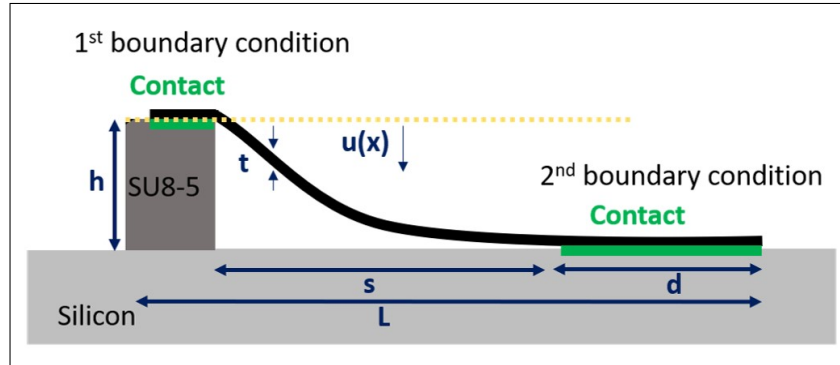


Figure 4.9: Schematic representation of the theoretical model of the one supported cantilever showing the contact length d , the unadhered length s , the thickness t , the deformation equation $u(x)$ and the height of the ridge (h).

The S-shape of the Si membrane from the top of the ridge to the substrate can be approximated by a simple cantilever model, where one part is fixed top of a ridge, and the other adheres to the substrate. A schematic representation can be seen in Figure 4.9. The printed membrane on top of the ridge, creates an s-shape conformal behavior on each side, which previous studies from different research groups have extensively examined this model to identify the maximum crack length (referred to as the unadhered part on a nanometer scale) [212] [213]. This length represents the extent to which the membrane can deform before transitioning from elastic to plastic deformation. In existing models, adhesive and elastic strain energies are computed using the beam and support's geometric characteristics, with the force applied known through load sensors. However, in this case, forces in the beam involve bonding forces on the contact area (Van der Waals), the Casimir forces close to the bonding area which are of unknown magnitude, as well as the force applied from the stamp during the transfer printing

process, given that we induce the model by transfer printing membranes onto ridges. Although the force used to print the membrane on the receiver is approximately in the microNewton range, the exact force during the entire pickup and transfer process, especially on non-flat surfaces, remains unclear.

Therefore, we employ a theoretical model to determine beam deformation and curvature. In the theoretical model, we address the lack of knowledge about the applied force by resolving the problem through energies. Focusing on the single support model, we divide the problem into two regions:

- Region (a) ($0 \leq x \leq s$):

the unadhered part (with maximum curvature) governed by elastic strain energy and

- Region (b) ($s \leq x \leq l$):

the bonding area, where bonding forces aim to bring the membrane into contact with the substrate.

The total energy in the attached beam combines elastic energy from the bending of the beam to meet the substrate and a reduction in surface energy from the beam/substrate interface. By solving for the system's minimum total energy, we can accurately determine the equilibrium surface energy. The process begins by quantitatively assessing the stored elastic energy in the adhered beam. With the body stable and no external forces acting, the equilibrium between these areas is described by the differential equation:

$$EI \frac{d^4 u}{dx^4} = 0, \quad I = \frac{wt^3}{12} \quad (4.1)$$

where E is the young modulus of the material, $u(x)$ is the deformation of the membrane, I is the moment of inertia and w and t the width and the thickness of the membrane, respectively. Taking into consideration the boundary conditions of the problem

$$\left. \frac{du}{dx} \right|_0 = 0, \quad \left. \frac{du}{dx} \right|_s = 0, \quad u(0) = 0, \quad u(s) = h \quad (4.2)$$

which means that the slope at the point $x=0$ (the top of the ridge) and $x=s$ (point that the unadhered part ends) is 0 and that the deformation at these points is 0 and h respectively.

By applying these boundary conditions in 4.1, the deformation $u(x)$ as a function of x is given by:

$$u(x) = h(x/s)^2(3 - 2(x/s)) \quad (4.3)$$

where h is the height of the support, and s is the unadhered part which can be easily calculated by subtracting the contact area of the total length

$$(L - d)$$

Figure 4.9 shows a schematic representation of the s-shape deformation and the areas of interest related to Equation 4.3 which is the unadhered part, the support and the contact length.

The resulted deformation graph as a function of the distance from the ridge for both $h=1.15 \mu m$ and $h=1.50 \mu m$ can be seen in Figure 4.10

4.3.1 Slope and curvature

The first derivative provides valuable information about the beam's curvature and bending behavior. Positive values of the derivative indicate an upward slope or convex curvature, while negative values indicate a downward slope or concave curvature. The magnitude of the derivative represents the steepness of the slope at that point. The first derivative of the deformation equation for an S-shaped cantilever beam reveals the slope of the beam at any given point along its length. This derivative indicates how the deflection of the beam changes with respect to the axial position along the beam. The deformation equation itself describes the relationship between the deflection, denoted as u , and the axial position, denoted as x , along the beam's length. By taking the first derivative of this equation, expressed as du/dx or $u'(x)$, we can determine the slope of the beam at a specific point. Mathematically, it represents the rate of change

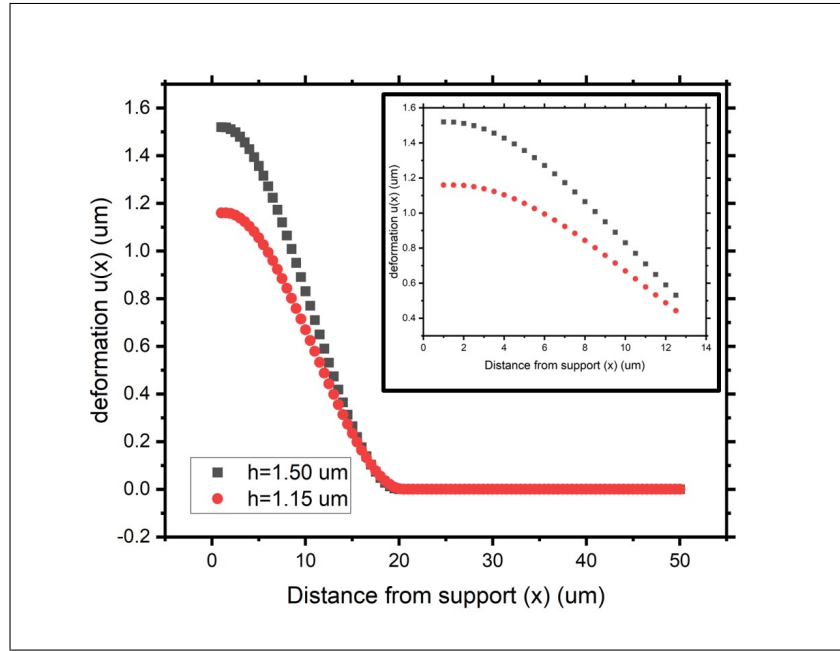


Figure 4.10: Schematic representation of the one-supported cantilever, indicating the curvature in the points of interests.

of the deflection with respect to the axial position:

$$u'(x) = \frac{du}{dx} \quad (4.4)$$

By examining the first derivative throughout the beam, points of maximum deflection, inflection points (where the curvature changes), and critical points where the slope is zero or approaches zero can be identified. These insights are crucial for analysing the structural integrity, stability, and design considerations of the cantilever beam. The second derivative, $u''(x)$, represents the curvature of the beam. It provides information about how the slope is changing along the beam and can help identify points of maximum curvature or points where the curvature changes sign (points of inflection).

The second derivative of 4.3 gives the curvature κ of the beam as a function of x .

$$\kappa = \frac{d^2u(x)}{dx^2} = \frac{6h}{s^2} - \frac{12h}{s^3}x \quad (4.5)$$

If the curvature is zero, implies that the object is either straight or is undergo-

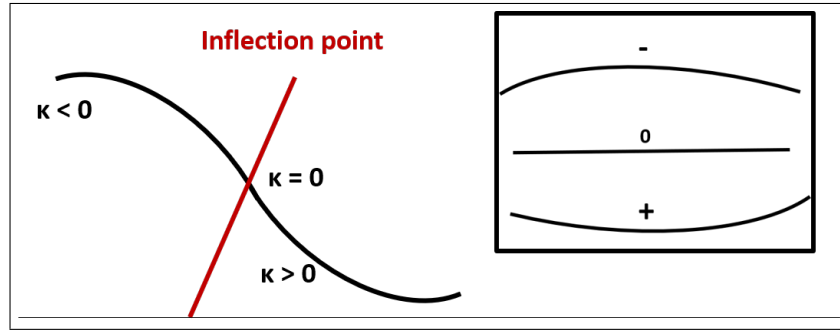


Figure 4.11: Schematic representation of the one-supported cantilever, indicating the curvature at the points of interest.

ing linear deformation without any bending. A schematic representation of the bent single supported cantilever, indicating the curvature at the points of interest and its corresponding sign can be seen in Figure 4.11.

The area that makes sense to talk about curvature is the unadhered part which is $0 \leq x \leq s$.

In that area there is a single point where the curvature is 0, which is the inflection point that the beam changes from concave to convex. This point can be found if we solve the Equation 4.5. and set it 0:

$$\frac{6h}{s^2} - \frac{12h}{s^3}x = 0 \Leftrightarrow \frac{6h}{s^2} = \frac{12h}{s^3}x \Leftrightarrow x = s/2 \quad (4.6)$$

The maximum value that the x can take is when $x=s$. that is the end point of the deformation with the curvature having the minimum value very close to 0. In the area

$$x > s$$

there is no bending or deflection and the beam has a linear configuration with zero curvature. Therefore, $\kappa=0$ (and thus R is infinity)

By using simple trigonometry and geometry, we can derive the radius of curvature of the membrane deformation over its length. This is important as by using a simplified version of the bending theory, we can derive the normal uniaxial strain in the perpendicular direction. The right image of Figure 4.12a) shows an SEM image at a tilt of 70°

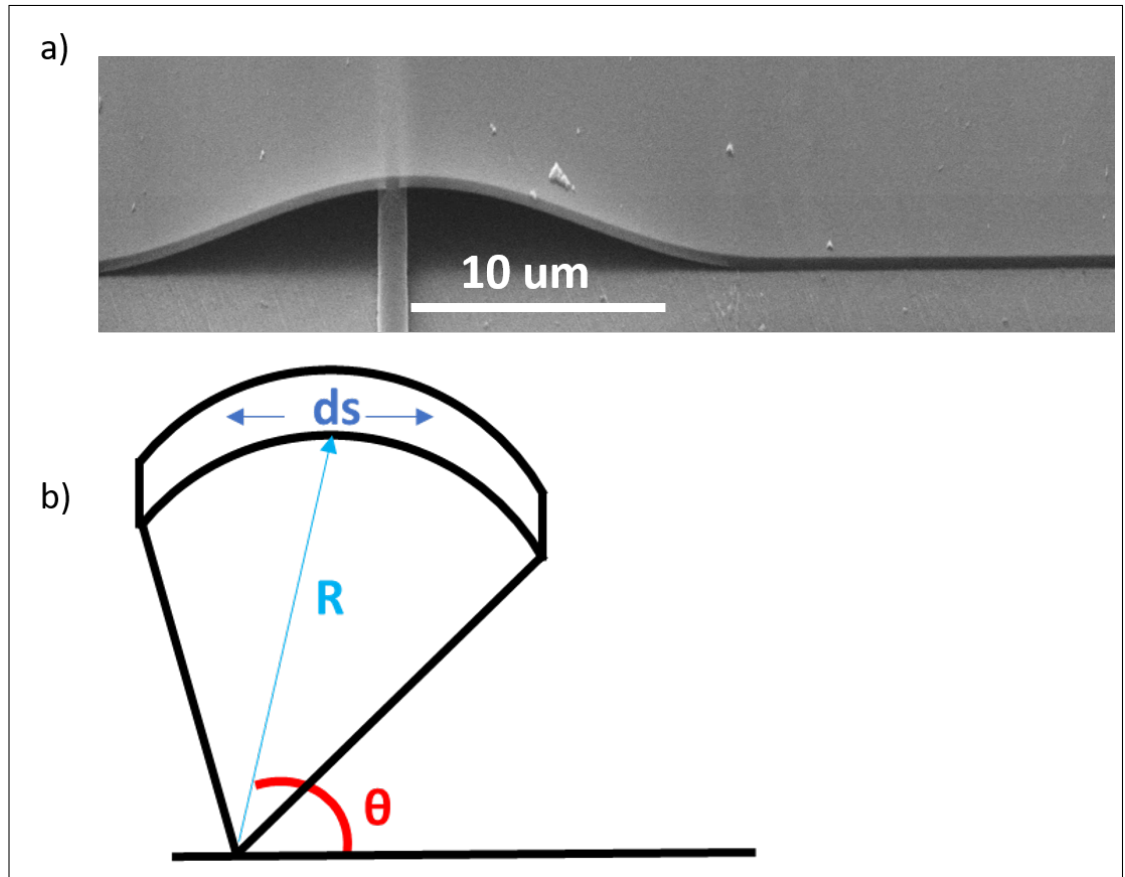


Figure 4.12: a) Close up SEM 70° tilted image of the transfer printed membrane on top of the ridge and b) schematic illustration of the deviation of the radius and angle of curvature.

of the membrane including a schematic of the radius of curvature deviation and Figure 4.12b) illustrates the corresponding schematic at scale for clarity. It indicates that with trigonometry and geometry rules, the radius of curvature of the membrane deformation can be derived. Therefore, in association with a simplified version of the bending theory, the normal uniaxial strain in the perpendicular direction of deformation can also be derived. From the circle, we know that

$$ds = R d\theta \quad (4.7)$$

where R is the radius of curvature and θ is the angle of curvature. Thus, from

trigonometry and Pythagoras' theorem, we also have:

$$\tan\theta = du/dx \quad (4.8)$$

and

$$ds = \sqrt{dx^2 + du^2} \quad (4.9)$$

where θ is the angle of curvature. By doing some modifications on Equation 4.7 and and insert them in Equation 4.9, we derive the following equation for the radius of curvature:

$$R = \frac{dx \sqrt{1 + (\frac{du}{dx})^2}}{\frac{d^2u}{dx^2} dx} (1 + (\frac{du}{dx})^2) = \frac{(1 + u'^2)^{3/2}}{u''} \quad (4.10)$$

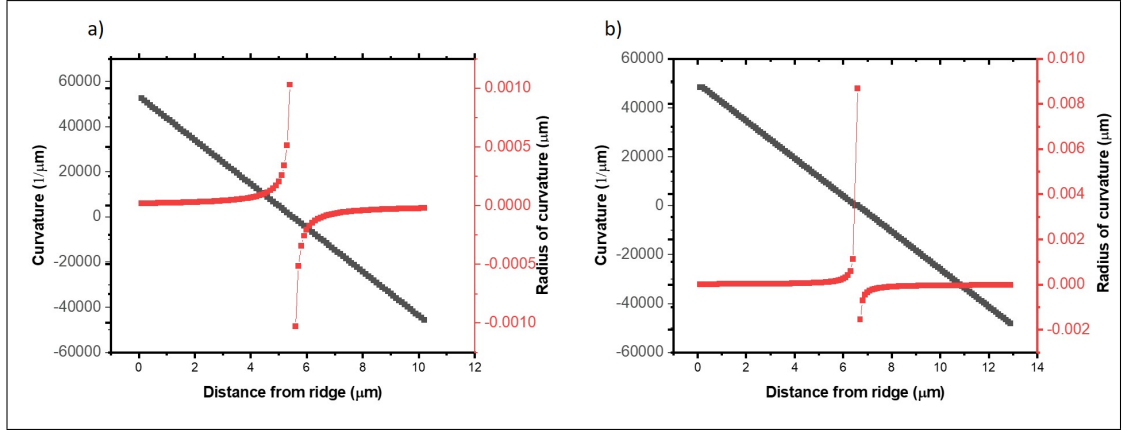


Figure 4.13: Graphs of curvature and radius as a function of the distance from the support a) for $h=1.15 \mu m$ and b) for $h=1.50 \mu m$.

where u' and u'' the first and second derivative of the deformation, respectively. By differentiating 4.3, the radius of curvature of the deformed membrane is calculated. Figure 4.13 shows the graphs of the curvature and radius of curvature as a function of distance from support for both $h=1.15$ and $h=1.50 \mu m$, respectively.

The calculated angle of curvature from Equation 4.8 can be seen for both cases in Figure 4.14. What we can see is that for $h=1.15 \mu m$ the maximum angle is 11° while for $h=1.50 \mu m$ is 9° . The angle of curvature is a measure of the deviation of a curve

from a straight line at a particular point. In the context of deformation, the angle of curvature can provide insight into how much a material or structure has been bent. That means that there is already an indication of which height gives the higher strain induced.

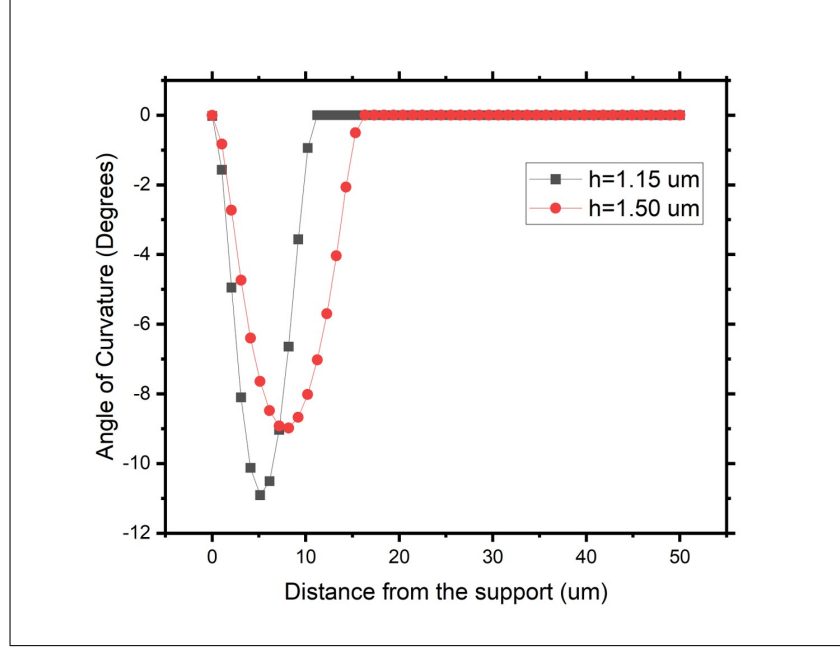


Figure 4.14: Graph of calculated angle of curvature as a function of the distance from the support.

4.3.2 Strain

In bending theory, the relationship between strain, thickness, and curvature can be derived through the analysis of the behavior of materials under bending stress. When a beam or a plate is subjected to bending, it experiences both tensile and compressive stresses through its cross-section. The strain in the material is a measure of the deformation that occurs due to these stresses. The relationship between strain, thickness, and curvature can be derived using fundamental principles of mechanics and material behavior [214].

Strain is related to the radius of curvature and thickness of a material through the concept of bending [215]. The radius of curvature plays a significant role in determining

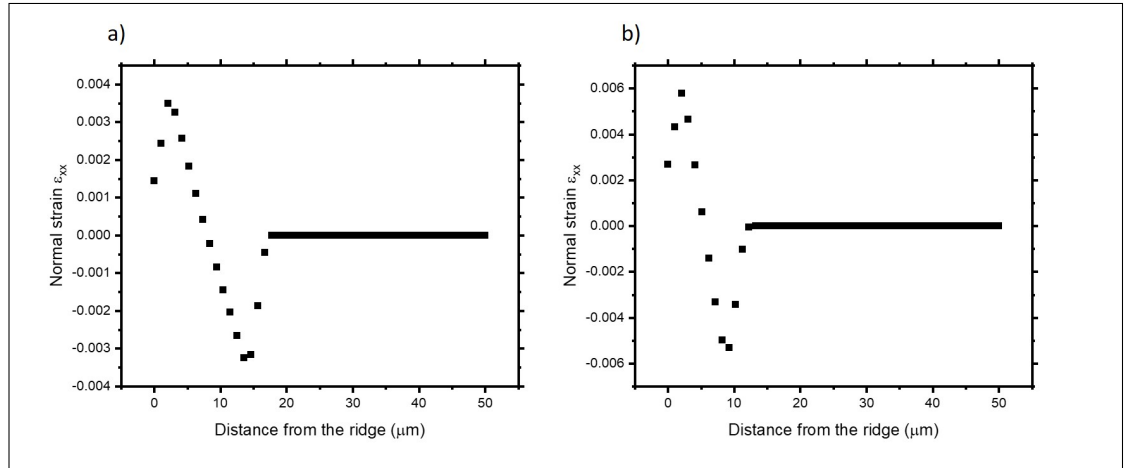


Figure 4.15: Graph of normal strain in x-direction as a function of the distance from the support. a) For $h=1.50 \mu\text{m}$ and b) for $h=1.15 \mu\text{m}$

the amount of strain experienced by a material during bending. A smaller radius of curvature results in higher strain levels in the material. The thickness of the material also affects the strain experienced during bending. Thicker materials tend to exhibit lower levels of strain compared to thinner materials when subjected to the same bending force. This is because thicker materials have more resistance to deformation due to their greater cross-sectional area. Thinner materials, on the other hand, are more susceptible to deformation and therefore experience higher levels of strain during bending.

The strain values can be calculated by using the simple equation of bending theory:

$$\epsilon = \delta R / R = t / 2R \quad (4.11)$$

where ϵ is then defined as the ratio of the radius change in length to the radius original length and t is the thickness of the membrane. [216]. This equation shows that strain is directly proportional to both curvature ($=1/R$) and thickness. From that equation, what we can see is that the more we increase the unadhered part, the less the curvature and the smaller the strain induced. Figure 4.15 shows the calculated strain for both cases by using Equation 4.11.

Figure 4.16 shows a schematic illustration of the strain induced in the cross section of the beam. The neutral axis at the middle of the beam experiences zero strain, while

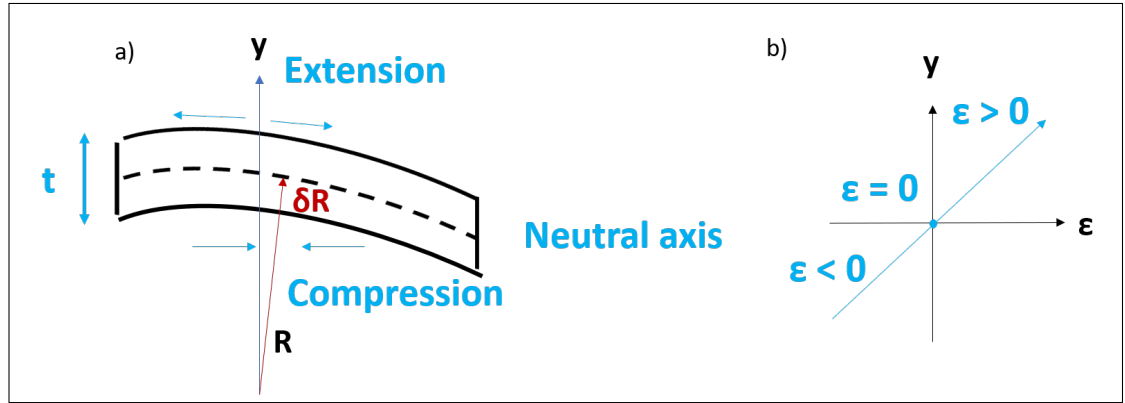


Figure 4.16: Cross section of the membrane a) Schematic illustration of the cross section of the beam, showing the thickness of the membrane t , the neutral axis which is in the middle of the membrane $t/2$, the radius of curvature R , the small deviation of R , δR when strain is applied, and the top and bottom layers where extension and compression occurs, respectively and b) graph indicating the strain values for compression ($\epsilon < 0$), in the middle section ($\epsilon = 0$) and for extension ($\epsilon > 0$).

the top and bottom layers upon bending, experience the same amount of strain with opposite signs, indicating extension and compression, respectively. In this work, the strain calculation is focused on the top layer of the beam, as this is what it is accessible for the electron backscatter measurements which are shown in the following sections.

4.3.3 Deformation as a function of time

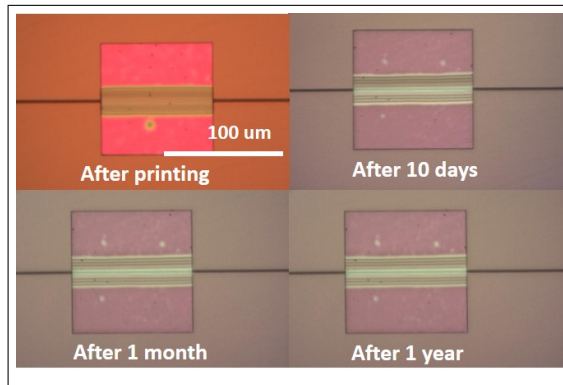


Figure 4.17: 20x microscope optical images of the printed membrane on top of the ridge with $h=1.15 \mu m$ after printing, after 10 days, after 1 month and after 1 year

In this work, it is important to show that the resulted deformation of the mem-

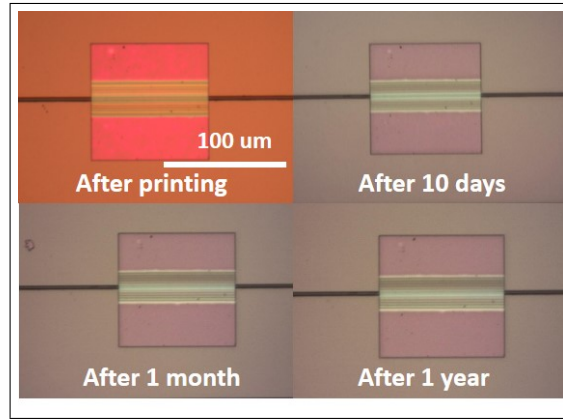


Figure 4.18: 20x microscope optical images of the printed membrane on top of the ridge with $h=1.50 \mu m$ after printing, after 10 days, after 1 month and after 1 year

brane on top of the ridges is not affected by time. For this reason, the deformation was calculated experimentally after the transfer printing process, after 10 days, after one month and finally after one year. The way that the measurement was conducted was by measuring the contact length through the microscope optical images. The following images are presented in Figure 4.17 and 4.18 for $h=1.15 \mu m$ and $h=1.50 \mu m$, respectively, and the results for each case can be seen in Figure. The contrast of the first photo in Figure 4.17 and 4.18, is due to the fact that the image was taken by the microscope camera in the transfer printing tool after the printing, rather than the microscope camera located in the optical microscope setup, which was used for the inspection of the rest. Although optically there is no obvious difference, when the Image J software [217] was used in order to measure the contact length, some changes were observed. these changes can be seen in Figure 4.19 , where a) and c) show the deformation after printing, and b) and d) show the deviation of the deformation over time and shows the graphs of the deformation for the different periods for $h=1.15 \mu m$ and $h=1.50 \mu m$, respectively. What can be noticed from these graphs, is that in both cases there is a very slight difference on the deformation within the first 10 days, while after that period, the deformation remains the same. This result ensures the maintenance of the deformed shape, indicating the stability of the potential device which it can be integrated into.

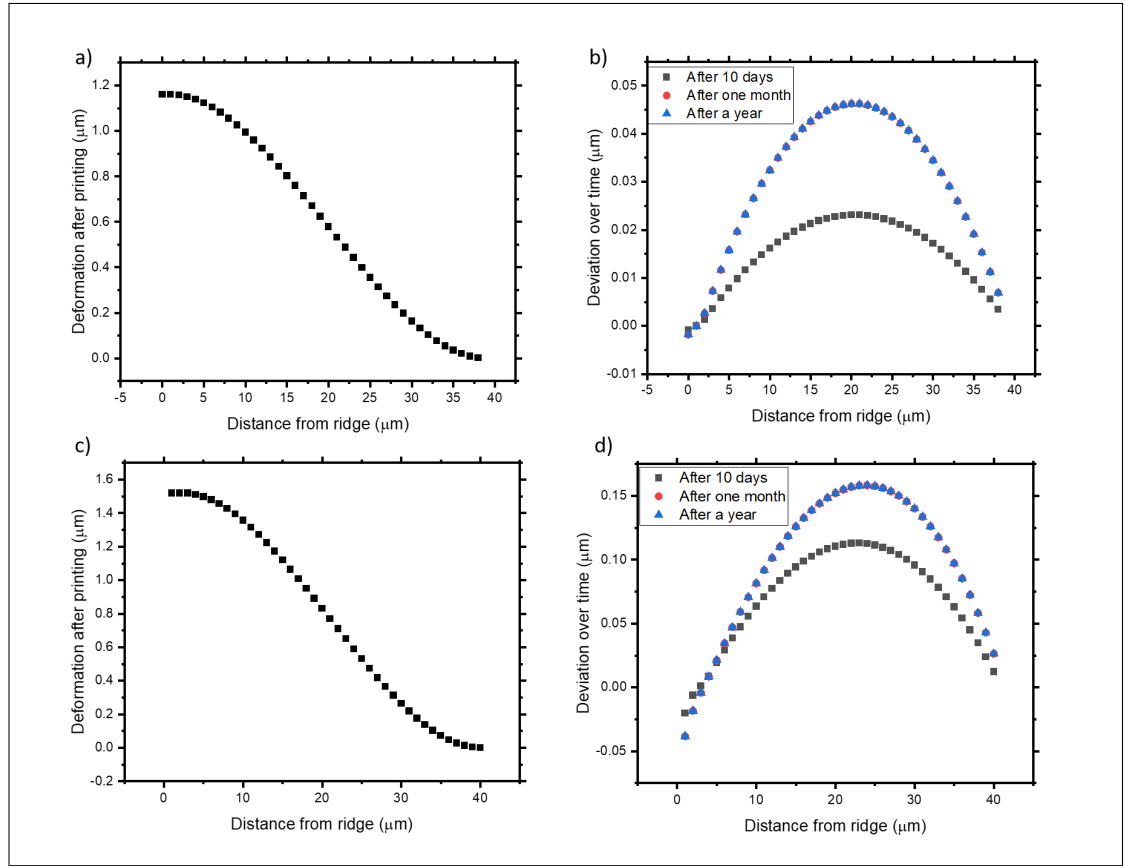


Figure 4.19: Graphs of the membrane deformation for different time periods. For $h=1.15 \mu\text{m}$: a) deformation after printing as function of the distance from ridge, b) Deviation of the deformation over time. For $h=1.50 \mu\text{m}$: c) deformation after printing and d) deviation over time.

4.3.4 Analysis of the optical fringes

When optical fringes appear, it indicates the presence of a gap between two materials due to the phenomenon of interference. Interference occurs when two or more waves overlap in space and time, leading to the reinforcement or cancellation of certain parts of the waves. In the case of optical fringes, they are produced when light waves from a source travel through different media with varying refractive indices and then recombine. The difference in optical path lengths traveled by the light waves results in constructive or destructive interference, leading to the formation of bright and dark fringes. The appearance of optical fringes can be explained by considering the behavior of light waves at the interface between two materials.

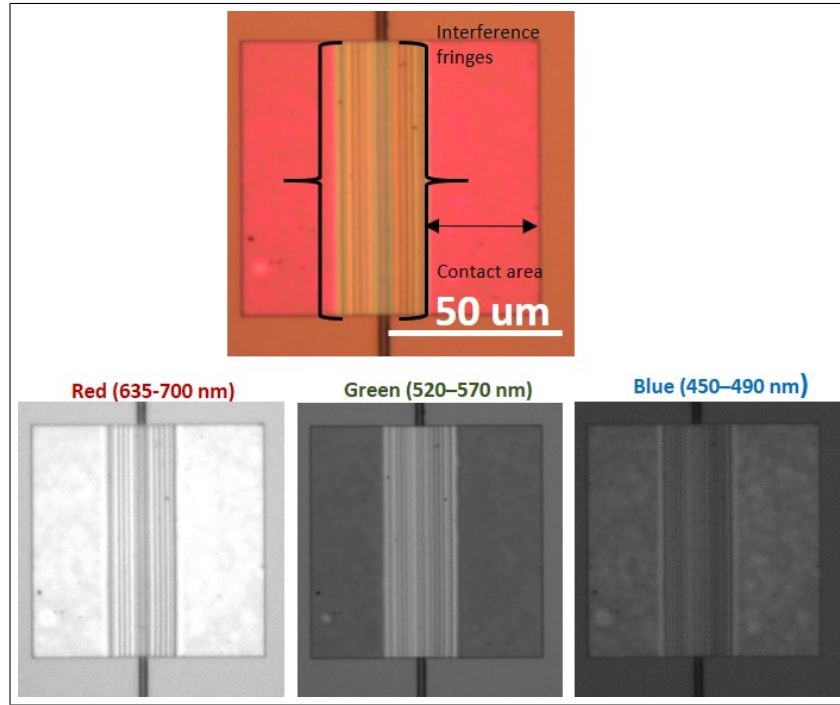


Figure 4.20: Split of the colourful image in different channels (example of the $h=1.50$ μm)

The condition for constructive interference for normal incidence, which leads to the formation of bright fringes, is expressed by the equation $2d \cdot n = (m + 1) \cdot \lambda$, where d represents the separation gap between the materials, n is the refractive index of the medium between the materials, m denotes the order of the fringe, and λ is the wavelength of the light source used. [218].

In order to analyze the fringes patterns in the conformal membranes, the original microscope image (captured by white light), was split into the three different filter channels: Red ($\lambda=635-700$ nm), Green ($\lambda=520-570$ nm) and Blue ($\lambda=450-490$ nm). Figure 4.20 shows the resultant images after the filter separation and Figure 4.21 shows the intensity profile for the different colour filters. We notice that in the case of the $h=1.50$ μm the number of constructive optical fringes is 5, while in the case of $h=1.15$ μm is 4. By using the refractive index of air as the medium ($n=1$), the plots for both cases can be plotted for the different filters. It can be noticed that the resulted separation height gives a good approximation of the deformed part for both cases.

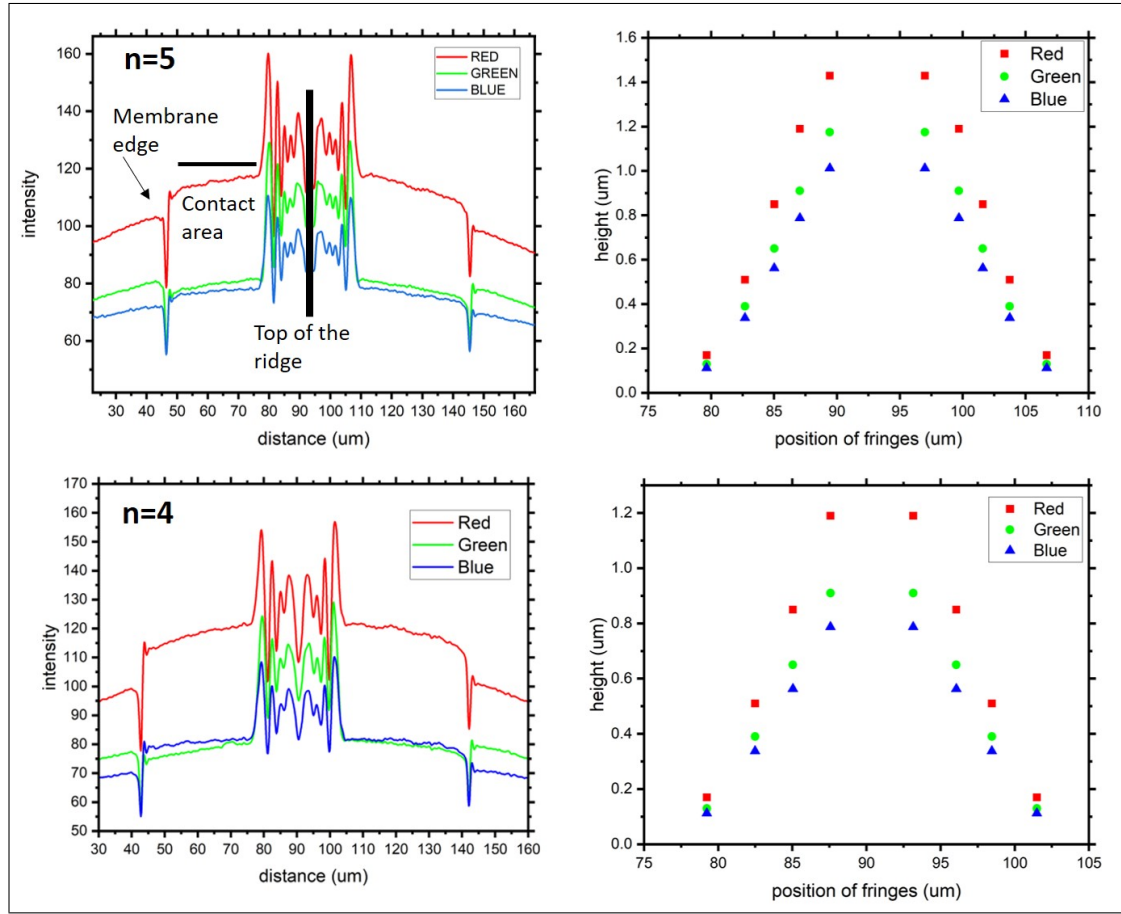


Figure 4.21: Intensity graphs for the different colour filters as a function of the scanning distance, highlighting the top of the ridge, the contact area and the edges of the membrane, and separation height as a function of the position of the fringes. Top graphs correspond to $h=1.50 \mu m$ and bottom graphs to $h=1.15 \mu m$

However, in order to have accurate results, a monochromatic light should be used for this analysis.

4.4 Finite Element analysis by using Static Structural Ansys Software

The simulations performed in this study employ Ansys Mechanical R2022 software [219], [220]. Ansys is widely utilized in a variety of fields, including aerospace engineering, medical sciences, and chemistry, as a mechanical engineering software solu-

tion [221], [222], [223], [224] [225]. Ansys Mechanical software is widely used for a diverse range of engineering applications, leveraging its capabilities for finite element analysis (FEA) and obtaining numerical solutions to various mechanical problems [226]. The software's versatility is evident in its application across different domains [227], [228], showcasing its utility in analyzing composite materials.

Ansys Mechanical was used to perform a Finite Element Analysis (FEA) on thin film silicon cantilevers. These cantilevers were arranged in such a way that one side was supported by a ridge with a height denoted as 'h', while the other part was attached to a substrate. As a result, the membrane formed an s-shaped deformation. Investigating the deflection and curvature of this deformation is crucial because it provides valuable insights into the induced strain. The Ansys Workbench Environment and the full procedure of the analysis are presenting in Appendix A.

4.4.1 Basics of the Finite Element Analysis (FEA).

The finite element analysis (FEA) is a powerful computational method used to analyse the behaviour of complex structures and systems. It is used for solving complex engineering problems by dividing the domain of interest into smaller, simpler subdomains called finite elements. These elements are interconnected at discrete points called nodes, forming a mesh that represents the original domain. The FEA is employed to approximate and solve differential equations governing the behavior of the system under consideration [229].

This method has found extensive application in various fields, including structural mechanics, fluid dynamics, heat transfer, and electromagnetics [230], [231], [232], [233], [234]. The finite element method (FEM) is widely used for stress analysis in beams due to its ability to accurately model and predict the behavior of complex structures [235], [236], [237].

At its core, FEM involves dividing the system into smaller, more manageable parts called finite elements. A schematic representation of the FEA method is illustrated in Figure 4.22. Each element represents a specific region of the structure and is characterized by its geometric shape, material properties, and connectivity to neighbouring

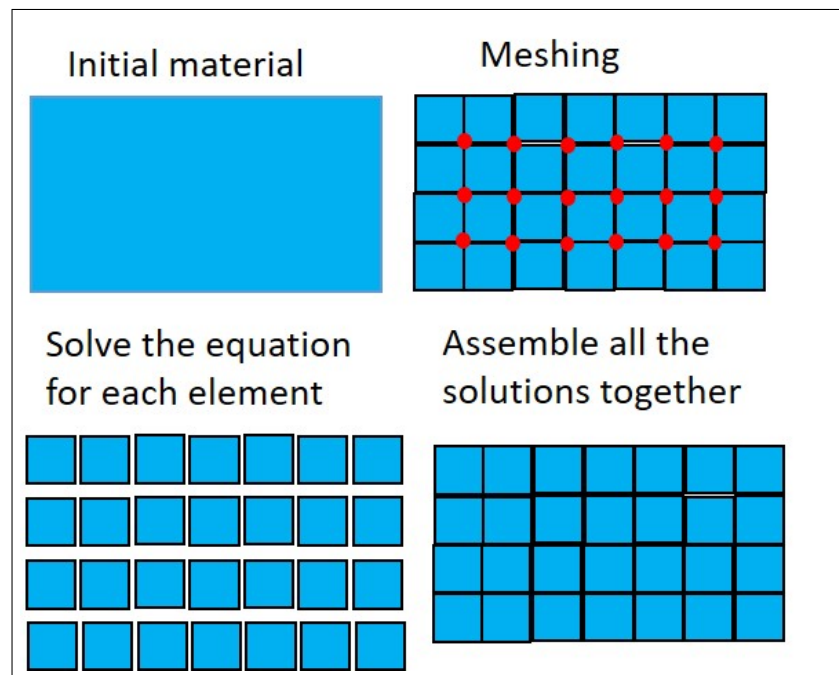


Figure 4.22: Schematic representation of the FEA method.

elements. To begin the analysis, the structure is discretized by placing nodes at key points within each element. These nodes serve as reference points where the behaviour of the structure is evaluated. The elements are then connected through these nodes to form a mesh, which represents the overall geometry of the system. Once the discretization is complete, the next step is to establish the governing equations for each finite element. These equations are derived from fundamental physical principles and describe the relationship between the applied loads, the structural response, and the material properties. The equations typically involve concepts such as equilibrium, constitutive relations, and boundary conditions. After formulating the governing equations, they are assembled to create a system of equations that represents the entire structure. This assembly process involves considering the connectivity of nodes and combining the individual element equations into a global system. With the system of equations in place, numerical techniques are employed to solve for the unknowns. These techniques may include the finite element method, matrix algebra, or iterative methods. By solving the system of equations, FEA provides valuable information about the behaviour of the structure, such as displacements, stresses, strains, and other relevant

quantities [238], [239], [240].

The fundamental equation for FEA is

$$[K]U = F \quad (4.12)$$

where F is the input load vector, $[K]$ is the global stiffness matrix, and U is the unknown displacement vector to be determined at each node in the model [241].

Non-linearities in an analysis can arise from material properties, geometry (deformations), and contact interactions. In this model, the force is non-linear, resulting in non-linear deformations, which necessitates the use of a non-linear analysis method.

In non-linear analysis, the global stiffness matrix is recalculated at every iteration. Here, the Newton-Raphson method, a robust numerical technique, is used to solve systems of equations iteratively [242]. Figure 4.23 shows a representative diagram of this method, where the X-axis represents cumulative iteration numbers and the Y-axis represents force in Newtons. Each point corresponds to an equilibrium iteration. This method iteratively solves the non-linear equation system by using tangents (stiffness matrices). At each iteration, the tangential stiffness matrix is determined based on the current state of deformation and then inverted to update the solution. Convergence occurs when the solution accurately determines displacements for the applied load [243]. This method is particularly effective for finding successively better approximations to the roots of real-valued functions and is widely used in structural analysis for deformation studies.

Once the numerical solution is obtained, post-processing techniques are applied to interpret and visualize the results. Contour plots, stress distribution maps, deformation animations, and extract specific quantities of interest from the analysis can be generated. This enables a comprehensive understanding of how the structure responds to different loads and conditions. For this particular study, the analysis of the directional deformation in all axes and the generation of maps depicting normal and shear strains are conducted. These data provide insights into how the applied force and ridge height impact the induced internal strain within the cantilever and its individual components. To aid in result interpretation, we visualize the outcomes using graphical

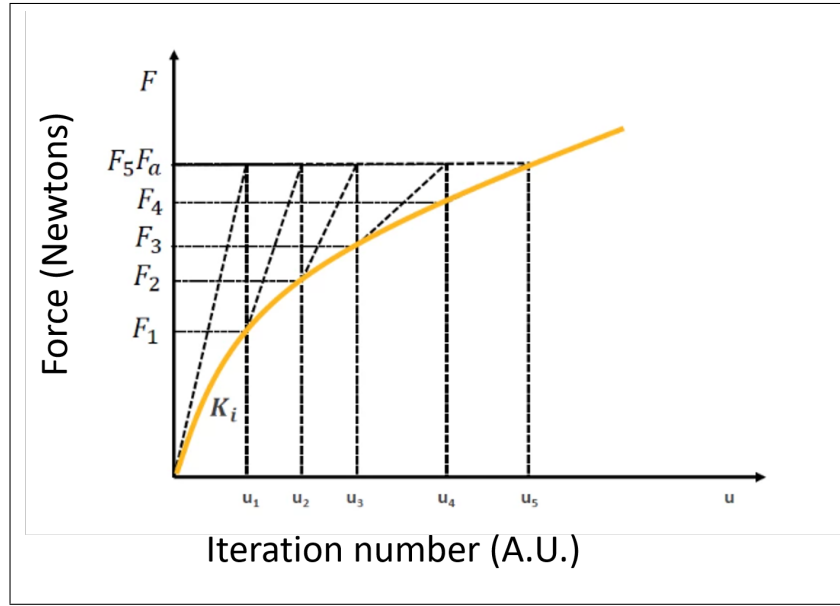


Figure 4.23: Representative graph of Newton-Raphson method [244].

representations and colour maps, facilitating a better understanding of the structural response.

Furthermore, we validate the analysis results through various approaches, including analytical analysis, experimental validation, or comparative analysis. By comparing the Ansys results with analytical solutions, experimental data, or established benchmarks, we ensure the accuracy and reliability of our findings. Any discrepancies or limitations identified during the validation process are carefully addressed and accounted for. In this work, in order to verify our simulation results, the deformation of our sample was tested experimentally and an EBSD measurement was performed on the resulted deformed cantilever. A theoretical model was also used to study the behavior on each case. The results matches the simulation results in the case that we compare the resulted contact length and the stress induced. As the results for both models are similar and they don't exhibit any major differences, in the following sections, only the one model with $h=1.50 \mu m$ is going to be presented, while the second one is presented in Appendix A.2.

4.4.2 Simulation results and analysis

The mechanical deformation simulations performed here employ Ansys Mechanical R2022 software [219, 220] to perform a FEA on thin film silicon cantilevers. These cantilevers were arranged in such a way that one end was supported by a ridge with a height denoted as ' h ', while the other end bent downwards to become attached to the substrate. As a result, the membrane formed an s-shaped deformation. Investigating the deflection and curvature of this deformation yields valuable insights into the induced strain. Prior to any geometry design, the materials properties need to be implemented in the model. In this study, silicon is used as material, which has the following properties: a density (ρ) of 2330 kg/m^3 , isotropic elasticity with a Young's modulus of 165 GPa , a Poisson's ratio of 0.22, a bulk modulus of $9.821 \times 10^{10} \text{ Pa}$, and a shear modulus of $6.76 \times 10^{10} \text{ Pa}$.

The model has two fixed, rigid, boundary conditions, one between the top of the ridge and the bottom surface of the membrane, the second at the surface of the substrate, representing the contacted area. The bonding of the membrane to the substrate was modelled as an applied distributed vertical force acting on the membrane, which could be varied as a parameter, as shown in Figure 4.24a). In this fashion, the adhesion force between the bottom surface of the membrane and the substrate is modelled and can then be compared with the experimental results through the measured contact length d of the two surfaces as described in the schematic of Figure 4.24b).

The behavior of the cantilever under variable loads acting downwards in the Z-direction is systematically modelled with magnitude in the order of μN . The dimensions of the cantilever are $50 \times 100 \text{ }\mu\text{m}^2$ and thickness 220 nm . Figure 4.24b) shows the resulting shape of the cantilever after the simulation and shows the top surface sampling of strain across one side of the membrane from ridge to contact area. This will give the following strain components, as can be seen on the element in Figure 4.24b). The ridge height was set at $1.50 \text{ }\mu\text{m}$, matching the experimental value. Under these different values, the curvature and the s-shape of the cantilever beam changed significantly, contributing to different normal (ε_{xx} and ε_{zz}) and shear (ε_{xy}) strains in the model, as analysed further below.

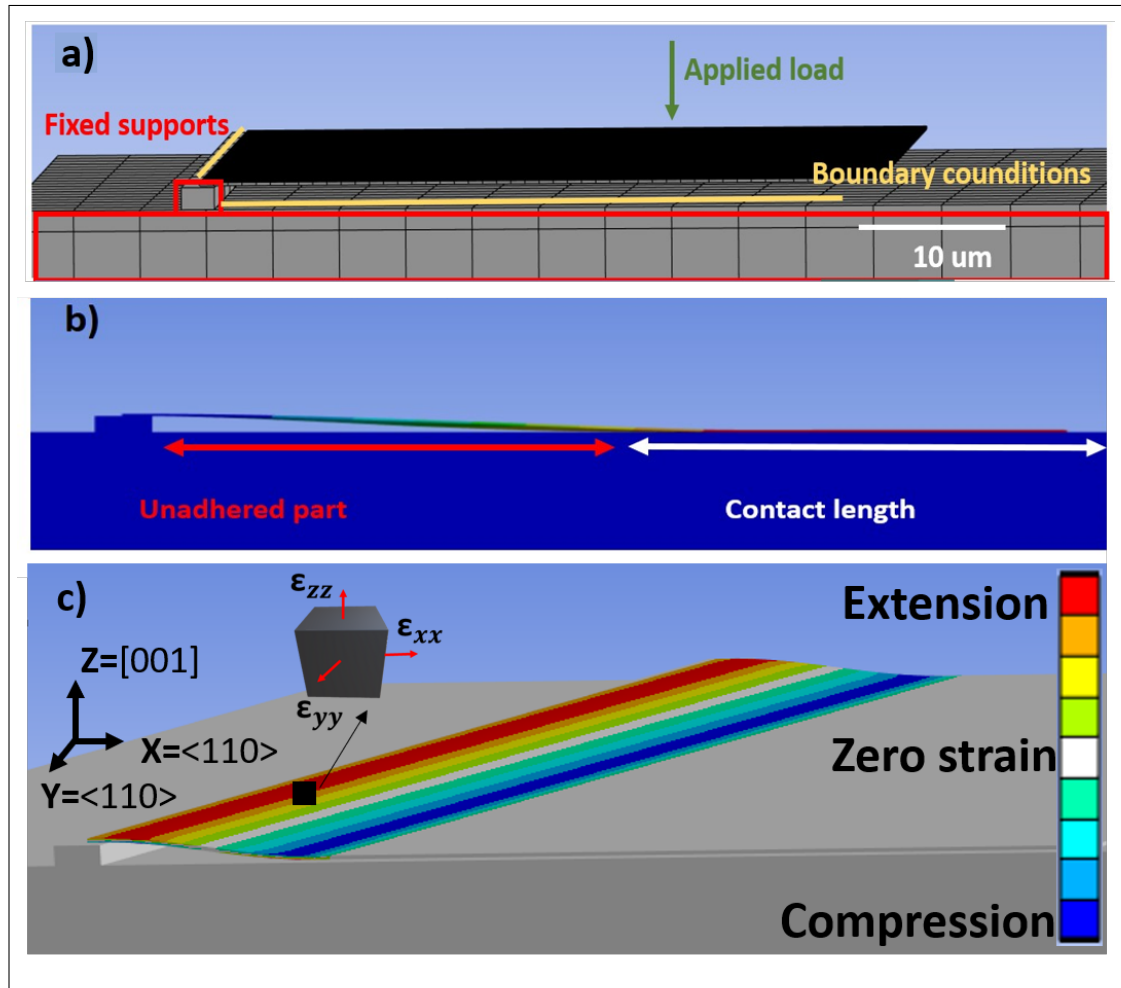


Figure 4.24: Ansys model for the deformed membrane. a) Initial state of the model, highlighting the fixed supports (ridge and substrate) the applied downwards force (Z direction), b) resulted shape after the simulation (s-shape deformation), and c) indicates the strain components of the deformed membrane with respect to the reference system.

Figure 4.25 a) shows the simulated results of the membrane deformation under selected magnitude of applied force of 1, 10, 100, 200 and 450 μN . The membrane starts contacting the substrate for loads in the region of 10 μN while a load of magnitude of 1 μN is not sufficient to bend the membrane into contact with the surface underneath. Figure 4.25b) shows the actual membrane profiles for the selected load magnitudes and depicts the associated vertical displacement against the contacted area. Upon increasing the magnitude of the applied load, the overall shape of the deformed membrane changed in terms of curvature, contacted and unadhered lengths. The latter increases

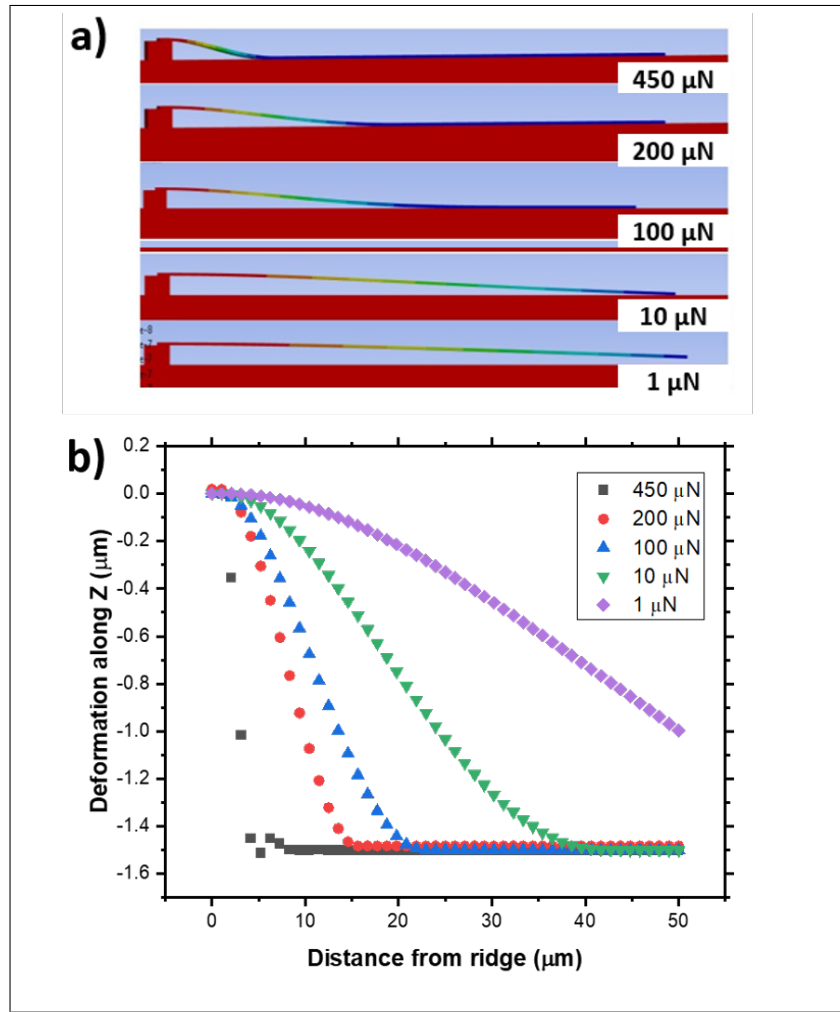


Figure 4.25: a) Representative s-shaped deformations for silicon membranes with various applied vertical load magnitude in relation to the contact length. b) Vertical deformation (Z direction) with the distance from the support for selected vertical load magnitudes in the μN range.

from 0 to 47 μm . The curvature of the membrane is employed to infer the internal shape of the membrane upon deformation.

4.5 Comparison of the different models to the experimental data

The FEA model was then run with the parameters matching the experimental configuration, notably a ridge height of $1.50\ \mu\text{m}$ and a membrane thickness of $220\ \text{nm}$. The membrane dimensions were kept unchanged.

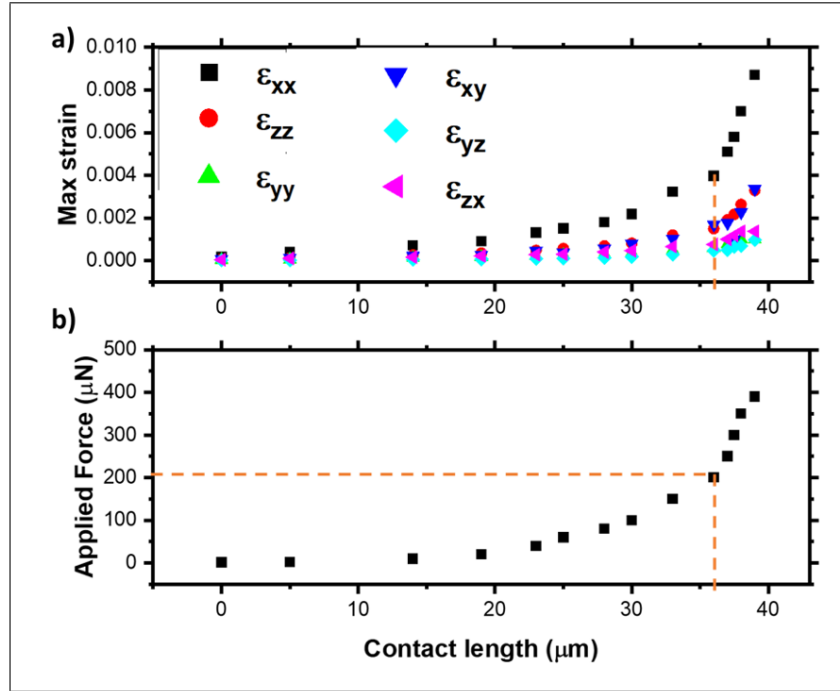


Figure 4.26: a) Maximum normal and shear strains against the contact length and b) the applied vertical force against contact length for ridge and membrane thickness corresponding to the experimental case, $h=1.50\ \mu\text{m}$ and $t=220\ \text{nm}$, respectively.

The top panel of Figure 4.26 shows the maximum values of shear and normal strains for each shape in the model, showing that the strain is strongly related to the contact length and, consequently, to the final shape induced by different vertical loads, as expected. Similarly, the bottom panel of Figure 4.26 shows the variation of the adhered part (contact length) of the membrane onto the substrate while the vertical load is varied. The contact length shows a sharp increase with load between 0 and $150\ \mu\text{N}$ with a contact length increasing from 0 to about $30\ \mu\text{m}$. At higher load, the contact length plateaus around $40\ \mu\text{m}$. For loads above $400\ \mu\text{N}$, there is a sudden increase in

the contact length to above $45\ \mu m$ that indicates where the model fails to represent real case scenario. When the applied load exceeds this threshold, the assumptions or limitations of the model no longer hold true, leading to unrealistic predictions such as an abrupt increase in contact length. This discrepancy indicates that the model's parameters are not suitable for simulating conditions beyond its intended range, causing it to deviate from actual physical behavior. Taking in consideration the experimental results from the previous section of a contact length of $35\ \mu m$ (marked with dash line in both panels of Figure 4.26), the FEA model indicates that the membrane has an equivalent load of $200\ \mu N$ applied. It corresponds to maximum normal strain across the whole membrane of 4×10^{-3} , 0.6×10^{-3} and 1.5×10^{-3} for ε_{xx} , ε_{yy} and ε_{zz} , respectively, and shear of 1.8×10^{-3} , 0.5×10^{-3} and 0.8×10^{-3} for ε_{xy} , ε_{yz} and ε_{zx} , respectively.

Figure 4.27 shows the comparison between the results obtained from the analytical model and FEA models plotted for a vertical load of $200\ \mu N$ with the experimental case parameters. Both models provide sensibly similar results in terms of s-shape deformation of the membrane. The directional deformation in Z-direction allows the identification of particular points of interest. The top flat part of the graph with the zero deformation refers to the point of the top of the ridge, while between $0 - 15\ \mu m$, the membrane does not adhere to the substrate. In the middle of the unadhered part, there is a transition point from concave to convex, where the curvature is zero. As the deformation reaches a height of $-1.50\ \mu m$, the membrane is in contact with the substrate which corresponds to the start of the contact length.

The normal and shear strain maps obtained from the FEA simulations are shown in Figure 4.28. The simulations show that the normal strains ε_{xx} and ε_{zz} are the largest. The shear strain is mainly induced in the XZ plane, while the shear strains in the XY and YZ planes are very small. The strain gradient across the YY, XY, and YZ directions is most pronounced at the edges of the membrane. This effect is due to the boundary constraints of the simulation model, where the midpoint cross-section perpendicular to the ridge is fixed, restricting displacement in these directions, particularly in the central region. As a result, the central region experiences less deformation, while the edges, which are less constrained, undergo greater strain. This difference in displacement

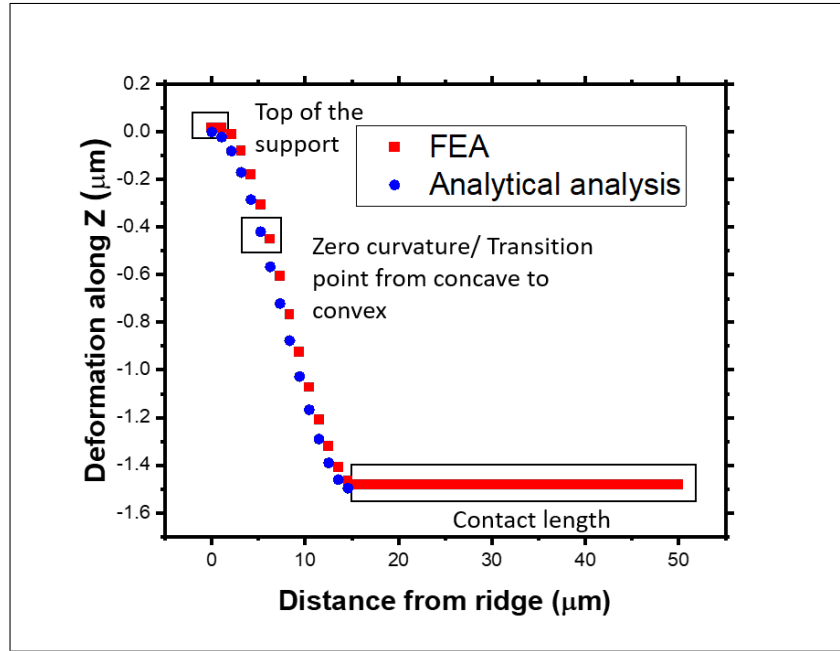


Figure 4.27: Comparison of the mechanical deformation of the membrane obtained from the analytical and FEA models with the experimental dimensions as parameters.

creates a steeper strain gradient near the edges of the membrane. The following section will further analyze the shear strain components, focusing on the middle part of the membrane. By taking line scans from the FEA simulation and the analytical model, each strain component can be plotted as a function of the distance from the support. Figure 4.29 shows the strain value for the ε_{xx} component, which is the dominant one for both models. The values of strain for the analytical model were obtained from Equation 4.10 and 4.11.

It is noticeable that the results from the FEA simulations match very well the predicted values from the analytical formalism. In Figure 4.29, the areas of interest are highlighted. The strain values go from extension to compression, passing through a zero point which indicates this transition. This is also the point where the curvature equals zero as previously described. The zone with a constant strain of zero corresponds to the contact length where there is complete balance between extension and compression.

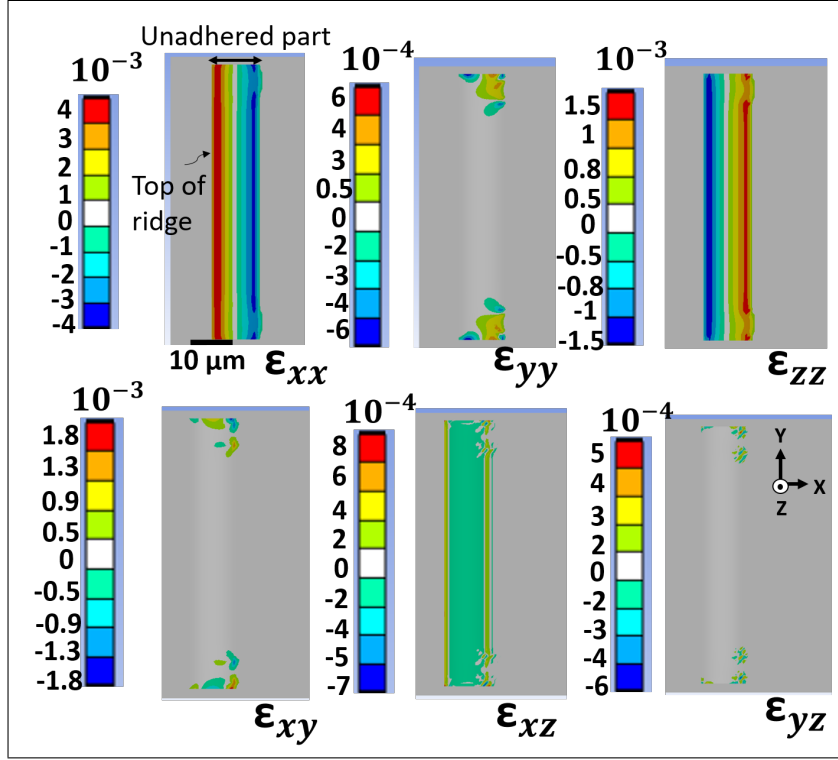


Figure 4.28: Normal (ϵ_{xx} , ϵ_{yy} , ϵ_{zz}) and shear (ϵ_{xy} , ϵ_{xz} , ϵ_{yz}) strain maps obtained from finite element simulations.

4.6 Electron backscatter diffraction measurements

4.6.1 Radius of curvature assessment

In order to study the resultant induced strain on the printed cantilevers, we performed electron backscatter diffraction (EBSD) measurements. EBSD has been utilized in various strain measurement applications, including strained epilayer films on substrates such as Si_{1-x}Gex/Si and ex-situ measurements near micro-hardness indents in silicon [245]. The technique of high-angular resolution EBSD (HR-EBSD) provides the opportunity to simultaneously map lattice rotation and elastic strain gradients with exceptional precision, making it suitable for strain analysis in silicon membranes [246]. Additionally, EBSD cross-correlation techniques have been applied to the strain fields surrounding a wedge indentation in silicon, allowing for the computation of stresses and comparison with those measured using confocal Raman microscopy. Furthermore,

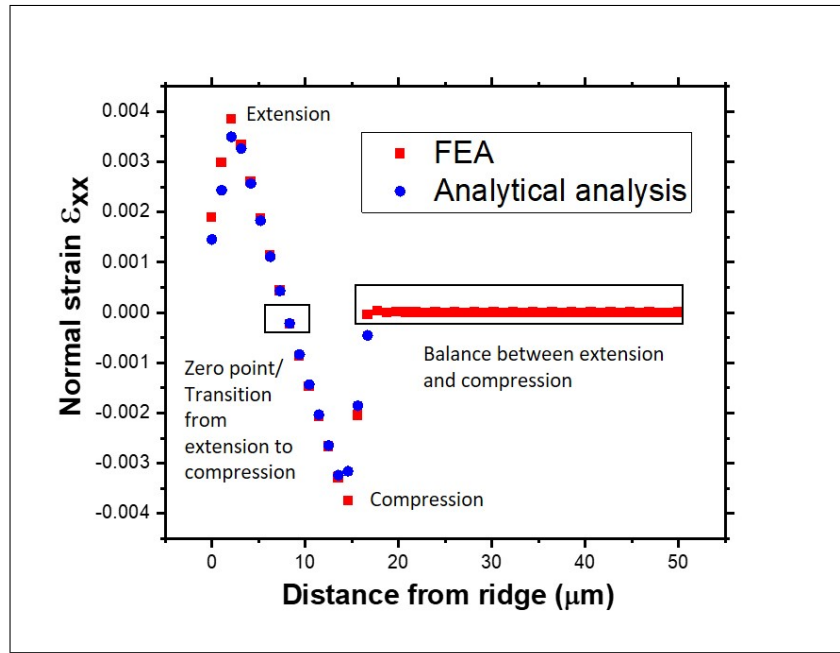


Figure 4.29: Comparison between the normal ϵ_{xx} strain obtained from the simulations and the theoretical model.

EBSD has been used for elastic strain measurements, demonstrating its applicability in strain analysis [247]. The technique of cross-correlation methods applied to high-resolution EBSD patterns obtained from unstrained and strained points on the same planar sample allows for the accurate comparison of crystal lattices to determine lattice strain and rotation, making it suitable for strain analysis in silicon membranes [248].

The EBSD measurements were carried out in a variable pressure field emission gun electron microscope (FEI Quanta 250) using an Oxford Instruments Nordlys EBSD system. After initial indexing (Oxford Instruments Refined Accuracy method), refined orientation information and strain determination was carried out via cross-correlation of the experimental electron backscatter pattern to dynamically simulated patterns [249–251]. Afterwards, the EBSD data was analysed using MTEX, a Matlab-based toolbox [252]. The EBSD data was acquired at a sample tilt of 70° and electron beam voltage of 30 kV; the pattern size was $1344 \times 1024 \text{ px}^2$ and the step size 500 nm.

Figure 4.30a) shows an SEM image of the Si membrane that was investigated using EBSD. The investigated area is delimited by the red rectangle and three example EBSD

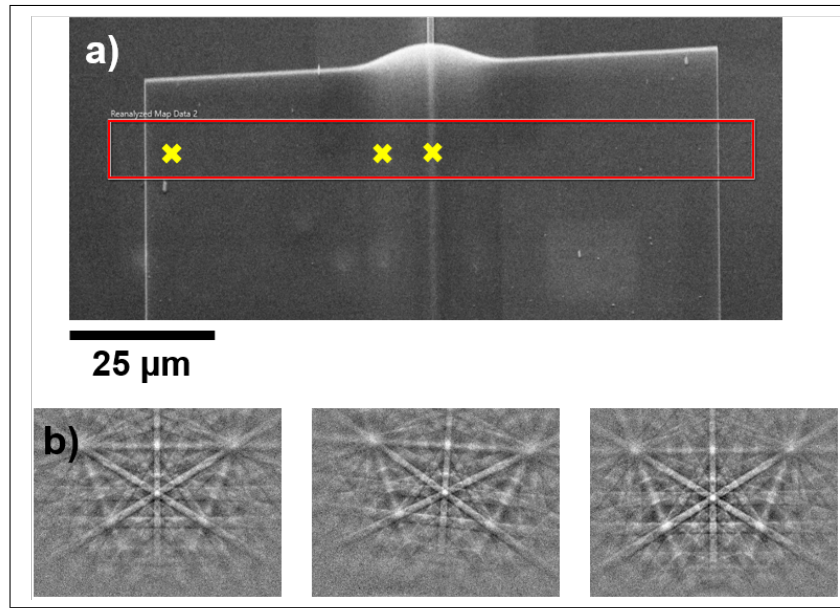


Figure 4.30: a) SEM image of the Si membrane measured using EBSD. The measured area is marked by the box. b) Example electron backscatter patterns acquired from the flat left side of the Si membrane, the side and the top. The spots are marked by the crosses in the SEM image in a).

patterns marked by crosses are shown in Figure 4.30b). The electron backscatter pattern on the sloped side of the membrane (middle) shows considerable rotation compared with the patterns from the flat side (left) and top of the ridge (right). This relates to a change in crystallographic orientation of the Si lattice. The variation of orientation of the crystal lattice of the membrane can be assessed by comparing how much the orientation in each pixel in the dataset deviates from a chosen reference orientation [253]. This is referred to as grain reference orientation deviation (GROD) analysis. In the context of strained materials, GROD provides valuable insights into the local intercrystalline distortions within the grains, which are indicative of the accumulated deformation or strain at a microstructural level [254]. This is particularly relevant for understanding the distribution of misorientation, or stored energy, within the grain, which can be influenced by the angle of curvature in a strained material [255]. The Si membrane is folded over the ridge, which is parallel to the Y axis in our reference in the analysis, the orientation change should be only caused by a rotation around the Y, while rotation around the X and Z axis (GROD_x and GROD_z, respectively) are negligibly (not shown

here). Figure 4.31a) shows the misorientation around the Y axis (GROD_y) for the Si membrane, where the reference orientation is the mean orientation on the flat part of the membrane as marked by the box in the figure. For angle of curvature evaluation, the Grain Reference Orientation (GROD) angle map in y-direction was analyzed. The GROD angle is related to the angle of curvature of a strained material. GROD is a measure of the intragranular misorientation, representing the deviation in orientation of a measurement point from the average orientation of the grain to which the point belongs.

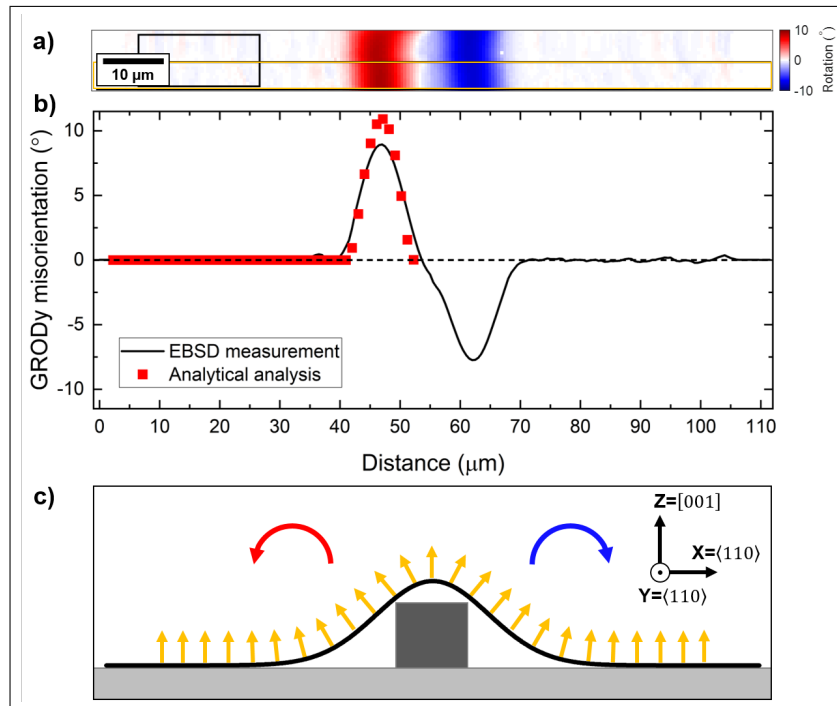


Figure 4.31: a) Misorientation angle around the Y axis (GROD_y). The black box on the left marks the misorientation reference. b) GROD_y line scan across the Si membrane. The line scan is marked by the yellow line in a), and was averaged over several lines. Superimposed is the angle of curvature from the analytical analysis. c) Cross-section schematic of the membrane showing the rotation around the Y axis.

An averaged line scan extracted from the GROD_y map is shown in Figure 4.31b). A symmetrical orientation change is clearly noticeable on either side of the top of the membrane. Due to the symmetrical orientation change around the top of the membrane, the rotation is positive to one side and negative to the side as illustrated in Figure 4.31c).

The maximum misorientation is measured to be about 8-9°. The angle of the membrane curvature as determined from the analytical model using Equation 4.8 is also plotted in Figure 4.31b). It agrees reasonably well with the EBSD measurement although it estimates a maximum misorientation of the membrane of 10.5°. This discrepancy is attributed to the simplifications of the analytical model.

4.6.2 Normal strain assessment

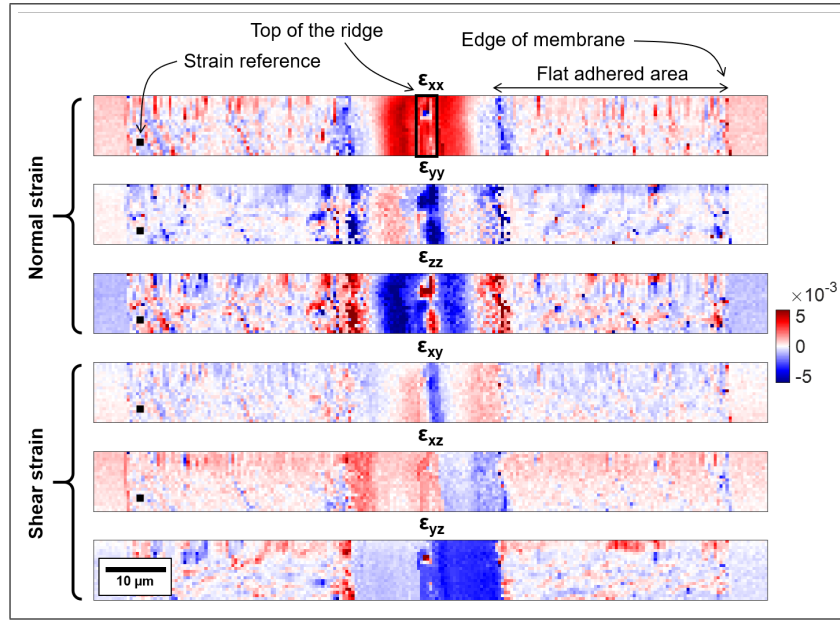


Figure 4.32: Normal (ϵ_{xx} , ϵ_{yy} , ϵ_{zz}) and shear (ϵ_{xy} , ϵ_{xz} , ϵ_{yz}) strain maps obtained from the EBSD measurements. The black pixel on the left marks the strain reference.

The strain maps are also obtained from the EBSD measurements. Figure 4.32 shows the normal and shear strains inferred from the rectangular area marked on the SEM image in Figure 4.30a). The first three colour maps correspond to the normal strain, while the rest three to the shear strain. The colour scale is in the 10^{-3} range, indicating the positive values (tensile strain) with red colour and the negative values (compressive strain) with blue colour. The strain reference that was used is marked with a black square and it is located on the flat part of the membrane. The edge of the membrane is highlighted in the figure for clarity. The graph presents the strain variation across the whole membrane, indicating the higher values of strain-induced in the curved part,

as expected. As seen previously in the FEA model, the dominant strain is present in the ε_{xx} and ε_{zz} components, with values as high as 5×10^{-3} .

An averaged line scan extracted from the normal strain map of the ε_{xx} component in Figure 4.33a) is shown in Figure 4.33b) along with the equivalent data as estimated with the analytical and FEA models. The predicted values in both model correspond reasonably well with the EBSD measurement. From the top down it shows an extension (tensile strain) passing through a transition point to a region of contraction where the membrane is compressed before approaching zero at the contact area. The measured values are slightly less symmetrical around the transition point. Effectively, the Si membrane around the top ridge area is not perfectly flat and this curvature deviates from the assumption taken in both models of a perfect contact with the ridge. Finally, in the experimental case, the sides of the membrane may not be perfectly parallel to the ridge which will skew the strain line scan. An offset of the actual value which is in the order of ± 0.001 , can be explained by the ideal cases of the simulated model as well as from the fact that the width of the support slightly changes in each case, which can contribute to the final strain values. Also, in the model we assume that the initial strain of the silicon membrane is zero. However, there is maybe residual strain present in the membrane due to fabrication processes as well as the printing process.

4.7 Strain influence on Silicon bandgap

The bandgap of silicon is significantly influenced by strain, as evidenced by various studies [256], [257], [258]. In silicon, the bandgap energy decreases as the material is subjected to tensile strain and increases under compressive strain [259]. In silicon, the relationship between strain and bandgap can be described by the equation: $\delta E_g = \alpha \epsilon$ where δE_g is the change in bandgap energy, α is the strain bandgap tuning coefficient which is a parameter used to describe the effect of strain on the bandgap of a material [260], and ϵ is the applied strain [261]. This equation shows that the bandgap energy of silicon can be modulated by applying strain to the material. When strain is applied to silicon, it causes a change in the bandgap energy, which can have significant implications for the electronic properties of the material [262]. Experimental studies have reported

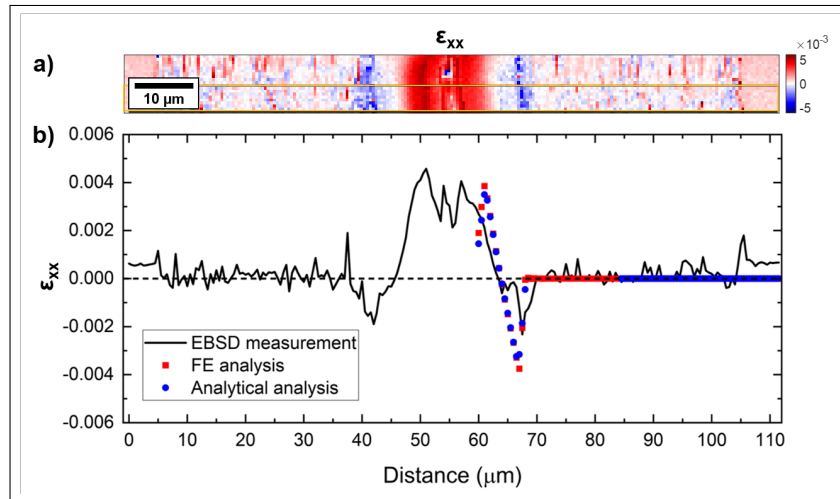


Figure 4.33: (a) ϵ_{xx} normal strain map obtained from the EBSD measurement. (b) Linescan of the ϵ_{xx} component across the Si membrane. The linescan is marked by the yellow box in (a), and was averaged over several lines. Superimposed are the ϵ_{xx} values from the FE and analytical analysis.

that a uniaxial strain of 1.8% can induce shrinkage in the indirect bandgap of silicon by approximately 0.3 eV. Transfer printing of silicon membranes on top of a ridge or equivalent waveguide demonstrates that a strain of about 0.4% can be induced. By comparing this value with the literature, we find that it is within a region that can significantly change significantly the band gap of silicon by a value as high as 0.10 eV [263]. From the linear relation between strain and bandgap energy, the value of α for strain can be approximate with 0.16 eV/strain.

By applying strain to these materials, researchers can effectively tune their bandgaps, which is essential for various applications in optoelectronics, photovoltaics, and other fields [264]. The strain bandgap tuning coefficient provides a quantitative measure of how much the bandgap changes in response to applied strain [265].

4.8 Chapter Summary

In this chapter, it was shown that a strain modification can be induced on a silicon membrane by physically bending it through a transfer printing process over features present on the target substrate. The incurred deformation remains once the external

force applied during the transfer is removed. Further analysis was performed analyzing the deformation over time and finding the separation gap between the membrane and substrate in the unadhered area from the optical fringes. We performed analytical and FEA simulations of the mechanical deformation and compared the results obtained in both models to experimental values taken from an EBSD measurement. The crystal orientation changes reflecting the conforming behavior of the printed membrane and normal strain was assessed at 0.4% in the measurement and with the models. This strain correspond to a band gap change of 0.10 eV . This printing method can be employed to locally modify the properties and the functionality of silicon based photonic devices in a heterogeneous integration paradigm.

Chapter 5

Conclusion and Future work

This chapter summarizes the key research achievements presented in each preceding chapter and provides a brief overview of future research goals for each specific focus area. The primary motivation for this research was to develop a new transfer printing method aimed at producing heterogeneous integrated devices on a large scale, with a particular emphasis on microLED displays. The chapter evaluates this methods' achievements in terms of individual accuracy and overall yield. By highlighting the research outcomes and outlining future goals, this chapter emphasizes the significant progress made and the necessary steps to further enhance this transfer printing technique.

5.1 Fabrication of large membrane device arrays and roll-transfer printing

This chapter introduces a novel transfer printing method based on continuous roll-transfer printing, providing a detailed explanation of both the mechanical setup and the physical mechanisms involved. The continuous nature of the roller setup enables the mass transfer of thousands of devices in less than 30 seconds without the need to disengage the roller. The importance of the roller surface is demonstrated through experimental tests with three rollers of varying roughness—high, medium, and low. Results show that using the roller with the lowest roughness ($0.3\ \mu m$) yields optimal results, given the micrometer size of the devices.

The chapter also addresses fabrication challenges that can affect the roll-printing process, such as issues with anchor design. These challenges are thoroughly analyzed, discussing how they influence the overall yield and quality of the fabricated arrays. Proposed solutions include three different anchor shapes positioned in the middle of the device, studied in various sizes. Additionally, the orientation of the roll-printing in relation to the anchor positions was examined, emphasizing the importance of positioning the roller parallel to the anchors. This method represents a significant advancement over traditional techniques, offering potential improvements in scalability and precision.

Furthermore, the chapter highlights the integration of this novel transfer printing method with existing fabrication workflows and explores its potential applications in various industries such as microLED displays, flexible electronics, and bio-integrated devices.

The chapter concludes by emphasizing the critical importance of fabrication yield in the roll-transfer printing process. It underscores the need for ongoing research and optimization to address the identified challenges, improve process reliability, and enhance the overall efficiency and success of the roll-transfer printing method. The insights and advancements discussed are crucial for the continued development and commercialization of high-yield, large-scale membrane device fabrication.

5.2 Automated inspection method for large array devices and analysis

Chapter 3 discussed the significance of high-speed automated inspection methods in volume manufacturing. A new automated sub-micron inspection method was developed to evaluate the continuous roll-transfer printing process in terms of positional accuracy, rotation, and yield.

This method consists of two main parts: high-resolution microscopy and image processing and analysis. The first part involves using a high magnification (50X) lens to capture high-resolution images, a nanometer precision translation stage that moves in the x and y directions, and a coding system that controls image capturing, stage

translation, and image stitching to form one high-resolution image at a centimeter scale. The second part focuses on processing and analyzing this high-resolution image to determine the position and rotation of each device. By leveraging the array format known from the photolithography mask, the code can also detect any missing devices. This recognition method is based on cross-correlation, where a template of the same size and shape is scanned across the entire image. The maximum correlation values indicate the center of each device, marked with a red dot and a missing device, marked with a white cross.

The chapter then utilized this inspection method to analyze both an as-fabricated donor chip for validation and the resultant roll-printed arrays. The analysis of the as-fabricated chip showed a measurement performance limit, with a standard deviation of the pixel pitch error at 830 nm . For the roll-printed mini-LED array, consisting of 4,000 pixels, the mean pitch error was 26 nm with a standard deviation of $1.43\text{ }\mu\text{m}$. The fully transferred QVGA array, containing over 75,000 devices, showed a mean pitch error of 430 nm and a standard deviation of 980 nm . The full array yield was 95% for miniLEDs and 98% for microLEDs, with spatial dependence indicating that most of the chip area had a yield over 99.9%, while defects were concentrated in small areas where donor chip processing failed. The work on this chapter highlights the potential for large-scale hybrid material device integration, compatible with established industrial foundry manufacturing processes and semiconductor infrastructure. By addressing both accuracy and yield, this chapter underscores the advancements and practical applications of high-speed automated inspection in ensuring the quality and reliability of roll-transfer printed arrays. Solutions and optimizations, including improvements in algorithm efficiency, enhanced imaging techniques, and refined mechanical controls, can be applied and further experiments can be done in order to test how the method can be adapted for various applications.

5.3 Mechanical deformation of thin film silicon

In Chapter 4, the significance of heterogeneous integration in strain engineering was discussed, with a particular focus on silicon and the impact of strain on its electrical

and optical properties. It was demonstrated that strain modification can be induced in a silicon membrane by physically bending it through a transfer printing process over features present on the target substrate. This process causes the printed membrane to conform on top of ridges, creating an s-shaped deformation that was analyzed both analytically and theoretically.

The relationship between this deformation and the resulting strain was explored, highlighting how the curvature in the unadhered sections influences the induced strain. Notably, this deformation persists once the external force applied during the transfer is removed. Further analysis involved examining the deformation over time and determining the separation gap between the membrane and substrate in the unadhered area using optical fringes.

Analytical methods and Finite Element Analysis (FEA) simulations of the mechanical deformation were performed and compared with experimental values obtained from Electron Backscatter Diffraction (EBSD) measurements. These comparisons revealed changes in crystal orientation, reflecting the conforming behavior of the printed membrane. Normal strain was assessed at 0.4% in both the measurements and the models, corresponding to a band gap change of 0.10 eV.

This printing method can be employed to locally modify the properties and functionality of silicon-based photonic devices within a heterogeneous integration paradigm. By leveraging this approach, specific areas of silicon devices can be tailored to enhance performance, offering a promising route for advanced photonic applications.

5.4 Future work

5.4.1 Further analysis and characterization of the continuous roll-transfer printing method.

In this thesis, a new transfer printing method based on continuous roll transfer printing was presented for the mass transfer of optoelectronic devices. The method was characterized in terms of accuracy and yield by analyzing the roll-printing of an entire QVGA device. To build this system, several parametric studies were conducted to determine

the optimal parameters for uniform printing of large arrays of devices. Specifically, the speed of the translation stage, the roller head, the direction of printing, and the design of the device anchors were studied in detail to understand their effects on the printing process.

However, further characterizations could enhance the understanding of the process. Firstly, proper pressure measurements could quantify the pressure used during the roll process. This can be achieved either by applying a load cell to the mounted part of the roller head or by using pressure-sensitive paper on the stage during the rolling process. Pressure analysis will provide evidence of uniform pressure application throughout the process and offer insights into the alignment of the roller with respect to the substrates. For instance, if the pressure on one side of the roller is higher than on the other, it indicates a misalignment across the y-axis of the roller.

Another important analysis involves checking the rotational speed of the roller under different speeds and applied pressures. This can be accomplished using a high-accuracy (0.05 rpm) tachometer, ideally a non-contact type to avoid affecting the rolling process. This analysis will reveal how the rotational speed is influenced by pressure and the resulting friction from the sides and the stage

5.4.2 Continuous roll transfer printing for functional devices

Based on the work presented in this thesis, the future prospects for continuous roll transfer printing are promising and should be further explored. The immediate next step is to fabricate microLED devices using the process detailed in Chapter 2, including the p and n contacts. Utilizing roll transfer printing, the entire array of pixels can be printed onto a wide range of materials receiver substrate. Post-printing fabrication will involve depositing metal tracks to create an addressing scheme for controlling each microLED's functionality.

Characterisation of the microLEDs should be conducted in terms of their electrical, thermal, and optical properties. I-V and L-I measurements, along with thermal analysis (both imaging and temperature measurement), should be performed on the microLEDs in both continuous and pulsed-mode operations. In this way, it will be

ensured quantitatively that the roll-transfer printing process does not affect any of the properties of the microLEDs.

5.4.3 Continuous roll-transfer printing for colourful displays

Building a full colour display using continuous roll-transfer printing will require repeating the roll process described in this work three times, once for each color pixel (red, blue, and green) from its respective substrate. These color pixels will then be integrated onto the same platform with $1\ \mu m$ accuracy. While the placement accuracy of the roller has been tested in this work, the overlay accuracy requires further investigation.

An automated and precise alignment method needs to be implemented to achieve chip-to-chip accuracy in a continuous process involving four wafers in total (three for the colors and one for the final receiver). Pre-alignment must be performed in advance for all four wafer rolls since the continuous process does not allow for individual alignment of each chip.

The system described in Chapter 3 could be further improved and integrated into the roller setup, allowing for analysis to be conducted within the same setup without needing to move the sample to another machine. The same analysis method can be adjusted for real-time overlay alignment of the colorful arrays. This will require advanced coding to implement the cross-correlation method for overlay printing accuracy. An automated mounted system could be used to scan the four chips in a row, ensuring the positional alignment of all arrays. Additionally, a longer travel linear stage, with a minimum travel length of $600\ mm$, is needed to facilitate the continuous rolling across all the chips.

5.4.4 Continuous roll-transfer printing for large scale integration

The continuous roll-transfer printing method detailed in this thesis is particularly well-suited for large-scale applications due to its ability to produce high-quality, uniform thin films over extensive areas efficiently and cost-effectively. Although this thesis focuses on its application in microLED displays, the technique is not limited to these devices. It can be broadly applied to any manufacturing process requiring large-scale

heterogeneous integration. One significant application is in wearable devices. The market for wearable electronics is vast and growing, with millions of units produced annually. Roll-transfer printing allows for the mass production of the flexible electronic components needed in these devices. Additionally, with the rising demand for foldable and rollable displays in consumer electronics, such as smartphones, tablets, and TVs, roll-transfer printing supports large-area production, meeting the high-volume requirements of the display industry. Another key application is in thin-film transistor (TFT) arrays, which are used in various products, including displays and sensors. Producing these arrays on a large scale is essential to meet the demands of consumer electronics, automotive displays, and more. Furthermore, the need for large-area electronic products, such as digital signage, electronic billboards, and industrial sensors, necessitates scalable manufacturing processes like roll-transfer printing. Moreover, the global push for renewable energy has significantly increased the demand for solar cells. In the concentrated photovoltaics (CPV) industry, there is a general trend toward handling smaller solar cell across larger areas. Roll-transfer printing enables the production of flexible and lightweight solar panels, suitable for deployment on a large scale, from residential rooftops to expansive solar farms. By facilitating the efficient production of high-performance solar cells, this technology supports the scaling up of solar energy solutions to meet global energy needs.

Also, healthcare and environmental monitoring industries require large quantities of sensors for widespread use. Roll transfer printing allows for the mass production of flexible biosensors and environmental sensors, ensuring availability for broad deployment. For implantable devices, the medical field requires large-scale production of biocompatible electronic devices for widespread healthcare applications, such as monitoring implants and therapeutic devices. For monitoring air and water quality on a large scale, vast numbers of sensors are needed. Applications in water purification and gas separation require large-scale deployment of high-precision membranes. Roll transfer printing facilitates the production of these membranes on a scale sufficient to meet industrial and environmental needs. Also, the healthcare industry demands large quantities of microfluidic devices for diagnostics and lab-on-a-chip applications. Roll

transfer printing enables their large-scale production. Another application can be for the large area integration of nanowires, targeting applications like sensors, photodetectors and photovoltaics.

This scalability is crucial for industries like consumer electronics, renewable energy, healthcare, and environmental monitoring, where demand for large volumes of advanced electronic components and systems is high.

5.4.5 Applications on strain engineering of silicon

In Chapter 4, the influence of strain in silicon membranes by physical bending was studied. It was demonstrated that a strain of 0.4% occurred in a 220 *nm* thick silicon membrane when transfer printed onto ridges with a height of 1.50 μm . We illustrated how this strain correlates with the resulting deformation of the conforming membrane over the ridge, which is influenced by the support height, material properties, and membrane thickness.

Future research could involve varying the thickness or height of the support to determine the maximum strain achievable according to the model. Additionally, testing the maximum height that the bonding force between the membrane and substrate can sustain before returning to its original undeformed state would be beneficial.

Further steps include implementing this method in practical optical devices and conducting characterization studies. For instance, transferring the membranes onto interferometric arms in optical devices for applications such as optical switching and refractive index modulation could be explored. The method proposed here offers an alternative approach to strain engineering in silicon, potentially enhancing its nonlinear electro-optic effects and advancing the use of active silicon-based photonics.

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Appendix A

Appendix A

A.1 Ansys mechanical structural Analysis

A.1.1 Ansys Workbench environment and Ansys Mechanical module.

To conduct an analysis using Ansys, the Workbench environment was utilized, which offers a seamless workflow for creating and managing systems. The process begins by selecting a system from the Toolbox and adding it to the Project Schematic. Then, the process progresses through the system's cells, typically in a top-to-bottom manner, completing all the necessary steps for the analysis. Ansys Workbench is a comprehensive simulation platform that integrates various Ansys tools to provide a unified environment for performing engineering simulations. It offers a wide range of capabilities for structural, thermal, fluid, and electromagnetic analyses, as well as multiphysics simulations and optimization studies.

The platform enables users to create and manipulate geometry, define material properties, apply boundary conditions, and set up simulation scenarios. Ansys Workbench supports finite element analysis (FEA) and finite volume analysis, allowing for the accurate prediction of structural and fluid behavior. It also facilitates the setup of parametric studies and optimization processes, enabling users to explore design alternatives and improve engineering performance.

For this study, static structural analysis was employed. A screenshot of the Ansys workbench static structural analysis can be seen in Figure A.1 (a). This particular

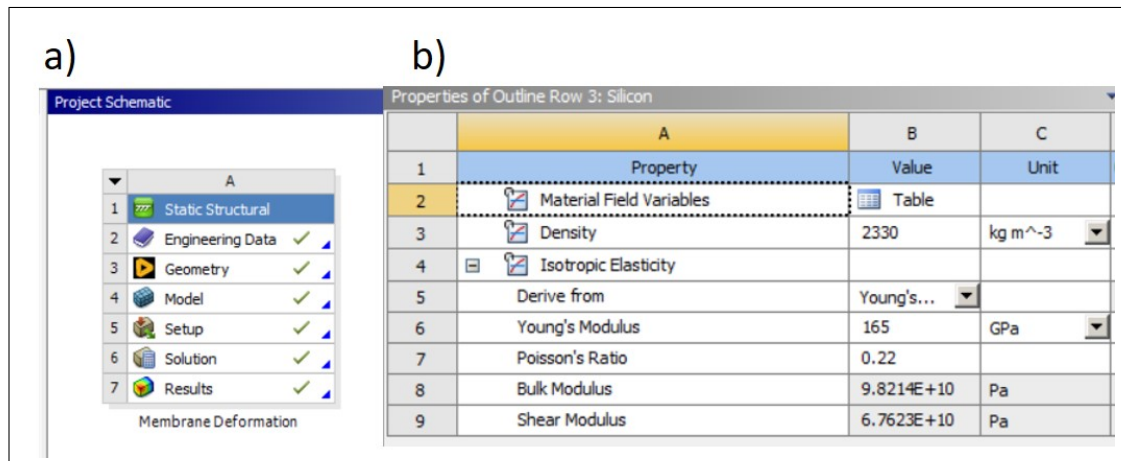


Figure A.1: a) Ansys Mechanical Workbench and b) engineering data set for silicon.

system within Ansys is responsible for evaluating displacements, stresses, strains, and forces in structures or components subjected to loads that do not generate significant inertia or damping effects. It assumes steady loading and response conditions, considering that both the loads and the structure's response change gradually over time.

In general, to work through a Static Structural system, the following steps need to be followed:

Pre-processing

Pre-processing comprises several essential steps that prepare the model for analysis. In this phase, we define the model's geometry, materials, and boundary conditions. An important aspect of pre-processing is the accurate definition of engineering data, as the response to applied loads varies based on material properties. Defining the materials used in the simulation involves specifying significant material properties, such as elastic modulus, Poisson's ratio, densities, and thermal coefficients for different parts of the model. In this study, silicon is used as material, which has the following properties: a density (ρ) of 2330 kg/m^3 , isotropic elasticity with a Young's modulus of 165 GPa , a Poisson's ratio of 0.22, a bulk modulus of $9.82 \times 10^{10} \text{ Pa}$, and a shear modulus of $6.76 \times 10^{10} \text{ Pa}$. These properties are added on the engineering data section, as it can be seen in Figure A.1 b).

Geometry Creation and Import

In this section, the geometric model of the structure to be analysed is created or imported using Ansys DesignModeler or other compatible CAD software. In this study, Ansys Design-Modeler is used for designing all the models. The process begins by defining the coordinate system and the desired plane for creating a 2D sketch of the geometry. Once this is established, a 3D body is generated by extruding the planar design in a specific direction. In this case, the xy plane is selected for the sketch and extruded it in the z-direction, allowing to define the length, width, and thickness of the different bodies. Each body is created as an individual component within the same system, consisting of the support (with height variations in different simulations), the substrate, and the cantilever (with consistent dimensions across all simulations). Finally, the geometry is carefully inspected to ensure cleanliness and suitability for analysis, making any necessary modifications or repairs as needed. Figure A.2 shows the final designed model.

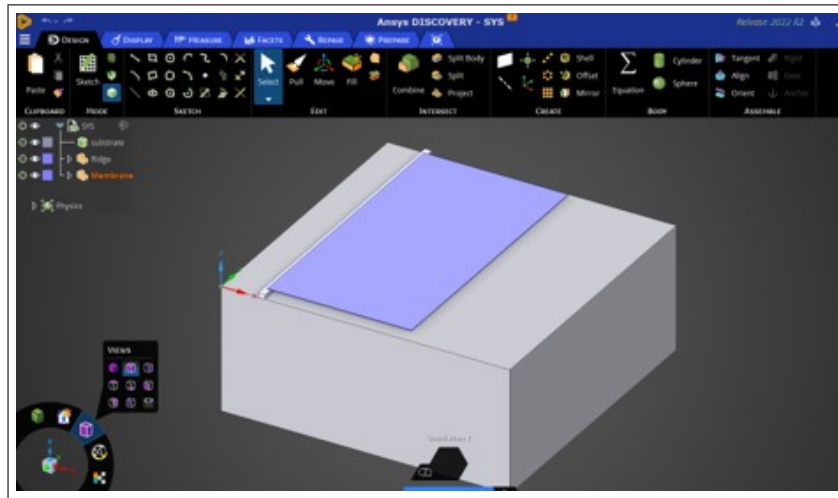


Figure A.2: Ansys DesignModeler for geometry import

Meshing

To apply FEM, the system's geometry is transformed into a mesh consisting of elements. These elements are defined by nodes, which represent spatial coordinates and vary

based on the element type used. The meshing process converts irregular shapes into recognizable volumes known as elements, facilitating analysis within the FEM solver. In this specific analysis, a mesh is generated that discretizes the structure into finite elements. The mesh density is determined by balancing the desired accuracy level and the geometric complexity of the system. For this case, the ridge and substrate primarily serve as boundary conditions and have an element size set to 10^{-5} m. Conversely, the cantilever, which is of greater interest for internal analysis, is meshed with smaller elements, specifically one order of magnitude smaller, at 10^{-6} m. This finer mesh resolution is also applied to the contact regions, as their behavior plays a critical role in the model.

Application of Boundary Conditions

Once the materials, geometry, and meshing are established, the subsequent step involves applying boundary conditions to the model. These boundary conditions encompass constraints, loads, supports, and other necessary conditions required to simulate the real-world behavior of the structure. Boundary conditions are crucial in Ansys structural mechanical analysis as they play a significant role in determining the behavior of the structure under various loads and constraints. The application of boundary conditions in Ansys is essential for regularizing parameter identification problems based on full-field measurements [266]. By assigning appropriate boundary conditions and material properties to the model, the behavior of the structure under specific loads can be accurately reconstructed [267]. The application of boundary conditions significantly impacts the behavior of beams under various loads. For instance, this work [268] highlighted that boundary conditions have a strong impact on the trajectory of beams, leading to increased acceleration during propagation and even causing beam bending in a direction opposite to the initial trajectory.

Additionally, another recent work demonstrated that the resolving equation in the problem of accounting for additional shear in beam bending introduces particular aspects when boundary conditions are considered [269], as well as the importance of studying the effects of changing boundary conditions, such as the support type of the

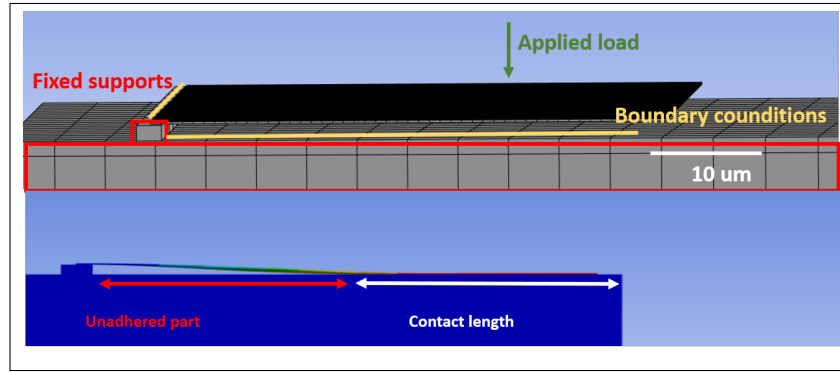


Figure A.3: Ansys model for the deformed membrane. a) Initial state of the model, highlighting the fixed supports (ridge and substrate) the applied downwards force (z direction) and b) resulted shape after the simulation (s-shape deformation)

beam, on the deflection response under load [270], [271]. This underscores the significance of considering different boundary conditions in Ansys structural mechanical simulations to accurately capture the behavior of bending beams.

In this study, the ridge and substrate are designated as fixed supports, indicating that they remain unaffected by any deformation, displacement, rotation, or physical changes when subjected to loads. The connections between the three distinct rigid bodies in the system are as follows. Firstly, the edge of the cantilever is positioned and fixed at the top of the ridge. This region remains in constant contact, resembling the behavior of a conventional fixed-supported cantilever beam. Secondly, the ridge is bonded to the top surface of the substrate, disallowing any movement or separation between them. Lastly, a constraint condition is implemented between the cantilever and the substrate. Initially, the cantilever does not come into contact with the substrate. However, under load application, the two bodies make contact and remain bonded, preventing penetration or sliding. This configuration gives rise to the s-shaped cantilever, commonly referred to as the "one supported adhered cantilever." In the Ansys software, the first two conditions are implemented as "bonded type" contact, while the last one is categorized as "rough type" contact. Prior to proceeding, it is important to conduct a final check to ensure that the applied boundary conditions align with the expected physical behavior of the structure and the objectives of the analysis. The bonding of the membrane to the substrate was modelled as a distributed vertical force acting on

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the membrane, which could be varied as a parameter. This is a simple way to model the adhesion force between the surface of the membrane and the substrate, which can then be compared with the experimental results through the measured contact length L of the two surfaces, shown in the schematic of Figure A.3.

Solution

Post-processing is the final step in the structural analysis process, involving the examination and interpretation of the obtained results. During this phase, the evaluation of various outcomes such as stress, strain, displacement, and deformation is occurred. Particular attention has to be paid to critical areas or regions of interest to assess the structural behaviour and identify potential failure modes. Additionally, a comparison between the results against relevant design criteria or standards is essential to validate the structural integrity and ensure safety. Post-processing in Ansys software involves the analysis and visualization of simulation results to extract meaningful engineering insights. It encompasses various activities such as stress analysis, flow visualization, and result interpretation. The post-processing stage is crucial for understanding the behavior of the simulated system and making informed engineering decisions. Various works have highlighted the use of Ansys Mechanical for stress, strain and other relevant curves estimation across the thickness of materials, emphasizing the role of postprocessing in stress analysis [272], [273].

A.2 EBSD results for $h=1.15 \mu m$

The same EBSD measurement and analysis was conducted on the printed membrane on top of the ridge of $h=1.15 \mu m$ as well, for comparison and validation. Figure A.4 shows the SE image of the membrane, highlighting the area that the analysis was conducted with the red rectangle. In this case, the entire image was scanned and that led to some changes in the results, which are going to be explained at the end of this section. Similar to the previous case, the resulted normal and shear strain maps are presented in Figure A.5 The size of the maps is different from the previous, as the scanning length

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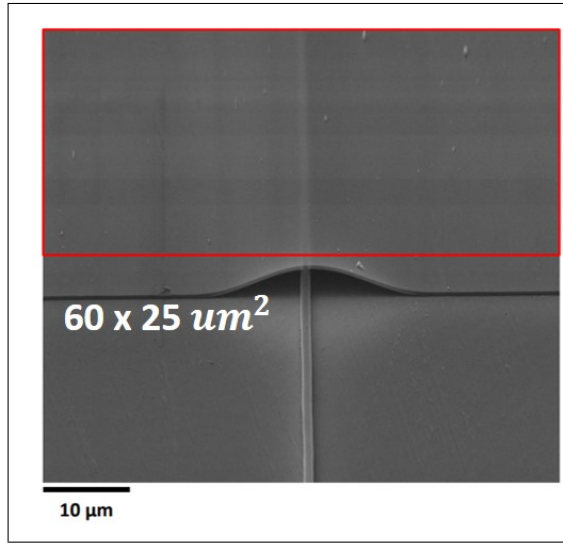


Figure A.4: SE image of the printed membrane on top of the ridge with $h=1.15 \mu m$, indicating the scanning area.

is not the same. The colour scale is again in the 10^{-3} range, indicating the positive values (tensile strain) with red colour and the negative values (compressive strain) with blue colour.

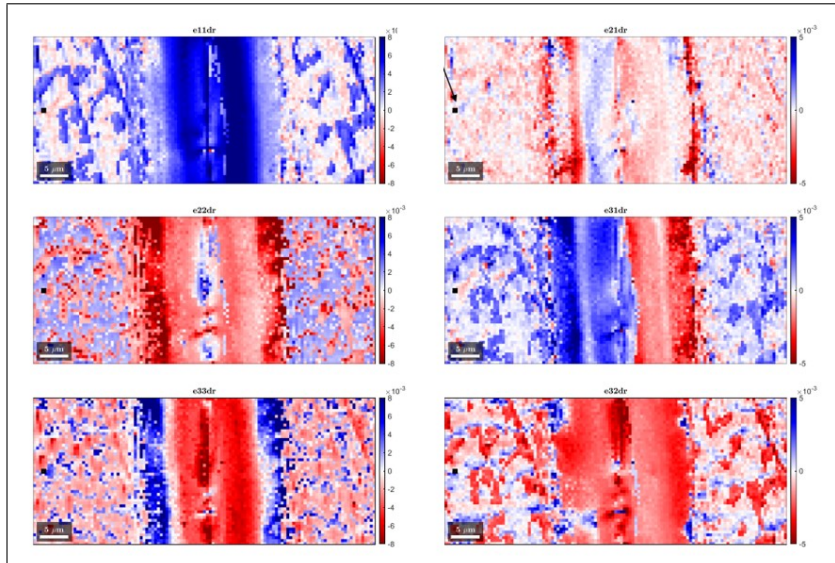


Figure A.5: Normal (ϵ_{xx} , ϵ_{yy} , ϵ_{zz}) and shear (ϵ_{xy} , ϵ_{xz} , ϵ_{yz}) strain maps obtained from finite element simulations.

In this case, the strain reference that was used is located on top of the ridge, rather

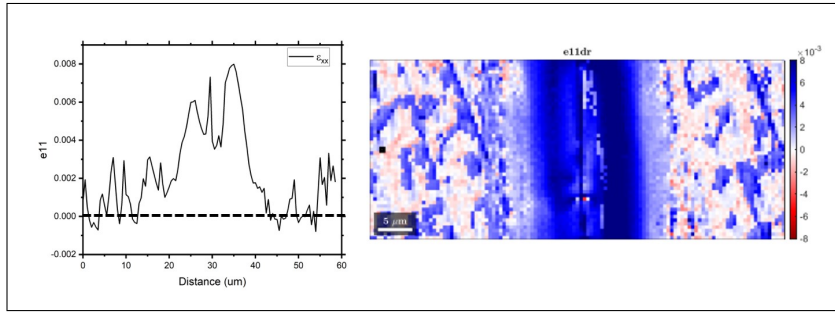


Figure A.6: Normal strain of the dominant direction x. Strain colour map and middle line scan graph

than the flat part of the membrane. From the maps, it can be seen that there is normal strain induced in the dominant x direction, as expected which is in the order of 8×10^{-3} . In order to quantify in detail this result, a linescan was performed at the middle section of the map which can be seen in Figure A.6. The graph presents the strain variation across the whole membrane, indicating the higher values of strain-induced in the curved part, as expected. In this graph, it can be noticed that there is strain induced in the flat part of the membrane as well. That could be explain by two main reasons. The one is that the values are shifted to the reference point that was selected in this case. Theoretically, the expectation was that the strain on top of the ridge is zero, however, in reality the membrane is not bonded on top of the ridge so there is some strain induced there as well. The other reason is that there should be some residual strain in the membrane due to the printing or due to the fabrication steps.

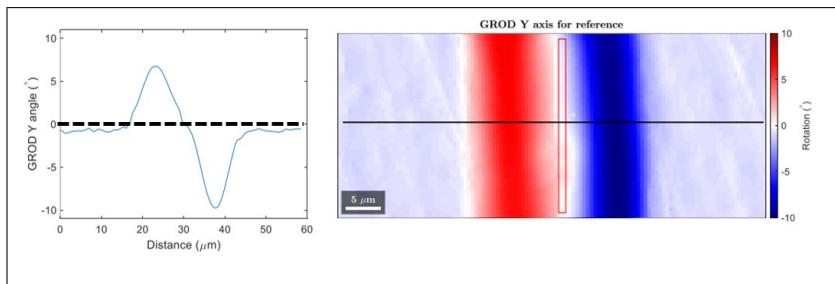


Figure A.7: GRODy misorientation angle. Colour map illustration and middle line scan graph.

Figure A.7 presents the misorientation angle around the Y axis (GRODy) and the linescan across the middle of the Si membrane. The results of this graph verify the

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strain line scan, as there is some rotation in the flat area presented as well.

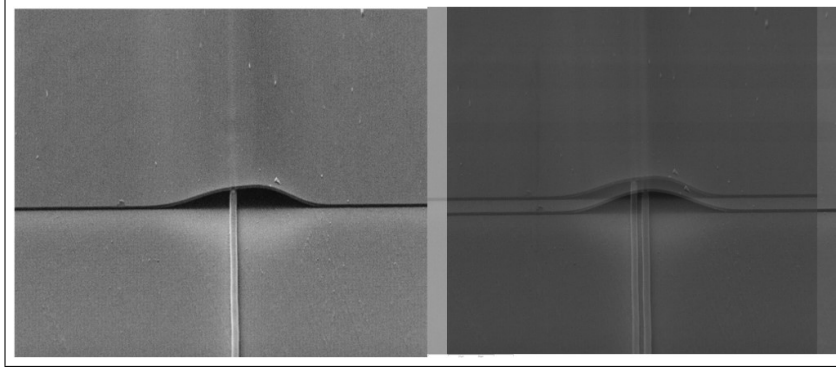


Figure A.8: SE images of the printed membrane on top of the ridge. a) Initial deformation before the scanning and b) overlap images of the initial and the after scan image showing the shifting of the membrane.

After performing the scan, a change in the slope of the deformed part was observed as it can be seen in Figure A.8. The slope is not symmetric around the ridge and a shift located on the right part of the membrane is noticed. At the beginning of this paragraph, the different scanning area was mentioned. As the scanning area is larger than the previous case, the time needed for the scan was longer and thus the gun was pointed on the membrane for longer. That is the reason that this shift is observed and that can explain the asymmetry in the line scan results.

A.3 Additional graphs from simulations

The behavior of the cantilever was studied under variable loads in the order of μN acting downwards in the z direction. The dimensions of the cantilever are $100 \times 100 \mu m^2$ and thickness $220 nm$, which are typical dimensions used in silicon photonic devices. Figure A.9 and A.10 show the resulted shape of the cantilever after the simulation for $h=1.15$ and $h=1.50 \mu m$, respectively, and Figure A.11 shows the top surface sampling of strain across one side of the membrane from ridge to contact area. This will give the following strain components, as it can be seen on the element in Figure A.11. Different heights of the support were used in micrometer scale to study if there

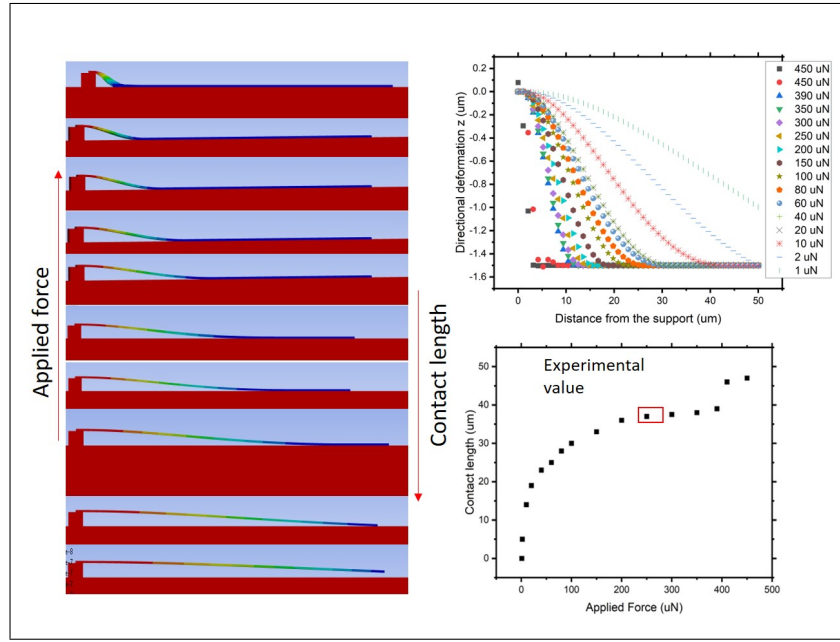


Figure A.9: Summary representation of the resulted deformed shape as we increase the applied force and the relation between the shape and the contact length for the model with height ridge $h=1.15 \mu m$. Imaging illustration and graphs of the directional deformation (z-direction) with the distance from the support for different forces in the μN scale and contact length as a relation with Applied force

is any effect on the resulting strain. It was noticed that under these different values, the curvature and the s-shape of the cantilever beam changed significantly, contributing to normal (e_{11} and e_{33} direction) and shear strains in the model (e_{12} direction). Figure A.9 and A.10 show the simulated resulted deformation of the membrane when we increase the magnitude of the force within the range of 10's micro-Newtons. It was noticed that the shape, including the curvature, the contact length and the unadhered part, changes as we increase the height. The curved part is the one that gives us the information of the internal strain so the resulted shape is important to determine the final value.

Figure A.12 shows the maximum values of shear and normal strains for each shape in the model, showing that indeed there is a strain variation which is strongly related to the contact length and subsequently to the final shape.

By comparing the results from the simulations and the experiments, it was found that the actual shape that is given by the following graphs in Figure A.13 a) resulting

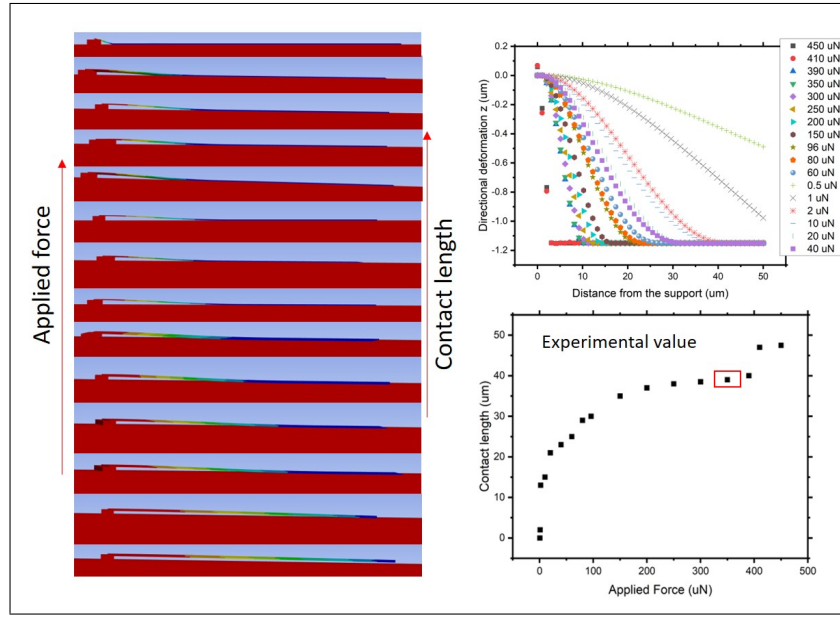


Figure A.10: Summary representation of the resulted deformed shape as we increase the applied force and the relation between the shape and the contact length for the model with height ridge $h=1.50 \mu m$. Imaging illustration and graphs of the directional deformation (z-direction) with the distance from the support for different forces in the uN scale and contact length as a relation with Applied force

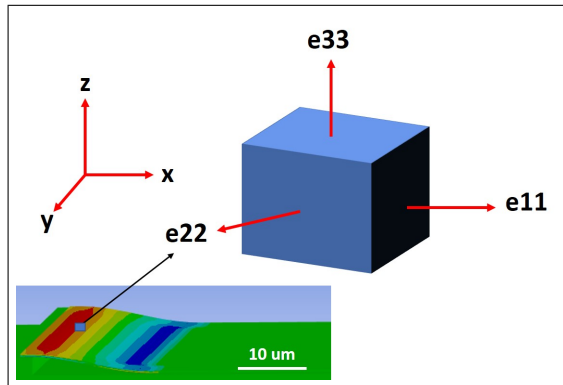


Figure A.11: Strain components of the deformed membrane with respect to the reference system for both cases.

in a contact length of $39 \mu m$ for $h=1.15 \mu m$ and $35 \mu m$ for $h=1.50 \mu m$. The contact length is calculated by using standard optical images and image processing. In Figure A.13 b) the optical fringes correspond to the curved part of the membrane, indicating that there is a gap between the membrane and the substrate.

Figure A.14 shows the simulations results for the case that matches the experimen-

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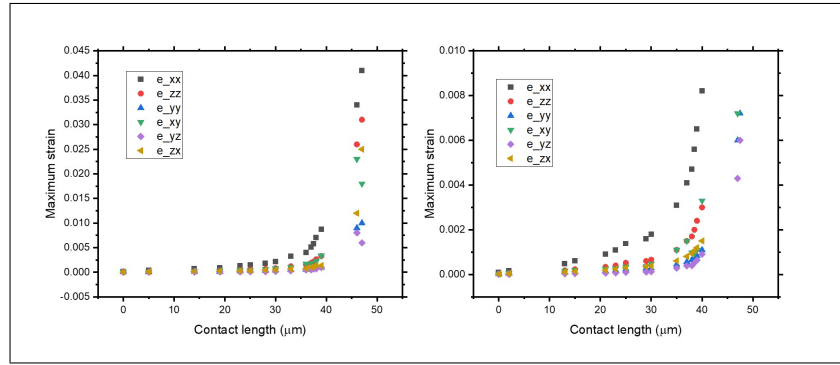


Figure A.12: Graph of the maximum normal and shear strain with the contact length with an inset for better illustration. Top images: for $h = 1.50 \mu m$ and bottom: for $h = 1.15 \mu m$

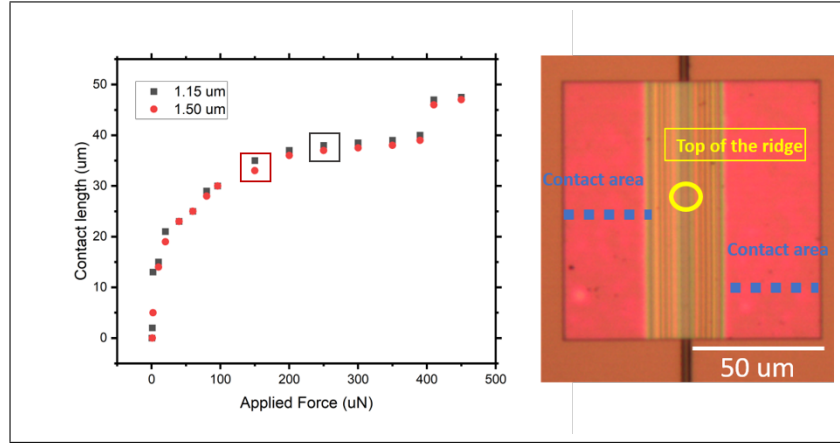


Figure A.13: a) Graph of the contact length with the applied force and the match of the experimental value for $h = 1.15 \mu m$ (grey square) and for $h = 1.50 \mu m$ (red square) and b) 50x optical microscope image of the printed membrane, highlighting areas of interest

tal results for $h = 1.15 \mu m$ and $h = 1.50 \mu m$, respectively. By plotting the directional deformation in z-direction, the points of interest in the model can be spotted. The top flat part of the graph with the zero deformation refers to the point of the top of the ridge. while between $0-11 \mu m$ and $0-15 \mu m$, respectively, it is the unadhered part, similar to the one calculated from the optical images. In the middle of the unadhered part, is the transition point from concave to convex, where the curvature is 0. The directional deformation in x-direction shows the distance between the atoms in the crystal due to the induced strain, verifying the impact of the strain in the atomic crystal of silicon.

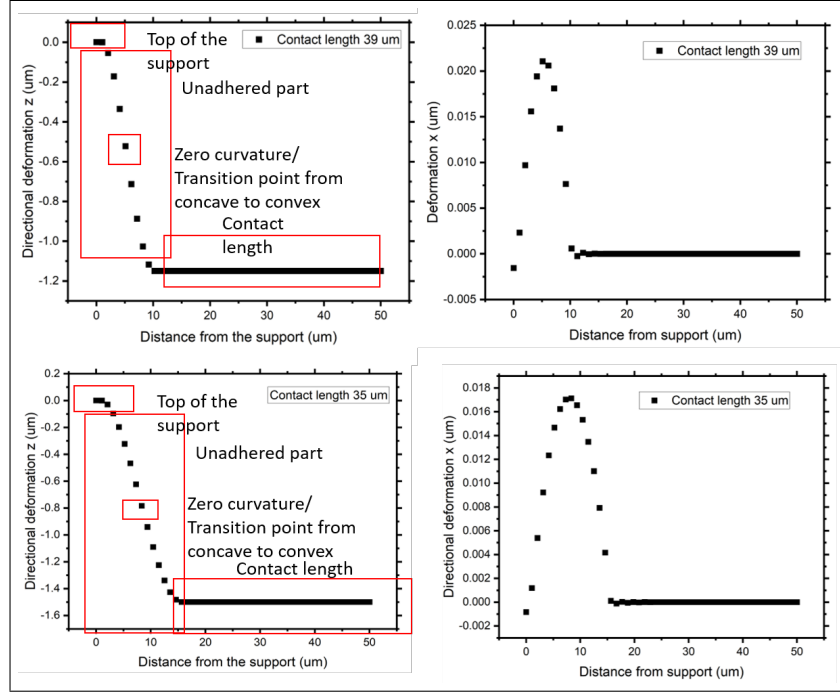


Figure A.14: Graphs obtained from the simulations for $h=1.15 \mu m$ (top) and $h=1.50 \mu m$ (bottom) a) directional deformation in z direction as a function of the distance from the support for the experimental value, highlighting points of interest and b) directional deformation in x direction as a function of the distance from the support.

We notice at first the appearance of compressive strain. This leads to a reduction in the interatomic distances between adjacent silicon atoms. As a result, the lattice becomes compressed, and the atoms are brought closer together. This compression alters the bond lengths and bond angles within the crystal lattice. Changing to tensile strain, an expansion of the interatomic distances between adjacent silicon atoms occurs. The lattice becomes stretched, and the atoms are pushed farther apart. This stretching also modifies the bond lengths and bond angles within the crystal lattice. In general, when subjected to tensile strains, the interatomic distances in the silicon lattice are enhanced, while compressive strains lead to a reduction in these distances [51].

The strain maps obtained from the simulations for $h=1.15 \mu m$ and $h=1.50 \mu m$ are shown in Figure A.15 and A.16. We noticed that the maximum induced strain is the normal strain, especially in x and z direction. This is due to the fact that the force is applied perpendicular to the membrane, in the z-direction. There is shear strained

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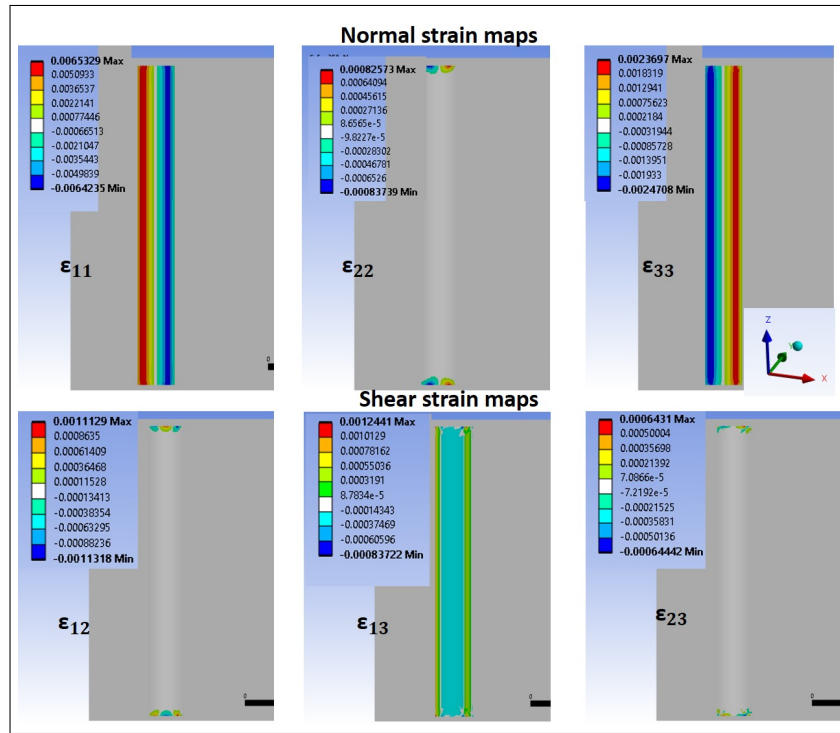


Figure A.15: Strain maps obtained from the simulations for $h=1.15 \mu m$

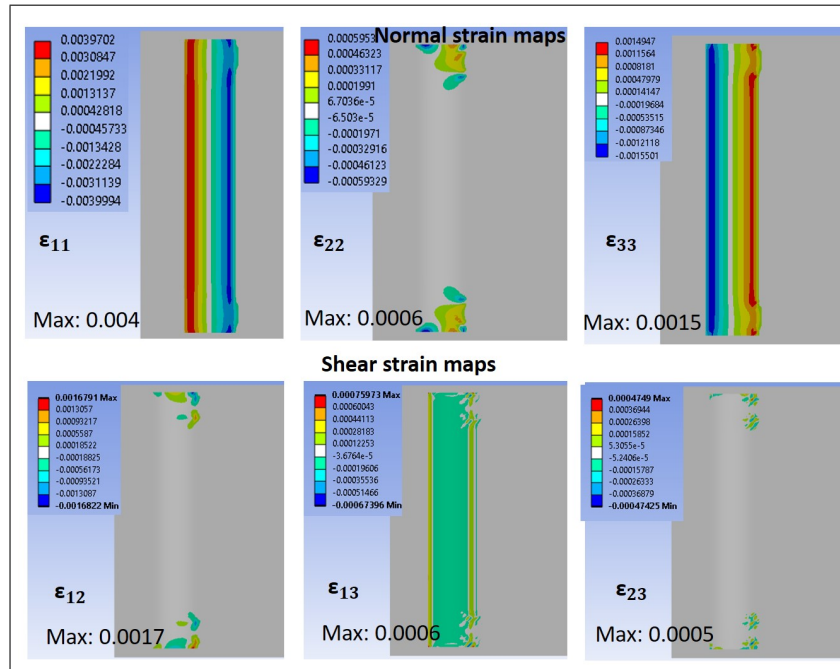


Figure A.16: Strain maps obtained from the simulations for $h=1.50 \mu m$

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induced as well, mainly in the 12 and 13 direction, while in 23 the values are very small to contribute to any change in the properties of silicon. By taking line scans in the models, the graphs of each strain components as a function of the distance from the support can be obtained. Figure A.17 shows these results for $h=1.15 \mu m$ and Figure A.18 shows the same results for $h=1.50 \mu m$. At the top right graph in both cases, the areas of interest are highlighted. As it can be noticed, the strain values go from extension to compression, passing through a zero point which indicates this transition. This is also the point that the curvature is 0, as it was previously mentioned. The line in 0 strain corresponds to the contact length where there is complete balance between extension and compression.

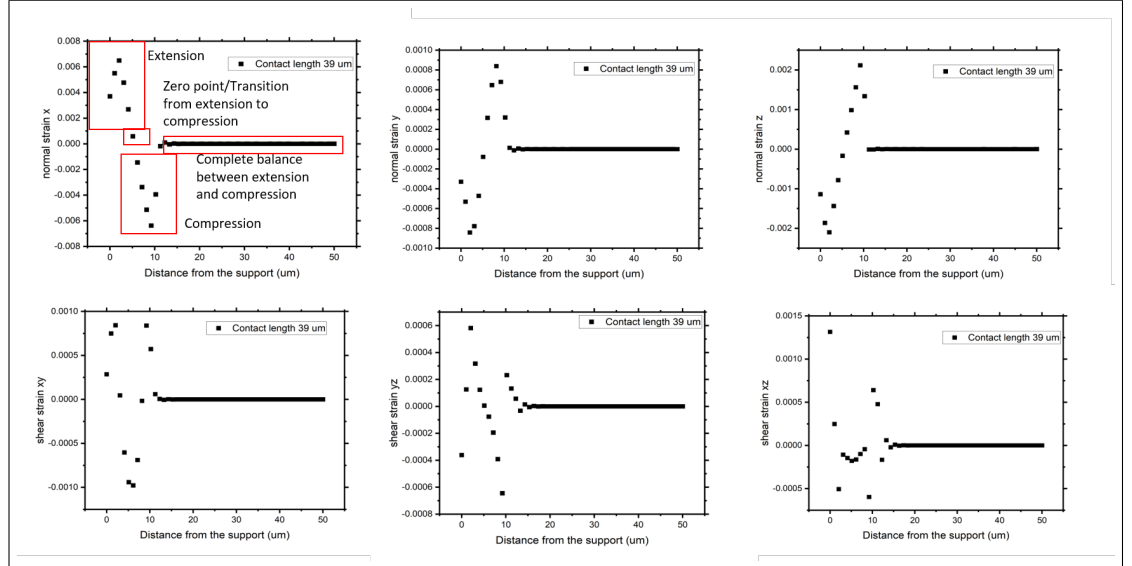


Figure A.17: Graphs obtained from the simulations for $h=1.15 \mu m$ between strain and distance from the support. a) normal x, highlighting points of interest, b) normal y, c) normal z, d) shear xy, e) shear yz and f) shear xz

A.3.1 Comparison between the three different approaches

In this section, a quantitative comparison between all the methods used in this chapter is presented.

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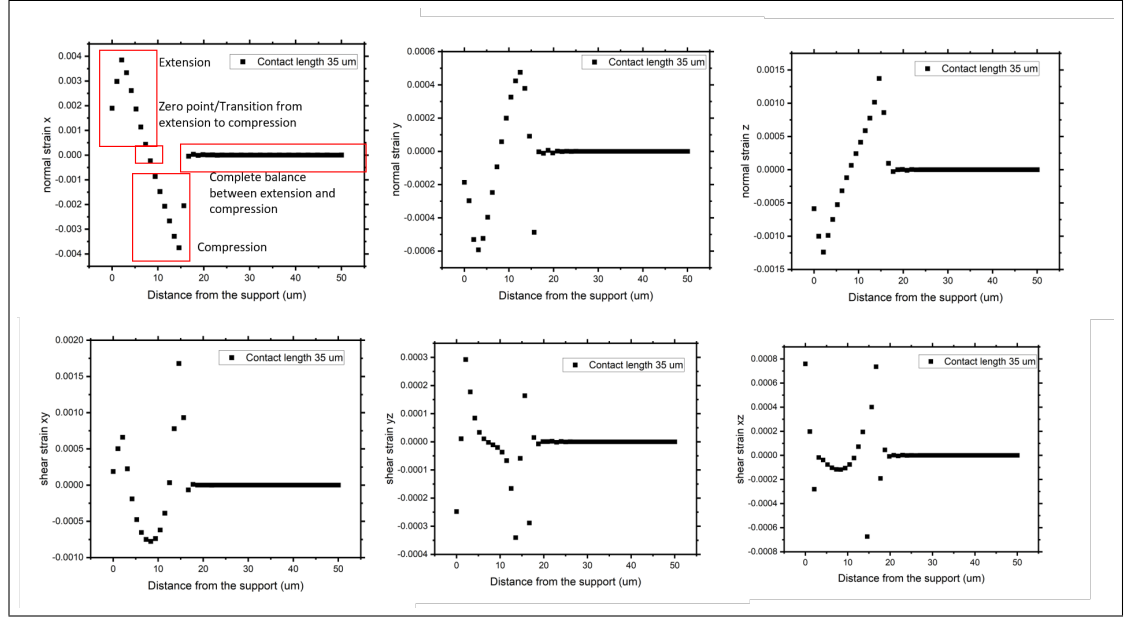


Figure A.18: Graphs obtained from the simulations for $h=1.50 \mu m$ between strain and distance from the support. a) normal x, highlighting points of interest, b) normal y, c) normal z, d) shear xy, e) shear yz and f) shear xz

A.3.2 Deformation

Figure A.19 a) and b) shows the directional deformation on z-axis comparison between simulations and theoretical model for $h=1.15 \mu m$ and $h=1.50 \mu m$, respectively. The deformation obtained from the theoretical model in both cases matches very well the results from the simulation. The different position of the points is due to the different steps in the distance range for the two different methods.

A.3.3 Angle of curvature

The bending of the membrane around the ridge will also result in a change in crystallographic directions of the Si lattice. Figure A.20 shows the comparison of the angle of curvature between the one obtained from the theoretical model and the one from the EBSD measurements for both cases. As mentioned in the previous sections, the theoretical value for the angle is calculated by using 4.8, while from the EBSD measurement, we can calculate the change in misorientation of the membrane by comparing how much the orientation in each pixel in the dataset deviates from a chosen reference

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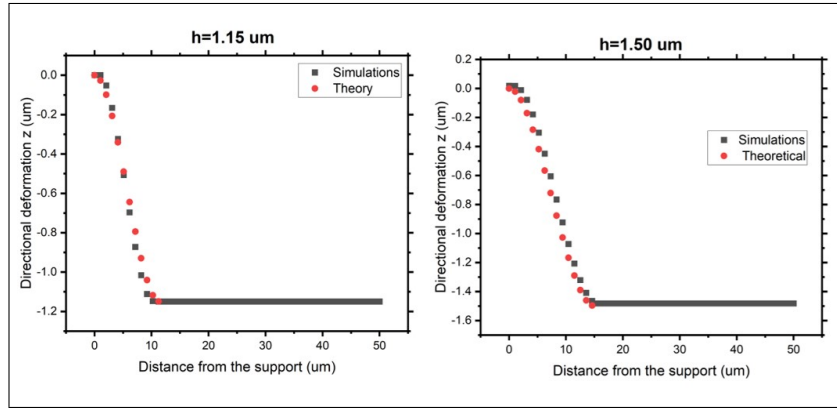


Figure A.19: Comparison between the directional z deformation derived from the simulations and the theoretical model a) for $h=1.15 \mu m$ and b) $h=1.50 \mu m$

orientation. This is referred to as grain reference orientation deviation (GROD) analysis. Considering the Si membrane is folded over the ridge, which is parallel to the Y axis, the orientation change should be only caused by a rotation around Y. Hence, the misorientation around the X and Z axis (GROD_x and GROD_z, respectively) are negligible when compared with GROD_y (not shown here). In the case of $h=1.15 \mu m$, the match is very good while in the case of $h=1.50 \mu m$, there is a slight difference between the two methods. The measured maximum angle from the EBSD is 1 degree higher than the calculated one, which can be attributed to the simplification of the model.

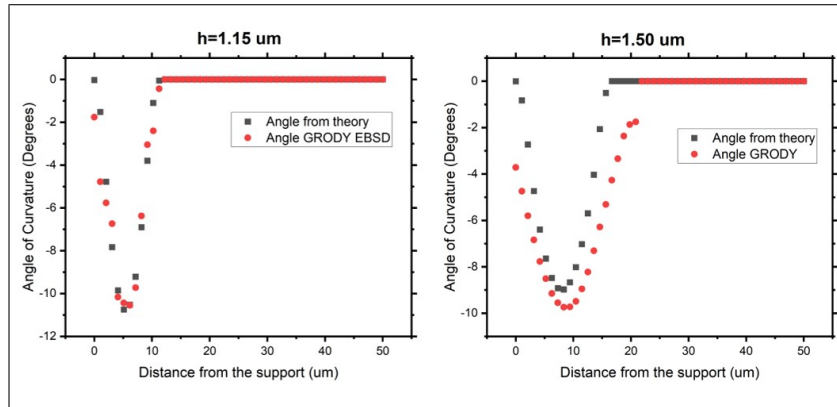


Figure A.20: Comparison between the angle of curvature obtained from EBSD and theory a) for $h=1.15 \mu m$ and b) $h=1.50 \mu m$

A.3.4 Strain

Figure A.21 shows the strain results for the two cases, comparing the strain values for the dominant direction that the strain is induced (ε_{xx}) obtained from the theoretical model, the simulation and the EBSD measurement. The theoretical value of strain was obtained from 4.11, for the simulation, the data were extracted from the linescan in the middle of the resulted strain maps and the values from the EBSD were extracted as a summary of multiple linescans at the middle of the measured strain maps.

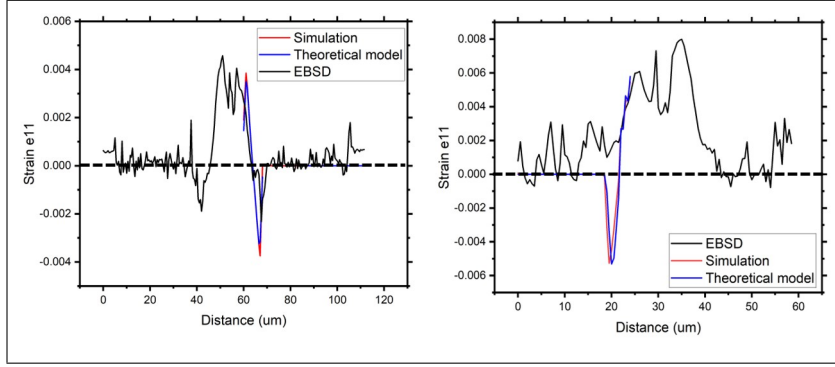


Figure A.21: Summary of all the results for the normal strain ε_{11} obtained from simulation, EBSD and theory a) for $h = 1.50 \mu m$ and b) $h = 1.15 \mu m$

As it can be noticed, the results from the simulations match reasonably well the predicted theoretical values. Figure A.21 shows this comparison for the two cases, verifying that the theoretical model can be a relative accurate way for determining the geometrical deformation and resulted values. The shift between the graphs come from the fact that there is a different scanning length in the EBSD measurement. The measured ε_{xx} corresponds reasonable well with the predicted values from the simulation and theoretical model. From the top down it shows an extension, tensile strain, passing through the transition point to a region of contraction where the membrane is compressed before approaching zero at the contact area. The measured values are slightly less symmetrical around the transition point. This is probably real since the contact at the top of the ridge and the flat contact area on the substrate are different. At the top, the Si membrane is not flat, it is curved around the ridge and may not be in perfect contact with the ridge. For the simulations, however, the Si membrane

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is only fixed at different heights, but does not assume the bending around the top of the ridge. Hence, it results in a symmetrical linescan. Additionally, the sides of the Si membrane may not be perfectly parallel with the ridge, which would also influence the measurement.

The results of the simulations are in the same order of magnitude with the results that we get both from the theoretical model and the EBSD measurements, verifying that by transfer printing silicon membranes on top of ridges, we can induce normal strain of 0.6% and 0.4% for $h=1.15\text{ }\mu m$ and $h=1.50\text{ }\mu m$, respectively.