Analysis in Circuit Breaker Performance Requirements for High-Voltage DC Networks

A thesis submitted for the degree of Doctor of Philosophy

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This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

Power transmission systems are seeing significant changes with the introduction of large amounts of renewable energy. Integration of these into the network is challenging on two fronts. Firstly, increased penetration stresses conventional generation as those from renewable are intermittent and fluctuate in power output. Secondly, many of these sources are located in areas which are difficult or impossible to economically connect to the network using convention ac technology. This is a major issue for offshore wind where distances to shore are increasing, particularly in the North Sea region. Large scale, multi-terminal high voltage dc networks may offer a solution to these issues, and modern voltage source converters have a small enough footprint to be located on offshore platforms. However, during dc faults these suffer from high currents and the system is unable to transfer power. Prototype dc circuit breakers have been developed by manufacturers to, in theory, allow seamless operation of the healthy areas of the network when a fault occurs. In order to do this they operate extremely fast; opening in less than 5ms. To achieve this the topologies have become complex and expensive, hindering development of multi-terminal systems.

In this thesis the requirements of the converter, dc breakers and overall HVDC network are reassessed. The factors influencing stress within the converter and breaker are quantified. Design adjustments which may be used to mitigate these are then investigated. Simplified circuit analysis allows approximations the stresses to calculated and used for initial design iterations. The impact these design alterations has on normal operation is then addressed.

A multi-terminal system model is then used to assess how different circuit breaker topologies can effect the fault ride-through of the network. Fault detection and discrimination algorithms are implemented to ensure accurate representation of the time overhead this incurs. It is shown that the variation between slower, cheaper circuit breakers and faster, more costly circuit breakers is not as large as indicated in the current literature. Ride-through for slower circuit breakers is achieved for only a marginal increase in restart time, which is still below the operating speed of conventional ac breakers.

Acknowledgements

I would like to thank Professor Steve Finney for his guidance over the course of my study, on both academic and on personal levels. He has always been able to get to the bottom of a technical issue I was stuck with and he always listened to my ideas, giving me confidence in my work I might never have otherwise found. Dr. Lie Xu for always having thirty-five minutes for my "just five minutes" technical questions, helping to distil much of the knowledge of HVDC I have gained. Derrick Holliday for giving me the opportunity to study within the power electronics group and helping with my transition to Glasgow. Grain Adam for always letting me draw on his vast power electronics knowledge over copious amounts of tea. He has the capacity to bring a smile and a laugh to me even when I am feeling quite the opposite.

Joe Burr and Yanni Zhong have been true friends throughout my time at Strathclyde, without whom I would surely have caved before this point. Joe has helped significantly with my academic work, providing an extra set of eyes when a model won't run or produces odd results I cannot fathom – he has doubtless saved me weeks of lost time. Whether is was a Sunday at 10:30AM or Wednesday evening at 11:30PM, Yanni was always there in 3.08 ready to take that well deserved tea break, listen to each others gripes and, most importantly, share her home-cooked food with me when I needed it most. To Azmy Gowaid and Dimirios Vozikis for their impeccable work ethic and rigour, which I can only strive to replicate, I thank you both. To my dearest friends from Bristol – Chandan Shergill, Chris Walsh, Joe Hampson, Michael Starr and Saleem Zuberi – who have helped to remind me that there is a life outside of Simulink to look forward to at some point in the future. Christopher Wilkinson, Colin Barron and Pascal Pillay for staying with me even after I have moved far away. Over the last ten years to Pollards have provided me with wonderful guidance on life, I thank them for this dearly.

Most of all to my mother Sarah, sisters Celine and Pop, brother Henry and my grandmother Edna that have given me great support through my academic life when I have most needed it.

List of Publications

[1] **"DC fault Parameter Sensitivity Analysis"**. F.P. Page, G.P. Adam, S.J. Finney, D.H. Holliday and L. Xu. Proceedings of the 12th IET International Conference on Developments in Power System Protection (DPSP 2014). Vol. 2014

Abstract: At present High Voltage Direct Current (HVDC) Voltage Source Converters (VSC) are susceptible dc faults leading to extreme currents. The fault current cannot be controlled by the converter switching flows in the anti-parallel diodes. Protection devices are, therefore, required to operate with sufficient speed to avoid device failure. A method is introduced to calculate the critical time for protection to operate. Using this method it is then shown how the critical time may be extended by way of optimization of passive system components. In order to perform this optimization a new post-fault (when the converter gating signals are inhibited) model of the Modular Multi-Level (MMC) converter is introduced which drastically reduces simulation time, allowing high resolution parameter sweeps to be performed. The model is validated and is shown to produce fault characteristics similar to that of a conventional switched model.

[2] **"An Alternative Protection Strategy for Multi-terminal HVDC"**. F.P. Page, S.J. Finney and L. Xu. Paper presented at 13th Wind Integration Workshop, Berlin, Germany 2014.

Abstract: Development of multi-terminal HVDC has been held back by the lack of adequate dc breakers. This has led to a number of novel breaker designs being developed by manufacturers. However, perceived operating time constraints have resulted in complex solutions with associated cost and size penalties. For this reason system operators have yet take up any of the proposed designs for use within real systems. To realise any multi-terminal system the cost of the dc breakers must, therefore, be reduced. Given that the complexity of the breakers is driven by the requirements of their speed it is prudent to question why there is this requirement. A relaxation of the operational speed will enable

simpler, cheaper solutions to appear, in turn assisting the economic case of multi-terminal systems. This paper re-evaluates the requirements for dc circuit breakers with an emphasis on the impact of dc faults on converter stations and ac connections. It is shown that ultra-fast dc breakers are not necessary in order to have adequate performance from the ac grid's point of view. The converter is also shown to survive for the required period of time. This allows slower, less complex dc breakers to be used, which could lead to a swifter uptake within commercial systems and eventually multi-terminal systems.

[3] **"Optimisation of Passive System Components to minimise DC Circuit Breaker Stresses in Multi-terminal HVDC Systems"**, F.P. Page, S.J. Finney, D.H. Holliday and L.Xu. Paper presented at Cigré International Symposium : Across Borders - HVDC Systems and Market Integration, Lund, Sweden 2015.

Abstract: HVDC circuit breaker designs have commonly included additional series inductance to reduce the rate of rise of current during the initial transient period after a fault occurs, minimising the peak current stress that the circuit breaker must endure. A method of approximating the peak fault current and energy dissipation in a circuit breaker is developed, through circuit analysis of a multi-level converter (MMC) under fault conditions. These approximations are validated against simulation results for an 800kV MMC system.

[4] **"Continuous Operation of Radial Multi-terminal HVDC Systems under DC Fault"**. R.Li, L. Xu, D.H. Holliday, F.P. Page, S.J. Finney and B.W. Williams. IEEE Transactions on Power Delivery, 2015.

Abstract: For a large multi-terminal HVDC system, it is important that a DC fault on a single branch does not cause significant disturbance to the operation of the healthy parts of the DC network. Some DC circuit breakers (DCCBs), e.g. mechanical type, have low cost and power loss, but have been considered unsuitable for DC fault protection and isolation in a multi-terminal HVDC system due to their long opening time. This paper proposes the use of additional DC passive components and novel converter control combined with mechanical DCCBs to ensure that the healthy DC network can continue to operate without disruption during a DC fault on one DC branch. Two circuit structures, using an additional DC reactor, and a reactor and capacitor combination, connected to the DC-link node in a radial HVDC system are proposed to ensure over-current risk at the converters connected to the healthy network is minimized before the isolation of the faulty branch by mechanical DCCBs. Active control of DC fault current by dynamically

regulating the DC components of the converter arm voltages is proposed to further reduce the fault arm current. Simulation of a radial three-terminal HVDC system demonstrates the effectiveness of the proposed method.

List of Acronyms and Symbols

Acronyms

ACCB	AC Circuit Breaker
BPS	Bypass Switch
CCGT	Combined Cycle Gas Turbine
CSC	Coltage Source Converter
DCCB	DC Circuit Breaker
FWD	Free-wheeling Diode
GTO	Gate Turn-off Thyristor
FB-MMB	Full-bridge Multi-level Converter
HB-MMC	Half-bridge multi-level Converter
HVAC	High-voltage ac
HVDC	High-voltage dc
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
M	Modulation index
MV	Medium Voltage
MOSA	Metal Oxide Surge arrester
MRTB	Metallic Return Transfer Breaker
PCC	Point of Common Coupling
PF	Power Factor
P2G	Pole-to-ground (fault)
P2P	Pole-to-pole (fault)

SOA	Safe Area of Operation
SM	Multi-level Converter Sub-module
SCC	Short Circuit Capacity
UFD	Ultra-fast Disconnector
VSC	Voltage Source Converter

Symbols

C_j	Device junction thermal capacity
C_{cell}	Sub-module cell capacitance
f_m	Modulation frequency
f_s	Witching frequency
i_{arm}	Converter arm current
I_{dc}	DC current
L_{arm}	Converter arm inductance
R_{fault}	Fault resistance
L_{dc}	DC inductor
L_{p}	Parasitic inductance
N	Number of sub-module (per arm)
P_j	Device junction power dissipation
R_{th}	Device thermal resistance
S_c	Rated converter power
S_B	Base power
T_a	Ambiant air temperature
V_{B1}	Network side nominal voltage
V_{B2}	Converter side nominal voltage
T_{cb}	Circuit breaker operating time
V_{cell}	Sum-module cell voltage
V_{cb}	Circuit breaker clamping voltage
V_{dc}	Pole-to-pole dc voltage
V_{LL}	Line-to-line ac voltage (RMS)
X_{ac}	Sum of network and transformer impedance
X_{TRM}	Transformer leakage reactance

Contents

Chapter 1

Introduction

1.1 Growth of Renewable Energy Sources

The desire to move away from carbon based energy sources to renewable ones has been increasing throughout the world. Figure 1.1 shows the increase in non-hydroelectric energy production over the last thirty years. China has increased its installation of wind and photovoltaic sources very rapidly in the last ten years. However, this has come alongside large increases in conventional sources, in particular coal, over the same time. This means that issues of increased penetration of intermittent sources is less of an issue. In Europe the European Energy Directive dictates that 20% of total energy consumed by member states should come from renewable sources by 2020 [1]. As Figure 1.1 demonstrates, the relative proportion of intermittent power has increased significantly as a result. Different power sources are more prevalent within different geographical locations. Solar energy in the form of photovoltaic and solar thermal in southern Europe (Spain dominantly) and North Africa, Geothermal in Iceland, Hydro in Norway and Wind from the North Sea and Atlantic coast. Figure 1.2a shows the cumulative installed wind capacity within EU member states. Growth has been substantial since the turn of the century and in 2014 produced enough to cover 10.2% of electricity consumption within the EU [1]. The difficulties in obtaining planning permission, along with higher average wind-speeds (see Figure 1.3), has lead to an increased interest in offshore installations. As Figure 1.2b shows, the share of offshore wind has been growing significantly.

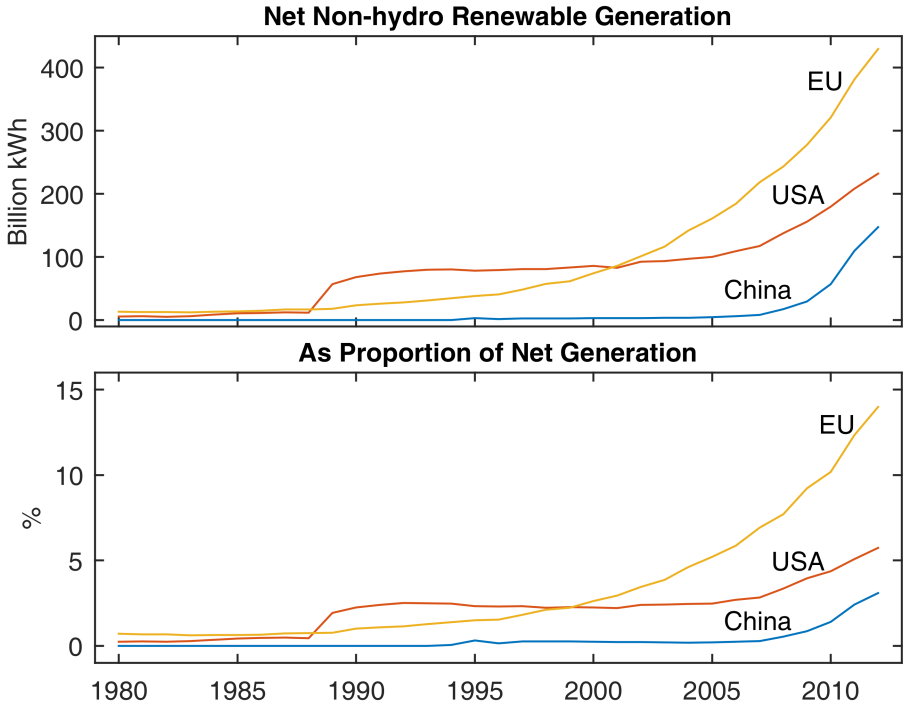
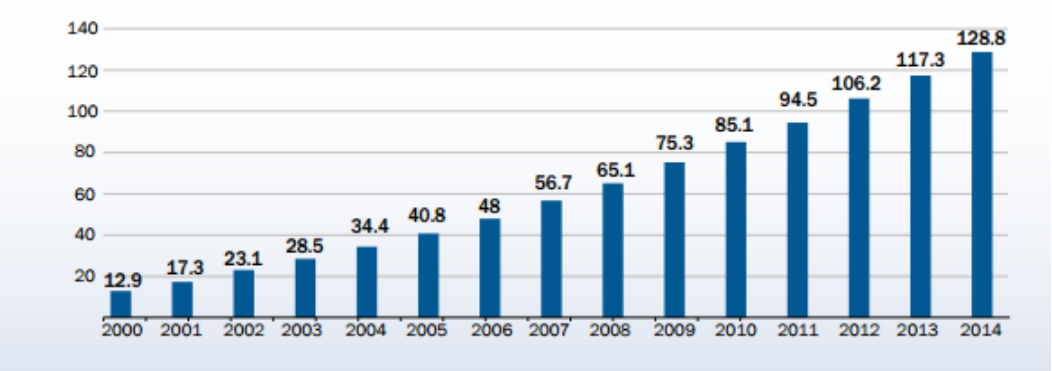
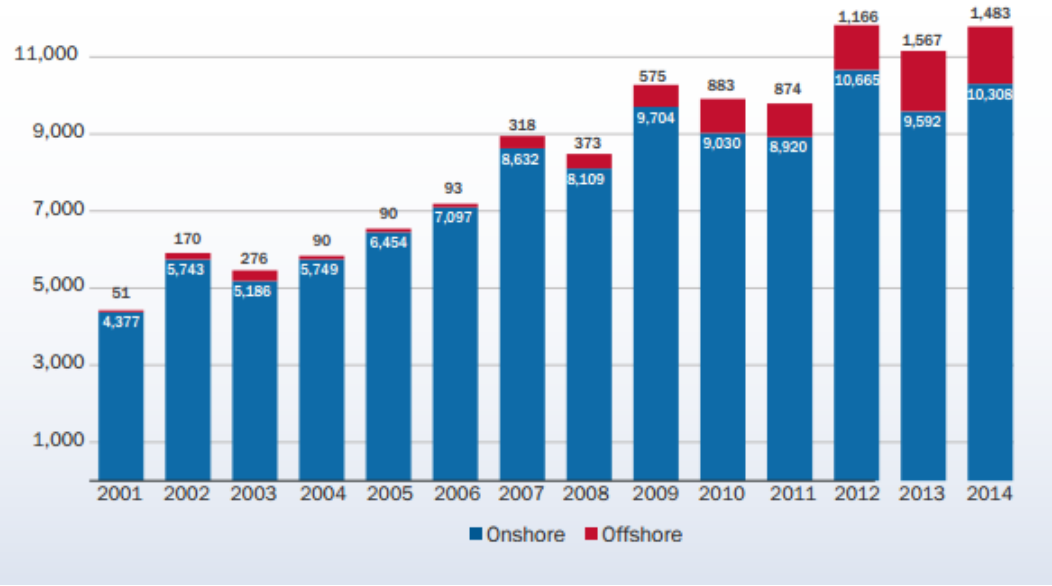


Figure 1.1: Growth of non-hydroelectric, renewable energy production for selected countries. Data sourced from U.S. Energy Information Administration [2]



(a)

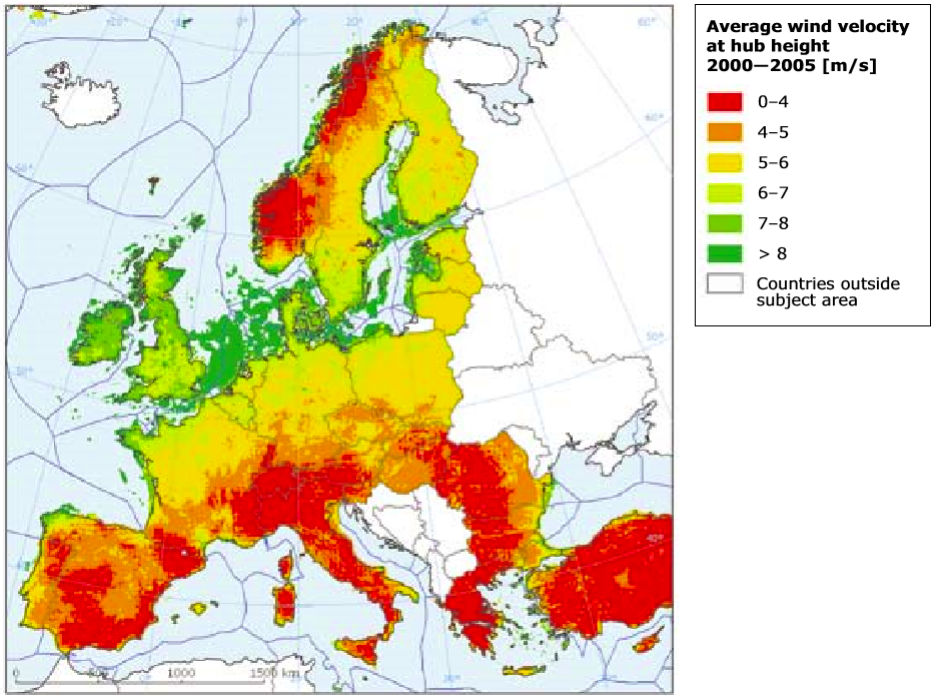


(b)

Figure 1.2: European wind: (a) Cumulative installed wind generation capacity [GW]; (b) Annual onshore and offshore installations [MW] [3]

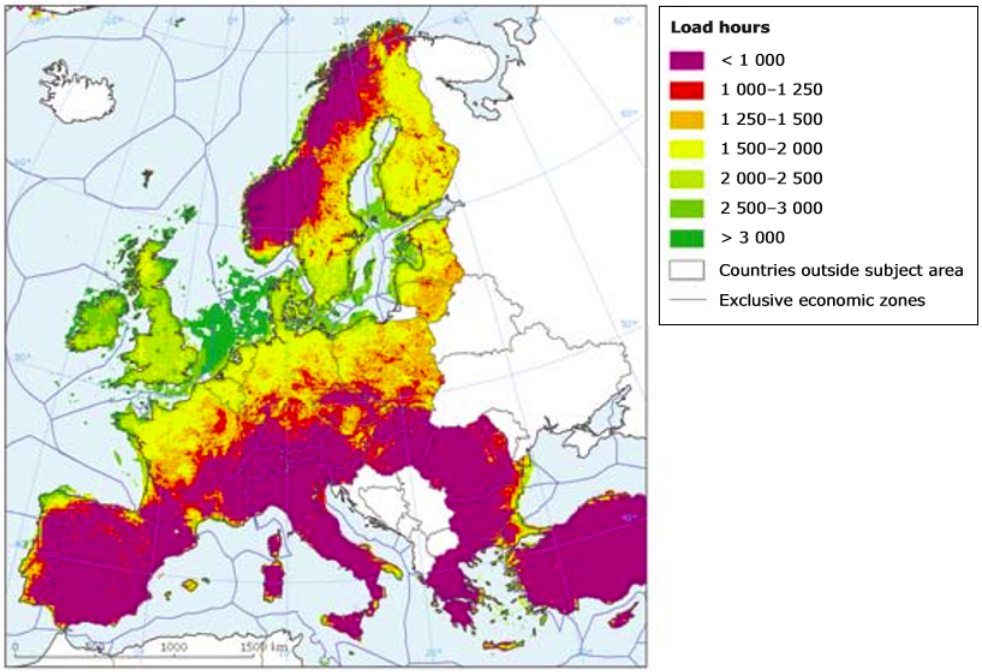
1.2 Transmission distance

Figure 1.3 shows average wind speeds throughout Europe, indicating the potential power output of wind farms in each location. It is clear that northern Europe, and particularly the U.K, are resource rich by this measure when compared to continental and southern Europe. The strongest resources are located in the North Sea, geographically between the U.K, Belgium, The Netherlands, Germany and Norway, where average wind speeds are over 8m/s. Not only is average wind speed greater, offshore locations also provide a more consistent resource. As Figure 1.4 shows, the number of full load equivalent hours for offshore is significantly higher than those onshore, providing a higher utilisation.



Source: EEA, 2008.

Figure 1.3: ECMFW wind field data after correction for orography and local roughness (80m onshore, 120m offshore) [4]



Source: EEA, 2008.

Figure 1.4: Distribution of full load hours in Europe (80m hub height onshore, 120m hub height offshore) [4]

Making use of this resource can be challenging – the best resources are located at significant distances from shore. As Figure 1.5 demonstrates, a large proportion of the potential wind energy resource of U.K. is located over 30km away. Connection to these locations poses additional costs due to increased water depth, making turbine foundations more complex, as well as the increased length of export cable required.

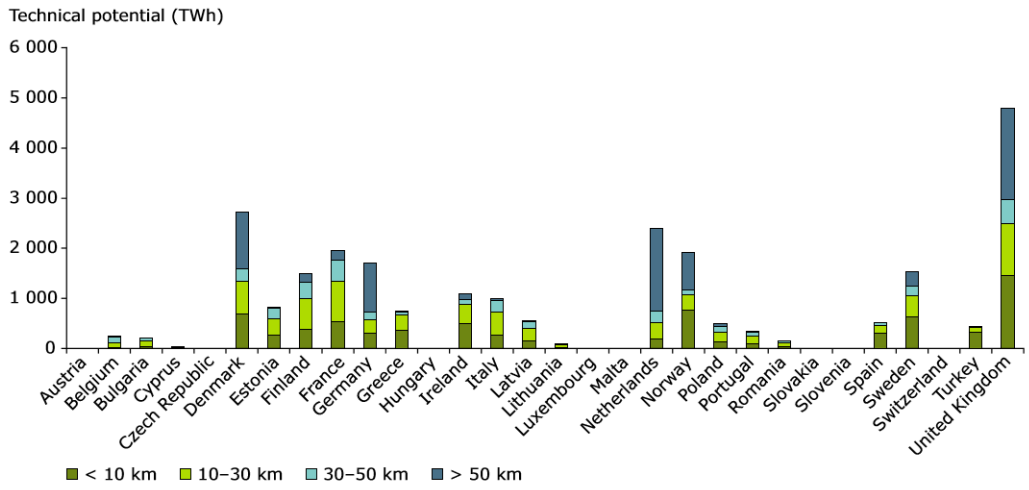


Figure 1.5: Distribution of wind resource by distance to shore for various European jurisdictions [4]

Transmission of power back to shore over long distances of cable is undesirable. The capacitive charging current required over increased lengths reduces the capacity of the cable to transmit real power and often requires compensation. This has limited the size and distance to shore of large wind farms. As Figure 1.6 shows, the export cable lengths began to plateau around 40-60km when ac transmission is used. Newer schemes have begun to make use of High Voltage DC (HVDC) for exporting power over long distances from large wind farms. To date six schemes are now in operation, which have led to a significant increase in the offshore cable length from approximately 60km to 160km, a trend that is continuing.

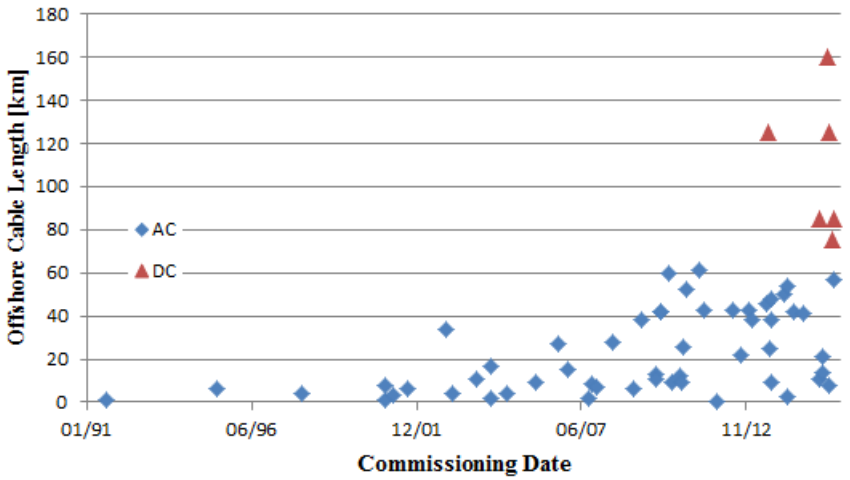


Figure 1.6: Length to shore of export cable for offshore wind farms built in the previous 25 years. Data points are plotted by commissioning date. Distinction made between ac connections (both MV and HV) and HVDC. Cable length refers to offshore portion.

1.2.1 Restrictions on HVAC

Cable insulation gives rise to parasitic capacitance between the conductor and the sheath. When energised by ac, this causes additional current to drawn from the source to charge and discharge the cable each cycle. For a simple circular geometry the capacitance is given by (1.1) where ε = relative permittivity of insulation, D = diameter of the main insulation [mm], d = diameter of the inner conductor [mm] [5]. The formula demonstrates that the amount of capacitance is proportional to both the cable length and the rated voltage (by which the insulation thickness D is determined). As cable length increases the effective shunt capacitance does so also, along with a higher reactive current. As total current through the cable is thermally limited, this results in a reduced capacity to transmit real power to the receiving end of the cable.

$$C_b = \frac{5.56 \cdot \varepsilon}{\ln\left(\frac{D}{d}\right)} [\mu\text{C/km}] \tag{1.1}$$

Table 1.1 shows sample maximum power throughput for cables at several different voltages and over different lengths. There is a marked reduction in real power throughput as cable length increases. In the highest voltage case (220kV) the charging current required to maintain unity power factor at the receiving end of a 30 mile cable exceeds the thermal limit, where soil resistivity is increased. The result is a physical limitation beyond which no real power can be transmitted through the cable, as shown in Figure 1.7. In reality, the practical maximum length is below the technical limit in order to reduce losses through large reactive power flows through the cable.

Table 1.1: Comparison Between Thermal Rating and Maximum Permissible Unity Power Factor Load Output for 20-and 30-Mile, 2,000,000-CM Oil-Pipe-Type Cable Lines [6]

Voltage Rating, Kv	Thermal Rating,* Mva	Soil Thermal Resistivity, Cm C† per Watt	Total Charging Reactive Power, Mva		Maximum Permissible Unity PF Load Output, Mw		Percentage of Line Rating Available	
			20 Miles	30 Miles	20 Miles	30 Miles	20 Miles	30 Miles
66	110	80	36	54	105	96	95	87
132	200	80	90	135	180	148	90	74
220	300	80	172	258	250	153	83	51
220	250	100	172	258	181	0	72	0

* Ratings are based on a single isolated pipe line, AEIC maximum permissible normal conductor temperatures, maximum dielectric power factor of 0.5%, 36 inches cover, 85% daily loss factor, and 25 C earth ambient.

† Degrees centigrade.

Cable utilisation, real power transmission and maximum length can be extended with the use of reactive power compensation. In the case of Horns Rev B, a 210MW Danish wind farm located 45km from shore, this is accomplished by placing a reactor 2km from the shore line [7].

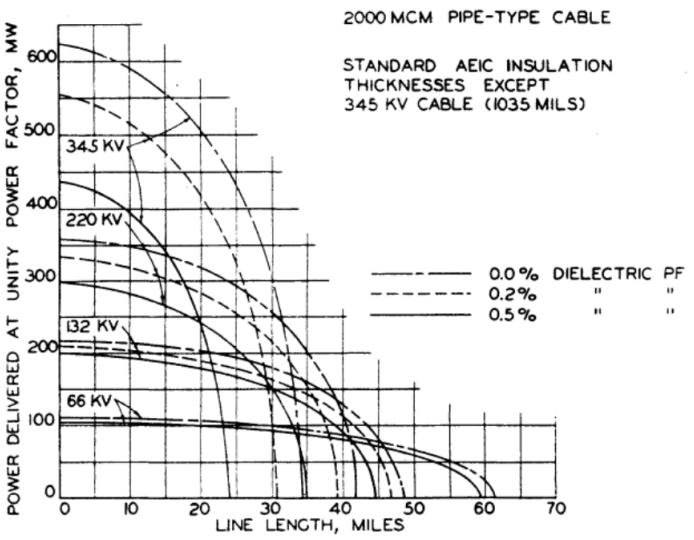


Figure 1.7: Maximum power delivered for various line lengths for vaious nominal voltages. Increased voltage results in an increase in power transfer capability, but maximum line lengths are significantly reduced [6]

This reduces the reactive current drawn through the cable, thus reducing losses and releasing capacity for real power transmission. However, for longer cables installing shunt compensation at multiple offshore locations becomes challenging, particularly offshore. The additional reactive components can alter the harmonic impedance of the network and potentially lead to resonance and instability.

Reactive power flows are eliminated when the cable is energised with dc, allowing full utilisation of the thermal capacity of the cable for transmission of real power – improving utilisation of the asset. However, this requires a conversion process at each end of the cable, from ac to dc at the wind-farm end and the reverse onshore. Transmission by dc therefore introduces additional costs, in the form of conversion losses and capital expenditure on the converters. These must then be balanced against the losses from reactive power flows and compensation equipment when energised using ac [8]. With no reactive power flow within the cable the limitation on transmission distance is removed, allowing a much wider ranges of resources to be reached.

1.3 Increased Penetration and Networking

As the amount of wind generation increases it becomes difficult for the network to cope with the fluctuation in power associated with the intermittent generation patterns. Traditionally, generation is ramped up and down to meet network demand. This becomes more challenging wind penetration increases and a larger proportion of the supply has an intermittent nature

(see Figure 1.8).

Hydro-carbon based generation such as Combined Cycle Gas Turbine (CCGT), which can rapidly vary their power output, will be required to smooth the generation profile of intermittent sources. By definition, these will operate part-loaded and in an on-off basis depending on wind-farm output. Their energy output per unit of capacity is lower, which results in a higher cost per unit of energy generated as utilisation is lower [9]. The additional generation from hydro-carbon based resources also has the potential to lower the impact of renewable sources in reducing carbon emissions.

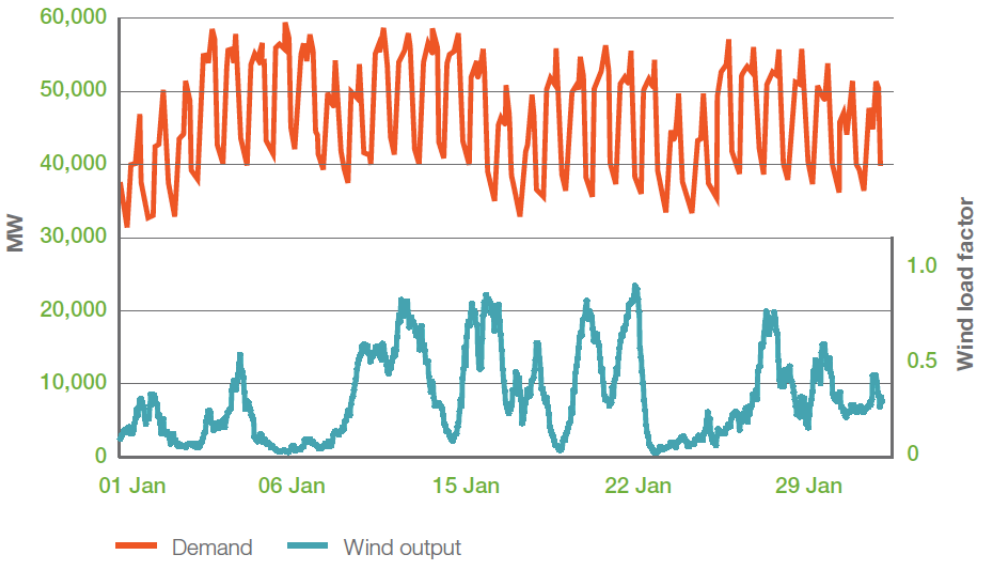


Figure 1.8: Energy demand and wind generation profile. The figure show Great Britain's demand profile (red line) for January 2010, together with a scaled January 2010 wind generation profile (blue line) that reflects the estimated wind capacity in January 2021 – i.e. 26,700 MW of offshore and onshore wind capacity (of which 9,000 MW onshore), in line with the 2020 'Gone Green' scenario developed by the Electricity Networks Strategy Group (ENSG, 2009). Overall, it shows how the estimated future onshore wind generation can contribute to a demand profile similar to our current (2010) needs [9]

The intermittent nature of renewable sources can, however, be mitigated by increasing connection between regions, allowing energy to flow between national borders and geographic areas more readily. Figure 1.9 shows existing and proposed HVDC links up to 2020. Large scale, multi-terminal networks have been suggested by various manufacturers and organisations. This can reduce the number of conversion processes that occur at nodes (which each incur a loss). An example is the pan-European network proposed by Friends of the Supergrid is shown in Figure 1.10.

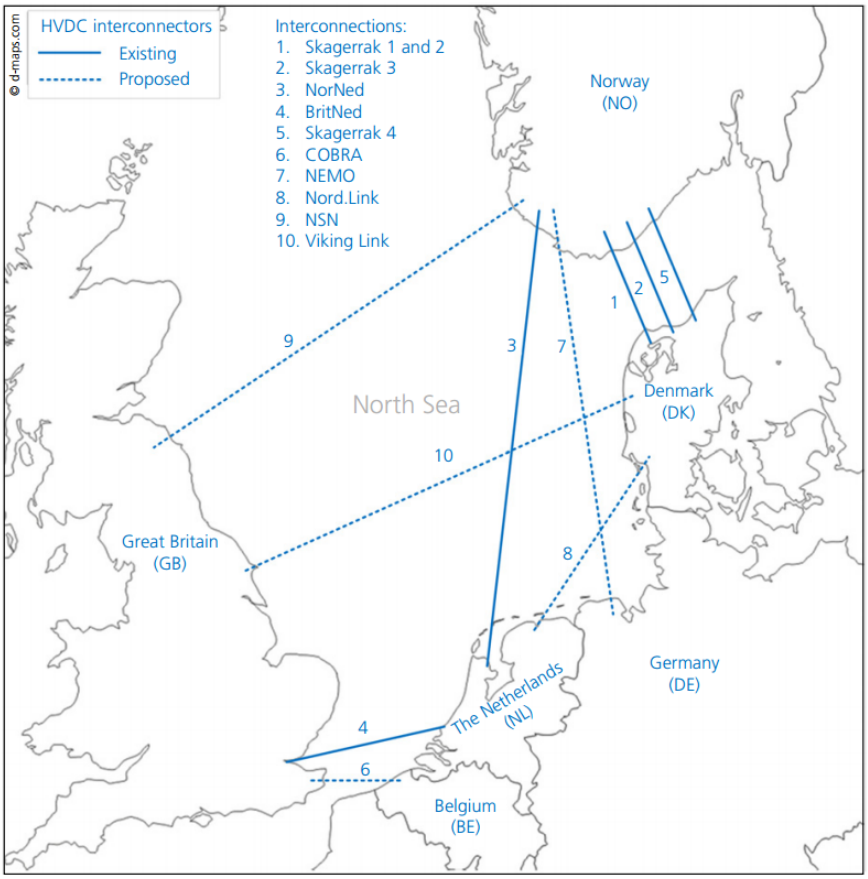


Figure 1.9: Existing and proposed HVDC interconnectors in the North Sea by 2020 [10]

Figure 1.10: Conceptualised HVDC pan-European supergrid [11]

1.4 HVDC

HVDC allows the transmission of large amounts of power over long distances and between asynchronous sources. This technology is, therefore, ideal for the task of integrating renewable energy sources which may be located far from load centres. Power throughput and transmission across boarders, such as the European and U.K, may be controlled actively in order to take advantage of price differentials and make optimum use of reserves. It allows connection between different power networks and the connection of offshore wind farms to more than one load centre.

1.4.1 Principles of HVDC

The current transmission system overwhelmingly utilises HVAC. HVDC encompasses the conversion of power as well as the transmission medium (overhead line or cable)and can be categorised based on the conversion technique used: Line Commuated Converters (LCC) and Voltage Source Converters (VSC).

The first commercial HVDC scheme was commissioned in 1954, a 100MW scheme linking the island of Gotland to mainland Sweden utilising mercury arc valves [12]. Technology has progressed and, with the use of high capacity thyristors, modern schemes are highly efficient, with capacities up to 10 GW and operating at voltages of up to ±800kV [13, 14]. Feasibility studies in China are investigating increasing further to 11GW and possibly even 14GW systems at ±1100kV [15].

Connection of more than two converters to form a networked HVDC system was accomplished in the 1980s, with the expansion of the Sardinia-mainland Italy link to include a station in Corsica [16]. However, the scheme operates on a fixed current direction; a change in power flow requires a change in voltage polarity. This makes control of the system complex and high level coordination is required, reducing the scope for large network applications.

The first commercial Voltage Source Converter (VSC) installation linked Gotland island, Sweden to the mainland via a 70km long cable in order to export the increased power generated by the expanded wind-farm [17]. At 50 MW the first schemes were relatively low capacity when contrasted to the current LCC technology. However, technological innovation has led to a rapid increase in power capacity. This has been possible chiefly due to the development of the Modular, Multi-level Converter (MMC) [18], allowing dc voltage and, subsequently, power throughput to increase (which had been restricted by the two level topologies of legacy converters). The topology also has a much lower switching frequency which has aided in reducing converter losses.

VSC operates with a fixed polarity dc voltage. This readily allows them to operate parallel in a multi-terminal network with a common dc bus. Power can be controlled at each converter individually without any coordinated control of the other converters. The power inflows and outflow of must still be matched to give a net zero energy balance (neglecting losses), but crucially the converters do not need to be physically reconfigured when changing power flow direction.

Where the local ac network is weak it is challenging for LCC systems to operate in. Sharp voltage fluctuation, such as during ac faults, can cause commutation failures – a form of fault whereby the dc side is short-circuited by device shoot-through [19]. The converters switch at ac line frequency, causing low frequency harmonic emissions, and require reactive power compensation. They also tend to require large land areas in order to accommodate filtering and reactive power compensation equipment. These requirements limit the scope of applications for LCC systems. For instance, they cannot be readily used in offshore applications due to the large filter footprints and weight.

VSC is a much more flexible as a technology. Its voltage output is independent of the local ac network, allowing freedom over real and reactive power throughput. Internally it is current controlled, giving it superior performance over LCC during ac side disturbances such as faults. The use of pulse-width modulation (PWM) switching for two-level converters and staircase output within MMC produces high-quality current and voltage output. This requires little or no filtering on the ac side and helps to reduce the footprint of the converter, allowing it to be installed in offshore platforms.

VSC is, however, susceptible to large currents during dc side fault. The low voltage causes currents to be drawn from the ac side, over which the converter has no control. Modified topologies of the MMC have been proposed that can actively block fault current. However, the additional life-time costs from losses and capital expenditure detract from the increased benefits [20, 21, 22].

1.4.2 Protection Issues

The use of VSC allows converters to be readily connected in parallel, facilitating multi-terminal networks. However, as larger meshed networks are envisioned the issue of ensuring systems are resilient to faults is critical. Interruption within a dc network is more complex than in the equivalent in ac networks. The impedance within the dc network is not the dominant factor in limiting the current that flows following a fault. The time for current to rise to its peak value is typically much faster than within ac systems. Breaking currents on the dc side is also

complex [23]. Unlike ac systems, where current passes through a zero point twice per cycle, dc fault current will remain at its steady-state level until acted on by an external force. Therefore, circuit breakers cannot open and clear on the natural current zero, they must generate one internally [24].

In order to create a current zero the circuit breakers must generate a counter voltage to overcome the driving-voltage – that is, they must oppose the residual voltage produced on the dc side of the converter, in itself produced by the ac network. Voltage collapse through the system is rapid and results in no power being able to be transmitted through the network. This is fundamentally different to ac faults where the depressed voltage is localised – nominal voltage is retained further from the fault.

Breakers for LCC based systems were developed in the 1980s [25]. The resonant/mechanical topology they used has been presumed too slow for the modern voltage source converter from which multi-terminal networks are to be constructed [26]. This has led to a new generation of circuit breaker topologies being developed, aimed at providing an operating speed in the sub-5ms time frame. However, these breakers have a high projected cost, limiting their potential applications [27, 28].

1.5 Organisation of Thesis

In Chapter 2 line-commutated and voltage source converters are discussed. The theory of operation, their relative merits and appropriateness for offshore applications are covered. Three circuit simulator models of the MMC are then given.

In Chapter 3 typical fault profiles for a modular, multi-level voltage source converter are documented. The principle effects different dc grounding topologies have on fault characteristics is analysed theoretically and with aid of simulation. Fault currents within the MMC are then analysed mathematically.

In Chapter 4 the impact of parameter changes on fault stress levels is investigated. A test system is defined along with a standardised measurement techniques used to compare and contrast results found from different parameter adjustments. Stress tests are performed for a number of parameter variations such as transformer impedance and system strength and the key findings highlighted. Design considerations for parameter changes are discussed to give to emphasis the benefits in fault performance that may be achieved in exchange for reduction in normal operation performance.

An overview of the challenges in building a dc breaker for HVDC applications if discussed

in Chapter 5. The basic building blocks used to create a dc breaker for HVDC applications are covered. Fundamental principles and theory of clearing faults within a dc system are covered. State of the art development in breaker designs and topologies aimed at VSC base multi-terminal systems are reviewed. The operating principles of each topology is over viewed and the relative performance benefits disscussed.

In Chapter 6 analysis is provided on circuit breaker stress. Parametric studies performed in Chapter 4 are extended to investigate how to optimise additional dc inductance placed next to the converter to reduce the stress on the breaker. Theoretical behaviour of the circuit under fault is assessed. A reduced complexity model is then created in order to study how the additional inductance will interact with the converter and circuit breaker. This is used to provide approximations of peak current stress and circuit breaker energy dissipation, which are contrasted with simulation results.

The protection strategies which may be used in multi-terminal HVDC grids are reviewed in Chapter 7. A test system is designed and used to investigate fault ride-through for different circuit breaker technology types.

Chapter 2

HVDC Converters and Modelling

2.1 Introduction

The capacity restrictions found with ac transmission, demonstrated in Chapter 1, is a property of continuously charging and discharging the line stray capacitance. When energised with dc no reactive power is drawn as the cable charge is fixed in polarity and magnitude. This leaves the full thermal capabilities of the cable for transmission of real power, significantly improving throughput of the transmission medium. There is no inductive voltage drop during steady state. This makes transmission at dc particularly attractive for long over-head lines, sub-sea or underground cables, where parasitic capacitance begins to significantly restrict transmission capacity.

High voltage DC (HVDC) has been used as an effective tool to connect load centres from remote sources of generation, interconnection of asynchronous ac networks and, in more recent cases, re-enforcement of existing ac networks without the need to construct additional overhead lines, which face heavy resistance to planning applications.

Converter technology can be split into two categories: Line Commutated Converters (LCC) and Voltage Source Converters (VSC). VSC has seen additional developments in the last five years resulting in sub-categories of multi-level and two-level converter systems. The two technologies offer different power levels and suitability for different tasks. LCC tends to be used in larger, long distance, bulk power transmission, such as connection of hydro-electric stations in remote areas. VSC lends itself to smaller scale connections, where space is constrained, for multi-terminal operation or ac networks may be weak. Offshore wind, therefore, presents a perfect application of the technology. They require long sub-sea cables, small converter footprint and there us a desire to integrate several systems together to form a multi-terminal network.

Section 2.2 introduces the line commutated converter, discusses general control theory, its attributes and drawbacks. Section 2.3 gives an overview of VSC technology. Two-level and Multi-level converters are discussed. The topology of each, along with their merits, are described. Section 2.4 describes the models which can be used to simulate the MMC converter. Three types of model are covered: detailed, simplified (single cell/diode) and average. The performance of these in terms of relative simulation speed is also discussed and their suitability to perform the simulation studies required in this thesis determined.

2.2 The Line Commutated Converter

The line commutated current source converter (LCC-CSC) is more commonly referred to simply as a line-commutated converter (LCC) within HVDC applications, which is the terminology used within this thesis from here on. The basic building block of the line-commutated converter is the three-phase, six pulse Graetz bridge shown in Figure 2.1. Losses is low at approximately 0.7% per converter, making the technology attractive for long distnce power transmission [29].

Thyristors are used within each of the six arms to control the voltage applied the dc side. Modern installations operate with dc voltages up to ±800kV. With state of the art devices in the 8.5kV range, a single thyristor device is not capable of providing the required blocking voltage [13]. To overcome this multiple devices are connected in series to attain the required blocking voltage, as shown by the expanded box in Figure 2.1. The string of thyristors is termed a 'valve' and, from the point of view of the converter's control, is operated as a single unit.

Thyristors are three-terminal, semi-controllable devices; that is, they may be switched into a conducting state on-demand (termed 'triggering' or 'firing') but not off again. This stems from the fact that a single current pulse into the devices gate is required in order to innate conduction. In effect, they operate similarly to a high capacity diode, except that they may be triggered to conduct on demand. Once triggered the device 'latches' (continues to remain in a conductive state) until current through it passes through zero. This must be forced by an external part of the circuit, hence the circuit naming (Line Commutated Converter) as it is the ac line voltage and network strength which commutates current from one valve to another. For this reason the converter may not be used to energise a passive network. With no local generation current will not naturally commutate between valves. This makes applications such as offshore wind farms and areas of weak generation challenging for LCC instillations. Static-Compensators (STATCOM) – voltage source converters (VSC) with no real power capacity – or standard VSC can be used to stabilise local ac waveforms to allow LCC to operate in otherwise

poor conditions [19].

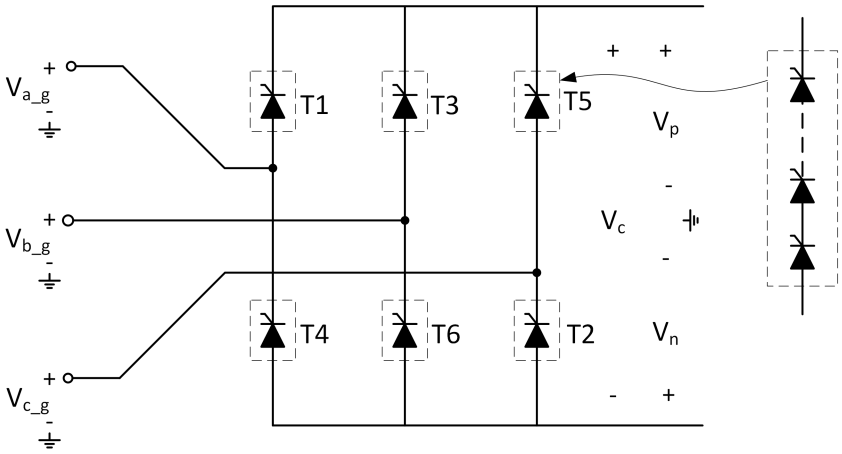


Figure 2.1: Six pulse thyristor controlled ac/dc converter. Each arm contains a string of high-voltage, high-power thyristors connected in series. These are operated as a single unit, often referred to as a 'valve'

The term natural commutation point refers to the point-on-wave where current commutates from one phase to the next in a standard diode rectifier. If thyristor valves are triggered at this point then the dc voltage produced replicates that of a simple three-phase, six-pulse diode rectifier circuit. However, delayed triggering gives a degree of freedom. It changes the the period of which ac line voltage which is applied to the dc side (conduction period) and as a result manipulates the voltage. The delay period is normally measured in degrees, termed the 'firing angle' and denoted as α. The average voltage applied by the bridge over a single cycle is given by (2.1). As the firing angle α is increased the dc voltage generated by the converter is reduced. Figure 2.2 shows examples of the dc voltage generated for firing angles of 10^o and 25^o.

$$\overline{V_c} = \frac{3\sqrt{3}V_p}{\pi}\cos(\alpha) \tag{2.1}$$

Current flow in the converter is unidirectional and therefore the dc voltage must change polarity in order to reverse power-flow. Increasing the firing angle beyond 90^o leads to an negative average voltage, as given by (2.1). Line-commutated converters are typically constructed from two six-pulse bridges connected in series, as shown in Figure 2.3. The use of a three-winding wye-wye/wye-delta transformer causes a 30^o phase-shift between the rectified voltage, which results in a reduction in harmonic content. A smoothing reactor is also placed on the dc side to reduce the current ripple and harmonics induced on the transmission line.

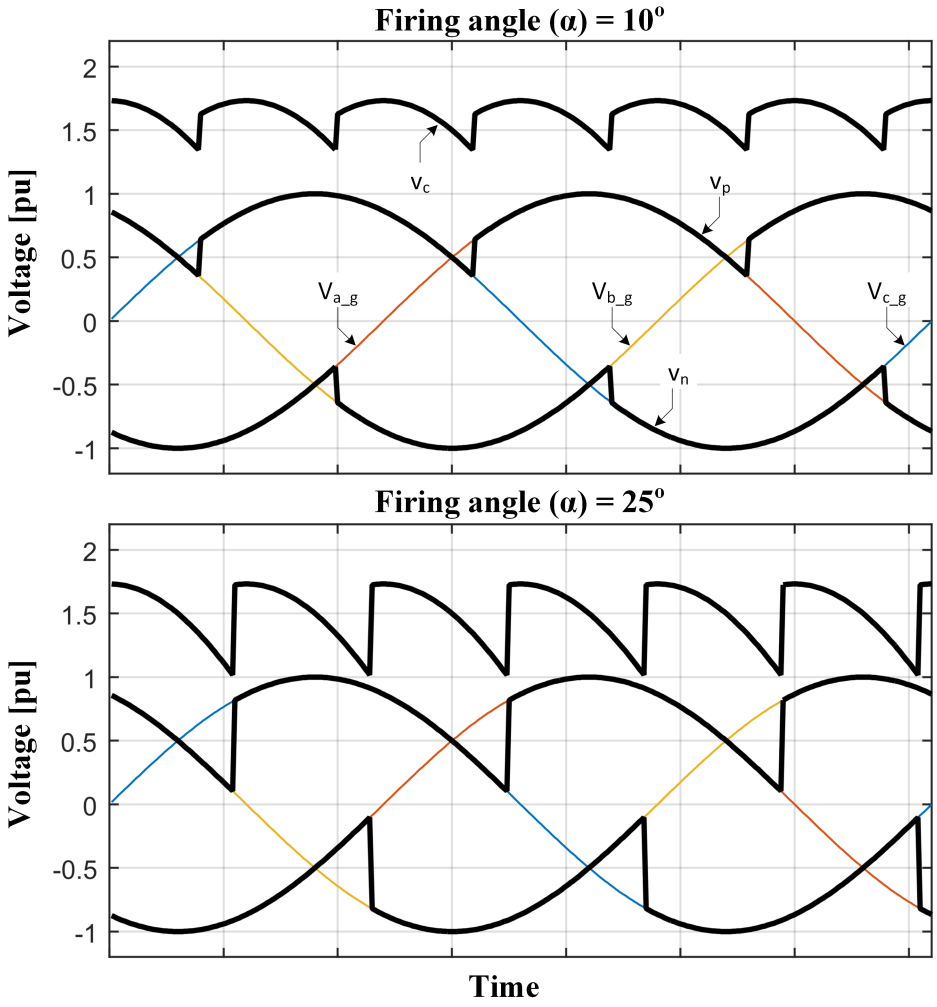


Figure 2.2: DC Voltage produced by a three-phase, six-pulse line commutated converter. Two conditions are shown, $\alpha = 10^o$ and $\alpha = 25^o$, to demonstrate how firing angle effects average dc voltage. Waveforms plotted in Excel based on fundamental thyristor controlled equations [30]. Commutation overlap is not considered in order to simplify the waveforms

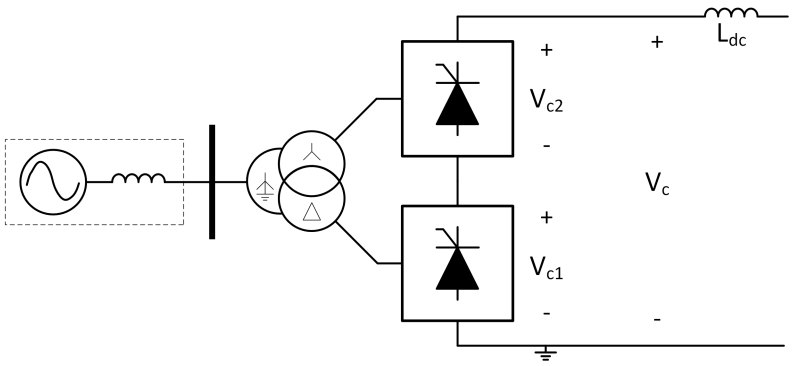


Figure 2.3: Two six-pulse converters connected in series. The wye-wye/wye-delta transformer configuration results in twelve commutations, and current pulses, per cycle, reducing harmonics. The two bridges in series allows also doubles the dc voltage. The combined unit is referred to as the twelve-pulse converter, which is the most common topology for LCC system now constructed

2.2.1 LCC Summary

With the largest systems capable of transmitting 10GW at ±800kV, LCC based HVDC still offers the largest power throughput capability when compared to VSC solutions. Thyristor technology offers higher capacity devices than IGBTs (which are used in VSC systems). Forward voltage is lower, leading to lower conduction losses. Typically, overall converter losses are in the range of 0.7% in comparison to 2-3% for 2-level VSC, although multi-level converter are closing the gap [29]. Thyristors are also much more robust, with devices capable of 6250A during normal operation and surge currents in excess of 140kA [13], which is of particular importance when designing for transient fault currents. However, the converter does suffer from several drawbacks which are described below.

Reactive power consumption Trapezoidal blocks of current are drawn from the ac side, the phase of which is linked to the firing angle. As such, reactive power compensation is required to maintain unity power factor for different operating conditions.

Harmonic content Substantial harmonics are generated by the converter on the ac and dc side. The nature of line frequency rectification means that these are low in frequency and not readily attenuated through the passive impedances of the system (e.g. interface transformer). Tuned filters are required to reduce the THD generated by the converter to an acceptable level for the local network.

Converter footprint The requirement for reactive power compensation and filtering increases the footprint of the converter station dramatically. While the thyristor valves have a high power density in comparison to VSC – reducing the space required for the converter bridge – ancillary filtering/reactive power compensation equipment can occupy in the range of 50% of the converter footprint. For offshore and urban locations this can be particularly challenging.

Strong ac network In order for the converter to commutate current from one valve to the next the local ac voltage must be sufficiently strong. Where system strength is low it is possible that current is not fully commutated out of a valve, resulting in a commutation failures, shoot through and possible device failure. It is not possible for this converter type to be used in passive systems or for black-start operation as it cannot synthesise its own ac voltage output.

Unidirectional current flow Power throughput of the converter is controlled by adjusting the dc side voltage. Changes in power flow direction (i.e. if the converter goes from

exporting power to the dc side to importing it) requires a polarity reversal of the dc voltage. In two terminal systems this can be readily co-ordinated. However, in large networks this is can be problematic and limits the scope of implementation of LCC.

2.3 Voltage Source Converter

The voltage source converter has a similar topology to that of the line commutated converter, in terms of circuit layout, but its operation and control are fundamentally different. Whereas LCC systems utilise thyristors and switch at line frequency, VSC uses the Insulated Gate Bipolar Transistor (IGBT) as the main switching device. As these are fully controllable – they may be switched both on and off on demand – the converter has a wider degree of flexibility in how it is controlled. Where LCC is limited to variations in the firing angle in order to control dc voltage, VSC has the ability to control the ac output voltage directly, and works from a fixed dc supply. The converter has the ability to generate arbitrary voltage output at a given frequency, phase and magnitude. Closed loop current control can then be used to adjust its real and reactive power flow as required.

The topology has been used extensively within variable frequency motor drive applications. In 1997 the first VSC test system was commissioned [31]. At just 3MW, with a dc side voltage of ±10kV, the scheme was very small by typical HVDC standards. Just three years later the first commercial transmission link was installed – linking Gotland, Sweden to the mainland – with a capacity of 50MW and a dc voltage of ±80kV [17]. Early systems were based on the two-level topology, described in Section 2.3.1. The limitations of this topology caused converter capacity to plateau at approximately 400MW, ±150kV, driving more advanced designs and, ultimately, the shift to the modular multi-level converter (see Section 2.3.2) for all new installations [32]. These allowed increased voltage power power levels whilst also removing the requirement for filtering [33] Installations may now be found with power ratings of 1000MW at ±320kV [34], with systems in the planning stage in excess of 1200MW and ±400kV.

2.3.1 The Two Level Converter

The basic structure of the two-level bridge leg is shown in Figure 2.4, which produces a single phase ac output from the dc supply voltage. Each leg (the structure shown in Figure 2.4) comprised of two ‘arms’, one upper and one lower. As individual IGBT devices are limited in blocking capability to approximately 6.5kV many must be connected in series to achieve the required blocking voltages [35]. To ensure adequate dynamic and static voltage sharing across

the devices active control may be necessary. This requires all devices in the string to switch only as fast as the slowest – reducing maximum sqitching frequency – while increasing switching losses [36]. Similarly to the devices in the line-commutated converters, these are operated in unison and referred to as a 'valve'.

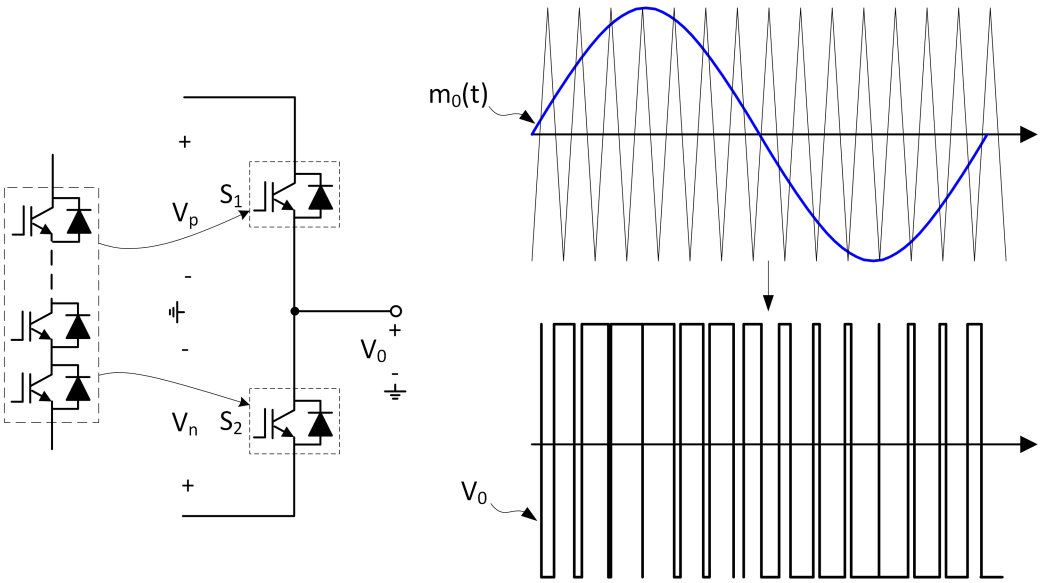


Figure 2.4: The basic 2-Level converter PWM

The valves in each leg are switched in anti-phase to produce a bi-polar output, alternating the output between the positive rail voltage and negative rail voltage. To avoid shoot-through (short-circuit), upper and lower valves of the same phase must not turned on simultaneously. A truth table of switch states and voltage output is given in Table 2.1.

Table 2.1: Switch state truth table of single phase bridge leg. 1 = ON, 2 = OFF. Switch numbers refer to the single phase diagram shown in Figure 2.4

S_1	S_2	V_o	Notes
1	0	$V_p \implies +\frac{1}{2}V_{\mathrm{dc}}$	Positive rail voltage
0	1	$V_n \implies -\frac{1}{2}V_{\mathrm{dc}}$	Negative rail voltage
0	0	–	Blocking state
1	1	–	Invalid state

Through pulse width modulation (PWM) the average voltage over a switching cycle can be controlled in each leg. For a symmetrically balanced system (voltage magnitude on each pole is equal in magnitude with reference to ground potential) the average (fundamental) output voltage is given by (2.2). To control the output the modulation function (m_o) is manipulated. Figure 2.4 shows an example of sinusoidal pulse width modulation (SPWM). The modulation

function, given by (2.3), is compared to the triangular carrier signal to produce a square wave output with varying duty cycle. The modulation index M can be adjusted to control the voltage magnitude; ϕ, the phase angle and ω, the frequency, allowing direct control over the output.

$$v_o(t) = \frac{V_{\text{dc}}}{2} m_o(t) \tag{2.2}$$

$$m_o(t) = M \sin(\omega t + \phi) \tag{2.3}$$

The switched nature of the output results in harmonic distortion of the voltage and current on the ac side. Tuned filters are used to meet harmonic requirements of the ac network. The ratio of switching frequency f_s to modulation frequency f_m influences the magnitude of harmonic distortion produced at the converter output. Typical HVDC converter switching frequencies are in the range of 1-2kHz [37, 29]. Increasing the switching frequency makes harmonics more readily attenuated, requiring smaller filters. However, gains from reduced filtering must be traded-off against the increased losses incurred with a higher switching frequency.

The three-phase, two-level converter used for HVDC applications is constructed from three legs (six arms in total), as shown in Figure 2.5. With SPWM maximum modulation index is limited to 1, resulting in an maximum peak phase output of $\frac{1}{2} \cdot V_{\text{dc}}$. Increasing beyond this result in distortion of the output waveform, inducing additional harmonics. Triplein harmonics can be superimposed on the ac output in order to increase utilisation of the dc supply and increase voltage output (2.4). This is possible as these cancel out in the line-to-line voltage and are not applied to the network side. Modulation schemes such as space-vector modulation induce a third harmonic component and can increase the dc voltage utilisation by up to 15%, reducing current throughput and converter losses [38, 33].

$$m_o(t) = M \left[\sin(\omega t + \phi) + M_{\text{SVM}} \sin(3\omega t + \phi)\right] \tag{2.4}$$

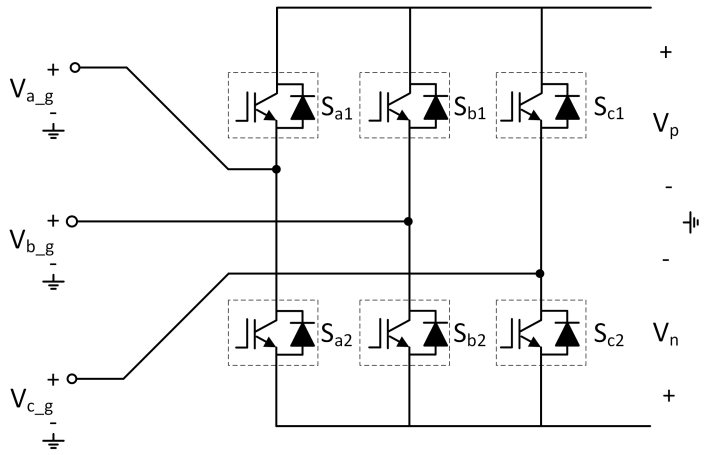


Figure 2.5: Circuit diagram of a three-phase, 2-Level voltage source converter

2.3.1.1 Drawbacks

The 2-level converter has grown in capacity from 3MW in 1997. However, its scalability has proved to be limited, with the largest converters reaching 400MW[32].

Series connection of devices As the dc voltage level increases, in order to increase power throughput, each valve is required to block higher voltages and requires more devices to be connected in series. Matching large numbers of devices is challenging and ensuring voltage sharing with active control limits switching frequency, thus increasing filtering requirements.

DC Capacitance A substantial filter capacitance is required on the dc side, which acts as a large energy store. During dc faults it discharges and causes large currents to circulate through free-wheeling diodes.

Mechanical stress High currents from the filter capacitance discharge during faults can cause mechanical stress [18].

High di/dt Larger numbers of series connected devices leads to larger stray inductances. This can cause increased overvoltages during switching [18].

High dv/dt Grid interface transformers are exposed to the increased dv/dt, stressing insulation requirements[39].

2.3.2 Multi-level Converters

Multi-level converters are able to reduce or eliminate some or all of the issues associated with the 2-level converter. Fundamentally, they are voltage source converters with more than two

output voltages available. In doing so the harmonic content of the output is reduced, thus requiring less filtering on the ac side. Indeed, with a large enough number of levels (typically in the order of several hundred) the need for filters may be eliminated all together [29, 33].

Losses in 2-level converters are dominated by switching loss, due to the high-frequency PWM (see Figure 2.6). The effective switching frequency in multi-level converters is much lower than a comparative 2-level converter (100-150Hz contrasted with 1-2kHz for 2-level [29]), which reduces losses. Estimates of the reduction in loss between 2-level and multi-level vary and are dependant on operating condition (particularly modulation index). However, as a guide losses for multi-level converters are in the range of 1% verses 2-3% for 2-level [40, 29].

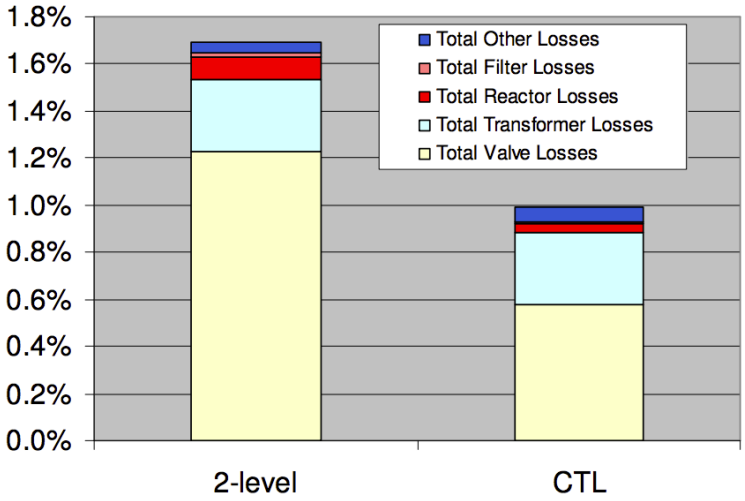


Figure 2.6: Comparison of losses from a 2-level and a cascaded muliti-level converter[37]

There are four key topologies that can be used to construct multi-level converters, which are reviewed in detail by Marquardt [18]. Neutral point clamped (NPC) and flying capacitor circuits have been used within industrial drives applications. However, as Marquardt highlights the scalability of these two topologies is somewhat constrained; parasitic loop inductances can become large and as the voltage level is increased. This can lead to reduced utilisation of the semiconductors and increase in stored energy, which is undesirable. Moreover, the high surge currents which occur during dc faults, and discharge of the link capacitors, cause very high currents, posing a significant mechanical stress due to the high magnetic forces involved [18].

2.3.3 Modular Multi-level Converter (MMC)

The modular multi-level converter proposed by Lesnicar improves upon the scalability and functionality of the diode-clamped and capacitor-clamped topologies [38]. The structure of a single phase, shown in Figure 2.7, consists of two symmetrical arms with the output taken from

the centre point. The upper and lower arms have a number of identical cells, also referred to as sub-modules (SM), connected in series. There are N sub-modules per arm, each containing a half-bridge and capacitor. Each SM capacitor is pre-charged to a nominal voltage of V_{dc}/N.

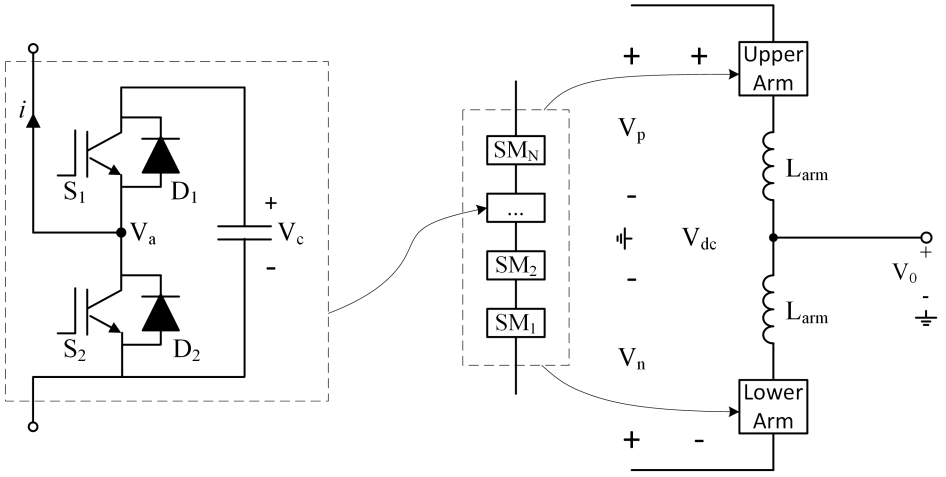


Figure 2.7: Single phase of a modular multi-level converter. Upper and lower arms are symmetrical with N sub-modules in each. Each sub-module is constructed from a half-bridge and storage capacitor. Arm inductors are used to control circulating currents

Valid switching configurations are shown in Table 2.2, where 1 represents the switch gated on and 0 off. During normal operation SM states 1 and 2 are used. In switch State 1 the capacitor in voltage ($V_c \approx V_{\mathrm{dc}}/N$) is inserted in series within the arm. In State 2 the cell is bypassed via S_2 and D_2. What would be State 4 is invalid because it causes shoot-through (short-circuit) of the SM.

Table 2.2: Half-Bridge MMC switch states

SM State	S_1	S_2	$i > 0$	$i < 0$	V_a
1	1	0	S_1	D_1	$+V_c$
2	0	1	S_1	D_1	0
3	0	0	D_2	–	0
			–	D_1	$+V_c$

The voltage across the upper and lower arms is controlled by selecting appropriate number of sub-modules to bypass and insert within both arms, as given by (2.5). In this way the voltage applied to the output can be manipulated. Each SM capacitor is nominally charged to V_{dc}/N, allowing the arm to produce a maximum voltage of V_{dc} with N SMs inserted, and 0 with all SMs bypassed. By controlling the number of SMs on and bypassed in both arms the total voltage across two arms and the output voltage may be controlled. With N SMs per arm, it is possible

to generate N+1 voltage levels at the phase output.

$$v_{\text{arm}} = \sum_{i=1}^{N} V_{\text{cell}_i} \tag{2.5}$$

Given the modular nature of the topology (all SMs are identical), it is possible to construct output voltages with an arbitrary number of voltage levels. An increase in the number of sub-modules does not lead to an exponential increase in the number of devices used (as in diode-clamped topologies), making the circuit scalable and ideally suited to HVDC applications. Each SM can utilise standard devices, with no series connection and voltage sharing required. The number of SMs used within each arm can then be set by the required dc voltage (once harmonic requirements are met). The three-phase circuit is shown in Figure 2.8.

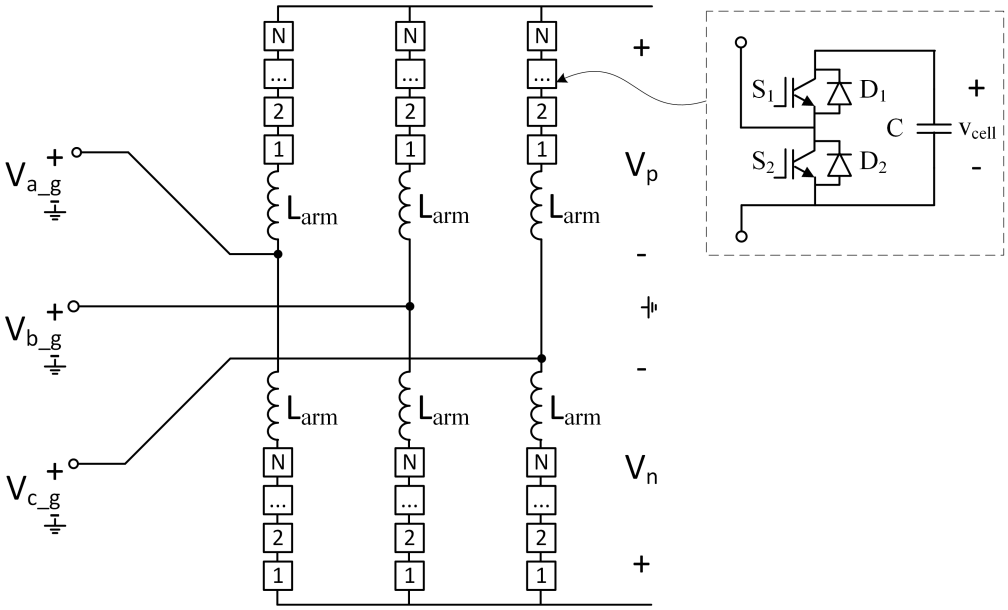


Figure 2.8: Three-phase modular, multi-level converter circuit topology. Each arm contains N identical sub-modules, allowing this converter to generate N+1 voltage levels per phase on the as output

To achieve the desired dc voltage level a large number of cells are required. This is typically in the range of 200-400 sub-modules per arm, depending of device rating and utilisation [41]. Harmonic requirements can be met without pulse width modulation of the sub-modules and a staircase modulation technique can be used to generate the required output. AC filtering is therefore not required [33].

Energy storage is distributed within the SM capacitors and not concentrated on the dc side (as in 2-level converters). The dc voltage is controlled by adjusting the total number of sub-modules inserted from each leg. This has the advantage that the stored energy is not discharged during dc faults as the SMs can be blocked (switch-state 3, Table 2.2). This reduces the surge

current and lowers the energy which must be dissipated by the dc breaker.

In practice there are non-ideal characteristics of the MMC which must be considered. While in the on-state current passing through a SM causes the capacitor charge (and, therefore, voltage) to increase or decrease, depending on the current direction. Cell capacitors are sized so that the voltage ripple is kept within a tolerance, typically 10% of nominal. The change in voltage leads to additional current components, which circulate between converter arms. The inductors placed within each arm impede the magnitude of this current. However, their placement also causes an additional voltage drop between the dc side and the ac side, as they form part of the ac current path. Their size must be optimised to balance the increased voltage drop obtained by reducing circulating current. Typical values are in the range of 15% pu impedance [41].

2.3.4 Fault Performance

Both the two-level (2-level) and the half-bridge modular multi-level converter (HB-MMC) require a minimum dc side voltage to operate. When a reduced voltage occurs (typically during dc side faults) the converter cannot synthesis a voltage large enough to counter that of the ac side source, assuming an ac network with generation. In this case uncontrolled inrush currents occur, from the ac side to the dc side, which can cause damage to the converter, as well as restricting the converter from operating. For both converters, a conduction path is formed through the free-wheeling diodes during dc faults, causing this response. These current paths are shown in Figure 2.9.

Stored energy is distributed between the sub-modules within an MMC, whereas it is lumped in a single dc filter capacitor in 2-level converters. During faults the filter capacitor will begin to discharge, and in doing so introduce a significant amount of additional energy to the fault which must then be removed by circuit breakers. Although MMC is equally susceptible to current in-feed from the ac side it is able to stop sub-module capacitors from discharging. This reduces the energy that the breaker must dissipate whilst also improving restart as the capacitors do not need to be recharged [42].

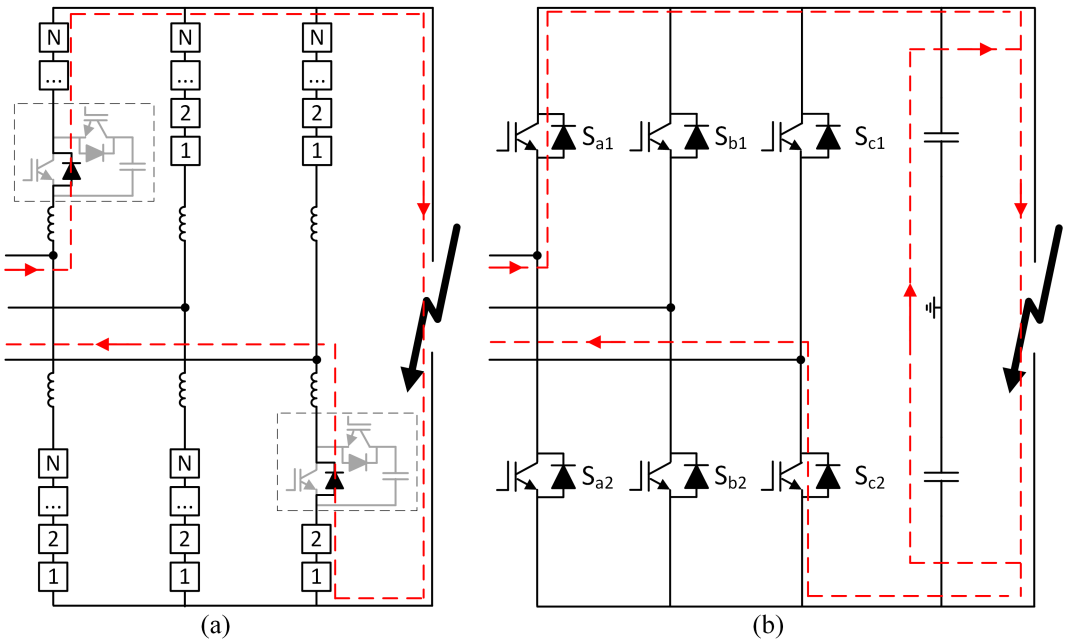


Figure 2.9: VSC fault current paths through free-wheeling diodes in (a) HB-MMC, (b) 2-Level converter

2.3.5 Fault Blocking Converters

During dc side faults the two VSC topologies discussed result in large currents being drawn through the converter from the ac side. If the converters have the ability to block contributions from the ac network, then the requirements for fast-acting dc breakers can be significantly reduced or eliminated, as demonstrated in in [20]. Converter topologies such as the Alternate Arm Converter (AAC) [43, 44], Full Bridge MMC (FB-MMC) [43], hybrid MMC mixed cell MMC [45, 21], and the mixed cell MMC [46] have the ability to perform this duty.

The general principle by which each of the topologies block fault current can be demonstrated readily with the full-bridge MMC topology (FB-MMC), a single phase of which is shown in Figure 2.10. Half-bridge sub-modules in the HB-MMC are replaced with full-bridge equivalents. The sub-modules are capable of the four switching states given in Table 2.3. During normal operation states 1, 2, 3, and 4 may be used. However, to minimise switching losses it is common that state 4 (providing negative voltage) is unused to minimise switching losses. States 1 and 2 create a bypass path for current, with no voltage applied. State 5 provides blocking functionality. Where current passes in the positive direction (from ac side to the dc side, as occurs in HB-MMC and 2-level converters) a voltage of -V_c is applied by the SM to the arm.

When the converter is blocked, the gating to all devices is inhibited (SM state 5). The fault current for the FB-MMC is shown in Figure 2.11. Each SM applies -$V_c \approx -V_{\mathrm{dc}}/N$, as given by state 5 in Table 2.3, with a combined voltage of $-V_{\mathrm{dc}}$ from the arm. The counter-voltage

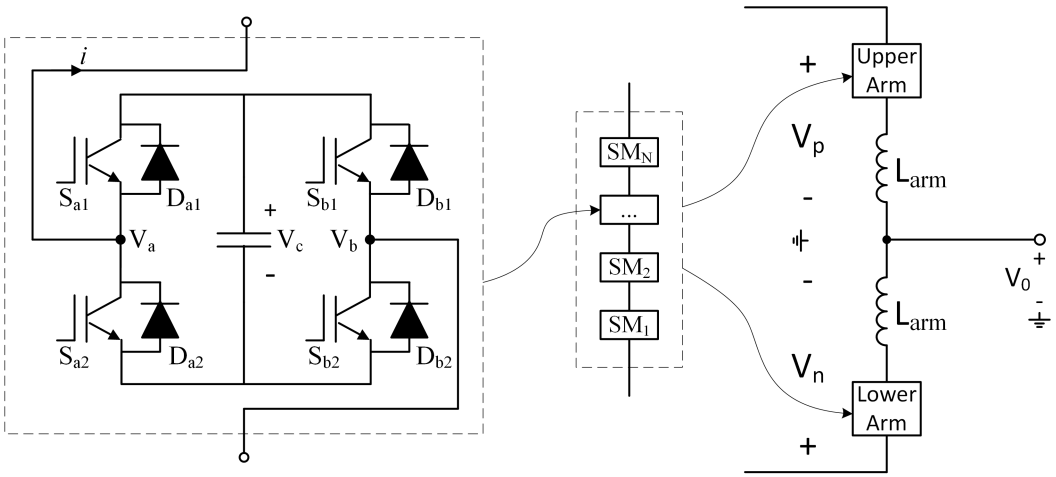


Figure 2.10: Full-bridge MMC topology

Table 2.3: Full-Bridge MMC switch states

SM State	S_{a1}	S_{a2}	S_{b1}	S_{b2}	$i > 0$	$i < 0$	V_a	V_b	V_{ab}
1	1	0	1	0	S_{a1}, D_{b1}	D_{a1}, S_{b1}	V_c	V_c	0
2	0	1	0	1	D_{a2}, S_{b2}	S_{a2}, D_{b2}	0	V_c	0
3	1	0	0	1	S_{a1}, D_{b1}	S_{a2}, D_{b2}	V_c	0	$+V_c$
4	0	1	1	0	D_{a2}, D_{b1}	S_{a2}, S_{b1}	0	V_c	$-V_c$
5	0	0	0	0	D_{a2}, D_{b1}	–	0	V_c	$-V_c$
					–	D_{a1}, D_{b2}	V_c	0	$+V_c$

generated by each arm causes current to rapidly reduce to zero upon blocking.

Along with fault blocking capability, the FB-MMC topology allows an extended range of operation, such as continued operation during reduced and zero dc side voltage, allowing the converter to provide reactive power support during dc side faults. However, the topology requires twice the device count to achieve these additional capabilities, representing an increased capital cost, losses and control complexity [47]. The life-time cost is also affected due to higher conduction losses, although switching losses can be mitigated by reducing the number of switch states used in normal operation (for instance switching between states 2 and 3).

To block fault currents the converter is required to counteract the line-to-line ac voltage. The FB-MM configuration is capable of producing $2V_{dc}$, which is far in excess of this. A compromise can be made through the use of hybrid topologies, where a mix of full bridge and half bridge sub-modules are used in each arm, providing enough counter-voltage to block fault currents [46, 47, 48, 49].

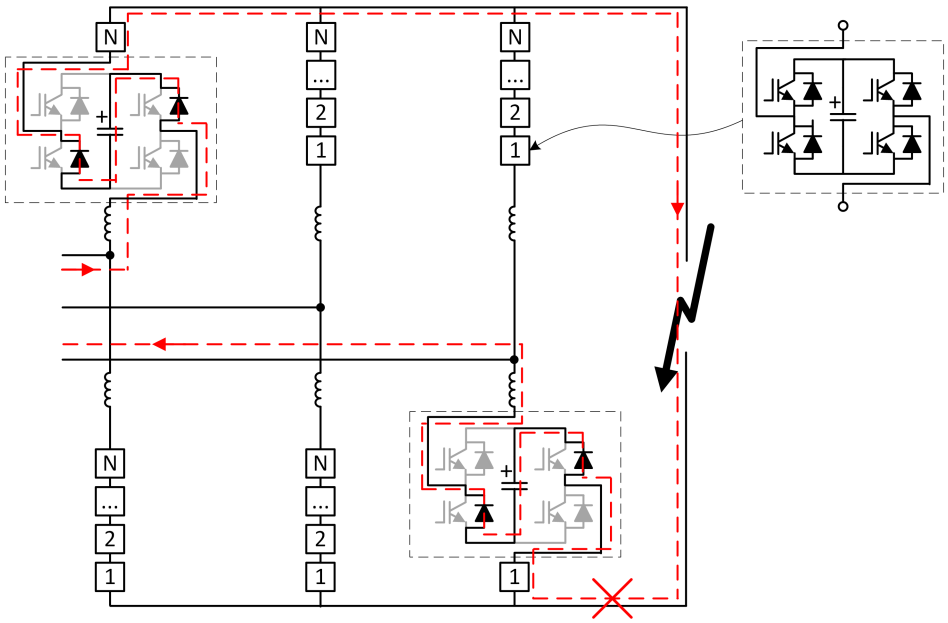


Figure 2.11: Full Bridge MMC under fault. In the blocked state the FB cells provide a counter voltage of $2V_{dc}$, which is larger than the ac source voltage. This rapidly reduces any current flowing in the converter to zero, blocking the fault current.

2.4 Converter Modelling

The converter model used to perform computer simulations must be appropriate to produce the desired results within a reasonable time-frame. The level of detail that is required from the simulation results must be first assessed in order to select and appropriate model to be used. For example, the 2-level converter consists of several hundred individual IGBTs within each arm connected in series. Simulation software such as SPICE allows accurate representation of device level characteristics and is appropriate for modelling the fast switching transients, voltage sharing and over-shoot that occur during PWM operation.

Detailed modelling at the device level presents two major constraints when performing analysis at the system level. Firstly, the ability to create control loops and logic in simulation software such as SPICE is very limited. Secondly, all devices are replicated across multiple converters. In larger, interconnected networks this significantly increases simulation time. For the studies carried out within this thesis, it is the system level response which is being observed. The model must allow pre-fault conditions to be set, accurate representation of fault current transients and mimic controller action during restart. Information on the switching transients is not required and therefore a reduced complexity model may be used.

2.4.1 Detailed Model

In the context of this thesis a switching (detailed) model is one that replicates the switching action performed by the half-bridge cells within the MMC. In its most detailed form each cell is modelled. However, in some cases a reduced number of cells may be used. The switches themselves can be modelled as ideal or represent the nonlinear current-voltage characteristics found in the physical devices. The level of details in constructing the model will depend on the required level of accuracy and the type of study being performed. For example, accurate studies on losses require detailed models of individual switches, i.e. non-linear characteristic curves. Analysis on capacitor balancing techniques does not require such low level detail and idealised switches will likely suffice.

A 401 level detailed model is presented by Peralta in [41]. Figure 2.12 shows a schematic diagram of a single converter used in the simulated model. Peralta simulated a 1000MW two terminal system with a dc voltage of ±320kV. This required 4800 individual switches per converter, and an equivalent number of diodes. The large number of devices makes the model computationally intensive. Table 2.4 gives a comparison of simulation times between the detailed model and average model presented by Peralta.

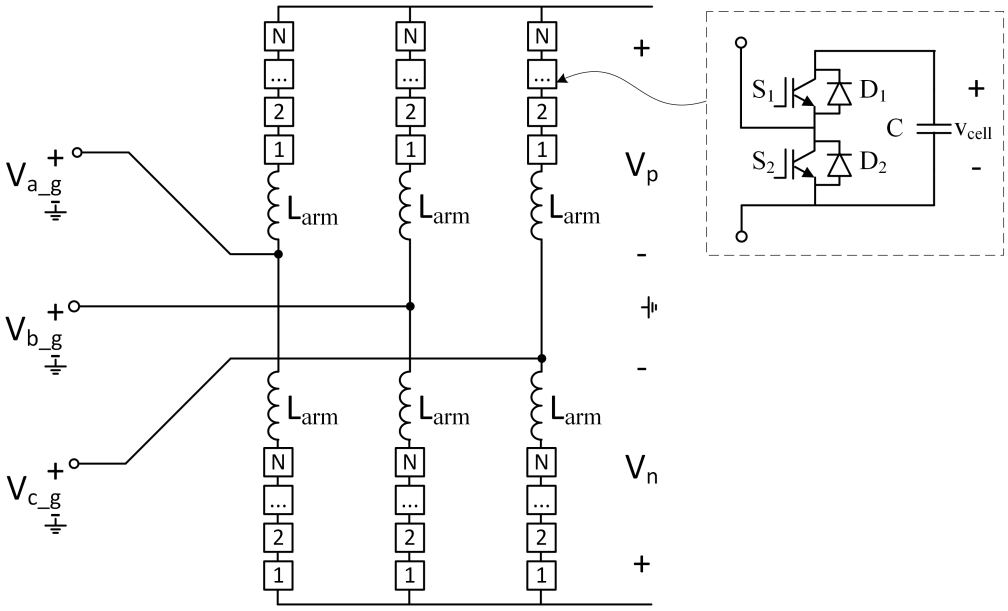


Figure 2.12: Schematic diagram of detailed model

The complexity of the detailed model makes it unattractive to simulate large, multi-terminal networks, as the simulation time is excessive. In this thesis accurate information on losses, capacitor voltage ripple etc. are not of prime importance. The primary focus is to investigate the stress placed on the circuit breakers, interaction between converters during fault interruption

Table 2.4: Times taken to simulate a 1000MW, ±320kV system for three seconds using a 401 level detailed and a average model [41].Simulation performed using EMTP-RV.

Model Type	Simulation time step [μs]	Simulation time [s]	Simulation time [h:mm:ss]
Detailed Model	20	25,292	07:01:32
	40	12,929	3:35:29
Average Model	20	69	0:01:09
	40	37	0:00:37

and the impact circuit breaker technology has on fault ride through. For these purposes the detailed model provides a level of detail not required. Moreover, it also presents a significant burden in terms of simulation time required, making parametric studies difficult. For these reason the detailed model is not used.

2.4.2 Single Cell, Diode only Model

The detailed model can be simplified using two assumptions. Firstly, that the converter is blocked immediately after a fault takes place. Secondly that the pre-fault current within the network and converter is negligible when contrasted to the contribution of fault current from the ac side. A post-fault single cell, diode only model was presented in [50]. A single cell is used within each arm, with two diodes (the two free-wheeling diodes from a HB cell) and a capacitor. This replaces all sub-modules in each arm which are used within the detailed model, reducing the circuit complexity significantly. Figure 2.13 shows the circuit layout of a single converter. The topology represents the current paths that can occur when current flows from the ac side to the dc side under dc faults. The inclusion of the capacitor and second diode allows replication of the current path that can occur when the dc link is overcharged (if surge arresters are not used). The single cell, diode only model is therefore the most simplistic model for fault analysis.

As the cells contain only diodes, the converter is unable to influence control over the current flow through the converter. It is also unable to regulate the dc voltage. In order to replicate pre-fault conditions as accurately as possible, fixed sources are used to charge the dc side cables prior to the fault being initiated. These are then isolated from the system once the fault occurs.

The reduction in circuit complexity significantly increases simulation speed, making it particularly suitable for parametric fault studies. Sample simulation times when compared to a 21 cell detailed model are given in Table 2.5. This reduction in simulation speed can be attributed to two areas. Firstly, the electrical circuit is greatly simplified as the number of components

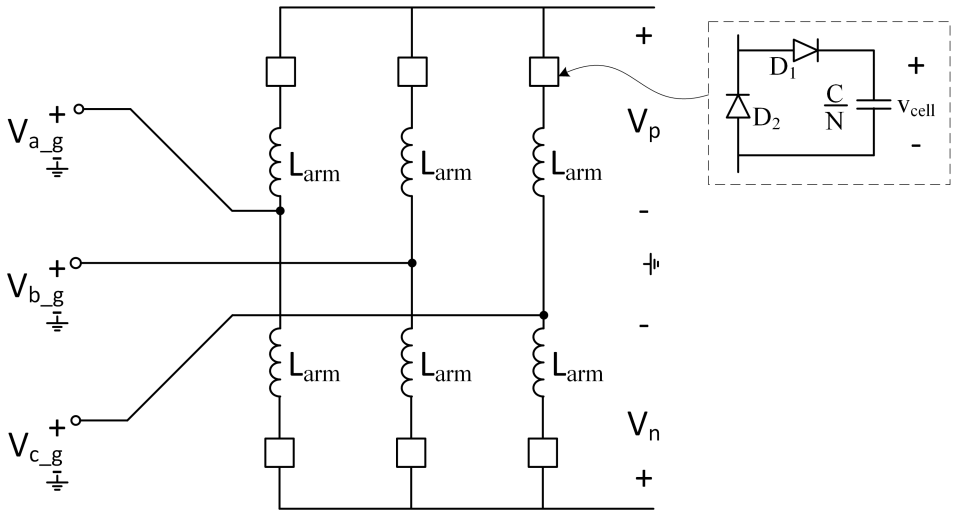


Figure 2.13: Schematic diagram of single cell, diode only model circuit topology [50]

is reduced by orders of magnitude. This makes it easier for the simulation software's internal solver to estimate the next state each time step. Secondly, as there are no switching devices there is no need for controllers to be implemented in software. The result is a significant reduced in computing power required. With no control the converter is initiated quickly (as Table 2.5 demonstrates), further reducing simulation time.

Table 2.5: Comparison of times taken to perform a 27 case parametric using a diode and 21 cell detailed model [50]. Simulations are performed using Matlab Simpower Systems

	21 Cell		Single Cell	
Initiation time	750	[ms]	20	[ms]
Total time simulated	900	[ms]	170	[ms]
Real time per ms of simulated tme	2180	[ms]	13	[ms]
Real time to simulate fault case	33	[min]	2	[s]
Real time to simulate 27 cases	14:45	[hh:mm]	54	[s]

The simplicity of the electrical model, combined with the lack of any control blocks, significantly increases simulation speed. The single cell, diode only model can, therefore, be used to perform a large number of simulations in a short space of time. This is attractive for parametric studies for component optimisation within the circuit. However, the pre-fault current conditions within the arms and on the ac and dc side are not replicated, which can influence the magnitude of resulting fault current that flows (the effect of pre-fault conditions is studied in detail in Chapter 6). As the model only mimics the action of the HB-MMC during fault, when the converter is already blocked, it is only applicable to dc fault studies and cannot be

used to investigate system interaction and post fault clearing re-start sequences. It is therefore not appropriate for the range of studies required within this thesis.

2.4.3 Average Model

Simulating multi-terminal systems, with several converters, is computationally intensive when using a detailed model. The interaction between the converter and the ac and dc networks is little effected by the switching operation of the individual converter cells. The single cell, diode only model is much faster to simulate, but does not provide have the capability to simulate system recovery and reconfiguratation. The average model proposed in [51] provides a balance between simulation speed and functionality of the two models. However, not all current paths during abnormal or fault conditions are replicated.

The average model used within this thesis is shown in is shown in Figure 2.14b. Each arm contains a single virtual cell, which consists of a controllable voltage source paired to a current source and capacitor. The voltage source output depends on the virtual cell voltage and modulation function (2.6). The voltage applied is analogous to the number of sub-modules being applied in their non-bypass state. As such, it can generate at minimum 0V and and maximum V_{cell}. The virtual cell capacitance, and current through it, is scaled to maintain the same stored energy as present in the detailed model (2.7).

The controllers used to generate the modulation function typically operate in the dq reference frame and space vector control may be used [52]. Third harmonic injection and second order current suppression may also be included. This can lead to a complex, composite modulation function. However, simple sinusoidal plus dc offset modulation strategy can be used to demonstrate the principle operation of the HB-MMC, in an an open loop manner. In this case the modulation function is given by (2.8).

$$v_o = m(t)v_{\text{cell}}(t) \tag{2.6}$$

$$i_{\text{cell}} = m(t)i_{\text{arm}}(t) \tag{2.7}$$

$$m(t) = \frac{1}{2}\left(1 + M\sin\left(\omega t + \phi\right)\right) \tag{2.8}$$

The average model presented also has the functionality to replicate fault currents through the converter, by virtue of devices S_1, D_1 and D_2. If the converter is blocked (due to a fault being detected) then S_1 is turned off and the modulation of arm voltage and average cell current is set to unity. This has the effect of placing the virtual capacitor in series with the arm and

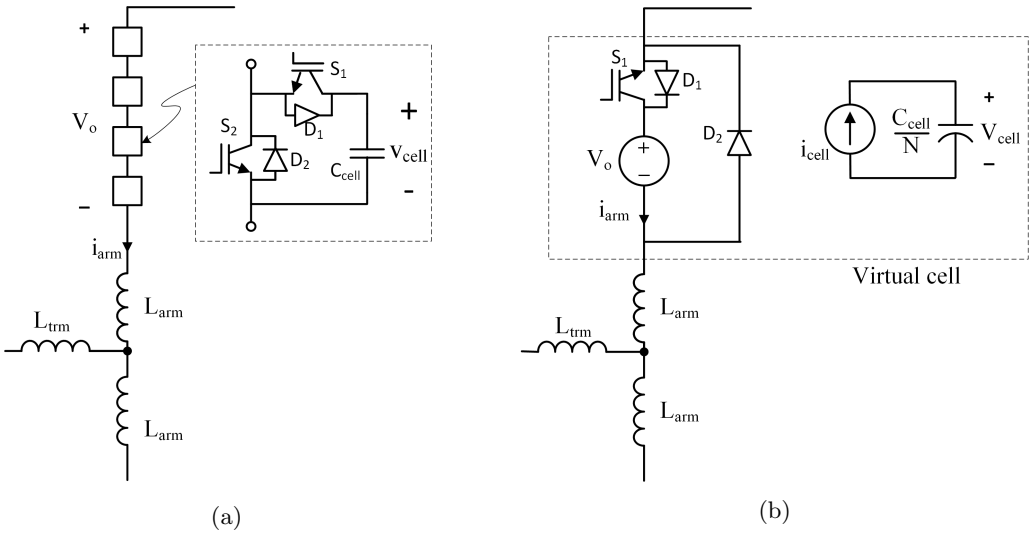


Figure 2.14: Modelling of sub modules (SM) in a HB-MMC arm. (a) detailed model approach. (b) Average value model of an arm, including fault-current paths during blocked state

D_1. Current will only flow into the capacitance when the voltage across the arm exceeds the cell capacitor voltage (nominally V_{dc}). In this case, it flows through D_1, replicating the current path in the switched cells (see Figure 2.14a). Fault current from the ac side can flow via D_2, replicating the current path in the switched cells (see Figure 2.14a). Virtual cell logic for fault compatibility is shown in Figure 2.15.

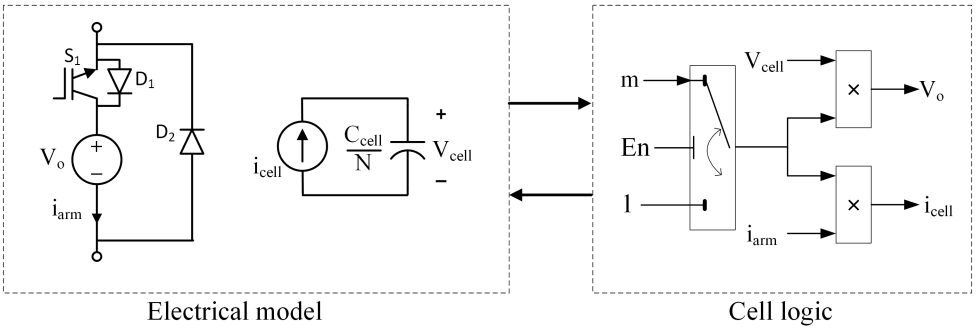


Figure 2.15: Average cell model with blocking capability

2.4.4 Converter Models Summary

Each of the converter models are applicable to different types of studies. The primary focus of this thesis is to observe the influence of converter control and protection strategy on fault-ride through of a multi-terminal system. Harmonic content, capacitor balancing algorithms, loss calculations etc. are not a primary focus. The level of fidelity produced by the detailed model is therefore not required. The single cell, diode only model can be used to estimate the peak

current and other stresses placed on the converter readily, for large ranges of converter conditions. However, it does not allow pre-fault conditions to be included and, more importantly, it does not allow the influence of converter control and re-establishment of power flow to be studied. The average model provides the appropriate amount of control, whilst also providing reasonable simulation times. Therefore it is ideal for the simulation studies required in this thesis and is used from here on.

Chapter 3

DC Faults

3.1 Introduction

DC faults can occur for a variety of reasons: insulation break down, bus bar short circuit, mechanical damage (e.g. anchor drag of a sub-sea cable) etc. Due to their low impedance, faults spread rapidly and voltage throughout the network collapses. Reduced dc voltage can cause disruption to power flow as well as significant fault currents occuring within the converters. In line commutated 'classic' HVDC systems a surge of current (typically in the order of 2.5pu) is experienced temporarily, but may be brought under control by adjustment of the firing angle within a single cycle [53]. The short term over-current capability of thyristors (used within LCC) means that dc faults pose little danger to the converters. Voltage source converters (VSC) are much more susceptible to damage from dc side faults [42, 54, 55, 56]. Reduced dc voltage causes current to flow through free-wheeling diodes, over which the converter has no control. Fault current is severe and, depending on the fault condition, may be continuous, requiring ac or dc circuit breakers to operate.

In this chapter an overview of dc faults, in relation to HB-VSC based HVDC systems, is given. Section 3.2 reviews the susceptibility of VSC to dc side faults. The test system used to demonstrate the impact of dc faults is described in Section 3.3. Section 3.4 gives a theoretical analysis of pole-to-pole faults which are validated through simulation results. Section 3.5 a theoretical analysis of pole-to-ground faults is given which are validated through simulation results. Simulation results are then given for two cases: where insulation coordination is considered (by means of surge arresters at cable ends) and where it is not. In section 3.6 the factors influencing the contribution of fault current from the converter are analysed.

3.2 Vulnerability of VSC to dc Faults

Within an HVAC system the amount by which voltage is suppressed during faults depends on the fault location and impedance of the network. The impedance provided by long conductors (over-head lines and cables) and transformer leakage inductance reduces the voltage sag further from the fault, meaning that locations far from a fault may only see a small voltage dip. As a result the impact to more distant areas of the network can be small. However, the impedance of the network is much lower within HVDC systems and the voltage drop spreads throughout the entire dc network, effectively reducing the pole-to-pole dc voltage at each converter to zero.

In order to control current flow, half-bridge modular multi-level converters (HB-MMC), such as that shown in Figure 3.1, require dc voltage to exceed that of the ac [42]. When peak line-to-line ac voltage at the converter exceeds the dc voltage current will conduct through cell free-wheeling diodes. The point at which this occurs (when peak line-to-line ac voltage matches dc side voltage) is termed the *critical voltage*. A current path is created between the two phases with the largest line-to-line voltage, conducting through a corresponding upper and lower arm (see Figure 3.1). Current will then commutate between each of the arms as the polarity of line-to-line voltage changes during each cycle.

Faults are broken into two categories: pole-to-pole (P2P) and pole-to-ground (P2G), as shown in Figure 3.1. VSC based systems installed to date are predominatly have a floating monopole topology, due to the voltage constrains of current cable technology. This allows double the pole-to-pole voltage, and therefore capacity for the same rated current, over a grounded monopole system. Given this, floating monopole systems are analysed throughout this thesis, which leads to fundamentally different fault current and voltage profiles between P2P and P2G faults.

Probabilities of different fault types occurring within HVDC system are difficult to obtain from in the public domain. However, single phase ac faults can be seen as analogous to single P2G faults in an HVDC system and phase-to-phase faults within an ac system analogous to P2P within HVDC. Frequency of fault type occurrences for ac systems are given in Table 3.1 [57]. Extrapolating from this, P2G faults are much more likely to occur. However, as will be shown in the following sections P2P faults result in much higher peak currents through the converter and dc breaker and must be investigated fully. The following sections discuss the nature of both fault types and the voltage and current stress placed on the converter as a result.

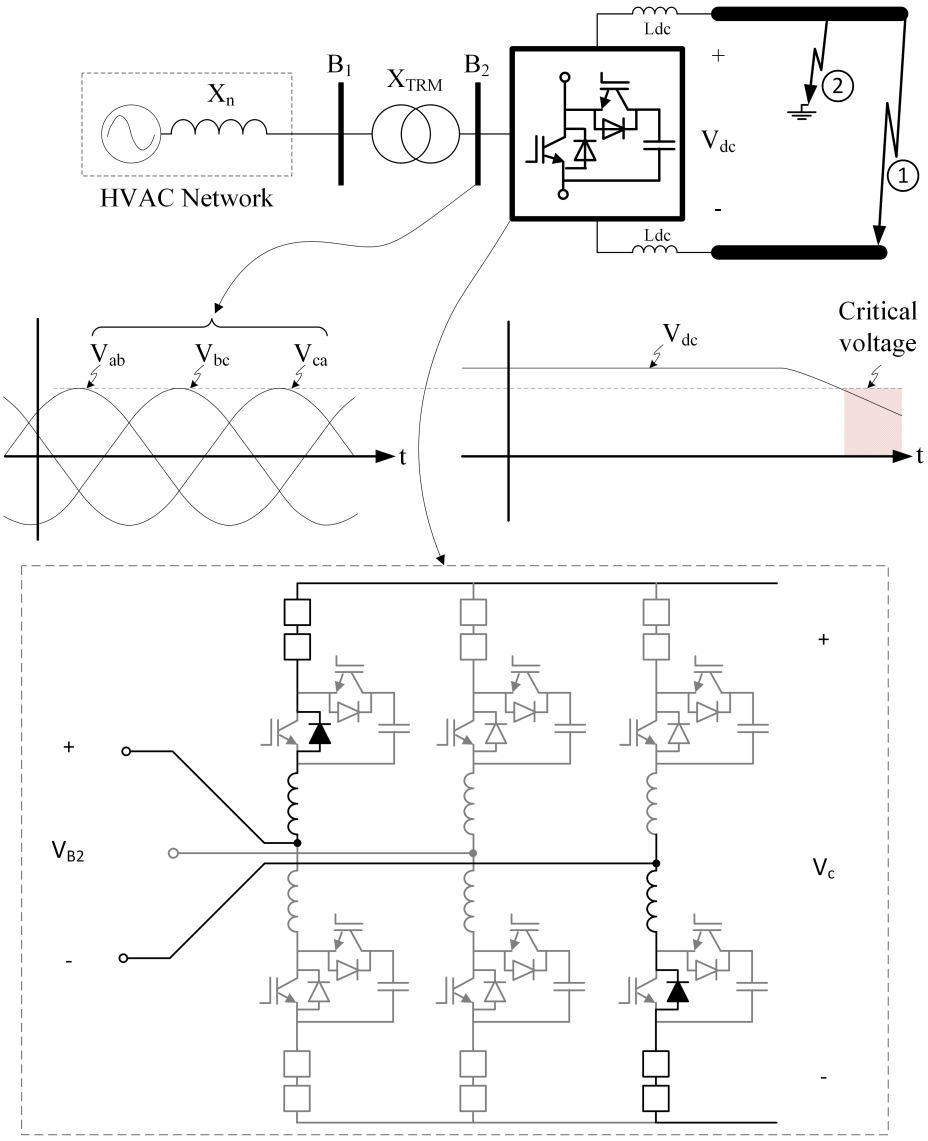


Figure 3.1: Critical dc voltage and resulting uncontrolled ac to dc side current flow

Table 3.1: Fault occurrences by type, for AC overhead lines

Fault type	Probability of occurrence
Single phase to earth	85%
Phase to phase	8%
Phase to phase to earth	5%
Symmetrical fault	2%

3.3 Test System

In the following sections theoretical cases are contrasted with those simulated. The test system used is shown in Figure 3.2. The two HB-MMC converters and ac networks are identical. System parameters are given in Table 3.2. In each simulation case VSC1 operates under P/V_{ac} control, with a reference power flow of +500MW to the dc side. VSC2 operates in V_{dc}/V_{ac} control.

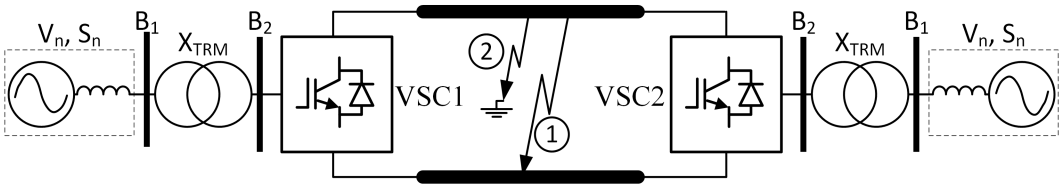


Figure 3.2: Test System

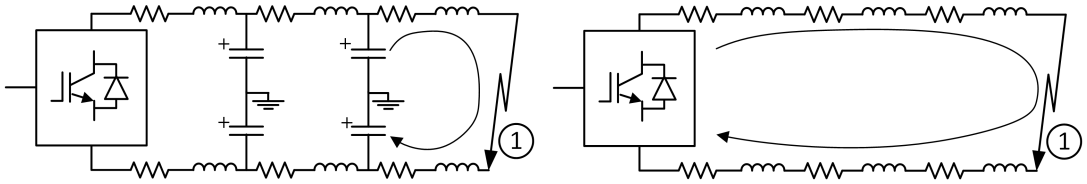
Table 3.2: System Parameters

	Parameter	Value	Notes
S_n	Network strength	10GVA	Short Circuit Capcity (SCC)
V_{B1}	Bus B1 voltage	400kV	Nominal, line-to-line RMS
V_{B2}	Bus B2 voltage	375kV	Nominal, line-to-line RMS
S_c	Rated power of converter	1000MW	PF = 0.95
V_{dc}	Nominal dc voltage	700kV	Pole-to-pole
X_{TRM}	Transformer leakage	0.20pu	
L_{arm}	Arm inductance	0.10pu	Referred to B2

3.4 Pole-to-Pole Faults

As will be shown in this section, P2P faults are more severe from a protection and stress perspective than P2G faults and, therefore, must be analysed in detail. However, as Table 3.1 indicated they are much less likely to occur. Figure 3.3 shows a converter with a section of line, of arbitrarily length, modelled as RLC Pi-sections. When a P2P fault occurs the parasitic cable capacitance will discharge into the fault and the voltage on both positive and negative poles will rapidly decay (Figure 3.3a). The reduction in voltage and associated rise in current will cause the converter to automatically block. Current is then drawn from the ac network through the converter in a similar fashion to that of a diode rectifier circuit with a suppressed dc voltage (Figure 3.3b).

Figure 3.4 shows simulation results of a pole-to-pole fault. The fault is placed at the mid-point of the cable 0.5 seconds into the simulation. As described by the theoretical analysis, dc voltage rapidly collapses after the fault occurs. Current is drawn through the converter to feed the fault, stressing semiconductors within the arms. In the example given, peak currents through the arms (and therefore diodes) are repetitively in excess of 6kA. When contrasted with the typical diode RMS current rating of 1200A, this represents a severe stress and cannot be sustained for long periods. Appropriate action must therefore be taken to protect the devices 4.3.



(a) (b)

Figure 3.3: Pole-to-pole fault characteristics: (a) initial capacitor discharge, (b) steady-state

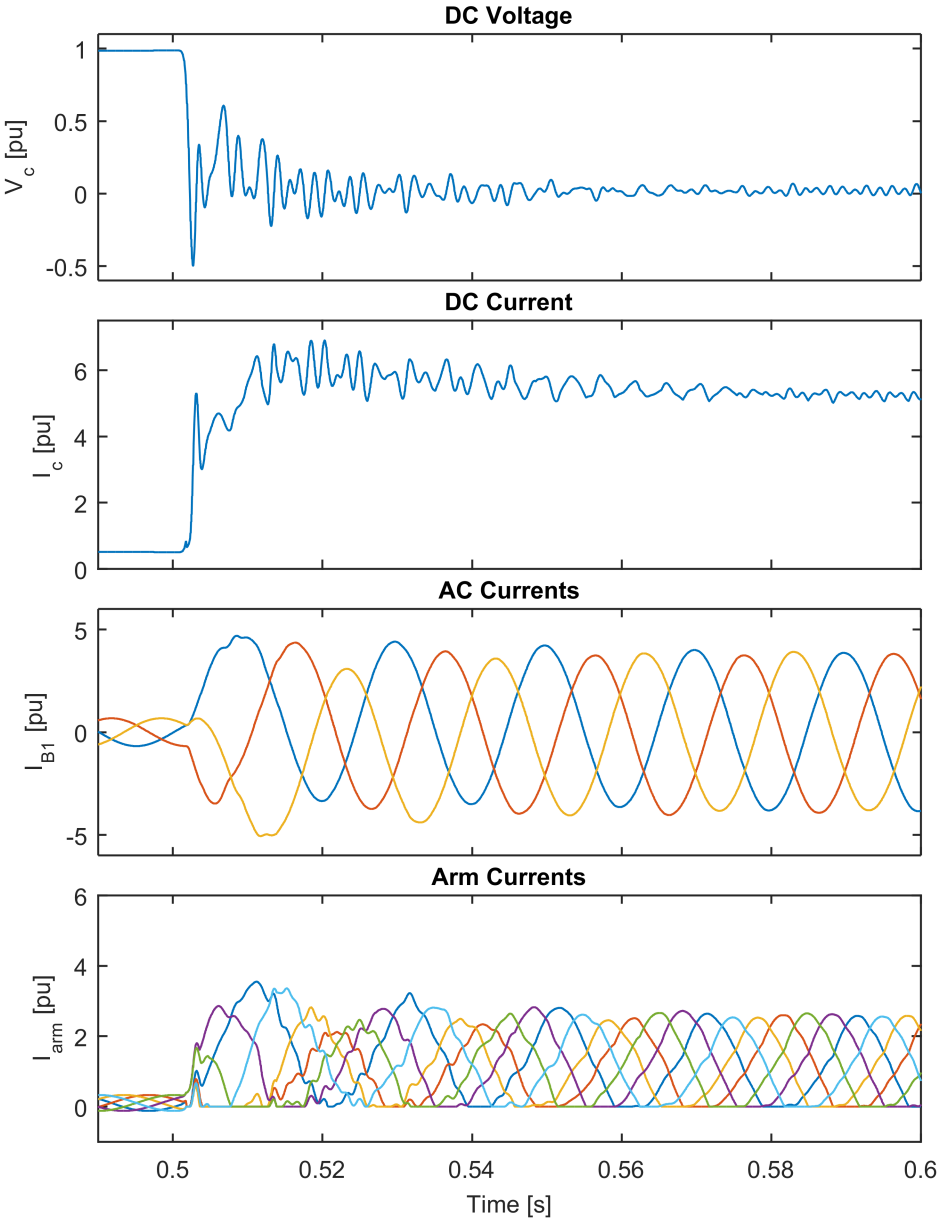
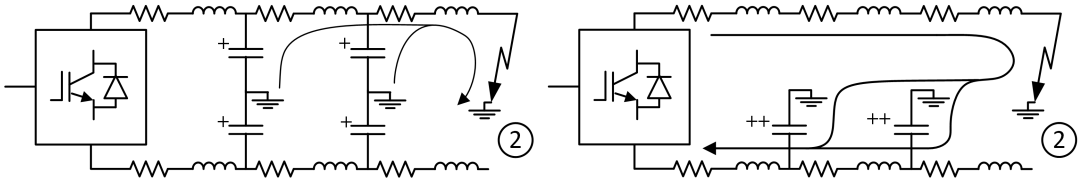


Figure 3.4: Simulation results for a typical pole-to-pole dc fault. Base values: $V_c = 700\text{kV}$, $I_c = 1428\text{A}$, $I_{\text{B1}} = 1443\text{A}$, $I_{\text{arm}} = 2350\text{A}$

3.5 Pole-to-Ground Faults

Figure 3.5 illustrates the sequence of events during a P2G fault. Although the following example is for a single positive P2G fault the principle is exactly the same for negative P2G faults, provided the system is perfectly symmetrical. To observe the natural response a balanced monopole system with no cable surge arresters is used. This allows the dc side to float relative to ground potential. It is assumed that the parasitic current leakage within the cables is balanced, leading to a symmetrical voltage the cables prior to the fault occurring. When a fault occurs cable capacitance will discharge through ground (see Figure 3.5a). The reduced dc voltage will draw current from the ac network which is circulated through the converter and fault. Current will feed to the dc side, increasing the charge on the healthy pole, until pole-to-pole dc voltage has been recharged to the critical voltage (see Figure 3.5b).



(a) (b)

Figure 3.5: Pole-to-ground fault characteristics: (a) initial capacitor discharge, (b) steady-state

The response of the system depends on insulation coordination. To observe the impact this has, two sets of simulation results are given. In the first, the dc cables are allowed to float relative to ground. In the second, metal oxide surge arresters (MOSA) are installed at the cable ends.

3.5.1 Simulation results : without surge arresters

Figures 3.6 shows simulated waveforms for a P2G fault placed 50km away from VSC1, 0.5 seconds into the simulation. The test system shown in Figure 3.2 is used to perform the simulation, with system parameters given in Table 3.2.

The fault results in a rapid decay in pole-to-pole voltage at the converter terminals. The converter is blocked after detecting the fault. Temporarily, additional current is drawn through the converter, in an uncontrolled manner, to increase the charge on the negative pole. The increased voltage which results raises the pole-to-pole voltage sufficiently to allow the converter to regain control. Subsequently, voltage sharing on the two poles asymmetrical, causing phase-to-ground voltages at the secondary side of the transformer to include a $V_{dc}/2$ superimposed

dc component. The converter is re-enabled and current flow is re-established within the arms.

Theoretically the converter is able to re-establish control again, once the current surge has decayed and voltage has stabilised. However, the system insulation is severely stressed; the healthy cable experiences twice rated voltage (as shown in Figure 3.6) and transformers have dc stress components superimposed. This additional voltage stress throughout the network would require system insulation coordination to be revised. In reality the system would be required to shut down until full voltage could be restored.

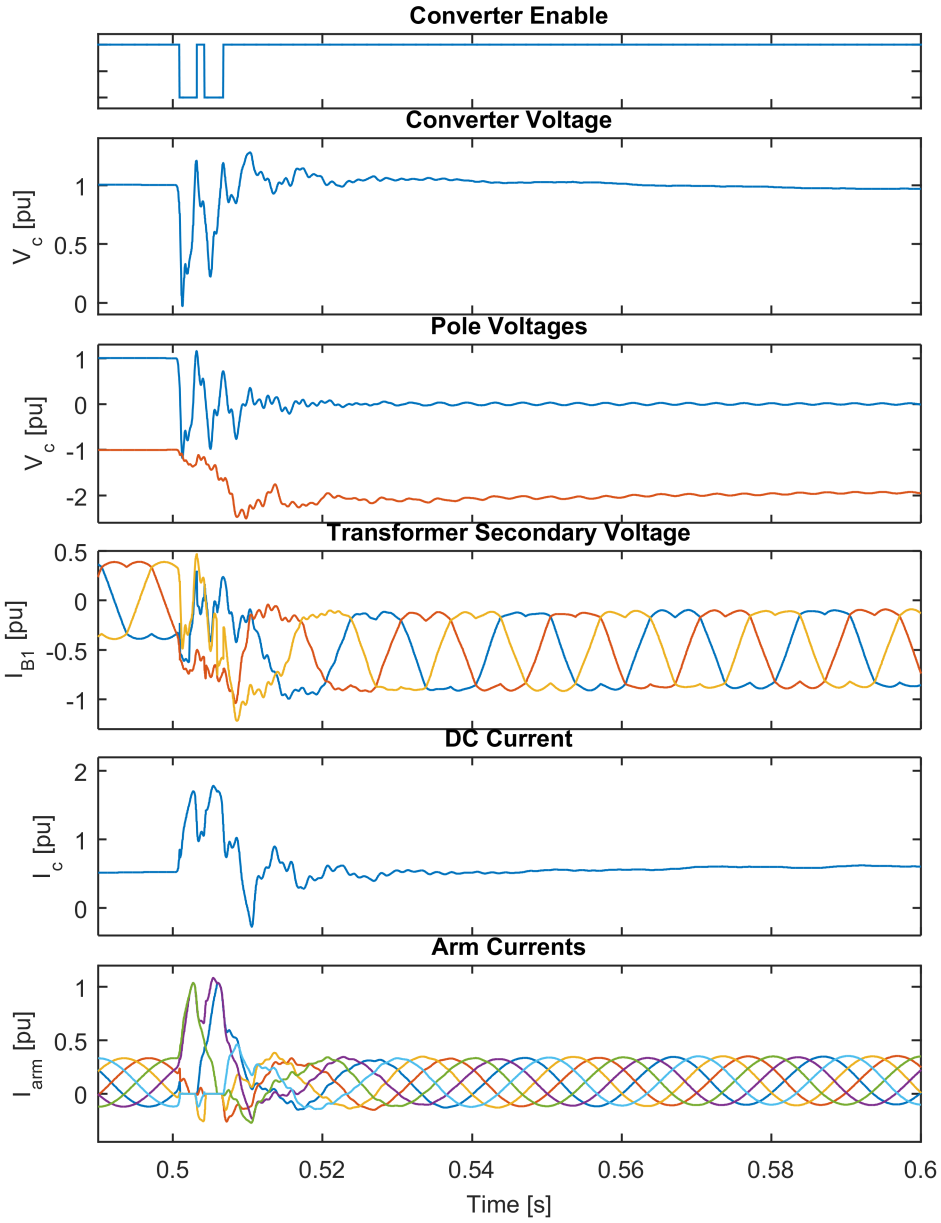


Figure 3.6: Simulation results for a typical pole-to-ground dc fault, with no surge arresters. Base values: $V_c = 700\text{kV}$, $I_c = 1428\text{A}$, $I_{\text{B1}} = 1443\text{A}$, $I_{\text{arm}} = 2350\text{A}$

3.5.2 Simulation results : with surge arresters

Practical systems include metal oxide surge arresters (MOSA) at cable ends to control over-voltage during system transients and faults[58, 59]. For HVDC systems these are, typically, set to 1.5pu of the nominal voltage, in line with the rest of the system insulation coordination. The demonstration system used within this chapter has a nominal voltage of ±350kV on each cable and MOSAs are set to constrain the voltage to 525kV. During normal operation these surge arresters will have minimal leakage current as their clamping voltage is significantly higher than the operating voltage of the cable. However, system voltage is redistributed asymmetrically between the cables during faults. The test system shown in Figure 3.2 is updated to include the surge arresters (Figure 3.7) and the simulation case repeated.

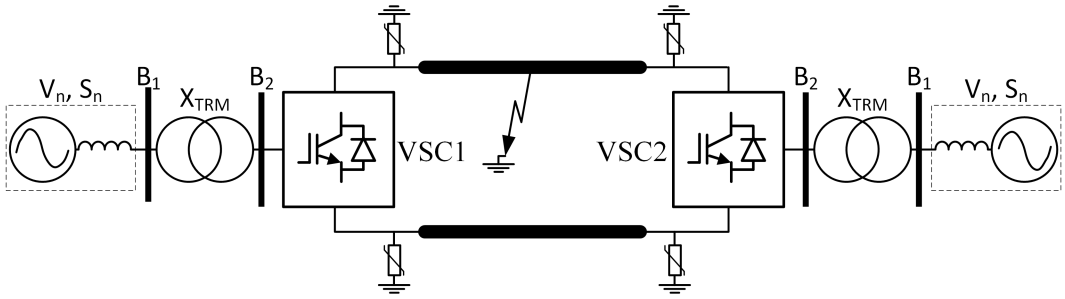


Figure 3.7: Pole-to-ground test system. Surge arresters are placed at each cable end. A positive pole-to-ground fault is placed 50km from VSC1

A positive pole-to-ground fault is placed 50km from VSC1, 0.5 seconds into the simulation. Figure 3.8 shows the waveforms that result. The positive pole voltage collapses to a mean zero rapidly with large, damped oscillations due to the line resonance. The voltage on the negative pole is constrained by the surge arrestor (in the previous case, without surge arresters, its voltage increased to 2pu). The converter cannot continue to operate due to the reduced pole-to-pole voltage. The surge arrester acts as a clamp on the dc side voltage, causing current to be drawn continuously from the ac side to the dc side even when the converter is in the blocked state. The continuous energy dissipation in the surge arresters is unacceptable. AC breakers must be operated to clear the fault to protect system equipment from damage. In this case the system is then no longer able to operate and transmit power.

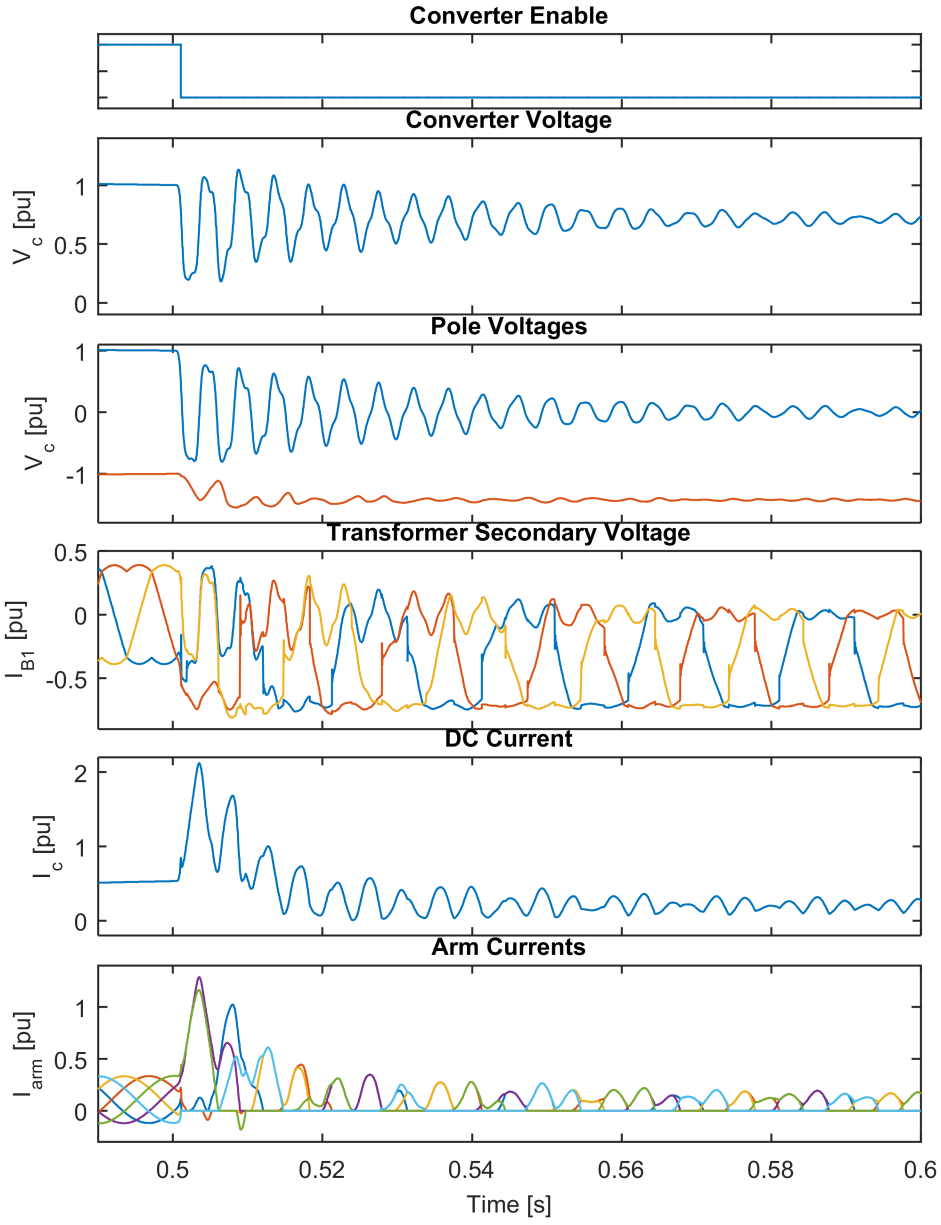


Figure 3.8: Simulation results for a pole-to-ground dc fault with surge arresters placed at cable ends

3.6 Fault Analysis

Following pole-to-pole faults current rapidly rises through the converter, as Figure 3.4 demonstrated. The period of 2ms to 20ms directly after the fault is critical, as this is the time-frame for which potential dc breakers could clear the fault before peak current or total system voltage collapse. If breakers are not operated, current can exceed that possible in steady-state in this short of space of time.

The contribution of current from the converter terminal in 2-level systems is dominated by the reservoir capacitor discharge, slowing the collapse in voltage. Subsequently, the contribution of current from the ac side over the time frame of circuit breaker operation is minimal. In MMC based systems cell capacitors cannot discharge when the converter is blocked and, with no additional capacitance on the dc side, voltage collapse is more rapid. As such, the fault current contribution from the converter terminal is now dominated by the that from the ac side. Estimating the fault current magnitude becomes complex due to the discontinuous nature of the conduction paths through the converter. In Chapter 6 a quantitative analysis and to estimate the peak current through the circuit breaker is provided.

Figure 3.9 shows dc side current and voltage waveforms for a typical dc fault placed at the converter terminals. The current contribution from the converter is characterised by three stages. The process that causes these are detailed in the following sections. However, these may be summarised in the following way. In the first stage, current rapidly rises while only two arms are in conduction and may overshoot what is possible in steady-state. In the second-stage additional arms come into conduction (forced by the ac nature of the driving voltage) which reduces the maximum current that can be sustained, leading to a decay period. In the third stage current will approach the steady-state value, where driving voltage on the dc side (governed by arm conduction periods) is balanced again the maximum current draw possible through the converter. The duration of each of the three stages is system and scenario dependant. If impedance is high (particularly with the addition of dc inductance) then current may not overshoot and stage one transitions directly to stage three. However, typically peak current is attained within 10-15ms.

The current profile from the converter terminal is dominated by the capacitor discharge and may be estimated as such [60]. Fault current contributions from MMC are more complex to estimate as conduction paths within the converter are discontinuous. Exact solutions for current magnitudes require complex mathematical analysis and the task is best suited to circuit simulators, such as SPICE or Simulink. However, the process by which fault currents

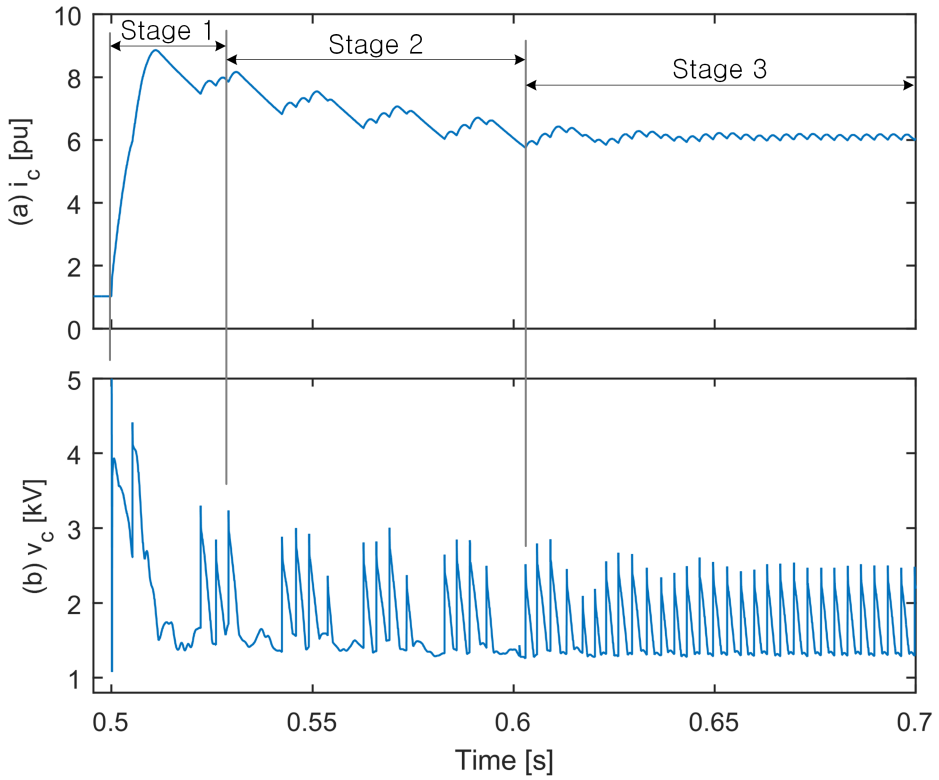


Figure 3.9: Evolution of fault current: (a) converter current, (b) dc voltage. The three phases of the transient are marked as follows: stage 1, initial current rise (and possible overshoot); stage 2, decay period; stage 3, steady-state

develop within the converter, and how to estimate the maximum current contribution from the converter, can be understood qualitatively.

The following section provides analysis which describes the stages of fault current development and the limiting factors in maximum fault current contribution. The analysis is performed for pole-to-pole faults at the converter terminals as these lead to the most severe current stress within the converter.

3.6.1 Relationship between dc Voltage and Arm Conduction Period

DC current is sustained by a driving voltage produced at the dc side of the converter. When the converter is blocked, and a low impedance fault placed at the converter terminals, the equivalent circuit is given by Figure 3.10. Free-wheeling diodes provide a conduction path from the ac side to the dc side, but block current flow in the other direction.

Where all six diodes conduct simultaneously two parallel, three-phase circuits are formed, both in series with the ac impedance; one in the upper arm set and one in the lower. In this condition no voltage is applied to the dc side from the ac side. When current in an arm attempts

to go negative the diode blocks, resulting in a driving voltage v_c being applied to the dc side. This only occurs when one or more diodes are reverse biased. Voltage impulses are then applied to the dc side of the converter, forcing current to circulate, when at least one diode is reverse biased. Conduction periods are, therefore, directly linked to the dc side current sustained. As Figure 3.9 demonstrated, when voltage impulses are applied to the dc side current increased marginally.

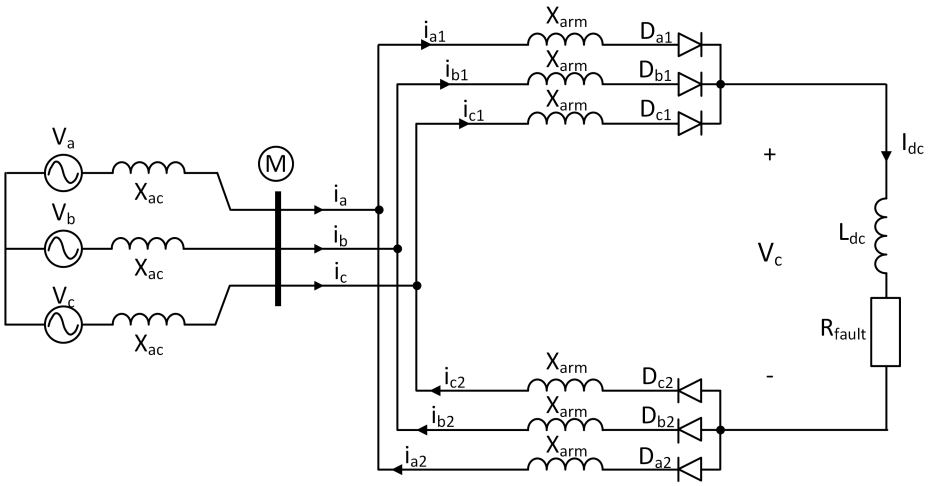


Figure 3.10: MMC circuit in the blocked state. Redrawn to demonstrate rectification action

Figure 3.11 shows current and voltage waveforms for the ac side, dc side and internal converter current measurements. The figure shows a single ac cycle, during which six voltage impulses are produced. Increases in dc current correspond to the voltage impulses, which are spaced 60^o (3.3ms at 50Hz) apart. Between the off-periods all six arms conduct current and all six diodes are forward biased and a reduced voltage is present on the dc side and dc current begins to decay according to the R/L time constant.

The duration of the cycle for which the diode is reversed in a given arm is referred to as ψ_D from here on. Voltage is only applied to the dc side when the diode is reverse biased, i.e. during ψ_D, and as ψ_D is increased the average voltage over the course of one cycle is increased. When fault resistance is very low, the voltage required to sustain current at the maximum possible (described in detail within the following sections) is low. In this case ψ_D approaches 0 where the arm is in conduction almost continuously.

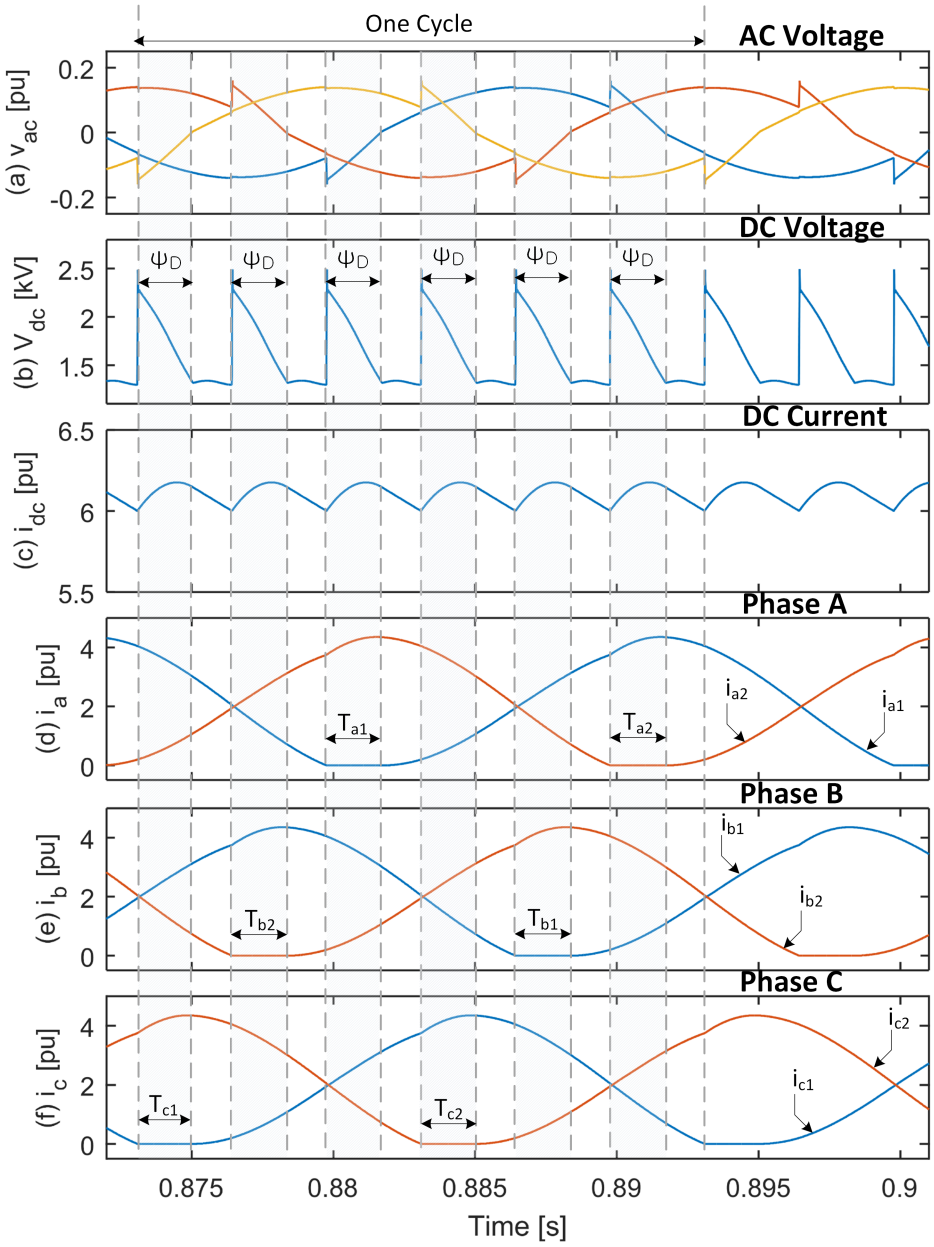


Figure 3.11: Commutation periods for arm current and dc current: (a) ac phase-to-ground voltage, measured at point M; (b) dc voltage; (c) dc current supplied by the converter; (d) phase A upper and lower arm currents; (e) phase B upper and lower arm currents; (f) phase C upper and lower arm currents

3.6.2 Current Flow in Steady-State: Stage 23

In steady-state, the magnitude of the dc side current is related to the ac impedance and dc resistance. In order to simplify the analysis, assumptions are made about the operation of the circuit in order to approximate the current flow. Without these assumptions circuit analysis becomes too complex for hand-based calculations and circuit simulators are more appropriate. The basis of the analysis is formed on the assumption that arms are conducting current for the majority of each cycle (which is later shown to hold true when fault resistance is low). In this case, the current in each arm can be decomposed into ac and dc components and the equivalent circuit shown in Figure by 3.12. The network and transformer impedances are lumped as X_{ac}. This, along with the ac source voltage, is referred to the converter side of the transformer. The ac and arm impedances are assumed to be balanced between the three phases.

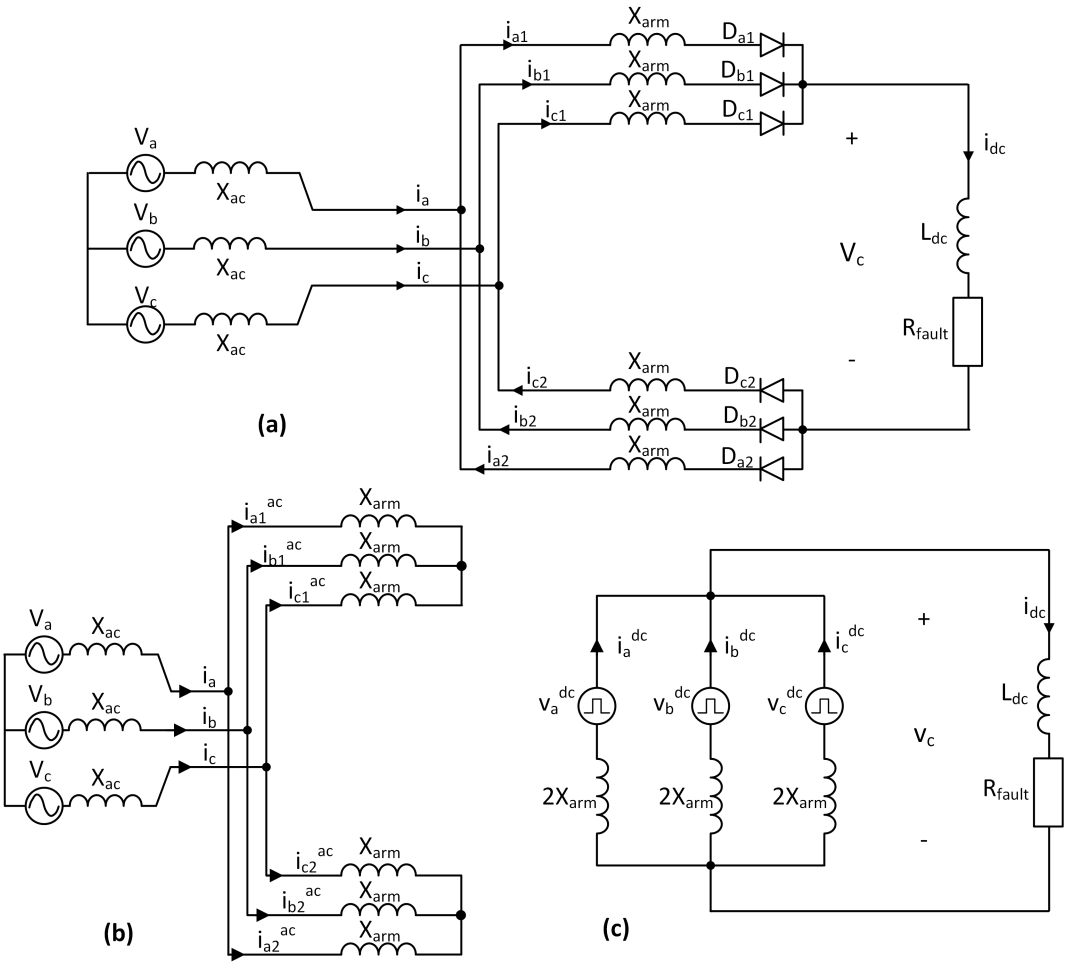


Figure 3.12: Equivalent circuit during steady-state: (a) full circuit; (b) ac components of arm current; (c) dc components of arm current. Voltage impulses are applied to the dc side when diodes commutate off.

As the system is assumed to be symmetrically balanced, any transient current imbalances

will decay due to parasitic resistances within the circuit. As the following analysis assumes a steady-state condition it is possible to use a single phase approach and replicate this across the remaining phases. The total composite current within an arm is given by (3.1).

$$\begin{aligned} i_1 &= i^{dc} + i_1^{ac} \\ i_2 &= i^{dc} - i_2^{ac} \end{aligned} \tag{3.1}$$

As Figure 3.12 shows, the upper and lower arms form two three-phase parallel circuits, in series with ac side impedance. With all diodes in conduction, the ac component of current flowing into sets of upper and lower arms are equal (Figure 3.12 (b)). The current flowing in the ac side is, therefore, twice that of the ac component within an arm, as given by (3.2).

$$i_1^{ac} = i_2^{ac} = i_{ac}/2 \tag{3.2}$$

On the dc side the thee legs (one leg constituting the two arms of a phase) are in parallel. Assuming matched parasitic resistance, the dc component through the upper and lower arms are equal and the dc current is summarised by (3.3).

$$i_a^{dc} = i_b^{dc} = i_c^{dc} = I_{dc}/3 \tag{3.3}$$

Current on the ac side is given by (3.4), where ϕ is an arbitrary phase angle and I_{ac} is the peak current amplitude.

$$i_{ac} = I_{ac}\sin(\omega t + \phi) \tag{3.4}$$

Combining (3.1), (3.2), (3.3) and (3.4) the upper and lower arm currents are given by (3.5).

$$\begin{aligned} i_1 &= \frac{1}{3}I_{dc} + \frac{1}{2}I_{ac}\sin(\omega t + \phi) \\ i_2 &= \frac{1}{3}I_{dc} - \frac{1}{2}I_{ac}\sin(\omega t + \phi) \end{aligned} \tag{3.5}$$

3.6.2.1 Maximum current

From (3.5) the maximum and minimum arm current can be found, given by (3.6).

$$\begin{aligned} i_{1|2}^{max} &= \frac{1}{3}I_{dc} + \frac{1}{2}I_{ac} \\ i_{1|2}^{min} &= \frac{1}{3}I_{dc} - \frac{1}{2}I_{ac} \end{aligned} \tag{3.6}$$

Arm current may not go below zero, as diodes block. Given this, (3.6) can be rearranged to give the maximum possible dc current (3.7) in steady-state.

$$I_{dc}^{\max} = \frac{3}{2} I_{ac} \tag{3.7}$$

3.6.2.2 AC Impedance

Eq. (3.7) demonstrates that dc current is limited by the component of ac current within the arms. If dc current exceeds the condition given then arm current does not reach zero each cycle and diodes do not become reverse biased periodically. This results in no voltage being applied to the dc side. Subsequently dc current will decay until this condition is met. This is the case in Figure 3.9, where current initially overshoots and then decays. The magnitude of ac current that can flow in the arms is in itself dictated by the ac impedance of the circuit. Based on the assumptions given, ac current can be approximated by (3.8), where V_{ac} is the peak phase voltage of the source.

$$I_{ac} = \frac{V_{ac}}{X_{ac} + X_{arm}/2} \tag{3.8}$$

Substituting (3.8) into (3.7), the maximum dc current which can be sourced from the converter to the dc side is given by (3.9). This highlights theoretical the relationship between the maximum contribution of current from there converter and and total impedance of the ac side.

$$I_{dc}^{max} = \frac{3}{2} \cdot \frac{V_{ac}}{X_{ac} + X_{arm}/2} \tag{3.9}$$

To demonstrate the effect this has on dc current flow, Figure 3.13 shows the current flows that occur in steady-state under two operating conditions. A low transformer impedance is used in the first, and a high in the second. As the transformer forms a dominant component of the ac impedance the ac current that flows under fault is significantly reduced. As a result the peak-to-peak arm current magnitude is reduced which also reduces that maximum dc current that can flow. The theoretical results are contrasted with the simulated results and are summarised in Table 3.3. DC current is estimated by (3.9). In the assumed condition of near continuous conduction, maximum arm current can be estimated by that for peak ac current, given by (3.8). The comparison shows that the method derived provides predictions within approximately 15%.

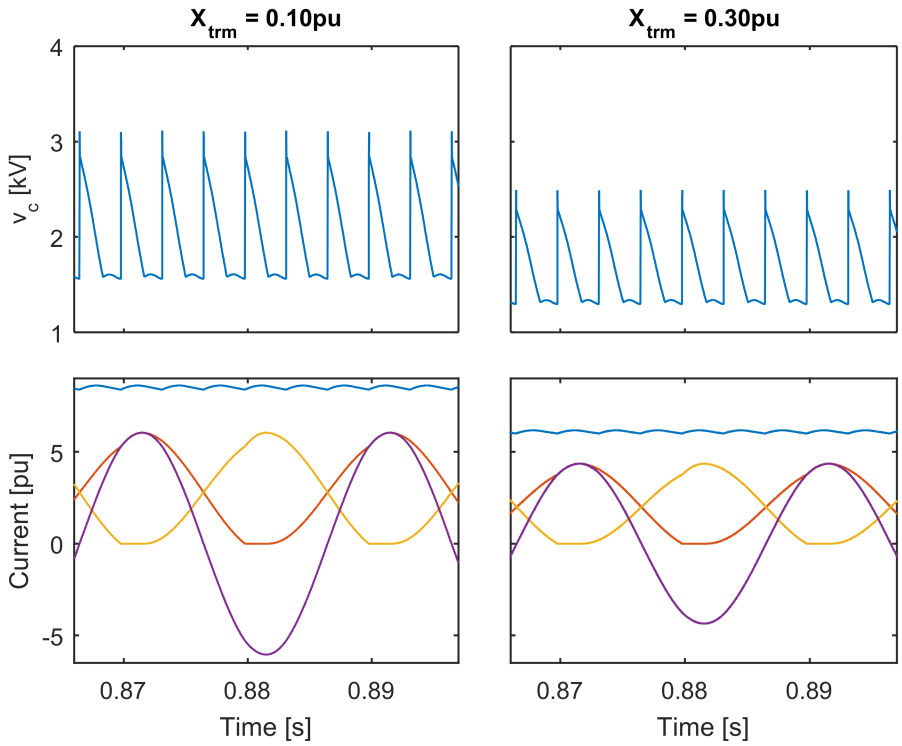


Figure 3.13: Steady-state current flow condition with high and low transformer impedance. Rated dc current is used as the base value: 11249A.

Table 3.3: Comparison of theoretical and simulated arm and dc currents in steady-state

		I_{ac}	I_{dc}	I_{ac}	I_{dc}
X_{TRM}	[pu]	0.1	0.1	0.3	0.3
Theory	[A]	8979	13468	5034	7551
Simulation	[A]	8925	12495	5950	8628
Error	[%]	0.6	7.8	-15.4	-12.5

3.6.2.3 Fault Resistance

With a low fault resistance a low dc voltage is required to sustain the current, thus commutation off time ϕ is also small. In this case, the arms conduct for close to the full cycle, the analysis holds and dc current approaches the limit of $3I_{ac}/2$ (set by the ac component of impedance). If fault resistance is increased then commutation time becomes larger, tending towards ψ_D, resulting in a larger average dc voltage. Figure 3.14 shows the voltage at the dc side of the converter and current measurements for two different cases: one high resistance and one low. In the high resistance case, the periods where all arms conduct are much shorter and, correspondingly, the dc side voltage is much larger.

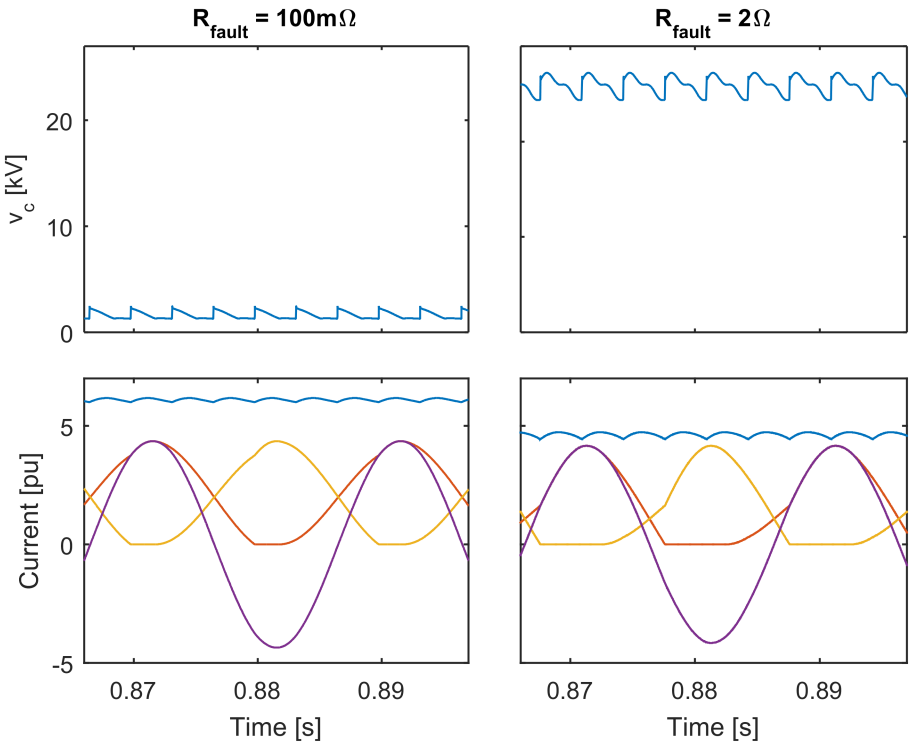


Figure 3.14: Steady-state current flow condition with high and low dc side resistance

3.6.3 Initial Current Rise: Stage 1

In steady state, dc current can not exceed the magnitude dictated by (3.7). However, during the initial transient it is possible for current to overshoot this value, as Figure 3.9 and 3.15 demonstrate. During the initial stage multiple diodes are reverse biased (due to the converter blocking pre-fault negative current within the arms). This results in a larger voltage impulse applied to the dc side which increases current significantly.

In the initial transient, the dc current component in the arms which conduct first exceeds $I_{dc}/3$, which leads to periods where all six arms are in conduction. No voltage impulse is applied to the dc side and a decay in current. Current gradually decays in these arms until the equilibrium condition is reached. In the case given, this occurs after approximately 100ms. With low (or no) dc inductance these voltage impulses typically result in current overshoot during the first set of commutation periods. If, however, dc inductance is used the di/dt can be reduced significantly enough that current does not reach steady-state within the first set of commutation periods. In this case current does not overshoot.

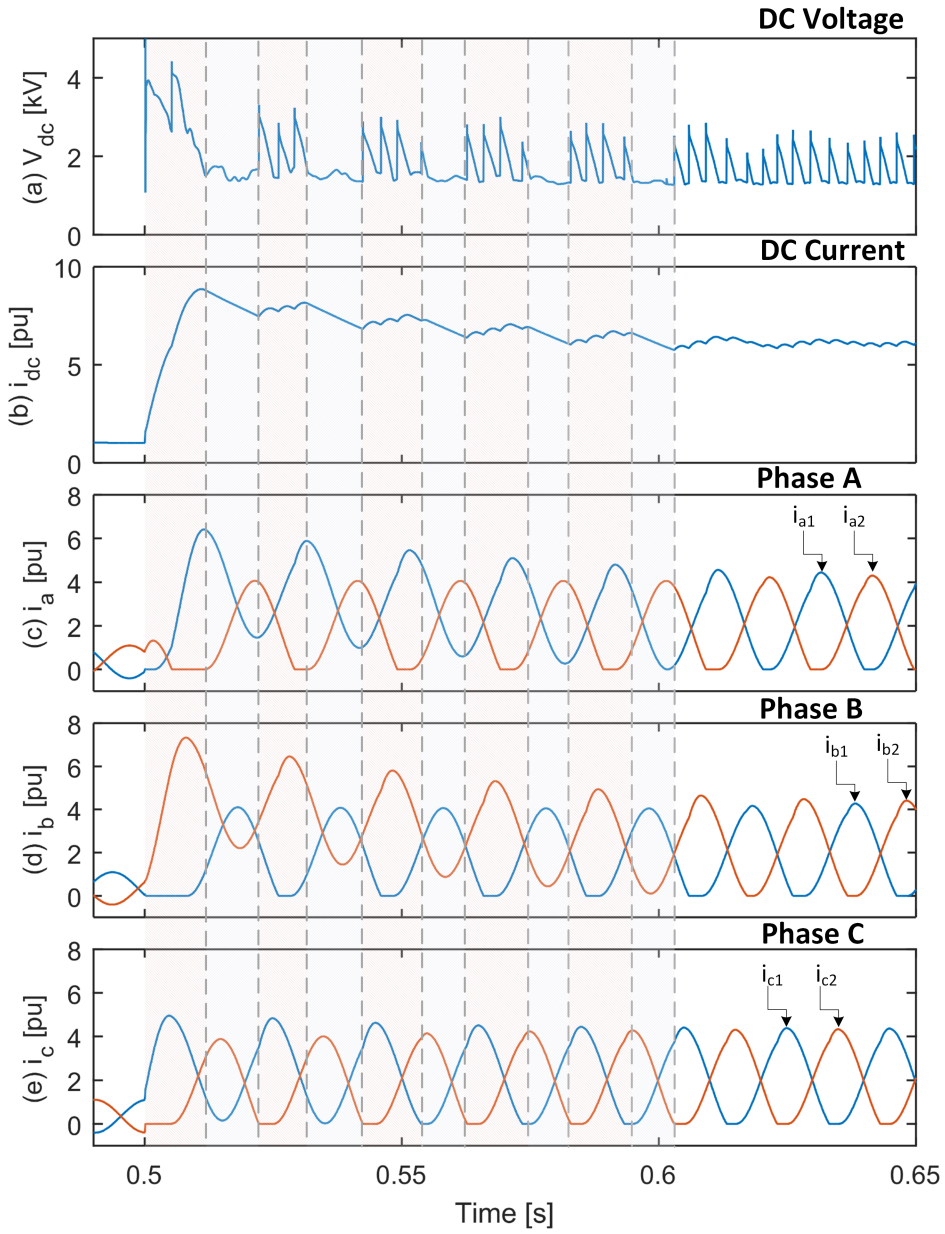


Figure 3.15: Evolution of fault current: (a) dc voltage; (b) dc current, contributed from converter; (c) phase A upper and lower arm currents; (d) phase B upper and lower arm currents; (d) phase C upper and lower arm currents

3.6.3.1 Additional dc inductance

The rate of rise of dc fault current can be limited with increased inductance within the dc current path. Overshoot does not occur if the rate of rise is decreased sufficiently so that dc current does not exceed the steady-state value within the first set of commutation periods. In this manner the peak current requirement of the dc breaker can may be significantly reduced by additional inductance on the dc side if the breaker opens prior the steady-state condition being reached.

Sample simulation results are shown in Figure 3.16 where 100mH of inductance (dc inductors on the dc side of the converter, L_{dc}, are 0mH). The results demonstrate that with the additional inductance no overshoot occurs. Given that state of the art dc breakers are being designed to operate within the 2ms-20ms time-frame (the region where peak current occurs), additional dc inductance can aid their design by reducing peak current stress.

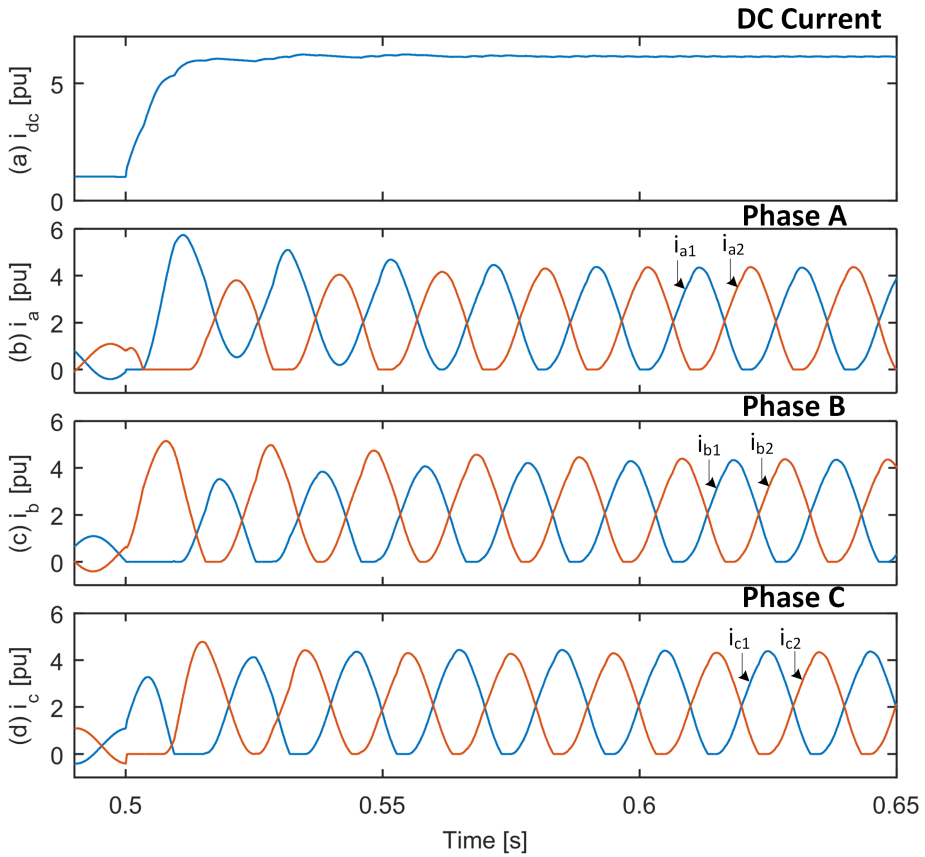


Figure 3.16: Evolution of fault current: (a) dc current, contributed from converter; (b) phase A upper and lower arm currents; (c) phase B upper and lower arm currents; (d) phase C upper and lower arm currents

3.7 Conclusion

A theoretical background and simulated results of pole-to-pole and pole-to-ground faults have been given. Pole-to-pole faults were demonstrated to be the most severe, with high fault currents occurring in a short space of time. The voltage collapse that results from pole-to-pole faults spreads rapidly throughout the dc network and results in high dc current. The converter must be protected from these sustained fault currents so that the semiconductor components are not permanently damaged. If protected by dc breakers these must operate much faster than ac counterparts, as peak current is reached within a 10ms to 20 ms time-frame.

Pole-to-ground faults cause a redistribution of voltage between the two dc lines. If unconstrained, this results in a 2pu voltage stress on the healthy line and s dc offset superimposed on other system equipment, increasing insulation requirements throughout the system. Insulation stress aside, the converter may otherwise continue to operate at full capacity, with only a temporary disruption to power flow.

Where insulation protection is taken into account (with surge arresters placed at cable ends) healthy cable voltage is constrained and the overall converter dc voltage reduced. Whilst clamping the healthy pole voltage the surge arresters continuously dissipate energy. They must be sized to dissipate this energy without thermal runaway occurring [61], until protection operates. The volume and cost of the arresters is, therefore, related to how fast protection can operate to isolate the faulted part of the system from the energised part. Circuit breaker speed must be traded-off with the required energy dissipation capability of the surge arresters.

Fault current analysis has highlighted the processes causing dc current overshoot and the limitations on maximum dc current. Overshoot can be controlled with increased inductance within the dc path. If slower dc breakers are used, then current can be broken once steady-state is reached, in which case overshoot is less onerous.

Chapter 4

Parametric Converter Stress Studies

4.1 Introduction

In Chapter 3 the impact of a dc fault on converter operation was covered. The result from both pole-to-pole and pole-to-ground faults was an increase in current, which is circulated through the converter. These can be significantly in excess of the device ratings and can therefore only be sustained for short periods of time before failure occurs. For future multi-terminal HVDC systems it has been proposed that dc breakers may be used to clear these faults and protect the converters [27]. The stress placed on both the breaker and converter is a function of system parameters, fault condition and circuit breaker speed. As pole-to-pole faults were shown to produce the most severe current stress studies carried out in this chapter are exclusively related to these.

In this chapter the impact on converter stress based on different circuit breaker operating speeds and component values within the system are studied. In Section 4.2 detail of the test system which is used to perform analysis are given. A method of quantitatively measuring converter and dc breaker stress is developed in section 4.3, to allow direct comparison of different fault cases and parameter values. In section section 4.4 simulation studies are performed to demonstrate how converter stress is affected by passive system component values and fault characteristics. Finally, in section 4.5 the benefits of changes to converter parameters on converter stress are contrasted with the possible degradation of performance in normal operation.

4.2 Test System

The stress placed on the converter and dc breaker during faults plays a role in equipment sizing and therefore the overall cost of the converter station. As this stress in influenced by many of the system parameters it is useful to understand how, if possible, these may be adjusted to improve the fault performance and reduce the overall cost of the system. In this section the sensitivity of fault characteristics to parameter variation is documented. Figure 4.1 shows the test system is used to perform the parametric studies. The system consists of two HB-MMC converters, which are identical, along with two matched ac networks. System parameters are given in Table 4.1. As a large number of simulation cases is performed, each converter uses the average-cell model, to reduce simulation time.

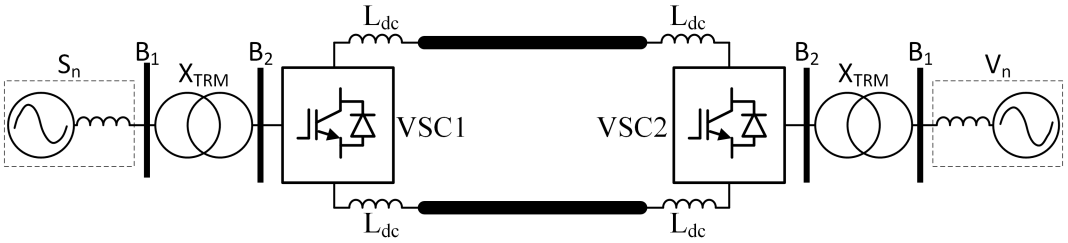


Figure 4.1: Two-terminal test system

Table 4.1: System Parameters

	Parameter	Value	Notes
V_n	Network voltage	400kV	line-to-line RMS
S_n	Network strength	10GW	$X/R = \inf$
V_{B1}	Bus B1 voltage	400kV	Nominal, line-to-line RMS
V_{B2}	Bus B2 voltage	385kV	Nominal, line-to-line RMS
S_c	Rated power of converter	1000MW	PF = 0.95
V_{dc}	Nominal dc voltage	700kV	Pole-to-pole
X_{TRM}	Transformer leakage	0.2pu	Per unit
X_{arm}	Arm inductance	0.1pu	Per unit, referred to B2
L_{dc}	DC inductance	0mH	At converter terminals

4.3 Measuring Converter Stress

To establish the relationship between converter/system parameters and fault characteristics a set of quantitative measurement criteria must be defined. In the studies performed here two

main quantities, peak dc current and semi-conductor energy dissipation, have been chosen to compare the severity of the fault, each of which is explained in detail in the following sections.

Typically, peak current occurs within approximately 20ms of fault inception, as Figure 4.2 demonstrates. DC breaker operation speed depends on technology type, see Chapter 5. Typical values are in the range of 2ms - 5ms for hybrid type and 10ms - 20ms for mechanical type. As they operate during the initial current rise they affect how much stress is placed on the converter and breaker. Measurements are taken for discrete times after the fault, as given in Table 4.2. The timings have been chosen as they are indicative of the operational speed for different dc breaker technology types (see Chapter 5).

Table 4.2: Discrete times for taking stress measurements. Timings based on typical opening times for different circuit breaker technologies. The time reflects the time for the circuit breaker generate a counter voltage. Detection times not included as there is a wide variation dependant on system topology, prefault condition, fault location and detection method

Parameter	Time	Notes / Likely breaker technology
t_0	0	Fault inception
t_1	2ms	Electronic/Hybrid DC Breaker
t_2	5ms	Hybrid breaker
t_3	10ms	Fast mechanical
t_4	20ms	Mechanical

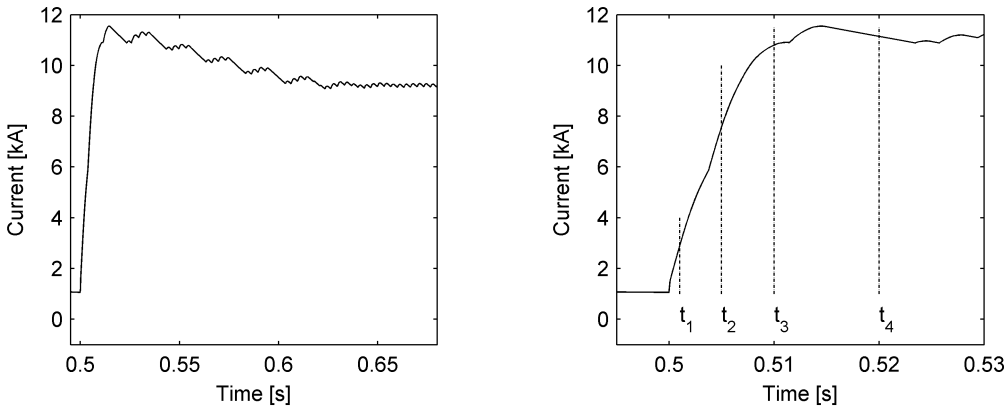
4.3.1 Peak dc Current

The magnitude of steady-state fault current through the converter is limited by the ac impedance (network, transformer and converter) as well dc resistance (cables and fault resistance), see Chapter 3. DC breakers, used to protect the converter, are in the fault path and must withstand the peak current. By identifying the conditions which produce the most severe peak current the dc breaker requirements may be defined. During the time-frame in which they may operate (up to 20ms) current through the converter to the dc side is still transient and rapidly rising. The peak current stress therefore relates to both the system condition and circuit breaker operation speed. To evaluate the effect of both parameters simultaneously, the peak current is measured at time intervals which correspond to feasible prospective dc breaker technologies (see Table 4.2).

Figure 4.2 shows a typical simulation waveform of the dc current, for a pole-to-pole dc fault at the converter terminals. As Figure 4.2b shows, the current stress varies significantly over the initial transient period, illustrating the impact of using different circuit breaker technologies on the peak current. For example, 2ms (t_1) after the fault current has reached approximately 3kA, whereas at 10ms (t_3) it has reached approximately 11kA. This gives an approximate

comparison between technology types: 2ms corresponding to a reasonable time-frame for a fast hybrid circuit breaker and 10ms for a fast mechanical/resonant circuit breaker.

Steady state current is limitted by the ac network strength/impedance and dc resistance. However, under the some conditions (low amounts of dc inductance) dc current can overshoot the steady-state fault current flow. In the case given an overshoot of approximately 20% occurs.



(a) (b)

Figure 4.2: DC Current sourced from the converter under a pole-to-pole fault. Initial condition: rated power flow from ac side to dc side. $t_1 = +2$ms (fast hybrid cb), $t_2 = +5$ms (hybrid cb), $t_3 = +10$ms (fast mechanical cb), $t_4 = +20$ms (slow mechanical cb).

4.3.2 Semiconductor Energy Dissipation

Figure 4.3 shows a simplified thermal model of a semiconductor, with a lumped thermal mass and impedance. Power dissipation at the junction is represented by power source P_j and the lumped thermal resistance between the junction and ambient air by R_{th}. (Ambient air temperature T_a is assumed to remain constant.) In steady-state, the temperature differential between the junction and ambient air depends on the heat flow and thermal impedance. However, the thermal mass, given by capacitance C_j, acts as an energy store giving a degree of freedom between P_j, R_{th} and T_a. This allows a device to dissipate larger amounts of energy during current surges without increasing T_j excessively. The permissible transient energy dissipation depends on the transient fault current profile, as well as the thermal properties of the device [30].

Additional current experienced during faults can lead to damage of semiconductors within the cells if junction temperature increases beyond rated. The magnitude and duration of transient fault current must therefore be kept low enough to ensure that this does not occur. Typically, device manufacturers quote the tolerable current surge using a half sine wave pulse.

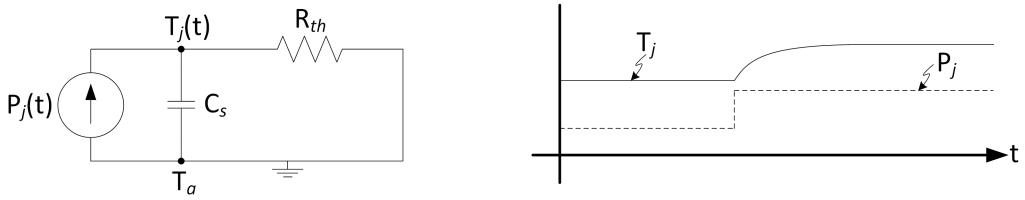
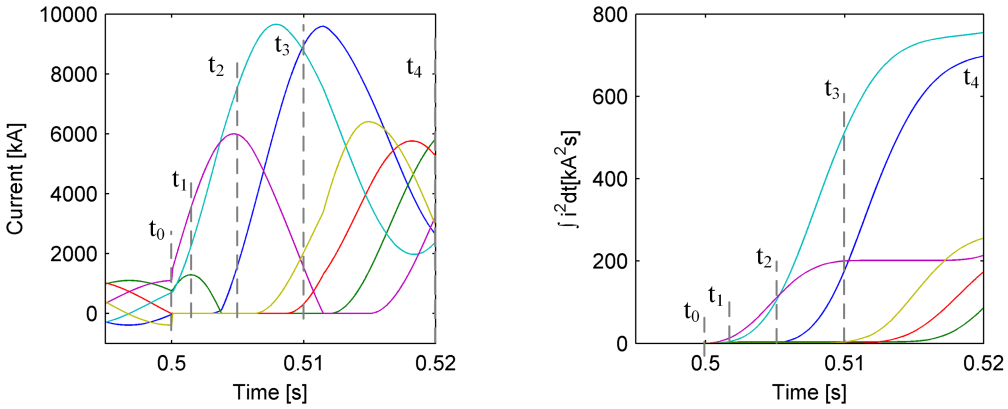


Figure 4.3: Thermal impedance of semiconductor

Energy dissipation capability is quantified by the time-integral of the device current squared ($\int i^2 dt$), which is proportional to energy dissipated. Although the current through the FWD during faults will vary from the ideal half sine wave profile used by manufacturers, measuring $\int i^2 dt$ indicates the temperature rise within the devices without the requirement for full thermal modelling.

During simulation a time integral of the square of the current through each of the arms is taken, beginning when the converter blocks. Measurements of $\int i^2 dt$ are taken at time periods $t_1 \rightarrow t_4$ (see Table 4.2). Figure 4.4 shows typical current profiles for the arms of a converter under a P2P dc fault occurring 0.5 seconds into the simulation. Current through the six arms is shown in Figure 4.4a. The converter is blocked immediately on fault inception and the time-integral ($\int i^2 dt$) is started, shown in Figure 4.4b. Fault current increases in the two arms which correspond to the largest line-to-line voltage at the instant the fault occurs. Current then begins to be commutated into the next arm as the ac line voltage changes. The effect is to have an asymmetric energy dissipation distribution between the arms, as shown in Figure 4.4b, where some devices dissipate significantly more energy than others in the 20ms time range observed.



(a) (b)

Figure 4.4: Current through arms and $\int i^2 dt$, under a pole-to-pole fault. $t_1 = +2$ms (fast hybrid cb), $t_2 = +5$ms (hybrid cb), $t_3 = +10$ms (fast mechanical cb), $t_4 = +20$ms (slow mechanical cb)

4.3.2.1 Cell protection Sharing

Inside each half bridge cell there are two protection mechanisms (see Figure 4.5). The first – a mechanical bypass switch (BPS) – is used to short circuit the cell if S_1 fails open circuit. Redundant cells may be included in each arm to allow for cells to be short-circuited whilst still maintaining the voltage across one phase leg, allowing the converter to continue to operate. With no redundant cells voltage must be redistributed, rising within the healthy cells, or the converter must must be shut down. Under a dc fault the cells carry large currents, in the order of 10kA during the initial current transient and repetitive peaks of approximately 6kA (see Figure 4.4a). Free-wheeling diodes, which have a limited over-current capability, conduct in this period and can be damaged. The second cell protection mechanism is a line frequency thyristor T_y, which has a much higher over-current capability, is placed in parallel with diode D_2 [62]. When the converter is blocked, upon fault detection, T_y is fired and reduces the current through $D2$

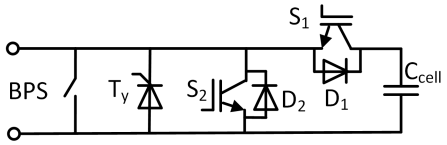


Figure 4.5: MMC Cell, showing mechanical bypass switch and protective thyristor

Current is split between the two devices according to their on-state current-voltage (I-V) characteristics. To assess how current through D_2 is reduced the current sharing between two applicable devices is investigated. Table 4.3 gives a summary of key attributes of the devices chosen [63, 64]. On-state characteristics V_{on} and R_{on} are found through a graphical, linear approximation of each device, based on data sheet information.

Table 4.3: Selected Devices

Device	Rated Voltage [V]	Rated Current [A_{RMS}]	$\int i^2dt$ Capability [kA^2s]	V_{on} [V]	R_{on} [$\mu\Omega$]
Diode	4500	1200	480	1.7	750
Thyristor	4200	6715	20,800	1	75

In Figure 4.6 I-V curves for the two devices are shown superimposed. With a constant voltage across the cell, current sharing can be assessed graphically. With the thyristor carrying 6kA approximately 200A is passed through the diode – a ratio of 30:1. Thereofre, firing T_y reduces the current through the cell diode to below its continuous rating (see Table 4.3).

The current sharing through the devices shown in Figure 4.6 is only valid in steady-state.

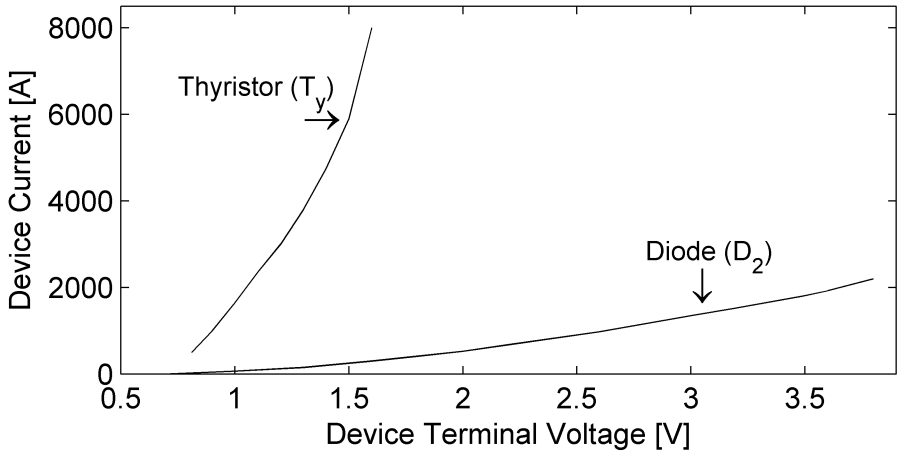
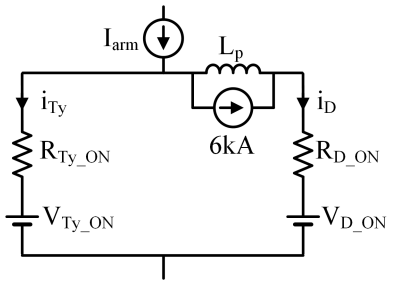


Figure 4.6: Device current sharing

To assess the transient redistribution of current upon triggering the thyristor a simplified model of the two devices is used, as shown in Figure 4.7. Each of the devices is represented by an equivalent on-state voltage and series resistance (values taken from Table 4.3). A wiring length between the two devices is assumed at 20cm giving a loop inductance (L_p) of 0.20μH.



Initial Conditions	
I_{arm}	6 kA
$i_{Ty}(0)$	0 kA
$i_D(0)$	6 kA

Figure 4.7: Equivalent circuit during current redistribution

Total current through the arm is assumed to remain constant (at 6kA) during the commutation, as the time-period is small when compared to an ac cycle. Figure 4.8 shows simulation results of current commutation, upon triggering T_y. Current in D_2 is brought below its continuous rating (given in Table 4.3) within 0.5ms. The $\int i^2 dt$ within the diodes is within their rating, as shown in Figure 4.4b. Therefore, the choice of thyristor, which determines the $\int i^2 dt$ capabilities, then dictates the length of time that the converter can sustain fault current.

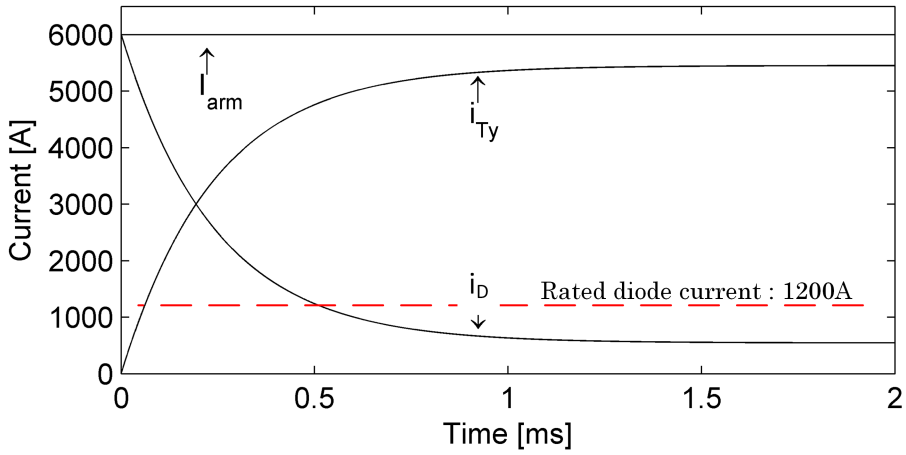


Figure 4.8: Current commutation between D2 and T_y

4.4 Parametric Studies

As pole-to-pole cases represent a worst-case scenario, in terms of system protection and dc breaker requirements, all simulation cases are carried out for P2P faults. Faults are located at the cable connections of VSC1. Measurements are taken at VSC1.

Table 4.4 lists the set of parameters which are altered. In each of the parametric studies carried out only the parameter under study is altered, whilst all others remain constant (as given in Table 4.1). In all cases, initial power flow is 1GW from VSC1 to VSC2. VSC1 operates under P/V_{ac} control and VSC2 under V_{dc}(PI) control.

Table 4.4: Variable Parameters

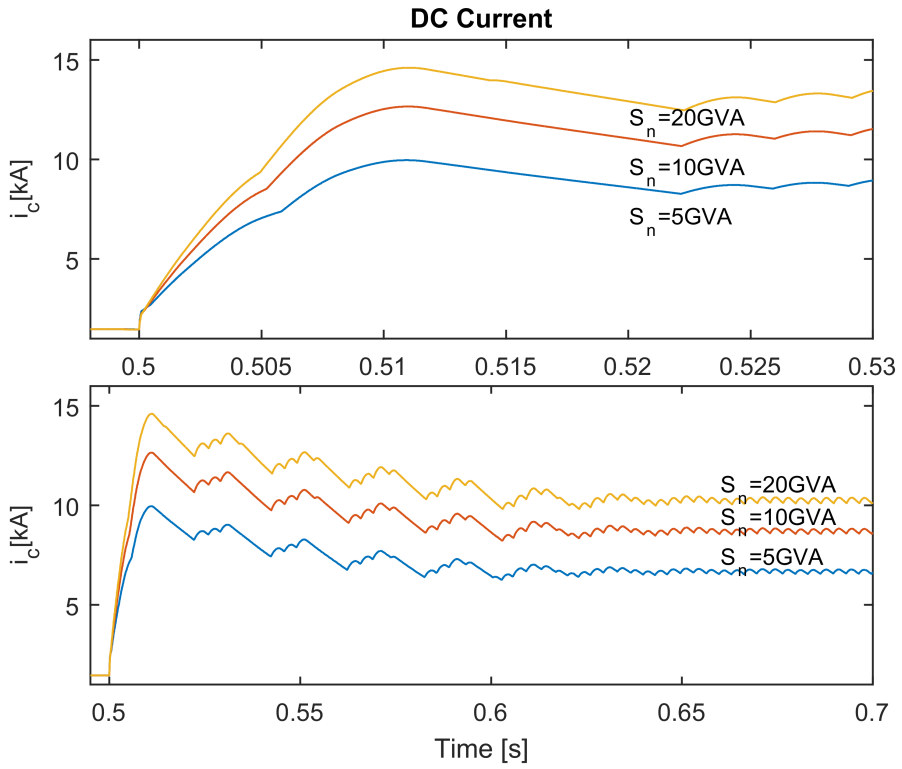
	Parameter	Base Value	Lower value	Upper value
S_n	Network strength	10GVA	5GW	20GW
X_{TRM}	Transformer leakage	0.2pu	0.10pu	0.30pu
L_{dc}	DC Inductance	0mH	10mH	300mH
X_{arm}	Arm inductance	0.1pu	0.05pu	0.15pu
R_{fault}	Fault Resistance	100mΩ	100mΩ	20Ω

4.4.1 AC Network Strength

Simulation cases are carried out for worst case stress – faults located at the converter terminals. The network strength (S_n) is varied to correspond to a network strength of 5GVA to 20GVA. Figure 4.9 shows the simulation results. The peak current through the breaker and energy dissipation within the cell semiconductors increases with network strength. Peak current shows

a marginal increase between $t_3 \rightarrow t_4$ when compared to the change between $t_1 \rightarrow t_2$ as the current has almost risen to its peak magnitude by this point in time. The energy dissipation shows a significant increase for stronger networks, over a longer time period (t_4).

Changes to network strength will have a significant impact on the converter and dc breaker stress, as simulation results have shown. Network strength depends on electrical location within the HVAC network and is likely to experience a temporal variation, as load and generation are connected and disconnected. The worst case (from a fault perspective) occurs with the strongest network. The designer has minimal influence over this and therefore the worst case must be designed for.



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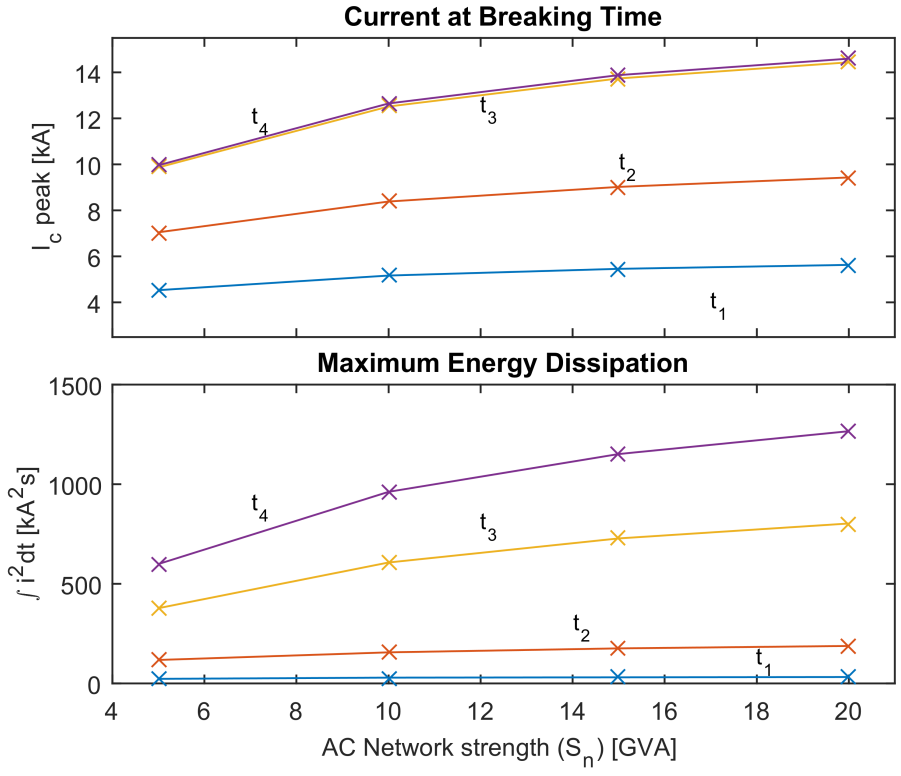


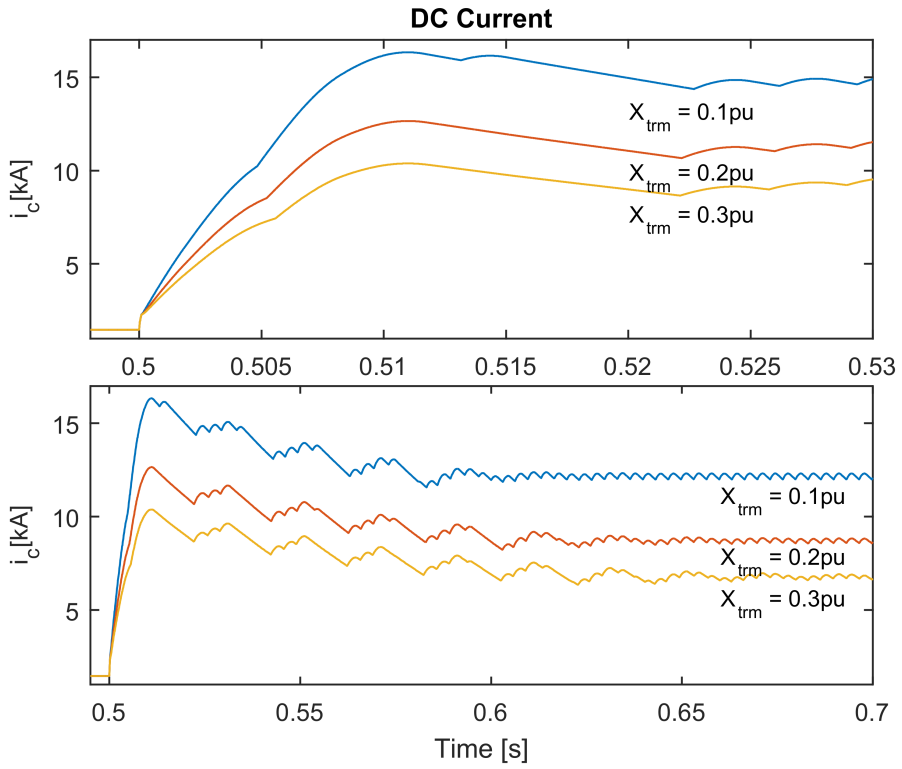
(b)

Figure 4.9: Simulation results for variable ac network strength. (a) Time domain converter current, (b) Maximum current and diode energy dissipation. $t_1 = +2$ms (fast hybrid cb), $t_2 = +5$ms (hybrid cb), $t_3 = +10$ms (fast mechanical cb), $t_4 = +20$ms (slow mechanical cb)

4.4.2 Transformer Impedance

Leakage within the interface transformer has broadly the same effect as the grid strength – it provides a source of ac impedance to fault current. The transformer impedance will limit magnitude of fault current that can flow in steady-state, for example 5pu current for an impedance of 0.20pu . In Figure 4.10 parametric simulation results are given for a feasible range of transformer impedances. Practical limitations place the lower limit at approximately 0.10pu and beyond 0.30pu losses are increased significantly (see Section 4.5). Increasing the leakage of the transformer is desirable from a fault perspective; as simulation results have shown peak dc current and energy dissipation are significantly reduced. When considering increasing the transformer leakage, the reduced stress during faults must be traded-off against the performance during steady-state. For a fixed turns ratio the PQ envelope of the converter will be reduced with increased leakage. To maintain the same capability the turns ratio must be altered to reduce the converter side voltage, resulting in higher currents and losses within the converter during normal operation. A detailed explanation may be found in Section 4.5.

The sample results show a strong correlation between the transformer leakage and both the steady-state and peak current through the converter. As described in Chapter 5 the increased impedance reduces the steady-state current by reducing the maximum current that may flow through the arms when they are in a balanced state. As a proportion, overshoot remains constant at approximately 40% of steady-state. As with network strength alterations, there is marginal different between peak currents at t_3 and t_4 as peak current has been reached by this point (see time domain waveforms in Figure 4.10a). However, there is a significant increase in energy dissipation within the diodes over the same period.



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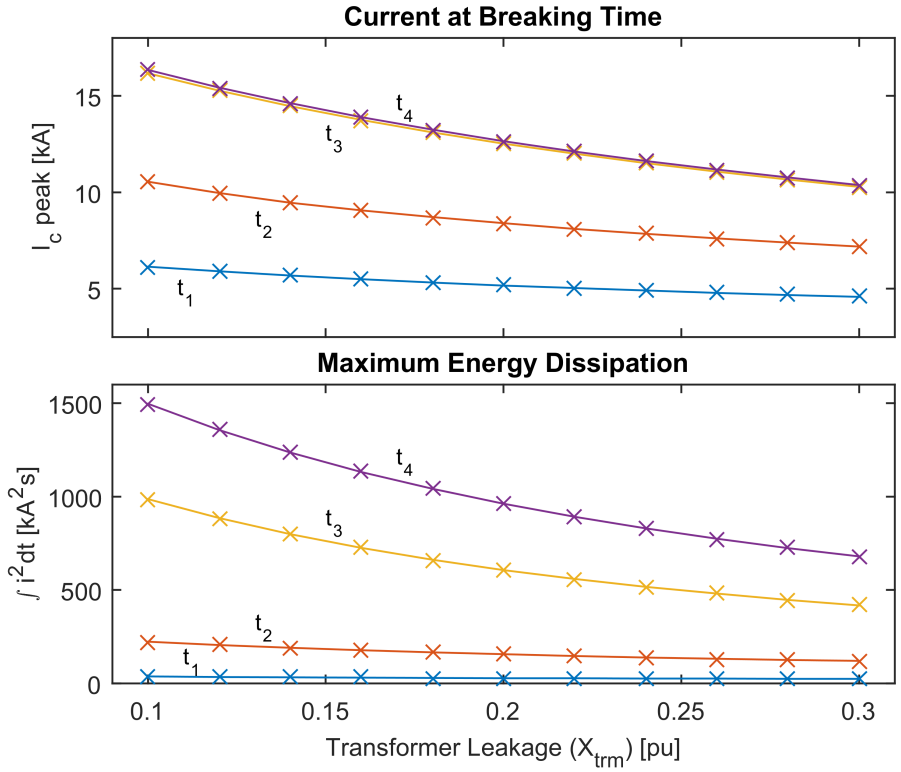


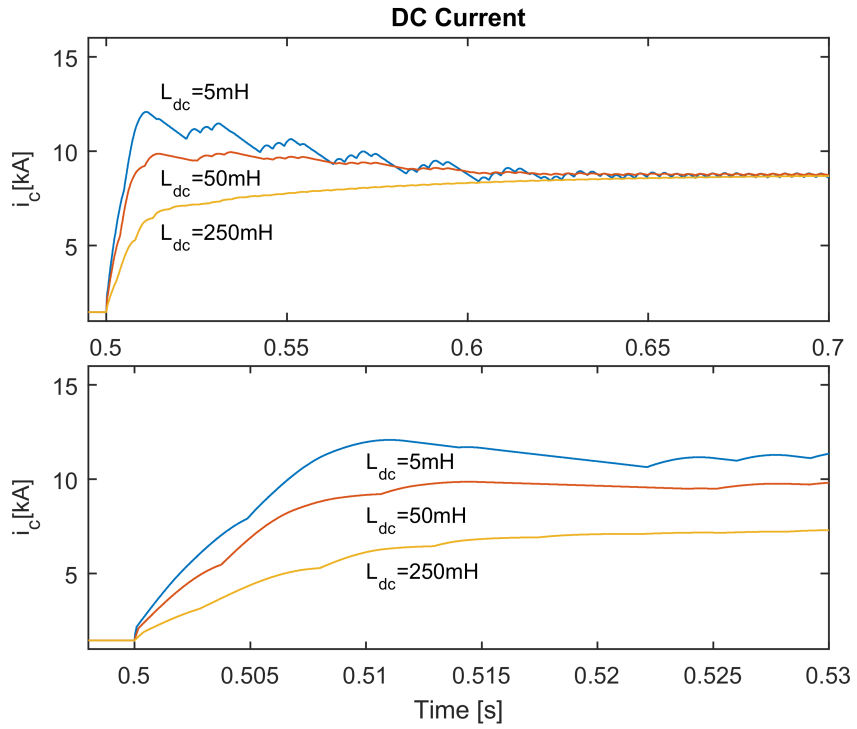
(b)

Figure 4.10: Simulation results for variable transformer leakage. (a) Time domain converter current, (b) Maximum current and diode energy dissipation. t_1 = +2ms (fast hybrid cb), t_2 = +5ms (hybrid cb), t_3 = +10ms (fast mechanical cb), t_4 = +20ms (slow mechanical cb)

4.4.3 Additional DC Inductance

Additional inductance (L_{dc}) placed at the converter terminals, as shown in Figure 4.1, has been suggested to reduce the stress placed on dc breakers [28]. Simulation results of fault studies are shown in Figure 4.11, where additional dc inductance is included in series with each of the converter poles. The results demonstrate that the peak current can be significantly reduced with even moderate values of L_{dc}. The difference in peak current over the time period $t_3 \rightarrow t_4$ is minimal when L_{dc} is low (similarly to the ac impedance parametric studies carried out) as peak current is reached within a short period with low inductance. As dc inductance is increased the time-constant of current rise is increased also and thus peak current occurs later. For larger values of L_{dc} (>50mH) the slower rate of rise of current causes a noticeable difference between peak current at t_3 and t_4 (the difference between a fast mechanical and a conventional mechanical dc breaker). As a result, energy dissipation within the cell semiconductors can be reduced significantly with additional inductance. For example, over the time-range t_4 an additional 50mH of inductance reduces the maximum $\int i^2 dt$ by approximately 45%. The decrease in $\int i^2 dt$ allows slower protection mechanisms or devices with lower ratings. For large values of L_{dc} the reduction in $i^2 dt$ is marginal.

The use of dc inductance has been shown to benefit the peak current stress in the dc breaker and reduce maximum energy dissipation (which can lead to an extension of the critical protection time). However, artificially increasing dc side inductance can reduce controllability of the system, as it begins to behave more like a current (rather than voltage) source and can cause issues during ac faults [65]. For commercial instillations the feasible inductance magnitudes are also likely to be constrained to a smaller range than has been examined in this study due to the increased volume (which is a particular issue for offshore instillations).



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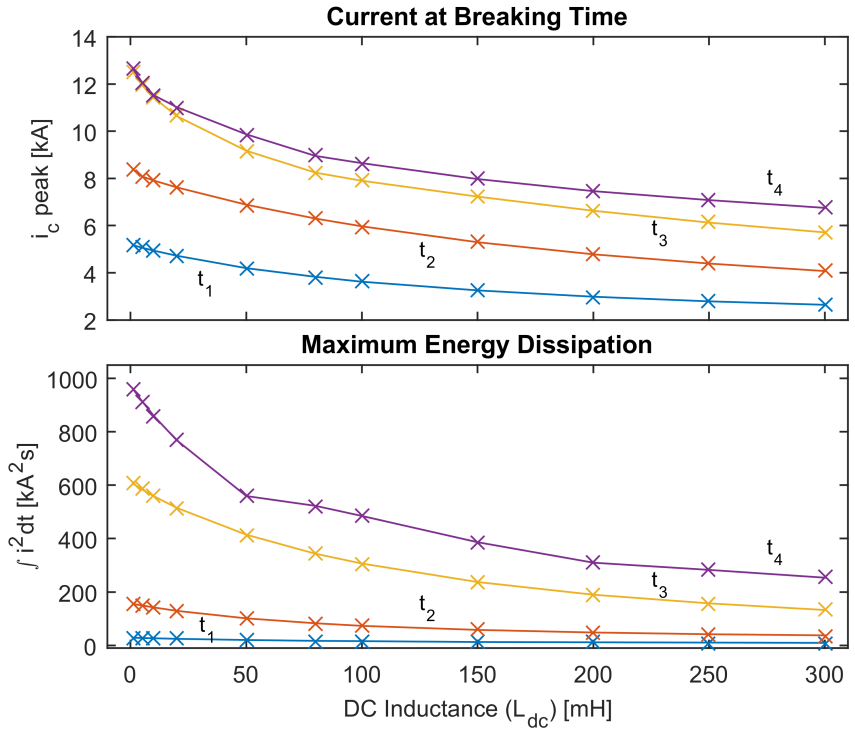


(b)

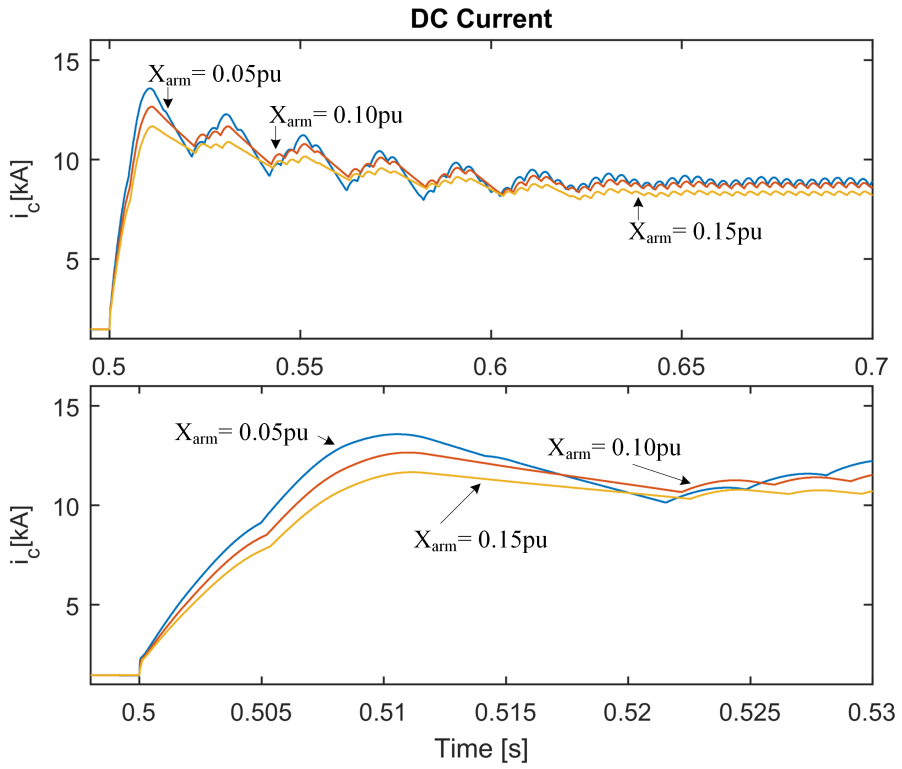
Figure 4.11: Simulation results for variable dc inductance. (a) Time domain converter current, (b) Maximum current and diode energy dissipation. $t_1 = +2$ms (fast hybrid cb), $t_2 = +5$ms (hybrid cb), $t_3 = +10$ms (fast mechanical cb), $t_4 = +20$ms (slow mechanical cb)

4.4.4 Arm Inductance

In this study the arm inductance is varied between 0.05pu and 0.15pu and the resulting peak dc current and arm energy dissipation are observed. Simulation results are shown in Figure 4.12. Changes to arm inductance show marginal influence over the steady-state current when contrasted to the results shown from variation of transformer leakage (Figure 4.10). The impact of arm inductance has a much larger effect on current overshoot when compared to transformer impedance. The causation of this is explained in Section 3.6.

In summary, additional transformer impedance has a greater effect on maximum current flow through the converter in steady-state, as only ac current flows though it. However, from the ac perspective the arm inductances are in parallel, therefore changes to their value have a smaller impact on steady-state current. The arm inductors form part of the dc-side current loop and therefore play a role in determining the rate of rise of current in the initial transient. Because they appear in series from the dc perspective they have a much larger influence when their value is changed, reducing overshoot.

Similarly to transformer leakage, increasing arm inductance (to decrease fault severity) must be traded-off with the reduction in PQ envelope of the converter (or additional losses inured with a different transformer turns ratio). A detailed explanation may be found in Section 4.5.



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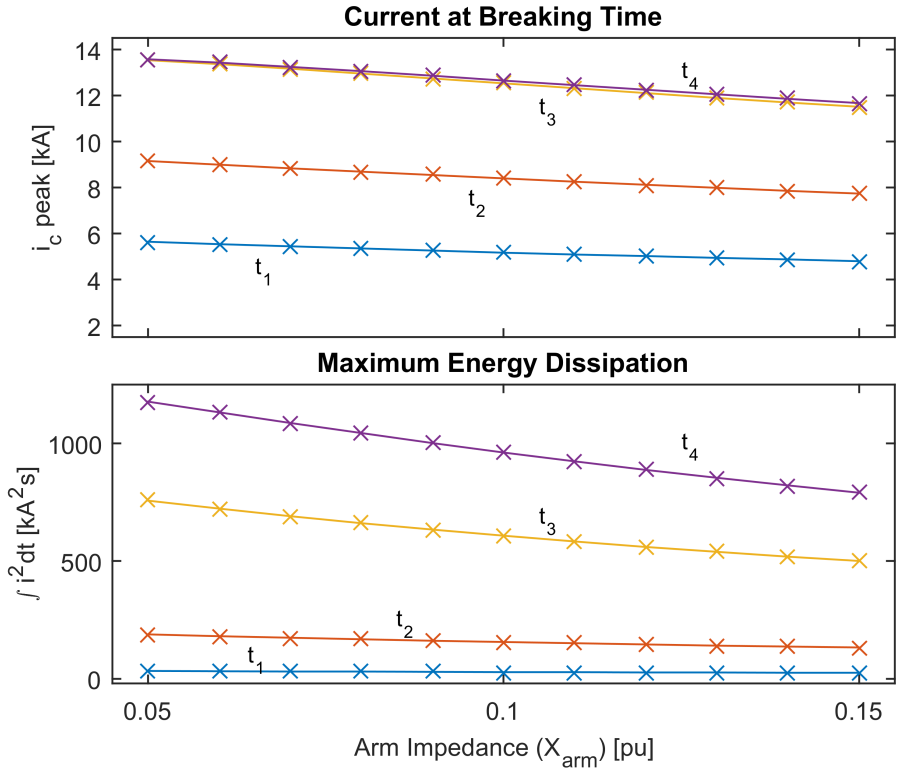
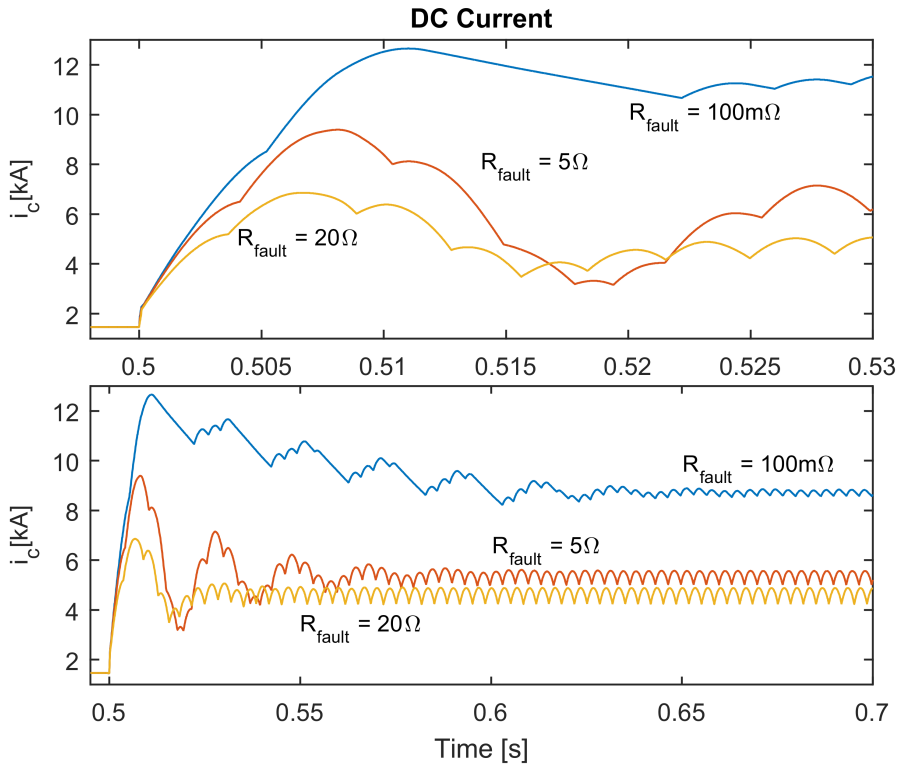


(b)

Figure 4.12: Simulation results for variable arm impedance. (a) Time domain converter current, (b) Maximum current and diode energy dissipation. $t_1 = +2$ms (fast hybrid cb), $t_2 = +5$ms (hybrid cb), $t_3 = +10$ms (fast mechanical cb), $t_4 = +20$ms (slow mechanical cb)

4.4.5 Fault Resistance

In this section the impact of fault resistance is documented. A fault is placed at the terminals of the converter station 0.5 seconds into the simulation. Resistance is varied between 100mΩ and 20Ω. Figure 4.13 shows the simulation results, with measurements taken for time periods $t_1 \rightarrow t_4$. Fault resistance has marginal effect on the rate of rise of current over the first 2ms (t_2). However, overshoot and peak current are reduced significantly, as well as steady-state current (Figure 4.13a). There is negligible difference between the peak current at t_3 and t_4 as maximum current occurs approximately 10ms after the fault (see Figure 4.13). Maximum device energy dissipation is reduced in line with the peak dc fault current. However, as with network strength the fault resistance may not be influenced at the design stage and the system must be designed to withstand the worst case scenario – the lowest feasible fault resistance.



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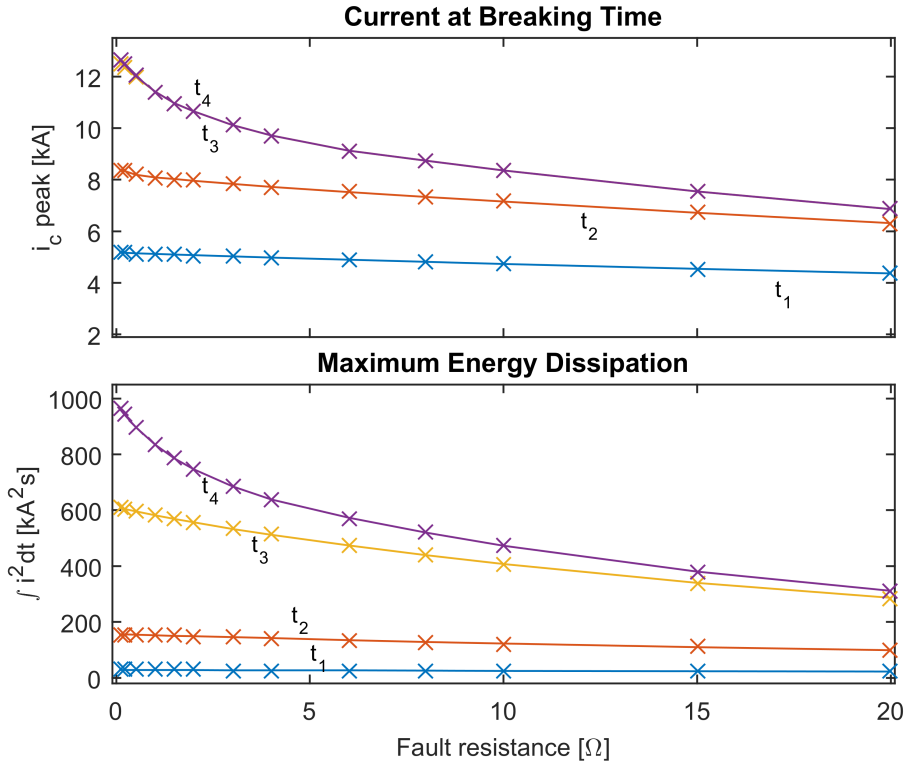


(b)

Figure 4.13: Simulation results for fault resistance. (a) Time domain converter current, (b) Maximum current and diode energy dissipation. t_1 = +2ms (fast hybrid cb), t_2 = +5ms (hybrid cb), t_3 = +10ms (fast mechanical cb), t_4 = +20ms (slow mechanical cb)

4.5 Design Considerations

The parametric studies carried out in the previous sections have verified that the stress on the converter and breaker may be reduced through adjustment of circuit parameters. Circuit parameters such as distance to fault and network strength are beyond the scope of design. As such the converter and system must be designed to withstand a worst case scenario. Parameters such as arm inductance, transformer leakage and dc inductance may be adjusted during the design phase to give better fault performance. However, by reducing stress during faults normal operation is impacted, typically resulting in higher current through the converter. In this section the influence of changing these parameters are assessed in a qualitative and quantitative manner.

Figure 4.14 shows a simplified, single-line power flow diagram of the converter and ac source. The ac source is assumed to be a perfectly stiff ac network – that is, current flow in or out has no effect on the bus voltage at the point of common coupling (PCC).

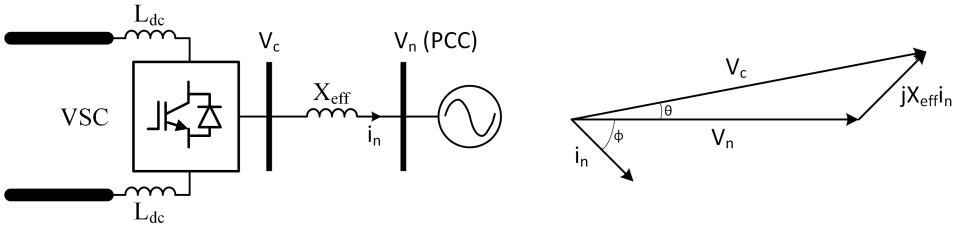


Figure 4.14: Converter power flow diagram

For MMC systems the effective interface reactance X is a combination the interface transformer reactance X_{trm} and the the arm reactances X_{arm}, which is given by (4.1).

$$X = X_{\text{trm}} + \frac{1}{2}X_{\text{arm}} \tag{4.1}$$

4.5.1 AC Impedance

Both the arm inductance and transformer leakage may be adjusted, within a range, to optimise the performance under fault. The combination of the two provide impedance to fault current, increasing these therefore reduces the fault current magnitude. Lower values of these parameters are constrained by the balance of cost of practical design capabilities. For example, arm inductors limit circulating current during normal operation and reducing their value must be balanced against increased capacitor sizes or loss of modulation capability [66]. The following analysis is provided to demonstrate the correlation between reduced stress during faults and increased current during normal operation – optimisation of these component values is outside

of the scope of this work. A single phase analysis is performed here, based on the notation given in Table 4.5.

Table 4.5: PQ Capability Calculation Notation

	Parameter	Notes
V_n	Network voltage (PCC)	Phase, RMS
I_n	Network current (PCC)	Phase, RMS
V_c	Converter output voltage	Phase, RMS
X	Interface impedance	Total effective (transformer and arms)
S_b	Base Power	

Fundamental equations are given below by (4.2) to (4.7)

$$I_n = I_d + jI_q \tag{4.2}$$

$$I_d = \frac{P}{V_n} \tag{4.3}$$

$$I_q = \frac{Q}{V_n} \tag{4.4}$$

$$|V_c|_{\max} = \frac{1}{\sqrt{2}} \cdot \frac{V_{dc}}{2} \tag{4.5}$$

$$|S| = \sqrt{P^2 + Q^2} \tag{4.6}$$

$$X = X^{\mathrm{pu}} \frac{V_n^2}{S_B} \tag{4.7}$$

The relationship between converter voltage and current flow is found by taking KVL within the phasor diagram shown in Figure 4.15, producing (4.8). The impedance X is that of the effective total reactance (transformer and arm) and voltage and currents are given in RMS.

$$V_c = V_n + jX \cdot I_n \tag{4.8}$$

Substituting the current I_n using (4.2) yields.

$$V_c = V_n + jX\,(I_d + jI_q) \tag{4.9}$$

This may then be multiplied out and grouped by its real and imaginary components

$$V_c = (V_n - X \cdot I_d) + jX \cdot I_q \tag{4.10}$$

Real and reactive currents I_d and I_q can be replaced by power flows P and Q using (4.3) and (4.4)

$$V_c = (V_n - X\frac{Q}{V_n}) + jX\frac{P}{V_n} \tag{4.11}$$

The interface impedance X may be replaced by its per unit equivalent X_{pu}

$$V_c = \left(V_n - V_n \frac{Q}{S} X^{\mathrm{pu}}\right) + jV_n \frac{P}{S} X^{\mathrm{pu}} \tag{4.12}$$

The required converter voltage is then found by taking the magnitude. This can then be simplified by substituting $P^2 + Q^2$ with (4.6)

$$\begin{aligned} |V_c| &= \sqrt{\left(V_n - V_n \frac{Q}{S_B} X_{\mathrm{pu}}\right)^2 + \left(V_n \frac{P}{S_B} X_{\mathrm{pu}}\right)^2} \\ &= \sqrt{V_n^2 - 2V_n \frac{Q}{S_B} X_{\mathrm{pu}} + V_n^2 \frac{P^2}{S_B^2} X_{\mathrm{pu}}^2 + V_n^2 \frac{Q^2}{S_B^2} X_{\mathrm{pu}}^2} \\ &= V_n \sqrt{1 - 2\frac{Q}{S_B} X_{\mathrm{pu}} + \frac{P^2 + Q^2}{S_B^2} X_{\mathrm{pu}}^2} \\ &= V_n \sqrt{1 - 2\frac{Q}{S_B} X_{\mathrm{pu}} + X_{\mathrm{pu}}^2} \end{aligned} \tag{4.13}$$

Given that the maximum converter output voltage is limited by the dc voltage (4.5), the source voltage V_n must therefore be set so that the converter is able to deliver 1pu VA at a power factor of 0.95 (in reality the turns ratio of the interface transformer to give the appropriate nominal voltage). Eq. (4.13) can be rearranged to give (4.14), allowing the required V_n to be determined for a given dc voltage and effective impedance.

$$|V_n| = \frac{|V_c|}{\sqrt{1 - 2\frac{Q}{S_B} X_{\mathrm{pu}} + X_{\mathrm{pu}}^2}} \tag{4.14}$$

The critical condition is found when the converter is required to deliver maximum Q in the negative direction, as it requires the lowest source voltage. With the source voltage determined the rated current can be found, as given by (4.15).

$$\begin{aligned} S &= P + jQ \\ &= I_d \cdot V_n + jI_q \cdot V_n \\ &= (I_d + jI_q)\, V_n \\ &= I_n \cdot V_n \\ \therefore I_n &= \frac{S}{V_n} \end{aligned} \tag{4.15}$$

The capability of the converter is then constrained by the current and voltage limits imposed on the design. Figure 4.15 shows the possible PQ area of operation for a converter which is

designed to operate down to a power factor of 0.95, correlating to 333MVAr for 1000MW. The turns network voltage required, determined by (4.5), and the current rating required, determined by (4.15), allow the converter to meet the PQ requirements – shown by the rectangular area in Figure 4.15. The total capability of the converter is shown by the outer area marked. Real power and positive reactive power flow are constrained by the converter current capability, as Figure 4.15 shows. Negative reactive power flow constrained by the maximum converter output voltage, given by (4.5), which leads to an asymmetrical capability of the converter.

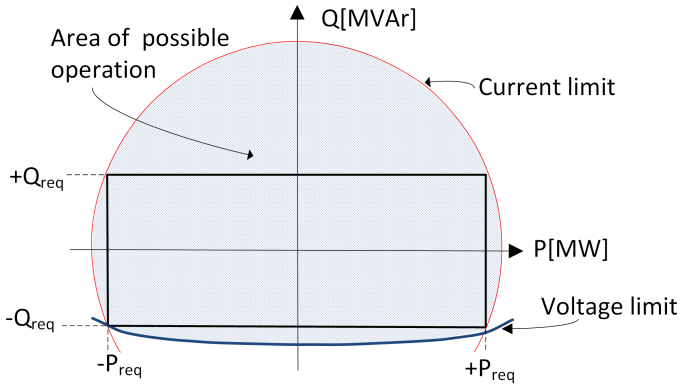


Figure 4.15: PQ diagram of converter capability

Eq. (4.14) can be substituted into (4.15) to give the relationship between interface impedance and the converter the rated current requirement (4.16).

$$|I_n| = S_B \cdot \frac{|V_c|}{\sqrt{1 - Q^{\text{-max}} \frac{2}{S} X_{\text{pu}} + X_{\text{pu}}^2}} \tag{4.16}$$

Eq. (4.16) demonstrates that as transformer or arm impedance is increased, and the transformer turns ratio reduced, converter current must increase, in order to maintain the same power throughput. Figure 4.16 gives a range of effective impedances and the current that is subsequently required. Current values are normalised against that at 20% pu impedance.

In the example given, an increase in impedance to 32% causes an additional 20% increase in rated current. For MMC systems, switching losses are relatively low (compared to 2-level converters) and system losses are dominated by conduction loss. The increase in impedance and current in normal operation is therefore highly undesirable when manufacturers compete on life-time losses.

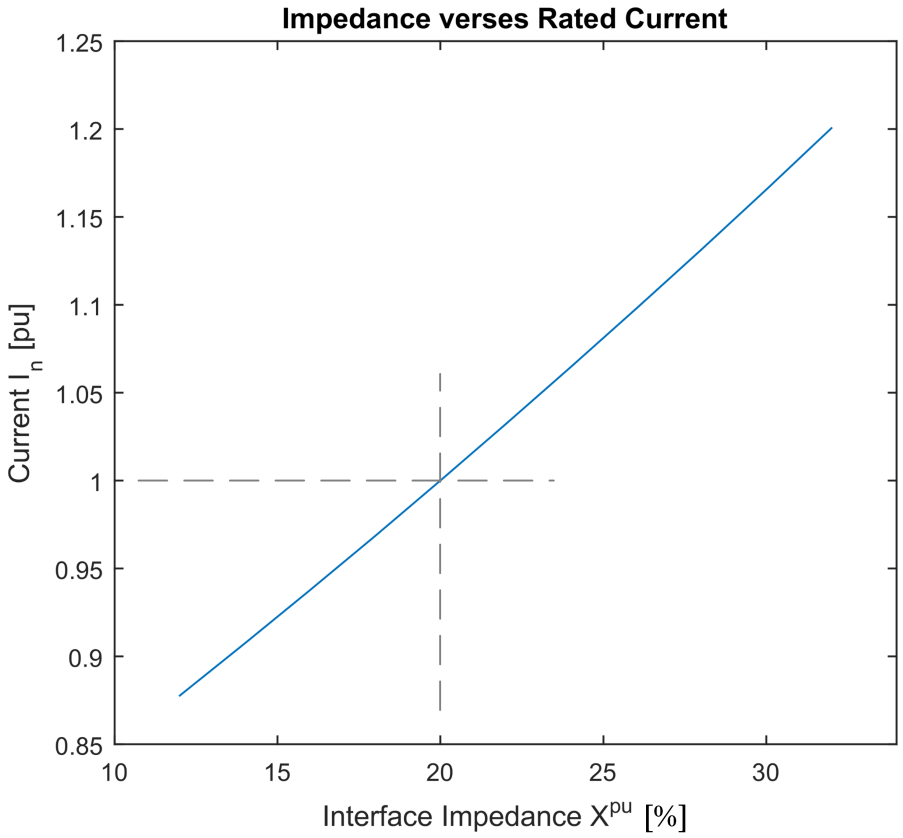


Figure 4.16: Converter current required for a range of interface impedances. Base current given at 20% impedance

4.5.2 DC Inductance

The primary purpose of including additional dc side inductance is to reduce the peak current stress through any dc side circuit breaker. Results shown in Section 4.4.3 demonstrated there is a significant reduction, provided dc breakers operate within the first 20ms of fault occurring.

However, the additional dc inductance leads to three main undesirable consequences. Firstly, large inductances will reduce the dynamic controllability of the converter, as it begins to behave closer to a current source than a stiff voltage source. Secondly, large dc inductances can have a high weight and volume. This is particularly an issue for offshore applications, where these two factors come at a premium. The third issue is related to the dc breaker's energy dissipation requirements; in the time between the fault occurring and dc breakers operating current increases on the dc side, storing energy within any dc side inductance. Additional dc side inductance may cause the energy stored to increase. This energy must be removed from the system by the dc breakers when they operate. In this case, one form of stress on the breaker may then be exchanged for a different form. In Chapter 6 the interaction between additional

dc inductance, fault current, and energy dissipation is analysed in detail.

4.6 Conclusion

High fault currents, in the order of 10kA, drawn through the converter under dc faults have the potential to irreparably damage semiconductors within the cells. The use of bypass thyristors has been shown to reduce current within the cell FWDs to a sustainable level. The converter is therefore able to sustain fault currents for an extended period of time and re-establish power flow once the fault has been isolated. The length of time for which these currents may be sustained is then a function of the energy dissipation capabilities of the bypass thyristors used, rather than the FWDs.

A method of quantifying stress to system equipment and devices was demonstrated. The quantitative method allows direct comparison of different fault cases with variable system parameters. For example, measurements of $\int i^2 dt$ indicate how much energy is dissipated over a given time period and may be used to select a suitable device.

Five sets of parametric studies have been carried out through simulation. Network impedance and transformer leakage have been shown to create much the same effect – a reduction in peak dc current along with a proportional decline in maximum device energy dissipation. The results highlight that changes in ac side inductances (such as network impedance and transformer leakage) have minimal effect on the time at which peak dc current is reached (there is marginal difference in peak dc current at t_3 and t_4). This implies that (to reduce the peak current) dc breakers must operate within this transient period (approximately 10ms), while current is still rising. Beyond this time-frame circuit breaker operational speed is driven by HVAC system dynamics. Results show that variable arm inductance was more influential on peak current and overshoot, as it is in the dc path, than on stead-state current, due to its smaller impedance relative to that of the ac network and transformer.

The system must be designed to withstand the stress under worst case fault for system parameters that are not under the control of the designer, such as network impedance and fault resistance. However, parameters that are available to the system designer, such as additional dc and arm inductance, can impact on operation during normal operation. Analysis was provided to demonstrated how increased ac impedance can lead to higher currents during normal operation, and thus increased life-time losses. Increasing dc inductance has the potential to increase circuit breaker energy dissipation requirements, which is analysed in detail in Chapter 6.

Chapter 5

HVDC Circuit Breaker Technology Review

5.1 Introduction

Circuit breakers within ac systems have a substantially easier task than those within a dc system. AC breakers are not required to 'break' current in the sense that they create current zeros. These in fact occur naturally even during faults, with external circuitry, such as rotating machinery, driving currents through zero twice per cycle. These provide an opportunity for the circuit breaker to diffuse any arc between the contacts without generating excessively high voltages. The key design requirement of the ac breaker in fact is to sustain the arc without significant contact erosion until current reaches zero and then withstand the transient recovery voltage immediately after current passes through zero.

Circuit breakers for dc systems have a greater task. With no naturally occurring current zeros they must artificially force one within the system. A simplistic circuit may be used as an example to illustrate the problems this creates for circuit breaker design. Figure 5.1 shows the most basic form of a dc system under fault, which is cleared with a dc circuit breaker. The upstream (healthy) area of the system may be thought of as a dc voltage source (battery) with an inductance included to represent system self-inductance. To drive the current from its pre-fault, positive value a negative di/dt must be generated. Simple application of KVL, giving (5.1), shows that to accomplish this the breaker voltage (V_{cb}) must exceed the source voltage. Although this model is overly simplistic – for instance, it does not take account of the internal resistance of the source, which will limit the maximum current – it does demonstrate that a dc

breaker must generate a voltage in exceed that of the system. All dc breakers operate under the principle outlined here; all must generate a counter voltage in order to reverse the di/dt initiated by the fault. Circuit breaker types are then categorised by the method by which they create counter voltage – be that current commutation, resonance or otherwise.

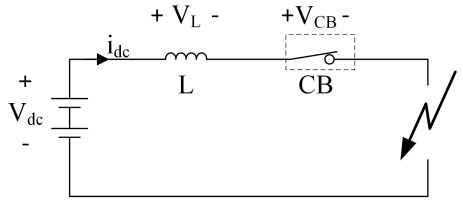


Figure 5.1: Generic DC breaker

$$\frac{di_{\mathrm{dc}}}{dt} = \frac{V_{\mathrm{dc}} - V_{\mathrm{cb}}}{L} \tag{5.1}$$

The second challenge in designing dc breaker is energy dissipation. The majority of energy that is introduced to the system during a fault in an ac system[1] is cycled back to the source when current reaches zero and very little energy must be dissipated within the circuit breaker itself. In contrast the dc breaker must absorb the stored energy within the system along with that which is introduced by the source during the breaking period. If this energy is not dissipated in the correct manner components may be damaged, leading to breaker failure. The duties which a dc breaker must perform can be summarised as follows:

1. In the closed position a circuit breaker must sustain the rated continuous current, without damage.
2. In the open position it must have the dielectric strength to withstand the open circuit system voltage.
3. During the transient phase, changing from closed to open position, the circuit breaker must provide a counter-voltage in excess of the system voltage.
4. During the breaking transient, it must absorb and/or dissipate the stored energy within the system

5.2 DC Breaker Building Blocks

DC circuit breakers are generally more complex than their ac counterparts, as they must create an artificial current zero. For HVDC applications, the circuit breakers are typically constructed

[1] High fault currents store additional energy within the system inductance

from several distinct components which work together to generate a counter-voltage, current zero and dissipate energy. As these components are common to most of the circuit breaker designs they are described in this section to save repetition.

5.2.1 Metal Oxide Surge Arrester (MOSA)

The ideal non-linear resistor is a two terminal device with an infinite resistance while terminal voltage is below the threshold value. At the clamping voltage (V_{clamp}) it appears as a fixed voltage in series with zero impedance, as shown in Figure 5.2. The result is a bidirectional element that clamps the voltage for any current.

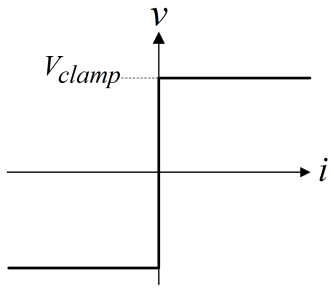


Figure 5.2: Ideal non-linear resistor voltage-Current characteristics

Non-linear resistors for high power, intermittent operation are constructed from a metal-oxide materials (typically Zinc). The metal-oxide (MO) resistor which is formed has a low leakage current below the clamping voltage and a low resistance above. The length of the device determines the clamping voltage, its area to the current carrying capability (which is related to its energy dissipation capability). MO resistors are connected in series to provide the required clamping voltage and encased in a housing, as shown in Figure 5.3, forming a Metal-Oxide Surge Arrester (MOSA).

Practical non-linear elements, such as the MOSA, exhibit non-ideal behaviour, as shown in Figure 5.4. During normal operation, where terminal voltage is lower than the clamping voltage, a small leakage current is drawn. This must be kept low to in order to avoid excesisve energy dissipation, which can lead to thermal runaway. In HVDC breaker applications the purpose of the arrester is to absorb energy when the breaker operates. In normal operation the arrester is short circuited by the breaker itself and therefore quiescent energy dissipation from leakage current is not a primary concern. The MOSA will exhibit a finite resistance once the clamping voltage is reached, unlike an ideal non-linear resistor. This causes a small rise in voltage as current begins to be drawn into the arrester. As such, the breaker should be designed to withstand the terminal voltage of the arrester for the required surge current.

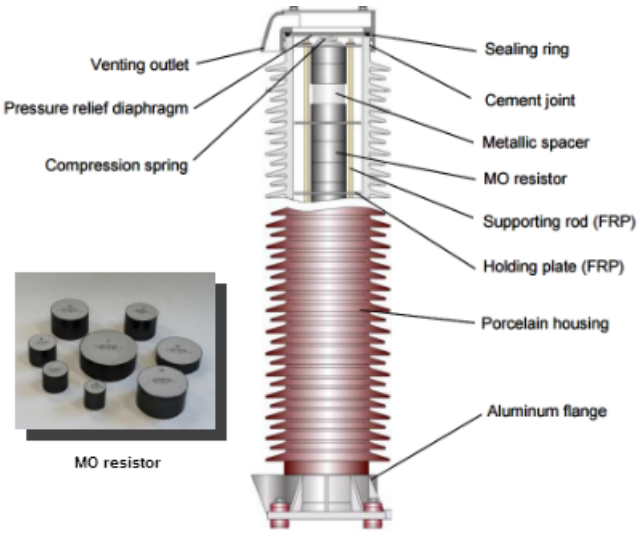


Figure 5.3: Metal-Oxide Surge Arrester [67]

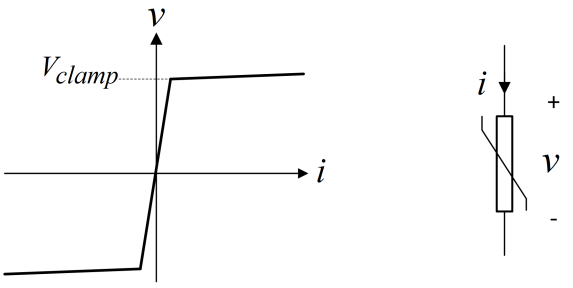


Figure 5.4: MOSA Voltage-Current characteristics and circuit symbol

MOSAs are used extensively within HVDC circuit breaker designs as they ensure the voltage is constrained (across internal elements, such as IGBTs, and external system elements, such as cables) and can remove the system energy more readily than other means, such as an arc. Excessive energy dissipated within the breaker, which translates into a temperature increase, can lead to permanent damage of the MOSA and mal-operation of the circuit breaker itself. Therefore, the energy dissipation capability must be considered, as much as peak current, when specifying the circuit breaker requirements.

5.2.2 Disconnector

The disconnector is a mechanical switching device. In the open position the contacts provide enough separation to ensure adequate voltage withstand. In the closed position it has the ability to conduct rated and fault current levels. It is intended to open or close a circuit under negligible current conditions. The disconnector is therefore only used for zero current switching operations. It is capable of carrying rated current under normal conditions and short circuit through currents for a specified time [68, p. 468].

For HVDC breakers applications they can be used to short circuit other circuit elements, providing a very low resistance/low loss path when compared to a semiconductor alternative. They can also be used to provide galvanic isolation between the breaker and the external network (a path of leakage current is often present through MOVs once circuit breakers are in the open position). The advantage of using disconectors over ac breakers for these tasks is actuation speed. As disconnectors are not designed to interrupt current in the open position there is no arcing between the contacts. They do not suffer the same erosion as that of the ac breaker – which have to sustain current flow in the open position – and therefore have a lighter mass, allowing faster actuation. However, in order to open under zero current conditions other circuit elements must first divert current from them. In [69] the ultra-fast disconnector developed for the ABB Hybrid HVDC circuit breaker was presented, shown in Figure 5.5. The novel topology allows for an increased speed over standard designs by separating the voltage stress over many interlaced contacts.

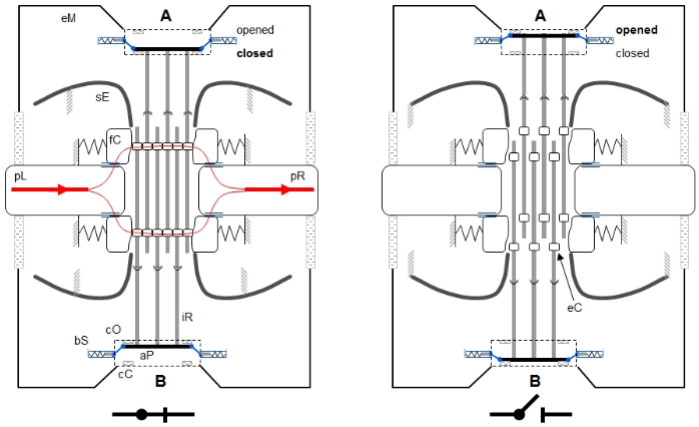


Figure 5.5: Ultra fast disconnector presented in [69]. Actuator movement perpendicular to current flow direction. In the close position (left) and open position (right)

5.2.3 AC Circuit Breaker

An ac circuit breaker is a mechanical switch used to isolate parts of the system from one another. Critically is can be opened under load or fault current, differentiating it from the disconnector. The switch consists of two contacts and an insulation medium. The dielectric strength between two open contacts in the open position is related to their separation distance and the insulation medium.

When contacts are opened under current an arc is formed between them, due to the inductive nature of most circuits. The external circuit forces current to pass through zero, at which point the arc will diffuse. The residual plasma within the chamber does not diffuse instantaneously,

which leads to a decreased dielectric strength between the contacts. The transient recovery voltage (TRV), the rate at which voltage is applied after current passes through zero, must be kept within acceptable limits to ensure that the arc does not re-strike.

AC circuit breakers are used within some dc breaker topologies and current zero crossings are created artificially. The rate at which current is brought to zero, and the subsequent dv/dt, is much more extreme than that found in ac applications [24]. Where an arc has been present dc breakers must delay the application of voltage in order to allow the arc plasma to diffuse and avoid re-strike. This 'de-ionisation time' reduces the speed of operation of the dc breaker and has led new topologies, for VSC applications which avoid arc occurring.

Vacuum circuit interrupters – ac breakers which use a vacuum as the insulation medium – are commonly used with dc breaker designs as the arc plasma is rapidly diffused. Voltage ratings of individual units are generally somewhat limited (when compared to SF_6 equivalents), typically to around 80kV, requiring series/hybrid connections to achieve the required voltage withstand [70, 71].

5.3 DC Breaker Fundamentals

To generate the counter-voltage required to produce a current zero within a dc system several techniques may be used. As the voltage, current and energy dissipation requirements increase different circuit breakers topologies have been investigated. To deal with these increased demands, HVDC circuit breakers have become much more complex than those for low voltage applications. In this section the general operating principles of dc breakers are reviewed. Circuit breaker topologies, and their restrictions, for different power levels are then discussed.

5.3.1 Purely Mechanical DC Breaker

The most basic form of dc breaker is a simple mechanical switch. Dielectric strength in the open position is determined broadly by the contact separation and insulation medium. Triggering the breaker causes the contacts to separate into the open position. The stored inductive energy within the network results in a high voltage across the breaker contracts, insulation breakdown and associated arcing.

For low voltage applications, such as automotive and marine, the arc voltage may exceed the system voltage sufficiently and thus produces a negative di/dt, with only a moderate contact separation. Typically ac breakers that have a dc breaking capability have been used where voltages of approximately 270-700V are met [72].

At higher system voltages the circuit breaker counter-voltage must also be greater. A larger contact separation can be used to accomplish this. However, travel distances and time can become excessive to attain the required dielectric strength. Arc chutes may be used to artificially lengthen the arc, and thus increase its voltage, until it exceeds that of the source voltage. An example of an arc chute is given in Figure 5.6. The arc moves along the runners and into the splitter plates breaking it into many sections and increasing the voltage. This method is typical for medium voltage dc applications [72], such as rail traction.

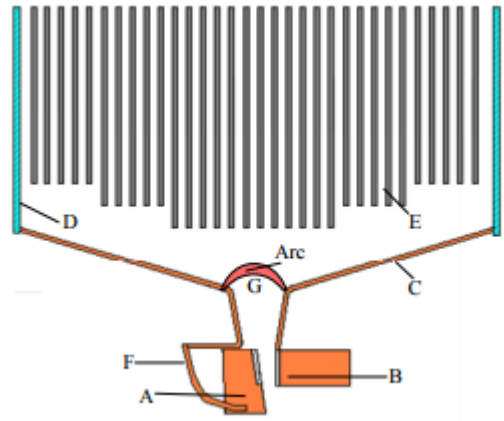


Figure 5.6: Arc chute system used for air insulated dc circuit breakers. (A) Moving Contact. (B) Fixed Contact. (C) Arc runner. (D) Insulating wall. (E) Splitter plates. (F) Flexible copper wire. (G) Entrance of arc chamber. [72]

The stored energy in the system is dissipated as heat within the arc and metal plates, causing erosion. In higher voltage and power applications, where the required speed and energy dissipation requirements increase, this topology becomes unfavourable. Moreover, the time taken for the arc to build up to its nominal counter-voltage is not insignificant: Even for the reasonably low voltage (1800V) example given in [72], it takes approximately 10ms for the arc to lengthen and produce the desired voltage, which does not take into account actuation time of the mechanical components. For HVDC applications, this is likely to make the overall circuit breaker operation too long.

5.3.2 DC Circuit Breaker Commutation Principles

Where the circuit breaker requirements cannot be met by a simple mechanical device, more complex topologies are available to further increase the counter-voltage. For these applications, it is common for the circuit breaker's functions (inserting a counter voltage, dissipating energy and providing open-circuit voltage-withstand) to be performed by different components, where previously they were performed by the mechanical contacts and resulting arc. To accomplish

this the circuit breaker is constructed from several distinct sections, each performing a specific role.

Many dc circuit breaker topologies have been proposed for this purpose, each of which rely on current commutation of some form. The most generic form is shown in Figure 5.7. During normal operation (closed position) current is carried in the primary branch and the other branch(s) are open circuit. When the breaker is tripped the current is commutated from the primary branch into a secondary branch, which produces the circuit breaker counter-voltage. Often a third branch is used to dissipate the energy absorbed during breaking, although in some cases the secondary branch performs both the counter-voltage and energy dissipation functions.

Current commutation from the primary to secondary branch is typically forced by current superposition (resonance) or inserting a small counter-voltage in the primary branch. The stray inductance of the circuit (L) of the current loop causes a counter-voltage to be generated upon a change in current. The voltage generated by the primary branch therefore needs to be large enough to overcome this in order to commutate the current in a relatively short period of time. Separation of the tasks allows each branch to be optimised to perform its given task; e.g. by generating a counter-voltage in the secondary branch a higher voltage can be achieved than is possible from an arc in the primary, in the case of the purely mechanical breaker.

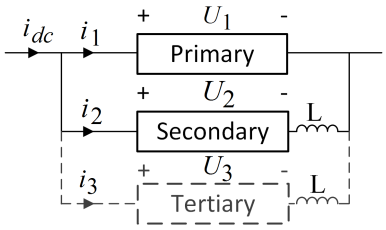


Figure 5.7: Generic form of dc breaker which encorperates commutation. Pramary branch for current carrying during normal operation, secondary for current commutation/energy dissipation and tertiary (optional) for energy dissipation

5.3.3 Example Commutation Topology

The circuit shown in Figure 5.8, was explored in [73]. The primary branch consists of an ac (mechanical) circuit breaker S_m. Semiconductor switches are used as an electronic circuit breaker (see Section 5.5) in the secondary branch[2]. These must have both turn-on and turn-off capability, and thus IGBTs, GTOs or similar devices may be used. The third branch contains

[2]Within [73] this topology is designation 'hybrid', to differentiate it from purely mechanical circuit breakers, as it combines both power electronic devices and mechanical circuit breakers. However, most circuit breaker topologies that are applicable for high voltage dc now utilise both power electronic and mechanical components. For this reason the topology is not classed as 'hybrid' within this thesis, as discussed in the section covering hybrid circuit breaker topologies.

an MOSA to dissipate the energy absorbed during current breaking and only switching energy is dissipated within the semiconductors.

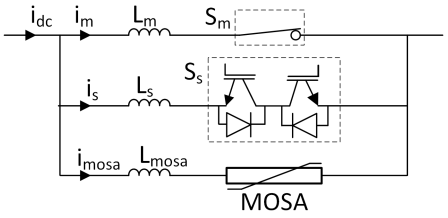


Figure 5.8: Combination of power electronic and mechanical switches to commutate current

In the closed position current passes through switch S_m, which has a low impedance. The circuit breaker is operated by opening S_m while simultaneously turning on the semiconductors in the secondary branch (S_s). The arc voltage within of S_m causes current to commutate between the primary and secondary branch. When current has fully transferred (i_m=0) the arc plasma will diffuse and S_m will begin to build-up dielectric strength. Once it can support the MOSA clamping voltage, S_s is switched off. When the voltage approaches the surge arrester clamping voltage (set by the MOSA) current will commutate from the switches into the MOSA. The counter-voltage across the circuit breaker then remains close the clamping voltage whilst current decays, dissipating energy built up during the fault in the process.

5.3.3.0.1 Benefits A higher counter-voltage may be achieved as it is produced by the MOSA and not the arc of the ac circuit breaker. Energy dissipation is not performed by the ac breaker, reducing wear, weight and complexity. The arc voltage needs only be large enough to commutate the current. This can be achieved with moderate contact travel distances and does not require arc lengthening. In the closed position losses are low as current is passed through the mechanical switch, providing a low loss path for normal operation.

5.3.3.0.2 Restrictions The residual plasma within the chamber must diffuse before the mechanical switch regains the required dielectric strength and can support voltage without re-striking occurring. So that re-strike does not occur there is an artificial delay between the current commutating into the secondary branch and S_s turning off (applying a counter-voltage), which can result reduces the a increased operation time. In higher voltage applications, where the stray circuit inductances L_m,L_s, and L_{mosa} increase, commutation times are also increased or a larger voltage is required.

5.3.3.0.3 Applications For low voltage applications the circuit can provide adequate performance as the on-state voltage of S_s is low, the loop inductance is small and the de-ionisation time can be tolerated. For high-voltage applications, such as HVDC, the on-state voltage of S_s is higher (due to the larger number of devices) and loop inductance is larger (due to the larger physical dimensions of the breaker). This requires a larger arc voltage to force commutation, which is limited by mechanical switch design. As previously described, arc chutes may be used to increase the commutation voltage. However, they increase the volume/weight of the breaker and the time it takes to build up arc voltage is not insignificant, as shown in [72, 74].

5.3.4 High Voltage DC Breakers

In high-voltage applications dc circuit breakers are required to produce a counter-voltage in the range of hundreds of kilovolts. The principles described previously are not appropriate when attempting to commutate such large currents at such high voltages and the topology becomes impractical.

Development of circuit topologies which could successfully interrupt dc at the current and voltage levels associated with HVDC initially started in the 1970s, after the early proposal of multiterminal HVDC networks [75]. The first topologies used a standard, high-voltage ac circuit breaker with the addition of a commutation circuit to force a current zero. Demonstration units, some at full scale, were tested in the 1980s [25, 76, 71]. However, large scale HVDC multi-terminal grids did not materialise and these never went into commercial production.

In the last ten years the expansion of offshore wind farms, often connected by VSC HVDC, has renewed interest in HVDC breakers as it gives the potential for individual connections to be meshed. Generally, it has been perceived that the technologies developed in the 1980s for LCC are too slow for the newer VSC installations and are not appropriate [28, 77]. This has resulted in a surge of research and development in the field to develop breakers with much faster operational capabilities [73, 26, 78]. Key manufacturers within the HVDC market have proposed their own designs and demonstrated scaled prototypes, although these have also yet to be installed in a commercial setting [28, 27, 79].

In this chapter circuit breaker topologies applicable for HVDC are analysed. Costs for finished products are not readily available as pricing information is commercially sensitive, making a totally quantitative comparison between technology types difficult. Instead, the key topologies which are generally suitable to the voltage and current requirements of HVDC are summarised in a more qualitative way. For each topology the operation principles are described and comment is given to the suitability in a practical application. The area is still under intense

and continuous development; a standardised system architecture and protection strategy have not yet become clear and circuit breaker design is constantly being improved. Therefore, at this stage it is not possible to provide a generic 'best solution'.

5.4 Resonant Circuit Breaker

LCC offers the ability to limit fault current by converter control, which is sufficient in point-to-point systems. However, during the 1970s it was envisioned that thyristor-based LCC systems were to expand into multi-terminal systems and therefore dc breakers would be required to isolate faulted segments of the system [75]. The resonant circuit breaker was developed to fulfil this requirement [80].

The general topology of a resonant dc circuit breaker is shown in Figure 5.9. The basic circuit consists of a standard, high-voltage ac circuit breaker in parallel with a resonant circuit, which is used to create a current zero through current superposition. By default, switch S_1 is in the closed position, allowing load current to flow. Its mechanical construction leads to a minimal loss during normal operation. The secondary, parallel branch contains passive elements in series with a second switch S_2. In the earliest designs a spark-gap was used to initiate the resonant circuit [24]. As semiconductor capabilities have vastly improved since the first designs in the 1970s typically thyristors are used for S_2, giving more precise control of the resonant circuit operation [81].

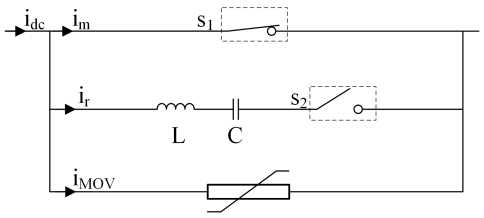


Figure 5.9: Generic Resonant Circuit Breaker Topology

A current zero is created in the main circuit breaker S_1 by inducing a current oscillation in the secondary branch. As the total current i_{dc} remains near constant during the commutation period, the additional current within the resonant branch (i_r) is subtracted from the main breaker (i_m). If the magnitude of the resonant current exceeds i_{dc} then through S_1 will pass through zero. When the current zero occurs the arc plasma diffuses and S_1 starts to regain dielectric strength. S_1 is then open circuit and current must pass fully through the secondary branch, charging the capacitor (C) and providing a counter-voltage which is clamped by the parallel MOSA.

There are two methods of initiating current resonance within the breaker: through current injection from a pre-charged capacitor, a principle known as 'active resonance', or by taking advantage of the negative resistance characteristics of the arc, known as 'passive resonance'. The two principles are now described in more detail.

5.4.1 Passive Resonance

In this section an overview of how the passive resonant topology may be used to generate a current is given. A detailed description of the operational theory of the passive circuit may be found in [82]. The general circuit topology of the passive resonant circuit breaker is shown in Figure 5.10. To activate the breaker, the thyristors in the secondary branch are triggered and a short circuit is created. At the same time the mechanical switch (S_1) is opened, resulting in an arc voltage. Applying KCL around the two branches that form a loop the current in the main breaker (i_m) can be found, as given in (5.2). The arc plasma exhibits what is commonly referred to as a 'negative resistance' characteristic as the voltage potential difference between the breaker contacts reduces as current increases (see Figure 5.10). This phenomena causes the resonant current to increase exponentially, as dU_{arc}/di_m is negative (k is negative, see Figure 5.10).

$$i_m = I_{dc}\left[1 + e^{-\frac{k}{2L}t} \cdot \sin(\omega_c t)\right] \text{ , where } k = \frac{dU_{arc}}{di_m},\ \omega_c = \sqrt{\frac{1}{LC}} \tag{5.2}$$

When the magnitude of resonant current reaches the same magnitude as the dc current the arc will extinguish, allowing the contacts to begin to support voltage (t_1). All current is now passed through the lower branch, and thus the capacitor voltage will increase until it reaches the clamping voltage of the parallel MOSA (t_2). System energy is then dissipated until the current is driven to zero.

The passive resonant circuit relies heavily on the arc voltage characteristic, between the circuit breaker contacts, to force the response. It can take in the order of 10ms for arc voltage to build-up [25]. In VSC based systems peak current can occur within the 10ms-20ms time frame, as was demonstrated shown in Chapter 3. As such, 10ms overhead for arc voltage build-up represents a significant time overhead. However, the topology is used extensively for applications such as metalic return transfer breakers (MRTB) within bipolar LCC systems, where operation within the 10ms time-frame is not essential. Moreover, in these applications the circuit breaker is only required to withstand a partial rating of the system voltage, rather than in excess of it, easing the design process.

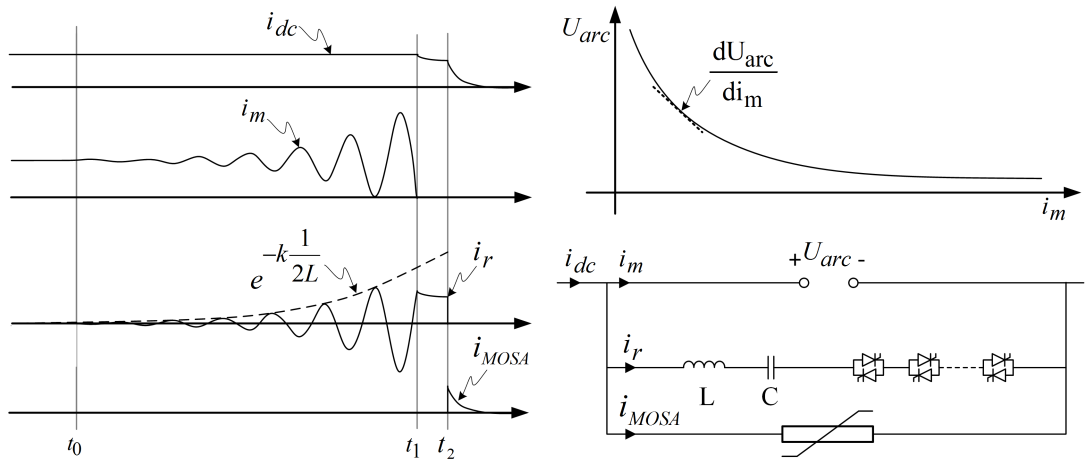


Figure 5.10: Operation of the passive resonant topology

5.4.2 Active Resonance - Current Injection

Creating a current zero through the use of passive resonance relies heavily on the arc characteristic of the mechanical switch. Alternatively it is possible to force a current zero within the mechanical switch by active current injection (current superposition). In this case the capacitor in the resonant branch is pre-charged to a voltage of (V_{c0}) and switch S_2 is initially open.

At t_0 the main circuit breaker S_1 is opened and S_2 is closed (by firing the thyristors), causing current to discharge from the capacitor around the loop formed by the resonant branch and main branch. Typically the arc voltage is small when compared to the capacitor pre-charge voltage and can be treated as a short circuit to simplify the analysis. The prospective current in the main branch is then given by (5.3).

$$i'_m(t) = I_{dc} - V_0\sqrt{\frac{C}{L}}\sin(\omega t) \tag{5.3}$$

When the resonant current magnitude matches that of the dc current a zero current condition is generated at time t_1 (see Figure 5.11). From $t_1 \rightarrow t_2$ current flows fully through the secondary branch and S_1 begins to regain dielectric strength as the arc has extinguished. Charge on the capacitor is increased and when the voltage reaches the clamping level of the MOSA, at t_3, current is diverted into the MOSA. Between $t_2 \rightarrow t_3$ the MOSA clamps and current is reduced until all energy is absorbed.

The peak of the resonant current is determined by the passive components in the resonant branch and the pre-charge voltage. In order to successfully bring the current in S_1 through zero the condition (5.4) must be met. Typically the resonant circuit is designed to produce a peak current of twice that of the required breaking current, to ensure that a current zero is created

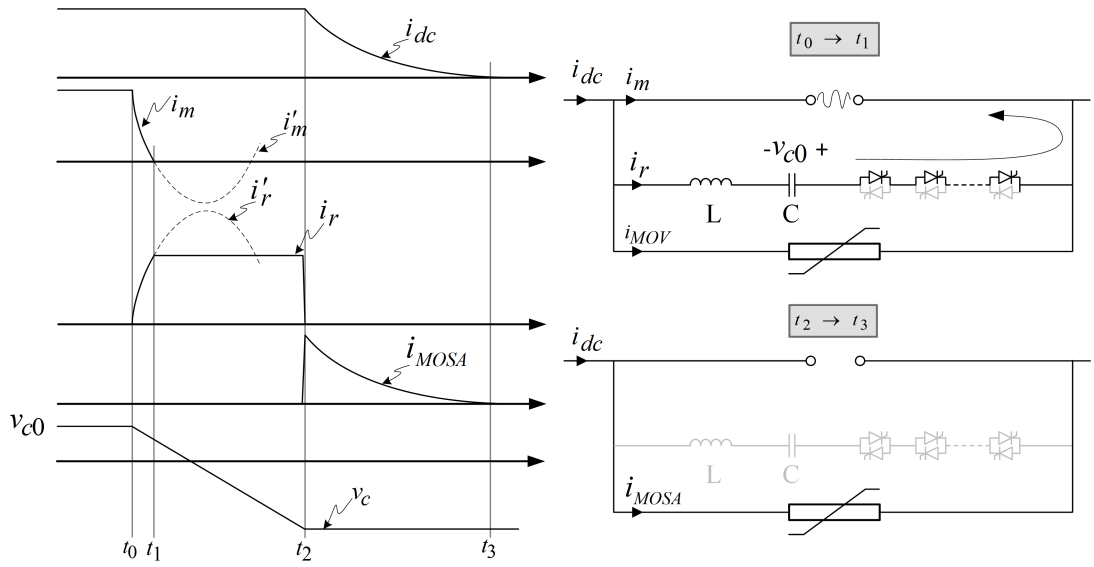


Figure 5.11: Operation of the active resonant topology

[24].

$$V_0\sqrt{\frac{C}{L}} > I_{dc} \tag{5.4}$$

5.4.3 Present Development

The resonant topology has been revisited more recently for VSC based applications. The projected high cost of hybrid circuit breakers, with faster operating speeds, has led to the resonant topology being revisited. In [79] Mitsubishi Electric announced a mechanical circuit breaker aimed at the HVDC market. The breaker has a high current breaking capability of 16kA. Key figures that are publicly available are given in Table 5.1. Figure 5.12 shows the circuit breaker test circuit.

Table 5.1: Technical Specification of Mitsubishi Mechanical Circuit Breaker [79]

	Value		Notes
Nominal Voltage	-	kV	Based on ±320kV system. However, voltage of tested device is not stated within paper
Maximum rated current	16	kA	
AC breaker	-	-	Vacuum Circuit breaker. Characteristics unknown
Operational speed	10	ms	It is unclear if this times period to build up counter-voltage or to clear the fault completely

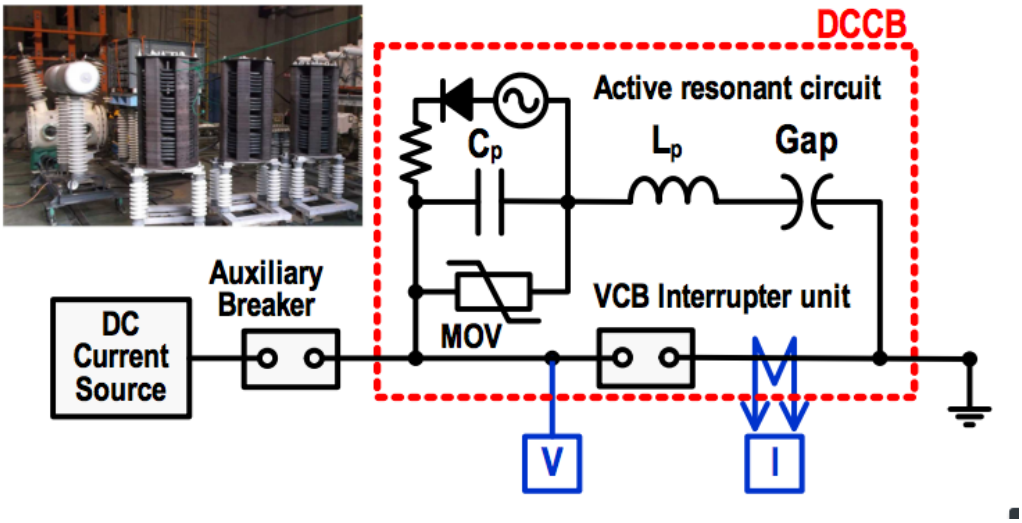


Figure 5.12: Mitsubishi mechanical circuit breaker topology and test system [79]

5.5 Electronic Circuit Breaker

Electronic circuit breakers have been investigated for both ac and dc applications, where ultra-fast disconnection is required. With no mechanical parts to actuate or arc plasma to diffuse they represent the fastest form of all dc breaker topologies available. The rate at which they are able to produce a counter-voltage is only constrained by the semiconductor devices themselves (typically within a few tens to hundreds of microseconds).

The most simplistic electronic breaker consists of a semiconductor in series with the load. Where bidirectional current flow is required devices are connected back-to-back. When the breaker is tripped these are turned off forcing current into parallel MOSAs which constrain the voltage rise across the devices, ensuring they are maintained within the safe area of operation. The combination of a semiconductor switch(s) and a voltage clamping device forms the basic electronic circuit breaker module.

The ratings of commercial available semiconductors limits the capability of the single device breaker. High voltage applications such as HVDC require counter-voltages typically be in the order of 450kV to 600kV. To achieve this modules (consisting of two IGBTs, snubbers and an MOSA) are connected in series.

The general topology for a high-voltage electronic dc breaker is as shown in Figure 5.13a. In each module two semiconductor switches are present, to enable bidirectional power flow. The number of series modules is chosen based on the nominal system voltage and insulation coordination.

5.5.1 Operation

During normal operation all switches are turned on. At any time current will flow through one diode and one IGBT in each module. In the positive direction current flows through the devices as shown in Figure 5.13b and in the negative direction current flows as shown in Figure 5.13c. When the circuit breaker is tripped all devices are gated off. As the device comes out of conduction the collector-emitter capacitance will charge, increasing the voltage across the device. When the clamping voltage is reached current will divert into MOSAs, as shown in Figure 5.13d. In this way the devices are maintained within their SOA. The total voltage across the breaker once opened (V_{cb}) is sum of the module voltages ($N \cdot V_{\mathrm{MOSA}}$), where N is the number of modules used and V_{MOSA} is the surge arrestor clamping voltage.

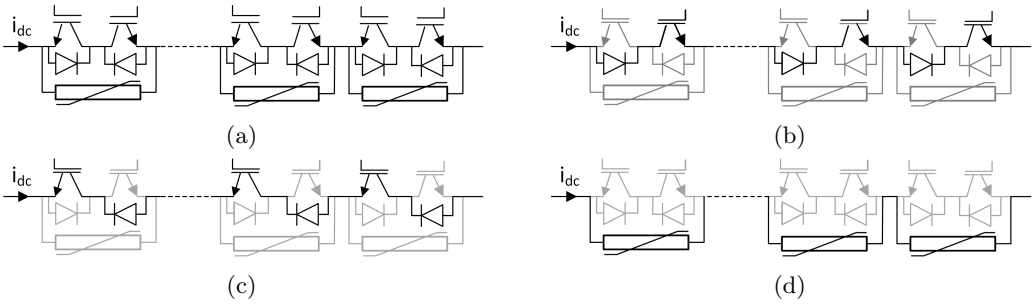


Figure 5.13: Electronic circuit breaker operation

5.5.2 Loss Considerations

While in the 'closed' position, the full pole current is passed through the semiconductors within the electronic dc breaker. Due to the finite voltage drop across each device a continuous loss is incurred. The loss of the overall circuit breaker can be estimated by calculating the number of modules required, based on over-voltage, device utilisation and rated power throughput and device current-voltage (I-V) characteristics. Table 5.2 describes the values used for the sample calculation given. A device blocking utilisation factor of of 0.6 is assumed to allow for transient over-voltage due to stray inductance within the module.

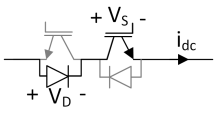
Loss can be approximated using (5.5), where V_{s0}, R_s, V_d and R_d are found using linear approximations from device data-sheet I-V curves. Figure 5.15 shows a comparison of losses based on a number high-voltage IGBT/diode devices from a variety of manufactures. The loss comparison of electronic circuits, given in [83], indicates that thyristors based semiconductor devices, such as GTO and GCT, are favourable over IGBTs. However, in dc applications, where the devices are hard switched, the drive requirements are significant [27]. For this reason IGBT

Table 5.2: Values used for HVDC Electronic Circuit Breaker Loss Calculation

	Value		Notes
Rated dc voltage	700	kV	350kV per pole
Rated power	1000	MW	
Device utilisation	0.6		40/% margin to allow for overshoot
Breaker over-voltage	1.5		Relative to rated dc voltage

solutions are considered here. Losses are expressed for a single circuit breaker relative to a 1000MW converter.

As V_{s0} and V_{d0} do not increase linearly with blocking capability higher voltage devices are more favourable, from a loss perspective, as demonstrated in Figure 5.15. However, capital cost of the devices, redundancy provided, cooling requirements and instillation complexity must also be taken into account during optimisation of the breaker design, which is outside of the scope of this thesis.



$$P_{\text{loss}} = N \cdot i_{\text{dc}} \cdot (V_d + V_s)$$
$$\text{Where} \begin{cases} V_s = V_{s0} + R_s I_{\text{dc}} \\ V_d = V_{d0} + R_d I_{\text{dc}} \end{cases} \tag{5.5}$$

Figure 5.14: Losses in electronic circuit breaker during normal operation

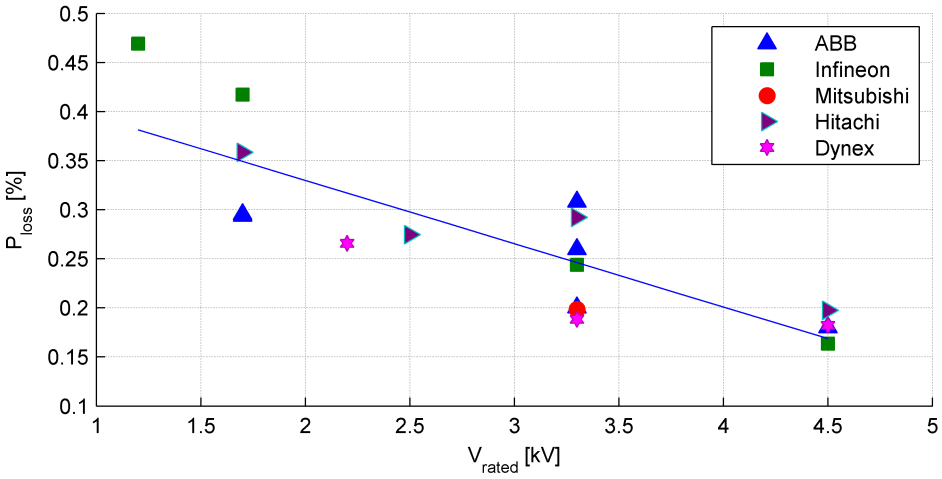
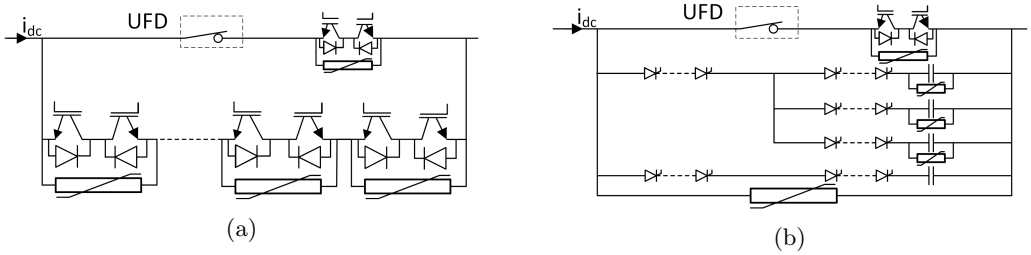


Figure 5.15: Electronic circuit breaker losses for various IGBTs, expressed as a fraction of 1000MW rated power. Calculation based on a single, unidirectionally blocking breaker

5.6 Hybrid Circuit Breakers

Both active resonant and passive resonant breaker topologies make use of a mechanical actuators which open under fault current leading to an arc being drawn. The plasma within the chamber must diffuse so that the breaker can sustain applied voltage without re-strike. The result is that operation must be slowed to allow the breaker to build up di-electric strength. Purely electronic breakers have a clear advantage in speed as there is no mechanical actuation time, arc plasma or re-strike issues. However, the power dissipation (loss) during steady-state operation is undesirable.

Hybrid topologies have been developed to combine the attributes of both solid state technology and ultra-fast disconnectors (UFD) to give high speed in combination with low loss. Within this thesis hybrid circuit breakers are categorised as those that include a semiconductor switch within the main branch for the purposes of current commutation. Several dc breaker concepts were introduced under the term hybrid in [73], as they included a both semiconductor and mechanical switches within the circuit. However, none of these topologies included a semiconductor element within the main path and therefore are not designated hybrid within this document. The two hybrid topologies which fulfil this requirement are shown in Figure 5.16.



(a) (b)

Figure 5.16: Hybrid circuit breaker topologies. (a) ABB topology (b) Alstom topology

The upper branch of each topology, which carries current while the closed position, contains a semiconductor switch, termed the 'auxiliary switch' or 'load commutation switch', and a mechanical switch. The mechanical switch UFD is an ultra-fast disconnector that is not capable of breaking current and used purely to provide galvanic isolation. Typically this is capable of opening within 1ms-2ms.

The auxiliary switch is used to commutate current out of the main branch, so that the UFD may open under zero current – thus avoiding any arcing. Once the contacts reach the required distance voltage may be applied immediately with no requirement to delay during de-ionisation as no arc is drawn. This means that there is a short time period from the circuit breaker being triggered counter-voltage being produced across the breaker.

The time period for commutation is a function of on-state voltage of the electronic circuit breaker, voltage rating of the auxiliary branch and loop inductance. The physical layout of the circuit breaker should be optimised in order to minimise the loop inductance. The composition of the load commutation switch requires optimisation for each circuit topology. However, the study performed in [84] used a 3x3 matrix connection of 4.5kV IGBT devices for use within a 320kV circuit breaker, representing a 24:1 voltage ratio between the load commutation switch and secondary branch. The additional branches in each topology provide a path for fault current to flow whilst the mechanical switch is opening.

Losses in the closed position are larger than those of resonant topologies, as current is carried continuously through the auxiliary switch. However, conduction losses may be minimised with the use of paralleled IGBTs. Power dissipation is quoted to be within several tens of kilowatts only [26]. Cooling requirements are therefore low and generally natural convection is sufficient [27]. As the hybrid circuit breaker operation time is dominated by the time period the mechanical actuator takes, rather than commutation time, the auxiliary switch's voltage clamping level may be relatively low allowing a single device to be used and thus losses reduced.

5.6.1 Proactive Hybrid Circuit Breaker Operation

The proactive circuit breaker topology was proposed in [28]. It combines an UFD and semiconductor auxiliary switch in the main branch with an electronic circuit breaker in a secondary branch, see Figure 5.16a. Technical specification of the device are given in Table 5.3. A single cell of 80kV has been successfully demonstrated, supplied by a ±150kV HVDC switch-yard. Currently maximum current is limited to below 10kA, beyond which the the IGBTs can saturate causing failure. A new generation of devices – Bimode Insulated Gate Transistors (BiGT) – is reported to allow the breaker to operate at up to 16kA [26].

Under normal (closed) operation current is carried via the mechanical switch and auxiliary switch (see Figure 5.17a). When the breaker is triggered the auxiliary switch is turned off, building up voltage across until the parallel MOSA clamps (see Figure 5.17b) and causing current to commutate out of the primary branch and into the secondary.

Once current through UFD has reached zero it can begin to actuate. During the actuation period all current is passed through the secondary branch (Figure 5.17c). Once the mechanical contacts have reached the required separation the electronic circuit breaker is turned off. Current is then diverted into the parallel MOSAs within each module, clamping the voltage rise across the devices (see Figure 5.17d).

Table 5.3: Technical Specification of ABB Proactive Hybrid Circuit Breaker [26]

	Value		Notes
Nominal Voltage	320	kV	
Maximum rated voltage	480	kV	1.5pu nominal voltage
Nominal current	2	kA	
Maximum rated current	9	kA	16kA feasible when next devices (BiGT) become available
Load commutation switch	-	-	3x3 matrix of 4.5kV IGBTs
Main breaker (electronic)	-	-	Constructed from 80kV cells. Each contains 20 series connected IGBTs, rated at 4.5kV
Ultra-fast disconnector speed	2ms		SF_6 insulated

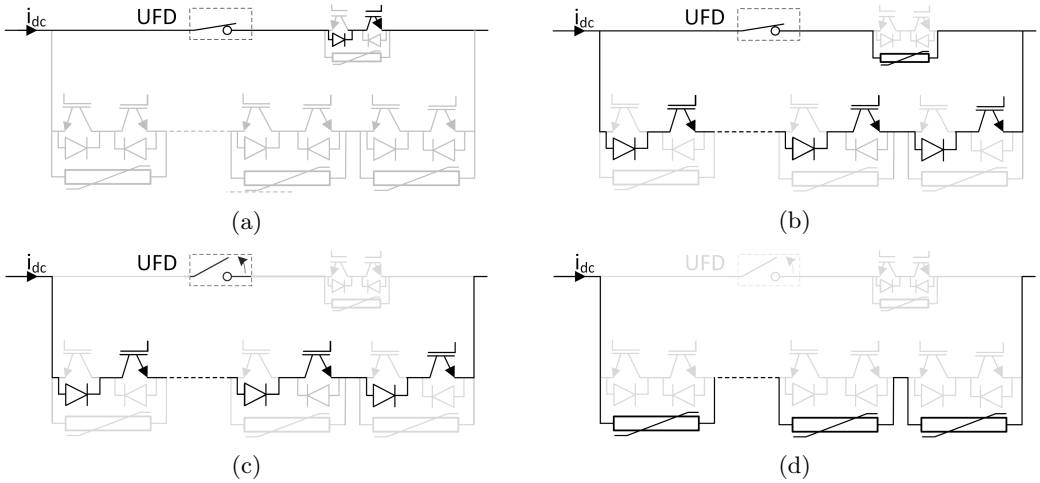


Figure 5.17: Hybrid circuit breaker operation

5.6.2 Alstom Hybrid Circuit Breaker Operation

The alternative hybrid circuit breaker was proposed in [27]. Figure 5.18 shows a diagram of the breaker at different stages of operation. Within the main branch a mechanical and semiconductor auxiliary switch are used in the same manner as the proactive hybrid topology. Current is diverted from the main branch into several additional, thyristor controlled, branches termed timing and arming branches. The purpose of the timing branches are to delay the voltage rise across the primary branch, whilst the UFD is moving and the auxiliary switch is supporting voltage. Technical specifications are given in Table 5.4. The commutation branches are constructed from Thyristors rather than IGBTs, which is possible as they do not require turn-off capability. The breaker has been extensively evaluated in partnership with RTE, the French transmission system operator, as part of the Twenties project. Testing included long

duration over-current (one minute), short duration current pulses and interruption of 7500A. The system was tested at 160kV peak using a synthetic circuit to generate the fault currents required.

Table 5.4: Technical Specification of Alstom Hybrid Circuit Breaker [27]

	Value		Notes
Nominal Voltage	120	kV	
Maximum rated voltage	180	kV	1.5pu nominal voltage
Nominal current	1500	A	3000A overload capability for 1 minute
Maximum rated current	7500	A	
Main breaker (electronic)	-	-	Constructed from pulse power thyristors. Quantity not stated
Ultra-fast disconnector speed	1.7ms	-	Dielectric strength >650kV

During normal operation current flows through the ultra-fast disconnector UFD and the auxiliary switch (see Figure 5.18a). When the breaker is tripped the auxiliary switch is turned off and voltage rises across the devices. Parallel MOSA will then clamp the voltage across the switch. At the same time thyristors in the first timing branch are fired. The voltage across the auxiliary switch will cause current to commutate from the primary branch into the first timing branch, see Figure 5.18b.

When current has fully commutated from the primary branch the UFD may begin to move, without causing arcing between the contacts. When voltage across the first timing branch capacitor reaches the MOSA clamping voltage then the secondary timing branch is triggered, see Figure 5.18c. Current in the first timing branch will attempt to reverse, causing the thyristors in that branch to turn-off. Current will pass through the capacitor of the secondary timing branch in the same way as the first, building up voltage until it meets the MOSA clamping voltage (Figure 5.18d).

When the UFD has reached the required displacement the third branch of thyristors may be fired. In doing so, the current within the timing branch attempts to reverse, turning off the thyristors in the timing branch. Voltage will build in the third branch according to the capacitor value causing current to commutate into the MOSA once the clamping voltage is met, as shown in Figure 5.18f.

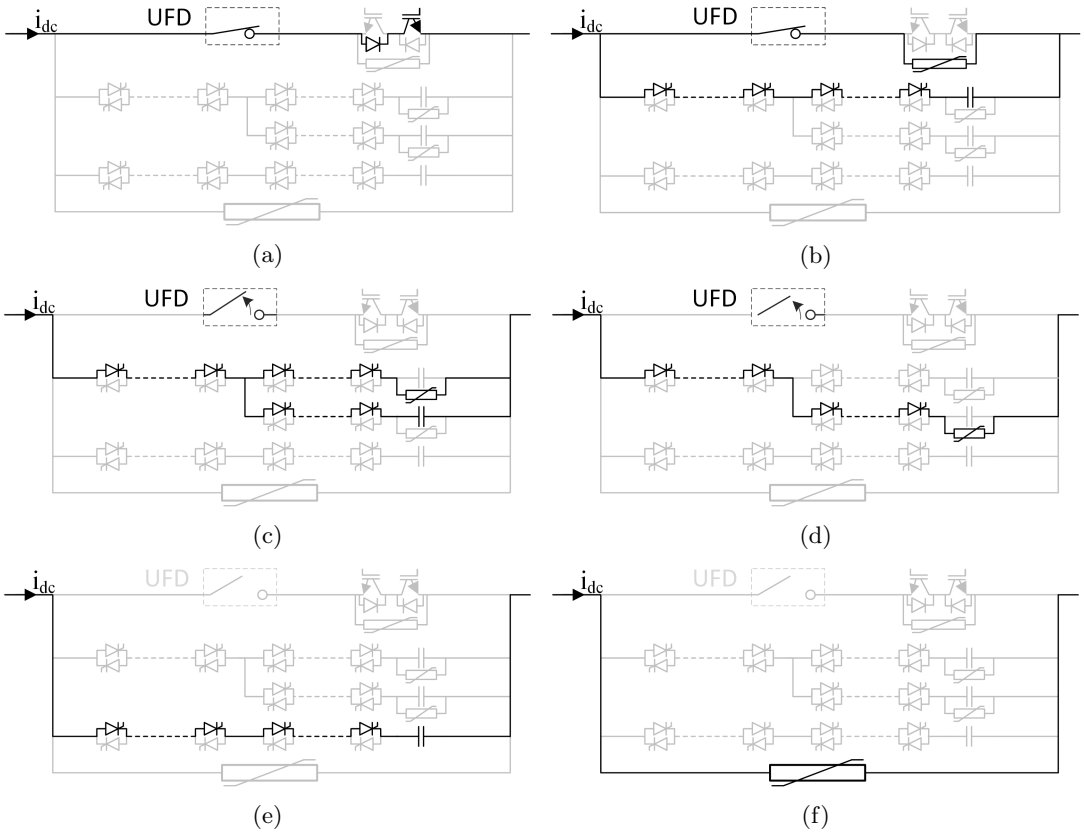


Figure 5.18: Alstom Hybrid Circuit Breaker Operation

5.7 Conclusion

Within this chapter the principles of dc circuit breakers have been reviewed. One of the principle differences from ac systems is that the circuit breaker must generate a counter-voltage which exceeds that of the system. In low voltage systems, where the required blocking voltage of the circuit breaker is low and the breaker isn't required to operate particularly fast, simple devices can perform adequately. In high voltage applications it becomes more difficult to create the required counter-voltage, particularly in the time-frame required.

The design principles in creating counter-voltages based on arcing within a traditional ac breaker have been explored, based on medium voltage systems such as railway traction. Circuit breakers designed for this purpose tend to be physically large, with a high weight and operate slowly, making them unsuitable for offshore HVDC applications. Literature covering the state-of-the-art circuit breakers topologies has shown that there are three candidates for HVDC applications: resonant, both passive and active current injection; electronic and hybrid. Hybrid circuit breakers have received the most attention within the HVDC community in the past five years, with many studies of large off-shore networks assuming their use. They have a clear

advantage over the electronic circuit breakers in terms of reduced power dissipation. However, capital costs are likely to be higher than an electronic solution, as they intrinsically contain an electronic circuit breaker internally.

Resonant circuit breakers are likely to have a lower cost than electronic and hybrid alternatives as the semiconductor count is much lower. Passive resonance is most likely to continue to be used within MRTB applications, as arc voltage build-up time can be too slow for use as a circuit breaker. However, active-resonant type has been demonstrated clear clear faults at both high-voltage and high-current. Peak current capability is likely to remain somewhat higher than both electronic and hybrid alternatives, as the mechanical topology has no semiconductor components in the main path, also helping to keep losses and purchase costs lost. Practical implementation can pose challenges. For instance pre-charging the capacitor that floats at pole voltage from a low voltage source.

Electronic circuit breakers offer extremely fast operation time when compared to the two main alternatives. This provides two benefits: primarily, the faulted area of the network is segregated from the healthy area faster, enabling improved ride-though; secondly, the peak current is lower, reducing stress and therefore cost. Due to steady-state losses, the life-time costs of the electronic circuit breaker make it unattractive presently.

At the time of writing, there are no commercially available products from manufacturers. Without cost information it is impossible to perform a fair evaluation between the three technology types to give an optimum candidate. Although electronic circuit breakers have generally been ruled out withing the literature, as it is assumed their losses would make them unattractive to transmission system operators, further studies are required to find the relative costs of reinforcing the network to withstand the lower speed of the alternatives. As has been shown in Chapter 4 parameter variation can be used to manipulate the characteristics of the network and thus the requirements of the breaker. In Chapter 7 simulations are performed to analyse system performance for different circuit breaker technology types. The choice of circuit breaker may then determined by the overall system performance requirements and cost evaluation of the improved performance gained by faster breakers.

Chapter 6

DC Breaker Stress Analysis

6.1 Introduction

The complexity of dc breakers is a product of the high current, voltage and speed requirements for HVDC applications. Maximum current stress is particularly a problem for topologies which utilise power electronics in the main path [28, 84, 27]. The energy dissipated within the breaker is also a design consideration as it influences capital cost and volume, which is of particular importance for offshore applications [85]. Reducing requirements in these areas assists in minimising the overall cost of the breaker.

HVDC circuit breaker designs have commonly included additional series inductance to reduce the rate of rise of current during the initial transient period after a fault occurs, minimising the peak current stress that the circuit breaker must endure [28, 86]. In chapter 3 the impact of dc inductance on fault current was demonstrated. The maximum current through the breaker could be significantly reduced by including additional inductance, provided the circuit breaker opened within a short period (up to approximately 20ms). However, determining the optimum amount of inductance to add has not been addressed within the literature up to this point. The decrease in fault current must be traded-off against the possible increase in energy that must be dissipated within the circuit breaker (requiring more MOSAs). This concept of increased energy is alluded to in [87] where the energy was approximated at $^1/_2LI^2$. However, within this chapter it is demonstrated that the energy to be dissipated by the circuit breaker is a more complex function of system parameters.

In this chapter the impact of additional dc inductance on peak circuit breaker current and energy dissipation is investigated. In Section 6.2 an 800kV MMC two-terminal test system is introduced and specified, which is used to observe the influence of additional dc inductance on

circuit breaker current and energy dissipation stress through parametric simulations. In Section 6.3 a simplified model is described and used to determine the expected peak current and energy dissipation within a circuit breaker, based on the system parameters. These estimations are then validated against results obtained from the test system described in Section 6.2. The limitations of the analysis are described and demonstrated with simulation results in Section 6.4.

6.2 Test System and Empirical Results

To evaluate the impact of having additional dc inductance on the peak current the circuit breaker must withstand, and the energy that it must dissipate, a test system is used. Analysis is performed for pole-to-pole faults at interface between the converter and cable/OHL, where there is minimum impedance between the fault and voltage source, as current stress is largest in this case.

Short circuit faults isolate the converter from all other areas on the network. Therefore, when analysing the impact of the fault on a single converter it is not necessary to model a large multi-terminal network. In the simulation studies performed in this chapter a two terminal system is used, giving the ability to set pre-fault power flow conditions which, as will be shown, influences the stress to the circuit breaker. With the minimum number of terminals required (two) the model complexity is reduced and simulation speed increased (when compared to a large multi-terminal network).

The two terminal system used to perform simulations is shown in Figure 6.1. Both ac networks are identical and represented by ideal three-phase voltage sources in series with an inductance to represent network strength. Circuit parameters for the test system used are given in Table 6.1. The average value cell model of the HB-MMC is used as it allows increased simulation speed over switched models whilst still providing the ability to set initial power flow (unlike the diode model, see Chapter 2). DC breakers are located adjacent to the converter station, with one per pole, and are triggered in pairs. The short time period in which electronic circuit breakers operate means that the effect of additional inductance has a marginal effect on breaking current. These are therefore neglected.

In the time frame that mechanical breakers operate, 10ms at fastest, the initial transient has broadly passed, with current approaching steady-state, where inductance has little to no effect. However, hybrid circuit breakers typically operate within the first 5ms, where current is still rapidly rising. It is in this region that changes to dc inductance have greatest effect. For

the analysis performed here it is assumed that the circuit breakers are assumed to be of hybrid type, with an operating speed of 5ms in order to observe the variation as much as possible. Each breaker is modelled as an ideal switch in parallel with an MOSA to clamp the voltage rise and dissipate the energy resulting from breaking current. The MOSA clamping voltage is set to 1.5pu of nominal cable voltage ($V_{dc}/2$).

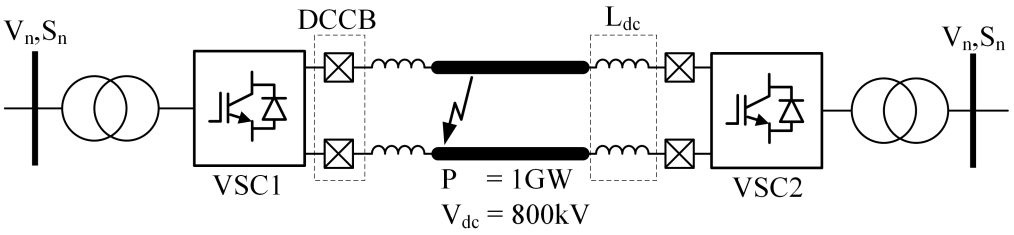


Figure 6.1: System model. DC breakers at each converter are assumed to be in the same location and, as such, are triggered in pairs

Table 6.1: System Parameters

	Parameter	Value	Notes
S_n	Network strength	10GVA	Short Circuit Capacity (SCC)
V_n	Network voltage	400kV	Nominal, line-to-line RMS
V_c	Converter voltage	392kV	Nominal, line-to-line RMS
S_c	Rated power of converter	1000MW	PF = 0.95
V_{dc}	Nominal dc voltage	800kV	Pole-to-pole
X_{TRM}	Transformer leakage	0.2pu	Per unit
L_{arm}	Arm inductance	0.05pu	46.5mH, referred to converter side
V_{cb}	DCCB Clamping voltage	600kV	1.5pu pole voltage
L'_n	Network inductance	49mH	Referred to converter side
L'_{trm}	Transformer inductance	97mH	Referred to converter side
T_{cb}	DCCB operation speed	5ms	Time after fault inception
L_{ac}	Effective ac inductance	192.5mH	$L'_n + L'_{trm} + L_{arm}$

6.2.1 Circuit Breaker Measurements

Measurements in each simulation case are taken within the circuit breaker, for both current and energy (Figure 6.2). As the system is symmetrical, and pole-to-pole faults are analysed, measurements are taken for a single breaker.

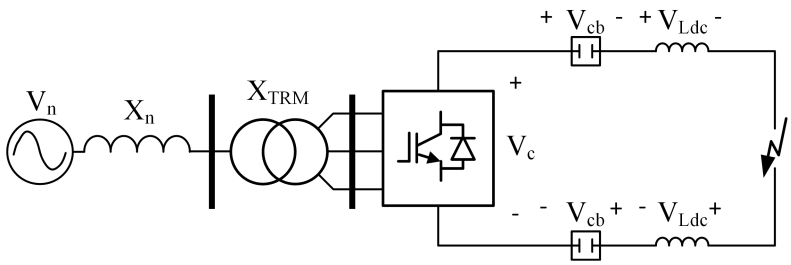


Figure 6.2: System measurements taken during simulation

6.2.2 Typical Results – Impact of DC Inductance

To demonstrate the effect of additional dc inductance (L_{dc}), Figure 6.3 shows simulation results for three different values of L_{dc}. So that the natural response of the system can be observed, circuit breakers are not operated. Over the one second time period following the fault, the steady-state current in all three cases settles to approximately 20kA. Over the shorter time period, in the region of 30ms, the peak current magnitude may be significantly reduced by additional dc inductance. Depending on technology type, breakers are likely to operate within the 2ms to 10ms time frame [28, 79]. Therefore, additional dc inductance can help to significantly reduce peak current stress within the circuit breaker as Figure 6.3 demonstrates.

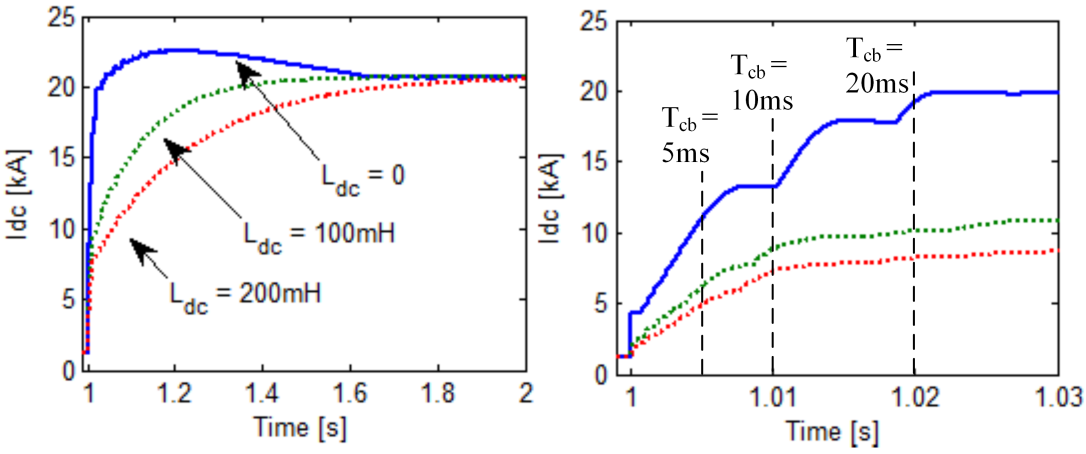


Figure 6.3: DC current waveforms from typical pole-to-pole fault. Time periods given are from fault inception. Detection and relaying time is not considered. Simulated results performed using Matlab Simulink.

6.2.3 Pre-fault Current

Current flowing into the link prior to the fault occurring can increase the maximum current stress through the breaker. Therefore, the current through, and energy dissipated within, the breaker depends on the system initial conditions as well as the system parameters. To evaluate

the impact of initial conditions on the stress placed on the circuit breaker, simulation cases are performed with three pre-fault power flow conditions, as shown in Table 6.2.

Table 6.2: Initial Conditions

Pre-fault Current	I_0	Notes
Positive	+1.25kA	1GW from AC network to DC side
Zero	0	No power flow
Negative	-1.25kA	1GW from DC side to AC network

6.2.4 Effect of L_{dc} on Peak Current

Figure 6.4 shows simulation results for peak dc current with variable L_{dc}. The results show that peak dc current is reduced by approximately 60% with maximum L_{dc}. Where pre-fault current is positive peak current exceeds the zero initial current case by approximately 1.25kA (equivalent to the pre-fault current I_0) implying that maximum current in the positive case is the summation of the fault contribution and the pre-fault current. In the reverse case, where pre-fault current is negative, peak dc current is reduced by only 500A when compared to the zero initial current case. This indicates peak dc current for a negative pre-fault current is not a simple superposition of a current injection and the pre-fault condition.

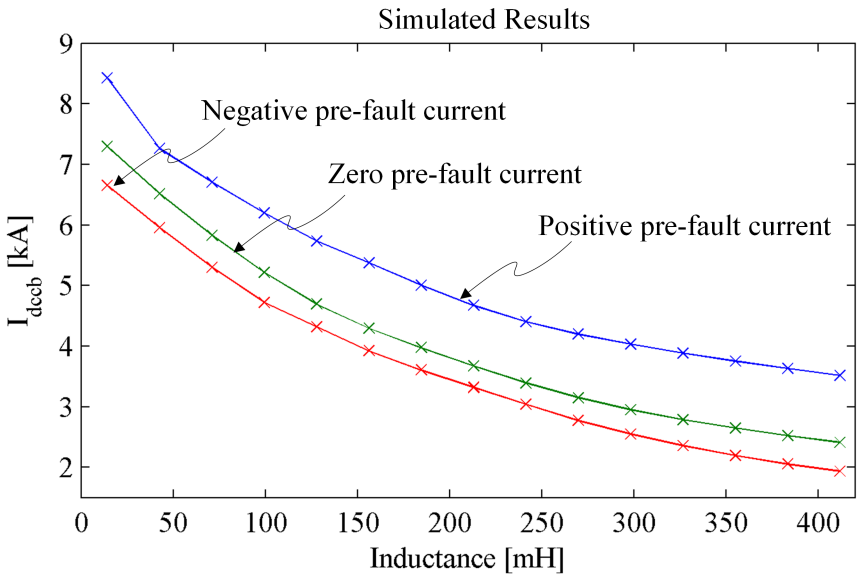


Figure 6.4: Simulation results showing peak dc current verses L_{dc} for the three initial power flow conditions. T_{cb}=5ms. Detection and relaying time is not considered. Simulated results performed using Matlab Simulink.

6.2.5 Effect of L_{dc} on Energy Dissipation

Figure 6.5 shows simulation results where the effect of L_{dc} on circuit breaker energy dissipation is measured. Simulations are performed for the range of inductances, for each of the three pre-fault current conditions given in Table 6.2. Where pre-fault current is positive (into the dc link) energy dissipation is highest. This is logical as the peak current is largest, as was shown in Figure 6.4. Energy dissipation does not continue to increase with L_{dc} indefinitely – for each of the three pre-fault conditions maximum energy dissipation occurs in the region between approximately 140mH and 220mH. Note that the effective ac inductance during the initial current rise is L_{ac} (192.5mH), see Table 6.1.

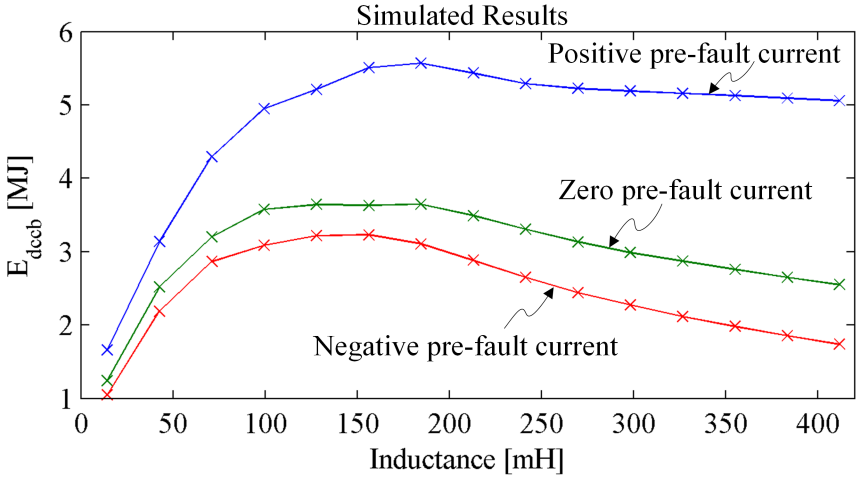


Figure 6.5: Simulation results showing circuit breaker energy dissipation verses L_{dc} for the three initial power flow conditions. T_{cb}=5ms. Detection and relaying time is not considered. Simulated results performed using Matlab Simulink.

6.3 Theoretical Analysis

Optimising the value of inductance to reduce peak current, and to trade this off against energy dissipation, requires large numbers of simulation studies to be performed using an empirical approach can be time consuming. Parametric studies produce trends but do not provide an understanding of the underlying, fundamental influences which determine dc fault behaviour. A simplified mathematical analysis of the converter during dc faults provides a clearer understanding of the primary and secondary effects of parameter choices, which is not possible from empirical studies alone. Such a tool then allows a reasonable ranges of component values to be selected before then performing in depth parametric studies. In this section a mathematical approach is used to determine the expected current and energy dissipation that the dc breaker

is required to withstand, for a given set of system parameters.

The complexity of the circuit means a mathematical analysis that takes into account all branches is prohibitive. (Circuit simulators, such as SPICE and Matlab Simulink are more suited for this purpose.) By modelling the converter and ac network in a simplified manner the circuit complexity may be reduced, making an analytical approach feasible. To simplify the model as much as possible assumptions given in Table 6.3 are used, which are related to the equivalent circuit shown in Figure 6.6. Assumption 1 simplifies the cells by removing the IGBTs. Current will initially build up in the two arms with the largest line-to-line voltage. If the pre-fault current is small relative to the fault contribution, initial current flowing in each of the arms may be neglected (assumption 2) and the circuit may then be simplified into a two phase, two-arm circuit from the three phase, six-arm circuit. This assumption is only valid over short time periods – such as the first commutation period. Over longer time periods current will begin to naturally commutate between the arms, significantly increasing the complexity of the analysis. Assumption 3 implies that as the circuit breaker opens in a short period of time the remaining arms only contribute a small amount of current – they would naturally come into conduction later in the cycle, after the breaker has opened. Therefore it is only necessary to study the contribution from the first two arms and the remaining may be neglected.

Table 6.3: Assumptions Used

	Assumption	Details
1	Converter Blocking	The converter is blocked immediately after the fault occurs
2	Fault Current Dominates	The increase in current is large when compared to the pre-fault current within the arms
3	T_{cb} is small	The circuit breaker operation speed is small when compared to an ac cycle

For a fault is placed at the converter terminals the equivalent circuit is given by Figure 6.6a. The assumptions discussed allow the circuit to be reduced significantly. Current builds up in the two phases with the largest line-to-line voltage at point-on-wave when the fault occurs (through the upper arms for positive current and lower arm for negative current). The remaining four arms are neglected and assumed open circuit. Diodes in series with the cell capacitors are reverse biased and are also neglected. To further simplify analysis the network and transformer impedances and ac source are referred to the converter side. The equivalent impedances are given in Table 6.1. The remaining circuit is as shown in Figure 6.6b.

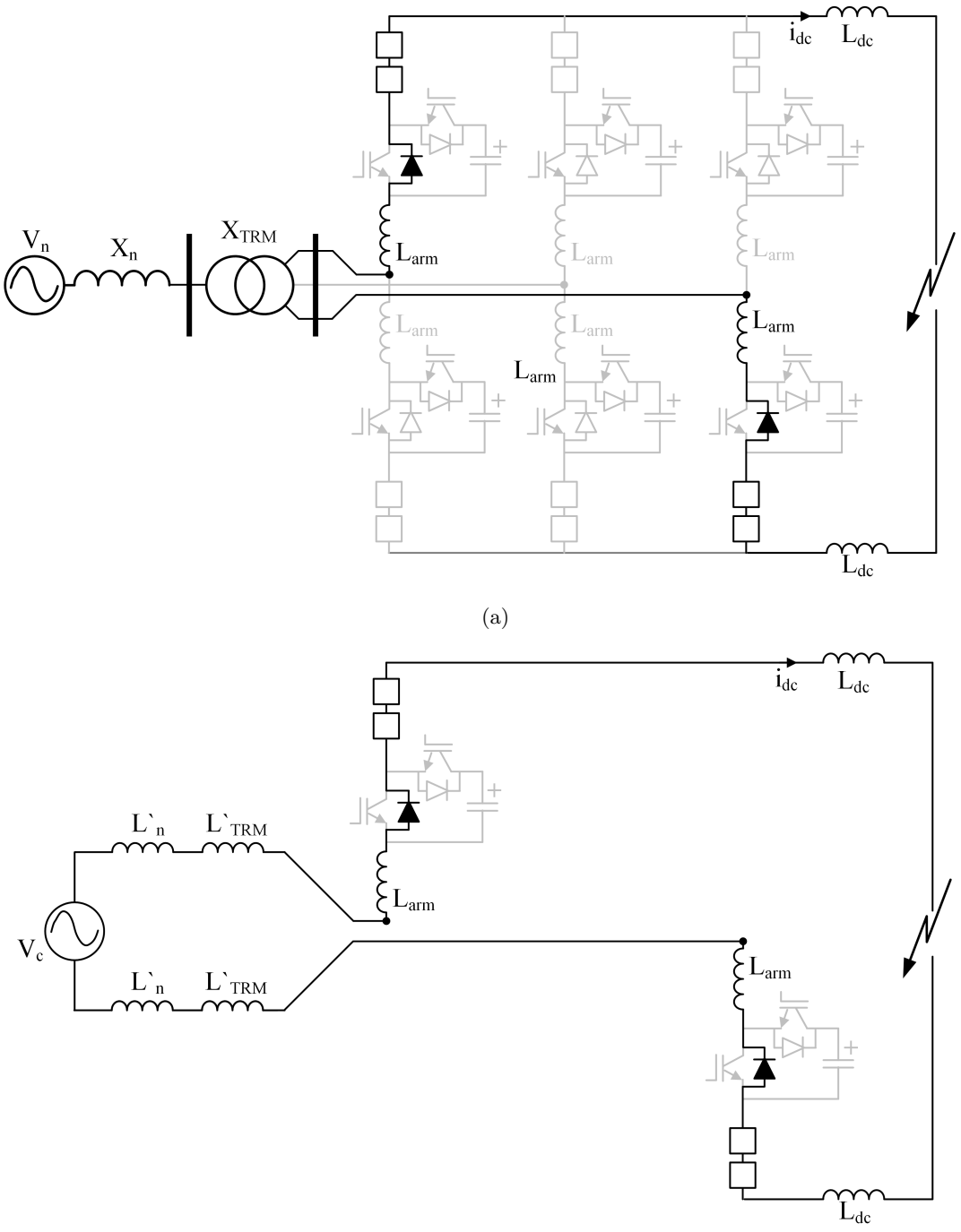


Figure 6.6: Equivalent circuit under fault. (a) conduction path of a single phase. (b) equivalent circuit with redundant arms removed

6.3.1 Estimating Peak DC Current

With the converter blocked current flows through the free-wheeling diodes (and bypass thyristors – not shown), as shown in Figure 6.6b. Taking KVL around the current loop the contribution of current from the fault may then be approximated by (6.1), where T_{cb} is the circuit breaker opening time and the line-to-line voltage is assumed to be at its peak.

$$\Delta I_{\mathrm{dc}} = \frac{\sqrt{2}V_{\mathrm{n}}}{2\left(L_{\mathrm{ac}} + L_{\mathrm{dc}}\right)} \cdot T_{\mathrm{cb}} \tag{6.1}$$

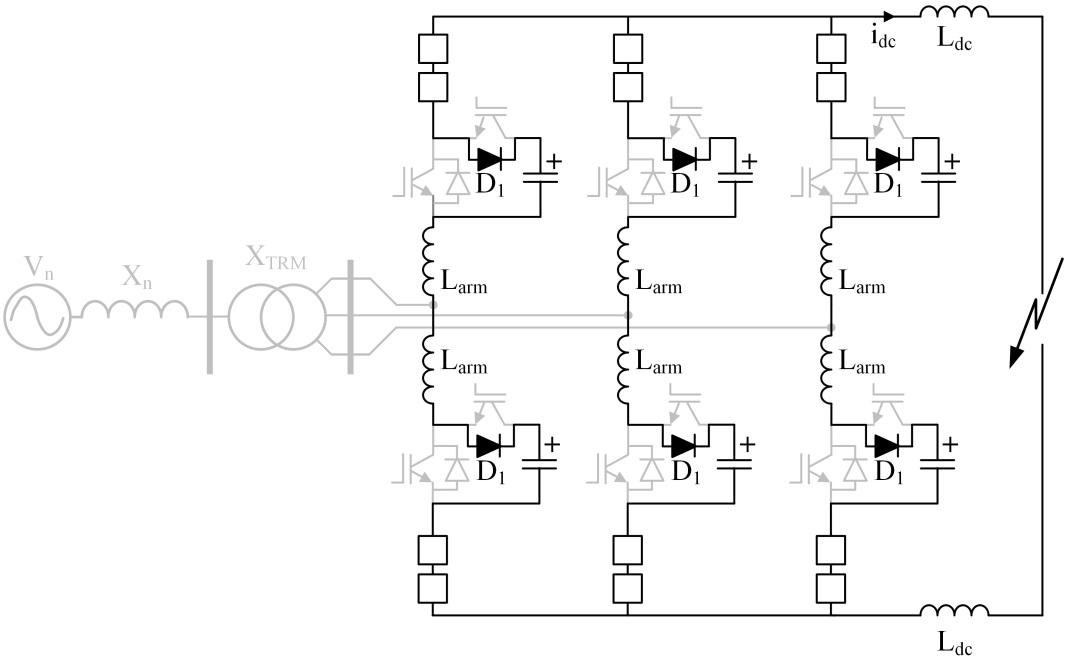
6.3.1.0.1 Zero pre-fault current flow If pre-fault current is zero then peak dc current is the same as the contribution from the fault. The peak current can, therefore, be approximated by (6.2).

$$\hat{I}_{dc} = \Delta I_{\mathrm{dc}} \tag{6.2}$$

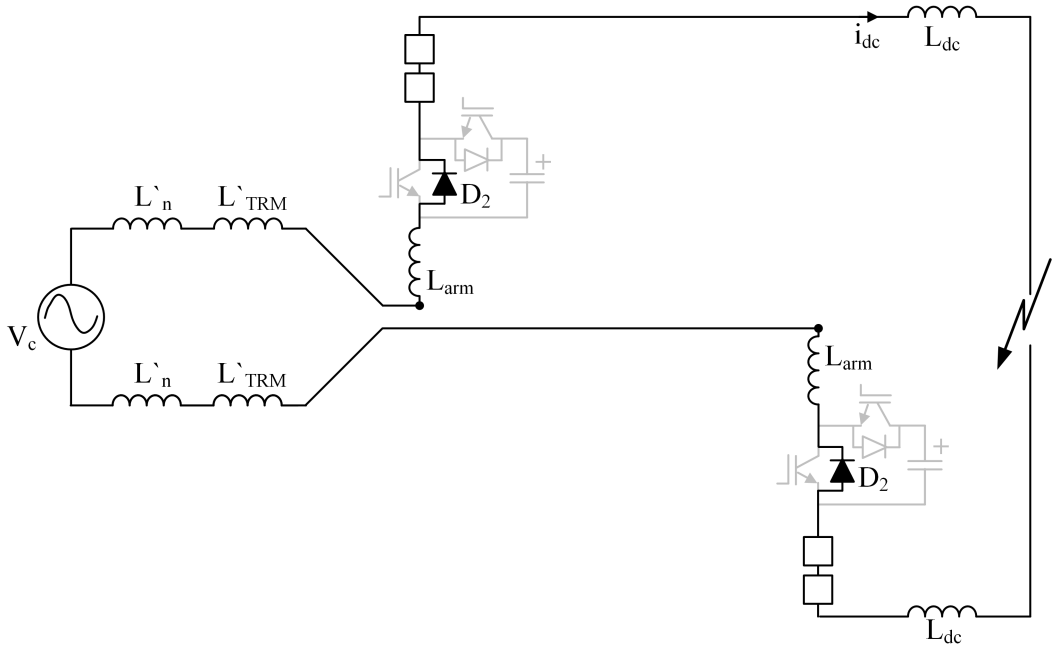
6.3.1.0.2 Positive pre-fault current Where current flow is initially positive, i.e. from the ac side to the dc side, the pre-fault and fault currents are additive, generating a larger peak current. The peak current through the circuit breaker may be approximated by (6.3), where I_0 is the pre-fault current flow in the dc line.

$$\hat{I}_{\mathrm{dc}} = \Delta I_{\mathrm{dc}} + I_0 \tag{6.3}$$

6.3.1.0.3 Negative pre-fault current flow Estimating peak current when pre-fault current is negative is more complex. With the converter blocked current passes through cell capacitors via diode D_1 in each cell (see Figure 6.7a) and no voltage impulse is applied to the dc side. Current must increase through zero before diodes D_1 can come into conduction and force an increase in current. To estimate the peak current for this case, first the time for current to increase to zero must be found.



(a)



(b)

Figure 6.7: Equivilent circuit for negative pre-fault current: (a) whilst dc current is negative. Note that positive current flow is shown in this diagram. In the case given here dc current is negative, i.e. in the reverse direction. (b) when current passes through zero and becomes positive.

While current is negative it must flow through the capacitors in an arm, as IGBTs are gated off. With N cells per arm a counter-voltage of V_{dc} is imposed by each arm (assuming that the capacitor voltages remain constant at $\frac{V_{dc}}{N}$). Current must flow through at least two arms, imposing a total counter-voltage of $2V_{dc}$. This voltage is applied across the two dc inductors (circuit breakers are still closed at this point), which forces current back to zero in a short space of time (see Figure 6.8). The time for the dc current to reach zero can be approximated by (6.4).

$$T_0 = \frac{L_{\mathrm{dc}}}{V_{\mathrm{dc}}} I_0 \tag{6.4}$$

Upon current passing through zero, diode D_1 becomes reverse biased and D_2 comes into conduction (Figure 6.7b). Current is then forced by the ac voltage (as in the zero and positive pre-fault current cases). However, the time period over which this takes place is now reduced. Peak current stress, when pre-fault current flow is negative, can be approximated by (6.5). Estimates for the peak current for the three pre-fault current flow conditions can be summarised by Table 6.4.

$$\hat{I}_{dc} = \frac{\sqrt{2} V_{\mathrm{LL}}}{2\left(L_{\mathrm{ac}} + L_{\mathrm{dc}}\right)} \cdot \left(T_{\mathrm{cb}} - T_0\right) \tag{6.5}$$

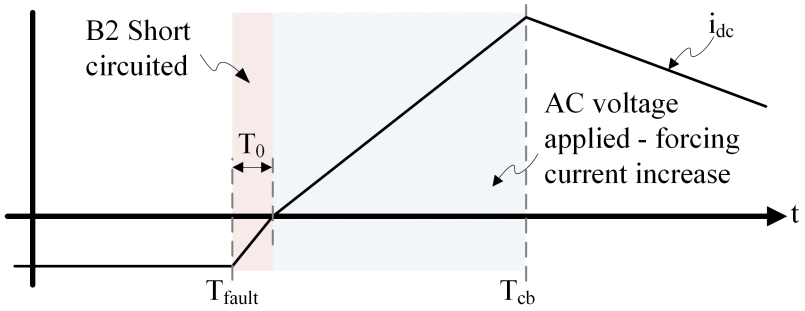


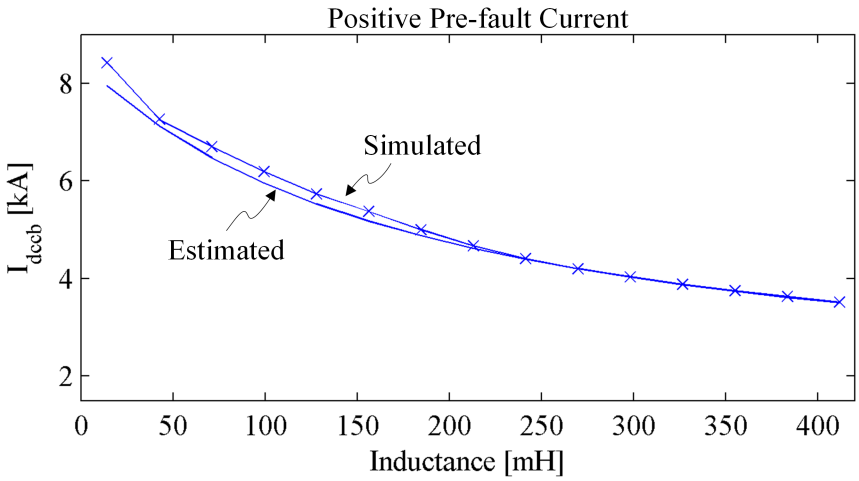
Figure 6.8: DC current being forced through zero, before being increased by ac source

Table 6.4: Summary of Peak dc Current Estimations

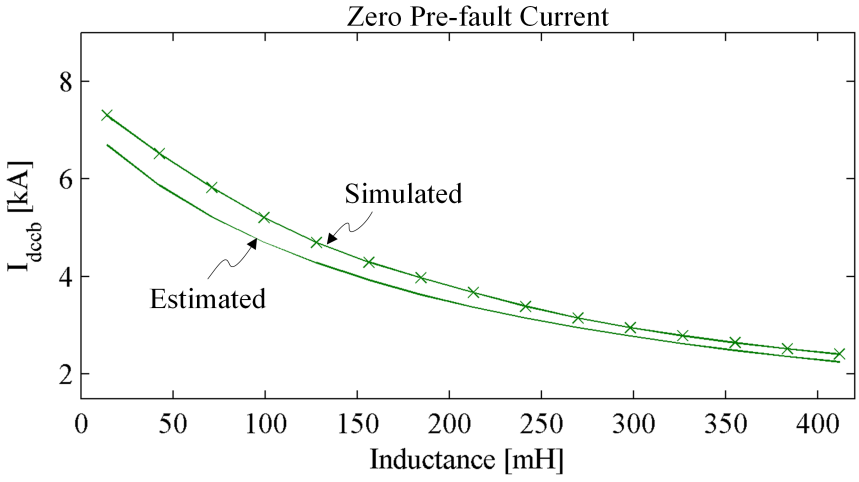
Pre-fault current (I_0)	Approximated peak dc current ($\hat{I}_{\mathrm{dc}}$)
> 0	$\frac{\sqrt{2} V_{\mathrm{B2}}}{2\left(L_{\mathrm{ac}} + L_{\mathrm{dc}}\right)} \cdot T_{\mathrm{cb}} + I_0$
$= 0$	$\frac{\sqrt{2} V_{\mathrm{B2}}}{2\left(L_{\mathrm{ac}} + L_{\mathrm{dc}}\right)} \cdot T_{\mathrm{cb}}$
< 0	$\frac{\sqrt{2} V_{\mathrm{B2}}}{2\left(L_{\mathrm{ac}} + L_{\mathrm{dc}}\right)} \cdot \left(T_{\mathrm{cb}} - \frac{L_{\mathrm{dc}}}{V_{\mathrm{dc}}} I_0\right)$

6.3.1.1 Validation

To verify the predictions of peak current through the circuit breaker, simulation studies are performed. Predictions are made for the three power flow conditions, using the three calculation methods provided in Table 6.4. Converter and system parameters are assumed constant (as given in Table 6.1) and the additional dc inductance is varied between 10mH and 410mH. Peak dc current is measured 5ms after the fault is appplied (when the circuit breaker is opened. Results are shown in Figure 6.9. The estimation of peak current correlates well with the simulation results for the three pre-fault current flow cases, with a maximum error of approximately 5%.



(a)



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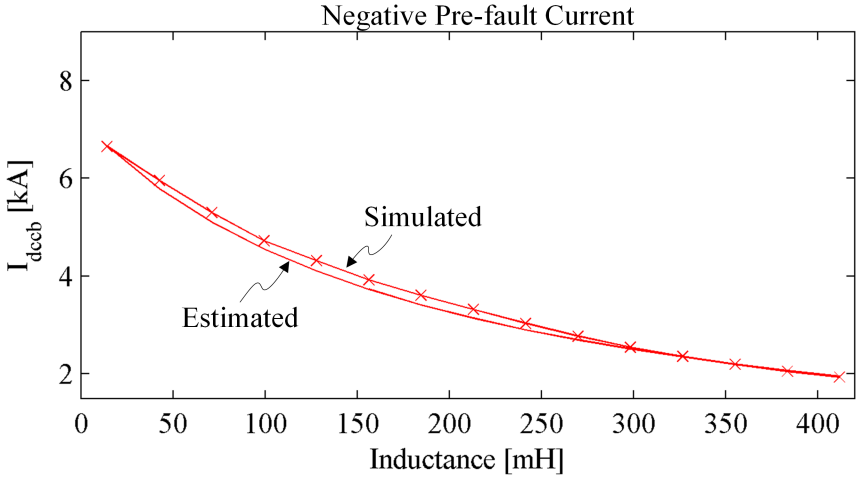


(c)

Figure 6.9: Circuit breaker peak current validation: (a) positive pre-fault current, (b) zero pre-fault current and (c) negative pre-fault current. T_{cb}=5ms. Detection is not considered. Simulated results performed using Matlab Simulink.

6.3.2 Estimating Energy Dissipation

When dc circuit breakers are used to clear faults they must absorb the stored energy within the system. As discussed in Chapter 5, dissipating the amount of energy associated with HVDC systems within the circuit breaker is a non-trivial task and directly reflects the complexity of the circuit breaker.

Energy dissipation within the circuit breaker can be estimated by (6.6), where T_0 is the time duration for which the circuit breaker is dissipating energy (the time for dc current to fall from its peak value to zero, see Figure 6.10), $\overline{I_{dc}}$ is the average dc current given by $\hat{I}_{dc}/2$ (taken from the estimate predicted in Table 6.4) and V_{cb} is the circuit breaker clamping voltage.

$$E_{cb} = \overline{I_{dc}} \cdot V_{cb} \cdot T_0 \tag{6.6}$$

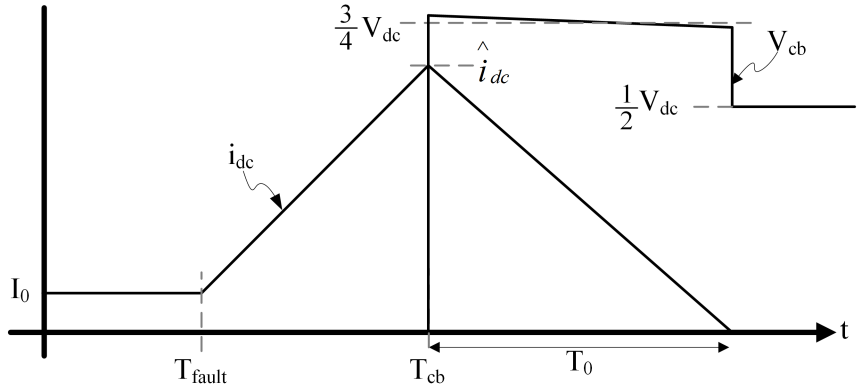


Figure 6.10: Idealised circuit breaker current and voltage waveforms

The time for current to reach zero (T_0) is determined by the circuit breaker counter-voltage, dc inductance and voltage present at the converter station terminals (V_c) (see Figure 6.11).

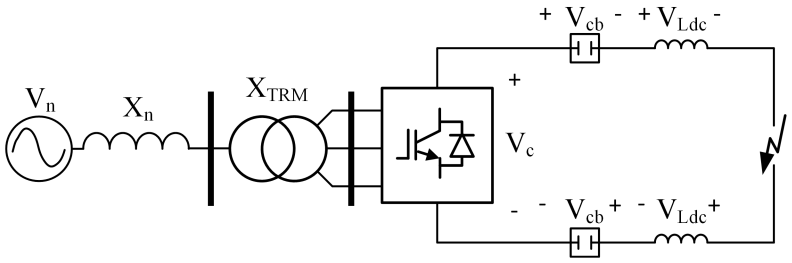


Figure 6.11: Converter under fault with circuit breakers open

During normal operation V_c is well regulated by the converter to V_{dc}. Whilst clearing the fault V_c is determined by circuit parameters rather than converter control. Figure 6.12 shows a simplified equivalent circuit of the system once the circuit breaker has opened. The MOSA

in each circuit breaker clamps at 1.5pu of nominal pole voltage ($\frac{1}{2}V_{\mathrm{dc}}$). The two act in series to produce a total counter voltage of $2V_{\mathrm{cb}}$, equal to $1.5V_{dc}$ (1200kV total, 600kV each). V_{ac} represents the ac line-to-line voltage and is assumed constant over the short time period. The central branch models the current path through the cell capacitors, which can conduct in some circumstances.

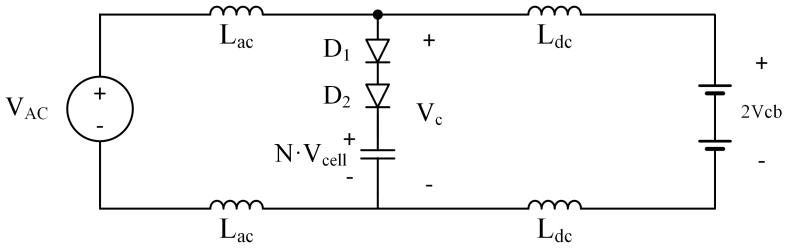


Figure 6.12: Approximate equivalent circuit showing cell clamping

When the circuit breakers opens a counter-voltage is generated on the dc side. V_c will depend on the ratio of $L_{dc} : L_{ac}$. Where $L_{dc} : L_{ac}$ is high the dc breaker must dissipate the stored energy from both L_{ac} and L_{dc}. In this case the central branch will not conduct and the approximate time for current to decay to zero is given by (6.7). V_{ac} depends on the point-on-wave at which the circuit breaker opens and is therefore variable.

$$T_0 = \frac{2(L_{dc} + L_{ac})}{2V_{cb} - V_{ac}} \cdot \hat{I_{dc}} \tag{6.7}$$

A low value of $L_{dc} : L_{ac}$ will result in current on the dc side decaying rapidly as there is little or no energy stored in L_{dc}. Energy from the ac side then cannot be absorbed by the dc breaker. AC current is forced to circulate through the arms whilst the energy stored in the ac side is transferred into the cell capacitors, causing the voltage to rise. Two current loops can form, one around the upper arms and one around the lower, each imposing a voltage of $N \cdot V_{\mathrm{cell}}$. The approximate time for i_{dc} to decay to zero can be estimated by (6.8). Table 6.5 summarises the formulae used to estimate the energy dissipation within the circuit breaker for the two conditions are possible: clamping and non-clamping action.

$$T_0 = \frac{2L_{dc}}{2V_{cb} - V_c} \cdot \hat{I_{dc}} \tag{6.8}$$

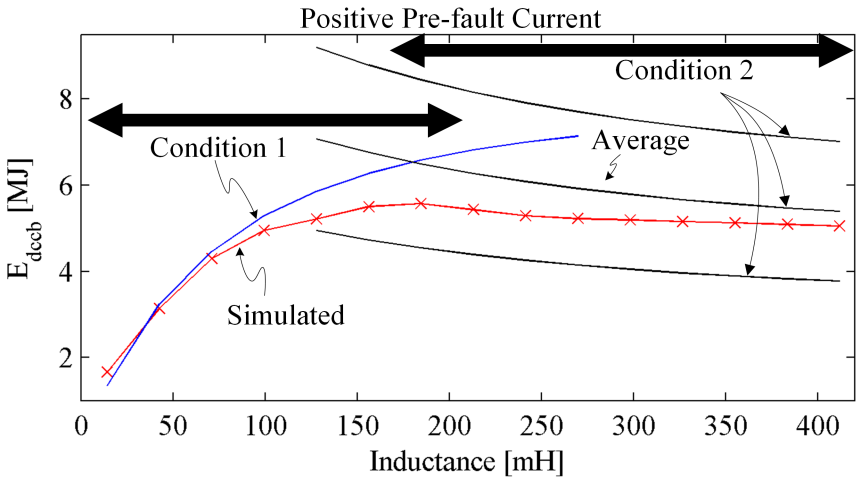
Table 6.5: Time to current zero summary

Condition	$L_{dc} : L_{ac}$	T_0	
1	Low	$\frac{2L_{dc}}{2V_{cb} - V_c} \cdot \hat{I_{dc}}$	(6.8)
2	High	$\frac{2(L_{dc} + L_{ac})}{2V_{cb} - V_{AC}} \cdot \hat{I_{dc}}$	(6.7)

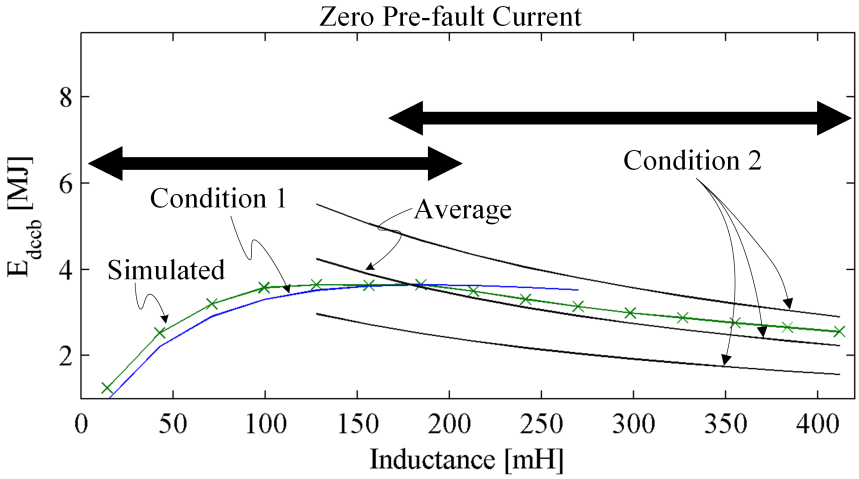
6.3.2.1 Validation

Figure 6.13 shows simulated and estimated energy dissipation measurements superimposed, for the three pre-fault power conditions. Simulated data points are the same as those from Figure 6.5. Estimates are formulated from equations found in Table 6.5. The appropriate value to use for V_{ac} (a value of which is required to calculat E_{dccb} in condition 2) depends on the instant at which the circuit breaker is opened – the point-on-wave. As this is unknown, the upper and lower bounds of V_{ac} are used, providing two curves. The upper corresponding to peak ac voltage; the lower to zero volts. The middle curve is the average of the two.

For higher values of L_{dc}, the average value of condition 2 correlates well with the simulated results. Where L_{dc} is smaller than L_{ac}, condition 1 correlates with the simulated results. The point at which the condition 1 curve crosses the average condition 2 curve corresponds to the maximum energy dissipation point. This point occurs when $L_{dc} \approx L_{ac}$ (192.5mH). Error is smallest for the largest and smallest values of L_{dc}. The largest error occurs during the transition between condition 1 and 2 (greatest in the positive pre-fault current case, where there is approximately a 20% overestimation in energy dissipated).



(a)



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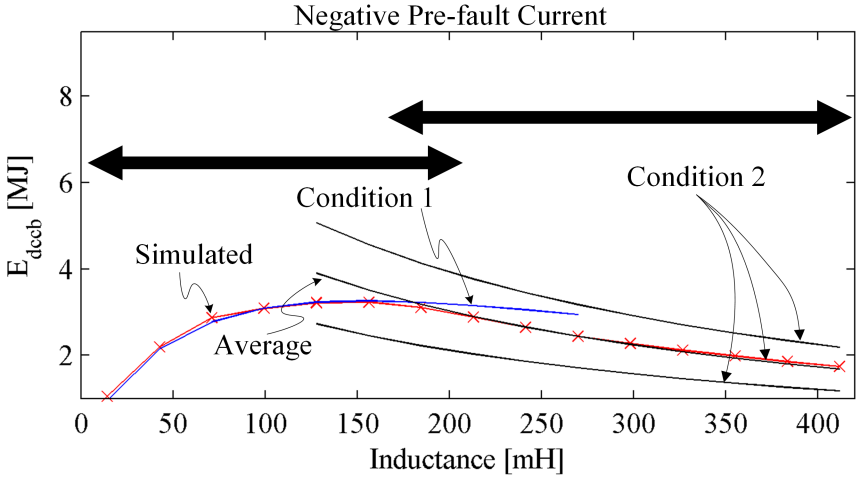

(c)

Figure 6.13: Circuit breaker energy dissipation: (a) positive pre-fault current, (b) zero pre-fault current and (c) negative pre-fault current. T_{cb}=5ms. Detection is not considered. Simulated results performed using Matlab Simulink.

6.4 Limitations of Tool

The analysis provided in this chapter hinges on the assumptions given in Table 6.3. The results presented so far have shown to provide adequate accuracy and thus the assumptions used appear valid. It is important, however, to demonstrate the limitations of the method used. If the circuit breaker operation spans more than a single commutation time period (one sixth of a line frequency cycle) then current begins to conduct in all three phases. The two phase, two arm simplification used for the converter is no longer valid and conduction paths through all six arms within the converter must be taken into account. The estimates used here are, therefore, no longer valid.

To demonstrate the limitations of the method the same analysis is performed with a slower circuit breaker (T_{cb}=10ms). Comparison of simulation results and estimates for peak current (Figure 6.14) and energy dissipation (Figure 6.15) are given. Error in peak current is much larger than in the 5ms case (40%). The error in estimated energy dissipation is greater still, at 100%. (As energy dissipation estimates utilise the estimate for peak current there is a compounding of errors, leading to a larger error overall.) The method provided here is, therefore, not applicable for systems which utilise slower circuit breakers (such as mechanical type). To increase the accuracy of the model the conduction paths through more than two legs must be accounted for.

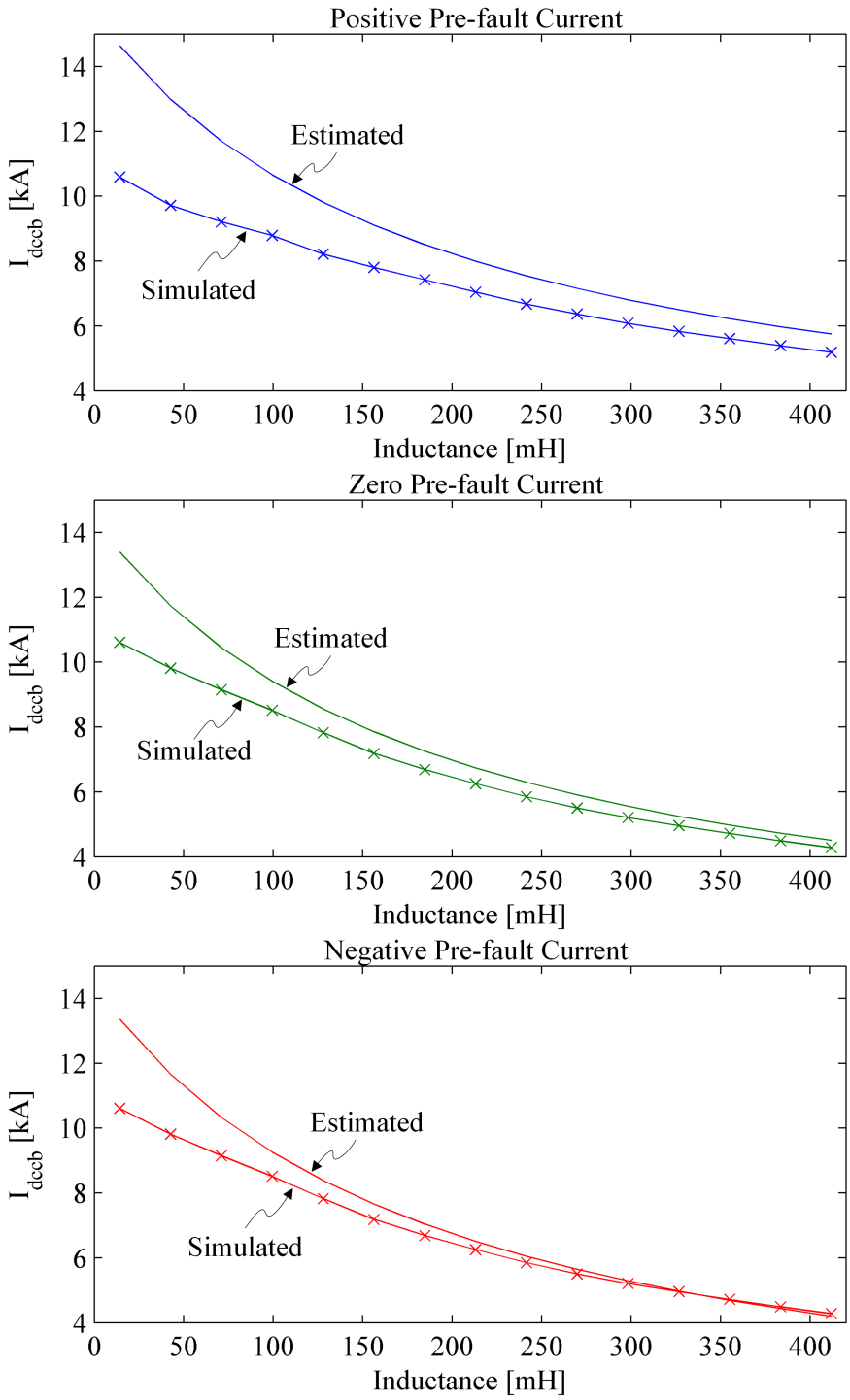

Figure 6.14: Circuit breaker peak current: (a) positive pre-fault current, (b) zero pre-fault current and (c) negative pre-fault current. T_{cb}=10ms. Detection is not considered. Simulated results performed using Matlab Simulink.

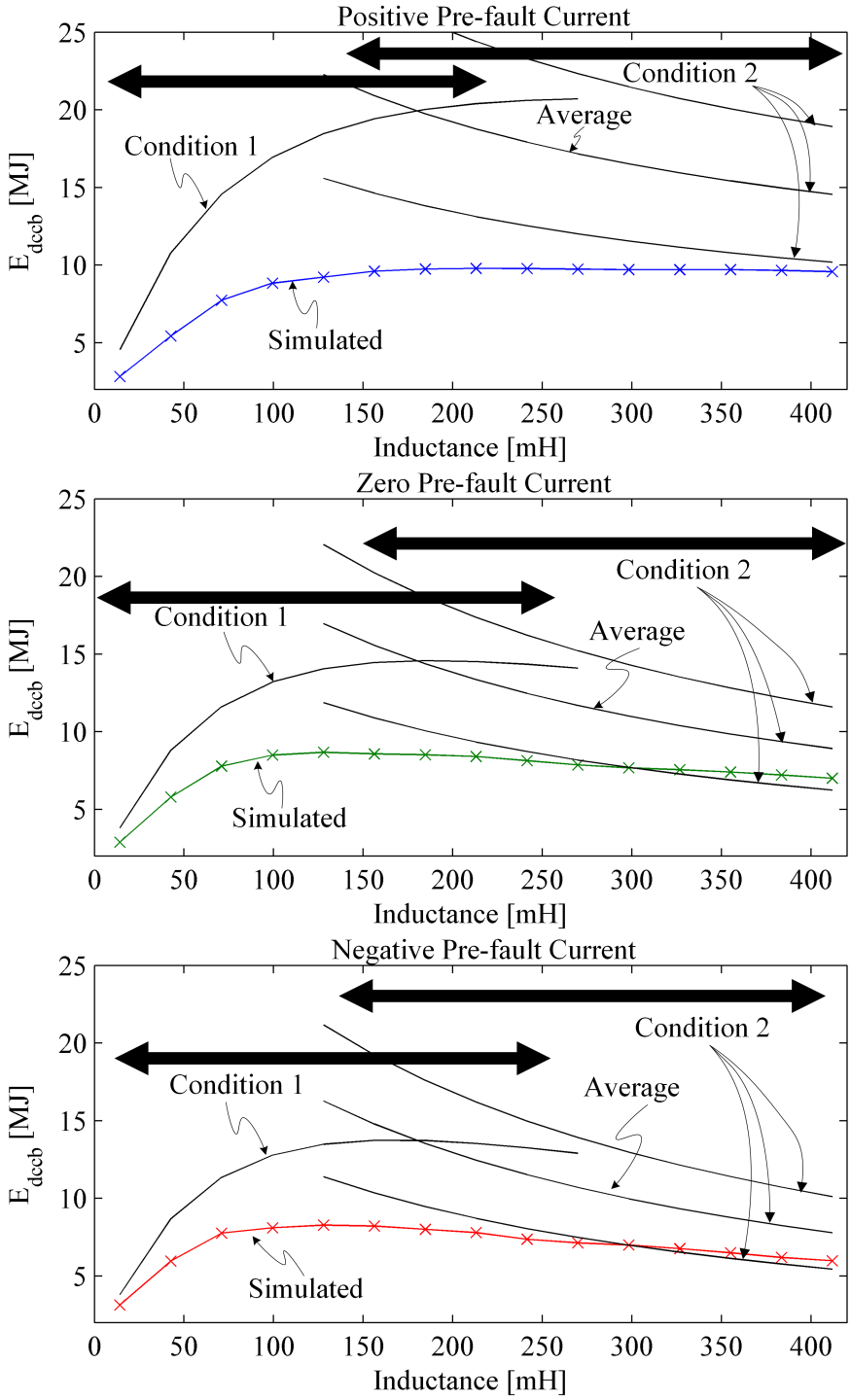

Figure 6.15: Circuit breaker energy dissipation: (a) positive pre-fault current, (b) zero pre-fault current and (c) negative pre-fault current. T_{cb}=10ms. Detection is not considered. Simulated results performed using Matlab Simulink.

6.5 Conclusion

Empirical simulation results have shown that additional dc inductance can be an effective tool for reducing the peak current stress in dc circuit breakers. As these inductors form part of the main conduction path, they must be designed to ensure low power loss. The requirement for high-current dc operation poses practical design challenges. The cost and scale of dc circuit breakers for high-voltage applications are closely related to their peak current capability. The reduction in peak current offered by dc inductors may therefore be sufficient to justify their inclusion.

Key performance indices of fault current rise and DCCB energy dissipation are dependent upon the transient response of the converter over a number of commutation cycles. Accurate figures for these quantities can only realistically be obtained through time-domain simulation which requires extensive parametric studies to identify trends and interactions resulting from component choice. The approximate mathematical analysis presented facilitates understanding of the underlying factors which relate parameter choice, peak current and circuit breaker energy.

The method of estimating circuit breaker peak current requirement has been shown to produce results that are accurate to within 10% of values obtained through simulation, when assuming very short circuit breaker opening time. The analysis has enabled estimation of circuit breaker energy dissipation. Maximum and minimum energy dissipation boundaries have been defined, according to converter parameters, allowing the required surge arrester capacity to be estimated. Estimated peak current and energy dissipated may then be used to optimise the breaker performance for a lowest cost solution, based on £/kA (relating to the peak current capability) and £/MJ (relating to the number of surge arrester columns required) data.

When considering a mechanical circuit breaker with 10ms opening time, the assumptions used to estimate peak current and energy dissipation become less valid when the additional dc inductance is small. Comparison of simulated and estimated results show that as the inductance increases, the error reduces. To further improve accuracy, the effect of commutation between the converter arms must also be considered. Although thorough analysis is required for individual system studies, the technique provides an indicative tool for estimation of the influence of dc inductance on peak current and energy dissipation. It is sufficient to enable initial assessment of the trade-off between additional capital cost, footprint and losses associated with the inclusion of additional dc inductance, and the cost associated with a higher performance circuit breaker, prior to performing detailed simulation studies.

Chapter 7

Multi-Terminal Protection Strategy

7.1 Introduction

Development of large scale, multi-terminal HVDC networks requires an adequate protection scheme. It must clear the large fault currents that occur within VSC based systems during dc faults and reconfigure the network appropriately. Blocking converters are one way of rapidly removing fault current from the converter and network [44][21]. These converters, however, do not provide a full solution to system protection; the faulted section of network must still be isolated from the healthy (normally with disconnectors). Power throughput is also lost during this reconfiguration time.

In [49] conversion losses for different converter types were estimated as follows: HB-MMC – 0.6%, FB-MMC – 1.1%, Hybrid-MMC – 0.8-1.1%. The FB and Hybrid MMC are both capable of fault blocking. The estimates demonstrate that this functionality comes at the expensive of a 30% increase in conversion losses in the best case. Losses for blocking converters over the operational lifespan of the converter have been estimated at an additional 81 M Euros [88], an indication as to why they have yet to be adopted for a commercial instillation.

Increased interest in multi-terminal VSC HVDC has led to a renewed phase of research and development of circuit breakers. The perceived operating time requirements for VSC system has led to resonant electro-mechanical topologies being discarded. Ultra-fast electronic circuit breakers have also been rejected on the basis of high losses over the system lifetime (an electronic circuit breaker can require in the order of 160 IGBT modules (IGBT plus diode),

representing a substantial capital cost [84].) New hybrid topologies which have subsequently been proposed, prototyped, and developed by manufacturers are complex. Both ABB and Alstom have intensively developed Hybrid breakers with the aim of providing a low loss, fast operating solution. The circuit breaker topologies both feature what is effectively an electronic circuit breaker with a parallel bypass circuit, to minimise losses in the closed position. The mechanical disconnector used in this bypass path dominates the length of time required for operation (in the order of 2ms-5ms [69]), when compared to the rest of the circuit (typically operating within the 40μs time-frame [84]). This makes the disconnectors a critical component in terms of time delay and has lead to development of the dc breaker being concentrated on it.

The first generation of VSC systems has employed two-level converters, based on series connection of IGBTs. If the network voltage collapses then a significant amount of energy is transferred from the dc capacitance (used in two-level systems) to the fault current, which must then be removed by the breaker. Upon dc voltage reaching zero, the energy transfrered from the capacitors to the dc side inductance is then circulated through the free-wheeling diodes, causing very high currents. When the fault is cleared high currents are then drawn from the network to recharge the dc link capacitors, which is undesirable. This collapse of dc voltage appears to have driven driven the speed requirement for any future dc breakers, to ensure that faults are cleared before the dc voltage drops below the critical rectification voltage (typically in the region of 5ms [28]).

More recently two-level instillations have been superseded by multi-level converters (typically variants of the modular multi-level converter (MMC)) with gains in efficiency and reduction in ac filter requirements [89]. MMC systems also contain no additional dc side capacitor. Instead, converter capacitance is split between the cells in each arm. During a fault the converter is blocked and the capacitors are isolated preventing discharge into the dc fault [42]. This improves the re-start capability of the converter as, depending on system topology, the amount of energy stored in the converter cells will dominate that of the parasitic cable capacitance, leading to a faster re-charge. Reduction in dc voltage is therefore less of a problem for multi-terminal networks based on MMC.

Given that the complexity of the breakers is largely driven by the requirements of their speed it is prudent to question what drives this requirement. If it would be possible to relax the operation speed of the circuit breaker then the choice of breaker topologies would become much broader. Resonant mechanical designs may then become feasible, with a potentially lower cost, in turn assisting the economic case of multi-terminal systems.

This chapter aims to demonstrate that it may be possible to protect MMC based multi-

terminal networks using much slower, less complex and, critically, cheaper dc breaker solutions. A representative three terminal system is used to demonstrate the concept of clearing a dc side fault with, relatively, slow dc breakers. It is shown that the impact of the ac connections may be kept to a minimum and the current within the converters remains within tolerable limit.

Section 7.2 reviews current literature on protection techniques with section 7.3 highlighting the areas still requiring further analysis. Section 7.4 details the converter fault detection and protection methods developed. Section 7.5 details the fault detection and discrimination techniques implemented to trigger and reclose breakers throughout the dc network. In section 7.6 the whole system performance is assessed for different circuit breaker operating speed.

7.2 Methods of Protecting an HVDC Network

Meshed, multi-terminal HVDC networks utilising voltage source converters are susceptible to dc faults, which propagate rapidly throughout the system. The resulting collapse in voltage isolates the converters from one another, making power transfer no longer possible. For the system to re-establish power flow the faulted area of the system must first be isolated. There are several approaches which can be used to protect the system from the high currents which occur as a result of fault, and to subsequently restore power flow within the system. These are described in the following sections.

7.2.1 AC Side Protection with DC Disconnectors

In [90] Tang suggested using fast dc switches (similar to those used as ultra-fast disconnectors within hybrid circuit breakers) to provide galvanic isolation between sections of the network. Figure 7.1 shows the topology proposed, where disconnectors are placed at the end of each line. Disconnectors are labelled using the following convention; SW_{ij}, where i is the line number and j is the converter number. For example, the disconnector which connects VSC3 to line L2 is numbered L_{32}. The disconnectors may only operate under zero voltage and current switching conditions. Therefore, these cannot be used to clear faults. Instead, ac circuit breakers remove the source of current from the network and current on the dc side must naturally decay.

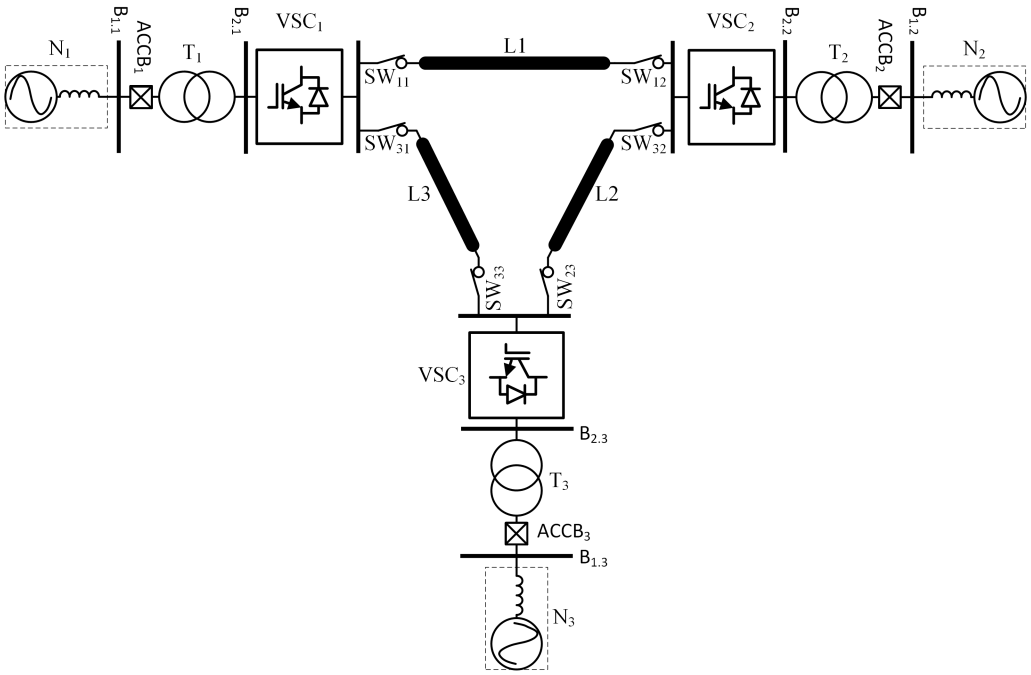

Figure 7.1: Single line diagram of the dc disconnector switch arrangement presented by Tang et al.

7.2.1.1 Operation

Faults are detected by over-current into the lines by the converter stations, at which point ac breakers are triggered. Whilst opening, the converter protection logic selects one line as that which is suspected of having a fault, choosing the line which has the largest current flow into it. Upon the ac breakers opening, and the dc current decaying to zero, the selected disconnector is opened. Figure 7.2 shows the fault current that flow in the case of a fault on line 1. The disconnectors are earmarked to open as follows: VSC1 (SW_{11}) will select line 1 as the potentially faulted line as it has the largest current inflow; VSC2 will also select line 1 (SW_{12}) as the potentially faulted line; and VSC3 may select line 2 or line 3, depending on which has the largest current depends on line impedances and pre-fault condition. In the example given it is assumed that current in line 3 is larger. SW_{33} is, therefore, selected by VSC3.

Once the ac breakers open throughout the system, and current within the dc network has decayed, the selected dc breakers then actuate (see Figure 7.2) and the ac breakers are then reclosed. Disconnectors at both ends of the faulted line are open, and so the line is not recharged, whereas each of the healthy lines remains connected to a converter. When the ac breakers are closed the dc line is recharged to the peak ac line to line voltage. The voltage increase can then be used to determine that the health of the line. Subsequently breakers are reclosed where the line voltage increases past a threshold.

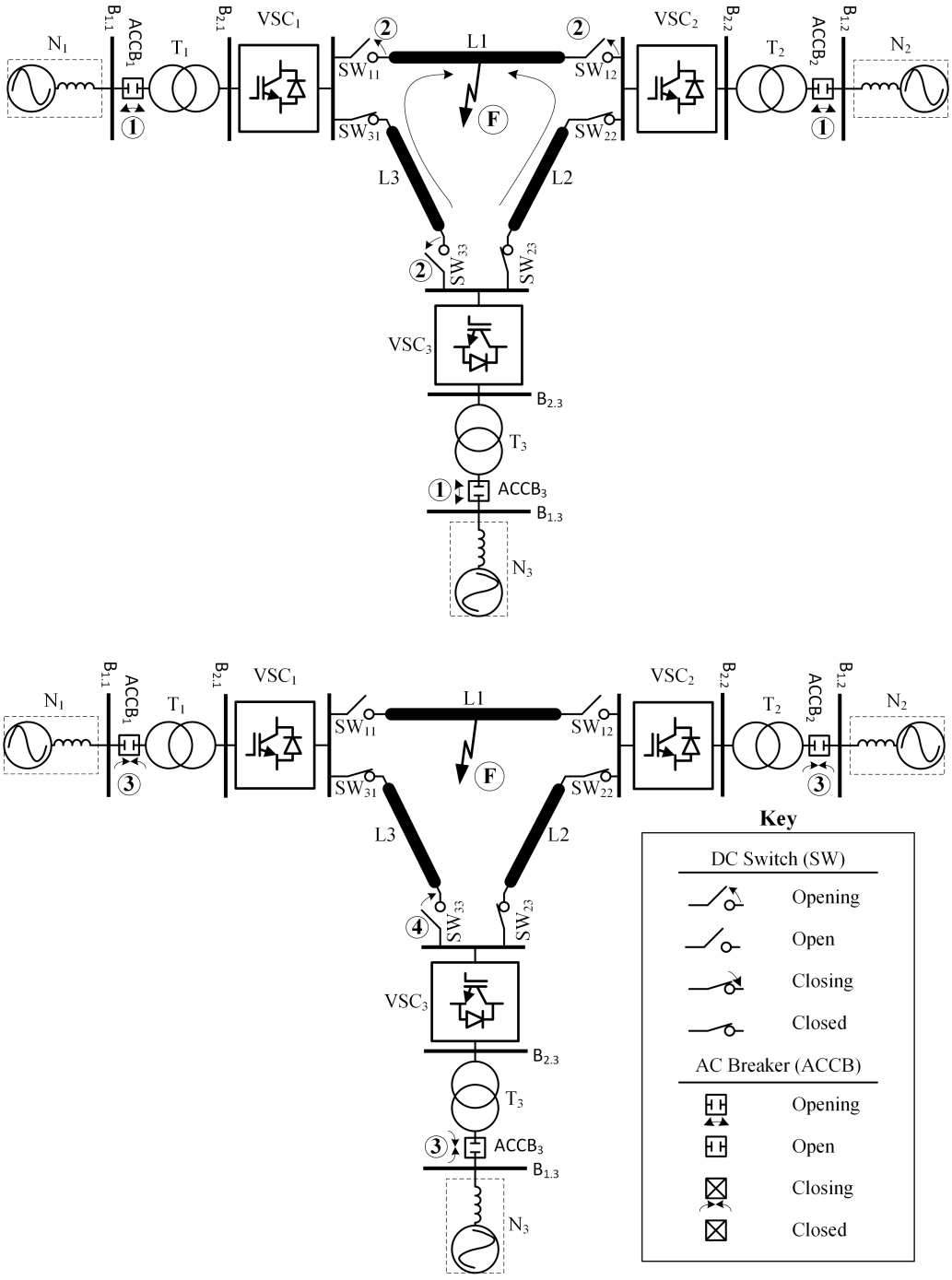

Figure 7.2: Single line diagram of a system where faults are cleared with dc disconnectors. (1) ac breakers opening to clear fault current, (2) disconnectors opening on potentially faulted lines, (3) ac breakers reclosing to re-energise healthy areas of the network, (4) selected disconnectors reclosing due to increase in voltage

7.2.1.2 Summary

The method proposed allows the dc network to clear faults and reconfigure itself with a low cost solution – fast dc switches. The advantage of this solution is that the dc switches used are lower in both capital and life-time cost over dc breakers. With no power electronic components in the load carrying path, their mechanical contacts have a low ohmic loss, similar to that of ac switchgear.

The total time between fault inception to the converters unblocking and the dc voltage stabilising is approximately 500ms for the system demonstrated by Tang [90]. For small systems, where loss of power flow for longer than typical ac clearing times is not critical, then this scheme may be satisfactory. However, for systems with a higher power capacity the loss of power throughput for extended times is unlikely to be acceptable.

Clearing using ac circuit breakers, however, brings two main disadvantages. Firstly, the ac circuit breakers take in the order of 50ms-60ms to actuate [90]. The actuation time to open and reclose, in addition to resynchronising the converter to the network, must be considered. Secondly, the fast dc switches have no current breaking capability they must be opened under zero current. Therefore, there is an additional delay whilst the current decays. In the results presented in [90] this was in the order of 100ms, but could be significantly longer for longer dc line lengths. For example, simulation results are given in Figure 7.3 showing the current decay for different line lengths. In each case a fault was applied and the ac breakers were opened 0.3 seconds into the simulation. Fault current differs in each case due to the variation in effective dc resistance (fault plus cable), which was shown to influence the steady-state fault current in Chapter 4. The simulation demonstrate that longer cable lengths increase the current decay time significantly.

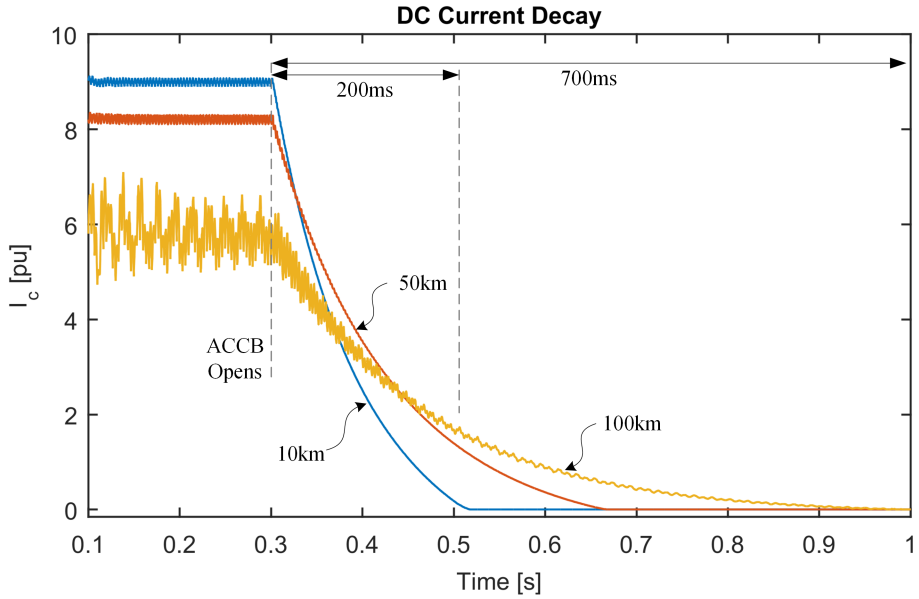

Figure 7.3: DC current decay for variable line lengths when clearing with ac circuit breakers

7.2.2 DC Breakers

An alternative method of isolating faults is to replace dc switches (disconnectors) at the end of each branch with dc circuit breakers. Every lines is treated as an individual protection zone, with breakers located at the end of each branch, on each pole. A fault on any given branch can be isolated from the remaining healthy areas of the system by opening breakers at each end of the branch. Power may then continue to be transmitted around the healthy areas of the network.

Faults are readily detected by the associated rapid voltage collapse and fast current rise. Selecting the appropriate breakers to open requires discrimination of the fault location. In [91] Barker proposed that the circuit breakers are triggered under local measurements only, with no high level communication (removing the time overhead for fault location discrimination). Simulation results within the paper highlighted how both peak current and the associated energy dissipation within the breaker may be reduced by operating in this manner.

Given that circuit breaker operation is not coordinated, it is feasible that breakers on healthy branches are also triggered. To re-establish power flow within the system the breakers on healthy lines must first be re-closed. To determine if the line is faulted or healthy the voltage is monitored by each circuit breaker once opened. If this recovers then the branch is deemed healthy and the circuit breaker is re-closed.

In [91] there is no detail given as to how the branch healthy is established (voltage thresholds etc.). A fixed period of 20ms is assumed for the decision time, but the actual logic does not

appear to have been implemented. Power flow is re-established, and current flow along the branches redistributed, within 50ms of fault inception.

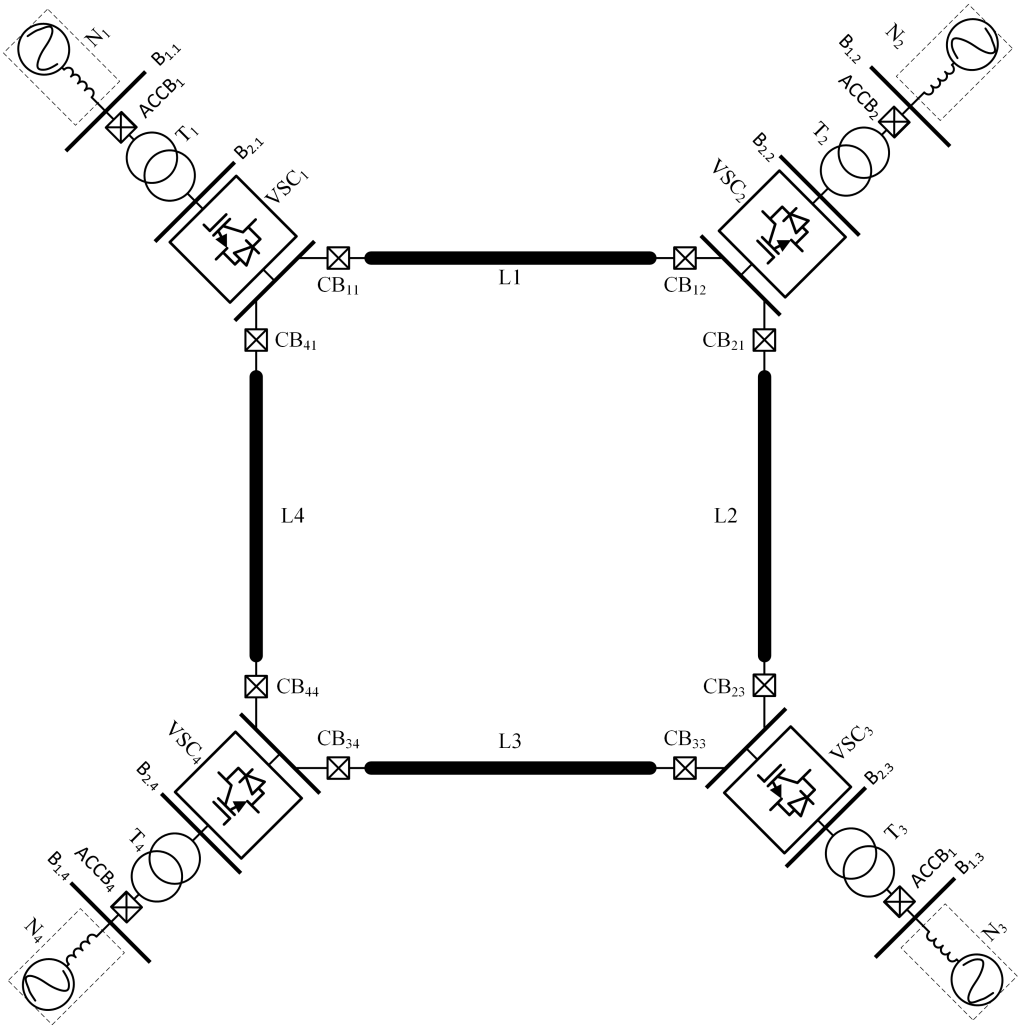

Figure 7.4: Single line diagram of the dc breaker arrangement presented by Barker and Whitehouse

Simulation results for the four terminal ring system given in [91] indicate that power flow can be re-estabished within 25ms (5ms for breaker opening and 20ms for the logic to establish which breakers should re-close). The scheme provides a much faster system response to fault clearance that that propsed in [90] using fast dc switches (25ms verses 500ms). However, this requires high speed circuit breakers operating within a 5ms time frame to provide this type of response. Hybrid circuit breakers are required to provide response of this speed, which means a high cost solution.

7.3 Gaps in the Literature

The strategies presented previously cover two methods to protecting and reconfigure the dc network. Although fast dc switches provide the a lower cost solution the time frame for outages is likely to be prohibitive for larger, higher-capacity systems. Installing dc breakers to segregate each branch into an individual protection zone has the benefit that ac breakers are not required to operate as a primary protective measure. This reduces the overall restart time as the converters are not then required to resynchronise the the grid. Operating these based on local measurements reduces the time from fault inception to breakers opening and therefore reduces the peak current and energy dissipation stress on the breakers.

The demonstration system used in [91] indicated that power flow can be re-established in a time-frame compatible to ac breaker clearing times. However, the accuracy and reliability of the results given is difficult to ascertain. The model used ideal voltage sources to replicate converters with only vary basic control and limitations on their capabilities. In a practical system there are many technical limitations on how fast an individual converter can respond. For example, the simple converter model does not take account of cell capacitor charge (which dictates if the converter can continue to generate the required ac voltage output), maximum current limitations of the converter to source and sink power etc.

Secondly, there is no detail of the logic driving the operation of the circuit breakers, which appear to have been operated in a pre-determined manner. Without taking into account the potential delay in detecting and discriminating the faults it is likely that the system could take longer to restart than proposed.

Within the next sections simulation studies are carried out to investigate the system restart following clearing a fault with dc breakers located at the end of each branch. The protection logic is implemented to trigger/re-close dc breakers. Converter protection logic is also implemented which controls blocking and the restart procedure following unblocking.

7.4 Converter Protection

To ensure that the converter avoids unnecessary damage it must, where possible, protect itself. Protection of the converter forms part of the protection system for the entire network and it must therefore provide a satisfactory response whilst also ensuring that it minimises stress to itself. When a fault is detected the converter cells are blocked (gating off the IGBTs). The converter should be unblocked only when the fault current has been removed, by isolating the fault.

To demonstrate the methods developed to detect faults, and the subsequent impact blocking has, a two terminal system is used. The test system used is shown in Figure 7.5. The average model described in Chapter 2, Section 2.4.3 is in Matlab Simulink to perform all simulations. Circuit parameters are given in Table 7.1. Measurements shown are those taken from VSC1. VSC1 operates on from a power reference and VSC2 operating under DC voltage control (PI). Power references of +500MW and -500MW for VSC1 and two fault locations are used to demonstrate the impact of pre-fault power flow has on fault detection.

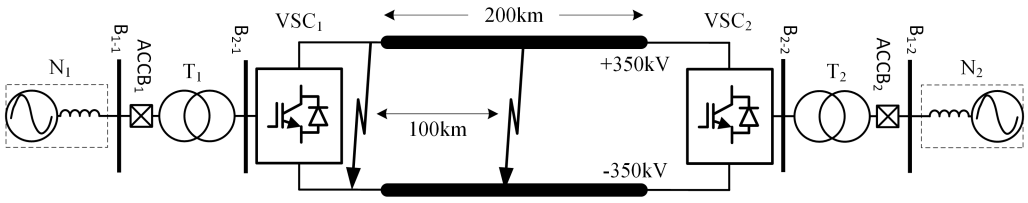

Figure 7.5: Converter protection demonstration system

Table 7.1: Converter Parameters: VSC1 and VSC2

	Parameter	Value	Notes
S_n	Network strength	17GVA	
V_{B1}	Bus B1 voltage	400kV	Nominal, line-to-line RMS
V_{B2}	Bus B2 voltage	375kV	Nominal, line-to-line RMS
S_c	Rated power of converter	1000MW	PF = 0.95
V_{dc}	Nominal dc voltage	700kV	Pole-to-pole
X_{TRM}	Transformer leakage	0.13pu	Per unit
L_{arm}	Arm inductance	0.10pu	Referred to B2
D_{line}	Line length	200km	
R_{fault}	Fault resistance	100mΩ	

7.4.1 Converter Enable/Blocking

The average model used for simulation includes blocking functionality to enable it to perform fault studies (see Chapter 2, Section 2.4.3). To demonstrate the impact blocking can have on the stress placed on the converter some simulation examples are given. A low impedance (100mΩ) fault is placed at the mid point of the 200km point-to-point link 0.5 seconds into the simulation. In the first case the converter continues to operate and in the second the converter is blocked upon detection (see Section 7.4.2). The voltage and current measured at the dc side of the converter for both cases are shown in Figure 7.6. Where the converter is not blocked

current overshoots the steady state value, reaching approximately 14pu of rated dc current (1pu = 1429A). With blocking the current reaches steady state within approximately 25ms, with a first-order characteristic.

Cell voltages are shown in the lower plots of Figure 7.6. Where the converter is not blocked the average cell capacitor is rapidly drained (within approximately 20ms), making system restart more challenging. With the converter blocked upon fault detection the cells cannot discharge and do not contribute current to the fault. As they maintain their healthy voltage of approximately V_{dc} they do not require recharging before restarting the converter when the fault is cleared.

Hybrid or full bridge MMC allows the control of ac and dc currents to be decoupled. The current controller presented by Zeng actively manipulates the dc voltage component of modulation function in order to control dc side current [48]. The controller schematic is shown in Figure 7.7. The control is possible because a hybrid converter is used, mixing full bridge cells and half bridge cells, which it to counter the ac side voltage even with a suppressed dc side voltage.

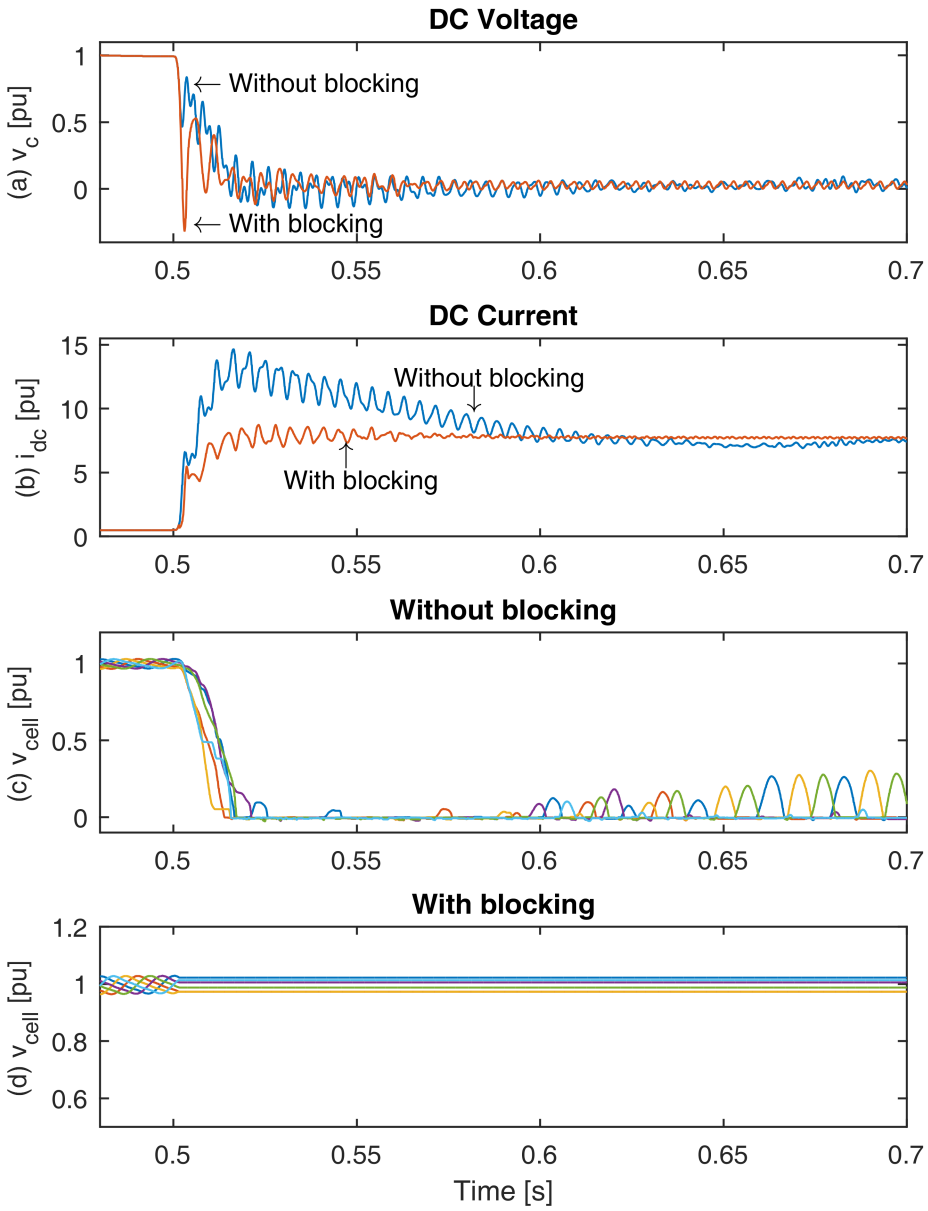

Figure 7.6: Comparison of blocking and non blocking. (a) converter dc side voltage, (b) converter current contribution, (c) cell capacitor voltages without blocking, (d) cell capacitor voltages with blocking

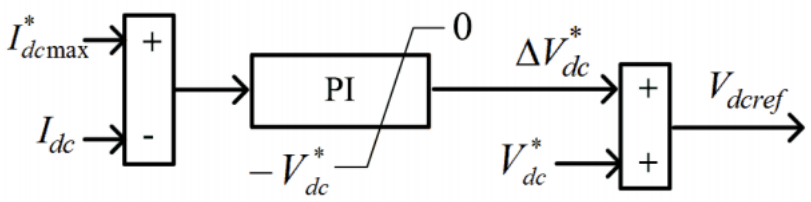

Figure 7.7: Schematic diagram of the maximum DC current controller presented in [48]

7.4.2 Fault Dsetection

The rapid rate-of-rise of current within the converter dictates that fault detection should be based on local measurements. Under-voltage occurs during faults but may also occur when power flow within the network is not balanced transiently (e.g. during restart). In either case, the result can be an uncontrolled current flow from the ac side to the dc (diode rectifier action) and the converter must be blocked. Equally, where system voltage is high the converter should also be blocked. During a fault the arm and dc currents will rise and the dc voltage will fall, which may be used to detect them. Readings outside of the safe area of operation (SOA) indicate that a fault condition may be present within the dc network and the fault flag is set. Thresholds are set as follows: the upper dc voltage is given by the MOSA clamping level, lower dc voltage by the peak ac line-to-line voltage at bus B2 (representing the rectified voltage), and maximum dc and arm current at 1.25pu. Table 7.2 summarises the thresholds. The detection mechanism includes a hysteresis loop to ensure that the converter doesn't 'hunt' in and out of a blocking and non-blocking state.

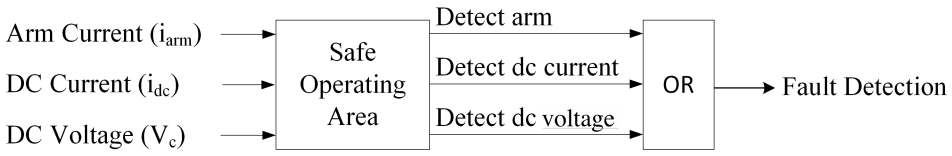

Figure 7.8: Fault Detection. Arm current, dc current and dc voltage are used to determine if a fault is present. Measurements are compared against references and logically gated together. The combined fault detection flag includes a hysteresis loop to minimise oscillations.

Table 7.2: Summary of converter detection thresholds

	Value	Notes
Upper dc voltage limit	1.5puV_{dc}	Set at the clamping voltage of the pole surge arresters
Lower dc voltage limit	$\hat{V}_{B2}$	Line-to-line voltage
Upper arm current limit	1.25pu	Of rated peak current whilst operating at maximum P/Q
Upper dc current limit	1.25pu	Of rated current at maximum power

Figure 7.9 shows the fault detection signals from a sample simulation case. The fault was placed 100km from the converter 0.5 seconds into the simulation. The converter electrical measurements and fault detection signals are given to show when the converter is outside the safe operating area.

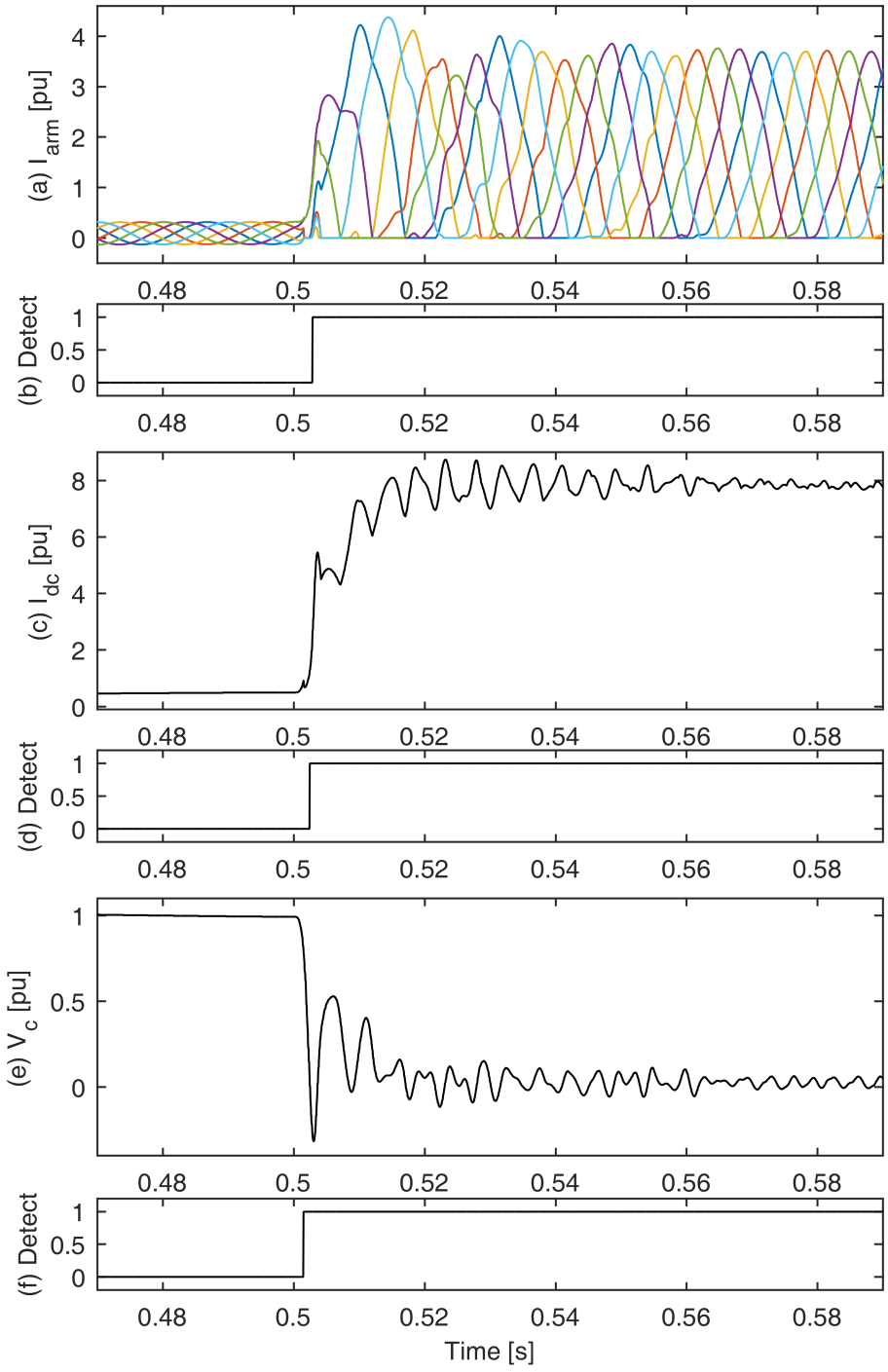

Figure 7.9: Fault detection simulation. (a) arm current; (b) over-current detection, threshold at 1.25pu of rated peak current whilst operating at maximum P/Q; (c) dc current; (d) over-current detection, threshold at 1.25pu of rated current at maximum power; (e) dc side voltage at the converter; (f) under/over voltage detection, upper threshold at 1.5puV_{dc} lower threshold at peak ac line-to-line voltage

Figure 7.10 shows the fault detection flags for four initial conditions (power flow in both directions and different fault distances). For distant faults (plots a and b), the initial power flow conditions have a minimal effect on the detection time. In both cases under-voltage is detected within approximately 1.5ms of the fault being applied. Where faults are placed at the converter terminals (i.e. zero distance from the converter) fault detection time is significantly faster (plots c and d). Where initial power flow is negative (current from the dc side to the ac side) over-current detection is between 0.5ms and 1ms slower, corresponding to the change in current flow direction required.

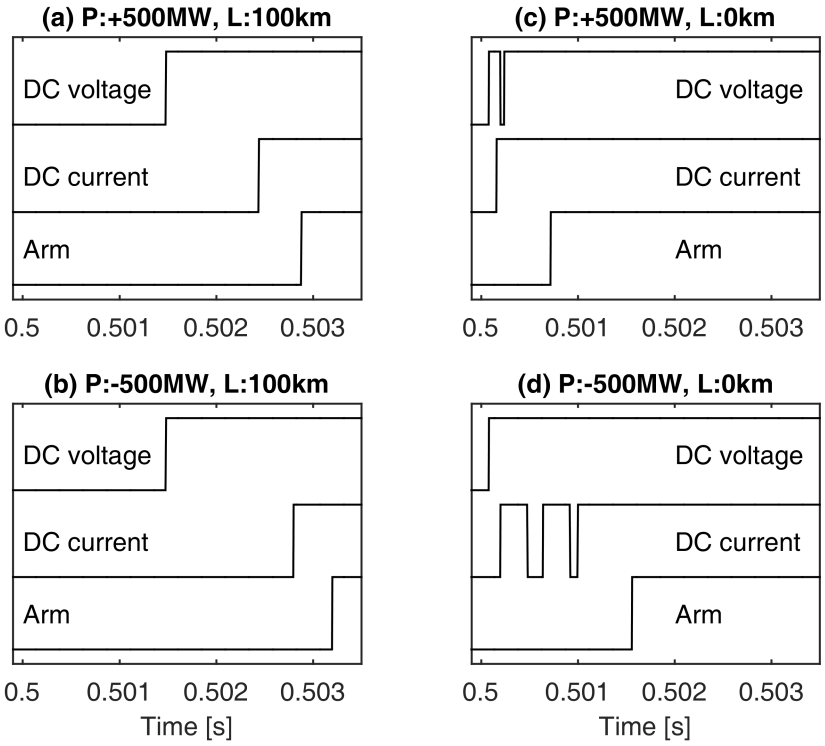

Figure 7.10: Fault detection simulation for different initial conditions: (a) power:+500MW, fault distance: 100km, (b) power:-500MW, fault distance: 100km, (c) power:+500MW, fault distance: 0km, (d) power:-500MW, fault distance: 0km. Detection threshold for dc voltage: upper threshold at 1.5puV_{dc} lower threshold at peak ac line-to-line voltage. Detection for dc current at 1.25pu of rated current at maximum power. Detection for arm current at 1.25pu of rated peak current whilst operating at maximum P/Q. Detection flags are based on raw thresholds, overall fault detection flag includes hysteresis to reduce oscillations

7.4.3 Circuit Breaker Position

The converter is only enabled when two conditions are met: no fault is detected and the converter is connected to the dc network (via at least one line). The positions of all dc circuit breakers located at the terminals of the converter are fed into the protection logic, as shown

in Figure 7.11. This ensures that if the converter is not directly linked to the rest of the dc network, then it remains disabled (blocked). If the converter is not held in a disabled state then shortly after the breaker opens the converter would register the fault as being clear and automatically re-enable itself. With no connection to the rest of the dc network then the cell capacitors would rapidly become under/over charged.

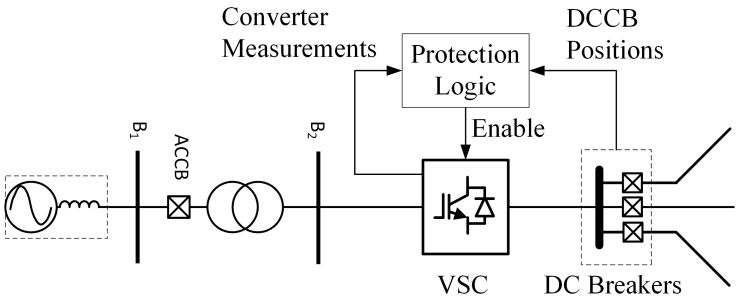

Figure 7.11: Converter enable based on circuit breaker position

Simulation results are given in Figure 7.12. A fault is initiated at 0.5 seconds into the simulation 100km from VSC1 (see Figure 7.5). The circuit breaker is not operated under automatic triggering (from fault detection). Instead it opens after a fixed 40ms delay in order to observe the system response. The fault is detected by the converter within approximately 1.5ms (plot (a)) causing it to block (plot (b)). At 0.54 seconds into the simulation the circuit breaker opens (plot (c)) causing the the dc voltage to rapidly increase (plot (d)) and the current to decrease to zero (plot (e)). Maximum voltage is constrained to 1.5pu by the MOSAs placed at the converter terminals. Within a further 6ms the dc voltage, dc current and arm currents are back within the safe area of operation and the fault detection flag is reset (plot (a)). However, the converter is not re-enabled as the circuit breaker position is open (plot (c)). The increased dc voltage causes current built up within the converter arms to feed into the cell capacitors, increasing their charge (plot (f)).

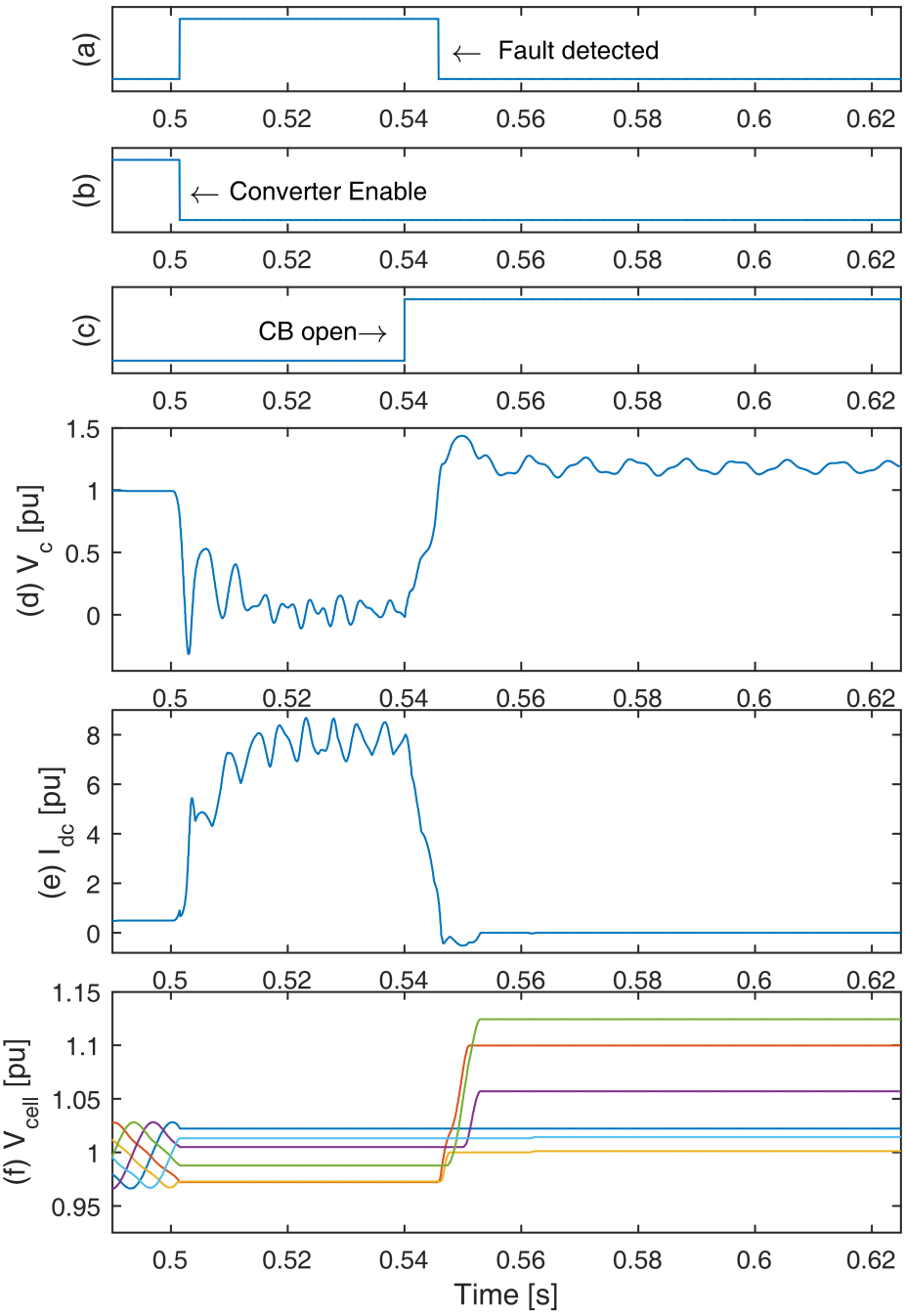

Figure 7.12: Simulation demonstration of converter blocking due to circuit breaker position: (a) fault detection, (b) converter enabled/blocked, dc breaker open/closed, (c) (d) dc voltage, (e) dc current, (f) cell voltages

7.4.4 Current Controller Reset

While the converter is blocked the controller actions have no impact on the current flow through the converter. An constant error will be present which can lead to integrator 'wind-up'. When the converter is re-enabled the output from the PI compensator can initially force an undesired response and then take some time to re-adjust. To facilitate a faster response following fault clearing, the current controller integral terms are reset upon the enabling of the converter. Figure 7.13 shows the block diagram for the current controller reset.

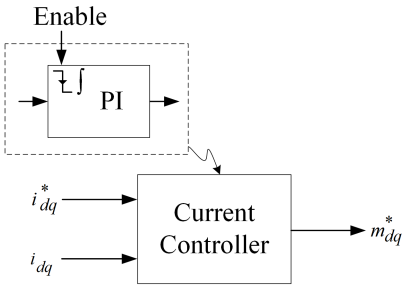

Figure 7.13: Current controller reset after blocking

7.5 Protection Zones

7.5.1 Test System

To demonstrate the protection zone circuit breaker operation logic a three terminal system is used based on [90]. Figure 7.14 shows a single line diagram of the system. The three converters used are identical in their parameters, which are given in Table 7.3. DC network parameters are given in Table 7.4. Initial conditions for the system and converter control set points are given in Table 7.5. For the purposes of demonstrating the protection system a fault is placed at the mid point of Line 1 (125km from VSC1 and VSC2). The aim of the studies in this section is not to investigate maximum stress on the converter and breaker. The aim is to investigate the how reconfiguration and restart takes place, when all detection and re-closing logic is considered. The symmetrical topology and fault scenario chosen can cause circuit breakers at both cable ends to open simultaneously, allowing the re-closing algorithm to be tested.

7.5.2 Protection Zones

DC breakers located at the end of each line both poles. The breakers are used to clear fault currents and isolate the faulted section of the network from the healthy. The combination of

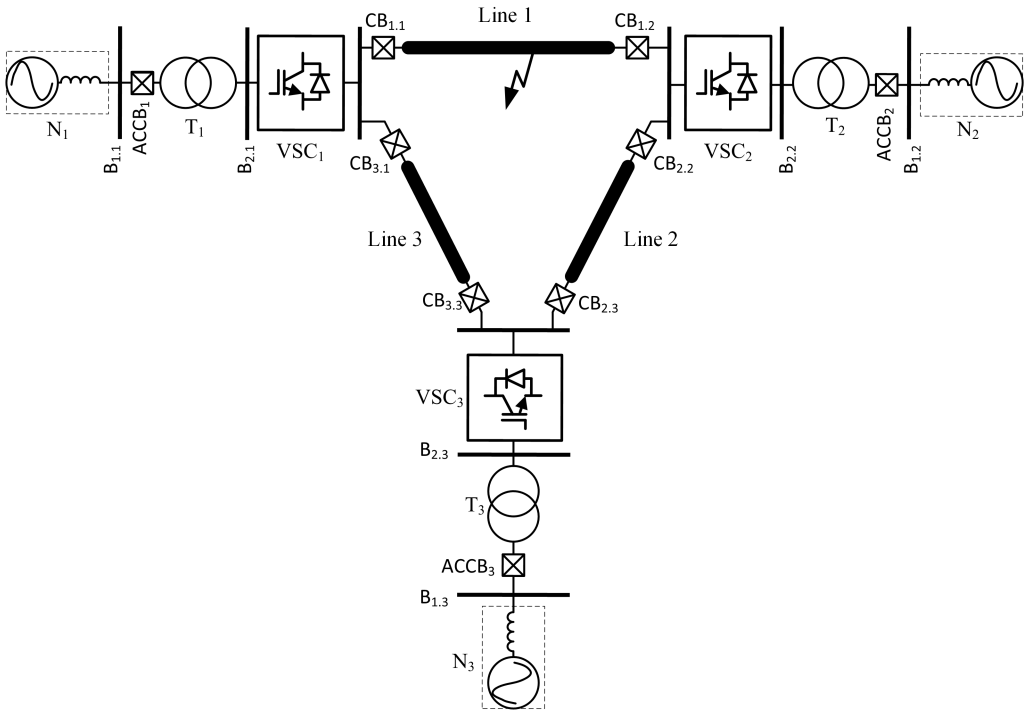

Figure 7.14: Single line diagram of the protection zone demonstration system

the line, dc breakers and the logic to drive them forms a protection zone. In the demonstration system there are three protection zones, one associated within each connection between two converters. A proction zone is shown in Figure 7.15. Shorthand notation is used for measurements throughout the network for plotting purposes. Currents and voltages are measured at each end of each line. The suffix of the label refers to the line and end, in the form V_{XY}, where X denotes the line number and Y denotes the converter number at that end of the cable. For example, V_{32} denotes the voltage measurement taken at the line side (i.e. the line side of the

Table 7.3: Converter Parameters: VSC1, VSC2, VSC3

	Parameter	Value	Notes
S_n	Network strength	17GVA	
V_{B1}	Bus B1 voltage	400kV	Nominal, line-to-line RMS
V_{B2}	Bus B2 voltage	375kV	Nominal, line-to-line RMS
S_c	Rated power of converter	1000MW	PF = 0.95
V_{dc}	Nominal dc voltage	700kV	Pole-to-pole
X_{TRM}	Transformer leakage	0.13	Per unit
L_{arm}	Arm inductance	0.10	Referred to B2
V_{cb}	DCCB Clamping voltage	525kV	1.5pu pole voltage

Table 7.4: DC Network Parameters

	Line 1	Line 2	Line 3
Rated Power	1000MW	1000MW	1000MW
Rated Voltage	700kV	700kV	700kV
Rated Current	1429A	1429A	1429A
Line Length	250km	100km	100km

Table 7.5: Initail Conditions

Converter	Control Mode	Power reference
VSC1	P/V_{ac}	-400MW
VSC2	V_{dc}(droop)/V_{ac}	N/A
VSC3	P/V_{ac}	+600MW

circuit breaker rather than the converter side) voltage measurement of the end of Line 3 at VSC2; I_{12} is the current flowing out of the breaker located at VSC2 into Line 1.

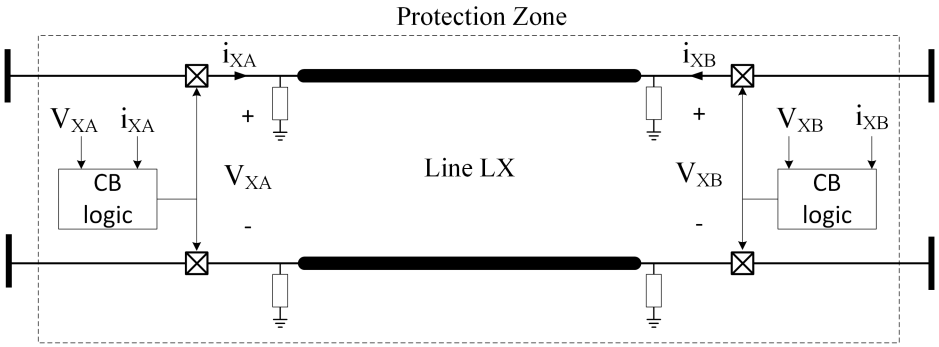

Figure 7.15: Protection zones

Differential protection (comparing the current measurements into and out of the two line ends) can be used to determine if the fault is located within the protection zone and, therefore, if the breakers should be operated. However, this requires communications between the two cable ends, introducing a time delay [92]. Given the rapid transients present within HVDC systems during faults, this could add a significant time overhead. Local measurements are instead used to determine whether to operate breakers.

Faults can be readily detected by the collapse in dc voltage (see Figure 7.9). However, as the voltage is common to all branches at a given node detection by voltage only indicates the presence of a fault, rather than providing information about its location. When a fault is present in a line excessive current flows into it from the external network (other lines and

converters which source the current). Excessive current flowing out from a line indicates a fault within another part of the network (outside of the protection zone being monitored). In this way information of the faults location can be ascertained. As there is no communication between the two ends the protection zone circuit breakers are operated independently.

Operating the protection in this manner can cause breakers on healthy lines to operate as well as those on faulted lines. For example, circuit breaker located at the VSC3 end of Line 3 can potentially see an inrush of current during a fault on Line 1. As far as Line 3 is concerned this indicates that there is potentially a fault in Line 3, thus triggering breakers $CB_{3.3}$ to open. This means that following a fault the network may not be configured correctly and can have open circuit sections in otherwise healthy areas. Without the appropriate circuit breakers re-closing the system cannot re-establish power flow. In [90] and [91] the residual voltage on the dc line was used to determine the heath of the cable.

7.5.3 DC Breaker Modelling

The dc circuit breaker forms an integral part of the system model. Its response plays a large part in the response and recovery of the network during faults. The time constants during some of the transitional periods the dc circuit breaker operation can be extremely short when compared to those of the network itself. Current may commutate between two parts of the breaker in time spaces as small as tens of microseconds whereas it may take ten to twenty milliseconds for the dc current to rise at a distant converter station. Therefore, it is impractical to simulate both the network and the DCCB in detail in a concurrently, which would allow the nuances of both to be observed.

In this chapter the network performance and interaction between the protection mechanisms is being studied and the internal operation of the DCCB is not a primary focus. In Chapter 5 the different circuit topologies for HVDC breaker were reviewed. Although each of the topologies has a different method of operation the underlying principle was the same; the breaker must create a counter-voltage greater than the system voltage and then dissipate the stored energy. The difference each topology has on the system response is related to their operation speed, rather than internal make-up. Therefore, in this study it is only required to consider the time delay between triggering the breaker and it generating counter-voltage.

The external characteristics of the DCCB can be replicated readily by an ideal switch and an MOSA to clamp the voltage (Figure 7.16). By adjusting the time delay from when an open command is given to it to the time it provides a counter-voltage it may be used to represent any of the main dc breaker topologies and compare how different breaker topologies effect the

network response.

Within Matlab Simulink the MOSA is modelled as a voltage dependant current source. As the breaker is placed in series with the line there can often be significant un-clamped inductances within the circuit in series with the breaker. As these inductances are also modelled as current sources it becomes difficult for the simulation to converge. By including an RC snubber an alternative current branch is created and allows the model to convergence during the fast transients of the breaker opening, without an prohibitive small time-step or significant alteration to circuit breaker operating time.

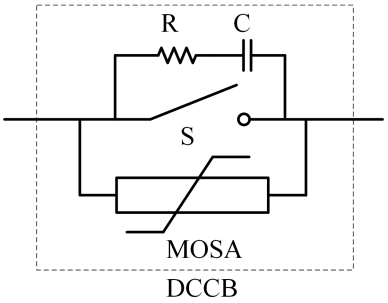

Figure 7.16: Ideal switch model of generic dc circuit breaker used to perform simulations in Matlab Simulink

7.5.4 Residual Line Voltage

In this section the residual voltage on healthy and unhealthy lines is demonstrated. A fault is placed at the mid-point of Line 1 0.5 seconds into the simulation (network topology is shown in Figure 7.14). The converters are not automatically re-enabled upon clearing of the fault so that the natural response of the system can be observed without the influence of the converter control. The circuit breakers are tripped upon fault detection, based on current direction. Again, to observe the natural response of the system they are locked in the open position triggered (no re-closing).

Figure 7.17 shows measurements of dc voltage, current and circuit breaker positions for Lines 1 and 2. Voltage measurements are taken from the VSC 2 end of Line 1 and VSC 3 end of Line 2 (cable side) – through circuit breakers $CB_{1.2}$ and $CB_{2.3}$. In both lines, fault current is drawn into the line which causes the breakers to be triggered (see protection zone logic, Section 7.5.2). The circuit breaker operation introduces a 10ms delay, after which breakers open and produce a counter-voltage. Upon breaker CB1.2 opening the current is rapidly forced down. The large transient induces an oscillation within the voltage of Line 1 ($V_{1.2}$), which damps as the remaining energy within the cable is dissipated. However, the mean residual voltage is zero.

The rapid disturbances to the system also induces oscillations to the voltage on Line 2 ($V_{2.3}$). Energy stored within the system inductance from additional current during the fault is transferred to the cable capacitance, restoring the voltage of Line 2. This residual voltage, of approximately 1pu, indicates the health of the line. This demonstrates that the residual voltage on each line indicates the health of the cable whether it is faulted or not.

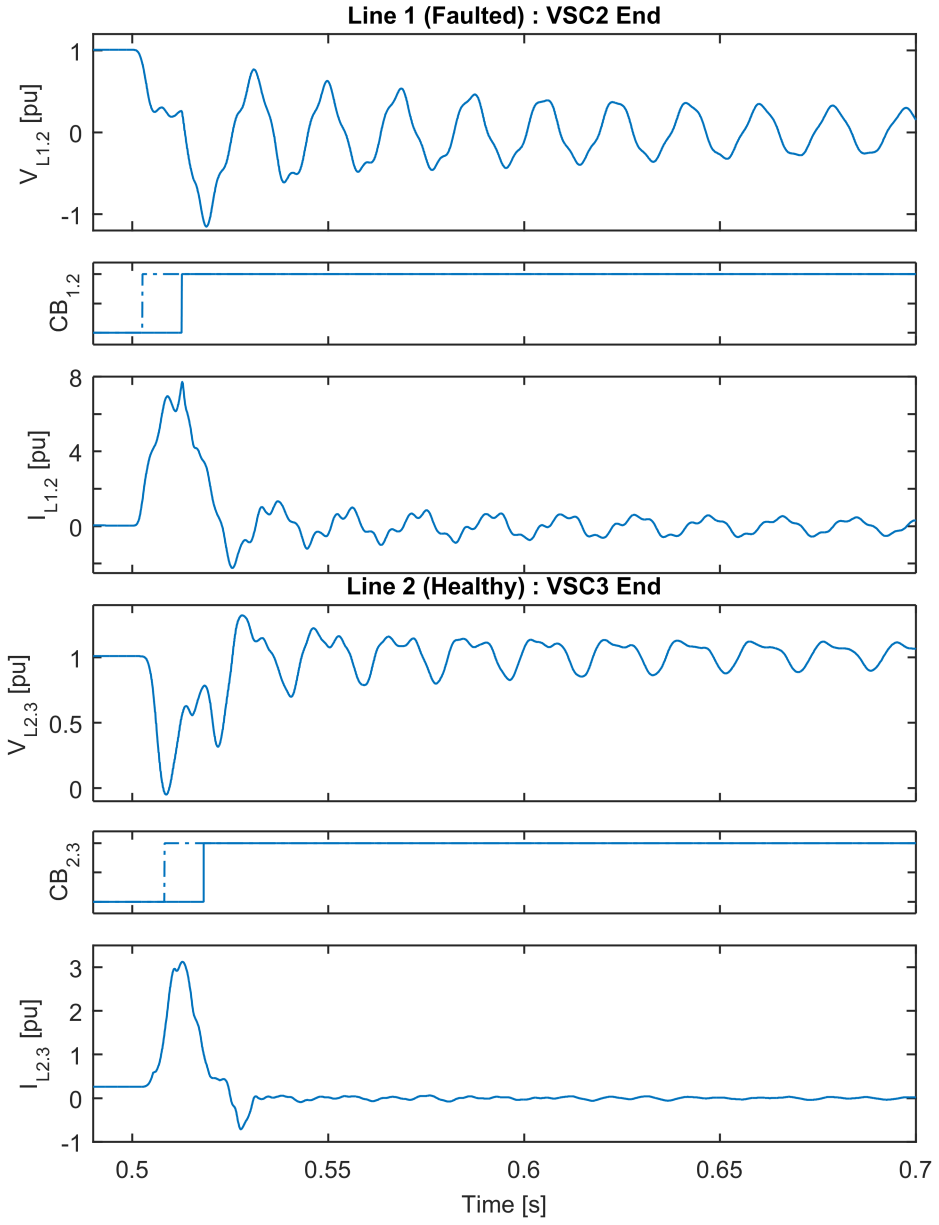

Figure 7.17: Circuit breaker operation on faulted and healthy lines. Dashed line – circuit breaker tripping and reclose signal. Solid line – circuit breaker position

7.5.4.1 DC Voltage Filter

In Figure 7.18 the measured voltage at $CB_{1.2}$ and $CB_{2.3}$ are shown (taken at the cable side). Voltage on the faulted line can have a significant oscillation once the breakers are opened, as plot (a) demonstrates. If this measurement is used directly to infer the health of the line the breaker could be triggered to reclose, reenergising a the faulted line. To avoid this a low pass filter (first order filter with a 10ms time constant) is used to infer the health of the line. This is engaged 10ms after the breaker has reached the open position, to minimise the impact of the transients occurring during fault clearing. (As shown in Figure 7.17, the dc voltage recovers on the healthy line and stabilises around zero on the faulted line within 10ms to 20ms.)

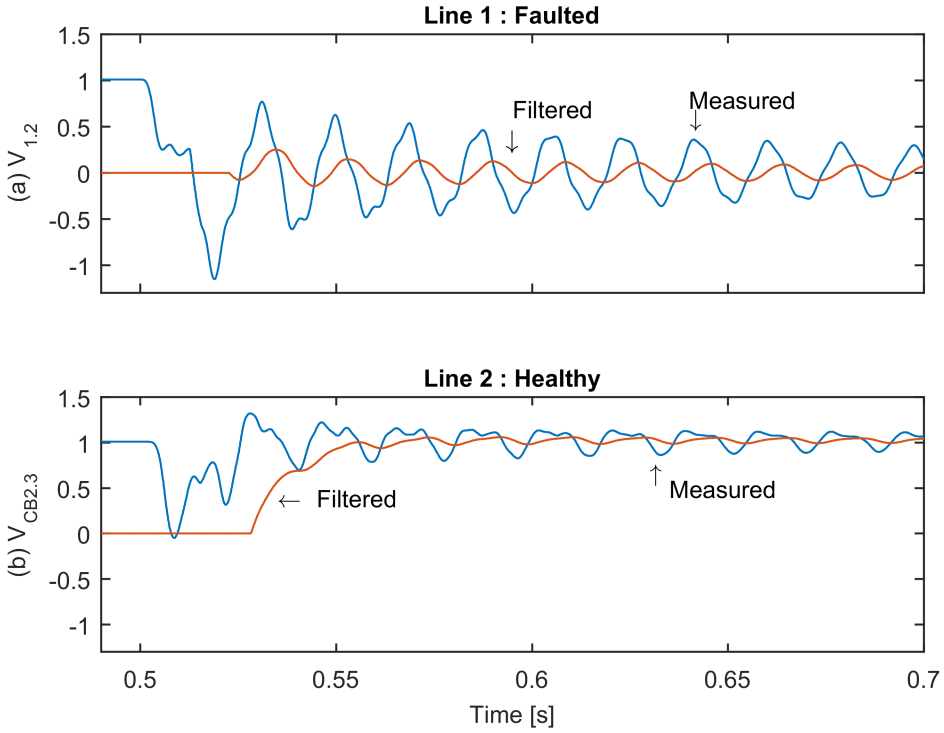

Figure 7.18: Filtered dc voltage measurements. (a) faulted Line 1, (b) healthy Line 2

7.5.5 Circuit Breaker Logic, Fault Discrimination and Reclosing

The circuit breaker logic is shown in Figure 7.19. The first flow chart, the detection and triggering loop, controls the demanded circuit breaker positioning. The second is used to replicate the circuit breaker movement based on a commanded position.

7.5.5.1 Triggering and reclosing

The first logic set operates as follows. In the start position the circuit breaker is initially untriggered (closed circuit breaker demand). The dc voltage filter measurement is also disabled (it is set to follow input V_0). If current into the branch exceeds the threshold I_{trip} then state two is reached, which triggers the circuit breaker opening sequence. After a fixed time delay (t_{filter}) the dc voltage measurement filter is initiated. This gives time for the circuit breaker to physically operate, clear the fault and the dc voltage to stabilise. If the dc voltage increases past the threshold V_{th} then the branch is deemed to be healthy and the circuit breaker is set to be reclosed.

7.5.5.2 Circuit breaker actuation

The second flow chart is used to control the physical movement of the circuit breaker. It is designed to mimic delay caused by the physical actuation and operation of the circuit breaker (e.g. the movement of the ultra-fast disconnector, in the case or the hybrid topology). The time delay induced can be set arbitrary in order to replicate the speed of the different circuit breaker types.

In the start position the circuit breaker position is set to logic 0, representing the closed state (1 representing the open position). When Trip == 1 (set by the detection loop) circuit breaker operation is initiated. The circuit breaker only operates after a fixed delay period of t_{mech} which represents the physical delay from circuit breaker activation to it producing a counter-voltage. This is generally governed by the mechanical delay of any moving parts within the circuit breaker. After the mechanical delay the circuit breaker position (CB_{pos}) is set to logic 1 (representing the open state). Until the trip signal is reset to logic 0 the state-machine will continue in this position. Upon receiving a reclose signal a further mechanical delay period is applied before the breaker position is set to closed.

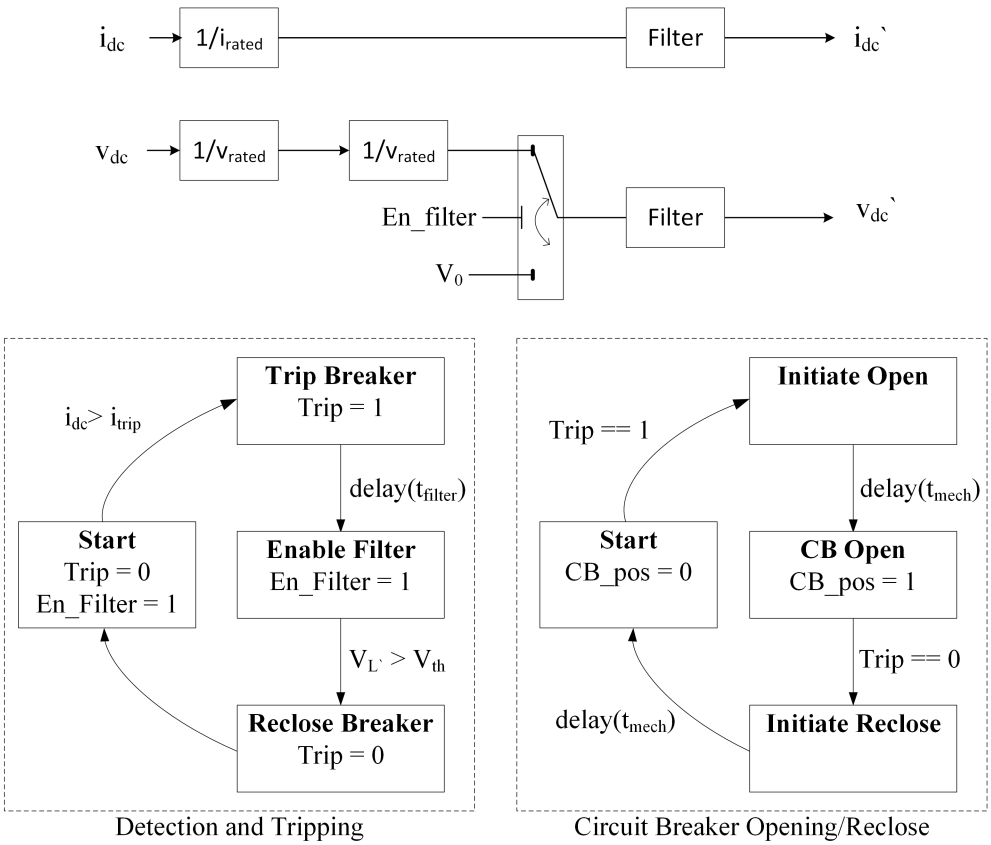

Figure 7.19: Circuit breaker logic for tripping and reclosing

7.5.5.3 Simulation Results

A fault is placed at the mid point of Line 1 0.5 seconds into the simulation. The system diagram is repeated in Figure 7.20 for clarity. Circuit breakers are operated according to the protection logic described (Figure 7.19). Converters are not re-enabled following fault clearance in order to observe the natural response of the system, recharging of the healthy lines and the re-closing procedure. Voltage (filtered and measured) and current measurements and breaker positions for the three lines are given in Figures 7.22, 7.23 and 7.24 showing the operation of the fault detection and discrimination logic. Figure 7.21 shows a summary of the detection and actuation signals for circuit breakers on each of the three lines. A more detailed description follows.

In Figure 7.22 plots are shown for measurements taken at both ends of Line 1: VSC1 end in the upper plots and VSC2 end in the lower plots. The fault causes a large inrush of current into the line from both ends. The increased current triggers breakers to open at both ends of the line, which open after the fixed delay period (10ms). Once breakers open the current decays within approximately 15ms. Voltage at both ends oscillate around zero as the remaining energy trapped within the line is dissipated. The large voltage oscillations on the line are attenuated

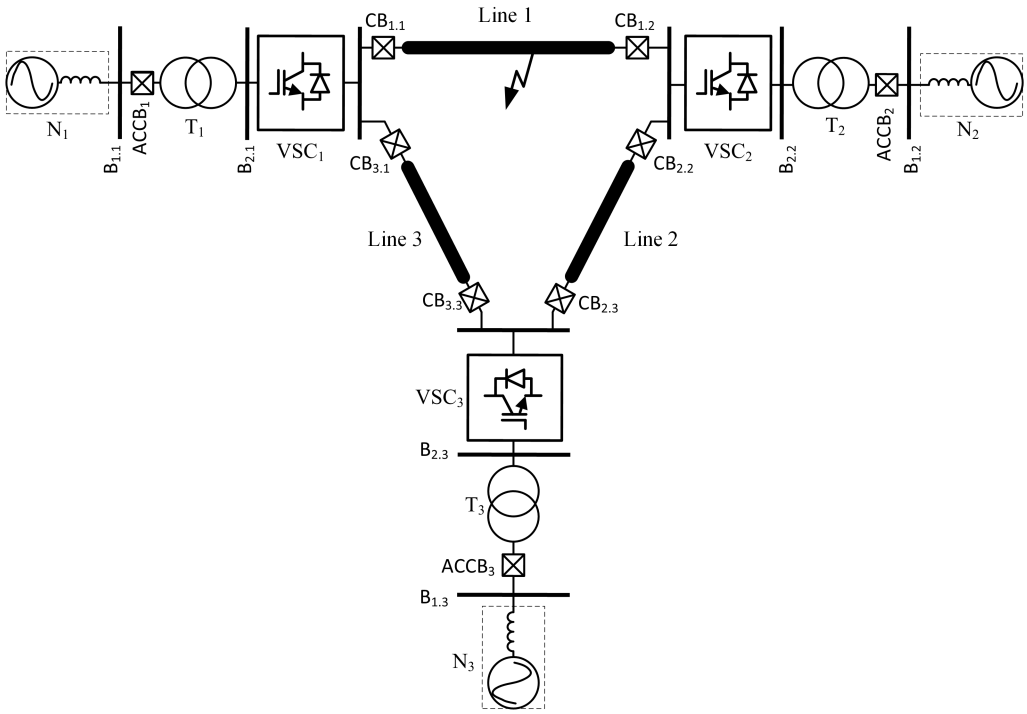

Figure 7.20: Single line diagram of the protection zone demonstration system topology. Fault located at the mid-point of Line 1

by the filter, ensuring that the breakers are not reclosed.

Measurements taken at both ends of Line 2 are shown in Figure 7.23. Measurements from VSC3 are given in the upper plots and VSC2 in the lower. Current is contributed from VSC3 into Line 2 to feed the fault in Line 1. This contribution of current causes breaker $CB_{2.3}$ to be tripped and subsequently open. Once the filtered voltage is enabled (10ms after the $CB_{2.3}$ opens) it increases to an average value of approximately 1pu. This causes the circuit breaker logic to register the branch as healthy and reclose the breakers at that end.

Current drawn from Line 2 into the fault does not initially cause the breakers to be tripped at the VSC2 end as the current direction is negative (out of the cable). However, clearing of the fault by breakers on Line 1 ($CB_{1.2}$) forces current into Line 2. This is caused by the stored energy built up in the converter inductances which must be released. Where this current was flowing into the fault though Line 1 it is now diverted into Line 2. The overcurrent into the line then triggers the breakers to open, as shown in the lower plots of Figure 7.23. For a short period both breakers located at both ends of Line 2 are open. However, the residual voltage that remains on the line causes both sets of breakers to reclose after a short time, as described in the reclose algorithm in Section 7.5.5.

Line 3 (Figure 7.24) experiences simulator phenomena to Line 2. Breaker $CB_{2.3}$ is triggered first due to the inrush of current to the cable (feeding the distant fault within Line 2). When

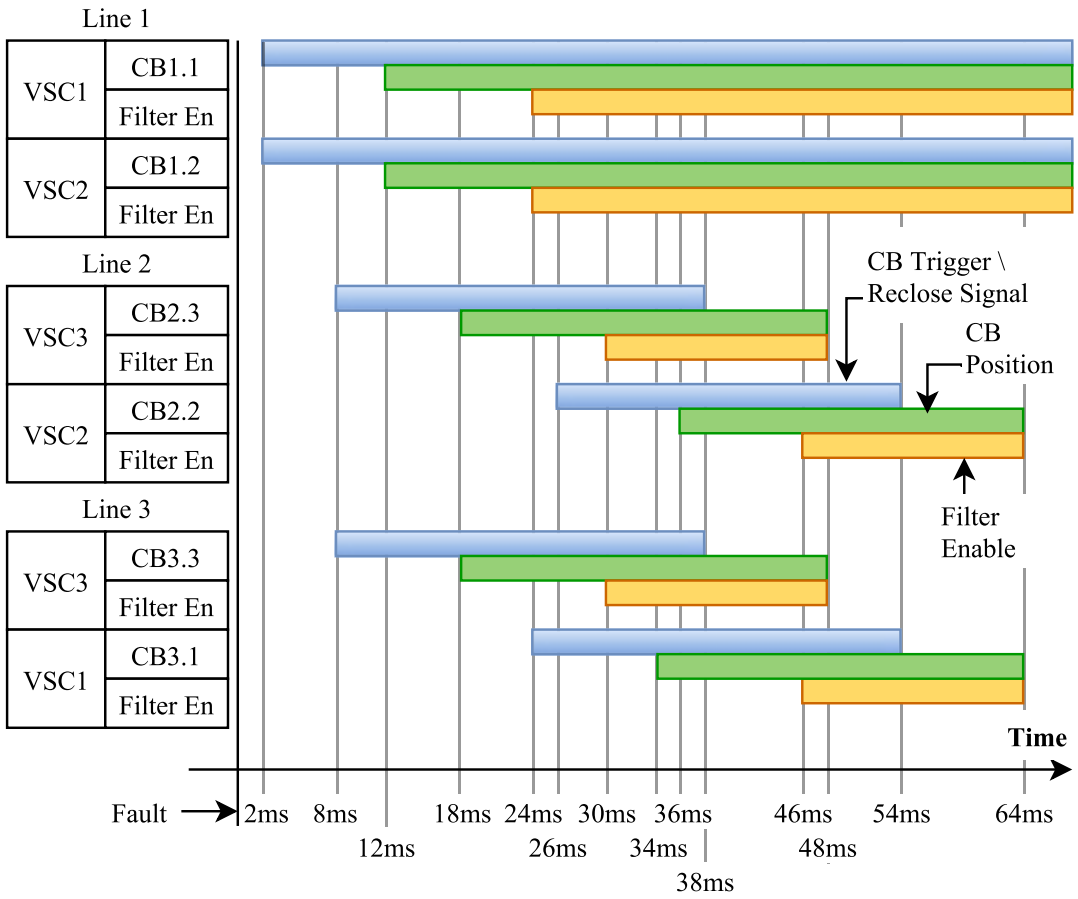

Figure 7.21: Summary chart of dc breaker triggering and reclosing operations. Circuit breaker triggering / reclosing signals, circuit breaker positions and line voltage filter enable signals are shown for both ends of each of the three lines. Time instances shown are measured with reference to the fault occurring at 0.5 seconds into the simulation

the fault is cleared by $CB_{1.1}$ the temporary inrush of current experienced causes breaker located at VSC1 end ($CB_{3.1}$) to be triggered also. The residual voltage on the line is detected by the filtered measurement taken after the breaker has opened and both sets of breakers $CB_{3.1}$ and $CB_{3.3}$ are reclosed.

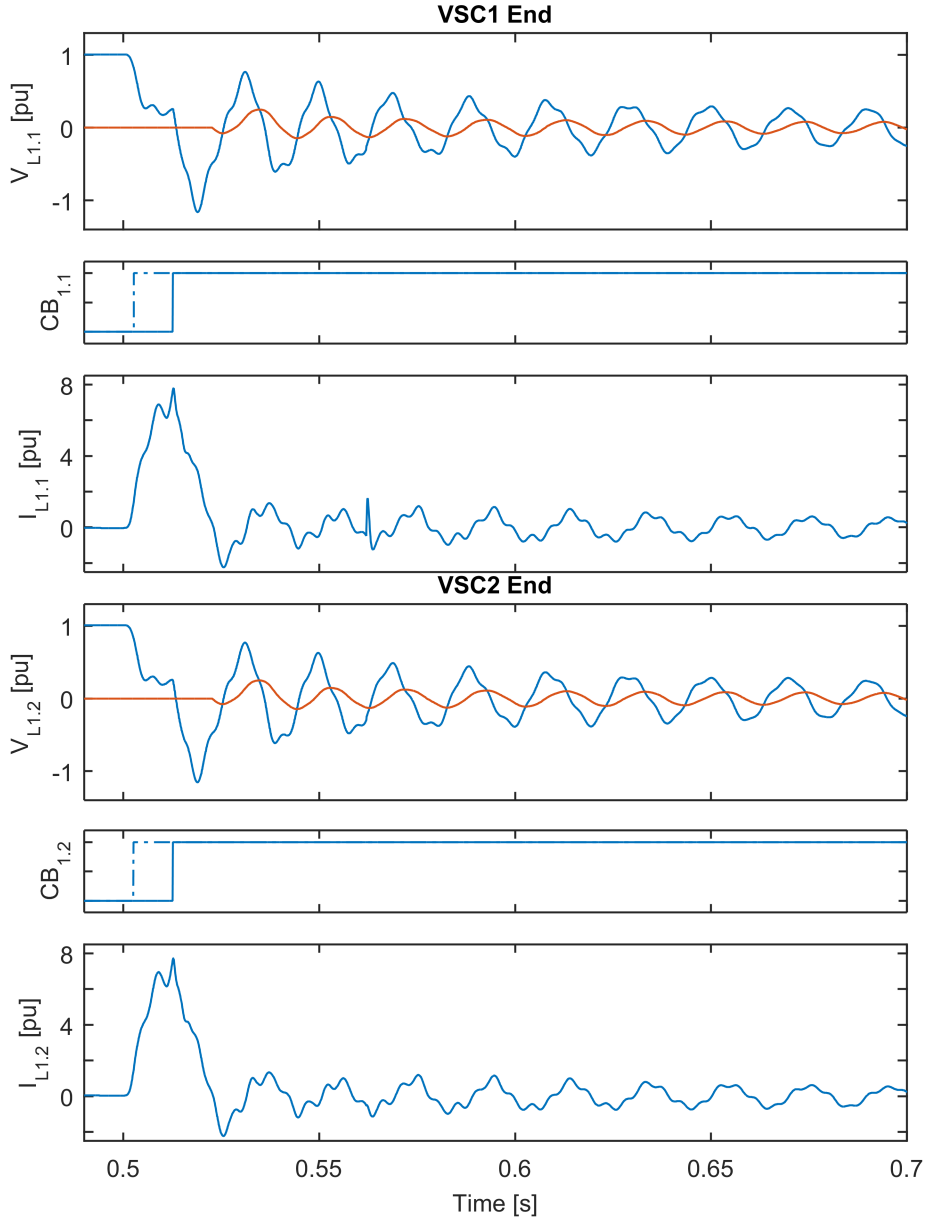

Figure 7.22: Line 1 measurements for both end of the cable. Fault placed at the mid-point of Line 1. Measurements of voltage (cable side), current and circuit breaker operation. Dashed line – triping/reclosing signal. Solid line – circuit breaker position

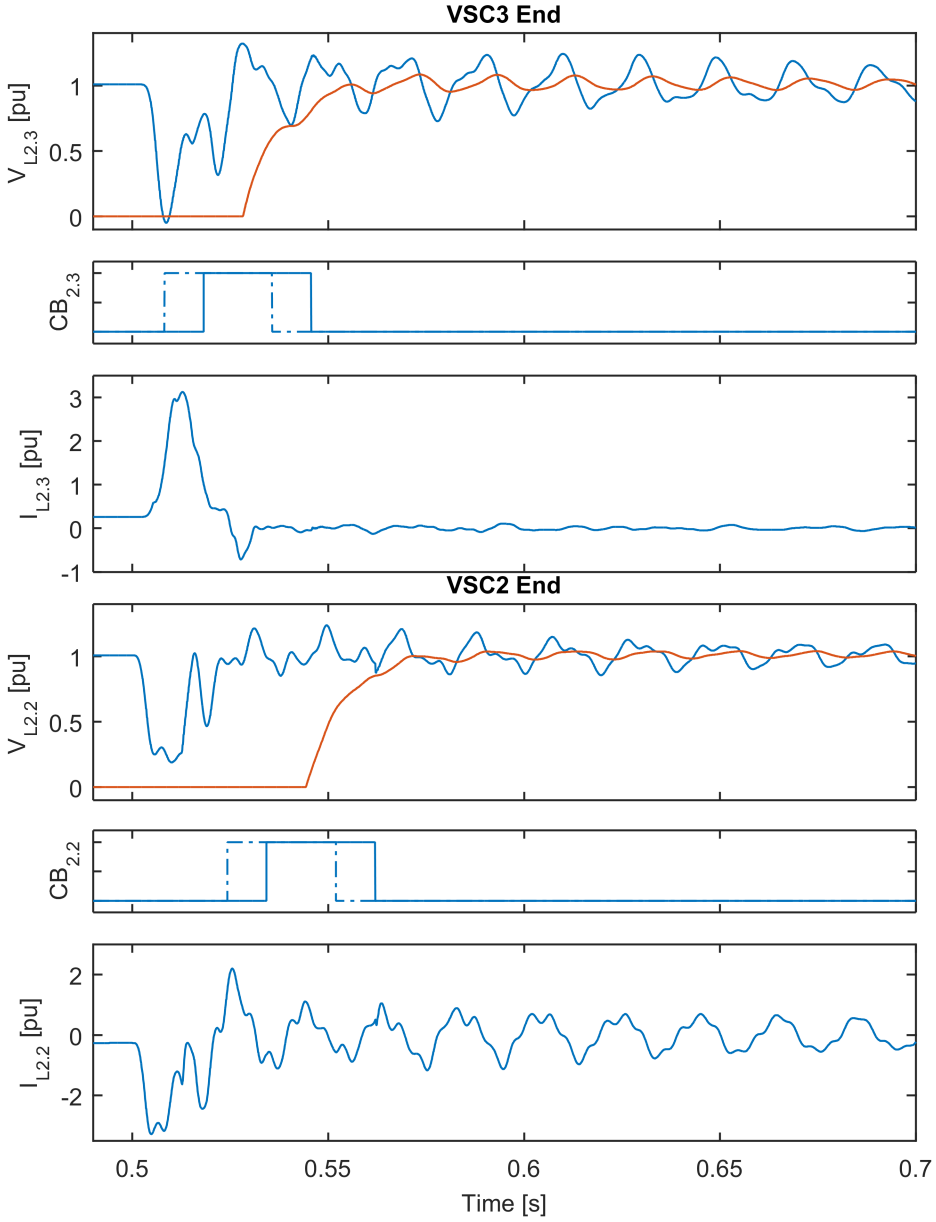

Figure 7.23: Line 2 measurements for both end of the cable. Fault placed at the mid-point of Line 1. Measurements of voltage (cable side), current and circuit breaker operation. Dashed line – triping/reclosing signal. Solid line – circuit breaker position

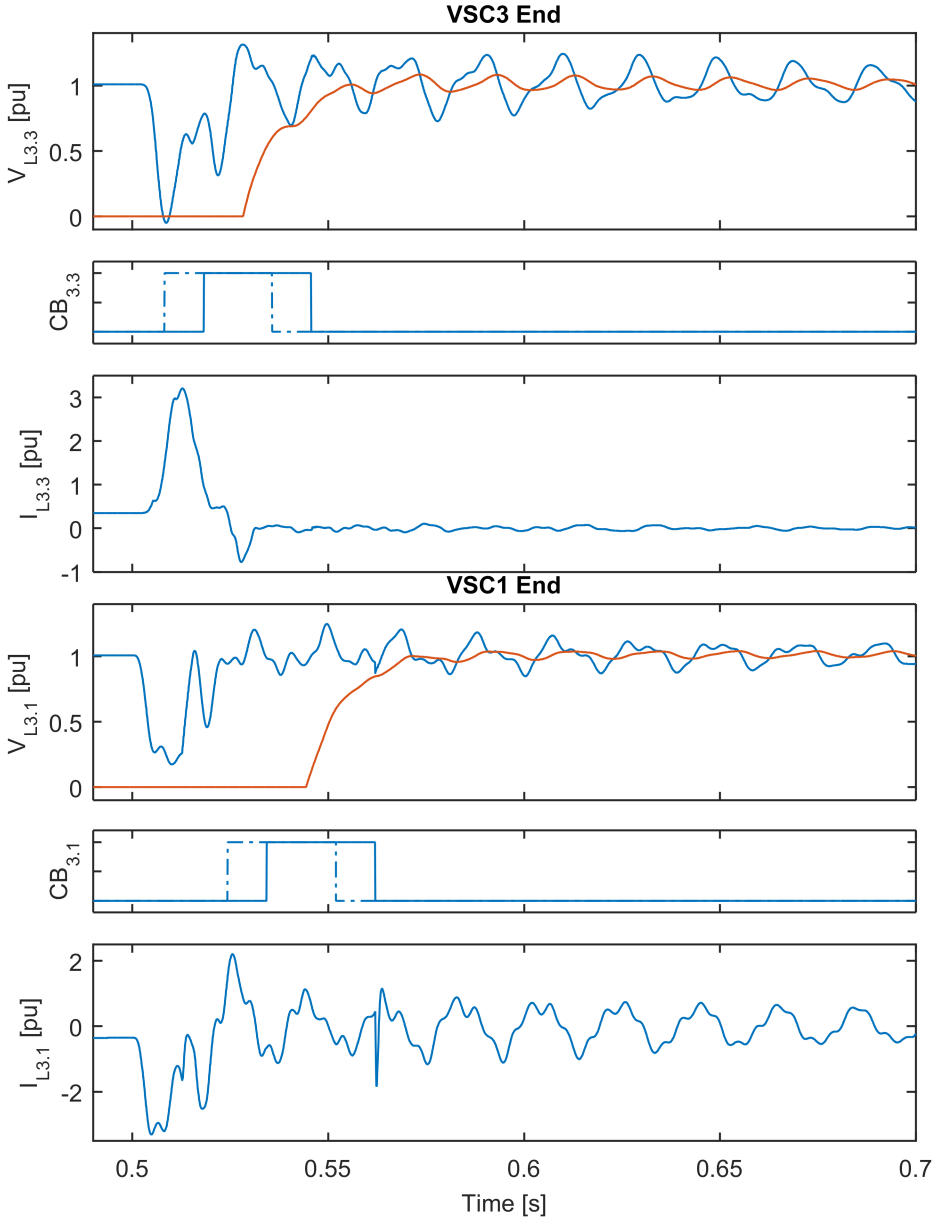

Figure 7.24: Line 3 measurements for both end of the cable. Fault placed at the mid-point of Line 1. Measurements of voltage (cable side), current and circuit breaker operation. Dashed line – triping/reclosing signal. Solid line – circuit breaker position

7.6 Full System Performance

In this section simulation results are given for a operation of the full protection system for various circuit breaker opening speeds. Circuit breakers are operated in accordance with the logic set out previously. Breaker positions for those located adjacent to each of the converters are fed into the converter to disable it should both breakers be in the open position. Each of the converters automatically re-enables itself upon the fault detection flag clearing.

To observe the effect different circuit breaker technologies have on the system ride-through three simulation cases are performed, shown in Table 7.6. The tests are performed on the three terminal system outlined in Figure 7.14, Table 7.3, Table 7.4, and Table 7.5. A copy of the test system schematic is presented in Figure 7.25 to aid readability.

Table 7.6: Initial conditions used for full system performance tests. Three cases are used to investigate the effect of different circuit breaker technologies

Case	Circuit breaker speed (T_{cb})	Representative Technology
1	100μs	Electronic Circuit Breaker
2	5ms	Hybrid Circuit Breaker
3	10ms	Mechanical Circuit Breaker

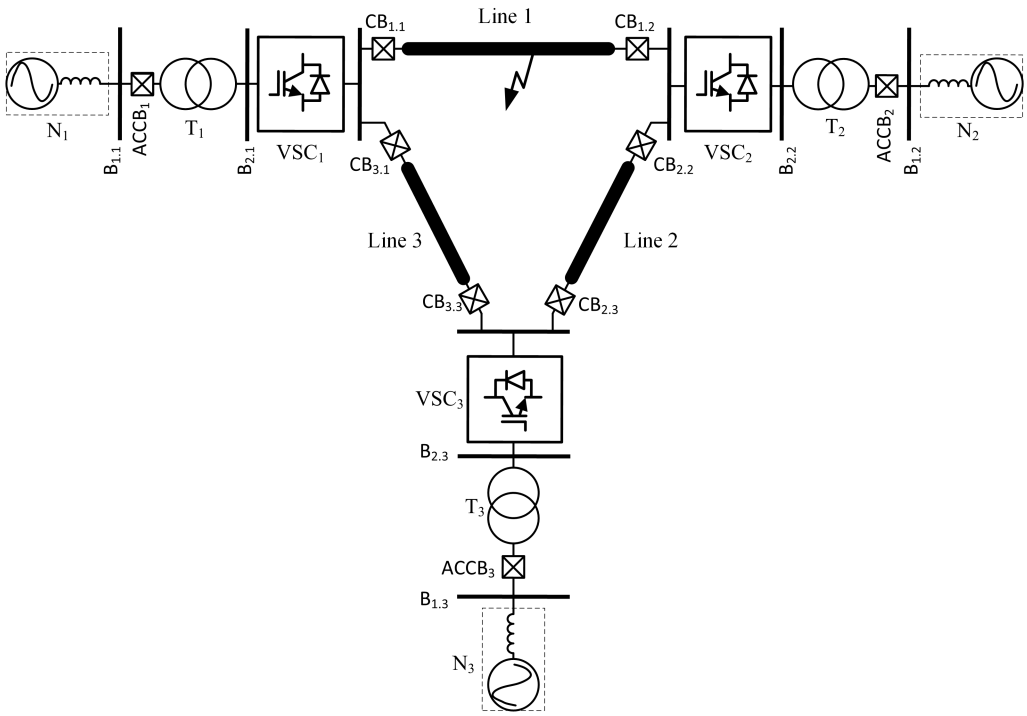

Figure 7.25: Full system performance test system

7.6.1 Case 1: Electronic Circuit Breaker

A solid state breaker is simulated by using an opening time of 100μs. Figure 7.26 shows the dc network measurements, Figure 7.27 shows three phase ac currents and converter enable signals, and Figure 7.28 shows current measurements of the three lines.

7.6.2 Case 2: Hybrid Circuit Breaker

A hybrid circuit breaker is simulated by using an opening time of 5ms. Figure 7.29 shows the dc network measurements, Figure 7.30 shows three phase ac currents and converter enable signals, and Figure 7.31 shows current measurements of the three lines.

7.6.3 Case 3: Mechanical Circuit Breaker

A mechanical circuit breaker is simulated by using an opening time of 10ms. Figure 7.32 shows the dc network measurements, Figure 7.33 shows three phase ac currents and converter enable signals, and Figure 7.34 shows current measurements of the three lines.

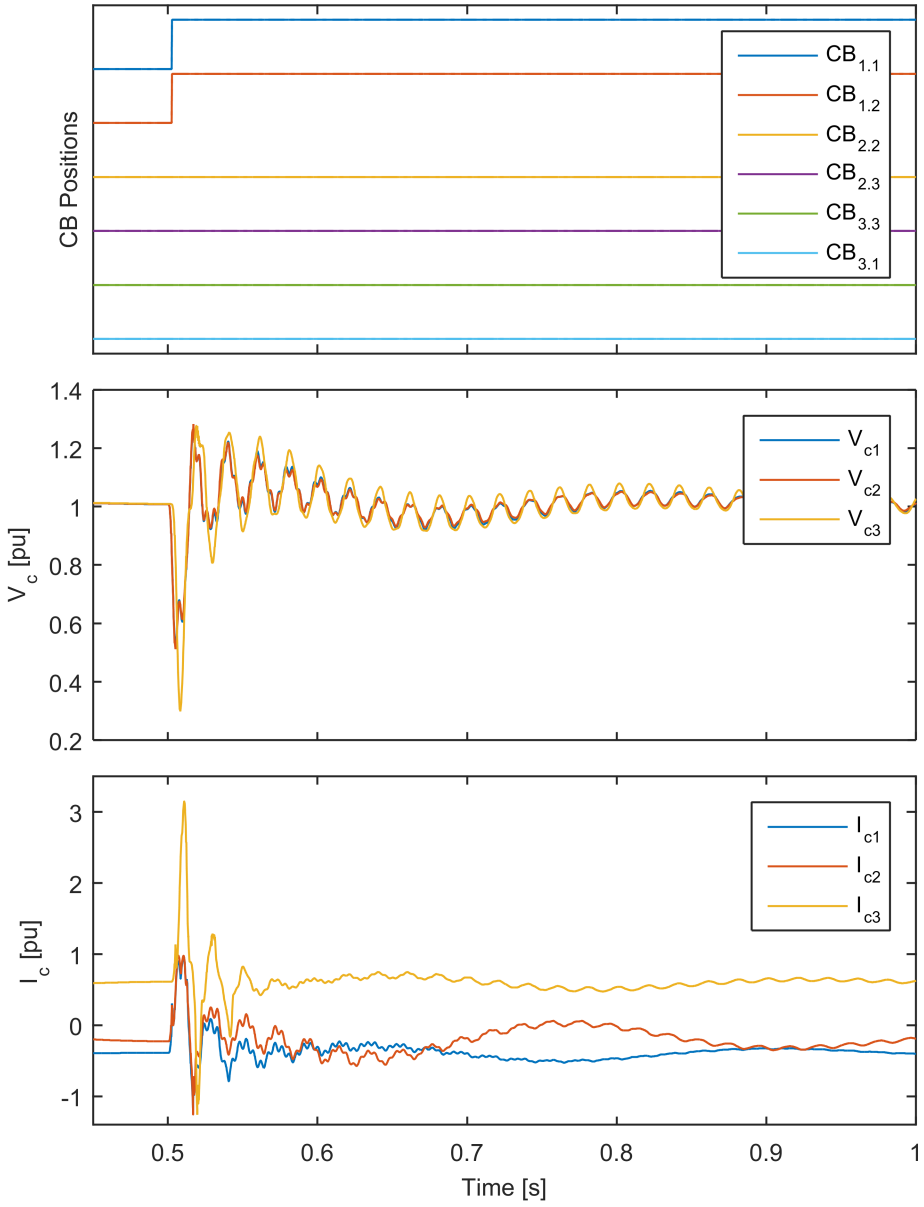

Figure 7.26: Case 1: DC network measurements for an electronic circuit breaker case ($T_{cb} = 100\mu$). Upper plot: circuit breaker positions for each end of the three cables. Centre plot: dc voltage at the terminals of each of the three converters. Lower plot: dc current from each of the three converters

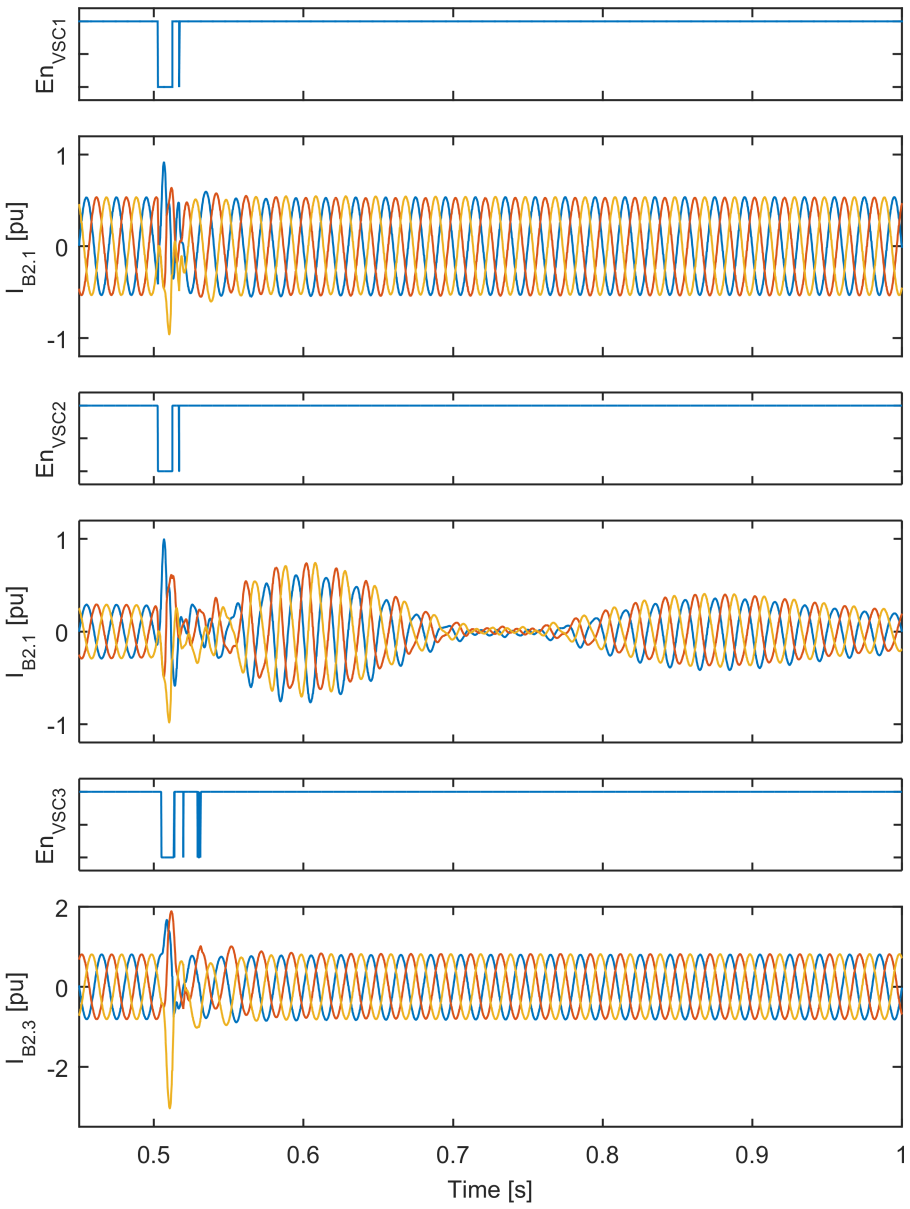

Figure 7.27: Case 1: Converter enable signals and three phase ac current measurements for an electronic circuit breaker case ($T_{cb} = 100\mu$). Upper plots: VSC 1 enable/block state and three-phase current measurements. Centre plots: VSC 2 enable/block state and three-phase current measurements. Lower plots: VSC 3 enable/block state and three-phase current measurements. (Note that current measurements are taken at the converter side of the interface transformer).

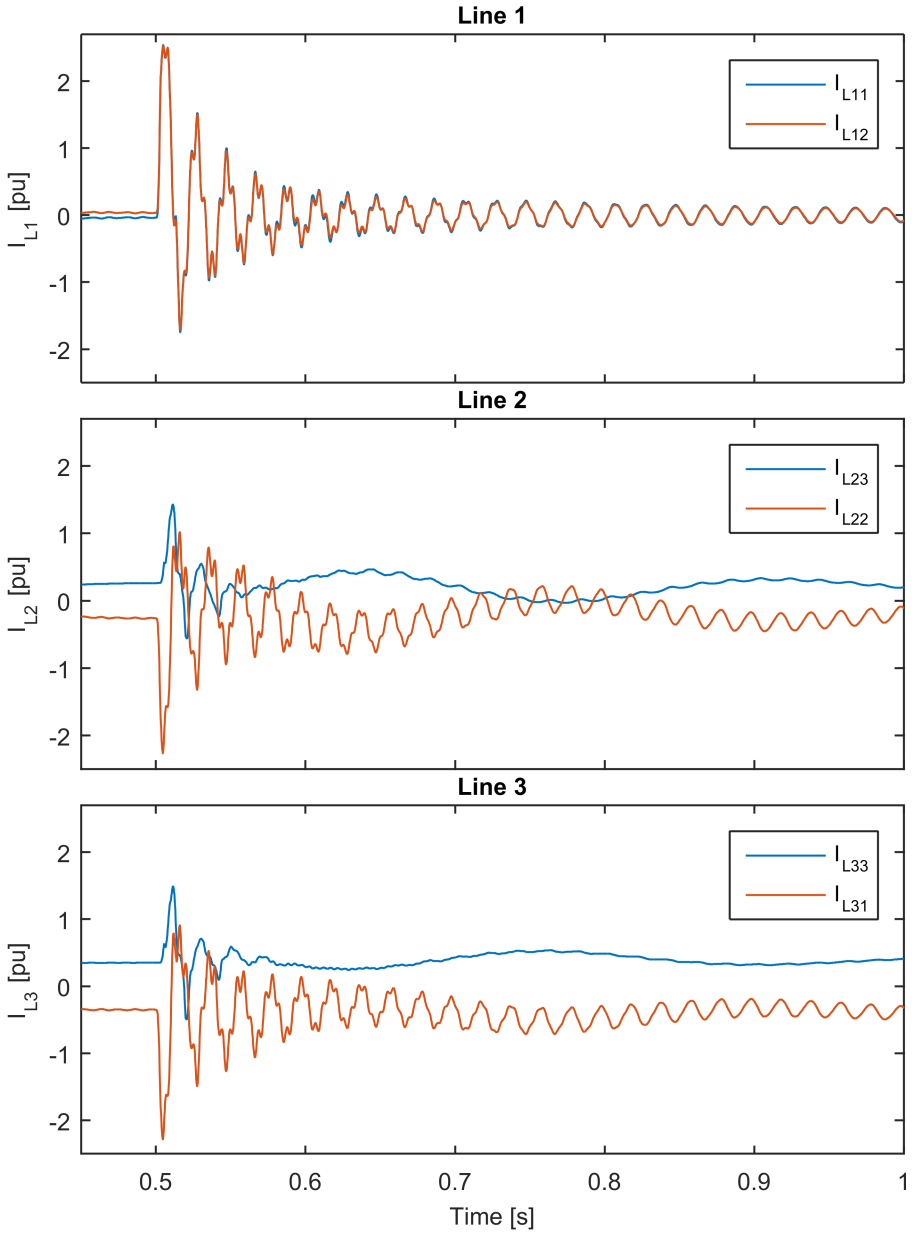

Figure 7.28: Case 1: Line current measurements for an electronic circuit breaker case ($T_{cb} = 100\mu s$). Upper plot: current measurements for VSC 1 and VSC 2 ends of cable L1. Centre plot: current measurements for VSC 2 and VSC 3 ends of cable L2. Lower plot: current measurements for VSC 3 and VSC 1 ends of cable L3

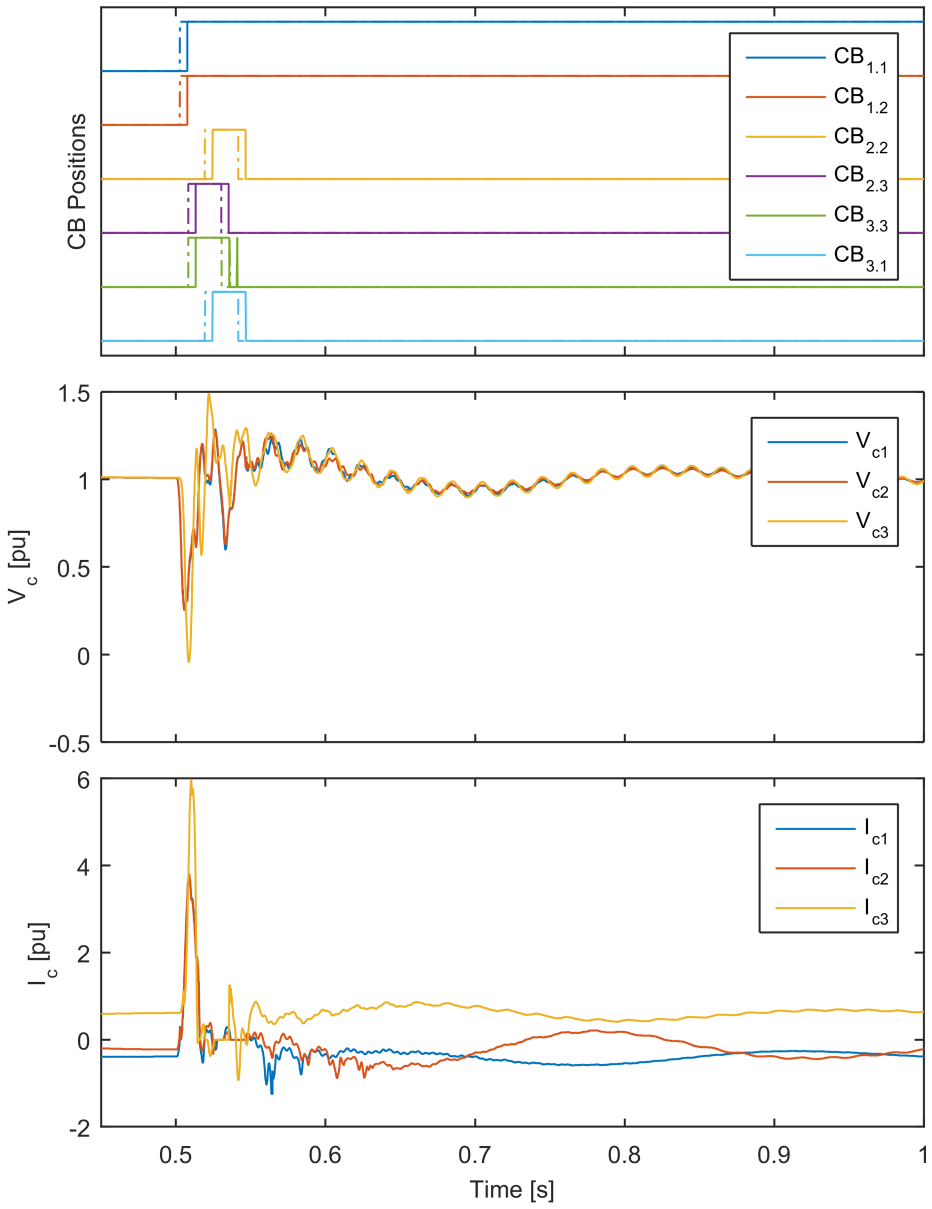

Figure 7.29: Case 2: DC network measurements for hybrid circuit breaker case (T_{cb} =5ms). Upper plot: circuit breaker positions for each end of the three cables. Mid plot: dc voltage at the terminals of each of the three converters. Lower plot: dc current from each of the three converters

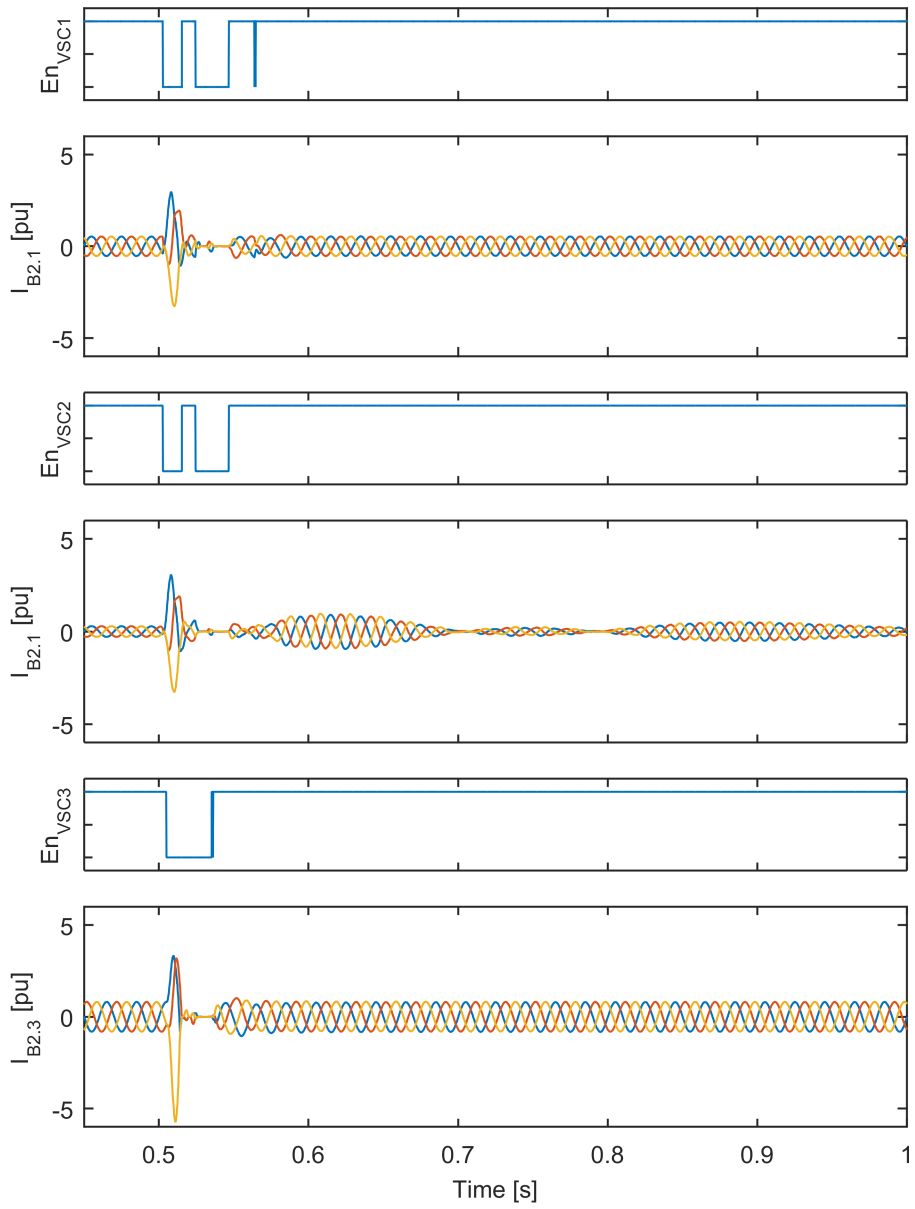

Figure 7.30: Case 2: Converter enable signals and three phase ac current measurements for hybrid circuit breaker case (T_{cb} =5ms). Upper plots: VSC 1 enable/block state and three-phase current measurements. Centre plots: VSC 2 enable/block state and three-phase current measurements. Lower plots: VSC 3 enable/block state and three-phase current measurements. (Note that current measurements are taken at the converter side of the interface transformer).

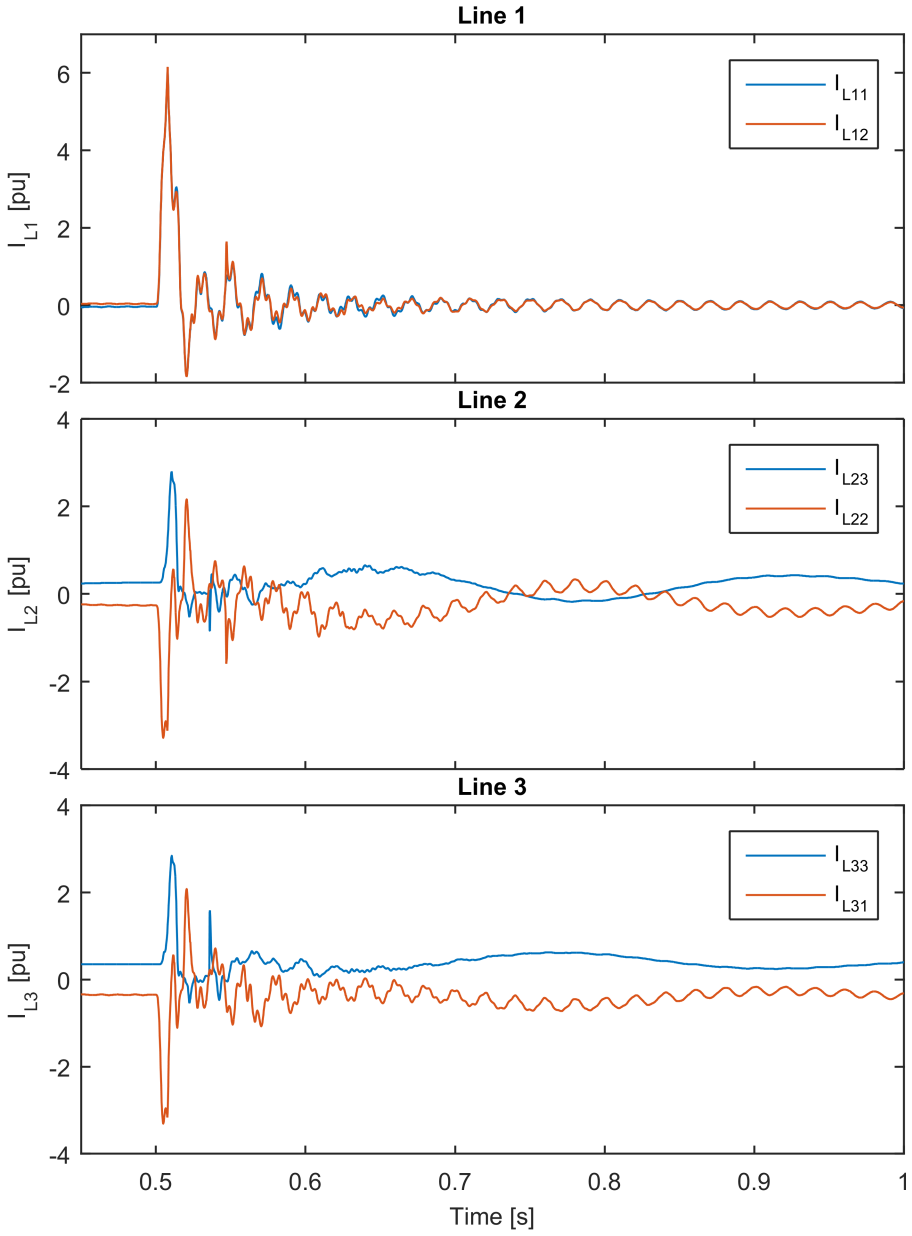

Figure 7.31: Case 2: Line current measurements for an electronic circuit breaker case (T_{cb} =5ms). Upper plot: current measurements for VSC 1 and VSC 2 ends of cable L1. Centre plot: current measurements for VSC 2 and VSC 3 ends of cable L2. Lower plot: current measurements for VSC 3 and VSC 1 ends of cable L3.

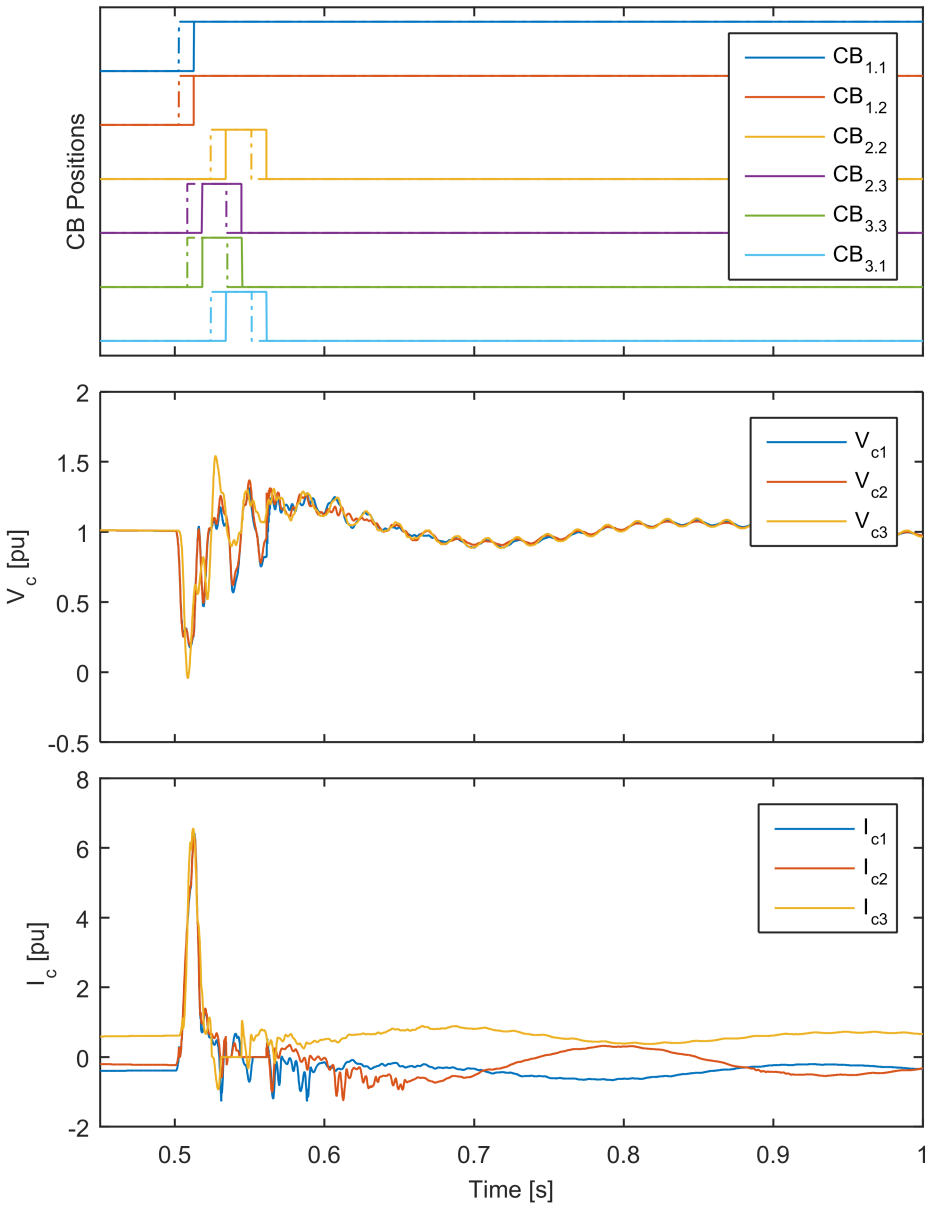

Figure 7.32: Case 3: DC network measurements for mechanical circuit breaker case (T_{cb} =10ms). Upper plot: circuit breaker positions for each end of the three cables. Mid plot: dc voltage at the terminals of each of the three converters. Lower plot: dc current from each of the three converters

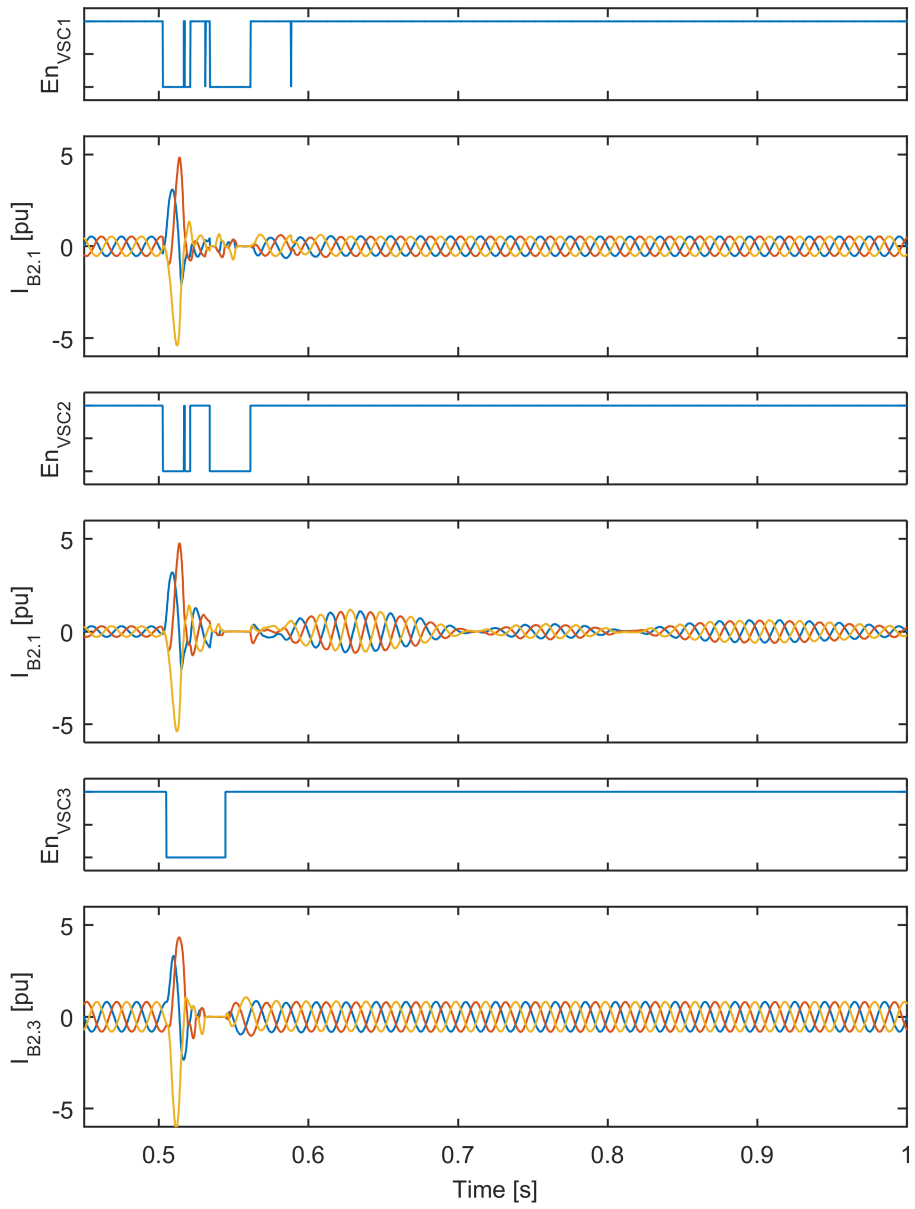

Figure 7.33: Case 3: Converter enable signals and three phase ac current measurements for mechanical circuit breaker case (T_{cb} =10ms). Upper plots: VSC 1 enable/block state and three-phase current measurements. Centre plots: VSC 2 enable/block state and three-phase current measurements. Lower plots: VSC 3 enable/block state and three-phase current measurements. (Note that current measurements are taken at the converter side of the interface transformer).

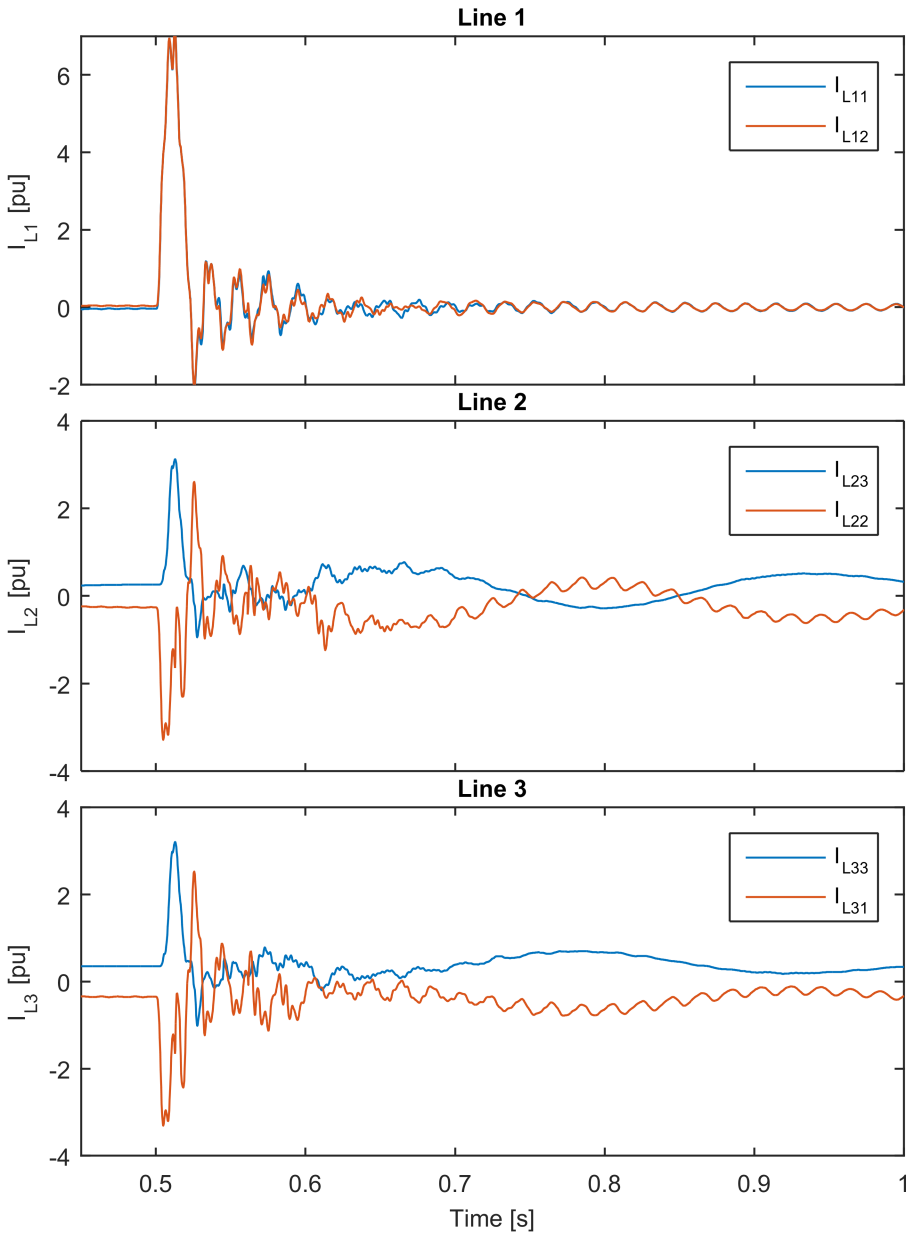

Figure 7.34: Case 3: Line current measurements for an electronic circuit breaker case (T_{cb} =10ms). Upper plot: current measurements for VSC 1 and VSC 2 ends of cable L1. Centre plot: current measurements for VSC 2 and VSC 3 ends of cable L2. Lower plot: current measurements for VSC 3 and VSC 1 ends of cable L3.

7.6.4 Analysis

Results from the full system performance test cases found that in Case 1, a system utilising electronic circuit breakers, had the best fault clearing and restart characteristics, as expected. The rapid action of the circuit breakers minimised the disturbance to the rest of the network and resulted in no other breakers tripping.

In Case 2 and 3 circuit breakers operated slower, opening 5ms and 10ms after being triggered respectively. The slower operation of the breakers led to the fault propagating through a larger area of the system. This resulted in breakers on the healthy areas of the system (Line 2 and 3) being triggered and subsequently opening. This significantly slows down the restart process; breakers must assess if the line is healthy and then actuate, both processes adding a time delay.

Hybrid circuit breakers have been developed to operate within the 5ms time range [28][27], being driven by a requirement for full system ride through, where power flow in the healthy areas of the network is not disturbed (i.e converters would not block and only circuit breakers on the faulted lines would open).

The simulation results shown in Case 2 and 3 highlight the differences and commonalities between operation of breakers at 5ms and 10ms. In both cases all converters block for a period of time and circuit breakers on healthy branches open temporary. (The simulation results show that in all three cases all three converters are temporarily blocked.) Current stress for the slower circuit breakers is higher, but only marginally (dc current in VSC 3 peaks at 6.55pu in Case 3 verses 6pu in Case 2). Chapter 6 demonstrated this can be reduced with the use of additional dc inductance.

System recovery is broadly similar between Case 2 and 3. There is a longer delay between the fault occurring and the system re-establishing power flow in Case 3. However, this is marginal when compared to the overall restart time, which is dominated by clearing fault current and reconfiguring breakers (see Figure 7.35).

A summary bar chart of key fault ride-through indicators is given in Figure 7.35 (raw data may be found in Table 7.36). The key measurements used are: time for converters to re-enable, time for ac current to stabilise and time for all healthy breakers to re-close. In the case of the electronic circuit breakers the re-close time is zero, as no healthy breakers are tripped. The chart highlights that the difference between Cases 2 and 3 are not as large as may be expected. With the mechanical breakers, fault ride through is slower than that of the hybrid system by any of the metrics used, but only be approximately 12ms. The system is able to return to its pre-fault condition within approximately 65ms, in line with the fastest ac breakers. In each

of the three cases there is a minimum overhead before the system begins to operate again of approximately 30ms, indicating that disturbance to power flow is caused no matter how fast breakers can operate.

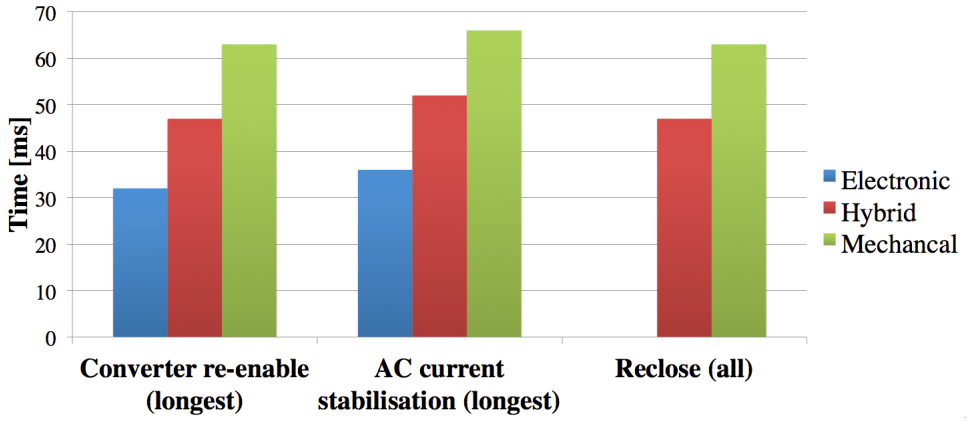

Figure 7.35: Key performance metrics of a full system test. Left: time that all converters are re-enabled. Centre: longest time for converter ac current to re-stabilise to pre-fault conditions. Right: time for circuit breakers in all healthy branches to re-close. All times given are relative to the fault occurring

		Case 1 Electronic	Case 2 Hybrid	Case 3 Mechanical
Circuit breaker operation time		100us	5ms	10ms
		[ms]	[ms]	[ms]
Converter enable	VSC 1	21	47	63
	VSC 2	15	47	60
	VSC 3	32	37	43
	All	32	47	63
	1.1	o	o	o
	1.2	o	o	o
Circuit breaker reclose	2.2	c	47	63
	2.3	c	34	47
	3.3	c	34	47
	3.1	c	47	63
	Longest	c	47	63
AC current stabilised	VSC 1	32	52	66
	VSC 2			
	VSC 3	36	47	53
	Longest	36	52	66

Figure 7.36: Key performance metrics of a full system test. All times given are relative to fault occurrence. Converter enable: time period before converter becomes re-enabled. Circuit breaker re-close: time period befor circuit breaker re-closes; o – opens and does not re-close, c – remains closed throughout i.e. does not trip. AC current stabilisation: time for converter ac current to return to pre-fault level; note that VSC 2 is not measured as it regulates voltage and therefore fluctuates overa long time period.

7.7 Conclusion

In this chapter, methods of protecting the dc network have been explored. The lower cost dc disconnector solution, that uses ac breakers to clear fault currents, suffers from the long

decay times of dc currents within the dc network. This technique may be applicable for low capacity/small networks, where loss of power exchange for an extended time is acceptable but is unlikely to be feasible in large/high capacity networks. DC breakers placed within the network provide a faster response and do not require ac breakers to open, which reduces the restart time.

Chapter 4, Section 4.3 demonstrated that the converter was able to sustain fault currents for extended periods of time and the circuit breakers were not required to operate before fault current reached exceeded diode current rating. The critical time for converter protection is then a function of the bypass thyristors used, allowing slower, lower cost breaker solutions to be considered.

The communication-less system, based only on local measurements, explored in [91], was used as a basis for the protection strategy. This was extended to include fault detection and protection algorithms and the scope for circuit breakers of varied operational speeds. This allowed assessment of the relative time overheads of protection and circuit reconfiguration and circuit breaker operation time itself. The studies highlighted that the time overhead of protection mechanisms (fault detection, dissemination and circuit reconfiguration) dominated the system response. Faster hybrid circuit breakers provided only a marginal increase in performance over slower, cheaper mechanical alternatives. Given that recent publications has indicated the superior current handling performance of mechanical breakers these would appear a favourable option in realising multi-terminal HVDC networks [79].

Further investigation is required to ensure adequate ride-through performance for different system conditions. Large parametric studies are required to highlight difficulties in restart that may occur when the network becomes more complex, lines are extremely long, power loading of the converters is high, and fault cases where converters may be disconnected from the network all together.

Chapter 8

Conclusion

8.1 General Conclusion

The increasing penetration of wind power requires reinforcement of the current network as well as new interconnection to mitigate fluctuations in power output due to intermittent generation. Proposals for meshed HVDC networks to connect large geographical areas, and integrate individual connections to offshore wind-farms, could be used to make more efficient use of assets and bring generation to a wider variety markets.

HVDC is key to the construction of such a meshed system, in particular the voltage source converter. While capable of readily being integrated into a networked system, these converters are susceptible to dc side faults. The resulting high current experienced by the converter can cause damage to the internal components. At the same time power transmission throughout the network is also lost. With converter capacities reaching 1000MW and more, it will not be acceptable to lose power throughput in large scale networks for significant periods of time. Networks must therefore have adequate protection so that the it may tolerate faults when they occur, without causing major disruption to the larger (ac) system.

DC breakers that have been developed in the last five years have been driven by the requirement to clear faults before healthy parts of the network are affected. New topologies have allowed breakers to operate in extremely short periods of time: in the region of 2ms - 5ms. To achieve this has required highly complex topologies, with large numbers of semiconductor components and high cost projections. To make the economic case for meshed networks the cost of circuit breakers needs to be reduced.

This thesis has set about determining what implications different circuit breaker topologies have on fault recovery of an HVDC network. Its aim was to examine what influences the

required speed of the circuit breakers and what functionality, if any, is lost when slower circuit breakers are used.

Chapter 2 introduced the converter technology available for HVDC systems. Conventional and fault blocking converters were discussed. The average MMC model used within the thesis was described and justified as fit for purpose. Chapter 3 reviewed the mechanisms behind dc faults. It described why HB-MMC is susceptible to high fault currents and how protective devices may be used successfully to stop the most fragile components being damaged. The converter was analysed to demonstrate the limiting factors on maximum current draw during fault.

In Chapter 4 the current stress placed on the converter and dc breaker were assessed through parametric simulation cases. Quantitative methods of measuring the stress were developed so that the performance benefits of could be clearly contrasted between cases. Alterations to passive components within the converter, such as transformer impedance, was shown to give a substantial influence over the fault current which resulted. The impact of such measures have during normal operating conditions was analysed. It was shown that the reduction in fault current came at the expense of higher converter losses.

In Chapter 5 the state of the art dc breaker topologies and developments were reviewed. Mechanical resonant/mechanical topologies showed robust characteristics and have proven track records when used as commutation devices within LCC systems. More recent topologies have showed improvements in operating speed, but with increasing complexity and cost. Circuit breaker cost and complexity are related to the speed, peak current and energy dissipation requirements. Empirical results demonstrated that circuit breaker current stress could be reduced with additional inductance placed on the dc side of the converter. In Chapter 6 the interaction between these was explored and a mathematical analysis demonstrated how increased inductance influences energy dissipation of the circuit breaker.

In Chapter 7 the overall protection strategy of a multi-terminal network was considered. The various approaches to clearing faults and reconfiguring the system were assessed. Areas of the literature which have not been explored thoroughly were identified and a test system created. Algorithms to drive of fault detection, converter blocking and circuit opening and re-closing logic were designed and verified individually. Finally, the full protection system was demonstrated through three test cases, representing each of the three key breaker technologies identified. The results showed that more complex and expensive hybrid circuit breakers did not lead to a perfect system ride through, as suggested within the current literature. Power flow was disturbed throughout the network for a period of time for each of the breaker technologies

replicated. The system did take a longer time to re-establish pre-fault power flow conditions when equipped with slower mechanical circuit breakers. However, when compared to the overhead that was present in all three cases the increase marginal. Even in the slowest case the system recovered within 80ms that HVAC breakers take to clear faults.

The studies performed within this thesis have demonstrated that while fast dc breakers do bring performance benefits they do not provide a 'perfect' system – healthy areas of the network are affected by the fault and power throughput is temporarily lost. In this case, the requirement Choice of circuit breaker depends heavily of external system requirements (that of the ac network) and cost optimisation. For example, circuit breaker current stress can be reduced at the expense of higher energy dissipation; cheaper, mechanical breakers may be used if a slightly longer re-start time can be tolerated. To provide an optimal solution more information of component costs are required, which are currently unavailable in the public domain.

8.2 Author's Contribution

The authors contribution can be summarised as follows:

- Converter and circuit breaker stress mechanisms have been identified and quantitative methods of evaluating case studies have been found. These have been used to identify variables at the disposal of the converter and system designer that may reduce the stress on both the converter and dc breaker.

- A method of approximating the effect increased dc side inductance has on circuit breaker stress has been developed. This analytical approach has shown that there is a non-linear correlation between energy dissipation and peak current which has not been previously observed. This tool allows approximations to be developed quickly during the initial design iterations. It also can also be used to ensure that the design is not inadvertent operating at a local maxima in terms of energy dissipation with respect to additional inductance.

- A full HVDC, multi-terminal simulation model has been built that in includes measurement driven logic to operate the protection system. By including all features of the protection system such as detection, discrimination and modelling actuation time for open and re-closing of breakers a better understanding of the nature of the problem has been given. This system can then be extended to evaluate different system topologies and operating conditions, as well as be extended to include ac inertia and frequency swings.

- The requirements for fast-acting dc breakers has been evaluated. It has shown that the case of these is not clear. Choice of technology is part of a wider system level optimisation. It has been demonstrated that converters can survive fault currents for extended period of time if required, opening the possibility for slower circuit breakers to be used. The impact on fault ride-through between hybrid and mechanical circuit breakers is not the difference between total system collapse and perfect system ride-through. Fault detection and selective protection can cause lead to as significant time cost as the breakers themselves. Fault ride-through, therefore, must be examined first at a high level, observing the interactions between different system components.

8.3 Suggestions for Further Work

The research provided here has shown that there are many options open for HVDC network protection. Converters are able to sustain fault currents for periods of time longer than assumed at present. This allows a wider variety of protection mechanisms, and combination of, to be investigated.

- Ultimately, if the converter can tolerate fault currents for periods of several cycles then it is the requirements of the ac network which dictate the HVDC system's performance during faults. The length of time for which power may be lost on a temporary basis is key. This should be investigated at a larger system level for different case studies, where penetration of converter connected generation is both high and low. By modelling the ac networks with rotating machines the frequency swings can be evaluated. The implication rapid changes in power throughput to the dc network has on ac protection, for instance rate-of-change-of-frequency triggers, can then be investigated.

- Further investigation into the role converter topology plays on fault current levels, both steady-state and transiently. Topologies such as the alternate arm converter may have fundamentally different interactions which may increase or decrease current stress.

- Hybrid protection topologies should be investigated, where several protection mechanisms may be used. The combination of blocking converters, low voltage-dc breakers and sub-networks with electronic circuit breakers providing firewalls may provide the required performance, but with a substantially lower cost than large numbers of breakers placed throughout the system.

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